1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB

PVT

REV. A

LAST_MODIFIED=Mon Jan 10 13:11:06 2011

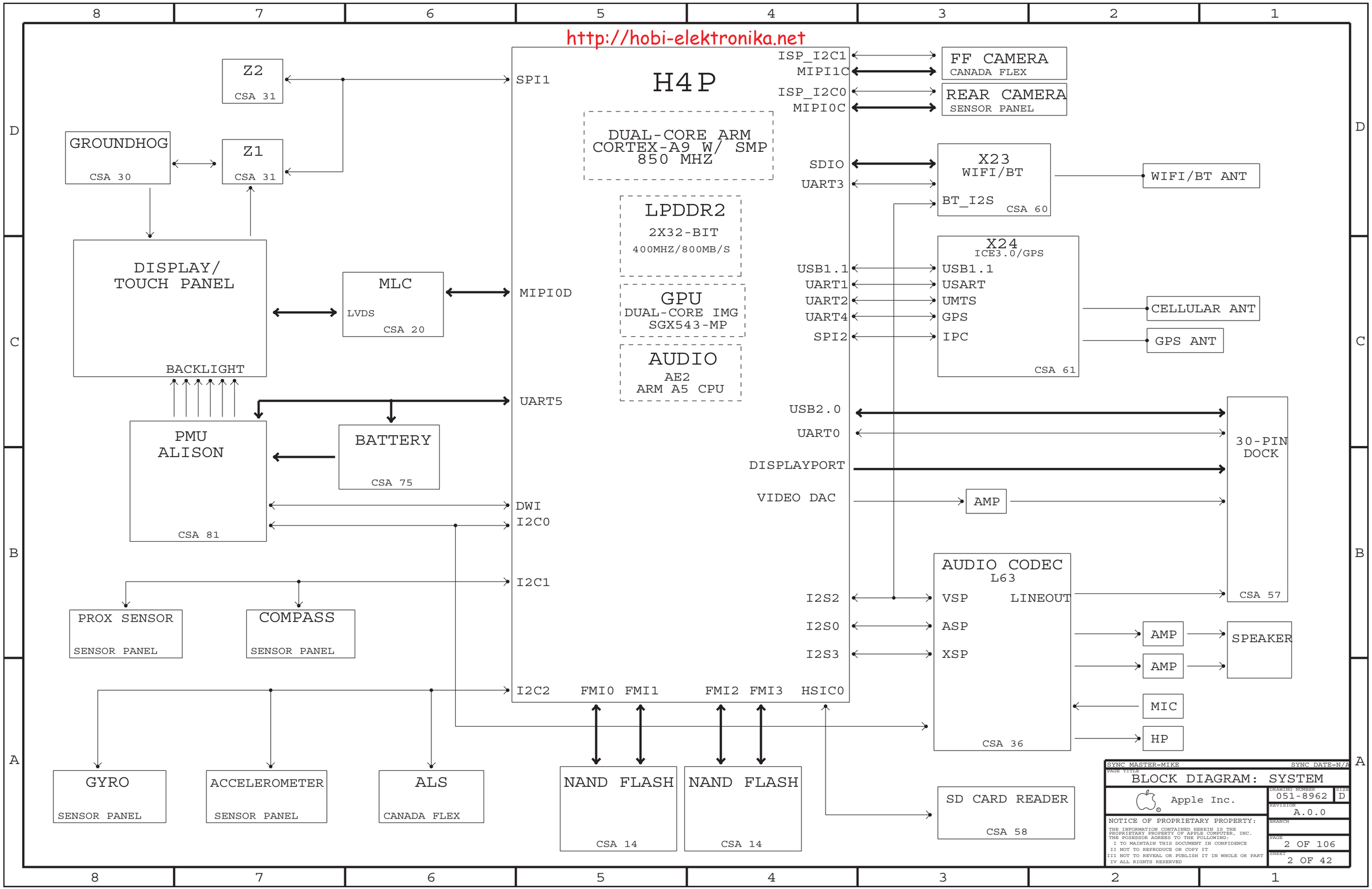
REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001052699	PRODUCTION RELEASED	2011-01-10

_DRAWING
TITLE=BACH
ABBREV=DRAWING

DRAWING TITLE: CHOPIN MLB

Apple Inc.

DRAWING NUMBER: 051-8962 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 106
SHEET: 1 OF 42



SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE

BLOCK DIAGRAM: SYSTEM

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD

BKLT_PLL

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP
JTAG_TAP_NOT

SPEAKER
INTERNAL_MIC

PORTRAIT_DOCK

MLC_DEV
MLC_PROD

K93
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH,CHOPIN_AUDIO,MLB,K94	SCH1	
820-3069	1	PCBF,CHOPIN_AUDIO,MLB,K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE,GRAPE,MLB,K93/K94	FENCE1	
806-1397	1	CAN,GRAPE,MLB,K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE,CPU,MLB,K93/K94	FENCE2	
806-1399	1	CAN,CPU,MLB,K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE,NAND,MLB,K93/K94	FENCE3	
806-1401	1	CAN,NAND,MLB,K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DFC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DFC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DFC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
BOM TABLE

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
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SHEET 3 OF 42

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION

U0652
H4P-512MB
BGA
SYM 11 OF 12
SC58940X01-A030

AU14 AU15 AU16 AU17 AV1 AV2 AV3 AV4 AV5 AV6 AV7 AV8 AV9 AV10 AV11 AV12 AV13 AV14 AV15 AV16 AV17 AV29 AV33 AV34 AW1 AW2 AW4 AW23 AW33 AW34 AY1 AY2 AY3 AY4 AY20 AY22 AY24 AY30 AY31 AY32 AY33 AY34 B1 B2 B7 B9 B10 B12 B13 B15 B17 B18 B20 B22 B23 B28 B29 B30 B32 B33 B34 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C23 C27 C29 C32 C33 D1 D3 D5 D7 D9 D11 D13 D15 D16 D23 D27 D32 E1 E2 E3 E4 E6 E8 E10 E12 E14 E16 E17 E18 E19 E20 E21 E22 E23 E25 E26 E27 E28 E30 E31 E32 E34 F1 F2 F3 F5 F19 F20 F21 F22 F23 F25 F26 F29 F30 F31 F32 G1 G3 G4 G7 G8 G9 G10 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G25 G28 G29 G30 H1 H2 H3 H5 H7 H8 H10 H12 H14 H16 H18 H20 H22 H24 H25 H29 H30 J1 J2 J3 J4 J7 J9 J11 J13 J15 J17 J19

VSS VSS

=PP1V1_PLL_H4

R0620 0.00 0% 1/32W MF 01005
C0651 0.01UF 10% 6.3V X5R 01005
PP1V1_PLL4_F
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

R0621 0.00 0% 1/32W MF 01005
C0648 0.01UF 10% 6.3V X5R 01005
PP1V1_PLL3_F
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

R0622 0.00 0% 1/32W MF 01005
C0646 0.01UF 10% 6.3V X5R 01005
PP1V1_PLL2_F
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

R0623 0.00 0% 1/32W MF 01005
C0644 0.01UF 10% 6.3V X5R 01005
PP1V1_PLL1_F
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

R0624 0.00 0% 1/32W MF 01005
C0608 0.01UF 10% 6.3V X5R 01005
C0660 56PF 5% 6.3V NPO-COG 01005
PP1V1_PLL0_F
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

=PP1V1_USB_H4
C0643 0.22UF 20% 6.3V X5R 0201

=PP1V2_HSIC_H4
C0642 0.01UF 10% 6.3V X5R 01005
C0641 0.01UF 10% 6.3V X5R 01005

JTAGSEL
0 - PARALLEL
1 - DAISY-CHAIN (FOR USE WITH 5-WIRE JTAG)
PER RADAR #6755237

HSIC_VDD121 D25 HSIC_VDD122 D24 HSIC_DVDD F24 PLL0_AVDD11 C19 PLL1_AVDD11 C20 PLL2_AVDD11 C21 PLL3_AVDD11 C18 PLL4_AVDD11 C17 PLL_USB_AVDD11 C22 MIPI0D_VDD11_PLL AR20 MIPI1D_VDD11_PLL AT19 USB_DVDD C28 USB_VDD330 H27 H28

TP_HSIC1_AP_DATA A26 HSIC1_DATA
TP_HSIC1_AP_STB A27 HSIC1_STB
NC_HSIC2_AP_DATA C26 HSIC2_DATA
NC_HSIC2_AP_STB D26 HSIC2_STB
SYM 1 OF 12
U0652
H4P-512MB
BGA
JTAG_SEL N31 JTAG_SEL
NC_JTAG_AP_RTCK M30 JTAG_TRTCK
JTAG_AP_TRST_L N29 JTAG_TRST*
JTAG_AP_TDO M31 JTAG_TDO
JTAG_AP_TDI M32 JTAG_TDI
JTAG_AP_TMS N32 JTAG_TMS
JTAG_AP_TCK N30 JTAG_TCK
AP_TESTMODE P29 TESTMODE
M28 FUSE1_FSRC
AP_TST_STPCLK P33 TST_STPCLK
TP_AP_TST_CLKOUT P34 TST_CLKOUT
AP_FAST_SCAN_CLK T32 FAST_SCAN_CLK (FOR IC TESTER)
AP_HOLD_RESET P31 HOLD_RESET (0=NORMAL)
RST_AP_1V8_L P32 RESET*
AP_CFSB W30 CFSB
G11 DDR0_CKEIN
R7 DDR1_CKEIN

HSIC_VSS121 C25 HSIC_VSS122 C24 HSIC_DVSS E24 PLL0_AVSS11 D19 PLL1_AVSS11 D20 PLL2_AVSS11 D21 PLL3_AVSS11 D18 PLL4_AVSS11 D17 PLL_USB_AVSS11 D22 MIPI_VSS_0 AN10 MIPI_VSS_1 AN11 USB_DVSS D28 USB_VSSA0 H26 USB_VSSAC J26

=PP1V1_PLL_USB_H4
R0625 0.00 0% 1/32W MF 01005
C0652 0.01UF 10% 6.3V X5R 01005
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

PP1V1_MIPID_PLL_F
FL0610 80-OHM-0.2A-0.4-OHM 0201-1 =PP1V1_MIPI_PLL_H4
C0661 56PF 5% 6.3V NPO-COG 01005
C0654 0.1UF 10% 6.3V X5R 201
C0655 1UF 10% 6.3V CERM 402

=PP1V1_USB_H4
C0627 0.01UF 10% 6.3V X5R 01005

=PP3V3_USB_H4
C0640 1UF 10% 6.3V CERM 402
C0630 0.01UF 10% 6.3V X5R 01005

WDOG P30 RST_PMU_IN
XI0 A18 XTAL_24M_I
XO0 A19 XTAL_24M_O
R0655 1.00M 1% MF 01005/32W
R0640 22 5% 1/32W MF 01005
CRITICAL
Y0602 24.000MHZ-16PF-60PPM SM-2
24M_O
C0613 22PF 5% 16V CERM 01005
C0607 22PF 5% 16V CERM 01005

USB11_DP A22 USB_FS_D_P
USB11_DM A23 USB_FS_D_N
USB_DP A29 USB_D_P
USB_DM A28 USB_D_N
USB_ANALOGTEST G26 NC_USB_ANALOGTEST
USB_VBUS F27 USB_AP_VBUS
USB_ID F28 NC_USB_ID
USB_BRICKID G27
USB_REXT A21 USB_REXT

R0651 100K 5% 1/32W MF 01005 PPVBUS_USB
DZ0600 GDZT2R5.1B GDZ-0201
R0642 44.2 1% 1/20W MF 201
NOTE: PAGE 4608 H4P UM V0.83
USB_BRICKID

=PP1V8_H4
R0645 100K JTAG_AP_TCK
R0646 100K JTAG_AP_TMS
R0647 100K JTAG_AP_TDI
DEVELOPMENT_JTAG_TAP
R0662 100K

=PP3V3_USB_H4
R0617 10K 1% 1/32W MF 01005
R0632 100K 1% 1/32W MF 01005
RST_AP_L
NOSTUFF XW0604 SHORT-01005
AP_CFSB
R0688 42.2K 1% 1/32W MF 01005
C0618 1000PF 10% 16V X7R 201
AP_DDR1_CKEIN_1V2
NOSTUFF XW0605 SHORT-01005
AP_DDR1_CKEIN
R0689 82.5K 1% 1/32W MF 01005

SYNC MASTER=JAMES	SYNC DATE=N/A
PAGE TITLE	AP: MAIN
Apple Inc.	DRAWING NUMBER 051-8962 SIZE D
	REVISION A.0.0
	BRANCH
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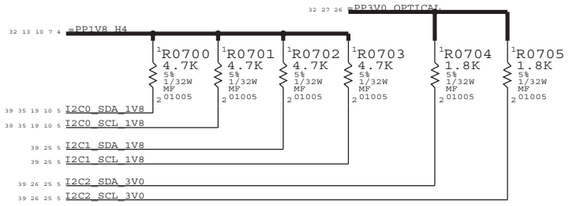
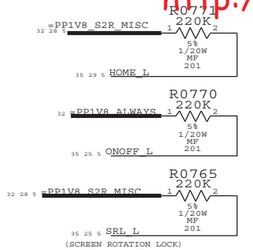
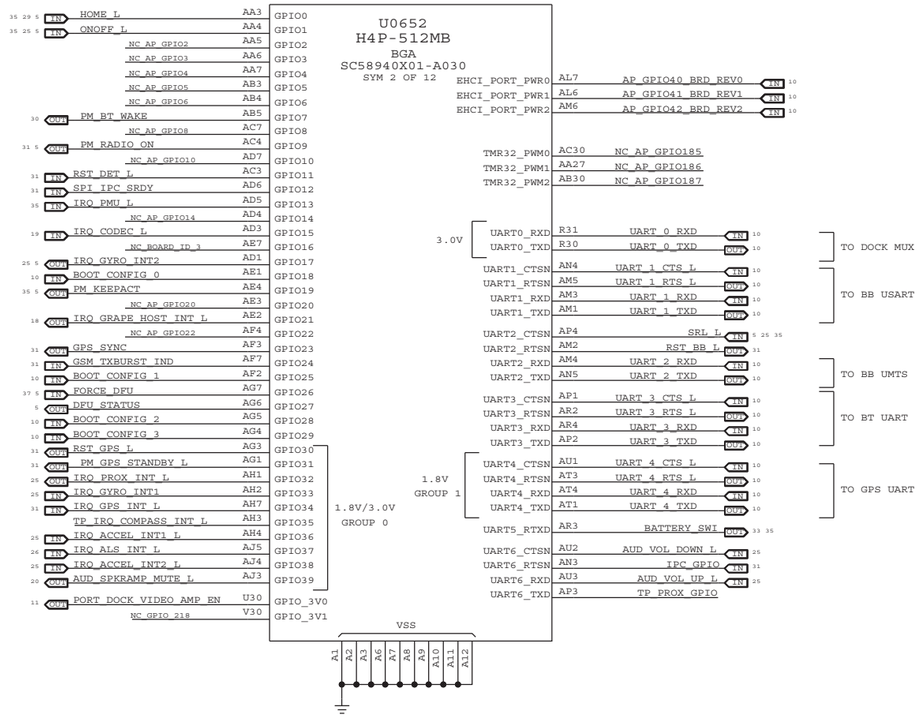
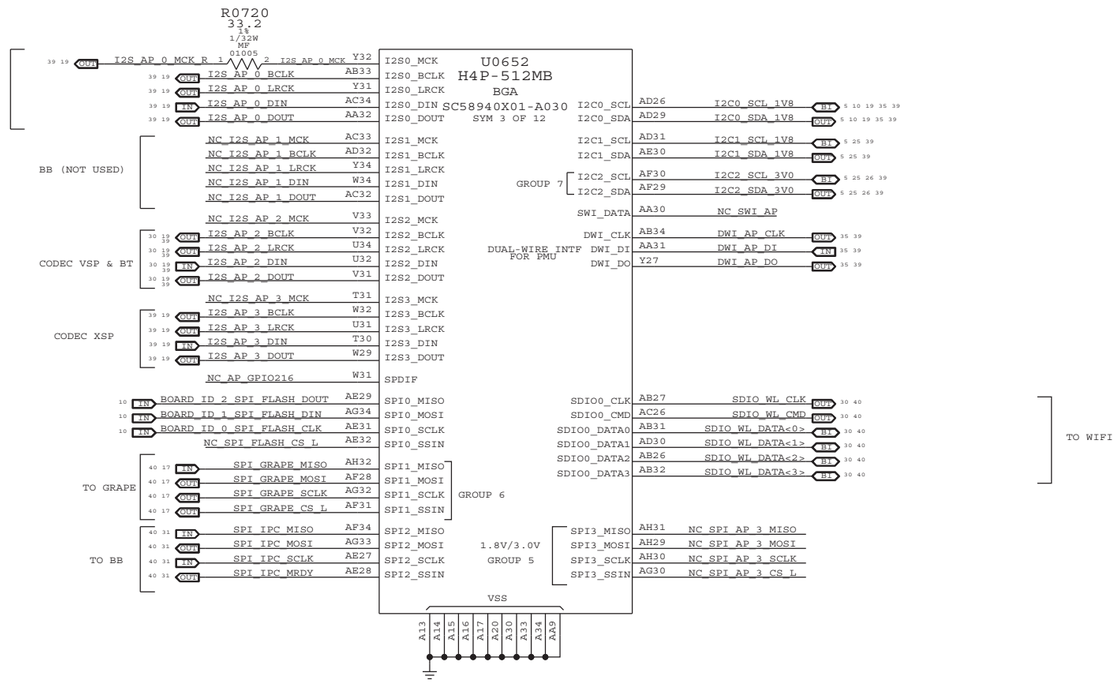
	SHEET 4 OF 42









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PAGE TITLE: AP: I/Os	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
	BRANCH:
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U0652
H4P-512MB
BGA
SYM 12 OF 12
SC58940X01-A030

VSS

=PPIO_NAND_H4

R0830 R0831 R0832 R0833 R0834 R0835 R0836 R0837
100K 5% 1/32W MF 01005

F1CE0_L
F1CE1_L
F1CE2_L
F1CE3_L
F0CE0_L
F0CE1_L
F0CE2_L
F0CE3_L

=PPIO_NAND_H4

R0860 R0861 R0862 R0863 R0864 R0865 R0866 R0867
100K 5% 1/32W MF 01005

F1CE4_L
F1CE5_L
F1CE6_L
F1CE7_L
F0CE4_L
F0CE5_L
F0CE6_L
F0CE7_L

=PPIO_NAND_H4

R0800 R0801 R0802 R0803
100K 5% 1/32W MF 01005

F0WE_L
F0RE_L
F1WE_L
F1RE_L

F0ALE
F0CLE
F1ALE
F1CLE

R0810 R0811 R0812 R0813
100K 5% 1/32W MF 01005

U0652
H4P-512MB BGA

F0CE0_L	AV20	FMI0_CEN0	GROUP 2	GROUP 2	FMI2_CEN0	AY26	NC_F2CE0_L
F0CE1_L	AW21	FMI0_CEN1			FMI2_CEN1	AU26	NC_F2CE1_L
F0CE2_L	AU19	FMI0_CEN2			FMI2_CEN2	AW26	NC_F2CE2_L
F0CE3_L	AU20	FMI0_CEN3			FMI2_CEN3	AV26	NC_F2CE3_L
F0CE4_L	AV31	FMI0_CEN4	SYM 4 OF 12		FMI2_CEN4	AP34	
F0CE5_L	AT31	FMI0_CEN5	GROUP 3	GROUP 5	FMI2_CEN5	AL32	TP_GPIO_SD_CTRL
F0CE6_L	AV32	FMI0_CEN6	3.3V		FMI2_CEN6	AK31	RST_GRAPE_L (OUT 17)
F0CE7_L	AU30	FMI0_CEN7			FMI2_CEN7	AM32	GRAPE_FW_DNLD_EN_L (OUT 17)
F0AD<0>	AV18	FMI0_IO0			FMI2_IO0	AY29	NC_F2AD<0>
F0AD<1>	AU18	FMI0_IO1			FMI2_IO1	AR30	NC_F2AD<1>
F0AD<2>	AT22	FMI0_IO2			FMI2_IO2	AU29	NC_F2AD<2>
F0AD<3>	AW19	FMI0_IO3			FMI2_IO3	AV28	NC_F2AD<3>
F0AD<4>	AV21	FMI0_IO4			FMI2_IO4	AY28	NC_F2AD<4>
F0AD<5>	AU22	FMI0_IO5			FMI2_IO5	AW30	NC_F2AD<5>
F0AD<6>	AY21	FMI0_IO6	GROUP 2	GROUP 2	FMI2_IO6	AW28	NC_F2AD<6>
F0AD<7>	AR20	FMI0_IO7			FMI2_IO7	AU28	NC_F2AD<7>
F0ALE	AT20	FMI0_ALE			FMI2_ALE	AW27	NC_F2ALE
F0CLE	AU21	FMI0_CLE			FMI2_CLE	AU27	NC_F2CLE
F0WE_L	AT19	FMI0_WEN			FMI2_WEN	AV27	NC_F2WE_L
F0RE_L	AV22	FMI0_REN			FMI2_REN	AY27	NC_F2RE_L
NC_AP_GPIO76	AT21	FMI0_DQS			FMI2_DQS	AV30	NC_AP_GPIO_110
F1CE0_L	AN22	FMI1_CEN0			FMI3_CEN0	AT30	NC_F3CE0_L
F1CE1_L	AY19	FMI1_CEN1	GROUP 2	GROUP 4	FMI3_CEN1	AP31	NC_F3CE1_L
F1CE2_L	AP20	FMI1_CEN2			FMI3_CEN2	AU31	NC_F3CE2_L
F1CE3_L	AT18	FMI1_CEN3			FMI3_CEN3	AU32	NC_F3CE3_L
F1CE4_L	AN30	FMI1_CEN4			FMI3_CEN4	AN34	NC_AP_GPIO_147
F1CE5_L	AU34	FMI1_CEN5	GROUP 3	GROUP 5	FMI3_CEN5	AM33	TP_RST_SD_CTRL_L
F1CE6_L	AU33	FMI1_CEN6	3.3V		FMI3_CEN6	AM34	PM_MLC_PWR_EN (OUT 36)
F1CE7_L	AP30	FMI1_CEN7			FMI3_CEN7	AN33	TP_CD_SD_CTRL_L
F1AD<0>	AV25	FMI1_IO0			FMI3_IO0	AP33	NC_F3AD<0>
F1AD<1>	AU23	FMI1_IO1			FMI3_IO1	AL31	NC_F3AD<1>
F1AD<2>	AW25	FMI1_IO2			FMI3_IO2	AR34	NC_F3AD<2>
F1AD<3>	AU25	FMI1_IO3			FMI3_IO3	AN32	NC_F3AD<3>
F1AD<4>	AU24	FMI1_IO4			FMI3_IO4	AM31	NC_F3AD<4>
F1AD<5>	AV24	FMI1_IO5		GROUP 4	FMI3_IO5	AN31	NC_F3AD<5>
F1AD<6>	AT23	FMI1_IO6	GROUP 2		FMI3_IO6	AR32	NC_F3AD<6>
F1AD<7>	AV23	FMI1_IO7			FMI3_IO7	AP32	NC_F3AD<7>
F1ALE	AP23	FMI1_ALE			FMI3_ALE	AT32	NC_F3ALE
F1CLE	AV19	FMI1_CLE			FMI3_CLE	AT34	NC_F3CLE
F1WE_L	AN23	FMI1_WEN			FMI3_WEN	AT33	NC_F3WE_L
F1RE_L	AN21	FMI1_REN			FMI3_REN	AR31	NC_F3RE_L
NC_AP_GPIO93	AY25	FMI1_DQS			FMI3_DQS	AR33	NC_AP_GPIO_135

VSS

AA11 AA13 AA15 AA17 AA19 AA21 AA23 AA25 AA29 AB1 AB6 AB8

RST_MLC_L (OUT 14)

R0878
100K 5% 1/32W MF 01005

SYNC_MASTER=JAMES	SYNC_DATE=N/A
PAGE TITLE	AP: NAND
Apple Inc.	DRAWING NUMBER 051-8962 / SIZE D
	REVISION A.0.0
	BRANCH
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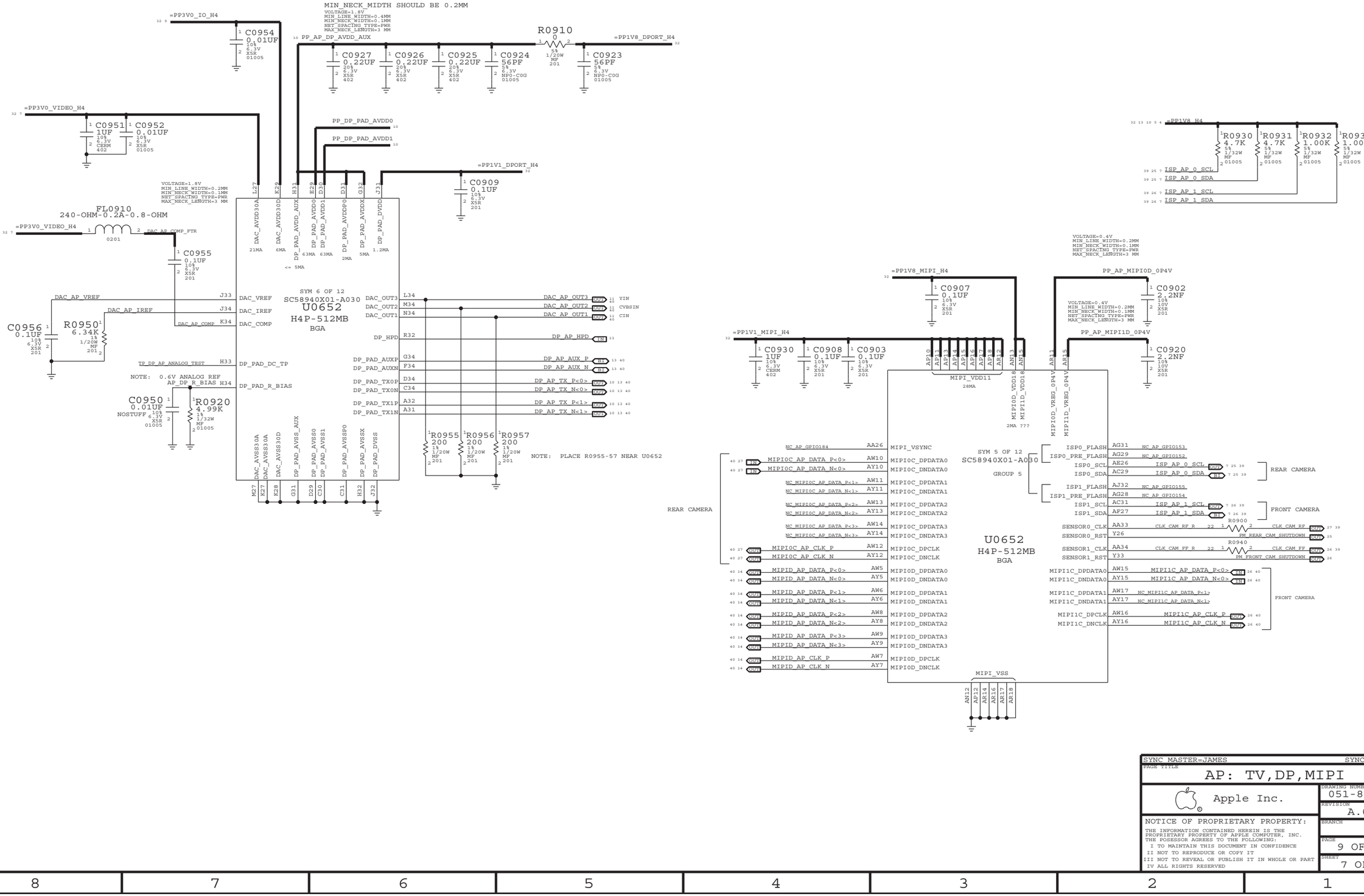

SYNC_MASTER=JAMES	SYNC_DATE=N/A
PAGE TITLE: AP: TV,DP,MIPI	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 9 OF 106
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=PP1V2_S2R_H4
R1005 2.21K 1% 1/32W MF 01005
PPVREF_DDR0_CA
R1006 2.21K 1% 1/32W MF 01005
NOSTUFF C1002 0.01UF 10% 6.3V X5R 01005 VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.1MM NET_SPACING_TYPE=VREF MAX_NECK_LENGTH=3 MM

=PP1V2_S2R_H4
R1051 2.21K 1% 1/32W MF 01005
PPVREF_DDR1_CA
R1052 2.21K 1% 1/32W MF 01005
NOSTUFF C1052 0.01UF 10% 6.3V X5R 01005 VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.1MM NET_SPACING_TYPE=VREF MAX_NECK_LENGTH=3 MM

=PP1V2_VDDQ_H4
R1053 1.00K 1% 1/32W MF 01005
PPVREF_DDR0_DQ
R1054 1.00K 1% 1/32W MF 01005
NOSTUFF C1054 0.01UF 10% 6.3V X5R 01005 VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.1MM NET_SPACING_TYPE=VREF MAX_NECK_LENGTH=3 MM

=PP1V2_VDDQ_H4
R1055 1.00K 1% 1/32W MF 01005
PPVREF_DDR1_DQ
R1056 1.00K 1% 1/32W MF 01005
NOSTUFF C1056 0.01UF 10% 6.3V X5R 01005 VOLTAGE=0.6V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.1MM NET_SPACING_TYPE=VREF MAX_NECK_LENGTH=3 MM

=PP1V2_S2R_H4
C1000 0.22UF 20% 6.3V X5R 0201
C1001 0.22UF 20% 6.3V X5R 0201

U0652
BGA
H4P-512MB
SYM 7 OF 12
SC58940X01-A030

R1001 240 1% 1/20W MF 201
(DDR IMPEDANCE CONTROL)
240 R1000

H11	DDR0_VDDQ_CKE <1MA	VSS_32	AB10
R8	DDR1_VDDQ_CKE <1MA	VSS_33	AB12
AY23	DDR0_VREF_CA	VSS_34	AB14
AE34	DDR1_VREF_CA	VSS_35	AB16
AA1	DDR1_VREF_DQ	VSS_36	AB18
A25	DDR0_VREF_DQ	VSS_37	AB20
AY18	DDR0_ZQ	VSS_38	AB22
AK34	DDR1_ZQ	VSS_39	AB24
AD33			AB29
AH33	VDDCA 80MA	VSS	AC1
AW20			AC5
AW24			AC9
AW29			AC11
W33			AC13
A24			AC15
AA2	VDD2 320MA	VSS	AC17
AF33			AC19
AK33			AC21
AL1			AC23
AW22			AC25
AW31			AC27
B4			AD2
B5			AD8
B25			AD10
F33			AD12
T34			AD14
Y1			AD16
A4			AD18
A5	VDD1 40MA	VSS	AD20
AB2			AD22
AL2			AD24
AL33			AD27
AW18			AD34
AW32			AE5
B26			AE9
E33			AE11
U33			AE13
AC2			AE15
AG2	VDDQ 500MA (VDDQ - VDDIOD; DON'T DOUBLE COUNT)	VSS	AE17
AK2			AE19
AN2			AE21
AT2			AE23
AW3			AE25
B3			AE33
B6			AF1
B8			AF5
B11			AF8
B14			AF10
B16			AF12
B19			AF14
B21			AF16
B24			AF18
B27			AF20
B31			AF22
D2			AF24
D33			AF26
G2			AF32
G33			AG9
K2			AG11
K33			AG13
M2			AG15
N33			AG17
R2			AG19
R33			AG21
U2			AG23
Y2			AG25

=PP1V2_S2R_H4
C1004 0.22UF 20% 6.3V X5R 0201
C1005 0.22UF 20% 6.3V X5R 0201
C1006 0.22UF 20% 6.3V X5R 0201
C1007 0.22UF 20% 6.3V X5R 0201
C1008 10UF 20% 6.3V X5R 603
C1009 4.3UF 20% 4V X5R-CERM 0610
C1010 1UF 10% 6.3V CERM 402
C1011 1UF 10% 6.3V CERM 402
C1012 0.01UF 10% 10V X5R 201
C1013 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF

=PP1V8_S2R_H4
C1014 10UF 20% 6.3V X5R 603
C1015 1UF 10% 6.3V CERM 402
C1016 1UF 10% 6.3V CERM 402
C1017 0.01UF 10% 6.3V X5R 01005
C1018 0.01UF 10% 6.3V X5R 01005
C1019 0.22UF 20% 6.3V X5R 0201
C1020 0.22UF 20% 6.3V X5R 0201
C1021 0.22UF 20% 6.3V X5R 0201
C1022 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF

=PP1V2_VDDQ_H4
C1023 10UF 20% 6.3V X5R 603
C1024 4.3UF 20% 4V X5R-CERM 0610
C1026 0.01UF 10% 6.3V X5R 01005
C1027 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF
C1029 0.22UF 20% 6.3V X5R 0201
C1030 0.22UF 20% 6.3V X5R 0201
C1031 0.22UF 20% 6.3V X5R 0201

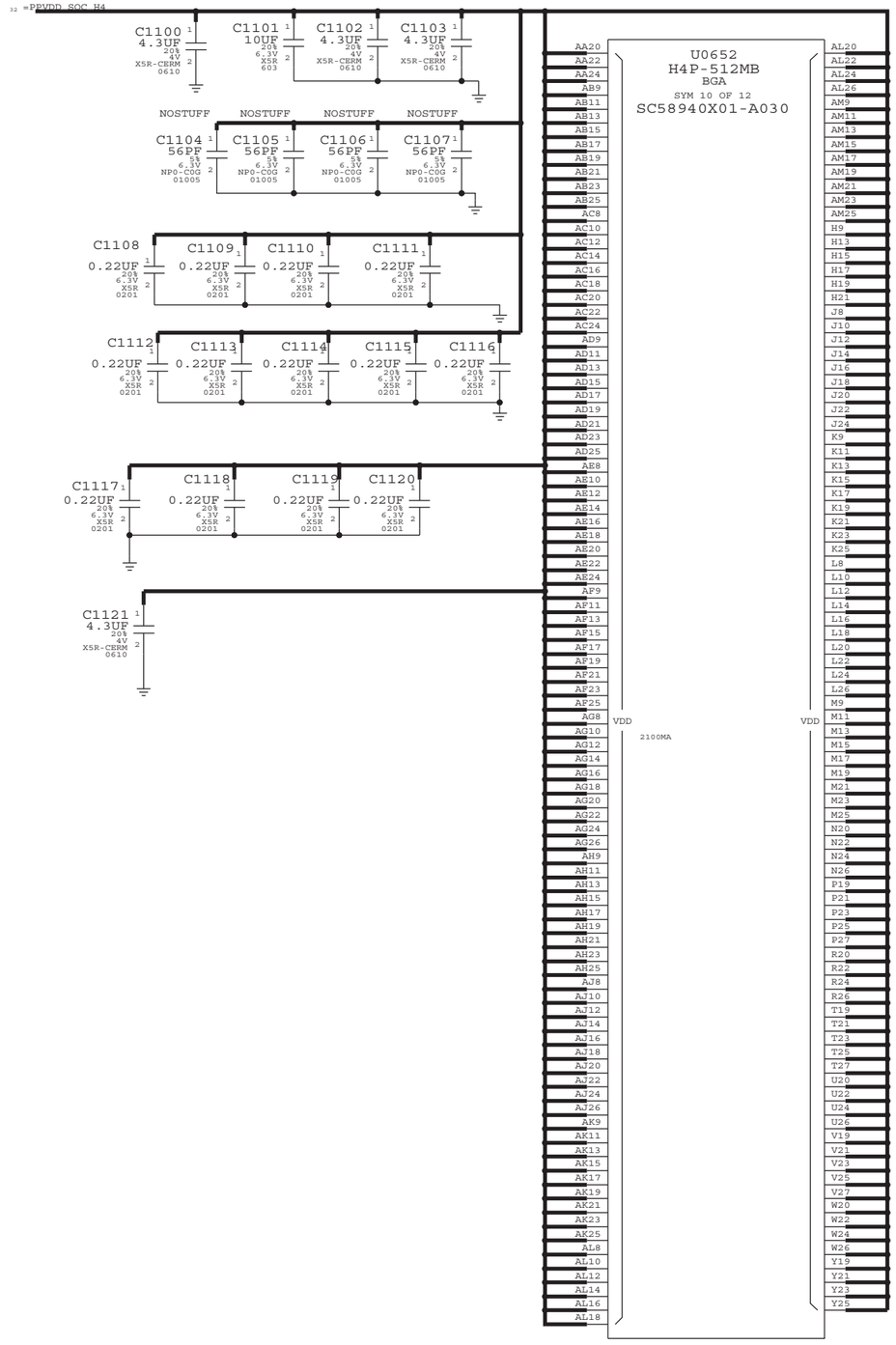
=PP1V2_VDDIOD_H4
C1032 10UF 20% 6.3V X5R 603
C1034 4.3UF 20% 4V X5R-CERM 0610
C1035 0.22UF 20% 6.3V X5R 0201
C1036 0.22UF 20% 6.3V X5R 0201
C1037 0.22UF 20% 6.3V X5R 0201
C1038 0.22UF 20% 6.3V X5R 0201
C1039 0.22UF 20% 6.3V X5R 0201
C1040 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF

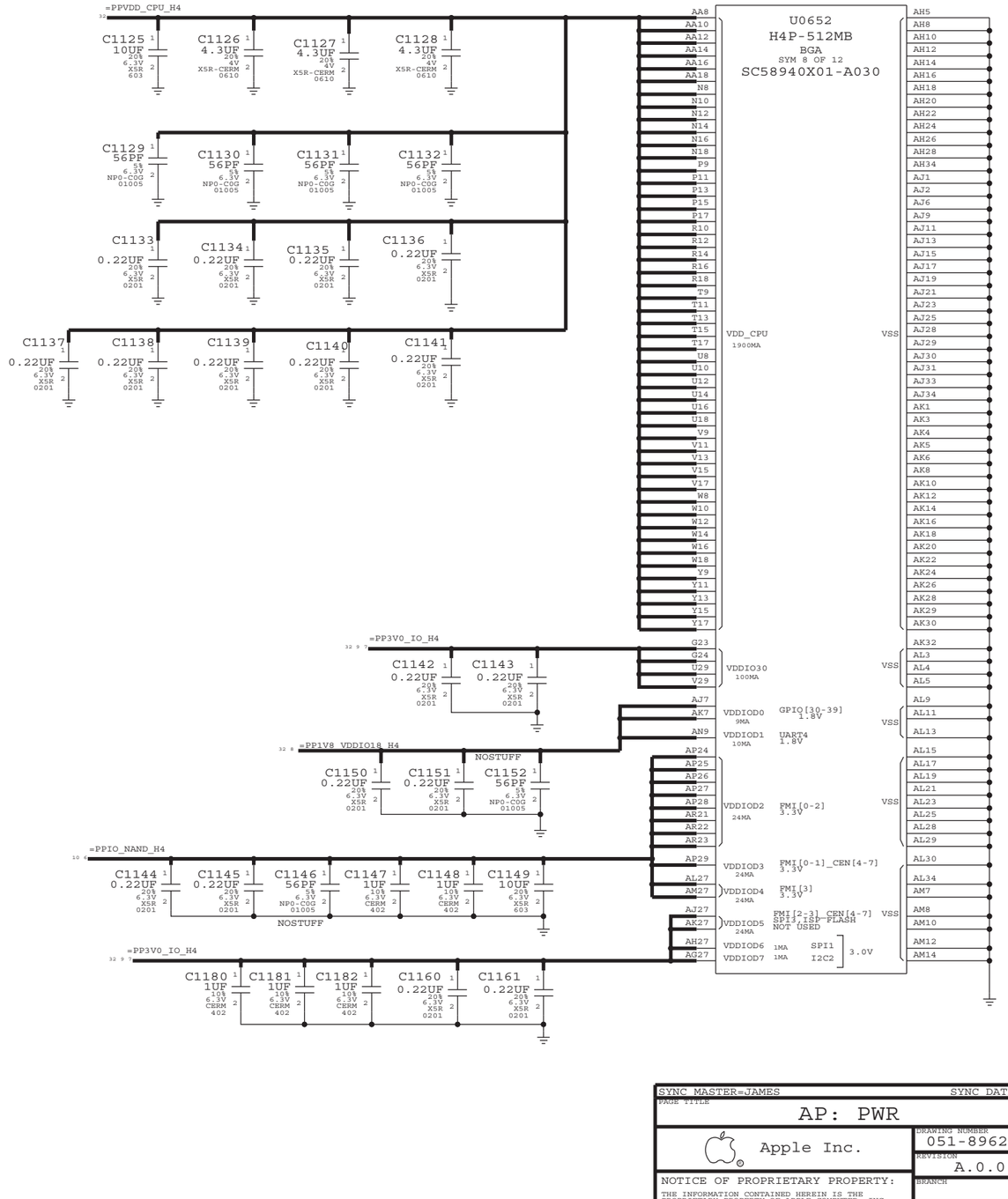
U0652
H4P-512MB
BGA
SYM 9 OF 12
SC58940X01-A030

D4	VDDIOD 500MA (VDDQ + VDDIOD; DON'T DOUBLE COUNT)	VSS	AM16
D6			AM18
D8			AM20
D10			AM22
D12			AM24
D14			AM26
E5			AM28
E7			AM29
E9			AM30
E11			AN1
E13			AN14
E15			AN16
F4			AN17
F6			AN18
F7			AN19
F8			AN20
F9			AN24
F10			AN25
F11			AN26
F12			AN27
F13			AN28
F14			AN29
F15			AP5
F16			AP6
F17			AP7
F18			AP8
G5			AP9
G6			AP19
H4			AP21
H6			AP22
J5			AR1
J6			AR5
K4			AR6
K6			AR7
L5			AR8
L6			AR9
M4			AR13
M6			AR19
N5			AR24
N6			AR25
P4			AR26
P6			AR27
R5			AR28
R6			AR29
T4			AT5
T6			AT6
U5			AT7
U6			AT8
V4			AT9
V6			AT10
W5			AT11
W6			AT12
Y4			AT13
Y6			AT15
AA28	VDDIO18 44MA	VSS	AT16
AB7			AT17
AB28			AT24
AC6			AT25
AC28			AT26
AD28			AT27
AE6			AT28
AF6			AT29
AH6			AU4
AN6			AU5
AN7			AU6
AN8			AU7
H23			AU8
P28			AU9
R28			AU10
T28			AU11
W28			AU12
Y28			AU13

=PP1V8_VDDIO18_H4
C1041 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF
C1042 0.22UF 20% 6.3V X5R 0201
C1043 1UF 10% 6.3V CERM 402
C1044 0.22UF 20% 6.3V X5R 0201
C1045 0.22UF 20% 6.3V X5R 0201
C1046 1UF 10% 6.3V CERM 402

SYNC_MASTER=JAMES SYNC_DATE=N/A
PAGE TITLE: AP: PWR
Apple Inc.
DRAWING NUMBER: 051-8962 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 10 OF 106
SHEET: 8 OF 42





SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE

AP: PWR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

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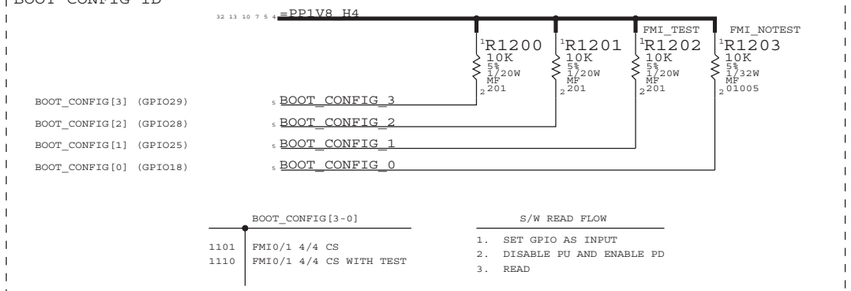
BOOT CONFIG ID

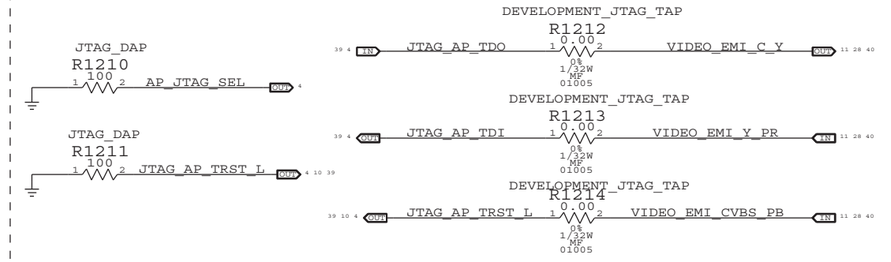


BOOT_CONFIG[3-0]	
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

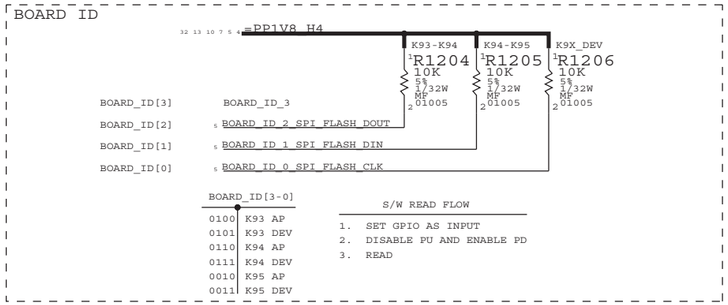
1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

JTAG



2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG JTAG_DAP	DEVELOPMENT_JTAG DEVELOPMENT_JTAG_TAP	JTAG_DAP

BOARD ID

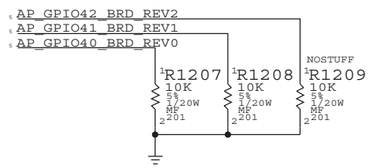


BOARD_ID[3-0]	
0100	K93 AP
0101	K93 DEV
0110	K94 AP
0111	K94 DEV
0010	K95 AP
0011	K95 DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



BRD_REV[2-0]	
000	PROTO 1
001	PROTO 2
010	EVT
011	EVT2
100	DVT

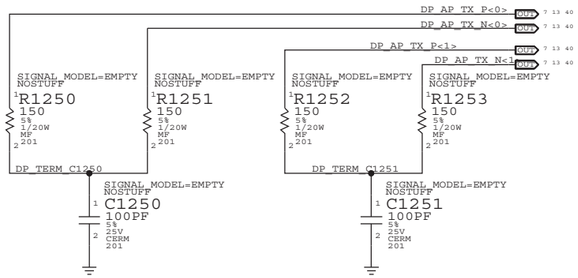
S/W READ FLOW

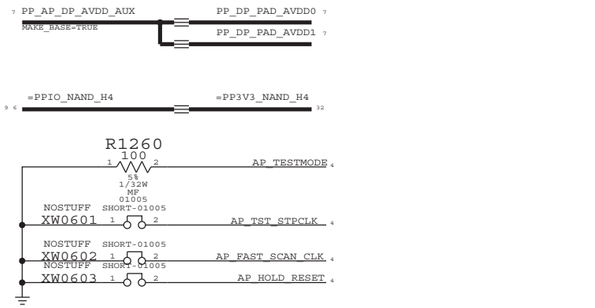
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

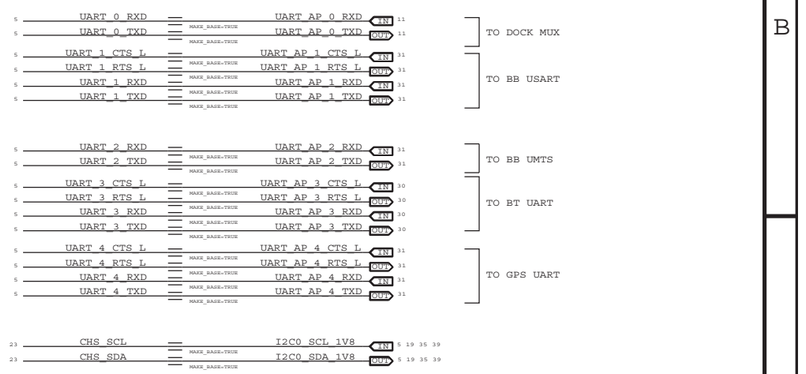
FOR REFERENCE

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1011	RESERVED
1100	FMI0/1 2/2 CS
CURRENT SETTING -> 1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

PLACEMENT NOTE: NEAR U0652







SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

AP: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

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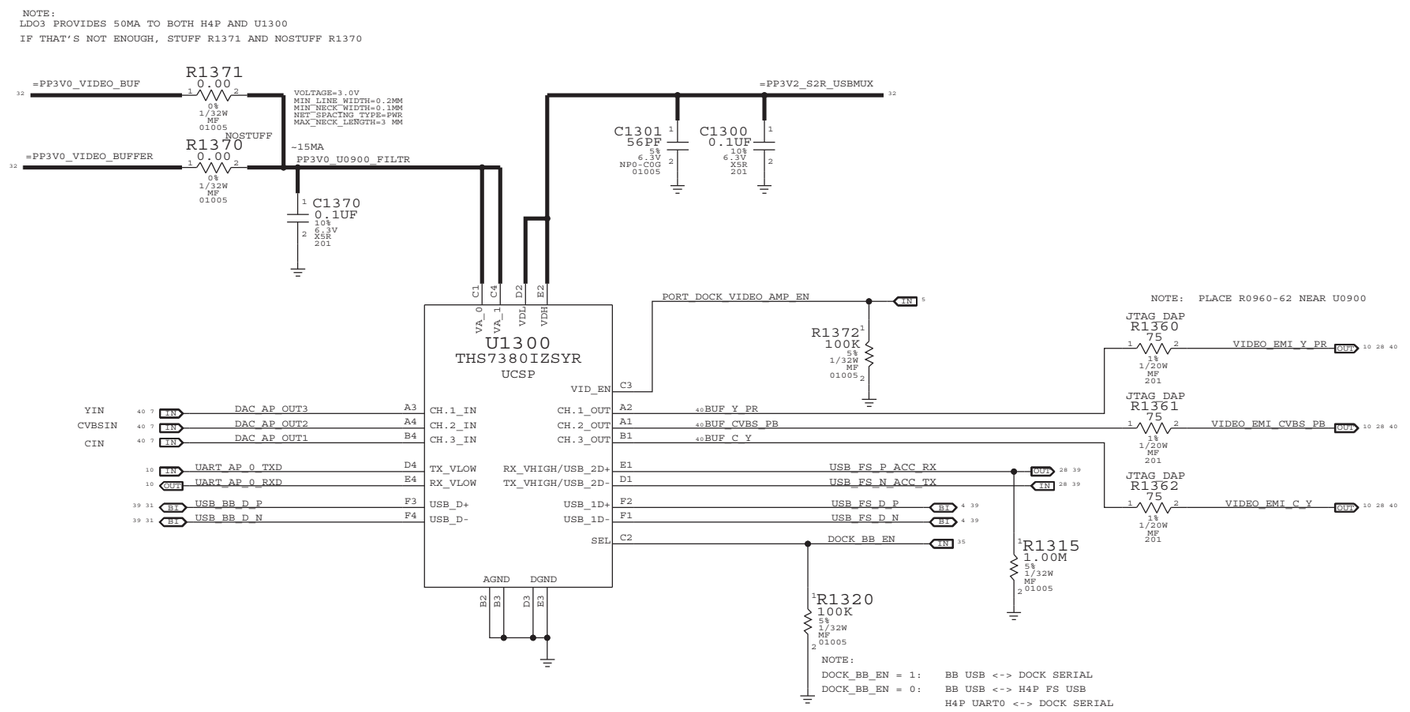

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

AP: VIDEO BUFFER,BB USB MUXES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

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16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

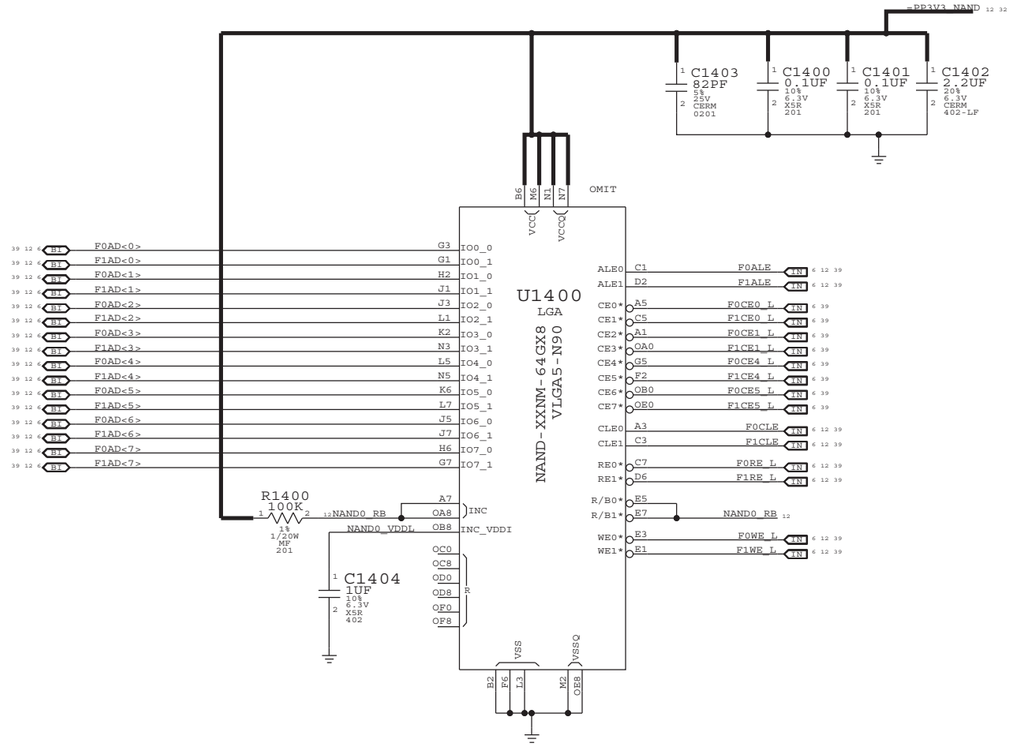
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

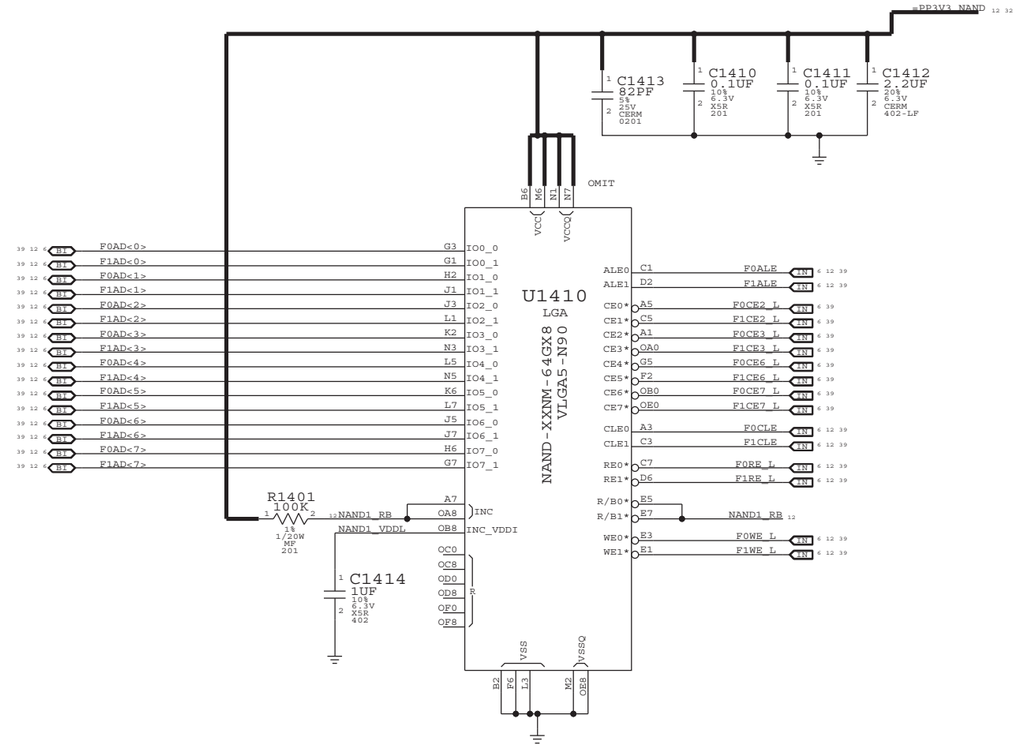
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN





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PAGE TITLE: NAND	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 14 OF 106
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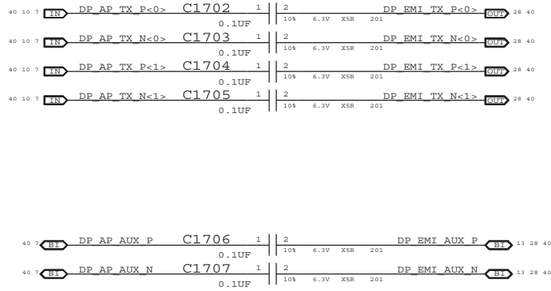
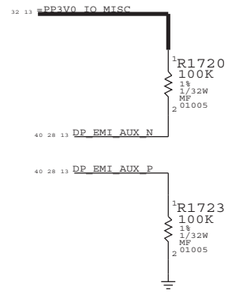
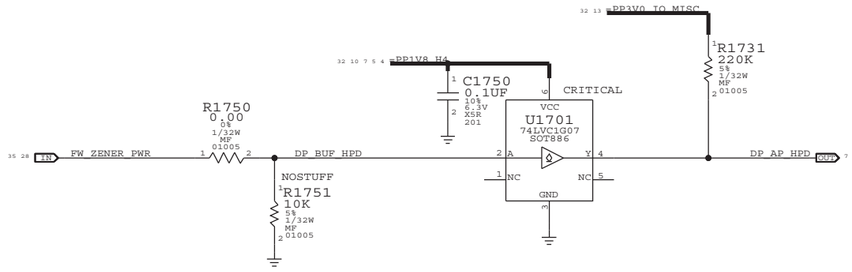
DISPLAYPORT AC COUPLING





DISPLAYPORT HOT PLUG DETECT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
VIDEO: DISPLAY PORT

Apple Inc.

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MLC EEPROM:RAW APN 335S0661

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0618			RADAR:8377307

WHEN WC_L IS LOW, CAN WRITE TO EEPROM
WHEN WC_L IS HIGH, CANNOT WRITE TO EEPROM

U2001 M24C64 EEPROM MLP
U2000 FBGA1 S6T2MLC

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: VIDEO: MLC

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 20 OF 106
SHEET: 14 OF 42

14 MLC_SDA_3V3 ⟷ MLC_MUX_SDA_3V3 14

14 MLC_SCL_3V3 ⟷ MLC_MUX_SCL_3V3 14

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

VIDEO: MLC ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

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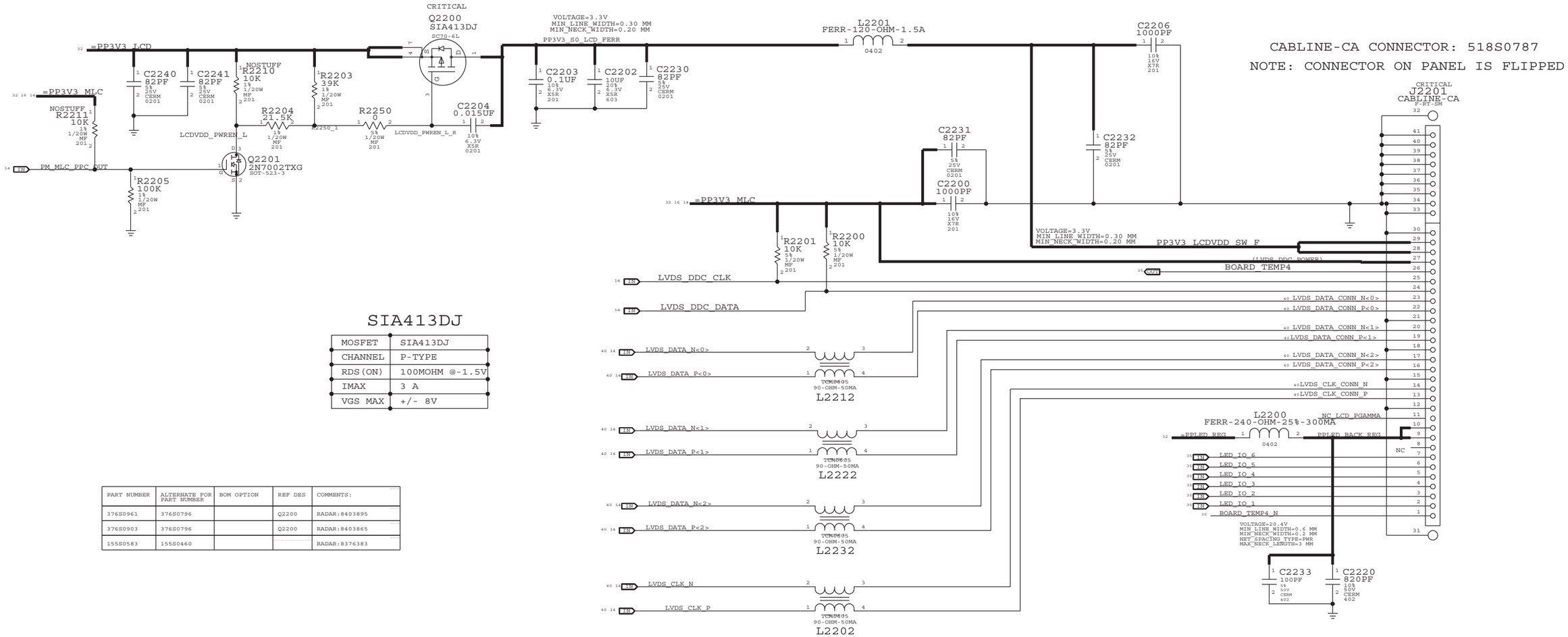
LVDS CONNECTOR



SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO
INVESTIGATE POSSIBILITY OF REMOVING
THE CHOKE

SYNC MASTER=ALEX SYNC DATE=N/A

PAGE TITLE

VIDEO: LVDS CONNECTOR

Apple Inc.

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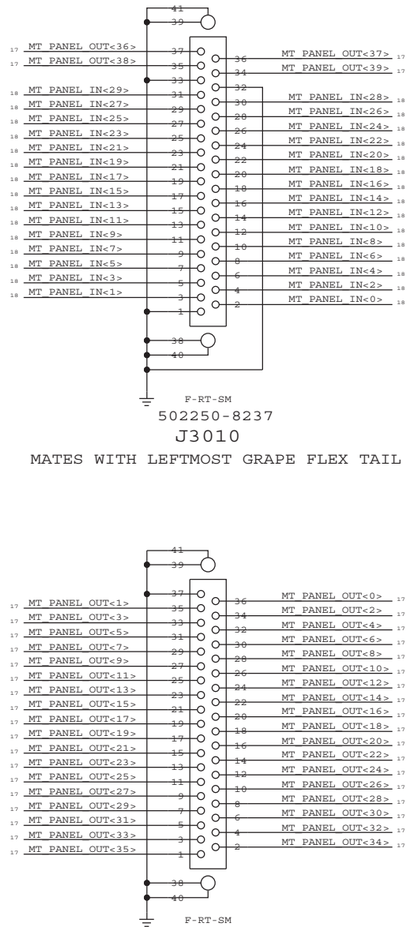
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

CONNECTORS TO GRAPE FLEX

P/N 518S0817



502250-8237

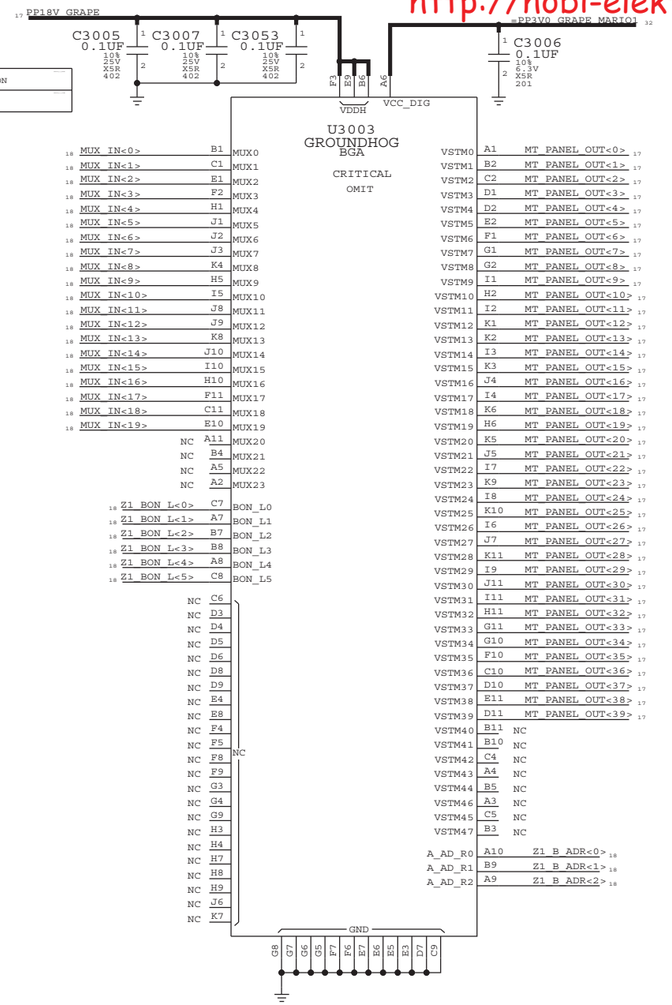
J3010

MATES WITH LEFTMOST GRAPE FLEX TAIL

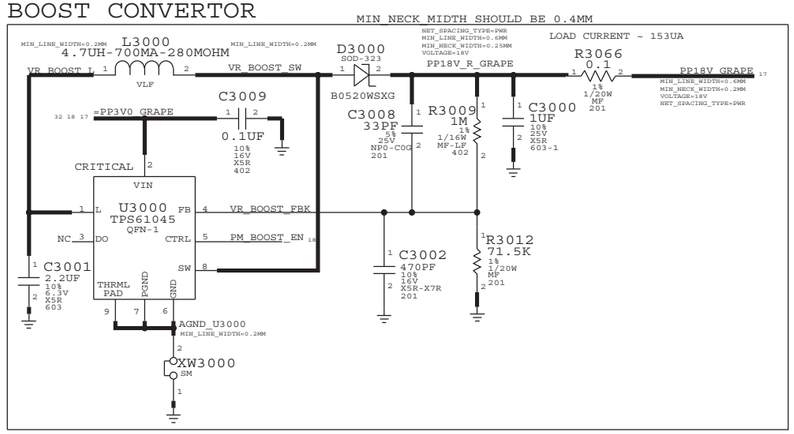
502250-8237

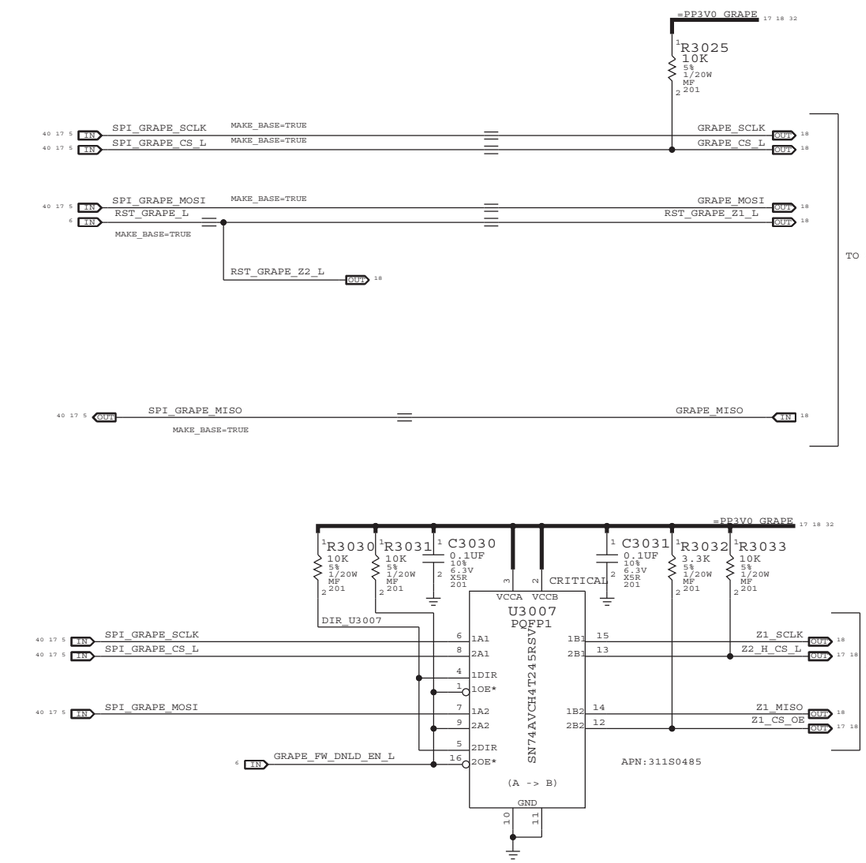
J3011

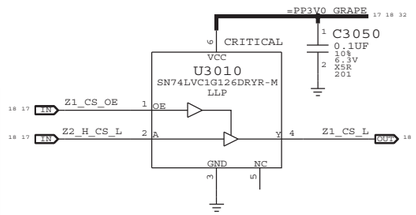
MATES WITH RIGHTMOST GRAPE FLEX TAIL

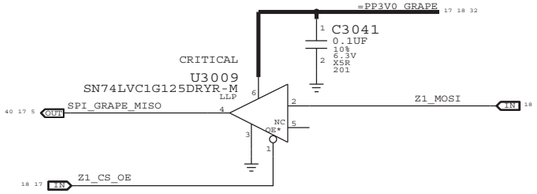


BOOST CONVERTOR









PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=RAMSIN SYNC_DATE=N/A

PAGE TITLE

GRAPE: GROUNDHOG,CONN,BOOST

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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ARM9 MCU (Z2 BASED)

Z2_VDDCORE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
C3111 10UF 20% 6.3V X5R 603
C3109 0.1UF 10% 6.3V X5R 201

VDDANA AND VDDCORE ARE EACH GENERATED WITHIN Z2 AND BYPASSED OUTSIDE

Z2_VDDANA
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
C3112 2.2UF 20% 4V X5R 402
C3110 0.1UF 10% 6.3V X5R 201

=PP3V0_GRAPE_Z2
C3105 0.1UF 10% 6.3V X5R 201
C3107 4.7UF 20% 6.3V X5R 402

VOLTAGE=1.8V
NET_SPACING_TYPE=PWR
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
C3108 0.1UF 10% 6.3V X5R 201
C3106 0.1UF 10% 6.3V X5R 201
C3191 22UF 20% 6.3V X5R-CERM 603

Z2_3V3_1V8_IN
R3190 1.00 1% 1/20W MF 201
Z1_1V8_OUT
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.8V
NET_SPACING_TYPE=PWR
MIN_NECK_MIDTH SHOULD BE 0.4MM

VDDANA VDDCORE VDDIO VDDLDO

CRITICAL
U3101
BCM5974CKFBGH
FBGA

NC	A9	IN0_0	
NC	B9	IN0_1	
NC	A7	IN1_0	
NC	A8	IN1_1	
NC	B8	IN2_0	
NC	C8	IN2_1	
NC	B7	IN3_0	
NC	C7	IN3_1	
NC	A6	IN4_0	
NC	B6	IN4_1	
NC	C6	IN5_0	
NC	C5	IN5_1	
NC	B5	IN6_0	
NC	A5	IN6_1	
NC	A4	IN7_0	
NC	B4	IN7_1	
NC	A3	IN8_0	
NC	B3	IN8_1	
NC	C2	IN9_0	
NC	A2	IN9_1	
NC	B2	IN10_0	
NC	C1	IN10_1	
NC	B1	IN11_0	
NC	A1	IN11_1	
NC	E6	ARMTAPMD*	
BOOT_CFG0_R	F6	BOOT_CFG0	
BOOT_CFG1_R	D3	BOOT_CFG1	
NC	G5	FLOO	
NC	F5	LFOO	
NC	G7	EXTFLLIN	

B_ADR0	F9	B_ADR0	
B_ADR1	F8	B_ADR1	
B_ADR2	G9	B_ADR2	
BON_L0	J8	BON_L0	Z1_CS_OE_R
BON_L1	H9	BON_L1	NC_BON_L1
BON_L2	J9	BON_L2	NC_BON_L2
BON_L3	H7	BON_L3	NC_BON_L3
BON_L4	J7	BON_L4	NC_BON_L4
BON_L5	H5	BON_L5	Z2_BON_L4
GPIO0	J2		IRQ_GRAPE_HOST_INT_L (OUT)
GPIO1	J3		PM_BOOST_EN (OUT)
GPIO2	H4		Z1_GO
GPIO3	J6		Z1_DONE
GPIO4	G3		GRAPE_CS_L (IN)
GPIO5	F3		GRAPE_MOSI (IN)
GPIO6	F4		GRAPE_MISO (OUT)
GPIO7	H6		GRAPE_SCLK (IN)
JTAG_TCK	G6		TP_U3101_TCK
JTAG_TDI	E8		TP_U3101_TDI
JTAG_TDO	E9		TP_U3101_TDO
JTAG_TMS	F7		TP_U3101_TMS
H_CS*	H1		Z2_H_CS_L (IN)
H_SCLK	J1		Z1_SCLK (IN)
H_SDI	H3		Z1_MISO (IN)
H_SDO	J4		Z1_MOSI (OUT)
A_CS*	F1		Z2_A_CS_L
A_SCLK	G1		TP_Z2_A_SCLK
A_SDI	F2		TP_Z2_A_SDI
A_SDO	G4		TP_Z2_A_SDO
TM0	E7		TP_U3101_TM0
TM1	D4		U3101_TM1
CLKIN	E5		HOST_REFCLK — CLK_32K_PMU (IN) MAKE_BASE=TRUE
CLKOUT	E4		NC
INTERNAL PU RESET*	D5		RST_GRAPE_Z2_L (IN)

R3120 0 5% 1/20W MF 201 — Z1_CS_OE (IN)
=PP3V0_GRAPE_Z2 NOSTUFF
R3161 100K 5% 1/20W MF 201

NOTE: PLATEFORM DETECTION PIN "H5"
PULL DOWN = K48
FLOATING = K93/K94
PULL UP = RESERVED FOR FUTURE

R3160 100K 5% 1/20W MF 201
=PP3V0_GRAPE
R3107 100K 5% 1/20W MF 201
R3180 100 5% 1/32W MF 01005

CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

R3173 0 5% 1/20W MF 201 — =PP3V0_GRAPE
R3171 0
GND
C3 C4 D6 D7 D8 C9 D9 G2 D1 H8

ZEPHYR 1+ ASIC

=PP3V0_GRAPE_Z1
R3101 4.7 5% 1/20W MF 201
MT_3V3_INT
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
C3102 0.1UF 10% 6.3V X5R 201
C3104 2.2UF 20% 4V X5R 402
C3103 0.1UF 10% 6.3V X5R 201

Z1_1V8_OUT
C3101 2.2UF 20% 4V X5R 402

=PP3V0_GRAPE
R3155 100K 5% 1/20W MF 201

CRITICAL
U3100
BGA-HF
BCM5973

VDDANA VDDDIG VDDIO V18

MT_PANEL_IN<0>	D1	IN0	
MT_PANEL_IN<1>	D2	IN1	
MT_PANEL_IN<2>	D3	IN2	
MT_PANEL_IN<3>	D4	IN3	
MT_PANEL_IN<4>	E1	IN4	
MT_PANEL_IN<5>	E2	IN5	
MT_PANEL_IN<6>	E3	IN6	
MT_PANEL_IN<7>	E4	IN7	
MT_PANEL_IN<8>	F1	IN8	
MT_PANEL_IN<9>	F2	IN9	
MT_PANEL_IN<10>	F3	IN10	
MT_PANEL_IN<11>	F4	IN11	
MT_PANEL_IN<12>	G1	IN12	
MT_PANEL_IN<13>	G2	IN13	
MT_PANEL_IN<14>	G3	IN14	
MT_PANEL_IN<15>	G4	IN15	
MT_PANEL_IN<16>	G5	IN16	
MT_PANEL_IN<17>	H1	IN17	
MT_PANEL_IN<18>	H2	IN18	
MT_PANEL_IN<19>	H3	IN19	
MT_PANEL_IN<20>	H4	IN20	
MT_PANEL_IN<21>	H5	IN21	
MT_PANEL_IN<22>	J1	IN22	
MT_PANEL_IN<23>	K1	IN23	
MT_PANEL_IN<24>	J2	IN24	
MT_PANEL_IN<25>	K2	IN25	
MT_PANEL_IN<26>	J3	IN26	
MT_PANEL_IN<27>	K3	IN27	
MT_PANEL_IN<28>	J4	IN28	
MT_PANEL_IN<29>	K4	IN29	
MUX_IN<0>	J5	IN30	
MUX_IN<1>	K5	IN31	
MUX_IN<2>	K6	IN32	
MUX_IN<3>	J6	IN33	
MUX_IN<4>	J7	IN34	
MUX_IN<5>	K7	IN35	
MUX_IN<6>	J8	IN36	
MUX_IN<7>	K8	IN37	
MUX_IN<8>	J9	IN38	
MUX_IN<9>	K9	IN39	
MUX_IN<10>	J10	IN40	
MUX_IN<11>	K10	IN41	
MUX_IN<12>	H6	IN42	
MUX_IN<13>	H7	IN43	
MUX_IN<14>	H8	IN44	
MUX_IN<15>	H9	IN45	
MUX_IN<16>	H10	IN46	
MUX_IN<17>	G6	IN47	
MUX_IN<18>	G7	IN48	
MUX_IN<19>	G8	IN49	
NC	G9	IN50	
NC	G10	IN51	
NC	F7	IN52	
NC	F8	IN53	
NC	F9	IN54	
NC	F10	IN55	
NC	E7	IN56	
NC	E8	IN57	
NC	E9	IN58	
NC	E10	IN59	
NC	D7	IN60	
NC	D8	IN61	
NC	D9	IN62	
NC	D10	IN63	

SCLK	A9		Z1_SCLK (IN)
CS*	A8		Z1_CS_L (IN)
MISO	A7		Z1_MISO (IN)
MOST	A6		Z1_MOSI (OUT)
GO	B5		Z1_GO
DONE	B6		Z1_DONE
PCLK	A10		Z1_PCLK
STMOUT	B9		
STMIN	B10		Z1_STMIN
B_ADR0	B2		Z1_B_ADR<0>
B_ADR1	B3		Z1_B_ADR<1>
B_ADR2	B4		Z1_B_ADR<2>
BON_L0	A1		Z1_BON_L<0>
BON_L1	A2		Z1_BON_L<1>
BON_L2	A3		Z1_BON_L<2>
BON_L3	A4		Z1_BON_L<3>
BON_L4	A5		Z1_BON_L<4>
BON_L5	B1		Z1_BON_L<5>
TM	B8		U3100_TM
INTERNAL PU RESET*	C5		RST_GRAPE_Z1_L

R3181 100 5% 1/32W MF 01005

GNDANA GNDDIG GNDIO
C2 C3 D6 E6 F6 B7 C8 C9

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR:8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

SYNC MASTER=RAMSIN SYNC DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

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L63 AUDIO CODEC

APN:338S0940

=PPVCC_MAIN_AUDIO
=PP1V8_AUDIO
=PP1V7_VA_VCP

C3600 1000PF 10% 6.3V X5R 01005
C3601 0.1UF 20% 4V X5R 01005
C3602 0.1UF 20% 4V X5R 01005
C3603 10UF 20% 6.3V X5R 603
C3604 0.1UF 10% 6.3V X5R 201
C3605 27PF 5% 16V NPO-COG 01005
C3606 10UF 20% 4V X5R 402
C3607 0.1UF 20% 4V X5R 01005
C3608 4.7UF 20% 4V TANT 402-3

XW3600 SM
XW3601 SM
XW3602 SM
GND_AUDIO_CODEC

MIN_LINE_WIDTH=1.0MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_HP_AMP

U3600
CS42L63B
WLCSP

I2C ADDRESS: 1001010X??

VD B11, VL C11, VP F5, VA G2, VCP D11

I2C0_SCL_1V8 → SCL C6
I2C0_SDA_1V8 → SDA C7
IRQ_CODEC_L ← INT* E4
RST_L63_L → RESET* E5
AUD_MIK_HS1_INT_L ← WAKE* E3
I2S_AP_0_MCK_R → MCLK B9
I2S_AP_0_LRCK → ASP_LRCLK C8
I2S_AP_0_BCLK → ASP_SCLK B7
I2S_AP_0_DOUT → ASP_SDIN B8
I2S_AP_0_DIN ← ASP_SDOUT A9
R3601 22 5% 1/32W MF 01005 — L63_ASP_SDOUT

I2S_AP_2_LRCK → VSP_LRCLK C9
I2S_AP_2_BCLK → VSP_SLCLK C10
I2S_AP_2_DOUT → VSP_SDIN A11
I2S_AP_2_DIN ← VSP_SDOUT A10
R3602 22 5% 1/32W MF 01005 — L63_VSP_SDOUT

I2S_AP_3_LRCK → XSP_LRCLK B6
I2S_AP_3_BCLK → XSP_SCLK A6
I2S_AP_3_DOUT → XSP_SDIN/DAC2B_MUTE A8
I2S_AP_3_DIN ← XSP_SDOUT A7
R3603 22 5% 1/32W MF 01005 — L63_XSP_SDOUT

NOSTUFF R3608 22 5% 1/32W MF 01005 — DMIC_SCLK_SENSOR → DMIC_SCLK_CODEC B5
R3620 22 5% 1/32W MF 01005 — DMIC_SCLK_CANADA → DMIC_SD_CODEC A5
NOSTUFF R3621 22 5% 1/32W MF 01005 — DMIC_SD_SENSOR
R3622 22 5% 1/32W MF 01005 — DMIC_SD_CANADA

NC_LINE_IN1_CODEC → LINEINA C5
NC_LINE_IN1_REF_CODEC → LINEINA_REF C4
NC_LINE_IN2_CODEC → LINEINB D6
NC_LINE_IN2_REF_CODEC → LINEINB_REF D5
NC_MIC1_BIAS_CODEC → MIC1_BIAS D4
NC_MIC1P_CODEC → MIC1 A3
NC_MIC1N_CODEC → MIC1_REF B3
NC_MIC1_FILT_CODEC → MIC1_BIAS_FILT E2

EXT_MIC_BIAS → MIC2_BIAS C2
HSMIC_C_P → MIC2_DETECT D3
R3604 1.00K 1% 1/32W MF 01005 — MIC2_DET
EXT_MIC_P → MIC2 B1
EXT_MIC_REF → MIC2_REF B2
HSMIC_C_N → MIC2_DETECT_REF C3
R3605 1.00K 1% 1/32W MF 01005 — MIC2_DET_REF
MIC2_BIAS_FILT C1 → MIC2_BIAS_FILT C1

MIC3A_BIAS D2
MIC3A A1
MIC3A_REF A2
MIC3A_BIAS_FILT D1
MIC3B_BIAS F1
MIC3B A4
MIC3B_REF B4
MIC3B_BIAS_FILT E1

GNDD B10, GNDA F2, GNDCP E10, GNDP G5, GND D8, D9

C3609 4.7UF 20% 6.3V X5R-CERM 402
C3611 4.7UF 20% 6.3V X5R-CERM 402

HP_DETECT E9 → HP_DET
HPOUTB G9 → HP_R
HPOUTA G10 → HP_L
HPOUT_REF F9 → HP_REF
LINEOUT1B G8 → CODEC_LINE_OUT_R
LINEOUT1A F8 → CODEC_LINE_OUT_L
LINEOUT1_REF E8 → CODEC_LINE_OUT_REF
LINEOUT2A D7 → LEFT_CH_OUT_P
LINEOUT2A_REF E7 → LEFT_CH_OUT_REF
LINEOUT2B F7 → RIGHT_CH_OUT_P
LINEOUT2B_REF G7 → RIGHT_CH_OUT_REF

EAROUT+ G3 — NC_EAROUT_AP
EAROUT- F3 — NC_EAROUT_AN
SPEAKEROUTA+ F6 — NC_SPEAKEROUT_AP
SPEAKEROUTA- G6 — NC_SPEAKEROUT_AN
SPEAKEROUTB+ F4 — NC_SPEAKEROUT_BP
SPEAKEROUTB- G4 — NC_SPEAKEROUT_BN

FLYP E11 VHP_FLYP — C3617 2.2UF 20% 10V X5R-CERM 402
FLYC F11 VHP_FLYC — C3618 2.2UF 20% 10V X5R-CERM 402
FLYN G11 VHP_FLYN
SPEAKER_VQ E6 SPKR_VQ — NOT USING SPEAKER AMPLIFIER, THIS CAN BE A NO STUFF
FILT+ G1 FILT_P

+VCP_FILT D10 VHPPFILT
-VCP_FILT F10 VHPNFILT

C3613 10UF 20% 6.3V X5R 603
C3614 10UF 20% 6.3V X5R 603
CRITICAL C3615 1UF 10% 6.3V TANT 402-1
2.2UF RECOMMENDED CRITICAL C3616 4.7UF 20% 6.3V X5R-CERM 402

GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=75 MM

SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE: AUDIO: L63 CODEC

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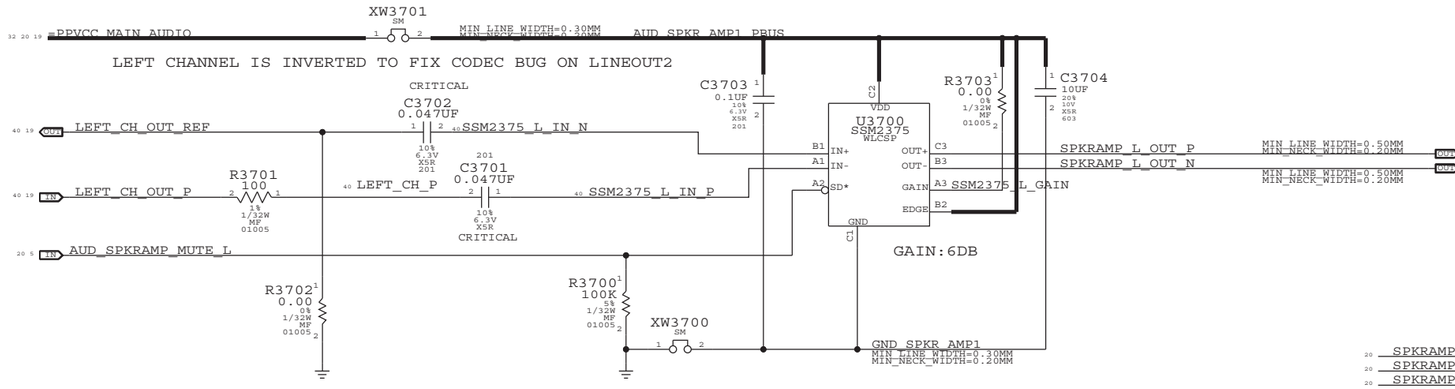
GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT

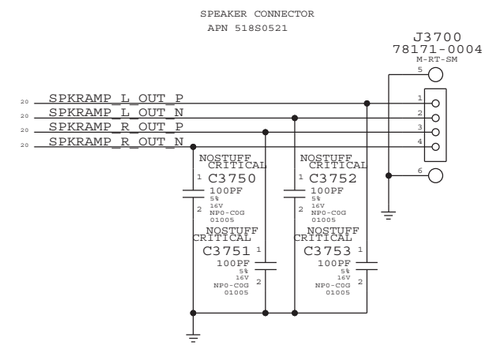
SPEAKER AMPLIFIER

APN:353S2958

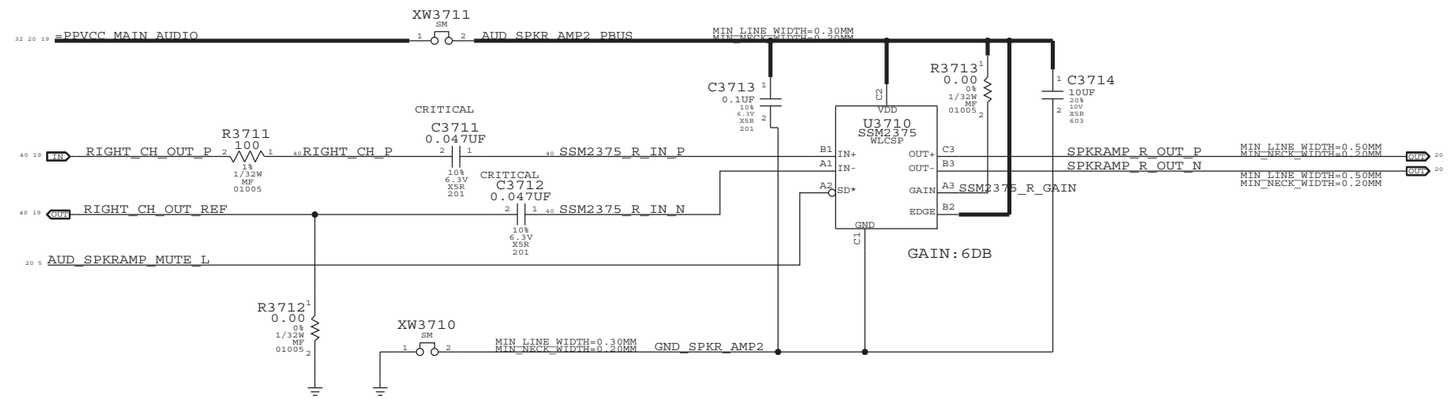
TURN ON TIME: 7.5MS

80HZ +/- XXX% TURN ON DELAY: 20MS





L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710



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PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH:
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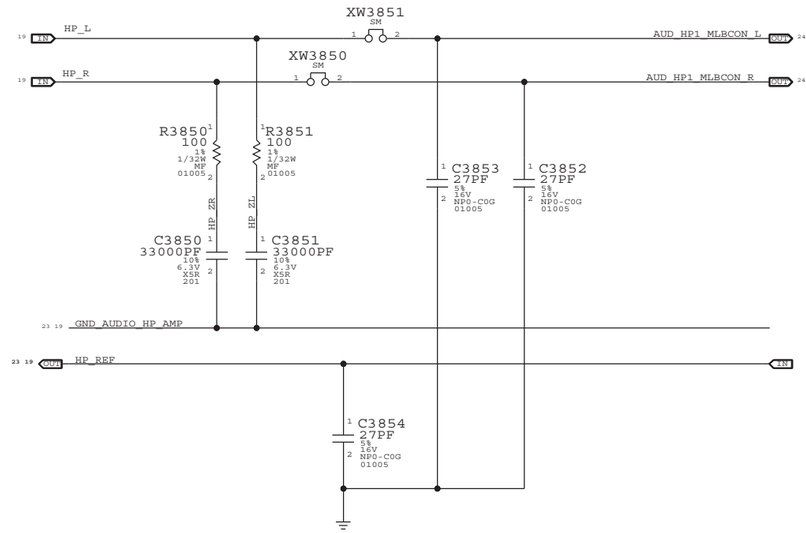
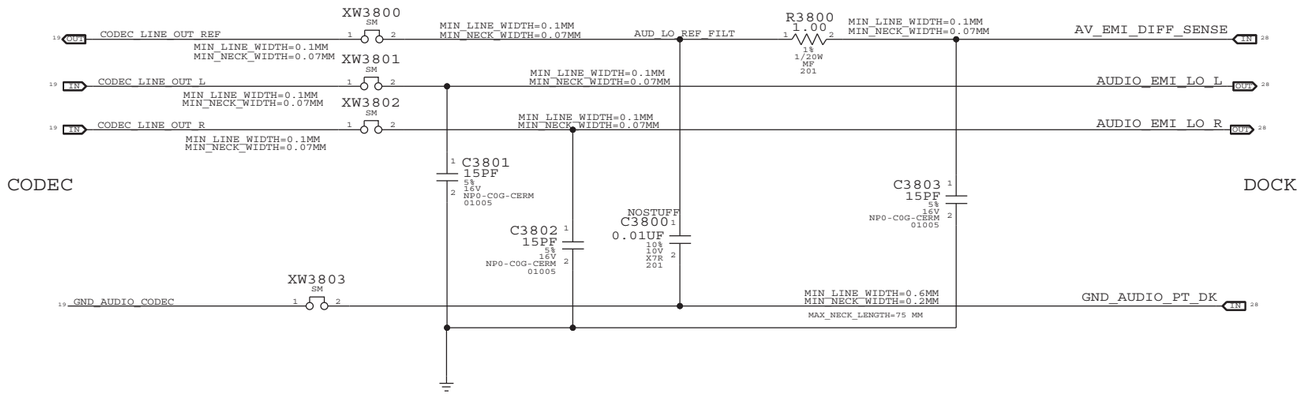
HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

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SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE

AUDIO: BLANK

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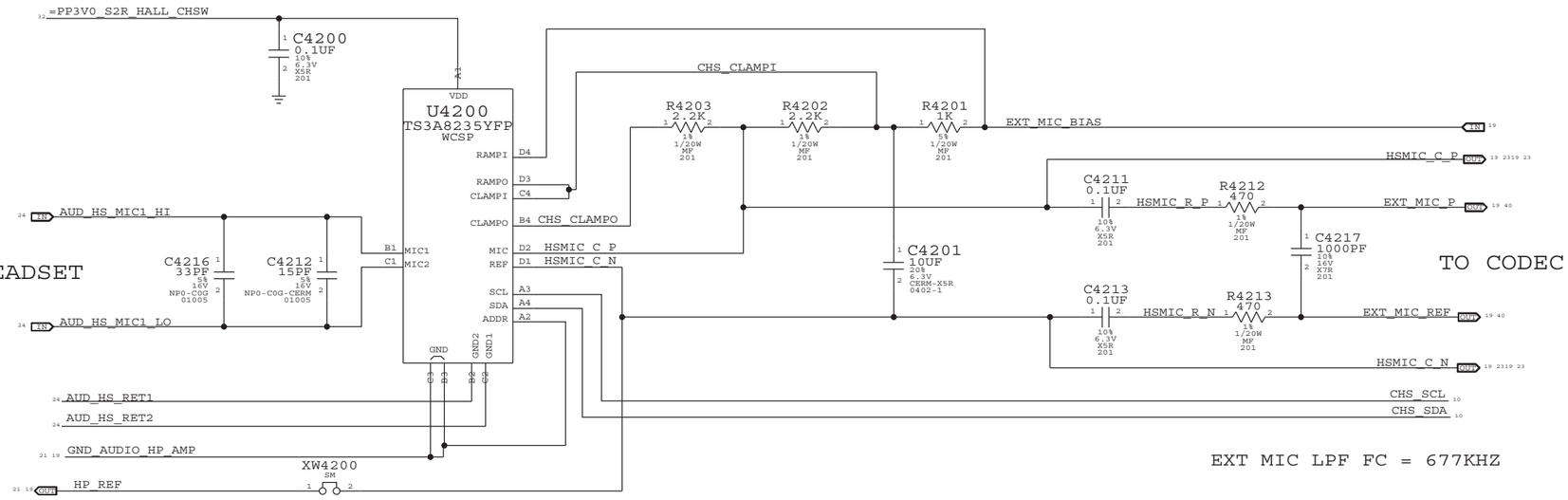
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



SYNC_MASTER=LENG	SYNC_DATE=N/A
PAGE TITLE	AUDIO: DETECT/MIC BIAS
Apple Inc.	DRAWING NUMBER 051-8962
	SIZE D
	REVISION A.0.0
	BRANCH
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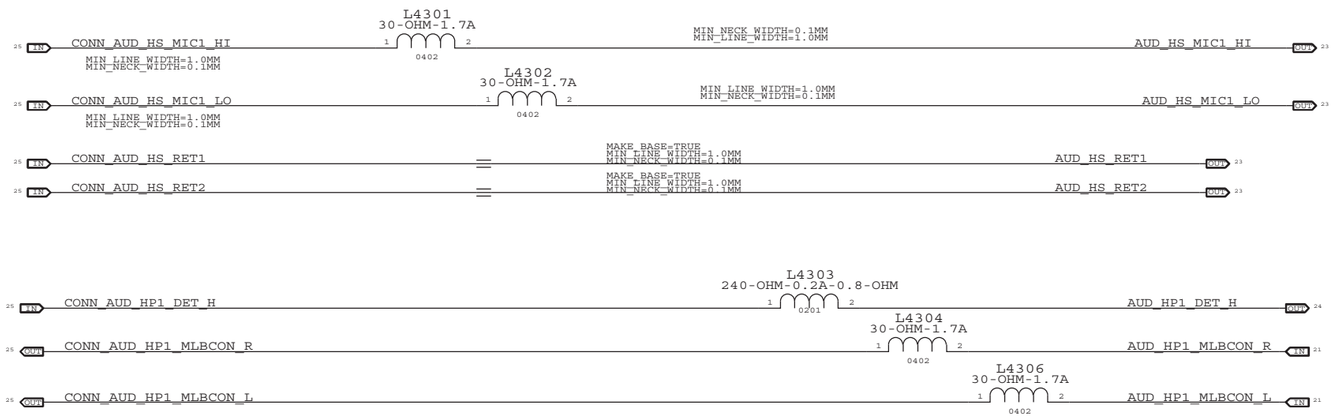
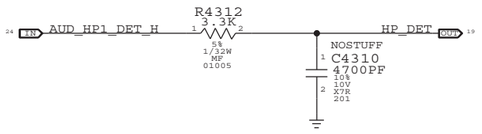
HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
PLACE ALL COMPONENTS NEAR J5501



HEADSET JACK INSERTION DETECT



SYNC MASTER=LENG
SYNC DATE=N/A

PAGE TITLE
AUDIO: HP/MIC FILTERS

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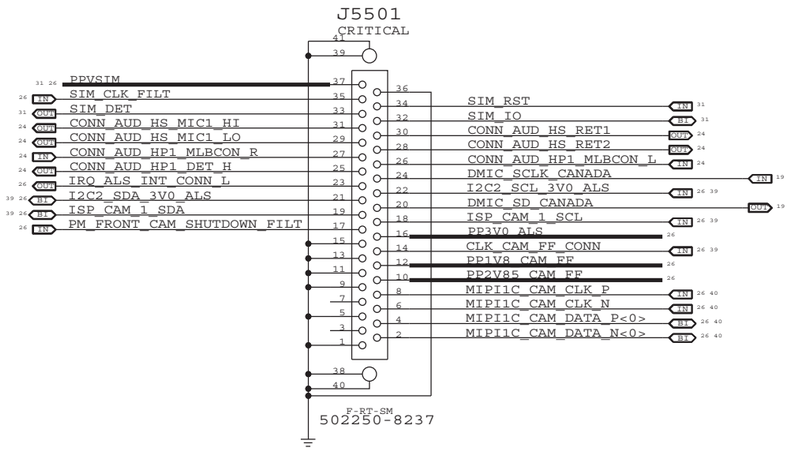
CANADA FLEXES CONN.

APN: 518S0817



SENSOR BOARD CONN ALIASES

39 27	CLK_CAM_RF_FILT	MAKE_BASE=TRUE	CONN_CLK_CAM_RF_FILT	27
40 27	MIPI0C_CAM_DATA_N<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_N<0>	27
40 27	MIPI0C_CAM_DATA_P<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_P<0>	27
		MAKE_BASE=TRUE		
40 27	MIPI0C_CAM_CLK_N	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_N	27
40 27	MIPI0C_CAM_CLK_P	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_P	27
7	PM_REAR_CAM_SHUTDOWN	MAKE_BASE=TRUE	CONN_PM_REAR_CAM_SHUTDOWN	27
27	PP1V8_SENSOR_FILT	MAKE_BASE=TRUE	CONN_PP1V8_SENSOR_FILT	27
27	PP2V85_CAM_REAR	MAKE_BASE=TRUE	CONN_PP2V85_CAM_REAR	27
19	DMIC_SD_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SD_SENSOR	27
19	DMIC_SCLK_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SCLK_SENSOR	27
39 7	ISP_AP_0_SCL	MAKE_BASE=TRUE	CONN_ISP_AP_0_SCL	27
39 7	ISP_AP_0_SDA	MAKE_BASE=TRUE	CONN_ISP_AP_0_SDA	27
39 26 5	I2C2_SCL_3V0	MAKE_BASE=TRUE	CONN_I2C2_SCL_3V0	27
39 26 5	I2C2_SDA_3V0	MAKE_BASE=TRUE	CONN_I2C2_SDA_3V0	27
5	IRQ_ACCEL_INT1_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT1_L	27
5	IRQ_ACCEL_INT2_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT2_L	27
5	IRQ_GYRO_INT1	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT1	27
5	IRQ_GYRO_INT2	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT2	27
39 5	I2C1_SCL_1V8	MAKE_BASE=TRUE	CONN_I2C1_SCL_1V8	27
39 5	I2C1_SDA_1V8	MAKE_BASE=TRUE	CONN_I2C1_SDA_1V8	27
35	IRQ_HALL	MAKE_BASE=TRUE	CONN_IRQ_HALL	27
5	IRQ_PROX_INT_L	MAKE_BASE=TRUE	CONN_IRQ_PROX_INT_L	27
27	PP3V0_S2R_HALL_FILT	MAKE_BASE=TRUE	CONN_PP3V0_S2R_HALL	27
35 5	ONOFF_L	MAKE_BASE=TRUE	CONN_ONOFF_FTR_L	27
35 5	SRL_L	MAKE_BASE=TRUE	CONN_SRL_FTR_L	27
5	AUD_VOL_UP_L	MAKE_BASE=TRUE	CONN_AUD_VOL_UP_FTR_L	27
5	AUD_VOL_DOWN_L	MAKE_BASE=TRUE	CONN_AUD_VOL_DOWN_FTR_L	27
		MAKE_BASE=TRUE		
27	PP3V0_OPTICAL_SENS	MAKE_BASE=TRUE	CONN_PP3V0_OPTICAL_SENS	27

SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES

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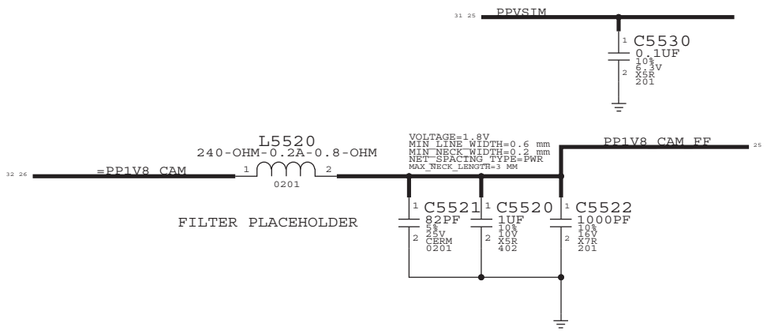
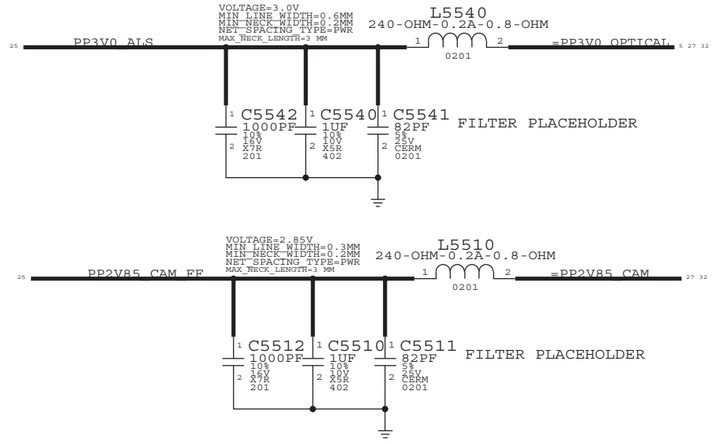
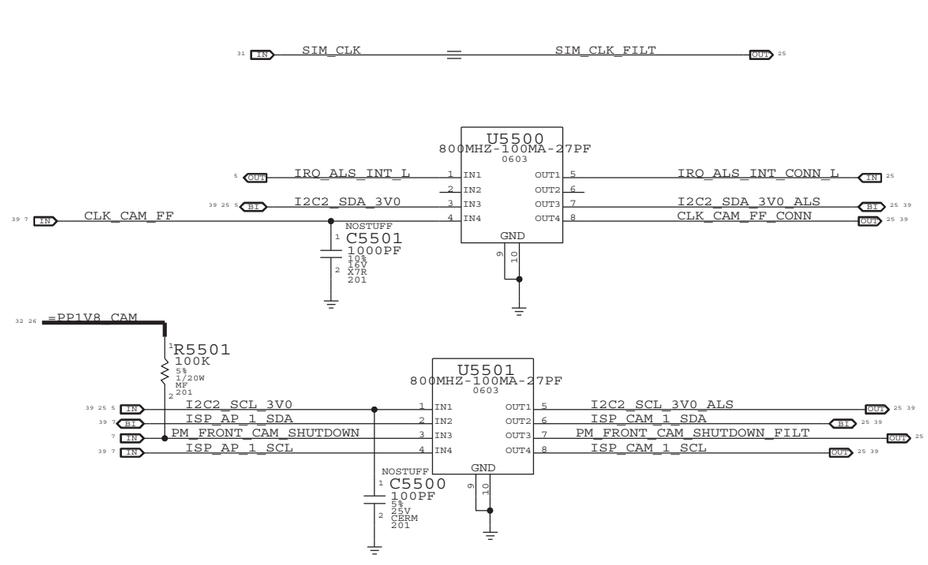
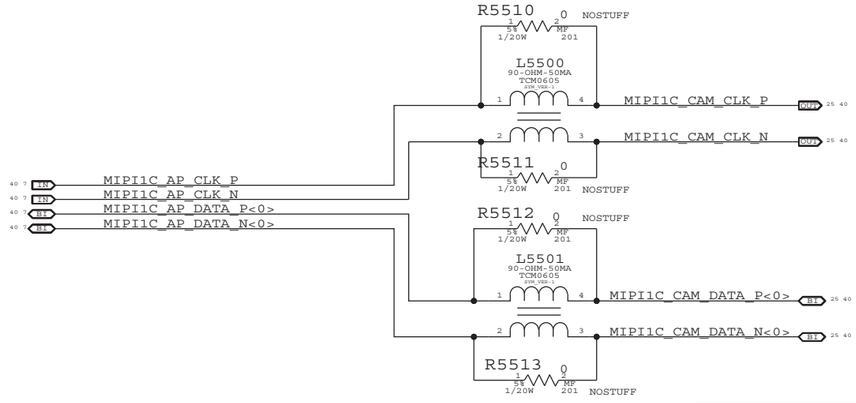


CANADA FLEX CONN ON PG 54



CANADA FLEX SIGNAL FILTERS





SYNC_MASTER=MARK_B. SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: CANADA FLEX FILTERS

Apple Inc.

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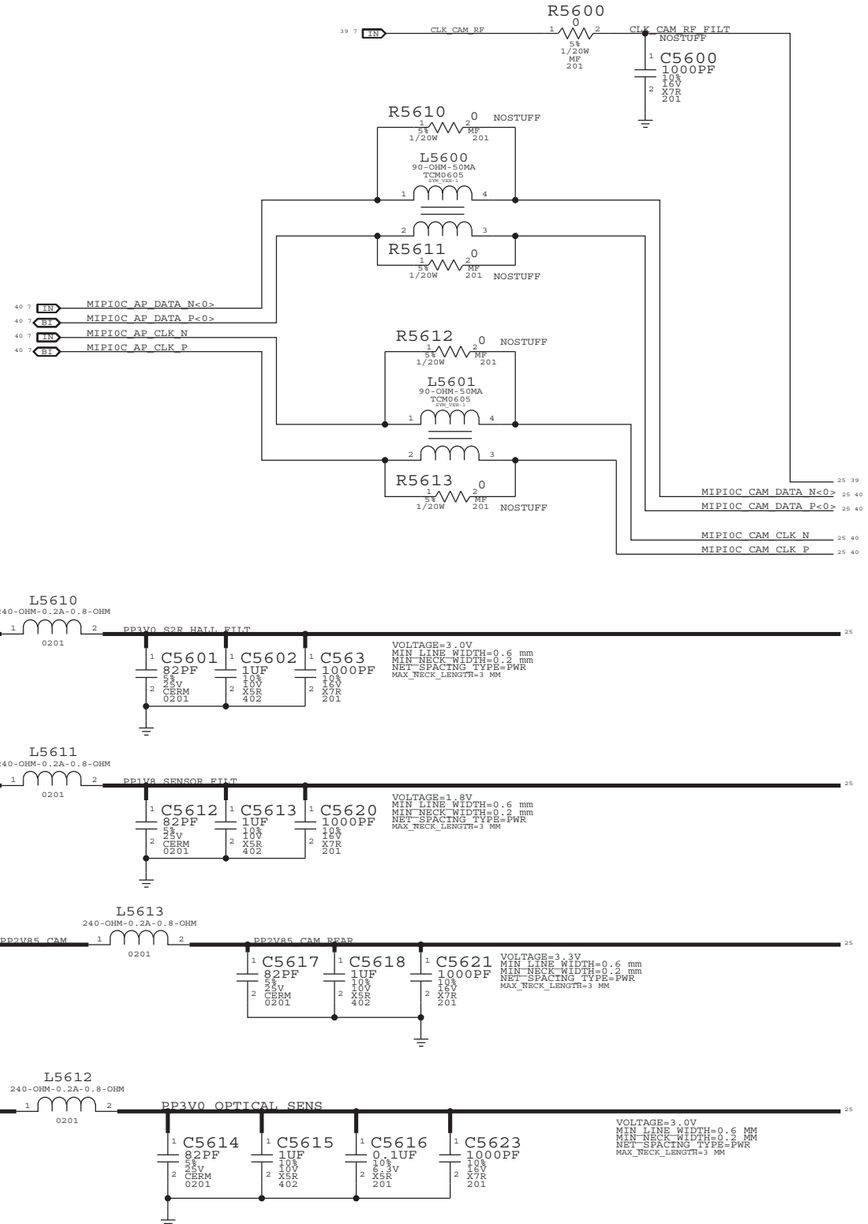
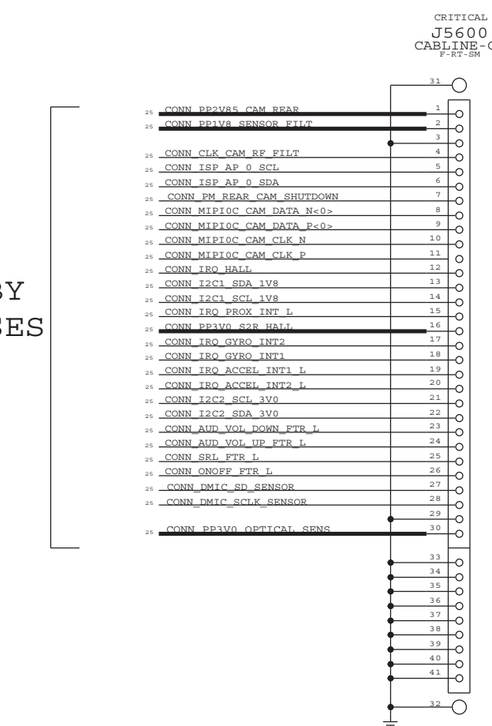


CONNECTED BY
PG 54 ALIASES

SENSOR PANEL CONNECTOR

CABLINE-CA CONNECTOR: 518S0787



SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: SENSOR PANEL CONNECTOR

Apple Inc.

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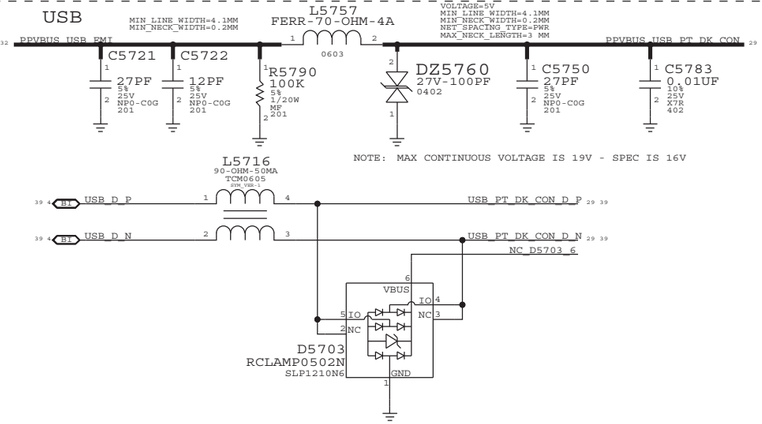
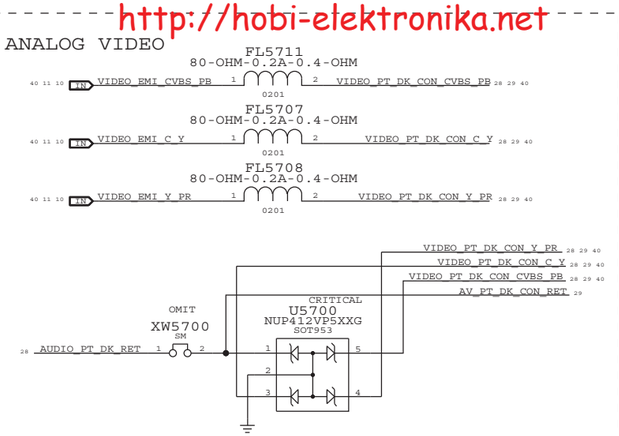
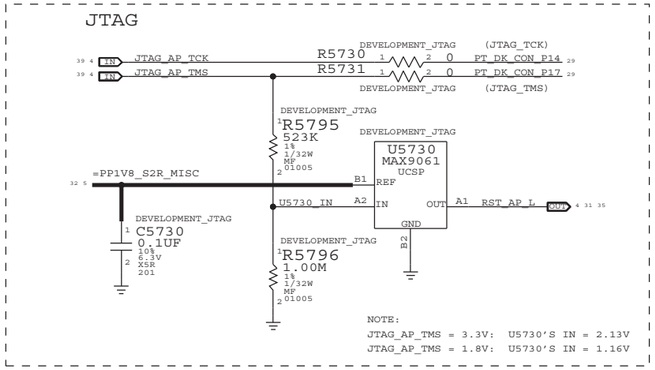
USB



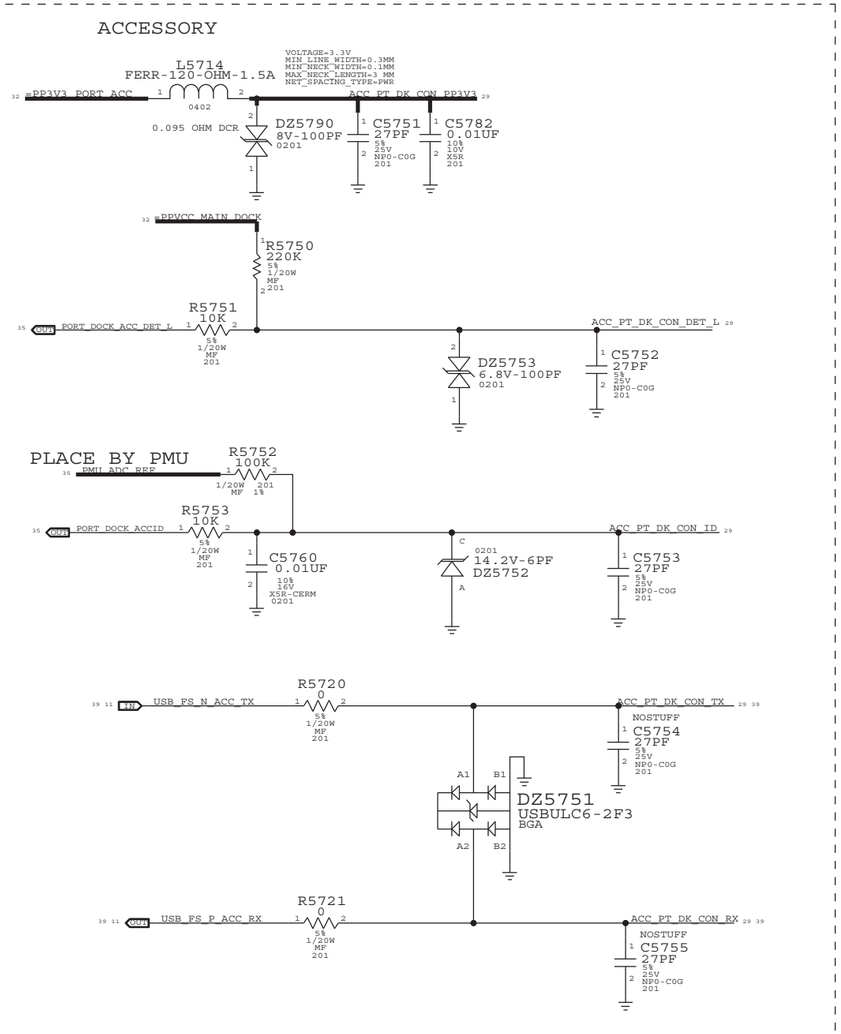
ANALOG VIDEO



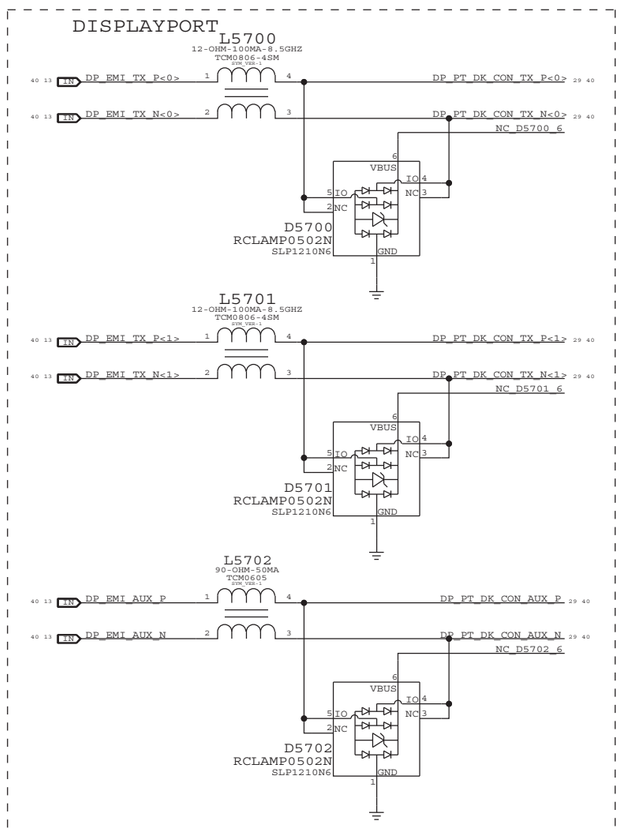
JTAG



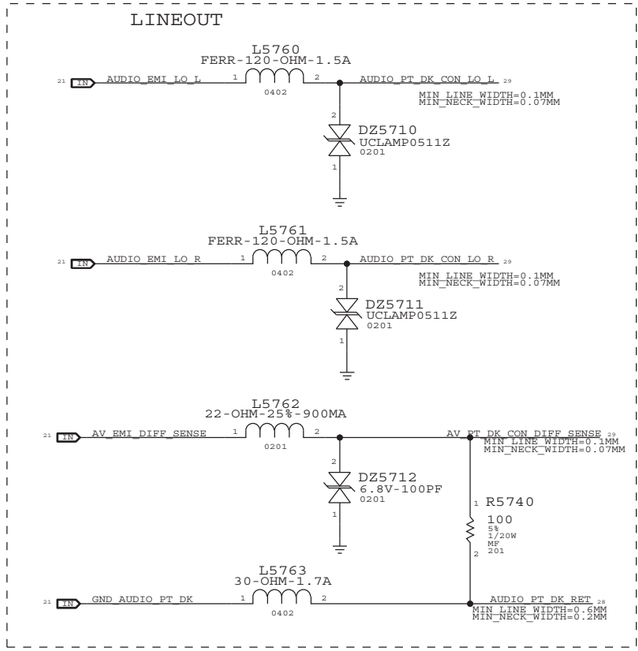
ACCESSORY



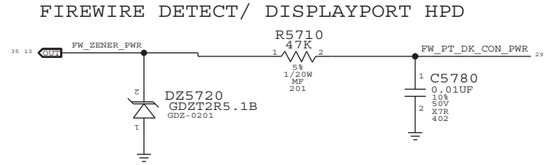
DISPLAYPORT



LINEOUT



FIREWIRE DETECT/ DISPLAYPORT HPD



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DZ5710,DZ5711	RADAR:8379541
377S0107	377S0066		DZ5700,DZ5701,DZ5702,DZ5712	RADAR:8289785
155S0625	155S0559		L5700,L5701	RADAR:8423156

SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE
IO FLEX: DOCK COMPONENTS

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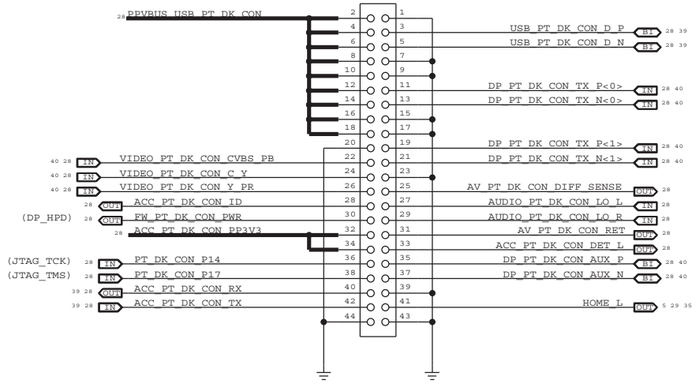
PN 516S0817 (PLUG - MALE)

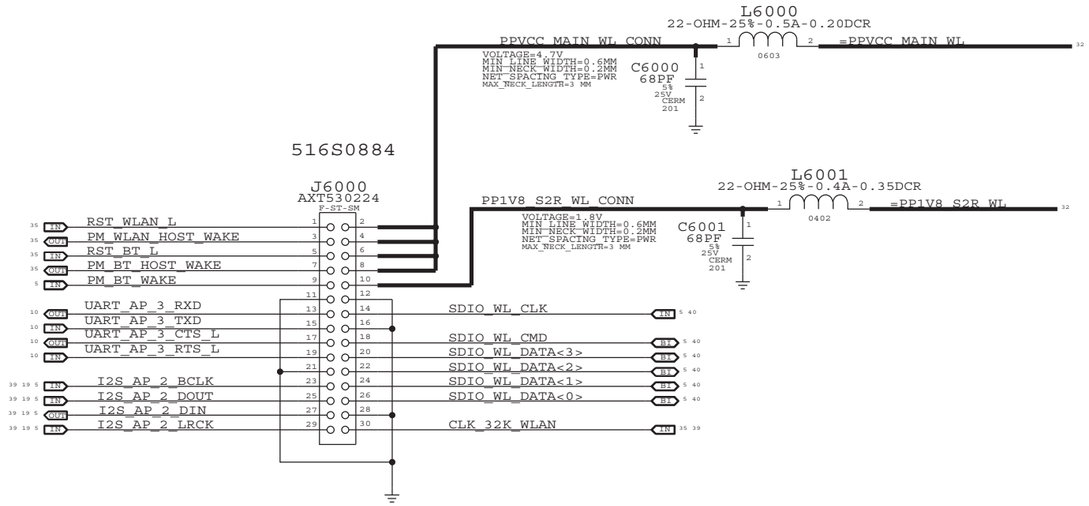
CRITICAL

J5900
AXK844135WG
M-ST-SM



SYNC_MASTER=JAMES	SYNC_DATE=N/A
PAGE TITLE: IO FELX: B2B Connector	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 59 OF 106
	SHEET: 29 OF 42

X23 WIFI/BT CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X23 WIFI/BT

Apple Inc.

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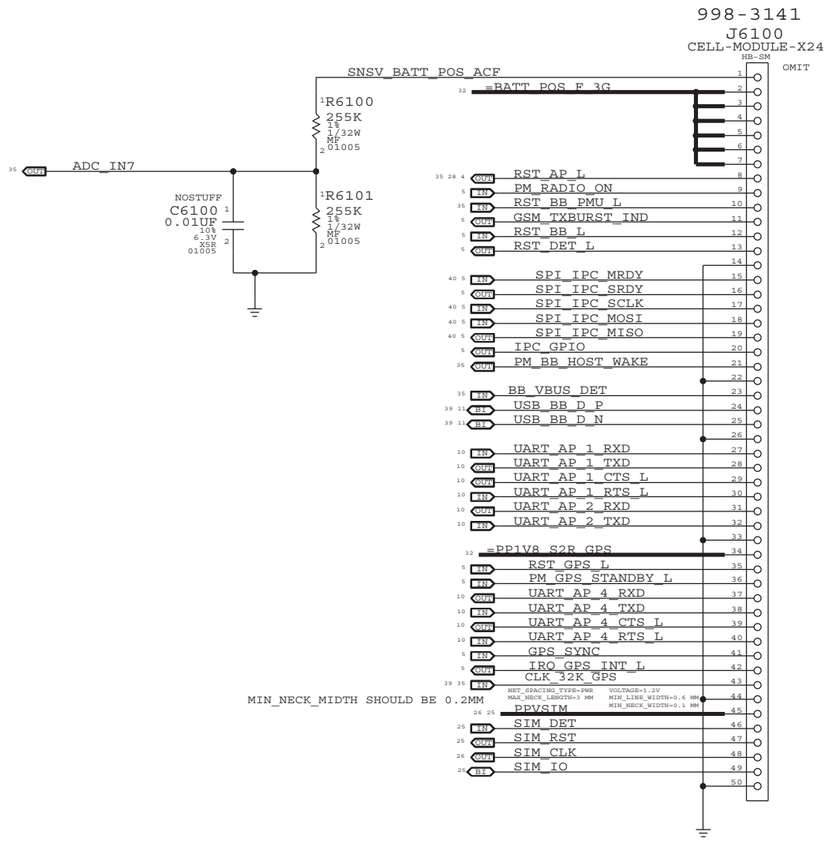
X24 CELLULAR/GPS CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X24 CELLULAR/GPS

Apple Inc.

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POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

34 PP3V0_S2R_HALL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_S2R_HALL (27)
→ =PP3V0_S2R_HALL_CHSW (23)

34 PP1V7_VA_VCP
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V7_VA_VCP (19)

34 PP3V0_VIDEO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_BUFFER (11)
→ =PP3V0_VIDEO_H4 (7)

34 PP3V0_OPTICAL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_OPTICAL (5 26 27)

34 PP3V2_SD
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V3_ACC
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V3_PORT_ACC (28)

34 PP3V0_VIDEO_BUF
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_VIDEO_BUF (11)

34 PP3V2_S2R_USBMUX
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V2_S2R_USBMUX (11)

34 PP3V0_IO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V0_IO_H4 (7 9)
→ =PP3V0_IO_MISC (13)

34 PP2V85_CAM
MAKE_BASE=TRUE
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP2V85_CAM (26 27)

34 PP3V0_GRAPE
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V0_GRAPE (17 18)
→ =PP3V0_GRAPE_Z1 (18)
→ =PP3V0_GRAPE_Z2 (18)
→ =PP3V0_GRAPE_MARIO1 (17)

34 PP1V1
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
→ =PP1V1_PLL_H4 (4)
→ =PP1V1_MIPI_H4 (7)
→ =PP1V1_DPORT_H4 (7)
→ =PP1V1_USB_H4 (4)
MIN_NECK_MIDTH SHOULD BE 0.2MM → =PP1V1_MIPI_PLL_H4 (4)

34 PP1V8_ALWAYS
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_ALWAYS (5)

BUCK RAILS

34 PP1V2_SOC
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PPVDD_SOC_H4 (9)

34 PP1V2_CPU
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PPVDD_CPU_H4 (9)

34 PP1V2_S2R
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP1V2_S2R_H4 (8)

34 PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP1V8_S2R_H4 (8)
→ =PP1V8_S2R_WL (30)
→ =PP1V8_S2R_GPS (31)
→ =PP1V8_S2R_MISC (5 28)

34 PP1V8
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP1V8_CAM (26)
→ =PP1V8_SENSOR (27)
→ =PP1V8_AUDIO (19)
→ =PP1V8_H4 (4 5 7 10 13)
→ =PP1V8_VDDIO18_H4 (8 9)
→ =PP1V8_MIPI_H4 (7)
→ =PP1V8_DPORT_H4 (7)

34 PP3V3_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP3V3_NAND (12)
→ =PP3V3_USB_H4 (4)
→ =PP3V3_MLC_HI (36)
→ =PP3V3_LCD (16)
→ =PP3V3_NAND_H4 (10)

35 PPLED_OUT
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPLED_REG (16)

36 PP3V3_MLC_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PP3V3_MLC (14 16)

34 PP1V2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
→ =PP1V2_VDDQ_H4 (8)
→ =PP1V2_VDDIOD_H4 (8)
→ =PP1V2_HSIC_H4 (4)

GND
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.10MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=5 MM

CHARGER MAIN

35 34 PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
→ =PPVCC_MAIN_AUDIO (19 20)
→ =PPVCC_MAIN_WL (30)
→ =PPVCC_MAIN_DOCK (28)
→ =PPVCC_MAIN_LED (35)

BATTERY

37 34 PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=1.7 MM
→ =BATT_POS_F_3G (31)
→ =BATT_POS_CONN (33)

USB POWER INPUT

28 PPVBUS_USB_EMI
PPVBUS_USB_DCIN (34)
MAKE_BASE=TRUE

SYNC_MASTER=YOSH SYNC_DATE=N/A
PAGE TITLE
POWER: ALIASES

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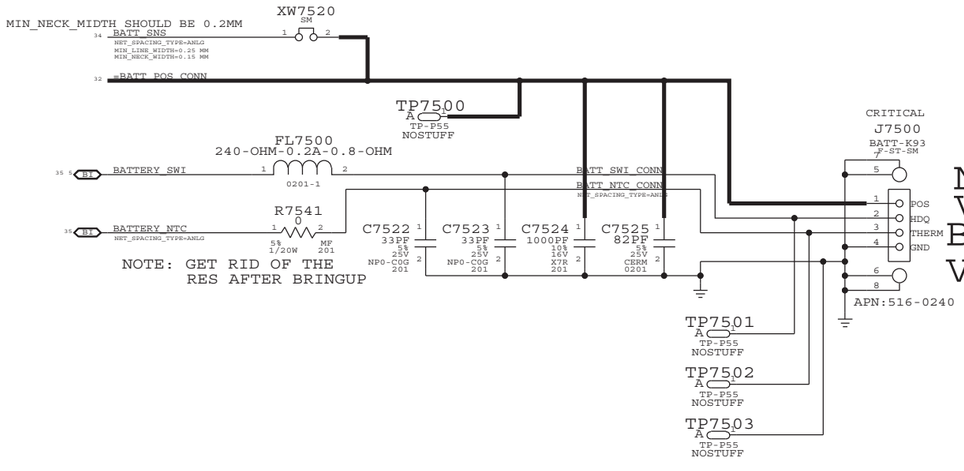

NOTE:
VERIFY PINOUT OF
BATTERY CONNECTOR
VERIFY MOUNTING CONN TO GND

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: BATTERY CONNECTOR

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0542	1	IC,PMU,ALISON,D1946A2,OTPXX,UFBGA292	U8100	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299		Y8138	ALT FOUNDRY

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

USB REVERSE VOLTAGE PROTECTION

CRITICAL Q8123 FDMC6676BZ MLP3.3X3.3

NOSTUFF R8116 470K 1% 1/20W MF 201

DZ8120 BZT52C10LP LLP CRITICAL NOTE: 10V ZENER

CRITICAL C8124 2.2UF 10% 25V X5R-CERM 805

LAYOUT NOTE: PLACE RIGHT AT THE PIN

C8125 10UF 10% 25V X5R 805 CRITICAL LAYOUT NOTE: PLACE RIGHT AT THE PIN

XW8114 SHORT-0201 NOSTUFF

R8130 220K 1% 1/20W MF 201

PPVBUS_USB_DCIN — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=ANLG MAX_NECK_LENGTH=3 MM VOLTAGE=6V

PPVBUS_PROT — MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.25MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=6V

VBUS_PROT_G — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=ANLG

NOTE: FOR NO BATTERY SITUATION

PPBATT_VCC — NOSTUFF CRITICAL C8100 22UF 20% 6.3V X5R-CERM 603; CRITICAL C8101 22UF 20% 6.3V X5R-CERM 603

R8100 0.5 1% 1/16W MF 402 — BATT_POS_RC — MIN_LINE_WIDTH=0.10MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=4.6V

VCC_MAIN BYPASS

TOTAL CAPS = ~400UF (DISTRIBUTED AND NO DE-RATING)

(PLACE ONE 1UF CAP AT EACH VDD INPUT)

PLACEMENT_NOTE=PLACE NEAR L8225.1

CRITICAL C8166 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B15G-SM; CRITICAL C8165 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B15G-SM

CRITICAL C8154 10UF 20% 6.3V X5R 603; CRITICAL C8155 10UF 20% 6.3V X5R 603

CRITICAL C8156 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8157 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8158 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8159 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8160 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8161 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8162 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8130 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL C8131 1.0UF 20% 6.3V X5R 0201-MUR

C8163 82PF 5% 25V CERM 0201

C8164 18PF 5% 25V NP0-C0G 201

PPVCC_MAIN

NOTE: CONCERNED ABOUT ESR > 20MOHM

CRITICAL L8112 2.2UH-3.5A-54M-OHM PIME061E-SM DCR=54MOHM MAX

SW_CHGA — D8100 PMEG4030ER SOD-123W CRITICAL

Q8104 FDMC6683 MLP3.3X3.3 — RDSON=0.0136@VGS=-2.5V ID=12.0A

NC_CHGB; BATT_SNS; PPBATT_VCC; ACT_DIO

PPVBUS_USB 2 — XW8114 SHORT-0201 NOSTUFF — PPVBUS_PROT

NC_VBUS_A_OV_N; PMU_VCENTER — MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.25MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=6V

NC_VBUS_B_OV_N

OMIT

U8100 ALISON-A0-OTPXX D1946A0-110-00 UFBGA (SYM 2 OF 3)

G24	CHG_A_LX		
G25			
H24	NC_CHGB		
H25	CHG_B_LX		
L25	VBAT		
P25	IBAT_S		
N17	IBAT		
P17			
N18			
P18			
P24	ACT_DIO		
F24	VCENTER_A		
F25			
A22	VBUS_A		
A23			
B24	VBUS_A_OV_N		
J24	VCENTER_B		
J25			
P22	VBUS_B		
P23			
N22	VBUS_B_OV_N		
A10	VDD_BUCK0		
B10			
A3	VDD_BUCK2		
B3			
B7			
B6			
A17	VDD_BUCK3		
A13	VDD_BUCK4		
B13			
E1	VDD_BUCK5		
E2			
G1	VDD_BUCK5_BYP		
G2			
H2			
G22	VCC_MAIN_S		
N19	VCC_MAIN		
P19			
N20			
P20			
K2	VDD_LDO1_6		
L4	VDD_LDO2		
N9	VDD_LDO3_5_8		
N4	VDD_LDO4_7		
N10	VDD_LDO9		
N6	VDD_LDO10		
L2	VDD_LDO11		
N7	VDD_LDO12		
P1	XTAL1		
P2	XTAL2		
A11	BUCK0_LXL	BUCK	
A9	BUCK0_LXM		
D9	BUCK0_FB		
A7	BUCK2_LXL		
B8			
A6	BUCK2_LXM		
A4	BUCK2_LXR		
D7	BUCK2_FB		
A16	BUCK3_LX		
D16	BUCK3_FB		
A14	BUCK4_LXL		
B11	BUCK4_LXM		
D14	BUCK4_FB		
F1	BUCK5_LX		
F2			
H1	BUCK5_BYP		
J1			
J2			
G4	BUCK5_FB		
L1	VLDO1 (150MA; 2.5-3.55V)	LDO	PP3V0_GRAPE
P3	VLDO2 (100MA; 1.65-1.805V; BUCK3)		PP1V7_VA_VCP
P9	VLDO3 (50MA; 2.5-3.3V)		PP3V0_VIDEO
N5	VLDO4 (100MA; 1.8-3.3V)		PP3V0_OPTICAL
P10	VLDO5 (300MA; 2.5-3.6V)		PP3V2_SD
K1	VLDO6 (150MA; 2.5-3.6V)		PP3V3_ACC
P4	VLDO7 (50MA; 1.5-3.3V)		PP3V0_VIDEO_BUF
P8	VLDO8 (10MA; 2.0-3.55V)		PP3V2_S2R_USBMUX
P11	VLDO9 (300MA; 1.2-3.0V)		PP3V0_IO
P5	VLDO10 (200MA; 2.5-3.55V)		PP3V0_S2R_HALL
M1	VLDO11 (200MA; 1.7-3.0V)		PP2V85_CAM
P6	VLDO12 (150MA; 0.6-1.3V)		PP1V1
M2	ON_BUF		PP1V8_ALWAYS
B17	VBUCK4	SWITCH POWER	PP1V2_S2R
A18	CPU1V2_SW (RON=0.1 OHM MAX)		PP1V2
B20	DSP_SW (RON=1 OHM MAX)		DSP_SW
A19	VBUCK3		PP1V8_S2R
A20	CPU1V8_SW (RON=0.2 OHM MAX)		PP1V8
B19	WDIG_SW (RON=0.5 OHM MAX)		PP1V8_GRAPE
B21	VBUCK0_SW0_G		NC_PMU_VBUCK0_SW0_G
A21	VBUCK0_SW0_S		NC_PMU_VBUCK0_SW0_S
B18	VPUMP		PMU_VPUMP

(BYPASS RON=0.14 OHM MAX)

PPBATT_VCC; PPVCC_MAIN; PP1V2_S2R

C8135 1UF 10% 6.3V CERM 402

C8136 1UF 10% 6.3V CERM 402

NET_SPACING_TYPE=CRYSTAL

CRITICAL Y8138 32.768K-20PPM-12.5PF PMU_XTAL PMU_EXTAL 2012

C8142 18PF 5% 25V NP0-C0G 201

C8143 18PF 5% 25V NP0-C0G 201

C8137 0.01UF 10% 6.3V X5R 01005 — MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=4.6V

LDO BYPASS

PP3V0_GRAPE; PP1V7_VA_VCP; PP3V0_VIDEO; PP3V0_OPTICAL; PP3V2_SD; PP3V3_ACC; PP3V0_VIDEO_BUF

CRITICAL C8150 2.2UF 10% 6.3V X5R 402; CRITICAL C8149 2.2UF 10% 6.3V X5R 402; CRITICAL C8148 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8146 2.2UF 10% 6.3V X5R 402; CRITICAL C8145 2.2UF 10% 6.3V X5R 402; CRITICAL C8144 10UF 20% 6.3V CERM-X5R 0402; CRITICAL C8147 2.2UF 10% 6.3V X5R 402

PP3V2_S2R_USBMUX; PP3V0_IO; PP3V0_S2R_HALL; PP2V85_CAM; PP1V1; PP1V8_ALWAYS

CRITICAL C8169 0.22UF 20% 6.3V X5R 0201; CRITICAL C8168 2.2UF 10% 6.3V X5R 402; CRITICAL C8167 2.2UF 10% 6.3V X5R 402; CRITICAL C8153 2.2UF 10% 6.3V X5R 402; CRITICAL C8152 4.7UF 20% 6.3V X5R-CERM1 402; CRITICAL C8151 1UF 10% 6.3V CERM 402

CRITICAL L8100 2.2UH-20%-1.85A-80MOHM PST25201B-SM

CRITICAL L8101 2.2UH-20%-1.85A-80MOHM PST25201B-SM

XW8103 SM NOSTUFF

CRITICAL L8105 2.2UH-20%-1.85A-80MOHM PST25201B-SM

CRITICAL L8107 2.2UH-20%-1.85A-80MOHM PST25201B-SM

CRITICAL L8110 2.2UH-20%-1.85A-80MOHM PST25201B-SM

XW8113 SM NOSTUFF

CRITICAL L8115 2.2UH-20%-1.85A-80MOHM PST25201B-SM

XW8117 SM NOSTUFF

CRITICAL L8119 2.2UH-20%-1.85A-80MOHM PST25201B-SM

CRITICAL L8121 2.2UH-20%-1.85A-80MOHM PST25201B-SM

XW8126 SM NOSTUFF

CRITICAL L8128 2.2UH-20%-3.3A-0.064OHM PIME051E-SM DCR=64MOHM MAX

XW8132 SM NOSTUFF

PP1V2_CPU — ADDITIONAL DISTRIBUTED 25UF (NO DE-RATING)

CRITICAL C8102 22UF 20% 6.3V X5R-CERM 603; CRITICAL C8103 22UF 20% 6.3V X5R-CERM 603

PP1V2_SOC — ADDITIONAL DISTRIBUTED 30UF (NO DE-RATING)

CRITICAL C8107 22UF 20% 6.3V X5R-CERM 603; CRITICAL C8108 22UF 20% 6.3V X5R-CERM 603

PP1V8_S2R — ADDITIONAL DISTRIBUTED 14UF (NO DE-RATING)

CRITICAL C8117 22UF 20% 6.3V X5R-CERM 603; CRITICAL C8118 22UF 20% 6.3V X5R-CERM 603

PP1V2_S2R — ADDITIONAL DISTRIBUTED 20UF (NO DE-RATING)

CRITICAL C8121 22UF 20% 6.3V X5R-CERM 603; CRITICAL C8122 10UF 20% 6.3V X5R 603

PP3V3_OUT — ADDITIONAL DISTRIBUTED 47UF (NO DE-RATING)

CRITICAL C8119 22UF 20% 6.3V X5R-CERM 603; CRITICAL C8120 22UF 20% 6.3V X5R-CERM 603

TP8133 TP-P55 NOSTUFF

TP8101 TP-P55 NOSTUFF

CRITICAL C8138 1UF 10% 6.3V X5R 0201; CRITICAL C8140 1UF 10% 6.3V CERM 402; CRITICAL C8139 1UF 10% 6.3V CERM 402; CRITICAL C8141 1UF 10% 6.3V CERM 402

ADDITIONAL DISTRIBUTED:
PP1V2: 30UF (NO DE-RATING)
PP1V8: 6UF (NO DE-RATING)

SYNC_MASTER=YOSH — SYNC_DATE=N/A

PAGE TITLE: POWER: PMU

Apple Inc.

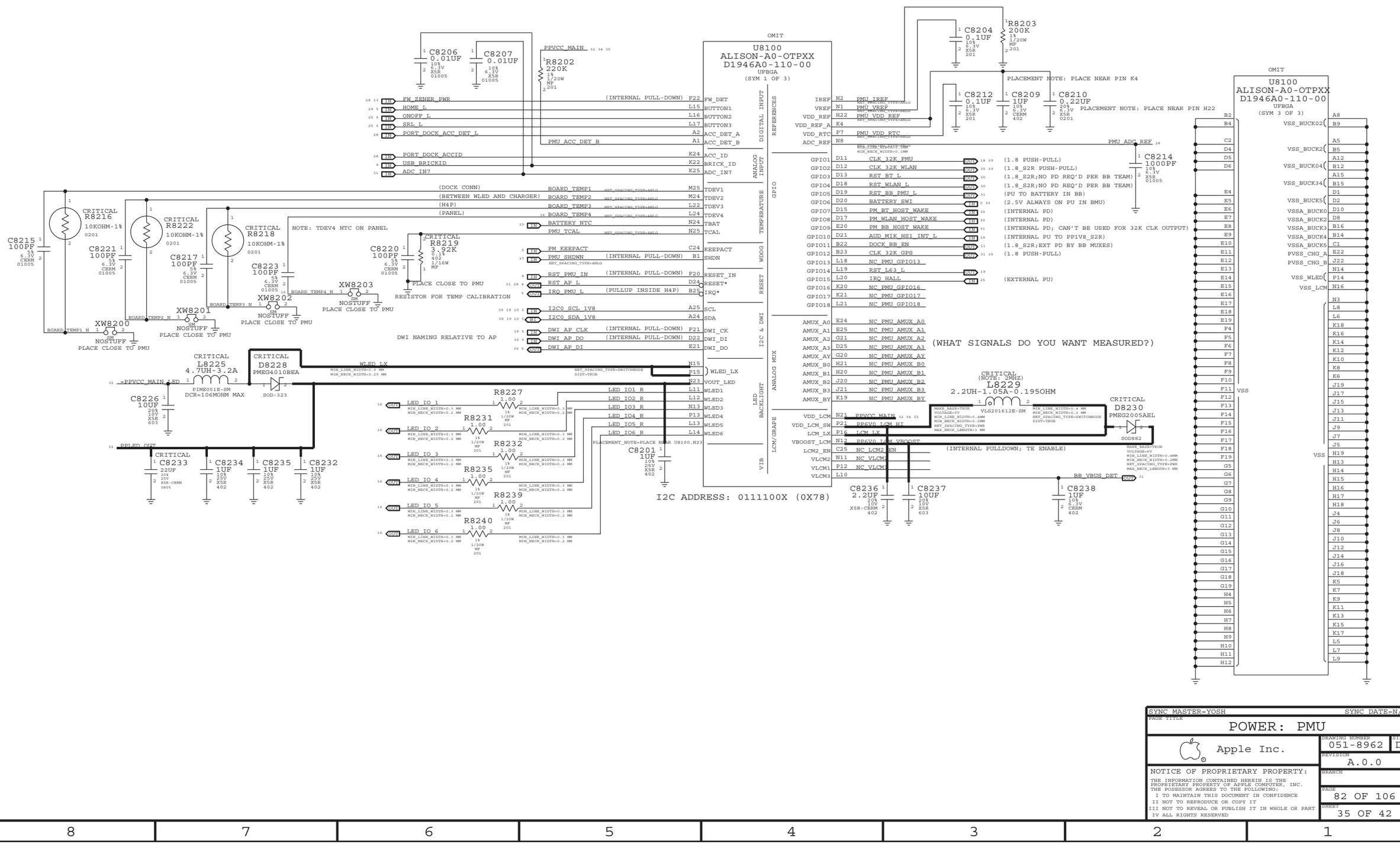
DRAWING NUMBER: 051-8962 — SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 81 OF 106

SHEET: 34 OF 42



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PAGE TITLE	POWER: PMU
Apple Inc.	DRAWING NUMBER 051-8962 · SIZE D
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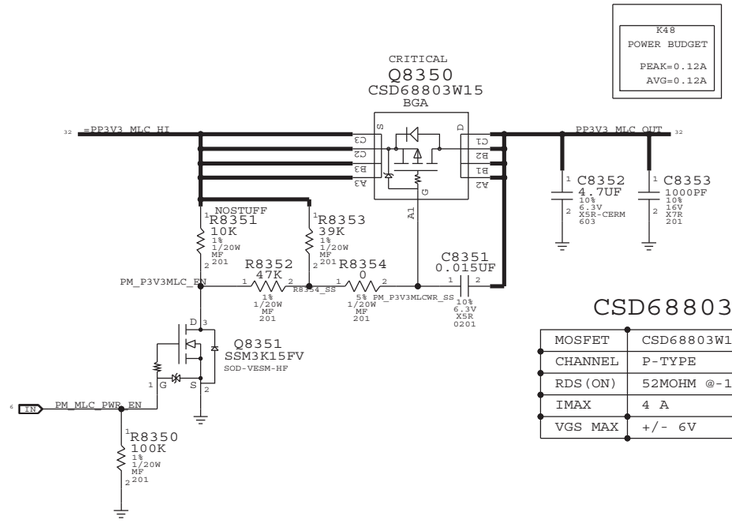
	BRANCH
	PAGE 82 OF 106
	SHEET 35 OF 42



K48
POWER BUDGET
PEAK=0.12A
AVG=0.12A

CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS(ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0972	376S0612		Q8351	RADAR:8537160

SYNC MASTER=YOSH SYNC DATE=N/A

PAGE TITLE
POWER: 3.3V MLC & 1.2V VR

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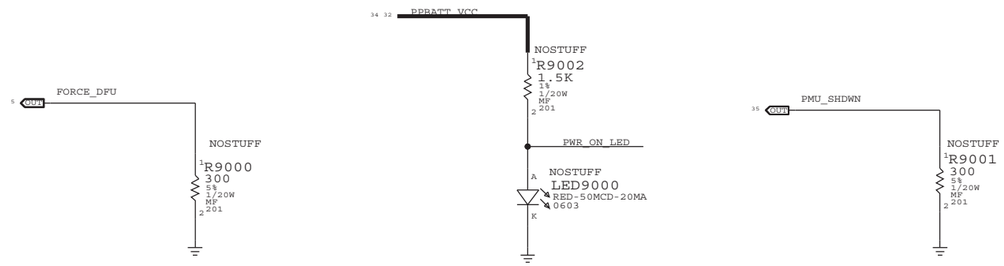
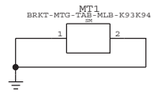
DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: DEBUG AND MISC

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PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
FCT/ICT TEST/BRACKETS

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I63	CLK_50S	CLK	CLK_32K_PMU 18 35
I162	CLK_50S	CLK	CLK_32K_WLAN 30 35
I61	CLK_50S	CLK	CLK_32K_GPS 31 35
I88	CLK_50S	CLK	CLK_CAM_FF 7 26
I80	CLK_50S	CLK	CLK_CAM_FF_FILT
I95	CLK_50S	CLK	CLK_CAM_FF_CONN 25 26
I96	CLK_50S	CLK	CLK_CAM_RF 7 27
I94	CLK_50S	CLK	CLK_CAM_RF_FILT 25 27
I130	CLK_50S	CLK	I2S_AP_0_MCK 5
I132	CLK_50S	CLK	I2S_AP_0_MCK_R 5 19
I155	CLK_50S	CLK	CLK_CAM_FF_R 7
I158	CLK_50S	CLK	CLK_CAM_RF_R 7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I150	NAND_50S	NAND	F0AD<7..0> 6 12
I145	NAND_50S	NAND	F0CE0_L 6 12
I148	NAND_50S	NAND	F0CE1_L 6 12
I147	NAND_50S	NAND	F0CE2_L 6 12
I146	NAND_50S	NAND	F0CE3_L 6 12
I143	NAND_50S	NAND	F0CE4_L 6 12
I144	NAND_50S	NAND	F0CE5_L 6 12
I140	NAND_50S	NAND	F0CE6_L 6 12
I165	NAND_50S	NAND	F0CE7_L 6 12
I141	NAND_50S	NAND	F0CLE 6 12
I142	NAND_50S	NAND	F0ALE 6 12
I163	NAND_50S	NAND	F0RE_L 6 12
I164	NAND_50S	NAND	F0WE_L 6 12
I137	NAND_50S	NAND	F0WP_L
I149	NAND_50S	NAND	F1AD<7..0> 6 12
I151	NAND_50S	NAND	F1CE0_L 6 12
I152	NAND_50S	NAND	F1CE1_L 6 12
I153	NAND_50S	NAND	F1CE2_L 6 12
I154	NAND_50S	NAND	F1CE3_L 6 12
I167	NAND_50S	NAND	F1CE4_L 6 12
I160	NAND_50S	NAND	F1CE5_L 6 12
I161	NAND_50S	NAND	F1CE6_L 6 12
I170	NAND_50S	NAND	F1CE7_L 6 12
I155	NAND_50S	NAND	F1CLE 6 12
I156	NAND_50S	NAND	F1ALE 6 12
I157	NAND_50S	NAND	F1RE_L 6 12
I158	NAND_50S	NAND	F1WE_L 6 12
I159	NAND_50S	NAND	F1WP_L 6 12
I100	NAND_50S	NAND	F2AD<7..0>
I102	NAND_50S	NAND	F2CE0_L
I106	NAND_50S	NAND	F2CE1_L
I108	NAND_50S	NAND	F2CE2_L
I107	NAND_50S	NAND	F2CE3_L
I105	NAND_50S	NAND	F2CLE
I110	NAND_50S	NAND	F2ALE
I111	NAND_50S	NAND	F2RE_L
I131	NAND_50S	NAND	F2WE_L
I113	NAND_50S	NAND	F2WP_L
I114	NAND_50S	NAND	F3AD<7..0>
I115	NAND_50S	NAND	F3CE0_L
I116	NAND_50S	NAND	F3CE1_L
I117	NAND_50S	NAND	F3CE2_L
I118	NAND_50S	NAND	F3CE3_L
I119	NAND_50S	NAND	F3CLE
I120	NAND_50S	NAND	F3ALE
I121	NAND_50S	NAND	F3RE_L
I122	NAND_50S	NAND	F3WE_L
I123	NAND_50S	NAND	F3WP_L

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I16		JTAG	JTAG_AP_TCK 4 28
I15		JTAG	JTAG_AP_TMS 4 28
I14		JTAG	JTAG_AP_TDI 4 10
I13		JTAG	JTAG_AP_TDO 4 10
I20		JTAG	JTAG_AP_TRST_L 4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I1	I2C_50S	I2C	I2C1_SDA_1V8 5 25
I2	I2C_50S	I2C	I2C1_SCL_1V8 5 25
I3	I2C_50S	I2C	I2C0_SDA_1V8 5 10 19 35
I4	I2C_50S	I2C	I2C0_SCL_1V8 5 10 19 35
I91	I2C_50S	I2C	I2C2_SDA_3V0 5 25 26
I92	I2C_50S	I2C	I2C2_SCL_3V0 5 25 26
I98	I2C_50S	I2C	ISP_AP_0_SCL 7 25
I99	I2C_50S	I2C	ISP_AP_0_SDA 7 25
I100	I2C_50S	I2C	ISP_AP_1_SCL 7 26
I101	I2C_50S	I2C	ISP_AP_1_SDA 7 26
I105	I2C_50S	I2C	I2C2_SCL_3V0_ALS 25 26
I104	I2C_50S	I2C	I2C2_SDA_3V0_ALS 25 26
I124	I2C_50S	I2C	ISP_CAM_1_SCL 25 26
I125	I2C_50S	I2C	ISP_CAM_1_SDA 25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I92		CRYSTAL	XTAL_24M_I 4
I90		CRYSTAL	XTAL_24M_O 4
I91		CRYSTAL	24M_O 4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I133		VREF	PPVREF_DDR0_CA 8
I131		VREF	PPVREF_DDR0_DQ 8
I135		VREF	PPVREF_DDR1_CA 8
I137		VREF	PPVREF_DDR1_DQ 8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I5	USB_90D	USB	USB_D_P 4 28
I6	USB_90D	USB	USB_D_N 4 28
I7	USB_90D	USB	USB_PT_DK_CON_D_P 28 29
I8	USB_90D	USB	USB_PT_DK_CON_D_N 28 29
I82	USB_90D	USB	USB_BB_D_P 11 31
I83	USB_90D	USB	USB_BB_D_N 11 31
I84	USB_90D	USB	USB_FS_D_P 4 11
I85	USB_90D	USB	USB_FS_D_N 4 11
I129	USB_90D	USB	USB_FS_N_ACC_TX 11 28
I128	USB_90D	USB	USB_FS_P_ACC_RX 11 28
I127	USB_90D	USB	ACC_PT_DK_CON_TX 28 29
I126	USB_90D	USB	ACC_PT_DK_CON_RX 28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I180	I2S_50S	I2S	I2S_AP_0_BCLK 5 19
I181	I2S_50S	I2S	I2S_AP_0_LRCK 5 19
I182	I2S_50S	I2S	I2S_AP_0_DIN 5 19
I183	I2S_50S	I2S	I2S_AP_0_DOUT 5 19
I186	I2S_50S	I2S	L63_ASP_SDOUT 19
I187	I2S_50S	I2S	I2S_AP_2_BCLK 5 19 30
I188	I2S_50S	I2S	I2S_AP_2_LRCK 5 19 30
I189	I2S_50S	I2S	I2S_AP_2_DIN 5 19 30
I190	I2S_50S	I2S	I2S_AP_2_DOUT 5 19 30
I191	I2S_50S	I2S	L63_VSP_SDOUT 19
I192	I2S_50S	I2S	I2S_AP_3_BCLK 5 19
I193	I2S_50S	I2S	I2S_AP_3_LRCK 5 19
I194	I2S_50S	I2S	I2S_AP_3_DIN 5 19
I195	I2S_50S	I2S	I2S_AP_3_DOUT 5 19
I196	I2S_50S	I2S	L63_XSP_SDOUT 19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
I198		DWI	DWI_AP_CLK 5 35
I199		DWI	DWI_AP_DI 5 35
I200		DWI	DWI_AP_DO 5 35

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONSTRAINTS: ASSIGNMENTS

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DRAWING NUMBER 051-8962 SIZE D

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ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E213	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
E214	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
E215	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
E216	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
E217	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
E218	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
E219	VID_50S	ANALOG_VIDEO	VIDEO_EMI_CVBS_PB 10 11 28
E220	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 28
E221	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 28
E222	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 28 29
E223	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 28 29
E224	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 28 29
E225	VID_50S	ANALOG_VIDEO	

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E236	LVDS_100D	LVDS	LVDS_DATA_P<2..0> 14 16
E237	LVDS_100D	LVDS	LVDS_DATA_N<2..0> 14 16
E238	LVDS_100D	LVDS	LVDS_DATA_CONN_P<2..0> 16
E239	LVDS_100D	LVDS	LVDS_DATA_CONN_N<2..0> 16
E240	LVDS_100D	LVDS	LVDS_CLK_P 14 16
E241	LVDS_100D	LVDS	LVDS_CLK_N 14 16
E242	LVDS_100D	LVDS	LVDS_CLK_CONN_P 16
E243	LVDS_100D	LVDS	LVDS_CLK_CONN_N 16

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E91	MIPI_100D	MIPI	MIPID_AP_DATA_P<0> 7 14
E92	MIPI_100D	MIPI	MIPID_AP_DATA_N<0> 7 14
E93	MIPI_100D	MIPI	MIPID_AP_DATA_P<1> 7 14
E94	MIPI_100D	MIPI	MIPID_AP_DATA_N<1> 7 14
E95	MIPI_100D	MIPI	MIPID_AP_DATA_P<2> 7 14
E96	MIPI_100D	MIPI	MIPID_AP_DATA_N<2> 7 14
E97	MIPI_100D	MIPI	MIPID_AP_DATA_P<3> 7 14
E270	MIPI_100D	MIPI	MIPID_AP_DATA_N<3> 7 14
E97	MIPI_100D	MIPI	MIPID_AP_CLK_P 7 14
E98	MIPI_100D	MIPI	MIPID_AP_CLK_N 7 14
E331	MIPI_100D	MIPI	MIPI0C_AP_DATA_P<0> 7 27
E332	MIPI_100D	MIPI	MIPI0C_AP_DATA_N<0> 7 27
E333	MIPI_100D	MIPI	MIPI0C_AP_CLK_P 7 27
E334	MIPI_100D	MIPI	MIPI0C_AP_CLK_N 7 27
E343	MIPI_100D	MIPI	MIPI0C_CAM_DATA_P<0> 25 27
E344	MIPI_100D	MIPI	MIPI0C_CAM_DATA_N<0> 25 27
E345	MIPI_100D	MIPI	MIPI0C_CAM_CLK_P 25 27
E346	MIPI_100D	MIPI	MIPI0C_CAM_CLK_N 25 27
E347	MIPI_100D	MIPI	MIPI1C_AP_DATA_P<0> 7 26
E348	MIPI_100D	MIPI	MIPI1C_AP_DATA_N<0> 7 26
E349	MIPI_100D	MIPI	MIPI1C_AP_CLK_P 7 26
E350	MIPI_100D	MIPI	MIPI1C_AP_CLK_N 7 26
E351	MIPI_100D	MIPI	MIPI1C_CAM_DATA_P<0> 25 26
E352	MIPI_100D	MIPI	MIPI1C_CAM_DATA_N<0> 25 26
E353	MIPI_100D	MIPI	MIPI1C_CAM_CLK_P 25 26
E354	MIPI_100D	MIPI	MIPI1C_CAM_CLK_N 25 26

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E249	DP_100D	DP	DP_AP_TX_P<0> 7 10 13
E249	DP_100D	DP	DP_AP_TX_N<0> 7 10 13
E248	DP_100D	DP	DP_AP_TX_P<1> 7 10 13
E250	DP_100D	DP	DP_AP_TX_N<1> 7 10 13
E251	DP_100D	DP	DP_AP_AUX_P 7 13
E252	DP_100D	DP	DP_AP_AUX_N 7 13
E273	DP_100D	DP	DP_EMI_TX_P<0> 13 28
E274	DP_100D	DP	DP_EMI_TX_N<0> 13 28
E275	DP_100D	DP	DP_EMI_TX_P<1> 13 28
E276	DP_100D	DP	DP_EMI_TX_N<1> 13 28
E277	DP_100D	DP	DP_EMI_AUX_P 13 28
E272	DP_100D	DP	DP_EMI_AUX_N 13 28
E327	DP_100D	DP	DP_PT_DK_CON_TX_P<0> 28 29
E326	DP_100D	DP	DP_PT_DK_CON_TX_N<0> 28 29
E328	DP_100D	DP	DP_PT_DK_CON_TX_P<1> 28 29
E329	DP_100D	DP	DP_PT_DK_CON_TX_N<1> 28 29
E330	DP_100D	DP	DP_PT_DK_CON_AUX_P 28 29
E332	DP_100D	DP	DP_PT_DK_CON_AUX_N 28 29

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E189	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
E188	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
E186	AUDIO	AUDIO	LEFT_CH_P 20
E187	AUDIO	AUDIO	SSM2375_L_IN_P 20
E185	AUDIO	AUDIO	SSM2375_L_IN_N 20
E224	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
E192	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
E191	AUDIO	AUDIO	RIGHT_CH_P 20
E190	AUDIO	AUDIO	SSM2375_R_IN_P 20
E193	AUDIO	AUDIO	SSM2375_R_IN_N 20
E172	AUDIO	AUDIO	EXT_MIC_P 19 23
E173	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E209	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
E208	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R
E210	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
E206	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E166	SPI_50S	SPI	SPI_GRAPE_MISO 5 17
E164	SPI_50S	SPI	SPI_GRAPE_MOSI 5 17
E163	SPI_50S	SPI	SPI_GRAPE_SCLK 5 17
E162	SPI_50S	SPI	SPI_GRAPE_CS_L 5 17
E165	SPI_50S	SPI	SPI_IPC_MISO 5 31
E168	SPI_50S	SPI	SPI_IPC_MOSI 5 31
E169	SPI_50S	SPI	SPI_IPC_SCLK 5 31
E167	SPI_50S	SPI	SPI_IPC_MRDY 5 31

SYNC_MASTER=MIKE SYNC_DATE=N/A

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2,ISL3,ISL8,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2,ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES
100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL3,ISL8,ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

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