1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D8 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0001607307	ENGINEERING RELEASED	2012-08-28

LAST_MODIFIED=Mon Aug 27 13:24:34 2012

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Mon Aug 27 13:24:34 2012

DRAWING TITLE: SCH,D8,MLB

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D
REVISION: 7.0.0
BRANCH: prefsb
PAGE: 1 OF 143
SHEET: 1 OF 117

System Block diagram can be found on Kismet

PATH: Kismet > K70/72 > Block Diagrams > K70 Block Diagram

PAGE TITLE
System Block Diagram

Apple Inc.

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Supply Module
AC/DC
Reg G3H 12V
PP12V_ACDC
VD2R
ID2R
PD2R
PP12V_G3H
PP12V_S0_BLC
PP12V_S0
PP12V_S5

U7801
Regulator
Vin
en G3H
Reg G3H 3V42
PP3V42_G3H
SMC, RTC, MojoMux

U7600
Regulator
Vin
en S5
LDO S5 5V
PP5V_S5
PCH, PwrCtl
Reg S5 3.3V
PP3V3_S5
Bootrom, PCH, SMC, XDP,
SD Card, USB Mux, VRD, PwrCtl
PP3V3_S4
ALS, CAM, BT
USB Hub, SMC, TBT I/O
V3V3
IW0R
PW0R
PP3V3_S4_AP
WIFI
PP3V3_S4_ENET
Ethernet
PP3V3_S0
Audio, LCD TCON, SnsCtl, VRD, PCH
SD Card, DP Mux, DP X-bar
V3V3
IW1R
PH1R
PP3V3_S0_SSD
SSD
PP3V3_TBTLC
TBT Router
en S4
Reg S4 5V
PP5V_S4
CAM, USB Ports, VRegCtl
VH05
IH05
PH05
PP5V_S0_HDD
HDD (5V)
PP5V_S0
Audio, PCH
VRegCtl, SnsCtl

U7700
Regulator
Vin
en S3
Reg S3 VDDQ
VM0R
IM0R
PM0R
PPVDDQ_S3_DDR
DIMM (1V5)
PP1V5_S0
Audio
VC0M
IC0M
PC0M
PP1V5_S0_CPU_MEM
CPU (Mem)
LDO S3 VTT
PPDDRVTT_S3
DIMM VREF Margining CA
en S0
LDO S0 VTT
PPDDRVTT_S0
DIMM (VTT)

PPHV_SW_TBTAPWR
TBT Port A
PPHV_SW_TBTBPWR
TBT Port B

U7100
Regulator
Vin
en S0
Reg S0 Core
Reg S0 AXG
VC0C
IC0C
PC0C
PPVCORE_S0_CPU
CPU (Core)
VC0G
IC0G
PC0G
PPVAXG_S0
CPU (AXG)

U7400
Regulator
Vin
en S0
Reg S0 VccIO
VD2R
IC0I
PC0I
PP1V05_S0_CPU
CPU (VccIO)

U7500
Regulator
Vin
en S0
Reg S0 VccSA
VD2R
IC0S
PC0S
PPVCCSA_S0
CPU

UB400
Regulator
Vin
en S0
Reg S0 GPU
VG0C
IG0C
PG0C
PPVCORE_S0_GPU
GPU (Core)

UB750
Regulator
Vin
en S0
Reg S0 GPU
FBVDDQ
VD2R
IG0F
PG0F
PPFBVDDQ_S0_GPU
GPU (FB)

UB700
Regulator
Vin
en S0
Reg S0 1V05
VD2R
IR1R
PR1R
P1V05_S0
GPU (IOVDD, PLLVDD)
VN1R
IN1R
PN1R
P1V05_S0_PCH
PCH (VCC, VccIO)
PP1V05_TBTCIO
TBT Router
PP1V05_TBTLC
TBT Router

Loads
Fan
LCD
GPU
Speaker amps
TBT IO

VD2R
IH02
PH02
PP12V_S0_HDD
HDD (12V)

U7750
Regulator
Vin
en S0
Reg S0 1.8V
PP5V_S0
PP1V8_S0_REG
CPU PLL

High-side Component Total Power Keys

PCTR = 1.176 * (PC0C + PC0G + PC0M) + PC0S + PC0I
PGTR = 1.176 * PG0C + PG0F + 5.7 (GK104/GK107_BLENDED_CONSTANT)
PH0R = PH02 + PH05

SYNC_MASTER=D8_MARK SYNC_DATE=04/23/2012
PAGE TITLE
Power Block Diagram
Apple Inc.
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SIZE D
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3816	PCBA,MLB,2.9G,4C,GK107,SAM,D8	D8_COMMON,D8,CPU:4C_2P9GHZ,GPU:107EGE,FB:BOTH_SAMSUNG,EEEE:F2FR
639-3952	PCBA,MLB,3.1G,4C,GK107,SAM,D8	D8_COMMON,D8,CPU:4C_3P1GHZ,GPU:107EGE,FB:BOTH_SAMSUNG,EEEE:F49T
639-4092	PCBA,MLB,2.9G,4C,GK107,HYN.D8	D8_COMMON,D8,CPU:4C_2P9GHZ,GPU:107EGE,FB:BOTH_HYNIX,EEEE:F653
639-4093	PCBA,MLB,3.1G,4C,GK107,HYN.D8	D8_COMMON,D8,CPU:4C_3P1GHZ,GPU:107EGE,FB:BOTH_HYNIX,EEEE:F654
085-4433	PCBA,MLB,DEV,D8	DEVELOPMENT,D8_DEVEL

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_DHNM	CRITICAL	EEEE:DHNM
825-7896	1	LABEL,MLB,2D	EEEE_F2FR	CRITICAL	EEEE:F2FR
825-7896	1	LABEL,MLB,2D	EEEE_F49V	CRITICAL	EEEE:F49V
825-7896	1	LABEL,MLB,2D	EEEE_F49T	CRITICAL	EEEE:F49T
825-7896	1	LABEL,MLB,2D	EEEE_F653	CRITICAL	EEEE:F653
825-7896	1	LABEL,MLB,2D	EEEE_F654	CRITICAL	EEEE:F654

BOM Groups

BOM GROUP	BOM OPTIONS
D8_COMMON	COMMON,ALTERNATE,D8_COMMON1,D8_PROGPARTS,D8_PRODUCTION
D8_COMMON1	XDP,RSMRST:GATE,SPEAKERID,VREF:CPU,TBTHV:P12V,FBA,FBB
D8_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG,BLCMCU:PROG
D8_DEVEL	XDP_CONN,LPCPLUS,VREFMRGN:EXT,DEVEL_AUDIO,TEMPSNSDEV
D8_PRODUCTION	VREFMRGN:N,PRODUCTION

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4355	1	IVB,SR0TA,PRQ,N1,2.9,65W,4+1,1.1,6M,LGA	CPU	CRITICAL	CPU:4C_2P9GHZ
337S4372	1	IVB,SR0T9,PRQ,N0,3.1,65W,4+1,1.1,6M,LGA	CPU	CRITICAL	CPU:4C_3P1GHZ

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4277	1	IC,PANTHER POINT,C1,SLJC7,PRQ,BD82Z77	U1800	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B1,PRQ,288 FCBGA,12X12MM	U3600	CRITICAL	
337S4280	1	IC, GPU, NV GK107-GE-PS-A2	U8000	CRITICAL	GPU:107EGE
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
341S3672	1	IC,EEPROM,CR,V14.1 (B1),D8	U3690	CRITICAL	TBTROM:PROG	
335S0865	1	IC,EEPROM,SERIAL,8KB,MLP8	U3690	CRITICAL	TBTROM:BLANK	
341S3673	1	IC,PROGRMD,EFI ROM,V00FC,D7/D8	U5110	CRITICAL	BOOTROM:PROG	ALTERNATE:335S0812
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5110	CRITICAL	BOOTROM:BLANK	
341S3394	1	IC,PROGRMD,SMC,A3,V2.2A32,D8	U4900	CRITICAL	SMC:PROG	
338S1098	1	IC,SMC,LX4FS1AH5BBCIGA3	U4900	CRITICAL	SMC:BLANK	
341S3675	1	IC,CAMERA FLASH,V7228,D7/D8	U4202	CRITICAL	CAMROM:PROG	
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK	
341S3645	1	IC,ENET 1MBIT, SPI,ROM, V1.13 D8	U3990	CRITICAL	CIVROM:PROG	ALTERNATE:335S0854
335S0862	1	IC,SERIAL FLASH,2MBIT, 2.7V, REF F	U3990	CRITICAL	CIVROM:BLANK	
341S3674	1	IC,BLC,MCU, PRPOGRAMMED, V0204, D8	U9700	CRITICAL	BLCMCU:PROG	
337S3978	1	IC,BLC MCU LPC2132FBD64/01, LQFP64	U9700	CRITICAL	BLCMCU:BLANK	

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0073	1	SOCKET,MOLEX,LGA1155,CPU-LF	U1000	CRITICAL	

CPU SOCKET ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0071	511S0073		ALL	TYCO SOCKET
511S0072	511S0073		ALL	FOXCONN SOCKET

D8 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9504	1	SCH,MLB,D8	SCH1	CRITICAL	D8
820-3298	1	PCBF,MLB,D8	PCB1	CRITICAL	D8

D8 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB diodes
157S0084	157S0058		ALL	Enet Magnetics
341S3644	341S3645		U3990	CIVROM
376S0975	376S1081		ALL	P/NCH DUAL FET
128S0365	128S0368		ALL	150UF CAPS BLK
138S0803	138S0804		ALL	2.2UF CAPS SOFT
102S0880	102S0879		ALL	0.010 OHM,1%,1206

VRAM MODULE PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0619	4	IC,SGRAM,GDDR5,32MX32,1.5GHz,G-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_SAMSUNG
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_HYNIX

SYNC_MASTER=D8_MLB SYNC_DATE=12/19/2011

PAGE TITLE

BOM Configuration

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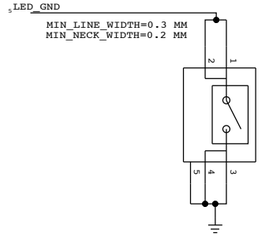
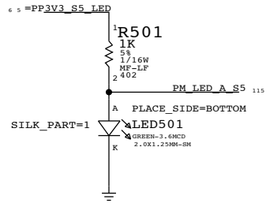
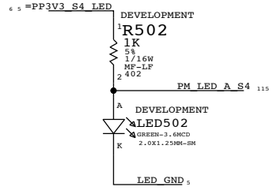
LED GND ISOLATION SWITCH



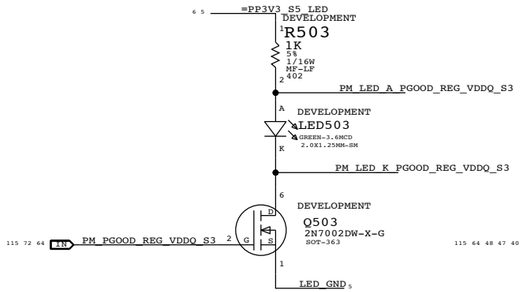
S5 LED



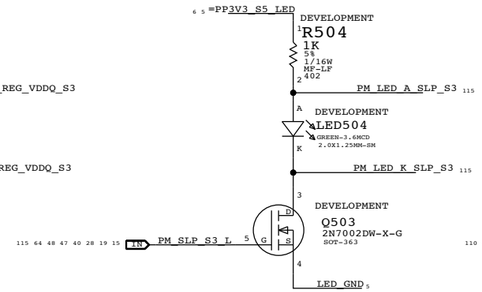
S4 (SLEEP) LED



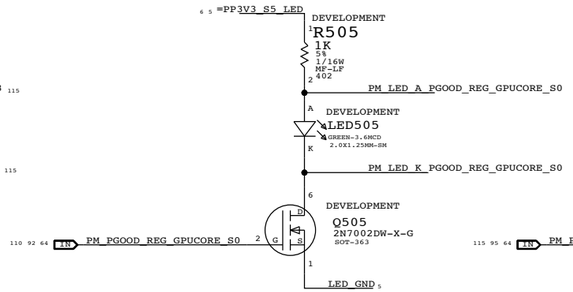
MEM 1V5_S3 LED



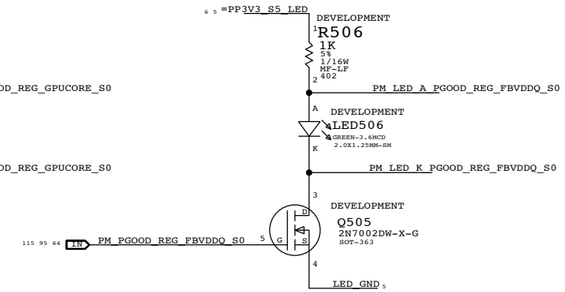
SLP_S3 LED



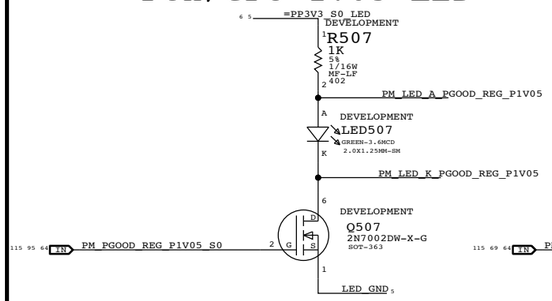
GPU VCORE LED



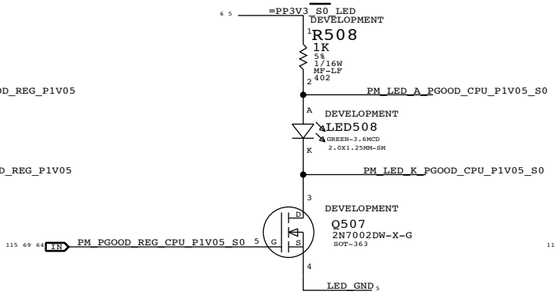
GPU FBVDD LED



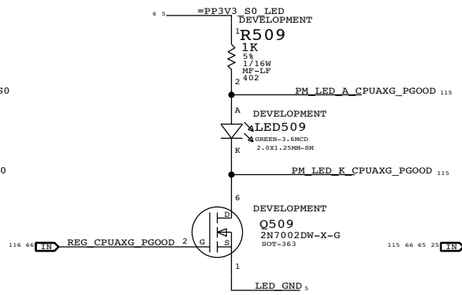
PCH/GPU 1V05 LED



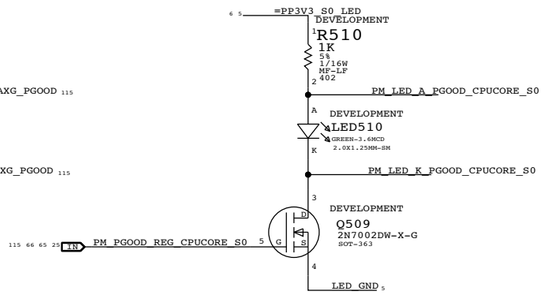
CPU 1V05_S0 LED



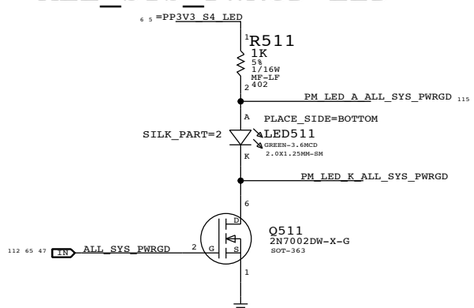
CPU AXG LED



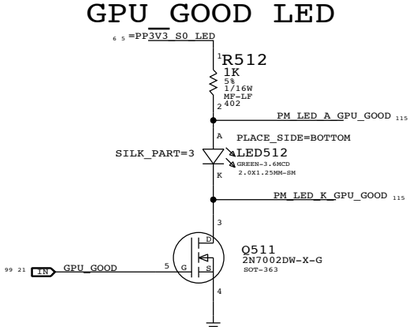
CPU VCORE LED



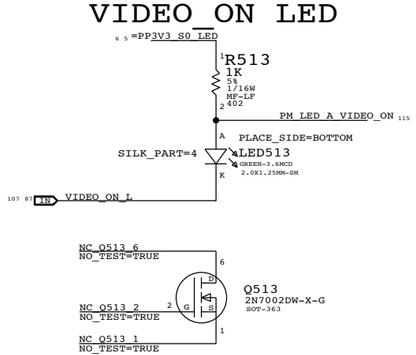
ALL_SYS_PWRGD LED



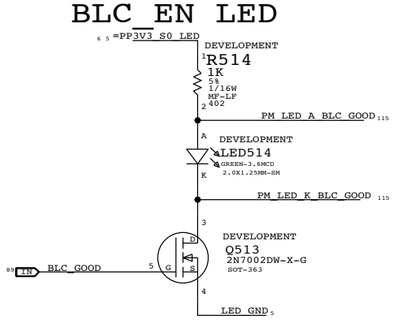
GPU_GOOD LED



VIDEO_ON LED



BLC_EN LED



SYNC_MASTER=D8_TAVYS SYNC_DATE=06/22/2012

PAGE TITLE
DEBUG LEDS

Apple Inc.

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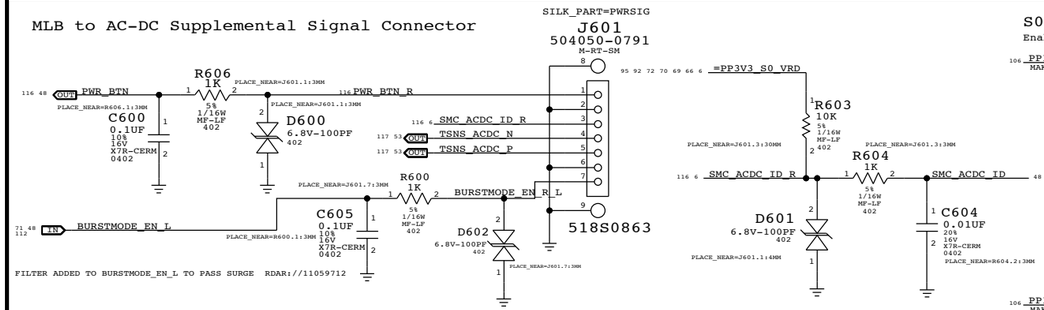
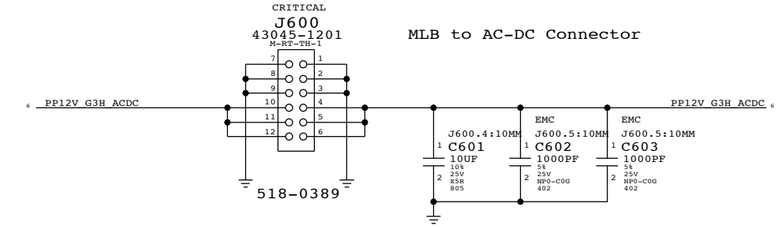
MLB to AC-DC Supplemental Signal Connector



MLB to AC-DC Connector



G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)	=PP3V3_G3_PCH_RTC	22
	=PP3V3_G3_PCH	18 19

G3H Rails

On with AC/DC plugged in

PP12V_ACDC (MAKE_BASE=TRUE)	=PP12V_G3H_ACDC	6
	=PP12V_G3H_PWR	51
PP12V_G3H (MAKE_BASE=TRUE)	=PP12V_G3H_SNS	51
	=PP12V_G3H_P3V42	73
	=PP12V_G3H_FET_P12V_S0	74
	=PP12V_G3H_FET_P12V_S5	74
PP3V42_G3H (MAKE_BASE=TRUE)	=PP3V42_G3H_REG	73
	=PP3V3_G3H_BT	35
	=PP3V3_G3H_RTC_D	26
	=PP3V3_G3H_SMC	47 48 50
	=PP3V3_G3H_SMC_USBMUX	45
	=PPVIN_G3H_SMCVREF	48
	=PP3V3_G3H_LPCPLUS	49

S5 Rails

On when in S5

PP12V_S5 (MAKE_BASE=TRUE)	=PP12V_S5_FET	74
	=PP12V_S5_REG_P3V3P5V_S5	71
	=PP12V_S5_REG_VDDQ_S3	72
	=PP12V_S5_PWRCTL	64 65 74
	=PPHV_SW_TBTAPWRSW	86
	=PPHV_SW_TBTBPWRSW	88
	=PP12V_S5_SNS	51
PP5V_S5 (MAKE_BASE=TRUE)	=PP5V_S5_LDO	71
	=PP5V_S5_PWRCTL	71
	=PP5V_S5_PCH	24
PP3V3_S5 (MAKE_BASE=TRUE)	=PP3V3_S5_REG	71
	=PP3V3_S5_FET_P3V3_S0	74
	=PP3V3_S5_FET_P3V3_S4	74
	=PP3V3_S5_SMC	48
	=PP3V3_S5_LED	5
	=PP3V3_S5_PCH	19 24 26
	=PP3V3_S5_PCH_STRAPS	15
	=PP3V3_S5_PCH_VCCSUS_HDA	22 24
	=PP3V3_S5_PCH_VCCSUS_USB	22 24
	=PP3V3_S5_PCH_VCC_DSW	22 24
	=PP3V3_S5_PCH_VCC_SPI	22 24
	=PP3V3_S5_PWRCTL	64 65
	=PP3V3_S5_ROM	49
	=PP3V3_S5_VRD	71
	=PP3V3_S5_XDP	25
	=PP3V3_S5_SMC_USBMUX	45 46
	=PP3V3_S5_SENSE	51
	=PP3V3_S5_SDCARD	41

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (MAKE_BASE=TRUE)	=PP5V_S4_REG	71
	=PP5V_S4_REG_VDDQ_S3	72
	=PP5V_S4_FET_P5V_S0	74
	=PP5V_S4_MEMRESET	28
	=PP5V_S4_USB	45 46
	=PP5V_S4_CAMERA	42
PP3V3_S4 (MAKE_BASE=TRUE)	=PP3V3_S4_FET	74
	=PP3V3_S4_ALS	42
	=PP3V3_S4_AP_PWR	55
	=PP3V3_S4_CAMERA	42 43
	=PP3V3_S4_ENET	40
	=PP3V3_S4_LED	5
	=PP3V3_S4_MEMRESET	28
	=PP3V3_S4_PM	28
	=PP3V3_S4_PWRCTL	65 72 74
	=PP3V3_S4_SENSE	51
	=PP3V3_S4_SMBUS	50
	=PP3V3_S4_SMBUS_SMC	50
	=PP3V3_S4_SMC	48
	=PP3V3_S4_TBT	36 37 38 86 88
	=PP3V3_S4_TBTAPWRSW	48 86
	=PP3V3_S4_TBTBPWRSW	48 88
	=PP3V3_S4_USB_HUB	27
	=PP3V3_S4_VREFMRGN	34
	=PP3V3_S4_AUDIO_DIG	60
PP3V3_S4_AP (MAKE_BASE=TRUE)	=PP3V3_S4_AP_SNS	55
	=PP3V3_S4_AP	15 35
PP3V3_S4_ENET (MAKE_BASE=TRUE)	=PP3V3_S4_ENET_FET	40
	=PP3V3_S4_ENET_FET	39 40
	=PP3V3_S4_ENET_SYSCLK	26
	=PP3V3_S4_ENET_CLK	26

S3 Rails

Enabled when system is in run or sleep

PPVDDQ_S3 (MAKE_BASE=TRUE)	=PPVDDQ_S3_REG	72
	=PPVDDQ_S3_DDR_PWR	51
	=PPVDDQ_S3_FET_VDDQ_S0	74
	=PPVDDQ_S3_LDO_DDRVTT	72
THIS IS 1.5V RAIL		
PPVDDQ_S3_DDR (MAKE_BASE=TRUE)	=PPVDDQ_S3_DDR_SNS	51
	=PPVDDQ_S3_DDR_VREF	34
	=PPVDDQ_S3_MEM_A	29 30
	=PPVDDQ_S3_MEM_B	31 32
	=PPVDDQ_S3_MEMRESET	28
THIS IS 1.5V RAIL		
PPDDRVTT_S3 (MAKE_BASE=TRUE)	=PPDDRVTT_S3_LDO	72
	=PPDDRVTT_S3_VREFCA	34
THIS IS 1.5V RAIL		

S0 Rails

Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)	=PP12V_S0_FET	74
	=PP12V_S0_AUDIO_SPKRAMP	58 59
	=PP12V_S0_FAN	54
	=PP12V_S0_FBVDDQ_PWR	51
	=PP12V_S0_REG_GPUCORE	92
	=PP12V_S0_HDD_PWR	51
	=PP12V_S0_LCD	87
	=PP12V_S0_REG_CPUCORE	67
	=PP12V_S0_REG_CPU_P1V05_PWR	55
	=PP12V_S0_REG_CPU_VCCSA_PWR	55
	=PP12V_S0_REG_P1V05_PWR	55
	=PP12V_S0_PWRCTL	65
PP12V_S0_HDD (MAKE_BASE=TRUE)	=PP12V_S0_HDD_SNS	51
	=PP12V_S0_HDD	52
PP12V_S0_BLC (MAKE_BASE=TRUE)	=PP12V_S0_BLC_FET	74
	=PP12V_S0_BLC	91
PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)	=PP12V_S0_FBVDDQ_SNS	51
	=PP12V_S0_REG_FBVDDQ	95
PP12V_S0_CPU_P1V05 (MAKE_BASE=TRUE)	=PP12V_S0_REG_CPU_P1V05_SNS	55
	=PP12V_S0_REG_CPU_P1V05	69
PP12V_S0_VCCSA (MAKE_BASE=TRUE)	=PP12V_S0_REG_CPU_VCCSA_SNS	55
	=PP12V_S0_REG_VCCSA	70
PP12V_S0_P1V05 (MAKE_BASE=TRUE)	=PP12V_S0_REG_P1V05_SNS	55
	=PP12V_S0_REG_P1V05	95
PP5V_S0 (MAKE_BASE=TRUE)	=PP5V_S0_FET	74
	=PP5V_S0_AUDIO	56 63
	=PP5V_S0_BLC	91
	=PP5V_S0_HDD_PWR	51
	=PP5V_S0_ISENSE	51
	=PP5V_S0_LPCPLUS	49
	=PP5V_S0_PCH	24
	=PP5V_S0_REG_CPUCORE	66
	=PP5V_S0_REG_CPU_P1V05	69
	=PP5V_S0_REG_FBVDDQ	95
	=PP5V_S0_REG_P1V05	95
	=PP5V_S0_REG_P1V8	72
	=PP5V_S0_REG_VCCSA	70
	=PP5V_S0_VRD	72 92
PP5V_S0_HDD (MAKE_BASE=TRUE)	=PP5V_S0_HDD_SNS	51
	=PP5V_S0_HDD	52
PP3V3_S0 (MAKE_BASE=TRUE)	=PP3V3_S0_FET	74
	=PP3V3_S0_GPU_IFPX_PLLVDD	78
	=PP3V3_S0_GPU_MISC	78
	=PP3V3_S0_GPU_VDD33	78
	=PP3V3_S0_AUDIO	42 56 58 59 62
	=PP3V3_S0_AUDIO_DIG	60
	=PP3V3_S0_BLC	89
	=PP3V3_S0_DP	85 87
	=PP3V3_S0_ENET	39
	=PP3V3_S0_FAN	54
	=PP3V3_S0_GPU	78 92
	=PP3V3_S0_INTDPMUX	84
	=PP3V3_S0_LED	5
	=PP3V3_S0_LED_SATA	15 44
	=PP3V3_S0_MEM_A_SPD	29 30
	=PP3V3_S0_MEM_B_SPD	31 32
	=PP3V3_S0_P3V3TBTFET	38
	=PP3V3_S0_PCH	18 21 24
	=PP3V3_S0_PCH_GPIO	15 19 20 38
	=PP3V3_S0_PCH_PM	26
	=PP3V3_S0_PCH_STRAPS	15
	=PP3V3_S0_PCH_VCC	22 24
	=PP3V3_S0_PCH_VCC_ADAC	17
	=PP3V3_S0_PCH_VCC_GPIO	22 24
	=PP3V3_S0_PCH_VCC_HVCMOS	22 24
	=PP3V3_S0_PCH_VCC_PCI	22 24
	=PP3V3_S0_PWRCTL	28 74
	=PP3V3_S0_RSTBUF	26
	=PP3V3_S0_SDCARD	41
	=PP3V3_S0_SENSE	51 52 53 55
	=PP3V3_S0_SMBUS	50
	=PP3V3_S0_SMBUS_SMC	50
	=PP3V3_S0_SMBUS_TCON	50
	=PP3V3_S0_SMC	48 51 82
	=PP3V3_S0_TBTPWRCTL	38
	=PP3V3_S0_VRD	6 66 69 70 72 92 95
	=PP3V3_S0_SSD_PWR	51
PP3V3_S0_SSD (MAKE_BASE=TRUE)	=PP3V3_S0_SSD_SNS	51
	=PP3V3_S0_SSD	44

PP1V8_S0 (MAKE_BASE=TRUE)	=PP1V8_S0_REG	72
	=PP1V8_S0_CPU_PLL	13 16
	=PP1V8_S0_PCH	19
	=PP1V8_S0_PCH_VCC_DFTERM	22 24
	=PP1V8_S0_PCH_VCC_VRM	24
	=PP1V8_S0_PCH_CLK	26
PP1V5_S0 (MAKE_BASE=TRUE)	=PP1V5_S0_FET	74
	=PP1V5_S0_AUD_DIG	56
	=PP1V5_S0_CPU_MEM_PWR	51
	=PP1V5_S0_DP	84
PP1V5_S0_CPU_MEM (MAKE_BASE=TRUE)	=PP1V5_S0_CPU_MEM_SNS	51
	=PP1V5_S0_CPU_MEM	11 13 16
PPDDRVTT_S0 (MAKE_BASE=TRUE)	=PPDDRVTT_S0_LDO	72
	=PPDDRVTT_S0_CLAMP	28
	=PPDDRVTT_S0_MEM_A	29 30
	=PPDDRVTT_S0_MEM_B	31 32
PPDDRVREF_DQ_MEM_A_S3 (MAKE_BASE=TRUE)	=PPDDRVREF_DQ_MEM_A	34
	=PPDDRVREF_DQ_MEM_A	29 30
PPDDRVREF_CA_MEM_A_S3 (MAKE_BASE=TRUE)	=PPDDRVREF_CA_MEM_A	34
	=PPDDRVREF_CA_MEM_A	29 30
PPDDRVREF_DQ_MEM_B_S3 (MAKE_BASE=TRUE)	=PPDDRVREF_DQ_MEM_B	34
	=PPDDRVREF_DQ_MEM_B	31 32
PPDDRVREF_CA_MEM_B_S3 (MAKE_BASE=TRUE)	=PPDDRVREF_CA_MEM_B	34
	=PPDDRVREF_CA_MEM_B	31 32
PP1V05_S0_CPU (MAKE_BASE=TRUE)	=PP1V05_S0_CPU_REG	69
	=PPVCCIO_S0_CPU	10 11 13 16 28 66
	=PPVCCIO_S0_SMC	48
	=PPVCCIO_S0_XDP	25
PP1V05_S0 (MAKE_BASE=TRUE)	=PP1V05_S0_REG	95
	=PP1V05_S0_PCH_PWR	51
	=PP1V05_S0_P1V05TBTFET	38
	=PP1V05_S0_GPU_IFPCD_IOVDD	78
	=PP1V05_S0_GPU_IFPEF_IOVDD	78
	=PP1V05_S0_GPU_PEX_PLLVDD	78
	=PP1V05_S0_GPU_PEX_IOVDD	78
PPVCORE_S0_CPU (MAKE_BASE=TRUE)	=PPCPUCORE_S0_REG	67 68
	=PPVCORE_S0_CPU	13 16 51 66
PPVAXG_S0 (MAKE_BASE=TRUE)	=PPCPUAXG_S0_REG	17 68
	=PPVAXG_S0_CPU	13 17 51 66
PPVCCSA_S0 (MAKE_BASE=TRUE)	=PPVCCSA_S0_REG	70
	=PPVCCSA_S0_CPU	13 16

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

PP3V3_TBTLC (MAKE_BASE=TRUE)	=PP3V3_TBTLC_FET	38
	=PP3V3_TBT_PCH_GPIO	15
	=PP3V3_TBTLC_RTR	15 36 37 38 50
	=PP3V3_TBT_CLK	26
PP1V05_TBTLC (MAKE_BASE=TRUE)	=PP1V05_TBTLC_FET	38
	=PP1V05_TBTLC_RTR	37
PP1V05_TBTCIO (MAKE_BASE=TRUE)	=PP1V05_TBTCIO_FET	38
	=PP1V05_TBTCIO_RTR	37

Ground/Common

GND (MAKE_BASE=TRUE)

GPU Rails (S0)

Enabled when system is in run

PPVCORE_S0_GPU (MAKE_BASE=TRUE)	=PPGPUCORE_S0_REG	93 94
	=PPVCORE_S0_GPU	51 78
PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)	=PP1V5R1V35_S0_GPU_REG	95 110
	=PP1V35_S0_GPU_FBVDDQ	78

PP1V05_S0_PCH (MAKE_BASE=TRUE)	=PP1V05_S0_PCH_SNS	51
	=PP1V05_S0_PCH	18
	=PP1V05_S0_PCH_VCCCLKDMI	22 24
	=PP1V05_S0_PCH_VCCIO_DMI	22 24
	=PP1V05_S0_PCH_VCCIO_PCIE	18 19 22 24
	=PP1V05_S0_PCH_VCCIO_SATA	18 22 24
	=PP1V05_S0_PCH_VCCIO_USB	22 24
	=PP1V05_S0_PCH_VCC_ADPLL	17
	=PP1V05_S0_PCH_VCC_ASW	22 24
	=PP1V05_S0_PCH_VCC_CORE	22 24
	=PP1V05_S0_PCH_VCC_DIFFCLK	22 24
	=PP1V05_S0_PCH_VCC_DMI	22 24
	=PP1V05_S0_PCH_VCC_SSC	22 24
	=PP1V05_S0_PCH_V_PROC_IO	22 24

SYNC_MASTER=D8_DOUG	SYNC_DATE=06/20/2012
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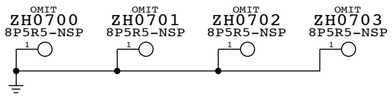
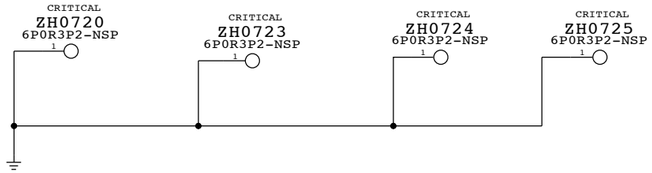
CPU Heatsink

4MM PLATED HOLES (998-4158)



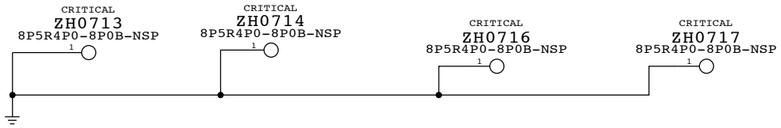
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



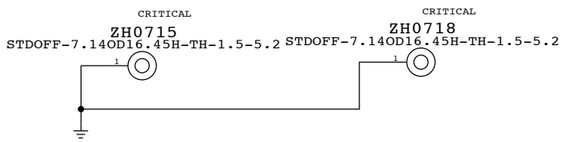
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



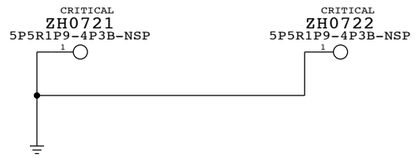
Rear Cover

860-1487 (PCB STANDOFF)



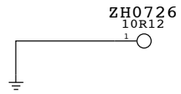
WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)



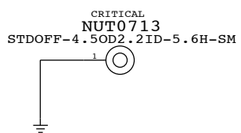
HEATPIPE MTG HOLES

998-4640 (PLATED HOLES, 10MM DIA, 12MM PAD)



SSD STANDOFF

APN: 860-1461



SYNC MASTER=D8_MLB SYNC DATE=03/25/2012

PAGE TITLE: Holes/PD parts

Apple Inc.

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CPU Reserved

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>
10	CPU_CFG<15..12>	TP_CPU_CFG<15..12>

MAKE_BASE=TRUE NO_TEST=TRUE

CPU Memory

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSNX<8>
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSPX<8>
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSNX<8>
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSPX<8>

MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCIe

18	TP_PCIE1_D2RN	NC_PCIE1_D2RNX
18	TP_PCIE1_D2RP	NC_PCIE1_D2RPX
18	TP_PCIE1_R2D_CN	NC_PCIE1_R2D_CNX
18	TP_PCIE1_R2D_CP	NC_PCIE1_R2D_CPX
18	TP_PCIE2_D2RN	NC_PCIE2_D2RNX
18	TP_PCIE2_D2RP	NC_PCIE2_D2RPX
18	TP_PCIE2_R2D_CN	NC_PCIE2_R2D_CNX
18	TP_PCIE2_R2D_CP	NC_PCIE2_R2D_PNX

MAKE_BASE=TRUE NO_TEST=TRUE

18	DMI_MIDBUS_CLK100M_N	NC_DMI_MIDBUS_CLK100NX
18	DMI_MIDBUS_CLK100M_P	NC_DMI_MIDBUS_CLK100PX

MAKE_BASE=TRUE NO_TEST=TRUE

18	TP_PCIE_CLK100M_PE0N	NC_PCIE_CLK100M_PE0NX
18	TP_PCIE_CLK100M_PE0P	NC_PCIE_CLK100M_PE0PX
18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4NX
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4PX
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5NX
18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5PX
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6NX
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6PX
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7NX
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7PX

MAKE_BASE=TRUE NO_TEST=TRUE

10	TP_PE_TX_N<3..0>	NC_PE_TNX<3..0>
10	TP_PE_TX_P<3..0>	NC_PE_TPX<3..0>
10	TP_PE_RX_N<3..0>	NC_PE_RNX<3..0>
10	TP_PE_RX_P<3..0>	NC_PE_RPX<3..0>

MAKE_BASE=TRUE NO_TEST=TRUE

PCH USB

20	USB_PCH_4_N	NC_USB_PCH_4NX
20	USB_PCH_4_P	NC_USB_PCH_4PX
20	USB_PCH_5_N	NC_USB_PCH_5NX
20	USB_PCH_5_P	NC_USB_PCH_5PX
20	USB_PCH_6_N	NC_USB_PCH_6NX
20	USB_PCH_6_P	NC_USB_PCH_6PX
20	USB_PCH_11_N	NC_USB_PCH_11NX
20	USB_PCH_11_P	NC_USB_PCH_11PX
20	USB_PCH_12_N	NC_USB_PCH_12NX
20	USB_PCH_12_P	NC_USB_PCH_12PX
20	USB_PCH_13_N	NC_USB_PCH_13NX
20	USB_PCH_13_P	NC_USB_PCH_13PX

MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPNX
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPPX
18	PCH_CLK25M_XTALOUT	NC_PCH_CLK25M_XTALOUT
18	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0
18	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1
18	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2
18	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3

MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

19	TP_CRT_IG_RED	NC_CRT_IG_RED
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC
19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

19	DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLNX<3..0>
19	DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLPX<3..0>
19	DP_IG_B_AUX_N	NC_DP_IG_B_AUXNX
19	DP_IG_B_AUX_P	NC_DP_IG_B_AUXPX
19	DP_IG_B_HPD	NC_DP_IG_B_HPD
19	DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK
19	DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

19	DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLNX<3..0>
19	DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLPX<3..0>
19	DP_IG_C_AUX_N	NC_DP_IG_C_AUXNX
19	DP_IG_C_AUX_P	NC_DP_IG_C_AUXPX
19	DP_IG_C_HPD	NC_DP_IG_C_HPD
19	DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK
19	DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

19	DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLNX<3..0>
19	DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLPX<3..0>
19	DP_IG_D_AUXN	NC_DP_IG_D_AUXNX
19	DP_IG_D_AUXP	NC_DP_IG_D_AUXPX
19	DP_IG_D_HPD	NC_DP_IG_D_HPD
19	DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK
19	DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINNX
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINPX
19	TP_SDVO_STALLN	NC_SDVO_STALLNX
19	TP_SDVO_STALLP	NC_SDVO_STALLPX
19	TP_SDVO_INTN	NC_SDVO_INTNX
19	TP_SDVO_INTP	NC_SDVO_INTPX

MAKE_BASE=TRUE NO_TEST=TRUE

18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN

MAKE_BASE=TRUE NO_TEST=TRUE

PCH SATA

18	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CNX
18	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CPX
18	TP_SATA_C_D2RN	NC_SATA_C_D2RNX
18	TP_SATA_C_D2RP	NC_SATA_C_D2RPX
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CNX
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CPX
18	TP_SATA_D_D2RN	NC_SATA_D_D2RNX
18	TP_SATA_D_D2RP	NC_SATA_D_D2RPX
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CNX
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CPX
18	TP_SATA_E_D2RN	NC_SATA_E_D2RNX
18	TP_SATA_E_D2RP	NC_SATA_E_D2RPX
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CNX
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CPX
18	TP_SATA_F_D2RN	NC_SATA_F_D2RNX
18	TP_SATA_F_D2RP	NC_SATA_F_D2RPX

MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reserved

19	TP_PCH_RESERVE_0	NC_PCH_RESERVE_0
19	TP_PCH_RESERVE_1	NC_PCH_RESERVE_1
19	TP_PCH_RESERVE_2	NC_PCH_RESERVE_2
19	TP_PCH_RESERVE_3	NC_PCH_RESERVE_3
19	TP_PCH_RESERVE_4	NC_PCH_RESERVE_4
19	TP_PCH_RESERVE_5	NC_PCH_RESERVE_5
19	TP_PCH_RESERVE_6	NC_PCH_RESERVE_6
19	TP_PCH_RESERVE_7	NC_PCH_RESERVE_7
19	TP_PCH_RESERVE_8	NC_PCH_RESERVE_8
19	TP_PCH_RESERVE_9	NC_PCH_RESERVE_9
19	TP_PCH_RESERVE_10	NC_PCH_RESERVE_10
19	TP_PCH_RESERVE_11	NC_PCH_RESERVE_11
19	TP_PCH_RESERVE_12	NC_PCH_RESERVE_12
19	TP_PCH_RESERVE_13	NC_PCH_RESERVE_13
19	TP_PCH_RESERVE_14	NC_PCH_RESERVE_14
19	TP_PCH_RESERVE_15	NC_PCH_RESERVE_15
19	TP_PCH_RESERVE_16	NC_PCH_RESERVE_16
19	TP_PCH_RESERVE_17	NC_PCH_RESERVE_17
19	TP_PCH_RESERVE_18	NC_PCH_RESERVE_18
19	TP_PCH_RESERVE_19	NC_PCH_RESERVE_19
19	TP_PCH_RESERVE_20	NC_PCH_RESERVE_20
19	TP_PCH_RESERVE_21	NC_PCH_RESERVE_21
19	TP_PCH_RESERVE_22	NC_PCH_RESERVE_22
19	TP_PCH_RESERVE_23	NC_PCH_RESERVE_23
19	TP_PCH_RESERVE_24	NC_PCH_RESERVE_24
19	TP_PCH_RESERVE_25	NC_PCH_RESERVE_25
19	TP_PCH_RESERVE_26	NC_PCH_RESERVE_26
19	TP_PCH_RESERVE_27	NC_PCH_RESERVE_27
19	TP_PCH_RESERVE_28	NC_PCH_RESERVE_28

MAKE_BASE=TRUE NO_TEST=TRUE

PCH and CPU FDI

10	TP_CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TNX<7..0>
10	TP_CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TPX<7..0>
19	PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RNX<7..0>
19	PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RPX<7..0>

MAKE_BASE=TRUE NO_TEST=TRUE

10	TP_CPU_FDI_FSYNC<1..0>	NC_CPU_FDI_FSYNC<1..0>
10	TP_CPU_FDI_LSYNC<1..0>	NC_CPU_FDI_LSYNC<1..0>
10	TP_CPU_FDI_INT	NC_CPU_FDI_INT

MAKE_BASE=TRUE NO_TEST=TRUE

19	PCH_FDI_FSYNC<1..0>	NC_PCH_FDI_FSYNC<1..0>
19	PCH_FDI_LSYNC<1..0>	NC_PCH_FDI_LSYNC<1..0>
19	PCH_FDI_INT	NC_PCH_FDI_INT

MAKE_BASE=TRUE NO_TEST=TRUE

PCH Test Points

21	TP_PCH_TP1	NC_PCH_TP1
21	TP_PCH_TP2	NC_PCH_TP2
21	TP_PCH_TP3	NC_PCH_TP3
21	TP_PCH_TP4	NC_PCH_TP4
21	TP_PCH_TP5	NC_PCH_TP5
21	TP_PCH_TP6	NC_PCH_TP6
21	TP_PCH_TP7	NC_PCH_TP7
21	TP_PCH_TP8	NC_PCH_TP8
21	TP_PCH_TP9	NC_PCH_TP9
21	TP_PCH_TP10	NC_PCH_TP10
21	TP_PCH_TP11	NC_PCH_TP11
21	TP_PCH_TP12	NC_PCH_TP12
21	TP_PCH_TP13	NC_PCH_TP13
21	TP_PCH_TP14	NC_PCH_TP14
21	TP_PCH_TP15	NC_PCH_TP15
21	TP_PCH_TP16	NC_PCH_TP16
21	TP_PCH_TP17	NC_PCH_TP17
21	TP_PCH_TP18	NC_PCH_TP18
21	TP_PCH_TP19	NC_PCH_TP19
21	TP_PCH_TP20	NC_PCH_TP20

MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>
20	TP_PCI_PAR	NC_PCI_PAR
20	TP_PCI_RESET_L	NC_PCI_RESET_L
20	TP_PCI_PCI_GNT0_L	NC_PCI_GNT0_L
19	TP_PCH_INIT3V3_L	NC_PCH_INIT3V3_L
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L

MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

18	TP_HDA_SDIN1	NC_HDA_SDIN1
18	TP_HDA_SDIN2	NC_HDA_SDIN2
18	TP_HDA_SDIN3	NC_HDA_SDIN3
21	TP_PCH_PWM0	NC_PCH_PWM0
21	TP_PCH_PWM1	NC_PCH_PWM1
21	TP_PCH_PWM2	NC_PCH_PWM2
21	TP_PCH_PWM3	NC_PCH_PWM3
21	TP_PCH_SST	NC_PCH_SST
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1
20	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2
20	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3

MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=D8 MLB ULTIMATE SYNC_DATE=04/02/2012

PAGE TITLE

Unused Signal Aliases

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

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ALIASES (BLANK)

SYNC MASTER=K70 MLB SYNC DATE=08/23/2011

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

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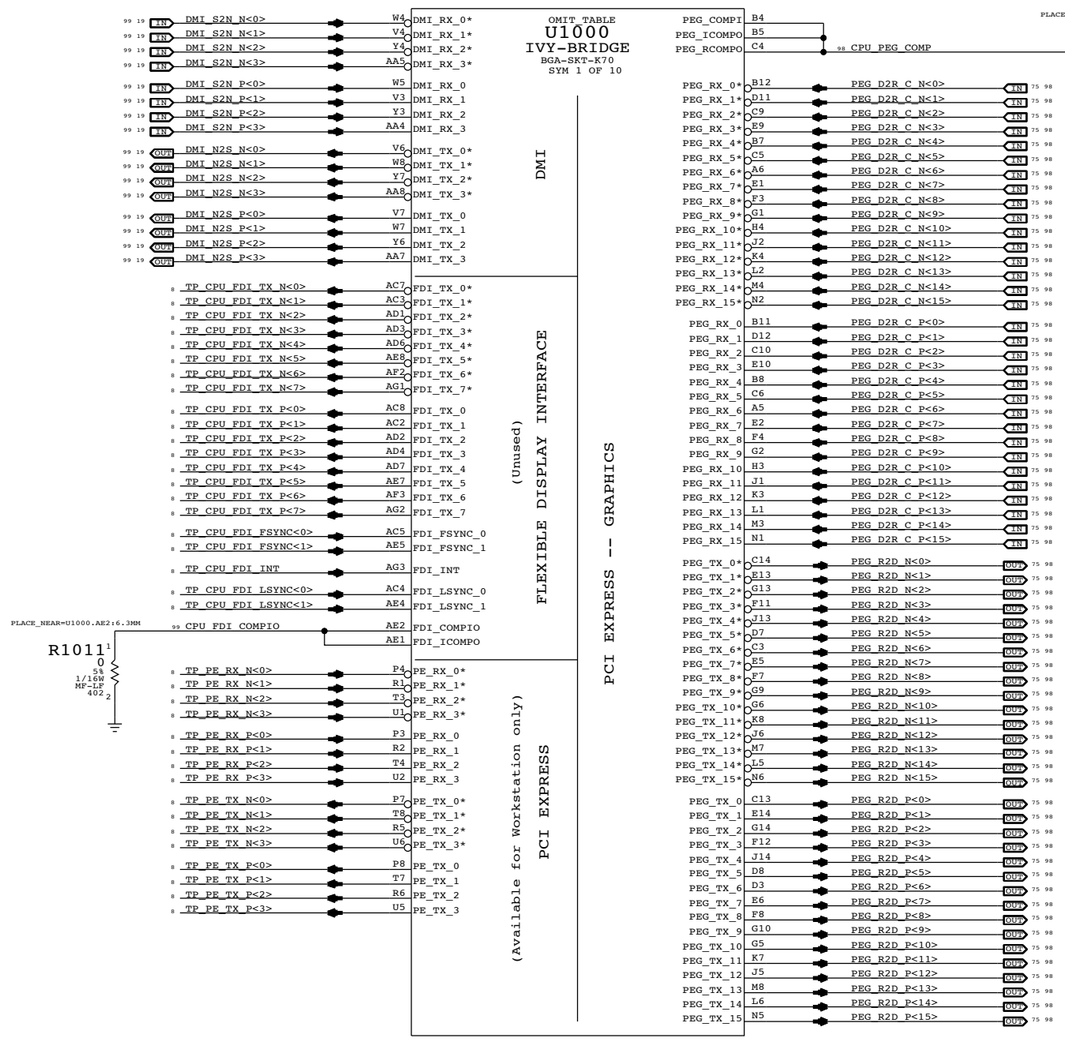

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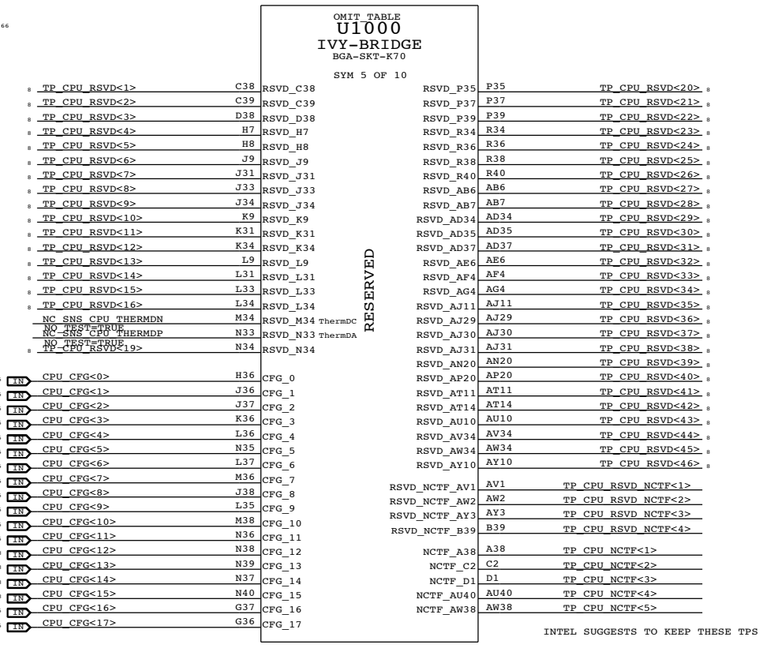
ROUTE B5 TO R1010.1 AS A SEPERATE 12 MIL TRACE.



(IVY BRIDGE EDS #473717 TABLE 6-5)

CFG [1:0]	RESERVED CONFIGURATION LANE	
CFG [2]	PCIE STATIC X16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [3]	PCIE STATIC X4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [4]	RESERVED CONFIGURATION LANE	
CFG [6:5]	PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = 1 X8, 2 X4
CFG [17:7]	RESERVED CONFIGURATION LANE	

SYNC_MASTER=D8 ROSITA SYNC_DATE=03/23/2012

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

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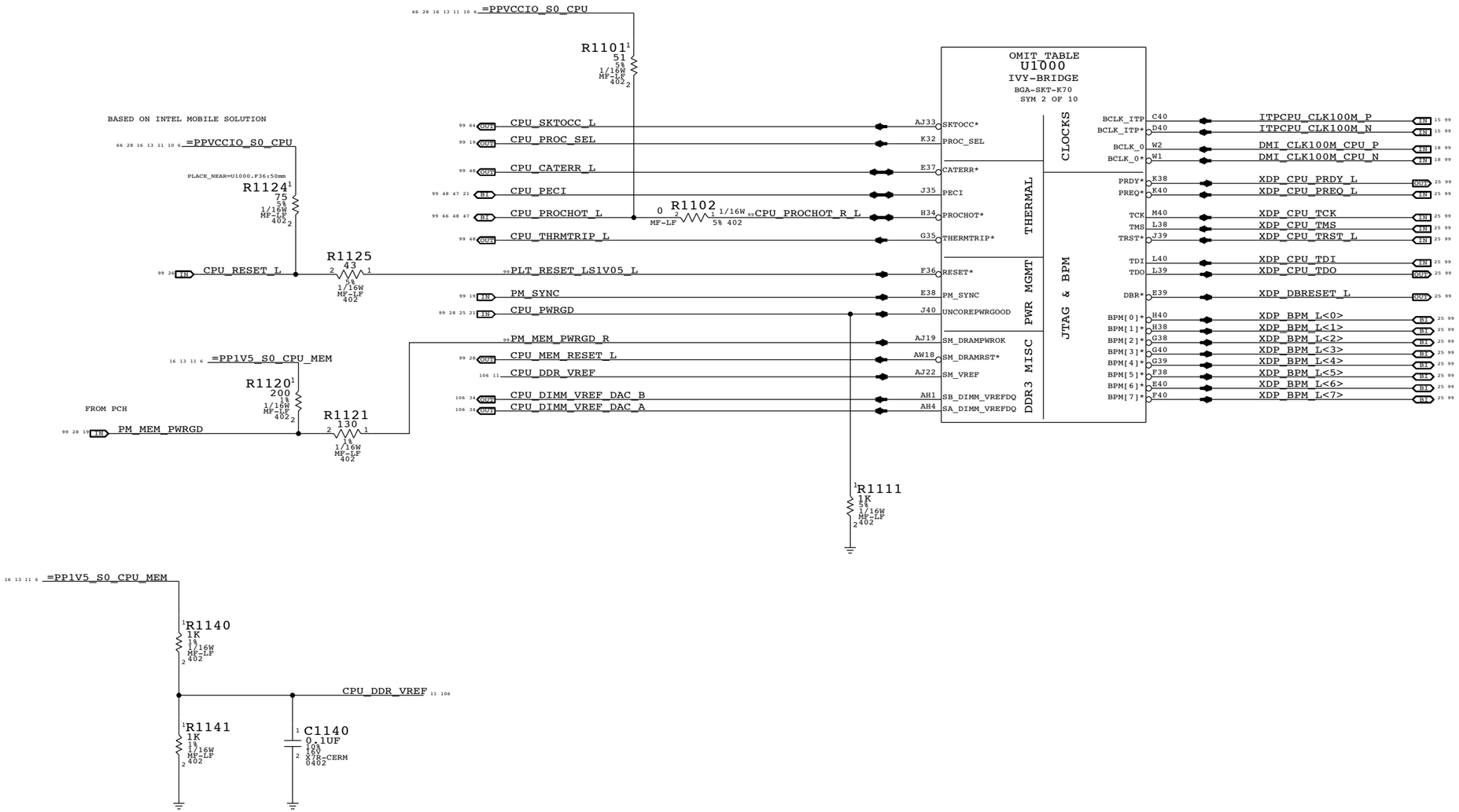

SYNC_MASTER=D7_MLB SYNC_DATE=03/15/2012

PAGE TITLE: CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

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DDR SYSTEM MEMORY A

MEM_A_DQ<0>	AJ3	SA_DQ_0	SA_CK_0	AY25	MEM_A_CLK_P<0>	OUT	29 97
MEM_A_DQ<1>	AJ4	SA_DQ_1	SA_CK_0*	AW25	MEM_A_CLK_N<0>	OUT	29 97
MEM_A_DQ<2>	AL3	SA_DQ_2	SA_CKE_0	AV19	MEM_A_CKE<0>	OUT	29 97
MEM_A_DQ<3>	AL4	SA_DQ_3	SA_CK_1	AU24	MEM_A_CLK_P<1>	OUT	29 97
MEM_A_DQ<4>	AJ2	SA_DQ_4	SA_CK_1*	AU25	MEM_A_CLK_N<1>	OUT	29 97
MEM_A_DQ<5>	AJ1	SA_DQ_5	SA_CKE_1	AT19	MEM_A_CKE<1>	OUT	29 97
MEM_A_DQ<6>	AL2	SA_DQ_6	SA_CK_2	AW27	MEM_A_CLK_P<2>	OUT	30 97
MEM_A_DQ<7>	AL1	SA_DQ_7	SA_CK_2*	AY27	MEM_A_CLK_N<2>	OUT	30 97
MEM_A_DQ<8>	AN1	SA_DQ_8	SA_CKE_2	AU18	MEM_A_CKE<2>	OUT	30 97
MEM_A_DQ<9>	AN4	SA_DQ_9	SA_CK_3	AV26	MEM_A_CLK_P<3>	OUT	30 97
MEM_A_DQ<10>	AR3	SA_DQ_10	SA_CK_3*	AW26	MEM_A_CLK_N<3>	OUT	30 97
MEM_A_DQ<11>	AR4	SA_DQ_11	SA_CKE_3	AV18	MEM_A_CKE<3>	OUT	30 97
MEM_A_DQ<12>	AN2	SA_DQ_12	SA_CS_0*	AU29	MEM_A_CS_L<0>	OUT	29 97
MEM_A_DQ<13>	AN3	SA_DQ_13	SA_CS_1*	AV32	MEM_A_CS_L<1>	OUT	29 97
MEM_A_DQ<14>	AR2	SA_DQ_14	SA_CS_2*	AW30	MEM_A_CS_L<2>	OUT	30 97
MEM_A_DQ<15>	AR1	SA_DQ_15	SA_CS_3*	AU33	MEM_A_CS_L<3>	OUT	30 97
MEM_A_DQ<16>	AV2	SA_DQ_16	SA_ODT_0	AV31	MEM_A_ODT<0>	OUT	29 97
MEM_A_DQ<17>	AW3	SA_DQ_17	SA_ODT_1	AU32	MEM_A_ODT<1>	OUT	29 97
MEM_A_DQ<18>	AV5	SA_DQ_18	SA_ODT_2	AU30	MEM_A_ODT<2>	OUT	30 97
MEM_A_DQ<19>	AW5	SA_DQ_19	SA_ODT_3	AW33	MEM_A_ODT<3>	OUT	30 97
MEM_A_DQ<20>	AU2	SA_DQ_20	SA_DQS_0*	AK2	MEM_A_DQS_N<0>	BI	33 97
MEM_A_DQ<21>	AU3	SA_DQ_21	SA_DQS_1*	AP2	MEM_A_DQS_N<1>	BI	33 97
MEM_A_DQ<22>	AU5	SA_DQ_22	SA_DQS_2*	AV4	MEM_A_DQS_N<2>	BI	33 97
MEM_A_DQ<23>	AY5	SA_DQ_23	SA_DQS_3*	AW8	MEM_A_DQS_N<3>	BI	33 97
MEM_A_DQ<24>	AY7	SA_DQ_24	SA_DQS_4*	AV36	MEM_A_DQS_N<4>	BI	33 97
MEM_A_DQ<25>	AU7	SA_DQ_25	SA_DQS_5*	AP39	MEM_A_DQS_N<5>	BI	33 97
MEM_A_DQ<26>	AV9	SA_DQ_26	SA_DQS_6*	AK39	MEM_A_DQS_N<6>	BI	33 97
MEM_A_DQ<27>	AU9	SA_DQ_27	SA_DQS_7*	AF39	MEM_A_DQS_N<7>	BI	33 97
MEM_A_DQ<28>	AV7	SA_DQ_28	SA_DQS_8*	AV12	TP_MEM_A_DQS_N<8>		8
MEM_A_DQ<29>	AW7	SA_DQ_29	SA_DQS_0	AK3	MEM_A_DQS_P<0>	BI	33 97
MEM_A_DQ<30>	AW9	SA_DQ_30	SA_DQS_1	AP3	MEM_A_DQS_P<1>	BI	33 97
MEM_A_DQ<31>	AY9	SA_DQ_31	SA_DQS_2	AW4	MEM_A_DQS_P<2>	BI	33 97
MEM_A_DQ<32>	AU35	SA_DQ_32	SA_DQS_3	AV8	MEM_A_DQS_P<3>	BI	33 97
MEM_A_DQ<33>	AW37	SA_DQ_33	SA_DQS_4	AV37	MEM_A_DQS_P<4>	BI	33 97
MEM_A_DQ<34>	AU39	SA_DQ_34	SA_DQS_5	AP38	MEM_A_DQS_P<5>	BI	33 97
MEM_A_DQ<35>	AU36	SA_DQ_35	SA_DQS_6	AK38	MEM_A_DQS_P<6>	BI	33 97
MEM_A_DQ<36>	AW35	SA_DQ_36	SA_DQS_7	AF38	MEM_A_DQS_P<7>	BI	33 97
MEM_A_DQ<37>	AY36	SA_DQ_37	SA_DQS_8	AV13	TP_MEM_A_DQS_P<8>		8
MEM_A_DQ<38>	AU38	SA_DQ_38	SA_MA_0	AV27	MEM_A_A<0>	OUT	29 30 97
MEM_A_DQ<39>	AU37	SA_DQ_39	SA_MA_1	AY24	MEM_A_A<1>	OUT	29 30 97
MEM_A_DQ<40>	AR40	SA_DQ_40	SA_MA_2	AW24	MEM_A_A<2>	OUT	29 30 97
MEM_A_DQ<41>	AR37	SA_DQ_41	SA_MA_3	AW23	MEM_A_A<3>	OUT	29 30 97
MEM_A_DQ<42>	AN38	SA_DQ_42	SA_MA_4	AV23	MEM_A_A<4>	OUT	29 30 97
MEM_A_DQ<43>	AN37	SA_DQ_43	SA_MA_5	AT24	MEM_A_A<5>	OUT	29 30 97
MEM_A_DQ<44>	AR39	SA_DQ_44	SA_MA_6	AT23	MEM_A_A<6>	OUT	29 30 97
MEM_A_DQ<45>	AR38	SA_DQ_45	SA_MA_7	AU22	MEM_A_A<7>	OUT	29 30 97
MEM_A_DQ<46>	AN39	SA_DQ_46	SA_MA_8	AV22	MEM_A_A<8>	OUT	29 30 97
MEM_A_DQ<47>	AN40	SA_DQ_47	SA_MA_9	AT22	MEM_A_A<9>	OUT	29 30 97
MEM_A_DQ<48>	AL40	SA_DQ_48	SA_MA_10	AV28	MEM_A_A<10>	OUT	29 30 97
MEM_A_DQ<49>	AL37	SA_DQ_49	SA_MA_11	AU21	MEM_A_A<11>	OUT	29 30 97
MEM_A_DQ<50>	AJ38	SA_DQ_50	SA_MA_12	AT21	MEM_A_A<12>	OUT	29 30 97
MEM_A_DQ<51>	AJ37	SA_DQ_51	SA_MA_13	AW32	MEM_A_A<13>	OUT	29 30 97
MEM_A_DQ<52>	AL39	SA_DQ_52	SA_MA_14	AU20	MEM_A_A<14>	OUT	29 30 97
MEM_A_DQ<53>	AL38	SA_DQ_53	SA_MA_15	AT20	MEM_A_A<15>	OUT	29 30 97
MEM_A_DQ<54>	AJ39	SA_DQ_54	SA_ECC_CB_0	AU12	TP_MEM_A_DQ_CB<0>		8
MEM_A_DQ<55>	AJ40	SA_DQ_55	SA_ECC_CB_1	AU14	TP_MEM_A_DQ_CB<1>		8
MEM_A_DQ<56>	AG40	SA_DQ_56	SA_ECC_CB_2	AW13	TP_MEM_A_DQ_CB<2>		8
MEM_A_DQ<57>	AG37	SA_DQ_57	SA_ECC_CB_3	AY13	TP_MEM_A_DQ_CB<3>		8
MEM_A_DQ<58>	AE38	SA_DQ_58	SA_ECC_CB_4	AU13	TP_MEM_A_DQ_CB<4>		8
MEM_A_DQ<59>	AE37	SA_DQ_59	SA_ECC_CB_5	AU11	TP_MEM_A_DQ_CB<5>		8
MEM_A_DQ<60>	AG39	SA_DQ_60	SA_ECC_CB_6	AY12	TP_MEM_A_DQ_CB<6>		8
MEM_A_DQ<61>	AG38	SA_DQ_61	SA_ECC_CB_7	AW12	TP_MEM_A_DQ_CB<7>		8
MEM_A_DQ<62>	AE39	SA_DQ_62					
MEM_A_DQ<63>	AE40	SA_DQ_63					
MEM_A_BA<0>	AY29	SA_BS_0					
MEM_A_BA<1>	AW28	SA_BS_1					
MEM_A_BA<2>	AV20	SA_BS_2					
MEM_A_CAS_L	AV30	SA_CAS*					
MEM_A_RAS_L	AU28	SA_RAS*					
MEM_A_WE_L	AW29	SA_WE*					

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DDR SYSTEM MEMORY B

MEM_B_DQ<0>	AG7	SB_DQ_0	SB_CK_0	AL21	MEM_B_CLK_P<0>	OUT	31 97
MEM_B_DQ<1>	AG8	SB_DQ_1	SB_CK_0*	AL22	MEM_B_CLK_N<0>	OUT	31 97
MEM_B_DQ<2>	AJ9	SB_DQ_2	SB_CKE_0	AU16	MEM_B_CKE<0>	OUT	31 97
MEM_B_DQ<3>	AJ8	SB_DQ_3	SB_CK_1	AL20	MEM_B_CLK_P<1>	OUT	31 97
MEM_B_DQ<4>	AG5	SB_DQ_4	SB_CK_1*	AK20	MEM_B_CLK_N<1>	OUT	31 97
MEM_B_DQ<5>	AG6	SB_DQ_5	SB_CKE_1	AY15	MEM_B_CKE<1>	OUT	31 97
MEM_B_DQ<6>	AJ6	SB_DQ_6	SB_CK_2	AL23	MEM_B_CLK_P<2>	OUT	32 97
MEM_B_DQ<7>	AJ7	SB_DQ_7	SB_CK_2*	AM22	MEM_B_CLK_N<2>	OUT	32 97
MEM_B_DQ<8>	AL7	SB_DQ_8	SB_CKE_2	AW15	MEM_B_CKE<2>	OUT	32 97
MEM_B_DQ<9>	AM7	SB_DQ_9	SB_CK_3	AP21	MEM_B_CLK_P<3>	OUT	32 97
MEM_B_DQ<10>	AM10	SB_DQ_10	SB_CK_3*	AN21	MEM_B_CLK_N<3>	OUT	32 97
MEM_B_DQ<11>	AL10	SB_DQ_11	SB_CKE_3	AV15	MEM_B_CKE<3>	OUT	32 97
MEM_B_DQ<12>	AL6	SB_DQ_12	SB_CS_0*	AN25	MEM_B_CS_L<0>	OUT	31 97
MEM_B_DQ<13>	AM6	SB_DQ_13	SB_CS_1*	AN26	MEM_B_CS_L<1>	OUT	31 97
MEM_B_DQ<14>	AL9	SB_DQ_14	SB_CS_2*	AL25	MEM_B_CS_L<2>	OUT	32 97
MEM_B_DQ<15>	AM9	SB_DQ_15	SB_CS_3*	AT26	MEM_B_CS_L<3>	OUT	32 97
MEM_B_DQ<16>	AP7	SB_DQ_16	SB_ODT_0	AL26	MEM_B_ODT<0>	OUT	31 97
MEM_B_DQ<17>	AR7	SB_DQ_17	SB_ODT_1	AP26	MEM_B_ODT<1>	OUT	31 97
MEM_B_DQ<18>	AP10	SB_DQ_18	SB_ODT_2	AM26	MEM_B_ODT<2>	OUT	32 97
MEM_B_DQ<19>	AR10	SB_DQ_19	SB_ODT_3	AK26	MEM_B_ODT<3>	OUT	32 97
MEM_B_DQ<20>	AP6	SB_DQ_20	SB_DQS_0*	AH6	MEM_B_DQS_N<0>	BI	33 97
MEM_B_DQ<21>	AR6	SB_DQ_21	SB_DQS_1*	AL8	MEM_B_DQS_N<1>	BI	33 97
MEM_B_DQ<22>	AP9	SB_DQ_22	SB_DQS_2*	AP8	MEM_B_DQS_N<2>	BI	33 97
MEM_B_DQ<23>	AR9	SB_DQ_23	SB_DQS_3*	AN12	MEM_B_DQS_N<3>	BI	33 97
MEM_B_DQ<24>	AM12	SB_DQ_24	SB_DQS_4*	AN28	MEM_B_DQS_N<4>	BI	33 97
MEM_B_DQ<25>	AM13	SB_DQ_25	SB_DQS_5*	AR33	MEM_B_DQS_N<5>	BI	33 97
MEM_B_DQ<26>	AR13	SB_DQ_26	SB_DQS_6*	AM33	MEM_B_DQS_N<6>	BI	33 97
MEM_B_DQ<27>	AP13	SB_DQ_27	SB_DQS_7*	AG34	MEM_B_DQS_N<7>	BI	33 97
MEM_B_DQ<28>	AL12	SB_DQ_28	SB_DQS_8*	AN15	TP_MEM_B_DQS_N<8>		8
MEM_B_DQ<29>	AL13	SB_DQ_29	SB_DQS_0	AH7	MEM_B_DQS_P<0>	BI	33 97
MEM_B_DQ<30>	AR12	SB_DQ_30	SB_DQS_1	AM8	MEM_B_DQS_P<1>	BI	33 97
MEM_B_DQ<31>	AP12	SB_DQ_31	SB_DQS_2	AR8	MEM_B_DQS_P<2>	BI	33 97
MEM_B_DQ<32>	AR28	SB_DQ_32	SB_DQS_3	AN13	MEM_B_DQS_P<3>	BI	33 97
MEM_B_DQ<33>	AR29	SB_DQ_33	SB_DQS_4	AN29	MEM_B_DQS_P<4>	BI	33 97
MEM_B_DQ<34>	AL28	SB_DQ_34	SB_DQS_5	AP33	MEM_B_DQS_P<5>	BI	33 97
MEM_B_DQ<35>	AL29	SB_DQ_35	SB_DQS_6	AL33	MEM_B_DQS_P<6>	BI	33 97
MEM_B_DQ<36>	AP28	SB_DQ_36	SB_DQS_7	AG35	MEM_B_DQS_P<7>	BI	33 97
MEM_B_DQ<37>	AP29	SB_DQ_37	SB_DQS_8	AN16	TP_MEM_B_DQS_P<8>		8
MEM_B_DQ<38>	AM28	SB_DQ_38	SB_MA_0	AK24	MEM_B_A<0>	OUT	31 32 97
MEM_B_DQ<39>	AM29	SB_DQ_39	SB_MA_1	AM20	MEM_B_A<1>	OUT	31 32 97
MEM_B_DQ<40>	AP32	SB_DQ_40	SB_MA_2	AM19	MEM_B_A<2>	OUT	31 32 97
MEM_B_DQ<41>	AP31	SB_DQ_41	SB_MA_3	AK18	MEM_B_A<3>	OUT	31 32 97
MEM_B_DQ<42>	AP35	SB_DQ_42	SB_MA_4	AP19	MEM_B_A<4>	OUT	31 32 97
MEM_B_DQ<43>	AP34	SB_DQ_43	SB_MA_5	AP18	MEM_B_A<5>	OUT	31 32 97
MEM_B_DQ<44>	AR32	SB_DQ_44	SB_MA_6	AM18	MEM_B_A<6>	OUT	31 32 97
MEM_B_DQ<45>	AR31	SB_DQ_45	SB_MA_7	AL18	MEM_B_A<7>	OUT	31 32 97
MEM_B_DQ<46>	AR35	SB_DQ_46	SB_MA_8	AN18	MEM_B_A<8>	OUT	31 32 97
MEM_B_DQ<47>	AR34	SB_DQ_47	SB_MA_9	AY17	MEM_B_A<9>	OUT	31 32 97
MEM_B_DQ<48>	AM32	SB_DQ_48	SB_MA_10	AN23	MEM_B_A<10>	OUT	31 32 97
MEM_B_DQ<49>	AM31	SB_DQ_49	SB_MA_11	AU17	MEM_B_A<11>	OUT	31 32 97
MEM_B_DQ<50>	AL35	SB_DQ_50	SB_MA_12	AT18	MEM_B_A<12>	OUT	31 32 97
MEM_B_DQ<51>	AL32	SB_DQ_51	SB_MA_13	AR26	MEM_B_A<13>	OUT	31 32 97
MEM_B_DQ<52>	AM34	SB_DQ_52	SB_MA_14	AY16	MEM_B_A<14>	OUT	31 32 97
MEM_B_DQ<53>	AL31	SB_DQ_53	SB_MA_15	AV16	MEM_B_A<15>	OUT	31 32 97
MEM_B_DQ<54>	AM35	SB_DQ_54	SB_ECC_CB_0	AL16	TP_MEM_B_DQ_CB<0>		8
MEM_B_DQ<55>	AL34	SB_DQ_55	SB_ECC_CB_1	AM16	TP_MEM_B_DQ_CB<1>		8
MEM_B_DQ<56>	AH35	SB_DQ_56	SB_ECC_CB_2	AP16	TP_MEM_B_DQ_CB<2>		8
MEM_B_DQ<57>	AH34	SB_DQ_57	SB_ECC_CB_3	AR16	TP_MEM_B_DQ_CB<3>		8
MEM_B_DQ<58>	AE34	SB_DQ_58	SB_ECC_CB_4	AL15	TP_MEM_B_DQ_CB<4>		8
MEM_B_DQ<59>	AE35	SB_DQ_59	SB_ECC_CB_5	AM15	TP_MEM_B_DQ_CB<5>		8
MEM_B_DQ<60>	AJ35	SB_DQ_60	SB_ECC_CB_6	AR15	TP_MEM_B_DQ_CB<6>		8
MEM_B_DQ<61>	AJ34	SB_DQ_61	SB_ECC_CB_7	AP15	TP_MEM_B_DQ_CB<7>		8
MEM_B_DQ<62>	AF33	SB_DQ_62					
MEM_B_DQ<63>	AF35	SB_DQ_63					
MEM_B_BA<0>	AP23	SB_BS_0					
MEM_B_BA<1>	AM24	SB_BS_1					
MEM_B_BA<2>	AW17	SB_BS_2					
MEM_B_CAS_L	AK25	SB_CAS*					
MEM_B_RAS_L	AP24	SB_RAS*					
MEM_B_WE_L	AR25	SB_WE*					

SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

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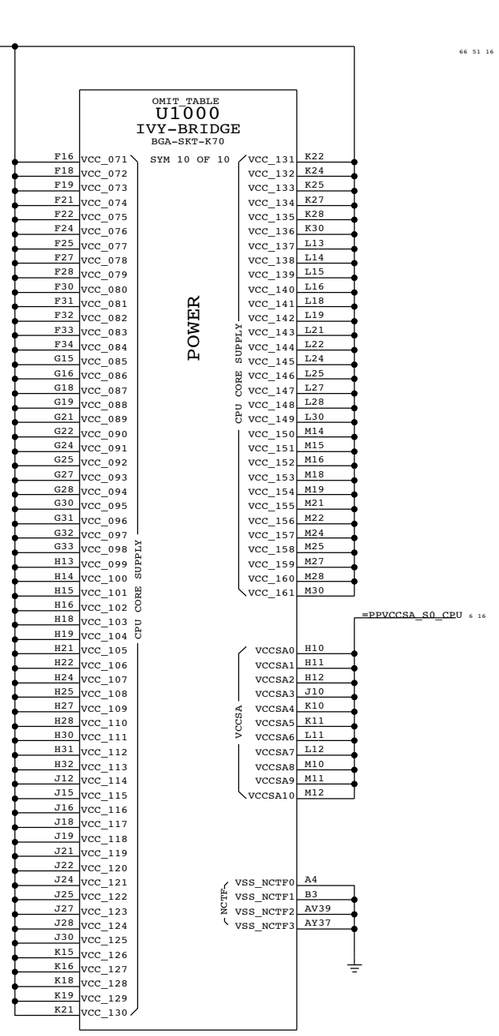

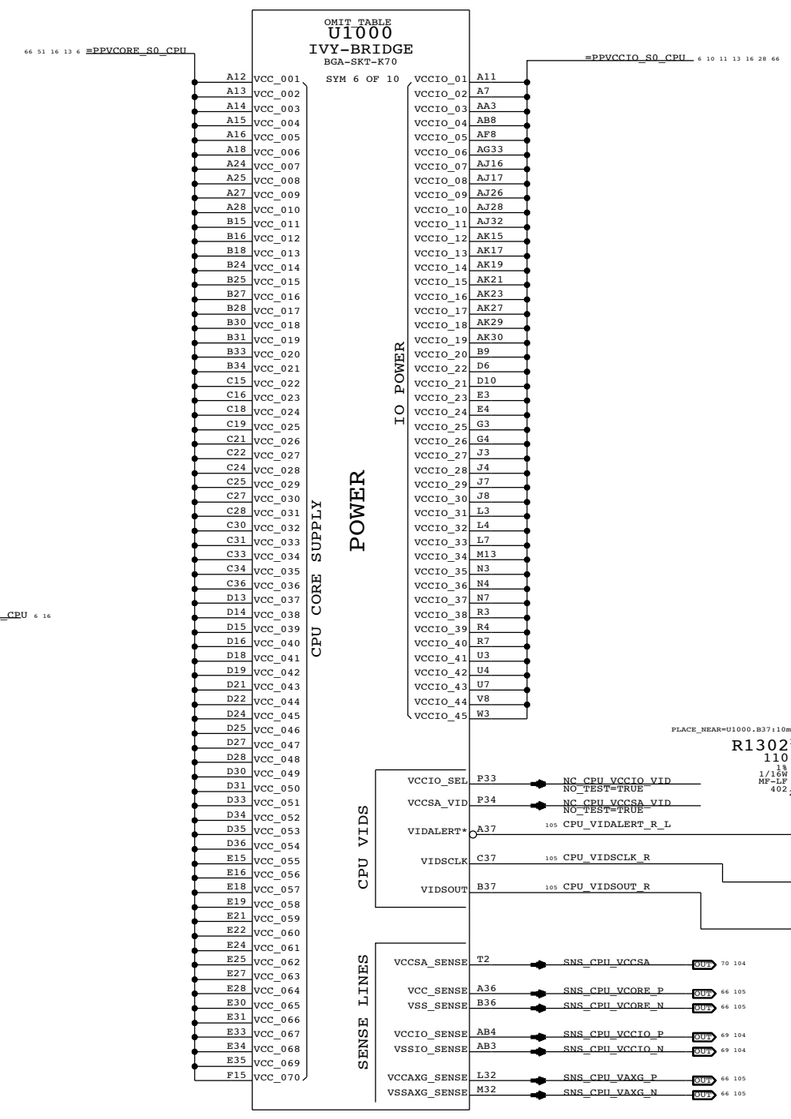

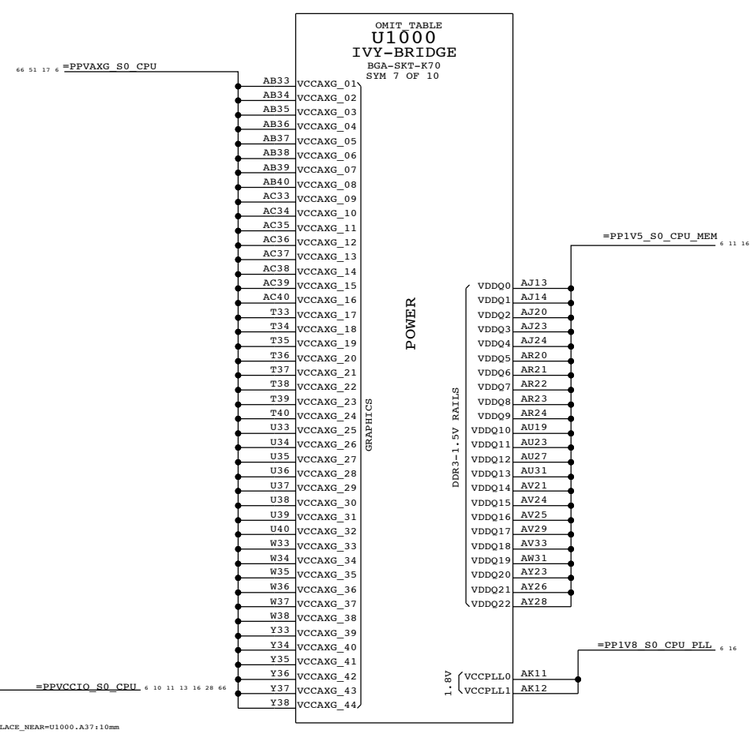

SYNC_MASTER=D7_MLB SYNC_DATE=03/15/2012

PAGE TITLE
CPU POWER

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
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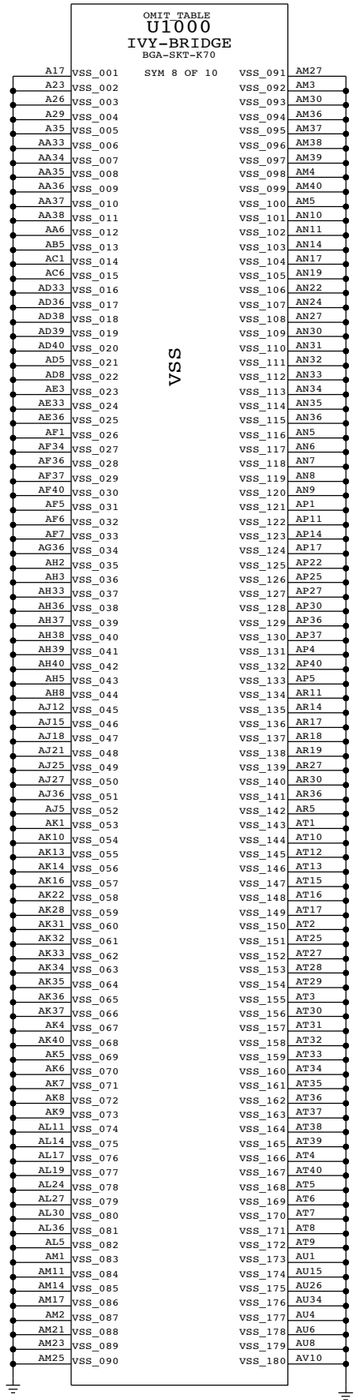
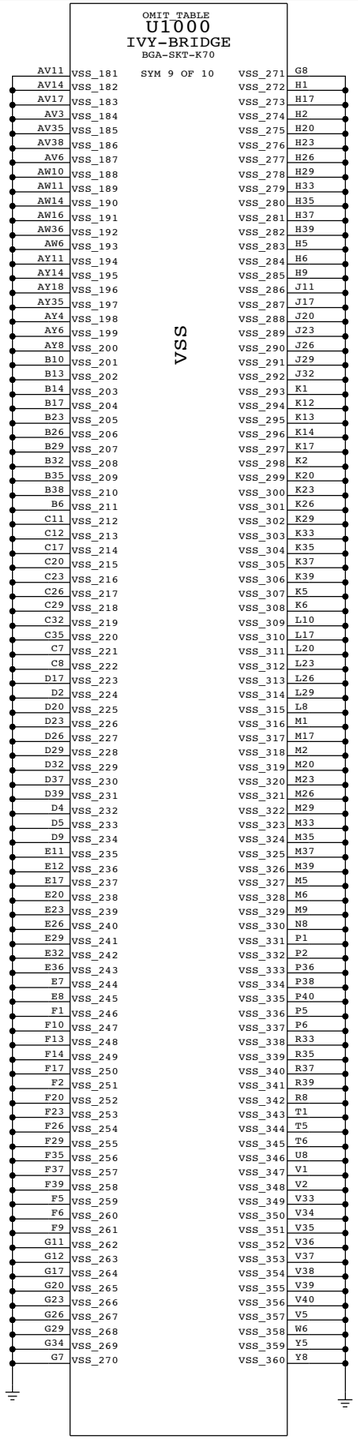
SHEET 13 OF 117





SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE

CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

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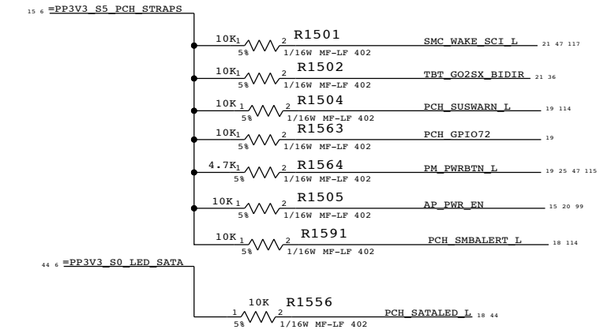
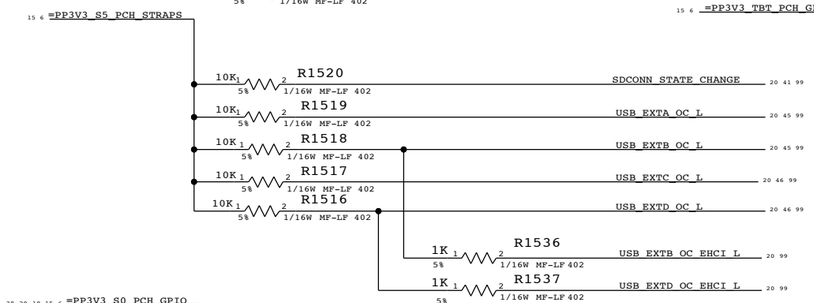
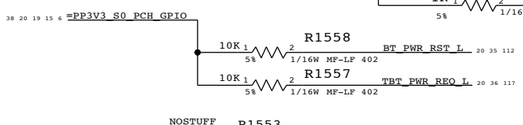
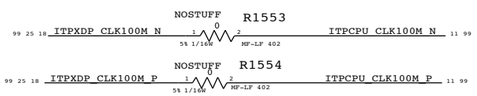
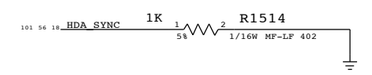
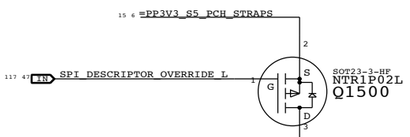


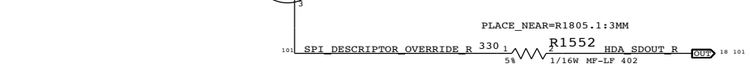


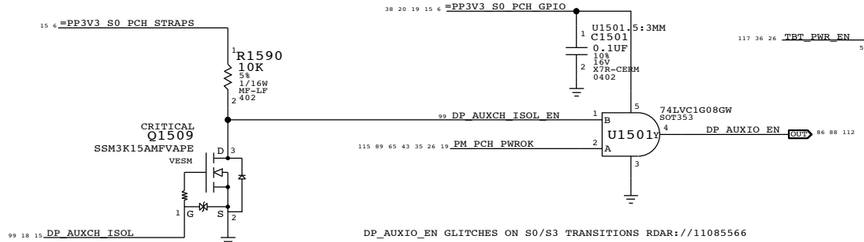










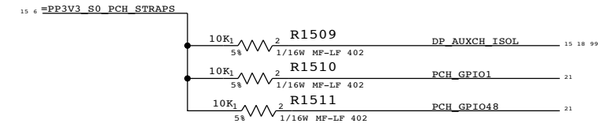


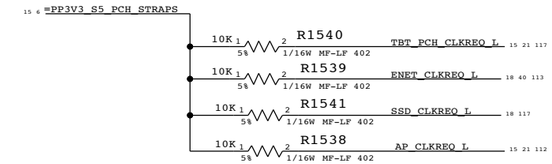
DP_AUXCH_ISOL IS ACTIVE LOW!

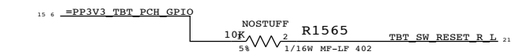
DP_AUXIO_EN GLITCHES ON S0/S3 TRANSITIONS RDAR://11085566

DP_AUXIO_EN Inversion

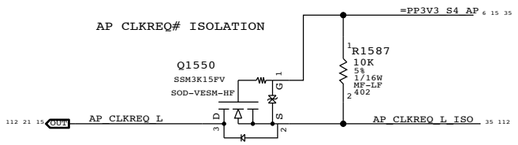
Inverts PCH GPIO DP_AUXCH_ISOL to drive DP_AUXIO_EN for external DP





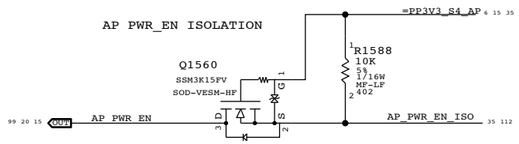


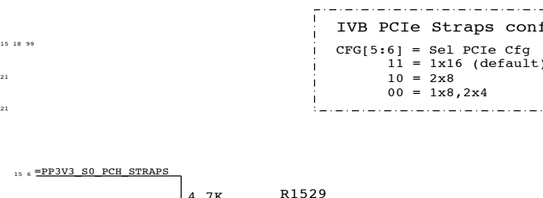
AP CLKREQ# ISOLATION

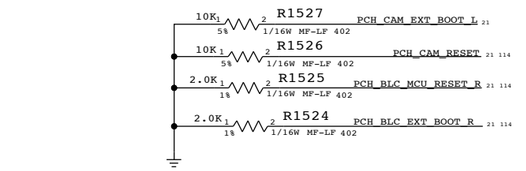


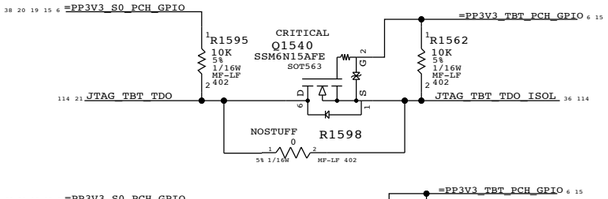
ISOLATION FET TO PREVENT LEAKAGE ON AP_PWR_EN AND AP_CLKREQ_L RDAR://11068662

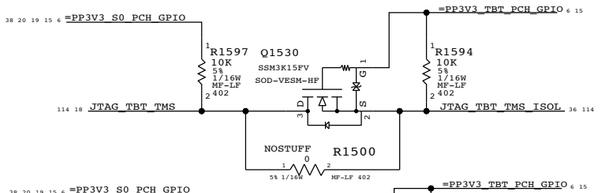
AP PWR_EN ISOLATION

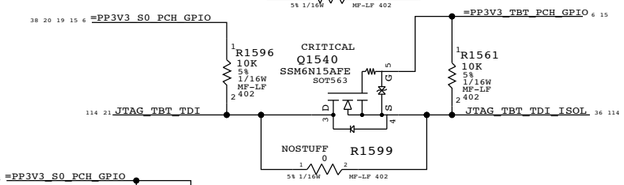


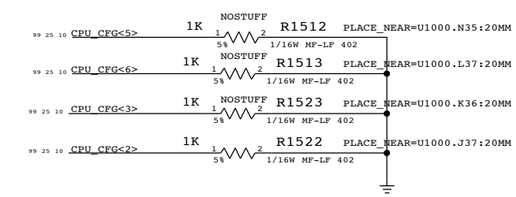


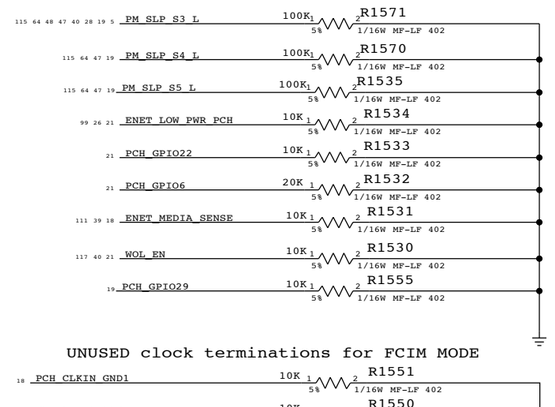




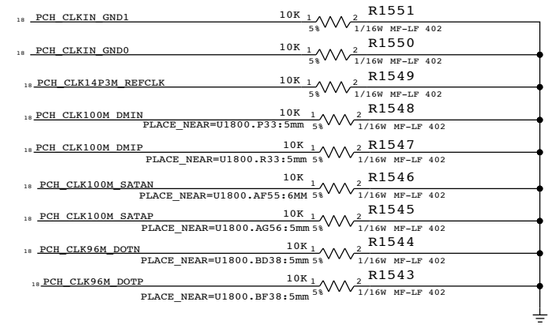


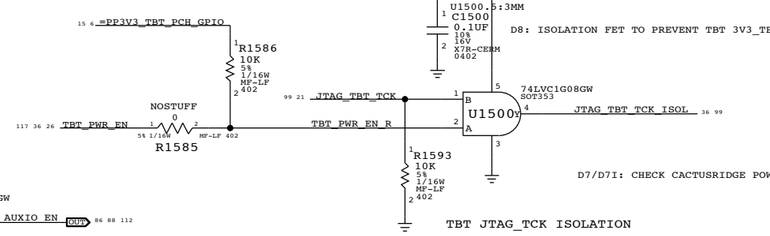






UNUSED clock terminations for FCIM MODE

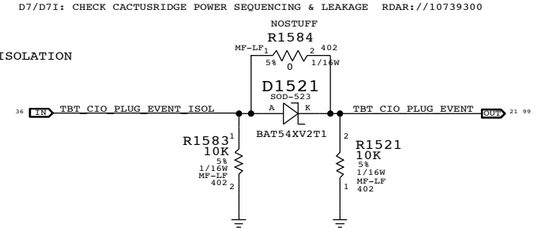


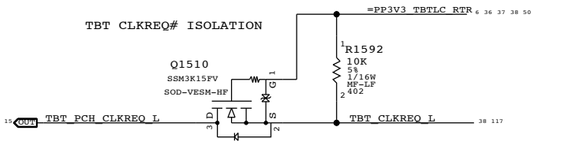


D8: ISOLATION FET TO PREVENT TBT 3V3_TBTLC LEAKAGE RDAR://10885566

TBT JTAG_TCK ISOLATION

D7/D7I: CHECK CACTUSRIDGE POWER SEQUENCING & LEAKAGE RDAR://10739300





TBT CLKREQ# ISOLATION

IVB PCIe Straps configuration:

CFG[5:6] = Sel PCIe Cfg
11 = 1x16 (default)
10 = 2x8
00 = 1x8,2x4

CFG[3]=Direct/Rev for X4
1 = DIR
0 = REV

CFG[2]= Direct/Rev for x16
1 = DIR
0 = REV

SYNC MASTER=D8 MLB SYNC DATE=03/29/2012

PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

Apple Inc.

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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613):

REPLACED WITH 603 PER RDAR://10700439

16 13 6 66 51 =PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609
22UF 20% 6.3V X5R-CERM2 0603

C1610 C1611 C1612 C1613
22UF 20% 6.3V X5R-CERM2 0603

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

66 51 16 13 6 =PPVCORE_S0_CPU

Place inside socket cavity

C1620 C1621 C1622 C1623 C1624 C1625 C1626 C1627 C1628 C1629
10UF 20% 6.3V X5R 603

C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 66 28 =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657
22UF 20% 6.3V X5R-CERM2 0603

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

C1660 C1661 C1662 C1663 C1664 C1665
10uF 20% 6.3V X5R 603

BULK CAPS ON CPU VREG PAGE 74

CRITICAL

C1670
330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805

13 6 =PPVCCSA_S0_CPU

C1666 C1667
10uF 20% 6.3V X5R 603

Bulk decoupling is on VCCSA reg page 75

Memory (CPU VCCDDR) DECOUPLING

13 11 6 =PP1V5_S0_CPU_MEM

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686
22UF 20% 6.3V X5R-CERM2 0603
1UF 20% 6.3V X5R 0201

CRITICAL
NOSTUFF

C1687
330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 C1694 C1692 C1691 C1695 C1690 C1696 C1697
1UF 10% 16V X5R 402
2.2UF 10% 6.3V X5R 402
4.7UF 10% 6.3V X5R-CERM 603
10UF 20% 6.3V X5R 603
22UF 20% 6.3V X5R-CERM2 0603
47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 77

SYNC MASTER=D7 MLB SYNC DATE=12/20/2011

PAGE TITLE
CPU NON-GFX DECOUPLING

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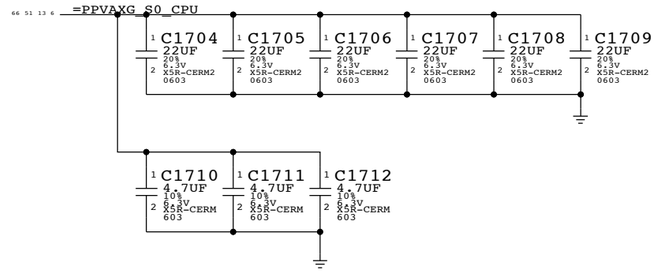
VAXG DECOUPLING

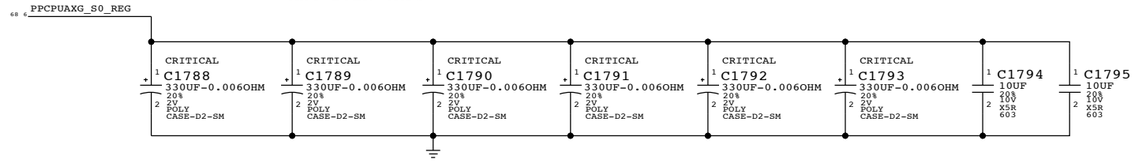
INTEL RECOMMENDATION 4X22UF 0805,3X 4.7UF

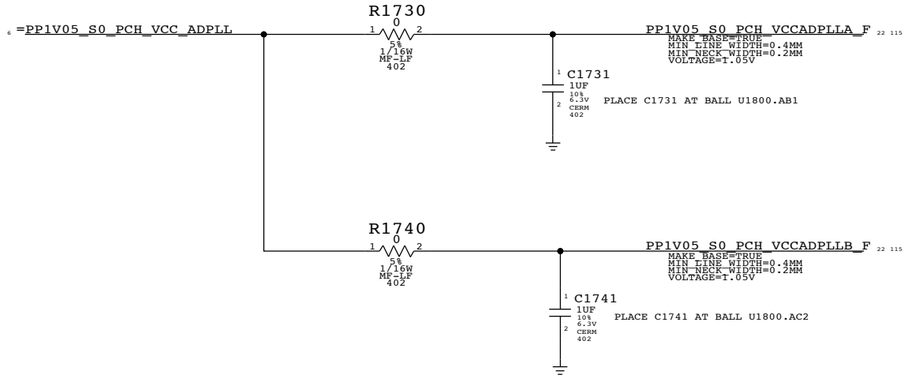
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



AXG BULK CAPS





SYNC_MASTER=D8 KOSECOFF SYNC_DATE=01/26/2012

PAGE TITLE

GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

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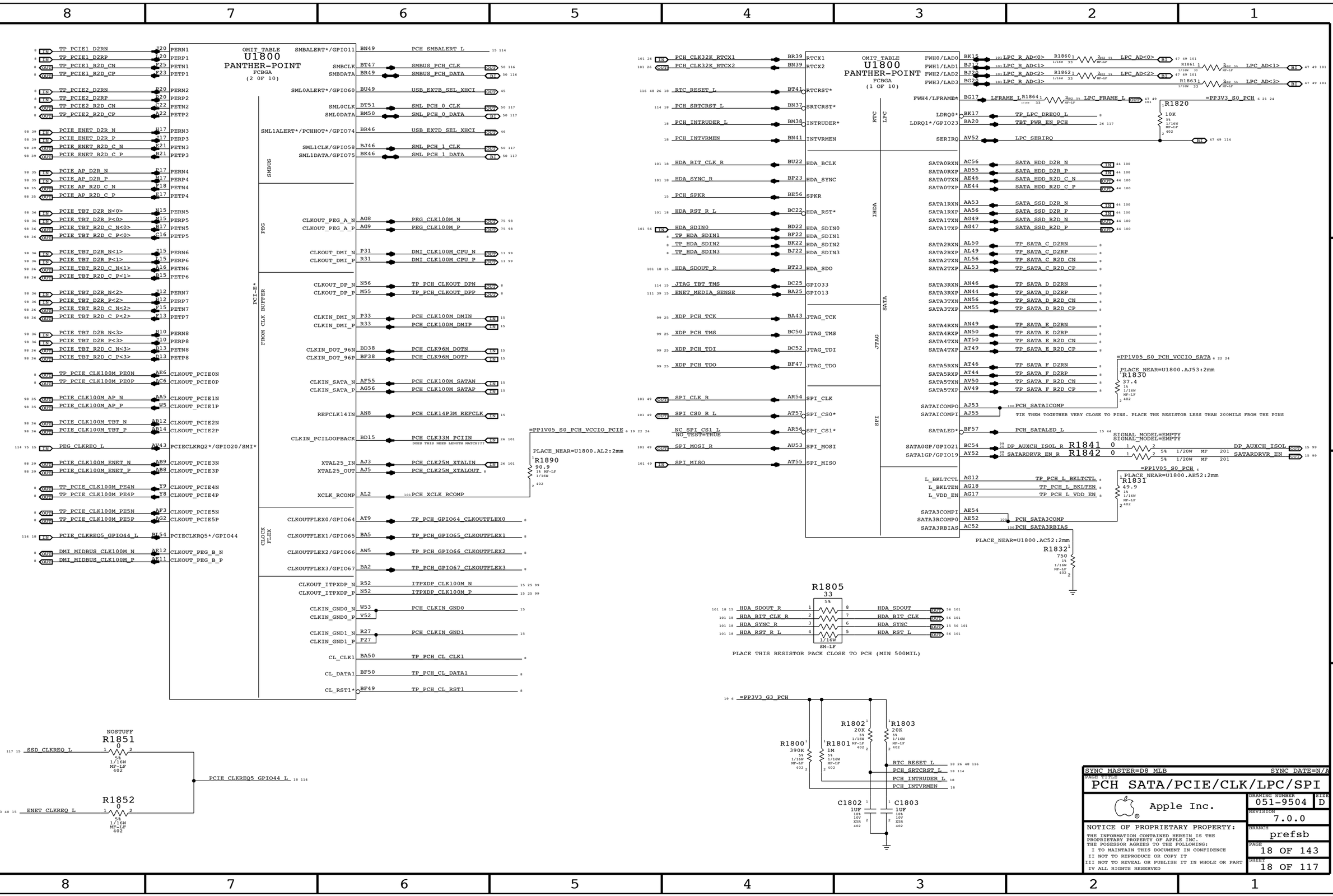
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U1800
PANTHER-POINT
FCBGA
(2 OF 10)
PCI-E*
FROM CLK BUFFER
SMBUS
PEG
CLOCK FLEX
OMIT_TABLE
U1800
PANTHER-POINT
FCBGA
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
PLACE THIS RESISTOR PACK CLOSE TO PCH (MIN 500MIL)
TIE THEM TOGETHER VERY CLOSE TO PINS. PLACE THE RESISTOR LESS THAN 200MILS FROM THE PINS
NOSTUFF
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PCH SATA/PCIE/CLK/LPC/SPI
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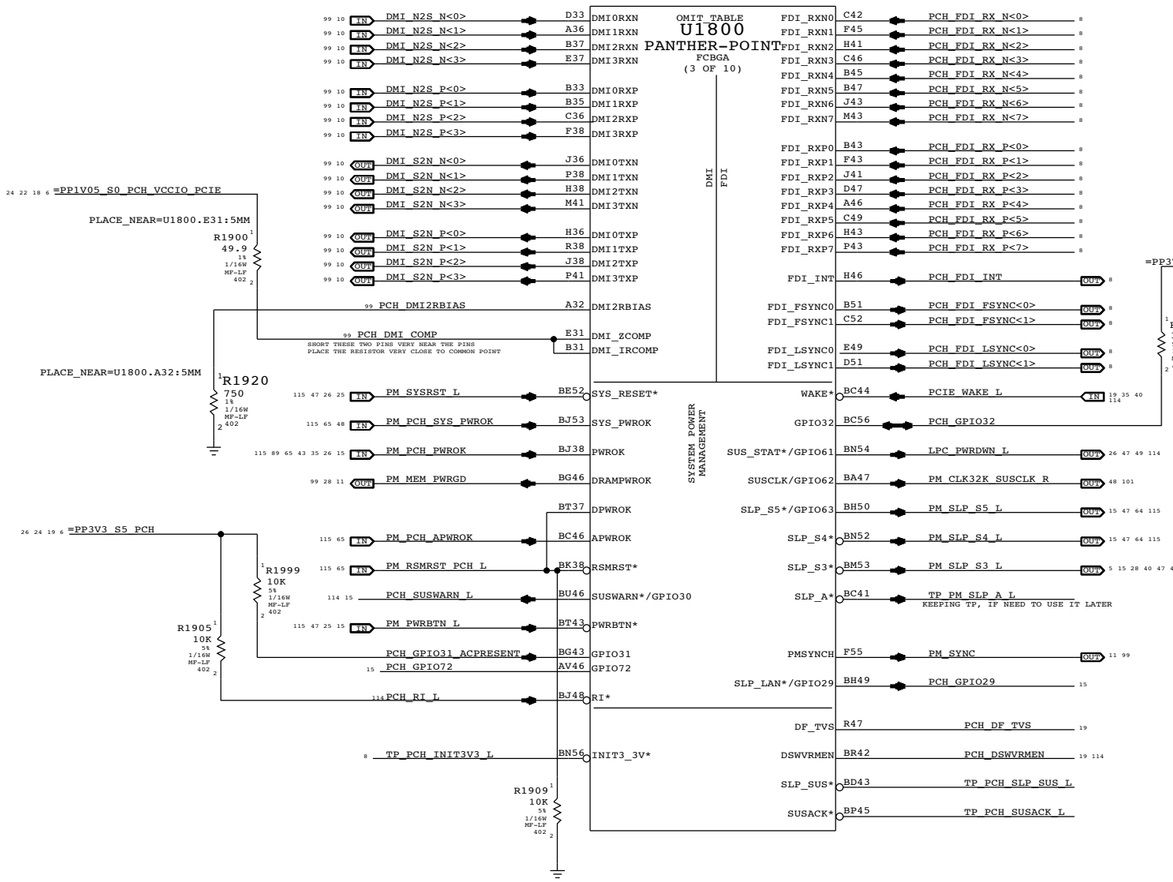

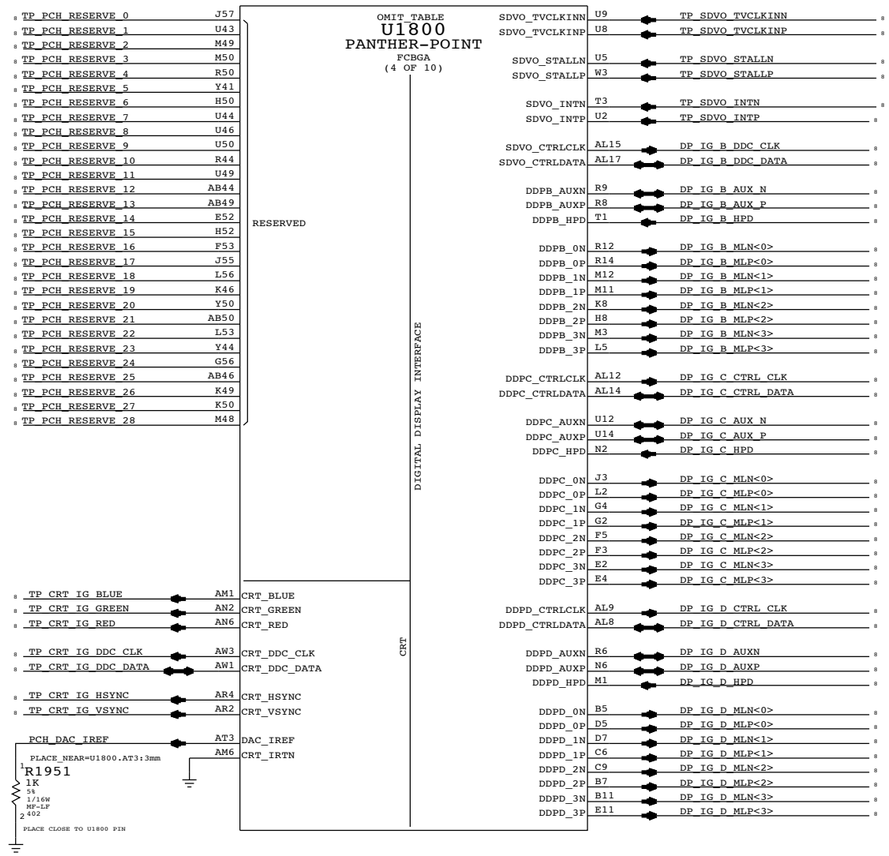

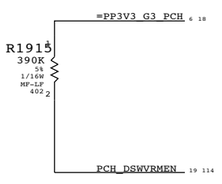

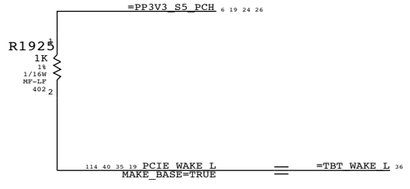

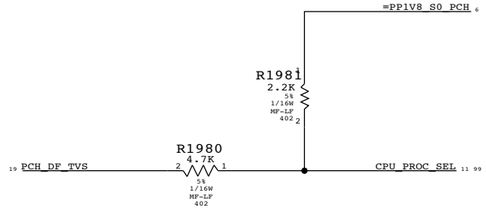

SYNC_MASTER=D7_MLB SYNC_DATE=03/15/2012

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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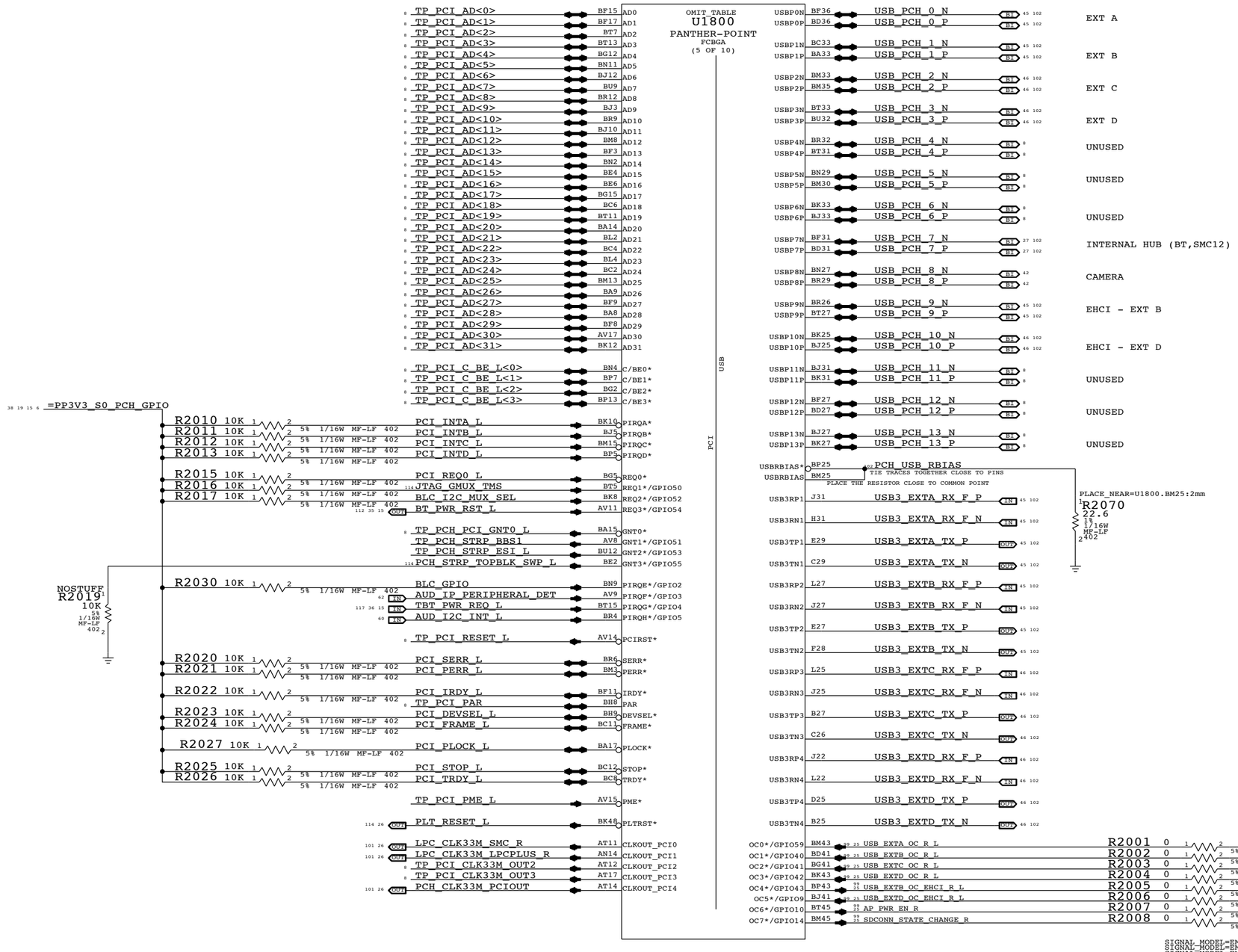
OMIT TABLE
U1800
PANTHER-POINT
FCBGA
(5 OF 10)
PCI
USB
TP_PCI_AD<0> BF15 AD0
TP_PCI_AD<1> BF17 AD1
TP_PCI_AD<2> BT7 AD2
TP_PCI_AD<3> BT13 AD3
TP_PCI_AD<4> BG12 AD4
TP_PCI_AD<5> BN11 AD5
TP_PCI_AD<6> BJ12 AD6
TP_PCI_AD<7> BU9 AD7
TP_PCI_AD<8> BR12 AD8
TP_PCI_AD<9> BJ3 AD9
TP_PCI_AD<10> BR9 AD10
TP_PCI_AD<11> BJ10 AD11
TP_PCI_AD<12> BM8 AD12
TP_PCI_AD<13> BF3 AD13
TP_PCI_AD<14> BN2 AD14
TP_PCI_AD<15> BE4 AD15
TP_PCI_AD<16> BE6 AD16
TP_PCI_AD<17> BG15 AD17
TP_PCI_AD<18> BC6 AD18
TP_PCI_AD<19> BT11 AD19
TP_PCI_AD<20> BA14 AD20
TP_PCI_AD<21> BL2 AD21
TP_PCI_AD<22> BC4 AD22
TP_PCI_AD<23> BL4 AD23
TP_PCI_AD<24> BC2 AD24
TP_PCI_AD<25> BM13 AD25
TP_PCI_AD<26> BA9 AD26
TP_PCI_AD<27> BF9 AD27
TP_PCI_AD<28> BA8 AD28
TP_PCI_AD<29> BF8 AD29
TP_PCI_AD<30> AV17 AD30
TP_PCI_AD<31> BK12 AD31
TP_PCI_C_BE_L<0> BN4 C/BE0*
TP_PCI_C_BE_L<1> BP7 C/BE1*
TP_PCI_C_BE_L<2> BG2 C/BE2*
TP_PCI_C_BE_L<3> BP13 C/BE3*
=PP3V3_S0_PCH_GPIO
R2010 10K 5% 1/16W MF-LF 402
R2011 10K 5% 1/16W MF-LF 402
R2012 10K 5% 1/16W MF-LF 402
R2013 10K 5% 1/16W MF-LF 402
PCI_INTA_L BK10 PIRQA*
PCI_INTB_L BJ5 PIRQB*
PCI_INTC_L BM15 PIRQC*
PCI_INTD_L BP5 PIRQD*
R2015 10K 5% 1/16W MF-LF 402
R2016 10K 5% 1/16W MF-LF 402
R2017 10K 5% 1/16W MF-LF 402
PCI_REQ0_L BG5 REQ0*
JTAG_GMUX_TMS BT5 REQ1*/GPIO50
BLC_I2C_MUX_SEL BK8 REQ2*/GPIO52
BT_PWR_RST_L AV11 REQ3*/GPIO54
TP_PCH_PCI_GNT0_L BA15 GNT0*
TP_PCH_STRP_BBS1 AV8 GNT1*/GPIO51
TP_PCH_STRP_ESI_L BU12 GNT2*/GPIO53
PCH_STRP_TOPBLK_SWP_L BE2 GNT3*/GPIO55
NOSTUFF
R2019 10K 5% 1/16W MF-LF 402
R2030 10K 5% 1/16W MF-LF 402
BLC_GPIO BN9 PIRQE*/GPIO2
AUD_IP_PERIPHERAL_DET AV9 PIRQF*/GPIO3
TBT_PWR_REQ_L BT15 PIRQG*/GPIO4
AUD_I2C_INT_L BR4 PIRQH*/GPIO5
TP_PCI_RESET_L AV14 PCIRST*
R2020 10K 5% 1/16W MF-LF 402
R2021 10K 5% 1/16W MF-LF 402
PCI_SERR_L BR6 SERR*
PCI_PERR_L BM3 PERR*
R2022 10K 5% 1/16W MF-LF 402
PCI_IRDY_L BF11 IRDY*
TP_PCI_PAR BH8 PAR
R2023 10K 5% 1/16W MF-LF 402
R2024 10K 5% 1/16W MF-LF 402
PCI_DEVSEL_L BH9 DEVSEL*
PCI_FRAME_L BC11 FRAME*
R2027 10K 5% 1/16W MF-LF 402
PCI_PLOCK_L BA17 PLOCK*
R2025 10K 5% 1/16W MF-LF 402
R2026 10K 5% 1/16W MF-LF 402
PCI_STOP_L BC12 STOP*
PCI_TRDY_L BC8 TRDY*
TP_PCI_PME_L AV15 PME*
PLT_RESET_L BK48 PLTRST*
LPC_CLK33M_SMC_R AT11 CLKOUT_PCI0
LPC_CLK33M_LPCPLUS_R AN14 CLKOUT_PCI1
TP_PCI_CLK33M_OUT2 AT12 CLKOUT_PCI2
TP_PCI_CLK33M_OUT3 AT17 CLKOUT_PCI3
PCH_CLK33M_PCIOUT AT14 CLKOUT_PCI4
USBP0N BF36 USB_PCH_0_N
USBP0P BD36 USB_PCH_0_P
EXT A
USBP1N BC33 USB_PCH_1_N
USBP1P BA33 USB_PCH_1_P
EXT B
USBP2N BM33 USB_PCH_2_N
USBP2P BM35 USB_PCH_2_P
EXT C
USBP3N BT33 USB_PCH_3_N
USBP3P BU32 USB_PCH_3_P
EXT D
USBP4N BR32 USB_PCH_4_N
USBP4P BT31 USB_PCH_4_P
UNUSED
USBP5N BN29 USB_PCH_5_N
USBP5P BM30 USB_PCH_5_P
UNUSED
USBP6N BK33 USB_PCH_6_N
USBP6P BJ33 USB_PCH_6_P
UNUSED
USBP7N BF31 USB_PCH_7_N
USBP7P BD31 USB_PCH_7_P
INTERNAL HUB (BT,SMC12)
USBP8N BN27 USB_PCH_8_N
USBP8P BR29 USB_PCH_8_P
CAMERA
USBP9N BR26 USB_PCH_9_N
USBP9P BT27 USB_PCH_9_P
EHCI - EXT B
USBP10N BK25 USB_PCH_10_N
USBP10P BJ25 USB_PCH_10_P
EHCI - EXT D
USBP11N BJ31 USB_PCH_11_N
USBP11P BK31 USB_PCH_11_P
UNUSED
USBP12N BF27 USB_PCH_12_N
USBP12P BD27 USB_PCH_12_P
UNUSED
USBP13N BJ27 USB_PCH_13_N
USBP13P BK27 USB_PCH_13_P
UNUSED
USBRBIAS* BP25 PCH_USB_RBIAS
USBRBIAS BM25
TIE TRACES TOGETHER CLOSE TO PINS
PLACE THE RESISTOR CLOSE TO COMMON POINT
PLACE_NEAR=U1800.BM25:2mm
R2070 22.6 1% 1/16W MF-LF 402
USB3RP1 J31 USB3_EXTA_RX_F_P
USB3RN1 H31 USB3_EXTA_RX_F_N
USB3TP1 E29 USB3_EXTA_TX_P
USB3TN1 C29 USB3_EXTA_TX_N
USB3RP2 L27 USB3_EXTB_RX_F_P
USB3RN2 J27 USB3_EXTB_RX_F_N
USB3TP2 E27 USB3_EXTB_TX_P
USB3TN2 F28 USB3_EXTB_TX_N
USB3RP3 L25 USB3_EXTC_RX_F_P
USB3RN3 J25 USB3_EXTC_RX_F_N
USB3TP3 B27 USB3_EXTC_TX_P
USB3TN3 C26 USB3_EXTC_TX_N
USB3RP4 J22 USB3_EXTD_RX_F_P
USB3RN4 L22 USB3_EXTD_RX_F_N
USB3TP4 D25 USB3_EXTD_TX_P
USB3TN4 B25 USB3_EXTD_TX_N
OC0*/GPIO59 BM43 USB_EXTA_OC_R_L
OC1*/GPIO40 BD41 USB_EXTB_OC_R_L
OC2*/GPIO41 BG41 USB_EXTC_OC_R_L
OC3*/GPIO42 BK43 USB_EXTD_OC_R_L
OC4*/GPIO43 BP43 USB_EXTB_OC_EHCI_R_L
OC5*/GPIO9 BJ41 USB_EXTD_OC_EHCI_R_L
OC6*/GPIO10 BT45 AP_PWR_EN_R
OC7*/GPIO14 BM45 SDCONN_STATE_CHANGE_R
R2001 0 5% 1/20W MF 201 USB_EXTA_OC_L
R2002 0 5% 1/20W MF 201 USB_EXTB_OC_L
R2003 0 5% 1/20W MF 201 USB_EXTC_OC_L
R2004 0 5% 1/20W MF 201 USB_EXTD_OC_L
R2005 0 5% 1/20W MF 201 USB_EXTB_OC_EHCI_L
R2006 0 5% 1/20W MF 201 USB_EXTD_OC_EHCI_L
R2007 0 5% 1/20W MF 201 AP_PWR_EN
R2008 0 5% 1/20W MF 201 SDCONN_STATE_CHANGE
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SIGNAL_MODEL=EMPTY
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PCH PCI/USB
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SIZE D
REVISION 7.0.0
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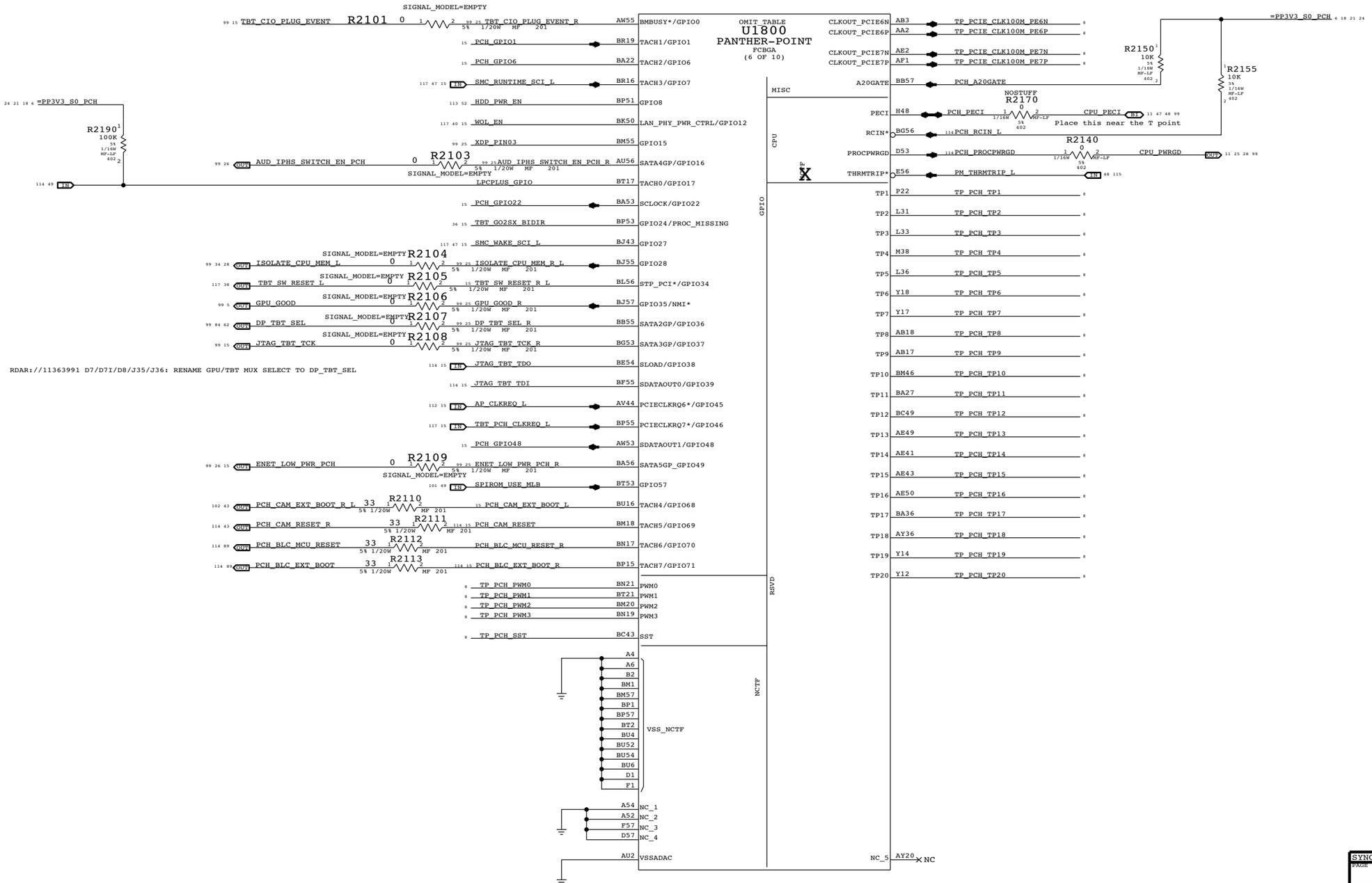

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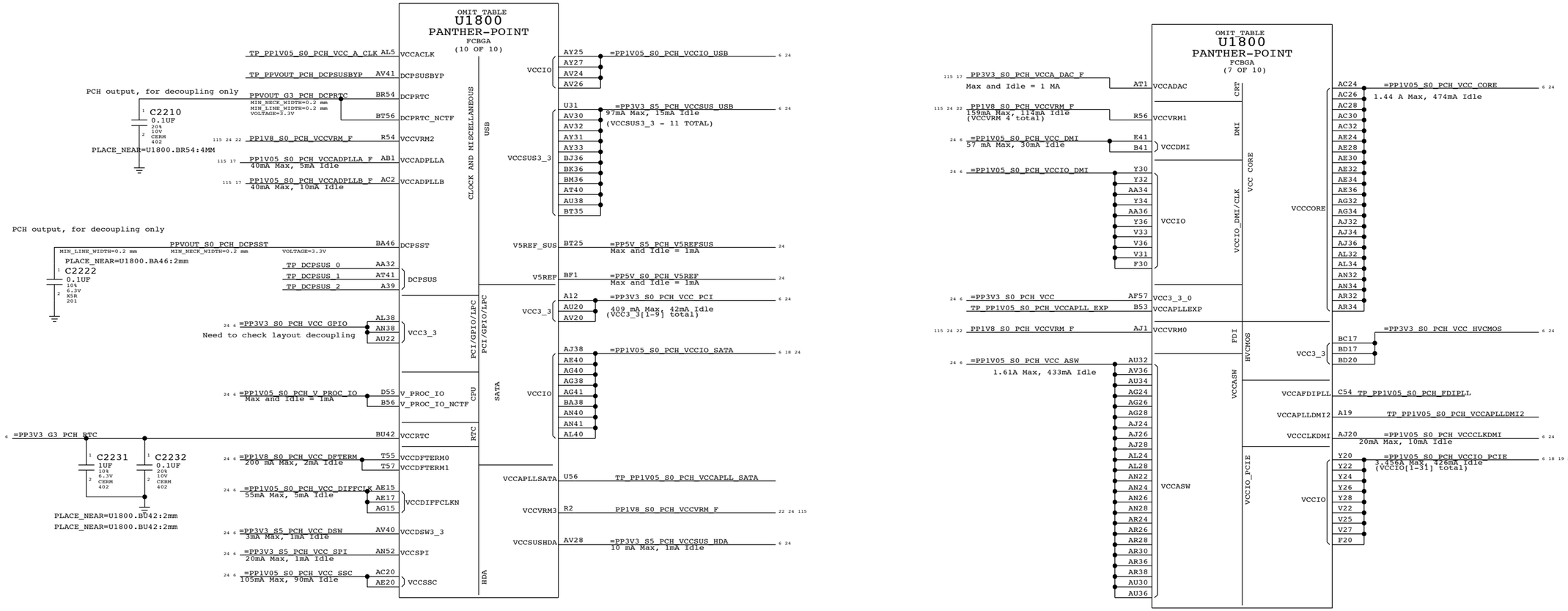

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PCH POWER

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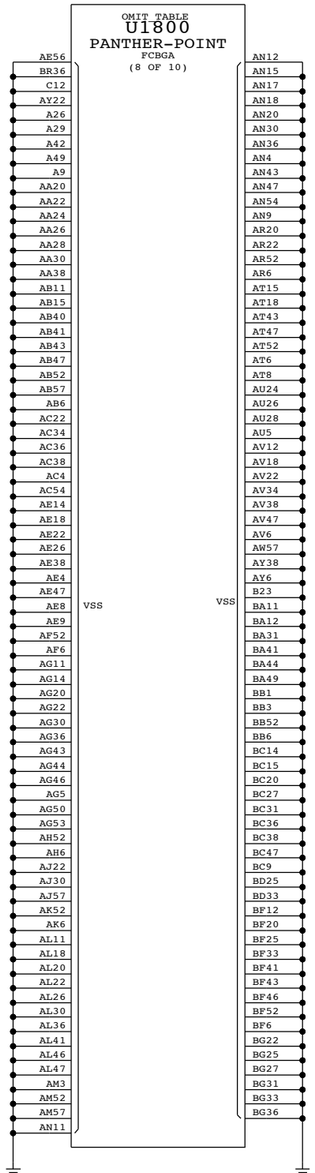

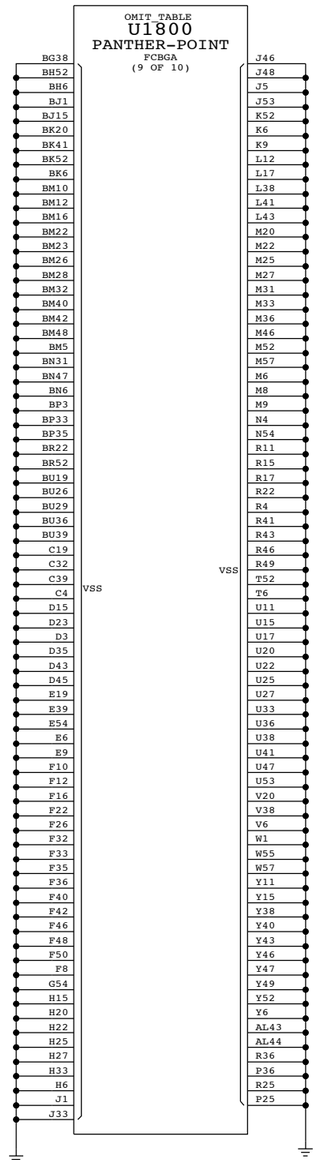

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PCH GROUNDS

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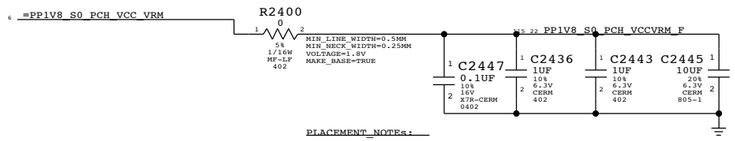

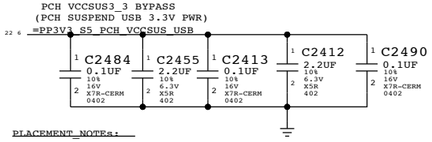

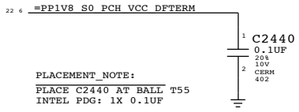

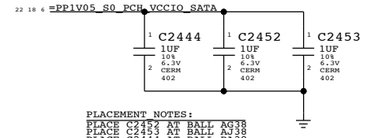

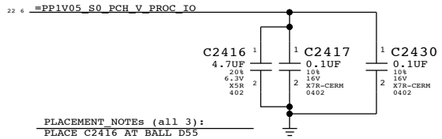

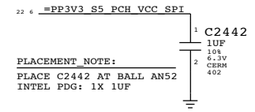

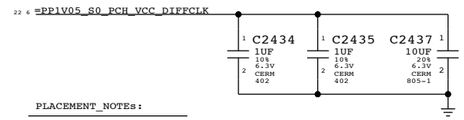

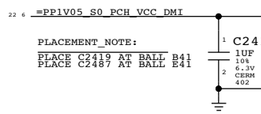

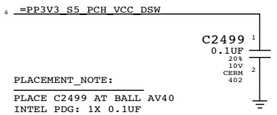

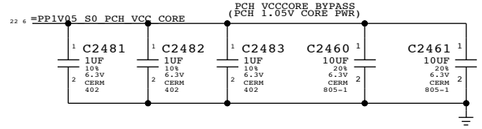

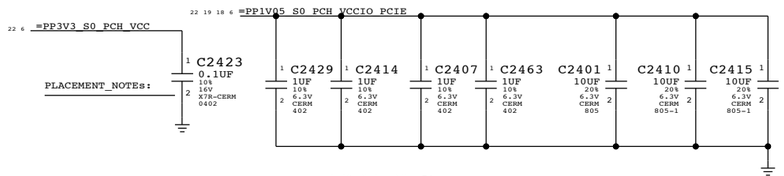

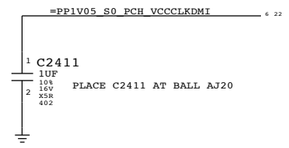

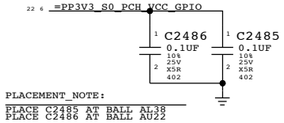

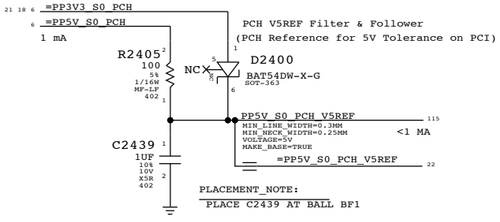

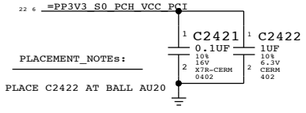

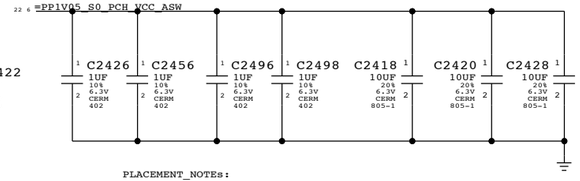

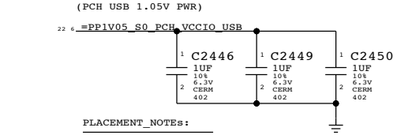

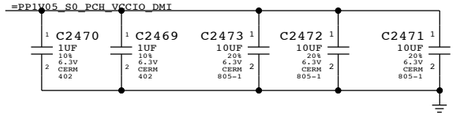

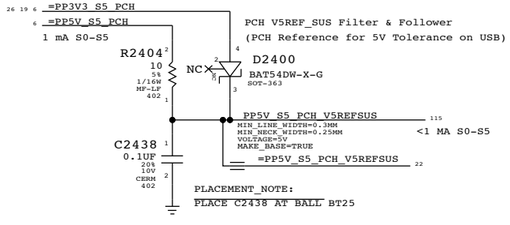

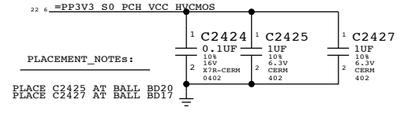

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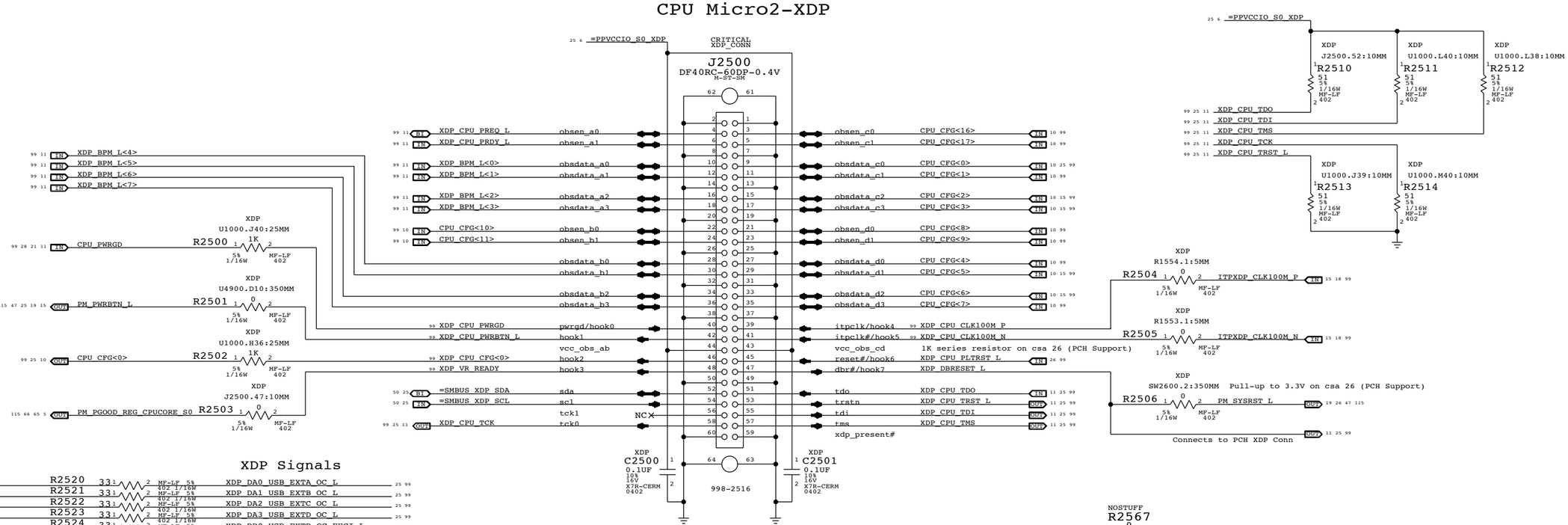
CPU Micro2-XDP

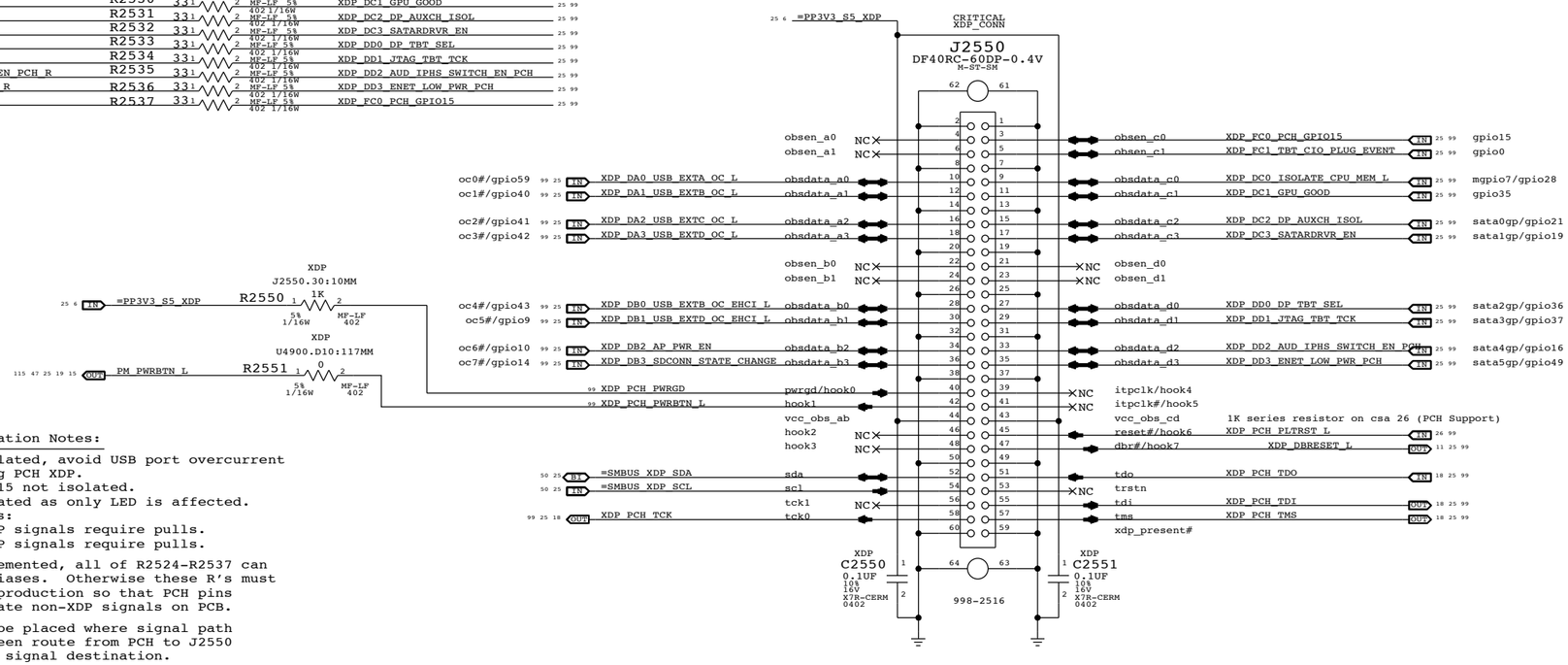


PCH Signals

USB_EXTA_OC_R_L	R2520	33	XDP_DA0_USB_EXTA_OC_L
USB_EXTB_OC_R_L	R2521	33	XDP_DA1_USB_EXTB_OC_L
USB_EXTC_OC_R_L	R2522	33	XDP_DA2_USB_EXTC_OC_L
USB_EXTD_OC_R_L	R2523	33	XDP_DA3_USB_EXTD_OC_L
USB_EXTB_OC_EHCI_R_L	R2524	33	XDP_DB0_USB_EXTB_OC_EHCI_L
USB_EXTD_OC_EHCI_R_L	R2525	33	XDP_DB1_USB_EXTD_OC_EHCI_L
AP_PWR_EN_R	R2526	33	XDP_DB2_AP_PWR_EN
SDCONN_STATE_CHANGE_R	R2527	33	XDP_DB3_SDCONN_STATE_CHANGE
TBT_CIO_PLUG_EVENT_R	R2528	33	XDP_FC1_TBT_CIO_PLUG_EVENT
ISOLATE_CPU_MEM_R_L	R2529	33	XDP_DC0_ISOLATE_CPU_MEM_L
GPU_GOOD_R	R2530	33	XDP_DC1_GPU_GOOD
DP_AUXCH_ISOL_R	R2531	33	XDP_DC2_DP_AUXCH_ISOL
SATARDRVR_EN_R	R2532	33	XDP_DC3_SATARDRVR_EN
DP_TBT_SEL_R	R2533	33	XDP_DD0_DP_TBT_SEL
JTAG_TBT_TCK_R	R2534	33	XDP_DD1_JTAG_TBT_TCK
AUD_IPHS_SWITCH_EN_PCH_R	R2535	33	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH_R	R2536	33	XDP_DD3_ENET_LOW_PWR_PCH
XDP_PIN03	R2537	33	XDP_FC0_PCH_GPIO15

XDP Signals

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

SYNC MASTER=D7 MLB SYNC DATE=01/26/2012

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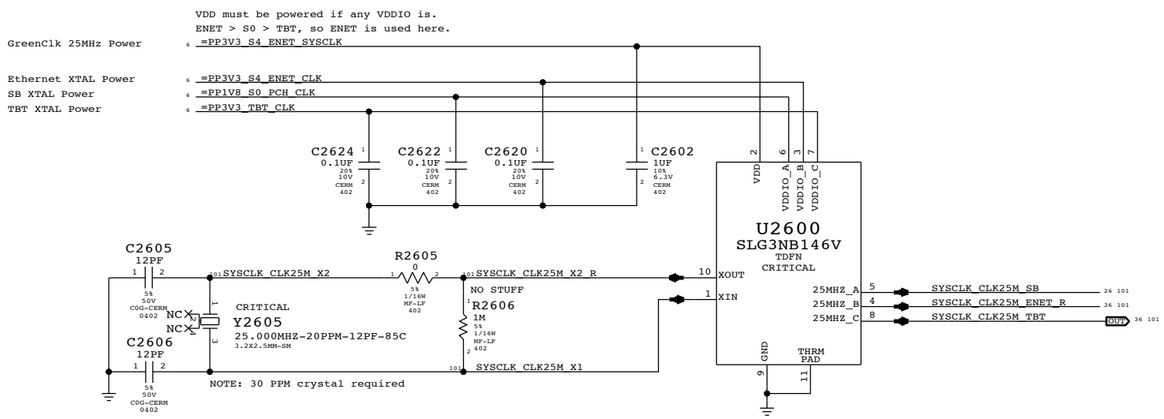
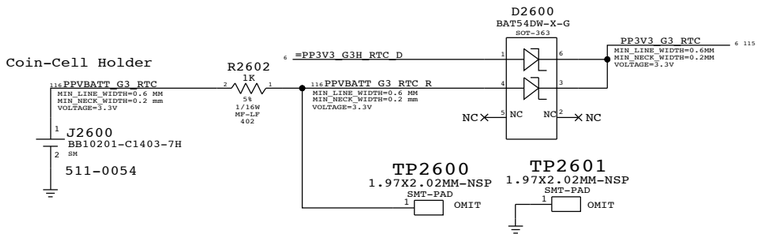
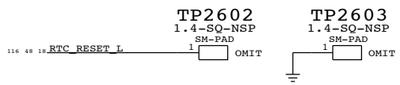
System 25MHz Clock Generator



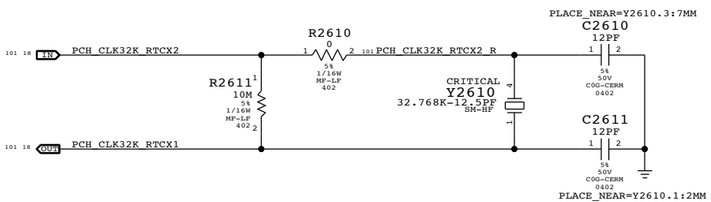
RTC Power Sources



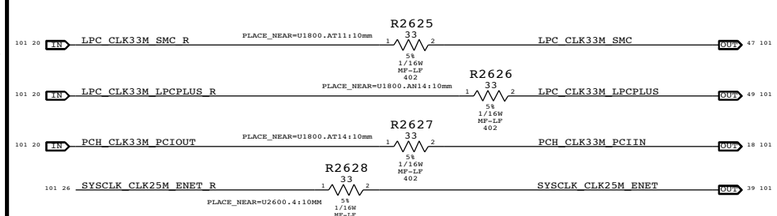
RDAR://11218892 TESTPOINT TO RESET RTC FOR APPLE CARE



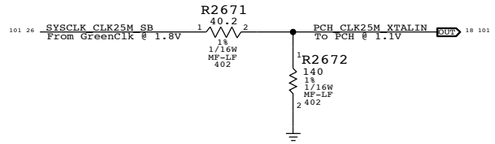
PCH RTC Crystal



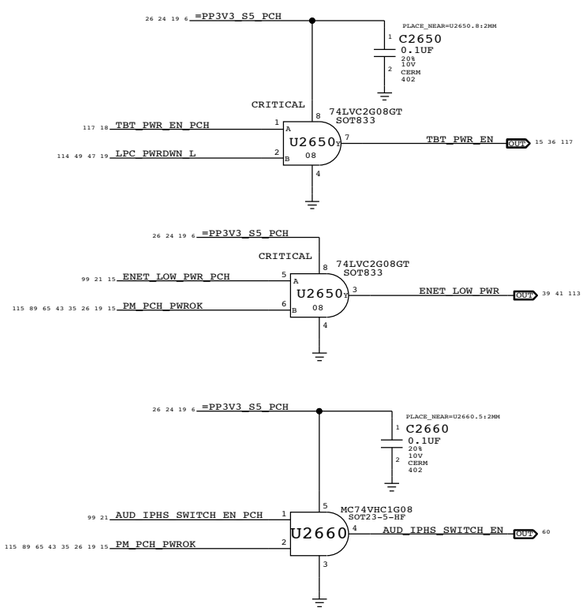
Clock series termination



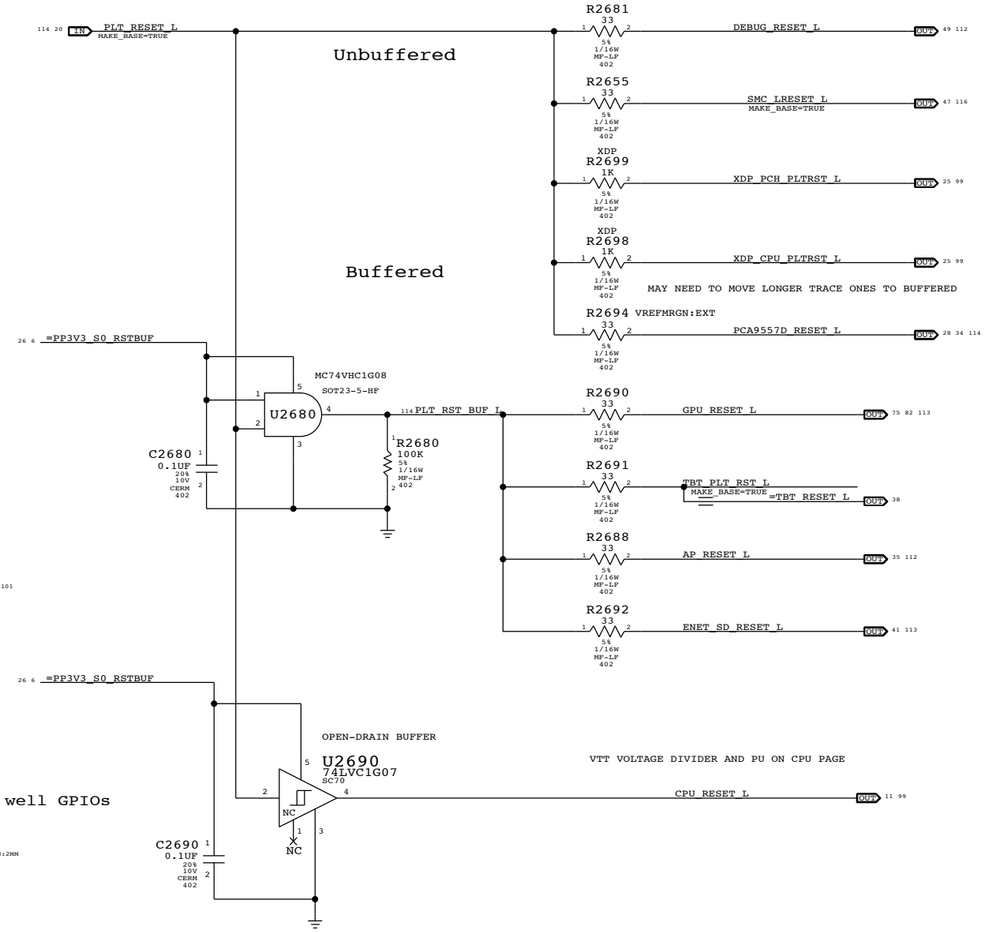
PCH 25MHZ CLOCK



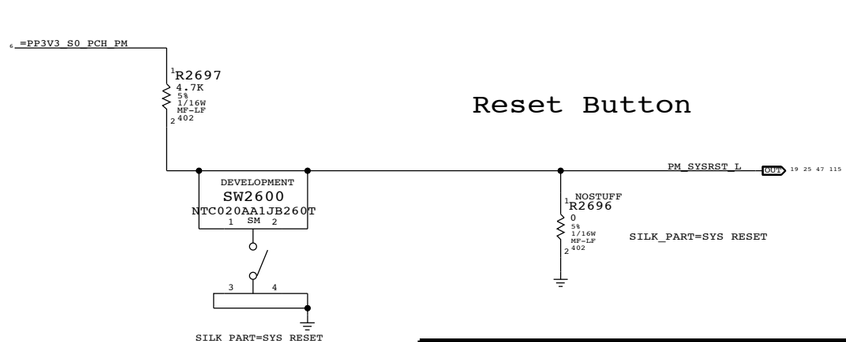
GPIO Isolation to prevent glitches on critical core well GPIOs



Platform Reset Connections



Reset Button



SYNC_MASTER=D8_MLB SYNC_DATE=N/A

PAGE TITLE
CHIPSET SUPPORT

Apple Inc.

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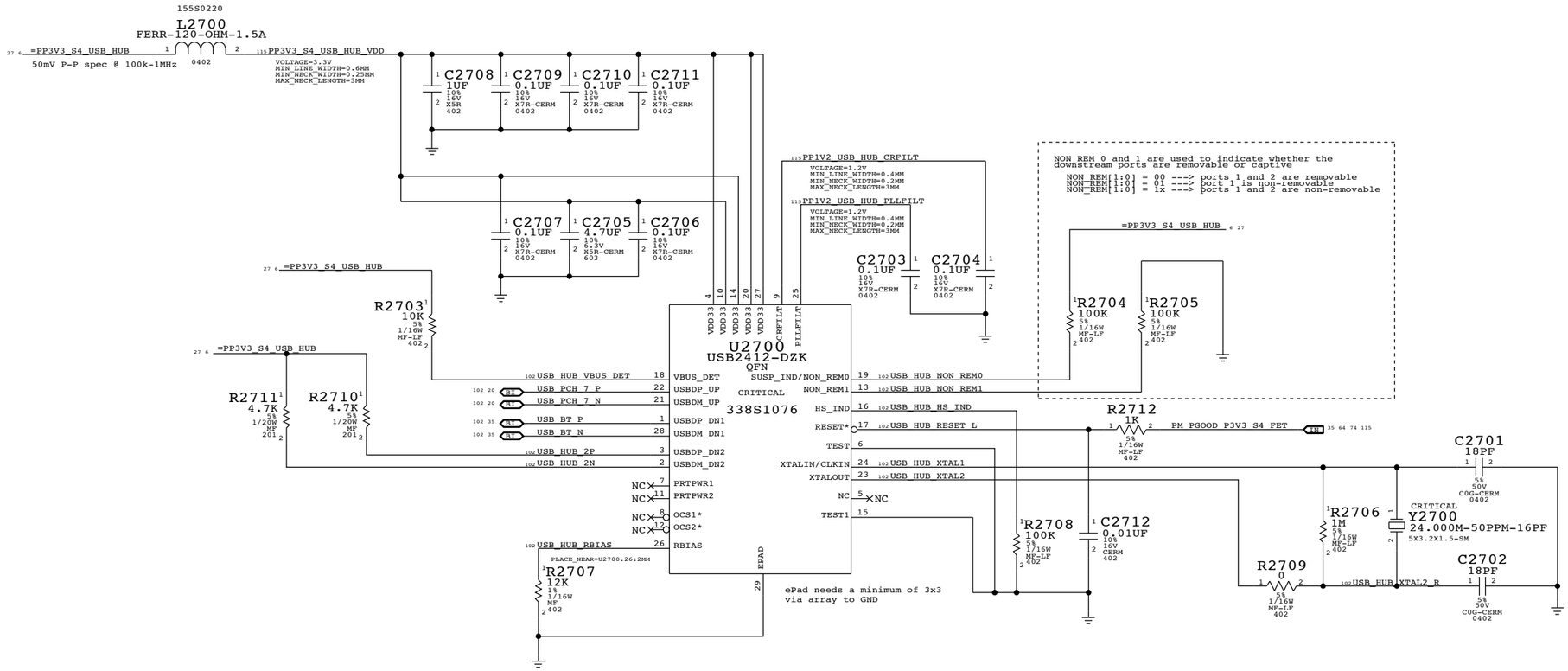

SYNC MASTER=D8 ROSITA SYNC DATE=03/23/2012

PAGE TITLE

USB 2.0 HUB (BT/SMC)

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DRAWING NUMBER 051-9504 SIZE D

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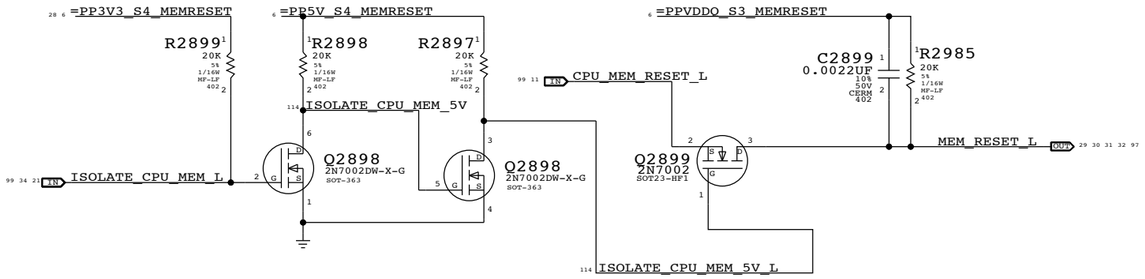
MEM_RESET_L Generator

The circuits below handle MEMVTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behaviour of signals.
WHEN HIGH: MEM_RESET_L NOT ISOLATED.
WHEN LOW: MEM_RESET_L IS ISOLATED.
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L (Block CPU from driving MEM_RESET_L in S3)

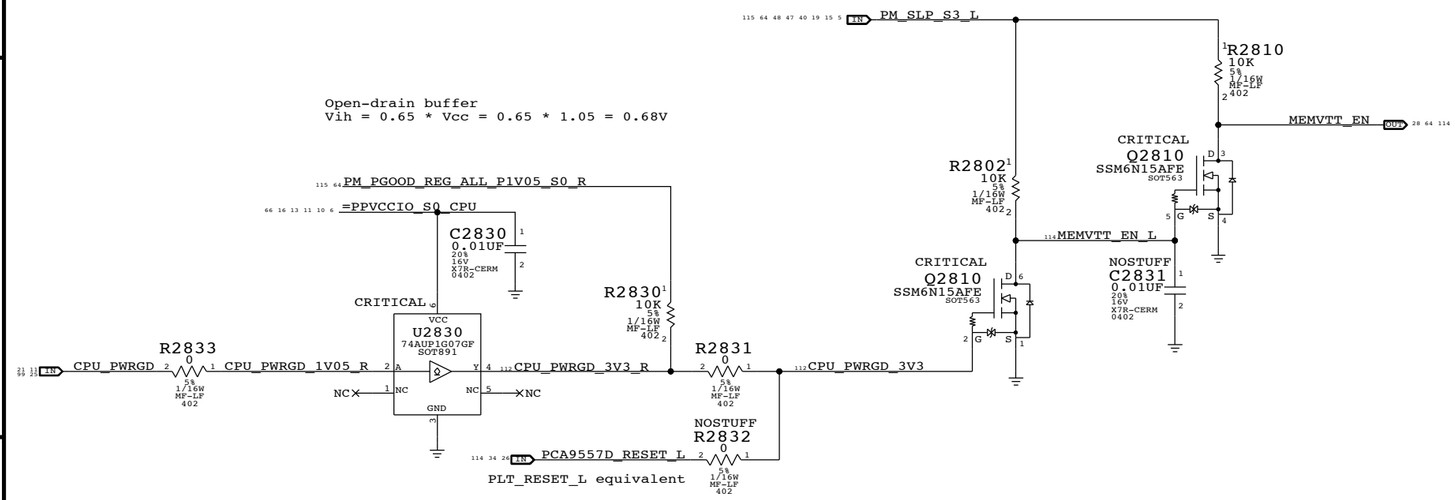


MEMVTT_EN Generator

rdar://11117167

Enables MEMVTT when PCH drives CPU PWRGD.

CPU does not drive MEM_CKE until VCCORE activated but CPU 1V5 (VDDQ) leaks into it.
Clamping MEMVTT will keep the MEM_CKE low until CPU actively controls it.
MEMVTT Clamp actively holds MEMVTT rail low until MEMVTT is enabled.
MEMVTT_EN = CPU_PWRGD * PM_SLP_S3_L (VTT is enabled when PCH tells CPU to enable VCCORE)



	Step	ISOLATE_CPU_MEM_L	PM_SLP_S3_L	CPU_PWRGD	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1
S3	2	0	1	1	1	1	1
	3	0	0	0	X	1	0
S3	4	0	0	0	X	1	0
to	5	0	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1
	7	1	1	1	CPU_MEM_RESET_L	1	1

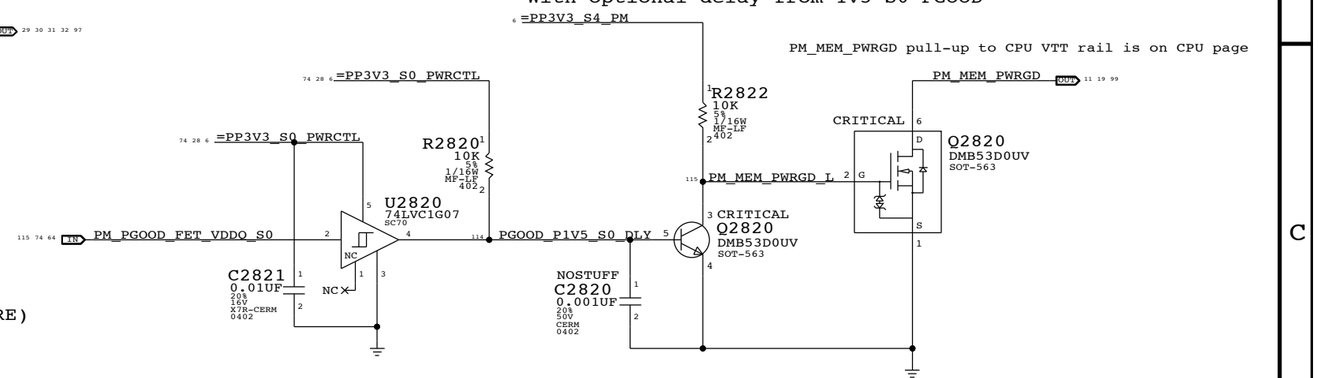
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: On a S5->S0 transition, ISOLATE_CPU_MEM_L will default low.
Rails will power-up as if from S3, but MEM_RESET_L now needs to be asserted in S0. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU

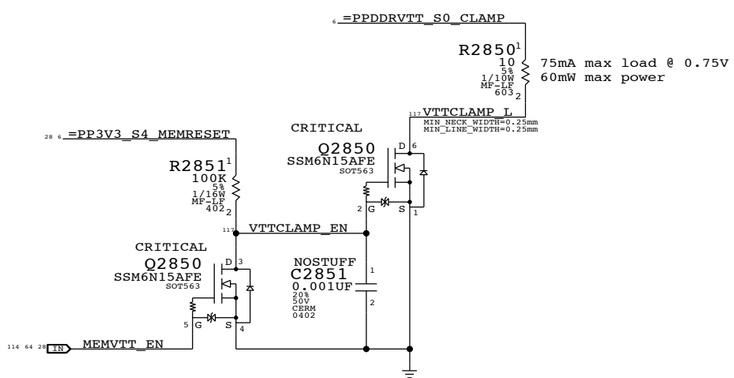
With optional delay from 1V5 S0 PGOOD

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3 and in S0 before CPU PWRGD



SYNC MASTER=D8 MARK	SYNC DATE=04/23/2012
PAGE TITLE	CPU Memory S3 Support
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	REVISION 7.0.0
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

=PPDDRVREF_DQ_MEM_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
	KEY		
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

MEM_A_DQ<0>, MEM_A_DQ<1>, MEM_A_DQ<2>, MEM_A_DQ<3>, MEM_A_DQ<8>, MEM_A_DQ<9>, MEM_A_DQS_N<1>, MEM_A_DQS_P<1>, MEM_A_DQ<10>, MEM_A_DQ<11>, MEM_A_DQ<16>, MEM_A_DQ<17>, MEM_A_DQS_N<2>, MEM_A_DQS_P<2>, MEM_A_DQ<18>, MEM_A_DQ<19>, MEM_A_DQ<24>, MEM_A_DQ<25>, MEM_A_DQ<26>, MEM_A_DQ<27>, MEM_A_CKE<0>, MEM_A_BA<2>, MEM_A_A<12>, MEM_A_A<9>, MEM_A_A<8>, MEM_A_A<5>, MEM_A_A<3>, MEM_A_A<1>, MEM_A_CLK_P<0>, MEM_A_CLK_N<0>, MEM_A_A<10>, MEM_A_BA<0>, MEM_A_WE_L, MEM_A_CAS_L, MEM_A_A<13>, MEM_A_CS_L<1>, MEM_A_DQ<32>, MEM_A_DQ<33>, MEM_A_DQS_N<4>, MEM_A_DQS_P<4>, MEM_A_DQ<34>, MEM_A_DQ<35>, MEM_A_DQ<40>, MEM_A_DQ<41>, MEM_A_DQ<42>, MEM_A_DQ<43>, MEM_A_DQ<48>, MEM_A_DQ<49>, MEM_A_DQS_N<6>, MEM_A_DQS_P<6>, MEM_A_DQ<50>, MEM_A_DQ<51>, MEM_A_DQ<56>, MEM_A_DQ<57>, MEM_A_DQ<58>, MEM_A_DQ<59>, MEM_DIMM0_SA<0>, =PP3V3_S0_MEM_A_SPD, MEM_DIMM0_SA<1>

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P/N: 516S1030

J2900 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 2 OF 2
205, 206, 207, 208, 209, MTG HOLE

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_A

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

=PPVDDQ_S3_MEM_A

=PPDDRVREF_CA_MEM_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

MEM_DIMM0_SA<1>
MEM_DIMM0_SA<0>
=PP3V3_S0_MEM_A_SPD

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_A

SYNC_MASTER=D8_KOSECOFF	SYNC_DATE=03/19/2013
PAGE TITLE	DDR3 SO-DIMM Connector A Slot0
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

P/N: 516S1030

J3000
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2
MTG HOLE 205 206 207 208 209

J3000
F-ANG-SM-2
SODIMM-P0.60-D8
SYM 1 OF 2

1	VREFDQ		2	VSS_0			
3	VSS_1		4	DQ4	=MEM_A_DQ<4>	BI	29 33
5	DQ0	=MEM_A_DQ<0>	6	DQ5	=MEM_A_DQ<5>	BI	29 33
7	DQ1	=MEM_A_DQ<1>	8	VSS_2			
9	VSS_3		10	DQS0*	=MEM_A_DQS_N<0>	BI	29 33
11	DM0		12	DQS0	=MEM_A_DQS_P<0>	BI	29 33
13	VSS_4		14	VSS_5			
15	DQ2	=MEM_A_DQ<2>	16	DQ6	=MEM_A_DQ<6>	BI	29 33
17	DQ3	=MEM_A_DQ<3>	18	DQ7	=MEM_A_DQ<7>	BI	29 33
19	VSS_6		20	VSS_7			
21	DQ8	=MEM_A_DQ<8>	22	DQ12	=MEM_A_DQ<12>	BI	29 33
23	DQ9	=MEM_A_DQ<9>	24	DQ13	=MEM_A_DQ<13>	BI	29 33
25	VSS_8		26	VSS_9			
27	DQS1*	=MEM_A_DQS_N<1>	28	DM1			
29	DQS1	=MEM_A_DQS_P<1>	30	RESET*	MEM_RESET_L	IN	28 29 31 32 97
31	VSS_10		32	VSS_11			
33	DQ10	=MEM_A_DQ<10>	34	DQ14	=MEM_A_DQ<14>	BI	29 33
35	DQ11	=MEM_A_DQ<11>	36	DQ15	=MEM_A_DQ<15>	BI	29 33
37	VSS_12		38	VSS_13			
39	DQ16	=MEM_A_DQ<16>	40	DQ20	=MEM_A_DQ<20>	BI	29 33
41	DQ17	=MEM_A_DQ<17>	42	DQ21	=MEM_A_DQ<21>	BI	29 33
43	VSS_14		44	VSS_15			
45	DQS2*	=MEM_A_DQS_N<2>	46	DM2			
47	DQS2	=MEM_A_DQS_P<2>	48	VSS_16			
49	VSS_17		50	DQ22	=MEM_A_DQ<22>	BI	29 33
51	DQ18	=MEM_A_DQ<18>	52	DQ23	=MEM_A_DQ<23>	BI	29 33
53	DQ19	=MEM_A_DQ<19>	54	VSS_18			
55	VSS_19		56	DQ28	=MEM_A_DQ<28>	BI	29 33
57	DQ24	=MEM_A_DQ<24>	58	DQ29	=MEM_A_DQ<29>	BI	29 33
59	DQ25	=MEM_A_DQ<25>	60	VSS_20			
61	VSS_21		62	DQS3*	=MEM_A_DQS_N<3>	BI	29 33
63	DM3		64	DQS3	=MEM_A_DQS_P<3>	BI	29 33
65	VSS_22		66	VSS_23			
67	DQ26	=MEM_A_DQ<26>	68	DQ30	=MEM_A_DQ<30>	BI	29 33
69	DQ27	=MEM_A_DQ<27>	70	DQ31	=MEM_A_DQ<31>	BI	29 33
71	VSS_24		72	VSS_25			
	KEY						
73	CKE0	MEM_A_CKE<2>	74	CKE1	MEM_A_CKE<3>	IN	12 97
75	VDD_0		76	VDD_1			
77	NC_0	NCX	78	A15	MEM_A_A<15>	IN	12 29 97
79	BA2	MEM_A_BA<2>	80	A14	MEM_A_A<14>	IN	12 29 97
81	VDD_2		82	VDD_3			
83	A12/BC*	MEM_A_A<12>	84	A11	MEM_A_A<11>	IN	12 29 97
85	A9	MEM_A_A<9>	86	A7	MEM_A_A<7>	IN	12 29 97
87	VDD_4		88	VDD_5			
89	A8	MEM_A_A<8>	90	A6	MEM_A_A<6>	IN	12 29 97
91	A5	MEM_A_A<5>	92	A4	MEM_A_A<4>	IN	12 29 97
93	VDD_6		94	VDD_7			
95	A3	MEM_A_A<3>	96	A2	MEM_A_A<2>	IN	12 29 97
97	A1	MEM_A_A<1>	98	A0	MEM_A_A<0>	IN	12 29 97
99	VDD_8		100	VDD_9			
101	CK0	MEM_A_CLK_P<2>	102	CK1	MEM_A_CLK_P<3>	IN	12 97
103	CK0*	MEM_A_CLK_N<2>	104	CK1*	MEM_A_CLK_N<3>	IN	12 97
105	VDD_10		106	VDD_11			
107	A10_AP	MEM_A_A<10>	108	BA1	MEM_A_BA<1>	IN	12 29 97
109	BA0	MEM_A_BA<0>	110	RAS*	MEM_A_RAS_L	IN	12 29 97
111	VDD_12		112	VDD_13			
113	WE*	MEM_A_WE_L	114	S0*	MEM_A_CS_L<2>	IN	12 97
115	CAS*	MEM_A_CAS_L	116	ODT0	MEM_A_ODT<2>	IN	12 97
117	VDD_14		118	VDD_15			
119	A13	MEM_A_A<13>	120	ODT1	MEM_A_ODT<3>	IN	12 97
121	S1*	MEM_A_CS_L<3>	122	NC_1	NCX		
123	VDD_16		124	VDD_17			
125	TEST	NCX	126	VREFCA	=PPDDRVREF_CA_MEM_A		6 29
127	VSS_26		128	VSS_27			
129	DQ32	=MEM_A_DQ<32>	130	DQ36	=MEM_A_DQ<36>	BI	29 33
131	DQ33	=MEM_A_DQ<33>	132	DQ37	=MEM_A_DQ<37>	BI	29 33
133	VSS_28		134	VSS_29			
135	DQS4*	=MEM_A_DQS_N<4>	136	DM4			
137	DQS4	=MEM_A_DQS_P<4>	138	VSS_30			
139	VSS_31		140	DQ38	=MEM_A_DQ<38>	BI	29 33
141	DQ34	=MEM_A_DQ<34>	142	DQ39	=MEM_A_DQ<39>	BI	29 33
143	DQ35	=MEM_A_DQ<35>	144	VSS_32			
145	VSS_33		146	DQ44	=MEM_A_DQ<44>	BI	29 33
147	DQ40	=MEM_A_DQ<40>	148	DQ45	=MEM_A_DQ<45>	BI	29 33
149	DQ41	=MEM_A_DQ<41>	150	VSS_34			
151	VSS_35		152	DQS5*	=MEM_A_DQS_N<5>	BI	29 33
153	DM5		154	DQS5	=MEM_A_DQS_P<5>	BI	29 33
155	VSS_36		156	VSS_37			
157	DQ42	=MEM_A_DQ<42>	158	DQ46	=MEM_A_DQ<46>	BI	29 33
159	DQ43	=MEM_A_DQ<43>	160	DQ47	=MEM_A_DQ<47>	BI	29 33
161	VSS_38		162	VSS_39			
163	DQ48	=MEM_A_DQ<48>	164	DQ52	=MEM_A_DQ<52>	BI	29 33
165	DQ49	=MEM_A_DQ<49>	166	DQ53	=MEM_A_DQ<53>	BI	29 33
167	VSS_40		168	VSS_41			
169	DQS6*	=MEM_A_DQS_N<6>	170	DM6			
171	DQS6	=MEM_A_DQS_P<6>	172	VSS_42			
173	VSS_43		174	DQ54	=MEM_A_DQ<54>	BI	29 33
175	DQ50	=MEM_A_DQ<50>	176	DQ55	=MEM_A_DQ<55>	BI	29 33
177	DQ51	=MEM_A_DQ<51>	178	VSS_44			
179	VSS_45		180	DQ60	=MEM_A_DQ<60>	BI	29 33
181	DQ56	=MEM_A_DQ<56>	182	DQ61	=MEM_A_DQ<61>	BI	29 33
183	DQ57	=MEM_A_DQ<57>	184	VSS_46			
185	VSS_47		186	DQS7*	=MEM_A_DQS_N<7>	BI	29 33
187	DM7		188	DQS7	=MEM_A_DQS_P<7>	BI	29 33
189	VSS_48		190	VSS_49			
191	DQ58	=MEM_A_DQ<58>	192	DQ62	=MEM_A_DQ<62>	BI	29 33
193	DQ59	=MEM_A_DQ<59>	194	DQ63	=MEM_A_DQ<63>	BI	29 33
195	VSS_50		196	VSS_51			
197	SA0	MEM_DIMM1_SA<0>	198	EVENT*	MEM_EVENT_L	OUTPD	29 31 32 47 48 114
199	VDDSPD	=PP3V3_S0_MEM_A_SPD	200	SDA	=I2C_SODIMMA_SDA	BI	29 30
201	SA1	MEM_DIMM1_SA<1>	202	SCL	=I2C_SODIMMA_SCL	IN	29 50
203	VTT_0		204	VTT_1			

=PPVDDQ_S3_MEM_A 6 29 30

=PPDDRVTT_S0_MEM_A 6 29 30

=PPDDRVREF_DQ_MEM_A 6 29

=PP3V3_S0_MEM_A_SPD 6 29 30

MEM_DIMM1_SA<0> 30

MEM_DIMM1_SA<1> 30

C3000	10UF	20%	6.3V	X5R	603				
C3001	10UF	20%	6.3V	X5R	603				
C3010	0.1UF	20%	10V	CERM	402				
C3011	0.1UF	20%	10V	CERM	402				
C3012	0.1UF	20%	10V	CERM	402				
C3013	0.1UF	20%	10V	CERM	402				
C3014	0.1UF	20%	10V	CERM	402				
C3015	0.1UF	20%	10V	CERM	402				
C3016	0.1UF	20%	10V	CERM	402				
C3017	0.1UF	20%	10V	CERM	402				
C3018	0.1UF	20%	10V	CERM	402				
C3019	0.1UF	20%	10V	CERM	402				
C3020	0.1UF	20%	10V	CERM	402				
C3021	0.1UF	20%	10V	CERM	402				
C3022	0.1UF	20%	10V	CERM	402				
C3023	0.1UF	20%	10V	CERM	402				
C3030	2.2UF	20%	6.3V	CERM	402-LF				
C3031	0.1UF	20%	10V	CERM	402				
C3035	2.2UF	20%	6.3V	CERM	402-LF				
C3036	0.1UF	20%	10V	CERM	402				
C3040	2.2UF	20%	6.3V	CERM	402-LF				
C3050	1UF	10%	10V	X5R	402				
C3051	1UF	10%	10V	X5R	402				
C3052	1UF	10%	10V	X5R	402				
C3053	1UF	10%	10V	X5R	402				
R3040	10K	5%	1/16W	MF-LF	402				
R3041	10K	5%	1/16W	MF-LF	402				

SYNC_MASTER=D8_KOSECOFF SYNC_DATE=03/19/2012

PAGE TITLE
DDR3 SO-DIMM Connector A Slot1

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

=PPDDRVREF_DQ_MEM_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 1 OF 2

J3100
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
	KEY		
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	XNC	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD

R3141 10K 5% 1/16W MF-LF 402
R3140 10K 5% 1/16W MF-LF 402
C3140 2.2UF 20% 6.3V CERM 402-LF

MEM_DIMM2_SA<1>
MEM_DIMM2_SA<0>

=PPDDRVTT_S0_MEM_B

C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

=PPDDRVREF_CA_MEM_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

SYNC_MASTER=D8_KOSECOFF SYNC_DATE=03/19/2012

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B SLOT0

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D
REVISION: 7.0.0
BRANCH: prefsb
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

=PPDDRVREF_DQ_MEM_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
	KEY		
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
NCX 77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1 XNC	122
123	VDD_16	VDD_17	124
NC 125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0		204

SODIMM-P0.60-D8

J3200 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B

C3210 C3211 C3212 C3213 C3214 C3215 C3216 C3217 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3218 C3219 C3220 C3221 C3222 C3223 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD

R3241 10K 5% 1/16W MF-LF 402
R3240 10K 5% 1/16W MF-LF 402

MEM_DIMM3_SA<1>
MEM_DIMM3_SA<0>
=PP3V3_S0_MEM_B_SPD

C3240 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVTT_S0_MEM_B

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

C3250 C3251 C3252 C3253 1UF 10% 10V X5R 402

SYNC MASTER=D8 KOSECOFF	SYNC DATE=03/19/2012
PAGE TITLE: DDR3 SO-DIMM CONNECTOR B SLOT1	
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MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	
MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	
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MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	
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MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	
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MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	
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MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	
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MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	
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MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	
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MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	
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MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	
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MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	
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MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	

SYNC_MASTER=D8_KOSECOFF SYNC_DATE=03/19/2012

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

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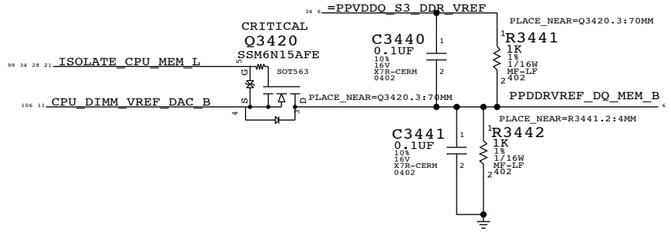
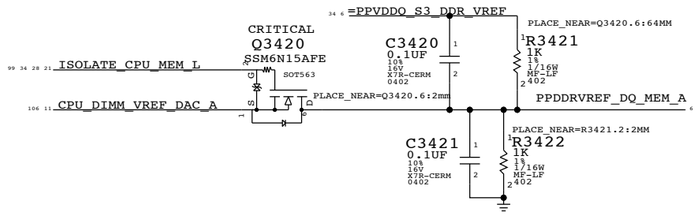
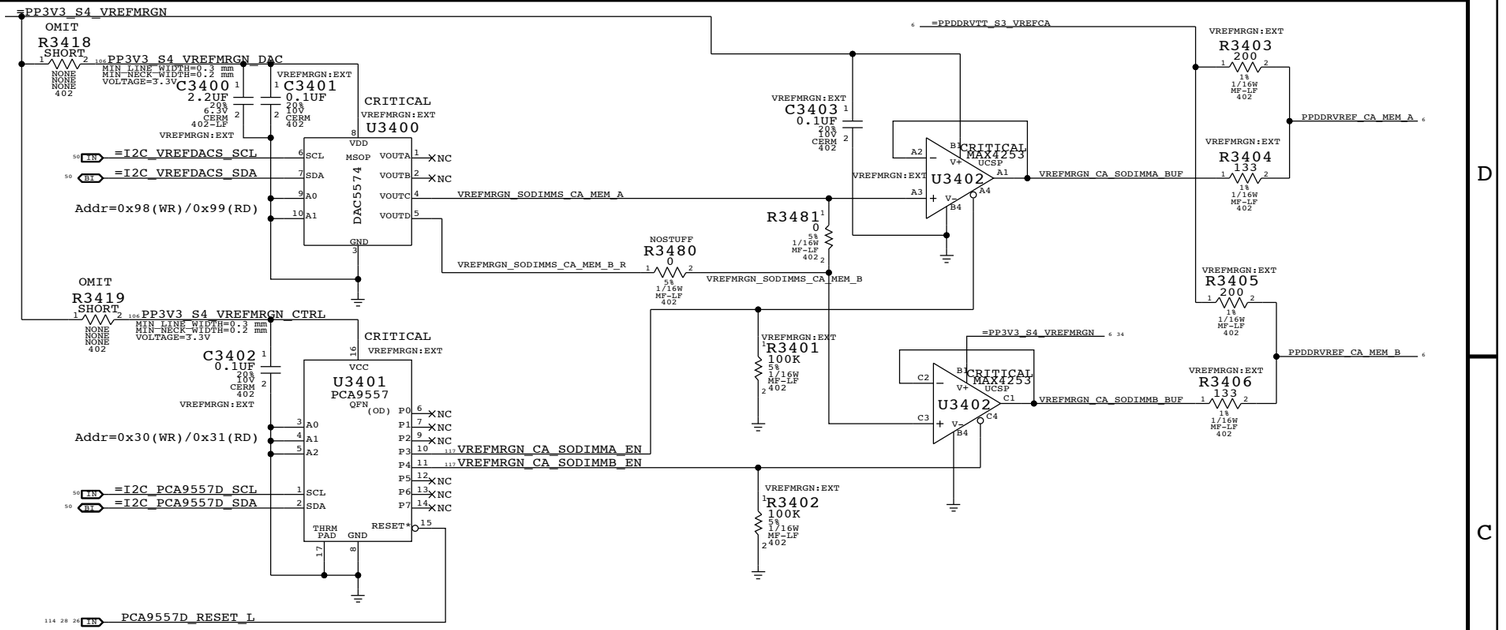
VRef DQ

Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step







RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FLM,0,5%,402,SM,LF	R3403,R3405		VREFMRGN:N

	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	C	C	D	D
PCA9557D Pin:	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=D8_KOSECOFF SYNC_DATE=03/19/2012

PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

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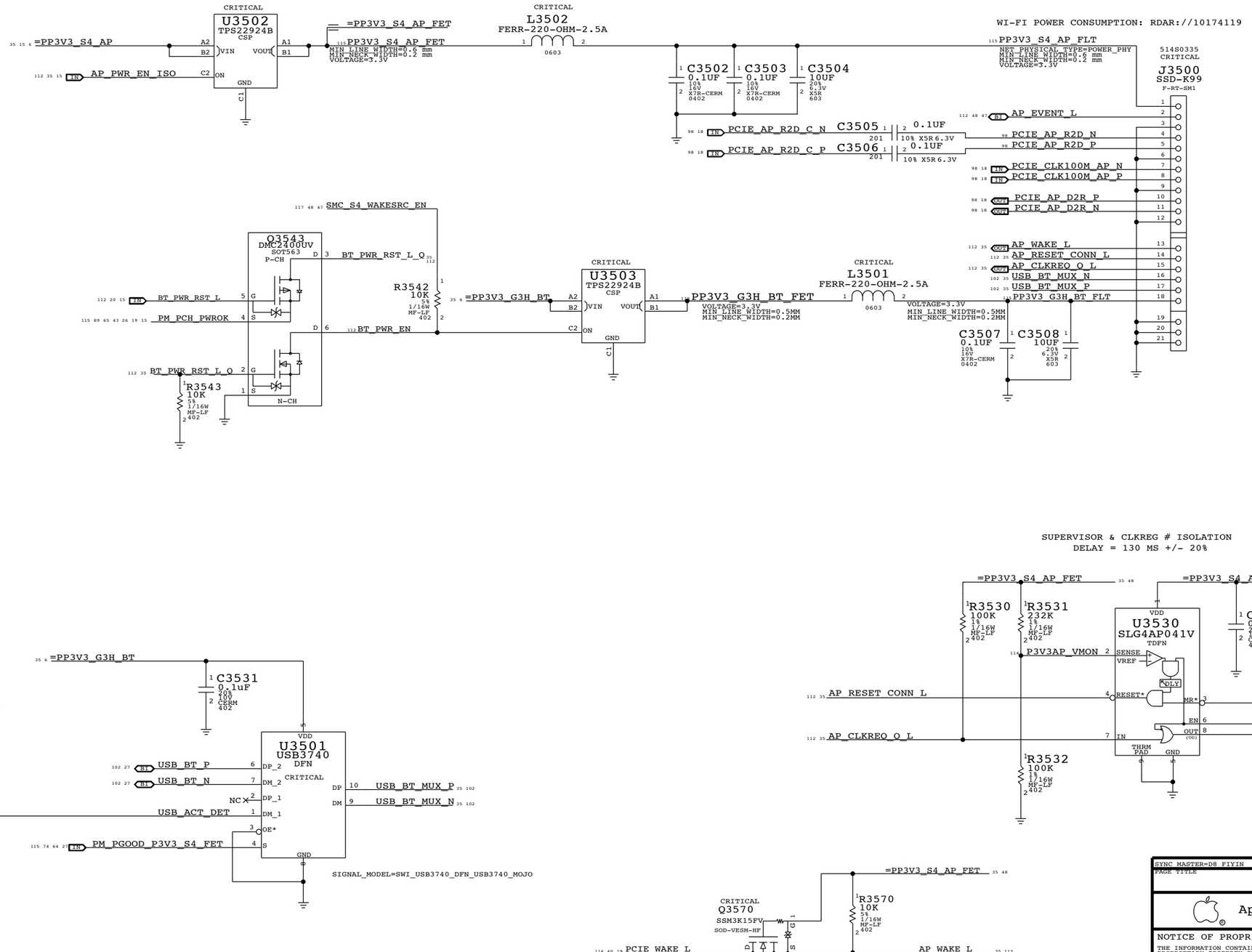
AIRPORT BLUETOOTH



SYNC MASTER=D8_FIYIN SYNC DATE=07/02/2012

PAGE TITLE

AIRPORT/BT

Apple Inc.

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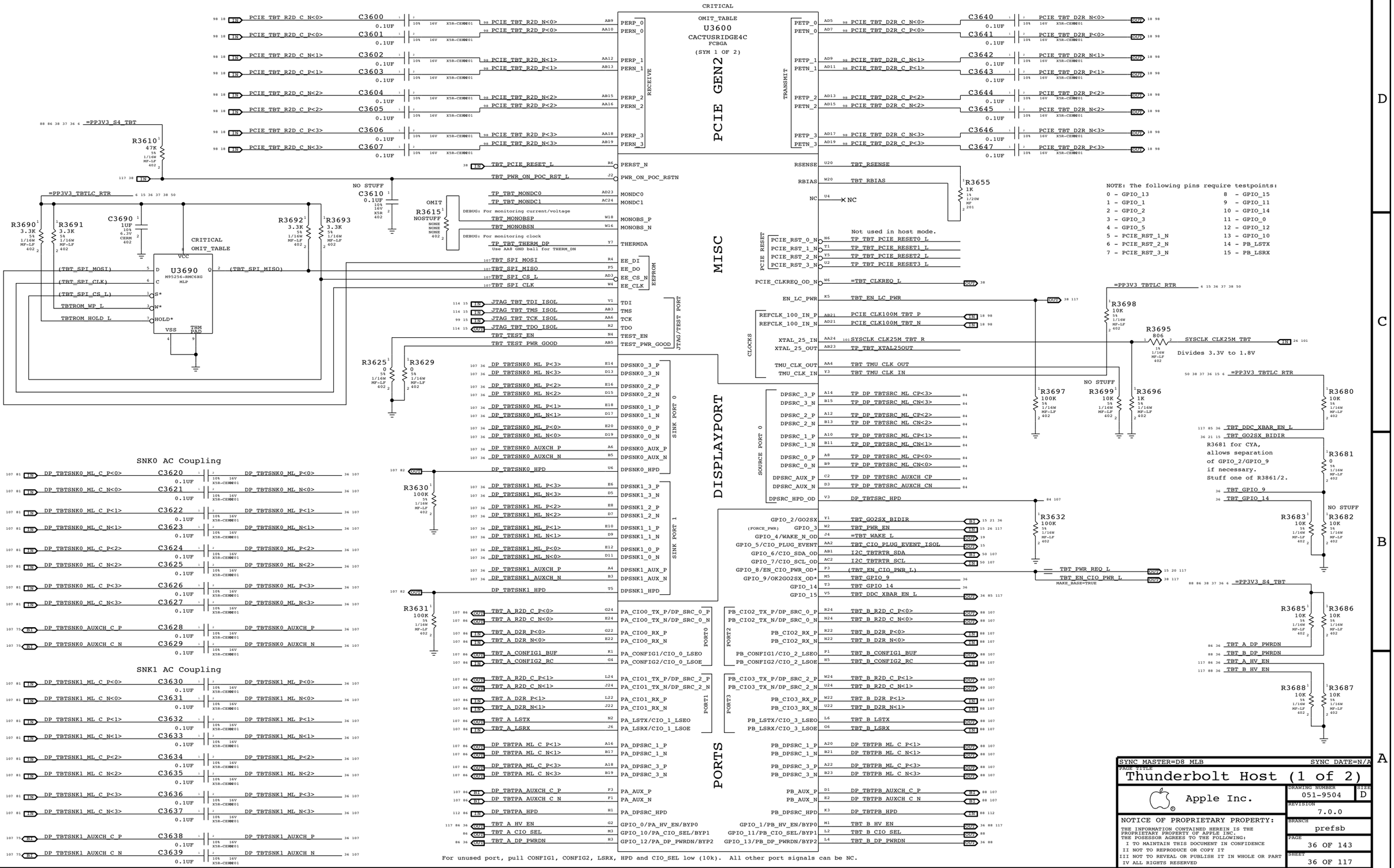

SYNC_MASTER=D8 MLB SYNC_DATE=N/A

PAGE TITLE

Thunderbolt Host (1 of 2)

Apple Inc.

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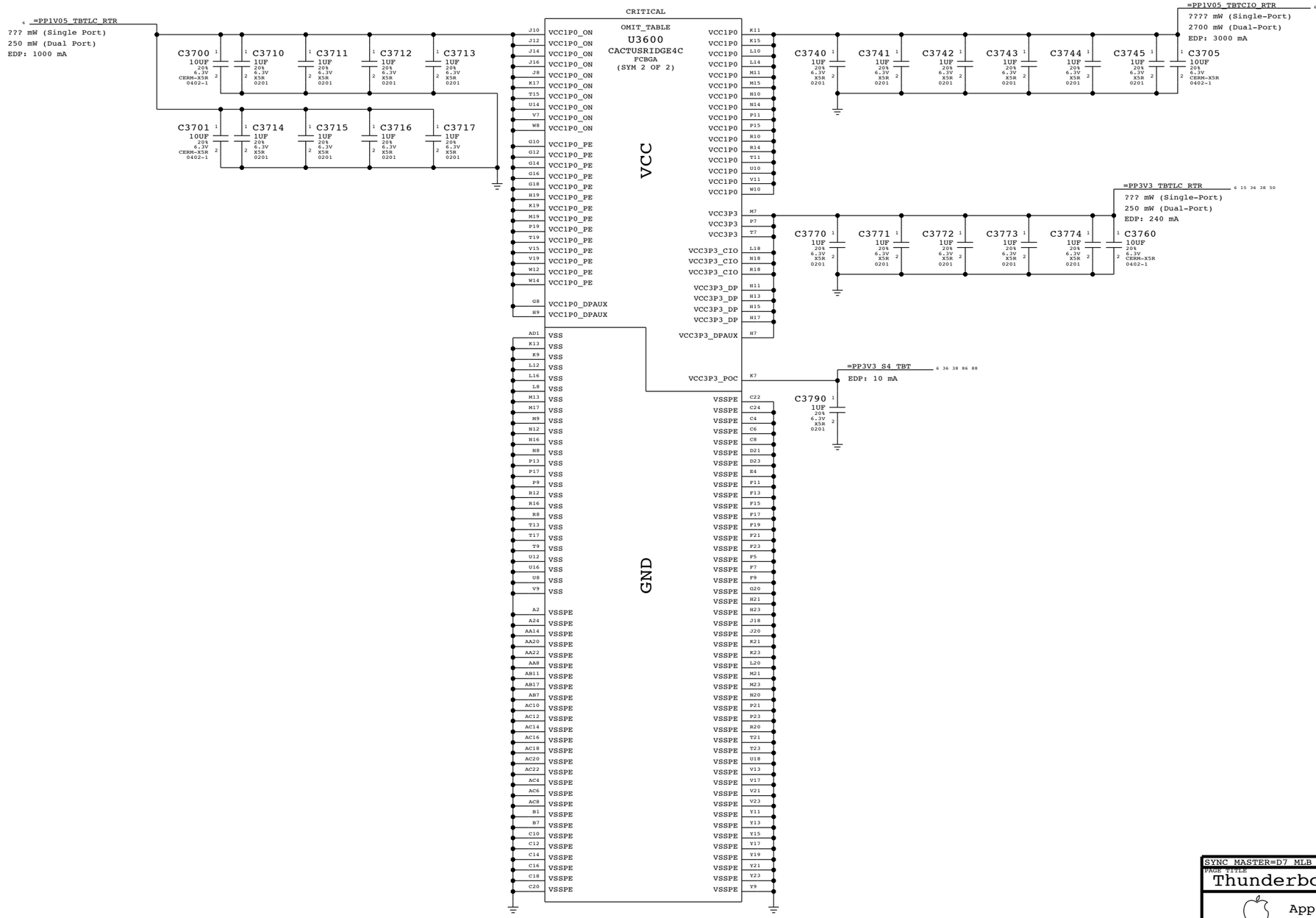

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=D7_MLB SYNC_DATE=03/15/2012

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

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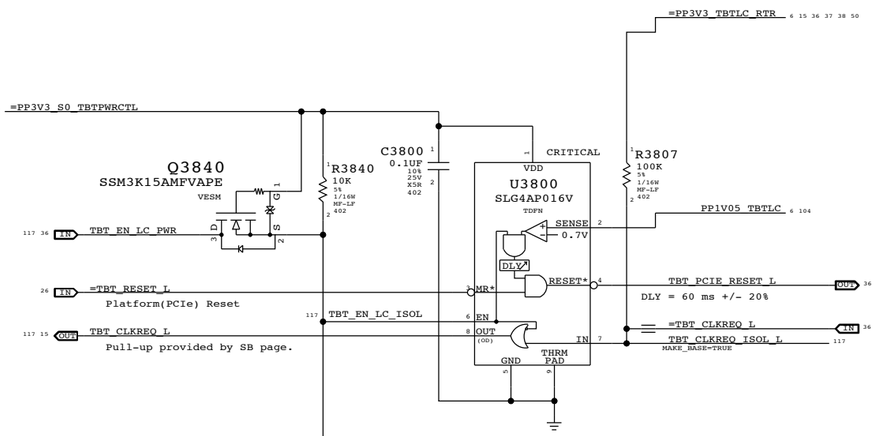
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

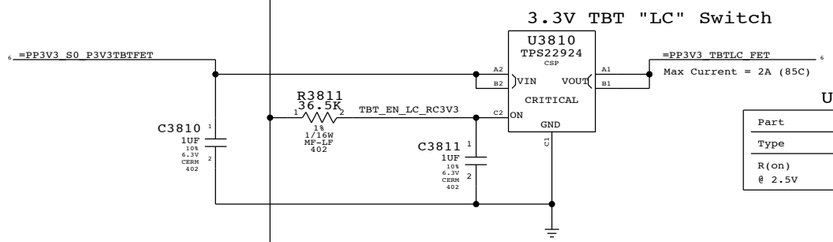
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation



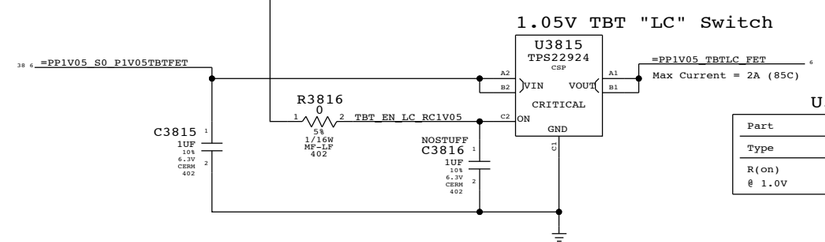
3.3V TBT "LC" Switch



U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

1.05V TBT "LC" Switch

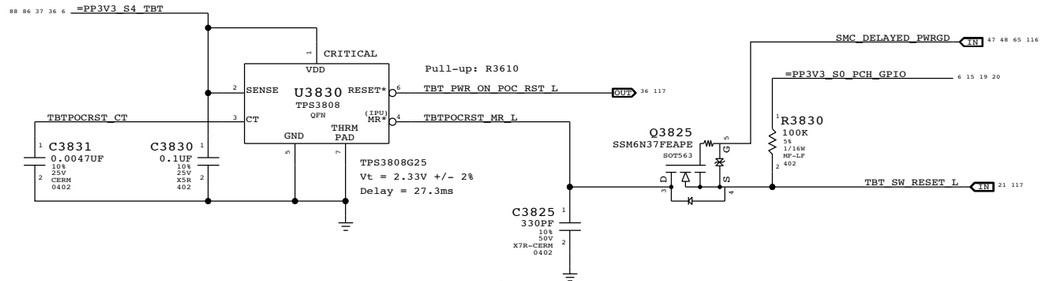


U3815

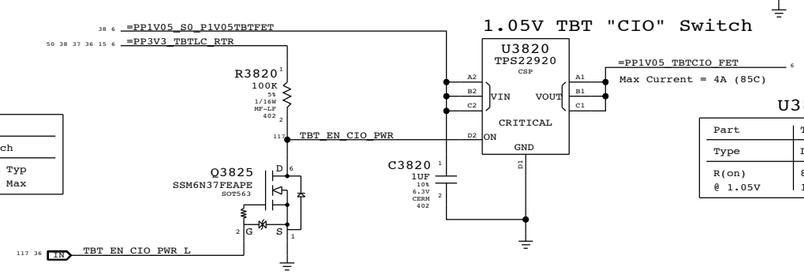
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=D7_MLB SYNC_DATE=03/15/2012

PAGE TITLE
Thunderbolt Power Support

Apple Inc.

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_S4_ENET_FET
281mA (1000base-T max power, Caesar IV)

R3901 0 5% 1/16W MF-LF 402

=PP3V3_S4_ENET_FET_SRVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3979 4.7UF 20% 6.3V X5R-CERM1 402
C3996 0.1UF 10% 16V X5R-CERM 0201
C3997 0.1UF 10% 16V X5R-CERM 0201

=PP3V3R1V8_CR_IOPWR_OUT
VDD for Card Reader I/O

CRITICAL
L3900 FERR-600-OHM-300MA-0.85OHM 0402
=PP3V3_S4_ENET_FET_XTALVDDH
C3900 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3905 FERR-600-OHM-300MA-0.85OHM 0402
=PP3V3_S4_ENET_FET_BIASVDDH
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3910 FERR-600-OHM-300MA-0.85OHM 0402
=PP3V3_S4_ENET_FET_AVDDH
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201
C3912 1.0UF 10% 6.3V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3999 0.1UF 10% 16V X5R-CERM 0201
C3998 0.1UF 10% 16V X5R-CERM 0201
C3916 0.1UF 10% 16V X5R-CERM 0201

=PP3V3_S0_ENET
Current Limiting Resistor
R3942 1K 5% 1/16W MF-LF 402

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
=ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT → VMAIN_PRSNT (IPD-ENET)
PCIE_ENET_D2R_C_N → PCIE_TXD_N
PCIE_ENET_D2R_C_P → PCIE_TXD_P
PCIE_ENET_R2D_P → PCIE_RXD_P
PCIE_ENET_R2D_N → PCIE_RXD_N
PCIE_CLK100M_ENET_P → PCIE_REFCLK_P
PCIE_CLK100M_ENET_N → PCIE_REFCLK_N
ENET_RESET_L → PERST* (IPD)
ENET_CLKREQ_L_O → CLKREQ* (OD)
WAKE* (OD)
ENET_LOW_PWR → LOW_PWR (IPD)
SMB_ENET_SCL → SMB_CLK
SMB_ENET_SDA → SMD_DATA (IPD-ENETM)
ENET_SCLK → SCLK
ENET_MISO → SI/LINKLED*
ENET_MOSI → SO
ENET_CS_L → CS*
TP_ENET_CR_3V3_EN_L → SPD100LED*/SERIAL_DO (OD)
ENET_TRAFFICLED_L → TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET → XTALI
NC → XTALO
ENET_RDAC → RDAC

R3965 1.24K 1% 1/16W MF-LF 402

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_S4_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL
L3920 FERR-600-OHM-300MA-0.85OHM 0402
=PP1V2_S4_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402
C3913 1.0UF 10% 6.3V X5R-CERM 0201

CRITICAL
L3925 FERR-600-OHM-0.5A SM
=PP1V2_S4_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
L3930 FERR-600-OHM-300MA-0.85OHM 0402
=PP1V2_S4_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE
U3900
BCM57765
QFN-8X8

AVDDH, BIASVDDH, XTALVDDH, VDDO, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

TRD0_P ENETCONN_MDI_P<0>
TRD0_N ENETCONN_MDI_N<0>
TRD1_P ENETCONN_MDI_P<1>
TRD1_N ENETCONN_MDI_N<1>
TRD2_P ENETCONN_MDI_P<2>
TRD2_N ENETCONN_MDI_N<2>
TRD3_P ENETCONN_MDI_P<3>
TRD3_N ENETCONN_MDI_N<3>

GPIO_0 TP_ENET_CR_1V8_EN
GPIO_1/CR_BUS_PWR PP3V3R1V8_ENET_LR_OUT_REG
RE*/GPIO_2 ENET_MEDIA_SENSE

MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3R1V8_CR_IOPWR_OUT

NOTE: "IPx" == Programmable pull-up/down

(IPx-ENETM) SD_DETECT/WE* → ENET_SD_DETECT_L
SD_DETECT can only be used active low due to errata.
(IPU-ENET) CR_CMD/CLE → ENET_SD_CMD R3961 33 5% 1/20W MF 201 SDCONN_CMD
CR_CLK/RY_BY* → ENET_SD_CLK R3979 33 5% 1/20W MF 201 SDCONN_CLK
(IPU-ENET) CR_DATA0 → ENET_CR_DATA<0> R3971 33 5% 1/20W MF 201 SDCONN_DATA<0>
CR_DATA1 → ENET_CR_DATA<1> R3972 33 5% 1/20W MF 201 SDCONN_DATA<1>
CR_DATA2 → ENET_CR_DATA<2> R3973 33 5% 1/20W MF 201 SDCONN_DATA<2>
CR_DATA3 → ENET_CR_DATA<3> R3974 33 5% 1/20W MF 201 SDCONN_DATA<3>
CR_DATA4 → ENET_CR_DATA<4> R3975 33 5% 1/20W MF 201 SDCONN_DATA<4>
CR_DATA5 → ENET_CR_DATA<5> R3976 33 5% 1/20W MF 201 SDCONN_DATA<5>
CR_DATA6 → ENET_CR_DATA<6> R3977 33 5% 1/20W MF 201 SDCONN_DATA<6>
CR_DATA7 → ENET_CR_DATA<7> R3978 33 5% 1/20W MF 201 SDCONN_DATA<7>

(IPU-ENET) CE*/MS_INS* → NC_ENET_CE_L_MS_INS_L NO_TEST=TRUE
No MS (Memory Stick) Insert feature needed.
(IPU-ENET) CR_LED/ALE → ENET_CR_PWREN
Control signal to light LED or control SD bus power.
(IPU-ENET) CR_WP*/XD_WP* → SDCONN_WP
XD_DETECT → ENET_SR_DISABLE R3981 1K 5% 1/16W MF-LF 402
(NO IPU OR IPD-ENET) THRM_PAD 69

ENET supports both active-levels for WP.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
IF ENET SWITCHING REGULATOR IS USED, THIS PIN SHOULD HAVE A 1K PD TO GND

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_S4_ENET_FET
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
ENET_SCLK → SCK
ENET_CS_L → CS*
WP*
RESET*
SI → ENET_MOSI
SO → ENET_MISO
GND
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
NOSTUFF R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC MASTER=D8_FIYIN
SYNC DATE=07/02/2012
PAGE TITLE
ETHERNET PHY (CAESAR IV+)

Apple Inc.

DRAWING NUMBER 051-9504
SIZE D
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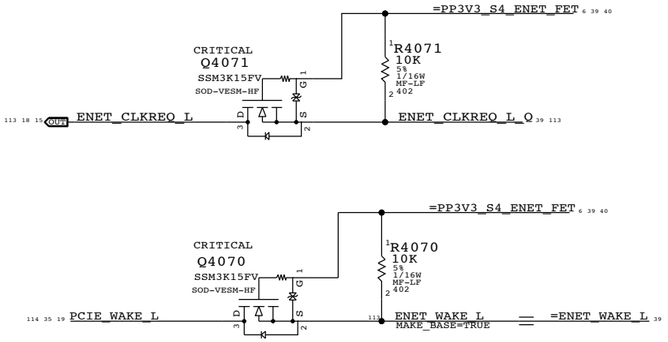
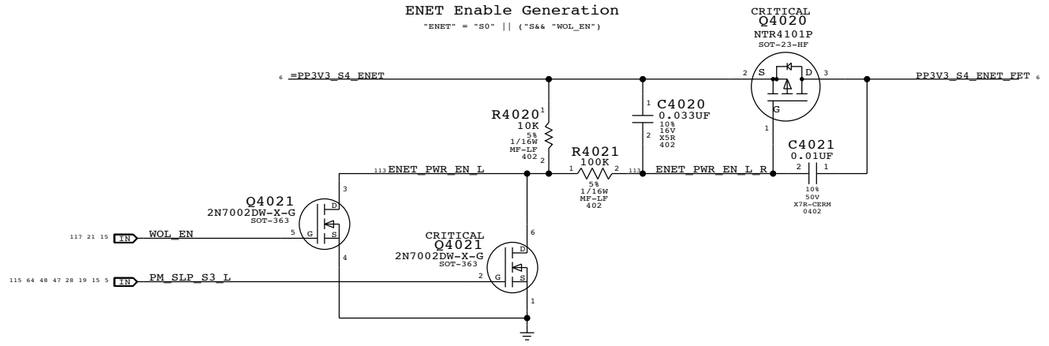
CAESAR IV WAKE# ISOLATION



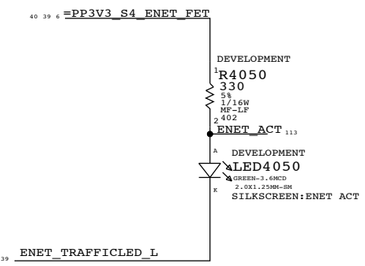
ENET Enable Generation

"ENET" = "S0" || ("S&& "WOL_EN")

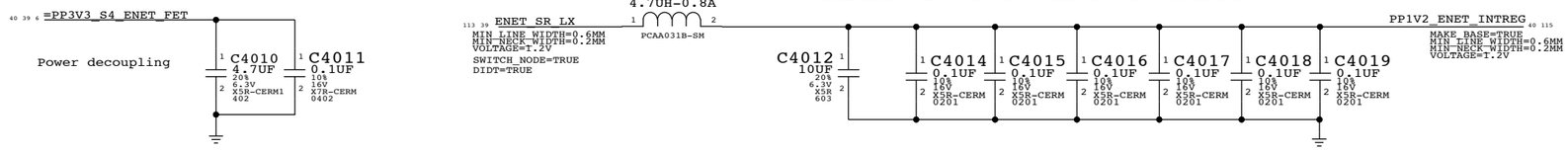
3.3V ENET FET



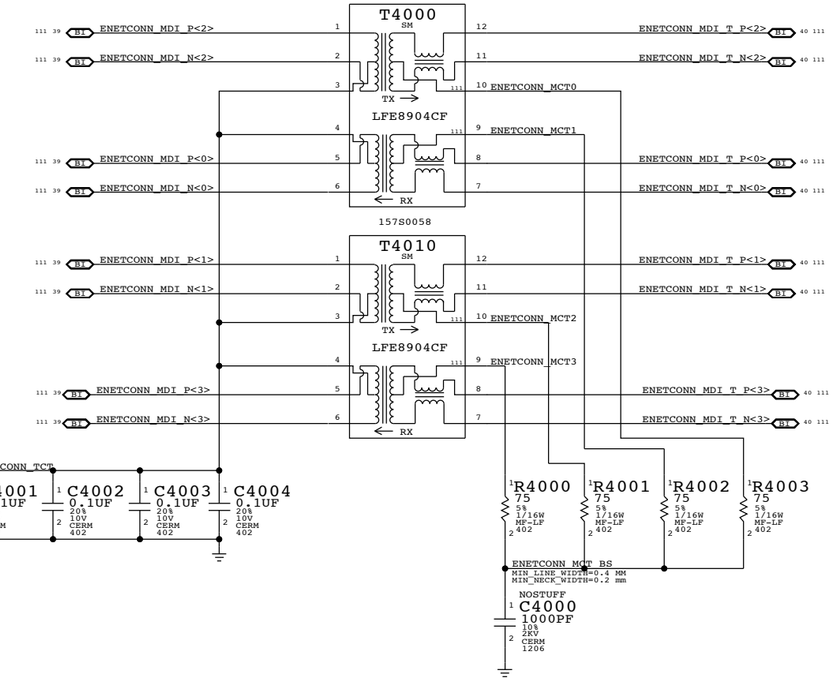
CAESAR IV ACTIVITY LED



CAESAR IV 1.2V INT.VR CMPTS

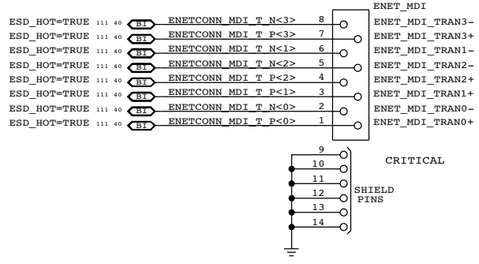


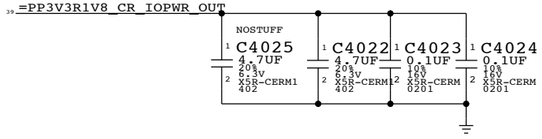
Feedback loop



J4000

RCPT-RJ45-D8
F-ANG-TH





SYNC_MASTER=D8_FIYIN SYNC_DATE=07/02/2012

PAGE TITLE: Ethernet Support & Connector

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

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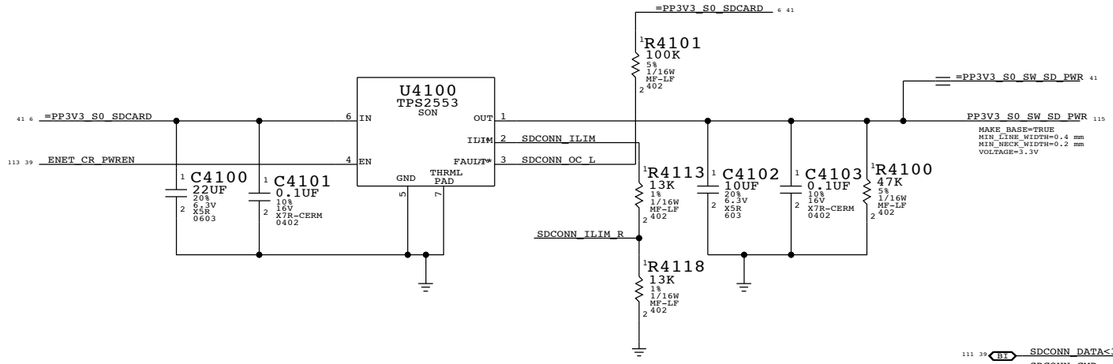
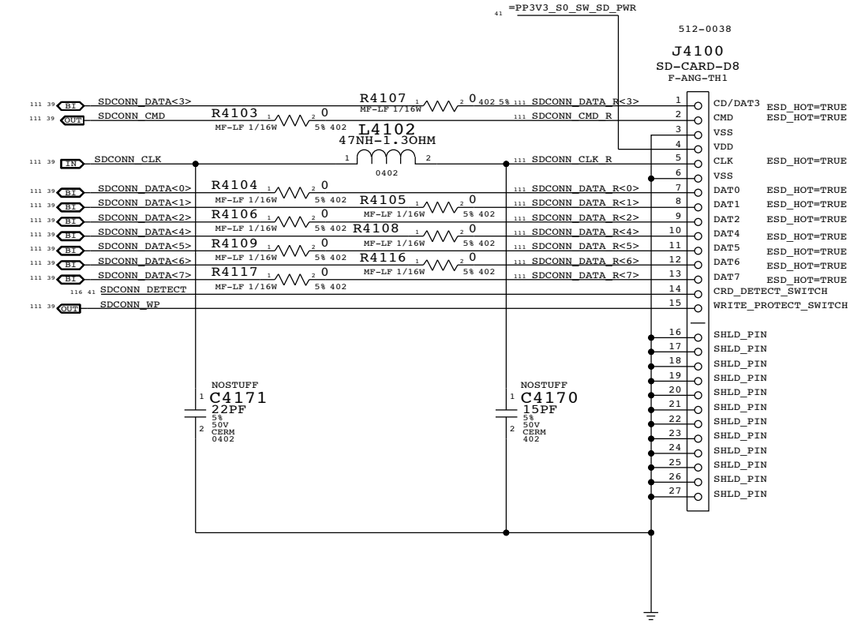
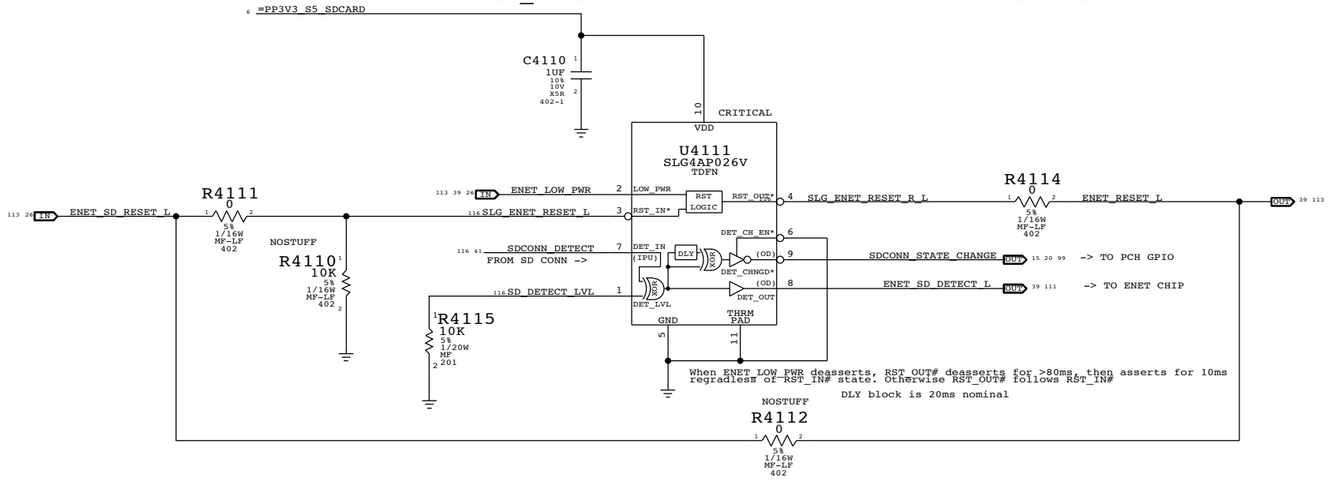
SD CARD 3.3V OVERCURRENT PROTECTION





SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=D8_FIYIN SYNC_DATE=07/02/2012

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

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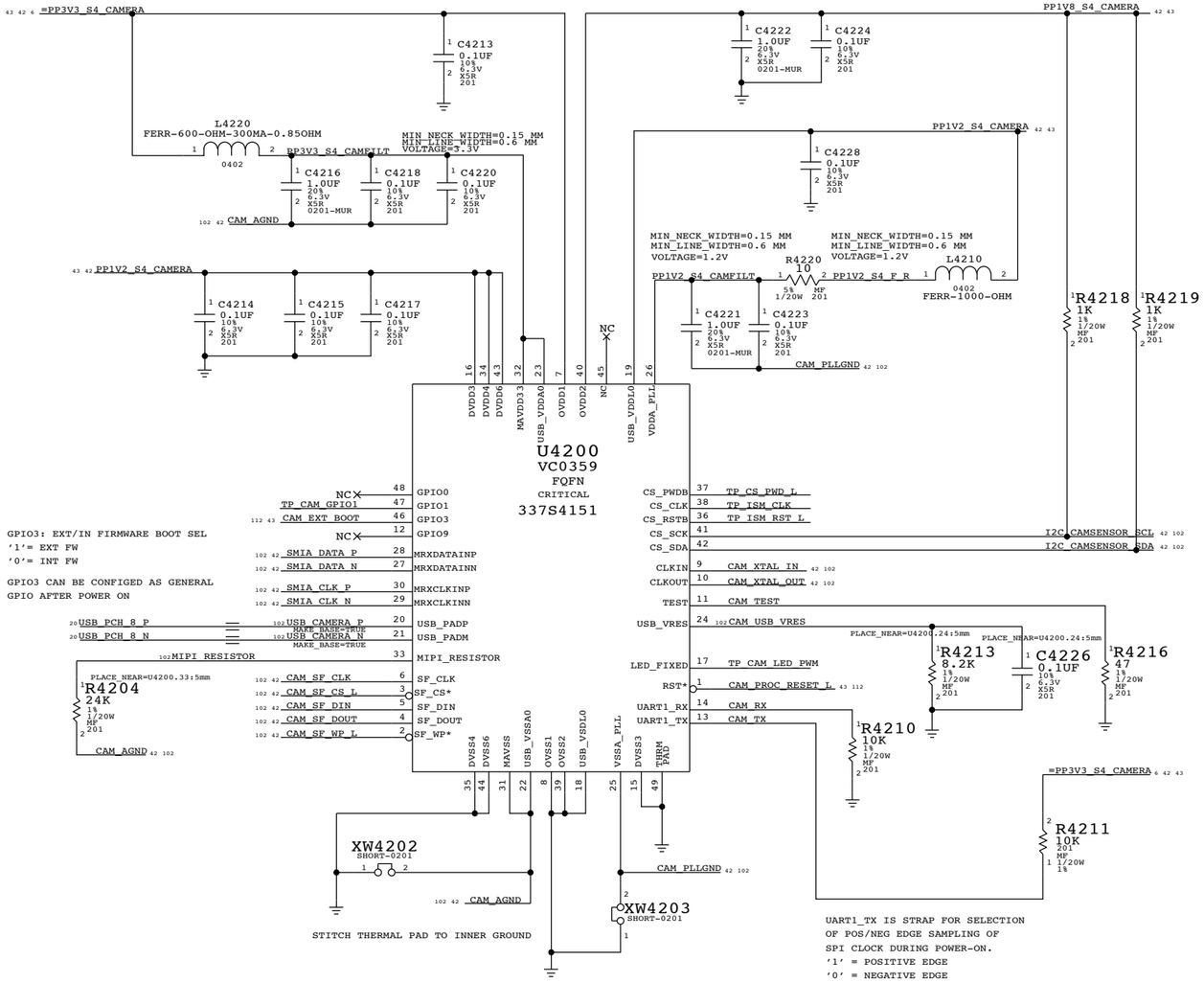
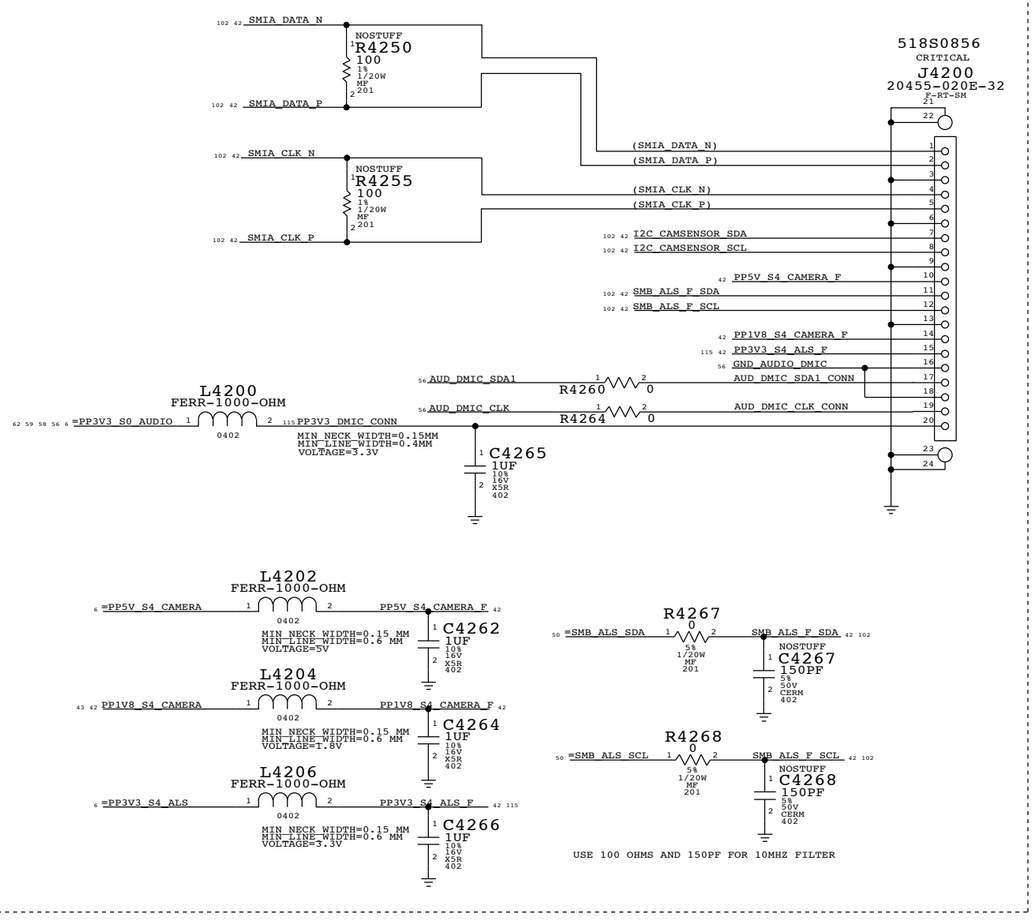
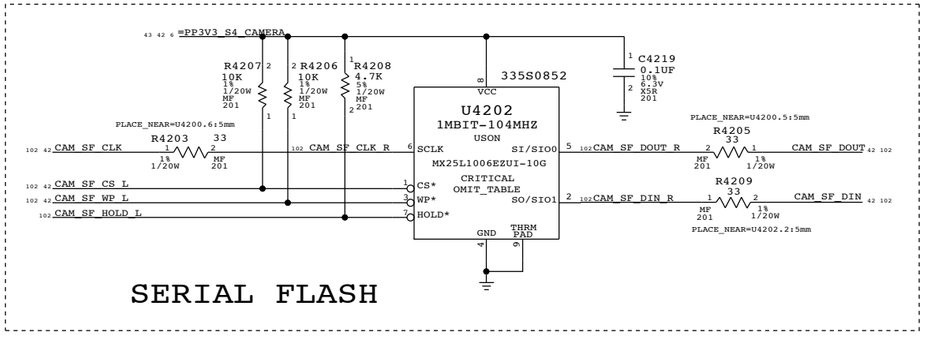
USB CAMERA CONTROLLER



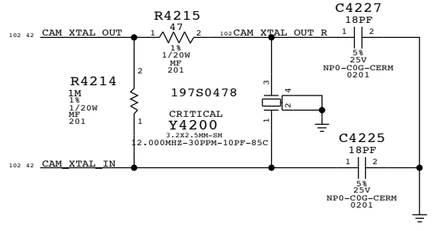
CAMERA/ALS/DMIC CONNECTOR





SERIAL FLASH

CRYSTAL



SYNC_MASTER=D8 ROSITA SYNC_DATE=03/23/2012

PAGE TITLE: Camera Controller

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

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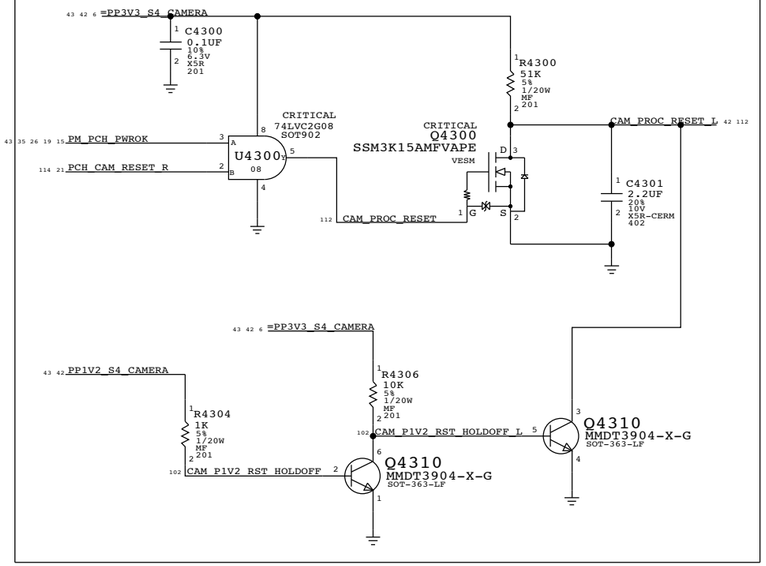
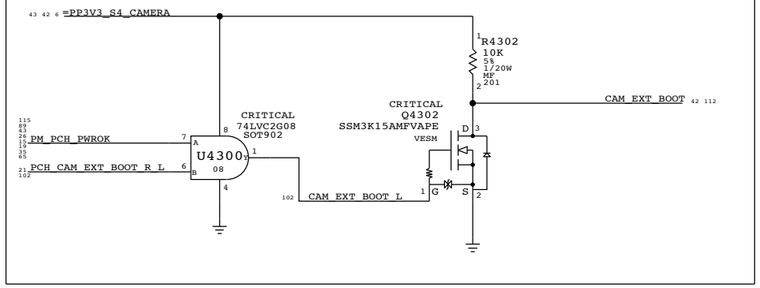
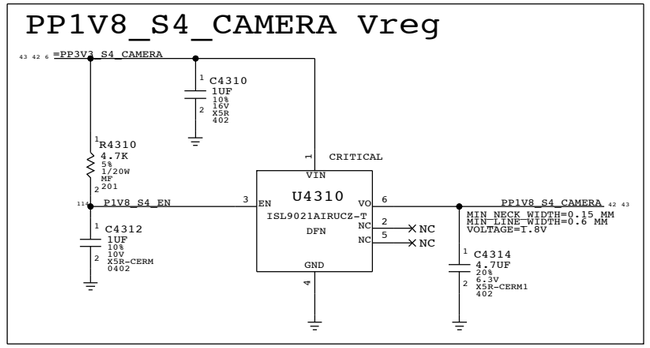
Camera Processor Reset



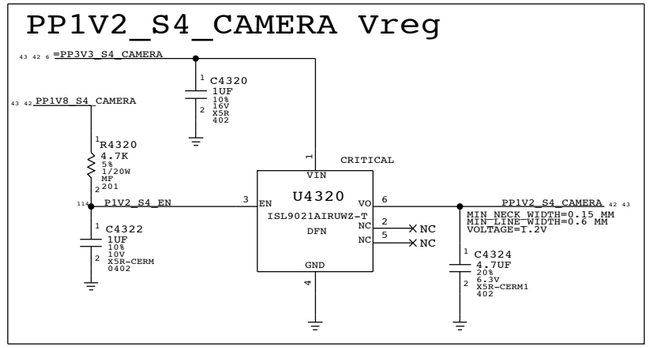
Camera Processor ExtBoot Cntl



PP1V8_S4_CAMERA Vreg



PP1V2_S4_CAMERA Vreg



SYNC_MASTER=D7_MLB SYNC_DATE=03/15/2012

PAGE TITLE
Camera Controller Support

Apple Inc.

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HDD DATA

J4520

EP00-081-91
M-ST-SM

CRITICAL
SILK_PART=HDD
518S0251

C4521 0.01UF
C4522 0.01UF
C4523 0.01UF
C4524 0.01UF

SATA_HDD_R2D_P → SATA_HDD_R2D_C_P
SATA_HDD_R2D_N → SATA_HDD_R2D_C_N
SATA_HDD_D2R_C_N → SATA_HDD_D2R_N
SATA_HDD_D2R_C_P → SATA_HDD_D2R_P

HDD POWER

PP12V_S0_HDD_FET
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=12V

PP5V_S0_HDD_FET
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=5V

CRITICAL
J4530
78047-0773
M-ST-SM-1

C4531 10UF 10% 25V X5R 1206-1
C4532 10UF 20% 10V X5R 603

SMC_OOB1_RX_CN → SMC_OOB1_RX_FILT

FERR-220-OHM
L4530
0402

SILK_PART=PWR
518S0865

GUMSTICK2

SILK_PART=GS2 SSD
J4500
SSD-K70
F-RT-SM1

155S0397 20mOHM
PLACE_NEAR=J4500.1:3MM
L4500
FERR-70-OHM-4A
0603
CRITICAL

PP3V3_S0_SSD_FLT
MIN_LINE_WIDTH=0.4mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=3.3V
=PP3V3_S0_SSD

C4500 0.1UF 20% 10V CERM 402
C4501 0.1UF 20% 10V CERM 402

NC
AC CAP O S12 SIDE
CLK_REQ
RESET_L

SATA_SSD_D2R_P
SATA_SSD_D2R_N
SATA_SSD_R2D_P
SATA_SSD_R2D_N

CRITICAL
514S0411
POR USE

=PP3V3_S0_SSD
R4521 100K 5% 1/16W MF-LF 402
R4522 100K 5% 1/16W MF-LF 402

SMC_OOB2_RX_L
SMC_OOB2_TX_L

D8:CONSIDER CHANGING SMC_OOB2_RX/TX_L PULL-UP TO 100K (FROM 10K) RDAR://10817697

SATA Activity LED

DEVELOPMENT
R4599 330 5% 1/10W MF-LF 603
=PP3V3_S0_LED_SATA → SATALED_R_L

DEVELOPMENT
D4599 GREEN-3.6MCD 2.0X1.25MM-SM

PCH_SATALED_L → SATALED_L
MAKE_BASE=TRUE

SILK_PART=SATA

SYNC_MASTER=D8_JERRY SYNC_DATE=01/31/2012

PAGE TITLE
SATA Connectors

Apple Inc.

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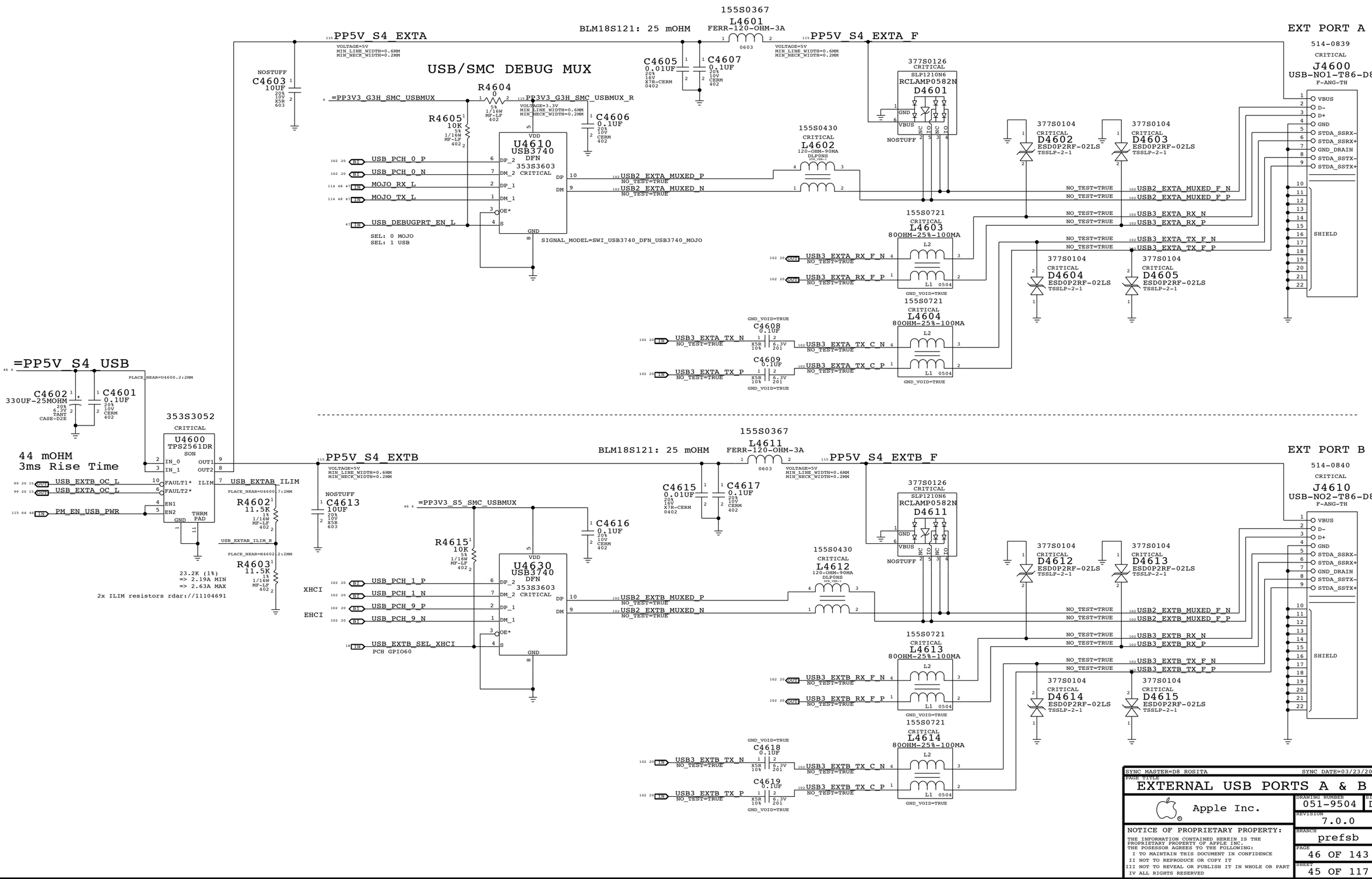
USB/SMC DEBUG MUX
EXTERNAL USB PORTS A & B
Apple Inc.
EXT PORT A
514-0839
J4600
USB-NO1-T86-D8
EXT PORT B
514-0840
J4610
USB-NO2-T86-D8
=PP5V_S4_USB
PP5V_S4_EXTA
PP5V_S4_EXTA_F
PP5V_S4_EXTB
PP5V_S4_EXTB_F
=PP3V3_G3H_SMC_USBMUX
PP3V3_G3H_SMC_USBMUX_R
=PP3V3_S5_SMC_USBMUX
U4610 USB3740 DFN 353S3603
U4630 USB3740 DFN 353S3603
U4600 TPS2561DR SON 353S3052
L4601 FERR-120-OHM-3A 155S0367
L4611 FERR-120-OHM-3A 155S0367
BLM18S121: 25 mOHM
L4602 120-OHM-90MA 155S0430
L4612 120-OHM-90MA 155S0430
L4603 80OHM-25%-100MA 155S0721
L4604 80OHM-25%-100MA 155S0721
L4613 80OHM-25%-100MA 155S0721
L4614 80OHM-25%-100MA 155S0721
D4601 RCLAMP0582N 377S0126
D4611 RCLAMP0582N 377S0126
D4602 ESD0P2RF-02LS 377S0104
D4603 ESD0P2RF-02LS 377S0104
D4604 ESD0P2RF-02LS 377S0104
D4605 ESD0P2RF-02LS 377S0104
D4612 ESD0P2RF-02LS 377S0104
D4613 ESD0P2RF-02LS 377S0104
D4614 ESD0P2RF-02LS 377S0104
D4615 ESD0P2RF-02LS 377S0104
SEL: 0 MOJO
SEL: 1 USB
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO
44 mOHM
3ms Rise Time
23.2K (1%)
=> 2.19A MIN
=> 2.63A MAX
2x ILIM resistors rdar://11104691
XHCI
EHCI
SYNC_MASTER=D8_ROSITA
SYNC_DATE=03/23/2012
PAGE TITLE
EXTERNAL USB PORTS A & B
DRAWING NUMBER 051-9504
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REVISION 7.0.0
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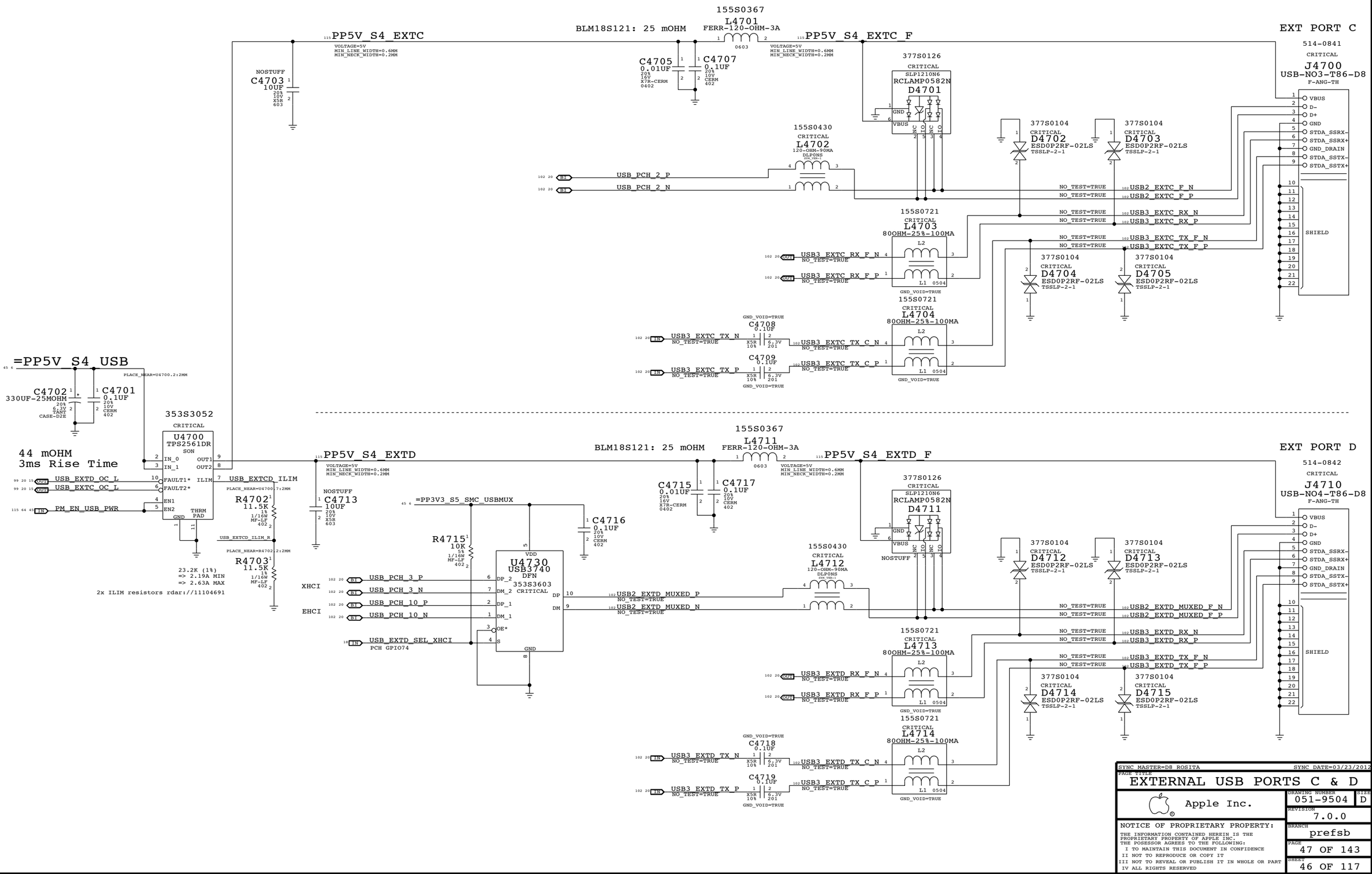
155S0367
L4701
BLM18S121: 25 mOHM
FERR-120-OHM-3A
0603
115 PP5V_S4_EXTC
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
115 PP5V_S4_EXTC_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF
C4703
10UF
20%
10V
X5R
603
C4705
0.01UF
20%
16V
X7R-CERM
0402
C4707
0.1UF
20%
10V
CERM
402
377S0126
CRITICAL
SLP1210N6
RCLAMP0582N
D4701
GND
VBUS
NC
IO
155S0430
CRITICAL
L4702
120-OHM-90MA
DLP0NS
377S0104
CRITICAL
D4702
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4703
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT C
514-0841
CRITICAL
J4700
USB-NO3-T86-D8
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
102 20 BI USB_PCH_2_P
102 20 BI USB_PCH_2_N
NO_TEST=TRUE
102 USB2_EXTC_F_N
102 USB2_EXTC_F_P
155S0721
CRITICAL
L4703
80OHM-25%-100MA
L2
L1 0504
GND_VOID=TRUE
102 20 OUT USB3_EXTC_RX_F_N
102 20 OUT USB3_EXTC_RX_F_P
102 USB3_EXTC_RX_N
102 USB3_EXTC_RX_P
377S0104
CRITICAL
D4704
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4705
ESD0P2RF-02LS
TSSLP-2-1
155S0721
CRITICAL
L4704
80OHM-25%-100MA
C4708
0.1UF
X5R
10%
6.3V
201
C4709
0.1UF
X5R
10%
6.3V
201
102 20 IN USB3_EXTC_TX_N
102 20 IN USB3_EXTC_TX_P
102 USB3_EXTC_TX_C_N
102 USB3_EXTC_TX_C_P
102 USB3_EXTC_TX_F_N
102 USB3_EXTC_TX_F_P
=PP5V_S4_USB
45 6
PLACE_NEAR=U4700.2:2MM
C4702
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
C4701
0.1UF
20%
10V
CERM
402
353S3052
CRITICAL
U4700
TPS2561DR
SON
IN_0
IN_1
OUT1
OUT2
FAULT1*
FAULT2*
ILIM
EN1
EN2
GND
THRM PAD
44 mOHM
3ms Rise Time
99 20 15 OUT USB_EXTD_OC_L
99 20 15 OUT USB_EXTC_OC_L
115 64 43 IN PM_EN_USB_PWR
USB_EXTCD_ILIM
PLACE_NEAR=U4700.7:2MM
R4702
11.5K
1%
1/16W
MF-LF
402
USB_EXTCD_ILIM_R
PLACE_NEAR=R4702.2:2MM
R4703
11.5K
1%
1/16W
MF-LF
402
23.2K (1%)
=> 2.19A MIN
=> 2.63A MAX
2x ILIM resistors rdar://11104691
155S0367
L4711
BLM18S121: 25 mOHM
FERR-120-OHM-3A
0603
115 PP5V_S4_EXTD
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
115 PP5V_S4_EXTD_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF
C4713
10UF
20%
10V
X5R
603
C4715
0.01UF
20%
16V
X7R-CERM
0402
C4717
0.1UF
20%
10V
CERM
402
377S0126
CRITICAL
SLP1210N6
RCLAMP0582N
D4711
GND
VBUS
NC
IO
NOSTUFF
155S0430
CRITICAL
L4712
120-OHM-90MA
DLP0NS
377S0104
CRITICAL
D4712
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4713
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT D
514-0842
CRITICAL
J4710
USB-NO4-T86-D8
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
=PP3V3_S5_SMC_USBMUX
45 6
C4716
0.1UF
10V
CERM
402
R4715
10K
5%
1/16W
MF-LF
402
U4730
USB3740
DFN
353S3603
CRITICAL
VDD
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
DP
DM
XHCI
EHCI
102 20 BI USB_PCH_3_P
102 20 BI USB_PCH_3_N
102 20 BI USB_PCH_10_P
102 20 BI USB_PCH_10_N
18 IN USB_EXTD_SEL_XHCI
PCH GPIO74
102 USB2_EXTD_MUXED_P
102 USB2_EXTD_MUXED_N
NO_TEST=TRUE
102 USB2_EXTD_MUXED_F_N
102 USB2_EXTD_MUXED_F_P
155S0721
CRITICAL
L4713
80OHM-25%-100MA
L2
L1 0504
GND_VOID=TRUE
102 20 OUT USB3_EXTD_RX_F_N
102 20 OUT USB3_EXTD_RX_F_P
102 USB3_EXTD_RX_N
102 USB3_EXTD_RX_P
377S0104
CRITICAL
D4714
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4715
ESD0P2RF-02LS
TSSLP-2-1
155S0721
CRITICAL
L4714
80OHM-25%-100MA
C4718
0.1UF
X5R
10%
6.3V
201
C4719
0.1UF
X5R
10%
6.3V
201
102 20 IN USB3_EXTD_TX_N
102 20 IN USB3_EXTD_TX_P
102 USB3_EXTD_TX_C_N
102 USB3_EXTD_TX_C_P
102 USB3_EXTD_TX_F_N
102 USB3_EXTD_TX_F_P
SYNC_MASTER=D8_ROSITA
SYNC_DATE=03/23/2012
PAGE TITLE
EXTERNAL USB PORTS C & D
Apple Inc.
DRAWING NUMBER
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SIZE
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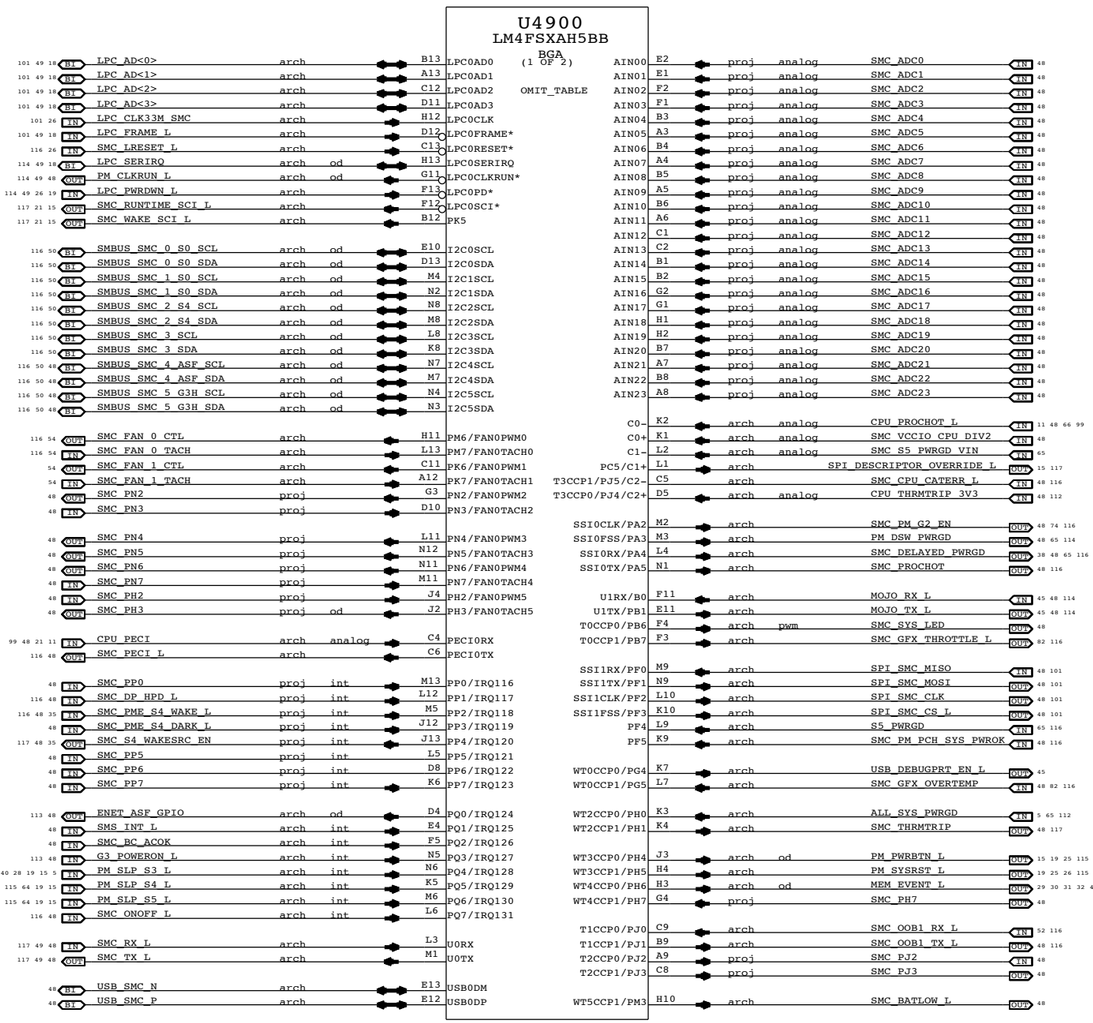
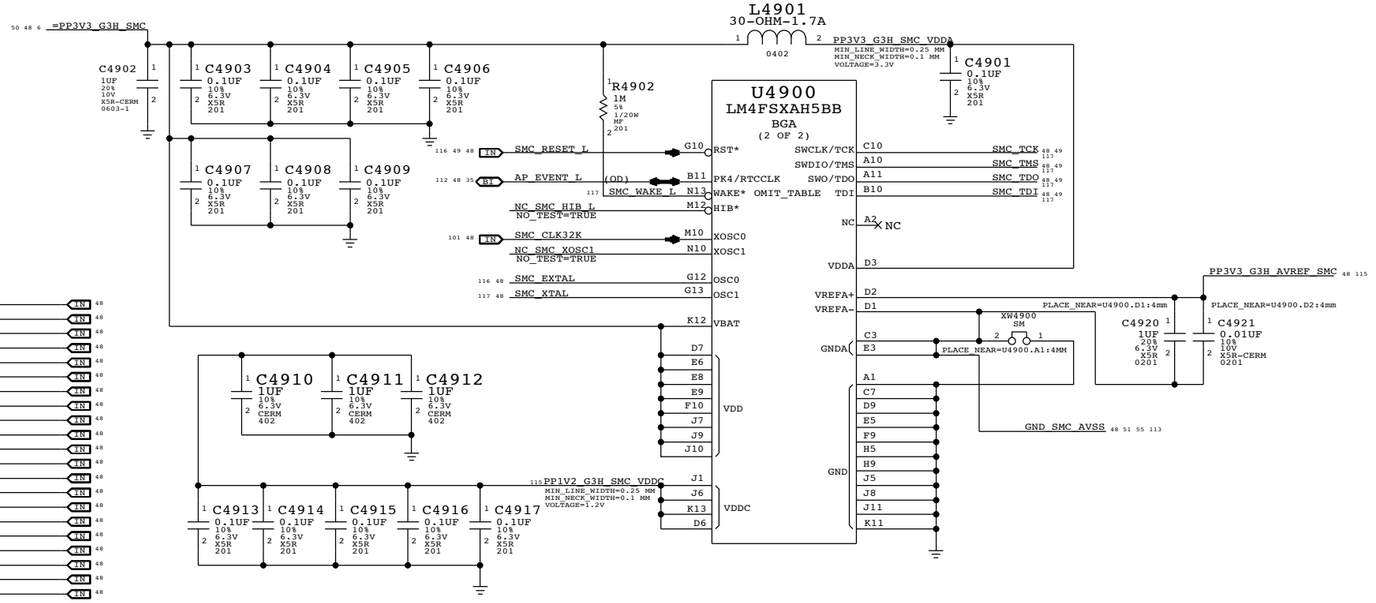
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





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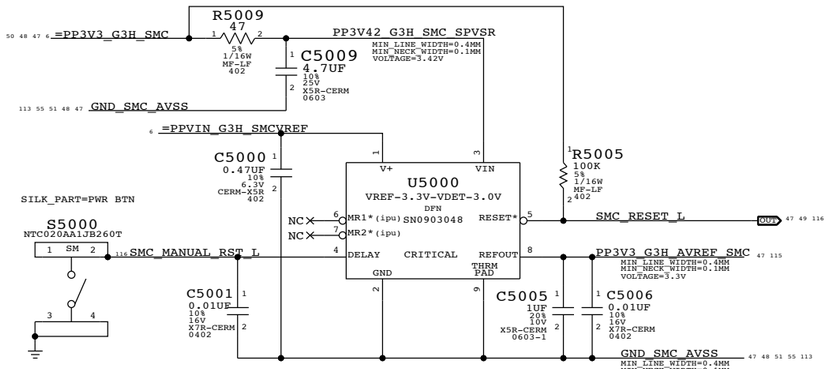
SMC Supervisor and AVREF Supply

rdar://11180279 SMC_RESET_L workaround



Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	SMCVSNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC1	SMCISNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC2	SMCVSNS_GPUCORE	MAKE_BASE=TRUE
SMC_ADC3	SMCISNS_GPUCORE	MAKE_BASE=TRUE
SMC_ADC4	SMCVSNS_P1V5S0_CPU_MEM	MAKE_BASE=TRUE
SMC_ADC5	SMCISNS_P1V5S0_CPU_MEM	MAKE_BASE=TRUE
SMC_ADC6	SMCVSNS_PVDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC7	SMCISNS_PVDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC8	SMCISNS_P12VS0_P1V05	MAKE_BASE=TRUE
SMC_ADC9	SMCISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE
SMC_ADC10	SMCVSNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC11	SMCISNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC12	SMCVSNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC13	SMCISNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC14	SMCVSNS_P5VS0_HDD	MAKE_BASE=TRUE
SMC_ADC15	SMCISNS_P5VS0_HDD	MAKE_BASE=TRUE
SMC_ADC16	SMCVSNS_P1V05S0_PCH	MAKE_BASE=TRUE
SMC_ADC17	SMCISNS_P1V05S0_PCH	MAKE_BASE=TRUE
SMC_ADC18	SMCISNS_P12VS0_HDD	MAKE_BASE=TRUE
SMC_ADC19	SMCISNS_P3V3S4_AP	MAKE_BASE=TRUE
SMC_ADC20	SMCVSNS_P3V3S0	MAKE_BASE=TRUE
SMC_ADC21	SMCISNS_P3V3S0_SSD	MAKE_BASE=TRUE
SMC_ADC22	SMCISNS_P12VS0_CPU_VCCSA	MAKE_BASE=TRUE
SMC_ADC23	SMCISNS_P12VS0_CPU_P1V05	MAKE_BASE=TRUE

Project-specific Aliases

SMC_PH3	BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PN5	ACDC_BURRST_EN_L	MAKE_BASE=TRUE
SMC_PJ3	SMC_OOB2_TX_L	MAKE_BASE=TRUE
SMC_PJ2	SMC_OOB2_RX_L	MAKE_BASE=TRUE
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE
SMC_PN4	SMC_BLC_FAULT	MAKE_BASE=TRUE

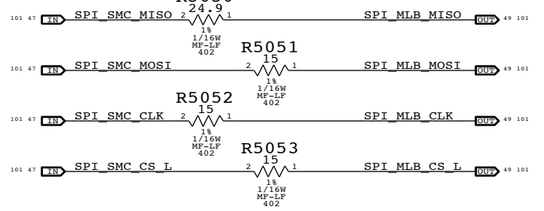
Unused Project-specific

radar://11033060 Remove USB hookup from SMC (not needed)

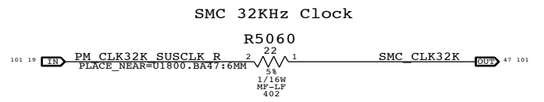
USB_SMC_P	NC_USB_SMC_P	MAKE_BASE=TRUE NO_TEST=TRUE
USB_SMC_N	NC_USB_SMC_N	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN2	NC_SMC_PN2	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN6	NC_SMC_PN6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE
TP for access if ZPB re-instated		
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_OOB1_TX_L	NC_SMB_OOB1_TX_L	MAKE_BASE=TRUE NO_TEST=TRUE

SMC SPI Support

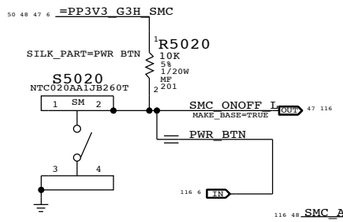
RDAR://11158919 D8:DETERMINE VALUE AND STUFF SERIES R FOR SPI BUS



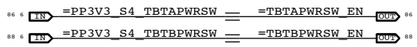
SMC 32KHz Clock



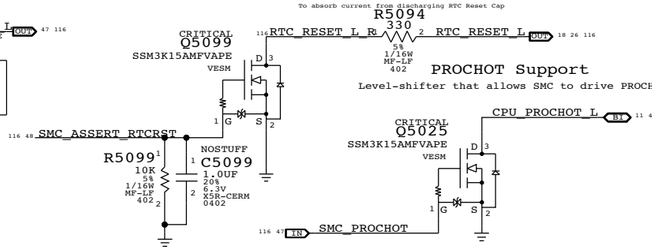
Power Button



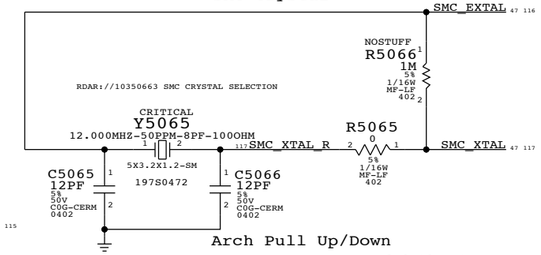
Enable S4 Wake Sources



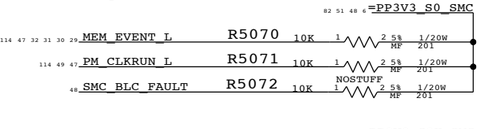
SMC Controlled RTC Reset



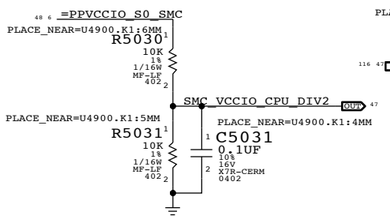
SMC Crystal



Arch Pull Up/Down



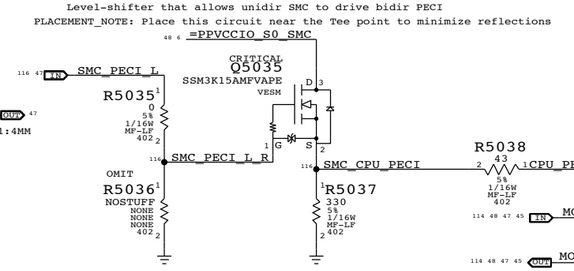
Comparator VCCIO Reference



PECI Support

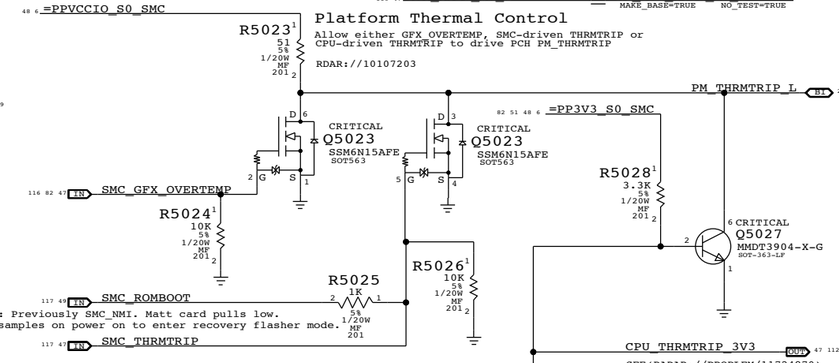
Level-shifter that allows unidir SMC to drive bidir PECI

PLACEMENT_NOTE: Place this circuit near the Tee point to minimize reflections

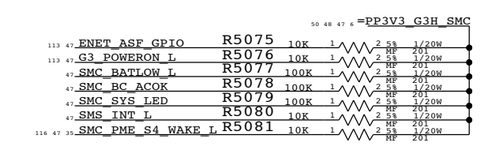


Platform Thermal Control

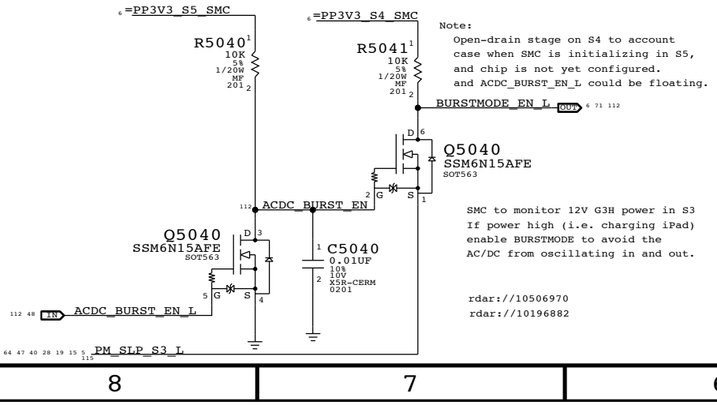
Allow either GFX_OVERTEMP, SMC-driven THRMTRIP or CPU-driven THRMTRIP to drive PCH PM_THRMTRIP



SMC SPI Support

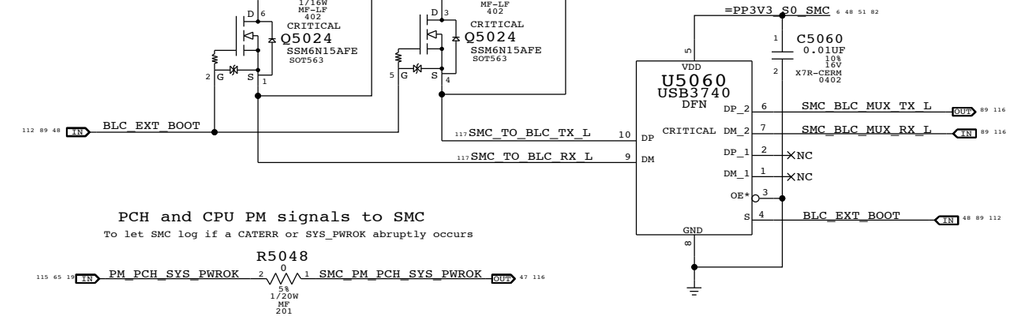


AC/DC Burst Mode Enable



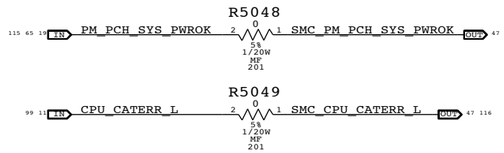
Connect BLC Serial through Mojo Mux

For a debug ability to communicate to BLC MCU through SMC

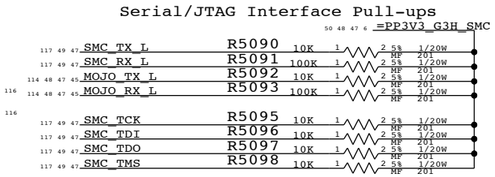


PCH and CPU PM signals to SMC

To let SMC log if a CATERR or SYS_PWROK abruptly occurs



Serial/JTAG Interface Pull-ups



Note:
Pull-down needed for SMC SSI signals

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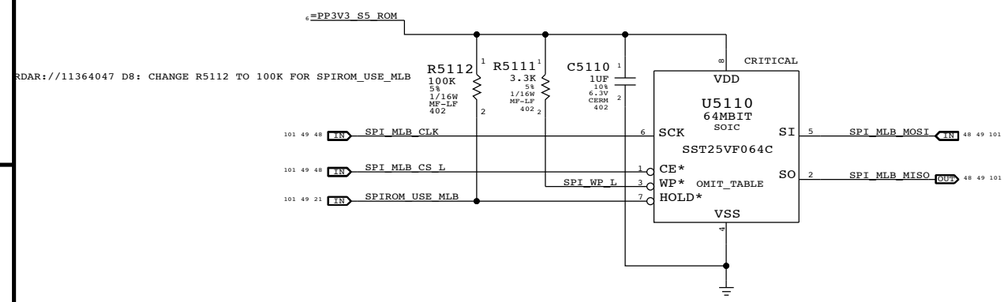
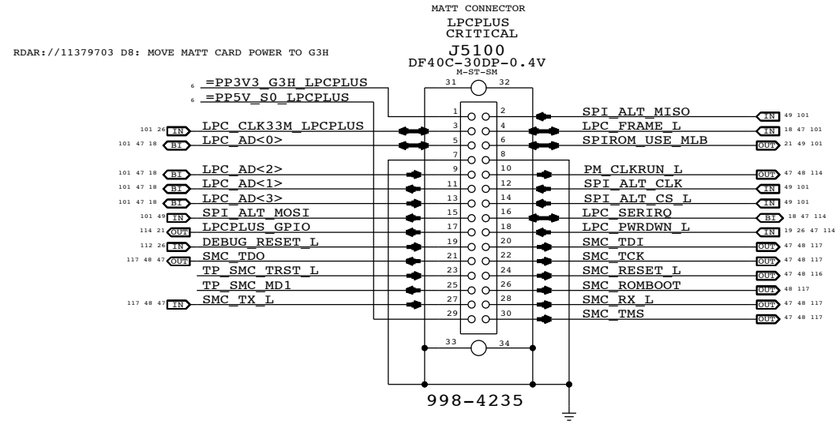
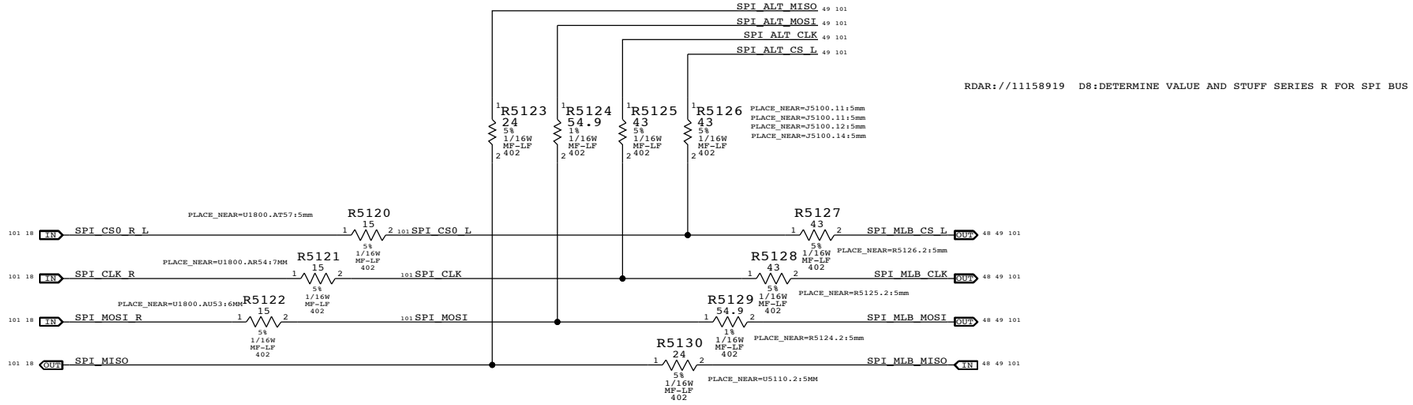
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC MASTER=D8 MLB	SYNC DATE=N/A
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Apple Inc.	DRAWING NUMBER: 051-9504 SIZE: D
	REVISION: 7.0.0
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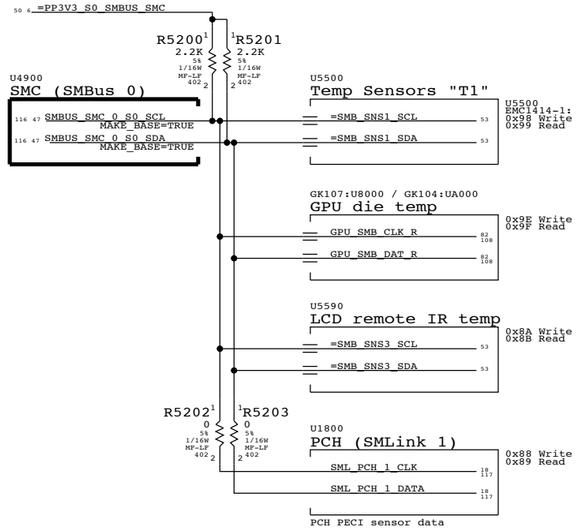

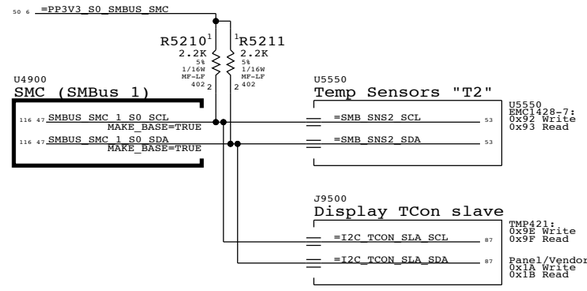

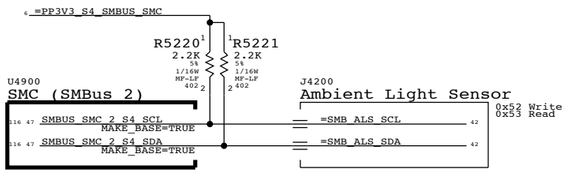

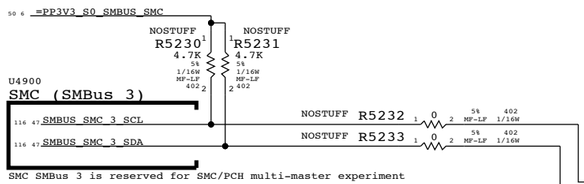

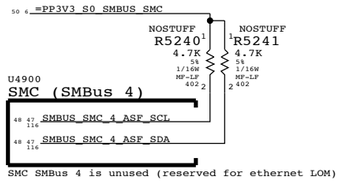

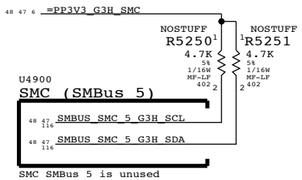

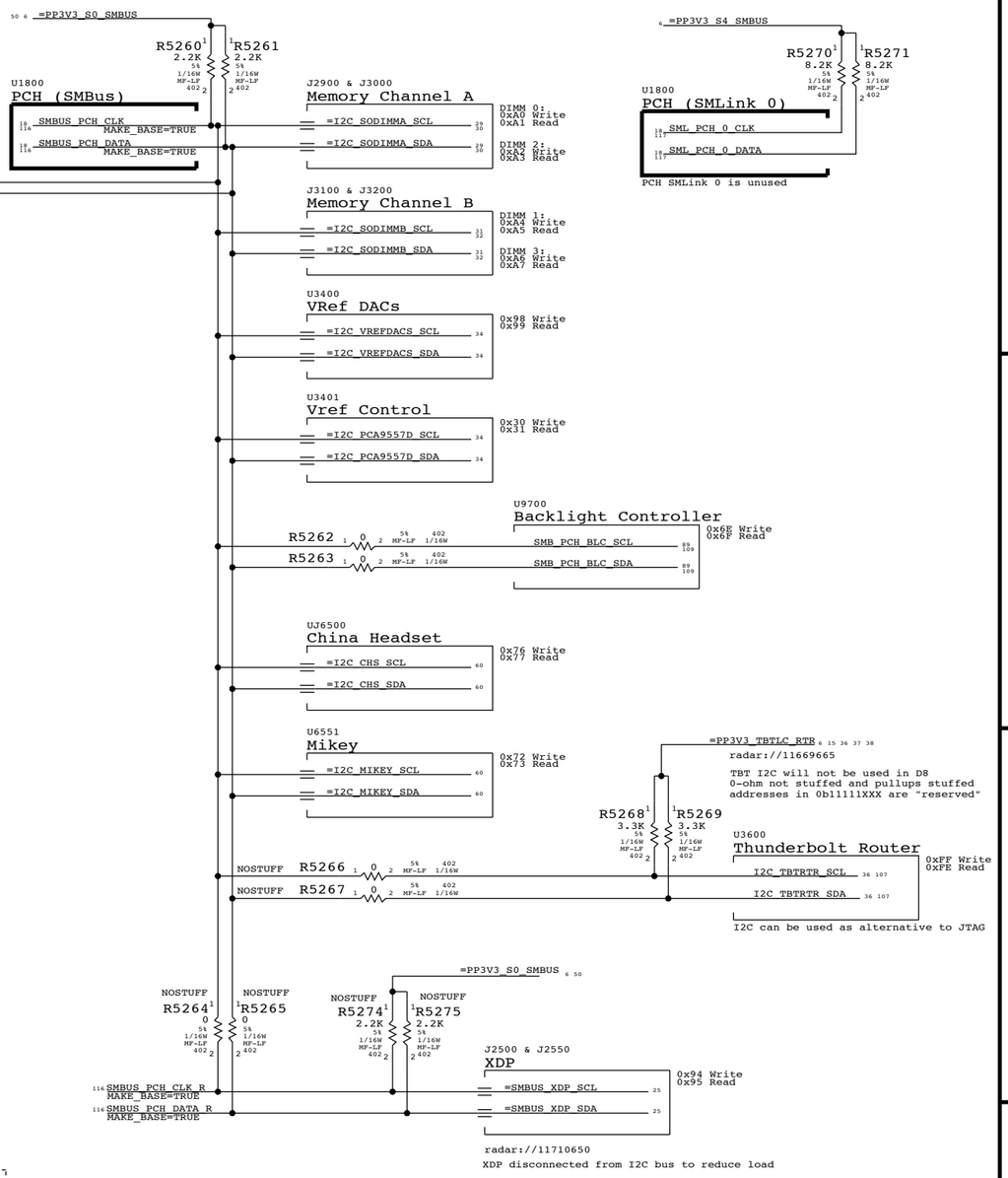

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ADC 0/1 12V G3H (ID2R/VD2R)

AC/DC lowside sense (System total)

AC/DC CURRENT SENSOR TO 100V/V: RDAR://10645440

TDP: 25 A
SCALE:33 A

R5300 0.001 1% 1W MF-1 0612

=PP12V_G3H_PWR → PP12V_G3H_SNS (OUT)

R5301 10K 1% 1/16W MF-LF 402 — U4900.E2:10mm

=PP12V_S5_SNS → SMCVSNS_P12VG3H (OUT)

R5302 3.32K 1% 1/16W MF-LF 402 — U4900.E2:10mm

C5302 0.1UF 20% 10V CERM 402

=PP3V3_S5_SENSE

C5300 0.22UF 20% 6.3V X5R 402

U5300 INA214 SC70

ISNSA_P12VG3H_N → IN-
ISNSA_P12VG3H_P → IN+
ISNS_P12VG3H_R ← OUT
REF → GND

353S2208
GAIN: 100 V/V

R5303 4.53K 1% 1/16W MF-LF 402 — U4900.E1:10mm

SMCISNS_P12VG3H (OUT)

C5303 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ADC 9 FBVDDQ 12V S0 (IG0F)

GPU FB highside sense

PEAK: 2.35 A
TDP: 1.76 A
SCALE:3.30 A

R5320 0.005 1% 1W MF 0612-2

=PP12V_S0_FBVDDQ_PWR → PP12V_S0_FBVDDQ_SNS (OUT)

=PP3V3_S0_SENSE

C5320 0.22UF 20% 6.3V X5R 402

U5320 INA210 SC70

ISNSA_P12VS0_FBVDDQ_N → IN-
ISNSA_P12VS0_FBVDDQ_P → IN+
ISNS_P12VS0_FBVDDQ_R ← OUT
REF → GND

353S2073
Gain: 200 V/V

R5323 4.53K 1% 1/16W MF-LF 402 — U4900.A5:10MM

SMCISNS_P12VS0_FBVDDQ (OUT)

C5323 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ADC 16/17 PCH 1.05V S0 (IN1R/VN1R)

PCH Vcc 1.05V lowside sense

PEAK: 5.93 A
TDP: 4.45 A
SCALE:8.25 A

R5340 0.002 1% 1W MF-1 0612

=PP1V05_S0_PCH_PWR → PP1V05_S0_PCH_SNS (OUT)

R5342 4.53K 1% 1/16W MF-LF 402 — U4900.G2:10MM

SMCVSNS_P1V05S0_PCH (OUT)

C5342 0.22UF 20% 6.3V X5R 402

=PP3V3_S0_SENSE

C5340 0.22UF 20% 6.3V X5R 402

U5340 INA210 SC70

ISNSA_P1V05S0_PCH_N → IN-
ISNSA_P1V05S0_PCH_P → IN+
ISNS_P1V05S0_PCH_R ← OUT
REF → GND

353S2073
Gain: 200 V/V

R5343 4.53K 1% 1/16W MF-LF 402 — U4900.G1:10MM

SMCISNS_P1V05S0_PCH (OUT)

C5343 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ADC 2/3 GPUCORE IMON S0 (IG0C/VG0C)

GPU Core

GK104: PEAK: 120 A TDP: 95 A SCALE:141 A
GK107: PEAK: 30 A TDP: 24 A SCALE:141 A

=PPVCORE_S0_GPU

R5308 4.53K 1% 1/16W MF-LF 402 — U4900.F2:10mm

SMCVSNS_GPUCORE (OUT)

C5308 0.22UF 20% 6.3V X5R 402

=PP5V_S0_ISENSE

C5305 0.01UF 20% 16V X7R-CERM 0402

VR IMON SCALE TENTATIVE

OpAmp Gain = 3.1 V/V

VMAX = 0.9V @ 120 A

VR_GPU_IMON (EN) → R5305 10K 1% 1/16W MF-LF 402 → ISNS_GPUCORE_P

ISNS_GPUCORE_N

U5305 OPA348 SC70-5 (CRITICAL)

R5306 10K 1% 1/16W MF-LF 402

R5307 21K 1% 1/16W MF-LF 402 → ISNS_GPUCORE_FB

R5309 5.1K 5% 1/16W MF-LF 402 — U4900.F1:10mm

SMCISNS_GPUCORE (OUT)

C5309 0.22UF 10% 6.3V X5R-CERM 0402

GND_SMC_AVSS

ADC 10/11 CPUCORE IMON S0 (VC0C/IC0C)

CPU VCCore

PEAK: 112 A
TDP: 83 A
SCALE:142 A

=PPVCORE_S0_CPU

R5328 4.53K 1% 1/16W MF-LF 402 — U4900.B6:10mm

SMCVSNS_CPUCORE (OUT)

C5328 0.22UF 20% 6.3V X5R 402

=PP5V_S0_ISENSE

C5325 0.01UF 20% 16V X7R-CERM 0402

OpAmp Gain = 3.1 V/V

VMax = 0.9V @ 120A

REG_CPUCORE_IMON (EN) → R5325 10K 1% 1/16W MF-LF 402 → ISNS_CPUCORE_P

ISNS_CPUCORE_N

U5325 OPA348 SC70-5 (CRITICAL)

R5326 10K 1% 1/16W MF-LF 402

R5327 21K 1% 1/16W MF-LF 402 → ISNS_CPUCORE_FB

R5329 5.1K 5% 1/16W MF-LF 402 — U4900.A6:10mm

SMCISNS_CPUCORE (OUT)

C5329 0.22UF 10% 6.3V X5R-CERM 0402

GND_SMC_AVSS

ADC18 HDD 12V S0 (IH02/VH02)

HIGHSIDE SENSE FOR HDD 12V

PEAK: 2.0 A
TDP: 0.8 A
SCALE:3.3 A

R5345 0.005 1% 1W MF 0612-2

=PP12V_S0_HDD_PWR → PP12V_S0_HDD_SNS (OUT)

=PP3V3_S0_SENSE

C5345 0.22UF 20% 6.3V X5R 402

U5345 INA210 SC70

ISNSA_P12VS0_HDD_N → IN-
ISNSA_P12VS0_HDD_P → IN+
ISNS_P12VS0_HDD_R ← OUT
REF → GND

353S2073
Gain: 200 V/V

R5348 4.53K 1% 1/16W MF-LF 402 — U4900.H1:10MM

SMCISNS_P12VS0_HDD (OUT)

C5348 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ADC 4/5 CPU DDR3 S0 (IC0M/VC0M)

CPU VDD (DDR3) lowside sense

PEAK: 4.75 A
TDP: 1.25 A
SCALE:6.60 A

R5310 0.001 1% 1W MF 0612

=PP1V5_S0_CPU_MEM_PWR → PP1V5_S0_CPU_MEM_SNS (OUT)

R5312 4.53K 1% 1/16W MF-LF 402 — U4900.B3:10mm

SMCVSNS_P1V5S0_CPU_MEM (OUT)

C5312 0.22UF 20% 6.3V X5R 402

=PP3V3_S0_SENSE

C5310 0.22UF 20% 6.3V X5R 402

U5310 INA211 SC70

ISNSA_P1V5S0_CPU_MEM_N → IN-
ISNSA_P1V5S0_CPU_MEM_P → IN+
ISNS_P1V5S0_CPU_MEM_R ← OUT
REF → GND

353S2216
Gain: 500 V/V

R5313 4.53K 1% 1/16W MF-LF 402 — U4900.A3:10mm

SMCISNS_P1V5S0_CPU_MEM (OUT)

C5313 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ADC12/13 CPUAXG IMON S0 (VC0G/IC0G)

CPU VCCAXG

PEAK: 35.0 A
TDP: 25.0 A
SCALE:41.4 A

=PPVAXG_S0_CPU

R5333 4.53K 1% 1/16W MF-LF 402 — U4900.C1:10mm

SMCVSNS_CPUAXG (OUT)

C5333 0.22UF 20% 6.3V X5R 402

=PP5V_S0_ISENSE

C5330 0.01UF 20% 16V X7R-CERM 0402

OpAmp Gain = 3.1 V/V

VMax = 0.9V @ 35A

REG_CPUAXG_IMON (EN) → R5330 10K 1% 1/16W MF-LF 402 → ISNS_CPUAXG_P

ISNS_CPUAXG_N

U5330 OPA348 SC70-5 (CRITICAL)

R5331 10K 1% 1/16W MF-LF 402

R5332 21K 1% 1/16W MF-LF 402 → ISNS_CPUAXG_FB

R5334 5.1K 5% 1/16W MF-LF 402 — U4900.C2:10mm

SMCISNS_CPUAXG (OUT)

C5334 0.22UF 10% 6.3V X5R-CERM 0402

GND_SMC_AVSS

ADC20/21 SSD 3.3V S0 (IH1R/VR3R)

Voltage sense of 3.3V S0
(radar://problem/1056794)
Current sense of SSD 3.3V FET

PEAK: 3.0A
TDP: 2.1 A
SCALE:3.3 A

R5350 0.002 1% 1W MF 0612

=PP3V3_S0_SSD_PWR → PP3V3_S0_SSD_SNS (OUT)

R5351 4.53K 1% 1/16W MF-LF 402 — U4900.B7:10MM

SMCVSNS_P3V3S0 (OUT)

C5352 0.22UF 20% 6.3V X5R 402

=PP3V3_S0_SMC

U5350 INA216A4YFFX WCSP-4

ISNSA_P3V3S0_SSD_P → IN+ (A1)
ISNSA_P3V3S0_SSD_N → IN- (A2)
ISNS_P3V3S0_SSD_R ← OUT (B2)
GND (B1)

353S3597
Gain: 200 V/V

R5353 4.53K 1% 1/16W MF-LF 402 — U4900.A7:10MM

SMCISNS_P3V3S0_SSD (OUT)

C5353 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ADC 6/7 SODIMM DDR3 S3 (IM0R/VM0R)

DIMM 1.5V lowside sense

PEAK: 11.3 A
TDP: 10.0 A
SCALE:13.2 A

R5315 0.0005 1% 1W MF 0612

=PPVDDQ_S3_DDR_PWR → PPVDDQ_S3_DDR_SNS (OUT)

R5317 4.53K 1% 1/16W MF-LF 402 — U4900.B4:10MM

SMCVSNS_PVDDQS3_DDR (OUT)

C5317 0.22UF 20% 6.3V X5R 402

R5316 0 5% 1/16W MF-LF 402

=PP3V3_S4_SENSE → NOSTUFF

R5319 0 5% 1/16W MF-LF 402

=PP3V3_S0_SENSE

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C5315 0.22UF 20% 6.3V X5R 402

U5315 INA211 SC70

ISNSA_PVDDQS3_DDR_N → IN-
ISNSA_PVDDQS3_DDR_P → IN+
ISNS_PVDDQS3_DDR_R ← OUT
REF → GND

353S2216
Gain: 500 V/V

R5318 4.53K 1% 1/16W MF-LF 402 — U4900.A4:10MM

SMCISNS_PVDDQS3_DDR (OUT)

C5318 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ADC14/15 HDD 5V S0 (VH05/IH05)

Highside sense for HDD 5V

PEAK: 1.2 A
TDP: 0.5 A
SCALE:3.3 A

R5335 0.005 1% 1W MF 0612-2

=PP5V_S0_HDD_PWR → PP5V_S0_HDD_SNS (OUT)

R5336 4.53K 1% 1/16W MF-LF 402 — U4900.B1:10MM

SMCVSNS_P5VS0_HDD (OUT)

C5337 0.22UF 20% 6.3V X5R 402

R5337 6.65K 1% 1/16W MF-LF 402

NOTE, MUST KEEP 5V OUT BELOW 3.3V

U5335 INA216A4YFFX WCSP-4

ISNSA_P5VS0_HDD_P → IN+ (A1)
ISNSA_P5VS0_HDD_N → IN- (A2)
ISNS_P5VS0_HDD_R ← OUT (B2)
GND (B1)

353S2073
Gain: 200 V/V

R5338 4.53K 1% 1/16W MF-LF 402 — U4900.B2:10MM

SMCISNS_P5VS0_HDD (OUT)

C5338 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

SYNC_MASTER=D8_DOUG SYNC_DATE=06/20/2012

PAGE TITLE: I and V Sense 1

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D
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BRANCH: prefsb
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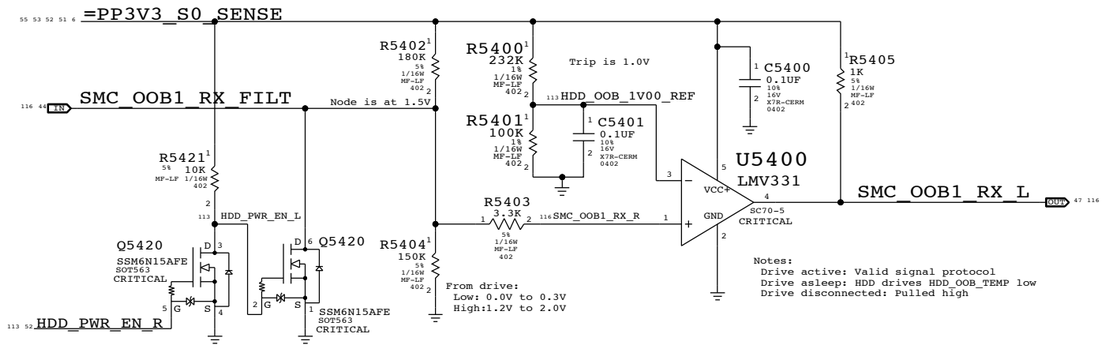
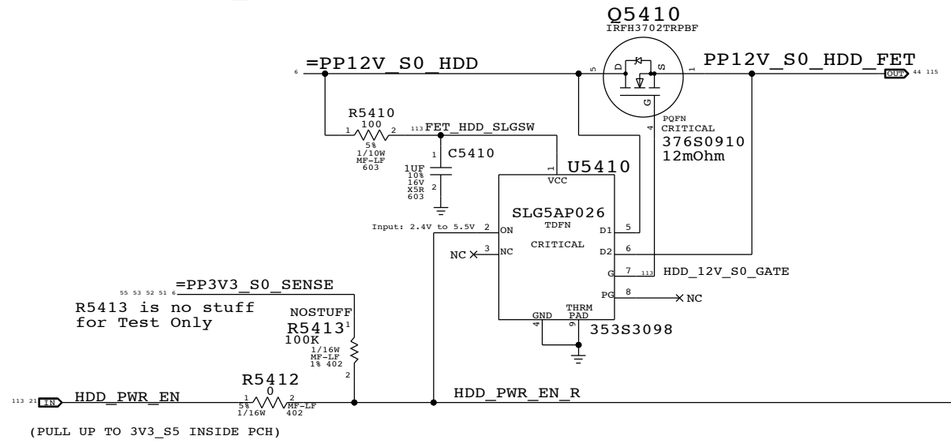
HDD Out-of-Band Temp Sensing

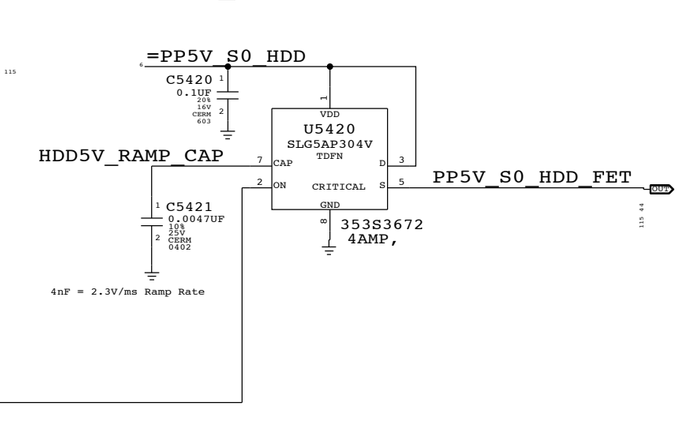
Temperature read from SATA power connecter pin 11



HDD 12V_S0 FET (max 2.8A,ave 0.6A)



HDD 5V_S0 FET (max 0.7A,ave 0.3A)



REMOVE R5413 AND SHORT R5412 AFTER HDD_PWR_EN WORKS

SYNC-MASTER=D8-JERRY- - - - - - - - SYNC-DATE=02/25/2012

PAGE TITLE: HDD/SSD Temp Sense

Apple Inc.

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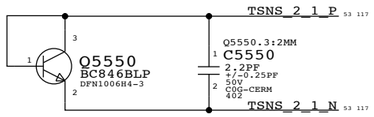
Temperature Sensor T2 EMC1428: Near GPU VR

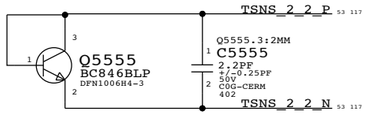
SNS T2: TEMP SENSOR IC

GPU Proximity



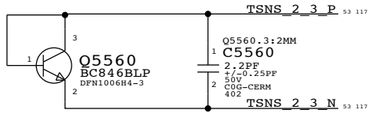
PLACEMENT_NOTE=Place Q5550 near GPU and GDDR5

Ambient



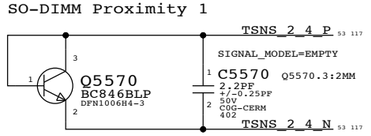
PLACEMENT_NOTE=Place Q5555 near bottom of board

BLC Proximity



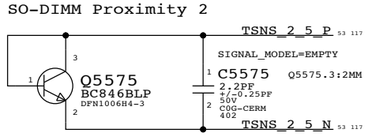
PLACEMENT_NOTE=Place Q5560 near BLC VR

SO-DIMM Proximity 1



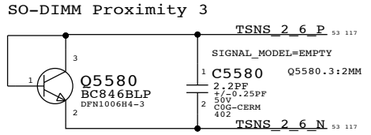
PLACEMENT_NOTE=Place Q5570 near SO-DIMM connectors (top left)

SO-DIMM Proximity 2



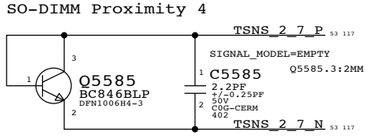
PLACEMENT_NOTE=Place Q5575 near SO-DIMM connectors (top right)

SO-DIMM Proximity 3



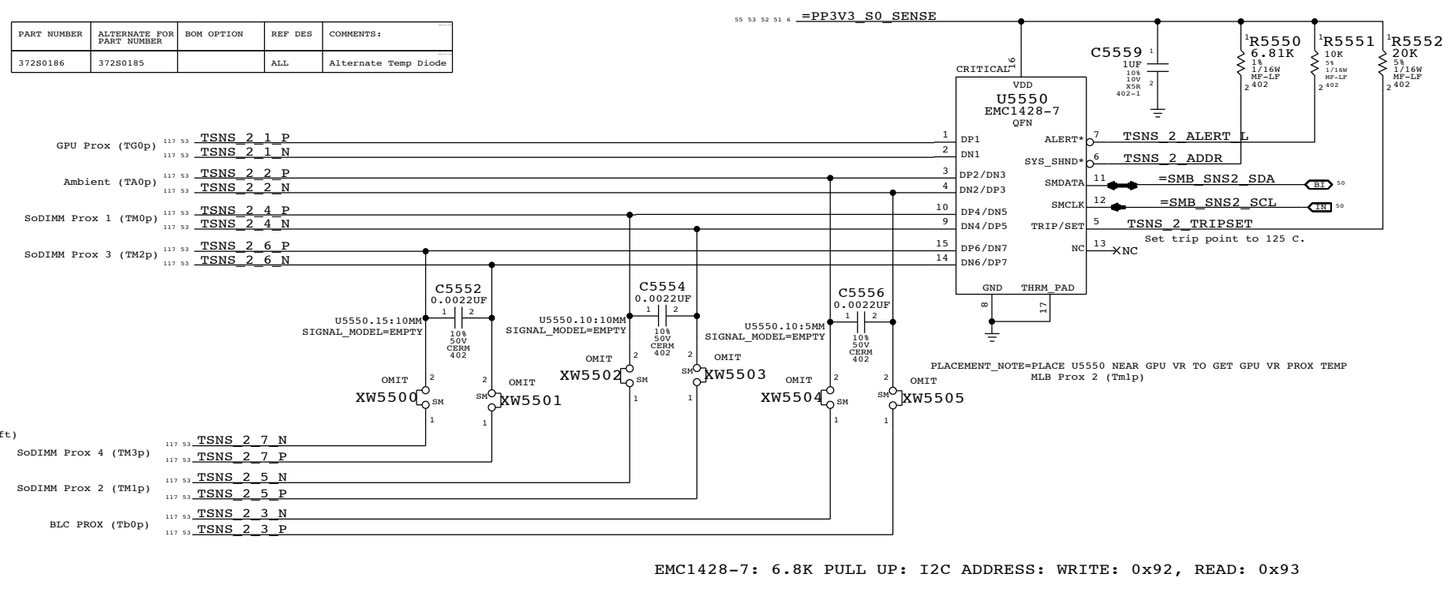
PLACEMENT_NOTE=Place Q5580 near SO-DIMM connectors (bottom left)

SO-DIMM Proximity 4



PLACEMENT_NOTE=Place Q5585 near SO-DIMM connectors (bottom right)

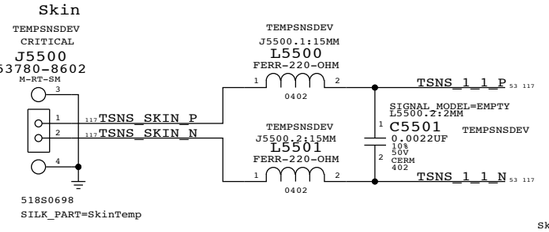
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



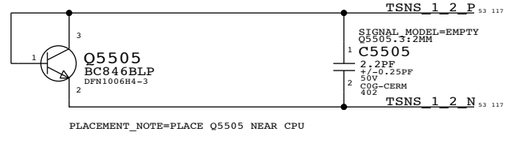
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

Temperature Sensor T1 EMC1414: Near PSU Conn

Skin

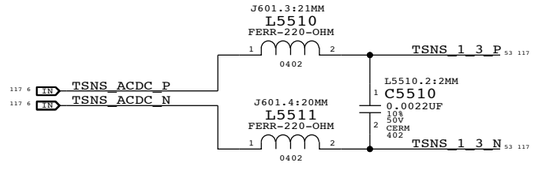


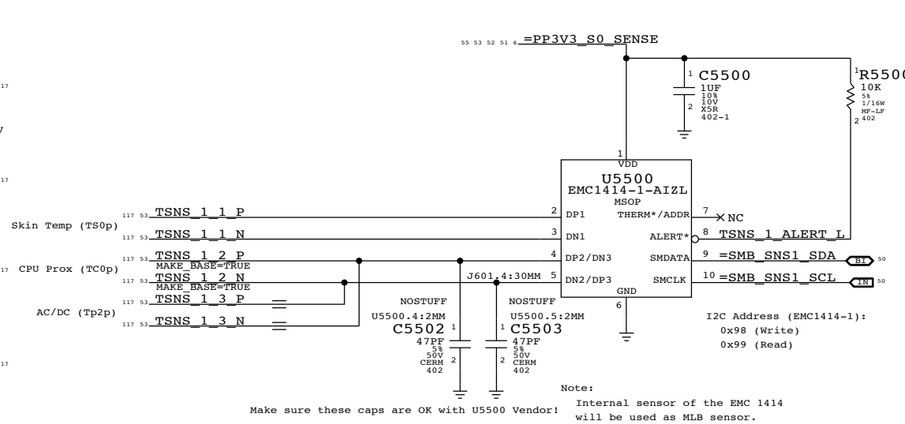
CPU Proximity



PLACEMENT_NOTE=PLACE Q5505 NEAR CPU

AC/DC Via connector to diode inside PSU



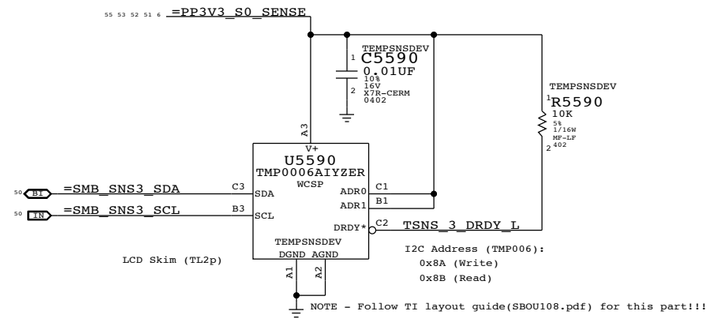


Make sure these caps are OK with U5500 Vendor!

Note:
Internal sensor of the EMC 1414
will be used as MLB sensor.
MLB Prox 1 (Tm0p)

PLACEMENT_NOTE=PLACE U5500 NEAR PSU CONNECTOR

Temperature Sensor T3: LCD Remote Sensor(Dev4Now)



NOTE - Follow TI layout guide(SBOU108.pdf) for this part!!!

SYNC_MASTER=D8 DOUG SYNC_DATE=06/07/2012

PAGE TITLE: Temperature Sensors

Apple Inc.

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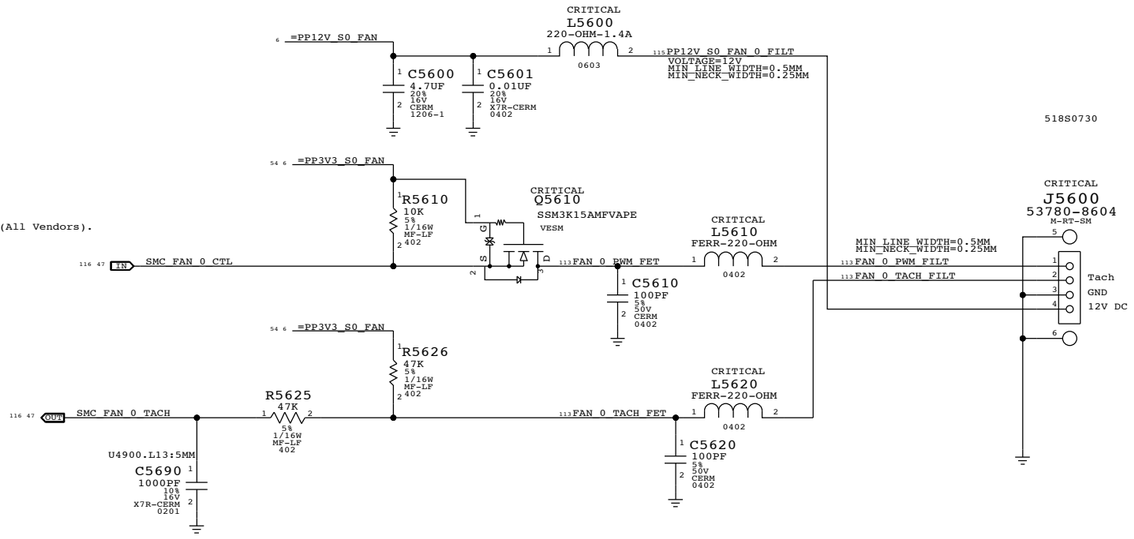
SMC Fan 0 (System)

Note:

The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



SMC Fan 1 (Unused)

47 IN SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
MAKE_BASE=TRUE NO_TEST=TRUE

47 OUT SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=D8_DOUG SYNC_DATE=07/19/2012

PAGE TITLE
System Fan

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
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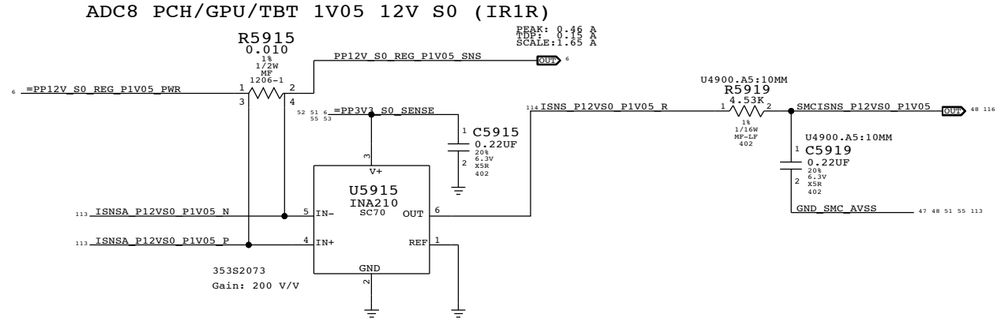
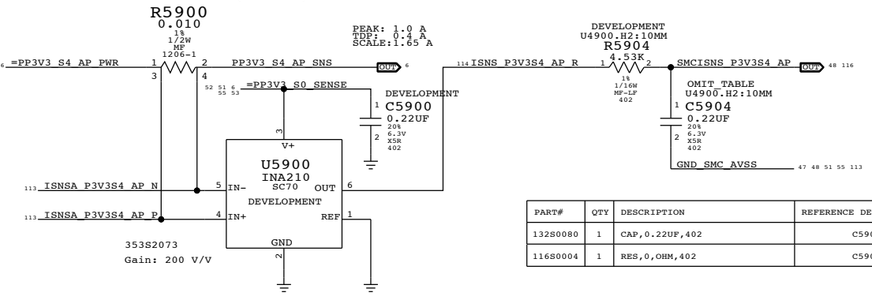
ADC8 PCH/GPU/TBT 1V05 12V S0 (IR1R)



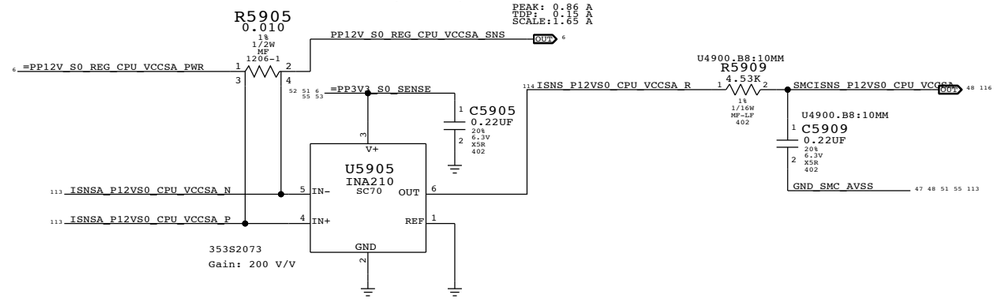
ADC19 AP 3.3V S4 (IW0R)

Current sense of AP 3.3V FET

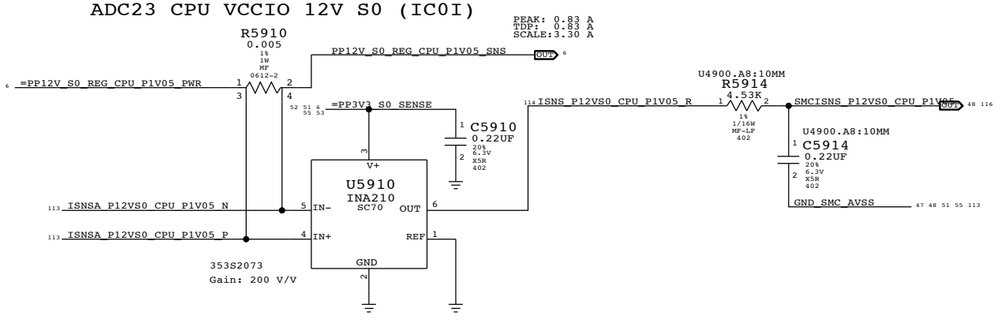


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	1	CAP,0.22UF,402	C5904	DEVELOPMENT
116S0004	1	RES,0,OHM,402	C5904	PRODUCTION

ADC22 CPU VCCSA 12V S0 (IC0S)



ADC23 CPU VCCIO 12V S0 (IC0I)



SYNC_MASTER=D8_MARK SYNC_DATE=04/23/2012

PAGE TITLE: I and V Sense 2

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

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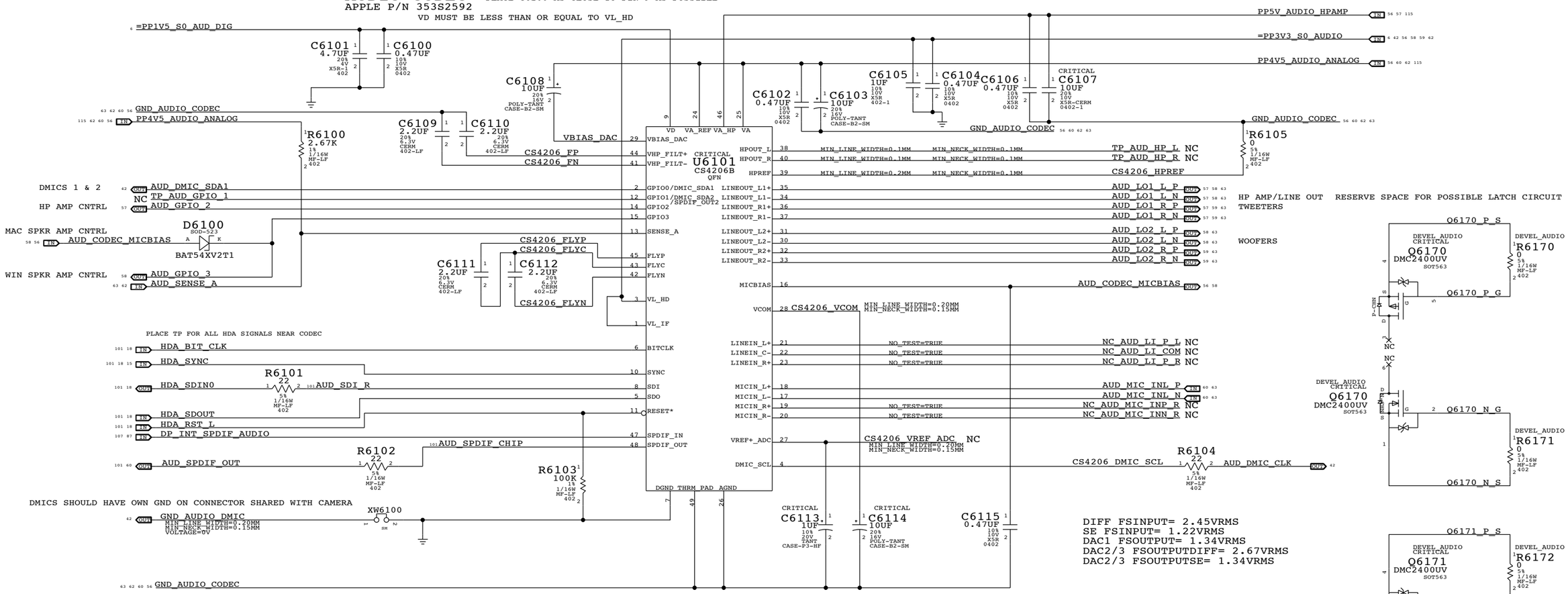
AUDIO CODEC

APPLE P/N 353S2592

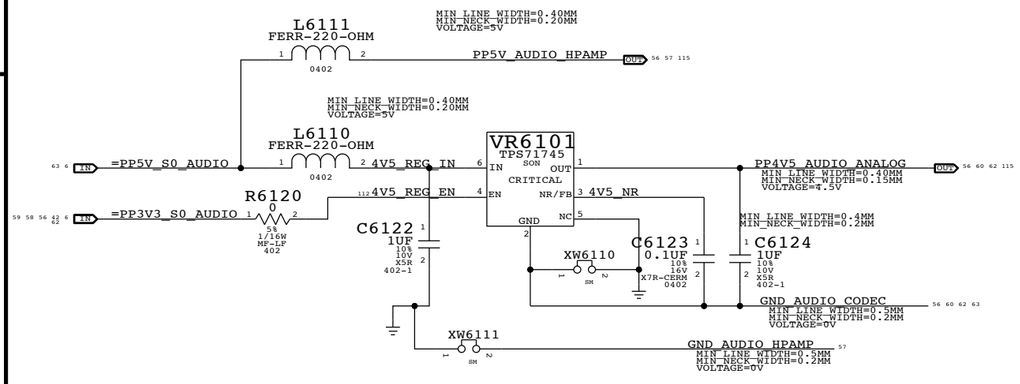
PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0134	127S0111		C6113	THAILAND ALTERNATE

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC



PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

SYNC_MASTER=D8_DAVID SYNC_DATE=06/13/2012

PAGE TITLE: AUDIO: CODEC/REGULATORS

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

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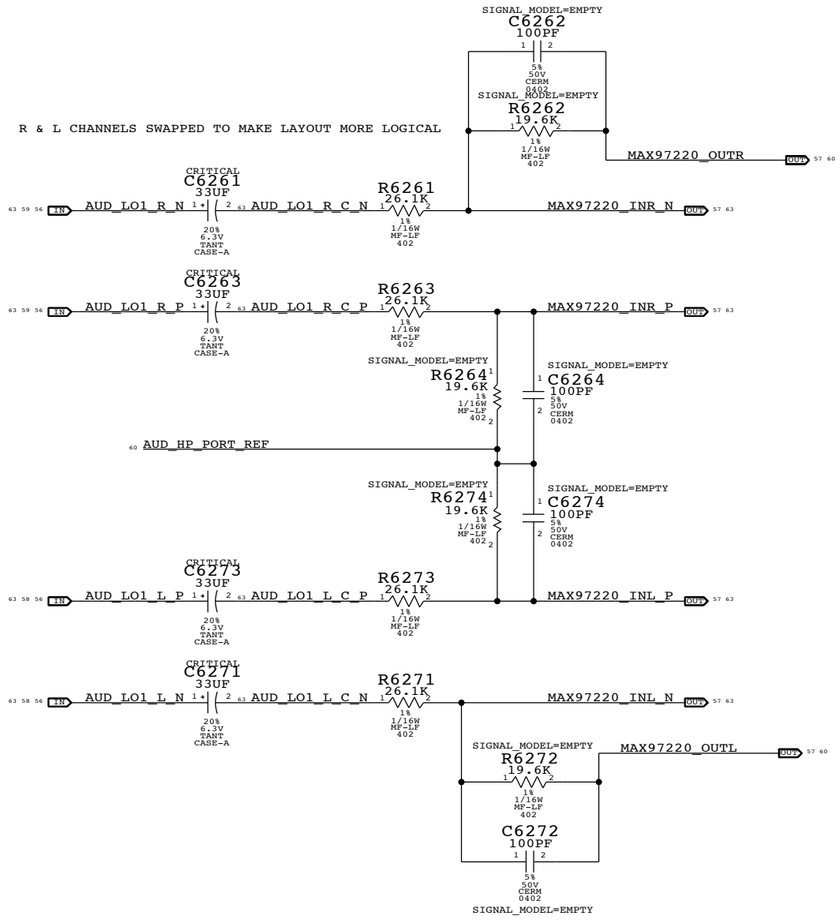

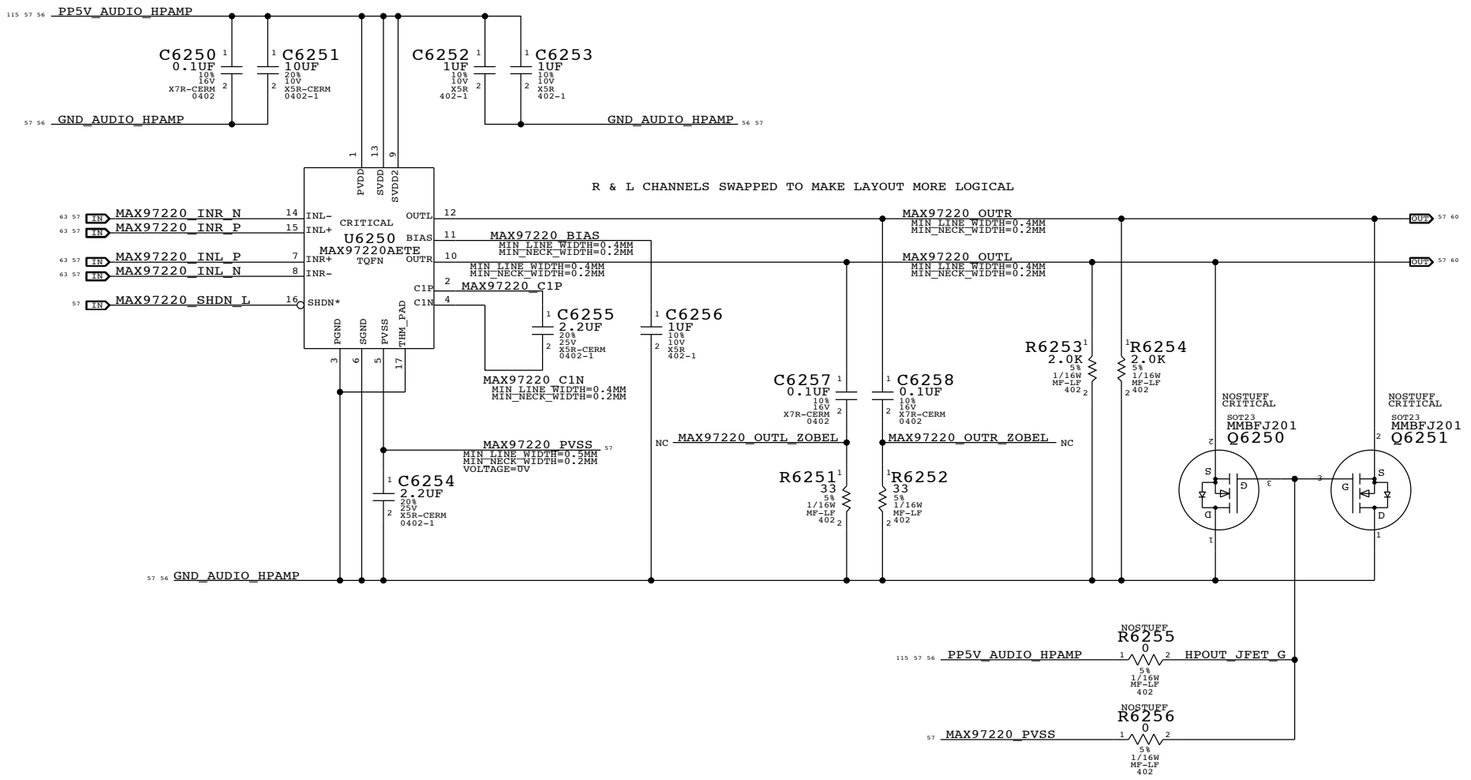

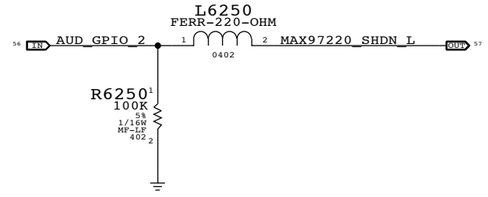

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0135	127S0120		C6261	THAILAND ALTERNATE
127S0135	127S0120		C6263	THAILAND ALTERNATE
127S0135	127S0120		C6271	THAILAND ALTERNATE
127S0135	127S0120		C6273	THAILAND ALTERNATE

SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE
AUDIO: HEADPHONE AMP

Apple Inc.

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 20% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 220UF 20% 16V ELEC SM-CASE-C1-HF
CRITICAL C6307 220UF 20% 16V ELEC SM-CASE-C1-HF

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6300 FERR-1000-OHM 0402 — AUD_LO2_L_N — C6308 1UF 10% 25V X5R 0402 — AUD_LAMP_RINC_P — AUD_LAMP_RIN_P
L6301 FERR-1000-OHM 0402 — AUD_LO2_L_P — C6309 1UF 10% 25V X5R 0402 — AUD_LAMP_RINC_N — AUD_LAMP_RIN_N
L6302 FERR-1000-OHM 0402 — AUD_LO1_L_P — C6310 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_LINC_P — AUD_LAMP_LIN_P
L6303 FERR-1000-OHM 0402 — AUD_LO1_L_N — C6311 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_LINC_N — AUD_LAMP_LIN_N

CRITICAL U6300 SSM3302 LFCSP

20	INR+	
19	INR-	
22	SDNR*	ONLY WOOFERS ON UNDER WINDOWS — AUD_SPKRAMP_WIN_SHDN_L
16	MONO	AUD_LAMP_MONO
9	SDNL*	WOOFERS & TWEETERS ON UNDER MAC OS — AUD_SPKRAMP_MAC_SHDN_L
11	INL+	
12	INL-	
21	GAIN	AUD_LAMP_GAIN
8	VREG/AVDD	AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	=PP3V3_S0_AUDIO
34,35,36,37	PVDD	
7,24,41	AGND	
31,32,33,38,39,40	PGND	
THERM 17		TP_AUD_LAMP_THERM — NC
BOOTR+ 30		C6313 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
OUTR+ 28,29		AUD_LAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
OUTR- 26,27		AUD_LAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
BOOTR- 25		C6314 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
EDGE 10		AUD_LAMP_EDGE
BOOTL+ 1		C6315 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
OUTL+ 2,3		AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
OUTL- 4,5		AUD_LAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
BOOTL- 6		C6316 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
NC 18		NC
NC 13		NC
TEST 14,15		

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

SIGNAL_MODEL=EMPTY
CRITICAL L6305 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LWFR_OUT_P / AUD_SPKR_LWFR_OUT_N
CRITICAL C6323 1000PF 5% 25V NPO-C0G 402

SIGNAL_MODEL=EMPTY
CRITICAL L6307 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LTWT_OUT_P / AUD_SPKR_LTWT_OUT_N
CRITICAL C6324 1000PF 5% 25V NPO-C0G 402

CRITICAL C6320 1000PF 5% 25V NPO-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6322 1000PF 5% 25V NPO-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6319 1000PF 5% 25V NPO-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6321 1000PF 5% 25V NPO-C0G 402 — SIGNAL_MODEL=EMPTY

L6308 FERR-1000-OHM 0402 — AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L
R6301 100K 5% 1/16W MF-LF 402 — NOSTUFF C6312 100PF 5% 50V CERM 402

R6308 0 5% 1/16W MF-LF 402 — AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L
R6309 100K 5% 1/16W MF-LF 402 — NOSTUFF C6318 100PF 5% 50V CERM 402

EDGE RATE CONTROL	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — AUD_LAMP_EDGE
NOSTUFF R6305 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402 — AUD_LAMP_MONO
NOSTUFF R6306 0 5% 1/16W MF-LF 402 — AUD_LAMP_GAIN
R6307 47K 5% 1/16W MF-LF 402

SYNC_MASTER=D8_DAVID SYNC_DATE=06/13/2012
PAGE TITLE: AUDIO: LEFT SPKR AMP

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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6400 10UF 10% 25V X5R 805
C6401 10UF 10% 25V X5R 805
C6402 0.1UF 10% 25V X5R 402
C6403 1UF 20% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL C6406 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

AUD_LO2_R_N → L6400 FERR-1000-OHM 0402 → AUD_RAMP_RINC_P → C6408 1UF 10% 25V X5R 0402 → AUD_RAMP_RIN_P
AUD_LO2_R_P → L6401 FERR-1000-OHM 0402 → AUD_RAMP_RINC_N → C6409 1UF 10% 25V X5R 0402 → AUD_RAMP_RIN_N
AUD_LO1_R_P → L6402 FERR-1000-OHM 0402 → AUD_RAMP_LINC_P → C6410 4700PF 5% 50V NPO-C0G-CERM 0805 → AUD_RAMP_LIN_P
AUD_LO1_R_N → L6403 FERR-1000-OHM 0402 → AUD_RAMP_LINC_N → C6411 4700PF 5% 50V NPO-C0G-CERM 0805 → AUD_RAMP_LIN_N

=PP3V3_S0_AUDIO

CRITICAL U6400 SSM3302 LFCSP

20	INR+	
19	INR-	
22	SDNR*	ONLY WOOFERS ON UNDER WINDOWS: AUD_SPKRAMP_WIN_SHDN_L
16	MONO	AUD_RAMP_MONO
9	SDNL*	WOOFERS & TWEETERS ON UNDER MAC OS: AUD_SPKRAMP_MAC_SHDN_L
11	INL+	
12	INL-	
21	GAIN	AUD_RAMP_GAIN
8	VREG/AVDD	AUD_RAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	
34,35,36,37	PVDD	
7,24,41	AGND	
31,32,33,38,39,40	PGND	
17	THERM	TP_AUD_RAMP_THERM = NC
30	BOOTR+	C6413 0.22UF 20% 25V X5R 603
28,29	OUTR+	AUD_RAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
26,27	OUTR-	AUD_RAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
25	BOOTR-	C6414 0.22UF 20% 25V X5R 603
10	EDGE	AUD_RAMP_EDGE
1	BOOTL+	C6415 0.22UF 20% 25V X5R 603
2,3	OUTL+	AUD_RAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
4,5	OUTL-	AUD_RAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
6	BOOTL-	C6416 0.22UF 20% 25V X5R 603
18	NC	NC
13	NC	NC
14	TEST	
15		

C6417 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_RAMP_OUTPR → SIGNAL_MODEL=EMPTY CRITICAL L6405 110-OHM-3A DLY5ATN111SQ2 → AUD_SPKR_RWFR_OUT_P
AUD_RAMP_OUTNR → SIGNAL_MODEL=EMPTY CRITICAL C6423 1000PF 5% 25V NPO-C0G 402 → AUD_SPKR_RWFR_OUT_N
AUD_RAMP_OUTPL → SIGNAL_MODEL=EMPTY CRITICAL L6407 110-OHM-3A DLY5ATN111SQ2 → AUD_SPKR_RTWT_OUT_P
AUD_RAMP_OUTNL → SIGNAL_MODEL=EMPTY CRITICAL C6424 1000PF 5% 25V NPO-C0G 402 → AUD_SPKR_RTWT_OUT_N

SIGNAL_MODEL=EMPTY CRITICAL C6420 1000PF 5% 25V NPO-C0G 402
SIGNAL_MODEL=EMPTY CRITICAL C6422 1000PF 5% 25V NPO-C0G 402 SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY CRITICAL C6419 1000PF 5% 25V NPO-C0G 402
CRITICAL C6421 1000PF 5% 25V NPO-C0G 402 SIGNAL_MODEL=EMPTY

EDGE RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_RAMP_AVDD
R6404 0 5% 1/16W MF-LF 402 → AUD_RAMP_EDGE
NOSTUFF R6405 0 5% 1/16W MF-LF 402
R6403 0 5% 1/16W MF-LF 402 → AUD_RAMP_MONO
NOSTUFF R6406 0 5% 1/16W MF-LF 402 → AUD_RAMP_GAIN
R6407 47K 5% 1/16W MF-LF 402

SYNC_MASTER=D8_DAVID SYNC_DATE=06/13/2012
PAGE TITLE: AUDIO: RIGHT SPKR AMP
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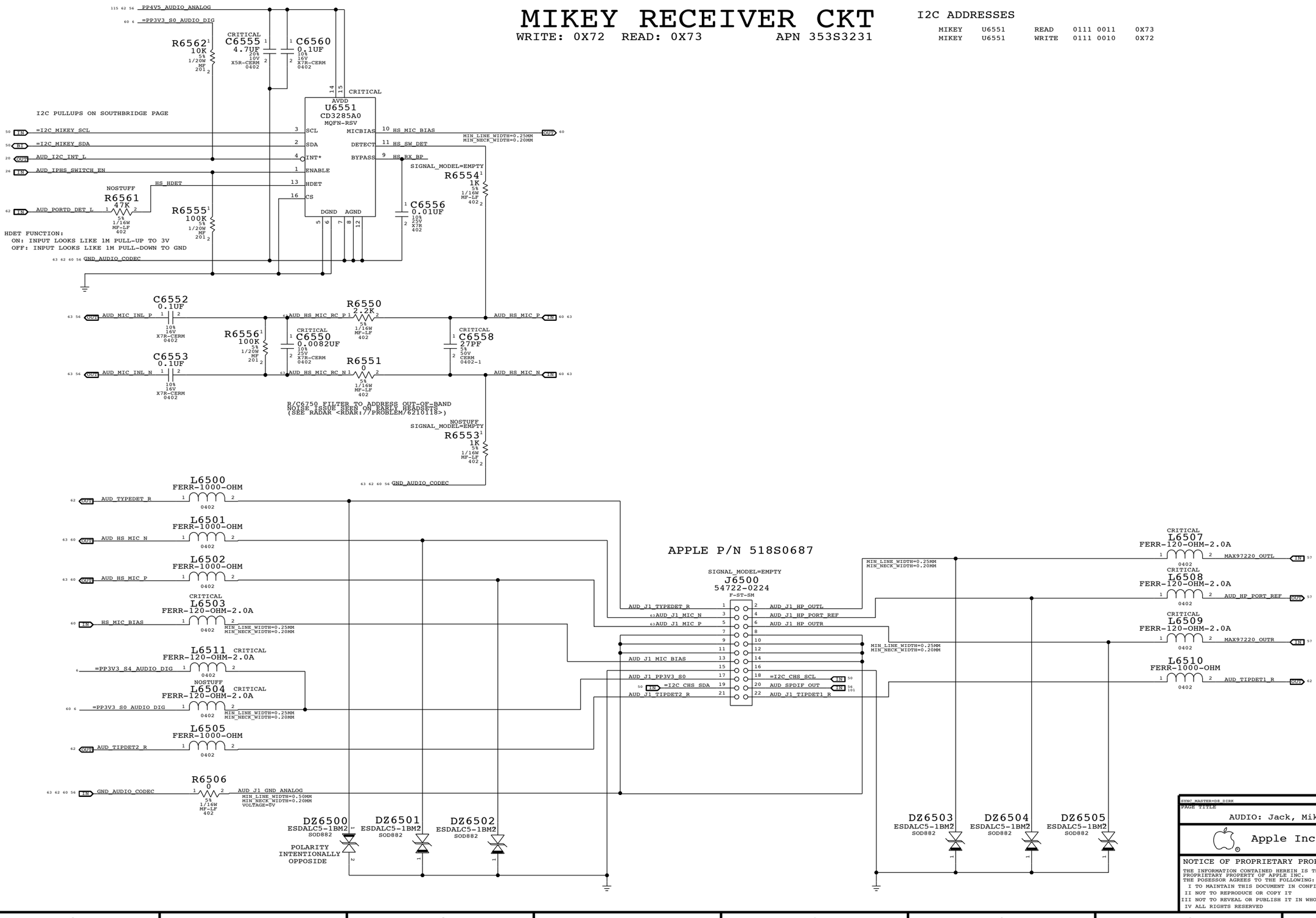
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=D8 DIRK SYNC_DATE=06/29/2017

PAGE TITLE

AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

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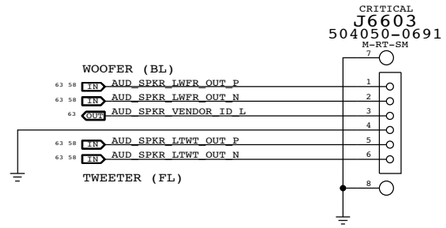
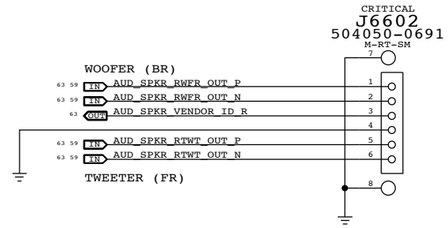
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862





SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE

Audio: Spkr/Mic Conn.

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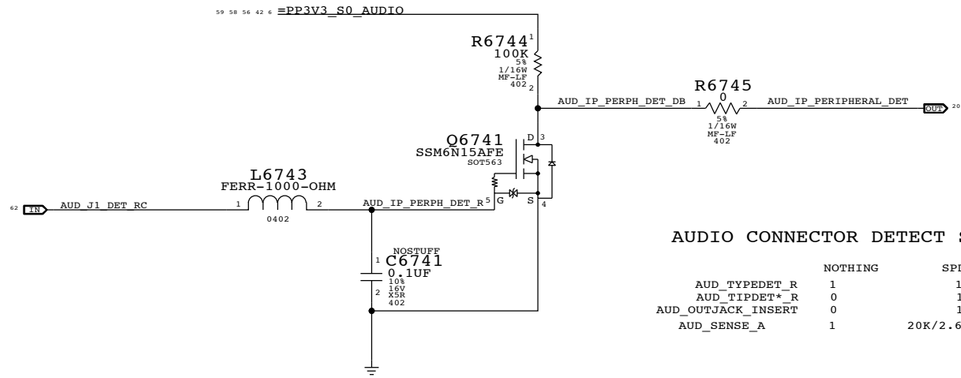
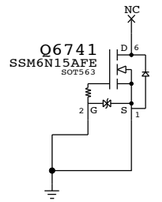
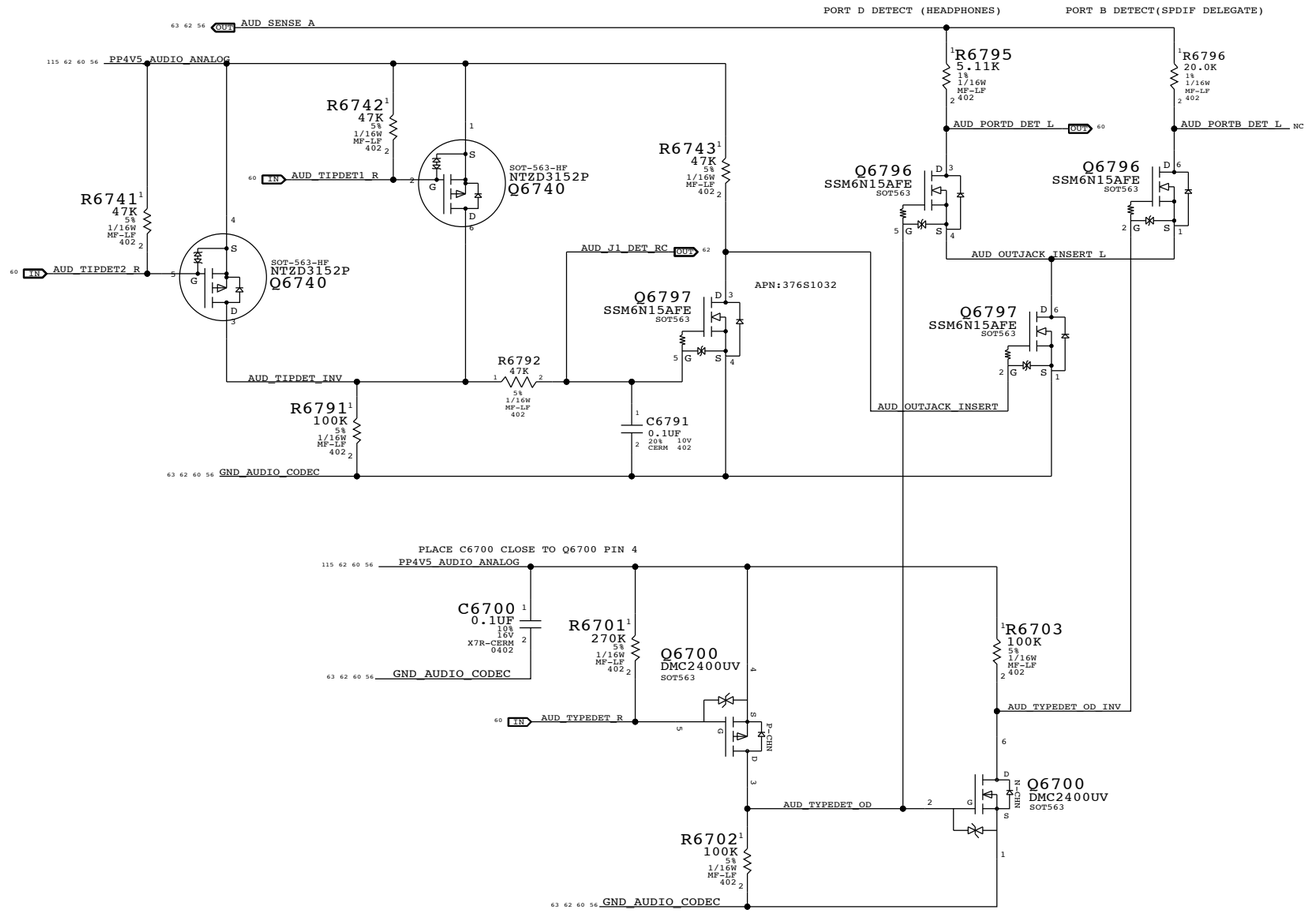
IPHS HS Detect Debounce CKT



AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





LI Insert Detect (DETECT A)

SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	PANTHER POINT GPIO 16	PANTHER POINT GPIO 5 (RCVR INT) PANTHER POINT GPIO 3 (PERIPH DET)

OTHER DETECT

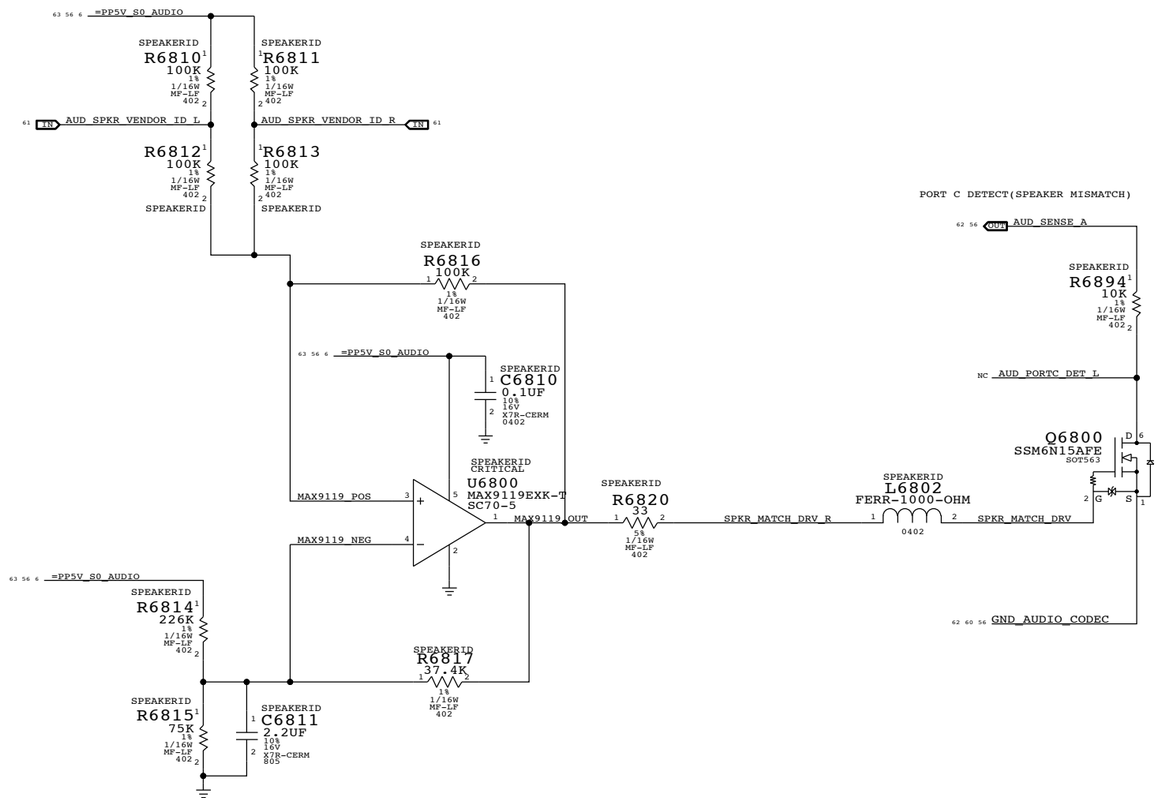
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



PORT C DETECT(SPEAKER MISMATCH)

NET_TYPE	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
P1A	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57 58
P1B	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57 58
P1C	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
P1D	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
P1E	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57 59
P1F	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57 59
P1G	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
P1H	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
P1J	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 58
P1K	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 58
P1L	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
P1M	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
P1N	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	59
P1P	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	59
P1Q	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	59
P1R	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	59
P1S	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	59
P1T	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	59
P1U	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	59
P1V	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	59
P1W	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	58
P1X	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	58
P1Y	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	58
P1Z	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	58
P1AA	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	58
P1AB	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	58
P1AC	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	58
P1AD	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	58
P1AE	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
P1AF	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
P1AG	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
P1AH	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
P1AJ	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	59 61
P1AK	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	59 61
P1AL	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	59 61
P1AM	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	59 61
P1AN	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	58 61
P1AP	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	58 61
P1AR	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	58 61
P1AS	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	58 61
P1AT	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	56 60
P1AU	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	56 60
P1AV	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	60
P1AW	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	60
P1AK	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	60
P1AY	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	60
P1AZ	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	60
P1B0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	60

SYNC_MASTER=D8_DAVID SYNC_DATE=06/13/2012

PAGE TITLE: AUDIO: Speaker ID

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D
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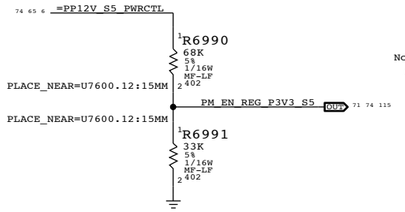
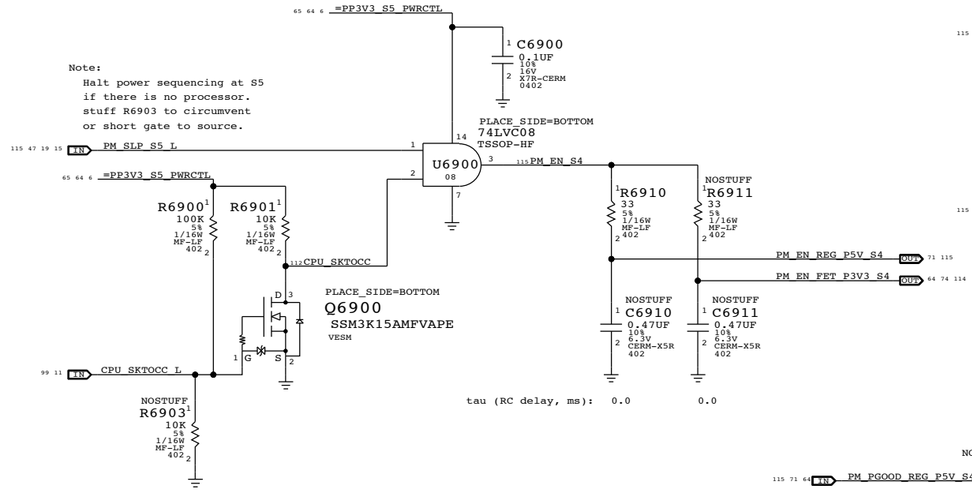
S5 3V3 Soft Enable



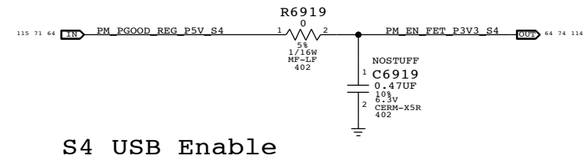
Note:
Expected 3.9V +/- 0.4V EN signal

S4 5V Enable

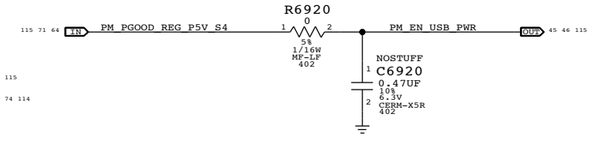


tau (RC delay, ms): 0.0 0.0

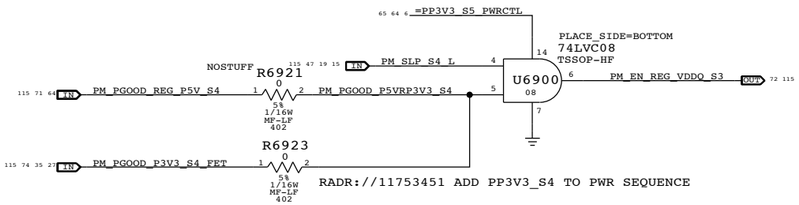
S4 3V3 Enable



S4 USB Enable

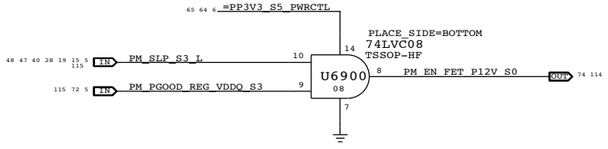


S3 1V5 Reg (S0/S3) Enable



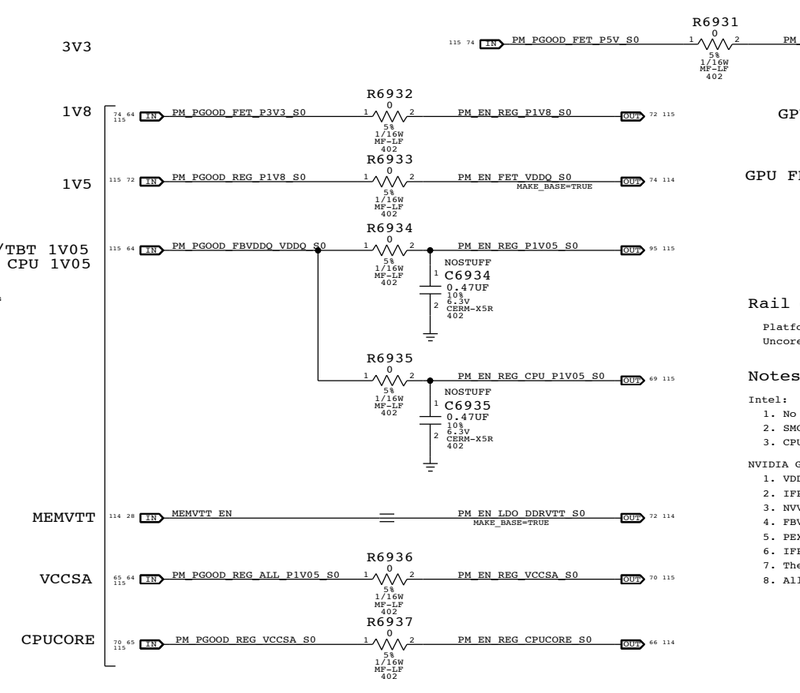
RADR://11753451 ADD PP3V3_S4 TO PWR SEQUENCE

S0 12V Enable

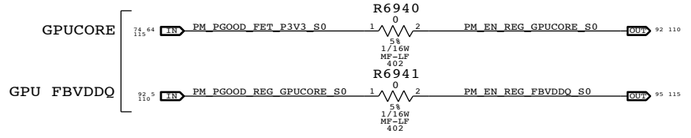


S0 Platform Parallel Sequence Enable

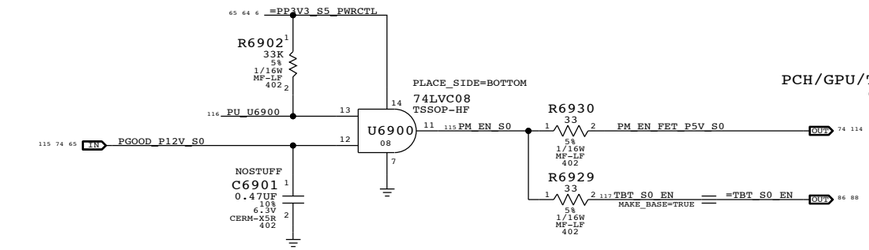
CPU/PCH Sequencing



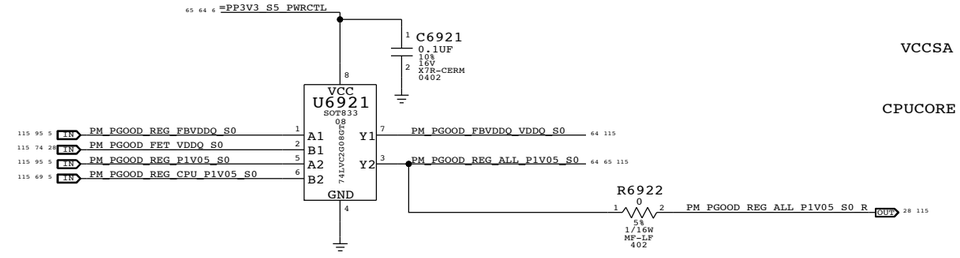
GPU Sequencing



S0 5V and TBT Enable



Parallel Enable PGOOD combinator



Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. CPU VDDQ must ramp before MEMVTT and vice versa on power down. It has no relationship to any other rails.

NVIDIA GFX:
1. VDD33 (our 3V3_S0)
2. IFPA/B_IOVDD (1.8 V) with or after 3V3_S0 (unused in our implementation)
3. NVVDD (our GPUCORE) after IFPA/B_IOVDD
4. FBVDDQ (our GPU_VDDQ) after NVVDD
5. PEX_VDD (our GPU_1V05) after FBVDDQ
6. IFPC/D/E/F_IOVDD (1.05V) wit or after PEX_VDD
7. The ramp time for any rail must be more than 40 uS
8. All rails must be powered off within 10 ms from first rail powering off

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PM Regulator Enables

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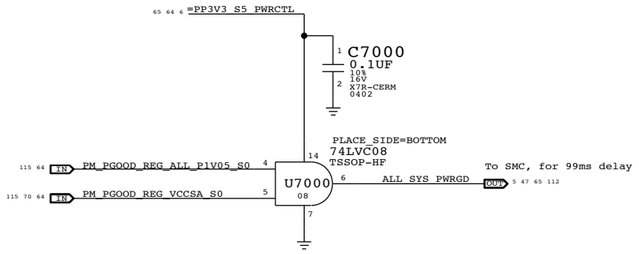
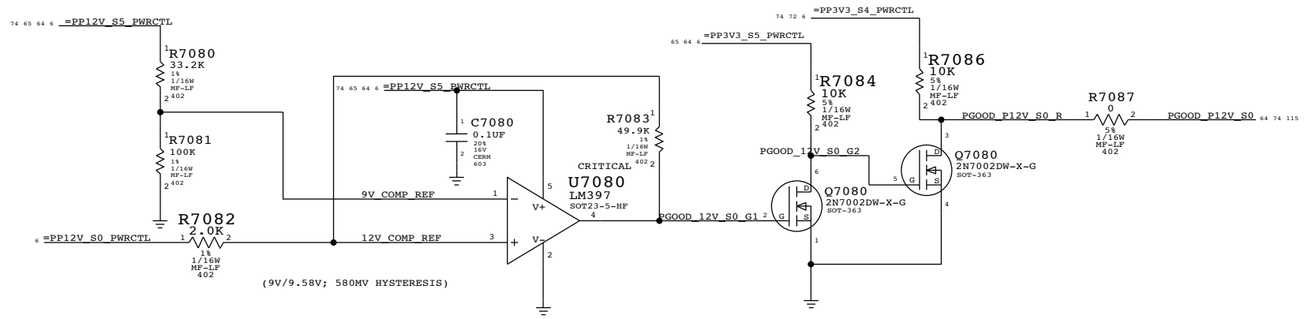
Platform Power Good Derive SMC ALL_SYS_PWRGD

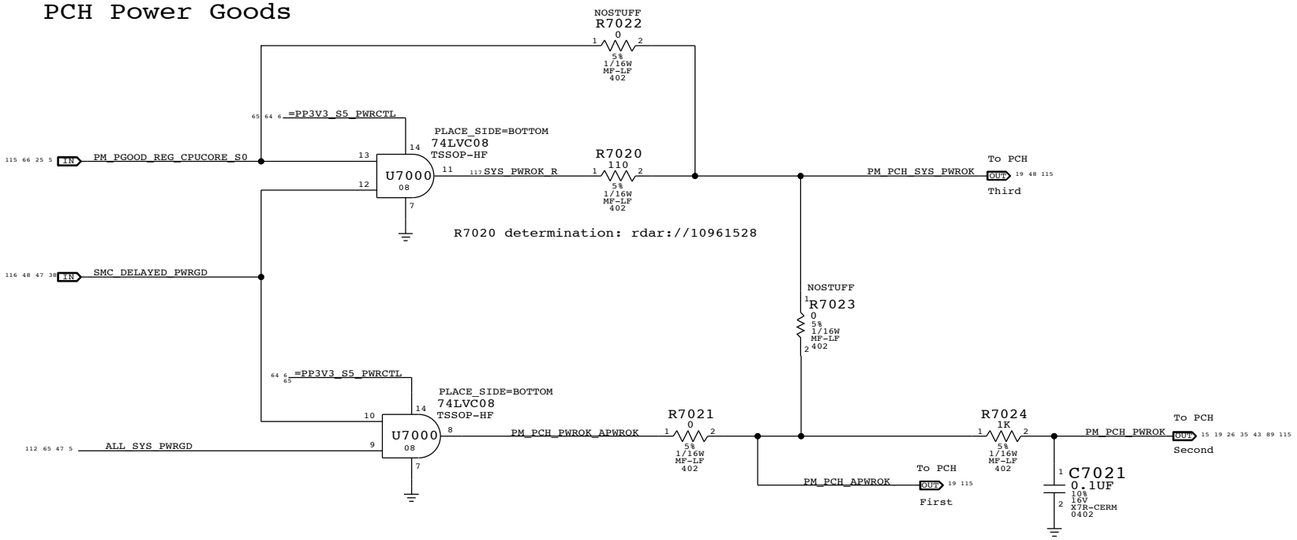
The end of the power sequence for S0 rails except CPU CORE.



PGOOD COMPARATORS FOR PP12V_S0



PCH Power Goods



Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

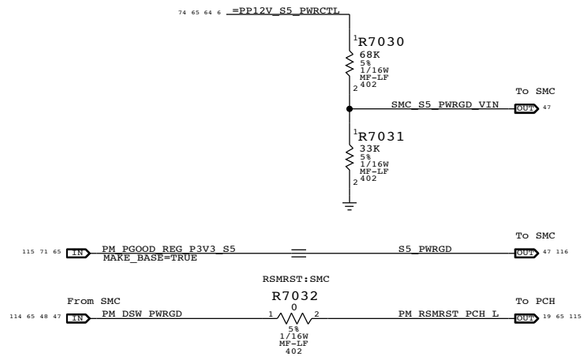
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

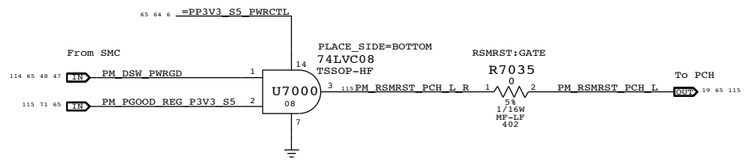
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.



Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



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PM Power Good

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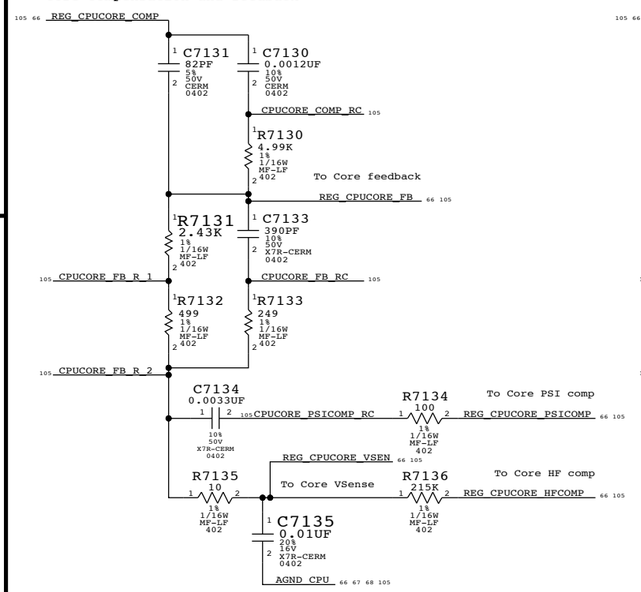
CPU Core S0 Regulator

Max avg current: 63 A (BUDGET)
Max peak current: 110 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

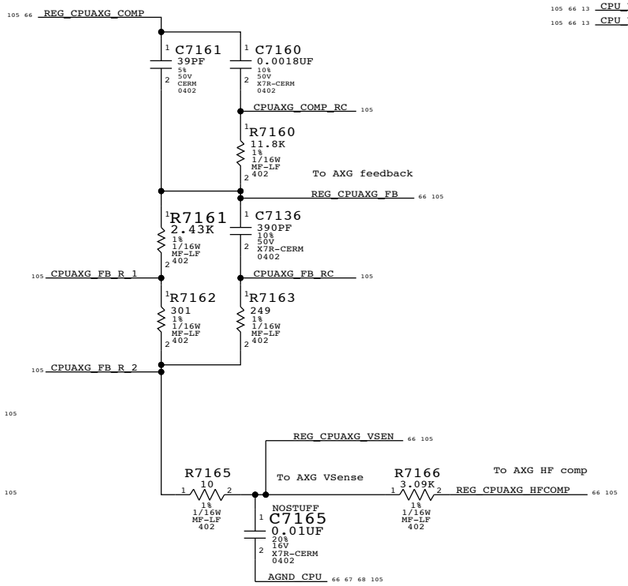
Core compensation and feedback



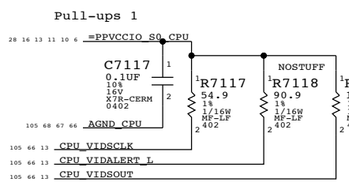
CPU AXG S0 Regulator

Max avg current: 12.7 A (BUDGET)
Max peak current: 30.0 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

AXG compensation and feedback

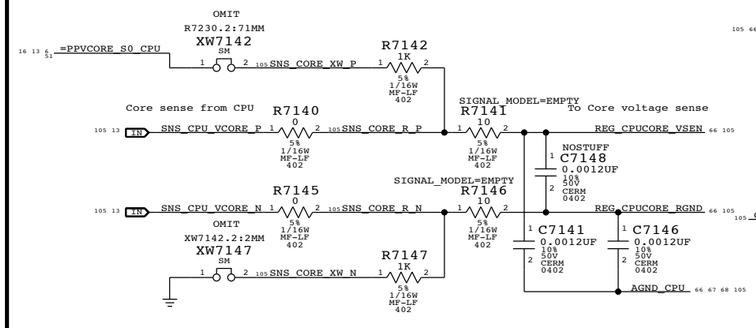


Pull-ups 1

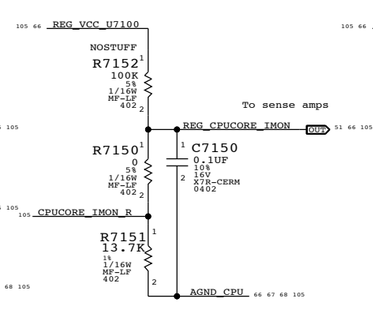


Pull-ups 2

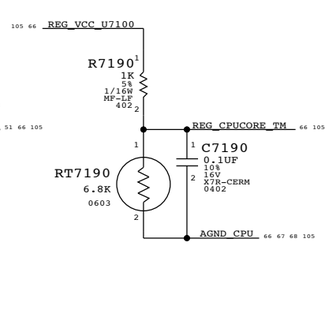
Core voltage sense input



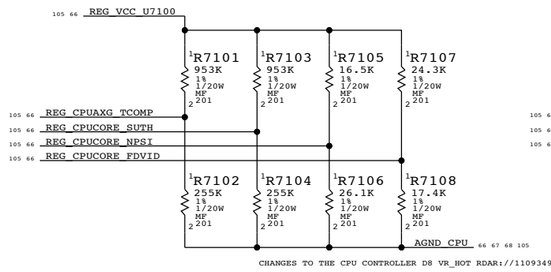
Core IMON output



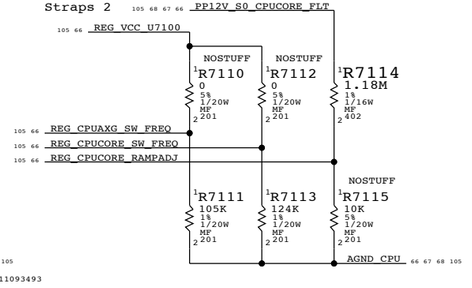
Core temp measurement



Straps 1

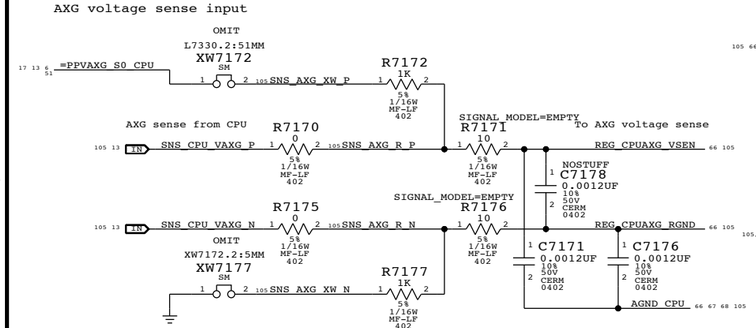


Straps 2

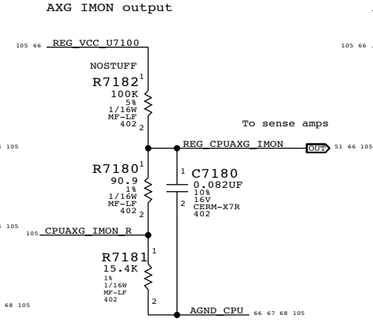


CHANGES TO THE CPU CONTROLLER D8 VR_HOT RDAR://11093493

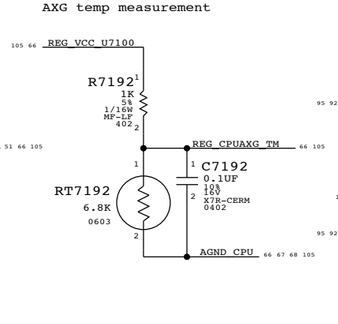
AXG voltage sense input



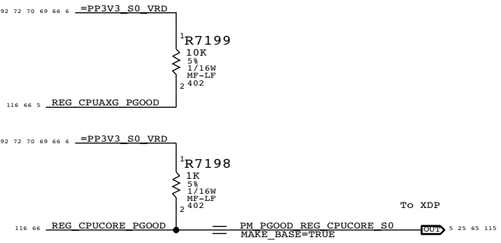
AXG IMON output



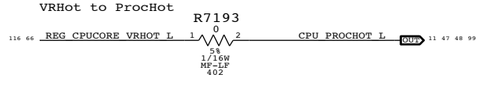
AXG temp measurement



Power goods



VRHot to ProcHot



SYNC_MASTER=D8 MLB SYNC_DATE=02/28/2012

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VReg CPU Core/AXG Cntl

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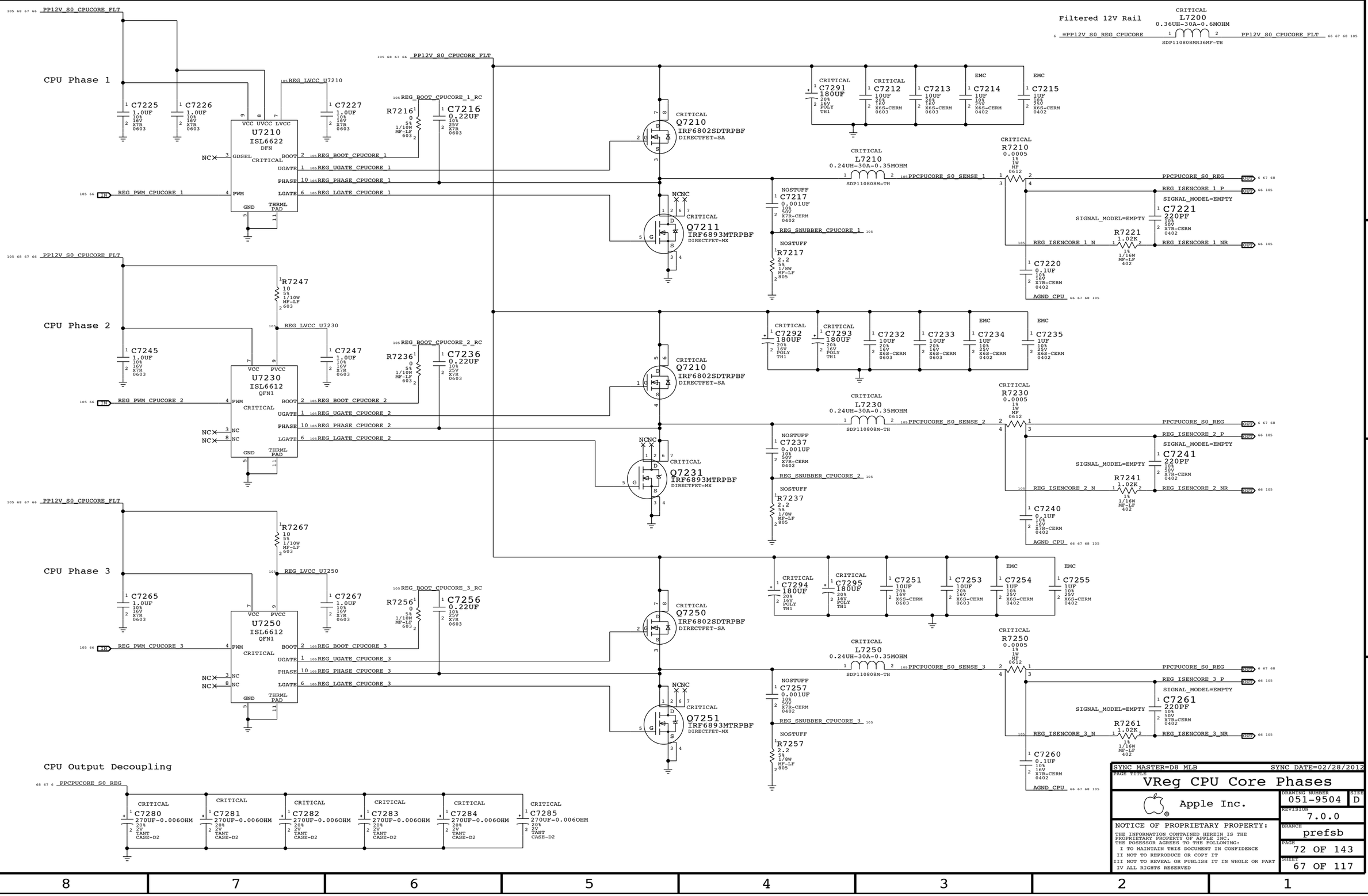
PP12V_S0_CPUCORE_FLT
CPU Phase 1
U7210
ISL6622
DFN
REG_LVCC_U7210
REG_BOOT_CPUCORE_1_RC
REG_PWM_CPUCORE_1
REG_BOOT_CPUCORE_1
REG_UGATE_CPUCORE_1
REG_PHASE_CPUCORE_1
REG_LGATE_CPUCORE_1
Q7210
IRF6802SDTRPBF
DIRECTFET-SA
Q7211
IRF6893MTRPBF
DIRECTFET-MX
CPU Phase 2
U7230
ISL6612
QFN1
REG_LVCC_U7230
REG_BOOT_CPUCORE_2_RC
REG_PWM_CPUCORE_2
REG_BOOT_CPUCORE_2
REG_UGATE_CPUCORE_2
REG_PHASE_CPUCORE_2
REG_LGATE_CPUCORE_2
Q7231
IRF6893MTRPBF
DIRECTFET-MX
CPU Phase 3
U7250
ISL6612
QFN1
REG_LVCC_U7250
REG_BOOT_CPUCORE_3_RC
REG_PWM_CPUCORE_3
REG_BOOT_CPUCORE_3
REG_UGATE_CPUCORE_3
REG_PHASE_CPUCORE_3
REG_LGATE_CPUCORE_3
Q7250
IRF6802SDTRPBF
DIRECTFET-SA
Q7251
IRF6893MTRPBF
DIRECTFET-MX
CPU Output Decoupling
PPCPUCORE_S0_REG
Filtered 12V Rail
L7200
0.36UH-30A-0.6MOHM
SDP110808MR36MF-TH
=PP12V_S0_REG_CPUCORE
PP12V_S0_CPUCORE_FLT
L7210
L7230
L7250
0.24UH-30A-0.35MOHM
SDP110808M-TH
PPCPUCORE_S0_SENSE_1
PPCPUCORE_S0_SENSE_2
PPCPUCORE_S0_SENSE_3
R7210
R7230
R7250
0.0005
REG_ISENCORE_1_P
REG_ISENCORE_1_N
REG_ISENCORE_2_P
REG_ISENCORE_2_N
REG_ISENCORE_3_P
REG_ISENCORE_3_N
SIGNAL_MODEL=EMPTY
REG_SNUBBER_CPUCORE_1
REG_SNUBBER_CPUCORE_2
REG_SNUBBER_CPUCORE_3
AGND_CPU
SYNC_MASTER=D8_MLB
SYNC_DATE=02/28/2012
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VReg CPU Core Phases
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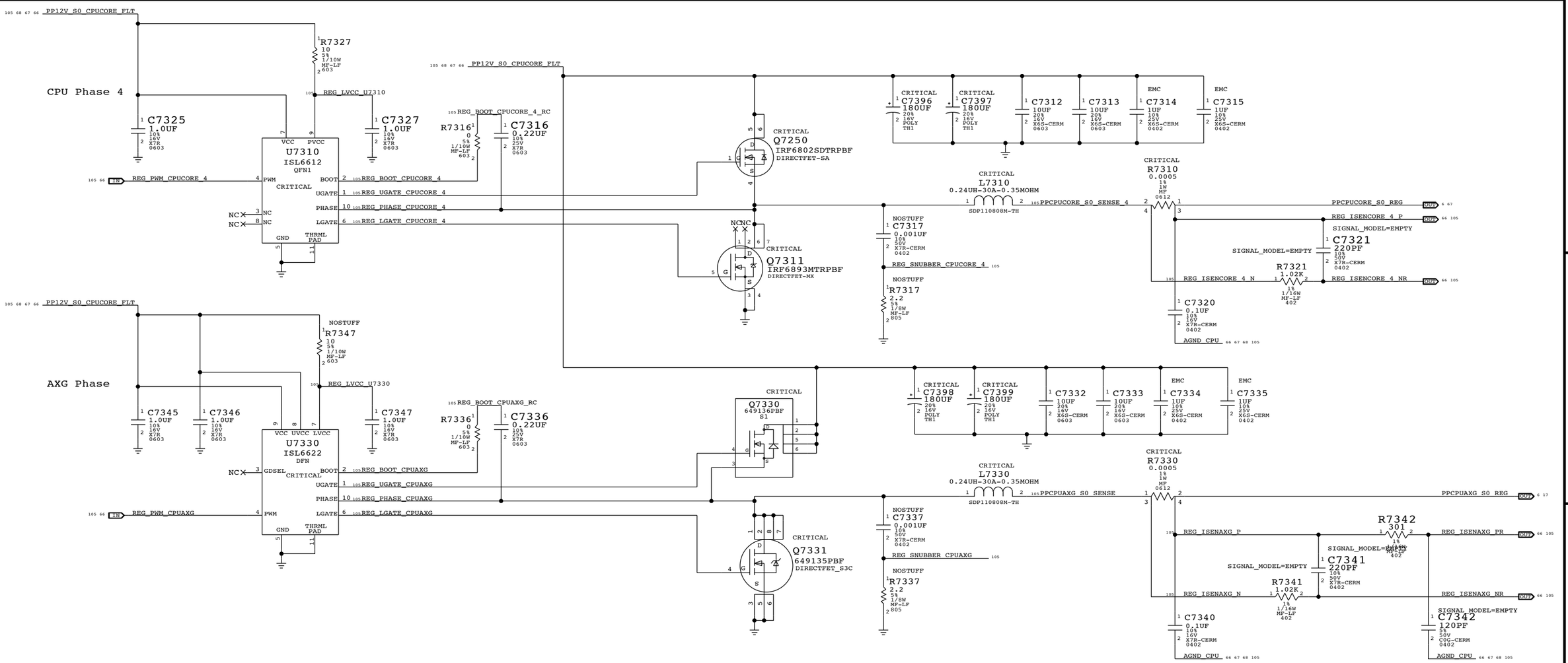

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VReg CPU AXG Phases

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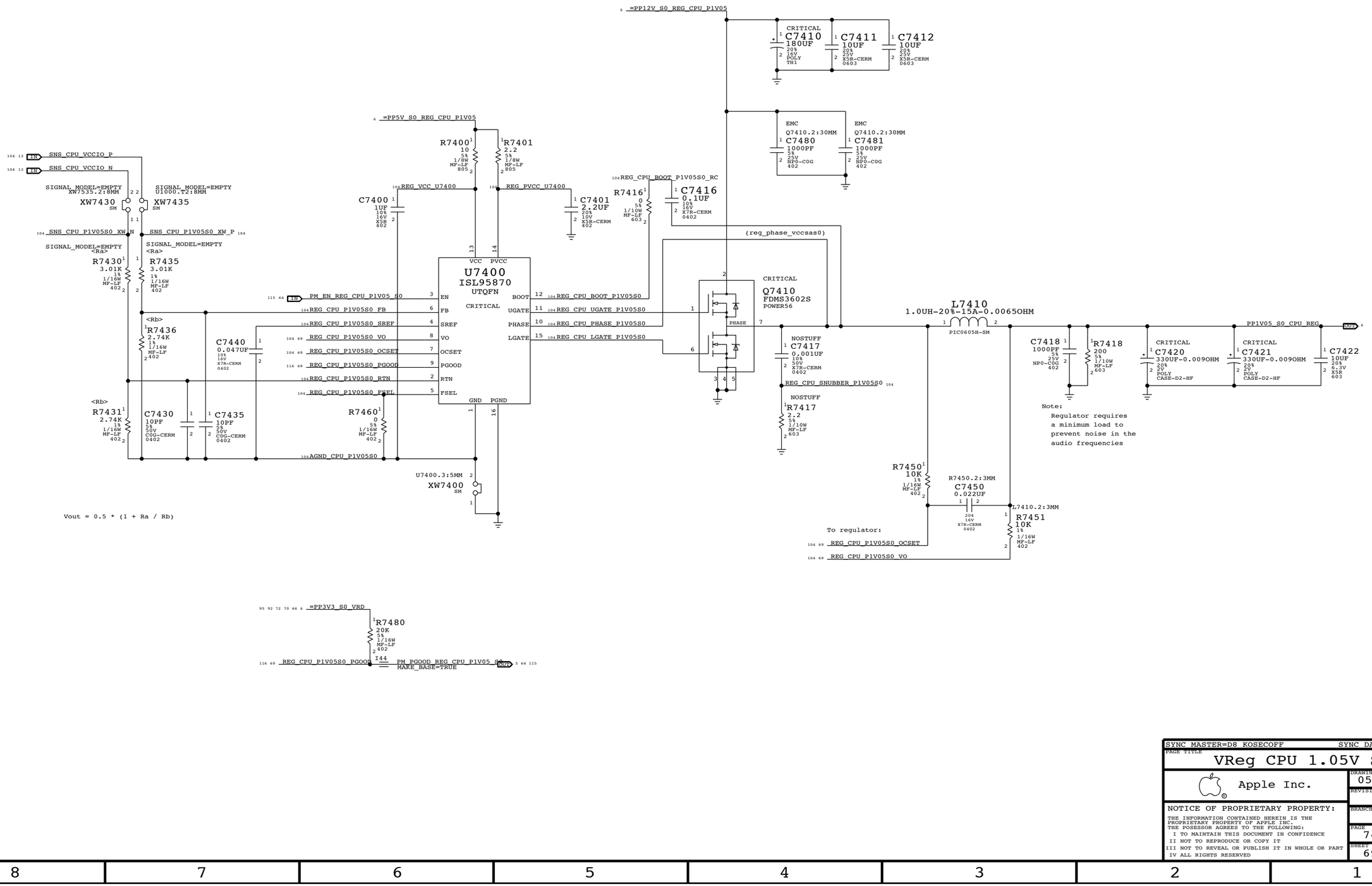
CPU VccIO (1.05V) S0 Regulator

Max avg current: 8.10 A (BUDGET)
Max peak current: 8.50 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



Vout = 0.5 * (1 + Ra / Rb)

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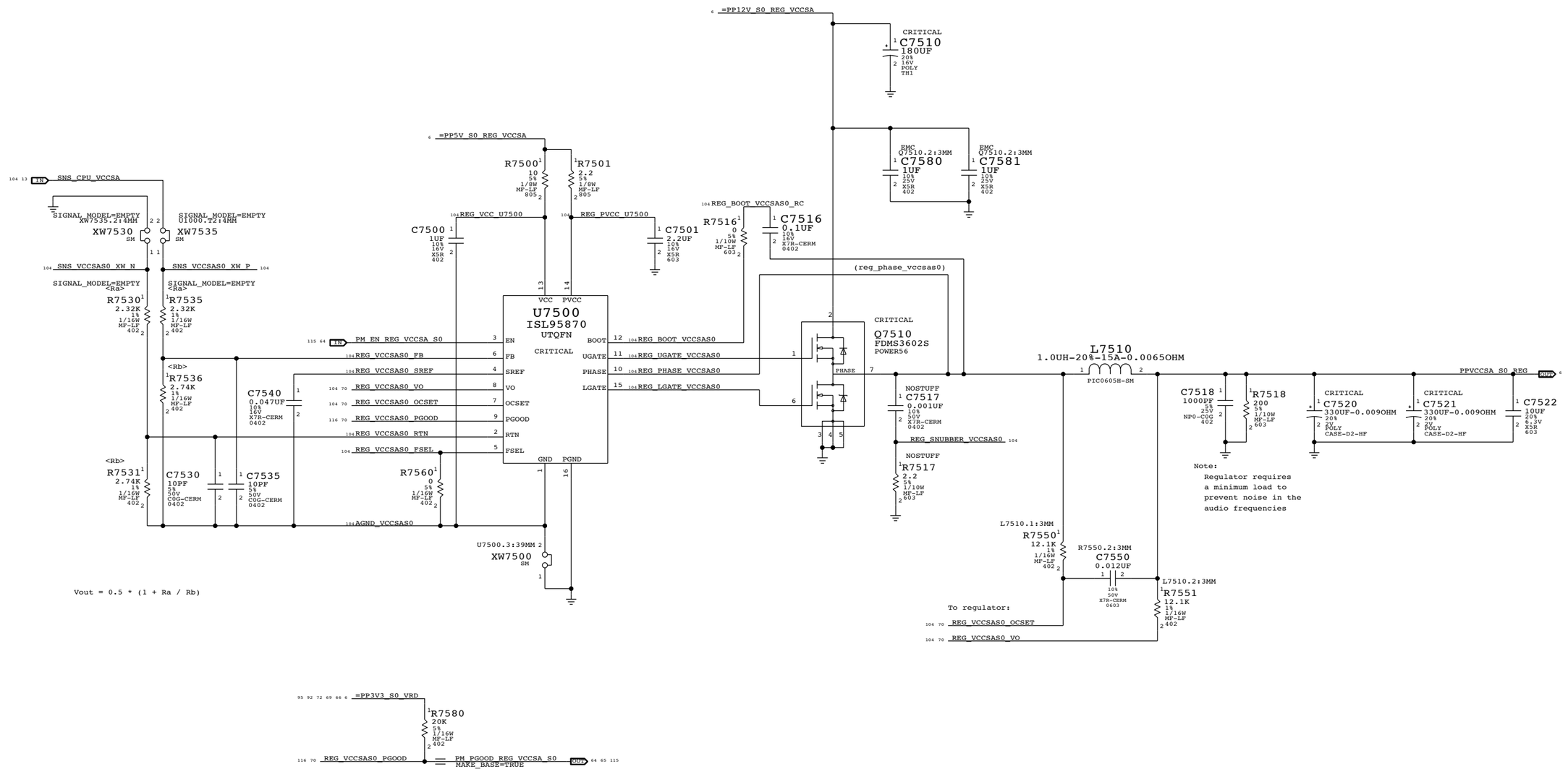
CPU VccSA (0.925V) S0 Regulator

Max avg current: 12.07 A (BUDGET)
Max peak current: 30 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



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VReg CPU VccSA S0

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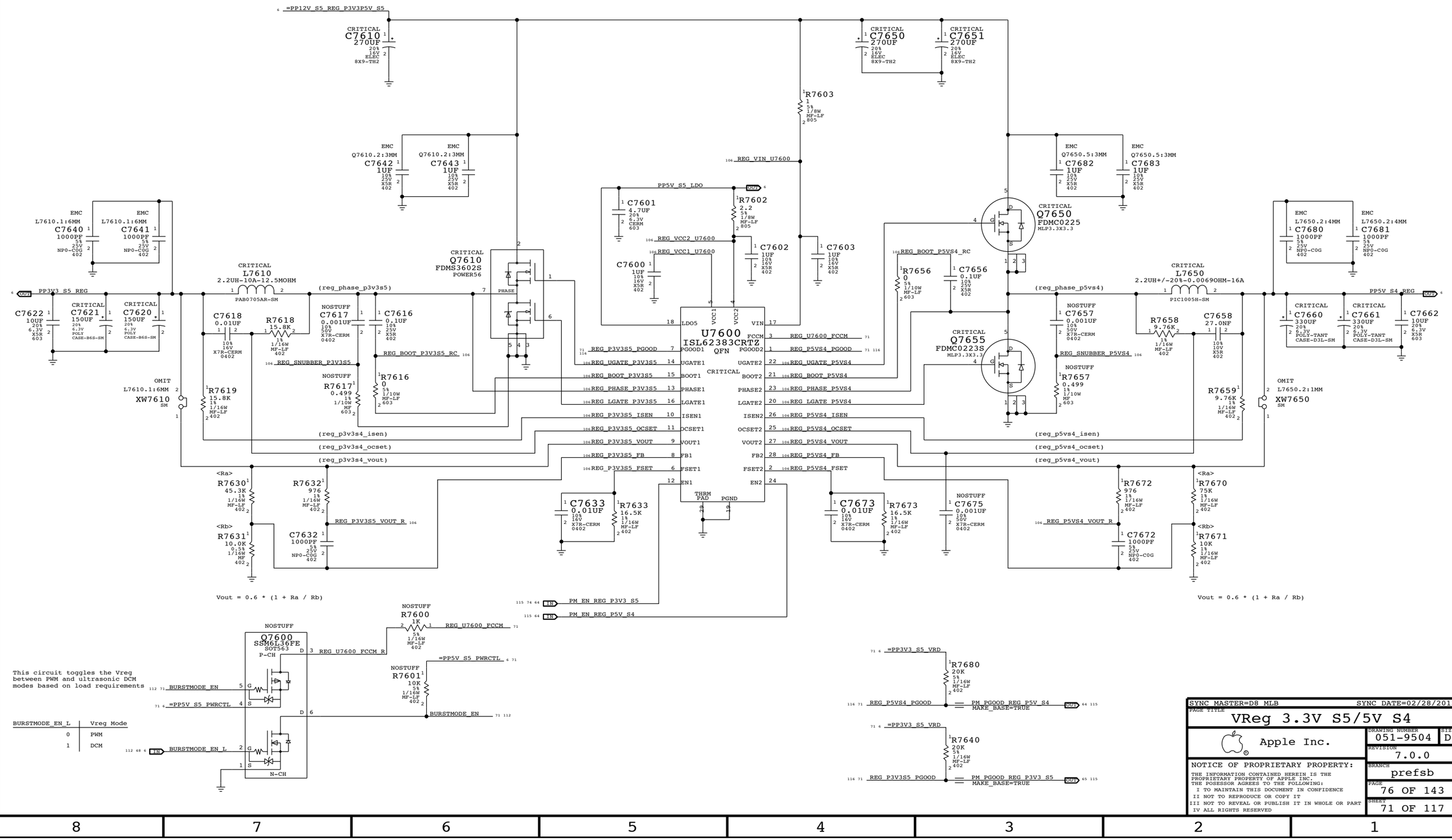
3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz



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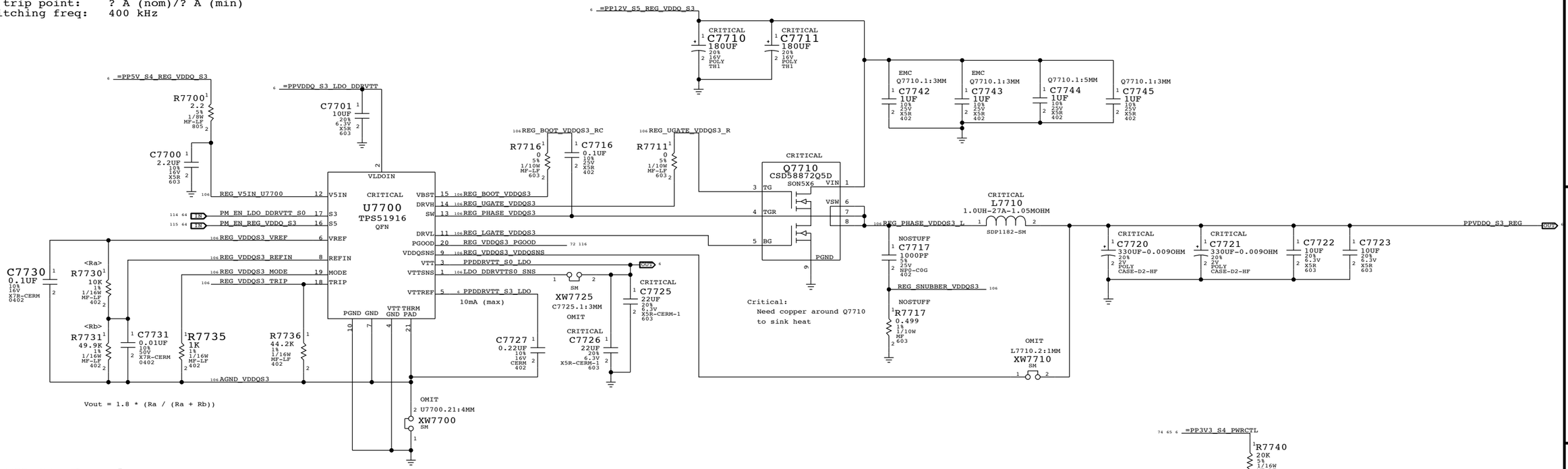
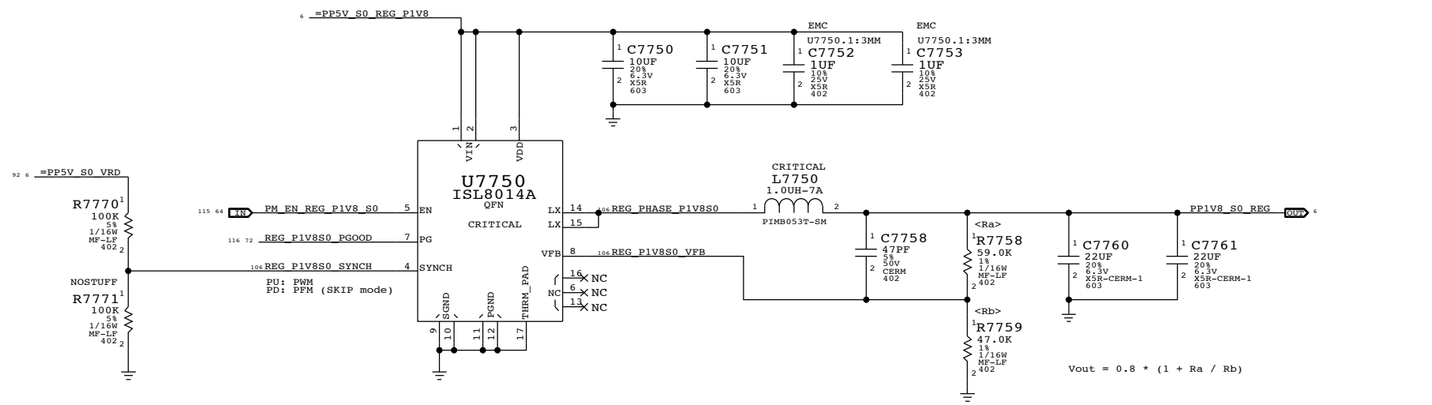
VDDQ (1.5V) S3 Regulator

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz



1.8V S0 Regulator

Max avg current: 0.6 A (BUDGET)
Max peak current: 1.7 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



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VReg VDDQ and 1.8V S0

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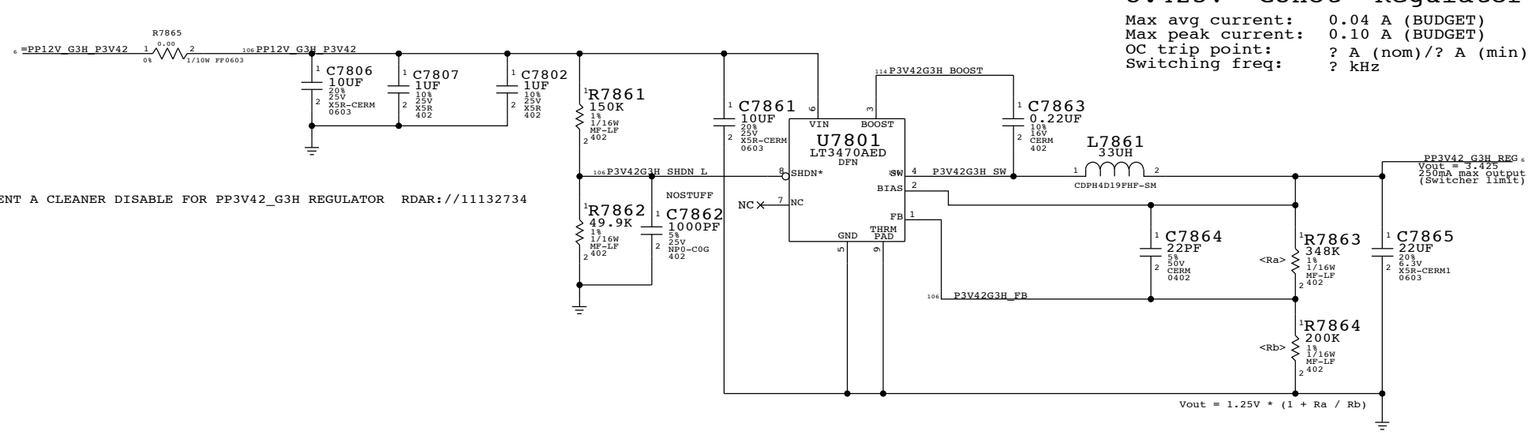
D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734

3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



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Apple Inc.	DRAWING NUMBER: 051-9504 SIZE: D
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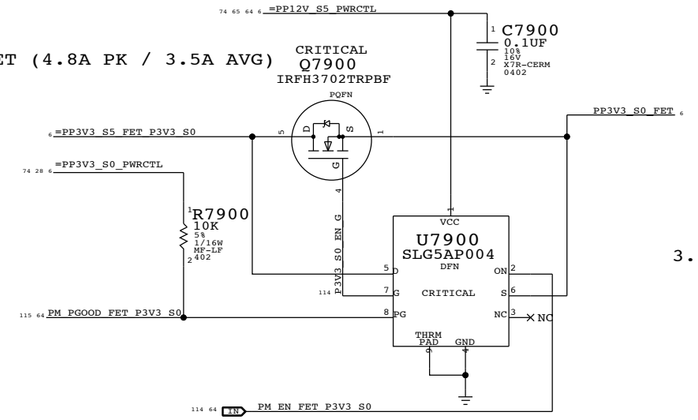
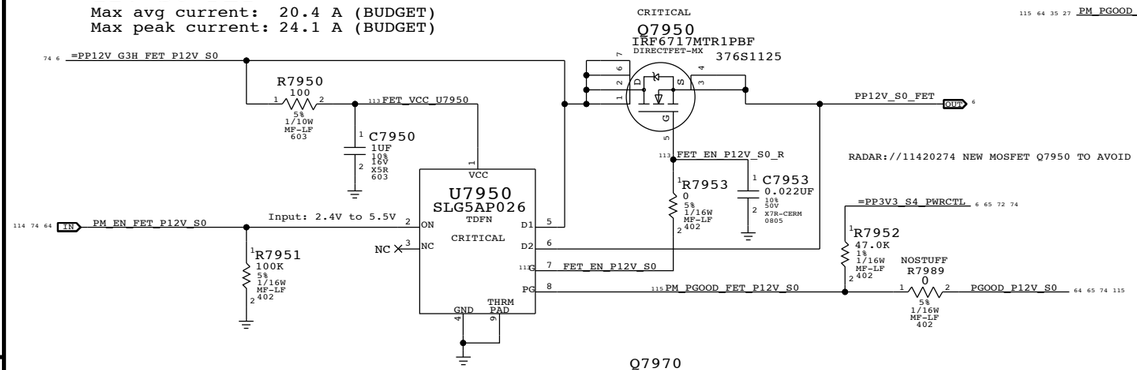
3.3V S0 FET (4.8A PK / 3.5A AVG)



12V S0 FET

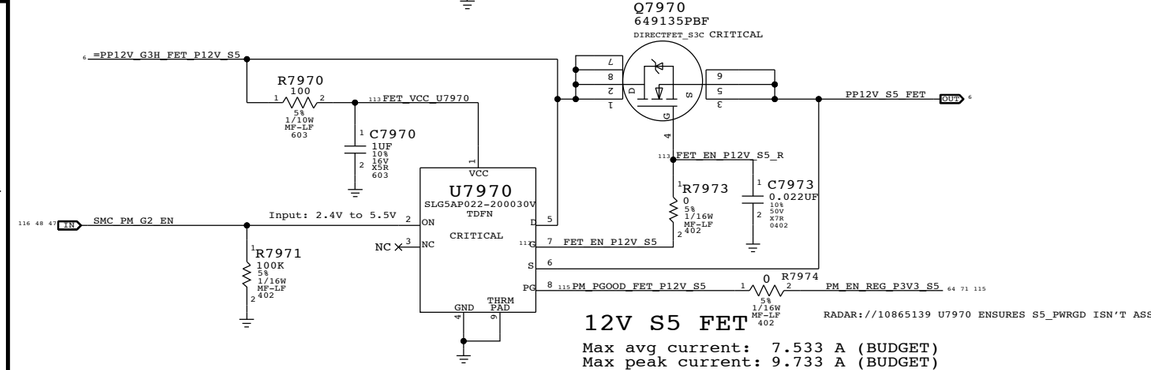
Max avg current: 20.4 A (BUDGET)
Max peak current: 24.1 A (BUDGET)



RADAR://11420274 NEW MOSFET Q7950 TO AVOID 50A 100US PULSE ON 12V S0.

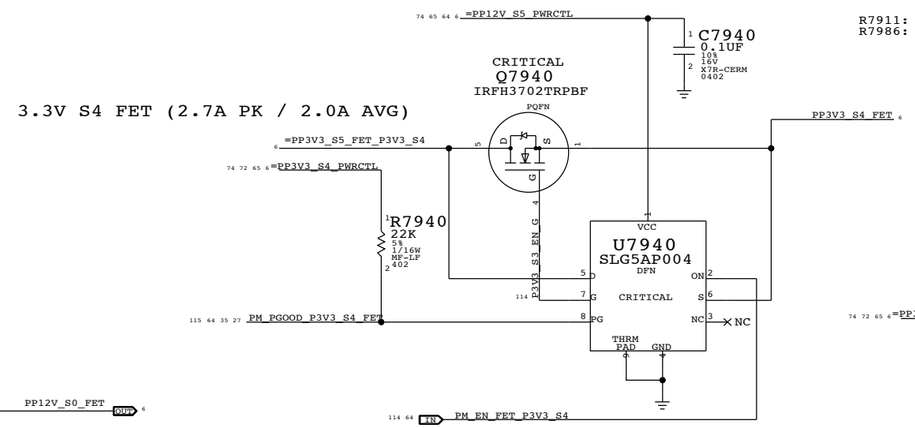
12V S5 FET

Max avg current: 7.533 A (BUDGET)
Max peak current: 9.733 A (BUDGET)



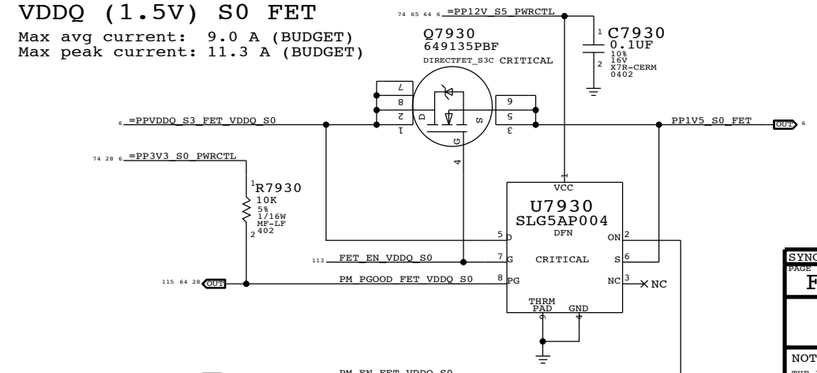
RADAR://10865139 U7970 ENSURES S5_PWRGD ISN'T ASSERTED AFTER HARD SHUTDOWN.

3.3V S4 FET (2.7A PK / 2.0A AVG)



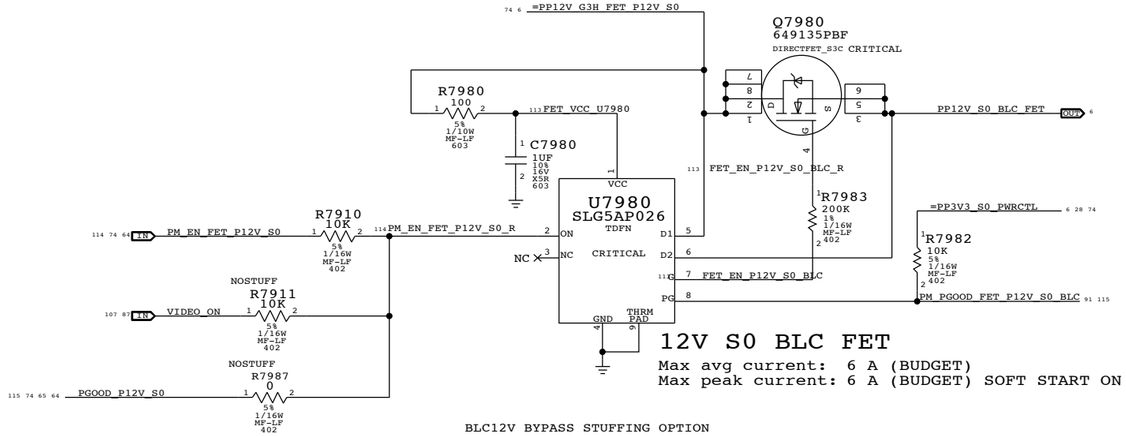
VDDQ (1.5V) S0 FET

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)



12V S0 BLC FET

Max avg current: 6 A (BUDGET)
Max peak current: 6 A (BUDGET) SOFT START ON BLC

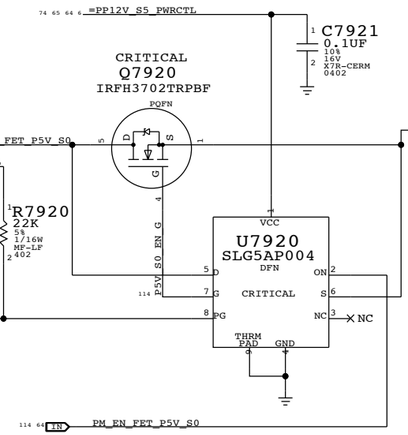


BLC12V BYPASS STUFFING OPTION

	BYPASS	NO BYPASS
R7911:	STUFF	NOSTUFF
R7986:	STUFF	NOSTUFF

5V S0 FET

Max avg current: 2.7 A (BUDGET)
Max peak current: 3.9 A (BUDGET)



SYNC MASTER=D8 MLB	SYNC DATE=05/14/2012
PAGE TITLE	FET-Controlled S0 and S4
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
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	SHEET 74 OF 117

Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

ALL LANES ARE REVERSED AND LANES 10,8,7,6,5,3,2,1 ARE POLARITY SWAPPED

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All CA*: 0.22UF, GND_VOID=TRUE, 20% 6.3V X5R 0201

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All CA*: 0.22UF, GND_VOID=TRUE, 20% 6.3V X5R 0201

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OMIT_TABLE

U8000
NV-GK107
BGA
(1 OF 10)

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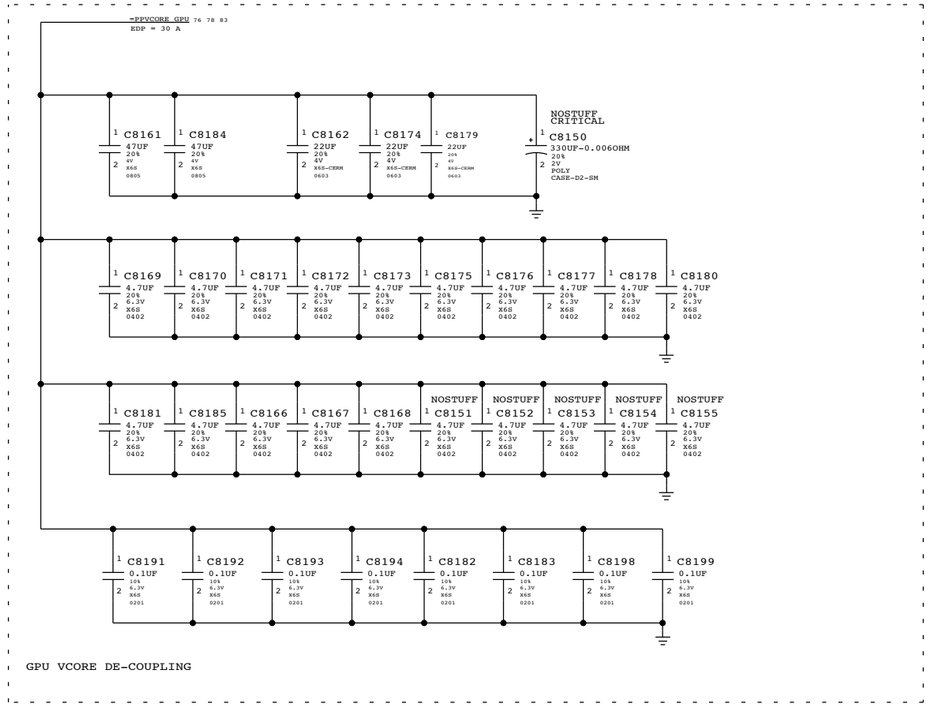
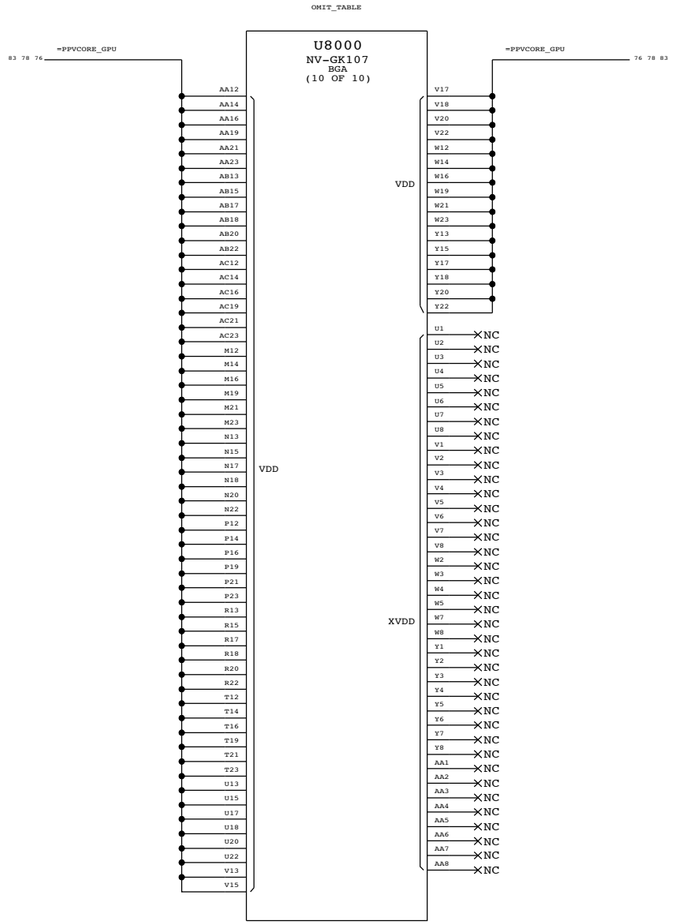
R8002 200 (MOSTUFF)

R8005 2.49K

SYNC_MASTER=D8_AARON	SYNC_DATE=03/13/2012
PAGE TITLE: KEPLER PCI-E	
Apple Inc.	DRAWING NUMBER: 051-9504 SIZE: D
	REVISION: 7.0.0
	BRANCH: prefsb
	PAGE: 80 OF 143
	SHEET: 75 OF 117

DE-COUPLING IS BASED ON NV DESIGN GUIDELINE DG-05587-001





Page Notes

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Signal aliases required by this page:

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BOM options provided by this page.

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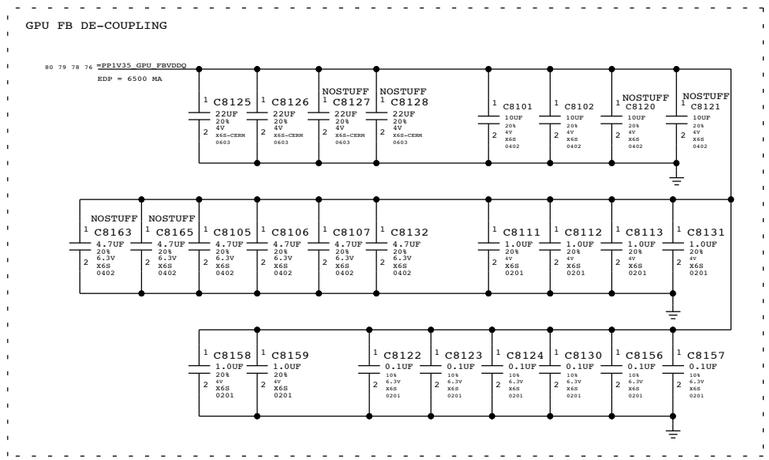

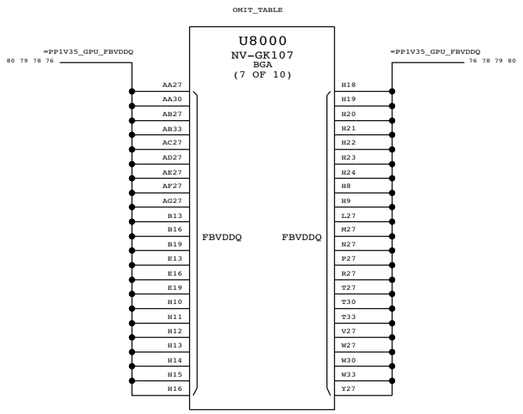

SYNC MASTER=D8 YAN SYNC DATE=04/09/2012

PAGE TITLE
KEPLER CORE/FB POWER

Apple Inc.

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NOTE:GDDR5 MODE N MAPPING

OMIT_TABLE

U8000
NV-GK107
BGA
(3 OF 10)
MEM INTERFACE A

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			U29	FBA_CMD2	
			R34	FBA_CMD3	
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			U32	FBA_CMD5	
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			Y32	FBA_CMD15	
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			Y30	FBA_CMD26	
			AA34	FBA_CMD27	
			Y31	FBA_CMD28	
			Y34	FBA_CMD29	
			Y33	FBA_CMD30	
			V31	FBA_CMD31	
			R30	FBA_CLK0	
			R31	FBA_CLK0*	
			AB31	FBA_CLK1	
			AC31	FBA_CLK1*	
			P30	FBA_DQM0	
			P31	FBA_DQM1	
			P34	FBA_DQM2	
			M32	FBA_DQM3	
			AD31	FBA_DQM4	
			AL29	FBA_DQM5	
			AM32	FBA_DQM6	
			AF34	FBA_DQM7	
			M30	FBA_DQS_RN0	NC
			H30	FBA_DQS_RN1	NC
			E34	FBA_DQS_RN2	NC
			M34	FBA_DQS_RN3	NC
			AF30	FBA_DQS_RN4	NC
			AH31	FBA_DQS_RN5	NC
			AH34	FBA_DQS_RN6	NC
			AF32	FBA_DQS_RN7	NC
			M31	FBA_DQS_WP0	
			G31	FBA_DQS_WP1	
			E33	FBA_DQS_WP2	
			M33	FBA_DQS_WP3	
			AE31	FBA_DQS_WP4	
			AK30	FBA_DQS_WP5	
			AN33	FBA_DQS_WP6	
			AF33	FBA_DQS_WP7	
			K27	FBA_DLL_AVDD	
			U27	FBA_PLL_AVDD	
			R28	FBA_DEBUG	
			AC28	FBA_DEBUG	
			J27	FB_CAL_PD_VDDQ	
			H27	FB_CAL_PU_GND	
			H25	FB_CAL_TERM_GND	
			E1	FB_CLAMP	
			R32	FBA_CMD_RFU	NC
			AC32	FBA_CMD_RFU	NC
			F1	FB_VDDQ_SENSE	
			F2	FB_GND_SENSE	

108 79	B1	FB_A0_DBI_L<0>	P30	FBA_DQM0	
108 79	B1	FB_A0_DBI_L<1>	P31	FBA_DQM1	
108 79	B1	FB_A0_DBI_L<2>	P34	FBA_DQM2	
108 79	B1	FB_A0_DBI_L<3>	M32	FBA_DQM3	
108 79	B1	FB_A1_DBI_L<0>	AD31	FBA_DQM4	
108 79	B1	FB_A1_DBI_L<1>	AL29	FBA_DQM5	
108 79	B1	FB_A1_DBI_L<2>	AM32	FBA_DQM6	
108 79	B1	FB_A1_DBI_L<3>	AF34	FBA_DQM7	
108 79	IN	FB_A0_EDC<0>	M31	FBA_DQS_WP0	
108 79	IN	FB_A0_EDC<1>	G31	FBA_DQS_WP1	
108 79	IN	FB_A0_EDC<2>	E33	FBA_DQS_WP2	
108 79	IN	FB_A0_EDC<3>	M33	FBA_DQS_WP3	
108 79	IN	FB_A1_EDC<0>	AE31	FBA_DQS_WP4	
108 79	IN	FB_A1_EDC<1>	AK30	FBA_DQS_WP5	
108 79	IN	FB_A1_EDC<2>	AN33	FBA_DQS_WP6	
108 79	IN	FB_A1_EDC<3>	AF33	FBA_DQS_WP7	

108 79 77 FB_A0_RESET_L

R8250 10K 1% 1/20W MF 201

108 79 77 FB_A1_RESET_L

R8251 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 77 78

R8252 10K 1% 1/20W MF 201

R8253 10K 1% 1/20W MF 201

108 79 77 FB_A0_CKE_L

108 79 77 FB_A1_CKE_L

=PP1V35_GPU_S0_FB 77 78

NOSTUFF R8258 1.33K 1% 1/20W MF 201

PLACE_NEAR=U8000.R26:6.6MM

FB_VREF 77 113

PLACE_NEAR=U8000.R26:6.6MM

NOSTUFF R8259 1.33K 1% 1/20W MF 201

NOSTUFF C8260 0.1UF 10% 6.3V X5R 201

FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB 77 78

NOSTUFF R8203 60.4 1% 1/20W MF 201

NOSTUFF R8202 60.4 1% 1/20W MF 201

NOSTUFF R8270 100 5% 1/20W MF 201

FB_DLL_AVDD PP1V05_GPU_FB_DLL_AVDD 77 115

FBA_PLL_AVDD PP1V05_GPU_FB_PLL_AVDD 77 115

FBA_DEBUG GPU_FBA_DEBUG0

FBA_DEBUG GPU_FBA_DEBUG1

FB_CAL_PD_VDDQ FB_CAL_PD_VDDQ 77 108

FB_CAL_PU_GND FB_CAL_PU_GND 77 108

FB_CAL_TERM_GND 108 FB_CAL_TERM_GND

PLACE_NEAR=U8000.H25:6.6MM

R8201 60.4 1% 1/20W MF 201

FB_CLAMP

R8261 10K MF 1% 1/20W 201

FBA_CMD_RFU NC

FBA_CMD_RFU NC

FB_VDDQ_SENSE SNS_GPUVDDQ_P OUT 78

FB_GND_SENSE SNS_GPUVDDQ_N OUT 78

NOSTUFF R8271 100 5% 1/20W MF 201

PLACE CLOSE TO BGA

108 77 FB_CAL_PU_GND

PLACE_NEAR=U8000.H27:6.6MM

R8204 40.2 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 77 78

PLACE_NEAR=U8000.J27:6.6MM

R8205 40.2 1% 1/20W MF 201

FB_CAL_PD_VDDQ 77 108

OMIT_TABLE

U8000
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B

108 80	B1	FB_B0_DQ<0>	G9	FBB_D0	
108 80	B1	FB_B0_DQ<1>	E9	FBB_D1	
108 80	B1	FB_B0_DQ<2>	G8	FBB_D2	
108 80	B1	FB_B0_DQ<3>	F9	FBB_D3	
108 80	B1	FB_B0_DQ<4>	F11	FBB_D4	
108 80	B1	FB_B0_DQ<5>	G11	FBB_D5	
108 80	B1	FB_B0_DQ<6>	F12	FBB_D6	
108 80	B1	FB_B0_DQ<7>	G12	FBB_D7	
108 80	B1	FB_B0_DQ<8>	G6	FBB_D8	
108 80	B1	FB_B0_DQ<9>	F5	FBB_D9	
108 80	B1	FB_B0_DQ<10>	E6	FBB_D10	
108 80	B1	FB_B0_DQ<11>	F6	FBB_D11	
108 80	B1	FB_B0_DQ<12>	F4	FBB_D12	
108 80	B1	FB_B0_DQ<13>	G4	FBB_D13	
108 80	B1	FB_B0_DQ<14>	E2	FBB_D14	
108 80	B1	FB_B0_DQ<15>	F3	FBB_D15	
108 80	B1	FB_B0_DQ<16>	C2	FBB_D16	
108 80	B1	FB_B0_DQ<17>	D4	FBB_D17	
108 80	B1	FB_B0_DQ<18>	D3	FBB_D18	
108 80	B1	FB_B0_DQ<19>	C1	FBB_D19	
108 80	B1	FB_B0_DQ<20>	B3	FBB_D20	
108 80	B1	FB_B0_DQ<21>	C4	FBB_D21	
108 80	B1	FB_B0_DQ<22>	B5	FBB_D22	
108 80	B1	FB_B0_DQ<23>	C5	FBB_D23	
108 80	B1	FB_B0_DQ<24>	A11	FBB_D24	
108 80	B1	FB_B0_DQ<25>	C11	FBB_D25	
108 80	B1	FB_B0_DQ<26>	D11	FBB_D26	
108 80	B1	FB_B0_DQ<27>	B11	FBB_D27	
108 80	B1	FB_B0_DQ<28>	D8	FBB_D28	
108 80	B1	FB_B0_DQ<29>	A8	FBB_D29	
108 80	B1	FB_B0_DQ<30>	C8	FBB_D30	
108 80	B1	FB_B0_DQ<31>	B8	FBB_D31	
108 80	B1	FB_B1_DQ<0>	F24	FBB_D32	
108 80	B1	FB_B1_DQ<1>	G23	FBB_D33	
108 80	B1	FB_B1_DQ<2>	E24	FBB_D34	
108 80	B1	FB_B1_DQ<3>	G24	FBB_D35	
108 80	B1	FB_B1_DQ<4>	D21	FBB_D36	
108 80	B1	FB_B1_DQ<5>	E21	FBB_D37	
108 80	B1	FB_B1_DQ<6>	G21	FBB_D38	
108 80	B1	FB_B1_DQ<7>	F21	FBB_D39	
108 80	B1	FB_B1_DQ<8>	G27	FBB_D40	
108 80	B1	FB_B1_DQ<9>	D27	FBB_D41	
108 80	B1	FB_B1_DQ<10>	G26	FBB_D42	
108 80	B1	FB_B1_DQ<11>	E27	FBB_D43	
108 80	B1	FB_B1_DQ<12>	E29	FBB_D44	
108 80	B1	FB_B1_DQ<13>	F29	FBB_D45	
108 80	B1	FB_B1_DQ<14>	E30	FBB_D46	
108 80	B1	FB_B1_DQ<15>	D30	FBB_D47	
108 80	B1	FB_B1_DQ<16>	A32	FBB_D48	
108 80	B1	FB_B1_DQ<17>	C31	FBB_D49	
108 80	B1	FB_B1_DQ<18>	C32	FBB_D50	
108 80	B1	FB_B1_DQ<19>	B32	FBB_D51	
108 80	B1	FB_B1_DQ<20>	D29	FBB_D52	
108 80	B1	FB_B1_DQ<21>	A29	FBB_D53	
108 80	B1	FB_B1_DQ<22>	C29	FBB_D54	
108 80	B1	FB_B1_DQ<23>	B29	FBB_D55	
108 80	B1	FB_B1_DQ<24>	B21	FBB_D56	
108 80	B1	FB_B1_DQ<25>	C23	FBB_D57	
108 80	B1	FB_B1_DQ<26>	A21	FBB_D58	
108 80	B1	FB_B1_DQ<27>	C21	FBB_D59	
108 80	B1	FB_B1_DQ<28>	B24	FBB_D60	
108 80	B1	FB_B1_DQ<29>	C24	FBB_D61	
108 80	B1	FB_B1_DQ<30>	B26	FBB_D62	
108 80	B1	FB_B1_DQ<31>	C26	FBB_D63	
108 80	OUT	FB_B0_WCLK_P<0>	F8	FBB_WCK01	
108 80	OUT	FB_B0_WCLK_N<0>	E8	FBB_WCK01*	
108 80	OUT	FB_B0_WCLK_P<1>	A5	FBB_WCK23	
108 80	OUT	FB_B0_WCLK_N<1>	A6	FBB_WCK23*	
108 80	OUT	FB_B1_WCLK_P<0>	D24	FBB_WCK45	
108 80	OUT	FB_B1_WCLK_N<0>	D25	FBB_WCK45*	
108 80	OUT	FB_B1_WCLK_P<1>	B27	FBB_WCK67	
108 80	OUT	FB_B1_WCLK_N<1>	C27	FBB_WCK67*	
NC			D6	FBB_WCKB01	
NC			D7	FBB_WCKB01*	
NC			C6	FBB_WCKB23	
NC			B6	FBB_WCKB23*	
NC			F26	FBB_WCKB45	
NC			E26	FBB_WCKB45*	
NC			A26	FBB_WCKB67	
NC			A27	FBB_WCKB67*	

			D13	FBB_CMD0	
			E14	FBB_CMD1	
			F14	FBB_CMD2	
			A12	FBB_CMD3	
			B12	FBB_CMD4	
			C14	FBB_CMD5	
			B14	FBB_CMD6	
			G15	FBB_CMD7	
			F15	FBB_CMD8	
			E15	FBB_CMD9	
			D15	FBB_CMD10	
			A14	FBB_CMD11	
			D14	FBB_CMD12	
			A15	FBB_CMD13	
			B15	FBB_CMD14	
			C17	FBB_CMD15	
			D18	FBB_CMD16	
			E18	FBB_CMD17	
			F18	FBB_CMD18	
			A20	FBB_CMD19	
			B20	FBB_CMD20	
			C18	FBB_CMD21	
			B18	FBB_CMD22	
			G18	FBB_CMD23	
			G17	FBB_CMD24	
			F17	FBB_CMD25	
			D16	FBB_CMD26	
			A18	FBB_CMD27	
			D17	FBB_CMD28	
			A17	FBB_CMD29	
			B17	FBB_CMD30	
			E17	FBB_CMD31	
			D12	FBB_CLK0	
			E12	FBB_CLK0*	
			E20	FBB_CLK1	
			F20	FBB_CLK1*	
			E11	FBB_DQM0	
			E3	FBB_DQM1	
			A3	FBB_DQM2	
			C9	FBB_DQM3	
			F23	FBB_DQM4	
			F27	FBB_DQM5	
			C30	FBB_DQM6	
			A24	FBB_DQM7	
			D9	FBB_DQS_RN0	NC
			E4	FBB_DQS_RN1	NC
			B2	FBB_DQS_RN2	NC
			A9	FBB_DQS_RN3	NC
			D22	FBB_DQS_RN4	NC
			D28	FBB_DQS_RN5	NC
			A30	FBB_DQS_RN6	NC
			B23	FBB_DQS_RN7	NC
			D10	FBB_DQS_WP0	
			D5	FBB_DQS_WP1	
			C3	FBB_DQS_WP2	
			B9	FBB_DQS_WP3	
			E23	FBB_DQS_WP4	
			E28	FBB_DQS_WP5	
			B30	FBB_DQS_WP6	
			A23	FBB_DQS_WP7	
			H17	FBB_PLL_AVDD	
			G14	FBB_DEBUG0	
			G20	FBB_DEBUG1	
			H26	FB_VREF	
			C12	FBB_CMD_RFU0	NC
			C20	FBB_CMD_RFU1	NC

108 80	B1	FB_B0_DBI_L<0>	E11	FBB_DQM0	
108 80	B1	FB_B0_DBI_L<1>	E3	FBB_DQM1	
108 80	B1	FB_B0_DBI_L<2>	A3	FBB_DQM2	
108 80	B1	FB_B0_DBI_L<3>	C9	FBB_DQM3	
108 80	B1	FB_B1_DBI_L<0>	F23	FBB_DQM4	
108 80	B1	FB_B1_DBI_L<1>	F27	FBB_DQM5	
108 80	B1	FB_B1_DBI_L<2>	C30	FBB_DQM6	
108 80	B1	FB_B1_DBI_L<3>	A24	FBB_DQM7	
108 80	IN	FB_B0_EDC<0>	D10	FBB_DQS_WP0	
108 80	IN	FB_B0_EDC<1>	D5	FBB_DQS_WP1	
108 80	IN	FB_B0_EDC<2>	C3	FBB_DQS_WP2	
108 80	IN	FB_B0_EDC<3>	B9	FBB_DQS_WP3	
108 80	IN	FB_B1_EDC<0>	E23	FBB_DQS_WP4	
108 80	IN	FB_B1_EDC<1>	E28	FBB_DQS_WP5	
108 80	IN	FB_B1_EDC<2>	B30	FBB_DQS_WP6	
108 80	IN	FB_B1_EDC<3>	A23	FBB_DQS_WP7	

FBB_PLL_AVDD PP1V05_GPU_FB_PLL_AVDD

FBB_DEBUG0 GPU_FBB_DEBUG0 77

FBB_DEBUG1 GPU_FBB_DEBUG1 77

FB_VREF FB_VREF 77 113

C8206 1.0UF 20% 4V X6S 0201

C8207 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_S0_FB 77 78

NOSTUFF R8206 60.4 1% 1/20W MF 201

NOSTUFF R8207 60.4 1% 1/20W MF 201

77 GPU_FBB_DEBUG0

77 GPU_FBB_DEBUG1

Page Notes

Power aliases required by this page:
- +PP1V35_GPU_S0_FB
- +PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

ROM options provided by this page:

(NONE)

L8201
30-OHM-25%-5A-0.01-OHM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

=PP1V05_GPU_PEX_IOVDD 1 2 CRITICAL 0603 ESR = 0.050HM

PP1V05_GPU_FB_PLL_AVDD 77 115

C8201 200UF 20% 4V X5R-CERM 0402

C8202 1.0UF 20% 4V X6S 0201

C8203 0.1UF 10% 6.3V X6S 0201

C8204 0.1UF 10% 6.3V X6S 0201

RDAR://11427653 D8: NV GUIDELINE USES 22UF. APPLE USES 20UF

L8202
30-OHM-25%-5A-0.01-OHM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

=PP1V05_GPU_PEX_IOVDD 1 2 CRITICAL 0603 ESR = 0.050HM

PP1V05_GPU_FB_DLL_AVDD 77 115

C8208 200UF 20% 4V X5R-CERM 0402

C8209 1.0UF 20% 4V X6S 0201

C8205 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

108 80 77 FB_B0_RESET_L

R8254 10K 1% 1/20W MF 201

108 80 77 FB_B1_RESET_L

R8255 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 77 78

R8256 10K 1% 1/20W MF 201

R8257 10K 1% 1/20W MF 201

108 80 77 FB_B0_CKE_L

108 80 77 FB_B1_CKE_L

MEM VREFC & VREFD SWITCH

80 79 OUT FB_SW_LEG

CRITICAL
Q8265
SSM3K15AMFVAPE
VESM

GPU_ALT_VREF IN B2 113

R8260 10K 5% 1/20W MF 201

SYNC_MASTER=D8_YAN	SYNC_DATE=05/15/2012
PAGE TITLE	KEPLER FRAME BUFFER I/F
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
	PAGE 82 OF 143
	SHEET 77 OF 117

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GPU POWER ALIAS

80 79 76 =PP1V35_GPU_FBVDDQ = =PP1V35_S0_GPU_FBVDDQ 6
77 =PP1V35_GPU_S0_FB =
83 76 =PPVCORE_GPU = =PPVCORE_S0_GPU 6 51
83 77 =PP1V05_GPU_PEX_IOVDD = =PP1V05_S0_GPU_PEX_IOVDD 6
83 82 81 75 =PP3V3_GPU_VDD33 = =PP3V3_S0_GPU_VDD33 6
81 =PP3V3_GPU_MISC = =PP3V3_S0_GPU_MISC 6
83 81 =PP1V05_GPU_PEX_PLLVDD = =PP1V05_S0_GPU_PEX_PLLVDD 6
81 =PP1V05_GPU_IFPCD_IOVDD = =PP1V05_S0_GPU_IFPCD_IOVDD 6
81 =PP1V05_GPU_IFPEF_IOVDD = =PP1V05_S0_GPU_IFPEF_IOVDD 6
81 =PP3V3_GPU_IFPX_PLLVDD = =PP3V3_S0_GPU_IFPX_PLLVDD 6

GPU SIGNAL & SENSE ALIAS

83 GPU_VDD_SENSE = VSNS_GPU_VDD 92 110
MAKE_BASE=TRUE
83 GPU_GND_SENSE = VSNS_GPU_VSS 92 110
MAKE_BASE=TRUE
77 SNS_GPUVDDQ_P = VSNS_FBVDDQ_P 95 110
MAKE_BASE=TRUE
77 SNS_GPUVDDQ_N = VSNS_FBVDDQ_N 95 110
MAKE_BASE=TRUE
81 GPU_TDIODE_P = NC_GPU_TDIODEP
MAKE_BASE=TRUE NO_TEST=TRUE
81 GPU_TDIODE_N = NC_GPU_TDIODEN
MAKE_BASE=TRUE NO_TEST=TRUE

GPU VIDS ALIAS (VR VID0 IS TIED LOW)

RA850 0 5% 1/20W MF 201
110 82 GPU_VCORE_VID0 — REG_GPUCORE_VID1 92 110

RA851 0 5% 1/20W MF 201
110 82 GPU_VCORE_VID1 — REG_GPUCORE_VID2 92 110

RA852 0 5% 1/20W MF 201
110 82 GPU_VCORE_VID2 — REG_GPUCORE_VID3 92 110

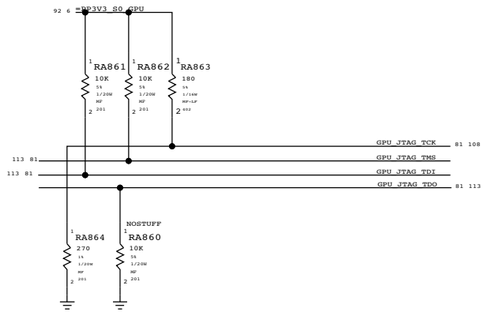
RA853 0 5% 1/20W MF 201
110 82 GPU_VCORE_VID3 — REG_GPUCORE_VID4 92 110

RA854 0 5% 1/20W MF 201
110 82 GPU_VCORE_VID4 — REG_GPUCORE_VID5 92 110

RA855 0 5% 1/20W MF 201
110 82 GPU_VCORE_VID5 — REG_GPUCORE_VID6 92 110

THESE POWER ALIASES ARE CRAETED TO MATCH D8 GK104

PU/PD IS BASED ON RECOMMENDATION FROM NV FOR NVDIA GPU JTAG DEBUGGER



SYNC MASTER=D8 YAN SYNC DATE=04/09/2012

PAGE TITLE
GPU SIGNAL & POWER ALIASES

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 83 OF 143
SHEET 78 OF 117

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

This memory device is in Mirrored Mode.

CK TERMINATION - A0

CK TERMINATION - A1

U8400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

U8400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

U8450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

U8450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

PLACE CLOSE TO U8400

PLACE CLOSE TO U8450

SYNC_MASTER=D8_YAN	SYNC_DATE=04/09/2012
PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
	PAGE 84 OF 143
	SHEET 79 OF 117

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

This memory device is in Mirrored Mode.

OMIT_TABLE

PLACE CLOSE TO U8500

PLACE CLOSE TO U8550

U8500
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

U8500
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

U8550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

U8550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

CK TERMINATION - B0

CK TERMINATION - B1

SYNC MASTER=D8 YAN	SYNC DATE=04/09/2012
PAGE TITLE: GDDR5 Frame Buffer B	
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
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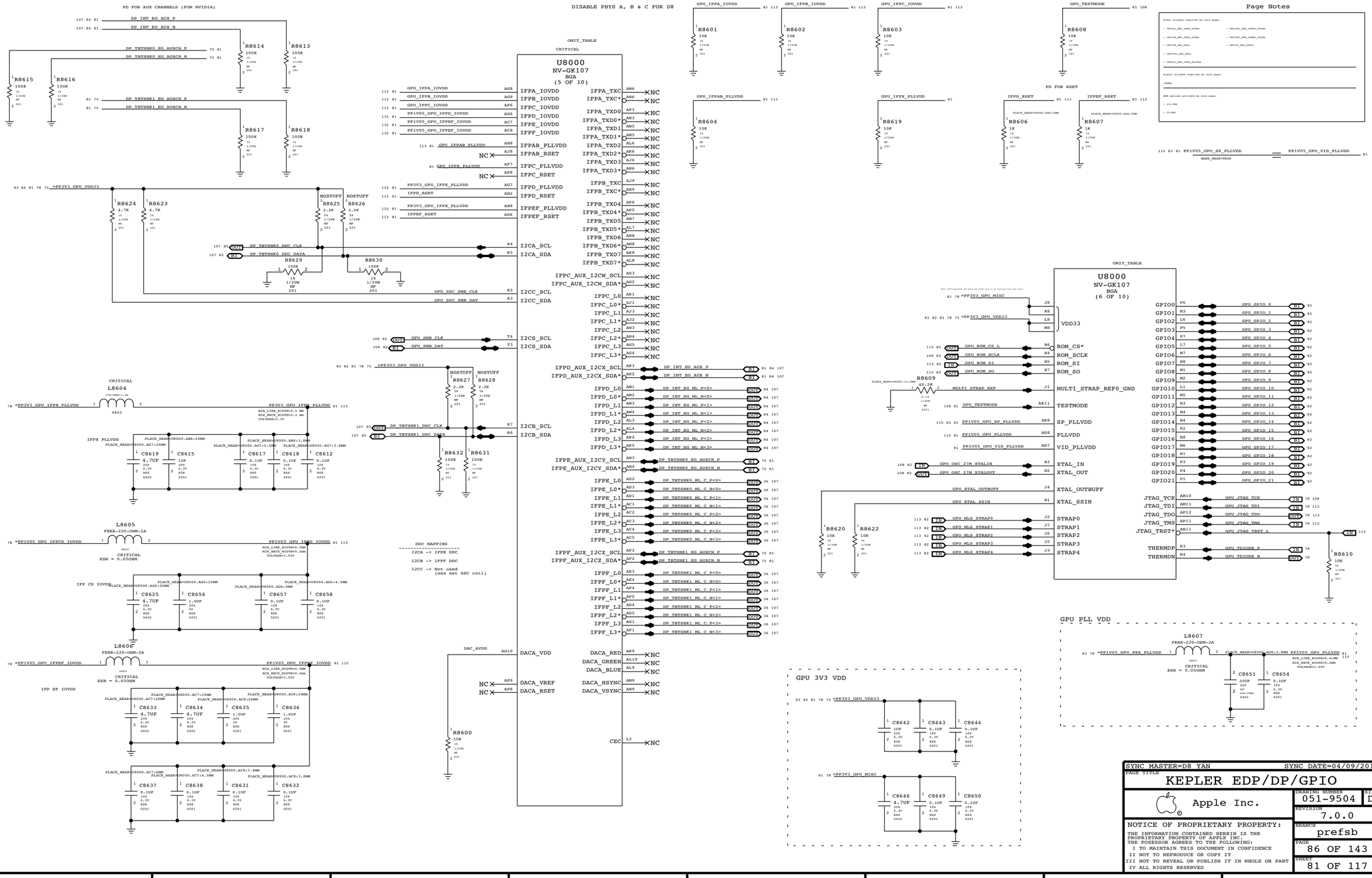
	SHEET 80 OF 117


PD FOR AUX CHANNELS (FOR NVIDIA)
DISABLE PHYS A, B & C FOR D8
OMIT_TABLE
U8000
NV-GK107
BGA
(5 OF 10)
Page Notes
PD FOR RSET
OMIT_TABLE
U8000
NV-GK107
BGA
(6 OF 10)
DDC MAPPING
I2CA -> IFPE DDC
I2CB -> IFPF DDC
I2CC -> Not used
(was ext SSC cntl)
GPU PLL VDD
GPU 3V3 VDD
SYNC MASTER=D8 YAN
SYNC DATE=04/09/2012
PAGE TITLE
KEPLER EDP/DP/GPIO
Apple Inc.
DRAWING NUMBER
051-9504
SIZE
D
REVISION
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prefsb
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81 OF 117
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ISOLATION R's for GPU Int Temp Sense

R8780 0 5% 1/20W MF 201
108 81 GPU_SMB_DAT — GPU_SMB_DAT_R — 50 108

R8781 0 5% 1/20W MF 201
108 81 GPU_SMB_CLK — GPU_SMB_CLK_R — 50 108

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0175	1	RES,MF,20.0k ,1,1/20W,0201	R8711		FB:BOTH_SAMSUNG
118S0105	1	RES,MF,15.0k ,1,1/20W,0201	R8711		FB:BOTH_HYNIX

GPIOs

	Native Func	GPIOs		
81 GPU_GPIO_0	GP	GPU_VCORE_VID4	MAKE_BASE=TRUE	78 110
81 GPU_GPIO_1	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE	78 110
81 GPU_GPIO_2	GP	GPU_LCD_BKLT_PWM	MAKE_BASE=TRUE	84 107
81 GPU_GPIO_3	GP	GPU_PSI_L	MAKE_BASE=TRUE	92 110
81 GPU_GPIO_4	GP	EG_BKLT_EN	MAKE_BASE=TRUE	82
81 GPU_GPIO_5	GP	GPU_VCORE_VID1	MAKE_BASE=TRUE	78 110
81 GPU_GPIO_6	GP	GPU_VCORE_VID2	MAKE_BASE=TRUE	78 110
81 GPU_GPIO_7	GP	FB_CLAMP_TOGGLE_REQ_L	MAKE_BASE=TRUE	
81 GPU_GPIO_8	GP	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE	82 116
81 GPU_GPIO_9	GP	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE	82 116
81 GPU_GPIO_10	GP	GPU_ALT_VREF	MAKE_BASE=TRUE	77 113
81 GPU_GPIO_11	GP	GPU_VCORE_VID0	MAKE_BASE=TRUE	78 110
81 GPU_GPIO_12	GP	NC_HDMI_EG_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	
81 GPU_GPIO_13	GP	GPU_VCORE_VID5	MAKE_BASE=TRUE	78 110

R8791 10K 5% 1/20W MF 201 — 1 — 2 NOSTUFF

	Native Func	GPIOs		
81 GPU_GPIO_14	GP	NC_DP_EXTA_CA_DET_EG	MAKE_BASE=TRUE NO_TEST=TRUE	
81 GPU_GPIO_15	GP	NC_DP_EXTB_CA_DET_EG	MAKE_BASE=TRUE NO_TEST=TRUE	
81 GPU_GPIO_16	GP	FBVDD_ALTVO	MAKE_BASE=TRUE	82 95 113
81 GPU_GPIO_17	GP	DP_INT_EG_HPD	MAKE_BASE=TRUE	84 112
81 GPU_GPIO_18	GP	DP_TBTSNXO_HPD	MAKE_BASE=TRUE	36 107
81 GPU_GPIO_19	GP	DP_TBTSNK1_HPD	MAKE_BASE=TRUE	36 107
81 GPU_GPIO_20	GP	NC_GPU_GPIO_20_RSVD	MAKE_BASE=TRUE NO_TEST=TRUE	
81 GPU_GPIO_21	GP	NC_GPU_GPIO_21_RSVD	MAKE_BASE=TRUE NO_TEST=TRUE	

CONFIG STRAPS - MLPS USE 1% FOR ACCURACY

=PP3V3_GPU_VDD33 (81 78 75 83 82)
R8700 45.3K 1% 1/20W MF 201 — OUT 81 113 — GPU_MLS_STRAP0
R8701 5.62K 1% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33 (83 82 81 78 75)
NOSTUFF R8708 3.24K 1% 1/20W MF 201 — OUT 81 113 — GPU_MLS_STRAP4
R8709 45.3K 1% 1/20W MF 201

=PP3V3_GPU_VDD33 (81 78 75 83 82)
NOSTUFF R8702 3.24K 1% 1/20W MF 201 — OUT 81 113 — GPU_MLS_STRAP1
R8703 34.8K 1% 1/20W MF 201

=PP3V3_GPU_VDD33 (83 82 81 78 75)
NOSTUFF R8710 3.24K 1% 1/20W MF 201 — OUT 81 82 113 — GPU_ROM_SI
R8711 15K 1% 1/20W MF 201 OMIT_TABLE

=PP3V3_GPU_VDD33 (81 78 75 83 82)
NOSTUFF R8704 10K 1% 1/20W MF 201 — OUT 81 113 — GPU_MLS_STRAP2
R8705 4.99K 1% 1/20W MF 201

=PP3V3_GPU_VDD33 (83 82 81 78 75)
R8712 10K 1% 1/20W MF 201 — OUT 81 82 113 — GPU_ROM_SO
R8713 10K 1% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33 (78 75 82 81 83)
R8706 10K 1% 1/20W MF 201 — OUT 81 113 — GPU_MLS_STRAP3
R8707 5.62K 1% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33 (83 82 81 78 75)
NOSTUFF R8714 35.7K 1% 1/20W MF 201 — OUT 81 82 108 — GPU_ROM_SCLK
R8715 15K 1% 1/20W MF 201

GPU VBIOS ROM

83 82 81 78 75 =PP3V3_GPU_VDD33
GPU_ROM:YES
R8723 33 1% 1/20W MF 201 — 113 GPU_ROM_SI — GPU_ROM_SI_R
R8720 10K 5% 1/20W MF 201
R8726 33 1% 1/20W MF 201 — 81 82 113 GPU_ROM_SO — GPU_ROM_SO_R
R8725 33 1% 1/20W MF 201 — 81 113 GPU_ROM_CS_L — GPU_ROM_CS_L_R
R8724 33 1% 1/20W MF 201 — 81 82 108 GPU_ROM_SCLK — GPU_ROM_SCLK_R

U8701 1MBIT MX25V1005C USON NOSTUFF CRITICAL
8 VCC
5 SI — GPU_ROM_SI_R
2 SO — GPU_ROM_SO_R
1 CS* — GPU_ROM_CS_L_R
6 SCLK — GPU_ROM_SCLK_R
3 WP* — GPU_ROM_WP_L
7 HOLD*
GND PAD 4 9

GPU_ROM:YES
R8721 0 5% 1/20W MF 201 — GPU_ROM_WP_L
C8721 0.1UF 10% 6.3V X5R 201 — GPU_ROM:YES
NO STUFF R8722 0 5% 1/20W MF 201

GPU XTAL 27 MHZ

GPU_OSC_27M_XTALIN — OUT 81 108
GPU_OSC_27M_XTALOUT — IN 81 108
197S0464
Y8700 2.50X2.00MM-SM 27MHZ-30PPM-18PF-60OHM CRITICAL
C8700 18PF 5% 25V NP0-C0G-CERM 0201
C8701 18PF 5% 25V NP0-C0G-CERM 0201
NC NC NC NC

GPU overtemp masking

83 82 81 78 75 =PP3V3_GPU_VDD33
R8752 10K 5% 1/20W MF 201
51 48 6 =PP3V3_S0_SMC
C8702 0.1UF 10% 16V X7R-CERM 0402
116 SMC_GFX_OVERTEMP_Q
U8702 74LVC1G08GW SOT353 — SMC_GFX_OVERTEMP — OUT 82 47 48 116
Q8701 SSM3K15AMFVAPE VESM
116 82 SMC_GFX_OVERTEMP_R_L
GPU_RESET_L — IN 26 113

GPU Thermal Throttle

83 82 81 78 75 =PP3V3_GPU_VDD33
R8796 10K 5% 1/20W MF 201
R8797 10K 5% 1/20W MF 201
116 82 SMC_GFX_OVERTEMP_R_L — R8798 NOSTUFF 0 5% 1/20W MF 201 — SMC_GFX_OVERTEMP — OUT 47 48 82 116
116 82 SMC_GFX_THROTTLE_R_L — R8799 0 5% 1/20W MF 201 — SMC_GFX_THROTTLE_L — IN 47 116
EG_BKLT_EN — OUT 82
FBVDD_ALTVO — OUT 82 95 113
NOSTUFF R8793 10K 5% 1/20W MF 201
R8794 10K 5% 1/20W MF 201
NOSTUFF R8790 10K 5% 1/20W MF 201

SYNC_MASTER=D8 YAN SYNC_DATE=07/27/2012
PAGE TITLE
KEPLER GPIOS,CLK & STRAPS

Apple Inc.

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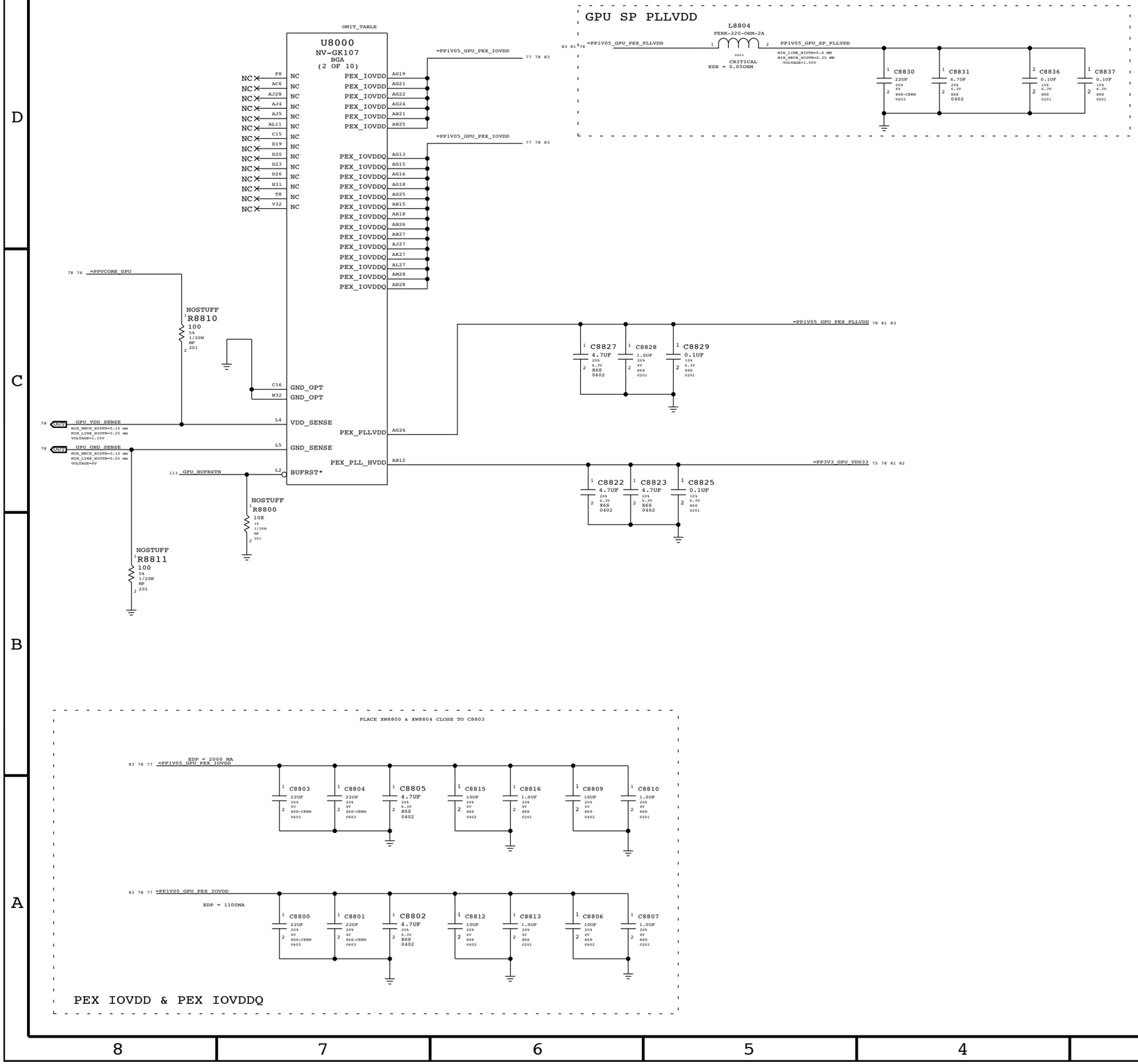
OMIT_TABLE
U8000
NV-GK107
BGA
(2 OF 10)
NC P8
NC AC6
NC AJ28
NC AJ4
NC AJ5
NC AL11
NC C15
NC D19
NC D20
NC D23
NC D26
NC H31
NC T8
NC V32
PEX_IOVDD AG19
PEX_IOVDD AG21
PEX_IOVDD AG22
PEX_IOVDD AG24
PEX_IOVDD AH21
PEX_IOVDD AH25
PEX_IOVDDQ AG13
PEX_IOVDDQ AG15
PEX_IOVDDQ AG16
PEX_IOVDDQ AG18
PEX_IOVDDQ AG25
PEX_IOVDDQ AH15
PEX_IOVDDQ AH18
PEX_IOVDDQ AH26
PEX_IOVDDQ AH27
PEX_IOVDDQ AJ27
PEX_IOVDDQ AK27
PEX_IOVDDQ AL27
PEX_IOVDDQ AM28
PEX_IOVDDQ AN28
GND_OPT C16
GND_OPT W32
VDD_SENSE L4
GND_SENSE L5
BUFRST* L2
PEX_PLLVDD AG26
PEX_PLL_HVDD AH12
=PP1V05_GPU_PEX_IOVDD 77 78 83
=PP1V05_GPU_PEX_IOVDD 77 78 83
=PP1V05_GPU_PEX_PLLVDD 78 81 83
=PP3V3_GPU_VDD33 75 78 81 82
GPU SP PLLVDD
L8804
FERR-220-OHM-2A
0603
CRITICAL
ESR = 0.050HM
=PP1V05_GPU_PEX_PLLVDD
PP1V05_GPU_SP_PLLVDD
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.05V
C8830 22UF 20% 4V X6S-CERM 0603
C8831 4.7UF 20% 6.3V X6S 0402
C8836 0.1UF 10% 6.3V X6S 0201
C8837 0.1UF 10% 6.3V X6S 0201
78 76 =PPVCORE_GPU
NOSTUFF
R8810
100
5%
1/20W
MF
201
C8827 4.7UF 20% 6.3V X6S 0402
C8828 1.0UF 20% 4V X6S 0201
C8829 0.1UF 10% 6.3V X6S 0201
78 OUT GPU_VDD_SENSE
MIN_NECK_WIDTH=0.10 mm
MIN_LINE_WIDTH=0.25 mm
VOLTAGE=1.05V
78 OUT GPU_GND_SENSE
MIN_NECK_WIDTH=0.10 mm
MIN_LINE_WIDTH=0.25 mm
VOLTAGE=0V
113 GPU_BUFRSTN
NOSTUFF
R8800
10K
1%
1/20W
MF
201
C8822 4.7UF 20% 6.3V X6S 0402
C8823 4.7UF 20% 6.3V X6S 0402
C8825 0.1UF 10% 6.3V X6S 0201
NOSTUFF
R8811
100
5%
1/20W
MF
201
PLACE XW8800 & XW8804 CLOSE TO C8803
EDP = 2000 MA
83 78 77 =PP1V05_GPU_PEX_IOVDD
C8803 22UF 20% 4V X6S-CERM 0603
C8804 22UF 20% 4V X6S-CERM 0603
C8805 4.7UF 20% 6.3V X6S 0402
C8815 10UF 20% 4V X6S 0402
C8816 1.0UF 20% 4V X6S 0201
C8809 10UF 20% 4V X6S 0402
C8810 1.0UF 20% 4V X6S 0201
83 78 77 =PP1V05_GPU_PEX_IOVDD
EDP = 1100MA
C8800 22UF 20% 4V X6S-CERM 0603
C8801 22UF 20% 4V X6S-CERM 0603
C8802 4.7UF 20% 6.3V X6S 0402
C8812 10UF 20% 4V X6S 0402
C8813 1.0UF 20% 4V X6S 0201
C8806 10UF 20% 4V X6S 0402
C8807 1.0UF 20% 4V X6S 0201
PEX IOVDD & PEX IOVDDQ
OMIT_TABLE
U8000
NV-GK107
BGA
(8 OF 10)
GND
AG11
A2
AJ3
AA13
AA15
AA17
AA18
AA20
AA22
AB12
AB14
AB16
AB19
AB2
AB21
AB23
AB28
AB30
AB32
AB5
AB7
AC13
AC15
AC17
AC18
AC20
AC22
AE2
AE28
AE30
AE32
AE33
AE5
AE7
AH10
AH13
AH16
AH19
AH2
AH22
AH24
AH28
AH29
AH30
AH32
AH33
AH5
AH7
AJ7
AK10
AK7
AL12
AL14
AL15
AL17
AL18
AL2
AL20
AL21
AL23
AL24
AL26
AL28
AL30
AL32
AL33
AL5
AM13
AM16
AM19
AM22
AM25
AN1
AN10
AN13
AN16
AN19
AN22
AN25
AN30
AN34
AN4
AN7
AP2
AP33
B1
B10
B22
B25
B28
B31
B34
B4
B7
C10
C13
C19
C22
C25
C28
OMIT_TABLE
U8000
NV-GK107
BGA
(9 OF 10)
GND
C7
D2
D31
D33
E10
E22
E25
E5
E7
F28
F7
G10
G13
G16
G19
G2
G22
G25
G28
G3
G30
G32
G33
G5
G7
K2
K28
K30
K32
K33
K5
K7
M13
M15
M17
M18
M20
M22
N12
N14
N16
N19
N2
N21
N23
N28
N30
N32
N33
N5
N7
P13
P15
P17
P18
P20
P22
R12
R14
R16
R19
R21
R23
T13
T15
T17
T18
T2
T20
T22
T28
T32
T5
T7
U12
U14
U16
U19
U21
U23
V12
V14
V16
V19
V21
V23
W13
W15
W17
W18
W20
W22
W28
Y12
Y14
Y16
Y19
Y21
Y23
AH11
Page Notes
Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
SYNC MASTER=D8 YAN
SYNC DATE=04/09/2012
PAGE TITLE
KEPLER PEX PWR/GNDS
Apple Inc.
DRAWING NUMBER 051-9504
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REVISION 7.0.0
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TP to DP aliases

TP_DP_TBTSRC_ML_CP<0>	=	DP_TBTSRC_ML_P<0>
TP_DP_TBTSRC_ML_CN<0>	=	DP_TBTSRC_ML_N<0>
TP_DP_TBTSRC_ML_CP<1>	=	DP_TBTSRC_ML_P<1>
TP_DP_TBTSRC_ML_CN<1>	=	DP_TBTSRC_ML_N<1>
TP_DP_TBTSRC_ML_CP<2>	=	DP_TBTSRC_ML_P<2>
TP_DP_TBTSRC_ML_CN<2>	=	DP_TBTSRC_ML_N<2>
TP_DP_TBTSRC_ML_CP<3>	=	DP_TBTSRC_ML_P<3>
TP_DP_TBTSRC_ML_CN<3>	=	DP_TBTSRC_ML_N<3>
TP_DP_TBTSRC_AUXCH_CP	=	DP_TBTSRC_AUXCH_P
TP_DP_TBTSRC_AUXCH_CN	=	DP_TBTSRC_AUXCH_N

MAKE_BASE=TRUE

=PP1V5_S0_DP

R9210 470K 5% 1/20W MF 201

R9211 470K 5% 1/20W MF 201

C9208 0.1UF

C9209 0.1UF

DP_INT_EG_AUX_P

DP_INT_EG_AUX_N

DP_INT_EG_AUX_C_P

DP_INT_EG_AUX_C_N

=PP1V5_S0_DP

R9212 470K 5% 1/20W MF 201

R9213 470K 5% 1/20W MF 201

C9210 0.1UF

C9211 0.1UF

DP_TBTSRC_AUXCH_P

DP_TBTSRC_AUXCH_N

DP_TBTSRC_AUX_C_P

DP_TBTSRC_AUX_C_N

DP_INT_EG_HPD

R9200 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX

R9204 10K 5% 1/20W MF 201

DP_GPU_MUX_EN

DP_TBT_SEL

R9201 10K 5% 1/20W MF 201

DP_TBT_HPD

PD is on the LR page

C9268 0.1UF 10% 6.3V X5R 201

C9269 0.1UF 10% 6.3V X5R 201

U9200
CBTL06142EEE
TFBGA
CRITICAL

DP_INT_EG_ML_P<0>	B4	DIN1_0+	
DP_INT_EG_ML_N<0>	A4	DIN1_0-	
DP_INT_EG_ML_P<1>	B5	DIN1_1+	
DP_INT_EG_ML_N<1>	A5	DIN1_1-	
DP_INT_EG_ML_P<2>	B6	DIN1_2+	
DP_INT_EG_ML_N<2>	A6	DIN1_2-	
DP_INT_EG_ML_P<3>	A8	DIN1_3+	
DP_INT_EG_ML_N<3>	A9	DIN1_3-	
	H9	DAUX1+	
	J9	DAUX1-	
	H8	DDC_CLK1	NC
	J8	DDC_DAT1	NC
	J2	HPD_1	
DP_TBTSRC_ML_C_P<0>	B8	DIN2_0+	
DP_TBTSRC_ML_C_N<0>	B9	DIN2_0-	
DP_TBTSRC_ML_C_P<1>	D8	DIN2_1+	
DP_TBTSRC_ML_C_N<1>	D9	DIN2_1-	
DP_TBTSRC_ML_C_P<2>	E8	DIN2_2+	
DP_TBTSRC_ML_C_N<2>	E9	DIN2_2-	
DP_TBTSRC_ML_C_P<3>	F8	DIN2_3+	
DP_TBTSRC_ML_C_N<3>	F9	DIN2_3-	
	H6	DAUX2+	
	J6	DAUX2-	
	H5	DDC_CLK2	NC
	J5	DDC_DAT2	NC
	H3	HPD_2	
	A1	GPU_SEL	
	B7	XSD*	

	B2	DOUT_0+	DP_INTPNL_ML_C_P<0>
	B1	DOUT_0-	DP_INTPNL_ML_C_N<0>
	D2	DOUT_1+	DP_INTPNL_ML_C_P<1>
	D1	DOUT_1-	DP_INTPNL_ML_C_N<1>
	E2	DOUT_2+	DP_INTPNL_ML_C_P<2>
	E1	DOUT_2-	DP_INTPNL_ML_C_N<2>
	F2	DOUT_3+	DP_INTPNL_ML_C_P<3>
	F1	DOUT_3-	DP_INTPNL_ML_C_N<3>
DP_INTPNL_AUX_P	H2	AUX+	
DP_INTPNL_AUX_N	H1	AUX-	
DP_INTPNL_HPD	J1	HPDIN	
	C2	DDC_AUX_SEL	
	B3	GND	
	C8	GND	
	G8	GND	
	H4	GND	
	H7	GND	
	G2	GND	

C9200 0.15UF 0201 10% X5R 6.3V

C9201 0.15UF 0201 10% X5R 6.3V

C9202 0.15UF 0201 10% X5R 6.3V

C9203 0.15UF 0201 10% X5R 6.3V

C9204 0.15UF 0201 10% X5R 6.3V

C9205 0.15UF 0201 10% X5R 6.3V

C9206 0.15UF 0201 10% X5R 6.3V

C9207 0.15UF 0201 10% X5R 6.3V

R9202 100K 5% 1/20W MF 201

R9203 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX

R9290 0 5% 1/16W MF-LF 402

=PP1V5_S0_DP

PP1V5_S0_DP_BIAS

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.5V

C9290 1UF 10% 16V X5R 402

C9291 0.1UF 10% 16V X7R-CERM 0402

R9260 470K 5% 1/20W MF 201

R9261 470K 5% 1/20W MF 201

R9262 470K 5% 1/20W MF 201

R9263 470K 5% 1/20W MF 201

R9264 470K 5% 1/20W MF 201

R9265 470K 5% 1/20W MF 201

R9266 470K 5% 1/20W MF 201

R9267 470K 5% 1/20W MF 201

DP_TBTSRC_ML_P<0>	C9250 0.22UF	DP_TBTSRC_ML_C_P<0>
DP_TBTSRC_ML_N<0>	C9251 0.22UF	DP_TBTSRC_ML_C_N<0>
DP_TBTSRC_ML_P<1>	C9252 0.22UF	DP_TBTSRC_ML_C_P<1>
DP_TBTSRC_ML_N<1>	C9253 0.22UF	DP_TBTSRC_ML_C_N<1>
DP_TBTSRC_ML_P<2>	C9254 0.22UF	DP_TBTSRC_ML_C_P<2>
DP_TBTSRC_ML_N<2>	C9255 0.22UF	DP_TBTSRC_ML_C_N<2>
DP_TBTSRC_ML_P<3>	C9256 0.22UF	DP_TBTSRC_ML_C_P<3>
DP_TBTSRC_ML_N<3>	C9257 0.22UF	DP_TBTSRC_ML_C_N<3>

All: 20% 6.3V X5R 0201

=PP3V3_S0_INTDPMUX

C9270 0.1uF 10% 16V X5R 402

BDV_BKL_PWM

GPU_LCD_BKLT_PWM

DP_TBT_SEL

U9220
74LVC1G157
SOT487

R9222 47 5% 1/16W MF-LF 402

L9201 FERR-220-OHM 0402

LCD_BL_PWM

LCD_BL_FILT

LCD_BKLT_PWM

SYNC_MASTER=D8_AARON	SYNC_DATE=03/13/2012
PAGE TITLE: Internal DP MUXing	
Apple Inc.	DRAWING NUMBER: 051-9504 SIZE: D
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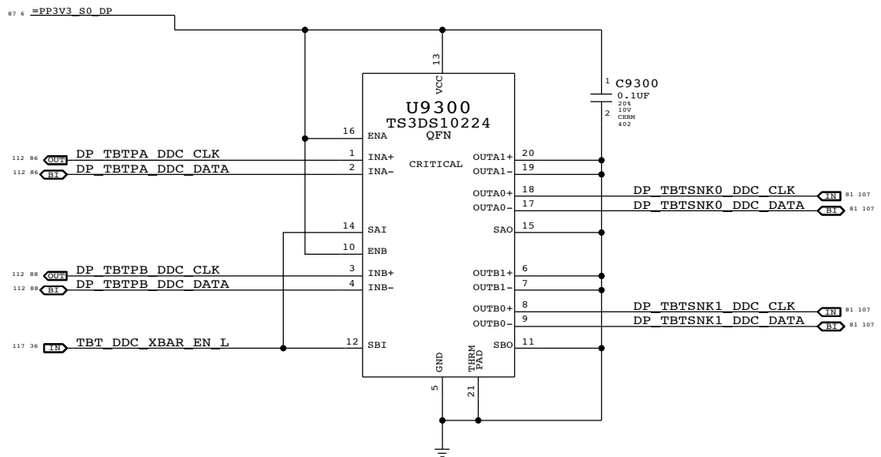
Dual-Port Host DDC Crossbar



SYNC_MASTER=D7_MLB SYNC_DATE=03/15/2012

PAGE TITLE

TBT DDC Crossbar

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTAPWRSW 18.9V Max
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 50V X7R 603-1
U9410 CD3210A0RGP QFN
V3P3 / VHV / RSVD / EN / HV_EN / S0 / GND / THRM PAD
V3P3OUT — NC
OUT — PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V
C9411 0.1UF 10% 50V X7R 603-1
ISET_V3P3 — TBTAPWRSW_ISET_V3P3
ISET_S0 — TBTAPWRSW_ISET_S0
ISET_S3 — TBTAPWRSW_ISET_S3
=TBTPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
12V: See below
TBTHV:P15V
R9410 22.6K 1% 1/16W MF-LF 402
R9411 22.6K 1% 1/16W MF-LF 402
R9412 36.5K 1% 1/16W MF-LF 402
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413 22.6K 1% 1/16W MF-LF 402
R9414 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

=PP3V3_S4_TBT
C9420 0.1UF 10% 6.3V X5R 201
C9421 0.1UF 10% 6.3V X5R 201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201
CRITICAL U9420 CBTL05023 HVQFN
VDD / BIASIN / AUXIO_EN / AUX- / AUX+ / DDC_DAT / DDC_CLK / CA_DETOUT / DP+ / DP- / LSTX / LSRX / DP_PD / HPDOUT / BIASOUT / AUXIO- / AUXIO+ / CA_DET / DPMLO+ / DPMLO- / HPD / GND_THMPAD
TBT_A_BIAS VOLTAGE=3.3V
C9425 0.1UF 10% 6.3V X5R 201
TBT_A_CIO_SEL
DP_AUXIO_EN
DP_TBTPA_AUXCH_C_N / DP_TBTPA_AUXCH_C_P
C9430 0.1UF 10% 6.3V X5R 201
C9431 0.1UF 10% 6.3V X5R 201
DP_TBTPA_AUXCH_N / DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA / DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1> / DP_TBTPA_ML_C_N<1>
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1> / DP_TBTPA_ML_N<1>
TBT_A_LSTX / TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
=PP3V3_S4_TBT
CRITICAL U9460 74AUP1T97 SOT891
TBT_A_LSRX
C9460 0.1UF 10% 16V X5R-CERM 0201
R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201
TBT_A_HPD
DP_A_AUXCH_DDC_N / DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1> / DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

L9400 FERR-120-OHM-3A 0603
PP3V3R3HV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V
C9400 0.01UF 10% 50V X7R-CERM 0402
C9401 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V
R9401 12 5% 1/20W MF 201
TBT Dir / DP Dir

CRITICAL
J9400 DUAL-MDP-D8 F-ANG-TH
SHLD
HPD / CONFIG1 / CONFIG2 / GND2 / ML_LANE3P / ML_LANE3N / GND4 / AUX_CHP / AUX_CHN / DP_PWR
ML_LANE0P / ML_LANE0N / GND1 / ML_LANE1P / ML_LANE1N / GND3 / ML_LANE2P / ML_LANE2N / RETURN
PORT A
SHLD
514-0831

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
C9405 0.01UF 10% 25V X5R-CERM 0201
DP Dir / TBT Dir
TBT_A_R2D_P<0> / TBT_A_R2D_N<0>
TBT: TX_0
GND_VOID=TRUE (Both C's)
C9470 0.22UF 20% 6.3V X5R 0201
C9471 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<0> / TBT_A_R2D_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
C9406 0.01UF 10% 25V X5R-CERM 0201
DP_A_LSX_ML_P<1> / DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_A_R2D_P<1> / TBT_A_R2D_N<1>
TBT: TX_1
NOTE: Polarity Swapped for layout!
GND_VOID=TRUE (Both C's)
C9472 0.22UF 20% 6.3V X5R 0201
C9473 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_N<1> / TBT_A_R2D_C_P<1>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

GND_VOID=TRUE (Both C's)
C9474 0.47UF 20% 4V CERM-X5R-1 201
C9475 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_N<0> / TBT_A_D2R_P<0>
TBT_A_D2R_C_P<0> / TBT_A_D2R_C_N<0>
NOTE: Polarity Swapped for layout!
R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
C9478 0.22UF 20% 6.3V X5R 0201
C9479 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<3> / DP_TBTPA_ML_C_N<3>
TBT: Terminated
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201
TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
GND_VOID=TRUE (Both C's)
C9476 0.47UF 20% 4V CERM-X5R-1 201
C9477 0.47UF 20% 4V CERM-X5R-1 201
TBT_A_D2R_N<1> / TBT_A_D2R_P<1>
TBT_A_D2R_C_P<1> / TBT_A_D2R_C_N<1>
NOTE: Polarity Swapped for layout!
CRITICAL GND_VOID=TRUE (Both D's)
D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P / TBT_A_D2R1_AUXDDC_N
CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
DP_A_AUXCH_DDC_P / DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V C0G-NP0 0402
C9499 30PF 5% 50V C0G-NP0 0402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R-CERM 0201
C9495 330PF 10% 16V X7R-CERM 0201
R9441 100K 5% 1/20W MF 201
C9402 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=D8_AARON SYNC_DATE=03/13/2012
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INTERNAL DP (STRAIGHT)

518S0852 CRITICAL
J9500
205-23-140E-01
F-RT-SM

L9500
FERR-120-OHM-3A
0603
155S0367
=PP12V_S0_LCD → PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C9520 10UF 10% 16V X5R-CERM 0805
C9501 0.001UF 20% 50V CERM 0402

Display TCon Master
- I2C_TCON_MAS_SDA
- I2C_TCON_MAS_SCL

Display TCon Slave
- =I2C_TCON_SLA_SDA
- =I2C_TCON_SLA_SCL

- DP_INT_SPDIF_AUDIO
- DP_INTPNL_HPD
- DP_INTPNL_AUX_N
- DP_INTPNL_AUX_P
- DP_INTPNL_ML_P<0>
- DP_INTPNL_ML_N<0>
- DP_INTPNL_ML_P<1>
- DP_INTPNL_ML_N<1>
- DP_INTPNL_ML_P<2>
- DP_INTPNL_ML_N<2>
- DP_INTPNL_ML_P<3>
- DP_INTPNL_ML_N<3>
- VIDEO_ON
- BLC_VSYNC

518S0778
DEVELOPMENT
CRITICAL
J9520
53780-8606
M-RT-SM

DEVELOPMENT
L9520
FERR-250-OHM
SM
=PP12V_S0_LCD → PP12V_LCD_EXT
VOLTAGE=12V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C9530 10UF 10% 16V X5R-CERM 0805 DEVELOPMENT
C9531 0.001UF 20% 50V CERM 0402 DEVELOPMENT

K6X BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video

R9505 0 5% 1/16W MF-LF 402 used by diag LED
VIDEO_ON_L

=PP3V3_S0_DP
C9502 0.1UF 20% 10V CERM 402
U9501 74AUP2G14GM SOT886
VIDEO_ON → VIDEO_ON_K6X_L
D9501 BAT54XG SOT23
R9503 20.0K 1% 1/16W MF-LF 402
VIDEO_ON_L_DLY
C9503 10UF 10% 16V X5R-CERM 0805
U9502 74AUP2G14GM SOT886
C9504 0.1UF 20% 10V CERM 402
R9504 47 5% 1/16W MF-LF 402
LCD_BKL_ON_DLY → BLC_EN

Backlight Control

U9500 OUTPUT Y2 IS A NON-INVERTED, DELAYED VERSION OF INPUT A
The delay applies only on a L->H transition on A. This guarantees video is valid before the backlight is enabled.
On a H->L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video
Y1 is simply an inverted version of A, with no delay

=PP3V3_S0_DP
NOSTUFF C9506 0.1UF 20% 10V CERM 402

U9500 SN1105002 SC70 CRITICAL
VCC, A, NC, GND, Y1, Y2
VIDEO_ON
VIDEO_ON_D8_L
BLC_EN_DELAY

NOSTUFF R9506 0 5% 1/16W MF-LF 402 → VIDEO_ON_L, TO DIAGS LED
NOSTUFF R9502 0 5% 1/16W MF-LF 402 → BLC_EN, To BLC
NOSTUFF R9501 0 5% 1/16W MF-LF 402

=PP3V3_S0_DP
U9501 74AUP2G14GM SOT886 NC
U9502 74AUP2G14GM SOT886 NC

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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

48 6 =PP3V3_S4_TBTBPWRSW

CRITICAL C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM

CRITICAL C9680 22UF 20% 6.3V X5R-CERM-1 603

C9681 0.1UF 20% 10V CERM 402

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

6 =PPHV_SW_TBTBPWRSW

18.9V Max

C9615 4.7UF 10% 25V X5R-CERM 0603

C9610 0.1UF 10% 50V X7R 603-1

CRITICAL U9610 CD3210A0RGP QFN

V3P3 19,20 | VHV 6,7 | V3P3OUT 18 | NC | OUT 12,14 | RSVD 16 | RSVD 15 | EN 5 | HV_EN 11 | S0 17 | ISET_V3P3 8 | ISET_S0 10 | ISET_S3 9 | GND 1,2,3,4,13,21 | THRM PAD

16 PPHV_SW_TBTBPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V

C9611 0.1UF 10% 50V X7R 603-1

48 IN =TBTBPWRSW_EN

117 36 IN TBT_B_HV_EN

86 64 IN =TBT_S0_EN

TBTBPWRSW_ISET_V3P3

TBTBPWRSW_ISET_S0

TBTBPWRSW_ISET_S3

TBTHV:P15V R9610 22.6K 1% 1/16W MF-LF 402

TBTHV:P15V R9611 22.6K 1% 1/16W MF-LF 402

R9612 36.5K 1% 1/16W MF-LF 402

12V: See below

TBTBPWRSW_ISET_S3_R

TBTBPWRSW_ISET_S0_R

TBTHV:P15V R9613 22.6K 1% 1/16W MF-LF 402

TBTHV:P15V R9614 22.6K 1% 1/16W MF-LF 402

Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9610,R9613		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

88 86 38 37 36 6 =PP3V3_S4_TBT

C9620 0.1UF 10% 6.3V X5R 201

C9621 0.1UF 10% 6.3V X5R 201

R9627 10K 5% 1/20W MF 201

R9629 100K 5% 1/20W MF 201

CRITICAL U9620 CBTL05023 HVQFN

VDD 3,15 | BIASIN 1 | AUXIO_EN 2 | AUX- 7 | AUX+ 8 | DDC_DAT 4 | DDC_CLK 5 | CA_DETOUT 16 | DP+ 11 | DP- 10 | LSTX 14 | LSRX 13 | DP_PD 6 | HPDOUT 12 | BIASOUT 24 | AUXIO- 23 | AUXIO+ 22 | CA_DET 18 | DPMLO+ 19 | DPMLO- 20 | GND_THMPAD 9,21,25

TBT_B_BIAS VOLTAGE=3.3V

C9625 0.1UF 10% 6.3V X5R 201

36 IN TBT_B_CIO_SEL

112 86 15 IN DP_AUXIO_EN

107 36 BI DP_TBTPB_AUXCH_C_N

107 36 BI DP_TBTPB_AUXCH_C_P

C9630 0.1UF 10% 6.3V X5R 201

C9631 0.1UF 10% 6.3V X5R 201

107 DP_TBTPB_AUXCH_N

107 DP_TBTPB_AUXCH_P

112 85 BI DP_TBTPB_DDC_DATA

112 85 IN DP_TBTPB_DDC_CLK

107 36 OUT TBT_B_CONFIG1_BUF

107 36 IN DP_TBTPB_ML_C_P<1>

107 36 IN DP_TBTPB_ML_C_N<1>

C9632 0.22UF 20% 6.3V X5R 0201

C9633 0.22UF 20% 6.3V X5R 0201

107 DP_TBTPB_ML_P<1>

107 DP_TBTPB_ML_N<1>

107 36 IN TBT_B_LSTX

TBT_B_LSRX_UNBUF

36 IN TBT_B_DP_PWRDN

112 36 OUT DP_TBTPB_HPD

DP_B_AUXCH_DDC_N 88 107

DP_B_AUXCH_DDC_P 88 107

TBT: RX_1 Bias Sink

TBT_B_CONFIG1_RC 88 117

DP_B_LSX_ML_P<1> 88 107

DP_B_LSX_ML_N<1> 88 107

TBT: LSX_A_R2P/P2R (P/N)

TBT_B_HPD 88

88 86 38 37 36 6 =PP3V3_S4_TBT

CRITICAL U9660 74AUP1T97 SOT891

107 36 OUT TBT_B_LSRX

C9660 0.1UF 10% 16V X5R-CERM 0201

R9626 1M 5% 1/20W MF 201

R9628 100K 5% 1/20W MF 201

L9600 FERR-120-OHM-3A 0603

PP3V3R1V_SW_TBTBPWR 115 2 1

MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V

C9600 0.01UF 10% 50V X7R-CERM 0402

C9601 0.01UF 10% 50V X7R-CERM 0402

TBTBCONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V

R9601 12 5% 1/20W MF 201

TBT Dir DP Dir

GND_VOID=TRUE (Both C's)

C9674 0.47UF 20% 4V CERM-X5R-1

C9675 0.47UF 20% 4V CERM-X5R-1

107 36 OUT TBT_B_D2R_N<0>

107 36 OUT TBT_B_D2R_P<0>

107 TBT_B_D2R_C_P<0>

107 TBT_B_D2R_C_N<0>

NOTE: Polarity Swapped for Layout!

R9694 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9695 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

C9678 0.22UF 20% 6.3V X5R 0201

C9679 0.22UF 20% 6.3V X5R 0201

107 36 IN DP_TBTPB_ML_C_P<3>

107 36 IN DP_TBTPB_ML_C_N<3>

107 DP_TBTPB_ML_P<3>

107 DP_TBTPB_ML_N<3>

R9678 470K 5% 1/20W MF 201

R9679 470K 5% 1/20W MF 201

TBT: Terminated

117 88 TBT_B_BIAS

R9698 2.2K 5% 1/20W MF 201

R9699 2.2K 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)

C9676 0.47UF 20% 4V CERM-X5R-1

C9677 0.47UF 20% 4V CERM-X5R-1

107 36 OUT TBT_B_D2R_N<1>

107 36 OUT TBT_B_D2R_P<1>

107 TBT_B_D2R_C_P<1>

107 TBT_B_D2R_C_N<1>

NOTE: Polarity Swapped for Layout!

CRITICAL

GND_VOID=TRUE (Both D's)

D9698 BAR90-02LRH TSLP-2-7

D9699 BAR90-02LRH TSLP-2-7

107 TBT_B_D2R1_AUXDDC_P

107 TBT_B_D2R1_AUXDDC_N

CRITICAL L9698 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY

CRITICAL L9699 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY

107 88 DP_B_AUXCH_DDC_P

107 88 DP_B_AUXCH_DDC_N

C9698 30PF 5% 50V C0G-NP0 0402

C9699 30PF 5% 50V C0G-NP0 0402

88 TBT_B_HPD

117 88 TBT_B_CONFIG1_RC

107 36 OUT TBT_B_CONFIG2_RC

R9652 1M 5% 1/20W MF 201

R9651 1M 5% 1/20W MF 201

C9694 330PF 10% 16V X7R-CERM 0201

C9695 330PF 10% 16V X7R-CERM 0201

R9641 100K 5% 1/20W MF 201

C9602 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL

J9400 DUAL-MDP-D8 F-ANG-TH

SHLD 58,57,56,55,54,53

HPD 22 | CONFIG1 24 | CONFIG2 26 | GND2 28 | ML_LANE3P 30 | ML_LANE3N 32 | GND4 34 | AUX_CHP 36 | AUX_CHN 38 | DP_PWR 40

GND0 21 | ML_LANE0P 23 | ML_LANE0N 25 | GND1 27 | ML_LANE1P 29 | ML_LANE1N 31 | GND3 33 | ML_LANE2P 35 | ML_LANE2N 37 | RETURN 39

PORT B SHLD 65,64,63,62,61,60,59

514-0831

C9605 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V

(0-18.9V)

DP Dir TBT Dir

107 TBT_B_R2D_P<0>

107 TBT_B_R2D_N<0>

TBT: TX_0

C9606 0.01UF 10% 25V X5R-CERM 0201

TBTBCONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V

(0-18.9V)

TBT: LSX_R2P/P2R (P/N)

107 TBT_B_R2D_P<1>

107 TBT_B_R2D_N<1>

TBT: TX_1

GND_VOID=TRUE (Both C's)

C9670 0.22UF 20% 6.3V X5R 0201

C9671 0.22UF 20% 6.3V X5R 0201

TBT_B_R2D_C_P<0> IN 36 107

TBT_B_R2D_C_N<0> IN 36 107

R9670 470K 5% 1/20W MF 201

R9671 470K 5% 1/20W MF 201

NOTE: Polarity Swapped for Layout!

GND_VOID=TRUE (Both C's)

C9672 0.22UF 20% 6.3V X5R 0201

C9673 0.22UF 20% 6.3V X5R 0201

TBT_B_R2D_C_N<1> IN 36 107

TBT_B_R2D_C_P<1> IN 36 107

R9672 470K 5% 1/20W MF 201

R9673 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=D8_AARON SYNC_DATE=03/13/2012

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14V BLC PRE-REGULATOR

L9703 1KOHM-25%-0.6A 0603
L9704 1KOHM-25%-0.6A 0603
NOSTUFF L9702 1KOHM-25%-0.6A 0603
R9701 0.100 0.1% 1/4W MF 1206
C9735 2.2UF 10% 16V X5R 603
C9733 1000PF 5% 25V CERM 603
C9734 2.2UF 10% 16V X5R 603
=PP3V3_S0_BLC
PP3V3_S0_BLC_R
BLC_P3V3S
BLC_P3V3A
BLC_P3V3_REF

R9752 0.001 1% 1W MF-LF 2512
L9740 12UH-7A-0.02OHM PIMB136T-8M NOSTUFF
D9740 TO277A SS12P4S
Q9741 NOSTUFF FDMS6681Z POWER56
C9748 10UF 10% 35V X5R 1210
C9749 470UF 20% 25V ELEC 10X10.8-SM
PRE_REG_OUT
C9747 0.068UF 10% 50V X7R-CERM 0603
R9751 49.9K 1% 1/10W MF-LF 603
R9750 49.9K 1% 1/10W MF-LF 603
BOOST_BYPASS_GATE
BOOST_BYPASS
Q9740 CSD16412Q5A MLP5X6-LFPAK-Q5A

R9743 330K 5% 1/10W MF-LF 603
NOSTUFF R9744 10 1% 1/8W MF-LF 805
C9742 270PF 5% 50V CERM 603
C9743 1.0UF 10% 50V X7R 0805
PP12V_S0_BLC_VIN

U9740 TPS40210 MSOP
DIS/EN* BP GDRV ISNS COMP FB SS RC GND THRM_PAD
BOOST_EN_L
BOOST_COMP_C
R9742 10K 1% 1/10W MF-LF 603
C9741 0.1UF 10% 50V X7R 603-1
C9740 1500PF 10% 50V CERM 603
R9740 0 5% 1/10W MF-LF 603
R9741 22K 5% 1/10W MF-LF 603
R9747 30.1 1% 1/10W MF-LF 603
R9748 1.0K 1% 1/10W MF-LF 603
R9745 1.10K 1% 1/8W MF-LF 805
C9746 0.1UF 10% 50V X7R 603-1
C9744 1.0UF 10% 16V X7R 0805
C9745 390PF 10% 50V X7R-CERM 0402
R9749 0.010 1% 1W MP 2010
BOOST_BP
BOOST_GDRV
BOOST_GDRV_R
BOOST_ISNS
BOOST_ISNS_R
BOOST_FB
BOOST_SS
BOOST_RC
BOOST_VDD
BOOST_FET_DRAIN

PM_PCH_PWROK
PCH_BLC_EXT_BOOT
U9710 74LVC2G08 SOT902
CRITICAL Q9711 SSM3K15AMFVAPE VESM
NOSTUFF R9711 100K 5% 1/16W MF-LF 402
BLC_EXT_BOOT_L
BLC_EXT_BOOT
0 R9712 5% 1/16W MF-LF 402
SMB_PCH_BLC_SDA

D8:SUOPERTEX GPIOS FOR BLC ISP RDAR://10987156

PM_PCH_PWROK
PCH_BLC_MCU_RESET
U9710 74LVC2G08 SOT902
CRITICAL Q9710 SSM3K15AMFVAPE VESM
NOSTUFF R9710 100K 5% 1/16W MF-LF 402
BLC_MCU_RESET_R_L
BLC_MCU_RESET_L
0 R9713 5% 1/16W MF-LF 402
BLC_MCU_RESET

C9710 0.1UF 10% 6.3V X5R 201
C9701 1000PF 5% 50V C0G-CERM 603
C9702 1000PF 5% 50V C0G-CERM 603
C9703 1000PF 5% 50V C0G-CERM 603
C9704 0.1UF 10% 16V X7R-CERM 0402
C9708 0.1UF 10% 16V X7R-CERM 0402
C9709 1000PF 5% 50V C0G-CERM 603

NOSTUFF R9732 10K 5% 1/16W MF-LF 402
R9733 10K 5% 1/16W MF-LF 402
SMC_BLC_MUX_RX_L
SMC_BLC_MUX_TX_L
R9730 0 5% 1/16W MF-LF 402
R9731 0 5% 1/16W MF-LF 402
BLC_MCU_TXD0
BLC_MCU_RXD0

MCU ISP PROG AND TEST CONNECTOR
DEVELOPMENT J9700 CF20151D0R0-NH F-RT-SM
APN 998-3605
(WAS BLC_BLON)
BLC_EN
LCD_BKLT_PWM
BLC_VSYNC
BLC_MCU_TXD0
BLC_MCU_RXD0
BLC_MCU_B_SDA_CONN
BLC_MCU_RESET_L
BLC_MCU_TRST
BLC_MCU_TDI
BLC_MCU_TMS
BLC_MCU_TCK
BLC_MCU_RTCK
BLC_MCU_TDO
SMB_PCH_BLC_SDA
NOSTUFF J9701 HB3902U-L M-ST-TH

NOSTUFF R9720 4.7K 5% 1/16W MF-LF 402
NOSTUFF R9721 4.7K 5% 1/16W MF-LF 402
NOSTUFF R9718 4.7K 5% 1/16W MF-LF 402
NOSTUFF R9719 4.7K 5% 1/16W MF-LF 402
NOSTUFF R9726 0 5% 1/16W MF-LF 402
R9702 1K 5% 1/16W MF-LF 402
R9703 100K 5% 1/16W MF-LF 402
R9797 0 5% 1/16W MF-LF 402
R9705 10K 5% 1/16W MF-LF 402
R9706 1K 5% 1/16W MF-LF 402
R9707 100K 5% 1/16W MF-LF 402
BLC_UVLO
BLC_VSYNC
FLAG_V
STRCLK_R1
LCD_BKLT_PWM
BLC_DIM_MCU
LED_DRIVER_OVP1P
LED_DRIVER_OVP2P
LED_DRIVER_OVP3P
SMB_TCON_BLC_SCL
SMB_TCON_BLC_SDA
BLC_GOOD
BLC_ENA
BLC_MCU_UVLO
BLC_MCU_FLAG_V
BLC_MCU_PWM5
BLC_VSYNC_R
BLC_PWM_1_R
BLC_PWM_2_R
BLC_PWM_3_R
TP_BLC_MCU_TP_2

U9700 LPC2132FBD64 LQFP
VDD VDDA VREF VBAT OMIT_TABLE VSS VSSA
P0.0/TXD0/PWM1
P0.1/RXD0/PWM3/EINT0
P0.2/SCL0/CAP0.0
P0.3/SDA0/MAT0.0/EINT1
P0.4/SCK0/CAP0.1/AD0.6
P0.5/MISO0/MAT0.1/AD0.7
P0.6/MOSI0/CAP0.2
P0.7/SSEL0/PWM2/EINT2
P0.8/TXD1/PWM4
P0.9/RXD1/PWM6/EINT3
P0.10/CAP1.0
P0.11/CAP1.1/SCL1
P0.12/MAT1.0
P0.13/MAT1.1
P0.14/EINT1/SDA1
P0.15/EINT2
P0.16/EINT0/MAT0.2/CAP0.2
P0.17/CAP1.2/SCK1/MAT1.2
P0.18/CAP1.3/MISO1/MAT1.3
P0.19/MAT1.2/MOSI1/CAP1.2
P0.20/MAT1.3/SSEL1/EINT3
P0.21/PWM5/CAP1.3
P0.22/CAP0.0/MAT0.0
P0.23
P0.25/AD0.4/AOUT
P0.26/AD0.5
P0.27/AD0.0/CAP0.1/MAT0.1
P0.28/AD0.1/CAP0.2/MAT0.2
P0.29/AD0.2/CAP0.3/MAT0.3
P0.30/AD0.3/EINT3/CAP0.0
P0.31
P1.16/TRACEPKT0 P1.17/TRACEPKT1 P1.18/TRACEPKT2 P1.19/TRACEPKT3 P1.20/TRACESYNC P1.21/PIPESTAT0 P1.22/PIPESTAT1 P1.23/PIPESTAT2 P1.24/TRACECLK P1.25/EXTIN0 P1.26/RTCK P1.27/TDO P1.28/TDI P1.29/TCK P1.30/TMS P1.31/TRST* (IPU)
RESET* XTALI XTALO RTCX1 RTCX2

(WAS BLC_GPIO)
TP_PCH_GPIO6_TACH2
BLC_EN_R
R9727 10K 5% 1/16W MF-LF 402
C9725 1000PF 5% 50V C0G-CERM 603
R9728 1K 5% 1/16W MF-LF 402
BLC_EN IS DRIVEN BY TCON (CSA95)

BLC_MCU_RTCK BLC_MCU_TDO BLC_MCU_TDI BLC_MCU_TCK BLC_MCU_TMS BLC_MCU_TRST
BLC_MCU_RESET_L
D9700 BAS316DG SOD323-SM
C9705 1UF 10% 16V X5R 402
R9715 10K 5% 1/16W MF-LF 402
BLC_MCU_XTAL_IN
BLC_MCU_XTAL_OUT_R
BLC_MCU_XTAL_OUT
R9716 0 5% 1/16W MF-LF 402
R9717 10M 5% 1/16W MF-LF 402
CRITICAL Y9705 3.2X2.5MM-SM 12.000MHZ-30PPM-10PF-85C
C9706 18PF 5% 50V COG-CERM 0402
C9707 18PF 5% 50V COG-CERM 0402

U9770 L78M08ABDT DPAK
PP12V_S0_BLC_VIN2
PP8V_BLC
C9770 4.7UF 20% 25V X5R-CERM 0603
C9771 2.2UF 10% 25V X5R-CERM 603
353S3748

C9790 0.1UF 10% 16V X7R-CERM 0402
U9780 74LVC1G08GW SOT353
BLC_ENA1
R9780 100K 1% 1/10W MF-LF 603
R9781 100K 5% 1/16W MF-LF 402

Q9700 BSH111DG SOT23-3
R9725 10K 1% 1/10W MF-LF 603
BLC_MCU_BV
R9722 0 5% 1/16W MF-LF 402
R9724 10K 1% 1/10W MF-LF 603
C9722 1000PF 5% 50V C0G-CERM 603

U9720 REF3333 SOT23-3
C9720 2.2UF 10% 16V X5R 603
C9721 4.7UF 10% 6.3V X5R-CERM 603

D8 PROTO 2 BLC ADDING 3.3V VOLTAGE REFERENCE RDAR://11280328

U9790 74LVC1G08GW SOT353
R9791 10K 5% 1/16W MF-LF 402
R9790 10K 5% 1/16W MF-LF 402
C9792 0.1UF 10% 16V X7R-CERM 0402
Q9701 2N7002 SOT23-HF1
R9793 10K 5% 1/16W MF-LF 402
R9792 10K 5% 1/16W MF-LF 402
C9791 0.1UF 10% 16V X7R-CERM 0402
BLC_P_ON
BLC_BST
BLC_BST_R
BOOST_EN_GATE
BOOST_EN_L
PP5V_S0_BLC_R

BLC MCU

SYNC_MASTER=D8_MLB SYNC_DATE=04/23/2012
PAGE TITLE: Backlight Controller MCU
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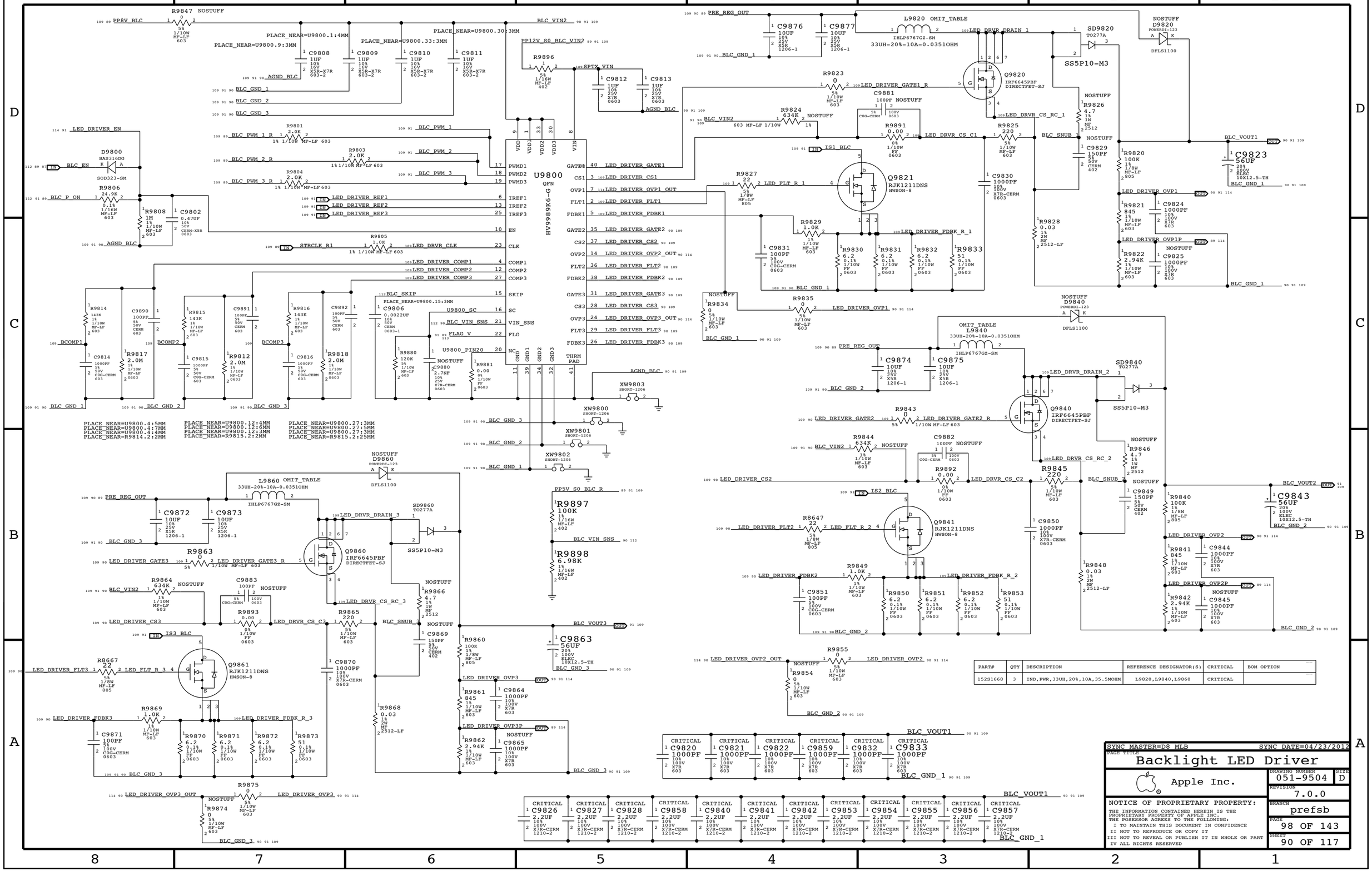

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	3	IND,PWR,33UH,20%,10A,35.5MOHM	L9820,L9840,L9860	CRITICAL	

SYNC_MASTER=D8_MLB SYNC_DATE=04/23/2012

PAGE TITLE: Backlight LED Driver

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Output Current Adjustment

R9931 10.0K 0.1% 1/16W MF-LF 603 — BLC_P3V3_REF → BLC_MCU_AOUT_R
R9940 0 5% 1/10W MF-LF 603 — OCA_FET_DRAIN → AGND_BLC
R9932 3.57K 0.1% 1/10W FF 603
R9933 3.57K 0.1% 1/10W FF 603
C9931 1UF 10% 16V X5R 603
R9941 100K 1% 1/10W MF-LF 603 — BLC_VIN2
Q9940 2N7002 SOT23-HF1
R9943 100K 1% 1/10W MF-LF 603 — LED_DRIVER_EN_L_R → LED_DRIVER_EN_L
Q9941 BSH111DG SOT23-3 — LED_DRIVER_EN
NOSTUFF C9942 1UF 10% 25V X5R 603-1
R9942 499K 1% 1/10W MF-LF 603

R9934 10 5% 1/10W MF-LF 603 — LED_DRIVER_REF1 (OUT) → C9934 1UF 10% 16V X5R 603, C9935 0.1UF 10% 50V X7R 603-1 → BLC_GND_1
R9936 10 5% 1/10W MF-LF 603 — LED_DRIVER_REF2 (OUT) → C9936 1UF 10% 16V X5R 603, C9937 0.1UF 10% 50V X7R 603-1 → BLC_GND_2
R9938 10 5% 1/10W MF-LF 603 — LED_DRIVER_REF3 (OUT) → C9938 1UF 10% 16V X5R 603, C9939 0.1UF 10% 50V X7R 603-1 → BLC_GND_3

Backlight Connector

R9920 0 5% 1/8W MF-LF 805 — NOSTUFF L9920 250-OHM-5A DLW5BT-SM-HF
L9921 220-OHM-1.4A 0603 — IS1_BLC → IS1_BLC_F → BLC_LED_N_1
R9921 0 5% 1/8W MF-LF 805 — BLC_VOUT1 → BLC_LED_P_1
R9922 0 5% 1/8W MF-LF 805 — NOSTUFF L9922 250-OHM-5A DLW5BT-SM-HF
L9923 220-OHM-1.4A 0603 — IS2_BLC → IS2_BLC_F → BLC_LED_N_2
R9923 0 5% 1/8W MF-LF 805 — BLC_VOUT2 → BLC_LED_P_2
R9924 0 5% 1/8W MF-LF 805 — NOSTUFF L9924 250-OHM-5A DLW5BT-SM-HF
L9925 220-OHM-1.4A 0603 — IS3_BLC → IS3_BLC_F → BLC_LED_N_3
R9925 0 5% 1/8W MF-LF 805 — BLC_VOUT3 → BLC_LED_P_3
J9920 504050-0691 M-RT-SM → 518S0862

IN-RUSH CURRENT LIMITER

F9900 10AMP-63V 1206 — =PP12V_S0_BLC → PP12V_S0_BLC_F
R9976 0.005 1% 1W MF 2512
Q9970 FDMS6681Z POWER56 — PP12V_S0_BLC_VIN2 → PP12V_S0_BLC_VINP
NOSTUFF C9971 0.068UF 10% 50V X7R-CERM 0603
C9998 1000PF 5% 25V CERM 603
C9999 1000PF 5% 25V CERM 603
C9972 4.7UF 20% 25V CERM 1206
C9973 4.7UF 20% 25V CERM 1206
C9974 100UF 20% 35V ELEC 6.3X8-SM-HF
R9975 10K 1% 1/10W MF-LF 603 — BLC_VINP_GATE
Q9971 BSS84 SOT23-3-HF — BLC_VIN2_SRC
R9977 215 1% 1W MF-LF 2512 — BLC_VIN2_SRC → BLC_VIN2_GATE
R9997 215 1% 1W MF-LF 2512
R9970 10K 5% 1/10W MF-LF 603
R9978 10K 1% 1/10W MF-LF 603 — BLC_P_ON_DRAIN
C9995 0.1UF 10% 16V X7R-CERM 0402 — BLC_P3V3S
U9960 74LVC1G08GW SOT353 — BLC_BL, BLC_ON_R
R9994 1K 5% 1/16W MF-LF 402 — PM_PGOOD_FET_P12V_S0_BLC
R9971 1K 5% 1/16W MF-LF 402 — BLC_ENA1
R9974 10K 5% 1/10W MF-LF 603 — BLC_ON_DRAIN
Q9973 BSH111DG SOT23-3 — BLC_ON
R9999 0 5% 1/16W MF-LF 402 — BLC12V_BYPASS:Y
R9972 100K 5% 1/10W MF-LF 603
NOSTUFF C9970 0.1UF 10% 50V X5R-CERM 0402

R9980 10K 5% 1/10W MF-LF 603
Q9972 BSH111DG SOT23-3 — BLC_P_ON_D_R
R9981 1.0K 5% 1/10W MF-LF 603 — BLC_P_ON_D
D9900 BAS316DG SOD323-SM — BLC_P_ON_BYPASS
R9979 1.0M 5% 1/10W MF-LF 603
NOSTUFF C9975 0.047UF 10% 16V CERM 603
C9996 0.1UF 10% 16V X7R-CERM 0402 — BLC_P3V3S
R9995 0 5% 1/16W MF-LF 402
BLC12V_BYPASS:Y R9998 0 5% 1/16W MF-LF 402
R9927 100K 5% 1/16W MF-LF 402 — FLAG_V_L
U9970 74LVC1G08GW SOT353 — BLC_P_ON_R
Q9974 BSH111DG SOT23-3 — FLAG_V
NOSTUFF R9996 0 5% 1/16W MF-LF 402

BLC12V BYPASS STUFFING OPTION

	BYPASS	NO BYPASS
R9998:	STUFF	NOSTUFF
R9995:	NOSTUFF	STUFF
R9999:	STUFF	NOSTUFF
R9994:	NOSTUFF	STUFF
R9976:	STUFF	NOSTUFF

OVP PROTECTION

R9928 0 5% 1/10W MF-LF 603 — =PP5V_S0_BLC → PP5V_S0_BLC_R
C9951 0.1UF 10% 16V X7R-CERM 0402
R9954 20K 0.5% 1/16W MF-LF 603 — BLC_P3V3_REF
R9955 499K 1% 1/10W MF-LF 603 — OVP_OREF
C9955 0.1UF 10% 50V X7R 603-1
U9950 LM324DEX SOI — LED_DRIVER_OVP1/2/3 → 1IN+/2IN+/3IN+; OVP_OUT1/2/3 ← 1OUT/2OUT/3OUT; 4OUT → NC; GND → AGND_BLC
R9951 0 5% 1/10W MF-LF 603 — OVP_OUT1 → OVP_OUT1_R → Q9951 BSH111DG SOT23-3 → BLC_PWM_1
R9952 0 5% 1/10W MF-LF 603 — OVP_OUT2 → OVP_OUT2_R → Q9952 BSH111DG SOT23-3 → BLC_PWM_2
R9953 0 5% 1/10W MF-LF 603 — OVP_OUT3 → OVP_OUT3_R → Q9953 BSH111DG SOT23-3 → BLC_PWM_3
All Q9951/Q9952/Q9953 → AGND_BLC

CRITICAL C9980–C9991 2.2UF 10% 100V X7R-CERM 1210-2 — BLC_VOUT2 → BLC_GND_2
CRITICAL C9944–C9949 1000PF 10% 100V X7R 603 — BLC_VOUT2 → BLC_GND_2
CRITICAL C9920–C9961 2.2UF 10% 100V X7R-CERM 1210-2 — BLC_VOUT3 → BLC_GND_3
CRITICAL C9965–C9990 1000PF 10% 100V X7R 603 — BLC_VOUT3 → BLC_GND_3

UVP PROTECTION

PWM <= 50% -> TURN ON BOOST
PWM > 50% -> TURN OFF BOOST

R9961 0 5% 1/10W MF-LF 603
R9962 10K 1% 1/10W MF-LF 603
R9963 2.0M 1% 1/10W MF-LF 0603
C9962 1UF 10% 16V X5R 603
R9964 130K 1% 1/10W MF-LF 603
C9963 0.1UF 10% 50V X7R 603-1
R9965 56K 5% 1/10W MF-LF 603
R9966 0 5% 1/10W MF-LF 603
C9964 1UF 10% 16V X5R 603
R9967 1M 1% 1/10W MF-LF 603
R9968 2.0M 1% 1/10W MF-LF 0603
D9901 BAS316DG SOD323-SM — BLC_MCU_BV → BLC_MCU_BV_R
D9902 BAS316DG SOD323-SM — BLC_MCU_BV → BLC_MCU_BV_D
U9920 LM324DEX SOI — UVP_IN_1/1_REF/2/3/4 → 1IN+/1IN-/2IN+/2IN-/3IN+/3IN-/4IN+/4IN-; 1OUT → BLC_P_ON_GATE; 2OUT → BLC_BL_GATE; 3OUT → BLC_BST; GND
R9910 100K 1% 1/10W MF-LF 603 — PP12V_S0_BLC_VINP
R9912 100K 1% 1/10W MF-LF 603 — PP12V_S0_BLC_VIN2
C9912 0.1UF 10% 50V X7R 603-1
R9914 38.3K 1% 1/10W MF-LF 603
R9916 42.2K 1% 1/10W MF-LF 603 — BLC_P3V3_REF
C9910 0.1UF 10% 50V X7R 603-1
R9911 43K 1% 1/10W MF-LF 0603
C9911 0.1UF 10% 50V X7R 603-1
R9913 34.8K 1% 1/10W MF-LF 603
C9913 0.1UF 10% 50V X7R 603-1
R9915 10K 1% 1/10W MF-LF 603
R9917 71.5K 1% 1/10W MF-LF 603
C9997 0.1UF 10% 50V X7R 603-1
C9914 0.1UF 10% 50V X7R 603-1
R9918 10K 1% 1/10W MF-LF 603 — BLC_ENA1
Q9924 2N7002 SOT23-HF1 — BLC_P_ON
R9919 10K 5% 1/10W MF-LF 603 — BLC_P3V3S
Q9925 2N7002 SOT23-HF1 — BLC_BL
R9969 1.5M 5% 1/10W MF-LF 603
Q9926 2N7002 SOT23-HF1 — BOOST_BYPASS → BLC_BYPASS_GATE

UVLO VIN2 BLC_BL
2.5V @12V = "1"
2.0V @10V = "0" (SHUTDOWN)

SYNC_MASTER=D8_MLB SYNC_DATE=04/23/2012
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GPU CORE REG 1.1V/???A O/P= PPGPUCORE_S0_REG

=PP5V_S0_VRD → RB418 2.2 5% 1/8W MF-LF 805 (MAX_NECK_LENGTH=3MM, MIN_NECK_WIDTH=0.3MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=5V)

PP5V_S0_GPU_VCORE_VCC

NOSTUFF RB447 0 5% 1/16W MF-LF 402
NOSTUFF RB448 0 5% 1/16W MF-LF 402
NOSTUFF RB444 0 5% 1/16W MF-LF 402
NOSTUFF RB455 0 5% 1/16W MF-LF 402

VR_GPU_PWM1_R
VR_GPU_PWM2_R
VR_GPU_PWM3_R
VR_GPU_PWM4_R

GPU VCORE
VOUT = VCORE
PEAK = ???A
AVG = ???A

VSNS_GPU_VDD → VR_GPU_VSEN
SM OMIT XWB420
VOLTAGE=1.1V, NET_PHYSICAL_TYPE=ENS_DIFF_PAIR, SIGNAL_MODEL=EMPTY

VSNS_GPU_VSS → VR_GPU_RGND
XWB430 SM OMIT
VOLTAGE=0V, NET_PHYSICAL_TYPE=ENS_DIFF_PAIR

1.25 mOhm loadline

NOSTUFF CB401 0.0022UF 10% 50V CERM 402
CB402 0.0022UF 10% 50V CERM 402
CB403 0.0022UF 10% 50V CERM 402

AGND_GPU

CB404 47PF 5% 50V CERM 402 (VR_GPU_FB_R → VR_GPU_COMP_R)
CB405 0.0047UF 10% 25V CERM 402
RB401 8.06K 1% 1/16W MF-LF 402 (VR_GPU_COMP_RC)
RB479 0 5% 1/16W MF-LF 402
RB402 1K 1% 1/16W MF-LF 402 (VR_VDF_R1)
RB403 287 1% 1/16W MF-LF 402
CB406 0.001UF 10% 50V X7R-CERM 0402 (VR_VDF_R2)
RB449 47.5 1% 1/16W MF-LF 402

LOCAL 5V
NOSTUFF RB446 1M 5% 1/16W MF-LF 402
RB404 0 5% 1/16W MF-LF 402
CB407 1UF 10% 10V X6S-CERM 0402
AGND_GPU

VCC CRITICAL SYM_VER_2 UB400 ISL6334D QFN

VR_GPU_COMP	13	COMP
VR_GPU_FB	14	FB
VR_GPU_VDIFF	15	VDIFF
	17	VSEN
	16	RGND
VR_GPU_TCOMP	18	TCOMP
VR_GPU_OFS	9	OFS
VR_GPU_FS	34	FS
VR_GPU_SS	35	SS
VR_GPU_DAC	11	DAC
VR_GPU_REF	12	REF
VR_GPU_TM	39	TM
VR_GPU_EN_VTT	33	EN_VTT
	36	VR_RDY
	7	VID0
	6	VID1
	5	VID2
	4	VID3
	3	VID4
	2	VID5
	1	VID6
	40	VID7
	8	PSI*
VR_GPU_IMON_R	10	IMON
VR_GPU_FAN	37	H_CPURST_N
VR_GPU_VRDHOT	38	VR_HOT
	32	EN_PWR
	26	PWM1
	28	ISEN1+
	27	ISEN1-
	20	PWM2
	22	ISEN2+
	21	ISEN2-
	31	PWM3
	29	ISEN3+
	30	ISEN3-
	25	PWM4
	23	ISEN4+
	24	ISEN4-

PP5V_S0_GPU_VCORE_VCC

VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.

RB400 1.02K 1% 1/16W MF-LF 402
NOSTUFF RB405 20.0K 1% 1/16W MF-LF 402
NOSTUFF RB498 0 5% 1/16W MF-LF 402
RB477 100K 1% 1/16W MF-LF 402

LAYOUT: PLACE RTB401 NEAR HOT SPOT

RTB401 6.8K 0603
CB480 0.1UF 10% 10V CERM 402
RB406 0 5% 1/16W MF-LF 402
NOSTUFF RB407 21K 1% 1/16W MF-LF 402
RB408 75K 1% 1/16W MF-LF 402
NOSTUFF RB409 100K 1% 1/16W MF-LF 402

AGND_GPU

CB410 0.0033UF 10% 50V X7R-CERM 0402
RB410 2.15K 1% 1/16W MF-LF 402

=PP5V_S0_VRD → RB411 10K 0.1% 1/16W MF-LF 0402

PP5V_S0_GPU_VCORE_VCC

=PP3V3_S0_VRD → RB412 2.0K 5% 1/16W MF-LF 402

=PP3V3_S0_GPU

RB499 10K 0.1% 1/16W MF-LF 0402

RB414 49.9K 1% 1/16W MF-LF 402
RB415 49.9K 1% 1/16W MF-LF 402

PM_PGOOD_REG_GPUCORE_S0
GPU_PSI_L
VR_GPU_IMON

RB445 0 5% 1/16W MF-LF 402

RB417 10K 1% 1/16W MF-LF 402 (VR_GPU_IOUT_PD)
CB412 0.022UF 10% 16V X5R-X7R-CERM 0402
RB416 0 5% 1/16W MF-LF 402

DEFAULT: 0.9000V STEP: 12.5MV

=PP3V3_S0_GPU

NOSTUFF RB478 1K 1% 1/16W MF-LF 402
NOSTUFF RB470 1K 1% 1/16W MF-LF 402
NOSTUFF RB471 1K 1% 1/16W MF-LF 402
NOSTUFF RB472 1K 1% 1/16W MF-LF 402
NOSTUFF RB473 1K 1% 1/16W MF-LF 402
NOSTUFF RB474 1K 1% 1/16W MF-LF 402
NOSTUFF RB475 1K 1% 1/16W MF-LF 402
NOSTUFF RB476 1K 1% 1/16W MF-LF 402

REG_GPUCORE_VID7
REG_GPUCORE_VID6
REG_GPUCORE_VID5
REG_GPUCORE_VID4
REG_GPUCORE_VID3
REG_GPUCORE_VID2
REG_GPUCORE_VID1
REG_GPUCORE_VID0

NOSTUFF RB495 1K 1% 1/16W MF-LF 402
NOSTUFF RB496 1K 1% 1/16W MF-LF 402
NOSTUFF RB497 1K 1% 1/16W MF-LF 402
NOSTUFF RB480 1K 1% 1/16W MF-LF 402
NOSTUFF RB481 1K 1% 1/16W MF-LF 402
NOSTUFF RB482 1K 1% 1/16W MF-LF 402
NOSTUFF RB485 1K 1% 1/16W MF-LF 402
NOSTUFF RB483 1K 1% 1/16W MF-LF 402

NEED TO FIGURE OUT SEQUENCING FOR ENABLE

RB434 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_1 (OUT)

RB431 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS1_RR_2)
RB432 0 5% 1/16W MF-LF 402
NOSTUFF CB430 15PF 1% 50V COG 402
CB431 150PF 5% 50V CERM 402
CB432 0.1UF 10% 16V X7R-CERM 0402
CB433 220PF 5% 25V COG-CERM 0402
RB433 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_1
REG_ISEN_GCORE_1_P
REG_ISEN_GCORE_1_N

RB440 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_2 (OUT)

RB441 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS2_RR_2)
RB442 0 5% 1/16W MF-LF 402
NOSTUFF CB440 15PF 1% 50V COG 402
CB441 150PF 5% 50V CERM 402
CB442 0.1UF 10% 16V X7R-CERM 0402
CB443 220PF 5% 25V COG-CERM 0402
RB443 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_2
REG_ISEN_GCORE_2_P
REG_ISEN_GCORE_2_N

RB450 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_3 (OUT)

RB451 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS3_RR_2)
RB452 0 5% 1/16W MF-LF 402
NOSTUFF CB450 15PF 1% 50V COG 402
CB451 150PF 5% 50V CERM 402
CB452 0.1UF 10% 16V X7R-CERM 0402
CB453 220PF 5% 25V COG-CERM 0402
RB453 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_3
REG_ISEN_GCORE_3_P
REG_ISEN_GCORE_3_N

RB438 0 5% 1/16W MF-LF 402 → REG_PWM_GPUCORE_4 (OUT)

RB439 178 1% 1/16W MF-LF 402 (VR_GPU_ISNS4_RR_2)
RB420 0 5% 1/16W MF-LF 402
NOSTUFF CB460 15PF 1% 50V COG 402
CB461 150PF 5% 50V CERM 402
CB462 0.1UF 10% 16V X7R-CERM 0402
CB463 220PF 5% 25V COG-CERM 0402
RB421 1.02K 1% 1/16W MF-LF 402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_4
REG_ISEN_GCORE_4_P
REG_ISEN_GCORE_4_N

OMIT XWB401 SM
AGND_GPU
MAX_NECK_LENGTH=3MM, MIN_NECK_WIDTH=0.3MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=0V

THRM PAD 41

PM_EN_REG_GPUCORE_S0_R

RB484 0 5% 1/16W MF-LF 402 (PM_EN_REG_GPUCORE_S0)
NOSTUFF CB409 0.01UF 10% 16V X7R-CERM 0402

AGND_GPU

=PP12V_S0_REG_GPUCORE → PP12V_S0_GPUCORE_FLT
IMAX = 10.5A
CRITICAL LB400 0.36UH-30A-0.6MOHM SDP110808MR36MF-TH
152-0110

GPU CORE INPUT Filtering

SYNC_MASTER=D8_MLB SYNC_DATE=02/28/2012

PAGE TITLE: VReg GPU Core Phases

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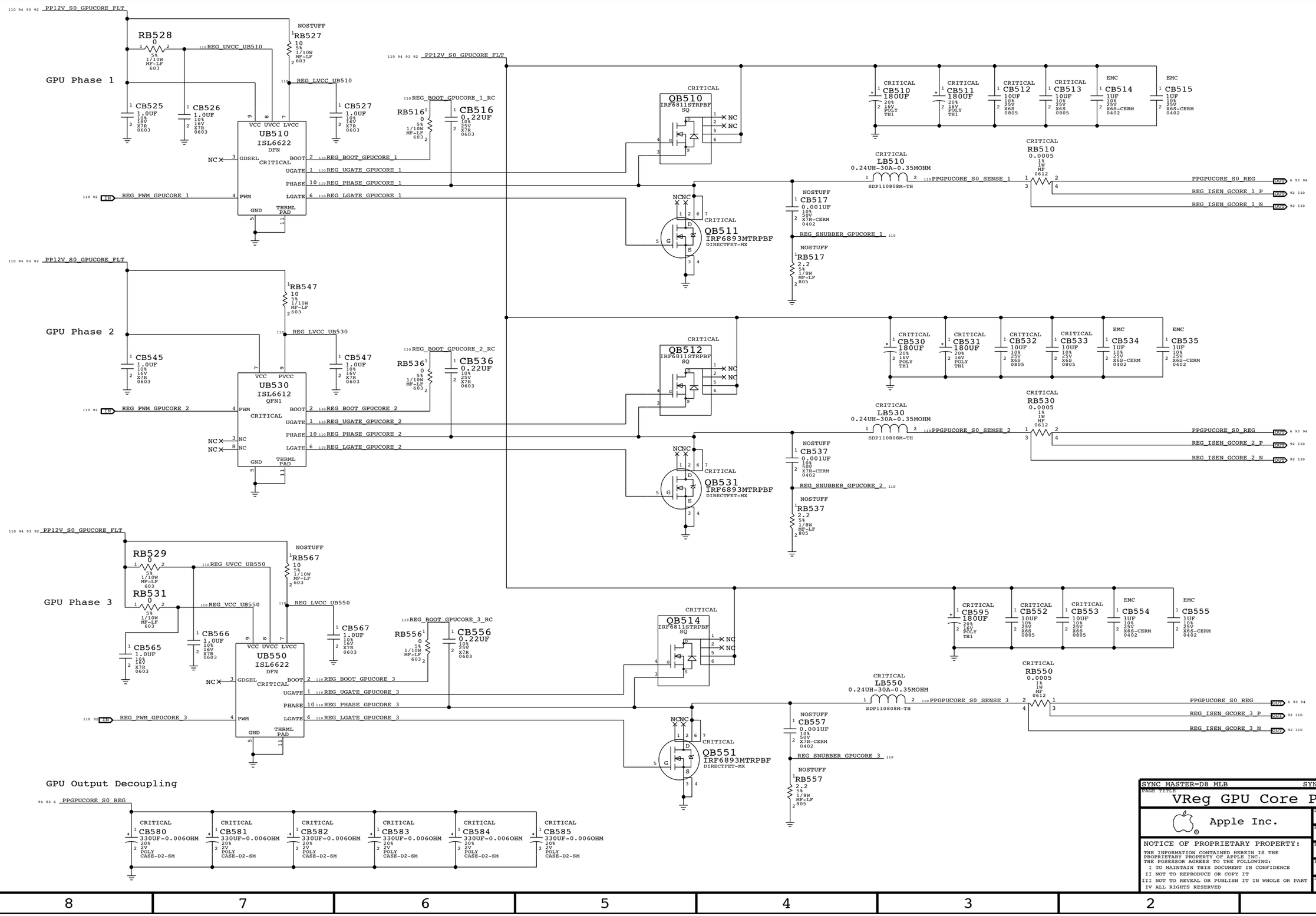

SYNC MASTER=D8_MLB SYNC DATE=02/25/2012

PAGE TITLE

VReg GPU Core Phases

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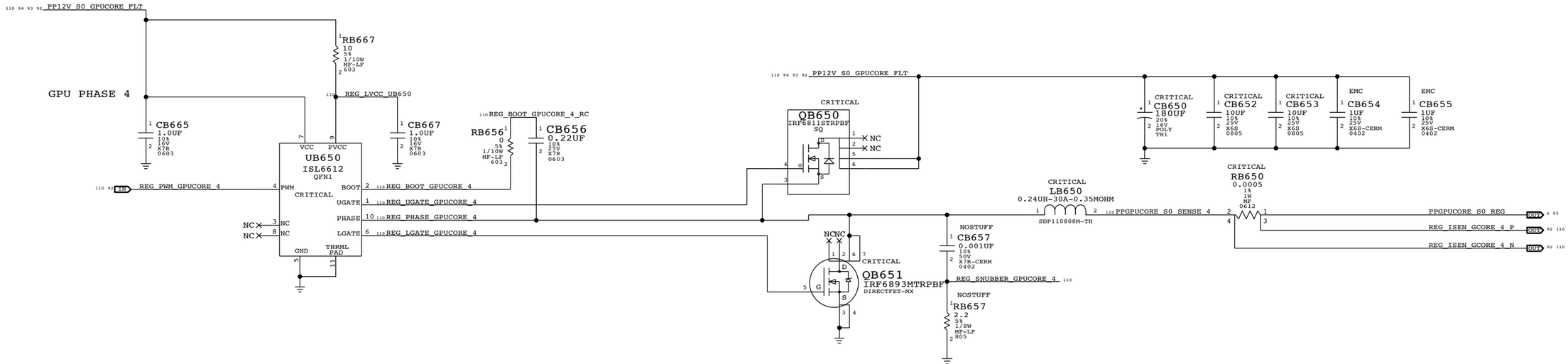

SYNC MASTER=D8 MLB SYNC DATE=02/06/2012

PAGE TITLE

VREG GPU CORE PHASE 4

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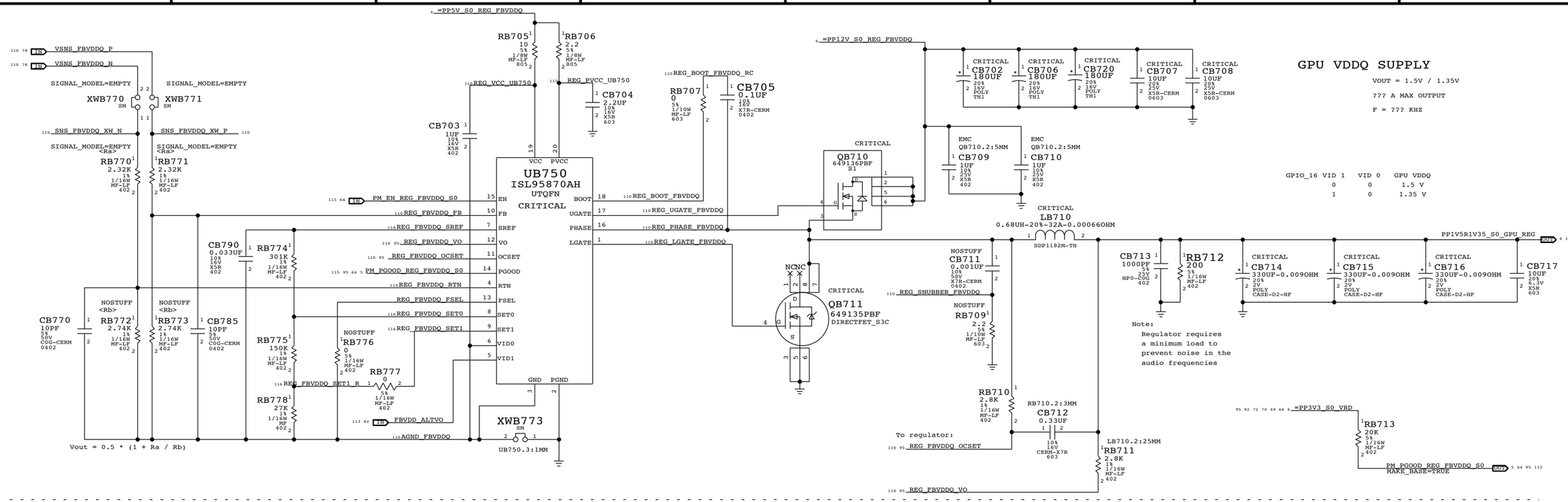

SYNC MASTER=D8 MLB
SYNC DATE=04/18/2012

PAGE TITLE
GPU VDDQ AND 1V05 GPU/PCH/TBT VREGS

Apple Inc.

DRAWING NUMBER 051-9504
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REVISION 7.0.0
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D8 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

Compensation Physical Rule Definition

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
COMP_SE	*	Y	0.305 MM	0.105 MM	3 MM	=STANDARD	=STANDARD

NOTE: line width based on 12 mil recommendation
NOTE: neck width based on 4 mil recommendation

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 MM	
2	Plane	1 oz	
	Core	0.101 MM	
3	Signal	0.5 oz	
	Prepreg	0.115 MM	
4	Plane	1 oz	
	Core	0.076 MM	
5	Signal	0.5 oz	
	Prepreg	0.380 MM	
6	Plane	1 oz	
	Core	0.076 MM	
7	Plane	1 oz	
	Prepreg	0.380 MM	
8	Signal	0.5 oz	
	Core	0.076 MM	
9	Plane	1 oz	
	Prepreg	0.115 MM	
10	Signal	0.5 oz	
	Core	0.101 MM	
11	Plane	1 oz	
	Prepreg	0.071 MM	
Btm	Signal	0.5 oz (Cu plated)	

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?
PM_ISO	*	=1:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	PM_ISO
PM	GND	*	DEFAULT

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

SYNC_MASTER=D8 KOSECOFF SYNC_DATE=03/19/2012

PAGE TITLE: D8 RULE DEFINITIONS

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DRAWING NUMBER: 051-9504 SIZE: D
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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_34S	BOTTOM	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_42S_D	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_42S_D	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR_PHY	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	TOP,BOTTOM	=5.5X_DIELECTRIC	?
DDR_CLK_ISO	ISL3,ISL10	=4.9X_DIELECTRIC	?
DDR_CLK_ISO	*	=6.5X_DIELECTRIC	?
DDR_CTRL_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CTRL_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CTRL_ISO	*	=5.3X_DIELECTRIC	?
DDR_CTRL2CTRL	TOP,BOTTOM	=3.0X_DIELECTRIC	?
DDR_CTRL2CTRL	ISL3,ISL10	=2.6X_DIELECTRIC	?
DDR_CTRL2CTRL	*	=3.5X_DIELECTRIC	?
DDR_CMD_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CMD_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CMD_ISO	*	=5.3X_DIELECTRIC	?
DDR_CMD2CMD	TOP,BOTTOM	=2.3X_DIELECTRIC	?
DDR_CMD2CMD	ISL3,ISL10	=2.0X_DIELECTRIC	?
DDR_CMD2CMD	*	=2.7X_DIELECTRIC	?
DDR_DATA_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_DATA_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_DATA_ISO	*	=5.3X_DIELECTRIC	?
DDR_DQ2DQ	TOP,BOTTOM	=3.2X_DIELECTRIC	900
DDR_DQ2DQ	ISL3,ISL10	=2.8X_DIELECTRIC	900
DDR_DQ2DQ	*	=3.8X_DIELECTRIC	900
DDR_DQ2DQS	TOP,BOTTOM	=3.7X_DIELECTRIC	?
DDR_DQ2DQS	ISL3,ISL10	=3.3X_DIELECTRIC	?
DDR_DQ2DQS	*	=4.4X_DIELECTRIC	?
DDR_BL2BL	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_BL2BL	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_BL2BL	*	=5.3X_DIELECTRIC	?
DDR_CH2CH	TOP,BOTTOM	=9.1X_DIELECTRIC	?
DDR_CH2CH	ISL3,ISL10	=8.2X_DIELECTRIC	?
DDR_CH2CH	*	=10.9X_DIELECTRIC	?
CMD2DATA_ISO	TOP,BOTTOM	=7X_DIELECTRIC	?
CMD2DATA_ISO	ISL3,ISL10	=5X_DIELECTRIC	?
CMD2DATA_ISO	*	=5X_DIELECTRIC	?

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR_ISO	*	=4.3X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER_DDR	*	*	POWER_DDR_ISO

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD
DDR_CMD	DDR_A_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_A_DQS*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQS*	*	CMD2DATA_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	12 29
DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	12 29
DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	12 30
DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	12 30
DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	12 29
DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	12 29
DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	12 29
DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	12 30
DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	12 30
DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	12 30
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	12 29 30
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	12 29 30
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	12 29 30
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	12 29 30
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	12 29 30
DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 33
DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 33
DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 33
DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 33
DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 33
DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 33
DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 33
DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 33
DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	12 33
DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	12 33
DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	12 33
DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	12 33
DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	12 33
DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	12 33
DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	12 33
DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	12 33
DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	12 33
DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	12 33
DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	12 33
DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	12 33
DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	12 33
DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	12 33
DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	12 33
DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	12 33
Channel B				
DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	12 31
DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	12 31
DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	12 32
DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	12 32
DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	12 31
DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	12 31
DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	12 31
DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	12 32
DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	12 32
DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	12 32
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	12 31 32
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	12 31 32
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	12 31 32
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	12 31 32
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	12 31 32
DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 33
DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 33
DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 33
DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 33
DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 33
DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 33
DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 33
DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 33
DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	12 33
DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	12 33
DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	12 33
DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	12 33
DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	12 33
DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	12 33
DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	12 33
DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	12 33
DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	12 33
DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	12 33
DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	12 33
DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	12 33
DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	12 33
DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	12 33
DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	12 33
DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	12 33
Reset				
DDR_A_RESET_L	DDR_SUS	CPU	MEM_RESET_L	28 29 30 31 32

SYNC_MASTER=D8 KOSECOFF SYNC_DATE=03/19/2012

PAGE TITLE: DDR3 Constraints

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D
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PCI EXPRESS

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	COMP_SE

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_ISO	*	=4X_DIELECTRIC	?
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO

PCIe Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	85	16	15.75	PCIe Gen2, PCIe Gen3, DMI

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x1 AirPort				
T59 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	NO_TEST=TRUE 35
T60 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	NO_TEST=TRUE 35
T61	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	NO_TEST=TRUE 18 35
T63	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	NO_TEST=TRUE 18 35
T65 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	NO_TEST=TRUE 18 35
T66 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	NO_TEST=TRUE 18 35
T60 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	18 35
T60 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	18 35
x1 Caesar IV				
T61 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	NO_TEST=TRUE 39
T60 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	NO_TEST=TRUE 39
T61	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	NO_TEST=TRUE 18 39
T63	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	NO_TEST=TRUE 18 39
T61 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	NO_TEST=TRUE 18 39
T61 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	NO_TEST=TRUE 18 39
T61	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	NO_TEST=TRUE 39
T61	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	NO_TEST=TRUE 39
T61 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	18 39
T61 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	18 39

PCIE (PCH - TBT)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
T57 PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<2..0>	NO_TEST=TRUE 36
T57 PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<2..0>	NO_TEST=TRUE 36
T62 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<3>	NO_TEST=TRUE 36
T61 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<3>	NO_TEST=TRUE 36
T57	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_P<3..0>	NO_TEST=TRUE 18 36
T57	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_N<3..0>	NO_TEST=TRUE 18 36
T57	PCIE_PHY	PCIE	PCIE_TBT_D2R_P<3..0>	NO_TEST=TRUE 18 36
T57	PCIE_PHY	PCIE	PCIE_TBT_D2R_N<3..0>	NO_TEST=TRUE 18 36
T57 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<1..0>	NO_TEST=TRUE 36
T57 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<1..0>	NO_TEST=TRUE 36
T62 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<2>	NO_TEST=TRUE 36
T62 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<2>	NO_TEST=TRUE 36
T62 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<3>	NO_TEST=TRUE 36
T62 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<3>	NO_TEST=TRUE 36
T57 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	18 36
T58 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	18 36

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
T44 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<15>	NO_TEST=TRUE 10 75
T44 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<15>	NO_TEST=TRUE 10 75
T44	PCIE_PHY	PCIE	PEG_R2D_C_P<15>	NO_TEST=TRUE 75
T44	PCIE_PHY	PCIE	PEG_R2D_C_N<15>	NO_TEST=TRUE 75
T44 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<15>	NO_TEST=TRUE 75
T44 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<15>	NO_TEST=TRUE 75
T44	PCIE_PHY	PCIE	PEG_D2R_C_P<15>	NO_TEST=TRUE 10 75
T44	PCIE_PHY	PCIE	PEG_D2R_C_N<15>	NO_TEST=TRUE 10 75
T44 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<14>	NO_TEST=TRUE 10 75
T44 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<14>	NO_TEST=TRUE 10 75
T45	PCIE_PHY	PCIE	PEG_R2D_C_P<14>	NO_TEST=TRUE 75
T45	PCIE_PHY	PCIE	PEG_R2D_C_N<14>	NO_TEST=TRUE 75
T45 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<14>	NO_TEST=TRUE 75
T45 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<14>	NO_TEST=TRUE 75
T45	PCIE_PHY	PCIE	PEG_D2R_C_P<14>	NO_TEST=TRUE 10 75
T45	PCIE_PHY	PCIE	PEG_D2R_C_N<14>	NO_TEST=TRUE 10 75
T45 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<13>	NO_TEST=TRUE 10 75
T45 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<13>	NO_TEST=TRUE 10 75
T45	PCIE_PHY	PCIE	PEG_R2D_C_P<13>	NO_TEST=TRUE 75
T46	PCIE_PHY	PCIE	PEG_R2D_C_N<13>	NO_TEST=TRUE 75
T45 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<13>	NO_TEST=TRUE 75
T46 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<13>	NO_TEST=TRUE 75
T46	PCIE_PHY	PCIE	PEG_D2R_C_P<13>	NO_TEST=TRUE 10 75
T46	PCIE_PHY	PCIE	PEG_D2R_C_N<13>	NO_TEST=TRUE 10 75
T46 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<12>	NO_TEST=TRUE 10 75
T46 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<12>	NO_TEST=TRUE 10 75
T46	PCIE_PHY	PCIE	PEG_R2D_C_P<12>	NO_TEST=TRUE 75
T46	PCIE_PHY	PCIE	PEG_R2D_C_N<12>	NO_TEST=TRUE 75
T46 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<12>	NO_TEST=TRUE 75
T47 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<12>	NO_TEST=TRUE 75
T46	PCIE_PHY	PCIE	PEG_D2R_C_P<12>	NO_TEST=TRUE 10 75
T47	PCIE_PHY	PCIE	PEG_D2R_C_N<12>	NO_TEST=TRUE 10 75
T47 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<11>	NO_TEST=TRUE 10 75
T47 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<11>	NO_TEST=TRUE 10 75
T47	PCIE_PHY	PCIE	PEG_R2D_C_P<11>	NO_TEST=TRUE 75
T47	PCIE_PHY	PCIE	PEG_R2D_C_N<11>	NO_TEST=TRUE 75
T47 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<11>	NO_TEST=TRUE 75
T47 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<11>	NO_TEST=TRUE 75
T47	PCIE_PHY	PCIE	PEG_D2R_C_P<11>	NO_TEST=TRUE 10 75
T47	PCIE_PHY	PCIE	PEG_D2R_C_N<11>	NO_TEST=TRUE 10 75
T48 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<10>	NO_TEST=TRUE 10 75
T48 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<10>	NO_TEST=TRUE 10 75
T48	PCIE_PHY	PCIE	PEG_R2D_C_P<10>	NO_TEST=TRUE 75
T48	PCIE_PHY	PCIE	PEG_R2D_C_N<10>	NO_TEST=TRUE 75
T48 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<10>	NO_TEST=TRUE 75
T48 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<10>	NO_TEST=TRUE 75
T48	PCIE_PHY	PCIE	PEG_D2R_C_P<10>	NO_TEST=TRUE 10 75
T48	PCIE_PHY	PCIE	PEG_D2R_C_N<10>	NO_TEST=TRUE 10 75
T48 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<9>	NO_TEST=TRUE 10 75
T48 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<9>	NO_TEST=TRUE 10 75
T49	PCIE_PHY	PCIE	PEG_R2D_C_P<9>	NO_TEST=TRUE 75
T49	PCIE_PHY	PCIE	PEG_R2D_C_N<9>	NO_TEST=TRUE 75
T49 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<9>	NO_TEST=TRUE 75
T49 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<9>	NO_TEST=TRUE 75
T49	PCIE_PHY	PCIE	PEG_D2R_C_P<9>	NO_TEST=TRUE 10 75
T49	PCIE_PHY	PCIE	PEG_D2R_C_N<9>	NO_TEST=TRUE 10 75
T49 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<8>	NO_TEST=TRUE 10 75
T49 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<8>	NO_TEST=TRUE 10 75
T49	PCIE_PHY	PCIE	PEG_R2D_C_P<8>	NO_TEST=TRUE 75
T49	PCIE_PHY	PCIE	PEG_R2D_C_N<8>	NO_TEST=TRUE 75
T50 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<8>	NO_TEST=TRUE 75
T50 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<8>	NO_TEST=TRUE 75
T50	PCIE_PHY	PCIE	PEG_D2R_C_P<8>	NO_TEST=TRUE 10 75
T50	PCIE_PHY	PCIE	PEG_D2R_C_N<8>	NO_TEST=TRUE 10 75

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
T49 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<7>	NO_TEST=TRUE 10 75
T50 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<7>	NO_TEST=TRUE 10 75
T50	PCIE_PHY	PCIE	PEG_R2D_C_P<7>	NO_TEST=TRUE 75
T50	PCIE_PHY	PCIE	PEG_R2D_C_N<7>	NO_TEST=TRUE 75
T50 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<7>	NO_TEST=TRUE 75
T50 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<7>	NO_TEST=TRUE 75
T51	PCIE_PHY	PCIE	PEG_D2R_C_P<7>	NO_TEST=TRUE 10 75
T51	PCIE_PHY	PCIE	PEG_D2R_C_N<7>	NO_TEST=TRUE 10 75
T51 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<6>	NO_TEST=TRUE 10 75
T51 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<6>	NO_TEST=TRUE 10 75
T51	PCIE_PHY	PCIE	PEG_R2D_C_P<6>	NO_TEST=TRUE 75
T51	PCIE_PHY	PCIE	PEG_R2D_C_N<6>	NO_TEST=TRUE 75
T51 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<6>	NO_TEST=TRUE 75
T51 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<6>	NO_TEST=TRUE 75
T51	PCIE_PHY	PCIE	PEG_D2R_C_P<6>	NO_TEST=TRUE 10 75
T51	PCIE_PHY	PCIE	PEG_D2R_C_N<6>	NO_TEST=TRUE 10 75
T52 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<5>	NO_TEST=TRUE 10 75
T52 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<5>	NO_TEST=TRUE 10 75
T52	PCIE_PHY	PCIE	PEG_R2D_C_P<5>	NO_TEST=TRUE 75
T52	PCIE_PHY	PCIE	PEG_R2D_C_N<5>	NO_TEST=TRUE 75
T52 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<5>	NO_TEST=TRUE 75
T52 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<5>	NO_TEST=TRUE 75
T52	PCIE_PHY	PCIE	PEG_D2R_C_P<5>	NO_TEST=TRUE 10 75
T52	PCIE_PHY	PCIE	PEG_D2R_C_N<5>	NO_TEST=TRUE 10 75
T53 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<4>	NO_TEST=TRUE 10 75
T53 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<4>	NO_TEST=TRUE 10 75
T53	PCIE_PHY	PCIE	PEG_R2D_C_P<4>	NO_TEST=TRUE 75
T53	PCIE_PHY	PCIE	PEG_R2D_C_N<4>	NO_TEST=TRUE 75
T53 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<4>	NO_TEST=TRUE 75
T53 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<4>	NO_TEST=TRUE 75
T53	PCIE_PHY	PCIE	PEG_D2R_C_P<4>	NO_TEST=TRUE 10 75
T53	PCIE_PHY	PCIE	PEG_D2R_C_N<4>	NO_TEST=TRUE 10 75
T54 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<3>	NO_TEST=TRUE 10 75
T54 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<3>	NO_TEST=TRUE 10 75
T54	PCIE_PHY	PCIE	PEG_R2D_C_P<3>	NO_TEST=TRUE 75
T54	PCIE_PHY	PCIE	PEG_R2D_C_N<3>	NO_TEST=TRUE 75
T54 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<3>	NO_TEST=TRUE 75
T54 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<3>	NO_TEST=TRUE 75
T54	PCIE_PHY	PCIE	PEG_D2R_C_P<3>	NO_TEST=TRUE 10 75
T54	PCIE_PHY	PCIE	PEG_D2R_C_N<3>	NO_TEST=TRUE 10 75
T55 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<2>	NO_TEST=TRUE 10 75
T55 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<2>	NO_TEST=TRUE 10 75
T55	PCIE_PHY	PCIE	PEG_R2D_C_P<2>	NO_TEST=TRUE 75
T55	PCIE_PHY	PCIE	PEG_R2D_C_N<2>	NO_TEST=TRUE 75
T55 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<2>	NO_TEST=TRUE 75
T55 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<2>	NO_TEST=TRUE 75
T55	PCIE_PHY	PCIE	PEG_D2R_C_P<2>	NO_TEST=TRUE 10 75
T55	PCIE_PHY	PCIE	PEG_D2R_C_N<2>	NO_TEST=TRUE 10 75
T56 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<1>	NO_TEST=TRUE 10 75
T56 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<1>	NO_TEST=TRUE 10 75
T56	PCIE_PHY	PCIE	PEG_R2D_C_P<1>	NO_TEST=TRUE 75
T56	PCIE_PHY	PCIE	PEG_R2D_C_N<1>	NO_TEST=TRUE 75
T56 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<1>	NO_TEST=TRUE 75
T56 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<1>	NO_TEST=TRUE 75
T56	PCIE_PHY	PCIE	PEG_D2R_C_P<1>	NO_TEST=TRUE 10 75
T56	PCIE_PHY	PCIE	PEG_D2R_C_N<1>	NO_TEST=TRUE 10 75
T56 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<0>	NO_TEST=TRUE 10 75
T56 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<0>	NO_TEST=TRUE 10 75
T56	PCIE_PHY	PCIE	PEG_R2D_C_P<0>	NO_TEST=TRUE 75
T56	PCIE_PHY	PCIE	PEG_R2D_C_N<0>	NO_TEST=TRUE 75
T56 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<0>	NO_TEST=TRUE 75
T56 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<0>	NO_TEST=TRUE 75
T56	PCIE_PHY	PCIE	PEG_D2R_C_P<0>	NO_TEST=TRUE 10 75
T56	PCIE_PHY	PCIE	PEG_D2R_C_N<0>	NO_TEST=TRUE 10 75
CPU PCIe Clocks				
T58 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P	NO_TEST=TRUE 18 75
T58 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N	NO_TEST=TRUE 18 75
CPU PCIe Compensation				
T57	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_COMP	10

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DMI

DMI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DMI_PHY	*	DMI_85D

CPU Misc / FDI

CPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI_SE	*	Y	0.3 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_PHY	*	CPU_50S
COMP_FDI_PHY	*	COMP_FDI_SE

CPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

FDI Compensation Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU	*	*	CPU_ISO
COMP_FDI	*	*	COMP_FDI_ISO

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_50S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
XDP_CLK_ISO	*	=4:1_SPACING	?

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	50	-	15.75	Isolation is for JTAG clocks.
					All signals default are 50 Ohm SE.

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	XDP_CLK_ISO
OBS_STROBE	*	*	XDP_CLK_ISO

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
DMI_N2S	DMI_PHY	PCIE	DMI_N2S_P<3..0>	NO_TEST=TRUE
DMI_N2S	DMI_PHY	PCIE	DMI_N2S_N<3..0>	NO_TEST=TRUE
DMI_S2N	DMI_PHY	PCIE	DMI_S2N_P<3..0>	NO_TEST=TRUE
DMI_S2N	DMI_PHY	PCIE	DMI_S2N_N<3..0>	NO_TEST=TRUE
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	
DMI Compensation				
	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI_COMP	
	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI2RBIAS	

CPU Misc.

Electrical Contraint Set	Physical	Spacing		
CPU Misc.				
	CPU_PHY	CPU	CPU_SKTOCC_L	
	CPU_PHY	CPU	CPU_PROC_SEL	
	CPU_PHY	CPU	CPU_CATERR_L	
	CPU_PHY	CPU	CPU_PECI	
	CPU_PHY	CPU	CPU_PROCHOT_L	
	CPU_PHY	CPU	CPU_PROCHOT_R_L	
	CPU_PHY	CPU	CPU_THRMTRIP_L	
	CPU_PHY	CPU	CPU_RESET_L	
	CPU_PHY	CPU	PLT_RESET_LS1V05_L	
	CPU_PHY	CPU	PM_SYNC	
	CPU_PHY	CPU	CPU_PWRGD	
	CPU_PHY	CPU	PM_MEM_PWRGD	
	CPU_PHY	CPU	PM_MEM_PWRGD_R	
	CPU_PHY	CPU	CPU_MEM_RESET_L	

FDI

Electrical Contraint Set	Physical	Spacing		
FDI Compensation				
	COMP_FDI_PHY	COMP_FDI	CPU_FDI_COMPIO	

XDP

Electrical Contraint Set	Physical	Spacing		
XDP MISC.				
XDP_BPM_L	XDP_PHY	XDP	XDP_BPM_L<7..0>	
	XDP_PHY	XDP	CPU_CFG<17..16>	
	XDP_PHY	XDP	CPU_CFG<11..0>	
	XDP_PHY	XDP	XDP_DBRESET_L	
	XDP_PHY	XDP	XDP_CPU_PWRGD	
	XDP_PHY	XDP	XDP_CPU_PWRBTN_L	
	XDP_PHY	XDP	XDP_CPU_CFG<0>	
	XDP_PHY	XDP	XDP_VR_READY	
	XDP_PHY	XDP	XDP_CPU_PLTRST_L	
	XDP_PHY	XDP	XDP_PCH_PWRGD	
	XDP_PHY	XDP	XDP_PCH_PWRBTN_L	
	XDP_PHY	XDP	XDP_PCH_PLTRST_L	
	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	
	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	
ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	
ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	
	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	
	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	
CPU JTAG				
	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	
	XDP_PHY	XDP	XDP_CPU_TMS	
	XDP_PHY	XDP	XDP_CPU_TDI	
	XDP_PHY	XDP	XDP_CPU_TDO	
	XDP_PHY	XDP	XDP_CPU_TRST_L	
	XDP_PHY	XDP	XDP_CPU_PRDY_L	
	XDP_PHY	XDP	XDP_CPU_PREQ_L	
PCH JTAG				
	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	
	XDP_PHY	XDP	XDP_PCH_TMS	
	XDP_PHY	XDP	XDP_PCH_TDI	
	XDP_PHY	XDP	XDP_PCH_TDO	

Chipset Test Interface

Electrical Contraint Set	Physical	Spacing		
OBS PCH Side				
XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTA_OC_R_L	
XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_R_L	
XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTC_OC_R_L	
XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_R_L	
XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_EHCI_R_L	
XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_EHCI_R_L	
XDP_PCH_OBS	XDP_PHY	XDP	AP_PWR_EN_R	
XDP_PCH_OBS	XDP_PHY	XDP	SDCONN_STATE_CHANGE_R	
XDP_PCH_OBS	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT_R	
XDP_PCH_OBS	XDP_PHY	XDP	ISOLATE_CPU_MEM_R_L	
XDP_PCH_OBS	XDP_PHY	XDP	GPU_GOOD_R	
XDP_PCH_OBS	XDP_PHY	XDP	DP_AUXCH_ISOL_R	
XDP_PCH_OBS	XDP_PHY	XDP	SATARDRVR_EN_R	
XDP_PCH_OBS	XDP_PHY	XDP	DP_TBT_SEL_R	
XDP_PCH_OBS	XDP_PHY	XDP	JTAG_TBT_TCK_R	
XDP_PCH_OBS	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH_R	
XDP_PCH_OBS	XDP_PHY	XDP	ENET_LOW_PWR_PCH_R	
XDP_PCH_OBS_UNUSED	XDP_PHY	OBS_STROBE	XDP_PIN03	
OBS XDP Side				
	XDP_PHY	XDP	XDP_DA0_USB_EXTA_OC_L	
	XDP_PHY	XDP	XDP_DA1_USB_EXTB_OC_L	
	XDP_PHY	XDP	XDP_DA2_USB_EXTC_OC_L	
	XDP_PHY	XDP	XDP_DA3_USB_EXTD_OC_L	
	XDP_PHY	XDP	XDP_DB0_USB_EXTB_OC_EHCI_L	
	XDP_PHY	XDP	XDP_DB1_USB_EXTD_OC_EHCI_L	
	XDP_PHY	XDP	XDP_DB2_AP_PWR_EN	
	XDP_PHY	XDP	XDP_DB3_SDCONN_STATE_CHANGE	
	XDP_PHY	OBS_STROBE	XDP_FC1_TBT_CIO_PLUG_EVENT	
	XDP_PHY	XDP	XDP_DC0_ISOLATE_CPU_MEM_L	
	XDP_PHY	XDP	XDP_DC1_GPU_GOOD	
	XDP_PHY	XDP	XDP_DC2_DP_AUXCH_ISOL	
	XDP_PHY	XDP	XDP_DC3_SATARDRVR_EN	
	XDP_PHY	XDP	XDP_DD0_DP_TBT_SEL	
	XDP_PHY	XDP	XDP_DD1_JTAG_TBT_TCK	
	XDP_PHY	XDP	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH	
	XDP_PHY	XDP	XDP_DD3_ENET_LOW_PWR_PCH	
	XDP_PHY	OBS_STROBE	XDP_FC0_PCH_GPIO15	
Standard usage branch off from OBS				
	XDP_PHY	XDP	USB_EXTA_OC_L	
	XDP_PHY	XDP	USB_EXTB_OC_L	
	XDP_PHY	XDP	USB_EXTC_OC_L	
	XDP_PHY	XDP	USB_EXTD_OC_L	
	XDP_PHY	XDP	USB_EXTB_OC_EHCI_L	
	XDP_PHY	XDP	USB_EXTD_OC_EHCI_L	
	XDP_PHY	XDP	AP_PWR_EN	
	XDP_PHY	XDP	SDCONN_STATE_CHANGE	
	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT	
	XDP_PHY	XDP	ISOLATE_CPU_MEM_L	
	XDP_PHY	XDP	GPU_GOOD	
	XDP_PHY	XDP	DP_AUXCH_ISOL	
	XDP_PHY	XDP	SATARDRVR_EN	
	XDP_PHY	XDP	DP_TBT_SEL	
	XDP_PHY	XDP	JTAG_TBT_TCK	
	XDP_PHY	XDP	JTAG_TBT_TCK_ISOL	
	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH	
	XDP_PHY	XDP	ENET_LOW_PWR_PCH	
	XDP_PHY	XDP	DP_AUXCH_ISOL_EN	

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PAGE TITLE: CPU MISC/DMI/FDI/XDP Constraints

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_90D
COMP_SATA_PHY	*	SATA_50S

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=7.2X_DIELECTRIC	?
COMP_SATA_ISO	*	=5.4X_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
B90 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_P	44
B92 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_N	44
B88	SATA_PHY	SATA	SATA_HDD_R2D_C_P	10 44
B89	SATA_PHY	SATA	SATA_HDD_R2D_C_N	10 44
B94 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_P	10 44
B95 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_N	10 44
B91	SATA_PHY	SATA	SATA_HDD_D2R_C_P	44
B93	SATA_PHY	SATA	SATA_HDD_D2R_C_N	44
PCH SATA Port 1 (SSD)				
B97 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_P	10 44
B99 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_N	10 44
B100 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_P	10 44
B102 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_N	10 44
PCH SATA Compensation				
B104	COMP_SATA_PHY	COMP_SATA	PCH_SATA1COMP	10
B106	COMP_SATA_PHY	COMP_SATA	PCH_SATA3COMP	10
B105	COMP_SATA_PHY	COMP_SATA	PCH_SATA3RBIAS	10

Unused

Electrical Contraint Set	Physical	Spacing

PAGE TITLE
SATA/FDI/XDP Constraints

Apple Inc.

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH_ISO	*	=6.5X_DIELECTRIC	?
COMP_PCH_ISO	*	=2:1_SPACING	?
PCH_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCH	*	*	CLK_PCH_ISO
COMP_PCH	*	*	COMP_PCH_ISO
PCH	*	*	PCH_ISO

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCI	*	*	CLK_PCI_ISO

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC_ISO	*	=1.5:1_SPACING	?
CLK_LPC_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LPC	*	*	LPC_ISO
CLK_LPC	*	*	CLK_LPC_ISO

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	HDA_ISO

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL_ISO	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XTAL	*	*	XTAL_ISO

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
E33	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIIN	18 26
E32	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIOUT	20 26

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
E32	LPC_50S	LPC	LPC_AD<3..0>	18 47 49
E33	LPC_50S	LPC	LPC_R_AD<3..0>	18
E33	LPC_50S	LPC	LPC_FRAME_L	18 47 49
E33	LPC_50S	LPC	LFRAME_L	18
LPC Clocks				
E33	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 49
E34	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 26
E33	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	26 47
E32	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	20 26

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
E18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_SB	26
E40	CLK_PCH_50S	CLK_PCH	PCH_CLK25M_XTALIN	18 26
PCH Ref Clock Comp				
E40	PCH_50S	COMP_PCH	PCH_XCLK_RCOMP	18
PCH RTC 32K				
E48	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 26
E48	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 26
E52	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	26
SMC 32K				
E26	CLK_PCH_50S	CLK_PCH	PM_CLK32K_SUSCLK_R	19 48
E50	CLK_PCH_50S	CLK_PCH	SMC_CLK32K	47 48

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
E52	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	26
E50	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	26
E51	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	26
25M Reference Clocks				
E18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET	26 39
E18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET_R	26
E18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT	26 36
E18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT_R	36

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
E35	HDA_50S	HDA	HDA_BIT_CLK	18 56
E36	HDA_50S	HDA	HDA_BIT_CLK_R	18
E36	HDA_50S	HDA	HDA_RST_L	18 56
E36	HDA_50S	HDA	HDA_RST_R_L	18
E36	HDA_50S	HDA	HDA_SDOUT	18 56
E36	HDA_50S	HDA	HDA_SDOUT_R	15 18
E36	HDA_50S	HDA	HDA_SYNC	15 18 56
E36	HDA_50S	HDA	HDA_SYNC_R	18
E36	HDA_50S	HDA	HDA_SDIN0	18 56
E36	HDA_50S	HDA	AUD_SDI_R	56
E41	HDA_50S	HDA	SPI_DESCRIPTOR_OVERRIDE_R	15
SPDIF				
E37		HDA	AUD_SPDIF_CHIP	56
E37		HDA	AUD_SPDIF_OUT	56 60

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
E31	SPI_50S	SPI	SPI_CLK_R	18 49
E42	SPI_50S	SPI	SPI_CLK	49
E39	SPI_50S	SPI	SPI_ALT_CLK	49
E40	SPI_50S	SPI	SPI_SMC_CLK	47 48
E49	SPI_50S	SPI	SPI_MLB_CLK	48 49
E34	SPI_50S	SPI	SPI_CS0_R_L	18 49
E33	SPI_50S	SPI	SPI_CS0_L	49
E38	SPI_50S	SPI	SPI_ALT_CS_L	49
E40	SPI_50S	SPI	SPI_SMC_CS_L	47 48
E37	SPI_50S	SPI	SPI_MLB_CS_L	48 49
E39	SPI_50S	SPI	SPI_MOSI_R	18 49
E40	SPI_50S	SPI	SPI_MOSI	49
E40	SPI_50S	SPI	SPI_ALT_MOSI	49
E40	SPI_50S	SPI	SPI_SMC_MOSI	47 48
E41	SPI_50S	SPI	SPI_MLB_MOSI	48 49
E40	SPI_50S	SPI	SPI_MISO	18 49
E40	SPI_50S	SPI	SPI_ALT_MISO	49
E41	SPI_50S	SPI	SPI_SMC_MISO	47 48
E41	SPI_50S	SPI	SPI_MLB_MISO	48 49
E40	SPI_50S	SPI	SPIROM_USE_MLB	21 49

SYNC_MASTER=D8_MARK SYNC_DATE=02/10/2012

PAGE TITLE

PCH and BR Constraints

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D
USB_HUB_PHY	*	USB_50S

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Comments
12.2.1	90	90	12/2.8 mils = 4.29:1	USB 2.0
13.3.1	85	85	20/2.8 mils = 7.14:1	USB 3.0
			50/2.8 mils = 17.9:1	USB 2.0/3.0

SMSC Hub Application Note 15.17
Single-ended impedance range from 45-80 ohm is acceptable

USB 2.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=4.4X_DIELECTRIC	?
USB2_ISO	TOP,BOTTOM	=4.4X_DIELECTRIC	?
USB2_CLK_ISO	*	=18X_DIELECTRIC	?
USB2_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB_HUB_ISO	*	=2:1_SPACING	?

USB 3.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_CLK_ISO	*	=18X_DIELECTRIC	?
USB3_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB3_USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	ISL10	=5X_DIELECTRIC	?

USB 2.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB2	*CLK*	*	USB2_CLK_ISO
USB2	DISPLAYPORT	*	USB2_CLK_ISO
USB2	*TBT*	*	USB2_CLK_ISO
USB2	*ENET*	*	USB2_CLK_ISO
USB2	*SD*	*	USB2_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB_HUB	*	*	USB_HUB_ISO

USB 3.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3	*	*	USB3_ISO
USB3	*CLK*	*	USB3_CLK_ISO
USB3	DISPLAYPORT	*	USB3_CLK_ISO
USB3	*TBT*	*	USB3_CLK_ISO
USB3	*ENET*	*	USB3_CLK_ISO
USB3	*SD*	*	USB3_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB3	USB3	*	USB3_USB3_ISO

CAMERA CONTROLLER

Camera Controller's SMIA Interface & MISC. Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CAM_SE	*	Y	0.2 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D
CAM_PHY	*	CAM_SE

Camera Controller's SMIA Interface & MISC. Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?
CAM_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF
CAM	*	*	CAM_ISO

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
B39 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	45
B38 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	45
B37	USB3_PHY	USB3	USB3_EXTA_RX_F_P	20 45
B36	USB3_PHY	USB3	USB3_EXTA_RX_F_N	20 45
B34 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	20 45
B33 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	20 45
B32	USB3_PHY	USB3	USB3_EXTA_TX_F_P	45
B31	USB3_PHY	USB3	USB3_EXTA_TX_F_N	45
B30	USB3_PHY	USB3	USB3_EXTA_TX_C_P	45
B29	USB3_PHY	USB3	USB3_EXTA_TX_C_N	45
B27 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_P	20 45
B26 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_N	20 45
B25	USB2_PHY	USB2	USB2_EXTA_MUXED_P	45
B24	USB2_PHY	USB2	USB2_EXTA_MUXED_N	45
B23	USB2_PHY	USB2	USB2_EXTA_MUXED_F_P	45
B22	USB2_PHY	USB2	USB2_EXTA_MUXED_F_N	45
External Port B (J4610)				
F47 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	45
F49 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	45
F50	USB3_PHY	USB3	USB3_EXTB_RX_F_P	20 45
F52	USB3_PHY	USB3	USB3_EXTB_RX_F_N	20 45
F53 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	20 45
F54 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	20 45
F56	USB3_PHY	USB3	USB3_EXTB_TX_F_P	45
F57	USB3_PHY	USB3	USB3_EXTB_TX_F_N	45
F58	USB3_PHY	USB3	USB3_EXTB_TX_C_P	45
F59	USB3_PHY	USB3	USB3_EXTB_TX_C_N	45
F60 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_P	20 45
F61 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_N	20 45
F62	USB2_PHY	USB2	USB_PCH_9_P	20 45
F63	USB2_PHY	USB2	USB_PCH_9_N	20 45
F65	USB2_PHY	USB2	USB2_EXTB_MUXED_P	45
F66	USB2_PHY	USB2	USB2_EXTB_MUXED_N	45
F67	USB2_PHY	USB2	USB2_EXTB_MUXED_F_P	45
F68	USB2_PHY	USB2	USB2_EXTB_MUXED_F_N	45
External Port C (J4700)				
E37 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	46
E38 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	46
E39	USB3_PHY	USB3	USB3_EXTC_RX_F_P	20 46
E40	USB3_PHY	USB3	USB3_EXTC_RX_F_N	20 46
E41 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	20 46
E42 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	20 46
E44	USB3_PHY	USB3	USB3_EXTC_TX_F_P	46
E45	USB3_PHY	USB3	USB3_EXTC_TX_F_N	46
E46	USB3_PHY	USB3	USB3_EXTC_TX_C_P	46
E47	USB3_PHY	USB3	USB3_EXTC_TX_C_N	46
E48 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_P	20 46
E49 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_N	20 46
E50	USB2_PHY	USB2	USB2_EXTC_F_P	46
E52	USB2_PHY	USB2	USB2_EXTC_F_N	46
External Port D (J4710)				
E53 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	46
E55 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	46
E56	USB3_PHY	USB3	USB3_EXTD_RX_F_P	20 46
E58	USB3_PHY	USB3	USB3_EXTD_RX_F_N	20 46
E59 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	20 46
E60 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	20 46
E62	USB3_PHY	USB3	USB3_EXTD_TX_F_P	46
E63	USB3_PHY	USB3	USB3_EXTD_TX_F_N	46
E64	USB3_PHY	USB3	USB3_EXTD_TX_C_P	46
E65	USB3_PHY	USB3	USB3_EXTD_TX_C_N	46
E66 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_P	20 46
E67 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_N	20 46
E68	USB2_PHY	USB2	USB_PCH_10_P	20 46
E69	USB2_PHY	USB2	USB_PCH_10_N	20 46
E70	USB2_PHY	USB2	USB2_EXTD_MUXED_P	46
E71	USB2_PHY	USB2	USB2_EXTD_MUXED_N	46
E72	USB2_PHY	USB2	USB2_EXTD_MUXED_F_P	46
E73	USB2_PHY	USB2	USB2_EXTD_MUXED_F_N	46
Camera (U4200)				
B20 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	42
B19 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N	42
PCH USB Compensation				
B18	PCH_50S	COMP_PCH	PCH_USB_RBIAS	20

Electrical Contraint Set	Physical	Spacing	Voltage	
Camera Controller Local Ground				
B21	GND_PHY	GND	0V	CAM_AGND 42
B20	GND_PHY	GND	0V	CAM_PLLGND 42

USB Hub

Electrical Contraint Set	Physical	Spacing		
USB 2.0 Hub				
E40 USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_P	20 27
E39 USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_N	20 27
E40 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_P	27 35
E41 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_N	27 35
E50 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_P	35
E50 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_N	35
E43	USB_HUB_PHY	USB_HUB	USB_HUB_2P	27
E42	USB_HUB_PHY	USB_HUB	USB_HUB_2N	27
USB 2.0 Hub Misc.				
E51	USB_HUB_PHY	USB_HUB	USB_HUB_RESET_L	27
E52	USB_HUB_PHY	USB_HUB	USB_HUB_VBUS_DET	27
E53	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM0	27
E54	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM1	27
E47	USB_HUB_PHY	USB_HUB	USB_HUB_HS_IND	27
USB 2.0 Hub Compensation				
E47	PCH_50S	COMP_PCH	USB_HUB_RBIAS	27
USB 2.0 Hub Crystal				
E49	CLK_XTAL	XTAL	USB_HUB_XTAL1	27
E48	CLK_XTAL	XTAL	USB_HUB_XTAL2	27
E45	CLK_XTAL	XTAL	USB_HUB_XTAL2_R	27

Camera Controller

Electrical Contraint Set	Physical	Spacing		
SMIA				
E40 SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	42
E42 SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	42
E52 SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	42
E52 SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	42
MISC				
E50	SPI_50S	SPI	CAM_SF_CLK	42
E50	SPI_50S	SPI	CAM_SF_CLK_R	42
E60	SPI_50S	SPI	CAM_SF_DIN	42
E50	SPI_50S	SPI	CAM_SF_DIN_R	42
E51	SPI_50S	SPI	CAM_SF_CS_L	42
E51	SPI_50S	SPI	CAM_SF_WP_L	42
E52	SPI_50S	SPI	CAM_SF_DOUT	42
E53	SPI_50S	SPI	CAM_SF_DOUT_R	42
E49	SPI_50S	SPI	CAM_SF_HOLD_L	42
B24	CAM_PHY	CAM	CAM_USB_VRES	42
B23	CAM_PHY	CAM	MIPI_RESISTOR	42
B30		PM	CAM_EXT_BOOT_L	43
B31		PM	PCH_CAM_EXT_BOOT_R_L	21 43
B37		PM	CAM_P1V2_RST_HOLDOFF	43
B36		PM	CAM_P1V2_RST_HOLDOFF_L	43
I2C				
B34	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	42
B35	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	42
B32	SMB_PHY	SMB	SMB_ALS_F_SDA	42
B33	SMB_PHY	SMB	SMB_ALS_F_SCL	42
Camera Controller Crystal				
B25	CLK_XTAL	XTAL	CAM_XTAL_IN	42
B26	CLK_XTAL	XTAL	CAM_XTAL_OUT	42
B27	CLK_XTAL	XTAL	CAM_XTAL_OUT_R	42

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
SNS_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR
SNS_PHY	*	SNS_50S

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_CTL_PHY	*	POWER_P5MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S
POWER_PHY	*	POWER_P6MM
GND_PHY	*	GND_P5MM

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?
SWNODE_LG2SW	*	=3:1_SPACING	?

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND
VR_LGATE	*	*	SWNODE_ISO
VR_LGATE	VR_SWITCH	*	SWNODE_LG2SW

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

CPU VccSA

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I24	POWER_PHY	POWER	5V			REG_VCC_U7500	70
I25	POWER_PHY	POWER	5V			REG_PVCC_U7500	70
Local Ground							
I26	GND_PHY	GND	0V			AGND_VCCSAS0	70
VCCIO							
I27	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VCCSAS0	70
I28	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VCCSAS0	70
I29	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VCCSAS0_RC	70
I31	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VCCSAS0	70
I30	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VCCSAS0	70
I33	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_VCCSAS0	70
I32	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_OCSET	70
I35	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_VO	70
I34		SENSE				SNS_CPU_VCCSA	13 70
I37	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE			SNS_VCCSAS0_XW_P	70
I36	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE			SNS_VCCSAS0_XW_N	70
I38		SENSE				REG_VCCSAS0_FB	70
I39		SENSE				REG_VCCSAS0_RTN	70
I40	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_SREF	70
I41	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_FSEL	70
Output Bus							
I42	POWER_PHY	POWER	0.925V			PPVCCSA_S0	6

CPU VccIO PCH 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I1	POWER_PHY	POWER	5V			REG_VCC_U7400	69
I2	POWER_PHY	POWER	5V			REG_PVCC_U7400	69
Local Ground							
I3	GND_PHY	GND	0V			AGND_CPU_P1V05S0	69
1.05V S0							
I5	POWER_PHY	VR_SWITCH	12V	TRUE		REG_CPU_PHASE_P1V05S0	69
I7	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_BOOT_P1V05S0	69
I6	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_BOOT_P1V05S0_RC	69
I8	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0	69
I9	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0_R	
I10	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_CPU_LGATE_P1V05S0	69
I12	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_SNUBBER_P1V05S0	69
I11	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_OCSET	69
I14	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_VO	69
I13	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE			SNS_CPU_VCCIO_P	13 69
I15	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE			SNS_CPU_VCCIO_N	13 69
I16		SNS_DIFF_PHY	SENSE			SNS_CPU_P1V05S0_XW_P	69
I17		SNS_DIFF_PHY	SENSE			SNS_CPU_P1V05S0_XW_N	69
I19			SENSE			REG_CPU_P1V05S0_FB	69
I18			SENSE			REG_CPU_P1V05S0_RTN	69
I21	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_SREF	69
I20	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_FSEL	69
Output Bus							
I22	POWER_PHY	POWER	1.05V			PP1V05_S0_CPU	6

PCH/GPU/TBT 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I44	POWER_PHY	POWER	5V			REG_VCC_UB700	95
Local Ground							
I46	GND_PHY	GND	0V			P1V05_AGND	95
1.05V S0							
I47	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	95
I48	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	95
I49	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	95
I50	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	95
I51	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	95
I52	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	95
I53	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P1V05S0	95
I54	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_P1V05S0	95
I55	VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	95
I56	VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	95
I57	POWER_PHY	VR_SWITCH	12V			REG_P1V05S0_VO_R	95
I58	POWER_PHY	VR_SWITCH	12V			P1V05_OCSET_R	95
I61		SENSE				REG_P1V05S0_FB	95
I62		SENSE				REG_P1V05S0_RTN	95
I63	VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	95
I64	VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	95
Output Bus							
I65	POWER_PHY	POWER	1.05V			PP1V05_S0_PCH	6
I66	POWER_PHY	POWER	1.05V			PP1V05_S0	6
FET Switched							
I67	POWER_PHY	POWER	1.05V			PP1V05_TBTLC	6 38
I68	POWER_PHY	POWER	1.05V			PP1V05_TBTCIO	6

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CPU Core Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H10	POWER_PHY	POWER	12V			PP12V_S0_CPUCORE_FLT	66 67 68
H11	POWER_PHY	POWER	5V			REG_VCC_U7100	66
Local Ground							
H12	GND_PHY	GND	0V			AGND_CPU	66 67 68
Phase 1							
H13	POWER_PHY	POWER	12V			REG_LVCC_U7210	67
H14	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1	66 67
H15	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1_R	66
H16	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_1	67
H17	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_1	67
H18	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_1_RC	67
H19	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_1	67
H20	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_1	67
H21	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_1	67
H22	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_1	67
H23 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_P	66 67
H24 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_N	67
H25		SENSE				REG_ISENCORE_1_NR	66 67
Phase 2							
H26	POWER_PHY	POWER	12V			REG_LVCC_U7230	67
H27	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2	66 67
H28	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2_R	66
H29	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_2	67
H30	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_2	67
H31	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_2_RC	67
H32	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_2	67
H33	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_2	67
H34	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_2	67
H35	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_2	67
H36 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_P	66 67
H37 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_N	67
H38		SENSE				REG_ISENCORE_2_NR	66 67
Phase 3							
H39	POWER_PHY	POWER	12V			REG_LVCC_U7250	67
H40	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3	66 67
H41	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3_R	66
H42	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_3	67
H43	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_3	67
H44	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_3_RC	67
H45	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_3	67
H46	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_3	67
H47	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_3	67
H48	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_3	67
H49 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_P	66 67
H50 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_N	67
H51		SENSE				REG_ISENCORE_3_NR	66 67
Phase 4							
H52	POWER_PHY	POWER	12V			REG_LVCC_U7310	68
H53	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4	66 68
H54	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4_R	66
H55	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_4	68
H56	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_4	68
H57	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_4_RC	68
H58	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_4	68
H59	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_4	68
H60	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_4	68
H61	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_4	68
H62 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_4_P	66 68
H63 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_4_N	68
H64		SENSE				REG_ISENCORE_4_NR	66 68
H65 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_XW_P	66
H66 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_XW_N	66
H67 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_R_P	66
H68 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_R_N	66
H69 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_P	13 66
H70 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_N	13 66
H71 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_P	13 66
H72 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_N	13 66
H73 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_P1V05_IOVDD_XW_P	95
H74 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_P1V05_IOVDD_XW_N	95

CPU AXG Phase and Core Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
AXG							
H75	POWER_PHY	POWER	12V			REG_LVCC_U7330	68
H76	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG	66 68
H77	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG_R	66
H78	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUAXG	68
H79	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUAXG	68
H80	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUAXG_RC	68
H81	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUAXG	68
H82	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUAXG	68
H83	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUAXG	68
H84	POWER_PHY	POWER	1.1V			PPCPUAXG_S0_SENSE	68
H85 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_P	68
H86 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_N	68
H87		SENSE				REG_ISENAXG_PR	66 68
H88		SENSE				REG_ISENAXG_NR	66 68
H89 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_R_P	66
H90 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_R_N	66
H91 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_XW_P	66
H92 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_XW_N	66
ISL6364							
H93	VR_CTL_PHY	VR_CTL				REG_CPUCORE_COMP	66
H94	VR_CTL_PHY	VR_CTL				CPUCORE_COMP_RC	66
H95	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FB	66
H96	VR_CTL_PHY	VR_CTL				CPUCORE_FB_RC	66
H97	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_1	66
H98	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_2	66
H99	VR_CTL_PHY	VR_CTL				CPUCORE_PSICOMP_RC	66
H100	VR_CTL_PHY	VR_CTL				REG_CPUCORE_PSICOMP	66
H101	VR_CTL_PHY	VR_CTL				REG_CPUCORE_HFCOMP	66
H102		SENSE				REG_CPUCORE_VSEN	66
H103		SENSE				REG_CPUCORE_RGND	66
H104	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IMON	51 66
H105	VR_CTL_PHY	VR_CTL				CPUCORE_IMON_R	66
H106	VR_CTL_PHY	VR_CTL				REG_CPUCORE_TM	66
H107	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SUTH	66
H108	VR_CTL_PHY	VR_CTL				REG_CPUCORE_NPSI	66
H109	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FDVID	66
H110	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IAUTO	66
H111	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SW_FREQ	66
H112	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RAMPADJ	66
H113	VR_CTL_PHY	VR_CTL				REG_CPUCORE_EN_PWR	66
H114	VR_CTL_PHY	VR_CTL				CPUCORE_EN_PWR_R	66
H115	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RSET	66
H116	VR_CTL_PHY	VR_CTL				REG_CPUAXG_COMP	66
H117	VR_CTL_PHY	VR_CTL				CPUAXG_COMP_RC	66
H118	VR_CTL_PHY	VR_CTL				REG_CPUAXG_FB	66
H119	VR_CTL_PHY	VR_CTL				CPUAXG_FB_RC	66
H120	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_1	66
H121	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_2	66
H122	VR_CTL_PHY	VR_CTL				REG_CPUAXG_HFCOMP	66
H123		SENSE				REG_CPUAXG_VSEN	66
H124		SENSE				REG_CPUAXG_RGND	66
H125	VR_CTL_PHY	VR_CTL				REG_CPUAXG_IMON	51 66
H126	VR_CTL_PHY	VR_CTL				CPUAXG_IMON_R	66
H127	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TM	66
H128	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TCOMP	66
H129	VR_CTL_PHY	VR_CTL				REG_CPUAXG_SW_FREQ	66
H130	VR_VID_PHY	VR_VID				CPU_VIDSCLK	13 66
H131	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	13
H132	VR_VID_PHY	VR_VID				CPU_VIDALERT_L	13 66
H133	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	13
H134	VR_VID_PHY	VR_VID				CPU_VIDSOUT	13 66
H135	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	13
Output Bus							
H136	POWER_PHY	POWER	1.1V			PPVCORE_S0_CPU	6
H137	POWER_PHY	POWER	1.1V			PPVAXG_S0	6

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3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
B152	POWER_PHY	POWER	12V			REG_VIN_U7600 — 71
B153	POWER_PHY	POWER	5V			REG_VCC1_U7600 — 71
B154	POWER_PHY	POWER	5V			REG_VCC2_U7600 — 71
3.3V S5						
B155	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5 — 71
B156	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5 — 73
B157	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC — 71
B158	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5 — 71
B159	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P3V3S5 — 71
B15A	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5 — 71
B15B	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN — 71
B15C	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET — 71
B15D	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET — 71
B15E	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT — 71
B15F	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R — 71
B160	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB — 71
5V S3						
B161	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4 — 71
B162	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4 — 71
B163	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC — 71
B164	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4 — 71
B165	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P5VS4 — 71
B166	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4 — 71
B167	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN — 71
B168	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET — 71
B169	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET — 71
B16A	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT — 71
B16B	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R — 71
B16C	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB — 71
Output Bus						
B16D	POWER_PHY	POWER	5V			PP5V_S5 — 6
B16E	POWER_PHY	POWER	5V			PP5V_S4 — 6
B16F	POWER_PHY	POWER	3.3V			PP3V3_S5 — 6
FET Switched						
B170	POWER_PHY	POWER	5V			PP5V_S0 — 6
B171	POWER_PHY	POWER	3.3V			PP3V3_S4 — 6
B172	POWER_PHY	POWER	3.3V			PP3V3_S0 — 6
B173	POWER_PHY	POWER	3.3V			PP3V3_S4_ENET — 6
B174	POWER_PHY	POWER	3.3V			PP3V3_TBTLC — 6
B175	POWER_PHY	POWER	3.3V			PP3V3_S4_AP — 6
B176	POWER_PHY	POWER	3.3V			PP3V3_S0_SSD — 6

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
B177	POWER_PHY	POWER	5V			REG_V5IN_U7700 — 72
Local Ground						
B178	GND_PHY	GND	0V			AGND_VDDQS3 — 72
VDDQ S3						
B179	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3 — 72
B17A	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L — 72
B17B	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3 — 72
B17C	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC — 72
B17D	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3 — 72
B17E	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R — 72
B17F	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VDDQS3 — 72
B180	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3 — 72
B181	POWER_PHY	POWER	1.5V			PPVDDQ_S3_SENSE
B182	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS — 72
B183	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF — 72
B184	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN — 72
B185	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE — 72
B186	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP — 72
B187	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS — 72
Output Bus						
B188	POWER_PHY	POWER	1.5V			PPVDDQ_S3 — 6
B189	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S0 — 6
FET Switched						
B18A	POWER_PHY	POWER	1.5V			PP1V5_S0 — 6
Sensed						
B18B	POWER_PHY	POWER	1.5V			PPVDDQ_S3_DDR — 6
B18C	POWER_PHY	POWER	1.5V			PP1V5_S0_CPU_MEM — 6
B18D	POWER_PHY	POWER	1.5V			PPFBVDDQ_S0_GPU — 6

DDR3 Vref

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Memory Vref						
B132	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_DAC — 34
B133	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_CTRL — 34
B134	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_A_S3 — 6
B135	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_B_S3 — 6
B142	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_A — 11 34
B143	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_B — 11 34
B135	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_A_S3 — 6
B136	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_B_S3 — 6
B13D	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DDR_VREF — 11
B140	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S3 — 6

1.8V S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
1.8V S0						
B115	POWER_PHY	VR_SWITCH	5V	TRUE		REG_PHASE_P1V8S0 — 72
B116	VR_CTL_PHY	VR_CTL				REG_P1V8S0_VFB — 72
B116	VR_CTL_PHY	VR_CTL				REG_P1V8S0_SYNCH — 72
Output Bus						
B118	POWER_PHY	POWER	1.8V			PP1V8_S0 — 6

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
HDD S0						
B139	POWER_PHY	POWER	5V			PP5V_S0_HDD — 6

12V S5

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
B13A	POWER_PHY	POWER	12V			PP12V_ACDC — 6
FET Switched						
B13B	POWER_PHY	POWER	12V			PP12V_S0 — 6
Sensed						
B13F	POWER_PHY	POWER	12V			PP12V_S5 — 6
B13G	POWER_PHY	POWER	12V			PP12V_G3H — 6
B141	POWER_PHY	POWER	12V			PP12V_G3H_P3V42 — 73
B14D	POWER_PHY	POWER	12V			PP12V_S0_FBVDDQ — 6
B14D	POWER_PHY	POWER	12V			PP12V_S0_CPU_P1V05 — 6
B14D	POWER_PHY	POWER	12V			PP12V_S0_VCCSA — 6
B14D	POWER_PHY	POWER	12V			PP12V_S0_P1V05 — 6
B13B	POWER_PHY	POWER	12V			PP12V_S0_HDD — 6
B14D	POWER_PHY	POWER	12V			PP12V_S0_BLC — 6

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Common						
B137	GND_PHY	GND	0V			GND

3V42 S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
3V42 S0						
B131	POWER_PHY	VR_SWITCH	5V	TRUE		P3V42G3H_SW — 73
B131	VR_CTL_PHY	VR_CTL				P3V42G3H_FB — 73
B131	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L — 73
B132	POWER_PHY	POWER	3.3V			PP3V3_G3 — 6
B132	POWER_PHY	POWER	3.3V			PP3V42_G3H — 6

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	0.075MM
TBT_GEN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C_ISO	*	=2x_DIELECTRIC	?
TBT_SPI_ISO	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
TBT_GEN_ISO	*	=2X_DIELECTRIC	?
BGA_TBT_AREA	*	0.075MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_TBT	BGA_TBT_AREA
TBT_I2C	*	*	TBT_I2C_ISO
TBT_SPI	*	*	TBT_SPI_ISO
TBTDP	*	*	TBTDP_ISO
TBT_GEN	*	*	TBT_GEN_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	*	=6.7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_ISO

MAX LENGTH OF DISPLAYPORT TRACES: 6 INCHES

DISPLAYPORT INTRA-PAIR MATCHING SHOULD BE 1 PS. INTER-PAIR MATCHING SHOULD BE WITHIN 150 PS.
DISPLAYPORT AUX CHANNEL INTRA-PAIR MATCHING SHOULD BE 5 PS.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	NO_TEST=TRUE 36 81
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	NO_TEST=TRUE 36 81
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	NO_TEST=TRUE 36
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	NO_TEST=TRUE 36
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	36 75
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	36 75
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	36
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	36
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	NO_TEST=TRUE 36 81
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	NO_TEST=TRUE 36 81
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	NO_TEST=TRUE 36
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	NO_TEST=TRUE 36
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	36 75
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	36 75
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	36
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	36
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	NO_TEST=TRUE 84
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	NO_TEST=TRUE 84
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	NO_TEST=TRUE 84
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	NO_TEST=TRUE 84
DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	84
DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	84
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	84
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	84
	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SCL	36 50
	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SDA	36 50
TBT_SPI_CLK	TBT_I2C_55S	TBT_SPI	TBT_SPI_CLK	36
TBT_SPI_MOSI	TBT_I2C_55S	TBT_SPI	TBT_SPI_MOSI	36
TBT_SPI_MISO	TBT_I2C_55S	TBT_SPI	TBT_SPI_MISO	36
TBT_SPI_CS_L	TBT_I2C_55S	TBT_SPI	TBT_SPI_CS_L	36
	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG1_BUF	36 86
	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG2_RC	36 86
	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG1_BUF	36 88
	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG2_RC	36 88
	TBT_GEN_55S	TBT_GEN	TBT_A_LSTX	36 86
	TBT_GEN_55S	TBT_GEN	TBT_A_LSRX	36 86
	TBT_GEN_55S	TBT_GEN	TBT_B_LSTX	36 88
	TBT_GEN_55S	TBT_GEN	TBT_B_LSRX	36 88
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_HPD	36 82
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_HPD	36 82
	TBT_GEN_55S	TBT_GEN	DP_TBTSRC_HPD	36 84
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_CLK	81 85
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_DATA	81 85
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_CLK	81 85
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_DATA	81 85
	TBT_GEN_55S	TBT_GEN	VIDEO_ON	74 87
	TBT_GEN_55S	TBT_GEN	VIDEO_ON_L	5 87
	TBT_GEN_55S	TBT_GEN	BDV_BKL_PWM	48 84
	TBT_GEN_55S	TBT_GEN	GPU_LCD_BKLT_PWM	82 84
	TBT_GEN_55S	TBT_GEN	LCD_BL_PWM	84
	TBT_GEN_55S	TBT_GEN	LCD_BL_FILT	84
	TBT_GEN_55S	TBT_GEN	LCD_BKLT_PWM	84 89

*: Only used on hosts supporting T29 video-in

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	NO_TEST=TRUE 36 86
TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	NO_TEST=TRUE 36 86
TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	NO_TEST=TRUE 36 86
TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	NO_TEST=TRUE 36 86
	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	NO_TEST=TRUE 86
	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	NO_TEST=TRUE 86
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	NO_TEST=TRUE 36 86
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	NO_TEST=TRUE 36 86
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	NO_TEST=TRUE 36 86
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	NO_TEST=TRUE 36 86
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	NO_TEST=TRUE 86
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	NO_TEST=TRUE 86
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	NO_TEST=TRUE 86
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	NO_TEST=TRUE 86
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	86
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	86
	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	NO_TEST=TRUE 86
	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	NO_TEST=TRUE 86
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	NO_TEST=TRUE 36 86
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	NO_TEST=TRUE 36 86
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	NO_TEST=TRUE 36 86
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	NO_TEST=TRUE 36 86
DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	36 86
DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	36 86
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	86
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	86
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	86
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	86
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	NO_TEST=TRUE 86
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	NO_TEST=TRUE 86
Port B				
TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1..0>	NO_TEST=TRUE 36 88
TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1..0>	NO_TEST=TRUE 36 88
	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	NO_TEST=TRUE 88
	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	NO_TEST=TRUE 88
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	NO_TEST=TRUE 36 88
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	NO_TEST=TRUE 36 88
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	NO_TEST=TRUE 36 88
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	NO_TEST=TRUE 36 88
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	NO_TEST=TRUE 88
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	NO_TEST=TRUE 88
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	NO_TEST=TRUE 88
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	NO_TEST=TRUE 88
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	88
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	88
	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	NO_TEST=TRUE 88
	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	NO_TEST=TRUE 88
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	NO_TEST=TRUE 36 88
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	NO_TEST=TRUE 36 88
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	NO_TEST=TRUE 36 88
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	NO_TEST=TRUE 36 88
DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	36 88
DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	36 88
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	88
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	88
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	88
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	88
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	NO_TEST=TRUE 88
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	NO_TEST=TRUE 88

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	NO_TEST=TRUE 81 84
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	NO_TEST=TRUE 81 84
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	NO_TEST=TRUE 81 84
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	NO_TEST=TRUE 81 84
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	84
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	84
Internal Panel				
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	NO_TEST=TRUE 84
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	NO_TEST=TRUE 84
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	NO_TEST=TRUE 84 87
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	NO_TEST=TRUE 84 87
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	84 87
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	84 87
Internal DP SPDIF				
		HDA	DP_INT_SPDIF_AUDIO	56 87

SYNC_MASTER=D8_AARON SYNC_DATE=03/13/2012

PAGE TITLE: TBT/DP Constraints

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=3X_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_MA2MA	*	=2X_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2X_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2X_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2X_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2X_DIELECTRIC	?
GDDR_CLK2CLK	*	=3X_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=3X_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_EDC2EDC	*	=3X_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=3X_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing			
Memory Address					
GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	NO_TEST=TRUE	?? 79
GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	NO_TEST=TRUE	?? 79
Address Dynamic Bus Inv					
GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	NO_TEST=TRUE	?? 79
GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	NO_TEST=TRUE	?? 79
Control					
GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	NO_TEST=TRUE	?? 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	NO_TEST=TRUE	?? 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	NO_TEST=TRUE	?? 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	NO_TEST=TRUE	?? 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	NO_TEST=TRUE	?? 79
GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	NO_TEST=TRUE	?? 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	NO_TEST=TRUE	?? 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	NO_TEST=TRUE	?? 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	NO_TEST=TRUE	?? 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	NO_TEST=TRUE	?? 79
Clock					
GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	NO_TEST=TRUE	?? 79
GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	NO_TEST=TRUE	?? 79
GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	NO_TEST=TRUE	?? 79
GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	NO_TEST=TRUE	?? 79
Data					
GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	NO_TEST=TRUE	?? 79
GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	NO_TEST=TRUE	?? 79
GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	NO_TEST=TRUE	?? 79
GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	NO_TEST=TRUE	?? 79
GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	NO_TEST=TRUE	?? 79
GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	NO_TEST=TRUE	?? 79
GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	NO_TEST=TRUE	?? 79
GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	NO_TEST=TRUE	?? 79
Error Detection					
GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	NO_TEST=TRUE	?? 79
GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	NO_TEST=TRUE	?? 79
GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	NO_TEST=TRUE	?? 79
GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	NO_TEST=TRUE	?? 79
GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	NO_TEST=TRUE	?? 79
GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	NO_TEST=TRUE	?? 79
GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	NO_TEST=TRUE	?? 79
GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	NO_TEST=TRUE	?? 79
Data Dynamic Bus Inv					
GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	NO_TEST=TRUE	?? 79
GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	NO_TEST=TRUE	?? 79
GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	NO_TEST=TRUE	?? 79
GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	NO_TEST=TRUE	?? 79
GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	NO_TEST=TRUE	?? 79
GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	NO_TEST=TRUE	?? 79
GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	NO_TEST=TRUE	?? 79
GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	NO_TEST=TRUE	?? 79
Forwarded Clock					
GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	NO_TEST=TRUE	?? 79
GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	NO_TEST=TRUE	?? 79
GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	NO_TEST=TRUE	?? 79
GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	NO_TEST=TRUE	?? 79
GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	NO_TEST=TRUE	?? 79
GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	NO_TEST=TRUE	?? 79
GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	NO_TEST=TRUE	?? 79
GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	NO_TEST=TRUE	?? 79

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing			
Memory Address					
GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	NO_TEST=TRUE	?? 80
GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	NO_TEST=TRUE	?? 80
Address Dynamic Bus Inv					
GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	NO_TEST=TRUE	?? 80
GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	NO_TEST=TRUE	?? 80
Control					
GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	NO_TEST=TRUE	?? 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	NO_TEST=TRUE	?? 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	NO_TEST=TRUE	?? 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	NO_TEST=TRUE	?? 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	NO_TEST=TRUE	?? 80
GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	NO_TEST=TRUE	?? 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	NO_TEST=TRUE	?? 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	NO_TEST=TRUE	?? 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	NO_TEST=TRUE	?? 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	NO_TEST=TRUE	?? 80
Clock					
GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	NO_TEST=TRUE	?? 80
GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	NO_TEST=TRUE	?? 80
GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	NO_TEST=TRUE	?? 80
GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	NO_TEST=TRUE	?? 80
Data					
GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	NO_TEST=TRUE	?? 80
GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	NO_TEST=TRUE	?? 80
GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	NO_TEST=TRUE	?? 80
GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	NO_TEST=TRUE	?? 80
GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	NO_TEST=TRUE	?? 80
GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	NO_TEST=TRUE	?? 80
GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	NO_TEST=TRUE	?? 80
GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	NO_TEST=TRUE	?? 80
Error Detection					
GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	NO_TEST=TRUE	?? 80
GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	NO_TEST=TRUE	?? 80
GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	NO_TEST=TRUE	?? 80
GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	NO_TEST=TRUE	?? 80
GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	NO_TEST=TRUE	?? 80
GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	NO_TEST=TRUE	?? 80
GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	NO_TEST=TRUE	?? 80
GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	NO_TEST=TRUE	?? 80
Data Dynamic Bus Inv					
GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	NO_TEST=TRUE	?? 80
GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	NO_TEST=TRUE	?? 80
GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	NO_TEST=TRUE	?? 80
GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	NO_TEST=TRUE	?? 80
GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	NO_TEST=TRUE	?? 80
GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	NO_TEST=TRUE	?? 80
GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	NO_TEST=TRUE	?? 80
GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	NO_TEST=TRUE	?? 80
Forwarded Clock					
GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	NO_TEST=TRUE	?? 80
GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	NO_TEST=TRUE	?? 80
GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	NO_TEST=TRUE	?? 80
GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	NO_TEST=TRUE	?? 80
GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	NO_TEST=TRUE	?? 80
GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	NO_TEST=TRUE	?? 80
GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	NO_TEST=TRUE	?? 80
GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	NO_TEST=TRUE	?? 80

GPU

Electrical Contraint Set	Physical	Spacing			
Clocks					
CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_PL			75
CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_NG			75
CLK_PCIE_PHY	CLK_PCIE	GPU_TESTMODE			81
CLK_PCIE_PHY	CLK_PCIE	GPU_PEX_TERMP			75
CLK_GPU_55S	CLK_GPU	FB_A0_CK_MID		NO_TEST=TRUE	79
CLK_GPU_55S	CLK_GPU	FB_A1_CK_MID		NO_TEST=TRUE	79
CLK_GPU_55S	CLK_GPU	FB_B0_CK_MID		NO_TEST=TRUE	80
CLK_GPU_55S	CLK_GPU	FB_B1_CK_MID		NO_TEST=TRUE	80
CLK_GPU_55S	CLK_GPU	FB_C0_CK_MID		NO_TEST=TRUE	
CLK_GPU_55S	CLK_GPU	FB_C1_CK_MID		NO_TEST=TRUE	ULTIMATE
CLK_GPU_55S	CLK_GPU	FB_D0_CK_MID		NO_TEST=TRUE	ONLY
CLK_GPU_55S	CLK_GPU	FB_D1_CK_MID		NO_TEST=TRUE	
CLK_GPU_55S	CLK_GPU	GPU_JTAG_TCK			78 81
CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK			81 82
CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK_R			82
CLK_GPU_55S	CLK_GPU	GPU_XTALOUT			
CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALOUT			81 82
CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALIN			81 82
SMB					
SMB_PHY	SMB	GPU_SMB_CLK			81 82
SMB_PHY	SMB	GPU_SMB_DAT			81 82
SMB_PHY	SMB	GPU_SMB_CLK_R			50 82
SMB_PHY	SMB	GPU_SMB_DAT_R			50 82
PCIe Compensation					
PCIE_50S	COMP_PCIE	FB_CAL_PD_VDDQ			77
PCIE_50S	COMP_PCIE	FB_CAL_PU_GND			77
PCIE_50S	COMP_PCIE	FB_CAL_TERM_GND			77

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing			
Reset					
GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L		?? 79
GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L		?? 79
GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L		?? 80
GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L		?? 80
GDDR_C0_RESET	GDDR_50S	GDDR_CTRL	FB_C0_RESET_L		
GDDR_C1_RESET	GDDR_50S	GDDR_CTRL	FB_C1_RESET_L		ULTIMATE
GDDR_D0_RESET	GDDR_50S	GDDR_CTRL	FB_D0_RESET_L		ONLY
GDDR_D1_RESET	GDDR_50S	GDDR_CTRL	FB_D1_RESET_L		

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions

BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	1.00MM	1000

Constraints

BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

BKLT MISCELLANEOUS

Electrical Contraint Set	Physical	Spacing		
SPI				
J56	SMB_PHY	SMB	SMB_PCH_BLC_SCL	50 89
J56	SMB_PHY	SMB	SMB_PCH_BLC_SDA	50 89
J81	SMB_PHY	SMB	SMB_TCON_BLC_SCL	50 89
J81	SMB_PHY	SMB	SMB_TCON_BLC_SDA	50 89
12M REFERENCE CRYSTAL				
E49	CLK_XTAL	XTAL	BLC_MCU_XTAL_IN	89
E48	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT	89
E46	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT_R	89
250K REFERENCE CLOCKS				
E45	CLK_PCH_50S	CLK_PCH	STRCLK_R1	89 90
E46	CLK_PCH_50S	CLK_PCH	LED_DRVR_CLK	90

Input Bus	Physical	Spacing	Voltage	DIDT	NO_TEST		
E90	POWER_PHY	POWER	12V			PP12V_S0_BLC_VIN2	89 90 91
E92	POWER_PHY	POWER	12V			PP12V_S0_BLC_VINP	89 91
E86	POWER_PHY	POWER	14V			PRE_REG_OUT	89 90
E87	POWER_PHY	POWER	3.3V			BLC_P3V3S	89 91
E84	POWER_PHY	POWER	3.3V			BLC_P3V3_REF	89 91
E90	POWER_PHY	POWER	3.3V			BLC_P3V3	
E82	POWER_PHY	POWER	3.3V			PP3V3_S0_BLC_R	89
E41	POWER_PHY	POWER	8V			SPTX_VIN	90
E40	POWER_PHY	POWER	8V			PP8V_BLC	89 90
E47	POWER_PHY	POWER	8V			BLC_VIN2	90 91
E82	POWER_PHY	POWER	14V			BOOST_FET_DRAIN	89
E85	POWER_PHY	POWER	12V			BOOST_VDD	89
E85	POWER_PHY	POWER	5V			PP5V_S0_BLC_R	89 90 91
E86	POWER_PHY	POWER	12V			PP12V_S0_BLC_F	91
Local Ground							
E99	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_1	90 91
E88	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_2	90 91
E85	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_3	90 91
E16	GND_PHY	GND	0V			AGND_BLC	90 91
Backlight							
D55	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1	90
D56	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1_R	90
D76	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2	90
D77	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2_R	90
E96	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3	90
D79	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3_R	90
D75	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_1	90
D74	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_2	90
D96	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_3	90
E80	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS1	90
E89	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS2	90
E79	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS3	90
E78	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C1	90
E77	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C2	90
E76	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C3	90
E93	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_1	90
E92	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_2	90
E91	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_3	90
E80	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK1	90
E81	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK2	90
E82	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK3	90
E83	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1_R	89 90
E84	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2_R	89 90
E85	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3_R	89 90
E40	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1	90 91
E39	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2	90 91
E38	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3	90 91
E48	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF1	90 91
E49	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF2	90 91
E47	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF3	90 91
M36	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP1	90
M36	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP2	90
M31	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP3	90
E97	BLC_CTL_PHY	BLC_CTL				BCOMP1	90
E97	BLC_CTL_PHY	BLC_CTL				BCOMP2	90
E96	BLC_CTL_PHY	BLC_CTL				BCOMP3	90
E44	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT1	90
E43	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT2	90
E42	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT3	90
E43	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_1	90
E42	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_2	90
E43	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_3	90
E36	BLC_CTL_PHY	BLC_CTL				PRE_REG_OUT_R	89
E35	BLC_CTL_PHY	BLC_CTL				BOOST_FB	89
E34	BLC_CTL_PHY	BLC_CTL				BOOST_COMP	89
E33	BLC_CTL_PHY	BLC_CTL				BOOST_COMP_C	89
E36	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV	89
E34	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV_R	89
E35	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS	89
E38	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS_R	89
D58	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_1	90
D57	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_2	90
D54	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_3	90
OUTPUT BUS							
E20	POWER_BLC_RET	BLC_HV	80V			IS1_BLC_F	91
E18	POWER_BLC_RET	BLC_HV	80V			IS2_BLC_F	91
E20	POWER_BLC_RET	BLC_HV	80V			IS3_BLC_F	91
E24	POWER_BLC_RET	BLC_HV	80V			IS1_BLC	90 91
E22	POWER_BLC_RET	BLC_HV	80V			IS2_BLC	90 91
E19	POWER_BLC_RET	BLC_HV	80V			IS3_BLC	90 91
E78	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_1	91
E79	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_1	91
E74	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_2	91
E75	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_2	91
E76	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_3	91
E73	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_3	91
E25	POWER_BLC	BLC_HV	80V			BLC_VOUT1	90 91
E24	POWER_BLC	BLC_HV	80V			BLC_VOUT2	90 91
E24	POWER_BLC	BLC_HV	80V			BLC_VOUT3	90 91

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BLC Constraints

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GPU CORE PHASES

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
	POWER_PHY	POWER	12V			PP12V_S0_GPUCORE_FLT 92 93 94
	POWER_PHY	POWER	5V			PP5V_S0_GPU_VCORE_VCC 92
Local Ground						
	GND_PHY	GND	0V			AGND_GPU 92
Phase 1						
	POWER_PHY	POWER	12V			REG_LVCC_UB510 93
	POWER_PHY	POWER	12V			REG_UVCC_UB510 93
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_1 92 93
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM1_R 92
	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1 93
	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_1 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_1 93
	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_1 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_P 92 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_N 92 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_P 92
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_N 92
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS1_RR_2 92
Phase 2						
	POWER_PHY	POWER	12V			REG_LVCC_UB530 93
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_2 92 93
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM2_R 92
	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2 93
	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_2 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_2 93
	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_2 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_P 92 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_N 92 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_P 92
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_N 92
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS2_RR_2 92
Phase 3						
	POWER_PHY	POWER	12V			REG_VCC_UB550 93
	POWER_PHY	POWER	12V			REG_UVCC_UB550 93
	POWER_PHY	POWER	12V			REG_LVCC_UB550 93
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_3 92 93
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM3_R 92
	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_3 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_3 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3_RC 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_3 93
	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_3 93
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_3 93
	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_3 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_P 92 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_N 92 93
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_P 92
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_N 92
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS3_RR_2 92
Phase 4						
	POWER_PHY	POWER	12V			REG_LVCC_UB650 94
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_4 92 94
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM4_R 92
	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_4 94
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_4 94
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4_RC 94
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_4 94
	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_4 94
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_4 94
	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_4 94
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_P 92 94
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_N 92 94
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_P 92
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_N 92
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS4_RR_2 92

GPU CORE CONTROLLER

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL6334						
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP 92
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_R 92
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_RC 92
	VR_CTL_PHY	VR_CTL				VR_GPU_FB 92
	VR_CTL_PHY	VR_CTL				VR_GPU_FB_R 92
	VR_CTL_PHY	VR_CTL				VR_GPU_VDIFF 92
	VR_CTL_PHY	VR_CTL				VR_VDF_R1 92
	VR_CTL_PHY	VR_CTL				VR_VDF_R2 92
	VR_CTL_PHY	VR_CTL				VR_GPU_TCOMP 92
	VR_CTL_PHY	VR_CTL				VR_GPU_OFS 92
	VR_CTL_PHY	VR_CTL				VR_GPU_FS 92
		VR_CTL				VR_GPU_EN_VTT 92
		VR_CTL				PM_EN_REG_GPUCORE_S0 64 92
		VR_CTL				PM_PGOOD_REG_GPUCORE_S0 5 64 92
		VR_CTL				GPU_PSI_L 82 92
	VR_CTL_PHY	VR_CTL				VR_GPU_IOUT
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON 51 92 110
	VR_CTL_PHY	VR_CTL				VR_GPU_FAN 92 110
		VR_CTL				VR_GPU_VRDHOT 92
		VR_CTL				VR_GPU_EN_PWR
	VR_CTL_PHY	VR_CTL				VR_GPU_SS 92
	VR_CTL_PHY	VR_CTL				VR_GPU_DAC 92
	VR_CTL_PHY	VR_CTL				VR_GPU_REF 92
	VR_CTL_PHY	VR_CTL				VR_GPU_TM 92
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON 51 92 110
	VR_CTL_PHY	VR_CTL				VR_GPU_FAN 92 110
	VR_CTL_PHY	VR_CTL				VR_GPU_VRHOT
		VR_CTL				GPU_PSI_R
		VR_CTL				GPU_PSI_L_R
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON_R 92
VSNS_GPU_VDD	SNS_DIFF_PHY	SENSE				VSNS_GPU_VDD 78 92
VSNS_GPU_VSS	SNS_DIFF_PHY	SENSE				VSNS_GPU_VSS 78 92
	SNS_DIFF_PHY	SENSE				VR_GPU_VSEN 92
	SNS_DIFF_PHY	SENSE				VR_GPU_RGND 92
GPU VIDS						
		VR_VID				REG_GPUCORE_VID7 92
		VR_VID				REG_GPUCORE_VID6 78 92
		VR_VID				REG_GPUCORE_VID5 78 92
		VR_VID				REG_GPUCORE_VID4 78 92
		VR_VID				REG_GPUCORE_VID3 78 92
		VR_VID				REG_GPUCORE_VID2 78 92
		VR_VID				REG_GPUCORE_VID1 78 92
		VR_VID				REG_GPUCORE_VID0 92
		VR_VID				GPU_VCORE_VID6
		VR_VID				GPU_VCORE_VID5 78 82
		VR_VID				GPU_VCORE_VID4 78 82
		VR_VID				GPU_VCORE_VID3 78 82
		VR_VID				GPU_VCORE_VID2 78 82
		VR_VID				GPU_VCORE_VID1 78 82
		VR_VID				GPU_VCORE_VID0 78 82
Output Bus						
	POWER_PHY	POWER	0.9V			PPVCORE_S0_GPU 6

GPU FBVDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
	POWER_PHY	POWER	5V			REG_VCC_UB750 95
	POWER_PHY	POWER	5V			REG_PVCC_UB750 95
Local Ground						
	GND_PHY	GND	0V			AGND_FBVDDQ 95
FBVDDQ						
	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_FBVDDQ 95
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_FBVDDQ 95
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_FBVDDQ_RC 95
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ 95
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ_R
	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_FBVDDQ 95
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_FBVDDQ 95
		SENSE				VSNS_FBVDDQ
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_P 78 95
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_N 78 95
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_P 95
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_N 95
		SENSE				FBVDDQ_SENSE_R
	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_OCSET
	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_VO 95
		SENSE				REG_FBVDDQ_FB 95
		SENSE				REG_FBVDDQ_RTN 95
Output Bus						
	POWER_PHY	POWER	1.5V			PP1V5R1V35_S0_GPU_REG 6 95

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VENI, VIDI, VICI!

Electrical Contraint Set		Physical	Spacing		
Ethernet					
I47A	ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	39 40
I47B	ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	39 40
I47C		ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	40
I47D		ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	40
I45D			ENET_TRANS	ENETCONN_MCT3	40
I45C			ENET_TRANS	ENETCONN_MCT2	40
I45B			ENET_TRANS	ENETCONN_MCT1	40
I45A			ENET_TRANS	ENETCONN_MCT0	40
I47E		ENET_COMP_PHY	COMP_ENET	ENET_RDAC	39
SD					
I47J	SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0> NO_TEST=TRUE	39
I48C		SD_PHY	SD	SDCONN_DATA<7..0>	39 41
I49C		SD_PHY	SD	SDCONN_DATA_R<7..0> NO_TEST=TRUE	41
I48J	SD_CMD	SD_PHY	SD	ENET_SD_CMD NO_TEST=TRUE	39
I48K		SD_PHY	SD	SDCONN_CMD NO_TEST=TRUE	39 41
I49K		SD_PHY	SD	SDCONN_CMD_R NO_TEST=TRUE	41
I48H	SD_CLK	SD_PHY	SD	ENET_SD_CLK NO_TEST=TRUE	39
I48G		SD_PHY	SD	SDCONN_CLK NO_TEST=TRUE	39 41
I48G		SD_PHY	SD	SDCONN_CLK_R NO_TEST=TRUE	41
I48D		SD_PHY	SD	ENET_MEDIA_SENSE	15 18 39
I48E		SD_PHY	SD	ENET_SD_DETECT_L	39 41
I48F		SD_PHY	SD	SDCONN_WP	39 41
CIV SPI					
I49D		SPI_50S	SPI	ENET_SCLK	39
I48D		SPI_50S	SPI	ENET_MISO	39
I49F		SPI_50S	SPI	ENET_MOSI	39
I49J		SPI_50S	SPI	ENET_CS_L	39

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S

CIV-specific Spacing Definitions
Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints
Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
ENET_DIFF	*	*	ENET_DIFF_ISO	
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF	
ENET_TRANS	*	*	ENET_TRANS_ISO	2 kV isolation
COMP_ENET	*	*	COMP_ENET_ISO	
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF	

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

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4V5_*

	Physical	Spacing	Netname	
H1		PM	4V5_REG_EN	56
H2	POWER_PHY	POWER	4V5_REG_IN	56

ACDC_*

	Spacing	Netname	
H3	PM	ACDC_BURST_EN	48
H4	PM	ACDC_BURST_EN_L	48

ALL_*

	Spacing	Netname	
H5	PM	ALL_SYS_PWRGD	5 47 65

AP_*

	Spacing	Netname	
H6	GENERIC_ISO	AP_CLKREQ_L	15 21
H7	GENERIC_ISO	AP_CLKREQ_L_ISO	15 35
H8	GENERIC_ISO	AP_CLKREQ_Q_L	35
H9	GENERIC_ISO	AP_EVENT_L	35 47 48
H10	GENERIC_ISO	AP_PWR_EN_ISO	15 35
H11	PM	AP_RESET_CONN_L	35
H12	PM	AP_RESET_L	26 35
H13	PM	AP_WAKE_L	35

BLC12V_*

	Spacing	Netname
H14	PM	BLC12V_FAULT
H15	PM	BLC12V_FAULT_L
H16	PM	BLC12V_UVLO
H17	PM	BLC12V_UVLO_OUT
H18	PM	BLC12V_UVLO_REF

BLC_*

	Physical	Spacing	Voltage	Netname	
H19		GENERIC_ISO		BLC_BL	89 91
H20		GENERIC_ISO		BLC_BL_GATE	91
H21		GENERIC_ISO		BLC_BST	89 91
H22		GENERIC_ISO		BLC_BST_R	89
H23		GENERIC_ISO		BLC_BYPASS_GATE	91
H24		GENERIC_ISO		BLC_DIM_MCU	89
H25		PM		BLC_EN	87 89 90
H26		GENERIC_ISO		BLC_ENA	89
H27		GENERIC_ISO		BLC_ENA1	89 91
H28		PM		BLC_EN_DELAY	87
H29		PM		BLC_EN_R	89

BLC_*

	Physical	Spacing	Voltage	Netname	
H30		PM		BLC_EXT_BOOT	48 89
H31		PM		BLC_EXT_BOOT_L	89
H32	BLC_CTL_PHY	BLC_CTL	5V	BLC_MCU_AOUT_R	91
H33		GENERIC_ISO		BLC_MCU_BV	89 91
H34		GENERIC_ISO		BLC_MCU_BV_D	91
H35		GENERIC_ISO		BLC_MCU_BV_R	91
H36	SMB_PHY	SMB		BLC_MCU_B_SDA_CONN	89
H37		GENERIC_ISO		BLC_MCU_FLAG_V	89
H38		GENERIC_ISO		BLC_MCU_PWM5	89
H39		GENERIC_ISO		BLC_MCU_PWM5_R	89
H40		PM		BLC_MCU_RESET	89
H41		PM		BLC_MCU_RESET_L	89
H42		PM		BLC_MCU_RESET_R_L	89
H43	XDP_PHY	CLK_JTAG		BLC_MCU_RTCK	89
H44		GENERIC_ISO		BLC_MCU_RXD0	89
H45	XDP_PHY	XDP		BLC_MCU_TCK	89
H46	XDP_PHY	XDP		BLC_MCU_TDI	89
H47	XDP_PHY	XDP		BLC_MCU_TDO	89
H48	XDP_PHY	XDP		BLC_MCU_TMS	89
H49	XDP_PHY	XDP		BLC_MCU_TRST	89
H50	XDP_PHY	XDP		BLC_MCU_TXD0	89
H51		GENERIC_ISO		BLC_MCU_UVLO	89
H52		GENERIC_ISO		BLC_ON	91
H53		GENERIC_ISO		BLC_ON_DRAIN	91
H54		GENERIC_ISO		BLC_ON_R	91
H55		GENERIC_ISO		BLC_P_ON	89 90 91
H56		GENERIC_ISO		BLC_P_ON_BYPASS	91
H57		GENERIC_ISO		BLC_P_ON_D	91
H58		GENERIC_ISO		BLC_P_ON_DRAIN	91
H59		GENERIC_ISO		BLC_P_ON_D_R	91
H60		GENERIC_ISO		BLC_P_ON_GATE	91
H61		GENERIC_ISO		BLC_P_ON_R	91
H62		GENERIC_ISO		BLC_SKIP	90
H63		GENERIC_ISO		BLC_SNUB_1	90
H64		GENERIC_ISO		BLC_SNUB_2	90
H65		GENERIC_ISO		BLC_SNUB_3	90
H66		GENERIC_ISO		BLC_UVLO	89 91
H67		GENERIC_ISO		BLC_VIN2_GATE	91
H68		GENERIC_ISO		BLC_VIN2_SRC	91
H69		GENERIC_ISO		BLC_VINP_GATE	91
H70		GENERIC_ISO		BLC_VIN_SNS	90
H71		GENERIC_ISO		BLC_VSYNC	87 89
H72		GENERIC_ISO		BLC_VSYNC_R	89

BOOST_*

	Spacing	Netname	
H73	GENERIC_ISO	BOOST_BP	89
H74	GENERIC_ISO	BOOST_BYPASS	89 91
H75	GENERIC_ISO	BOOST_BYPASS_GATE	89
H76	PM	BOOST_EN_GATE	89
H77	PM	BOOST_EN_L	89
H78	GENERIC_ISO	BOOST_RC	89
H79	GENERIC_ISO	BOOST_SS	89

BT_*

	Spacing	Netname	
H80	PM	BT_PWR_EN	35
H81	PM	BT_PWR_RST_L	15 20 35
H82	PM	BT_PWR_RST_L_Q	35

BURSTMODE_*

	Spacing	Netname	
H83	PM	BURSTMODE_EN	71
H84	PM	BURSTMODE_EN_L	6 48 71

CAM_*

	Spacing	Netname	
H85	PM	CAM_EXT_BOOT	42 43
H86	PM	CAM_PROC_RESET	43
H87	PM	CAM_PROC_RESET_L	42 43

CPU_*

	Physical	Spacing	Netname	
H88		PM	CPU_PWRGD_1V05_R	28
H89		PM	CPU_PWRGD_3V3	28
H90		PM	CPU_PWRGD_3V3_R	28
H91		GENERIC_ISO	CPU_SKTOCC	64
H92	CPU_PHY	CPU	CPU_THRMTRIP_3V3	47 48
H93	CPU_PHY	CPU	CPU_THRMTRIP_R_L	48

DEBUG_*

	Spacing	Netname	
H94	PM	DEBUG_RESET_L	26 49

DP_*

	Physical	Spacing	Netname	
H95		PM	DP_AUXIO_EN	15 86 88
H96		PM	DP_GPU_MUX_EN	84
H97		GENERIC_ISO	DP_INTPNL_HPD	84 87
H98		GENERIC_ISO	DP_INT_EG_HPD	82 84
H99	TBT_GEN_55S	TBT_GEN	DP_TBTPA_DDC_CLK	85 86
H100	TBT_GEN_55S	TBT_GEN	DP_TBTPA_DDC_DATA	85 86
H101		GENERIC_ISO	DP_TBTPA_HPD	36 86
H102	TBT_GEN_55S	TBT_GEN	DP_TBTPB_DDC_CLK	85 88
H103	TBT_GEN_55S	TBT_GEN	DP_TBTPB_DDC_DATA	85 88
H104		GENERIC_ISO	DP_TBTPB_HPD	36 88

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ENETCONN_*

	Spacing	Netname	
E1	GENERIC_ISO	ENETCONN_TCT	40

ENET_*

	Physical	Spacing	Netname	
E2		GENERIC_ISO	ENET_ACT	40
E3		GENERIC_ISO	ENET_ASF_GPIO	47 48
E4		GENERIC_ISO	ENET_CLKREQ_L	15 18 40
E5		PM	ENET_CLKREQ_L_Q	39 40
E6		PM	ENET_CR_1V8_EN	
E7		PM	ENET_CR_1V8_EN_R	
E8		PM	ENET_CR_3V3_EN_L	
E9		PM	ENET_CR_3V3_EN_L_R	
E10		PM	ENET_CR_PWREN	39 41
E11	XDP_PHY	XDP	ENET_LOW_PWR	26 39 41
E12		PM	ENET_PWR_EN_L	40
E13		PM	ENET_PWR_EN_L_R	40
E14		PM	ENET_RESET_L	39 41
E15		PM	ENET_SD_RESET_L	26 41
E16		GENERIC_ISO	ENET_SR_DISABLE	39
E17		GENERIC_ISO	ENET_SR_LX	39 40
E18		PM	ENET_WAKE_L	40

FAN_*

	Spacing	Netname	
E19	GENERIC_ISO	FAN_0_PWM_FET	54
E20	GENERIC_ISO	FAN_0_PWM_FILT	54
E21	GENERIC_ISO	FAN_0_TACH_FET	54
E22	GENERIC_ISO	FAN_0_TACH_FILT	54

FBVDD_*

	Spacing	Netname	
E23	GENERIC_ISO	FBVDD_ALTVO	82 95

FB_*

	Spacing	Netname	
E24	GENERIC_ISO	FB_A0_VREFC	79
E25	GENERIC_ISO	FB_A0_VREFD	79
E26	GENERIC_ISO	FB_A1_VREFC	79
E27	GENERIC_ISO	FB_A1_VREFD	79
E28	GENERIC_ISO	FB_B0_VREFC	80
E29	GENERIC_ISO	FB_B0_VREFD	80
E30	GENERIC_ISO	FB_B1_VREFC	80
E31	GENERIC_ISO	FB_B1_VREFD	80
E32	GENERIC_ISO	FB_VREF	77

FET_*

	Physical	Spacing	Voltage	Netname	
E33		GENERIC_ISO		FET_EN_P12V_S0	74
E34		GENERIC_ISO		FET_EN_P12V_S0_BLC	74
E35		GENERIC_ISO		FET_EN_P12V_S0_BLC_R	74
E36		GENERIC_ISO		FET_EN_P12V_S0_R	74
E37		GENERIC_ISO		FET_EN_P12V_S5	74
E38		GENERIC_ISO		FET_EN_P12V_S5_R	74
E39		GENERIC_ISO		FET_EN_VDDQ_S0	74
E40		GENERIC_ISO		FET_HDD_SLGSW	52
E41	POWER_PHY	POWER	12V	FET_VCC_U7950	74
E42	POWER_PHY	POWER	12V	FET_VCC_U7970	74
E43	POWER_PHY	POWER	12V	FET_VCC_U7980	74

FLAG_*

	Spacing	Netname	
E44	GENERIC_ISO	FLAG_V	89 90 91

G3_*

	Spacing	Netname	
E45	GENERIC_ISO	G3_POWERON_L	47 48

GND_*

	Spacing	Netname	
E46	SENSE	GND_SMC_AVSS	47 48 51 55

GPU_*

	Physical	Spacing	Netname	
E47		GENERIC_ISO	GPU_ALT_VREF	77 82
E48		GENERIC_ISO	GPU_BUFRSTN	83
E49		GENERIC_ISO	GPU_IFPAB_PLLVDD	81
E50		GENERIC_ISO	GPU_IFPA_IOVDD	81
E51		GENERIC_ISO	GPU_IFPB_IOVDD	81
E52		GENERIC_ISO	GPU_IFPC_IOVDD	81
E53	XDP_PHY	XDP	GPU_JTAG_TDI	78 81
E54	XDP_PHY	XDP	GPU_JTAG_TDO	78 81
E55	XDP_PHY	XDP	GPU_JTAG_TMS	78 81
E56	XDP_PHY	XDP	GPU_JTAG_TRST_L	81
E57		GENERIC_ISO	GPU_MLS_STRAP0	81 82
E58		GENERIC_ISO	GPU_MLS_STRAP1	81 82
E59		GENERIC_ISO	GPU_MLS_STRAP2	81 82
E60		GENERIC_ISO	GPU_MLS_STRAP3	81 82
E61		GENERIC_ISO	GPU_MLS_STRAP4	81 82
E62		GENERIC_ISO	GPU_RESET_L	26 75 82
E63	SPI_50S	SPI	GPU_ROM_CS_L	81 82
E64	SPI_50S	SPI	GPU_ROM_CS_L_R	82
E65	SPI_50S	SPI	GPU_ROM_SI	81 82
E66	SPI_50S	SPI	GPU_ROM_SI_R	82
E67	SPI_50S	SPI	GPU_ROM_SO	81 82
E68	SPI_50S	SPI	GPU_ROM_SO_R	82
E69	SPI_50S	SPI	GPU_ROM_WP_L	82

HDD_*

	Spacing	Netname	
E70	GENERIC_ISO	HDD_12V_S0_GATE	52
E71	GENERIC_ISO	HDD_OOB_1V00_REF	52
E72	PM	HDD_PWR_EN	21 52
E73	GENERIC_ISO	HDD_PWR_EN_L	52
E74	GENERIC_ISO	HDD_PWR_EN_R	52

I2C_*

	Physical	Spacing	Netname	
E75	SMB_PHY	SMB	I2C_TCON_MAS_SCL	50 87
E76	SMB_PHY	SMB	I2C_TCON_MAS_SDA	50 87

IFPD_*

	Spacing	Netname	
E77	GENERIC_ISO	IFPD_RSET	81

IFPEF_*

	Spacing	Netname	
E78	GENERIC_ISO	IFPEF_RSET	81

ISNSA_*

	Electrical	Physical	Spacing	Netname	
E79	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_N	51
E80	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_P	51
E81	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_N	55
E82	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_P	55
E83	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_N	55
E84	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_P	55
E85	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_N	51
E86	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_P	51
E87	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_N	51
E88	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_P	51
E89	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_N	55
E90	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_P	55
E91	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_N	51
E92	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_P	51
E93	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_N	51
E94	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_P	51
E95	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_N	51
E96	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_P	51
E97	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_N	55
E98	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_P	55
E99	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_N	51
E100	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_P	51
E101	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_N	51
E102	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_P	51

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ISNS_*

	Physical	Spacing	Netname	
E1	SNS_PHY	SENSE	ISNS_CPUAXG_FB	51
E2	SNS_PHY	SENSE	ISNS_CPUAXG_N	51
E3	SNS_PHY	SENSE	ISNS_CPUAXG_P	51
E4	SNS_PHY	SENSE	ISNS_CPUCORE_FB	51
E5	SNS_PHY	SENSE	ISNS_CPUCORE_N	51
E6	SNS_PHY	SENSE	ISNS_CPUCORE_P	51
E7	SNS_PHY	SENSE	ISNS_GPUCORE_FB	51
E8	SNS_PHY	SENSE	ISNS_GPUCORE_N	51
E9	SNS_PHY	SENSE	ISNS_GPUCORE_P	51
E10	SNS_PHY	SENSE	ISNS_P12VG3H_R	51
E11	SNS_PHY	SENSE	ISNS_P12VS0_CPU_P1V05_R	55
E12	SNS_PHY	SENSE	ISNS_P12VS0_CPU_VCCSA_R	55
E13	SNS_PHY	SENSE	ISNS_P12VS0_FBVDDQ_R	51
E14	SNS_PHY	SENSE	ISNS_P12VS0_HDD_R	51
E15	SNS_PHY	SENSE	ISNS_P12VS0_P1V05_R	55
E16	SNS_PHY	SENSE	ISNS_P1V05S0_PCH_R	51
E17	SNS_PHY	SENSE	ISNS_P1V5S0_CPU_MEM_R	51
E18	SNS_PHY	SENSE	ISNS_P3V3S0_SSD_R	51
E19	SNS_PHY	SENSE	ISNS_P3V3S4_AP_R	55
E20	SNS_PHY	SENSE	ISNS_P5VS0_HDD_R	51
E21	SNS_PHY	SENSE	ISNS_PVDDQS3_DDR_R	51

ISOLATE_*

	Spacing	Netname	
E22	PM	ISOLATE_CPU_MEM_5V	28
E23	PM	ISOLATE_CPU_MEM_5V_L	28

JTAG_*

	Physical	Spacing	Netname	
E24	XDP_PHY	XDP	JTAG_GMUX_TMS	20
E25	XDP_PHY	XDP	JTAG_TBT_TDI	15 21
E26	XDP_PHY	XDP	JTAG_TBT_TDI_ISOL	15 36
E27	XDP_PHY	XDP	JTAG_TBT_TDO	15 21
E28	XDP_PHY	XDP	JTAG_TBT_TDO_ISOL	15 36
E29	XDP_PHY	XDP	JTAG_TBT_TMS	15 18
E30	XDP_PHY	XDP	JTAG_TBT_TMS_ISOL	15 36

LED_*

	Spacing	Netname	
E31	PM	LED_DRIVER_EN	90 91
E32	PM	LED_DRIVER_EN_L	91
E33	PM	LED_DRIVER_EN_L_R	91
E34	GENERIC_ISO	LED_DRIVER_OVP1	90 91
E35	GENERIC_ISO	LED_DRIVER_OVP1P	89 90
E36	GENERIC_ISO	LED_DRIVER_OVP1_OUT	90
E37	GENERIC_ISO	LED_DRIVER_OVP2	90 91
E38	GENERIC_ISO	LED_DRIVER_OVP2P	89 90
E39	GENERIC_ISO	LED_DRIVER_OVP2_OUT	90
E40	GENERIC_ISO	LED_DRIVER_OVP3	90 91
E41	GENERIC_ISO	LED_DRIVER_OVP3P	89 90
E42	GENERIC_ISO	LED_DRIVER_OVP3_OUT	90

LPCPLUS_*

	Spacing	Netname	
E43	GENERIC_ISO	LPCPLUS_GPIO	21 49

LPC_*

	Spacing	Netname	
E44	GENERIC_ISO	LPC_PWRDWN_L	19 26 47 49
E45	GENERIC_ISO	LPC_SERIRQ	18 47 49

MEMVTT_*

	Spacing	Netname	
E46	PM	MEMVTT_EN	28 64
E47	PM	MEMVTT_EN_L	28

MEM_*

	Spacing	Netname	
E48	GENERIC_ISO	MEM_EVENT_L	29 30 31 32 47 48

MOJO_*

	Physical	Spacing	Netname	
E49	XDP_PHY	XDP	MOJO_RX_L	45 47 48
E50	XDP_PHY	XDP	MOJO_TX_L	45 47 48

OCA_*

	Spacing	Netname	
E51	GENERIC_ISO	OCA_FET_DRAIN	91

OVP_*

	Spacing	Netname	
E52	GENERIC_ISO	OVP_OREF	91
E53	GENERIC_ISO	OVP_OUT1	91
E54	GENERIC_ISO	OVP_OUT1_R	91
E55	GENERIC_ISO	OVP_OUT2	91
E56	GENERIC_ISO	OVP_OUT2_R	91
E57	GENERIC_ISO	OVP_OUT3	91
E58	GENERIC_ISO	OVP_OUT3_R	91

P1V2_*

	Spacing	Netname	
E59	PM	P1V2_S4_EN	43

P1V8_*

	Spacing	Netname	
E60	PM	P1V8_S4_EN	43

P3V3AP_*

	Spacing	Netname	
E61	GENERIC_ISO	P3V3AP_VMON	35

P3V3_*

	Spacing	Netname	
E62	GENERIC_ISO	P3V3_S0_EN_G	74
E63	GENERIC_ISO	P3V3_S3_EN_G	74

P3V42G3H_*

	Spacing	Netname	
E64	GENERIC_ISO	P3V42G3H_BOOST	73

P5V_*

	Spacing	Netname	
E65	GENERIC_ISO	P5V_S0_EN_G	74

PCA9557D_*

	Spacing	Netname	
E66	GENERIC_ISO	PCA9557D_RESET_L	26 28 34

PCH_*

	Physical	Spacing	Netname	
E67		PM	PCH_BLC_EXT_BOOT	21 89
E68		PM	PCH_BLC_EXT_BOOT_R	15 21
E69		PM	PCH_BLC_MCU_RESET	21 89
E70		PM	PCH_BLC_MCU_RESET_R	15 21
E71		PM	PCH_CAM_RESET	15 21
E72		PM	PCH_CAM_RESET_R	21 43
E73		GENERIC_ISO	PCH_DSWVRMEN	19
E74	CPU_PHY	CPU	PCH_PECI	21
E75	CPU_PHY	CPU	PCH_PROCPWRGD	21
E76		GENERIC_ISO	PCH_RCIN_L	21
E77		GENERIC_ISO	PCH_RI_L	19
E78		GENERIC_ISO	PCH_SMBALERT_L	15 18
E79		GENERIC_ISO	PCH_SRTCRST_L	18
E80		GENERIC_ISO	PCH_STRP_TOPBLK_SWP_L	20
E81		GENERIC_ISO	PCH_SUSWARN_L	15 19

PCIE_*

	Spacing	Netname	
E82	GENERIC_ISO	PCIE_CLKREQ5_GPIO44_L	18
E83	PM	PCIE_WAKE_L	19 35 40

PEG_*

	Spacing	Netname	
E84	GENERIC_ISO	PEG_CLKREQ_L	15 18 75

PGOOD_*

	Spacing	Netname	
E85	PM	PGOOD_P1V5_S0_DLY	28

PLT_*

	Spacing	Netname	
E86	PCH	PLT_RESET_L	20 26
E87	PCH	PLT_RST_BUF_L	26

PM_*

	Spacing	Netname	
E88	PM	PM_CLKRUN_L	47 48 49
E89	PM	PM_DSW_PWRGD	47 48 65
E90	PM	PM_EN_FET_P12V_S0	64 74
E91	PM	PM_EN_FET_P12V_S0_R	74
E92	PM	PM_EN_FET_P3V3_S0	64 74
E93	PM	PM_EN_FET_P3V3_S4	64 74
E94	PM	PM_EN_FET_P5V_S0	64 74
E95	PM	PM_EN_FET_VDDQ_S0	64 74
E96	PM	PM_EN_LDO_DDRVTT_S0	64 72
E97	PM	PM_EN_REG_CPUCORE_S0	64 66

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PM_*

	Spacing	Netname	
B1	PM	PM_EN_REG_CPU_P1V05_S0	64 69
B2	PM	PM_EN_REG_FBVDDQ_S0	64 95
B3	PM	PM_EN_REG_GPUCORE_S0_R	92
B4	PM	PM_EN_REG_P1V05_S0	64 95
B5	PM	PM_EN_REG_P1V8_S0	64 72
B6	PM	PM_EN_REG_P3V3_S5	64 71 74
B7	PM	PM_EN_REG_P5V_S4	64 71
B8	PM	PM_EN_REG_VCCSA_S0	64 70
B9	PM	PM_EN_REG_VDDQ_S3	64 72
B10	PM	PM_EN_S0	64
B11	PM	PM_EN_S4	64
B12	PM	PM_EN_USB_PWR	45 46 64
B13	PM	PM_LED_A_ALL_SYS_PWRGD	5
B14	PM	PM_LED_A_BLC_GOOD	5
B15	PM	PM_LED_A_CPUAXG_PGOOD	5
B16	PM	PM_LED_A_GPU_GOOD	5
B17	PM	PM_LED_A_PGOOD_CPUCORE_S0	5
B18	PM	PM_LED_A_PGOOD_CPU_P1V05_S0	5
B19	PM	PM_LED_A_PGOOD_REG_FBVDDQ_S0	5
B20	PM	PM_LED_A_PGOOD_REG_GPUCORE_S0	5
B21	PM	PM_LED_A_PGOOD_REG_P1V05	5
B22	PM	PM_LED_A_PGOOD_REG_VDDQ_S3	5
B23	PM	PM_LED_A_S4	5
B24	PM	PM_LED_A_S5	5
B25	PM	PM_LED_A_SLP_S3	5
B26	PM	PM_LED_A_VIDEO_ON	5
B27	PM	PM_LED_K_ALL_SYS_PWRGD	5
B28	PM	PM_LED_K_BLC_GOOD	5
B29	PM	PM_LED_K_CPUAXG_PGOOD	5
B30	PM	PM_LED_K_GPU_GOOD	5
B31	PM	PM_LED_K_PGOOD_CPUCORE_S0	5
B32	PM	PM_LED_K_PGOOD_CPU_P1V05_S0	5
B33	PM	PM_LED_K_PGOOD_REG_FBVDDQ_S0	5
B34	PM	PM_LED_K_PGOOD_REG_GPUCORE_S0	5
B35	PM	PM_LED_K_PGOOD_REG_P1V05	5
B36	PM	PM_LED_K_PGOOD_REG_VDDQ_S3	5
B37	PM	PM_LED_K_SLP_S3	5
B38	PM	PM_MEM_PWRGD_L	28
B39	PM	PM_PCH_APWROK	19 65
B40	PM	PM_PCH_PWROK	15 19 26 35 43 65 89
B41	PM	PM_PCH_PWROK_APWROK	65
B42	PM	PM_PCH_SYS_PWROK	19 48 65
B43	PM	PM_PGOOD_FBVDDQ_VDDQ_S0	64
B44	PM	PM_PGOOD_FET_P12V_S0	74
B45	PM	PM_PGOOD_FET_P12V_S0_BLC	74 91
B46	PM	PM_PGOOD_FET_P12V_S5	74
B47	PM	PM_PGOOD_FET_P3V3_S0	64 74
B48	PM	PM_PGOOD_FET_P5V_S0	64 74
B49	PM	PM_PGOOD_FET_VDDQ_S0	28 64 74
B50	PM	PM_PGOOD_P3V3_S4_FET	27 35 64 74
B51	PM	PM_PGOOD_REG_ALL_P1V05_S0	64 65
B52	PM	PM_PGOOD_REG_ALL_P1V05_S0_R	28 64
B53	PM	PM_PGOOD_REG_CPUCORE_S0	5 25 65 66
B54	PM	PM_PGOOD_REG_CPU_P1V05_S0	5 64 69
B55	PM	PM_PGOOD_REG_FBVDDQ_S0	5 64 95
B56	PM	PM_PGOOD_REG_P1V05_S0	5 64 95
B57	PM	PM_PGOOD_REG_P1V8_S0	64 72
B58	PM	PM_PGOOD_REG_P3V3_S5	65 71
B59	PM	PM_PGOOD_REG_P5V_S4	64 71
B60	PM	PM_PGOOD_REG_VCCSA_S0	64 65 70
B61	PM	PM_PGOOD_REG_VDDQ_S3	5 64 72
B62	PM	PM_PWRBTN_L	15 19 25 47
B63	PM	PM_RSMRST_PCH_L	19 65
B64	PM	PM_RSMRST_PCH_L_R	65
B65	PM	PM_SLP_S3_L	5 15 19 28 40 47 48 64
B66	PM	PM_SLP_S4_L	15 19 47 64
B67	PM	PM_SLP_S5_L	15 19 47 64
B68	PCH	PM_SYSRST_L	19 25 26 47
B69	PCH	PM_THRMTRIP_L	21 48
B120	PM	PGOOD_P12V_S0_R	65
B130	PM	PGOOD_P12V_S0	64 65 74

PP12V_*

	Physical	Spacing	Voltage	Netname	
B30	POWER_PHY	POWER	12V	PP12V_LCD	87
B41	POWER_PHY	POWER	12V	PP12V_LCD_EXT	87
B72	POWER_PHY	POWER	12V	PP12V_S0_FAN_0_FILT	54
B73	POWER_PHY	POWER	12V	PP12V_S0_HDD_FET	44 52

PP1V05_*

	Physical	Spacing	Voltage	Netname	
B74	POWER_PHY	POWER	1.05V	PP1V05_GPU_FB_DLL_AVDD	77
B75	POWER_PHY	POWER	1.05V	PP1V05_GPU_FB_PLL_AVDD	77
B76	POWER_PHY	POWER	1.05V	PP1V05_GPU_IFPD_IOVDD	81
B77	POWER_PHY	POWER	1.05V	PP1V05_GPU_IFPEF_IOVDD	81
B78	POWER_PHY	POWER	1.05V	PP1V05_GPU_PLLVDD	81
B79	POWER_PHY	POWER	1.05V	PP1V05_GPU_SP_PLLVDD	81 83
B80	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	17 22
B81	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	17 22

PP1V2_*

	Physical	Spacing	Voltage	Netname	
B82	POWER_PHY	POWER	1.2V	PP1V2_ENET_INTREG	40
B83	POWER_PHY	POWER	1.2V	PP1V2_G3H_SMC_VDDC	47
B84	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_AVDDL	39
B85	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_GPHYPLL	39
B86	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_PCIEPLL	39
B87	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_CRFILT	27
B88	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_PLLFILT	27

PP1V5_*

	Physical	Spacing	Voltage	Netname	
B89	POWER_PHY	POWER	1.5V	PP1V5_S0_DP_BIAS	84

PP1V8_*

	Physical	Spacing	Voltage	Netname	
B90	POWER_PHY	POWER	1.8V	PP1V8_S0_PCH_VCCVRM_F	22 24

PP3V3R1V8_*

	Physical	Spacing	Netname	
B92	POWER_PHY	POWER	PP3V3R1V8_ENET_LR_OUT_REG	39

PP3V3RHV_*

	Physical	Spacing	Voltage	Netname	
B93	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTAPWR	86
B94	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTBPWR	88

PP3V3_*

	Physical	Spacing	Voltage	Netname	
B95	POWER_PHY	POWER	3.3V	PP3V3_DMIC_CONN	42
B96	POWER_PHY	POWER	3.3V	PP3V3_G3H_AVREF_SMC	47 48
B97	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FET	35
B98	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FLT	35
B99	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_USBMUX_R	45
B100	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_VDDA	47
B101	POWER_PHY	POWER	3.3V	PP3V3_G3_RTC	6 26
B102	POWER_PHY	POWER	3.3V	PP3V3_GPU_IFPX_PLLVDD	81
B103	POWER_PHY	POWER	3.3V	PP3V3_PVDDQS3_ISNS	51
B104	POWER_PHY	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	17 22
B105	POWER_PHY	POWER	3.3V	PP3V3_S0_SSD_FLT	44
B106	POWER_PHY	POWER	3.3V	PP3V3_S0_SW_SD_PWR	41
B107	POWER_PHY	POWER	3.3V	PP3V3_S4_ALS_F	42
B108	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FET	35
B109	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FLT	35
B110	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_AVDDH	39
B111	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_BIASVDDH	39
B112	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_SRVDD	39
B113	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_XTALVDDH	39
B114	POWER_PHY	POWER	3.3V	PP3V3_S4_USB_HUB_VDD	27
B115	POWER_PHY	POWER	3.3V	PP3V3_S5_XDP_R	25

PP4V5_*

	Physical	Spacing	Voltage	Netname	
B116	POWER_PHY	POWER	4.5V	PP4V5_AUDIO_ANALOG	56 60 62

PP5V_*

	Physical	Spacing	Voltage	Netname	
B117	POWER_PHY	POWER	5V	PP5V_AUDIO_HPAMP	56 57
B118	POWER_PHY	POWER	5V	PP5V_S0_HDD_FET	44 52
B119	POWER_PHY	POWER	5V	PP5V_S0_PCH_V5REF	24
B120	POWER_PHY	POWER	5V	PP5V_S4_EXTA	45
B121	POWER_PHY	POWER	5V	PP5V_S4_EXTA_F	45
B122	POWER_PHY	POWER	5V	PP5V_S4_EXTB	45
B123	POWER_PHY	POWER	5V	PP5V_S4_EXTB_F	45
B124	POWER_PHY	POWER	5V	PP5V_S4_EXTC	46
B125	POWER_PHY	POWER	5V	PP5V_S4_EXTC_F	46
B126	POWER_PHY	POWER	5V	PP5V_S4_EXTD	46
B127	POWER_PHY	POWER	5V	PP5V_S4_EXTD_F	46
B128	POWER_PHY	POWER	5V	PP5V_S5_PCH_V5REFSUS	24

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PPHV_*

	Physical	Spacing	Voltage	Netname
E8	POWER_PHY	POWER	12V	PPHV_SW_TBTAPWR 86
E9	POWER_PHY	POWER	12V	PPHV_SW_TBTBPWR 88

PPVBATT_*

	Physical	Spacing	Voltage	Netname
E6	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC 26
E7	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC_R 26

PU_*

	Spacing	Netname
E6	GENERIC_ISO	PU_U6900 64

PWR_*

	Spacing	Netname
E6	PM	PWR_BTN 6 48
E7	PM	PWR_BTN_R 6

REG_*

	Physical	Spacing	Netname
E8		PM	REG_CPUAXG_PGOOD 5 66
E9		PM	REG_CPUCORE_PGOOD 66
E10	CPU_PHY	CPU	REG_CPUCORE_VRHOT_L 66
E11		PM	REG_CPU_P1V05S0_PGOOD 69
E12	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET0 95
E13	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1 95
E14	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1_R 95
E15	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SREF 95
E16		PM	REG_P1V8S0_PGOOD 72
E17		PM	REG_P3V3S5_PGOOD 71
E18		PM	REG_P5VS4_PGOOD 71
E19		PM	REG_VCCSAS0_PGOOD 70
E20		PM	REG_VDDQS3_PGOOD 72

RTC_*

	Spacing	Netname
E21	PM	RTC_RESET_L 18 26 48
E22	PM	RTC_RESET_L_R 48

S5_*

	Spacing	Netname
F23	PM	S5_PWRGD 47 65

SATALED_*

	Spacing	Netname
F24	GENERIC_ISO	SATALED_L 44

SDCONN_*

	Spacing	Netname
F25	GENERIC_ISO	SDCONN_DETECT 41
F26	GENERIC_ISO	SDCONN_ILIM 41
F27	GENERIC_ISO	SDCONN_OC_L 41

SD_*

	Spacing	Netname
F28	GENERIC_ISO	SD_DETECT_LVL 41

SLG_*

	Spacing	Netname
F29	PM	SLG_ENET_RESET_L 41
F30	PM	SLG_ENET_RESET_R_L 41

SMBUS_*

	Physical	Spacing	Netname
F31	SMB_PHY	SMB	SMBUS_PCH_CLK 18 50
F32	SMB_PHY	SMB	SMBUS_PCH_CLK_R 50
F33	SMB_PHY	SMB	SMBUS_PCH_DATA 18 50
F34	SMB_PHY	SMB	SMBUS_PCH_DATA_R 50
F35	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL 47 50
F36	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA 47 50
F37	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL 47 50
F38	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA 47 50
F39	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL 47 50
F40	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA 47 50
F41	SMB_PHY	SMB	SMBUS_SMC_3_SCL 47 50
F42	SMB_PHY	SMB	SMBUS_SMC_3_SDA 47 50
F43	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL 47 48 50
F44	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA 47 48 50
F45	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL 47 48 50
F46	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA 47 48 50

SMCISNS_*

	Physical	Spacing	Netname
F47	SNS_PHY	SENSE	SMCISNS_CPUAXG 48 51
F48	SNS_PHY	SENSE	SMCISNS_CPUCORE 48 51
F49	SNS_PHY	SENSE	SMCISNS_GPUCORE 48 51
F50	SNS_PHY	SENSE	SMCISNS_P12VG3H 48 51
F51	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_P1V05 48 55
F52	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_VCCSA 48 55
F53	SNS_PHY	SENSE	SMCISNS_P12VS0_FBVDDQ 48 51
F54	SNS_PHY	SENSE	SMCISNS_P12VS0_HDD 48 51
F55	SNS_PHY	SENSE	SMCISNS_P12VS0_P1V05 48 55
F56	SNS_PHY	SENSE	SMCISNS_P1V05S0_PCH 48 51
F57	SNS_PHY	SENSE	SMCISNS_P1V5S0_CPU_MEM 48 51
F58	SNS_PHY	SENSE	SMCISNS_P3V3S0_SSD 48 51
F59	SNS_PHY	SENSE	SMCISNS_P3V3S4_AP 48 55
F60	SNS_PHY	SENSE	SMCISNS_P5VS0_HDD 48 51
F61	SNS_PHY	SENSE	SMCISNS_PVDDQS3_DDR 48 51

SMCVSNS_*

	Physical	Spacing	Netname
F62	SNS_PHY	SENSE	SMCVSNS_CPUAXG 48 51
F63	SNS_PHY	SENSE	SMCVSNS_CPUCORE 48 51
F64	SNS_PHY	SENSE	SMCVSNS_GPUCORE 48 51
F65	SNS_PHY	SENSE	SMCVSNS_P12VG3H 48 51
F66	SNS_PHY	SENSE	SMCVSNS_P1V05S0_PCH 48 51
F67	SNS_PHY	SENSE	SMCVSNS_P1V5S0_CPU_MEM 48 51
F68	SNS_PHY	SENSE	SMCVSNS_P3V3S0 48 51
F69	SNS_PHY	SENSE	SMCVSNS_P5VS0_HDD 48 51
F70	SNS_PHY	SENSE	SMCVSNS_PVDDQS3_DDR 48 51

SMC_*

	Physical	Spacing	Netname
F71		GENERIC_ISO	SMC_ACDC_ID 6 48
F72		GENERIC_ISO	SMC_ACDC_ID_R 6
F73		PM	SMC_ASSERT_RTCRST 48
F74		GENERIC_ISO	SMC_BLC_MUX_RX_L 48 89
F75		GENERIC_ISO	SMC_BLC_MUX_TX_L 48 89
F76		GENERIC_ISO	SMC_CPU_CATERR_L 47 48
F77	CPU_PHY	CPU	SMC_CPU_PECI 48
F78		PM	SMC_DELAYED_PWRGD 38 47 48 65
F79		GENERIC_ISO	SMC_DP_HPD_L 47 48
F80	CLK_XTAL	XTAL	SMC_EXTAL 47 48
F81		GENERIC_ISO	SMC_FAN_0_CTL 47 54
F82		GENERIC_ISO	SMC_FAN_0_TACH 47 54
F83		GENERIC_ISO	SMC_GFX_OVERTEMP 47 48 82
F84		GENERIC_ISO	SMC_GFX_OVERTEMP_Q 82
F85		GENERIC_ISO	SMC_GFX_OVERTEMP_R_L 82
F86		PM	SMC_GFX_THROTTLE_L 47 82
F87		PM	SMC_GFX_THROTTLE_R_L 82
F88		PM	SMC_LRESET_L 26 47
F89		PM	SMC_MANUAL_RST_L 48
F90		PM	SMC_ONOFF_L 47 48
F91		SENSE	SMC_OOB1_RX_CN 44
F92		SENSE	SMC_OOB1_RX_FILT 44 52
F93		SENSE	SMC_OOB1_RX_L 47 52
F94		SENSE	SMC_OOB1_RX_R 52
F95		SENSE	SMC_OOB1_TX_L 47 48
F96		SENSE	SMC_OOB2_RX_L 44 48
F97		SENSE	SMC_OOB2_TX_L 44 48
F98	CPU_PHY	CPU	SMC_PECI_L 47 48
F99	CPU_PHY	CPU	SMC_PECI_L_R 48
F100		PM	SMC_PME_S4_WAKE_L 35 47 48
F101		GENERIC_ISO	SMC_PM_G2_EN 47 48 74
F102		PM	SMC_PM_PCH_SYS_PWROK 47 48
F103		CPU	SMC_PROCHOT 47 48
F104		PM	SMC_RESET_L 47 48 49

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SMC_*

	Physical	Spacing	Netname	
A1		GENERIC_ISO	SMC_ROMBOOT	48 49
A2		GENERIC_ISO	SMC_RUNTIME_SCI_L	15 21 47
A3		GENERIC_ISO	SMC_RX_L	47 48 49
A4		PM	SMC_S4_WAKESRC_EN	35 47 48
A5		GENERIC_ISO	SMC_TCK	47 48 49
A6		GENERIC_ISO	SMC_TDI	47 48 49
A7		GENERIC_ISO	SMC_TDO	47 48 49
A8		PM	SMC_THRMTRIP	47 48
A9		GENERIC_ISO	SMC_TMS	47 48 49
A10		GENERIC_ISO	SMC_TO_BLC_RX_L	48
A11		GENERIC_ISO	SMC_TO_BLC_TX_L	48
A12		GENERIC_ISO	SMC_TX_L	47 48 49
A13		PM	SMC_WAKE_L	47
A14		GENERIC_ISO	SMC_WAKE_SCI_L	15 21 47
A15	CLK_XTAL	XTAL	SMC_XTAL	47 48
A16	CLK_XTAL	XTAL	SMC_XTAL_R	48

SML_*

	Physical	Spacing	Netname	
A17	SMB_PHY	SMB	SML_PCH_0_CLK	18 50
A18	SMB_PHY	SMB	SML_PCH_0_DATA	18 50
A19	SMB_PHY	SMB	SML_PCH_1_CLK	18 50
A20	SMB_PHY	SMB	SML_PCH_1_DATA	18 50

SPI_*

	Spacing	Netname	
A21	GENERIC_ISO	SPI_DESCRIPTOR_OVERRIDE_L	15 47

SSD_*

	Spacing	Netname	
B22	GENERIC_ISO	SSD_CLKREQ_L	15 18

SYS_*

	Spacing	Netname	
B23	PM	SYS_PWROK_R	65

TBT_*

	Physical	Spacing	Voltage	Netname	
B24		GENERIC_ISO	3.3V	TBT_A_BIAS	86
B25	TBT_GEN_55S	TBT_GEN		TBT_A_CONFIG1_RC	86
B26		PM		TBT_A_HV_EN	36 86
B27		GENERIC_ISO	3.3V	TBT_B_BIAS	88
B28	TBT_GEN_55S	TBT_GEN		TBT_B_CONFIG1_RC	88
B29		PM		TBT_B_HV_EN	36 88
B30		GENERIC_ISO		TBT_CLKREQ_ISOL_L	38
B31		GENERIC_ISO		TBT_CLKREQ_L	15 38
B32		GENERIC_ISO		TBT_DDC_XBAR_EN_L	36 85
B33		GENERIC_ISO		TBT_EN_CIO_PWR	38
B34		PM		TBT_EN_CIO_PWR_L	36 38
B35		GENERIC_ISO		TBT_EN_LC_ISOL	38
B36		GENERIC_ISO		TBT_EN_LC_PWR	36 38
B37		GENERIC_ISO		TBT_PCH_CLKREQ_L	15 21
B38		PM		TBT_PWR_EN	15 26 36
B39		PM		TBT_PWR_EN_PCH	18 26
B40		PM		TBT_PWR_ON_POC_RST_L	36 38
B41		PM		TBT_PWR_REQ_L	15 20 36
B42		PM		TBT_S0_EN	64
B43		PM		TBT_SW_RESET_L	21 38

TSNS_*

	Electrical	Physical	Spacing	Netname	
B44	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_N	53
B45	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_P	53
B46	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_N	53
B47	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_P	53
B48	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_N	53
B49	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_P	53
B50	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_N	53
B51	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_P	53
B52	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_N	53
B53	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_P	53
B54	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_N	53
B55	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_P	53
B56	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_N	53
B57	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_P	53
B58	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_N	53
B59	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_P	53
B60	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_N	53
B61	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_P	53
B62	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_N	53
B63	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_P	53
B64	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_N	6 53
B65	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_P	6 53
B66	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_N	53
B67	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_P	53

UVP_*

	Spacing	Netname	
B68	PM	UVP_IN_1	91
B69	PM	UVP_IN_1_REF	91
B70	PM	UVP_IN_2	91
B71	PM	UVP_IN_3	91
B72	PM	UVP_IN_4	91
B73	PM	UVP_REF	91

VREFMRGN_*

	Spacing	Netname	
B74	GENERIC_ISO	VREFMRGN_CA_SODIMMA_EN	34
B75	GENERIC_ISO	VREFMRGN_CA_SODIMMB_EN	34

VTTCLAMP_*

	Spacing	Netname	
B76	GENERIC_ISO	VTTCLAMP_EN	28
B77	GENERIC_ISO	VTTCLAMP_L	28

WOL_*

	Spacing	Netname	
B78	GENERIC_ISO	WOL_EN	15 21 40

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