1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K62 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-02-08

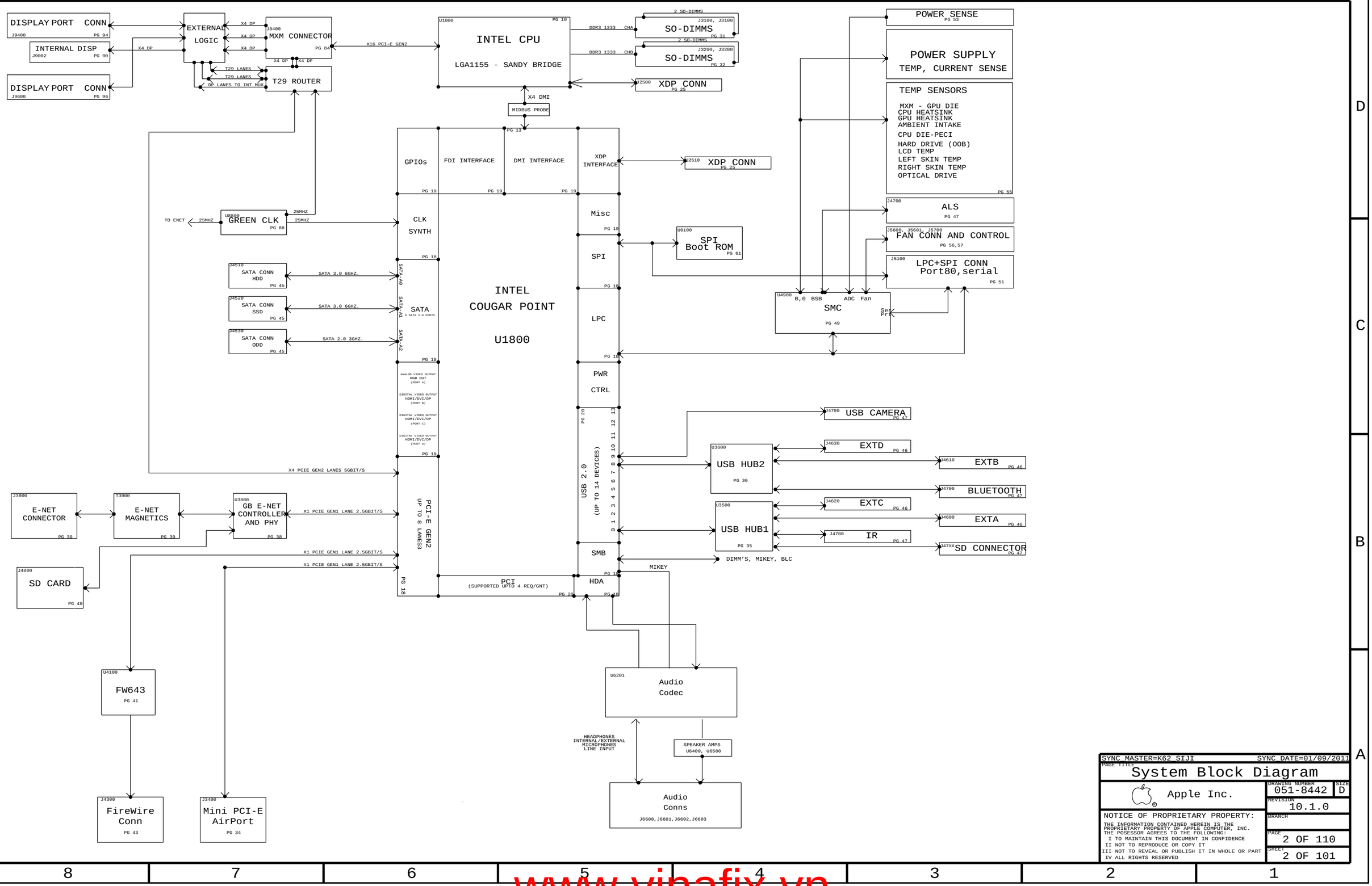
LAST_MODIFIED=Tue Feb 8 15:20:30 2011

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Tue Feb 8 15:20:30 2011

DRAWING TITLE: SCH,K62,MLB

Apple Inc.

DRAWING NUMBER: 051-8442 | SIZE: D
REVISION: 10.1.0
BRANCH:
PAGE: 1 OF 110
SHEET: 1 OF 101



SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE: System Block Diagram

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

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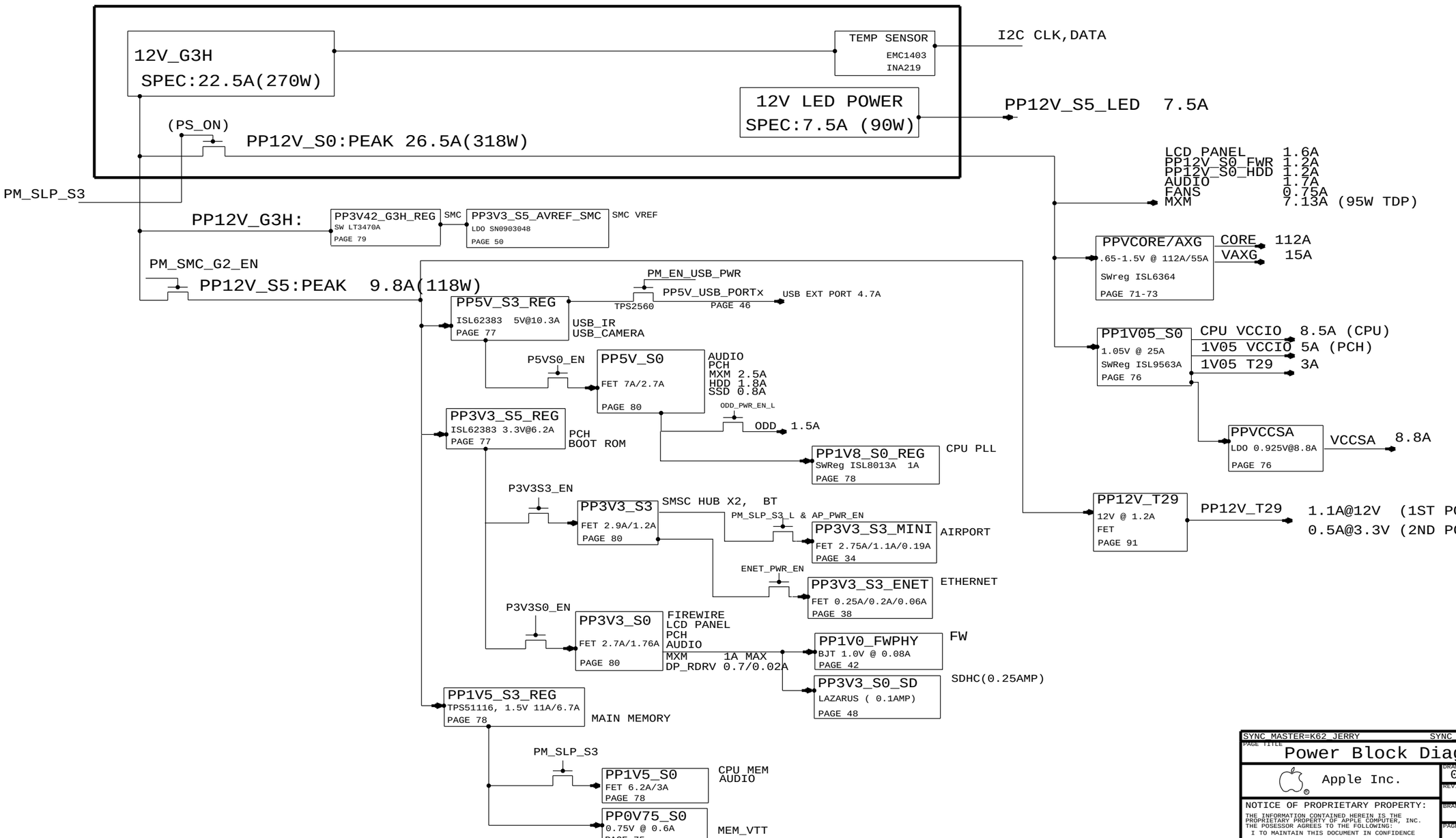
K75F AC/DC POWER SUPPLY (SPEC:310W)



SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

PAGE TITLE: Power Block Diagram

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1226	PCBA,MLB,DEV,K62	DEVELOPMENT,DEV_GROUP
639-1769	PCBA,MLB,K62,2.8G,4C,PRQ,P2_ODD	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG
639-1770	PCBA,MLB,K62,3.1G,4C,PRQ,P2_ODD	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG
639-1771	PCBA,MLB,K62,3.4G,4C,PRQ,P2_ODD	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,YES_DBG
639-2186	PCBA,MLB,K62,2.8G,4C,PRQ,P2_ODD,NO_DBG	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG
639-2187	PCBA,MLB,K62,3.1G,4C,PRQ,P2_ODD,NO_DBG	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG
639-2188	PCBA,MLB,K62,3.4G,4C,PRQ,P2_ODD,NO_DBG	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P2,NO_DBG
639-2124	PCBA,MLB,K62,2.8G,4C,PRQ,P1_ODD	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG
639-2121	PCBA,MLB,K62,3.1G,4C,PRQ,P1_ODD	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG
639-2123	PCBA,MLB,K62,3.4G,4C,PRQ,P1_ODD	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,YES_DBG
639-2129	PCBA,MLB,K62,2.8G,4C,PRQ,P1_ODD,NO_DBG	K62,2P8GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG
639-2131	PCBA,MLB,K62,3.1G,4C,PRQ,P1_ODD,NO_DBG	K62,3P1GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG
639-2130	PCBA,MLB,K62,3.4G,4C,PRQ,P1_ODD,NO_DBG	K62,3P4GHZ_SNB_CPU,BASIC1,BASIC2,CPUVCORE-4PH,ODD_SATA:P1,NO_DBG

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC1	COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE
BASIC2	HUB_USX2061,AP,BT,IR,T29,VAXG,PRODUCTION
DEV_GROUP	VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE
YES_DBG	XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES
NO_DBG	MOJOMUX:NO,LPCPLUS:NO

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0071	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	TYCO_SOCKET
604-1474	1	ASSY,PURCHASED,ILM,TYCO	ILM	CRITICAL	TYCO_SOCKET
511S0073	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX	ILM	CRITICAL	MOLEX_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2451	SUB ASSY,CPU SOCKET,K62,TYCO	TYCO_SOCKET
085-2450	SUB ASSY,CPU SOCKET,K62,MOLEX	MOLEX_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-2451	1	TYCO CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-2450	085-2451		SKT_ILM	MOLEX ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S4088	1	IC,COUGAR POINT,SLJ4F,BD82Z68,PRQ,B3	U1800	CRITICAL	
	353S3055	2	IC,PI3VEDP212,X2 DP MUX,QFN	U9390,U9590	CRITICAL	
	338S0753	1	IC,FW643,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
	343S0534	1	IC,BCM57765,ENET&SD,8X8	U3900	CRITICAL	
RAW: 335S0807	341T0184	1	FLASH,EFI BOOTROM,K60/K62	U6100	CRITICAL	
RAW: 335S0539	341T0328	1	SFLASH ENET 2MBIT,CIV	U3990	CRITICAL	
	338S0945	1	T29 ROUTER, IC, ASSP	U9700	CRITICAL	T29
RAW: 335S0550	341T0329	1	IC,T29 SERIAL EEPROM	U9790	CRITICAL	T29
RAW: 337S3997	341T0327	2	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330,U9530	CRITICAL	T29
RAW: 338S0878	341T0186	1	IC,SMC,K62	U4900	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4042	1	SNB,SR00D,PRQ,D2,2.8,95W,4+1,6M,LGA	CPU	CRITICAL	2P8GHZ_SNB_CPU
337S4040	1	SNB,SR00Q,PRQ,D2,3.1,95W,4+1,6M,LGA	CPU	CRITICAL	3P1GHZ_SNB_CPU
337S4041	1	SNB,SR00B,PRQ,D2,3.4,95W,4+1,8M,LGA	CPU	CRITICAL	3P4GHZ_SNB_CPU

K62 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8442	1	SCH,MLB,K62	SCH1		K62
820-2828	1	PCBF,MLB,K62	MLB1		K62

K62 ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293		ALL	330UF
371S0679	371S0652		ALL	PIN DIODE
377S0107	377S0066		ALL	USB DIODE
376S0972	376S0612		ALL	ROHM TRA-BJT

SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

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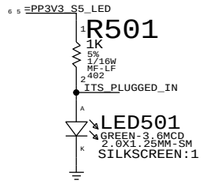
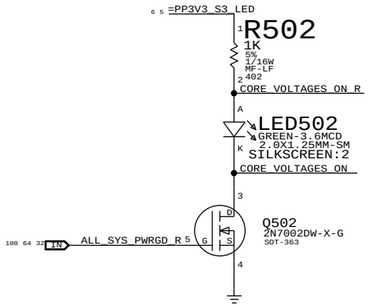
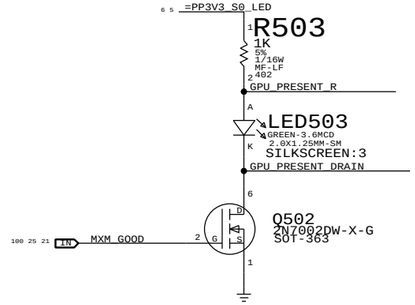
S5 Led



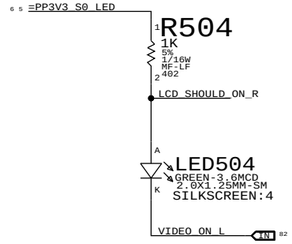
ALL_SYS_PWRGD Led



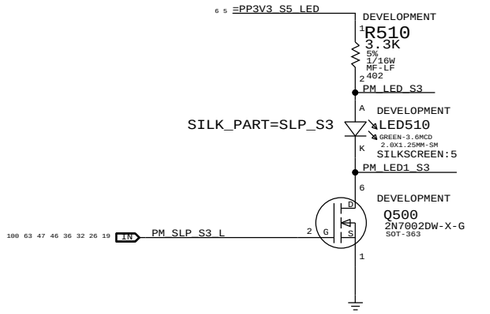
MXM PWR GOOD Led

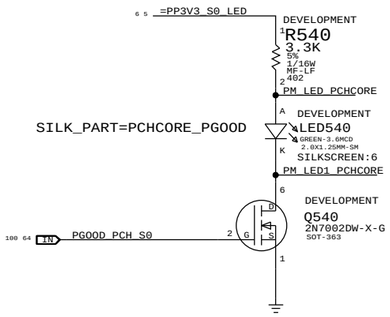


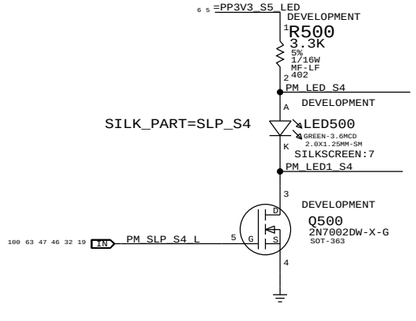
VIDEO ON Led

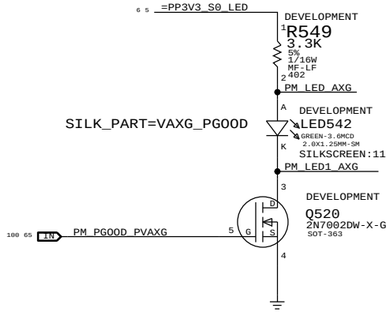


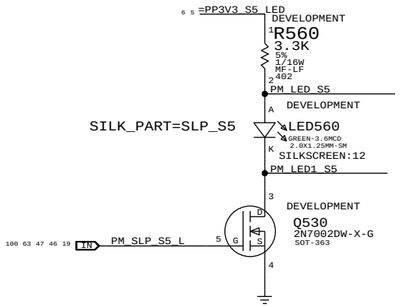
PROTO DEBUG LEDS ARE SHOWN BELOW

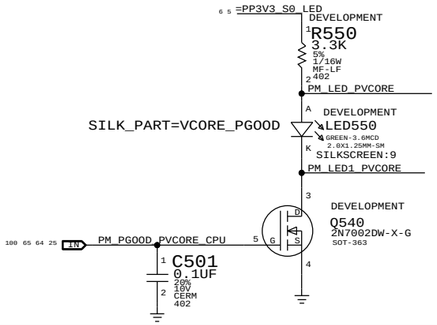


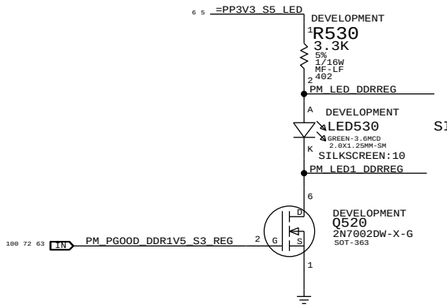


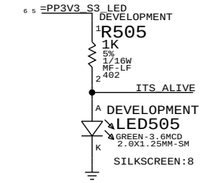












SYNC_MASTER=K62_AARON SYNC_DATE=07/01/2009

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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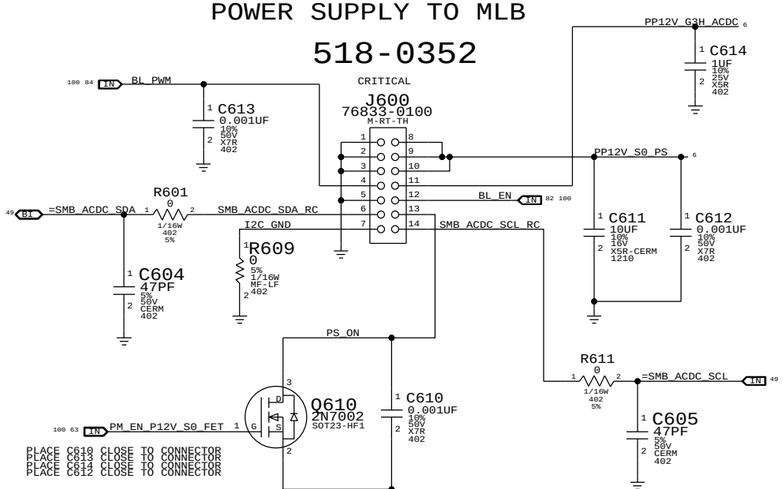
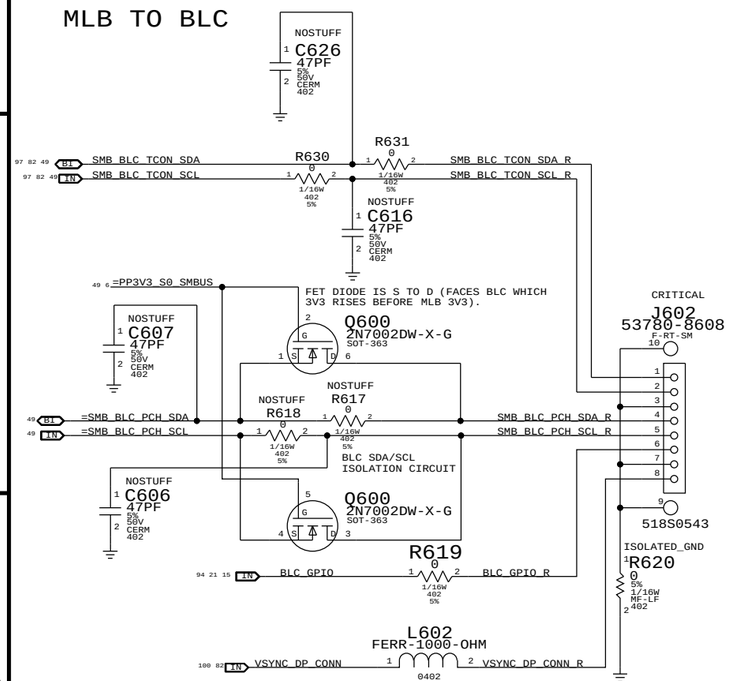
POWER SUPPLY TO MLB

518-0352



MLB TO BLC



"S0" RAILS

ONLY ON IN RUN

- PP0V75_S0 (MAKE_BASE=TRUE; VOLTAGE=0.75V; MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PPVTT_S0_DDR_LDO 72
  - =PP0V75_S0_MEM_VTT_S0FET 32
- PPVTT_S0_DDR (MAKE_BASE=TRUE; VOLTAGE=0.75V; MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PPVTT_S0_DDR_FET 32
  - =PP0V75_S0_MEM_VTT_B 31
  - =PP0V75_S0_MEM_VTT_A 30
- PPVCORE_S0_CPU (MAKE_BASE=TRUE; VOLTAGE=1.1V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.3MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PPVCORE_S0_CPU_REG 66 67
  - =PPVCORE_S0_CPU 13 16 50 65
- PPVAXG_S0 (MAKE_BASE=TRUE; VOLTAGE=1.05V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.3MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PPVAXG_S0_REG 67
  - =PPVAXG_S0_CPU 13 17 50 65
- PP1V05_S0 (MAKE_BASE=TRUE; VOLTAGE=1.05V; MIN_LINE_WIDTH=0.5MM; MIN_NECK_WIDTH=0.25MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V05_S0_REG 68
  - =PP1V05_S0_PWR 50
  - =PPVCCIO_S0_XDP 25
  - =PPVCCIO_S0_CPU 10 11 13 16 65
  - =PPVCCIO_S0_SMC 46 47
  - =PP1V05_S0_PCH_PWR 50
  - =PPVCCSA_S0_INPUT_PWR 50 69
  - =PP1V05_S0_CK505 26
- PP1V05_S0_PCH (MAKE_BASE=TRUE; VOLTAGE=1.05V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V05_S0_PCH_SNS 50
  - =PP1V05_S0_PCH_VCC_DMI 22 24
  - =PP1V05_S0_PCH_VCCADPLL 17
  - =PP1V05_S0_PCH_VCCIO_DMI 22 24
  - =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
  - =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
  - =PP1V05_S0_PCH_VCC_CORE 22 24
  - =PP1V05_S0_PCH_VCCIO_USB 22 24
  - =PP1V05_S0_PCH 18 24 80
  - =PP1V05_S0_PCH_VCCDIFFCLK 22 24
  - =PP1V05_S0_PCH_VCCSSC 22 24
  - =PP1V05_S0_PCH_V_PROC_IO 22 24
  - =PP1V05_S0_PCH_VCCASW 22 24
  - =PP1V05_S0_P1V05T29FET 81
- PP1V05_S0_INPUT_VCCSA (MAKE_BASE=TRUE; VOLTAGE=1.05V; MIN_LINE_WIDTH=0.5MM; MIN_NECK_WIDTH=0.25MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PPVCCSA_S0_INPUT_SNS 50
  - =PPVCCIO_S0_CPU_VCCSA 69
- PPVCCSA_S0_CPU (MAKE_BASE=TRUE; VOLTAGE=0.925V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.3MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PPVCCSA_S0_FET 69
  - =PPVCCSA_S0_CPU 13 50
  - =PPVCCSA_S0_PWRCTL 64
- PP1V5_S0 (MAKE_BASE=TRUE; VOLTAGE=1.5V; MIN_LINE_WIDTH=0.4MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V5_S0_FET 74
  - =PP1V5_S0_AUD_DIG 56
  - =PP1V5_S0_CK505 26
  - =PP1V5_S0_MINI 33
  - =PP1V5_S0_PWR 50
  - =PP1V5_S0_DP 84
- PP1V5_S0_CPU_MEM (MAKE_BASE=TRUE; VOLTAGE=1.5V; MIN_LINE_WIDTH=0.4MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V5_S0_CPU_MEM_SNS 50
  - =PP1V5_S0_CPU_MEM 11 13 16 28 29
- PP3V3_S0 (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.4MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP3V3_S0_FET 74
  - =PP3V3_S0_PCH 18 21 24
  - =PP3V3_S0_FAN 53 54
  - =PP3V3_S0_PCH_VCCADAC 17
  - =PPSPD_S0_MEM_A 30 47
  - =PPSPD_S0_MEM_B 31
  - =PP3V3_S0_AUDIO 56 58 59 60 61 62
  - =PP3V3R1V5_S0_PCH_VCCSUSHDA 24
  - =PP3V3_S0_SMBUS 6 49
  - =PP3V3_S0_SMC_LS 47 51
  - =PP3V3_S0_SMBUS_SMC_0 49
  - =PP3V3_S0_SMBUS_SMC_B 49
  - =PP3V3_S0_SMBUS_SMC_MGMT 49
  - =PP3V3_S0_MXM 21 64 76 77
  - =PP3V3_S0_ODD 42
  - =PP3V3_S0_SATALED 18 42
  - =PP3V3_S0_SENSE 50 52
  - =PP3V3_S0_PWRCTL 63 64 74 81
  - =PP3V3_S0_PCH_VCC3_3_GPIO 22 24
  - =PP3V3_S0_FWPHY 39 40 41
  - =PP3V3_S0_DP 82
  - =PP3V3_S0_PCH_VCC3_3_PCI 22 24
  - =PP3V3_S0_CK505 26
  - =PP3V3_S0_PCH_GPIO 20 45
  - =PP3V3_S0_PCH_STRAPS 15
  - =PP3V3_S0_PCH_VCC3_3_SATA 22 24
  - =PP3V3_S0_RSTBUF 11 27
  - =PP3V3_S0_PCH_PM 27
  - =PP3V3_S0_SMBUS_SMC_BSA 49
  - =PP3V3_S0_SDCARD 45
  - =PP3V3_S0_P1V05_VREG 68
  - =PP3V3_S0_PCH_VCC3V3 22 24
  - =PP3V3_S0_VRD 65 68
  - =PP3V3_S0_LED 5
  - =PP3V3_S0_P3V3T29FET 81
  - =PP3V3_S0_DPSDRVA 85
  - =PP3V3_S0_DPSDRVB 87
  - =PP3V3_S0_INTDPMUX 84
  - =PP3V3_S0_T29PWRCTL 81
  - =PP3V3_S0_T29I2C 49
  - =PP3V3_S0_ENET_PHY 36 37
- PP1V8_S0 (MAKE_BASE=TRUE; VOLTAGE=1.8V; MIN_LINE_WIDTH=0.5MM; MIN_NECK_WIDTH=0.25MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V8_S0_REG 72
  - =PP3V3R1V8_S0_PCH_VCCDFTERM 22 24
  - =PP1V8R1V5_S0_PCH_VCCVRM 24 80
  - =PP1V8_S0_CPU_PLL 13 16
  - =PP1V8_S0_PCH 19
  - =PP1V8_S0_PWRCTL 64
- PP5V_S0 (MAKE_BASE=TRUE; VOLTAGE=5V; MIN_LINE_WIDTH=0.5 mm; MIN_NECK_WIDTH=0.2 MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP5V_S0_FET 74
  - =PP5V_S0_AUDIO 56
  - =PP5V_S0_SATA 42
  - =PP5V_S0_MXM 76
  - =PP5V_S0_VRD 65 67
  - =PP5V_S0_ISENSE 50
  - =PP5V_S0_PCH 24
  - =PP5V_S0_P1V05_VREG 68
  - =PP5V_S0_LPCPLUS 48
  - =PP5V_S0_P1V8_REG 72
- PP12V_S0 (MAKE_BASE=TRUE; VOLTAGE=12V; MIN_LINE_WIDTH=1mm; MIN_NECK_WIDTH=0.5mm; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP12V_S0_PS 6
  - =PP12V_S0_AUDIO_SPKRAMP 58 59
  - =PP12V_S0_VRD 65
  - =PP12V_S0_MXM_PWR 50
  - =PP12V_S0_LCD 82
  - =PP12V_S0_P1V05_VREG 68
  - =PP12V_S0_PWRCTL 63 64 81
  - =PP12V_S0_SENSE 51
  - =PP12V_S0_FW 41
  - =PP12V_S0_CPU_VCCSA 69
  - =PP12V_S0_SATA 42
  - =PP12V_S0_FAN 53 54
- PP12V_S0_MXM (MAKE_BASE=TRUE; VOLTAGE=12V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP12V_S0_MXM_SNS 50
  - =PP12V_S0_MXM 76

"S3" RAILS

ON IN RUN AND SLEEP

- PP1V5_S3 (MAKE_BASE=TRUE; VOLTAGE=1.5V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V5_S3_REG 72
  - =PP1V5_S3_MEM_PWR 50
  - =PP1V5_S3_S0FET 74
- PP1V5_S3_MEM (MAKE_BASE=TRUE; VOLTAGE=1.5V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V5_S3_MEM_SNS 50
  - =PP1V5_S3_MEMRESET 32
  - =PP1V5_S3_MEM_A 28 29 30
  - =PP1V5_S3_MEM_B 28 29 31
- PP3V3_S3 (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.4MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP3V3_S3_FET 74
  - =PP3V3_S3_BT 44
  - =PP3V3_S3_SMBUS_SMC_A 49
  - =PP3V3_S3_MINI 33
  - =PP3V3_S3_PWRCTL 64 74 83
  - =PP3V3_S3_MEMRESET 32
  - =PP3V3_S3_USB_HUB 34 35
  - =PP3V3_S3_ENET_PHY 36
  - =PP3V3_S3_SDCARD 44 45
  - =PP3V3_S3_VREFMRGN 28
  - =PP3V3_S3_VRD 72
  - =PP3V3_S3_LED 5
  - =PP3V3_SW_DPAPWR 79
  - =PP3V3_SW_DPBPWR 79
  - =PP3V3_S3_SYSCLK 80
  - =PP3V3_S3_P3V3R2V9_REG_A 83
  - =PP3V3_S3_P3V3R2V9_REG_B 83
  - =PP3V3_S3_PCH 21
- PP5V_S3 (MAKE_BASE=TRUE; VOLTAGE=5V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP5V_S3_REG 71
  - =PP5V_S3_USB 43
  - =PP5V_S3_S0FET 74
  - =PP5V_S3_CAMERA 44
  - =PP5V_S3_IR 44
  - =PP5V_S3_MEMRESET 32
  - =PP5V_S3_DDR_VREG 72
  - =PP5V_S3_VREFMRGN 28
  - =PP5V_S3_P3V3R2V9_REG_A 83
  - =PP5V_S3_P3V3R2V9_REG_B 83

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

- PP3V3_S5 (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.4MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP3V3_S5_REG 71
  - =PP3V3_S5_PCH 18 19 21 24
  - =PP3V3_S5_PCH_GPIO 20
  - =PP3V3_S5_ROM 48 55
  - =PP3V3_S5_PCH_VCCSUS3_3_USB 22 24
  - =PP3V3_S5_PWRCTL 11 63 64
  - =PP3V3_S5_S3FET 74
  - =PP3V3_S5_S0FET 74
  - =PP3V3_S5_PCH_STRAPS 15
  - =PP3V3_S5_XDP 25
  - =PP3V3_S5_LPCPLUS 48
  - =PP3V3_S5_PCH_VCCDSW 22 24
  - =PP3V3_S5_USB_HUB 34
  - =PP3V3_S5_CPU_VCCSA 69
  - =PP3V3_S5_PCH_VCCSPI 22 24
  - =PP3V3_S5_VRD 71
  - =PP3V3_S5_LED 5
  - =PP3V3_S5_MEMRESET 32
  - =PP3V3_S5_RSTBUF 27
  - =PP3V3_S5_SMCUSBMUX 43
  - =PP3V3_S5_P3V3R2V9_A 83
  - =PP3V3_S5_P3V3R2V9_B 83
  - =PP3V3R1V5_S5_PCH_VCCSUSHDA 24
- PP5V_S5 (MAKE_BASE=TRUE; VOLTAGE=5V; MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP5V_S5_LDO 71
  - =PP5V_S5_PCH 24
- PP12V_S5 (MAKE_BASE=TRUE; VOLTAGE=12V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP12V_S5_FET 75 98
  - =PP12V_S5_DDR_VREG 72
  - =PP12V_S5_P5VS3_VREG 71
  - =PP12V_S5_PWRCTL 33 64 74
  - =PP12V_S5_T29_A 83
  - =PP12V_S5_T29_B 83

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

- PP3V42_G3H (MAKE_BASE=TRUE; VOLTAGE=3.42V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP3V42_G3H_REG 73
  - =PP3V3_G3H_RTC_D 27
  - =PP3V3_G3H_SMC 46 47
  - =PP3V3_G3H_SMCUSBMUX 43
  - =PP3V3_G3H_LPCPLUS 48
- PP12V_G3H (MAKE_BASE=TRUE; VOLTAGE=12V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP12V_G3H_ACDC 6
  - =PP12V_G3H_S5_FET 75
  - =PP12V_G3H_3V42 73

T29 RAILS

- PP3V3_S0_T29 (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP3V3_T29_FET 81
  - =PP3V3_T29_RTR 80 81 89 90
- PP1V05_S0_T29 (MAKE_BASE=TRUE; VOLTAGE=1.05V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.2MM; NET_SPACING_TYPE=POWER; MAX_NECK_LENGTH=3 MM)
  - PP1V05_S0_T29_FET 81
  - =PP1V05_T29_RTR 90
  - =PP1V05_T29 81

GND RAILS

- GND (MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.2MM; VOLTAGE=0V; NET_SPACING_TYPE=GND; MAKE_BASE=TRUE; MAX_NECK_LENGTH=4.1 MM)

SYNC_MASTER=K62_AARON SYNC_DATE=12/30/2010

PAGE TITLE: Power Conn / Alias

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D

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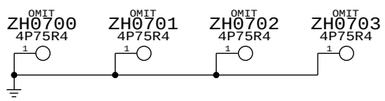
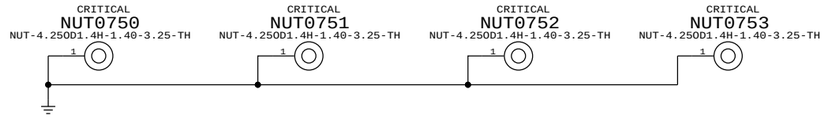
CPU Heatsink

4mm Plated Holes (998-0850)



DIMM CONNECTOR NUTS

Nuts (805-9582)



PCH HEATSINK MTG HOLES (NON-PLATED HOLE ON PCB ONLY)

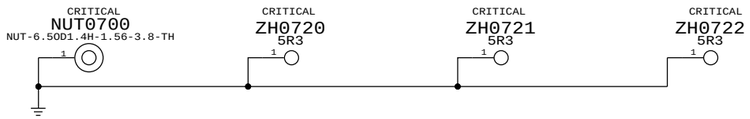
Rear Cover

STANDOFFS (WAS 860-1255 BUT NOW REPLACED WITH 860-1430)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	6	STANDOFF,MLB,K60/K62	SDF0713,SDF0714,SDF0715,SDF0717,SDF0718,SDF0719	COMMON

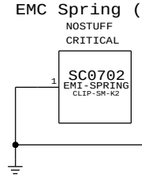
Backer Plate

Nuts (835-0269)

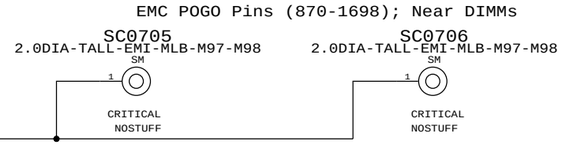


For EMC

EMC Spring (870-1577); Near DIMMs



EMC POGO Pins (870-1698); Near DIMMs



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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UNUSED CPU SIGNALS

10 TP_CPU_RSVD<16..1>	=	NC_CPU_RSVD<16..1>
10 TP_CPU_RSVD<46..19>	=	NC_CPU_RSVD<46..19>

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20 TP_PCI_AD<31..0>	=	NC_PCI_AD<31..0>
20 TP_PCI_C_BE_L<3..0>	=	NC_PCI_C_BE_L<3..0>
20 TP_PCI_PAR	=	NC_PCI_PAR
20 TP_PCI_RESET_L	=	NC_PCI_RESET_L

MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_LPC_DREQ0_L	=	NC_LPC_DREQ0_L

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12 TP_MEM_A_DQ_CB<7..0>	=	NC_MEM_A_DQ_CB<7..0>
12 TP_MEM_A_DQS_N<8>	=	NC_MEM_A_DQSN<8>
12 TP_MEM_A_DQS_P<8>	=	NC_MEM_A_DQSP<8>
12 TP_MEM_B_DQ_CB<7..0>	=	NC_MEM_B_DQ_CB<7..0>
12 TP_MEM_B_DQS_N<8>	=	NC_MEM_B_DQSN<8>
12 TP_MEM_B_DQS_P<8>	=	NC_MEM_B_DQSP<8>

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

18 TP_HDA_SDIN1	=	NC_HDA_SDIN1
18 TP_HDA_SDIN2	=	NC_HDA_SDIN2
18 TP_HDA_SDIN3	=	NC_HDA_SDIN3

MAKE_BASE=TRUE NO_TEST=TRUE

21 TP_PCH_PWM0	=	NC_PCH_PWM0
21 TP_PCH_PWM1	=	NC_PCH_PWM1
21 TP_PCH_PWM2	=	NC_PCH_PWM2
21 TP_PCH_PWM3	=	NC_PCH_PWM3
21 TP_PCH_SST	=	NC_PCH_SST

MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_CL_CLK1	=	NC_PCH_CL_CLK1
18 TP_PCH_CL_DATA1	=	NC_PCH_CL_DATA1
18 TP_PCH_CL_RST1	=	NC_PCH_CL_RST1

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

18 TP_PCIE_CLK100M_PE5P	=	NC_PCIE_CLK100M_PE5P
18 TP_PCIE_CLK100M_PE5N	=	NC_PCIE_CLK100M_PE5N
21 TP_PCIE_CLK100M_PE6P	=	NC_PCIE_CLK100M_PE6P
21 TP_PCIE_CLK100M_PE6N	=	NC_PCIE_CLK100M_PE6N
21 TP_PCIE_CLK100M_PE7P	=	NC_PCIE_CLK100M_PE7P
21 TP_PCIE_CLK100M_PE7N	=	NC_PCIE_CLK100M_PE7N

MAKE_BASE=TRUE NO_TEST=TRUE

10 TP_PE_RX_N<3..0>	=	NC_PE_RXN<3..0>
10 TP_PE_RX_P<3..0>	=	NC_PE_RXP<3..0>
10 TP_PE_TX_N<3..0>	=	NC_PE_TXN<3..0>
10 TP_PE_TX_P<3..0>	=	NC_PE_TXP<3..0>

MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_D2R_PERN4	=	NC_PCIE_D2R_PERN4
18 TP_PCIE_D2R_PERP4	=	NC_PCIE_D2R_PERP4
18 TP_PCIE_R2D_PETN4	=	NC_PCIE_R2D_PETN4
18 TP_PCIE_R2D_PETP4	=	NC_PCIE_R2D_PETP4

MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCIE_CLK100M_PE4P	=	NC_PCIE_CLK100M_PE4P
18 TP_PCIE_CLK100M_PE4N	=	NC_PCIE_CLK100M_PE4N

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

20 TP_USB_1N	=	NC_USB_1N
20 TP_USB_1P	=	NC_USB_1P
20 TP_USB_2N	=	NC_USB_2N
20 TP_USB_2P	=	NC_USB_2P
20 TP_USB_3N	=	NC_USB_3N
20 TP_USB_3P	=	NC_USB_3P
20 TP_USB_4N	=	NC_USB_4N
20 TP_USB_4P	=	NC_USB_4P
20 TP_USB_5N	=	NC_USB_5N
20 TP_USB_5P	=	NC_USB_5P
20 TP_USB_6N	=	NC_USB_6N
20 TP_USB_6P	=	NC_USB_6P
20 TP_USB_7N	=	NC_USB_7N
20 TP_USB_7P	=	NC_USB_7P

MAKE_BASE=TRUE NO_TEST=TRUE

20 TP_USB_10N	=	NC_USB_10N
20 TP_USB_10P	=	NC_USB_10P
20 TP_USB_11N	=	NC_USB_11N
20 TP_USB_11P	=	NC_USB_11P
20 TP_USB_12N	=	NC_USB_12N
20 TP_USB_12P	=	NC_USB_12P
20 TP_USB_13N	=	NC_USB_13N
20 TP_USB_13P	=	NC_USB_13P

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19 TP_CRT_IG_DDC_CLK	=	NC_CRT_IG_DDC_CLK
19 TP_CRT_IG_DDC_DATA	=	NC_CRT_IG_DDC_DATA
19 TP_CRT_IG_RED	=	NC_CRT_IG_RED
19 TP_CRT_IG_GREEN	=	NC_CRT_IG_GREEN
19 TP_CRT_IG_BLUE	=	NC_CRT_IG_BLUE
19 TP_CRT_IG_HSYNC	=	NC_CRT_IG_HSYNC
19 TP_CRT_IG_VSYNC	=	NC_CRT_IG_VSYNC

MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_B_MLN<3..0>	=	NC_DP_IG_B_MLN<3..0>
19 TP_DP_IG_B_MLP<3..0>	=	NC_DP_IG_B_MLP<3..0>
19 TP_DP_IG_B_AUX_N	=	NC_DP_IG_B_AUXN
19 TP_DP_IG_B_AUX_P	=	NC_DP_IG_B_AUXP
19 TP_DP_IG_B_HPD	=	NC_DP_IG_B_HPD
19 TP_DP_IG_B_DDC_CLK	=	NC_DP_IG_B_CTRL_CLK
19 TP_DP_IG_B_DDC_DATA	=	NC_DP_IG_B_CTRL_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_C_MLN<3..0>	=	NC_DP_IG_C_MLN<3..0>
19 TP_DP_IG_C_MLP<3..0>	=	NC_DP_IG_C_MLP<3..0>
19 TP_DP_IG_C_AUX_N	=	NC_DP_IG_C_AUXN
19 TP_DP_IG_C_AUX_P	=	NC_DP_IG_C_AUXP
19 TP_DP_IG_C_HPD	=	NC_DP_IG_C_HPD
19 TP_DP_IG_C_CTRL_CLK	=	NC_DP_IG_C_CTRL_CLK
19 TP_DP_IG_C_CTRL_DATA	=	NC_DP_IG_C_CTRL_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_DP_IG_D_MLN<3..0>	=	NC_DP_IG_D_MLN<3..0>
19 TP_DP_IG_D_MLP<3..0>	=	NC_DP_IG_D_MLP<3..0>
19 TP_DP_IG_D_AUXN	=	NC_DP_IG_D_AUXN
19 TP_DP_IG_D_AUXP	=	NC_DP_IG_D_AUXP
19 TP_DP_IG_D_HPD	=	NC_DP_IG_D_HPD
19 TP_DP_IG_D_CTRL_CLK	=	NC_DP_IG_D_CTRL_CLK
19 TP_DP_IG_D_CTRL_DATA	=	NC_DP_IG_D_CTRL_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

19 TP_SDVO_TVCLKINN	=	NC_SDVO_TVCLKINN
19 TP_SDVO_TVCLKINP	=	NC_SDVO_TVCLKINP
19 TP_SDVO_STALLN	=	NC_SDVO_STALLN
19 TP_SDVO_STALLP	=	NC_SDVO_STALLP
19 TP_SDVO_INTN	=	NC_SDVO_INTN
19 TP_SDVO_INTP	=	NC_SDVO_INTP

MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_L_BKLTCTL	=	NC_PCH_L_BKLTCTL
18 TP_PCH_L_BKLTEN	=	NC_PCH_L_BKLTEN
18 TP_PCH_L_VDD_EN	=	NC_PCH_L_VDD_EN

MAKE_BASE=TRUE NO_TEST=TRUE

18 TP_PCH_CLKOUT_DPN	=	NC_PCH_CLKOUT_DPN
18 TP_PCH_CLKOUT_DPP	=	NC_PCH_CLKOUT_DPP

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

10 TP_CPU_FDI_TX_N<7..0>	=	NC_CPU_FDI_TXN<7..0>
10 TP_CPU_FDI_TX_P<7..0>	=	NC_CPU_FDI_TXP<7..0>
19 TP_PCH_FDI_RX_N<7..0>	=	NC_PCH_FDI_RXN<7..0>
19 TP_PCH_FDI_RX_P<7..0>	=	NC_PCH_FDI_RXP<7..0>

MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

18 TP_SATA_D_D2RN	=	NC_SATA_D_D2RN
18 TP_SATA_D_D2RP	=	NC_SATA_D_D2RP
18 TP_SATA_D_R2D_CN	=	NC_SATA_D_R2D_CN
18 TP_SATA_D_R2D_CP	=	NC_SATA_D_R2D_CP
18 TP_SATA_E_D2RN	=	NC_SATA_E_D2RN
18 TP_SATA_E_D2RP	=	NC_SATA_E_D2RP
18 TP_SATA_E_R2D_CN	=	NC_SATA_E_R2D_CN
18 TP_SATA_E_R2D_CP	=	NC_SATA_E_R2D_CP
18 TP_SATA_F_D2RN	=	NC_SATA_F_D2RN
18 TP_SATA_F_D2RP	=	NC_SATA_F_D2RP
18 TP_SATA_F_R2D_CN	=	NC_SATA_F_R2D_CN
18 TP_SATA_F_R2D_CP	=	NC_SATA_F_R2D_CP

MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE: UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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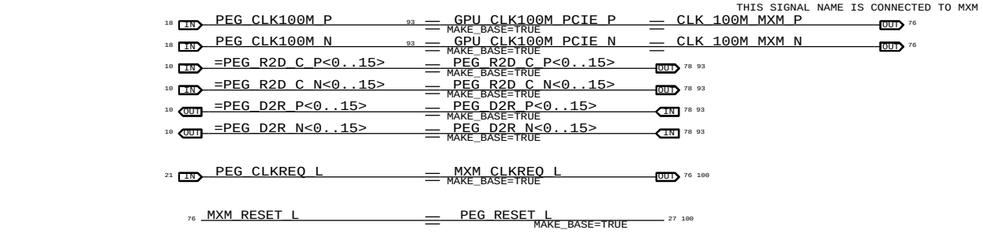
PEG Slot Support



SYNC_MASTER=K62_SIJI SYNC_DATE=09/11/2010

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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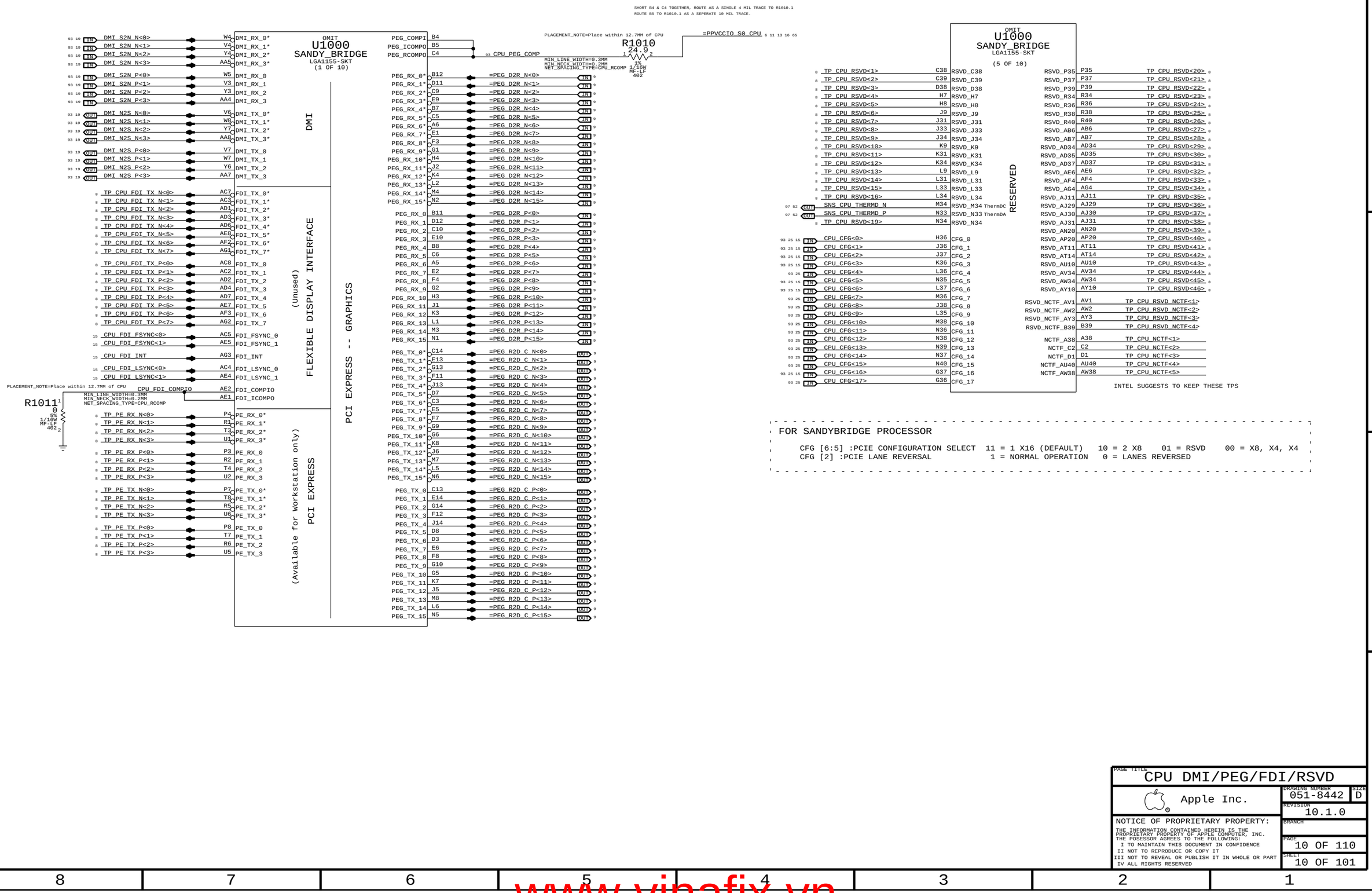

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

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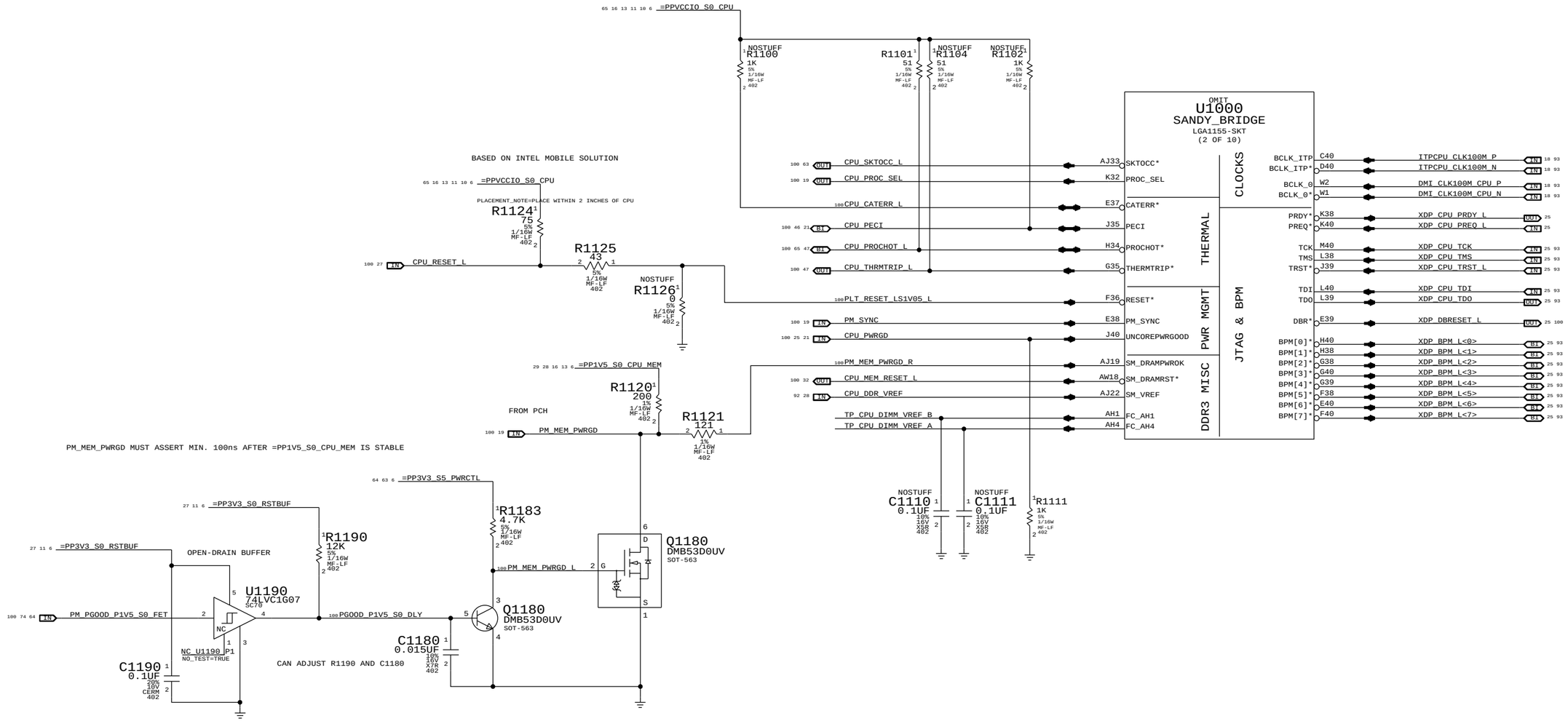

PAGE TITLE	CPU CLOCK/MISC/JTAG
	Apple Inc.
DRAWING NUMBER	051-8442
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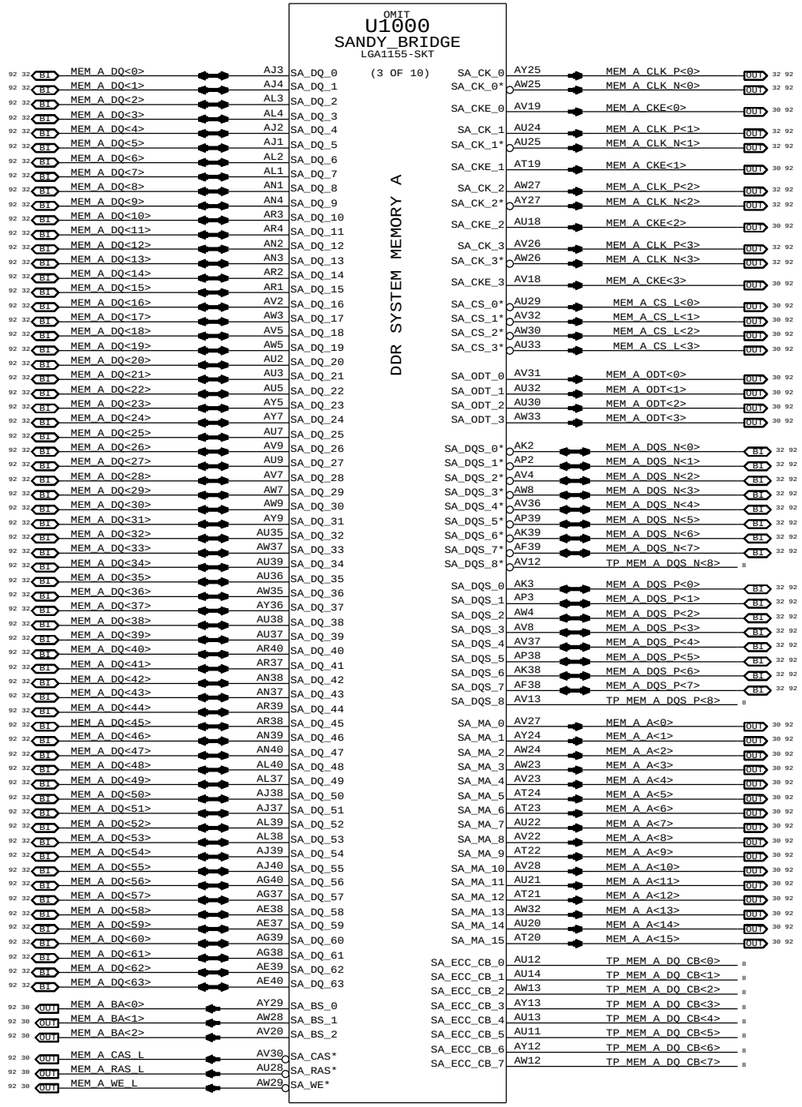

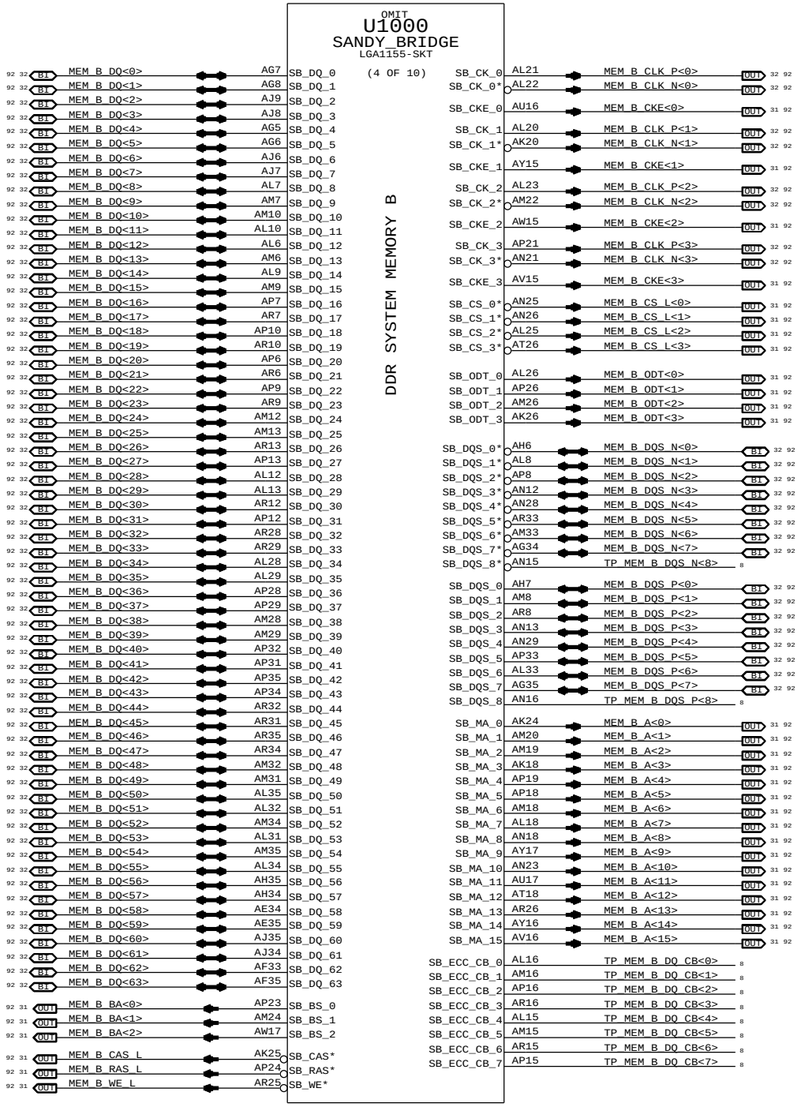

SYNC DATE=01/09/2011

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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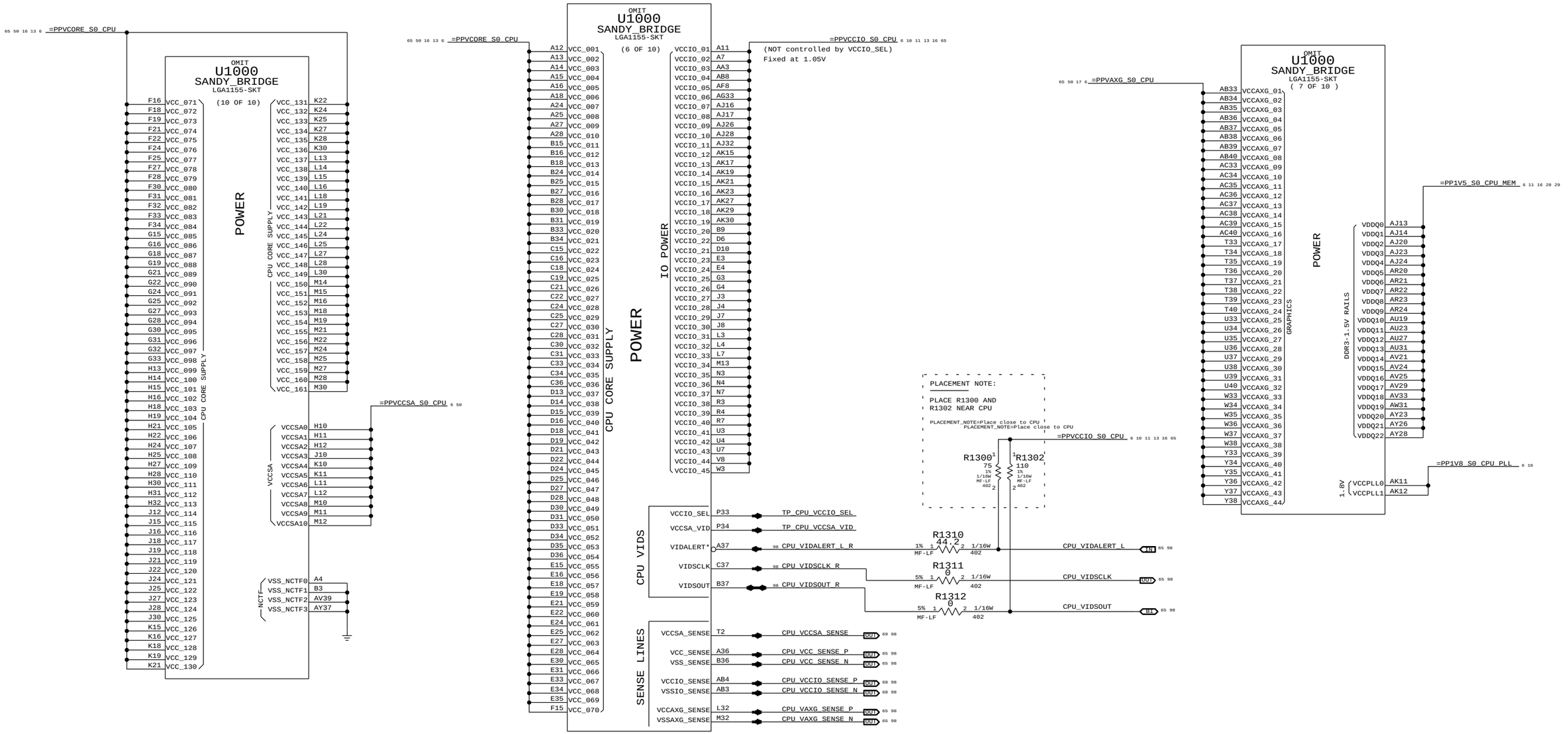

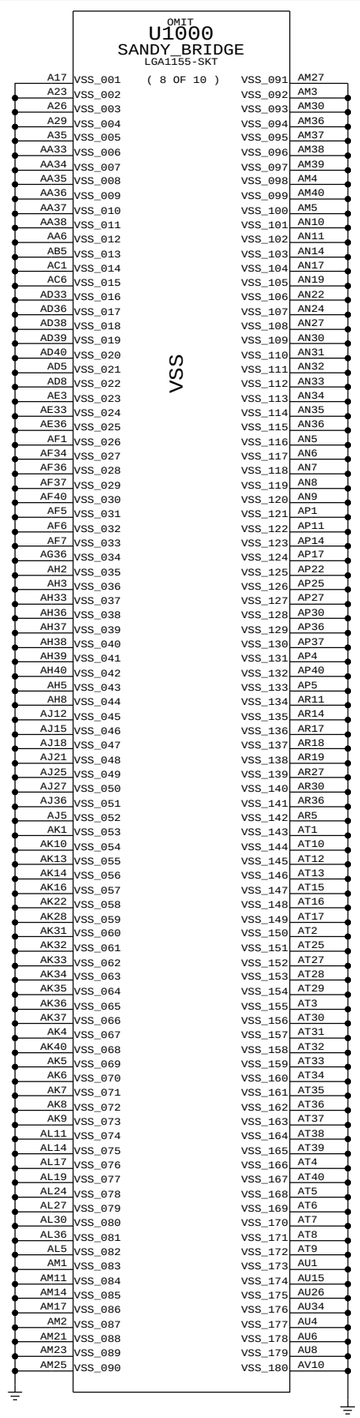

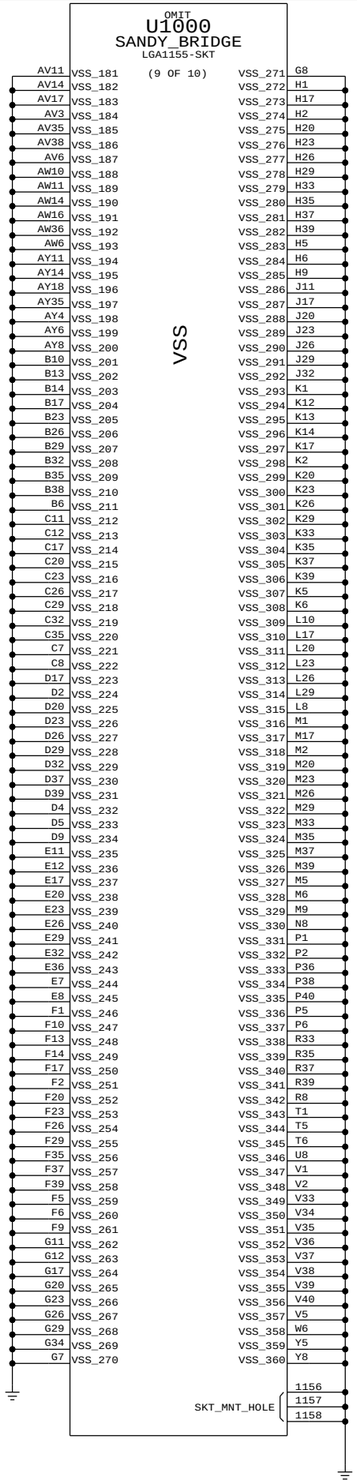

PAGE TITLE	CPU GROUNDS
	Apple Inc.
DRAWING NUMBER	051-8442
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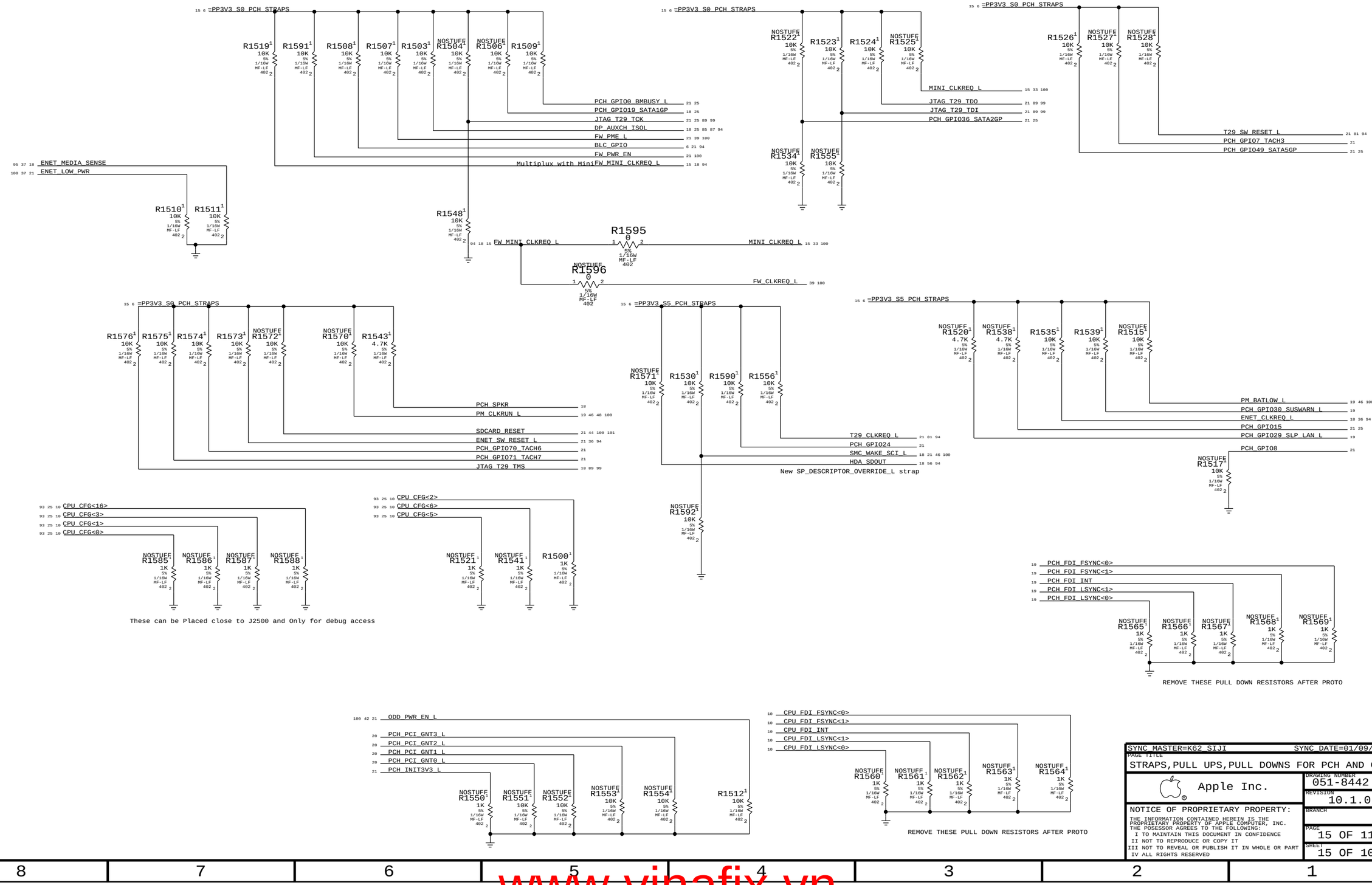

CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

16 13 6 =PPVCORE_S0_CPU
65 50

PLACEMENT_NOTE (C1600-C1613):

Place inside socket cavity

C1600 22UF 20% 6.3V CERM-X5R 805-3
C1601 22UF 20% 6.3V CERM-X5R 805-3
C1602 22UF 20% 6.3V CERM-X5R 805-3
C1603 22UF 20% 6.3V CERM-X5R 805-3
C1604 22UF 20% 6.3V CERM-X5R 805-3
C1605 22UF 20% 6.3V CERM-X5R 805-3
C1606 22UF 20% 6.3V CERM-X5R 805-3
C1607 22UF 20% 6.3V CERM-X5R 805-3
C1608 22UF 20% 6.3V CERM-X5R 805-3
C1609 22UF 20% 6.3V CERM-X5R 805-3

C1610 22UF 20% 6.3V CERM-X5R 805-3
C1611 22UF 20% 6.3V CERM-X5R 805-3
C1612 22UF 20% 6.3V CERM-X5R 805-3
C1613 22UF 20% 6.3V CERM-X5R 805-3

BULK CAPS ON CPU VREG PAGE 72

65 50 16 13 6 =PPVCORE_S0_CPU

10x 10UF and 10x 1UF CAPACITORS

Place inside socket cavity

C1620 10UF 20% 10V X5R 603
C1621 10UF 20% 10V X5R 603
C1622 10UF 20% 10V X5R 603
C1623 10UF 20% 10V X5R 603
C1624 10UF 20% 10V X5R 603
C1625 10UF 20% 10V X5R 603
C1626 10UF 20% 10V X5R 603
C1627 10UF 20% 10V X5R 603
C1628 10UF 20% 10V X5R 603
C1629 10UF 20% 10V X5R 603

C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 6s =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

C1650 22UF 20% 6.3V CERM-X5R 805
C1651 22UF 20% 6.3V CERM-X5R 805
C1652 22UF 20% 6.3V CERM-X5R 805
C1653 22UF 20% 6.3V CERM-X5R 805
C1654 22UF 20% 6.3V CERM-X5R 805
C1655 22UF 20% 6.3V CERM-X5R 805
C1656 22UF 20% 6.3V CERM-X5R 805
C1657 22UF 20% 6.3V CERM-X5R 805

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

BULK CAPS ON CPU VREG PAGE 72

C1660 10uF 20% 6.3V X5R 603
C1661 10uF 20% 6.3V X5R 603
C1662 10uF 20% 6.3V X5R 603
C1663 10uF 20% 6.3V X5R 603
C1664 10uF 20% 6.3V X5R 603
C1665 10uF 20% 6.3V X5R 603

C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805

28 13 11 6 29 =PP1V5_S0_CPU_MEM

C1676 22uF 20% 6.3V CERM-X5R 805
C1677 22uF 20% 6.3V CERM-X5R 805
C1678 22uF 20% 6.3V CERM-X5R 805
C1679 22uF 20% 6.3V CERM-X5R 805
C1680 22uF 20% 6.3V CERM-X5R 805
C1681 22uF 20% 6.3V CERM-X5R 805
C1682 1UF 10% 10V X5R 402
C1683 1UF 10% 10V X5R 402
C1684 1UF 10% 16V X5R 402
C1685 1UF 10% 16V X5R 402
C1686 1UF 10% 16V X5R 402

Note: VCCSA decoupling is on regulator page

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22UF 20% 6.3V CERM-X5R 805
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 78

SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE: CPU NON-GFX DECOUPLING

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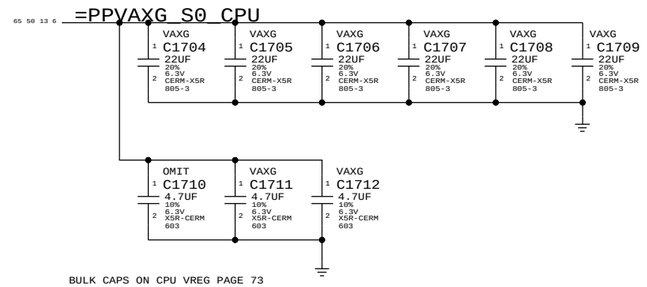
VAXG DECOUPLING

INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

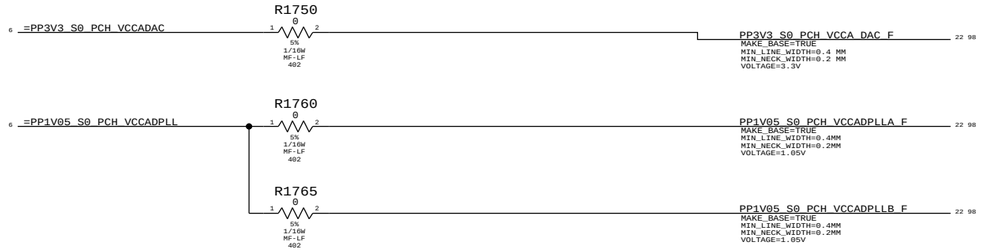
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



BULK CAPS ON CPU VREG PAGE 73

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
113S0022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

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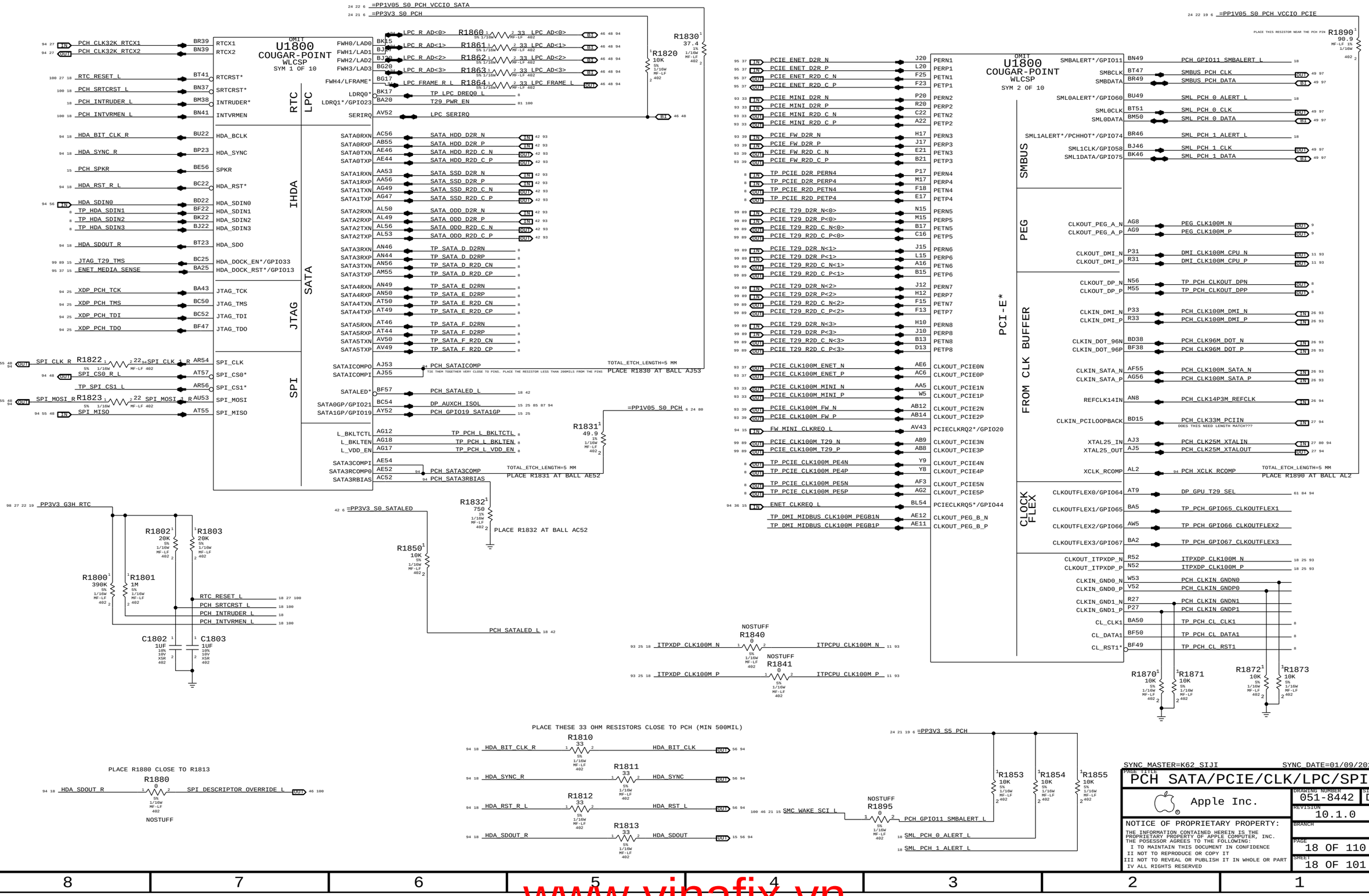

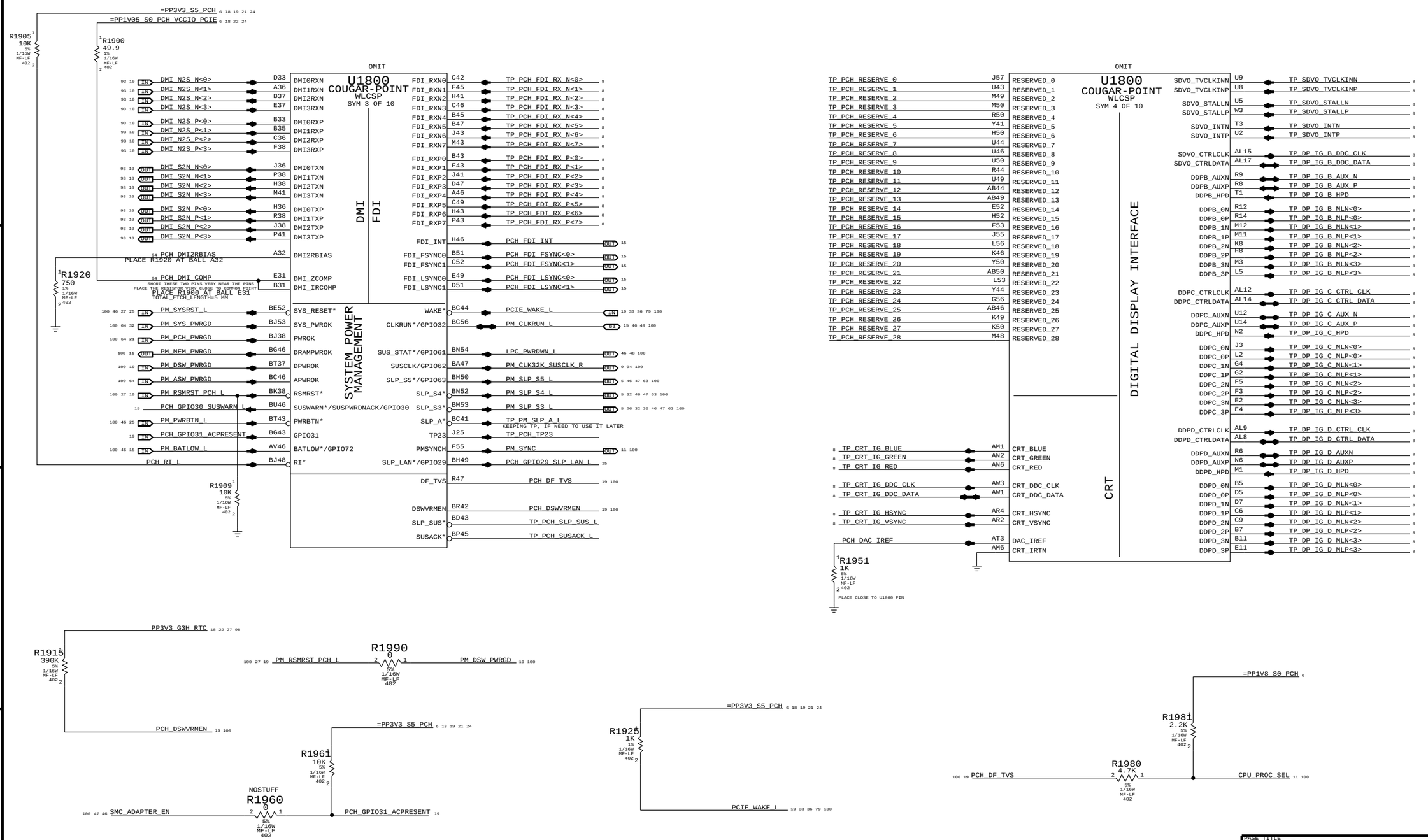

PAGE TITLE: PCH DMI/FDI/GRAPHICS

Apple Inc.

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OMIT

U1800
COUGAR-POINT
WLCSP
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PCI

TP_PCI_AD<0>	BF15	AD0	
TP_PCI_AD<1>	BF17	AD1	
TP_PCI_AD<2>	BT7	AD2	
TP_PCI_AD<3>	BT13	AD3	
TP_PCI_AD<4>	BG12	AD4	
TP_PCI_AD<5>	BN11	AD5	
TP_PCI_AD<6>	BJ12	AD6	
TP_PCI_AD<7>	BU9	AD7	
TP_PCI_AD<8>	BR12	AD8	
TP_PCI_AD<9>	BJ3	AD9	
TP_PCI_AD<10>	BR9	AD10	
TP_PCI_AD<11>	BJ10	AD11	
TP_PCI_AD<12>	BM8	AD12	
TP_PCI_AD<13>	BF3	AD13	
TP_PCI_AD<14>	BN2	AD14	
TP_PCI_AD<15>	BE4	AD15	
TP_PCI_AD<16>	BE6	AD16	
TP_PCI_AD<17>	BG15	AD17	
TP_PCI_AD<18>	BC6	AD18	
TP_PCI_AD<19>	BT11	AD19	
TP_PCI_AD<20>	BA14	AD20	
TP_PCI_AD<21>	BL2	AD21	
TP_PCI_AD<22>	BC4	AD22	
TP_PCI_AD<23>	BL4	AD23	
TP_PCI_AD<24>	BC2	AD24	
TP_PCI_AD<25>	BM13	AD25	
TP_PCI_AD<26>	BA9	AD26	
TP_PCI_AD<27>	BF9	AD27	
TP_PCI_AD<28>	BA8	AD28	
TP_PCI_AD<29>	BF8	AD29	
TP_PCI_AD<30>	AV17	AD30	
TP_PCI_AD<31>	BK12	AD31	
TP_PCI_C_BE_L<0>	BN4	C/BE0*	
TP_PCI_C_BE_L<1>	BP7	C/BE1*	
TP_PCI_C_BE_L<2>	BG2	C/BE2*	
TP_PCI_C_BE_L<3>	BP13	C/BE3*	
PCI_INTA_L	BK10	PIRQA*	
PCI_INTB_L	BJ5	PIRQB*	
PCI_INTC_L	BM15	PIRQC*	
PCI_INTD_L	BP5	PIRQD*	
PCI_REQ0_L	BG5	REQ0*	
PCI_REQ1_L	BT5	REQ1*/GPIO50	
PCI_REQ2_L	BK8	REQ2*/GPIO52	
PCI_REQ3_L	AV11	REQ3*/GPIO54	
PCH_PCI_GNT0_L	BA15	GNT0*	
PCH_PCI_GNT1_L	AV8	GNT1*/GPIO51	
PCH_PCI_GNT2_L	BU12	GNT2*/GPIO53	
PCH_PCI_GNT3_L	BE2	GNT3*/GPIO55	
USE_HDD_OOB_L	BN9	PIRQE*/GPIO2	
AUD_IP_PERIPHERAL_DET	AV9	PIRQF*/GPIO3	
T29_MCU_INT_L	BT15	PIRQG*/GPIO4	
AUD_I2C_INT_L	BR4	PIRQH*/GPIO5	
TP_PCI_RESET_L	AV14	PCIRST*	
PCI_SERR_L	BR6	SERR*	
PCI_PERR_L	BM3	PERR*	
PCI_IRDY_L	BF11	IRDY*	
TP_PCI_PAR	BH8	PAR	
PCI_DEVSEL_L	BH9	DEVSEL*	
PCI_FRAME_L	BC11	FRAME*	
PCI_PLOCK_L	BA17	PLOCK*	
PCI_STOP_L	BC12	STOP*	
PCI_TRDY_L	BC8	TRDY*	
TP_PCI_PME_L	AV15	PME*	
PLT_RESET_L	BK48	PLTRST*	
LPC_CLK33M_SMC_R	AT11	CLKOUT_PCI0	
LPC_CLK33M_LPCPLUS_R	AN14	CLKOUT_PCI1	
TP_PCI_CLK33M_OUT2	AT12	CLKOUT_PCI2	
TP_PCI_CLK33M_OUT3	AT17	CLKOUT_PCI3	
PCH_CLK33M_PCIOUT	AT14	CLKOUT_PCI4	

USB

USBP0N	BF36	USB_HUB1_UP_N	USB HUB 1
USBP0P	BD36	USB_HUB1_UP_P	
USBP1N	BC33	TP_USB_1N	Unused
USBP1P	BA33	TP_USB_1P	
USBP2N	BM33	TP_USB_2N	Unused
USBP2P	BM35	TP_USB_2P	
USBP3N	BT33	TP_USB_3N	Unused
USBP3P	BU32	TP_USB_3P	
USBP4N	BR32	TP_USB_4N	Unused
USBP4P	BT31	TP_USB_4P	
USBP5N	BN29	TP_USB_5N	Unused
USBP5P	BM30	TP_USB_5P	
USBP6N	BK33	TP_USB_6N	Unused
USBP6P	BJ33	TP_USB_6P	
USBP7N	BF31	TP_USB_7N	Unused
USBP7P	BD31	TP_USB_7P	
USBP8N	BN27	USB_HUB2_UP_N	USB HUB 2
USBP8P	BR29	USB_HUB2_UP_P	
USBP9N	BR26	USB_CAMERA_N	USB CAMERA
USBP9P	BT27	USB_CAMERA_P	
USBP10N	BK25	TP_USB_10N	Unused
USBP10P	BJ25	TP_USB_10P	
USBP11N	BJ31	TP_USB_11N	Unused
USBP11P	BK31	TP_USB_11P	
USBP12N	BF27	TP_USB_12N	Unused
USBP12P	BD27	TP_USB_12P	
USBP13N	BJ27	TP_USB_13N	Unused
USBP13P	BK27	TP_USB_13P	
USBRBIAS*	BP25	PCH_USB_RBIAS	
USBRBIAS	BM25		

TIE TRACES TOGETHER CLOSE TO PIN
PLACE THE RESISTOR CLOSE TO COMMON POINT

OC0*/GPIO59	BM43	
OC1*/GPIO40	BD41	
OC2*/GPIO41	BG41	
OC3*/GPIO42	BK43	
OC4*/GPIO43	BP43	
OC5*/GPIO9	BJ41	
OC6*/GPIO10	BT45	
OC7*/GPIO14	BM45	

R2070 22.6 1% 1/16W MF-LF 402
PLACE R2070 AT BALL BM25

=PP3V3_S5_PCH_GPIO

R2060 10K 5% 1/16W MF-LF 402
R2061 10K 5% 1/16W MF-LF 402
R2062 10K 5% 1/16W MF-LF 402
R2063 10K 5% 1/16W MF-LF 402
R2064 10K 5% 1/16W MF-LF 402
PRODUCTION
R2065 10K 5% 1/16W MF-LF 402
R2066 10K 5% 1/16W MF-LF 402
R2068 10K 5% 1/16W MF-LF 402

AP_PWR_EN
USB_HUB_SOFT_RESET_L
T29_DP_PORTA_PWR_EN
ENET_PWR_EN
T29_DP_PORTB_PWR_EN
SDCONN_STATE_CHANGE
PCH_GPIO10_OC6_L
PCH_GPIO14_OC7_L

=PP3V3_S0_PCH_GPIO

R2010 10K 5% 1/16W MF-LF 402 PCI_INTA_L
R2011 10K 5% 1/16W MF-LF 402 PCI_INTB_L
R2012 10K 5% 1/16W MF-LF 402 PCI_INTC_L
R2013 10K 5% 1/16W MF-LF 402 PCI_INTD_L
R2015 10K 5% 1/16W MF-LF 402 PCI_REQ0_L
R2016 10K 5% 1/16W MF-LF 402 PCI_REQ1_L
R2018 10K 5% 1/16W MF-LF 402 PCI_REQ3_L
R2030 10K 5% 1/16W MF-LF 402 USE_HDD_OOB_L
R2031 10K 5% 1/16W MF-LF 402 T29_MCU_INT_L
R2020 10K 5% 1/16W MF-LF 402 PCI_SERR_L
R2021 10K 5% 1/16W MF-LF 402 PCI_PERR_L
R2022 10K 5% 1/16W MF-LF 402 PCI_IRDY_L
R2023 10K 5% 1/16W MF-LF 402 TP_PCI_PAR
R2024 10K 5% 1/16W MF-LF 402 PCI_DEVSEL_L
R2027 10K 5% 1/16W MF-LF 402 PCI_FRAME_L
R2025 10K 5% 1/16W MF-LF 402 PCI_PLOCK_L
R2026 10K 5% 1/16W MF-LF 402 PCI_STOP_L
PCI_TRDY_L

PCH SATA PORT 1 OPTION SELECT IS ODD OR SSD

PCI_REQ2_L
R2017 10K 5% 1/16W MF-LF 402 ODD_SATA:P2 =PP3V3_S0_PCH_GPIO
R2098 10K 5% 1/16W MF-LF 402 ODD_SATA:P1

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE
PCH PCI/FLASHCACHE/USB

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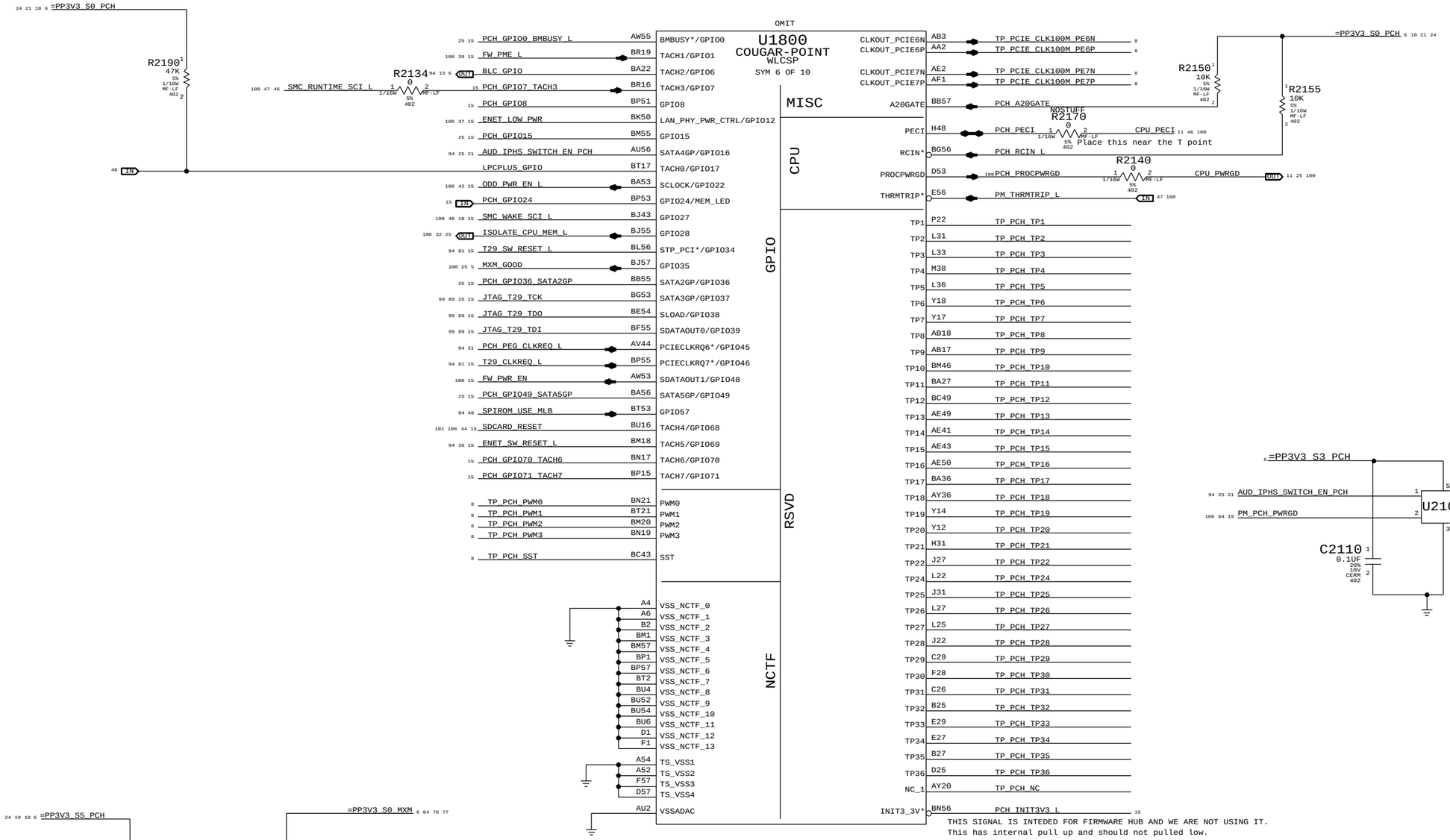

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PAGE TITLE: PCH MISC

Apple Inc.

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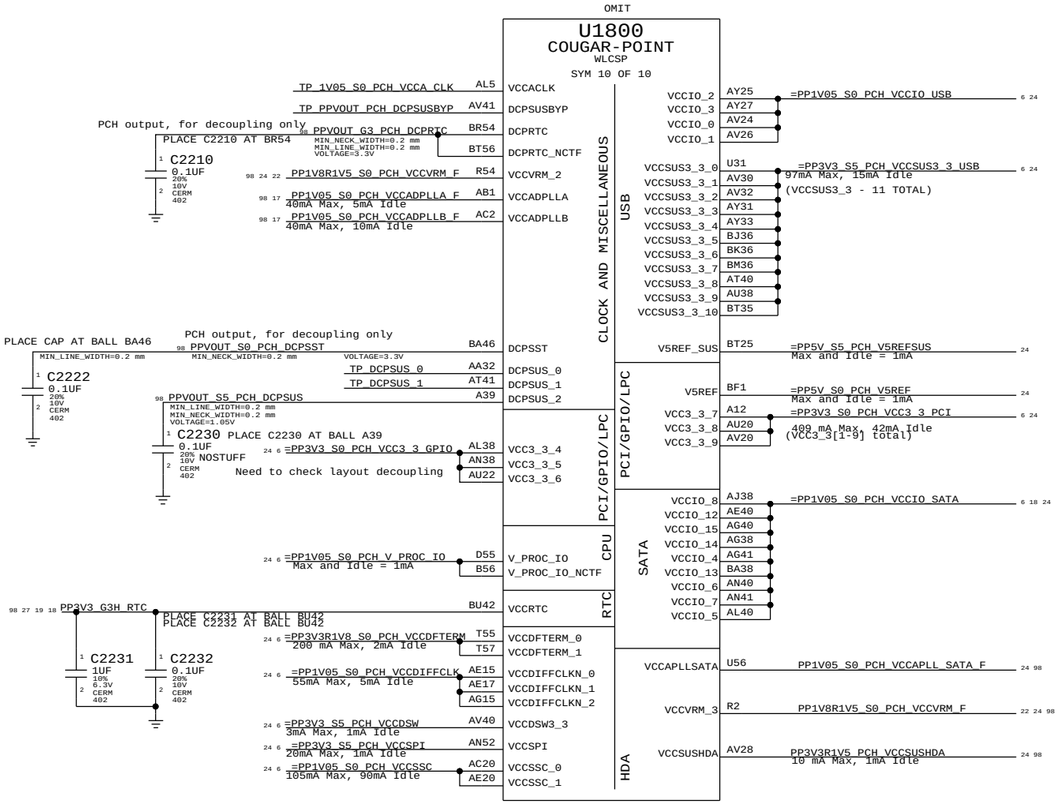

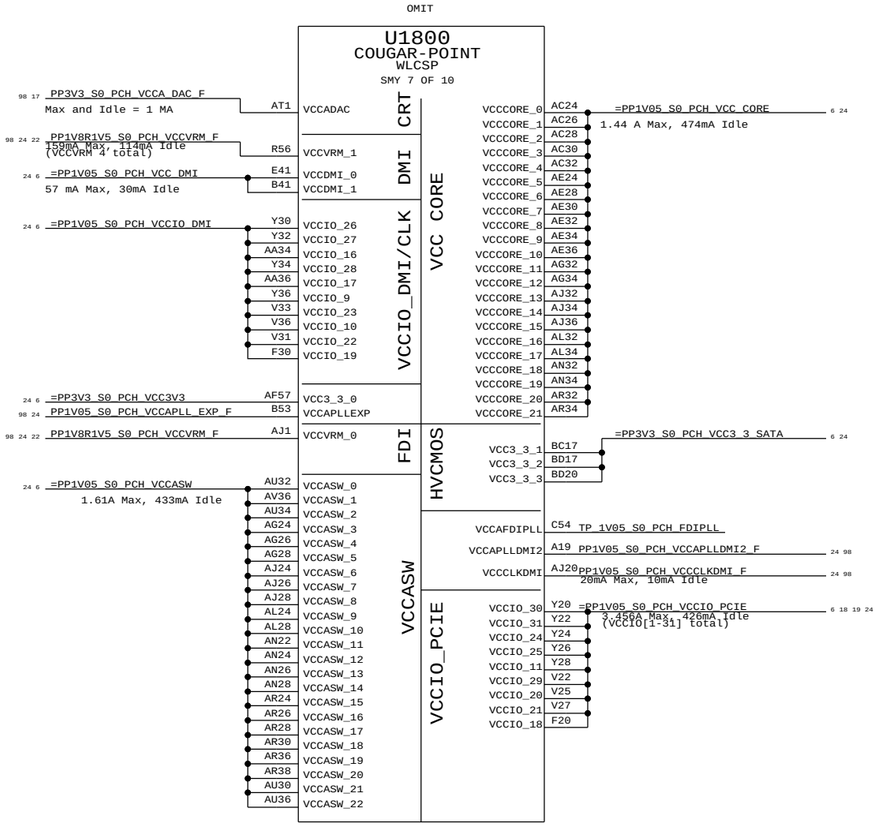

PAGE TITLE
PCH POWER

Apple Inc.

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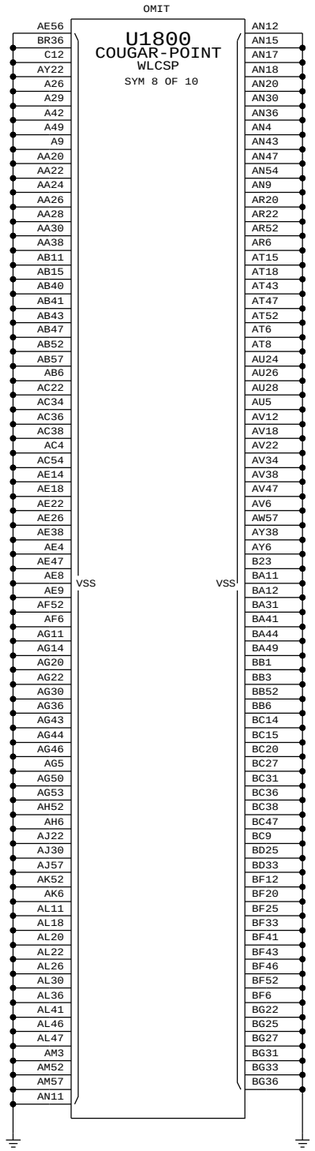

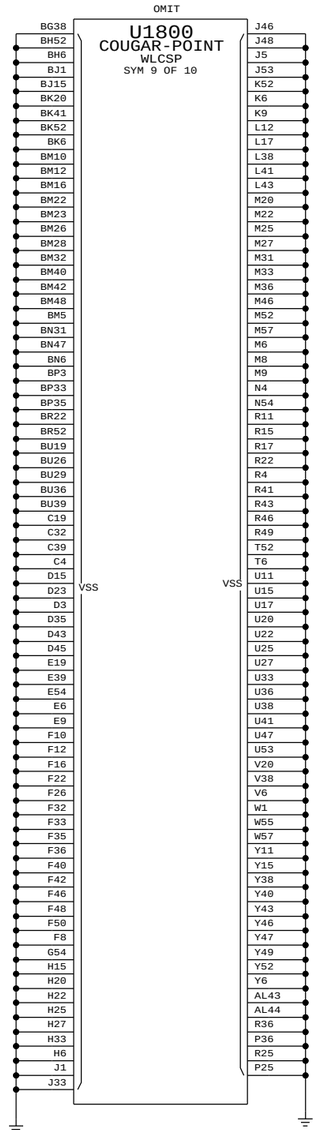

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PAGE TITLE

PCH GROUNDS

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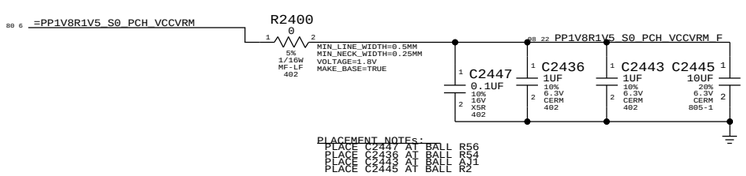

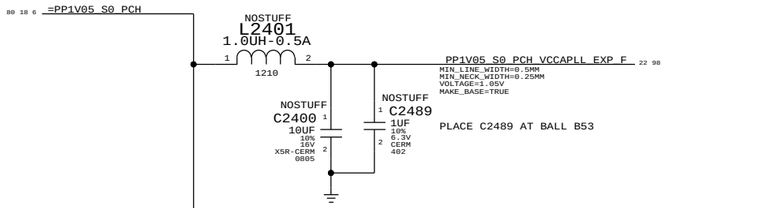

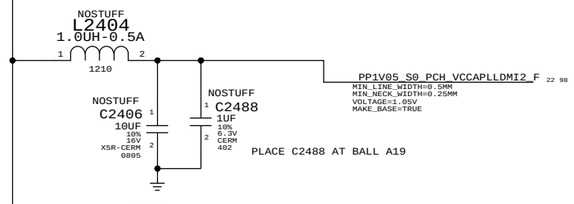

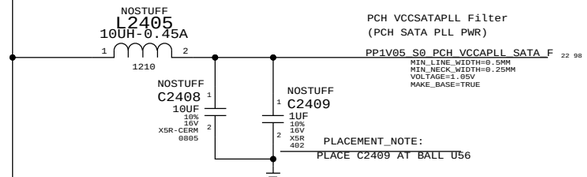

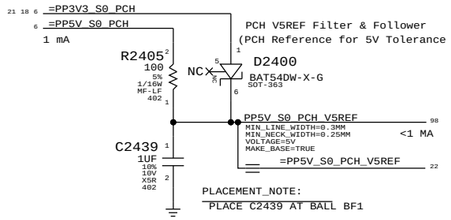

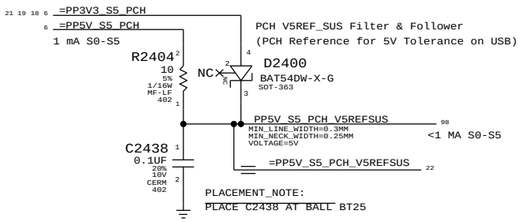

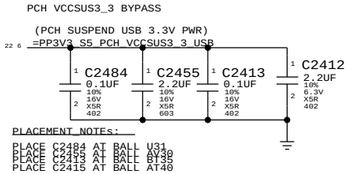

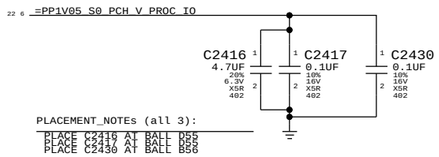

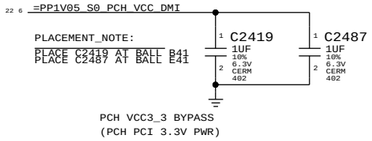

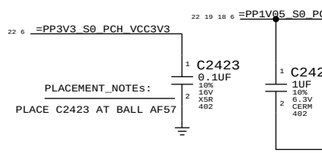

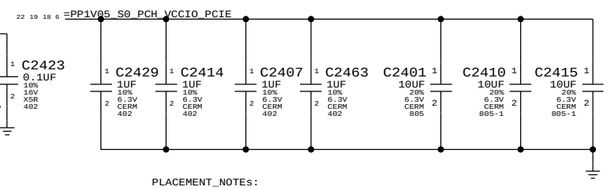

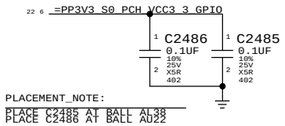

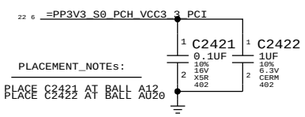

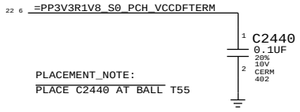

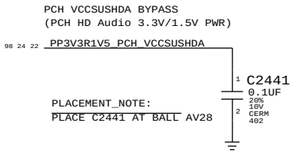

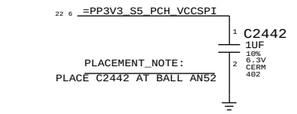

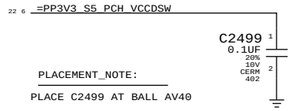

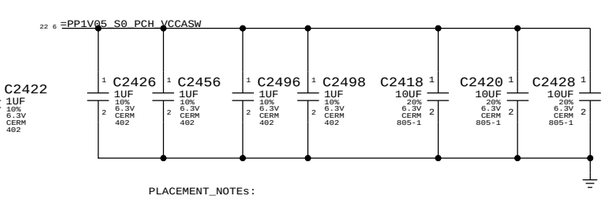

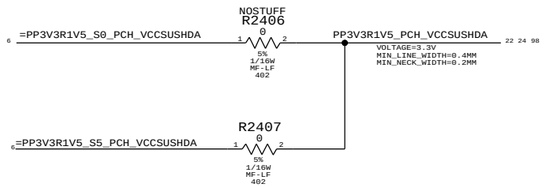

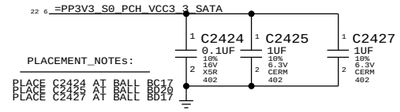

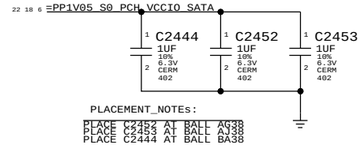

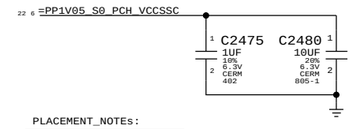

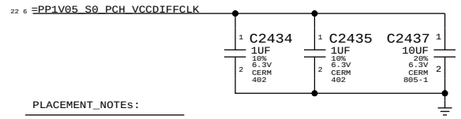

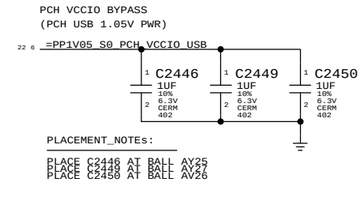

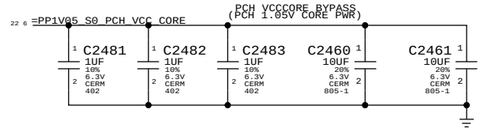

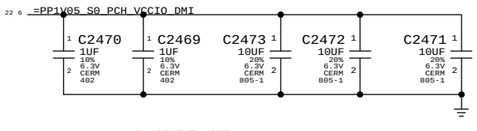

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PAGE TITLE
PCH DECOUPLING

Apple Inc.

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PROCESSOR MINI XDP

PLACEMENT_NOTE=Place R2501 close to R2500 to minimize stubs

XDP_CPU_BPM
RP2500
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>

XDP_CPU_CFG
RP2501
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>

XDP R2500 1K — CPU_PWRGD — PLACEMENT_NOTE=Place close to CPU
XDP R2502 0 — PM_PWRBTN_L — PLACEMENT_NOTE=Place close to SMC
XDP R2501 1K — CPU_CFG<0> — PLACEMENT_NOTE=Place close to CPU
XDP R2504 0 — PM_PGOOD_PVCORE_CPU

=PPVCCIO_S0_XDP

CRITICAL
XDP_CONN
J2500
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
CPU_CFG<10>
CPU_CFG<11>
XDP_OBSDATA_B<0>
XDP_OBSDATA_B<1>
XDP_OBSDATA_B<2>
XDP_OBSDATA_B<3>
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_CFG<0>
XDP_VR_READY
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_CPU_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

CPU_CFG<16> CPU_CFG<17> CPU_CFG<0> CPU_CFG<1> CPU_CFG<2> CPU_CFG<3> CPU_CFG<8> CPU_CFG<9> CPU_CFG<4> CPU_CFG<5> CPU_CFG<6> CPU_CFG<7>

XDP_CPU_CLK100M_P
XDP_CPU_CLK100M_N
XDP_DBRESET_L
XDP_CPU_TDO
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS

XDP C2500 0.1uF — XDP C2501 0.1uF

XDP R2515 0 — PLACEMENT_NOTE=Place close to R1841 — ITPXDP_CLK100M_P
XDP R2516 0 — PLACEMENT_NOTE=Place close to R1840 — ITPXDP_CLK100M_N

<- 1K SERIES R ON PCH SUPPORT P. 28

NOTE: XDP_DBRESET_L pulled-up to 3.3V on P. 28

DESIGN NOTE:
ODT AVAILABLE ON JTAG

PLACEMENT NOTE:
PLACE TDO TERM NEAR SNB XDP CONN
XDP R2510 51 — PLACEMENT_NOTE=Place close to J2500
XDP R2511 51 — PLACEMENT_NOTE=Place close to CPU
XDP R2512 51 — PLACEMENT_NOTE=Place close to CPU

XDP_CPU_TDO
XDP_CPU_TDI
XDP_CPU_TMS
XDP_CPU_TCK
XDP_CPU_TRST_L

XDP R2513 51 — PLACEMENT_NOTE=Place close to CPU
XDP R2514 51 — PLACEMENT_NOTE=Place close to CPU

PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR CPU

XDP R2506 0 — PLACEMENT_NOTE=Place close to SW2800 — XDP_DBRESET_L — To Reset Button — PM_SYSRST_L

PCH MINI XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40C-60DS-0.4V
F-ST-SM-HF
518S0774

TP_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1>
XDP_PCH_AP_PWR_EN
XDP_PCH_USB_HUB_SOFT_RST_L
XDP_PCH_T29_DP_PORTA_PWR_EN
XDP_PCH_ENET_PWR_EN
TP_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1>
XDP_PCH_T29_DP_PORTB_PWR_EN
XDP_PCH_SDCONN_CHANGE
PCH_GPIO10_OC6_L
PCH_GPIO14_OC7_L
XDP_PCH_S5_PWRGD
XDP_PCH_PWRBTN_L
TP_XDPPCH_HOOK2
TP_XDPPCH_HOOK3
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_PCH_TCK

OBSEN_A0 OBSEN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3 OBSEN_B0 OBSEN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3 PWRGD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 SDA SCL TCK1 TCK0

OBSEN_C0 OBSEN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3 OBSEN_D0 OBSEN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 TDO TRSTn TDI TMS XDP_PRESENT#

XDP_PCH_GPIO15
PCH_GPIO9_BMBUSY_L
XDP_PCH_ISOLATE_CPU_MEM_L
XDP_PCH_MXM_GOOD
XDP_PCH_DP_AUXCH_ISOL
PCH_GPIO19_SATA1GP
TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1>
PCH_GPIO36_SATA2GP
XDP_PCH_JTAG_T29_TCK
XDP_PCH_AUD_IPHS_SWITCH_EN
PCH_GPIO49_SATA5GP
TP_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5
XDPPCH_PLTRST_L
XDP_DBRESET_L
XDP_PCH_TDO
TP_XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

XDP C2580 0.1uF — XDP C2581 0.1uF

XDP R2582 0 — AP_PWR_EN — PLACEMENT_NOTE=Place close to PCH
XDP R2580 0 — USB_HUB_SOFT_RESET_L — PLACEMENT_NOTE=Place close to PCH
XDP R2583 0 — T29_DP_PORTA_PWR_EN — PLACEMENT_NOTE=Place close to PCH
XDP R2587 0 — ENET_PWR_EN — PLACEMENT_NOTE=Place close to PCH
XDP R2586 0 — T29_DP_PORTB_PWR_EN — PLACEMENT_NOTE=Place close to PCH
XDP R2581 0 — SDCONN_STATE_CHANGE — PLACEMENT_NOTE=Place close to PCH
XDP R2584 1K — =PP3V3_S5_XDP — PLACEMENT_NOTE=Place close to J2550
XDP R2585 0 — PM_PWRBTN_L — PLACEMENT_NOTE=Place close to SMC

XDP R2578 0 — PCH_GPIO15 — PLACEMENT_NOTE=Place close to PCH
XDP R2576 0 — ISOLATE_CPU_MEM_L — PLACEMENT_NOTE=Place close to PCH
XDP R2577 0 — MXM_GOOD — PLACEMENT_NOTE=Place close to PCH
XDP R2575 0 — DP_AUXCH_ISOL — PLACEMENT_NOTE=Place close to PCH
XDP R2573 0 — JTAG_T29_TCK — PLACEMENT_NOTE=Place close to PCH
XDP R2579 0 — AUD_IPHS_SWITCH_EN_PCH — PLACEMENT_NOTE=Place close to PCH

<- 1K SERIES R ON PCH SUPPORT P. 28

=PP3V3_S5_XDP

PLACEMENT NOTE:
PLACE TDO TERM NEAR PCH XDP CONN
XDP R2550 200 — PLACEMENT_NOTE=Place close to J2550
XDP R2551 200 — PLACEMENT_NOTE=Place close to PCH
XDP R2552 200 — PLACEMENT_NOTE=Place close to PCH

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_TCK

XDP R2553 100 — PLACEMENT_NOTE=Place close to PCH
XDP R2554 100 — PLACEMENT_NOTE=Place close to PCH
XDP R2555 100 — PLACEMENT_NOTE=Place close to PCH
XDP R2556 51 — PLACEMENT_NOTE=Place close to PCH

This is to derive 1.05V SUS RAIL

PLACEMENT NOTE:
PLACE TCK/TDI/TMS/TRST* TERM NEAR PCH

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE: CPU & PCH XDP

Apple Inc.

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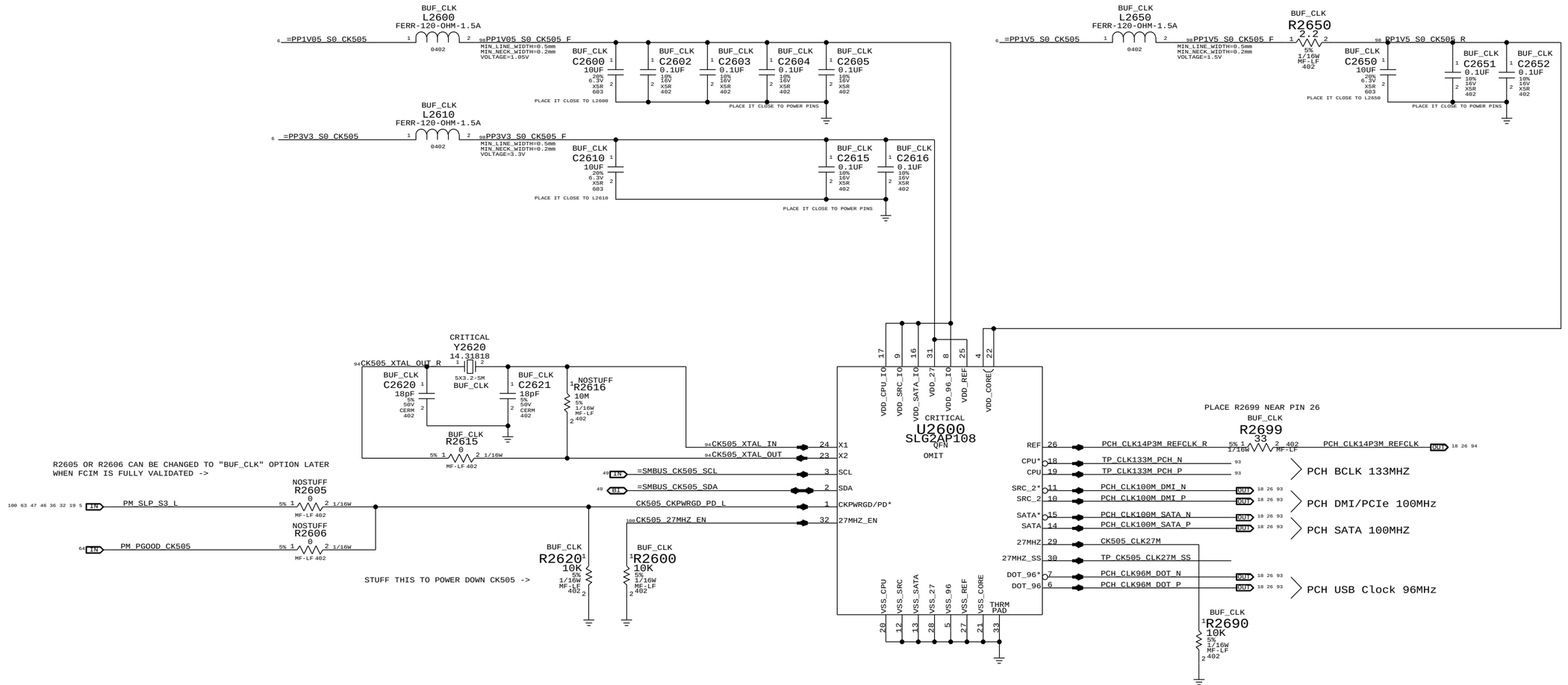
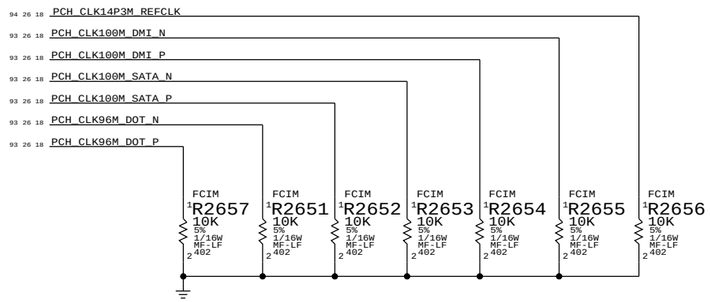


UNUSED clock terminations for FCIM MODE



SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: CLOCK (CK505)

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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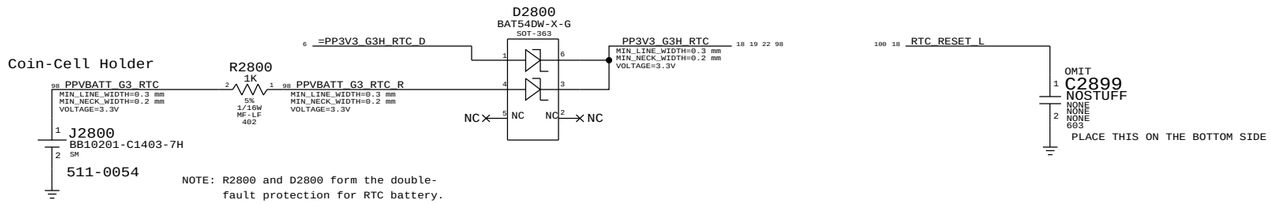
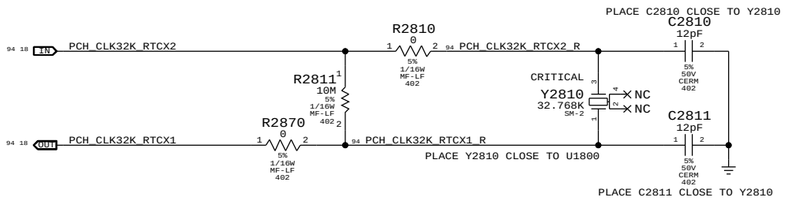
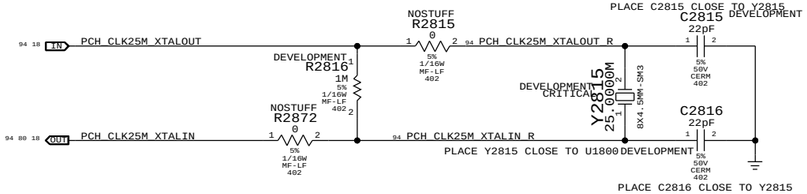
RTC Power Sources

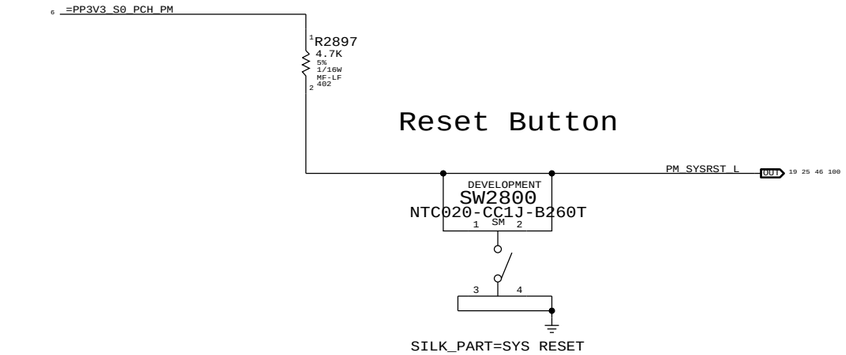


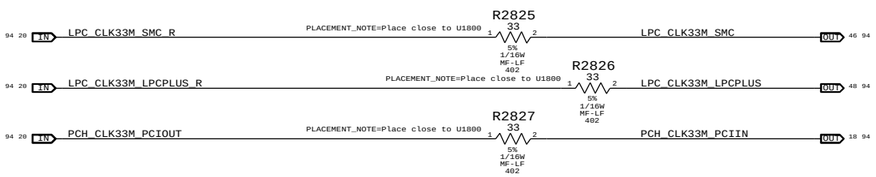
PCH RTC Crystal



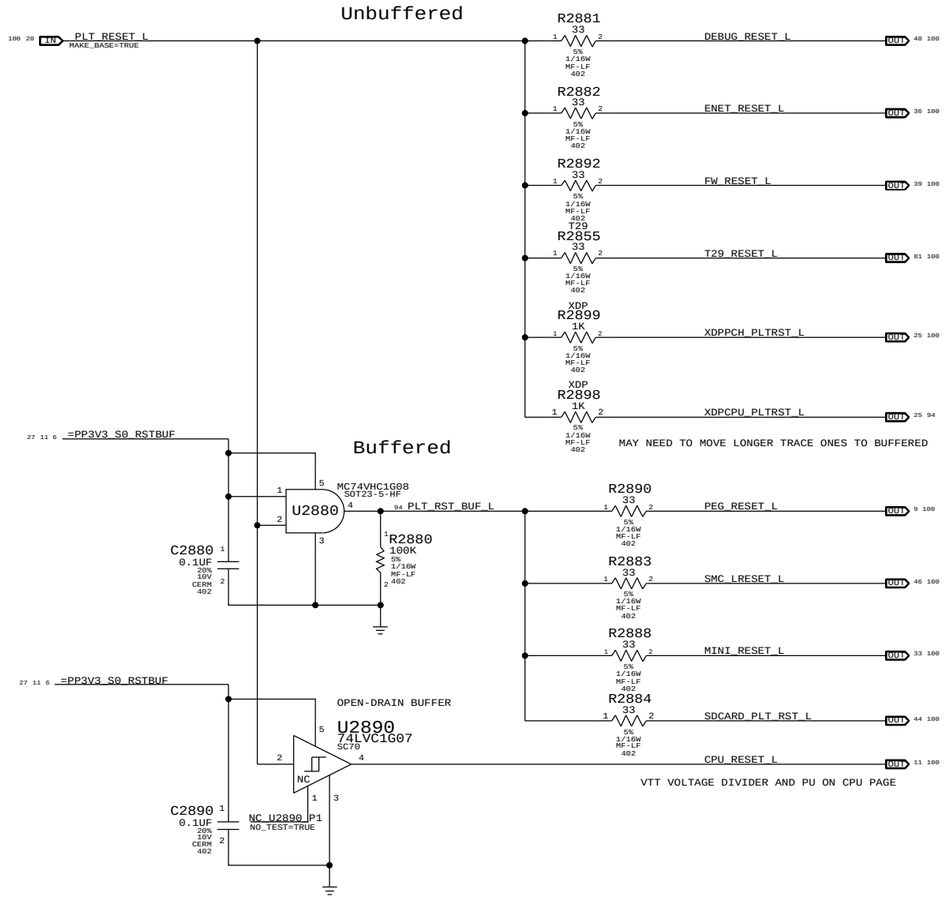
PCH 25MHZ CRYSTAL

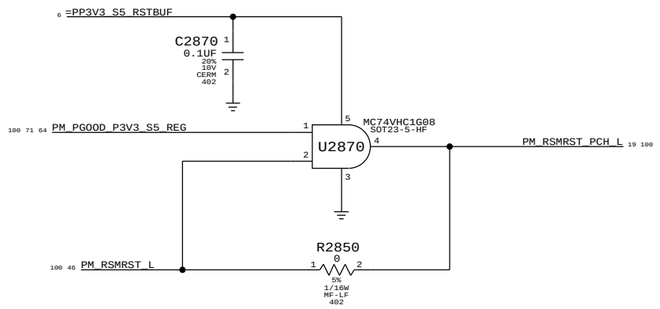






Platform Reset Connections





SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

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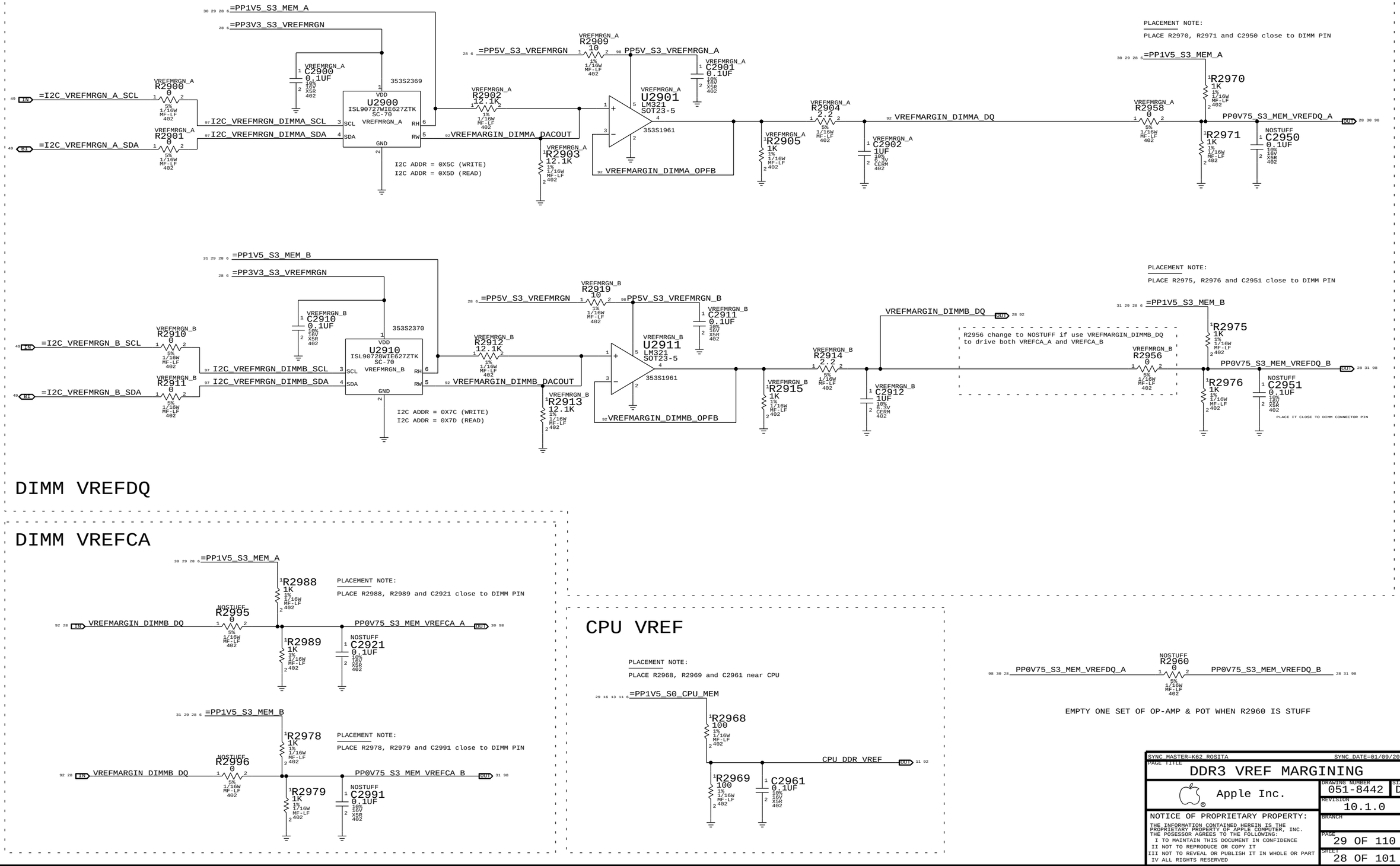
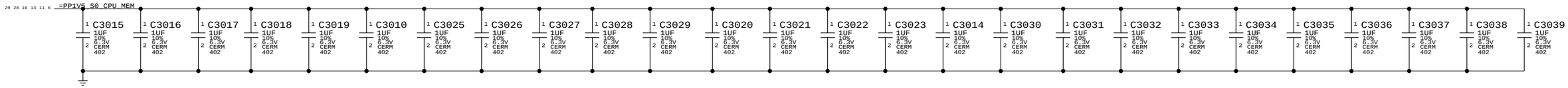


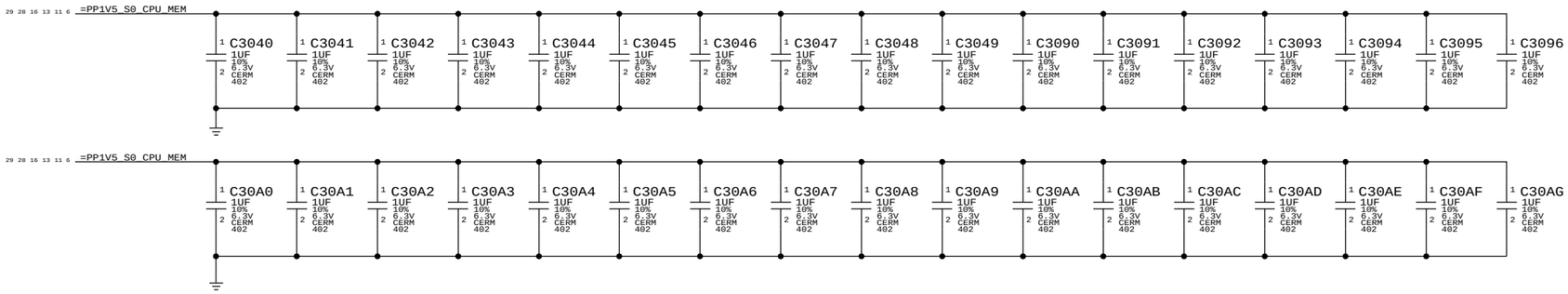
DIMM A (CLOSER TO CPU)

CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM

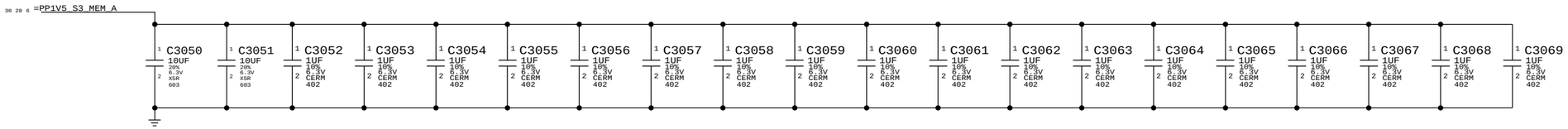
DIMM B (FURTHER FROM CPU)



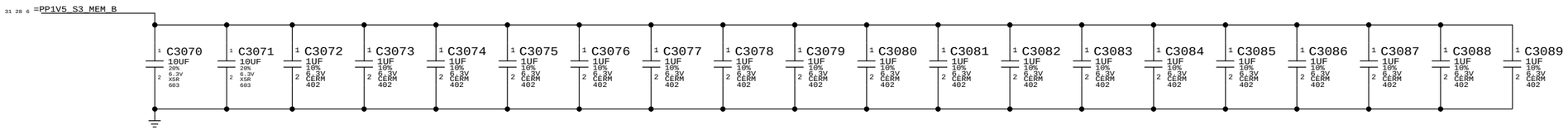
EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR



SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: MEMORY CAPS

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DRAWING NUMBER: 051-8442 SIZE: D

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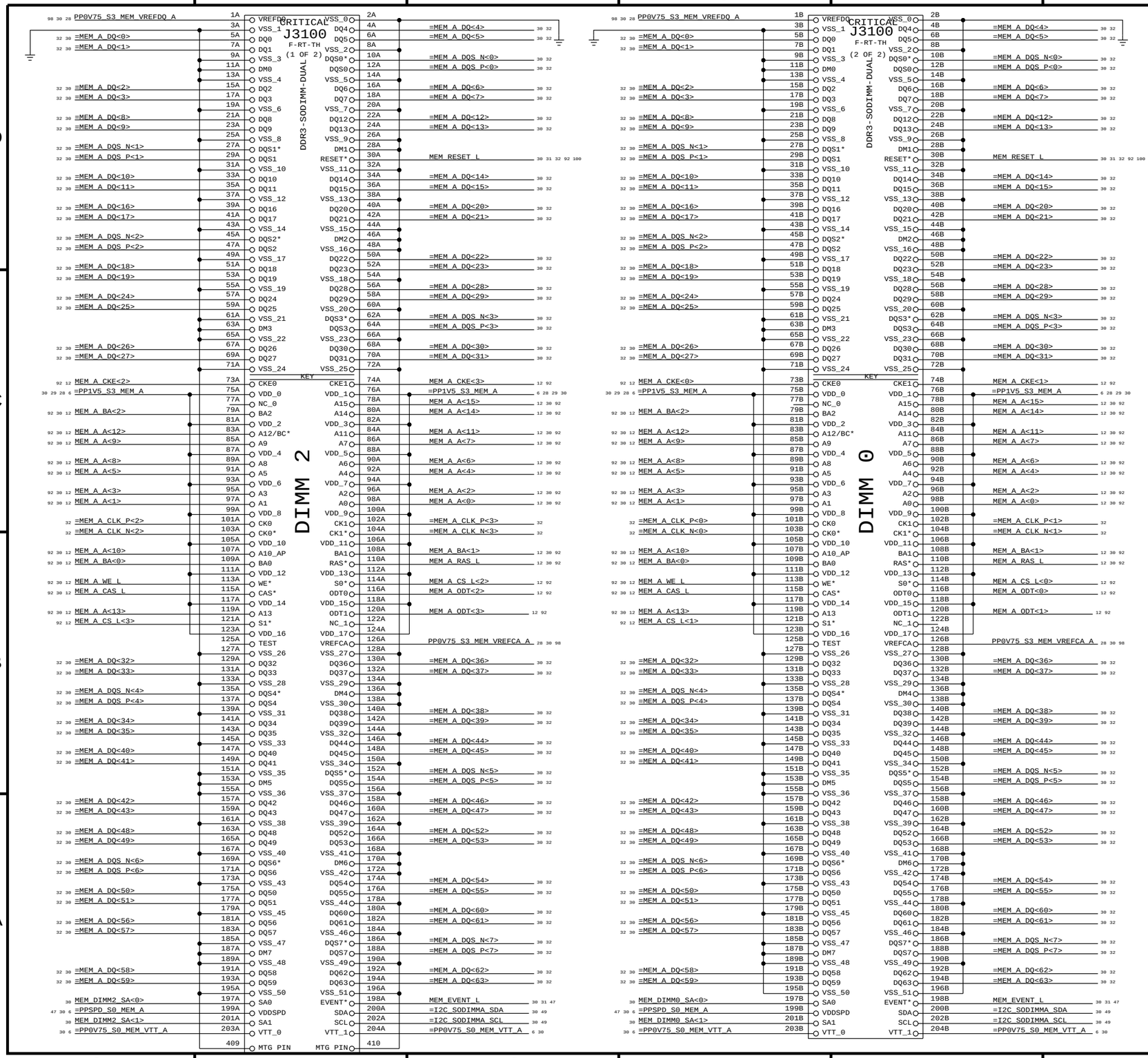

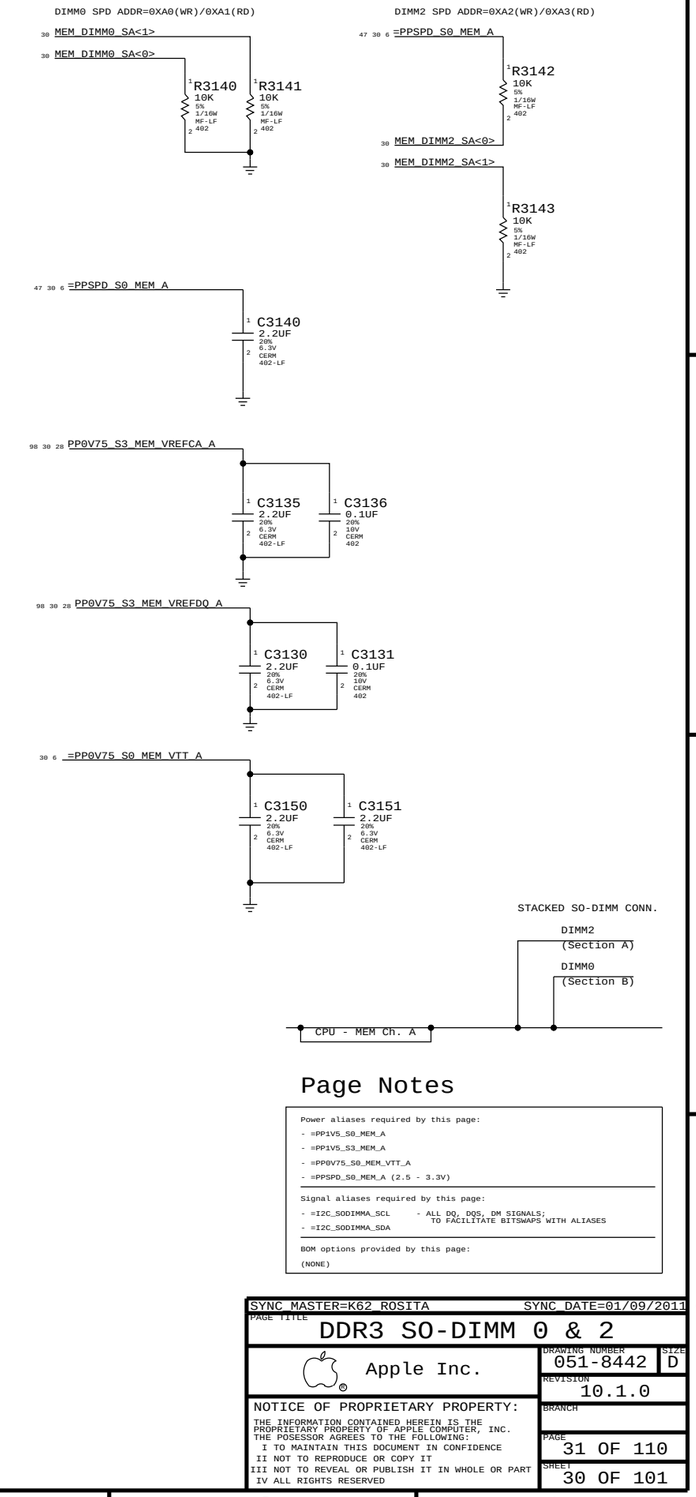

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: DDR3 SO-DIMM 0 & 2

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
BRANCH:
PAGE: 31 OF 110
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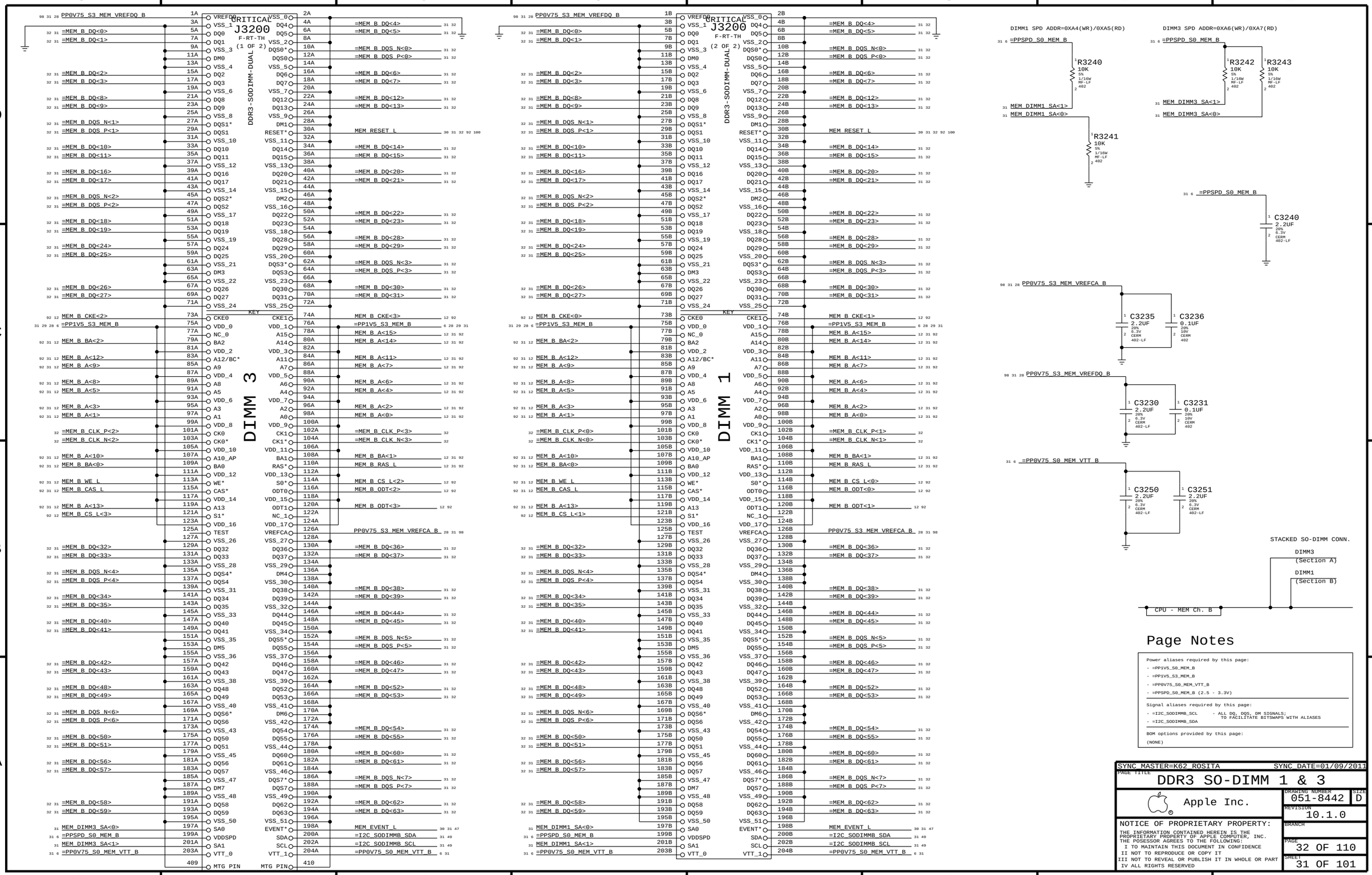

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: DDR3 SO-DIMM 1 & 3

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
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CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<7>
MEM_A_DQS_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<7>

MEM_A_DQ<7> MAKE_BASE=TRUE =MEM_A_DQ<57>
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MEM_A_DQ<5> MAKE_BASE=TRUE =MEM_A_DQ<58>
MEM_A_DQ<4> MAKE_BASE=TRUE =MEM_A_DQ<59>
MEM_A_DQ<3> MAKE_BASE=TRUE =MEM_A_DQ<60>
MEM_A_DQ<2> MAKE_BASE=TRUE =MEM_A_DQ<61>
MEM_A_DQ<1> MAKE_BASE=TRUE =MEM_A_DQ<62>
MEM_A_DQ<0> MAKE_BASE=TRUE =MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<6>
MEM_A_DQS_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<6>

MEM_A_DQ<15> MAKE_BASE=TRUE =MEM_A_DQ<49>
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MEM_A_DQ<13> MAKE_BASE=TRUE =MEM_A_DQ<51>
MEM_A_DQ<12> MAKE_BASE=TRUE =MEM_A_DQ<50>
MEM_A_DQ<11> MAKE_BASE=TRUE =MEM_A_DQ<48>
MEM_A_DQ<10> MAKE_BASE=TRUE =MEM_A_DQ<53>
MEM_A_DQ<9> MAKE_BASE=TRUE =MEM_A_DQ<55>
MEM_A_DQ<8> MAKE_BASE=TRUE =MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<5>
MEM_A_DQS_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<5>

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MEM_A_DQ<22> MAKE_BASE=TRUE =MEM_A_DQ<45>
MEM_A_DQ<21> MAKE_BASE=TRUE =MEM_A_DQ<46>
MEM_A_DQ<20> MAKE_BASE=TRUE =MEM_A_DQ<47>
MEM_A_DQ<19> MAKE_BASE=TRUE =MEM_A_DQ<41>
MEM_A_DQ<18> MAKE_BASE=TRUE =MEM_A_DQ<44>
MEM_A_DQ<17> MAKE_BASE=TRUE =MEM_A_DQ<43>
MEM_A_DQ<16> MAKE_BASE=TRUE =MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<4>
MEM_A_DQS_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<4>

MEM_A_DQ<31> MAKE_BASE=TRUE =MEM_A_DQ<37>
MEM_A_DQ<30> MAKE_BASE=TRUE =MEM_A_DQ<33>
MEM_A_DQ<29> MAKE_BASE=TRUE =MEM_A_DQ<35>
MEM_A_DQ<28> MAKE_BASE=TRUE =MEM_A_DQ<34>
MEM_A_DQ<27> MAKE_BASE=TRUE =MEM_A_DQ<36>
MEM_A_DQ<26> MAKE_BASE=TRUE =MEM_A_DQ<32>
MEM_A_DQ<25> MAKE_BASE=TRUE =MEM_A_DQ<38>
MEM_A_DQ<24> MAKE_BASE=TRUE =MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<3>
MEM_A_DQS_P<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<3>

MEM_A_DQ<39> MAKE_BASE=TRUE =MEM_A_DQ<28>
MEM_A_DQ<38> MAKE_BASE=TRUE =MEM_A_DQ<29>
MEM_A_DQ<37> MAKE_BASE=TRUE =MEM_A_DQ<27>
MEM_A_DQ<36> MAKE_BASE=TRUE =MEM_A_DQ<31>
MEM_A_DQ<35> MAKE_BASE=TRUE =MEM_A_DQ<25>
MEM_A_DQ<34> MAKE_BASE=TRUE =MEM_A_DQ<24>
MEM_A_DQ<33> MAKE_BASE=TRUE =MEM_A_DQ<26>
MEM_A_DQ<32> MAKE_BASE=TRUE =MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<2>
MEM_A_DQS_P<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<2>

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MEM_A_DQ<46> MAKE_BASE=TRUE =MEM_A_DQ<16>
MEM_A_DQ<45> MAKE_BASE=TRUE =MEM_A_DQ<22>
MEM_A_DQ<44> MAKE_BASE=TRUE =MEM_A_DQ<23>
MEM_A_DQ<43> MAKE_BASE=TRUE =MEM_A_DQ<21>
MEM_A_DQ<42> MAKE_BASE=TRUE =MEM_A_DQ<20>
MEM_A_DQ<41> MAKE_BASE=TRUE =MEM_A_DQ<18>
MEM_A_DQ<40> MAKE_BASE=TRUE =MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<1>
MEM_A_DQS_P<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<1>

MEM_A_DQ<55> MAKE_BASE=TRUE =MEM_A_DQ<12>
MEM_A_DQ<54> MAKE_BASE=TRUE =MEM_A_DQ<13>
MEM_A_DQ<53> MAKE_BASE=TRUE =MEM_A_DQ<10>
MEM_A_DQ<52> MAKE_BASE=TRUE =MEM_A_DQ<15>
MEM_A_DQ<51> MAKE_BASE=TRUE =MEM_A_DQ<8>
MEM_A_DQ<50> MAKE_BASE=TRUE =MEM_A_DQ<9>
MEM_A_DQ<49> MAKE_BASE=TRUE =MEM_A_DQ<11>
MEM_A_DQ<48> MAKE_BASE=TRUE =MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_N<0>
MEM_A_DQS_P<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_DQS_P<0>

MEM_A_DQ<63> MAKE_BASE=TRUE =MEM_A_DQ<5>
MEM_A_DQ<62> MAKE_BASE=TRUE =MEM_A_DQ<4>
MEM_A_DQ<61> MAKE_BASE=TRUE =MEM_A_DQ<3>
MEM_A_DQ<60> MAKE_BASE=TRUE =MEM_A_DQ<2>
MEM_A_DQ<59> MAKE_BASE=TRUE =MEM_A_DQ<1>
MEM_A_DQ<58> MAKE_BASE=TRUE =MEM_A_DQ<0>
MEM_A_DQ<57> MAKE_BASE=TRUE =MEM_A_DQ<7>
MEM_A_DQ<56> MAKE_BASE=TRUE =MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<7>
MEM_B_DQS_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<7>

MEM_B_DQ<7> MAKE_BASE=TRUE =MEM_B_DQ<61>
MEM_B_DQ<6> MAKE_BASE=TRUE =MEM_B_DQ<60>
MEM_B_DQ<5> MAKE_BASE=TRUE =MEM_B_DQ<62>
MEM_B_DQ<4> MAKE_BASE=TRUE =MEM_B_DQ<63>
MEM_B_DQ<3> MAKE_BASE=TRUE =MEM_B_DQ<56>
MEM_B_DQ<2> MAKE_BASE=TRUE =MEM_B_DQ<57>
MEM_B_DQ<1> MAKE_BASE=TRUE =MEM_B_DQ<58>
MEM_B_DQ<0> MAKE_BASE=TRUE =MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<6>
MEM_B_DQS_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<6>

MEM_B_DQ<15> MAKE_BASE=TRUE =MEM_B_DQ<51>
MEM_B_DQ<14> MAKE_BASE=TRUE =MEM_B_DQ<54>
MEM_B_DQ<13> MAKE_BASE=TRUE =MEM_B_DQ<53>
MEM_B_DQ<12> MAKE_BASE=TRUE =MEM_B_DQ<52>
MEM_B_DQ<11> MAKE_BASE=TRUE =MEM_B_DQ<48>
MEM_B_DQ<10> MAKE_BASE=TRUE =MEM_B_DQ<49>
MEM_B_DQ<9> MAKE_BASE=TRUE =MEM_B_DQ<50>
MEM_B_DQ<8> MAKE_BASE=TRUE =MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<5>
MEM_B_DQS_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<5>

MEM_B_DQ<23> MAKE_BASE=TRUE =MEM_B_DQ<45>
MEM_B_DQ<22> MAKE_BASE=TRUE =MEM_B_DQ<40>
MEM_B_DQ<21> MAKE_BASE=TRUE =MEM_B_DQ<42>
MEM_B_DQ<20> MAKE_BASE=TRUE =MEM_B_DQ<47>
MEM_B_DQ<19> MAKE_BASE=TRUE =MEM_B_DQ<44>
MEM_B_DQ<18> MAKE_BASE=TRUE =MEM_B_DQ<41>
MEM_B_DQ<17> MAKE_BASE=TRUE =MEM_B_DQ<46>
MEM_B_DQ<16> MAKE_BASE=TRUE =MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<4>
MEM_B_DQS_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<4>

MEM_B_DQ<31> MAKE_BASE=TRUE =MEM_B_DQ<32>
MEM_B_DQ<30> MAKE_BASE=TRUE =MEM_B_DQ<39>
MEM_B_DQ<29> MAKE_BASE=TRUE =MEM_B_DQ<37>
MEM_B_DQ<28> MAKE_BASE=TRUE =MEM_B_DQ<38>
MEM_B_DQ<27> MAKE_BASE=TRUE =MEM_B_DQ<35>
MEM_B_DQ<26> MAKE_BASE=TRUE =MEM_B_DQ<34>
MEM_B_DQ<25> MAKE_BASE=TRUE =MEM_B_DQ<36>
MEM_B_DQ<24> MAKE_BASE=TRUE =MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<3>
MEM_B_DQS_P<4> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<3>

MEM_B_DQ<39> MAKE_BASE=TRUE =MEM_B_DQ<28>
MEM_B_DQ<38> MAKE_BASE=TRUE =MEM_B_DQ<24>
MEM_B_DQ<37> MAKE_BASE=TRUE =MEM_B_DQ<31>
MEM_B_DQ<36> MAKE_BASE=TRUE =MEM_B_DQ<30>
MEM_B_DQ<35> MAKE_BASE=TRUE =MEM_B_DQ<29>
MEM_B_DQ<34> MAKE_BASE=TRUE =MEM_B_DQ<25>
MEM_B_DQ<33> MAKE_BASE=TRUE =MEM_B_DQ<27>
MEM_B_DQ<32> MAKE_BASE=TRUE =MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<2>
MEM_B_DQS_P<5> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<2>

MEM_B_DQ<47> MAKE_BASE=TRUE =MEM_B_DQ<18>
MEM_B_DQ<46> MAKE_BASE=TRUE =MEM_B_DQ<20>
MEM_B_DQ<45> MAKE_BASE=TRUE =MEM_B_DQ<23>
MEM_B_DQ<44> MAKE_BASE=TRUE =MEM_B_DQ<22>
MEM_B_DQ<43> MAKE_BASE=TRUE =MEM_B_DQ<19>
MEM_B_DQ<42> MAKE_BASE=TRUE =MEM_B_DQ<21>
MEM_B_DQ<41> MAKE_BASE=TRUE =MEM_B_DQ<17>
MEM_B_DQ<40> MAKE_BASE=TRUE =MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<1>
MEM_B_DQS_P<6> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<1>

MEM_B_DQ<55> MAKE_BASE=TRUE =MEM_B_DQ<8>
MEM_B_DQ<54> MAKE_BASE=TRUE =MEM_B_DQ<14>
MEM_B_DQ<53> MAKE_BASE=TRUE =MEM_B_DQ<10>
MEM_B_DQ<52> MAKE_BASE=TRUE =MEM_B_DQ<11>
MEM_B_DQ<51> MAKE_BASE=TRUE =MEM_B_DQ<9>
MEM_B_DQ<50> MAKE_BASE=TRUE =MEM_B_DQ<15>
MEM_B_DQ<49> MAKE_BASE=TRUE =MEM_B_DQ<12>
MEM_B_DQ<48> MAKE_BASE=TRUE =MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_N<0>
MEM_B_DQS_P<7> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_DQS_P<0>

MEM_B_DQ<63> MAKE_BASE=TRUE =MEM_B_DQ<2>
MEM_B_DQ<62> MAKE_BASE=TRUE =MEM_B_DQ<1>
MEM_B_DQ<61> MAKE_BASE=TRUE =MEM_B_DQ<3>
MEM_B_DQ<60> MAKE_BASE=TRUE =MEM_B_DQ<7>
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MEM_B_DQ<58> MAKE_BASE=TRUE =MEM_B_DQ<5>
MEM_B_DQ<57> MAKE_BASE=TRUE =MEM_B_DQ<6>
MEM_B_DQ<56> MAKE_BASE=TRUE =MEM_B_DQ<0>

DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

=PP3V3_S3_MEMRESET
R3350 20K 5% 1/16W MF-LF 402
=PP5V_S3_MEMRESET
R3351 20K 5% 1/16W MF-LF 402
R3352 20K 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM
ISOLATE_CPU_MEM_L_R1
Q3306 2N7002DW-X-G SOT-363
Q3306 2N7002DW-X-G SOT-363
=PP1V5_S3_MEMRESET
CPU_MEM_RESET_L
NOSTUFF R3355 0 5% 1/16W MF-LF 402
C3353 0.0022UF 20% 16V CERM 402
R3353 20K 5% 1/16W MF-LF 402
Q3304 2N7002 SOT23-HF1
ISOLATE_CPU_MEM_5V_L
MEM_RESET_L

=PP3V3_S5_MEMRESET
MEM_RESET_HW C3300 0.1UF 20% 16V CERM 402
U3300 74LVC74ABQ DHVQFN
MEM_RESET_HW
PM_SLP_S4_L
PM_SYS_PWRGD
=PP3V3_S3_MEMRESET
PM_SLP_S4_D_L
=PP3V3_S3_MEMRESET
CPU_MEM_RESET3V3_L
PM_SLP_S3_L
PM_SLP_S4_D_L
TP_PM_SLP_S4_D
ISOLATE_CPU_MEMHW_L
TP_ISOLATE_CPU
THRM GND_PAD
R3385 0 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM_L
NOSTUFF R3383 0 5% 1/16W MF-LF 402
ISOLATE_CPU_MEM_L_R1
MEM_RESET_HW R3380 10K 5% 1/16W MF-LF 402
CPU_MEM_RESET_L
CPU_MEM_RESET_R_L

=PP3V3_S5_MEMRESET
MEM_RESET_HW R3381 10K 5% 1/16W MF-LF 402
MEM_RESET_HW R3382 10K 5% 1/16W MF-LF 402
CPU_MEM_RESET3V3
CPU_MEM_RESET3V3_L
MEM_RESET_HW Q3360 2N3904 SOT23-HF
MEM_RESET_HW Q3350 2N7002 SOT23-HF1

NOSTUFF R3390 0 5% 1/16W MF-LF 402
ALL_SYS_PWRGD_R
NOSTUFF R3391 0 5% 1/16W MF-LF 402
PM_EN_DDRVTT_S0_REG
DDRSYS_EN
NOSTUFF C3390 0.1UF 20% 16V CERM 402
=PP3V3_S5_MEMRESET
NOSTUFF MC74VHC1G08 SOT23-5-HF
U3390
NOSTUFF R3393 0 5% 1/16W MF-LF 402
SLP_S3_CTL_L
R3394 0 5% 1/16W MF-LF 402
PM_SLP_S3_L
PM_SLP_S3_5V_R2

=PP5V_S3_MEMRESET
R3387 20K 5% 1/16W MF-LF 402
R3384 20K 5% 1/16W MF-LF 402
PM_SLP_S3_5V
PM_SLP_S3_5V_L
Q3370 2N7002DW-X-G SOT-363
Q3370 2N7002DW-X-G SOT-363

NOSTUFF R3386 0 5% 1/16W MF-LF 402
Q3375 FDMC8296 POWER33
=PP0V75_S0_MEM_VTT_S0FET
PPVTT_S0_DDR_FET
R3340 100K 5% 1/16W MF-LF 402
PM_SLP_S3_5V_L
R3388 10 5% 1/16W MF-LF 402
VTT_R
Q3380 2N7002 SOT23-HF1
PM_SLP_S3_5V

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<0>
MEM_A_CLK_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<0>
MEM_A_CLK_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<1>
MEM_A_CLK_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<1>
MEM_A_CLK_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<2>
MEM_A_CLK_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<2>
MEM_A_CLK_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_P<3>
MEM_A_CLK_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_A_CLK_N<3>

MEM_B_CLK_P<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<0>
MEM_B_CLK_N<0> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<0>
MEM_B_CLK_P<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<1>
MEM_B_CLK_N<1> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<1>
MEM_B_CLK_P<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<2>
MEM_B_CLK_N<2> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<2>
MEM_B_CLK_P<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_P<3>
MEM_B_CLK_N<3> MAKE_BASE=TRUE NO_TEST=TRUE =MEM_B_CLK_N<3>

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: DDR3 SUPPORT AND BITSWAPS

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
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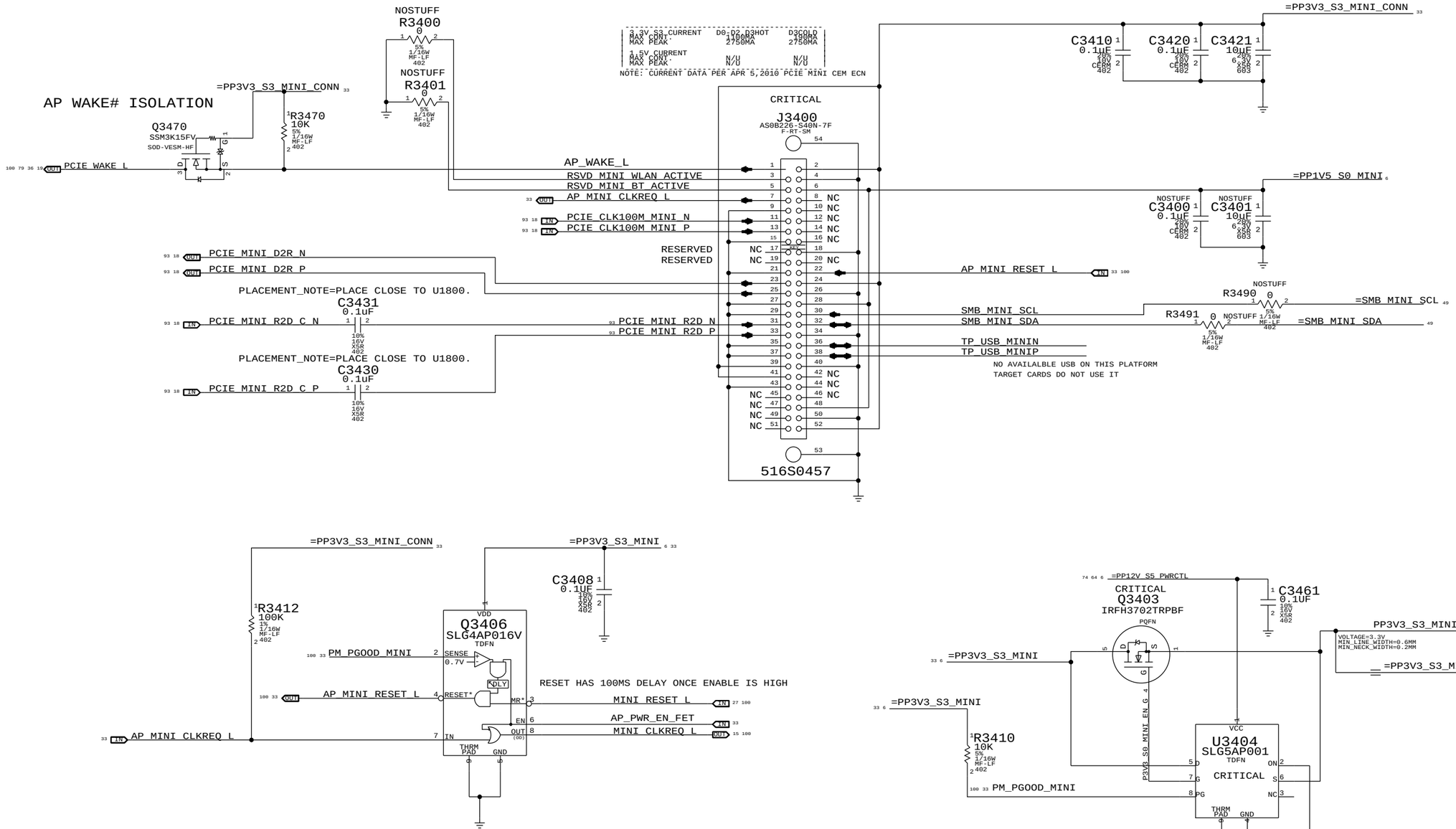

SYNC_MASTER=K62_AARON SYNC_DATE=07/16/2009

PAGE TITLE
PCI-E Wireless Connector

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
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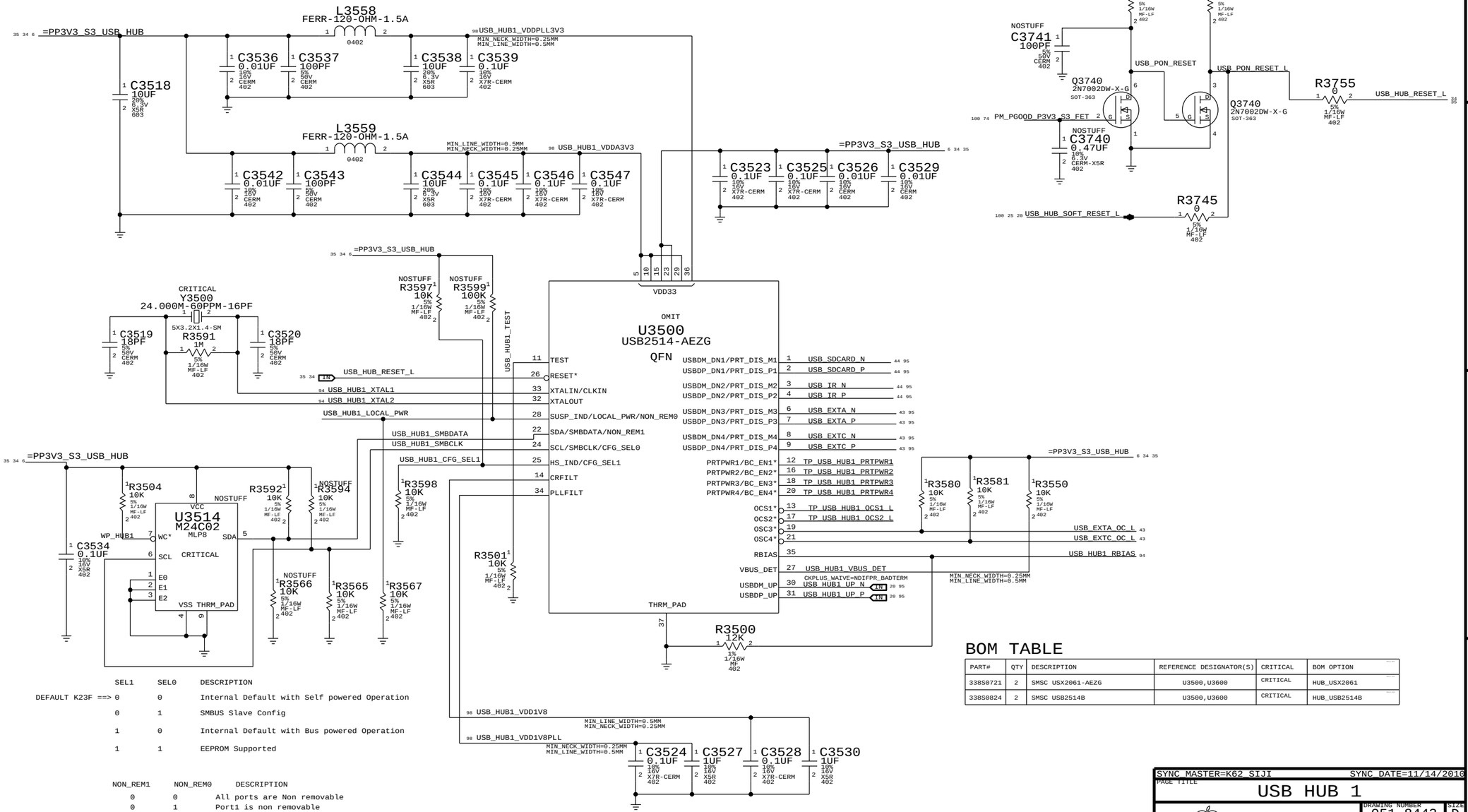
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

SYNC_MASTER=K62_SIJI SYNC_DATE=11/14/2010

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

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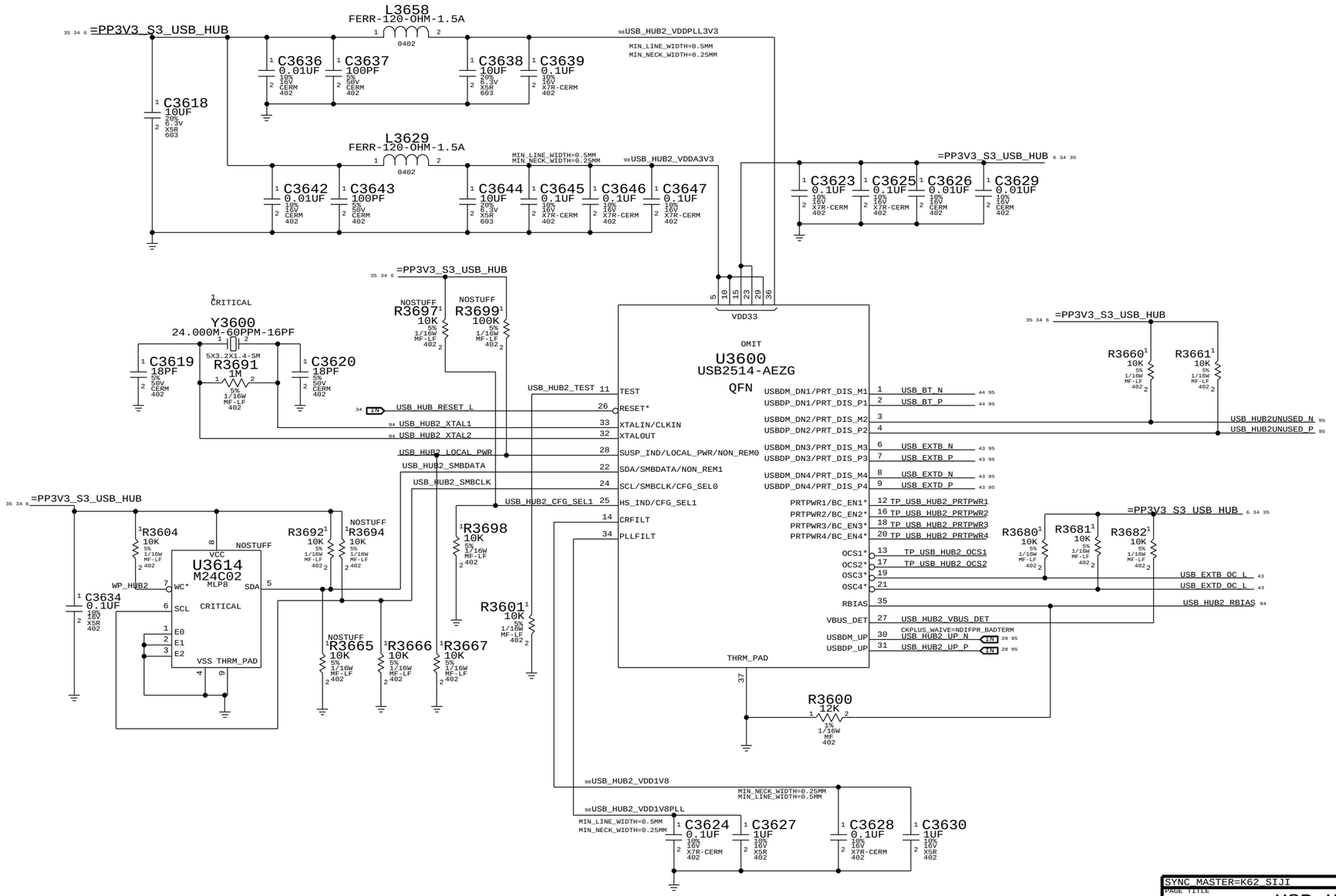
USB HUB-2



SYNC_MASTER=K62_SIJI	SYNC_DATE=11/14/2010
PAGE TITLE: USB HUB 2	
Apple Inc.	DRAWING NUMBER: 051-8442 SIZE: D
	REVISION: 10.1.0
	BRANCH:
	PAGE: 36 OF 110
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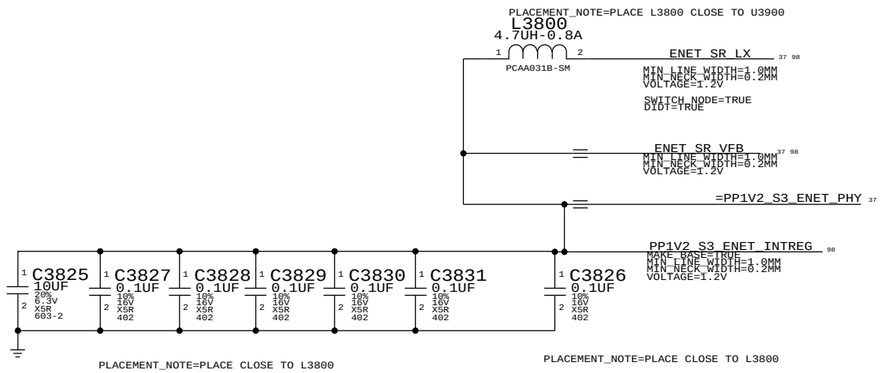
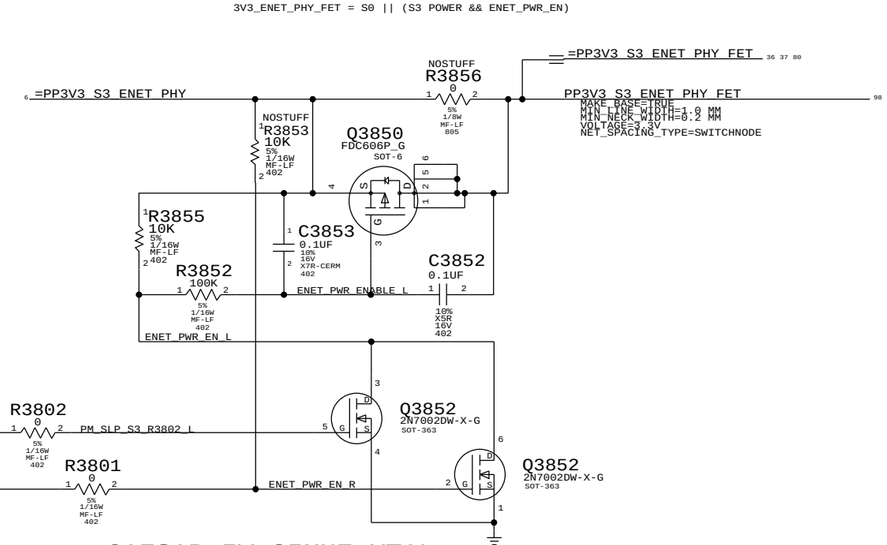
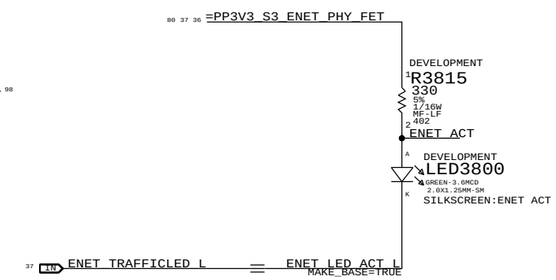
CAESAR IV 1.2V INT.VR CMPTS



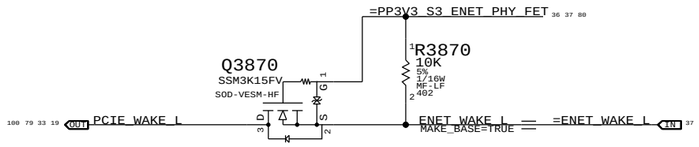
CAESAR IV POWER ENABLE CIRCUIT



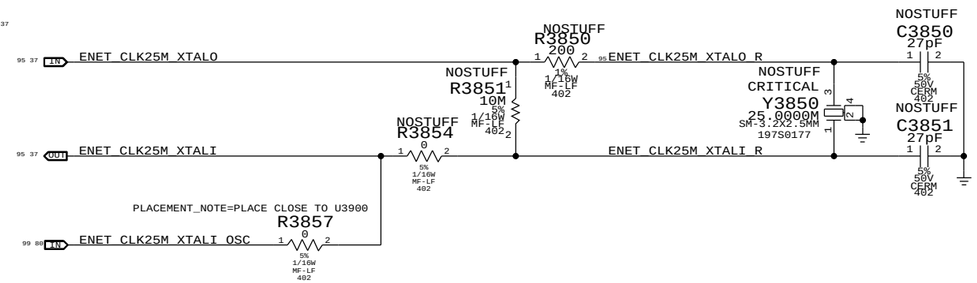
CAESAR IV ACTIVITY LED



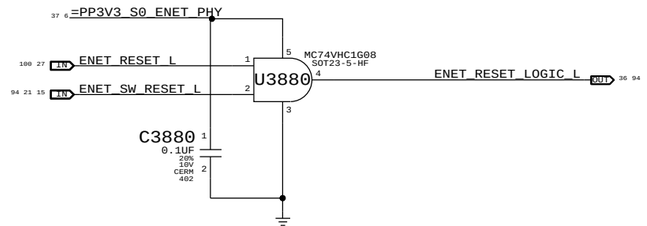
CAESAR IV WAKE# ISOLATION



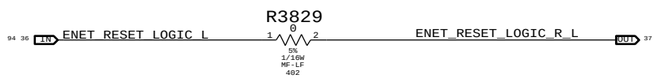
CAESAR IV 25MHZ XTAL



CAESAR IV SW RESET GATING

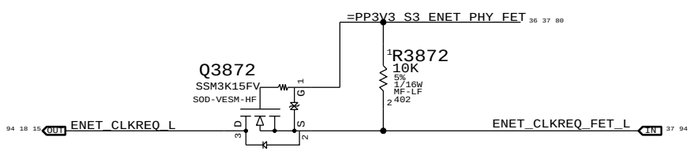


CAESAR IV RESET CONNECTION



CAESAR IV STRAPS (NONE)

CAESAR IV CLKREQ ISOLATION



SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

PAGE TITLE: CAESAR IV SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

=PP3V3_S3_ENET_PHY_FET

R3901 0 5% 1/16W MF-LF 402 — ENET_3V3_S3_SR_IN
SWITCH_NODE=TRUE
DIDT=TRUE
NET_SPACING_TYPE=SWITCHNODE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C3979 4.7UF 20% 6.3V CERM 603
C3980 0.1UF 10% 16V X5R 402
C3981 0.1UF 10% 16V X5R 402

CRITICAL
L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3900 0.1UF 10% 16V X7R-CERM 402
R3900 0 5% 1/16W MF-LF 402 — ENET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

VDD for Card Reader I/O
=PP3V3R1V8_ENET_LR_OUT

CRITICAL
L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3917 0.1UF 10% 16V X7R-CERM 402
C3918 0.1UF 10% 16V X7R-CERM 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

ENET_SR_LX 36 98
ENET_SR_VFB 36 98

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY 36
396mA (1000base-T, Caesar II)

CRITICAL
L3920 FERR-600-OHM-0.5A — PP1V2_S3_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3925 FERR-600-OHM-0.5A — PP1V2_S3_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3930 FERR-600-OHM-0.5A — PP1V2_S3_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT 37
PP3V3R1V8_ENET_LR_OUT_REG 98
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
DEVELOPMENT: C3970 4.7UF 10% 6.3V X5R-CERM 603; C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402 — NOSTUFF R3959 150 5% 1/16W MF-LF 402; NOSTUFF C3959 10PF 5% 50V CERM 402

MUST DO: REMOVE C/R3959 AFTER PROTO 2

=PP3V3_S0_ENET_PHY 36 6
R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_N
C3951 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_P
C3955 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_C_P
C3956 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_C_N
R3943 0 5% 1/16W MF-LF 402 — =ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_LOGIC_R_L
ENET_CLKREQ_FET_L
ENET_WAKE_R_L
ENET_LOW_PWR
ENET_SMB_CLK
ENET_SMB_DATA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
TP_ENET_SPD100LED_L
ENET_TRAFFICLED_L
ENET_CLK25M_XTALI
ENET_CLK25M_XTALO
ENET_RDAC

U3900 BCM57765 QFN-8X8 (OMIT)

58	VMAIN_PRSNT	(IPD-ENET)
27	PCIE_TXD_N	
28	PCIE_TXD_P	
33	PCIE_RXD_P	
34	PCIE_RXD_N	
31	PCIE_REFCLK_P	
30	PCIE_REFCLK_N	
11	PERST*	(IPD)
12	CLKREQ*	(OD)
3	WAKE*	(OD)
4	LOW_PWR	(IPD)
6	SMB_CLK	
10	SMD_DATA	(IPD-ENETM)
66	SCLK	
64	SI/LINKLED*	
65	SO	
63	CS*	
2	SPD100LED*/SERIAL_DO	(OD)
67	TRAFFICLED*/SERIAL_DI	(OD)
18	XTALI	
19	XTALO	
38	RDAC	
69	THRM_PAD	(NO IPU OR IPD-ENET)

42	AVDDH	
48	BIASVDDH	
37	XTALVDDH	
7	VDDO	
20	SR_VDD	
56	SR_VDDP	
62	SR_LX	
14	SR_VFB	
15	AVDDL	
16	PCIE_PLLVDDL	
13	GPHY_PLLVDDL	
39	VDDC	

45	TRD0_P	ENETCONN_MDI_P<0>
51	TRD0_N	ENETCONN_MDI_N<0>
29	TRD1_P	ENETCONN_MDI_P<1>
32	TRD1_N	ENETCONN_MDI_N<1>
36	TRD2_P	ENETCONN_MDI_P<2>
35	TRD2_N	ENETCONN_MDI_N<2>
61	TRD3_P	ENETCONN_MDI_P<3>
	TRD3_N	ENETCONN_MDI_N<3>
5	GPIO_0	NC
8	GPIO_1/CR_BUS_PWR	
9	RE*/GPIO_2	ENET_MEDIA_SENSE
1	SD_DETECT/WE*	ENET_SD_DETECT_L
26	CR_CMD/CLE	ENET_SD_CMD
21	CR_CLK/RY_BY*	ENET_SD_CLK
25	CR_DATA0	ENET_CR_DATA<0>
24	CR_DATA1	ENET_CR_DATA<1>
23	CR_DATA2	ENET_CR_DATA<2>
22	CR_DATA3	ENET_CR_DATA<3>
52	CR_DATA4	ENET_CR_DATA<4>
53	CR_DATA5	ENET_CR_DATA<5>
54	CR_DATA6	ENET_CR_DATA<6>
55	CR_DATA7	ENET_CR_DATA<7>
59	CE*/MS_INS*	NC_ENET_CE_L_MS_INS_L NO_TEST=TRUE
60	CR_LED/ALE	ENET_CR_PWREN
57	CR_WP*/XD_WP*	
68	XD_DETECT	ENET_SR_DISABLE

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

DEVELOPMENT
R3960 0 5% 1/16W MF-LF 402 — SDCONN_DETECT_L
R3961 33 5% 1/16W MF-LF 402 — SDCONN_CMD
R3979 33 5% 1/16W MF-LF 402 — SDCONN_CLK
R3971 33 — SDCONN_DATA<0>
R3972 33 — SDCONN_DATA<1>
R3973 33 — SDCONN_DATA<2>
R3974 33 — SDCONN_DATA<3>
R3975 33 — SDCONN_DATA<4>
R3976 33 — SDCONN_DATA<5>
R3977 33 — SDCONN_DATA<6>
R3978 33 — SDCONN_DATA<7>
PLACEMENT_NOTE=PLACE NEAR U3900

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

SDCONN_WP
R3980 1K 5% 1/16W MF-LF 402 — NOSTUFF
R3981 1K 5% 1/16W MF-LF 402
=PP3V3_S3_ENET_PHY_FET 36 37 80

ENET supports both active-levels for WP.

PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900
PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_S3_ENET_PHY_FET
R3993 4.7K 5% 1/16W MF-LF 402
R3992 4.7K 5% 1/16W MF-LF 402
R3904 0 5% 1/16W MF-LF 402
C3990 0.1UF 10% 16V X7R-CERM 402
U3990 AT45DB021D SOIC-8S1 OMIT_TABLE
VCC, GND
ENET_SCLK, ENET_SCLK_R, ENET_CS_L, ENET_SWP_L, ENET_SRESET_L
SCK, CS*, WP*, RESET*, SI, SO
ENET_MOSI, ENET_MISO
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

R3965 1.24K 1% 1/16W MF-LF 402

SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2013
PAGE TITLE: ETHERNET PHY (CAESAR IV)
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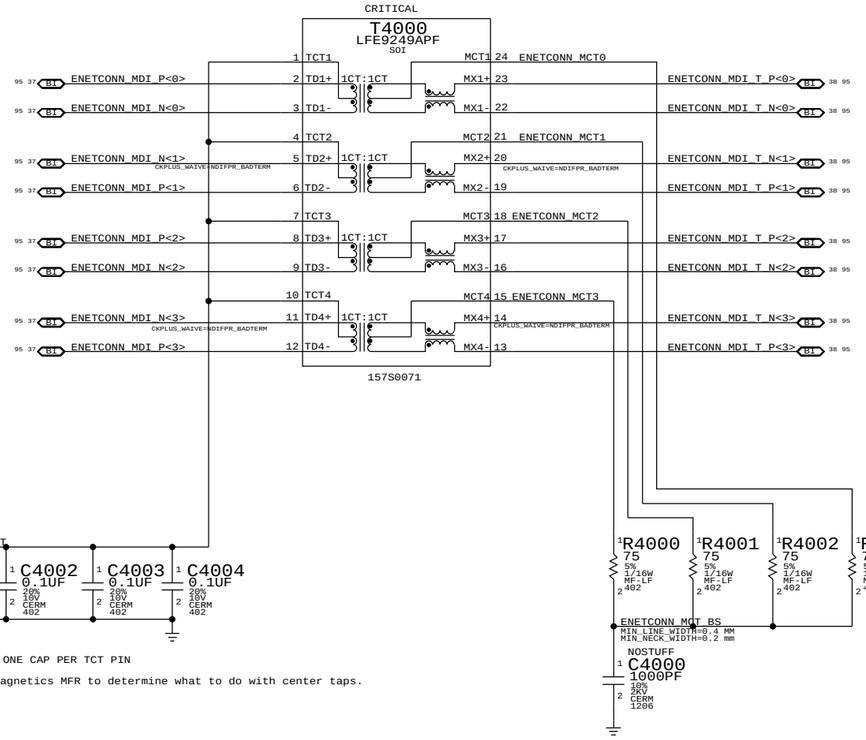
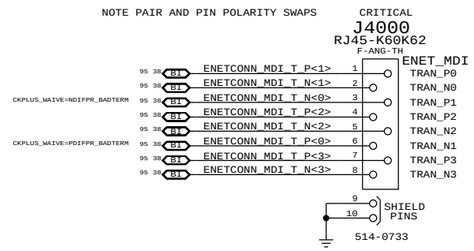
PAGE 39 OF 110
SHEET 37 OF 101

THIS PAGE IS DIFFERENT BETWEEN K60 AND K62.





SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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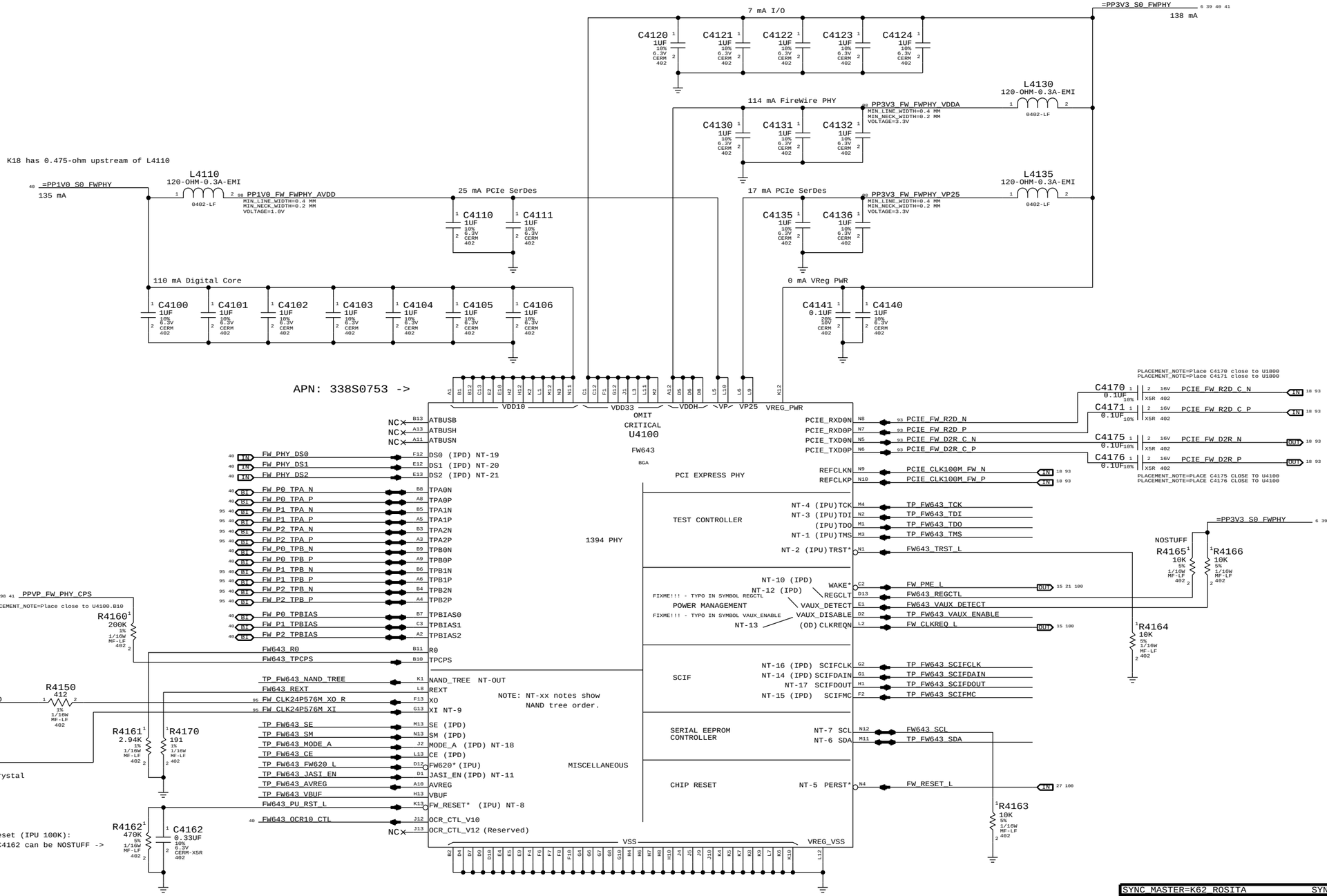

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE
FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
REVISION 10.1.0
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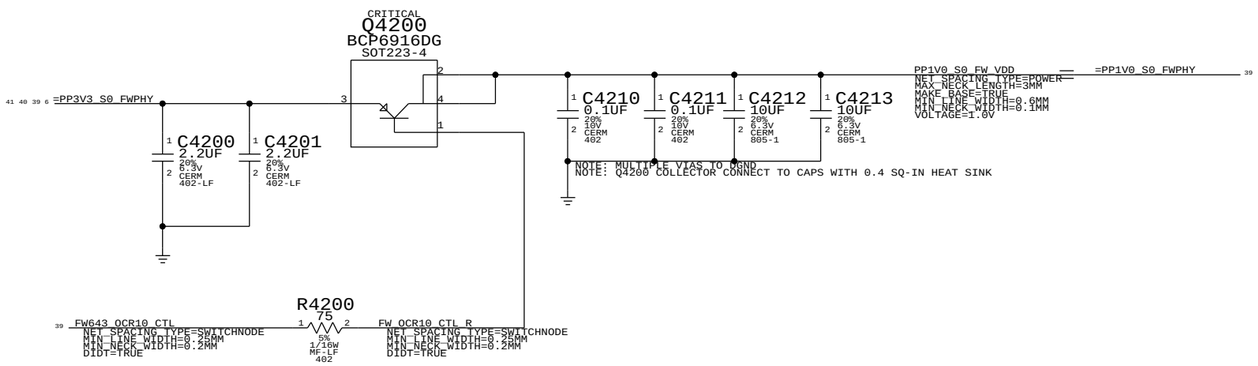
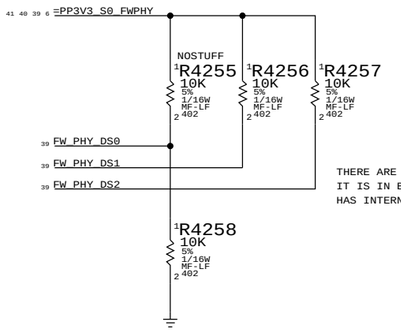
FW643 1.0V GENERATION



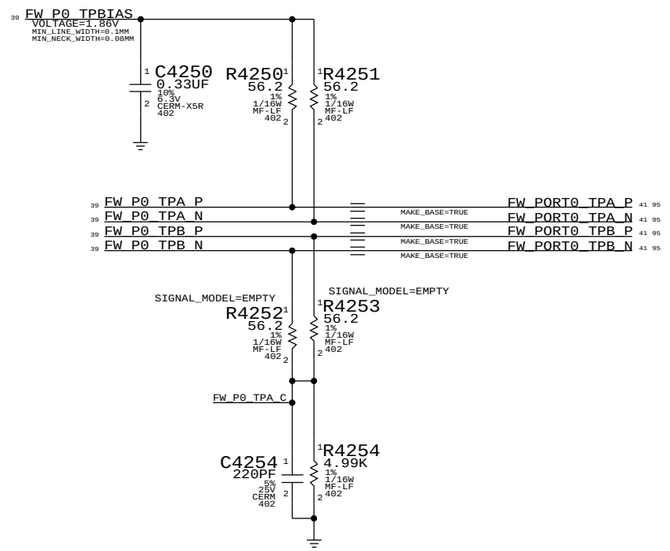
1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBIAS		NC_FW_PORT1_TPBIAS
FW_P1_TPA_P		NC_FW_PORT1_TPA_P
FW_P1_TPA_N		NC_FW_PORT1_TPA_N
FW_P1_TPB_P		NC_FW_PORT1_TPB_P
FW_P1_TPB_N		NC_FW_PORT1_TPB_N
FW_P2_TPBIAS		NC_FW_PORT2_TPBIAS
FW_P2_TPA_P		NC_FW_PORT2_TPA_P
FW_P2_TPA_N		NC_FW_PORT2_TPA_N
FW_P2_TPB_P		NC_FW_PORT2_TPB_P
FW_P2_TPB_N		NC_FW_PORT2_TPB_N

MAKE_BASE=TRUE
NO_TEST=TRUE

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: FireWire: 1394B MISC

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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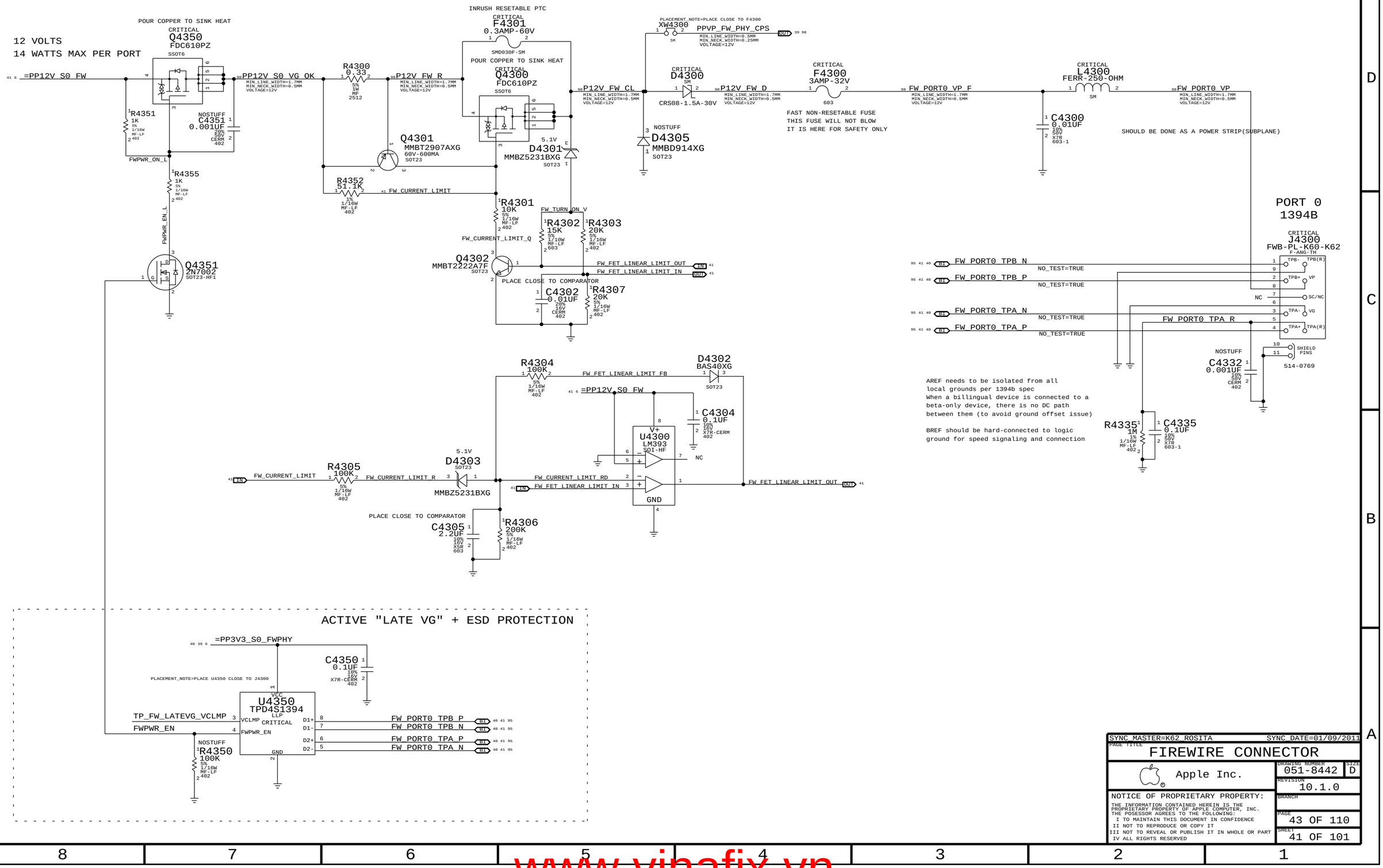

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

PAGE TITLE: FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

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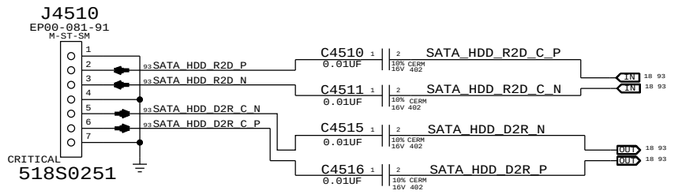
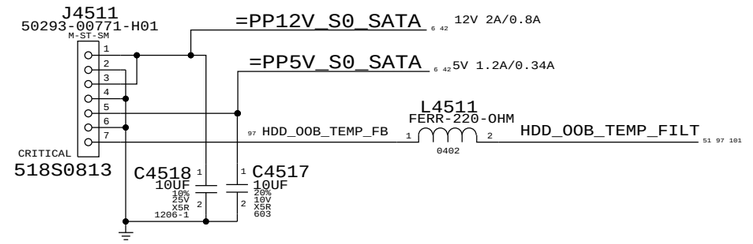
SATA PORT A0 FOR HDD

SILKSCREEN:SATA0



HDD Power

SILKSCREEN:HDD PWR



BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

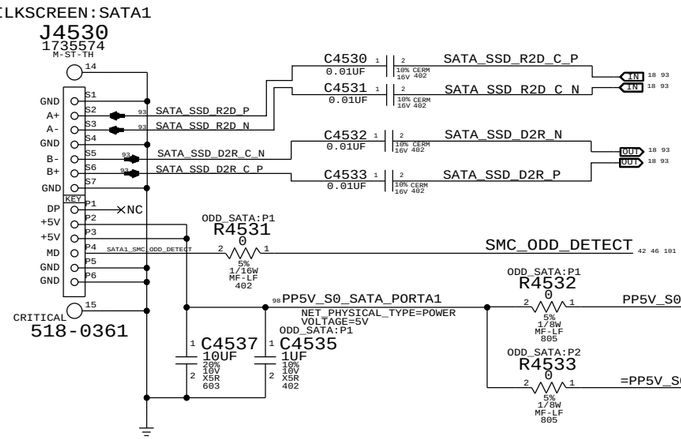
A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT.

5V (SSD) 1.4A/0.8A/0.03A
5V (ODD) 1.5A/1A/0.14A

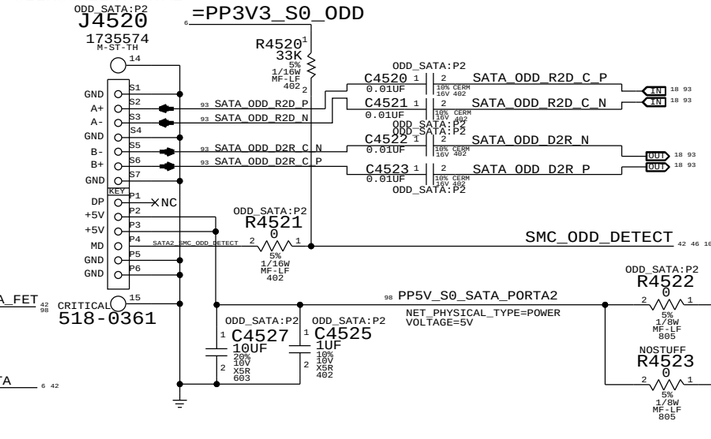
SATA PORT A1 FOR SSD/ODD

SILKSCREEN:SATA1

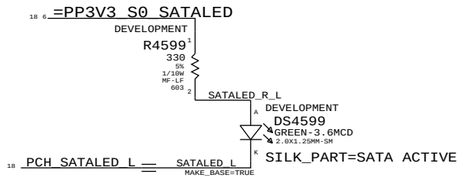


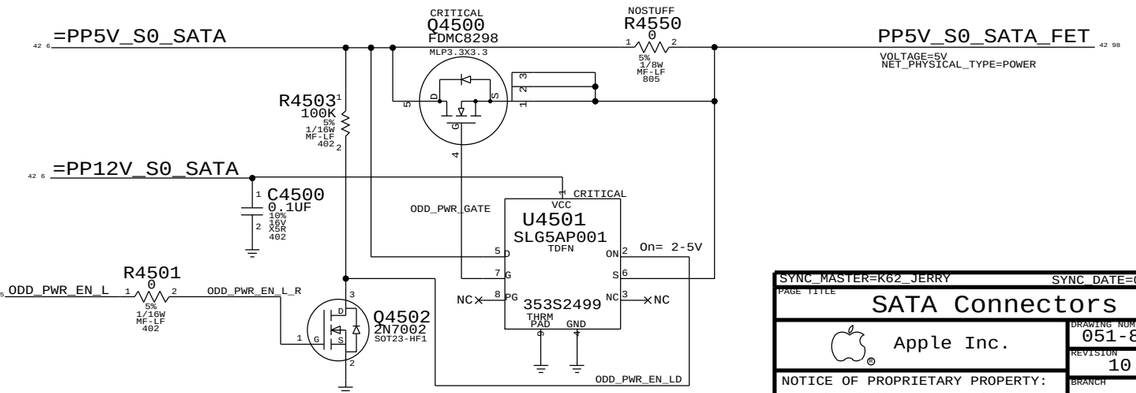
SATA PORT A2 FOR ODD

SILKSCREEN:SATA2



SATA Activity LED





SYNC_MASTER=K62_JERRY	SYNC_DATE=01/09/2011
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USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL

Current Limit at 2.1Amp (@ S3 & S0)

=PP5V_S3_USB

U4600 TPS2561DR SON
IN_0 IN_1 FAULT1* FAULT2* EN1 EN2 GND THRM PAD OUT1 OUT2 ILIM ILIM_IN1

USB_EXTC_OC_L
USB_EXTD_OC_L

C4601 0.1UF 20% 10V CERM 402
C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
R4600 23.2K 1% 1/16W MF-LF 402

Place R4600 very close to ILIM pin

PM_EN_USB_PWR

PP5V_USB_PORT3
155S0329 L4630 FERR-220-OHM-2.5A 0603 CRITICAL
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PP5V_USB_PORT2
155S0329 L4660 FERR-220-OHM-2.5A 0603 CRITICAL
C4603 0.1UF C4630 0.01uF C4661 0.1UF C4660 0.01uF 20% 10V CERM 402

(PUT CAP ON CONNECTOR SIDE)

=PP3V3_G3H_SMCUSBMUX
=PP3V3_S5_SMCUSBMUX
NOSTUFF R4653 0 5% 1/16W MF-LF 402
R4654 0 5% 1/16W MF-LF 402 MOJOMUX:YES

PP3V3_SMCUSBMUX
C4650 0.1UF 20% 10V CERM 402 MOJOMUX:YES

PP5V_USB_PORT3_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

SMC_RX_L
SMC_TX_L
USB_EXTD_P
USB_EXTD_N

U4650 PI3USB102ZLE TQFN
VCC M+ M- D+ D- OE* SEL Y+ Y- GND MOJOMUX:YES

R4651 0 5% 1/16W MF-LF 402
R4652 0 5% 1/16W MF-LF 402 MOJOMUX:NO MOJOMUX:NO

USB_DEBUGPRT_EN_L
SEL=1: CHOOSE USB
SEL=0: CHOOSE SMC

USB_D_MUXED_N
USB_D_MUXED_P

L4631 120-OHM-90MA DLP0NS

USB_PORT3_N
USB_PORT3_P

J4630 USB-K60K62 F-ANG-TH
VBUS DATA- DATA+ GND
514-0768

D4630 RCLAMP0502N SLP1210N6

PORT 3

PP5V_USB_PORT2_F
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V

PP5V_USB_PORT0
155S0329 L4600 FERR-220-OHM-2.5A CRITICAL
C4633 0.1UF C4600 0.01uF 20% 10V CERM 402
VOLTAGE=5V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM

PP5V_USB_PORT0_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

=PP5V_S3_USB

U4620 TPS2561DR SON
IN_0 IN_1 FAULT1* FAULT2* EN1 EN2 GND THRM PAD OUT1 OUT2 ILIM ILIM_IN2

USB_EXTA_OC_L
USB_EXTB_OC_L

C4621 0.1UF 20% 10V CERM 402
C4622 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
R4620 23.2K 1% 1/16W MF-LF 402

Place R4620 very close to ILIM pin

PP5V_USB_PORT1
155S0329 L4620 FERR-220-OHM-2.5A 0603 CRITICAL
C4623 0.1UF C4624 0.01uF 20% 10V CERM 402
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

(PUT CAP ON CONNECTOR SIDE)

PP5V_USB_PORT1_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PORT 2

L4621 120-OHM-90MA DLP0NS
USB_EXTC_N
USB_EXTC_P
USB_PORT2_N
USB_PORT2_P

J4620 USB-K60K62 F-ANG-TH
VBUS DATA- DATA+ GND
514-0768

D4620 RCLAMP0502N SLP1210N6

L4611 120-OHM-90MA DLP0NS
USB_EXTB_N
USB_EXTB_P
USB_PORT1_N
USB_PORT1_P

J4610 USB-MG6-K60-K62 F-ANG-TH
VBUS DATA- DATA+ GND
514-0770

D4610 RCLAMP0502N SLP1210N6

PORT 1

L4601 120-OHM-90MA DLP0NS
USB_EXTA_N
USB_EXTA_P
USB_PORT0_N
USB_PORT0_P

J4600 USB-MG6-K60-K62 F-ANG-TH
VBUS DATA- DATA+ GND
514-0770

D4600 RCLAMP0502N SLP1210N6

PORT 0

USB PORT POWER:

EACH PORT IS HARDWARE Capable of :

STATE	MAX	MIN (WITHIN THE TOLERANCE)
S0, S3	2.7A	2.1A -- PER PORT

WHEN CURRENT HITS LIMIT, TPS2561 BECOME CONSTANT CURRENT MODE AND STAY AT THE LIMIT LEVEL UNTIL THERMAL SHUTDOWN WHEN JUNCTION REACH 130C

SOFTWARE WILL ALOW 500MA/PORT, PLUS 2700MA EXTRA POWER TO BE distributed to approved devices on a 1st-come, 1st-served basis.

EXAMPLE: Port 1 - iPad fast charging = 2100mA
Port 2 - Wired Keyboard = 1100mA
Port 3 - iPhone fast charging = 1000mA
PORT 4 - USB 2.0 500MA = 500MA
TOTAL: 4700MA

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EXTERNAL USB CONNECTORS

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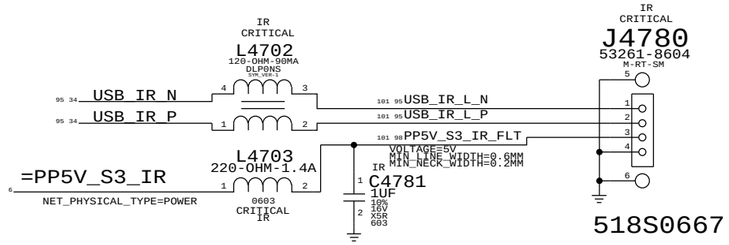
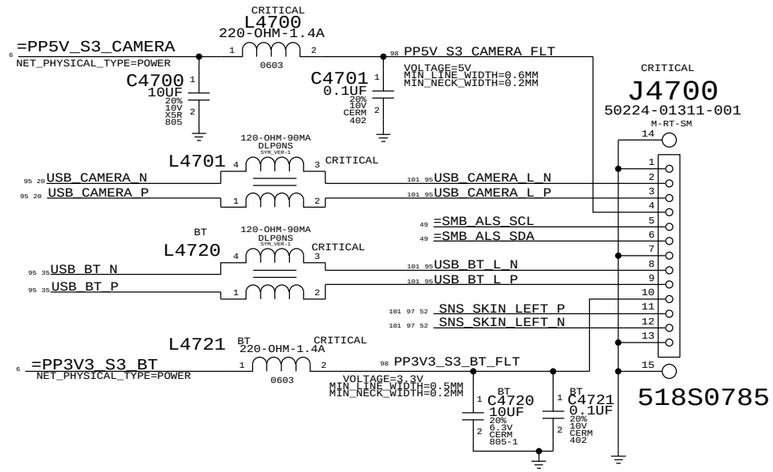
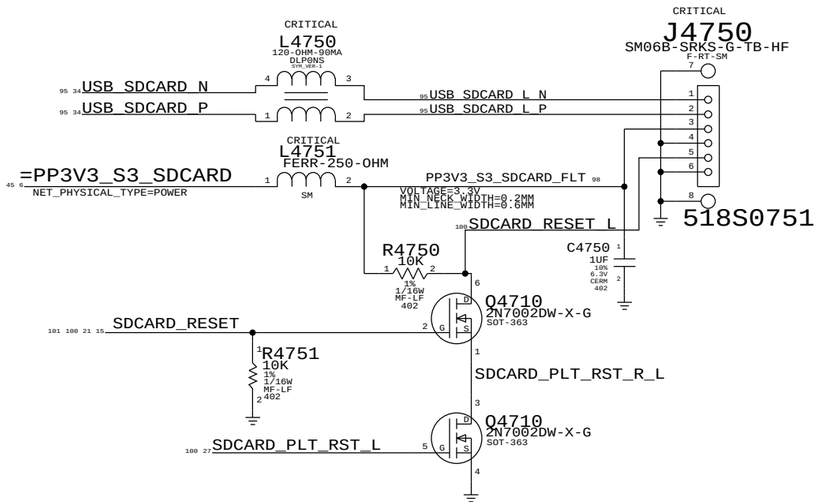
IR RECEIVER CONNECTOR



CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



SD Card Reader Board (Lazarus)



Skin Temp sense at upper Left Screen corner

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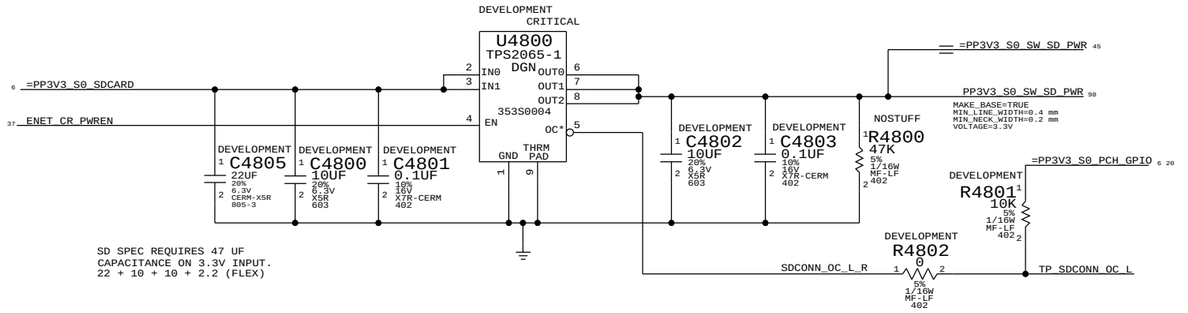
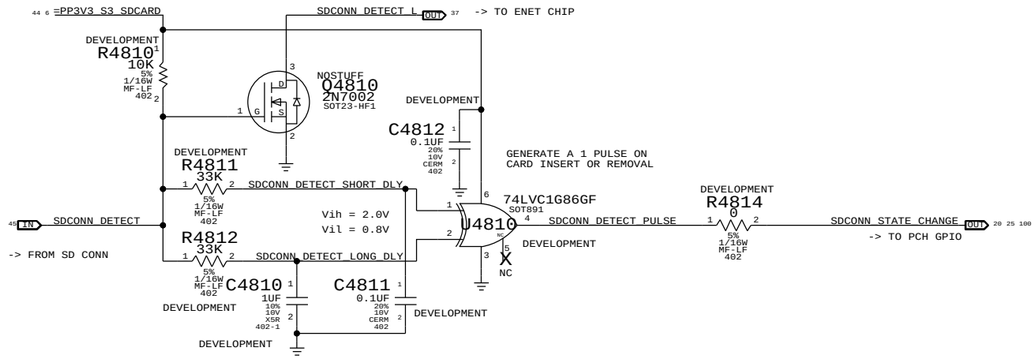
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.

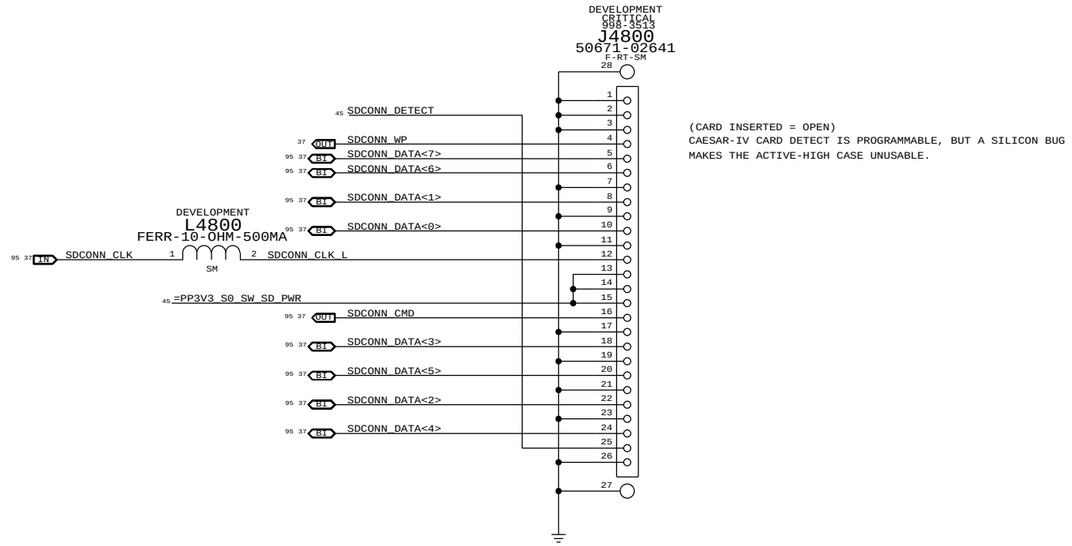


SD SPEC REQUIRES 47 UF
CAPACITANCE ON 3.3V INPUT.
22 + 10 + 10 + 2.2 (FLEX)

SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



SD CARD CONNECTOR



SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

PAGE TITLE: SD READER CONNECTOR

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

U4900
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LFBGA
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OMIT

47 OUT	SMC_EXCARD_PWR_EN	B12	P10		
47 OUT	SMC_RSTGATE_L	C13	P11		
100 64 IN	ALL_SYS_PWRGD_SMC	A15	P12		
100 64 IN	RSMRST_PWRGD	B14	P13		
	NC	B15	P14		
100 27 OUT	PM_RSMRST_L	C14	P15		
47 OUT	CPUIMVP_VR_ON	D12	P16		
100 25 19 OUT	PM_PWRBTN_L	C15	P17		
K62 NEW:NOT USE	NC	D13	P20		
	NC	D14	P21		
	NC	D15	P22		
	NC	E12	P23		
K62 NEW:NOT USE	NC	E14	P24		
	NC	E15	P25		
K62 NEW:NOT USE	NC	E13	P26		
	NC	F14	P27		
94 48 18 BI	LPC_AD<0>	D9	P30		
94 48 18 BI	LPC_AD<1>	C9	P31		
94 48 18 BI	LPC_AD<2>	A9	P32		
94 48 18 BI	LPC_AD<3>	B9	P33		
94 48 18 IN	LPC_FRAME_L	D8	P34		
100 27 IN	SMC_LRESET_L	C8	P35		
94 27 IN	LPC_CLK33M_SMC	A8	P36		
48 18 BI	LPC_SERIRQ	D7	P37		
	NC	A5	P40		
K62 P1 NOT USED, WAS OOB_TEMP	NC	B5	P41		
49 BI	SMB_MGMT_DATA	D5	P42 (OC)		
47 OUT	SMS_ONOFF_L	C3	P43		
	NC	B1	P44		
	NC	C2	P45		
47 OUT	SMC_GFX_THROTTLE_L	D3	P46		
	NC	C1	P47		
48 47 46 43 OUT	SMC_TX_L	G1	P50		
48 47 46 43 IN	SMC_RX_L	G4	P51		
49 BI	SMB_0_S0_CLK	F2	P52 (OC)		

P60	L13	SMC_PM_G2_EN	OUT 75 100		
P61	L14	NC			
P62	L15	NC			
P63	K12	NC			
P64	K13	SMC_ADAPTER_EN	OUT 19 47 100		
P65	K14	NC			
P66	J12	SMC_PROCHOT_3_3_L	IN 47 100		
P67	J13	SMC_BIL_BUTTON_L	IN 47		
P70	N12	SMC_VCORE_ISENSE	IN 50 97 (IMON)		
P71	R13	SMC_VCORE_VSENSE	IN 50 97 (IMON)		
P72	P13	SMC_CPU_1V5_ISENSE	IN 50 97		
P73	R14	SMC_CPU_1V5_VSENSE	IN 50 97		
P74	P14	SMC_VCCSA_ISENSE	IN 50 97		
P75	R15	SMC_VCCSA_VSENSE	IN 50 97		
P76	N13	SMC_VAXG_ISENSE	IN 50 97 (IMON)		
P77	P15	SMC_VAXG_VSENSE	IN 50 97 (IMON)		
P80	C7	SMC_WAKE_SCI_L	OUT 15 18 21 100	PROTO-3, Change back to WAKE_SCI_L	
P81	A7	NC			
P82	B7	PM_CLKRUN_L	OUT 15 19 48 100		
P83	D6	LPC_PWRDWN_L	IN 19 48 100		
P84	C6	SMC_TX_L	OUT 43 46 47 48		
P85	A6	SMC_RX_L	IN 43 46 47 48		
P86	B6	(OC) SMB_MGMT_CLK	BI 49		
P90	K4	SMC_ONOFF_L	IN 47 100		
P91	J2	SMC_BC_ACOK	IN 47		
P92	J1	NC			
P93	J3	PM_SLP_S3_L	IN 5 19 26 32 36 47 63 100		
P94	J4	PM_SLP_S4_L	IN 5 19 32 47 53 100	K60 New Change	
P95	H2	PM_SLP_S5_L	IN 5 19 47 63 100	K60 New Change	
P96	H1	PM_CLK32K_SUSCLK	IN 9 94 100		
P97	G2	(OC) SMB_0_S0_DATA	BI 49		

U4900
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LFBGA
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OMIT

K62 NEW:NOT USE,PULLED UP	IN SMC_PA0	R3	PA0	PE0	M3
100 18 OUT	SPI_DESCRIPTOR_OVERRIDE_L (OC)	P3	PA1	PE1*	M2
100 27 25 19 OUT	PM_SYSRST_L (OC)	R2	PA2	PE2*	M1
47 43 OUT	USB_DEBUGPRT_EN_L (OC)	N3	PA3	PE3*	L4
47 IN	MEM_EVENT_A_L (OC)	R1	PA4	PE4*	L2
47 IN	MEM_EVENT_B_L (OC)	N2	PA5	PF0	M7
47 BI	SYS_ONEWIRE (OC)	M4	PA6	PF1	P6
100 19 15 OUT	PM_BATLOW_L (OC)	N1	PA7	PF2	R6
	NC	B10	PB0	PF3	N6
PROTO-3:back to K75F	100 47 23 OUT SMC_RUNTIME_SCI_L	A10	PB1	PF4	M6
	101 42 IN SMC_ODD_DETECT	D10	PB2	PF5	R5
K62 NEW:NOT USE,PULLED UP	47 IN (See below) SMC_PB3	A11	PB3	PF6	P5
	97 51 IN SMC_HDD_OOB_TEMP	B11	PB4	PF7	N5
	NC	C11	PB5	PG0	P9
K62 NEW:NOT USE,PULLED UP	IN SMC_PB6	A12	PB6	PG1	R9
47 IN	SMC_GFX_OVERTEMP_L	D11	PB7	PG2	N9
53 OUT	SMC_FAN_0_CTL	G14	PC0	PG3	P8
53 OUT	SMC_FAN_1_CTL	G15	PC1	PG4	R8
	NC	G13	PC2	PG5	M8
54 OUT	SMC_FAN_3_CTL	G12	PC3	PG6	P7
53 IN	SMC_FAN_0_TACH	H14	PC4	PG7	R7
53 IN	SMC_FAN_1_TACH	H15	PC5	PH0	E1
	NC	H13	PC6	PH1	F3
54 IN	SMC_FAN_3_TACH	H12	PC7	PH2	K2
(IMON) 97 50 IN	SMC_1V05_ISENSE	M11	PD0	PECI	PH3 C4
(IMON) 97 50 IN	SMC_1V05_VSENSE	P11	PD1	PEVref	PH4 D4
97 50 IN	SMC_PCH_1V05_ISENSE	R11	PD2	PEVSTP	PH5 B3
97 50 IN	SMC_PCH_1V05_VSENSE	N11	PD3		
97 50 IN	SMC_GPU_ISENSE	P10	PD4		
97 50 IN	SMC_GPU_VSENSE	R10	PD5		
97 50 IN	SMC_DIMM_ISENSE	N10	PD6		
97 50 IN	SMC_DIMM_VSENSE	M10	PD7		

SMC_PE0	IN 47	K62 NEW:NOT USE,PULLED UP		
SMC_TCK	IN 47 48			
SMC_TDI	IN 47 48			
SMC_TDO	OUT 47 48			
SMC_TMS	IN 47 48			
G3_POWERON_L	IN 47			
SMC_SYS_LED	OUT 47			
SMC_LID	47			
NC				
NC				
BDV_BKL_PWM	OUT 84 100	K62 PROTO-2:NEW		
NC				
NC				
NC				
SMC_SMS_INT	IN 47			
(OC) SMB_BSA_DATA	BI 49			
(OC) SMB_BSA_CLK	BI 49			
(OC) SMB_A_S3_DATA	BI 49			
(OC) SMB_A_S3_CLK	BI 49			
(OC) SMB_B_S0_DATA	BI 49			
(OC) SMB_B_S0_CLK	BI 49			
SMC_PROCHOT	OUT 47 100			
SMC_THRMTRIP	OUT			
NC				
109 CPU_PECI_R		R4910 0 MF-LF 5% 402 1/16W	CPU_PECI	11 21 100
PVCCIO_S0_SMC_R		R4911 0 MF-LF 5% 402 1/16W	=PPVCCIO_S0_SMC	6 47
108 PM_PECI_PWRGD_R		R4912 0 MF-LF 5% 402 1/16W	PM_PECI_PWRGD	64 100

C4910 0.1UF 20% 10V CERM 402

SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

98 47 46 PP3V3_G3H_AVREF_SMC Peak/Ave/Standby = 2mA/1mA/5uA
47 46 6 =PP3V3_G3H_SMC Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

R4999 4.7 5% 1/16W MF-LF 402

98 46 PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V

PLACEMENT_NOTE=Place C4907 close to U4900 pin 13

C4907 0.47UF 10% 6.3V CERM-XSR 402

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place R4999 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76

U4900
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LFBGA
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OMIT

AVCC	N14		
VCC	A1 P1 J15		
VCL	F1 M14		
AVREF			
100 48 47 IN SMC_RESET_L	E3	RES*	
97 47 SMC_XTAL	A2	XTAL	
97 47 SMC_EXTAL	B2	EXTAL	
MD1	E2		SMC_MD1 IN 48
MD2	K1		SMC_KBC_MDE
NMI	F4		SMC_NMI IN 48
ETRST*	L1		SMC_TRST_L IN 48
AVSS	R12		NOSTUFF
VSS	D2 P4 F12 B13 A4		

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402

XW4900 SM

GND_SMC_AVSS 46 47 50 97

98 47 46 PP3V3_G3H_AVREF_SMC
47 46 6 =PP3V3_G3H_SMC
98 46 PP3V3_G3H_SMC_AVCC

U4900
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OMIT

AVCC1	M15		
VCC3	P2		
AVREF1	M15		
E4		PJ0	C5 NC
N4		PJ1	B8 NC
M9		PJ2	C10 NC
M12	NC	PJ3	C12 NC
M13		PJ4	A14 NC
L12		PJ5	F15 NC
A3		PJ6	J14 NC
		PJ7	K15 NC
		PI0	N8 NC
		PI1	N7 NC
		PI2	M5 NC
		PI3	L3 NC
		PI4	K3 NC
		PI5	H3 NC
		PI6	H4 NC
		PI7	G3 NC
AVSS1	P12		
VSS	R4 F13 A13 B4 D1		

97 50 47 46 GND_SMC_AVSS

SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

PAGE TITLE: SMC

Apple Inc.

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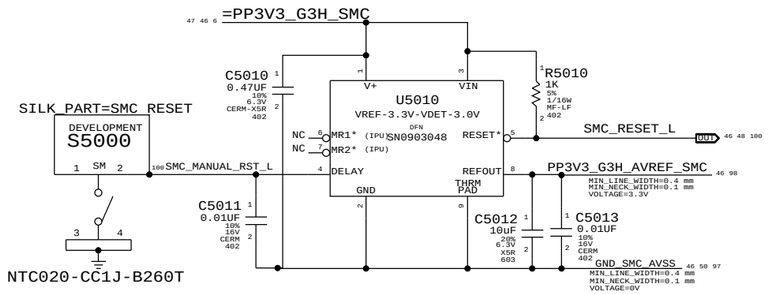
SMC Reset "Button", Supervisor & AVREF Supply



MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L ═ MXM_ALERT_L (MAKE_BASE=TRUE)
SMC_GFX_THROTTLE_L ═ MXM_PWR_LEVEL (MAKE_BASE=TRUE)
CPUIMVP_VR_ON ═ SMC_DELAYED_PWRGD (MAKE_BASE=TRUE)

UNUSED PORT 7 ANALOG SENSORS

UNUSED TP/NC ALIASES

SMC_EXCARD_PWR_EN ═ TP_SMC_EXCARD_PWR_EN (MAKE_BASE=TRUE)
SMS_ONOFF_L ═ TP_SMS_ONOFF_L (MAKE_BASE=TRUE)
SMC_RSTGATE_L ═ TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)
SMC_SYS_LED ═ TP_SMC_SYS_LED (MAKE_BASE=TRUE)
SMC_PB3 ═ TP_SMC_PB3 (MAKE_BASE=TRUE)

=PP3V3_G3H_SMC

SMC_ONOFF_L	R5020	10K	5% 1/16W MF-LF 402
SMC_TX_L	R5021	10K	5% 1/16W MF-LF 402
SMC_RX_L	R5022	100K	5% 1/16W MF-LF 402
SYS_ONEWIRE	R5023	2.0K	5% 1/16W MF-LF 402
SMC_TMS	R5024	10K	5% 1/16W MF-LF 402
SMC_TDO	R5025	10K	5% 1/16W MF-LF 402
SMC_TDI	R5026	10K	5% 1/16W MF-LF 402
SMC_TCK	R5027	10K	5% 1/16W MF-LF 402
SMC_BIL_BUTTON_L	R5028	10K	5% 1/16W MF-LF 402
SMC_BC_ACOK	R5029	10K	5% 1/16W MF-LF 402
SMC_ADAPTER_EN	R5030	10K	5% 1/16W MF-LF 402
USB_DEBUGPRT_EN_L	R5031	10K	5% 1/16W MF-LF 402
G3_POWERON_L	R5034	10K	5% 1/16W MF-LF 402
SMC_SMS_INT	R5032	10K	5% 1/16W MF-LF 402
SMC_LID	R5033	10K	5% 1/16W MF-LF 402
SMC_PA0	R5037	100K	5% 1/16W MF-LF 402
SMC_PB6	R5038	100K	5% 1/16W MF-LF 402
SMC_PE0	R5036	100K	5% 1/16W MF-LF 402

=PP3V3_S0_SMC_LS

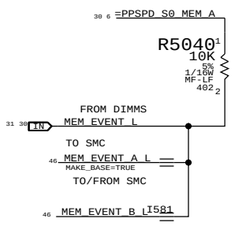
SMC_GFX_OVERTEMP_L	R5035	10K	5% 1/16W MF-LF 402
SMC_RUNTIME_SCI_L	R5044	10K	5% 1/16W MF-LF 402

PM_SLP_S3_L	R5041	100K	5% 1/16W MF-LF 402
PM_SLP_S5_L	R5042	100K	5% 1/16W MF-LF 402
PM_SLP_S4_L	R5043	100K	5% 1/16W MF-LF 402

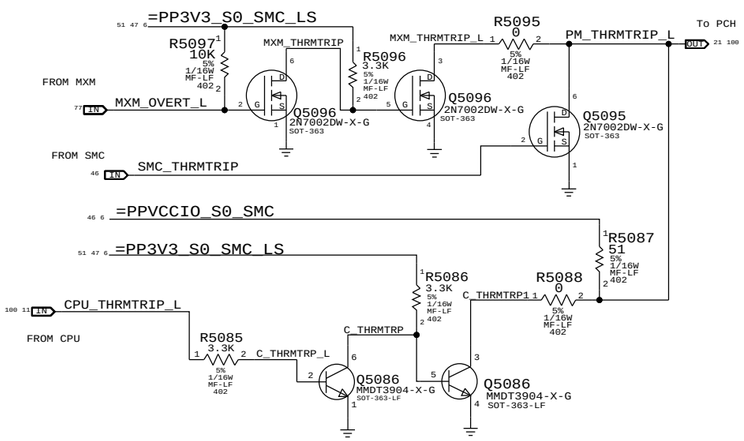
SMC Crystal Circuit

POWER BUTTON

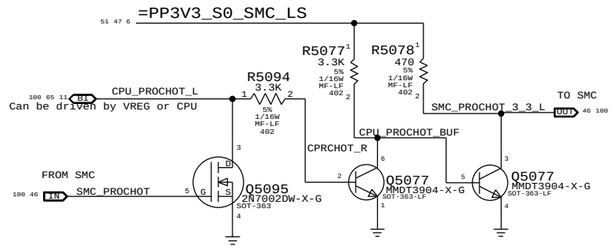
MEM_EVENT



SMC & MXM THERMTRIP LEVEL SHIFTING



SMC PROCHOT 3.3V LEVEL SHIFTING



SYNC_MASTER=K62_JERRY	SYNC_DATE=01/09/2011
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-8442 · SIZE D
	REVISION 10.1.0
	BRANCH
	PAGE 50 OF 110
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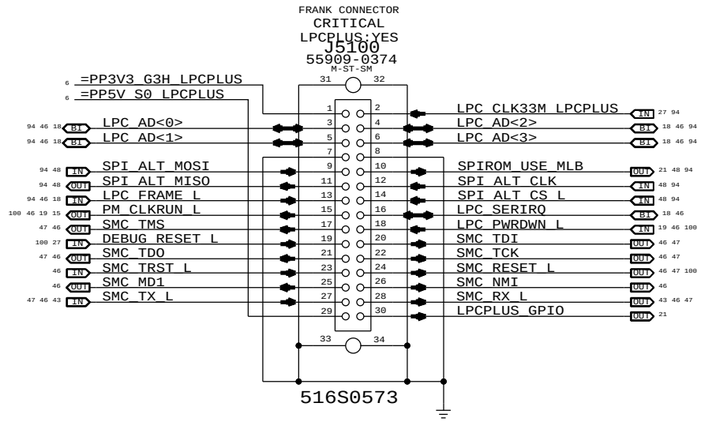
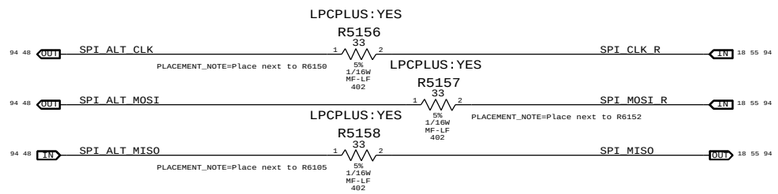
LPC+SPI Connector



Alternate SPI ROM Support

SPI Bus Series Resistance Option



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

REVISION: 10.1.0

BRANCH:

PAGE: 51 OF 110

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PCH "SMBUS" CONNECTIONS

=PP3V3_S0_SMBUS (49, 6)

PCH U1800 (MASTER)
- SMBUS_PCH_CLK (97, 18) — MAKE_BASE=TRUE
- SMBUS_PCH_DATA (97, 18) — MAKE_BASE=TRUE

R5208[1] 2.2K 5% 1/16W MF-LF 402 (2)
R5209[1] 2.2K 5% 1/16W MF-LF 402 (2)

MEMORY A DIMMS J3100-A/B
(DIMM0: WRITE: 0XA0 READ: 0XA1)
(DIMM2: WRITE: 0XA2 READ: 0XA3)
- =I2C_SODIMMA_SCL (30)
- =I2C_SODIMMA_SDA (30)

MEMORY B DIMMS J3200-A/B
(DIMM1: WRITE: 0XA4 READ: 0XA5)
(DIMM3: WRITE: 0XA6 READ: 0XA7)
- =I2C_SODIMMB_SCL (31)
- =I2C_SODIMMB_SDA (31)

XDP (PCH) J2550
- =SMBUS_XDP_SCL (49, 25)
- =SMBUS_XDP_SDA (49, 25)

MIKEY U6806
(WRITE: 0X72 READ: 0X73)
- =I2C_AUDIO_SCL (62)
- =I2C_AUDIO_SDA (62)

XDP (CPU) J2500
- =SMBUS_XDP_SCL (49, 25)
- =SMBUS_XDP_SDA (49, 25)

CK505 U2600
(WRITE: 0XD2 READ: 0XD3)
- =SMBUS_CK505_SCL (26)
- =SMBUS_CK505_SDA (26)

SPTX BLC MICRO VIA J602
(WRITE: 0X6E READ: 0X6F)
- =SMB_BLC_PCH_SCL (6)
- =SMB_BLC_PCH_SDA (6)

NEED TO ADD PCH_SDA ISOLATION CIRCUITRY

MEM VREF MARGIN A U2900
(WRITE: 0X5C READ: 0X5D)
- =I2C_VREFMRGN_A_SCL (28)
- =I2C_VREFMRGN_A_SDA (28)

MEM VREF MARGIN B U2910
(WRITE: 0X7C READ: 0X7D)
- =I2C_VREFMRGN_B_SCL (28)
- =I2C_VREFMRGN_B_SDA (28)

DP SDRV "A" U9310, PS8301
(WRITE: 0X94, READ: 0X95)
- =I2C_DPSDRVA_SCL (85)
- =I2C_DPSDRVA_SDA (85)

DP SDRV "B" U9510, PS8301
(WRITE: 0XB4, READ: 0XB5)
- =I2C_DPSDRVB_SCL (87)
- =I2C_DPSDRVB_SDA (87)

PCH "SML 1" CONNECTIONS

=PP3V3_S0_SMBUS (49, 6)

PCH (FOR TEMP) U1800 (SLAVE)
(WRITE: 0X86 READ: 0X89)
- SML_PCH_1_CLK (97, 18) — MAKE_BASE=TRUE
- SML_PCH_1_DATA (97, 18) — MAKE_BASE=TRUE

NOSTUFF R5204[1] 8.2K 5% 1/16W MF-LF 402 (2)
NOSTUFF R5205[1] 8.2K 5% 1/16W MF-LF 402 (2)
R5206 0 5% 1/10W MF-LF 402 (1, 2)
R5207 0 5% 1/10W MF-LF 402 (1, 2)

THE PCH address is user programmable by SPI ROM

PCH "SML 0" CONNECTIONS

=PP3V3_S0_SMBUS (49, 6)

PCH U1800 (MASTER)
- SML_PCH_0_CLK (97, 18) — MAKE_BASE=TRUE
- SML_PCH_0_DATA (97, 18) — MAKE_BASE=TRUE

R5202[1] 8.2K 5% 1/16W MF-LF 402 (2)
R5203[1] 8.2K 5% 1/16W MF-LF 402 (2)

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)

=PP3V3_S0_SMBUS_SMC_BSA (6)

SMC U4900 (SLAVE)
- SMB_BSA_CLK (46) — SMBUS_SMC_BSA_SCL (97) MAKE_BASE=TRUE
- SMB_BSA_DATA (46) — SMBUS_SMC_BSA_SDA (97) MAKE_BASE=TRUE

R5280[1] 100K 5% 1/16W MF-LF 402 (2)
R5281[1] 100K 5% 1/16W MF-LF 402 (2)

SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0

=PP3V3_S0_SMBUS_SMC_B (6)

SMC U4900 (MASTER)
- SMB_B_S0_CLK (46) — SMBUS_SMC_B_S0_SCL (97) MAKE_BASE=TRUE
- SMB_B_S0_DATA (46) — SMBUS_SMC_B_S0_SDA (97) MAKE_BASE=TRUE

R5260[1] 2.0K 5% 1/16W MF-LF 402 (2)
R5261[1] 2.0K 5% 1/16W MF-LF 402 (2)

AC/DC PS TEMPS EMC1403-[1,2] : ACDC THRU J600
(WRITE: 0X98 OR 0X9A, READ: 0X99 OR 0X9B)
3 SENSE POINTS - PRIMARY, SECONDARY, AMB
- =SMB_ACDC_SCL (6)
- =SMB_ACDC_SDA (6)

AC/DC PS POWER INA219: ACDC THRU J600
(WRITE: 0X80, READ: 0X81)
OUTPUT VOLTAGE, CURRENT, POWER

SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY

=PP3V3_S0_SMBUS_SMC_0 (6)

Also reserve 0x56 and 0x32 per spec

SMC U4900 (MASTER)
- SMB_0_S0_CLK (46) — SMBUS_SMC_0_S0_SCL (97) MAKE_BASE=TRUE
- SMB_0_S0_DATA (46) — SMBUS_SMC_0_S0_SDA (97) MAKE_BASE=TRUE

R5250[1] 2.2K 5% 1/16W MF-LF 402 (2)
R5251[1] 2.2K 5% 1/16W MF-LF 402 (2)

MXM TEMP GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
EMC1402 ON AMD MXM CARD (WRITE: 0X98 READ: 0X99)
- =SMB_MXM_THRM_SCL (77)
- =SMB_MXM_THRM_SDA (77)

EMC1414: U5520
DEV: CPU_D,CPU_HTSK
(WRITE: 0X78 READ: 0X79)
EMC1428: U5500
PROD: AMB,L_SKIN,R_SKIN,ODD, LCD,CPU_PROX,MXM_TEMPS
(WRITE: 0X92 READ:0X93)
- =SMB_SNS1_SCL (52)
- =SMB_SNS1_SDA (52)

PCIE MINI-CARD X18 WI-FI MODULE
TMP106: J3400
(WRITE: 0X90 READ: 0X91)
- =SMB_MINI_SCL (33)
- =SMB_MINI_SDA (33)

SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

=PP3V3_S3_SMBUS_SMC_A (6)

SMC U4900 (MASTER)
- SMB_A_S3_CLK (46) — SMBUS_SMC_A_S3_SCL (97) MAKE_BASE=TRUE
- SMB_A_S3_DATA (46) — SMBUS_SMC_A_S3_SDA (97) MAKE_BASE=TRUE

R5270[1] 4.7K 5% 1/16W MF-LF 402 (2)
R5271[1] 4.7K 5% 1/16W MF-LF 402 (2)

ALS (WRITE: 0X52 READ: 0X53)
- =SMB_ALS_SCL (44)
- =SMB_ALS_SDA (44)

SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

=PP3V3_S0_SMBUS_SMC_MGMT (6)

SMC U4900 (MASTER)
- SMB_MGMT_CLK (46) — SMBUS_SMC_MGMT_SCL (97) MAKE_BASE=TRUE
- SMB_MGMT_DATA (46) — SMBUS_SMC_MGMT_SDA (97) MAKE_BASE=TRUE

R5290[1] 2.2K 5% 1/16W MF-LF 402 (2)
R5291[1] 2.2K 5% 1/16W MF-LF 402 (2)

PANEL TEMP SENSOR TMP421 ON TCON BOARD VIA J9002
(SLAVE)
(WRITE: 0X9E READ: 0X9F)
- SMB_DP_TCON_SLA_SCL (82)
- SMB_DP_TCON_SLA_SDA (82)

DISPLAY TCON PARADE ON TCON BOARD VIA J9002
(SLAVE)
(TBD WRITE: 0X1A READ: 0X1B)
(TO READ VENDOR ID AND PANEL ID)
TCON ALSO HAS MASTER BUS TO LUT ROM AND EDID ROM.

DISPLAY TCON TO SPTX OR O2M BLC

=PP3V3_S0_SMBUS (49, 6)

DISPLAY TCON VIA J9002 (MASTER)
- =SMB_DP_TCON_SDA — MAKE_BASE=TRUE
- =SMB_DP_TCON_SCL — MAKE_BASE=TRUE

R5210[1] 2.2K 5% 1/16W MF-LF 402 (2)
R5211[1] 2.2K 5% 1/16W MF-LF 402 (2)

BLC MICRO VIA J602 (SLAVE)
(WRITE: 0X6E READ: 0X6F)
- SMB_BLC_TCON_SDA (82, 6) — MUX
- SMB_BLC_TCON_SCL (97, 82) — BY

NOTE: DISPLAY TCON HAS 4.7K PU.
NOTE: SPTX BLC HAS 4.7K PU.
NOTE: O2MICRO BLC HAS NO PU.

T29 I2C CONNECTIONS

=PP3V3_S0_T29I2C (6)

I2C BUS PULL-UP RAIL MUST REFLECT WHEN USB POWER (VBUS) IS VALID.

T29 IC U9700 (MASTER)
- I2C_T29_SCL (99, 89) — MAKE_BASE=TRUE
- I2C_T29_SDA (99, 89) — MAKE_BASE=TRUE

T29 R5230[1] 4.7K 5% 1/16W MF-LF 402 (2)
T29 R5231[1] 4.7K 5% 1/16W MF-LF 402 (2)

T29 PORT A MCU U9330
(WRITE: 0X26 READ: 0X27)
- =I2C_T29AMCU_SCL (85)
- =I2C_T29AMCU_SDA (85)

T29 PORT B MCU U9530
(WRITE: 0X24 READ: 0X25)
- =I2C_T29BMCU_SCL (87)
- =I2C_T29BMCU_SDA (87)

SYNC_MASTER=K62_MARK
SYNC_DATE=01/09/2011
PAGE TITLE: SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER	051-8442
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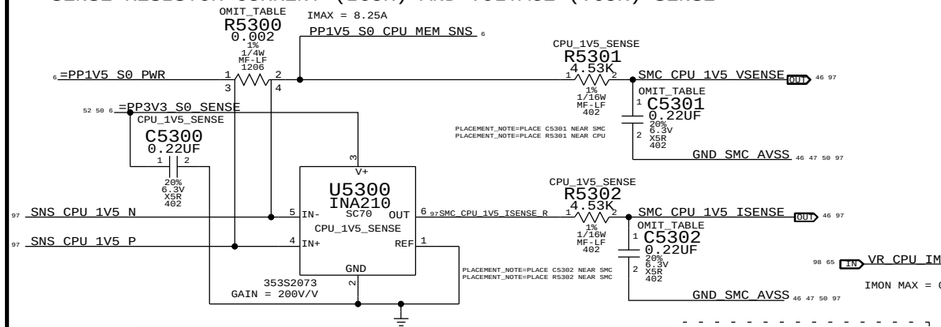
CPU VDD 1.5V

SENSE RESISTOR CURRENT (IC5R) AND VOLTAGE (VC5R) SENSE

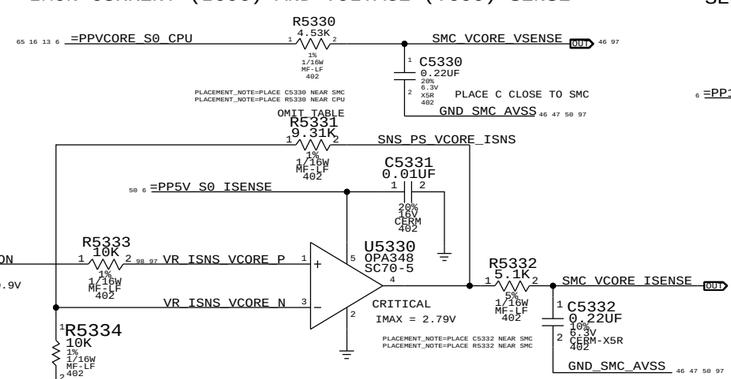


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	NO_CPU_1V5_SENSE
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	NO_CPU_1V5_SENSE

THE NO_1V05_PCH_SENSE,
NO_CPU_VCCSA_SENSE, AND
NO_CPU_1V5_SENSE
COMPOTIONS SHOULD IDEALLY
NEVER BE USED AS TOTAL CPU POWER
SENSING REQUIRES ALL
3 SENSORS.

CPU VCC (VCORE)

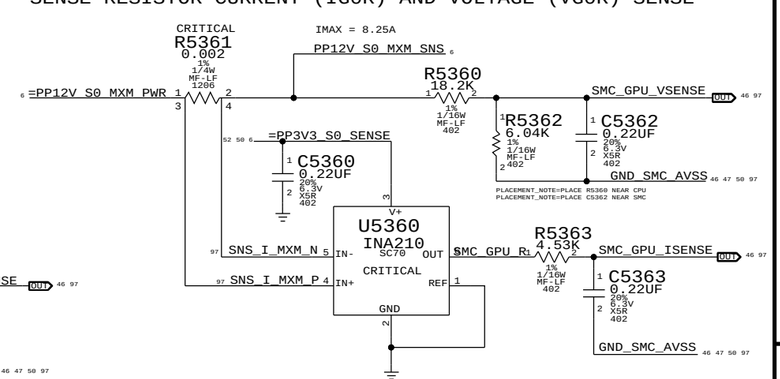
IMON CURRENT (IC0C) AND VOLTAGE (VC0C) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5331	CPUVCORE-3PH
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5331	CPUVCORE-4PH

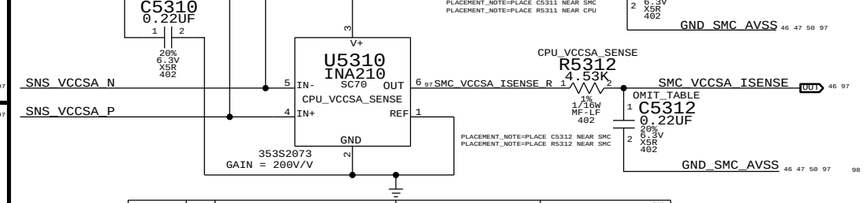
GPU MXM

SENSE RESISTOR CURRENT (IG0R) AND VOLTAGE (VG0R) SENSE



CPU VCCSA

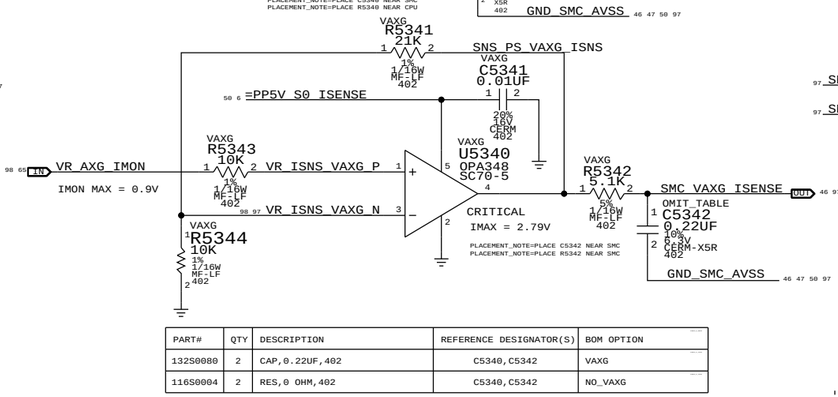
SENSE RESISTOR CURRENT (ICSR) AND VOLTAGE (VCSR) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP,0.22UF,402	C5311,C5312	CPU_VCCSA_SENSE
116S0004	2	RES,0 OHM,402	C5311,C5312	NO_CPU_VCCSA_SENSE

CPU VAXG

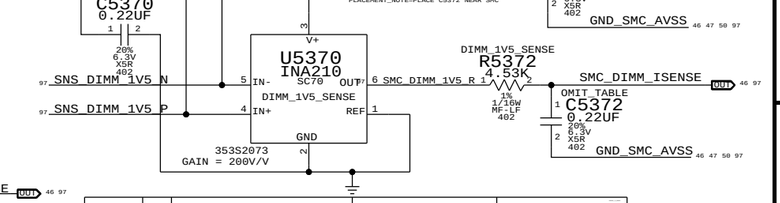
IMON CURRENT (IC0G) AND VOLTAGE (VC0G) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5340,C5342	VAXG
116S0004	2	RES,0 OHM,402	C5340,C5342	NO_VAXG

DIMM VDD 1.5V (LIKELY DEVELOPMENT ONLY)

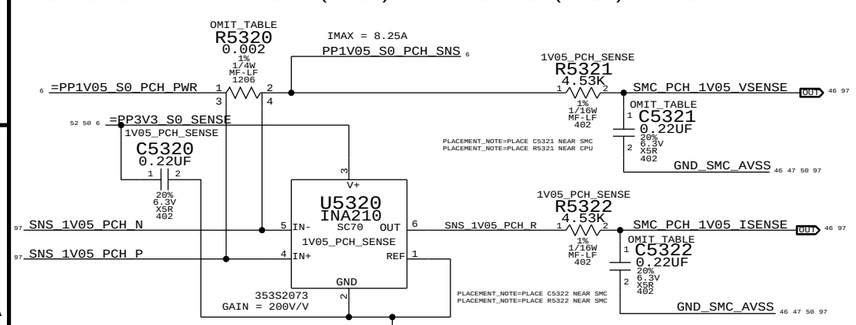
SENSE RESISTOR CURRENT (IM0R) AND VOLTAGE (VM0R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5371,C5372	DIMM_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5371,C5372	PRODUCTION

PCH 1.05V

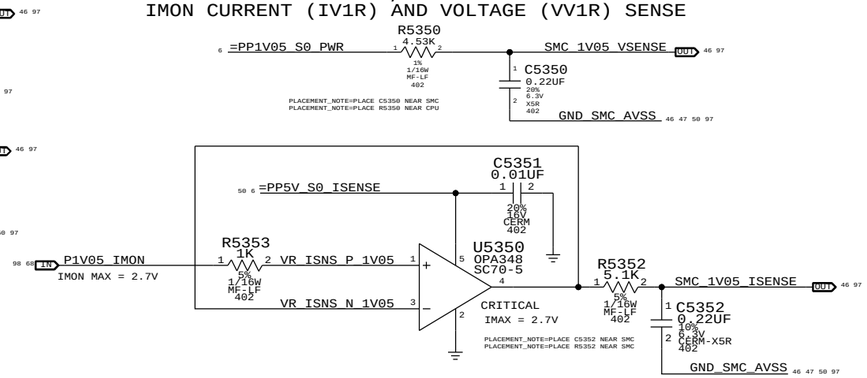
SENSE RESISTOR CURRENT (IN1R) AND VOLTAGE (VN1R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5320	1V05_PCH_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP,0.22UF,402	C5321,C5322	1V05_PCH_SENSE
116S0004	2	RES,0 OHM,402	C5321,C5322	NO_1V05_PCH_SENSE

1.05V FOR CPU VCCIO, CPU VCCSA & PCH 1.05V

IMON CURRENT (IV1R) AND VOLTAGE (VV1R) SENSE



NOTE: TOTAL CPU POWER = VC0C+IC0C
+ VC5R*IC5R
+ VCSR*ICSR
+ VC0G*IC0G
+ VV1R*ICIR

where
ICIR = IV1R - IN1R - ICSR

SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

PAGE TITLE
CPU/PCH/GPU POWER SENSE

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
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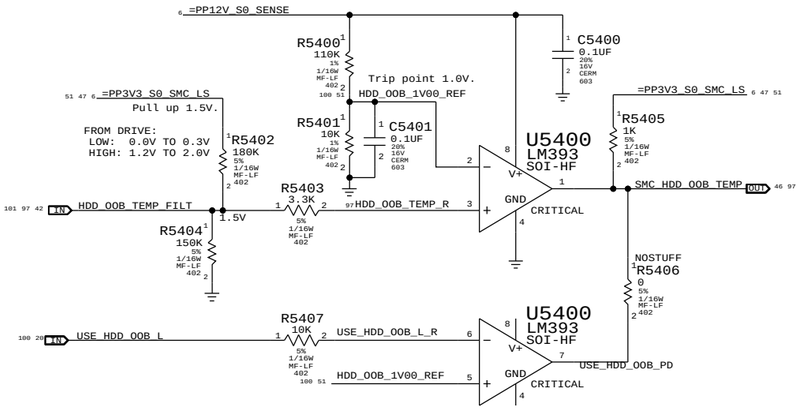
HDD OOB TEMPERATURE SENSING



DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

PAGE TITLE: HDD OOB SENSE

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
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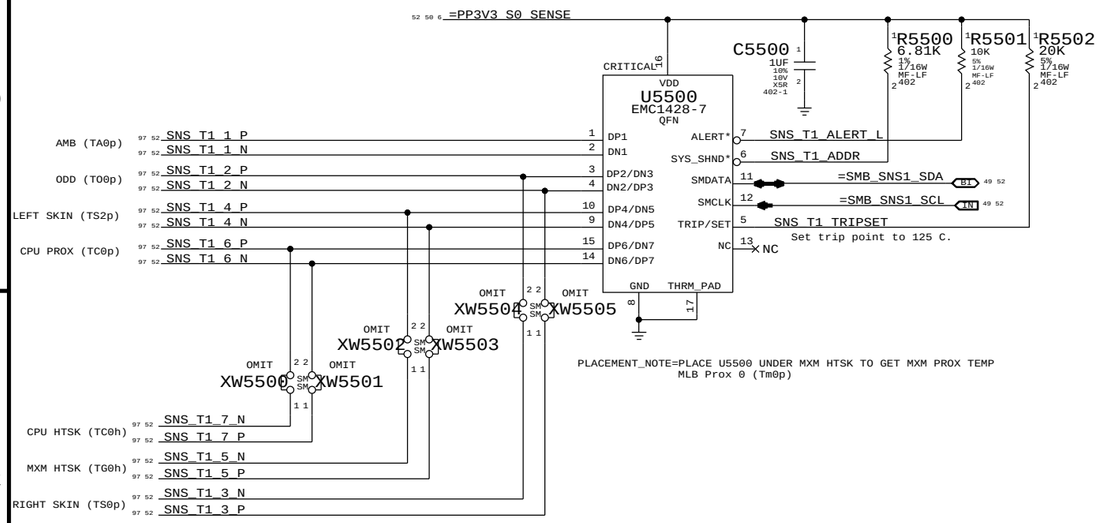
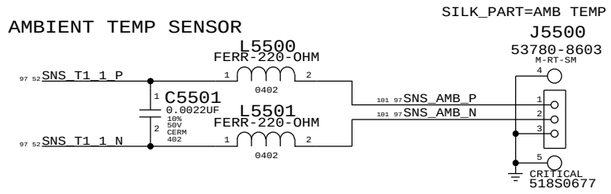
SNS T1: PRODUCTION TEMP SENSOR IC



PLACEMENT_NOTE=PLACE U5500 UNDER MXM HTSK TO GET MXM PROX TEMP
MLB Prox 0 (Tm0p)

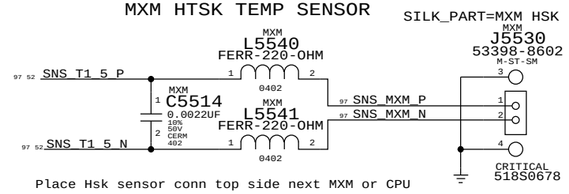
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

AMBIENT TEMP SENSOR



SILK_PART=AMB TEMP

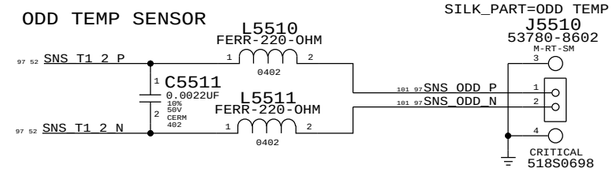
MXM HTSK TEMP SENSOR



SILK_PART=MXM HSK

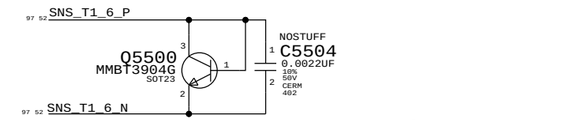
Place Hsk sensor conn top side next MXM or CPU

ODD TEMP SENSOR



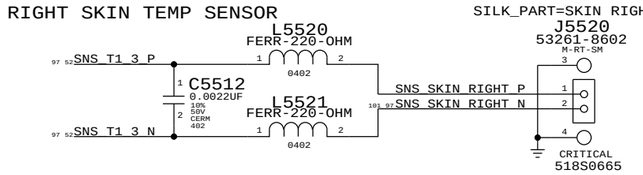
SILK_PART=ODD TEMP

CPU PROXIMITY TEMP SENSOR



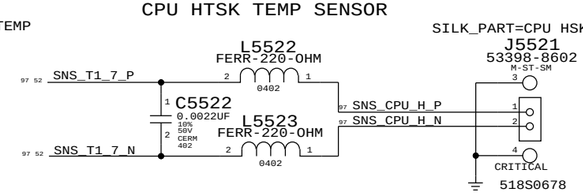
Place Q5500 (CPU Proximity Sensor) at the solder side
at edge near backer plate of CPU to replace HeatSink Temp Sensor

RIGHT SKIN TEMP SENSOR



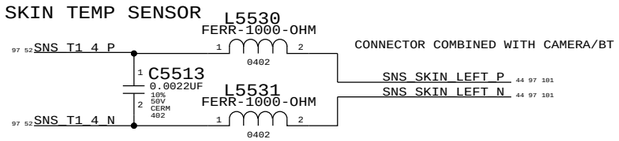
SILK_PART=SKIN RIGHT TEMP

CPU HTSK TEMP SENSOR



SILK_PART=CPU HSK

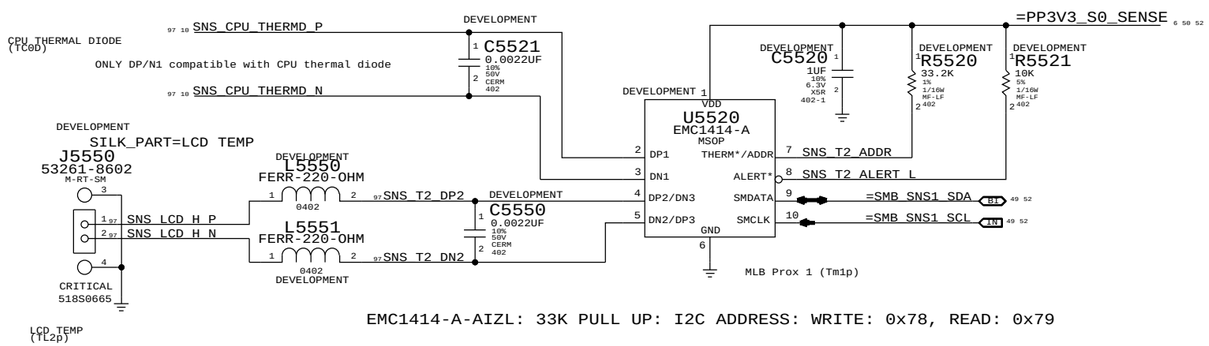
LEFT SKIN TEMP SENSOR



CONNECTOR COMBINED WITH CAMERA/BT

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SNS T2: DEVELOPMENT TEMP SENSOR IC



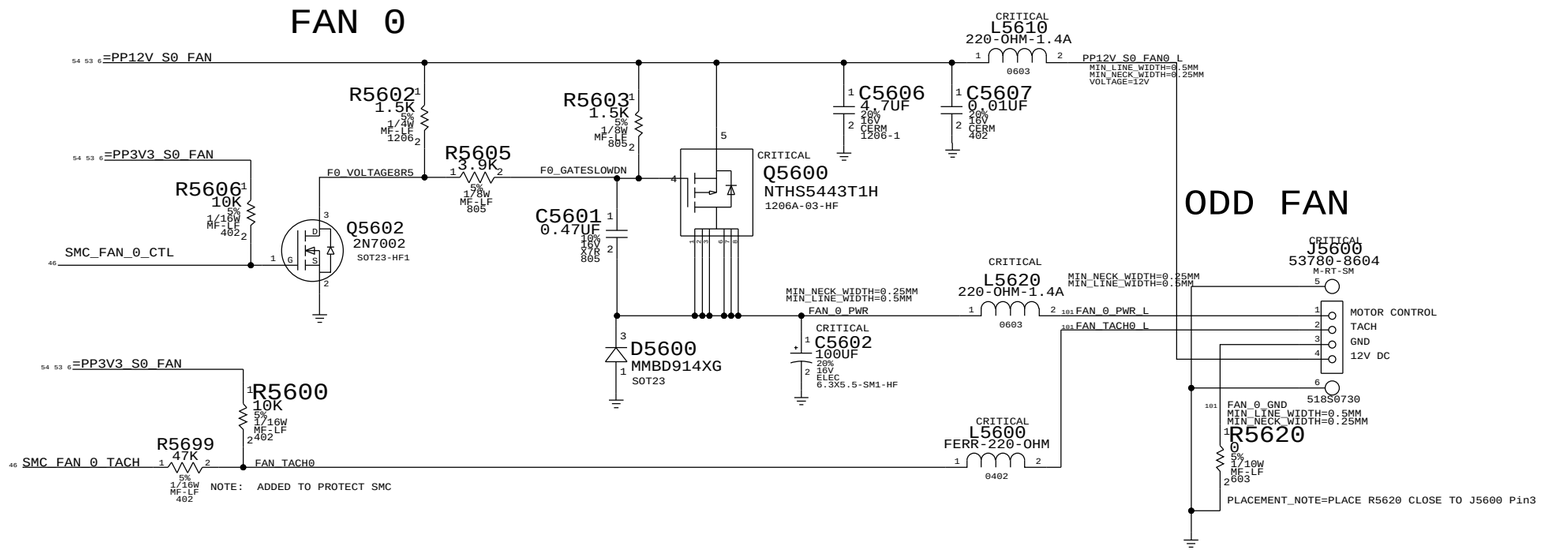
EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

PAGE TITLE: TEMP SENSORS

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
BRANCH:
PAGE: 55 OF 110
SHEET: 52 OF 101



SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

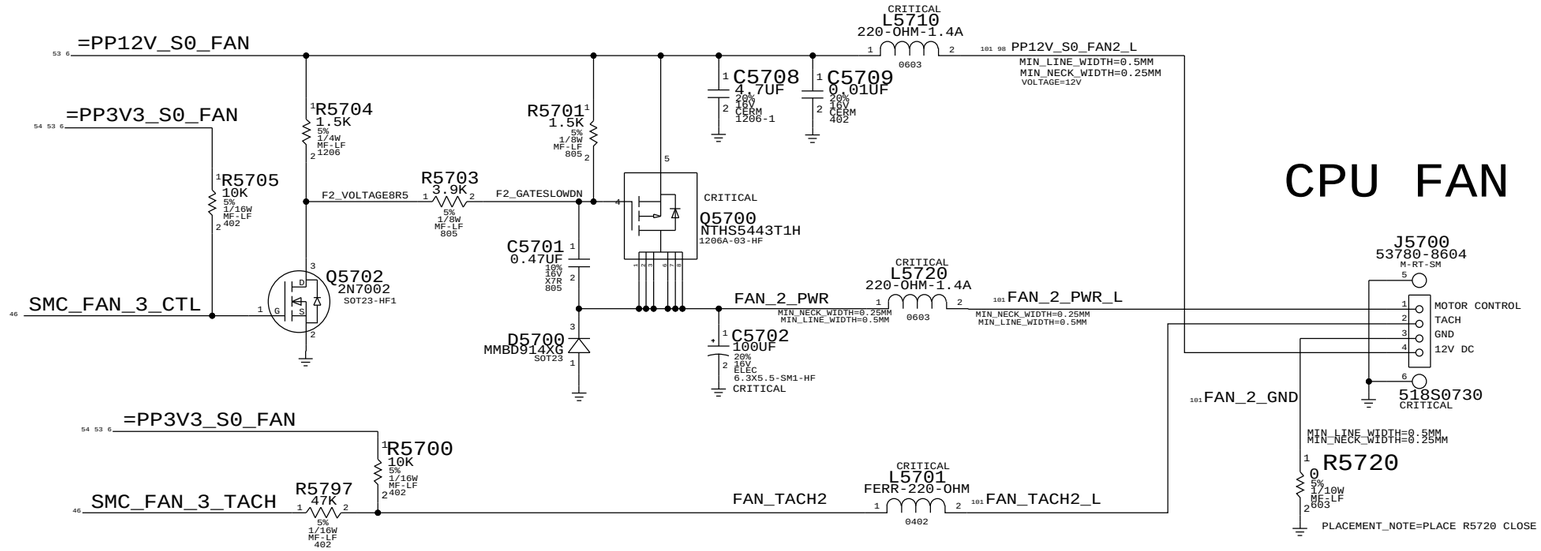
REVISION: 10.1.0

BRANCH:

PAGE: 56 OF 110

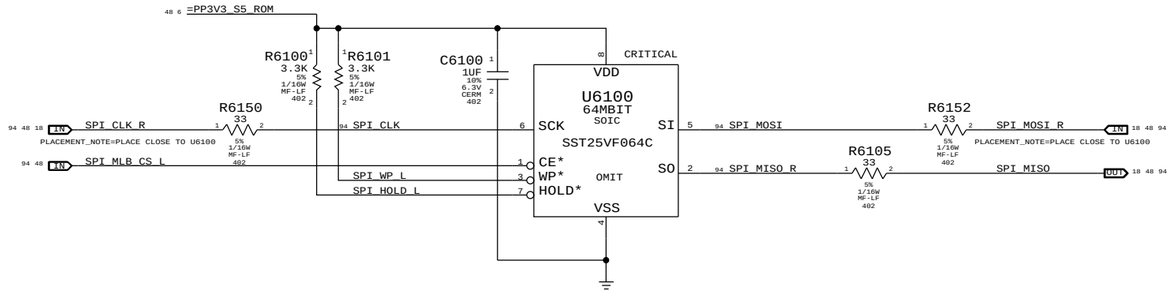
SHEET: 53 OF 101

SMC'S FAN3 OUTPUT CONTROL FAN 2



FAN 3 SMC CONTROL (UNUSED)

SYNC_MASTER=K62_JERRY	SYNC_DATE=01/09/2011
PAGE TITLE: CPU FAN	
Apple Inc.	DRAWING NUMBER: 051-8442 SIZE: D
	REVISION: 10.1.0
	BRANCH:
	PAGE: 57 OF 110
	SHEET: 54 OF 101



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D

REVISION 10.1.0

BRANCH

PAGE 61 OF 110

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6201 4.7UF 20% 4V X5R-1 402

C6200 0.47UF 10% 10V X5R 402

C6208 10UF 20% 10V POLY-TANT CASE-B2-SM

C6202 0.47UF 10% 10V X5R 402

C6203 10UF 20% 10V POLY-TANT CASE-B2-SM

C6205 1UF 10% 10V X5R 402-1

C6204 0.47UF 10% 10V X5R 402

C6206 0.47UF 10% 10V X5R 402

C6207 CRITICAL 10UF 20% 6.3V CERM-X5R 0402-1

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_HPAMP

GND_AUDIO_CODEC

GND_AUDIO_HPAMP

PP4V5_AUDIO_ANALOG

R6200 2.67K 1% 1/16W MF-LF 402

C6209 2.2UF 20% 6.3V CERM 402-LF

C6210 2.2UF 20% 6.3V CERM 402-LF

VBIAS_DAC

CS4206_FP

CS4206_FN

U6201 CS4206B QFN CRITICAL

9	VD	24	VA_REF
46	VA_HP	25	VA
29	VBIAS_DAC		
44	VHP_FILT+	38	HPOUT_L
41	VHP_FILT-	40	HPOUT_R
		39	HPREF
2	GPIO0/DMIC_SDA1	35	LINEOUT_L1+
12	GPIO1/DMIC_SDA2/SPDIF_OUT2	34	LINEOUT_L1-
14	GPIO2	36	LINEOUT_R1+
15	GPIO3	37	LINEOUT_R1-
13	SENSE_A	31	LINEOUT_L2+
		30	LINEOUT_L2-
		32	LINEOUT_R2+
		33	LINEOUT_R2-
16	MICBIAS		
28	VCOM		
21	LINEIN_L+		
22	LINEIN_C-		
23	LINEIN_R+		
18	MICIN_L+		
17	MICIN_L-		
19	MICIN_R+		
20	MICIN_R-		
27	VREF+_ADC		
4	DMIC_SCL		
45	FLYP		
43	FLYC		
42	FLYN		
3	VL_HD		
1	VL_IF		
6	BITCLK		
10	SYNC		
8	SDI		
5	SDO		
11	RESET*		
47	SPDIF_IN		
48	SPDIF_OUT		
7	DGND	49	THRM_PAD
26	AGND		

TWEETERS

AUD_HP_PORT_L

AUD_HP_PORT_R

AUD_HP_PORT_REF

R6205 0 5% 1/16W MF-LF 402

HP AMP/LINE OUT

AUD_LO1_L_P

AUD_LO1_L_N

AUD_LO1_R_P

AUD_LO1_R_N

WOOFERS

AUD_LO2_L_P

AUD_LO2_L_N

AUD_LO2_R_P

AUD_LO2_R_N

HP AMP SPEAKERS

NC TP_AUD_DMIC_SDA1

NC TP_AUD_GPIO_1

AUD_GPIO_2

AUD_GPIO_3

AUD_SENSE_A

C6211 2.2UF 20% 6.3V CERM 402-LF

C6212 2.2UF 20% 6.3V CERM 402-LF

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.15MM

AUD_CODEC_MICBIAS

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

CS4206_VCOM

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

AUD_LI_P_L

AUD_LI_COM

AUD_LI_P_R

AUD_MIC_INP_L

AUD_MIC_INN_L

AUD_MIC_INR_P

AUD_MIC_INR_N

CS4206_VREF_ADC_NC

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

TP_CS4206_DMIC_SCL NC

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0

R6201 22 5% 1/16W MF-LF 402

AUD_SDI_R

HDA_SDOUT

HDA_RST_L

AUD_SPDIF_IN_CODEC

AUD_SPDIF_CHIP

AUD_SPDIF_OUT

R6202 22 5% 1/16W MF-LF 402

R6203 100K 1% 1/16W MF-LF 402

DGND_THRM_PAD_AGND

CRITICAL C6213 1UF 10% 20V TANT CASE-P3-MF

CRITICAL C6214 10UF 20% 10V POLY-TANT CASE-B2-SM

GND_AUDIO_HPAMP

GND_AUDIO_CODEC

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S2592	353S3199		U6201	CS4206A

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

XW6212

PP5V_AUDIO_HPAMP

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.28MM VOLTAGE=4.5V

L6210 FERR-220-OHM 0402

=PP5V_S0_AUDIO

VR6201 TPS71745 SON CRITICAL

4V5_REG_IN

4V5_REG_EN

4V5_NR

PP4V5_AUDIO_ANALOG

R6220 0 5% 1/16W MF-LF 402

NOSTUFF C6221 1UF 10% 10V X5R 402-1

C6222 1UF 10% 10V X5R 402-1

C6223 0.1UF 10% 16V X7R-CERM 402

C6224 1UF 10% 10V X5R 402-1

GND_AUDIO_CODEC

NOSTUFF R6212 0 5% 1/16W MF-LF 402

R6210 0 5% 1/16W MF-LF 603

XW6211

GND_AUDIO_HPAMP

ISOLATED 5 V POWER SUPPLY FOR HP AMP

APN 152S1314

=PP5V_S0_AUDIO

C6250 10UF 20% 10V X5R 603

CRITICAL Q6250 DMMT3906W-7-F SOT-363

NOSTUFF R6258 1K 1% 1/16W MF-LF 402

CRITICAL C6256 1UF 10% 25V X5R 402

R6255 1.0K 1% 1/10W MF-LF 603

SC4503_SW

CRITICAL T6250 1.8UH-1.6A-243MOHM LPD3015-SM

AUD_XFRMR_SEC

D6252 DO222-SM STPS1L30MF

PP5V_AUDIO_ISO

CRITICAL C6258 150UF-.025-OHM 20% 6.3V TANT CASE-B2-SM

APN 128S0271

C6259 10UF 20% 10V X5R 603

R6257 4.99K 1% 1/16W MF-LF 603

GND_AUDIO_ISO

R6260 10 1% 1/16W MF-LF 603

SC4503_SW_SNBR

SC4503_FB_DDROP

C6257 0.1UF 10% 16V X7R-CERM 402

R6256 49.9K 1% 1/16W MF-LF 402

D6250 SOD-523 BAT54XV2T1

APN 353S3080

R6250 40.2K 1% 1/16W MF-LF 402

U6250 SC4503 TSOT-23 SYM_VER_2 CRITICAL

SC4503_SHDN

SC4503_FB

C6252 0.1UF 10% 16V X7R-CERM 402

C6251 0.1UF 10% 16V X7R-CERM 402

NOSTUFF C6253 1UF 10% 10V X5R 402-1

R6251 3.40K 1% 1/16W MF-LF 402

R6252 12.4K 1% 1/16W MF-LF 402

DMMT3906W-7-F SOT-363

SC4503_FB_RDIV

SC4503_FB_PNP

SC4503_FB_FILT

R6253 43.2K 1% 1/16W MF-LF 402

R6254 20 1% 1/16W MF-LF 603

D6251 SOD-523 BAT54XV2T1

SC4503_SW_D

C6254 0.01UF 10% 16V CERM 402

NOSTUFF C6261 0.001UF 10% 50V X7R 402

NOSTUFF R6259 100K 1% 1/16W MF-LF 402

C6255 0.001UF 10% 50V X7R 402

SYNC_MASTER=K62_DAVID	SYNC_DATE=01/09/2011
PAGE TITLE	AUDIO: CODEC/REGULATOR
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
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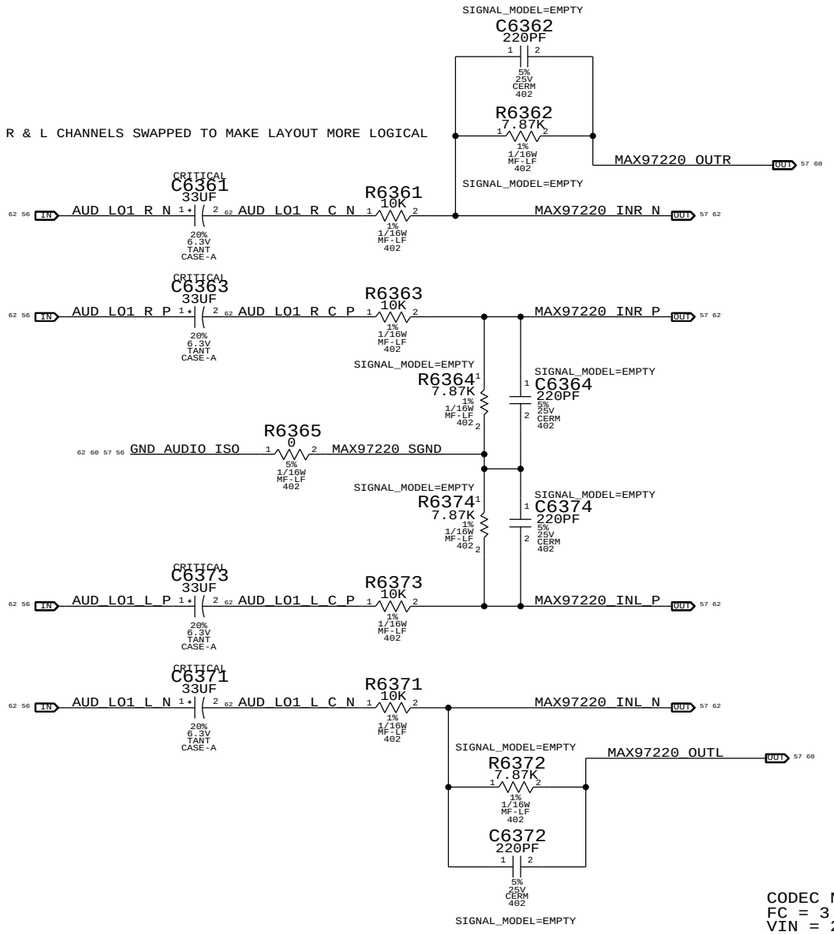
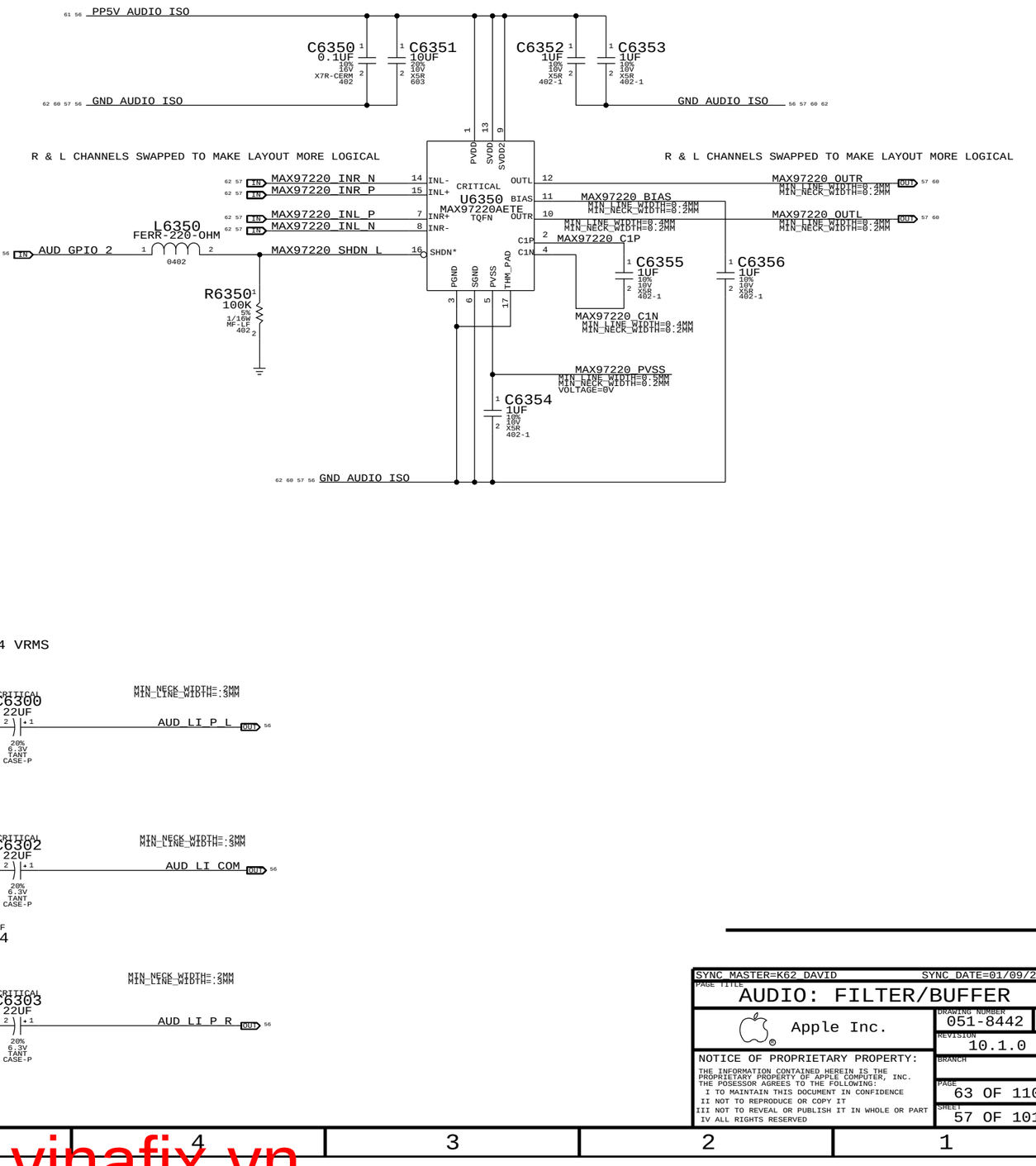
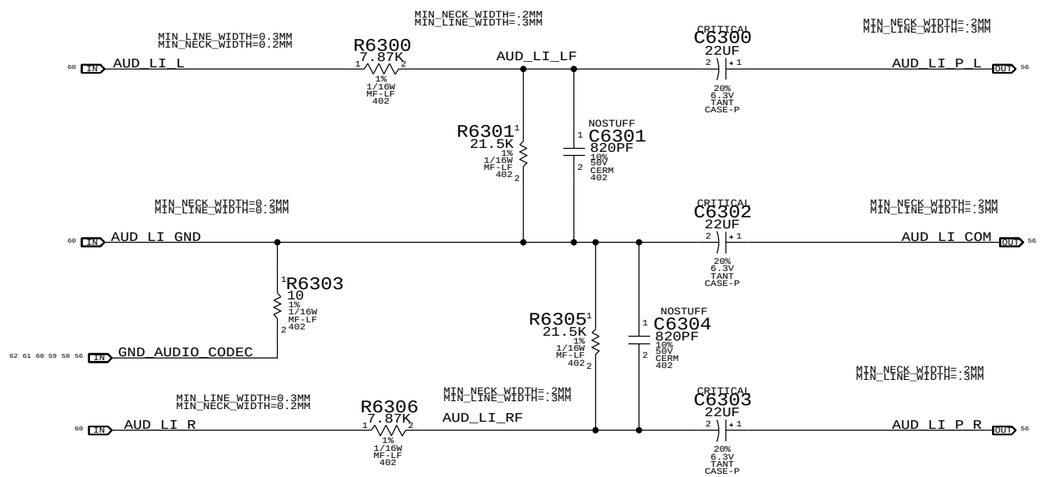




CODEC Nom SE RIN = 20K OHMS
FC = 3.62 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

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RIGHT CH SPEAKER AMP
APPLE P/N 353S3069

R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 210K NOMINAL W/ +9 DB GAIN
FC_HPF, TWEETERS = ~924 HZ (820 PF)
FC_HPF, WOOFERS = ~23 HZ (0.033 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

SE-TO-DIFF CONVERTER

SYNC_MASTER=K62_DAVID	SYNC_DATE=01/09/2011
PAGE TITLE: AUDIO: SPEAKER AMP_1	
Apple Inc.	DRAWING NUMBER 051-8442 · SIZE D
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LEFT CH SPEAKER AMP
APPLE P/N 353S3069

=PP12V_S0_AUDIO_SPKRAMP

C6500 10UF 10% 25V X5R 805
C6501 0.1UF 10% 25V X5R 402

=PP3V3_S0_AUDIO

NOSTUFF R6504 0 5% 1/16W MF-LF 402
NOSTUFF R6506 0 5% 1/16W MF-LF 402
AUD_LAMP_GAIN0
AUD_LAMP_GAIN1
R6505 0 5% 1/16W MF-LF 402
R6507 0 5% 1/16W MF-LF 402

C6502 0.1UF 10% 25V X5R 402
C6503 1UF 10% 25V X5R 603-1
C6504 0.1UF 10% 25V X5R 402
C6505 1UF 10% 25V X5R 603-1
CRITICAL C6506 220UF 20% 16V ELEC SM-CASE-C1-HF

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 210K NOMINAL W/ +9 DB GAIN
FC_HPF, TWEETERS = ~924 HZ (820 PF)
FC_HPF, WOOFERS = ~23 HZ (0.033 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

AUD_HP_L_N → L6500 FERR-1000-OHM 0402 → AUD_LAMP_RINC_P → C6508 820PF 10% 50V CERM 402 → AUD_LAMP_RIN_P
AUD_HP_L_P → L6501 FERR-1000-OHM 0402 → AUD_LAMP_RINC_N → C6509 820PF 10% 50V CERM 402 → AUD_LAMP_RIN_N
AUD_LO2_L_N → L6502 FERR-1000-OHM 0402 → AUD_LAMP_LINC_N → C6510 0.033UF 10% 16V X5R 402 → AUD_LAMP_LIN_N
AUD_LO2_L_P → L6503 FERR-1000-OHM 0402 → AUD_LAMP_LINC_P → C6511 0.033UF 10% 16V X5R 402 → AUD_LAMP_LIN_P

PP5V_LAMP_VREG
MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM
R6508 10 1% 1/16W MF-LF 402 → AUD_LAMP_REG_OUT
AUD_LAMP_PLIMIT
AUD_LAMP_FSEL
AUD_SPKRAMP_MUTE_L
R6509 0 5% 1/16W MF-LF 402

U6500 TPA3117D2 QFN CRITICAL

4	AVCC	BSPL	25
26	PVCCL	OUTPL	24
27	PVCCL	OUTNL	22
14	PVCCR	BSNL	21
15	PVCCR	BSPR	16
9	RINP	OUTPR	17
8	RINN	OUTNR	19
1	LINN	BSNR	20
32	LINP	NC	12
2	GAIN0	NC	13
3	GAIN1	NC	28
6	REG_OUT	NC	29
7	PLIMIT	NC	10
11	PBTL		
31	FSEL		
30	SD*		
5	AGND		
18	PGND		
23	PGND		
33	THRM PAD		

AUD_LAMP_PBTL

R6502 0 5% 1/10W MF-LF 402
C6517 2.2UF 20% 10V X5R-CERM 402
NOSTUFF R6510 10K 1% 1/10W MF-LF 402
C6518 1UF 10% 10V X5R 402
R6503 0 5% 1/16W MF-LF 402

AUD_LAMP_BSPL → C6513 0.22UF 20% 25V X5R 603 → AUD_LAMP_OUTPL → L6504 SIGNAL_MODEL=EMPTY CRITICAL 220-OHM-25%-2.5A 0603 → AUD_SPKR_LWFR_OUT_P
AUD_LAMP_BSNL → C6514 0.22UF 20% 25V X5R 603 → AUD_LAMP_OUTNL → L6505 SIGNAL_MODEL=EMPTY CRITICAL 220-OHM-25%-2.5A 0603 → AUD_SPKR_LWFR_OUT_N
AUD_LAMP_BSPR → C6515 0.22UF 20% 25V X5R 603 → AUD_LAMP_OUTPR → L6506 SIGNAL_MODEL=EMPTY CRITICAL 220-OHM-25%-2.5A 0603 → AUD_SPKR_LTWT_OUT_N
AUD_LAMP_BSNR → C6516 0.22UF 20% 25V X5R 603 → AUD_LAMP_OUTNR → L6507 SIGNAL_MODEL=EMPTY CRITICAL 220-OHM-25%-2.5A 0603 → AUD_SPKR_LTWT_OUT_P

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

SIGNAL_MODEL=EMPTY
CRITICAL C6520 1000PF 5% 25V NP0-C0G 402
CRITICAL C6522 1000PF 5% 25V NP0-C0G 402
CRITICAL C6519 1000PF 5% 25V NP0-C0G 402
CRITICAL C6521 1000PF 5% 25V NP0-C0G 402
SIGNAL_MODEL=EMPTY

SE-TO-DIFF CONVERTER

AUD_HP_PORT_L → CRITICAL C6553 3.3UF 10% 16V TANT SMA-HF1 → AUD_L_SE_DIFF_IN
R6553 21K 1% 1/16W MF-LF 402
AUD_L_SE_DIFF_IN_R
SIGNAL_MODEL=EMPTY R6554 21K 1% 1/16W MF-LF 402

AUD_SE_DIFF_SHDN_L

U6550 MAX4253 UCSP CRITICAL

B4	V-	C4	
C3	+	C1	OUT
C2	-	B1	V+
B1	V+	A2	-
A1	OUT	A3	+
A4	V-	B4	

AUD_HP_L_P
AUD_HP_L_N

SIGNAL_MODEL=EMPTY R6555 2.21K 1% 1/16W MF-LF 402
SIGNAL_MODEL=EMPTY R6557 2.21K 1% 1/16W MF-LF 402
AUD_L_SE_DIFF_P_INV
SIGNAL_MODEL=EMPTY R6558 2.21K 1% 1/16W MF-LF 402
SIGNAL_MODEL=EMPTY R6556 2.21K 1% 1/16W MF-LF 402
AUD_L_SE_DIFF_N_INV

PP4V5_AUDIO_ANALOG
C6550 4.7UF 20% 6.3V X5R 402
C6551 0.47UF 10% 10V X5R 402
AUD_SE_DIFF_VBIAS
GND_AUDIO_CODEC

SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011
PAGE TITLE: AUDIO: SPEAKER AMP
Apple Inc.
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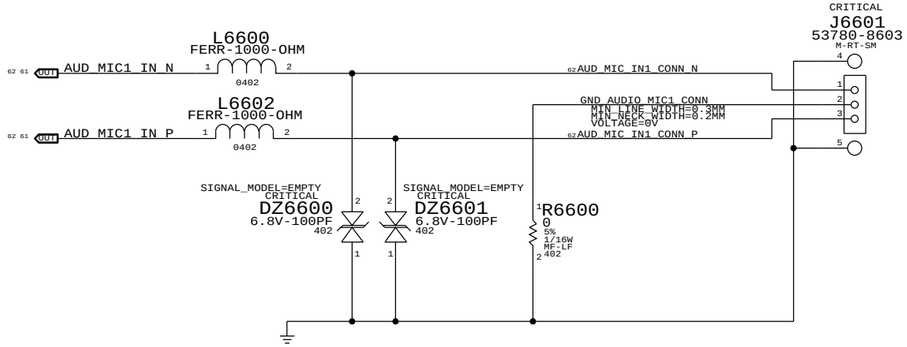
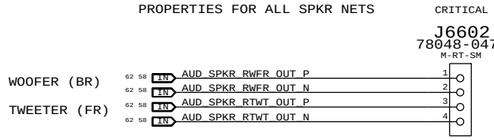
INTERNAL MIC CON
APPLE P/N 518S0677

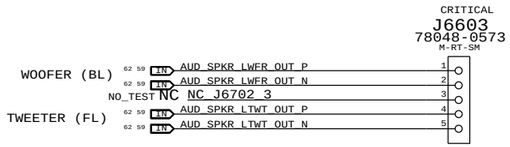


SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

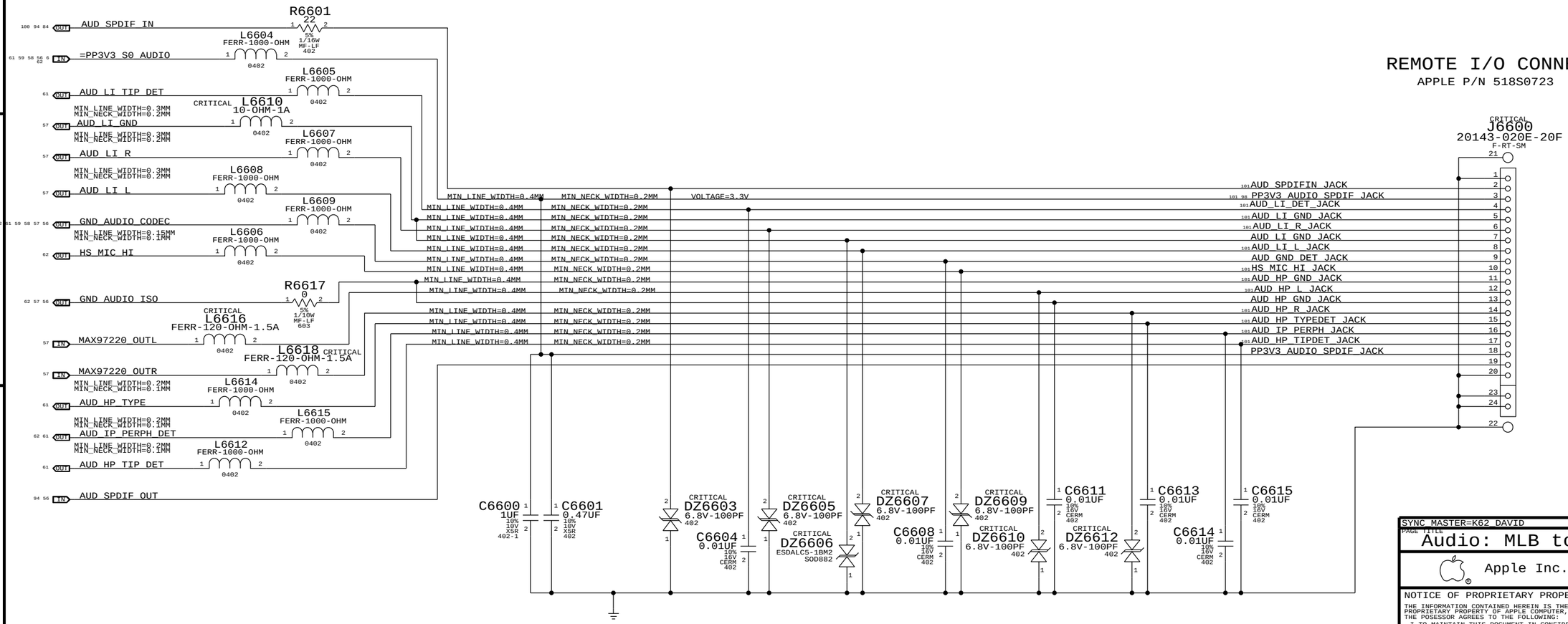
PROPERTIES FOR ALL SPKR NETS



PROPERTIES FOR ALL SPKR NETS



REMOTE I/O CONNECTOR
APPLE P/N 518S0723



SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

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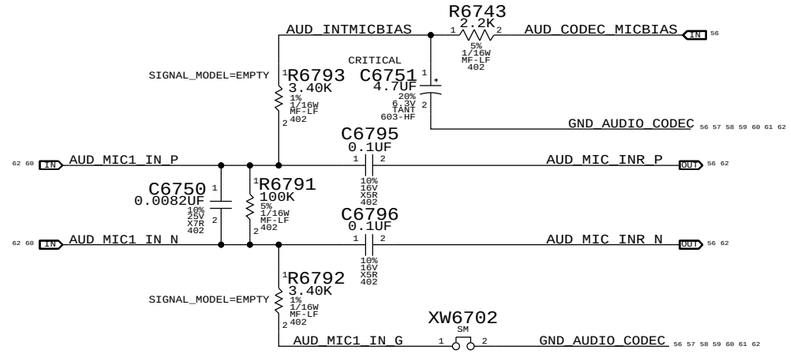
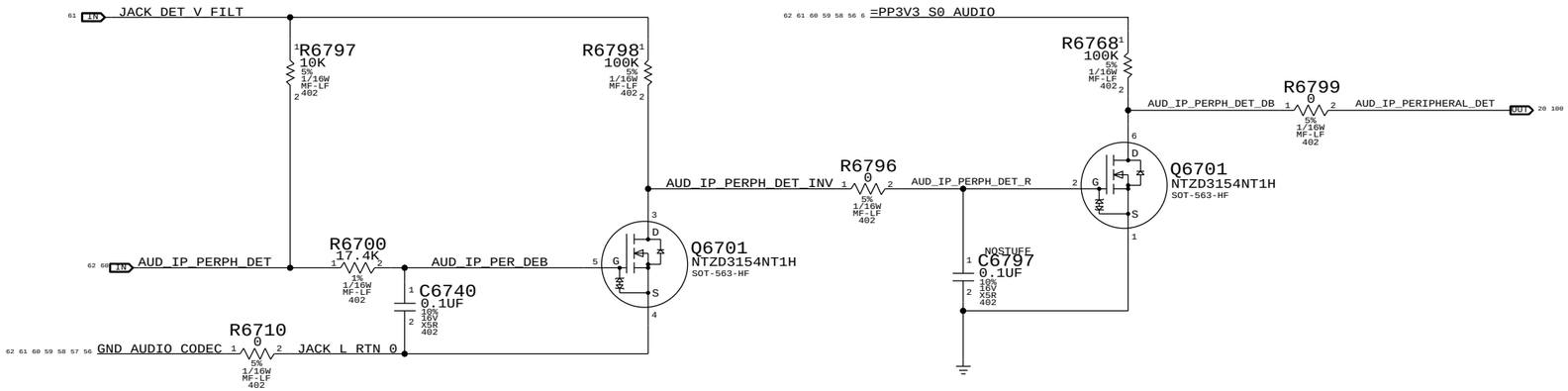
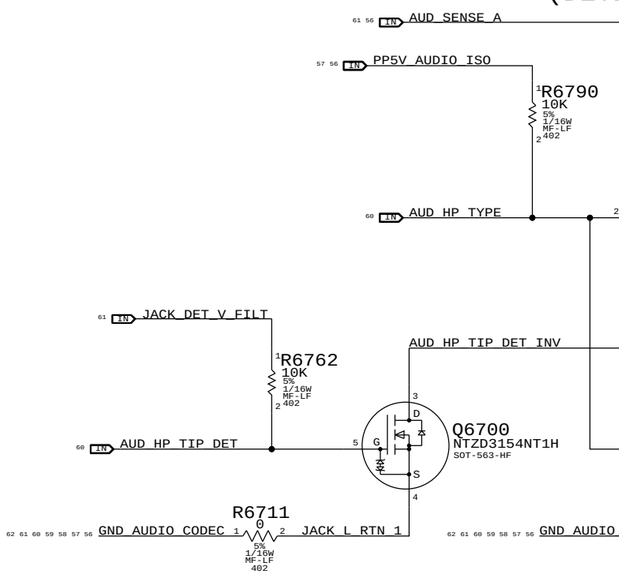
Internal Microphone Impedance Matching



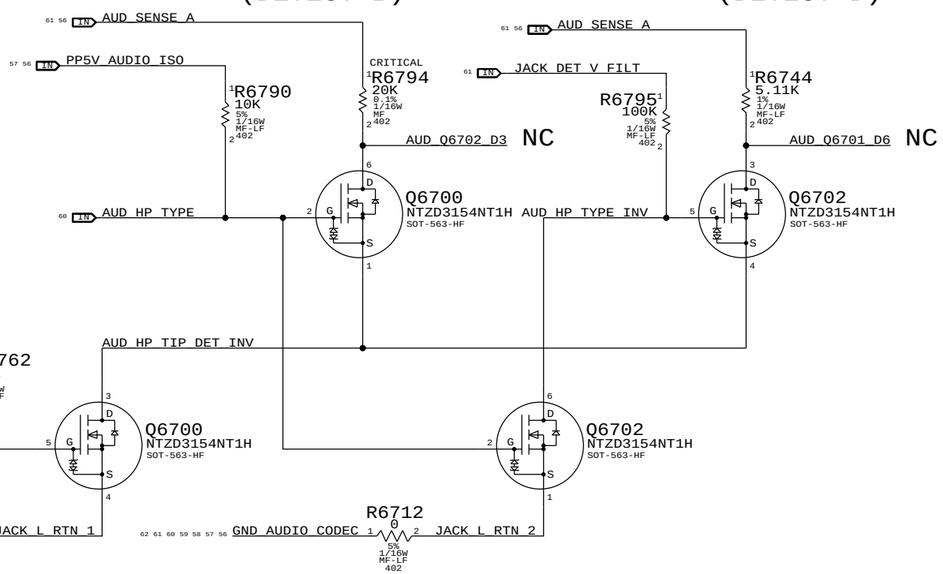
IPHS HS Detect Debounce CKT



Digital Out (DETECT B)

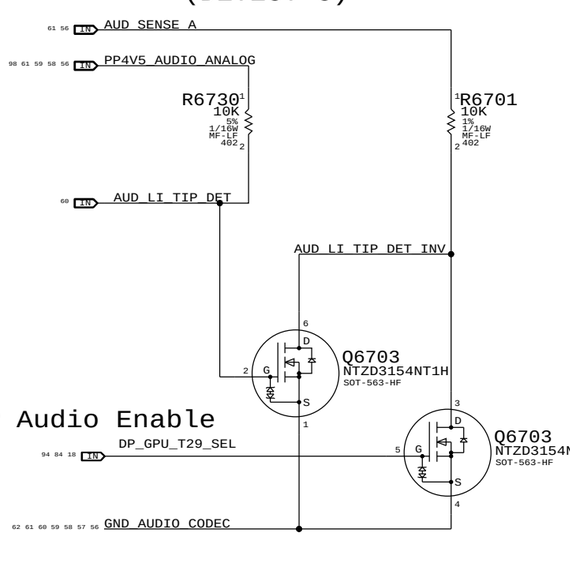


Headphone Out (DETECT D)



Headphone Out (DETECT D)

LI Insert Detect (DETECT C)



SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011

PAGE TITLE: AUDIO: Detects/Grounding

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0x0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (PCVR_INT) COUGAR POINT GPIO 3 (PERIPH_DET)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

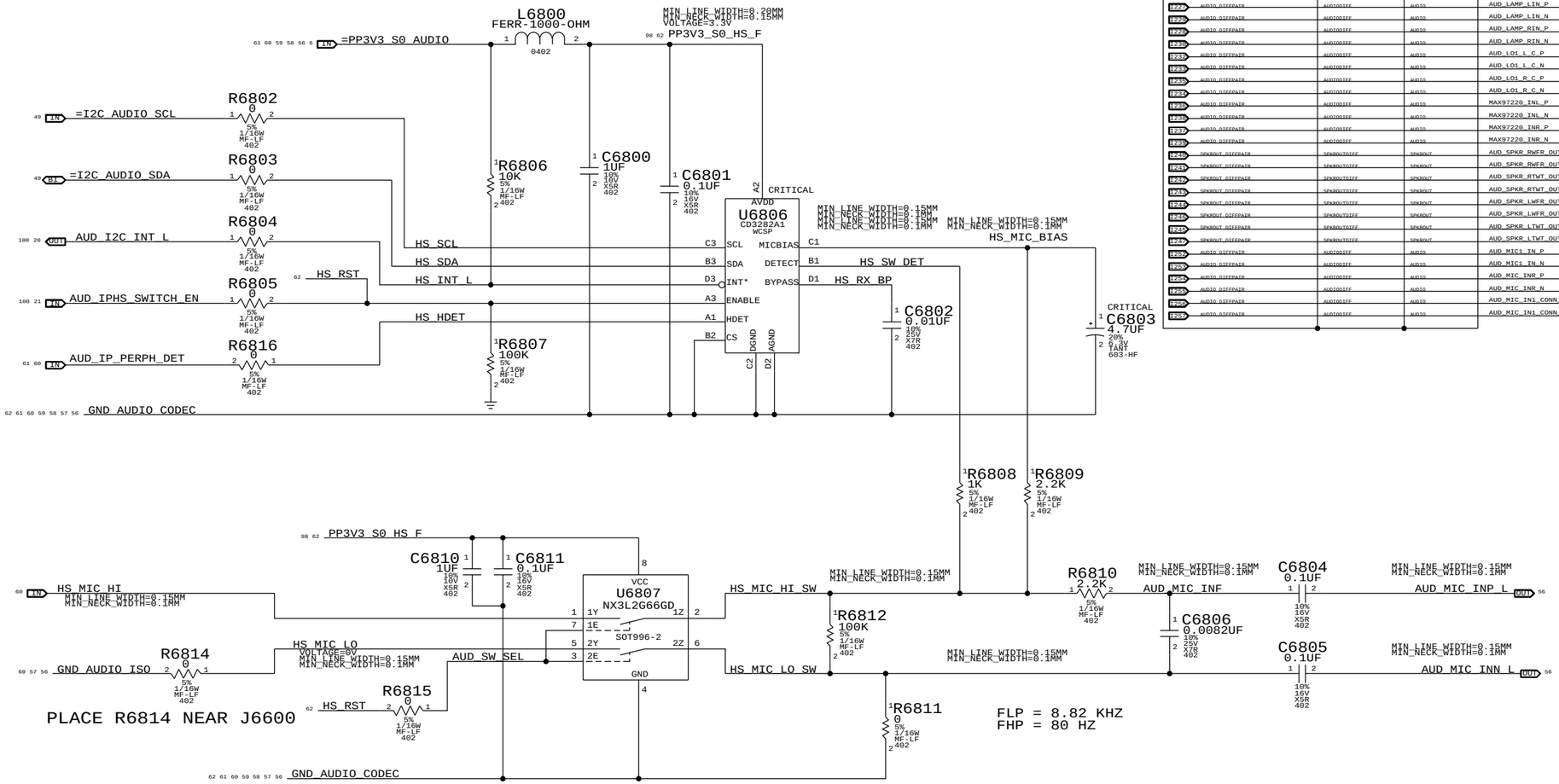
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	58 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	59 60
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	59 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_P	60 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_N	60 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	56 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_N	56 61
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_P	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_N	60

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640



SYNC_MASTER=K62_DAVID SYNC_DATE=01/09/2011

PAGE TITLE: AUDIO: Mikey

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SLP_S4 ENABLES

MEMVTT_EN SEQUENCE

=PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
NOSTUFF C6951 100PF 5% 50V CERM 402
PM_EN_DDRVTT_S0_REG 32 63 72 100
NOSTUFF C6953 0.1UF 10% 10V X5R 402
VTT_REG_PGOOD_L
Q6911 MMDT3904-X-G SOT-363-LF
R6950 10K 5% 1/16W MF-LF 402
64 63 PM_PGOOD_P1V05_S0_REG 100 68
CPUVTT_REG_PGOOD_R 100
Q6911 SOT-363-LF
MMDT3904-X-G
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
R6971 0 5% 1/16W MF-LF 402
100 47 46 19 5 PM_SLP_S5_L
NOSTUFF R6972 0 5% 1/16W MF-LF 402
100 63 47 46 32 19 5 PM_SLP_S4_L
100 PM_SLP_S4_1_L_R
U6900 08 74LVC08 TSSOP-HF
C6910 0.1UF 20% 10V CERM 402
100 S4_ENABLES
R6911 33 5% 1/16W MF-LF 402
R6912 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S3_FET 74 100
Enable FET
PM_EN_P5V_S3_REG 71 100
ENABLE REGULATOR
NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC 94
Q6910 2N7002 SOT23-HF1
100 11 CPU_SKTOCC_L
NOSTUFF R6917 10K 5% 1/16W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

100 83 71 63 PM_PGOOD_P5V_S3_REG
R6970 0 5% 1/16W MF-LF 402
PM_EN_USB_PWR 43 94
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402

64 63 11 6 =PP3V3_S5_PWRCTL
100 63 47 46 32 19 5 PM_SLP_S4_L
U6900 08 74LVC08 TSSOP-HF
PM_EN_DDR1V5_S3_REG 72 100
100 83 71 63 PM_PGOOD_P5V_S3_REG

NOSTUFF R6931 33 5% 1/16W MF-LF 402
100 74 64 63 PM_PGOOD_P3V3_S0_FET
PM_EN_P1V5_S0_FET 63 74 100

SLP_S3 ENABLES

64 63 11 6 =PP3V3_S5_PWRCTL
R6955 10K 5% 1/16W MF-LF 402
P3V3_S5_PWRCTL_U6900_R
100 64 PGOOD_P12V_S0
U6900 08 74LVC08 TSSOP-HF

OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)

NOSTUFF R6946 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET
Enable FET
OUT 63 74 100
NOSTUFF R6947 33 5% 1/16W MF-LF 402
PM_EN_P5V_S0_FET
Enable FET
OUT 74 100

NOSTUFF R6944 33 5% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
PM_SLP_S3_BUF_L 100
Enable FET
PM_EN_P1V5_S0_FET 63 74 100
PM_EN_DDRVTT_S0_REG 32 63 72 100
Enable regulator

NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

64 63 11 6 =PP3V3_S5_PWRCTL
100 63 47 46 36 32 26 19 5 PM_SLP_S3_L
100 72 5 PM_PGOOD_DDR1V5_S3_REG
U6900 08 74LVC08 TSSOP-HF
PM_EN_P12V_S0_FET 6 100

OPTION TO DELAY 1V8
R6932 33 5% 1/16W MF-LF 402
100 74 64 63 PM_PGOOD_P3V3_S0_FET
NOSTUFF R6990 33 5% 1/16W MF-LF 402
100 74 64 63 PM_PGOOD_P5V_S0_FET
PM_EN_P1V8_S0_REG 72 100
NOSTUFF C6994 0.47UF 10% 6.3V CERM-X5R 402

OPTIONAL SEQUENCE TO DELAY 3V,1V5
100 74 64 63 PM_PGOOD_P5V_S0_FET
R6930 33 5% 1/16W MF-LF 402
PM_EN_P3V3_S0_FET 63 74 100
100 74 64 63 PM_PGOOD_P5V_S0_FET
R6933 33 5% 1/16W MF-LF 402
PM_EN_P1V5_S0_FET 63 74 100

=PP12V_S0_PWRCTL 6 64 81
R6934 82K 5% 1/16W MF-LF 402
PM_PGOOD_P5V_S0_FET 63 64 74 100
R6935 33K 5% 1/16W MF-LF 402

NOSTUFF R6942 33 5% 1/16W MF-LF 402
Enable regulator
PM_EN_P1V05_S0_REG
NOSTUFF C6942 1UF 10% 6.3V CERM 402
100 74 64 63 PM_PGOOD_P3V3_S0_FET
R6936 33 5% 1/16W MF-LF 402
OPTION TO DELAY 1V05

CPUVTT_VREG/ PCH CORE
68 100
100 68 64 63
NOTE: PM_PGOOD_P1V05_S0_REG ENABLES VCCSA REGULATOR CIRCUIT ON PAGE 70
PM_PGOOD_P1V05_S0_REG = =PM_EN_VCCSA_S0_CPU
MAKE_BASE=TRUE

VCCSA REGULATOR
100 64
PM_PGOOD_PVCCSA_S0_REG = Enable regulator PM_EN_PVCORE_CPU 65 100
MAKE_BASE=TRUE
TO ENABLE OF CPU VCORE

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011
PAGE TITLE
POWER SEQUENCING ENABLES

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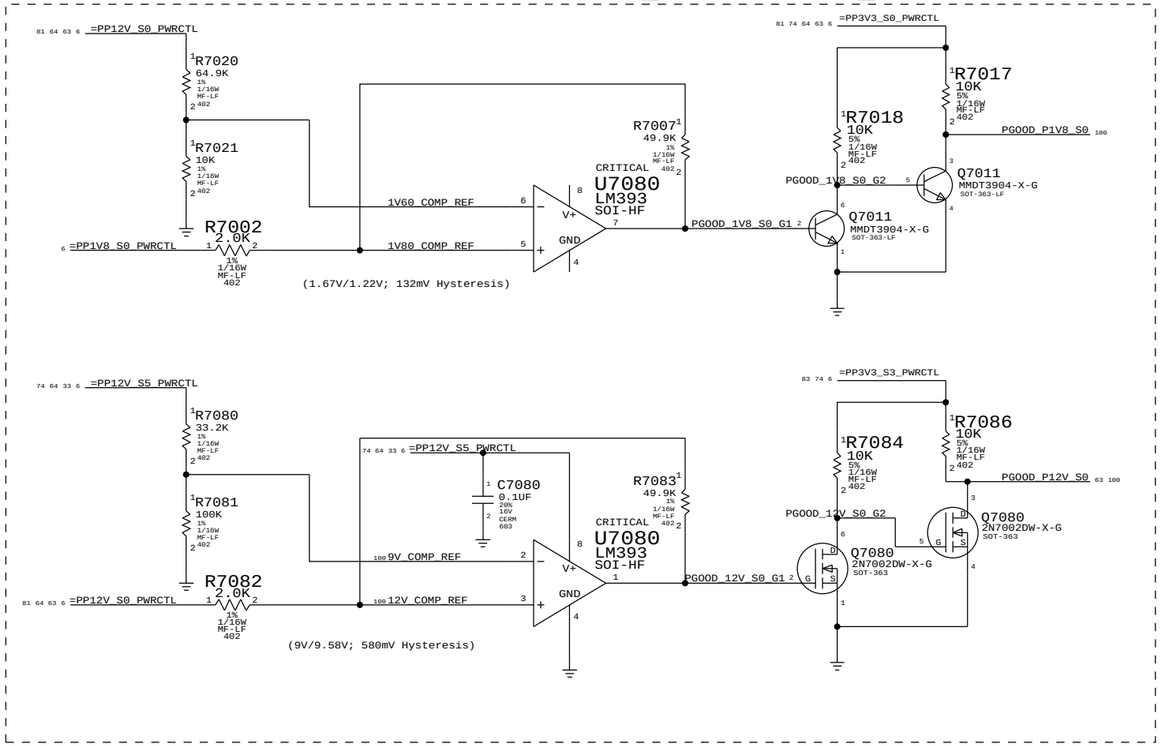
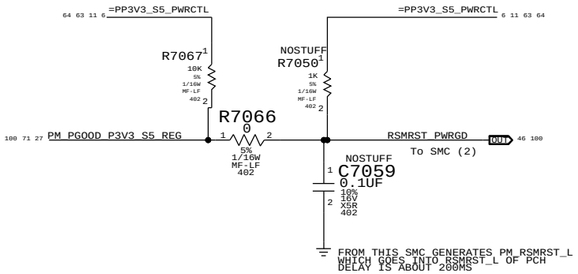
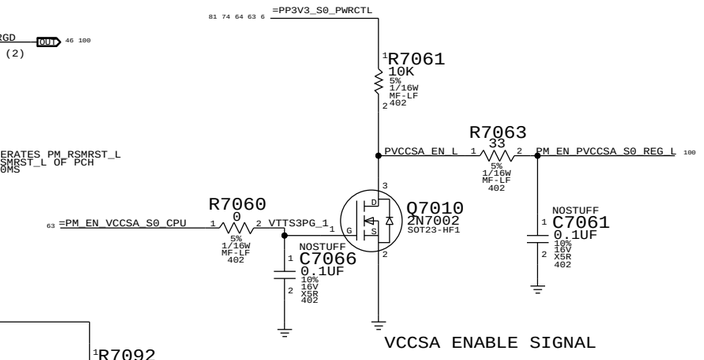
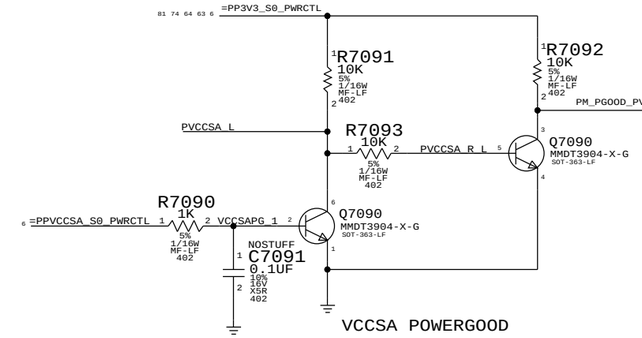
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

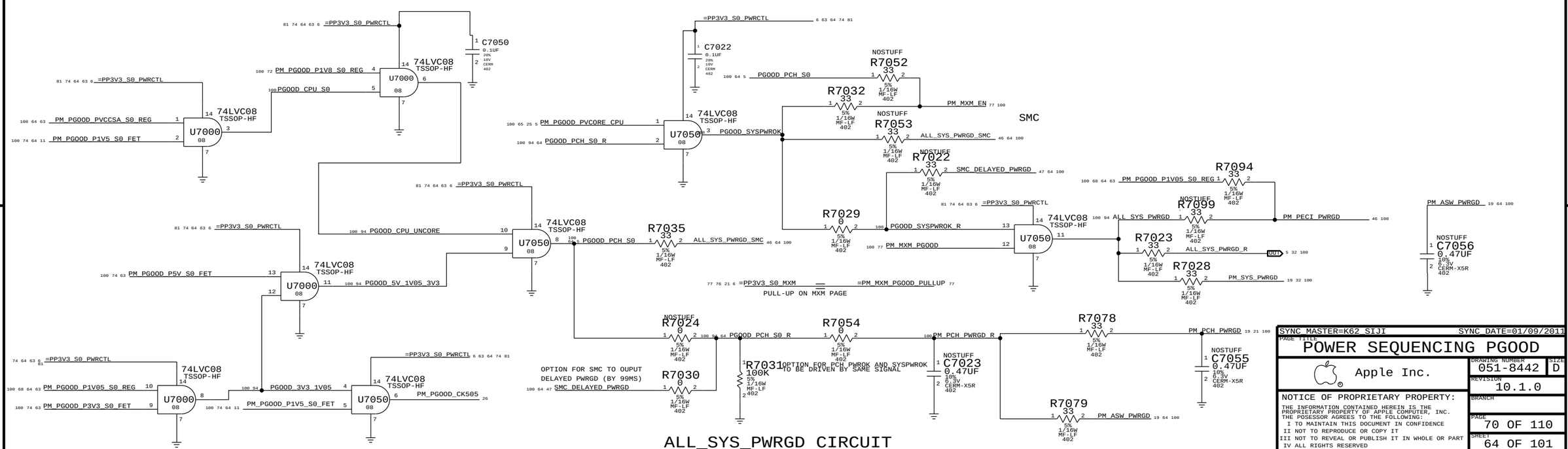


S0 RAILS PGOOD









ALL_SYS_PWRGD CIRCUIT

SYNC_MASTER=K62_SIJI SYNC_DATE=01/09/2011

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CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG

=PPVAXG_S0_CPU
CPU_VAXG_SENSE_P
CPU_VAXG_SENSE_N
R7160 1K
R7161 0
R7162 10
R7163 0
R7164 10
R7165 1K
XW7130 OMIT
XW7120 OMIT
VR_AXG_VSNS_XW_P
VR_AXG_VSNS_R_P
VR_AXG_VSNS_R_N
VR_AXG_VSNS_XW_N
VR_AXG_VSEN
VR_AXG_RGND
SIGNAL_MODEL=EMPTY
1.25 mOhm loadline
NOSTUFF C7155 0.0022UF
C7156 0.0022UF
C7157 0.0022UF
AGND_CPU

=PP5V_S0_VRD
R7127 2.2
PP5V_S0_CPU_VCORE_VCC
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=5V

=PP3V3_S0_VRD
R7157 1K
C7114 10UF
R7189 1K
R77103 6.8K
C7113 0.1UF
AGND_CPU

C7116 0.0022UF
R7128 249
R7129 0
R7130 806
R7131 10
VR_SEN_R2
VR_SEN_R3
VR_SEN_R1

R7132 9.09K
C7117 3900PF
VR_AXG_COMP_RC
C7118 39PF

C7119 4700PF
R7133 301
VR_CPU_PSICOMP2
VR_CPU_PSICOMP1

R7134 249
C7120 390PF
VR_CPU_FB_RC
R7135 1.33K
R7121 10
R7136 1.02K
VR_CPU_FB_R

C7122 82PF
R7145 4.99K
C7123 820PF
VR_CPU_FB2

C7124 0.01UF
R7152 0
AGND_CPU

R7159 1K
RT7104 6.8K
C7132 0.1UF
PP5V_S0_CPU_VCORE_VCC

=PPVCCIO_S0_CPU
R7146 110
NOSTUFF R7147 90.9
R7148 54.9
C7126 0.1UF
AGND_CPU

R7141 OMIT 1.21K
VR_AXG_HFREQ_COMP
VR_AXG_FB
VR_AXG_COMP
PM_PGOOD_PVCORE_CPU

PP5V_S0_CPU_VCORE_VCC
R7140 953K
R7156 953K
R7142 OMIT 16.5K
R7143 15.0K
VR_CPU_VIDSCLK
CPU_VIDALERT_L
CPU_VIDSOUT
VR_CPU_FB
VR_CPU_PSICOMP
R7144 OMIT 2.55K
VR_CPU_HFREQ_COMP
VR_CPU_COMP
VR_CPU_IALUTO
VR_CPU_IMON
CPU_PROCHOT_L
R7199 0
VR_HOT_L
VR_CPU_TM

R7149 30.1K
R7150 OMIT 26.1K
R7151 255K
R7158 255K

R7153 845
C7127 27.0NF
R7154 OMIT 9.76K
VR_CPU_IMON_R
AGND_CPU

=PP12V_S0_VRD
152-0118 CRITICAL L7100
0.24UH+/-20%-0.000420HM-40A
SDP1108M-TH
PP12V_S0_CPU_FLTRD
NET_PHYSICAL_TYPE=POWER
VOLTAGE=12V

CPU CORE INPUT FILTER

U7100 ISL6364 QFN

23	TMS	
20	VSENS	
16	HFCOMPS/DVCS	
19	FBS	
21	RGNDS	
18	COMPS	
13	VR_RDY	
30	BTS_DES_TCOMPS	
29	BT_FDVID_TCOMP	
28	NPSI_DE_IMAX	
27	ADDR_IMAXS_TMAX	
12	SVCLK	
11	SVALERT*	
10	SVDATA	
4	VSEN	
3	RGND	
7	FB	
6	PSICOMP	
5	HFCOMP	
8	COMP	
32	SICI	
9	IMON	
15	VR_HOT*	
31	TM	
26	PWMS	
24	ISENS+	VR_AXG_ISNS_R_P
25	ISENS-	VR_AXG_ISNS_R_N
38	PWM1	VR_CPU_PWM1_R
46	ISEN1+	
45	ISEN1-	VR_CPU_ISNS1_R_N
36	PWM2	VR_CPU_PWM2_R
42	ISEN2+	
41	ISEN2-	VR_CPU_ISNS2_R_N
39	PWM3	VR_CPU_PWM3_R
48	ISEN3+	
47	ISEN3-	VR_CPU_ISNS3_R_N
37	PWM4	VR_CPU_PWM4_R
44	ISEN4+	
43	ISEN4-	VR_CPU_ISNS4_R_N
22	FSS_DRPS	VR_AXG_SW_FREQ
17	VR_RDYS	PM_PGOOD_PVAXG
14	IMONS	VR_AXG_IMON
34	FS_DRP	VR_CPU_SW_FREQ
2	RAMP_ADJ	VR_CPU_RAMP_ADJ
40	EN_VTT	PM_EN_PVCORE_CPU
1	EN_PWR	VR_EN_PWR_OVP
33	RSET	
49	THRM PAD	

R7195 10K
R7106 0
R7107 0
NOSTUFF R7101 0
NOSTUFF R7102 0
NOSTUFF R7104 0
NOSTUFF R7103 0
NOSTUFF R7105 0
NOSTUFF R7100 0
CPUVCORE-3PH
VR_AXG_PWM
LOCAL 5V
VR_AXG_PWM_R

R7108 110
C7100 220PF
C7101 0.1UF
C7102 220PF
R7109 1.02K
DIFFERENTIAL_PAIR=VR_AXG_ISNS
VR_AXG_ISNS_P
VR_AXG_ISNS_N

R7110 0
C7103 220PF
C7104 0.1UF
R7111 1.02K
VR_CPU_PWM1
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N

R7112 0
C7105 220PF
C7106 0.1UF
R7113 1.02K
VR_CPU_PWM2
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N

R7114 0
C7107 220PF
C7108 0.1UF
R7115 1.02K
VR_CPU_PWM3
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N

R7184 0
C7187 220PF
C7188 0.1UF
R7185 1.02K
VR_CPU_PWM4
VR_CPU_ISNS4_P
VR_CPU_ISNS4_N

R7181 10K
PP12V_S0_CPU_FLTRD
R7180 100K
PP5V_S0_CPU_VCORE_VCC
R7122 100K
R7123 2.74K
R7124 6.65K
R7120 124K
R7155 105K
R7118 1.18M
R7119 12.4K
VR_RSET
VR_EN_PWR_OVP_R
R7125 1K
C7111 0.1UF
R7126 13.7K
VR_AXG_IMON_R

=PPVCORE_S0_CPU
CPU_VCC_SENSE_P
CPU_VCC_SENSE_N
R7166 1K
R7167 10
R7168 0
R7169 0
R7170 10
R7171 1K
XW7123 OMIT
XW7133 OMIT
VR_CPU_VSNS_XW_P
VR_CPU_VSNS_R_P
VR_CPU_VSNS_R_N
VR_CPU_VSNS_XW_N
VR_CPU_VSEN
VR_CPU_RGND
SIGNAL_MODEL=EMPTY
1.25 mOhm loadline
NOSTUFF C7158 0.0022UF
C7159 0.0022UF
C7160 0.0022UF
AGND_CPU

CPU VCORE
VOUT = VCORE
PEAK = 75A
AVG = 55A

SYNC_MASTER=K62_AARON SYNC_DATE=N/A
PAGE TITLE
VREG: PPVCORE_S0_CPU
Apple Inc.
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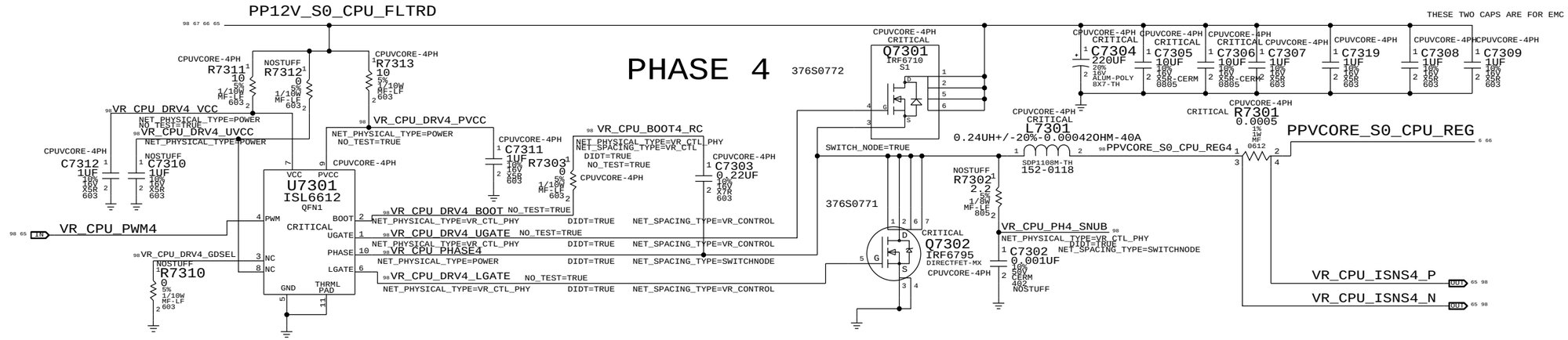

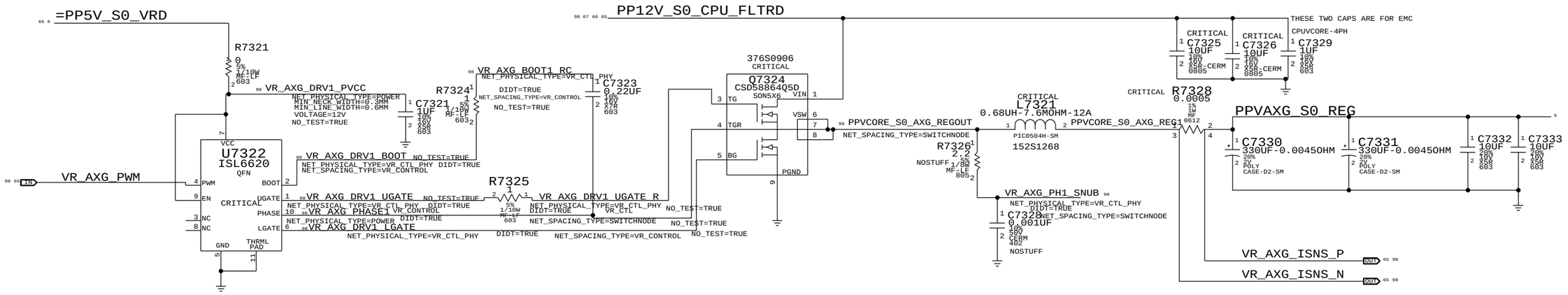

SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE
VREG:AXG PHASE/CORE - CAPS

Apple Inc.

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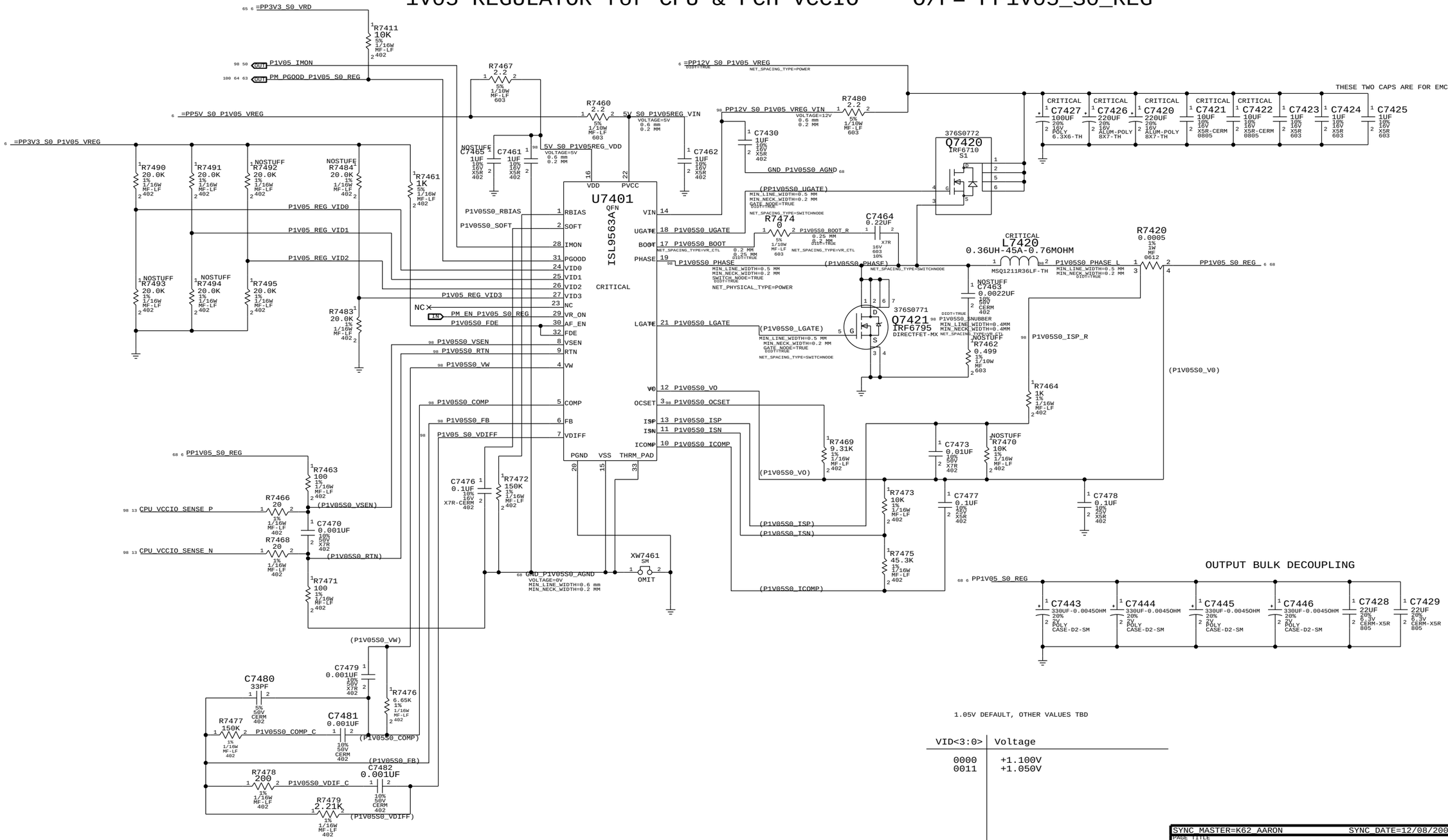
1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG



1.05V DEFAULT, OTHER VALUES TBD

VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

SYNC_MASTER=K62_AARON SYNC_DATE=12/08/2009

PAGE TITLE: 1V05 REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8442 SIZE: D

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CPU VCCSA 0.925V (8.8A MAX)

=PP3V3_S5_CPU_VCCSA — R7531 100 5% 1/10W MF-LF 402 — VCCSA_REF

CRITICAL
U7505 ISL21070 SOT23-3
VIN, VOUT, GND

C7515 1UF 10% 10V X5R 402
C7516 1UF 10% 10V X5R 402

C7551 10PF 5% 50V CERM 402

R7550 49.9K 1% 1/16W MF-LF 402 — VCCSA_FIL — C7550 560PF 10% 50V CERM 402

VCCSA_CNTRL_INPUT1

U7501 LM358-SOI-HF

VCCSA_OUT
NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

R7505 0 5% 1/10W MF-LF 402 — VCCSA_GATE
NET_PHYSICAL_TYPE=VR_CTL_PHY
DIDT=TRUE
NET_SPACING_TYPE=VR_CTL

Q7500 IRFH3702TRPBF PQFN
376S0910

=PPVCCIO_S0_CPU_VCCSA

NOTE: THIS RAIL IS COMING FROM PPVCCSA_S0_INPUT_SNS AFTER SENSE RES

NOSTUFF R7506 1K 5% 1/10W MF-LF 402
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE
NET_SPACING_TYPE=POWER

PPVCCSA_S0_FET

CRITICAL OMIT_TABLE
C7509 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM
CRITICAL OMIT_TABLE
C7510 220UF-25MOHM 20% 6V POLY-TANT CASE-D2E-SM
C7507 10UF 10% 6.3V X5R 805
C7508 10UF 10% 6.3V X5R 805

Place C7507 inside cavity
Place C7508 inside cavity

=PP12V_S0_CPU_VCCSA

R7504 2.2 5% 1/10W MF-LF 603

VCCSA_PWR_RC

C7502 1UF 10% 25V X5R 603-1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT,6V,220UF,25MOHM	C7509,C7510	

VCCSA_CNTRL_INPUT2 — R7507 5.49K 1% 1/16W MF-LF 402 — VCCSA_CNTRL_INPUT2_R — R7535 22 5% 1/10W MF-LF 402

R7533 10K 1% 1/16W MF-LF 402

NOSTUFF C7512 10PF 5% 50V CERM 402

R7552 1K 5% 1/16W MF-LF 402 — VCCSA_CRL — C7552 560PF 10% 50V CERM 402

CPU_VCCSA_SENSE — R7503 0 5% 1/10W MF-LF 402

C7501 100PF 5% 50V CERM 402

=PPVCCSA_S0_INPUT_PWR

CRITICAL
C7506 330UF-0.009OHM 20% 2V POLY CASE-D2-HF
C7504 4.7UF 20% 6.3V X5R-CERM1 402
C7505 0.1UF 20% 10V CERM 402

U7501 LM358-SOI-HF

NOTE: THIS POWER RAIL IS BEFORE THE SENSE RES R5310

SYNC_MASTER=K62_AARON SYNC_DATE=12/08/2009

PAGE TITLE
CPU VCCSA REGULATOR

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CPU VCORE 3 PHASE/4 PHASE BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES,1K,5%,0402	R7125	CPUVCORE-4PH
114S0303	1	RES,7.5K,5%,0402	R7125	CPUVCORE-3PH
114S0327	1	RES,13.7K,1%,0402	R7126	CPUVCORE-4PH
114S0316	1	RES,10.2K,1%,0402	R7126	CPUVCORE-3PH
114S0323	1	RES,12.4K,1%,0402	R7119	CPUVCORE-4PH
114S0316	1	RES,10.2K,1%,0402	R7119	CPUVCORE-3PH
114S0355	1	RES,26.1K,1%,0402	R7150	CPUVCORE-4PH
114S0338	1	RES,17.8K,1%,0402	R7150	CPUVCORE-3PH
114S0211	1	RES,845,1%,0402	R7153	CPUVCORE-4PH
116S0004	1	RES,0,1%,0402	R7153	CPUVCORE-3PH
114S0314	1	RES,9.76K,1%,0402	R7154	CPUVCORE-4PH
114S0316	1	RES,10.2K,1%,0402	R7154	CPUVCORE-3PH
114S0225	1	RES,1.21K,1%,0402	R7141	CPUVCORE-4PH
114S0217	1	RES,976,1%,0402	R7141	CPUVCORE-3PH
114S0335	1	RES,16.5K,1%,0402	R7142	CPUVCORE-4PH
114S0349	1	RES,23.2K,1%,0402	R7142	CPUVCORE-3PH
114S0331	1	RES,15K,1%,0402	R7143	CPUVCORE-3PH
114S0257	1	RES,2.55K,1%,0402	R7144	CPUVCORE-4PH
114S0252	1	RES,2.32K,1%,0402	R7144	CPUVCORE-3PH
114S0209	1	RES,806,1%,0402	R7130	CPUVCORE-4PH
114S0188	1	RES,487,1%,0402	R7130	CPUVCORE-3PH
116S0004	1	RES,0R,1%,0402	R7129	CPUVCORE-4PH
114S0189	1	RES,499,1%,0402	R7129	CPUVCORE-3PH
114S0219	1	RES,1.02K,1%,0402	R7136	CPUVCORE-4PH
114S0131	1	RES,130,1%,0402	R7136	CPUVCORE-3PH
132S8221	1	CAP,820PF,10%,0402	C7123	CPUVCORE-4PH
132S1534	1	CAP,0.0012UF,10%,0402	C7123	CPUVCORE-3PH

SYNC_MASTER=K62_AARON SYNC_DATE=12/08/2009

PAGE TITLE
CPU 3P/4P BOM OPTIONS

Apple Inc.

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3V3 S5 REGULATOR

3V3 OUTPUT

=PP12V_S5_P5VS3_VREG
NET_SPACING_TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6.3X6-TH
C7712 10UF 10% 16V X5R-CERM 0805
C7710 10UF 10% 16V X5R-CERM 0805
C7711 1UF 10% 16V X5R 603
C7722 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER
DIDT=TRUE

PP3V3_S5_REG
R7776 0.002 1% 1/4W MF-LF 1206
CRITICAL
L7710 2.2UH-14A MMD06CZ-SM
PP3V3_S5_REG_R
NET_PHYSICAL_TYPE=POWER
C7790 0.01UF 10% 16V CERM 402
R7790 15.8K 1% 1/16W MF-LF 402
R7791 15.8K 1% 1/16W MF-LF 402
C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF
NET_SPACING_TYPE=VR_CTL
R7730 0.499 1% 1/10W MF 603
P3V3S5_REG_SNUB
DIDT=TRUE

Q7710 RJK0384DPA WPAK 376S0801
D1
G1 1 (P3V3S5_UGATE)
MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM GATE_NODE=TRUE NET_SPACING_TYPE=VR_CONTROL
S1/D2 7
G2 6 (P3V3S5_LGATE)
MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM GATE_NODE=TRUE NET_SPACING_TYPE=VR_CONTROL
S2

C7714 0.1UF 10% 50V X7R 603-1
P3V3S5_REG_BOOT_R 98
MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM DIDT=TRUE NET_SPACING_TYPE=VR_CONTROL
(P3V3S5_PHASE)
R7710 0 5% 1/10W MF-LF 603
NET_SPACING_TYPE=VR_CONTROL MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM NET_SPACING_TYPE=SWITCHNODE NET_PHYSICAL_TYPE=POWER

PM_PGOOD_P3V3_S5_REG 100 64 27
P3V3S5_REG_UGATE 14
P3V3S5_REG_BOOT 15
P3V3S5_REG_PHASE 13
P3V3S5_REG_LGATE 16
P3V3S5_REG_ISEN 10
P3V3S5_REG_OCSET 11
P3V3S5_REG_VOUT1 9
P3V3S5_REG_FB 8

U7700 ISL62383 QFN CRITICAL

LDO5	18		
VCC1	5		
VCC2	4		
VIN	17	VIN_5V_S5_REG_RC	
FCCM	3	TP_P5VS3_REG_FCCM	
PGOOD1	7	PGOOD2	1
UGATE1	14	UGATE2	22 P5VS3_REG_UGATE
BOOT1	15	BOOT2	21 P5VS3_REG_BOOT
PHASE1	13	PHASE2	23 P5VS3_REG_PHASE
LGATE1	16	LGATE2	20 P5VS3_REG_LGATE
ISEN1	10	ISEN2	26 P5VS3_REG_ISEN
OCSET1	11	OCSET2	25 P5VS3_REG_OCSET
VOUT1	9	VOUT2	27 P5VS3_REG_VOUT2
FB1	8	FB2	28 P5VS3_REG_FB
FSET1	6	FSET2	2 P5VS3_REG_FSET2
EN1	12	EN2	24
THRM PAD	29	PGND	29

OUTPUT BULK DECOUPLING:
PLACEMENT_NOTE=PLACE NEXT TO C7716
C7715 10UF 10% 16V X5R-CERM 0805
C7717 10UF 10% 16V X5R-CERM 0805
128S0237 CRITICAL C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
XW7716 SM OMIT
R7720 45.3K 1% 1/16W MF-LF 402 <Ra>
R7721 10.0K 0.5% 1/16W MF 402 <Rb>
R7724 976 1% 1/16W MF-LF 402
P3V3S5_REG_FB_R
C7720 1000PF 5% 25V NP0-C0G 402
C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603
EMC CAPS PLACE CLOSE TO L
Vout = 0.6V * (1 + Ra / Rb)

R7722 68K 5% 1/16W MF-LF 402
R7723 33K 5% 1/16W MF-LF 402
PM_EN_P3V3_S5_REG 100
C7701 0.01UF 10% 16V CERM 402
R7701 16.5K 1% 1/16W MF-LF 402
PM_EN_P5V_S3_REG 100 63

C7719 100UF 20% 16V POLY 6.3X6-TH
C7766 100UF 20% 16V POLY 6.3X6-TH
C7767 100UF 20% 16V POLY 6.3X6-TH
C7768 100UF 20% 16V POLY 6.3X6-TH
C7758 10UF 10% 16V X5R-CERM 0805
C7765 10UF 10% 16V X5R-CERM 0805

=PP12V_S5_P5VS3_VREG 6 71
NOSTUFF
R7725 20K 5% 1/16W MF-LF 402

=PP3V3_S5_VRD 6
R7726 20K 5% 1/16W MF-LF 402

PP5V_S5_LDO 6
EMC: C7754,C7755 PLACE AT Q7330
C7754 1UF 10% 16V X5R 603
C7755 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER
C7742 4.7UF 20% 6.3V CERM 603
R7740 2.2 5% 1/8W MF-LF 805
P5V_S5_LDO_R
R7741 1 5% 1/8W MF-LF 805
P5V_S5_VCC1
C7740 1UF 10% 16V X5R 603
C7741 1UF 10% 16V X5R 603
C7743 1UF 10% 16V X5R 603

PM_PGOOD_P5V_S3_REG 63 83 100 OUT
CRITICAL Q7750 FDMS0346 POWER56 376S0875
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2 MM NET_SPACING_TYPE=VR_CONTROL
P5VS3_REG_BOOT_R MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.6MM NET_SPACING_TYPE=VR_CONTROL
R7750 0 5% 1/10W MF-LF 603 DIDT=TRUE
C7756 0.1UF 10% 25V X5R 402
NET_SPACING_TYPE=SWITCHNODE DIDT=TRUE NET_PHYSICAL_TYPE=POWER
NOSTUFF C7757 0.001UF 10% 50V CERM 402
5V_SNUBBER DIDT=TRUE MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2 MM NET_SPACING_TYPE=SWITCHNODE
R7752 0.499 1% 1/10W MF 603 NOSTUFF
CRITICAL Q7751 FDMS0355S POWER56 376S0917
MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.6MM NET_SPACING_TYPE=VR_CONTROL

C7747 0.01UF 10% 16V CERM 402
R7747 16.5K 1% 1/16W MF-LF 402
NOSTUFF C7777 0.001UF 10% 50V CERM 402

R7759 976 1% 1/16W MF-LF 402
P5VS5_REG_FB_R
C7759 1000PF 5% 25V NP0-C0G 402
R7755 75K 1% 1/16W MF-LF 402 RA
R7756 10K 1% 1/16W MF-LF 402 RB

5V S3 REGULATOR

Power Rating ?

5V OUTPUT

EMC: C7763,C7764 PLACE AT L7750.2
C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

PP5V_S3_REG 6
R7775 0.002 1% 1/4W MF-LF 1206
CRITICAL L7750 2.2UH+/-20%-0.0069OHM-16A PIC1005H-SM
PP5V_S3_REG_R
NET_PHYSICAL_TYPE=POWER
R7770 9.76K 1% 1/16W MF-LF 402
C7770 27.0NF 10% 10V X5R 402
R7771 9.76K 1% 1/16W MF-LF 402

OUTPUT BULK DECOUPLING:
C7760 10UF 20% 6.3V CERM 805-1
C7769 10UF 20% 6.3V CERM 805-1
CRITICAL C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
CRITICAL C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
XW7751 SM OMIT

SYNC_MASTER=K62_AARON	SYNC_DATE=12/08/2009
PAGE TITLE	5V_S3 / 3V3_S5 VREGS
Apple Inc.	DRAWING NUMBER 051-8442 SIZE D
	REVISION 10.1.0
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1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A

=PP12V_S5_DDR_VREG
=PP5V_S3_DDR_VREG
=PP3V3_S3_VRD
PM_EN_DDRVTT_S0_REG
PM_EN_DDR1V5_S3_REG
PM_PGOOD_DDR1V5_S3_REG
TP_PPVTT_S3_DDR_BUF (NOT USED)
PPVTT_S0_DDR_LDO
PP5V_S3_DDR_REG_V5FILT
NET_PHYSICAL_TYPE=POWER
NET_SPACING_TYPE=POWER

U7800 TPS51116 QFN SYM (2 OF 2)
CRITICAL

R7801 4.7 5% 1/16W MF-LF 402
R7820 10K 5% 1/16W MF-LF 402
C7800 4.7UF 20% 6.3V CERM 603
C7801 1UF 10% 16V X5R 402
C7815 10UF 20% 6.3V X5R 603
R7810 3.57K 1% 1/16W MF-LF 402
C7830 270UF 20% 16V ELEC 8X9-TH1
C7831 270UF 20% 16V ELEC 8X9-TH1
C7832 10UF 10% 16V X5R-CERM 0805
EMC CAPS PLACE CLOSE TO FET
C7833 1UF 10% 16V X5R 603
C7834 1UF 10% 16V X5R 603
R7841 4.7 5% 1/16W MF-LF 603
C7840 0.1UF 20% 25V CERM 603
R7840 0 5% 1/10W MF-LF 603
Q7830 CSD58864Q5D SON5X6
L7830 1.5UH-15%-22A-3.3MOHM SDP1182M-TH
EMC CAPS PLACE CLOSE TO L7830
C7838 0.001UF 10% 50V X7R 402
C7839 0.001UF 10% 50V X7R 402
C7835 330UF 20% 2.5V POLY-TANT CASE-D2E-SM3
C7836 330UF 20% 2.5V POLY-TANT CASE-D2E-SM3
C7837 10UF 20% 6.3V X5R 603
C7841 1000PF 5% 25V NP0-C0G 402
R7831 0.499 1% 1/10W MF 603
C7804 22UF 20% 6.3V CERM-X5R 805-3
C7803 22UF 20% 6.3V CERM-X5R 805-3
C7805 0.033UF 10% 16V X5R 402
C7820 100PF 5% 50V CERM 402
R7832 15.0K 1% 1/16W MF-LF 402 <Ra>
R7833 15.0K 1% 1/16W MF-LF 402 <Rb>
XW7803 OMIT
XW7800 OMIT
XW7801 OMIT
XW7831 OMIT
XW7830 OMIT

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

Vout = 0.75V * (1 + Ra / Rb)

OUTPUT BULK DECOUPLING:

1.8 V SUPPLY

=PP5V_S0_P1V8_REG
PM_EN_P1V8_S0_REG
PM_PGOOD_P1V8_S0_REG
P1V8_REG_SYNC
CONTINUOUS MODE

U7850 ISL8013A QFN CRITICAL

C7854 22UF 20% 6.3V X5R-CERM-1 603
C7855 22UF 20% 6.3V X5R-CERM-1 603
R7853 100K 5% 1/16W MF-LF 402
R7854 100K 5% 1/16W MF-LF 402
NOSTUFF R7860 100K 5% 1/16W MF-LF 402
L7850 1.5UH-4A MMD04BZ-SM
C7850 47PF 5% 50V 402 CERM
R7850 59.0K 1% 1/16W MF-LF 402 <Ra>
R7851 47.0K 1% 1/16W MF-LF 402 <Rb>
C7852 22UF 20% 6.3V X5R-CERM-1 603
C7853 22UF 20% 6.3V X5R-CERM-1 603

Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V

1A Average current

SYNC_MASTER=K62_AARON	SYNC_DATE=11/30/2009
PAGE TITLE: 1.5V / 1.8V VREGS	
Apple Inc.	DRAWING NUMBER: 051-8442 SIZE: D
	REVISION: 10.1.0
	BRANCH:
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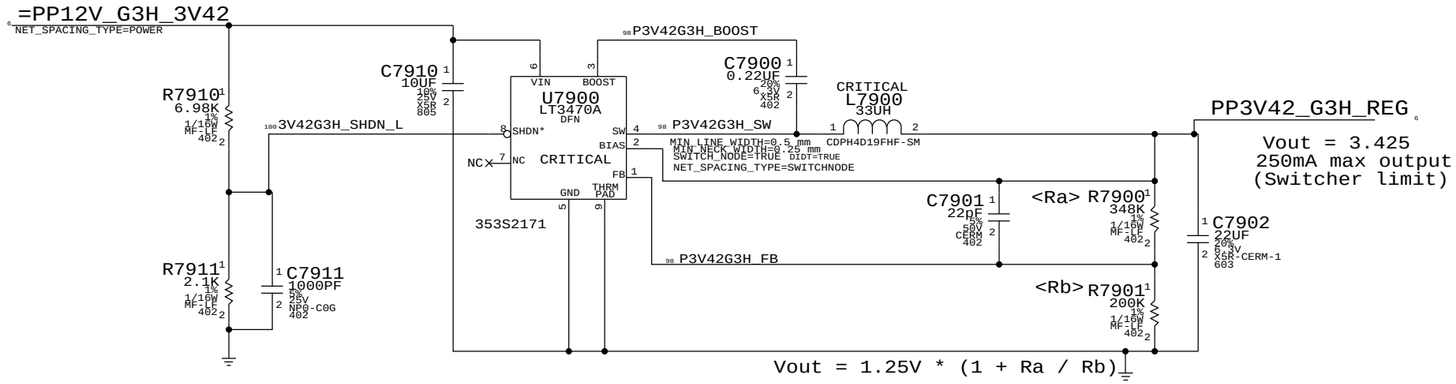
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC_MASTER=K62_AARON	SYNC_DATE=N/A
PAGE TITLE: 3.42 G3HOT SUPPLY	
Apple Inc.	DRAWING NUMBER: 051-8442 SIZE: D
	REVISION: 10.1.0
	BRANCH:
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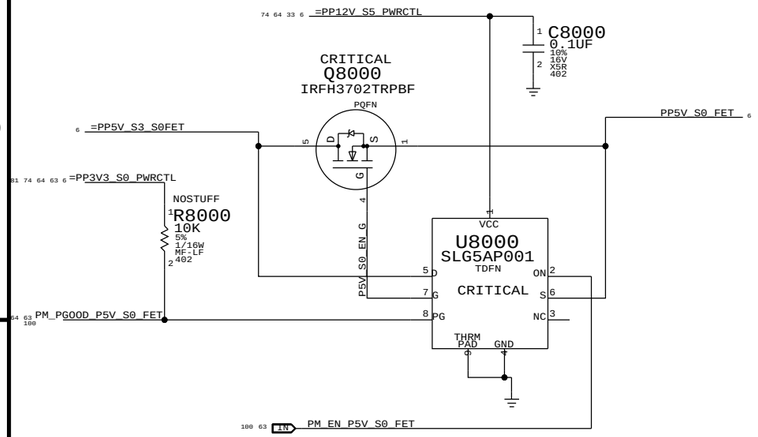
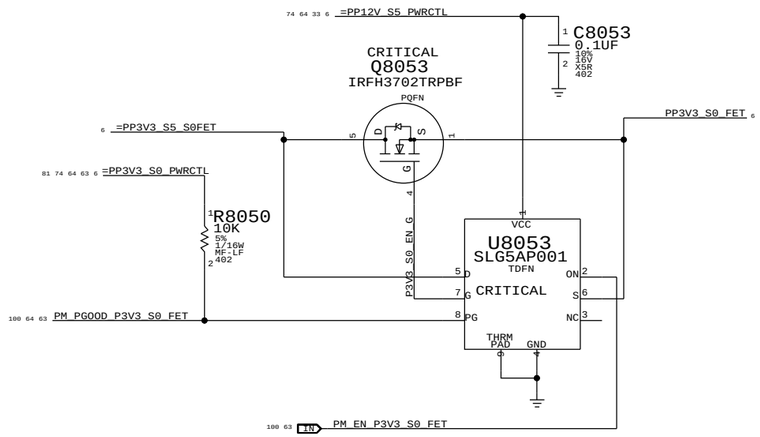
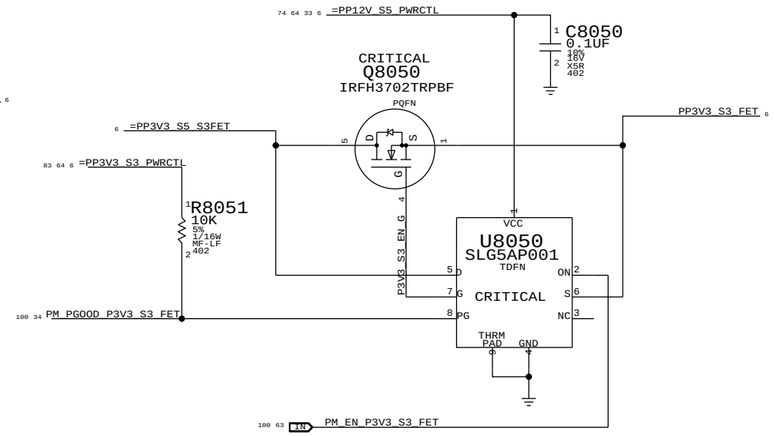
5V S0 FET (6.6A PK/3.1A AVG)



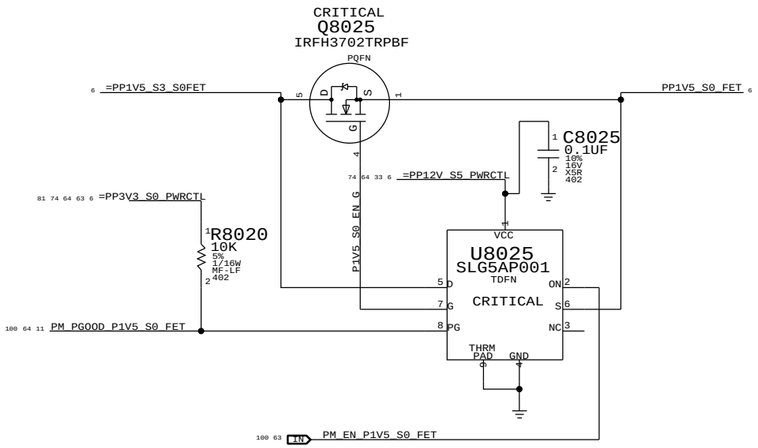
3.3V S0 FET (2.9APK / 2.0A AVG)



3.3V S3 FET (3.4A PK / 1.6A AVG)



1.5V S0 FET (4.8A PK / 4.8A AVG)



SYNC_MASTER=K62_AARON	SYNC_DATE=04/07/2010
PAGE TITLE: S3+S0 FETS	
Apple Inc.	DRAWING NUMBER: 051-8442 · SIZE: D
	REVISION: 10.1.0
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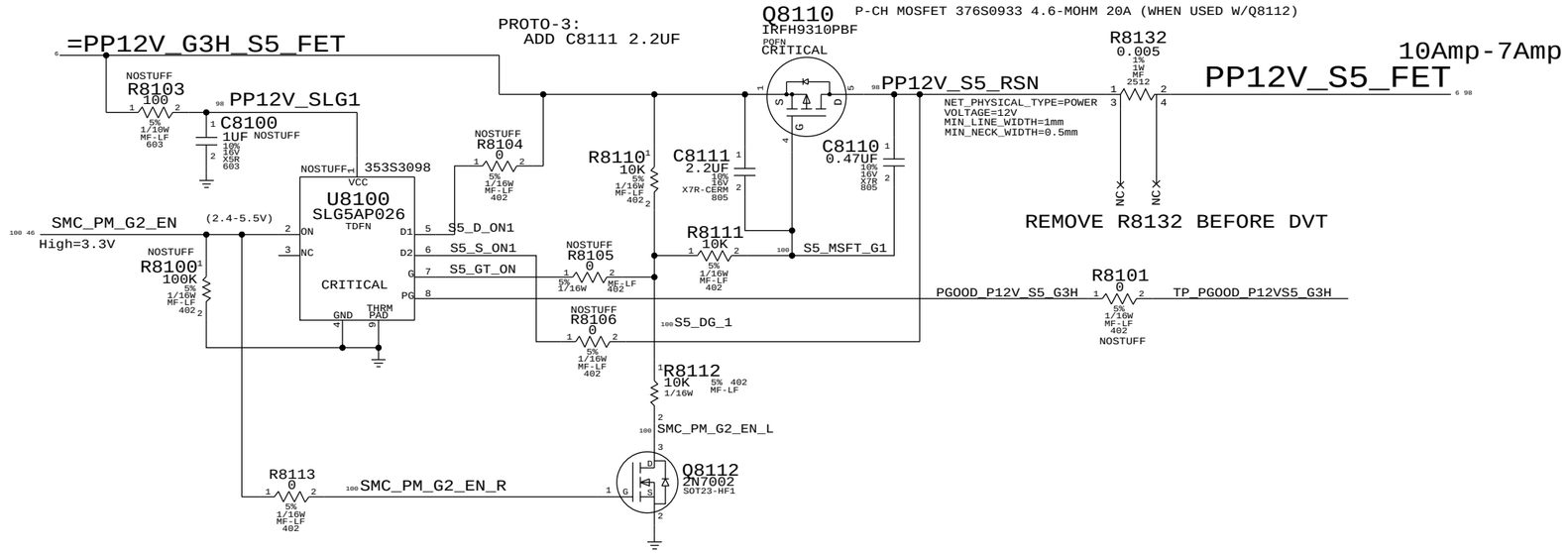
THE NMOS PMOS SHARING FOOTPRINT WILL NOT WORK DUE TO THE REVERSE POLARITY OF BODY DIODE.



SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

PAGE TITLE
12V_S0 & 12V_S5 switch

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D

REVISION 10.1.0

BRANCH

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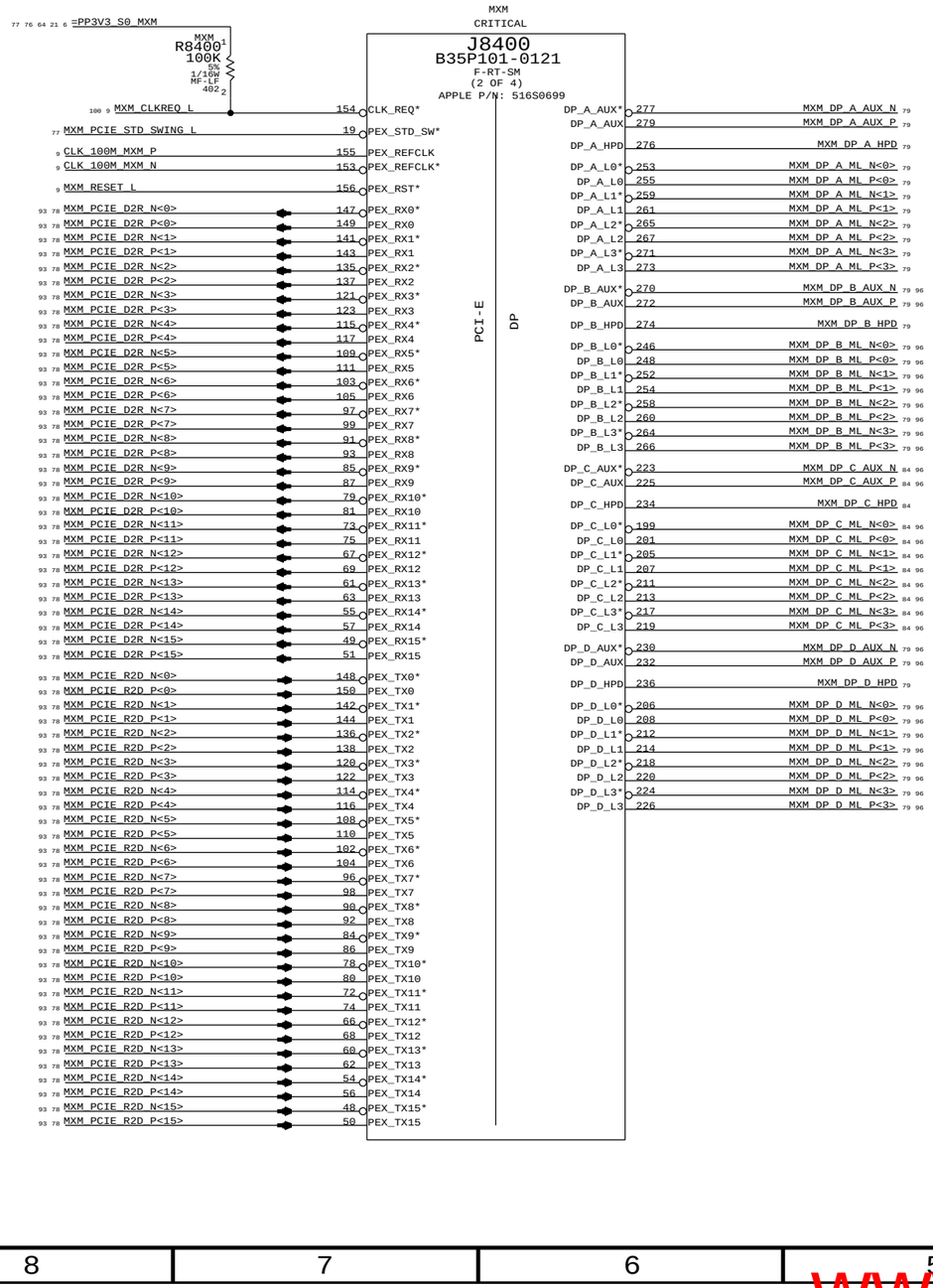
SHEET 75 OF 101

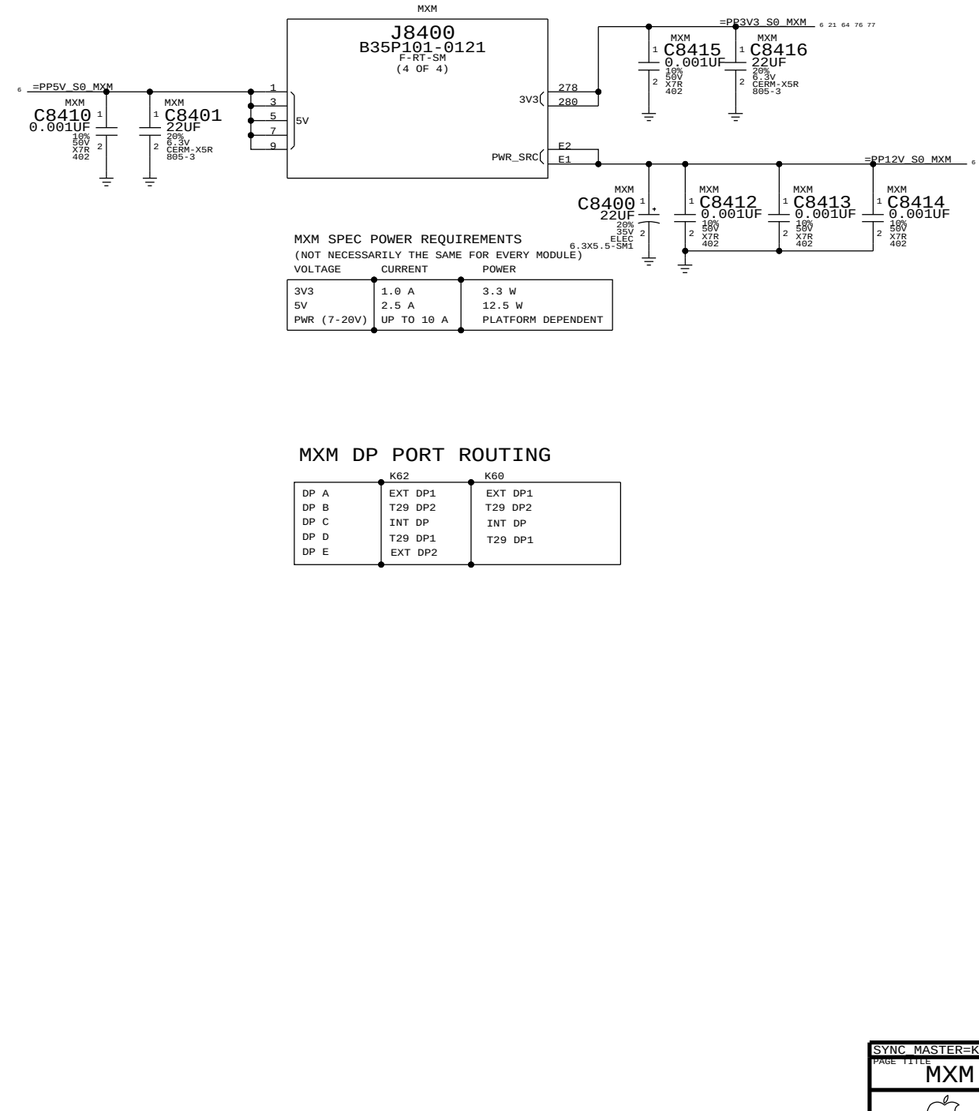
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM DP PORT ROUTING

	K62	K60
DP A	EXT DP1	EXT DP1
DP B	T29 DP2	T29 DP2
DP C	INT DP	INT DP
DP D	T29 DP1	T29 DP1
DP E	EXT DP2	

SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8442 SIZE D
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SHEET 76 OF 101

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

MXM
J8400
B35P101-0121
F-RT-SM
(1 OF 4)

LVDS
79 MXM_DP_E_AUX_P 35 LVDS_DDC_CLK
79 MXM_DP_E_AUX_N 33 LVDS_DDC_DAT
79 MXM_DP_E_HPD 31 DVI_HPD
79 MXM_DP_E_ML_N<3> 176 LVDS_LCLK*
79 MXM_DP_E_ML_P<3> 178 LVDS_LCLK
79 MXM_DP_E_ML_N<2> 200 LVDS_LTX0*
79 MXM_DP_E_ML_P<2> 202 LVDS_LTX0
79 MXM_DP_E_ML_N<1> 194 LVDS_LTX1*
79 MXM_DP_E_ML_P<1> 196 LVDS_LTX1
79 MXM_DP_E_ML_N<0> 188 LVDS_LTX2*
79 MXM_DP_E_ML_P<0> 190 LVDS_LTX2
96 79 MXM_LVDS_A_DATA_N<3> 182 LVDS_LTX3*
96 79 MXM_LVDS_A_DATA_P<3> 184 LVDS_LTX3
96 79 MXM_LVDS_B_CLK_N 169 LVDS_UCLK*
96 79 MXM_LVDS_B_CLK_P 171 LVDS_UCLK
96 79 MXM_LVDS_B_DATA_N<0> 193 LVDS_UTX0*
96 79 MXM_LVDS_B_DATA_P<0> 195 LVDS_UTX0
96 79 MXM_LVDS_B_DATA_N<1> 187 LVDS_UTX1*
96 79 MXM_LVDS_B_DATA_P<1> 189 LVDS_UTX1
96 79 MXM_LVDS_B_DATA_N<2> 181 LVDS_UTX2*
96 79 MXM_LVDS_B_DATA_P<2> 183 LVDS_UTX2
96 79 MXM_LVDS_B_DATA_N<3> 175 LVDS_UTX3*
96 79 MXM_LVDS_B_DATA_P<3> 177 LVDS_UTX3

SYSTEM MANAGEMENT
MANAGEMENT POWER/THERMAL
100 64 PM_MXM_EN 8 PWR_EN
100 77 64 PM_MXM_PGOOD 6 PWRGOOD
47 MXM_PWR_LEVEL 18 PWR_LEVEL
49 =SMB_MXM_THRM_SCL 34 SMB_CLK
49 =SMB_MXM_THRM_SDA 32 SMB_DAT
47 MXM_ALERT_L 22 TH_ALERT*
47 MXM_OVERT_L 20 TH_OVERT*
TP_MXM_TH_PWM 24 TH_PWM

ANALOG DISPLAY
TP_MXM_VGA_DDC_CLK 160 VGA_DDC_CLK
TP_MXM_VGA_DDC_DAT 158 VGA_DDC_DAT
TP_MXM_VGA_BLUE 172 VGA_BLUE
TP_MXM_VGA_GREEN 170 VGA_GREEN
TP_MXM_VGA_HSYNC 164 VGA_HSYNC
TP_MXM_VGA_RED 168 VGA_RED
TP_MXM_VGA_VSYNC 162 VGA_VSYNC

VGA_DISABLE* 21 MXM_VGA_DISABLE_L 77
GPIO0 26 TP_MXM_GPIO0
GPIO1 28 TP_MXM_GPIO1
GPIO2 30 TP_MXM_GPIO2
HDMI_CEC 29 TP_MXM_HDMI_CEC
OEM0 38
OEM1 39
OEM2 40
OEM3 41
OEM4 42
OEM5 43
OEM6 44
OEM7 45
PNL_BL_EN 25 MXM_PNL_BL_EN 79
PNL_BL_PWM 27 MXM_PNL_BL_PWM 84 100
PNL_PWR_EN 23 MXM_PNL_PWR_EN 79
77 76 64 21 6 =PP3V3_S0_MXM
RSVD0 10
RSVD1 159 TP_MXM_N_TDO
RSVD2 12
RSVD3 161 TP_MXM_N_TDI
RSVD4 163 TP_MXM_N_TCK
RSVD5 165 TP_MXM_N_TMS
RSVD6 167 TP_MXM_N_TRST_L
RSVD7 227 MXM_A_TESTEN
RSVD8 229 TP_MXM_A_TRST_L
RSVD9 231 TP_MXM_A_TDO
RSVD10 233 TP_MXM_A_TDI
RSVD11 235 TP_MXM_A_TMS
RSVD12 237 TP_MXM_A_TCK
RSVD13 238
RSVD14 239
RSVD15 240
RSVD16 241
RSVD17 242
RSVD18 243
RSVD19 245
RSVD20 247
RSVD21 249
RSVD22 14
RSVD23 16
PRSNT_L* 281 MXM_DETECT_L 77
PRSNT_R* 2 MXM_DETECT_R 77
WAKE* 4 TP_MXM_WAKE_L

NOSTUFF
R8579 4.7K 5% 1/16W MF-LF 402 1 2
NOSTUFF
R8580 4.7K 5% 1/16W MF-LF 402 1 2

MXM
J8400
B35P101-0121
F-RT-SM
(3 OF 4)

GND: 11 13 15 17 36 37 46 47 52 53 58 59 64 65 70 71 76 77 82 83 88 89 94 95 100 101 106 107 112 113 118 119 124 125 133 134 139 140
GND: 145 146 151 152 157 166 173 174 179 180 185 186 191 192 197 198 203 204 209 210 215 216 221 222 228 244 E3 250 251 256 257 262 263 268 269 275 282 283 E4

PULLUPS & PULLDOWNS AT MXM CONNECTOR

FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD
NOSTUFF
R8510 0 MF-LF 5% 1/16W 402 1 2
77 MXM_VGA_DISABLE_L

FLOAT = LOW SWING
GND = HIGH SWING
MXM
R8504 0 MF-LF 5% 1/16W 402 1 2
76 MXM_PCIE_STD_SWING_L

=PP3V3_S0_MXM 6 21 64 76 77
R8500 100K MF-LF 5% 1/16W 402 1 2
77 MXM_DETECT_L
PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT
R8501 100K MF-LF 5% 1/16W 402 1 2
77 MXM_DETECT_R

=PM_MXM_PGOOD_PULLUP 64
SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR
R8503 10K MF-LF 5% 1/16W 402 1 2
100 77 64 PM_MXM_PGOOD

SYNC_MASTER=K62_AARON SYNC_DATE=N/A
PAGE TITLE: MXM I/O
Apple Inc.
DRAWING NUMBER: 051-8442
SIZE: D
REVISION: 10.1.0
BRANCH:
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MXM TX CAPS

PEG_R2D_C_P<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>
PEG_R2D_C_N<0>	MXM	C8601	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>
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PEG_R2D_C_P<2>	MXM	C8605	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>
PEG_R2D_C_P<3>	MXM	C8606	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>
PEG_R2D_C_N<3>	MXM	C8607	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>
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PEG_R2D_C_P<4>	MXM	C8609	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>
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PEG_R2D_C_P<5>	MXM	C8611	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>
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PEG_R2D_C_P<11>	MXM	C8623	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>
PEG_R2D_C_P<12>	MXM	C8624	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>
PEG_R2D_C_N<12>	MXM	C8625	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>
PEG_R2D_C_N<13>	MXM	C8626	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>
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PEG_R2D_C_N<14>	MXM	C8629	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>
PEG_R2D_C_N<15>	MXM	C8630	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>
PEG_R2D_C_P<15>	MXM	C8631	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>

MXM RX CAPS

MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<0>
MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<0>
MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<1>
MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<1>
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MXM_PCIE_D2R_N<13>	MXM	C8637	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<2>
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MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<3>
MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<4>
MXM_PCIE_D2R_N<11>	MXM	C8641	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<4>
MXM_PCIE_D2R_P<10>	MXM	C8642	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<5>
MXM_PCIE_D2R_N<10>	MXM	C8643	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<5>
MXM_PCIE_D2R_P<9>	MXM	C8644	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<6>
MXM_PCIE_D2R_N<9>	MXM	C8645	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<6>
MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<7>
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MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>
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MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<14>
MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<15>
MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<15>

SYNC_MASTER=K62 SYNC_DATE=N/A

PAGE TITLE
MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8442 | SIZE D
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Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

76	MXM_DP_A_ML_P<0..3>	DP_EXTA_ML_C_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	85 96
76	MXM_DP_A_ML_N<0..3>	DP_EXTA_ML_C_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	85 96
76	MXM_DP_A_AUX_P	DP_EXTA_AUXCH_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	79 85 96
76	MXM_DP_A_AUX_N	DP_EXTA_AUXCH_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	79 85 96
76	MXM_DP_A_HPD	DP_EXTA_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	85
77	MXM_DP_E_ML_P<0..3>	DP_EXTB_ML_C_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	87 96
77	MXM_DP_E_ML_N<0..3>	DP_EXTB_ML_C_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	87 96
77	MXM_DP_E_AUX_P	DP_EXTB_AUXCH_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	79 87 96
77	MXM_DP_E_AUX_N	DP_EXTB_AUXCH_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	79 87 96
77	MXM_DP_E_HPD	DP_EXTB_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	87

DDC/AUX ALIAS

96 85 79	DP_EXTA_AUXCH_C_P	DP_EXTA_DDC_CLK	MAKE_BASE=TRUE	85
96 85 79	DP_EXTA_AUXCH_C_N	DP_EXTA_DDC_DATA	MAKE_BASE=TRUE	85
96 87 79	DP_EXTB_AUXCH_C_P	DP_EXTB_DDC_CLK	MAKE_BASE=TRUE	87
96 87 79	DP_EXTB_AUXCH_C_N	DP_EXTB_DDC_DATA	MAKE_BASE=TRUE	87

NO_TEST T29 & DP DC BIAS

H63	T29_A_BIAS_R2D_P0		NO_TEST=TRUE	85 86
F62	T29_A_BIAS_R2D_N0		NO_TEST=TRUE	85 86
H64	T29_A_BIAS_R2D_P1		NO_TEST=TRUE	85 86
H64	T29_A_BIAS_R2D_N1		NO_TEST=TRUE	85 86
H64	T29_A_BIAS		NO_TEST=TRUE	83 85 86 99
H66	T29_A_BIAS_P0		NO_TEST=TRUE	86
F119	T29_A_BIAS_N0		NO_TEST=TRUE	86
H68	DP_A_BIAS_P_0		NO_TEST=TRUE	85 86
H68	DP_A_BIAS_N_0		NO_TEST=TRUE	85 86
F62	DP_A_BIAS_P_2		NO_TEST=TRUE	85 86
H64	DP_A_BIAS_N_2		NO_TEST=TRUE	85 86
H64	DP_A_BIAS		NO_TEST=TRUE	85 99
H69	T29_B_BIAS_R2D_P2		NO_TEST=TRUE	87 88
H68	T29_B_BIAS_R2D_N2		NO_TEST=TRUE	87 88
H69	T29_B_BIAS_R2D_P3		NO_TEST=TRUE	87 88
H69	T29_B_BIAS_R2D_N3		NO_TEST=TRUE	87 88
H69	T29_B_BIAS		NO_TEST=TRUE	83 87 88 99
H69	T29_B_BIAS_P3		NO_TEST=TRUE	88
H119	T29_B_BIAS_N3		NO_TEST=TRUE	88
H69	DP_B_BIAS_P_3		NO_TEST=TRUE	87 88
H68	DP_B_BIAS_N_3		NO_TEST=TRUE	87 88
H69	DP_B_BIAS_P_2		NO_TEST=TRUE	87 88
H68	DP_B_BIAS_N_2		NO_TEST=TRUE	87 88
H68	DP_B_BIAS		NO_TEST=TRUE	87

T29 CONN POWER AND CONTROL ALIAS

0	=PP3V3_SW_DPAPWR	PP3V3_SW_DPAPWR		85 98
0	=PP3V3_SW_DPBPWR	PP3V3_SW_DPBPWR		87 98
100 36 33 19	PCIE_WAKE_L	=T29_WAKE_L		85 87
96 76	MXM_DP_B_ML_P<0..3>	DP_T29SNK1_ML_C_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
96 76	MXM_DP_B_ML_N<0..3>	DP_T29SNK1_ML_C_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
96 76	MXM_DP_B_AUX_P	DP_T29SNK1_AUXCH_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
96 76	MXM_DP_B_AUX_N	DP_T29SNK1_AUXCH_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
76	MXM_DP_B_HPD	DP_T29SNK1_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	89
96 76	MXM_DP_D_ML_P<0..3>	DP_T29SNK0_ML_C_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
96 76	MXM_DP_D_ML_N<0..3>	DP_T29SNK0_ML_C_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
96 76	MXM_DP_D_AUX_P	DP_T29SNK0_AUXCH_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
96 76	MXM_DP_D_AUX_N	DP_T29SNK0_AUXCH_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	89 99
76	MXM_DP_D_HPD	DP_T29SNK0_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	89

UNUSED MXM CONTROL SIGNALS

77	MXM_PNL_BL_EN	NC_MXM_PNL_BL_EN	MAKE_BASE=TRUE NO_TEST=TRUE	
77	MXM_PNL_PWR_EN	NC_MXM_PNL_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE	

Unused MXM Interfaces

96 77	MXM_LVDS_A_DATA_N<3>	NC_MXM_LVDS_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_A_DATA_P<3>	NC_MXM_LVDS_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_CLK_N	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_CLK_P	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_N<0>	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_P<0>	NC_MXM_LVDS_B_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_N<1>	NC_MXM_LVDS_B_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_P<1>	NC_MXM_LVDS_B_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_N<2>	NC_MXM_LVDS_B_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_P<2>	NC_MXM_LVDS_B_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_N<3>	NC_MXM_LVDS_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	
96 77	MXM_LVDS_B_DATA_P<3>	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	

SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE
DP ALIAS

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System RTC Power Source & 32kHz / 25MHz Clock Generator

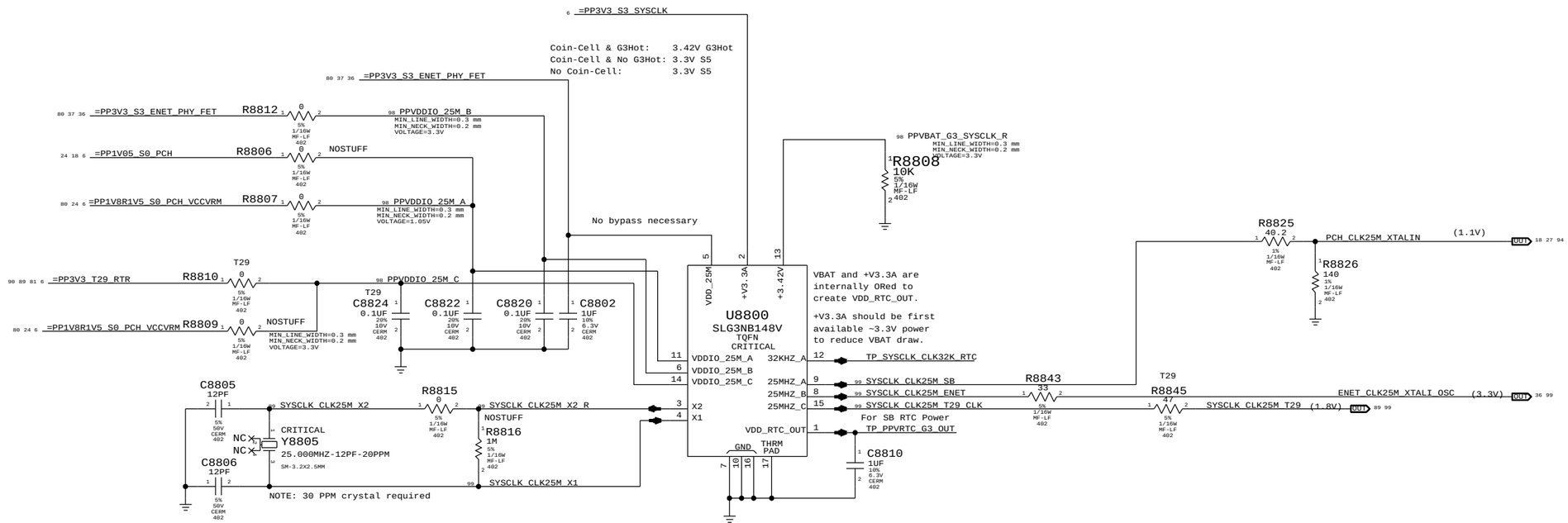
GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary



SYNC MASTER=K62_AARON	SYNC_DATE=N/A
PAGE TITLE: GREEN CLOCK	
Apple Inc.	DRAWING NUMBER: 051-8442 SIZE: D
	REVISION: 10.1.0
	BRANCH:
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Page Notes

Power aliases required by this page:
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:
(NONE)

Supervisor & CLKREQ# Isolation

=PP3V3_S0_T29PWRCTL

T29 C8900 0.1UF 10% 25V X5R 402

R8906 10K 5% 1/16W MF-LF 402

T29 CRITICAL U8900 SLG4AP016V TDFN

VDD

=PP3V3_T29_RTR

T29 R8907 100K 5% 1/16W MF-LF 402

=PP1V05_T29

SENSE 0.7V

Platform (PCIe) Reset

T29_RESET_L

R8903 10K 5% 1/16W MF-LF 402

DLY

RESET*

T29_RESET_RTR_L

DLY = 60 ms +/- 20%

Open-Drain GPIO

T29_SW_RESET_L

MR*

EN

OUT (OD)

IN

=T29_CLKREQ_L

T29_CLKREQ_ISOL_L

MAKE_BASE=TRUE

GND

THRM PAD

T29 CLKREQ# ISOLATION

=PP3V3_T29_RTR

T29 R8904 10K 5% 1/16W MF-LF 402

T29 Q8950 SSM3K15FV SOD-VESM-HF

T29_CLKREQ_L

T29_CLKREQ_FET_L

Pull-up provided by SB page.

3.3V T29 Switch

=PP3V3_S0_P3V3T29FET

U8910 TPS22924 CSP

VIN VOUT ON GND

T29 CRITICAL

T29 C8910 1UF 10% 6.3V CERM 402

PP3V3_T29_FET

Max Current = 1.7A (85C)

U8910

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.05V T29 Switch

=PP12V_S0_PWRCTL

T29 C8930 0.1UF 10% 16V X5R 402

CRITICAL Q8930 BSZ035N03MSG P-TSDSON-8

T29

=PP1V05_S0_P1V05T29FET

PP1V05_T29_FET

=PP3V3_S0_PWRCTL

T29 R8930 10K 5% 1/16W MF-LF 402

P1V05_S0_T29_EN

U8930 SLG5AP001 TDFN

VCC

D ON G S PG NC

CRITICAL

T29

THRM PAD GND

PM_PGOOD_P1V05_S0_T29_FET

T29_PWR_EN

SYNC_MASTER=K62_AARON	SYNC_DATE=(MASTER)
PAGE TITLE	T29 POWER
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Page Notes

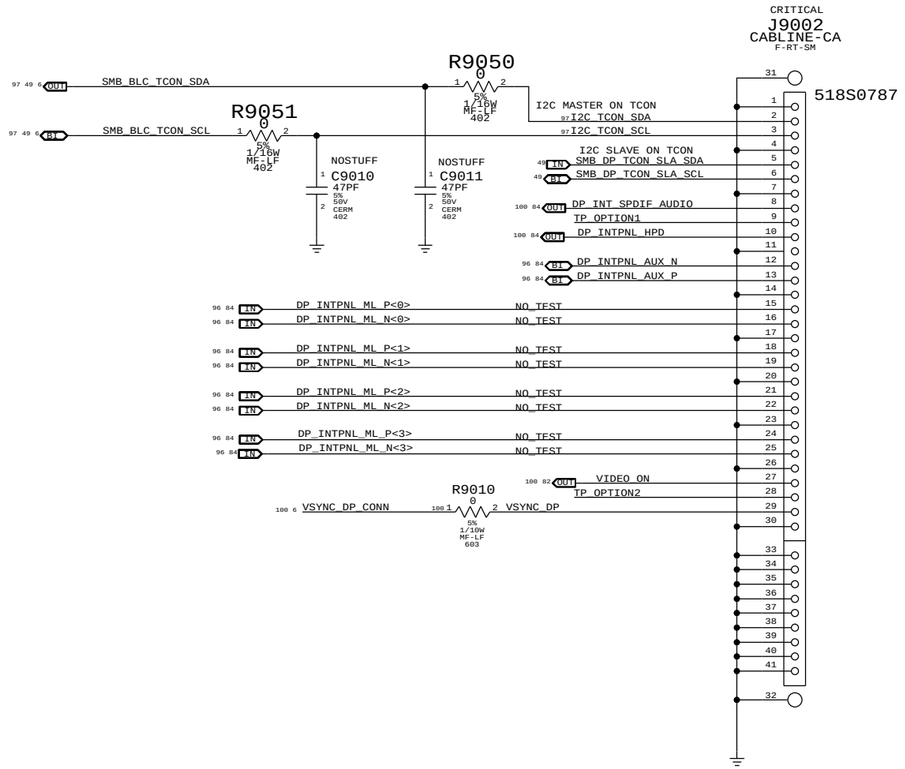
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

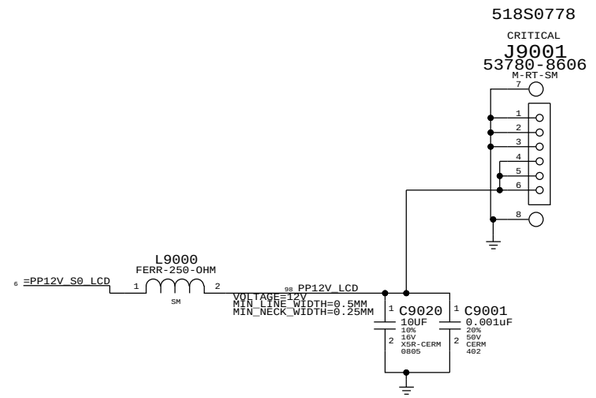
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

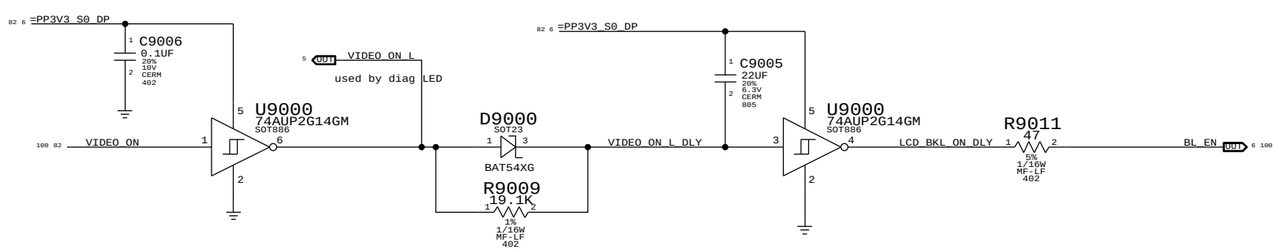


INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE
Display: Int DP Connector

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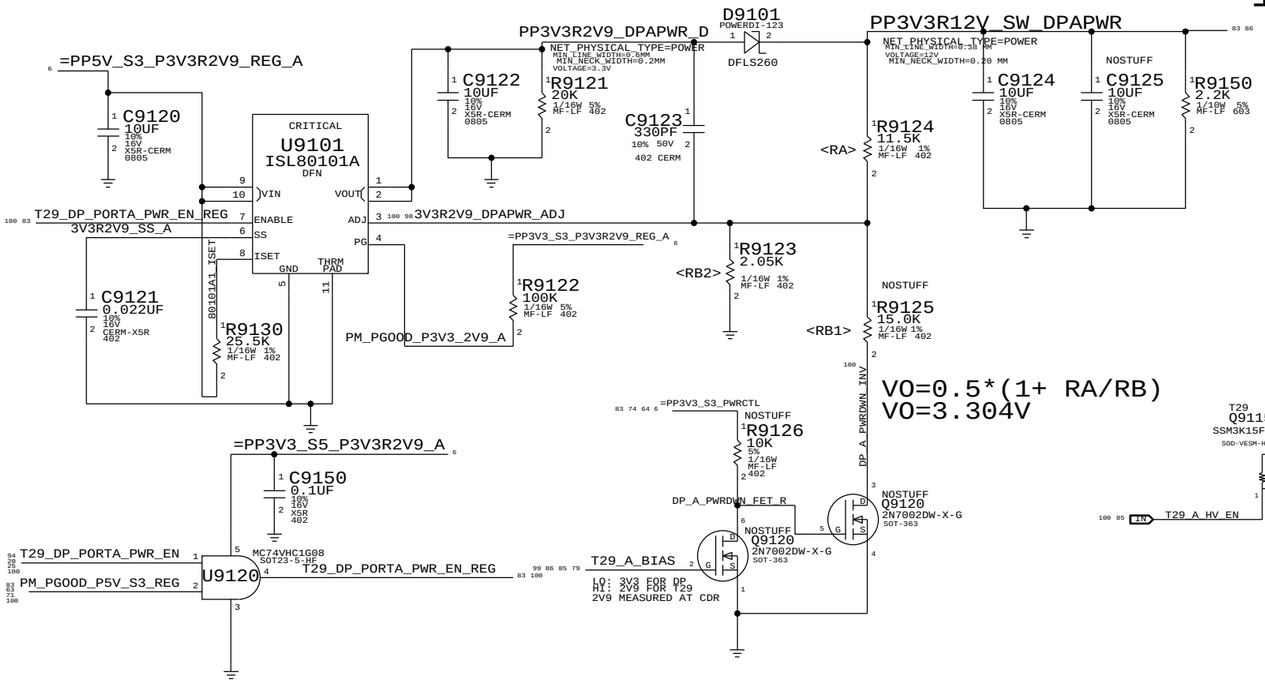
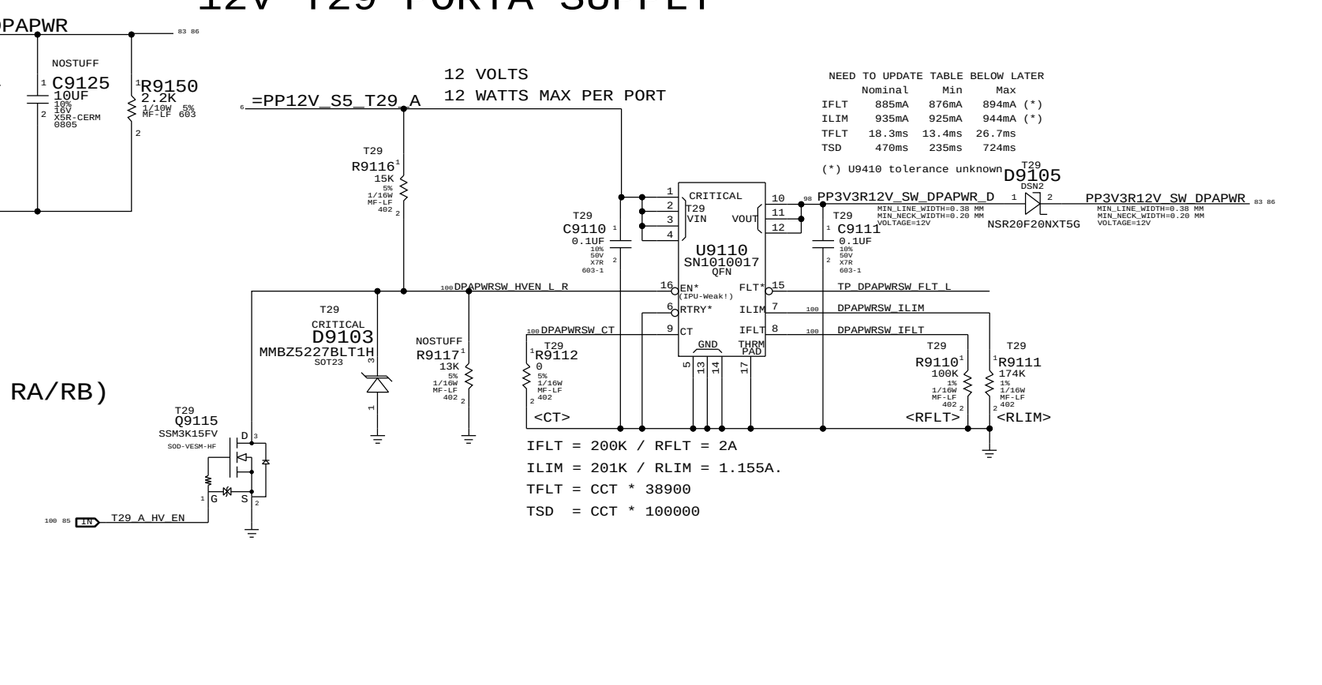
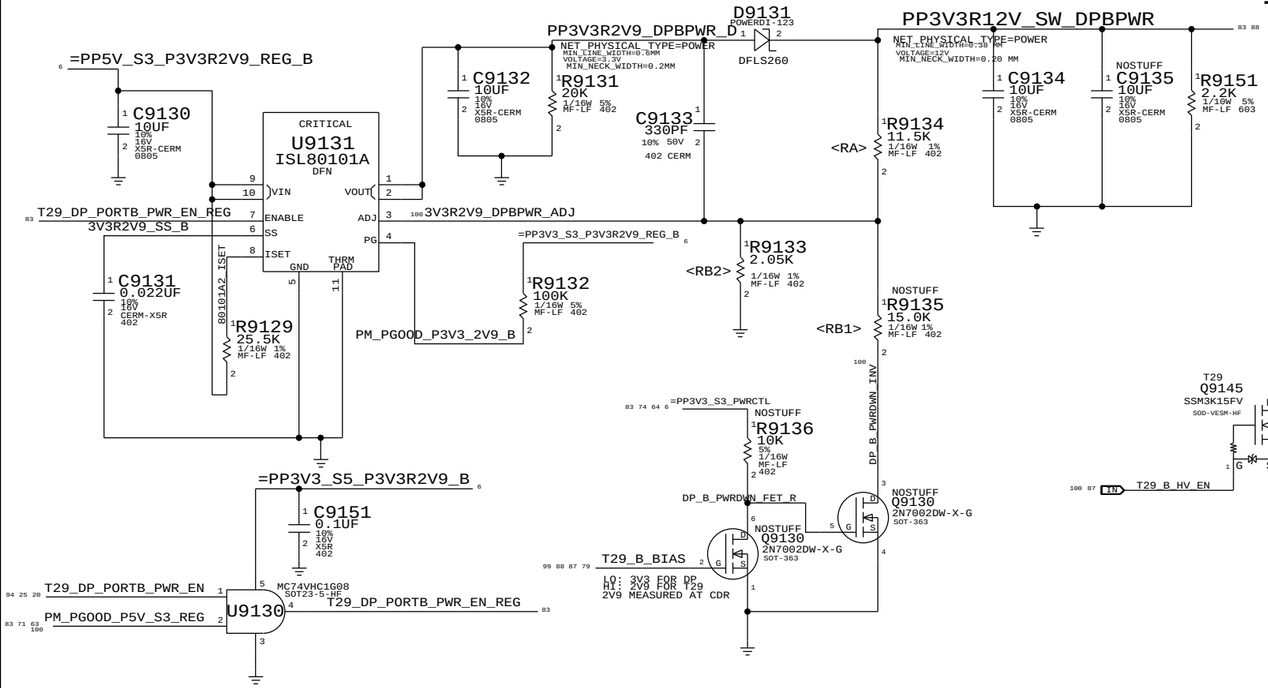
3V3(DP)/2V9(T29) PORTA SUPPLY



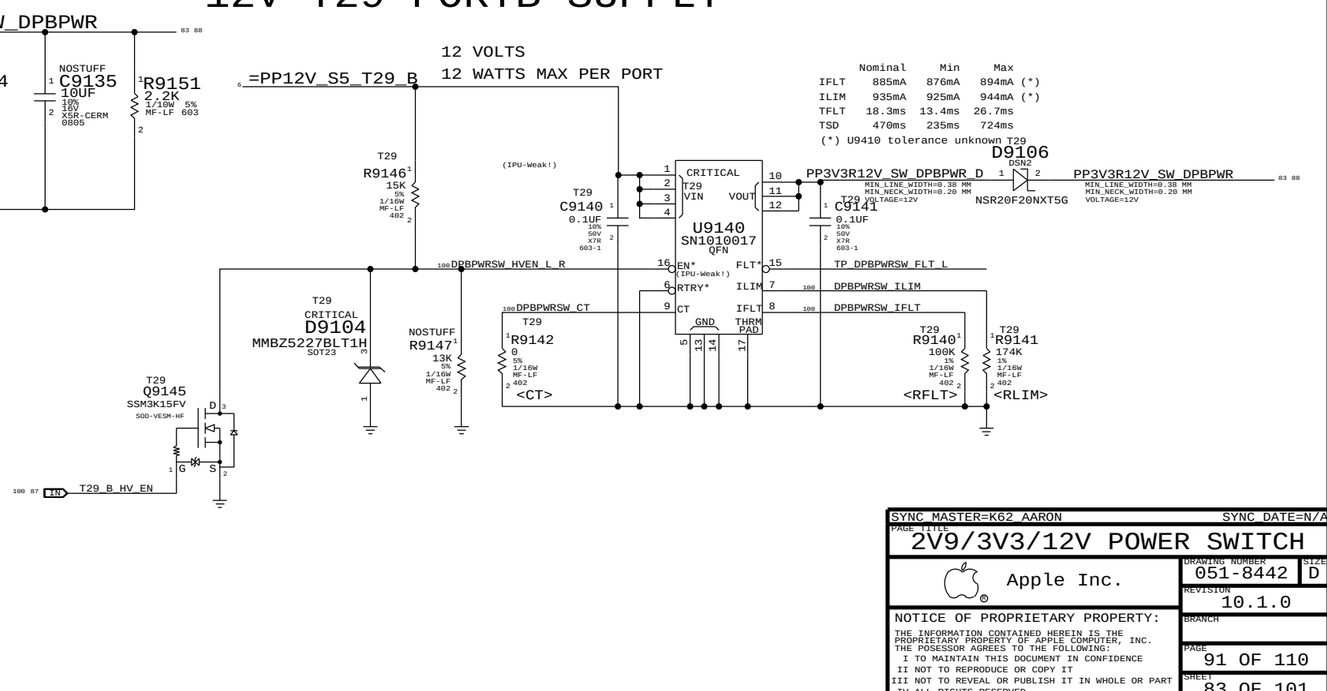
12V T29 PORTA SUPPLY



3V3(DP)/2V9(T29) PORTB SUPPLY



12V T29 PORTB SUPPLY



SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE
2V9/3V3/12V POWER SWITCH

Apple Inc.

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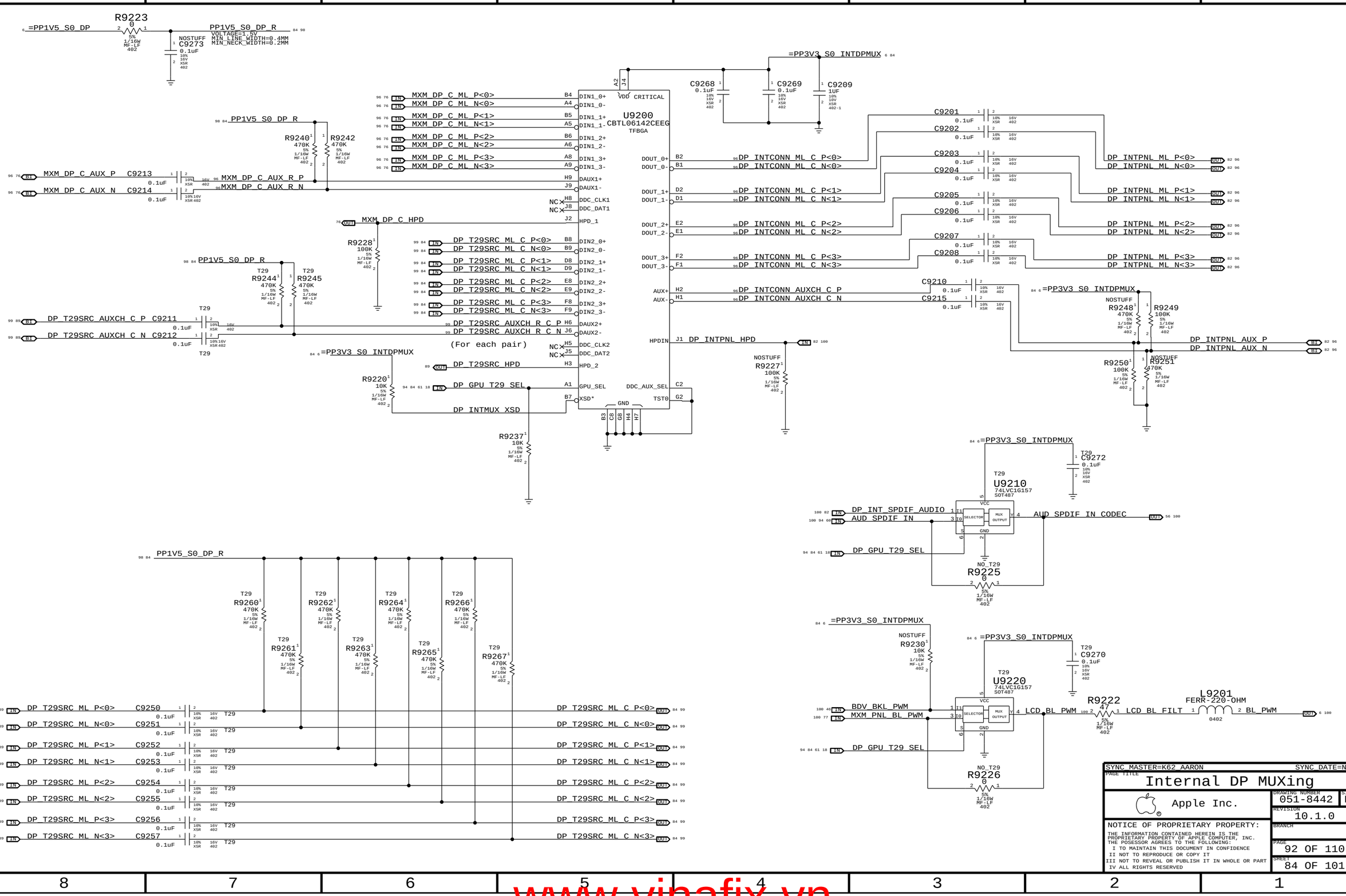

T29 A High-Speed Signals

DP EXTA ML C P<0> C9300 0.1uF → DP EXTA ML P<0>
DP EXTA ML C N<0> C9301 0.1uF → DP EXTA ML N<0>
DP EXTA ML C P<1> C9302 0.1uF → DP EXTA ML P<1>
DP EXTA ML C N<1> C9303 0.1uF → DP EXTA ML N<1>
DP EXTA ML C P<2> C9304 0.1uF → DP EXTA ML P<2>
DP EXTA ML C N<2> C9305 0.1uF → DP EXTA ML N<2>
DP EXTA ML C P<3> C9306 0.1uF → DP EXTA ML P<3>
DP EXTA ML C N<3> C9307 0.1uF → DP EXTA ML N<3>
DP EXTA AUXCH C P C9308 0.1uF → DP EXTA AUXCH P
DP EXTA AUXCH C N C9309 0.1uF → DP EXTA AUXCH N

R9309 1M 5% MF-LF 1/16W 402 =PP3V3_S0_DPSDRVA
R9308 1M 5% MF-LF 1/16W 402

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29 A BIAS R2D P0 VOLTAGE=3.3V
GND_VOID=TRUE (C9370/C9371)
C9370 0.47uF
C9371 0.47uF
T29 D2R N<0> / T29 D2R P<0>

OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9372 1.0NH+/-0.1NH 0201-1
L9373 1.0NH+/-0.1NH 0201-1
T29 R2D C N<0> / T29 R2D C P<0>
T29 R2D C F N<0> / T29 R2D C F P<0>

(C9372.2) GND_VOID=TRUE
C9372 0.47uF
C9373 0.47uF
(C9373.2) GND_VOID=TRUE
R9372 1.5K 5% MF 1/20W 201
R9373 1.5K 5% MF 1/20W 201
GND_VOID=TRUE
SIGNAL_MODEL=EMPTY
T29 R2D P<0> / T29 R2D N<0>

T29 A BIAS R2D N0 VOLTAGE=3.3V

T29 signals are P/N-swapped after AC caps to improve layout.

(All 4 L's)

T29 A BIAS R2D P1 VOLTAGE=3.3V
GND_VOID=TRUE (C9380/C9381)
C9380 0.47uF
C9381 0.47uF
T29 D2R N<1> / T29 D2R P<1>

OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9382 1.0NH+/-0.1NH 0201-1
L9383 1.0NH+/-0.1NH 0201-1
T29 R2D C N<1> / T29 R2D C P<1>
T29 R2D C F N<1> / T29 R2D C F P<1>

(C9383.2) GND_VOID=TRUE
C9382 0.47uF
C9383 0.47uF
(C9383.2) GND_VOID=TRUE
R9382 1.5K 5% MF 1/20W 201
R9383 1.5K 5% MF 1/20W 201
GND_VOID=TRUE
SIGNAL_MODEL=EMPTY
T29 R2D N<1> / T29 R2D N<1>

T29 A BIAS R2D N1 VOLTAGE=3.3V
C9364 0.22uF
C9365 0.22uF
C9360 0.22uF
C9361 0.22uF
DP SDRVA ML R P<0> / DP SDRVA ML R N<0>
DP SDRVA ML R P<2> / DP SDRVA ML R N<2>
DP SDRVA ML P<0> / DP SDRVA ML N<0>
DP SDRVA ML P<2> / DP SDRVA ML N<2>

T29 Path Biasing

D9364 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9364.2)
D9372 BAR90-02LRH TSLP-2-7
D9373 BAR90-02LRH TSLP-2-7
D9365 BAR90-02LRH TSLP-2-7
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY

T29: TX_0
T29DPA ML C P<0> / T29DPA ML C N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K 5% MF 1/20W 201
R9375 1.5K 5% MF 1/20W 201
GND_VOID=TRUE SIGNAL_MODEL=EMPTY

T29 D2R C P<1> / T29 D2R C N<1>

D9360 BAR90-02LRH TSLP-2-7 GND_VOID=TRUE (D9360.2)
D9382 BAR90-02LRH TSLP-2-7
D9383 BAR90-02LRH TSLP-2-7
D9361 BAR90-02LRH TSLP-2-7
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)

T29: TX_1
T29DPA ML C P<2> / T29DPA ML C N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K 5% MF 1/20W 201
R9385 1.5K 5% MF 1/20W 201
GND_VOID=TRUE SIGNAL_MODEL=EMPTY

DP Path Biasing

R9361 1.5K 5% MF 1/20W 201 DP A BIAS N 2 VOLTAGE=3.3V
R9360 1.5K 5% MF 1/20W 201 DP A BIAS P 2 VOLTAGE=3.3V
R9365 1.5K 5% MF 1/20W 201 DP A BIAS N 0 VOLTAGE=3.3V
R9364 1.5K 5% MF 1/20W 201 DP A BIAS P 0 VOLTAGE=3.3V
R9362 51 5% MF 1/20W 201
R9363 51 5% MF 1/20W 201
R9366 51 5% MF 1/20W 201
R9367 51 5% MF 1/20W 201
Both R's:
C9358 0.1uF 10% 16V X5R-CERM 0201

DP A Super-Driver

=PP3V3_S0_DPSDRVA
C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 20% 10V CERM 402
C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NOSTUFF R9311 1K 5% 1/16W MF-LF 402
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP EXTA ML P<0>	1	IN_D0P	OUT_D0P 30 DP SDRVA ML C P<0>
DP EXTA ML N<0>	2	IN_D0N	OUT_D0N 29 DP SDRVA ML C N<0>
DP EXTA ML P<1>	4	IN_D1P	OUT_D1P 28 DP SDRVA ML C P<1>
DP EXTA ML N<1>	5	IN_D1N	OUT_D1N 27 DP SDRVA ML C N<1>
DP EXTA ML P<2>	7	IN_D2P	OUT_D2P 25 DP SDRVA ML C P<2>
DP EXTA ML N<2>	8	IN_D2N	OUT_D2N 24 DP SDRVA ML C N<2>
DP EXTA ML P<3>	9	IN_D3P	OUT_D3P 23 DP SDRVA ML C P<3>
DP EXTA ML N<3>	10	IN_D3N	OUT_D3N 22 DP SDRVA ML C N<3>
DP EXTA DDC CLK	14	IN_SCL	AC_AUXP 20 DP SDRVA AUXCH C P
DP EXTA DDC DATA	13	IN_SDA	AC_AUXN 19 DP SDRVA AUXCH C N
DP EXTA AUXCH P	16	IN_AUXP	OUT_AUXP_SCL 18 (DP_SDRVA_AUXCH_P)
DP EXTA AUXCH N	15	IN_AUXN	OUT_AUXN_SDA 17 (DP_SDRVA_AUXCH_N)
DP EXTA HPD	3	IN_HPD	(IPD) OUT_HPD 31 (DP_SDRVA_HPD)
DPSDRVA I2C CTL EN	26	I2C_CTL_EN (IPU)	CA_DET 32 DP A CA DET
DPSDRVA I2C ADDR0	36	I2C_ADDR0 (IPD)	
DPSDRVA I2C ADDR1	35	I2C_ADDR1 (IPD)	CEXT 11 DPSDRVA CEXT
=I2C DPSDRVA SCL	38	SCL_CTL	
=I2C DPSDRVA SDA	37	SDA_CTL	
DPSDRVA REXT	12	REXT	
DP AUXCH ISOL	39	AUXDDC_OFF (IPD)	
DP A PWRDWN R	34	PD (IPD)	
	6	GND	
	33	THMPAD	
	41		

PLACE_NEAR=U9310.11:2 mm
C9319 2.2UF 20% 6.3V CERM 402-LF

SDRV_PD R9318 0 5% 1/16W MF-LF 402
R9319 4.02K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9370 390 5% 1/20W MF 201
R9371 390 5% 1/20W MF 201
R9352 390 5% 1/20W MF 201
R9353 390 5% 1/20W MF 201
R9354 22 5% 1/20W MF 201 DP SDRVA ML R P<0>
R9355 22 5% 1/20W MF 201 DP SDRVA ML R N<0>
R9350 22 5% 1/20W MF 201 DP SDRVA ML R P<2>
R9351 22 5% 1/20W MF 201 DP SDRVA ML R N<2>

C9363 0.1UF 10% 16V X5R-CERM 0201
C9362 0.1UF 10% 16V X5R-CERM 0201
C9367 0.1UF 10% 16V X5R-CERM 0201
C9366 0.1UF 10% 16V X5R-CERM 0201
C9369 0.1UF 10% 16V X5R 402
C9368 0.1UF 10% 16V X5R 402

AUXCH Snoop Port, used by PS8301 during training.

=PP3V3_S0_DPSDRVA
C9359 0.1UF 10% 16V X5R 402
CRITICAL U9359 74LVC1G04DBDCK SC70
DP A PWRDWN → DP A BIAS
IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR Must be 3.3V DP A port power
C9390 0.1UF 10% 16V X5R-CERM 0201
C9391 0.1UF 10% 16V X5R-CERM 0201
R9399 100K 5% 1/16W MF-LF 402

U9390 CBTL04DP081 HVQFN CRITICAL

DP SDRVA ML N<3>	31	DIN1_0+	DOUT_0+ 1 T29DPA ML N<3>
DP SDRVA ML P<3>	30	DIN1_0-	DOUT_0- 2 T29DPA ML P<3>
DP SDRVA ML N<1>	27	DIN1_1+	T29: Unused
DP SDRVA ML P<1>	26	DIN1_1-	
DP SDRVA AUXCH P	19	AUX1+	DOUT_1+ 4 T29DPA ML N<1>
DP SDRVA AUXCH N	18	AUX1-	DOUT_1- 5 T29DPA ML P<1>
DP SDRVA HPD	17	HPD_1	T29: LSX_A_R2P/P2R (P/N)
T29 A RSVD N	25	DIN2_0+	AUX+ 6 DP A EXT AUXCH P
T29 A RSVD P	24	DIN2_0-	AUX- 7 DP A EXT AUXCH N
(T29_A_LSX_P2R)	23	DIN2_1+	T29: RX_1 Bias Sink
(T29_A_LSX_R2P)	22	DIN2_1-	
T29_D2R1_BIASP	15	AUX2+	HPD_IN 8 DP A EXT HPD
T29_D2R1_BIASN	14	AUX2-	
NC	13	HPD_2	
DP A PWRDWN	10	GPU_SEL	LO=Port A HI=Port B
T29 A BIAS	32	AUX_SEL	
	11	NC	
	29	VDD	
	20		
	16		
	12		
	9		
	3		
	33	THMPAD	
	28	GND	
	21		

SIGNAL_MODEL=T29DP_MUX

R9392 51 5% 1/16W MF-LF 402
R9393 51 5% 1/16W MF-LF 402
R9396 1K 5% 1/16W MF-LF 402
R9397 1K 5% 1/16W MF-LF 402
R9398 100K 5% 1/16W MF-LF 402

CBTL04DP081 (353S3151) and PI3VEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power
C9330 0.1UF 20% 16V CERM 402
C9331 0.1UF 20% 10V CERM 402
R9338 10K 5% 1/16W MF-LF 402

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP A CA DET	1	RESET#/PIO0_0	R/PIO1_0/AD1 16 T29DPA CONFIG1 RC
	2	PIO0_1/CLKOUT	R/PIO1_1/AD2 17 T29DPA CONFIG2 RC
T29 LSEO<0>	7	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18 T29 A HV EN R
		(IPU)	SWDIO/PIO1_3/AD4 19 T29 A UC ADDR
=I2C T29AMCU SCL	8	PIO0_4/SCL (OD)	PIO1_4/AD5/WAKEUP 20 DP A EXT HPD
=I2C T29AMCU SDA	9	PIO0_5/SDA (OD)	
T29DPA HPD	10	PIO0_6/SCK	PIO1_6/RXD 23 T29 A LSX P2R (P2R = PLUG TO RECEPTACLE)
T29 A BIAS	11	PIO0_7/CTS#	PIO1_7/TXD 24 T29 A LSX R2P (R2P = RECEPTACLE TO PLUG)
T29 LSOE<0>	12	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6 T29 LSEO<1>
T29 LSOE<1>	13	PIO0_9/MOSI/CT16B0_MAT1	
	14	SWCLK/PIO0_10/SCK/CT16B0_MAT2	(OD)
T29 MCU INT L	15	R/PIO0_11/AD0	(OD) XTALIN 4
	3	VSS	
	21	THRM PAD	
	25		

R9335 1K 5% 1/16W MF-LF 402
R9336 10K 5% 1/16W MF-LF 402
R9339 1M 5% 1/16W MF-LF 402
R9334 10K 5% 1/16W MF-LF 402 T29_A_HV_EN

I2C Addr: 0x26/0x27 (Wr/Rd)

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#
=T29_WAKE_L
OMIT R9330 0 5% 1/16W MF-LF 402 SWCLK SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
PAGE TITLE: DisplayPort/T29 A MUXing
Apple Inc.
DRAWING NUMBER: 051-8442 SIZE: D
REVISION: 10.1.0
BRANCH:
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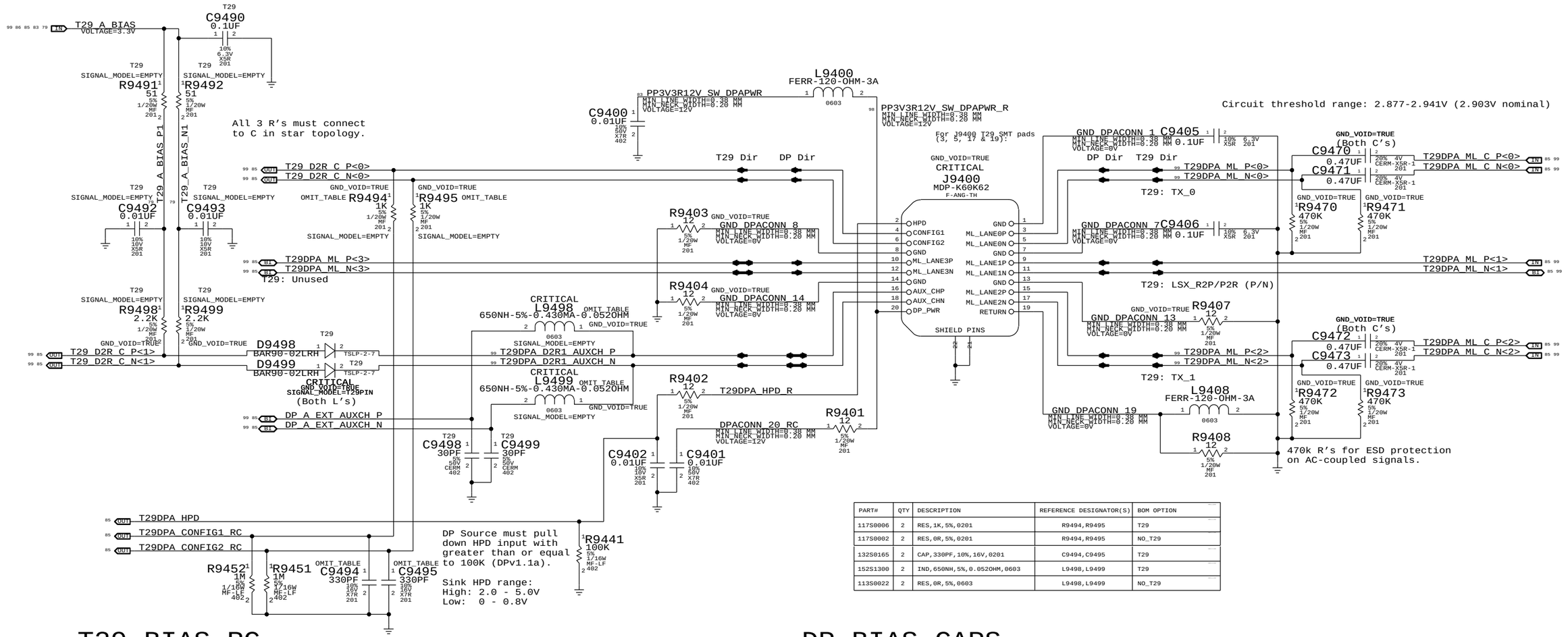
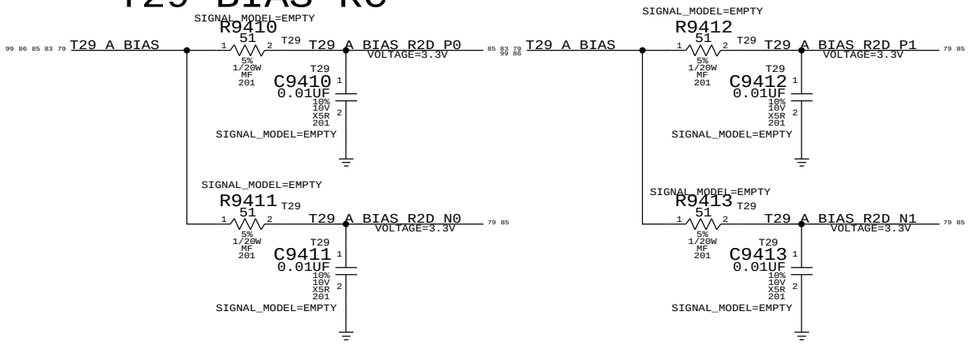
DisplayPort/T29 A Connector

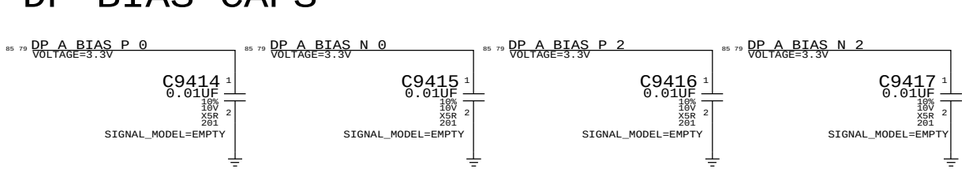


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	2	RES,1K,5%,0201	R9494,R9495	T29
117S0002	2	RES,0R,5%,0201	R9494,R9495	NO_T29
132S0165	2	CAP,330PF,10%,16V,0201	C9494,C9495	T29
152S1300	2	IND,650NH,5%,0.052OHM,0603	L9498,L9499	T29
113S0022	2	RES,0R,5%,0603	L9498,L9499	NO_T29

T29 BIAS RC



DP BIAS CAPS



SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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T29 B High-Speed Signals

T29 signals are P/N-swapped after AC caps to improve layout.

T29 Path Biasing

DP Path Biasing

DP B Super-Driver

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9508/R9509 maintain bias on C9508/C9509 to prevent spikes when U9510 AUXDDC_OFF transitions from high to low.

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

DP/T29 B Low-Speed MUX

IC supports input high while Vcc = 0V.

AUXCH Snoop Port, used by PS8301 during training.

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 11 for HPD.

Note: U9590 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9590 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

Port B MCU

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

R9530 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

P2R = Plug to Receptacle
R2P = Receptacle to Plug

SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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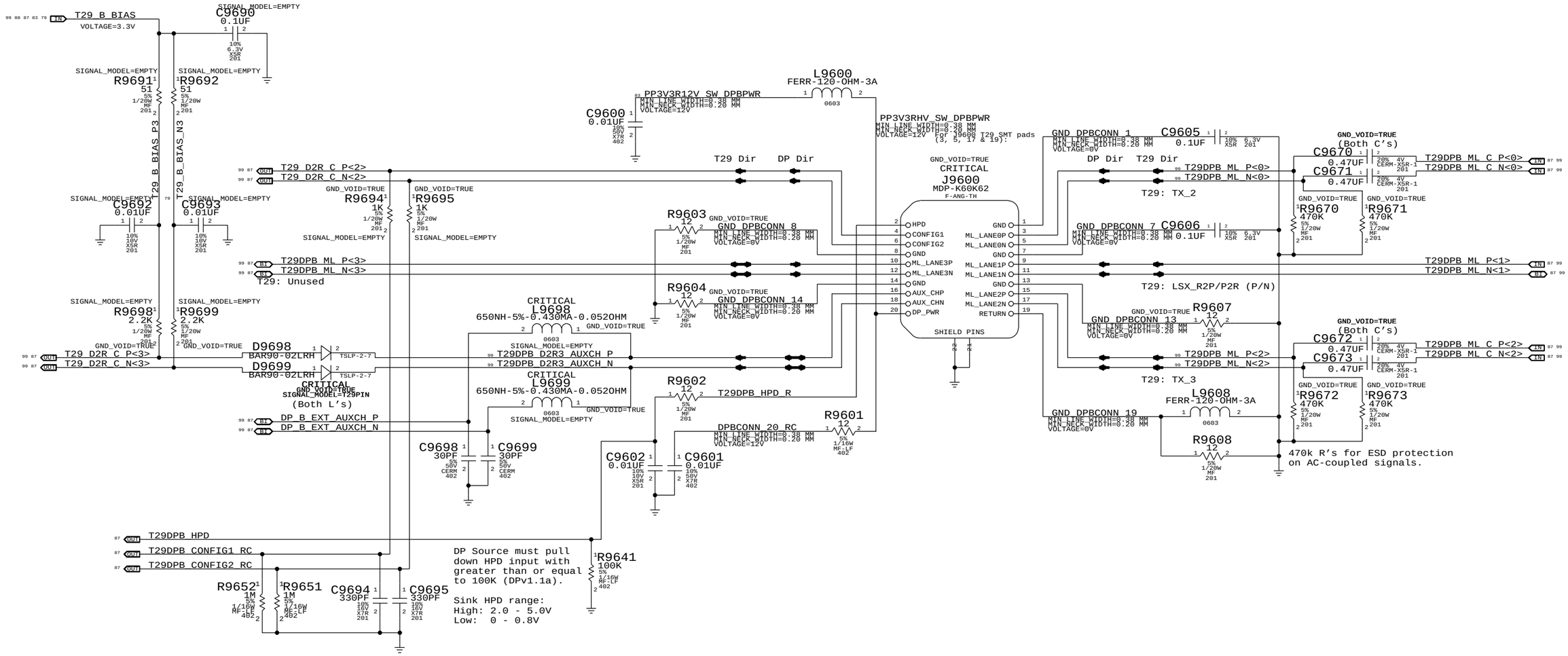
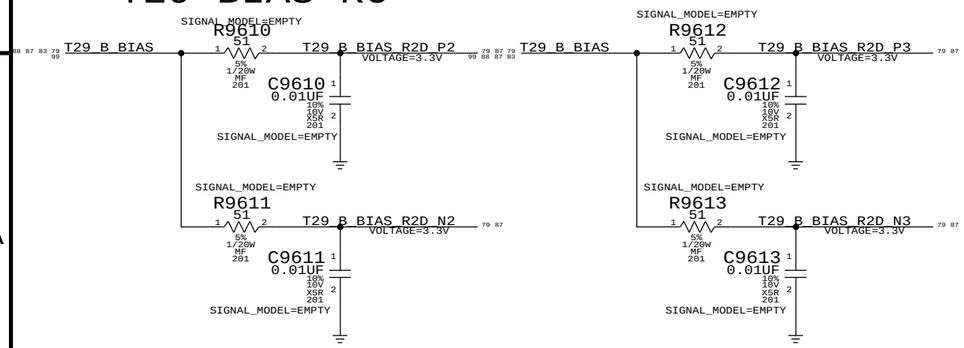
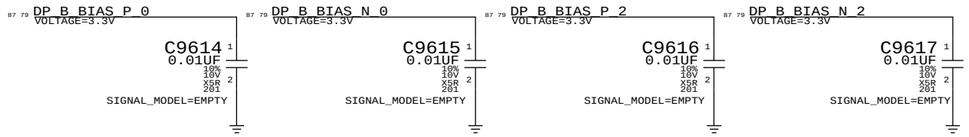
DisplayPort/T29 B Connector



T29 BIAS RC



DP BIAS CAPS



SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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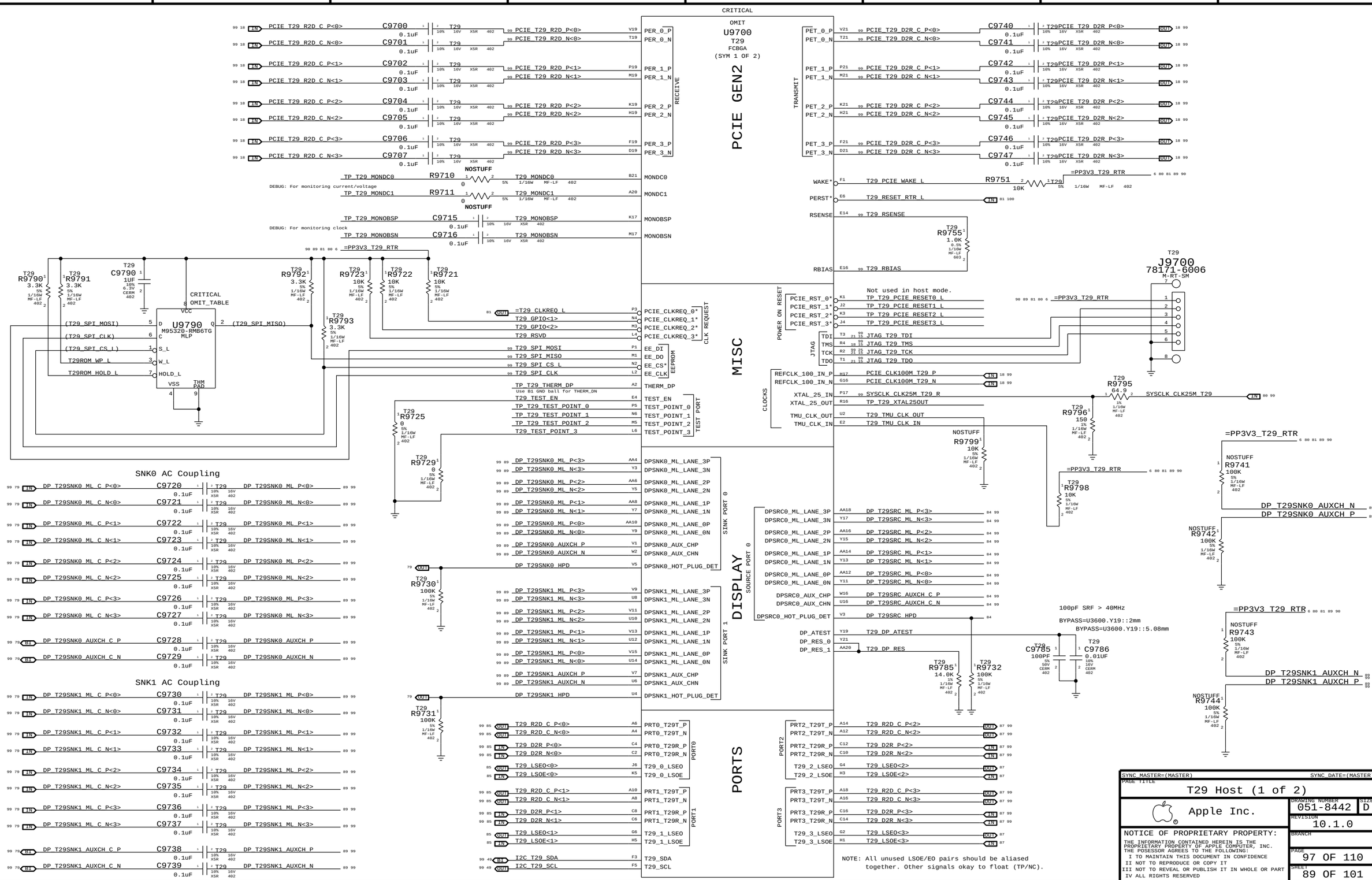

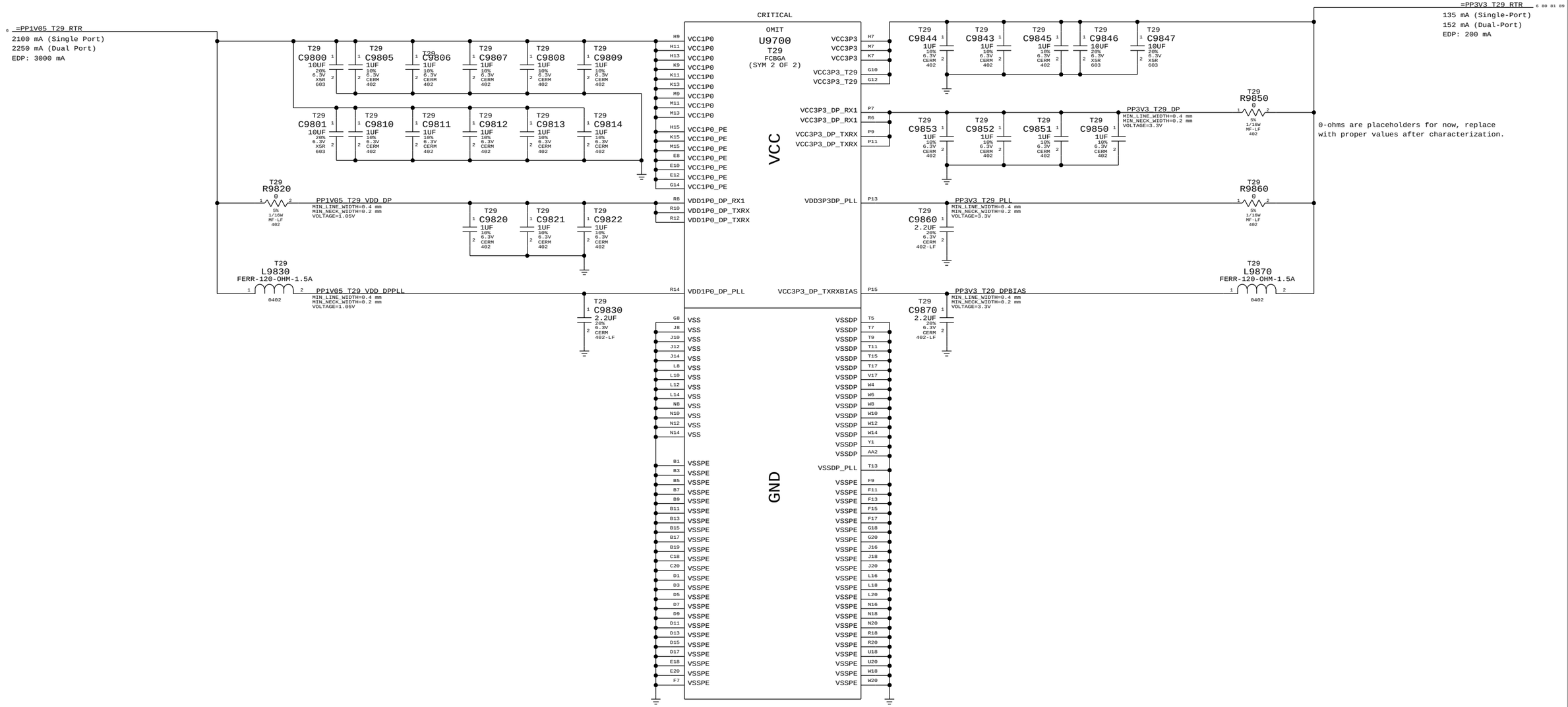

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

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K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.090 MM	=STANDARD		
34_OHM_SE	*	Y	0.19 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.090 MM	=STANDARD		
39_OHM_SE	*	Y	0.159 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.090 MM	=STANDARD		
42_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
68_OHM_DIFF	ISL3,ISL6	Y	0.16 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.2 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.081 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
3.5:1_SPACING	*	0.35 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.155 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.145 MM	?
3X_DIELECTRIC	*	0.230 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.215 MM	?
4X_DIELECTRIC	*	0.305 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.285 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.355 MM	?
7X_DIELECTRIC	*	0.532 MM	?
7X_DIELECTRIC	TOP,BOTTOM	0.497 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P1P5MM	*	0.15 MM	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P1P5MM
CLK_PCIE	*	BGA	BGA_P1MM
CLK_LPC	*	BGA	BGA_P1MM
CLK_PCI	*	BGA	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CONTROL	*	*	SWITCHNODE
VR_CONTROL	VR_CONTROL	*	STANDARD
VR_CONTROL	SWITCHNODE	*	STANDARD
VR_CONTROL	GND	*	STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

BOARD STACK-UP

TOP	HALF OZ	SIGNAL
	0.071	PREPREG
2	TWO OZ	GND
	0.076	PREPREG
3	ONE OZ	SIGNAL
	0.370	PREPREG
4	TWO OZ	POWER
	0.101	CORE
5	TWO OZ	POWER
	0.370	PREPREG
6	ONE OZ	SIGNAL
	0.076	PREPREG
7	TWO OZ	GND
	0.071	PREPREG
BOTTOM	HALF OZ	SIGNAL

BOARD THICKNESS = 62 MIL (1.5748 mm)

SYNC_MASTER=K62_AARON SYNC_DATE=06/08/2010

PAGE TITLE: K60/K62 RULE DEFINITIONS

Apple Inc.

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MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
MEM_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
MEM_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=5:1_SPACING	?
MEM_CTRL2CTRL	*	=2.5:1_SPACING	?
MEM_CTRL2MEM	*	=3.5:1_SPACING	?
MEM_CMD2CMD	*	=2:1_SPACING	?
MEM_CMD2MEM	*	=3.5:1_SPACING	?
MEM_DQ_SAMEBYTE	*	=3:1_SPACING	?
MEM_DQ_DIFFBYTE	*	=5:1_SPACING	?
MEM_DATA2MEM	*	=4:1_SPACING	?
MEM_DQS2MEM	*	=4:1_SPACING	?
MEM_2OTHER	*	=5:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE0	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE1	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE2	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE3	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE4	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE5	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE6	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE7	*	MEM_DQS2MEM
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE5	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_DQ_BYTE5	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE6	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_DQ_BYTE6	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE6	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE6	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE7	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_DQ_BYTE7	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE0	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_DQ_BYTE0	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE1	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE1	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_DQ_BYTE1	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE2	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_DQ_BYTE2	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE3	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_DQ_BYTE3	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE4	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_DQ_BYTE4	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_68D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_42S	MEM_DQ_BYTE0	MEM_A_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_A_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_A_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_A_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_A_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_A_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_A_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_A_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<7>	12 32
H17A	MEM_50S	PM	MEM_RESET_L	30 31 32 100

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_68D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_42S	MEM_DQ_BYTE0	MEM_B_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_B_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_B_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_B_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_B_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_B_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_B_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_B_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<7>	12 32

MEMORY MISC PROPERTIES

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING	VOLTAGE		
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A	
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B	
H16C	MEM_POWER_PHY	MEM_POWER		CPU_DDR_VREF	11 28
H16D	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DACOUT	28
H16E	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_OPFB	28
H17C	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DQ	28
H17A	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A_SW	
H17J	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DACOUT	28
H17K	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_OPFB	28
H17P	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DQ	28
H17N	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B_SW	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	=3:1_SPACING	?

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4:1_SPACING	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=6:1_SPACING	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SATA				
H50	SATA_90D	SATA	SATA_SSD_R2D_C_P	18 42
H49	SATA_90D	SATA	SATA_SSD_R2D_C_N	18 42
H51	SATA_90D	SATA	SATA_SSD_R2D_P	42
H52	SATA_90D	SATA	SATA_SSD_R2D_N	42
H53	SATA_90D	SATA	SATA_SSD_D2R_P	18 42
H54	SATA_90D	SATA	SATA_SSD_D2R_N	18 42
H55	SATA_90D	SATA	SATA_SSD_D2R_C_P	42
H56	SATA_90D	SATA	SATA_SSD_D2R_C_N	42
PCIE				
H31	PCIE_85D	PCIE	PCIE_USB3_1_R2D_P	
H30	PCIE_85D	PCIE	PCIE_USB3_1_R2D_N	
H29	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_P	
H28	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_N	
H27	PCIE_85D	PCIE	PCIE_USB3_1_D2R_P	
H26	PCIE_85D	PCIE	PCIE_USB3_1_D2R_N	
H25	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_P	
H24	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_N	
H32	PCIE_85D	PCIE	PCIE_USB3_2_R2D_P	
H33	PCIE_85D	PCIE	PCIE_USB3_2_R2D_N	
H34	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_P	
H35	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_N	
H36	PCIE_85D	PCIE	PCIE_USB3_2_D2R_P	
H37	PCIE_85D	PCIE	PCIE_USB3_2_D2R_N	
H38	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_P	
H39	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_N	
CPU ITP				
H45	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	11 25
H46	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 15 25
H44	CPU_50S	CPU_ITP	XDP_OBSDATA_B<3..0>	25
H43	CPU_50S	CPU_ITP	XDP_CPU_CFG<0>	25
H48	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 25
H47	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 25
H49	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 25
H50	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 25
H51	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 25
CPU_MISC				
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_COMP	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCIE GRAPHICS				
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	9 78
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	9 78
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	9 78
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	9 78
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<7..0>	76 78
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<7..0>	76 78
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<7..0>	76 78
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<7..0>	76 78
PCIE I/O				
	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
H115	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_N	
H116	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_P	
H118	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
H117	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	10 19
PCIE REF CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_P	9
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_N	9
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	18 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	18 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	18 37
SATA				
	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_HDD_R2D_P	42
	SATA_90D	SATA	SATA_HDD_R2D_N	42
	SATA_90D	SATA	SATA_HDD_D2R_P	18 42
	SATA_90D	SATA	SATA_HDD_D2R_N	18 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	42
	SATA_90D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_ODD_R2D_P	42
	SATA_90D	SATA	SATA_ODD_R2D_N	42
	SATA_90D	SATA	SATA_ODD_D2R_P	18 42
	SATA_90D	SATA	SATA_ODD_D2R_N	18 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	18 26
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 18
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 18
H137	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	25
H138	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	25
UNUSED CLOCKS				
H135	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_N	26
H136	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_P	26
UNUSED PCIE				
H139	PCIE_85D	PCIE	MXM_PCIE_R2D_P<8..15>	76 78
H140	PCIE_85D	PCIE	MXM_PCIE_R2D_N<8..15>	76 78
H142	PCIE_85D	PCIE	MXM_PCIE_D2R_P<8..15>	76 78
H141	PCIE_85D	PCIE	MXM_PCIE_D2R_N<8..15>	76 78

SYNC_MASTER=K62_ROSITA SYNC_DATE=01/09/2011

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PCIE/DMI/FDI/SATA CONSTRAINTS

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	0.2 MM	?
ITP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

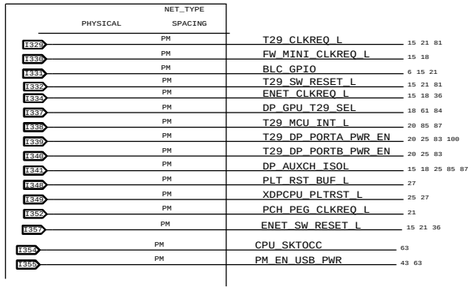
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

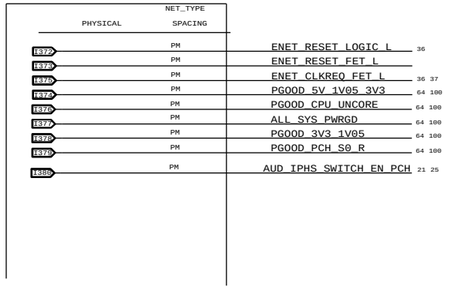
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

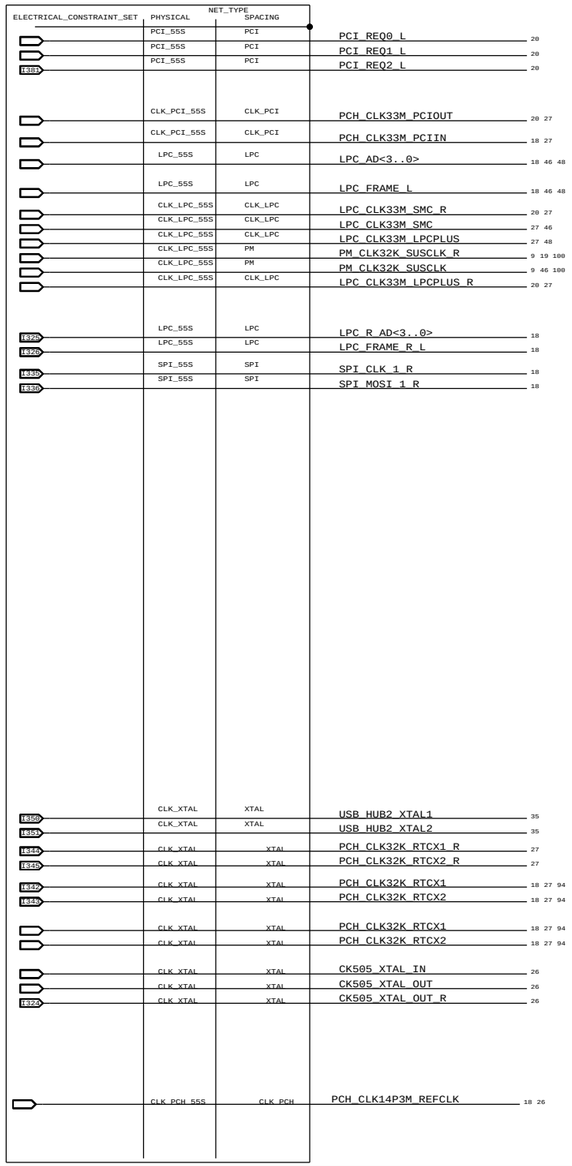
XTAL Constraints

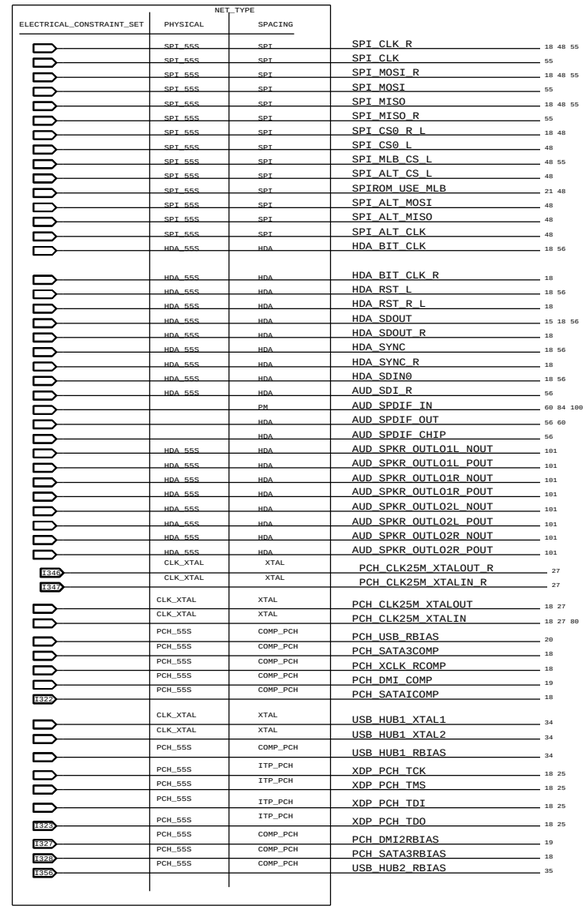
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?









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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_2OTHER	*	=50MIL_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50MIL_SPACING	*	1.27 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_DIFF_T	*	*	ENET_2OTHER

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	ENET_50S	ENET_SE	ENET_RDAC 37
	CLK_PCH_55S	XTAL	ENET_CLK25M_XTALI 36 37
	CLK_PCH_55S	XTAL	ENET_CLK25M_XTALO 36 37
	CLK_PCH_55S	XTAL	ENET_CLK25M_XTALO_R 36
	ENET_100D	ENET_DIFF	ENETCONN_MDI_P<3..0> 37 38
	ENET_100D	ENET_DIFF	ENETCONN_MDI_N<3..0> 37 38
	ENET_100D	ENET_DIFF_T	ENETCONN_MDI_T_P<3..0> 38
	ENET_100D	ENET_DIFF_T	ENETCONN_MDI_T_N<3..0> 38
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_P 37
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_N 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_P 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_N 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_C_P 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_R2D_C_N 18 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_C_P 37
	PCIE_85D	ENET_MII	PCIE_ENET_D2R_C_N 37
	SD_50S	SD	ENET_SD_CMD 37
	SD_50S	SD	SDCONN_CMD 37 45
	SD_50S	SD	SDCONN_CLK 37 45
	SD_50S	SD	ENET_SD_CLK 37
	SD_50S	SD	SDCONN_DATA<7..0> 37 45
	SD_50S	SD	ENET_CR_DATA<7..0> 37
	SD_50S	PM	ENET_MEDIA_SENSE 15 18 37
	SD_50S	SD	ENET_MEDIA_SENSE_R
	SD_50S	SD	ENET_SD_DETECT_L 37
	SD_50S	PM	SDCONN_DETECT_BUF_L 100

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	USB_90D	USB	USB_EXTA_P 34 43
	USB_90D	USB	USB_EXTA_N 34 43
	USB_90D	USB	USB_PORT0_P 43
	USB_90D	USB	USB_PORT0_N 43
	USB_90D	USB	USB_EXTB_P 35 43
	USB_90D	USB	USB_EXTB_N 35 43
	USB_90D	USB	USB_PORT1_P 43
	USB_90D	USB	USB_PORT1_N 43
	USB_90D	USB	USB_EXTC_P 34 43
	USB_90D	USB	USB_EXTC_N 34 43
	USB_90D	USB	USB_PORT2_P 43
	USB_90D	USB	USB_PORT2_N 43
	USB_90D	USB	USB_EXTD_P 35 43
	USB_90D	USB	USB_EXTD_N 35 43
	USB_90D	USB	USB_D_MUXED_P 43
	USB_90D	USB	USB_D_MUXED_N 43
	USB_90D	USB	USB_PORT3_P 43
	USB_90D	USB	USB_PORT3_N 43
	USB_90D	USB	USB_CAMERA_P 20 44
	USB_90D	USB	USB_CAMERA_N 20 44
	USB_90D	USB	USB_CAMERA_L_P 44 101
	USB_90D	USB	USB_CAMERA_L_N 44 101
	USB_90D	USB	USB_BT_P 35 44
	USB_90D	USB	USB_BT_N 35 44
	USB_90D	USB	USB_BT_L_P 44 101
	USB_90D	USB	USB_BT_L_N 44 101
	USB_90D	USB	USB_IR_P 34 44
	USB_90D	USB	USB_IR_N 34 44
	USB_90D	USB	USB_IR_L_P 44 101
	USB_90D	USB	USB_IR_L_N 44 101
	USB_90D	USB	USB_SDCARD_P 34 44
	USB_90D	USB	USB_SDCARD_N 34 44
	USB_90D	USB	USB_SDCARD_L_P 44
	USB_90D	USB	USB_SDCARD_L_N 44
	USB_90D	USB	USB_HUB1_UP_P 20 34
	USB_90D	USB	USB_HUB1_UP_N 20 34
	USB_90D	USB	USB_HUB2_UP_P 20 35
	USB_90D	USB	USB_HUB2_UP_N 20 35
	USB_90D	USB	USB_HUB2UNUSED_P 35
	USB_90D	USB	USB_HUB2UNUSED_N 35

FireWire Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
P25	CLK_PCH_55S	XTAL	FW_CLK24P576M_XO 39
P24	CLK_PCH_55S	XTAL	FW_CLK24P576M_XO_R 39
P26	CLK_PCH_55S	XTAL	FW_CLK24P576M_XI 39
	FW_110D	FW_TP	FW_PORT0_TPA_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPA_N 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_N 40 41
UNUSED FW NETS PHYSICAL PROPERTIES			
P23	FW_110D	FW_TP	FW_P1_TPA_P 39 40
P25	FW_110D	FW_TP	FW_P1_TPA_N 39 40
P24	FW_110D	FW_TP	FW_P2_TPA_P 39 40
P26	FW_110D	FW_TP	FW_P2_TPA_N 39 40
	FW_110D	FW_TP	FW_P1_TPB_P 39 40
	FW_110D	FW_TP	FW_P1_TPB_N 39 40
	FW_110D	FW_TP	FW_P2_TPB_P 39 40
	FW_110D	FW_TP	FW_P2_TPB_N 39 40

SYNC_MASTER=K62_MARK SYNC_DATE=01/09/2011

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USB/ENET/SD/FW/AUD CONSTRAINTS

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GRAPHICS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET
ASSINGED IN CONT. MGR.

NET_TYPE	PHYSICAL	SPACING		
T160	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_P<3..0>	84
T174	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_N<3..0>	84
	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_P	84
	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_N	84
T153	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	82 84
T154	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	82 84
	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	82 84
	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	82 84
T181	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	85
T180	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	85
T178	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	85
T179	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	85
T172	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	79 85
T173	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	79 85
T177	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	79 85
T175	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	79 85
T191	DP_85D	DISPLAYPORT	DP_EXTB_ML_P<3..0>	87
T192	DP_85D	DISPLAYPORT	DP_EXTB_ML_N<3..0>	87
T193	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_P	87
T194	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_N	87
T195	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_P<3..0>	79 87
T196	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_N<3..0>	79 87
T189	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_P	79 87
T190	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_N	79 87
T199	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0>	76 79
T200	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0>	76 79
T203	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P	76 79
T202	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N	76 79
T205	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	76 84
T206	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	76 84
T209	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P	76 84
T208	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N	76 84
T211	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_P	84
T212	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_N	84
T207	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0>	76 79
T208	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0>	76 79
T209	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P	76 79
T210	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N	76 79

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P	
DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N	
DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P	77 79
DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N	77 79
DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0>	77 79
DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0>	77 79
DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0>	77 79
DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0>	77 79

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GRAPHICS CONSTRAINTS

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	49
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	49
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 97
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 97
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 97
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 97
	SMB_55S	SMB	SMBUS_PCH_CLK	18 49
	SMB_55S	SMB	SMBUS_PCH_DATA	18 49
	SMB_55S	SMB	SML_PCH_0_CLK	18 49
	SMB_55S	SMB	SML_PCH_0_DATA	18 49
	SMB_55S	SMB	SML_PCH_1_CLK	18 49
	SMB_55S	SMB	SML_PCH_1_DATA	18 49
	CLK_XTAL	XTAL	SMC_EXTAL	46 47
	CLK_XTAL	XTAL	SMC_XTAL	46 47
I254	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SCL	28
I253	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SDA	28
I255	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SCL	28
I254	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SDA	28
I265	SMB_55S	SMB	SMB_BLC_TCON_SCL	6 49 82
I264	SMB_55S	SMB	SMB_BLC_TCON_SDA	6 49 82
I268	SMB_55S	SMB	I2C_TCON_SCL	82
I269	SMB_55S	SMB	I2C_TCON_SDA	82
I266	SMB_55S	SMB	SMB_BLC_PCH_SCL_R	6
I267	SMB_55S	SMB	SMB_BLC_PCH_SDA_R	6

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_T1_1_P	52
	THERM_DIFF	THERMAL	SNS_T1_1_N	52
	THERM_DIFF	THERMAL	SNS_T2_DP2	52
	THERM_DIFF	THERMAL	SNS_T2_DN2	52
I209	THERM_DIFF	THERMAL	SNS_T1_2_P	52
I208	THERM_DIFF	THERMAL	SNS_T1_2_N	52
I207	THERM_DIFF	THERMAL	SNS_T1_3_P	52
I206	THERM_DIFF	THERMAL	SNS_T1_3_N	52
I211	THERM_DIFF	THERMAL	SNS_T1_4_P	52
I212	THERM_DIFF	THERMAL	SNS_T1_4_N	52
I213	THERM_DIFF	THERMAL	SNS_T1_5_P	52
I214	THERM_DIFF	THERMAL	SNS_T1_5_N	52
I215	THERM_DIFF	THERMAL	SNS_T1_6_P	52
I216	THERM_DIFF	THERMAL	SNS_T1_6_N	52
I217	THERM_DIFF	THERMAL	SNS_T1_7_P	52
I218	THERM_DIFF	THERMAL	SNS_T1_7_N	52
I224	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 52
I225	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 52
I219	THERM_DIFF	THERMAL	SNS_LCD_H_P	52
I210	THERM_DIFF	THERMAL	SNS_LCD_H_N	52
	THERM_DIFF	THERMAL	SNS_ODD_P	52 101
	THERM_DIFF	THERMAL	SNS_ODD_N	52 101
	THERM_DIFF	THERMAL	SNS_CPU_H_P	52
	THERM_DIFF	THERMAL	SNS_CPU_H_N	52
I222	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_P	52 101
I223	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_N	52 101
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_P	44 52 101
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_N	44 52 101
	THERM_DIFF	THERMAL	SNS_AMB_P	52 101
	THERM_DIFF	THERMAL	SNS_AMB_N	52 101
	THERM_DIFF	THERMAL	SNS_MXM_P	52
	THERM_DIFF	THERMAL	SNS_MXM_N	52
		THERMAL	HDD_OOB_TEMP_FILT	42 51 101
		THERMAL	HDD_OOB_TEMP_FB	42
		THERMAL	HDD_OOB_TEMP_R	51
		THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_I_MXM_P	50
	THERM_DIFF	THERMAL	SNS_I_MXM_N	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_P	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_N	50
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 98
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 98
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 98
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 98
I243	SNS_DIFF	THERMAL	VR_ISNS_1V05_P	98
I244	SNS_DIFF	THERMAL	VR_ISNS_1V05_N	98
I245	THERM_DIFF	THERMAL	SNS_CPU_1V5_P	50
I246	THERM_DIFF	THERMAL	SNS_CPU_1V5_N	50
I247	THERM_DIFF	THERMAL	SNS_VCCSA_P	50
I248	THERM_DIFF	THERMAL	SNS_VCCSA_N	50
I253	THERM_DIFF	THERMAL	SNS_1V05_PCH_P	50
I252	THERM_DIFF	THERMAL	SNS_1V05_PCH_N	50
I230		THERMAL	GND_SMC_AVSS	46 47 50 97
I241		THERMAL	SMC_CPU_1V5_ISENSE	46 50
I240		THERMAL	SMC_CPU_1V5_ISENSE_R	50
I242		THERMAL	SMC_CPU_1V5_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 97
I238		THERMAL	SMC_DIMM_ISENSE	46 50
I228		THERMAL	SMC_DIMM_1V5_R	50
I231		THERMAL	SMC_DIMM_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 97
I227		THERMAL	SMC_VCCSA_ISENSE	46 50
I226		THERMAL	SMC_VCCSA_ISENSE_R	50
I227		THERMAL	SMC_VCCSA_VSENSE	46 50
		THERMAL	GND_SMC_AVSS	46 47 50 97
		THERMAL	SMC_PCH_1V05_ISENSE	46 50
		THERMAL	SMC_VAXG_VSENSE	46 50
		THERMAL	SMC_PCH_1V05_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 97
I233		THERMAL	SMC_1V05_ISENSE	46 50
I232		THERMAL	SMC_VAXG_ISENSE	46 50
I233		THERMAL	SMC_1V05_VSENSE	46 50
I235		THERMAL	SMC_GPU_ISENSE	46 50
		THERMAL	SMC_GPU_VSENSE	46 50
		THERMAL	SMC_VCORE_ISENSE	46 50
I237		THERMAL	SMC_VCORE_VSENSE	46 50
I236		THERMAL	SMC_CPU_VSENSE	

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE	PHYSICAL	SPACING	VOLTAGE	
U12D	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1 66
U12C	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2 66
U13D	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3 66
U12T	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4 67
U12T	POWER	SWITCHNODE	1.5V	VR_AXG_PHASE1 67
U13T	POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE 71
U13S	POWER	SWITCHNODE	5V	P5VS3_REG_PHASE 71
U13C	POWER	SWITCHNODE	1.05V	P1V05S0_PHASE 68
U12C	POWER	SWITCHNODE	1.05V	P1V05_REG_PHASE
U12T	POWER	SWITCHNODE	3.4V	P3V42G3H_SW 73
U13D	POWER	SWITCHNODE	3.3V	ENET_3V3_S3_SR_IN 37
U13T	POWER	SWITCHNODE	1.2V	ENET_SR_LX 36 37
U13D	POWER	SWITCHNODE	1.5V	DDR_REG_PHASE 72
U14D	POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE 72
T16J	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_A 28 30
T14J	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_B 28 31
T14J	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_A 28 30
T16J	POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_B 28 31
T14D	POWER	POWER	12V	PP12V_S0 6
T14D	POWER	POWER	12V	PP12V_S0_CPU_FLTRD 65 66 67
T17C	POWER	POWER	12V	PP12V_S0_FAN0_L 53 101
T17C	POWER	POWER	12V	PP12V_S0_FAN1_L 53 101
T17C	POWER	POWER	12V	PP12V_S0_FAN2_L 54 101
T07J	POWER	POWER	12V	VR_CPU_DRV1_PVCC 66
T07J	POWER	POWER	12V	VR_CPU_DRV1_UVCC 66
T07J	POWER	POWER	12V	VR_CPU_DRV2_PVCC 66
T07C	POWER	POWER	12V	VR_CPU_DRV2_UVCC 66
T07C	POWER	POWER	12V	VR_CPU_DRV3_PVCC 66
T07C	POWER	POWER	12V	VR_CPU_DRV3_UVCC 66
T07J	POWER	POWER	12V	VR_CPU_DRV4_PVCC 67
T07J	POWER	POWER	12V	VR_CPU_DRV4_UVCC 67
T07C	POWER	POWER	12V	VR_AXG_DRV1_PVCC 67
T07J	POWER	POWER	12V	VR_AXG_DRV1_UVCC
T09J	POWER	POWER	12V	VR_CPU_DRV1_VCC 66
T08J	POWER	POWER	12V	VR_CPU_DRV2_VCC 66
T08D	POWER	POWER	12V	VR_CPU_DRV3_VCC 66
T07D	POWER	POWER	12V	VR_CPU_DRV4_VCC 67
T16S	POWER	POWER	12V	PP12V_S0_VG_OK 41
T16S	POWER	POWER	12V	P12V_FW_R 41
T16S	POWER	POWER	12V	P12V_FW_CL 41
T16S	POWER	POWER	12V	P12V_FW_D 41
T26S	POWER	POWER	12V	FW_PORT0_VP 41
T27S	POWER	POWER	12V	FW_PORT0_VP_F 41
T16S	POWER	POWER	12V	PPVP_FW_PHY_CPS 39 41
T08D	POWER	POWER	12V	PP12V_S0_P1V05_VREG_VIN 68
T16D	POWER	POWER	12V	VCCSA_PWR_RC 69
T77S	POWER	POWER	12V	PP12V_S0_BL_R
T77S	POWER	POWER	12V	PP12V_S5_FET 6 75
T07S	POWER	POWER	12V	PP12V_LCD 82
T06J	POWER	POWER	12V	PP12V_G3H 6
T17S	POWER	POWER	12V	PP12V_S5 6
T13S	POWER	POWER	12V	PP12V_S5_RSN 75
T26D	POWER	POWER	0.75V	PPVTT_S0_DDR 6
U61S	POWER	POWER	0.75V	PP0V75_S0 6
T70J	POWER	POWER	0.925V	PPVCCSA_S0_CPU 6
T65J	POWER	POWER	1.0V	PP1V0_FW_FWPHY_AVDD 39
T65J	POWER	POWER	1.0V	PP1V0_S0_FW_VDD 40
U82S	POWER	POWER	1.05V	PP1V05_S0_T29 6
T47S	POWER	POWER	1.05V	PP1V05_S0_INPUT_VCCSA 6
T13J	POWER	POWER	1.05V	PPVAXG_S0 6
T13J	POWER	POWER	1.05V	PP1V05_S0 6
T13C	POWER	POWER	1.05V	PP1V05_S0_PCH 6
T47S	POWER	POWER	1.05V	PP1V05_S0_CK505_F 26
T47S	POWER	POWER	1.05V	PPVOUT_S5_PCH_DCPSUS 22
T13D	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F 17 22
T13D	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F 17 22
T13D	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP_F 22 24
T13J	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLLDMI2_F 22 24
T13D	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA_F 22 24
T13S	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCCLKDMI_F 22 24
T75S	POWER	POWER	1.1V	PPVCORE_S0_AXG_REG1 67
T75J	POWER	POWER	1.1V	PPVCORE_S0_AXG_REGOUT 67
T25S	POWER	POWER	1.1V	PPVCORE_S0_CPU 6
T25S	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1 66
T25S	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2 66
T56S	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3 66
T78S	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4 67
T69S	VR_CTL_PHY	VR_CTL	1.2V	PP1V2_S3_ENET_INTREG 36
T66D	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_AVDDL 37
T66S	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_PCIEPLL 37
T66S	POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_GPHYPLL 37
T49J	POWER	POWER	1.5V	PP1V5_S0 6
T47C	POWER	POWER	1.5V	PP1V5_S0_CK505_F 26
T68J	POWER	POWER	1.5V	PP1V5_S0_CK505_R 26
T57S	POWER	POWER	1.5V	PP1V5_S0_CPU_MEM 6
T47S	POWER	POWER	1.5V	PP1V5_S0_CPU_SNS
T21J	POWER	POWER	1.5V	PP1V5_S3 6
T78S	POWER	POWER	1.5V	PP1V5_S3_MEM 6

POWER NET PROPERTIES

NET_TYPE	PHYSICAL	SPACING	VOLTAGE	
T45D	POWER	POWER	12V	PP12V_S0_MXM 6
T47D	POWER	POWER	12V	PP12V_SLG1 75
T48D	POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_1
T48D	POWER	POWER	12V	PP3V3R12V_SW_DPBPWR_1
T77J	POWER	POWER	1.8V	USB_HUB2_VDD1V8 35
T78D	POWER	POWER	1.8V	USB_HUB2_VDD1V8PLL 35
T74J	POWER	POWER	1.8V	PP1V8_S0 6
T74J	POWER	POWER	1.8V	PP1V8R1V5_S0_PCH_VCCVRM_F 22 24
T75D	POWER	POWER	1.8V	USB_HUB1_VDD1V8 34
T75D	POWER	POWER	1.8V	USB_HUB1_VDD1V8PLL 34
T82S	POWER	POWER	1.8V	PP3V3R1V8_ENET_LR_OUT_REG 37
T78J	POWER	POWER	3.3V	PPVBAT_G3_SYSCLK_R 80
T66D	POWER	POWER	3.3V	USB_HUB1_VDDPLL3V3 34
T66D	POWER	POWER	3.3V	USB_HUB1_VDDA3V3 34
T79D	POWER	POWER	3.3V	USB_HUB2_VDDPLL3V3 35
T79D	POWER	POWER	3.3V	USB_HUB2_VDDA3V3 35
T21D	POWER	POWER	3.3V	PP3V3R1V5_PCH_VCCSUSHDA 22 24
T21D	POWER	POWER	3.3V	PP3V3_S0_CK505_F 26
T22J	POWER	POWER	3.3V	PP3V3_S0_HS_F 62
T65D	POWER	POWER	3.3V	PP3V3_S0_SW_SD_PWR 45
T22D	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F 17 22
T83D	POWER	POWER	3.3V	PP3V3_S0 6
T82D	POWER	POWER	3.3V	PP3V3_SMCUSBMUX 43
T22J	POWER	POWER	3.3V	PP3V3_S3 6 101
T66S	POWER	POWER	3.3V	PP3V3_S3_BT_FLT 44
T57S	POWER	POWER	3.3V	PP3V3_S3_MINI_CONN 33
T82C	POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT 44
T74D	POWER	SWITCHNODE	3.3V	PP3V3_S3_ENET_PHY_FET 36
T66S	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_XTALVDDH 37
T66S	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_BIASVDDH 37
T66S	POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_AVDDH 37
T74J	POWER	POWER	3.3V	ENET_XTALVDDH 37
T23S	POWER	POWER	3.3V	PP3V3_S5 6
T74S	POWER	POWER	3.3V	PP3V3_S5_REG_R 71
T82J	POWER	POWER	3.3V	PPVBATT_G3_RTC 27
T47C	POWER	POWER	3.3V	PPVBATT_G3_RTC_R 27
T42D	POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK 60 101
T42D	POWER	POWER	3.3V	PP3V3_FW_FWPHY_VDDA 39
T42D	POWER	POWER	3.3V	PP3V3_FW_FWPHY_VP25 39
T83J	POWER	POWER	3.3V	PP3V3_S0_T29 6
T81D	POWER	POWER	3.3V	PP3V3_SW_DPAPWR 79 85
T81D	POWER	POWER	3.3V	PP3V3_SW_DPBPWR 79 87
T82J	POWER	POWER	3.3V	PP3V3_G3H_RTC 18 19 22 27
T23J	POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC 46 47
T23D	POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC 46
T49D	POWER	POWER	3.42V	PP3V42_G3H 6
T47J	POWER	POWER	4.5V	4V5_REG_IN 56
T28S	POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG 56 58 59 61
T47J	POWER	POWER	4.5V	PP5V_AUDIO_HPAMP 56
T49D	POWER	POWER	5V	PP5V_LAMP_VREG 59
T49J	POWER	POWER	5V	PP5V_RAMP_VREG 58
T28J	POWER	POWER	5V	PP5V_S0 6 101
T28D	POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC 65
T43D	POWER	POWER	5V	PP5V_S0_PCH_V5REF 24
T49D	POWER	POWER	5V	PP5V_S0_SATA_FET 42
T49D	POWER	POWER	5V	5V_S0_P1V05REG_VIN 68
T47S	POWER	POWER	5V	5V_S0_P1V05REG_VDD 68
T82J	POWER	POWER	5V	PP5V_S3 6 101
T82J	POWER	POWER	5V	PP5V_S3_VREFMRGN_A 28
T25D	POWER	POWER	5V	PP5V_S3_VREFMRGN_B 28
T42J	POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT 72
T42D	POWER	POWER	5V	PP5V_S3_CAMERA_FLT 44
T42S	POWER	POWER	5V	PP5V_S3_REG_R 71
T76D	POWER	POWER	5V	PP5V_S3_IR_FLT 44 101
T24D	POWER	POWER	5V	PP5V_S5 6
T24J	POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS 24
T25J	POWER	POWER	5V	PP5V_USB_PORT0 43
T25D	POWER	POWER	5V	PP5V_USB_PORT0_F 43
T24S	POWER	POWER	5V	PP5V_USB_PORT1 43
T24S	POWER	POWER	5V	PP5V_USB_PORT1_F 43
T24S	POWER	POWER	5V	PP5V_USB_PORT2 43
T28J	POWER	POWER	5V	PP5V_USB_PORT2_F 43
T28J	POWER	POWER	5V	PP5V_USB_PORT3 43
T25S	POWER	POWER	5V	PP5V_USB_PORT3_F 43
T42S	POWER	POWER		DDR_REG_PGND 72
T84D	POWER	POWER		DDR_REG_CSGND 72
T83J		POWER	3.3V	PPVDDIO_25M_B 80
T83J		POWER	1.05V	PPVDDIO_25M_A 80
T83D		POWER	3.3V	PPVDDIO_25M_C 80
T83S		POWER	12V	PP3V3R12V_SW_DPAPWR_R 86
T83J		POWER	12V	PP3V3R12V_SW_DPAPWR_D 83
T83J		POWER	1.5V	PP1V5_S0_DP_R 84
T84D	POWER	POWER	5V	PP5V_S0_SATA_PORTA1 42
T84S	POWER	POWER	5V	PP5V_S0_SATA_PORTA2 42

SENSING NET PROPERTIES

NET_TYPE	PHYSICAL	SPACING	
T85S	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P 65 66
T85S	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N 65 66
T85S	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N 65
T85D	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P 65 66
T85D	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N 65 66
T85D	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N 65
T85D	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P 65 66
T85S	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N 65 66
T85S	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N 65
T48D	SNS_DIFF	THERMAL	VR_CPU_ISNS4_P 65 67
T48D	SNS_DIFF	THERMAL	VR_CPU_ISNS4_N 65 67
T48D	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N 65
T68D	SNS_DIFF	THERMAL	P1V05S0_ISN 68
T68J	SNS_DIFF	THERMAL	P1V05S0_ISP 68
T69S	SNS_DIFF	THERMAL	VR_AXG_ISNS_R_P 65
T69S	SNS_DIFF	THERMAL	VR_AXG_ISNS_R_N 65
T69S	SNS_DIFF	THERMAL	VR_AXG_ISNS_N 65 67
T69S	SNS_DIFF	THERMAL	VR_AXG_ISNS_P 65 67
T69D	SNS_DIFF	THERMAL	VR_ISNS_1V05_N 97
T69D	SNS_DIFF	THERMAL	VR_ISNS_1V05_P 97
T69D	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N 50 97
T69D	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P 50 97
T69D	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N 50 97
T69D	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P 50 97
T47S	SNS_DIFF		CPU_VAXG_SENSE_P 13 65
T47S	SNS_DIFF		CPU_VAXG_SENSE_N 13 65
T48D	SNS_DIFF		VR_AXG_VSNS_R_N 65
T48D	SNS_DIFF		VR_AXG_VSNS_R_P 65
T58	SNS_DIFF		VR_AXG_VSEN 65
T59	SNS_DIFF		VR_AXG_RGND 65
T71S	SNS_DIFF		VR_AXG_VSNS_XW_N 65
T14S	SNS_DIFF		VR_AXG_VSNS_XW_P 65
T61D	SNS_DIFF		CPU_VCC_SENSE_N 13 65
T61D	SNS_DIFF		CPU_VCC_SENSE_P 13 65
T61S	SNS_DIFF		VR_CPU_VSEN 65
T71S	SNS_DIFF		VR_CPU_RGND 65
T62	SNS_DIFF		VR_CPU_VSNS_R_N 65
T62	SNS_DIFF		VR_CPU_VSNS_R_P 65
T63S	SNS_DIFF		VR_CPU_VSNS_XW_P 65
T14S	SNS_DIFF		VR_CPU_VSNS_XW_N 65
T66	SNS_DIFF		CPU_VCCIO_SENSE_P 13 68
T67	SNS_DIFF		CPU_VCCIO_SENSE_N 13 68
T43S	SNS_DIFF		P1V05S0_VSEN 68
T43S	SNS_DIFF		P1V05S0_RTN 68

VR CTRL NET PROPERTIES

NET_TYPE	PHYSICAL	SPACING	
T27S	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH1_SNUB 66
T33S	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH2_SNUB 66
T31S	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH3_SNUB 66
T78S	VR_CTL_PHY	SWITCHNODE	VR_CPU_PH4_SNUB 67
T69S	VR_CTL_PHY	VR_CTL	VR_CPU_COMP 65
T69J	VR_CTL_PHY	VR_CTL	VR_AXG_TM 65
T69J	VR_CTL_PHY	VR_CTL	VR_AXG_PWM_R 65
T61S	VR_CTL_PHY	VR_CTL	VR_AXG_PWM 65 67
T62S	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2 65 66
T62D	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1 65 66
T84S	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1_R 65
T84S	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R 65
T83S	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3 65 66
T84S	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R 65
T78S	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4 65 67
T78S	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R 65
T84S	VR_CTL_PHY	VR_CTL	VR_AXG_SW_FREQ 65
T84S	VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP 65
T83S	VR_CTL_PHY	VR_CTL	VR_RSET 65
T83S	VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP_R 65
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT1_RC 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT2_RC 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT3_RC 67
T83S	VR_CTL_PHY	VR_CONTROL	VR_AXG_BOOT1_RC 67
T69S	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT4_RC 67
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_BOOT 66
T83S	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_LGATE 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_UGATE 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_BOOT 66
T83S	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_LGATE 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_UGATE 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_BOOT 66
T83S	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_LGATE 66
T83S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_UGATE 66
T78S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_BOOT 67
T78S	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL 67
T78S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_LGATE 67
T78S	VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_UGATE 67
T69S	VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_BOOT 67
T69S	VR_CTL_PHY	VR_CTL	VR_AXG_DRV1_UGATE_R 67
T69S	VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_LGATE 67
T69S	VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_UGATE 67
T38S	VR_CTL_PHY	VR_CTL	VR_CPU_SW_FREQ 65
T38S	VR_CTL_PHY	VR_CTL	VR_CPU_FB 65
T38S	VR_CTL_PHY	VR_CTL	VR_CPU_FB_R 65
T38S	VR_CTL_PHY	VR_CTL	VR_CPU_RAMP_ADJ 65
T39S	VR_CTL_PHY	VR_CTL	VR_CPU_IMON 50 65
T63S	VR_CTL_PHY	VR_CTL	VR_CPU_SUTH 65
T63J	VR_CTL_PHY	VR_CTL	VR_CPU_N_PSI 65
T63S	VR_CTL_PHY	VR_CTL	VR_CPU_FDVID 65
T64S	VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP 65
T63D	VR_CTL_PHY	VR_CTL	VR_CPU_IAUTO 65
T64S	VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP1 65
T64S	VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP2 65
T64S	VR_CTL_PHY	VR_CTL	VR_CPU_FB_RC 65
T64J	VR_CTL_PHY	VR_CTL	VR_CPU_FB2 65
T64S	VR_CTL_PHY	VR_CTL	VR_CPU_IMON_R 65
T64S	VR_CTL_PHY	VR_CTL	VR_CPU_HFREQ_COMP 65
T68S	VR_CTL_PHY	SWITCHNODE	VR_AXG_PH1_SNUB 67
T62J	VR_CTL_PHY	VR_CTL	VR_AXG_IMON 50 65
T65S	VR_CTL_PHY	VR_CTL	VR_AXG_IMON_R 65
T62S	VR_CTL_PHY	VR_CTL	VR_AXG_HFREQ_COMP 65
T63S	VR_CTL_PHY	VR_CTL	VR_AXG_FB 65
T62S	VR_CTL_PHY	VR_CTL	VR_AXG_R1 65
T63S	VR_CTL_PHY	VR_CTL	VR_AXG_R2 65
T63S	VR_CTL_PHY	VR_CTL	VR_AXG_R3 65
T63S	VR_CTL_PHY	VR_CTL	VR_AXG_COMP_RC 65
T63S	VR_CTL_PHY	VR_CTL	VR_AXG_COMP 65
T63S	VR_CTL_PHY	VR_CTL	VR_AXG_TCOMP 65
T39S	VR_CTL_PHY	SWITCHNODE	P1V05S0_UGATE 68
T39S	VR_CTL_PHY	SWITCHNODE	P1V05S0_LGATE 68
T39S	VR_CTL_PHY	VR_CTL	P1V05S0_BOOT 68
T68S	VR_CTL_PHY	VR_CTL	P1V05S0_BOOT_R 68
T71S	VR_CTL_PHY	VR_CTL	P1V05_IMON 50 68
T71S	VR_CTL_PHY	VR_CTL	P1V05S0_FB 68
T39S	VR_CTL_PHY	VR_CTL	P1V05S0_PHASE_L 68
T69S	VR_CTL_PHY	VR_CTL	P1V05S0_VW 68
T40S	VR_CTL_PHY	VR_CTL	P1V05S0_COMP 68
T40S	VR_CTL_PHY	VR_CTL	P1V05S0_ICOMP 68
T40S	VR_CTL_PHY	VR_CTL	P1V05_S0_VDIFF 68
T40S	VR_CTL_PHY	VR_CTL	P1V05S0_COMP_C 68
T40S	VR_CTL_PHY	VR_CTL	P1V05S0_VDIF_C 68
T40S	VR_CTL_PHY	VR_CTL	P1V05S0_VO 68
T40S	VR_CTL_PHY	VR_CTL	P1V05S0_OCSET 68
T40S	VR_CTL_PHY	VR_CTL	P1V05S0_SNUBBER 68
T71S	VR_CTL_PHY	VR_CTL	P1V05_REG_VFB
T76S	VR_CTL_PHY	VR_CTL	ENET_SR_VFB 36 37
T76S	VR_CTL_PHY	VR_CTL	P1V05S0_ISP_R 68
T80D	VR_CTL_PHY	VR_CONTROL	VR_CPU_TM 65
T80D	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R 69 98
T80D	VR_CTL_PHY	VR_CTL	T29BST_FBX
T69D	VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST 73
T68D	VR_CTL_PHY	VR_CTL	P3V42G3H_FB 73

VR CTRL NET PROPERTIES

NET_TYPE	PHYSICAL	SPACING	
T45J	VR_CTL_PHY	VR_CTL	DDR_REG_CS 72
T83D	VR_CTL_PHY	VR_CTL	DDR_REG_FB 72
T48D	VR_CTL_PHY	VR_CONTROL	DDR_REG_LGATE 72
T89D	VR_CTL_PHY	VR_CONTROL	DDR_REG_UGATE 72
T44S	VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT 72
T44S	VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT_R 72
T41J	VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS 72
T41J	VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS 72
T44J	VR_CTL_PHY	VR_CTL	DDR_REG_PHASE_R 72
T42S	VR_CTL_PHY	VR_CTL	DDR_REG_UGATE_R 72
T42D	VR_CTL_PHY	SWITCHNODE	1V5_SNUBBER 72
T42D	VR_CTL_PHY	VR_CTL	P1V8_REG_VFB 72
T42J	VR_CTL_PHY	VR_CTL	P1V8_REG_SYNC 72
T45D	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT 71
T45D	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT_R 71
T45D	VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB 71
T45J	VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN 71
T45S	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_LGATE 71
T45S	VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET 71
T45S	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_VOUT1 71
T47D	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_FSET1 71
T45D	VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_UGATE 71
T45J	VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB 71
T43S	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_BOOT 71
T46J	VR_CTL_PHY	VR_CTL	P5VS3_REG_FB 71
T46D	VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN 71
T46S	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_LGATE 71
T46S	VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET 71
T46D	VR_CTL_PHY	VR_CTL	P5VS3_REG_FSET2 71
T47D	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_UGATE 71
T47D	VR_CTL_PHY	VR_CONTROL	P5VS3_REG_VOUT2 71
T41D	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT1 69
T41D	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2 69
T75S	VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R 69 98
T42D	VR_CTL_PHY	VR_CTL	VCCSA_OUT 69
T42J	VR_CTL_PHY	VR_CTL	VCCSA_GATE 69
T43D	VR_CTL_PHY	VR_CTL	VCCSA_REF 69
T83S	VR_CTL_PHY	VR_CTL	VCCSA_CRL 69
T42S	VR_CTL_PHY	VR_CTL	CPU_VCCSA_SENSE 13 69
T47S	VR_CTL_PHY	VR_CTL	VR_CPU_TM 65
T83J	VR_CTL_PHY	PM	3V3R2V9_DPAPWR_ADJ 83 100

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.35MM	?

VR VID NET PROPERTIES

NET_TYPE	PHYSICAL	SPACING	
T47S	VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK_R 13
T47C	VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L_R 13
T47S	VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT_R 13
T49J	VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK 13 65
T49D	VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L 13 65
T65D	VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT 13 65

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_VIDS	*	=4X_DIELECTRIC	?

SYNC_MASTER=K62_JERRY SYNC_DATE=01/09/2011

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T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	TOP,BOTTOM	=7X_DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	0.2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_XTAL_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_XTAL	*	=4X_DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SMB	*	=2x_DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_COMP	*	0.2 MM	?

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING (NET_TYPE)		
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_P<3..0>	85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_N<3..0>	85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_P<3..0>	85 86 87 88
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_N<3..0>	85 86 87 88
NO_TEST=TRUE	T29_90D	T29	T29_R2D_P<3..0>	85 87
NO_TEST=TRUE	T29_90D	T29	T29_R2D_N<3..0>	85 87
NO_TEST=TRUE	T29_90D	T29	T29_D2R_P<3..0>	85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_D2R_N<3..0>	85 87 89
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_P<3..0>	85 87
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_N<3..0>	85 87
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_P<3..0>	85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_N<3..0>	85 86
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_P<3..0>	87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_N<3..0>	87 88
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_P	85 86
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_N	85 86
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_P	85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_N	85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_P	87
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_N	87
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_P	87 88
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_N	87 88
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_P	86
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_N	86
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_P	88
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_N	88
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<0>	85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<0>	85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<2>	85 86
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<2>	85 86
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<0>	87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<0>	87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<2>	87 88
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<2>	87 88
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	18 89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	89
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	89
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	18 89
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	18 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_P<3..0>	84 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_N<3..0>	84 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	79 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_P	84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_N	84
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	84 89
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	84 89
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_P	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_N	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_P	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_N	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_P<3..0>	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_N<3..0>	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_P<3..0>	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_N<3..0>	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_P<3..0>	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_N<3..0>	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_P<3..0>	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_N<3..0>	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_P<3..0>	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_N<3..0>	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_P<3..0>	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_N<3..0>	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_N	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_P	85
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_N	87
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_P	87

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING (NET_TYPE)		
	T29_SPI_55S	T29_SPI	JTAG_T29_TDI	15 21 89
	T29_SPI_55S	T29_SPI	JTAG_T29_TMS	15 18 89
	T29_SPI_55S	T29_SPI	JTAG_T29_TCK	15 21 25 89
	T29_SPI_55S	T29_SPI	JTAG_T29_TDO	15 21 89
U43?	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	89
U43H	T29_SPI_55S	T29_SPI	T29_SPI_MISO	89
U43G	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	89
U44D	T29_SPI_55S	T29_SPI	T29_SPI_CLK	89
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	80 89 99
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	89 99
	T29_SMB_55S	T29_SMB	I2C_T29_SDA	49 89
	T29_SMB_55S	T29_SMB	I2C_T29_SCL	49 89
U42?	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	80
U42G	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	80
U42J	CLK_25M_55S	CLK_25M	ENET_CLK25M_XTALI_OSC	36 80
U42K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_CLK	80
U43K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	80 89 99
U42K	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	89 99
U42C	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2	80
U42D	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2_R	80
U42?	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X1	80
U43J	T29_55S	T29_COMP	T29_RSENSE	89
U43J	T29_55S	T29_COMP	T29_RBIAS	89
U43K		T29_COMP	T29_A_BIAS	79 83 85 86
U43K		T29_COMP	T29_B_BIAS	79 83 87 88
U42K		T29_COMP	DP_A_BIAS	79 85

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE PHYSICAL	NET_TYPE SPACING		
I357	PM	4V5_REG_EN	56
I358	PM	3V42G3H_SHDN_L	73
I359	PM	ALL_SYS_PWRGD_R	5 32 64
I360	PM	ALL_SYS_PWRGD_SMC	46 64
I361	PM	AP_PWR_EN	20 25 33
I362	PM	AP_MINI_RESET_L	33
I363	PM	AUD_I2C_INT_L	20 62
I364	PM	AUD_IP_PERIPHERAL_DET	20 61
I365	PM	AUD_IPHS_SWITCH_EN	21 62
I366	PM	AUD_SPDIF_IN	60 84 94
I367	PM	AUD_SPDIF_IN_CODEC	56 84
I368	PM	BDV_BKL_PWM	46 84 100
I369	PM	BL_PWM	6 84
I410	PM	BL_EN	6 82
I411	PM	BDV_BKL_PWM	46 84 100
I369	PM	CK505_27MHZ_EN	26
I370	PM	CPUVTT_REG_EN	
I371	PM_VTT	CPUVTT_REG_PGOOD_R	63
I372	PM	CPU_MEM_RESET_L	11 32
I373	PM	CPU_PECI_R	46
I374	PM_VTT	CPU_PWRGD	11 21 25
I375	PM	CPU_RESET_L	11 27
I376	PM	CPU_SKTOCC_L	11 63
I377	PM	CPU_CATERR_L	11
I378	PM	CPU_PECI	11 21 46
I379	PM	CPU_PROCHOT_L	11 47 65
I380	PM	CPU_THRMTRIP_L	11 47
I381	PM	CPU_PROC_SEL	11 19
I382	PM	DEBUG_RESET_L	27 48
I383	PM	DDRVTT_EN	
I384	PM	DP_INT_SPDIF_AUDIO	82 84
I385	PM	DP_INTPNL_HPD	82 84
I386	PM	3V3R2V9_DPAPWR_ADJ	83 98
I387	PM	DP_A_PWRDWN	85
I388	PM	DP_A_PWRDWN_FET_R	83
I389	PM	DP_A_PWRDWN_INV	83
I390	PM	DPAPWRSW_HVEN_L_R	83
I391	PM	DPAPWRSW_CT	83
I392	PM	DPAPWRSW_ILIM	83
I393	PM	DPAPWRSW_IFLT	83
I394	PM	T29_A_HV_EN	83 85
I395	PM	3V3R2V9_DPBPWR_ADJ	83
I396	PM	DP_B_PWRDWN	87
I397	PM	DP_B_PWRDWN_FET_R	83
I398	PM	DP_B_PWRDWN_INV	83
I399	PM	DPBPWRSW_HVEN_L_R	83
I400	PM	DPBPWRSW_CT	83
I401	PM	DPBPWRSW_ILIM	83
I402	PM	DPBPWRSW_IFLT	83
I403	PM	T29_B_HV_EN	83 87
I404	PM	T29_PWR_EN	18 81 100
I429	PM	T29_RESET_RTR_L	81 89
I412	PM	LCD_BL_FILT	84
I413	PM	LCD_BLK_ON_DLY	
I405	PM	LCD_BL_PWM	84
I406	PM	MXM_PNL_BL_PWM	77 84

NET_TYPE PHYSICAL	NET_TYPE SPACING		
I230	PM	ENET_PWR_EN	20 25 36
I224	PM	ENET_LOW_PWR	15 21 37
I229	PM	FW_RESET_L	27 39
I231	PM	ENET_RESET_L	27 36
I236	PM	FW_PME_L	15 21 39
I237	PM	FW_PWR_EN	15 21
I235	PM	FW_CLKREQ_L	15 39
I248	PM	ISOLATE_CPU_MEM_L	21 25 32
I260	PM	LPC_PWRDWN_L	19 46 48
I269	PM	MEM_RESET_L	30 31 32 92
I262	PM	MINI_CLKREQ_L	15 33
I263	PM	MINI_RESET_L	27 33
I264	PM	MXM_CLKREQ_L	9 76
I267	PM	MXM_GOOD	5 21 25
I270	PM	ODD_PWR_EN_L	15 21 42
I68	PM	RTC_RESET_L	18 27 100
I48	PM	RSMRST_PWRGD	46 64
I67	PM	RTC_RESET_L	18 27 100
I331	PM	S4_ENABLES	63
I268	PM	SDCONN_STATE_RST_L	
I408	PM	SDCONN_DETECT_BUF_L	95
I407	PM	SDCONN_STATE_CHANGE	20 25 45
I265	PM	SDCARD_RESET	15 21 44 101
I334	PM	SDCARD_RESET_L	44
I416	PM	SDCARD_PLT_RST_L	27 44
I335	PM	SDCARD_PLT_RST_L_R	
I415	PM	SMC_PM_G2_EN	46 75
I336	PM	SMC_PM_G2_EN_R	75
I414	PM	SMC_PM_G2_EN_L	75
I338	PM	S5_DG_1	75
I339	PM	S5_MSFT_G1	75
I418	PM	USE_HDD_OOB_L	20 51
I419	PM	HDD_OOB_1V00_REF	51
I420	PM	SMC_ADAPTER_EN	19 46 47
I340	PM	SMC_RUNTIME_SCI_L	21 46 47
I341	PM	SMC_WAKE_SCI_L	15 18 21 46
I342	PM	SMC_DELAYED_PWRGD	47 64
I343	PM	SMC_LRESET_L	27 46
I344	PM	SMC_RESET_L	46 47 48
I345	PM	SMC_PROCHOT	46 47
I417	PM	SMC_PROCHOT_3_3_L	46 47
I421	PM	SMC_ONOFF_L	46 47
I422	PM	SMC_MANUAL_RST_L	47
I259	PM	SPI_DESCRIPTOR_OVERRIDE_L	18 46
I416	PM	T29_PWR_EN	18 81 100
I350	PM	T29_RESET_L	27 81
I409	PM	T29_DP_PORTA_PWR_EN	20 25 83 94
I409	PM	T29_DP_PORTA_PWR_EN_REG	83
I355	PM_VTT	XDP_CPUPWRGD	
I261	PM_VTT	XDP_DBRESET_L	11 25
I266	PM_VTT	XDP_PWRGD	
I266	PM	XDPPCH_PLTRST_L	25 27
I256	PM	USB_HUB_SOFT_RESET_L	20 25 34
I424	PM	VSYNC_DP_CONN	6 82
I424	PM	VSYNC_DP	82
I424	PM	VIDEO_ON	82
I344	PM	VTT_REG_PGOOD_L	63

NET_TYPE PHYSICAL	NET_TYPE SPACING		
I272	PM	PLT_RESET_L	20 27
I442	PM_VTT	PLT_RESET_LS1V05_L	11
I273	PM	PM_BATLOW_L	15 19 46
I274	PM	PM_CLK32K_SUSCLK	9 46 94
I275	PM	PM_CLK32K_SUSCLK_R	9 19 94
I277	PM	PM_CLKRUN_L	15 19 46 48
I278	PM	PM_PWRBTN_L	19 25 46
I279	PM	PM_RSMRST_L	27 46
I276	PM	PM_RSMRST_PCH_L	19 27
I138	PM	PCH_SRTCRST_L	18
I137	PM	PCH_INTVRMEN_L	18
I141	PM	PCH_DSWVRMEN	19
I139	PM	PCH_DF_TVS	19
I152	PM	PCH_PROCPWRGD	21
I144	PM	PCIE_WAKE_L	19 33 36 79
I442	PM	PM_DSW_PWRGD	19
I443	PM	PM_ASW_PWRGD	19 64
I140	PM	PM_MEM_PWRGD_R	11
I450	PM	PM_EN_DDR1V5_S3_REG	63 72
I437	PM	PM_EN_DDRVTT_S0_REG	32 63 72
I438	PM	PM_EN_P12V_S0_FET	6 63
I446	PM	PM_EN_P1V05_S0_REG	63 68
I470	PM	PM_EN_P1V05_S3_REG	
I473	PM	PM_EN_P1V5_S0_FET	63 74
I472	PM	PM_EN_P1V8_S0_REG	63 72
I475	PM	PM_EN_P3V3_S0_FET	63 74
I476	PM	PM_EN_P3V3_S3_FET	63 74
I477	PM	PM_EN_P3V3_S5_REG	71
I478	PM	PM_EN_P5V_S0_FET	63 74
I479	PM	PM_EN_P5V_S3_REG	63 71
I480	PM	PM_EN_PVCCSA_S0_REG_L	64
I440	PM	PM_EN_VCCSA_S0_CPU	
I479	PM	PM_EN_PVCORE_CPU	63 65
I139	PM_VTT	PM_MEM_PWRGD	11 19 100
I151	PM	PM_MXM_EN	64 77
I132	PM	PM_PCH_PWRGD_R	64
I133	PM	PM_PECI_PWRGD	46 64
I135	PM	PM_PECI_PWRGD_R	46
I136	PM	PM_PGOOD_DDR1V5_S3_REG	5 63 72
I137	PM	PM_PGOOD_P1V05_S0_REG	63 64 68
I138	PM	PM_PGOOD_P1V5_S0_FET	11 64 74
I140	PM	PM_PGOOD_P1V8_S0_REG	64 72
I139	PM	PM_PGOOD_P3V3_S0_FET	63 64 74
I141	PM	PM_PGOOD_P3V3_S3_FET	34 74
I142	PM	PM_PGOOD_P3V3_S5_REG	27 64 71
I143	PM	PM_PGOOD_P5V_S0_FET	63 64 74
I281	PM	PM_PGOOD_MINI	33
I282	PM	PM_PGOOD_PVCORE_CPU	5 25 64 65
I283	PM	PM_PGOOD_PVCCSA_S0_REG	63 64
I284	PM	PM_PGOOD_P5V_S3_REG	63 71 83
I285	PM	PM_PGOOD_PVAXG	5 65
I439	PM_VTT	PM_MEM_PWRGD	11 19 100
I441	PM	PM_MEM_PWRGD_L	11
I254	PM	PM_MXM_PGOOD	64 77
I253	PM	PM_PCH_PWRGD	19 21 64
I287	PM	PM_SLP_S3_5V	32
I287	PM	PM_SLP_S3_5V_L	32
I286	PM	PM_SLP_S3_5V_R2	32
I288	PM	PM_SLP_S3_L	5 19 26 32 36 46 47 63
I289	PM	PM_SLP_S4_L	5 19 32 46 47 63 100
I290	PM	PM_SLP_S5_L	5 19 46 47 63
I427	PM_VTT	PM_SYNC	11 19
I255	PM	PM_SYSRST_L	19 25 27 46
I480	PM	PM_SYS_PWRGD	19 32 64
I481	PM_VTT	PM_THRMTRIP_L	21 47
I482	PM	PM_SLP_S3_BUF_L	63
I483	PM	PM_SLP_S4_1_L_R	63
I484	PM	PM_SLP_S4_D_L	32
I485	PM	PM_SLP_S4_L	5 19 32 46 47 63 100
I438	PM	PGOOD_P1V5_S0_DLY	11
I439	PM	PGOOD_1V8_S0_G1	64
I440	PM	PGOOD_1V8_S0_G2	64
I480	PM	PGOOD_P12V_S0	63 64
I430	PM	PGOOD_P1V8_S0	64
I431	PM	PGOOD_PCH_S0	5 64
I429	PM	PGOOD_PCH_S0_R	64 94
I315	PM	PGOOD_SYSPWROK	64
I316	PM	PGOOD_SYSPWROK_R	64
I317	PM	POWER_BUTTON_L	47
I331	PM	PEG_RESET_L	9 27
I431	PM	PGOOD_CPU_S0	64
I422	PM	PGOOD_CPU_UNCORE	64 94
I424	PM	PGOOD_5V_1V05_3V3	64 94
I426	PM	PGOOD_3V3_1V05	64 94
I427	PM	PGOOD_12V_S0_G1	64
I428	PM	PGOOD_12V_S0_G2	64
I422	PM	9V_COMP_REF	64
I426	PM	12V_COMP_REF	64
I430	PM	ALL_SYS_PWRGD	64 94

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

98 6 IN PP5V_S3 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
95 44 IN USB_CAMERA_L_P FUNC_TEST=TRUE
95 44 IN USB_CAMERA_L_N FUNC_TEST=TRUE
95 44 IN USB_BT_L_P FUNC_TEST=TRUE
95 44 IN USB_BT_L_N FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

100 44 21 15 IN SDCARD_RESET FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

95 44 IN USB_IR_L_P FUNC_TEST=TRUE
95 44 IN USB_IR_L_N FUNC_TEST=TRUE
98 44 IN PP5V_S3_IR_FLT FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42 IN SMC_ODD_DETECT FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

97 52 IN SNS_ODD_P FUNC_TEST=TRUE
97 52 IN SNS_ODD_N FUNC_TEST=TRUE

J5600 ODD FAN

53 IN FAN_0_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH0_L FUNC_TEST=TRUE
98 53 IN PP12V_S0_FAN0_L FUNC_TEST=TRUE
53 IN FAN_0_GND FUNC_TEST=TRUE

J5700 CPU FAN

54 IN FAN_2_PWR_L FUNC_TEST=TRUE
54 IN FAN_TACH2_L FUNC_TEST=TRUE
98 54 IN PP12V_S0_FAN2_L FUNC_TEST=TRUE
54 IN FAN_2_GND FUNC_TEST=TRUE
97 52 IN SNS_AMB_P FUNC_TEST=TRUE
97 52 IN SNS_AMB_N FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53 IN FAN_1_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH1_L FUNC_TEST=TRUE
98 53 IN PP12V_S0_FAN1_L FUNC_TEST=TRUE
53 IN FAN_1_GND FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

97 51 42 IN HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

97 52 44 IN SNS_SKIN_LEFT_P FUNC_TEST=TRUE
97 52 44 IN SNS_SKIN_LEFT_N FUNC_TEST=TRUE
97 52 IN SNS_SKIN_RIGHT_P FUNC_TEST=TRUE
97 52 IN SNS_SKIN_RIGHT_N FUNC_TEST=TRUE

J6602 AUDIO RIGHT SPEAKER

94 IN AUD_SPKR_OUTL02R_POUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTL02R_NOUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTL01R_POUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTL01R_NOUT FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

94 IN AUD_SPKR_OUTL02L_POUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTL02L_NOUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTL01L_POUT FUNC_TEST=TRUE
94 IN AUD_SPKR_OUTL01L_NOUT FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

2 TP'S

98 60 IN PP3V3_AUDIO_SPDIF_JACK FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
60 IN AUD_LI_DET_JACK FUNC_TEST=TRUE
60 IN AUD_LI_R_JACK FUNC_TEST=TRUE
60 IN AUD_LI_GND_JACK FUNC_TEST=TRUE
60 IN AUD_LI_L_JACK FUNC_TEST=TRUE
60 IN HS_MIC_HI_JACK FUNC_TEST=TRUE
60 IN AUD_HP_L_JACK FUNC_TEST=TRUE
60 IN AUD_HP_GND_JACK FUNC_TEST=TRUE
60 IN AUD_HP_R_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TYPEDET_JACK FUNC_TEST=TRUE
60 IN AUD_IP_PERPH_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TIPDET_JACK FUNC_TEST=TRUE
60 IN AUD_SPDIFIN_JACK FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

GND 17 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=17

98 6 IN PP3V3_S3 2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2

98 6 IN PP5V_S0 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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