1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

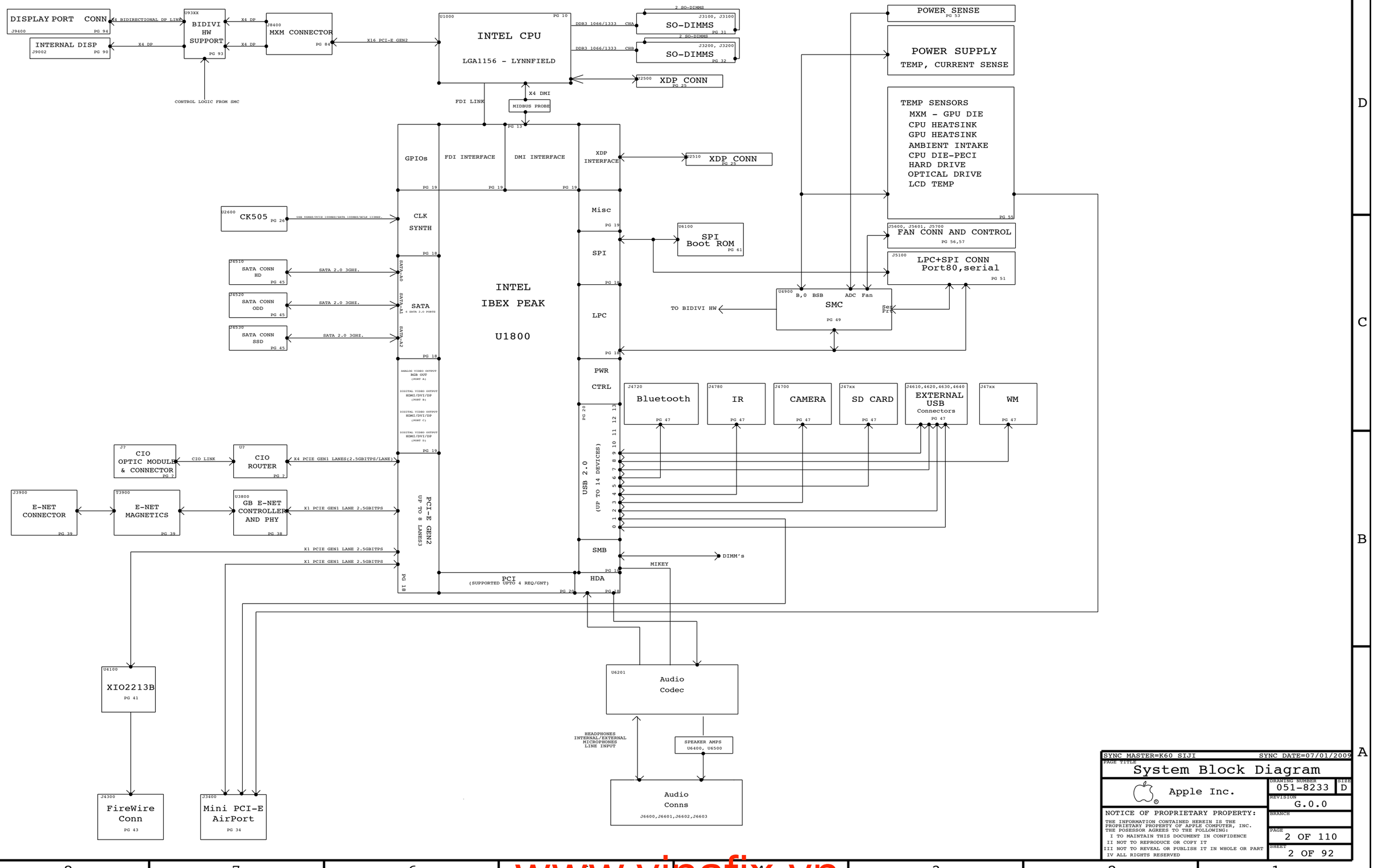
REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
G	0000830522	PRODUCTION RELEASED	2009-12-07

K23F MLB

LAST_MODIFIED=Mon Dec 7 09:47:19 2009

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Mon Dec 7 09:47:19 2009

DRAWING TITLE: sch,k61,Kalahari,mlb
Apple Inc.
DRAWING NUMBER: 051-8233
SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 1 OF 110
SHEET: 1 OF 92



SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE

System Block Diagram

Apple Inc.

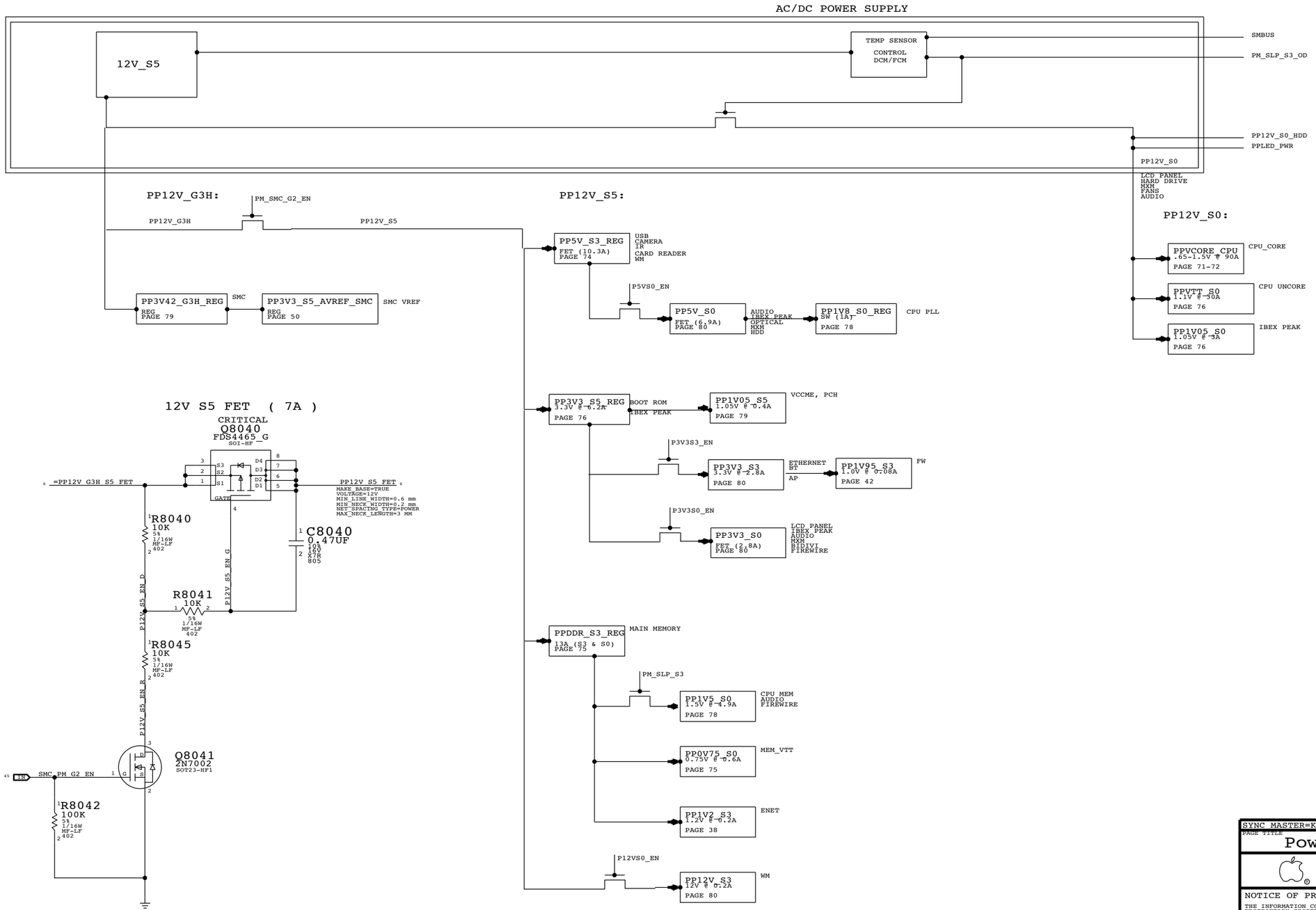
DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 2 OF 110

SHEET 2 OF 92



SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 3 OF 110

SHEET 3 OF 92

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0439	PCBA,MLB,K23F,2.66GHZ,MOLEX SOCKET	K23F,2P66GHZ_CPU,BASIC,CPUPOC_IMAX_100_120,MOLEX_SOCKET
639-0440	PCBA,MLB,K23F,2.80GHZ,MOLEX SOCKET	K23F,2P80GHZ_CPU,BASIC,CPUPOC_IMAX_100_120,MOLEX_SOCKET
639-0685	PCBA,MLB,K23F,2.66GHZ,FOXCONN SOCKET	K23F,2P66GHZ_CPU,BASIC,CPUPOC_IMAX_100_120,FOXCONN_SOCKET
639-0684	PCBA,MLB,K23F,2.80GHZ,FOXCONN SOCKET	K23F,2P80GHZ_CPU,BASIC,CPUPOC_IMAX_100_120,FOXCONN_SOCKET
085-1023	PCBA,MLB,DEV,K23F	DEVELOPMENT,DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,BETTER,MXM,XDP_CPU_BPM,INT_VREF,PCH_VRM,BUF_CLK,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_TDIODE,MEM_RESET_HW

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S3828	1	IC,IBEX PEAK B3 PRQ,DESKTOP,FCBGA,P425	U1800	CRITICAL	
	359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
	341T0211	1	IC,EFI BOOTROM,K23F	U6100	CRITICAL	
	338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	343S0485	1	IC,BCM5764M,68PIN QFN	U3700	CRITICAL	
RAW: 335S0663	341T0213	1	IC,FLASH,45DB0011D,SOIC-8S1	U3701	CRITICAL	
	511S0063	1	SOCKET,MOLEX,LGA1156,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
	511S0069	1	SOCKET,FOXCONN,LGA1156,CPU-LF	U1000	CRITICAL	FOXCONN_SOCKET
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3810	1	LFD,SLBLC,PRQ,2.66,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P66GHZ_CPU
337S3811	1	LFD,SLBJJ,PRQ,2.80,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P80GHZ_CPU

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293		C7460,C7461,C7462,C7463	

K23F PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-8233	1	SCH,K23F,MLB	SCH1		K23F
	820-2733	1	PCBF,K23F,MLB	MLB1		K23F
(338S0489 - BLNK)	341T0212	1	IC,SMC,K23F	U4900	CRITICAL	K23F

SYNC MASTER=K60 AARON SYNC DATE=07/01/2009

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

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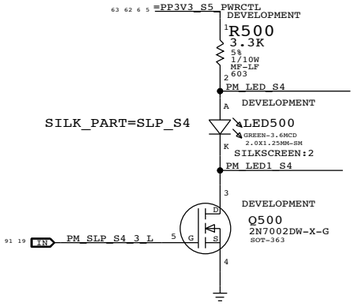
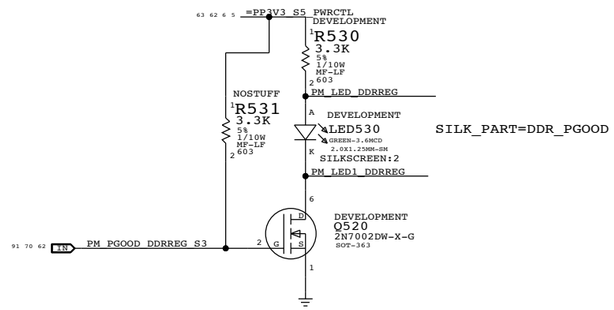
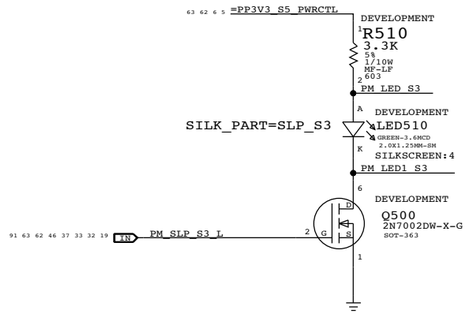
PAGE 4 OF 110

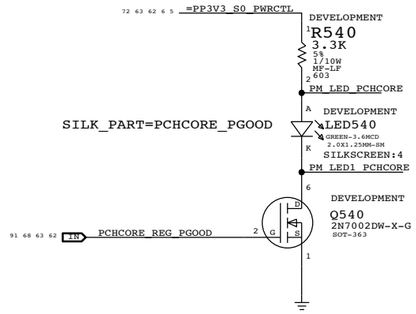
SHEET 4 OF 92

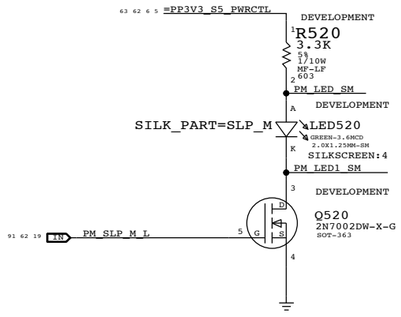
CAN DELETE THESE FOR PROTO1 AND BEYOND

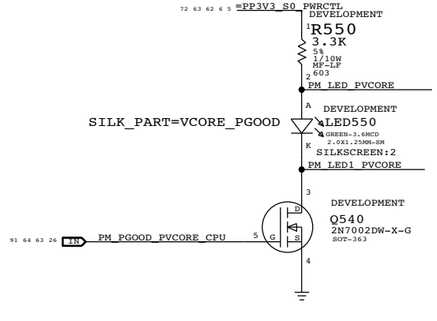












State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE: PROTO 0 DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: G.0.0

BRANCH:

PAGE: 5 OF 110

SHEET: 5 OF 92

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

EMC: C600,C626,C627,C628,C629,C630,C631

PLACE AT J600.

=SMB_ACDC_SCL
=PP5V_S0_SATA
PP12V_G3H
LCD_PWM
=SMB_ACDC_SDA
PP12V_S0
LCD_BKL_ON

C623 10UF 20% 10V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 10% 16V X5R-CERM 1210

PM_ACDC_PS_ON
PM_SLPS3_BUF2_L
Q610 2N7002 SOT23-HF1
C600 0.001UF 10% 50V X7R 402

PP3V3_S3
R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT
LED605 GREEN-3.6MCD 2.0X1.25MM-SM

PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:1

PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:2
CORE_VOLTAGES_ON
ALL_SYS_PWRGD_R
Q602 2N7002DW-X-G SOT-363

PP3V3_S0
MXM
R604 1K 5% 1/16W MF-LF 402
GPU_PRESENT_R
MXM
LED604 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:3
GPU_PRESENT_DRAIN
MXM_GOOD
Q602 2N7002DW-X-G SOT-363

PP3V3_S0
R603 1K 5% 1/16W MF-LF 402
LCD_SHOULD_ON_R
LED603 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:4
VIDEO_ON_L

"S0" RAILS

ONLY ON IN RUN

PPVTT_S0_DDR
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_DDR_FET 32
→ =PP0V75_S0_MEM_VTT_B 31
→ =PP0V75_S0_MEM_VTT_A 30

PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVCORE_S0_CPU_REG 64 65 66
→ =PPVCORE_S0_CPU 13 16

PPVTT_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PPVTT_S0_CPU 11 13 16 46 64

PPVTT_S0
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_CPU_REG 49 67
→ =PPVTT_S0_PCH_VCC_DMI 22 24
→ =PPVTT_S0_XDP 25
→ =PPVTT_S0_PCH_VCCP_CPU 22 24

PP1V5_CPU_MEM
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP1V5_CPU_MEM 11 13 16 29

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V5_S0_FET 49 72
→ =PP1V5_S0_AUD_DIG 55
→ =PP1V5_FWRS0_FWXIO 39
→ =PP1V5_S0_CK505 26

PP1V8_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP1V8_S0_CPU_PLL 13 16 63

PP1V8_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V8_S0_REG 49 70
→ =PP3V3R1V8_S0_PCH_VCCPNAND 22 24
→ =PP1V8R1V5_S0_PCH_VCCVRM 24

PPVAXG_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PPVAXG_S0_CPU 13 17

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S0_FET 72
→ =PP3V3_S0_PCH 18 21 24 68
→ =PP3V3_S0_FAN 52 53
→ =PP3V3_S0_PCH_VCCADAC 17
→ =PPSPD_S0_MEM_A 30 46
→ =PPSPD_S0_MEM_B 31
→ =PP3V3_S0_VRD 64
→ =PP3V3_S0_AUDIO 55 57 58 59 60 61
→ =PP3V3R1V5_S0_PCH_VCCSUSHDA 22 24
→ =PP3V3_S0_SMBUS 48
→ =PP3V3_S0_SMC_LS 46 51
→ =PP3V3_S0_SMBUS_SMC_0_S0 48
→ =PP3V3_S0_SMBUS_SMC_B_S0 48
→ =PP3V3_S0_SMBUS_SMC_MGMT 48
→ =PP3V3_S0_DPCONN 80
→ =PP3V3_S0_TSENS 51
→ =PP3V3_S0_MXM 63 73 74
→ =PP3V3_S0_XDP 25
→ =PP3V3_S0_ODD 42
→ =PP3V3_S0_SATALED 18 42
→ =PP3V3_S0_SMC 46 49 50
→ =PP3V3_S0_PWRCTL 5 62 63 72
→ =PP3V3_S0_PCH_VCC3_3_CORE 22 24
→ =PP3V3_S0_VIDEO 77
→ =PP3V3_FW_FWPHY 39 40 41
→ =PP3V3_FWRS0_FWXIO 39
→ =PP3V3_S0_DP 77 78 79 81
→ =PP3V3_S0_PCH_VCC3_3_PCI 22 24
→ =PP3V3_S0_CK505 26
→ =PP3V3_S0_PCH_GPIO 20
→ =PP3V3_S0_PCH_STRAPS 15
→ =PP3V3_S0_PCH_VCC3_3_SATA 22 24
→ =PP3V3_S0_RSTBUF 27
→ =PP3V3_S0_ME 72
→ =PP3V3_S0_ENET 36
→ =PP3V3_S0_PCH_PM 27
→ =PP3V3_S0_SMBUS_SMC_BSA 48

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S0_FET 72
→ =PP5V_S0_AUDIO 55 61
→ =PP5V_S0_SATA 6 42
→ =PP5V_S0_MXM 73
→ =PP5V_S0_VRD 64
→ =PP5V_S0_ISENSE 49
→ =PP5V_S0_P1V8_VREG 70
→ =PP5V_S0_PCH 24
→ =PP5V_S0_CPU_VTT_VREG 67
→ =PP5V_S0_LPCPLUS 47
→ =PP5V_S0_PCH_CORE_VREG 68

PP1V05_S0
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V05_S0_REG 68
→ =PP1V05_S0_PCH_VCCADPLL 17
→ =PP1V05_S0_PCH_VCCIO_DMI 22 24
→ =PP1V05_S0_PCH 24
→ =PP1V05_S0_SM_FET 72
→ =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
→ =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
→ =PP1V05_S0_PCH_VCC_CORE 22 24
→ =PP1V05_S0_PCH_VCCIO_USB 22 24
→ =PP1V05_S0_CK505 26

PP1V05_SM_PCH_LAN
MAKE_BASE=TRUE
VOLTAGE=1.05V
THIS NET IS NOT CONNECTED TO ANY VOLTAGE RAIL. INSTEAD ON PAGE 24 IT IS CONNECTED TO GND THROUGH A RESISTOR
→ =PP1V05_SM_PCH_VCC_LAN 22 24

PP0V75_S0
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PPVTT_S0_DDR_LDO 70
→ =PP0V75_S0_MEM_VTT_S0FET 32

PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP12V_S0_FAN 52 53
→ =PP12V_S0_AUDIO_SPKRAMP 60
→ =PP12V_S0_VRD 64
→ =PPV_S0_MXM_PWR 50
→ =PP12V_S0_LCD 77
→ =PP12V_S0_PCH_CORE_VREG 68
→ =PP12V_S0_CPU_VTT_VREG 67
→ =PP12V_S0_PWRCTL 63

"S3" RAILS

ON IN RUN AND SLEEP

PP1V5_S3
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V5_S3_REG 49 50 70
→ =PP1V5_S3_MEMRESET 32
→ =PPDDR_S3_S0FET 72
→ =PP1V5_S3_MEM_A 28 29 30
→ =PP1V5_S3_MEM_B 28 29 31

PP12V_S3
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP12V_S3_FET 72
→ =PP12V_S3_WM 44

PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S3_FET 72
→ =PP3V3_S3_VREFMRGN 28
→ =PP3V3_S3_BT 44
→ =PP3V3_S3_PCH_STRAPS 15
→ =PP3V3_S3_SDCARD 44
→ =PP3V3_S3_SMBUS_SMC_A_S3 48
→ =PP3V3_S3_MINI 33
→ =PP3V3_S3_PWRCTL 63 72
→ =PP3V3_S3_WM 44
→ =PP3V3_S3_SMBUS 48
→ =PP3V3_S3_MEMRESET 32
→ =PP3V3_S3_BRCRYPT 44
→ =PP3V3_S3_ENET 37
→ =PP3V3_S3_USB_HUB 34 35
→ =PP3V3_S3_USB_RESET 34

PP5V_S3
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S3_REG 69 92
→ =PP5V_S3_USB 43
→ =PP5V_S3_S0FET 72
→ =PP5V_S3_CAMERA 44
→ =PP5V_S3_IR 44
→ =PP5V_S3_VREFMRGN 28
→ =PP5V_S3_PWRCTL 62
→ =PP5V_S3_MEMRESET 32
→ =PP5V_S3_DDR_VREG 70
→ =PP5V_S3_BRAY 44

PP3V3_S0M
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_SM_FET 72
→ =PP3V3_SM_PCH_VCC_ME 22 24
→ =PP3V3_SM_PWRCTL 63 72

PP1V05_SM
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V05_SM_FET 72
→ =PP1V05_SM_PCH_VCC_ME 22 24
→ =PP1V05_SM_ME 63

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

PP1V05_S5
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP1V05_S5_REG 71
→ =PP1V05_S5_SM_FET 72

PP3V3_S5
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V3_S5_REG 6 69
→ =PP3V3_S5_PCH 18 19 24
→ =PP3V3_S5_PCH_GPIO 20
→ =PP3V3_S5_ROM 47 54
→ =PP3V3_S5_PCH_VCCSUS3_3_USB 22 24
→ =PP3V3_S5_PWRCTL 5 62 63
→ =PP3V3_S5_S3FET 72
→ =PP3V3_S5_S0FET 72
→ =PP3V3_S5_P1V05S5_VREG 71
→ =PP3V3_S5_SM_FET 72
→ =PP3V3_S5_PCH_STRAPS 15
→ =PP3V3_S5_CPURESET 11
→ =PP3V3_S5_XDP 25
→ =PP3V3_S5_MEMRESET 32
→ =PP3V3_S5_LPCPLUS 47

PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP5V_S5_LDO 69
→ =PP5V_S5_PCH 24

PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP12V_S5_FET 3
→ =PP12V_S5_DDR_VREG 70
→ =PP12V_S5_P3V3S5_VREG 69
→ =PP12V_S5_P5VS3_VREG 69
→ =PP12V_S5_S3_FET 72
→ =PP12V_S5_PWRCTL 63 72
→ =PP12V_S5_FW 41

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

PP3V42_G3H
MAKE_BASE=TRUE
VOLTAGE=3.42V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ PP3V42_G3H_REG 71
→ =PP3V3_S5_RTC_D 27
→ =PP3V3_G3H_SMC 45 46
→ =PP3V3_G3H_SMCUSBMUX 43
→ =PP3V42_G3H_AVREF 46
→ =PP3V3_G3H_LPCPLUS 47

PP12V_G3H
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
NET_SPACING_TYPE=POWER
MAX_NECK_LENGTH=3 MM
→ =PP12V_G3H_S5_FET 3

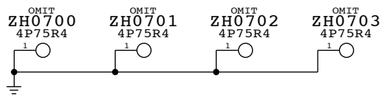
GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009
PAGE TITLE
Power Conn / Alias
Apple Inc.
DRAWING NUMBER 051-8233
SIZE D
REVISION G.0.0
BRANCH
PAGE 6 OF 110
SHEET 6 OF 92

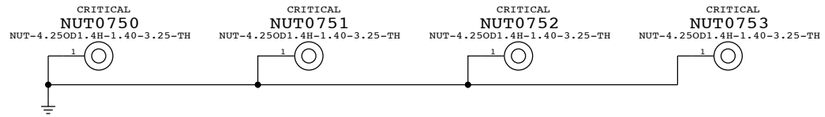
CPU Heatsink

4mm Plated Holes (998-0850)



DIMM CONNECTOR NUTS

Nuts (805-9582)



PCH HEATSINK

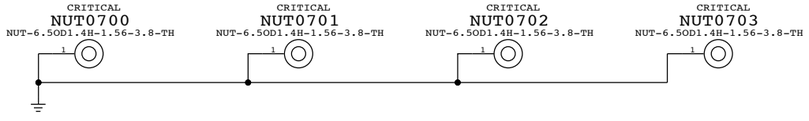
EMC Springs (870-1125) Removed 2009-10-05

Rear Cover

Standoffs (860-1255)

Backer Plate

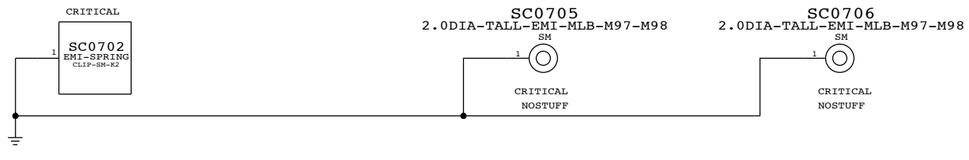
Nuts (835-0269)



For EMC

EMC Spring (870-1577); Near DIMMs

EMC POGO Pins (870-1698); Near DIMMs



SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE

Holes

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 7 OF 110

SHEET 7 OF 92

UNUSED CPU SIGNALS

TP_CPU_RSVD<41..29> = NC_CPU_RSVD<41..29> MAKE_BASE=TRUE NO_TEST=TRUE
TP_CPU_RSVD<26..1> = NC_CPU_RSVD<26..1> MAKE_BASE=TRUE NO_TEST=TRUE
TP_CPU_FC_AE38 = NC_CPU_FC_AE38 MAKE_BASE=TRUE NO_TEST=TRUE
TP_CPU_FC_AG40 = NC_CPU_FC_AG40 MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

TP_PCI_AD<31..0> = NC_PCI_AD<31..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_C_BE_L<3..0> = NC_PCI_C_BE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE

TP_PCI_PAR = NC_PCI_PAR MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_RESET_L = NC_PCI_RESET_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCIE_CLK100M_XDPP = NC_PCIE_CLK100M_XDPP MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCIE_CLK100M_XDPN = NC_PCIE_CLK100M_XDPN MAKE_BASE=TRUE NO_TEST=TRUE
TP_DMI_CLK100M_LAP = NC_DMI_CLK100M_LAP MAKE_BASE=TRUE NO_TEST=TRUE
TP_DMI_CLK100M_LAN = NC_DMI_CLK100M_LAN MAKE_BASE=TRUE NO_TEST=TRUE
TP_LPC_DREQ1_L = NC_LPC_DREQ1_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_LPC_DREQ0_L = NC_LPC_DREQ0_L MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED NAND ALIASES

TP_NV_CE_L<3..0> = NC_NV_CE_L<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_NV_DQS<1..0> = NC_NV_DQS<1..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_NV_DQ<15..0> = NC_NV_DQ<15..0> MAKE_BASE=TRUE NO_TEST=TRUE

TP_NV_RB_L = NC_NV_RB_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_NV_WR_RE_L<1..0> = NC_NV_WR_RE_L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_NV_WE_CK_L<1..0> = NC_NV_WE_CK_L<1..0> MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

TP_JTAG_XDP_TRST_L = NC_JTAG_XDP_TRST_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCH_PWM0 = NC_PCH_PWM0 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCH_PWM1 = NC_PCH_PWM1 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCH_PWM2 = NC_PCH_PWM2 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCH_PWM3 = NC_PCH_PWM3 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCH_SST = NC_PCH_SST MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

TP_MEM_A_CS_L<7..4> = NC_MEM_A_CS_L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE
TP_MEM_A_DQ_CB<7..0> = NC_MEM_A_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_MEM_A_DQS_N<8> = NC_MEM_A_DQS_N<8> MAKE_BASE=TRUE NO_TEST=TRUE
TP_MEM_A_DQS_P<8> = NC_MEM_A_DQS_P<8> MAKE_BASE=TRUE NO_TEST=TRUE
TP_MEM_B_CS_L<7..4> = NC_MEM_B_CS_L<7..4> MAKE_BASE=TRUE NO_TEST=TRUE
TP_MEM_B_DQ_CB<7..0> = NC_MEM_B_DQ_CB<7..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_MEM_B_DQS_N<8> = NC_MEM_B_DQS_N<8> MAKE_BASE=TRUE NO_TEST=TRUE
TP_MEM_B_DQS_P<8> = NC_MEM_B_DQS_P<8> MAKE_BASE=TRUE NO_TEST=TRUE

TP_PCI_T28_D2R_N<3..0> = NC_PCI_T28_D2R_N<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_T28_D2R_P<3..0> = NC_PCI_T28_D2R_P<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_T28_R2D_C_N<3..0> = NC_PCI_T28_R2D_C_N<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCI_T28_R2D_C_P<3..0> = NC_PCI_T28_R2D_C_P<3..0> MAKE_BASE=TRUE NO_TEST=TRUE

TP_HDA_SDIN1 = NC_HDA_SDIN1 MAKE_BASE=TRUE NO_TEST=TRUE
TP_HDA_SDIN2 = NC_HDA_SDIN2 MAKE_BASE=TRUE NO_TEST=TRUE
TP_HDA_SDIN3 = NC_HDA_SDIN3 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCIE_CLK100M_PE5P = NC_PCIE_CLK100M_PE5P MAKE_BASE=TRUE NO_TEST=TRUE
TP_PCIE_CLK100M_PE5N = NC_PCIE_CLK100M_PE5N MAKE_BASE=TRUE NO_TEST=TRUE
TP_NV_RCOMP = NC_NV_RCOMP MAKE_BASE=TRUE NO_TEST=TRUE
PCIE_CLK100M_EXCARD_P = NC_PCIE_CLK100M_EXCARD_P MAKE_BASE=TRUE NO_TEST=TRUE
PCIE_CLK100M_EXCARD_N = NC_PCIE_CLK100M_EXCARD_N MAKE_BASE=TRUE NO_TEST=TRUE

TP_USB_7N = NC_USB_7N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_7P = NC_USB_7P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_6N = NC_USB_6N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_6P = NC_USB_6P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_1N = NC_USB_1N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_1P = NC_USB_1P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_3N = NC_USB_3N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_3P = NC_USB_3P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_5N = NC_USB_5N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_5P = NC_USB_5P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_9N = NC_USB_9N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_9P = NC_USB_9P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_10N = NC_USB_10N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_10P = NC_USB_10P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_11N = NC_USB_11N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_11P = NC_USB_11P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_12N = NC_USB_12N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_12P = NC_USB_12P MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_13N = NC_USB_13N MAKE_BASE=TRUE NO_TEST=TRUE
TP_USB_13P = NC_USB_13P MAKE_BASE=TRUE NO_TEST=TRUE

PCIE_EXCARD_D2R_P = NC_PCIE_EXCARD_D2R_P MAKE_BASE=TRUE NO_TEST=TRUE
PCIE_EXCARD_D2R_N = NC_PCIE_EXCARD_D2R_N MAKE_BASE=TRUE NO_TEST=TRUE
PCIE_EXCARD_R2D_C_P = NC_PCIE_EXCARD_R2D_C_P MAKE_BASE=TRUE NO_TEST=TRUE
PCIE_EXCARD_R2D_C_N = NC_PCIE_EXCARD_R2D_C_N MAKE_BASE=TRUE NO_TEST=TRUE
TP_SDVO_TVCLKINN = NC_SDVO_TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SDVO_TVCLKINP = NC_SDVO_TVCLKINP MAKE_BASE=TRUE NO_TEST=TRUE
TP_SDVO_STALLN = NC_SDVO_STALLN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SDVO_STALLP = NC_SDVO_STALLP MAKE_BASE=TRUE NO_TEST=TRUE
TP_SDVO_INTN = NC_SDVO_INTN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SDVO_INTP = NC_SDVO_INTP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

TP_SATA_D_D2RN = NC_SATA_D_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_D_D2RP = NC_SATA_D_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_D_R2D_CN = NC_SATA_D_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_D_R2D_CP = NC_SATA_D_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_E_D2RN = NC_SATA_E_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_E_D2RP = NC_SATA_E_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_E_R2D_CN = NC_SATA_E_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_E_R2D_CP = NC_SATA_E_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_F_D2RN = NC_SATA_F_D2RN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_F_D2RP = NC_SATA_F_D2RP MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_F_R2D_CN = NC_SATA_F_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE
TP_SATA_F_R2D_CP = NC_SATA_F_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

TP_CRT_IG_DDC_CLK = NC_CRT_IG_DDC_CLK MAKE_BASE=TRUE NO_TEST=TRUE
TP_CRT_IG_DDC_DATA = NC_CRT_IG_DDC_DATA MAKE_BASE=TRUE NO_TEST=TRUE
TP_CRT_IG_RED = NC_CRT_IG_RED MAKE_BASE=TRUE NO_TEST=TRUE
TP_CRT_IG_GREEN = NC_CRT_IG_GREEN MAKE_BASE=TRUE NO_TEST=TRUE
TP_CRT_IG_BLUE = NC_CRT_IG_BLUE MAKE_BASE=TRUE NO_TEST=TRUE
TP_CRT_IG_HSYNC = NC_CRT_IG_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE
TP_CRT_IG_VSYNC = NC_CRT_IG_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE

TP_DP_IG_B_MLN<3..0> = NC_DP_IG_B_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_B_MLP<3..0> = NC_DP_IG_B_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_B_AUX_N = NC_DP_IG_B_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_B_AUX_P = NC_DP_IG_B_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_B_HPD = NC_DP_IG_B_HPD MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_B_DDC_CLK = NC_DP_IG_B_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_B_DDC_DATA = NC_DP_IG_B_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

TP_DP_IG_C_MLN<3..0> = NC_DP_IG_C_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_C_MLP<3..0> = NC_DP_IG_C_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_C_AUX_N = NC_DP_IG_C_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_C_AUX_P = NC_DP_IG_C_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_C_HPD = NC_DP_IG_C_HPD MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_C_CTRL_CLK = NC_DP_IG_C_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_C_CTRL_DATA = NC_DP_IG_C_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

TP_DP_IG_D_MLN<3..0> = NC_DP_IG_D_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_D_MLP<3..0> = NC_DP_IG_D_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_D_AUXN = NC_DP_IG_D_AUXN MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_D_AUXP = NC_DP_IG_D_AUXP MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_D_HPD = NC_DP_IG_D_HPD MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_D_CTRL_CLK = NC_DP_IG_D_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE
TP_DP_IG_D_CTRL_DATA = NC_DP_IG_D_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE

TP_GFX_VID<0..6> = NC_GFX_VID<0..6> MAKE_BASE=TRUE NO_TEST=TRUE
TP_GFX_VSENSE_N = NC_GFX_VSENSE_N MAKE_BASE=TRUE NO_TEST=TRUE
TP_GFX_VSENSE_P = NC_GFX_VSENSE_P MAKE_BASE=TRUE NO_TEST=TRUE

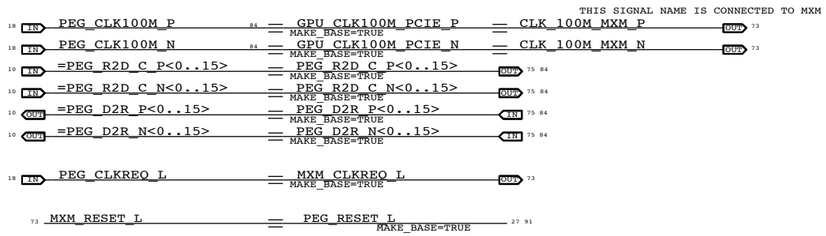
SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 8 OF 110
SHEET: 8 OF 92

PEG Slot Support



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

Signal Aliases

Apple Inc.

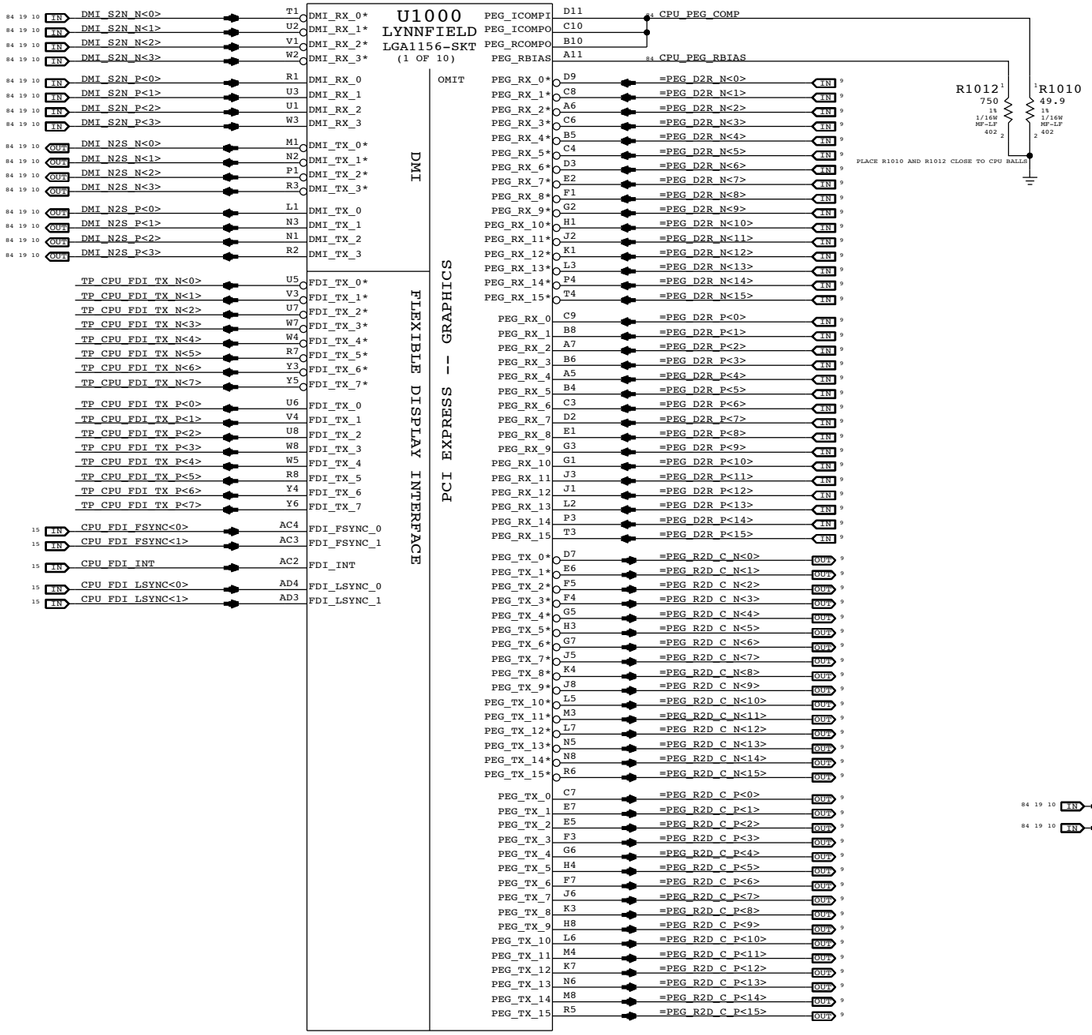
DRAWING NUMBER 051-8233 SIZE D

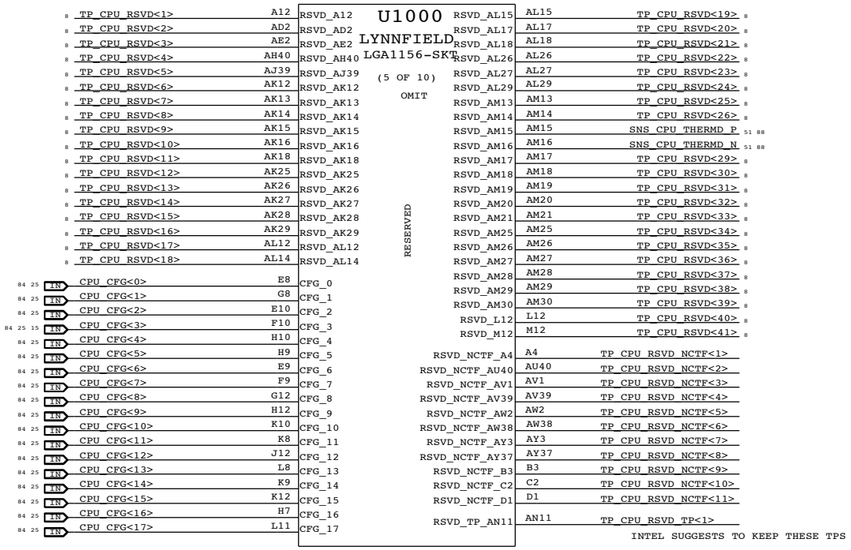
REVISION G.0.0

BRANCH

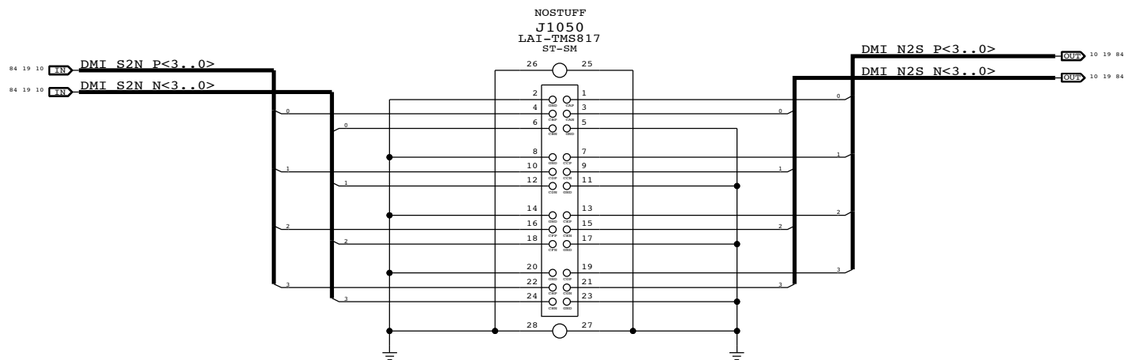
PAGE 9 OF 110

SHEET 9 OF 92

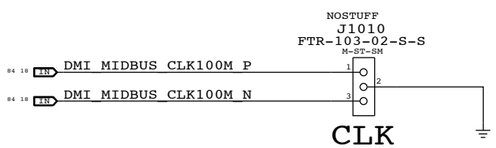




FOR LYNNFIELD PROCESSOR
CFG [1:0] :PCIE CONFIGURATION SELECT 11 = 1 X16 PCI EXPRESS 10 = 2 X8 PCI EXPRESS
FOR CLARKDALE PROCESSOR
CFG3 :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG4 :NOT USED ON DESKTOP



DMI MID-BUS PROBE

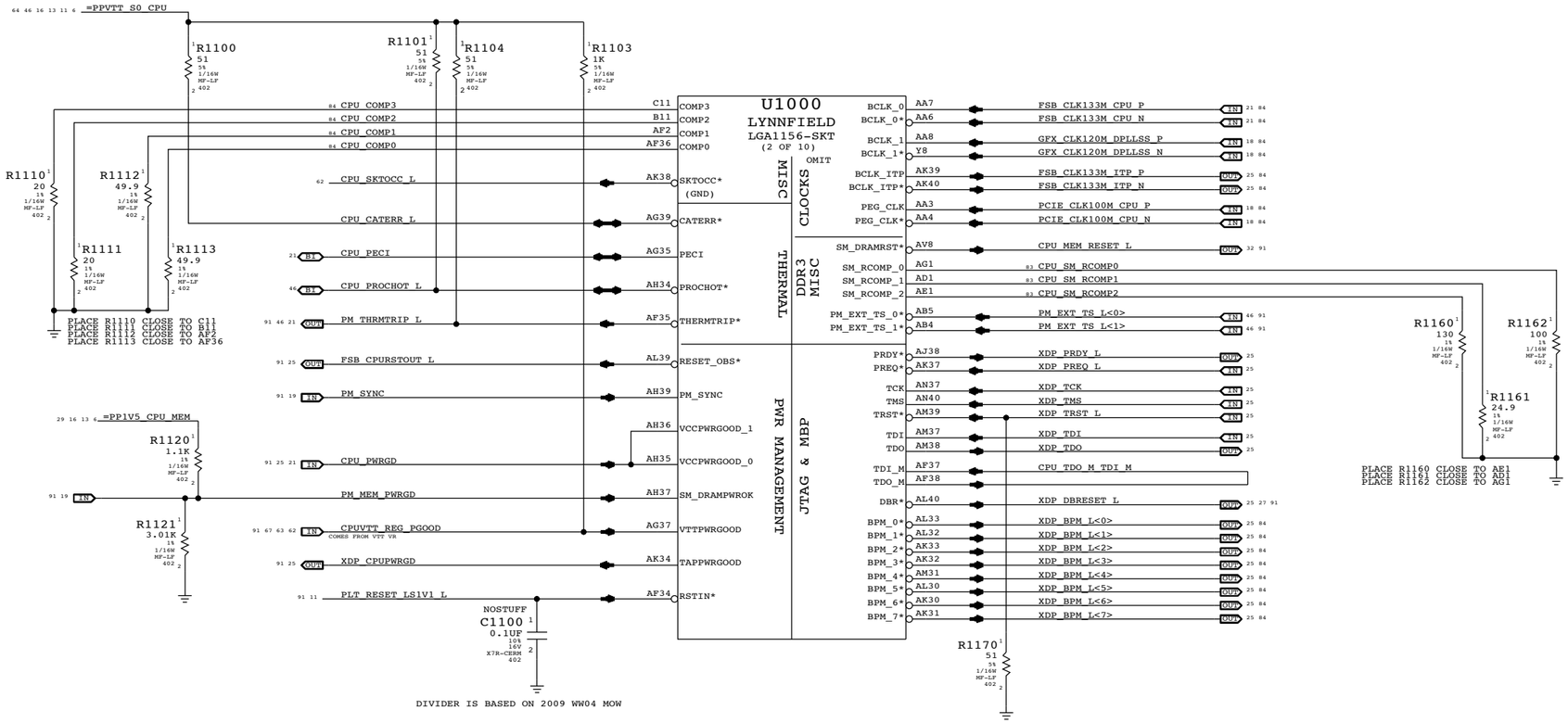


CLK

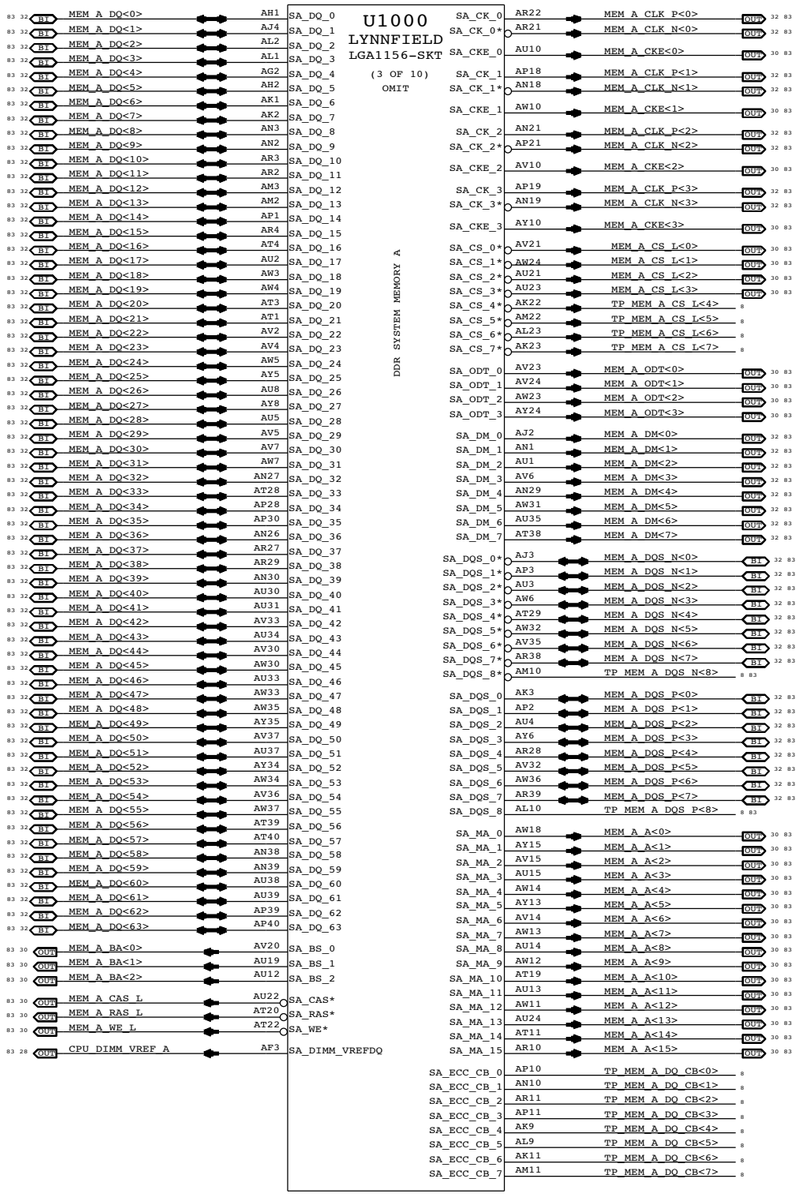
PAGE TITLE
CPU DMI/PEG/FDI/RSVD

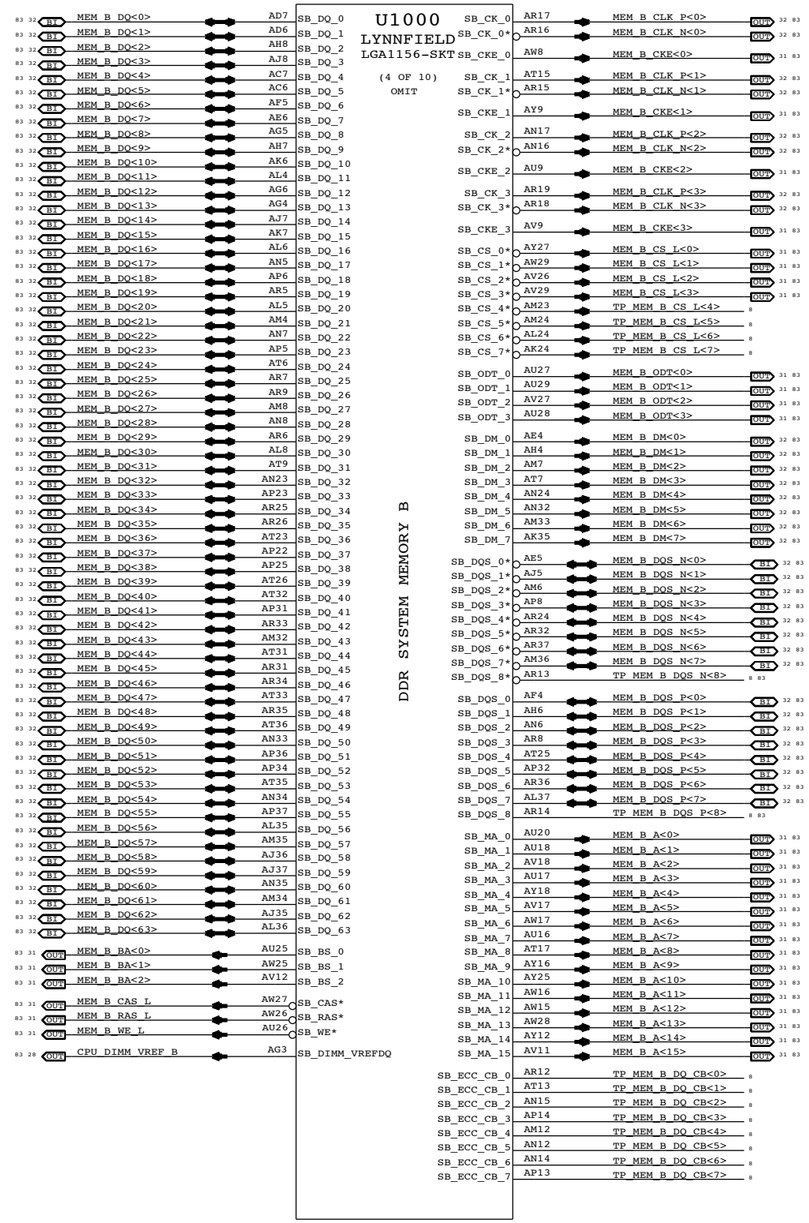
Apple Inc.

DRAWING NUMBER 051-8233
SIZE D
REVISION G.0.0
BRANCH
PAGE 10 OF 110
SHEET 10 OF 92



PAGE TITLE	CPU CLOCK/MISC/JTAG
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION G.0.0
	BRANCH
	PAGE 11 OF 110
	SHEET 11 OF 92





SYNC_MASTER=K60 SIJI SYNC_DATE=07/01/2009

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 12 OF 110
SHEET 12 OF 92

=PPVCORE_S0_CPU 6 13 16

U1000
LYNNFIELD
LGA1156-SKT
(10 OF 10)
OMIT

VCC

J21	VCC_100	
J22	VCC_101	
J24	VCC_102	
J25	VCC_103	
J27	VCC_104	
J28	VCC_105	
J30	VCC_106	
J31	VCC_107	
J33	VCC_108	
J34	VCC_109	
J36	VCC_110	
J37	VCC_111	
J39	VCC_112	
J40	VCC_113	
K17	VCC_114	
K18	VCC_115	
K20	VCC_116	
K21	VCC_117	
K23	VCC_118	
K24	VCC_119	
K26	VCC_120	
K27	VCC_121	
K29	VCC_122	
K30	VCC_123	
K32	VCC_124	
K33	VCC_125	
K35	VCC_126	
K36	VCC_127	
K38	VCC_128	
K39	VCC_129	
L17	VCC_130	
L19	VCC_131	
L20	VCC_132	
L22	VCC_133	
L23	VCC_134	
L25	VCC_135	
L26	VCC_136	
L28	VCC_137	
L29	VCC_138	
L31	VCC_139	
L32	VCC_140	
L34	VCC_141	
L35	VCC_142	
L37	VCC_143	
L38	VCC_144	
L40	VCC_145	
M17	VCC_146	
M19	VCC_147	
M21	VCC_148	
M22	VCC_149	
M24	VCC_150	
M25	VCC_151	
M27	VCC_152	
M28	VCC_153	
M30	VCC_154	
M33	VCC_155	
M34	VCC_156	
M36	VCC_157	
M37	VCC_158	
M39	VCC_159	
M40	VCC_160	
N33	VCC_161	
N35	VCC_162	
N36	VCC_163	
N38	VCC_164	
N39	VCC_165	
P33	VCC_166	
P34	VCC_167	
P35	VCC_168	
P36	VCC_169	
P37	VCC_170	
P38	VCC_171	
P39	VCC_172	
P40	VCC_173	
R33	VCC_174	
R34	VCC_175	
R35	VCC_176	
R36	VCC_177	
R37	VCC_178	
R38	VCC_179	
R39	VCC_180	
R40	VCC_181	

NCTF

CGC_TP_NCTF	B39	TP_CPU_CGC_NCTF
VCC_NCTF_0	A38	=PPVCORE_S0_CPU 6 13 16
VCC_NCTF_1	C40	
FC_AE38	AE38	TP_CPU_FC_AE38 8
FC_AG40	AG40	TP_CPU_FC_AG40 8

16 13 6 =PPVCORE_S0_CPU

U1000
LYNNFIELD
LGA1156-SKT
(6 OF 10)
OMIT

CPU CORE SUPPLY POWER

A23	VCC_0		VTT_0	AA33	
A24	VCC_1		VTT_1	AA34	
A26	VCC_2		VTT_2	AA35	
A27	VCC_3		VTT_3	AA36	
A33	VCC_4		VTT_4	AA37	
A35	VCC_5		VTT_5	AA38	
A36	VCC_6		VTT_6	AB7	
B23	VCC_7		VTT_7	AC33	
B25	VCC_8		VTT_8	AC34	
B26	VCC_9		VTT_9	AC35	
B28	VCC_10		VTT_10	AC36	
B29	VCC_11		VTT_11	AC37	
B31	VCC_12		VTT_12	AC38	
B32	VCC_13		VTT_13	AC39	
B34	VCC_14		VTT_14	AC40	
B35	VCC_15		VTT_15	AC5	
B37	VCC_16		VTT_16	AC8	
B38	VCC_17		VTT_17	AD33	
C23	VCC_18		VTT_18	AD34	
C24	VCC_19		VTT_19	AD35	
C25	VCC_20		VTT_20	AD36	
C27	VCC_21		VTT_21	AD37	
C28	VCC_22		VTT_22	AD38	
C30	VCC_23		VTT_23	AD39	
C31	VCC_24		VTT_24	AD40	
C33	VCC_25		VTT_25	AE33	
C34	VCC_26		VTT_26	AE34	
C36	VCC_27		VTT_27	AE39	
C37	VCC_28		VTT_28	AE40	
C39	VCC_29		VTT_29	AE8	
D23	VCC_30		VTT_30	AF33	
D24	VCC_31		VTT_31	AG33	
D26	VCC_32		VTT_32	AJ17	
D27	VCC_33		VTT_33	AJ19	
D29	VCC_34		VTT_34	AJ21	
D30	VCC_35		VTT_35	AJ23	
D32	VCC_36		VTT_36	AJ25	
D33	VCC_37		VTT_37	AJ27	
D35	VCC_38		VTT_38	AJ29	
D36	VCC_39		VTT_39	AJ31	
D38	VCC_40		VTT_40	AJ32	
D39	VCC_41		VTT_41	AK19	
E22	VCC_42		VTT_42	AK20	
E23	VCC_43		VTT_43	AK21	
E25	VCC_44		VTT_44	AL20	
E26	VCC_45		VTT_45	AL21	
E28	VCC_46		VTT_46	L10	
E29	VCC_47		VTT_47	M10	
E31	VCC_48		VTT_48	M11	
E32	VCC_49		VTT_49	M9	
E34	VCC_50		VTT_50	N7	
E35	VCC_51		VTT_51	P6	
E37	VCC_52		VTT_52	P7	
E38	VCC_53		VTT_53	P8	
E40	VCC_54		VTT_54	T2	
F21	VCC_55		VTT_55	T6	
F22	VCC_56		VTT_56	T7	
F24	VCC_57		VTT_57	T8	
F25	VCC_58		VTT_58	V2	
F27	VCC_59		VTT_59	V33	
F28	VCC_60		VTT_60	V34	
F30	VCC_61		VTT_61	V35	
F31	VCC_62		VTT_62	V36	
F33	VCC_63		VTT_63	V37	
F34	VCC_64		VTT_64	V38	
F36	VCC_65		VTT_65	V39	
F37	VCC_66		VTT_66	V40	
F39	VCC_67		VTT_67	V6	
F40	VCC_68		VTT_68	V7	
G20	VCC_69		VTT_69	V8	
G21	VCC_70		VTT_70	W1	
G23	VCC_71		VTT_71	W6	
G24	VCC_72		VTT_72	Y33	
G26	VCC_73		VTT_73	Y34	
G27	VCC_74		VTT_74	Y35	
G29	VCC_75		VTT_75	Y36	
G30	VCC_76		VTT_76	Y37	
G32	VCC_77		VTT_77	Y38	
G33	VCC_78				
G35	VCC_79				
G36	VCC_80				
G38	VCC_81				
G39	VCC_82				
H19	VCC_83				
H20	VCC_84				
H22	VCC_85				
H23	VCC_86				
H25	VCC_87				
H26	VCC_88				
H28	VCC_89				
H29	VCC_90				
H31	VCC_91				
H32	VCC_92				
H34	VCC_93				
H35	VCC_94				
H37	VCC_95				
H38	VCC_96				
H40	VCC_97				
J18	VCC_98				
J19	VCC_99				

1.1V RAIL POWER

=PPVTT_S0_CPU 6 11 16 46 64
(Controlled by VTT_SELECT pin)

CPU VIDS

PSI*	AG38	CPU_PSI_L	OUT 16 64 89
VID_0/MSID_0	U40	CPU_VID<0>	OUT 16 64 89
VID_1/MSID_1	U39	CPU_VID<1>	OUT 16 64 89
VID_2/MSID_2	U38	CPU_VID<2>	OUT 16 64 89
VID_3/CSC_0	U37	CPU_VID<3>	OUT 16 64 89
VID_4/CSC_1	U36	CPU_VID<4>	OUT 16 64 89
VID_5/CSC_2	U35	CPU_VID<5>	OUT 16 64 89
VID_6	U34	CPU_VID<6>	OUT 16 64 89
VID_7	U33	CPU_VID<7>	OUT 16 64 89
VTT_SELECT	AF39	TP_CPU_VTTSELECT	

SENSE LINES

ISENSE	T40	VR_CPU_IOUT (CONNECTED TO THE IMON OUT FROM CPU REG)	IN 64 88
VCC_SENSE	T35	CPU_VCC_PKG_SENSE_P	OUT 49 64 89
VSS_SENSE	T34	CPU_VCC_PKG_SENSE_N	OUT 64 89
VTT_SENSE	AE35	CPU_VTTSENSE_P	OUT 49 67 89
VSS_SENSE_VTT	AE36	CPU_VTTSENSE_N	OUT 67 89

17 6 =PPVAXG_S0_CPU
THIS SUPPLY IS NEEDED ONLY FOR SYSTEM WITH DALE IG

U1000
LYNNFIELD
LGA1156-SKT
(7 OF 10)
OMIT

GRAPHICS POWER

A14	VAXG_0	
A15	VAXG_1	
A17	VAXG_2	
A18	VAXG_3	
B14	VAXG_4	
B15	VAXG_5	
B17	VAXG_6	
B18	VAXG_7	
C14	VAXG_8	
C15	VAXG_9	
C17	VAXG_10	
C18	VAXG_11	
C20	VAXG_12	
C21	VAXG_13	
D14	VAXG_14	
D15	VAXG_15	
D17	VAXG_16	
D18	VAXG_17	
D20	VAXG_18	
D21	VAXG_19	
E14	VAXG_20	
E15	VAXG_21	
E17	VAXG_22	
E18	VAXG_23	
E20	VAXG_24	
F14	VAXG_25	
F15	VAXG_26	
F17	VAXG_27	
F18	VAXG_28	
F19	VAXG_29	
G14	VAXG_30	
G15	VAXG_31	
G17	VAXG_32	
G18	VAXG_33	
H14	VAXG_34	
H15	VAXG_35	
H17	VAXG_36	
J14	VAXG_37	
J15	VAXG_38	
J16	VAXG_39	
K14	VAXG_40	
K15	VAXG_41	
K16	VAXG_42	
L14	VAXG_43	
L15	VAXG_44	
L16	VAXG_45	
M14	VAXG_46	
M15	VAXG_47	
M16	VAXG_48	

SENSE LINES

VSSAXG_SENSE	B13	TP_GFX_VSENSE_N 8
VAXG_SENSE	A13	TP_GFX_VSENSE_P 8

GRAPHICS VIDS

GFX_VID_0	G10	TP_GFX_VID<0> 8
GFX_VID_1	B12	TP_GFX_VID<1> 8
GFX_VID_2	E12	TP_GFX_VID<2> 8
GFX_VID_3	E11	TP_GFX_VID<3> 8
GFX_VID_4	C12	TP_GFX_VID<4> 8
GFX_VID_5	G11	TP_GFX_VID<5> 8
GFX_VID_6	J11	TP_GFX_VID<6> 8
GFX_VR_EN	F12	TP_GFX_VR_EN
GFX_DPRSLPVR	J10	TP_GFX_DPRSLPVR
GFX_IMON	F6	

=PP1V5_CPU_MEM 6 11 16 29

DDR3-1.5V RAILS

VDDQ_0	AJ11	
VDDQ_1	AJ13	
VDDQ_2	AJ15	
VDDQ_3	AT10	
VDDQ_4	AT18	
VDDQ_5	AT21	
VDDQ_6	AU11	
VDDQ_7	AV13	
VDDQ_8	AV16	
VDDQ_9	AV19	
VDDQ_10	AV22	
VDDQ_11	AV25	
VDDQ_12	AV28	
VDDQ_13	AW9	
VDDQ_14	AY11	
VDDQ_15	AY14	
VDDQ_16	AY17	
VDDQ_17	AY23	
VDDQ_18	AY26	

=PP1V8_S0_CPU_PLL 6 16 63

1.8V

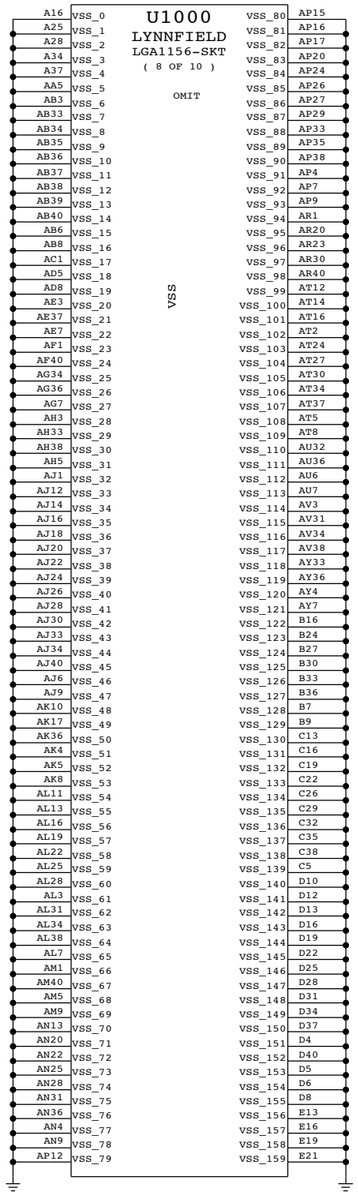
VCCPLL_0	AF7	
VCCPLL_1	AF8	
VCCPLL_2	AG8	

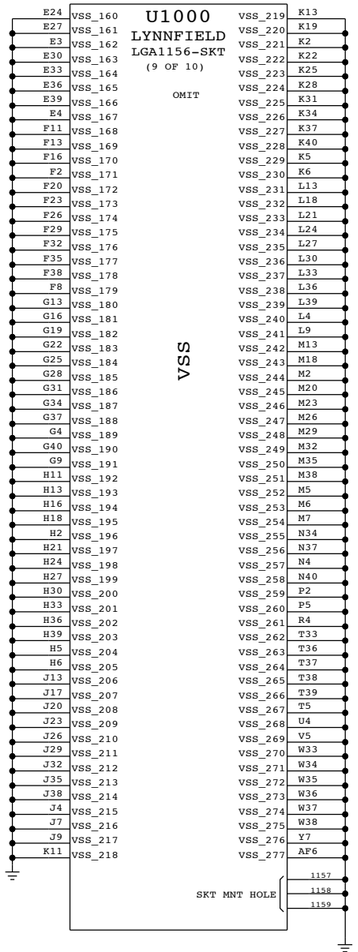
SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
CPU POWER

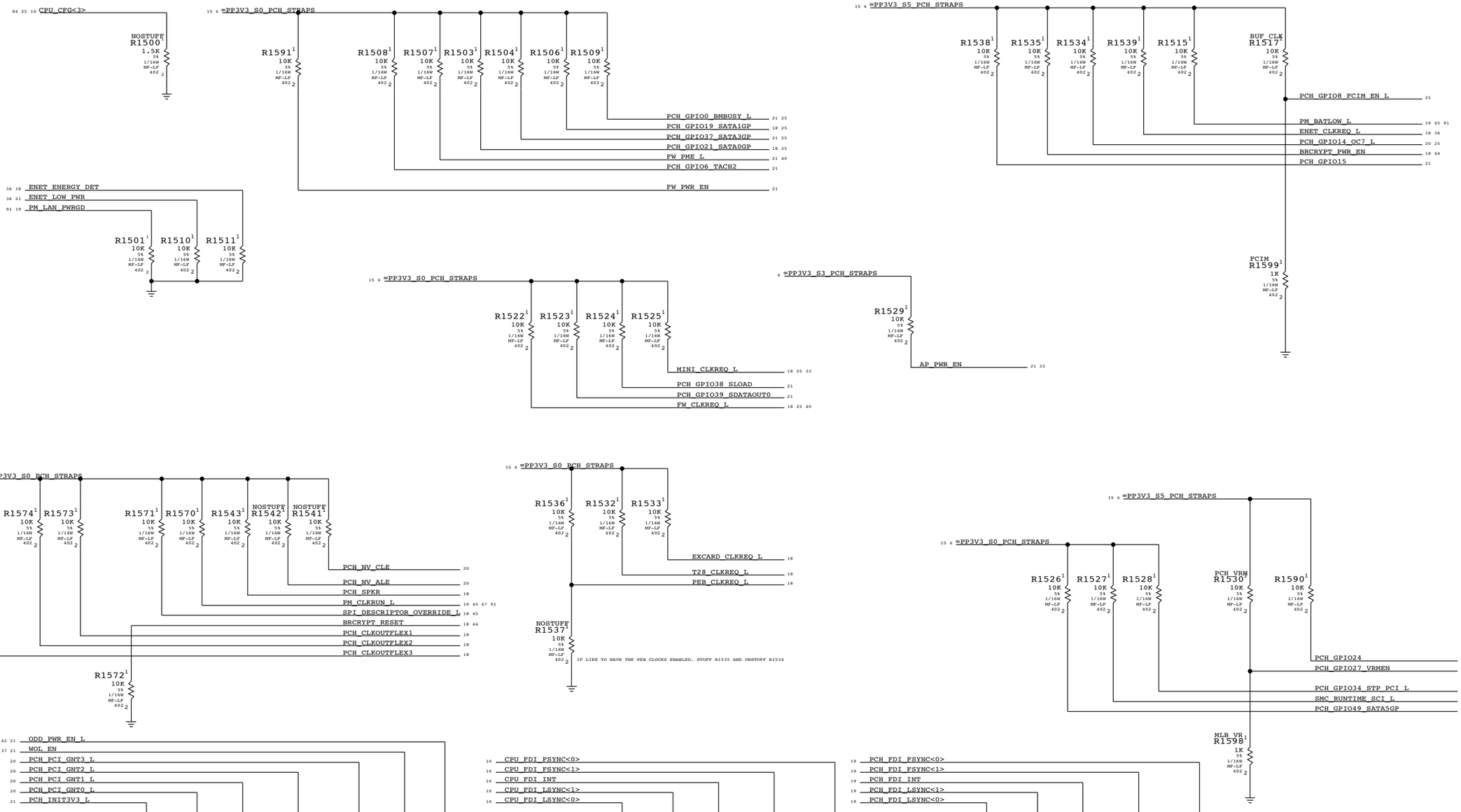
Apple Inc.

DRAWING NUMBER 051-8233
SIZE D
REVISION G.0.0
BRANCH
PAGE 13 OF 110
SHEET 13 OF 92



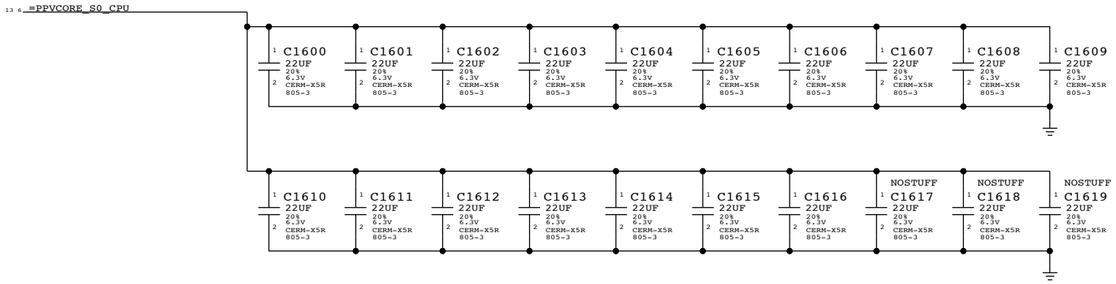


PAGE TITLE	CPU GROUNDS
	Apple Inc.
DRAWING NUMBER	051-8233
SIZE	D
REVISION	G.0.0
BRANCH	
PAGE	14 OF 110
SHEET	14 OF 92



CPU VCORE DECOUPLING

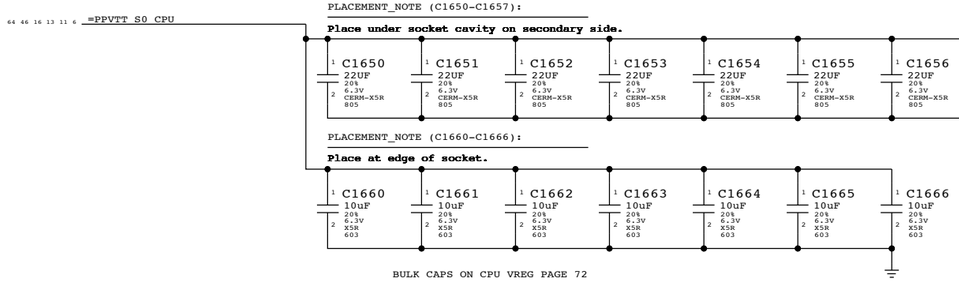
INTEL RECOMMENDATION 17X 22UF 0805



BULK CAPS ON CPU VREG PAGE 74

VTT (CPU Uncore) DECOUPLING

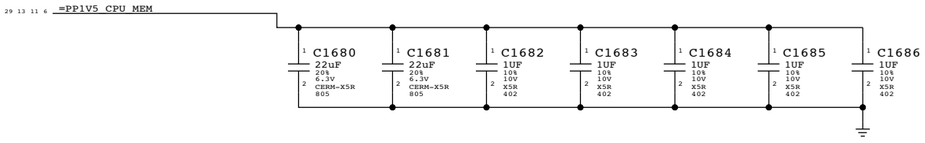
8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805



BULK CAPS ON CPU VREG PAGE 72

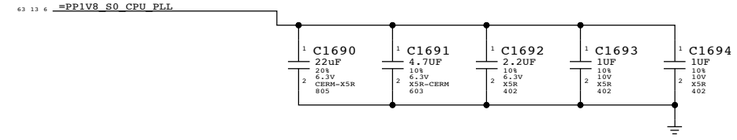
Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402



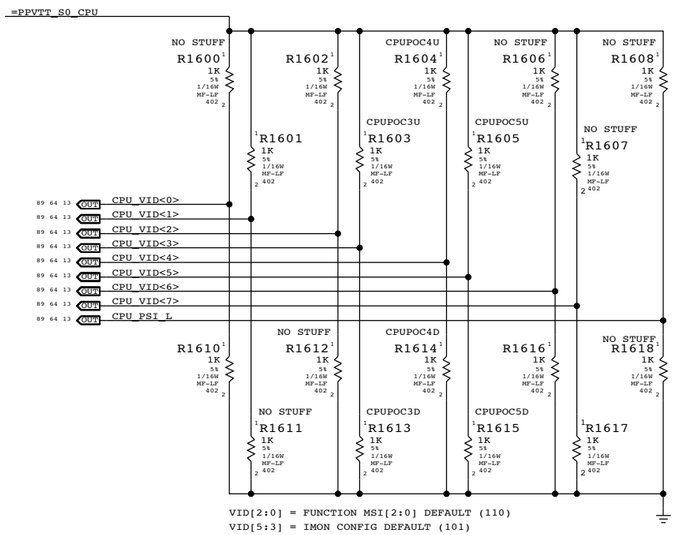
PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402



CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout



VID[2:0] = FUNCTION MSI[2:0] DEFAULT (110)
VID[5:3] = IMON CONFIG DEFAULT (101)
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)
PSI# = Reserved (0)

MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 16 OF 110
SHEET 16 OF 92

13 6 =PPVAXG_S0_CPU

Grounding the Rail because Integrated Graphics wont be used

R1700
0
5%
1/16W
MF-LF
402

6 =PP3V3_S0_PCH_VCCADAC

69 mA

R1750
0
5%
1/16W
MF-LF
402

PP3V3_S0_PCH_VCCA_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

69 mA

22 89

6 =PP1V05_S0_PCH_VCCADPLL

150 MA

R1760
0
5%
1/16W
MF-LF
402

PP1V05_S0_PCH_VCCADPLLA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

75 MA

22 89

R1765
0
5%
1/16W
MF-LF
402

PP1V05_S0_PCH_VCCADPLLB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

75 MA

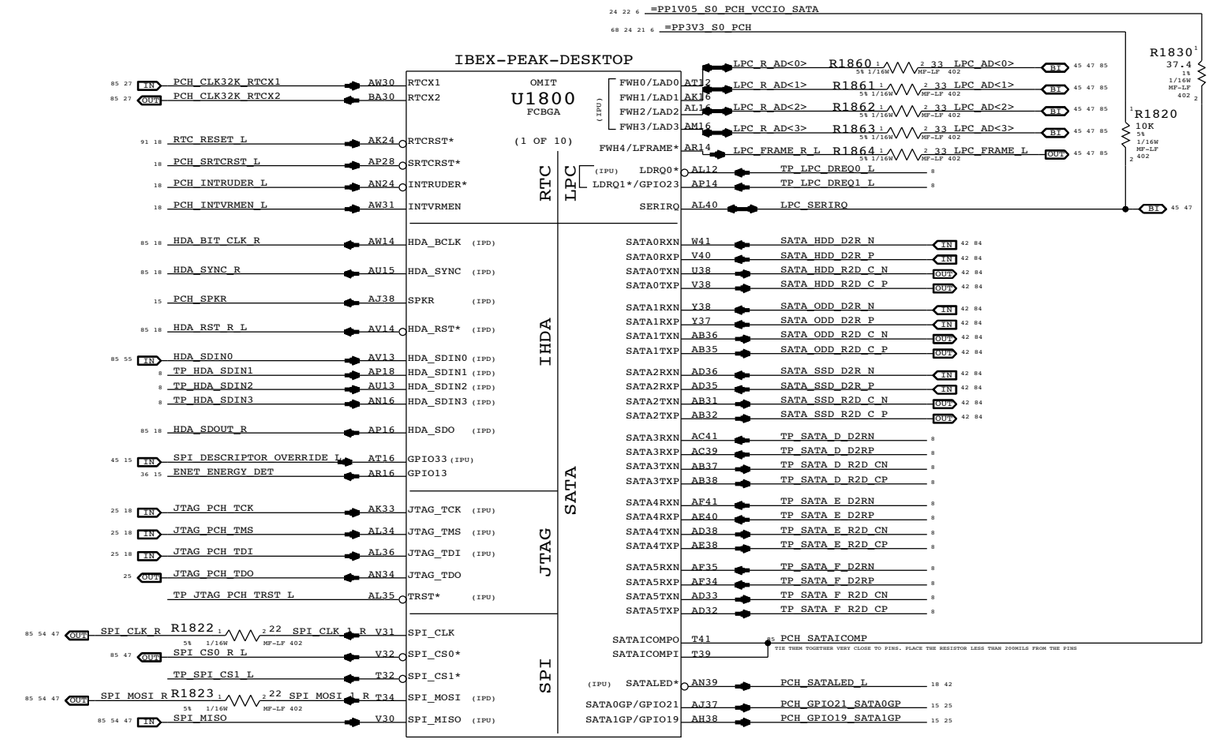
22 89

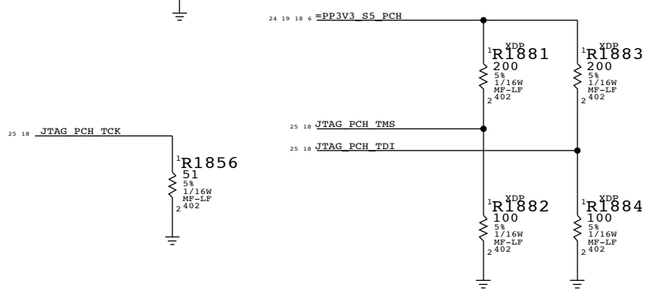
SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

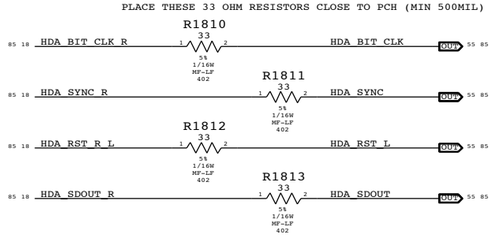
PAGE TITLE
CPU/PCH GFX DECOUPLING

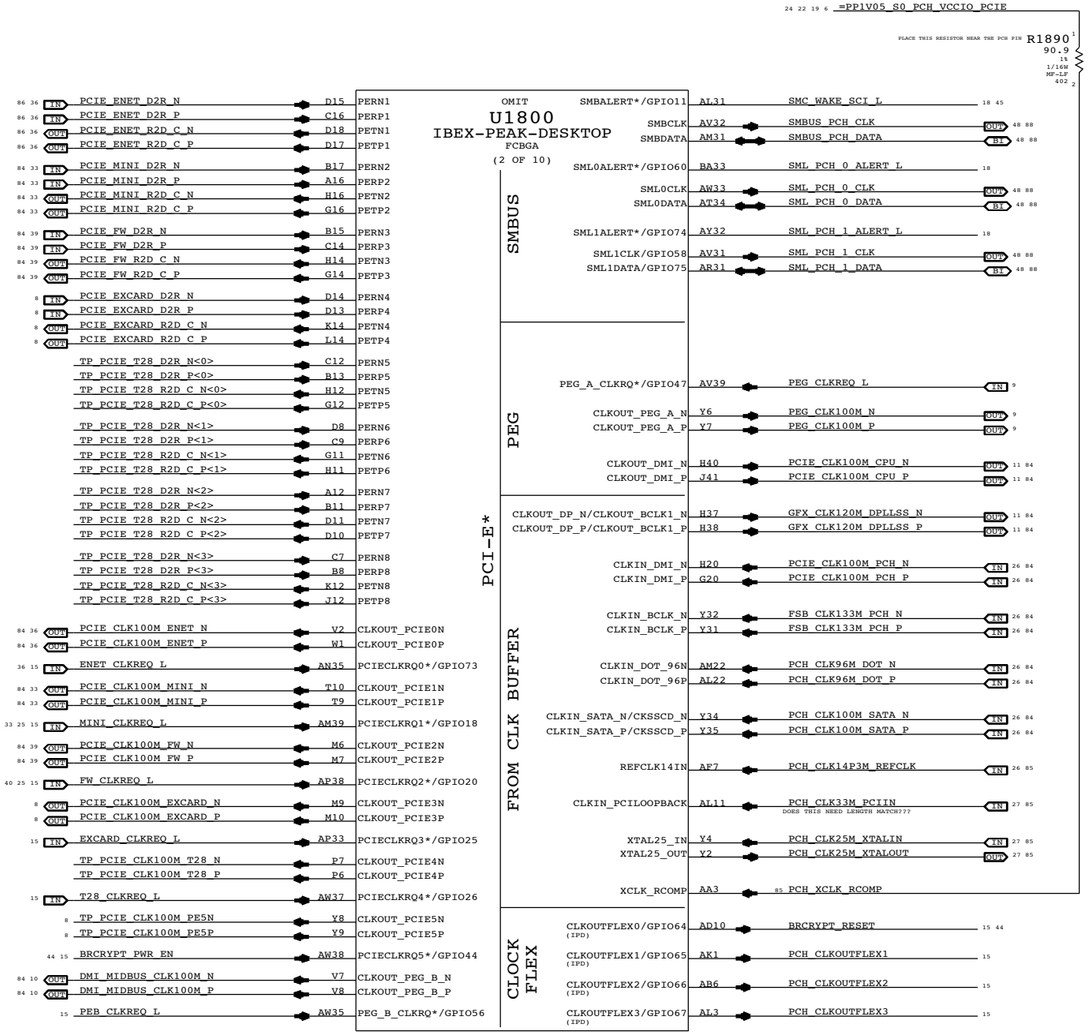
Apple Inc.

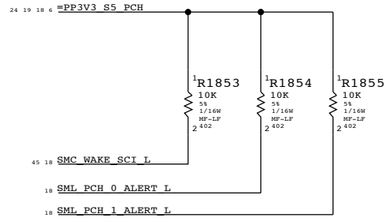
DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 17 OF 110
SHEET 17 OF 92









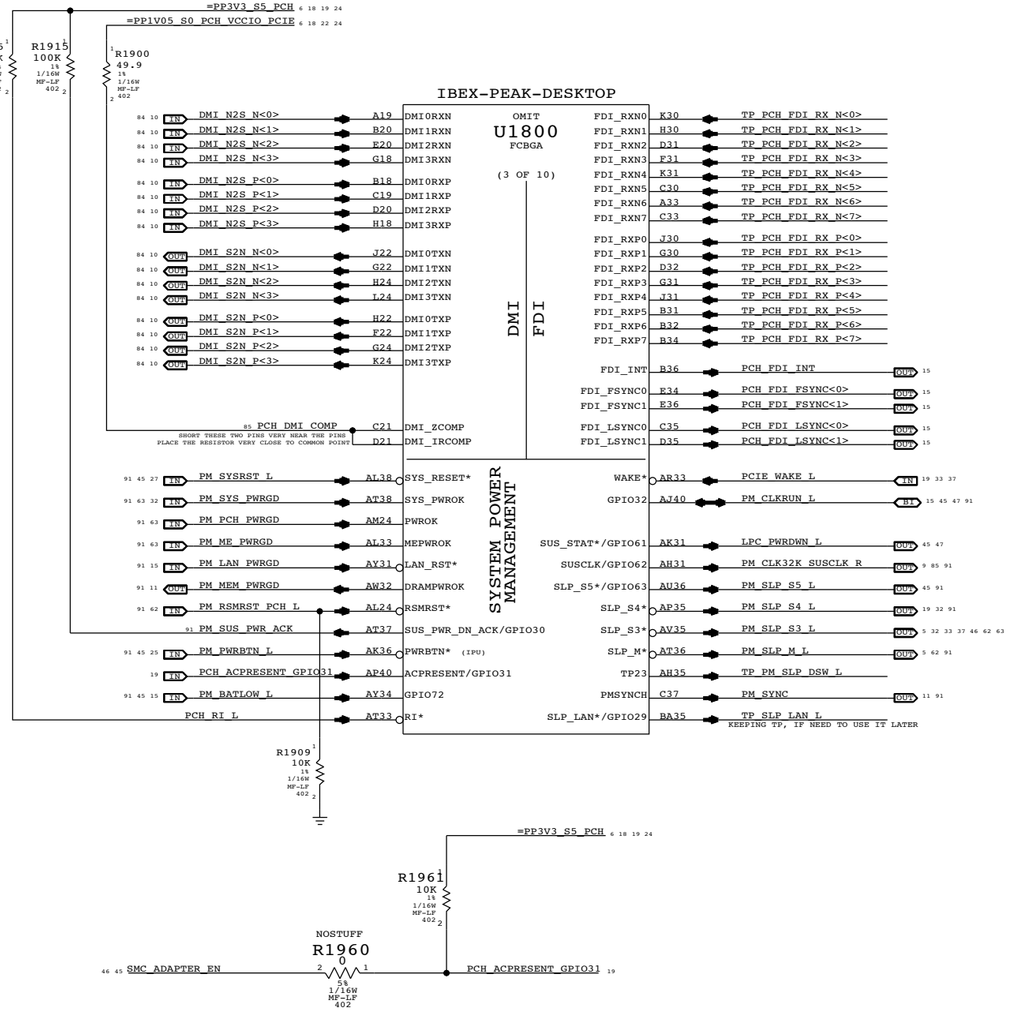


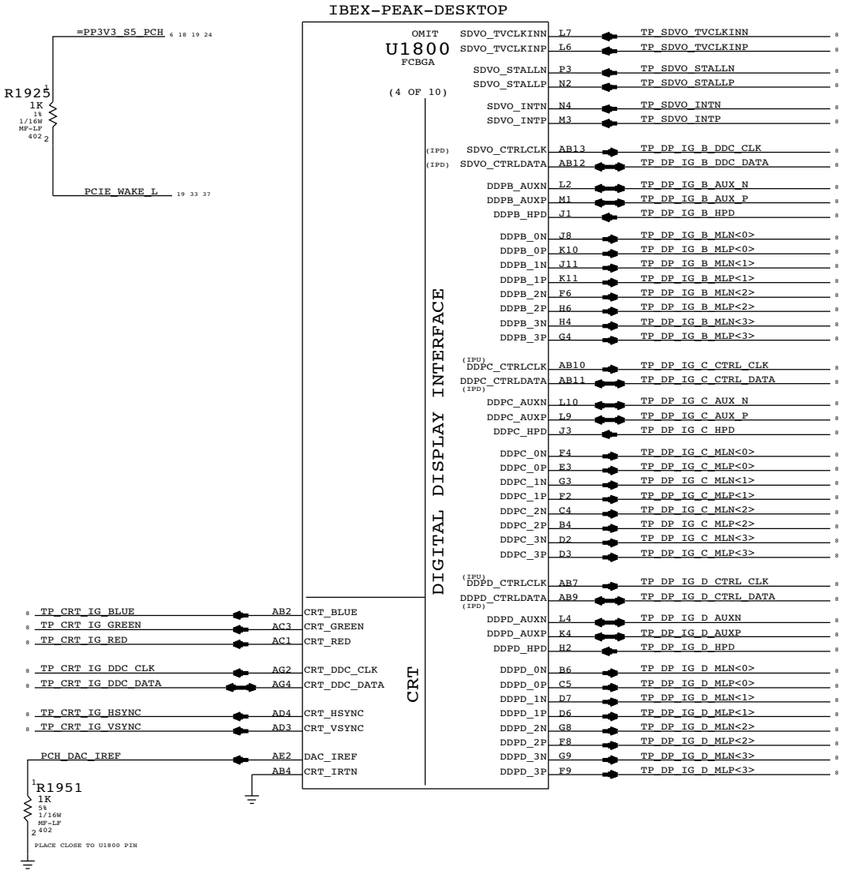
SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 18 OF 110
SHEET 18 OF 92

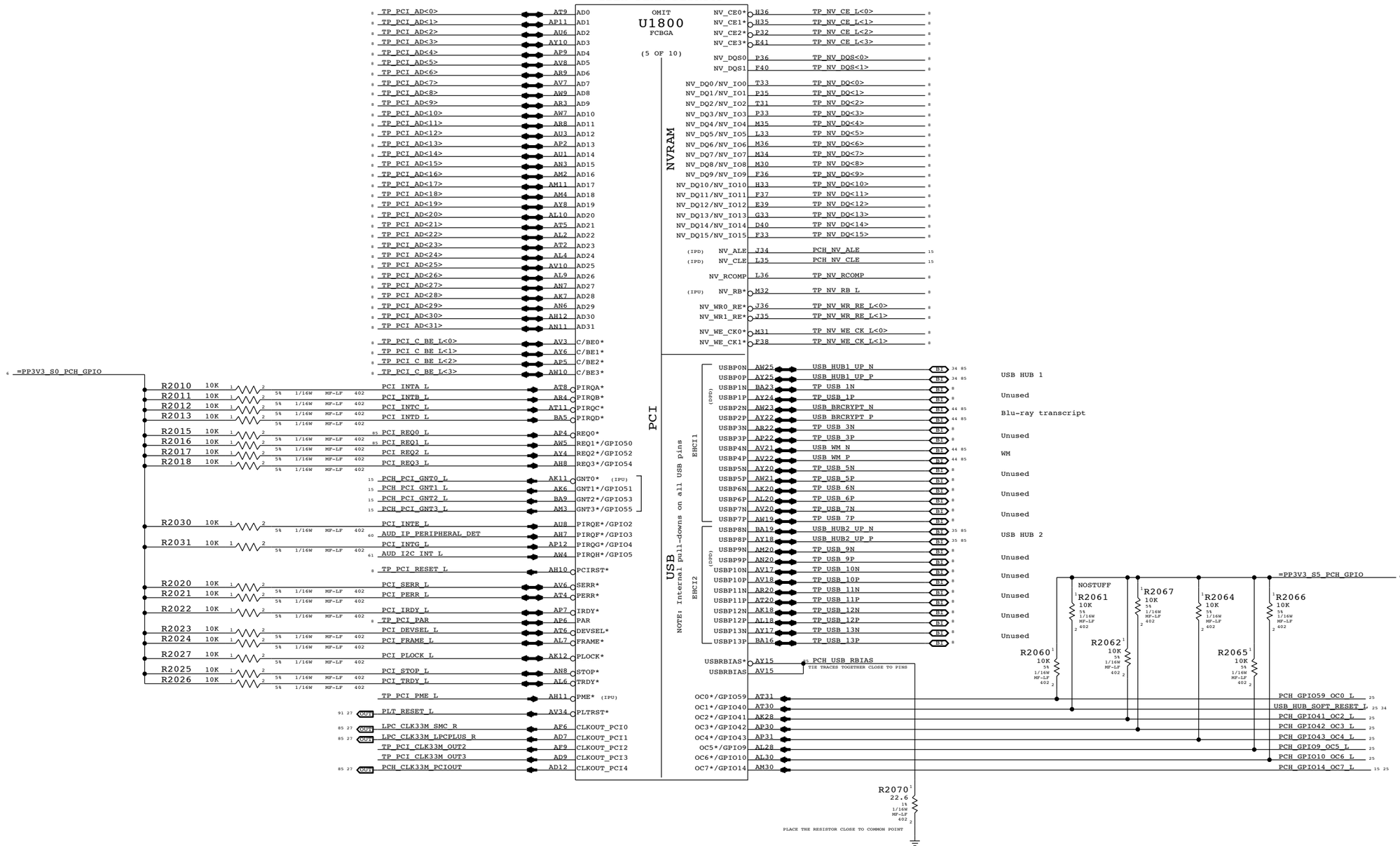




PAGE TITLE
PCH DMI/FDI/GRAPHICS

Apple Inc.

DRAWING NUMBER 051-8233
SIZE D
REVISION G.0.0
BRANCH
PAGE 19 OF 110
SHEET 19 OF 92



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 20 OF 110
SHEET 20 OF 92

IPU* = Only on TACH function.

=PP3V3_S0_PCH 68 24 21 18 6

R2190[1] 47K 5% 1/16W MF-LF 402 2

47 EN

=PP3V3_S0_PCH 6 18 21 24 68

R2150[1] 10K 5% 1/16W MF-LF 402 2

[1]R2155 10K 5% 1/16W MF-LF 402 2

U1800 IBEX-PEAK-DESKTOP FCBGA (6 OF 10) OMIT

25 15	PCH_GPIO0_BMBUSY_L	AK41	BMBUSY*/GPIO0		
40 15	FW_PME_L	AL14	TACH1/GPIO1 (IPU*)		
15 OUT	PCH_GPIO6_TACH2	AV11	TACH2/GPIO6 (IPU*)		
45 15 IN	SMC_RUNTIME_SCI_L	AY11	TACH3/GPIO7 (IPU*)		
15	PCH_GPIO8_FCIM_EN_L	AK30	GPIO8 (IPU)		
36 15	ENET_LOW_PWR	AU34	LAN_PHY_PWR_CTRL/GPIO12		
15	PCH_GPIO15	AY36	GPIO15 (IPD)		
61 25	AUD_IPHS_SWITCH_EN	AH39	SATA4GP/GPIO16		
	LPCPLUS_GPIO	AW11	TACH0/GPIO17 (IPU*)		
42 15	ODD_PWR_EN_L	AN41	SCLOCK/GPIO22		
15 IN	PCH_GPIO24	AR34	GPIO24		
15	PCH_GPIO27_VRMEN	AP37	GPIO27		
32 25 OUT	ISOLATE_CPU_MEM_L	AV40	GPIO28		
15	PCH_GPIO34_STP_PCI_L	AT40	STP_PCI*/GPIO34		
6	MXM_GOOD	AR41	GPIO35		
92 91 44 25	SDCARD_RESET	AK39	SATA2GP/GPIO36		
25 15	PCH_GPIO37_SATA3GP	AR38	SATA3GP/GPIO37		
15	PCH_GPIO38_SLOAD	AM38	SLOAD/GPIO38		
15	PCH_GPIO39_SDATAOUT0	AL39	SDATAOUT0/GPIO39		
37 15	WOL_EN	AV36	PCIECLKRQ6*/GPIO45		
33 15	AP_PWR_EN	AP36	PCIECLKRQ7*/GPIO46		
15	FW_PWR_EN	AG38	SDATAOUT1/GPIO48		
25 15	PCH_GPIO49_SATA5GP	AG40	SATA5GP/GPIO49		
85 47	SPIROM_USE_MLB	AL32	GPIO57		
				CLKOUT_PCIE6N	U4
				CLKOUT_PCIE6P	V4
				CLKOUT_PCIE7N	T7
				CLKOUT_PCIE7P	T6
				A20GATE	AG37
				CLKOUT_BCLK0_N/CLKOUT_PCIE8N	L38
				CLKOUT_BCLK0_P/CLKOUT_PCIE8P	K38
				PECI	D36
				RCIN*	AM40
				PROCPWRGD	B38
				THRMTRIP*	C38

MISC

CPU

GPIO

RSVD

NCTF

	TP_PCH_PWM0	BA12	PWM0
	TP_PCH_PWM1	AR12	PWM1
	TP_PCH_PWM2	AW12	PWM2
	TP_PCH_PWM3	AY13	PWM3
	TP_PCH_SST	AN31	SST

A40	VSS_NCTF0	
A5	VSS_NCTF1	
AW41	VSS_NCTF2	
AY2	VSS_NCTF3	
AY41	VSS_NCTF4	
B2	VSS_NCTF5	
B40	VSS_NCTF6	
B41	VSS_NCTF7	
BA1	VSS_NCTF8	
BA2	VSS_NCTF9	
C1	VSS_NCTF10	
C41	VSS_NCTF11	
E1	VSS_NCTF12	

	FSB_CLK133M_CPU_N	OUT	11 84
	FSB_CLK133M_CPU_P	OUT	11 84
	CPU_PECI	BI	11
	PCH_RCIN_L		
	CPU_PWRGD	OUT	11 25 91
	PM_THRMTRIP_L	IN	11 46 91

TP1	L18	TP_PCH_TP1	
TP2	K18	TP_PCH_TP2	
TP3	J20	TP_PCH_TP3	
TP4	P12	TP_PCH_TP4	
TP5	P13	TP_PCH_TP5	
TP6	T13	TP_PCH_TP6	
TP7	T12	TP_PCH_TP7	
TP8	V34	TP_PCH_TP8	
TP9	AT24	TP_PCH_TP9	
TP10	AR24	TP_PCH_TP10	
TP11	V20	TP_PCH_TP11	
TP12	P10	TP_PCH_TP12	
TP13	P9	TP_PCH_TP13	
TP20	AU39	TP_PCH_TP20	
TP21	AH30	TP_PCH_TP21	
TP22_NCTF0	A3		
TP22_NCTF1	A41		
TP22_NCTF2	AY1		
TP22_NCTF3	BA41		
TP18	AK35	TP_PCH_TP18	
TP19	AN36	TP_PCH_TP19	
NC0	AF15		
NC1	V10		
NC2	V11		
NC3	Y11		
NC4	Y12		

(IPD) INIT3_3V* AR39 PCH_INIT3V3_L 15

THIS SIGNAL IS INTEDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE: PCH MISC

Apple Inc.

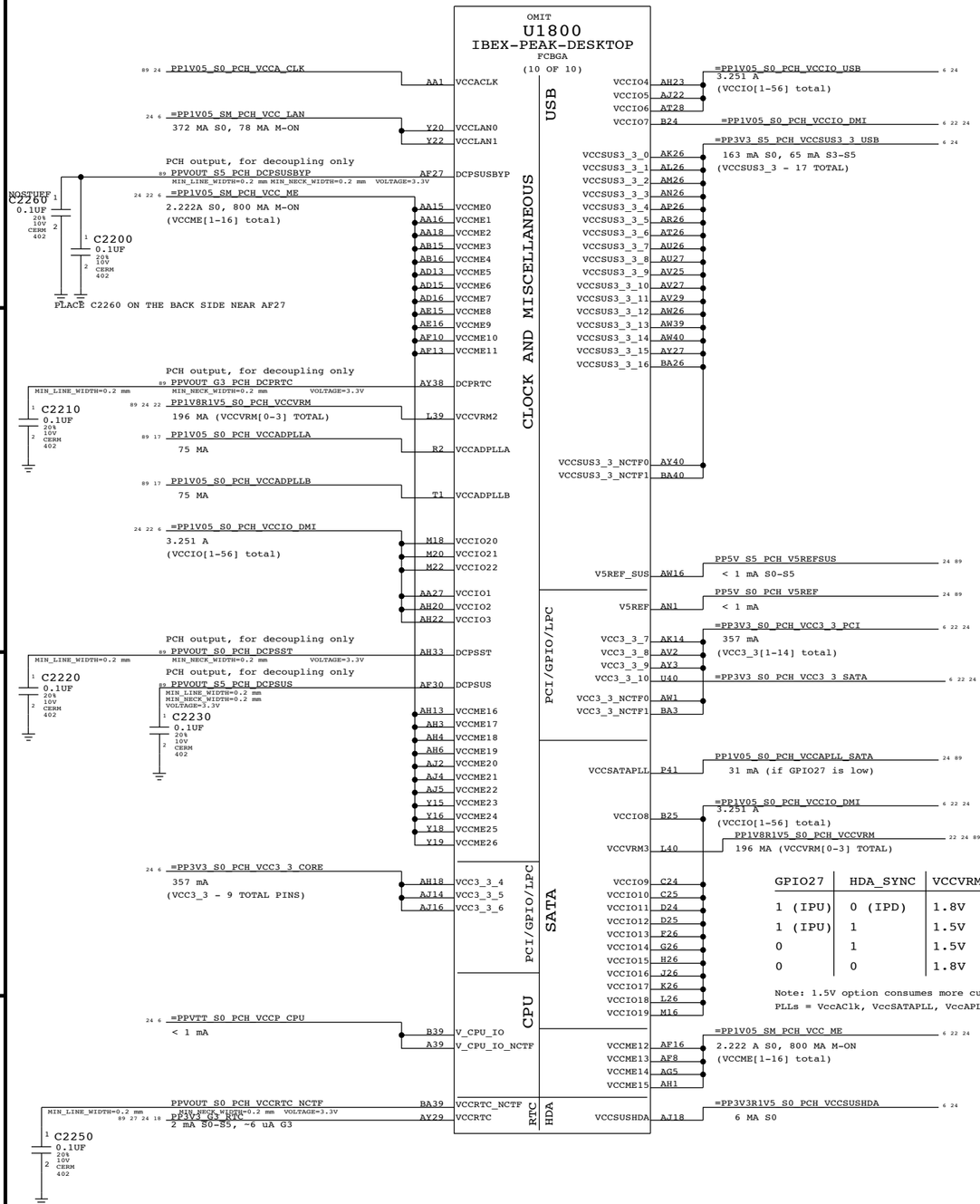
DRAWING NUMBER 051-8233 SIZE D

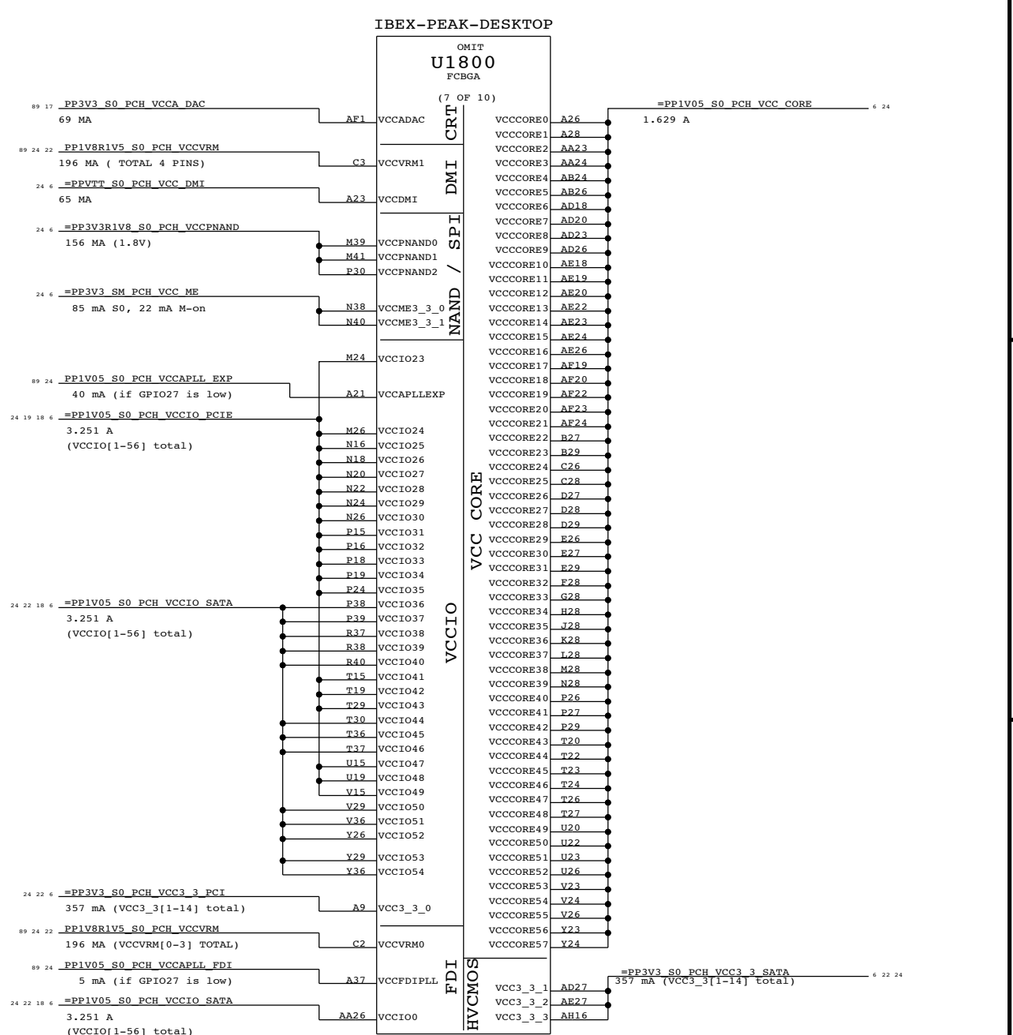
REVISION G.0.0

BRANCH

PAGE 21 OF 110

SHEET 21 OF 92

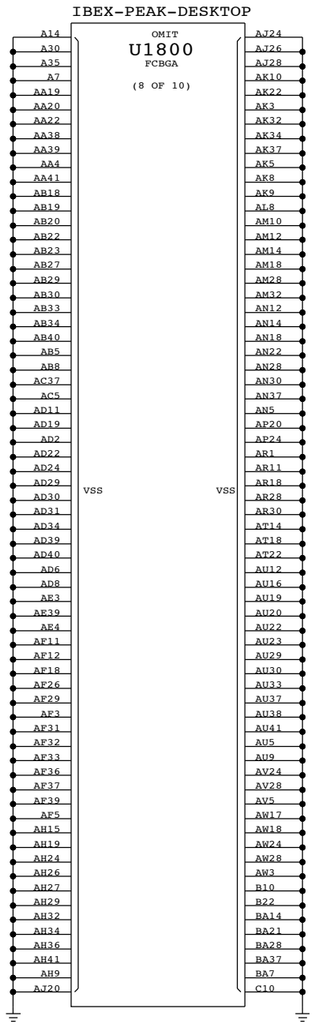


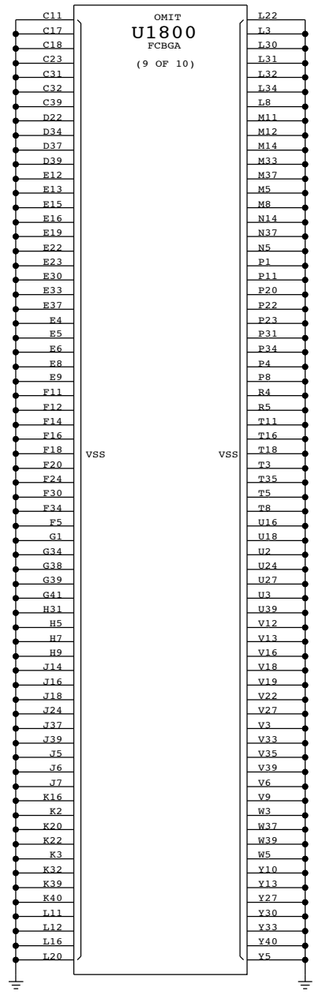


PAGE TITLE
PCH POWER

Apple Inc.

DRAWING NUMBER	SIZE
051-8233	D
REVISION	
G.0.0	
BRANCH	
PAGE	
22 OF 110	
SHEET	
22 OF 92	





SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE

PCH GROUNDS

Apple Inc.

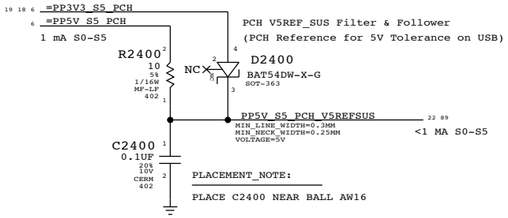
DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

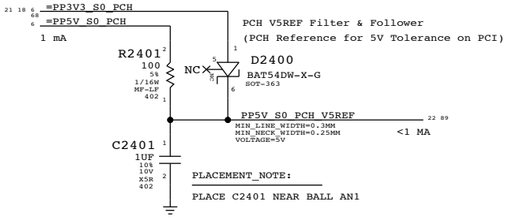
BRANCH

PAGE 23 OF 110

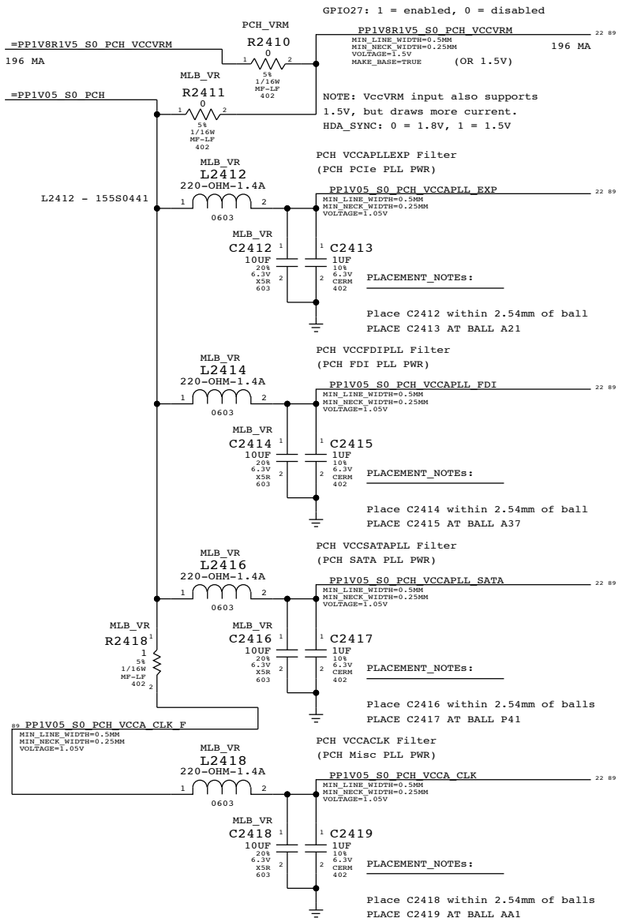
SHEET 23 OF 92



PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)

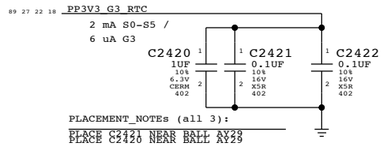


PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)

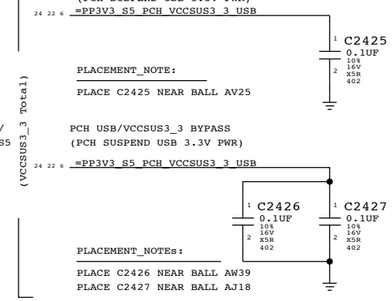


Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

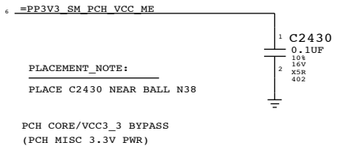
PCH VCCRTC BYPASS
(PCH RTC 3.3V PWR)



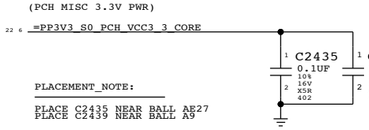
PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)



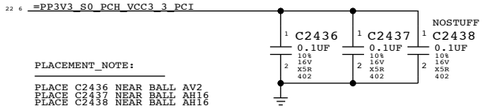
PCH VCCME3_3 BYPASS
(PCH ME 3.3V PWR)



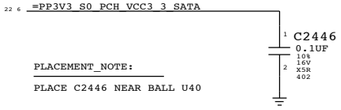
PCH CORE/VCC3_3 BYPASS
(PCH MISC 3.3V PWR)



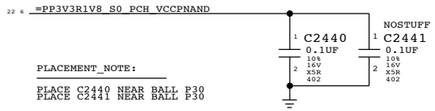
PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)



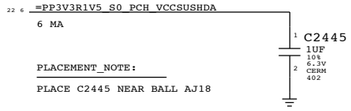
PCH VCC3_3 BYPASS
(PCH SATA 3.3V PWR)



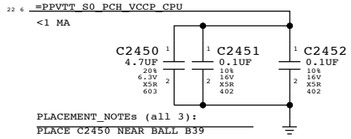
PCH VCCPNAND BYPASS
(PCH NAND 1.8V/3.3V PWR)



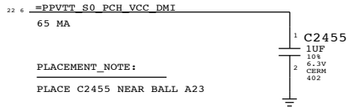
PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)



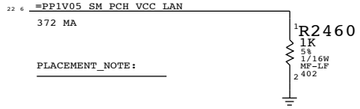
PCH V_CPU_IO BYPASS
(PCH 1.1V/1.05V CPU I/O PWR)



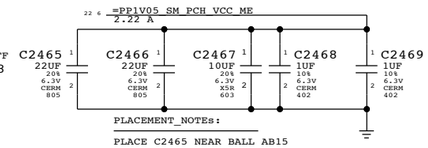
PCH VCCIO BYPASS
(PCH DMI 1.05V PWR)



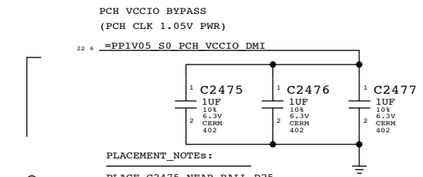
PCH VCCLAN BYPASS
(PCH 1.05V LAN Core PWR)



PCH VCCME BYPASS
(PCH 1.05V ME Core PWR)

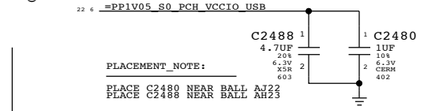


PCH VCCIO BYPASS
(PCH CLK 1.05V PWR)

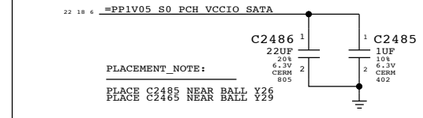


3.251 A S0 /
369 MA IDLE
(VCCIO TOTAL)

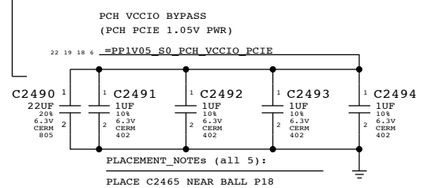
PCH VCCIO BYPASS
(PCH USB 1.05V PWR)



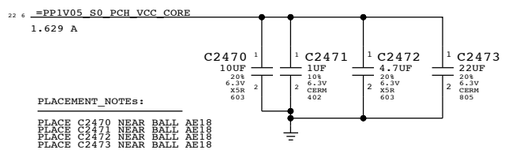
PCH VCCIO BYPASS
(PCH SATA 1.05V PWR)



PCH VCCIO BYPASS
(PCH PCIE 1.05V PWR)



PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)



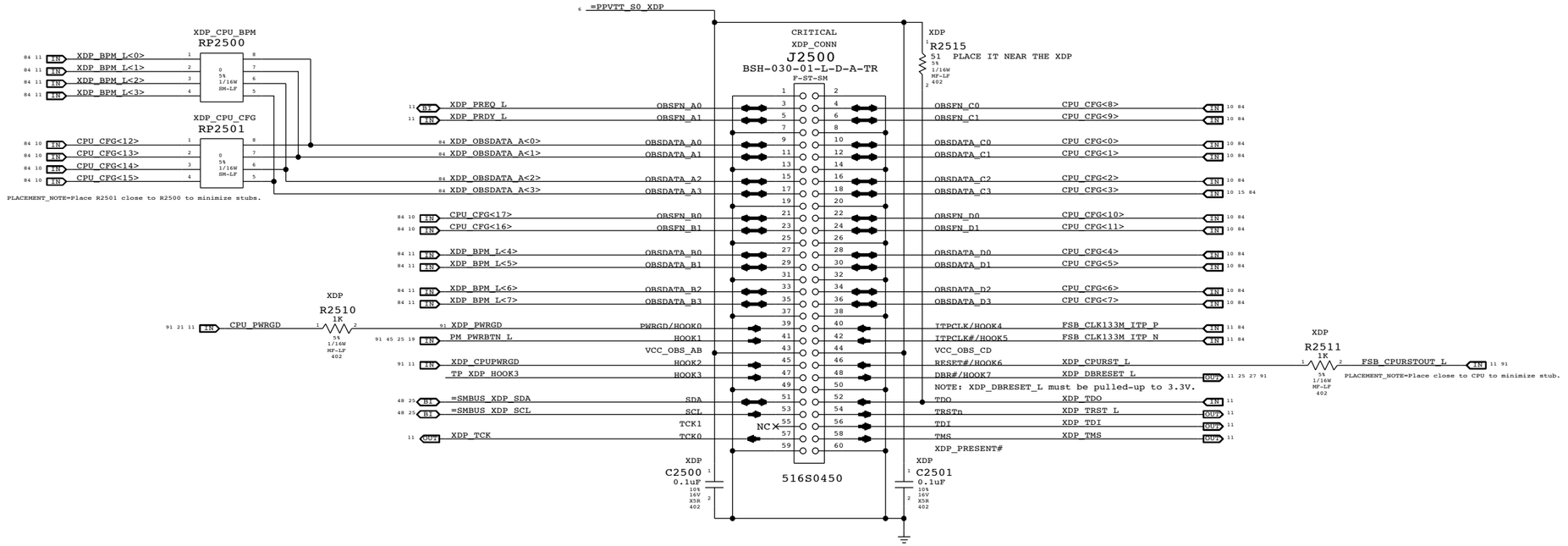
SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCH DECOUPLING

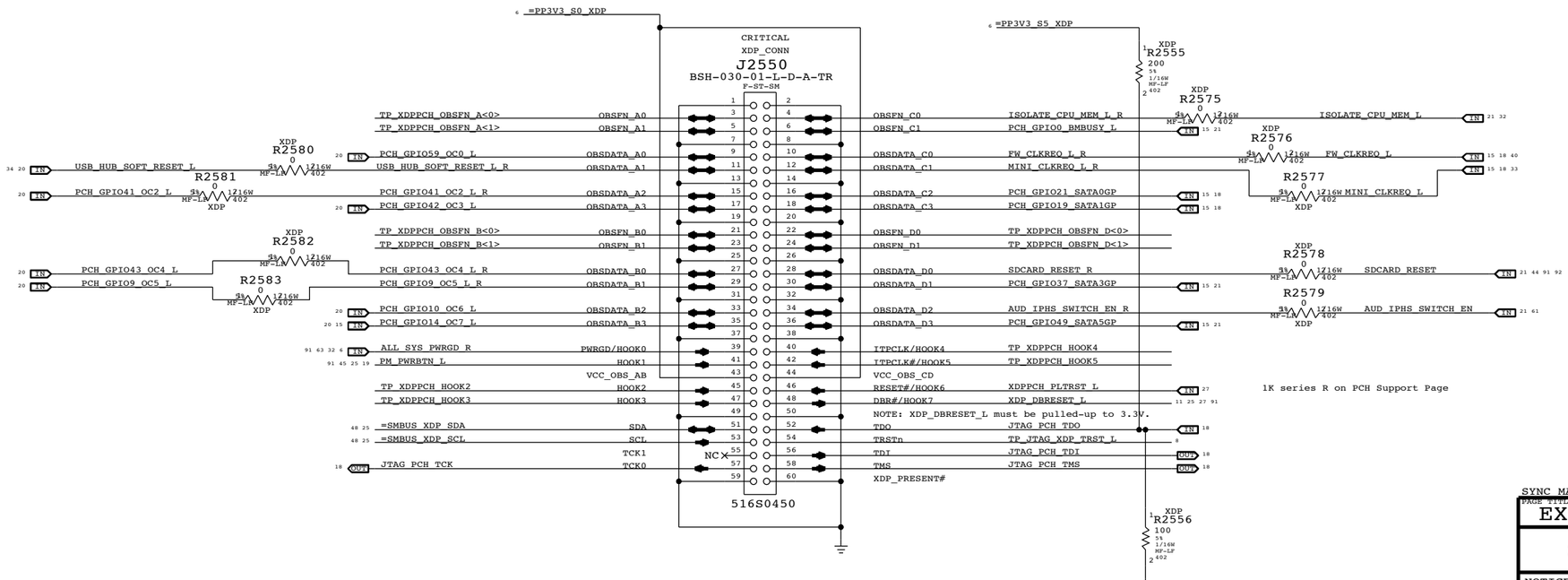
Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 24 OF 110
SHEET 24 OF 92

PROCESSOR XDP



PCH XDP



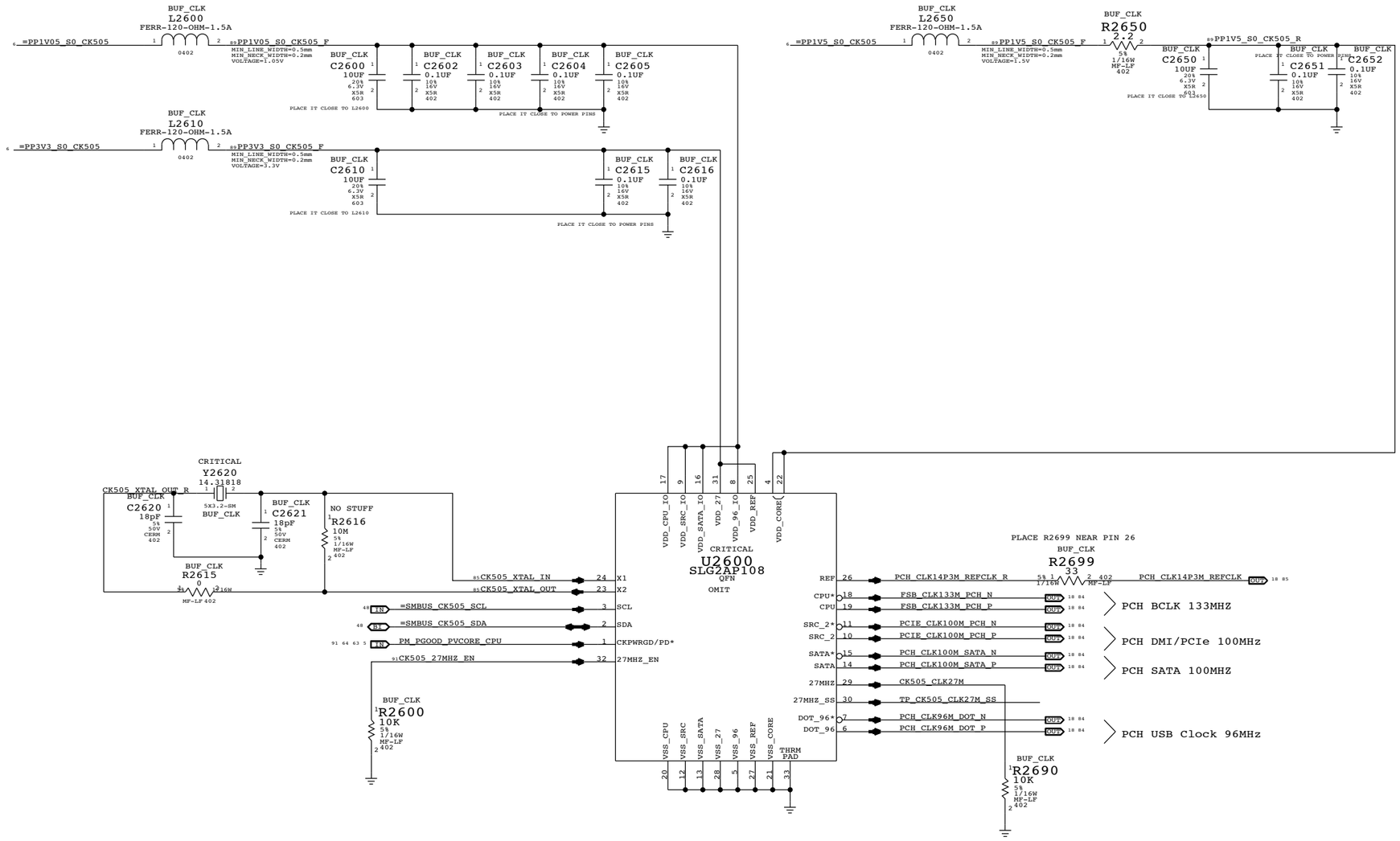
SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

EXTENDED DEBUG PORT(XDP)

Apple Inc.

DRAWING NUMBER	051-8233
SIZE	D
REVISION	G.0.0
BRANCH	
PAGE	25 OF 110
SHEET	25 OF 92



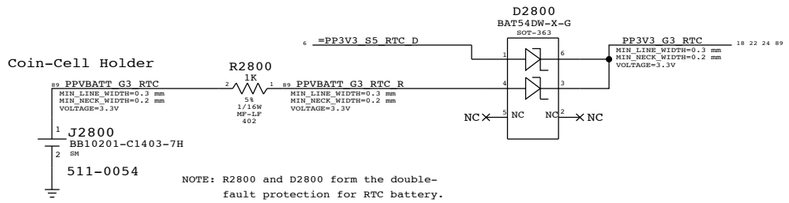
SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE
CLOCK (CK505)

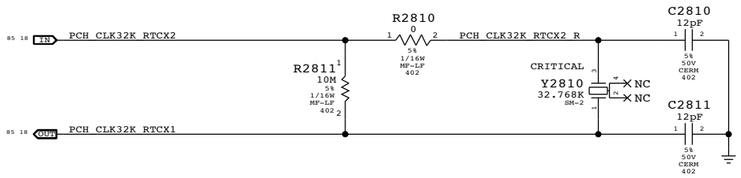
Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 26 OF 110
SHEET 26 OF 92

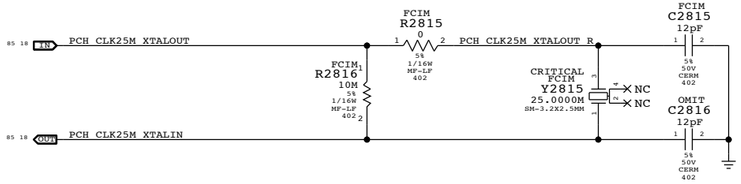
RTC Power Sources



PCH RTC Crystal

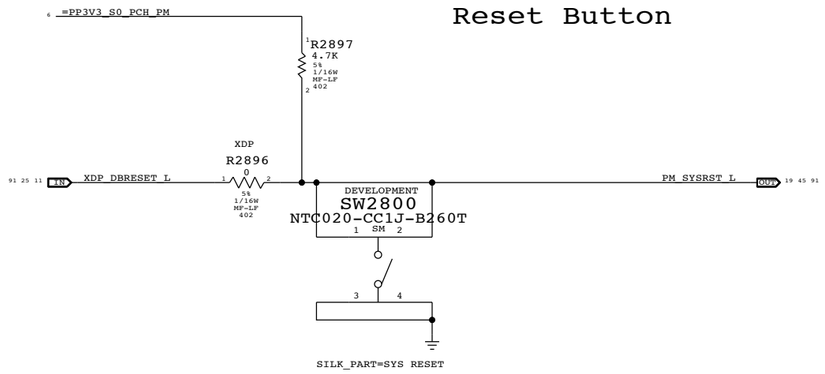


PCH 25MHz Crystal



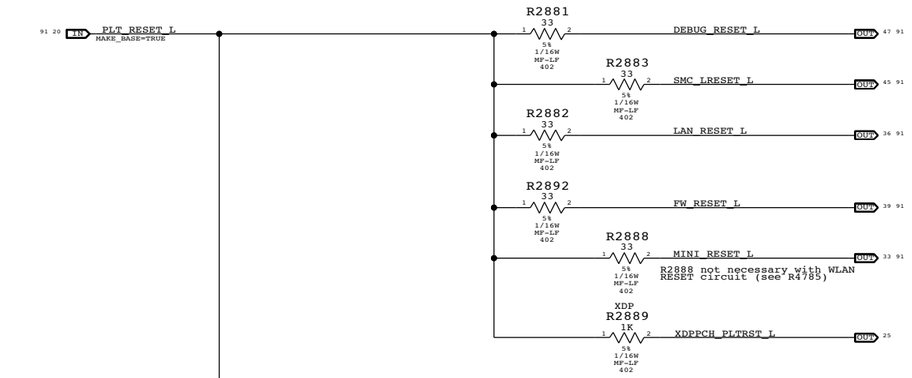
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	1	RES,0,5%,0402	C2816	

Reset Button



Platform Reset Connections

Unbuffered



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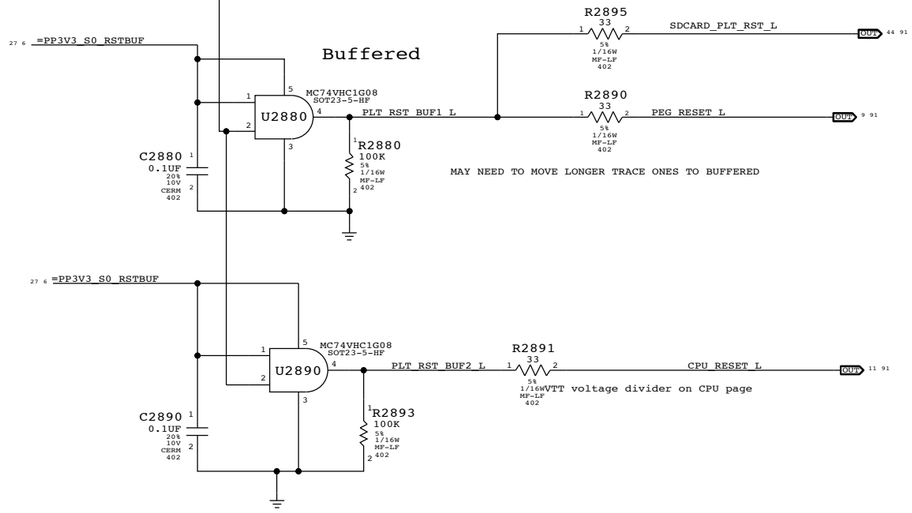
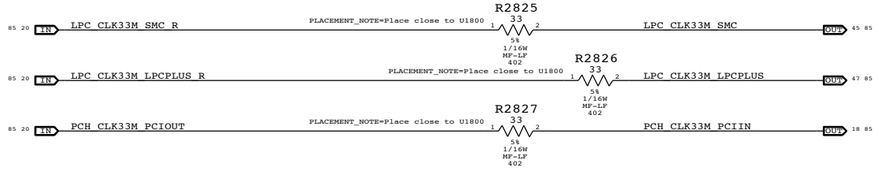




SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

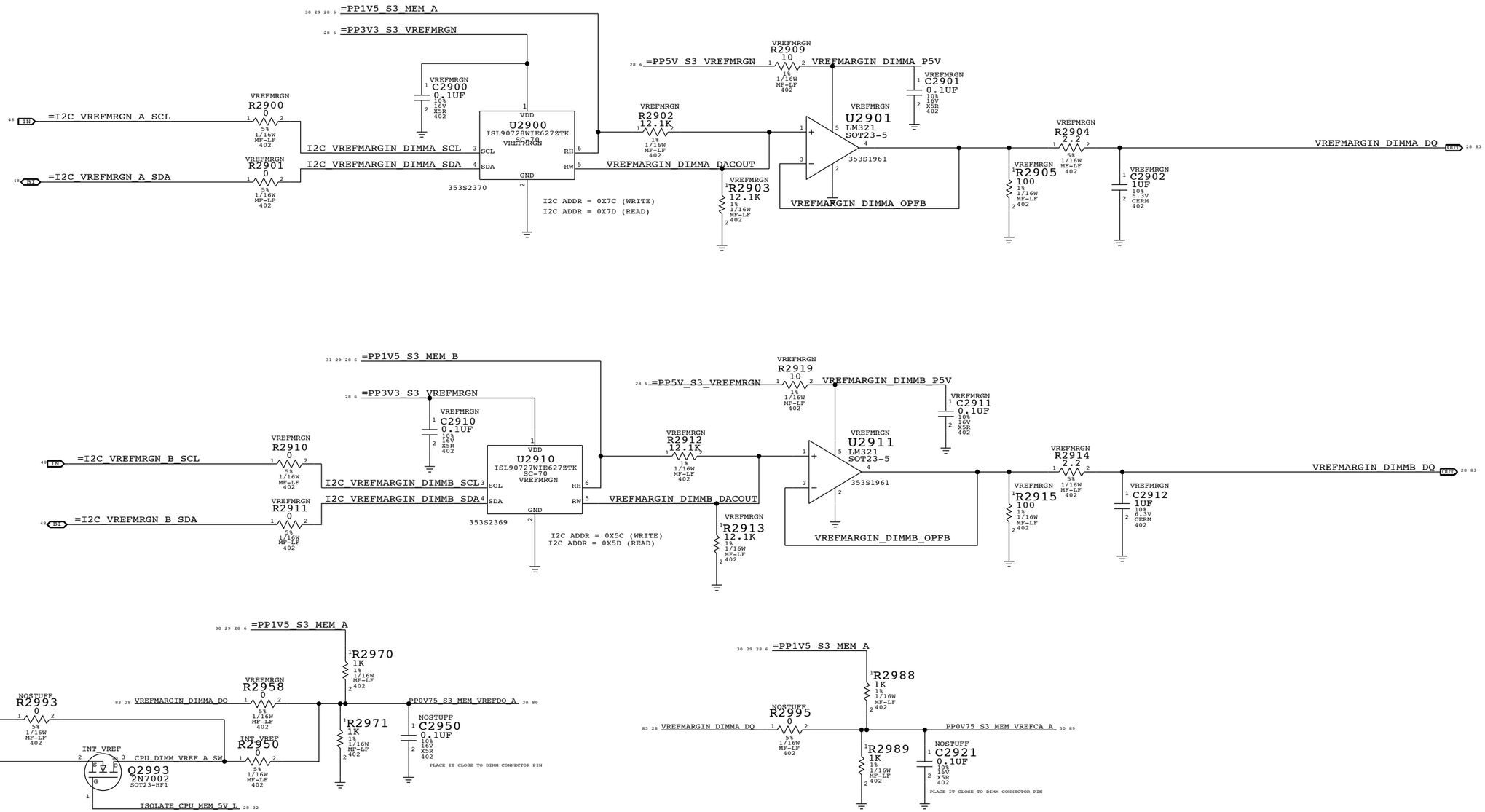
DRAWING NUMBER: 051-8233 SIZE: D

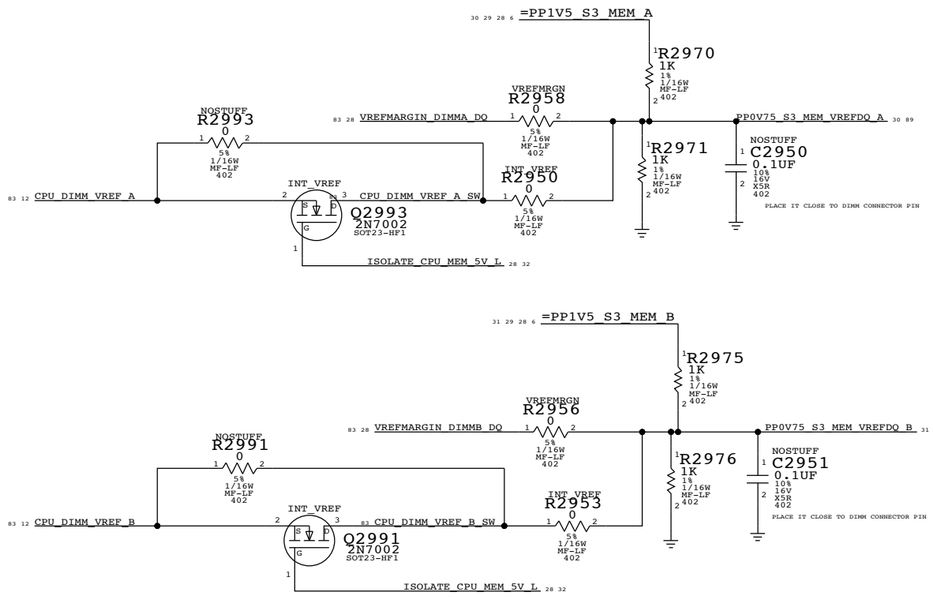
REVISION: G.0.0

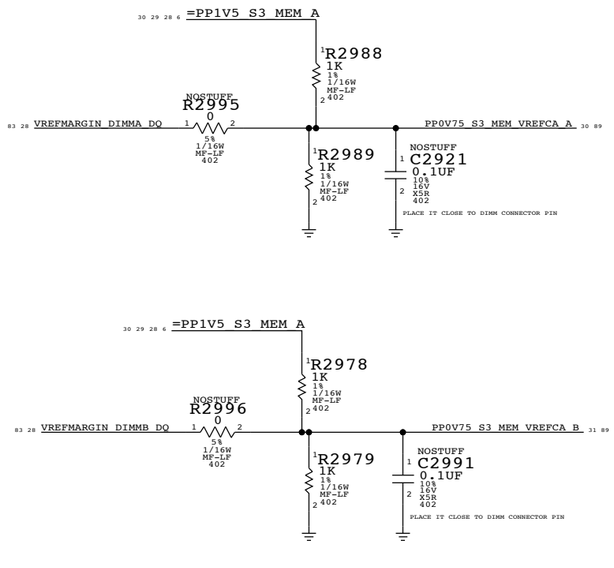
BRANCH:

PAGE: 28 OF 110

SHEET: 27 OF 92

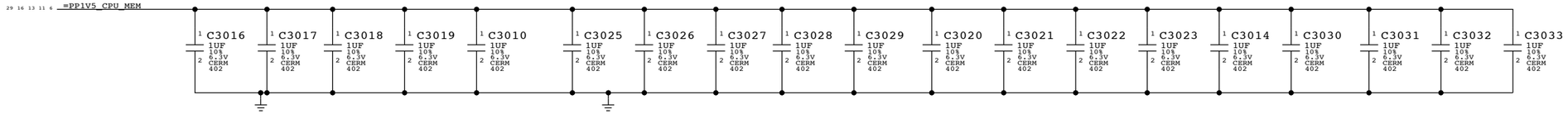




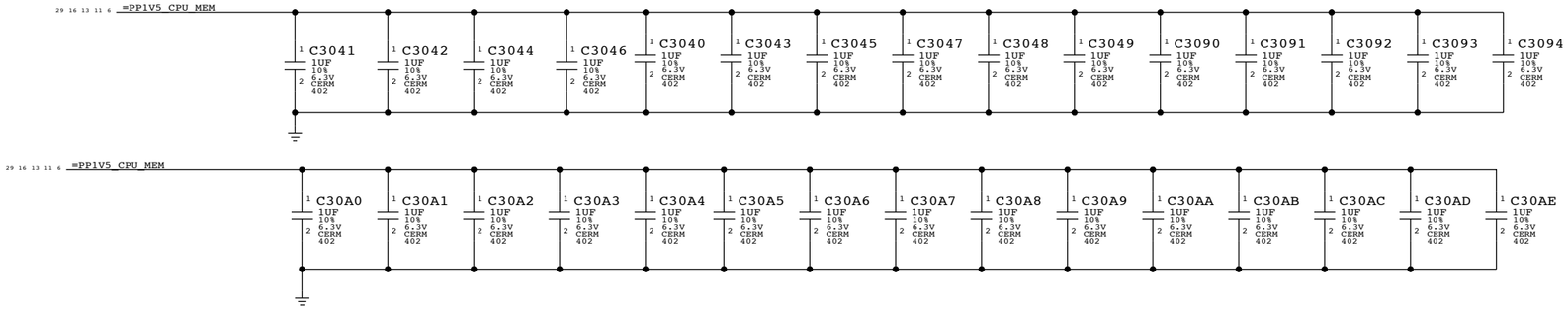


SYNC MASTER=K60 SIJI	SYNC DATE=07/01/2009
PAGE TITLE	DDR3 VREF MARGINING
Apple Inc.	DRAWING NUMBER 051-8233 · SIZE D
	REVISION G.0.0
	BRANCH
	PAGE 29 OF 110
	SHEET 28 OF 92

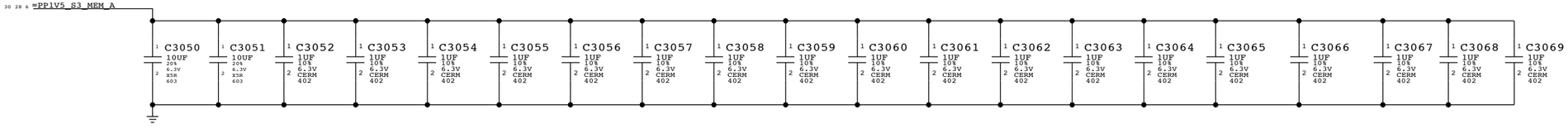
DIMM A (FURTHER FROM CPU) CAPS TO COUPLE CPU 1V5_MEM DIMM B (CLOSER TO CPU)



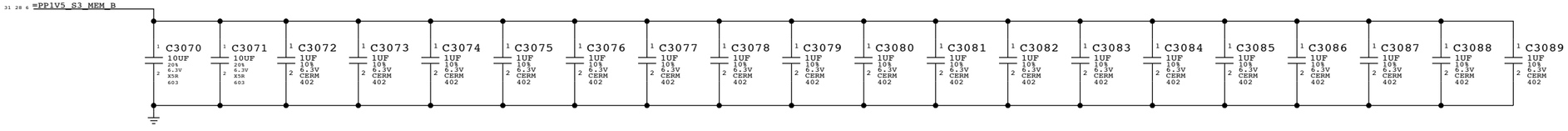
EXTRA DECOUPLING CAPS FOR CPU MEM RAIL



DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR



DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

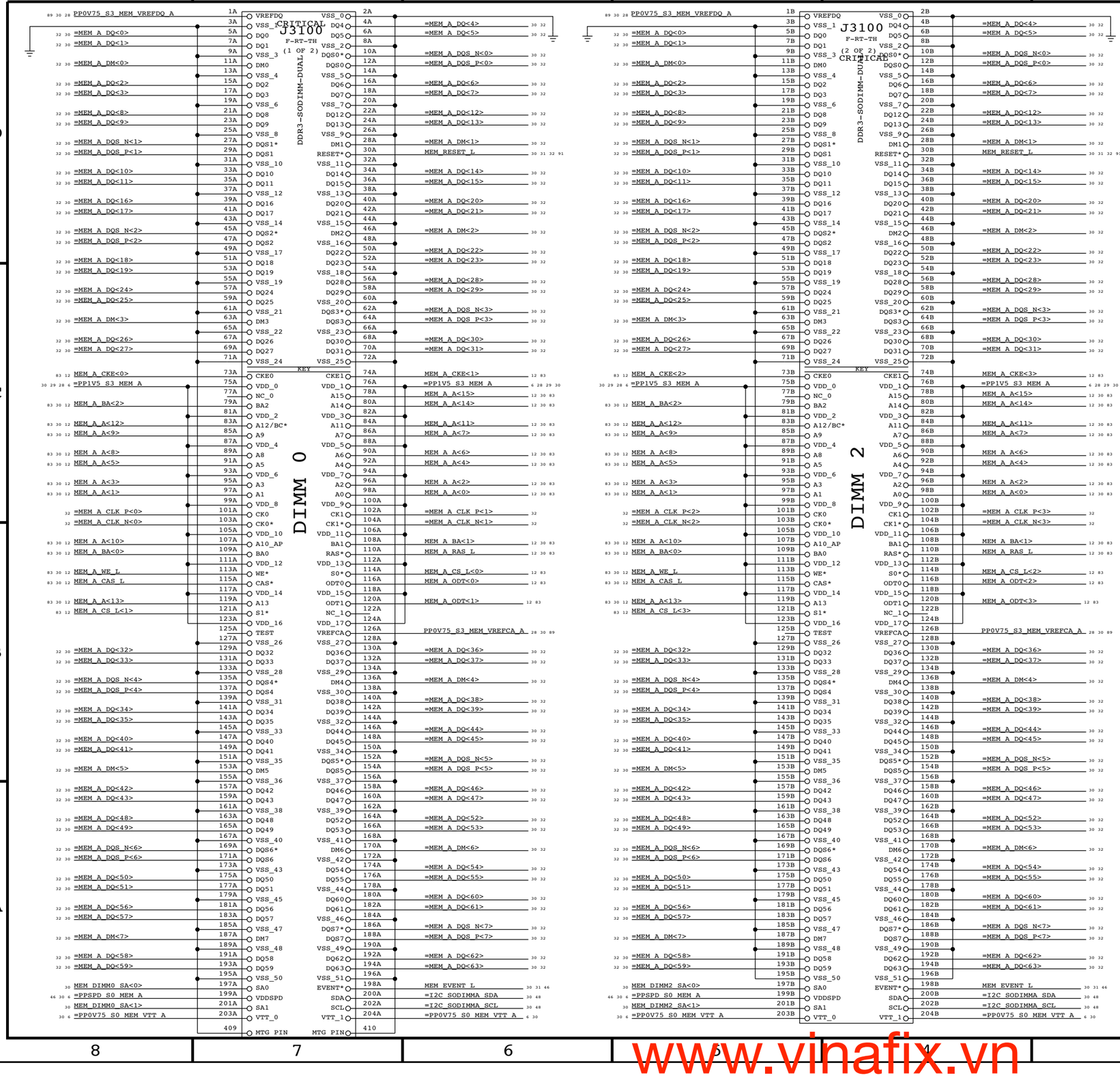


SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE
MEMORY CAPS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 30 OF 110
SHEET 29 OF 92



Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

– ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE: DDR3 SO-DIMMs 0 & 2

Apple Inc.

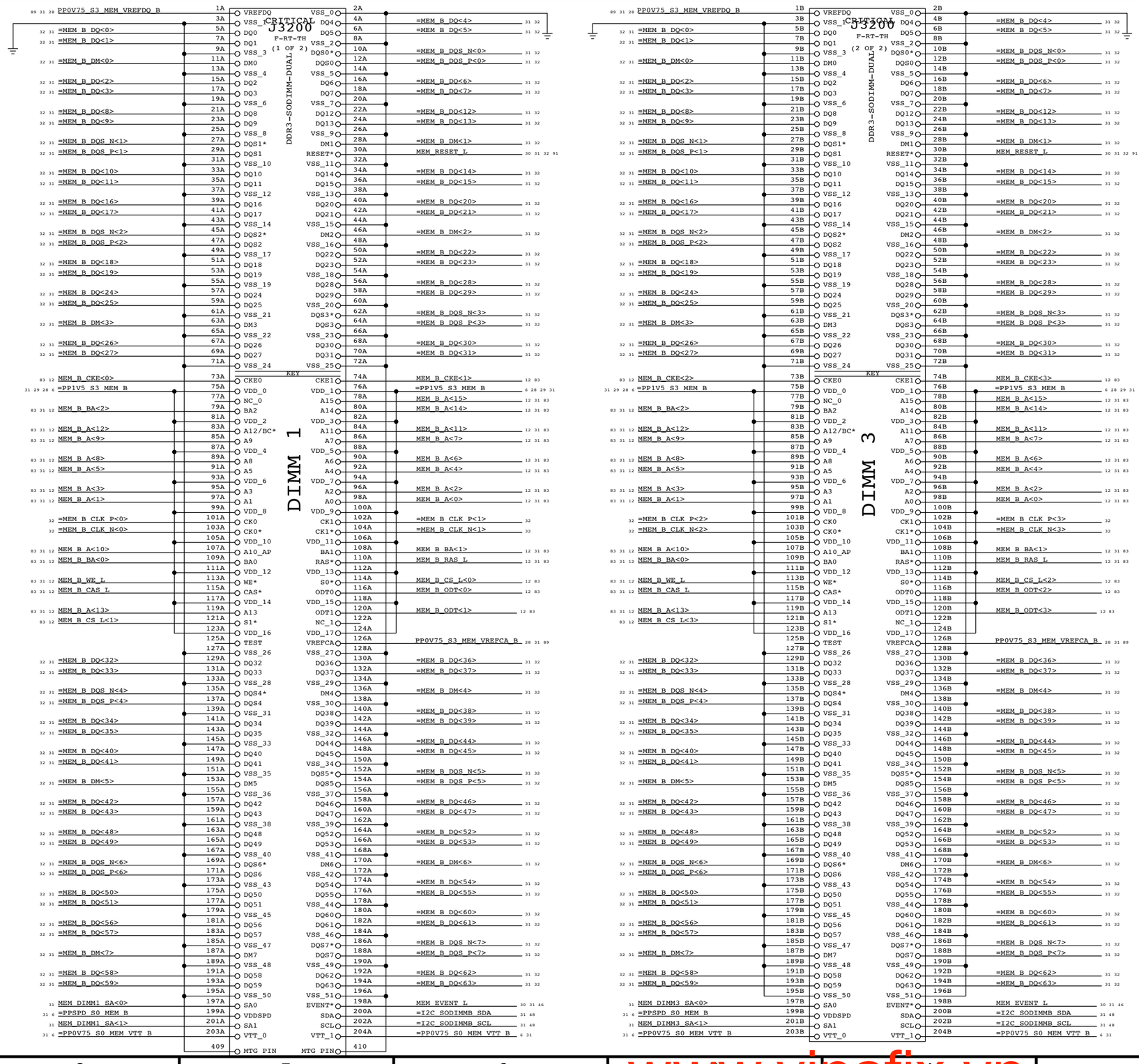
DRAWING NUMBER: 051-8233 SIZE: D

REVISION: G.0.0

BRANCH:

PAGE: 31 OF 110

SHEET: 30 OF 92



SYNC MASTER=K60 SIJI — SYNC DATE=07/01/2009

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B

Apple Inc.

DRAWING NUMBER: 051-8233 — SIZE: D

REVISION: G.0.0

BRANCH:

PAGE: 32 OF 110

SHEET: 31 OF 92

CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE		=MEM_A_DQS_N<7>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE		=MEM_A_DQS_P<7>
MEM_A_DM<0>	MAKE_BASE=TRUE		=MEM_A_DM<7>
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<57>
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<56>
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<58>
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<59>
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<60>
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<61>
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<62>
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE		=MEM_A_DQS_N<6>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE		=MEM_A_DQS_P<6>
MEM_A_DM<1>	MAKE_BASE=TRUE		=MEM_A_DM<6>
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<49>
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<52>
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<51>
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<50>
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<48>
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<53>
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<55>
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE		=MEM_A_DQS_N<5>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE		=MEM_A_DQS_P<5>
MEM_A_DM<2>	MAKE_BASE=TRUE		=MEM_A_DM<5>
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<40>
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<45>
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<46>
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<47>
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<41>
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<44>
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<43>
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE		=MEM_A_DQS_N<4>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE		=MEM_A_DQS_P<4>
MEM_A_DM<3>	MAKE_BASE=TRUE		=MEM_A_DM<4>
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<37>
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<33>
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<35>
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<34>
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<36>
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<32>
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<38>
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE		=MEM_A_DQS_N<3>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE		=MEM_A_DQS_P<3>
MEM_A_DM<4>	MAKE_BASE=TRUE		=MEM_A_DM<3>
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<28>
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<29>
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<27>
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<31>
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<25>
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<24>
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<26>
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE		=MEM_A_DQS_N<2>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE		=MEM_A_DQS_P<2>
MEM_A_DM<5>	MAKE_BASE=TRUE		=MEM_A_DM<2>
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<17>
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<16>
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<22>
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<23>
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<21>
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<20>
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<18>
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE		=MEM_A_DQS_N<1>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE		=MEM_A_DQS_P<1>
MEM_A_DM<6>	MAKE_BASE=TRUE		=MEM_A_DM<1>
MEM_A_DQ<55>	MAKE_BASE=TRUE		=MEM_A_DQ<12>
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<13>
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<10>
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<15>
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<8>
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<9>
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<11>
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE		=MEM_A_DQS_N<0>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE		=MEM_A_DQS_P<0>
MEM_A_DM<7>	MAKE_BASE=TRUE		=MEM_A_DM<0>
MEM_A_DQ<63>	MAKE_BASE=TRUE		=MEM_A_DQ<5>
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<4>
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<3>
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<2>
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<1>
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<0>
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<7>
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE		=MEM_B_DQS_N<7>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE		=MEM_B_DQS_P<7>
MEM_B_DM<0>	MAKE_BASE=TRUE		=MEM_B_DM<7>
MEM_B_DQ<7>	MAKE_BASE=TRUE		=MEM_B_DQ<61>
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<60>
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<62>
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<63>
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<56>
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<57>
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<58>
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE		=MEM_B_DQS_N<6>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE		=MEM_B_DQS_P<6>
MEM_B_DM<1>	MAKE_BASE=TRUE		=MEM_B_DM<6>
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<51>
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<54>
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<53>
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<52>
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<48>
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<49>
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<50>
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE		=MEM_B_DQS_N<5>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE		=MEM_B_DQS_P<5>
MEM_B_DM<2>	MAKE_BASE=TRUE		=MEM_B_DM<5>
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<45>
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<40>
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<42>
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<47>
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<44>
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<41>
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<46>
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE		=MEM_B_DQS_N<4>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE		=MEM_B_DQS_P<4>
MEM_B_DM<3>	MAKE_BASE=TRUE		=MEM_B_DM<4>
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<32>
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<39>
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<37>
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<38>
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<35>
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<34>
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<36>
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE		=MEM_B_DQS_N<3>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE		=MEM_B_DQS_P<3>
MEM_B_DM<4>	MAKE_BASE=TRUE		=MEM_B_DM<3>
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<28>
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<24>
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<31>
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<30>
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<29>
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<25>
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<27>
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE		=MEM_B_DQS_N<2>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE		=MEM_B_DQS_P<2>
MEM_B_DM<5>	MAKE_BASE=TRUE		=MEM_B_DM<2>
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<18>
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<20>
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<23>
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<22>
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<19>
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<21>
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<17>
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

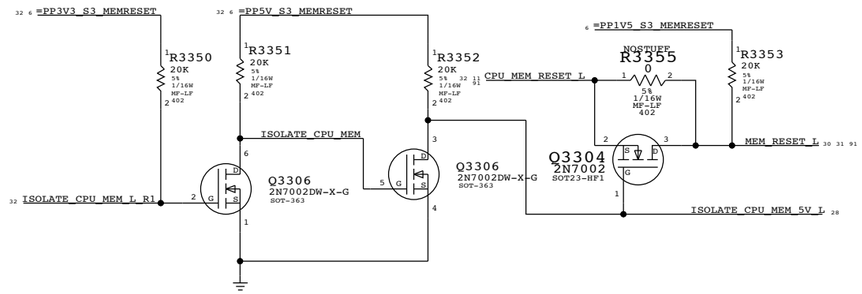
MEM_B_DQS_N<6>	MAKE_BASE=TRUE		=MEM_B_DQS_N<1>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE		=MEM_B_DQS_P<1>
MEM_B_DM<6>	MAKE_BASE=TRUE		=MEM_B_DM<1>
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<8>
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<14>
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<10>
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<11>
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<9>
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<15>
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<12>
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE		=MEM_B_DQS_N<0>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE		=MEM_B_DQS_P<0>
MEM_B_DM<7>	MAKE_BASE=TRUE		=MEM_B_DM<0>
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<2>
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<1>
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<3>
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<7>
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<4>
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<5>
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<6>
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<0>

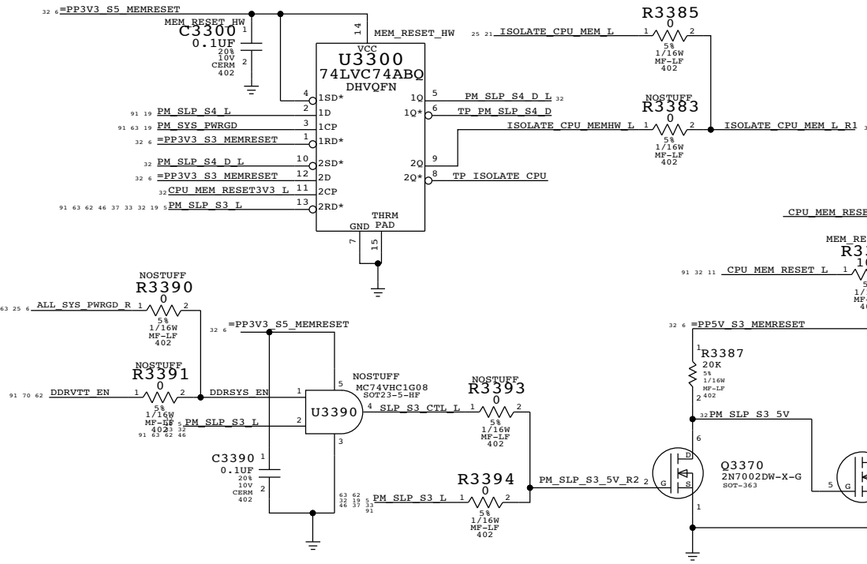
DDR3 RESET Support

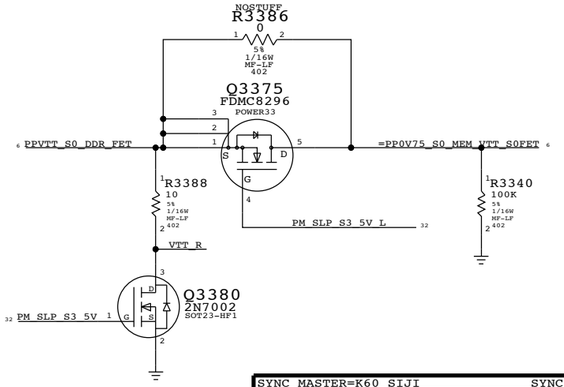
LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.



S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0





MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE		=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE		=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE		=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE		=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE		=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE		=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE		=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE		=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>			=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE		=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE		=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE		=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE		=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE		=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE		=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE		=MEM_B_CLK_N<3>

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE: DDR3 SUPPORT AND BITSWAPS

Apple Inc.

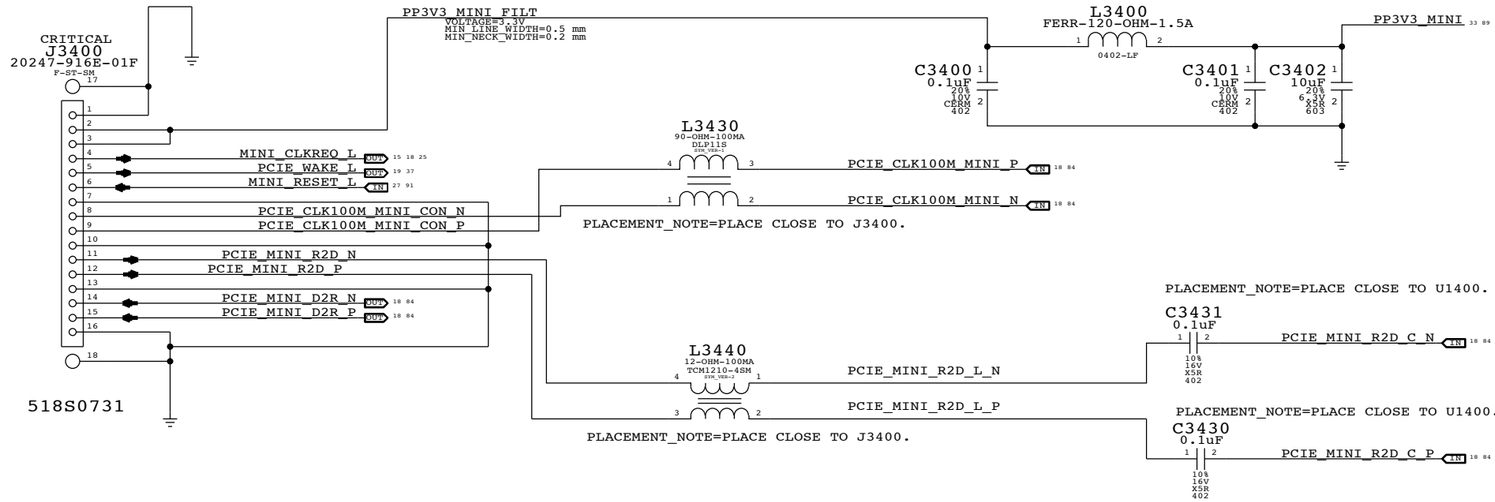
DRAWING NUMBER: 051-8233 SIZE: D

REVISION: G.0.0

BRANCH:

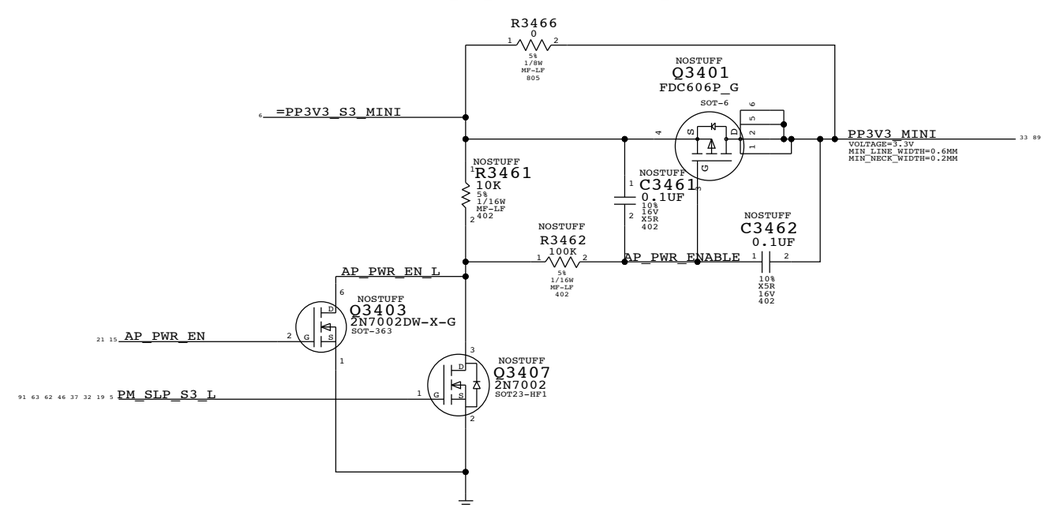
PAGE: 33 OF 110

SHEET: 32 OF 92



AP POWER ENABLE CIRCUIT

AP_PWR_ON = S0 || (S3 && AP_EN)



SYNC_MASTER=K23 AARON SYNC_DATE=07/16/2009

PAGE TITLE

PCI-E Wireless Connector

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

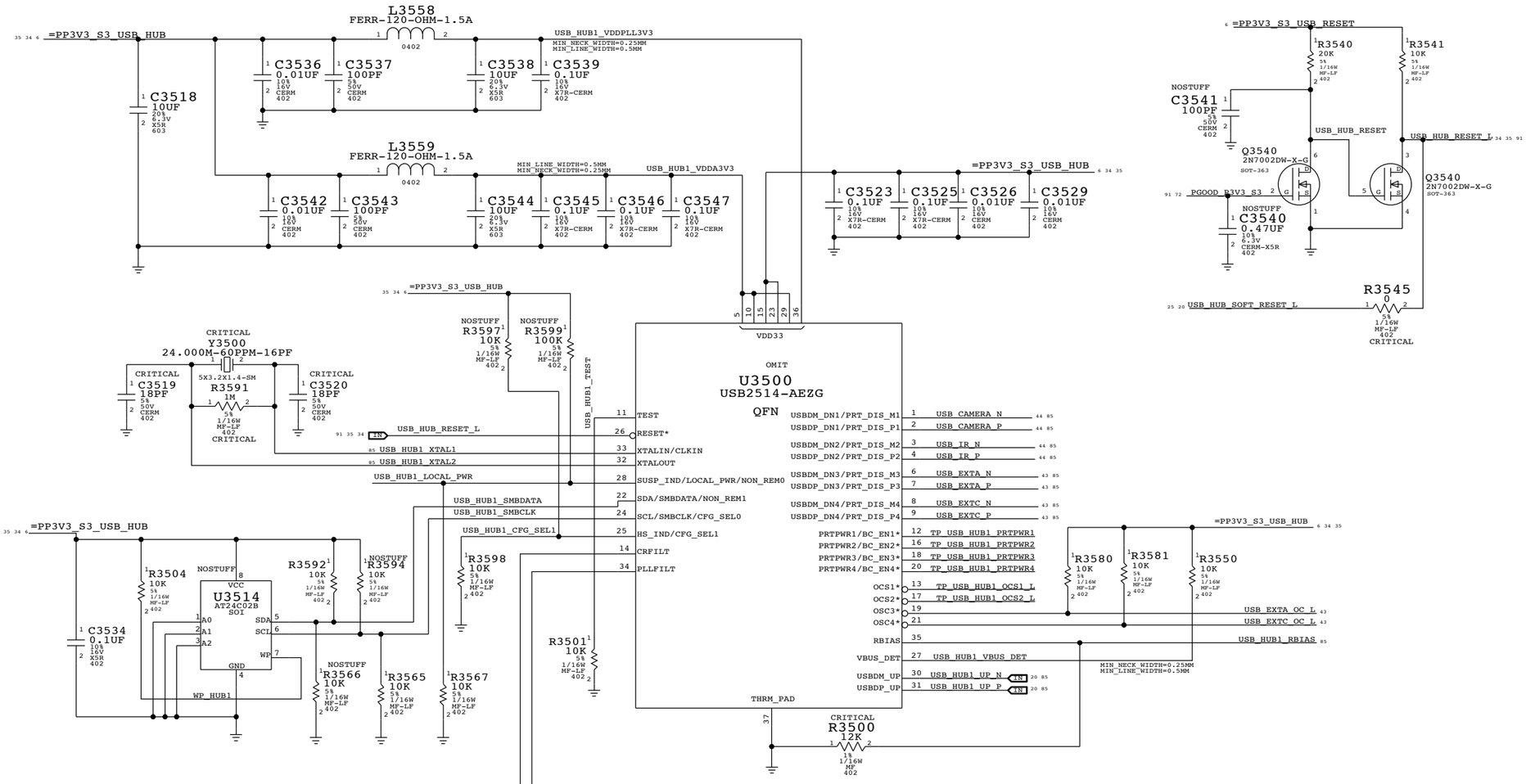
REVISION G.0.0

BRANCH

PAGE 34 OF 110

SHEET 33 OF 92

USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

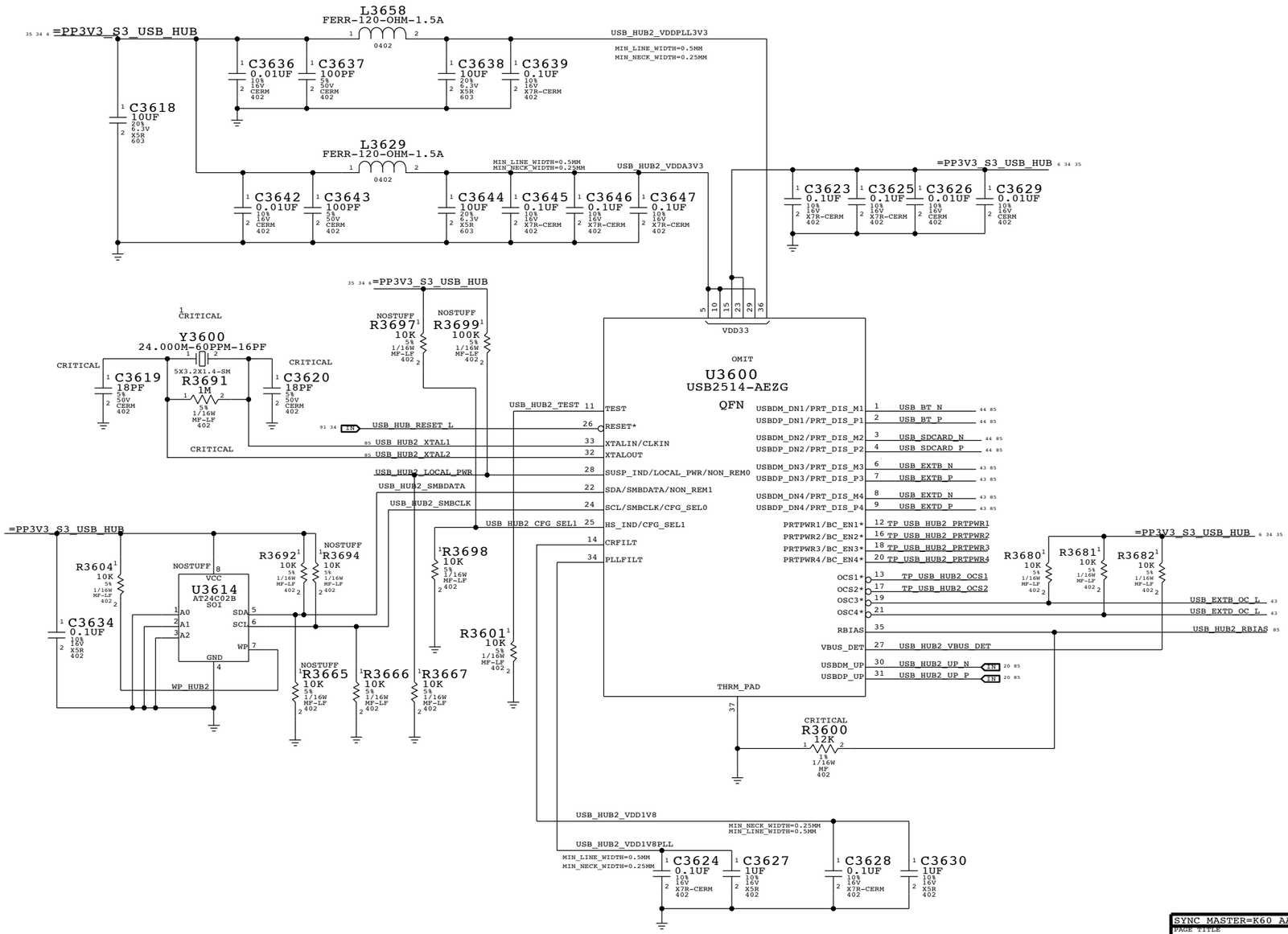
REVISION: G.0.0

BRANCH:

PAGE: 35 OF 110

SHEET: 34 OF 92

USB HUB-2



SYNC MASTER=K60 AARON	SYNC DATE=07/01/2009
PAGE TITLE: USB HUB 2	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
	REVISION: G.0.0
	BRANCH:
	PAGE: 36 OF 110
	SHEET: 35 OF 92

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Page Notes

Power aliases required by this page:
- PP3V3_ENET (CAESAR II)
- =PP1V2_ENET

CRITICAL
L3703 FERR-600-OHM-0.5A SM
=PP1V2_ENET → PP1V2_LAN_PLL_VDDL
VOLTAGE=1.2V MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM
C3746 4.7UF 10% 6.3V X5R-CERM 603
C3747 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3702 FERR-600-OHM-0.5A SM
=PP1V2_ENET → PP1V2_LAN_VDDL
VOLTAGE=1.2V MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM
C3748 4.7UF 10% 6.3V X5R-CERM 603
C3749 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3701 FERR-600-OHM-0.5A SM
=PP1V2_ENET → PP1V2_LAN_AVDDL
VOLTAGE=1.2V MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM
C3750 4.7UF 10% 6.3V X5R-CERM 603
C3751 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3700 FERR-600-OHM-0.5A SM
PP3V3_ENET → PP3V3_LAN_AVDDH
VOLTAGE=3.3V MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM
C3752 0.1UF 10% 16V X7R-CERM 402
C3753 0.1UF 10% 16V X7R-CERM 402

=PP1V2_ENET
C3726 10UF 10% 6.3V X5R 805
C3762 0.1UF 10% 16V X7R-CERM 402
PP1V2_ENET_VDDCIO
C3712 0.1UF 10% 16V X7R-CERM 402
C3713 0.1UF 10% 16V X7R-CERM 402
PP3V3_ENET
C3714 4.7UF 10% 6.3V X5R-CERM 603
C3715 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3718 FERR-600-OHM-0.5A SM
PP3V3_ENET → PP3V3_LAN_BIASVDDH
VOLTAGE=3.3V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.4MM
C3723 0.1UF 10% 16V X7R-CERM 402
PP3V3_LAN_XTALVDDH
C3724 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3711 FERR-600-OHM-0.5A SM
PP3V3_ENET → PP1V2_LAN_GPHY_PLLVDDL
VOLTAGE=3.3V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.4MM

CRITICAL
L3710 FERR-600-OHM-0.5A SM
PP3V3_ENET → =PP1V2_ENET
C3727 4.7UF 10% 6.3V X5R-CERM 603
C3725 0.1UF 10% 16V X7R-CERM 402

OMIT
CRITICAL
U3700 BCM5764M QFN

AVDDH (42,48) AVDDL (39,45,51) PCIE_PLLVDDL (27,30) PCIE_VDDL (24,33) VDDC (13,20,34,60) VDDC_IO (5,17,55) VDDIO (6,15,19,56,61) BIASVDDH (36) XTALVDDH (23) GPHY_PLLVDDL (35)

PCIE_ENET_D2R_N → C3716 0.1uF 10% 16V X5R 402 → PCIE_ENET_D2R_C_N → PCIE_TXD_N (25)
PCIE_ENET_D2R_P → C3717 0.1uF 10% 16V X5R 402 → PCIE_ENET_D2R_C_P → PCIE_TXD_P (26)
PLACEMENT_NOTE=PLACE C3718,C3719 CLOSE TO SB
PCIE_ENET_R2D_C_P → C3718 0.1uF → PCIE_ENET_R2D_P → PCIE_RXD_P (31)
PCIE_ENET_R2D_C_N → C3719 0.1uF → PCIE_ENET_R2D_N → PCIE_RXD_N (32)
PCIE_CLK100M_ENET_P → PCIE_REFCLK_P (29)
PCIE_CLK100M_ENET_N → PCIE_REFCLK_N (28)
LAN_RESET_L → PERST* (10)
BCM5764M_WAKE_L → WAKE* (12)
ENET_CLKREQ_L → CLKREQ* (11)
ENET_RDAC → RDAC (37)
PP3V3_ENET → NOSTUFF R3700 0 5% 1/16W MF-LF 402 → UART_MODE (9)
ENET_LOW_PWR → LOW_PWR (3)
=PP3V3_S0_ENET → R3702 1K 5% 1/16W MF-LF 402 → VMAIN_PRSNT (53)
PP3V3_ENET → R3703 1K 5% 1/16W MF-LF 402 → VAUX_PRSNT (54)
SUPER_IDDQ (16)

WAKE#
Must isolate from PCIE WAKE# if Phy is powered-down in S3/S5.
ENET_WAKE_L → R3723 0 5% 1/16W MF-LF 402

R3701 1.24K 1% 1/16W MF-LF 402

ENET_CLK25M_XTALI → XTALI (21)
R3704 200 5% 1/16W MF-LF 402 → ENET_CLK25M_XTALO → XTALO (22)
CRITICAL
Y3700 25.0000M SM-3-LF 197S0167 CL = 20PF
C3720 27PF 5% 50V CERM 402
C3721 27PF 5% 50V CERM 402

NC (38, 52, 68)
DC0 (28)
DC1 (52)
THRM_PAD (69)

ENERGY_DET (59) → ENET_ENERGY_DET
TRD0_P (40) → ENET_MDI_P<0>
TRD0_N (41) → ENET_MDI_N<0>
TRD1_P (44) → ENET_MDI_P<1>
TRD1_N (43) → ENET_MDI_N<1>
TRD2_P (46) → ENET_MDI_P<2>
TRD2_N (47) → ENET_MDI_N<2>
TRD3_P (50) → ENET_MDI_P<3>
TRD3_N (49) → ENET_MDI_N<3>
LINKLED* (2) → ENET_LED_ACT_L
SPD100LED* (1) → ENET_LED_LINK10_100_L
SPD1000LED* (67) → ENET_LED_LINK1000_L
TRAFFICLED* (66) → ENET_LED_LINK_L
SCLK/EECLK (65) → ENET_SCLK
SI (63) → ENET_MISO
SO/EEDATA (64) → ENET_MOSI
CS* (62) → ENET_CS
SMB_CLK (58) → ENET_SMB_CLK
SMB_DATA (57) → ENET_SMB_DATA
GPIO_0/SERIAL_DO (4) → NC
GPIO_1/SERIAL_DI (7) → NC
GPIO_2 (8) → NC
REGCTL12 (14) → ENET_CTRL12
REGOUT12_IO (18) → PP1V2_ENET_VDDCIO VOLTAGE=1.2V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.4MM

PP3V3_ENET
R3765 10K 5% 1/16W MF-LF 402
R3766 10K 5% 1/16W MF-LF 402

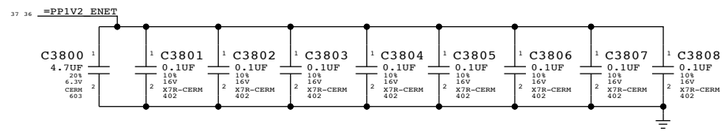
Flash Strapping Support
Atmel SO, CS, SCLK logic high; SI logic low
ST Micro CS logic high; SCLK, SI, SO logic low

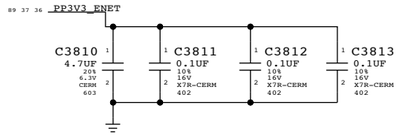
Note: CAESAR II has internal pullups on SPI pins
Pullup provisions will be removed in Proto 2
SI PIN OF CAESAR II SHOULD BE CONNECTED TO SO OF AT45DB011D, AND VICE VERSA

PP3V3_ENET
C3788 0.1UF 10% 16V X7R-CERM 402
NOSTUFF R3714 4.7K 5% 1/16W MF-LF 402
NOSTUFF R3715 4.7K 5% 1/16W MF-LF 402
OMIT
U3701 AT45DB011D SOIC-8S1
VCC
SCK ← ENET_SCLK
CS* ← ENET_CS
WP*
RESET*
GND
SI → ENET_MOSI
SO → ENET_MISO
NOSTUFF R3718 4.7K 5% 1/16W MF-LF 402
NOSTUFF R3719 4.7K 5% 1/16W MF-LF 402
NOSTUFF R3716 4.7K 5% 1/16W MF-LF 402
NOSTUFF R3717 4.7K 5% 1/16W MF-LF 402

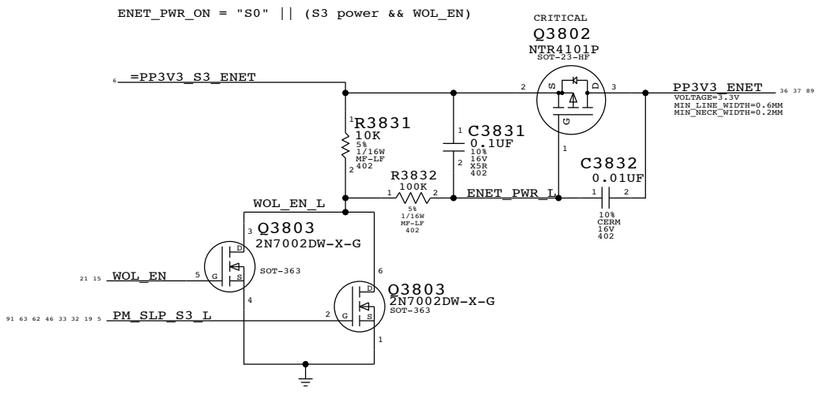
SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009
PAGE TITLE: ETHERNET (CAESAR II)
Apple Inc.
DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 37 OF 110
SHEET 36 OF 92

CAESAR II DECOUPLING

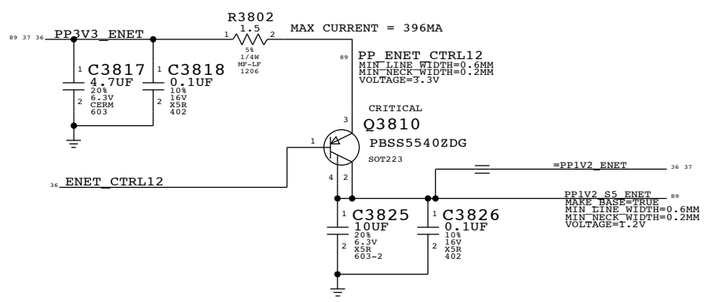


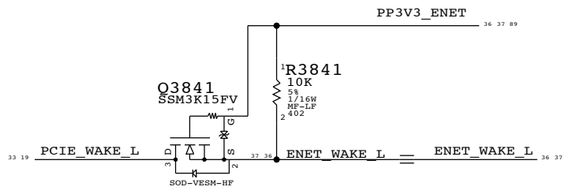


ENET POWER ENABLE CIRCUIT

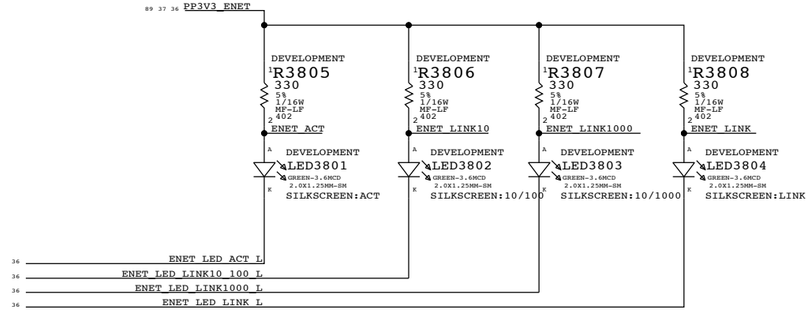


CAESAR II 1V2 RAIL SUPPLY





CAESAR II LED SUPPORT



SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE

CAESAR II SUPPORT

Apple Inc.

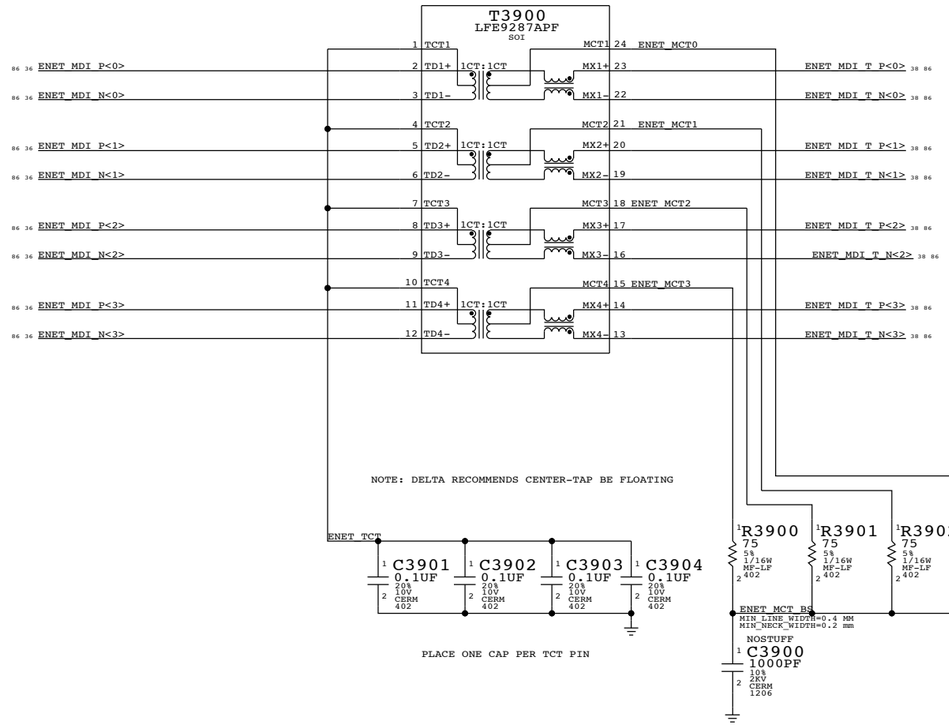
DRAWING NUMBER 051-8233 SIZE D

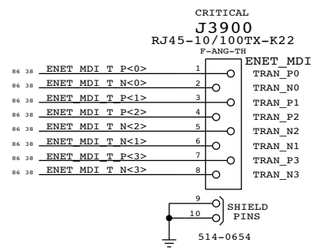
REVISION G.0.0

BRANCH

PAGE 38 OF 110

SHEET 37 OF 92





SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 39 OF 110
SHEET 38 OF 92

PCI EXPRESS

1394B OHCI & PHY

Power Aliases:

FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.

FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.

For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

Single-port:
PC[0:2] = '000'

Multiple-ports:
PC[0:2] = '100'

Alias =FWPHY_PC0 as appropriate

Unused Ports:

TP/NC TPBIASx

TP/NC TPAx_P/TPAx_N

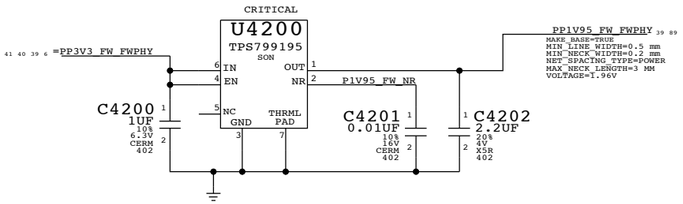
Ground TPBx_P/TPBx_N

DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors

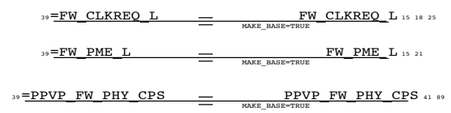
Strap DSx high on unused ports.

SYNC MASTER=K23 AARON	SYNC DATE=07/16/2009
PAGE TITLE: FireWire LLC/PHY (XIO2213B)	
Apple Inc.	DRAWING NUMBER 051-8233, SIZE D
	REVISION G.0.0
	BRANCH
	PAGE 41 OF 110
	SHEET 39 OF 92

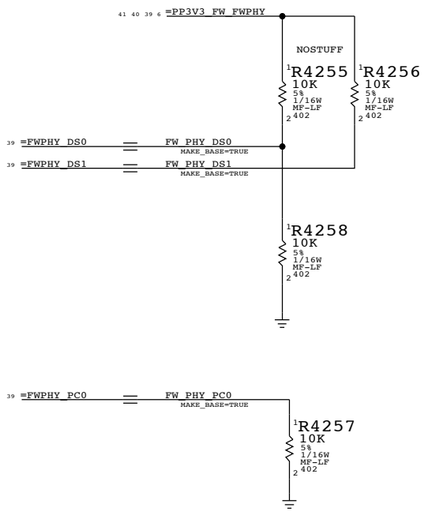
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



1394 PHY STRAPPING OPTIONS

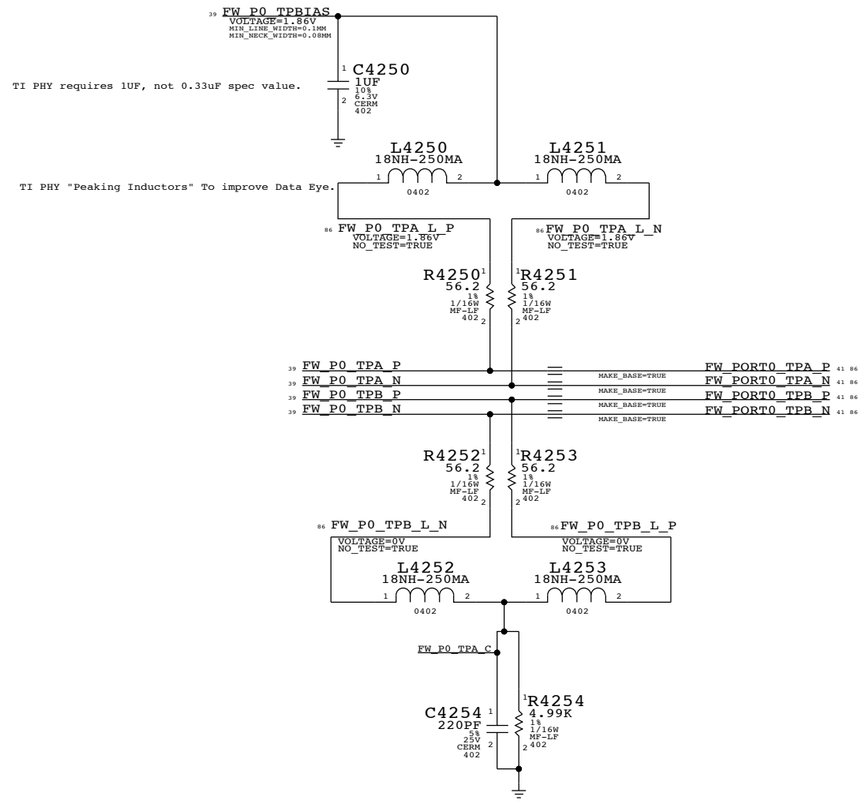


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

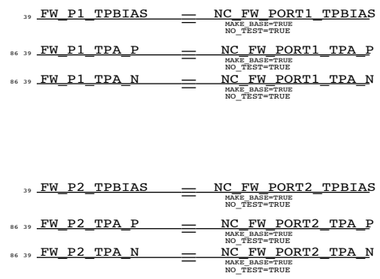
iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE: FW: 1394B MISC

Apple Inc.

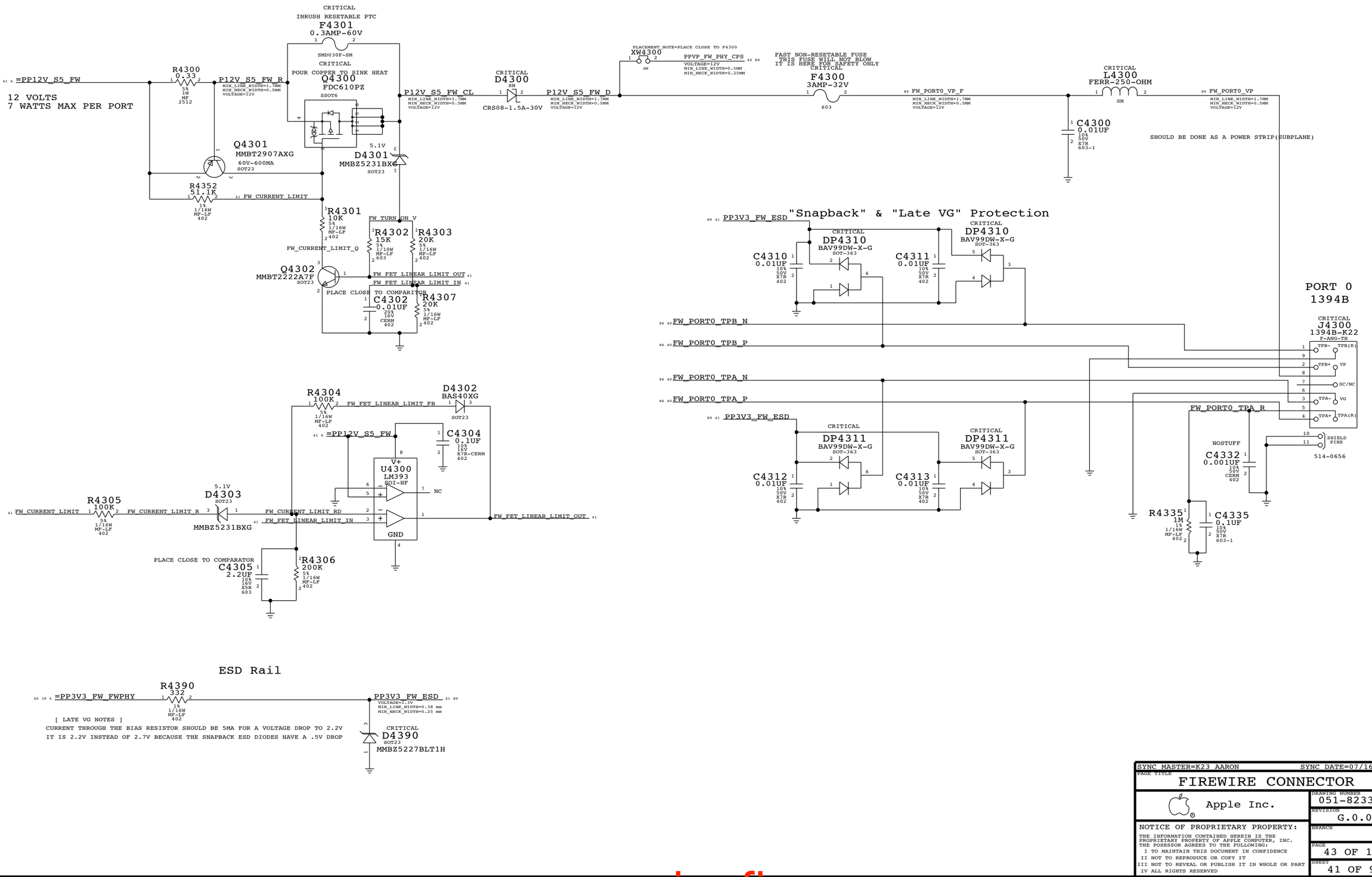
DRAWING NUMBER: 051-8233 SIZE: D

REVISION: G.0.0

BRANCH:

PAGE: 42 OF 110

SHEET: 40 OF 92



SYNC MASTER=K23 AARON SYNC DATE=07/16/2009

PAGE TITLE: FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: G.0.0

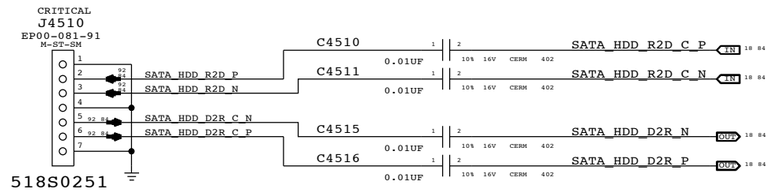
BRANCH:

PAGE: 43 OF 110

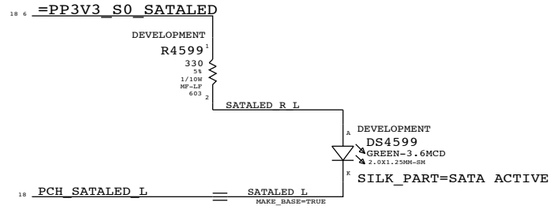
SHEET: 41 OF 92

SATA PORT A0 FOR HDD

SILKSCREEN:HDD



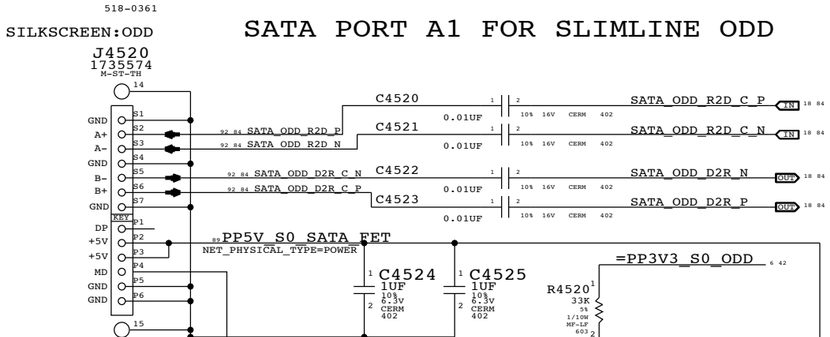
SATA Activity LED



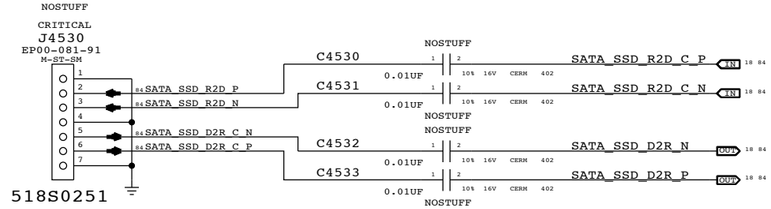
SATA PORT A1 FOR SLIMLINE ODD

518-0361

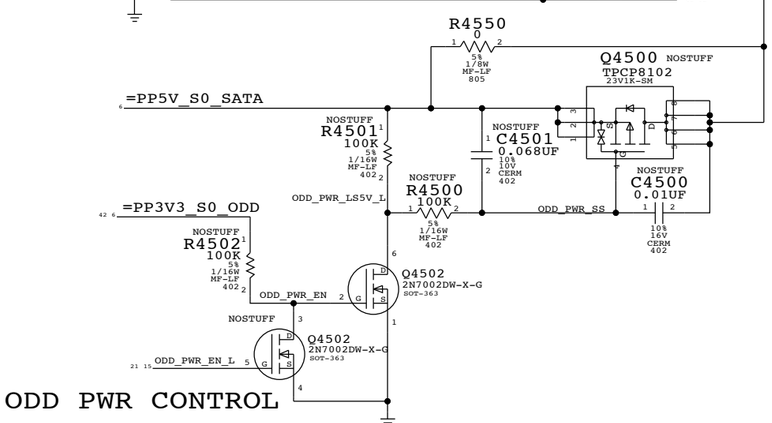
SILKSCREEN:ODD



SATA PORT A2 FOR SSD



ODD PWR CONTROL



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 45 OF 110
SHEET: 42 OF 92

USB/SMC DEBUG MUX

=PP3V3_G3H_SMCUSBMUX

U4650 PI3USB102ZLE TQFN

MOJOMUX

SMC_RX_L
SMC_TX_L
USB_EXTD_P
USB_EXTD_N
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB

PRODUCTION R4651 0 5% 1/16W MF-LF 402

PRODUCTION R4652 0 5% 1/16W MF-LF 402

PORT 3

=PP5V_S3_USB
U4601 TPS2060 MSOP
USB_EXTC_OC_L
USB_EXTD_OC_L
R4600 10K 5% 1/16W MF-LF 402
USB_PWR_ENA_L
C4605 0.1UF 20% 10V CERM 402
C4606 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
Q4600 2N7002 SOT23-HF1
PM_EN_USB_PWR
C4621 0.1UF 20% 10V CERM 402
C4631 0.1UF 20% 10V CERM 402
C4650 0.1UF 20% 10V CERM 402

PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4630 FERR-250-OHM SM
PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4630 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

USB_D_MUXED_N
USB_D_MUXED_P
L4631 120-OHM-90MA DLP0NS
USB_PORT3_N
USB_PORT3_P

J4630 USB-K22 F-ANG-TH
VDD VBUS
D- DATA-
D+ DATA+
GND GND
514-0659

D4630 RCLAMP0502N SLP1210N6
VBUS GND NC IO NC IO

PORT 2

=PP5V_S3_USB
U4600 TPS2060 MSOP
USB_EXTA_OC_L
USB_EXTB_OC_L
C4601 0.1UF 20% 10V CERM 402
C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C4603 0.1UF 20% 10V CERM 402
C4611 0.1UF 20% 10V CERM 402

PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4610 FERR-250-OHM SM
PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4610 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

USB_EXTB_N
USB_EXTB_P
L4611 120-OHM-90MA DLPONS
USB_PORT1_N
USB_PORT1_P

J4610 USB-K22 F-ANG-TH
VDD VBUS
D- DATA-
D+ DATA+
GND GND
514-0672

D4610 RCLAMP0502N SLP1210N6
VBUS GND NC IO NC IO

PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4620 FERR-250-OHM SM
PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4620 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

USB_EXTC_N
USB_EXTC_P
L4621 120-OHM-90MA DLPONS
USB_PORT2_N
USB_PORT2_P

J4620 USB-K22 F-ANG-TH
VDD VBUS
D- DATA-
D+ DATA+
GND GND
514-0659

D4620 RCLAMP0502N SLP1210N6
VBUS GND NC IO NC IO

PORT 0

PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
L4600 FERR-250-OHM SM
PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4600 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

USB_EXTA_N
USB_EXTA_P
L4601 120-OHM-90MA DLPONS
USB_PORT0_N
USB_PORT0_P

J4600 USB-K22 F-ANG-TH
VDD VBUS
D- DATA-
D+ DATA+
GND GND
514-0672

D4600 RCLAMP0502N SLP1210N6
VBUS GND NC IO NC IO

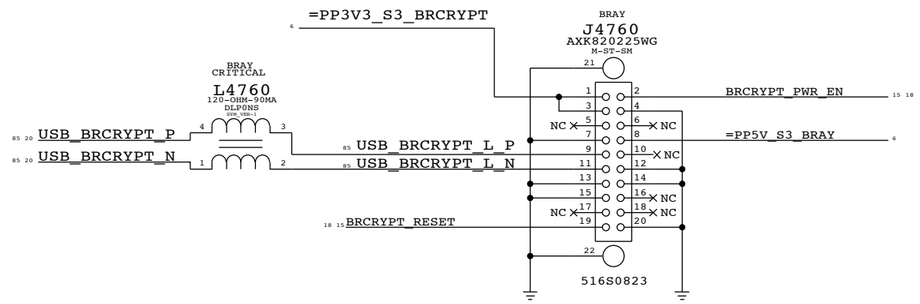
SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE
EXTERNAL USB CONNECTORS

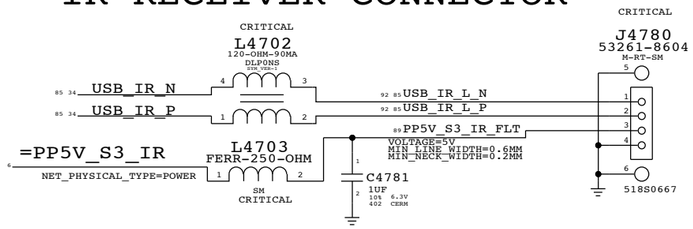
Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 46 OF 110
SHEET 43 OF 92

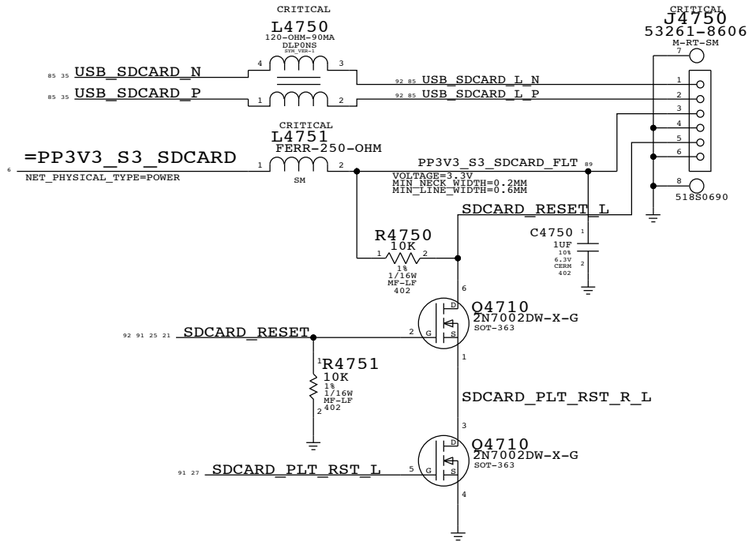
BLURAY DECRYPTOR CONN & FLTR



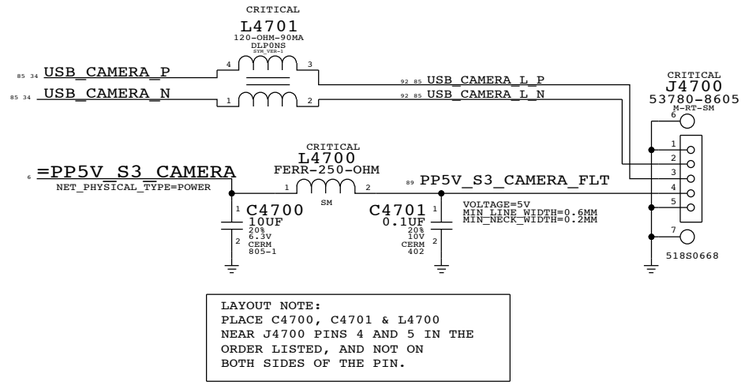
IR RECEIVER CONNECTOR



SD Card Reader Board Connector

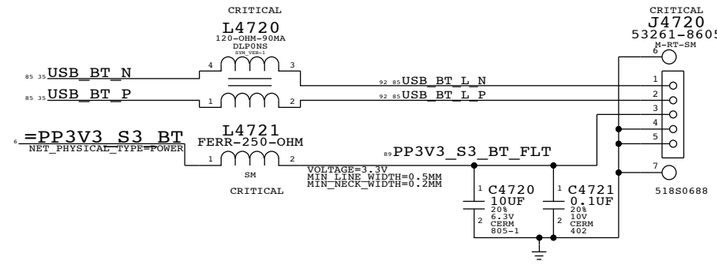


CAMERA CONNECTOR & FILTER

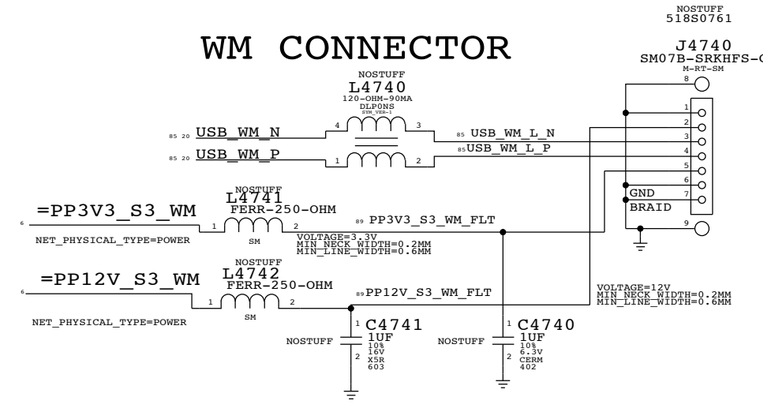


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

K37L (BLUETOOTH) CONNECTOR



WM CONNECTOR



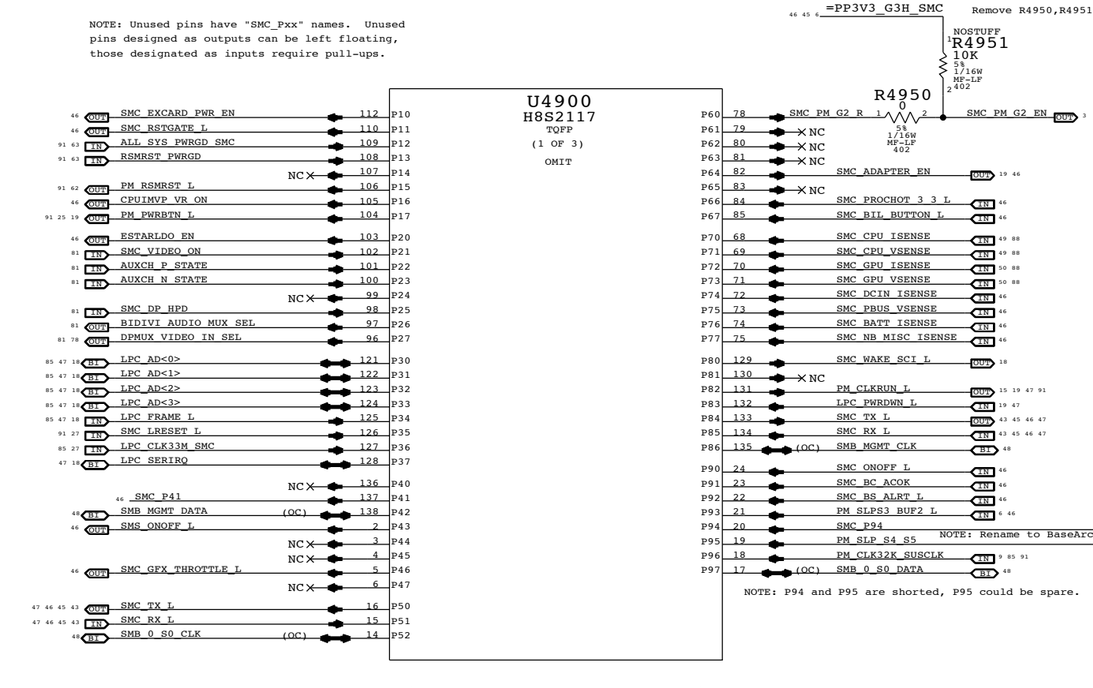
SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE
Internal USB Connections

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 47 OF 110
SHEET 44 OF 92

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



=PP3V3_G3H_SMC Remove R4950,R4951 after Proto-1

NOSTUFF R4951 10K 5% 1/16W MF-LF 402

R4950 0 5% 1/16W MF-LF 402

SMC_PM_G2_R → SMC_PM_G2_EN

NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: Rename to BaseArch

=PP3V3_G3H_SMC

NOSTUFF R4952 10K 5% 1/16W MF-LF 402

R4954 0 5% 1/16W MF-LF 402 PM_SLP_S4_2_L

NOSTUFF R4953 0 5% 1/16W MF-LF 402

R4955 0 5% 1/16W MF-LF 402 PM_SLP_S5_L

REMOVE R4953/4/5 AFTER PROTO-1

PP3V3_G3H_AVREF_SMC Peak/Ave/Standby = 2mA/1mA/5uA

=PP3V3_G3H_SMC Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805

C4903 0.1UF 20% 10V CERM 402

C4904 0.1UF 20% 10V CERM 402

C4905 0.1UF 20% 10V CERM 402

C4906 0.1UF 20% 10V CERM 402

R4999 4.7 5% 1/16W MF-LF 402

Peak/Ave/Standby= 2mA/1mA/5uA

PP3V3_G3H_SMC_AVCC

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C4907 close to U4900 pin 13

SMC_VCL

C4907 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place R4999 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76

U4900
H8S2117
TQFP
(3 OF 3)
OMIT

AVCC VCC VCL AVREF

SMC_RESET_L → RES*
SMC_XTAL → XTAL
SMC_EXTAL → EXTAL

R4909 10K 5% 1/16W MF-LF 402

R4901 10K 5% 1/16W MF-LF 402

MD1 SMC_MD1
MD2 SMC_KBC_MDE
NMI SMC_NMI
ETRST* SMC_TRST_L

NOSTUFF R4903 0 5% 1/16W MF-LF 402

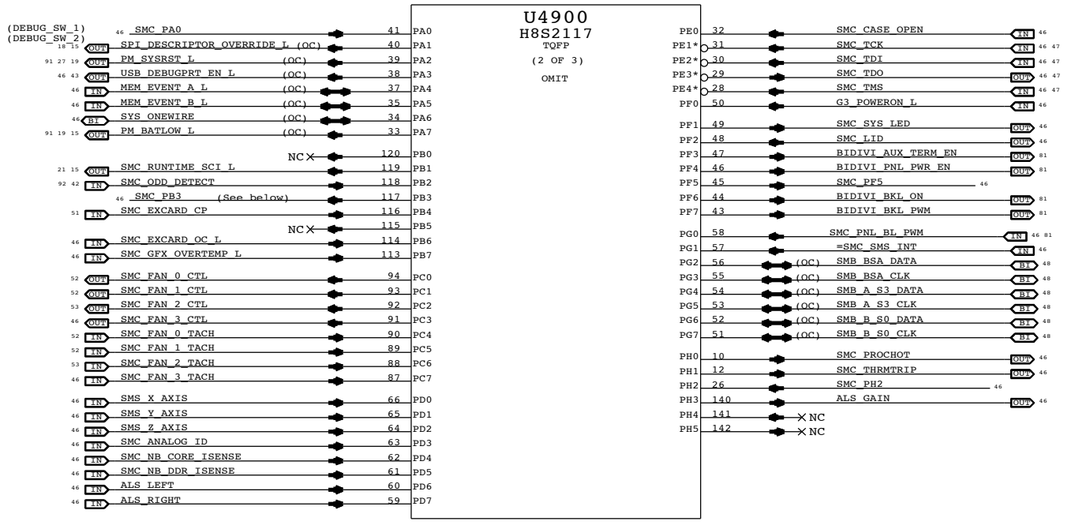
R4902 10K 5% 1/16W MF-LF 402

R4998 10K 5% 1/16W MF-LF 402

VSS AVSS

XW4900

GND_SMC_AVSS



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

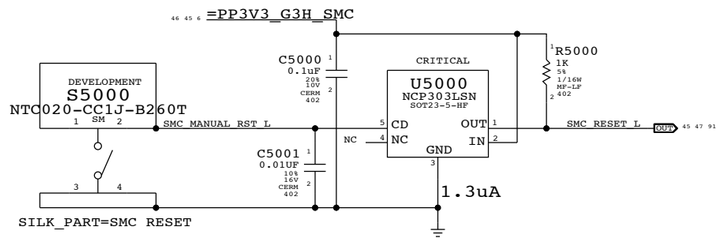
REVISION G.0.0

BRANCH

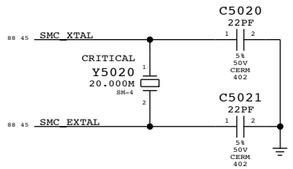
PAGE 49 OF 110

SHEET 45 OF 92

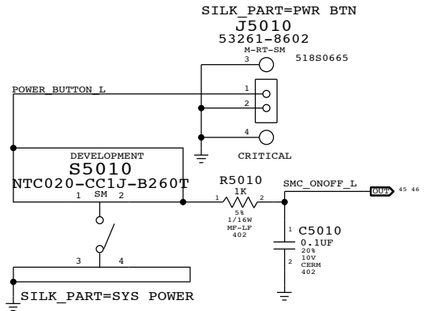
SMC Reset Button / Brownout Detect



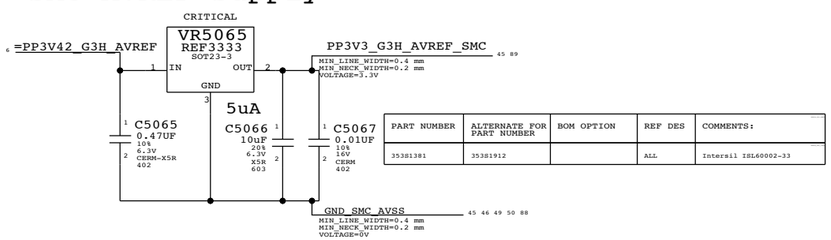
SMC Crystal Circuit



POWER BUTTON

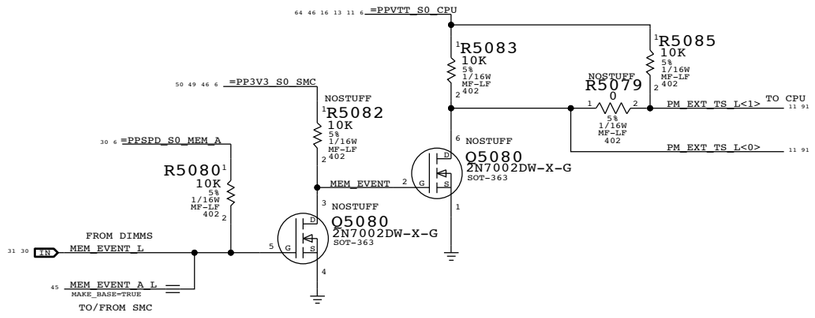


SMC AVREF Supply

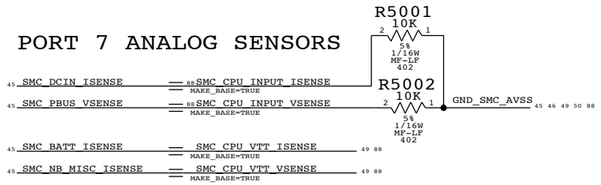


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

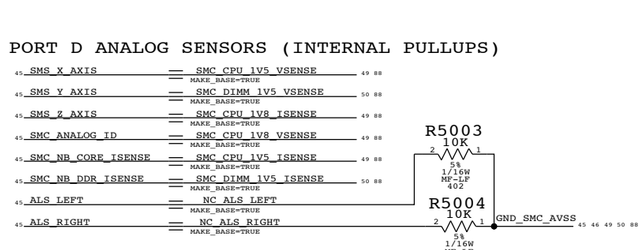
PM_EXTTS_L / MEM_EVENT LEVEL SHIFTING



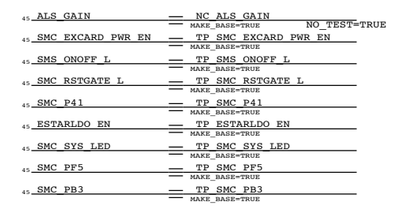
PORT 7 ANALOG SENSORS



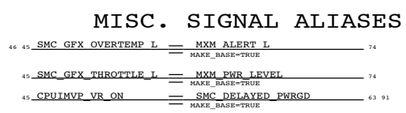
PORT D ANALOG SENSORS (INTERNAL PULLUPS)



UNUSED TP/NC ALIASES



MISC. SIGNAL ALIASES



=PP3V3_G3H_SMC

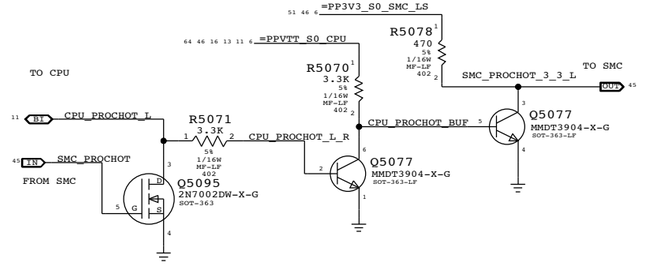
SMC_ONOFF_L	R5032	10K	5%	1/16W	MF-LF	402		
SMC_PNL_BL_PWM	R5033	100K	5%	1/16W	MF-LF	402		
SMC_PH2	R5034	10K	5%	1/16W	MF-LF	402		
SMC_TX_L	R5035	10K	5%	1/16W	MF-LF	402		
SMC_RX_L	R5036	100K	5%	1/16W	MF-LF	402		
SYS_ONEWIRE	R5037	2.0K	5%	1/16W	MF-LF	402		
SMC_BS_ALRT_L	R5038	100K	5%	1/16W	MF-LF	402		
SMC_TMS	R5039	10K	5%	1/16W	MF-LF	402		
SMC_TDO	R5040	10K	5%	1/16W	MF-LF	402		
SMC_TDI	R5041	10K	5%	1/16W	MF-LF	402		
SMC_TCK	R5042	10K	5%	1/16W	MF-LF	402		
SMC_EXCARD_OC_L	R5043	10K	5%	1/16W	MF-LF	402		
SMC_PA0	R5096	10K	5%	1/16W	MF-LF	402		
SMC_BIL_BUTTON_L	R5092	10K	5%	1/16W	MF-LF	402		
SMC_FAN_3_CTL	R5095	100K	5%	1/16W	MF-LF	402		
SMC_FAN_3_TACH	R5097	100K	5%	1/16W	MF-LF	402		
SMC_BC_ACOK	R5047	10K	5%	1/16W	MF-LF	402		
SMC_ADAPTER_EN	R5049	10K	5%	1/16W	MF-LF	402		
USB_DEBUGPRT_EN_L	R5098	10K	5%	1/16W	MF-LF	402		
=SMC_SMS_INT	R5091	10K	5%	1/16W	MF-LF	402		
SMC_LID	R5087	10K	5%	1/16W	MF-LF	402		
G3_POWERON_L	R5086	10K	5%	1/16W	MF-LF	402		

=PP3V3_S0_SMC

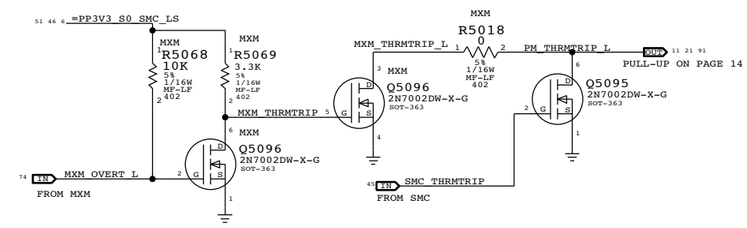
MEM_EVENT_B_L	R5093	10K	5%	1/16W	MF-LF	402		
SMC_GFX_OVERTEMP_L	R5099	10K	5%	1/16W	MF-LF	402		

SMC_CASE_OPEN	R5046	10K	5%	1/16W	MF-LF	402		
PM_SLP_S3_L	R5094	100K	5%	1/16W	MF-LF	402		
PM_SLPS3_BUF1_L								
PM_SLPS3_BUF2_L								
PM_SLP_S4_2_L	R5089	100K	5%	1/16W	MF-LF	402		

SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SYNC MASTER=K60 JERRY SYNC DATE=07/01/2009

PAGE TITLE

SMC Support

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

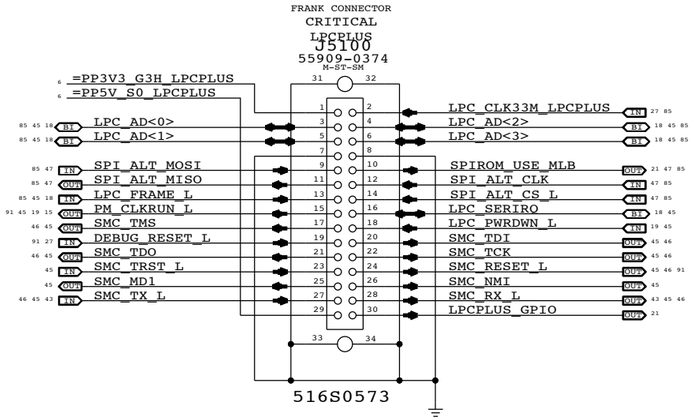
REVISION G.0.0

BRANCH

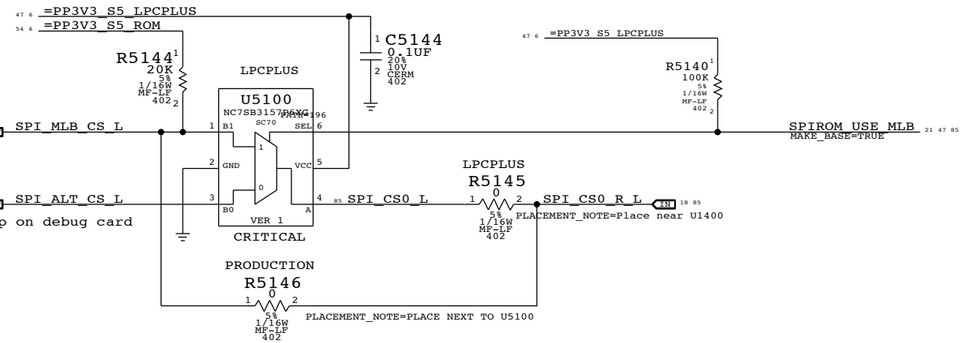
PAGE 50 OF 110

SHEET 46 OF 92

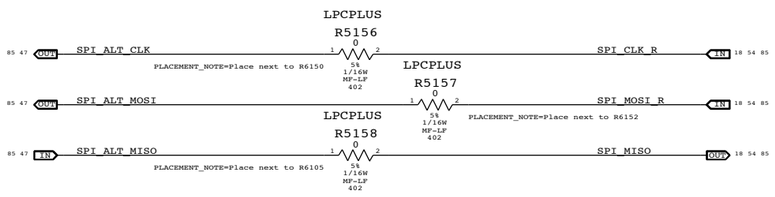
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

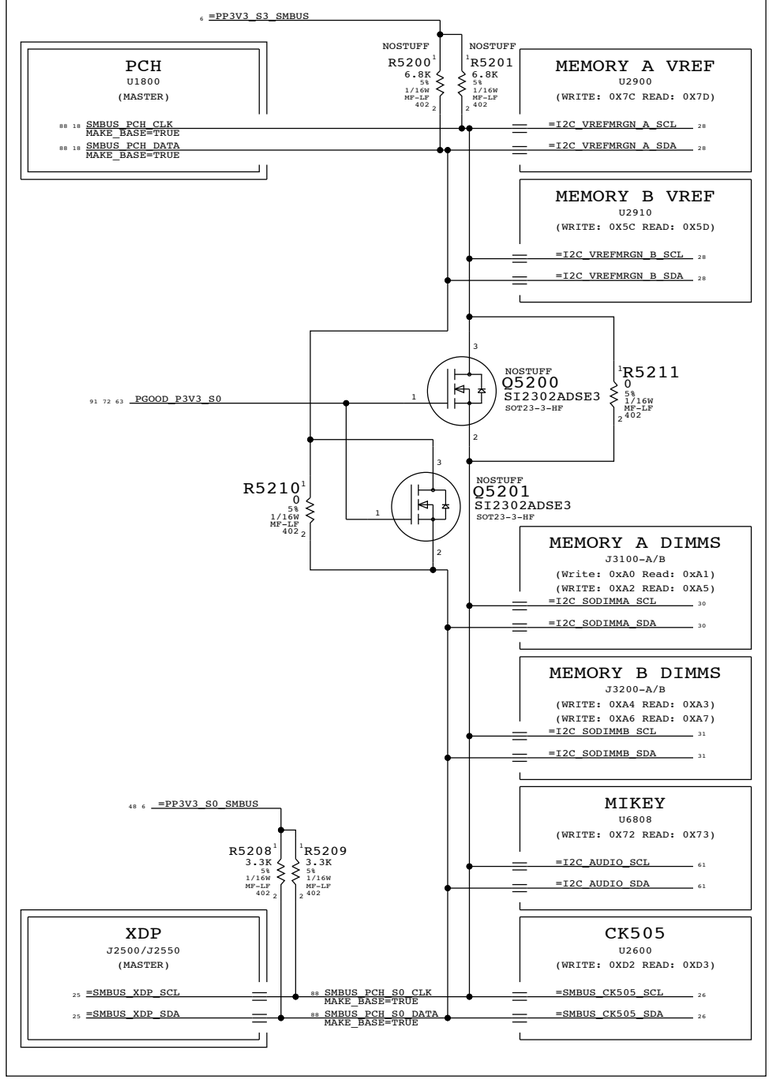
REVISION: G.0.0

BRANCH:

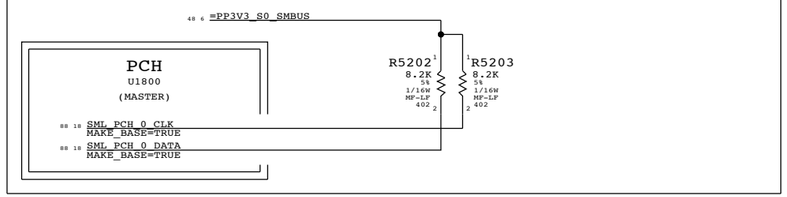
PAGE: 51 OF 110

SHEET: 47 OF 92

PCH "SMBUS" CONNECTIONS

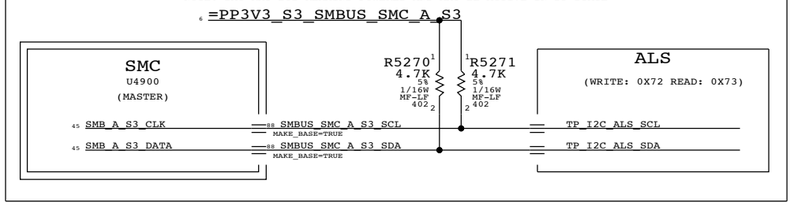


PCH "SML 0" CONNECTIONS

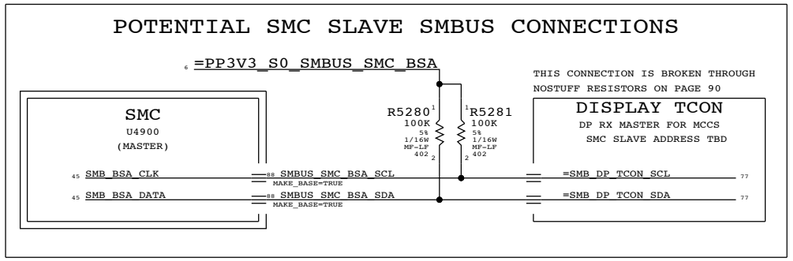


SMC "A" SMBus Connections

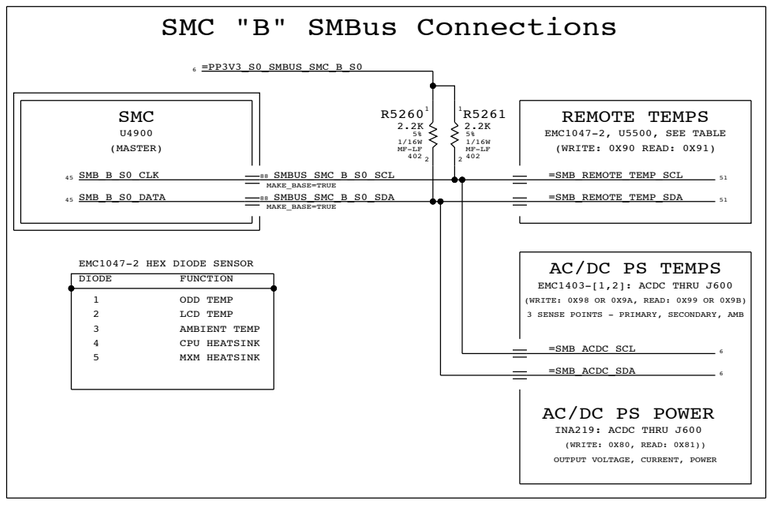
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE



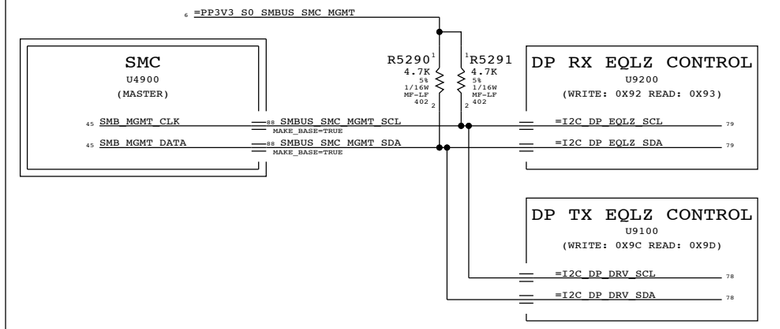
POTENTIAL SMC SLAVE SMBUS CONNECTIONS



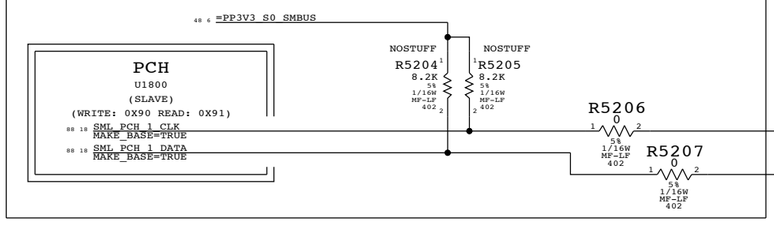
SMC "B" SMBus Connections



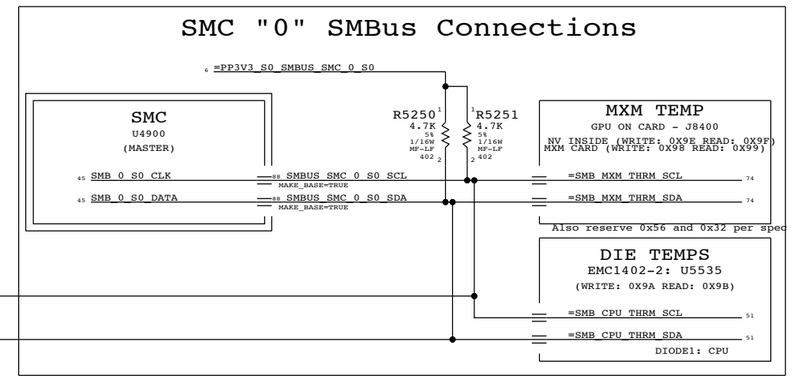
SMC "MANAGEMENT" SMBUS CONNECTIONS



PCH "SML 1" CONNECTIONS



SMC "0" SMBus Connections



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

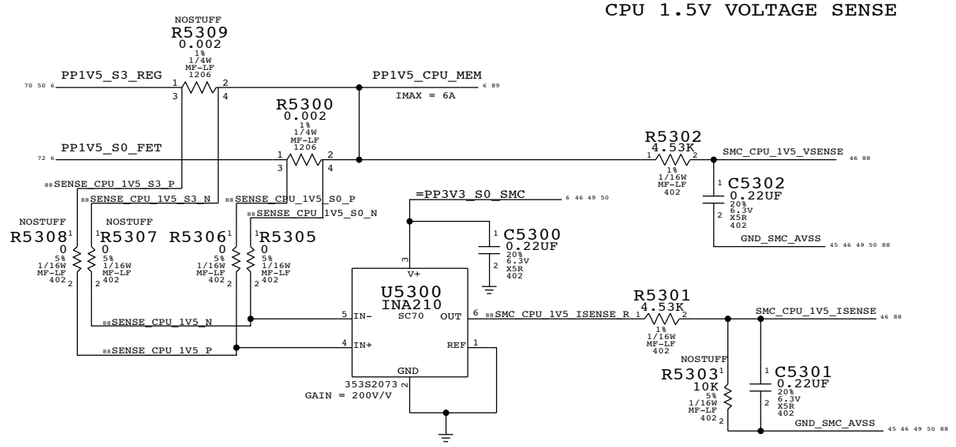
REVISION G.0.0

BRANCH

PAGE 52 OF 110

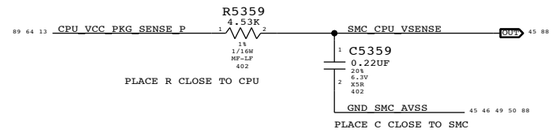
SHEET 48 OF 92

CPU 1.5V CURRENT SENSE

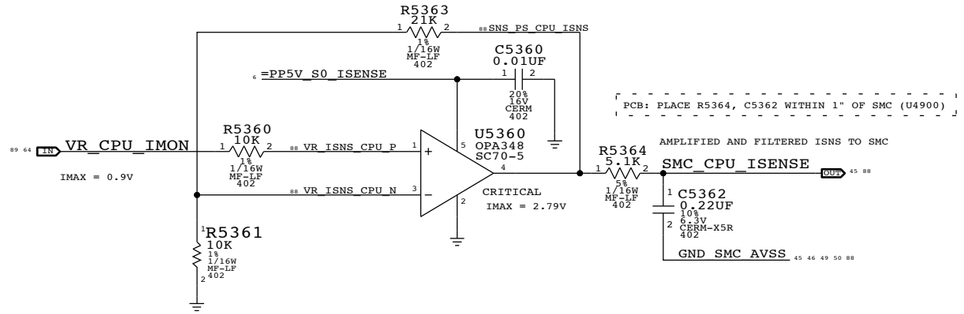


CPU 1.5V VOLTAGE SENSE

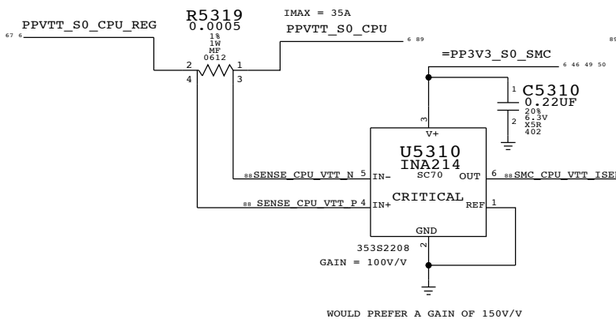
CPU Voltage Sense / Filter



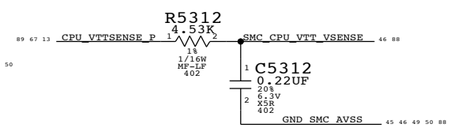
CPU CURRENT SENSE AMP & FILTER

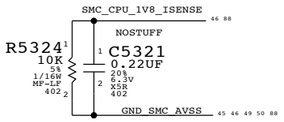


CPU VTT CURRENT SENSE



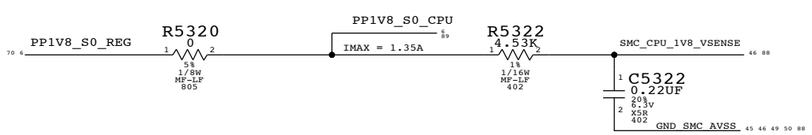
CPU VTT VOLTAGE SENSE





CPU 1.8V CURRENT SENSE

CPU 1.8V VOLTAGE SENSE



SYNC MASTER=K60 JERRY SYNC DATE=07/01/2009

PAGE TITLE: CPU POWER SENSE

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

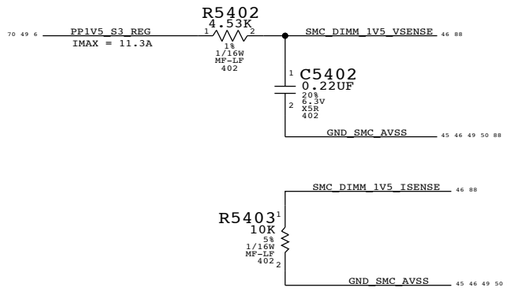
REVISION: G.0.0

BRANCH:

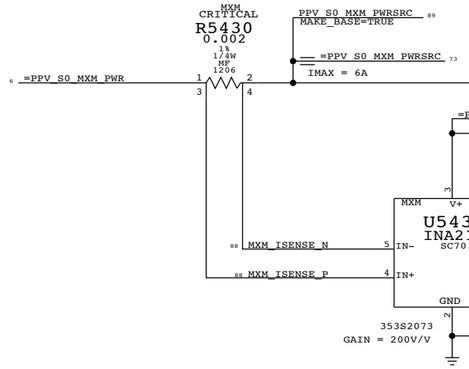
PAGE: 53 OF 110

SHEET: 49 OF 92

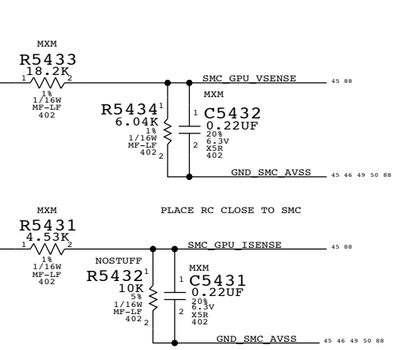
1.5V S3 VOLTAGE SENSE



MXM PWRSRC CURRENT SENSE



MXM PWRSRC VOLTAGE SENSE



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

GRAPHICS / DIMM POWER SENSE

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

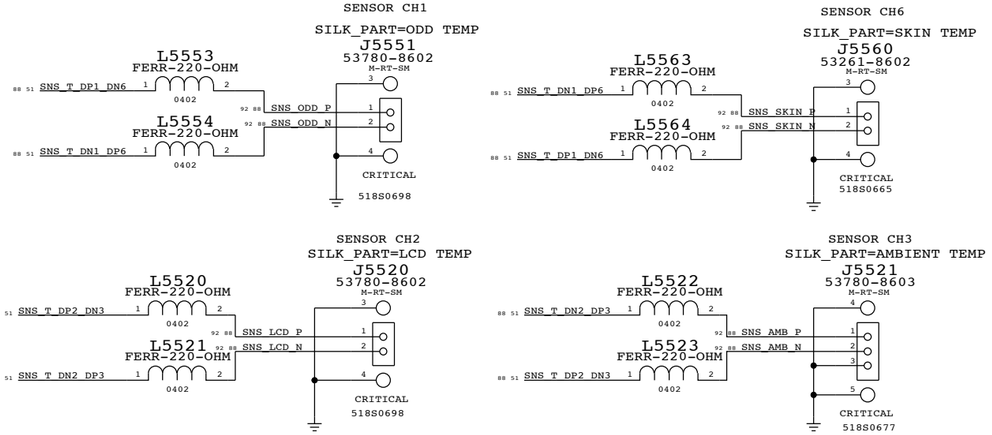
REVISION G.0.0

BRANCH

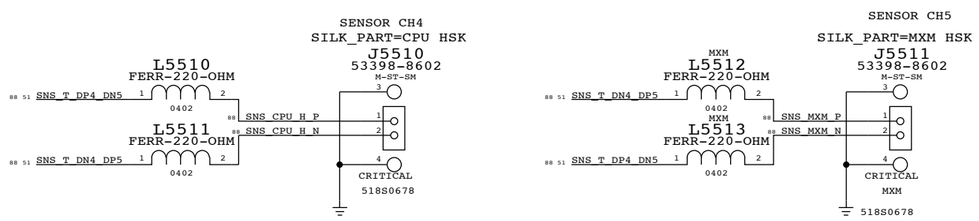
PAGE 54 OF 110

SHEET 50 OF 92

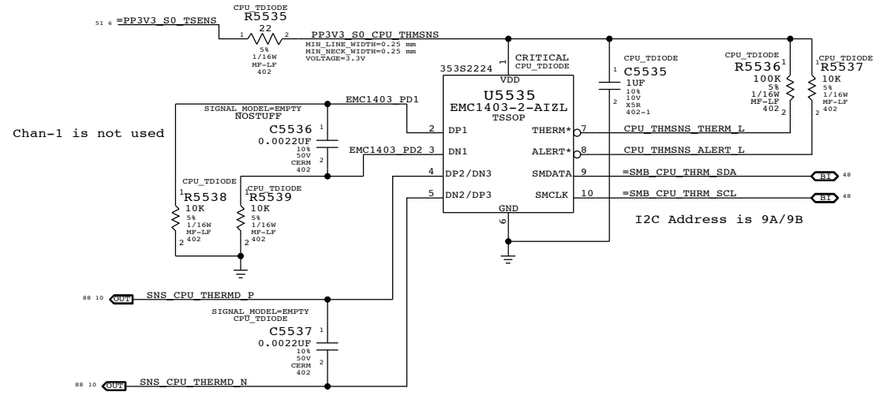
REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD



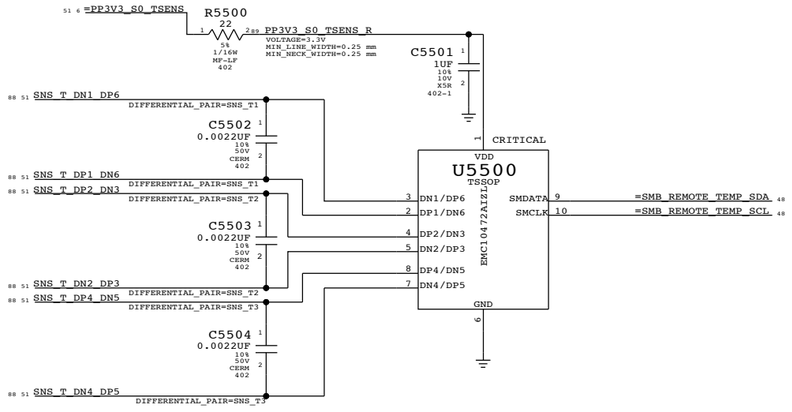
PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU



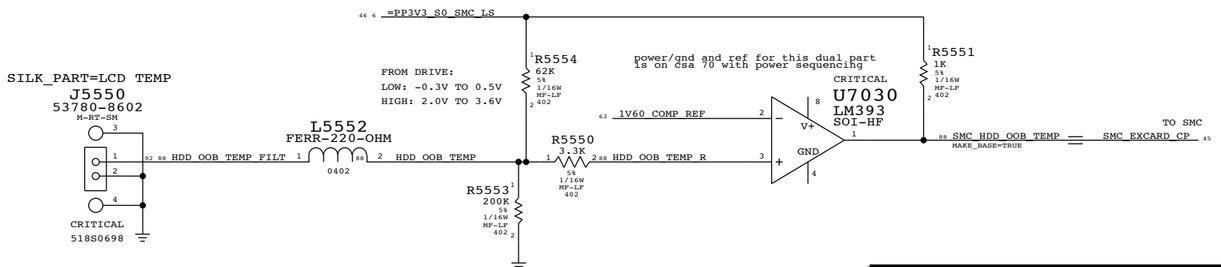
CPU T-DIODE THERMAL SENSOR



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



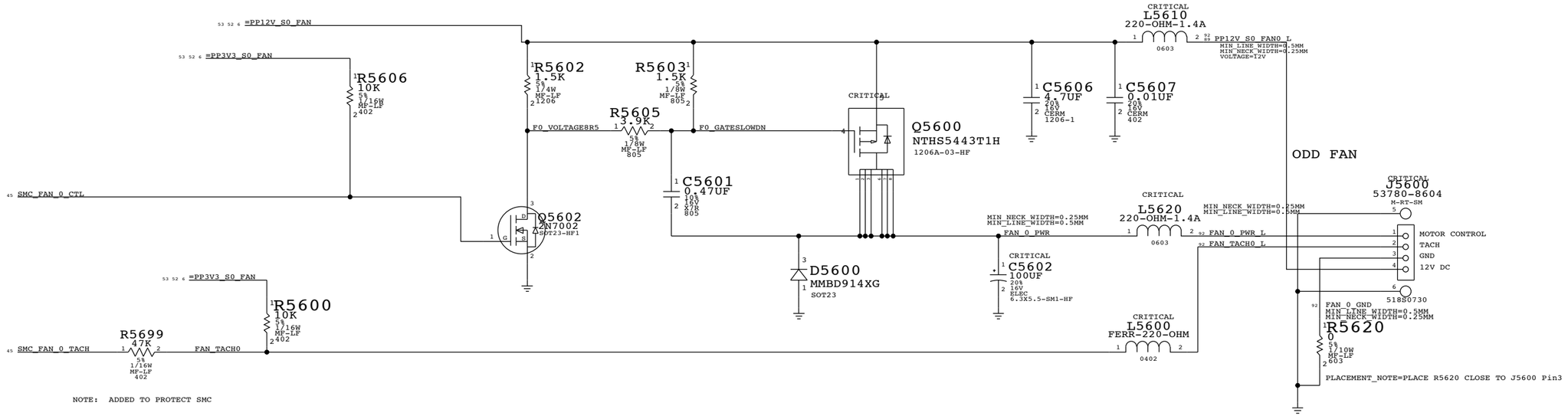
SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE: Thermal Sensors

Apple Inc.

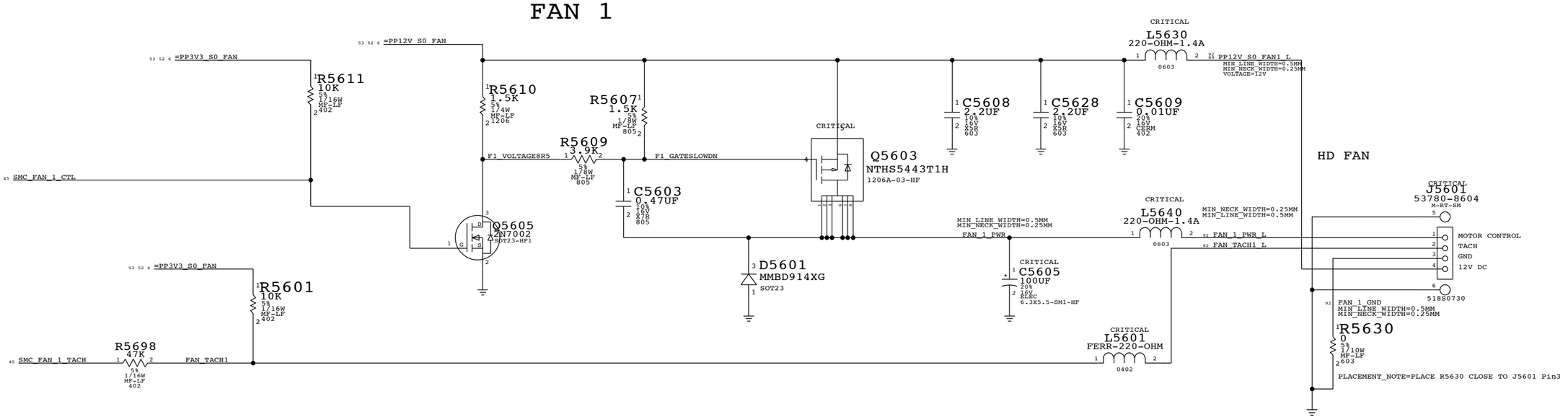
DRAWING NUMBER: 051-8233 SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 55 OF 110
SHEET: 51 OF 92

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

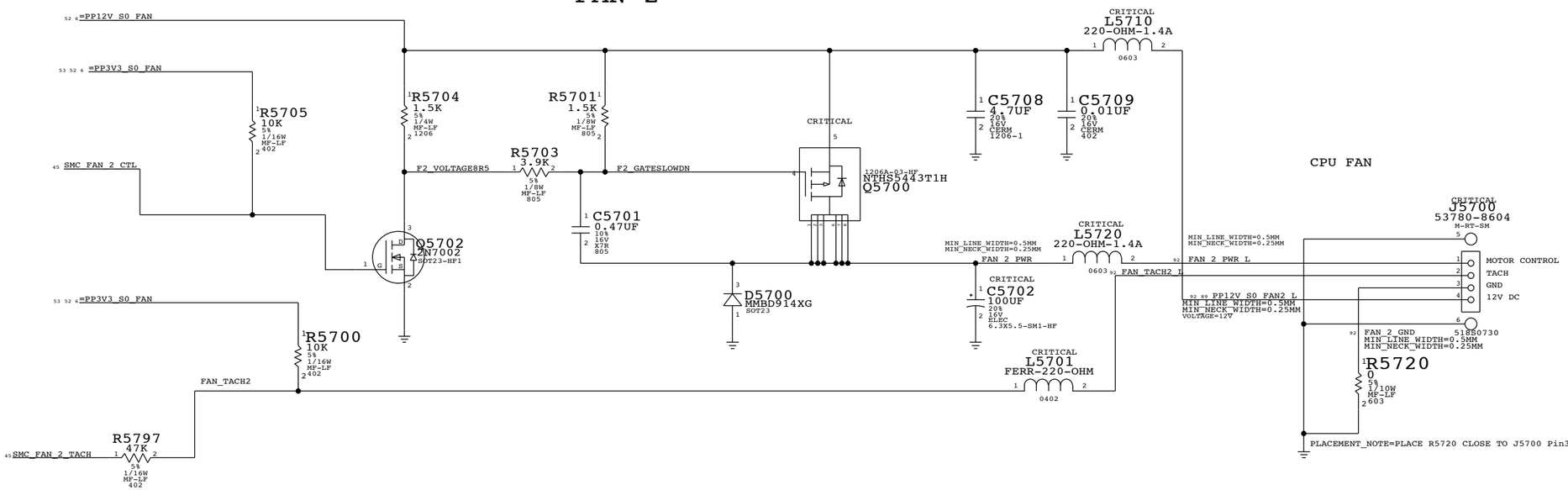
REVISION: G.0.0

BRANCH:

PAGE: 56 OF 110

SHEET: 52 OF 92

FAN 2



SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

PAGE TITLE: CPU FAN

Apple Inc.

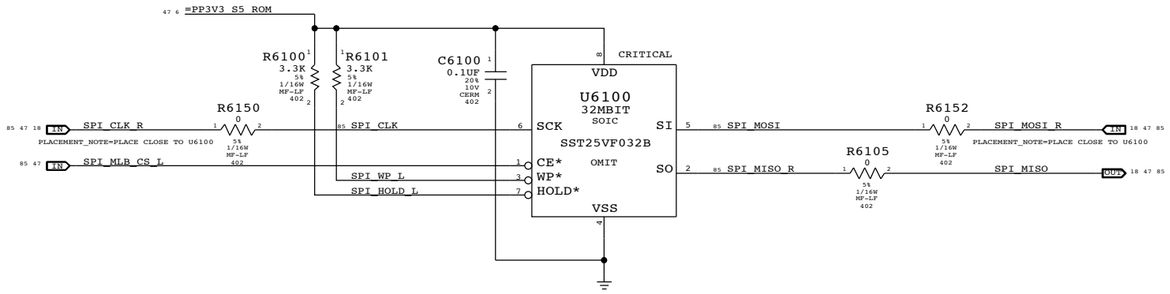
DRAWING NUMBER: 051-8233 SIZE: D

REVISION: G.0.0

BRANCH:

PAGE: 57 OF 110

SHEET: 53 OF 92



SYNC MASTER=K60 SIJI	SYNC DATE=07/01/2009
PAGE TITLE: SPI ROM	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
	REVISION: G.0.0
	BRANCH:
	PAGE: 61 OF 110
	SHEET: 54 OF 92

AUDIO CODEC
APPLE P/N 353S2592

=PP1V5_S0_AUD_DIG

C6203 4.7UF 20% 6.3V X5R 402
C6258 0.47UF 10% 10V X5R 402
C6260 10UF 20% 16V POLY-TANT CASE-B2-SM
C6261 0.47UF 10% 10V X5R 402
C6262 10UF 20% 16V POLY-TANT CASE-B2-SM
C6259 1UF 10% 10V X5R 402-1
C6264 0.47UF 10% 10V X5R 402
C6265 0.47UF 10% 10V X5R 402
C6213 CRITICAL 10UF 20% 6.3V X5R 603

=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG VOLTAGE=4.5V MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM
GND_AUDIO_HP_AMP_L
GND_AUDIO_CODEC

GND_AUDIO_HP_AMP_L
PP4V5_AUDIO_ANALOG
R6255 2.67K 1% 1/16W MF-LF 402
C6204 10UF 20% 6.3V X5R 603
C6205 10UF 20% 6.3V X5R 603

K22 = NC
K23 LOW = S/PDIF IN, HIGH = DP SPDIF

AUD_MUX_CNTRL
AUD_GPIO_1
AUD_GPIO_2
AUD_GPIO_3
AUD_SENSE_A

VBIAS_DAC
CS4206_FP
CS4206_FN

U6201 CS4206ACNZC QFN

2	GPIO0/DMIC_SDA1				
12	GPIO1/DMIC_SDA2/SPDIF_OUT2				
14	GPIO2				
15	GPIO3				
13	SENSE_A				
29	VBIAS_DAC				
44	VHP_FILT+	CRITICAL	HPOUT_L	38	MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
41	VHP_FILT-		HPOUT_R	40	MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
			HPREF	39	MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM
45	FLYP		LINEOUT_L1+	35	
43	FLYC		LINEOUT_L1-	34	
42	FLYN		LINEOUT_R1+	36	
3	VL_HD		LINEOUT_R1-	37	
1	VL_IF		LINEOUT_L2+	31	
			LINEOUT_L2-	30	
			LINEOUT_R2+	32	
			LINEOUT_R2-	33	
			MICBIAS	16	
			VCOM	28	CS4206_VCOM
6	BITCLK		LINEIN_L+	21	
10	SYNC		LINEIN_C-	22	
8	SDI		LINEIN_R+	23	
5	SDO		MICIN_L+	18	
11	RESET*		MICIN_L-	17	
47	SPDIF_IN		MICIN_R+	19	
48	SPDIF_OUT		MICIN_R-	20	
			VREF+_ADC	27	CS4206_VREF_ADC NC
			DMIC_SCL	4	TP_AUD_DMIC_CLK NC
7	DGND				
49	THRM_PAD				
26	AGND				
9	VD				
24	VA_REF				
46	VA_HP				
25	VA				

AUD_HP_PORT_L
AUD_HP_PORT_R
AUD_HP_PORT_REF
AUD_LO1_P_L
TP_AUD_LO1_N_L NC
AUD_LO1_P_R
TP_AUD_LO1_N_R NC
AUD_LO2_P_L
TP_AUD_LO2_N_L NC
AUD_LO2_P_R
TP_AUD_LO2_N_R NC
AUD_CODEC_MICBIAS

CS4206_FLYP
CS4206_FLYC
CS4206_FLYN
C6206 2.2UF 20% 6.3V CERM 402-LF
C6208 2.2UF 20% 6.3V CERM 402-LF

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
AUD_SPDIF_IN_CODEC
AUD_SPDIF_OUT
AUD_SPDIF_CHIP
R6254 22 5% 1/16W MF-LF 402
AUD_SDI_R
R6257 22 5% 1/16W MF-LF 402

AUD_LI_P_L
AUD_LI_COM MAKE_BASE=TRUE
AUD_LI_P_R
AUD_LI_N_L
AUD_LI_N_R
AUD_MIC_INP_L
AUD_MIC_INN_L
AUD_MIC_INP_R
AUD_MIC_INN_R

R6295 100K 1% 1/16W MF-LF 402
NOSTUFF R6263 0 5% 1/16W MF-LF 402
CRITICAL C6211 1UF 10% 20V TANT CASE-P3-HF
CRITICAL C6263 10UF 20% 16V POLY-TANT CASE-B2-SM
NOSTUFF R6267 100K 5% 1/16W MF-LF 402

GND_AUDIO_CODEC
XW6201 SM
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
VOLTAGE=0V
GND_AUDIO_HP_AMP_L

HP OUT ZOBEL NETWORK
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
AUD_HP_PORT_L
AUD_HP_PORT_R
C6298 0.1UF 10% 16V X7R-CERM 402
C6297 0.1UF 10% 16V X7R-CERM 402
AUD_Z_R NC
AUD_Z_L NC
R6296 39 5% 1/16W MF-LF 402
R6297 39 5% 1/16W MF-LF 402
GND_AUDIO_HP_AMP_L

BETTER
R6299 100K 5% 1/16W MF-LF 402
AUD_GPIO_1
EDUCATION
R6298 10K 5% 1/16W MF-LF 402

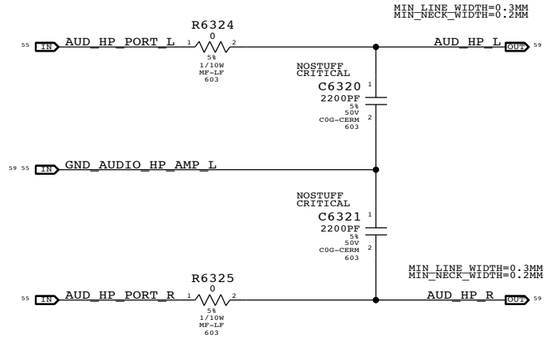
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

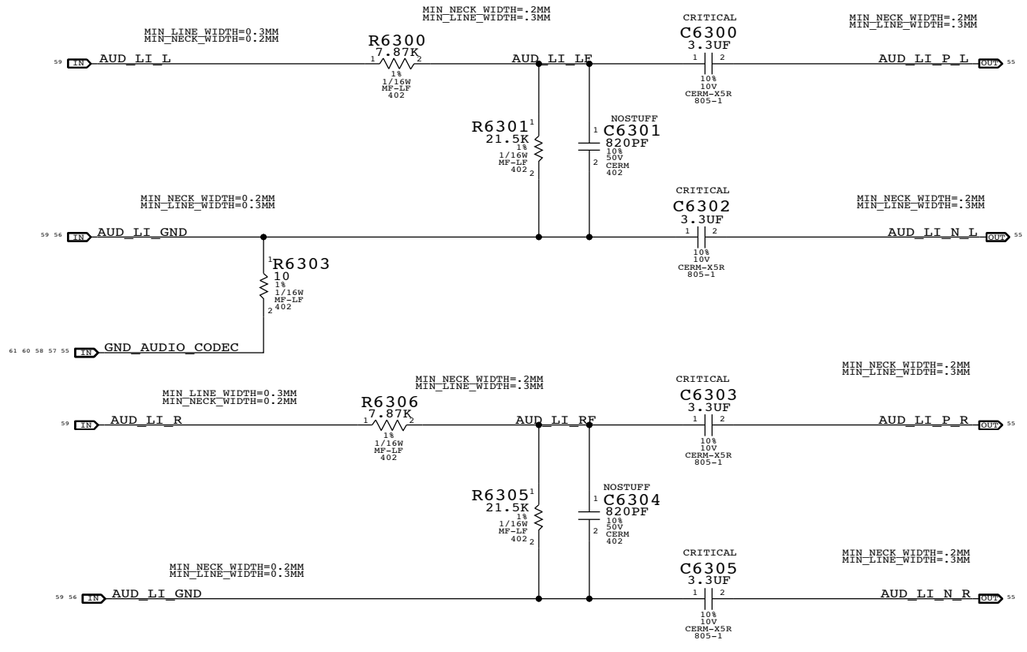
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V
L6201 FERR-220-OHM 0402
=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
R6201 2.21K 1% 1/16W MF-LF 402
4V5_REG_IN
4V5_REG_EN
VR6201 TPS71745 SON CRITICAL
IN OUT EN NR/FB GND NC
4V5_NR
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V
PP4V5_AUDIO_ANALOG
C6201 1UF 10% 10V X5R 402-1
C6202 1UF 10% 10V X5R 402-1
C6266 0.1UF 10% 16V X7R-CERM 402
C6207 1UF 10% 10V X5R 402-1
GND_AUDIO_CODEC

SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009
PAGE TITLE: AUDIO: CODEC/REGULATOR
Apple Inc.
DRAWING NUMBER: 051-8233 SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 62 OF 110
SHEET: 55 OF 92

1ST ORDER DAC FILTER PLACEHOLDER



CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC MASTER=K23 SKIP SYNC DATE=07/16/2009

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

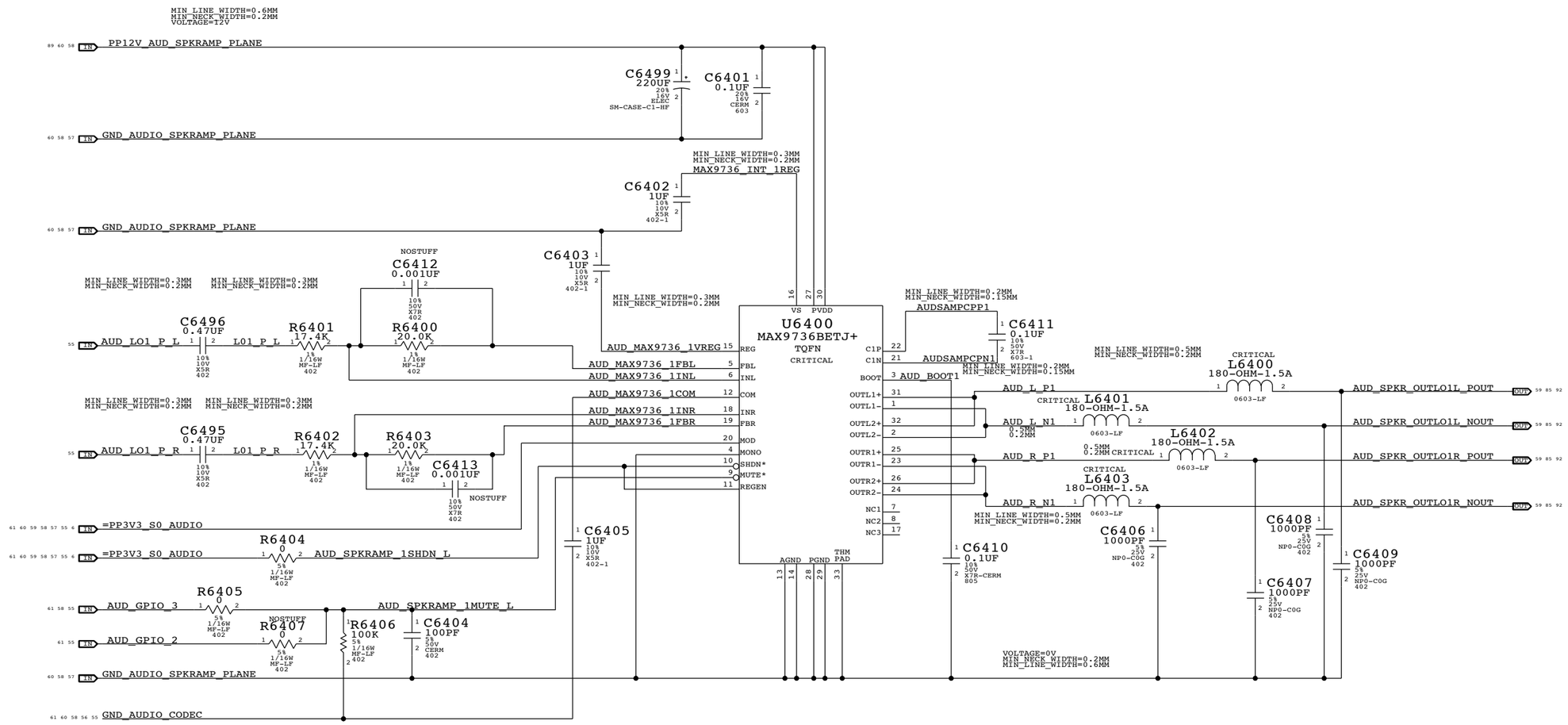
DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 63 OF 110
SHEET 56 OF 92

TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC MASTER=K23 SKIP
SYNC DATE=07/16/2009

PAGE TITLE
AUDIO: Tweeter Amp 1

Apple Inc.

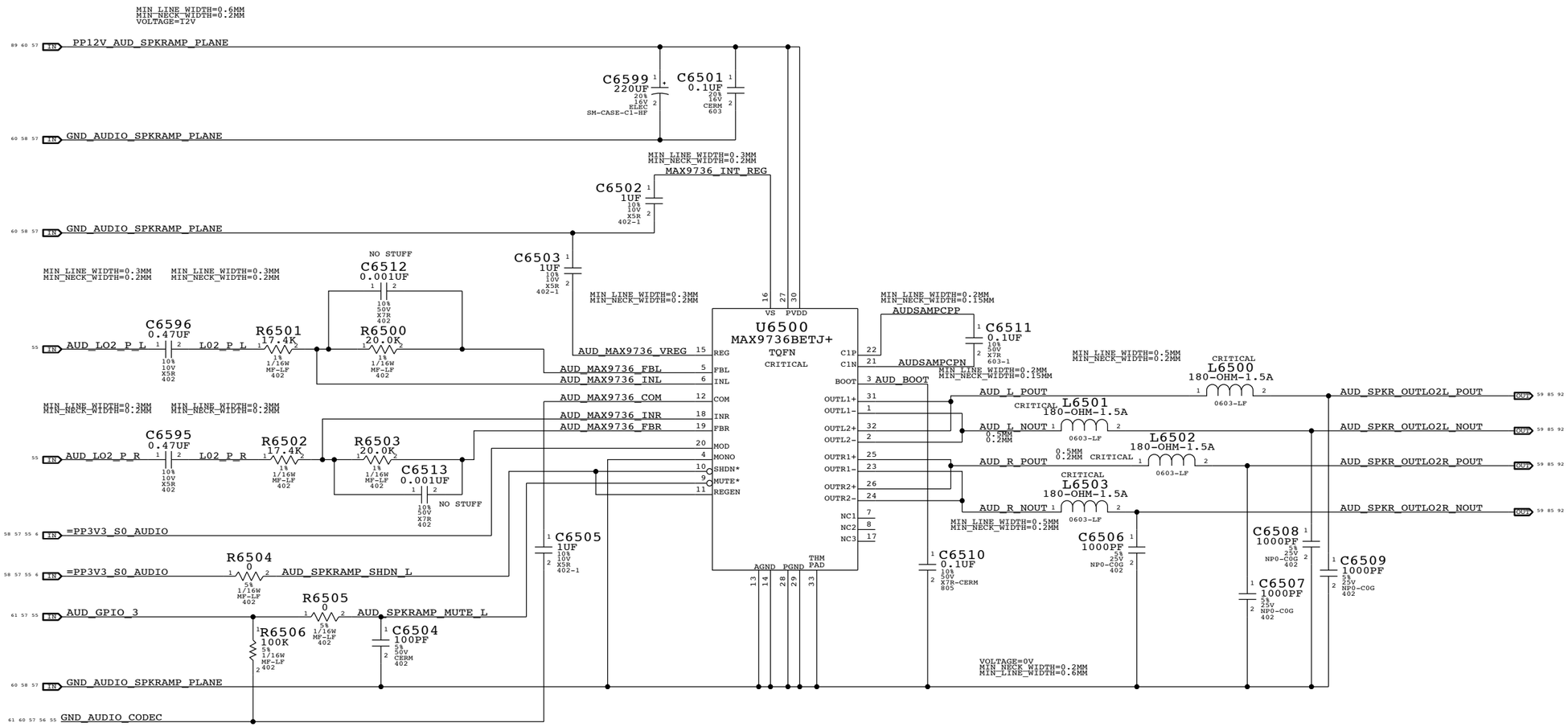
DRAWING NUMBER 051-8233
SIZE D
REVISION G.0.0
BRANCH
PAGE 64 OF 110
SHEET 57 OF 92

WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



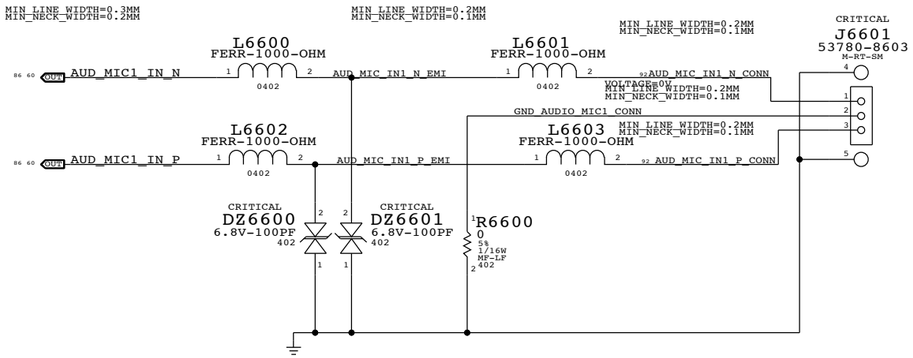
SYNC MASTER=K23 SKIP
SYNC DATE=07/16/2009

PAGE TITLE
AUDIO: Woofer Amp

Apple Inc.

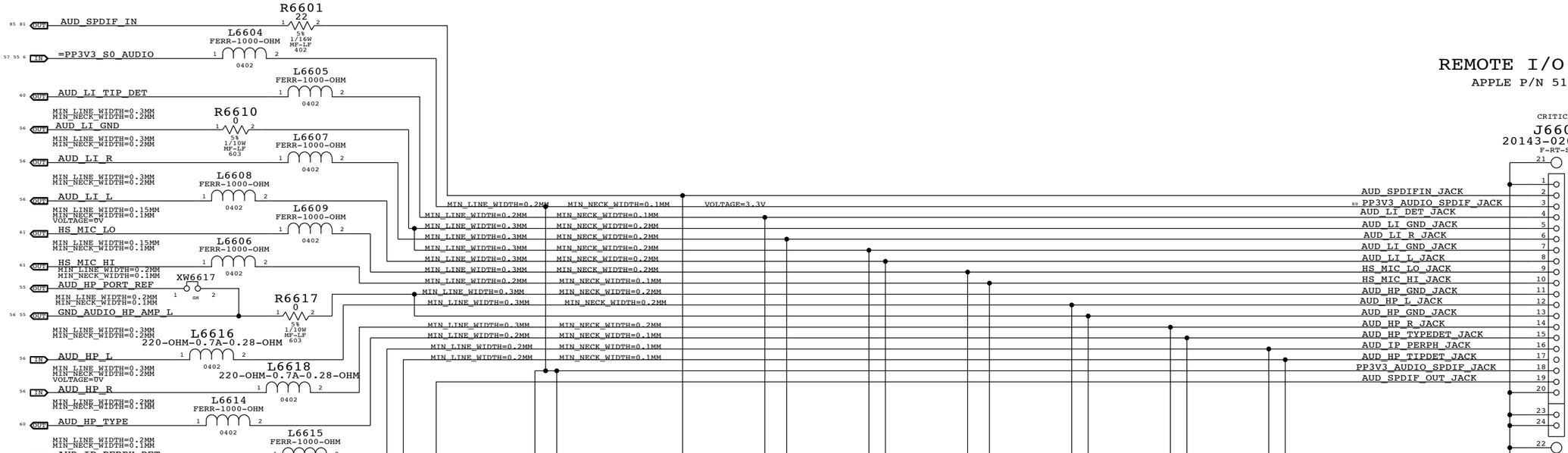
DRAWING NUMBER 051-8233
SIZE D
REVISION G.0.0
BRANCH
PAGE 65 OF 110
SHEET 58 OF 92

INTERNAL MIC CON
APPLE P/N 518S0677



SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

REMOTE I/O CONNECTOR
APPLE P/N 518S0723



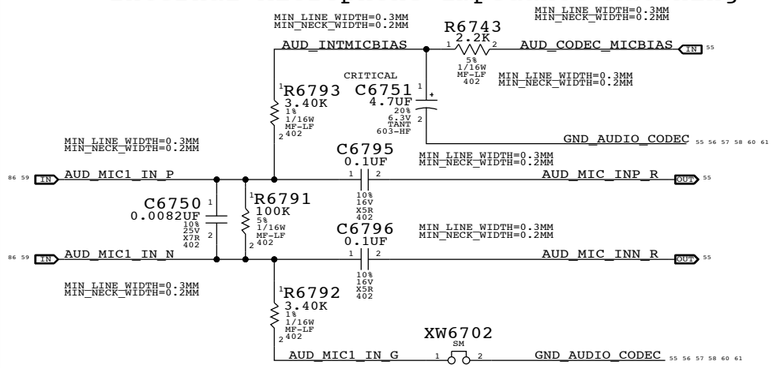
SYNC_MASTER=K60 SYNC_DATE=06/05/2009

PAGE TITLE
Audio: MLB to I/O Conn.

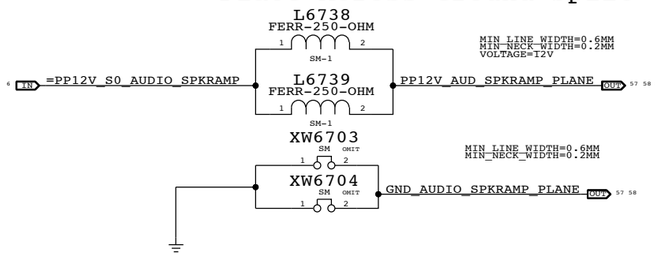
Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 66 OF 110
SHEET 59 OF 92

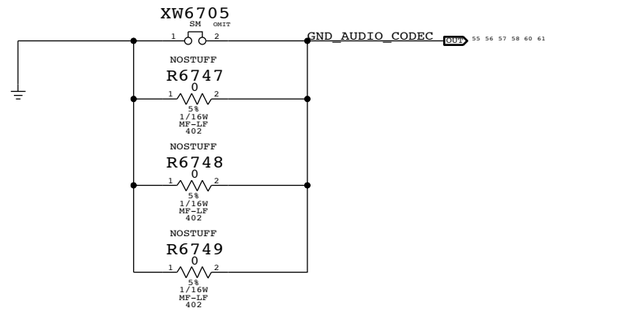
Internal Microphone Impedance Matching



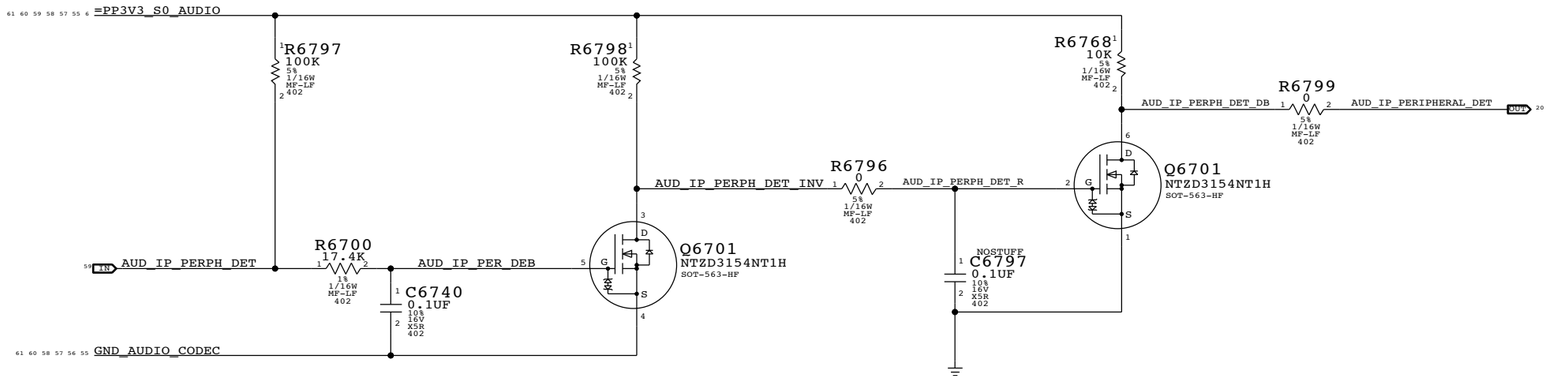
Place Across Ground Split



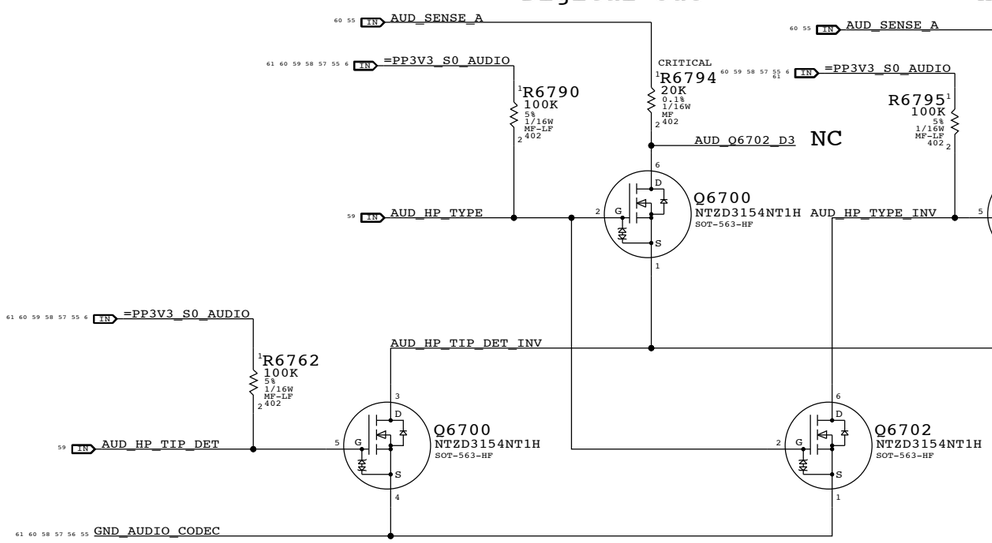
Audio Ground Returns



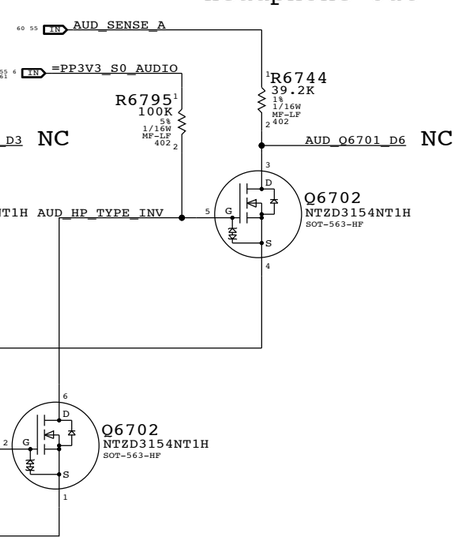
IPHS HS Detect Debounce CKT



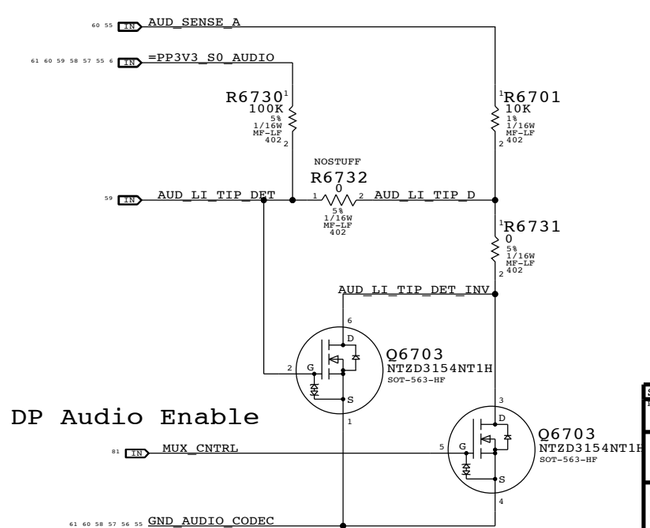
Digital Out



Headphone Out



LI Insert Detect



DP Audio Enable

SYNC MASTER=K23 SKIP | SYNC DATE=07/16/2009

PAGE TITLE: AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER: 051-8233 | SIZE: D

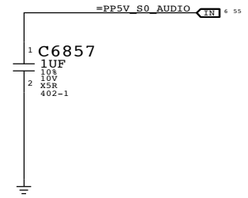
REVISION: G.0.0

BRANCH:

PAGE: 67 OF 110

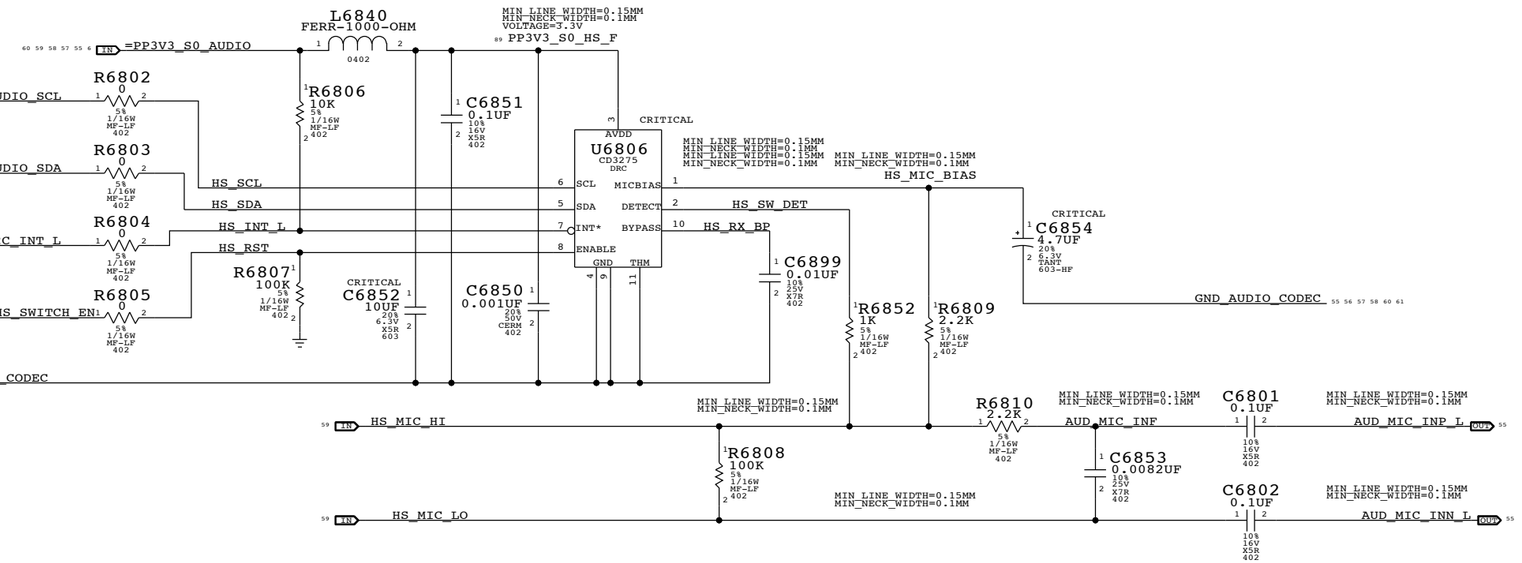
SHEET: 60 OF 92

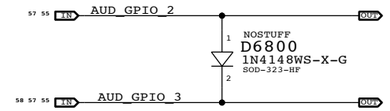
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5



MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256





FLP = 8.82 KHZ
FHP = 80 HZ

SYNC MASTER=K23 SKIP SYNC DATE=07/16/2009

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 68 OF 110

SHEET 61 OF 92

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

R6901 0 5% 1/16W MF-LF 402
91 45 IN PM_RSMRST_L 1 — 2 PM_RSMRST_PCH_L OUT 19 91

SLP_S4 ENABLES

MEMVTT_EN SEQUENCE

72 63 62 6 5 =PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
R6953 0 5% 1/16W MF-LF 402
DDRVTT_EN 32 62 70 91
NOSTUFF C6951 100PF 5% 50V CERM 402
VTT_REG_PGOOD_R2
VTT_REG_PGOOD_R1
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6953 0.1UF 10% 16V X5R 402
67 63 62 11 91 CPUVTT_REG_PGOOD
R6950 100K 5% 1/16W MF-LF 402
CPUVTT_RP_R
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

63 62 6 5 =PP3V3_S5_PWRCTL
C6910 0.1UF 20% 10V CERM 402
91 19 PM_SLP_S4_L_L
U6900 08 74LVC08 TSSOP-HF
S4_ENABLES
R6911 33 5% 1/16W MF-LF 402 — P3V3S3_EN 72 91 Enable FET
R6912 33 5% 1/16W MF-LF 402 — P5VS3_EN 69 91 ENABLE REGULATOR
R6914 33 5% 1/16W MF-LF 402 — P12V_S3_EN 72 91 Enable FET
NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6923 0.47UF 10% 6.3V CERM-X5R 402

63 62 6 5 =PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
Q6910 2N7002DW-X-G SOT-363
11 CPU_SKTOCC_L
NOSTUFF R6917 0 5% 1/16W MF-LF 402
PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

6 =PP5V_S3_PWRCTL
R6910 100K 5% 1/16W MF-LF 402
69 P5VS3_REG_PGOOD MAKE_BASE=TRUE
PM_EN_USB_PWR 43
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402
=DDRREG_EN 70

SLP_M ENABLES

THIS SLP_M CIRCUIT IS A BACKUP IN CASE
VCC_ME IS REQUIRED IN ANY STATE
OTHER THAN S0. DELETE AFTER PROTO1

NOSTUFF R6920 33 5% 1/16W MF-LF 402 — Enable FET P3V3ME_EN 72 91
PLACE SERIES R'S NEAR SOURCE

91 19 5 PM_SLP_M_L
R6922 1K 5% 1/16W MF-LF 402
P1V05_ME_SM_EN 72 91 Enable FET
R6927 0 5% 1/16W MF-LF 402
72 63 62 6 5 =PP3V3_S0_PWRCTL
72 63 62 6 5 =PP3V3_S5_PWRCTL
C6925 1UF 10% 6.3V CERM 402
P1V05_SM_DIS_L
62 PM_SLP_S3_BUF_L
R6925 10K 5% 1/16W MF-LF 402
PM_SLP_S3_B_R
PCHCORE_PGOOD_R
74LVC08 TSSOP-HF U6900 08
P1V05_ME_SM_DIS
Q6910 2N7002DW-X-G SOT-363
68 63 62 5 91 PCHCORE_REG_PGOOD
R6926 10K 5% 1/16W MF-LF 402
C6926 1UF 10% 6.3V CERM 402

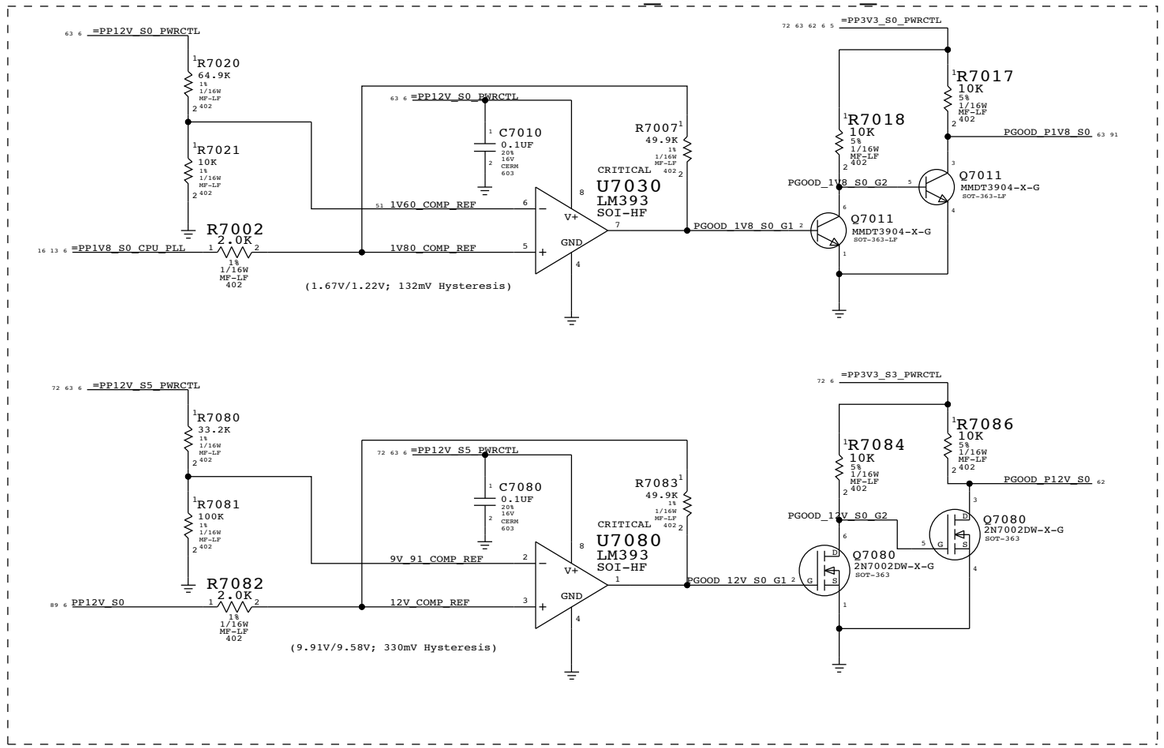
SLP_S3 ENABLES

63 62 6 5 =PP3V3_S5_PWRCTL
91 63 46 37 33 32 19 5 PM_SLP_S3_L
74LVC08 TSSOP-HF U6900 08 (PM_SLP_S3_L_BUF)
MAKE_BASE=TRUE
R6946 33 5% 1/16W MF-LF 402 — P3V3S0_EN Enable FET OUT 72 91
R6947 33 5% 1/16W MF-LF 402 — P5VS0_EN Enable FET OUT 72 91
OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)
63 PGOOD_P12V_S0
R6944 10K 1% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
PM_SLP_S3_BUF_L 62
91 70 5 PM_PGOOD_DDRREG_S3
R6948 0 5% 1/16W MF-LF 402
switch to alias after proto1
Enable FET P1V5_S0_EN 72 91
DDRVTT_EN 32 62 70 91 Enable regulator
NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

72 63 62 6 5 =PP3V3_S0_PWRCTL
R6942 10K 5% 1/16W MF-LF 402
Enable regulator PCHCORE_REG_EN
PCHCORE VREG
68 91 91 68 63 62 5 PCHCORE_REG_PGOOD MAKE_BASE=TRUE
ENABLE FET P1V05_ME_S0_EN 72
91 72 PGOOD_P5V_S0 MAKE_BASE=TRUE
C6942 1UF 10% 6.3V CERM 402
R6949 0 5% 1/16W MF-LF 402
Enable regulator CPUVTT_REG_EN
CPUVTT VREG
67 91 91 67 63 62 11 CPUVTT_REG_PGOOD MAKE_BASE=TRUE
Enable regulator PM_EN_PVCORE_CPU 64 TO ENABLE OF CPU VREG
switch to alias after proto1

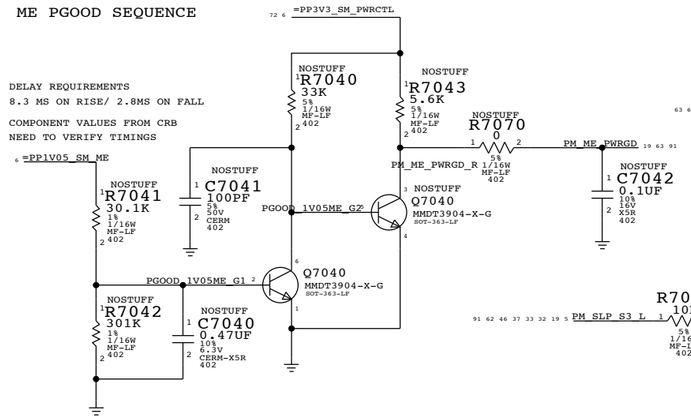
SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009
PAGE TITLE
POWER SEQUENCING ENABLES
Apple Inc.
DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 69 OF 110
SHEET 62 OF 92

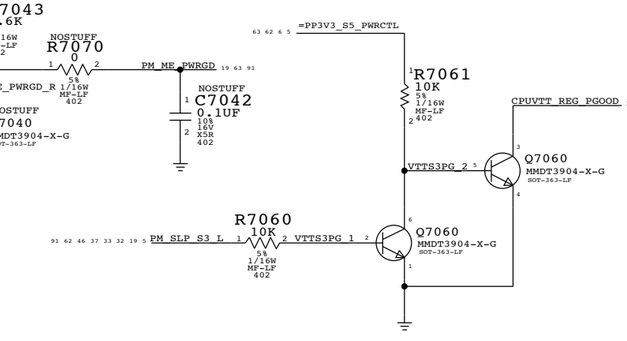
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0



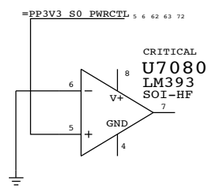
S0 RAILS PGOOD

ME PGOOD SEQUENCE

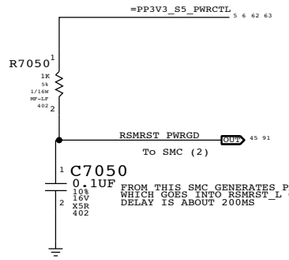




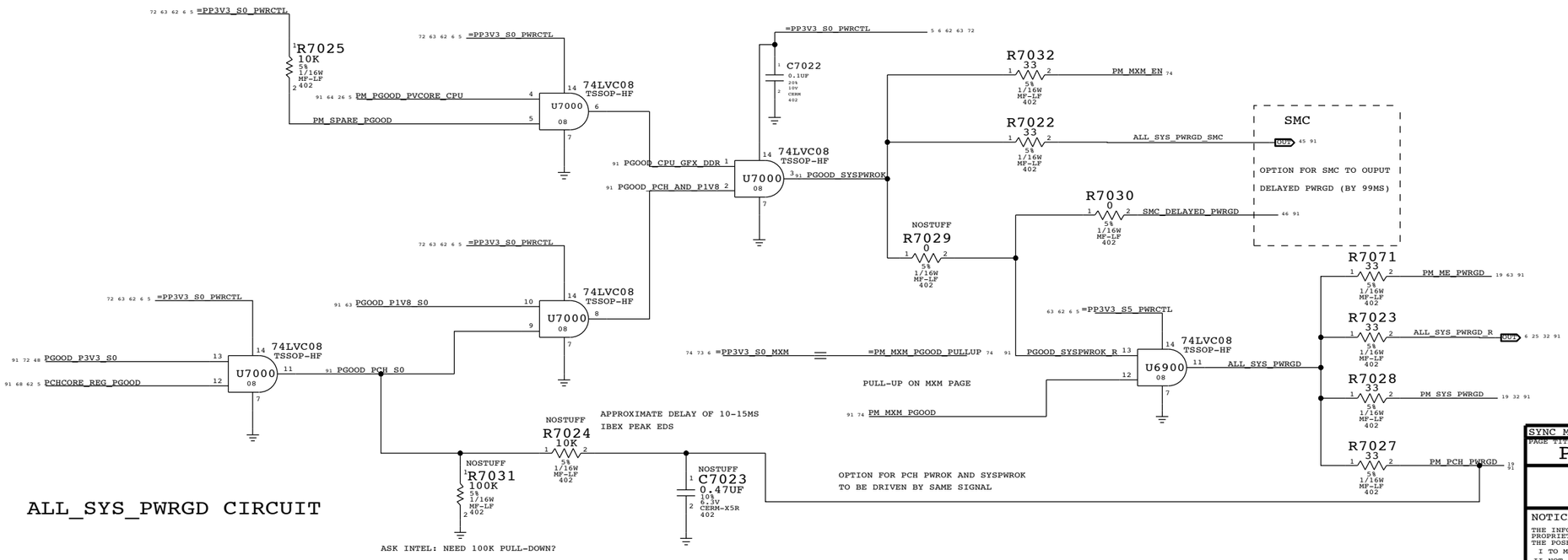
DISABLE CPUVTT_REG_PGOOD WHEN SLP_S3_L = 0 (PER PIKETON PDG)



SPARE



ALL_SYS_PWRGD CIRCUIT



SYNC MASTER=K60 MIKE	SYNC DATE=07/01/2009
PAGE TITLE	POWER SEQUENCING PGOOD
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION G.0.0
	BRANCH
	PAGE 70 OF 110
	SHEET 63 OF 92

CPU CORE REG 1.1V/110A O/P= PPVCORE_S0_CPU_REG

CPU VCORE
VOUT = VCORE
PEAK = 110A
AVG = 90A

=PP5V_S0_VRD
PPVCORE_S0_CPU_REG
CPU_VCC_PKG_SENSE_P
CPU_VCC_PKG_SENSE_N
1.25 mOhm loadline
SIGNAL_MODEL=EMPTY
VR_CPU_VSEN
VR_CPU_RGND
AGND_CPU
PP5V_S0_CPU_VCORE_VCC
R7118 2.2 1% 1/8W MF-LF 805
MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=5V
LOCAL 5V
VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.
LAYOUT: PLACE RT7101 NEAR HOT SPOT.
PM_EN_PVCORE_CPU
=PP3V3_S0_VRD
=PPVTT_S0_CPU
PM_PGOOD_PVCORE_CPU
VR_CPU_IOUT
CPU_PSI_L
CPU_VID<7..0>
=PP12V_S0_VRD
IMAX = 10.5A
CRITICAL
L7100
0.36UH-45A-0.76MOHM
MSQ1211R36LF-TH
152-0104
PP12V_S0_CPU_FLTRD
NET_PHYSICAL_TYPE=POWER
VOLTAGE=12V
CPU VCORE CONTROLLER
CPU VCORE INPUT Filtering

CRITICAL
U7100
ISL6334
QFN
SYM_VER_2

VR_CPU_PWM1
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N
VR_CPU_PWM2
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N
VR_CPU_PWM3
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N
VR_CPU_PWM4
VR_CPU_ISNS4_P
VR_CPU_ISNS4_N

SYNC MASTER=K61 JERRY SYNC DATE=07/16/2009
PAGE TITLE: VREG: PPVCORE_S0_CPU
Apple Inc.
DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 71 OF 110
SHEET 64 OF 92

SYNC MASTER=K60 JERRY	SYNC DATE=07/01/2009
PAGE TITLE: VREG: CPU CORE - PHASES 1-3	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
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PHASE 4

PP12V_S0_CPU_FLTRD

R7311 10 5% 1/10W MF-LF 603
R7312 NOSTUFF 0 5% 1/10W MF-LF 603
R7313 10 5% 1/10W MF-LF 603

VR_CPU_DRV4_VCC
VR_CPU_DRV4_UVCC
VR_CPU_DRV4_PVCC

C7312 1UF 10% 16V X5R 603
C7310 NOSTUFF 1UF 10% 16V X5R 603
C7311 1UF 10% 16V X5R 603

U7301 ISL6612 QFN1
VCC PVCC PWM BOOT UGATE PHASE LGATE NC NC GND THRML PAD

VR_CPU_PWM4
VR_CPU_DRV4_GDSEL
R7310 NOSTUFF 0 5% 1/10W MF-LF 603

VR_CPU_DRV4_BOOT DIDT=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_DRV4_UGATE DIDT=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY
VR_CPU_PHASE4 DIDT=TRUE NET_PHYSICAL_TYPE=POWER
VR_CPU_DRV4_LGATE DIDT=TRUE NET_PHYSICAL_TYPE=VR_CTL_PHY

VR_CPU_BOOT4_RC NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
R7303 0 5% 1/10W MF-LF 603
C7303 0.22UF 10% 16V X7R 603

376S0772
CRITICAL Q7301 IRF6710 S1

CRITICAL Q7302 IRF6795 DIRECTFET-MX
376S0771

CRITICAL L7301 0.36UH-35A MSQ1208-TH 152-0114
PPVCORE_S0_CPU_REG4

NOSTUFF R7302 2.2 5% 1/8W MF-LF 805
VR_CPU_PH4_SNUB NET_PHYSICAL_TYPE=VR_CTL_PHY DIDT=TRUE
C7302 0.001UF 10% 50V CERM 402 NOSTUFF

THESE TWO CAPS ARE FOR EMC
CRITICAL C7304 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7305 10UF 10% 16V X5R-CERM 0805
CRITICAL C7306 10UF 10% 16V X5R-CERM 0805
C7307 1UF 10% 16V X5R 603
C7308 0.001UF 10% 50V X7R 402
C7309 0.001UF 10% 50V X7R 402

CRITICAL R7301 0.0005 1% 1W MF 0612

PPVCORE_S0_CPU_REG
VR_CPU_ISNS4_XW_N
VR_CPU_ISNS4_XW_P

OMIT XW7301 SM SIGNAL_MODEL=EMPTY
OMIT XW7302 SM SIGNAL_MODEL=EMPTY

VR_CPU_ISNS4_P
VR_CPU_ISNS4_N

PPVCORE_S0_CPU_REG

C7330 C7331 C7332 C7333 C7334 C7335 C7336 C7337 C7338 C7339
0.1UF 20% 10V CERM 402

C7340 C7341 C7342 C7343 C7344 C7345 C7346 C7347 C7348 C7349
1UF 10% 16V X5R 603

SYNC MASTER=K61 JERRY SYNC DATE=07/16/2009
PAGE TITLE
VREG: CPU CORE - PHASE 4

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 73 OF 110
SHEET 66 OF 92

CPU VTT REG 1.1V/30A O/P= PPVTT_S0_CPU_REG

CPU VTT
VOUT = 1.1V OR 1.05V
PEAK = 35A
AVG = 30A

=PP12V_S0_CPU_VTT_VREG
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE

=PP5V_S0_CPU_VTT_VREG
NET_PHYSICAL_TYPE=POWER

R7462 4.7 5% 1/10W MF-LF 603

PP5V_CPUVTT_VR

CPUVTT_REG_PGOOD
"PULL-UP" TO VTT RAIL ON CPU PAGE

CPUVTT_REG_EN

OMIT
TH7401 0603-LF
10KOHM

R7405 35.7K 1% 1/16W MF-LF 402
R7406 35.7K 1% 1/16W MF-LF 402
R7404 10.5K 1% 1/16W MF-LF 402
R7402 20.0K 1% 1/16W MF-LF 402
R7403 42.2K 1% 1/16W MF-LF 402
R7401 487 1% 1/16W MF-LF 402

VTT_REG_PHASE1
VTT_REG_PHASE2
VTT_ICOMP2
VTT_ICOMP1
VTT_REG_ICOMP
VTT_REG_ISUM
VTT_REG_IREF
VTT_REG_OCSET

NOSTUFF C7406 1000PF 5% 25V NP0-C0G 402
NOSTUFF C7405 1000PF 5% 25V NP0-C0G 402
C7403 0.012UF 10% 25V X7R 402
C7404 1000PF 5% 25V NP0-C0G 402
C7401 1.0UF 10% 16V X7R 805
C7402 1.0UF 10% 16V X7R 805

NET_PHYSICAL_TYPE=POWER

U7400 ISL6568 QFN
CRITICAL
VCC PVCC
ICOMP ISUM IREF RGND VSEN VDIFF VID4 VID3 VID2 VID1 VID0 VID12.5 REF FB COMP OFS
OCSET PGOOD ENLL BOOT1 UGATE1 PHASE1 LGATE1 FS BOOT2 UGATE2 PHASE2 LGATE2 ISEN1 ISEN2
THRM_PAD 33

PPVTT_S0_CPU_REG

NOSTUFF R7407 10 1% 1/16W MF-LF 402
R7408 4.99 1% 1/16W MF-LF 402
NOSTUFF R7409 1K 5% 1/16W MF-LF 402
NOSTUFF R7410 1K 5% 1/16W MF-LF 402
NOSTUFF R7411 1K 5% 1/16W MF-LF 402
NOSTUFF R7412 1K 5% 1/16W MF-LF 402
R7413 1K 5% 1/16W MF-LF 402
R7414 1K 5% 1/16W MF-LF 402

VID0=0, VID[4-1]=1, VTT VR o/p= 1.10V
Internal Pu on VID lines

(SELECT MODE= VRM10)

VTT_VID4 VTT_VID3 VTT_VID2 VTT_VID1 VTT_VID0 VTT_VID12P5

C7492 100PF 5% 50V CERM 402

R7430 0 5% 1/10W MF-LF 603
C7430 0.1UF 10% 16V X7R-CERM 402
VTT_REG_BOOT1_R
VTT_REG_ISEN1
R7432 1K 1% 1/16W MF-LF 402
R7431 0 5% 1/10W MF-LF 603
C7431 0.1UF 10% 16V X7R-CERM 402
VTT_REG_BOOT2_R
VTT_REG_ISEN2
R7433 1K 1% 1/16W MF-LF 402
R7434 88.7K 1% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE

Q7440 CRITICAL RJK0365DPA MLP5X6-LFPAK-WPAK
Q7450 CRITICAL RJK0365DPA MLP5X6-LFPAK-WPAK
Q7441 CRITICAL RJK0348DPA WPAK
Q7451 CRITICAL RJK0348DPA WPAK

VTT_REG_UGATE1
VTT_REG_LGATE1
VTT_REG_UGATE2
VTT_REG_LGATE2
VTT_REG_PHASE1
VTT_REG_PHASE2

C7442 CRITICAL 10UF 10% 16V X5R-CERM 1206
C7443 CRITICAL 1UF 10% 16V X5R 402
C7444 CRITICAL 10UF 10% 16V X5R-CERM 1206
C7445 CRITICAL 270UF 20% 16V ELEC 8X9-TH1
C7450 CRITICAL 10UF 10% 16V X5R-CERM 1206
C7451 CRITICAL 1UF 10% 16V X5R 402
C7452 CRITICAL 10UF 10% 16V X5R-CERM 1206
C7453 CRITICAL 270UF 20% 16V ELEC 8X9-TH1

L7441 CRITICAL 0.36UH-45A-0.76MOHM MSQ1211R36LF-TH
L7454 CRITICAL 0.36UH-45A-0.76MOHM MSQ1211R36LF-TH

SWITCHNODE
D7440 CRITICAL CTLSH3-30M833 TLM833
D7450 CRITICAL CTLSH3-30M833 TLM833

VTT_REG_PH1_SNUB
VTT_REG_PH2_SNUB
NOSTUFF R7440 1.1 1% 1/10W MF-LF 603
NOSTUFF R7455 1.1 1% 1/10W MF-LF 603
NOSTUFF C7440 1000PF 5% 25V NP0-C0G 402
NOSTUFF C7455 1000PF 5% 25V NP0-C0G 402

PPVTT_S0_CPU_REG
NET_PHYSICAL_TYPE=POWER

OUTPUT BULK DECOUPLING
C7460 CRITICAL 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7461 CRITICAL 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7462 CRITICAL 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM
C7463 CRITICAL 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

VTT_REG_COMP
VTT_REG_FB
C7417 390PF 10% 50V CERM 402
R7417 1.0K 1% 1/10W MF-LF 603
VTT_REG_VIDFF1
VTT_REG_VIDFF
R7416 3.01K 1% 1/16W MF-LF 402
C7416 0.022UF 10% 25V X7R 0402
VTT_REG_COMP1
C7418 4700PF 10% 50V CERM 603
VTT_REG_VIDFF2
R7418 100 1% 1/16W MF-LF 402
R7419 0 5% 1/16W MF-LF 402

R7421 100 1% 1/16W MF-LF 402
VTT_REG_RGND_1
OMIT XW7421
R7424 10 1% 1/16W MF-LF 402
VTT_REG_RGND
R7422 0 5% 1/16W MF-LF 402
CPU_VTTSENSE_R_N
CPU_VTTSENSE_N
PLACEMENT_NOTE=PLACE R7422 WITHIN 25.4MM OF CPU, NO STUBS.
PLACEMENT_NOTE=PLACE R7423 WITHIN 25.4MM OF CPU, NO STUBS.
NOSTUFF C7423 1000PF 5% 25V NP0-C0G 402
R7423 0 5% 1/16W MF-LF 402
CPU_VTTSENSE_R_P
CPU_VTTSENSE_P
R7425 10 1% 1/16W MF-LF 402
VTT_REG_VSEN
NOSTUFF C7426 100PF 5% 50V CERM 402
R7420 100 1% 1/16W MF-LF 402
VTT_REG_VSEN_1
PPVTT_S0_CPU_REG
OMIT XW7422

PP5V_CPUVTT_VR
NOSTUFF R7460 75K 1% 1/16W MF-LF 402
VTT_OFST
R7461 28K 1% 1/10W MF-LF 603

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0127	1	RES,68k,0603,5%	TH7401	

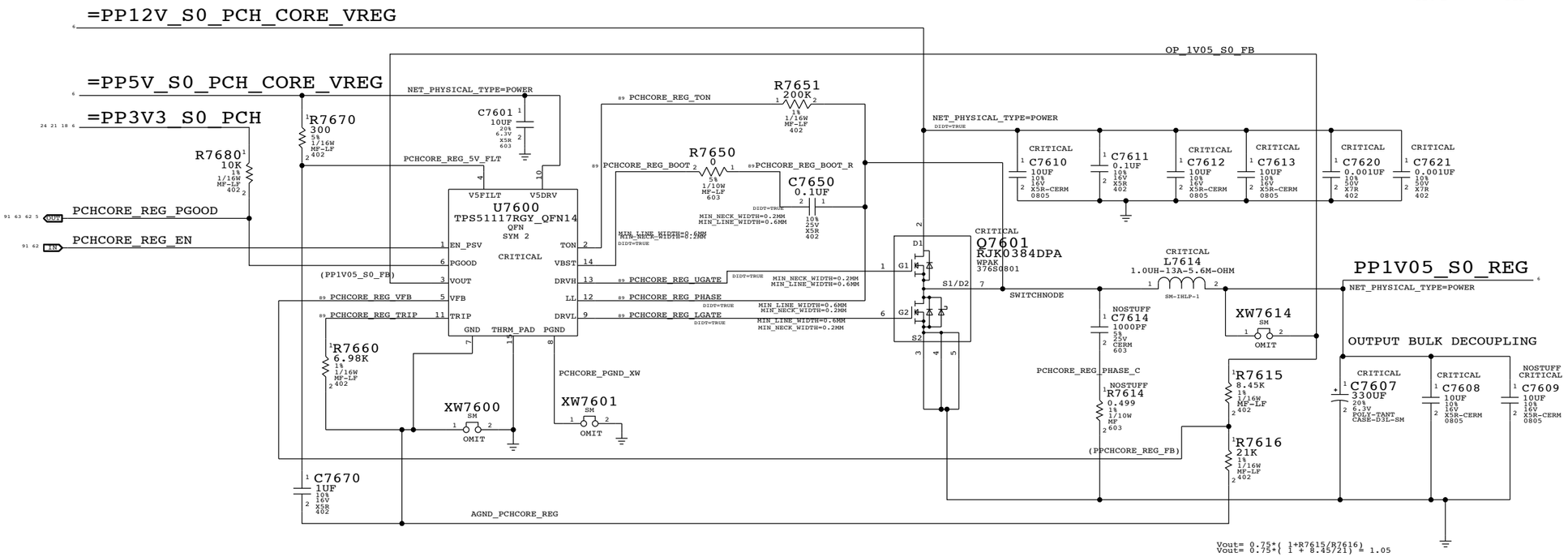
SYNC MASTER=K61 JERRY SYNC DATE=07/16/2009
PAGE TITLE
CPU VTT REGULATOR

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 74 OF 110
SHEET 67 OF 92

IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A



PAGE TITLE: IBEX PEAK CORE

Apple Inc.

DRAWING NUMBER: 051-8233
SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 76 OF 110
SHEET: 68 OF 92

3V3 S5 REGULATOR

=PP12V_S5_P5VS3_VREG

NET_PHYSICAL_TYPE=POWER

=PP12V_S5_P3V3S5_VREG

EMC CAPS PLACE CLOSE TO FET

CRITICAL C7713 100UF 20% 16V POLY 6.3X9-TH

C7712 10UF 10% 16V X5R-CERM 0805

C7710 10UF 10% 16V X5R-CERM 0805

C7711 0.1UF 10% 16V X5R 402

C7722 0.1UF 10% 16V X5R 402

NET_PHYSICAL_TYPE=POWER DIDT=TRUE

3V3 OUTPUT

PP3V3_S5_REG

CRITICAL L7710 2.2UH-14A MMD06CZ-SM

SWITCHNODE

NET_PHYSICAL_TYPE=POWER

C7790 8200PF 50V 10% 2 CERM 603

R7790 16.5K 1% 1/16W MF-LF 402

R7791 16.5K 1% 1/16W MF-LF 402

P3V3S5_REG_SNUB

C7730 1000PF 5% 25V NP0-C0G 402 NOSTUFF

R7730 0.499 1% 1/10W MF 603 NOSTUFF

Q7710 RJK0384DPA WPAK 376S0801

D7700 CRITICAL CTLSH3-30M833 TLM833

1 (P3V3S5_UGATE) MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM GATE_NODE=TRUE

6 (P3V3S5_LGATE) MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM GATE_NODE=TRUE

C7714 0.1UF 10% 50V X7R 603-1

P3V3S5_REG_BOOT_R MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM

R7710 0 5% 1/10W MF-LF 603

(P3V3S5_PHASE)

MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM

U7700 ISL62383 QFN CRITICAL

LDO5	18	VIN	17
VCC1	5	FCCM	3 TP_P5VS3_REG_FCCM
VCC2	4	PGOOD1	7 TP_P3V3S5_REG_PGOOD
		PGOOD2	1
UGATE1	14	UGATE2	22 P5VS3_REG_UGATE
BOOT1	15	BOOT2	21 P5VS3_REG_BOOT
PHASE1	13	PHASE2	23 P5VS3_REG_PHASE
LGATE1	16	LGATE2	20 P5VS3_REG_LGATE
ISEN1	10	ISEN2	26 P5VS3_REG_ISEN
OCSET1	11	OCSET2	25 P5VS3_REG_OCSET
VOUT1	9	VOUT2	27 P5VS3_REG_VOUT2
FB1	8	FB2	28 P5VS3_REG_FB
FSET1	6	FSET2	2 P5VS3_REG_FSET2
EN1	12	EN2	24
THRM PAD	13	PGND	19

P3V3S5_REG_UGATE

P3V3S5_REG_BOOT

P3V3S5_REG_PHASE

P3V3S5_REG_LGATE

P3V3S5_REG_ISEN

P3V3S5_REG_OCSET

P3V3S5_REG_VOUT1

P3V3S5_REG_FB

P3V3S5_12VE_EN1

P3V3S5_REG_FSET1

C7701 0.01UF 10% 16V CERM 402

R7701 16.5K 1% 1/16W MF-LF 402

OUTPUT BULK DECOUPLING:

PLACEMENT_NOTE=PLACE NEXT TO C7716

128S0237 CRITICAL C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7715 10UF 10% 16V X5R-CERM 0805

C7717 10UF 10% 16V X5R-CERM 0805

XW7716 SM OMIT

R7720 45.3K 1% 1/16W MF-LF 402 <Ra>

R7721 10.0K 0.5% 1/16W MF 402 <Rb>

R7724 976 1% 1/16W MF-LF 402 P3V3S5_REG_FB_R

C7720 1000PF 5% 25V NP0-C0G 402

C7723 0.1UF 20% 16V CERM 603

C7716 0.1UF 20% 16V CERM 603

EMC CAPS PLACE CLOSE TO L

Vout = 0.6V * (1 + Ra / Rb)

R7722 68K 5% 1/16W MF-LF 402

R7723 33K 5% 1/16W MF-LF 402

P5VS3_EN

5V S3 REGULATOR

Power Rating ?

CRITICAL C7750 270UF 20% 16V ELEC 8X9-TH1

C7751 10UF 10% 16V X5R-CERM 0805

C7752 10UF 10% 16V X5R-CERM 0805

C7753 10UF 10% 16V X5R-CERM 0805

PP5V_S5_LDO

EMC: C7754,C7755 PLACE AT Q7330

C7754 0.1UF 10% 25V X5R 402

C7755 0.1UF 10% 25V X5R 402

DIDT=TRUE

5V OUTPUT

NET_PHYSICAL_TYPE=POWER

C7742 4.7UF 20% 6.3V CERM 603

R7740 2.2 5% 1/8W MF-LF 805

P5V_S5_LDO_R

P5V_S5_VCC1

C7740 1UF 10% 16V X5R 603

C7741 1UF 10% 16V X5R 603

P5VS3_REG_PGOOD

CRITICAL Q7750 CSD58851Q5A MLP5X6-LFPAK-Q5A 376S0631

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2 MM

P5VS3_REG_BOOT_R MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.6MM

R7750 0 5% 1/10W MF-LF 603

C7756 0.1UF 10% 25V X5R 402

NOSTUFF C7757 0.001UF 10% 50V CERM 402

5V_SNUBBER MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2 MM

R7752 0.499 1% 1/10W MF 603 NOSTUFF

CRITICAL Q7751 CSD58851Q5A MLP5X6-LFPAK-Q5A 376S0631

CRITICAL D7750 CTLSH3-30M833 TLM833

EMC: C7763,C7764 PLACE AT L7750.2

C7763 0.001UF 10% 50V X7R 402

C7764 0.001UF 10% 50V X7R 402

CRITICAL L7750 2.2UH-10A-13.6MOHM MMD06EZ-SM

SWITCHNODE

NET_PHYSICAL_TYPE=POWER

R7770 16.5K 1% 1/16W MF-LF 402

C7770 0.01UF 10% 16V CERM 402

R7771 16.5K 1% 1/16W MF-LF 402

PP5V_S3_REG

OUTPUT BULK DECOUPLING:

C7760 10UF 20% 6.3V CERM 805-1

C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

XW7751 SM OMIT

R7759 976 1% 1/16W MF-LF 402 P5VS5_REG_FB_R

C7759 1000PF 5% 25V NP0-C0G 402

R7755 75K 1% 1/16W MF-LF 402 RA

R7756 10K 1% 1/16W MF-LF 402 RB

C7747 0.01UF 10% 16V CERM 402

R7747 16.5K 1% 1/16W MF-LF 402

NOSTUFF C7777 0.001UF 10% 50V CERM 402

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE: 5V_S3 / 3V3_S5 VREGS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 77 OF 110

SHEET 69 OF 92

1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A

=PP12V_S5_DDR_VREG
=PP5V_S3_DDR_VREG
NET_PHYSICAL_TYPE=POWER
R7801 4.7 5% 1/16W MF-LF 402
PP5V_S3_DDR_REG_V5FILT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C7800 4.7UF 20% 6.3V CERM 603
C7801 1UF 10% 10V X5R 402
C7815 10UF 20% 6.3V X5R 603
R7810 6.04K 1% 1/16W MF-LF 402
CRITICAL C7830 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7831 270UF 20% 16V ELEC 8X9-TH1
C7832 10UF 10% 16V X5R-CERM 0805
EMC CAPS PLACE CLOSE TO FET
C7833 0.1UF 20% 16V CERM 603
C7834 0.1UF 20% 16V CERM 603
CRITICAL Q7830 CSD58851Q5A MLP5X6-LFPAK-Q5A
EMC CAPS PLACE CLOSE TO L7830
C7838 0.001UF 10% 50V X7R 402
C7839 0.001UF 10% 50V X7R 402
(DDRREG_DRVH)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
DIDT=TRUE
C7840 0.1UF 20% 25V CERM 603
DDR_REG_BOOT_R
R7840 0 5% 1/10W MF-LF 603
SWITCHNODE
CRITICAL L7830 1.5UH-22A-4MOHM MSQ12111R5LF-TH
PP1V5_S3_REG
NET_PHYSICAL_TYPE=POWER
OUTPUT BULK DECOUPLING:
CRITICAL C7835 330UF-0.009OHM 20% 2V POLY CASE-D2-HF
NOSTUFF CRITICAL C7836 330UF-0.009OHM 20% 2V POLY CASE-D2-HF
C7837 10UF 20% 6.3V X5R 603
NOSTUFF C7841 1000PF 5% 25V NP0-C0G 402
1V5_SNUBBER
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.4MM
NOSTUFF R7831 0.499 1% 1/10W MF 603
CRITICAL D7831 CTLSH3-30M833 TLM833
CRITICAL Q7831 CSD58850Q5A MLP5X6-LFPAK-Q5A
OMIT XW7831
PLACEMENT_NOTE=PLACE NEXT TO Q7831
OMIT XW7830
PLACEMENT_NOTE=PLACE NEXT TO L7830
(DDRREG_CSGND)
(DDRREG_VDDQSNS)
(DDRREG_FB)
NO STUFF C7820 100PF 5% 50V CERM 402
R7832 15.0K 1% 1/16W MF-LF 402 <Ra>
R7833 15.0K 1% 1/16W MF-LF 402 <Rb>
Vout = 0.75V * (1 + Ra / Rb)

DDRVTT_EN
=DDRREG_EN
PM_PGOOD_DDRREG_S3
PPVTT_S3_DDR_BUF (NOT USED)
10mA max load
Vout = VDDQSNS/2
Vout = VTTREF
PPVTT_S0_DDR_LDO
OMIT XW7803 SM
NO_TEST=TRUE
FEEDBACK THROUGH SHORT SHOULD NOT NEED TP
CRITICAL C7804 22UF 20% 6.3V CERM-X5R 805-3
CRITICAL C7803 22UF 20% 6.3V CERM-X5R 805-3
C7805 0.033UF 10% 16V X5R 402
XW7800 OMIT SM
XW7801 OMIT SM
AGND_DDR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

U7800 TPS51116 QFN SYM (2 OF 2)
V5IN, V5FILT, VLDOIN
COMP
S3 — VTT Enable
S5 — VDDQ/VTTREF Enable
PGOOD — VDDQ PGOOD
VTTREF, VTT, VTTSNS
NC0, NC1
VTTGND, THRM_PAD GND, PGND_CS_GND
VDDQSNS, MODE, VBST, DRVH, LL, DRVL, CS, VDDQSET
DDR_REG_VDDQSNS, DDR_REG_BOOT, DDR_REG_UGATE, DDR_REG_PHASE, DDR_REG_LGATE, DDR_REG_CS, DDR_REG_FB
DDR_REG_CSGND
DDR_REG_PGND

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

1.8 V SUPPLY

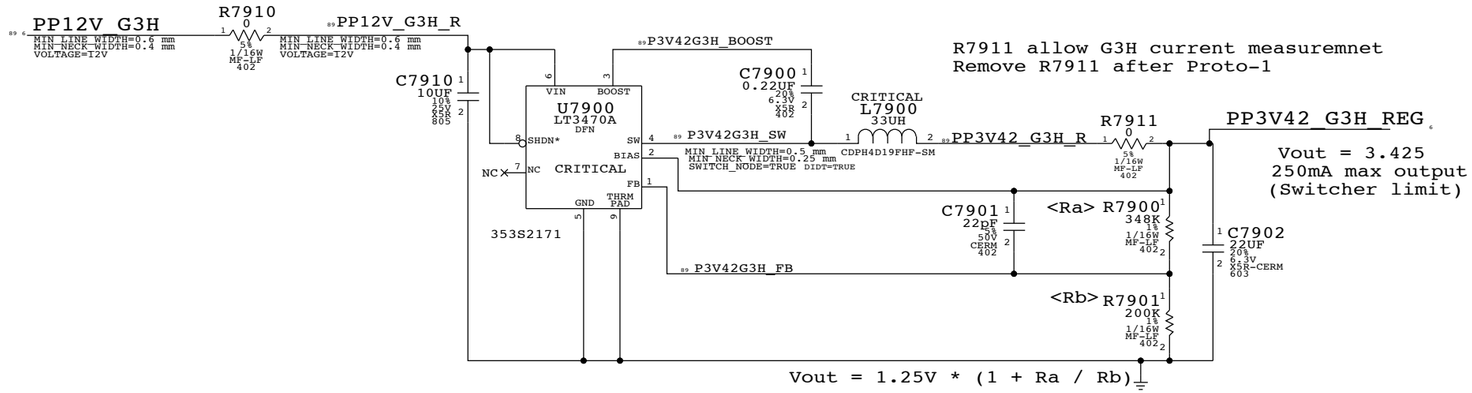
=PP5V_S0_P1V8_VREG
C7854 10UF 10% 6.3V X5R 805
C7855 10UF 10% 6.3V X5R 805
R7852 100K 5% 1/16W MF-LF 402
R7853 100K 5% 1/16W MF-LF 402
C7851 1UF 10% 16V X5R 402
U7850 ISL8009B DFN CRITICAL
VIN, EN, POR, SKIP, VFB, RSI, LX, GND THRM_PAD
P1V8_REG_PHASE
P1V8_REG_POR
P1V8_REG_SKIP
P1V8_REG_VFB
NET_PHYSICAL_TYPE=POWER
DIDT=TRUE
SWITCHNODE
CRITICAL L7850 2.2UH-3.25A-68M-OHM MMD04BZ-SM
C7850 120PF 5% 50V 402 CERM
<Ra> R7850 59.0K 1% 1/16W MF-LF 402
<Rb> R7851 47.0K 1% 1/16W MF-LF 402
C7852 22UF 20% 6.3V CERM 805
C7853 22UF 20% 6.3V CERM 805
PP1V8_S0_REG

Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V

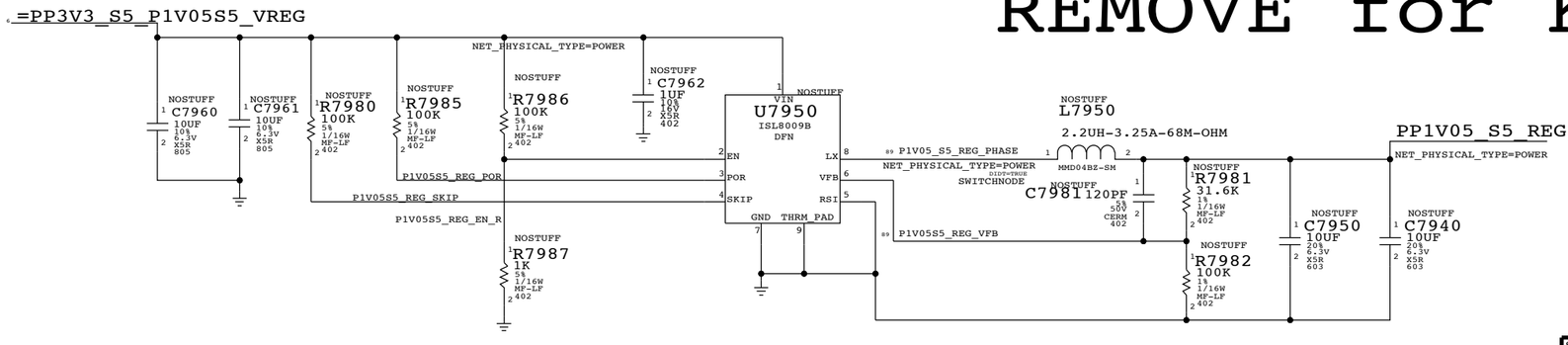
SYNC_MASTER=K60_JERRY
SYNC_DATE=07/01/2009
PAGE TITLE: 1.5V / 1.8V VREGS
Apple Inc.
DRAWING NUMBER: 051-8233
SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 78 OF 110
SHEET: 70 OF 92

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.05V S5 SUPPLY



REMOVE for K60/K61

SYNC_MASTER=K60 JERRY SYNC_DATE=07/01/2009

PAGE TITLE: 1.05 S5 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

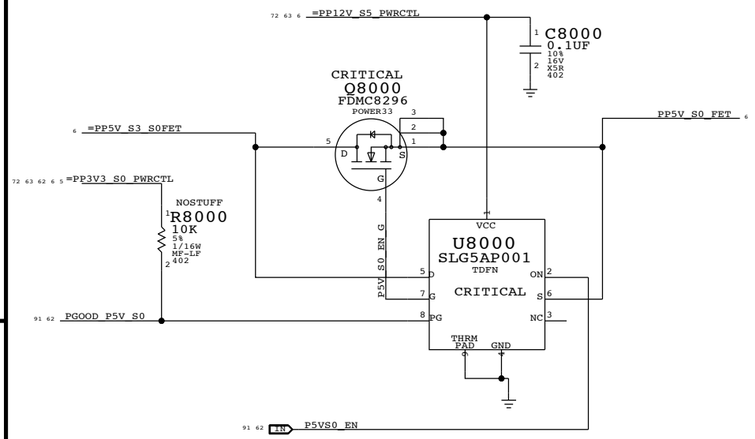
REVISION: G.0.0

BRANCH:

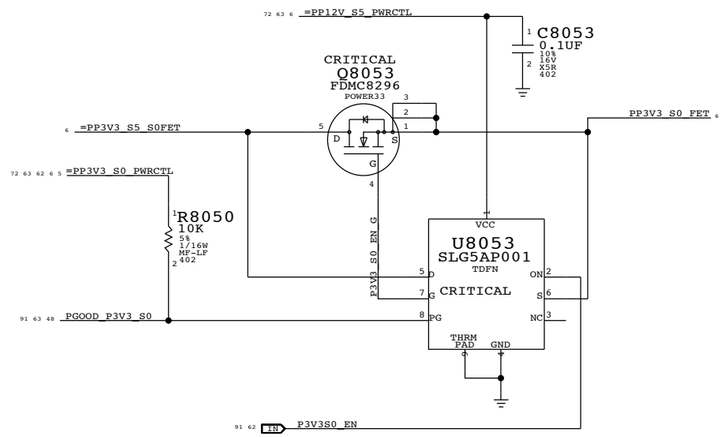
PAGE: 79 OF 110

SHEET: 71 OF 92

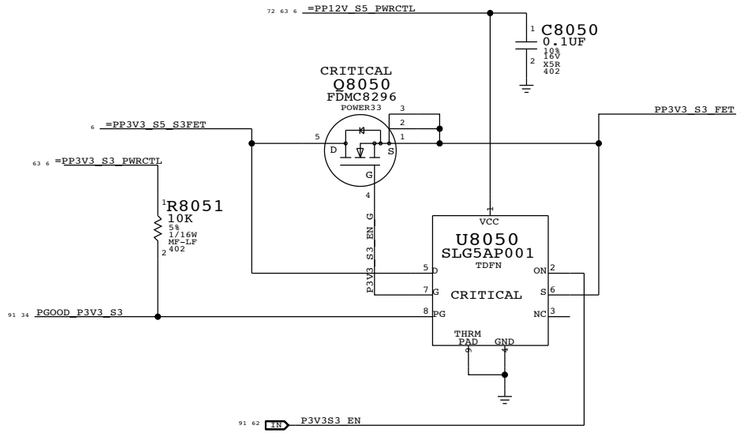
5V S0 FET (7A PK/2.7A AVG)



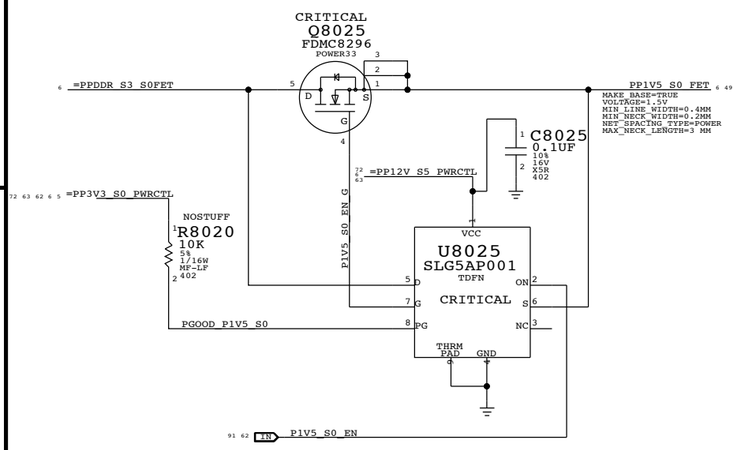
3.3V S0 FET (3.4APK / 1.9A AVG)



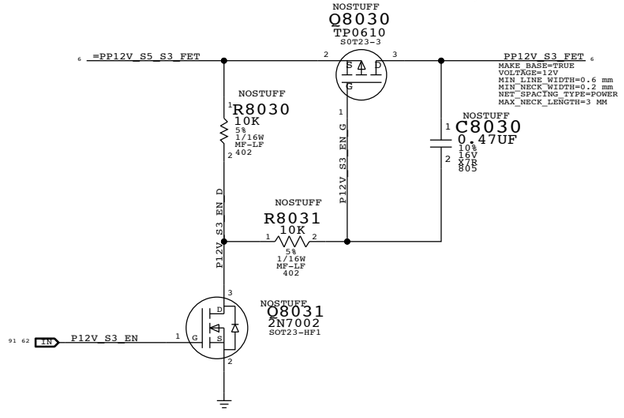
3.3V S3 FET (2.9A PK / 1.2A AVG)



1.5V S0 FET (6.2A PK / 3A AVG)

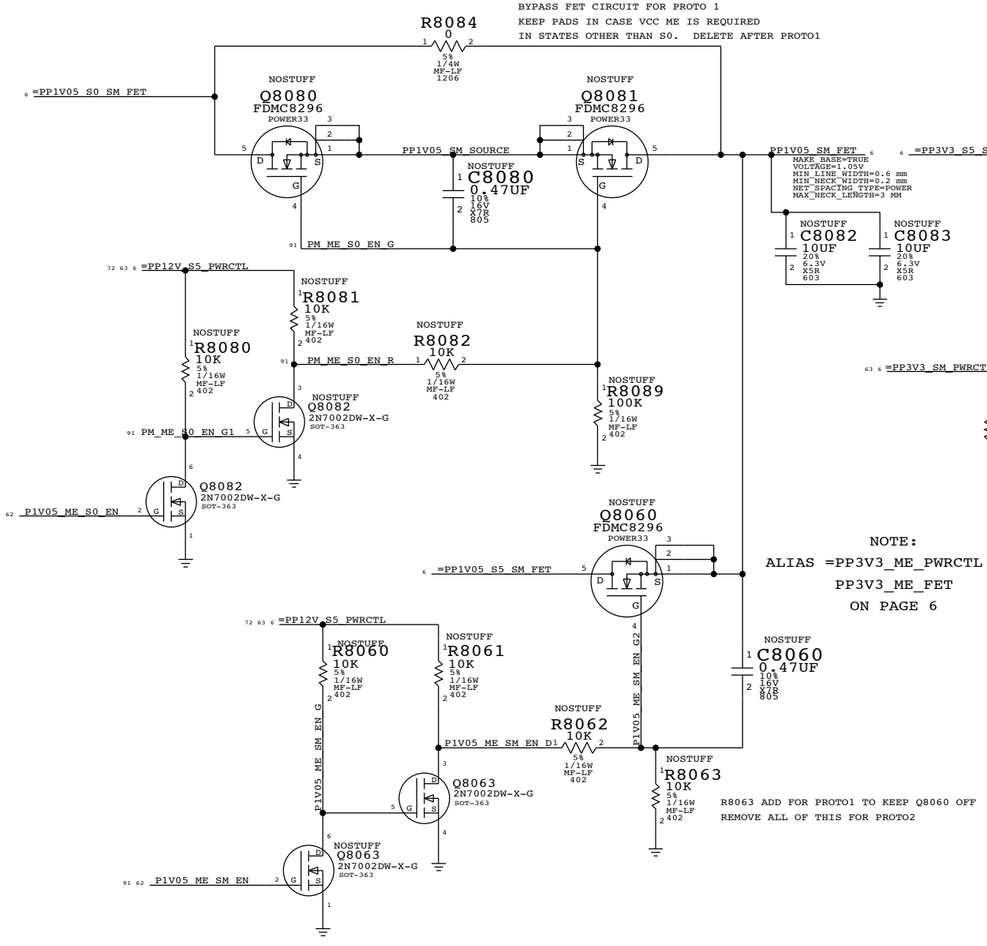


12V S3 FET (< 200MA)



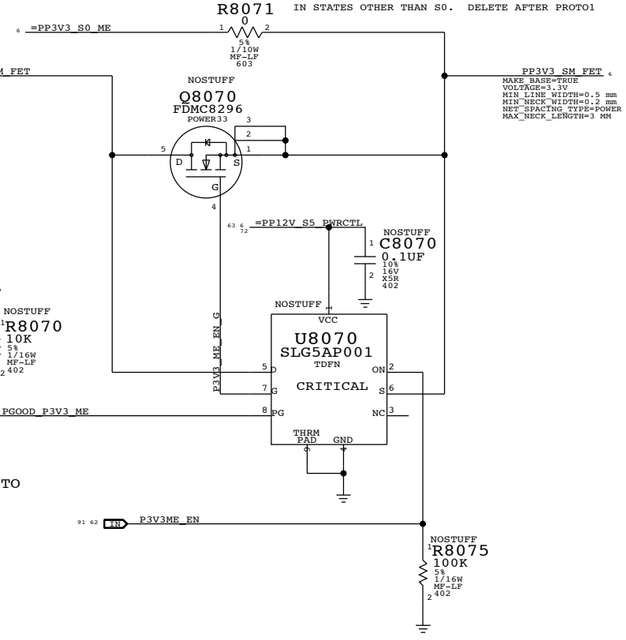
1V05 ME FETS (S0: 2.2A MAX SM: 387MA)

BYPASS FET CIRCUIT FOR PROTO 1
KEEP PADS IN CASE VCC ME IS REQUIRED
IN STATES OTHER THAN S0. DELETE AFTER PROTO1



3.3VME FET (86MA MAX)

BYPASS FET CIRCUIT FOR PROTO 1
KEEP PADS IN CASE VCC_3V3 ME IS REQUIRED
IN STATES OTHER THAN S0. DELETE AFTER PROTO1



NOTE:
ALIAS =PP3V3_ME_PWRCTL TO
PP3V3_ME_FET
ON PAGE 6

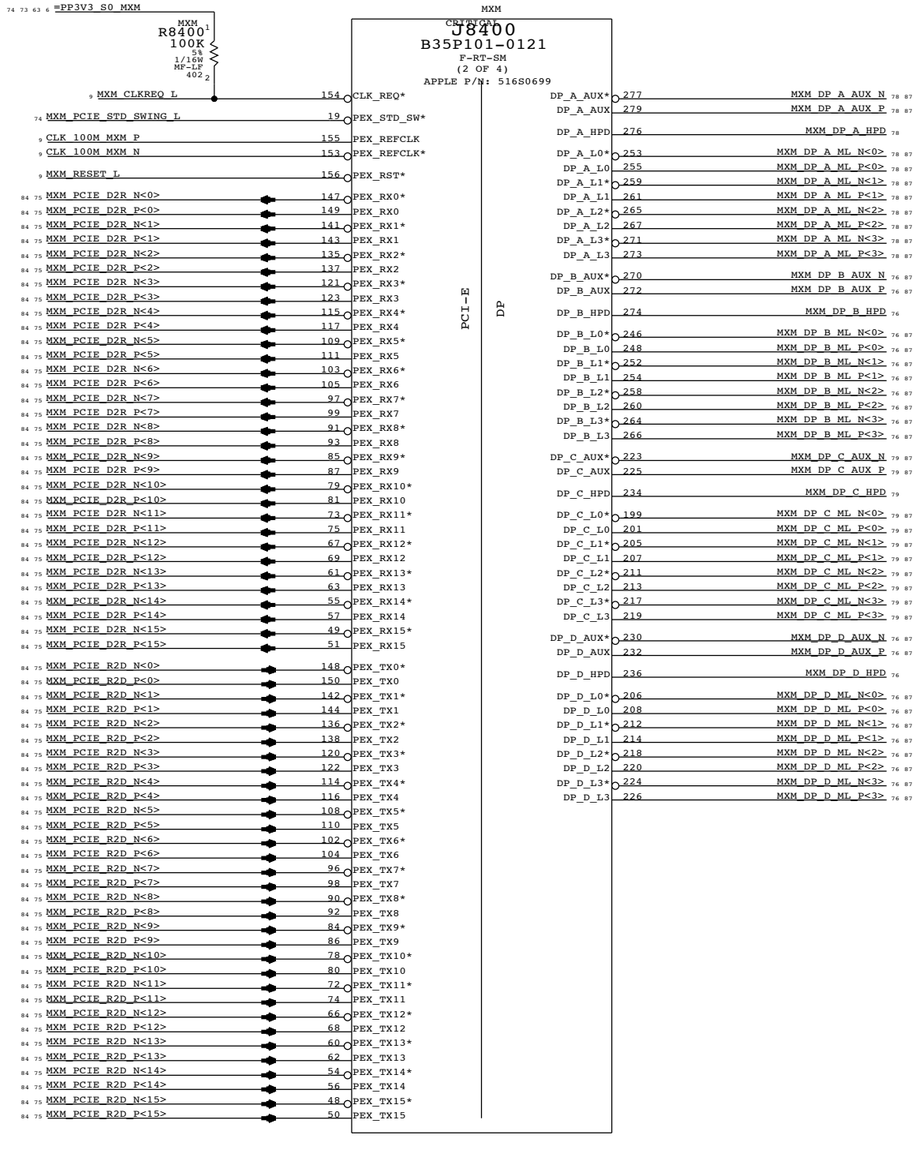
SYNC MASTER=K60 MIKE	SYNC DATE=07/01/2009
PAGE TITLE: S3+S0 FETS	
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION G.0.0
	BRANCH
	PAGE 80 OF 110
	SHEET 72 OF 92

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K23 AARON SYNC DATE=07/16/2009

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 84 OF 110
SHEET 73 OF 92

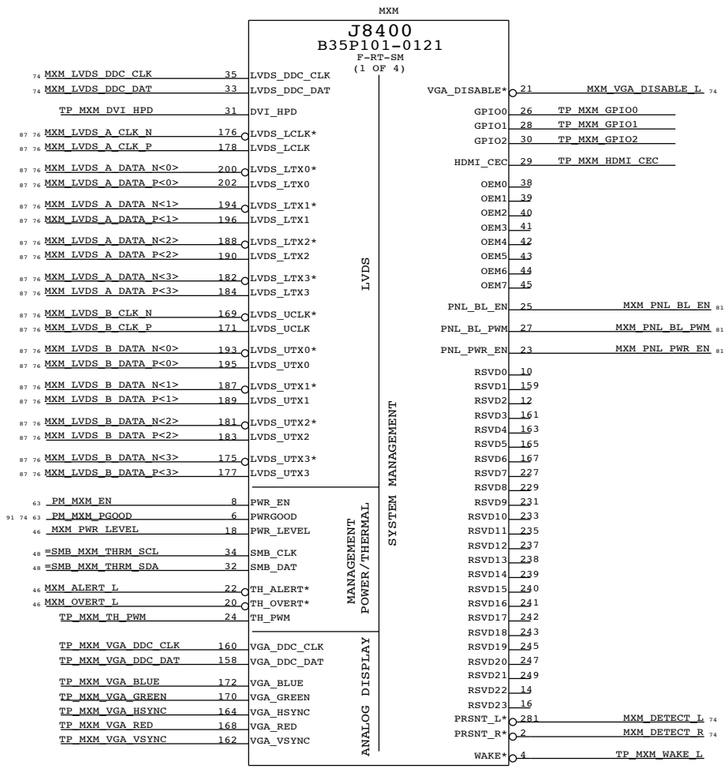
Page Notes

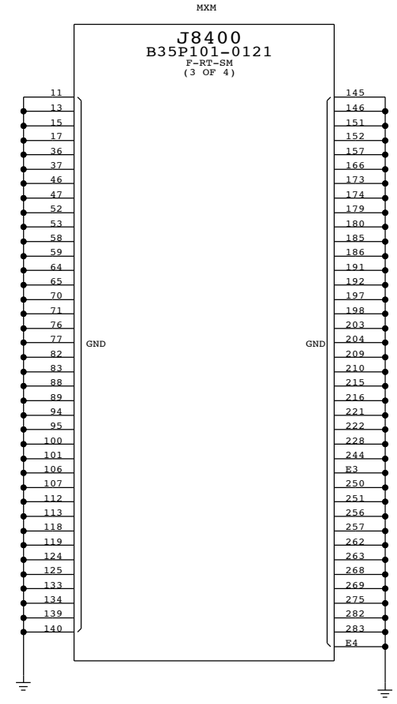
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR





FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

NOSTUFF
R8510
0
MXM_VGA_DISABLE_L
MF-LF 5% 1/16W
402

FLOAT = LOW SWING
GND = HIGH SWING

R8504
0
MXM_PCIE_STD_SWING_L
MF-LF 5% 1/16W
402

=PP3V3_S0_MXM

R8500
100K
MXM_DETECT_L
MF-LF 5% 1/16W
402

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501
100K
MXM_DETECT_R
MF-LF 5% 1/16W
402

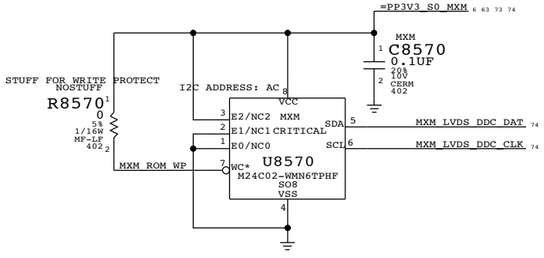
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503
10K
PM_MXM_PGOOD
MF-LF 5% 1/16W
402

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



SYNC_MASTER=K23_AARON	SYNC_DATE=07/16/2009
PAGE TITLE: MXM I/O	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
	REVISION: G.0.0
	BRANCH:
	PAGE: 85 OF 110
	SHEET: 74 OF 92

MXM TX CAPS

84 9	IN	PEG_R2D_C_P<0>	MXM C8600	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT 73 84
84 9	IN	PEG_R2D_C_N<0>	MXM C8601	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT 73 84
84 9	IN	PEG_R2D_C_N<1>	MXM C8602	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	OUT 73 84
84 9	IN	PEG_R2D_C_P<1>	MXM C8603	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	OUT 73 84
84 9	IN	PEG_R2D_C_N<2>	MXM C8604	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>	OUT 73 84
84 9	IN	PEG_R2D_C_P<2>	MXM C8605	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>	OUT 73 84
84 9	IN	PEG_R2D_C_P<3>	MXM C8606	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>	OUT 73 84
84 9	IN	PEG_R2D_C_N<3>	MXM C8607	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>	OUT 73 84
84 9	IN	PEG_R2D_C_N<4>	MXM C8608	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>	OUT 73 84
84 9	IN	PEG_R2D_C_P<4>	MXM C8609	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>	OUT 73 84
84 9	IN	PEG_R2D_C_N<5>	MXM C8610	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>	OUT 73 84
84 9	IN	PEG_R2D_C_P<5>	MXM C8611	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>	OUT 73 84
84 9	IN	PEG_R2D_C_P<6>	MXM C8612	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>	OUT 73 84
84 9	IN	PEG_R2D_C_N<6>	MXM C8613	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>	OUT 73 84
84 9	IN	PEG_R2D_C_N<7>	MXM C8614	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>	OUT 73 84
84 9	IN	PEG_R2D_C_P<7>	MXM C8615	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<8>	OUT 73 84
84 9	IN	PEG_R2D_C_P<8>	MXM C8616	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<7>	OUT 73 84
84 9	IN	PEG_R2D_C_N<8>	MXM C8617	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<7>	OUT 73 84
84 9	IN	PEG_R2D_C_P<9>	MXM C8618	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>	OUT 73 84
84 9	IN	PEG_R2D_C_N<9>	MXM C8619	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<6>	OUT 73 84
84 9	IN	PEG_R2D_C_N<10>	MXM C8620	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<5>	OUT 73 84
84 9	IN	PEG_R2D_C_P<10>	MXM C8621	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<5>	OUT 73 84
84 9	IN	PEG_R2D_C_N<11>	MXM C8622	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<4>	OUT 73 84
84 9	IN	PEG_R2D_C_P<11>	MXM C8623	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>	OUT 73 84
84 9	IN	PEG_R2D_C_P<12>	MXM C8624	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>	OUT 73 84
84 9	IN	PEG_R2D_C_N<12>	MXM C8625	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>	OUT 73 84
84 9	IN	PEG_R2D_C_N<13>	MXM C8626	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>	OUT 73 84
84 9	IN	PEG_R2D_C_P<13>	MXM C8627	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>	OUT 73 84
84 9	IN	PEG_R2D_C_P<14>	MXM C8628	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>	OUT 73 84
84 9	IN	PEG_R2D_C_N<14>	MXM C8629	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>	OUT 73 84
84 9	IN	PEG_R2D_C_N<15>	MXM C8630	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>	OUT 73 84
84 9	IN	PEG_R2D_C_P<15>	MXM C8631	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>	OUT 73 84

MXM RX CAPS

84 73	IN	MXM_PCIE_D2R_P<15>	MXM C8632	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<0>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<15>	MXM C8633	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<0>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<14>	MXM C8634	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<1>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<14>	MXM C8635	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<1>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<13>	MXM C8636	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<2>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<13>	MXM C8637	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<2>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<12>	MXM C8638	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<3>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<12>	MXM C8639	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<3>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<11>	MXM C8640	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<4>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<11>	MXM C8641	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<4>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<10>	MXM C8642	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<5>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<10>	MXM C8643	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<5>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<9>	MXM C8644	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<6>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<9>	MXM C8645	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<6>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<8>	MXM C8646	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<7>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<8>	MXM C8647	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<7>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<7>	MXM C8648	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<8>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<7>	MXM C8649	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<8>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<6>	MXM C8650	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<9>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<6>	MXM C8651	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<9>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<5>	MXM C8652	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<10>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<5>	MXM C8653	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<10>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<4>	MXM C8654	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<4>	MXM C8655	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<11>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<3>	MXM C8656	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<12>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<3>	MXM C8657	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<12>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<2>	MXM C8658	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<13>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<2>	MXM C8659	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<13>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<1>	MXM C8662	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<14>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<1>	MXM C8663	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<14>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<0>	MXM C8660	0.1UF	2 10% 16V X5R 402	PEG_D2R_N<15>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<0>	MXM C8661	0.1UF	2 10% 16V X5R 402	PEG_D2R_P<15>	OUT 9 84

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE

MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 86 OF 110

SHEET 75 OF 92

Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 74	MXM_LVDS_A_CLK_N	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_CLK_P	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<0>	NC_MXM_LVDS_A_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<0>	NC_MXM_LVDS_A_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<1>	NC_MXM_LVDS_A_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<1>	NC_MXM_LVDS_A_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<2>	NC_MXM_LVDS_A_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<2>	NC_MXM_LVDS_A_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<3>	NC_MXM_LVDS_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<3>	NC_MXM_LVDS_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_N	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_P	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<0>	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<0>	NC_MXM_LVDS_B_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<1>	NC_MXM_LVDS_B_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<1>	NC_MXM_LVDS_B_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<2>	NC_MXM_LVDS_B_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<2>	NC_MXM_LVDS_B_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<3>	NC_MXM_LVDS_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<3>	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

87 73	MXM_DP_B_ML_P<0..3>	NC_MXM_DP_B_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_ML_N<0..3>	NC_MXM_DP_B_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_AUX_P	NC_MXM_DP_B_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_AUX_N	NC_MXM_DP_B_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
73	MXM_DP_B_HPD	NC_MXM_DP_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_ML_P<0..3>	NC_MXM_DP_D_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_ML_N<0..3>	NC_MXM_DP_D_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_AUX_P	NC_MXM_DP_D_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_AUX_N	NC_MXM_DP_D_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
73	MXM_DP_D_HPD	NC_MXM_DP_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE

Display: Aliases

SYNC_MASTER=K61_AARON SYNC_DATE=07/01/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7997	3.0.0
SCALE: NONE	SHT 76 OF 92	

Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

CRITICAL
J9002
20389-Y30E-01
F-RT-SM
518S0685

NOSTUFF R9050 0 5% 1/16W MF-LF 402
NOSTUFF R9051 0 5% 1/16W MF-LF 402

=SMB_DP_TCON_SCL
=SMB_DP_TCON_SDA
I2C MASTER ON TCON
I2C_TCON_SCL
I2C_TCON_SDA

DP_INT_AUXCH_N
DP_INT_AUXCH_P

DP_INT_LINK_P<0> C9040 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_P<0> NO_TEST
DP_INT_LINK_N<0> C9041 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_N<0> NO_TEST
DP_INT_LINK_P<1> C9042 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_P<1> NO_TEST
DP_INT_LINK_N<1> C9043 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_N<1> NO_TEST
DP_INT_LINK_P<2> C9044 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_P<2> NO_TEST
DP_INT_LINK_N<2> C9045 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_N<2> NO_TEST
DP_INT_LINK_P<3> C9046 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_P<3> NO_TEST
DP_INT_LINK_N<3> C9047 0.1uF 10% 16V X5R 402 → DP_INT_LINK_CONN_N<3> NO_TEST

SPDIF_DP_AUDIO_OUT
VIDEO_ON
DP_HPD_INT

PANEL POWER CONTROL

=PP12V_S0_LCD
R9000 100K 5% 1/16W MF-LF 402
LCD_PANEL_PWR_L_DIV
R9001 29.4K 1% 1/16W MF-LF 402
R9002 100K 5% 1/16W MF-LF 402
C9000 0.1UF 10% 50V X7R 603-1
CRITICAL Q9000 FDC638P_G SM
LCD_PANEL_PWR_L_RC
PLACE NEAR J9002

PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
L9000 FERR-250-OHM SM
C9020 10UF 10% 16V X5R-CERM 0805
C9001 0.001uF 20% 50V CERM 402
PP12V_LCD_CONN
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

=PP3V3_S0_VIDEO
C9010 0.001uF 20% 50V CERM 402

LCD_PANEL_PWR_L
LCD_PANEL_PWR
LCD_PANEL_PWR_G
NOSTUFF R9071 0 5% 1/10W MF-LF 603
Q9001 2N7002 SOT23-HF1
VIDEO_ON
R9072 0 5% 1/10W MF-LF 603
R9070 100K 5% 1/16W MF-LF 402

BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video
Options for GPU or MLB HW controlled backlight enable are included

=PP3V3_S0_DP
NOSTUFF C9011 0.1UF 20% 10V CERM 402
VIDEO_ON
LCD_BKL_ON_MUX
NOSTUFF U9050 TC7SZ08AFEAPE SOT665
NOSTUFF R9012 1K 5% 1/16W MF-LF 402
LCD_BKL_MLB_EN

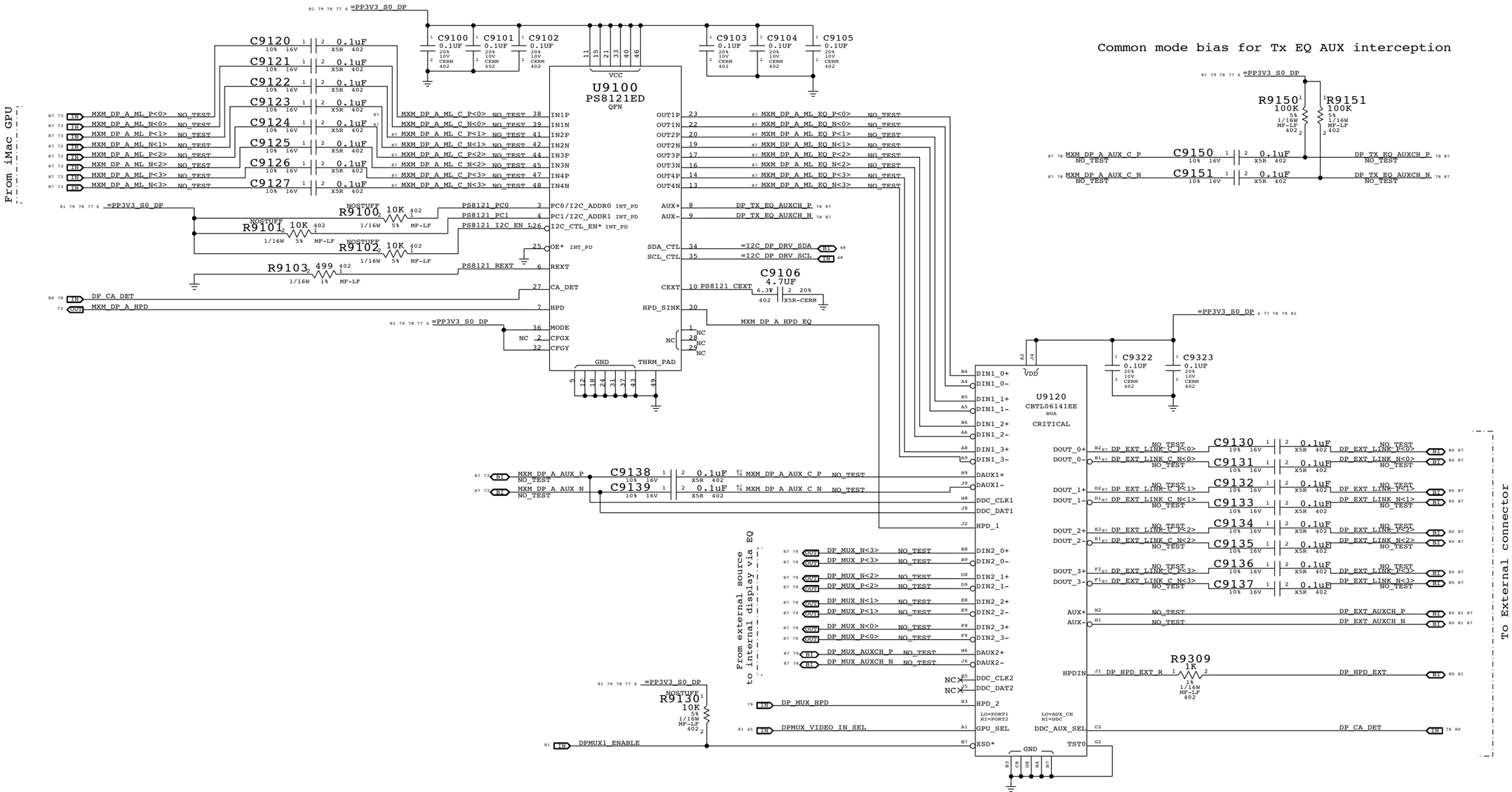
CRITICAL L9050 FERR-250-OHM SM
R9081 47 5% 1/16W MF-LF 402
BACKLIGHT_PWM
LCD_PWM_FILT
LCD_PWM

=PP3V3_S0_DP
VIDEO_ON_L
used by diag LED
C9005 22UF 20% 6.3V CERM 805
=PP3V3_S0_DP
VIDEO_ON
U9500 74LVC14 TSSOP-HF
D9000 SOT23 BAT54XG
R9009 19.1K 1% 1/16W MF-LF 402
VIDEO_ON_L_DLY
U9520 74AUP2G14GM SOT886
R9011 1K 5% 1/16W MF-LF 402
LCD_BKL_ON_DLY
LCD_BKL_ON

buffers are multiple parts, other parts are on csa 95

SYNC MASTER=K23 AARON	SYNC DATE=07/16/2009
PAGE TITLE: Display: Int DP Connector	
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION G.0.0
	BRANCH
	PAGE 90 OF 110
	SHEET 77 OF 92

EQ & Re-Driver for DP source



DisplayPort Mux 1
Analog mux at External Connector

SYNC MASTER=K23 AARON	SYNC DATE=07/16/2009
PAGE TITLE: Display: BiDiVi Mux1	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
	REVISION: G.0.0
	BRANCH:
	PAGE: 91 OF 110
	SHEET: 78 OF 92

DisplayPort Equalizer & MUX 2

Note: INT_PD = Internal Pulldown on this pin of >=100 kOhms

From iMac GPU

MXM_DP_C_ML_P<0> NO_TEST — C9240 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_P<0> NO_TEST
MXM_DP_C_ML_N<0> NO_TEST — C9241 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_N<0> NO_TEST
MXM_DP_C_ML_P<1> NO_TEST — C9242 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_P<1> NO_TEST
MXM_DP_C_ML_N<1> NO_TEST — C9243 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_N<1> NO_TEST
MXM_DP_C_ML_P<2> NO_TEST — C9244 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_P<2> NO_TEST
MXM_DP_C_ML_N<2> NO_TEST — C9245 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_N<2> NO_TEST
MXM_DP_C_ML_P<3> NO_TEST — C9246 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_P<3> NO_TEST
MXM_DP_C_ML_N<3> NO_TEST — C9247 0.1uF 10% 16V X5R 402 — MXM_DP_C_ML_C_N<3> NO_TEST

From external input via MUX 1

DP_MUX_P<0>
DP_MUX_N<0>
DP_MUX_P<1>
DP_MUX_N<1>
DP_MUX_P<2>
DP_MUX_N<2>
DP_MUX_P<3>
DP_MUX_N<3>

=PP3V3_S0_DP

C9200 C9201 C9202 C9203 C9204 0.1UF 20% 10V CERM 402

VDD: 4, 22, 38, 47, 62

U9200 PS8325 QFN

CRITICAL

2	IN1_D0P	DP_D0P	61 NO_TEST DP_INT_LINK_P<0> OUT
3	IN1_D0N	DP_D0N	60 NO_TEST DP_INT_LINK_N<0> OUT
5	IN1_D1P	DP_D1P	58 NO_TEST DP_INT_LINK_P<1> OUT
6	IN1_D1N	DP_D1N	57 NO_TEST DP_INT_LINK_N<1> OUT
8	IN1_D2P	DP_D2P	55 NO_TEST DP_INT_LINK_P<2> OUT
9	IN1_D2N	DP_D2N	54 NO_TEST DP_INT_LINK_N<2> OUT
11	IN1_D3P	DP_D3P	52 NO_TEST DP_INT_LINK_P<3> OUT
12	IN1_D3N	DP_D3N	51 NO_TEST DP_INT_LINK_N<3> OUT
68	IN1_PEQ/SDA_CTL		
14	IN2_D0P	TMDS_CH0P	43 NC
15	IN2_D0N	TMDS_CH0N	42 NC
17	IN2_D1P	TMDS_CH1P	46 NC
18	IN2_D1N	TMDS_CH1N	45 NC
20	IN2_D2P	TMDS_CH2P	49 NC
21	IN2_D2N	TMDS_CH2N	48 NC
23	IN2_D3P	TMDS_CLKN	39 NC
24	IN2_D3N	TMDS_CLKP	40 NC
67	IN2_PEQ/SCL_CTL		
64	MODE0		
65	MODE1		
69	MODE2		
70	REXT	CEXT	1 DP_EQLZ_EXTC
34	NC TMDS_SCL	DP_AC_AUXP	30 NO_TEST DP_EQLZ_AUXCH_P BI
35	NC TMDS_SDA	DP_AC_AUXN	31 NO_TEST DP_EQLZ_AUXCH_N BI
66	SW/I2C_ADDR INT_PD		
28	IN1_AUXP_SCL	DP_AUXP_SCL	32 NO_TEST DP_INT_AUXCH_P BI
29	IN1_AUXN_SDA	DP_AUXN_SDA	33 NO_TEST DP_INT_AUXCH_N BI
25	IN2_AUXP_SCL		
26	IN2_AUXN_SDA		
56	DP_CADET	INT_PDIN1_CADET	7 NC
		INT_PDIN2_CADET	16 NC
53	DP_HPD INT_PD	IN1_HPDX	10 MXM_DP_C_HPD MUX — TO IMAC GPU
41	NC TMDS_HPD INT_PD	IN2_HPDX	19 DP_MUX_HPD MUX — TO EXTERNAL SOURCE VIA MUX1
37	NC TMDS_PC0		
44	NC TMDS_PC1		
71	NC PIOINT_PD		
59	NC PDINT_PD		
	GND	THRM_PAD	13, 27, 36, 50, 63, 72, 73

To Internal display

C9212 4.7UF 20% 6.3V X5R-CERM 402

see below

To Internal display

=I2C DP EQLZ SDA
=I2C DP EQLZ SCL

=PP3V3_S0_DP

R9221 1K 5% 1/16W MF-LF 402
R9215 1K 5% 1/16W MF-LF 402
R9220 1K 5% 1/16W MF-LF 402

MODE[2..0] = 111 SELECTS I2C CONTROL MODE

R9222 4.99K 1% 1/16W MF-LF 402 — DP_EQLZ_EXTR

R9280 0 5% 1/16W MF-LF 402 — DP_EQLZ_ADDR — NOSTUFF

R9281 1M 5% 1/16W MF-LF 402 — DP_EQLZ_CADET

From iMac GPU

MXM_DP_C_AUX_P NO_TEST — C9248 0.1uF 10% 16V X5R 402 — MXM_DP_C_AUX_C_P NO_TEST
MXM_DP_C_AUX_N NO_TEST — C9249 0.1uF 10% 16V X5R 402 — MXM_DP_C_AUX_C_N NO_TEST

From external input via MUX 1

DP_MUX_AUXCH_P NO_TEST
DP_MUX_AUXCH_N NO_TEST

From Internal display

DP_HPD_INT

Pulls for AUX_CH from DisplayPort Mux #2

=PP3V3_S0_DP

R9212 100K 1% 1/16W MF-LF 402 — MXM_DP_C_AUX_C_N
R9213 100K 1% 1/16W MF-LF 402 — MXM_DP_C_AUX_C_P

AC caps for EQ AUX interception

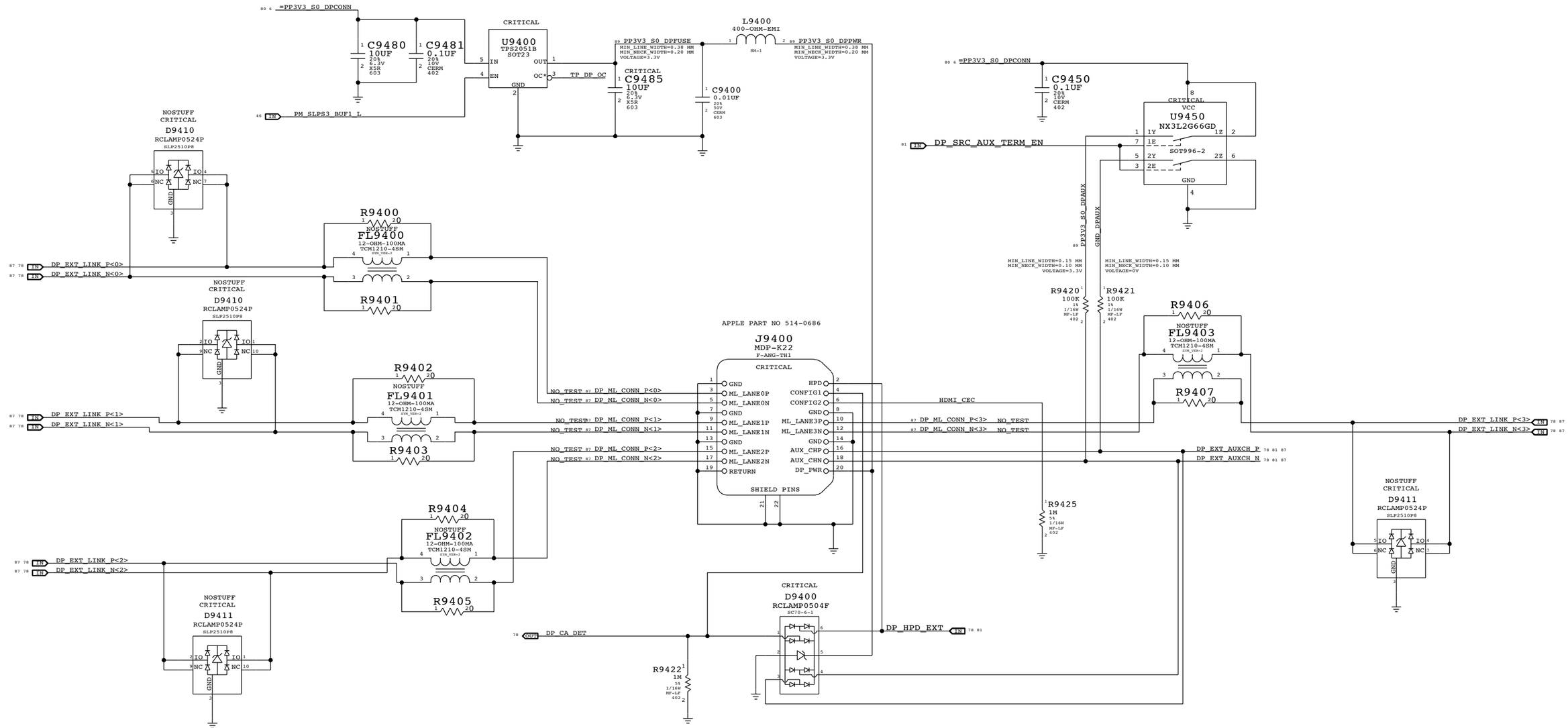
DP_EQLZ_AUXCH_P NO_TEST — DP_INT_AUXCH_P NO_TEST — C9290 0.1uF 10% 16V X5R 402
DP_EQLZ_AUXCH_N NO_TEST — DP_INT_AUXCH_N NO_TEST — C9291 0.1uF 10% 16V X5R 402

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE: BIDIVI DP MUX2

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 92 OF 110
SHEET 79 OF 92



SYNC MASTER=K23 AARON SYNC DATE=07/16/2009

PAGE TITLE

Display: Ext DP Connector

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

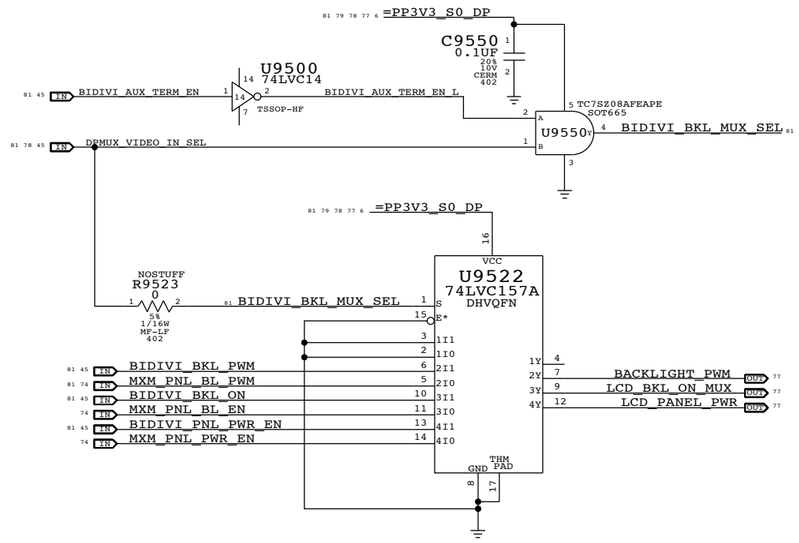
REVISION G.0.0

BRANCH

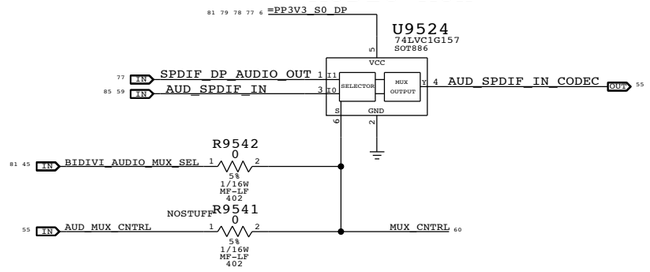
PAGE 94 OF 110

SHEET 80 OF 92

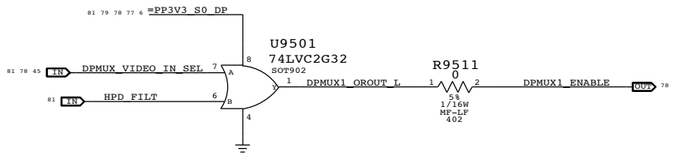
PANEL/BACKLIGHT CONTROL MUX



DisplayPort AUDIO MUX PLACE NEAR U6201

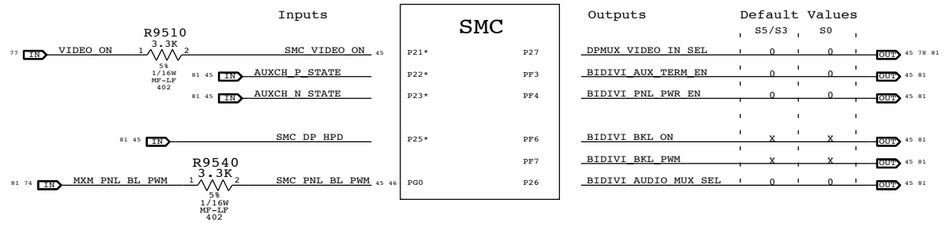


BiDiVi MUX Enable

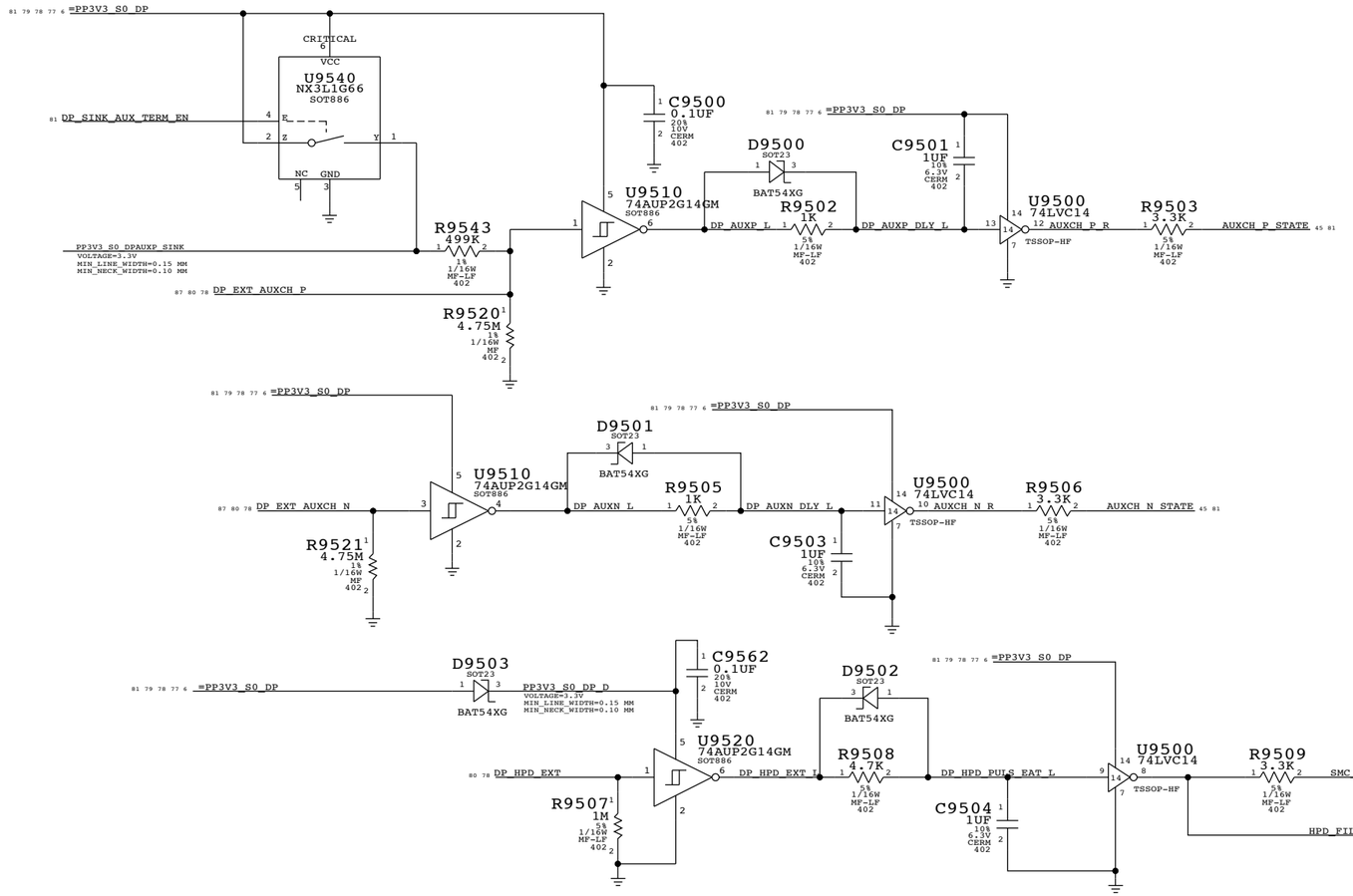


*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

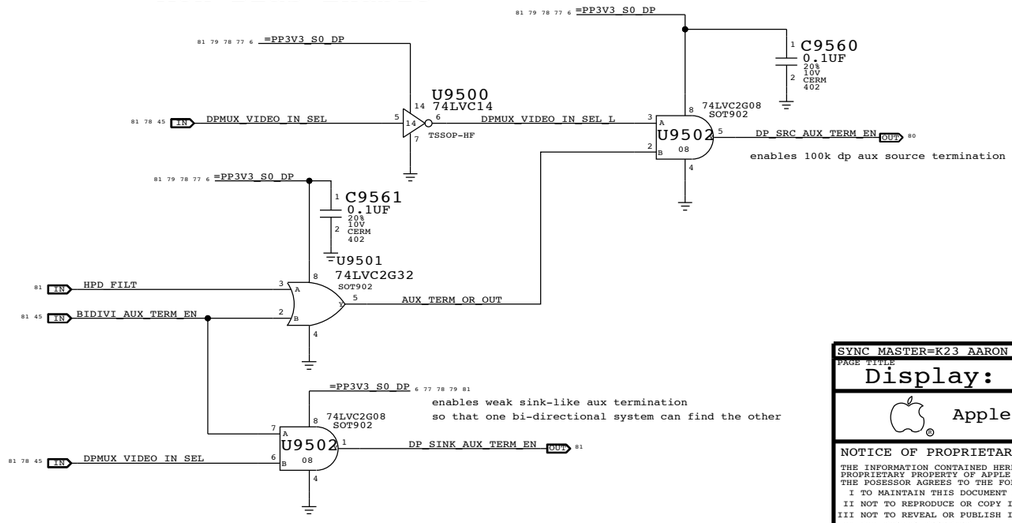
SMC Signals for BiDiVi



External AUX Channel and HPD Buffers & filters



AUX Bias Enable



SYNC_MASTER=K23_AARON	SYNC_DATE=07/16/2009
PAGE TITLE: Display: BiDiVi Support	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
	REVISION: G.0.0
	BRANCH:
	PAGE: 95 OF 110
	SHEET: 81 OF 92

K60/K61 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.085 MM	=STANDARD		
35_OHM_SE	*	Y	0.19 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD		
39_OHM_SE	*	Y	0.16 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD		
45_OHM_SE	*	Y	0.12 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

K60/K61 RULE DEFINITIONS

SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7997	3.0.0

SCALE: NONE SHT 82 OF 92

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DQ_ODD	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER
MEM_DQ_EVEN	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<7>	12 32

MEMORY POWER PROPERTIES

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1.5S	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	12 28
1.5S	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	12 28
1.6S	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMA_DQ	28
1.6S	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMB_DQ	28
1.6S	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A_SW	28
1.6S	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B_SW	28

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	12 32
1.6D	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP0	11
1.5D	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP1	11
1.6D	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP2	11
1.6D	MEM_70D	MEM_DQS	TP_MEM_B_DQS_P<8>	8 12
1.6D	MEM_70D	MEM_DQS	TP_MEM_B_DQS_N<8>	8 12
1.6D	MEM_70D	MEM_DQS	TP_MEM_A_DQS_P<8>	8 12
1.6D	MEM_70D	MEM_DQS	TP_MEM_A_DQS_N<8>	8 12

ADD RULES TO NC_DQS<8>
TO CLEAR CHECK_PLUS ERRORS

SYNC MASTER=K60 MIKE SYNC DATE=07/01/2009

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 101 OF 110
SHEET: 83 OF 92

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FDI_MISC			
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>
	CPU_50S	CPU_AGTL	FDI_INT
SATA SSD			
	SATA_85D	SATA	SATA_SSD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_SSD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_SSD_R2D_P 42
	SATA_85D	SATA	SATA_SSD_R2D_N 42
	SATA_85D	SATA	SATA_SSD_D2R_P 18 42
	SATA_85D	SATA	SATA_SSD_D2R_N 18 42
	SATA_85D	SATA	SATA_SSD_D2R_C_P 42
	SATA_85D	SATA	SATA_SSD_D2R_C_N 42
CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_P 10 18
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_N 10 18
CPU ITP			
	CPU_50S	CPU_ITP	XDP_BPM_L<7..0> 11 25
	CPU_50S	CPU_ITP	CPU_CFG<17..0> 10 15 25
	CPU_50S	CPU_ITP	XDP_OBSDATA_A<3..0> 25
CPU_MISC			
	CPU_50S	CPU_RCOMP	CPU_PEG_COMP 10
	CPU_50S	CPU_RCOMP	CPU_PEG_RBIAS 10
	CPU_50S	CPU_RCOMP	CPU_COMP3 11
	CPU_50S	CPU_RCOMP	CPU_COMP2 11
	CPU_50S	CPU_RCOMP	CPU_COMP1 11
	CPU_50S	CPU_RCOMP	CPU_COMP0 11

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE GRAPHICS			
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0> 9 75
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0> 9 75
	PCIE_85D	PCIE	PEG_D2R_P<15..0> 9 75
	PCIE_85D	PCIE	PEG_D2R_N<15..0> 9 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<15..0> 73 75
PCIE I/O			
	PCIE_85D	PCIE	PCIE_MINI_R2D_P 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P 18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N 18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P 18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N 18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_P 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_N 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P 39
	PCIE_85D	PCIE	PCIE_FW_R2D_N 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P 18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N 39
DMI			
	PCIE_85D	PCIE	DMI_S2N_P<3..0> 10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0> 10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0> 10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0> 10 19
FDI			
	PCIE_85D	PCIE	FDI_DATA_N<7..0>
	PCIE_85D	PCIE	FDI_DATA_P<15..0>
PCIE REF CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P 9
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N 9
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P 18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N 18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P 18 39
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N 18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P 18 36
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N 18 36
SATA			
	SATA_85D	SATA	SATA_HDD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_HDD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_HDD_R2D_P 42 92
	SATA_85D	SATA	SATA_HDD_R2D_N 42 92
	SATA_85D	SATA	SATA_HDD_D2R_P 18 42
	SATA_85D	SATA	SATA_HDD_D2R_N 18 42
	SATA_85D	SATA	SATA_HDD_D2R_C_P 42 92
	SATA_85D	SATA	SATA_HDD_D2R_C_N 42 92
	SATA_85D	SATA	SATA_ODD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_ODD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_ODD_R2D_P 42 92
	SATA_85D	SATA	SATA_ODD_R2D_N 42 92
	SATA_85D	SATA	SATA_ODD_D2R_P 18 42
	SATA_85D	SATA	SATA_ODD_D2R_N 18 42
	SATA_85D	SATA	SATA_ODD_D2R_C_P 42 92
	SATA_85D	SATA	SATA_ODD_D2R_C_N 42 92
CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_P 11 21
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_N 11 21
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_P 11 18
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_N 11 18
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_P 11 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_N 11 25
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_P 11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_N 11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_N 18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_P 18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_N 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_N
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_N 18 26

SYNC_MASTER=K60 SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 102 OF 110
SHEET 84 OF 92

PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_REQ0_L	20
	PCI_55S	PCI	PCI_REQ1_L	20
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	20 27
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	18 27
	LPC_55S	LPC	LPC_AD<3..0>	18 45 47
	LPC_55S	LPC	LPC_FRAME_L	18 45 47
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	20 27
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	27 47
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R	9 19 91
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK	9 45 91
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 27
	USB_90D	USB	USB_EXTA_P	34 43
	USB_90D	USB	USB_EXTA_N	34 43
	USB_90D	USB	USB_PORT0_P	43
	USB_90D	USB	USB_PORT0_N	43
	USB_90D	USB	USB_EXTB_P	35 43
	USB_90D	USB	USB_EXTB_N	35 43
	USB_90D	USB	USB_PORT1_P	43
	USB_90D	USB	USB_PORT1_N	43
	USB_90D	USB	USB_EXTC_P	34 43
	USB_90D	USB	USB_EXTC_N	34 43
	USB_90D	USB	USB_PORT2_P	43
	USB_90D	USB	USB_PORT2_N	43
	USB_90D	USB	USB_EXTD_P	35 43
	USB_90D	USB	USB_EXTD_N	35 43
	USB_90D	USB	USB_D_MUXED_P	43
	USB_90D	USB	USB_D_MUXED_N	43
	USB_90D	USB	USB_PORT3_P	43
	USB_90D	USB	USB_PORT3_N	43
	USB_90D	USB	USB_CAMERA_P	34 44
	USB_90D	USB	USB_CAMERA_N	34 44
	USB_90D	USB	USB_CAMERA_L_P	44 92
	USB_90D	USB	USB_CAMERA_L_N	44 92
	USB_90D	USB	USB_BT_P	35 44
	USB_90D	USB	USB_BT_N	35 44
	USB_90D	USB	USB_BT_L_P	44 92
	USB_90D	USB	USB_BT_L_N	44 92
	USB_90D	USB	USB_IR_P	34 44
	USB_90D	USB	USB_IR_N	34 44
	USB_90D	USB	USB_IR_L_P	44 92
	USB_90D	USB	USB_IR_L_N	44 92
	USB_90D	USB	USB_SDCARD_P	35 44
	USB_90D	USB	USB_SDCARD_N	35 44
	USB_90D	USB	USB_SDCARD_L_P	44 92
	USB_90D	USB	USB_SDCARD_L_N	44 92
	USB_90D	USB	USB_WM_P	20 44
	USB_90D	USB	USB_WM_N	20 44
	USB_90D	USB	USB_WM_L_P	44
	USB_90D	USB	USB_WM_L_N	44
	USB_90D	USB	USB_MINI_P	
	USB_90D	USB	USB_MINI_N	
	USB_90D	USB	USB_BRCRYPT_P	20 44
	USB_90D	USB	USB_BRCRYPT_N	20 44
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	26
	CLK_XTAL	XTAL	CK505_XTAL_OUT	26
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK	18 26
	USB_90D	USB	USB_BRCRYPT_L_P	44
	USB_90D	USB	USB_BRCRYPT_L_N	44
	USB_90D	USB	USB_HUB1_UP_P	20 34
	USB_90D	USB	USB_HUB1_UP_N	20 34
	USB_90D	USB	USB_HUB2_UP_P	20 35
	USB_90D	USB	USB_HUB2_UP_N	20 35

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_55S	SPI	SPI_CLK_R	18 47 54
	SPI_55S	SPI	SPI_CLK	54
	SPI_55S	SPI	SPI_MOSI_R	18 47 54
	SPI_55S	SPI	SPI_MOSI	54
	SPI_55S	SPI	SPI_MISO	18 47 54
	SPI_55S	SPI	SPI_MISO_R	54
	SPI_55S	SPI	SPI_CS0_R_L	18 47
	SPI_55S	SPI	SPI_CS0_L	47
	SPI_55S	SPI	SPI_MLB_CS_L	47 54
	SPI_55S	SPI	SPI_ALT_CS_L	47
	SPI_55S	SPI	SPIROM_USE_MLB	21 47
	SPI_55S	SPI	SPI_ALT_MOSI	47
	SPI_55S	SPI	SPI_ALT_MISO	47
	SPI_55S	SPI	SPI_ALT_CLK	47
	HDA_55S	HDA	HDA_BIT_CLK	18 55
	HDA_55S	HDA	HDA_BIT_CLK_R	18
	HDA_55S	HDA	HDA_RST_L	18 55
	HDA_55S	HDA	HDA_RST_R_L	18
	HDA_55S	HDA	HDA_SDOUT	18 55
	HDA_55S	HDA	HDA_SDOUT_R	18
	HDA_55S	HDA	HDA_SYNC	18 55
	HDA_55S	HDA	HDA_SYNC_R	18
	HDA_55S	HDA	HDA_SDIN0	18 55
	HDA_55S	HDA	AUD_SDI_R	55
		HDA	AUD_SPDIF_IN	59 81
		HDA	AUD_SPDIF_OUT	55 59
		HDA	AUD_SPDIF_CHIP	55
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1L_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO1R_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2L_POUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTLO2R_POUT	58 59 92
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT	18 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN	18 27
	PCH_55S	COMP_PCH	PCH_USB_RBIAS	20
	PCH_55S	COMP_PCH	PCH_SATAICOMP	18
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	18
	PCH_55S	COMP_PCH	PCH_DMI_COMP	19
	CLK_XTAL	XTAL	USB_HUB1_XTAL1	34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2	34
	PCH_55S	COMP_PCH	USB_HUB1_RBIAS	34
	CLK_XTAL	XTAL	USB_HUB2_XTAL1	35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2	35
	PCH_55S	COMP_PCH	USB_HUB2_RBIAS	35

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: IBEX PEAK CONSTRAINTS

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: G.0.0

BRANCH:

PAGE: 103 OF 110

SHEET: 85 OF 92

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

SOURCE: BROADCOM 5764-DS04-RDS. PAGE 38

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	ENET_50S	ENET_SE	ENET_RDAC 36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTALI 36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTALO 36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTAL 36
	ENET_100D	ENET_DIFF	ENET_MDI_P<3..0> 36 38
	ENET_100D	ENET_DIFF	ENET_MDI_N<3..0> 36 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_P<3..0> 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_N<3..0> 38
	ENET_100D	ENET_MII	PCIE_ENET_R2D_P 36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_N 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_P 18 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_N 18 36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_P 18 36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_N 18 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_P 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_N 36

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	FW_110D	FW_TP	FW_PORT0_TPA_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPA_N 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P 40 41
	FW_110D	FW_TP	FW_PORT0_TPB_N 40 41

PORT 1 & 2 NOT USED

	FW_110D	FW_TP	FW_P0_TPA_L_P 40
	FW_110D	FW_TP	FW_P0_TPA_L_N 40
	FW_110D	FW_TP	FW_P0_TPB_L_P 40
	FW_110D	FW_TP	FW_P0_TPB_L_N 40

UNUSED FW NETS PHYSICAL PROPERTIES

	FW_110D	FW_TP	FW_P1_TPA_P 39 40
	FW_110D	FW_TP	FW_P1_TPA_N 39 40
	FW_110D	FW_TP	FW_P2_TPA_P 39 40
	FW_110D	FW_TP	FW_P2_TPA_N 39 40

AUDIO MIC PHYSICAL PROPERTIES

	AUDIO_PHY	AUDIO	AUD_MIC1_IN_N 59 60
	AUDIO_PHY	AUDIO	AUD_MIC1_IN_P 59 60

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_PHY	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=STANDARD	?

SYNC MASTER=K60 AARON SYNC DATE=07/01/2009

PAGE TITLE

ENET/FIREWIRE CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 104 OF 110

SHEET 86 OF 92

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	7

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ASSINGED IN CONT. MGR.			
	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0> 80
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0> 80
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0> 77
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0> 77
	DP_85D	DISPLAYPORT	DP_INT_LINK_P<3..0> 77 79
	DP_85D	DISPLAYPORT	DP_INT_LINK_N<3..0> 77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_P 77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_N 77 79
	DP_85D	DISPLAYPORT	DP_EXT_LINK_P<3..0> 78 80
	DP_85D	DISPLAYPORT	DP_EXT_LINK_N<3..0> 78 80
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_P 78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_N 78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_P<3..0> 78
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_N<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_P<3..0> 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_N<3..0> 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_P 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_N 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_P 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_N 73 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0> 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0> 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_P 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_N 79
	DP_85D	DISPLAYPORT	DP_MUX_P<3..0> 78 79
	DP_85D	DISPLAYPORT	DP_MUX_N<3..0> 78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_P 78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_N 78 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_P 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_N 79
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0> 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0> 79
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_P 78
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_N 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_P<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_N<3..0> 78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P 73 76
DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N 73 76
DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P 73 76
DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N 73 76
DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P 74 76
DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N 74 76
DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P 74 76
DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N 74 76
DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0> 73 76
DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0> 73 76
DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0> 73 76
DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0> 73 76
DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0> 74 76
DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0> 74 76
DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0> 74 76
DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0> 74 76

SYNC MASTER=K60 AARON SYNC DATE=07/01/2009

PAGE TITLE
GRAPHICS CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 105 OF 110
SHEET 87 OF 92

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48 88
R130	SMB_55S	SMB	SMBUS_PCH_S0_CLK	48
R133	SMB_55S	SMB	SMBUS_PCH_S0_DATA	48
R160	SMB_55S	SMB	SMBUS_PCH_CLK	10 48
R163	SMB_55S	SMB	SMBUS_PCH_DATA	10 48
R137	SMB_55S	SMB	SML_PCH_0_CLK	10 48
R139	SMB_55S	SMB	SML_PCH_0_DATA	10 48
R138	SMB_55S	SMB	SML_PCH_1_CLK	10 48
R140	SMB_55S	SMB	SML_PCH_1_DATA	10 48
R192	CLK_XTAL	XTAL	SMC_EXTAL	45 46
R190	CLK_XTAL	XTAL	SMC_XTAL	45 46

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
R87	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
R88	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
R89	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	51
R90	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	51
R200	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
R201	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
R93	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	51
R94	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	51
R101	THERM_DIFF	THERMAL	SNS_LCD_P	51 92
R102	THERM_DIFF	THERMAL	SNS_LCD_N	51 92
R103	THERM_DIFF	THERMAL	SNS_ODD_P	51 92
R104	THERM_DIFF	THERMAL	SNS_ODD_N	51 92
R105	THERM_DIFF	THERMAL	SNS_CPU_H_P	51
R106	THERM_DIFF	THERMAL	SNS_CPU_H_N	51
R198	THERM_DIFF	THERMAL	SNS_SKIN_P	51 92
R199	THERM_DIFF	THERMAL	SNS_SKIN_N	51 92
R107	THERM_DIFF	THERMAL	SNS_AMB_P	51 92
R110	THERM_DIFF	THERMAL	SNS_AMB_N	51 92
R111	THERM_DIFF	THERMAL	SNS_MXM_P	51
R112	THERM_DIFF	THERMAL	SNS_MXM_N	51
R124	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 51
R125	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 51
R115		THERMAL	HDD_OOB_TEMP_FILT	51 92
R133		THERMAL	HDD_OOB_TEMP	51
R139		THERMAL	HDD_OOB_TEMP_R	51
R132		THERMAL	SMC_HDD_OOB_TEMP	51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
R97	THERM_DIFF	THERMAL	MXM_ISENSE_P	50
R98	THERM_DIFF	THERMAL	MXM_ISENSE_N	50
R99	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_P	49
R100	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_N	49
R148	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_P	49
R149	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_N	49
R150	THERM_DIFF	THERMAL	SENSE_CPU_1V5_P	49
R153	THERM_DIFF	THERMAL	SENSE_CPU_1V5_N	49
R152	THERM_DIFF	THERMAL	SENSE_CPU_VTT_P	49
R155	THERM_DIFF	THERMAL	SENSE_CPU_VTT_N	49
R181	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_P	
R182	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_N	
R183	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_P	
R184	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_N	
R160		THERMAL	GND_SMC_AVSS	45 46 49 50
R124		THERMAL	SMC_CPU_1V5_ISENSE	46 49
R125		THERMAL	SMC_CPU_1V5_ISENSE_R	49
R122		THERMAL	SMC_CPU_1V5_VSENSE	46 49
R163		THERMAL	SMC_CPU_VTT_ISENSE	46 49
R164		THERMAL	SMC_CPU_VTT_ISENSE_R	49
R165		THERMAL	SMC_CPU_VTT_VSENSE	46 49
R166		THERMAL	SMC_CPU_1V8_ISENSE	46 49
R167		THERMAL	SMC_CPU_1V8_ISENSE_R	
R168		THERMAL	SMC_CPU_1V8_VSENSE	46 49
R128		THERMAL	SMC_CPU_VSENSE	45 49
R113	VID_PHY	VR_CTL	VR_CPU_IOUT	13 64
R131	THERM_DIFF	THERMAL	VR_ISNS_CPU_P	49
R130	THERM_DIFF	THERMAL	VR_ISNS_CPU_N	49
R129		THERMAL	SNS_PS_CPU_ISNS	49
R114		THERMAL	SMC_CPU_ISENSE	45 49
R169		THERMAL	SMC_CPU_INPUT_ISENSE	46
R171		THERMAL	SMC_CPU_INPUT_VSENSE	46
R172		THERMAL	SMC_DIMM_1V5_ISENSE	46 50
R173		THERMAL	SMC_1V5_S3_ISENSE_R	
R174		THERMAL	SMC_DIMM_1V5_VSENSE	46 50
R175		THERMAL	SMC_GPU_ISENSE	45 50
R176		THERMAL	SMC_MXM_ISENSE_R	50
R180		THERMAL	SMC_GPU_VSENSE	45 50

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 106 OF 110

SHEET 88 OF 92

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE PHYSICAL	SPACING	VOLTAGE		
POWER	SWITCHNODE	1.5V	B128	VR_CPU_PHASE1 65
POWER	SWITCHNODE	1.5V	B129	VR_CPU_PHASE2 65
POWER	SWITCHNODE	1.5V	B130	VR_CPU_PHASE3 65
POWER	SWITCHNODE	1.5V	B131	VR_CPU_PHASE4 66
POWER	SWITCHNODE	3.3V	B132	P3V3S5_REG_PHASE 69
POWER	SWITCHNODE	5V	B133	P5VS3_REG_PHASE 69
POWER	SWITCHNODE	1.1V	B134	VTT_REG_PHASE1 67
POWER	SWITCHNODE	1.1V	B135	VTT_REG_PHASE2 67
POWER	SWITCHNODE	3.4V	B136	P3V42G3H_SW 71
POWER	SWITCHNODE	1.05V	B137	PCHCORE_REG_PHASE 68
POWER	SWITCHNODE	1.05V	B138	P1V05_S5_REG_PHASE 71
POWER	SWITCHNODE	1.5V	B139	DDR_REG_PHASE 70
POWER	SWITCHNODE	1.8V	B140	P1V8_REG_PHASE 70
POWER	POWER	1.5V	B141	PP0V75_S3_MEM_VREFCA_A 28 30
POWER	POWER	1.5V	B142	PP0V75_S3_MEM_VREFCA_B 28 31
POWER	POWER	1.5V	B143	PP0V75_S3_MEM_VREFDQ_A 28 30
POWER	POWER	1.5V	B144	PP0V75_S3_MEM_VREFDQ_B 28 31
POWER	POWER	12V	B145	PP12V_S0_CPUVTT_FLTD
POWER	POWER	12V	B146	PP12V_AUD_SPKRAMP_FLANE 57 58 60
POWER	POWER	12V	B147	PP12V_LCD 77
POWER	POWER	12V	B148	PP12V_LCD_CONN 77
POWER	POWER	12V	B149	PP12V_S0 6 63
POWER	POWER	12V	B150	PP12V_S0_CPU_FLTRD 64 65 66
POWER	POWER	12V	B175	PP12V_S0_FAN0_L 52 92
POWER	POWER	12V	B176	PP12V_S0_FAN1_L 52 92
POWER	POWER	12V	B177	PP12V_S0_FAN2_L 53 92
POWER	POWER	12V	B604	PP12V_G3H 6 71
POWER	POWER	12V	B605	PP12V_G3H_R 71
POWER	POWER	12V	B152	PP12V_S5 6
POWER	POWER	12V	B155	P12V_S0_FW
POWER	POWER	12V	B274	P12V_S0_FW_CL
POWER	POWER	12V	B275	P12V_S0_FW_D
POWER	POWER	12V	B276	P12V_S0_FW_R
POWER	POWER	12V	B265	FW_PORT0_VP 41
POWER	POWER	12V	B266	FW_PORT0_VP_F 41
POWER	POWER	12V	B264	PPVP_FW_PHY_CPS 40 41
POWER	POWER	12V	B549	PP12V_S3 6
POWER	POWER	12V	B551	PP12V_S3_WM_FLT 44
POWER	POWER	1.1V	B259	PPVCORE_S0_CPU 6
POWER	POWER	1.1V	B258	PPVCORE_S0_CPU_REG1 65
POWER	POWER	1.1V	B562	PPVCORE_S0_CPU_REG2 65
POWER	POWER	1.1V	B563	PPVCORE_S0_CPU_REG3 65
POWER	POWER	1.1V	B565	PPVCORE_S0_CPU_REG4 66
POWER	POWER	1.05V	B256	PP1V05_SM_SOURCE 72
POWER	POWER	1.05V	B182	PP1V05_S0 6
POWER	POWER	1.05V	B173	PP1V05_S0_CK505_F 26
POWER	POWER	1.05V	B181	PP1V05_S0_PCH_VCCADPLLA 17 22
POWER	POWER	1.05V	B183	PP1V05_S0_PCH_VCCADPLLA_F
POWER	POWER	1.05V	B184	PP1V05_S0_PCH_VCCADPLLB 17 22
POWER	POWER	1.05V	B185	PP1V05_S0_PCH_VCCADPLLB_F
POWER	POWER	1.05V	B186	PP1V05_S0_PCH_VCCAPLL_EXP 22 24
POWER	POWER	1.05V	B187	PP1V05_S0_PCH_VCCAPLL_FDI 22 24
POWER	POWER	1.05V	B188	PP1V05_S0_PCH_VCCAPLL_SATA 22 24
POWER	POWER	1.05V	B189	PP1V05_S0_PCH_VCCA_CLK 22 24
POWER	POWER	1.05V	B190	PP1V05_S0_PCH_VCCA_CLK_F 24
POWER	POWER	1.05V	B599	PP1V05_S0_CIO_VDD1P0_DP
POWER	POWER	1.05V	B599	PP1V05_S0_CIO_VDD1P0_DP_PLL
POWER	POWER	1.05V	B614	PP1V05_SM_PCH_LAN 6
POWER	POWER	1.05V	B192	PP1V05_S5 6
POWER	POWER	1.05V	B577	PP1V05_SM 6
POWER	POWER	1.1V	B265	PPVTT_S0 6
POWER	POWER	1.1V	B555	PPVTT_S0_CPU 6 49
POWER	POWER	0.75V	B266	PPVTT_S0_DDR 6
POWER	POWER	0.75V	B613	PP0V75_S0 6
POWER	POWER	1.2V	B190	PP1V2_S5_FNET 37
POWER	POWER	1.5V	B192	PP1V5_S0 6
POWER	POWER	1.5V	B193	PP1V5_S0_CK505_F 26
POWER	POWER	1.5V	B587	PP1V5_S0_CK505_R 26
POWER	POWER	1.5V	B195	PP1V5_S3 6
POWER	POWER	1.5V	B578	PP1V5_CPU_MEM 6 49
POWER	POWER	1.5V	B206	PP1V8R1V5_S0_PCH_VCCVRM 22 24
POWER	POWER	1.5V	B195	PP1V5_FW_VDDA 39
POWER	POWER	1.5V	B204	PP1V8_S0 6
POWER	POWER	1.8V	B204	PP1V8_S0_CPU 6 49
POWER	POWER	1.96V	B206	PP1V96_FW_PLLVDD 39
POWER	POWER	1.96V	B206	PP1V95_FW_FWPHY 39 40

POWER NET PROPERTIES

NET_TYPE PHYSICAL	SPACING	VOLTAGE		
POWER	POWER	3.3V	B618	PP3V3_S0 6
POWER	POWER	3.3V	B619	PP3V3_S0_CK505_F 26
POWER	POWER	3.3V	B214	PP3V3_S0_DPAUX 80
POWER	POWER	3.3V	B216	PP3V3_S0_DPFUSE 80
POWER	POWER	3.3V	B215	PP3V3_S0_DPPWR 80
POWER	POWER	3.3V	B252	PP3V3_S0_HS_F 61
POWER	POWER	3.3V	B676	PP3V3_S0M 6
POWER	POWER	3.3V	B618	PP3V3_MINI 33
POWER	POWER	3.3V	B618	PP3V3_ENET 36 37
POWER	POWER	3.3V	B228	PP3V3_S0_PCH_VCCA_DAC 17 22
POWER	POWER	3.3V	B228	PP3V3_S0_PCH_VCCA_DAC_F
POWER	POWER	3.3V	B678	PP3V3_S0_TSENS_R 51
POWER	POWER	3.3V	B224	PP3V3_S3 6 92
POWER	POWER	3.3V	B659	PP3V3_S3_BT_FLT 44
POWER	POWER	3.3V	B240	PP3V3_S3_SDCARD_FLT 44
POWER	POWER	3.3V	B658	PP3V3_S3_WM_FLT 44
POWER	POWER	3.3V	B235	PP3V3_S5 6
POWER	POWER	3.3V	B697	PPVTT_S3_DDR_BUF 70
POWER	POWER	3.3V	B676	PPV_S0_MXM_PWRSRC 50
POWER	POWER	3.3V	B266	PPVOUT_S0_PCH_DCPSST 22
POWER	POWER	3.3V	B680	PPVOUT_S5_PCH_DCPSUS 22
POWER	POWER	3.3V	B666	PPVOUT_S5_PCH_DCPSUSBYP 22
POWER	POWER	3.3V	B262	PPVOUT_G3_PCH_DCPRTC 22
POWER	POWER	3.3V	B610	PPVOUT_SO_PCH_VCCRTC_NCTF
POWER	POWER	3.3V	B695	PPVBATT_G3_RTC 27
POWER	POWER	3.3V	B266	PPVBATT_G3_RTC_R 27
POWER	POWER	3.3V	B209	PP3V3_AUDIO_SPDIF_JACK 59
POWER	POWER	3.3V	B606	PP3V3_FW_AVDD 39
POWER	POWER	3.3V	B218	PP3V3_FW_ESD 41
POWER	POWER	3.3V	B218	PP3V3_FW_PLLVDD 39
POWER	POWER	3.3V	B410	PP3V3_FW_VDDA 39
POWER	POWER	3.3V	B215	PP3V3_G3_RTC 18 22 24 27
POWER	POWER	3.3V	B214	PP_ENET_CTRL12 37
POWER	POWER	3.4V	B230	PP3V3_G3H_SMC_AVCC 45
POWER	POWER	3.3V	B231	PP3V3_G3H_AVREF_SMC 45 46
POWER	POWER	3.42V	B606	PP3V42_G3H 6
POWER	POWER	3.42V	B609	PP3V42_G3H_R 71
POWER	POWER	4.5V	B597	4V5_REG_IN 55
POWER	POWER	4.5V	B238	PP4V5_AUDIO_ANALOG 55
POWER	POWER	5V	B233	PP5V_S0 6 92
POWER	POWER	5V	B238	PP5V_S0_CPU_VCORE_VCC 44
POWER	POWER	5V	B238	PP5V_S0_PCH_V5REF 22 24
POWER	POWER	5V	B600	PP5V_S0_SATA_FET 42
POWER	POWER	5V	B645	PP5V_S3 6
POWER	POWER	5V	B249	PP5V_S3_DDR_REG_V5PILT 70
POWER	POWER	5V	B238	PP5V_S3_CAMERA_FLT 44
POWER	POWER	5V	B645	PP5V_S3_IR_FLT 44
POWER	POWER	5V	B608	VREFMARGIN_DIMMA_P5V 28
POWER	POWER	5V	B608	VREFMARGIN_DIMMB_P5V 28
POWER	POWER	5V	B240	PP5V_S5 6
POWER	POWER	5V	B244	PP5V_S5_PCH_V5REFSUS 22 24
POWER	POWER	5V	B688	PP5V_CPUVTT_VR 67
POWER	POWER	5V	B247	PP5V_USB2_PORT0 43
POWER	POWER	5V	B250	PP5V_USB2_PORT0_F 43
POWER	POWER	5V	B248	PP5V_USB2_PORT1 43
POWER	POWER	5V	B251	PP5V_USB2_PORT1_F 43
POWER	POWER	5V	B253	PP5V_USB2_PORT2 43
POWER	POWER	5V	B262	PP5V_USB2_PORT2_F 43
POWER	POWER	5V	B254	PP5V_USB2_PORT3 43
POWER	POWER	5V	B255	PP5V_USB2_PORT3_F 43
POWER	POWER		B648	DDR_REG_PGND 70
POWER	POWER		B646	DDR_REG_CSGND 70

SENSING NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
SNS_DIFF	THERMAL	B155	VR_CPU_ISNS1_P 64 65
SNS_DIFF	THERMAL	B156	VR_CPU_ISNS1_N 64 65
SNS_DIFF	THERMAL	B157	VR_CPU_ISNS1_R_P 64
SNS_DIFF	THERMAL	B158	VR_CPU_ISNS1_R_N 64
SNS_DIFF	THERMAL	B160	VR_CPU_ISNS2_P 64 65
SNS_DIFF	THERMAL	B159	VR_CPU_ISNS2_N 64 65
SNS_DIFF	THERMAL	B161	VR_CPU_ISNS2_R_P 64
SNS_DIFF	THERMAL	B162	VR_CPU_ISNS2_R_N 64
SNS_DIFF	THERMAL	B163	VR_CPU_ISNS3_P 64 65
SNS_DIFF	THERMAL	B164	VR_CPU_ISNS3_N 64 65
SNS_DIFF	THERMAL	B165	VR_CPU_ISNS3_R_P 64
SNS_DIFF	THERMAL	B166	VR_CPU_ISNS3_R_N 64
SNS_DIFF	THERMAL	B167	VR_CPU_ISNS4_P 64 66
SNS_DIFF	THERMAL	B168	VR_CPU_ISNS4_N 64 66
SNS_DIFF	THERMAL	B169	VR_CPU_ISNS4_R_P 64
SNS_DIFF	THERMAL	B170	VR_CPU_ISNS4_R_N 64
SNS_DIFF	THERMAL	B640	VR_CPU_ISNS1_XW_P 65
SNS_DIFF	THERMAL	B639	VR_CPU_ISNS1_XW_N 65
SNS_DIFF	THERMAL	B641	VR_CPU_ISNS2_XW_P 65
SNS_DIFF	THERMAL	B642	VR_CPU_ISNS2_XW_N 65
SNS_DIFF	THERMAL	B643	VR_CPU_ISNS3_XW_P 65
SNS_DIFF	THERMAL	B644	VR_CPU_ISNS3_XW_N 65
SNS_DIFF	THERMAL	B637	VR_CPU_ISNS4_XW_P 66
SNS_DIFF	THERMAL	B638	VR_CPU_ISNS4_XW_N 66
SNS_DIFF		B156	CPU_VCC_PKG_SENSE_P 13 49 64
SNS_DIFF		B636	CPU_VCC_PKG_SENSE_N 13 64
SNS_DIFF		B154	CPU_VTTSENSE_P 13 49 67
SNS_DIFF		B153	CPU_VTTSENSE_N 13 67
SNS_DIFF		B152	CPU_VTTSENSE_R_P 67
SNS_DIFF		B151	CPU_VTTSENSE_R_N 67
SNS_DIFF		B158	VR_CPU_VSEN 64
SNS_DIFF		B159	VR_CPU_RGND 64
SNS_DIFF		B154	VR_CPU_VSNS_R_N 64
SNS_DIFF		B150	VR_CPU_VSNS_R_P 64
SNS_DIFF		B156	VR_CPU_VSNS_XW_P 64
SNS_DIFF		B154	VR_CPU_VSNS_XW_N 64

VR CTRL NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VR_CTL_PHY	VR_CTL	B278	VR_CPU_PH1_SNUB 65
VR_CTL_PHY	VR_CTL	B331	VR_CPU_PH2_SNUB 65
VR_CTL_PHY	VR_CTL	B330	VR_CPU_PH3_SNUB 65
VR_CTL_PHY	VR_CTL	B340	VR_CPU_PH4_SNUB 66
VR_CTL_PHY	VR_CTL	B341	VR_CPU_PWM1 64 65
VR_CTL_PHY	VR_CTL	B342	VR_CPU_PWM2 64 65
VR_CTL_PHY	VR_CTL	B343	VR_CPU_PWM2_R 64
VR_CTL_PHY	VR_CTL	B344	VR_CPU_PWM3 64 65
VR_CTL_PHY	VR_CTL	B345	VR_CPU_PWM3_R 64
VR_CTL_PHY	VR_CTL	B346	VR_CPU_PWM4 64 66
VR_CTL_PHY	VR_CTL	B347	VR_CPU_PWM4_R 64
VR_CTL_PHY	VR_CTL	B348	VR_CPU_REF 64
VR_CTL_PHY	VR_CTL	B349	VR_CPU_SS 64
VR_CTL_PHY	VR_CTL	B350	VR_CPU_TCOMP 64
VR_CTL_PHY	VR_CTL	B351	VR_CPU_TM 64
VR_CTL_PHY	VR_CTL	B352	VR_CPU_BOOT1_RC 65
VR_CTL_PHY	VR_CTL	B353	VR_CPU_BOOT2_RC 65
VR_CTL_PHY	VR_CTL	B354	VR_CPU_BOOT3_RC 65
VR_CTL_PHY	VR_CTL	B355	VR_CPU_COMP 64
VR_CTL_PHY	VR_CTL	B357	VR_CPU_COMP_R 64
VR_CTL_PHY	VR_CTL	B358	VR_CPU_COMP_RC 64
VR_CTL_PHY	VR_CTL	B359	VR_CPU_DAC 64
VR_CTL_PHY	VR_CTL	B360	VR_CPU_DRV1_BOOT 65
VR_CTL_PHY	VR_CTL	B361	VR_CPU_DRV1_GDSEL 65
VR_CTL_PHY	SWITCHNODE	B362	VR_CPU_DRV1_LGATE 65
VR_CTL_PHY	SWITCHNODE	B363	VR_CPU_DRV1_UGATE 65
VR_CTL_PHY	VR_CTL	B364	VR_CPU_DRV2_BOOT 65
VR_CTL_PHY	VR_CTL	B365	VR_CPU_DRV2_GDSEL 65
VR_CTL_PHY	SWITCHNODE	B366	VR_CPU_DRV2_LGATE 65
VR_CTL_PHY	SWITCHNODE	B370	VR_CPU_DRV2_UGATE 65
VR_CTL_PHY	VR_CTL	B371	VR_CPU_DRV3_BOOT 65
VR_CTL_PHY	VR_CTL	B372	VR_CPU_DRV3_GDSEL 65
VR_CTL_PHY	SWITCHNODE	B373	VR_CPU_DRV3_LGATE 65
VR_CTL_PHY	SWITCHNODE	B377	VR_CPU_DRV3_UGATE 65
VR_CTL_PHY	VR_CTL	B378	VR_CPU_DRV4_BOOT 66
VR_CTL_PHY	VR_CTL	B379	VR_CPU_DRV4_GDSEL 66
VR_CTL_PHY	SWITCHNODE	B380	VR_CPU_DRV4_LGATE 66
VR_CTL_PHY	SWITCHNODE	B384	VR_CPU_DRV4_UGATE 66
VR_CTL_PHY	VR_CTL	B387	VR_CPU_FAN 64
VR_CTL_PHY	VR_CTL	B388	VR_CPU_FB 64
VR_CTL_PHY	VR_CTL	B389	VR_CPU_FB_R 64
VR_CTL_PHY	VR_CTL	B392	VR_CPU_FS 64
VR_CTL_PHY	VR_CTL	B393	VR_CPU_IMON 49 64
VR_CTL_PHY	VR_CTL	B397	VR_CPU_IOUT_PD 64
VR_CTL_PHY	SWITCHNODE	B391	PCHCORE_REG_UGATE 68
VR_CTL_PHY	SWITCHNODE	B392	PCHCORE_REG_LGATE 68
VR_CTL_PHY	VR_CTL	B393	PCHCORE_REG_VFB 68
VR_CTL_PHY	VR_CTL	B397	PCHCORE_REG_TON 68
VR_CTL_PHY	VR_CTL	B398	PCHCORE_REG_TRIP 68
VR_CTL_PHY	VR_CTL	B399	PCHCORE_REG_BOOT 68
VR_CTL_PHY	VR_CTL	B592	PCHCORE_REG_BOOT_R 68
VR_CTL_PHY	VR_CTL	B400	VTT_REG_BOOT1 67
VR_CTL_PHY	VR_CTL	B401	VTT_REG_BOOT2 67
VR_CTL_PHY	VR_CTL	B402	VTT_REG_COMP 67
VR_CTL_PHY	VR_CTL	B403	VTT_REG_FB 67
VR_CTL_PHY	VR_CTL	B404	VTT_REG_FS 67
VR_CTL_PHY	VR_CTL	B405	VTT_REG_ICOMP 67
VR_CTL_PHY	VR_CTL	B406	VTT_REG_IREF 67
VR_CTL_PHY	VR_CTL	B407	VTT_REG_ISUM 67
VR_CTL_PHY	SWITCHNODE	B408	VTT_REG_LGATE1 67
VR_CTL_PHY	SWITCHNODE	B409	VTT_REG_LGATE2 67
VR_CTL_PHY	VR_CTL	B410	VTT_REG_OCSET 67
VR_CTL_PHY	VR_CTL	B411	VTT_REG_OFST 67
VR_CTL_PHY	VR_CTL	B412	VTT_REG_REF 67
VR_CTL_PHY	VR_CTL	B413	VTT_REG_RGND 67
VR_CTL_PHY	VR_CTL	B414	VTT_REG_SEL 67
VR_CTL_PHY	VR_CTL	B415	VTT_REG_UGATE2 67
VR_CTL_PHY	VR_CTL	B416	VTT_REG_UGATE1 67
VR_CTL_PHY	VR_CTL	B418	VTT_REG_PH1_SNUB 67
VR_CTL_PHY	VR_CTL	B419	VTT_REG_PH2_SNUB 67
VR_CTL_PHY	VR_CTL	B417	VTT_REG_VSEN 67
VR_CTL_PHY	VR_CTL	B599	P1V05S5_REG_VFB 71
VR_CTL_PHY	VR_CTL	B607	P3V42G3H_BOOST 71
VR_CTL_PHY	VR_CTL	B608	P3V42G3H_FB 71

VR CTRL NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VR_CTL_PHY	VR_CTL	B437	DDR_REG_CS 70
VR_CTL_PHY	VR_CTL	B438	DDR_REG_FB 70
VR_CTL_PHY	SWITCHNODE	B439	DDR_REG_LGATE 70
VR_CTL_PHY	SWITCHNODE	B596	DDR_REG_UGATE 70
VR_CTL_PHY	VR_CTL	B440	DDR_REG_BOOT 70
VR_CTL_PHY	VR_CTL	B441	DDR_REG_BOOT_R 70
VR_CTL_PHY	VR_CTL	B442	DDR_REG_VDDQSNS 70
VR_CTL_PHY	VR_CTL	B444	DDR_REG_VTTSNS 70
VR_CTL_PHY	VR_CTL	B446	P1V8_REG_POR 70
VR_CTL_PHY	VR_CTL	B450	P3V3S5_REG_BOOT 69
VR_CTL_PHY	VR_CTL	B452	P3V3S5_REG_BOOT_R 69
VR_CTL_PHY	VR_CTL	B453	P3V3S5_REG_FB 69
VR_CTL_PHY	VR_CTL	B455	P3V3S5_REG_ISEN 69
VR_CTL_PHY	SWITCHNODE	B465	P3V3S5_REG_LGATE 69
VR_CTL_PHY	VR_CTL	B454	P3V3S5_REG_OCSET 69
VR_CTL_PHY	SWITCHNODE	B458	P3V3S5_REG_UGATE 69
VR_CTL_PHY	VR_CTL	B459	P3V3S5_REG_SNUB 69
VR_CTL_PHY	VR_CTL	B460	P5VS3_REG_BOOT 69
VR_CTL_PHY	VR_CTL	B461	P5VS3_REG_FB 69
VR_CTL_PHY	VR_CTL	B462	P5VS3_REG_ISEN 69
VR_CTL_PHY	SWITCHNODE	B463	P5VS3_REG_LGATE 69
VR_CTL_PHY	VR_CTL	B465	P5VS3_REG_OCSET 69
VR_CTL_PHY	SWITCHNODE	B464	P5VS3_REG_UGATE 69

VR VID NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VID_PHY	VR_CTL	B499	CPU_VID<0> 13 16 64
VID_PHY	VR_CTL	B498	CPU_VID<1> 13 16 64
VID_PHY	VR_CTL	B523	CPU_VID<2> 13 16 64
VID_PHY	VR_CTL	B522	CPU_VID<3> 13 16 64
VID_PHY	VR_CTL	B524	CPU_VID<4> 13 16 64
VID_PHY	VR_CTL	B521	CPU_VID<5> 13 16 64
VID_PHY	VR_CTL	B525	CPU_VID<6> 13 16 64
VID_PHY	VR_CTL	B520	CPU_VID<7> 13 16 64
VID_PHY	VR_CTL	B554	CPU_PSI_L 13 16 64

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	39_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.2MM	7

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE: POWER CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 107 OF 110
SHEET 89 OF 92

8 7 6 5 4 3 2 1

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SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE

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Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION G.0.0

BRANCH

PAGE 108 OF 110

SHEET 90 OF 92

PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

	NET_TYPE PHYSICAL	SPACING		
T2	PM		PLT_RESET_L	20 27
T3	PM_VTT		PLT_RESET_LS1V1_L	11
T4	PM		PM_ACDC_PS_ON	6
T5	PM		PM_BATLOW_L	15 19 45
T7	PM		PM_CLK32K_SUSCLK	9 45 85
T8	PM		PM_CLK32K_SUSCLK_R	9 19 85
T6	PM		PM_CLKRUN_L	15 19 45 47
T10	PM		PM_EXT_TS_L<0>	11 46
T9	PM		PM_EXT_TS_L<1>	11 46
T12	PM		PM_LAN_PWRGD	15 19
T11	PM_VTT		FSB_CPURSTOUT_L	11 25
T13	PM		USB_HUB_RESET_L	34 35
T25	PM_VTT		PM_MEM_PWRGD	11 19
T24	PM		PM_ME_PWRGD	19 63
T27	PM		PM_ME_S0_EN_G	72
T26	PM		PM_ME_S0_EN_G1	72
T28	PM		PM_ME_S0_EN_R	72
T30	PM		PM_MXM_PGOOD	63 74
T29	PM		PM_PCH_PWRGD	19 63
T31	PM		PM_PGOOD_DDRREG_S3	5 62 70
T33	PM		PM_PGOOD_PVCORE_CPU	5 26 63 64
T32	PM		PM_PWRBTN_L	19 25 45
T35	PM		PM_RSMRST_L	45 62
T34	PM		PM_RSMRST_PCH_L	19 62
T36	PM		PM_SLP_M_L	5 19 62
T38	PM		PM_SLP_M_R	
T39	PM		PM_SLP_S3_L	5 19 32 33 37 46 62 63
T40	PM		PM_SLP_S3_L_AND_S0_RDY	
T100	PM		PM_SLP_S4_1_L	19 62
T101	PM		PM_SLP_S4_2_L	19 45 46
T102	PM		PM_SLP_S4_3_L	5 19
T30	PM		PM_SLP_S4_L	19 32
T41	PM		PM_SLP_S5_L	19 45
T43	PM		PM_SUS_PWR_ACK	19
T22	PM_VTT		PM_SYNC	11 19
T103	PM		SDCARD_PLT_RST_L	27 44
T45	PM		PM_SYSRST_L	19 27 45
T44	PM		PM_SYS_PWRGD	19 32 63
T46	PM_VTT		PM_THRMTRIP_L	11 21 46
T48	PM		RSMRST_PWRGD	45 63
T47	PM		RTC_RESET_L	18 91
T50	PM_VTT		CPU_PWRGD	11 21 25
T49	PM		CPU_RESET_L	11 27
T51	PM		PGOOD_1V05ME_G1	63
T53	PM		PGOOD_1V05ME_G2	63
T52	PM		PGOOD_1V8_S0_G1	63
T54	PM		PGOOD_1V8_S0_G2	63
T55	PM		PGOOD_CPU_GFX_DDR	63
T58	PM		PGOOD_P12V_S3	
T57	PM		PGOOD_P1V05_ME_S5	
T56	PM		PGOOD_P1V5_S0	72
T59	PM		PGOOD_P1V8_S0	63
T61	PM		PGOOD_P3V3_ME	72
T60	PM		PGOOD_P3V3_S0	48 63 72
T67	PM		PGOOD_P3V3_S3	34 72
T62	PM		PGOOD_P5V_S0	62 72
T64	PM		PGOOD_PCH_AND_P1V8	63
T66	PM		PGOOD_PCH_S0	63
T65	PM		PGOOD_SYSPWROK	63
T63	PM		PGOOD_SYSPWROK_R	63
T68	PM		RTC_RESET_L	18 91
T69	PM		P12V_S3_EN	62 72
T71	PM		P1V05_ME_SM_EN	62 72
T70	PM		P1V5_S0_EN	62 72
T72	PM		P3V3ME_EN	62 72
T74	PM		P3V3S0_EN	62 72
T73	PM		P3V3S3_EN	62 72
T76	PM		P5VS0_EN	62 72
T75	PM		P5VS3_EN	62 69
T77	PM		PCHCORE_REG_EN	62 68
T78	PM		PCHCORE_REG_PGOOD	5 62 63 68
T79	PM		PEG_RESET_L	9 27
T80	PM		SDCARD_RESET	21 25 44 92

	NET_TYPE PHYSICAL	SPACING		
T82	PM		4V5_REG_EN	55
T81	PM		ALL_SYS_PWRGD_R	6 25 32 63
T84	PM		ALL_SYS_PWRGD_SMC	45 63
T83	PM		CK505_27MHZ_EN	26
T85	PM		CPUVTT_REG_EN	62 67
T86	PM_VTT		CPUVTT_REG_PGOOD	11 62 63 67
T87	PM		CPU_MEM_RESET_L	11 32
T88	PM		DDRVTT_EN	32 62 70
T89	PM		DEBUG_RESET_L	27 47
T90	PM		FWPHY_RESET_L	39
T91	PM		FWXIO_SNOOP_EN	39
T92	PM		FW_RESET_L	27 39
T93	PM		GFX_VR_EN	
T94	PM		GFX_VR_PGOOD	
T95	PM		LAN_RESET_L	27 36
T97	PM		MEM_RESET_L	30 31 32
T96	PM		MINI_RESET_L	27 33
T98	PM		SMC_DELAYED_PWRGD	46 63
T105	PM		SMC_LRESET_L	27 45
T99	PM		SMC_RESET_L	45 46 47
T104	PM		T28_RESET_L	
T106	PM_VTT		XDP_CPUPWRGD	11 25
T107	PM_VTT		XDP_DBRESET_L	11 25 27
T108	PM_VTT		XDP_PWRGD	25

NET PHYSICAL FOR NC NETS
REMOVE WHEN CHECKPLUS IS FIXED

	NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCIE GRAPHICS			
R95		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_N
R96		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_P
R97		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_N
R98		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_P
R99		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_N
R100		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_P
R112	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_N
R111	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_P
R115	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_N
R113	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_P
R116	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_N
R114	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_P

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE
PM RESETS ENABLES PGOOD CONST

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION G.0.0
BRANCH
PAGE 109 OF 110
SHEET 91 OF 92

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

	IN	PP5V_S3_CAMERA	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
85 44	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
85 44	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

85 44	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
85 44	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE
91 44 25 21	IN	SDCARD_RESET	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

85 44	IN	USB_BT_L_P	FUNC_TEST=TRUE
85 44	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

85 44	IN	USB_IR_L_P	FUNC_TEST=TRUE
85 44	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

84 42	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
45 42	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

84 42	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

88 51	IN	SNS_LCD_P	FUNC_TEST=TRUE
88 51	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

88 51	IN	SNS_AMB_P	FUNC_TEST=TRUE
88 51	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

88 51	IN	SNS_ODD_P	FUNC_TEST=TRUE
88 51	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

52	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
52	IN	FAN_TACH0_L	FUNC_TEST=TRUE
89 52	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
52	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

53	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH2_L	FUNC_TEST=TRUE
89 53	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
53	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

52	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
52	IN	FAN_TACH1_L	FUNC_TEST=TRUE
89 52	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
52	IN	FAN_1_GND	FUNC_TEST=TRUE

J5550 HDD TEMP SENSOR

88 51	IN	HDD_OOB_TEMP_FILT	FUNC_TEST=TRUE

J5560 SKIN TEMP SENSOR

88 51	IN	SNS_SKIN_P	FUNC_TEST=TRUE
88 51	IN	SNS_SKIN_N	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

59	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
59	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
59	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

85 59 58	IN	AUD_SPKR_OUTLO2R_POUT	FUNC_TEST=TRUE
85 59 58	IN	AUD_SPKR_OUTLO2R_NOUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1R_POUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1R_NOUT	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

85 59 58	IN	AUD_SPKR_OUTLO2L_POUT	FUNC_TEST=TRUE
85 59 58	IN	AUD_SPKR_OUTLO2L_NOUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1L_POUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1L_NOUT	FUNC_TEST=TRUE

		GND	16 TP'S MIN_ALLOWED_TPS=16
89 6	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
69 6	IN	PP5V_S3_REG	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
89 6	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

PAGE TITLE: K22/K23 ICT/FCT

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DRAWING NUMBER: 051-8233 SIZE: D
REVISION: G.0.0
BRANCH:
PAGE: 110 OF 110
SHEET: 92 OF 92