

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
8	0003549590	ENGINEERING RELEASED		2014-12-19

X304 MLB SCHEMATIC - DVT

Fri Dec 19 12:14:48 2014

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59	76	1.05V Power Supply	AHARTMAN_052	10/29/2013
60	77	LCD & KBD Backlight Driver	SHART_044	11/20/2012
61	78	Misc Power Supplies	AHARTMAN_052	11/06/2013
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65	83	eDP Display Connector	GR00_052	05/04/2014
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-1573	1	SCHEM,MLB,X304	SCH	CRITICAL	
820-4924	1	PCBF,MLB,X304	PCB	CRITICAL	

DRAWING TITLE		SCHEM,MLB,X304	
Apple Inc.	DRAWING NUMBER	051-1573	SIZE D
	REVISION	8.0.0	
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BOM Groups

BOM GROUP	BOM OPTIONS
X304_COMMON	ALTERNATE, COMMON, X304_COMMON1, X304_COMMON2, X304_COMMON3, X304_COMMON4, X304_PROGPARTS
X304_COMMON1	TBTHV:P15V, SKIP_5V3V3:AUDIBLE, PANEL:NEW, SSD_CLKREQ:BI
X304_COMMON2	EDP, EDP_LS_CAP, CAMERA_3V3:S0, CAM_WAKE:NO, CAM_XTAL:NO, VCORE_FETS
X304_COMMON3	XDP, SAMCONN, BKLT:PROD, CPUTHRM:ALRT, LOADRC:NO, OTHERRC:NO, DDRRC:NO, TBTRC:NO, BMONRC:NO, TPADRC:NO
X304_PROGPARTS	SMC_PROG:PROTO0, BOOTROM_PROG, TBTRM_PROG
X304_DEVEL:ENG	ALTERNATE, ENGISNS, XDP_CONN,DBGLED
X304_DEVEL:DVT	ALTERNATE, ENGISNS, XDP_CONN, S0PGOOD_ISL
X304_DEVEL:PVT	ALTERNATE
ENGISNS	LOADISNS, OTHERISNS, DDRISNS, TBTISNS, BMONISNS, TPADISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00107	1	CPU, BW, SR26K, PRQ, F0-B2, 2.7, 28W, 1.05, 1168	U0500	CRITICAL	CPU_BDW23:2.7G
337S00108	1	CPU, BW, SR26H, PRQ, F0-B2, 2.9, 28W, 1.1, 1168	U0500	CRITICAL	CPU_BDW23:2.9G
337S00109	1	CPU, BW, SR26E, PRQ, F0-B2, 3.1, 28W, 1.1, 1168	U0500	CRITICAL	CPU_BDW23:3.1G

DVT

998-7866	1	INTERPOSER, BGA1168P, SINGLE SIDE	U0500	CRITICAL	CPU_SOCKET
338S1247	1	IC, TBT, FR-4C, A0, PRQ, CIO, SR1JC, PCBGA288	U2800	CRITICAL	
338S1264	1	IC, BCM15700A2KFE4G, S2 CMRA, 8X8, 208FCBGA	U3900	CRITICAL	
376S1194	2	MOSFET, N-CH, 30V, 15.3A, 12M, 8P, 3.3X3.3 DFN	Q7310, Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET, N-CH, 30V, 22A, 6.0M, 8P, 3.3X3.3 DFN	Q7311, Q7321	CRITICAL	VCORE_FET:VSHY
376S00036	2	MOSFET, N-CH, 30V, 52A, 5.9MO, 3.3X3.3 DFN8	Q7310, Q7320	CRITICAL	VCORE_FET:ONSMI
376S00037	2	MOSFET, N-CH, 30V, 64A, 3.5MO, 3.3X3.3 DFN8	Q7311, Q7321	CRITICAL	VCORE_FET:ONSMI

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00192	1	T29, EPROM, FALCON RIDGE (V27.1) EVT2, X304	U2890	CRITICAL	TBTROM_PROG

SMC

341S3982	1	IC, SMC-B1, EXT (V2.21A5) PROTO 0, X304	U5000	CRITICAL	SMC_PROG:PROTO0
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EFI ROM

341S00235	1	EFI ROM, MLB (V0145) DVT, X304	U6100	CRITICAL	BOOTROM_PROG
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Variable BOM Groups

BOM GROUP	BOM OPTIONS
X304_COMMON4	SMCBOARDID:16

Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-1314	1	X304 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-1319	1	X304 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-1318	1	VCORE FET, VSHY, X304	VCOREFETS	CRITICAL	VCORE_FETS

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_16G_HYNIX_1600	16G_HYNIX_1600, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L
RAM_16G_HYNIX_1866	16G_HYNIX_1866, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:L
RAM_8G_HYNIX_1600	8G_HYNIX_1600, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H
RAM_8G_HYNIX_1866	8G_HYNIX_1866, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:H
RAM_4G_HYNIX_1600	4G_HYNIX_1600, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L
RAM_4G_HYNIX_1866	4G_HYNIX_1866, RAMCFG3:L, RAMCFG2:H, RAMCFG1:L, RAMCFG0:L
RAM_16G_ELPIDA_1600	16G_ELPIDA_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L
RAM_16G_ELPIDA_1866	16G_ELPIDA_1866, RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:L
RAM_8G_ELPIDA_1600	8G_ELPIDA_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H
RAM_8G_ELPIDA_1866	8G_ELPIDA_1866, RAMCFG3:H, RAMCFG2:H, RAMCFG1:L, RAMCFG0:H
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L
RAM_4G_ELPIDA_1866	4G_ELPIDA_1866, RAMCFG3:H, RAMCFG2:H, RAMCFG1:L, RAMCFG0:L
RAM_8G_SAMSUNG_1600	8G_SAMSUNG_1600, RAMCFG3:H, RAMCFG2:L, RAMCFG1:H, RAMCFG0:H
RAM_8G_SAMSUNG_1866	8G_SAMSUNG_1866, RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:H
RAM_4G_SAMSUNG_1866	4G_SAMSUNG_1866, RAMCFG3:L, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00068	08	CPU
337S00069	08	CPU
337S00070	08	CPU
337S00071	08	CPU
353S00200	07	TPAD ELRC FUSE
333S0786	07	SYS MEMORY HYNIX
333S0784	07	SYS MEMORY HYNIX
333S0792	07	SYS MEMORY MICRON
333S0790	07	SYS MEMORY MICRON
333S00004	07	SYS MEMORY SAMSUNG
311S0597	02	KEYBOARD I2C EXPANDER
359S0197	01	GREEN CLOCK
338S1247	01	FALCON RIDGE
353S3931	01	TBT PWR MUX
353S3812	01	TBT MIX
353S3814	01	TBT MIX
353S00095	01	DDC CROSSBAR
353S3328	01	DDC CROSSBAR
343S0511	01	PCIE DELAY IC
338S1264	01	S2
333S0700	01	S2 MEMORY
333S0704	01	S2 MEMORY
353S3054	01	USB POWER/SAFETY
343S0649	01	SMC RESET CHIP
353S4080	01	AUDIO
353S2888	01	AUDIO AMPS
353S2958	01	AUDIO AMPS
353S2929	01	BAT CHARGER
353S00036	01	VR12.6 CONTROLLER
353S4160	01	BEN
343S0666	01	SAK, HDMI SELECT
341S3982	01	SMC
341S00192	01	T29 ROM
341S00235	01	EFI ROM

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0783	4	IC, SDRAM, 25nm 32Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	16G_HYNIX_1600
333S0784	4	IC, SDRAM, 25nm 32Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	16G_HYNIX_1866
333S0785	4	IC, SDRAM, 29nm 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	8G_HYNIX_1600
333S0786	4	IC, SDRAM, 29nm 16Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	8G_HYNIX_1866
333S0787	4	IC, SDRAM, 29nm 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	4G_HYNIX_1600
333S0788	4	IC, SDRAM, 29nm 8Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	4G_HYNIX_1866
333S0789	4	IC, SDRAM, 25nm 32Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	16G_SAMSUNG_1600
333S0790	4	IC, SDRAM, 25nm 32Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	16G_SAMSUNG_1866
333S0791	4	IC, SDRAM, 25nm 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	8G_SAMSUNG_1600
333S0792	4	IC, SDRAM, 25nm 16Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	8G_SAMSUNG_1866
333S0793	4	IC, SDRAM, 25nm 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	4G_SAMSUNG_1600
333S0794	4	IC, SDRAM, 25nm 8Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	4G_SAMSUNG_1866
333S00003	4	IC, SDRAM, 23nm 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	8G_SAMSUNG_1600
333S00004	4	IC, SDRAM, 23nm 16Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	8G_SAMSUNG_1866
333S00001	4	IC, SDRAM, 23nm 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	4G_SAMSUNG_1600
333S00002	4	IC, SDRAM, 23nm 8Gb, LPDDR3-1866, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	4G_SAMSUNG_1866

S2 DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	IC, SDRAM, 4GBIT, DDR3L-1600, HUMA, 96B BGA	U4000		

SYMC MASTER-SHEET_046 SYMC_DATE:11/27/2015

Apple Inc.

BOM Configuration

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-1314	COMMON,MLB,X304	X304_COMMON
985-1319	DEV,MLB,X304	X304_DEVEL:ENG
639-00772	MLB,BDW2+3,2.7GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_HYNIX_1866
639-00773	MLB,BDW2+3,2.7GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_16G_HYNIX_1866
639-00774	MLB,BDW2+3,2.7GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_ELPIDA_1866
639-00775	MLB,BDW2+3,2.7GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_16G_ELPIDA_1866
639-00776	MLB,BDW2+3,2.7GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.7G,RAM_8G_SAMSUNG_1866
639-00777	MLB,BDW2+3,2.9GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_HYNIX_1866
639-00778	MLB,BDW2+3,2.9GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_16G_HYNIX_1866
639-00779	MLB,BDW2+3,2.9GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_ELPIDA_1866
639-00780	MLB,BDW2+3,2.9GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_16G_ELPIDA_1866
639-00781	MLB,BDW2+3,2.9GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:2.9G,RAM_8G_SAMSUNG_1866
639-00782	MLB,BDW2+3,3.1GHz,8GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_HYNIX_1866
639-00783	MLB,BDW2+3,3.1GHz,16GB-HY-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_16G_HYNIX_1866
639-00784	MLB,BDW2+3,3.1GHz,8GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_ELPIDA_1866
639-00785	MLB,BDW2+3,3.1GHz,16GB-EP-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_16G_ELPIDA_1866
639-00786	MLB,BDW2+3,3.1GHz,8GB-SM-1866,X304	BASE_BOM,DEVEL_BOM,CPU_BDW23:3.1G,RAM_8G_SAMSUNG_1866

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00035	PCBA,MLB,NO CPU,X304	BASE_BOM,DEVEL_BOM,RAM_8G_HYNIX_1866
639-00036	PCBA,MLB,CPU SOCKET,X304	BASE_BOM,DEVEL_BOM,CPU_SOCKET,RAM_8G_HYNIX_1866
685-1318	VCORE FET,VSHY,X304	VCORE_FET:VSHY
685-00022	VCORE FET,ONSMI,X304	VCORE_FET:ONSMI

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00022	685-1318		ALL	
333S0704	333S0700		ALL	

Onsemi alt to Vishay for CPU Core Mosfets
Elpida alt to Hynix for S2 Camera DDR3 Memory

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	
128S0311	128S0329		ALL	
138S0739	138S0706		ALL	
197S0481	197S0480		ALL	
152S0461	152S1645		ALL	
376S1080	376S0820		ALL	

Diodes alt to Fairchild
NEC alt to Sanyo
Samsung alt to Murata
Epson alt to NDK
Cyttec alt to Vishay
Diodes alt to On Semi

138S0725	138S0724		ALL	
376S00074	376S0855		ALL	
376S1129	376S0855		ALL	
376S1089	376S1128		ALL	
353S3452	353S1286		ALL	

Samsung alt to Murata
Toshiba alt for Diodes Dual
NXP Alt for Diodes Dual
NXP Alt for Diodes Single
Maxim alt to Microchip

128S0364	128S0264		ALL	
107S0254	107S0241		ALL	
138S0843	138S0674		ALL	

Sanyo 2nd Factory alt
Cyttec alt to TFT
Samsung alt to Murata (BKLT)

138S0846	138S0811		ALL	
197S0542	197S0544		ALL	
197S0545	197S0544		ALL	

Samsung alt to Murata (BKLT)
NDK alt to TXC
Epson alt to TXC

107S0248	107S0250		ALL	
127S0164	127S0162		ALL	
353S4070	353S4069		ALL	
353S4068	353S4069		ALL	
353S3814	353S3812		ALL	
311S0649	311S0541		ALL	
138S0614	138S0578		ALL	
155S0694	155S0387		ALL	
155S0660	155S0513		ALL	

TFT alt to Cyttec
Rohm alt to Vishay
Pericom alt to TI DP Mux U9750
NXP alt to TI DP Mux U9750
TI alt to NXP
ONsemi alt to Toshiba
Murata, TDK, Samsung, Taiyo Yuden alt to Murata, TDK
Murata alt to TDK
Murata alt to TDK

740S00003	740S0135		ALL	
138S0738	138S1101		ALL	
353S00095	353S3328		ALL	
311S00007	311S0426		ALL	
128S0398	128S0220		ALL	
128S0386	128S0284		ALL	
128S0397	128S0325		ALL	
377S00011	377S0184		ALL	
377S0155	377S0184		ALL	
155S0914	155S0897		ALL	
371S0558	371S0713		ALL	
128S0436	128S0392		ALL	
128S0445	128S0392		ALL	
353S00034	353S2220		ALL	
311S00014	311S0515		ALL	
311S00008	311S0271		ALL	
197S0479	197S0478		ALL	
311S00013	311S0508		ALL	
376S00014	376S0761		ALL	
371S00019	371S0463		ALL	
371S00018	371S0619		ALL	
311S00015	311S0450		ALL	
371S00017	371S0749		ALL	

AEM alt to Tyco
Samsung alt to Murata for LCD BKL caps
Pericom alt to TI
Diodes alt to NXP
Kemet alt to Sanyo
Kemet alt to Sanyo
Kemet alt to Sanyo
Infineon alt to Infineon
On Semi alt to Infineon
Panasonic alt to TDK
ST Micro alt to Diodes
Kemet alt to Sanyo
Panasonic alt to Sanyo
Pericom alt to Fairchild
Diodes alt to NXP
Diodes alt to NXP
Epson alt to NDK
Diodes alt to NXP
Toshiba alt to Vishay
Rohm alt to Rohm
Rohm alt to Rohm
Diodes alt to NXP
Diodes alt to Onsemi

353S00107	353S3239	ANY	ALL	
107S00024	107S0226		ALL	
372S0186	372S0185		ALL	
353S00231	353S3987		ALL	
353S00135	353S2220		ALL	
353S00133	353S2741		ALL	
131S00040	131S00041		ALL	
107S00015	107S00011		ALL	
107S00031	107S00032		ALL	
107S00029	107S00030		ALL	

Onsemi alt to Intersil
Yageo alt to Cyttec
NXP alt to Diodes
NXP alt to TI
Onsemi alt to Fairchild
Onsemi alt to TI
Murata alt to Taiyo Yuden
TFT alt to Cyttec
TFT alt to Cyttec
TFT alt to Cyttec

SYNC_MASTER=T14 SYNC_DATE=09/04/2012

BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

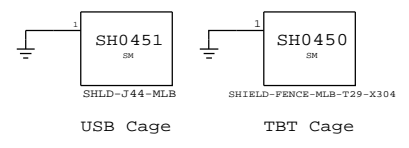
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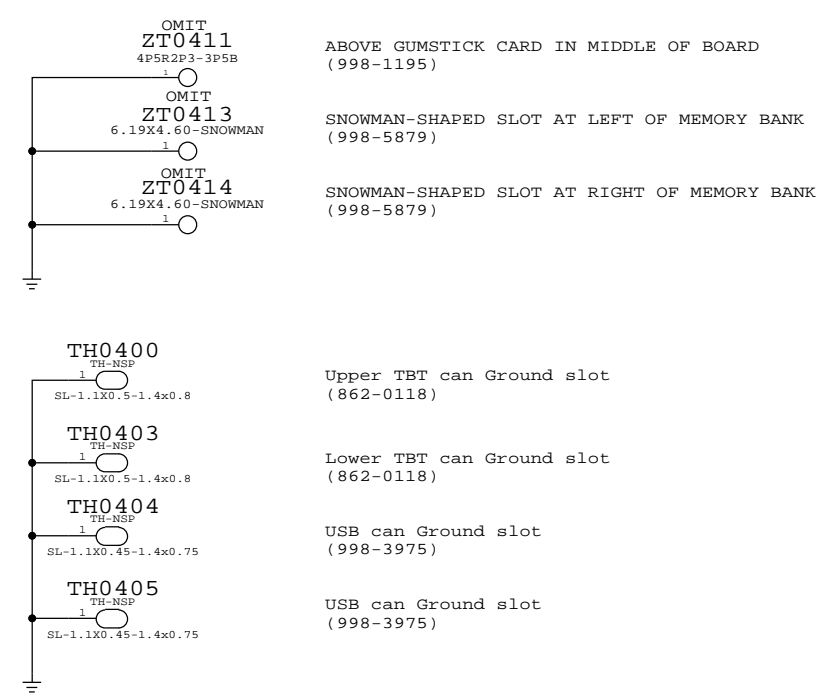
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Shield Cans



Mounting Holes & Slots



ABOVE GUMSTICK CARD IN MIDDLE OF BOARD
(998-1195)

SNOWMAN-SHAPED SLOT AT LEFT OF MEMORY BANK
(998-5879)

SNOWMAN-SHAPED SLOT AT RIGHT OF MEMORY BANK
(998-5879)

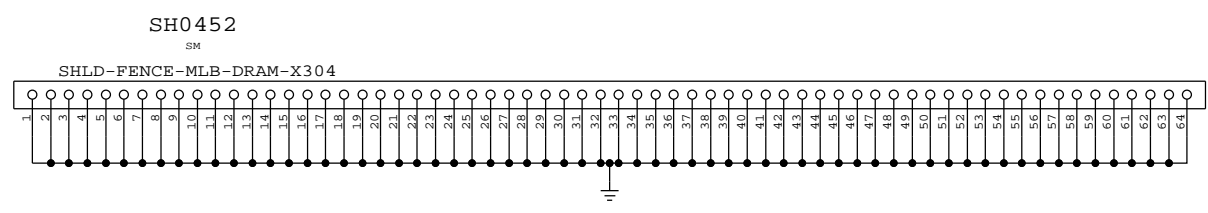
Upper TBT can Ground slot
(862-0118)

Lower TBT can Ground slot
(862-0118)

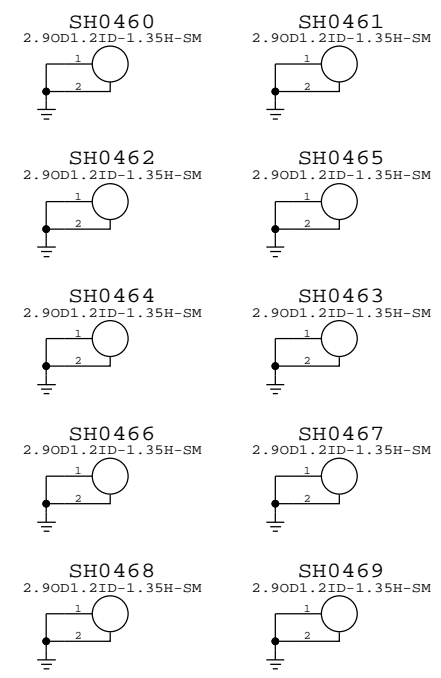
USB can Ground slot
(998-3975)

USB can Ground slot
(998-3975)

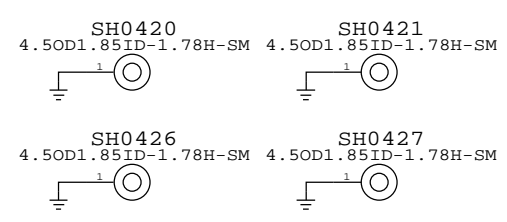
Memory Shield CAN (806-00037)



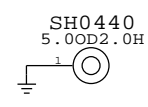
Rubber Mount Standoffs (860-1448)



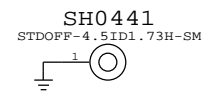
THERMAL MODULE STANDOFF (860-00165)



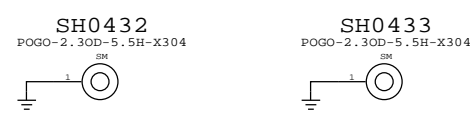
SSD STANDOFF (860-00164)



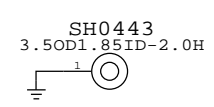
FAN STANDOFF (860-00183)



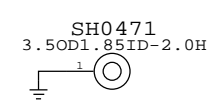
POGO PINS (870-00607)
SH0435 & SH0436 removed.



RIO FLEX BRACKET BOSSES (860-00166)



IPD FLEX BRACKET BOSSES (860-00166)



SYNC MASTER=LJUNN J44		SYNC DATE=01/13/2013	
PAGE TITLE			
PD Parts		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
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		4 OF 82	

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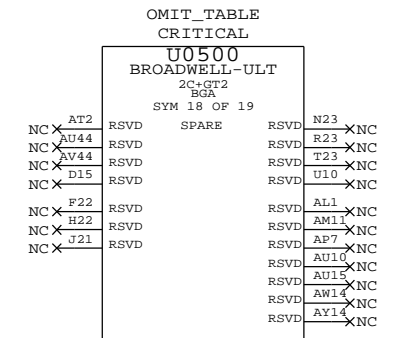
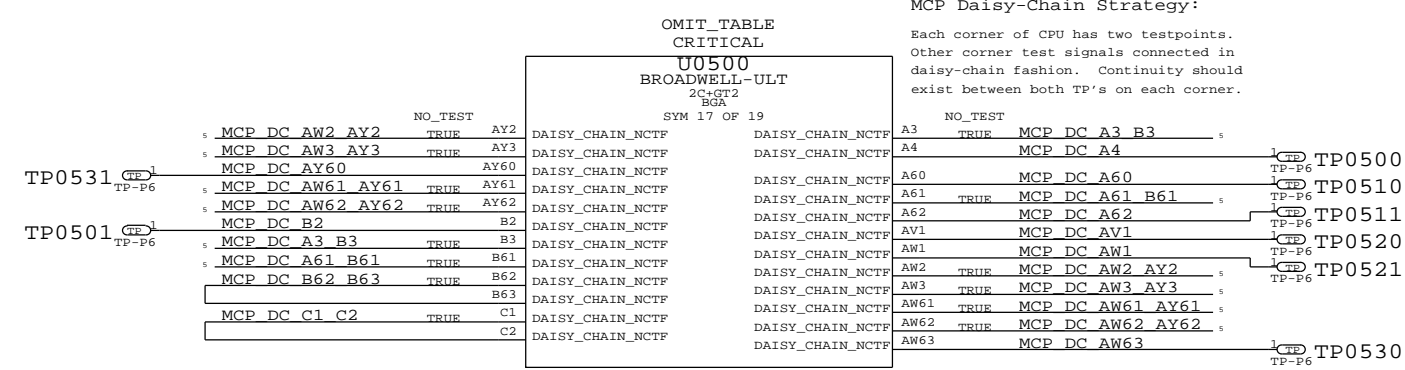
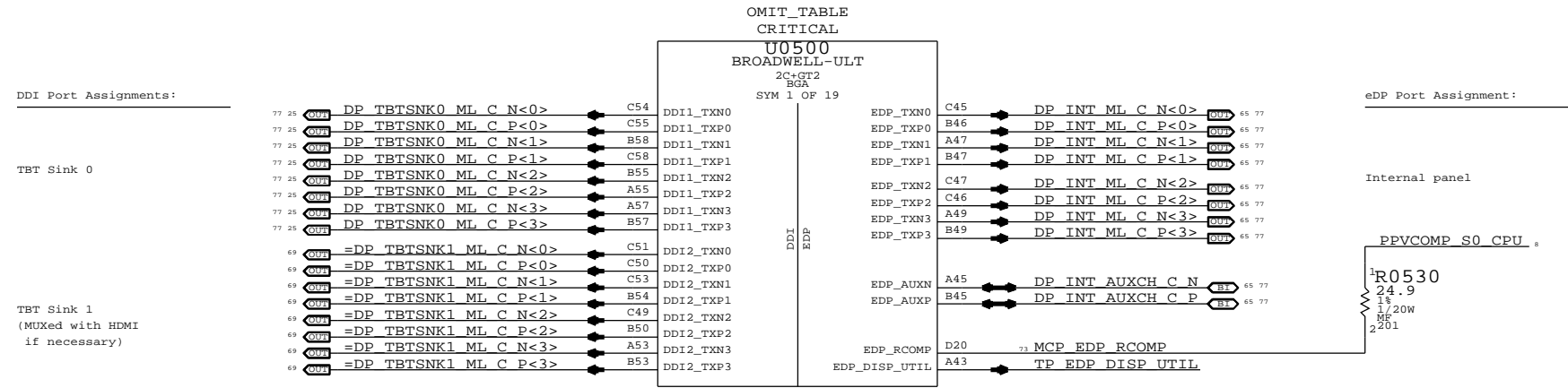
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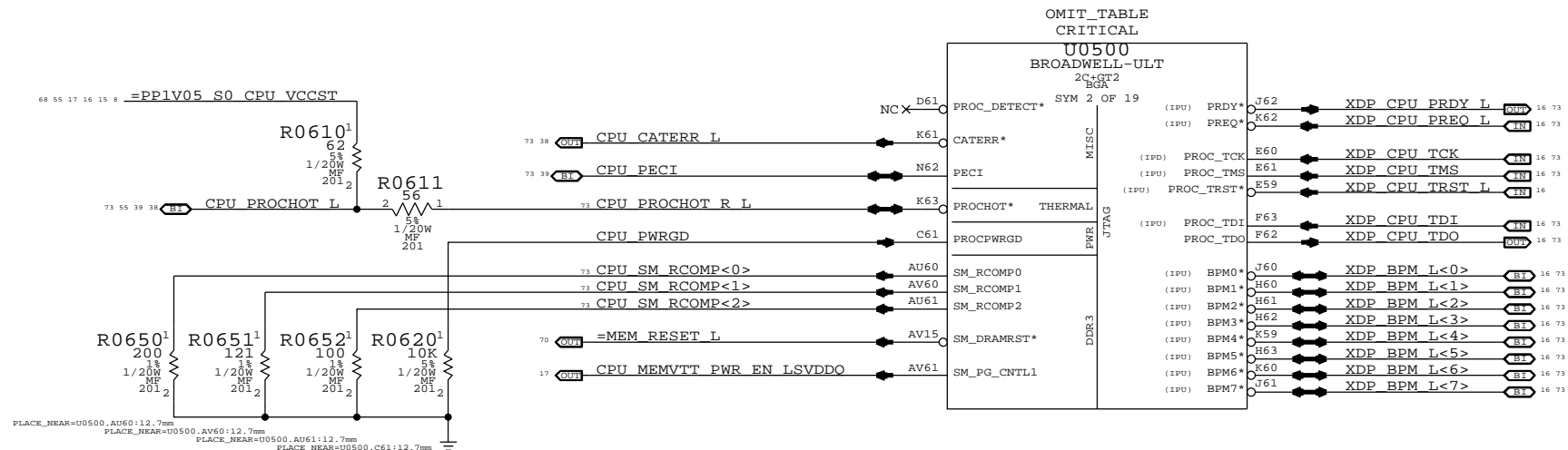
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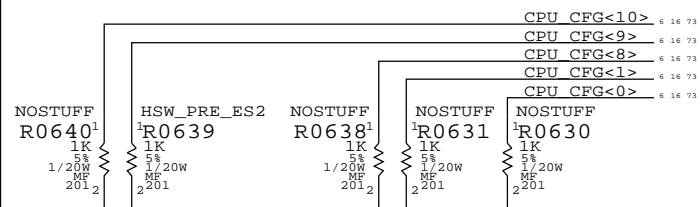


SYNC MASTER=141		SYNC DATE=10/23/2012	
PAGE TITLE			
CPU GFX, NCTF, RSVD			
Apple Inc.		DRAWING NUMBER	SIZE
		051-1573	D
		REVISION	
		8.0.0	
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		PAGE	5 OF 120
		SHEET	5 OF 82

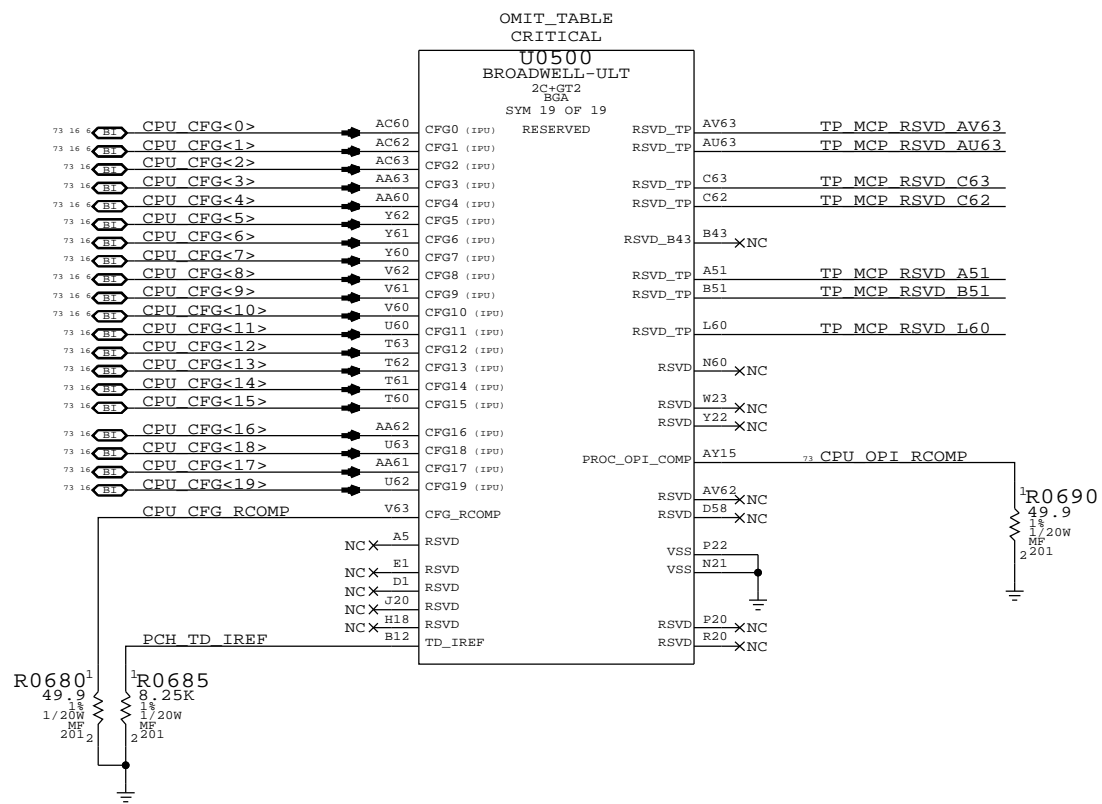
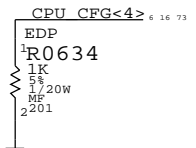


CFG<10>:SAFE MODE BOOT 1 = NORMAL OPERATION 0 = POWER FEATURES NOT ACTIVE
 CFG<9>:NO SVID-CAPABLE VR 1 = VR SUPPORTS SVID 0 = VR DOES NOT SUPPORT SVID
 CFG<8>:ALLOW NOA ON LOCKED UNITS 1 = NORMAL OPERATION 0 = NOA ALWAYS UNLOCKED
 CFG<4>:EDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
 CFG<1>:PCH-LESS MODE 1 = NORMAL OPERATION 0 = PCH-LESS MODE
 CFG<0>:RESET SEQUENCE STALL 1 = NORMAL OPERATION 0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800 and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC MASTER=J41 SYNC DATE=10/23/2012

CPU Misc, JTAG, CFG, RSVD

Apple Inc.

DRAWING NUMBER 051-1573 SIZE D

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OMIT_TABLE CRITICAL

U0500 BROADWELL-ULT 2C+GT2 3GA SYM 3 OF 19

76 71 70	MEM A DO<0>	AH63	SA_DQ0	AU37	MEM A CLK N<0>	70 76
76 71 70	MEM A DO<1>	AH62	SA_DQ1	AV37	MEM A CLK P<0>	70 76
76 71 70	MEM A DO<2>	AK63	SA_DQ2	AW36	MEM A CLK N<1>	21 24 76
76 71 70	MEM A DO<3>	AK62	SA_DQ3	AY36	MEM A CLK P<1>	21 24 76
76 71 70	MEM A DO<4>	AH61	SA_DQ4	AU43	MEM A CKE<0>	70 76
76 71 70	MEM A DO<5>	AH60	SA_DQ5	AM43	MEM A CKE<1>	20 24 76
76 71 70	MEM A DO<6>	AK61	SA_DQ6	AY42	MEM A CKE<2>	20 24 76
76 71 70	MEM A DO<7>	AK60	SA_DQ7	AY43	MEM A CKE<3>	21 24 76
76 71 70	MEM A DO<8>	AM63	SA_DQ8	AP33	MEM A CS L<0>	20 21 24 76
76 71 70	MEM A DO<9>	AM62	SA_DQ9	AR32	MEM A CS L<1>	20 21 24 76
76 71 70	MEM A DO<10>	AP63	SA_DQ10	AP32	=MEM A ODT<0>	70
76 71 70	MEM A DO<11>	AP62	SA_DQ11	AY34	=MEM A RAS L	70
76 71 70	MEM A DO<12>	AM61	SA_DQ12	AW34	=MEM A WE L	70
76 71 70	MEM A DO<13>	AM60	SA_DQ13	AU34	=MEM A CAS L	70
76 71 70	MEM A DO<14>	AP61	SA_DQ14	AU35	=MEM A BA<0>	70
76 71 70	MEM A DO<15>	AP60	SA_DQ15	AV35	=MEM A BA<1>	70
76 71 70	MEM A DO<16>	AP58	SA_DQ16	AY41	=MEM A BA<2>	70
76 71 70	MEM A DO<17>	AR58	SA_DQ17	AU36	=MEM A A<0>	70
76 71 70	MEM A DO<18>	AM57	SA_DQ18	AY37	=MEM A A<1>	70
76 71 70	MEM A DO<19>	AK57	SA_DQ19	AR38	=MEM A A<2>	70
76 71 70	MEM A DO<20>	AL58	SA_DQ20	AP36	=MEM A A<3>	70
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76 71 70	MEM A DO<22>	AR57	SA_DQ22	AR36	=MEM A A<5>	70
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76 71 70	MEM A DO<48>	AK40	SA_DQ48	AL49	MEM A DOS P<7>	70 76
76 71 70	MEM A DO<49>	AK42	SA_DQ49	AP49	CPU DIMM VREFCA	19 76
76 71 70	MEM A DO<50>	AM43	SA_DQ50	AR51	CPU DIMMA VREFDO	19 76
76 71 70	MEM A DO<51>	AM45	SA_DQ51	AP51	CPU DIMMB VREFDO	19 76
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76 71 70	MEM A DO<53>	AK43	SA_DQ53			
76 71 70	MEM A DO<54>	AM40	SA_DQ54			
76 71 70	MEM A DO<55>	AM42	SA_DQ55			
76 71 70	MEM A DO<56>	AM46	SA_DQ56			
76 71 70	MEM A DO<57>	AK46	SA_DQ57			
76 71 70	MEM A DO<58>	AK49	SA_DQ58			
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76 71 70	MEM A DO<61>	AK48	SA_DQ61			
76 71 70	MEM A DO<62>	AM51	SA_DQ62			
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OMIT_TABLE CRITICAL

U0500 BROADWELL-ULT 2C+GT2 3GA SYM 4 OF 19

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76 71 70	MEM B DO<4>	AV31	SB_DQ4	AY49	MEM B CKE<0>	22 24 76
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76 71 70	MEM B DO<8>	AY27	SB_DQ8	AM32	MEM B CS L<0>	22 23 24 76
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76 71 70	MEM B DO<61>	AM20	SB_DQ61			
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SYNC MASTER=141 SYNC DATE=10/23/2012

CPU LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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SHEET: 7 OF 82

BDW-ULT current estimates from Broadwell Mobile ULT Processor EDS vol.1 Doc# 514405, Rev.: 0.9v1
 Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9
 Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

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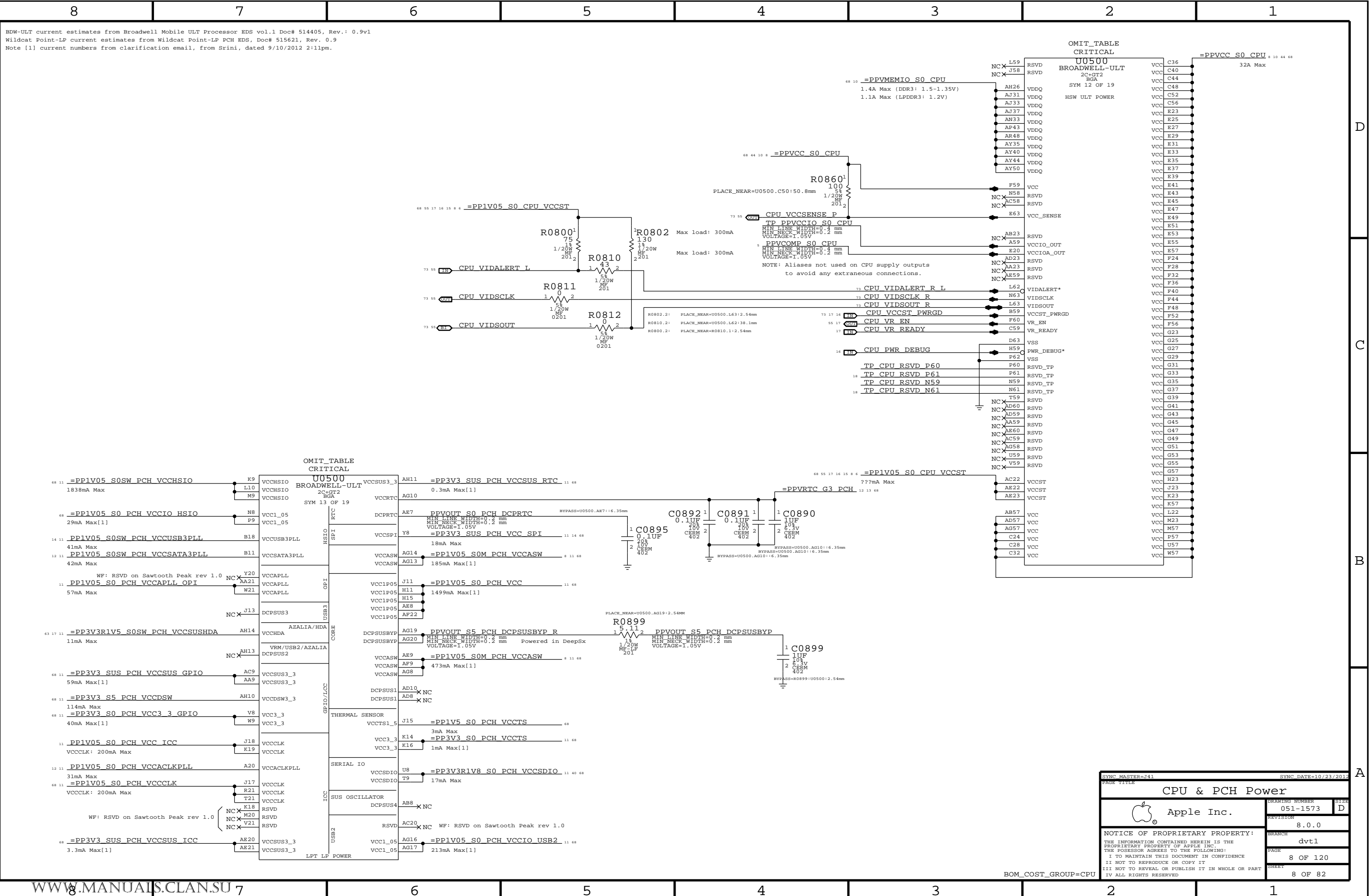
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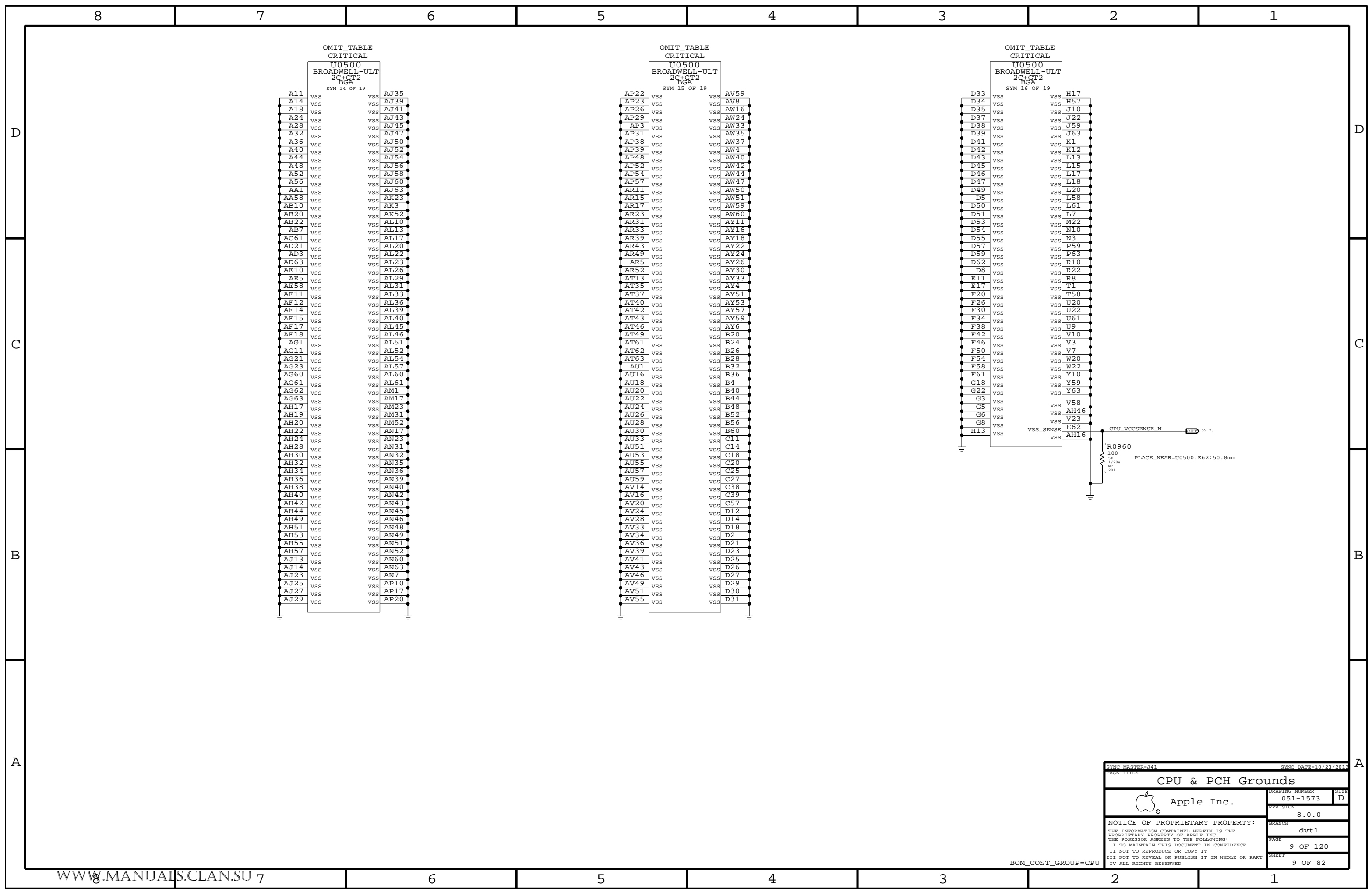
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	2C+GT2 BGA	VCC	C40
	SYM 12 OF 19	VCC	C44
	HSW ULT POWER	VCC	C48
		VCC	C52
		VCC	C56
		VCC	E23
		VCC	E25
		VCC	E27
		VCC	E29
		VCC	E31
		VCC	E33
		VCC	E35
		VCC	E37
		VCC	E39
		VCC	E41
		VCC	E43
		VCC	E45
		VCC	E47
		VCC	E49
		VCC	E51
		VCC	E53
		VCC	E55
		VCC	E57
		VCC	F24
		VCC	F28
		VCC	F32
		VCC	F36
		VCC	F40
		VCC	F44
		VCC	F48
		VCC	F52
		VCC	F56
		VCC	G23
		VCC	G25
		VCC	G27
		VCC	G29
		VCC	G31
		VCC	G33
		VCC	G35
		VCC	G37
		VCC	G39
		VCC	G41
		VCC	G43
		VCC	G45
		VCC	G47
		VCC	G49
		VCC	G51
		VCC	G53
		VCC	G55
		VCC	G57
		VCC	H23
		VCC	J23
		VCC	K23
		VCC	K57
		VCC	L22
		VCC	M23
		VCC	M57
		VCC	P57
		VCC	U57
		VCC	W57

OMIT_TABLE CRITICAL		U0500 BROADWELL-ULT		VCCSUS3_3		=PP3V3 SUS_PCH_VCCSUS_RTC	
11	=PP1V05_S0_SW_PCH_VCCHSIO	VCCHSIO	L10	VCCSUS3_3	AG11	0.3mA Max[1]	11 68
68	=PP1V05_S0_PCH_VCCIO_HSIO	VCCHSIO	M9	VCCRTC	AG10		
14	PP1V05_S0_SW_PCH_VCCUSB3PLL	VCCUSB3PLL	B18	VCCSPI	AE7	PPVOUT_S0_PCH_DCPRTC	11 14 68
12	PP1V05_S0_SW_PCH_VCCSATA3PLL	VCCSATA3PLL	B11	VCCASW	Y8	PP3V3 SUS_PCH_VCC_SPI	11 14 68
11	PP1V05_S0_PCH_VCCAPLL_OPI	VCCAPLL	Y20	VCCASW	AG14	PP1V05_S0M_PCH_VCCASW	8 11 68
63	PP3V3R1V5_S0_SW_PCH_VCCSUSHDA	VCCCHDA	AH14	VCCASW	AG13		
68	PP3V3 SUS_PCH_VCCSUS_GPIO	VCCSUS3_3	AC9	VCCASW	J11	PP1V05_S0_PCH_VCC	11 68
68	PP3V3 S5_PCH_VCCDSW	VCCDSW3_3	AH10	VCCASW	H11	1499mA Max[1]	
68	PP3V3 S0_PCH_VCC3_3_GPIO	VCC3_3	V8	VCCASW	H15		
11	PP1V05_S0_PCH_VCC_ICC	VCCCLK	K19	VCCASW	H15		
12	PP1V05_S0_PCH_VCCACKPLL	VCCACKPLL	A20	VCCASW	AE8		
68	PP1V05_S0_PCH_VCCCLK	VCCCLK	J17	VCCASW	AF22		
68	PP3V3 SUS_PCH_VCCSUS_ICC	VCCSUS3_3	AE20	VCCASW	AG8	473mA Max[1]	

CPU & PCH Power		DRAWING NUMBER	051-1573	SIZE	D
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OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 14 OF 19

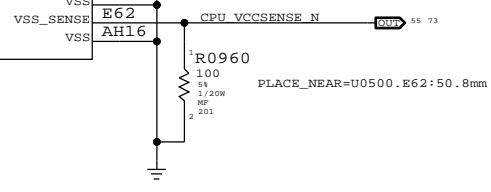
- | | | |
|------|-----|------|
| A11 | VSS | AJ35 |
| A14 | VSS | AJ39 |
| A18 | VSS | AJ41 |
| A24 | VSS | AJ43 |
| A28 | VSS | AJ45 |
| A32 | VSS | AJ47 |
| A36 | VSS | AJ50 |
| A40 | VSS | AJ52 |
| A44 | VSS | AJ54 |
| A48 | VSS | AJ56 |
| A52 | VSS | AJ58 |
| A56 | VSS | AJ60 |
| AA1 | VSS | AJ63 |
| AA58 | VSS | AK23 |
| AB10 | VSS | AK3 |
| AB20 | VSS | AK52 |
| AB22 | VSS | AL10 |
| AB7 | VSS | AL13 |
| AC61 | VSS | AL17 |
| AD21 | VSS | AL20 |
| AD3 | VSS | AL22 |
| AD63 | VSS | AL23 |
| AE10 | VSS | AL26 |
| AE5 | VSS | AL29 |
| AE58 | VSS | AL31 |
| AF11 | VSS | AL33 |
| AF12 | VSS | AL36 |
| AF14 | VSS | AL39 |
| AF15 | VSS | AL40 |
| AF17 | VSS | AL45 |
| AF18 | VSS | AL46 |
| AG1 | VSS | AL51 |
| AG11 | VSS | AL52 |
| AG21 | VSS | AL54 |
| AG23 | VSS | AL57 |
| AG60 | VSS | AL60 |
| AG61 | VSS | AL61 |
| AG62 | VSS | AM1 |
| AG63 | VSS | AM17 |
| AH17 | VSS | AM23 |
| AH19 | VSS | AM31 |
| AH20 | VSS | AM52 |
| AH22 | VSS | AN17 |
| AH24 | VSS | AN23 |
| AH28 | VSS | AN31 |
| AH30 | VSS | AN32 |
| AH32 | VSS | AN35 |
| AH34 | VSS | AN36 |
| AH36 | VSS | AN39 |
| AH38 | VSS | AN40 |
| AH40 | VSS | AN42 |
| AH42 | VSS | AN43 |
| AH44 | VSS | AN45 |
| AH49 | VSS | AN46 |
| AH51 | VSS | AN48 |
| AH53 | VSS | AN49 |
| AH55 | VSS | AN51 |
| AH57 | VSS | AN52 |
| AJ13 | VSS | AN60 |
| AJ14 | VSS | AN63 |
| AJ23 | VSS | AN7 |
| AJ25 | VSS | AP10 |
| AJ27 | VSS | AP17 |
| AJ29 | VSS | AP20 |

OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 15 OF 19

- | | | |
|------|-----|------|
| AP22 | VSS | AV59 |
| AP23 | VSS | AV8 |
| AP26 | VSS | AW16 |
| AP29 | VSS | AW24 |
| AP3 | VSS | AW33 |
| AP31 | VSS | AW35 |
| AP38 | VSS | AW37 |
| AP39 | VSS | AW4 |
| AP48 | VSS | AW40 |
| AP52 | VSS | AW42 |
| AP54 | VSS | AW44 |
| AP57 | VSS | AW47 |
| AR11 | VSS | AW50 |
| AR15 | VSS | AW51 |
| AR17 | VSS | AW59 |
| AR23 | VSS | AW60 |
| AR31 | VSS | AY11 |
| AR33 | VSS | AY16 |
| AR39 | VSS | AY18 |
| AR43 | VSS | AY22 |
| AR49 | VSS | AY24 |
| AR5 | VSS | AY26 |
| AR52 | VSS | AY30 |
| AT13 | VSS | AY33 |
| AT35 | VSS | AY4 |
| AT37 | VSS | AY51 |
| AT40 | VSS | AY53 |
| AT42 | VSS | AY57 |
| AT43 | VSS | AY59 |
| AT46 | VSS | AY6 |
| AT49 | VSS | B20 |
| AT61 | VSS | B24 |
| AT62 | VSS | B26 |
| AT63 | VSS | B28 |
| AU1 | VSS | B32 |
| AU16 | VSS | B36 |
| AU18 | VSS | B4 |
| AU20 | VSS | B40 |
| AU22 | VSS | B44 |
| AU24 | VSS | B48 |
| AU26 | VSS | B52 |
| AU28 | VSS | B56 |
| AU30 | VSS | B60 |
| AU33 | VSS | C11 |
| AU51 | VSS | C14 |
| AU53 | VSS | C18 |
| AU55 | VSS | C20 |
| AU57 | VSS | C25 |
| AU59 | VSS | C27 |
| AV14 | VSS | C38 |
| AV16 | VSS | C39 |
| AV20 | VSS | C57 |
| AV24 | VSS | D12 |
| AV28 | VSS | D14 |
| AV33 | VSS | D18 |
| AV34 | VSS | D2 |
| AV36 | VSS | D21 |
| AV39 | VSS | D23 |
| AV41 | VSS | D25 |
| AV43 | VSS | D26 |
| AV46 | VSS | D27 |
| AV49 | VSS | D29 |
| AV51 | VSS | D30 |
| AV55 | VSS | D31 |

OMIT_TABLE
CRITICAL
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 16 OF 19

- | | | |
|-----|-----|------|
| D33 | VSS | H17 |
| D34 | VSS | H57 |
| D35 | VSS | J10 |
| D37 | VSS | J22 |
| D38 | VSS | J59 |
| D39 | VSS | J63 |
| D41 | VSS | K1 |
| D42 | VSS | K12 |
| D43 | VSS | L13 |
| D45 | VSS | L15 |
| D46 | VSS | L17 |
| D47 | VSS | L18 |
| D49 | VSS | L20 |
| D5 | VSS | L58 |
| D50 | VSS | L61 |
| D51 | VSS | L7 |
| D53 | VSS | M22 |
| D54 | VSS | N10 |
| D55 | VSS | N3 |
| D57 | VSS | P59 |
| D59 | VSS | P63 |
| D62 | VSS | R10 |
| D8 | VSS | R22 |
| E11 | VSS | R8 |
| E17 | VSS | T1 |
| F20 | VSS | T58 |
| F26 | VSS | U20 |
| F30 | VSS | U22 |
| F34 | VSS | U61 |
| F38 | VSS | U9 |
| F42 | VSS | V10 |
| F46 | VSS | V3 |
| F50 | VSS | V7 |
| F54 | VSS | W20 |
| F58 | VSS | W22 |
| F61 | VSS | Y10 |
| G18 | VSS | Y59 |
| G22 | VSS | Y63 |
| G3 | VSS | V58 |
| G5 | VSS | AH46 |
| G6 | VSS | V23 |
| G8 | VSS | E62 |
| H13 | VSS | AH16 |



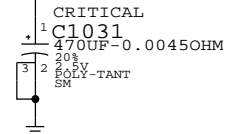
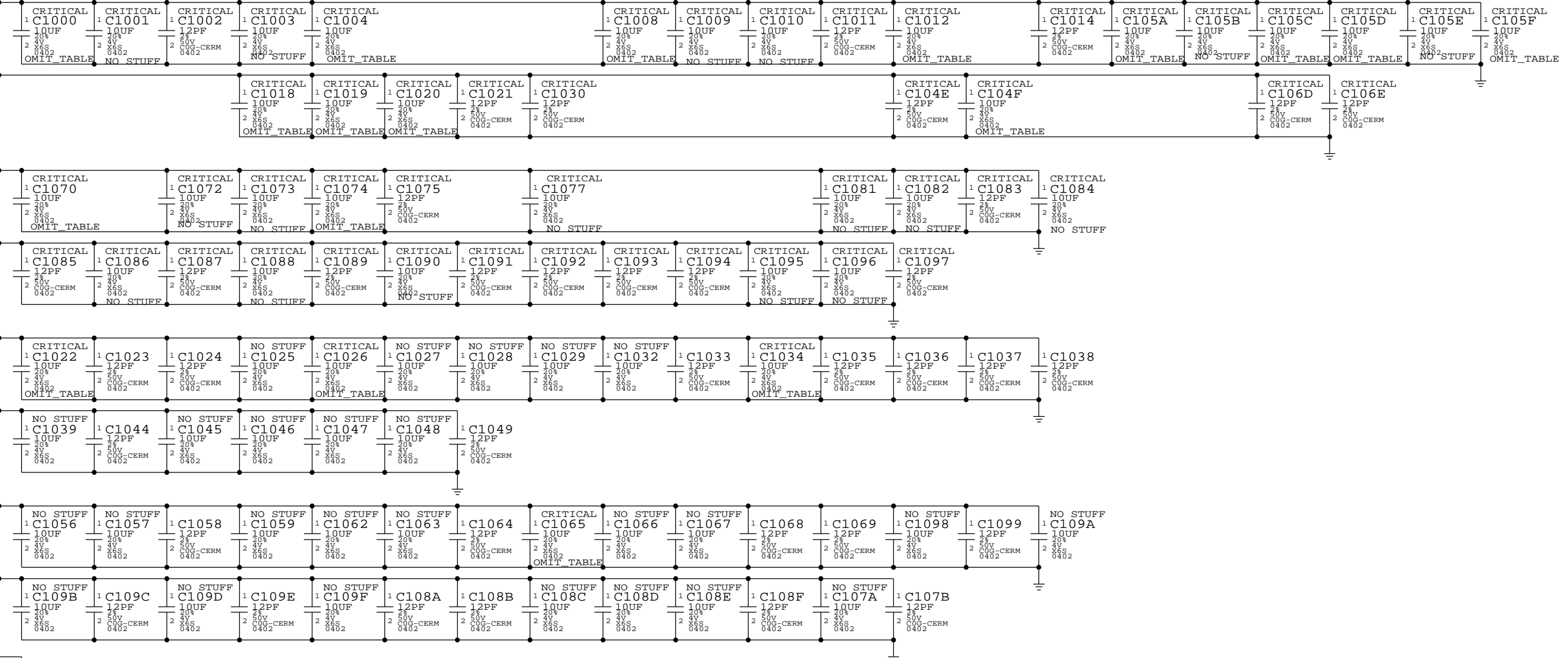
SYNC MASTER=J41		SYNC DATE=10/23/2012	
CPU & PCH Grounds			
Apple Inc.		DRAWING NUMBER	051-1573
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		PAGE	9 OF 120
		SHEET	9 OF 82

All Intel recommendations from Intel doc #603160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff

==PPVCC_S0_CPU



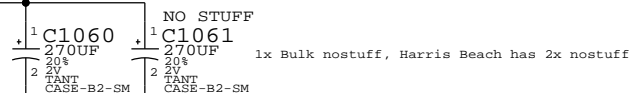
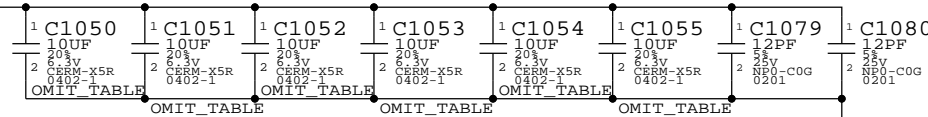
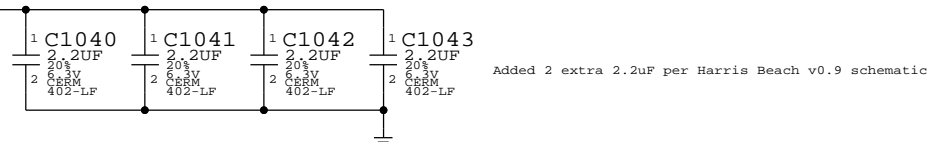
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0942	18	CAP,CER,10UF,20%,4V,X5S,HRZTL,0402		CRITICAL	

C1000,C1004,C1008,C1012,C1018,C1019,C1020,C1022,C1026,C1034,C1065,C1070,C1074,C105A,C105C,C105D,C104F,C105F

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

==PPVMEMIO_S0_CPU



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	6	CAP,CER,10UF,20%,6.3V,HRZTL,0402		CRITICAL	

C1050,C1051,C1052,C1053,C1054,C1055

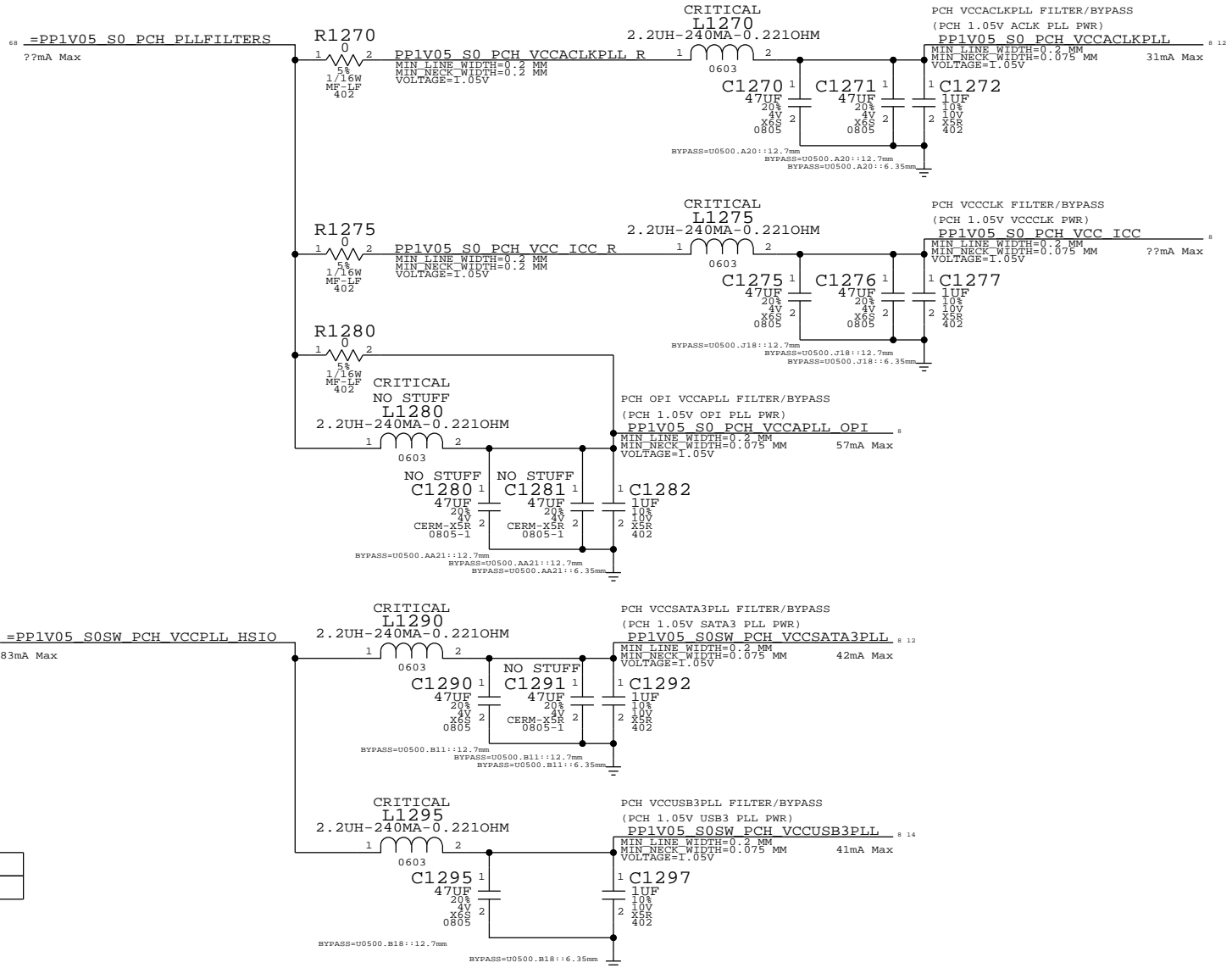
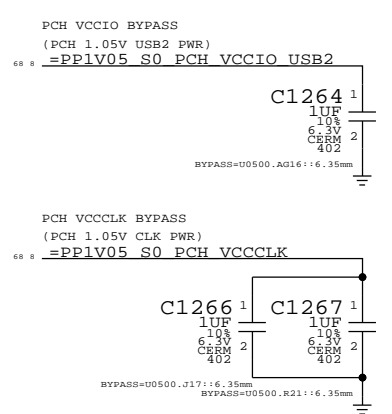
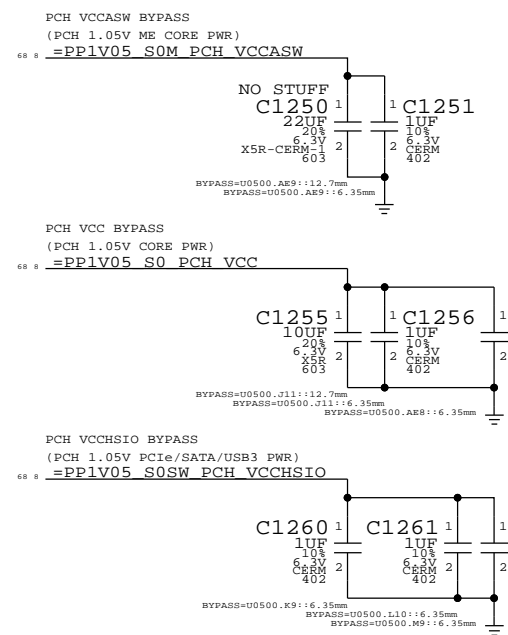
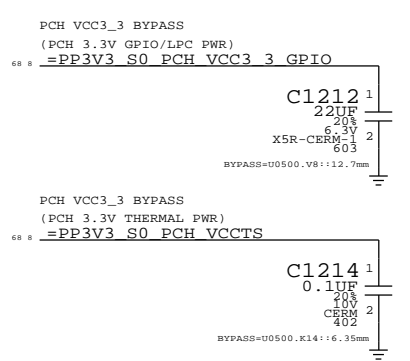
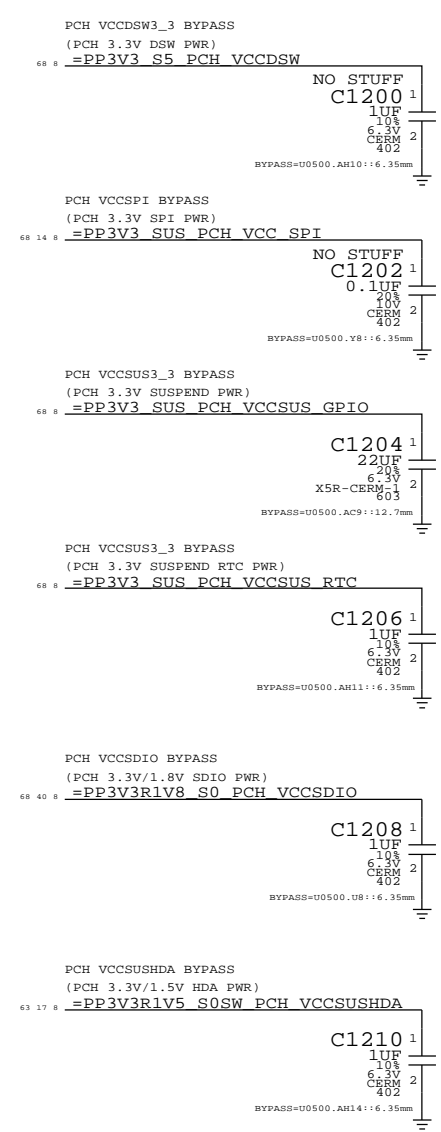
CPU VCC Decoupling

NOTE: 38X capacitors are STUFFED and have been changed to 12pF for Noise Floor Reasons (Radar # 17754026).

SYNC MASTER=141		SYNC DATE=10/23/2012	
PAGE TITLE: CPU Decoupling			
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C
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A

D
C
B
A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	1	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C1262	CRITICAL	

SYNC MASTER=J41 SYNC DATE=10/23/2012

PAGE TITLE: PCH Decoupling

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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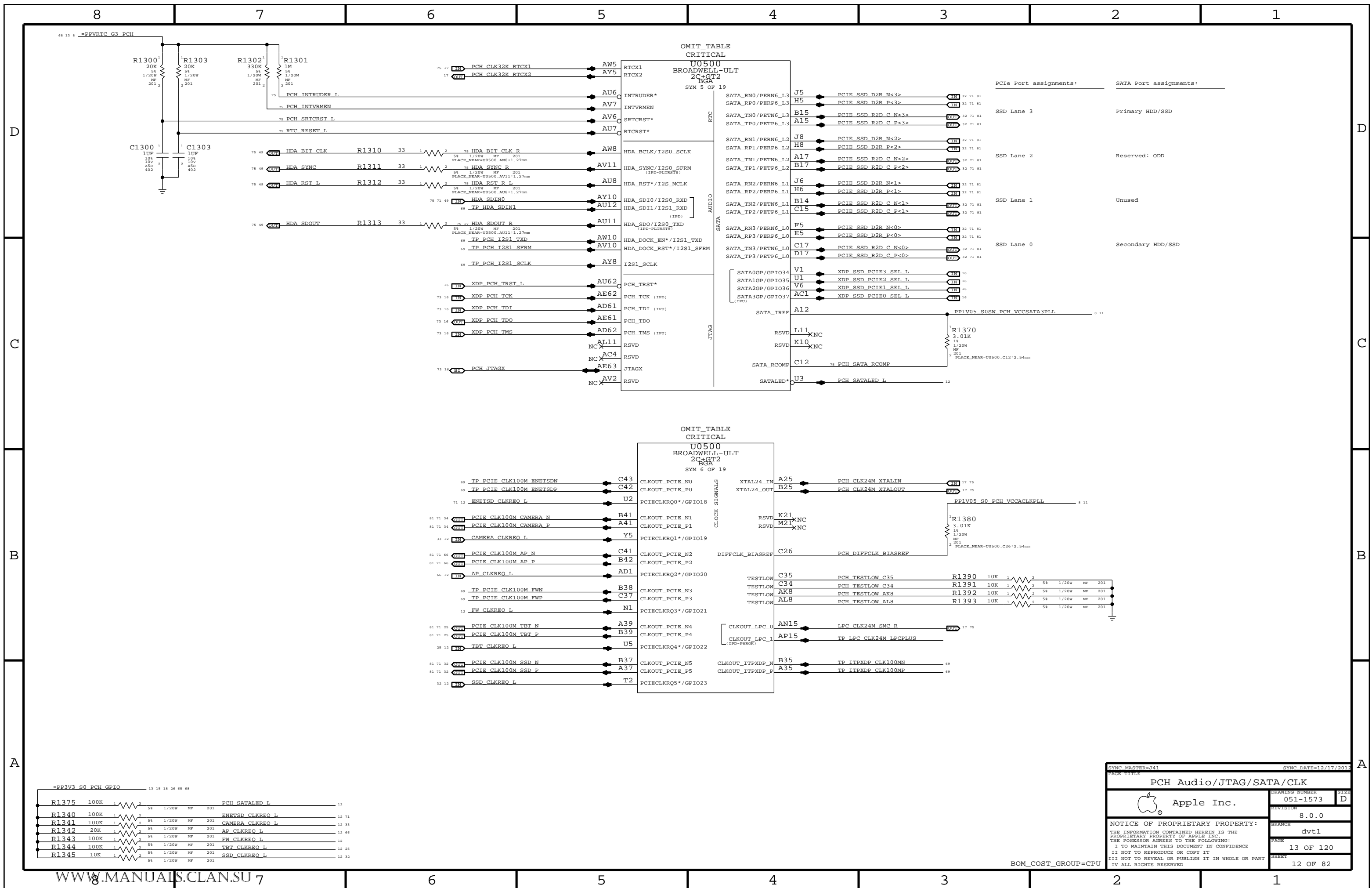
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BOM_COST_GROUP=CPU

Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9 as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.



OMIT TABLE
CRITICAL

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2C+GT2
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RTC

AUDIO

SATA

JTAG

CLOCK SIGNALS

OMIT TABLE
CRITICAL

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 6 OF 19

CLOCK SIGNALS

OMIT TABLE
CRITICAL

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 7 OF 19

CLOCK SIGNALS

OMIT TABLE
CRITICAL

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 8 OF 19

CLOCK SIGNALS

OMIT TABLE
CRITICAL

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BROADWELL-ULT
2C+GT2
BGA
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CLOCK SIGNALS

OMIT TABLE
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2C+GT2
BGA
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CLOCK SIGNALS

OMIT TABLE
CRITICAL

U0500
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2C+GT2
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CLOCK SIGNALS

OMIT TABLE
CRITICAL

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 12 OF 19

CLOCK SIGNALS

OMIT TABLE
CRITICAL

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 13 OF 19

CLOCK SIGNALS

PCIe Port assignments: SATA Port assignments:

Connector	Assignment	Notes
J5	PCIE SSD D2R N<3>	32 71 81
H5	PCIE SSD D2R P<3>	32 71 81
B15	PCIE SSD R2D C N<3>	32 71 81
A15	PCIE SSD R2D C P<3>	32 71 81
J8	PCIE SSD D2R N<2>	32 71 81
H8	PCIE SSD D2R P<2>	32 71 81
A17	PCIE SSD R2D C N<2>	32 71 81
B17	PCIE SSD R2D C P<2>	32 71 81
J6	PCIE SSD D2R N<1>	32 71 81
H6	PCIE SSD D2R P<1>	32 71 81
B14	PCIE SSD R2D C N<1>	32 71 81
C15	PCIE SSD R2D C P<1>	32 71 81
F5	PCIE SSD D2R N<0>	32 71 81
E5	PCIE SSD D2R P<0>	32 71 81
C17	PCIE SSD R2D C N<0>	32 71 81
D17	PCIE SSD R2D C P<0>	32 71 81
V1	XDP SSD PCIE3 SEL L	16
U1	XDP SSD PCIE2 SEL L	16
V6	XDP SSD PCIE1 SEL L	16
AC1	XDP SSD PCIE0 SEL L	16

Connector	Assignment	Notes
A12	PP1V05_S0SW_PCH_VCCSATA3PLL	8 11
L11	XNC	
K10	XNC	
C12	PCH SATA RCOMP	75
U3	PCH SATALED L	12

Connector	Assignment	Notes
A25	PCH CLK24M XTALIN	17 75
B25	PCH CLK24M XTALOUT	17 75
K21	XNC	
M21	XNC	
C26	PCH DIFFCLK_BIASREF	

Connector	Assignment	Notes
C35	PCH TESTLOW C35	R1390 10K 1 2 58 1/20W MF 201
C34	PCH TESTLOW C34	R1391 10K 1 2 58 1/20W MF 201
AK8	PCH TESTLOW AK8	R1392 10K 1 2 58 1/20W MF 201
AL8	PCH TESTLOW AL8	R1393 10K 1 2 58 1/20W MF 201

Connector	Assignment	Notes
AN15	LPC CLK24M SMC R	17 75
AP15	TP LPC CLK24M LPCPLUS	
B35	TP ITPXDP CLK100MN	69
A35	TP ITPXDP CLK100MP	69

Connector	Assignment	Notes
R1375	PCH SATALED L	13 15 18 26 65 68
R1340	ENETSD_CLKREQ L	12 71
R1341	CAMERA_CLKREQ L	12 33
R1342	AP_CLKREQ L	12 66
R1343	FW_CLKREQ L	12
R1344	TBT_CLKREQ L	12 25
R1345	SSD_CLKREQ L	12 20

SYNC MASTER=J41 SYNC DATE=12/17/2012
PAGE TITLE

PCH Audio/JTAG/SATA/CLK

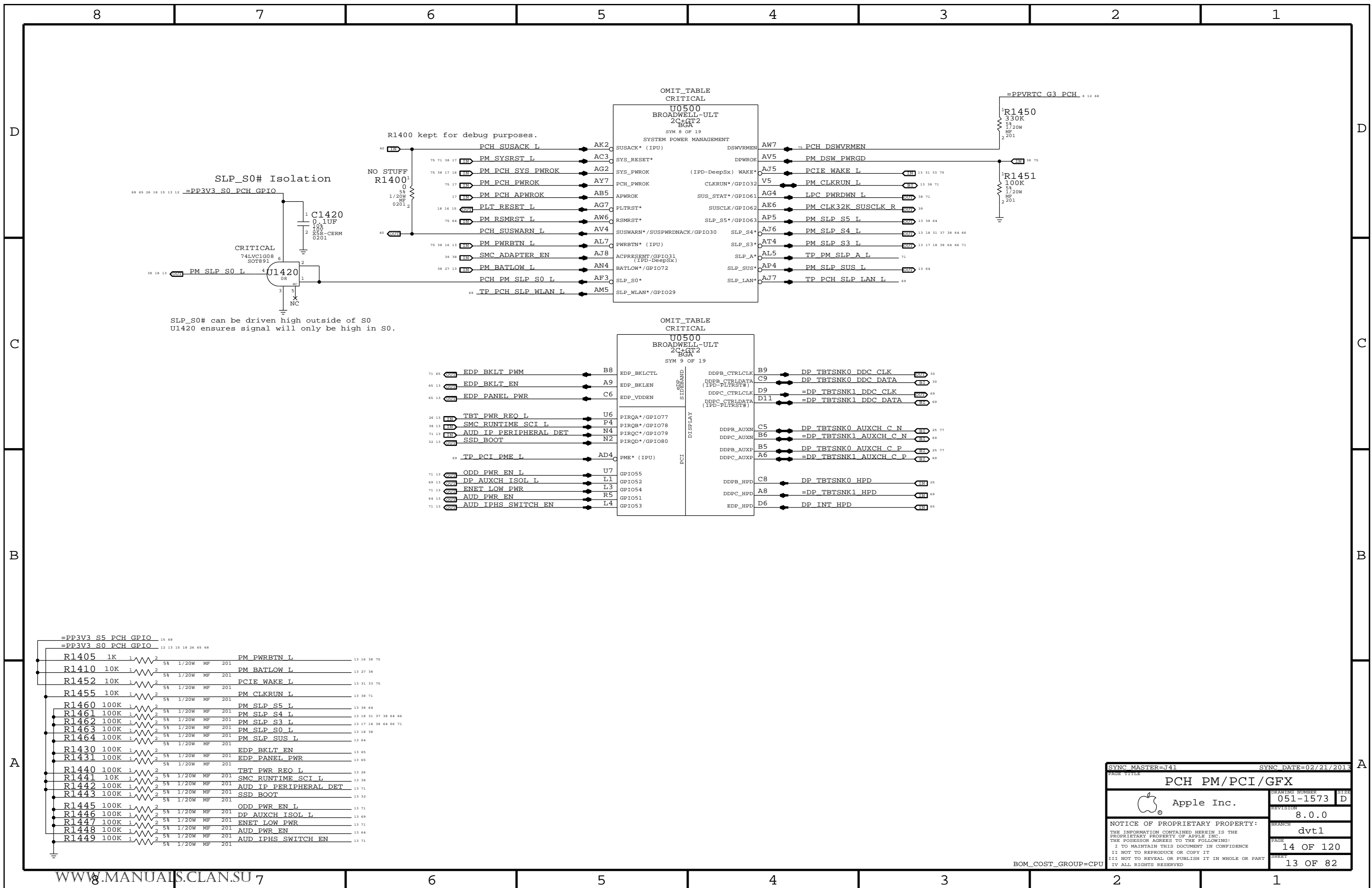
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PAGE: 13 OF 120
SHEET: 12 OF 82

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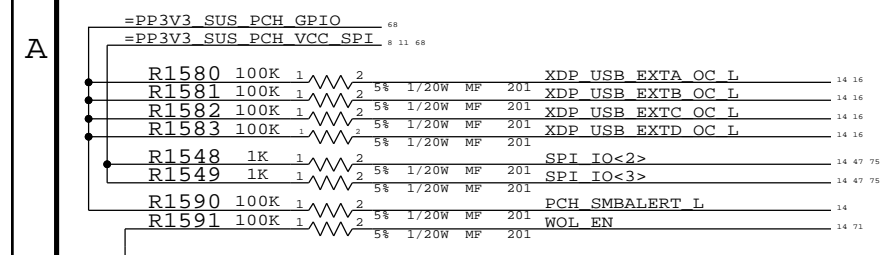
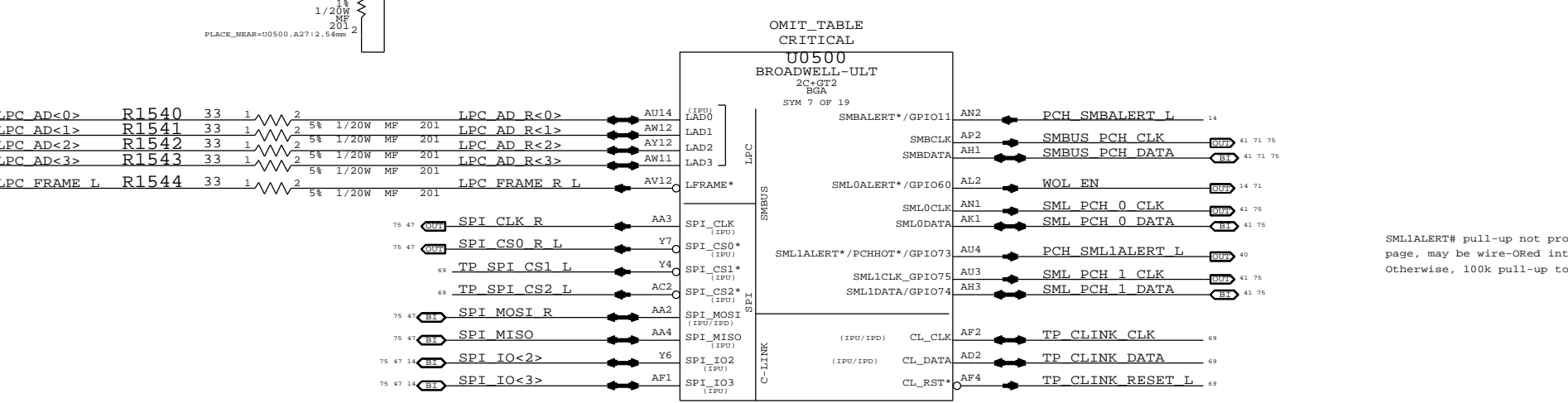
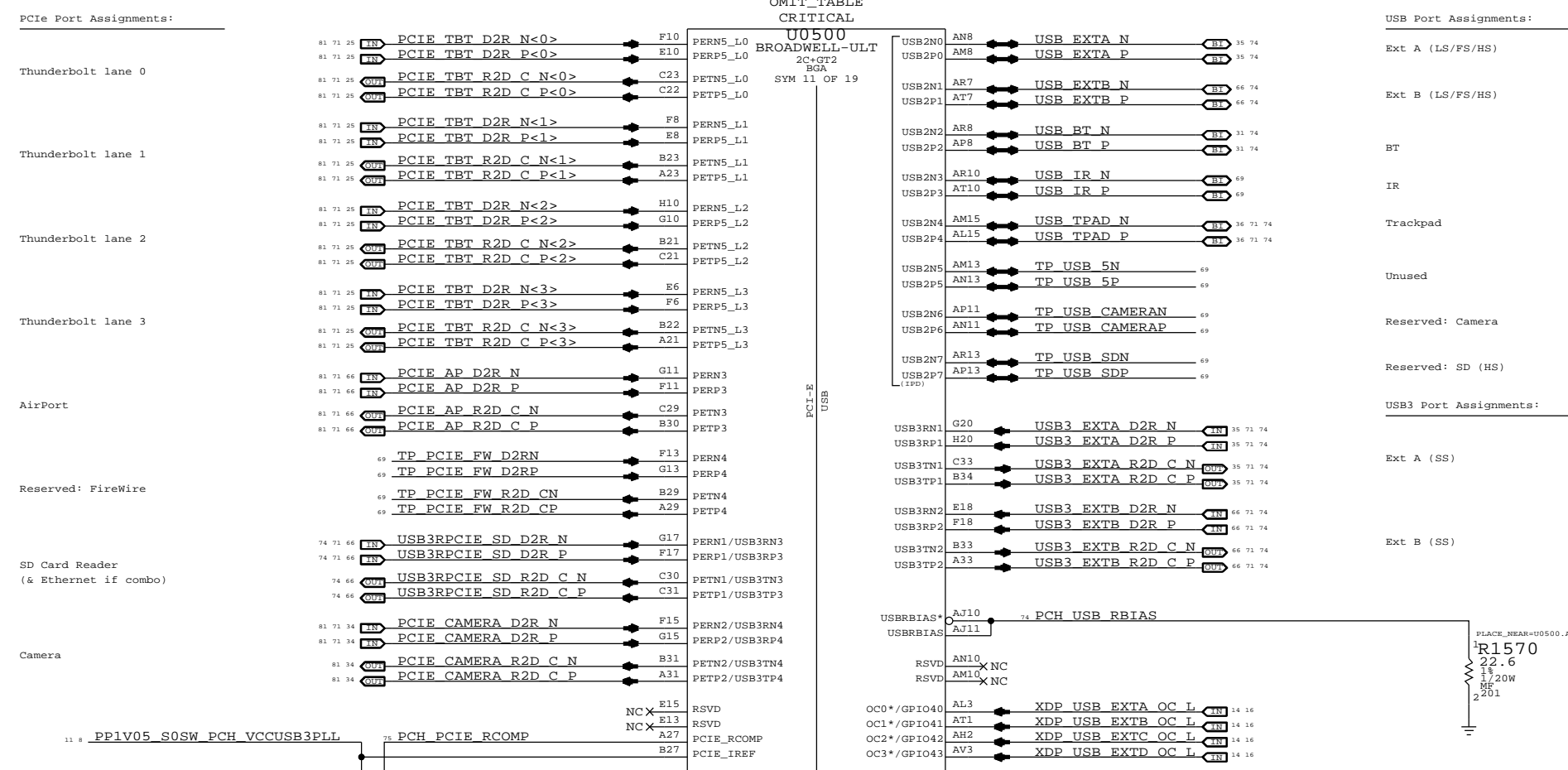


SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.

SYNC MASTER=J41		SYNC DATE=02/21/2013	
PCH PM/PCI/GFX			
Apple Inc.		DRAWING NUMBER	051-1573
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D
C
B
A

D
C
B
A



SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

SYNC MASTER=J41 SYNC DATE=10/23/2012

PAGE TITLE: PCH PCIe, USB, LPC, SPI, SMBus

Apple Inc.

DRAWING NUMBER: 051-1573

REVISION: 8.0.0

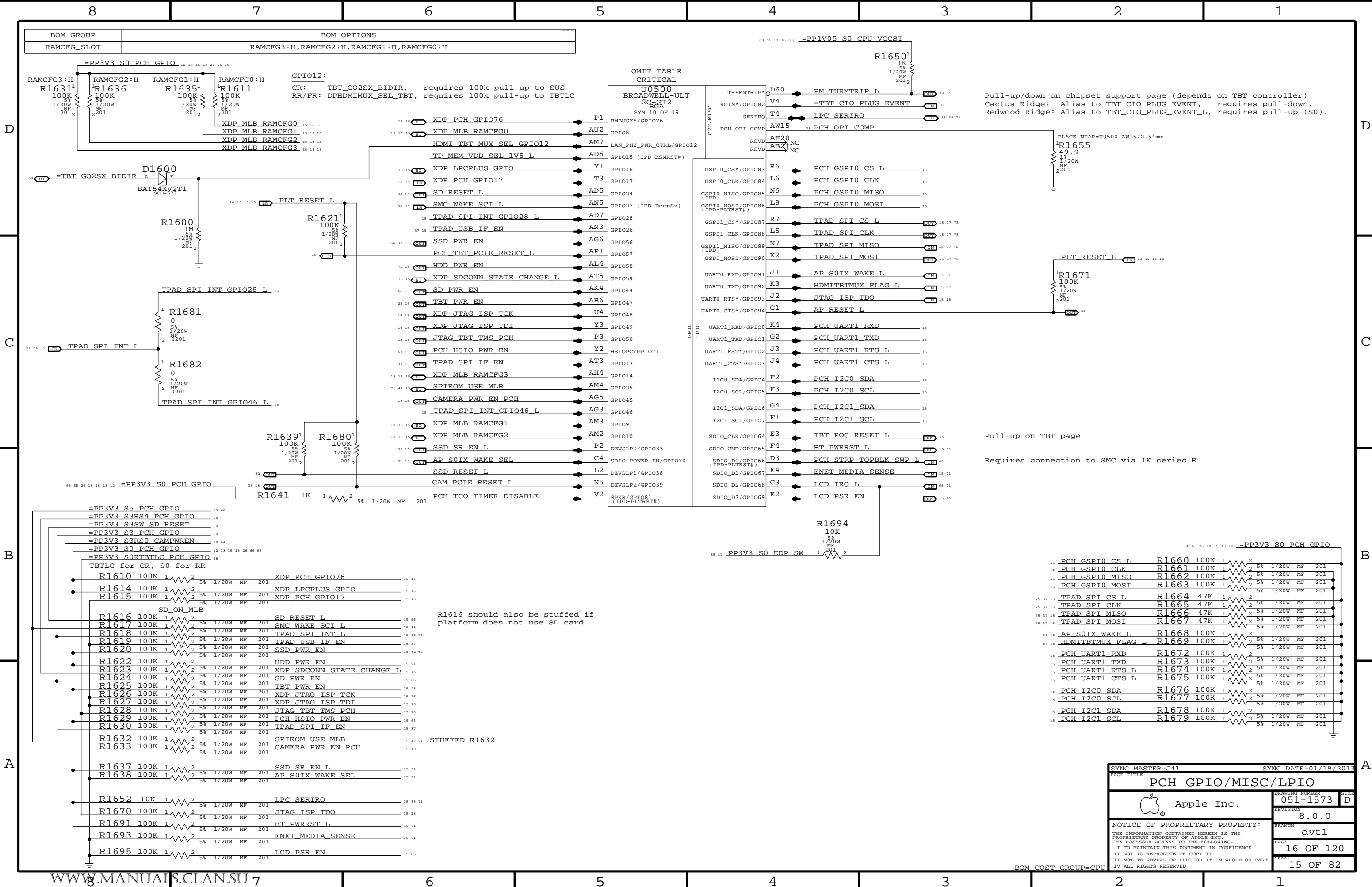
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BOM_COST_GROUP=CPU



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

OMIT_TABLE
CRITICAL

U0500 BROADWELL-ULT 2C+CT2 BGA SYM 10 OF 19	GPIO12: CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC
BMBUSY*/GPIO76	
LAN_PHY_PWR_CTRL/GPIO12	
GPIO15 (IPD-RSMRST#)	
GPIO16	
GPIO17	
GPIO24	
GPIO27 (IPD-DeepSx)	
GPIO28	
GPIO26	
GPIO56	
GPIO57	
GPIO58	
GPIO59	
GPIO44	
GPIO47	
GPIO48	
GPIO49	
GPIO50	
HSIOPC/GPIO71	
GPIO13	
GPIO14	
GPIO25	
GPIO45	
GPIO46	
GPIO9	
GPIO10	
DEVSLP0/GPIO33	
SDIO_POWER_EN/GPIO70	
DEVSLP1/GPIO38	
DEVSLP2/GPIO39	
SPKR/GPIO81 (IPD-PLTRST#)	

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUGIN_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUGIN_EVENT_L, requires pull-up (S0).

Pull-up on TBT page
Requires connection to SMC via 1K series R

R1631 100K 1/20W MF 201	RAMCFG3:H	R1636 100K 1/20W MF 201	RAMCFG2:H	R1635 100K 1/20W MF 201	RAMCFG1:H	R1611 100K 1/20W MF 201	RAMCFG0:H
XDP MLB RAMCFG0 15 16 18							
XDP MLB RAMCFG1 15 16 18							
XDP MLB RAMCFG2 15 16 18							
XDP MLB RAMCFG3 15 16 18							
GPIO12: CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS							
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC							
=PP3V3 S0 PCH GPIO 12 13 15 16 26 65 68							
R1631 100K 1/20W MF 201							
R1636 100K 1/20W MF 201							
R1635 100K 1/20W MF 201							
R1611 100K 1/20W MF 201							
XDP PCH GPIO76 P1 15 16							
XDP MLB RAMCFG0 AU2 18 16 15							
HDMI TBT MUX_SEL GPIO12 AM7 16 15							
TP MEM VDD_SEL 1V5 L AD6 16 15							
XDP LPCPLUS GPIO Y1 16 15							
XDP PCH GPIO17 T3 16 15							
SD RESET L AD5 66 15							
SMC WAKE SCI L AN5 38 15							
TPAD SPI INT GPIO28 L AD7 15							
TPAD USB IF EN AN3 37 15							
SSD PWR EN AG6 64 32 15							
PCH TBT PCIE RESET L AP1 71 15							
HDD PWR EN AL4 71 15							
XDP SDCONN STATE CHANGE L AT5 16 15							
SD PWR EN AK4 66 15							
TBT PWR EN AB6 25 15							
XDP JTAG ISP TCK U4 16 15							
XDP JTAG ISP TDI Y3 16 15							
JTAG TBT TMS PCH P3 18 15							
PCH HSIO PWR EN Y2 63 15							
TPAD SPI IF EN AT3 37 15							
XDP MLB RAMCFG3 AH4 18 15							
SPIROM USE MLB AM4 71 47 15							
CAMERA PWR_EN_PCH AG5 18 15							
TPAD SPI INT GPIO46 L AG3 15							
XDP MLB RAMCFG1 AM3 18 15							
XDP MLB RAMCFG2 AM2 18 15							
SSD SR EN L P2 32 15							
AP SOIX WAKE SEL C4 31 15							
SSD RESET L L2 31 15							
CAM_PCIE_RESET_L N5 31 15							
PCH TCO_TIMER_DISABLE V2 31 15							
=PP3V3 S5 PCH GPIO 13 68							
=PP3V3 S3RS4 PCH GPIO 68							
=PP3V3 S3SW_SD_RESET 68							
=PP3V3 S3 PCH GPIO 68							
=PP3V3 S3RS0_CAMPWREN 18 44							
=PP3V3 S0 PCH GPIO 12 13 15 16 26 65 68							
=PP3V3 S0RTTBTLC_PCH_GPIO 68							
TBTLC for CR, S0 for RR							
R1610 100K 1/20W MF 201							
XDP PCH GPIO76 15 16							
R1614 100K 1/20W MF 201							
XDP LPCPLUS GPIO 15 16							
R1615 100K 1/20W MF 201							
XDP PCH GPIO17 15 16							
SD_ON_MLB							
R1616 100K 1/20W MF 201							
SD RESET L 15 66							
R1617 100K 1/20W MF 201							
SMC WAKE SCI L 15 38							
R1618 100K 1/20W MF 201							
TPAD SPI INT L 15 36 71							
R1619 100K 1/20W MF 201							
TPAD USB IF EN 15 37							
R1620 100K 1/20W MF 201							
SSD PWR EN 15 32 64							
R1622 100K 1/20W MF 201							
HDD PWR EN 15 71							
R1623 100K 1/20W MF 201							
XDP SDCONN STATE CHANGE L 15 16							
R1624 100K 1/20W MF 201							
SD PWR EN 15 66							
R1625 100K 1/20W MF 201							
TBT PWR EN 15 25							
R1626 100K 1/20W MF 201							
XDP JTAG ISP TCK 15 16							
R1627 100K 1/20W MF 201							
XDP JTAG ISP TDI 15 16							
R1628 100K 1/20W MF 201							
JTAG TBT TMS PCH 15 18							
R1629 100K 1/20W MF 201							
PCH HSIO PWR EN 15 63							
R1630 100K 1/20W MF 201							
TPAD SPI IF EN 15 37							
R1632 100K 1/20W MF 201							
SPIROM USE MLB 15 47 71							
R1633 100K 1/20W MF 201							
CAMERA PWR_EN_PCH 15 18							
R1637 100K 1/20W MF 201							
SSD SR EN L 15 32							
R1638 100K 1/20W MF 201							
AP SOIX WAKE SEL 15 31							
R1652 10K 1/20W MF 201							
LPC SERIRO 15 38 71							
R1670 100K 1/20W MF 201							
JTAG ISP_TDO 15 18							
R1691 100K 1/20W MF 201							
BT_PWRST_L 15 71							
R1693 100K 1/20W MF 201							
ENET_MEDIA_SENSE 15 71							
R1695 100K 1/20W MF 201							
LCD_PSR_EN 15 65							

R1616 should also be stuffed if platform does not use SD card

STUFFED R1632

=PP3V3 S0 PCH GPIO 68 65 26 18 15 13 12							
15	PCH GSPI0_CS_L	R1660	100K	1	2	5%	1/20W MF 201
15	PCH GSPI0_CLK	R1661	100K	1	2	5%	1/20W MF 201
15	PCH GSPI0_MISO	R1662	100K	1	2	5%	1/20W MF 201
15	PCH GSPI0_MOSI	R1663	100K	1	2	5%	1/20W MF 201
75 37 15	TPAD SPI_CS_L	R1664	47K	1	2	5%	1/20W MF 201
75 37 15	TPAD SPI_CLK	R1665	47K	1	2	5%	1/20W MF 201
75 37 15	TPAD SPI_MISO	R1666	47K	1	2	5%	1/20W MF 201
75 37 15	TPAD SPI_MOSI	R1667	47K	1	2	5%	1/20W MF 201
31 15	AP_SOIX_WAKE_L	R1668	100K	1	2	5%	1/20W MF 201
67 15	HDMITBTMUX_FLAG_L	R1669	100K	1	2	5%	1/20W MF 201
15	PCH_UART1_RXD	R1672	100K	1	2	5%	1/20W MF 201
15	PCH_UART1_TXD	R1673	100K	1	2	5%	1/20W MF 201
15	PCH_UART1_RTS_L	R1674	100K	1	2	5%	1/20W MF 201
15	PCH_UART1_CTS_L	R1675	100K	1	2	5%	1/20W MF 201
15	PCH_I2C0_SDA	R1676	100K	1	2	5%	1/20W MF 201
15	PCH_I2C0_SCL	R1677	100K	1	2	5%	1/20W MF 201
15	PCH_I2C1_SDA	R1678	100K	1	2	5%	1/20W MF 201
15	PCH_I2C1_SCL	R1679	100K	1	2	5%	1/20W MF 201

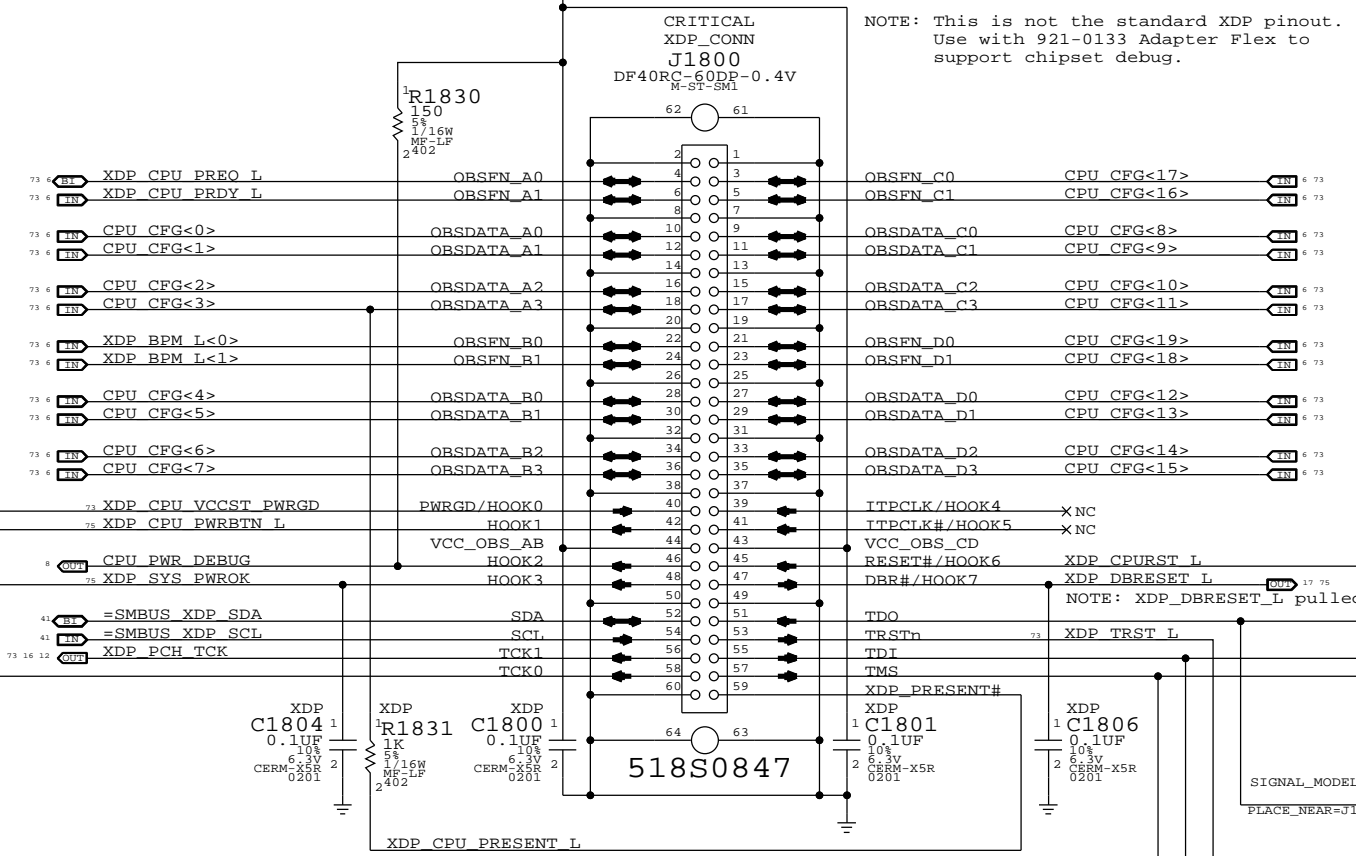
SYNC MASTER=J41		SYNC DATE=01/19/2013	
PAGE TITLE			
PCH GPIO/MISC/LPIO			
Apple Inc.		DRAWING NUMBER	051-1573
REVISION		BRANCH	dvt1
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Extra BPM Testpoints

- 73 6 XDP BPM L<2> TP1802
- 73 6 XDP BPM L<3> TP1803
- 73 6 XDP BPM L<4> TP1804
- 73 6 XDP BPM L<5> TP1805
- 73 6 XDP BPM L<6> TP1806
- 73 6 XDP BPM L<7> TP1807

Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.



- 73 16 XDP CPU TDO R1810 51 1
 - 73 16 XDP CPU TCK R1813 51 2
- TDI and TMS are terminated in CPU.

D

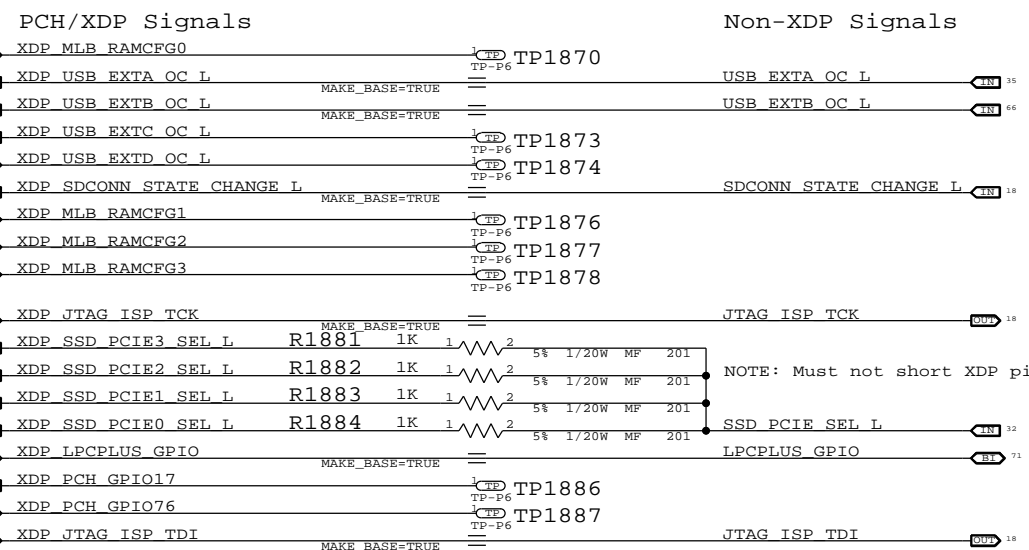
D

C

C

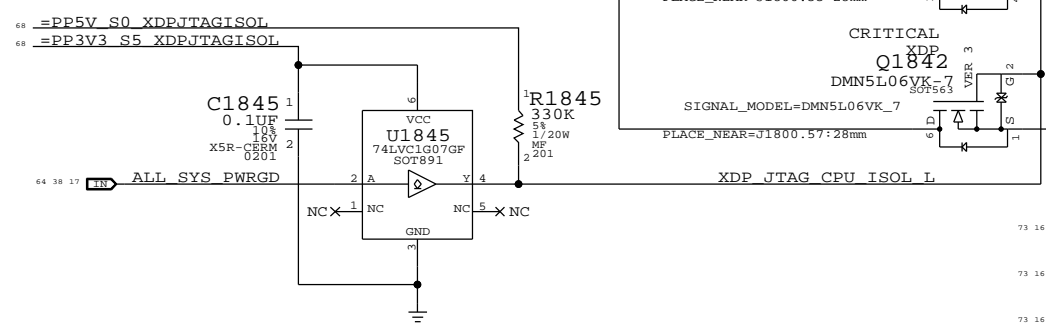
PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.



Unused & MLB_RAMCFGx GPIOs have TPs.
 USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
 SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
 JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
 NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
 SSD_PCIEx_SEL_L straps are connected via 1K to common net.
 LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation



- 73 16 PCH JTAGX R1899 1K
- 73 16 XDP_PCH_TDO R1890 51
- 73 16 XDP_PCH_TDI R1891 51
- 73 16 XDP_PCH_TMS R1892 51
- 73 16 XDP_PCH_TCK R1896 51
- 73 16 XDP_PCH_TRST_L R1897 51

A

A

PAGE TITLE		SYNC DATE=12/21/2012	
CPU/PCH Merged XDP			
Apple Inc.		DRAWING NUMBER	051-1573
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		BRANCH	dvt1
		PAGE	18 OF 120
		SHEET	16 OF 82

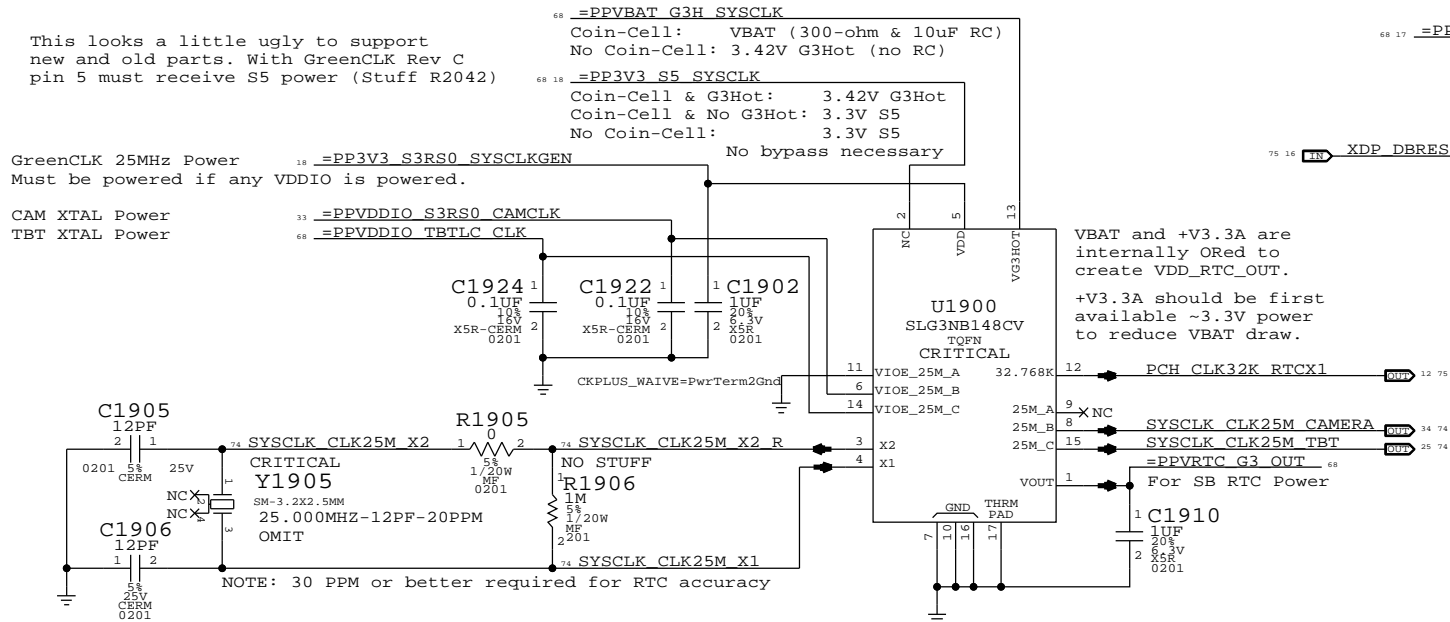
System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

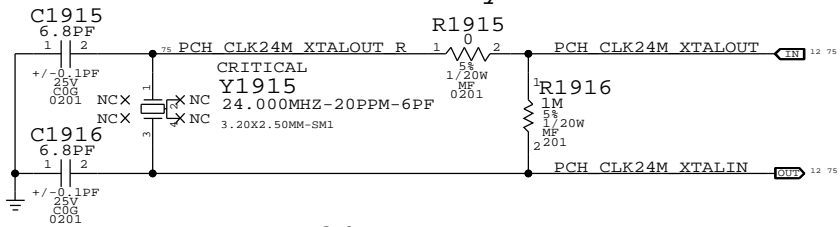
This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

GreenCLK 25MHz Power Must be powered if any VDDIO is powered.

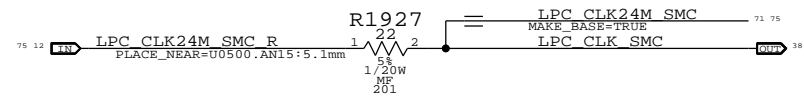
CAM XTAL Power
TBT XTAL Power



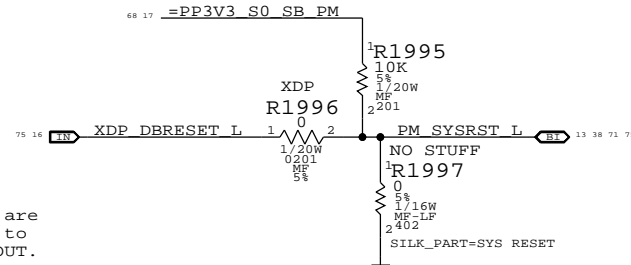
PCH 24MHz Crystal



PCH 24MHz Outputs

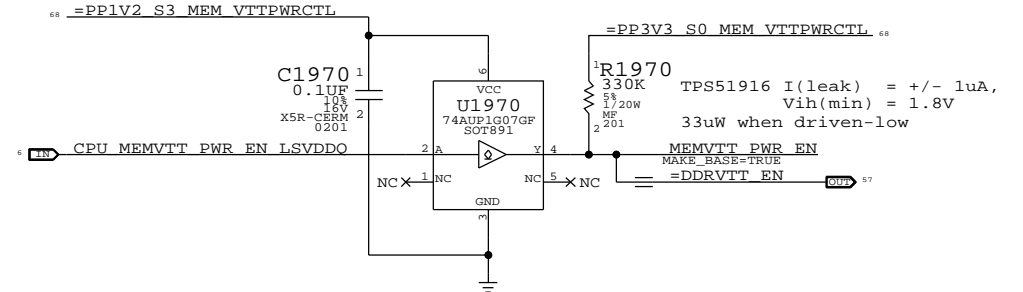


PCH Reset Button

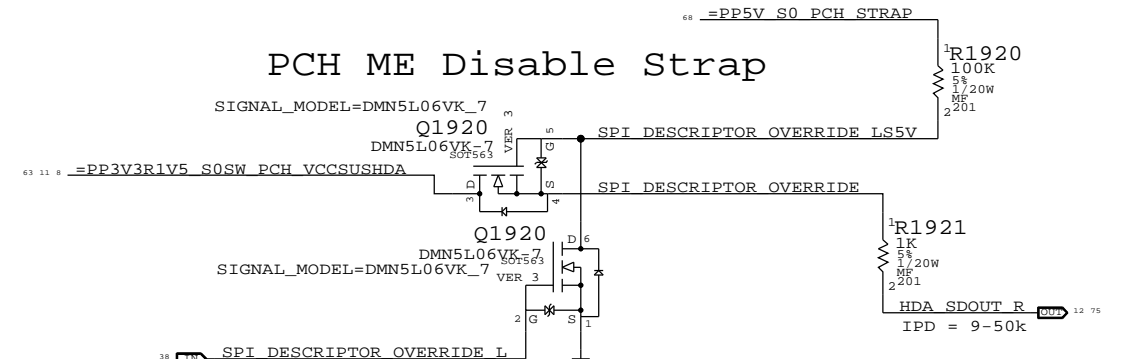


Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

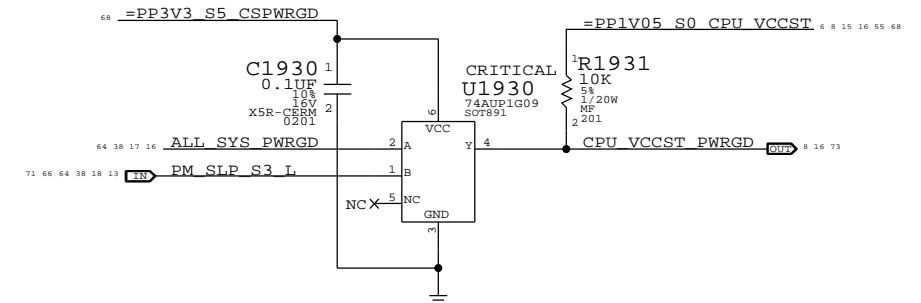


PCH ME Disable Strap

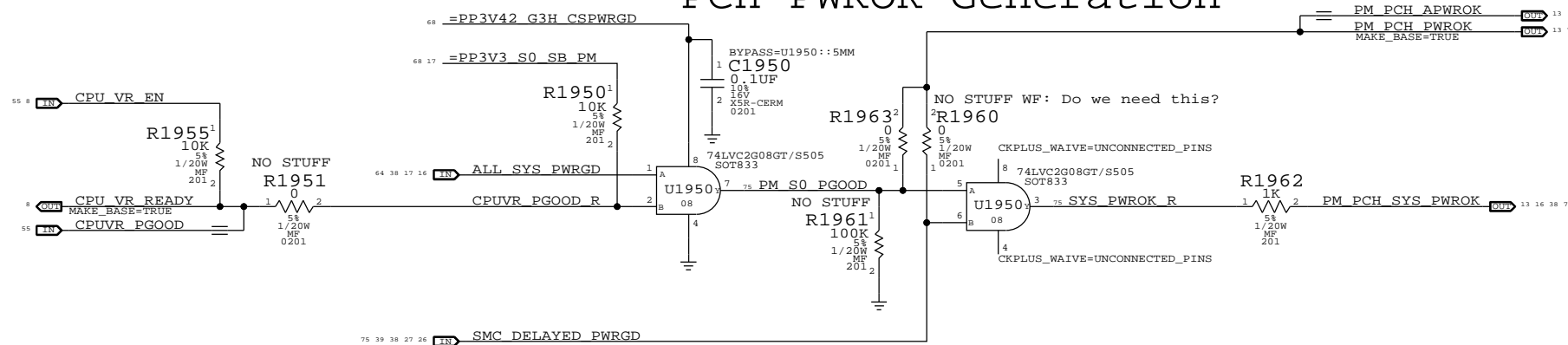


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD



PCH PWROK Generation



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL, 25MHZ, 20PPM, 12PF, 3.2X2.5X.6MM, 85C	Y1905		

SYNC MASTER=J41 SYNC DATE=01/30/2013

Chipset Support

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

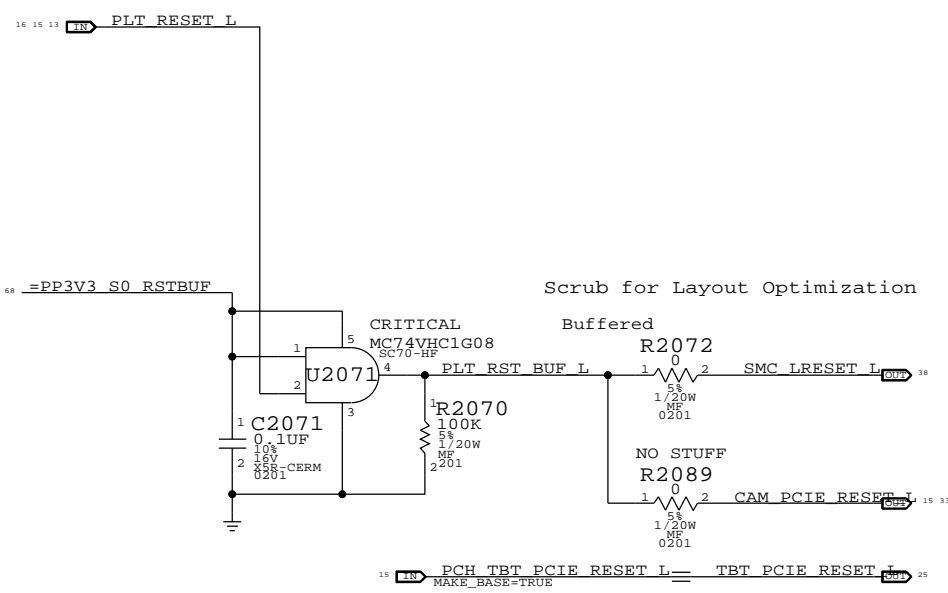
PAGE: 19 OF 120

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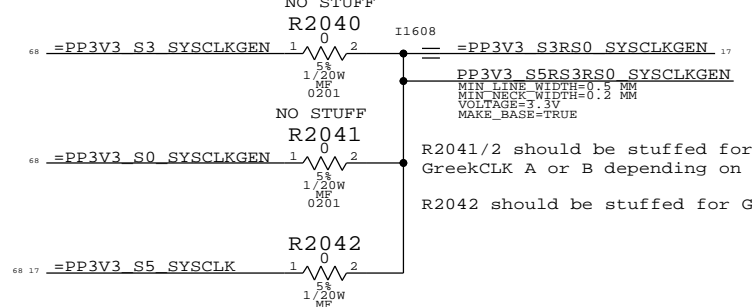
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Platform Reset Connections

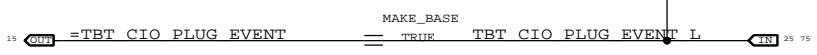


GreenCLK 25MHz Power



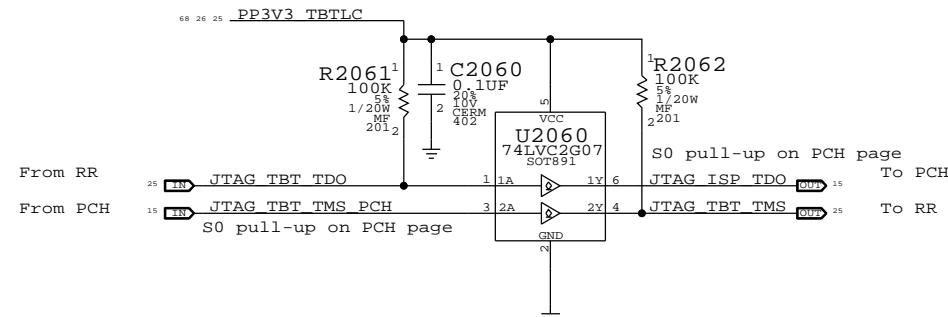
THUNDERBOLT PULL-UP

REDWOOD RIDGE PLUG_EVENT IS ACTIVE-LOW, ALWAYS DRIVEN (PULL-UP)



Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa. Isolation ensures no leakage to RR or PCH

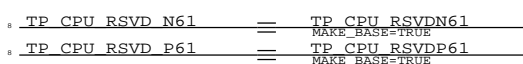


NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.

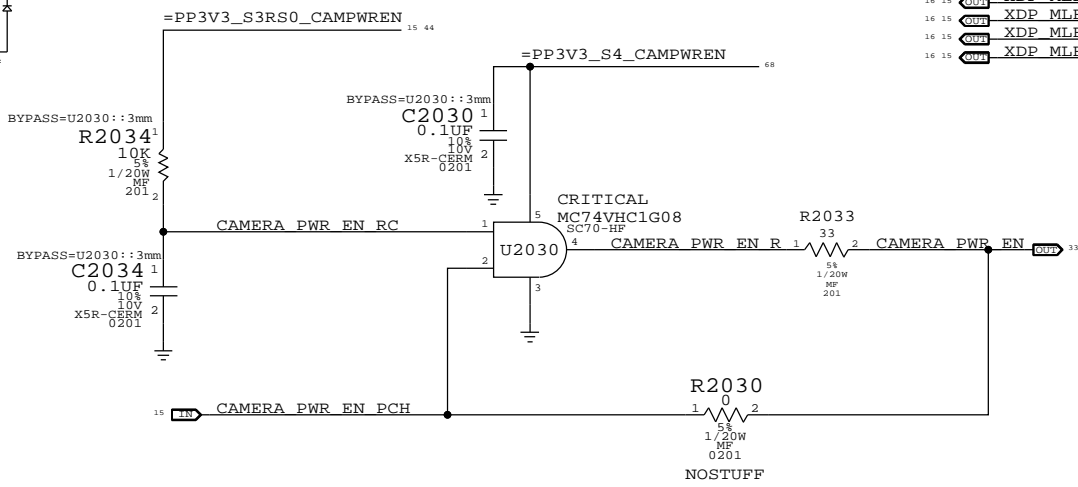
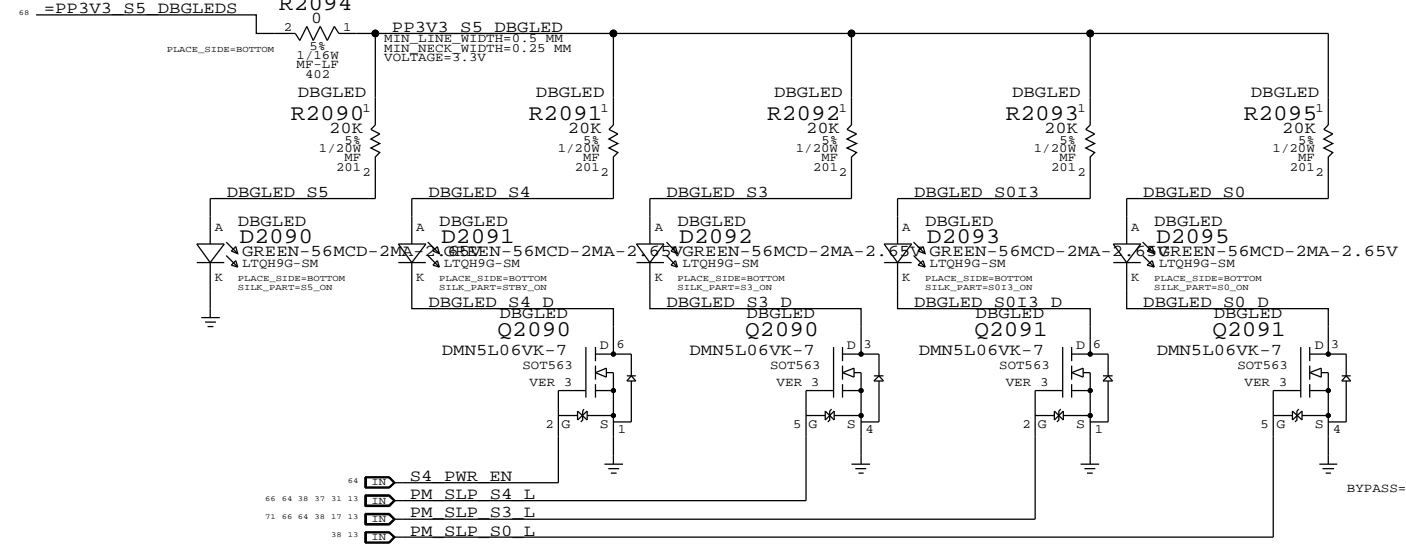


Pin N61 needs a TP for Power to perform iFDIM test. Renaming the pins N61 and P61 to remove automatic diffpari property



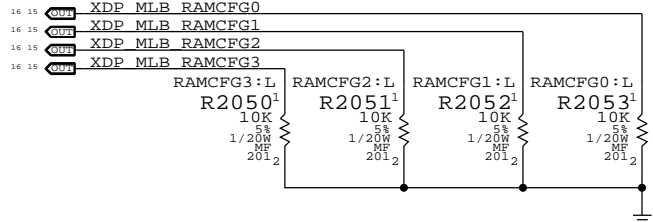
Power State Debug LEDs

(For development only)



RAM Configuration Straps

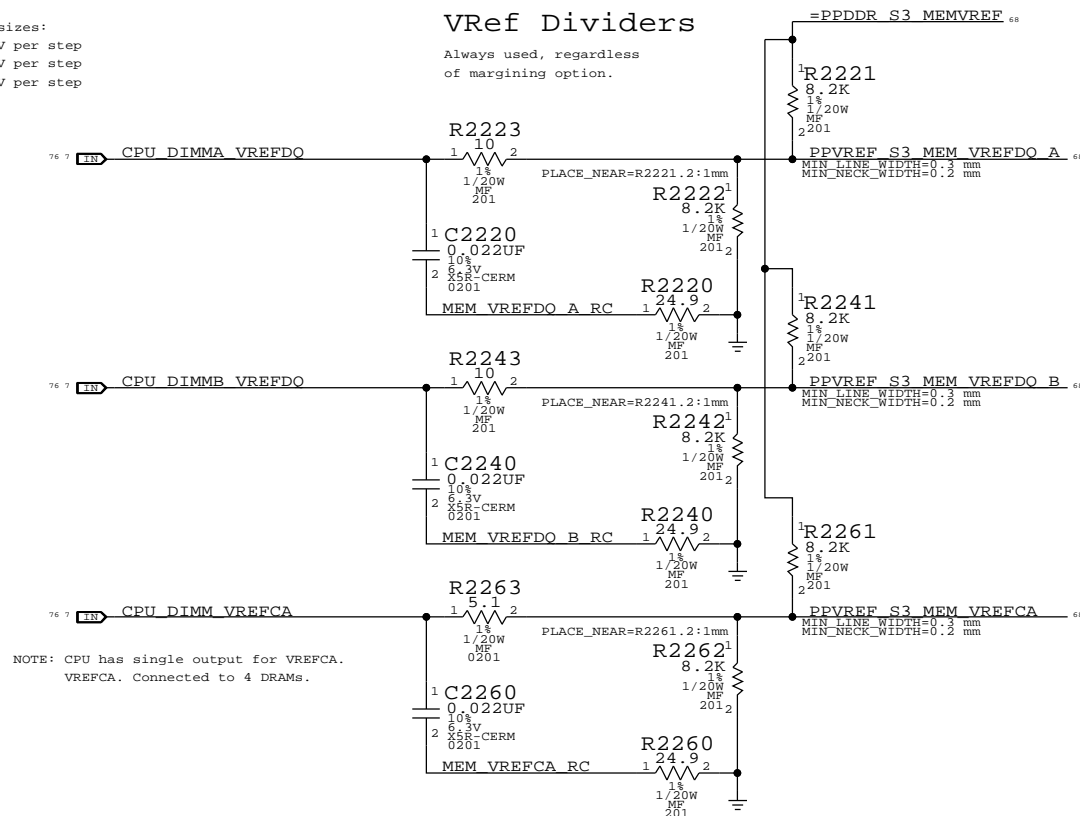
Pull-downs for chip-down RAM systems



SYNC MASTER=J41		SYNC DATE=10/23/2012	
Project Chipset Support			
Apple Inc.		DRAWING NUMBER	051-1573
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CPU-Based Margining

NOTE: CPU DAC output step sizes:
 DDR3 (1.5V) 7.70mV per step
 DDR3L (1.35V) 6.99mV per step
 LPDDR3 (1.2V) 7.77mV per step



Vref Dividers

Always used, regardless of margining option.

NOTE: CPU has single output for VREFCA. VREFCA. Connected to 4 DRAMs.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)
Margin target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)
Vref current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
 DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC MASTER=YHARTANTO J44 SYNC DATE=01/02/2013

LPDDR3 VREF Margining

Apple Inc.

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REVISION: 8.0.0

BRANCH: dvt1

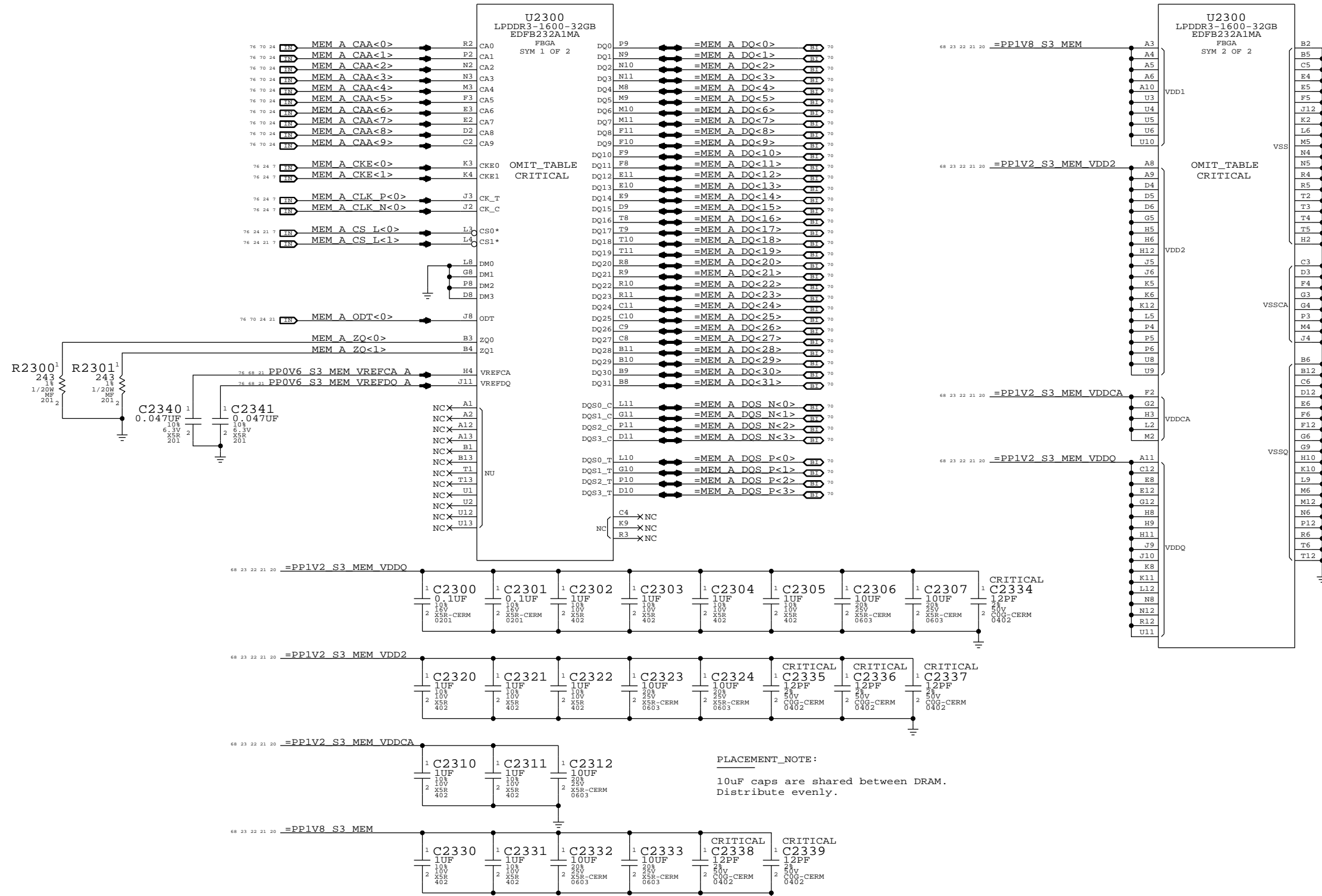
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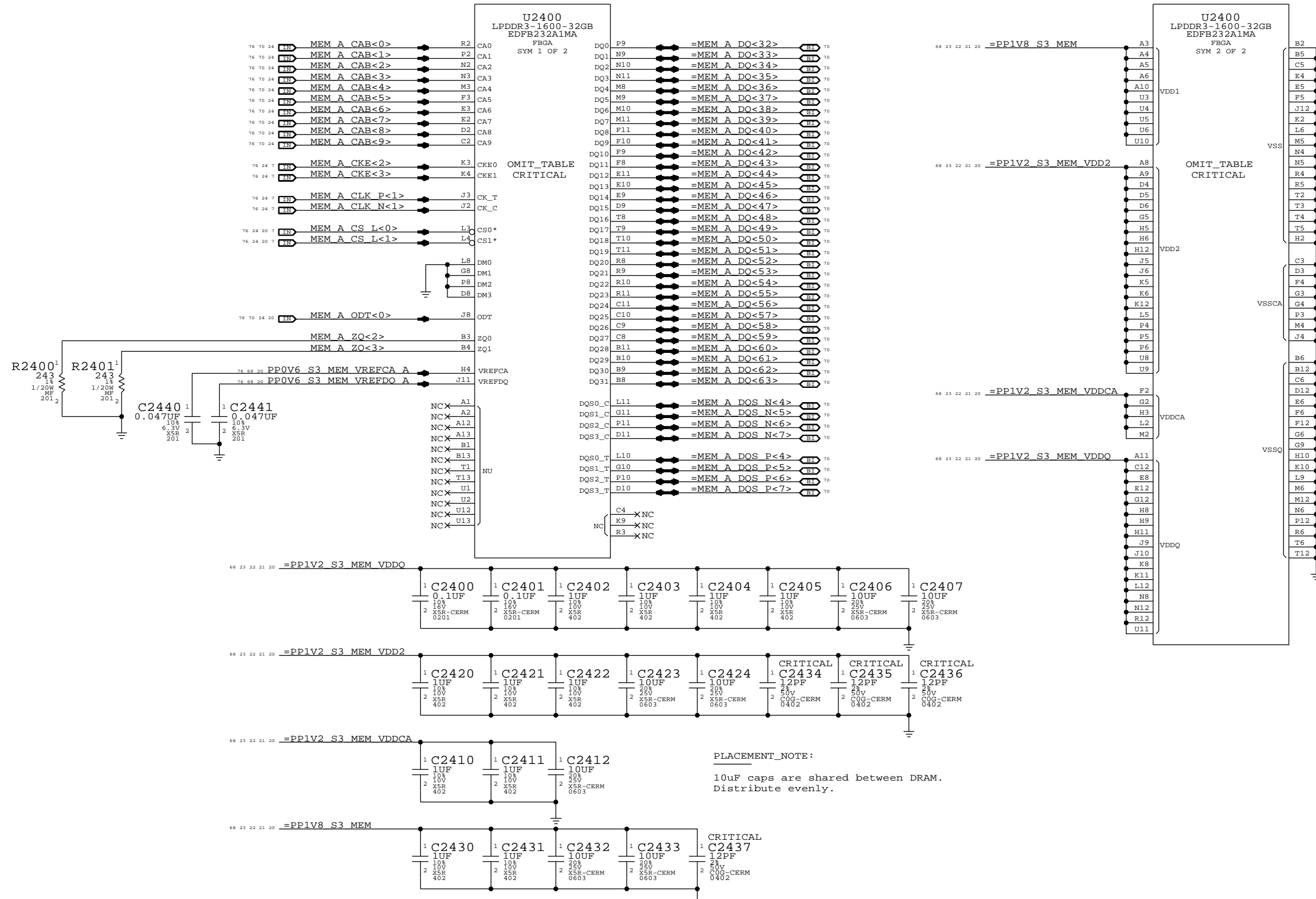
BOM_COST_GROUP=CPU SUPPORT

LPDDR3 CHANNEL A (0-31)



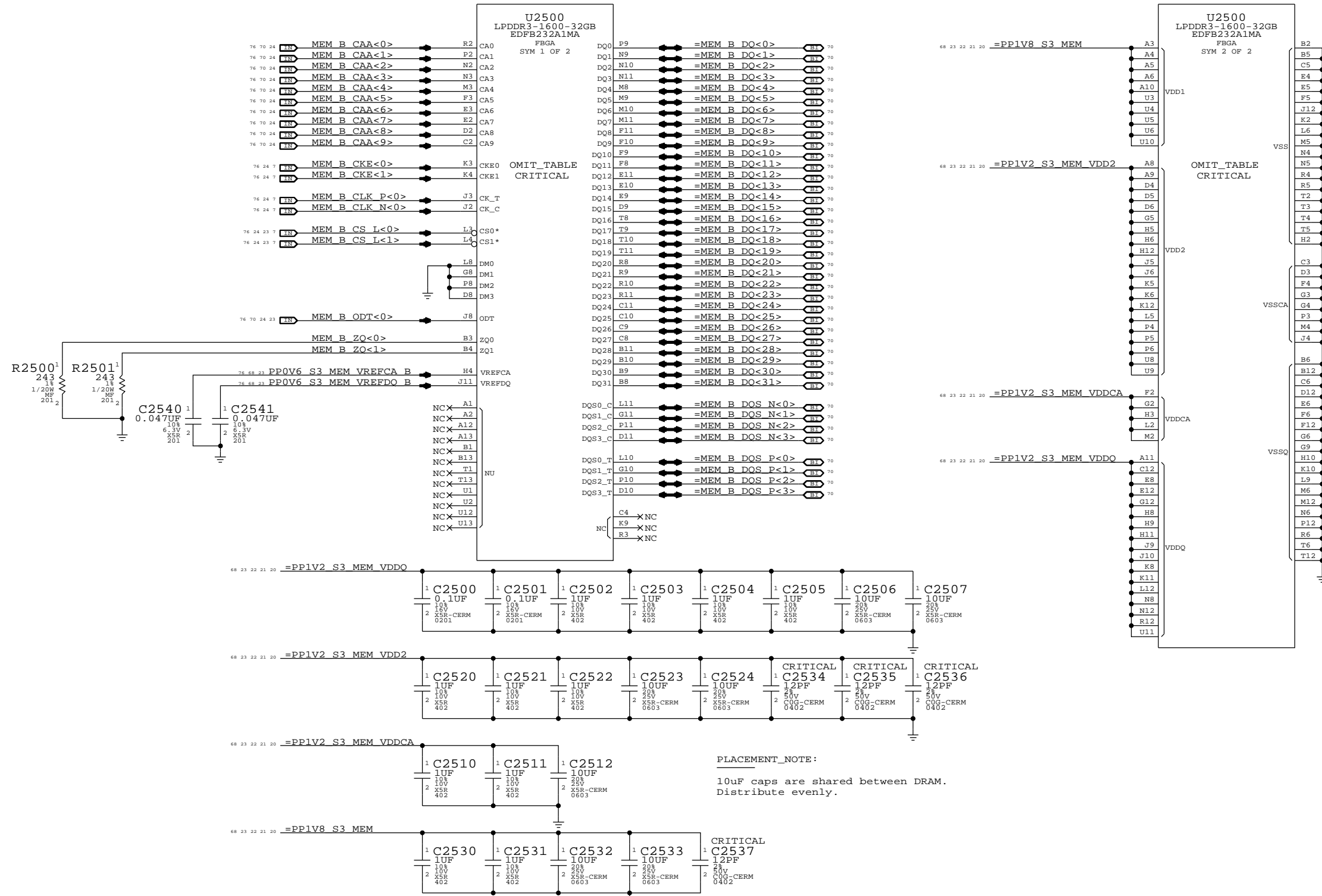
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REVISION 8.0.0		BRANCH dvt1	
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LPDDR3 CHANNEL A (32-63)



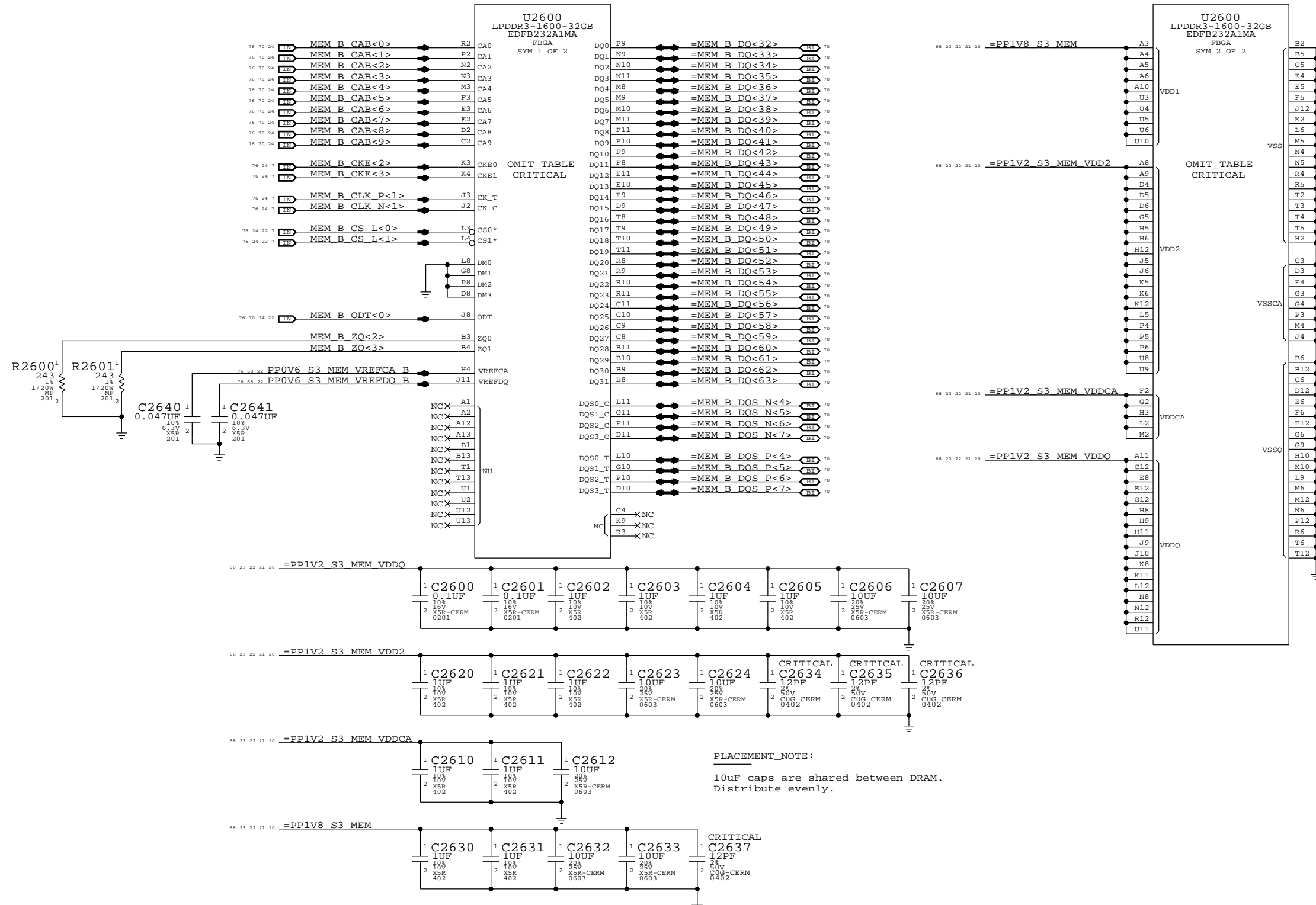
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LPDDR3 CHANNEL B (0-31)



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PAGE TITLE LPDDR3 DRAM Channel B (00-31)			
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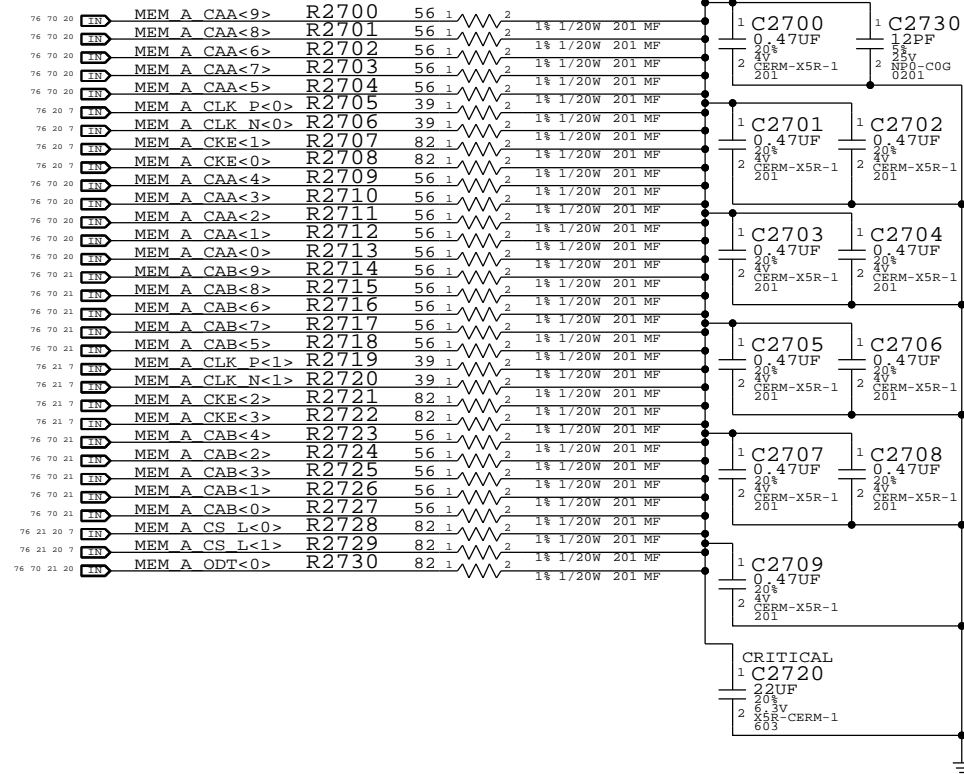
LPDDR3 CHANNEL B (32-63)



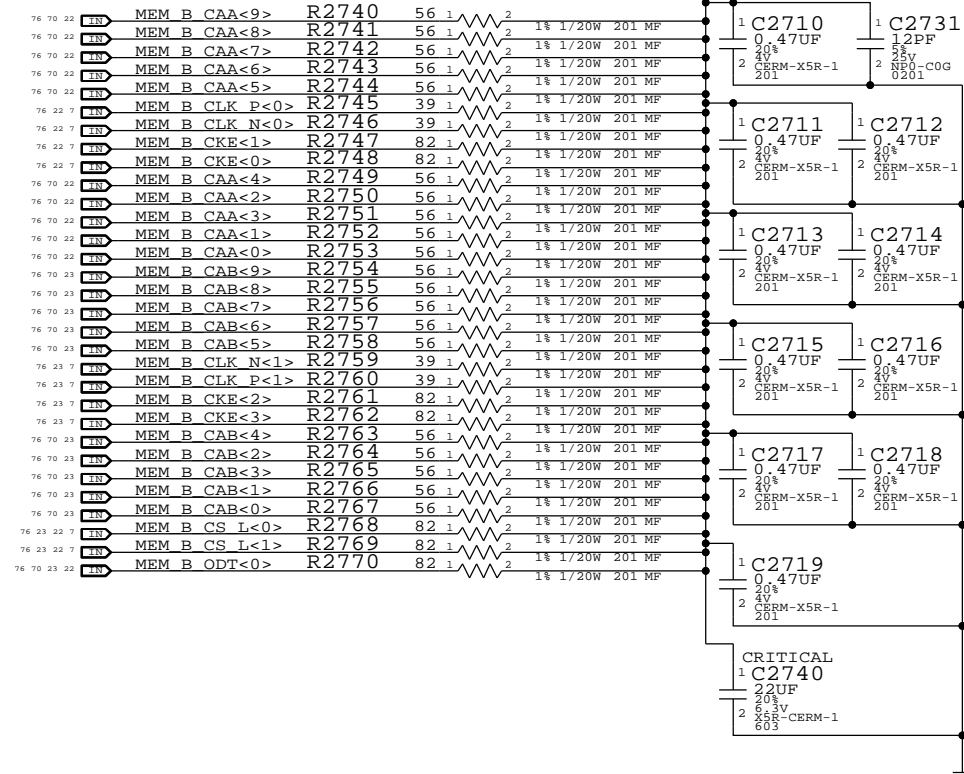
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REVISION 8.0.0		BRANCH dvt1	
PAGE 26 OF 120		SHEET 23 OF 82	
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Intel recommends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

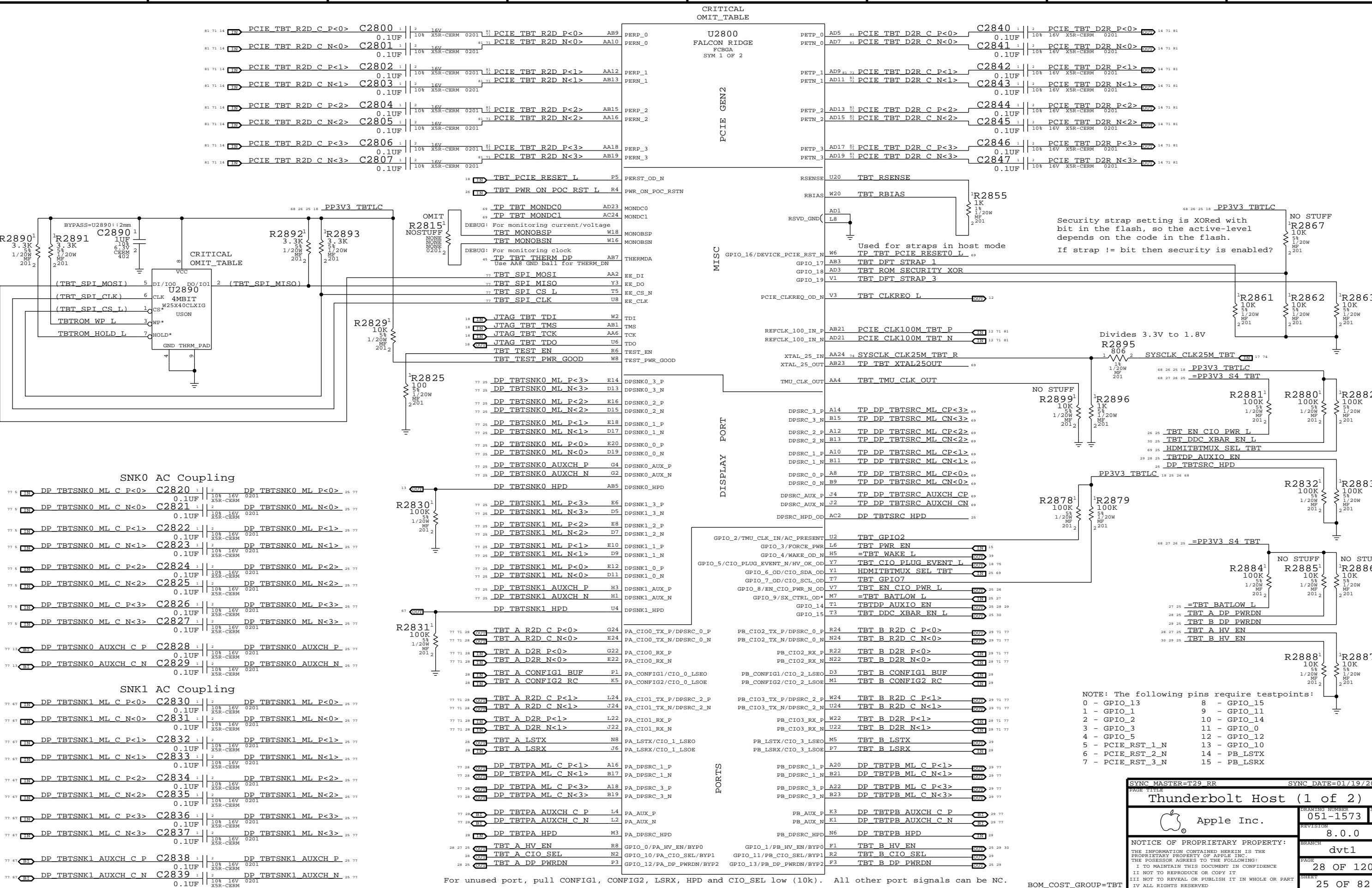
==PP0V6_S0_MEM_VTT_A



==PP0V6_S0_MEM_VTT_B



SYNC MASTER=J41_MLB		SYNC DATE=02/06/2013	
PAGE TITLE LPDDR3 DRAM Termination			
DRAWING NUMBER 051-1573		SIZE D	
REVISION 8.0.0		BRANCH dvt1	
PAGE 27 OF 120		SHEET 24 OF 82	
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Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash. If strap != bit then security is enabled?

Divides 3.3V to 1.8V

- NOTE: The following pins require testpoints:
- | | |
|------------------|--------------|
| 0 - GPIO_13 | 8 - GPIO_15 |
| 1 - GPIO_1 | 9 - GPIO_11 |
| 2 - GPIO_2 | 10 - GPIO_14 |
| 3 - GPIO_3 | 11 - GPIO_0 |
| 4 - GPIO_5 | 12 - GPIO_12 |
| 5 - PCIE_RST_1_N | 13 - GPIO_10 |
| 6 - PCIE_RST_2_N | 14 - PB_LSTX |
| 7 - PCIE_RST_3_N | 15 - PB_LSRX |

SYNC MASTER=T29 RE SYNC DATE=01/19/2013

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

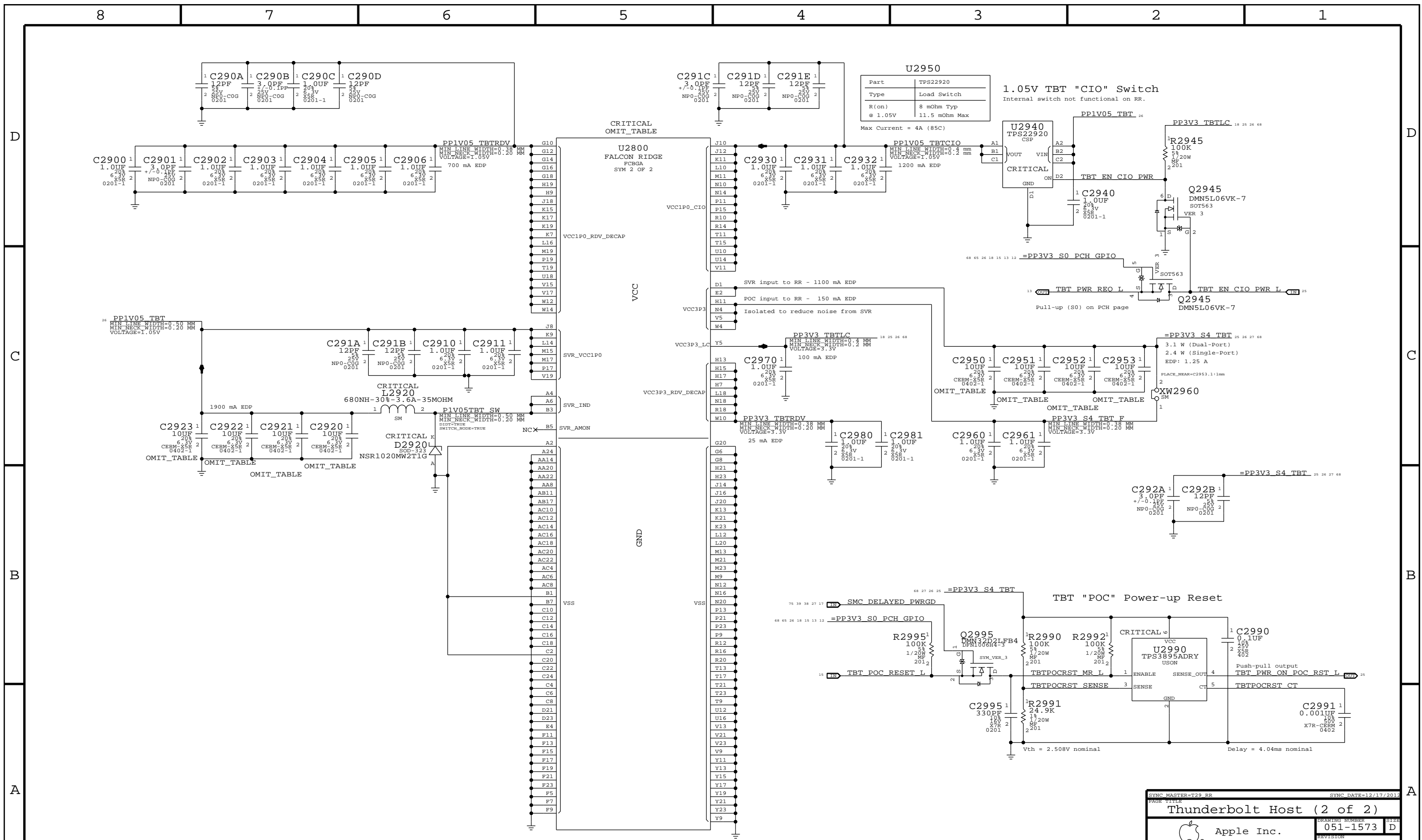
BRANCH: dvt1

PAGE: 28 OF 120

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SHEET: 25 OF 82

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	8	CAP, CER, 10UF, 20%, 6.3V, HRZTL, 0402		CRITICAL	

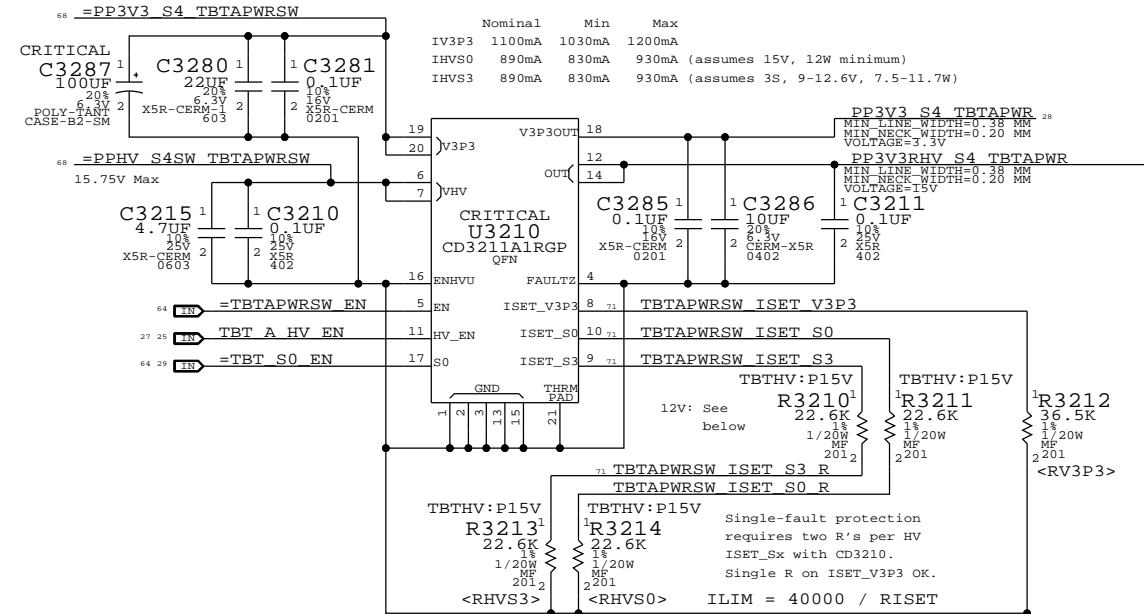
C2920, C2921, C2922, C2923, C2950, C2951, C2952, C2953

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC MASTER=T29_RR SYNC DATE=12/17/2012
 PAGE TITLE
Thunderbolt Host (2 of 2)
 Apple Inc.
 DRAWING NUMBER: 051-1573 SIZE: D
 REVISION: 8.0.0
 BRANCH: dvt1
 PAGE: 29 OF 120
 SHEET: 26 OF 82
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 BOM_COST_GROUP=TBT

3.3V/HV Power MUX

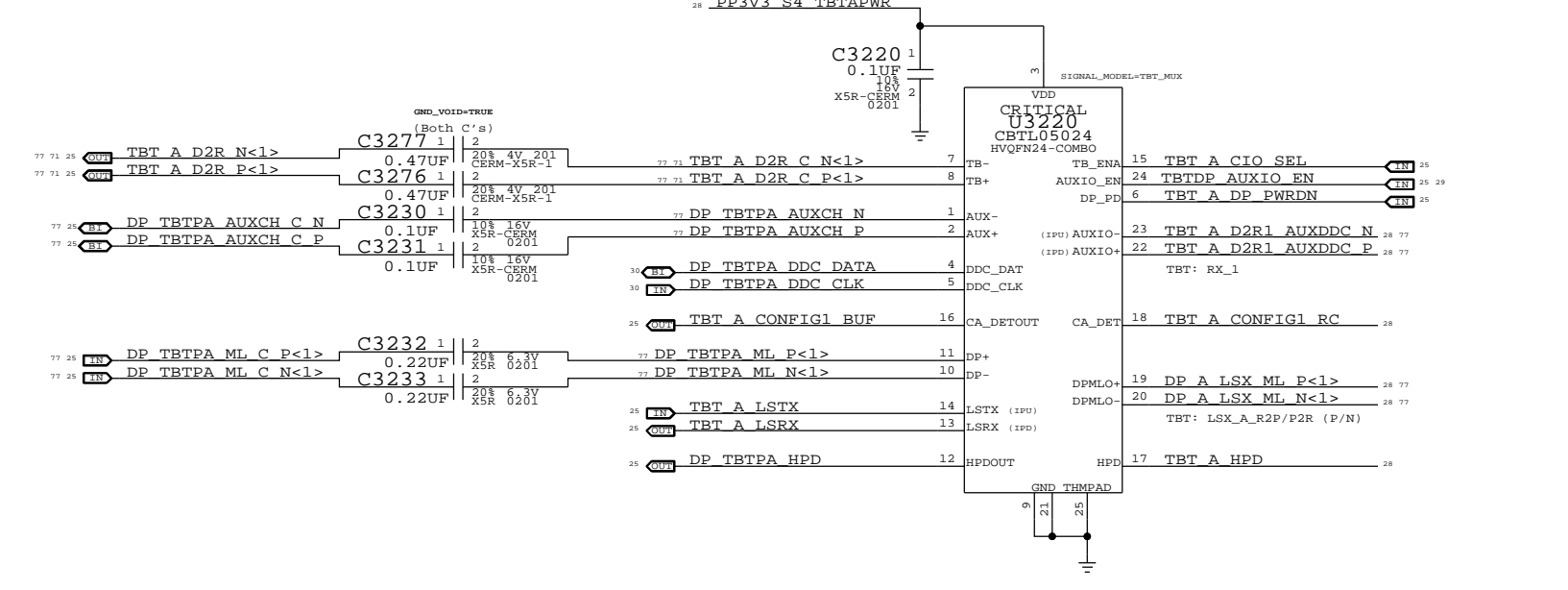
V3P3 must be S4 to support wake from Thunderbolt devices.



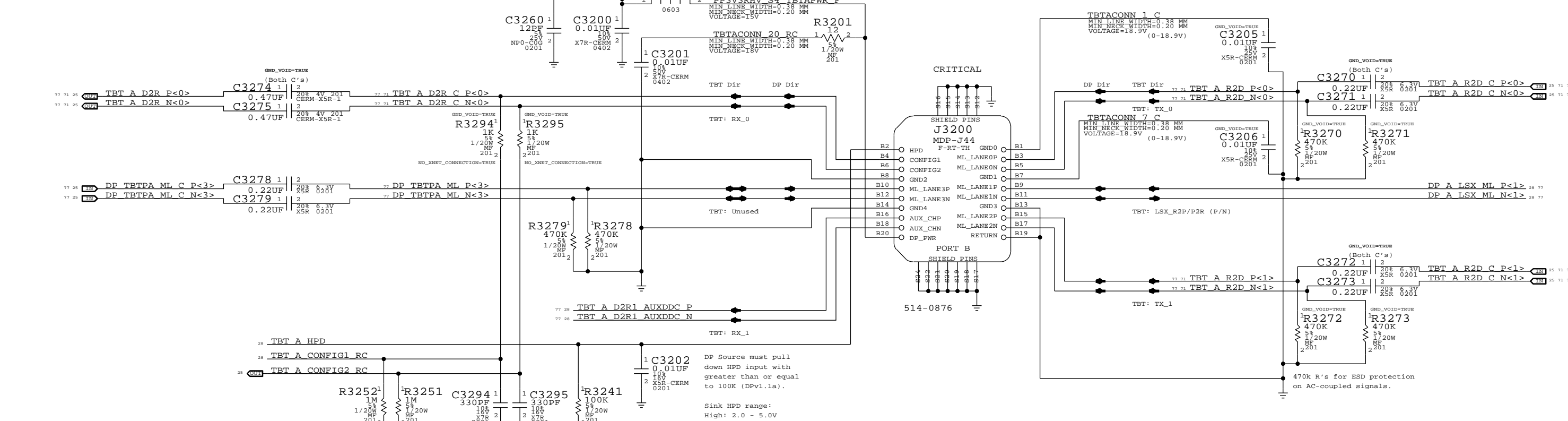
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal	Min	Max
IHV50/S3 1120mA	1090mA	1170mA (12W minimum)



Thunderbolt Connector A

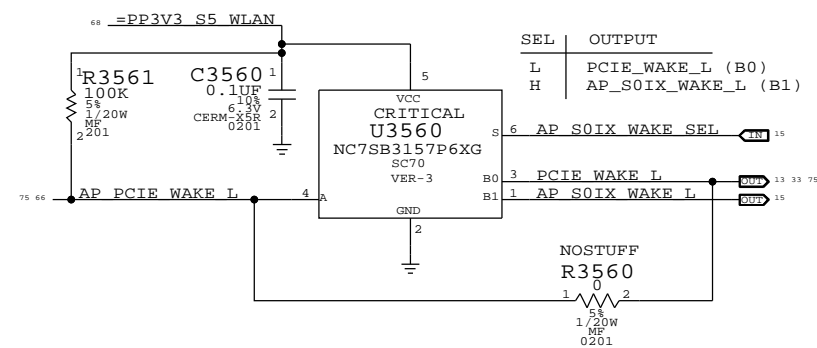


DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

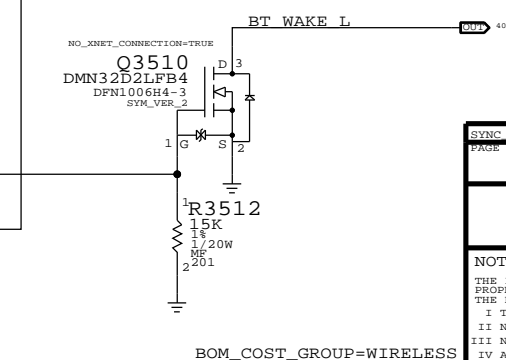
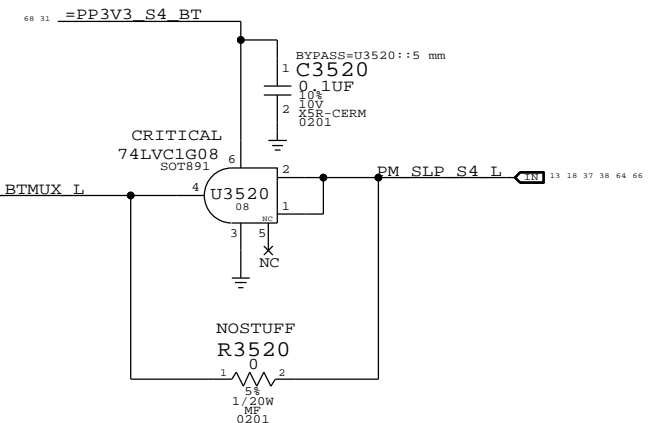
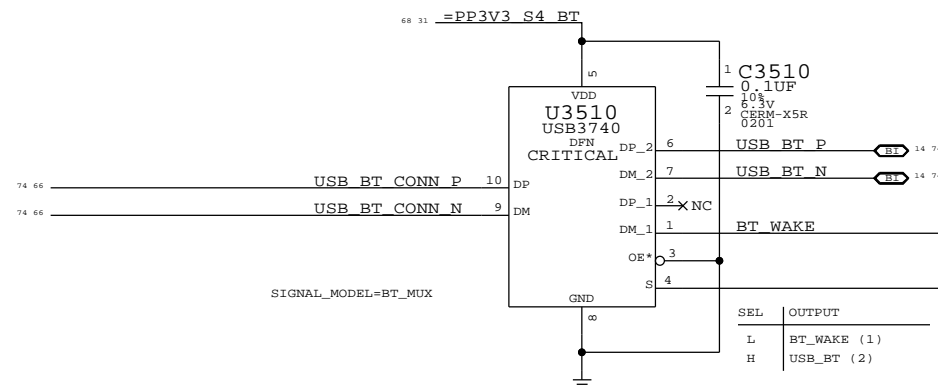
SYNC MASTER=T29 RR SYNC DATE=10/26/2012
PAGE TITLE
Thunderbolt Connector A
Apple Inc.
DRAWING NUMBER: 051-1573
REVISION: 8.0.0
BRANCH: dvt1
PAGE: 32 OF 120
SHEET: 28 OF 82
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D
C
B
A

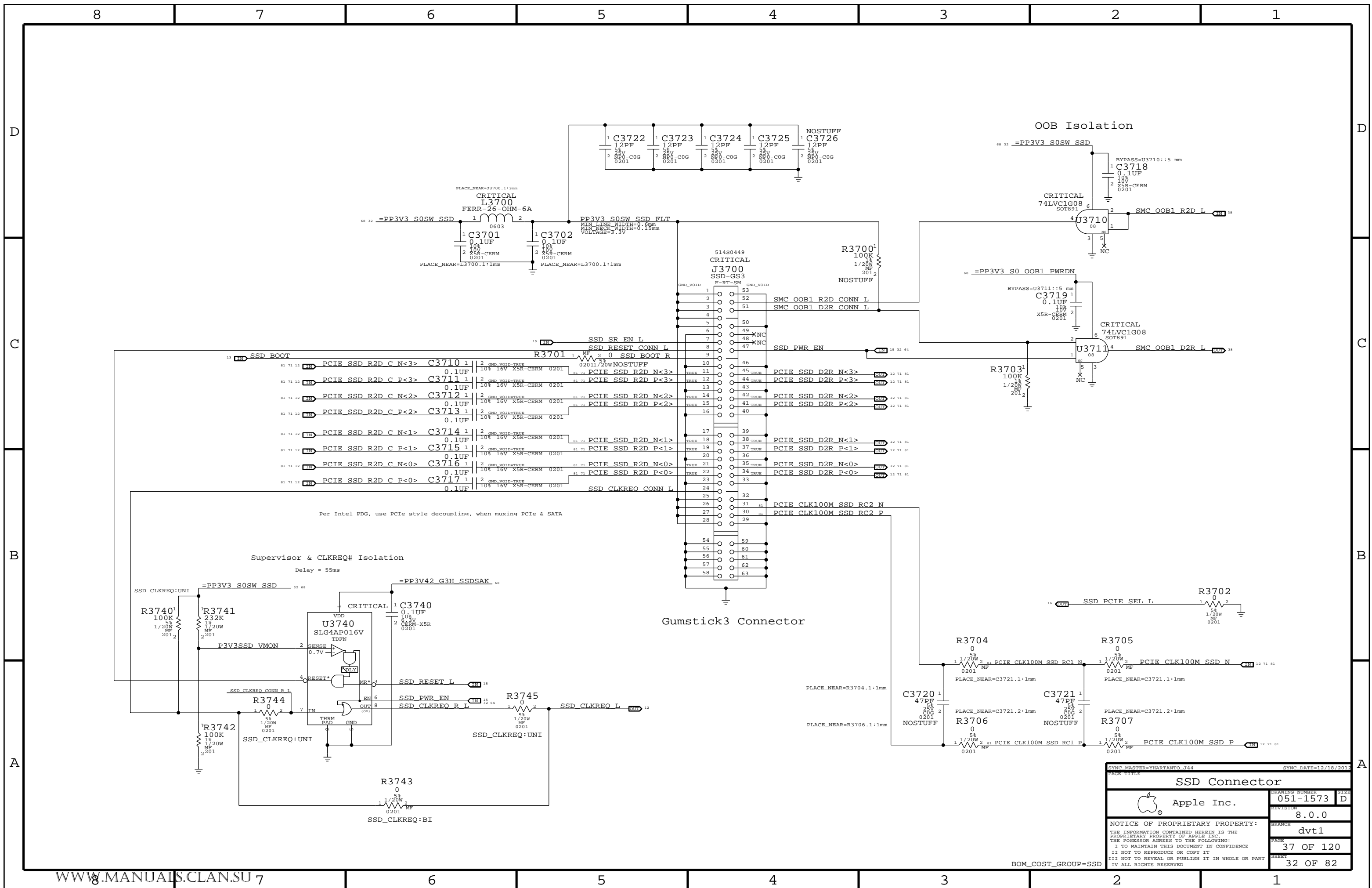
PCIe Wake Muxing



BLUETOOTH

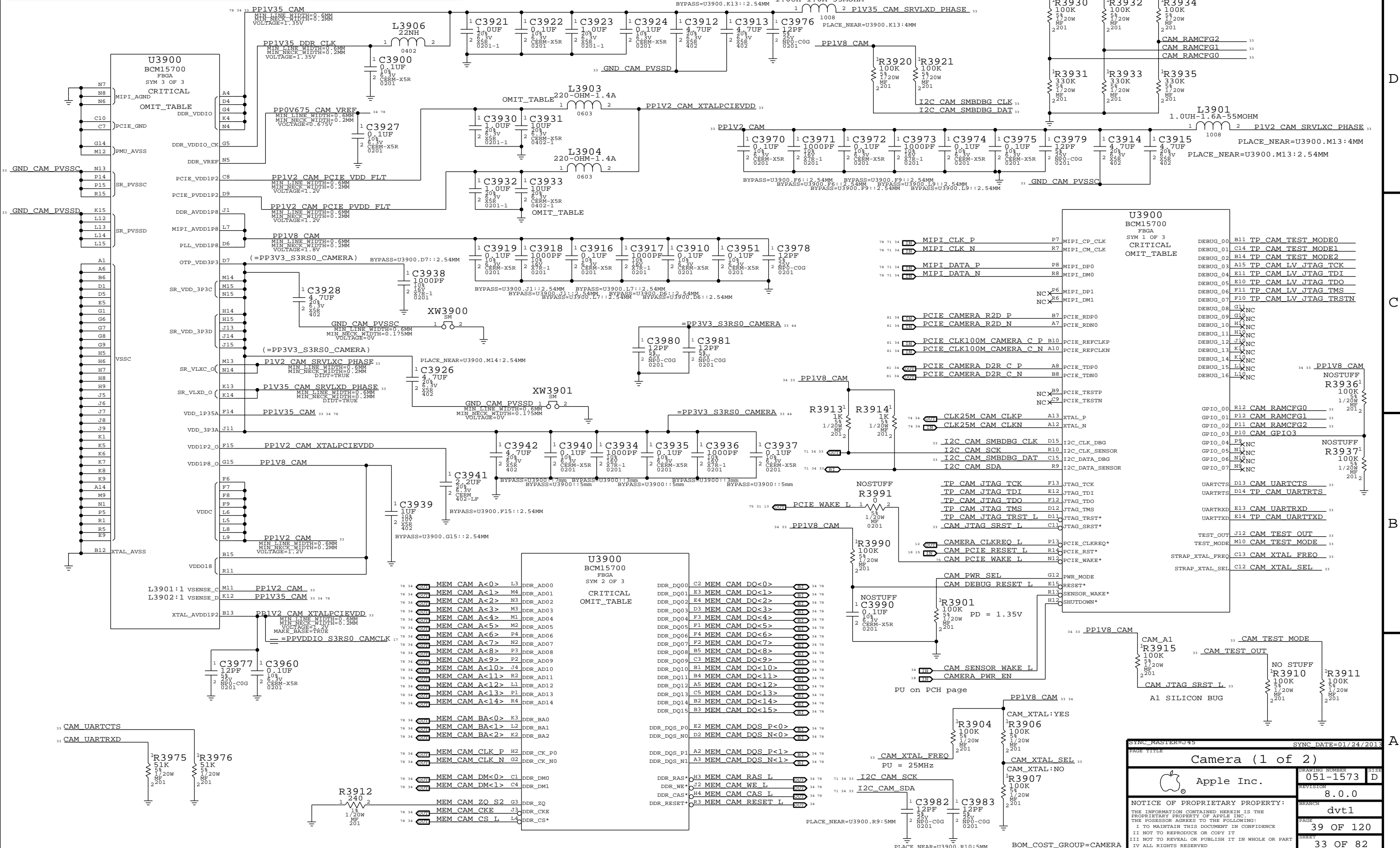


SYNC MASTER=141		SYNC DATE=11/01/2012	
PAGE TITLE			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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		PAGE	35 OF 120
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SYNC MASTER=YHARTANTO J44		SYNC DATE=12/18/2012	
PAGE TITLE			
SSD Connector		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
		REVISION	
		8.0.0	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	2	CAP_CER,10UF,20%,6.3V,MRZTL,0402	C3931,C3933	CRITICAL	



Camera (1 of 2)

Apple Inc.

051-1573

8.0.0

dvt1

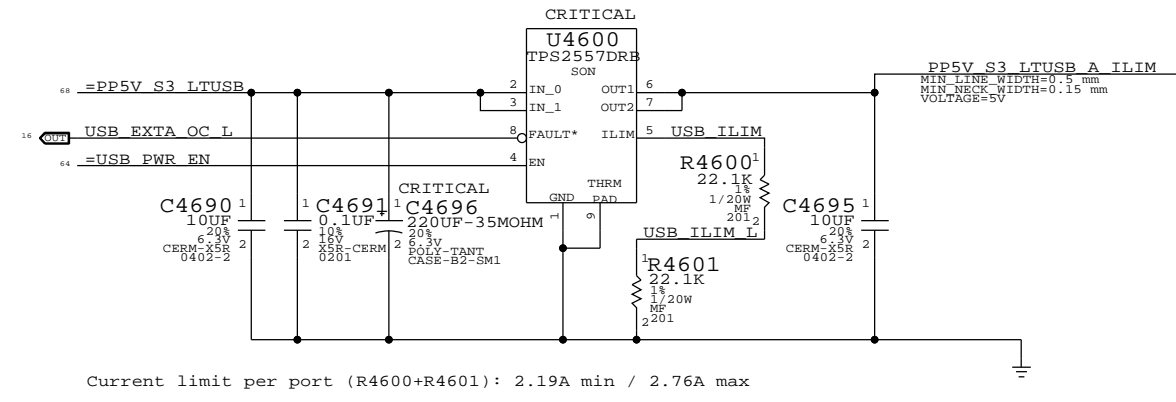
39 OF 120

33 OF 82

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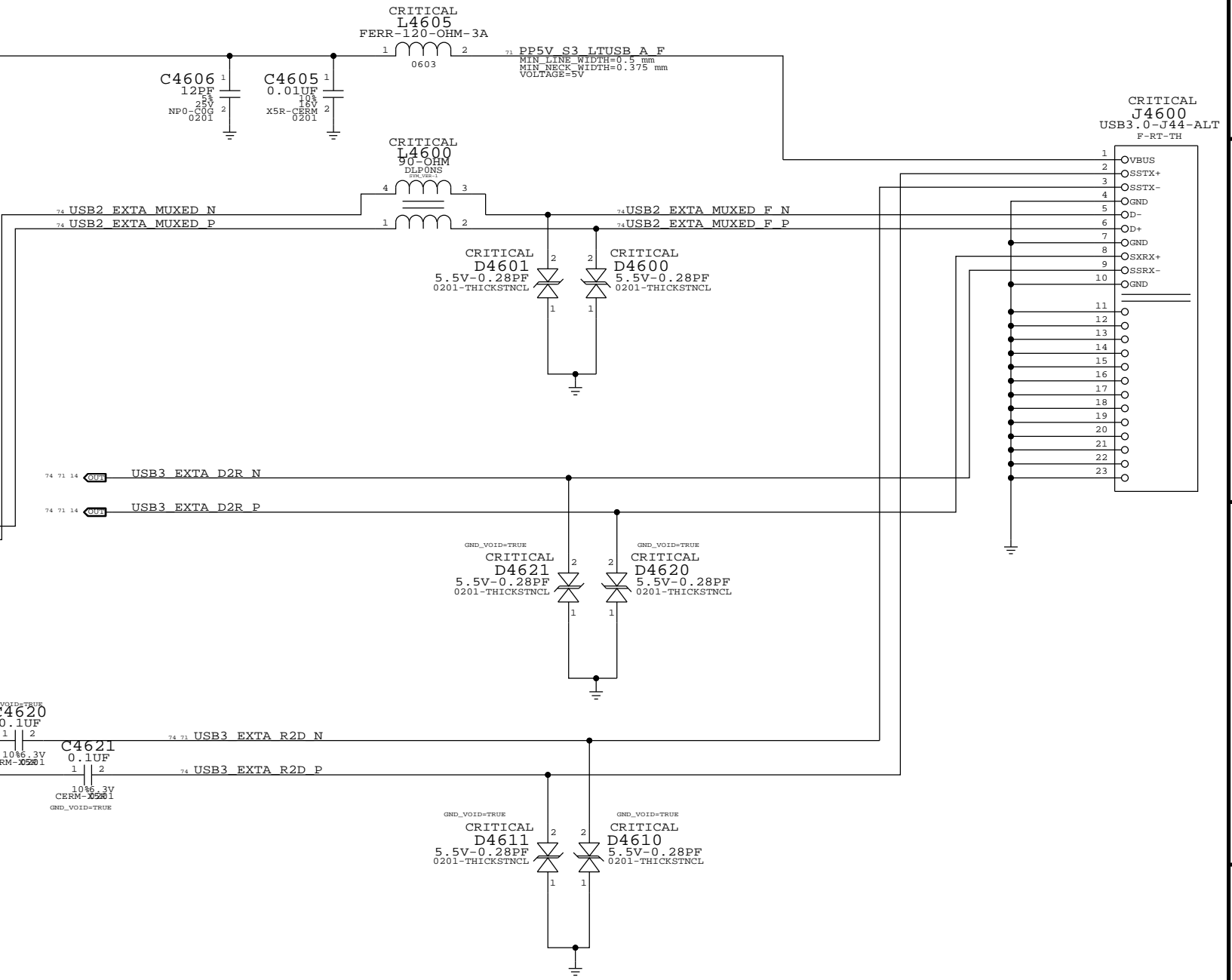
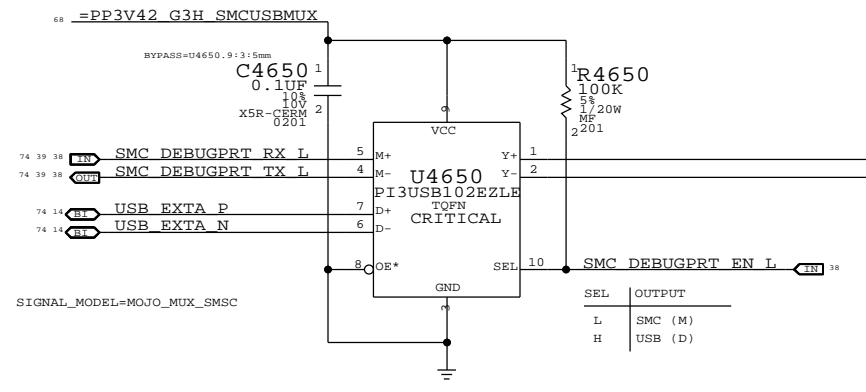
RIGHT USB PORT A

USB Port Power Switch



Mojo SMC Debug Mux

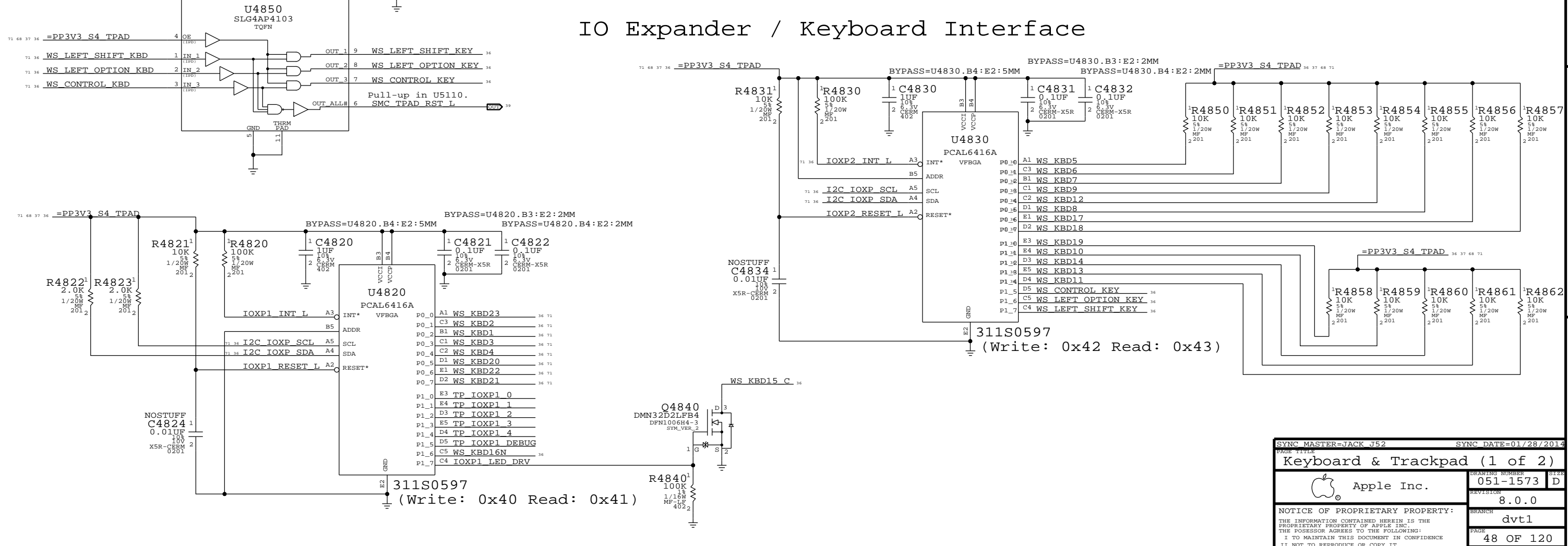
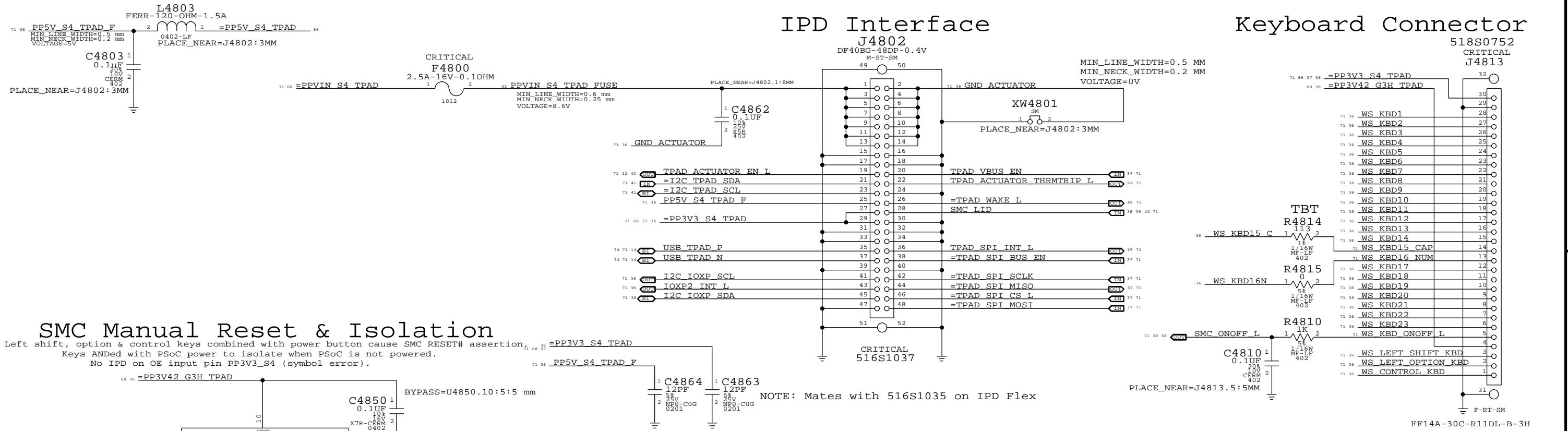
THE PI3USB102E CAN CLAMP VOLTAGE IN THE INTERNAL USB PINS



SYNC MASTER=J41		SYNC DATE=10/23/2012	
External A USB3 Connector			
Apple Inc.		DRAWING NUMBER	051-1573
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		PAGE	46 OF 120
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IPD Interface

Keyboard Connector



SYNC MASTER=JACK J52		SYNC DATE=01/28/2014	
Keyboard & Trackpad (1 of 2)			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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Keyboard Backlight Connector

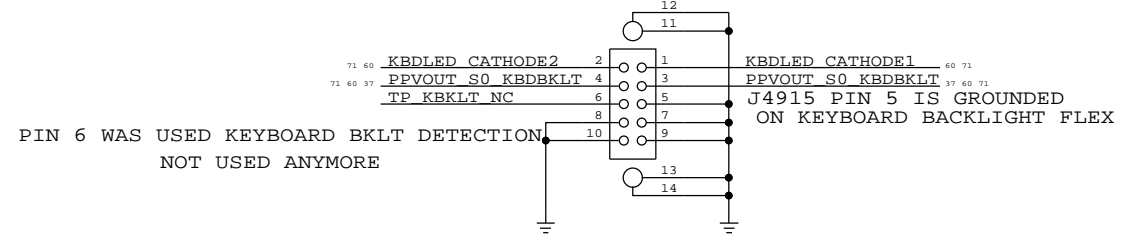
516S0899

CRITICAL

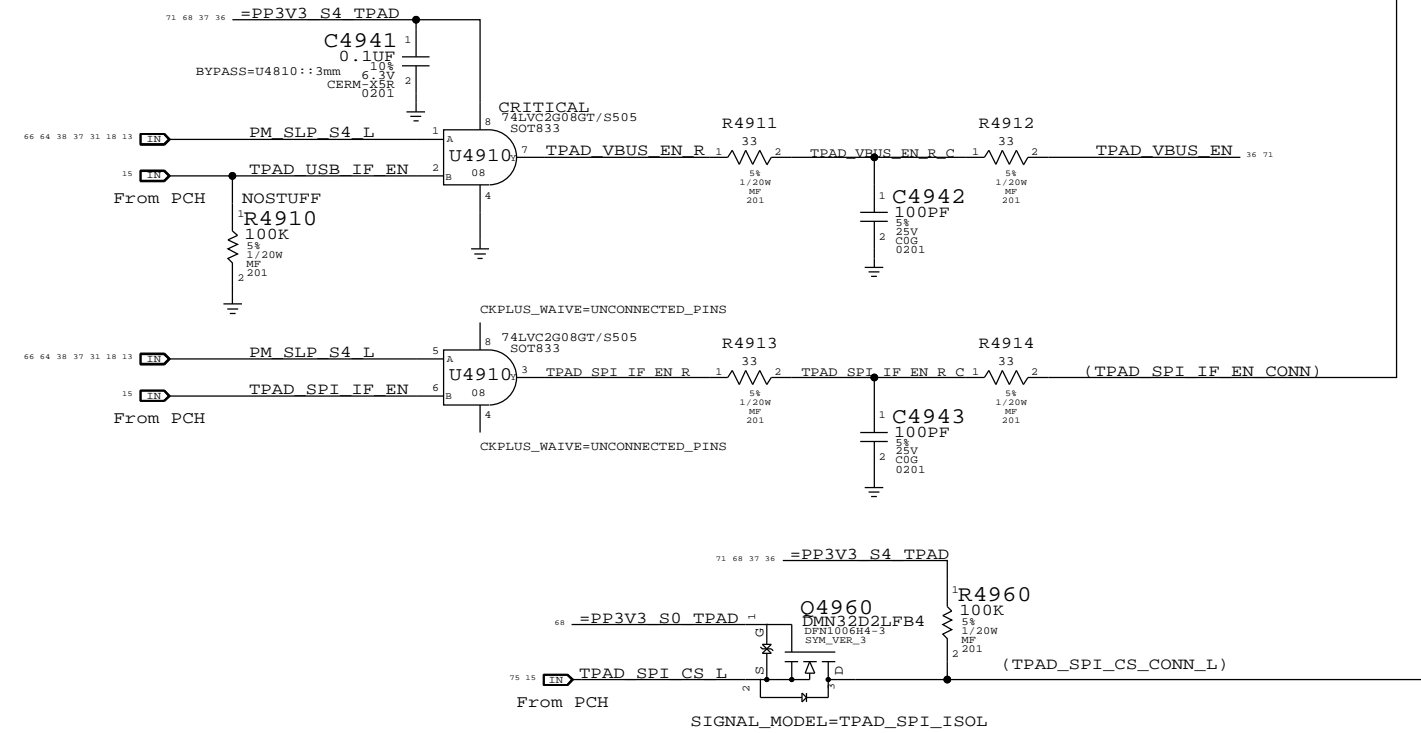
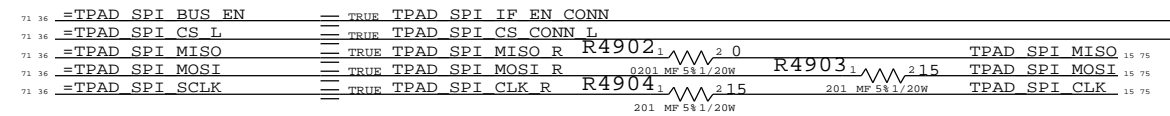
J4915

AA07A-S010-VA1

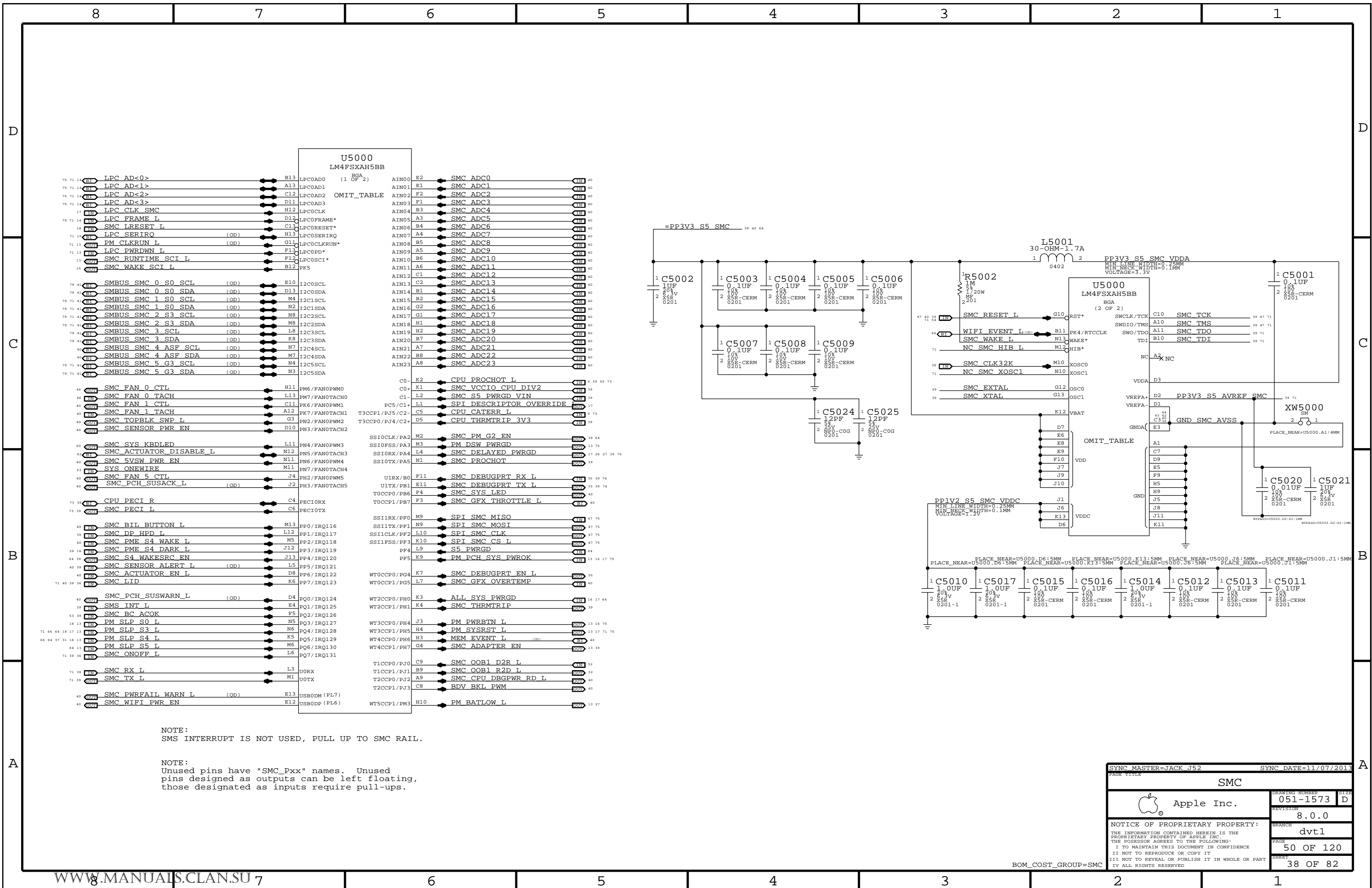
F-ST-SM



TPAD SPI WITH SRC TERMINATION



SYNC MASTER=JACK J5 SYNC DATE=01/31/2014		
PAGE TITLE Keyboard & Trackpad (2 of 2)		
Apple Inc.	DRAWING NUMBER 051-1573	SIZE D
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	SHEET 37 OF 82	

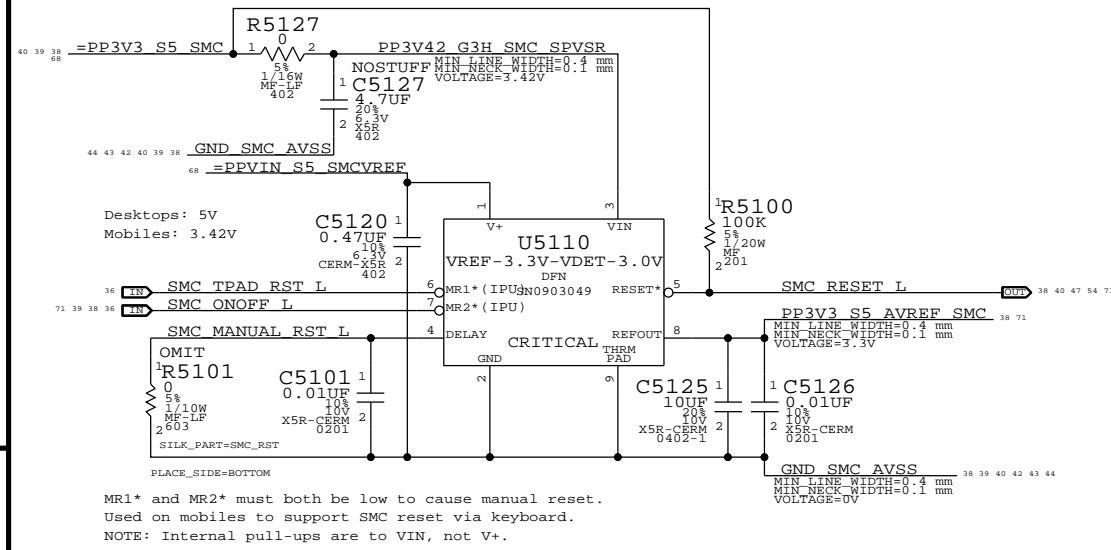


NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

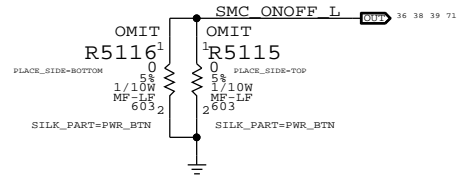
NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=JACK J52		SYNC DATE=11/07/2013	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
051-1573		051-1573	D
REVISION		8.0.0	
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SMC Reset "Button", Supervisor & AVREF Supply

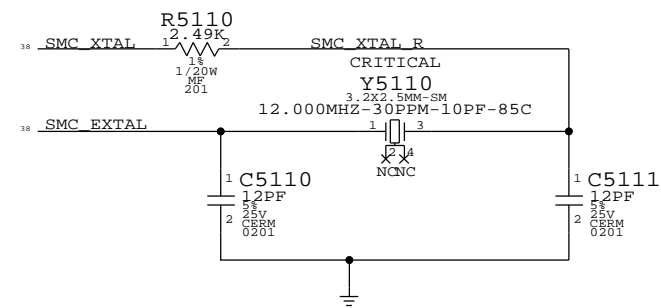


Debug Power "Buttons"

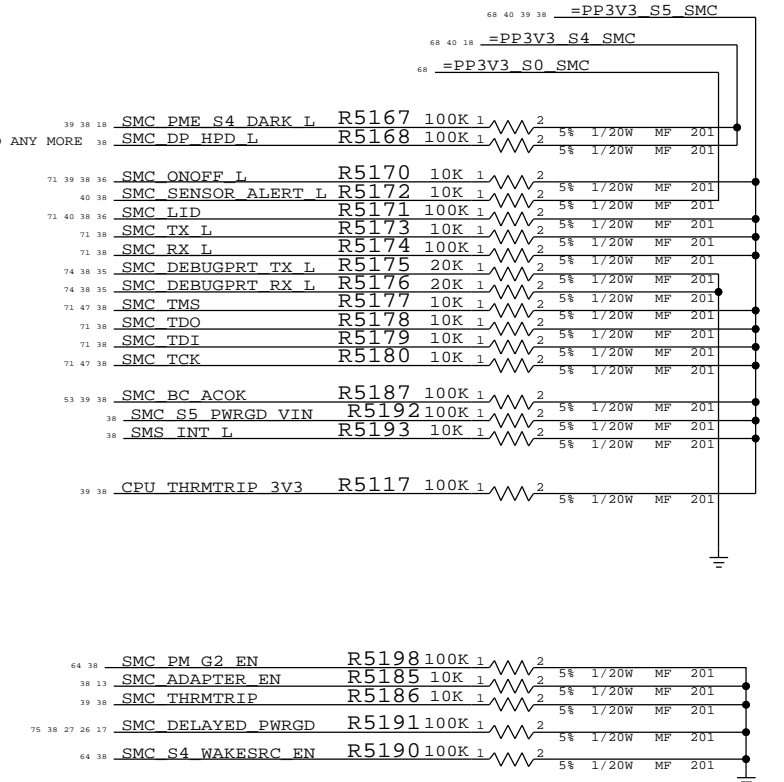
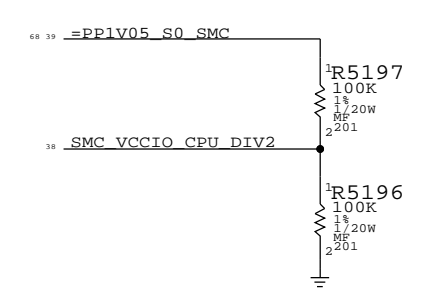
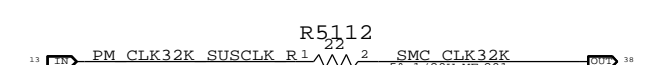
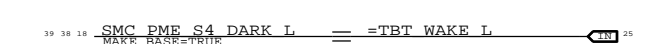
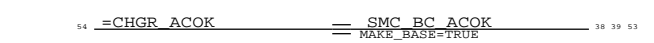
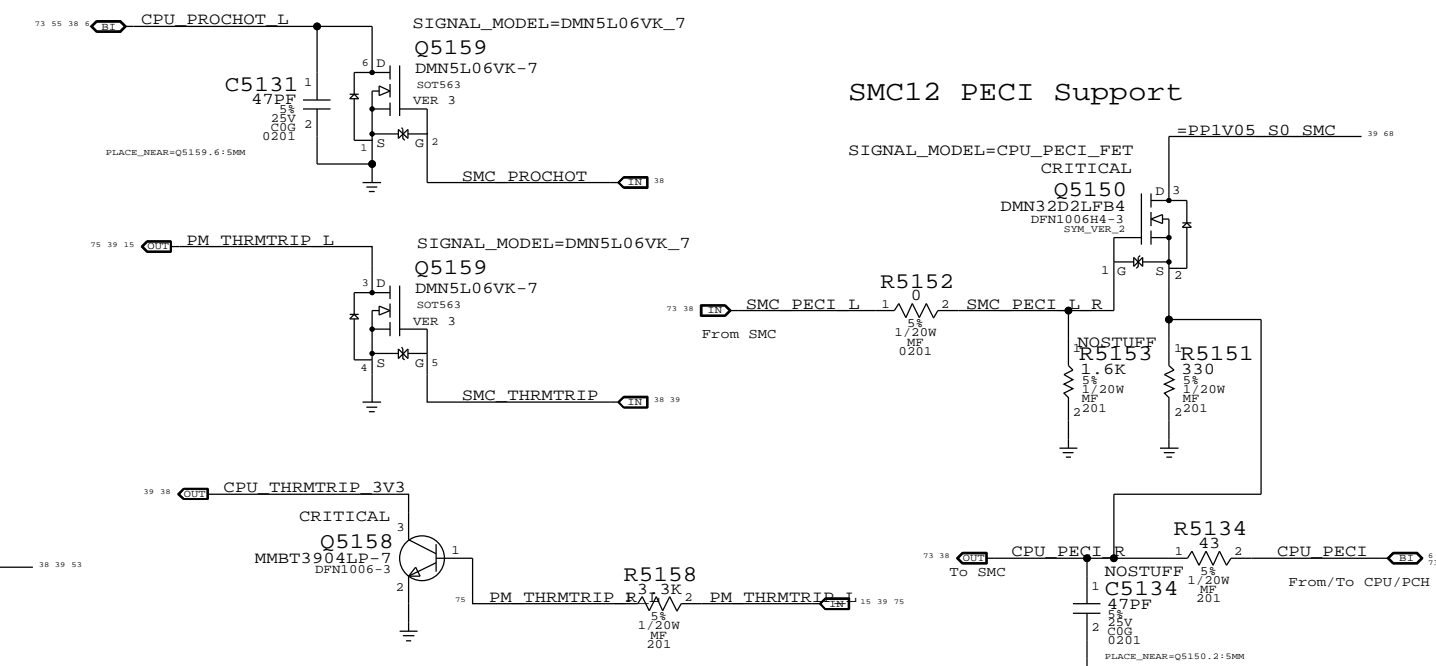


SMC Crystal Circuit

SMC USB Clock require these crystal values: 5, 6, 8, 10, 12, 16, 18, 20, 24, 25 Mhz



SMC12 PECCI Support



SYNC MASTER=JACK J52		SYNC DATE=10/24/2013	
SMC Shared Support			
Apple Inc.		DRAWING NUMBER	051-1573
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		BRANCH	dvt1
		PAGE	51 OF 120
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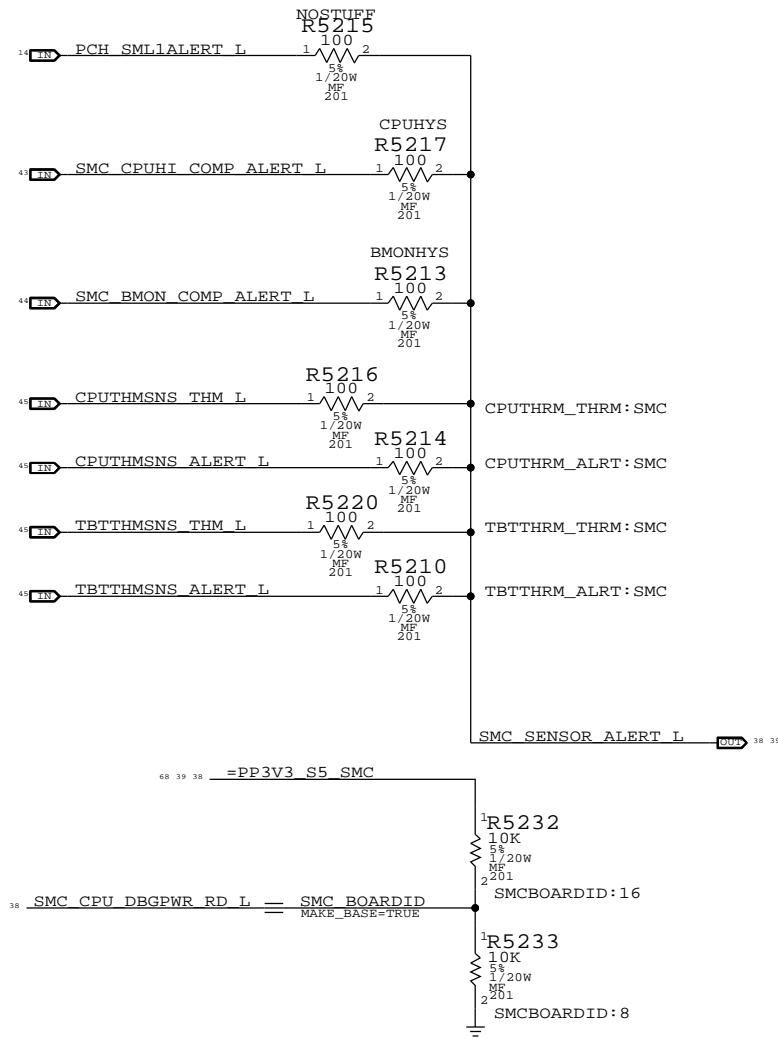
SMC12 ADC Assignments

SMC ADC0	SMC CPU HI ISENSE
SMC ADC1	SMC PBUS VSENSE
SMC ADC2	SMC_BMON ISENSE
SMC ADC3	SMC DCIN ISENSE
SMC ADC4	SMC DCIN VSENSE
SMC ADC5	SMC_BMON DISCRETE ISENSE
SMC ADC6	SMC CPU ISENSE
SMC ADC7	SMC_OTHER5V HI ISENSE
SMC ADC8	SMC_OTHER3V3 HI ISENSE
SMC ADC9	SMC_DDR ISENSE
SMC ADC10	SMC_LCDBKLT ISENSE
SMC ADC11	SMC_TPAD ISENSE
SMC ADC12	SMC_DDR1V8 ISENSE
SMC ADC13	SMC_SSD ISENSE
SMC ADC14	SMC_PP3V3S0 ISENSE
SMC ADC15	SMC_CAMERA ISENSE
SMC ADC16	SMC_TPAD VSENSE
SMC ADC17	SMC_PP5V50 ISENSE
SMC ADC18	SMC_CPUDD ISENSE
SMC ADC19	SMC_PCH ISENSE
SMC ADC20	SMC_CPU VSENSE
SMC ADC21	SMC_LCDPANEL ISENSE
SMC ADC22	SMC_CPU IMON ISENSE
SMC ADC23	SMC_TBT ISENSE

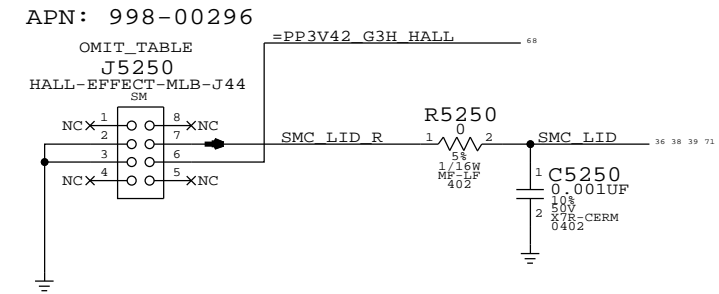
SMC12 Pin Assignments

SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA
BDV_BKL_PWM	NC_SMC_TPAD_BOOST_DISABLE_L
SMC_SYS_LED	NC_SMC_SYS_LED
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH
SMC_5VSW_PWR_EN	NC_SMC_5VSW_PWR_EN
SMC_FAN_5_CTL	NC_SMC_FAN_5_CTL
SMC_BIL_BUTTON_L	NC_SMC_BIL_BUTTON_L
MEM_EVENT_L	NC_MEM_EVENT_L
SMC_PWRFAIL_WARN_L	NC_SMC_PWRFAIL_WARN_L

Thermal Alerts



Hall Effect Pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-01216	1	SUBASSY,PCBA,HALL EFFECT,X304	J5250	CRITICAL	
639-00525 (PCBA,HALL EFFECT,X304) REPORTS TO 677-01216					

Specify one of these BOM GROUPS.

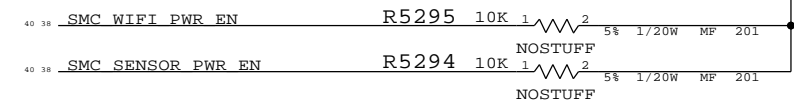
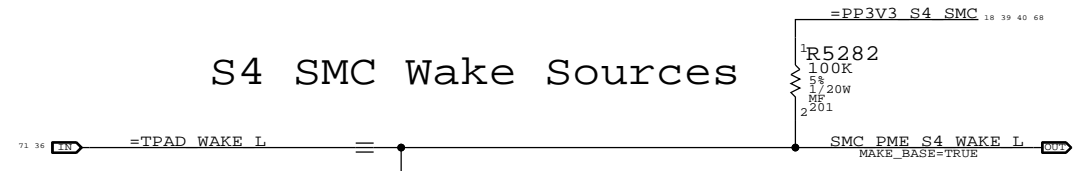
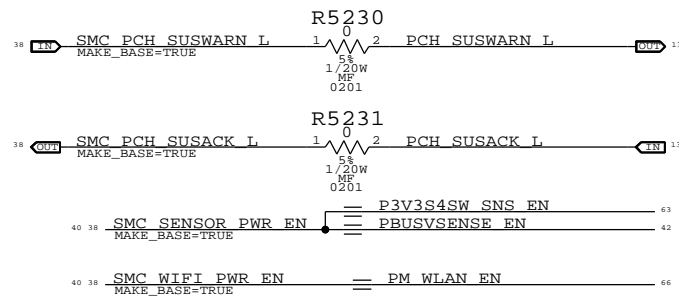
BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALERT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALERT:PU
CPUTHRM:ALRT	CPUTHRM_THRM:PU,CPUTHRM_ALERT:SMC
CPUTHRM:NONE	CPUTHRM_THRM:PU,CPUTHRM_ALERT:PU

Specify one of these BOM GROUPS.

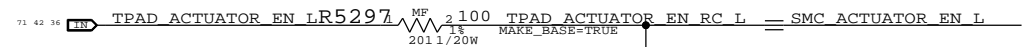
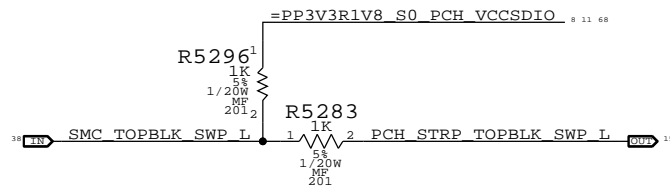
BOM GROUP	BOM OPTIONS
TBTHRM:BOTH	TBTHRM_THRM:SMC,TBTHRM_ALERT:SMC
TBTHRM:THRM	TBTHRM_THRM:SMC,TBTHRM_ALERT:PU
TBTHRM:ALRT	TBTHRM_THRM:PU,TBTHRM_ALERT:SMC
TBTHRM:NONE	TBTHRM_THRM:PU,TBTHRM_ALERT:PU

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

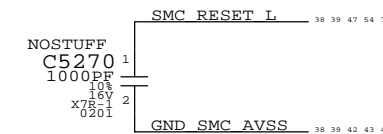
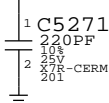
S4 SMC Wake Sources



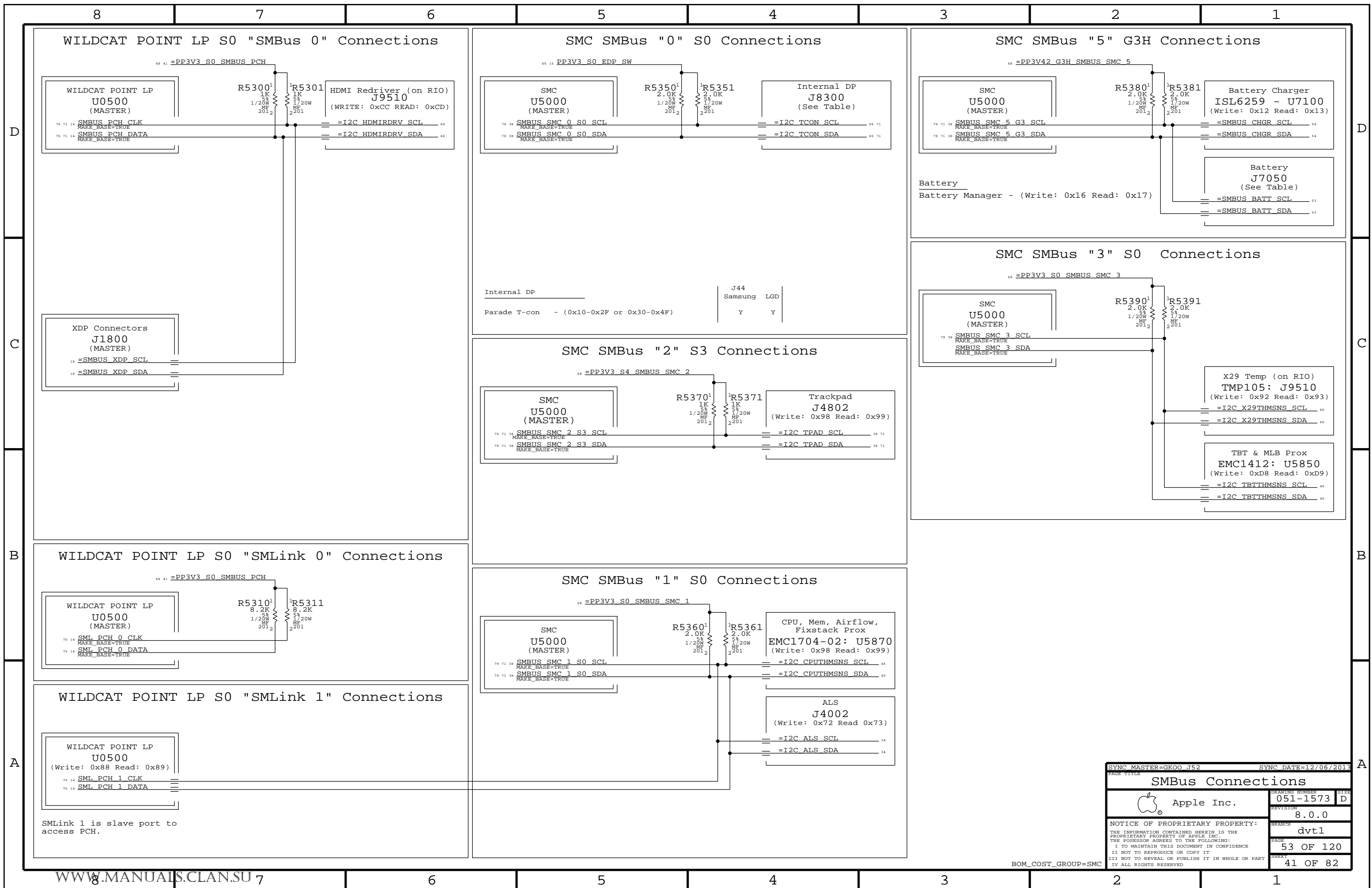
Top Block Swap



RC Placeholder to filter noise on this signal towards SMC IO.



PAGE TITLE		DRAWING NUMBER	SIZE
SMC Project Support		051-1573	D
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WILDCAT POINT LP S0 "SMBus 0" Connections

SMC SMBus "0" S0 Connections

SMC SMBus "5" G3H Connections

SMC SMBus "3" S0 Connections

SMC SMBus "2" S3 Connections

WILDCAT POINT LP S0 "SMLink 0" Connections

SMC SMBus "1" S0 Connections

WILDCAT POINT LP S0 "SMLink 1" Connections

SYNC MASTER=GK00 J52		SYNC DATE=12/06/2013	
SMBus Connections			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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		PAGE	53 OF 120
		SHEET	41 OF 82

D

D

C

C

B

B

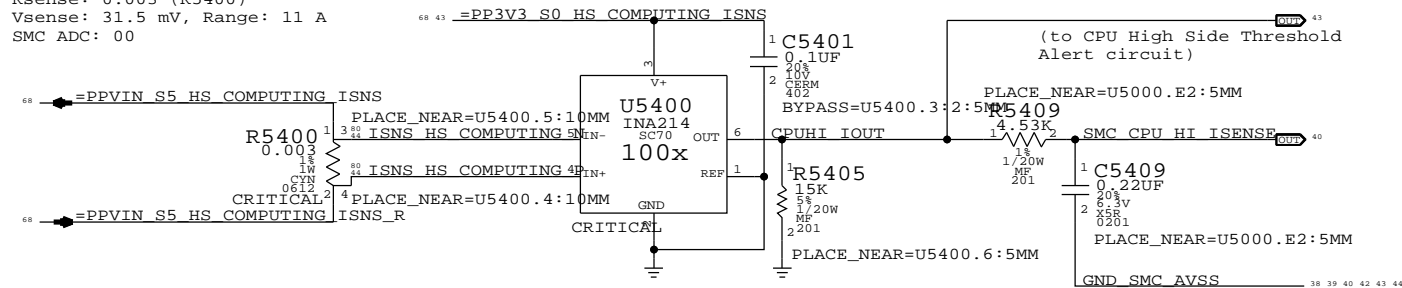
A

A

SMLink 1 is slave port to access PCH.

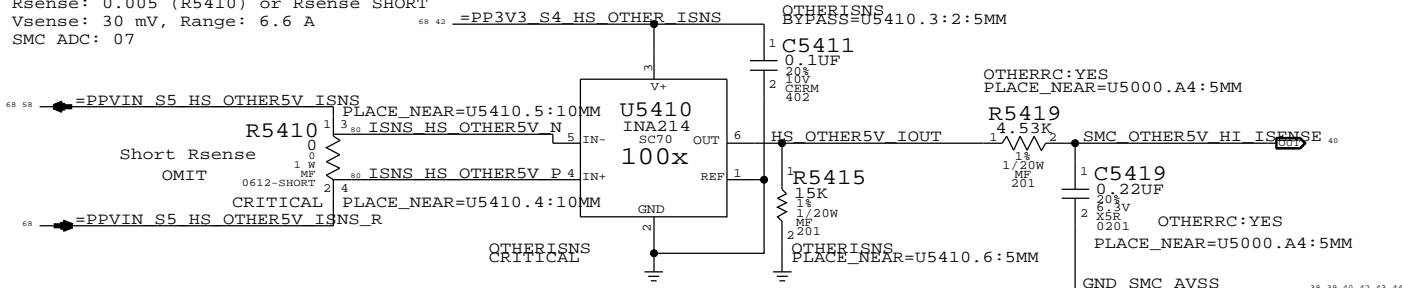
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 10.5 A
 Rsense: 0.003 (R5400)
 Vsense: 31.5 mV, Range: 11 A
 SMC ADC: 00



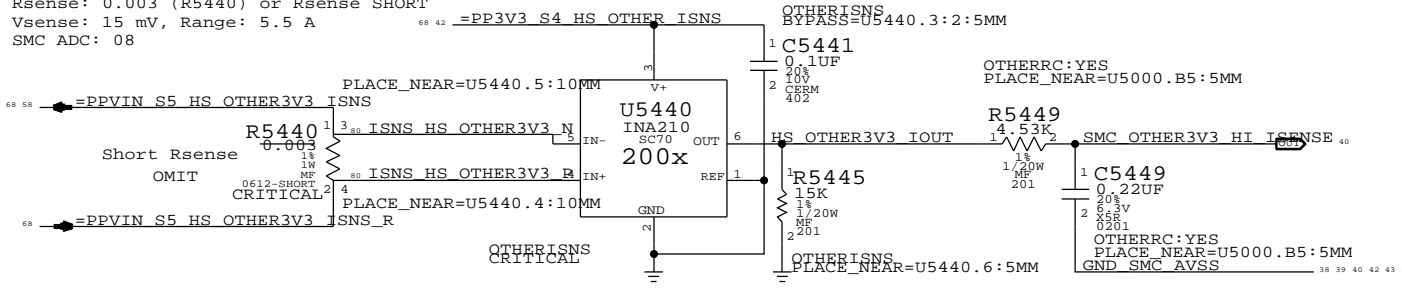
OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 6 A
 Rsense: 0.005 (R5410) or Rsense SHORT
 Vsense: 30 mV, Range: 6.6 A
 SMC ADC: 07



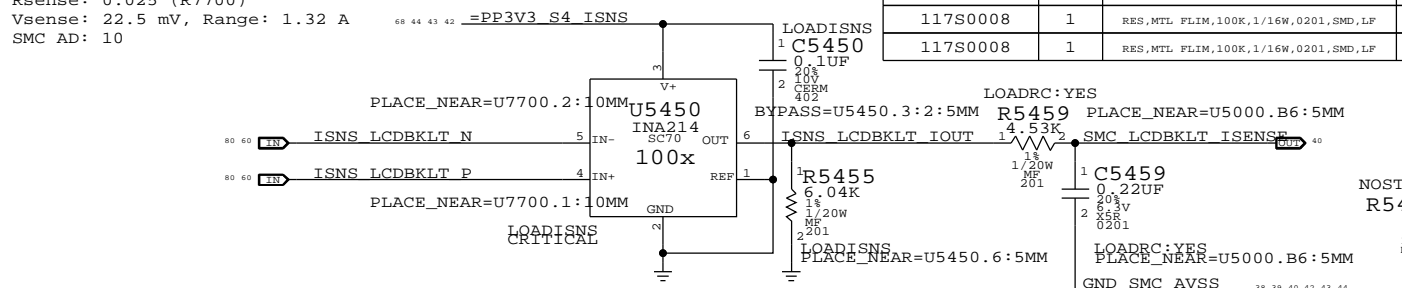
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 5 A
 Rsense: 0.003 (R5440) or Rsense SHORT
 Vsense: 15 mV, Range: 5.5 A
 SMC ADC: 08



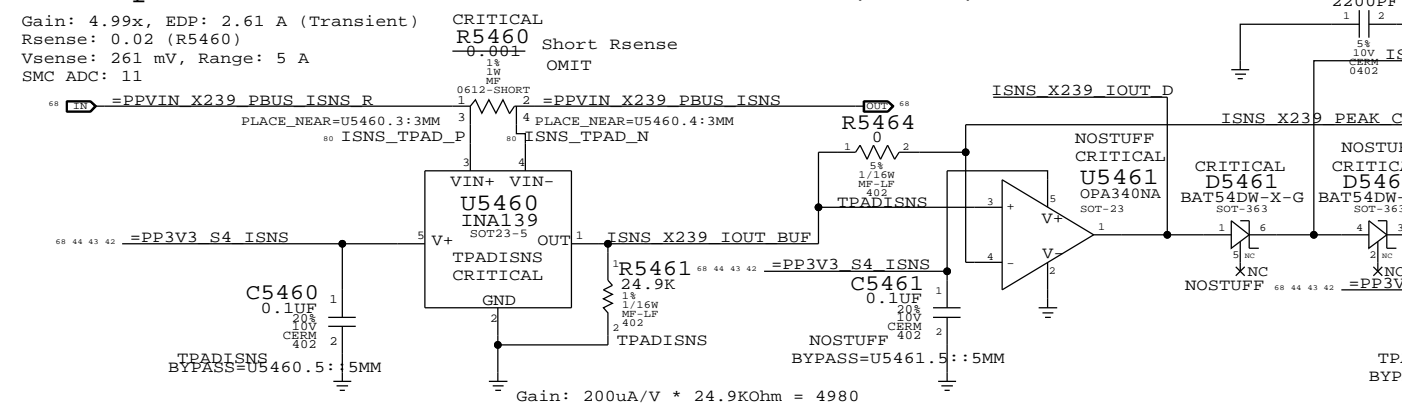
LCD Backlight Current Sense (IBLC)

Gain: 100x, EDP: 0.9 A
 Rsense: 0.025 (R7700)
 Vsense: 22.5 mV, Range: 1.32 A
 SMC AD: 10



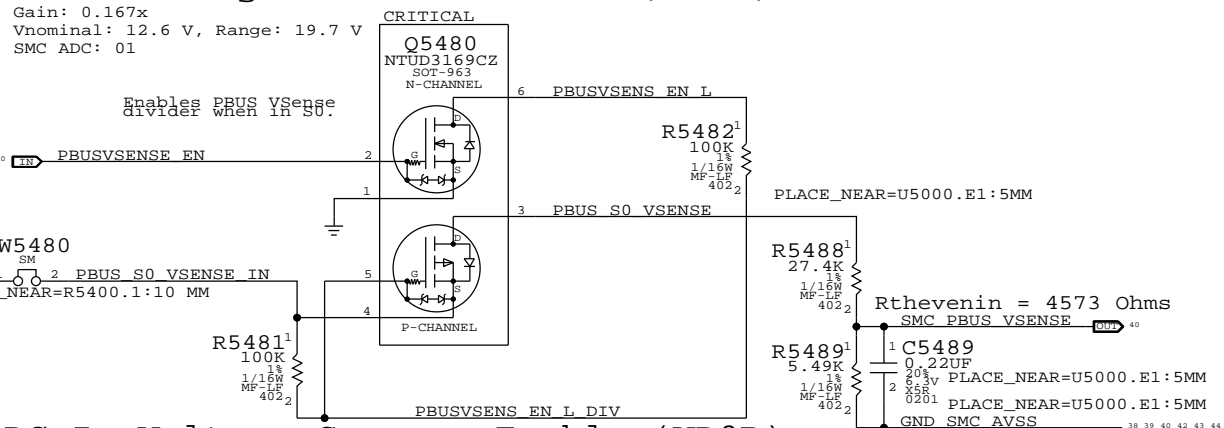
Trackpad Actuator X239 Current Sense (ITPC)

Gain: 4.99x, EDP: 2.61 A (Transient)
 Rsense: 0.02 (R5460)
 Vsense: 261 mV, Range: 5 A
 SMC ADC: 11



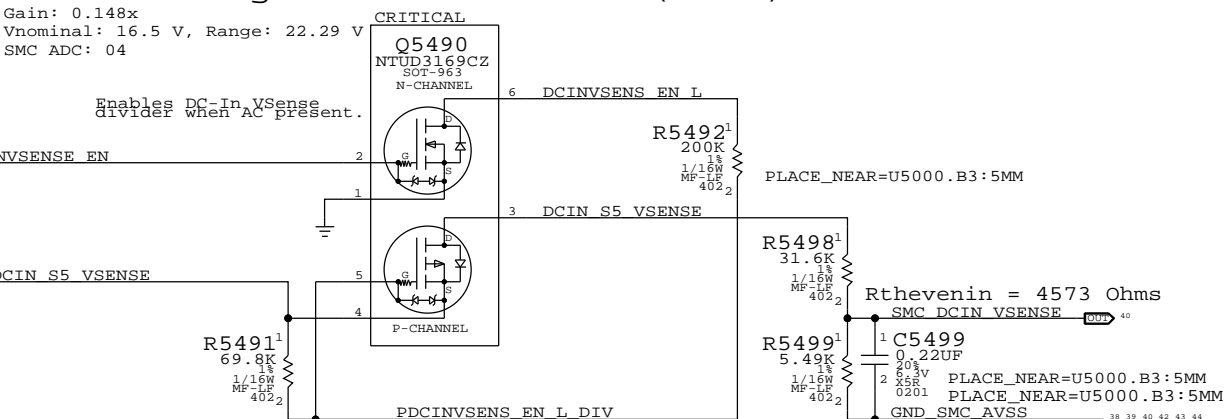
PBUS Voltage Sense & Enable (VPUR)

Gain: 0.167x
 Vnominal: 12.6 V, Range: 19.7 V
 SMC ADC: 01



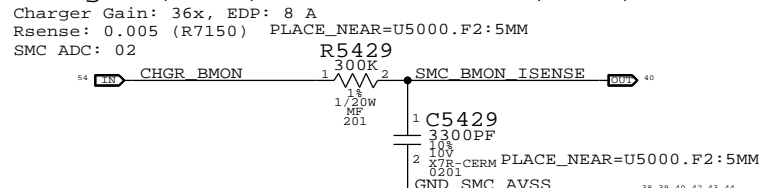
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
 Vnominal: 16.5 V, Range: 22.29 V
 SMC ADC: 04



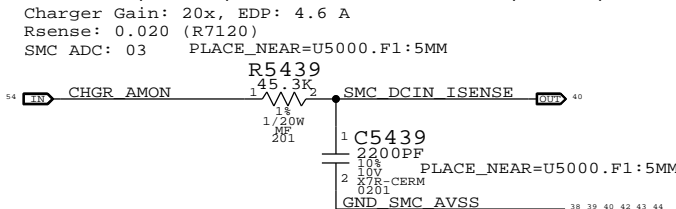
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
 Rsense: 0.005 (R7150) PLACE_NEAR=U5000.F2:5MM
 SMC ADC: 02



DC-IN (AMON) Current Sense (ID0R)

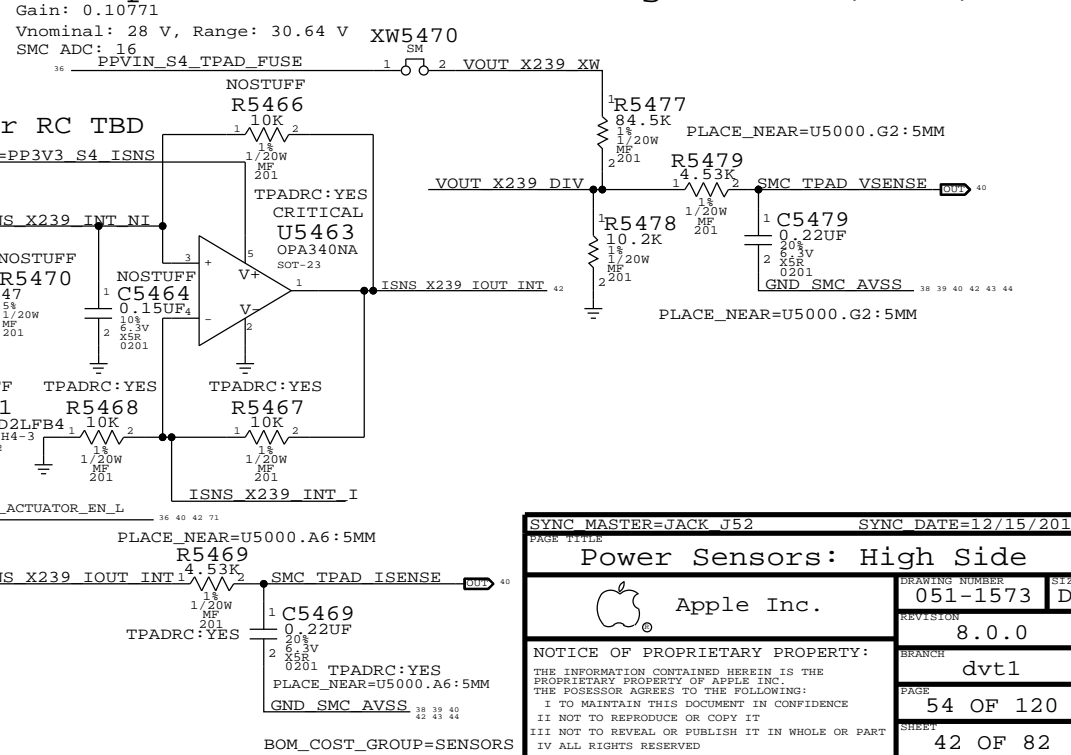
Charger Gain: 20x, EDP: 4.6 A
 Rsense: 0.020 (R7120)
 SMC ADC: 03 PLACE_NEAR=U5000.F1:5MM



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

Trackpad Actuator X239 Voltage Sense (VTPC)

Gain: 0.10771
 Vnominal: 28 V, Range: 30.64 V XW5470
 SMC ADC: 16
 PLACE_NEAR=U5000.G2:5MM



SYNC MASTER=JACK J52 SYNC DATE=12/15/2013

Power Sensors: High Side

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 54 OF 120

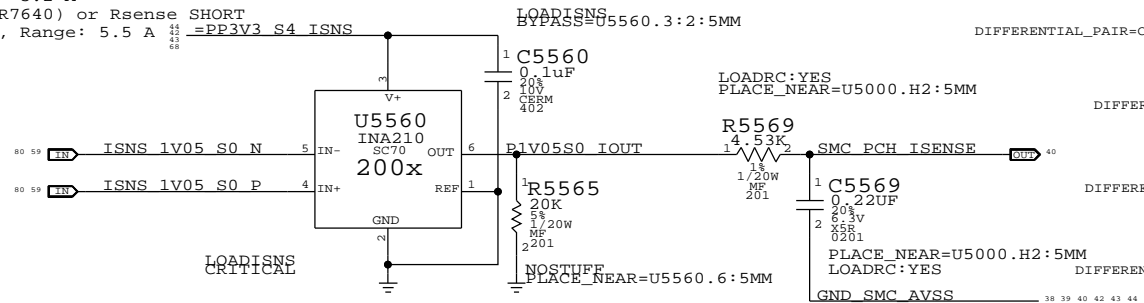
SHEET: 42 OF 82

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BOM_COST_GROUP=SENSORS

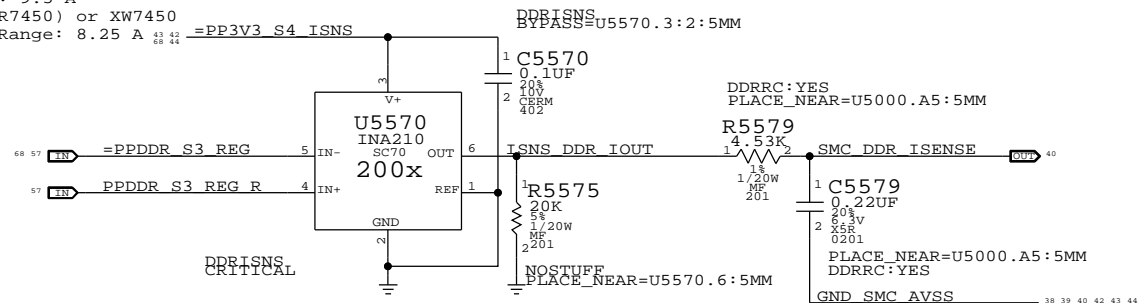
PCH 1.05V Current Sense (IC1C)

Gain: 200x, EDP: 5.2 A
 Rsense: 0.003 (R7640) or Rsense SHORT
 Vsense: 15.6 mV, Range: 5.5 A
 SMC ADC: 19



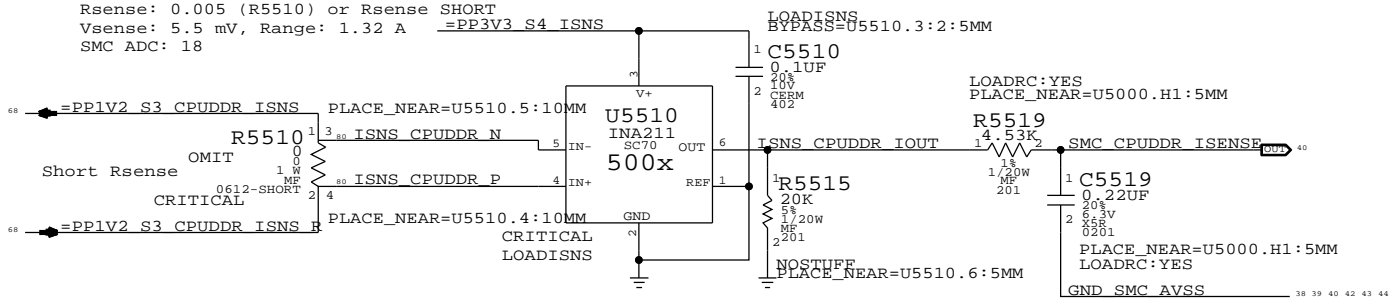
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 200x, EDP: 9.5 A
 Rsense: 0.002 (R7450) or XW7450
 Vsense: 19 mV, Range: 8.25 A
 SMC ADC: 09



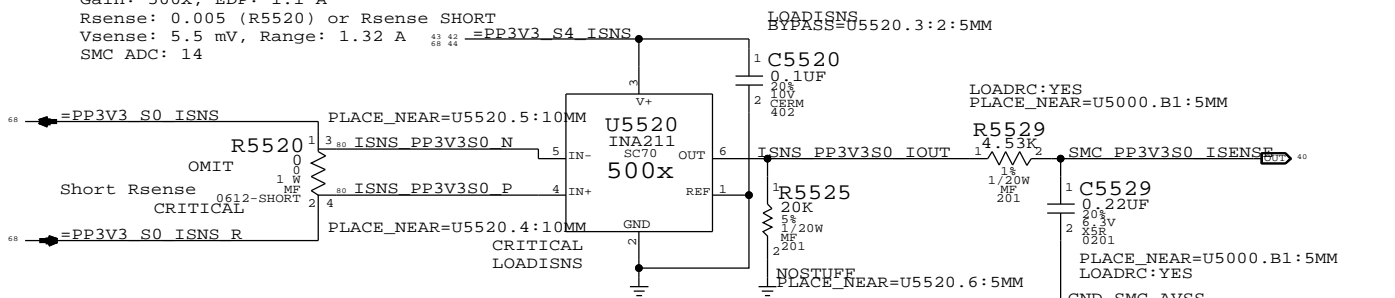
CPU DDR 1.2V S3 (CPU Only) Current Sense (IM1C)

Gain: 500x, EDP: 1.1 A
 Rsense: 0.005 (R5510) or Rsense SHORT
 Vsense: 5.5 mV, Range: 1.32 A
 SMC ADC: 18



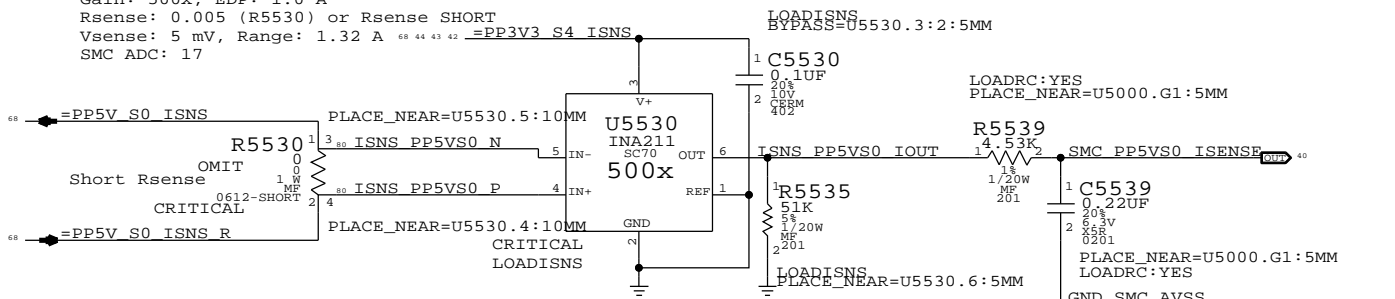
3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.1 A
 Rsense: 0.005 (R5520) or Rsense SHORT
 Vsense: 5.5 mV, Range: 1.32 A
 SMC ADC: 14



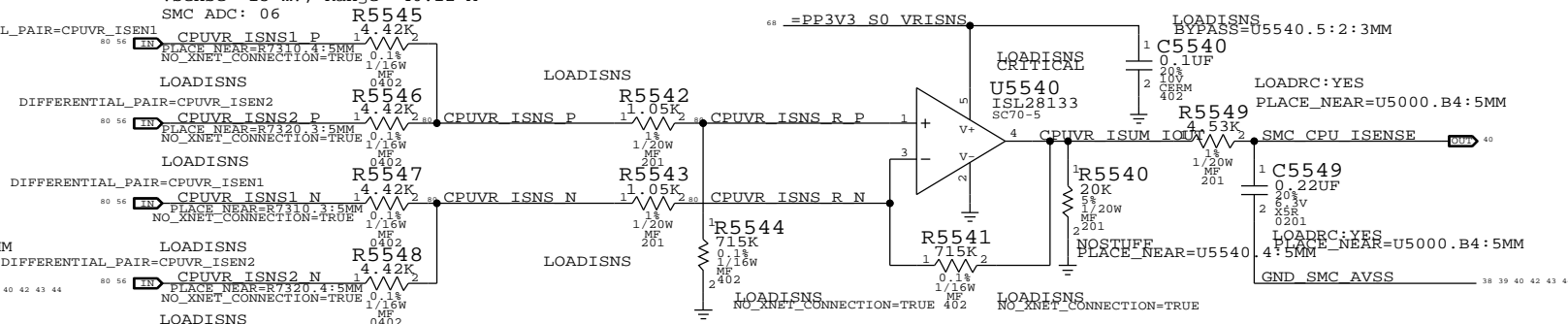
5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A
 Rsense: 0.005 (R5530) or Rsense SHORT
 Vsense: 5 mV, Range: 1.32 A
 SMC ADC: 17



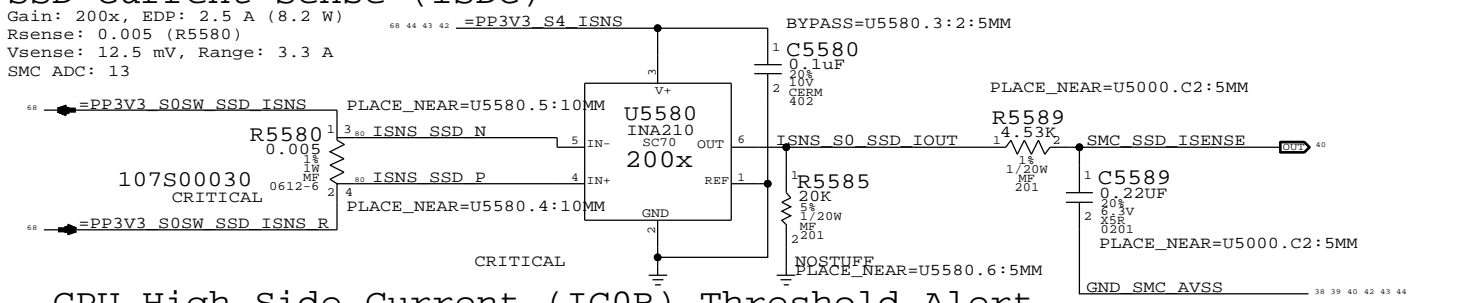
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
 Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
 Vsense: 15 mV, Range: 40.12 A
 SMC ADC: 06



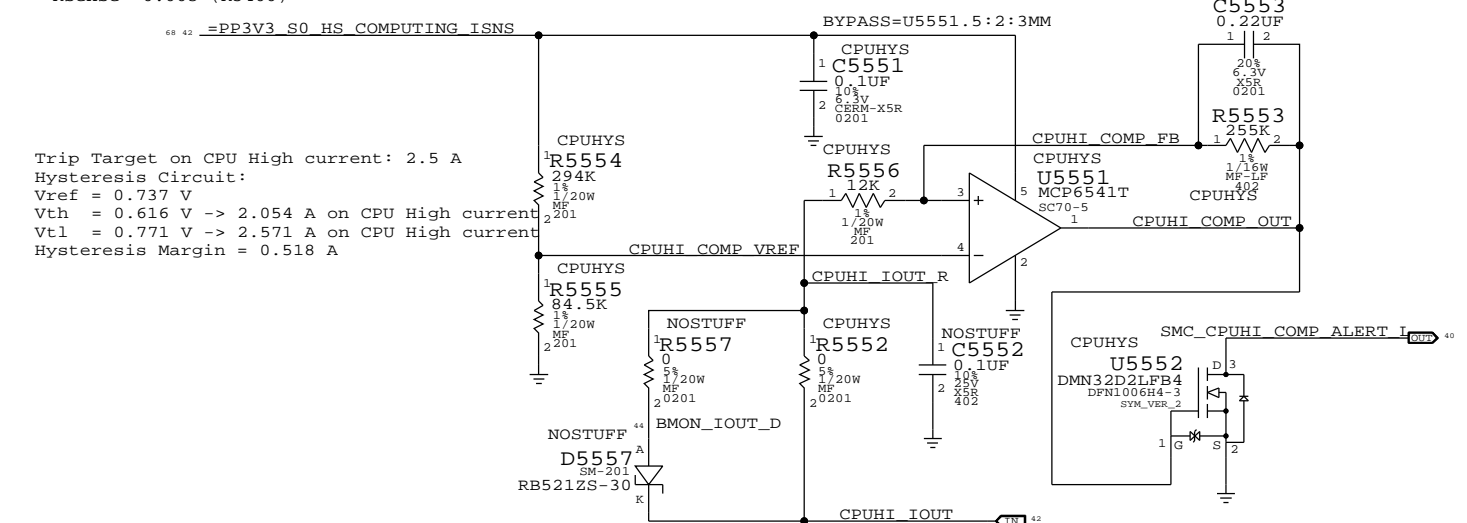
SSD Current Sense (ISDC)

Gain: 200x, EDP: 2.5 A (8.2 W)
 Rsense: 0.005 (R5580)
 Vsense: 12.5 mV, Range: 3.3 A
 SMC ADC: 13



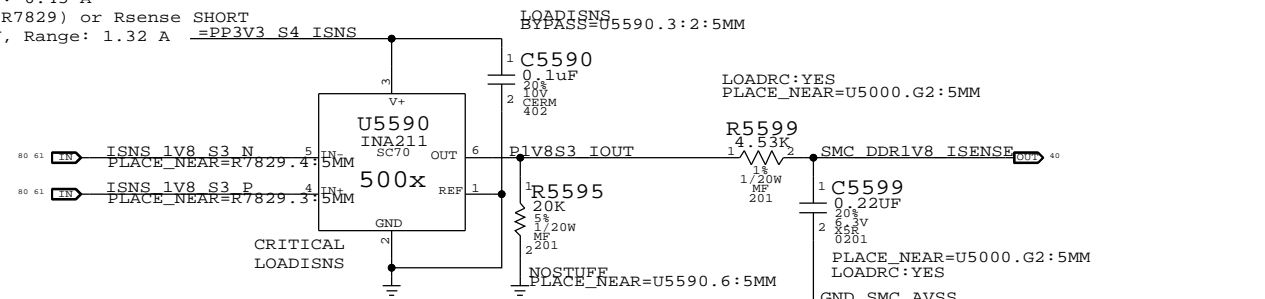
CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
 Rsense: 0.003 (R5400)



DDR 1.8V Current Sense (IM2C)

Gain: 500x, EDP: 0.45 A
 Rsense: 0.005 (R7829) or Rsense SHORT
 Vsense: 2.25 mV, Range: 1.32 A
 SMC ADC: 12



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519,C5599		LOADRC:NO
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

SYNC MASTER=JACK J52 SYNC DATE=12/06/2013

Power Sensors: Load Side

Apple Inc.

051-1573 D

REVISION 8.0.0

BRANCH dvt1

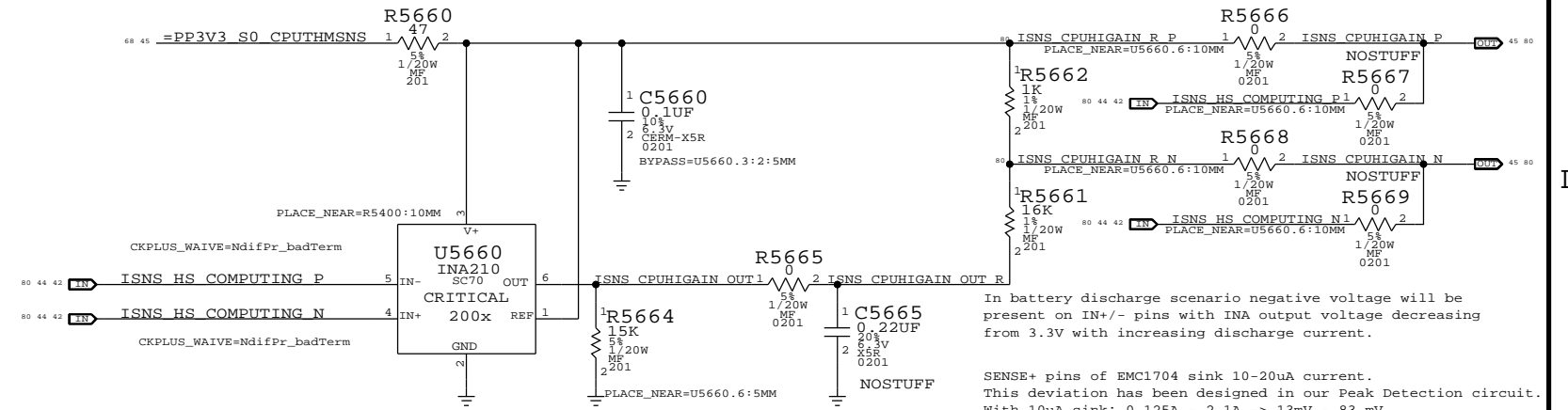
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BOM_COST_GROUP=SENSORS

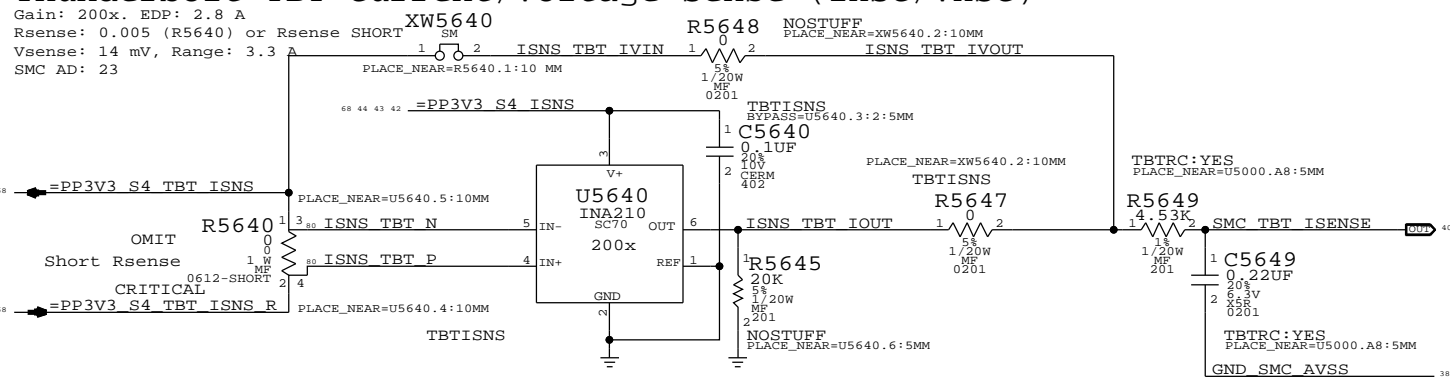
CPU High Side (IC0R) Peak Detection Support



In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

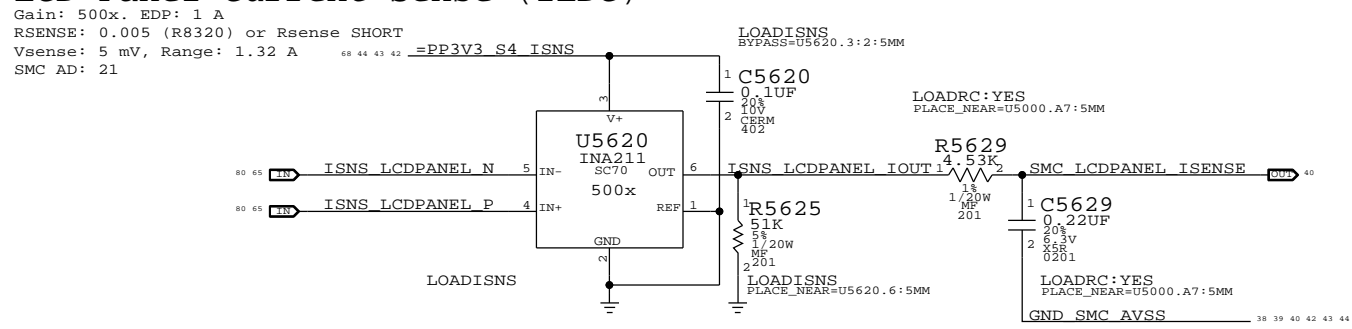
SENSE+ pins of EMC1704 sink 10-20uA current. This deviation has been designed in our Peak Detection circuit. With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)



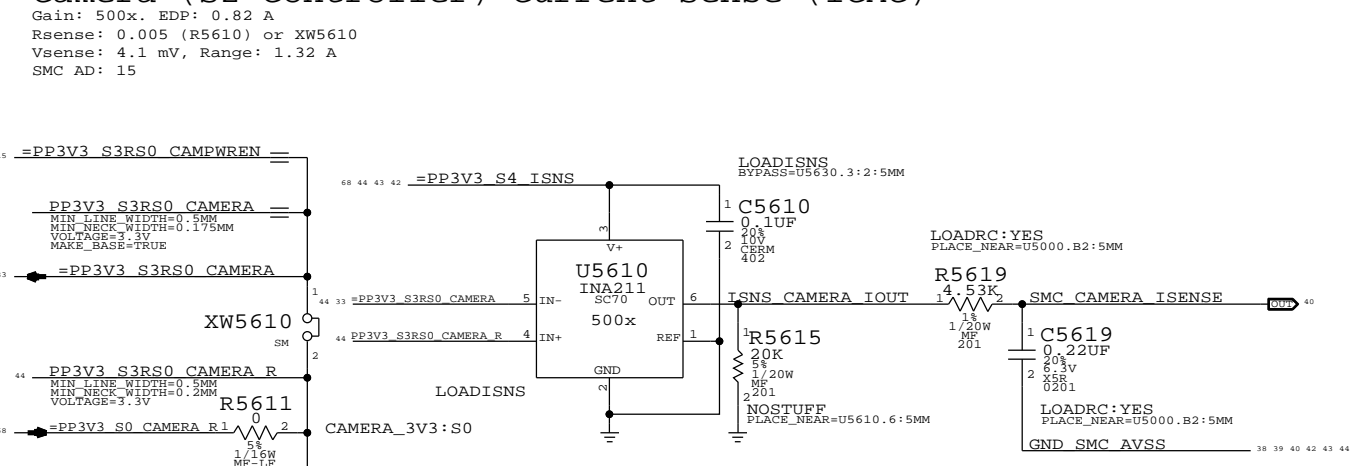
Gain: 200x. EDP: 2.8 A
Rsense: 0.005 (R5640) or Rsense SHORT
Vsense: 14 mV, Range: 3.3 A
SMC AD: 23

LCD Panel Current Sense (ILDC)



Gain: 500x. EDP: 1 A
RSENSE: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC AD: 21

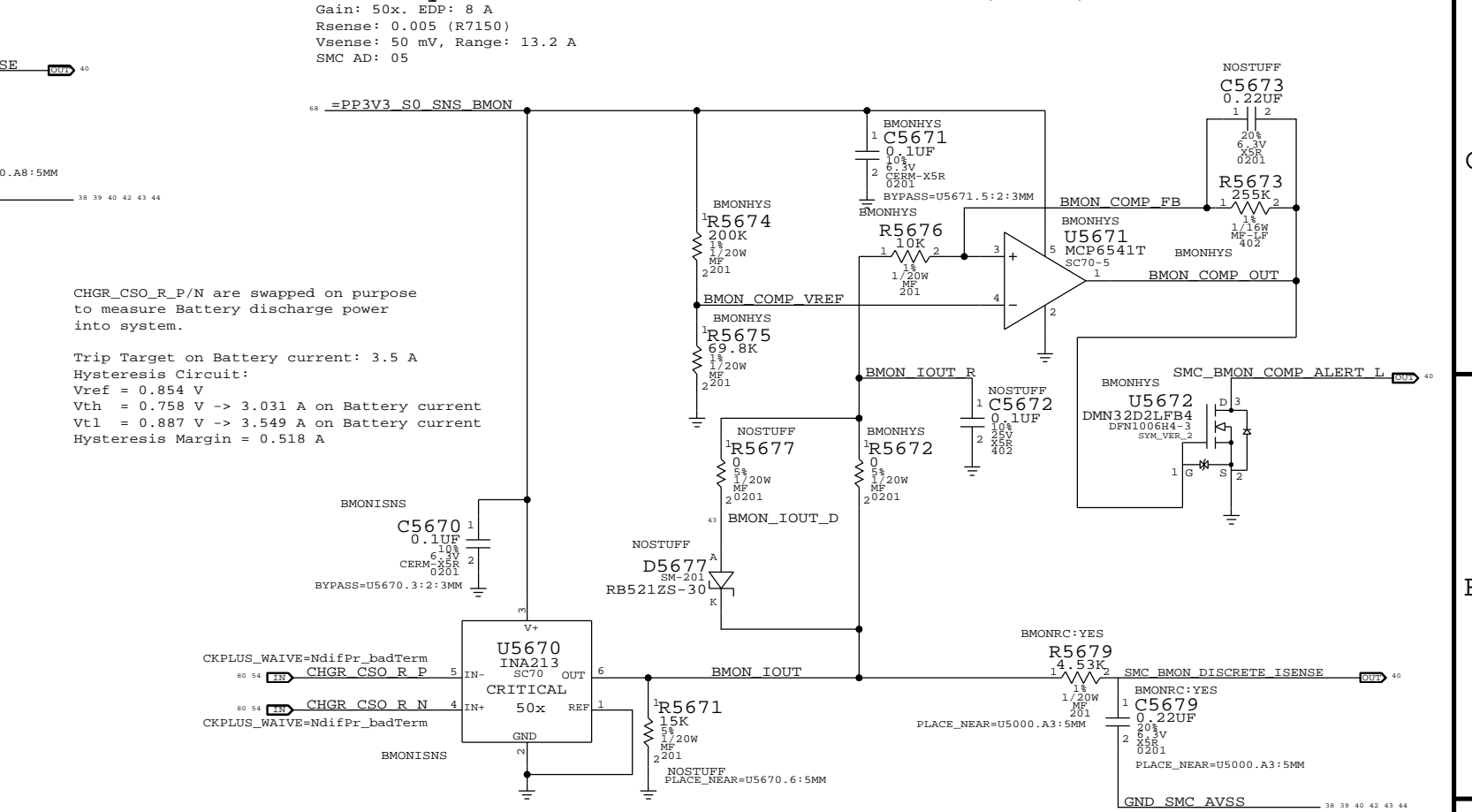
Camera (S2 Controller) Current Sense (ICMC)



Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES.MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629		LOADRC:NO
117S0008	1	RES.MTL FILM,100K,1/16W,0201,SMD,LF	C5679		BMONRC:NO
117S0008	1	RES.MTL FILM,100K,1/16W,0201,SMD,LF	C5649		TBTRC:NO

Battery BMON Discrete Current Sense (IP0R) & Threshold Alert

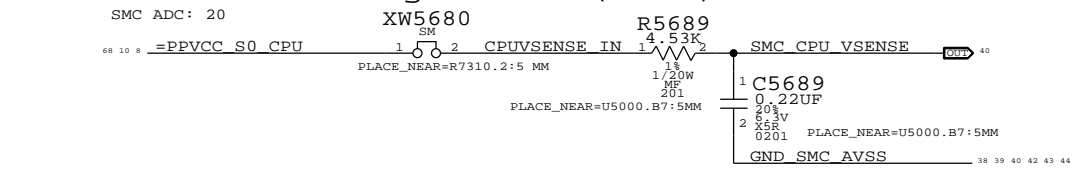


Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05

CHGR_CS0_R/P/N are swapped on purpose to measure Battery discharge power into system.

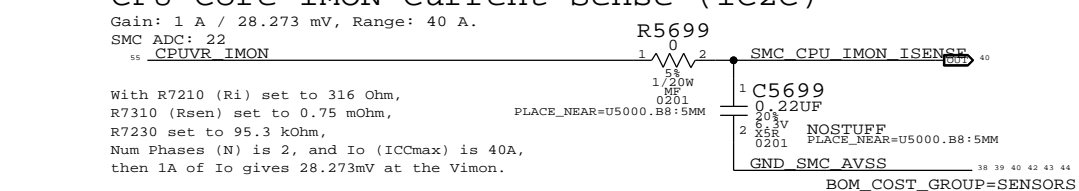
Trip Target on Battery current: 3.5 A
Hysteresis Circuit:
Vref = 0.854 V
Vth = 0.758 V -> 3.031 A on Battery current
Vtl = 0.887 V -> 3.549 A on Battery current
Hysteresis Margin = 0.518 A

CPU Core Voltage Sense (VC0C)



SMC ADC: 20

CPU Core IMON Current Sense (IC2C)



Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 22

With R7210 (Ri) set to 316 Ohm, R7310 (Rsen) set to 0.75 mOhm, R7230 set to 95.3 kOhm, Num Phases (N) is 2, and Io (ICmax) is 40A, then 1A of Io gives 28.273mV at the Vimon.

SYNC MASTER=JACK_U52 SYNC DATE=10/26/2013

Power Sensors: Extended

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

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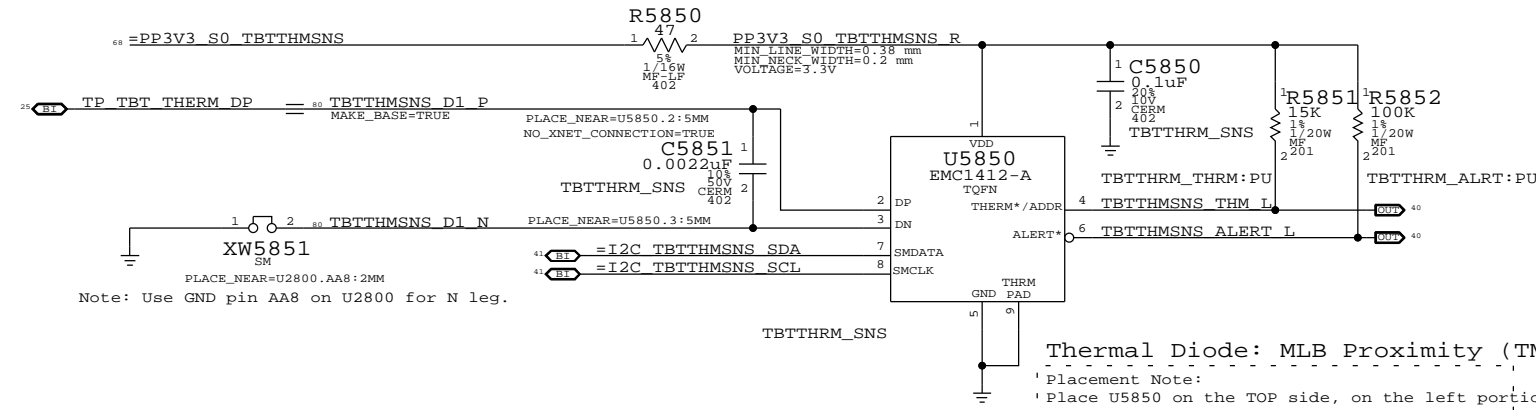
SHEET: 44 OF 82

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**Thermal Sensor A:
Thunderbolt Die, MLB Proximity**

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (THSP)
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.



U5850 I2C Address:
By setting R5851 to 15k, I2C address for U5850 is 0xD8/0xD9.

Thermal Diode: MLB Proximity (TMLB)
Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

**Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity**

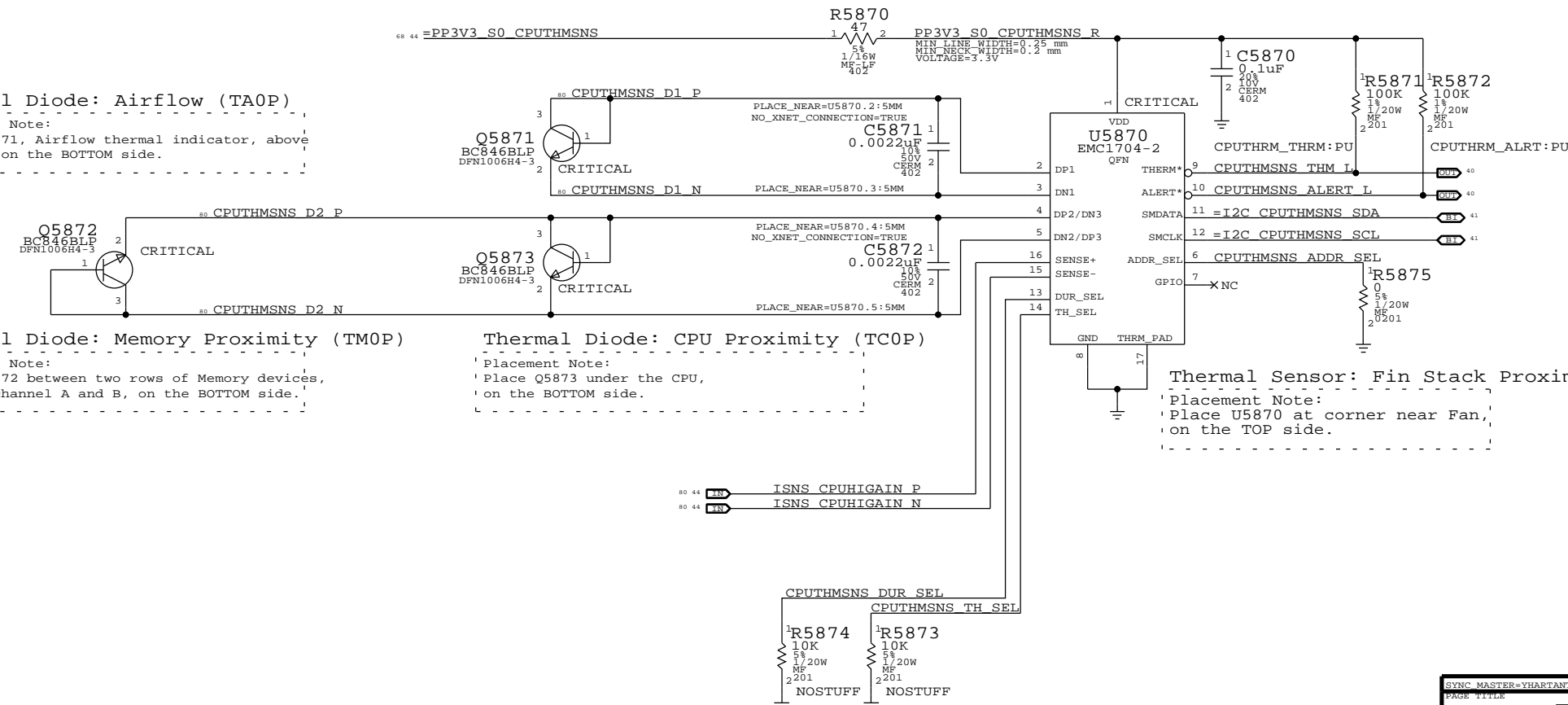
I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: Airflow (TA0P)
Placement Note:
Place Q5871, Airflow thermal indicator, above the SSD, on the BOTTOM side.

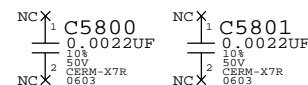
Thermal Diode: Memory Proximity (TM0P)
Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Diode: CPU Proximity (TC0P)
Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Sensor: Fin Stack Proximity (Th1H)
Placement Note:
Place U5870 at corner near Fan, on the TOP side.



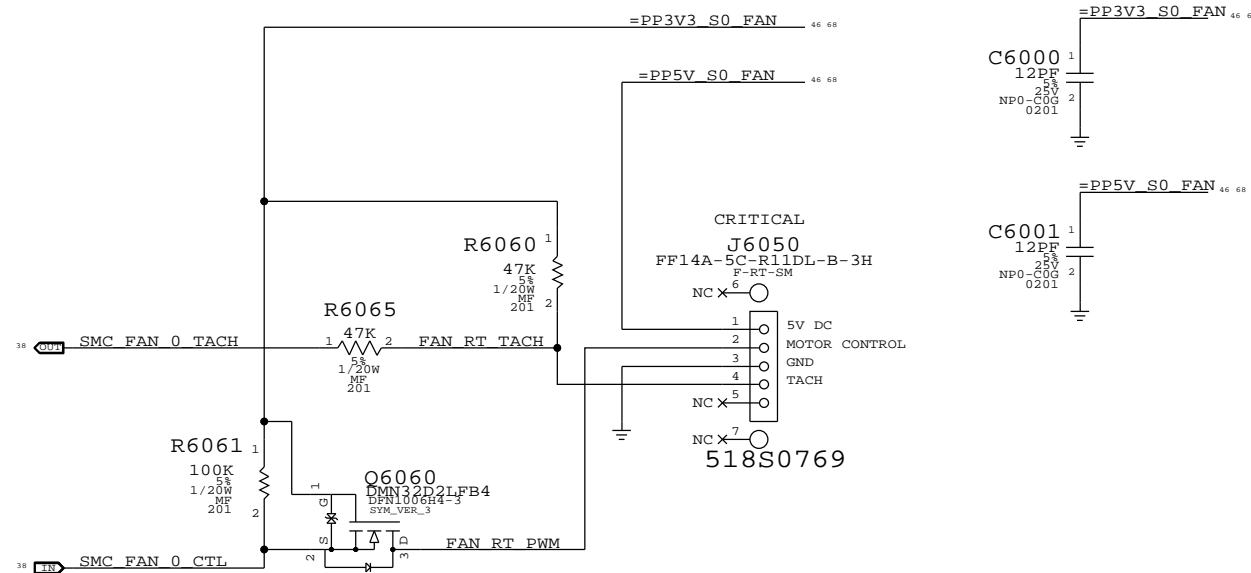
Placement Note: Place C5800 and C5801 near Q5871.



SYNC MASTER=YHARTANTO J44		SYNC DATE=01/07/2015	
Thermal Sensors			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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		PAGE	58 OF 120
		SHEET	45 OF 82

FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1



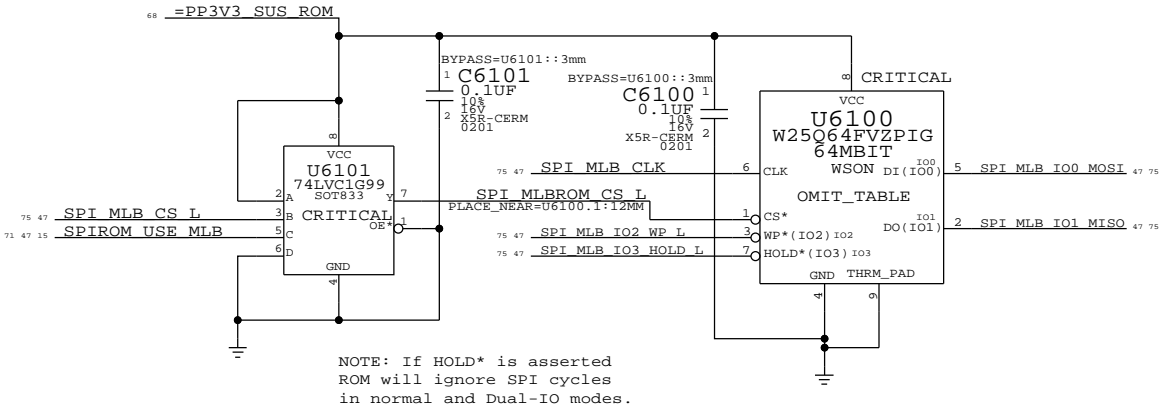
Placement Note: Place C6002 and C6003 near Q6060



SYNC MASTER=141		SYNC DATE=10/23/2012	
PAGE TITLE			
Fan		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
		REVISION	
		8.0.0	
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		dvt1	
		PAGE	
		60 OF 120	
		SHEET	
		46 OF 82	

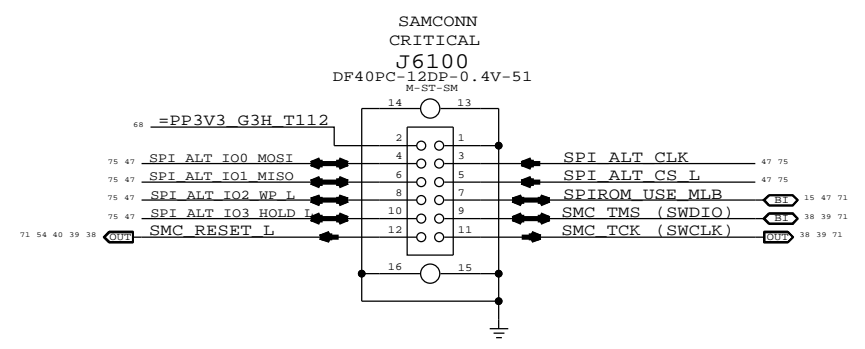
BOM_COST_GROUP=FAN

SPI ROM
 Quad-IO Mode (Mode 0 & 3) supported.
 SPI Frequency: 50MHz for CPU, 20MHz for SMC.

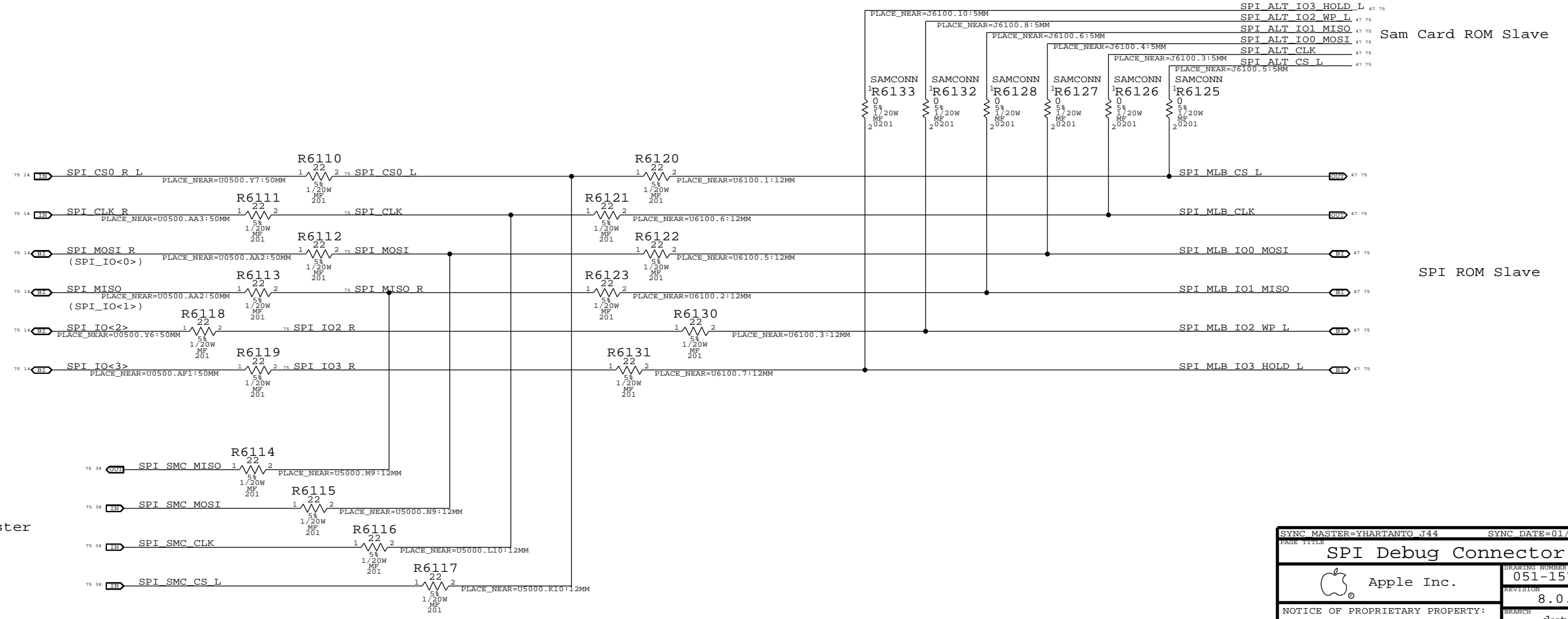


Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



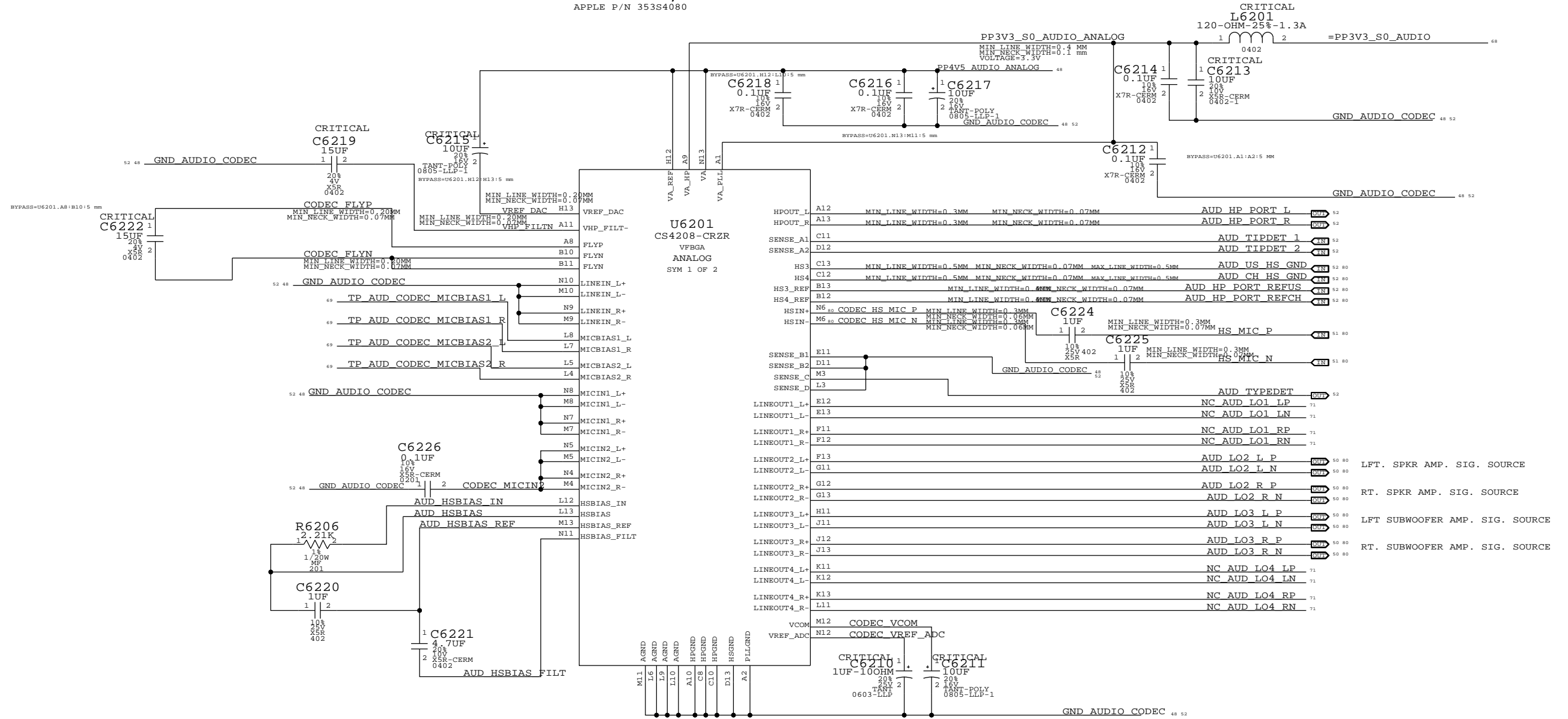
SPI Bus Series Termination



SYNC MASTER=YHARTANTO J44		SYNC DATE=01/09/2013	
SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	051-1573
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		BRANCH	dvt1
		PAGE	61 OF 120
		SHEET	47 OF 82

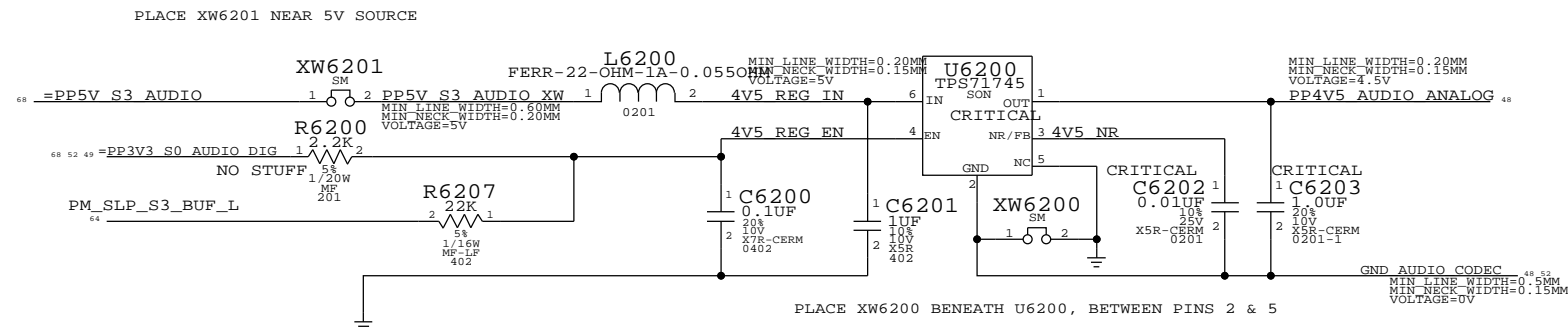
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



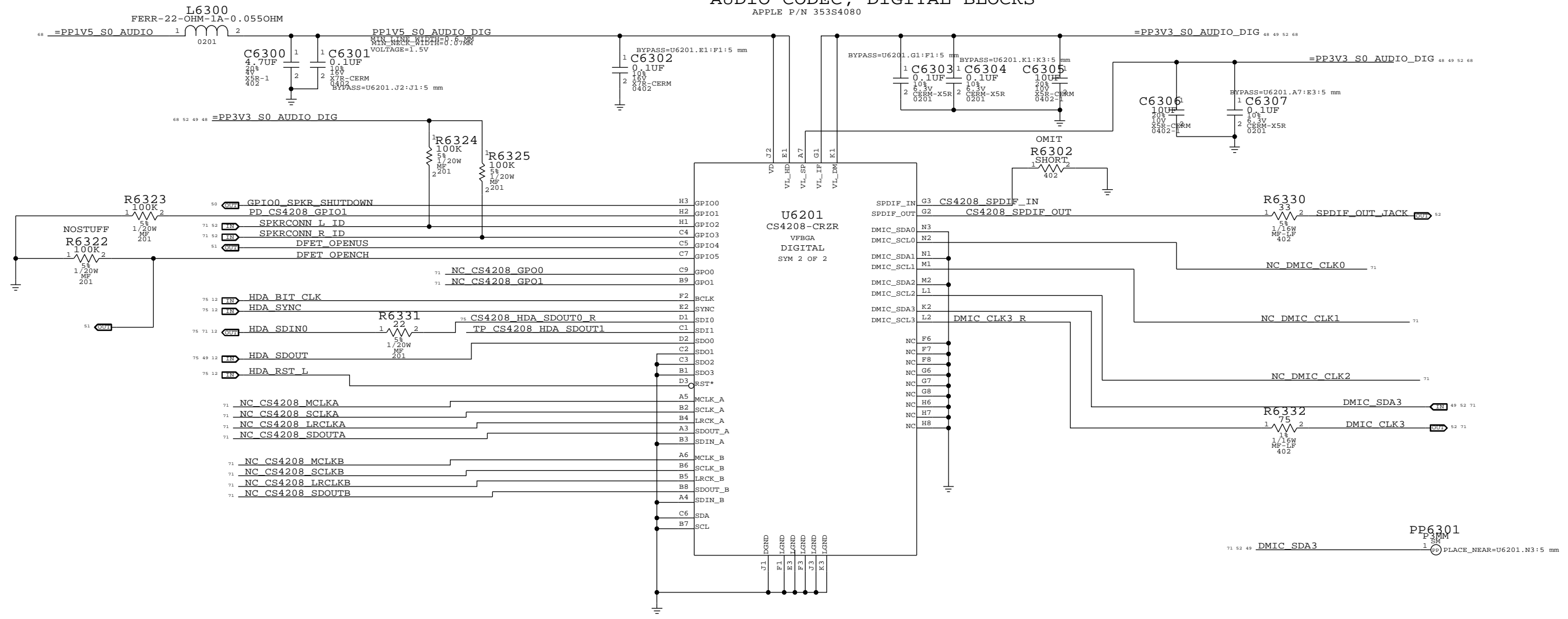
4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



SYNC MASTER=ICURCIO-J44		SYNC DATE=05/13/2011	
PAGE TITLE			
Audio: Codec, Analog		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
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		8.0.0	dvt1
		PAGE	SHEET
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AUDIO CODEC, DIGITAL BLOCKS
APPLE P/N 353S4080



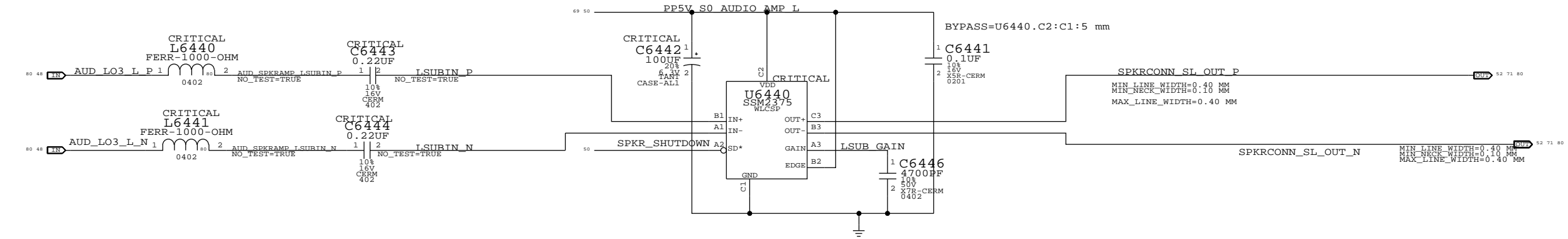
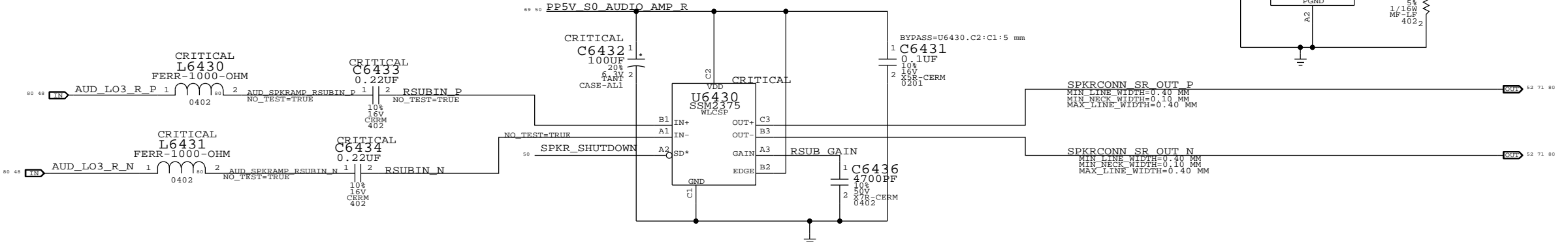
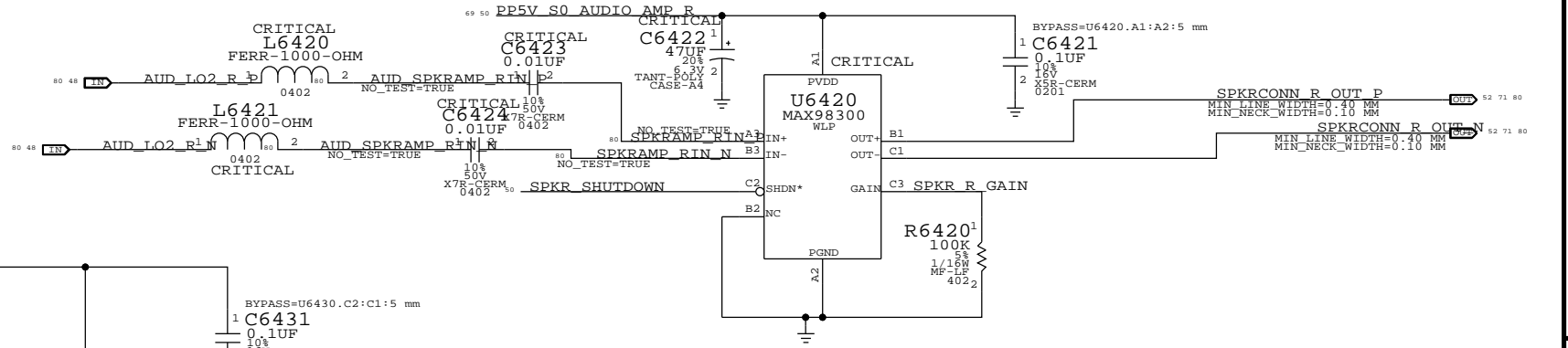
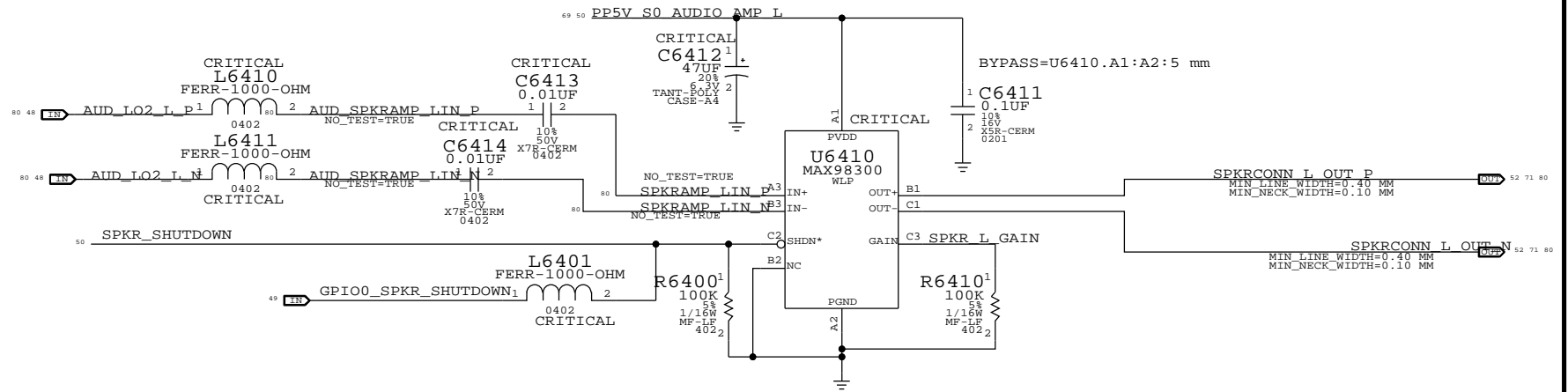
PP6301
P 3MM
1
PLACE_NEAR=U6201.N3:5 mm

PP6304
P 3MM
1
PLACE_NEAR=U6201.D2:5 mm

SYNC MASTER=ICURCIO J44		SYNC DATE=07/25/2013	
PAGE TITLE Audio: Codec, Digital			
Apple Inc.		DRAWING NUMBER 051-1573	SIZE D
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BOM_COST_GROUP=AUDIO		PAGE 63 OF 120	SHEET 49 OF 82

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
 GAIN = +3 DB
 1ST ORDER FC (L&R) = NOM 569 HZ
 1ST ORDER FC (SUB) = NOM 9 HZ

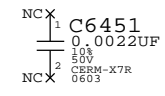
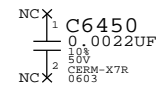
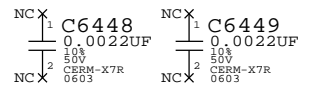
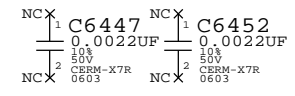


Placement Note: Place C6447 and C6452 near U6420

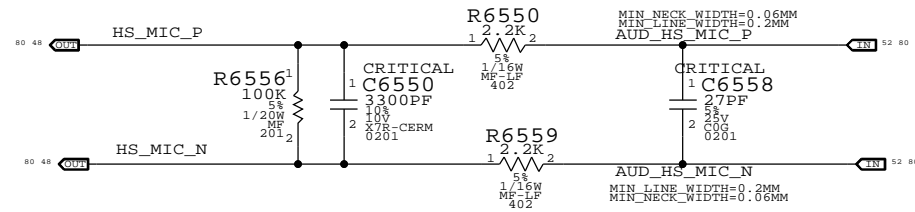
Placement Note: Place C6448 and C6449 near U6430

Placement Note: Place C6450 near U6410

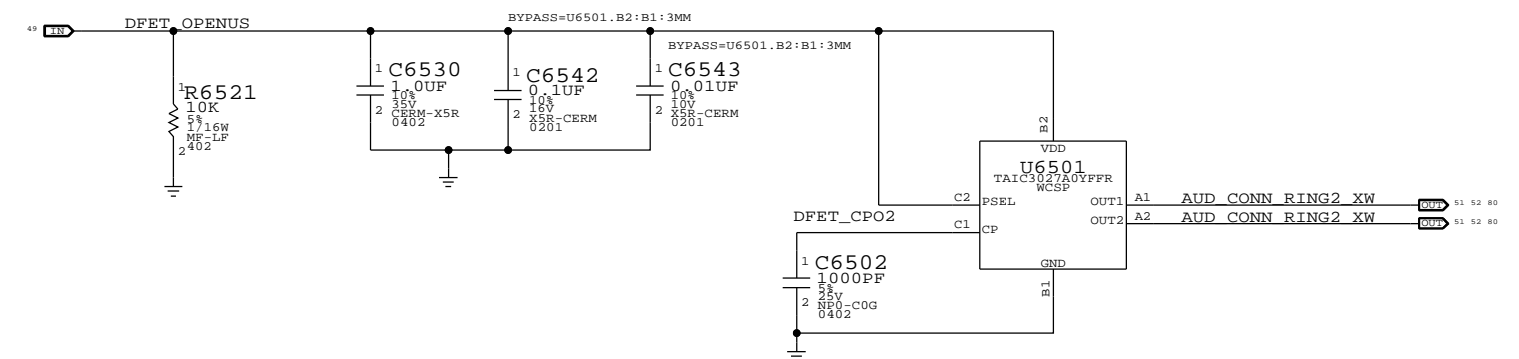
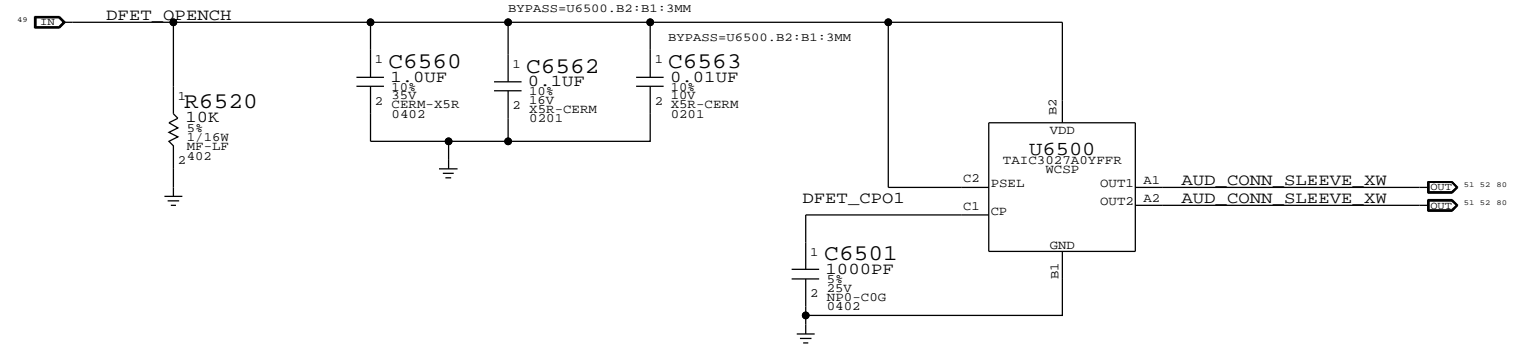
Placement Note: Place C6451 near U6440



SYNC MASTER=DIRK J44		SYNC DATE=01/09/2013	
Audio: Speaker Amps			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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		PAGE	64 OF 120
		SHEET	50 OF 82



R/C6550 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)



SYNC MASTER=ICIRCIO J44		SYNC DATE=07/25/2013	
Audio: Jack Support			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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		PAGE	65 OF 120
		SHEET	51 OF 82
		BOM_COST_GROUP=AUDIO	

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

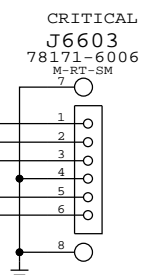
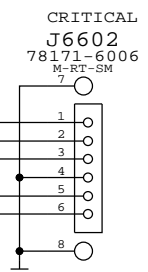
FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETs OPEN

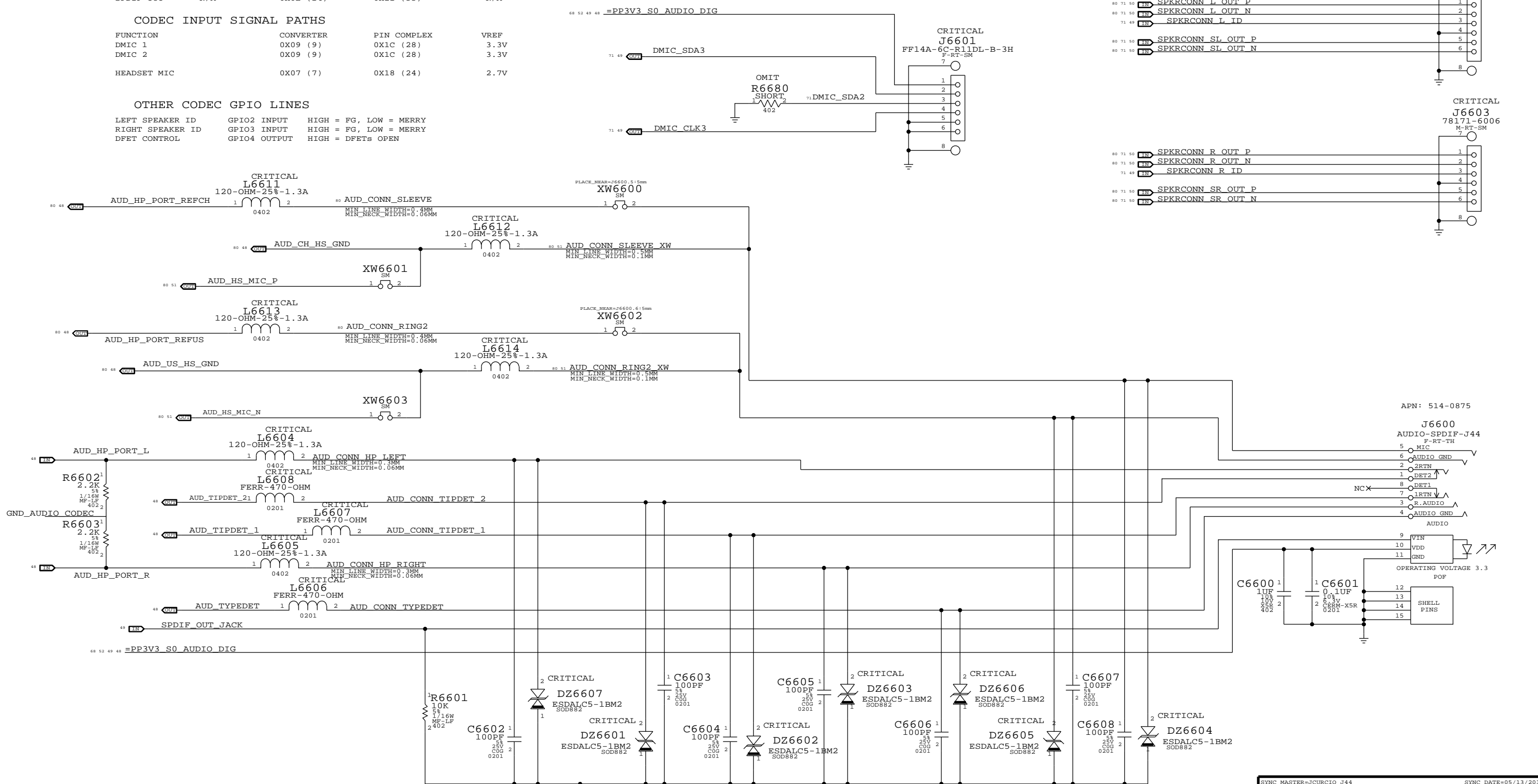
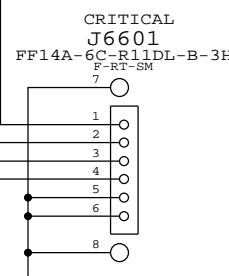
SPEAKER CONNECTOR

HP=80HZ
APN: 518S0672



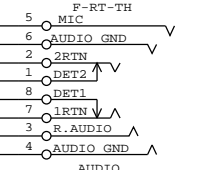
2-MIC CONNECTOR

APN: 518S0818



APN: 514-0875

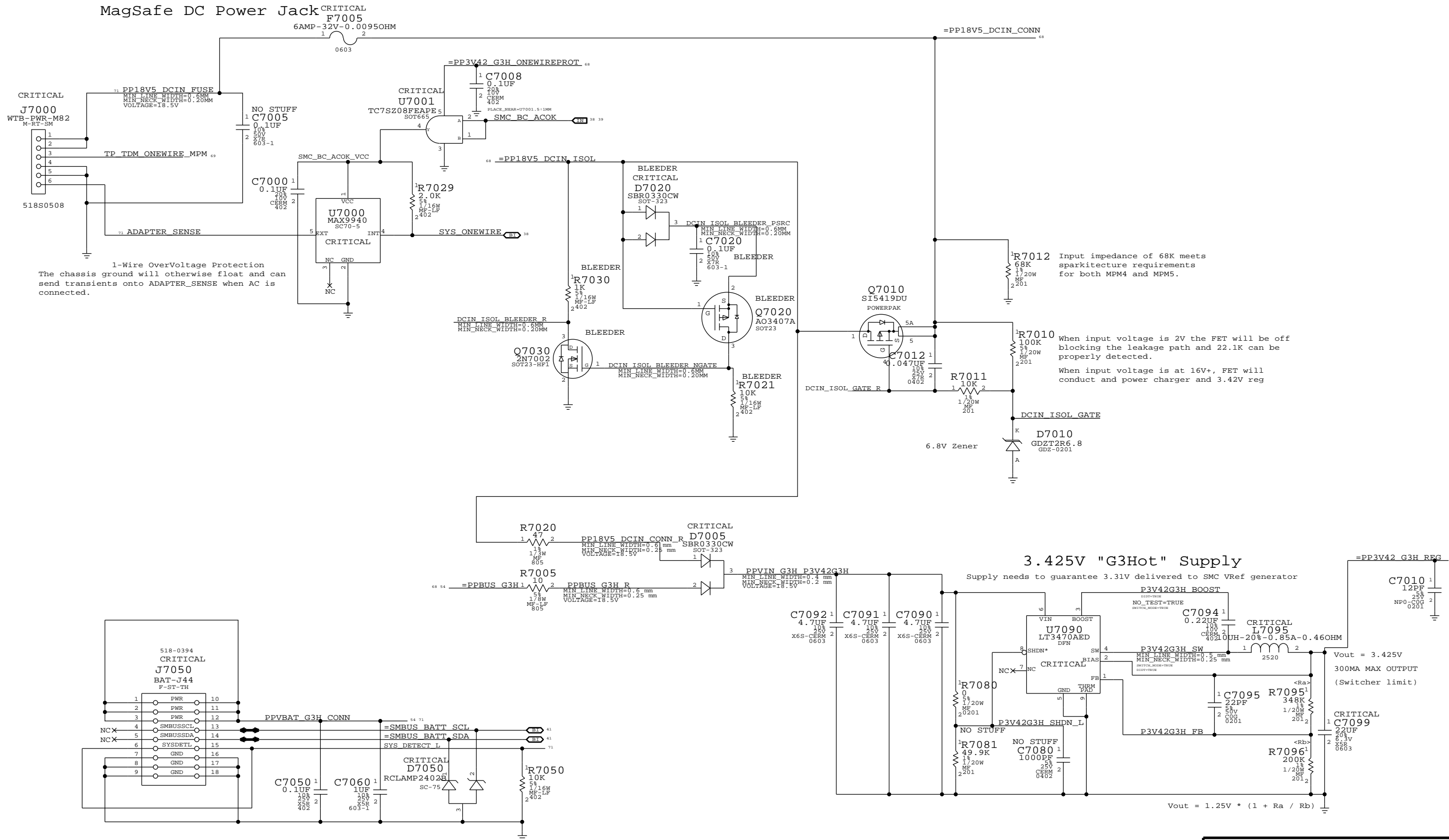
J6600



OPERATING VOLTAGE 3.3V
POF

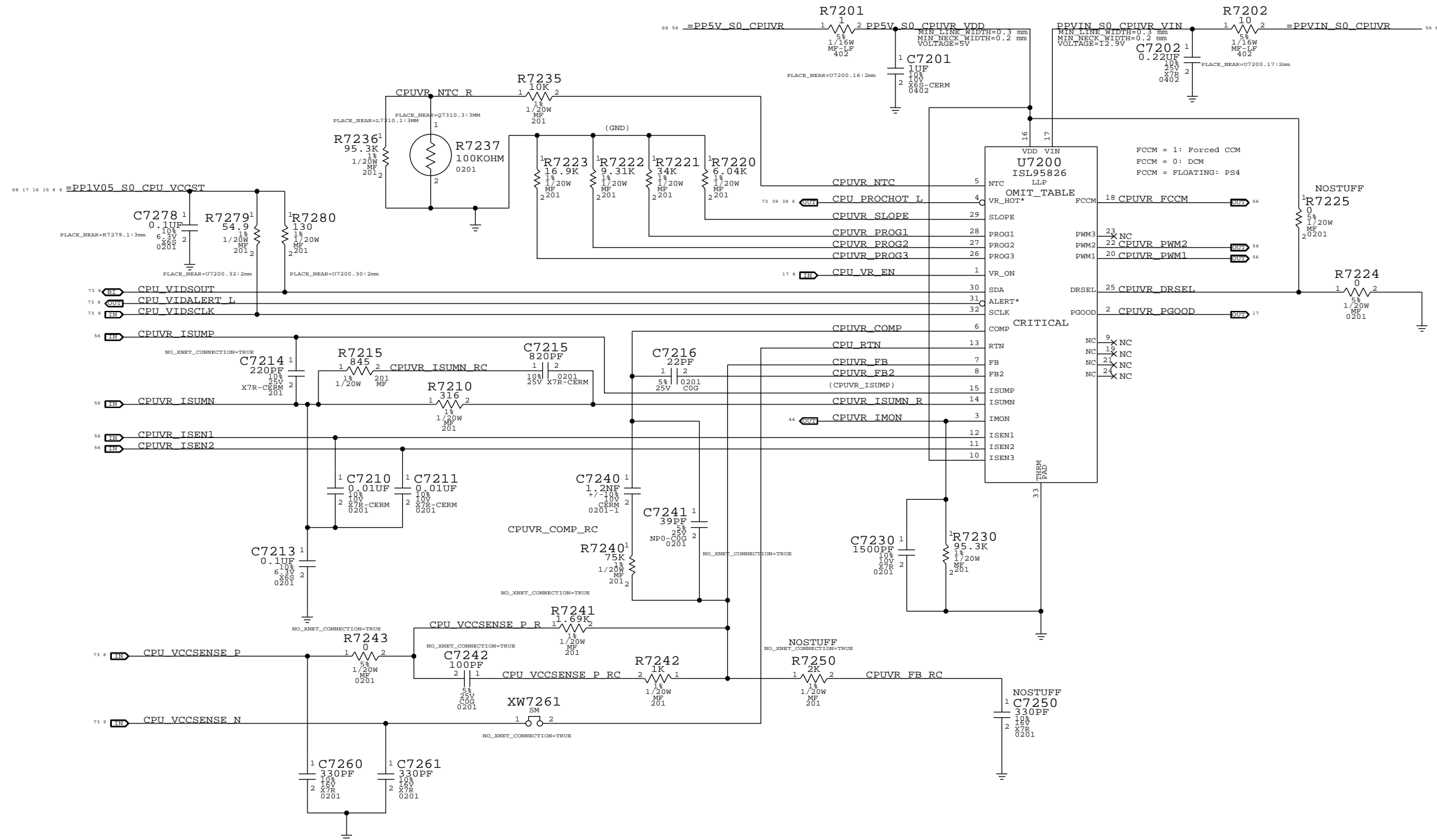
SYNC MASTER=ICIRCIO J44		SYNC DATE=05/13/2013	
PAGE TITLE			
Audio: Jack Translators			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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		SHEET	52 OF 82

MagSafe DC Power Jack

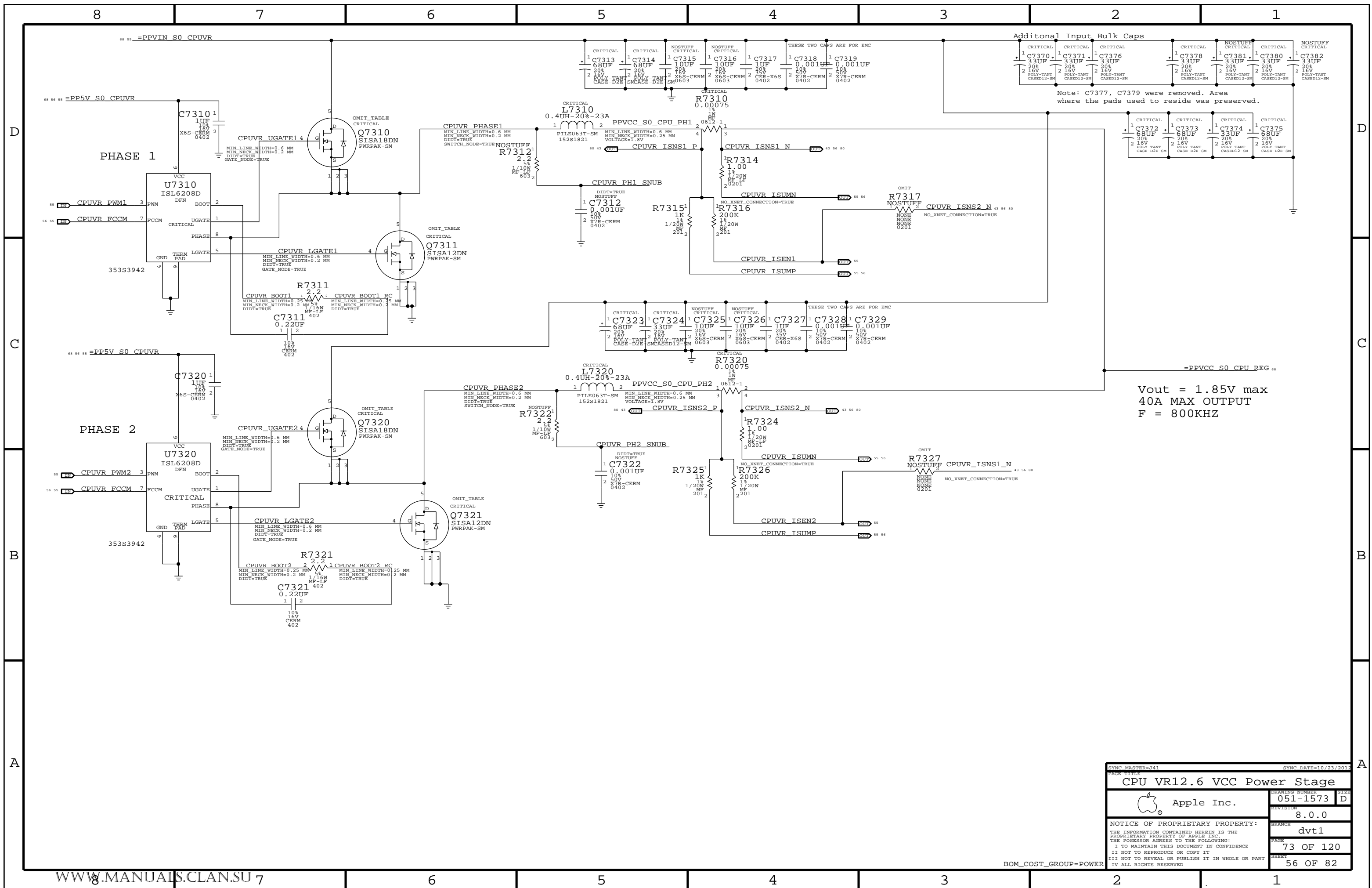


SYMC-WATER-STARTINTO_144		SYMC-DATA-01/09/2011	
DC-In & Battery Connectors			
Apple Inc.	DRAWING NUMBER	051-1573	SIZE D
	REVISION	8.0.0	
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		SHEET	53 OF 82

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00036	1	IC, ISL95826AS2378, PWM, PG, VR12.5/6, QFN-32	U7200	CRITICAL	



SYNC MASTER=141		SYNC DATE=10/23/2012	
CPU VR12.6 VCC Regulator IC			
Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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Additional Input Bulk Caps

Note: C7377, C7379 were removed. Area where the pads used to reside was preserved.

Vout = 1.85V max
40A MAX OUTPUT
F = 800KHZ

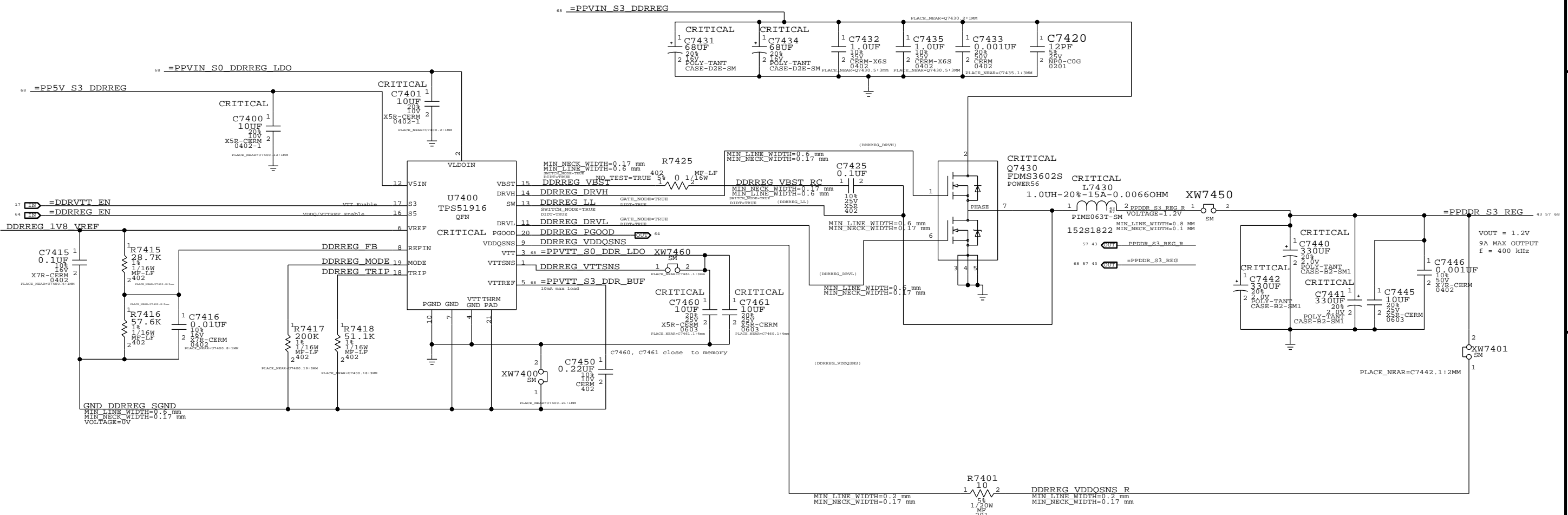
CPU VR12.6 VCC Power Stage		DRAWING NUMBER	051-1573	SIZE	D
Apple Inc.		REVISION	8.0.0		
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	dvt1		
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1.2V S3 Regulator

8 7 6 5 4 3 2 1

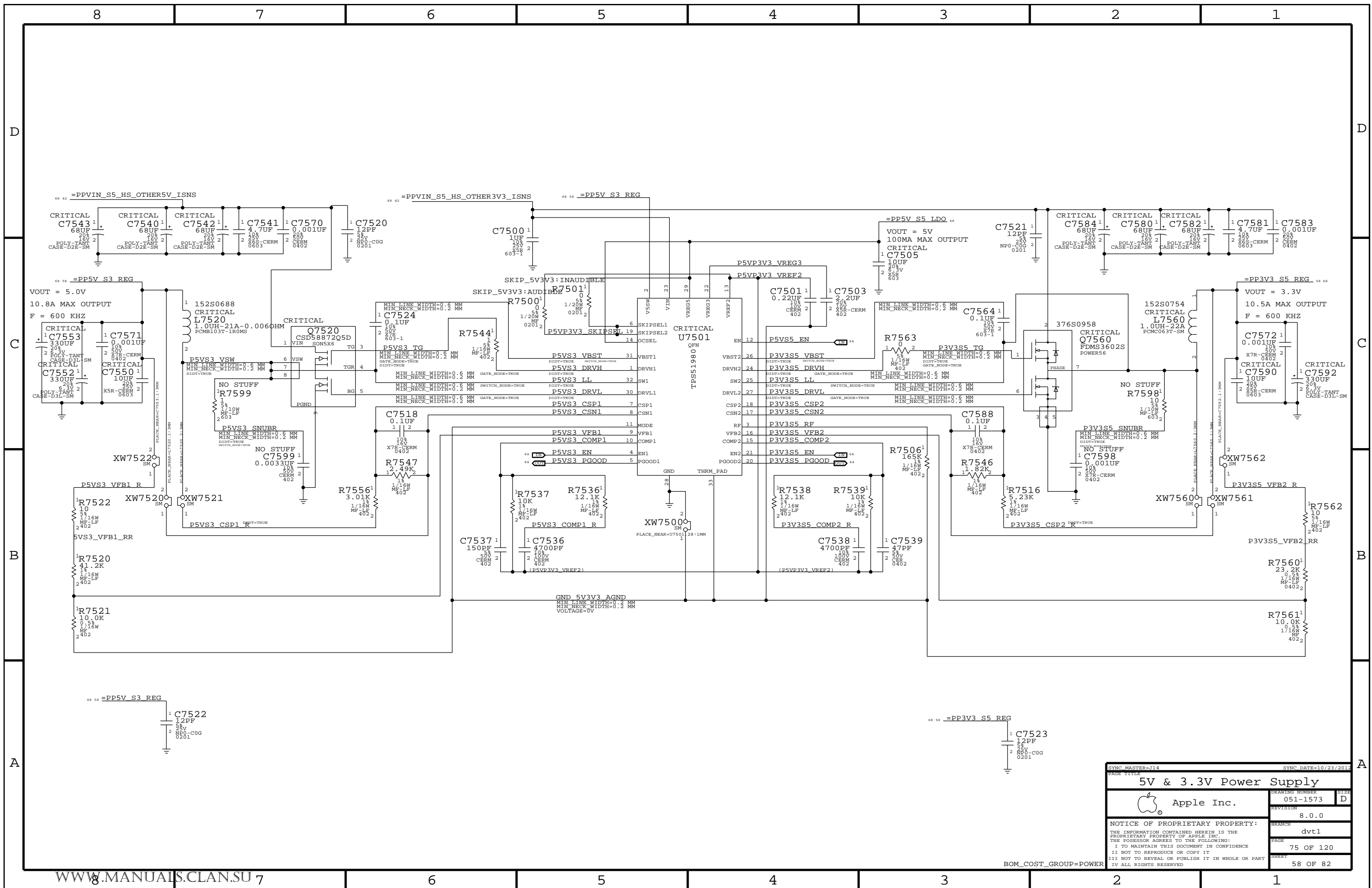
D
C
B
A

D
C
B
A



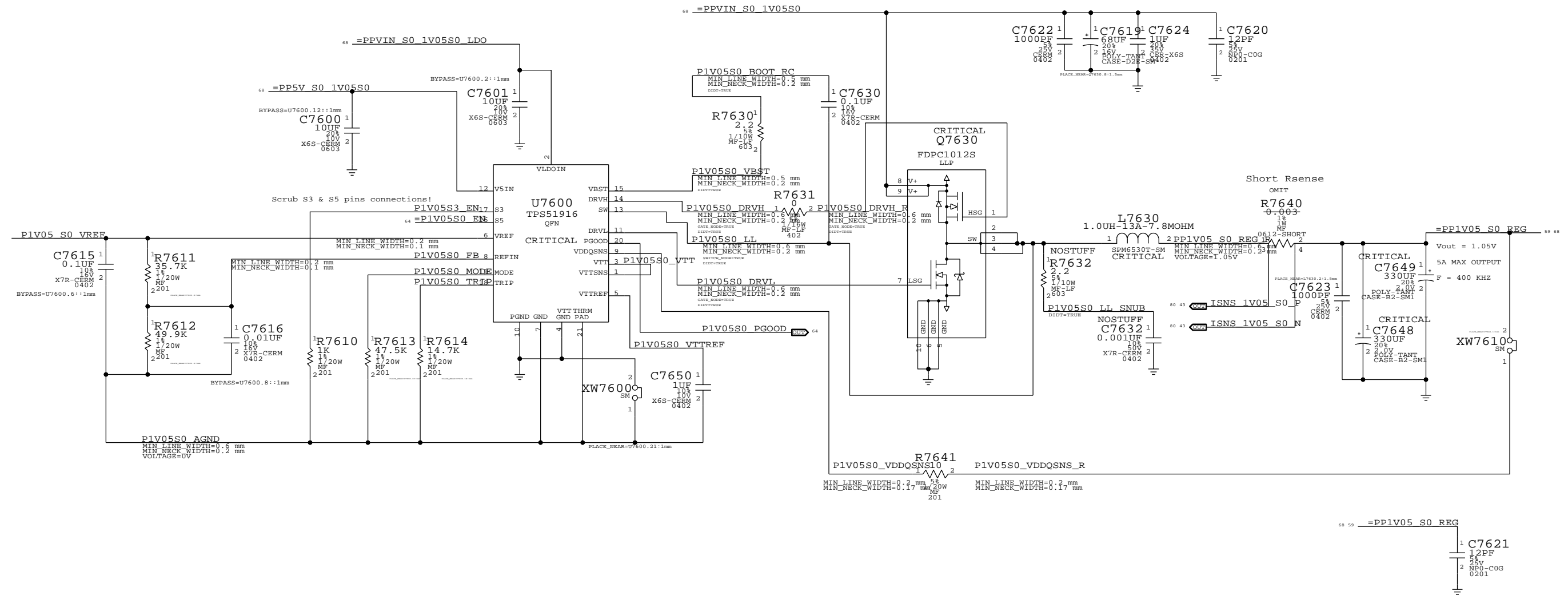
SYNC MASTER=141_MLB		SYNC DATE=05/21/2013	
PAGE TITLE			
LPDDR3 Supply		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
NOTICE OF PROPRIETARY PROPERTY:		REVISION	BRANCH
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8 7 6 5 4 3 2 1



SYNC MASTER=114		SYNC DATE=10/23/2012	
PAGE TITLE			
5V & 3.3V Power Supply		DRAWING NUMBER	051-1573
Apple Inc.		REVISION	8.0.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	dvt1
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1.05V S0 Regulator



SYNC MASTER=AHARTMAN J52		SYNC DATE=10/29/2013	
PAGE TITLE			
1.05V Power Supply		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
NOTICE OF PROPRIETARY PROPERTY:		REVISION	8.0.0
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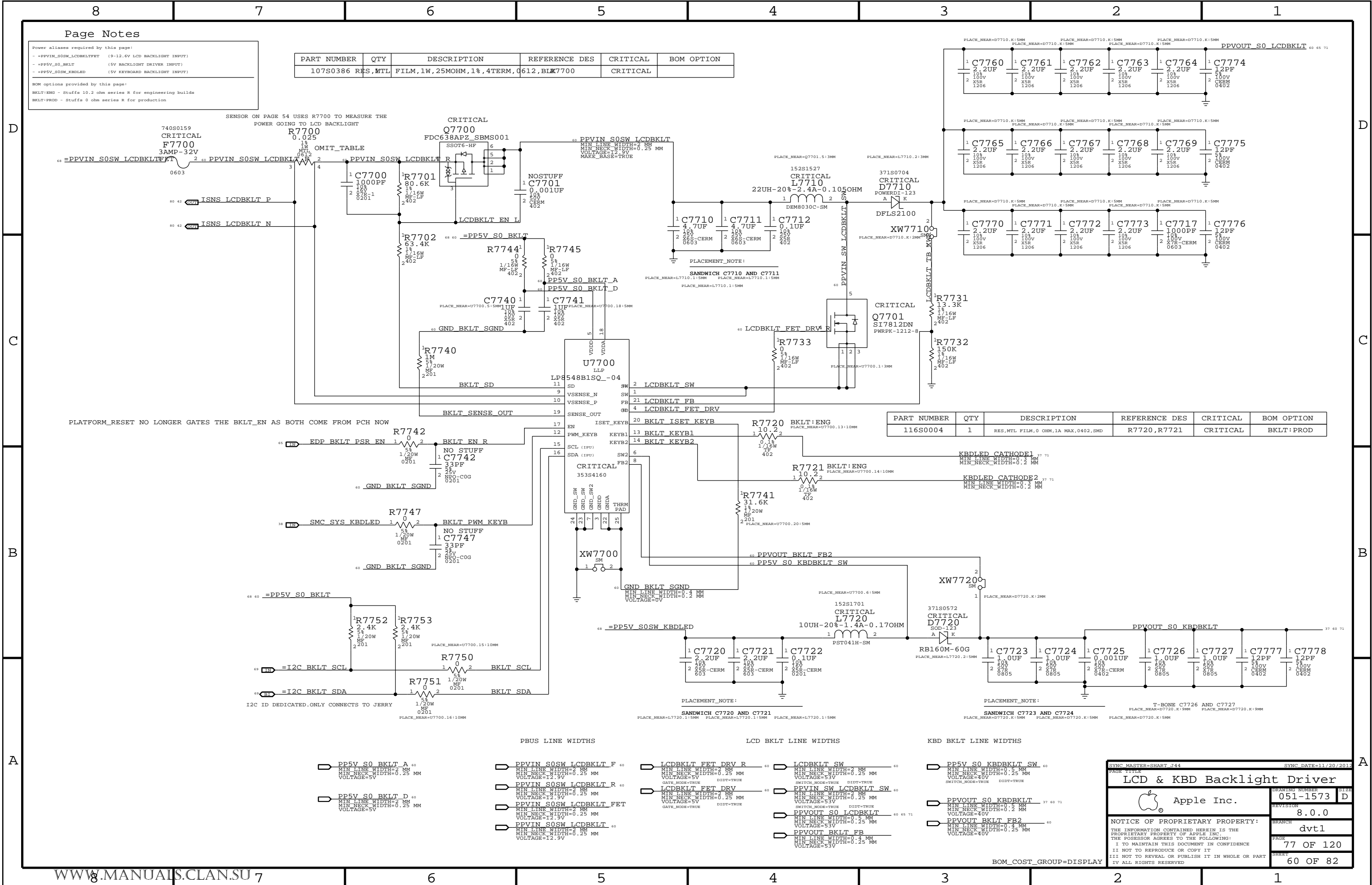
Page Notes

Power aliases required by this page:
 -PPVIN_S0SW_LCDCLKT (9-12.6V LCD BACKLIGHT INPUT)
 -PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
 -PP5V_S0SW_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

BOM options provided by this page:
 BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
 BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0386	RES, MTL	FILM, 1W, 25MOHM, 1%, 4TERM, G612, BLK7700		CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES, MTL FILM, 0 OHM, 1A MAX, 0402, SMD	R7720, R7721	CRITICAL	BKLT:PROD



A

A

SYNC MASTER=SHART_344 SYNC DATE=11/20/2012

LCD & KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

BRANCH: dvt1

PAGE: 77 OF 120

SHEET: 60 OF 82

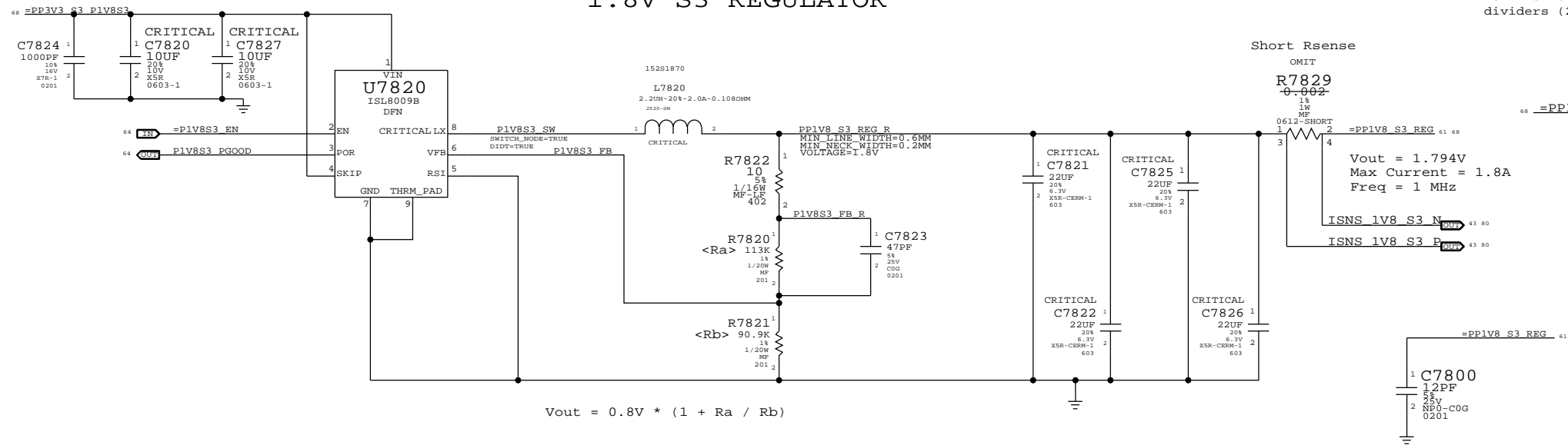
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BOM_COST_GROUP=DISPLAY

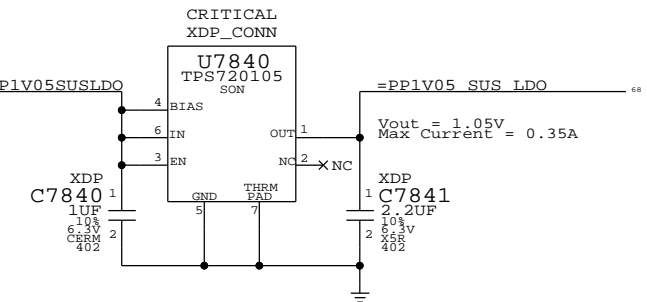
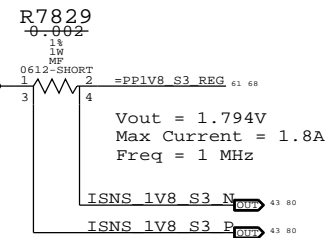
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

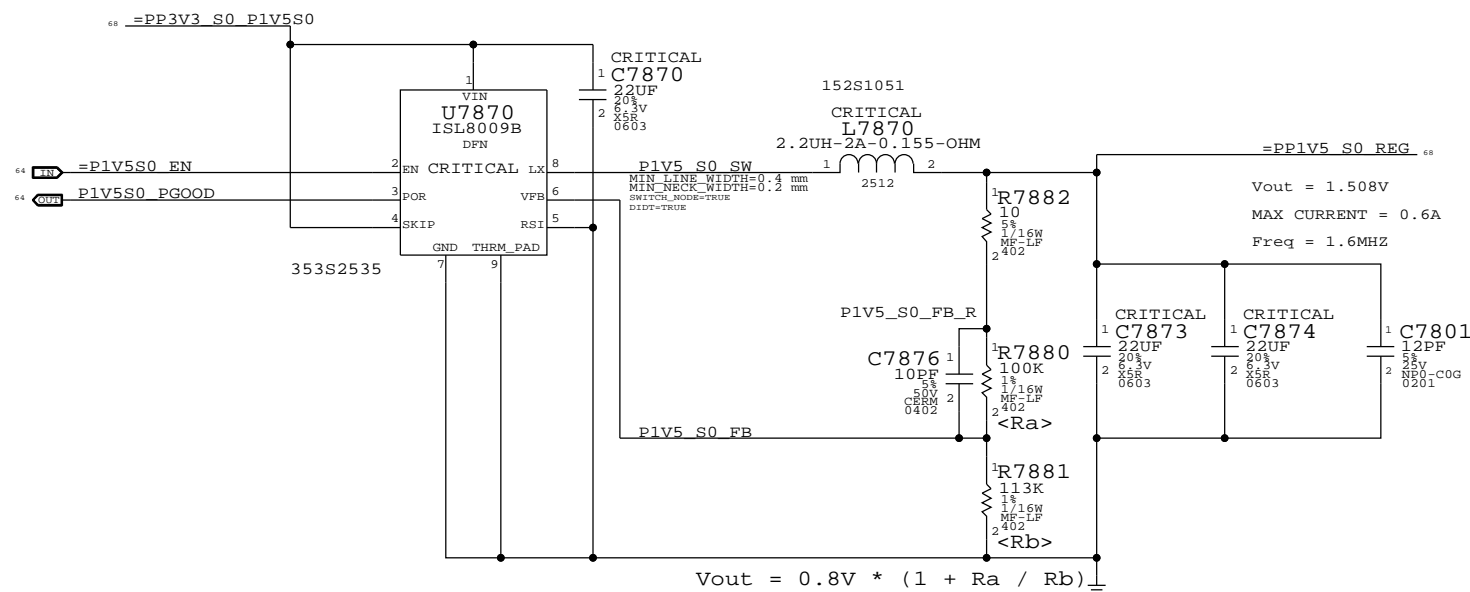
1.8V S3 REGULATOR



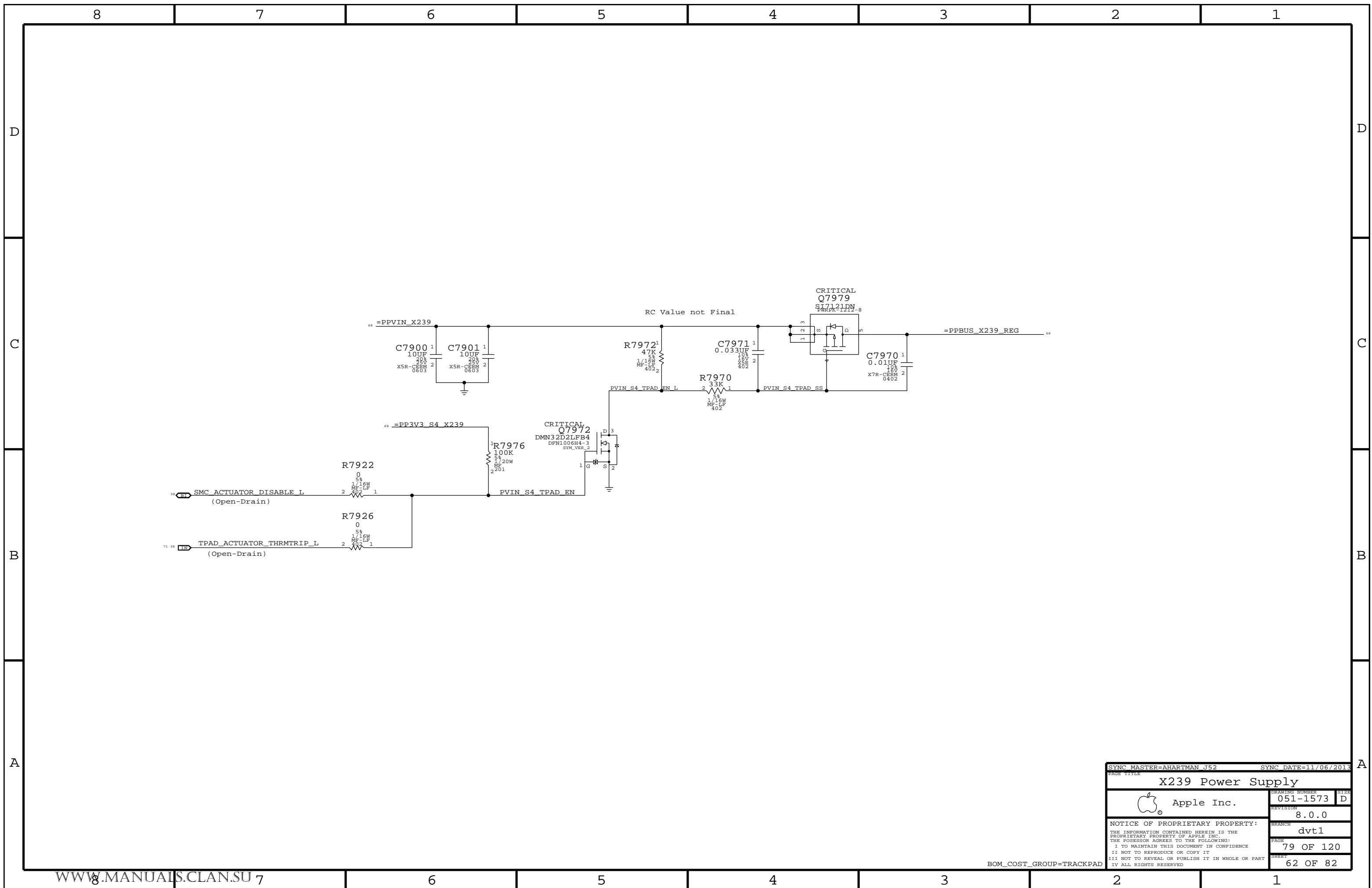
Short Rsense



1.5V S0 Switcher



SYNC MASTER=AHARTMAN J52		SYNC DATE=11/06/2013	
PAGE TITLE			
Misc Power Supplies			
DRAWING NUMBER		051-1573	
REVISION		8.0.0	
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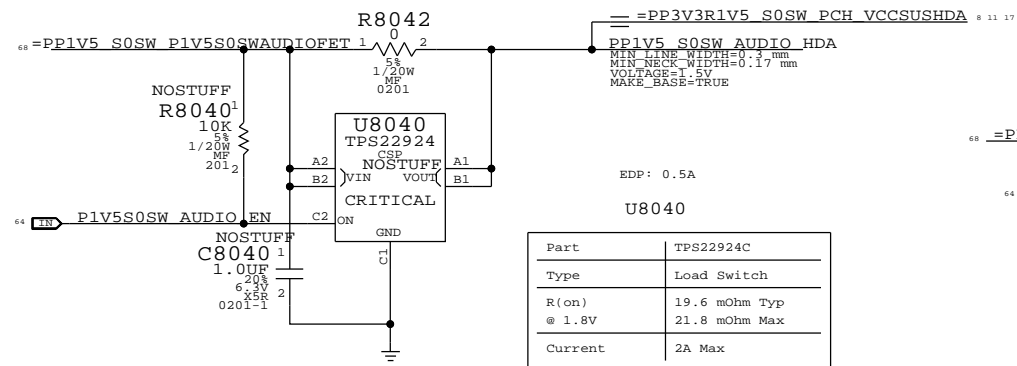


SYNC MASTER=AHARTMAN J52		SYNC DATE=11/06/2013	
X239 Power Supply			
Apple Inc.		DRAWING NUMBER	SIZE
		051-1573	D
		REVISION	
		8.0.0	
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			dvt1
		PAGE	79 OF 120
		SHEET	62 OF 82

BOM_COST_GROUP=TRACKPAD

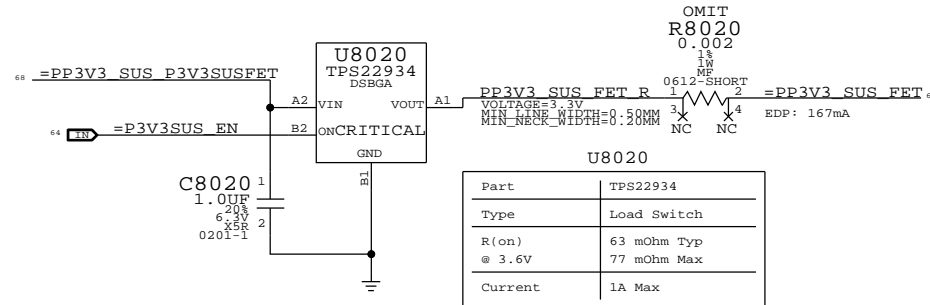
1.5V S0 Audio Switch (BYPASSED)

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



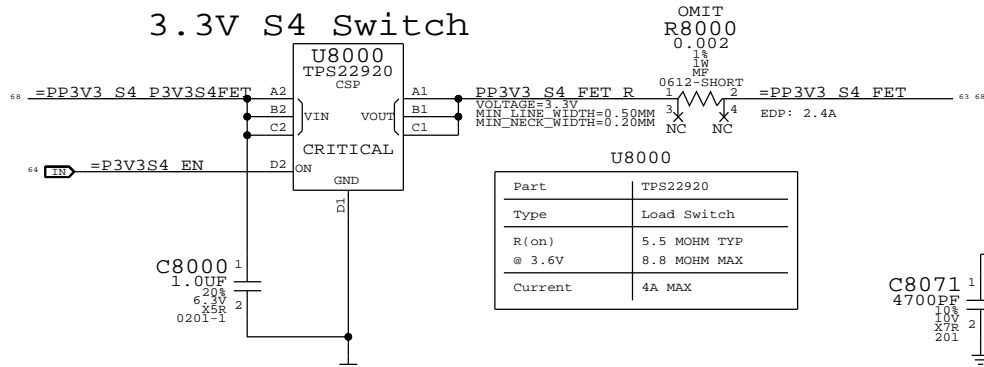
Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ
R(on) @ 1.5V	21.8 mOhm Max
Current	2A Max

3.3V SUS Switch



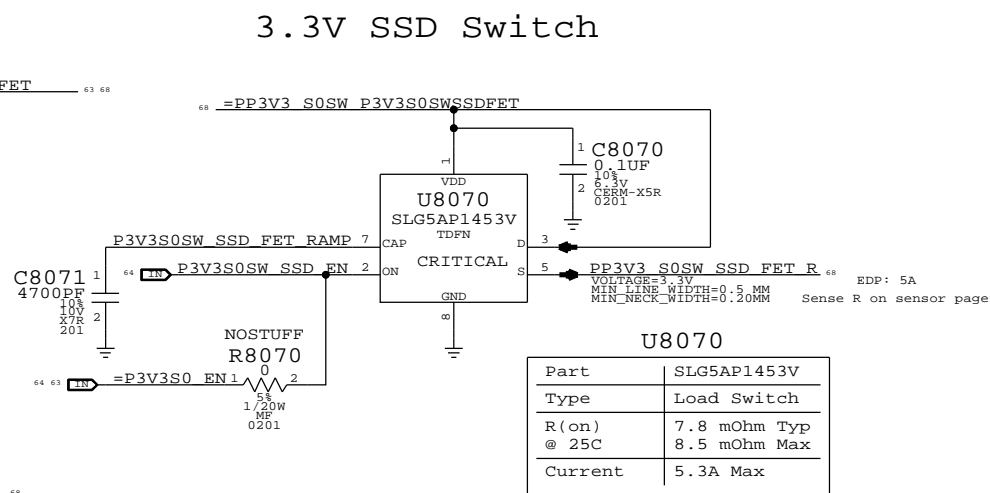
Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ
R(on) @ 3.3V	77 mOhm Max
Current	1A Max

3.3V S4 Switch



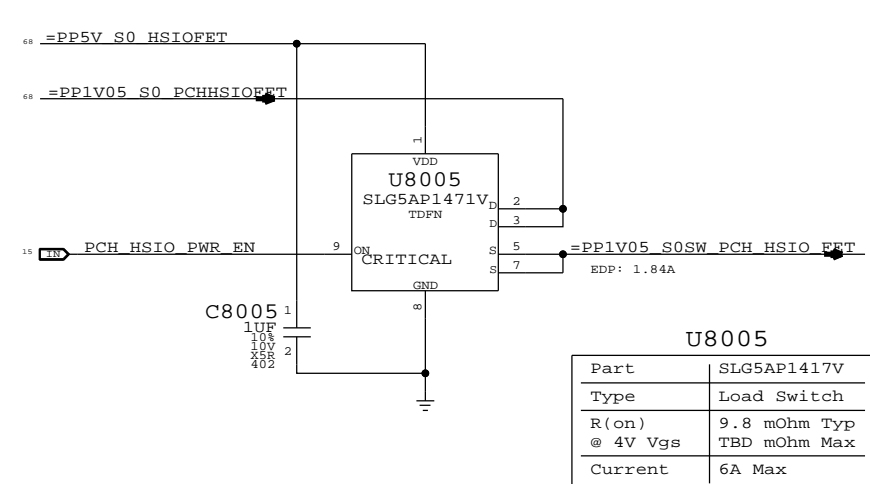
Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.5 MOHM TYP
R(on) @ 3.3V	8.8 MOHM MAX
Current	4A MAX

3.3V SSD Switch



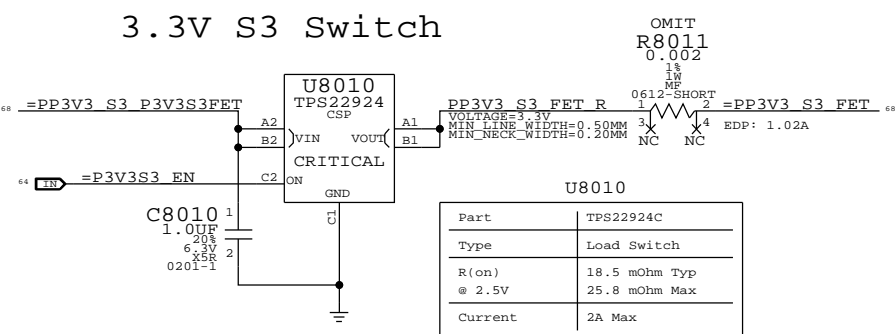
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ
R(on) @ 3.3V	8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch



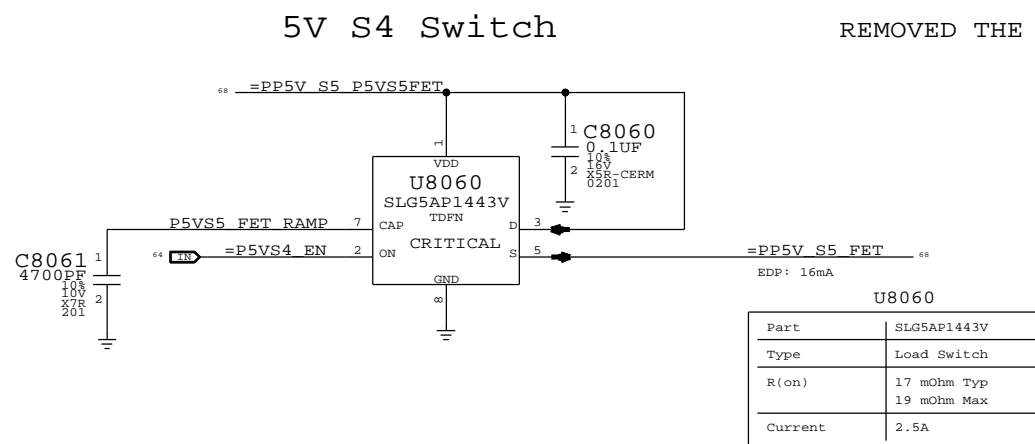
Part	SLG5AP1471V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ
R(on) @ 1.05V	TBD mOhm Max
Current	6A Max

3.3V S3 Switch



Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ
R(on) @ 3.3V	25.8 mOhm Max
Current	2A Max

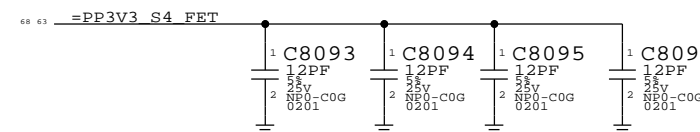
5V S4 Switch



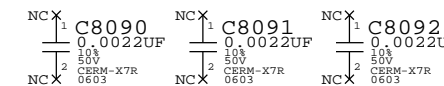
Part	SLG5AP1443V
Type	Load Switch
R(on) @ 5V	17 mOhm Typ
R(on) @ 5.5V	19 mOhm Max
Current	2.5A

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

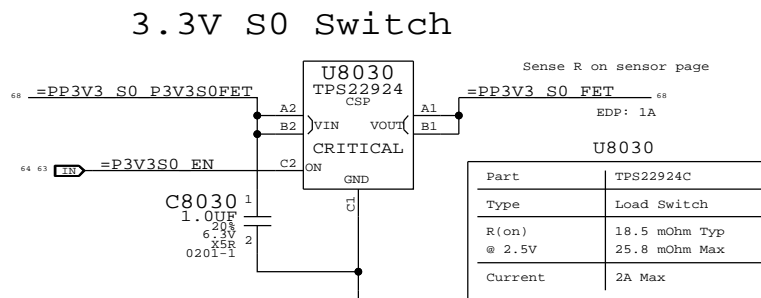
CAPACITORS ADDED FOR NOISE FLOOR REASONS:



Placement Note: Place C8090, C8091 and C8092 near U8000

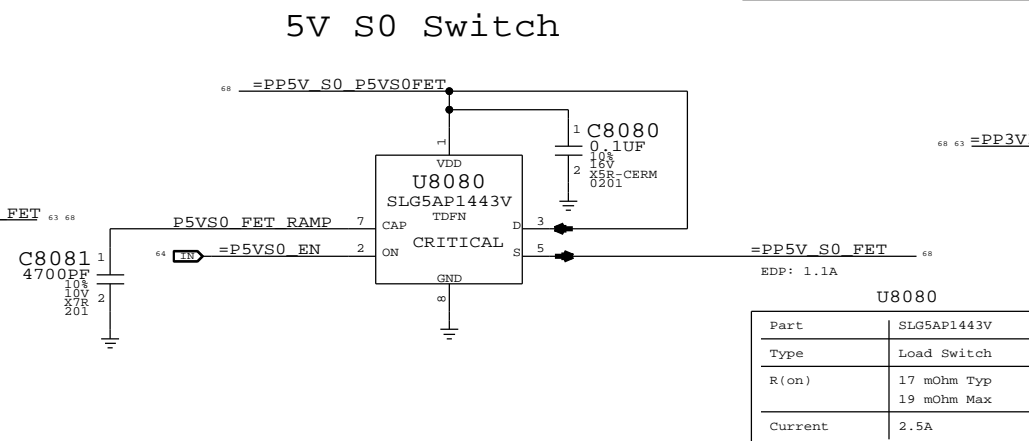


3.3V S0 Switch



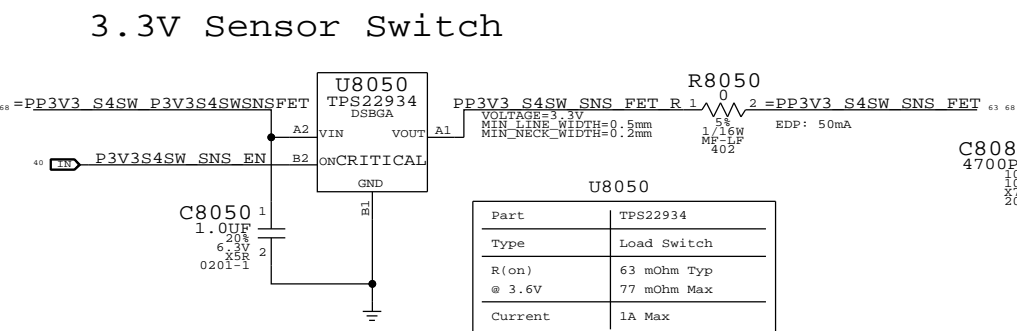
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ
R(on) @ 3.3V	25.8 mOhm Max
Current	2A Max

5V S0 Switch

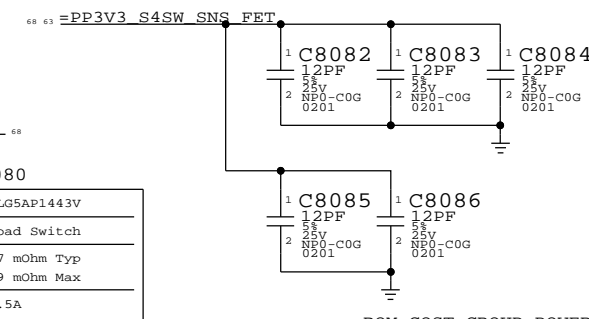


Part	SLG5AP1443V
Type	Load Switch
R(on) @ 5V	17 mOhm Typ
R(on) @ 5.5V	19 mOhm Max
Current	2.5A

3.3V Sensor Switch



Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ
R(on) @ 3.3V	77 mOhm Max
Current	1A Max



Power FETs

Apple Inc.

051-1573 D

8.0.0

dvt1

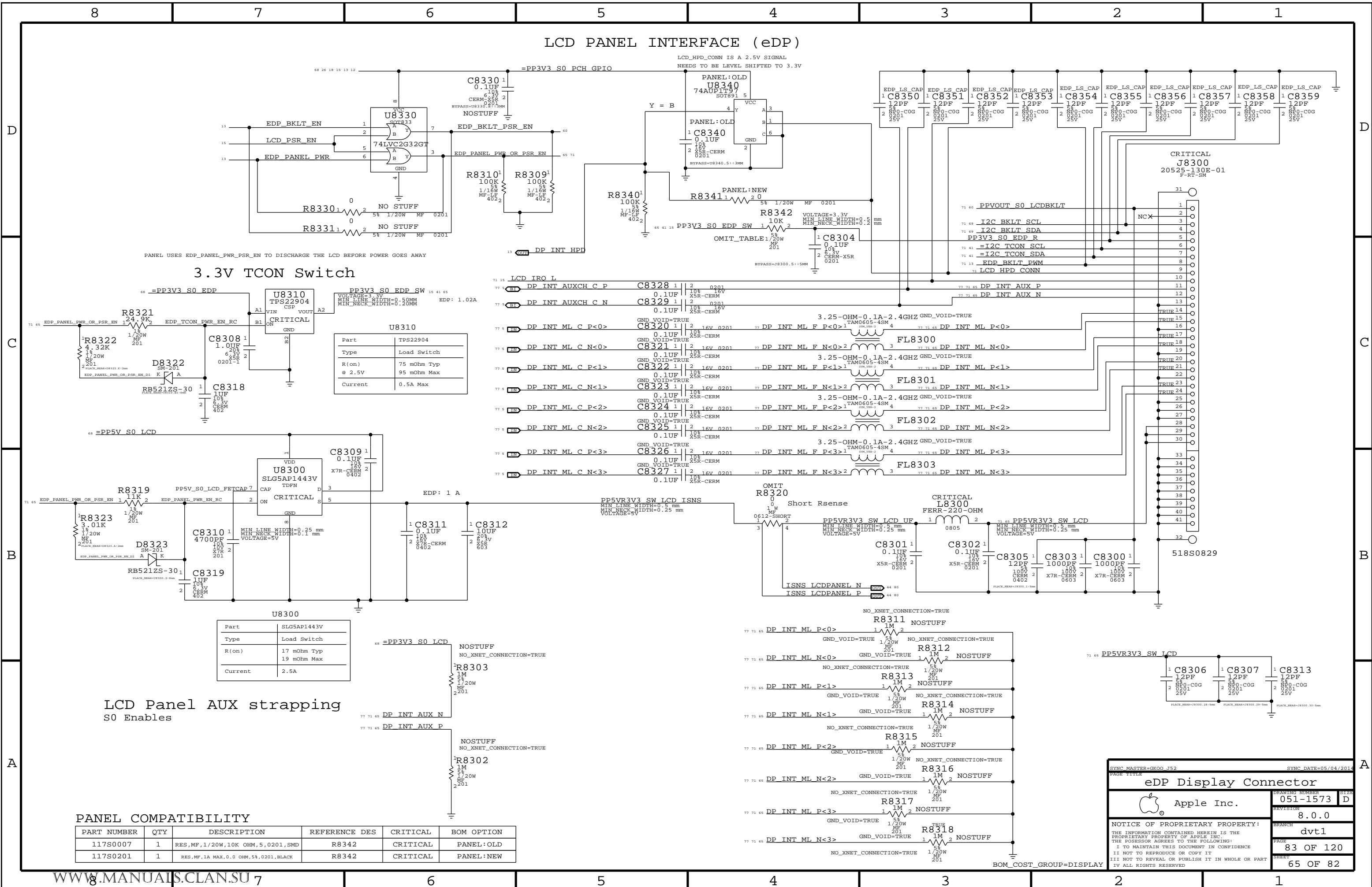
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BOM_COST_GROUP=POWER

LCD PANEL INTERFACE (eDP)



3.3V TCON Switch

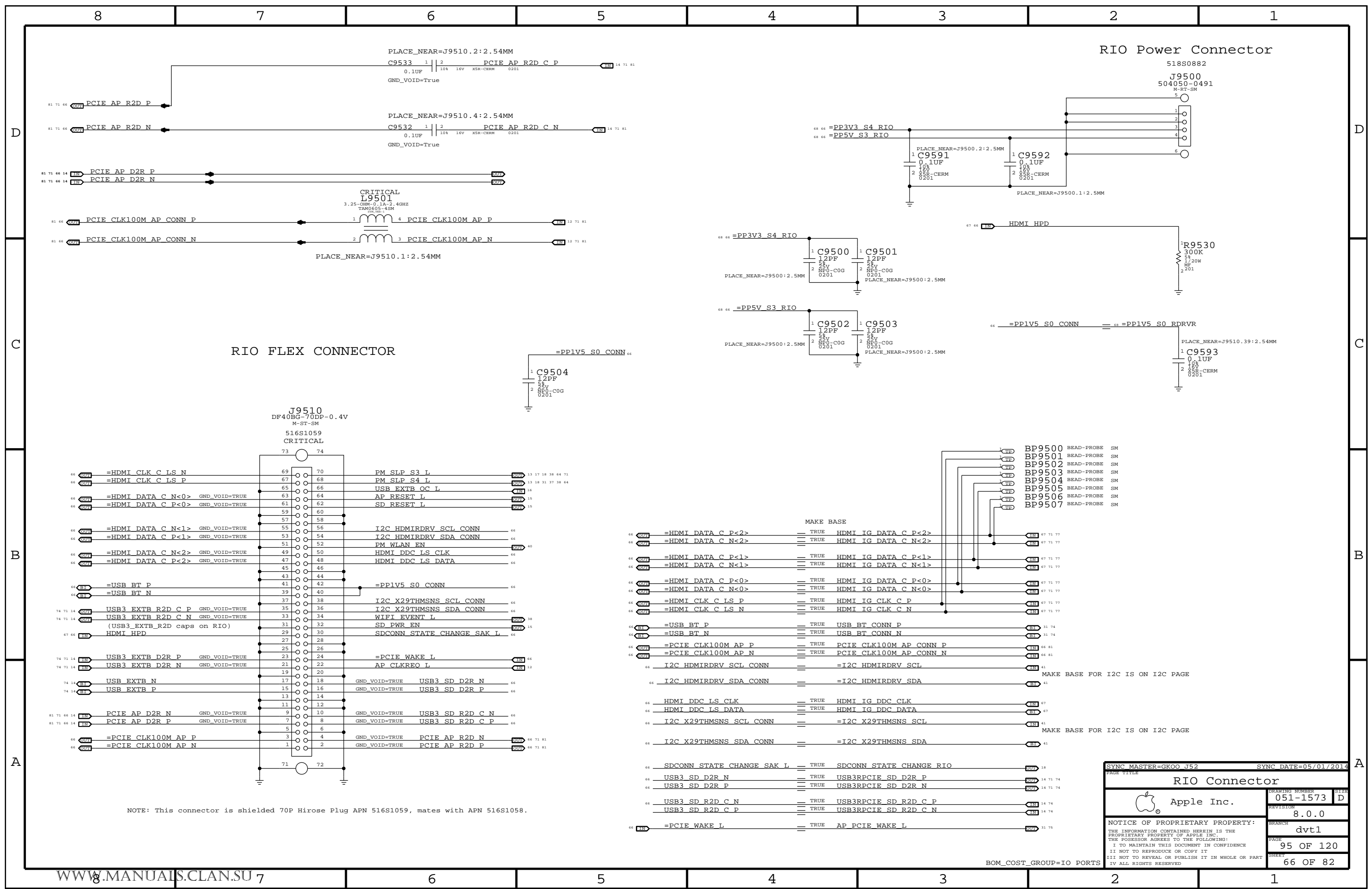
Part	TPS22904
Type	Load Switch
R(on)	75 mOhm Typ 95 mOhm Max
Current	0.5A Max

LCD Panel AUX strapping S0 Enables

PANEL COMPATIBILITY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0007	1	RES, MF, 1/20W, 10K OHM, 5, 0201, SMD	R8342	CRITICAL	PANEL:OLD
117S0201	1	RES, MF, 1A MAX, 0.0 OHM, 5K, 0201, BLACK	R8342	CRITICAL	PANEL:NEW

SYNC MASTER=GK00_J52		SYNC DATE=05/04/2011	
PAGE TITLE			
eDP Display Connector		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
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		8.0.0	dvt1
		PAGE	SHEET
		83 OF 120	65 OF 82



RIO FLEX CONNECTOR

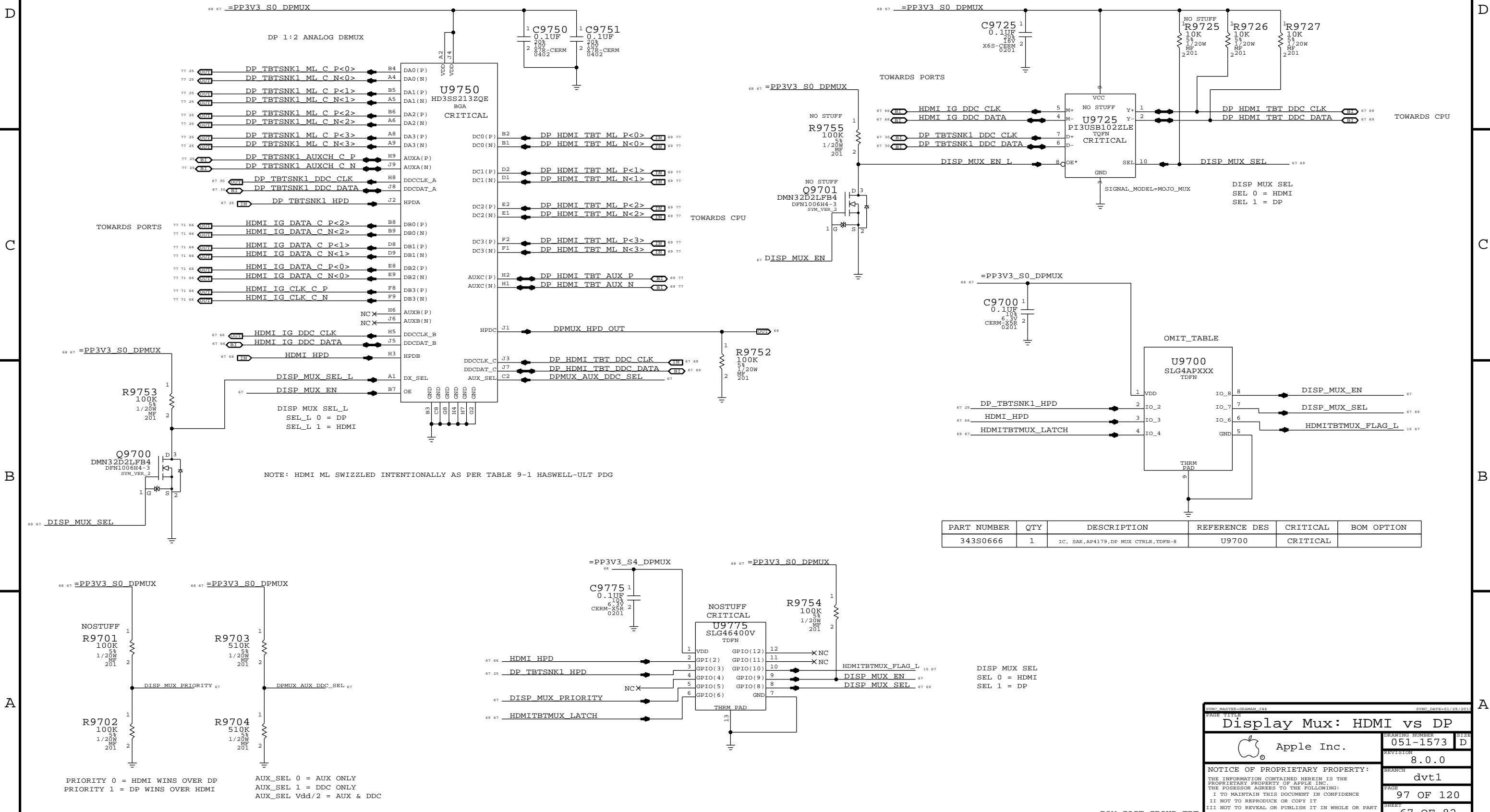
RIO Power Connector

NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.

SYNC MASTER=GK00 J52		SYNC DATE=05/01/2014	
PAGE TITLE			
RIO Connector			
		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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		PAGE	95 OF 120
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BOM_COST_GROUP=IO PORTS

DISPLAY MUX: DP OR HDMI



NOTE: HDMI ML SWIZZLED INTENTIONALLY AS PER TABLE 9-1 HASWELL-ULT PDG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0666	1	IC, SAK,AP4179,DP MUX CTRLR,TDFN-8	U9700	CRITICAL	

PRIORITY 0 = HDMI WINS OVER DP
 PRIORITY 1 = DP WINS OVER HDMI

AUX_SEL 0 = AUX ONLY
 AUX_SEL 1 = DDC ONLY
 AUX_SEL Vdd/2 = AUX & DDC

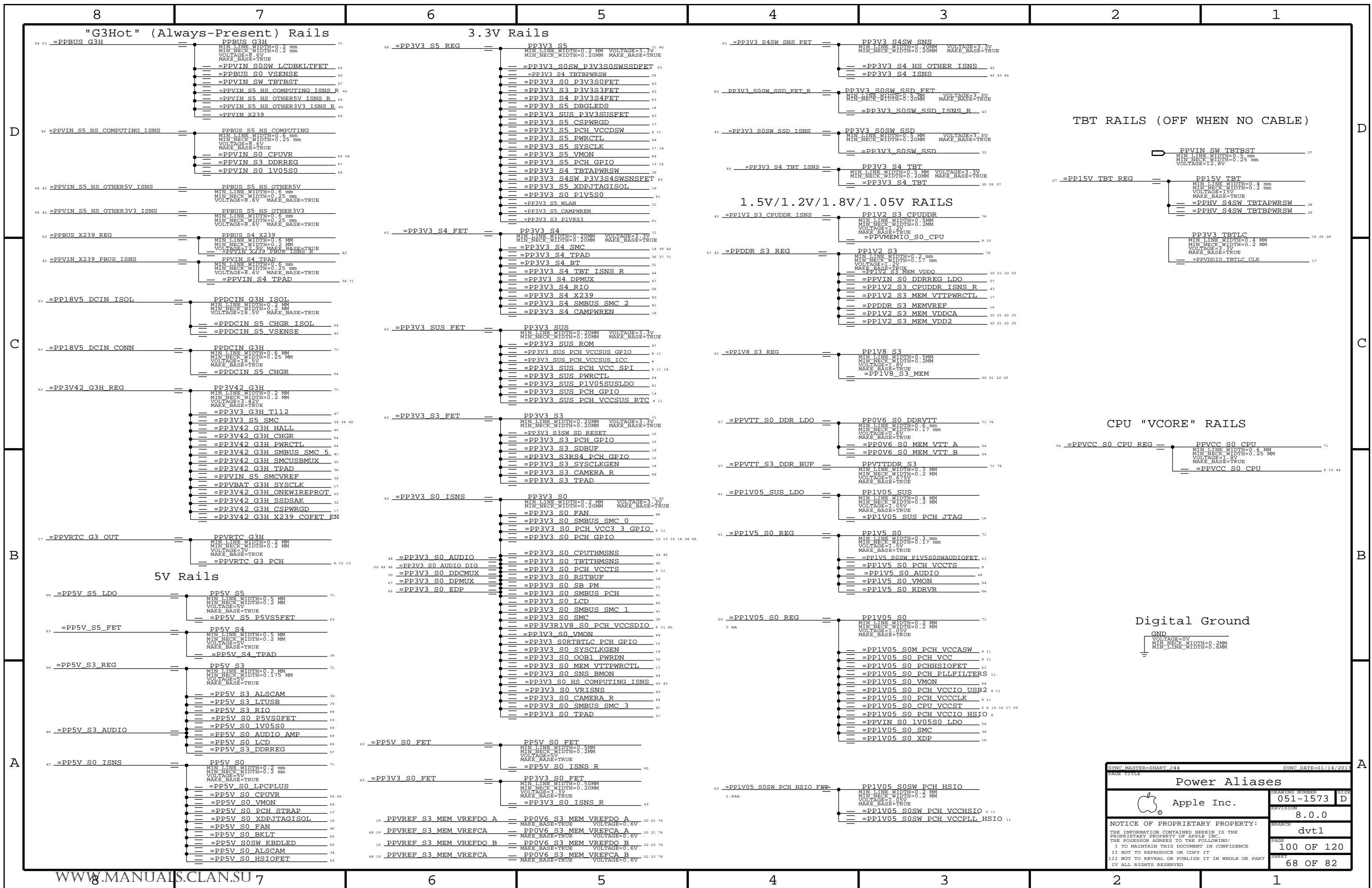
DISP MUX SEL
 SEL 0 = HDMI
 SEL 1 = DP

Display Mux: HDMI vs DP

Apple Inc.

DRAWING NUMBER: 051-1573
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"G3Hot" (Always-Present) Rails

3.3V Rails

1.5V/1.2V/1.8V/1.05V RAILS

5V Rails

TBT RAILS (OFF WHEN NO CABLE)

CPU "Vcore" RAILS

Digital Ground

SYNC MASTER=SHART J44		SYNC DATE=01/14/2013	
PAGE TITLE			
Power Aliases		DRAWING NUMBER	SIZE
Apple Inc.		051-1573	D
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		8.0.0	
		BRANCH	
		dvt1	
		PAGE	
		100 OF 120	
		SHEET	
		68 OF 82	

HDMI VS TBT

```

MAKE_BASE
5 =DP TBTSNK1 ML C P<0> == TRUE DP HDMI TBT ML P<0> 67 77
5 =DP TBTSNK1 ML C N<0> == TRUE DP HDMI TBT ML N<0> 67 77
5 =DP TBTSNK1 ML C P<1> == TRUE DP HDMI TBT ML P<1> 67 77
5 =DP TBTSNK1 ML C N<1> == TRUE DP HDMI TBT ML N<1> 67 77
5 =DP TBTSNK1 ML C P<2> == TRUE DP HDMI TBT ML P<2> 67 77
5 =DP TBTSNK1 ML C N<2> == TRUE DP HDMI TBT ML N<2> 67 77
5 =DP TBTSNK1 ML C P<3> == TRUE DP HDMI TBT ML P<3> 67 77
5 =DP TBTSNK1 ML C N<3> == TRUE DP HDMI TBT ML N<3> 67 77
13 =DP TBTSNK1 AUXCH C P == TRUE DP HDMI TBT AUX P 67 77
13 =DP TBTSNK1 AUXCH C N == TRUE DP HDMI TBT AUX N 67 77
13 =DP TBTSNK1 DDC CLK == TRUE DP HDMI TBT DDC CLK 67
13 =DP TBTSNK1 DDC DATA == TRUE DP HDMI TBT DDC DATA 67
13 =DP TBTSNK1 HPD == TRUE DPMUX HPD OUT 67

```

```

25 HDMITBTMUX SEL TBT == TBT GO2SX BIDIR 15
MAKE_BASE=TRUE
DISP_MUX_SEL 67
13 DP AUXCH ISOL L == HDMITBTMUX LATCH 67
MAKE_BASE=TRUE

```

EPD PANEL

```

MAKE_BASE
60 =I2C BKLT_SCL == TRUE I2C BKLT_SCL 65 71
60 =I2C BKLT_SDA == TRUE I2C BKLT_SDA 65 71

```

UNUSED SIGNALS

```

MAKE_BASE
12 TP PCIE CLK100M_FWP == TRUE NO_TEST=TRUE NC PCIE CLK100M_FWP
12 TP PCIE CLK100M_FWN == TRUE NO_TEST=TRUE NC PCIE CLK100M_FWN
14 TP PCIE FW_D2RP == TRUE NO_TEST=TRUE NC PCIE FW_D2RP
14 TP PCIE FW_D2RN == TRUE NO_TEST=TRUE NC PCIE FW_D2RN
14 TP PCIE FW_R2D_CP == TRUE NO_TEST=TRUE NC PCIE FW_R2D_CP
14 TP PCIE FW_R2D_CN == TRUE NO_TEST=TRUE NC PCIE FW_R2D_CN
13 TP PCIE CLK100M_ENETSDP == TRUE NO_TEST=TRUE NC PCIE CLK100M_ENETSDP
13 TP PCIE CLK100M_ENETSDN == TRUE NO_TEST=TRUE NC PCIE CLK100M_ENETSDN
14 USB_IR_P == TRUE NO_TEST=TRUE NC USB_IRP 74
14 USB_IR_N == TRUE NO_TEST=TRUE NC USB_IRN 74
14 TP_USB_CAMERAP == TRUE NO_TEST=TRUE NC_USB_CAMERAP 74
14 TP_USB_CAMERAN == TRUE NO_TEST=TRUE NC_USB_CAMERAN 74
14 TP_USB_SDP == TRUE NO_TEST=TRUE NC_USB_SDP 74
14 TP_USB_SDN == TRUE NO_TEST=TRUE NC_USB_SDN 74
12 TP_HDA_SDIN1 == TRUE NO_TEST=TRUE NC_HDA_SDIN1
12 TP_PCI_PME_L == TRUE NO_TEST=TRUE NC_PCI_PME_L
14 TP_CLINK_CLK == TRUE NO_TEST=TRUE NC_CLINK_CLK
14 TP_CLINK_DATA == TRUE NO_TEST=TRUE NC_CLINK_DATA
14 TP_CLINK_RESET_L == TRUE NO_TEST=TRUE NC_CLINK_RESET_L
12 TP_ITPXDP_CLK100MN == TRUE NO_TEST=TRUE NC_ITPXDP_CLK100MN
12 TP_ITPXDP_CLK100MP == TRUE NO_TEST=TRUE NC_ITPXDP_CLK100MP
12 TP_PCH_I2S1_TXD == TRUE NO_TEST=TRUE NC_PCH_I2S1_TXD
12 TP_PCH_I2S1_SFRM == TRUE NO_TEST=TRUE NC_PCH_I2S1_SFRM
12 TP_PCH_I2S1_SCLK == TRUE NO_TEST=TRUE NC_PCH_I2S1_SCLK
13 TP_PCH_SLP_WLAN_L == TRUE NO_TEST=TRUE NC_PCH_SLP_WLAN_L
13 TP_PCH_SLP_LAN_L == TRUE NO_TEST=TRUE NC_PCH_SLP_LAN_L
14 TP_SPI_CS1_L == TRUE NO_TEST=TRUE NC_SPI_CS1_L
14 TP_SPI_CS2_L == TRUE NO_TEST=TRUE NC_SPI_CS2_L
14 TP_USB_5N == TRUE NO_TEST=TRUE NC_USB_5N 74
14 TP_USB_5P == TRUE NO_TEST=TRUE NC_USB_5P 74
48 TP_AUD_CODEC_MICBIAS1_L == TRUE NO_TEST=TRUE NC_AUD_CODEC_MICBIAS1_L
48 TP_AUD_CODEC_MICBIAS1_R == TRUE NO_TEST=TRUE NC_AUD_CODEC_MICBIAS1_R
48 TP_AUD_CODEC_MICBIAS2_L == TRUE NO_TEST=TRUE NC_AUD_CODEC_MICBIAS2_L
48 TP_AUD_CODEC_MICBIAS2_R == TRUE NO_TEST=TRUE NC_AUD_CODEC_MICBIAS2_R
64 TP_SUS_PGOOD_MR_L == TRUE NO_TEST=TRUE NC_SUS_PGOOD_MR_L
TP_SMC_TRST_L == TRUE NO_TEST=TRUE NC_SMC_TRST_L
TP_SMC_MD1 == TRUE NO_TEST=TRUE NC_SMC_MD1
53 TP_TDM_ONEWIRE_MPM == TRUE NO_TEST=TRUE NC_TDM_ONEWIRE_MPM

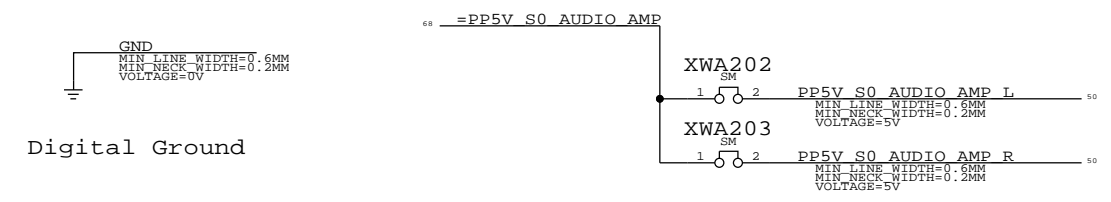
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TBT UNUSED NETS

```

25 TP_TBT_MONDC0 == TRUE NC_TBT_MONDC0
25 TP_TBT_MONDC1 == TRUE NC_TBT_MONDC1
25 TP_TBT_PCIE_RESET0_L == TRUE NC_TBT_PCIE_RESET0_L
25 TP_TBT_XTAL25OUT == TRUE NC_TBT_XTAL25OUT
25 TP_DP_TBTSRC_ML_CP<3> == TRUE NC_DP_TBTSRC_ML_CP<3>
25 TP_DP_TBTSRC_ML_CN<3> == TRUE NC_DP_TBTSRC_ML_CN<3>
25 TP_DP_TBTSRC_ML_CP<2> == TRUE NC_DP_TBTSRC_ML_CP<2>
25 TP_DP_TBTSRC_ML_CN<2> == TRUE NC_DP_TBTSRC_ML_CN<2>
25 TP_DP_TBTSRC_ML_CP<1> == TRUE NC_DP_TBTSRC_ML_CP<1>
25 TP_DP_TBTSRC_ML_CN<1> == TRUE NC_DP_TBTSRC_ML_CN<1>
25 TP_DP_TBTSRC_ML_CP<0> == TRUE NC_DP_TBTSRC_ML_CP<0>
25 TP_DP_TBTSRC_ML_CN<0> == TRUE NC_DP_TBTSRC_ML_CN<0>
25 TP_DP_TBTSRC_AUXCH_CP == TRUE NC_DP_TBTSRC_AUXCH_CP
25 TP_DP_TBTSRC_AUXCH_CN == TRUE NC_DP_TBTSRC_AUXCH_CN

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SYNC MASTER=SHART_344		SYNC DATE=11/19/2012	
PAGE TITLE			
Signal Aliases			
		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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LPDDR3 COMMAND/ADDRESS

	MAKE_BASE		
7	==MEM A A<5>	== TRUE	MEM A CAA<0>
7	==MEM A A<9>	== TRUE	MEM A CAA<1>
7	==MEM A A<6>	== TRUE	MEM A CAA<2>
7	==MEM A A<8>	== TRUE	MEM A CAA<3>
7	==MEM A A<7>	== TRUE	MEM A CAA<4>
7	==MEM A BA<2>	== TRUE	MEM A CAA<5>
7	==MEM A A<12>	== TRUE	MEM A CAA<6>
7	==MEM A A<11>	== TRUE	MEM A CAA<7>
7	==MEM A A<15>	== TRUE	MEM A CAA<8>
7	==MEM A A<14>	== TRUE	MEM A CAA<9>
7	==MEM A A<13>	== TRUE	MEM A CAB<0>
7	==MEM A CAS L	== TRUE	MEM A CAB<1>
7	==MEM A WE L	== TRUE	MEM A CAB<2>
7	==MEM A RAS L	== TRUE	MEM A CAB<3>
7	==MEM A BA<0>	== TRUE	MEM A CAB<4>
7	==MEM A A<2>	== TRUE	MEM A CAB<5>
7	==MEM A BA<1>	== TRUE	MEM A CAB<6>
7	==MEM A A<10>	== TRUE	MEM A CAB<7>
7	==MEM A A<1>	== TRUE	MEM A CAB<8>
7	==MEM A A<0>	== TRUE	MEM A CAB<9>
7	==MEM A ODT<0>	== TRUE	MEM A ODT<0>
7	==MEM A A<3>	== TRUE	TP LPDDR3 RSVD1
7	==MEM A A<4>	== TRUE	TP LPDDR3 RSVD2
7	==MEM B A<5>	== TRUE	MEM B CAA<0>
7	==MEM B A<9>	== TRUE	MEM B CAA<1>
7	==MEM B A<6>	== TRUE	MEM B CAA<2>
7	==MEM B A<8>	== TRUE	MEM B CAA<3>
7	==MEM B A<7>	== TRUE	MEM B CAA<4>
7	==MEM B BA<2>	== TRUE	MEM B CAA<5>
7	==MEM B A<12>	== TRUE	MEM B CAA<6>
7	==MEM B A<11>	== TRUE	MEM B CAA<7>
7	==MEM B A<15>	== TRUE	MEM B CAA<8>
7	==MEM B A<14>	== TRUE	MEM B CAA<9>
7	==MEM B A<13>	== TRUE	MEM B CAB<0>
7	==MEM B CAS L	== TRUE	MEM B CAB<1>
7	==MEM B WE L	== TRUE	MEM B CAB<2>
7	==MEM B RAS L	== TRUE	MEM B CAB<3>
7	==MEM B BA<0>	== TRUE	MEM B CAB<4>
7	==MEM B A<2>	== TRUE	MEM B CAB<5>
7	==MEM B BA<1>	== TRUE	MEM B CAB<6>
7	==MEM B A<10>	== TRUE	MEM B CAB<7>
7	==MEM B A<1>	== TRUE	MEM B CAB<8>
7	==MEM B A<0>	== TRUE	MEM B CAB<9>
7	==MEM B ODT<0>	== TRUE	MEM B ODT<0>
7	==MEM B A<3>	== TRUE	TP LPDDR3 RSVD3
7	==MEM B A<4>	== TRUE	TP LPDDR3 RSVD4

UNUSED MEMORY SIGNALS

	MAKE_BASE	
7	==MEM RESET L	== TRUE TP CPU MEM RESET L

20	==MEM A DOS P<0>	== TRUE	MEM A DOS P<0>
20	==MEM A DOS N<0>	== TRUE	MEM A DOS N<0>
20	==MEM A DOS P<1>	== TRUE	MEM A DOS P<1>
20	==MEM A DOS N<1>	== TRUE	MEM A DOS N<1>
20	==MEM A DOS P<2>	== TRUE	MEM A DOS P<2>
20	==MEM A DOS N<2>	== TRUE	MEM A DOS N<2>
20	==MEM A DOS P<3>	== TRUE	MEM A DOS P<3>
20	==MEM A DOS N<3>	== TRUE	MEM A DOS N<3>
20	==MEM A DOS P<4>	== TRUE	MEM A DOS P<4>
20	==MEM A DOS N<4>	== TRUE	MEM A DOS N<4>
20	==MEM A DOS P<5>	== TRUE	MEM A DOS P<5>
20	==MEM A DOS N<5>	== TRUE	MEM A DOS N<5>
20	==MEM A DOS P<6>	== TRUE	MEM A DOS P<6>
20	==MEM A DOS N<6>	== TRUE	MEM A DOS N<6>
20	==MEM A DOS P<7>	== TRUE	MEM A DOS P<7>
20	==MEM A DOS N<7>	== TRUE	MEM A DOS N<7>
20	==MEM A DOS P<8>	== TRUE	MEM A DOS P<8>
20	==MEM A DOS N<8>	== TRUE	MEM A DOS N<8>

22	==MEM B DOS P<0>	== TRUE	MEM B DOS P<0>
22	==MEM B DOS N<0>	== TRUE	MEM B DOS N<0>
22	==MEM B DOS P<1>	== TRUE	MEM B DOS P<1>
22	==MEM B DOS N<1>	== TRUE	MEM B DOS N<1>
22	==MEM B DOS P<2>	== TRUE	MEM B DOS P<2>
22	==MEM B DOS N<2>	== TRUE	MEM B DOS N<2>
22	==MEM B DOS P<3>	== TRUE	MEM B DOS P<3>
22	==MEM B DOS N<3>	== TRUE	MEM B DOS N<3>
22	==MEM B DOS P<4>	== TRUE	MEM B DOS P<4>
22	==MEM B DOS N<4>	== TRUE	MEM B DOS N<4>
22	==MEM B DOS P<5>	== TRUE	MEM B DOS P<5>
22	==MEM B DOS N<5>	== TRUE	MEM B DOS N<5>
22	==MEM B DOS P<6>	== TRUE	MEM B DOS P<6>
22	==MEM B DOS N<6>	== TRUE	MEM B DOS N<6>
22	==MEM B DOS P<7>	== TRUE	MEM B DOS P<7>
22	==MEM B DOS N<7>	== TRUE	MEM B DOS N<7>

Memory Bit/Byte Swizzle

76 71 7	MEM A DQ<0>	==	==MEM A DQ<7>	76 71 7	MEM B DQ<0>	==	==MEM B DQ<7>
76 71 7	MEM A DQ<1>	==	==MEM A DQ<6>	76 71 7	MEM B DQ<1>	==	==MEM B DQ<6>
76 71 7	MEM A DQ<2>	==	==MEM A DQ<5>	76 71 7	MEM B DQ<2>	==	==MEM B DQ<5>
76 71 7	MEM A DQ<3>	==	==MEM A DQ<4>	76 71 7	MEM B DQ<3>	==	==MEM B DQ<4>
76 71 7	MEM A DQ<4>	==	==MEM A DQ<3>	76 71 7	MEM B DQ<4>	==	==MEM B DQ<3>
76 71 7	MEM A DQ<5>	==	==MEM A DQ<2>	76 71 7	MEM B DQ<5>	==	==MEM B DQ<2>
76 71 7	MEM A DQ<6>	==	==MEM A DQ<1>	76 71 7	MEM B DQ<6>	==	==MEM B DQ<1>
76 71 7	MEM A DQ<7>	==	==MEM A DQ<0>	76 71 7	MEM B DQ<7>	==	==MEM B DQ<0>
76 71 7	MEM A DQ<8>	==	==MEM A DQ<10>	76 71 7	MEM B DQ<8>	==	==MEM B DQ<4>
76 71 7	MEM A DQ<9>	==	==MEM A DQ<14>	76 71 7	MEM B DQ<9>	==	==MEM B DQ<14>
76 71 7	MEM A DQ<10>	==	==MEM A DQ<8>	76 71 7	MEM B DQ<10>	==	==MEM B DQ<8>
76 71 7	MEM A DQ<11>	==	==MEM A DQ<9>	76 71 7	MEM B DQ<11>	==	==MEM B DQ<9>
76 71 7	MEM A DQ<12>	==	==MEM A DQ<15>	76 71 7	MEM B DQ<12>	==	==MEM B DQ<15>
76 71 7	MEM A DQ<13>	==	==MEM A DQ<11>	76 71 7	MEM B DQ<13>	==	==MEM B DQ<11>
76 71 7	MEM A DQ<14>	==	==MEM A DQ<12>	76 71 7	MEM B DQ<14>	==	==MEM B DQ<12>
76 71 7	MEM A DQ<15>	==	==MEM A DQ<13>	76 71 7	MEM B DQ<15>	==	==MEM B DQ<13>
76 71 7	MEM A DQ<16>	==	==MEM A DQ<21>	76 71 7	MEM B DQ<16>	==	==MEM B DQ<22>
76 71 7	MEM A DQ<17>	==	==MEM A DQ<16>	76 71 7	MEM B DQ<17>	==	==MEM B DQ<18>
76 71 7	MEM A DQ<18>	==	==MEM A DQ<23>	76 71 7	MEM B DQ<18>	==	==MEM B DQ<17>
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76 71 7	MEM A DQ<20>	==	==MEM A DQ<19>	76 71 7	MEM B DQ<20>	==	==MEM B DQ<23>
76 71 7	MEM A DQ<21>	==	==MEM A DQ<22>	76 71 7	MEM B DQ<21>	==	==MEM B DQ<19>
76 71 7	MEM A DQ<22>	==	==MEM A DQ<17>	76 71 7	MEM B DQ<22>	==	==MEM B DQ<20>
76 71 7	MEM A DQ<23>	==	==MEM A DQ<20>	76 71 7	MEM B DQ<23>	==	==MEM B DQ<21>
76 71 7	MEM A DQ<24>	==	==MEM A DQ<27>	76 71 7	MEM B DQ<24>	==	==MEM B DQ<27>
76 71 7	MEM A DQ<25>	==	==MEM A DQ<26>	76 71 7	MEM B DQ<25>	==	==MEM B DQ<26>
76 71 7	MEM A DQ<26>	==	==MEM A DQ<25>	76 71 7	MEM B DQ<26>	==	==MEM B DQ<24>
76 71 7	MEM A DQ<27>	==	==MEM A DQ<29>	76 71 7	MEM B DQ<27>	==	==MEM B DQ<28>
76 71 7	MEM A DQ<28>	==	==MEM A DQ<30>	76 71 7	MEM B DQ<28>	==	==MEM B DQ<31>
76 71 7	MEM A DQ<29>	==	==MEM A DQ<31>	76 71 7	MEM B DQ<29>	==	==MEM B DQ<30>
76 71 7	MEM A DQ<30>	==	==MEM A DQ<24>	76 71 7	MEM B DQ<30>	==	==MEM B DQ<29>
76 71 7	MEM A DQ<31>	==	==MEM A DQ<28>	76 71 7	MEM B DQ<31>	==	==MEM B DQ<25>
76 71 7	MEM A DQ<32>	==	==MEM A DQ<38>	76 71 7	MEM B DQ<32>	==	==MEM B DQ<39>
76 71 7	MEM A DQ<33>	==	==MEM A DQ<39>	76 71 7	MEM B DQ<33>	==	==MEM B DQ<38>
76 71 7	MEM A DQ<34>	==	==MEM A DQ<37>	76 71 7	MEM B DQ<34>	==	==MEM B DQ<37>
76 71 7	MEM A DQ<35>	==	==MEM A DQ<33>	76 71 7	MEM B DQ<35>	==	==MEM B DQ<33>
76 71 7	MEM A DQ<36>	==	==MEM A DQ<35>	76 71 7	MEM B DQ<36>	==	==MEM B DQ<35>
76 71 7	MEM A DQ<37>	==	==MEM A DQ<34>	76 71 7	MEM B DQ<37>	==	==MEM B DQ<34>
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76 71 7	MEM A DQ<39>	==	==MEM A DQ<36>	76 71 7	MEM B DQ<39>	==	==MEM B DQ<36>
76 71 7	MEM A DQ<40>	==	==MEM A DQ<42>	76 71 7	MEM B DQ<40>	==	==MEM B DQ<42>
76 71 7	MEM A DQ<41>	==	==MEM A DQ<46>	76 71 7	MEM B DQ<41>	==	==MEM B DQ<46>
76 71 7	MEM A DQ<42>	==	==MEM A DQ<40>	76 71 7	MEM B DQ<42>	==	==MEM B DQ<40>
76 71 7	MEM A DQ<43>	==	==MEM A DQ<41>	76 71 7	MEM B DQ<43>	==	==MEM B DQ<41>
76 71 7	MEM A DQ<44>	==	==MEM A DQ<47>	76 71 7	MEM B DQ<44>	==	==MEM B DQ<47>
76 71 7	MEM A DQ<45>	==	==MEM A DQ<43>	76 71 7	MEM B DQ<45>	==	==MEM B DQ<43>
76 71 7	MEM A DQ<46>	==	==MEM A DQ<44>	76 71 7	MEM B DQ<46>	==	==MEM B DQ<44>
76 71 7	MEM A DQ<47>	==	==MEM A DQ<45>	76 71 7	MEM B DQ<47>	==	==MEM B DQ<45>
76 71 7	MEM A DQ<48>	==	==MEM A DQ<61>	76 71 7	MEM B DQ<48>	==	==MEM B DQ<53>
76 71 7	MEM A DQ<49>	==	==MEM A DQ<60>	76 71 7	MEM B DQ<49>	==	==MEM B DQ<55>
76 71 7	MEM A DQ<50>	==	==MEM A DQ<58>	76 71 7	MEM B DQ<50>	==	==MEM B DQ<49>
76 71 7	MEM A DQ<51>	==	==MEM A DQ<62>	76 71 7	MEM B DQ<51>	==	==MEM B DQ<54>
76 71 7	MEM A DQ<52>	==	==MEM A DQ<63>	76 71 7	MEM B DQ<52>	==	==MEM B DQ<51>
76 71 7	MEM A DQ<53>	==	==MEM A DQ<59>	76 71 7	MEM B DQ<53>	==	==MEM B DQ<52>
76 71 7	MEM A DQ<54>	==	==MEM A DQ<57>	76 71 7	MEM B DQ<54>	==	==MEM B DQ<48>
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76 71 7	MEM A DQ<57>	==	==MEM A DQ<49>	76 71 7	MEM B DQ<57>	==	==MEM B DQ<63>
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76 71 7	MEM A DQ<62>	==	==MEM A DQ<54>	76 71 7	MEM B DQ<62>	==	==MEM B DQ<58>
76 71 7	MEM A DQ<63>	==	==MEM A DQ<50>	76 71 7	MEM B DQ<63>	==	==MEM B DQ<59>

SYNC MASTER=AHARTMAN_552 SYNC DATE=10/29/2013

Memory Bit & Byte Swizzle

Apple Inc.

DRAWING NUMBER: 051-1573 SIZE: D

REVISION: 8.0.0

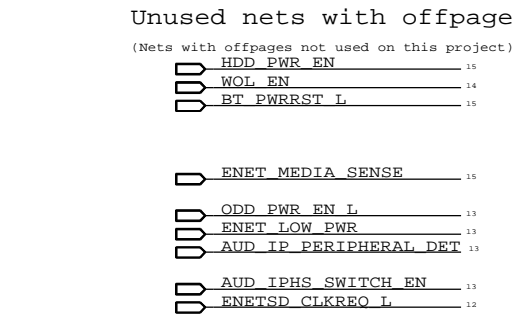
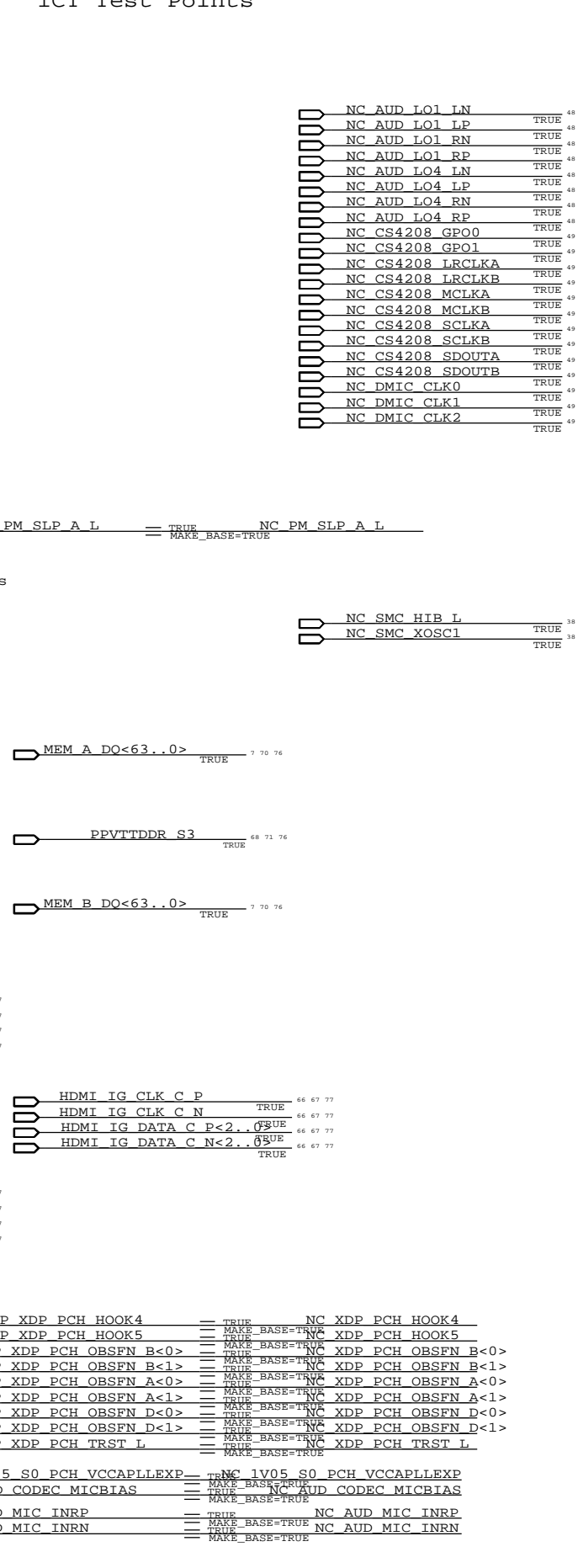
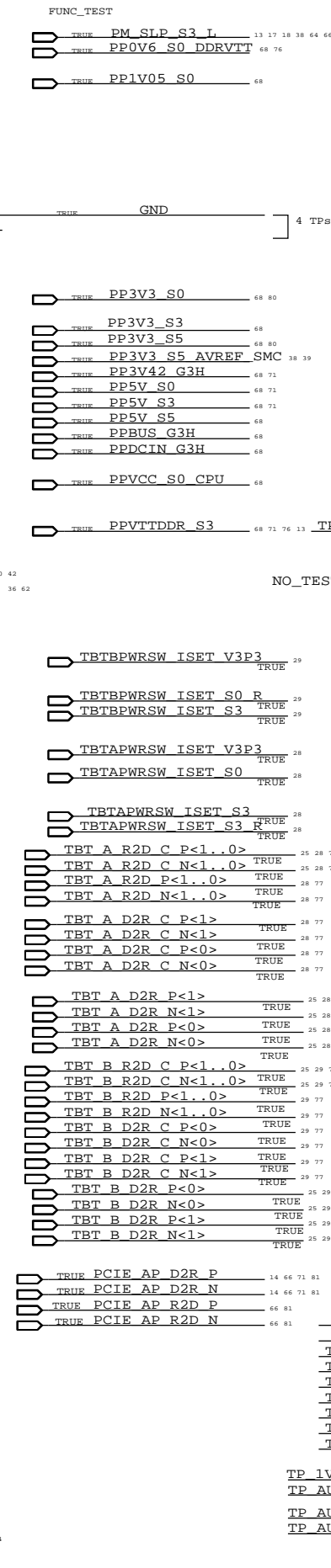
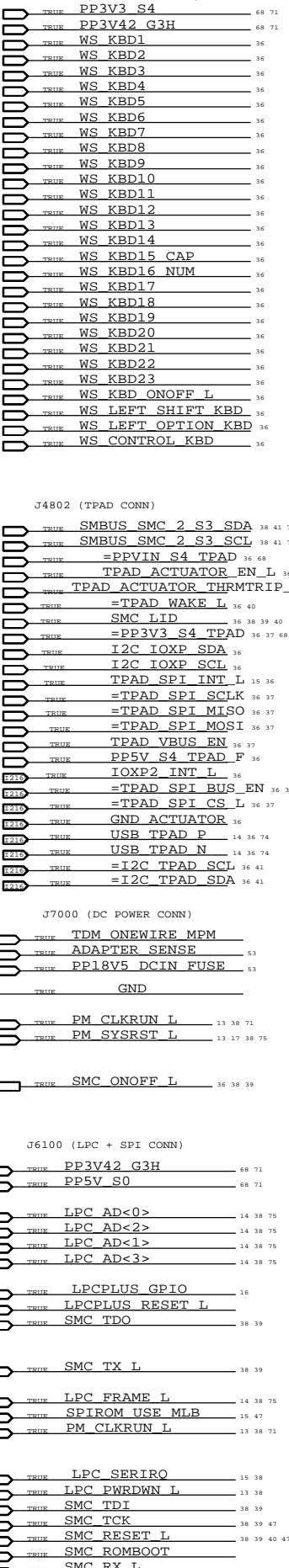
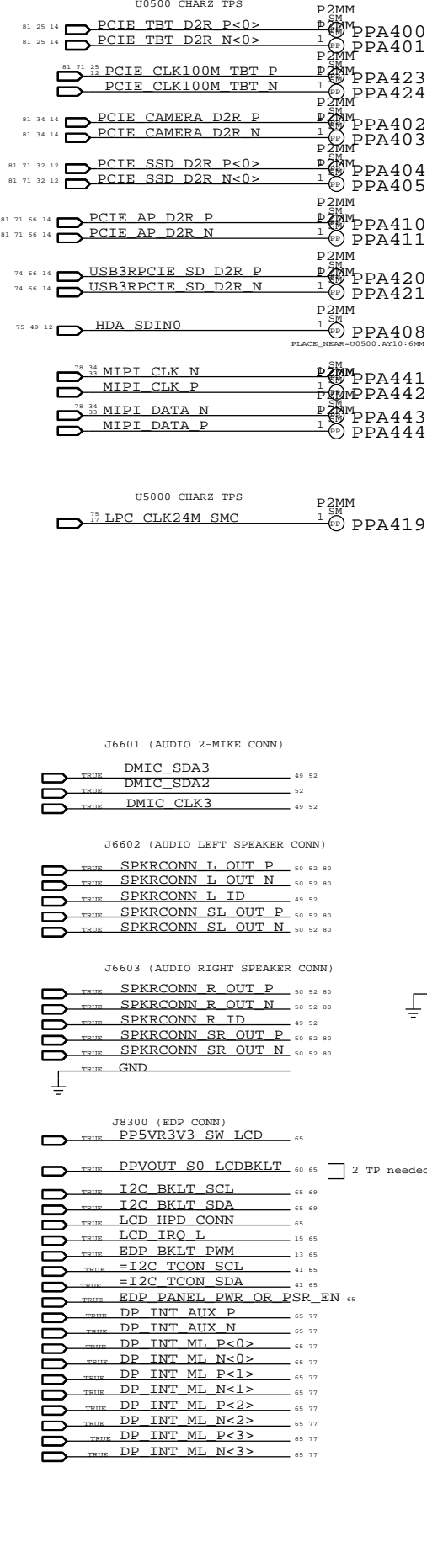
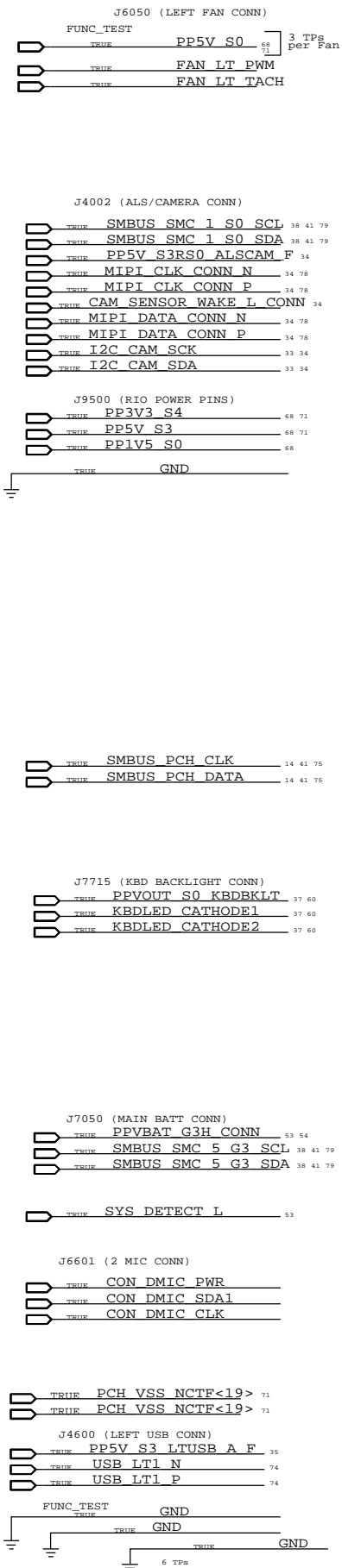
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Functional Test Points



Functional & ICT Test

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X304 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, P65BGA, BGA_MEM			MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.155 MM	0.155 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
73_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	ISL2, ISL11	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.141 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2, ISL11, ISL12, ISL13, ISL14, ISL15, ISL16, ISL17, ISL18, ISL19, ISL20	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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PAGE TITLE			
PCB Rule Definitions			SIZE
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
XDP_TCK0	CPU_45S	CPU_18MIL	XDP CPU TCK	6 16
XDP_TCK0	CPU_45S	CPU_18MIL	PCH JTAGX	12 16
XDP_TCK1	CPU_45S	CPU_18MIL	XDP PCH TCK	12 16
XDP_TDO	CPU_45S		XDP CPU TDO	6 16
XDP_TDO	CPU_45S		XDP PCH TDO	12 16
XDP_TDI	CPU_45S		XDP CPU TDI	6 16
XDP_TDI	CPU_45S		XDP PCH TDI	12 16
XDP_TMS	CPU_45S		XDP CPU TMS	6 16
XDP_TMS	CPU_45S		XDP PCH TMS	12 16
XDP_TRST_L	CPU_45S		XDP TRST L	16
XDP_TRST_L	CPU_45S		XDP CPUPCH TRST L	16
XDP_PRDY_L	CPU_45S		XDP CPU PRDY L	6 16
XDP_PREQ_L	CPU_45S		XDP CPU PREQ L	6 16
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	CPU VCCST_PWRGD	8 16 17
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	XDP CPU VCCST_PWRGD	16
CPU_BPM	CPU_45S	CPU_08MIL	XDP BPM L<1..0>	6 16
CPU_BPM_TP	CPU_45S		XDP BPM L<7..2>	6 16
CPU_RCOMP_SM	CPU_27P4S	CPU_25MIL	CPU SM RCOMP<2..0>	6
CPU_RCOMP_EDP	CPU_27P4S	CPU_25MIL	MCP EDP RCOMP	6
CPU_RCOMP_OPI	CPU_27P4S	CPU_12MIL	CPU OPI RCOMP	6
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU PROCHOT L	6 38 39 55
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU PROCHOT R L	6
CPU_CATERR	CPU_45S	CPU_08MIL	CPU CATERR L	6 38
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU VIDALERT L	8 55
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU VIDALERT R L	8
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU VIDSCLK	8 55
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU VIDSCLK R	8
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU VIDSOUT	8 55
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU VIDSOUT R	8
CPU_PECT	CPU_45S	CPU_18MIL	CPU PECT	6 39
CPU_PECT	CPU_45S	CPU_18MIL	CPU PECT R	38 39
CPU_PECT	CPU_45S	CPU_18MIL	SMC PECT L	38 39
CPU_PECT	CPU_45S	CPU_18MIL	SMC PECT L R	39
CPU_CFG	CPU_45S		CPU CFG<19..11>	6 16
CPU_CFG_PD	CPU_45S		CPU CFG<10..8>	6 16
CPU_CFG	CPU_45S		CPU CFG<7..5>	6 16
CPU_CFG_PD	CPU_45S		CPU CFG<4>	6 16
CPU_CFG_3	CPU_45S		CPU CFG<3>	6 16
CPU_CFG	CPU_45S		CPU CFG<2>	6 16
CPU_CFG_PD	CPU_45S		CPU CFG<1..0>	6 16
CPU_MEM_RESET	CPU_45S	CPU_08MIL	MEM RESET L	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	8 55
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	9 55

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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP, BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?	USB_RBIAS	TOP, BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP, BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP, BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP, BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP, BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP, BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?	SATA_2OTHER	TOP, BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
USB_BT	USB_85D	USB	USB BT P	14 31
USB_BT	USB_85D	USB	USB BT N	14 31
USB_BT	USB_85D	USB	USB BT CONN P	31 66
USB_BT	USB_85D	USB	USB BT CONN N	31 66
USB_EXTA	USB_85D	USB	USB EXTA P	14 35
USB_EXTA	USB_85D	USB	USB EXTA N	14 35
DEFAULT	DEFAULT	DEFAULT	SMC DEBUGPRT RX L	35 38 39
DEFAULT	DEFAULT	DEFAULT	SMC DEBUGPRT TX L	35 38 39
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED P	35
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED N	35
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED F P	35
USB_EXTA	USB_85D	USB	USB2 EXTA MUXED F N	35
USB_EXTA	USB_85D	USB	USB LT1 P	71
USB_EXTA	USB_85D	USB	USB LT1 N	71
USB_EXTB	USB_85D	USB	USB EXTB P	14 66
USB_EXTB	USB_85D	USB	USB EXTB N	14 66
USB_TPAD	USB_85D	USB	USB TPAD P	14 36 71
USB_TPAD	USB_85D	USB	USB TPAD N	14 36 71
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3 EXTA D2R P	14 35 71
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3 EXTA D2R N	14 35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D P	35
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D N	35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D C P	14 35 71
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3 EXTA R2D C N	14 35 71
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3 EXTB D2R P	14 66 71
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3 EXTB D2R N	14 66 71
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3 EXTB R2D C P	14 66 71
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3 EXTB R2D C N	14 66 71
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE SD D2R P	14 66 71
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE SD D2R N	14 66 71
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE SD R2D C P	14 66
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE SD R2D C N	14 66
USB_NC	USB_85D	USB	NC USB IRP	69
USB_NC	USB_85D	USB	NC USB IRN	69
USB_NC	USB_85D	USB	NC USB 5P	69
USB_NC	USB_85D	USB	NC USB 5N	69
USB_NC	USB_85D	USB	NC USB SDP	69
USB_NC	USB_85D	USB	NC USB SDN	69
USB_NC	USB_85D	USB	NC USB CAMERAP	69
USB_NC	USB_85D	USB	NC USB CAMERAN	69
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH USB RBIAS	14
SATA_85D	SATA_85D	SATA_RX	DUMMY SATA D2R P	
SATA_85D	SATA_85D	SATA_RX	DUMMY SATA D2R N	
SATA_85D	SATA_85D	SATA_TX	DUMMY SATA R2D P	
SATA_85D	SATA_85D	SATA_TX	DUMMY SATA R2D N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X1	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2 R	17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK CLK25M CAMERA	17 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM CLKP	33 34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP R	34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP	34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM XTALN	34
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M CAM CLKN	33 34
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT	17 25
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT R	25

Notes:
This is here to keep the SATA rules.

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USB Constraints

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 38 71
LPC_AD	LPC_45S	LPC	LPC_FRAME L	14 38 71
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC R	12 17
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 71
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_CLK	14 41 71
SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_DATA	14 41 71
SML_PCH_0	SMB_45S	SMB	SML_PCH_0_CLK	14 41
SML_PCH_0	SMB_45S	SMB	SML_PCH_0_DATA	14 41
	SMB_45S	SMB	SML_PCH_1_CLK	14 41
	SMB_45S	SMB	SML_PCH_1_DATA	14 41
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 49
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 49
HDA_SYNC	HDA_45S	HDA	HDA_SYNC R	12
HDA_RST	HDA_45S	HDA	HDA_RST R L	12
HDA_RST	HDA_45S	HDA	HDA_RST L	12 49
HDA_SDIN	HDA_45S	HDA	HDA_SDIN0	12 49 71
HDA_SDIN	HDA_45S	HDA	CS4208_HDA_SDOUT0 R	49
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 49
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT R	12 17
SPT_MLB	SPT_45S	SPT	SPI_ALT_CLK	47
SPT_MLB	SPT_45S	SPT	SPI_CLK	47
SPT_MLB	SPT_45S	SPT	SPI_CLK R	14 47
SPT_MLB	SPT_45S	SPT	SPI_MLB_CLK	47
SPT_MLB	SPT_45S	SPT	SPI_SMC_CLK	38 47
SPT_MLB	SPT_45S	SPT	SPI_ALT_CS L	47
SPT_MLB	SPT_45S	SPT	SPI_CS0 L	47
SPT_MLB	SPT_45S	SPT	SPI_CS0 R L	14 47
SPT_MLB	SPT_45S	SPT	SPI_MLB_CS L	47
SPT_MLB	SPT_45S	SPT	SPI_SMC_CS L	38 47
SPT_MLB	SPT_45S	SPT	SPI_ALT_IO1_MISO	47
SPT_MLB	SPT_45S	SPT	SPI_MISO	14 47
SPT_MLB	SPT_45S	SPT	SPI_MISO R	47
SPT_MLB	SPT_45S	SPT	SPI_MLB_IO1_MISO	47
SPT_MLB	SPT_45S	SPT	SPI_SMC_MISO	38 47
SPT_MLB	SPT_45S	SPT	SPI_ALT_IO0_MOSI	47
SPT_MLB	SPT_45S	SPT	SPI_MOSI	47
SPT_MLB	SPT_45S	SPT	SPI_MOSI R	14 47
SPT_MLB	SPT_45S	SPT	SPI_MLB_IO0_MOSI	47
SPT_MLB	SPT_45S	SPT	SPI_SMC_MOSI	38 47
SPT_MLB_IO2	SPT_45S	SPT	SPI_IO<2>	14 47
SPT_MLB_IO2	SPT_45S	SPT	SPI_IO2 R	47
SPT_MLB_IO2	SPT_45S	SPT	SPI_MLB_IO2_WP L	47
SPT_MLB_IO2	SPT_45S	SPT	SPI_ALT_IO2_WP L	47
SPT_MLB_IO3	SPT_45S	SPT	SPI_IO<3>	14 47
SPT_MLB_IO3	SPT_45S	SPT	SPI_IO3 R	47
SPT_MLB_IO3	SPT_45S	SPT	SPI_MLB_IO3_HOLD L	47
SPT_MLB_IO3	SPT_45S	SPT	SPI_ALT_IO3_HOLD L	47
SPT_TPAD	SPT_45S	SPT	TPAD_SPI_CLK	15 37
SPT_TPAD_CS	SPT_45S	SPT	TPAD_SPI_CS L	15 37
SPT_TPAD	SPT_45S	SPT	TPAD_SPI_MISO	15 37
SPT_TPAD	SPT_45S	SPT	TPAD_SPI_MOSI	15 37
PCH_RTCX	PCH_45S	PCH_15MTL	PCH_CLK32K_RTCX1	12 17
PCH_SRTCST	PCH_45S	PCH_15MTL	PCH_SRTCST L	12
PCH_RTCRST	PCH_45S	PCH_15MTL	RTC_RESET L	12
PCH_THRMTRIP	PCH_45S	PCH_18MTL	PM_THRMTRIP L	15 39
PCH_THRMTRIP	PCH_45S	PCH_18MTL	PM_THRMTRIP R L	39
	PCH_45S	PCH_15MTL	PCH_INTRUDER L	12
	PCH_45S	PCH_15MTL	PCH_INTVRMEN	12
	PCH_45S	PCH_15MTL	PCH_DSWVRMEN	13
	PCH_45S	PCH_15MTL	PM_RSMRST L	13 44
	PCH_45S	PCH_15MTL	PM_SYSRST L	13 17 38 71
	PCH_45S	PCH_15MTL	XDP_DBRESET L	16 17
	PCH_45S	PCH_15MTL	PM_PCH_SYS_PWROK	13 16 17 38
	PCH_45S	PCH_15MTL	XDP_SYS_PWROK	16
	PCH_45S	PCH_15MTL	SYS_PWROK R	17
	PCH_45S	PCH_15MTL	PM_PCH_PWROK	13 17
	PCH_45S	PCH_15MTL	PM_S0_PGOOD	17
	PCH_45S	PCH_15MTL	SMC_DELAYED_PWRGD	17 26 27 38 39
	PCH_45S	PCH_15MTL	PM_DSW_PWRGD	13 38
	PCH_45S	PCH_15MTL	PM_PWRBTN L	13 16 38
	PCH_45S	PCH_15MTL	XDP_CPU_PWRBTN L	16
	PCH_45S	PCH_15MTL	PCIE_WAKE L	13 31 33
	PCH_45S	PCH_15MTL	AP_PCIE_WAKE L	13 66
	PCH_45S	PCH_15MTL	CAM_PCIE_WAKE L	13
	PCH_45S	PCH_15MTL	TBT_CIO_PLUG_EVENT L	18 25
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALIN	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT R	17
PCH_RCOMP_PCIE	PCH_27P4S	PCH_12MTL	PCH_PCIE_RCOMP	14
PCH_RCOMP_OPI	PCH_27P4S	PCH_12MTL	PCH_OPI_COMP	15
PCH_RCOMP_SATA	PCH_27P4S	PCH_12MTL	PCH_SATA_RCOMP	12

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PCH Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	0.066 MM	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTL	*	=3x_DIELECTRIC	?
MEM_CTL2CTL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_BM	*	=3x_DIELECTRIC	?
MEM_CMD2CTL_BM	*	=3x_DIELECTRIC	?
MEM_CTL2CTL_BM	*	=3x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_BM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_BM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_BM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	BGA_MEM	MEM_73D
MEM_40S	BGA_MEM	MEM_50S

Broadwell ULT Memory Down LPDDR3 1x4 Length Matching

LPDDR3 Signal Group	Unit	Min Length	Max Length
CTL/CKEmax - CTL/CKEmin	mils	0	50
CTL/CKE to CLK	mils	CLK - 100	0
(CMDmax - CMDmin)	mils	0	50
CMD to CLK	mils	CLK - 250	CLK + 250
DQmax - DQmin per byte	mils	0	125
DQmax to DQs per byte	mils	DQS - 200	DQS + 50
DQS to DQS#	mils	-2.5	2.5
DQS to CLK (Rule 1)	mils	CLK - 750	CLK + 1250
CLK to CLK#	mils	-2.5	2.5

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK N<1>	7 21 24
MEM_A_CTL	MEM_40S	MEM_CTL	MEM A CS L<1..0>	7 20 21 24
MEM_A_CTL	MEM_40S	MEM_CTL	MEM A ODT<0>	20 21 24 70
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM A CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM A CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM A CAA<9..0>	20 24 70
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM A CAB<9..0>	21 24 70
MEM_A_DQBYTE0	MEM_40S	MEM_A_DQBYTE_0	MEM A DQ<7..0>	7 70 71
MEM_A_DQBYTE1	MEM_40S	MEM_A_DQBYTE_1	MEM A DQ<15..8>	7 70 71
MEM_A_DQBYTE2	MEM_40S	MEM_A_DQBYTE_2	MEM A DQ<23..16>	7 70 71
MEM_A_DQBYTE3	MEM_40S	MEM_A_DQBYTE_3	MEM A DQ<31..24>	7 70 71
MEM_A_DQBYTE4	MEM_40S	MEM_A_DQBYTE_4	MEM A DQ<39..32>	7 70 71
MEM_A_DQBYTE5	MEM_40S	MEM_A_DQBYTE_5	MEM A DQ<47..40>	7 70 71
MEM_A_DQBYTE6	MEM_40S	MEM_A_DQBYTE_6	MEM A DQ<55..48>	7 70 71
MEM_A_DQBYTE7	MEM_40S	MEM_A_DQBYTE_7	MEM A DQ<63..56>	7 70 71
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS P<0>	7 70
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS N<0>	7 70
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS P<1>	7 70
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS N<1>	7 70
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS P<2>	7 70
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS N<2>	7 70
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS P<3>	7 70
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS N<3>	7 70
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS P<4>	7 70
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS N<4>	7 70
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS P<5>	7 70
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS N<5>	7 70
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS P<6>	7 70
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS N<6>	7 70
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS P<7>	7 70
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS N<7>	7 70
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK N<1>	7 23 24
MEM_B_CTL	MEM_40S	MEM_CTL	MEM B CS L<1..0>	7 22 23 24
MEM_B_CTL	MEM_40S	MEM_CTL	MEM B ODT<0>	22 23 24 70
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM B CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM B CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM B CAA<9..0>	22 24 70
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM B CAB<9..0>	23 24 70
MEM_B_DQBYTE0	MEM_40S	MEM_B_DQBYTE_0	MEM B DQ<7..0>	7 70 71
MEM_B_DQBYTE1	MEM_40S	MEM_B_DQBYTE_1	MEM B DQ<15..8>	7 70 71
MEM_B_DQBYTE2	MEM_40S	MEM_B_DQBYTE_2	MEM B DQ<23..16>	7 70 71
MEM_B_DQBYTE3	MEM_40S	MEM_B_DQBYTE_3	MEM B DQ<31..24>	7 70 71
MEM_B_DQBYTE4	MEM_40S	MEM_B_DQBYTE_4	MEM B DQ<39..32>	7 70 71
MEM_B_DQBYTE5	MEM_40S	MEM_B_DQBYTE_5	MEM B DQ<47..40>	7 70 71
MEM_B_DQBYTE6	MEM_40S	MEM_B_DQBYTE_6	MEM B DQ<55..48>	7 70 71
MEM_B_DQBYTE7	MEM_40S	MEM_B_DQBYTE_7	MEM B DQ<63..56>	7 70 71
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS P<0>	7 70
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS N<0>	7 70
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS P<1>	7 70
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS N<1>	7 70
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS P<2>	7 70
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS N<2>	7 70
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS P<3>	7 70
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS N<3>	7 70
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS P<4>	7 70
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS N<4>	7 70
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS P<5>	7 70
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS N<5>	7 70
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS P<6>	7 70
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS N<6>	7 70
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS P<7>	7 70
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS N<7>	7 70
		MEM_PWR	PP1V2 S3	68
		MEM_PWR	PP1V2 S3 CPUDDR	68
		MEM_PWR	PP0V6 S0 DDRVTT	68 71
		MEM_PWR	PPVTTDDR S3	68 71
		MEM_12MIL	CPU DIMMA VREFDO	7 19
		MEM_12MIL	CPU DIMMB VREFDO	7 19
		MEM_12MIL	CPU DIMM VREFCA	7 19
		MEM_12MIL	PP0V6 S3 MEM VREFDO A	20 21 68
		MEM_12MIL	PP0V6 S3 MEM VREFDO B	22 23 68
		MEM_12MIL	PP0V6 S3 MEM VREFCA A	20 21 68
		MEM_12MIL	PP0V6 S3 MEM VREFCA B	22 23 68

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Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3x_DIELECTRIC	?
TBTDP_TXRX	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DPHDMI	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMIDATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMIDATA_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_2OTHER
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	HDMI_DATA	*	DP_2SAME
DISPLAYPORT	TBTDP_TX	*	DP_2SAME
DISPLAYPORT	TBTDP_RX	*	TBTDP_TXRX

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
 DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
 SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
 MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

ELECTRICAL CONST SET	PHYSICAL	NET TYPE	SPACING
	DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N
	TBT_SPI_45S	TBT_SPI	TBT SPI CLK
	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI
	TBT_SPI_45S	TBT_SPI	TBT SPI MISO
	TBT_SPI_45S	TBT_SPI	TBT SPI CS L
	DP_85D	DISPLAYPORT	DP HDMI TBT ML P<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT ML N<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX P
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX N
	HDMI_85D	HDMI_CLK	HDMI IG CLK C P
	HDMI_85D	HDMI_CLK	HDMI IG CLK C N
	HDMI_85D	HDMI_DATA	HDMI IG DATA C P<2..0>
	HDMI_85D	HDMI_DATA	HDMI IG DATA C N<2..0>

Only used on hosts supporting Thunderbolt video-in

Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	PHYSICAL	NET TYPE	SPACING
	TBTDP_85D	TBTDP_TX	TBT A R2D C P<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D C N<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D P<1..0>
	TBTDP_85D	TBTDP_TX	TBT A R2D N<1..0>
	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>
	DP_85D	DISPLAYPORT	DP A LSX ML P<1>
	DP_85D	DISPLAYPORT	DP A LSX ML N<1>
	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>
	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>
	TBTDP_85D	TBTDP_RX	TBT A D2R C P<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R C N<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R P<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R N<0>
	TBTDP_85D	TBTDP_RX	TBT A D2R C P<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R C N<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R P<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R N<1>
	TBTDP_85D	TBTDP_RX	TBT A D2R1 AUXDDC P
	TBTDP_85D	TBTDP_RX	TBT A D2R1 AUXDDC N
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH P
	DP_85D	DISPLAYPORT	DP TBTPA AUXCH N
	TBTDP_85D	TBTDP_TX	TBT B R2D C P<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D C N<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D P<1..0>
	TBTDP_85D	TBTDP_TX	TBT B R2D N<1..0>
	DP_85D	DISPLAYPORT	DP TBTPB ML C P<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML C N<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML P<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML N<1>
	DP_85D	DISPLAYPORT	DP B LSX ML P<1>
	DP_85D	DISPLAYPORT	DP B LSX ML N<1>
	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML P<3>
	DP_85D	DISPLAYPORT	DP TBTPB ML N<3>
	TBTDP_85D	TBTDP_RX	TBT B D2R C P<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R C N<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R P<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R N<0>
	TBTDP_85D	TBTDP_RX	TBT B D2R C P<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R C N<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R P<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R N<1>
	TBTDP_85D	TBTDP_RX	TBT B D2R1 AUXDDC P
	TBTDP_85D	TBTDP_RX	TBT B D2R1 AUXDDC N
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH P
	DP_85D	DISPLAYPORT	DP TBTPB AUXCH N
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH P
	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH N
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C N
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH P
	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH N
	DP_85D	DISPLAYPORT	DP INT ML F P<3..0>
	DP_85D	DISPLAYPORT	DP INT ML F N<3..0>
	DP_85D	DISPLAYPORT	DP INT ML C P<3..0>
	DP_85D	DISPLAYPORT	DP INT ML C N<3..0>
	DP_85D	DISPLAYPORT	DP INT ML P<3..0>
	DP_85D	DISPLAYPORT	DP INT ML N<3..0>
	DP_85D	DISPLAYPORT	DP INT AUXCH C P
	DP_85D	DISPLAYPORT	DP INT AUXCH C N
	DP_85D	DISPLAYPORT	DP INT AUXCH P
	DP_85D	DISPLAYPORT	DP INT AUXCH N

Notes:
 AUX and DDC was removed from DISPLAYPORT or TBTDP_RX/TX because it's not high speed, and to save routing space.

Only used on dual-port hosts.

SYNC MASTER=GR00 J52 SYNC DATE=12/06/2011
 DRAWING NUMBER 051-1573 SIZE D
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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?	MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?	MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?	MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?	S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?	S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?	S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?	S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?	S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?	S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?	S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?	S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?	S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK P
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK N
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CKE
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CS L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM ODT
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CAS L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM RAS L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM WE L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<0>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<1>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<2>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS P<0>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS N<0>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS P<1>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS N<1>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DM<0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DM<1>
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM CAM A<14..0>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DO<7..0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DO<15..8>
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA N
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN N
		S2_MEM_PWR	PP1V35 CAM
		S2_MEM_PWR	PP0V675 CAM VREF
		S2_MEM_PWR	PP0V675 MEM CAM VREFCA
		S2_MEM_PWR	PP0V675 MEM CAM VREFDO

SYNC MASTER=YHARTANTO J44 SYNC DATE=01/09/2013

Camera Constraints

Apple Inc.

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SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE		SMBUS_SMC_2_S3_SCL	38 41 71
	PHYSICAL	SPACING		
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	38 41 71
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	38 41 71
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	38 41 71
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	38 41
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	38 41
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	38 41 71
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	38 41 71
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	38 41
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	38 41

D

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C

C

B

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SYNC MASTER=YHARTANTO_J44		SYNC DATE=01/02/2013	
SMC Constraints			
	DRAWING NUMBER		051-1573
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.070 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
MEM_40S	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
MEM_72D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
MEM_85D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
PCIE_85D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	10 MM	OVERVERRIDE	OVERVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS
Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO

X304 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE		NET NAME
	PHYSICAL	SPACING	
	THERM	THERM	TBTTHMSNS D1 P
	THERM	THERM	TBTTHMSNS D1 N
	THERM	THERM	CPUTHMSNS D1 P
	THERM	THERM	CPUTHMSNS D1 N
	THERM	THERM	CPUTHMSNS D2 P
	THERM	THERM	CPUTHMSNS D2 N
	SENSE	SENSE	ISNS CPUDDR P
	SENSE	SENSE	ISNS CPUDDR N
	SENSE	SENSE	ISNS LCDBKLT P
	SENSE	SENSE	ISNS LCDBKLT N
	SENSE	SENSE	ISNS TBT P
	SENSE	SENSE	ISNS TBT N
	SENSE	SENSE	ISNS LCDPANEL P
	SENSE	SENSE	ISNS LCDPANEL N
	SENSE	SENSE	ISNS HS COMPUTING P
	SENSE	SENSE	ISNS HS COMPUTING N
	SENSE	SENSE	ISNS HS OTHER5V P
	SENSE	SENSE	ISNS HS OTHER5V N
	SENSE	SENSE	ISNS HS_OTHER3V3 P
	SENSE	SENSE	ISNS HS_OTHER3V3 N
	SENSE	SENSE	CPUVR ISNS P
	SENSE	SENSE	CPUVR ISNS N
	SENSE	SENSE	CPUVR ISNS R P
	SENSE	SENSE	CPUVR ISNS R N
	SENSE	SENSE	ISNS 1V05_S0 P
	SENSE	SENSE	ISNS 1V05_S0 N
	SENSE	SENSE	ISNS SSD P
	SENSE	SENSE	ISNS SSD N
	SENSE	SENSE	ISNS TPAD P
	SENSE	SENSE	ISNS TPAD N
	SENSE	SENSE	ISNS 1V8_S3 P
	SENSE	SENSE	ISNS 1V8_S3 N
	SENSE	SENSE	ISNS PP3V3S0_P
	SENSE	SENSE	ISNS PP3V3S0_N
	SENSE	SENSE	ISNS PP5V50_P
	SENSE	SENSE	ISNS PP5V50_N
	SENSE	SENSE	ISNS CPUHIGAIN P
	SENSE	SENSE	ISNS CPUHIGAIN N
	SENSE	SENSE	ISNS CPUHIGAIN R P
	SENSE	SENSE	ISNS CPUHIGAIN R N
	SENSE	SENSE	CHGR CSI P
	SENSE	SENSE	CHGR CSI N
	SENSE	SENSE	CHGR CSI R P
	SENSE	SENSE	CHGR CSI R N
	SENSE	SENSE	CHGR CSO P
	SENSE	SENSE	CHGR CSO N
	SENSE	SENSE	CHGR CSO R P
	SENSE	SENSE	CHGR CSO R N
	DP_NO_TOPOLOGY	SENSE	CPUVR ISNS1 P
	DP_NO_TOPOLOGY	SENSE	CPUVR ISNS1 N
	DP_NO_TOPOLOGY	SENSE	CPUVR ISNS2 P
	DP_NO_TOPOLOGY	SENSE	CPUVR ISNS2 N

The signals below have no topologies assigned.

X304 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE		NET NAME
	PHYSICAL	SPACING	
	ANL_AUDIO	AUDIO	AUD LO2 L P
	ANL_AUDIO	AUDIO	AUD LO2 L N
	ANL_AUDIO	AUDIO	AUD SPKRAMP LIN P
	ANL_AUDIO	AUDIO	AUD SPKRAMP LIN N
	ANL_AUDIO	AUDIO	SPKRAMP LIN P
	ANL_AUDIO	AUDIO	SPKRAMP LIN N
	ANL_AUDIO	AUDIO	AUD LO2 R P
	ANL_AUDIO	AUDIO	AUD LO2 R N
	ANL_AUDIO	AUDIO	AUD SPKRAMP RIN P
	ANL_AUDIO	AUDIO	AUD SPKRAMP RIN N
	ANL_AUDIO	AUDIO	SPKRAMP RIN P
	ANL_AUDIO	AUDIO	SPKRAMP RIN N
	ANL_AUDIO	AUDIO	AUD LO3 L P
	ANL_AUDIO	AUDIO	AUD LO3 L N
	ANL_AUDIO	AUDIO	AUD SPKRAMP LSUBIN P
	ANL_AUDIO	AUDIO	AUD SPKRAMP LSUBIN N
	ANL_AUDIO	AUDIO	LSUBIN P
	ANL_AUDIO	AUDIO	LSUBIN N
	ANL_AUDIO	AUDIO	AUD LO3 R P
	ANL_AUDIO	AUDIO	AUD LO3 R N
	ANL_AUDIO	AUDIO	AUD SPKRAMP RSUBIN P
	ANL_AUDIO	AUDIO	AUD SPKRAMP RSUBIN N
	ANL_AUDIO	AUDIO	RSUBIN P
	ANL_AUDIO	AUDIO	RSUBIN N
	DIG_AUDIO	AUDIO	SPKRCONN SL OUT P
	DIG_AUDIO	AUDIO	SPKRCONN SL OUT N
	DIG_AUDIO	AUDIO	SPKRCONN SR OUT P
	DIG_AUDIO	AUDIO	SPKRCONN SR OUT N
	DIG_AUDIO	AUDIO	SPKRCONN L OUT P
	DIG_AUDIO	AUDIO	SPKRCONN L OUT N
	DIG_AUDIO	AUDIO	SPKRCONN R OUT P
	DIG_AUDIO	AUDIO	SPKRCONN R OUT N
	ANL_AUDIO_WIDE	AUDIO	AUD CH HS GND
	ANL_AUDIO_WIDE	AUDIO	AUD CONN HS MIC P
	ANL_AUDIO_WIDE	AUDIO	AUD CONN SLEEVE
	ANL_AUDIO_WIDE	AUDIO	AUD CONN SLEEVE XW
	ANL_AUDIO_WIDE	AUDIO	AUD HP PORT REFCH
	ANL_AUDIO_WIDE	AUDIO	AUD HS MIC P
	ANL_AUDIO_WIDE	AUDIO	CODEC HS MIC P
	ANL_AUDIO_WIDE	AUDIO	HS MIC P
	ANL_AUDIO_WIDE	AUDIO	AUD CONN HS MIC N
	ANL_AUDIO_WIDE	AUDIO	AUD CONN RING2
	ANL_AUDIO_WIDE	AUDIO	AUD CONN RING2 XW
	ANL_AUDIO_WIDE	AUDIO	AUD HP PORT REFUS
	ANL_AUDIO_WIDE	AUDIO	AUD HS MIC N
	ANL_AUDIO_WIDE	AUDIO	AUD US HS GND
	ANL_AUDIO_WIDE	AUDIO	HS MIC N
	ANL_AUDIO_WIDE	AUDIO	CODEC HS MIC N
	SB_POWER		PP3V3_S5
	SB_POWER		PP3V3_S0
	GND		GND

Project Specific Constraints

Apple Inc.

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PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYERS?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?	PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?	PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?	PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?	PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?	PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
PCIE_SSD_D2R	PCIE_85D	PCIE_BX	PCIE SSD D2R P<3..1>	12 32 71
PCIE_SSD_D2R	PCIE_85D	PCIE_BX	PCIE SSD D2R N<3..1>	12 32 71
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_BX	PCIE SSD D2R P<0>	12 32 71
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_BX	PCIE SSD D2R N<0>	12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D C P<3..0>	12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D C N<3..0>	12 32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D P<3..0>	32 71
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D N<3..0>	32 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_BX	PCIE TBT D2R P<0>	14 25 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_BX	PCIE TBT D2R N<0>	14 25 71
PCIE_TBT_D2R_0	PCIE_85D	PCIE_BX	PCIE TBT D2R C P<0>	25
PCIE_TBT_D2R_0	PCIE_85D	PCIE_BX	PCIE TBT D2R C N<0>	25
PCIE_TBT_D2R	PCIE_85D	PCIE_BX	PCIE TBT D2R P<3..1>	14 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_BX	PCIE TBT D2R N<3..1>	14 25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_BX	PCIE TBT D2R C P<3..1>	25 71
PCIE_TBT_D2R	PCIE_85D	PCIE_BX	PCIE TBT D2R C N<3..1>	25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D P<3..0>	25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D N<3..0>	25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D C P<3..0>	14 25 71
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D C N<3..0>	14 25 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D P	66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D N	66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D C P	14 66 71
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE AP R2D C N	14 66 71
PCIE_AP_D2R	PCIE_85D	PCIE_BX	PCIE AP D2R P	14 66 71
PCIE_AP_D2R	PCIE_85D	PCIE_BX	PCIE AP D2R N	14 66 71
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN P	66
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN N	66
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP P	12 66 71
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP N	12 66 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA P	12 34 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA N	12 34 71
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C P	33 34
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C N	33 34
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD P	12 32 71
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD N	12 32 71
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC1 P	32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC1 N	32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC2 P	32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC2 N	32
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT P	12 25 71
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT N	12 25 71
PCIE_CAMERA_D2R	PCIE_85D	PCIE_BX	PCIE CAMERA D2R P	14 34 71
PCIE_CAMERA_D2R	PCIE_85D	PCIE_BX	PCIE CAMERA D2R N	14 34 71
PCIE_CAMERA_D2R	PCIE_85D	PCIE_BX	PCIE CAMERA D2R C P	33 34
PCIE_CAMERA_D2R	PCIE_85D	PCIE_BX	PCIE CAMERA D2R C N	33 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D P	33 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D N	33 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D C P	14 34
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D C N	14 34

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