1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0002265654	ENGINEERING RELEASED	2013-08-22

SCHEM,MLB_KEPLER,J45G

8/22/2013 DVT

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0675	1	SCHEM,MLB_KEPLER,J45G	SCH	CRITICAL	
820-3787	1	PCBF,MLB_KEPLER,J45G	PCB	CRITICAL	

_DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Thu Aug 22 12:19:14 2013

DRAWING TITLE: SCHEM,MLB,KEPLER,J45G

Apple Inc.

DRAWING NUMBER: 051-0675 | SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0177	COMMON PARTS,MLB,KEPLER,J45	J45G_COMMON
985-0181	DEV,MLB,KEPLER,J45	J45G_DEVEL:DVT
639-5245	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5246	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5247	PCBA,MLB,KEPLER,CRW_BSET,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5248	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5249	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5250	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5251	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5252	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5253	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5254	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5255	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5256	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
-> 639-5257	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5258	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5259	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5260	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5261	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5262	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5263	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5264	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5265	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5266	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5267	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5268	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
-> 639-5478	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5479	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5480	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5481	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5482	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5483	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX
639-5484	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5485	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5486	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5487	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5488	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5489	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX

J45G BOM Groups

BOM GROUP	BOM OPTIONS
J45G_COMMON	ALTERNATE,COMMON,J45G_COMMON1,J45G_COMMON2,J45G_PROGPARTS,GFX_BM,ACAPS:A2
J45G_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X8X8,S2_PWR:S0
J45G_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45G_PVT	BKLT:PROD,SENSOR_NONPROD:N
J45G_PROGPARTS	SMC_PROG:PROTO4,BOOTROM_PROG:PROTO4,TBTROM:PROG,TPAD_PSOC:PROG,GFX_PROGPARTS
GFX_PROGPARTS	DPMUXMCU:PROG
J45G_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,BKLT:ENG,DBGLED,CAM_XTAL:YES,DPMUX_DEBUG
J45G_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
GFX_BM	GK107:GX,DPMUX:HOCO
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	IC,CPU,CRW,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	IC,CPU,CRW,PRQ,C0,2.3,47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	IC,CPU,CRW,PRQ,C0,2.6,47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,PCH,LPT-M, HM87,C2,SR199,PRQ,20x20mm,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC, FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA	.....	CRITICAL	4Gb_HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	.....	CRITICAL	4Gb_SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P	.....	CRITICAL	4Gb_ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA	.....	CRITICAL	4Gb_MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA	.....	CRITICAL	4Gb_HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	.....	CRITICAL	4Gb_SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P	.....	CRITICAL	4Gb_ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA	.....	CRITICAL	4Gb_MICRON_1600
337S4256	1	IC,GPU,GK107-GT A2,BGA908	U8400	CRITICAL	GK107:GT
337S4427	1	IC,GPU,107GX,926MHZ,1.0375V,1.5V,FBGA908	U8400	CRITICAL	GK107:GX
337S4616	1	IC,GPU,CK107-762,A2,940MHz,5GBPS,1.2V,1.5V908BG	U8400	CRITICAL	GK107:GX2
333S0630	4	IC,SDRAM,GDDR5,64MX32,A-DIE,HYNIX	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_A_DIE
333S0631	4	IC,SDRAM,GDDR5,64MX32,D-DIE,SAMSUNG	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_SAMSUNG
333S0695	4	IC,SDRAM,GDDR5,2GBIT,5GBPS,170FBGA	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA
333S0701	4	IC,SDRAM,GDDR5,2GBIT,5GBPS,170FBGA,EDW2032BBBG-6A-F	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA_29nm
333S0734	4	IC,SDRAM,GDDR5,64MX3,HYNIX,H5GC2H24BFR-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_29nm
333S0685	4	IC,SDRAM,GDDR5,64MX3,HYNIX,H5GC4H24MFP-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_HYNIX

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:2Gb_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:2Gb_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:2Gb_ELPIDA_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:2Gb_MICRON_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM:4Gb_HYNIX_1600_S	4Gb_HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:4Gb_SAMSUNG_1600_S	4Gb_SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:4Gb_ELPIDA_1600_S	4Gb_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:4Gb_MICRON_1600_S	4Gb_MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:4Gb_HYNIX_1600	4Gb_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:4Gb_SAMSUNG_1600	4Gb_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:4Gb_ELPIDA_1600	4Gb_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:4Gb_MICRON_1600	4Gb_MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

Development/Base BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0177	1	J45G MLB,KEPLER BASE BOM	BASE	CRITICAL	BASE_BOM
985-0181	1	J45G MLB,KEPLER, DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

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Programmables - All builds

341S3920	1	IC,EEPROM,FALCON RIDGE (V13.1),J44/J45	U2890	CRITICAL	TBTROM:PROG
335S0915	1	EEPROM,SPI FLASH ROM,4MBit,50MHZ,USON8	U2890	CRITICAL	TBTROM:BLANK
335S0852	1	IC,GPUROM,D2,BLANK	U9101	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C,(RENESAS) V3.2.8,DVB,D2	U9600	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9600	CRITICAL	DPMUXMCU:BLANK
341S3856	1	IC,TRKPD/KYBD CNTRLR,CU only,V225,J45	U4801	CRITICAL	TPAD_PSOC:PROG
337S4587	1	IC,TP PSOC,QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK

SMC

338S1214	1	IC,SMC-A3,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3901	1	IC,SMC-B1,SCPL,EXT,V2.16Q13,PROTO4,J45G	U5000	CRITICAL	SMC_PROG:PROTO4
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE,L	U6100	CRITICAL	BOOTROM_PROG:BLANK
335S0812	1	64MBIT SPI SRL DUAL I/O FLSH,SOIC8,Z	U6100	CRITICAL	BOOTROM_PROG:BLANK2
341S3712	1	IC,EFI ROM(V0008)PROTO 0,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO
341S3742	1	IC,EFI ROM(V0013) PROTO 1,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3890	1	IC,EFI ROM(V0100) PROTO 3-J45 & EVT-J45	U6100	CRITICAL	BOOTROM_PROG:PROTO3
341S3904	1	IC,EFI ROM(V0106) PROTO 4,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO4

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
376S1053	376S0604		ALL	Diodes alt to Fairchild	
128S0311	128S0329		ALL	NEC alt to Sanyo	
138S0739	138S0706		ALL	Samsung alt to Murata	
197S0481	197S0480		ALL	EPSON Alt to NDK	
371S0713	371S0558		ALL	DDS alt to ST	
152S0461	152S1645		ALL	Cyntec alt to Vishay	
376S1080	376S0820		ALL	Diodes alt to On Semi	
155S0667	155S0583		ALL	Panasonic alt to TDK	
376S1032	376S0855		ALL	Toshiba alt to Diodes	
376S1129	376S0855		ALL	NXP alt to Diodes	
376S1089	376S1128		ALL	NXP alt to Diodes	
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung	
128S0371	128S0376		ALL	Kemet alt to Sanyo	
333S0629	333S0703		ALL	Epida Alt die	
138S0803	138S0639		ALL	Samsung Alt to Murata	
138S0843	138S0674		ALL	Samsung Alt to Murata	
138S0846	138S0811		ALL	Samsung Alt to Murata	
127S0164	127S0162		ALL	Rohm Alt to Vishay	
138S0732	138S0715		ALL	Rohm Alt to Vishay	
128S0364	128S0264		ALL	Kemet alt to Sanyo	
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000	
353S3527	353S3528		ALL	Pericom eDP MUX	FROM J15
353S3526	353S3528		ALL	TI eDP MUX	
197S0466	197S0464		ALL	Epson alt to NDK	
311S0649	311S0541		ALL	ON alt to Toshiba (U2030,U7001)	
197S0479	197S0478		ALL	Epson alt to NDK	

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Frame Holes

ZT0415 2.8R2.3 — GND_BATT_CHGND

ZT0450 TH-NSP — GND_CHASSIS_FAN — SL-2.3X3.9-2.9X4.5

ZT0474 TH-NSP — GND_CHASSIS_MLBCAN5 — SL-1.1X0.45-1.4X0.75

ZT0475 TH-NSP — GND_CHASSIS_MLBCAN6 — SL-1.1X0.45-1.4X0.75

ZT0470 TH-NSP — GND_CHASSIS_MLBCAN1 — SL-1.1X0.45-1.4X0.75

ZT0471 TH-NSP — GND_CHASSIS_MLBCAN2 — SL-1.1X0.45-1.4X0.75

ZT0472 TH-NSP — GND_CHASSIS_MLBCAN3 — SL-1.1X0.45-1.4X0.75

ZT0473 TH-NSP — GND_CHASSIS_MLBCAN4 — SL-1.1X0.45-1.4X0.75

SMT GND TEST PONTS

ZT0490 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0491 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0492 2.1SM2.0MM-CIR SMT-PAD-NSP

APN 806-2247
BR0401 MLB-MTG_BRKT-J5 TH

J45 THERMAL MODULE STANDOFF

GPU BOSS APN 860-4772

SH0427 4.5OD1.85ID-1.95H

SH0428 4.5OD1.85ID-1.95H

SH0430 4.5OD1.85ID-1.95H

APN 860-1327
SH0425 STDOFF-4.5OD1.8H-SM

SH0423 STDOFF-4.5OD1.8H-SM

APN 817-0688
SH0446 STDOFF-4.9OD2.38H-SM-2

APN 817-0741
SH0445 STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

APN 860-1328
SH0424 STDOFF-4.5OD1.9H-SM

APN 817-4517
SH0421 4.5OD1.85ID-1.95H-1

CPU BOSS APN 860-2931

SH0420 5.0OD1.85ID-2.35H

SH0426 5.0OD1.85ID-2.35H

SH0422 5.0OD1.85ID-2.35H

SH0429 5.0OD1.85ID-2.35H

Thermal Module gaskets APN 875-9290

OMIT CG0400 6.0OD3.9H-SM

OMIT CG0402 6.0OD3.9H-SM

OMIT CG0401 6.0OD3.9H-SM

OMIT CG0403 6.0OD3.9H-SM

APN 806-9391
SH0450 SM — SHLD-MLB-USB-J45

APN 806-6192
SH0452 SM — SHLD-J45-CAN-FENCE1-MDP

APN 806-6194
SH0451 SM — SHLD-J45-CAN-FENCE2-MDP

PD parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	

J45 POGO PINS

APN 870-2451

SH0431 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0432 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0433 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0434 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0435 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0436 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0437 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

J45 STANDOFF

APN 860-1448

SH0440 2.9OD1.2ID-1.35H-SM

SH0441 2.9OD1.2ID-1.35H-SM

SH0444 2.9OD1.2ID-1.35H-SM

SH0460 2.9OD1.2ID-1.35H-SM

SH0461 2.9OD1.2ID-1.35H-SM

SH0442 2.9OD1.2ID-1.35H-SM

SH0443 2.9OD1.2ID-1.35H-SM

SH0462 2.9OD1.2ID-1.35H-SM

SH0465 2.9OD1.2ID-1.35H-SM

SH0466 2.9OD1.2ID-1.35H-SM

SH0467 2.9OD1.2ID-1.35H-SM

SYNC_MASTER=CLEAN_J45 SYNC_DATE=05/03/2013

PAGE TITLE: PD Parts

Apple Inc.

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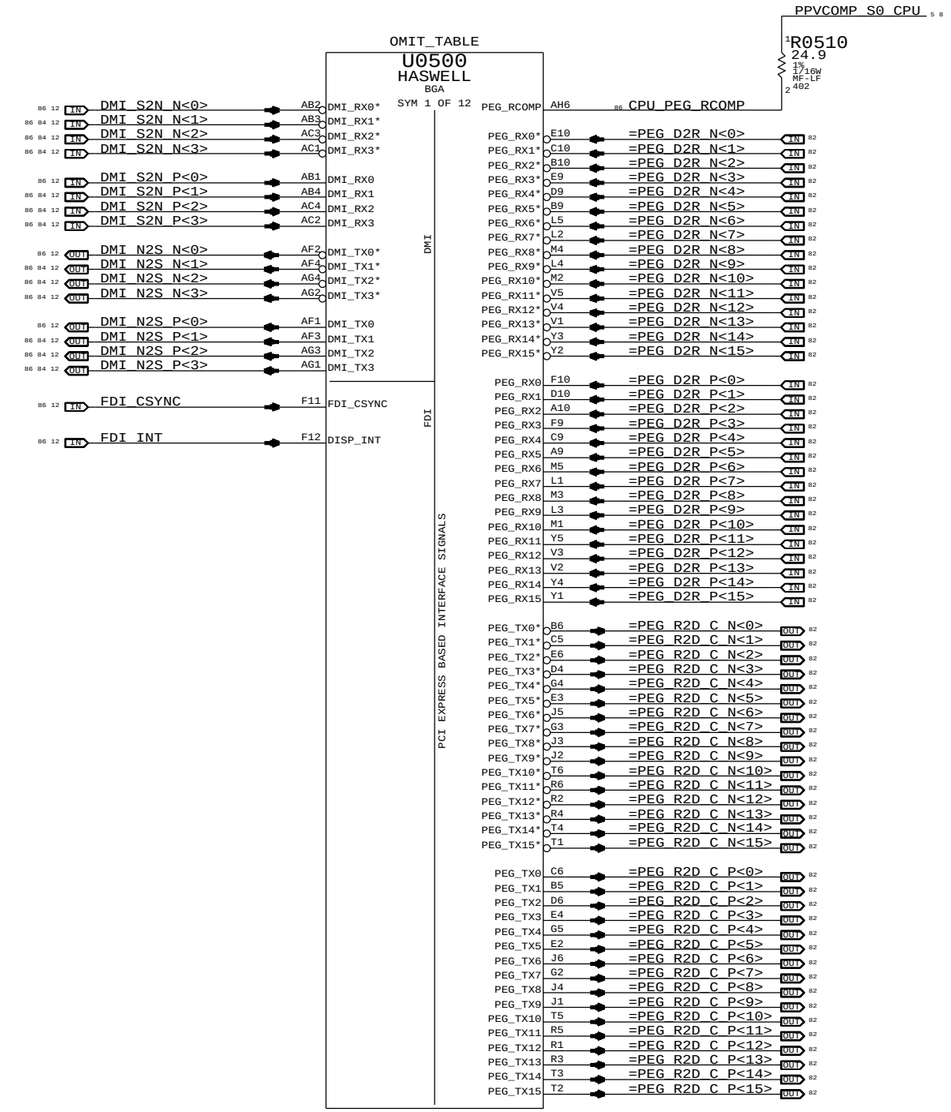

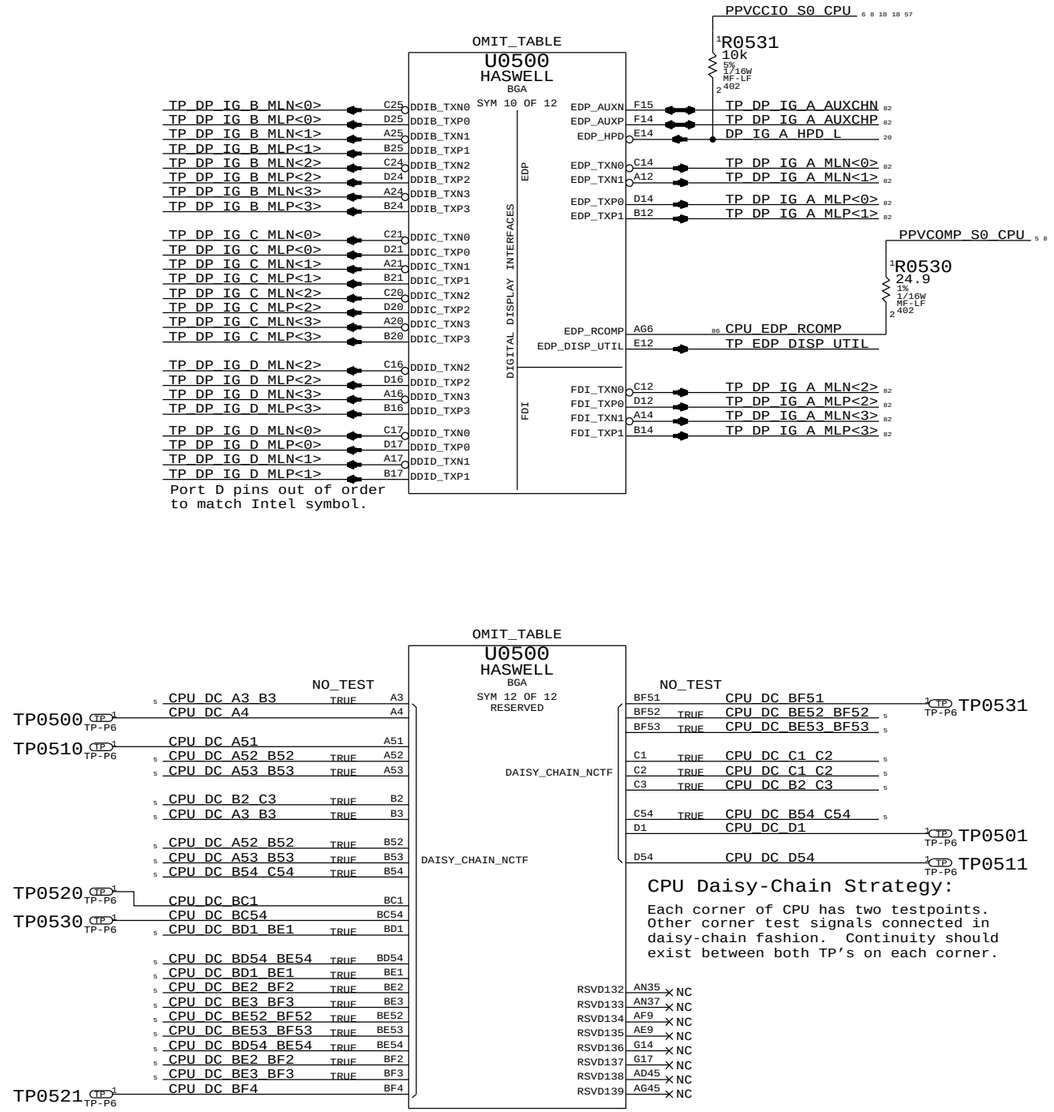

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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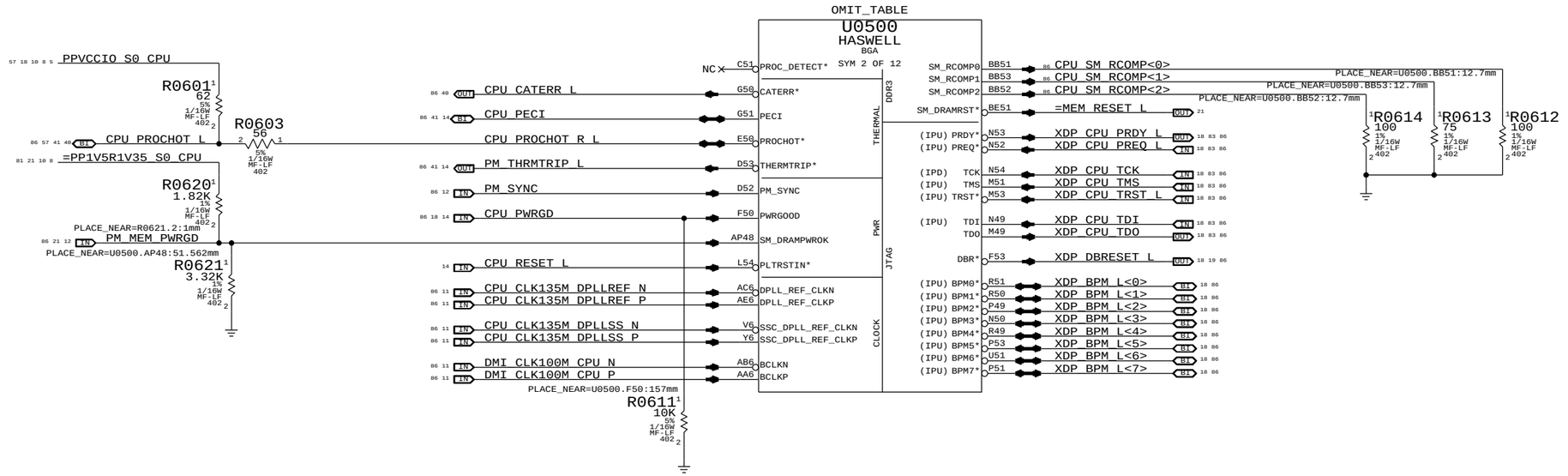
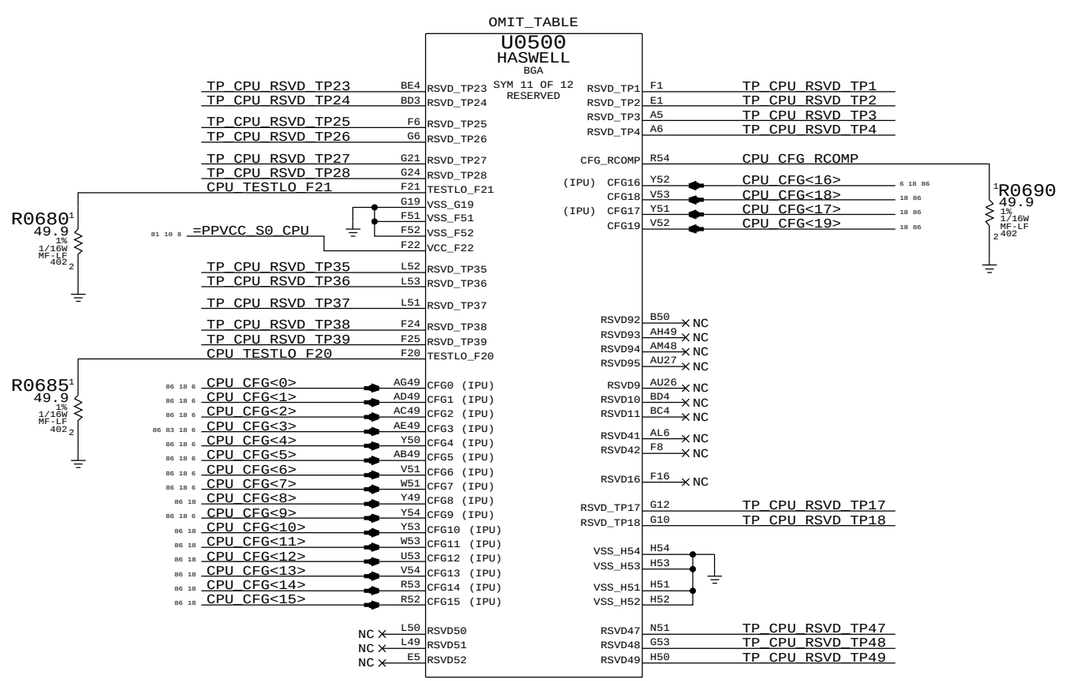
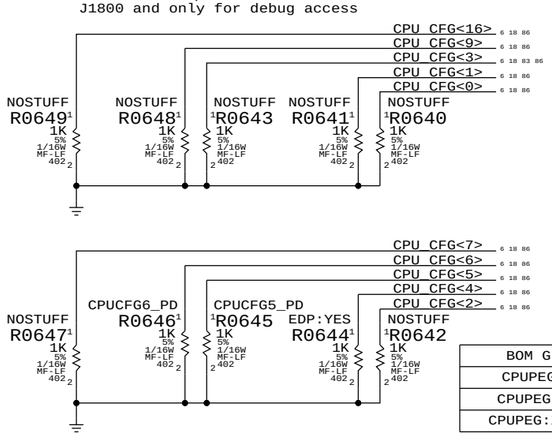




CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU Clock/Misc/JTAG/CFG

Apple Inc.

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MEMORY CHANNEL A

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MEM_A_DQ<10>	AR51	SA_DQ10	
MEM_A_DQ<11>	AR53	SA_DQ11	
MEM_A_DQ<12>	AN53	SA_DQ12	
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MEM_A_DQ<14>	AR52	SA_DQ14	
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MEM_A_DQ<29>	AY43	SA_DQ29	
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MEM_A_DQ<32>	BF14	SA_DQ32	
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MEM_A_DQ<51>	AW2	SA_DQ51	
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MEM_A_DQ<59>	AR4	SA_DQ59	
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MEM_A_DQ<63>	AR3	SA_DQ63	

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CPU_DIMMB_VREFDQ	AN6	SB_DIMM_VREFDQ	
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RSVD160	BD31	NC	
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SA_CKP2	BF23	NC	
SA_CKE2	BC34	NC	
SA_CKN3	BD23	NC	
SA_CKP3	BC23	NC	
SA_CKE3	BD34	NC	
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SA_CS3*	BD16	NC	
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SA_WE*	BF21	MEM_A_WE_L	
SA_CAS*	BE21	MEM_A_CAS_L	
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RSVD163	BA40	NC	
RSVD164	AY40	NC	
RSVD165	BA39	NC	
RSVD166	AY39	NC	
RSVD167	AV40	NC	
RSVD168	AU40	NC	
RSVD169	AV39	NC	
RSVD170	AU39	NC	

OMIT_TABLE

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MEMORY CHANNEL B

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SB_CKP2	AY26	NC	
SB_CKE2	AV35	NC	
SB_CKN3	BA27	NC	
SB_CKP3	AY27	NC	
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SB_WE*	AW23	MEM_B_WE_L	
SB_CAS*	AV20	MEM_B_CAS_L	
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RSVD179	BC39	NC	
RSVD180	BC37	NC	
RSVD181	BD37	NC	

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PAGE TITLE
CPU DDR3 Interfaces

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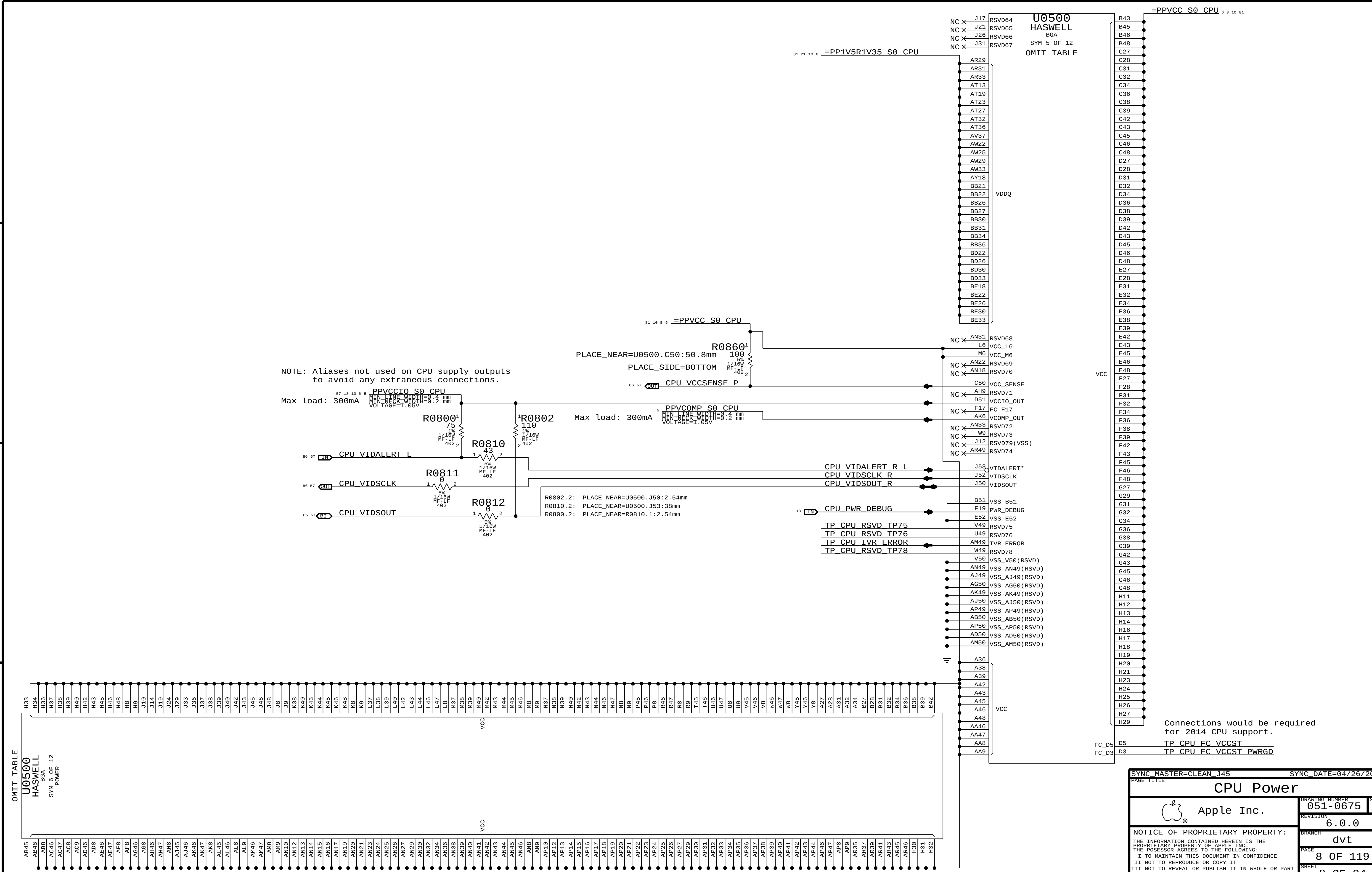

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CPU Power

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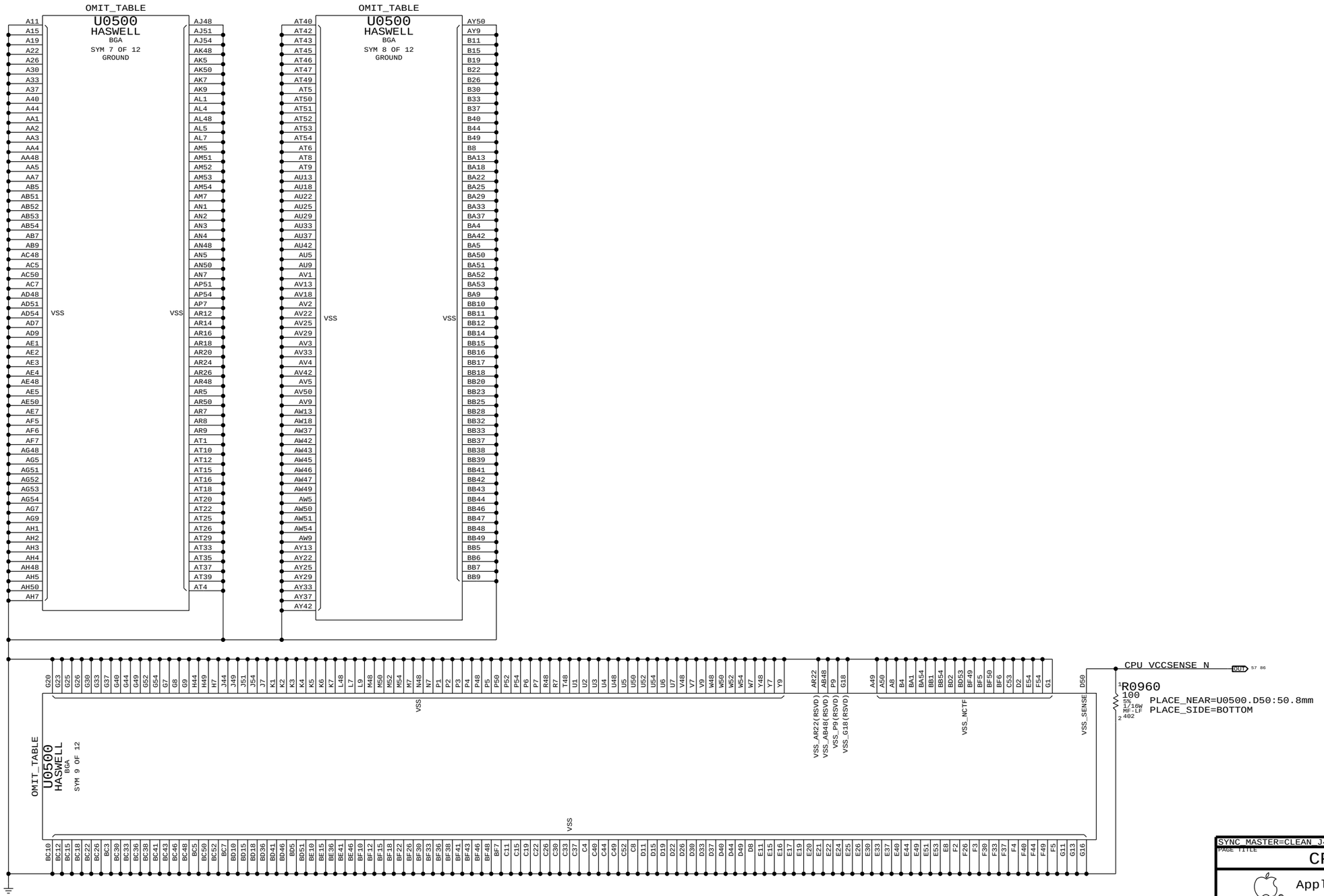

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

81 8 6 =PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 | C1001 1UF 10% 10V X6S-CERM 0402 | C1002 1UF 10% 10V X6S-CERM 0402 | C1003 1UF 10% 10V X6S-CERM 0402 | C1004 1UF 10% 10V X6S-CERM 0402 | C1005 1UF 10% 10V X6S-CERM 0402 | C1006 1UF 10% 10V X6S-CERM 0402 | C1007 1UF 10% 10V X6S-CERM 0402 | C1008 1UF 10% 10V X6S-CERM 0402 | C1009 1UF 10% 10V X6S-CERM 0402 | C1010 1UF 10% 10V X6S-CERM 0402 | C1011 1UF 10% 10V X6S-CERM 0402 | C1012 1UF 10% 10V X6S-CERM 0402 | C1013 1UF 10% 10V X6S-CERM 0402 | C1014 1UF 10% 10V X6S-CERM 0402 | C1015 1UF 10% 10V X6S-CERM 0402 | C1016 1UF 10% 10V X6S-CERM 0402 | C1017 1UF 10% 10V X6S-CERM 0402 | C1018 1UF 10% 10V X6S-CERM 0402 | C1019 1UF 10% 10V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

NO STUFF

C1020 20UF 20% 4V X5R-CERM 0402-2 | C1021 20UF 20% 4V X5R-CERM 0402-2 | C1022 20UF 20% 4V X5R-CERM 0402-2 | C1023 20UF 20% 4V X5R-CERM 0402-2

NO STUFF NO STUFF NO STUFF

ACAPS:A2
CAPS for Acoustic Control (C109A to C102D)
ACAPS:A2

NO STUFF | CRITICAL C109A 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C109B 20UF 20% 4V X5R-CERM 0402-2 | NO STUFF | CRITICAL C109C 20UF 20% 4V X5R-CERM 0402-2 | NO STUFF | CRITICAL C109D 20UF 20% 4V X5R-CERM 0402-2 | ACAPS:A1 | CRITICAL C109E 20UF 20% 4V X5R-CERM 0402-2 | ACAPS:A1 | CRITICAL C109F 20UF 20% 4V X5R-CERM 0402-2 | ACAPS:A1 | CRITICAL C101A 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C101B 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C101C 20UF 20% 4V X5R-CERM 0402-2 | NO STUFF | CRITICAL C101D 20UF 20% 4V X5R-CERM 0402-2 | ACAPS:A1 | CRITICAL C101E 20UF 20% 4V X5R-CERM 0402-2 | NO STUFF | CRITICAL C101F 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C102A 20UF 20% 4V X5R-CERM 0402-2 | NO STUFF | CRITICAL C102B 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C102C 20UF 20% 4V X5R-CERM 0402-2 | ACAPS:A2 | CRITICAL C102D 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

NO STUFF ACAPS:A2

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1025 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1026 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1027 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1028 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1029 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1030 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1031 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1032 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1033 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1034 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1035 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1036 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1037 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1038 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1039 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1040 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1041 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1042 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1043 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1044 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1045 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

ACAPS:A1 ACAPS:A2 ACAPS:A1 ACAPS:A1 ACAPS:A2 ACAPS:A2 ACAPS:A1 ACAPS:A2 NO STUFF ACAPS:A2 ACAPS:A2 ACAPS:A1 ACAPS:A1

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1047 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1048 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1049 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1050 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1051 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1052 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1053 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1054 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1055 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1056 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1057 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1058 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1059 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1060 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1061 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1062 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1063 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1064 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1065 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1066 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1067 20UF 20% 4V X5R-CERM 0402-2

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1068-C1076):
Place near inductors on bottom side.

NO STUFF NO STUFF

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1077 330UF-9MOHM 20% 2.5V POLY-TANT D15T-1

CAPS for Acoustic Control (C102E to C103F)
ACAPS:A2 NO STUFF NO STUFF ACAPS:A2

CRITICAL C102E 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C102F 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C103A 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C103B 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C103C 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C103D 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C103E 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C103F 20UF 20% 4V X5R-CERM 0402-2

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

81 21 8 6 =PP1V5R1V35_S0_CPU

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402 | C1081 1UF 10% 10V X6S-CERM 0402 | C1082 1UF 10% 10V X6S-CERM 0402 | C1083 1UF 10% 10V X6S-CERM 0402 | C1084 1UF 10% 10V X6S-CERM 0402 | C1085 1UF 10% 10V X6S-CERM 0402 | C1086 1UF 10% 10V X6S-CERM 0402 | C1087 1UF 10% 10V X6S-CERM 0402 | C1088 1UF 10% 10V X6S-CERM 0402 | C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603 | C1091 10UF 20% 4V X6S-CERM 0603 | C1092 10UF 20% 4V X6S-CERM 0603 | C1093 10UF 20% 4V X6S-CERM 0603 | C1094 10UF 20% 4V X6S-CERM 0603 | C1095 10UF 20% 4V X6S-CERM 0603 | C1096 10UF 20% 4V X6S-CERM 0603 | C1097 10UF 20% 4V X6S-CERM 0603

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2.5V POLY-TANT D15T-ECGLT-COMBO
CRITICAL C1099 330UF-6MOHM 20% 2.5V POLY-TANT D15T-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

57 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 10V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=CLEAN_J15 SYNC_DATE=05/02/2013
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
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OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (1 OF 11)

RTC
SYSCLK_CLK32K_RTC — B5 RTCX1; B4 RTCX2 (NC)
PCH_SRTCRST_L — B9 SRTCRST*
PCH_INTRUDER_L — A8 INTRUDER*
PCH_INTVRMEN_L — G10 INTVRMEN
RTC_RESET_L — D9 RTCRST*

AZALIA
HDA_BIT_CLK — R1110 33 1/20W MF 201 — HDA_BIT_CLK_R — B25 HDA_BCLK
HDA_SYNC — R1111 33 1/20W MF 201 — HDA_SYNC_R — A22 HDA_SYNC (IPD-boot)
PCH_SPKR — AL10 SPKR (IPD-PLTRST#)
HDA_RST_L — R1112 33 1/20W MF 201 — HDA_RST_R_L — C24 HDA_RST*
PLACE_NEAR=U1100.B25:1.27mm
PLACE_NEAR=U1100.A22:1.27mm
PLACE_NEAR=U1100.C24:1.27mm
HDA_SDIN0 — L22 HDA_SDI0 (IPD)
TP_HDA_SDIN1 — K22 HDA_SDI1 (IPD)
TP_HDA_SDIN2 — G22 HDA_SDI2 (IPD)
TP_HDA_SDIN3 — F22 HDA_SDI3 (IPD)
HDA_SDOUT — R1113 33 1/20W MF 201 — HDA_SDOUT_R — A24 HDA_SDO (IPD-boot)
PLACE_NEAR=U1100.A24:1.27mm
DP_TBT_SEL — B17 (IPD-DOCKEN#) DOCKEN*/GPIO33
ENET_MEDIA_SENSE_RDIV — C22 HDA_DOCK_RST*/GPIO13

JTAG
XDP_PCH_TCK — AB3 JTAG_TCK (IPD)
XDP_PCH_TMS — AD1 JTAG_TMS (IPU)
XDP_PCH_TDI — AE2 JTAG_TDI (IPU)
XDP_PCH_TDO — AD3 JTAG_TDO
F8 TP25; C26 TP22; AB6 TP20 (NC)

SATA
SATA_RXN0 BC8 — SATA_A_D2R_N — SATA_TXN0 AW8 — SATA_A_R2D_C_N
SATA_RXP0 BE8 — SATA_A_D2R_P — SATA_TXP0 AY8 — SATA_A_R2D_C_P
SATA_RXN1 BC10 — SATA_B_D2R_N — SATA_TXN1 AV10 — SATA_B_R2D_C_N
SATA_RXP1 BE10 — SATA_B_D2R_P — SATA_TXP1 AW10 — SATA_B_R2D_C_P
SATA_RXN2 BB9 — TP_SATA_ODD_D2RN — SATA_TXN2 AY13 — TP_SATA_ODD_R2D_CN
SATA_RXP2 BD9 — TP_SATA_ODD_D2RP — SATA_TXP2 AW13 — TP_SATA_ODD_R2D_CP
SATA_RXN3 BC12 — TP_SATA_D_D2RN — SATA_TXN3 AR13 — TP_SATA_D_R2D_CN
SATA_RXP3 BE12 — TP_SATA_D_D2RP — SATA_TXP3 AT13 — TP_SATA_D_R2D_CP
SATA_RXN4/PERN1 BD13 — TP_PCIE_ENET_D2RN — SATA_TXN4/PETN1 AV15 — TP_PCIE_ENET_R2D_CN
SATA_RXP4/PERP1 BB13 — TP_PCIE_ENET_D2RP — SATA_TXP4/PETP1 AW15 — TP_PCIE_ENET_R2D_CP
SATA_RXN5/PERN2 BC14 — TP_SATA_F_D2RN — SATA_TXN5/PETN2 AP15 — TP_SATA_F_R2D_CN
SATA_RXP5/PERP2 BE14 — TP_SATA_F_D2RP — SATA_TXP5/PETP2 AR15 — TP_SATA_F_R2D_CP
SATA_RCOMP AY5 — PCH_SATA_RCOMP
SATALED* AP3 — PCH_SATALED_L
SATA0GP/GPIO21 AT1 — XDP_DC0_DP_AUXCH_ISOL_L
SATA1GP/GPIO19 (IPU-PLTRST#) AU2 — XDP_DC1_SATARDRVR_EN
SATA_IREF BD4
TP9 BA2 (NC); TP8 BB2 (NC)

SATA Port assignments:

Primary HDD/SSD (SATA only)

Secondary HDD/SSD (SATA only)

Reserved: ODD

Unused

PCIe:
Reserved: Ethernet
(if not combo w/SD Card)

Unused

=PP1V5_S0_PCH_SATA
R1130 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.AY5:2.54mm

NOTE: ENET pair only used if SD Card Reader is USB3.

=PPVRTC_G3_PCH
R1100 330K 5% 1/20W MF 201
R1101 1M 5% 1/20W MF 201
R1102 20K 5% 1/20W MF 201
R1103 20K 5% 1/20W MF 201
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
C1102 1UF 10% 10V X5R 402
C1103 1UF 10% 10V X5R 402

OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (2 OF 11)

PCIE_CLK100M_SSD_N — Y43 CLKOUT_PCIE_N0
PCIE_CLK100M_SSD_P — Y45 CLKOUT_PCIE_P0
SSD_CLKREQ_L — AB1 PCIECLKRQ0*/GPIO73
PCIE_CLK100M_ENETSD_N — AA44 CLKOUT_PCIE_N1
PCIE_CLK100M_ENETSD_P — AA42 CLKOUT_PCIE_P1
XDP_DD2_ENETSD_CLKREQ_L — AF1 PCIECLKRQ1*/GPIO18
PCIE_CLK100M_AP_N — AB43 CLKOUT_PCIE_N2
PCIE_CLK100M_AP_P — AB45 CLKOUT_PCIE_P2
XDP_DD3_AP_CLKREQ_L — AF3 PCIECLKRQ2*/GPIO20/SMI*
PCIE_CLK100M_CAMERA_N — AD43 CLKOUT_PCIE_N3
PCIE_CLK100M_CAMERA_P — AD45 CLKOUT_PCIE_P3
CAMERA_CLKREQ_L — T3 PCIECLKRQ3*/GPIO25
TP_PCIE_CLK100M_GPUN — AF43 CLKOUT_PCIE_N4
TP_PCIE_CLK100M_GPUP — AF45 CLKOUT_PCIE_P4
TBT_CLKREQ_L — V3 PCIECLKRQ4*/GPIO26
TP_PCIE_CLK100M_PE5N — AE44 CLKOUT_PCIE_N5
TP_PCIE_CLK100M_PE5P — AE42 CLKOUT_PCIE_P5
PCH_CLKRQ5_L_GPIO44 — AA2 PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
TP_PCIE_CLK100M_SWN — AB40 CLKOUT_PCIE_N6
TP_PCIE_CLK100M_SWP — AB39 CLKOUT_PCIE_P6
PEG_CLKREQ_L — AE4 PCIECLKRQ6*/GPIO45
PCIE_CLK100M_TBT_N — AJ44 CLKOUT_PCIE_N7
PCIE_CLK100M_TBT_P — AJ42 CLKOUT_PCIE_P7
PCH_CLKRQ7_L_GPIO46 — Y3 PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
ITPXDP_CLK100M_N — AH43 CLKOUT_ITPXDP_N
ITPXDP_CLK100M_P — AH45 CLKOUT_ITPXDP_P
LPC_CLK33M_SMC_R — D44 CLKOUT_33MHZ0 (IPD-PWROK)
LPC_CLK33M_LPCPLUS_R — E44 CLKOUT_33MHZ1 (IPD-PWROK)
TP_PCI_CLK33M_OUT2 — B42 CLKOUT_33MHZ2 (IPD-PWROK)
TP_PCI_CLK33M_OUT3 — F41 CLKOUT_33MHZ3 (IPD-PWROK)
PCH_CLK33M_PCIOUT — A40 CLKOUT_33MHZ4 (IPD-PWROK)

CLOCKS

CLKOUT_PEG_A_N AB35 — TP_PCIE_CLK100M_ENETN
CLKOUT_PEG_A_P AB36 — TP_PCIE_CLK100M_ENETP
PEG_A_CLKRQ*/GPIO47 AF6 — ENET_CLKREQ_L
CLKOUT_PEG_B_N Y39 — TP_PCIE_CLK100M_PEGBN
CLKOUT_PEG_B_P Y38 — TP_PCIE_CLK100M_PEGBP
PEG_B_CLKRQ*/GPIO56 U4 — PCH_PEGCLKRQB_L_GPIO56
CLKOUT_DMI_N AF39 — DMI_CLK100M_CPU_N
CLKOUT_DMI_P AF40 — DMI_CLK100M_CPU_P
CLKOUT_DP_N AJ40 — CPU_CLK135M_DPLLSS_N
CLKOUT_DP_P AJ39 — CPU_CLK135M_DPLLSS_P
CLKOUT_DPNS_N AF35 — CPU_CLK135M_DPLLREF_N
CLKOUT_DPNS_P AF36 — CPU_CLK135M_DPLLREF_P
CLKIN_DMI_N AY24 — PCIE_CLK100M_PCH_N
CLKIN_DMI_P AW24 — PCIE_CLK100M_PCH_P
CLKIN_GND_N AR24 — PCH_CLKIN_GNDN
CLKIN_GND_P AT24 — PCH_CLKIN_GNDP
CLKIN_DOT96_N H33 — PCH_CLK96M_DOT_N
CLKIN_DOT96_P G33 — PCH_CLK96M_DOT_P
CLKIN_SATA_N BE6 — PCH_CLK100M_SATA_N
CLKIN_SATA_P BC6 — PCH_CLK100M_SATA_P
REFCLK14IN F45 — PCH_CLK14P3M_REFCLK
CLKIN_33MHZLOOPBACK D17 — PCH_CLK33M_PCIIN
XTAL25_IN AM43 — SYSCLK_CLK25M_SB_R
XTAL25_OUT AL44 (NC)
(IPD-PWROK) CLKOUTFLEX0/GPIO64 C40 — TP_PCH_GPIO64_CLKOUTFLEX0
(IPD-PWROK) CLKOUTFLEX1/GPIO65 F38 — TP_PCH_GPIO65_CLKOUTFLEX1
(IPD-PWROK) CLKOUTFLEX2/GPIO66 F36 — TP_PCH_GPIO66_CLKOUTFLEX2
(IPD-PWROK) CLKOUTFLEX3/GPIO67 F39 — TP_PCH_GPIO67_CLKOUTFLEX3
ICLK_IREF AM45 — =PP1V5_S0_PCH_CLK
TP19 AD39 (NC); TP18 AD38 (NC)
DIFFCLK_BIASREF AN44 — PCH_DIFFCLK_BIASREF
PLACE_NEAR=U1100.AN44:2.54mm
R1190 7.5K 1% 1/20W MF 201 — =PP1V5_S0_PCH_VCCVRM_BIAS

Unused clock terminations for FCIM Mode
R1196 10K 5% 1/20W MF 201 — PCIE_CLK100M_PCH_N
R1195 10K 5% 1/20W MF 201 — PCIE_CLK100M_PCH_P
R1171 10K 5% 1/20W MF 201 — PCH_CLKIN_GNDN
R1170 10K 5% 1/20W MF 201 — PCH_CLKIN_GNDP
R1192 10K 5% 1/20W MF 201 — PCH_CLK96M_DOT_N
R1191 10K 5% 1/20W MF 201 — PCH_CLK96M_DOT_P
R1194 10K 5% 1/20W MF 201 — PCH_CLK100M_SATA_N
R1193 10K 5% 1/20W MF 201 — PCH_CLK100M_SATA_P
R1197 10K 5% 1/20W MF 201 — PCH_CLK14P3M_REFCLK
R1172 340 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB
1.5V -> 1.1V
R1173 1K 1% 1/20W MF 201

NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO

R1177 4.7K 5% 1/20W MF 201 — PCH_SPKR
R1176 10K 5% 1/20W MF 201 — DP_TBT_SEL
R1178 4.7K 5% 1/20W MF 201 — PCH_SATALED_L
R1134 10K 5% 1/20W MF 201 — DP_AUXCH_ISOL_L
R1133 10K 5% 1/20W MF 201 — SATARDRVR_EN
R1143 10K 5% 1/20W MF 201 — SSD_CLKREQ_L
R1142 10K 5% 1/20W MF 201 — ENETSD_CLKREQ_L
R1169 10K 5% 1/20W MF 201 — AP_CLKREQ_L
R1144 10K 5% 1/20W MF 201 — CAMERA_CLKREQ_L
R1145 10K 5% 1/20W MF 201 — TBT_CLKREQ_L
R1147 10K 5% 1/20W MF 201 — PCH_CLKRQ5_L_GPIO44
R1114 10K 5% 1/20W MF 201 — PEG_CLKREQ_L
R1115 10K 5% 1/20W MF 201 — PCH_CLKRQ7_L_GPIO46
R1146 10K 5% 1/20W MF 201 — ENET_CLKREQ_L
R1148 10K 5% 1/20W MF 201 — PCH_PEGCLKRQB_L_GPIO56
R1179 10K 5% 1/20W MF 201 — ENET_MEDIA_SENSE_RDIV

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013
PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
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OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (4 OF 11)

DMI_RXN0 AW22 ← DMI_N2S_N<0>
DMI_RXN1 AR20 ← DMI_N2S_N<1>
DMI_RXN2 AP17 ← DMI_N2S_N<2>
DMI_RXN3 AV20 ← DMI_N2S_N<3>
DMI_RXP0 AY22 ← DMI_N2S_P<0>
DMI_RXP1 AP20 ← DMI_N2S_P<1>
DMI_RXP2 AR17 ← DMI_N2S_P<2>
DMI_RXP3 AW20 ← DMI_N2S_P<3>
DMI_TXN0 BD21 → DMI_S2N_N<0>
DMI_TXN1 BE20 → DMI_S2N_N<1>
DMI_TXN2 BD17 → DMI_S2N_N<2>
DMI_TXN3 BE18 → DMI_S2N_N<3>
DMI_TXP0 BB21 → DMI_S2N_P<0>
DMI_TXP1 BC20 → DMI_S2N_P<1>
DMI_TXP2 BB17 → DMI_S2N_P<2>
DMI_TXP3 BC18 → DMI_S2N_P<3>

DMI_IREF BE16 ← =PP1V5_S0_PCH_RCOMP
R1200 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.AY17:12.7mm
DMI_RCOMP AY17 ← PCH_DMI_RCOMP

TP12 AW17 — NC
TP7 AV17 — NC

FDI_RXN0 AJ35 — NC
FDI_RXN1 AL35 — NC
FDI_RXP0 AJ36 — NC
FDI_RXP1 AL36 — NC
TP16 AV43 — NC
TP5 AY45 — NC
TP15 AV45 — NC
TP10 AW44 — NC
FDI_CSYNC AL39 → FDI_CSYNC (OUT 5,86)
FDI_INT AL40 → FDI_INT (OUT 5,86)
FDI_IREF AT45 ← =PP1V5_S0_PCH_RCOMP
R1210 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.AR44:12.7mm
FDI_RCOMP AR44 ← PCH_FDI_RCOMP

TP17 AU42 — NC
TP13 AU44 — NC
=PPVRTC_G3_PCH
R1215 330K 5% 1/20W MF 201

SUSACK* (IPU) R6 ← PCH_SUSACK_L
SYS_RESET* AM1 ← PM_SYSRST_L
SYS_PWROK AD7 ← PM_PCH_SYS_PWROK
PWROK F10 ← PM_PCH_PWROK
APWROK AB7 ← PM_PCH_APWROK
DRAMPWROK (OD) H3 ← PM_MEM_PWRGD
RSMRST* J2 ← PM_RSMRST_L
SUSWARN*/SUSPWRNACK/GPIO30 J4 ← PCH_SUSWARN_L
PWRBTN* (IPU) K1 ← PM_PWRBTN_L
ACPRESENT/GPIO31 (IPD-DeepSx) E6 ← SMC_ADAPTER_EN
BATLOW*/GPIO72 K7 ← PM_BATLOW_L
RI* N4 ← PCH_RI_L
TP21 AB10 ← TP_PCH_SLP_S0_L
SLP_WLAN*/GPIO29 D2 ← TP_PCH_SLP_WLAN_L

R1286 0 5% 1/20W MF 0201
=PP3V3_SUS_PCH_GPIO
R1205 10K 5% 1/20W MF 201

DSWVRMEN C8 → PCH_DSWVRMEN
DPWROK L13 → PM_DSW_PWRGD
WAKE* (IPD-DeepSx) K3 → PCIE_WAKE_L (IN 12,33,35,83,88)
CLKRUN* AN7 ↔ PM_CLKRUN_L (BI 12,40,49,83)
SUS_STAT*/GPIO61 U7 → LPC_PWRDWN_L (OUT 20,40,49,83)
SUSCLK/GPIO62 (IPU-RSMRST#) Y6 → PM_CLK32K_SUSCLK_R (OUT 41)
SLP_S5*/GPIO63 Y7 → PM_SLP_S5_L (OUT 12,40,65)
SLP_S4* C6 → PM_SLP_S4_L (OUT 12,21,33,37,40,65,78,83)
SLP_S3* H1 → PM_SLP_S3_L (OUT 12,21,40,65,83)
SLP_A* F3 → TP_PM_SLP_A_L
SLP_SUS* F1 → PM_SLP_SUS_L (OUT 12,65)
PMSYNCH AY3 → PM_SYNC (OUT 6,86)
SLP_LAN* G5 → TP_PCH_SLP_LAN_L
R1209 100K 5% 1/20W MF 201 (IN 40,83,88)

SYSTEM POWER MANAGEMENT

OMIT_TABLE

U1100 LYNXPOINT MOBILE FCBGA (5 OF 11)

VGA_BLUE T45 — NC
VGA_GREEN U44 — NC
VGA_RED V45 — NC
VGA_DDC_CLK M43 — NC
VGA_DDC_DATA M45 — NC
VGA_HSYNC N42 — NC
VGA_VSYNC N44 — NC
DAC_IREF U40
VGA_IRTN U39

VGA DAC Disabled per SB DG v1.0 (Table 12-18).

DDPB_CTRLCLK R40 → TP_DP_IG_B_DDC_CLK
DDPB_CTRLDATA (IPD-PLTRST#) R39 → TP_DP_IG_B_DDC_DATA
DDPC_CTRLCLK R35 → TP_DP_IG_C_DDC_CLK
DDPC_CTRLDATA (IPD-PLTRST#) R36 → TP_DP_IG_C_DDC_DATA
DDPD_CTRLCLK N40 → TP_DP_IG_D_DDC_CLK
DDPD_CTRLDATA (IPD-PLTRST#) N38 → TP_DP_IG_D_DDC_DATA
DDPB_AUXN H45 → TP_DP_IG_B_AUXCHN
DDPC_AUXN K43 → TP_DP_IG_C_AUXCHN
DDPD_AUXN J42 → TP_DP_IG_D_AUXCHN
DDPB_AUXP H43 → TP_DP_IG_B_AUXCHP
DDPC_AUXP K45 → TP_DP_IG_C_AUXCHP
DDPD_AUXP J44 → TP_DP_IG_D_AUXCHP
DDPB_HPD K40 → TP_DP_IG_B_HPD
DDPC_HPD K38 → TP_DP_IG_C_HPD
DDPD_HPD H39 → TP_DP_IG_D_HPD

CRT / DISPLAY / EDP

EDP_BKLTCTL N36 ← EDP_IG_BKL_PWM (OUT 84)
EDP_BKLTEN K36 ← EDP_IG_BKL_ON (OUT 82,12)
EDP_VDDEN G36 ← EDP_IG_PANEL_PWR (OUT 82,12)

PIRQA* H20 ← PCI_INTA_L
PIRQB* L20 ← PCI_INTB_L
PIRQC* K17 ← PCI_INTC_L
PIRQD* M20 ← PCI_INTD_L
=PP3V3_S0_PCH_GPIO
R1260 10K 5% 1/20W MF 201
R1261 10K 5% 1/20W MF 201
R1262 10K 5% 1/20W MF 201
R1263 10K 5% 1/20W MF 201

GPIO50 A12 ← ENET_LOW_PWR_PCH (OUT 82,12)
GPIO52 B13 ← AUD_IPHS_SWITCH_EN_PCH (OUT 82,12)
GPIO54 C12 ← BT_PWRRST_L (OUT 82,12)
GPIO51 C10 ← TP_PCH_STRP_BBS1
GPIO53 A10 ← TP_PCH_STRP_ESI_L
GPIO55 AL6 ← PCH_STRP_TOPBLK_SWP_L (IN 42)

PIRQE*/GPIO2 G17 → SDCONN_OC_L (IN 12,82)
PIRQF*/GPIO3 F17 → AUD_IP_PERIPHERAL_DET (IN 12,82)
PIRQG*/GPIO4 L15 → TBT_PWR_REQ_L (IN 12,29)
PIRQH*/GPIO5 M15 → AUD_I2C_INT_L (IN 12,82)
(IPU) PME* AD10 → TP_PCI_PME_L (84)
PLTRST* Y11 → PLT_RESET_L (OUT 18,20,21,83)
(IPU-PWROK&PCIRST#)

PCI

=PP3V3_S5_PCH_GPIO (14,81)
=PP3V3_S0_PCH_GPIO (11,12,14,20,29,81)

R1239 3.0K 5% 1/20W MF 201 — PM_PWRBTN_L (12,18,40,88)
R1240 10K 5% 1/20W MF 201 — PM_BATLOW_L (12,30,42)
R1291 10K 5% 1/20W MF 201 — PM_CLKRUN_L (12,40,49,83)
R1216 10K 5% 1/20W MF 201 — ENET_LOW_PWR_PCH (12,82)
R1217 100K 5% 1/20W MF 201 — AUD_IPHS_SWITCH_EN_PCH (12,82)
R1218 10K 5% 1/20W MF 201 — BT_PWRRST_L (12,82)
R1230 10K 5% 1/20W MF 201 — SDCONN_OC_L (12,82)
NO STUFF Redundant to pull-up on audio page
R1214 100K 5% 1/20W MF 201 — AUD_IP_PERIPHERAL_DET (12,82)
R1231 10K 5% 1/20W MF 201 — TBT_PWR_REQ_L (12,29)
NO STUFF Redundant to pull-up on audio page
R1233 10K 5% 1/20W MF 201 — AUD_I2C_INT_L (12,82)
R1225 1K 5% 1/20W MF 201 — PCIE_WAKE_L (12,33,35,83,88)
R1224 100K 5% 1/20W MF 201 — PM_SLP_S3_L (12,21,40,65,83)
R1221 100K 5% 1/20W MF 201 — PM_SLP_S4_L (12,21,33,37,40,65,78,83)
R1222 100K 5% 1/20W MF 201 — PM_SLP_S5_L (12,40,65)
R1223 100K 5% 1/20W MF 201 — PM_SLP_SUS_L (12,65)
R1281 100K 5% 1/20W MF 201 — EDP_IG_BKL_ON (12,82)
R1284 100K 5% 1/20W MF 201 — EDP_IG_PANEL_PWR (12,82)

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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USB3 Port Assignments:

Unused

PCIe/USB3 Port Assignments:

SD Card Reader
(& Ethernet if combo)

PCIe Port Assignments:

AirPort

Camera

SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD

OMIT_TABLE

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PCI-E

TP_USB3_SPARE_D2RN	AW31	PERN1_USB3RN3
TP_USB3_SPARE_D2RP	AY31	PERP1_USB3RP3
TP_USB3_SPARE_R2D_CN	BE32	PETN1_USB3TN3
TP_USB3_SPARE_R2D_CP	BC32	PETP1_USB3TP3
USB3RPCIE_SD_D2R_N	AT31	PERN2_USB3RN4
USB3RPCIE_SD_D2R_P	AR31	PERP2_USB3RP4
USB3RPCIE_SD_R2D_C_N	BD33	PETN2_USB3TN4
USB3RPCIE_SD_R2D_C_P	BB33	PETP2_USB3TP4
PCIE_AP_D2R_N	AW33	PERN3
PCIE_AP_D2R_P	AY33	PERP3
PCIE_AP_R2D_C_N	BE34	PETN3
PCIE_AP_R2D_C_P	BC34	PETP3
PCIE_CAMERA_D2R_N	AT33	PERN4
PCIE_CAMERA_D2R_P	AR33	PERP4
PCIE_CAMERA_R2D_C_N	BE36	PETN4
PCIE_CAMERA_R2D_C_P	BC36	PETP4
PCIE_SSD_D2R_N<0>	AW36	PERN5
PCIE_SSD_D2R_P<0>	AV36	PERP5
PCIE_SSD_R2D_C_N<0>	BD37	PETN5
PCIE_SSD_R2D_C_P<0>	BB37	PETP5
PCIE_SSD_D2R_N<1>	AY38	PERN6
PCIE_SSD_D2R_P<1>	AW38	PERP6
PCIE_SSD_R2D_C_N<1>	BC38	PETN6
PCIE_SSD_R2D_C_P<1>	BE38	PETP6
PCIE_SSD_D2R_N<2>	AT40	PERN7
PCIE_SSD_D2R_P<2>	AT39	PERP7
PCIE_SSD_R2D_C_N<2>	BE40	PETN7
PCIE_SSD_R2D_C_P<2>	BC40	PETP7
PCIE_SSD_D2R_N<3>	AN38	PERN8
PCIE_SSD_D2R_P<3>	AN39	PERP8
PCIE_SSD_R2D_C_N<3>	BD42	PETN8
PCIE_SSD_R2D_C_P<3>	BD41	PETP8

=PP1V5_S0_PCH_RCOMP

R1300 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.BD29:12.7mm

	BE30	PCIE_IREF
NC	BC30	TP11
NC	BB29	TP6
PCH_PCIE_RCOMP	BD29	PCIE_RCOMP

USB

USB2N0	B37	USB_EXTA_N
USB2P0	D37	USB_EXTA_P
USB2N1	A38	USB_EXTC_N
USB2P1	C38	USB_EXTC_P
USB2N2	A36	TP_USB_SDN
USB2P2	C36	TP_USB_SDP
USB2N3	A34	TP_USB_WLANN
USB2P3	C34	TP_USB_WLANP
USB2N4	B33	TP_USB_4N
USB2P4	D33	TP_USB_4P
USB2N5	F31	TP_USB_PSOCN
USB2P5	G31	TP_USB_PSOCP
USB2N6	K31	TP_USB_6N
USB2P6	L31	TP_USB_6P
USB2N7	G29	TP_USB_7N
USB2P7	H29	TP_USB_7P
USB2N8	A32	USB_EXTB_N
USB2P8	C32	USB_EXTB_P
USB2N9	A30	USB_EXTD_N
USB2P9	C30	USB_EXTD_P
USB2N10	B29	TP_USB_CAMERAN
USB2P10	D29	TP_USB_CAMERAP
USB2N11	A28	USB_BT_N
USB2P11	C28	USB_BT_P
USB2N12	G26	USB_IR_N
USB2P12	F26	USB_IR_P
USB2N13	F24	USB_TPAD_N
USB2P13	G24	USB_TPAD_P
(IPD)		

USB3RN1	AR26	USB3_EXTA_D2R_N
USB3RP1	AP26	USB3_EXTA_D2R_P
USB3TN1	BE24	USB3_EXTA_R2D_C_N
USB3TP1	BD23	USB3_EXTA_R2D_C_P
USB3RN2	AW26	USB3_EXTB_D2R_N
USB3RP2	AV26	USB3_EXTB_D2R_P
USB3TN2	BD25	USB3_EXTB_R2D_C_N
USB3TP2	BC24	USB3_EXTB_R2D_C_P
USB3RN5	AW29	USB3_EXTC_D2R_N
USB3RP5	AV29	USB3_EXTC_D2R_P
USB3TN5	BE26	USB3_EXTC_R2D_C_N
USB3TP5	BC26	USB3_EXTC_R2D_C_P
USB3RN6	AR29	USB3_EXTD_D2R_N
USB3RP6	AP29	USB3_EXTD_D2R_P
USB3TN6	BD27	USB3_EXTD_R2D_C_N
USB3TP6	BE28	USB3_EXTD_R2D_C_P

USBRBIAS*	K24	PCH_USB_RBIAS
USBRBIAS	K26	

PLACE_NEAR=U1100.K24:11.4mm
R1370 22.6 1% 1/20W MF 201

TP24	M33	NC
TP23	L33	NC

OC0*/GPIO59	P3	XDP_DA0_USB_EXTA_OC_L
OC1*/GPIO40	V1	XDP_DA1_USB_EXTC_OC_L
OC2*/GPIO41	U2	XDP_DA2_SSD_PWR_EN
OC3*/GPIO42	P1	XDP_DA3_CAMERA_PWR_EN
OC4*/GPIO43	M3	XDP_DB0_USB_EXTB_OC_L
OC5*/GPIO9	T1	XDP_DB1_USB_EXTD_OC_L
OC6*/GPIO10	N2	XDP_DB2_SD_PWR_EN
OC7*/GPIO14	M1	XDP_DB3_SDCONN_STATE_CHANGE_L

USB Port Assignments:

Ext A (LS/FS/HS)

Ext C (LS/FS/HS)

Reserved: SD (HS)

Reserved: WiFi (HS)

Unused

Reserved: PSOC (Legacy Trackpad)

Unused

Unused

Ext B (LS/FS/HS)

Ext D (LS/FS/HS)

Reserved: Camera

BT

IR

Trackpad

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

Ext C (SS)

Ext D (SS)

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
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LPC

LPC_AD<0>	R1340 33	LPC_AD_R<0>
LPC_AD<1>	R1341 33	LPC_AD_R<1>
LPC_AD<2>	R1342 33	LPC_AD_R<2>
LPC_AD<3>	R1343 33	LPC_AD_R<3>
LPC_FRAME_L	R1344 33	LPC_FRAME_R_L

5% 1/20W MF 201

LAD0 (IPU)	A20	LFRAME*
LAD1 (IPU)	C20	
LAD2 (IPU)	A18	
LAD3 (IPU)	C18	
TP_LPC_DREQ0_L	B21	
TBT_PWR_EN_PCH	D21	LDRQ0* (IPU)
LPC_SERIRQ	G20	LDRQ1*/(GPIO23 (IPU-LDRQ1#?)
	AL11	SERIRQ

SMBUS

SMBALERT*/GPIO11	N7	PCH_SMBALERT_L
SMBCLK	R10	SMBUS_PCH_CLK
SMBDATA	U11	SMBUS_PCH_DATA
SML0ALERT*/GPIO60	N8	PCH_SML0ALERT_L
SML0CLK	U8	SML_PCH_0_CLK
SML0DATA	R7	SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO74	H6	PCH_SML1ALERT_L
SML1CLK/GPIO58	K6	SML_PCH_1_CLK
SML1DATA/GPIO75	N11	SML_PCH_1_DATA

SPI

SPI_CLK_R	AJ11	SPI_CLK
SPI_CS0_R_L	AJ7	SPI_CS0* (IPU)
TP_SPI_CS1_L	AL7	SPI_CS1* (IPU)
TP_SPI_CS2_L	AJ10	SPI_CS2* (IPU)
SPI_MOSI_R	AH1	SPI_MOSI (IPD)
SPI_MISO	AH3	SPI_MISO (IPU)
SPI_IO<2>	AJ4	SPI_IO2 (IPU)
SPI_IO<3>	AJ2	SPI_IO3 (IPU)

C-LINK

(IPU/IPD) CL_CLK	AF11	TP_CLINK_CLK
(IPU/IPD) CL_DATA	AF10	TP_CLINK_DATA
CL_RST*	AF7	TP_CLINK_RESET_L

TP1	BA45	NC
TP2	BC45	NC
TP4	BE43	NC
TP3	BE44	NC
TD_IREF	AY43	PCH_TD_IREF

R1380 8.2K 1% 1/20W MF 201

=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_S3RS4_PCH_GPIO
=PP3V3_S3RS0_CAMPWREN
=PP3V3_S0_PCH

R1350 10K	LPC_SERIRQ	
R1351 10K	TBT_PWR_EN_PCH	
R1360 10K	XDP_DA0_USB_EXTA_OC_L	
R1361 10K	XDP_DA1_USB_EXTC_OC_L	
R1362 10K	SSD_PWR_EN	
R1368 10K	CAMERA_PWR_EN	
R1320 10K	XDP_DB0_USB_EXTB_OC_L	
R1321 10K	XDP_DB1_USB_EXTD_OC_L	
R1367 10K	SD_PWR_EN	
R1369 10K	XDP_DB3_SDCONN_STATE_CHANGE_L	
R1392 1K	SPI_IO<2>	
R1393 1K	SPI_IO<3>	
R1353 10K	PCH_SMBALERT_L	
R1354 10K	PCH_SML0ALERT_L	
R1355 10K	PCH_SML1ALERT_L	

5% 1/20W MF 201

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
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BRANCH: dvt
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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
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20 IN	=TBT_CIO_PLUG_EVENT_ISOL	AT8	BMBUSY*/GPIO0	
82 14 IN	FW_PME_L	F13	TACH1/GPIO1	
82 79 14 IN	DPMUX_UC_IRQ	A14	TACH2/GPIO6	
40 14 IN	SMC_RUNTIME_SCI_L	G15	TACH3/GPIO7	
18 OUT	XDP_FC0_HDD_PWR_EN	Y1	GPIO8 (IPU-RSMRST#)	
82 14 OUT	WOL_EN	K13	LAN_PHY_PWR_CTRL/GPIO12	
82 14 OUT	MEM_VDD_SEL_1V5_L	AB11	GPIO15	
18 14 IN	XDP_DD0_SSD_PCIE_SEL_L	AN2	SATA4GP/GPIO16 (IPU-BOOT/SATA4GP?)	
83 49 14 BI	LPCPLUS_GPIO	C14	TACH0/GPIO17	
20 14 OUT	JTAG_TBT_TMS_PCH	BB4	SCLOCK/GPIO22	
82 14 BI	TBT_GO2SX_BIDIR	Y10	GPIO24	
40 14 IN	SMC_WAKE_SCI_L	R11	GPIO27 (IPU-DeepSx)	
21 OUT	ISOLATE_CPU_MEM_L	AD11	GPIO28	
20 OUT	TBT_POC_RESET_L	AN6	GPIO34	
18 OUT	XDP_FC1_GPU_GOOD	AP1	GPIO35/NMI*	
18 OUT	XDP_DC2_ODD_PWR_EN_L	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)	
18 OUT	XDP_DC3_JTAG_ISP_TCK	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)	
20 14 IN	JTAG_ISP_TDO	AT7	SLOAD/GPIO38	
20 14 OUT	JTAG_ISP_TDI	AM3	SDATAOUT0/GPIO39	
82 14 OUT	FW_PWR_EN_PCH	AN4	SDATAOUT1/GPIO48	
	XDP_DD1_MLB_RAMCFG1	AK3	SATA5GP/GPIO49 (IPU-BOOT/SATA5GP?)	
83 49 14 BI	SPIROM_USE_MLB	U12	GPIO57	
20	MLB_RAMCFG3	C16	TACH4/GPIO68	
20	MLB_RAMCFG2	D13	TACH5/GPIO69	
20 IN	SD_SEL_PCIE_L_USB_H	G13	TACH6/GPIO70 (IPU-BOOT?)	
20	MLB_RAMCFG0	H15	TACH7/GPIO71 (IPU-BOOT?)	
		BE41		
		BE5		
		C45	VSS	
		A5		

CPU/MISC

GPIO

TP14	AN10	PCH_A20GATE	14
(IPD) PECI	AY1	PCH_PECI	
RCIN*	AT6	PCH_RCIN_L	14 88
PROCPWRGD	AV3	PCH_PROCPWRGD	
THRMTRIP*	AV1	PM_THRMTRIP_L_R	18 41
PLTRST_PROC*	AU4	CPU_RESET_L	OUT 6
VSS	N10		
	A2		
	A41		
	A43		
	A44		
	B1		
	B2		
	B44		
	B45		
	BA1		
	BC1		
	BD1		
	BD2		
VSS	BD44		
	BD45		
	BE2		
	BE3		
	D1		
	E1		
	E45		
	A4		

=PP1V05_S0_PCH_V_PROC_IO 15 17 81

NO STUFF
R1457 1K 5% 1/16W MF-LF 402

NO STUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI BI 6 41 86
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD OUT 6 18 86
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L IN 6 41 86

=PP3V3_S0_PCH_GPIO 81 29 20 14 12 11

RAMCFG0:H	R1475 10K 5% 1/20W MF 201	
RAMCFG1:H	R1474 10K 5% 1/20W MF 201	
RAMCFG2:H	R1473 10K 5% 1/20W MF 201	
RAMCFG3:H	R1472 10K 5% 1/20W MF 201	

18 IN

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

=PP3V3_S5_PCH_GPIO 12 81
=PP3V3_SUS_PCH_GPIO 11 12 13 81
=PP3V3_S0_PCH_GPIO 11 12 14 20 29 81

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K 5% 1/20W MF 201	FW_PME_L 14 82
R1411	20K 5% 1/20W MF 201	DPMUX_UC_IRQ 14 79 82
R1496	10K 5% 1/20W MF 201	SMC_RUNTIME_SCI_L 14 40
R1494	10K 5% 1/20W MF 201	WOL_EN 14 82
R1489	10K 5% 1/20W MF 201	MEM_VDD_SEL_1V5_L 14 82
R1495	100K 5% 1/20W MF 201	XDP_DD0_SSD_PCIE_SEL_L 14 18
R1490	100K 5% 1/20W MF 201	LPCPLUS_GPIO 14 49 83
R1412	10K 5% 1/20W MF 201	JTAG_TBT_TMS_PCH 14 20
R1492	10K 5% 1/20W MF 201	TBT_GO2SX_BIDIR 14 82
R1491	10K 5% 1/20W MF 201	SMC_WAKE_SCI_L 14 40
R1498	10K 5% 1/20W MF 201	ODD_PWR_EN_L 18
R1413	10K 5% 1/20W MF 201	JTAG_ISP_TCK 18 20
R1486	10K 5% 1/20W MF 201	JTAG_ISP_TDO 14 20
R1499	10K 5% 1/20W MF 201	JTAG_ISP_TDI 14 20
R1484	10K 5% 1/20W MF 201	FW_PWR_EN_PCH 14 82
R1493	100K 5% 1/20W MF 201	SPIROM_USE_MLB 14 49 83

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	PCH_A20GATE 14
R1455	10K 5% 1/20W MF 201	PCH_RCIN_L 14 88

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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OMIT_TABLE

U1100
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MOBILE
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=PP1V05_S0_PCH_VCC
VCC: 1.312 A Max, 130mA Idle

Y26, AA24, AA26, AD20, AD22, AD24, AD26, AD28, AE18, AE20, AE22, AE24, AE26, AG18, AG20, AG22, AG24 → VCC

PLACE_NEAR=R1550.1:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

C1550 1UF ±10% 6.3V CERM 402

R1550 5.11 1% 1/20W MF-LF 201

PLACE_NEAR=U1100.U14:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

Powered in DeepSx

U14 → DCPSUSBYP

=PP1V05_S0M_PCH_VCCASW
VCCASW: 670mA Max, 34mA Idle

U18, U20, U22, U24, V18, V20, V22, V24, Y18, Y20, Y22, AA18 → VCCASW

CORE:

- CRT: VCCADAC1_5 P45 — CKPLUS_WAIVE=PwrTerm2Gnd; VGA DAC Disabled per SB DG v1.0 (Table 12-18).
- CRT: VSS P43
- CRT: VCCADACBG3_3 M31 — CKPLUS_WAIVE=PwrTerm2Gnd
- FDI: VCCVRM BB44 — =PP1V5_S0_PCH_VCCVRM_FDI; VCCVRM: 183mA Max, 68mA Idle
- FDI: VCCIO AN34, AN35 — =PP1V05_S0_PCH_VCCIO_FDI; VCCIO: 3629mA Max, 264mA Idle
- HVCMOS: VCC3_3 R30, R32 — =PP3V3_S0_PCH_VCC3_3_HVCMOS; VCC3_3: 133mA Max, 3mA Idle
- USB3: DCPSUS1 Y12 — NC
- USB3: VCCSUS3_3 AJ30, AJ32 — =PP3V3_SUS_PCH_VCCSUS_USB3; VCCSUS3_3: 261mA Max, 6mA Idle
- USB3: DCPSUS3 AJ26, AJ28 — NC, NC
- USB3: VCCIO AK20 — =PP1V05_S0_PCH_VCCIO; VCCIO: 3629mA Max, 264mA Idle
- USB3: VCCVRM AK26, AK28 — =PP1V05_S0_PCH_VCCVRM_USB3; VCCVRM: 183mA Max, 68mA Idle
- PCIE/DMI: VCCVRM BE22 — =PP1V5_S0_PCH_VCCVRM_PCIE; VCCVRM: 183mA Max, 68mA Idle
- PCIE/DMI: VCCIO AK18
- SATA: VCCVRM AN11 — =PP1V5_S0_PCH_VCCVRM_SATA; VCCVRM: 183mA Max, 68mA Idle
- SATA: VCCIO AK22
- VCCMPHY: VCCIO AM18, AM20, AM22, AP22, AR22, AT22

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(8 OF 11)

=PP3V3_SUS_PCH_VCCSUS_USB
VCCSUS3_3: 261mA Max, 6mA Idle

R24, R26, R28, U26 → VCCSUS3_3

M24 → VSS

=PP1V05_S0_PCH_VCCUSBPLL
??mA Max, ??mA Idle

U35 → VCCUSBPLL

=PP3V3_S0_PCH_VCC3_3_USB
VCC3_3: 133mA Max, 3mA Idle

L24 → VCC3_3

=PP1V05_S0_PCH_VCCIO_USB2
VCCIO: 3629mA Max, 264mA Idle

U30, V28, V30, Y30 → VCCIO

Y35 → NC — DCPSUS2

=PP1V5_S0_PCH_VCCVRM_CLK
VCCVRM: 183mA Max, 68mA Idle

AF34 → VCCVRM

PP1V05_S0_PCH_VCC_CLK_F
??mA Max, ??mA Idle

AP45 → VCC

=PP1V05_S0_PCH_VCCCLK_SSC
VCCCLK: 306mA Max, 89mA Idle

Y32 → VCCCLK

=PP3V3_S0_PCH_VCCCLK3_3
VCCCLK3_3: 55mA Max, 11mA Idle

M29, L29, L26, M26, U32, V32 → VCCCLK3_3

=PP1V05_S0_PCH_VCCCLK_CLK135
VCCCLK: 306mA Max, 89mA Idle

AD34 → AA30, AA32

=PP1V05_S0_PCH_VCCCLK_CLK100

AD35 → AG30, AG32, AD36, AE30, AE32

=PP1V05_S0_PCH_VCCCLK_SSC100
VCCCLK: 306mA Max, 89mA Idle

VCCCLK

USB:

- VCCSUS3_3 R20, R22 — =PP3V3_SUS_PCH_VCCSUS_GPIO; VCCSUS3_3: 261mA Max, 6mA Idle
- VCCDSW3_3 A16 — =PP3V3_S5_PCH_VCCDSW; 15 mA Max, 1mA Idle
- DCPSST AA14 — PPVOUT_S0_PCH_DCPSST; BYPASS=U1100.AA14:6.35mm; MIN_LINE_WIDTH=0.2 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=1.05V; C1580 0.1UF 20% 10V CERM 402
- VCC3_3 AE14, AF12, AG14 — =PP3V3_S0_PCH_VCC3_3_GPIO; VCC3_3: 133mA Max, 3mA Idle
- VCCIO U36 — =PP1V05_S0_PCH_VCCIO_GPIO; VCCIO: 3629mA Max, 264mA Idle
- HDA: VCCSUSHDA A26 — =PP3V3R1V5_S0_PCH_VCCSUSHDA; 10mA Max, 1mA Idle
- RTC: VCCSUS3_3 K8 — =PP3V3_SUS_PCH_VCCSUS_RTC; VCCSUS3_3: 261mA Max, 6mA Idle
- RTC: VCCRTC A6 — =PPVRTC_G3_PCH; 6uA Max (3.0V, room temperature); C1533 0.1UF 20% 10V CERM 402; C1532 0.1UF 20% 10V CERM 402; C1531 1UF 10% 6.3V CERM 402; BYPASS=U1100.A6:6.35mm
- RTC: DCPRTC P14, P16 — PPVOUT_S0_PCH_DCPRTC; BYPASS=U1100.P14:6.35mm; MIN_LINE_WIDTH=0.2 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=1.05V; C1590 0.1UF 20% 10V CERM 402
- CPU: V_PROC_IO AJ12, AJ14 — =PP1V05_S0_PCH_V_PROC_IO; 4mA Max, 2mA Idle
- SPI: VCCSPI AD12 — =PP3V3_SUS_PCH_VCC_SPI; 22mA Max, 1mA Idle
- CLK/MISC: NOTE: Pin name is VCC but really is 3.3V
- VCC P18, P20 — =PP3V3_S0_PCH_VCC_FUSE; ??mA Max, ??mA Idle
- VCCASW L17, R18 — =PP1V05_S0M_PCH_VCCASW; VCCASW: 670mA Max, 34mA Idle; =PP1V05_S0M_PCH_VCCASW; VCCASW: 670mA Max, 34mA Idle
- THERMAL: VCCVRM AW40 — =PP1V5_S0_PCH_VCCVRM_THRM; VCCVRM: 183mA Max, 68mA Idle
- VCC3_3 AK30, AK32 — =PP3V3_S0_PCH_VCC3_3_THRM; VCC3_3: 133mA Max, 3mA Idle

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: PCH Power

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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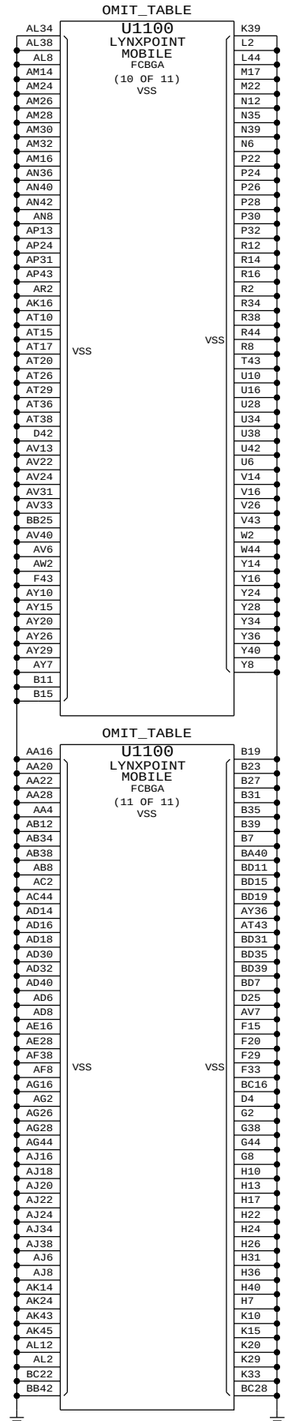

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
=PP3V3_S5_PCH_VCCDSW
C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
=PP3V3_SUS_PCH_VCC_SPI
C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
=PP3V3_SUS_PCH_VCCSUS_GPIO
C1704 0.1UF 20% 10V CERM 402
BYPASS=U1100.R20:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
=PP3V3_SUS_PCH_VCCSUS_USB
C1706 0.1UF 20% 10V CERM 402
BYPASS=U1100.R26:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
=PP3V3_SUS_PCH_VCCSUS_RTC
C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8:6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
=PP3V3_S0_PCH_VCCCLK3_3
C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26:6.35mm
BYPASS=U1100.L29:6.35mm
BYPASS=U1100.M29:6.35mm
BYPASS=U1100.U32:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
=PP3V3_S0_PCH_VCC3_3_HVCMOS
C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.R30:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
=PP3V3_S0_PCH_VCC3_3_GPIO
C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
=PP3V3_S0_PCH_VCC3_3_USB
C1730 0.1UF 20% 10V CERM 402
BYPASS=U1100.L24:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
=PP3V3_S0_PCH_VCC3_3_THRM
C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK30:6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
=PP3V3_S0_PCH_VCC_FUSE
C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
=PP1V05_S0M_PCH_VCCASW
670mA Max, 34mA Idle
C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
=PP1V05_S0_PCH_VCC
C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18:12.7mm
BYPASS=U1100.AG24:6.35mm
BYPASS=U1100.AP20:6.35mm
BYPASS=U1100.AE18:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
=PP1V05_S0_PCH_VCCIO
C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18:12.7mm
BYPASS=U1100.AK18:6.35mm
BYPASS=U1100.AK22:6.35mm
BYPASS=U1100.AK20:6.35mm
BYPASS=U1100.AM18:6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
=PP1V05_S0_PCH_VCCUSBPLL
C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
=PP1V05_S0_PCH_VCCIO_FDI
C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
=PP1V05_S0_PCH_VCCIO_USB2
C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30:6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
=PP1V05_S0_PCH_V_PROC_IO
C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12:12.7mm
BYPASS=U1100.AJ12:6.35mm
BYPASS=U1100.AJ12:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
=PP1V05_S0_PCH_VCCCLK_SSC100
C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30:6.35mm
BYPASS=U1100.AG30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
=PP1V05_S0_PCH_VCCCLK_CLK100
C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
=PP1V05_S0_PCH_VCCCLK_CLK135
C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
=PP1V05_S0_PCH_VCCCLK_SSC
C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
=PP3V3R1V5_S0_PCH_VCCSUSHDA
C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26:6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
=PP1V5_S0_PCH_VCCVRM
183mA Max, 68mA Idle
=PP1V5_S0_PCH_VCCVRM_BIAS
=PP1V5_S0_PCH_VCCVRM_FDI
=PP1V5_S0_PCH_VCCVRM_USB3
=PP1V5_S0_PCH_VCCVRM_PCIE
=PP1V5_S0_PCH_VCCVRM_SATA
=PP1V5_S0_PCH_VCCVRM_CLK
=PP1V5_S0_PCH_VCCVRM_THRM
C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34:12.7mm

=PP1V05_S0_PCH_VCC_CLK
??mA Max, ??mA Idle
R1790 1 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603
PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45:12.7mm
BYPASS=U1100.AP45:6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

518S0847

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

=PP1V05_S0_CPU_JTAG → R1830 150 5% 1/16W MF-LF 402

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

CPU_PWRGD → R1800 1K XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.F50:2.54mm
PM_PWRBTN_L → R1802 0 XDP 5% 1/20W MF 0201 PLACE_NEAR=U5000.J3:2.54mm
PM_PCH_SYS_PWROK → R1804 0 XDP 5% 1/16W MF-LF 402

R1805 1K XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.A67:2.54mm
PLT_RESET_L → XDP_DBRESET_L
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

XDP_CPU_PRESENT_L

CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 → XDP_CPU_TDO
CRITICAL XDP Q1840 DMN5L06VK-7 SOT-563 → XDP_CPUPCH_TRST_L → XDP_CPU_TRST_L
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 → XDP_CPU_TDI
CRITICAL XDP Q1842 DMN5L06VK-7 SOT-563 → XDP_CPU_TMS

PLACE_NEAR=J1800.51:28mm
PLACE_NEAR=J1800.53:28mm
PLACE_NEAR=J1800.55:28mm
PLACE_NEAR=J1800.57:28mm
MAKE_BASE=TRUE

=PP1V05_S0_CPU_JTAG
XDP_CPU_TDO → R1820 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.M49:28mm
XDP_CPU_TCK → R1823 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.N54:28mm
XDP_CPU_TRST_L → R1824 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U0500.M53:28mm

TDI and TMS are terminated in CPU.

CPU JTAG Isolation

=PP5V_S0_XDPJTAGISOL
=PP3V3_S5_XDPJTAGISOL
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

=PP1V05_SUS_PCH_JTAG
XDP_PCH_TDO → R1860 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AD3:28mm
XDP_PCH_TDI → R1861 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AE2:28mm
XDP_PCH_TMS → R1862 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AD1:28mm
XDP_PCH_TCK → R1866 51 XDP 5% 1/20W MF 201 PLACE_NEAR=U1100.AB3:28mm

PCH/XDP Signals

OMIT (All 10 R's)

XDP_DA0_USB_EXTA_OC_L	R1890	SHORT		USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT		SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT		CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT		USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT		SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT		SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT		DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN		MAKE_BASE=TRUE		SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L		MAKE_BASE=TRUE		ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT		JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT		SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1		MAKE_BASE=TRUE		MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L		MAKE_BASE=TRUE		ENETSD_CLKREQ_L
XDP_DD3_AP_CLKREQ_L	R1879	SHORT		AP_CLKREQ_L

NONE NONE NONE 201

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

(TP-P6)

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU & PCH XDP

Apple Inc.

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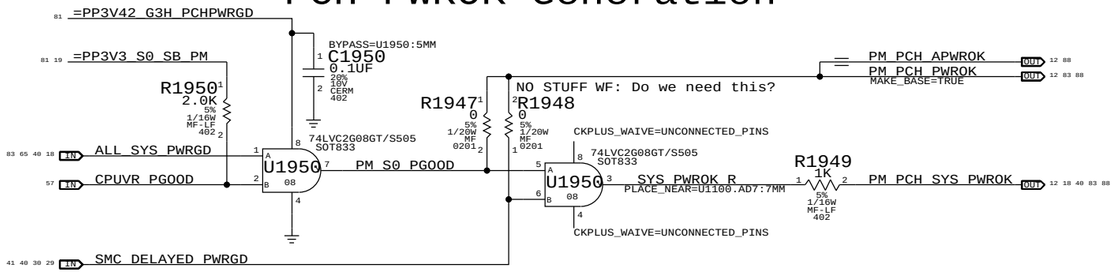
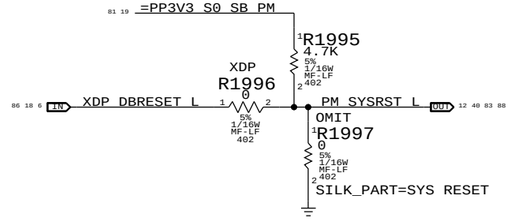
PCH PWROK Generation

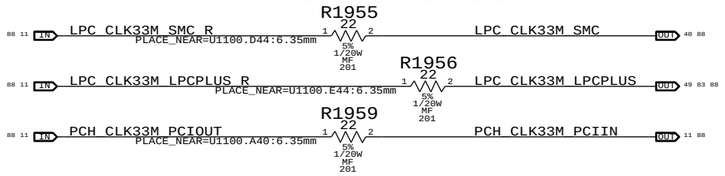


NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

PCH Reset Button

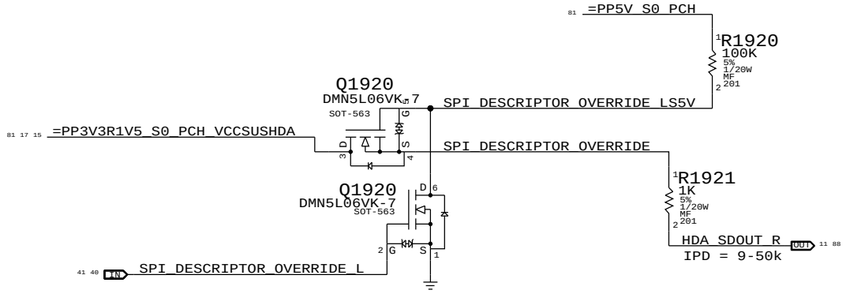


PCH 33MHz Clocks



PCH ME Disable Strap

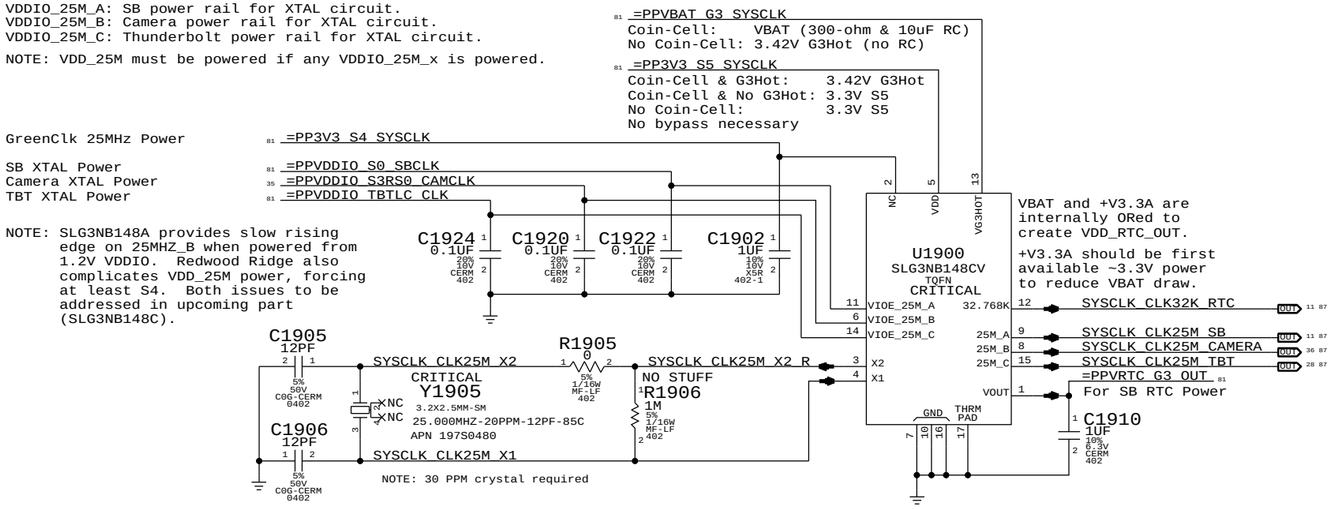
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



NOTE: 30 PPM crystal required

NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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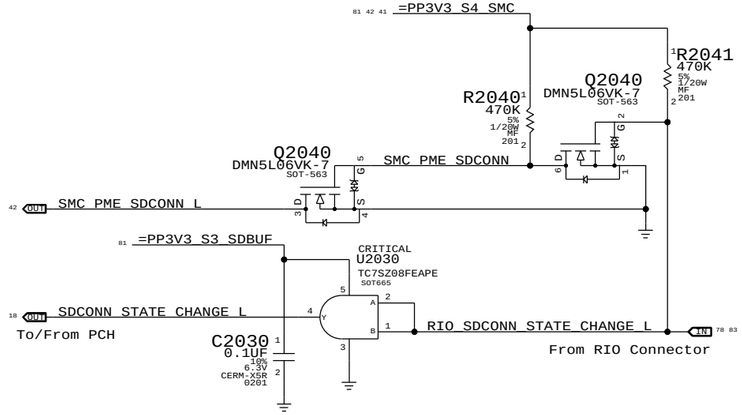
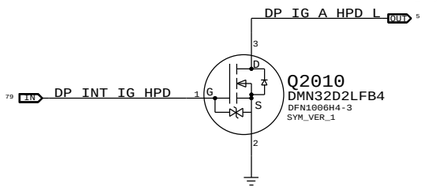
RIO SD Card Reader Support

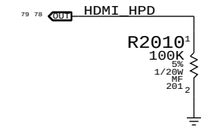


LCD HPD Inverter

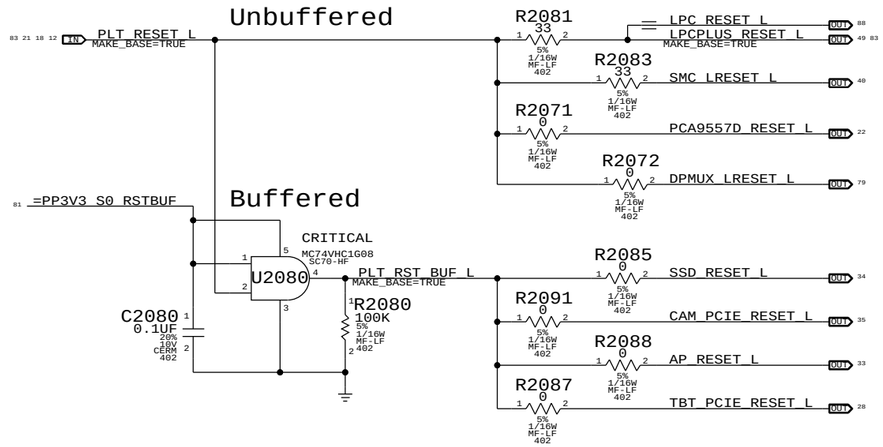
(Pull-Up on CPU Page)



HDMI HPD pull-down

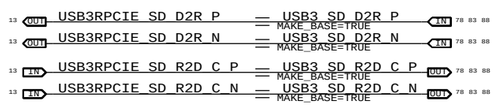


Platform Reset Connections



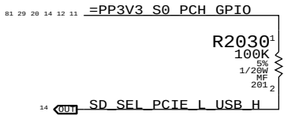
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



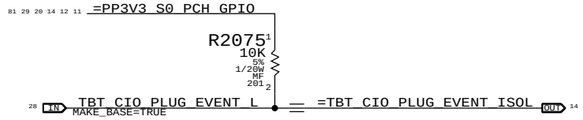
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe



Redwood Ridge Support

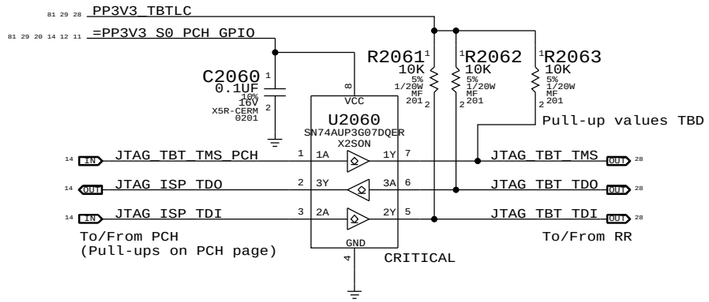
RR output is open-drain, no isolation necessary



PCH 33MHz Clock for DPMUX

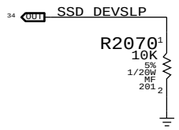
Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V

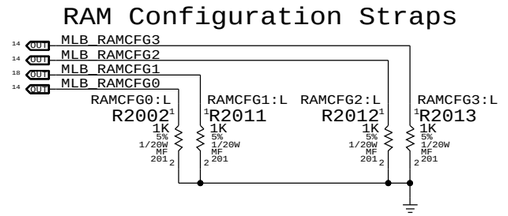


GS3 Connector Support

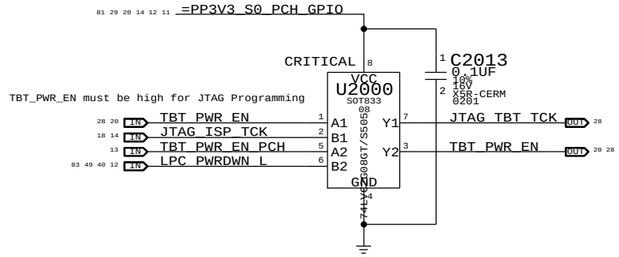
DEVSLP not supported on LPT-H



RAM Configuration Straps



GPIO Glitch Prevention



GND

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE

Project Chipset Support

Apple Inc.

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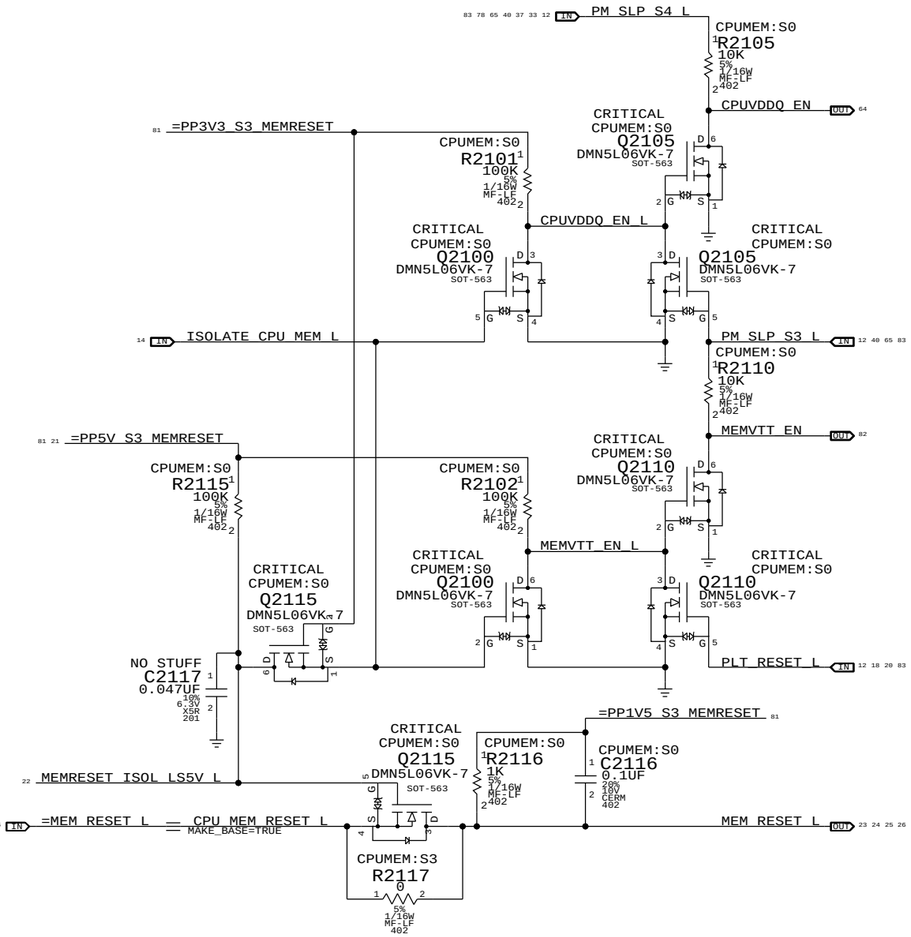
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



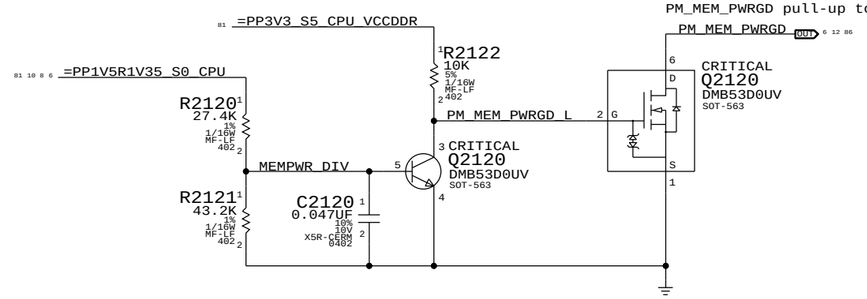
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
S3	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

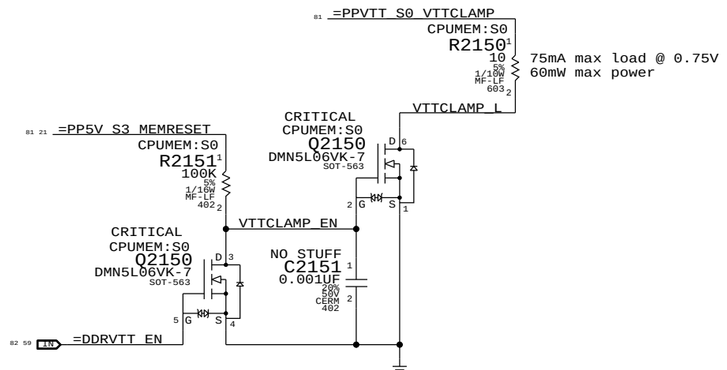
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



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PAGE TITLE: CPU Memory S3 Support

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

MEMRESET_ISOL_LS5V_L
CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches

DDRVREF_DAC R2225 100K 1% 1/16W MF-LF 402 — VREFMRGN_DQ_A_EN_RC — DDRVREF_DAC C2225 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2245 100K 1% 1/16W MF-LF 402 — VREFMRGN_DQ_B_EN_RC — DDRVREF_DAC C2245 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2265 100K 1% 1/16W MF-LF 402 — VREFMRGN_CA_A_EN_RC — DDRVREF_DAC C2265 0.1UF 20% 10V CERM 402
DDRVREF_DAC R2285 100K 1% 1/16W MF-LF 402 — VREFMRGN_CA_B_EN_RC — DDRVREF_DAC C2285 0.1UF 20% 10V CERM 402

DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC R2208 100K 5% 1/20W MF 201

CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 — VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 — VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

=PPDDR_S3_MEMVREF

PLACE_NEAR=C2220.1:2mm — R2223 2 5% 1/20W MF 201 — PLACE_NEAR=R2221.2:1mm — R2221 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2223.2:1mm — PPVREF_S3_MEM_VREFDQ_A
PLACE_NEAR=Q2220.6:2mm — C2220 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_A_RC — R2220 24.9 1% 1/20W MF 201 — PLACE_NEAR=R2222.2:1mm — R2222 1K 1% 1/16W MF-LF 402
PLACE_NEAR=C2240.1:2mm — R2243 2 5% 1/20W MF 201 — PLACE_NEAR=R2241.2:1mm — R2241 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2243.2:1mm — PPVREF_S3_MEM_VREFDQ_B
PLACE_NEAR=Q2260.6:2mm — C2240 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_B_RC — R2240 24.9 1% 1/20W MF 201 — PLACE_NEAR=R2242.2:1mm — R2242 1K 1% 1/16W MF-LF 402
PLACE_NEAR=C2260.1:2mm — R2263 2 5% 1/20W MF 201 — PLACE_NEAR=R2261.2:1mm — R2261 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2263.2:1mm — PPVREF_S3_MEM_VREFCA_A
PLACE_NEAR=Q2220.3:2mm — C2260 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_A_RC — R2260 24.9 1% 1/20W MF 201 — PLACE_NEAR=R2262.2:1mm — R2262 1K 1% 1/16W MF-LF 402
PLACE_NEAR=C2280.1:2mm — R2283 2 5% 1/20W MF 201 — PLACE_NEAR=R2281.2:1mm — R2281 1K 1% 1/16W MF-LF 402 — PLACE_NEAR=R2283.2:1mm — PPVREF_S3_MEM_VREFCA_B
PLACE_NEAR=Q2260.3:2mm — C2280 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_B_RC — R2280 24.9 1% 1/20W MF 201 — PLACE_NEAR=R2282.2:1mm — R2282 1K 1% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

=PP3V3_S3_VREFMRGN — OMIT R2218 SHORT NONE NONE NONE NONE 402 — PP3V3_S3_VREFMRGN (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574
VDD 8
SCL 6 — =I2C_VREFDACS_SCL
SDA 7 — =I2C_VREFDACS_SDA
A0 9
A1 10
GND 3
VOUTA 1 — VREFMRGN_DQ_A
VOUTB 2 — VREFMRGN_DQ_B
VOUTC 4 — VREFMRGN_CA_AB
VOUTD 5 — VREFMRGN_MEMVREG_FBVREF

Addr=0x98(WR)/0x99(RD)

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2201 QFN PCA9557 (OD)
VCC 16
A0 3
A1 4
A2 5
SCL 1 — =I2C_PCA9557D_SCL
SDA 2 — =I2C_PCA9557D_SDA
P0 6 — NC
P1 7 — VREFMRGN_DQ_A_EN
P2 9 — VREFMRGN_DQ_B_EN
P3 10 — VREFMRGN_CA_A_EN
P4 11 — VREFMRGN_CA_B_EN
P5 12 — VREFMRGN_MEMVREG_EN
P6 13 — VREFMRGN_FRAMEBUF_EN
P7 14 — NC
RESET* 15 — PCA9557D_RESET_L
THRM PAD 17
GND 8

Addr=0x30(WR)/0x31(RD)

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

=PP3V3_S3_VREFMRGN

DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402 — DDRREG_FB

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 5% 1/16W MF-LF 402

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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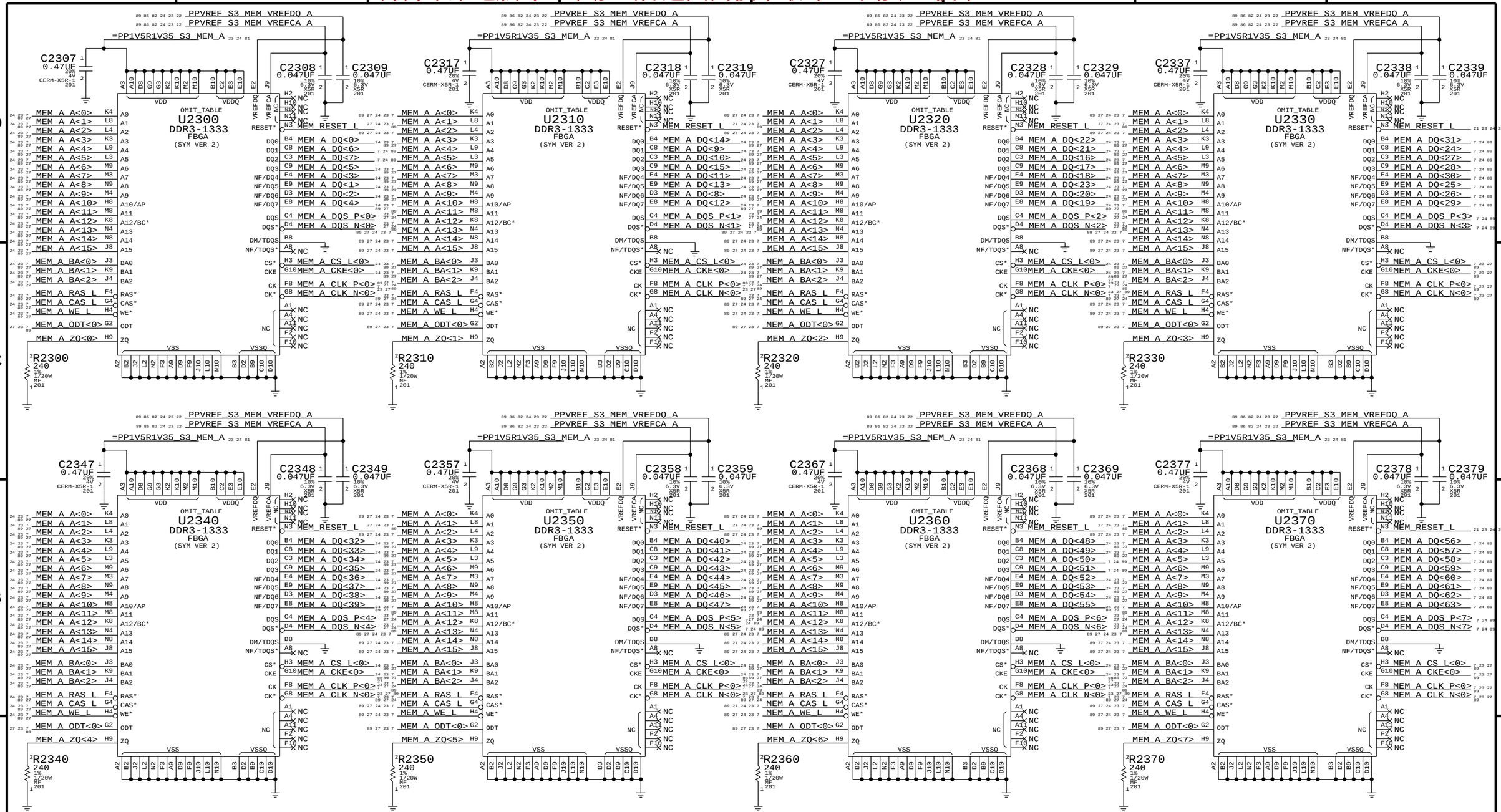

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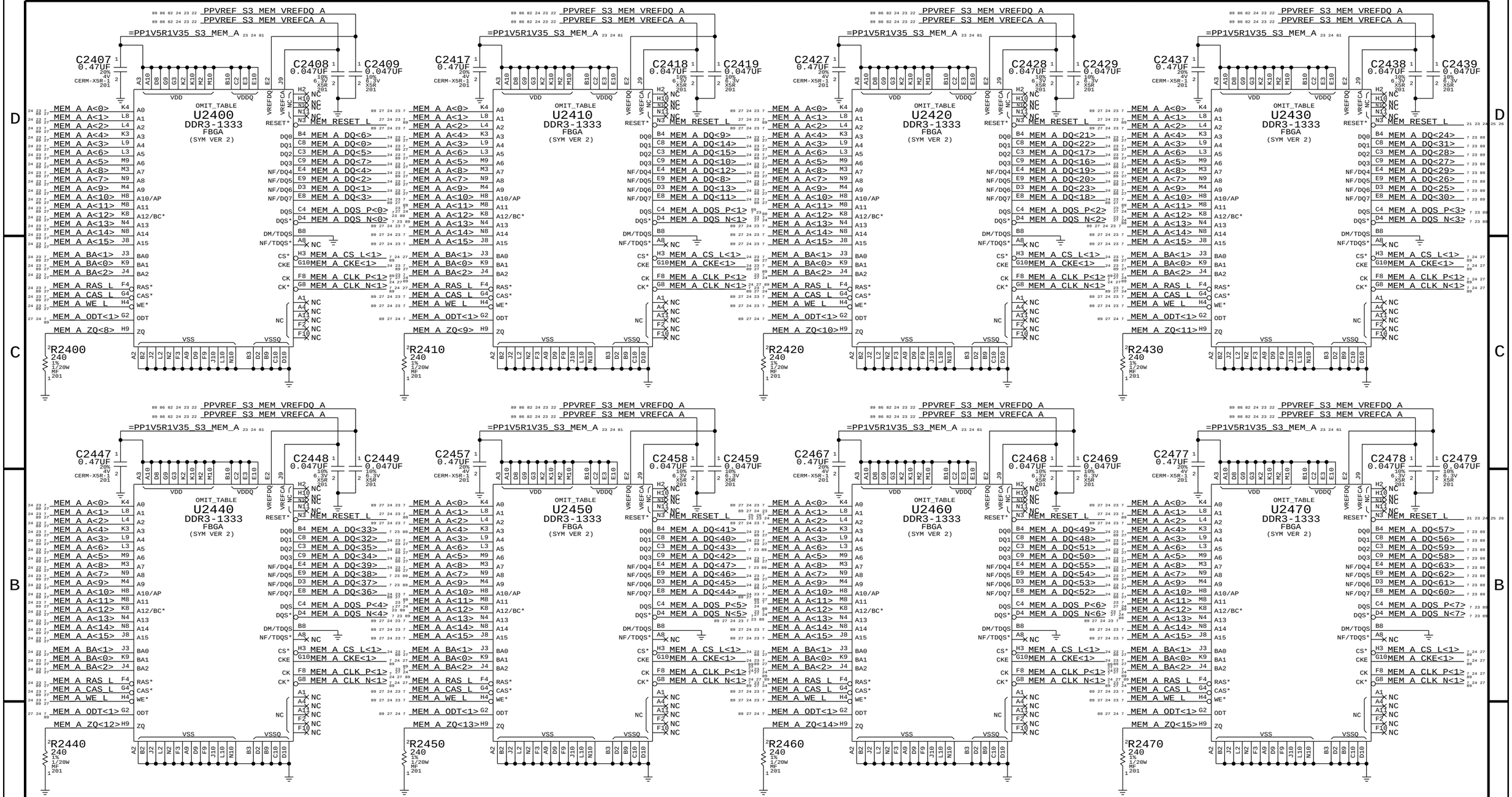
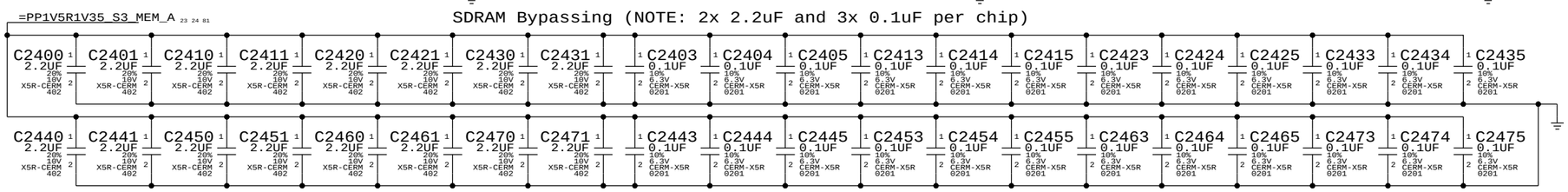


SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)



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=PP1V5R1V35_S3_MEM_B

PPVREF_S3_MEM_VREFDQ_B
PPVREF_S3_MEM_VREFCA_B

C2507 0.47UF 20% 4V CERM-X5R-1 201
C2508 0.047UF 10% 6.3V X5R 201
C2509 0.047UF 10% 6.3V X5R 201

U2500 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<0>
MEM_RESET_L

MEM_B_DQ<6> MEM_B_DQ<1> MEM_B_DQ<3> MEM_B_DQ<5> MEM_B_DQ<2> MEM_B_DQ<4> MEM_B_DQ<7> MEM_B_DQ<0>
MEM_B_DQS_P<0> MEM_B_DQS_N<0>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2500 240 1% 1/20W MF 201

C2517 0.47UF 20% 4V CERM-X5R-1 201
C2518 0.047UF 10% 6.3V X5R 201
C2519 0.047UF 10% 6.3V X5R 201

U2510 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<1>
MEM_RESET_L

MEM_B_DQ<14> MEM_B_DQ<9> MEM_B_DQ<11> MEM_B_DQ<13> MEM_B_DQ<10> MEM_B_DQ<12> MEM_B_DQ<15> MEM_B_DQ<8>
MEM_B_DQS_P<1> MEM_B_DQS_N<1>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2510 240 1% 1/20W MF 201

C2527 0.47UF 20% 4V CERM-X5R-1 201
C2528 0.047UF 10% 6.3V X5R 201
C2529 0.047UF 10% 6.3V X5R 201

U2520 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<2>
MEM_RESET_L

MEM_B_DQ<18> MEM_B_DQ<20> MEM_B_DQ<19> MEM_B_DQ<16> MEM_B_DQ<23> MEM_B_DQ<21> MEM_B_DQ<22> MEM_B_DQ<17>
MEM_B_DQS_P<2> MEM_B_DQS_N<2>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2520 240 1% 1/20W MF 201

C2537 0.47UF 20% 4V CERM-X5R-1 201
C2538 0.047UF 10% 6.3V X5R 201
C2539 0.047UF 10% 6.3V X5R 201

U2530 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<3>
MEM_RESET_L

MEM_B_DQ<27> MEM_B_DQ<25> MEM_B_DQ<26> MEM_B_DQ<29> MEM_B_DQ<30> MEM_B_DQ<28> MEM_B_DQ<31> MEM_B_DQ<24>
MEM_B_DQS_P<3> MEM_B_DQS_N<3>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2530 240 1% 1/20W MF 201

C2547 0.47UF 20% 4V CERM-X5R-1 201
C2548 0.047UF 10% 6.3V X5R 201
C2549 0.047UF 10% 6.3V X5R 201

U2540 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<4>
MEM_RESET_L

MEM_B_DQ<32> MEM_B_DQ<33> MEM_B_DQ<34> MEM_B_DQ<35> MEM_B_DQ<36> MEM_B_DQ<37> MEM_B_DQ<38> MEM_B_DQ<39>
MEM_B_DQS_P<4> MEM_B_DQS_N<4>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2540 240 1% 1/20W MF 201

C2557 0.47UF 20% 4V CERM-X5R-1 201
C2558 0.047UF 10% 6.3V X5R 201
C2559 0.047UF 10% 6.3V X5R 201

U2550 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<5>
MEM_RESET_L

MEM_B_DQ<40> MEM_B_DQ<41> MEM_B_DQ<42> MEM_B_DQ<43> MEM_B_DQ<44> MEM_B_DQ<45> MEM_B_DQ<46> MEM_B_DQ<47>
MEM_B_DQS_P<5> MEM_B_DQS_N<5>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2550 240 1% 1/20W MF 201

C2567 0.47UF 20% 4V CERM-X5R-1 201
C2568 0.047UF 10% 6.3V X5R 201
C2569 0.047UF 10% 6.3V X5R 201

U2560 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<6>
MEM_RESET_L

MEM_B_DQ<48> MEM_B_DQ<49> MEM_B_DQ<50> MEM_B_DQ<51> MEM_B_DQ<52> MEM_B_DQ<53> MEM_B_DQ<54> MEM_B_DQ<55>
MEM_B_DQS_P<6> MEM_B_DQS_N<6>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2560 240 1% 1/20W MF 201

C2577 0.47UF 20% 4V CERM-X5R-1 201
C2578 0.047UF 10% 6.3V X5R 201
C2579 0.047UF 10% 6.3V X5R 201

U2570 DDR3-1333 FBGA (SYM VER 2) OMIT_TABLE

MEM_B_A<0> MEM_B_A<1> MEM_B_A<2> MEM_B_A<3> MEM_B_A<4> MEM_B_A<5> MEM_B_A<6> MEM_B_A<7> MEM_B_A<8> MEM_B_A<9> MEM_B_A<10> MEM_B_A<11> MEM_B_A<12> MEM_B_A<13> MEM_B_A<14> MEM_B_A<15>
MEM_B_BA<0> MEM_B_BA<1> MEM_B_BA<2>
MEM_B_RAS_L MEM_B_CAS_L MEM_B_WE_L
MEM_B_ODT<0>
MEM_B_ZQ<7>
MEM_RESET_L

MEM_B_DQ<56> MEM_B_DQ<57> MEM_B_DQ<58> MEM_B_DQ<59> MEM_B_DQ<60> MEM_B_DQ<61> MEM_B_DQ<62> MEM_B_DQ<63>
MEM_B_DQS_P<7> MEM_B_DQS_N<7>
MEM_B_CS_L<0> MEM_B_CKE<0>
MEM_B_CLK_P<0> MEM_B_CLK_N<0>

R2570 240 1% 1/20W MF 201

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

=PP1V5R1V35_S3_MEM_B

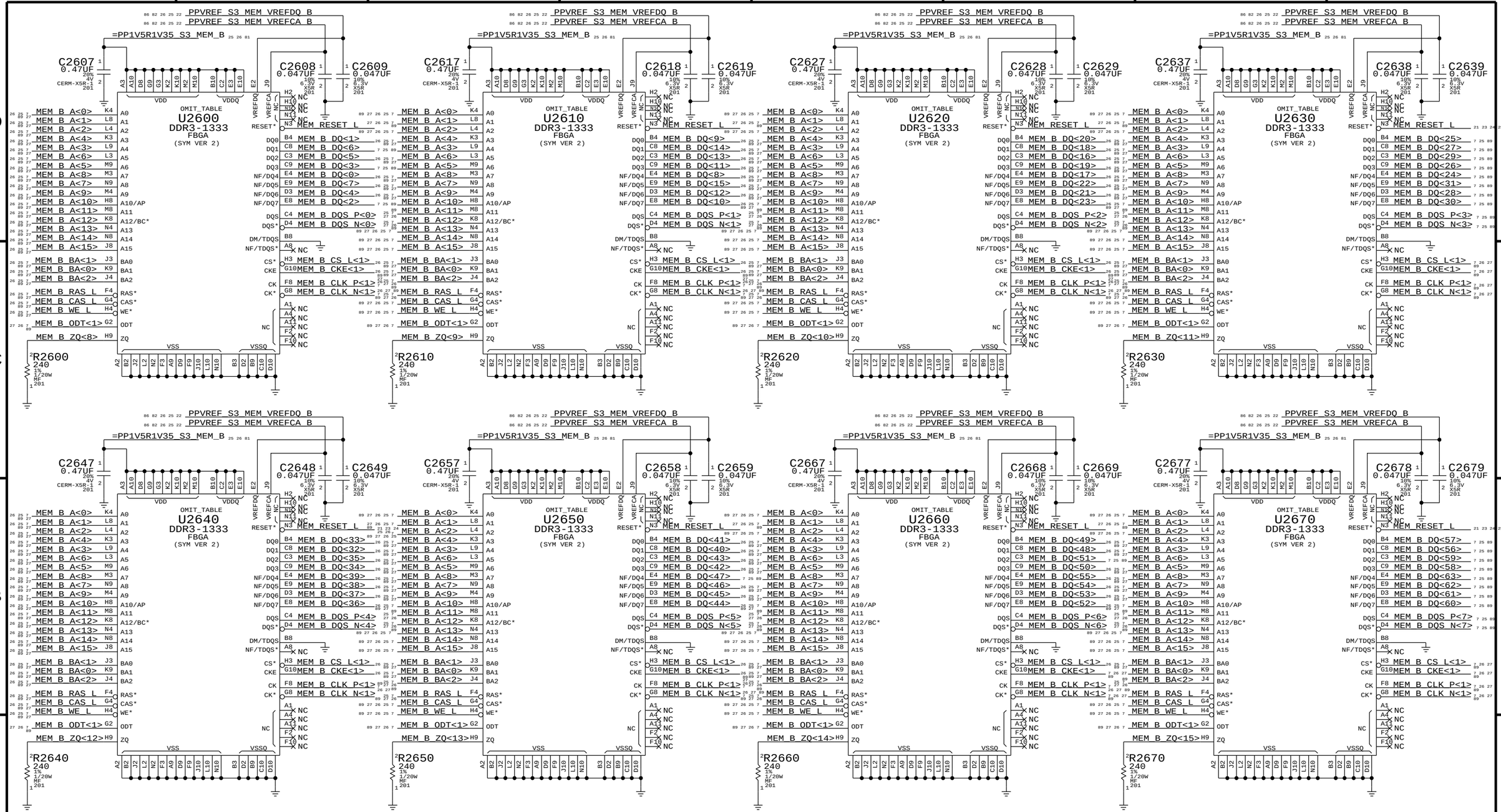
C2500 C2501 C2510 C2511 C2520 C2521 C2530 C2531 2.2UF 20% 10V X5R-CERM 402
C2503 C2504 C2505 C2513 C2514 C2515 C2523 C2524 C2525 C2533 C2534 C2535 0.1UF 10% 6.3V CERM-X5R 0201
C2540 C2541 C2550 C2551 C2560 C2561 C2570 C2571 2.2UF 20% 10V X5R-CERM 402
C2543 C2544 C2545 C2553 C2554 C2555 C2563 C2564 C2565 C2573 C2574 C2575 0.1UF 10% 6.3V CERM-X5R 0201

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
PAGE: 25 OF 119
SHEET: 25 OF 94



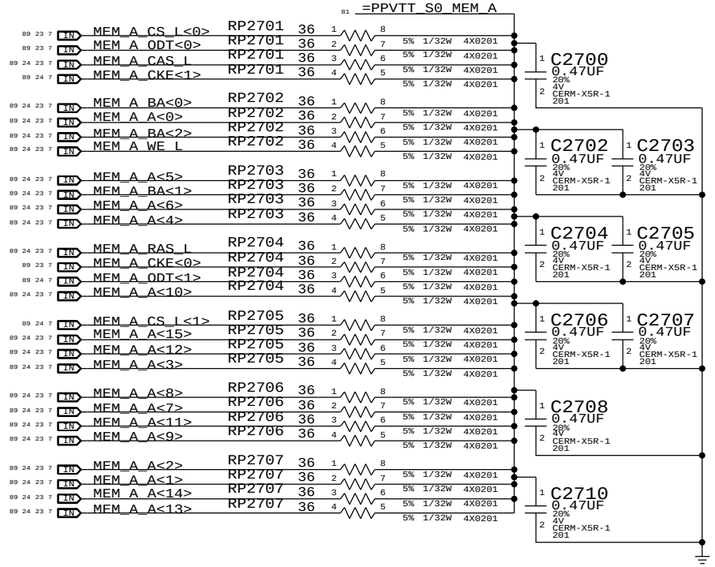
SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

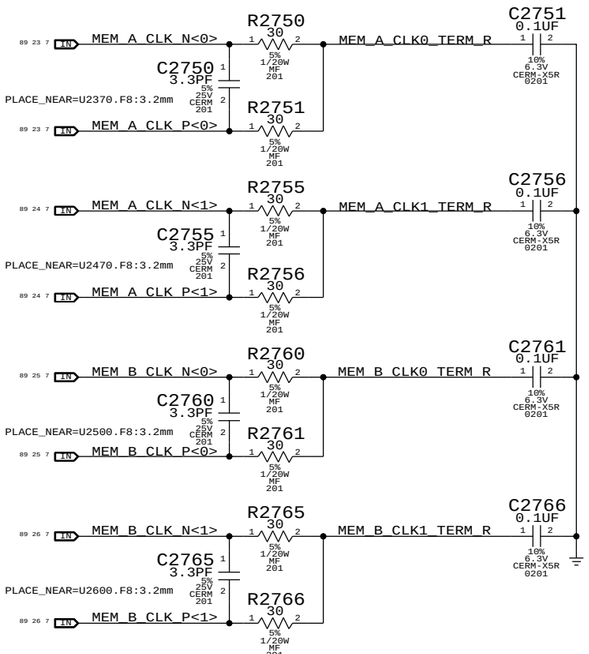
DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 26 OF 119
SHEET 26 OF 94

JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	DDR3 Termination
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 27 OF 119
	SHEET 27 OF 94

CRITICAL
OMIT_TABLE

U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9 PERP_0
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10 PERN_0
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12 PERP_1
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13 PERN_1
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15 PERP_2
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16 PERN_2
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18 PERP_3
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19 PERN_3

PETP_0	AD5	PCIE_TBT_D2R_C_P<0> → C2840 0.1UF → PCIE_TBT_D2R_P<0>
PETN_0	AD7	PCIE_TBT_D2R_C_N<0> → C2841 0.1UF → PCIE_TBT_D2R_N<0>
PETP_1	AD9	PCIE_TBT_D2R_C_P<1> → C2842 0.1UF → PCIE_TBT_D2R_P<1>
PETN_1	AD11	PCIE_TBT_D2R_C_N<1> → C2843 0.1UF → PCIE_TBT_D2R_N<1>
PETP_2	AD13	PCIE_TBT_D2R_C_P<2> → C2844 0.1UF → PCIE_TBT_D2R_P<2>
PETN_2	AD15	PCIE_TBT_D2R_C_N<2> → C2845 0.1UF → PCIE_TBT_D2R_N<2>
PETP_3	AD17	PCIE_TBT_D2R_C_P<3> → C2846 0.1UF → PCIE_TBT_D2R_P<3>
PETN_3	AD19	PCIE_TBT_D2R_C_N<3> → C2847 0.1UF → PCIE_TBT_D2R_N<3>

MISC

	P5	TBT_PCIE_RESET_L → PERST_OD_N
	R4	TBT_PWR_ON_POC_RST_L → PWR_ON_POC_RSTN
	AD23	TP_TBT_MONDC0 → MONDC0
	AC24	TP_TBT_MONDC1 → MONDC1
DEBUG: For monitoring current/voltage		
	W18	TBT_MONOBSP → MONOBSP
	W16	TBT_MONOBSN → MONOBSN
DEBUG: For monitoring clock		
Use AA8 GND ball for THERM_DN	AB7	TP_TBT_THERM_DP → THERMDA
	AA2	TBT_SPI_MOSI → EE_DI
	Y3	TBT_SPI_MISO → EE_DO
	T5	TBT_SPI_CS_L → EE_CS_N
	U8	TBT_SPI_CLK → EE_CLK
	W2	JTAG_TBT_TDI → TDI
	AB1	JTAG_TBT_TMS → TMS
	AA6	JTAG_TBT_TCK → TCK
	U6	JTAG_TBT_TDO → TDO
	R6	TBT_TEST_EN → TEST_EN
	W8	TBT_TEST_PWR_GOOD → TEST_PWR_GOOD

RSENSE	U20	TBT_RSENSE
RBIAS	W20	TBT_RBIAS → R2855 1K 1% 1/20W MF 201
RSVD	AD1, L8	

Used for straps in host mode

PCIE_RST_0_N	W6	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N	AB3	TBT_DFT_STRAP_1
PCIE_RST_2_N	AD3	TBT_ROM_SECURITY_XOR
PCIE_RST_3_N	V1	TBT_DFT_STRAP_3
PCIE_CLKREQ_OD_N	V3	TBT_CLKREQ_L → OUT 11
REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P → IN 11 88
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N → IN 11 88
XTAL_25_IN	AA24 87	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	AB23	TP_TBT_XTAL25OUT → 84
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

PP3V3_TBTLC
NO STUFF R2867 10K 5% 1/20W MF 201
R2861 10K, R2862 10K, R2863 10K (5% 1/20W MF 201)

Divides 3.3V to 1.8V
R2895 806 1% 1/20W MF 201
SYSCLK_CLK25M_TBT → IN 19 87

PP3V3_TBTLC
=PP3V3_S4_TBT
R2881 100K, R2880 100K, R2882 100K (5% 1/20W MF 201)

NO STUFF R2899 10K 5% 1/20W MF 201
R2896 1K 5% 1/20W MF 201

TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD

PP3V3_TBTLC
R2878 100K, R2879 100K (5% 1/20W MF 201)
R2832 100K, R2883 100K (5% 1/20W MF 201)

=PP3V3_S4_TBT
R2884 100K 5% 1/20W MF 201
NO STUFF R2885 10K 5% 1/20W MF 201
NO STUFF R2886 10K 5% 1/20W MF 201

=TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN

R2888 10K, R2887 10K (5% 1/20W MF 201)

PP3V3_TBTLC
R2829 10K 5% 1/20W MF 201
R2825 100 5% 1/20W MF 201

BYPASS=U2890:2mm
R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
C2890 1UF 16V 6-10V CERM 402
R2892 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U2890
4MBIT
W25X40CLXIG
USON

(TBT_SPI_MOSI)	5	DI/IO0
(TBT_SPI_CLK)	6	CLK
(TBT_SPI_CS_L)	1	CS*
TBTROM_WP_L	3	WP*
TBTROM_HOLD_L	7	HOLD*
(TBT_SPI_MISO)	2	DO/IO1
	8	VCC
	4, 9	GND THRM_PAD

OMIT
R2815 NOSTUFF 0201

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N

DISPLAY PORTS

DP_TBTSNK0_ML_P<3>	E14	DPSNK0_3_P
DP_TBTSNK0_ML_N<3>	D13	DPSNK0_3_N
DP_TBTSNK0_ML_P<2>	E16	DPSNK0_2_P
DP_TBTSNK0_ML_N<2>	D15	DPSNK0_2_N
DP_TBTSNK0_ML_P<1>	E18	DPSNK0_1_P
DP_TBTSNK0_ML_N<1>	D17	DPSNK0_1_N
DP_TBTSNK0_ML_P<0>	E20	DPSNK0_0_P
DP_TBTSNK0_ML_N<0>	D19	DPSNK0_0_N
DP_TBTSNK0_AUXCH_P	G4	DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N	G2	DPSNK0_AUX_N
DP_TBTSNK0_HPD	AB5	DPSNK0_HPD
DP_TBTSNK1_ML_P<3>	E6	DPSNK1_3_P
DP_TBTSNK1_ML_N<3>	D5	DPSNK1_3_N
DP_TBTSNK1_ML_P<2>	E8	DPSNK1_2_P
DP_TBTSNK1_ML_N<2>	D7	DPSNK1_2_N
DP_TBTSNK1_ML_P<1>	E10	DPSNK1_1_P
DP_TBTSNK1_ML_N<1>	D9	DPSNK1_1_N
DP_TBTSNK1_ML_P<0>	E12	DPSNK1_0_P
DP_TBTSNK1_ML_N<0>	D11	DPSNK1_0_N
DP_TBTSNK1_AUXCH_P	H3	DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N	H1	DPSNK1_AUX_N
DP_TBTSNK1_HPD	U4	DPSNK1_HPD

R2830 100K 5% 1/20W MF 201
R2831 100K 5% 1/20W MF 201

TBT_A_R2D_C_P<0>	G24	PA_CIO0_TX_P/DPSRC_0_P
TBT_A_R2D_C_N<0>	E24	PA_CIO0_TX_N/DPSRC_0_N
TBT_A_D2R_P<0>	G22	PA_CIO0_RX_P
TBT_A_D2R_N<0>	E22	PA_CIO0_RX_N
TBT_A_CONFIG1_BUF	P1	PA_CONFIG1/CIO_0_LSEO
TBT_A_CONFIG2_RC	K5	PA_CONFIG2/CIO_0_LSOE
TBT_A_R2D_C_P<1>	L24	PA_CIO1_TX_P/DPSRC_2_P
TBT_A_R2D_C_N<1>	J24	PA_CIO1_TX_N/DPSRC_2_N
TBT_A_D2R_P<1>	L22	PA_CIO1_RX_P
TBT_A_D2R_N<1>	J22	PA_CIO1_RX_N
TBT_A_LSTX	N8	PA_LSTX/CIO_1_LSEO
TBT_A_LSRX	J6	PA_LSRX/CIO_1_LSOE
TP_TBTPA_ML_C_P<1>	A16	PA_DPSRC_1_P
TP_TBTPA_ML_C_N<1>	B17	PA_DPSRC_1_N
TP_TBTPA_ML_C_P<3>	A18	PA_DPSRC_3_P
TP_TBTPA_ML_C_N<3>	B19	PA_DPSRC_3_N
TP_TBTPA_AUXCH_C_P	L4	PA_AUX_P
TP_TBTPA_AUXCH_C_N	L2	PA_AUX_N
TP_TBTPA_HPD	M3	PA_DPSRC_HPD
TBT_A_HV_EN	R8	GPIO_0/PA_HV_EN/BYP0
TBT_A_CIO_SEL	N2	GPIO_10/PA_CIO_SEL/BYP1
TBT_A_DP_PWRDN	P3	GPIO_12/PA_DP_PWRDN/BYP2

DPSRC_3_P	A14	TP_DP_TBTSRC_ML_CP<3>
DPSRC_3_N	B15	TP_DP_TBTSRC_ML_CN<3>
DPSRC_2_P	A12	TP_DP_TBTSRC_ML_CP<2>
DPSRC_2_N	B13	TP_DP_TBTSRC_ML_CN<2>
DPSRC_1_P	A10	TP_DP_TBTSRC_ML_CP<1>
DPSRC_1_N	B11	TP_DP_TBTSRC_ML_CN<1>
DPSRC_0_P	A8	TP_DP_TBTSRC_ML_CP<0>
DPSRC_0_N	B9	TP_DP_TBTSRC_ML_CN<0>
DPSRC_AUX_P	J4	TP_DP_TBTSRC_AUXCH_CP
DPSRC_AUX_N	J2	TP_DP_TBTSRC_AUXCH_CN
DPSRC_HPD_OD	AC2	DP_TBTSRC_HPD

GPIO_2/TMU_CLK_IN/AC_PRESENT	U2	TBT_GPIO2
GPIO_3/FORCE_PWR	L6	TBT_PWR_EN → IN 20
GPIO_4/WAKE_OD_N	H5	=TBT_WAKE_L → OUT 42
GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD	Y7	TBT_CIO_PLUG_EVENT_L → OUT 20
GPIO_6_OD/CIO_SDA_OD	Y1	HDMITBTMUX_SEL_TBT → IN 28 82
GPIO_7_OD/CIO_SCL_OD	T7	TBT_GPIO7
GPIO_8/EN_CIO_PWR_OD*	V7	TBT_EN_CIO_PWR_L → OUT 28 29
GPIO_9/SX_CTRL_OD*	M7	=TBT_BATLOW_L → IN 28 30
GPIO_14	T1	TBTDP_AUXIO_EN → OUT 28 31 32
GPIO_15	T3	TBT_DDC_XBAR_EN_L → OUT 28 79

PB_CIO2_TX_P/DPSRC_0_P	R24	TBT_B_R2D_C_P<0> → OUT 32 90
PB_CIO2_TX_N/DPSRC_0_N	N24	TBT_B_R2D_C_N<0> → OUT 32 90
PB_CIO2_RX_P	R22	TBT_B_D2R_P<0> → IN 32 90
PB_CIO2_RX_N	N22	TBT_B_D2R_N<0> → IN 32 90
PB_CONFIG1/CIO_2_LSEO	D3	TBT_B_CONFIG1_BUF → OUT 32 79
PB_CONFIG2/CIO_2_LSOE	M1	TBT_B_CONFIG2_RC → IN 32
PB_CIO3_TX_P/DPSRC_2_P	W24	TBT_B_R2D_C_P<1> → OUT 32 90
PB_CIO3_TX_N/DPSRC_2_N	U24	TBT_B_R2D_C_N<1> → OUT 32 90
PB_CIO3_RX_P	W22	TBT_B_D2R_P<1> → IN 32 90
PB_CIO3_RX_N	U22	TBT_B_D2R_N<1> → IN 32 90
PB_LSTX/CIO_3_LSEO	M5	TBT_B_LSTX → OUT 32
PB_LSRX/CIO_3_LSOE	P7	TBT_B_LSRX → IN 32
PB_DPSRC_1_P	A20	DP_TBTPB_ML_C_P<1> → OUT 32 90
PB_DPSRC_1_N	B21	DP_TBTPB_ML_C_N<1> → OUT 32 90
PB_DPSRC_3_P	A22	DP_TBTPB_ML_C_P<3> → OUT 32 90
PB_DPSRC_3_N	B23	DP_TBTPB_ML_C_N<3> → OUT 32 90
PB_AUX_P	K3	DP_TBTPB_AUXCH_C_P → BI 32 90
PB_AUX_N	K1	DP_TBTPB_AUXCH_C_N → BI 32 90
PB_DPSRC_HPD	N6	DP_TBTPB_HPD → IN 32
GPIO_1/PB_HV_EN/BYP0	F1	TBT_B_HV_EN → OUT 28 30 32
GPIO_11/PB_CIO_SEL/BYP1	R2	TBT_B_CIO_SEL → OUT 32
GPIO_13/PB_DP_PWRDN/BYP2	F3	TBT_B_DP_PWRDN → OUT 28 32

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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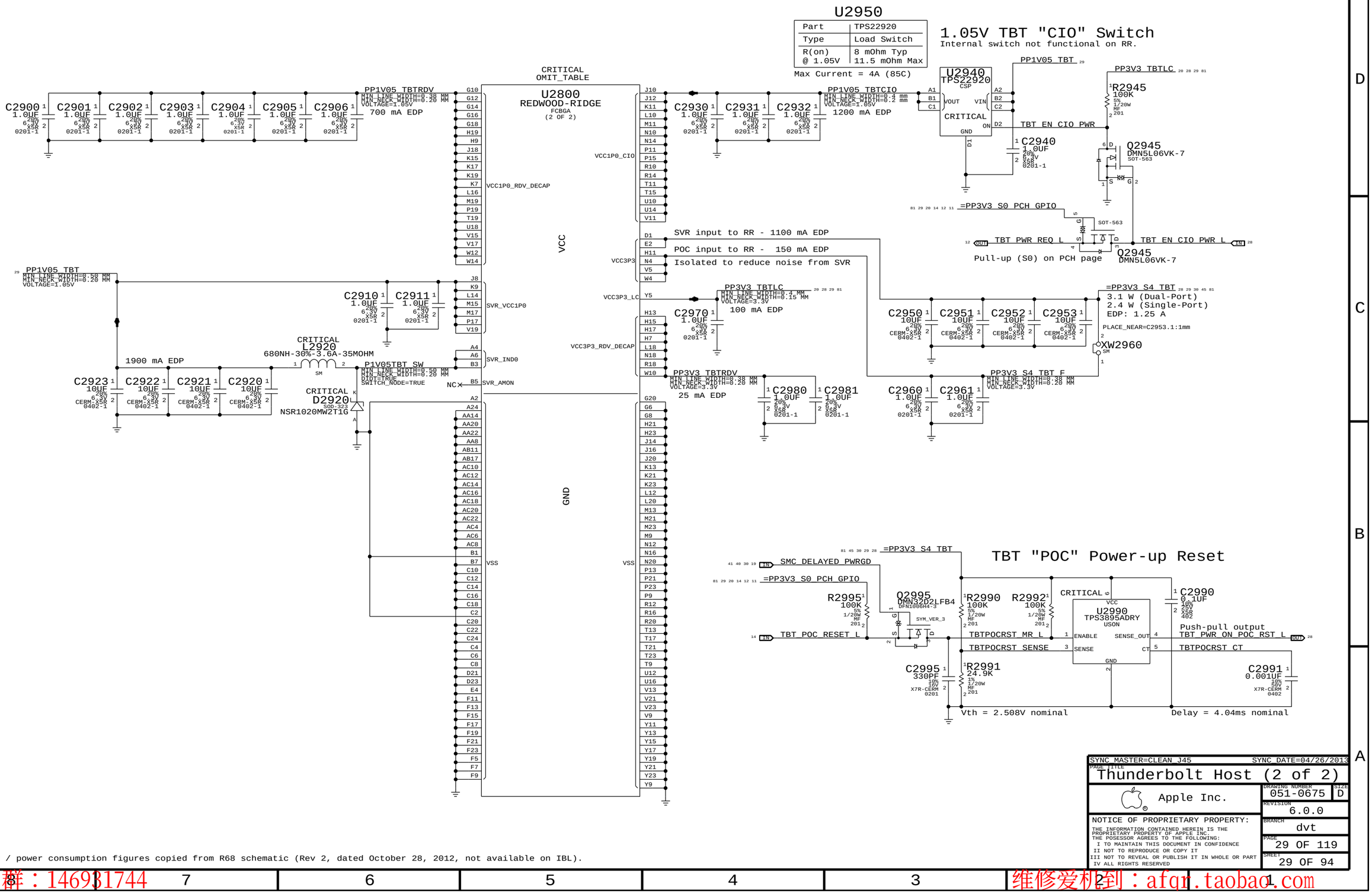

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

=PPVIN_SW_TBTBST
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/16W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

Q3005 DMN5L06VK-7 SOT-563
Q3005 DMN5L06VK-7 SOT-563
TBT_A_HV_EN
TBT_B_HV_EN

CRITICAL
Q3080 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here,
add property on another page.

R3091 200K 1% 1/16W MF-LF 402 <R1>
C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095 3.3UH-6.5A PIMB063T-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090 LT3957 QFN
VIN
SW
SNS1
SNS2
EN/UVLO
INTVCC
VC
RT
SS
SYNC
FBX
NC
SGND
GND

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
TBTBST_FBX

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V C0G-CERM 0402
R3093 49.9K 1% 1/16W MF-LF 402
C3092 2.2UF 20% 10V X5R-CERM 402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3094 26.7K 1% 1/16W MF-LF 402
C3094 0.33UF 10% 6.3V CERM-X5R 402
R3092 73.2K 1% 1/16W MF-LF 402 <R2>

GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to
GND inside package,
no XW necessary.

R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5
TBTBST_SNS1
TBTBST_SNS2
XW3095 SM
PLACE_NEAR=C3095.1:2 mm
TBTBST_VSNS
C3088 10PF 5% 50V C0G-CERM 0402
R3095 137K 1% 1/16W MF-LF 402 <Ra>
C3089 100PF 5% 50V CERM 402
NO STUFF
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>

=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L
C3096 10UF 10% 25V X5R 1206-2
NO STUFF
C3097 10UF 10% 25V X5R 805
C3099 0.001UF 10% 50V X7R-CERM 0402

Vout = 1.6V * (1 + Ra / Rb)

Q3088 DMN5L06VK-7 SOT-563
Max Vgs: 10V
TBTBST_SHDN_DIV
R3088 330K 5% 1/10W MF-LF 402
R3087 330K 5% 1/10W MF-LF 402
Q3088 DMN5L06VK-7 SOT-563
SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
=PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
=TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Thunderbolt Mobile Support

Apple Inc.

DRAWING NUMBER	051-0675
SIZE	D
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BRANCH	dvt
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL
C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 603
C3281 0.1UF 10% 16V X5R-CERM 0201
=PPHV_S4SW_TBTAPWRSW
15.75V Max
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 25V X5R 402
CRITICAL
U3210
CD3211A0RGPR
QFN
V3P3
VHV
ENHVU
EN
HV_EN
S0
V3P3OUT
OUT
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V 402
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3210 22.6K 1% 1/20W MF 201
TBTHV:P15V
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201
<RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
TBTHV:P15V
R3213 22.6K 1% 1/20W MF 201
TBTHV:P15V
R3214 22.6K 1% 1/20W MF 201
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
<RHVS3>
<RHVS0> ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector A

CRITICAL
L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X5R-CERM 0402
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V
R3201 12 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)
C3274 0.47UF 20% 4V 201 CERM-X5R-1
C3275 0.47UF 20% 4V 201 CERM-X5R-1
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
GND_VOID=TRUE
R3294 1K 5% 1/20W MF 201
R3295 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE

C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201

TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1

CRITICAL
SHIELD PINS
J3200
MDP-J44
F-RT-TH
PORT B
SHIELD PINS
514-0876

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
SIGNAL_MODEL=TBT_MUX
CRITICAL
U3220
CBTL05024
HVQFN24-COMBO
VDD
GND THMPAD

GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V 201 CERM-X5R-1
C3276 0.47UF 20% 4V 201 CERM-X5R-1
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<1>
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBT_A_TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
TBT_A_HPD
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
GND_VOID=TRUE
C3205 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
GND_VOID=TRUE
C3206 0.01UF 10% 25V X5R-CERM 0201
DP Dir TBT Dir
TBT: TX_0
TBT: TX_1
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>

GND_VOID=TRUE (Both C's)
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
470K R's for ESD protection on AC-coupled signals.

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE	Thunderbolt Connector A
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

81 =PP3V3_S4_TBTBPWRSW
CRITICAL
C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM 603
C3381 0.1UF 10% 16V X5R-CERM 0201
81 =PPHV_S4SW_TBTBPWRSW
15.75V Max
C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 25V X5R 402
CRITICAL
U3310
CD3211A0RGPR
QFN
V3P3
VHV
ENHVU
EN
HV_EN
S0
V3P3OUT
OUT
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V 402
PP3V3_S4_TBTBPWR 32
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
65 IN =TBTBPWRSW_EN
30 28 IN TBT_B_HV_EN
65 31 IN =TBT_S0_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3310 22.6K 1% 1/20W MF 201
TBTHV:P15V
R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201
<RV3P3>
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V
R3313 22.6K 1% 1/20W MF 201
TBTHV:P15V
R3314 22.6K 1% 1/20W MF 201
Single-fault protection
requires two R's per HV
ISET_Sx with CD3210.
Single R on ISET_V3P3 OK.
<RHVS3>
<RHVS0> ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

CRITICAL
L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3300 0.01UF 10% 50V X7R-CERM 0402
C3301 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V
R3301 12 5% 1/20W MF 201
TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
C3302 0.01UF 10% 16V X5R-CERM 0201

GND_VOID=TRUE (Both C's)
C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1
90 28 OUT TBT_B_D2R_P<0>
90 28 OUT TBT_B_D2R_N<0>
90 TBT_B_D2R_C_P<0>
90 TBT_B_D2R_C_N<0>
R3394 1K 5% 1/20W MF 201
R3395 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
90 28 IN DP_TBTPB_ML_C_P<3>
90 28 IN DP_TBTPB_ML_C_N<3>
90 DP_TBTPB_ML_P<3>
90 DP_TBTPB_ML_N<3>
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201
90 32 TBT_B_D2R1_AUXDDC_P
90 32 TBT_B_D2R1_AUXDDC_N
32 TBT_B_HPD
32 TBT_B_CONFIG1_RC
28 OUT TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201

CRITICAL
J3200 MDP-J44 F-RT-TH
SHIELD PINS
PORT A
SHIELD PINS
514-0876
A2 HPD
A4 CONFIG1
A6 CONFIG2
A8 GND2
A10 ML_LANE3P
A12 ML_LANE3N
A14 GND4
A16 AUX_CHP
A18 AUX_CHN
A20 DP_PWR
GND0 A1
ML_LANE0P A3
ML_LANE0N A5
GND1 A7
ML_LANE1P A9
ML_LANE1N A11
GND3 A13
ML_LANE2P A15
ML_LANE2N A17
RETURN A19

32 PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
SIGNAL_MODEL=TBT_MUX
CRITICAL
U3320 CBTL05024 HVQFN24-COMBO
VDD
TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX (IPU)
LSRX (IPD)
HPDOUT
GND_THMPAD
TB_ENA
AUXIO_EN
DP_PD
(IPU) AUXIO-
(IPD) AUXIO+
CA_DET
DPML0+
DPML0-
HPD
90 TBT_B_D2R_C_N<1>
90 TBT_B_D2R_C_P<1>
90 DP_TBTPB_AUXCH_C_N
90 DP_TBTPB_AUXCH_P
89 BI DP_TBTPB_DDC_DATA
89 IN DP_TBTPB_DDC_CLK
79 28 OUT TBT_B_CONFIG1_BUF
90 DP_TBTPB_ML_P<1>
90 DP_TBTPB_ML_N<1>
28 IN TBT_B_LSTX
28 OUT TBT_B_LSRX
28 OUT DP_TBTPB_HPD
15 TBT_B_CIO_SEL 28 IN
24 TBTDP_AUXIO_EN 28 IN 31
6 TBT_B_DP_PWRDN 28 IN
23 TBT_B_D2R1_AUXDDC_N 32 90
22 TBT_B_D2R1_AUXDDC_P 32 90
TBT: RX_1
18 TBT_B_CONFIG1_RC 32
19 DP_B_LSX_ML_P<1> 32 90
20 DP_B_LSX_ML_N<1> 32 90
TBT: LSX_A_R2P/P2R (P/N)
17 TBT_B_HPD 32

TBTBCONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
GND_VOID=TRUE
C3305 0.01UF 10% 25V X5R-CERM 0201
DP Dir TBT Dir
90 TBT_B_R2D_P<0>
90 TBT_B_R2D_N<0>
TBT: TX_0
TBTBCONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
GND_VOID=TRUE
C3306 0.01UF 10% 25V X5R-CERM 0201
90 TBT_B_R2D_P<1>
90 TBT_B_R2D_N<1>
TBT: TX_1
470K R's for ESD protection
on AC-coupled signals.

GND_VOID=TRUE (Both C's)
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<0> IN 28 90
TBT_B_R2D_C_N<0> IN 28 90
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<1> IN 28 90
TBT_B_R2D_C_N<1> IN 28 90
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013
PAGE TITLE: Thunderbolt Connector B
Apple Inc.
DRAWING NUMBER: 051-0675
SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

AIRPORT

BLUETOOTH

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

Supervisor & CLKREQ # Isolation

Delay = 130 ms +/- 20%

SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	X29C CONNECTOR
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
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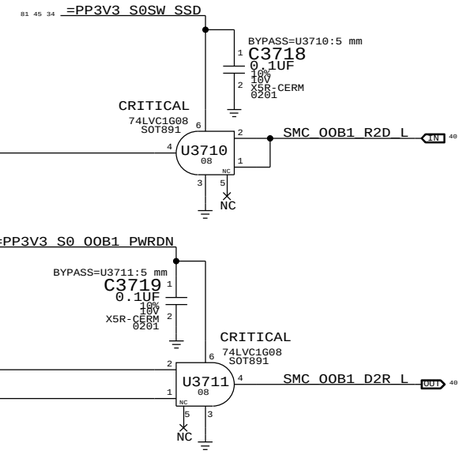
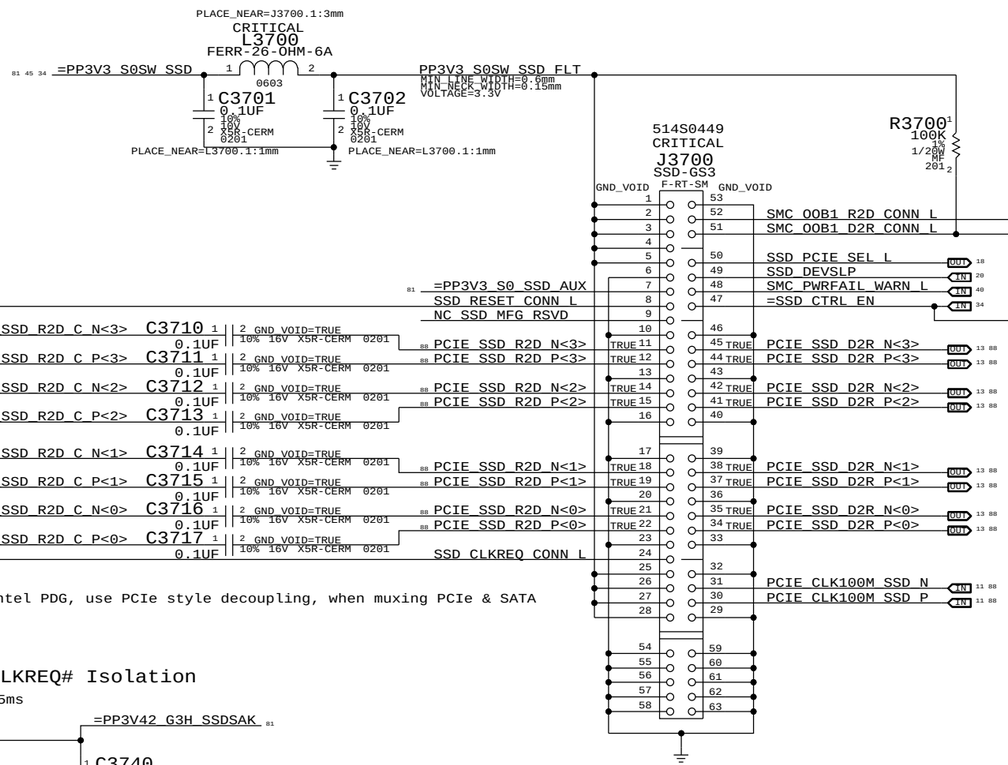
OOB Isolation



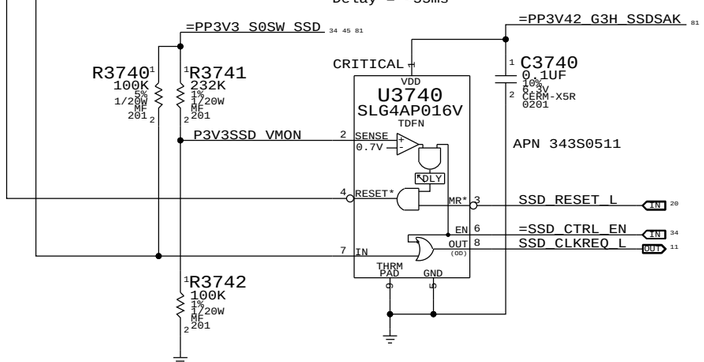


Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

Gumstick3 Connector

Supervisor & CLKREQ# Isolation

Delay = ~55ms



34 =SSD_CTRL_EN — SSD_PWR_FET_EN 64

MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	SSD Connector
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
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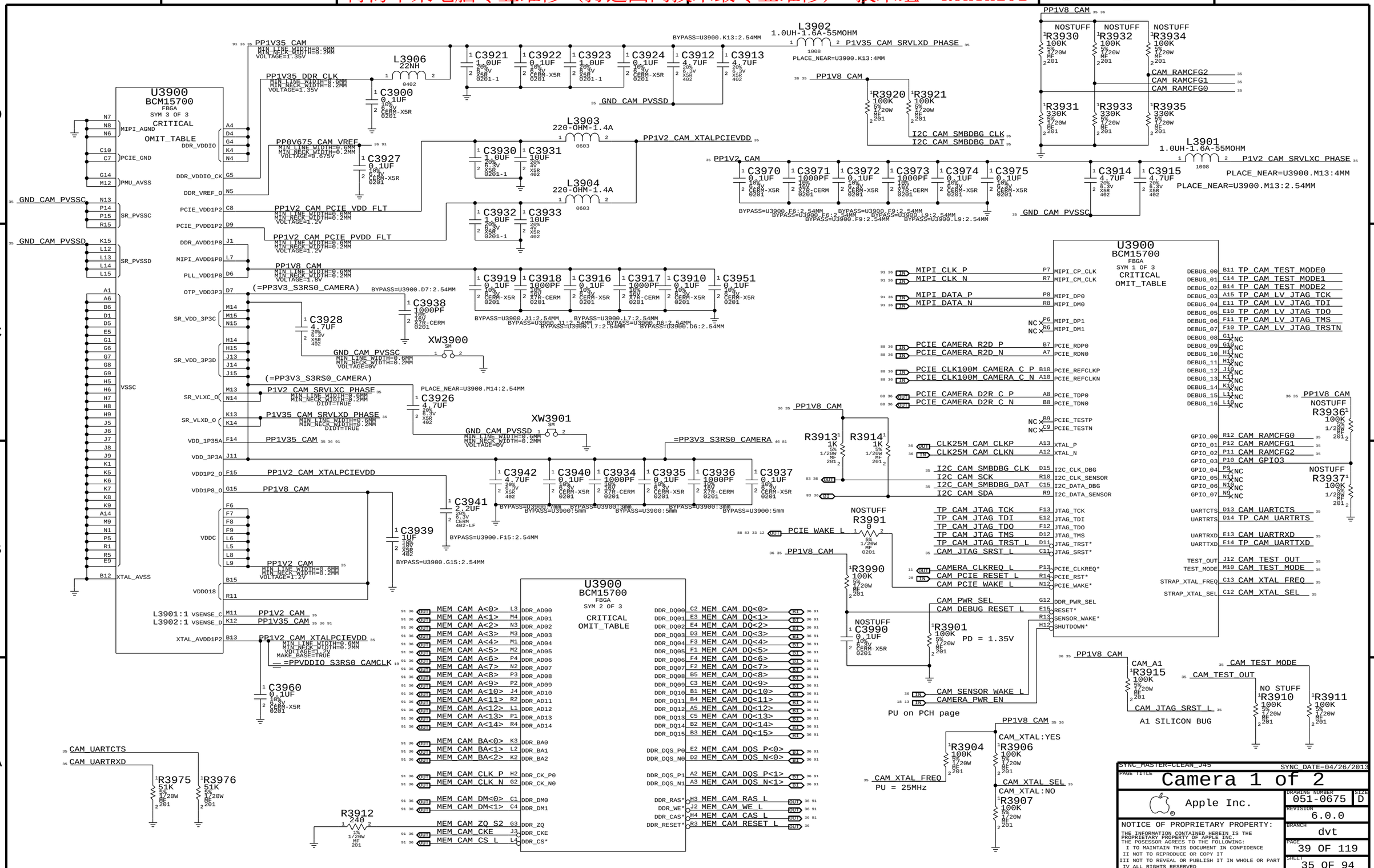
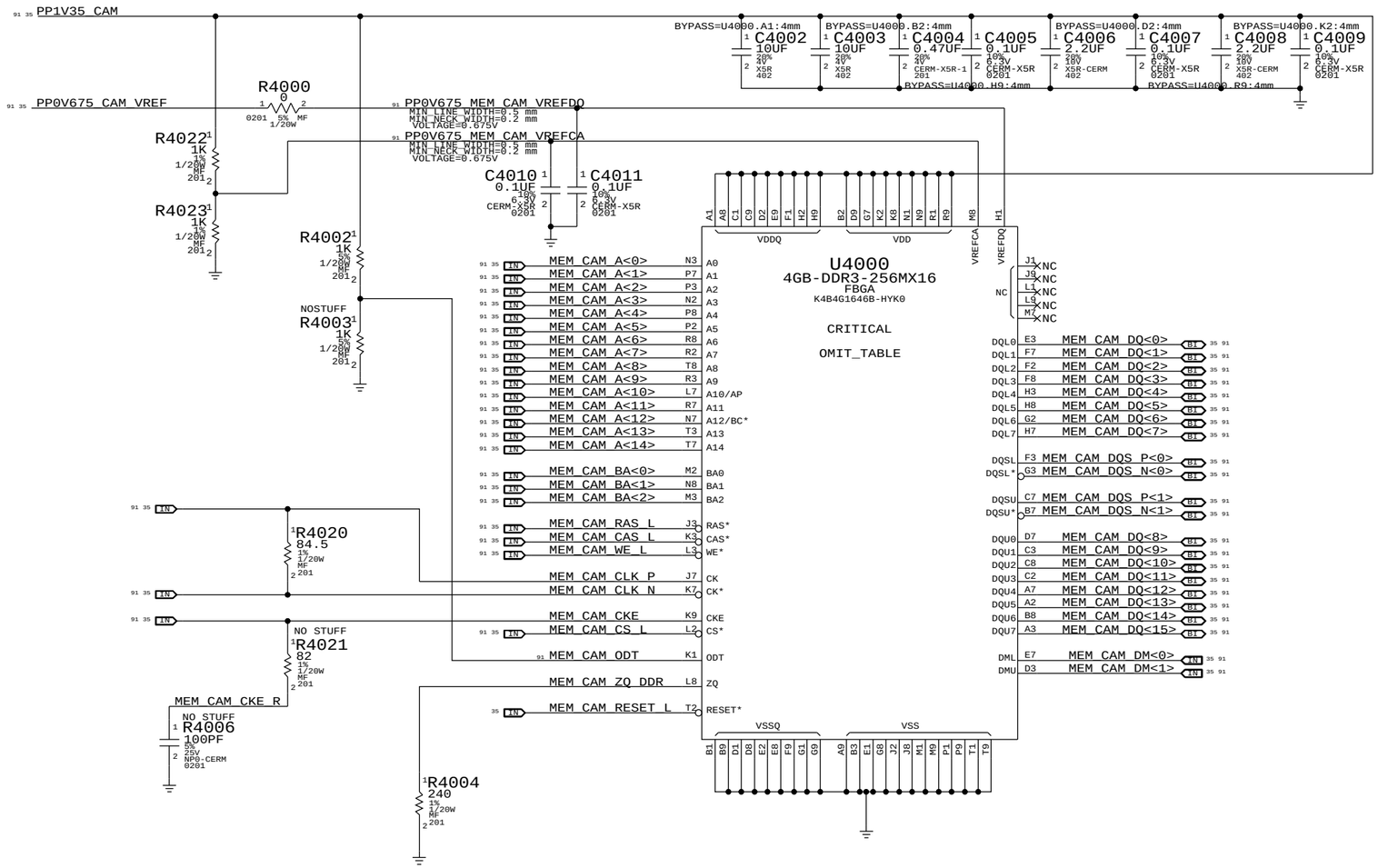




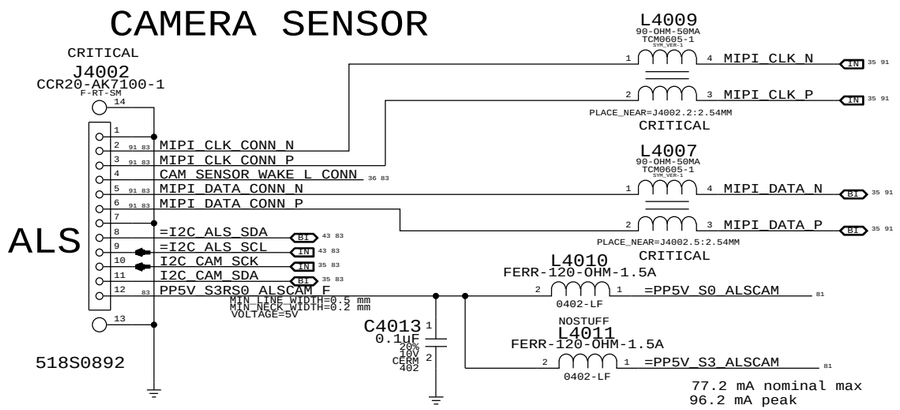
remove DRAM SPD Straps

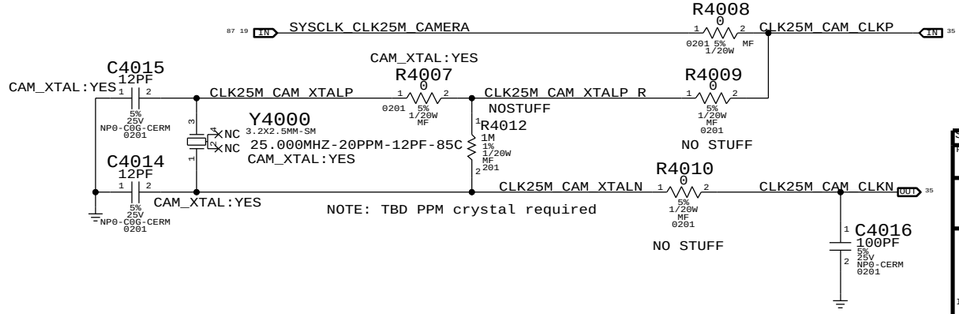
DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR





SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Camera 2 of 2

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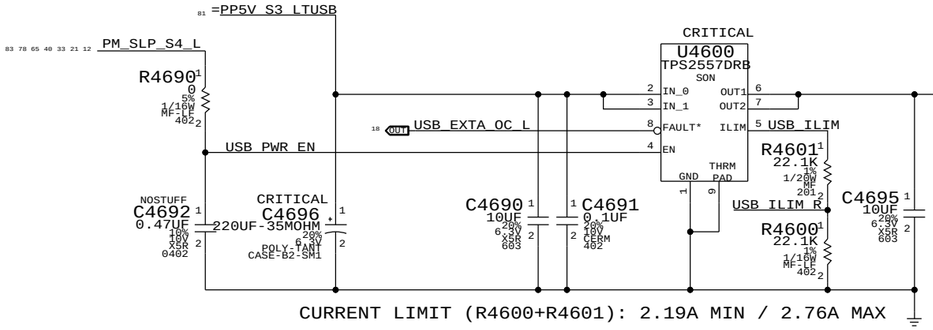
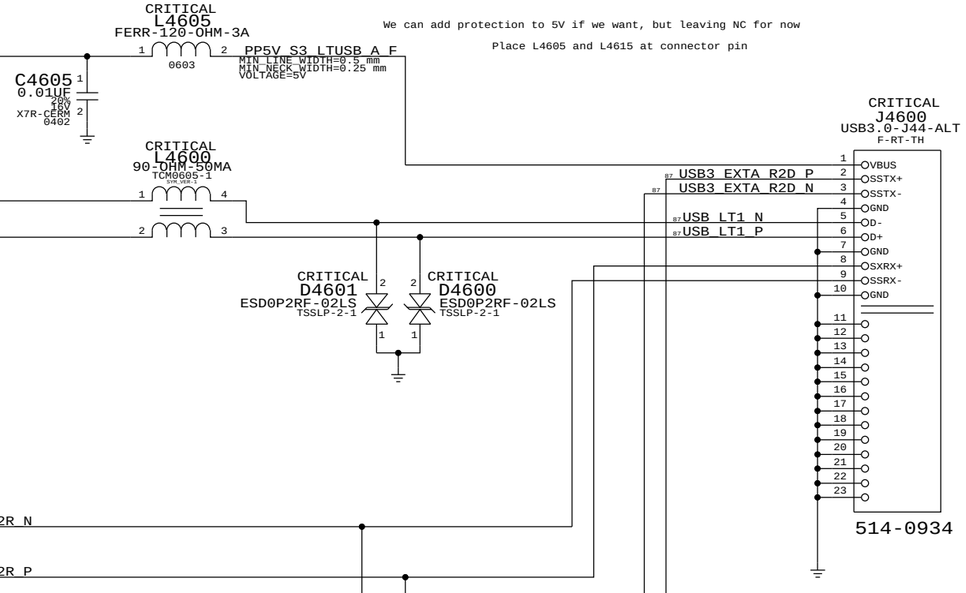
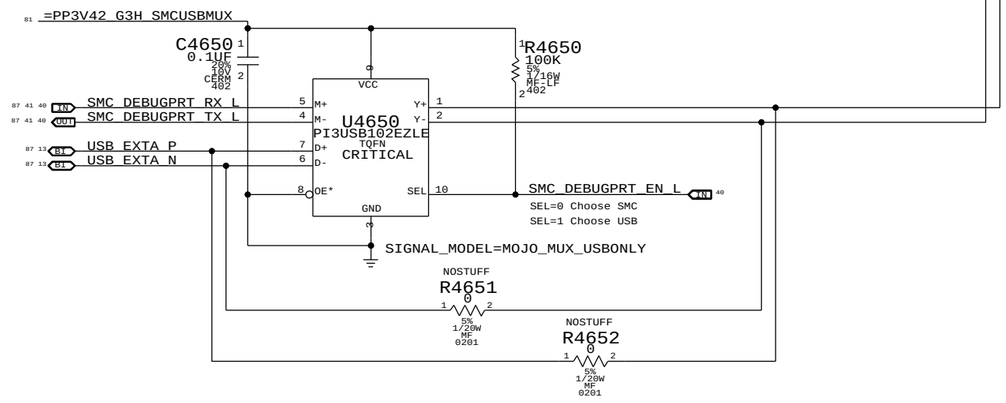
USB Port Power Switch

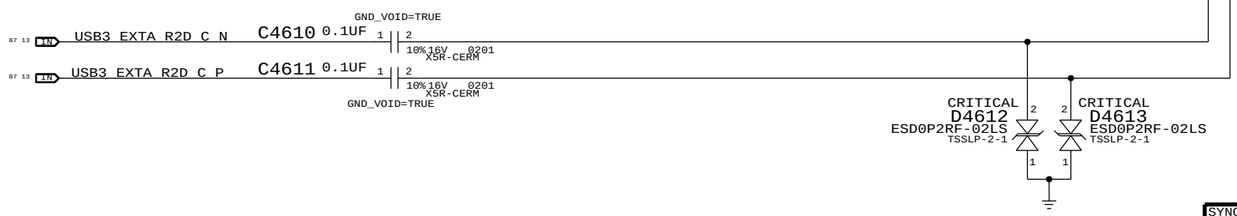


Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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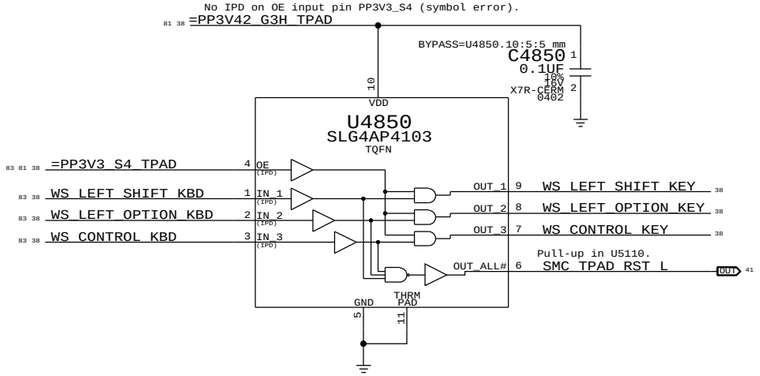
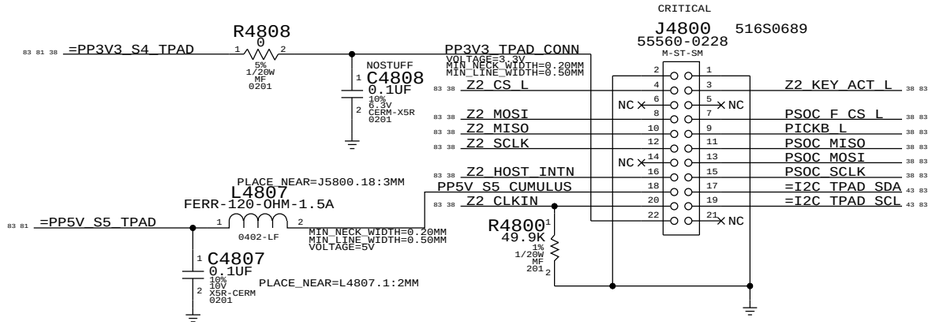
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

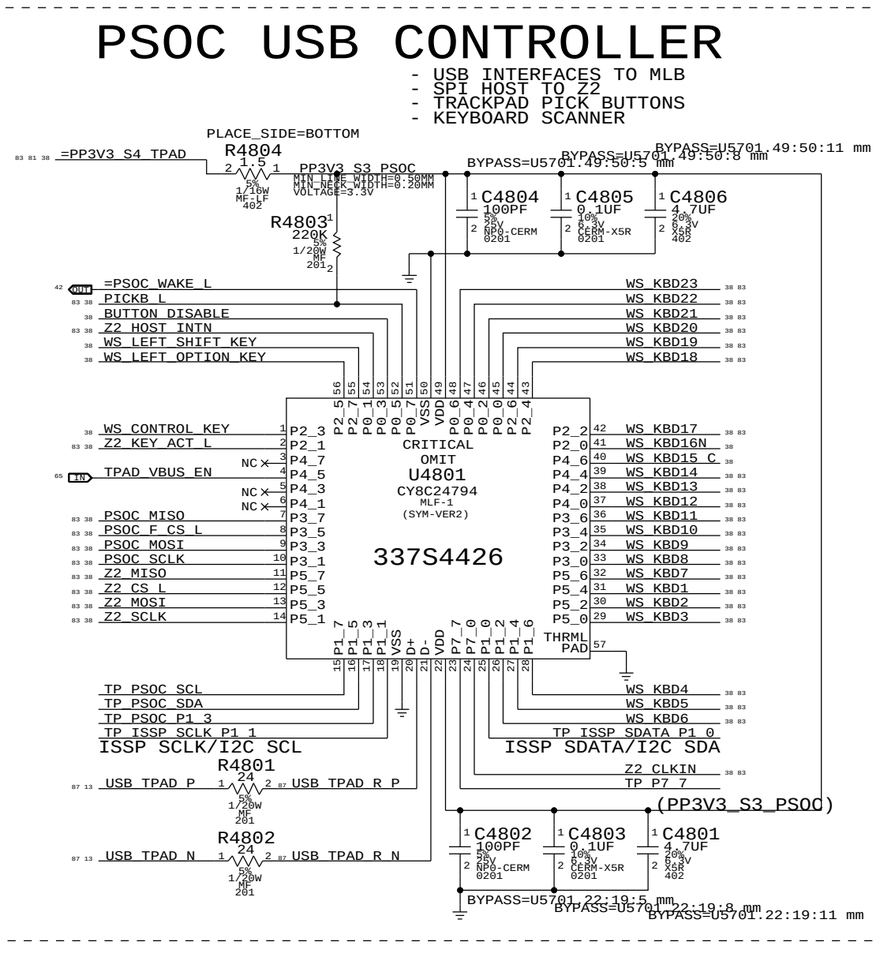


IPD Flex Connector

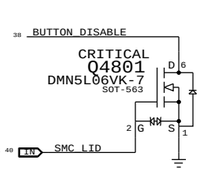


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

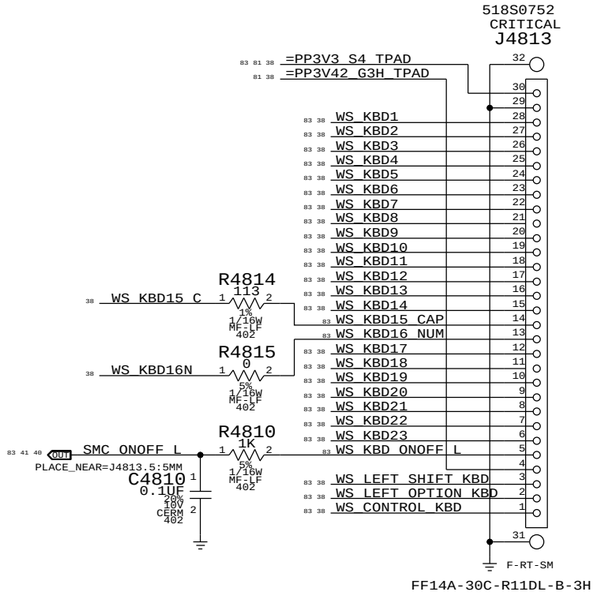


TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

Keyboard Connector



FF14A-30C-R11DL-B-3H

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

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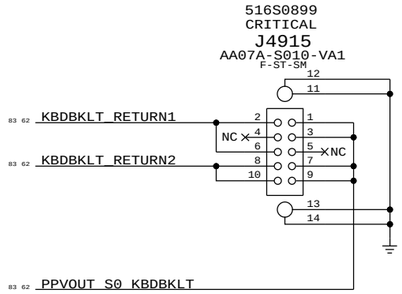
Keyboard Backlight Connector



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

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BRANCH dvt
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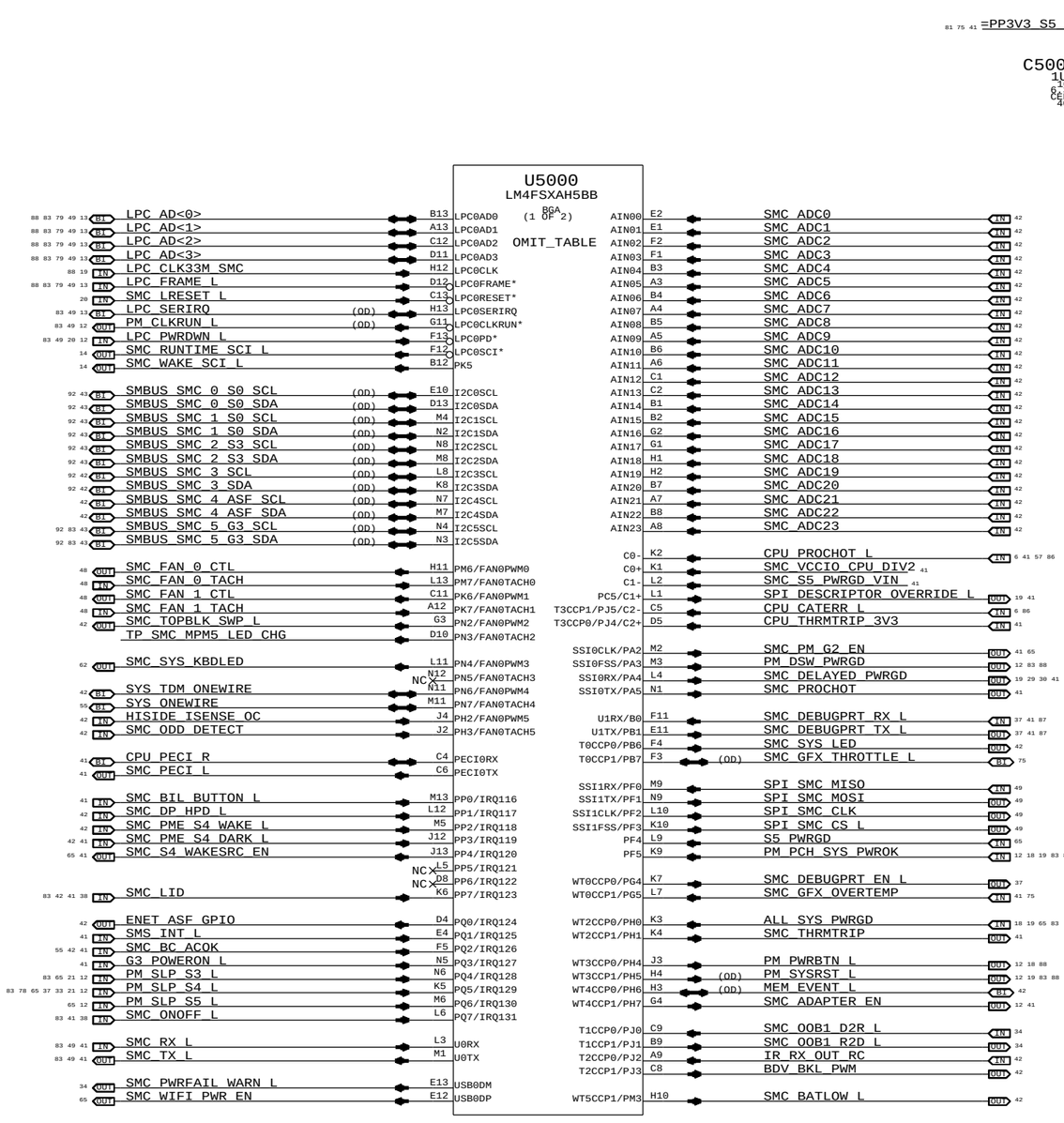
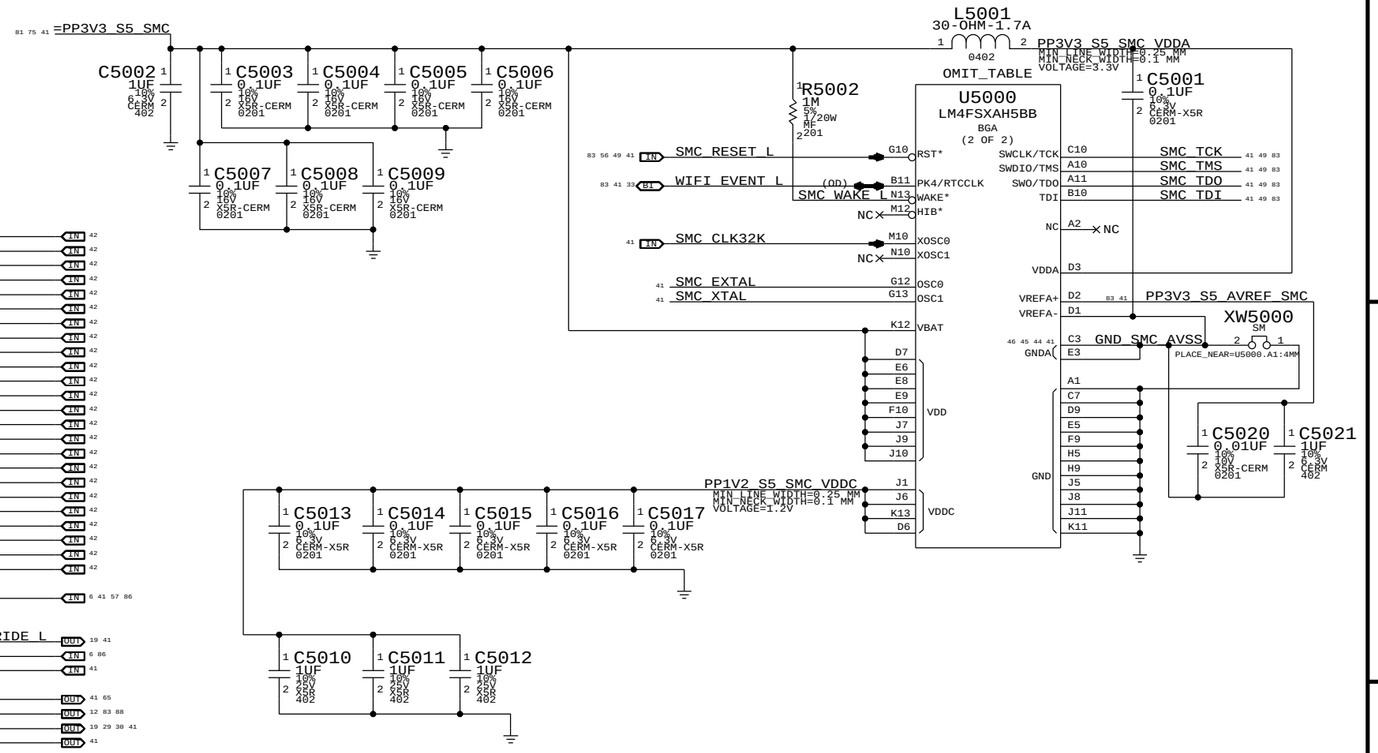
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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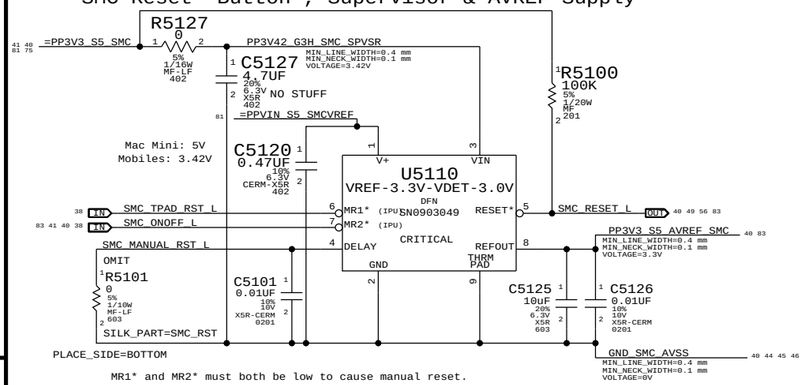
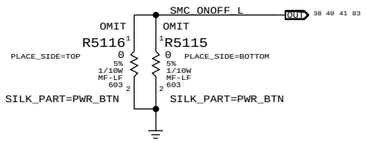
SMC Reset "Button", Supervisor & AVREF Supply



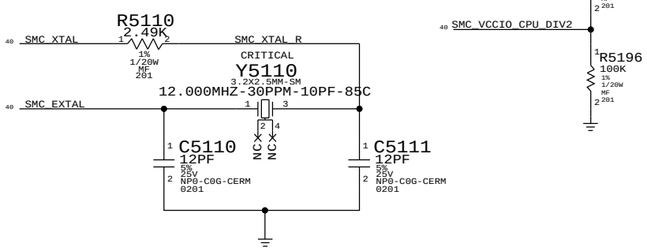
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

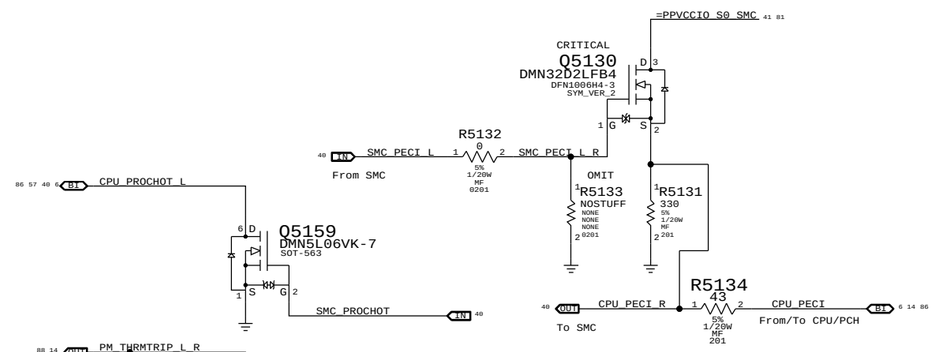


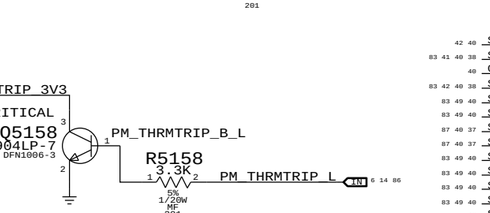
SMC Crystal Circuit

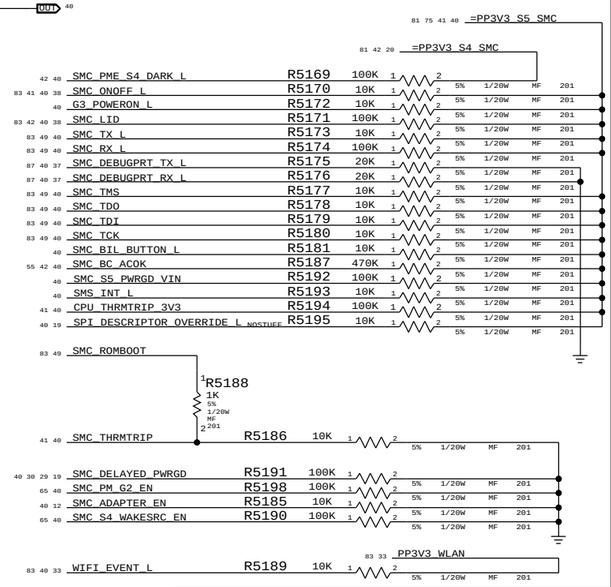


SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

SMC12 PECI SUPPORT







SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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56 =CHGR_ACOK — SMC_BC_ACOK 40 41 55
MAKE_BASE=TRUE

40 HISIDE_ISENSE_OC — NC_HISIDE_ISENSE_OC
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_ADC0 — SMC_CPUPKG_VSENSE 45
MAKE_BASE=TRUE

40 SMC_ADC1 — SMC_CPUPKG_ISENSE 45
MAKE_BASE=TRUE

40 SMC_ADC2 — SMC_GPU_HI_ISENSE 44
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_ADC3 — SMC_DCIN_VSENSE 44
MAKE_BASE=TRUE

40 SMC_ADC4 — SMC_DCIN_ISENSE 44
MAKE_BASE=TRUE

40 SMC_ADC5 — SMC_PBUS_VSENSE 44
MAKE_BASE=TRUE

40 SMC_ADC6 — SMC_SSD_ISENSE 45
MAKE_BASE=TRUE

40 SMC_ADC7 — SMC_CHGR_BMON_ISENSE 44
MAKE_BASE=TRUE

40 SMC_ADC8 — SMC_CPU_HI_ISENSE 44
MAKE_BASE=TRUE

40 SMC_ADC9 — SMC_OTHER3V3_HI_ISENSE 44
MAKE_BASE=TRUE

40 SMC_ADC10 — SMC_P1V35MEM_ISENSE 45
MAKE_BASE=TRUE

40 SMC_ADC11 — SMC_CPUDDR_ISENSE 46
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_ADC12 — SMC_LCDPANEL_ISENSE 46
MAKE_BASE=TRUE

40 SMC_ADC13 — SMC_OTHER5V_HI_ISENSE 44
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_ADC14 — SMC_GPUCORE_VSENSE 45
MAKE_BASE=TRUE

40 SMC_ADC15 — SMC_GPUCORE_ISENSE 46
MAKE_BASE=TRUE

40 SMC_ADC16 — NC_SMC_ADC16
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_ADC17 — SMC_LCDBKLT_ISENSE 46
MAKE_BASE=TRUE

40 SMC_ADC18 — SMC_GPU_FB_VSENSE 45
MAKE_BASE=TRUE

40 SMC_ADC19 — SMC_GPU_FB_ISENSE 45
MAKE_BASE=TRUE

40 SMC_ADC20 — SMC_S2_ISENSE 46
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_ADC21 — SMC_GPU1V05_ISENSE 46
MAKE_BASE=TRUE

40 SMC_ADC22 — SMC_X29_ISENSE 46
MAKE_BASE=TRUE

40 SMC_ADC23 — SMC_TBT_ISENSE 45
MAKE_BASE=TRUE

40 SMBUS_SMC_4_ASF_SCL — NC_SMBUS_SMC_4_ASF_SCL
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMBUS_SMC_4_ASF_SDA — NC_SMBUS_SMC_4_ASF_SDA
MAKE_BASE=TRUE NO_TEST=TRUE

92 40 SMBUS_SMC_3_SCL — NC_SMBUS_SMC_3_SCL
MAKE_BASE=TRUE NO_TEST=TRUE

92 40 SMBUS_SMC_3_SDA — NC_SMBUS_SMC_3_SDA
MAKE_BASE=TRUE NO_TEST=TRUE

40 BDV_BKL_PWM — NC_BDV_BKL_PWM
MAKE_BASE=TRUE NO_TEST=TRUE

41 40 SMC_PME_S4_DARK_L — SMC_PME_SDCONN_L 20
MAKE_BASE=TRUE =TBT_WAKE_L 28

40 ENET_ASF_GPIO — NC_ENET_ASF_GPIO
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_SYS_LED — NC_SMC_SYS_LED
MAKE_BASE=TRUE NO_TEST=TRUE

40 MEM_EVENT_L — NC_MEM_EVENT_L
MAKE_BASE=TRUE NO_TEST=TRUE

40 SMC_ODD_DETECT — NC_SMC_ODD_DETECT
MAKE_BASE=TRUE NO_TEST=TRUE

40 IR_RX_OUT_RC — NC_IR_RX_OUT_RC
MAKE_BASE=TRUE NO_TEST=TRUE

40 SYS_TDM_ONEWIRE — NC_SYS_TDM_ONEWIRE
MAKE_BASE=TRUE NO_TEST=TRUE

Spare S4 IRQ

=PP3V3_S4_SMC 20 41 42 81
R5259 100K 5% 1/20W MF 201
40 OUT SMC_DP_HPD_L

Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99
SM
NC 1 2 NC 8 7 NC
=PP3V42_S3_HALL 3 6 83 SMC_LID_R
NC 4 5 NC
R5250 0 5% 1/20W MF 0201
SMC_LID 38 40 41 83
C5250 0.001UF 10% 50V X7R-CERM 0402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

=PP3V3_S4_SMC 20 41 42 81
R5282 100K 5% 1/20W MF 201
38 IN =PSOC_WAKE_L
33 IN =BT_WAKE_L
SMC_PME_S4_WAKE_L OUT 40
MAKE_BASE=TRUE

40 IN SMC_TOPBLK_SWP_L — R5283 1K 5% 1/20W MF 201 — PCH_STRP_TOPBLK_SWP_L OUT 12

40 IN SMC_BATLOW_L — PM_BATLOW_L OUT 12 30
MAKE_BASE=TRUE

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PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

Lynx Point
U1100
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA
MAKE_BASE=TRUE

R5300 1K 5% 1/10W MF-LF 402
R5301 1K 5% 1/16W MF-LF 402

VRef DACs
U2200
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

Margin Control
U2201
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

XDP Connectors
J1800 & J1850
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

R5390 0 5% 1/16W MF-LF 402
R5391 0 5% 1/16W MF-LF 402

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
I2C_HDMIRDRV_SCL
I2C_HDMIRDRV_SDA

NO STUFF
R5392 0 5% 1/16W MF-LF 402
R5393 0 5% 1/16W MF-LF 402

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
I2C_DPMUX_A_SCL
I2C_DPMUX_A_SDA
I2C_HDMIRDRV_SCL
I2C_HDMIRDRV_SDA

NO STUFF R5393 0 5% 1/16W MF-LF 402

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

Lynx Point
U1100
(MASTER)
SML_PCH_0_CLK
SML_PCH_0_DATA
MAKE_BASE=TRUE

R5310 8.2K 5% 1/10W MF-LF 402
R5311 8.2K 5% 1/16W MF-LF 402

PCH "SMLink 1" Connections

=PP3V3_S0_SMBUS_PCH

Lynx Point
U1100
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA
MAKE_BASE=TRUE

NO STUFF R5320 8.2K 5% 1/20W MF 201
NO STUFF R5321 8.2K 5% 1/20W MF 201
R5323 0 5% 1/20W MF 0201
R5322 0 5% 1/20W MF 0201

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U5000
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5350 2.0K 5% 1/10W MF-LF 402
R5351 2.0K 5% 1/16W MF-LF 402

L&R Fin Stack Temp
EMC1414-A: U5850
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA

J4002
ALS
(Write: 0x72 Read: 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA

GPU Temp (Int)
GK107: U8400
(Write: 0x9E Read: 0x9F)
GPU_SMB_CLK_R
GPU_SMB_DAT_R

Need to check with SMC team

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

SMC
U5000
(MASTER)
SMB_2_S3_CLK
SMB_2_S3_DATA
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
MAKE_BASE=TRUE

R5370 1K 5% 1/20W MF 201
R5371 1K 5% 1/20W MF 201

Trackpad
J4801
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

SMC
U5000
(MASTER)
SMB_1_S0_CLK
SMB_1_S0_DATA
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
MAKE_BASE=TRUE

R5360 1K 5% 1/20W MF 201
R5361 1K 5% 1/20W MF 201

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5870
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

X29 TEMP
TMP105: U5823
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

SMC
U5000
(MASTER)
SMB_5_CLK
SMB_5_DATA
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
MAKE_BASE=TRUE

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

Battery Charger
ISL6258 - U7100
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J7050
(Write: 0x16 Read: 0x17)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

=PP3V3_S0_DPMUXI2C

DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_A_SCL
=I2C_DPMUX_A_SDA

R5336 4.7K 5% 1/10W MF-LF 402
R5337 4.7K 5% 1/16W MF-LF 402

I2C_DPMUX_A_SCL
I2C_DPMUX_A_SDA
MAKE_BASE=TRUE

=PP3V3_S0_DPMUXI2C

LED BACKLIGHT SMBUS CONNECTION

DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_UC_SCL
=I2C_DPMUX_UC_SDA

R5334 4.7K 5% 1/20W MF 201
R5335 4.7K 5% 1/20W MF 201

I2C_DPMUX_UC_SCL
I2C_DPMUX_UC_SDA
MAKE_BASE=TRUE

LED BACKLIGHT
U7100
(WRITE: 0x58 READ: 0x59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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SMBus Connections

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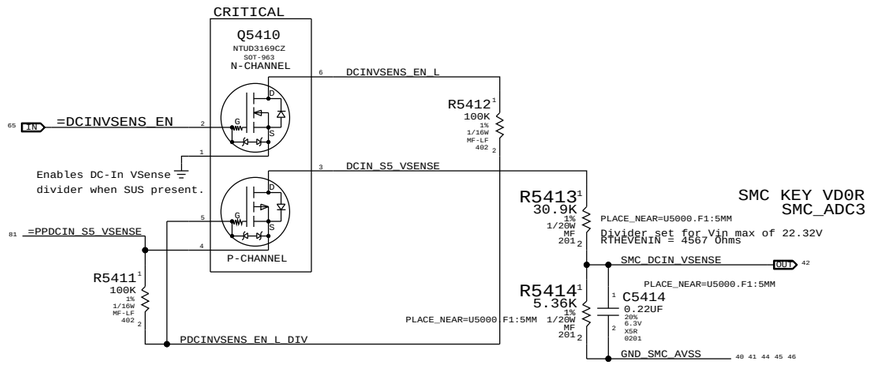
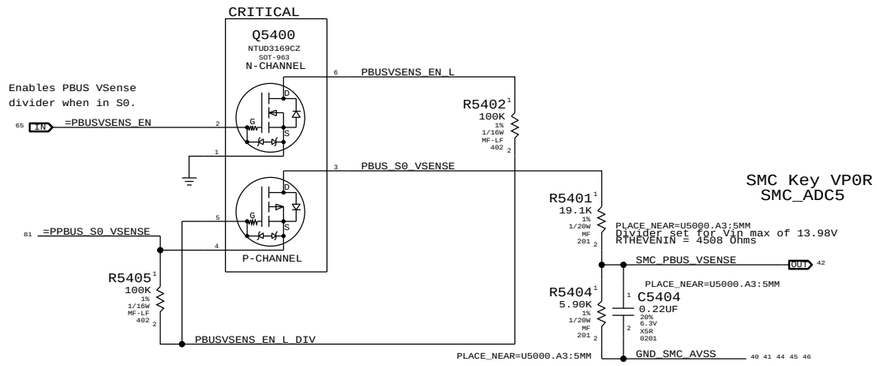
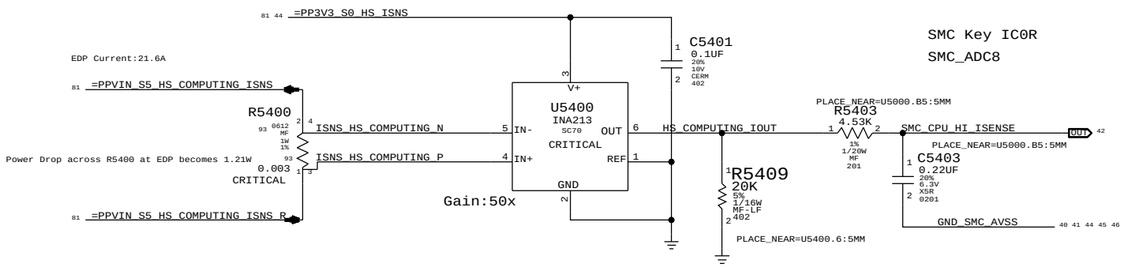
DC-In Voltage Sense Enable & Filter



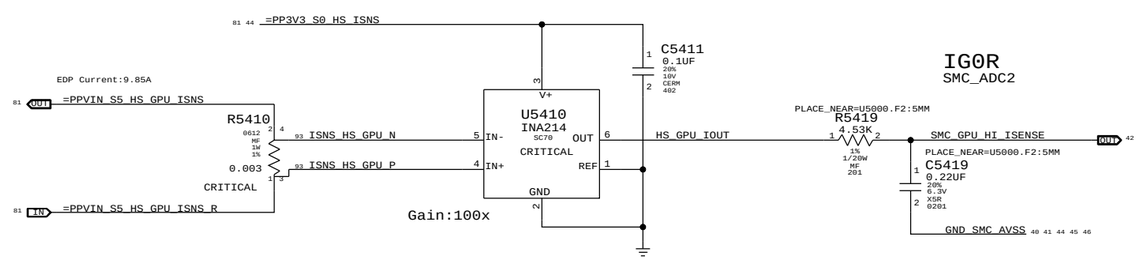
PBUS Voltage Sense Enable & Filter



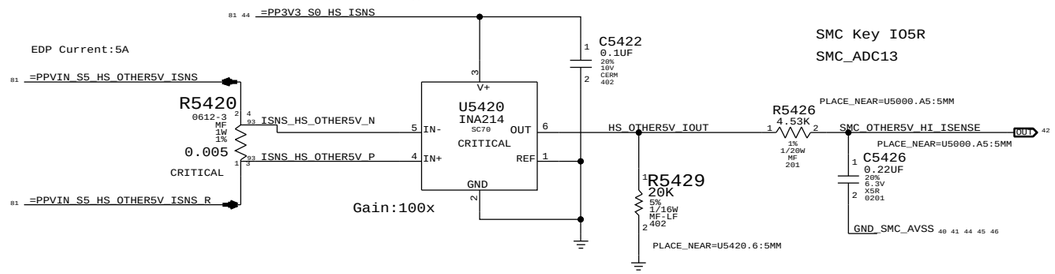
COMPUTING High Side Current Sense / Filter



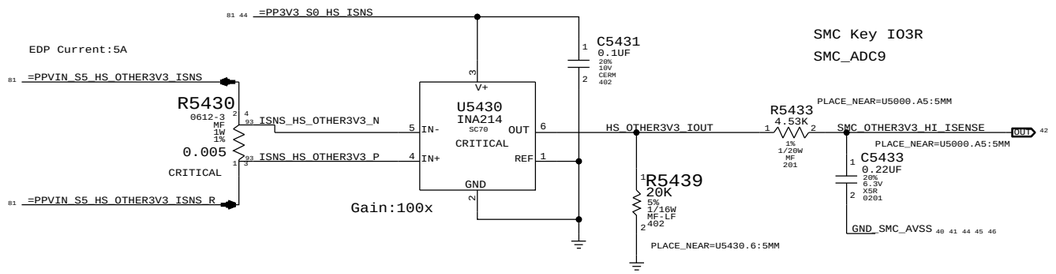
GRAPHICS High Side Current Sense / Filter



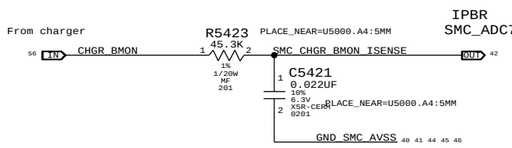
OTHERS (5V) High Side Current Sense / Filter



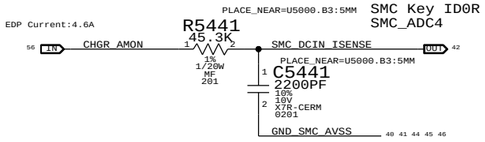
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	High Side Voltage and Current Sensing
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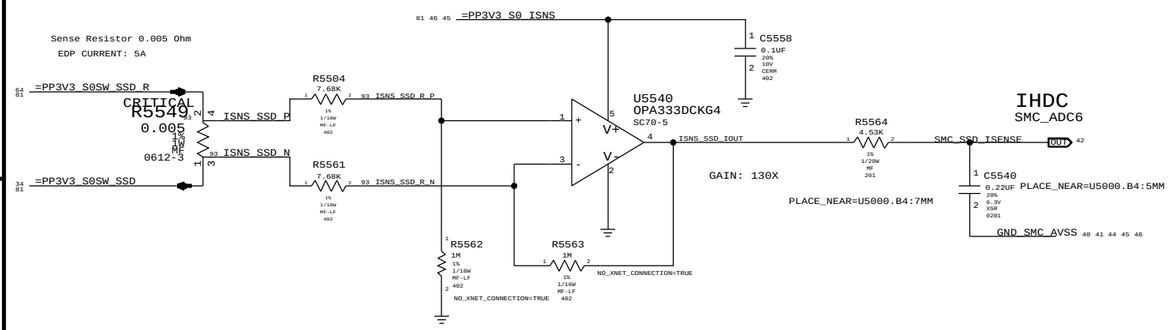
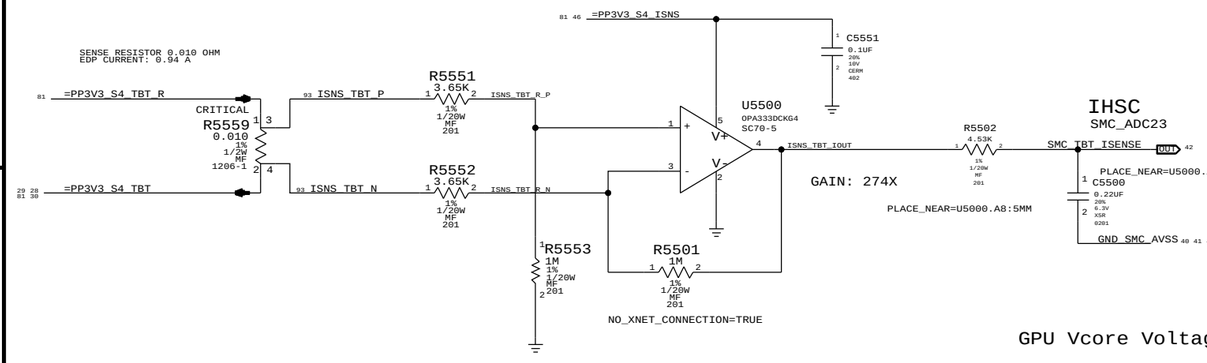
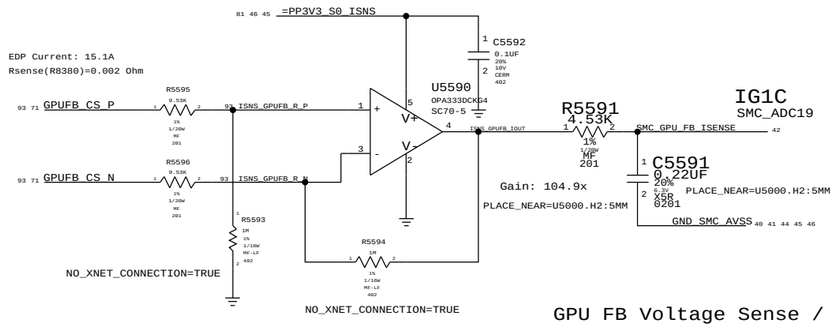
SSD CURRENT SENSE



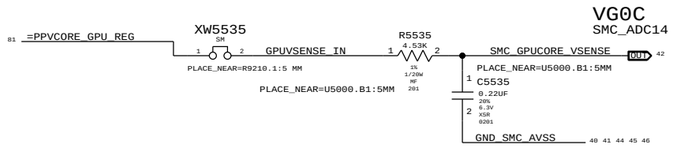
TBT Router CURRENT SENSE



GPU FB (1.35V/1.5V) CURRENT SENSE



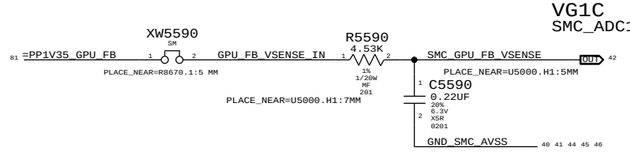
GPU Vcore Voltage Sense / Filter



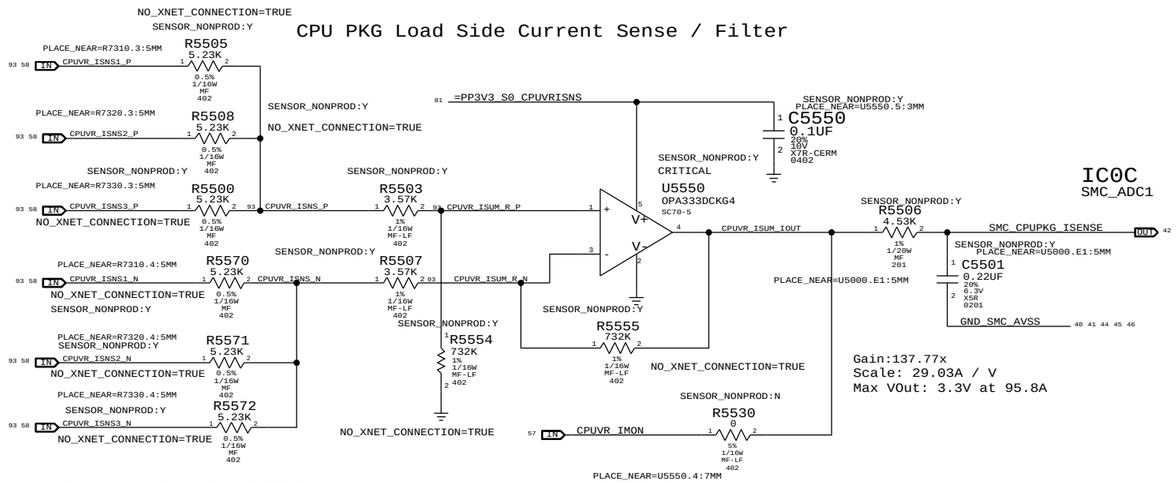
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MTL FILM,0,5,1/20W,0201,SMD,LF	R5506		SENSOR_NONPROD:N

removed LCD BKLT Voltage Sensing

GPU FB Voltage Sense / Filter

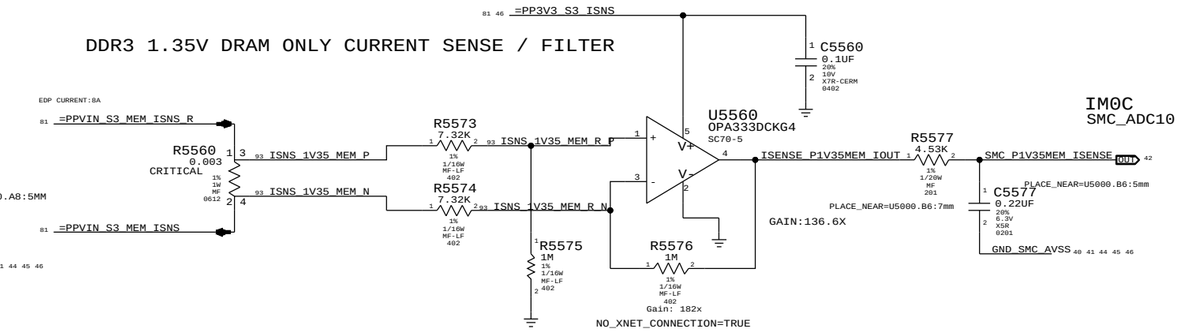


CPU PKG Load Side Current Sense / Filter

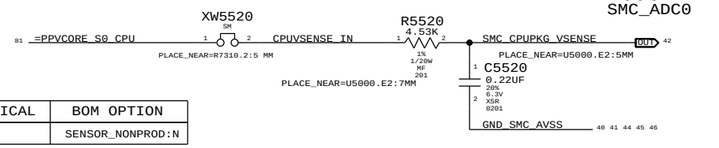


Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER



CPU Vcore Voltage Sense / Filter



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE: Load Side Voltage and Current Sensing	
Apple Inc.	DRAWING NUMBER: 051-0675 SIZE: D
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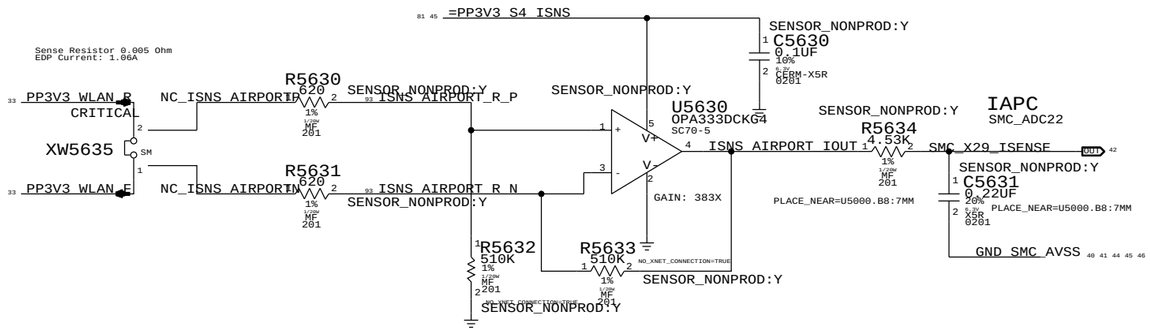
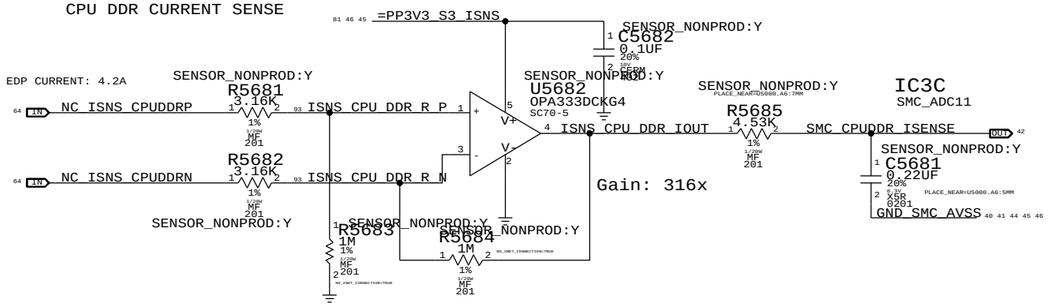
X29 AIRPORT CURRENT SENSE



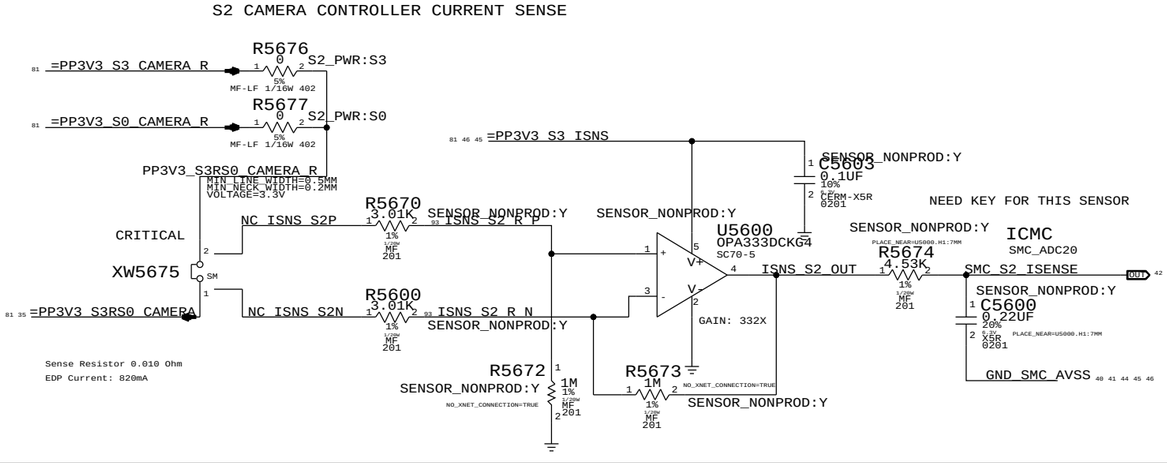
C5601,C5631,C5600,C5681,C5671,C5618,C5642

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF			SENSOR_NONPROD:N

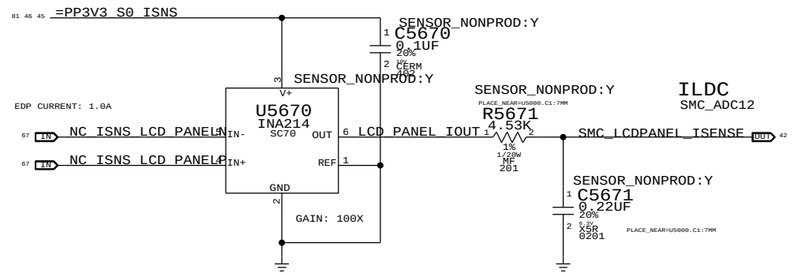
CPU DDR CURRENT SENSE



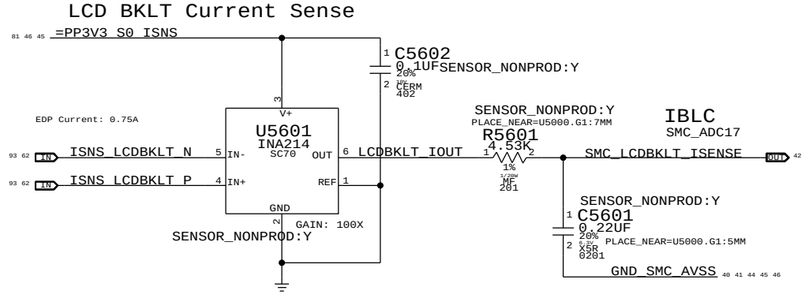
S2 CAMERA CONTROLLER CURRENT SENSE



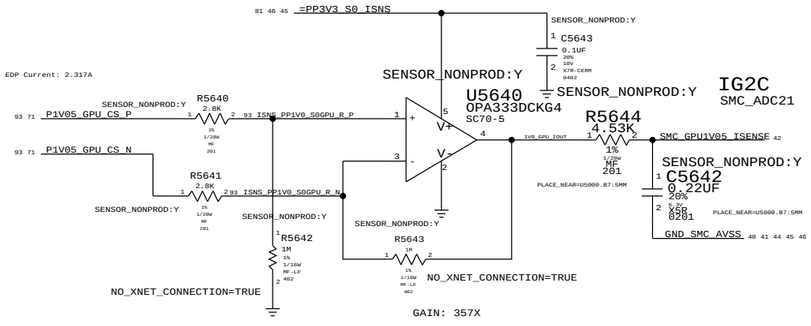
LCD PANEL CURRENT SENSE



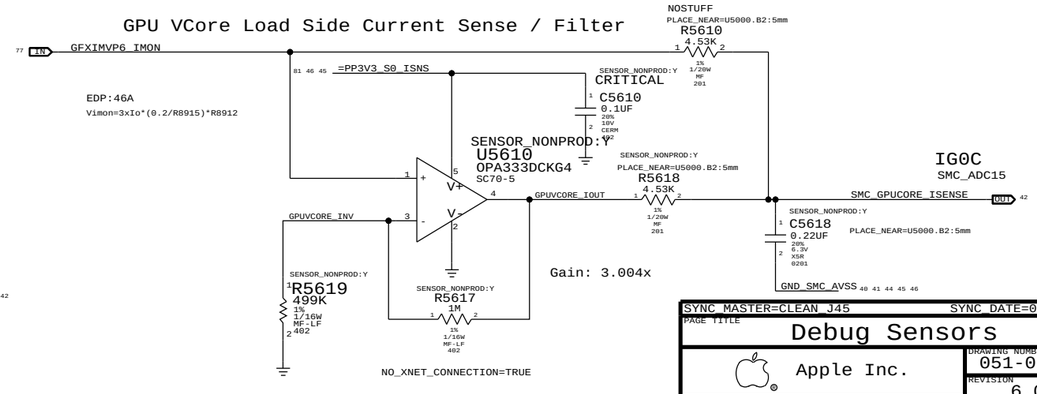
LCD BKLT Current Sense



GPU 1.05V CURRENT SENSE



GPU VCore Load Side Current Sense / Filter



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
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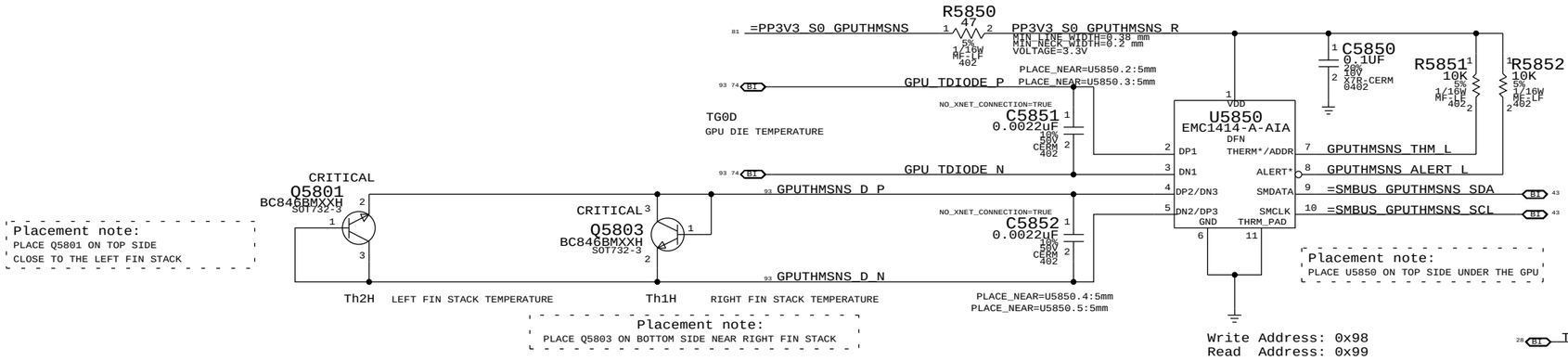
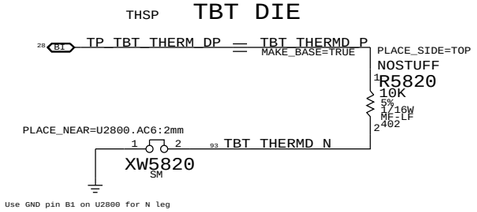
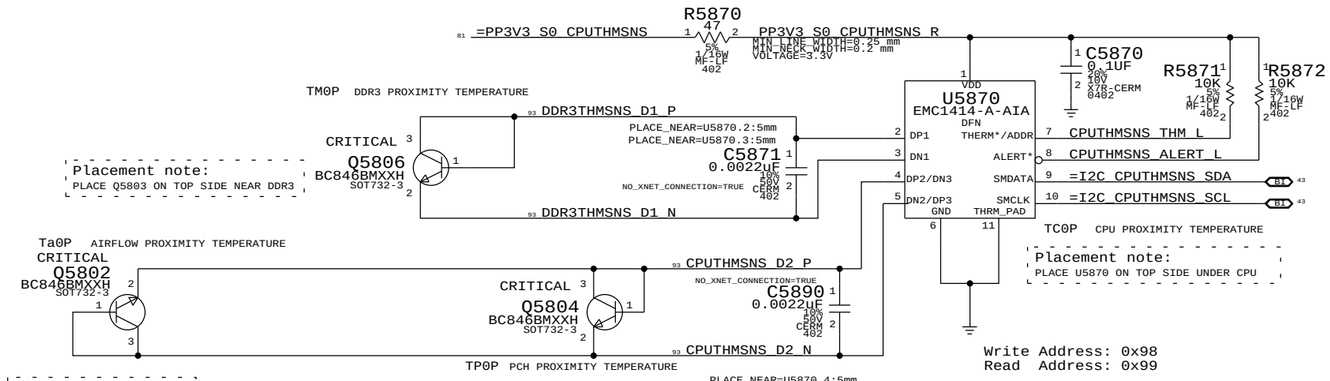
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



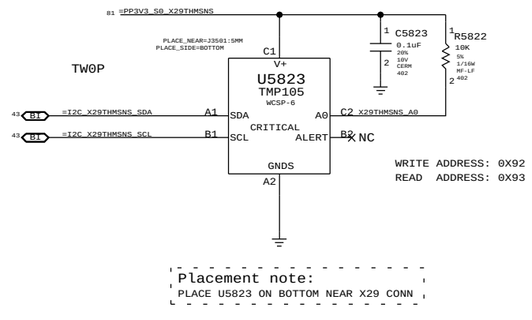
TBT DIE



DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



X29 PROXIMITY



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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Apple Inc.

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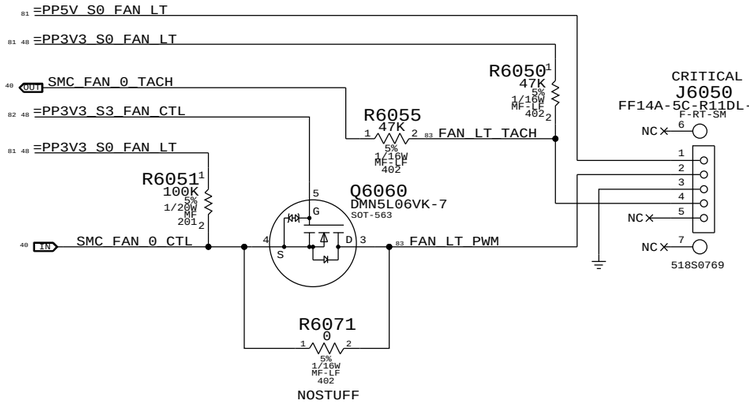
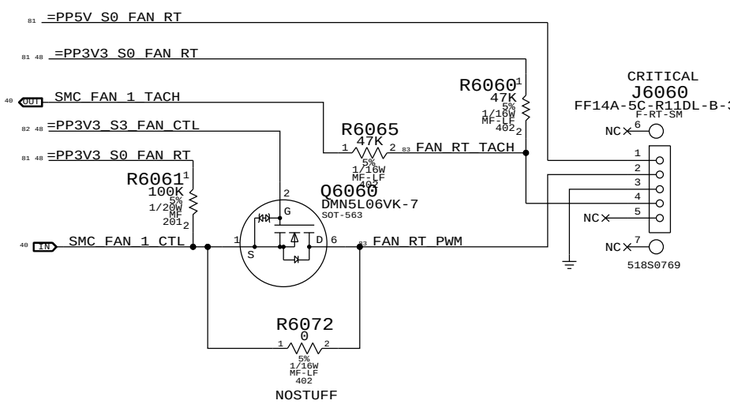
Left Fan



Right Fan



SYNC_MASTER=CLEAN_J45 SYNC_DATE=06/23/2013

PAGE TITLE: Fan Connectors

Apple Inc.

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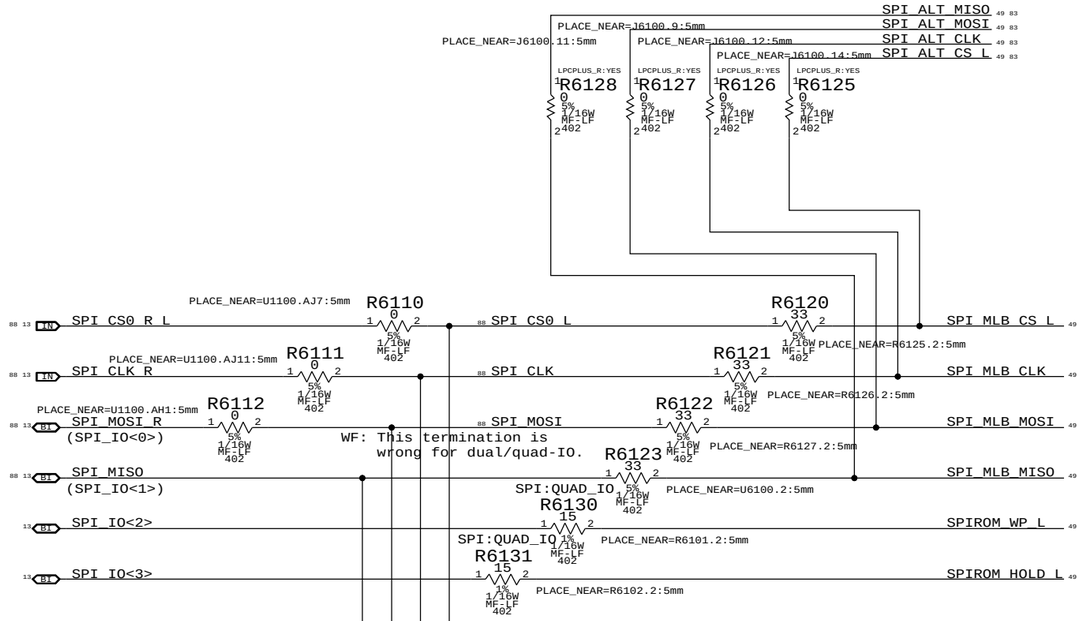
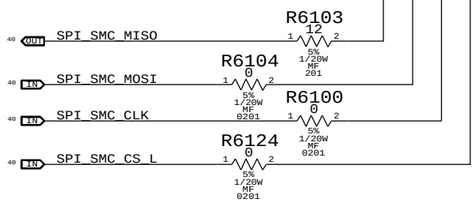
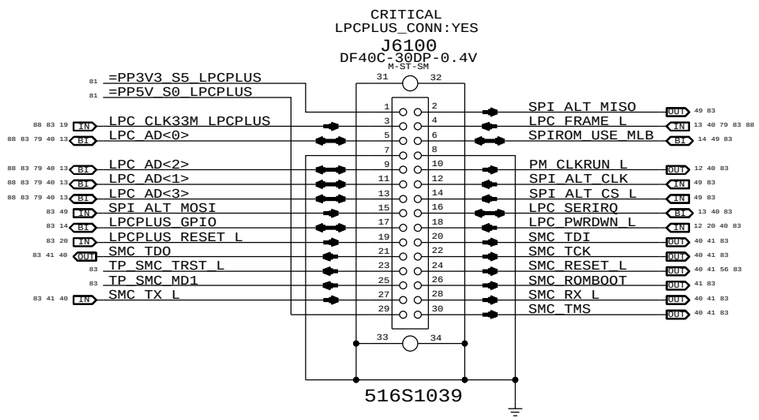
SPI Bus Series Termination



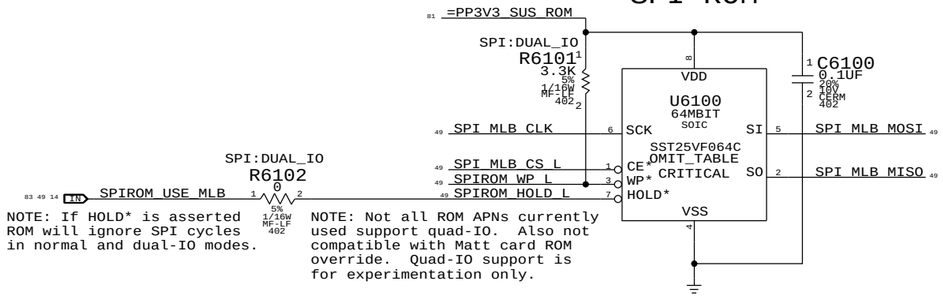
SMC12 SPI SUPPORT



LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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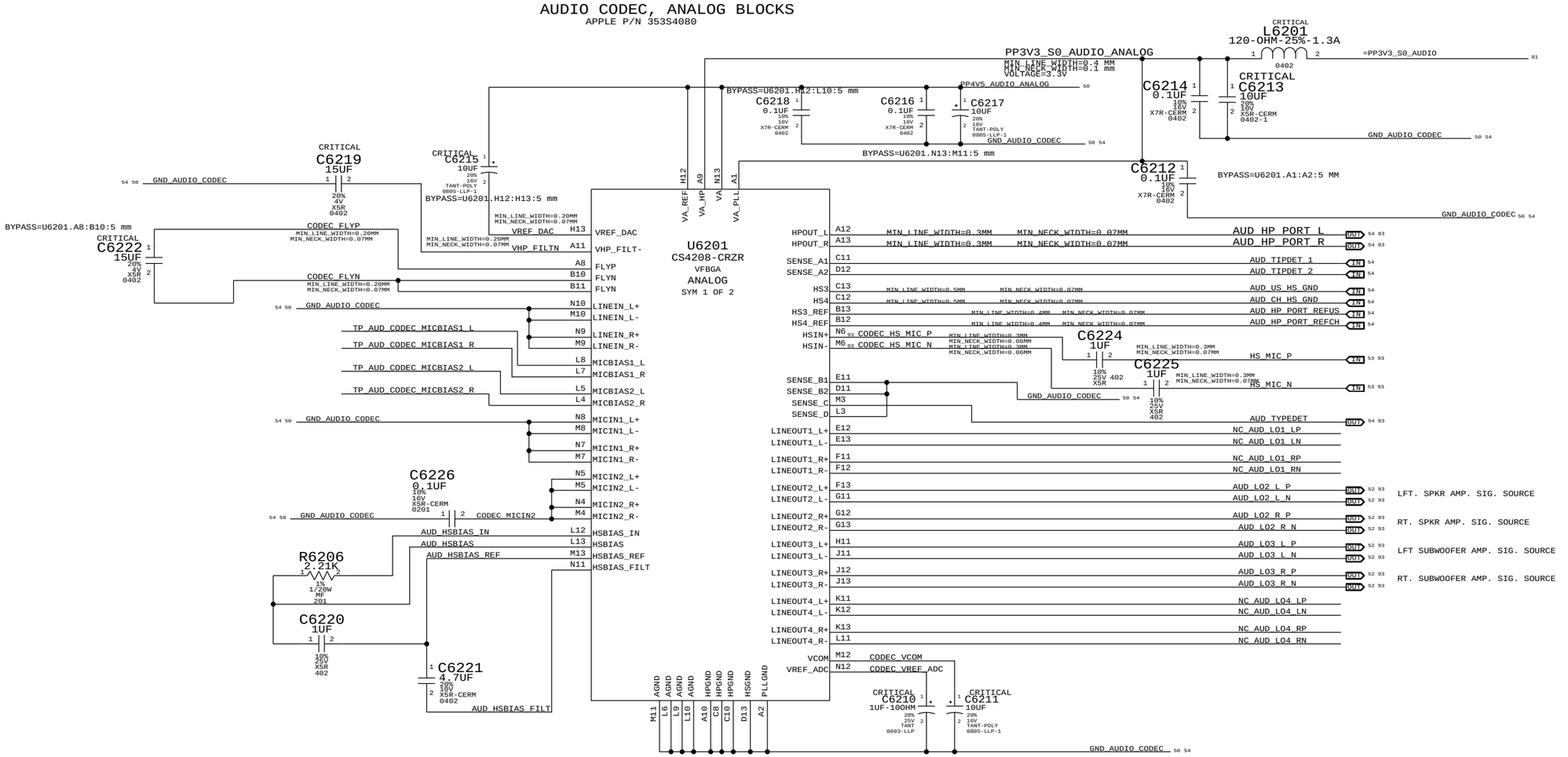
AUDIO CODEC, ANALOG BLOCKS

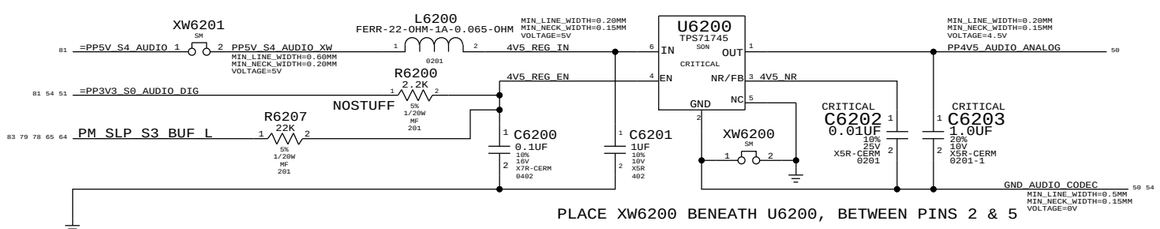
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: AUDIO:CODEC, ANALOG

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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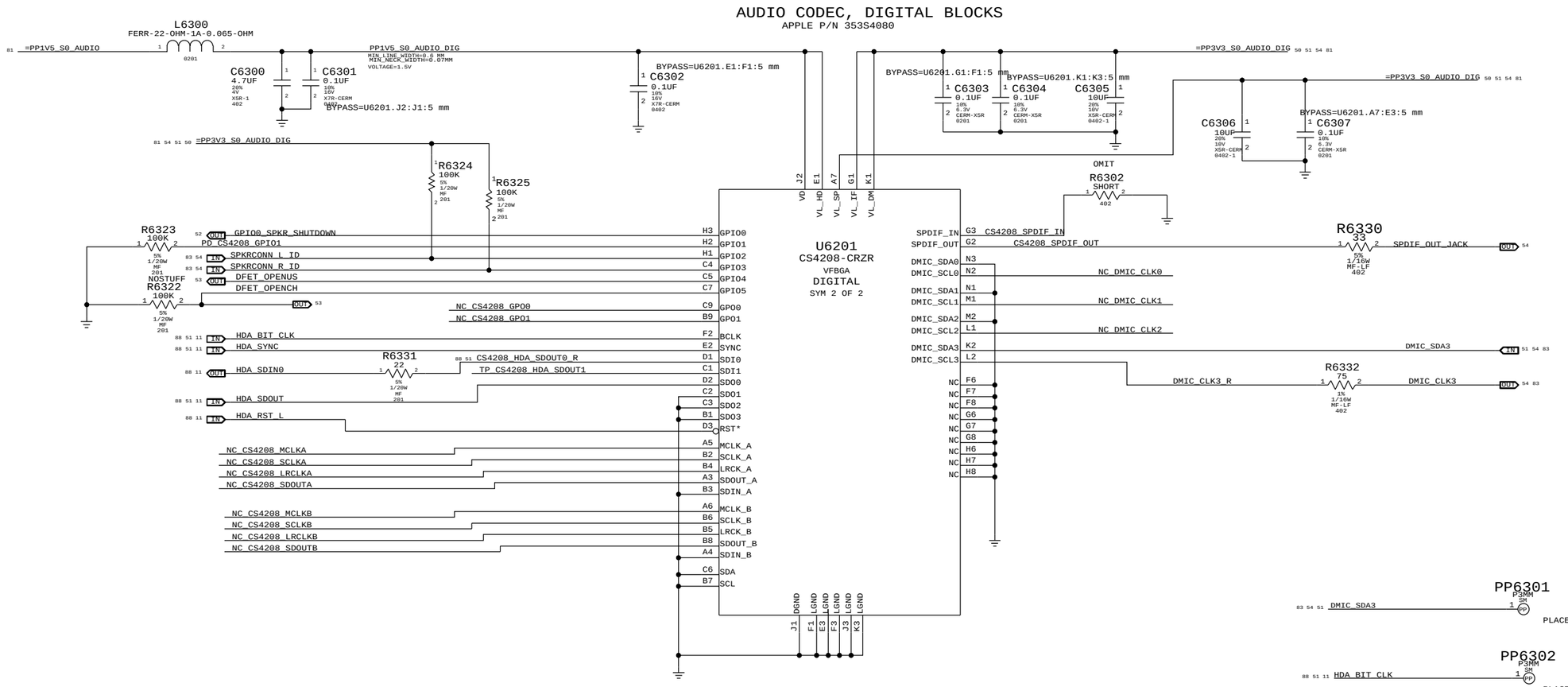
AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



PP6301
DMIC_SDA3
PLACE_NEAR=U6201.N3:5 mm

PP6302
HDA_BIT_CLK
PLACE_NEAR=U6201.F2:5 mm

PP6303
HDA_SYNC
PLACE_NEAR=U6201.E2:5 mm

PP6304
HDA_SDOUT
PLACE_NEAR=U6201.D2:5 mm

PP6305
CS4208_HDA_SDOUT0_R
PLACE_NEAR=U6201.D1:5 mm

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
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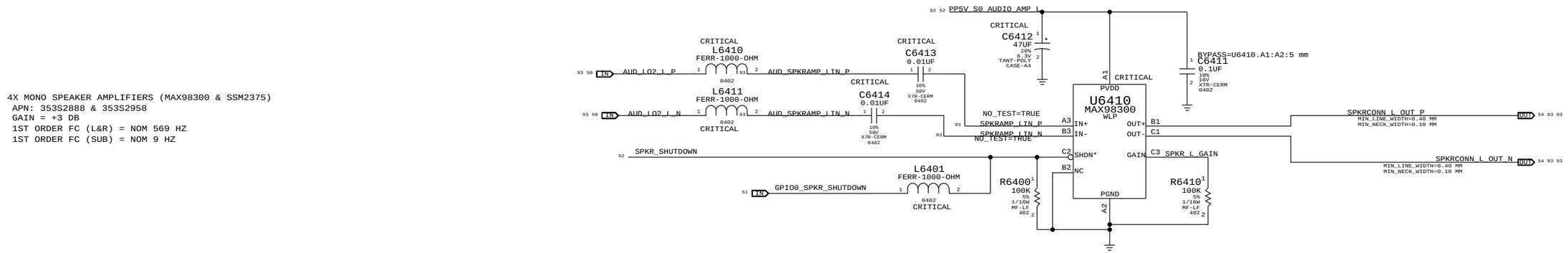
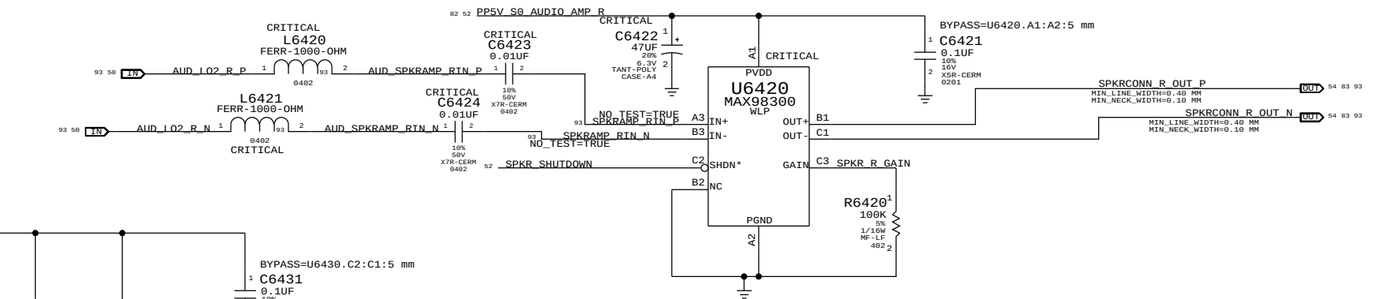
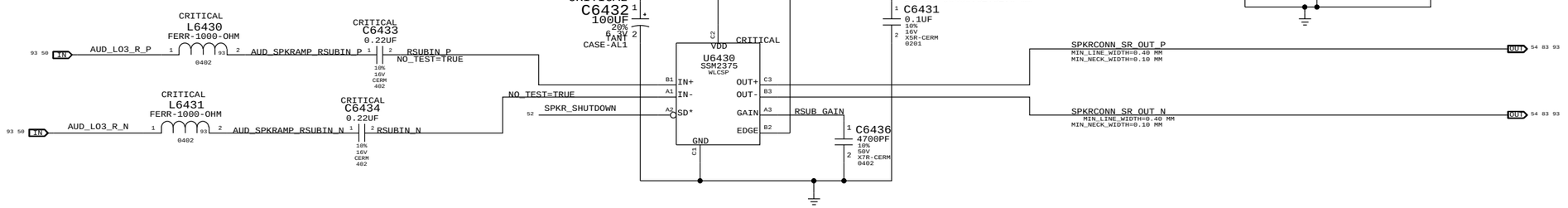
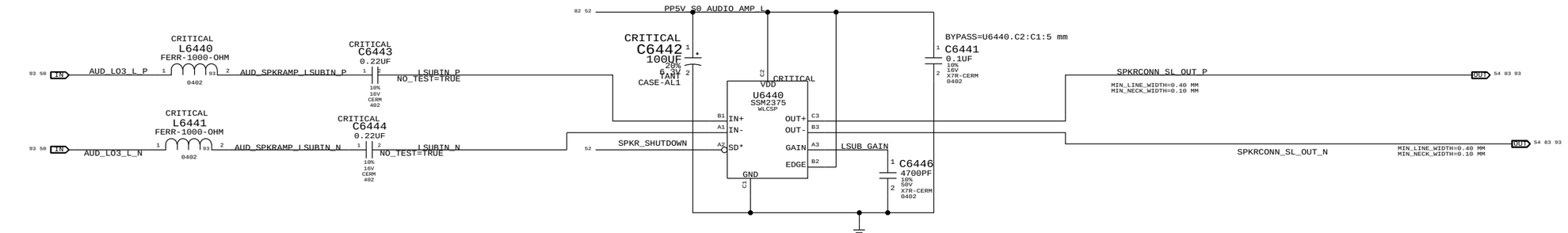
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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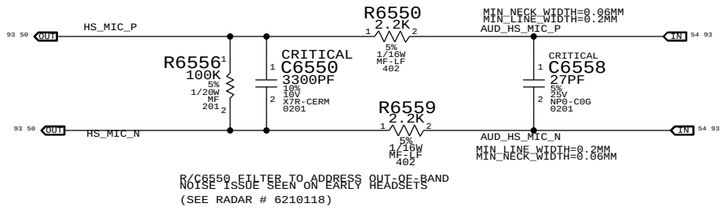

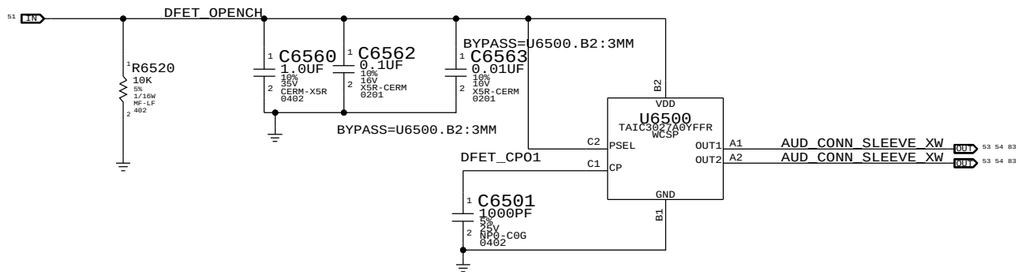

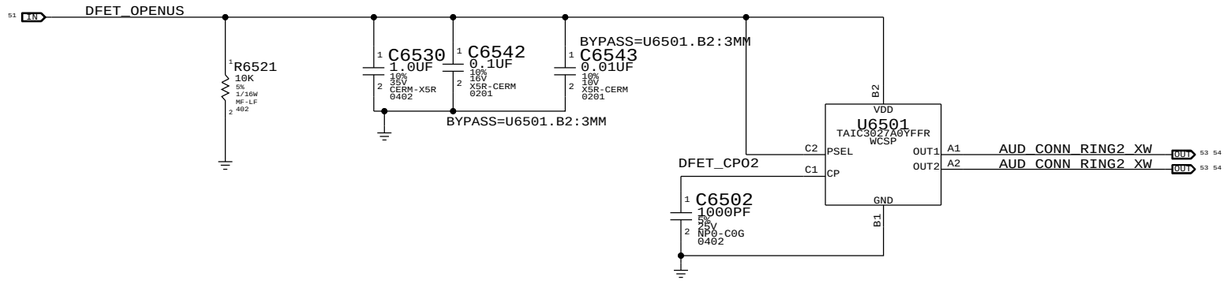

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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BRANCH: dvt

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

=PP3V3_S0_AUDIO_DIG
DMIC_SDA3
DMIC_CLK3
OMIT
R6680
SHORT
402
DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

L6611 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.3:2.54mm
XW6600 SM
L6612 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
AUD_CH_HS_GND
XW6601 SM
AUD_HS_MIC_P

L6613 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.5:2.54mm
XW6602 SM
L6614 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
AUD_US_HS_GND
XW6603 SM
AUD_HS_MIC_N

L6604 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
R6602 2.2K 5% 1/20W MF 201
L6608 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_2
AUD_CONN_TIPDET_2
GND_AUDIO_CODEC
R6603 2.2K 5% 1/20W MF 201
L6607 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_1
L6605 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CONN_TIPDET_1
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
L6606 FERR-470-OHM 0201 CRITICAL
AUD_TYPEDET
AUD_CONN_TYPEDET
SPDIF_OUT_JACK
=PP3V3_S0_AUDIO_DIG

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC
VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF
SHELL PINS

C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

R6601 10K 5% 1/16W MF-LF 402

DZ6607 ESDALC5-1BM2 SOD882 CRITICAL
C6602 100PF 5% 25V NP0-CERM 0201
DZ6601 ESDALC5-1BM2 SOD882 CRITICAL
C6603 100PF 5% 25V NP0-CERM 0201
C6604 100PF 5% 25V NP0-CERM 0201
DZ6602 ESDALC5-1BM2 SOD882 CRITICAL
C6605 100PF 5% 25V NP0-CERM 0201
DZ6603 ESDALC5-1BM2 SOD882 CRITICAL
C6606 100PF 5% 25V NP0-CERM 0201
DZ6606 ESDALC5-1BM2 SOD882 CRITICAL
DZ6605 ESDALC5-1BM2 SOD882 CRITICAL
C6607 100PF 5% 25V NP0-CERM 0201
C6608 100PF 5% 25V NP0-CERM 0201
DZ6604 ESDALC5-1BM2 SOD882 CRITICAL

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D
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MagSafe DC Power Jack

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM

518S0508

PP20V_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=20V

CRITICAL
F7005
6AMP-32V-0.00950HM
0603

=PP20V_DCIN_CONN

NOSTUFF
C7005
0.01UF
20% 50V CERM 0603

TP_TDM_ONEWIRE_MPM

=PP3V42_G3H_ONEWIREPROT

C7008
0.1UF
20% 10V CERM 402
PLACEMENT_NOTE=PLACE NEAR U7100 and U7001

CRITICAL
U7001
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK_VCC
SMC_BC_ACOK
SMC_BC_ACOK

C7000
0.1UF
20% 10V CERM 402

R7029
2.0K
5% 1/16W MF-LF 402

U7000
MAX9940
SC70-5
CRITICAL
VCC
EXT
INT
NC
GND

ADAPTER_SENSE
SYS_ONEWIRE

R7012
22.1K
1% 1/20W MF 201

Input impedance of 22.1K meets sparkitecture requirements for D2 design only

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

Q7010
SI5419DU
POWERPAK

R7010
100K
5% 1/20W MF 201

C7012
0.047UF
10% 25V X5R 0402

R7011
10K
5% 1/20W MF 201

DCIN_ISOL_GATE_R

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

DCIN_ISOL_GATE

=PP20V_DCIN_ISOL

D7010
CDZ6.8B
SM
6.8V Zener

R7020
47
1% 1/3W MF 805

PP20V_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V

CRITICAL
D7005
BAT30CWFILM
SOT-323

R7005
10
5% 1/8W MF-LF 805

=PPBUS_G3H

PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=20V

APN:353S3733
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

P3V42G3H_BOOST
DIDT=TRUE

C7090 4.7UF 10% 25V X5R-CERM 0603
C7091 4.7UF 10% 25V X5R-CERM 0603
NOSTUFF C7092 4.7UF 10% 25V X5R-CERM 0603
C7093 4.7UF 10% 25V X5R-CERM 0603
NOSTUFF C7096 4.7UF 10% 25V X5R-CERM 0603
NOSTUFF C7097 4.7UF 10% 25V X5R-CERM 0603

R7001
0
5% 1/20W MF 0201

P3V42G3H_SHDN_L

U7090
LT3470AED
DFN
VIN
BOOST
SHDN*
SW
BIAS
FB
GND
THRM PAD
NC

C7094
0.22UF
10% 10V CERM 402

CRITICAL
L7095
33UH-20%-0.39A-0.435OHM
DP418C-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

=PP3V42_G3H_REG

Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

C7095
22PF
5% 50V NPO-C0G-CERM 0201

<Ra>
R7095
348K
1% 1/20W MF 201

<Rb>
R7096
200K
1% 1/20W MF 201

C7099
22UF
20% 6.3V X5R-CERM-1 603

OMIT
C7001
NOSTUFF
NONE
NONE
NONE
402

NOSTUFF
R7002
49.9K
1% 1/20W MF 201

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

BATTERY CONNECTOR

518-0376
CRITICAL
J7050
BAT-J5
F-ST-TH
VER 1

PPVBAT_G3H_CONN
NC
NC
SMBUS_BATT_SCL
SMBUS_BATT_SDA
SYS_DETECT_L

C7050 0.1UF 10% 25V X5R 402
C7060 1UF 10% 25V X5R 603-1

CRITICAL
D7050
RCLAMP2402B
SC-75

R7050
10K
5% 1/10W MF-LF 402

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

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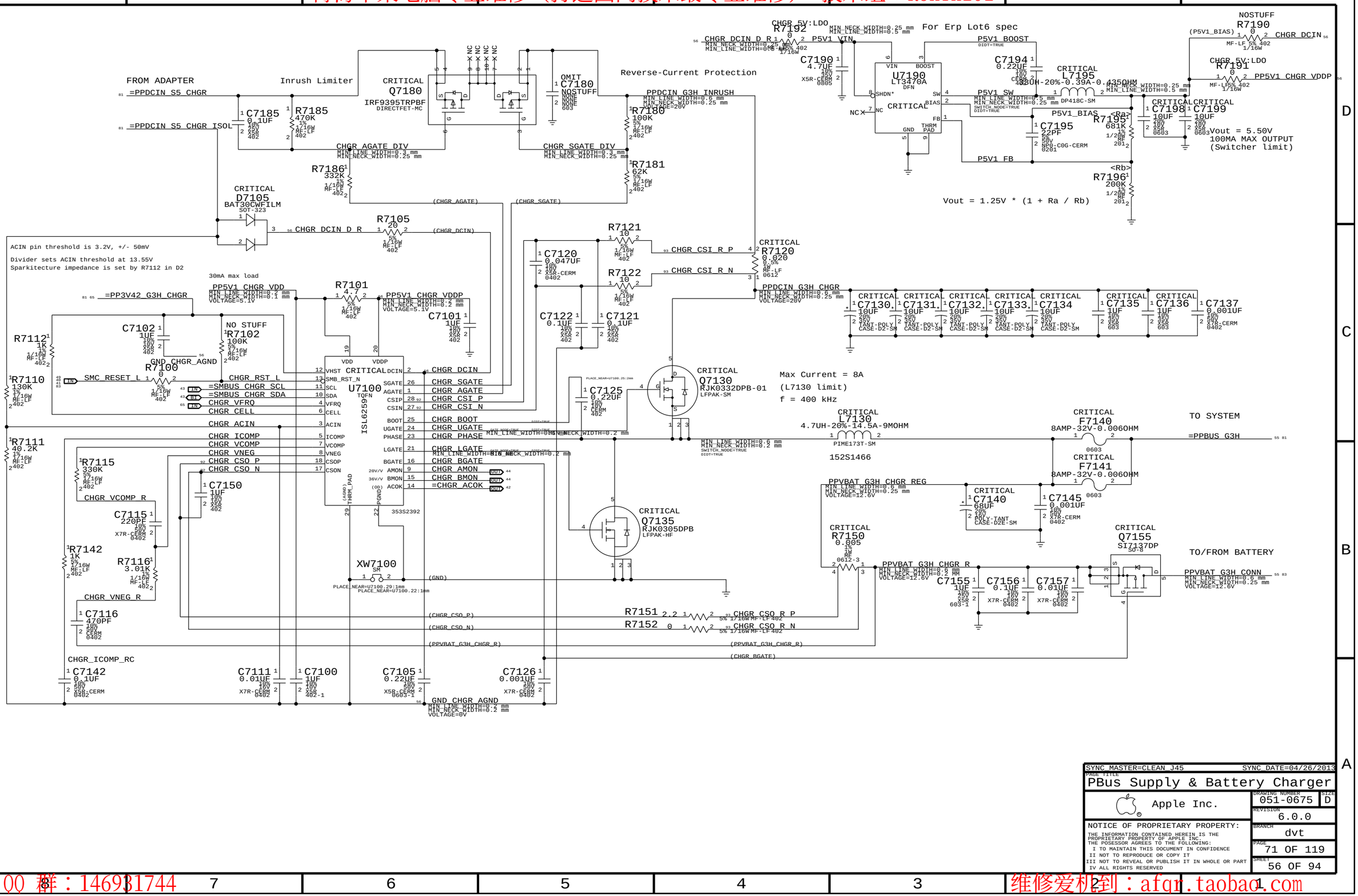

SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
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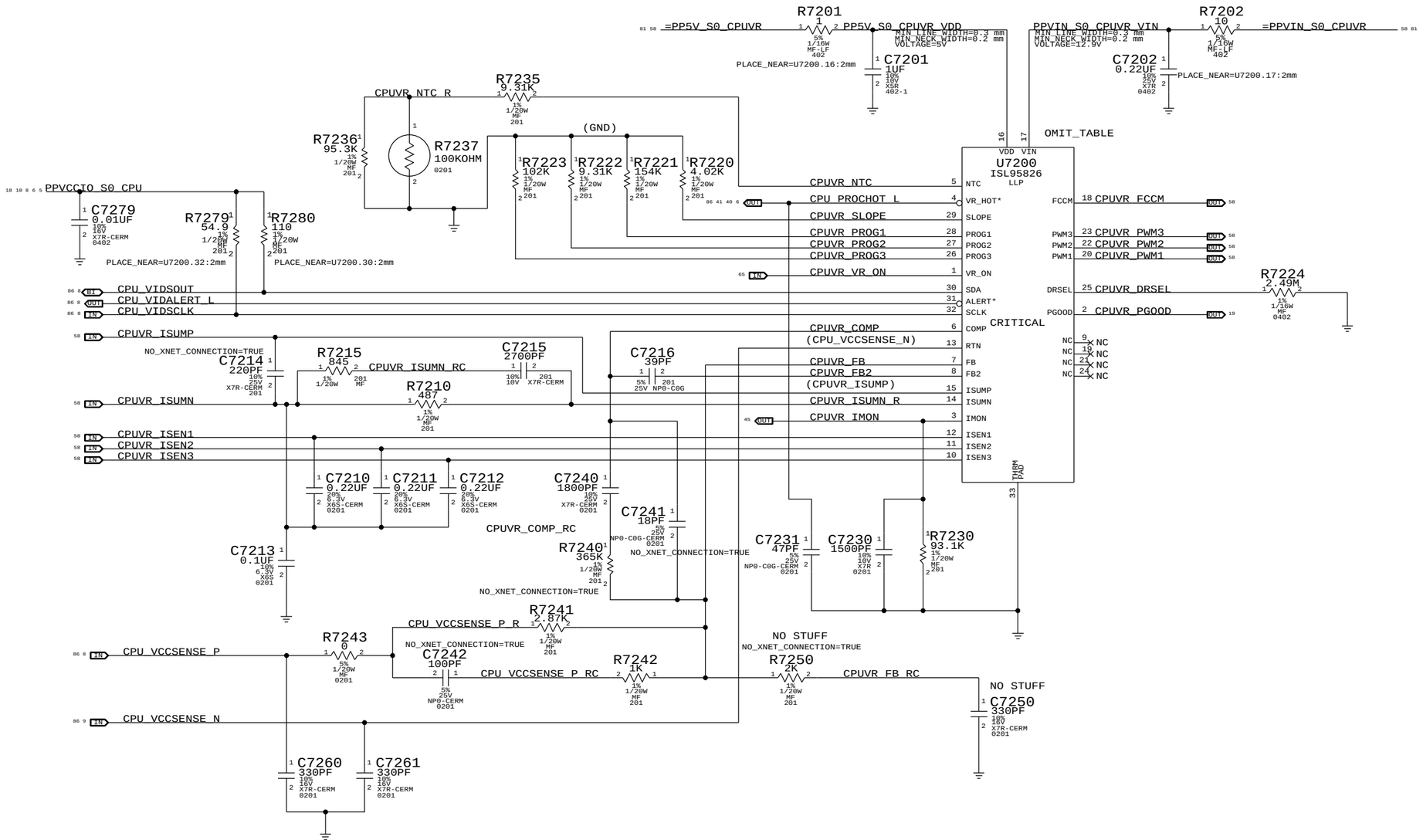
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

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=PPVIN_S0_CPUVR
=PP5V_S0_CPUVR

PHASE 1

U7310 FDMF6808N PQFN CRITICAL 353S3836

R7311 0 5% 1/10W MF-LF 402
CPUVR_BOOT1_RC — CPUVR_BOOT1
C7311 0.22UF 10% 16V CERM 402
CPUVR_PHASE1_K
CPUVR_PWM1
CPUVR_FCCM

C7310 1UF 10% 16V X6S-CERM 0402

L7310 CRITICAL 0.36UH-20%-36A-0.001080HM
PIMS103T-SM 152S1538
CPUVR_PHASE1 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.2 MM — DIDT=TRUE — SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH1 — MIN_LINE_WIDTH=0.6 MM — MIN_NECK_WIDTH=0.25 MM — VOLTAGE=1.8V
CPUVR_ISNS1_P

R7310 0.00075 1% 1W MF 0612 CRITICAL
R7312 2.2 5% 1/10W MF-LF 603 NOSTUFF
C7312 0.001UF 10% 50V X7R-CERM 0402 DIDT=TRUE NOSTUFF
CPUVR_PH1_SNUB

CPUVR_ISNS1_N
R7314 3.9 1% 1/20W MF 201
CPUVR_ISUMN — NO_XNET_CONNECTION=TRUE
R7315 1K 1% 1/20W MF 201
R7316 10K 1% 1/20W MF 201
CPUVR_ISEN1
CPUVR_ISUMP

R7317 10K 1% 1/20W MF 201 — CPUVR_ISNS2_N — NO_XNET_CONNECTION=TRUE
R7318 10K 1% 1/20W MF 201 — CPUVR_ISNS3_N — NO_XNET_CONNECTION=TRUE

C7313 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7314 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7315 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7316 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7317 1UF 10% 16V X6S-CERM 0402
C7318 0.001UF 10% 50V X7R-CERM 0402 — THESE TWO CAPS ARE FOR EMC
C7319 0.001UF 10% 50V X7R-CERM 0402

Additonal Input Bulk Caps
C7370 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7371 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7372 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7373 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7374 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7375 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7376 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7377 CRITICAL 15UF 20% 16V TANT SM
C7378 CRITICAL 15UF 20% 16V TANT SM
C7379 CRITICAL 15UF 20% 16V TANT SM
C7380 CRITICAL 15UF 20% 16V TANT SM

=PPVCC_S0_CPU_REG

Vout = 1.85V max
95A max output
f = 450 kHz

PHASE 2

U7320 FDMF6808N PQFN CRITICAL 353S3836

R7321 0 5% 1/10W MF-LF 402
CPUVR_BOOT2_RC — CPUVR_BOOT2
C7321 0.22UF 10% 16V CERM 402
CPUVR_PHASE2_K
CPUVR_PWM2
CPUVR_FCCM

C7320 1UF 10% 16V X6S-CERM 0402

L7320 CRITICAL 0.36UH-20%-36A-0.001080HM
PIMS103T-SM 152S1538
CPUVR_PHASE2 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.2 MM — DIDT=TRUE — SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH2 — MIN_LINE_WIDTH=0.6 MM — MIN_NECK_WIDTH=0.25 MM — VOLTAGE=1.8V
CPUVR_ISNS2_P

R7320 0.00075 1% 1W MF 0612 CRITICAL
R7322 2.2 5% 1/10W MF-LF 603 NOSTUFF
C7322 0.001UF 10% 50V X7R-CERM 0402 DIDT=TRUE NOSTUFF
CPUVR_PH2_SNUB

CPUVR_ISNS2_N
R7324 3.9 1% 1/20W MF 201
CPUVR_ISUMN — NO_XNET_CONNECTION=TRUE
R7325 1K 1% 1/20W MF 201
R7326 10K 1% 1/20W MF 201
CPUVR_ISEN2
CPUVR_ISUMP

R7327 10K 1% 1/20W MF 201 — CPUVR_ISNS1_N — NO_XNET_CONNECTION=TRUE
R7328 10K 1% 1/20W MF 201 — CPUVR_ISNS3_N — NO_XNET_CONNECTION=TRUE

C7323 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7324 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7325 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7326 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7327 1UF 10% 16V X6S-CERM 0402
C7328 0.001UF 10% 50V X7R-CERM 0402 — THESE TWO CAPS ARE FOR EMC
C7329 0.001UF 10% 50V X7R-CERM 0402

PHASE 3

U7330 FDMF6808N PQFN CRITICAL 353S3836

R7331 0 5% 1/10W MF-LF 402
CPUVR_BOOT3_RC — CPUVR_BOOT3
C7331 0.22UF 10% 16V CERM 402
CPUVR_PHASE3_K
CPUVR_PWM3
CPUVR_FCCM

C7330 1UF 10% 16V X6S-CERM 0402

L7330 CRITICAL 0.36UH-20%-36A-0.001080HM
PIMS103T-SM 152S1538
CPUVR_PHASE3 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.2 MM — DIDT=TRUE — SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH3 — MIN_LINE_WIDTH=0.6 MM — MIN_NECK_WIDTH=0.25 MM — VOLTAGE=1.8V
CPUVR_ISNS3_P

R7330 0.00075 1% 1W MF 0612 CRITICAL
R7332 2.2 5% 1/10W MF-LF 603 NOSTUFF
C7332 0.001UF 10% 50V X7R-CERM 0402 DIDT=TRUE NOSTUFF
CPUVR_PH3_SNUB

CPUVR_ISNS3_N
R7334 3.9 1% 1/20W MF 201
CPUVR_ISUMN — NO_XNET_CONNECTION=TRUE
R7335 1K 1% 1/20W MF 201
R7336 10K 1% 1/20W MF 201
CPUVR_ISEN3
CPUVR_ISUMP

R7337 10K 1% 1/20W MF 201 — CPUVR_ISNS1_N — NO_XNET_CONNECTION=TRUE
R7338 10K 1% 1/20W MF 201 — CPUVR_ISNS2_N — NO_XNET_CONNECTION=TRUE

C7333 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7334 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7335 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7336 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7337 1UF 10% 16V X6S-CERM 0402
C7338 0.001UF 10% 50V X7R-CERM 0402 — THESE TWO CAPS ARE FOR EMC
C7339 0.001UF 10% 50V X7R-CERM 0402

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU VR12.5 VCC Power Stage

Apple Inc.

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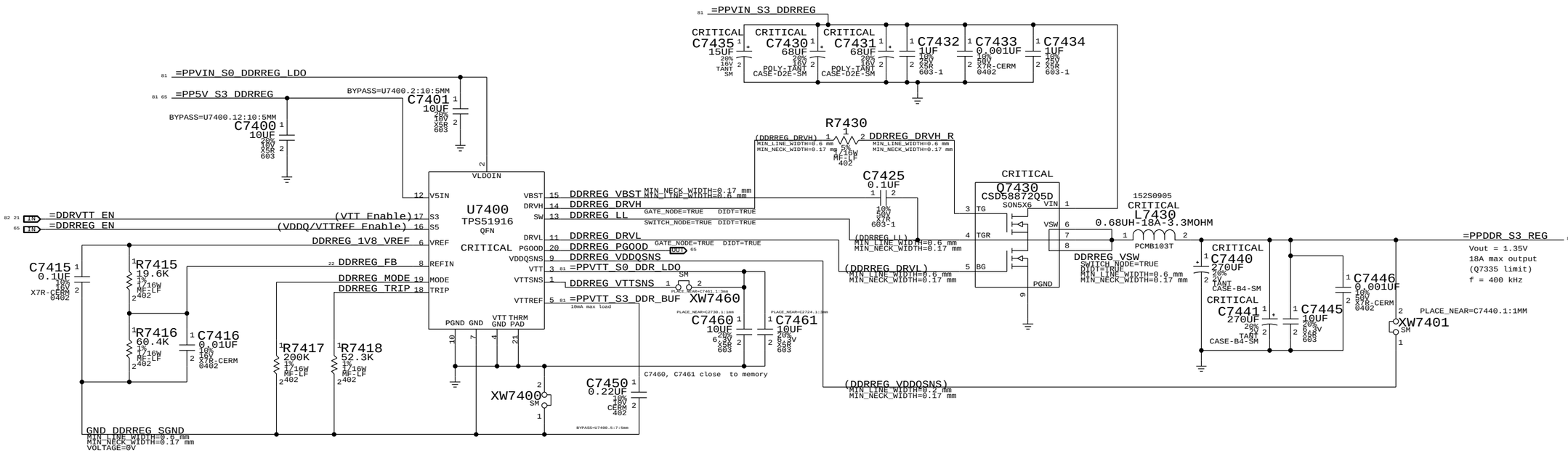
DDR3L (1V35 S3) REGULATOR



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	1.35V DDR3L SUPPLY
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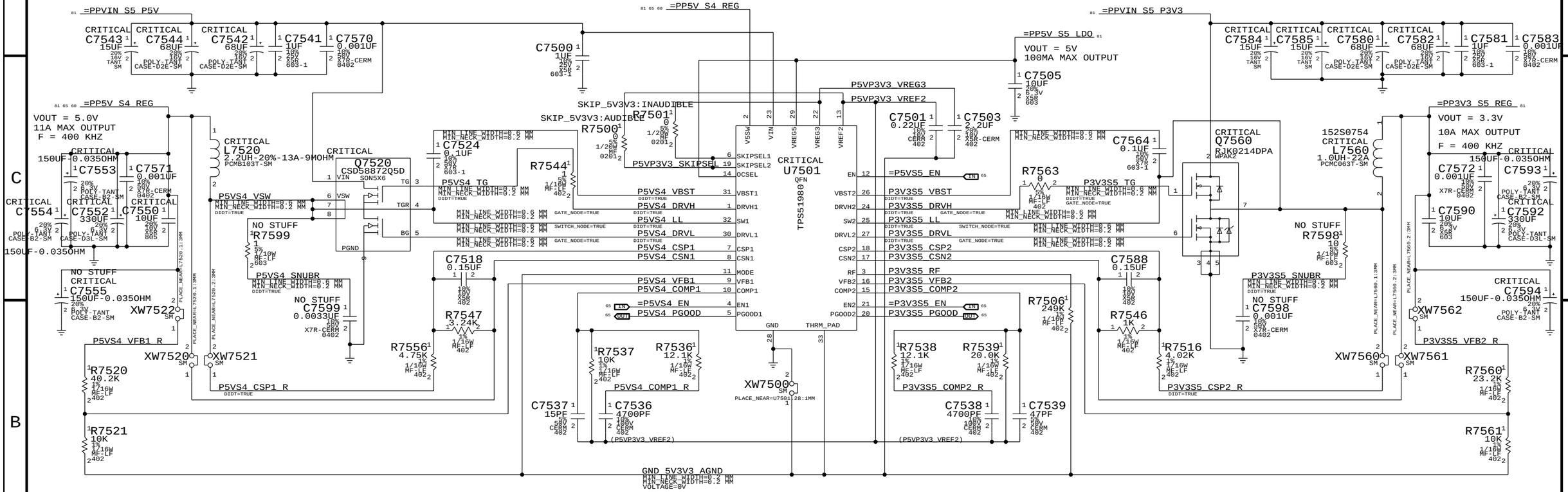
NOTICE OF PROPRIETARY PROPERTY:



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

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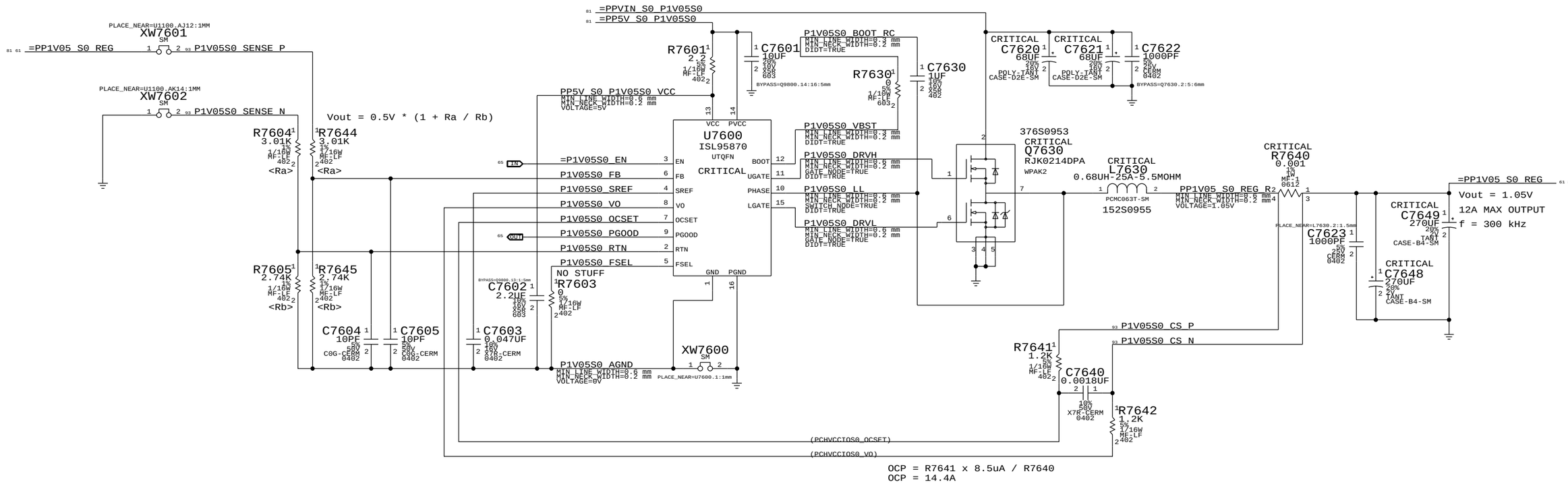
1V05 S0 REGULATOR



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	1V05V POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-0675 · SIZE D
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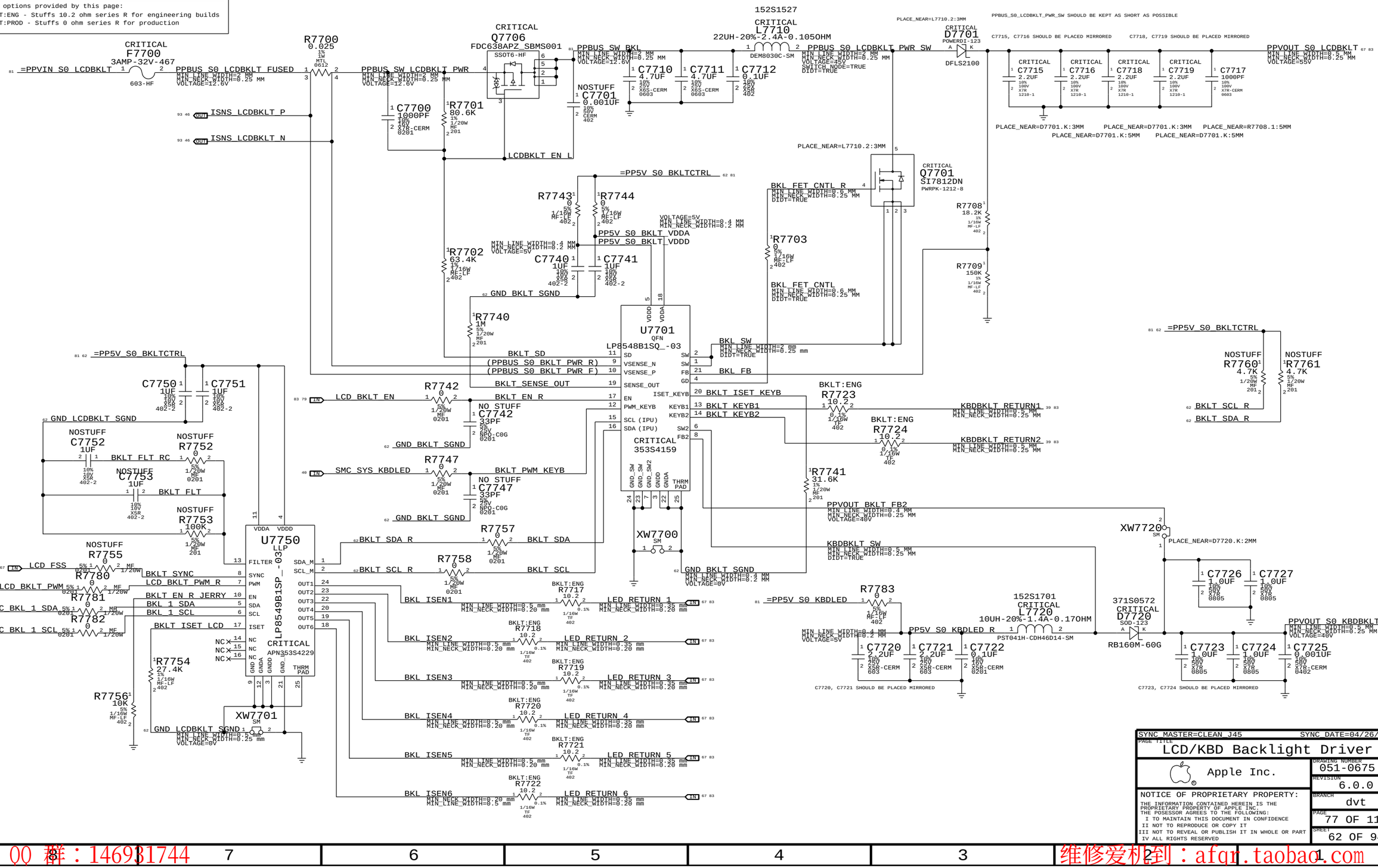
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717,R7718,R7719,R7720,R7721,R7722,R7723,R7724		BKLT:PROD



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: LCD/KBD Backlight Driver

Apple Inc.

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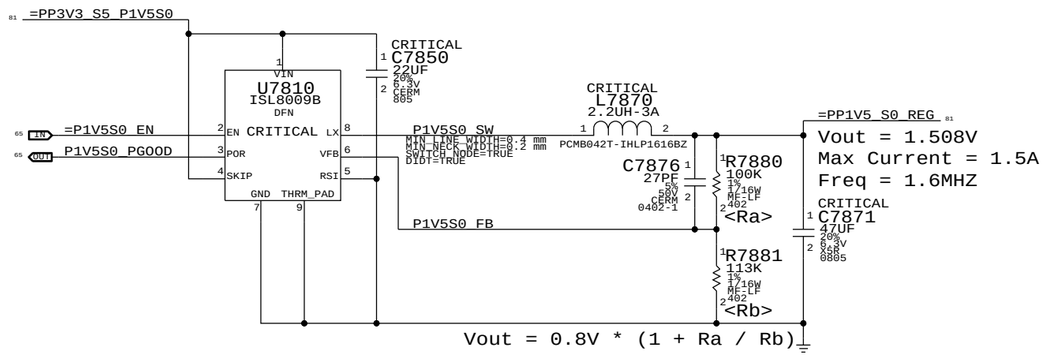
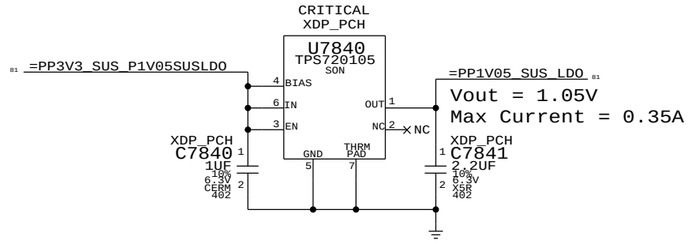
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Misc Power Supplies

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EDP is per J45 Power Budget rev5

3.3V S4 FET

Q8000 SIA413DJ CRITICAL SC70-6L 376S0945

=PP3V3_S4_P3V3S4FET → Q8000 S → =PP3V3_S4_FET

Q8002 DMN5L06VK-7 SOT-563

R8002 220K 5% 1/16W MF-LF 402 (=PP3V3_S4_P3V3S4FET → P3V3S4_EN_L)

C8009 0.033UF 10% 16V X5R 402

R8000 47K 5% 1/16W MF-LF 402 (P3V3S4_EN_L → P3V3S3_S4)

C8000 0.01UF 10% 16V X7R-CERM 0402

65 IN =P3V3S4_EN

3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

Q8010 SIA413DJ CRITICAL SC70-6L

=PP3V3_S3_P3V3S3FET → Q8010 S → =PP3V3_S3_FET

Q8012 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

R8012 47K 5% 1/16W MF-LF 402 (=PP3V3_S3_P3V3S3FET → P3V3S3_EN_L)

C8011 0.033UF 10% 16V X5R 402

R8010 39K 5% 1/16W MF-LF 402 (P3V3S3_EN_L → P3V3S3_SS)

C8010 0.01UF 10% 16V X7R-CERM 0402

65 IN =P3V3S3_EN

3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

Q8050 SIA427DJ CRITICAL SC70-6L

=PP5V_S4_P5VS3FET → Q8050 S → =PP5V_S3_FET

Q8052 DMN5L06VK-7 SOT-563

R8052 200K 5% 1/16W MF-LF 402 (=PP5V_S4_P5VS3FET → P5VS3_EN_L)

C8051 0.033UF 10% 16V X5R 402

R8050 5.1K 5% 1/16W MF-LF 402 (P5VS3_EN_L → P5VS3_SS)

C8050 0.01UF 10% 16V X7R-CERM 0402

65 IN =P5VS3_EN

5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

=PP5V_S5_P1V35S3RS0FET

C8001 0.1UF 20% 10V CERM 402

U8001 SLG5AP1438V TDFN CRITICAL (VDD, CAP, ON, D, S, GND)

P1V35CPU_SLEW_CTL → CAP

21 IN CPUVDDQ_EN → ON

C8002 0.018UF 10% 16V X7R 402

Slew rate : 0.8V/ms = 19.75nF

U8001 D → =PPVIN_S3_P1V35S3RS0_FET

U8001 S → =PP1V35_S3RS0_FET

XW8005 SM =PP1V35_S3RS0_FET → =PP1V35_S3RS0_FET_ISNS

NC_ISNS_CPUDDRN (OUT 46)

NC_ISNS_CPUDDRP (OUT 46)

1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

3.3V S0 GPU MISC FET

Q8080 SIA413DJ CRITICAL SC70-6L

=PP3V3_GPU_MISC_P3V3GPUMISCFET → Q8080 S → =PP3V3_S0GPU_MISC_FET

R8082 33K 5% 1/16W MF-LF 402 (=PP3V3_GPU_MISC_P3V3GPUMISCFET → P3V3GPU_MISC_EN)

C8081 0.47UF 10% 6.3V CERM-X5R 402

R8080 1K 5% 1/16W MF-LF 402 (P3V3GPU_MISC_EN → P3V3GPU_MISC_SS)

C8080 0.01UF 10% 16V X7R-CERM 0402

Q8082 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

66 IN =P3V3GPU_MISC_EN

3.3V S0 MISC GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

SSD_PWR_EN:GPIO 66 IN =P3V3SUS_EN

R8073 0 0201 1/20W 5% MF

SSD_PWR_EN:S0

18 13 SSD_PWR_EN

R8074 0 0201 1/20W 5% MF

83 79 78 65 50 PM_SLP_S3_BUF_L

34 SSD_PWR_FET_EN

3.3V SUS FET

Q8020 SIA413DJ CRITICAL SC70-6L

=PP3V3_S5_P3V3SUSFET → Q8020 S → =PP3V3_SUS_FET

Q8002 DMN5L06VK-7 SOT-563

R8022 100K 5% 1/16W MF-LF 402 (=PP3V3_S5_P3V3SUSFET → P3V3SUS_EN_L)

C8021 0.033UF 10% 16V X5R 402

R8020 12K 5% 1/16W MF-LF 402 (P3V3SUS_EN_L → P3V3SUS_SS)

C8020 0.01UF 10% 16V X7R-CERM 0402

3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm

Q8070 SI7615DN CRITICAL PWRPK-1212-8

=PP3V3_S5_P3V3S0SW_SSD → Q8070 S → =PP3V3_S0SW_SSD_R

Q8072 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

R8072 47K 5% 1/16W MF-LF 402 (=PP3V3_S5_P3V3S0SW_SSD → P3V3_SSD_EN_L)

C8071 0.033UF 10% 16V X5R 402

R8070 33K 5% 1/16W MF-LF 402 (P3V3_SSD_EN_L → P3V3_SSD_SS)

C8070 0.01UF 10% 16V X7R-CERM 0402

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

Q8060 SI7615DN CRITICAL PWRPK-1212-8

=PP5V_S4_P5VS0FET → Q8060 S → =PP5V_S0_FET

R8062 270K 5% 1/16W MF-LF 402 (=PP5V_S4_P5VS0FET → P5V0S0_EN_L)

C8061 0.12UF 10% 10.0V CERM-X5R 402

R8060 6.2K 5% 1/16W MF-LF 402 (P5V0S0_EN_L → P5V0S0_SS)

C8060 0.47UF 10% 10V X5R 0402

Q8052 DMN5L06VK-7 SOT-563

65 IN =P5VS0_EN

5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 GPU FET

Q8090 SIA413DJ CRITICAL SC70-6L

=PP3V3_GPU_P3V3GPUFET → Q8090 S → =PP3V3_S0GPU_FET

R8092 33K 5% 1/16W MF-LF 402 (=PP3V3_GPU_P3V3GPUFET → P3V3GPU_EN_L)

C8091 0.33UF 10% 6.3V X6S-X6M 0402

R8090 1K 5% 1/16W MF-LF 402 (P3V3GPU_EN_L → P3V3GPU_SS)

C8090 0.01UF 10% 16V X7R-CERM 0402

Q8092 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

66 IN =P3V3GPU_EN

3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.6A (EDP)

3.3V S0 Switch

U8030 TPS22924C

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

APN 353S2741

=PP3V3_S0_P3V3S0FET → U8030 A2/B2 VIN

U8030 CSP CRITICAL ON C2 ← =P3V3S0_EN

U8030 A1/B1 VOUT → =PP3V3_S0_FET

Max Current = 2A

U8030 GND C1

C8030 1UF 10% 6.3V X5M 402

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Power FETs

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Power State Debug LEDs
(For development only)

=PP3V3_S5_DBGLED 81
DBGLED
PLACE_SIDE=BOTTOM
PP3V3_S5_DBGLED
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.25 MM
VOLTAGE=3.3V
R8194 0 5% 1/16W MF-LF 402

DBGLED_S5: R8190 20K 5% 1/20W MF 201 → D8190 GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S5_ON) → Q8190 DMN5L06VK-7 SOT-563 → S4_PWR_EN
DBGLED_S4: R8191 20K 5% 1/20W MF 201 → D8191 GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S4_ON) → Q8190 DMN5L06VK-7 SOT-563 → PM_SLP_S4_L
DBGLED_S3: R8192 20K 5% 1/20W MF 201 → D8192 GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S3_ON) → Q8190 DMN5L06VK-7 SOT-563 → PM_SLP_S3_BUF_L
DBGLED_S0: R8193 20K 5% 1/20W MF 201 → D8193 GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S0_ON) → Q8191 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

=PP3V3_S5_PWRCTL 81 65
BYPASS=U8170.6:3:2.3mm
C8170 0.1uF 20% 10V CERM 402
PM_SLP_S5_L:100K pull down on PCH page
PM_SLP_S5_L 40 12 IN
SMC_S4_WAKESRC_EN 41 40 IN
U8170 74LVC1G32 SOT891 (NC)
S4_PWR_EN 4 65 OUT
MAKE_BASE=TRUE
P5VS4_EN_D
D8174 BAT54XV2T1 SOD-523
R8174 43K 5% 1/16W MF-LF 402
R8175 240 5% 1/10W MF-LF 402
C8174 2.2UF 10% 6.3V X5R 402
P5VS4_EN = =P5VS4_EN OUT 60
=P3V3S4_EN OUT 64
=TBTAPWRSW_EN OUT 31
=TBTBPWRSW_EN OUT 32

S3 ENABLE

PM_SLP_S4_L 83 78 65 40 37 33 21 12 IN
PM_SLP_S4_L:100K pull down in PCH page
R8111 5.1K 5% 1/16W MF-LF 402
R8112 0 5% 1/16W MF-LF 402
R8113 0 5% 1/16W MF-LF 402
R8114 3.3K 5% 1/20W MF 201
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402
C8113 0.47UF 10% 6.3V CERM-X5R 402
C8114 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF
TPAD_VBUS_EN OUT 38
P5VS3_EN = =P5VS3_EN OUT 64
P3V3S3_EN = =P3V3S3_EN OUT 64
DDRREG_EN = =DDRREG_EN OUT 59
MAKE_BASE=TRUE

CPUVCORE ENABLE

ALL_SYS_PWRGD 83 65 40 19 18 = CPUVR_VR_ON OUT 57
MAKE_BASE=TRUE

S0 ENABLE

=PP3V3_S5_PWRCTL 81 65
BYPASS=U8180.5:2:2.3mm
C8180 0.1uF 20% 10V CERM 402
MC74VHC1G08 SC70-HF (U8180)
PM_SLP_S3_BUF_L OUT 50 64 65 78 79 83
(PM_SLP_S3_BUF_L)
PM_SLP_S3_L 83 40 21 12 IN
R8178 100 5% 1/16W MF-LF 402
PM_SLP_S3_L:100K pull down in PCH page
MAKE_BASE=TRUE
R8180 100K 5% 1/16W MF-LF 402 NO STUFF
D8185 BAT54XV2T1 SOD-523
R8185 130K 5% 1/16W MF-LF 402
R8186 20K 5% 1/16W MF-LF 402
R8187 0 5% 1/16W MF-LF 402
R8138 820 5% 1/16W MF-LF 402
P1V05_EN_D
P1V05S0_EN MAKE_BASE=TRUE
C8185 0.82UF 10% 6.3V X5R 402
C8186 0.68UF 10% 6.3V CERM 402
C8187 0.68UF 10% 6.3V CERM 402 NO STUFF
MAKE_BASE=TRUE
P5VS0_EN = =P5VS0_EN OUT 64
P3V3S0_P1V5_S0_EN = =P3V3S0_P1V5_S0_EN OUT 64
=P1V5S0_EN OUT 63
=P1V05S0_EN OUT 61
=PBUSVSENS_EN OUT 44
=TBT_S0_EN OUT 31 32

3.3V SUS Enable

PM_SLP_SUS_L 12 IN
MAKE_BASE=TRUE
=P3V3SUS_EN OUT 64
=DCINVSENS_EN OUT 44
PM_SLP_SUS_L: 100K pull down on PCH page

3.3V SUS Detect

=PP3V3_S5_PWRCTL 81 65
No stuff C8131, 12ms Min delay time
U8130 Sense input threhold is 3.07V
C8130 0.1uF 20% 10V CERM 402
CRITICAL
U8130 TPS3808G33DBVRG4 SOT23-6 (VDD, SENSE, CT, GND, RESET*, MR*)
=PP3V3_SUS_CNTRL 65 81
R8133 100K 5% 1/16W MF-LF 402
=PP3V3_SUS_CNTRL 81 65
PM_RSMRST_L OUT 12 83 88
PM_RSMRST_L goes to U1100.C21
SUS_PGOOD_CT
C8131 0.001UF 20% 50V CERM 402 NO STUFF
TP_SUS_PGOOD_MR_L

S5 Rail Enables & PGOOD

SMC_PM_G2_EN 41 40 IN
MAKE_BASE=TRUE
R8140 100 5% 1/16W MF-LF 402
P3V3S5_EN = =P3V3S5_EN OUT 60
=P5VS5_EN OUT 60
C8142 0.0033UF 10% 50V X7R-CERM 0402 NO STUFF
PLACE_NEAR=U7501.21:7mm
=PP3V42_G3H_PWRCTL 81
PLACE_NEAR=U7501.20:7mm
R8141 100K 5% 1/16W MF-LF 402
S5_PWRGD-->SMC
SMC-->PM_DSW_PWRGD
P3V3S5_PGOOD 60 = S5_PWRGD OUT 40
MAKE_BASE=TRUE

S0 Rail PGOOD (BJT Version)

=PP5V_S0_VMON 65 81
R8151 54.9K 1% 1/16W MF-LF 402
VMON_5V_DIV
5.0V Divider:1.07V
R8152 15.6K 1% 1/16W MF-LF 402
=PP3V3_S5_VMON 81
R8156 150K 1% 1/16W MF-LF 402
S0PGD_C
ALL_SYS_PWRGD 18 19 40 65 83
R8153 1K 5% 1/16W MF-LF 402 VMON_Q2_BASE
R8154 1K 5% 1/16W MF-LF 402 VMON_Q3_BASE
R8155 1K 5% 1/16W MF-LF 402 VMON_Q4_BASE
Q8150 ASMCC0179 DFN2015H4-8 353S2809 (Q1 Q2 Q3 Q4)
NC NC CRITICAL
=PP1V35_S3RS0_VMON 81 65
=PP3V3_S0_VMON 65 81
R8158 15.0K 1% 1/16W MF-LF 402
VMON_3V3_DIV
3V3 Divider:1.07V
R8159 7.15K 1% 1/16W MF-LF 402
S0PGD_BJT_GND_R
R8157 100 5% 1/16W MF-LF 402
Vbe 0.7V max @2mA
Vce(sat) 0.1V max @1mA
Q1 Vth 0.7~1V @Id 250uA

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V5MON: 2.015V-3.009V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V
keep R8171 DDRCPU 1.35V only

=PP3V3_S0_VMON NOSTUFF R8195 10 5% 1/16W MF-LF 402 (PP3V3_S0_VMON_P2)
C8162 0.1UF 20% 10V X7R-CERM 0402
C8160 0.1UF 20% 10V X7R-CERM 0402 S0PGOOD_ISL
=PP5V_S0_VMON 81 65
=PP1V35_S3RS0_VMON
R8160 6.04K 1% 1/16W MF-LF 402 (P5V_VMON divider 3.16V @4.5V)
=PP1V05_S0_VMON
R8170 10K 1% 1/16W MF-LF 402
R8172 6.04K 1% 1/16W MF-LF 402
P5V_DIV_VMON
R8161 15.0K 1% 1/16W MF-LF 402 (1V35_VMON divider 0.731V @1.31V)
R8171 12.4K 1% 1/16W MF-LF 402
R8173 15.0K 1% 1/16W MF-LF 402 (1V05_VMON divider 0.716V @1.02V)
P1V05_DIV_VMON
P1V05_VID_VMON
U8160 ISL88042IRTEZ TDFN (VDD, V2MON, V3MON, V4MON, GND, THRM_PAD, RST*)
353S2310 (CRIT) CRITICAL
1VMON_MR 65
S0PGOOD_ISL
R8162 330 5% 1/16W MF-LF 402
ALL_SYS_PWRGD
PP3V3_S0_VMON_P7 NOSTUFF R8197 100K 5% 1/16W MF-LF 402 VMON_MR
MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
R8196 10 5% 1/16W MF-LF 402 (PP3V3_S0_VMON_P7)
C8161 0.1UF 20% 10V X7R-CERM 0402
C8163 0.1UF 20% 10V X7R-CERM 0402
PM_SLP_S3_BUF_L
R8167 10K 5% 1/16W MF-LF 402
P1V5S0_PGOOD from U7810
P1V5S0_PGOOD 63 IN
R8168 100 5% 1/16W MF-LF 402
P1V05S0_PGOOD 61 IN
R8169 100 5% 1/16W MF-LF 402
S0PGOOD_ISL OUT 18 19 40 65 83

1V5 S0 "PGOOD" Delay

=PP3V3_S5_1V5PGOOD 81
R8136 23.7K 1% 1/16W MF-LF 402
C8134 2.2UF 10% 6.3V X5R 402
PM_1V5_PGD_L
R8139 2.0K 1% 1/16W MF-LF 402
PM_1V5_PGD_L_R
=PP1V5_S0_DIV 81
R8135 54.9K 1% 1/16W MF-LF 402
PM_P1V5_PGD_DIV
R8134 61.9K 1% 1/16W MF-LF 402
CRITICAL Q8151 DMB53D0UV SOT-563
Vgs:0.7V~1.0V
VBEon: 0.58~0.7V
1V5 Divider:0.75~0.85V
R8137 100 5% 1/16W MF-LF 402
DELAY_1V5S0_PGD 1 2 ALL_SYS_PWRGD OUT 18 19 40 65 83

CHGR VFRQ Generation

VFRQ High: Variable Frequency
VFRQ Low: Fix Frequency
=PP3V42_G3H_CHGR 81 56
R8131 100K 5% 1/16W MF-LF 402
CHGR_VFRQ OUT 56
Q8131 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
PM_SLP_S3_R_L 65

Unused PGOOD signals

=PP5V_S3_DDRREG 59 81
R8120 470K 5% 1/20W MF 201
=PP5V_S4_REG 60 81
R8165 470K 5% 1/16W MF-LF 402
DDRREG_PGOOD 59 IN
P5VS4_PGOOD 60 IN

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

=PP3V3_S4_WLAN 81
R8125 330K 5% 1/20W MF 201
SMC_WIFI_PWR_EN 40 IN
PM_WLAN_EN OUT 33
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_J45 SYNC_DATE=06/23/2013
PAGE TITLE: Power Control 1/ENABLE
Apple Inc.
DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
PAGE: 81 OF 119
SHEET: 65 OF 94

GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME up in the following order:

1) GPU_3.3V
2) IFPX IOVDD - 1.8V
3) GPUVCORE
4) FBVDDQ/GDDR5 1.35V
5) PEXVDD/Q OR IFPY IOVDD - 1.05V

EG_RAIL1_EN	P3V3GPU_EN	MAKE_BASE=TRUE	=P3V3GPU_EN	=P3V3GPU_MISC_EN
EG_RAIL2_EN	P1V8GPU_EN	MAKE_BASE=TRUE	=P1V8GPU_EN	
EG_RAIL3_EN	GPUVCORE_EN	MAKE_BASE=TRUE	=GPUVCORE_EN	
EG_RAIL4_EN	P1V35GPUFB_EN	MAKE_BASE=TRUE	=P1V35FB_EN	
EG_RAIL5_EN	P1V05_S0GPU_EN	MAKE_BASE=TRUE	=P1V05_GPU_EN	

NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

=PP3V3_S0_PWRCTL

R8200 R8201 R8202 100K 5% 1/20W ME 0201

=PP3V3_S0GPU_FET	MAKE_BASE=TRUE	GPU_PGOOD1	
TP_GPU_PGOOD2	MAKE_BASE=TRUE	GPU_PGOOD2	
GPUVCORE_PGOOD	MAKE_BASE=TRUE	GPU_PGOOD3	
GPUFB_PGOOD	MAKE_BASE=TRUE	GPU_PGOOD4	
P1V05_S0GPU_PGOOD	MAKE_BASE=TRUE	PM_ALL_GPU_PGOOD	

NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

PEG_R2D_P<0> — R8210 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<0>

PEG_R2D_P<5> — R8215 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<5>

PEG_R2D_P<3> — R8213 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<3>

PEG_R2D_P<7> — R8217 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<7>

PLACE R8210 - R8217 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_D2R_P<0> — R8220 82 5% 1/20W ME 0201 — NOSTUFF — PEG_D2R_N<0>

PEG_D2R_P<4> — R8224 82 5% 1/20W ME 0201 — NOSTUFF — PEG_D2R_N<4>

PEG_D2R_P<7> — R8227 82 5% 1/20W ME 0201 — NOSTUFF — PEG_D2R_N<7>

PLACE R8220 - R8227 CLOSE TO U1000

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
PAGE: 82 OF 119
SHEET: 66 OF 94

LCD PANEL INTERFACE (eDP)

C8350 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8351 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8352 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8353 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8354 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8355 9.1PF ±/-0.1PF C0G-CERM 0201 50V

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

R8300 0 5% 1/20W MF 0201

LCD_HPD
LCD_FSS
LCD_HPD_CONN

DP_INT_AUXCH_C_P C8328 0.1UF 10% 16V X5R-CERM 0201
DP_INT_AUXCH_C_N C8329 0.1UF 10% 16V X5R-CERM 0201

DP_INT_ML_C_P<0> C8320 0.1UF
DP_INT_ML_C_N<0> C8321 0.1UF
DP_INT_ML_C_P<1> C8322 0.1UF
DP_INT_ML_C_N<1> C8323 0.1UF
DP_INT_ML_C_P<2> C8324 0.1UF
DP_INT_ML_C_N<2> C8325 0.1UF
DP_INT_ML_C_P<3> C8326 0.1UF
DP_INT_ML_C_N<3> C8327 0.1UF

DP_INT_ML_F_P<0> DP_INT_ML_F_N<0> DP_INT_ML_F_P<1> DP_INT_ML_F_N<1> DP_INT_ML_F_P<2> DP_INT_ML_F_N<2> DP_INT_ML_F_P<3> DP_INT_ML_F_N<3>

150OHM-100MA-8.5GHZ DLP0NS
CRITICAL FL8300
CRITICAL FL8301
CRITICAL FL8302
CRITICAL FL8303

DP_INT_ML_P<0> DP_INT_ML_N<0> DP_INT_ML_P<1> DP_INT_ML_N<1> DP_INT_ML_P<2> DP_INT_ML_N<2> DP_INT_ML_P<3> DP_INT_ML_N<3>

CRITICAL
J8300
20525-130E-01
F-RT-SM

PPVOUT_S0_LCDBKLT
NC
518S0829

LCD_PWR_EN

CRITICAL
U8300
FPF1009
MFET-2X2-8IN
ON
VIN_1 VIN_2
VOUT_1 VOUT_2
GND THERM PAD

=PP5V_S0_LCD

C8309 0.1UF 10% 16V X7R-CERM 0402
C8311 0.1UF 10% 16V X7R-CERM 0402
C8312 10UF 20% 6.3V X5R 603

PP5VR3V3_SW_LCD_ISNS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

XW8320 SM

NC_ISNS_LCD_PANELN
NC_ISNS_LCD_PANELP

PP5VR3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL
L8300
FERR-220-OHM
0805

C8301 0.1UF 10% 16V X7R-CERM 0402
C8302 0.001UF 10% 50V X7R-CERM 0402
C8300 1000PF 10% 100V X7R 0603

PP5VR3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

LCD Panel HPD & AUX strapping

=PP3V3_S0_LCD
R8303 1M 5% 1/20W MF 201
DP_INT_AUX_N
LCD_HPD_CONN
DP_INT_AUX_P
R8301 1M 5% 1/20W MF 201
R8302 1M 5% 1/20W MF 201

R8311 1M 5% 1/20W MF 201
R8312 1M 5% 1/20W MF 201
R8313 1M 5% 1/20W MF 201
R8314 1M 5% 1/20W MF 201
R8315 1M 5% 1/20W MF 201
R8316 1M 5% 1/20W MF 201
R8317 1M 5% 1/20W MF 201
R8318 1M 5% 1/20W MF 201

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013
PAGE TITLE: eDP Display Connector
Apple Inc.
DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 83 OF 119
SHEET 67 OF 94

Page Notes

Power aliases required by this page:
- +PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

86 82	IN	PEG_R2D_C_P<0>	C8420 0.22UF GND_VOID=TRUE	PEG_R2D_P<0>		66 68 86
86 82	IN	PEG_R2D_C_N<0>	C8421 0.22UF GND_VOID=TRUE	PEG_R2D_N<0>		66 68 86
86 82	IN	PEG_R2D_C_P<1>	C8422 0.22UF GND_VOID=TRUE	PEG_R2D_P<1>		68 86
86 82	IN	PEG_R2D_C_N<1>	C8423 0.22UF GND_VOID=TRUE	PEG_R2D_N<1>		68 86
86 82	IN	PEG_R2D_C_P<2>	C8424 0.22UF GND_VOID=TRUE	PEG_R2D_P<2>		68 86
86 82	IN	PEG_R2D_C_N<2>	C8425 0.22UF GND_VOID=TRUE	PEG_R2D_N<2>		68 86
86 82	IN	PEG_R2D_C_P<3>	C8426 0.22UF GND_VOID=TRUE	PEG_R2D_P<3>		66 68 86
86 82	IN	PEG_R2D_C_N<3>	C8427 0.22UF GND_VOID=TRUE	PEG_R2D_N<3>		66 68 86
86 82	IN	PEG_R2D_C_P<4>	C8428 0.22UF GND_VOID=TRUE	PEG_R2D_P<4>		68 86
86 82	IN	PEG_R2D_C_N<4>	C8429 0.22UF GND_VOID=TRUE	PEG_R2D_N<4>		68 86
86 82	IN	PEG_R2D_C_P<5>	C8430 0.22UF GND_VOID=TRUE	PEG_R2D_P<5>		66 68 86
86 82	IN	PEG_R2D_C_N<5>	C8431 0.22UF GND_VOID=TRUE	PEG_R2D_N<5>		66 68 86
86 82	IN	PEG_R2D_C_P<6>	C8432 0.22UF GND_VOID=TRUE	PEG_R2D_P<6>		68 86
86 82	IN	PEG_R2D_C_N<6>	C8433 0.22UF GND_VOID=TRUE	PEG_R2D_N<6>		68 86
86 82	IN	PEG_R2D_C_P<7>	C8434 0.22UF GND_VOID=TRUE	PEG_R2D_P<7>		66 68 86
86 82	IN	PEG_R2D_C_N<7>	C8435 0.22UF GND_VOID=TRUE	PEG_R2D_N<7>		66 68 86

86 68	PEG_D2R_C_P<0>		C8455 0.22UF GND_VOID=TRUE	PEG_D2R_P<0>	OUT	66 82 86
86 68	PEG_D2R_C_N<0>		C8456 0.22UF GND_VOID=TRUE	PEG_D2R_N<0>	OUT	66 82 86
86 68	PEG_D2R_C_P<1>		C8457 0.22UF GND_VOID=TRUE	PEG_D2R_P<1>	OUT	82 86
86 68	PEG_D2R_C_N<1>		C8458 0.22UF GND_VOID=TRUE	PEG_D2R_N<1>	OUT	82 86
86 68	PEG_D2R_C_P<2>		C8459 0.22UF GND_VOID=TRUE	PEG_D2R_P<2>	OUT	82 86
86 68	PEG_D2R_C_N<2>		C8460 0.22UF GND_VOID=TRUE	PEG_D2R_N<2>	OUT	82 86
86 68	PEG_D2R_C_P<3>		C8461 0.22UF GND_VOID=TRUE	PEG_D2R_P<3>	OUT	82 86
86 68	PEG_D2R_C_N<3>		C8462 0.22UF GND_VOID=TRUE	PEG_D2R_N<3>	OUT	82 86
86 68	PEG_D2R_C_P<4>		C8463 0.22UF GND_VOID=TRUE	PEG_D2R_P<4>	OUT	66 82 86
86 68	PEG_D2R_C_N<4>		C8464 0.22UF GND_VOID=TRUE	PEG_D2R_N<4>	OUT	66 82 86
86 68	PEG_D2R_C_P<5>		C8465 0.22UF GND_VOID=TRUE	PEG_D2R_P<5>	OUT	82 86
86 68	PEG_D2R_C_N<5>		C8466 0.22UF GND_VOID=TRUE	PEG_D2R_N<5>	OUT	82 86
86 68	PEG_D2R_C_P<6>		C8467 0.22UF GND_VOID=TRUE	PEG_D2R_P<6>	OUT	82 86
86 68	PEG_D2R_C_N<6>		C8468 0.22UF GND_VOID=TRUE	PEG_D2R_N<6>	OUT	82 86
86 68	PEG_D2R_C_P<7>		C8469 0.22UF GND_VOID=TRUE	PEG_D2R_P<7>	OUT	66 82 86
86 68	PEG_D2R_C_N<7>		C8470 0.22UF GND_VOID=TRUE	PEG_D2R_N<7>	OUT	66 82 86

OMIT_TABLE

U8400
NV-GK107
BGA
(1 OF 10)

86 68 66	PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0> 68 86
86 68 66	PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0> 68 86
86 68	PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1> 68 86
86 68	PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1> 68 86
86 68	PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2> 68 86
86 68	PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2> 68 86
86 68 66	PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3> 68 86
86 68 66	PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3> 68 86
86 68	PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4> 68 86
86 68	PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4> 68 86
86 68 66	PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5> 68 86
86 68 66	PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5> 68 86
86 68	PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6> 68 86
86 68	PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6> 68 86
86 68 66	PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7> 68 86
86 68 66	PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7> 68 86
NC		AP20	PEX_RX8	PEX_TX8	AK20	NC
NC		AP21	PEX_RX8*	PEX_TX8*	AJ20	NC
NC		AN21	PEX_RX9	PEX_TX9	AH20	NC
NC		AM21	PEX_RX9*	PEX_TX9*	AG20	NC 81 76 75 74
NC		AN23	PEX_RX10	PEX_TX10	AK21	NC
NC		AM23	PEX_RX10*	PEX_TX10*	AJ21	NC
NC		AP23	PEX_RX11	PEX_TX11	AL22	NC
NC		AP24	PEX_RX11*	PEX_TX11*	AK22	NC
NC		AN24	PEX_RX12	PEX_TX12	AK23	NC
NC		AM24	PEX_RX12*	PEX_TX12*	AJ23	NC
NC		AN26	PEX_RX13	PEX_TX13	AH23	NC
NC		AM26	PEX_RX13*	PEX_TX13*	AG23	NC
NC		AP26	PEX_RX14	PEX_TX14	AK24	NC
NC		AP27	PEX_RX14*	PEX_TX14*	AJ24	NC
NC		AN27	PEX_RX15	PEX_TX15	AL25	NC
NC		AM27	PEX_RX15*	PEX_TX15*	AK25	NC
88 83 82	IN PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	
88 83 82	IN PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	
82 75	IN GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29	
75 68	OUT PEX_CLKREQ_L_R	AK12	PEX_CLKREQ*	PEX_SVDD_3V3	AG12	
NC		AJ11	PEX_WAKE*			

=PP3V3_GPU_VDD33

R8401 10K 1% 1/20W MF 201

PEX_CLKREQ_L_R 75 68

NOSTUFF R8402 200 1% 1/20W MF 201

PEX_TSTCLK_O_P 94

PEX_TSTCLK_O_N 94

R8400 0 MF 5% 1/20W 0201

GPU_RESET_L 82 75 IN

GPU_RESET_R_L

R8405 2.49K 1% 1/20W MF 201

GPU_PEX_TERMP

PP3V3_GPU_PEX_PLL_HVDD 76

SYNC_MASTER=D2_MLB
SYNC_DATE=07/31/2012

PAGE TITLE
KEPLER PCI-E

Apple Inc.

DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 84 OF 119
SHEET 68 OF 94

OMIT_TABLE

U8400
NV-GK107
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=PP1V35_GPU_FBVDDQ
81 73 72 69

AA27			H18
AA30			H19
AB27			H20
AB33			H21
AC27			H22
AD27			H23
AE27			H24
AF27			H8
AG27			H9
B13			L27
B16	FBVDDQ	FBVDDQ	M27
B19			N27
E13			P27
E16			R27
E19			T27
H10			T30
H11			T33
H12			V27
H13			W27
H14			W30
H15			W33
H16			Y27

=PP1V35_GPU_FBVDDQ
69 72 73 81

OMIT_TABLE

U8400
NV-GK107
BGA
(10 OF 10)

=PPVCORE_GPU
81 76 69

AA12			V17
AA14			V18
AA16			V20
AA19			V22
AA21			W12
AA23			W14
AB13			W16
AB15		VDD	W19
AB17			W21
AB18			W23
AB20			Y13
AB22			Y15
AC12			Y17
AC14			Y18
AC16			Y20
AC19			Y22
AC21			U1
AC23			U2
M12			U3
M14			U4
M16			U5
M19			U6
M21			U7
M23			U8
N13			V1
N15			V2
N17		VDD	V3
N18			V4
N20			V5
N22			V6
P12			V7
P14			V8
P16			W2
P19			W3
P21			W4
P23			W5
R13		XVDD	W7
R15			W8
R17			Y1
R18			Y2
R20			Y3
R22			Y4
T12			Y5
T14			Y6
T16			Y7
T19			Y8
T21			AA1
T23			AA2
U13			AA3
U15			AA4
U17			AA5
U18			AA6
U20			AA7
U22			AA8
V13			
V15			

=PPVCORE_GPU
69 76 81

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

GPU FB DE-COUPLING

=PP1V35_GPU_FBVDDQ
81 73 72 69

EDP = 6500 MA

C8525 20UF 20% 2V X6T-CERM 0402	C8526 20UF 20% 2V X6T-CERM 0402	C8527 20UF 20% 2V X6T-CERM 0402	C8528 20UF 20% 2V X6T-CERM 0402	C8501 10UF 20% 4V X6S-CERM 0402-1	C8502 10UF 20% 4V X6S-CERM 0402-1	C8503 10UF 20% 4V X6S-CERM 0402-1	C8504 10UF 20% 4V X6S-CERM 0402-1
C8505 4.7UF 20% 6.3V X6S 0402	C8506 4.7UF 20% 6.3V X6S 0402	C8507 4.7UF 20% 6.3V X6S 0402	C8508 4.7UF 20% 6.3V X6S 0402	C8509 4.7UF 20% 6.3V X6S 0402	C8510 4.7UF 20% 6.3V X6S 0402	C8511 1UF 20% 4V CERM-X6S 0201	C8512 1UF 20% 4V CERM-X6S 0201	C8513 1UF 20% 4V CERM-X6S 0201	C8514 1UF 20% 4V CERM-X6S 0201
C8515 0.1UF 10% 6.3V X6S 0201	C8518 0.1UF 10% 6.3V X6S 0201	C8519 0.1UF 10% 6.3V X6S 0201	C8520 0.1UF 10% 6.3V X6S 0201	C8521 0.1UF 10% 6.3V X6S 0201	C8522 0.1UF 10% 6.3V X6S 0201	C8523 0.1UF 10% 6.3V X6S 0201	C8524 0.1UF 10% 6.3V X6S 0201

GPU VCORE DE-COUPLING

=PPVCORE_GPU
81 76 69

EDP = 30 A

NOSTUFF C8561 47UF 20% 2V X6S 0805	NOSTUFF CRITICAL C8598 22UF 20% 4V X6S-CERM 0603	NOSTUFF CRITICAL C8599 22UF 20% 4V X6S-CERM 0603	CRITICAL C8562 20UF 20% 4V X5R-CERM 0402-2	CRITICAL C8563 20UF 20% 4V X5R-CERM 0402-2	CRITICAL C8564 20UF 20% 4V X5R-CERM 0402-2	CRITICAL C8565 20UF 20% 4V X5R-CERM 0402-2	NOSTUFF CRITICAL C8582 20UF 20% 4V X5R-CERM 0402-2	NOSTUFF CRITICAL C8583 20UF 20% 4V X5R-CERM 0402-2	C8566 10UF 20% 6.3V CERM 0402	C8567 10UF 20% 6.3V CERM 0402
CRITICAL C8545 20UF 20% 4V X5R-CERM 0402-2	CRITICAL C8546 20UF 20% 4V X5R-CERM 0402-2	CRITICAL C8547 20UF 20% 4V X5R-CERM 0402-2	CRITICAL C8548 20UF 20% 4V X5R-CERM 0402-2	NOSTUFF CRITICAL C8549 20UF 20% 4V X5R-CERM 0402-2	NOSTUFF CRITICAL C8550 20UF 20% 4V X5R-CERM 0402-2	NOSTUFF CRITICAL C8551 20UF 20% 4V X5R-CERM 0402-2				
C8568 10UF 20% 6.3V CERM 0402	C8569 10UF 20% 6.3V CERM 0402	C8570 10UF 20% 6.3V CERM 0402	C8571 10UF 20% 6.3V CERM 0402	C8572 10UF 20% 6.3V CERM 0402	C8573 10UF 20% 6.3V CERM 0402	C8574 10UF 20% 6.3V CERM 0402	C8575 10UF 20% 6.3V CERM 0402	C8576 10UF 20% 6.3V CERM 0402	C8577 10UF 20% 6.3V CERM 0402	
C8578 10UF 20% 6.3V CERM 0402	C8579 10UF 20% 6.3V CERM 0402	C8580 10UF 20% 6.3V CERM 0402	C8581 10UF 20% 6.3V CERM 0402	C8584 10UF 20% 6.3V CERM 0402	C8585 10UF 20% 6.3V CERM 0402	CRITICAL C8586 1UF 20% 4V CERM-X6S 0201	CRITICAL C8587 1UF 20% 4V CERM-X6S 0201	CRITICAL C8588 1UF 20% 4V CERM-X6S 0201	CRITICAL C8589 1UF 20% 4V CERM-X6S 0201	
CRITICAL C8590 1UF 20% 4V CERM-X6S 0201	C8591 0.1UF 10% 6.3V X6S 0201	C8592 0.1UF 10% 6.3V X6S 0201	C8593 0.1UF 10% 6.3V X6S 0201	C8594 0.1UF 10% 6.3V X6S 0201	C8595 0.1UF 10% 6.3V X6S 0201	C8596 1000PF 10% 16V X7R-CERM 0201	C8597 1000PF 10% 16V X7R-CERM 0201			

NOTE: ATLEAST 2 GND VIAS & 2 POWER VIAS PER CAP

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012

PAGE TITLE

KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 85 OF 119
SHEET 69 OF 94

NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

U8400
NV-GK107
BGA
(3 OF 10)
MEM INTERFACE A

FB_A0_DQ<0>	L28	FBA_D0	U30	FB_A0_CS_L	
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FB_A0_DQ<8>	J28	FBA_D8	V28	FB_A0_ABI_L	
FB_A0_DQ<9>	H29	FBA_D9	V29	FB_A0_A<8>	
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FB_A0_DQ<13>	E31	FBA_D13	V34	FB_A0_RESET_L	
FB_A0_DQ<14>	E32	FBA_D14	V33	FB_A0_CKE_L	
FB_A0_DQ<15>	F30	FBA_D15	Y32	FB_A0_CAS_L	
FB_A0_DQ<16>	C34	FBA_D16	AA31	FB_A1_CS_L	
FB_A0_DQ<17>	D32	FBA_D17	AA29	FB_A1_A<3>	
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FB_A0_DQ<25>	P32	FBA_D25	W31	FB_A1_A<8>	
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FB_A0_DQ<30>	L32	FBA_D30	Y33	FB_A1_CKE_L	
FB_A0_DQ<31>	L33	FBA_D31	V31	FB_A1_CAS_L	
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FB_A1_DQ<1>	AF29	FBA_D33			
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FB_A1_DQ<3>	AF28	FBA_D35	R31	FB_A0_CLK_N	
FB_A1_DQ<4>	AD30	FBA_D36	AB31	FB_A1_CLK_P	
FB_A1_DQ<5>	AD29	FBA_D37	AC31	FB_A1_CLK_N	
FB_A1_DQ<6>	AC29	FBA_D38			
FB_A1_DQ<7>	AD28	FBA_D39	P30	FB_A0_DBI_L<0>	
FB_A1_DQ<8>	AJ29	FBA_D40	F31	FB_A0_DBI_L<1>	
FB_A1_DQ<9>	AK29	FBA_D41	F34	FB_A0_DBI_L<2>	
FB_A1_DQ<10>	AJ30	FBA_D42	M32	FB_A0_DBI_L<3>	
FB_A1_DQ<11>	AK28	FBA_D43	AD31	FB_A1_DBI_L<0>	
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FB_A1_DQ<13>	AM31	FBA_D45	AM32	FB_A1_DBI_L<2>	
FB_A1_DQ<14>	AN29	FBA_D46	AF34	FB_A1_DBI_L<3>	
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FB_A1_DQ<16>	AN31	FBA_D48			
FB_A1_DQ<17>	AN32	FBA_D49			
FB_A1_DQ<18>	AP30	FBA_D50			
FB_A1_DQ<19>	AP32	FBA_D51			
FB_A1_DQ<20>	AM33	FBA_D52			
FB_A1_DQ<21>	AL31	FBA_D53			
FB_A1_DQ<22>	AK33	FBA_D54			
FB_A1_DQ<23>	AK32	FBA_D55			
FB_A1_DQ<24>	AD34	FBA_D56			
FB_A1_DQ<25>	AD32	FBA_D57			
FB_A1_DQ<26>	AC30	FBA_D58			
FB_A1_DQ<27>	AD33	FBA_D59			
FB_A1_DQ<28>	AF31	FBA_D60			
FB_A1_DQ<29>	AG34	FBA_D61			
FB_A1_DQ<30>	AG32	FBA_D62			
FB_A1_DQ<31>	AG33	FBA_D63			

FBA_DQS_RN0	M30	NC	
FBA_DQS_RN1	H30	NC	
FBA_DQS_RN2	E34	NC	
FBA_DQS_RN3	M34	NC	
FBA_DQS_RN4	AF30	NC	
FBA_DQS_RN5	AK31	NC	
FBA_DQS_RN6	AM34	NC	
FBA_DQS_RN7	AF32	NC	
FBA_DQS_WP0	M31	FB_A0_EDC<0>	
FBA_DQS_WP1	G31	FB_A0_EDC<1>	
FBA_DQS_WP2	E33	FB_A0_EDC<2>	
FBA_DQS_WP3	M33	FB_A0_EDC<3>	
FBA_DQS_WP4	AE31	FB_A1_EDC<0>	
FBA_DQS_WP5	AK30	FB_A1_EDC<1>	
FBA_DQS_WP6	AN33	FB_A1_EDC<2>	
FBA_DQS_WP7	AF33	FB_A1_EDC<3>	
FB_DLL_AVDD	K27	PP1V05_GPU_FB_DLL_AVDD	70
FBA_PLL_AVDD	U27	PP1V05_GPU_FB_PLL_AVDD	70
FBA_DEBUG	R28	GPU_FBA_DEBUG0	
FBA_DEBUG	AC28	GPU_FBA_DEBUG1	
FB_CAL_PD_VDDQ	J27	FB_CAL_PD_VDDQ	70
FB_CAL_PU_GND	H27	FB_CAL_PU_GND	70
FB_CAL_TERM_GND	H25	FB_CAL_TERM_GND	1
FB_CLAMP	E1	70 FB_CLAMP	
FBA_CMD_RFU	R32	NC	
FBA_CMD_RFU	AC32	NC	
FB_VDDQ_SENSE	F1	GPU_FBVDDQ_SENSE	
FB_GND_SENSE	F2	GPU_FBGND_SENSE	

FBA_CLK0	R30	FB_A0_CLK_P	FBA_CMD0	U30	FB_A0_CS_L
FBA_CLK0*	R31	FB_A0_CLK_N	FBA_CMD1	T31	FB_A0_A<3>
FBA_CLK1	AB31	FB_A1_CLK_P	FBA_CMD2	U29	FB_A0_A<2>
FBA_CLK1*	AC31	FB_A1_CLK_N	FBA_CMD3	R34	FB_A0_A<4>
			FBA_CMD4	R33	FB_A0_A<5>
FBA_DQM0	P30	FB_A0_DBI_L<0>	FBA_CMD5	U32	FB_A0_WE_L
FBA_DQM1	F31	FB_A0_DBI_L<1>	FBA_CMD6	U33	FB_A0_A<7>
FBA_DQM2	F34	FB_A0_DBI_L<2>	FBA_CMD7	U28	FB_A0_A<6>
FBA_DQM3	M32	FB_A0_DBI_L<3>	FBA_CMD8	V28	FB_A0_ABI_L
FBA_DQM4	AD31	FB_A1_DBI_L<0>	FBA_CMD9	V29	FB_A0_A<8>
FBA_DQM5	AL29	FB_A1_DBI_L<1>	FBA_CMD10	V30	FB_A0_A<0>
FBA_DQM6	AM32	FB_A1_DBI_L<2>	FBA_CMD11	U34	FB_A0_A<1>
FBA_DQM7	AF34	FB_A1_DBI_L<3>	FBA_CMD12	U31	FB_A0_RAS_L
			FBA_CMD13	V34	FB_A0_RESET_L
			FBA_CMD14	V33	FB_A0_CKE_L
			FBA_CMD15	V32	FB_A0_CAS_L
			FBA_CMD16	AA31	FB_A1_CS_L
			FBA_CMD17	AA29	FB_A1_A<3>
			FBA_CMD18	AA28	FB_A1_A<2>
			FBA_CMD19	AC34	FB_A1_A<4>
			FBA_CMD20	AC33	FB_A1_A<5>
			FBA_CMD21	AA32	FB_A1_WE_L
			FBA_CMD22	AA33	FB_A1_A<7>
			FBA_CMD23	Y28	FB_A1_A<6>
			FBA_CMD24	Y29	FB_A1_ABI_L
			FBA_CMD25	W31	FB_A1_A<8>
			FBA_CMD26	Y30	FB_A1_A<0>
			FBA_CMD27	AA34	FB_A1_A<1>
			FBA_CMD28	Y31	FB_A1_RAS_L
			FBA_CMD29	Y34	FB_A1_RESET_L
			FBA_CMD30	Y33	FB_A1_CKE_L
			FBA_CMD31	V31	FB_A1_CAS_L

FBA_DQS_RN0	M30	NC	
FBA_DQS_RN1	H30	NC	
FBA_DQS_RN2	E34	NC	
FBA_DQS_RN3	M34	NC	
FBA_DQS_RN4	AF30	NC	
FBA_DQS_RN5	AK31	NC	
FBA_DQS_RN6	AM34	NC	
FBA_DQS_RN7	AF32	NC	
FBA_DQS_WP0	M31	FB_A0_EDC<0>	
FBA_DQS_WP1	G31	FB_A0_EDC<1>	
FBA_DQS_WP2	E33	FB_A0_EDC<2>	
FBA_DQS_WP3	M33	FB_A0_EDC<3>	
FBA_DQS_WP4	AE31	FB_A1_EDC<0>	
FBA_DQS_WP5	AK30	FB_A1_EDC<1>	
FBA_DQS_WP6	AN33	FB_A1_EDC<2>	
FBA_DQS_WP7	AF33	FB_A1_EDC<3>	
FB_DLL_AVDD	K27	PP1V05_GPU_FB_DLL_AVDD	70
FBA_PLL_AVDD	U27	PP1V05_GPU_FB_PLL_AVDD	70
FBA_DEBUG	R28	GPU_FBA_DEBUG0	
FBA_DEBUG	AC28	GPU_FBA_DEBUG1	
FB_CAL_PD_VDDQ	J27	FB_CAL_PD_VDDQ	70
FB_CAL_PU_GND	H27	FB_CAL_PU_GND	70
FB_CAL_TERM_GND	H25	FB_CAL_TERM_GND	1
FB_CLAMP	E1	70 FB_CLAMP	
FBA_CMD_RFU	R32	NC	
FBA_CMD_RFU	AC32	NC	
FB_VDDQ_SENSE	F1	GPU_FBVDDQ_SENSE	
FB_GND_SENSE	F2	GPU_FBGND_SENSE	

94 72 70 FB_A0_RESET_L — R8650 10K 1% 1/20W MF 201

94 72 70 FB_A1_RESET_L — R8651 10K 1% 1/20W MF 201

FB_A0_CKE_L 70 72 94 — R8652 10K 1% 1/20W MF 201

FB_A1_CKE_L 70 72 94 — R8653 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 70 81

R8658 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8400.H26:8.4MM

FB_VREF 70 — PLACE_NEAR=U8400.H26:8.4MM

R8659 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8400.H26:8.4MM

NOSTUFF C8660 0.1UF 10% 6.3V X6S 0201

FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB 70 81

R8603 60.4 1% 1/20W MF 201

R8602 60.4 1% 1/20W MF 201

R8670 100 5% 1/20W MF 201

R8601 60.4 1% 1/20W MF 201 — PLACE_NEAR=U8400.H25:8.4MM

R8661 10K 1% 1/20W MF 201

PLACE CLOSE TO BGA

70 FB_CAL_PU_GND — R8604 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8400.H27:8.4MM

=PP1V35_GPU_S0_FB 70 81 — R8605 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8400.J27:8.4MM

FB_CAL_PD_VDDQ 70

R8671 100 5% 1/20W MF 201

OMIT_TABLE

U8400
NV-GK107
BGA
(4 OF 10)
MEM INTERFACE B

FB_B0_DQ<0>	G9	FBB_D0	D13	FB_B0_CS_L	
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FB_B0_DQ<2>	G8	FBB_D2	F14	FB_B0_A<2>	
FB_B0_DQ<3>	F9	FBB_D3	A12	FB_B0_A<4>	
FB_B0_DQ<4>	F11	FBB_D4	B12	FB_B0_A<5>	
FB_B0_DQ<5>	G11	FBB_D5	C14	FB_B0_WE_L	
FB_B0_DQ<6>	F12	FBB_D6	B14	FB_B0_A<7>	
FB_B0_DQ<7>	G12	FBB_D7	G15	FB_B0_A<6>	
FB_B0_DQ<8>	G6	FBB_D8	F15	FB_B0_ABI_L	
FB_B0_DQ<9>	F5	FBB_D9	E15	FB_B0_A<8>	
FB_B0_DQ<10>	E6	FBB_D10	D15	FB_B0_A<0>	
FB_B0_DQ<11>	F6	FBB_D11	A14	FB_B0_A<1>	
FB_B0_DQ<12>	F4	FBB_D12	D14	FB_B0_RAS_L	
FB_B0_DQ<13>	G4	FBB_D13	A15	FB_B0_RESET_L	
FB_B0_DQ<14>	E2	FBB_D14	B15	FB_B0_CKE_L	
FB_B0_DQ<15>	F3	FBB_D15	C17	FB_B0_CAS_L	
FB_B0_DQ<16>	C2	FBB_D16	D18	FB_B1_CS_L	
FB_B0_DQ<17>	D4	FBB_D17	E18	FB_B1_A<3>	
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FB_B0_DQ<23>	C5	FBB_D23	G18	FB_B1_A<6>	
FB_B0_DQ<24>	A11	FBB_D24	G17	FB_B1_ABI_L	
FB_B0_DQ<25>	C11	FBB_D25	F17	FB_B1_A<8>	
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FB_B0_DQ<28>	D8	FBB_D28	D17	FB_B1_RAS_L	
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FB_B0_DQ<30>	C8	FBB_D30	B17	FB_B1_CKE_L	
FB_B0_DQ<31>	B8	FBB_D31	E17	FB_B1_CAS_L	
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FB_B1_DQ<1>	G23	FBB_D33			
FB_B1_DQ<2>	E24	FBB_D34	D12	FB_B0_CLK_P	
FB_B1_DQ<3>	G24	FBB_D35	E12	FB_B0_CLK_N	
FB_B1_DQ<4>	D21	FBB_D36	E20	FB_B1_CLK_P	
FB_B1_DQ<5>	E21	FBB_D37	F20	FB_B1_CLK_N	
FB_B1_DQ<6>	G21	FBB_D38			
FB_B1_DQ<7>	F21	FBB_D39	E11	FB_B0_DBI_L<0>	
FB_B1_DQ<8>	G27	FBB_D40	E3	FB_B0_DBI_L<1>	
FB_B1_DQ<9>	D27	FBB_D41	A3	FB_B0_DBI_L<2>	
FB_B1_DQ<10>	G26	FBB_D42	C9	FB_B0_DBI_L<3>	
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FB_B1_DQ<13>	F29	FBB_D45	C30	FB_B1_DBI_L<2>	
FB_B1_DQ<14>	E30	FBB_D46	A24	FB_B1_DBI_L<3>	
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FB_B1_DQ<16>	A32	FBB_D48			
FB_B1_DQ<17>	C31	FBB_D49			
FB_B1_DQ<18>	C32	FBB_D50			
FB_B1_DQ<19>	B32	FBB_D51			
FB_B1_DQ<20>	D29	FBB_D52			
FB_B1_DQ<21>	A29	FBB_D53			
FB_B1_DQ<22>	C29	FBB_D54			
FB_B1_DQ<23>	B29	FBB_D55			
FB_B1_DQ<24>	B21	FBB_D56			
FB_B1_DQ<25>	C23	FBB_D57			
FB_B1_DQ<26>	A21	FBB_D58			
FB_B1_DQ<27>	C21	FBB_D59			
FB_B1_DQ<28>	B24	FBB_D60			
FB_B1_DQ<29>	C24	FBB_D61			
FB_B1_DQ<30>	B26	FBB_D62			
FB_B1_DQ<31>	C26	FBB_D63			

FB_B0_WCLK_P<0>	F8	FBB_WCK01	
FB_B0_WCLK_N<0>	E8	FBB_WCK01*	
FB_B0_WCLK_P<1>	A5	FBB_WCK23	
FB_B0_WCLK_N<1>	A6	FBB_WCK23*	
FB_B1_WCLK_P<0>	D24	FBB_WCK45	
FB_B1_WCLK_N<0>	D25	FBB_WCK45*	
FB_B1_WCLK_P<1>	B27	FBB_WCK67	
FB_B1_WCLK_N<1>	C27	FBB_WCK67*	
	D6	FBB_WCKB01	
	D7	FBB_WCKB01*	
	C6	FBB_WCKB23	
	B6	FBB_WCKB23*	
	F26	FBB_WCKB45	
	E26	FBB_WCKB45*	
	A26	FBB_WCKB67	
	A27	FBB_WCKB67*	

FBB_DQS_RN0	D9	NC	
FBB_DQS_RN1	E4	NC	
FBB_DQS_RN2	B2	NC	
FBB_DQS_RN3	A9	NC	
FBB_DQS_RN4	D22	NC	
FBB_DQS_RN5	D28	NC	
FBB_DQS_RN6	A30	NC	
FBB_DQS_RN7	B23	NC	
FBB_DQS_WP0	D10	FB_B0_EDC<0>	
FBB_DQS_WP1	D5	FB_B0_EDC<1>	
FBB_DQS_WP2	C3	FB_B0_EDC<2>	
FBB_DQS_WP3	B9	FB_B0_EDC<3>	
FBB_DQS_WP4	E23	FB_B1_EDC<0>	
FBB_DQS_WP5	E28	FB_B1_EDC<1>	
FBB_DQS_WP6	B30	FB_B1_EDC<2>	
FBB_DQS_WP7	A23	FB_B1_EDC<3>	
FBB_PLL_AVDD	H17	70 PP1V05_GPU_FB_PLL_AVDD	
FBB_DEBUG0	G14	GPU_FBB_DEBUG0	70
FBB_DEBUG1	G20	GPU_FBB_DEBUG1	70
FB_VREF	H26	FB_VREF	70
FBB_CMD_RFU0	C12	NC	
FBB_CMD_RFU1	C20	NC	

C8606 1UF 20% 4V CERM-X6S 0201

C8607 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_S0_FB 70 81

R8606 60.4 1% 1/20W MF 201

R8607 60.4 1% 1/20W MF 201

GPU_FBB_DEBUG0 70

GPU_FBB_DEBUG1 70

L8601
FERR-220-OHM-2A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD 70 — PP1V05_GPU_FB_PLL_AVDD 70
0603
CRITICAL
ESR = 0.050OHM

C8601 20UF 20% 2V X6T-CERM 0402

C8602 1UF 20% 4V CERM-X6S 0201

C8603 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

L8602
FERR-220-OHM-2A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD 76 70 81 — PP1V05_GPU_FB_DLL_AVDD 70
0603
CRITICAL
ESR = 0.050OHM

C8608 20UF 20% 2V X6T-CERM 0402

C8604 1UF 20% 4V CERM-X6S 0201

C8605 0.1UF 10% 6.3V X6S 0201

94 73 70 FB_B0_RESET_L — R8654 10K 1% 1/20W MF 201

94 73 70 FB_B1_RESET_L — R8655 10K 1% 1/20W MF 201

70 73 94 FB_B0_CKE_L — R8656 10K 1% 1/20W MF 201

70 73 94 FB_B1_CKE_L — R8657 10K 1% 1/20W MF 201

MEM VREFC & VREFD SWITCH

73 72 FB_SW_LEG

Q8665
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

GPU_ALT_VREF — 75

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=D2_MLB	SYNC_DATE=07/31/2012
PAGE TITLE	KEPLER FRAME BUFFER I/F
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 86 OF 119
	SHEET 70 OF 94

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GPU FB SUPPLY

VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ

GPIO(16)	VID1	VID0	FBVDD
	0	0	1.5V
	1	0	1.35V

GPU 1V05 SUPPLY

VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=D2_MLB	SYNC_DATE=07/31/2012
PAGE TITLE	1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 87 OF 119
	SHEET 71 OF 94

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

CK TERMINATION - A0

R8801 FB_A0_CLK_P 40.2 1% 1/20W MF 201 — FBA0_CK_MID — R8802 40.2 1% 1/20W MF 201 — FB_A0_CLK_N
PLACE_NEAR=U8800.J11:8.4MM
C8890 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8800.J12:8.4MM
PLACE_NEAR=U8800.J11:8.4MM

R8800 120 1% 1/20W MF 201
R8804 120 1% 1/20W MF 201
R8803 120 1% 1/20W MF 201

CK TERMINATION - A1

R8851 FB_A1_CLK_P 40.2 1% 1/20W MF 201 — FBA1_CK_MID — R8852 40.2 1% 1/20W MF 201 — FB_A1_CLK_N
PLACE_NEAR=U8850.J12:8.4MM
C8891 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8850.J11:8.4MM

U8800
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_A0_A<2>	H11	BA0/A2	
FB_A0_A<5>	K10	BA1/A5	
FB_A0_A<4>	K11	BA2/A4	
FB_A0_A<3>	H10	BA3/A3	
FB_A0_A<7>	K4	A8/A7	
FB_A0_A<1>	H5	A9/A1	
FB_A0_A<0>	H4	A10/A0	
FB_A0_A<6>	K5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	G12	CS*	
FB_A0_WE_L	L12	WE*	
FB_A0_CAS_L	L3	CAS*	
FB_A0_RAS_L	G3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=0)	
FB_A0_SEN	J10	SEN	
FB_A0_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	C2	EDC0	
FB_A0_EDC<1>	C13	EDC1	
FB_A0_EDC<2>	R13	EDC2	
FB_A0_EDC<3>	R2	EDC3	
FB_A0_WCLK_P<0>	D4	WCK01	
FB_A0_WCLK_N<0>	D5	WCK01*	
FB_A0_WCLK_P<1>	P4	WCK23	
FB_A0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A0_DBI_L<0>	
DBI1*	D13	FB_A0_DBI_L<1>	
DBI2*	P13	FB_A0_DBI_L<2>	
DBI3*	P2	FB_A0_DBI_L<3>	
DQ0	A4	FB_A0_DQ<0>	
DQ1	A2	FB_A0_DQ<1>	
DQ2	B4	FB_A0_DQ<2>	
DQ3	B2	FB_A0_DQ<3>	
DQ4	E4	FB_A0_DQ<4>	
DQ5	E2	FB_A0_DQ<5>	
DQ6	F4	FB_A0_DQ<6>	
DQ7	F2	FB_A0_DQ<7>	
DQ8	A11	FB_A0_DQ<8>	
DQ9	A13	FB_A0_DQ<9>	
DQ10	B11	FB_A0_DQ<10>	
DQ11	B13	FB_A0_DQ<11>	
DQ12	E11	FB_A0_DQ<12>	
DQ13	E13	FB_A0_DQ<13>	
DQ14	F11	FB_A0_DQ<14>	
DQ15	F13	FB_A0_DQ<15>	
DQ16	U11	FB_A0_DQ<16>	
DQ17	U13	FB_A0_DQ<17>	
DQ18	T11	FB_A0_DQ<18>	
DQ19	T13	FB_A0_DQ<19>	
DQ20	N11	FB_A0_DQ<20>	
DQ21	N13	FB_A0_DQ<21>	
DQ22	M11	FB_A0_DQ<22>	
DQ23	M13	FB_A0_DQ<23>	
DQ24	U4	FB_A0_DQ<24>	
DQ25	U2	FB_A0_DQ<25>	
DQ26	T4	FB_A0_DQ<26>	
DQ27	T2	FB_A0_DQ<27>	
DQ28	N4	FB_A0_DQ<28>	
DQ29	N2	FB_A0_DQ<29>	
DQ30	M4	FB_A0_DQ<30>	
DQ31	M2	FB_A0_DQ<31>	
NC	A5, J5, U5	NC	FB_A0_A<8>

OMIT_TABLE

U8850
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_A1_A<2>	H11	BA0/A2	
FB_A1_A<5>	K10	BA1/A5	
FB_A1_A<4>	K11	BA2/A4	
FB_A1_A<3>	H10	BA3/A3	
FB_A1_A<7>	K4	A8/A7	
FB_A1_A<1>	H5	A9/A1	
FB_A1_A<0>	H4	A10/A0	
FB_A1_A<6>	K5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	G12	CS*	
FB_A1_WE_L	L12	WE*	
FB_A1_CAS_L	L3	CAS*	
FB_A1_RAS_L	G3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=0)	
FB_A1_SEN	J10	SEN	
FB_A1_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	C2	EDC0	
FB_A1_EDC<1>	C13	EDC1	
FB_A1_EDC<2>	R13	EDC2	
FB_A1_EDC<3>	R2	EDC3	
FB_A1_WCLK_P<0>	D4	WCK01	
FB_A1_WCLK_N<0>	D5	WCK01*	
FB_A1_WCLK_P<1>	P4	WCK23	
FB_A1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A1_DBI_L<0>	
DBI1*	D13	FB_A1_DBI_L<1>	
DBI2*	P13	FB_A1_DBI_L<2>	
DBI3*	P2	FB_A1_DBI_L<3>	
DQ0	A4	FB_A1_DQ<0>	
DQ1	A2	FB_A1_DQ<1>	
DQ2	B4	FB_A1_DQ<2>	
DQ3	B2	FB_A1_DQ<3>	
DQ4	E4	FB_A1_DQ<4>	
DQ5	E2	FB_A1_DQ<5>	
DQ6	F4	FB_A1_DQ<6>	
DQ7	F2	FB_A1_DQ<7>	
DQ8	A11	FB_A1_DQ<8>	
DQ9	A13	FB_A1_DQ<9>	
DQ10	B11	FB_A1_DQ<10>	
DQ11	B13	FB_A1_DQ<11>	
DQ12	E11	FB_A1_DQ<12>	
DQ13	E13	FB_A1_DQ<13>	
DQ14	F11	FB_A1_DQ<14>	
DQ15	F13	FB_A1_DQ<15>	
DQ16	U11	FB_A1_DQ<16>	
DQ17	U13	FB_A1_DQ<17>	
DQ18	T11	FB_A1_DQ<18>	
DQ19	T13	FB_A1_DQ<19>	
DQ20	N11	FB_A1_DQ<20>	
DQ21	N13	FB_A1_DQ<21>	
DQ22	M11	FB_A1_DQ<22>	
DQ23	M13	FB_A1_DQ<23>	
DQ24	U4	FB_A1_DQ<24>	
DQ25	U2	FB_A1_DQ<25>	
DQ26	T4	FB_A1_DQ<26>	
DQ27	T2	FB_A1_DQ<27>	
DQ28	N4	FB_A1_DQ<28>	
DQ29	N2	FB_A1_DQ<29>	
DQ30	M4	FB_A1_DQ<30>	
DQ31	M2	FB_A1_DQ<31>	
NC	A5, J5, U5	NC	FB_A1_A<8>

OMIT_TABLE

U8800
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ
C8800 4.7UF 20% 6.3V X6S 0402
C8801 4.7UF 20% 6.3V X6S 0402
C8802 4.7UF 20% 6.3V X6S 0402
C8803 4.7UF 20% 6.3V X6S 0402
C8804 4.7UF 20% 6.3V X6S 0402
C8805 4.7UF 20% 6.3V X6S 0402
C8806 1UF 20% 4V CERM-X6S 0201
C8807 1UF 20% 4V CERM-X6S 0201
C8808 1UF 20% 4V CERM-X6S 0201
C8809 1UF 20% 4V CERM-X6S 0201
C8810 1UF 20% 4V CERM-X6S 0201
C8811 1UF 20% 4V CERM-X6S 0201
C8812 1UF 20% 4V CERM-X6S 0201
C8813 1UF 20% 4V CERM-X6S 0201
C8814 1UF 20% 4V CERM-X6S 0201
C8815 1UF 20% 4V CERM-X6S 0201
C8816 0.1UF 10% 6.3V X6S 0201
C8817 0.1UF 10% 6.3V X6S 0201
C8818 0.1UF 10% 6.3V X6S 0201
C8819 0.1UF 10% 6.3V X6S 0201
C8820 0.1UF 10% 6.3V X6S 0201
C8821 0.1UF 10% 6.3V X6S 0201
C8822 0.1UF 10% 6.3V X6S 0201
C8823 0.1UF 10% 6.3V X6S 0201
C8824 0.1UF 10% 6.3V X6S 0201
C8825 0.1UF 10% 6.3V X6S 0201

VDD
VSS
VDDQ
VSSQ
FB_A0_VREFC
FB_A0_VREFD
VREFC
VREFD

PLACE CLOSE TO U8800

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8830 549 1% 1/20W MF 201
FB_A0_VREFC
C8831 820PF 10% 25V X7R-CERM 0201
R8831 1.33K 1% 1/20W MF 201
R8834 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8800.J14:8.4MM
PLACE_NEAR=U8800.J13:8.4MM

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8832 549 1% 1/20W MF 201
FB_A0_VREFD
C8832 820PF 10% 25V X7R-CERM 0201
C8833 820PF 10% 25V X7R-CERM 0201
R8833 1.33K 1% 1/20W MF 201
R8835 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8800.U10:8.4MM
PLACE_NEAR=U8800.A10:8.4MM

U8850
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ
C8850 4.7UF 20% 6.3V X6S 0402
C8851 4.7UF 20% 6.3V X6S 0402
C8852 4.7UF 20% 6.3V X6S 0402
C8853 4.7UF 20% 6.3V X6S 0402
C8854 4.7UF 20% 6.3V X6S 0402
C8855 4.7UF 20% 6.3V X6S 0402
C8856 1UF 20% 4V CERM-X6S 0201
C8857 1UF 20% 4V CERM-X6S 0201
C8858 1UF 20% 4V CERM-X6S 0201
C8859 1UF 20% 4V CERM-X6S 0201
C8860 1UF 20% 4V CERM-X6S 0201
C8861 1UF 20% 4V CERM-X6S 0201
C8862 1UF 20% 4V CERM-X6S 0201
C8863 1UF 20% 4V CERM-X6S 0201
C8864 1UF 20% 4V CERM-X6S 0201
C8865 1UF 20% 4V CERM-X6S 0201
C8866 0.1UF 10% 6.3V X6S 0201
C8867 0.1UF 10% 6.3V X6S 0201
C8868 0.1UF 10% 6.3V X6S 0201
C8869 0.1UF 10% 6.3V X6S 0201
C8870 0.1UF 10% 6.3V X6S 0201
C8871 0.1UF 10% 6.3V X6S 0201
C8872 0.1UF 10% 6.3V X6S 0201
C8873 0.1UF 10% 6.3V X6S 0201
C8874 0.1UF 10% 6.3V X6S 0201
C8875 0.1UF 10% 6.3V X6S 0201

VDD
VSS
VDDQ
VSSQ
FB_A1_VREFC
FB_A1_VREFD
VREFC
VREFD

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8880 549 1% 1/20W MF 201
FB_A1_VREFC
C8881 820PF 10% 25V X7R-CERM 0201
R8881 1.33K 1% 1/20W MF 201
R8884 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8850.J14:8.4MM
PLACE_NEAR=U8850.J13:8.4MM

PLACE CLOSE TO U8850

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8882 549 1% 1/20W MF 201
FB_A1_VREFD
C8882 820PF 10% 25V X7R-CERM 0201
C8883 820PF 10% 25V X7R-CERM 0201
R8883 1.33K 1% 1/20W MF 201
R8885 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8850.U10:8.4MM
PLACE_NEAR=U8850.A10:8.4MM

SYNC_MASTER=D2_MLB	SYNC_DATE=07/31/2012
PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 88 OF 119
	SHEET 72 OF 94

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CK TERMINATION - B0

R8901 40.2 1% 1/20W MF 201 — FB_B0_CLK_P — FBB0_CK_MID — R8902 40.2 1% 1/20W MF 201 — FB_B0_CLK_N
PLACE_NEAR=U8900.J12:8.4MM
PLACE_NEAR=U8900.J11:8.4MM
C8990 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8900.J11:8.4MM

R8900 120 1% 1/20W MF 201
R8904 120 1% 1/20W MF 201
R8903 120 1% 1/20W MF 201

CK TERMINATION - B1

R8951 40.2 1% 1/20W MF 201 — FB_B1_CLK_P — FBB1_CK_MID — R8952 40.2 1% 1/20W MF 201 — FB_B1_CLK_N
PLACE_NEAR=U8950.J12:8.4MM
PLACE_NEAR=U8950.J11:8.4MM
C8991 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8950.J11:8.4MM

U8900

32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_B0_A<2>	H11	BA0/A2
FB_B0_A<5>	K10	BA1/A5
FB_B0_A<4>	K11	BA2/A4
FB_B0_A<3>	H10	BA3/A3
FB_B0_A<7>	K4	A8/A7
FB_B0_A<1>	H5	A9/A1
FB_B0_A<0>	H4	A10/A0
FB_B0_A<6>	K5	A11/A6
FB_B0_CKE_L	J3	CKE*
FB_B0_CLK_P	J12	CK
FB_B0_CLK_N	J11	CK*
FB_B0_CS_L	G12	CS*
FB_B0_WE_L	L12	WE*
FB_B0_CAS_L	L3	CAS*
FB_B0_RAS_L	G3	RAS*
FB_B0_ZQ	J13	ZQ
FB_B0_MF	J1	MF (MF=0)
FB_B0_SEN	J10	SEN
FB_B0_RESET_L	J2	RESET*
FB_B0_ABI_L	J4	ABI*
FB_B0_EDC<0>	C2	EDC0
FB_B0_EDC<1>	C13	EDC1
FB_B0_EDC<2>	R13	EDC2
FB_B0_EDC<3>	R2	EDC3
FB_B0_WCLK_P<0>	D4	WCK01
FB_B0_WCLK_N<0>	D5	WCK01*
FB_B0_WCLK_P<1>	P4	WCK23
FB_B0_WCLK_N<1>	P5	WCK23*

OMIT_TABLE

DBI0*	D2	FB_B0_DBI_L<0>
DBI1*	D13	FB_B0_DBI_L<1>
DBI2*	P13	FB_B0_DBI_L<2>
DBI3*	P2	FB_B0_DBI_L<3>
DQ0	A4	FB_B0_DQ<0>
DQ1	A2	FB_B0_DQ<1>
DQ2	B4	FB_B0_DQ<2>
DQ3	B2	FB_B0_DQ<3>
DQ4	E4	FB_B0_DQ<4>
DQ5	E2	FB_B0_DQ<5>
DQ6	F4	FB_B0_DQ<6>
DQ7	F2	FB_B0_DQ<7>
DQ8	A11	FB_B0_DQ<8>
DQ9	A13	FB_B0_DQ<9>
DQ10	B11	FB_B0_DQ<10>
DQ11	B13	FB_B0_DQ<11>
DQ12	E11	FB_B0_DQ<12>
DQ13	E13	FB_B0_DQ<13>
DQ14	F11	FB_B0_DQ<14>
DQ15	F13	FB_B0_DQ<15>
DQ16	U11	FB_B0_DQ<16>
DQ17	U13	FB_B0_DQ<17>
DQ18	T11	FB_B0_DQ<18>
DQ19	T13	FB_B0_DQ<19>
DQ20	N11	FB_B0_DQ<20>
DQ21	N13	FB_B0_DQ<21>
DQ22	M11	FB_B0_DQ<22>
DQ23	M13	FB_B0_DQ<23>
DQ24	U4	FB_B0_DQ<24>
DQ25	U2	FB_B0_DQ<25>
DQ26	T4	FB_B0_DQ<26>
DQ27	T2	FB_B0_DQ<27>
DQ28	N4	FB_B0_DQ<28>
DQ29	N2	FB_B0_DQ<29>
DQ30	M4	FB_B0_DQ<30>
DQ31	M2	FB_B0_DQ<31>
NC	A5	NC
NC	J5	NC
NC	U5	NC
FB_B0_A<8>		

U8950

32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

FB_B1_A<2>	H11	BA0/A2
FB_B1_A<5>	K10	BA1/A5
FB_B1_A<4>	K11	BA2/A4
FB_B1_A<3>	H10	BA3/A3
FB_B1_A<7>	K4	A8/A7
FB_B1_A<1>	H5	A9/A1
FB_B1_A<0>	H4	A10/A0
FB_B1_A<6>	K5	A11/A6
FB_B1_CKE_L	J3	CKE*
FB_B1_CLK_P	J12	CK
FB_B1_CLK_N	J11	CK*
FB_B1_CS_L	G12	CS*
FB_B1_WE_L	L12	WE*
FB_B1_CAS_L	L3	CAS*
FB_B1_RAS_L	G3	RAS*
FB_B1_ZQ	J13	ZQ
FB_B1_MF	J1	MF (MF=0)
FB_B1_SEN	J10	SEN
FB_B1_RESET_L	J2	RESET*
FB_B1_ABI_L	J4	ABI*
FB_B1_EDC<0>	C2	EDC0
FB_B1_EDC<1>	C13	EDC1
FB_B1_EDC<2>	R13	EDC2
FB_B1_EDC<3>	R2	EDC3
FB_B1_WCLK_P<0>	D4	WCK01
FB_B1_WCLK_N<0>	D5	WCK01*
FB_B1_WCLK_P<1>	P4	WCK23
FB_B1_WCLK_N<1>	P5	WCK23*

OMIT_TABLE

DBI0*	D2	FB_B1_DBI_L<0>
DBI1*	D13	FB_B1_DBI_L<1>
DBI2*	P13	FB_B1_DBI_L<2>
DBI3*	P2	FB_B1_DBI_L<3>
DQ0	A4	FB_B1_DQ<0>
DQ1	A2	FB_B1_DQ<1>
DQ2	B4	FB_B1_DQ<2>
DQ3	B2	FB_B1_DQ<3>
DQ4	E4	FB_B1_DQ<4>
DQ5	E2	FB_B1_DQ<5>
DQ6	F4	FB_B1_DQ<6>
DQ7	F2	FB_B1_DQ<7>
DQ8	A11	FB_B1_DQ<8>
DQ9	A13	FB_B1_DQ<9>
DQ10	B11	FB_B1_DQ<10>
DQ11	B13	FB_B1_DQ<11>
DQ12	E11	FB_B1_DQ<12>
DQ13	E13	FB_B1_DQ<13>
DQ14	F11	FB_B1_DQ<14>
DQ15	F13	FB_B1_DQ<15>
DQ16	U11	FB_B1_DQ<16>
DQ17	U13	FB_B1_DQ<17>
DQ18	T11	FB_B1_DQ<18>
DQ19	T13	FB_B1_DQ<19>
DQ20	N11	FB_B1_DQ<20>
DQ21	N13	FB_B1_DQ<21>
DQ22	M11	FB_B1_DQ<22>
DQ23	M13	FB_B1_DQ<23>
DQ24	U4	FB_B1_DQ<24>
DQ25	U2	FB_B1_DQ<25>
DQ26	T4	FB_B1_DQ<26>
DQ27	T2	FB_B1_DQ<27>
DQ28	N4	FB_B1_DQ<28>
DQ29	N2	FB_B1_DQ<29>
DQ30	M4	FB_B1_DQ<30>
DQ31	M2	FB_B1_DQ<31>
NC	A5	NC
NC	J5	NC
NC	U5	NC
FB_B1_A<8>		

VDD / VDDQ / VSS / VSSQ / VREFC / VREFD

=PP1V35_GPU_FBVDDQ

C8900 4.7UF 20% 6.3V X6S 0402
C8901 4.7UF 20% 6.3V X6S 0402
C8902 4.7UF 20% 6.3V X6S 0402
C8903 4.7UF 20% 6.3V X6S 0402
C8904 4.7UF 20% 6.3V X6S 0402
C8905 4.7UF 20% 6.3V X6S 0402
C8906 1UF 20% 4V CERM-X6S 0201
C8907 1UF 20% 4V CERM-X6S 0201
C8908 1UF 20% 4V CERM-X6S 0201
C8909 1UF 20% 4V CERM-X6S 0201
C8910 1UF 20% 4V CERM-X6S 0201
C8911 1UF 20% 4V CERM-X6S 0201
C8912 1UF 20% 4V CERM-X6S 0201
C8913 1UF 20% 4V CERM-X6S 0201
C8914 1UF 20% 4V CERM-X6S 0201
C8915 1UF 20% 4V CERM-X6S 0201
C8916 0.1UF 10% 6.3V X6S 0201
C8917 0.1UF 10% 6.3V X6S 0201
C8918 0.1UF 10% 6.3V X6S 0201
C8919 0.1UF 10% 6.3V X6S 0201
C8920 0.1UF 10% 6.3V X6S 0201
C8921 0.1UF 10% 6.3V X6S 0201
C8922 0.1UF 10% 6.3V X6S 0201
C8923 0.1UF 10% 6.3V X6S 0201
C8924 0.1UF 10% 6.3V X6S 0201
C8925 0.1UF 10% 6.3V X6S 0201

VDD: C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10
VSS: B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14
VDDQ: B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10
VSSQ: A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14
VREFC: J14
VREFD: A10, U10

FB_B0_VREFC
FB_B0_VREFD

PLACE CLOSE TO U8900

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
FB_B0_VREFC
R8930 549 1% 1/20W MF 201
C8931 820PF 10% 25V X7R-CERM 0201
R8931 1.33K 1% 1/20W MF 201
R8934 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8900.J14:8.4MM
PLACE_NEAR=U8900.J14:8.4MM
PLACE_NEAR=U8900.J14:8.4MM

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
FB_B0_VREFD
R8932 549 1% 1/20W MF 201
C8932 820PF 10% 25V X7R-CERM 0201
C8933 820PF 10% 25V X7R-CERM 0201
R8933 1.33K 1% 1/20W MF 201
R8935 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8900.U10:8.4MM
PLACE_NEAR=U8900.U10:8.4MM
PLACE_NEAR=U8900.A10:8.4MM

PLACE CLOSE TO U8950

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
FB_B1_VREFC
R8980 549 1% 1/20W MF 201
C8981 820PF 10% 25V X7R-CERM 0201
R8981 1.33K 1% 1/20W MF 201
R8984 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8950.J14:8.4MM
PLACE_NEAR=U8950.J14:8.4MM
PLACE_NEAR=U8950.J14:8.4MM

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
FB_B1_VREFD
R8982 549 1% 1/20W MF 201
C8982 820PF 10% 25V X7R-CERM 0201
C8983 820PF 10% 25V X7R-CERM 0201
R8983 1.33K 1% 1/20W MF 201
R8985 931 1% 1/20W MF 201
FB_SW_LEG
PLACE_NEAR=U8950.U10:8.4MM
PLACE_NEAR=U8950.U10:8.4MM
PLACE_NEAR=U8950.A10:8.4MM

SYNC_MASTER=D2_MLB
SYNC_DATE=07/31/2012

PAGE TITLE: GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER: 051-0675
SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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PD FOR AUX CHANNELS (FOR NVIDIA)

DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N
HDMI_EG_DDC_CLK_Q
HDMI_EG_DDC_DATA_Q

R9014 100K 1% 1/20W MF 201
R9013 100K 1% 1/20W MF 201
R9015 100K 1% 1/20W MF 201
R9016 100K 1% 1/20W MF 201
R9017 100K 1% 1/20W MF 201
R9018 100K 1% 1/20W MF 201
R9027 100K 1% 1/20W MF 201 NO STUFF
R9028 100K 1% 1/20W MF 201 NO STUFF

=PP3V3_GPU_VDD33
R9023 4.7K 1% 1/20W MF 201
R9024 4.7K 1% 1/20W MF 201

GPU_SSC_SMB_CLK R2
GPU_SSC_SMB_DAT R3
GPU_SMB_CLK T4
GPU_SMB_DAT T3
DPA_EG_DDC_CLK R4
DPA_EG_DDC_DATA R5
DPB_EG_DDC_CLK R7
DPB_EG_DDC_DATA R6

CRITICAL
L9004 330-OHM-1.2A 0603
=PP3V3_GPU_IFPX_PLLVDD
PP3V3_GPU_IFPX_PLLVDD
IFPX PLLVDD
C9010 10UF 20% 10V X6S-CERM 0603
C9011 1UF 10% 25V X6S-CERM 0402
C9012 0.1UF 20% 16V X6S-CERM 0201

PLACE BELOW GPU NEAR DISPLAY SECTION

C9013 10UF 20% 10V X6S-CERM 0603
C9019 4.7UF 20% 6.3V X6S 0603
C9015 1UF 20% 25V X6S-CERM 0402
C9016 1UF 20% 25V X6S-CERM 0402
C9017 0.1UF 20% 16V X6S-CERM 0201
C9018 0.1UF 20% 16V X6S-CERM 0201

L9005 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_IFPCD_IOVDD
PP1V05_GPU_IFPCD_IOVDD
IFP CD IOVDD
C9025 4.7UF 20% 6.3V X6S 0402
C9026 1UF 20% 4V CERM-X6S 0201
C9027 0.1UF 20% 16V X6S-CERM 0201
C9028 0.1UF 20% 16V X6S-CERM 0201
C9055 10UF 20% 4V X6S-CERM 0402-1
C9056 1UF 20% 4V CERM-X6S 0201
C9057 0.1UF 20% 16V X6S-CERM 0201
C9058 0.1UF 20% 16V X6S-CERM 0201

L9006 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD
IFP EF IOVDD
C9029 10UF 20% 4V X6S-CERM 0402-1
C9030 1UF 20% 4V CERM-X6S 0201
C9031 0.1UF 20% 16V X6S-CERM 0201
C9032 0.1UF 20% 16V X6S-CERM 0201
C9033 4.7UF 20% 6.3V X6S 0402
C9034 4.7UF 20% 6.3V X6S 0402
C9035 1UF 20% 4V CERM-X6S 0201
C9036 1UF 20% 4V CERM-X6S 0201
C9037 0.1UF 20% 16V X6S-CERM 0201
C9038 0.1UF 20% 16V X6S-CERM 0201

OMIT_TABLE
CRITICAL
U8400 NV-GK107 BGA (5 OF 10)

PP1V8_GPU_IFPA_IOVDD	AG8	IFPA_IOVDD	
PP3V3_GPU_IFPB_IOVDD	AG9	IFPB_IOVDD	
PP1V05_GPU_IFPCD_IOVDD	AF6	IFPC_IOVDD	
PP1V05_GPU_IFPCD_IOVDD	AG6	IFPD_IOVDD	
PP1V05_GPU_IFPEF_IOVDD	AC7	IFPE_IOVDD	
PP1V05_GPU_IFPEF_IOVDD	AC8	IFPF_IOVDD	
PP1V05_GPU_IFPAB_PLLVDD	AH8	IFPAB_PLLVDD	
NC	AJ8	IFPAB_RSET	
PP3V3_GPU_IFPX_PLLVDD	AF7	IFPC_PLLVDD	
IFPC_RSET	AF8	IFPC_RSET	
PP3V3_GPU_IFPX_PLLVDD	AG7	IFPD_PLLVDD	
IFPD_RSET	AN2	IFPD_RSET	
PP3V3_GPU_IFPX_PLLVDD	AB8	IFPEF_PLLVDD	
IFPEF_RSET	AD6	IFPEF_RSET	

IFPA_TXC	AM6	NC	
IFPA_TXC*	AN6	NC	
IFPA_TXD0	AP3	NC	
IFPA_TXD0*	AN3	NC	
IFPA_TXD1	AN5	NC	
IFPA_TXD1*	AM5	NC	
IFPA_TXD2	AL6	NC	
IFPA_TXD2*	AK6	NC	
IFPA_TXD3	AJ6	NC	
IFPA_TXD3*	AH6	NC	
IFPB_TXC	AJ9	NC	
IFPB_TXC*	AH9	NC	
IFPB_TXD4	AP6	NC	
IFPB_TXD4*	AP5	NC	
IFPB_TXD5	AM7	NC	
IFPB_TXD5*	AL7	NC	
IFPB_TXD6	AN8	NC	
IFPB_TXD6*	AM8	NC	
IFPB_TXD7	AK8	NC	
IFPB_TXD7*	AL8	NC	
IFPC_AUX_I2CW_SCL	AG3	HDMI_EG_DDC_CLK_Q	
IFPC_AUX_I2CW_SDA*	AG2	HDMI_EG_DDC_DATA_Q	
IFPC_L0	AK1	HDMI_EG_DATA_C_P<2>	
IFPC_L0*	AJ1	HDMI_EG_DATA_C_N<2>	
IFPC_L1	AJ3	HDMI_EG_DATA_C_P<1>	
IFPC_L1*	AJ2	HDMI_EG_DATA_C_N<1>	
IFPC_L2	AH3	HDMI_EG_DATA_C_P<0>	
IFPC_L2*	AH4	HDMI_EG_DATA_C_N<0>	
IFPC_L3	AG5	HDMI_EG_CLK_C_P	
IFPC_L3*	AG4	HDMI_EG_CLK_C_N	
IFPD_AUX_I2CX_SCL	AK3	DP_INT_EG_AUX_P	
IFPD_AUX_I2CX_SDA*	AK2	DP_INT_EG_AUX_N	
IFPD_L0	AM1	DP_INT_EG_ML_P<0>	
IFPD_L0*	AM2	DP_INT_EG_ML_N<0>	
IFPD_L1	AM3	DP_INT_EG_ML_P<1>	
IFPD_L1*	AM4	DP_INT_EG_ML_N<1>	
IFPD_L2	AL3	DP_INT_EG_ML_P<2>	
IFPD_L2*	AL4	DP_INT_EG_ML_N<2>	
IFPD_L3	AK4	DP_INT_EG_ML_P<3>	
IFPD_L3*	AK5	DP_INT_EG_ML_N<3>	
IFPE_AUX_I2CY_SCL	AB3	DP_TBTSNK0_EG_AUXCH_P	
IFPE_AUX_I2CY_SDA*	AB4	DP_TBTSNK0_EG_AUXCH_N	
IFPE_L0	AD2	DP_TBTSNK0_ML_C_P<0>	
IFPE_L0*	AD3	DP_TBTSNK0_ML_C_N<0>	
IFPE_L1	AD1	DP_TBTSNK0_ML_C_P<1>	
IFPE_L1*	AC1	DP_TBTSNK0_ML_C_N<1>	
IFPE_L2	AC2	DP_TBTSNK0_ML_C_P<2>	
IFPE_L2*	AC3	DP_TBTSNK0_ML_C_N<2>	
IFPE_L3	AC4	DP_TBTSNK0_ML_C_P<3>	
IFPE_L3*	AC5	DP_TBTSNK0_ML_C_N<3>	
IFPF_AUX_I2CZ_SCL	AF3	DP_TBTSNK1_EG_AUXCH_P	
IFPF_AUX_I2CZ_SDA*	AF2	DP_TBTSNK1_EG_AUXCH_N	
IFPF_L0	AE3	DP_TBTSNK1_ML_C_P<0>	
IFPF_L0*	AE4	DP_TBTSNK1_ML_C_N<0>	
IFPF_L1	AF4	DP_TBTSNK1_ML_C_P<1>	
IFPF_L1*	AF5	DP_TBTSNK1_ML_C_N<1>	
IFPF_L2	AD4	DP_TBTSNK1_ML_C_P<2>	
IFPF_L2*	AD5	DP_TBTSNK1_ML_C_N<2>	
IFPF_L3	AG1	DP_TBTSNK1_ML_C_P<3>	
IFPF_L3*	AF1	DP_TBTSNK1_ML_C_N<3>	

DDC MAPPING
I2CA -> IFPE
I2CB -> IFPF
I2CC -> SSC CLK GEN

DAC_AVDD	AG10	DACA_VDD	
		DACA_RED	AK9
		DACA_GREEN	AL10
		DACA_BLUE	AL9
	AP9	DACA_VREF	
	AP8	DACA_RSET	
		DACA_HSYNC	AM9
		DACA_VSYNC	AN9
		CEC	L3

R9000 10K 1% 1/20W MF 201

DISABLE PHY A & B FOR 15" MBP

PP1V8_GPU_IFPA_IOVDD — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V — R9001 10K 1% 1/20W MF 201
PP3V3_GPU_IFPB_IOVDD — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V — R9002 10K 1% 1/20W MF 201
PP1V05_GPU_IFPAB_PLLVDD — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V — R9003 10K 1% 1/20W MF 201
GPU_TESTMODE — R9008 10K 1% 1/20W MF 201

PD FOR RSET
IFPC_RSET — PLACE_NEAR=U8400.AF8:5MM — R9021 1K 1% 1/20W MF 201
IFPD_RSET — PLACE_NEAR=U8400.AN2:5MM — R9006 1K 1% 1/20W MF 201
IFPEF_RSET — PLACE_NEAR=U8400.AD6:5MM — R9007 1K 1% 1/20W MF 201

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_IFPB_IOVDD
- =PP1V8_GPU_IFPA_IOVDD
- =PP1V8_GPU_DPLL
- =PP1V05_GPU_DPLL
- =PP3V3_GPU_IFPX_PLLVDD
- =PP1V05_GPU_IFPFCD_IOVDD
- =PP1V05_GPU_IFPEF_IOVDD
- =PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- J31:YES
- D2:YES

PP1V05_GPU_SP_PLLVDD = PP1V05_GPU_VID_PLLVDD (MAKE_BASE=TRUE)

GPU_OSC_27M_XTAL_BUFFOUT_R — PLACE_NEAR=U8400.J4:8.4MM — R9011 10K 1% 1/20W MF 201
GPU_OSC_27M_SSIN — PLACE_NEAR=U8400.H1:8.4MM — R9012 10K 1% 1/20W MF 201

=PP3V3_GPU_VDD33
R9025 4.7K 1% 1/20W MF 201
R9026 4.7K 1% 1/20W MF 201

Q9000 DMN5L06VK-7 SOT-563
HDMI_EG_DDC_CLK
HDMI_EG_DDC_DATA

DDC 3.3V/5V LEVEL TRANSLATOR

Q9000 DMN5L06VK-7 SOT-563
HDMI_EG_DDC_DATA

OMIT_TABLE
U8400 NV-GK107 BGA (6 OF 10)

=PP3V3_GPU_MISC	J8		
=PP3V3_GPU_VDD33	K8		
	L8	VDD33	
	M8		
GPU_ROM_CS_L	H6	ROM_CS*	
GPU_ROM_SCLK	H4	ROM_SCLK	
GPU_ROM_SI	H5	ROM_SI	
GPU_ROM_SO	H7	ROM_SO	
R9009 40.2K 0.1% 1/20W MF 0201	J1	MULTI_STRAP_REF0_GND	
MULTI_STRAP_REF		MULTI_STRAP_REF0	
GPU_TESTMODE	AK11	TESTMODE	
PP1V05_GPU_SP_PLLVDD	AE8	SP_PLLVDD	
PP1V05_GPU_PLLVDD	AD8	PLLVDD	
PP1V05_GPU_VID_PLLVDD	AD7	VID_PLLVDD	
GPU_OSC_27M_XTALIN	H3	XTAL_IN	
GPU_OSC_27M_XTALOUT	H2	XTAL_OUT	
GPU_OSC_27M_XTAL_BUFFOUT_R	J4	XTAL_OUTBUFF	
GPU_OSC_27M_SSIN	H1	XTAL_SSIN	
GPU_MLS_STRAP0	J2	STRAP0	
GPU_MLS_STRAP1	J7	STRAP1	
GPU_MLS_STRAP2	J6	STRAP2	
GPU_MLS_STRAP3	J5	STRAP3	
GPU_MLS_STRAP4	J3	STRAP4	

GPIO0	P6	GPU_GPIO_0	
GPIO1	M3	GPU_GPIO_1	
GPIO2	L6	GPU_GPIO_2	
GPIO3	P5	GPU_GPIO_3	
GPIO4	P7	GPU_GPIO_4	
GPIO5	L7	GPU_GPIO_5	
GPIO6	M7	GPU_GPIO_6	
GPIO7	N8	GPU_GPIO_7	
GPIO8	M1	GPU_GPIO_8	
GPIO9	M2	GPU_GPIO_9	
GPIO10	L1	GPU_GPIO_10	
GPIO11	M5	GPU_GPIO_11	
GPIO12	N3	GPU_GPIO_12	
GPIO13	M4	GPU_GPIO_13	
GPIO14	N4	GPU_GPIO_14	
GPIO15	P2	GPU_GPIO_15	
GPIO16	R8	GPU_GPIO_16	
GPIO17	M6	GPU_GPIO_17	
GPIO18	R1	GPU_GPIO_18	
GPIO19	P3	GPU_GPIO_19	
GPIO20	P4	GPU_GPIO_20	
GPIO21	P1	GPU_GPIO_21	
JTAG_TCK	AM10	GPU_JTAG_TCK	
JTAG_TDI	AM11	GPU_JTAG_TDI	
JTAG_TDO	AP12	GPU_JTAG_TDO	
JTAG_TMS	AP11	GPU_JTAG_TMS	
JTAG_TRST*	AN11	GPU_JTAG_TRST_L	
THERMDP	K3	GPU_TDIODE_P	
THERMDN	K4	GPU_TDIODE_N	

GPU 3V3 VDD
=PP3V3_GPU_VDD33
C9040 10UF 20% 10V X6S-CERM 0603
C9041 1UF 10% 25V X6S-CERM 0402
C9042 1UF 10% 25V X6S-CERM 0402
C9043 0.1UF 20% 16V X6S-CERM 0201
C9044 0.1UF 20% 16V X6S-CERM 0201
=PP3V3_GPU_MISC
C9045 4.7UF 20% 6.3V X6S 0402
C9046 4.7UF 20% 6.3V X6S 0402
C9049 0.1UF 20% 16V X6S-CERM 0201
C9050 0.1UF 20% 16V X6S-CERM 0201

GPU PLL VDD
L9007 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_PEX_PLLVDD
PP1V05_GPU_PLLVDD
C9051 20UF 20% 2V X6T-CERM 0402
C9052 1UF 20% 4V CERM-X6S 0201
C9053 0.1UF 20% 16V X6S-CERM 0201
C9054 0.1UF 20% 16V X6S-CERM 0201

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012
PAGE TITLE: KEPLER EDP/DP/GPIO
Apple Inc.
DRAWING NUMBER: 051-0675 SIZE: D
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GPIOs

74	GPU_GPIO_0	GFXIMVP_VID<4>	77
74	GPU_GPIO_1	GFXIMVP_VID<3>	77
74	GPU_GPIO_2	GFXIMVP_PSI_R_L	77
74	GPU_GPIO_3	EG_LCD_PWR_EN	75 79
74	GPU_GPIO_4	EG_BKLT_EN	75 79
74	GPU_GPIO_5	GFXIMVP_VID<1>	77
74	GPU_GPIO_6	GFXIMVP_VID<2>	77
74	GPU_GPIO_7	FB_CLAMP_TOGGLE_REQ_L	75 79
74	GPU_GPIO_8	SMC_GFX_OVERTEMP_R_L	75
74	GPU_GPIO_9	SMC_GFX_THROTTLE_R_L	75
74	GPU_GPIO_10	GPU_ALT_VREF	70
74	GPU_GPIO_11	GFXIMVP_VID<0>	77
74	GPU_GPIO_12	HDMI_EG_HPD	79
74	GPU_GPIO_13	GFXIMVP_VID<5>	77

GPIOs

74	GPU_GPIO_14	DP_EXTA_CA_DET_EG	79
74	GPU_GPIO_15	DP_EXTB_CA_DET_EG	79
74	GPU_GPIO_16	FBVDD_ALTVO	71 75
74	GPU_GPIO_17	DP_INT_EG_HPD	79
74	GPU_GPIO_18	DP_TBTSNK0_HPD_EG	79
74	GPU_GPIO_19	DP_TBTSNK1_HPD_EG	79
74	GPU_GPIO_20	NC_GPU_GPIO_20_RSVD (NO_TEST=TRUE)	
74	GPU_GPIO_21	NC_GPU_GPIO_21_RSVD (NO_TEST=TRUE)	

68 PEX_CLKREQ_L_R — R9195 0 5% 1/20W MF 0201 — EG_CLKREQ_IN_L (OUT 79)

GPU internal Temp isolation

=PP3V3_GPU_VDD33

R9155 10K 5% 1/20W MF 201

Q9102 DMN5L06VK-7 SOT-563

GPU_SMB_DAT (BI 74) — GPU_SMB_DAT_R (BI 43)

R9180 0 5% 1/20W MF 0201 NOSTUFF

=PP3V3_GPU_VDD33

R9154 10K 5% 1/20W MF 201

Q9102 DMN5L06VK-7 SOT-563

GPU_SMB_CLK (OUT 74) — GPU_SMB_CLK_R (IN 43)

R9181 0 5% 1/20W MF 0201 NOSTUFF

Unused signals

TP_GPU_JTAG_TCK (MAKE_BASE=TRUE)	GPU_JTAG_TCK	74
TP_GPU_JTAG_TDI (MAKE_BASE=TRUE)	GPU_JTAG_TDI	74
TP_GPU_JTAG_TDO (MAKE_BASE=TRUE)	GPU_JTAG_TDO	74
	GPU_JTAG_TMS	74
	GPU_JTAG_TRST_L	74

NOSTUFF R9151 10K 5% 1/20W MF 201

NOSTUFF R9158 10K 5% 1/20W MF 201

NOSTUFF GC6 SUPPORT R9153 10K 5% 1/20W MF 201

Note: PU to non GPU_S0 3v3 source

81 79 =PP3V3_S0_DPMUX_UC

79 75 FB_CLAMP_TOGGLE_REQ_L

CONFIG STRAPS - MLPS

=PP3V3_GPU_VDD33	R9100	45.3K 1% 1/20W MF 201	GPU_MLS_STRAP0 (OUT 74)	
=PP3V3_GPU_VDD33	R9101	5.62K 1% 1/20W MF 201	NOSTUFF	
=PP3V3_GPU_VDD33	R9108	3.24K 1% 1/20W MF 201	GPU_MLS_STRAP4 (OUT 74)	NOSTUFF
=PP3V3_GPU_VDD33	R9109	45.3K 1% 1/20W MF 201		
=PP3V3_GPU_VDD33	R9102	3.24K 1% 1/20W MF 201	GPU_MLS_STRAP1 (OUT 74)	NOSTUFF
=PP3V3_GPU_VDD33	R9103	45.3K 1% 1/20W MF 201		
=PP3V3_GPU_VDD33	R9110	3.24K 1% 1/20W MF 201	GPU_ROM_SI (OUT 74 75)	NOSTUFF
=PP3V3_GPU_VDD33	R9111	25.5K 1% 1/20W MF 201		OMIT_TABLE
=PP3V3_GPU_VDD33	R9104	10K 1% 1/20W MF 201	GPU_MLS_STRAP2 (OUT 74)	OMIT_TABLE
=PP3V3_GPU_VDD33	R9105	30K 1% 1/20W MF 201		
=PP3V3_GPU_VDD33	R9112	10K 1% 1/20W MF 201	GPU_ROM_SO (OUT 74 75)	NOSTUFF
=PP3V3_GPU_VDD33	R9113	10K 1% 1/20W MF 201		
=PP3V3_GPU_VDD33	R9106	20K 1% 1/20W MF 201	GPU_MLS_STRAP3 (OUT 74)	
=PP3V3_GPU_VDD33	R9107	5.62K 1% 1/20W MF 201	NOSTUFF	
=PP3V3_GPU_VDD33	R9114	24.9K 1% 1/20W MF 201	GPU_ROM_SCLK (OUT 74 75)	OMIT_TABLE
=PP3V3_GPU_VDD33	R9115	34.8K 1% 1/20W MF 201		OMIT_TABLE

Straps for GK107. GF108 support has been removed.

GPU GC6 ROM

=PP3V3_GPU_VDD33

GPU_ROM_SI (74 75) — R9123 33 5% 1/20W MF 201 — GPU_ROM:YES — GPU_ROM_SI_R — SI

GPU_ROM_SO (74 75) — R9126 33 5% 1/20W MF 201 — GPU_ROM:YES — GPU_ROM_SO_R — SO

U9101 1MBIT USON MX25L1005CMI-12G CRITICAL

OMIT_TABLE

VCC 8 — SCLK 6 — CS* 1 — WP* 3 — HOLD* 7 — THRM PAD 9 — GND 4

R9120 10K 5% 1/20W MF 201 GPU_ROM:YES

R9121 0 5% 1/20W MF 0201 GPU_ROM:YES

C9121 0.1UF 10% 6.3V X6S 0201 GPU_ROM:YES

GPU_ROM_SCLK_R — R9124 33 5% 1/20W MF 201 — GPU_ROM_SCLK (74 75) GPU_ROM:YES

GPU_ROM_CS_L_R — R9125 33 5% 1/20W MF 201 — GPU_ROM_CS_L (74) GPU_ROM:YES

GPU_ROM_WP_L

NO STUFF R9122 0 5% 1/20W MF 0201

STRAP NOTES:

CURRENTLY STUFFED FOR GF108a/GK107-GTX

STUFF R9104 FOR THICK DIE

STUFF R9105 FOR THIN DIE

GPU overtemp masking

=PP3V3_GPU_VDD33 — R9152 10K 5% 1/20W MF 201 — SMC_GFX_OVERTEMP_Q

=PP3V3_GPU_VDD33 — =PP3V3_S5_SMC — R9156 0 5% 1/20W MF 0201 — R9157 NOSTUFF 0 5% 1/20W MF 0201

VOLTAGE=3.3V MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.1 MM

PP3V3_GPU_OVERTEMP

U9102 74LVC1G08 SOT891

SMC_GFX_OVERTEMP_Q — 2 — 08 — 4 — SMC_GFX_OVERTEMP (OUT 75 40 41)

1 — NC — 5 — 3 — NC

Q9101 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 (D 3, G 1, S 2)

75 SMC_GFX_OVERTEMP_R_L

GPU_RESET_L (68 82 IN)

GPU XTAL 27 MHZ

GPU_OSC_27M_XTALIN (OUT 74 94) — GPU_OSC_27M_XTALOUT (IN 74 94)

CRITICAL Y9100 2.50X2.00MM-SM 27MHZ-30PPM-18PF-60OHM

C9100 18PF 5% 25V NP0-C0G-CERM 0201 — NC — NC — C9101 18PF 5% 25V NP0-C0G-CERM 0201

=PP3V3_GPU_VDD33

R9196 10K 5% 1/20W MF 201 — R9197 10K 5% 1/20W MF 201

75 SMC_GFX_OVERTEMP_R_L — R9198 0 NO STUFF — SMC_GFX_OVERTEMP (OUT 40 41 75)

75 SMC_GFX_THROTTLE_R_L — R9199 0 — SMC_GFX_THROTTLE_L (IN 40)

EG_LCD_PWR_EN (OUT 75 79)

EG_BKLT_EN (OUT 75 79)

FBVDD_ALTVO (OUT 71 75)

R9192 10K — R9193 10K — R9194 10K — R9190 10K NO STUFF — R9191 10K NOSTUFF

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0230	1	RES,MF,24.9KOHM,1,1/20W,0201,1%	R9111		FB_2G_HYNIX_A_DIE
118S0280	1	RES,MF,30.1KOHM,1,1/20W,0201,1%	R9111		FB_2G_ELPIDA
118S0013	1	RES, 10KOHM, 0201,1%	R9111		FB_2G_HYNIX_29nm
118S0409	1	RES, 4.99 KOHM, 0201,1%	R9111		FB_2G_ELPIDA_29nm
118S0105	1	RES, 15.0 KOHM, 0201,1%	R9111		FB_4G_HYNIX
118S0013	1	RES, 10KOHM, 0201,1%	R9104		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201, 1%	R9115		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201,1%	R9105		GK107:GT
118S0013	1	RES, 10KOHM, 0201,1%	R9114		GK107:GT

Die Rev	Strap
Hynix	0x4
ELPIDA	0x5
Hynix_29nm	0x1
ELPIDA_29nm	0x0

SYNC_MASTER=D2_MLB — SYNC_DATE=07/31/2012

PAGE TITLE: KEPLER GPIOS,CLK & STRAPS

Apple Inc.

DRAWING NUMBER 051-0675 — SIZE D

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Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

GPU SP PLLVDD

=PP1V05_GPU_PEX_PLLVDD → L9204 FERR-220-OHM-2A (0603, CRITICAL, ESR = 0.050OHM) → PP1V05_GPU_SP_PLLVDD 74

MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.05V

C9230 20UF 20% 2V X6T-CERM 0402
C9231 4.7UF 20% 6.3V X6S 0402
C9232 1UF 20% 4V CERM-X6S 0201
C9233 1UF 20% 4V CERM-X6S 0201
C9234 0.1UF 20% 16V X6S-CERM 0201
C9235 0.1UF 20% 16V X6S-CERM 0201
C9236 0.1UF 20% 16V X6S-CERM 0201
C9237 0.1UF 20% 16V X6S-CERM 0201

XW9201 SM — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V → GND_GPU_SP_PLLVDD

U8400 NV-GK107 BGA (2 OF 10)

OMIT_TABLE

NC	P8	PEX_IOVDD	AG19
NC	AC6	PEX_IOVDD	AG21
NC	AJ28	PEX_IOVDD	AG22
NC	AJ4	PEX_IOVDD	AG24
NC	AJ5	PEX_IOVDD	AH21
NC	AL11	PEX_IOVDD	AH25
NC	C15		
NC	D19		
NC	D20	PEX_IOVDDQ	AG13
NC	D23	PEX_IOVDDQ	AG15
NC	D26	PEX_IOVDDQ	AG16
NC	H31	PEX_IOVDDQ	AG18
NC	T8	PEX_IOVDDQ	AG25
NC	V32	PEX_IOVDDQ	AH15
		PEX_IOVDDQ	AH18
		PEX_IOVDDQ	AH26
		PEX_IOVDDQ	AH27
		PEX_IOVDDQ	AJ27
		PEX_IOVDDQ	AK27
		PEX_IOVDDQ	AL27
		PEX_IOVDDQ	AM28
		PEX_IOVDDQ	AN28
C16	GND_OPT		
W32	GND_OPT		
L4	VDD_SENSE		
L5	GND_SENSE		
L2	BUFRST*	PEX_PLL_HVDD	AH12
		PEX_PLLVDD	AG26

=PP1V05_GPU_PEX_IOVDD 70 76 81

=PP1V05_GPU_PEX_IOVDD 70 76 81

=PPVCORE_GPU 81 69

R9210 100 5% 1/20W MF 201

GPUVCORE_SENSE_P 93 77 OUT

GPUVCORE_SENSE_N 93 77 OUT

GPU_BUFRSTN

R9211 100 5% 1/20W MF 201

R9200 10K 1% 1/20W MF 201

PEX_PLLVDD

MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V

PP1V05_GPU_PEX_PLLVDD → R9203 0 5% 1/10W MF-LF 603 → =PP1V05_GPU_PEX_PLLVDD 74 76 81

C9226 4.7UF 20% 6.3V X6S 0402
C9227 4.7UF 20% 6.3V X6S 0402
C9228 1UF 20% 4V CERM-X6S 0201
C9229 0.1UF 10% 6.3V X6S 0201

XW9202 SM — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V → GND_GPU_PEX_PLLVDD

PEX_PLL_HVDD

MIN_LINE_WIDTH=0.8 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V

PP3V3_GPU_PEX_PLL_HVDD 68 → R9202 0 5% 1/16W MF-LF 402 → =PP3V3_GPU_VDD33 68 74 75 81

C9222 4.7UF 20% 6.3V X6S 0402
C9223 4.7UF 20% 6.3V X6S 0402
C9224 1UF 20% 4V CERM-X6S 0201
C9225 0.1UF 10% 6.3V X6S 0201

XW9203 SM — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V → GND_GPU_PEX_PLL_HVDD

PEX IOVDD & PEX IOVDDQ

PLACE XW9200 & XW9204 CLOSE TO C9203

XW9204 SM 1 2 P1V05_GPU_PEX_IOVDD_SNS_P OUT 71 93
PLACE_NEAR=C9203.1:2MM

=PP1V05_GPU_PEX_IOVDD 81 76 70

C9203 20UF 20% 2V X6T-CERM 0402
C9204 20UF 20% 2V X6T-CERM 0402
C9205 4.7UF 20% 6.3V X6S 0402

XW9200 SM 1 2 P1V05_GPU_PEX_IOVDD_SNS_N OUT 71 93
PLACE_NEAR=C9203.2:2MM

C9215 10UF 20% 4V X6S-CERM 0402-1
C9216 1UF 20% 4V CERM-X6S 0201
C9217 0.1UF 10% 6.3V X6S 0201
C9218 100PF 5% 25V NP0-CERM 0201

C9209 10UF 20% 4V X6S-CERM 0402-1
C9210 1UF 20% 4V CERM-X6S 0201
C9211 0.1UF 10% 6.3V X6S 0201
C9219 100PF 5% 25V NP0-CERM 0201

EDP = 2000 MA

C9200 20UF 20% 2V X6T-CERM 0402
C9201 20UF 20% 2V X6T-CERM 0402
C9202 4.7UF 20% 6.3V X6S 0402

C9212 10UF 20% 4V X6S-CERM 0402-1
C9213 1UF 20% 4V CERM-X6S 0201
C9214 0.1UF 10% 6.3V X6S 0201
C9221 100PF 5% 25V NP0-CERM 0201

C9206 10UF 20% 4V X6S-CERM 0402-1
C9207 1UF 20% 4V CERM-X6S 0201
C9208 0.1UF 10% 6.3V X6S 0201
C9220 100PF 5% 25V NP0-CERM 0201

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OMIT_TABLE

AG11	GND	GND	AK7
A2			AL12
A33			AL14
AA13			AL15
AA15			AL17
AA17			AL18
AA18			AL2
AA20			AL20
AA22			AL21
AB12			AL23
AB14			AL24
AB16			AL26
AB19			AL28
AB2			AL30
AB21			AL32
AB23			AL33
AB28			AL5
AB30			AM13
AB32			AM16
AB5			AM19
AB7			AM22
AC13			AM25
AC15			AN1
AC17			AN10
AC18			AN13
AC20			AN16
AC22			AN19
AE2			AN22
AE28			AN25
AE30			AN30
AE32			AN34
AE33			AN4
AE5			AN7
AE7			AP2
AH10			AP33
AH13			B1
AH16			B10
AH19			B22
AH2			B25
AH22			B28
AH24			B31
AH28			B34
AH29			B4
AH30			B7
AH32			C10
AH33			C13
AH5			C19
AH7			C22
AJ7			C25
AK10			C28

U8400 NV-GK107 BGA (9 OF 10)

OMIT_TABLE

C7	GND	GND	N7
D2			P13
D31			P15
D33			P17
E10			P18
E22			P20
E25			P22
E5			R12
E7			R14
F28			R16
F7			R19
G10			R21
G13			R23
G16			T13
G19			T15
G2			T17
G22			T18
G25			T2
G28			T20
G3			T22
G30			T28
G32			T32
G33			T5
G5			T7
G7			U12
K2			U14
K28			U16
K30			U19
K32			U21
K33			U23
K5			V12
K7			V14
M13			V16
M15			V19
M17			V21
M18			V23
M20			W13
M22			W15
N12			W17
N14			W18
N16			W20
N19			W22
N2			W28
N21			Y12
N23			Y14
N28			Y16
N30			Y19
N32			Y21
N33			Y23
N5			AH11

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012

PAGE TITLE: KEPLER PEX PWR/GNDS

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D
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=PPVIN_S0_GFXIMVP

=PP5V_S0_GFXIMVP

PLACE_NEAR=U9300.25:1mm
C9302 1UF 10% 25V X6S-CERM 0402

R9301 1 5% 1/20W MF 201
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V
PP5V_S0_GFXIMVP_VDD

PLACE_NEAR=U9300.16:1mm
C9301 1UF 10% 25V X6S-CERM 0402

R9300 10 5% 1/20W MF 201
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=12.8V
PPVIN_S0_GFXIMVP_R

PLACE_NEAR=U9300.17:1mm
C9300 0.22UF 10% 25V X7R 0402

(GND_GFXIMVP_AGND)

R9340 147K 1% 1/20W MF 201
R9318 30.1K 1% 1/20W MF 201

U9300 ISL62882C TQFN
VDD 16 VCCP 25 VIN 17
RBIAS 3 353S3679
NTC 5
PGOOD 1
VR_TT* 4
CLK_EN* 40
VID0 31
VID1 32
VID2 33
VID3 34
VID4 35
VID5 36
VID6 37
PSI* 2
DPRSLPVR 39
VR_ON 38
VW 6
COMP 7
FB2 9
FB 8
VSEN 12
RTN 13
IMON 18
THRM PAD 41
BOOT2 30
UGATE2 29
PHASE2 28
LGATE2 26
VSSP2 27
ISEN2 10
BOOT1 19
UGATE1 20
PHASE1 21
LGATE1A 23
LGATE1B 24
VSSP1 22
ISEN1 11
ISUM+ 15
ISUM- 14

Line Width & DIDT on all DIDT nets

GFXIMVP_RBIAS
GFXIMVP_NTC
GPUVCORE_PGOOD
GFXIMVP_VR_TT_L
GFXIMVP_VID<0>
GFXIMVP_VID<1>
GFXIMVP_VID<2>
GFXIMVP_VID<3>
GFXIMVP_VID<4>
GFXIMVP_VID<5>
GFXIMVP_VID<6>
GFXIMVP_PSI_L
GFXIMVP_DPSLP_EN
=GPUVCORE_EN
GFXIMVP_VW
GFXIMVP_COMP
GFXIMVP_FB2
GFXIMVP_FB
CKPLUS_WAIVE=PdifPr_badTerm
GPUVCORE_SENSE_P
GPUVCORE_SENSE_N
GFXIMVP6_IMON
GFXIMVP_BOOT2
GFXIMVP_UGATE2
GFXIMVP_PHASE2
GFXIMVP_LGATE2
GFXIMVP_VSSP2
GFXIMVP_ISEN2
GFXIMVP_BOOT1
GFXIMVP_UGATE1
GFXIMVP_PHASE1
GFXIMVP_LGATE1
NC
GFXIMVP_VSSP1
GFXIMVP_ISEN1
GFXIMVP_ISUMP
GFXIMVP_ISUMN_R

R9314 5.11K 1% 1/20W MF 201
C9319 1000PF 10% 16V X7R-CERM 0201
C9316 560PF 10% 16V X7R-CERM 0201 GFXIMVP_COMP_R
C9317 330PF 10% 16V X7R-CERM 0201
C9318 22PF 5% 50V NP0-C0G-CERM 0201 NOSTUFF
R9313 8.06K 1% 1/20W MF 201
R9316 49.9 1% 1/20W MF 201 GFXIMVP_FB_SNS_R
R9315 301 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
C9340 3300PF 10% 16V X7R-CERM 0201
NO_XNET_CONNECTION=TRUE
NOSTUFF R9317 49.9 1% 1/20W MF 201
GFXIMVP_FB_GND_R
NOSTUFF C9341 5600PF 10% 16V CERM 201

NO_XNET_CONNECTION=TRUE C9315 1000PF 10% 16V X7R-CERM 0201
NO_XNET_CONNECTION=TRUE C9314 1000PF 10% 16V X7R-CERM 0201
NO_XNET_CONNECTION=TRUE R9312 10K 1% 1/20W MF 201
C9313 0.1UF 10% 6.3V X6S 0201
NO_XNET_CONNECTION=TRUE
XW9300 SM
PLACE_NEAR=U9300.41:1mm

GND_GFXIMVP_AGND
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM DIDT=TRUE
GFXIMVP_BOOT2_R
C9330 0.22UF 10% 16V CERM 402
R9330 0 5% 1/10W MF-LF 603

Q9330 IRF6802SDTRPBF DIRECTFET-SA
CRITICAL L9330 0.2UH-20%-24A-0.003OHM PIMB063T-SM
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.05V
PPVCORE_S0_GFX_PH2
NCNC
CRITICAL Q9331 649135PBF DIRECTFET_S3C 376S1011
PLACE_NEAR=Q9331.3:1mm
XW9330 SM

R9398 0.00075 1% 1W MF 0612
GFXIMVP_ISNS2_P
GFXIMVP_ISNS2_N
R9331 10K 1% 1/20W MF 201
R9333 1K 1% 1/20W MF 201
R9334 1.00 1% 1/20W MF-LF 0201
GFXIMVP_ISUMN
GFXIMVP_ISUMP
R9332 10K 1% 1/20W MF 201
C9331 0.22UF 20% 6.3V X6S-CERM 0201
GFXIMVP_ISNS1_N

25A max per phase
=PPVCORE_S0_GFX_REG
CRITICAL C9361 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9362 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9363 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9364 330UF-6MOHM 20% 2.0V POLY-TANT D1ST-ECGLT-COMBO

C9328 0.001UF 10% 50V X7R-CERM 0402
C9327 0.001UF 10% 50V X7R-CERM 0402
CRITICAL C9326 680UF 20% 2V POLY-TANT CASE-D2E-SM
CRITICAL C9320 680UF 20% 2V POLY-TANT CASE-D2E-SM
CRITICAL C9321 680UF 20% 2V POLY-TANT CASE-D2E-SM
CRITICAL C9322 680UF 20% 2V POLY-TANT CASE-D2E-SM
C9323 1UF 10% 25V X6S-CERM 0402
C9324 1UF 10% 25V X6S-CERM 0402
CRITICAL C9325 150UF 20% 16V TANT SM

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM DIDT=TRUE
GFXIMVP_BOOT1_R
C9365 0.22UF 10% 16V CERM 402
R9360 0 5% 1/10W MF-LF 603

Q9330 IRF6802SDTRPBF DIRECTFET-SA
CRITICAL L9360 0.2UH-20%-24A-0.003OHM PIMB063T-SM
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.05V
PPVCORE_S0_GFX_PH1
NCNC
CRITICAL Q9361 649135PBF DIRECTFET_S3C 376S1011
PLACE_NEAR=Q9361.3:1mm
XW9331 SM

R9399 0.00075 1% 1W MF 0612
GFXIMVP_ISNS1_P
GFXIMVP_ISNS1_N
R9361 10K 1% 1/20W MF 201
R9363 1K 1% 1/20W MF 201
R9364 1.00 1% 1/20W MF-LF 0201
GFXIMVP_ISUMN
GFXIMVP_ISUMP
R9362 10K 1% 1/20W MF 201
C9366 0.22UF 20% 6.3V X6S-CERM 0201
GFXIMVP_ISNS2_N

R9310 1.24K 1% 1/20W MF 201
C9310 5600PF 10% 16V CERM 201
GFXIMVP_ISUMN
NOSTUFF C9312 0.1UF 10% 6.3V X6S 0201
GFXIMVP_ISUMP_C
NOSTUFF R9311 1.15K 1% 1/20W MF 201
C9311 0.1UF 10% 6.3V X6S 0201

GPU VCORE VID STRAPS
DEFAULT = 0.9 V

=PP3V3_S0_GFX3V3BIAS
NOSTUFF R9343 10K 1% 1/20W MF 201 GFXIMVP_VID<0>
NOSTUFF R9344 10K 1% 1/20W MF 201 GFXIMVP_VID<1>
NOSTUFF R9345 10K 1% 1/20W MF 201 GFXIMVP_VID<2>
NOSTUFF R9346 10K 1% 1/20W MF 201 GFXIMVP_VID<3>
NOSTUFF R9347 10K 1% 1/20W MF 201 GFXIMVP_VID<4>
NOSTUFF R9348 10K 1% 1/20W MF 201 GFXIMVP_VID<5>
NOSTUFF R9349 10K 1% 1/20W MF 201 GFXIMVP_VID<6>
NOSTUFF R9350 10K 1% 1/20W MF 201
R9351 10K 1% 1/20W MF 201
R9352 10K 1% 1/20W MF 201
R9353 10K 1% 1/20W MF 201
NOSTUFF R9354 10K 1% 1/20W MF 201
NOSTUFF R9355 10K 1% 1/20W MF 201
R9356 10K 1% 1/20W MF 201

Stuff option for GPIO control
R9381 = PSI Control
R9382 = VID6 control (old connection)
R9382 = DPSLP Control

GFXIMVP_PSI_R_L
R9381 0 5% 1/20W MF 0201 GFXIMVP_PSI_L
NOSTUFF R9382 0 5% 1/20W MF 0201 GFXIMVP_VID<6>
NOSTUFF R9383 0 5% 1/20W MF 0201 GFXIMVP_DPSLP_EN

=PP3V3_S0_GFX3V3BIAS
NOSTUFF R9370 499 1% 1/20W MF 201 GFXIMVP_VR_TT_L
R9371 100K 5% 1/20W MF 201 GFXIMVP_PSI_L
NOSTUFF R9374 100K 5% 1/20W MF 201 GFXIMVP_DPSLP_EN
NOSTUFF R9372 100K 5% 1/20W MF 201
R9373 100K 5% 1/20W MF 201

Do not config
PSI_L = HIGH & DPSLP_EN = HIGH

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012
PAGE TITLE: GFX IMVP VCore Regulator
Apple Inc.
DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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Wire-to-Board (Micro-coax) Connector

CRITICAL

J9500
20525-130E-01
F-RT-SM

NO_XNET_CONNECTION=TRUE
BP9501 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9502 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9505 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9506 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9503 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9504 SM
BEAD-PROBE TP 1

87 13 IN USB3_EXTB_R2D_C_P
87 13 IN USB3_EXTB_R2D_C_N
C9501 1 2 0.1UF GND_VOID=TRUE 10% 16V X5R-CERM 0201
C9502 1 2 0.1UF GND_VOID=TRUE 10% 16V X5R-CERM 0201
87 83 13 OUT USB3_EXTB_D2R_P
87 83 13 OUT USB3_EXTB_D2R_N

87 83 13 BI USB_EXTB_P
87 83 13 BI USB_EXTB_N
87 83 USB3_EXTB_R2D_P GND_VOID=TRUE
87 83 USB3_EXTB_R2D_N GND_VOID=TRUE
GND_VOID=TRUE
GND_VOID=TRUE
94 74 IN HDMI_EG_DATA_C_P<0> GND_VOID=TRUE
94 74 IN HDMI_EG_DATA_C_N<0> GND_VOID=TRUE
94 74 IN HDMI_EG_DATA_C_P<1> GND_VOID=TRUE
94 74 IN HDMI_EG_DATA_C_N<1> GND_VOID=TRUE
94 74 IN HDMI_EG_DATA_C_P<2> GND_VOID=TRUE
94 74 IN HDMI_EG_DATA_C_N<2> GND_VOID=TRUE
94 74 IN HDMI_EG_CLK_C_P
94 74 IN HDMI_EG_CLK_C_N
88 83 20 OUT USB3_SD_D2R_P GND_VOID=TRUE
88 83 20 OUT USB3_SD_D2R_N GND_VOID=TRUE
88 83 20 IN USB3_SD_R2D_C_P GND_VOID=TRUE
88 83 20 IN USB3_SD_R2D_C_N GND_VOID=TRUE

31 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 33 34 35 36 37 38 39 40 41 32

518S0829

Board-to-Board (Flex) Connector

CRITICAL

J9510
20590-032E-25
F-ST-SM

Note. Pin1 in symbol is different to 516S0853 in J15.

34 33 2 1 4 3 6 5 8 7 10 9 12 11 14 13 16 15 18 17 20 19 22 21 24 23 26 25 28 27 30 29 32 31 36 35

GND

79 20 OUT HDMI_HPD
83 18 OUT USB_EXTB_OC_L
83 18 13 IN SD_PWR_EN
83 20 OUT RIO_SDCONN_STATE_CHANGE_L
81 =PP3V3_S3_RIO
81 =PP3V3_S4_RIO
43 IN I2C_HDMIRDRV_SCL
43 BI I2C_HDMIRDRV_SDA

PM_SLP_S3_BUF_L IN 50 64 65 79 83
PM_SLP_S4_L IN 12 21 33 37 40 65 83
HDMI_EG_DDC_CLK IN 74
HDMI_EG_DDC_DATA BI 74

81 PP1V5R1V35_S0_RIO
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
81 =PP5V_S4_RIO

C9510 1 2 0.1uF 20% 10V CERM 402
C9511 1 2 0.1uF 20% 10V CERM 402

516S1106

RIO_PWR:1V5
R9535 0 2 1 5% 1/10W MF-LF 402
81 =PP1V5_S0_RIO

RIO_PWR:1V35
R9534 0 2 1 5% 1/10W MF-LF 402
81 =PP1V35_S0_RIO

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
RIO Connectors

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
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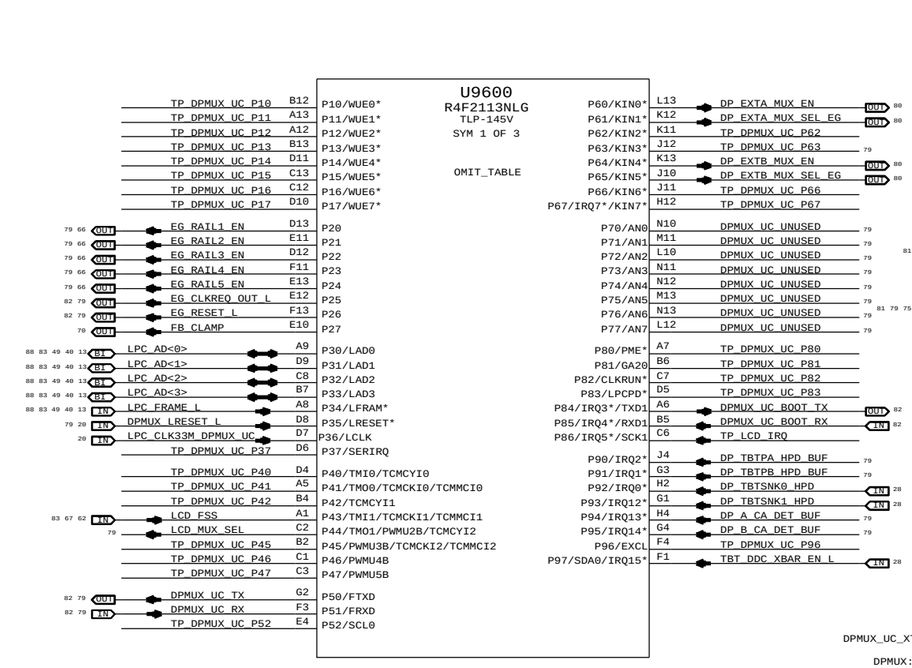
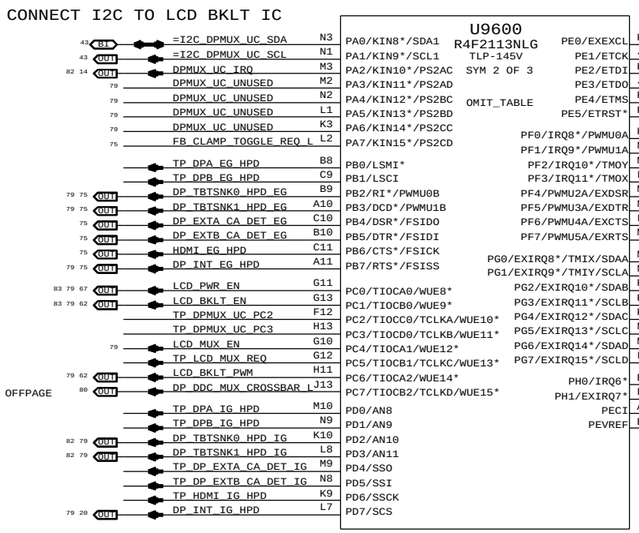
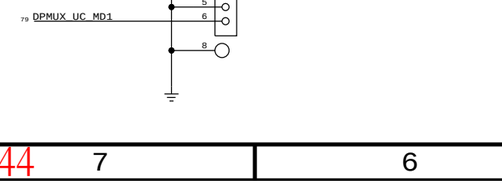
SHEET 78 OF 94

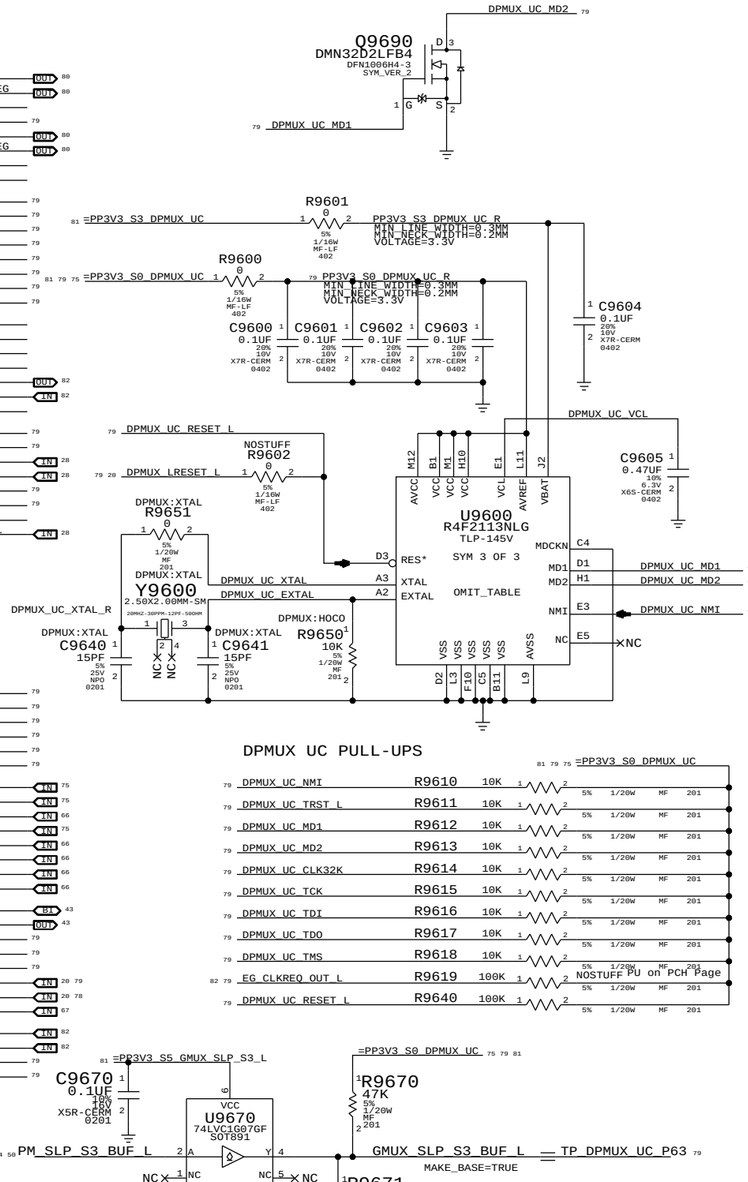


CONNECT I2C TO LCD BKLT IC



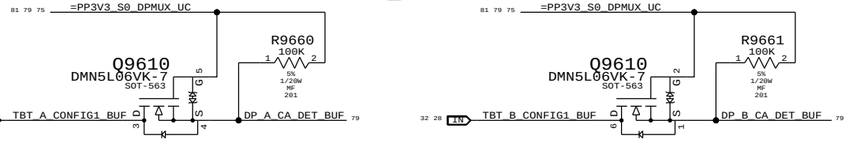


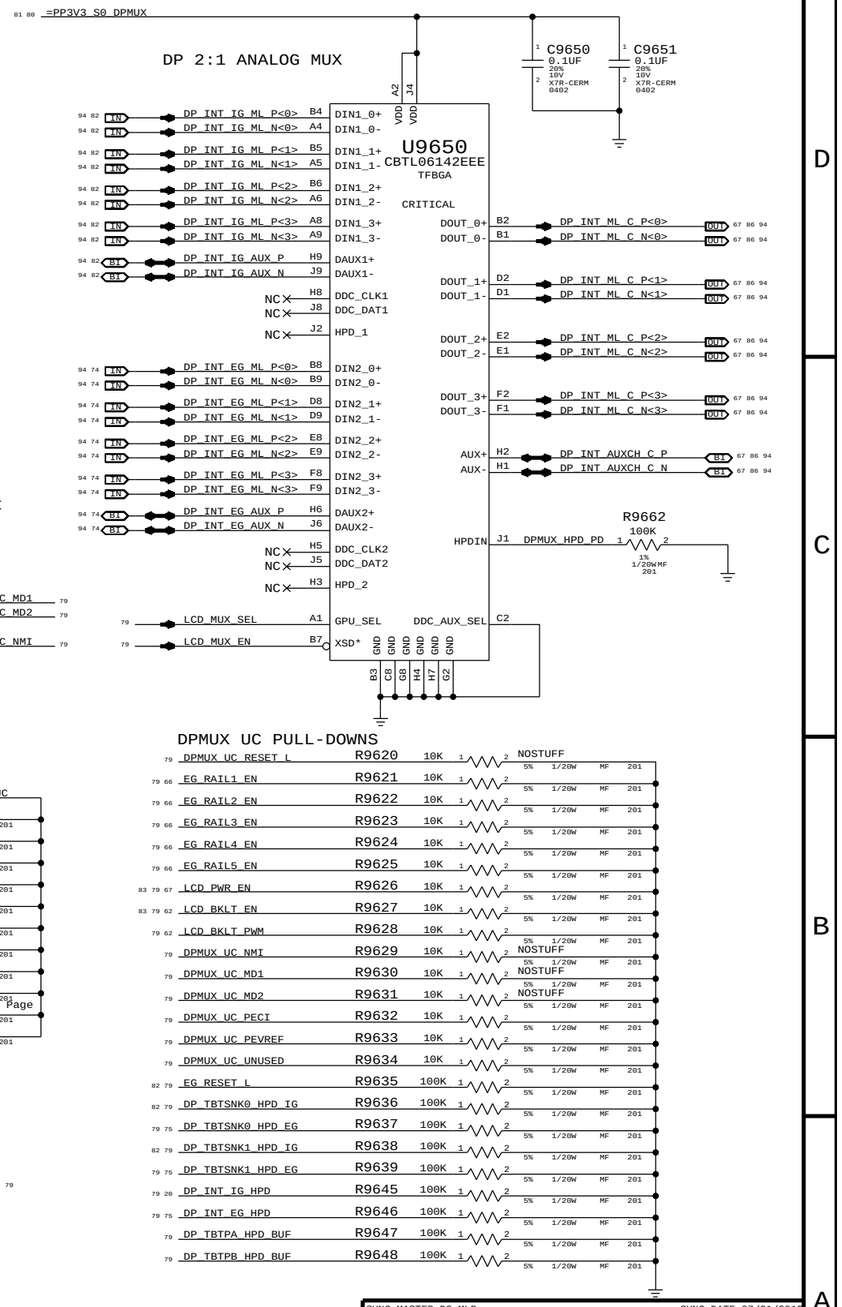
DPMUX UC DEBUG HEADER



DPMUX UC PULL-UPS

CA_DET ISOLATION





DPMUX UC PULL-DOWNS

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012

PAGE TITLE: eDP Mux

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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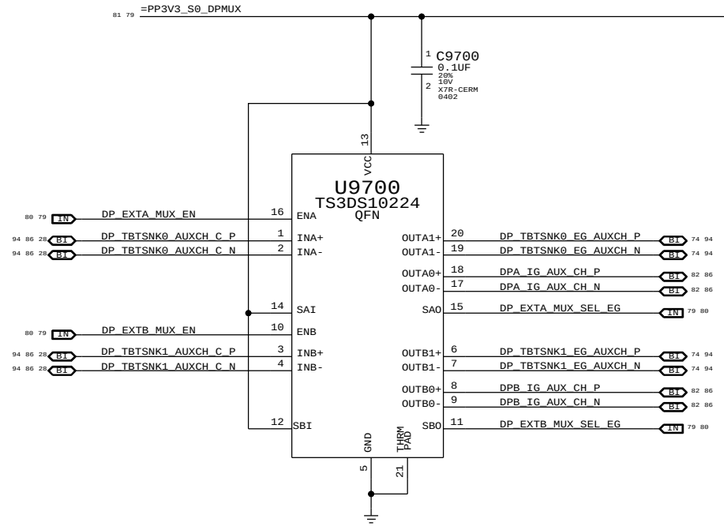
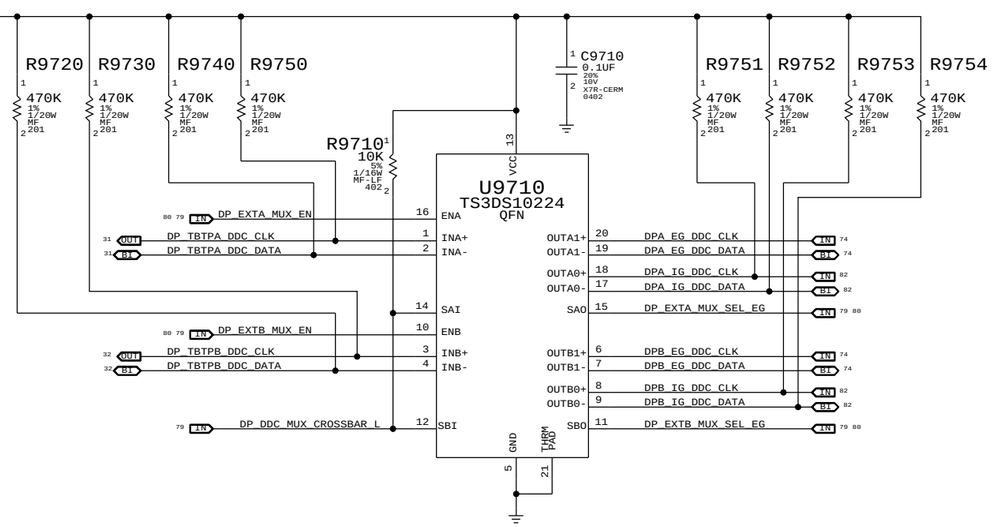
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC_MASTER=CLEAN_D2 SYNC_DATE=08/14/2012

PAGE TITLE: eDP Muxed Graphics Support

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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G3H/5V Rails

=PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_S5_HS_GPU_ISNS_R
=PPVIN_S5_HS_OTHER3V3_ISNS_R
=PPVIN_S5_HS_OTHER5V_ISNS_R
=PPVIN_S0_LCDBKLT
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE

=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S0_CPUVR
=PPVIN_S3_DDRREG
=PPVIN_S0_P1V05S0

=PPVIN_S5_HS_GPU_ISNS
PPVIN_S5_HS_GPU_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S0_GFXIMVP
=PPVIN_S0GPU_P1V5P1V0

=PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S5_P3V3

=PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S5_HS_OTHER5V_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S5_P5V

=PPVIN_T101_BOOSTRPBUS_ISNS
PPVIN_S4_TPAD
MIN_LINE_WIDTH=0.6 MM VOLTAGE=20V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S4_TPAD

=PP20V_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM VOLTAGE=20V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PP20V_DCIN_ISOL
PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM VOLTAGE=20V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V42_G3H_CHGR
=PP3V42_S3_HALL
=PP3V3_S5_LPCPLUS
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
=PP3V3_S5_SMC
=PP3V42_G3H_SMCUSBMUX
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK
=PP3V42_G3H_TPAD
=PP3V42_G3H_PCHPWRGD
=PP3V42_G3H_SSDSAK

=PPVRTC_G3_OUT
PPVRTC_G3H
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVRTC_G3_PCH

=PP5V_S5_LDO
PP5V_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP5V_S5_P1V35S3RS0FET
=PP5V_S5_TPAD

=PP5V_S4_REG
PP5V_S4
MIN_LINE_WIDTH=0.3 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_S4_AUDIO
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_P5VS0FET
=PP5V_S4_P5VS3FET
=PP5V_S4_RIO

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.5 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_S3_MEMRESET
=PP5V_S3_DDRREG
=PP5V_S3_ALSCAM

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.2 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_S0_AUDIO_XW
=PP5V_S0_CPUVR
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_P1V05S0
=PP5V_S0_VMON
=PP5V_S0_ALSCAM
=PP5V_S0_BKLTCTRL
=PP5V_S0_XDPJTAGISOL
=PP5V_S0_GFXIMVP
=PP5V_S0GPU_P1V0P1V35_GPU

3.3V Rails

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S4_SYSCLK
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_P3V3S4FET
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW
=PP3V3_S5_1V5PGOOD
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_DBGLED
=PP3V3_S5_P1V5S0
=PP3V3_S5_P3V3S0SW_SSD
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_WLAN
=PP3V3_S5_XDPJTAGISOL
=PP3V3_GPU_MISC_P3V3GPUMISCFET
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S5_GMUX_SLP_S3_L
=PP3V3_S5_FAN_CTL

=PP3V3_S4_FET
PP3V3_S4
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP3V3_S4_BT
=PP3V3_S4_RIO
=PP3V3_S4_SMC
=PP3V3_S4_TBT_R
=PP3V3_S4_TPAD
=PP3V3_S4_ISNS
=PP3V3_S4_WLAN
=PP3V3_S4_FAN_CTL

=PP3V3_SUS_FET
PP3V3_SUS
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_SUS_CNTRL
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_PCH_VCCSUS_RTC
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_PCH_VCCSUS_USB3
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_SUS_ROM

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S3RS4_PCH_GPIO
=PP3V3_S3_CAMERA_R
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_RIO
=PP3V3_S3_SDBUF
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_VREFMRGN
=PP3V3_S3_DPMUX_UC

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.4 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.075 MM MAKE_BASE=TRUE
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_CAMERA_R
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_CPUVRISNS
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_HS_ISNS
=PP3V3_S0_ISNS
=PP3V3_S0_LCD
=PP3V3_S0_OOB1_PWRDN
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_THRM
=PP3V3_S0_PCH_VCC3_3_USB
=PP3V3_S0_PCH_VCCCLK3_3
=PP3V3_S0_PCH_VCC_FUSE
=PP3V3_S0_RSTBUF
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD_AUX
=PP3V3_S0_VMON
=PP3V3_S0_X29THMSNS

=PP3V3_S0_DPMUX
=PP3V3_S0_DPMUXI2C
=PP3V3_S0_DPMUX_UC
=PP3V3_S0_PWRCTL

=PP3V3_S3RS0_CAMERA
PP3V3_S3RS0_CAMERA
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S3RS0_CAMPWREN

1.5V/1.35V/1.05V/VCORE/BKLT Rails

=PPDDR_S3_REG
PP1V35_S3
MIN_LINE_WIDTH=0.7 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.17 MM MAKE_BASE=TRUE
=PP1V5_S3_MEMRESET
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V35S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS
PP1V35_S3_MEM
MIN_LINE_WIDTH=0.2 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.17 MM MAKE_BASE=TRUE
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B

=PP1V35_S3RS0_FET_ISNS
PP1V35_S3RS0_CPUDDR
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V35_S3RS0_VMON
=PP1V5R1V35_S0_CPU

=PP1V35_S3RS0_FET
PP1V35_S3RS0_FET
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V35_S0_RIO

=PP1V5_S0_REG
PP1V5_S0
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V5_S0_AUDIO
=PP1V5_S0_PCH_CLK
=PP1V5_S0_PCH_SATA
=PP1V5_S0_PCH_RCOMP
=PP1V5_S0_PCH_VCCVRM
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PPVDDIO_S0_SBCLK
=PP1V5_S0_RIO
=PP1V5_S0_DIV

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM VOLTAGE=0.675V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO
PPVTT_S0_DDR
MIN_LINE_WIDTH=0.4 MM VOLTAGE=0.675V
MIN_NECK_WIDTH=0.17 MM MAKE_BASE=TRUE
=PPVTT_S0_MEM_A
=PPVTT_S0_MEM_B
=PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO
PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG

=PP1V05_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCC
=PP1V05_S0_PCH_VCCCLK_CLK100
=PP1V05_S0_PCH_VCCCLK_CLK135
=PP1V05_S0_PCH_VCCCLK_SSC
=PP1V05_S0_PCH_VCCCLK_SSC100
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_FDI
=PP1V05_S0_PCH_VCCIO_GPIO
=PP1V05_S0_PCH_VCCIO_USB2
=PP1V05_S0_PCH_VCCUSBPLL
=PP1V05_S0_PCH_VCC_CLK
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0M_PCH_VCCASW
=PP1V05_S0_CPU_JTAG
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON

=PPVCC_S0_CPU_REG
PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVCORE_S0_CPU
=PPVCC_S0_CPU

=PPBUS_SW_BKL
PPBUS_SW_BKL
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE

=PP3V3_S4_TBT
PP3V3_S4_TBT
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP3V3_S0SW_SSD_R
PP3V3_S0SW_SSD_R
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S0SW_SSD
PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

TBT RAILS

=PP3V3_TBTLC_FET
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.15 MM MAKE_BASE=TRUE
=PPVDDIO_TBTLC_CLK

=PP15V_TBT_REG
PP15V_TBT
MIN_LINE_WIDTH=0.4 MM VOLTAGE=15V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPHV_S4SW_TBTAPWRSW
=PPHV_S4SW_TBTBPWRSW

PPVIN_SW_TBTBST
VOLTAGE=12.6V

"GPU" Rails

=PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_IFPX_PLLVDD
=PP3V3_S0_GFX3V3BIAS
=PP3V3_GPU_VDD33

=PP3V3_S0GPU_MISC_FET
PP3V3_S0GPU_MISC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_MISC

=PP1V5R1V35_GPU_REG
PP1V5R1V35_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V35_GPU_FBVDDQ
=PP1V35_GPU_S0_FB
=PP1V35_GPU_FB

=PP1V05_S0GPU_REG
PP1V0_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_GPU_IFPCD_IOVDD
=PP1V05_GPU_IFPEF_IOVDD
=PP1V05_GPU_PEX_IOVDD
=PP1V05_GPU_PEX_PLLVDD

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVCORE_GPU
=PPVCORE_S0_GFX_REG

GND
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.085 MM
VOLTAGE=0V
MAKE_BASE=TRUE

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Display Aliases

12	EDP_IG_PANEL_PWR	=	IG_LCD_PWR_EN	79
	MAKE_BASE=TRUE			
12	EDP_IG_BKL_ON	=	IG_BKLT_EN	79
	MAKE_BASE=TRUE			
94 79	DP_INT_IG_ML_P<3..0>	=	TP_DP_IG_A_MLP<3..0>	5
	MAKE_BASE=TRUE			
94 79	DP_INT_IG_ML_N<3..0>	=	TP_DP_IG_A_MLN<3..0>	5
	MAKE_BASE=TRUE			
94 79	DP_INT_IG_AUX_P	=	TP_DP_IG_A_AUXCHP	5
	MAKE_BASE=TRUE			
94 79	DP_INT_IG_AUX_N	=	TP_DP_IG_A_AUXCHN	5
	MAKE_BASE=TRUE			
86 80	DPA_IG_AUX_CH_P	=	TP_DP_IG_B_AUXCHP	12
	MAKE_BASE=TRUE			
86 80	DPA_IG_AUX_CH_N	=	TP_DP_IG_B_AUXCHN	12
	MAKE_BASE=TRUE			
86 80	DPB_IG_AUX_CH_P	=	TP_DP_IG_C_AUXCHP	12
	MAKE_BASE=TRUE			
86 80	DPB_IG_AUX_CH_N	=	TP_DP_IG_C_AUXCHN	12
	MAKE_BASE=TRUE			
80	DPA_IG_DDC_CLK	=	TP_DP_IG_B_DDC_CLK	12
	MAKE_BASE=TRUE			
80	DPA_IG_DDC_DATA	=	TP_DP_IG_B_DDC_DATA	12
	MAKE_BASE=TRUE			
80	DPB_IG_DDC_CLK	=	TP_DP_IG_C_DDC_CLK	12
	MAKE_BASE=TRUE			
80	DPB_IG_DDC_DATA	=	TP_DP_IG_C_DDC_DATA	12
	MAKE_BASE=TRUE			
79	DP_TBTSNK0_HPD_IG	=	TP_DP_IG_B_HPD	12
	MAKE_BASE=TRUE			
79	DP_TBTSNK1_HPD_IG	=	TP_DP_IG_C_HPD	12
	MAKE_BASE=TRUE			
79	DPMUX_UC_RX	=	DPMUX_UC_BOOT_RX	79
	MAKE_BASE=TRUE			
79	DPMUX_UC_TX	=	DPMUX_UC_BOOT_TX	79
	MAKE_BASE=TRUE			
79	EG_RESET_L	=	GPU_RESET_L	68 75
	MAKE_BASE=TRUE			
82 11	PEG_CLKREQ_L	=	EG_CLKREQ_OUT_L	79
	MAKE_BASE=TRUE			
18 11	DP_AUXCH_ISOL_L	=	DP_AUXIO_EN	
	MAKE_BASE=TRUE			

CPU signals

21	MEMVTT_EN	=	=DDRVTT_EN	21 59
	MAKE_BASE=TRUE			

86 68 66	PEG_D2R_P<7..0>	=	=PEG_D2R_P<7..0>	5
	MAKE_BASE=TRUE			
86 68 66	PEG_D2R_N<7..0>	=	=PEG_D2R_N<7..0>	5
	MAKE_BASE=TRUE			
86 68	PEG_R2D_C_P<7..0>	=	=PEG_R2D_C_P<7..0>	5
	MAKE_BASE=TRUE			
86 68	PEG_R2D_C_N<7..0>	=	=PEG_R2D_C_N<7..0>	5
	MAKE_BASE=TRUE			

	NC_PCIE_PEG_D2RP<15..12>	=	=PEG_D2R_P<15..12>	5
	MAKE_BASE=TRUE NO_TEST=TRUE			
	NC_PCIE_PEG_D2RN<15..12>	=	=PEG_D2R_N<15..12>	5
	MAKE_BASE=TRUE NO_TEST=TRUE			
	NC_PCIE_PEG_R2D_CP<15..12>	=	=PEG_R2D_C_P<15..12>	5
	MAKE_BASE=TRUE NO_TEST=TRUE			
	NC_PCIE_PEG_R2D_CN<15..12>	=	=PEG_R2D_C_N<15..12>	5
	MAKE_BASE=TRUE NO_TEST=TRUE			

Thunderbolt Signals Through PEG

86 28	PCIE_TBT_D2R_P<3..0>	=	=PEG_D2R_P<11..8>	5
	MAKE_BASE=TRUE			
86 28	PCIE_TBT_D2R_N<3..0>	=	=PEG_D2R_N<11..8>	5
	MAKE_BASE=TRUE			
86 28	PCIE_TBT_R2D_C_P<3..0>	=	=PEG_R2D_C_P<11..8>	5
	MAKE_BASE=TRUE			
86 28	PCIE_TBT_R2D_C_N<3..0>	=	=PEG_R2D_C_N<11..8>	5
	MAKE_BASE=TRUE			

88 83 68	PEG_CLK100M_N	=	TP_PCIE_CLK100M_GPUN	11
	MAKE_BASE=TRUE			
88 83 68	PEG_CLK100M_P	=	TP_PCIE_CLK100M_GPUP	11
	MAKE_BASE=TRUE			

48	=PP3V3_S3_FAN_CTL	=	PP3V3_S3_FAN_CTL	
			MIN_LINE_WIDTH=0.4MM	
			MIN_NECK_WIDTH=0.2MM	
			VOLTAGE=3.3V	
			MAKE_BASE=TRUE	

RA201
0
1 2 5% 1/20W MF 0201 =PP3V3_S5_FAN_CTL 81
0
1 2 5% 1/20W MF 0201 =PP3V3_S4_FAN_CTL 81
RA202
NOSTUFF

	TP_P1V8GPU_EN	=	=P1V8GPU_EN	66

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
79 14	DPMUX_UC_IRQ
82 11	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L

		VOLTAGE	MAKE_BASE			
89 86 24 23 22	PPVREF_S3_MEM_VREFDQ_A	= 0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A		
86 26 25 22	PPVREF_S3_MEM_VREFDQ_B	= 0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B		
89 86 24 23 22	PPVREF_S3_MEM_VREFCA_A	= 0.675V	TRUE	PP0V75_S3_MEM_VREFCA_A		
86 26 25 22	PPVREF_S3_MEM_VREFCA_B	= 0.675V	TRUE	PP0V75_S3_MEM_VREFCA_B		

81	=PP5V_S0_AUDIO_XW			
	XWA202 SM 1 2	=	PP5V_S0_AUDIO_AMP_L	52
			MIN_LINE_WIDTH=0.4MM	
			MIN_NECK_WIDTH=0.2MM	
			VOLTAGE=5V	
	XWA203 SM 1 2	=	PP5V_S0_AUDIO_AMP_R	52
			MIN_LINE_WIDTH=0.4MM	
			MIN_NECK_WIDTH=0.2MM	
			VOLTAGE=5V	

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PAGE TITLE: Signal Aliases

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Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_Q_L	33
TRUE	AP_RESET_CONN_L	33
TRUE	PCIE_AP_D2R_PI_N	33 88
TRUE	PCIE_AP_D2R_PI_P	33 88
TRUE	PCIE_AP_R2D_N	33 88
TRUE	PCIE_AP_R2D_P	33 88
TRUE	PCIE_CLK100M_AP_CONN_N	33 88
TRUE	PCIE_CLK100M_AP_CONN_P	33 88
TRUE	PCIE_WAKE_L	12 33 35 88
TRUE	PP3V3_S3RS4_BT_F	33
TRUE	PP3V3_WLAN	33 41
TRUE	USB_BT_CONN_N	33 87
TRUE	USB_BT_CONN_P	33 87
TRUE	WIFI_EVENT_L	33 40 41
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	36 91
TRUE	MIPI_CLK_CONN_P	36 91
TRUE	CAM_SENSOR_WAKE_L_CONN	36
TRUE	MIPI_DATA_CONN_N	36 91
TRUE	MIPI_DATA_CONN_P	36 91
TRUE	=I2C_ALS_SDA	36 43
TRUE	=I2C_ALS_SCL	36 43
TRUE	I2C_CAM_SCK	35 36
TRUE	I2C_CAM_SDA	35 36
TRUE	PP5V_S3RS0_ALSCAM_F	36
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	86
TRUE	HDMI_CLK_P	86
TRUE	HDMI_DATA_N<0>	86
TRUE	HDMI_DATA_N<1>	86
TRUE	HDMI_DATA_N<2>	86
TRUE	HDMI_DATA_P<0>	86
TRUE	HDMI_DATA_P<1>	86
TRUE	HDMI_DATA_P<2>	86
TRUE	USB3_SD_D2R_N	20 78 88
TRUE	USB3_SD_D2R_P	20 78 88
TRUE	USB3_SD_R2D_C_N	20 78 88
TRUE	USB3_SD_R2D_C_P	20 78 88
TRUE	USB3_EXTB_D2R_N	13 78 87
TRUE	USB3_EXTB_D2R_P	13 78 87
TRUE	USB3_EXTB_R2D_N	78 87
TRUE	USB3_EXTB_R2D_P	78 87
TRUE	USB_EXTB_N	13 78 87
TRUE	USB_EXTB_P	13 78 87
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 78
TRUE	PP1V5R1V35_S0_RIO	78
TRUE	HDMI_DDC_CLK	
TRUE	HDMI_DDC_DATA	
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 43 88
TRUE	SMBUS_PCH_DATA	13 43 88
TRUE	PM_SLP_S3_BUF_L	50 64 65 78 79
TRUE	PM_SLP_S4_L	12 21 33 37 40 65 78
TRUE	PP3V3_S3	3X 81 83
TRUE	PP3V3_S4	81 83
TRUE	PP5V_S4	5X 81
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 78
TRUE	USB_EXTB_OC_L	18 78
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	81 83
TRUE	SMC_LID_R	42
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	48
TRUE	FAN_LT_TACH	48
TRUE	PP5V_S0	3X 81 83
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	48
TRUE	FAN_RT_TACH	48
TRUE	PP5V_S0	3X 81 83
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 49
TRUE	LPCPLUS_RESET_L	20 49
TRUE	LPC_AD<0>	13 40 49 79 88
TRUE	LPC_AD<1>	13 40 49 79 88
TRUE	LPC_AD<2>	13 40 49 79 88
TRUE	LPC_AD<3>	13 40 49 79 88
TRUE	LPC_CLK33M_LPCPLUS	19 49 88
TRUE	LPC_FRAME_L	13 40 49 79 88
TRUE	LPC_PWRDWN_L	12 20 40 49
TRUE	LPC_SERIRQ	13 40 49
TRUE	PM_CLKRUN_L	12 40 49
TRUE	PP5V_S0	81 83
TRUE	SMC_RESET_L	40 41 49 56
TRUE	SMC_ROMBOOT	41 49
TRUE	SMC_RX_L	40 41 49
TRUE	SMC_TCK	40 41 49
TRUE	SMC_TDI	40 41 49
TRUE	SMC_TDO	40 41 49
TRUE	SMC_TMS	40 41 49
TRUE	SMC_TX_L	40 41 49
TRUE	SPIROM_USE_MLB	14 49
TRUE	SPI_ALT_CLK	49
TRUE	SPI_ALT_CS_L	49
TRUE	SPI_ALT_MISO	49
TRUE	SPI_ALT_MOSI	49
TRUE	TP_SMC_MD1	49
TRUE	TP_SMC_TRST_L	49
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	38
TRUE	Z2_MOSI	38
TRUE	Z2_MISO	38
TRUE	Z2_SCLK	38
TRUE	Z2_HOST_INTN	38
TRUE	Z2_CLKIN	38
TRUE	Z2_KEY_ACT_L	38
TRUE	PSOC_F_CS_L	38
TRUE	PICKB_L	38
TRUE	PSOC_MOSI	38
TRUE	PSOC_MISO	38
TRUE	PSOC_SCLK	38
TRUE	=I2C_TPAD_SCL	38 43
TRUE	=I2C_TPAD_SDA	38 43
TRUE	SMC_LID	38 40 41 42
TRUE	SMC_T101_COM_1	
TRUE	=PP3V3_S4_TPAD	38 81
TRUE	=PP5V_S5_TPAD	38 81
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	81 83
TRUE	PP3V42_G3H	81 83
TRUE	WS_CONTROL_KBD	38
TRUE	WS_KBD1	38
TRUE	WS_KBD10	38
TRUE	WS_KBD11	38
TRUE	WS_KBD12	38
TRUE	WS_KBD13	38
TRUE	WS_KBD14	38
TRUE	WS_KBD15_CAP	38
TRUE	WS_KBD16_NUM	38
TRUE	WS_KBD17	38
TRUE	WS_KBD18	38
TRUE	WS_KBD19	38
TRUE	WS_KBD2	38
TRUE	WS_KBD20	38
TRUE	WS_KBD21	38
TRUE	WS_KBD22	38
TRUE	WS_KBD23	38
TRUE	WS_KBD3	38
TRUE	WS_KBD4	38
TRUE	WS_KBD5	38
TRUE	WS_KBD6	38
TRUE	WS_KBD7	38
TRUE	WS_KBD8	38
TRUE	WS_KBD9	38
TRUE	WS_KBD_ONOFF_L	38
TRUE	WS_LEFT_OPTION_KBD	38
TRUE	WS_LEFT_SHIFT_KBD	38
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 39 62
TRUE	KBDBKLT_RETURN2	2X 39 62
TRUE	PPVOUT_S0_KBDBKLT	39 62
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	50 54
TRUE	AUD_HP_PORT_R	50 54
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	50 54
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	81 83 93
TRUE	AUD_CONN_SLEEVE_XW	4X 53 54
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	51 54
TRUE	PP3V3_S0	81 83 93
TRUE	DMIC_SDA2	54
TRUE	DMIC_SDA3	51 54
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	51 54
TRUE	SPKRCONN_L_OUT_N	52 54 93
TRUE	SPKRCONN_L_OUT_P	52 54 93
TRUE	SPKRCONN_SL_OUT_N	52 54 93
TRUE	SPKRCONN_SL_OUT_P	52 54 93
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	51 54
TRUE	SPKRCONN_R_OUT_N	52 54 93
TRUE	SPKRCONN_R_OUT_P	52 54 93
TRUE	SPKRCONN_SR_OUT_N	52 54 93
TRUE	SPKRCONN_SR_OUT_P	52 54 93
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	55
TRUE	PP20V_DCIN_FUSE	2X 55
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 55 56
TRUE	SMBUS_SMC_5_G3_SCL	40 43 92
TRUE	SMBUS_SMC_5_G3_SDA	40 43 92
TRUE	SYS_DETECT_L	55
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 86 94
TRUE	DP_INT_AUX_P	67 86 94
TRUE	DP_INT_ML_N<0>	67 86 94
TRUE	DP_INT_ML_N<1>	67 86 94
TRUE	DP_INT_ML_N<2>	67 86 94
TRUE	DP_INT_ML_N<3>	67 86 94
TRUE	DP_INT_ML_P<0>	67 86 94
TRUE	DP_INT_ML_P<1>	67 86 94
TRUE	DP_INT_ML_P<2>	67 86 94
TRUE	DP_INT_ML_P<3>	67 86 94
TRUE	LCD_FSS	62 67 79
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	62 67
TRUE	LED_RETURN_2	62 67
TRUE	LED_RETURN_3	62 67
TRUE	LED_RETURN_4	62 67
TRUE	LED_RETURN_5	62 67
TRUE	LED_RETURN_6	62 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	62 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 40 65
TRUE	PPVTT_S0_DDR	81
TRUE	PP3V3_S0	81 83 93
TRUE	PP3V3_S3	81 83
TRUE	PP3V3_S5	81 93
TRUE	PP3V3_S5_AVREF_SMC	40 41
TRUE	PP3V42_G3H	81 83
TRUE	PP5V_S0	81 83
TRUE	PP5V_S3	81
TRUE	PP5V_S5	81
TRUE	PPBUS_G3H	81
TRUE	PPDCIN_G3H	81
TRUE	PPVCC_S0_CPU	81
TRUE	PPVTTDDR_S3	81
TRUE	PP3V3_S0SW_SSD	81
TRUE	PP1V5_S0	81
TRUE	PP1V35_S3	81

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 86
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 86
TRUE	XDP_CPU_TDO	6 18 86
TRUE	XDP_CPU_TRST_L	6 18 86
TRUE	XDP_CPU_TMS	6 18 86
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 86
TRUE	XDP_CPU_PRDY_L	6 18 86
TRUE	PM_RSMRST_L	12 65 88
TRUE	PM_PCH_PWROK	12 19 88
TRUE	PM_SYSRST_L	12 19 40 88
TRUE	CPU_CFG<3>	6 18 86
TRUE	PP1V05_S0	81
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	38 40 41
TRUE	PM_DSW_PWRGD	12 40 88
TRUE	ALL_SYS_PWRGD	18 19 40 65
TRUE	PM_PCH_SYS_PWROK	12 18 19 40 88
TRUE	PLT_RESET_L	12 18 20 21
TRUE	LCD_PWR_EN	67 79
TRUE	LCD_BKLT_EN	62 79

TPA401 / TPA402

TPA401 A TP-P6	PEG_CLK100M_P	68 82 88
TPA402 A TP-P6	PEG_CLK100M_N	68 82 88

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NC NO_TESTs

PCH

		NO_TEST	MAKE_BASE	
13	TP_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
13	TP_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
13	TP_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
13	TP_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
13	USB3_EXTC_D2R_N	TRUE	TRUE	NC_USB3_EXTC_D2RN 87
13	USB3_EXTC_D2R_P	TRUE	TRUE	NC_USB3_EXTC_D2RP 87
13	USB3_EXTC_R2D_C_N	TRUE	TRUE	NC_USB3_EXTC_R2D_CN 87
13	USB3_EXTC_R2D_C_P	TRUE	TRUE	NC_USB3_EXTC_R2D_CP 87
13	USB3_EXTD_D2R_N	TRUE	TRUE	NC_USB3_EXTD_D2RN 87
13	USB3_EXTD_D2R_P	TRUE	TRUE	NC_USB3_EXTD_D2RP 87
13	USB3_EXTD_R2D_C_N	TRUE	TRUE	NC_USB3_EXTD_R2D_CN 87
13	USB3_EXTD_R2D_C_P	TRUE	TRUE	NC_USB3_EXTD_R2D_CP 87
	PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
	PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
	PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
	PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
11	SATA_A_D2R_N	TRUE	TRUE	NC_SATA_A_D2RN 87
11	SATA_A_D2R_P	TRUE	TRUE	NC_SATA_A_D2RP 87
11	SATA_A_R2D_C_N	TRUE	TRUE	NC_SATA_A_R2D_CN 87
11	SATA_A_R2D_C_P	TRUE	TRUE	NC_SATA_A_R2D_CP 87
11	SATA_B_D2R_N	TRUE	TRUE	NC_SATA_B_D2RN 87
11	SATA_B_D2R_P	TRUE	TRUE	NC_SATA_B_D2RP 87
11	SATA_B_R2D_C_N	TRUE	TRUE	NC_SATA_B_R2D_CN 87
11	SATA_B_R2D_C_P	TRUE	TRUE	NC_SATA_B_R2D_CP 87
11	TP_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
11	TP_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
11	TP_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
11	TP_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
11	TP_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
11	TP_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
11	TP_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
11	TP_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
11	TP_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
11	TP_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
11	TP_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
11	TP_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
13	USB_EXTC_N	TRUE	TRUE	NC_USB_EXTCN 87
13	USB_EXTC_P	TRUE	TRUE	NC_USB_EXTCP 87
13	TP_USB_SDN	TRUE	TRUE	NC_USB_SDN 87
13	TP_USB_SDP	TRUE	TRUE	NC_USB_SDP 87
13	TP_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
13	TP_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
13	TP_USB_6N	TRUE	TRUE	NC_USB_6N 87
13	TP_USB_6P	TRUE	TRUE	NC_USB_6P 87
13	TP_USB_7N	TRUE	TRUE	NC_USB_7N 87
13	TP_USB_7P	TRUE	TRUE	NC_USB_7P 87
13	USB_EXTD_N	TRUE	TRUE	NC_USB_EXTDN 87
13	USB_EXTD_P	TRUE	TRUE	NC_USB_EXTDP 87
13	TP_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
13	TP_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
13	USB_IR_N	TRUE	TRUE	NC_USB_IRN 87
13	USB_IR_P	TRUE	TRUE	NC_USB_IRP 87
86 11	ITPXDP_CLK100M_N	TRUE	TRUE	NC_ITPXDP_CLK100MN
86 11	ITPXDP_CLK100M_P	TRUE	TRUE	NC_ITPXDP_CLK100MP
12	TP_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
20 11	TP_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
11	TP_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
11	TP_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
11	TP_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
11	TP_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
13	TP_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
13	TP_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
13	TP_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
13	TP_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
12	EDP_IG_BKL_PWM	TRUE	TRUE	NC_EDP_IG_BKL_PWM
87	USB_SMC_P	TRUE	TRUE	NC_USB_SMCP
87	USB_SMC_N	TRUE	TRUE	NC_USB_SMCN
	SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

		NO_TEST	MAKE_BASE	
28	TP_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
28	TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
28	TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
28	TP_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
28	TP_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
12	TP_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
12	TP_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
11	TP_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
11	TP_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
11	PCIE_CLK100M_ENETSD_N	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
11	PCIE_CLK100M_ENETSD_P	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
11	TP_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
11	TP_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
11	TP_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
11	TP_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
11	TP_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
11	TP_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
11	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
11	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
11	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
11	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
13	TP_USB_4N	TRUE	TRUE	NC_USB_4N
13	TP_USB_4P	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	28 86
TRUE	PCIE_TBT_R2D_N<3..0>	28 86
TRUE	PCIE_TBT_D2R_C_P<3..0>	28 86
TRUE	PCIE_TBT_D2R_C_N<3..0>	28 86
TRUE	DMI_S2N_P<3..1>	5 12 86
TRUE	DMI_S2N_N<3..1>	5 12 86
TRUE	DMI_N2S_P<3..1>	5 12 86
TRUE	DMI_N2S_N<3..1>	5 12 86

PLACEABLE BEAD-PROBES FOR TBT

90 31 28	TBT_A_R2D_C_P<1>	1	SM	BEAD-PROBE BPA535 NO_XNET_CONNECTION=TRUE
90 31 28	TBT_A_D2R_P<1>	1	SM	BEAD-PROBE BPA531 NO_XNET_CONNECTION=TRUE
90 31 28	TBT_A_D2R_N<1>	1	SM	BEAD-PROBE BPA532 NO_XNET_CONNECTION=TRUE

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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE_ADJ	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE_ADJ	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 84
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 84
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 84
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 84
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 83
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	ITPXDP_CLK100M_P	11 84
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	ITPXDP_CLK100M_N	11 84
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 83
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 83
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 83
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 83
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L	6 18 83
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 83
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 83
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 40
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 41
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 40 41 57
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTI	PM_THRMTRIP_L	6 14 41
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 57
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 57
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 57
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A	22 23 24 82 89
CPU_MEM_VREF		CPU_VREF	PPVREF_S3_MEM_VREFDQ_B	22 25 26 82
CPU_MEM_VREF		MEM_PWR	PPVREF_S3_MEM_VREFCA_A	22 23 24 82 89
CPU_MEM_VREF		CPU_VREF	PPVREF_S3_MEM_VREFCA_B	22 25 26 82
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R P<7..0>	66 68 82
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R N<7..0>	66 68 82
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	68
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	68
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	66 68
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	66 68
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	68 82
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	68 82
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	28 82
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	28 82
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 84
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 84
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 84
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 84
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	28 82
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	28 82

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	67 79 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	67 79 94
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 83 86 94
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 83 86 94
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67 94
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67 94
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 83 86 94
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 83 86 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	67 79 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	67 79 94
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 83 94
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 83 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	80 82

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	83
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	83
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	83
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	83
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 74 94
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 74 94
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28 94
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 74 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 74 94
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28 94
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28 94
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28 94
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28 94
	DP_85D		DP_TBTSNK0_AUXCH_C_P	28 80 94
	DP_85D		DP_TBTSNK0_AUXCH_C_N	28 80 94
TBTSNK1_AUXCH1	DP_85D		DP_TBTSNK1_AUXCH_P	28 94
TBTSNK1_AUXCH1	DP_85D		DP_TBTSNK1_AUXCH_N	28 94
	DP_85D		DP_TBTSNK1_AUXCH_C_P	28 80 94
	DP_85D		DP_TBTSNK1_AUXCH_C_N	28 80 94

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	84
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	84
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	84
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	84
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	84
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	84
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	84
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	84
T21 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
USB_EXTA	USB_85D	USB	USB_EXTA_P	13 37
USB_EXTA	USB_85D	USB	USB_EXTA_N	13 37
T24 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	37
T24 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	37
T23 USB_EXTA	USB_85D	USB	USB_LT1_P	37
T23 USB_EXTA	USB_85D	USB	USB_LT1_N	37
USB_NC	USB_85D	USB	NC_USB_EXTCP	84
USB_NC	USB_85D	USB	NC_USB_EXTCN	84
T23 USB_NC	USB_85D	USB	NC_USB_SDP	84
T23 USB_NC	USB_85D	USB	NC_USB_SDN	84
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	37 40 41
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	37 40 41
USB_SMC	USB_85D	USB	USB_SMC_P	84
USB_SMC	USB_85D	USB	USB_SMC_N	84
T28 USB_NC	USB_85D	USB	NC_USB_6P	84
T28 USB_NC	USB_85D	USB	NC_USB_6N	84
T28 USB_NC	USB_85D	USB	NC_USB_7P	84
T28 USB_NC	USB_85D	USB	NC_USB_7N	84
USB_EXTB	USB_85D	USB	USB_EXTB_P	13 78 83
USB_EXTB	USB_85D	USB	USB_EXTB_N	13 78 83
T26 USB_NC	USB_85D	USB	NC_USB_EXTDP	84
T25 USB_NC	USB_85D	USB	NC_USB_EXTDN	84
USB_BT	USB_85D	USB	USB_BT_P	13 33
USB_BT	USB_85D	USB	USB_BT_N	13 33
	USB_85D	USB	USB_BT_CONN_P	33 83
	USB_85D	USB	USB_BT_CONN_N	33 83
T28 USB_NC	USB_85D	USB	NC_USB_IRP	84
T28 USB_NC	USB_85D	USB	NC_USB_IRN	84
T28 USB_TPAD	USB_85D	USB	USB_TPAD_P	13 38
T28 USB_TPAD	USB_85D	USB	USB_TPAD_N	13 38
T30	USB_85D	USB	USB_TPAD_R_P	38
T30	USB_85D	USB	USB_TPAD_R_N	38
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T22 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 37
T23 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 37
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T23 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	37
T22 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	37
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 37
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 37
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 78 83
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 78 83
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	78 83
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	78 83
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 78
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 78
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	84
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	84
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	84
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	84
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	84
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	84
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	84
T29	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	84

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T25 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T25 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T25	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T25 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 36
T25 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T25	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 40 49 79 83
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 40 49 79 83
LPC_RESET_L	LPC_45S	LPC	LPC_RESET_L	20
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 43 83
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 43 83
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 43
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 43
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 43
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 43
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 51
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 51
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 51
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 51
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	51
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 51
	HDA_45S	HDA	HDA_SDOUT_R	11 19
	SPI_45S	SPI	SPI_CLK_R	13 49
SPI_CLK	SPI_45S	SPI	SPI_CLK	49
	SPI_45S	SPI	SPI_MOSI_R	13 49
SPI_MOSI	SPI_45S	SPI	SPI_MOSI	49
SPI_MISO	SPI_45S	SPI	SPI_MISO	13 49
	SPI_45S	SPI	SPI_CS0_R_L	13 49
SPI_CS0	SPI_45S	SPI	SPI_CS0_L	49
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	20 78 83
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	20 78 83
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	20 78 83
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	20 78 83
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	33 83
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	33 83
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 33
[1804]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 33
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	33
[1805]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	33
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 33
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 33
[1275]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	33 83
[1276]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	33 83
[1325] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	35 36
[1326] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	35 36
[1327]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 36
[1328]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 36
[1329] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 36
[1330] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 36
[1331]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	35 36
[1332]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	35 36
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 40
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 49 83
[2462]	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
[2463] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
[254] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
[255] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
[253] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
[254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
[257] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
[258] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
[255] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
[257] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
[256] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
[258] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PEG_CLK100M	PEG_80D	CLK_PCIE	PEG_CLK100M_P	68 82 83
PEG_CLK100M	PEG_80D	CLK_PCIE	PEG_CLK100M_N	68 82 83
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 33
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 33
[1806]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	33 83
[1807]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	33 83
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 36
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 36
[1333]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	35 36
[1334]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	35 36
[2461] PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 34
[2460]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 34

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
[1813] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
[1814] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
[1815] PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
[1816] PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
[1808] PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 65 83
[1807] PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 40 83
[1810] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 83
[1817] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_APWROK	12 19
[1820] PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 40 83
[1819] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 40 83
[1822] PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 40
[1824] PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 41
[1826] PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 33 35 83
[1827] PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
[1835] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 34
[1836] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 34
[1838] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 34
[1837] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 34
[1839]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	34
[1840]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	34

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A 22 23 24 82 86
		MEM_PWR	PPVREF_S3_MEM_VREFCA_A 22 23 24 82 86
		MEM_PWR	PP1V35_S3_MEM 81

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius’s Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31 84
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 84
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 84
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		NET_TYPE		
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE
1101	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L
1102		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT
1103	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L
1104	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>
1105	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>
1106	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>
1107	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>
1108	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>
1109	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>
1110	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>
1127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P
1128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N
1129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P
1130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N
1131	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P
1132	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N
1133		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P
1134		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N
1135			S2_MEM_PWR	PP1V35_CAM
1136			S2_MEM_PWR	PP0V675_CAM_VREF
1137			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA
1138			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ

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PAGE TITLE: Camera Constraints

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	40 43 83
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	40 43 83
SMBUS_SMC_3_SCL	SMB_45S	SMB	SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_45S	SMB	SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	56
	1TO1_DIFFPAIR		CHGR_CSI_N	56
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	56
	1TO1_DIFFPAIR		CHGR_CSO_N	56

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N
		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P 46
		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N 46
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P 47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N 47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P 47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N 47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_P 47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_N 47
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P 45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N 45
L41P		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P 45
L42P		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N 45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P 46
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N 46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N 46 62
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P 46 62
L20P	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPUFB_R_P 45
L22P	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPUFB_R_N 45
L23P	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_P 45 71
L23N	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_N 45 71
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P 44
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N 44
L51P	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P 44
L51N	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N 44
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P 44
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N 44
L52P	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_P 46 71
L52N	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_N 46 71
L53P	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P 44
L53N	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N 44
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P 45
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N 45
L55P	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P 46
L55N	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N 46
L61P	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P 71 76
L61N	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N 71 76
L42P	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P 45 58
L43P	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N 45 58
L43N	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P 45 58
L44P	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N 45 58
L44N	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P 45 58
L45P	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N 45 58
L32P	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P 45
L32N	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N 45
L51P	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_P 77
L53P	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_N 77
L52P	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_P 77
L53N	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_N 77
L53P	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P 47 74
L53N	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N 47 74
L63P	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P 76 77
L63N	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N 76 77
L40P	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N 45
L40N	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P 45
L40P		AUDIODIFF	AUDIO	ISNS_TBT_R_N 45
L40N		AUDIODIFF	AUDIO	ISNS_TBT_R_P 45
L44P	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P 45
L44N		THERM_1TO1_45S	THERM	ISNS_SSD_N 45
L44P	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P 45
L44N		THERM_1TO1_45S	THERM	ISNS_SSD_R_N 45
L44P	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P 61
L45N		THERM_1TO1_45S	THERM	P1V05S0_CS_N 61
L45P	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P 61
L45N		THERM_1TO1_45S	THERM	P1V05S0_SENSE_N 61
L45P	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P 47
L45N		THERM_1TO1_45S	THERM	TBT_THERMD_N 47
L45P	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P 56
L45N		AUDIODIFF	AUDIO	CHGR_CSI_R_N 56
L46P	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P 56
L46N		AUDIODIFF	AUDIO	CHGR_CSO_R_N 56
L61P	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P
L61N	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N
L61P	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P 46
L61N	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N 46

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
L49P		AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P 52
L49N		AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N 52
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P 52
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N 52
L43P		AUDIODIFF	AUDIO	RSUBIN_P 52
L44P		AUDIODIFF	AUDIO	RSUBIN_N 52
L41P		AUDIODIFF	AUDIO	LSUBIN_P 52
L42P		AUDIODIFF	AUDIO	LSUBIN_N 52
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P 50 52
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N 50 52
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P 50 52
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N 50 52
		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P 52
		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N 52
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P 52
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N 52
L49P		AUDIODIFF	AUDIO	SPKRAMP_RIN_P 52
L49N		AUDIODIFF	AUDIO	SPKRAMP_RIN_N 52
L46P		AUDIODIFF	AUDIO	SPKRAMP_LIN_P 52
L46N		AUDIODIFF	AUDIO	SPKRAMP_LIN_N 52
L35P	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P 52 54 83
L35N	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N 52 54 83
L36P	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P 52 54 83
L36N	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N 52 54 83
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P 52 54 83
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N 52 54 83
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P 52 54 83
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N 52 54 83
L38P	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P
L38N	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N
L48P	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P 50
L48N	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N 50
L48A	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P
L48B		DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N
L48C		DIFFPAIR	AUDIO	AUD_HS_MIC_P 53 54
L48D		DIFFPAIR	AUDIO	AUD_HS_MIC_N 53 54
L48E		DIFFPAIR	AUDIO	HS_MIC_P 50 53
L48F		DIFFPAIR	AUDIO	HS_MIC_N 50 53
L49C		DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P
L49D		DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N
L49A	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P 50 52
L49B	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N 50 52
L48A	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P 50 52
L48B	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N 50 52
			SB_POWER	PP3V3_S5 81 83
			SB_POWER	PP3V3_S0 81 83
			SB_POWER	PP1V35_S3RS0_CPUDDR 81
			GND	GND

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	70 72
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	70 72
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	70 72
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	70 72
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>	70 72
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>	70 72
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L	70 72
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L	70 72
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L	70 72
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L	70 72
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L	70 72
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L	70 72
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L	70 72
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L	70 72
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L	70 72
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L	70 72
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L	70 72
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L	70 72
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	70 72
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	70 72
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	70 72
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	70 72
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	70 72
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	70 72
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	70 72
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	70 72
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	70 72
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	70 72
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	70 72
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	70 72
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	70 72
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	70 72
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	70 72
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	70 72
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	70 72
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	70 72
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	70 72
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	70 72
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	70 72
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	70 72
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	70 72
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	70 72
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	70 72
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	70 72
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	70 72
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	70 72
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	70 72
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	70 72
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	70 72
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	70 72
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L	70 72
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L	70 72

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	70 73
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	70 73
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	70 73
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	70 73
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>	70 73
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>	70 73
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L	70 73
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L	70 73
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L	70 73
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L	70 73
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L	70 73
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L	70 73
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L	70 73
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L	70 73
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L	70 73
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L	70 73
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L	70 73
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L	70 73
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	70 73
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	70 73
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	70 73
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	70 73
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	70 73
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	70 73
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	70 73
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	70 73
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	70 73
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	70 73
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	70 73
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	70 73
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	70 73
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	70 73
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	70 73
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	70 73
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	70 73
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	70 73
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	70 73
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	70 73
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	70 73
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	70 73
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	70 73
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	70 73
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	70 73
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	70 73
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	70 73
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	70 73
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	70 73
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	70 73
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	70 73
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	70 73
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L	70 73
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L	70 73

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	67 79 86
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	67 79 86
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67 86
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67 86
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 83 86
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 83 86
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	67 79 86
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	67 79 86
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 83 86
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 83 86
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	79 82
	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	79 82
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3..0>	79 82
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3..0>	79 82
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	74 79
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	74 79
DP_INT_EG_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	74 79
	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	74 79
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P	74 80
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N	74 80
DP_INT_EG_AUX1	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P	74 80
DP_INT_EG_AUX1	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N	74 80
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	28 86
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	28 86
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	28 80 86
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	28 80 86
TBTSNK1_AUXCH1	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	28 86
TBTSNK1_AUXCH1	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	28 86
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	28 80 86
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	28 80 86
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28 86
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28 86
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 74 86
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 74 86
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28 86
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28 86
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 74 86
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 74 86

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALIN	74 75
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALOUT	74 75
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT_R	74
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_SSIN	74
	1TO1_DIFFPAIR		PEX_TSTCLK_O_P	68
	1TO1_DIFFPAIR		PEX_TSTCLK_O_N	68
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_P<2..0>	74 78
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_N<2..0>	74 78
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_P	74 78
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_N	74 78

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