

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
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J44 MLB-4GB SCHEMATIC

08/20/2013

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ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0052	1	SCHEM,MLB-4GB,J44	SCH	CRITICAL	
820-3536	1	PCBF,MLB-4GB,J44	PCB	CRITICAL	

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BOM Groups

BOM GROUP	BOM OPTIONS
J44_COMMON	ALTERNATE,COMMON,J44_COMMON1,J44_COMMON2,J44_COMMON3,J44_COMMON4,J44_PROGPARTS
J44_COMMON1	TBTHV:P15V,SKIP_5V3V3:AUDIBLE,SPI:DUAL_IO
J44_COMMON2	EDP,EDP_LS_CAP,CAMERA_3V3:S0,CAM_WAKE:NO,CAM_XTAL:NO,MEM_ODT:PU,VCORE_FETS
J44_COMMON3	XDP,LPCPLUS,BKLT:PROD,CPU_THRM:ALRT,LOADRC:NO,OTHERRC:NO,DDRR:NO,TBTRC:NO,BMONRC:NO
J44_PROGPARTS	SMC_PROG:PVT,BOOTROM:PVT,TBTROM:PVT,TPAD_PSOC:PROG
ENGISNS	LOADISNS,OTHERISNS,DDRISNS,TBTISNS,BMONISNS

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3918	1	EPROM,FALCON RIDGE (V13.7) J44	U2890	CRITICAL	TBTROM:PVT

SMC

341S3922	1	IC,SMC-B1,EXT(V2.16F39),PVT,J44	U5000	CRITICAL	SMC_PROG:PVT
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EFI ROM

341S3924	1	IC,EFI ROM (V0116),PVT,J44	U6100	CRITICAL	BOOTROM:PVT
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PSOC

341S3862	1	IC,TRKPD/KYBD PSOC,CU ONLY (V224) J44	U4801	CRITICAL	TPAD_PSOC:PROG
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Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4596	1	HSWULT,SR18A,PRO,CO,2.4,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.4G
337S4597	1	HSWULT,SR189,PRO,CO,2.6,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.6G
337S4598	1	HSWULT,SR188,PRO,CO,2.8,28W,2+3,4M,BGA	U0500	CRITICAL	CPU_HSW:2.8G
338S1247	1	IC,TBT,FR-4C,A0,PRO,CIO,SR13C,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson alt to NDK
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
138S0725	138S0724		ALL	Samsung alt to Murata
376S1032	376S0855		ALL	Toshiba alt for Diodes Dual
376S1129	376S0855		ALL	NXP Alt for Diodes Dual
376S1089	376S1128		ALL	NXP Alt for Diodes Single
353S3452	353S1286		ALL	Maxim alt to Microchip
376S1180	376S0761		ALL	Renesas alt to Vishay
128S0364	128S0264		ALL	Sanyo 2nd Factory alt
107S0254	107S0241		ALL	Cyntec alt to TFT
138S0843	138S0674		ALL	Samsung alt to Murata (BKLT)
138S0803	138S0639		ALL	Samsung alt to Murata (BKLT)
138S0846	138S0811		ALL	Samsung alt to Murata (BKLT)
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
127S0164	127S0162		ALL	Rohm alt to Vishay
353S4070	353S4069		ALL	Pericom alt to TI DP Mux U9750
353S4068	353S4069		ALL	NXP alt to TI DP Mux U9750
353S3814	353S3812		ALL	TI alt to NXP
311S0649	311S0541		ALL	ONsemi alt to Toshiba
128S0436	128S0392		ALL	Kemet alt to Sanyo

SYNCH MASTERS/14 SYNCH DATE/08/20/2014

BOM Configuration

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0054	COMMON,MLB-4GB,J44	J44_COMMON
985-0053	DEV,MLB-4GB,J44	XDP_CONN
639-4878	PCBA,MLB-4GB,2.4G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-4879	PCBA,MLB-4GB,2.4G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-4880	PCBA,MLB-4GB,2.4G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_MICRON,CAMDRAM:MICRON
639-5272	PCBA,MLB-4GB,2.6G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5273	PCBA,MLB-4GB,2.6G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-5274	PCBA,MLB-4GB,2.6G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_MICRON,CAMDRAM:MICRON
639-5275	PCBA,MLB-4GB,2.8G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5276	PCBA,MLB-4GB,2.8G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-5277	PCBA,MLB-4GB,2.8G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_MICRON,CAMDRAM:MICRON
685-0074	VCORE,FET,VSHY,J44	VCORE_FET:VSHY
685-0075	VCORE,FET,REN,J44	VCORE_FET:REN

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0054	1	J44 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-0053	1	J44 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SUB-BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0074	1	VCORE,FET,VSHY,J44	VCOREFETS	CRITICAL	VCORE_FETS

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0075	685-0074		ALL	RENDSAS ALT TO VISHAY

DRAM PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0704	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,F,DIE,96FBGA	U4000	CRITICAL	4G_ELPIDA
333S0700	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,HUMA,96FBGA	U4000	CRITICAL	4G_HYNIX_H
333S0698	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,REV E,96FBGA	U4000	CRITICAL	4G_MICRON
333S0715	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,F,DIE,96FBGA	U4000	CRITICAL	4G_ELPIDA_1866
333S0717	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,HUMA,96FBGA	U4000	CRITICAL	4G_HYNIX_H_1866
333S0720	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,REV E,96FBGA	U4000	CRITICAL	4G_MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G_ELPIDA	4G_ELPIDA,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L,PPDDR:1V35
RAM_4G_HYNIX_H	4G_HYNIX_H,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H,PPDDR:1V35
RAM_4G_MICRON	4G_MICRON,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L,PPDDR:1V35
RAM_4G_ELPIDA_1866	4G_ELPIDA_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L,PPDDR:1V5
RAM_4G_HYNIX_H_1866	4G_HYNIX_H_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H,PPDDR:1V5
RAM_4G_MICRON_1866	4G_MICRON_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L,PPDDR:1V5

NOTE: 1866 PARTS BEING STRAPPED TO RUN AT 1600

13" MBP VARIABLE BOM GROUPS

BOM GROUP	BOM OPTIONS
J44_COMMON4	SMCBOARDID:8

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
CAMDRAM:HYNIX_H	CAMDRAM_TYPE:HYNIX_H
CAMDRAM:ELPIDA	CAMDRAM_TYPE:ELPIDA
CAMDRAM:MICRON	CAMDRAM_TYPE:MICRON

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	1C,SDRAM,4GBIT,DDR3L-1600,HUMA,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:HYNIX_H
333S0704	1	1C,SDRAM,4GBIT,DDR3L-1600,DIE P,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:ELPIDA
333S0698	1	1C,SDRAM,4GBIT,DDR3L-1600,REV E,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:MICRON

SYNC MASTER=J44 SYNC DATE=01/03/2013

BOM Configuration

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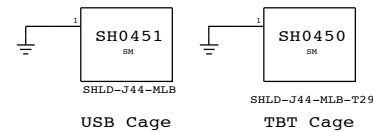
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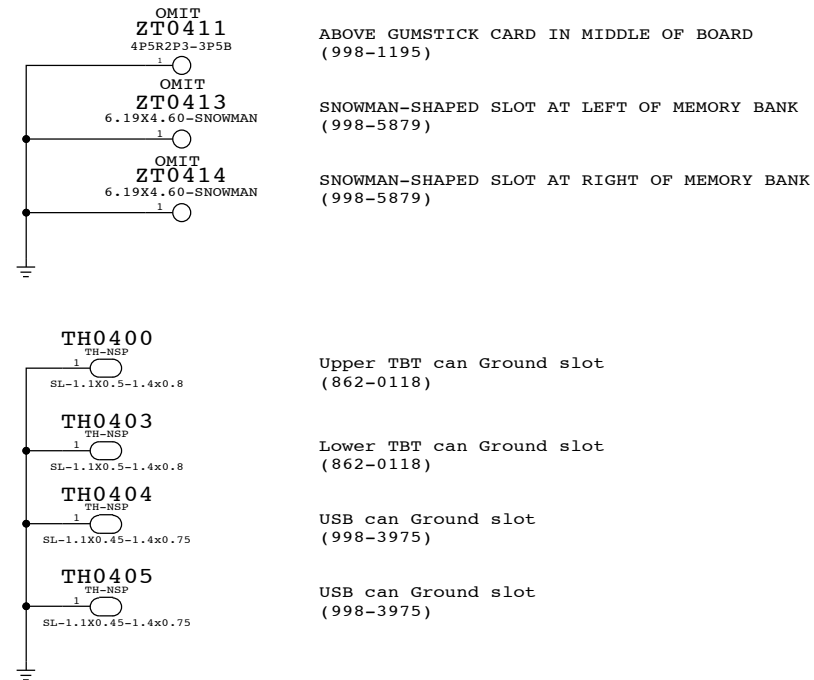
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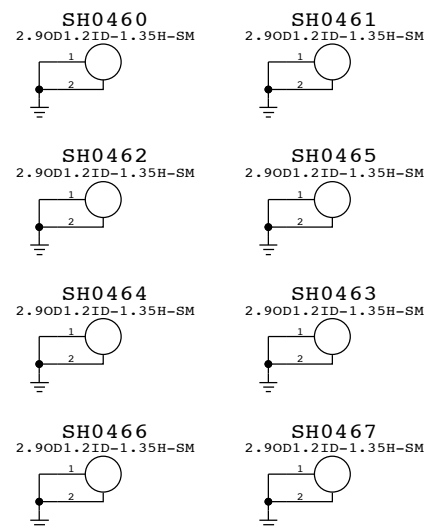
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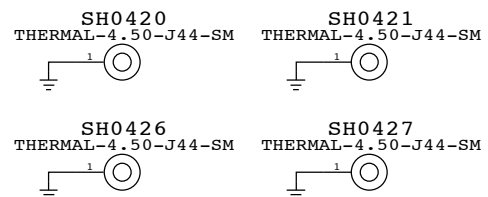
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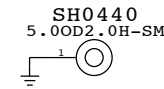
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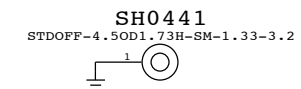
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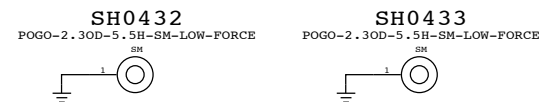
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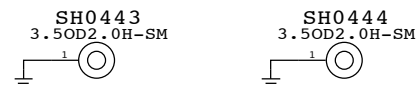
FAN STANDOFF (806-5376)



POGO PINS (870-2451) SH0435 & SH0436 removed.



RIO FLEX BRACKET BOSSES (860-2354)



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SYNC MASTER=J44		SYNC DATE=08/12/2013	
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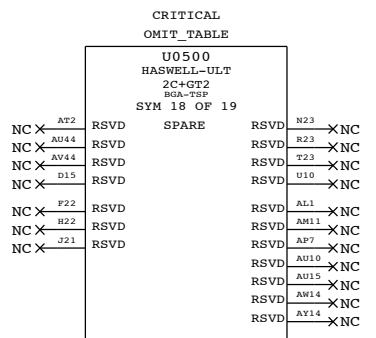
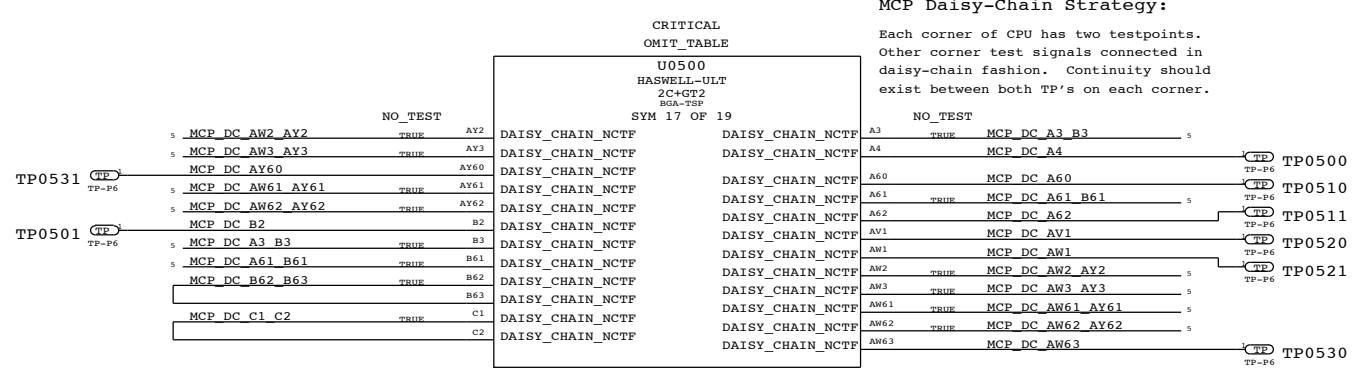
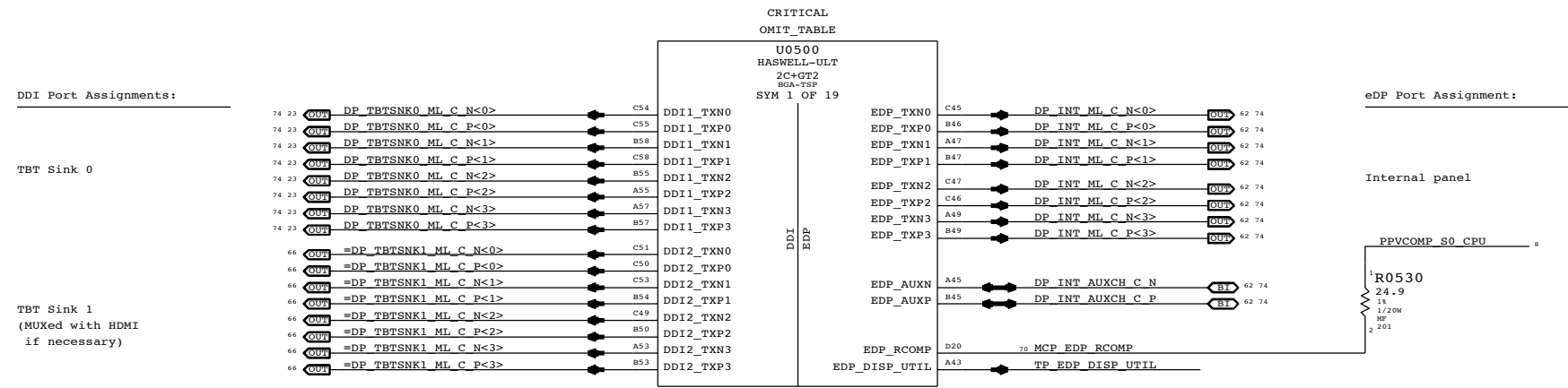
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SYNC MASTER=144 SYNC DATE=08/12/2013

CPU GFX/NCTF/RSVD

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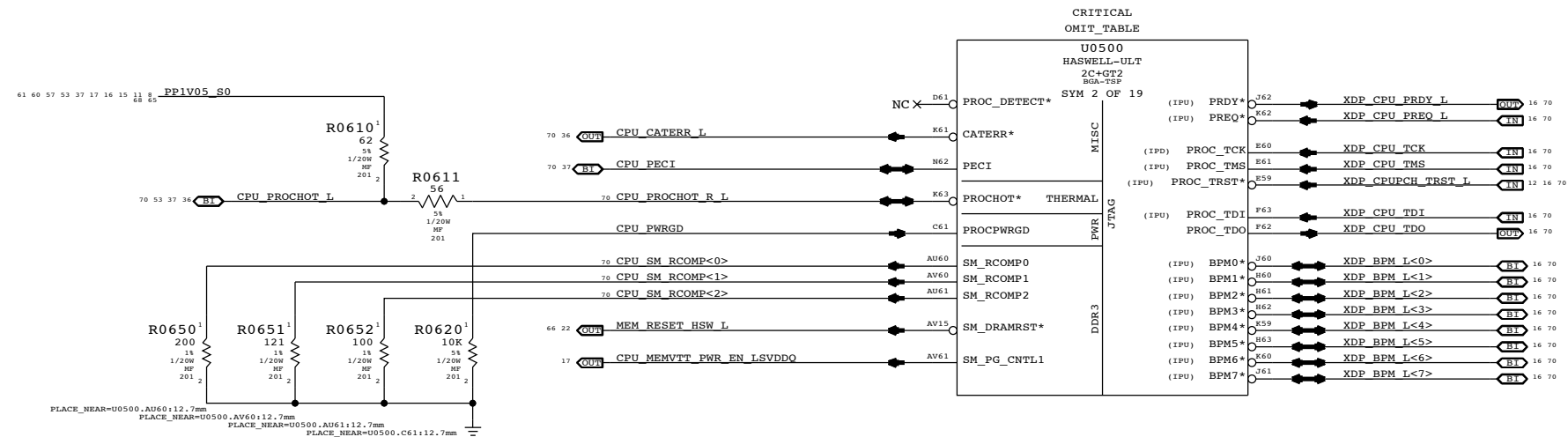
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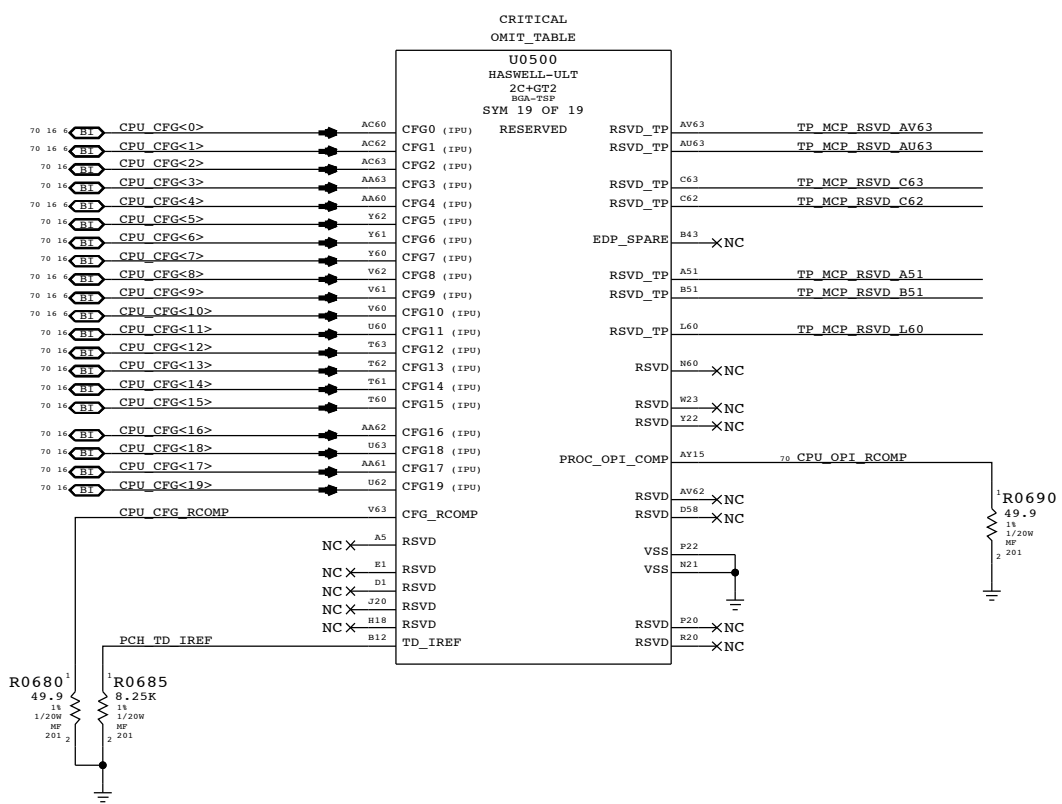
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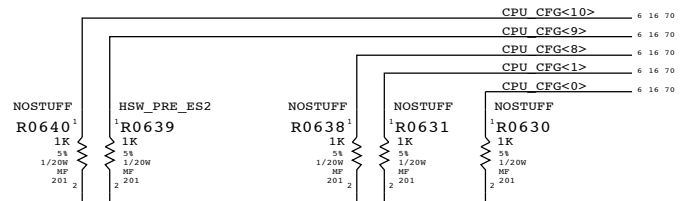


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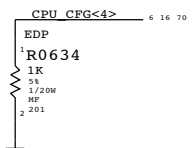
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CFG<10>:SAFE MODE BOOT 1 = NORMAL OPERATION 0 = POWER FEATURES NOT ACTIVE
 CFG<9> :NO SVID-CAPABLE VR 1 = VR SUPPORTS SVID 0 = VR DOES NOT SUPPORT SVID
 CFG<8> :ALLOW NOA ON LOCKED UNITS 1 = NORMAL OPERATION 0 = NOA ALWAYS UNLOCKED
 CFG<4> :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
 CFG<1> :PCH-LESS MODE 1 = NORMAL OPERATION 0 = PCH-LESS MODE
 CFG<0> :RESET SEQUENCE STALL 1 = NORMAL OPERATION 0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800 and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



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8 7 6 5 4 3 2 1

SYNC MASTER=J44 SYNC DATE=08/12/2013
 PAGE TITLE
CPU Misc/JTAG/CFG/RSVD
 Apple Inc.
 DRAWING NUMBER <SCH_NUM> SIZE D
 REVISION <E4LABEL>
 BRANCH <BRANCH>
 PAGE 6 OF 120
 SHEET 6 OF 78
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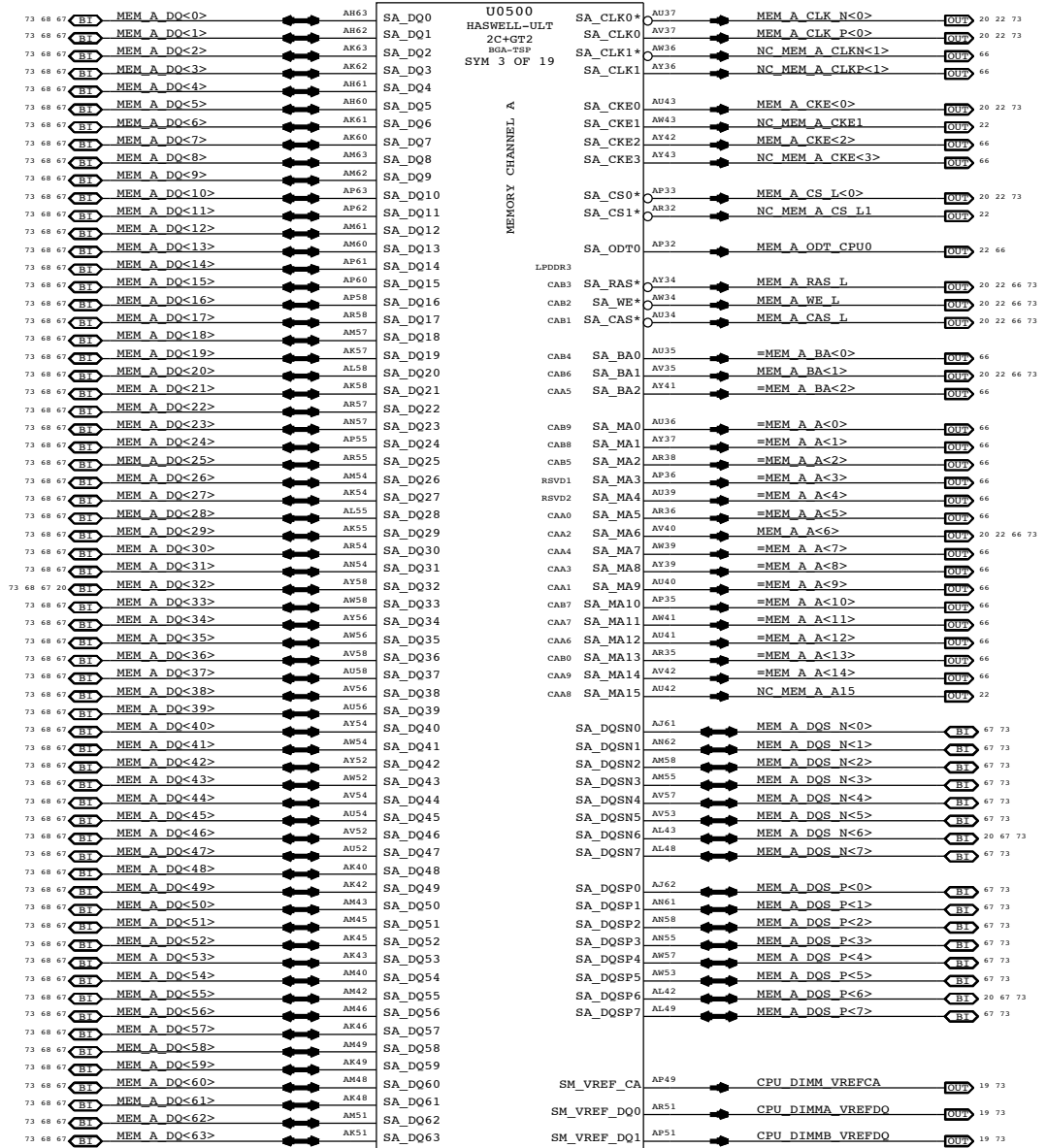
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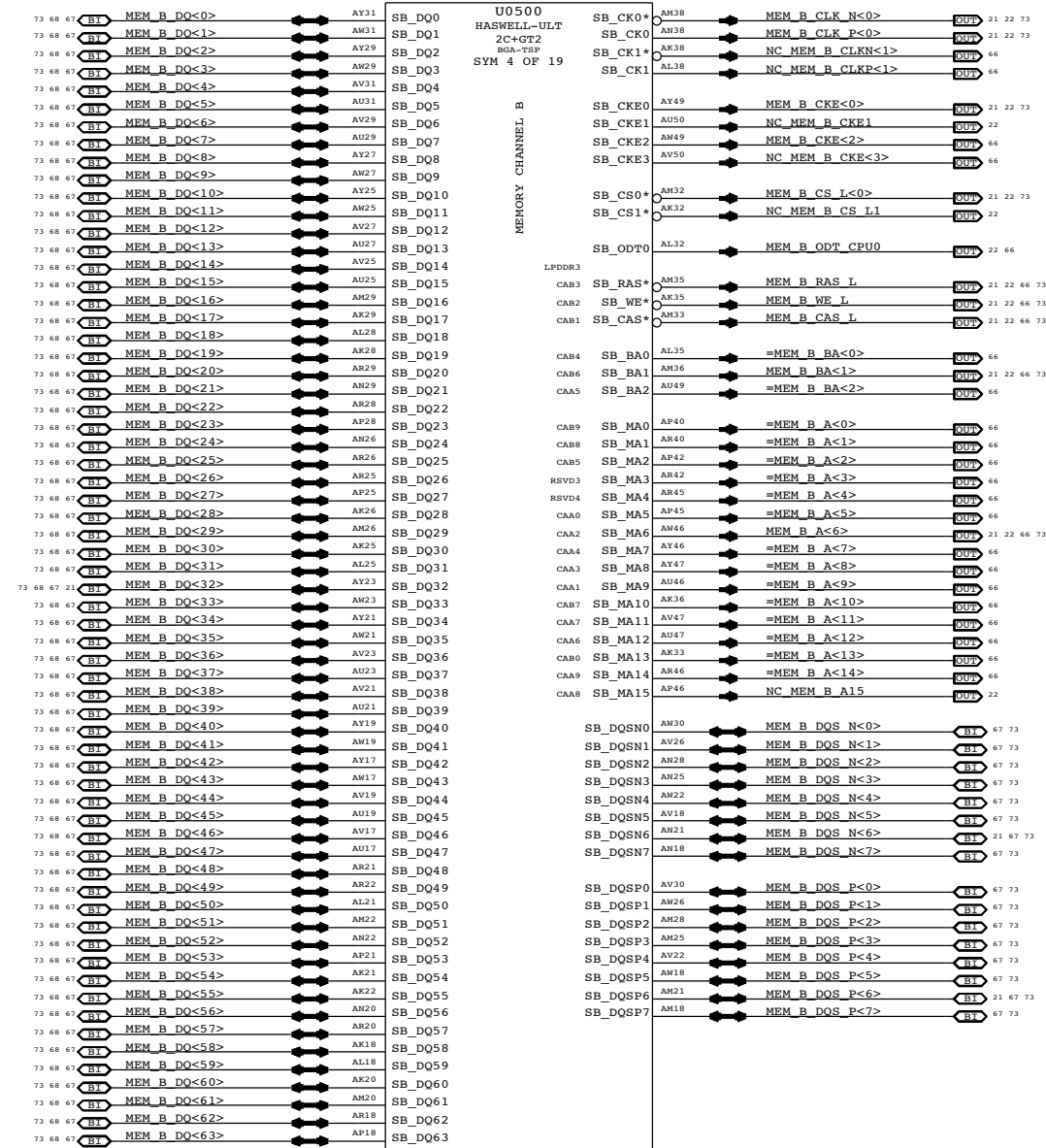
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CRITICAL OMIT_TABLE



CRITICAL OMIT_TABLE



SYNC MASTER=144 SYNC DATE=08/12/2013

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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SHEET 7 OF 78

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HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

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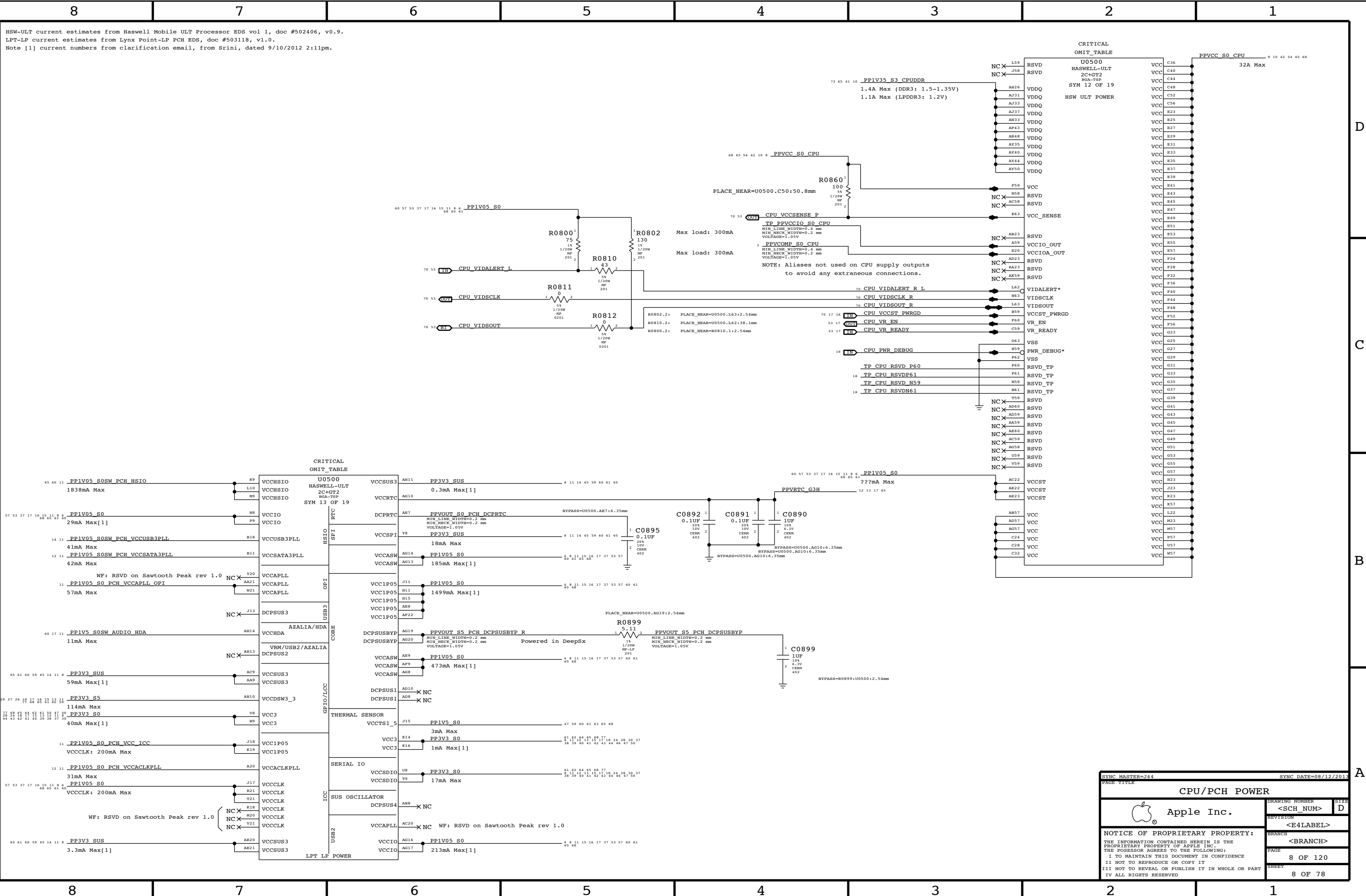
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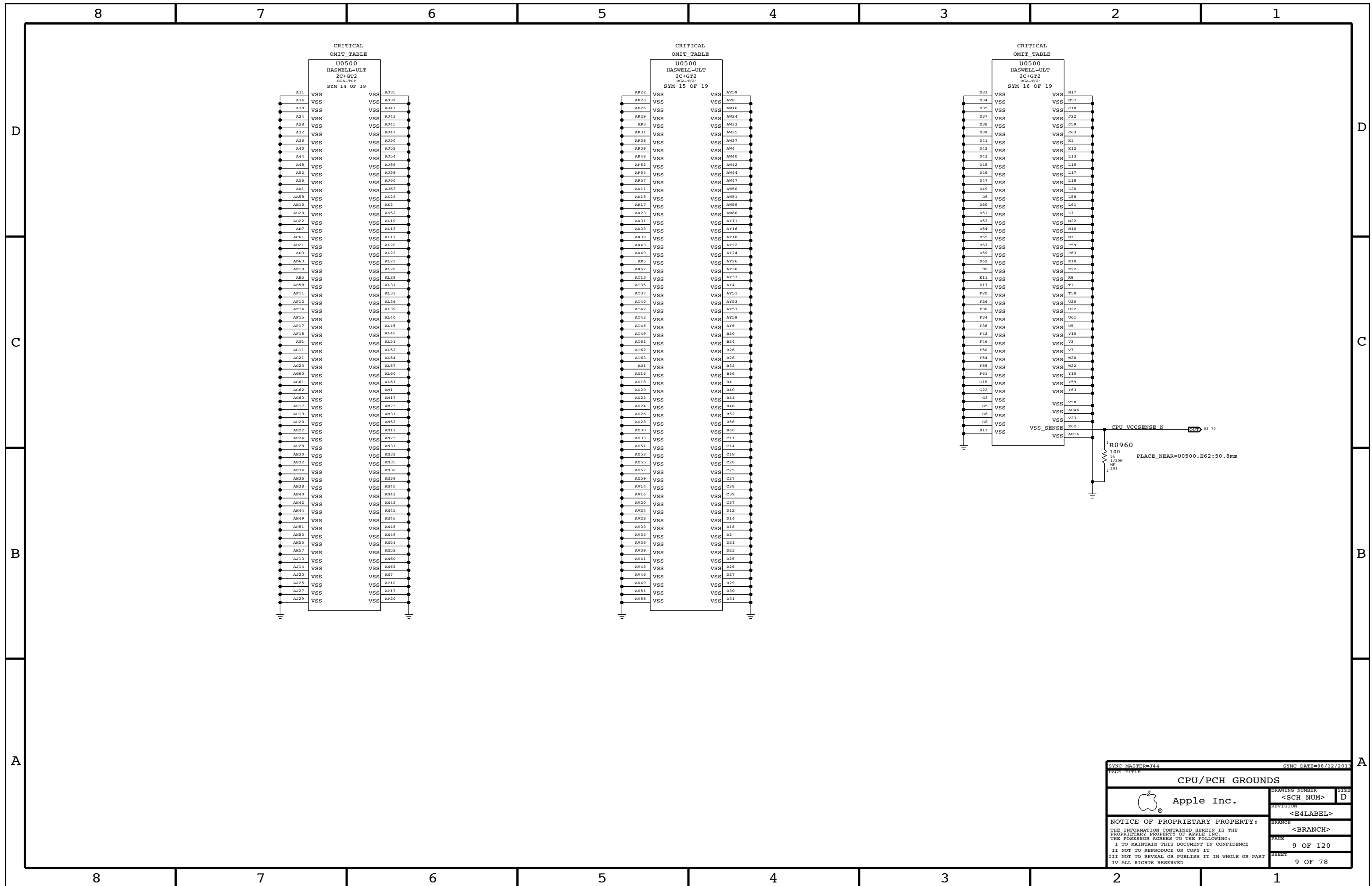
CRITICAL OMIT_TABLE		U0500 HASWELL-ULT 2C+GT2 BGA-TSP SYM 12 OF 19 HSW ULT POWER	PPVCC S0 CPU 8 10 42 54 65 68
C36	VCC	VCC	32A Max
C40	VCC	VCC	
C44	VCC	VCC	
C48	VCC	VCC	
C52	VCC	VCC	
C56	VCC	VCC	
E23	VCC	VCC	
E25	VCC	VCC	
E27	VCC	VCC	
E29	VCC	VCC	
E31	VCC	VCC	
E33	VCC	VCC	
E35	VCC	VCC	
E37	VCC	VCC	
E39	VCC	VCC	
E41	VCC	VCC	
E43	VCC	VCC	
E45	VCC	VCC	
E47	VCC	VCC	
E49	VCC	VCC	
E51	VCC	VCC	
E53	VCC	VCC	
E55	VCC	VCC	
E57	VCC	VCC	
F24	VCC	VCC	
F28	VCC	VCC	
F32	VCC	VCC	
F36	VCC	VCC	
F40	VCC	VCC	
F44	VCC	VCC	
F48	VCC	VCC	
F52	VCC	VCC	
F56	VCC	VCC	
G23	VCC	VCC	
G25	VCC	VCC	
G27	VCC	VCC	
G29	VCC	VCC	
G31	VCC	VCC	
G33	VCC	VCC	
G35	VCC	VCC	
G37	VCC	VCC	
G39	VCC	VCC	
G41	VCC	VCC	
G43	VCC	VCC	
G45	VCC	VCC	
G47	VCC	VCC	
G49	VCC	VCC	
G51	VCC	VCC	
G53	VCC	VCC	
G55	VCC	VCC	
H23	VCC	VCC	
J23	VCC	VCC	
K23	VCC	VCC	
K57	VCC	VCC	
L22	VCC	VCC	
M23	VCC	VCC	
M57	VCC	VCC	
P57	VCC	VCC	
U57	VCC	VCC	
V57	VCC	VCC	

SYNC MASTER=J44 SYNC DATE=08/12/2013

PAGE TITLE: CPU/PCH POWER

DRAWING NUMBER	SIZE
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REVISION	
<E4LABEL>	
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<BRANCH>	
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SYNC MASTER=144		SYNC DATE=08/12/2013	
CPU/PCH GROUNDS			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	<E4LABEL>
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		PAGE	9 OF 120
		SHEET	9 OF 78

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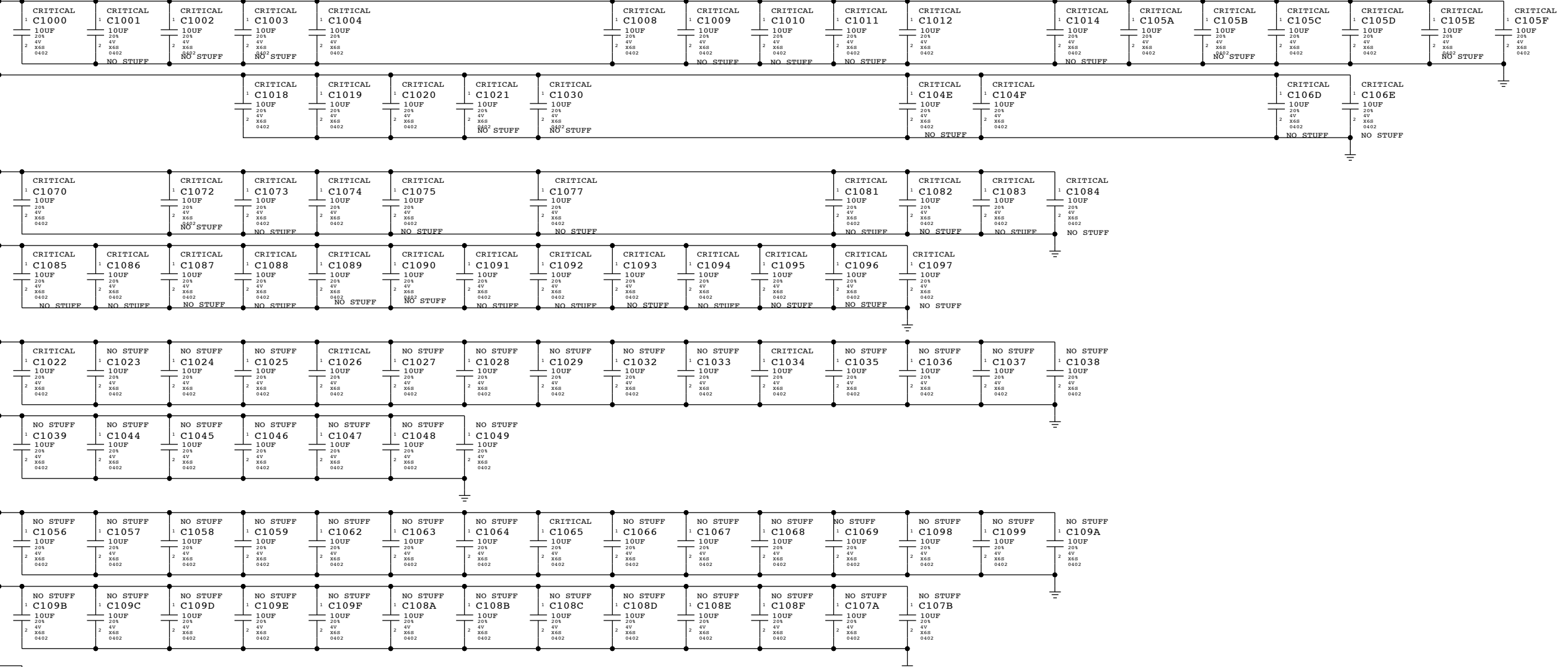
1

All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff

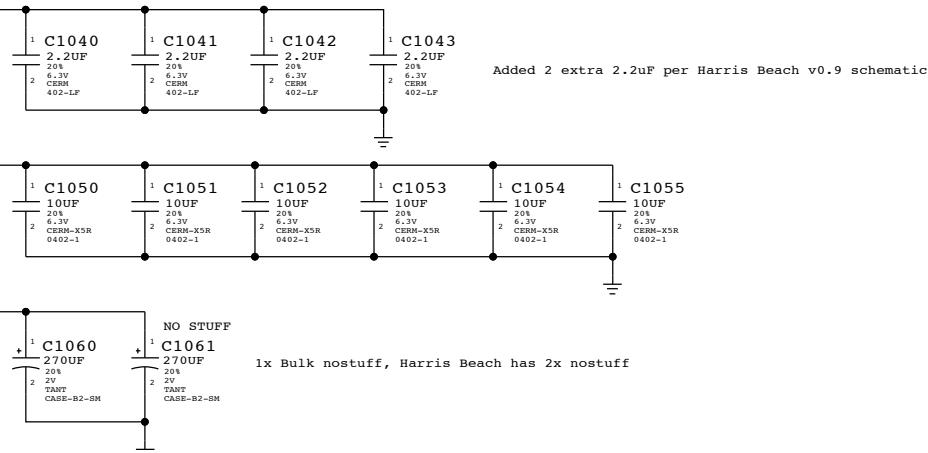
68 65 54 42 8_PPVCC_S0_CPU



CPU VDDQ DECOUPLING

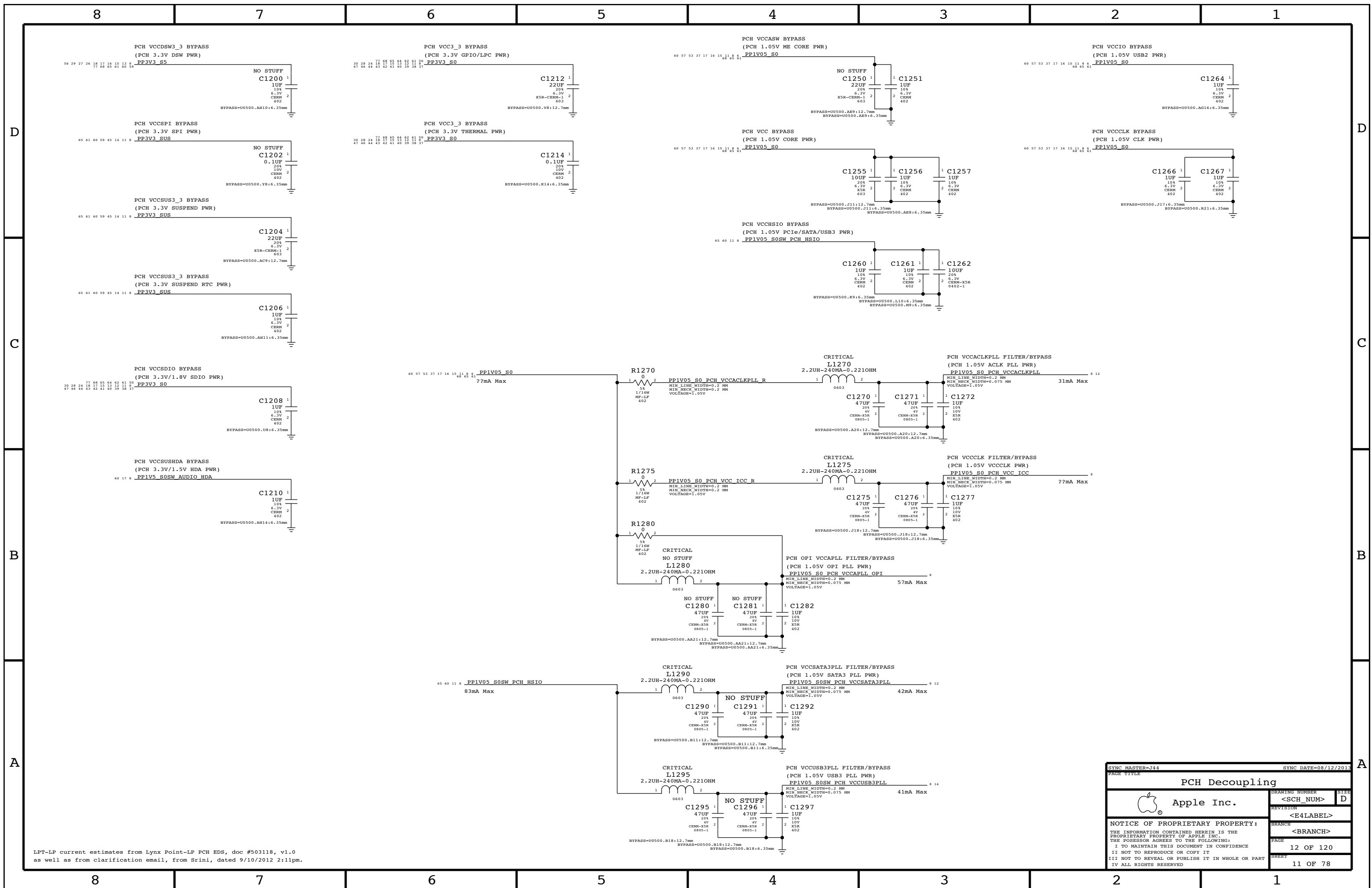
Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

73 65 41 8_PP1V35_S3_CPUDDR



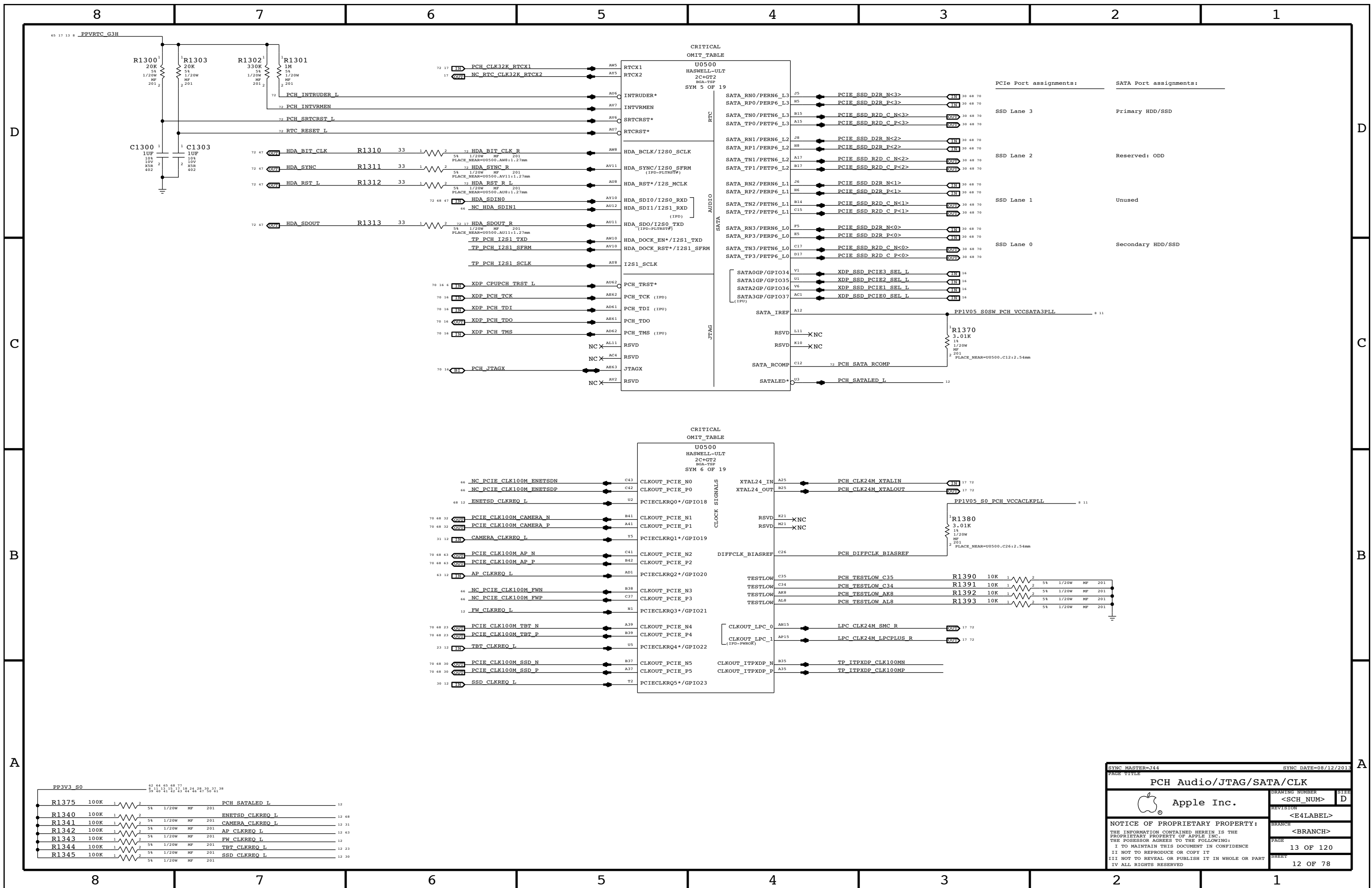
CPU VCC Decoupling

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CPU Decoupling			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		<BRANCH>	
		PAGE	10 OF 120
		SHEET	10 OF 78



LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0 as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

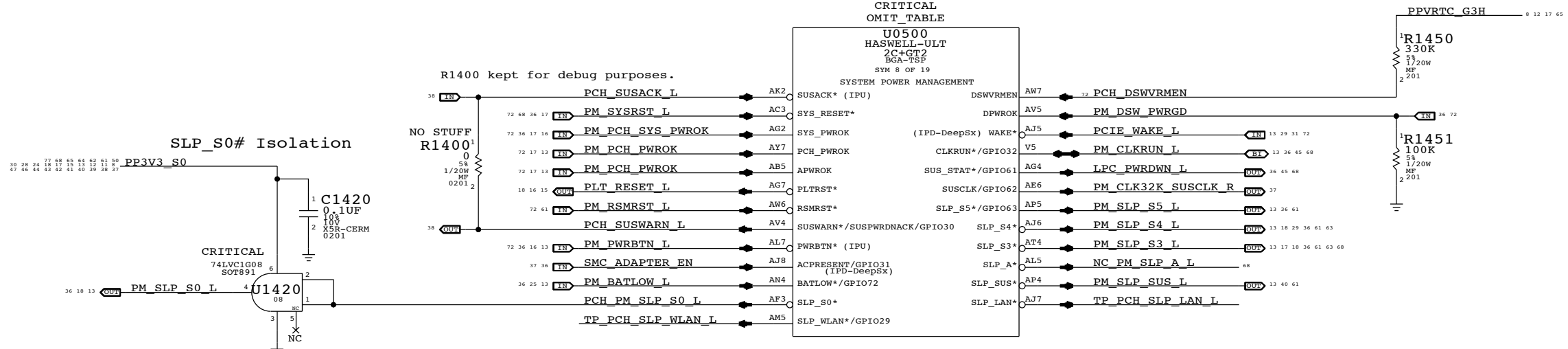
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PAGE TITLE			
PCH Decoupling		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
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		BRANCH	<BRANCH>
		PAGE	12 OF 120
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SYNC MASTER=144 SYNC DATE=08/12/2013
 PAGE TITLE
PCH Audio/JTAG/SATA/CLK
 Apple Inc.
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 REVISION: <E4LABEL>
 BRANCH: <BRANCH>
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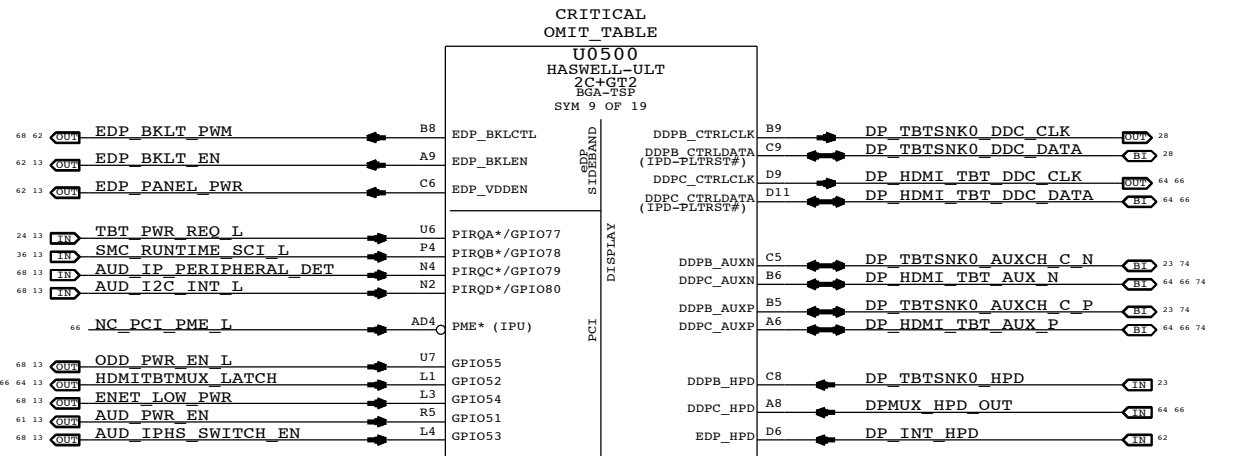
8 7 6 5 4 3 2 1

D

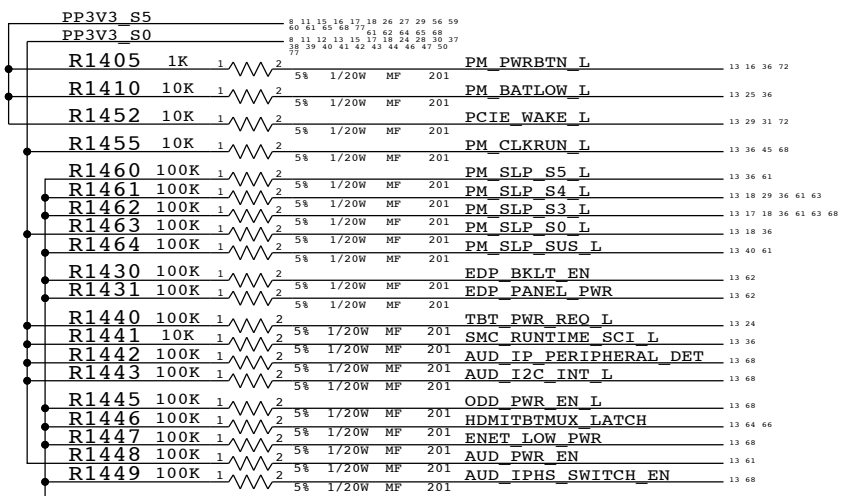


SLP_S0# can be driven high outside of S0 U1420 ensures signal will only be high in S0.

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SYNC MASTER=J44 SYNC DATE=08/12/2013

PCH PM/PCI/GFX

Apple Inc.

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DRAWING NUMBER <SCH_NUM> D

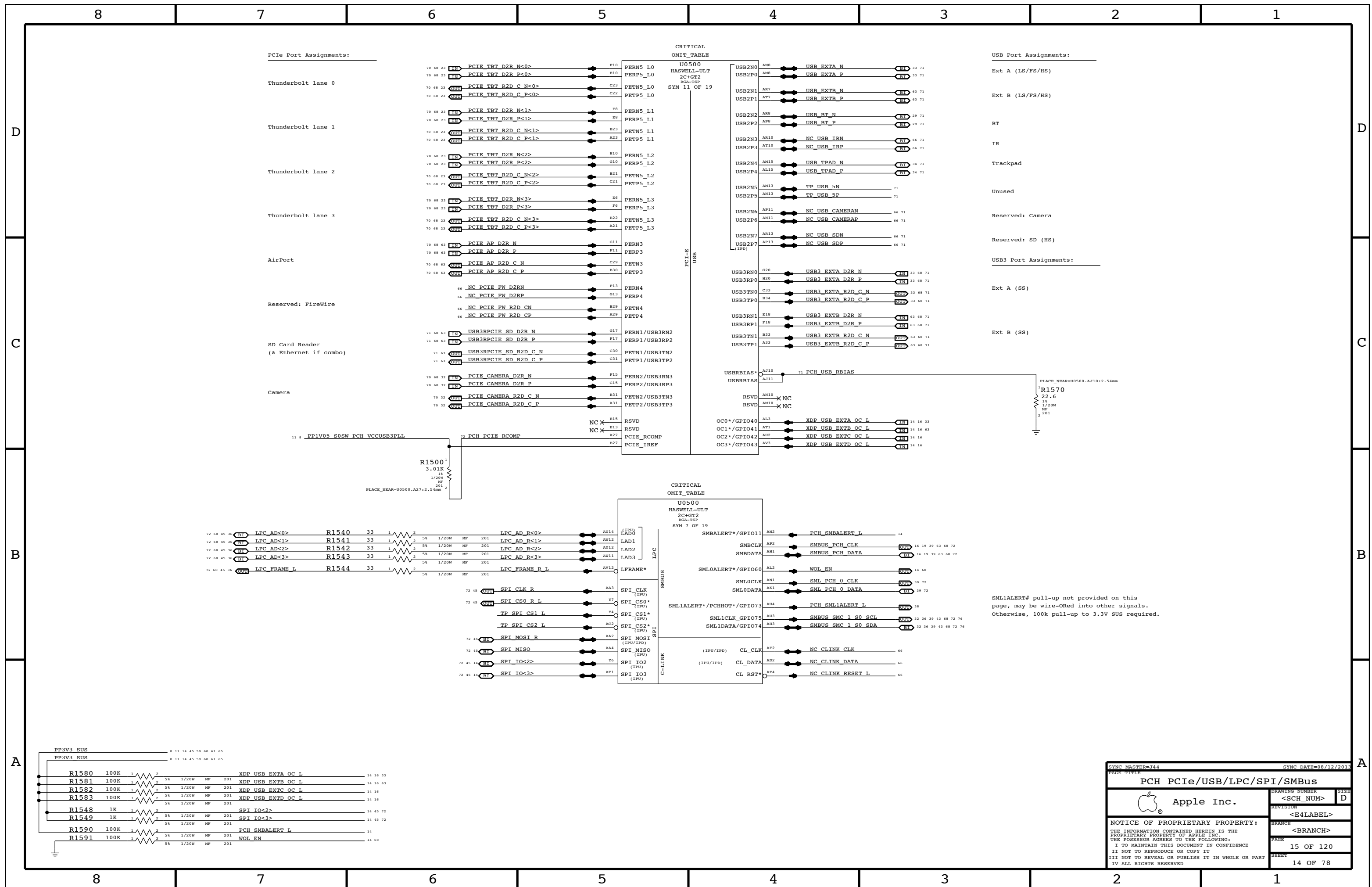
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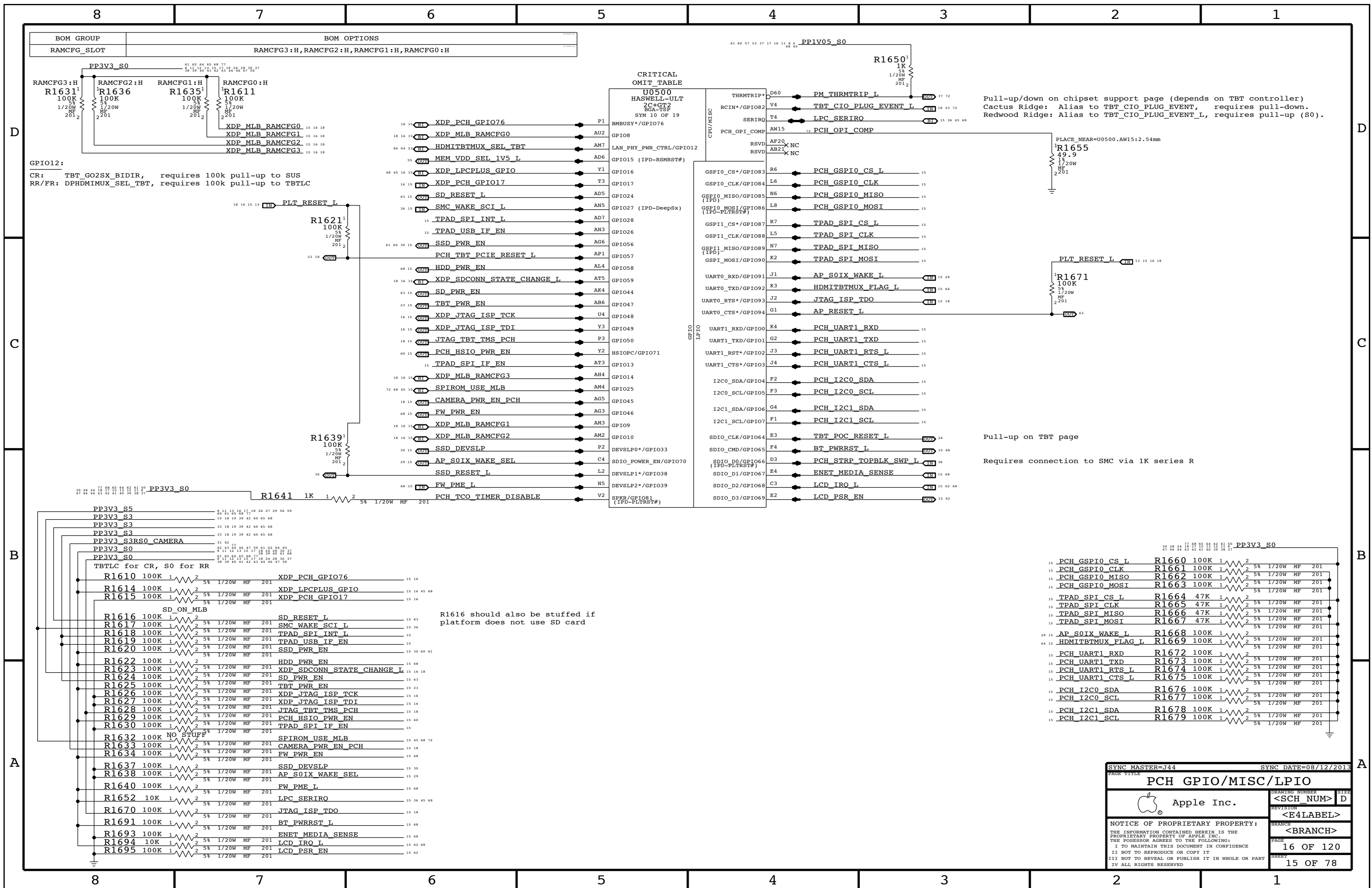
SHEET 13 OF 78

8 7 6 5 4 3 2 1



SML1ALERT# pull-up not provided on this page, may be wire-Ored into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
PCH PCIe/USB/LPC/SPI/SMBus			
DRAWING NUMBER		SIZE	
<SCH_NUM>		D	
REVISION		<E4LABEL>	
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

CRITICAL OMIT TABLE

U0500 HASWELL-ULT	2C+CP2 BGA-TSF	SYM 10 OF 19
BMBUSY*/GPIO76		
GPIO8		
LAN_PHY_PWR_CTRL/GPIO12		
GPIO15 (IPD-RSMRST#)		
GPIO16		
GPIO17		
GPIO24		
GPIO27 (IPD-DeepSx)		
GPIO28		
GPIO26		
GPIO56		
GPIO57		
GPIO58		
GPIO59		
GPIO44		
GPIO47		
GPIO48		
GPIO49		
GPIO50		
HSIOPC/GPIO71		
GPIO13		
GPIO14		
GPIO25		
GPIO45		
GPIO46		
GPIO9		
GPIO10		
DEVSLP0*/GPIO33		
SDIO_POWER_EN/GPIO70		
DEVSLP1*/GPIO38		
DEVSLP2*/GPIO39		
SPKR/GPIO81 (LPD-PLTRST#)		

THRMTrip*	D60	PM_THRMTrip_L	15 37 72
RCIN*/GPIO82	V4	TBT_CIO_PLUG_EVENT_L	18 23 72
SERIRO	T4	LPC_SERIRO	15 36 45 68
PCH_OPI_COMP	AW15	PCH_OPI_COMP	
RSVD	AF20	XNC	
RSVD	AB21	XNC	
GPIO103	R6	PCH_GSPI0_CS_L	15
GPIO104	L6	PCH_GSPI0_CLK	15
GPIO105	N6	PCH_GSPI0_MISO	15
GPIO106	L8	PCH_GSPI0_MOSI	15
GPIO107	R7	TPAD_SPI_CS_L	15
GPIO108	L5	TPAD_SPI_CLK	15
GPIO109	N7	TPAD_SPI_MISO	15
GPIO110	K2	TPAD_SPI_MOSI	15
GPIO111	J1	AP_SOIX_WAKE_L	15 29
GPIO112	K3	HDMITBTMUX_FLAG_L	15 64
GPIO113	J2	JTAG_ISP_TDO	15 18
GPIO114	G1	AP_RESET_L	
GPIO115	K4	PCH_UART1_RXD	15
GPIO116	G2	PCH_UART1_TXD	15
GPIO117	J3	PCH_UART1_RTS_L	15
GPIO118	J4	PCH_UART1_CTS_L	15
GPIO119	F2	PCH_I2C0_SDA	15
GPIO120	F3	PCH_I2C0_SCL	15
GPIO121	G4	PCH_I2C1_SDA	15
GPIO122	F1	PCH_I2C1_SCL	15
GPIO123	E3	TBT_POC_RESET_L	24
GPIO124	F4	BT_PWRST_L	15 68
GPIO125	D3	PCH_STRP_TOPBLK_SWP_L	15 38
GPIO126	E4	ENET_MEDIA_SENSE	15 68
GPIO127	C3	LCD_IRO_L	15 62 68
GPIO128	E2	LCD_PSR_EN	15 62

Pull-up/down on chipset support page (depends on TBT controller)
 Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
 Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

Pull-up on TBT page
 Requires connection to SMC via 1K series R

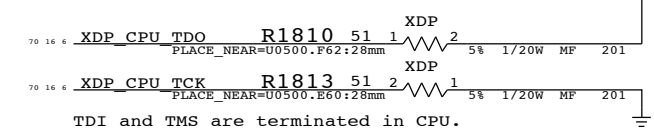
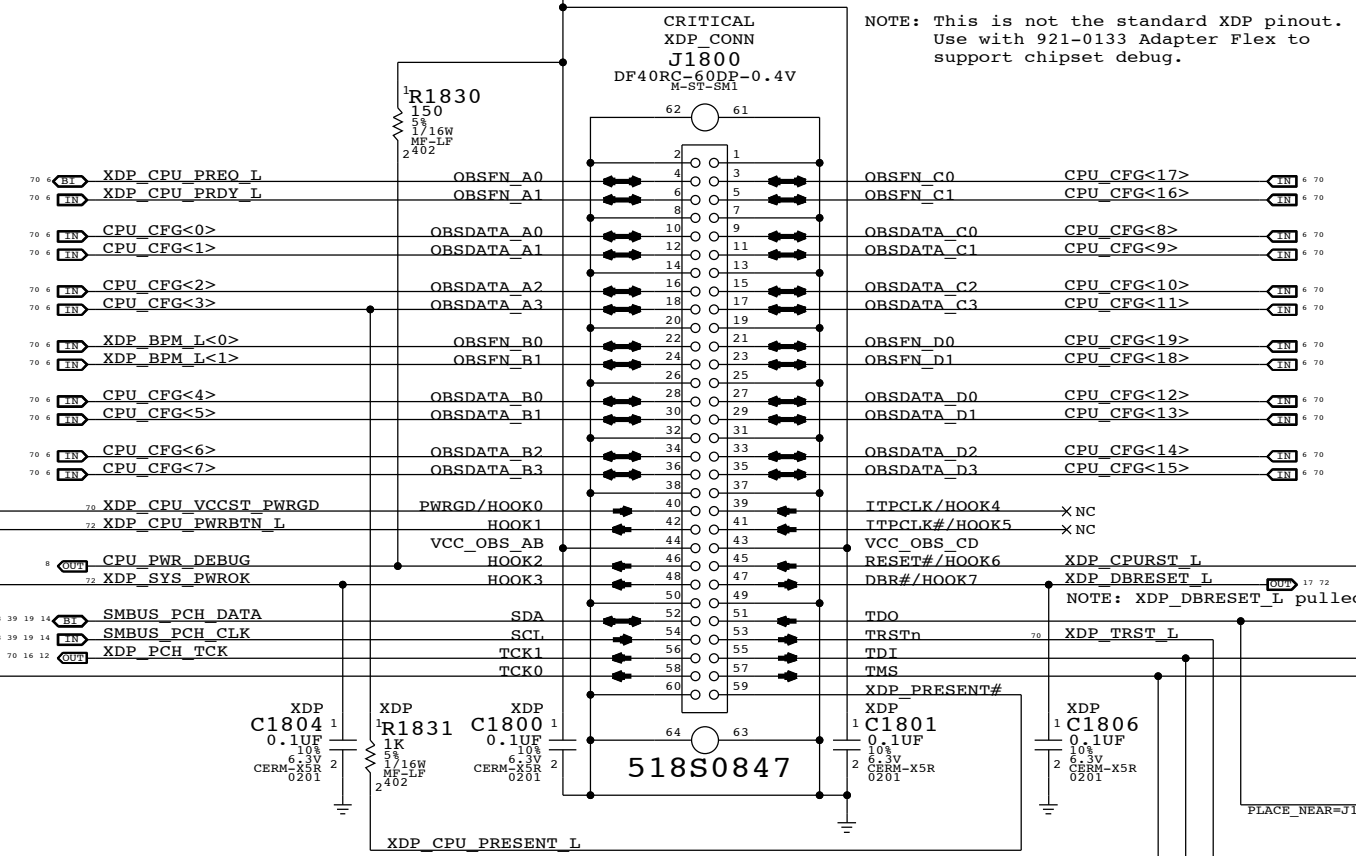
PP3V3_S0	30 28 24 72 68 65 62 61 50
PP3V3_S5	8 11 12 16 17 18 26 27 29 36 39
PP3V3_S3	60 61 65 68 77
PP3V3_S3	15 18 19 39 42 60 65 68
PP3V3_S3	15 18 19 39 42 60 65 68
PP3V3_S3RS0_CAMERA	31 42
PP3V3_S0	42 43 44 46 47 50 61 62 64 65
PP3V3_S0	8 11 12 13 15 17 38 39 40 41 42
PP3V3_S0	8 11 12 13 15 17 38 39 40 41 42
TBTLC for CR, S0 for RR	8 11 12 13 15 17 38 39 40 41 42
R1610	100K 1 2 5% 1/20W MF 201
R1614	100K 1 2 5% 1/20W MF 201
R1615	100K 1 2 5% 1/20W MF 201
R1616	100K 1 2 5% 1/20W MF 201
R1617	100K 1 2 5% 1/20W MF 201
R1618	100K 1 2 5% 1/20W MF 201
R1619	100K 1 2 5% 1/20W MF 201
R1620	100K 1 2 5% 1/20W MF 201
R1622	100K 1 2 5% 1/20W MF 201
R1623	100K 1 2 5% 1/20W MF 201
R1624	100K 1 2 5% 1/20W MF 201
R1625	100K 1 2 5% 1/20W MF 201
R1626	100K 1 2 5% 1/20W MF 201
R1627	100K 1 2 5% 1/20W MF 201
R1628	100K 1 2 5% 1/20W MF 201
R1629	100K 1 2 5% 1/20W MF 201
R1630	100K 1 2 5% 1/20W MF 201
R1632	100K NO STUFF
R1633	100K 1 2 5% 1/20W MF 201
R1634	100K 1 2 5% 1/20W MF 201
R1637	100K 1 2 5% 1/20W MF 201
R1638	100K 1 2 5% 1/20W MF 201
R1640	100K 1 2 5% 1/20W MF 201
R1652	10K 1 2 5% 1/20W MF 201
R1670	100K 1 2 5% 1/20W MF 201
R1691	100K 1 2 5% 1/20W MF 201
R1693	100K 1 2 5% 1/20W MF 201
R1694	10K 1 2 5% 1/20W MF 201
R1695	100K 1 2 5% 1/20W MF 201

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PCH GPIO/MISC/LPIO			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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Extra BPM Testpoints

- XDP_BPM_L<2> TP1802
- XDP_BPM_L<3> TP1803
- XDP_BPM_L<4> TP1804
- XDP_BPM_L<5> TP1805
- XDP_BPM_L<6> TP1806
- XDP_BPM_L<7> TP1807

Merged (CPU/PCH) Micro2-XDP



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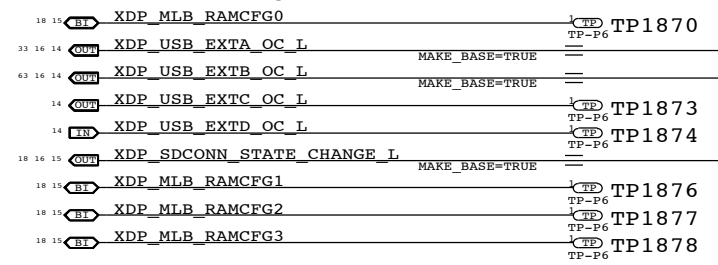
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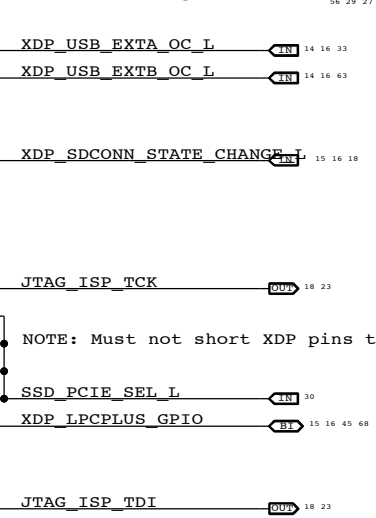
PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

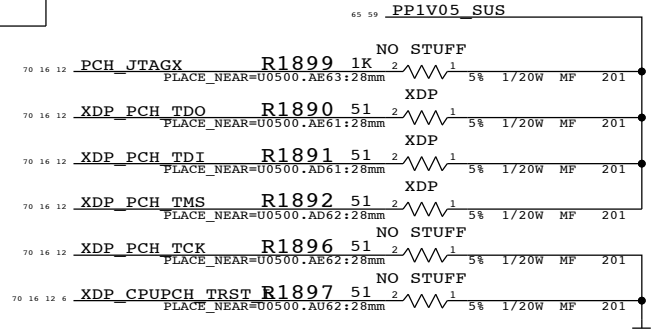
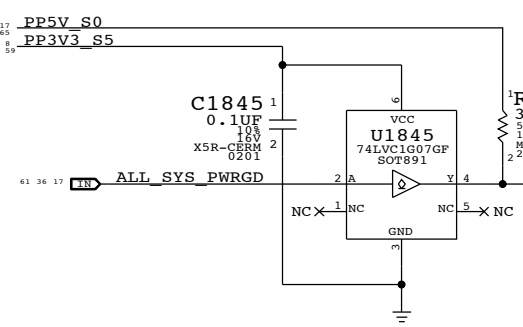
PCH/XDP Signals



Non-XDP Signals



CPU JTAG Isolation



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Unused & MLB_RAMCFGx GPIOs have TPs.
 USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
 SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
 JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
 NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
 SSD_PCIE*_SEL_L straps are connected via 1K to common net.
 LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

SYNC MASTER=J44		SYNC DATE=08/12/2013	
CPU/PCH Merged XDP			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
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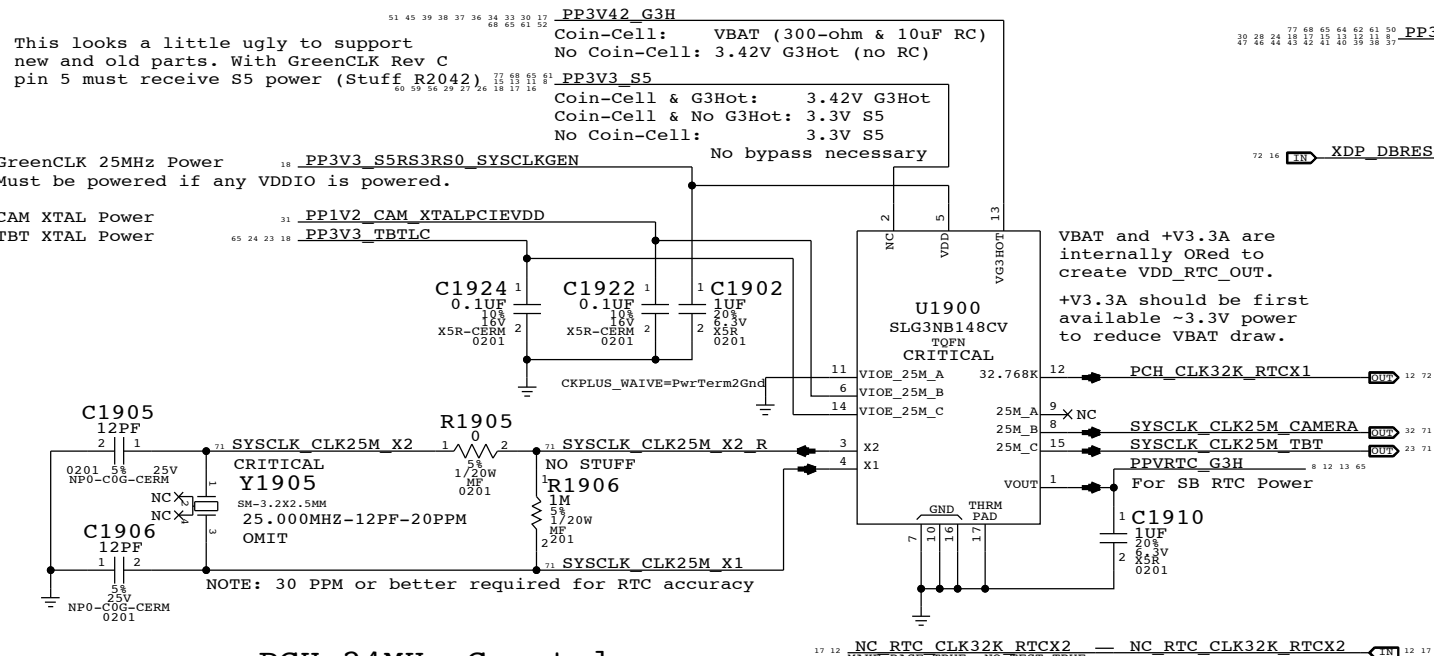
System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

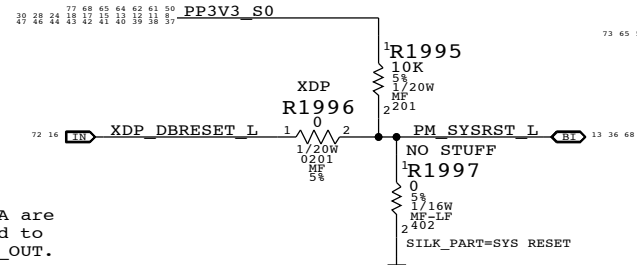
This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042).

GreenCLK 25MHz Power Must be powered if any VDDIO is powered.

CAM XTAL Power
TBT XTAL Power

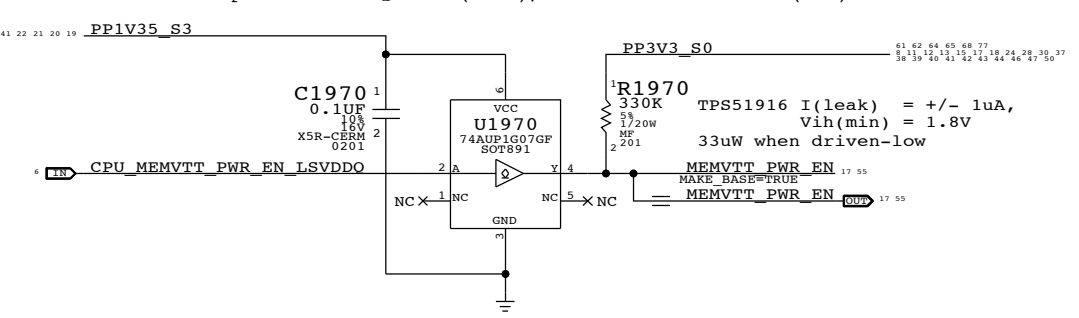


PCH Reset Button

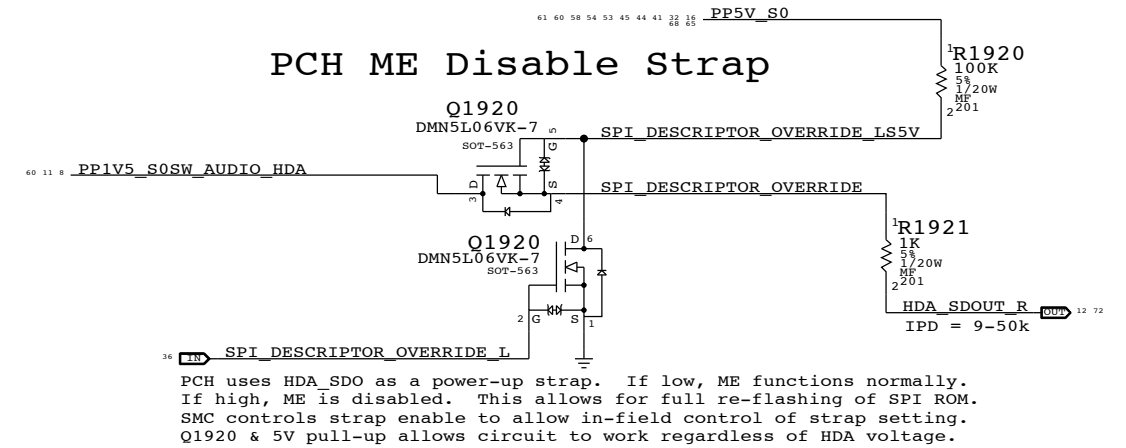


Memory VTT Enable Level-Shifter

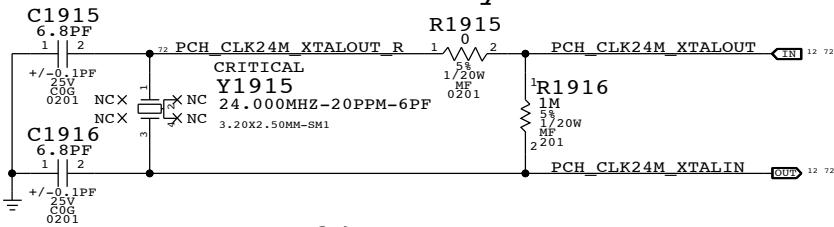
CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).



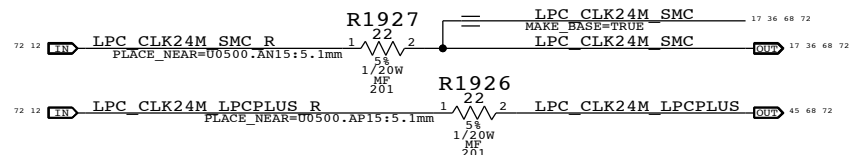
PCH ME Disable Strap



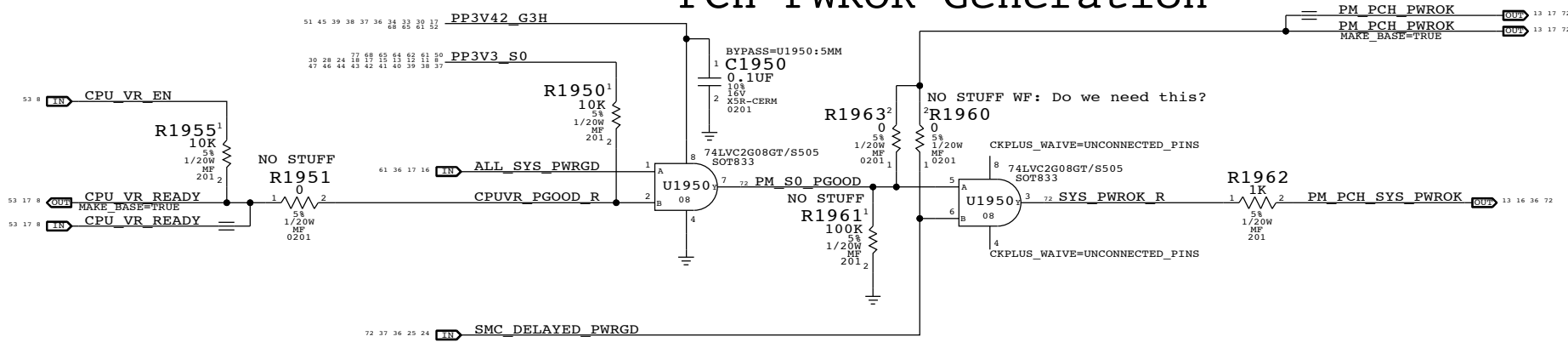
PCH 24MHz Crystal



PCH 24MHz Outputs



PCH PWROK Generation



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL, 25MHZ, 20PPM, 12PF, 3.2X2.5X.6MM, 85C	Y1905		

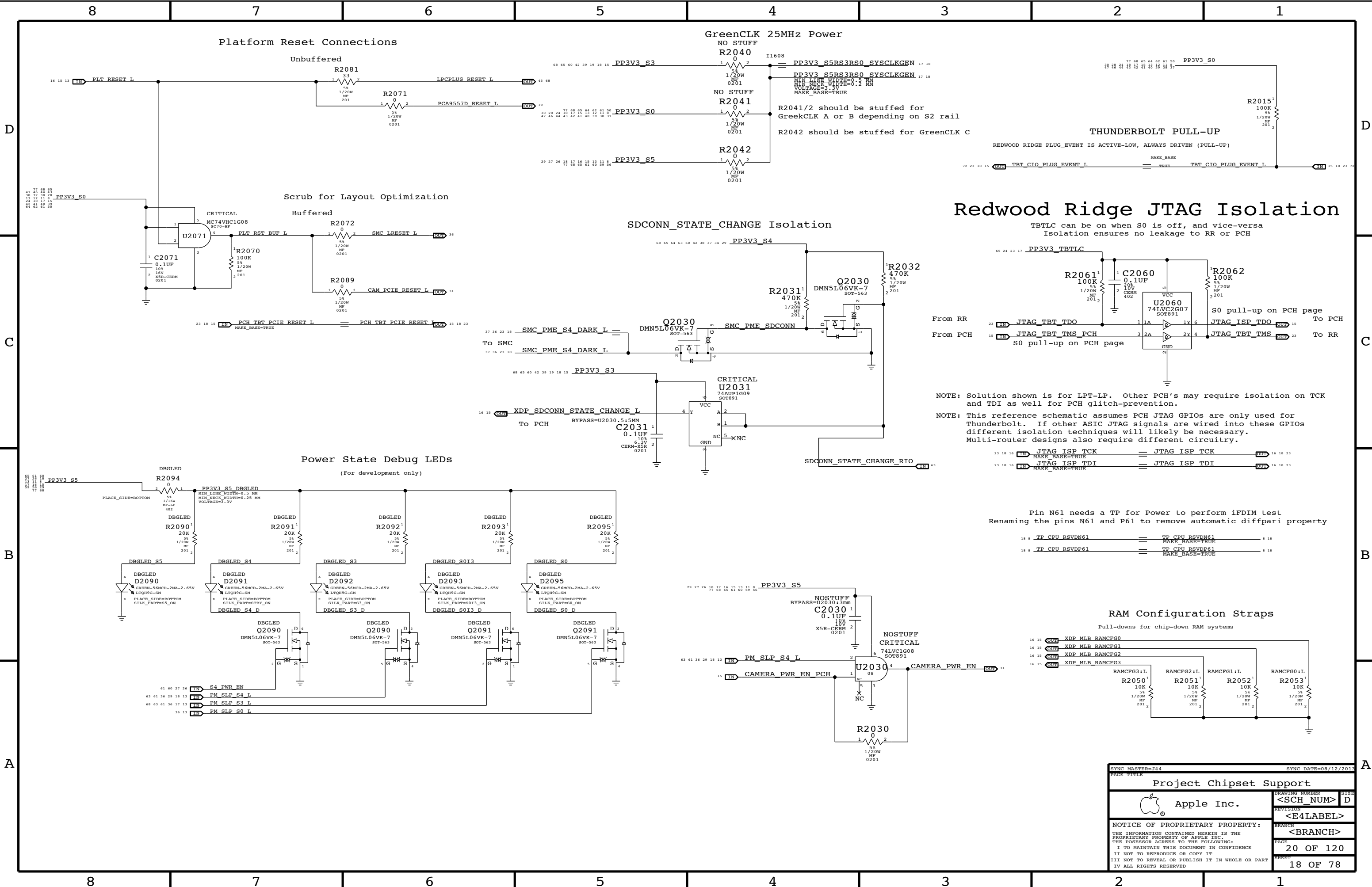
SYNC MASTER=J44 SYNC DATE=08/12/2013

Chipset Support

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Platform Reset Connections

GreenCLK 25MHz Power

THUNDERBOLT PULL-UP

Scrub for Layout Optimization

SDCONN_STATE_CHANGE Isolation

Redwood Ridge JTAG Isolation

Power State Debug LEDs

RAM Configuration Straps

TBTLIC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.
NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.

Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
Project Chipset Support			
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Apple		<SCH NUM>	D
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Page Notes

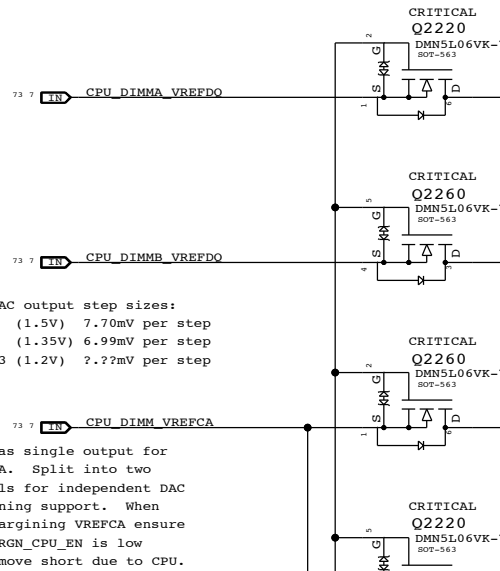
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPDDR_S3_MEMVREF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 - DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining



DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

OMIT

R2218 SHORT

PP3V3_S3 VREFMRGN DAC

MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.3V

DDRREF_DAC C2200 2.2UF

DDRREF_DAC C2201 0.1UF

SMBUS_PCH_CLK

SMBUS_PCH_DATA

Addr=0x98 (WR) / 0x99 (RD)

VDD MSOP

VOUTB

SDA

A0

A1

A2

VOUTD

A1

GND

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRREF_DAC C2202 0.1UF

VCC

U2201 PCA9557

A0

A1

A2

P1

P2

P3

P4

P5

P6

P7

SCL

SDA

THRM PAD

RESET*

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PCA9557D RESET_L

VREFMRGN CPU_EN

VREFMRGN DO A_EN

VREFMRGN DO B_EN

VREFMRGN CA A_EN

VREFMRGN CA B_EN

VREFMRGN MEMVREG_EN

VREFMRGN SPARE_EN

VREFMRGN DO A

VREFMRGN DO B

VREFMRGN CA AB

VREFMRGN MEMVREG

VREFMRGN DO A RDIV

VREFMRGN DO B RDIV

VREFMRGN CA A RDIV

VREFMRGN CA B RDIV

VREFMRGN MEMVREG_BUF

VREFMRGN SPARE_BUF

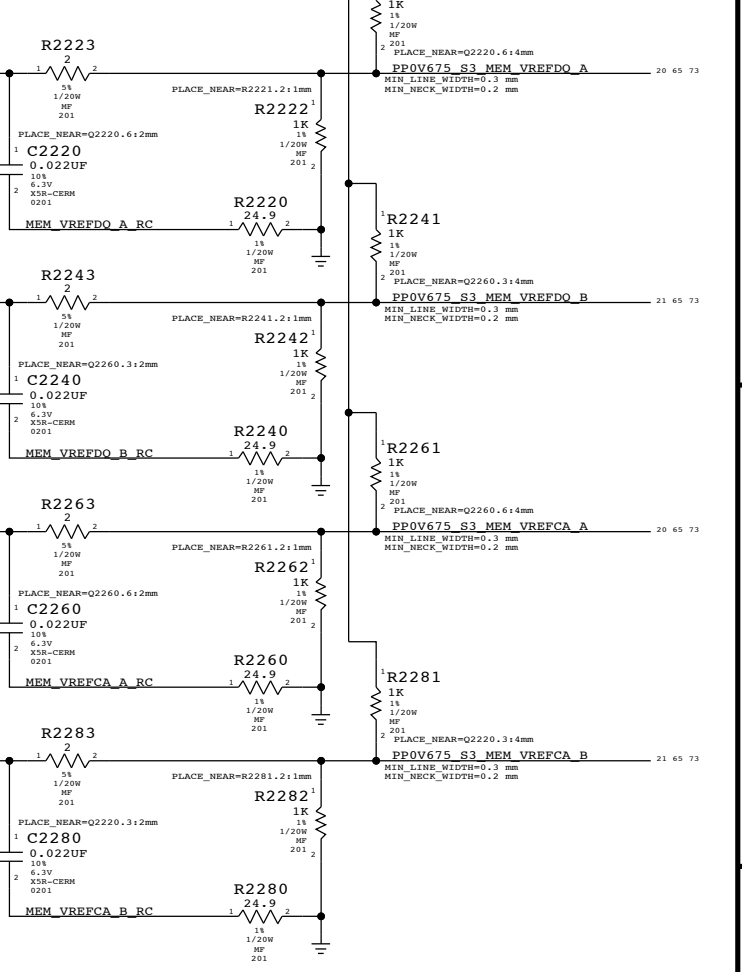
DDRREG_FB

U2204 MAX4253

Pins B1 & B4: CKPLUS_WAIVE=unconnected_pins

VRef Dividers

Always used, regardless of margining option.

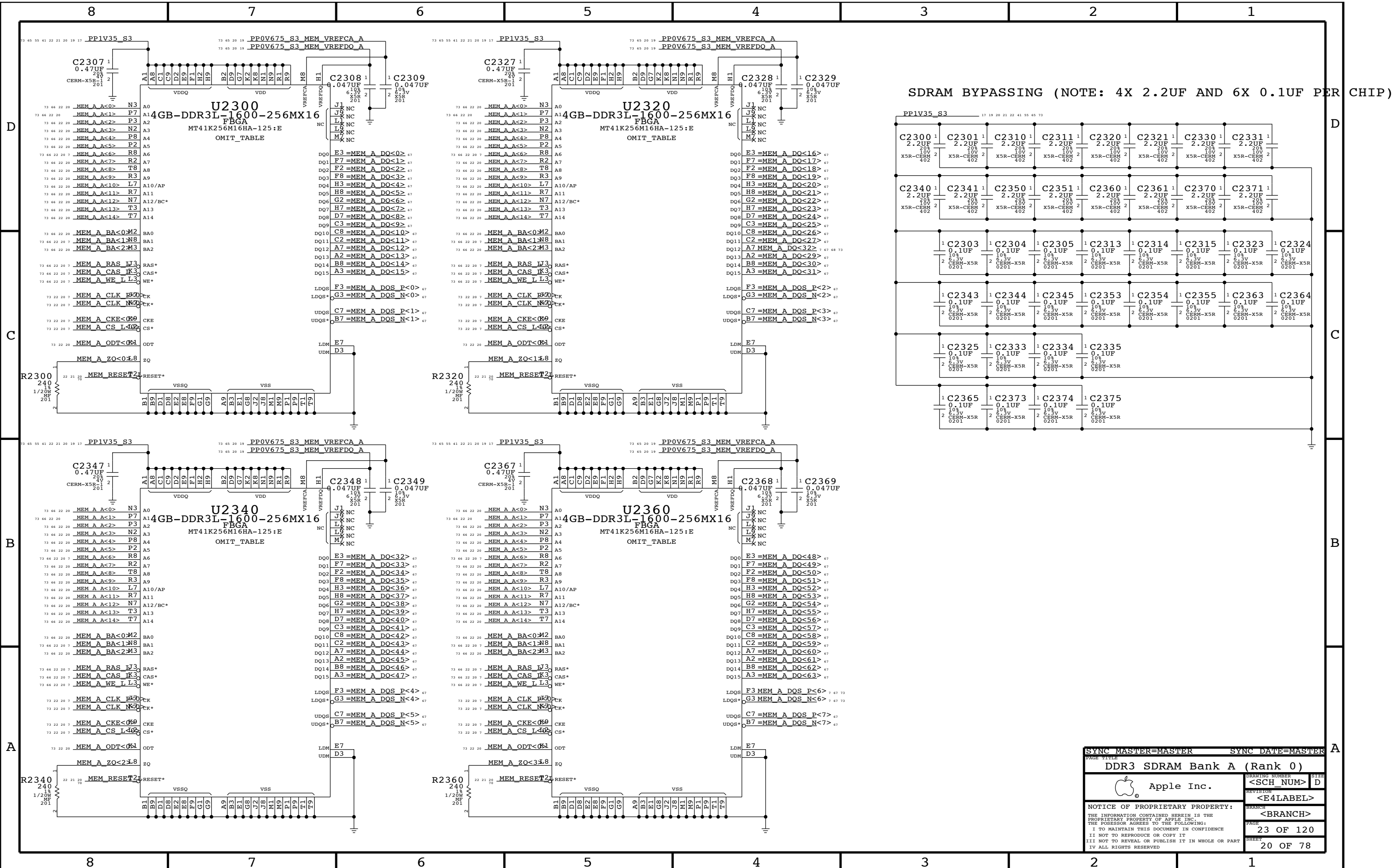


	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
Nominal value	LPDDR3 (1.2V) 0.600V (DAC: 0x2E.5)		DDR3L (1.35V) 0.675V (DAC: 0x34)		LPDDR3 (1.2V) 1.200V (DAC: 0x5D)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0x8A)
Vref current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
 DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

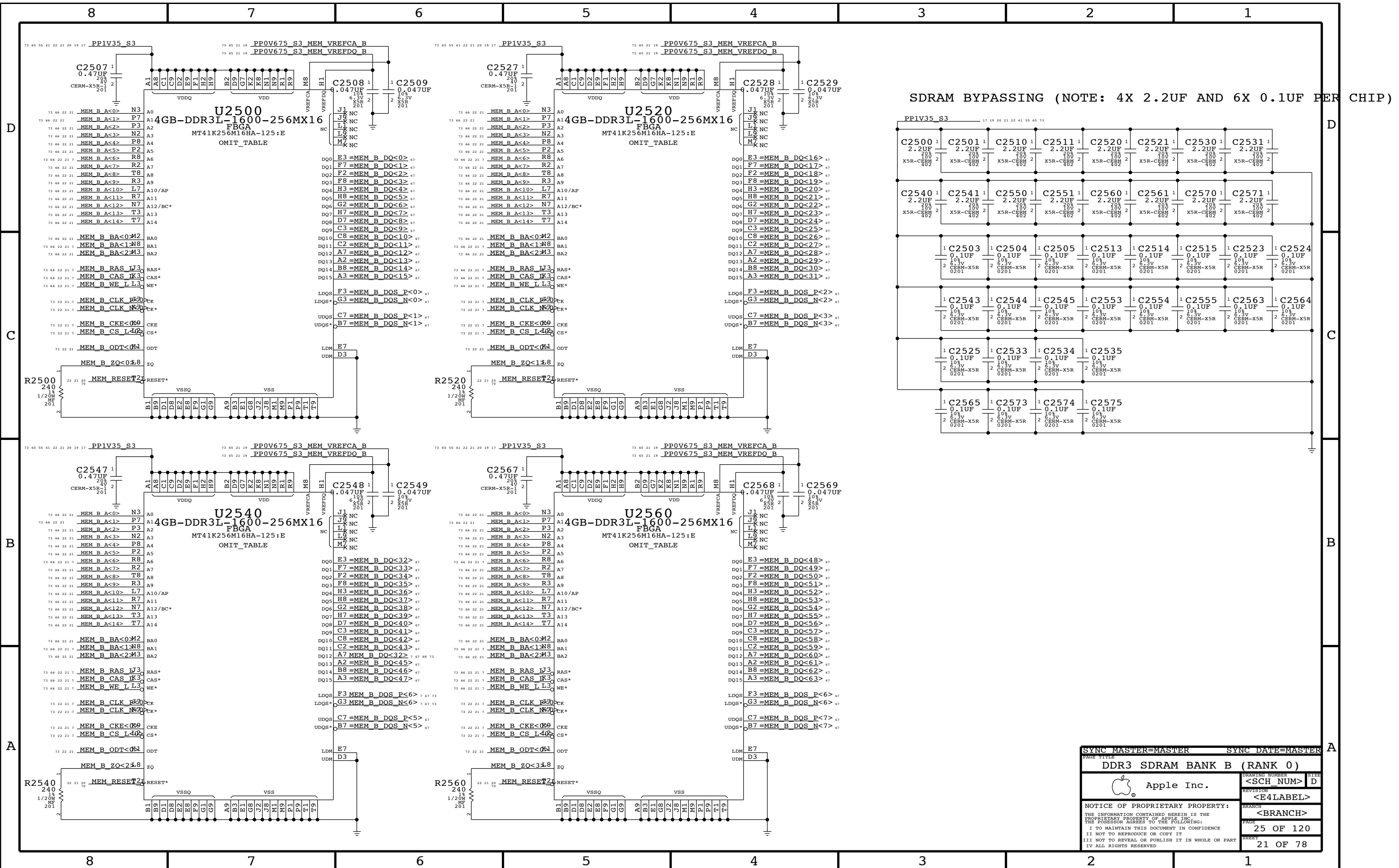
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SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DDR3 SDRAM Bank A (Rank 0)			
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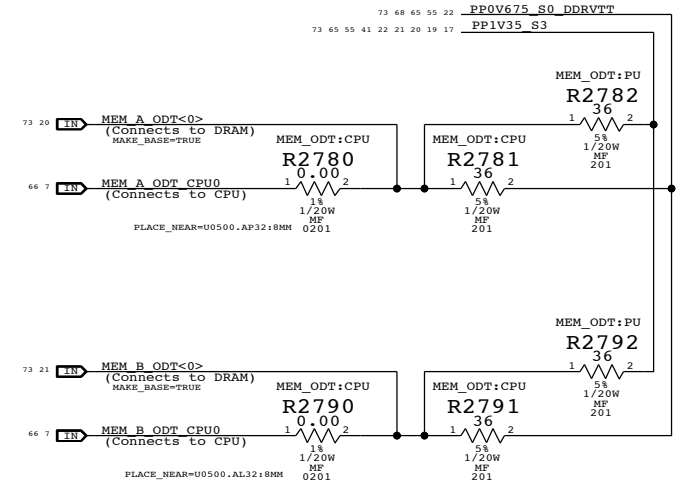
SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

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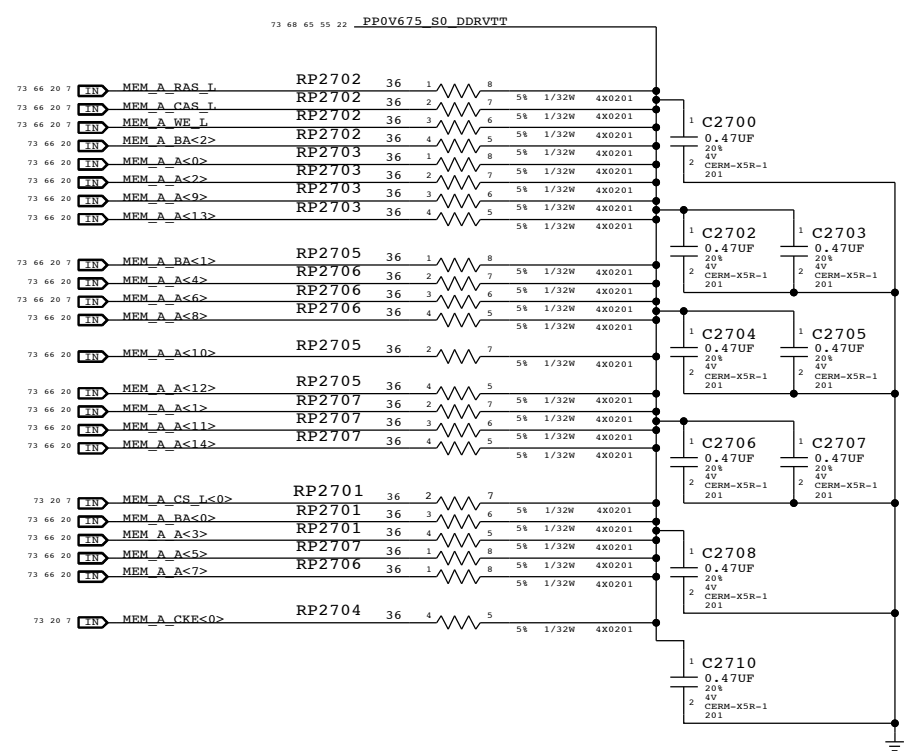
8 7 6 5 4 3 2 1

Memory ODT Option

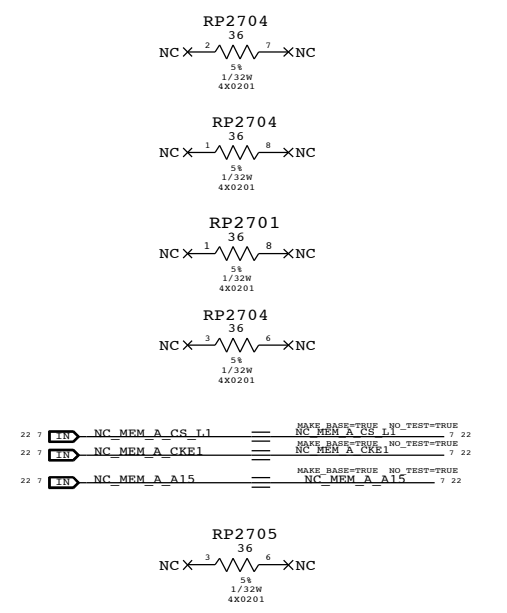
MEM_ODT:CPU drives ODT from CPU, terminated to 0.675V VTT.
MEM_ODT:PU disconnect ODT from CPU, ODT pins on DRAM pulled up to 1.35V VDDQ.



Memory CMD/CTL Termination - Channel A

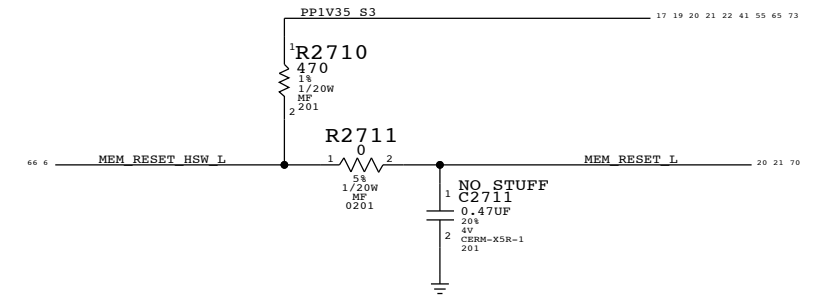


MEMORY RPACK SPARES

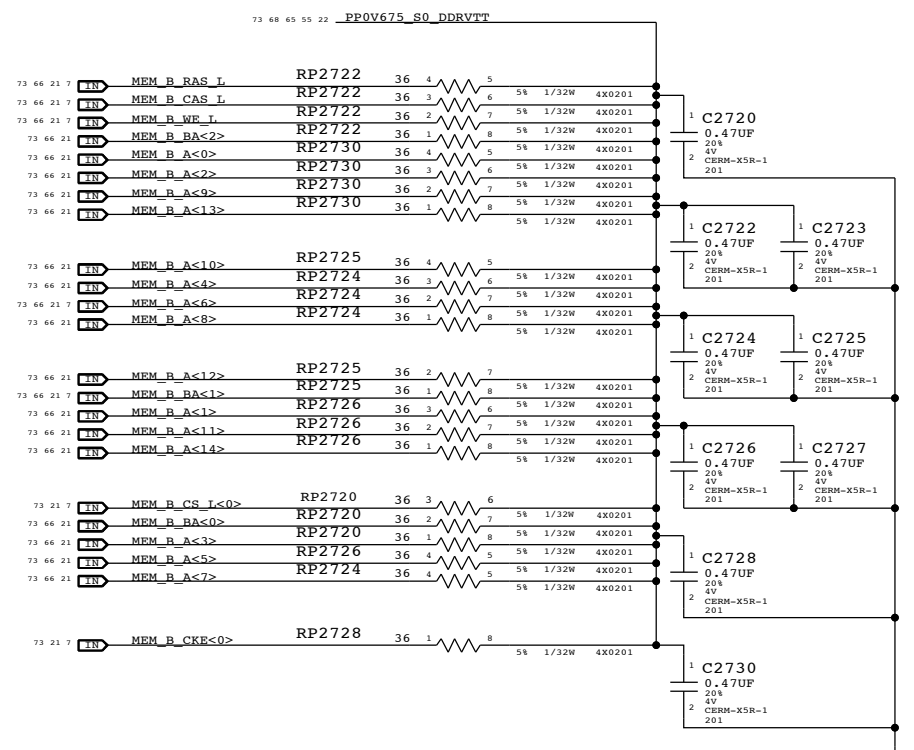


Memory Reset Pull Up

Reset is an open drain in Haswell ULT and needs pull up

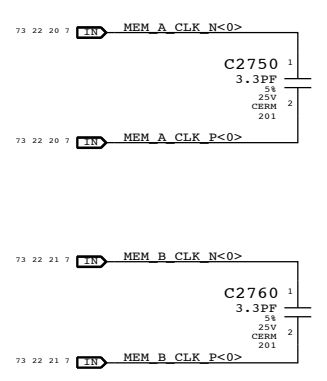


Memory CMD/CTL Termination - Channel B



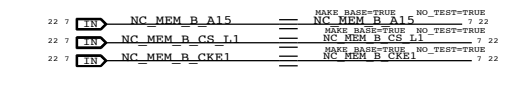
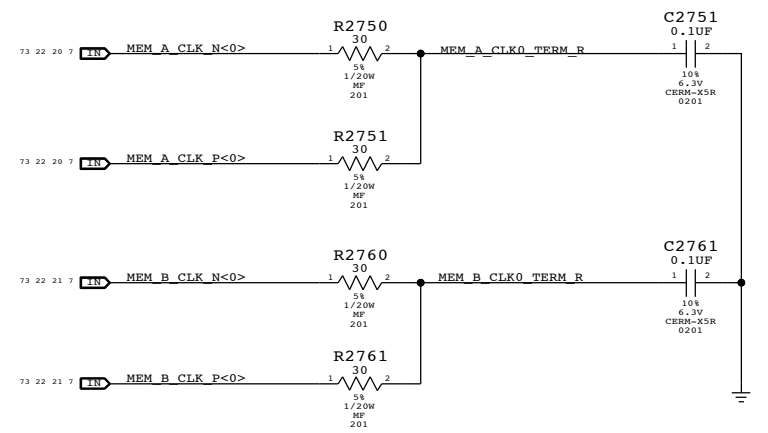
Memory Clock Near-End Termination

Place Source C termination before first DRAM



Memory Clock Far-End Termination

Place RC end termination after last DRAM



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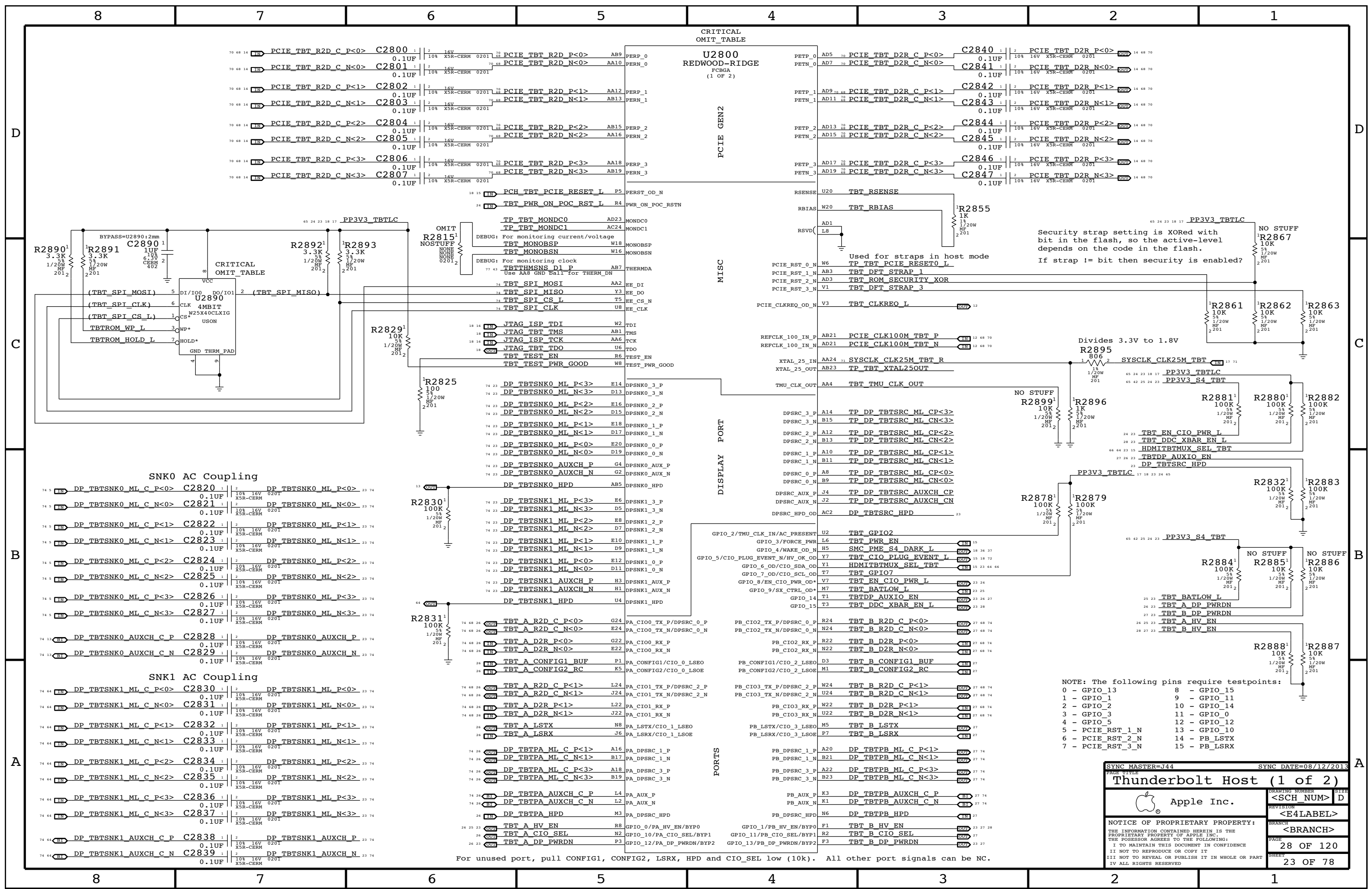
DDR3 Termination

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8 7 6 5 4 3 2 1



Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash. If strap != bit then security is enabled?

Divides 3.3V to 1.8V

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC MASTER=J44 SYNC DATE=08/12/2013

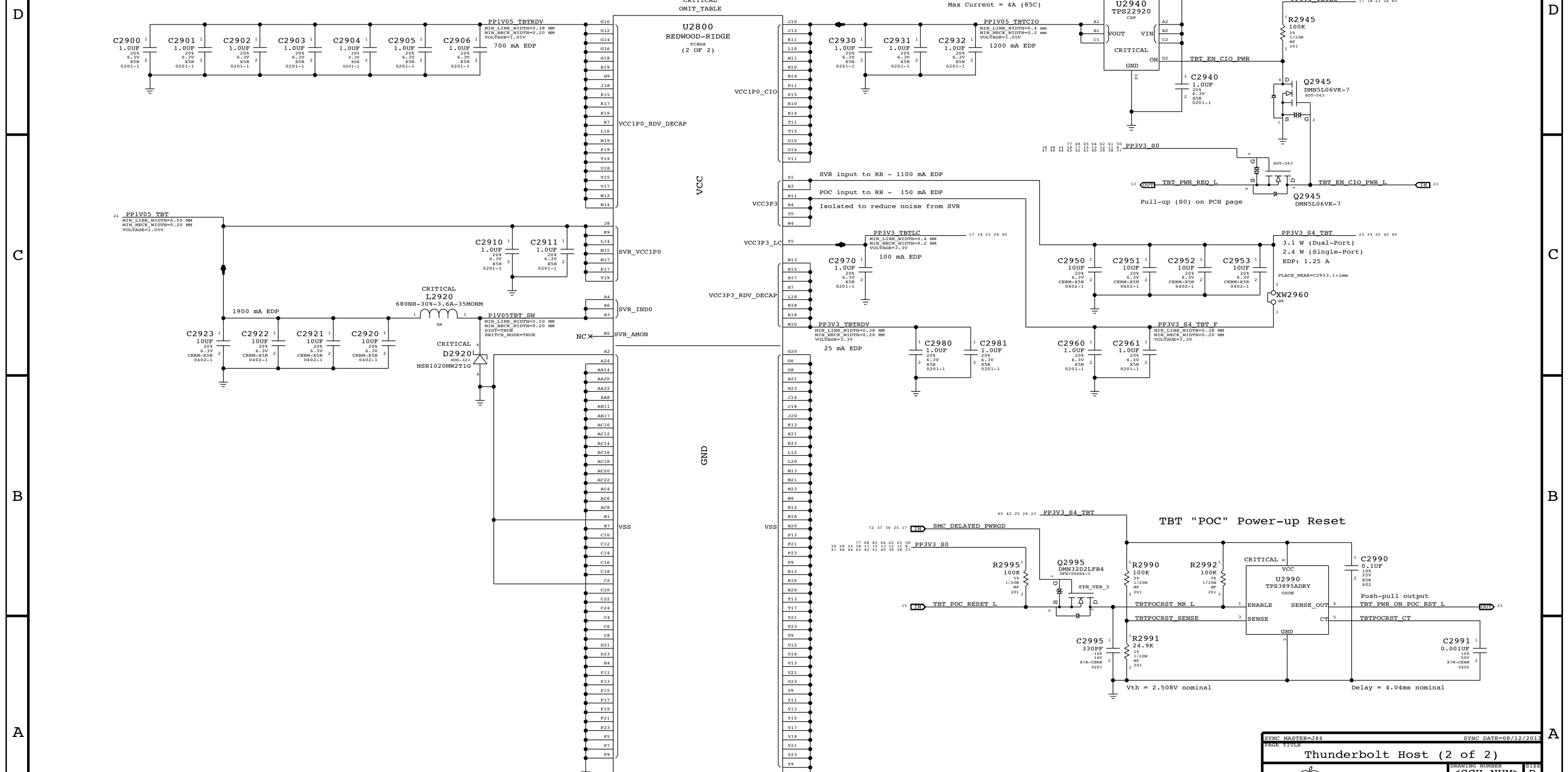
Thunderbolt Host (1 of 2)

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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

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Thunderbolt Host (2 of 2)	
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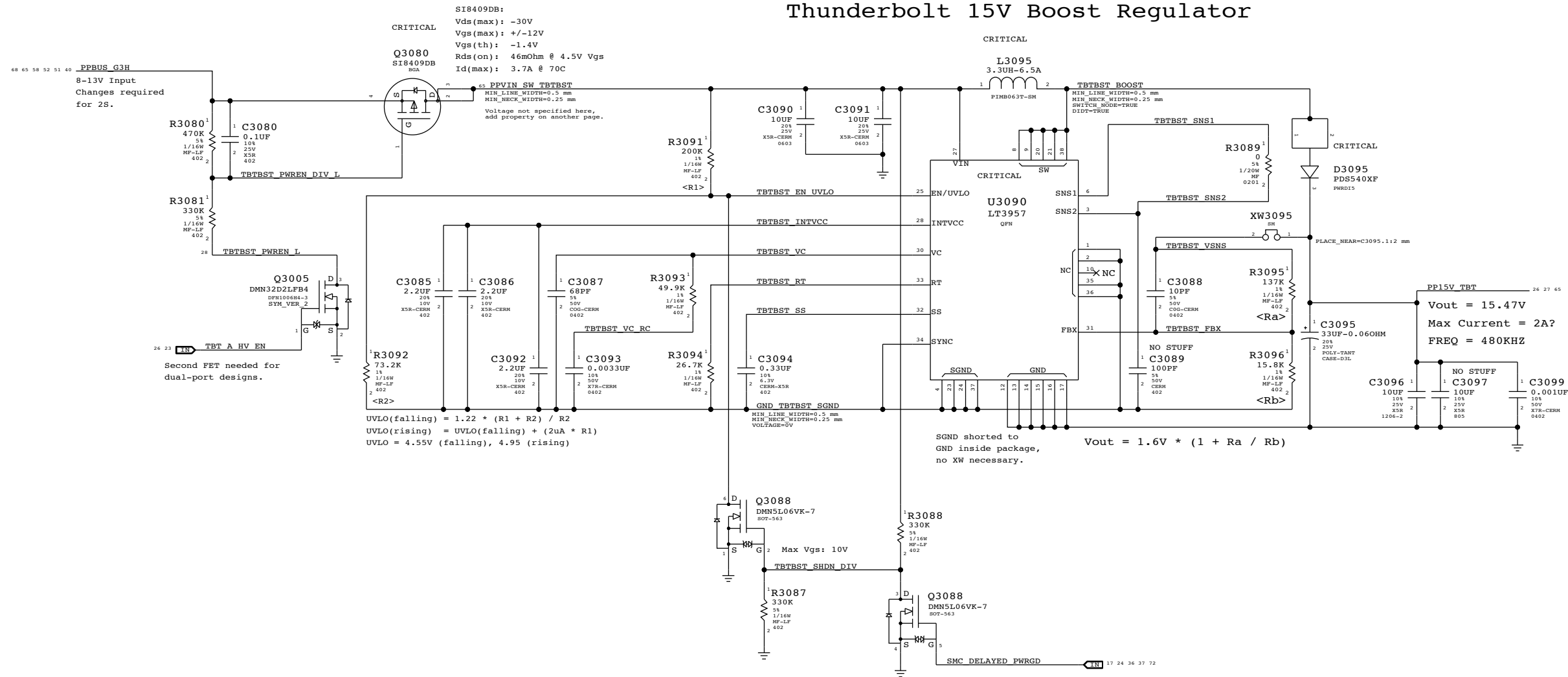
Page Notes

Power aliases required by this page:
 - =PPVIN_SW_TBTBST (8-13V Boost Input)
 - =PP15V_TBT_REG (15V Boost Output)

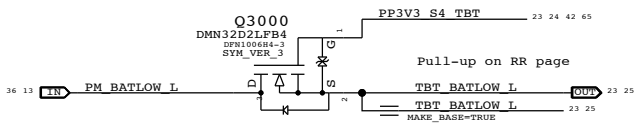
Signal aliases required by this page:
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BOM options provided by this page:
 (NONE)

Thunderbolt 15V Boost Regulator



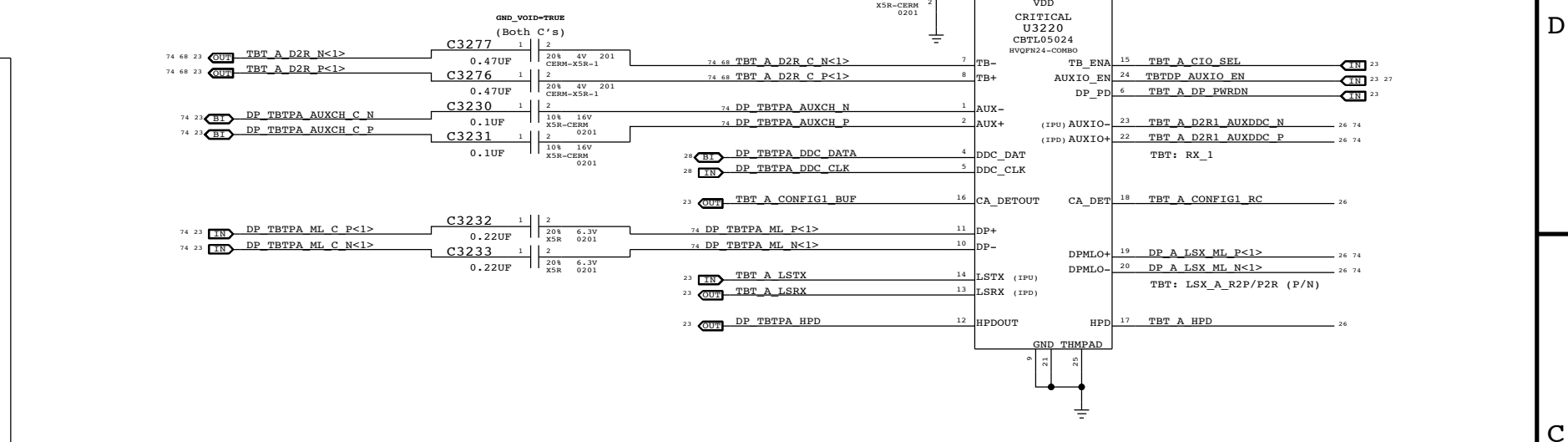
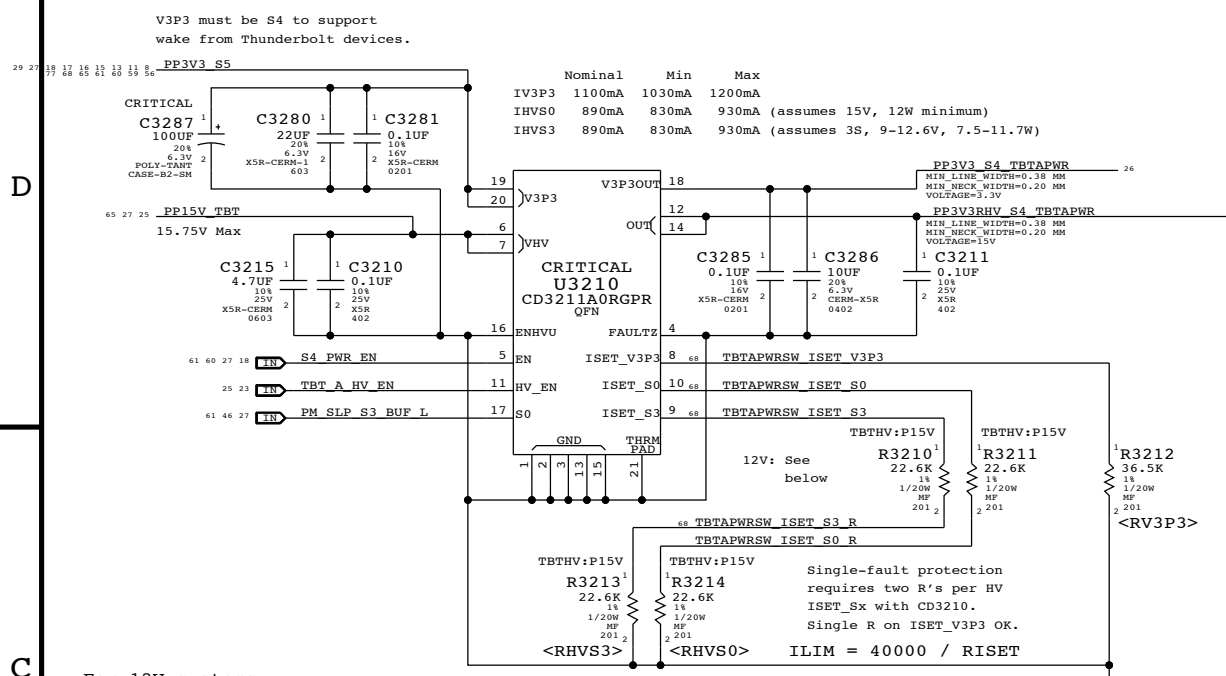
BATLOW# Isolation



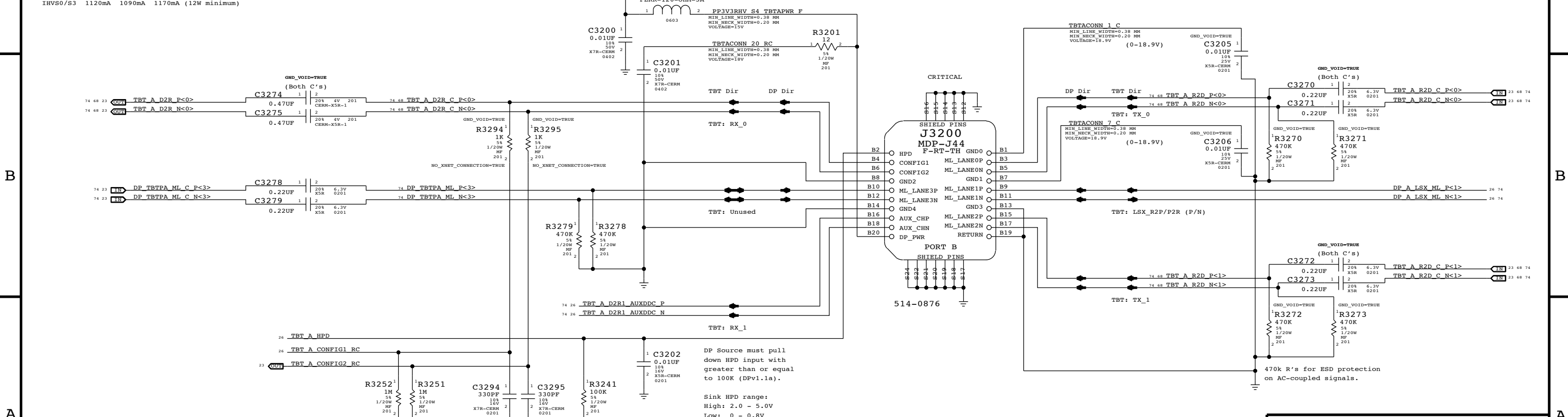
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8 7 6 5 4 3 2 1

3.3V/HV Power MUX



Thunderbolt Connector A

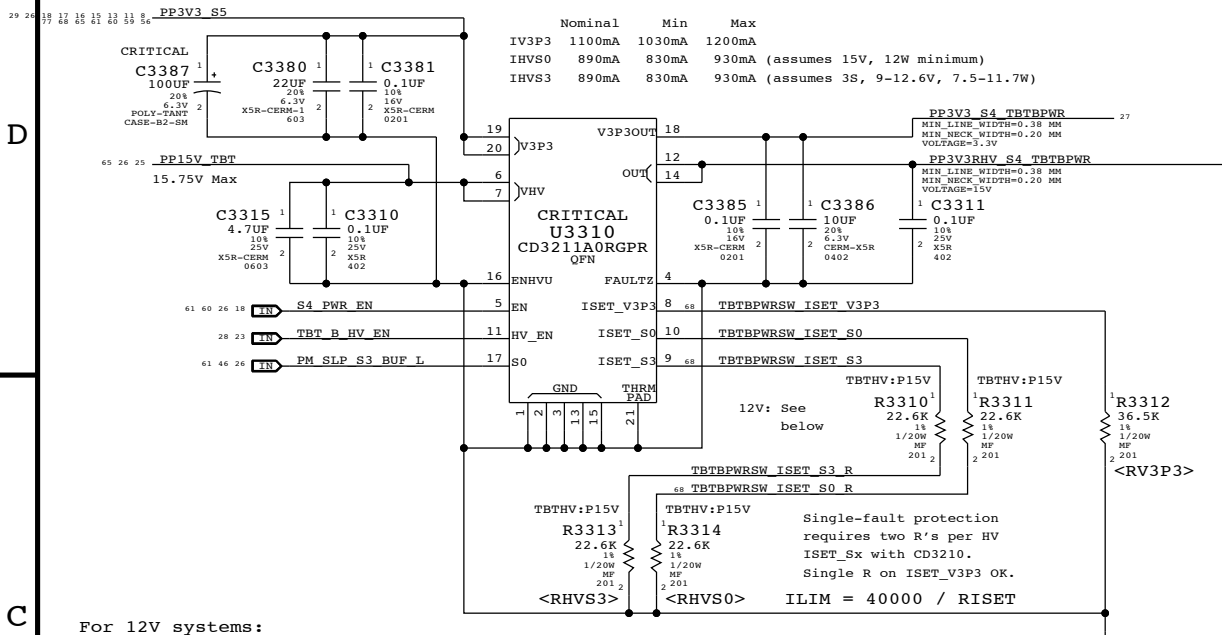


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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

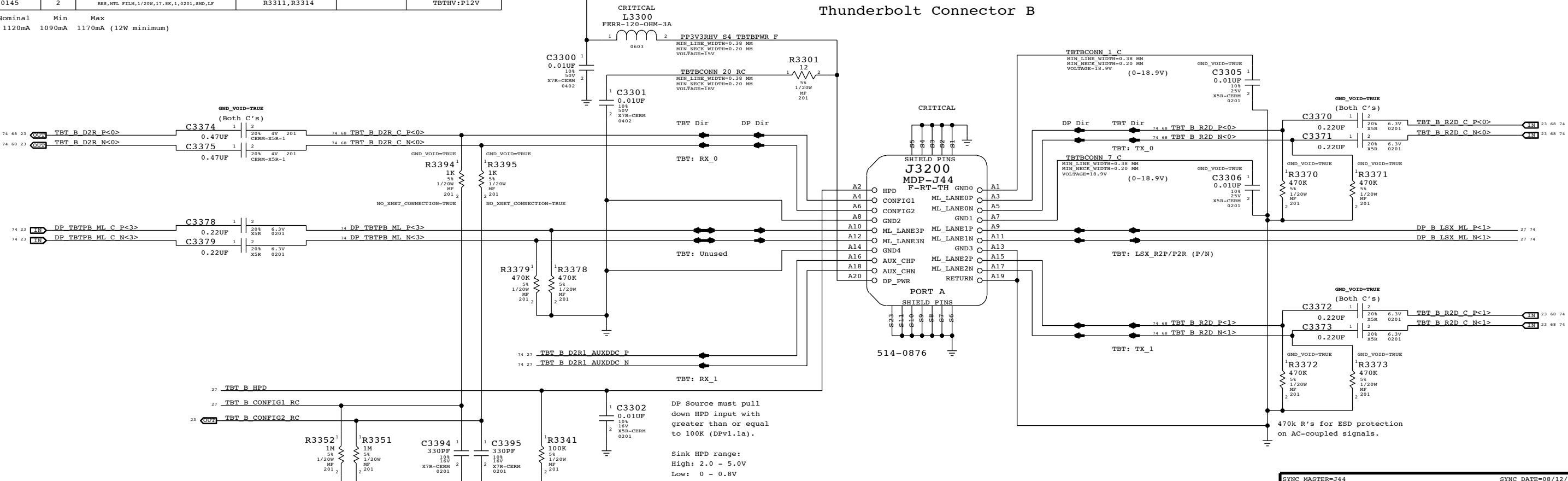


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

Nominal	Min	Max
IHV50/S3	1120mA	1090mA
		1170mA (12W minimum)

Thunderbolt Connector B



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Thunderbolt Connector B

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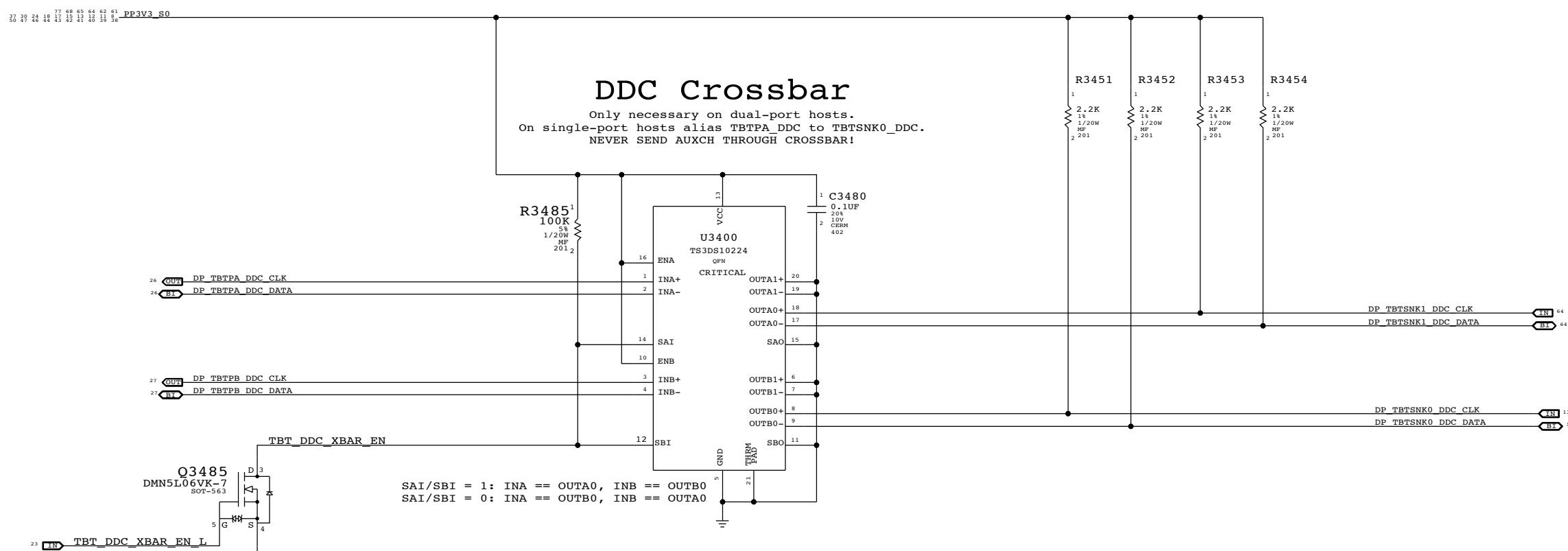
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D C B A

DDC Pull-Ups

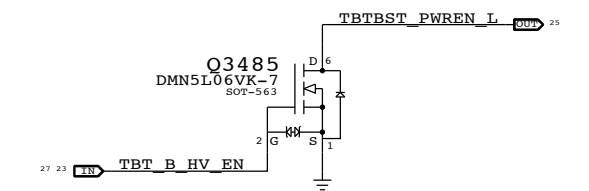
2.2k pull-ups are required by PCH to indicate active display interface. DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK pull-ups are unstuffed.



SAI/SBI = 1: INA == OUTA0, INB == OUTB0
 SAI/SBI = 0: INA == OUTB0, INB == OUTA0

Second FET needed for dual-port designs.
 CONNECTS TO TBTBTS_PWREN_L ON PAGE 30.



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DDC Crossbar			
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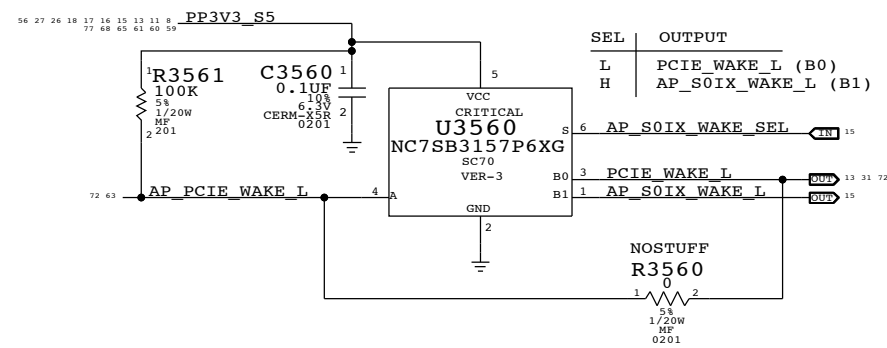
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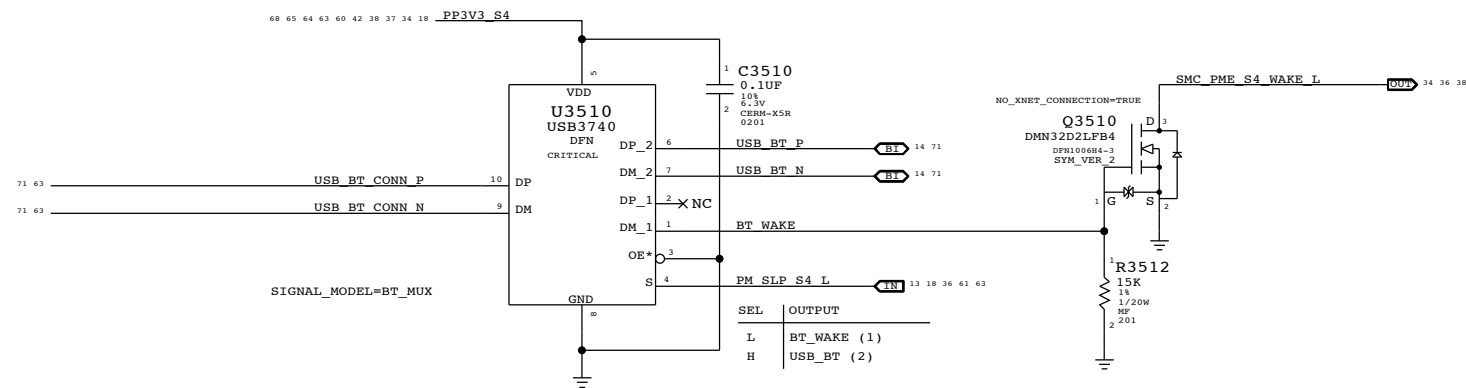
D
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B
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D
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B
A

PCIe Wake Muxing

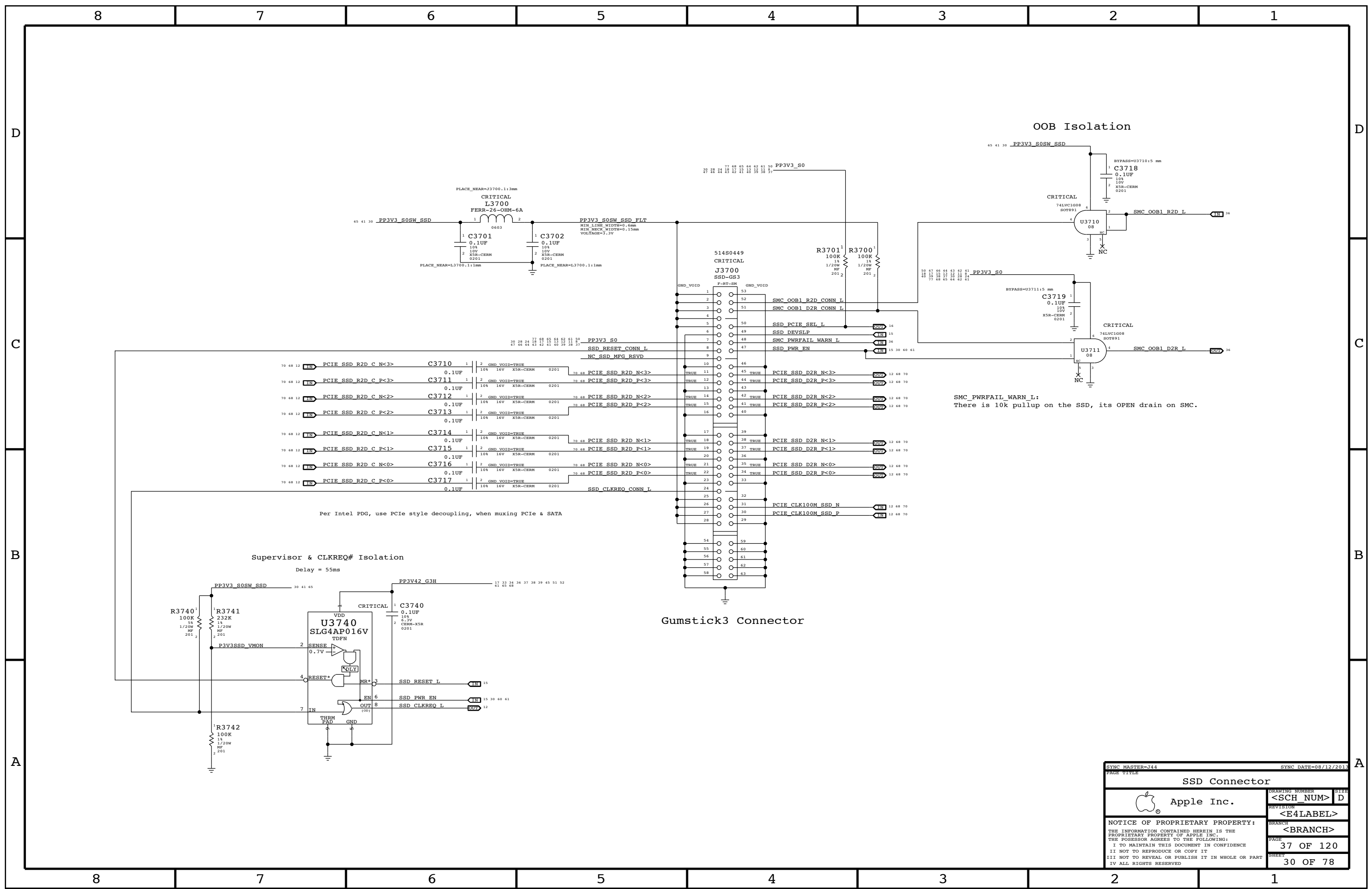


BLUETOOTH

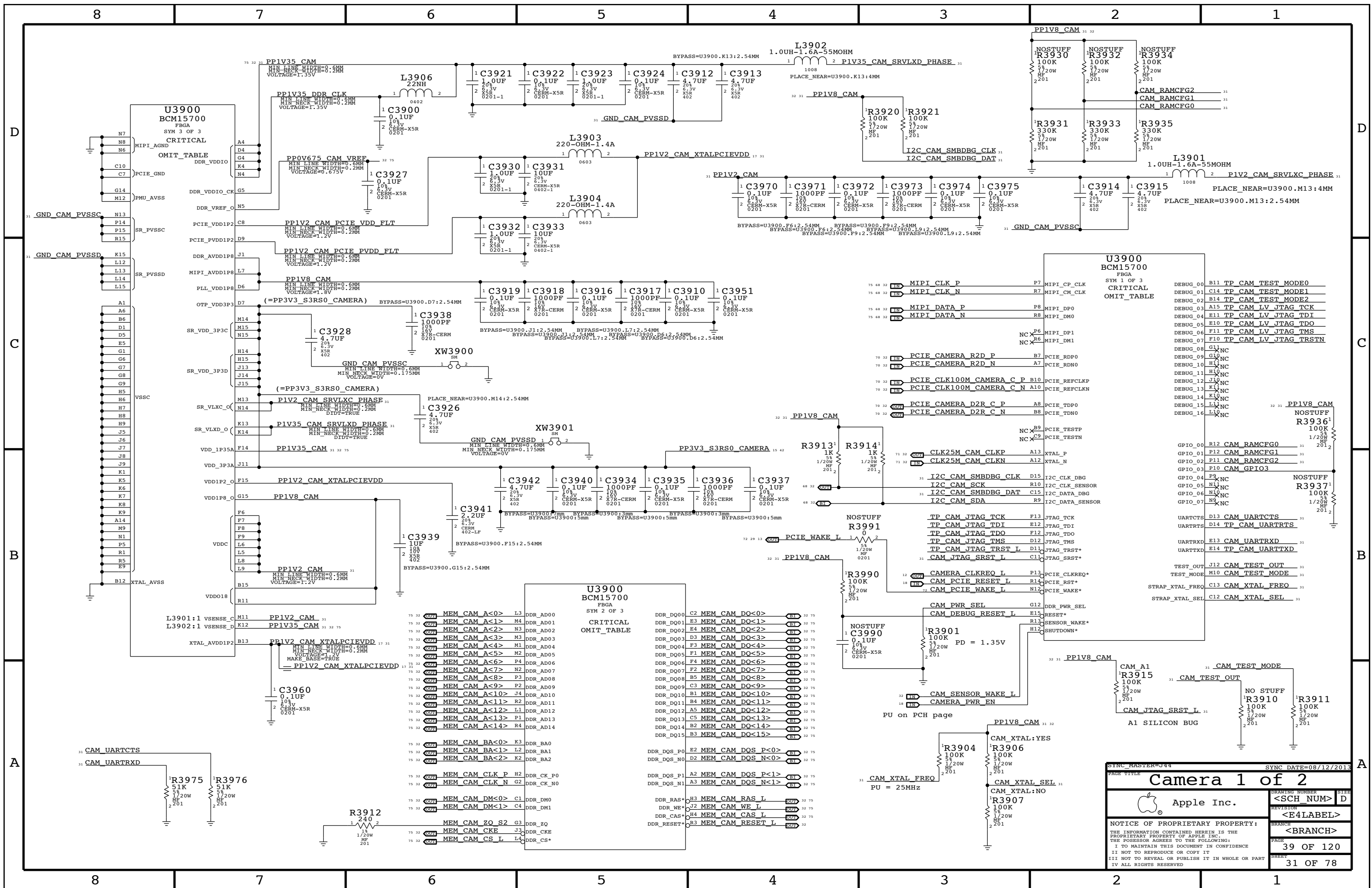


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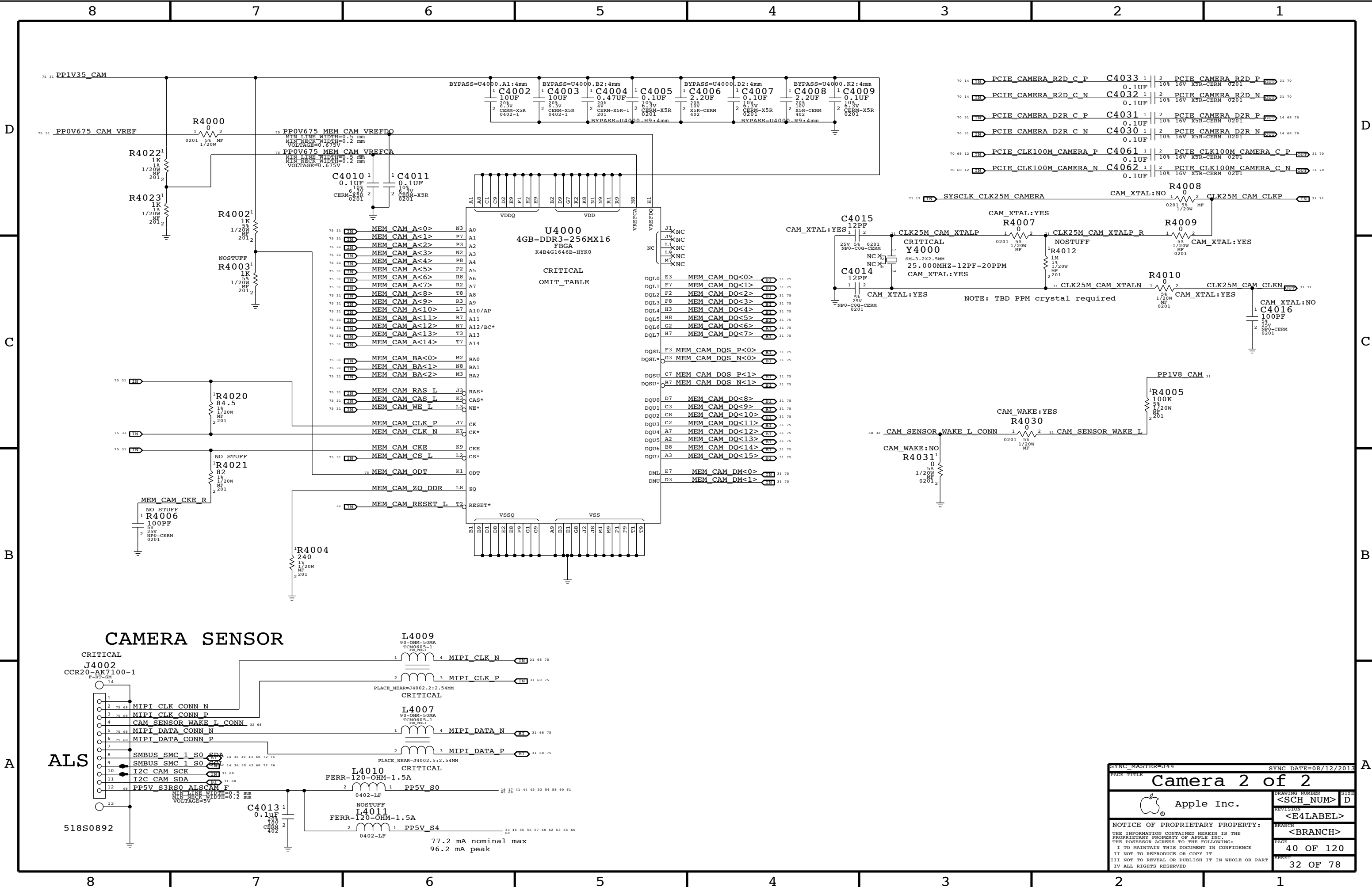
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D

D

C

C

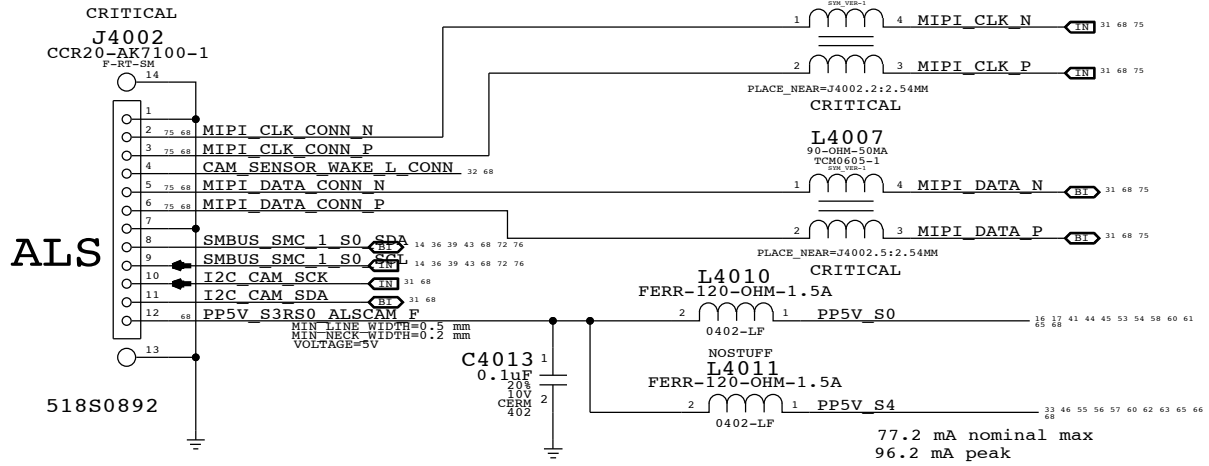
B

B

A

A

CAMERA SENSOR

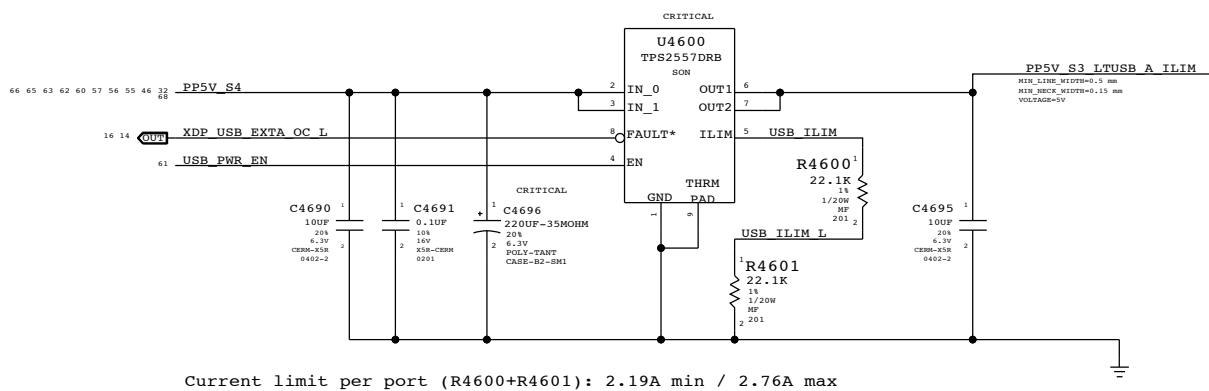


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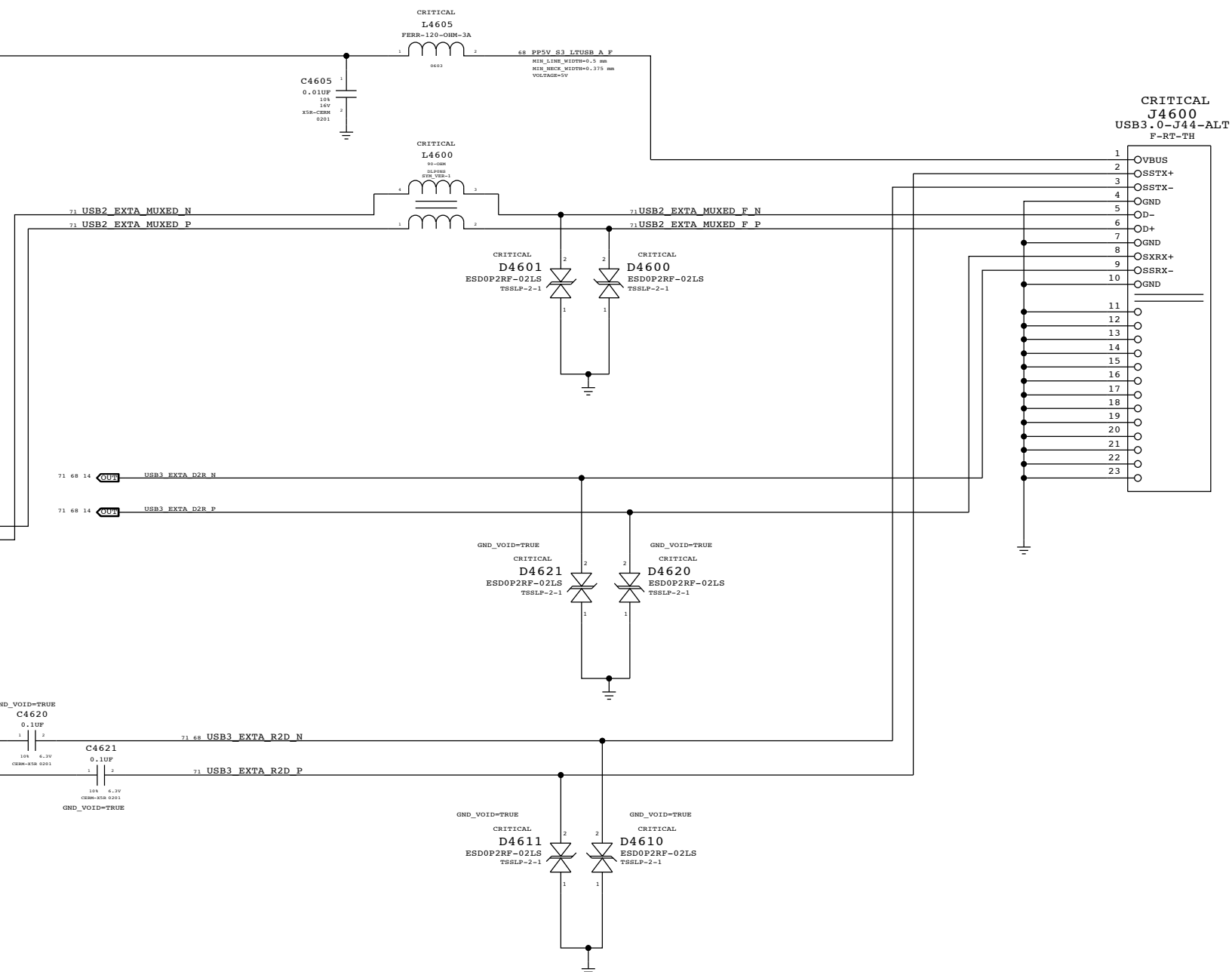
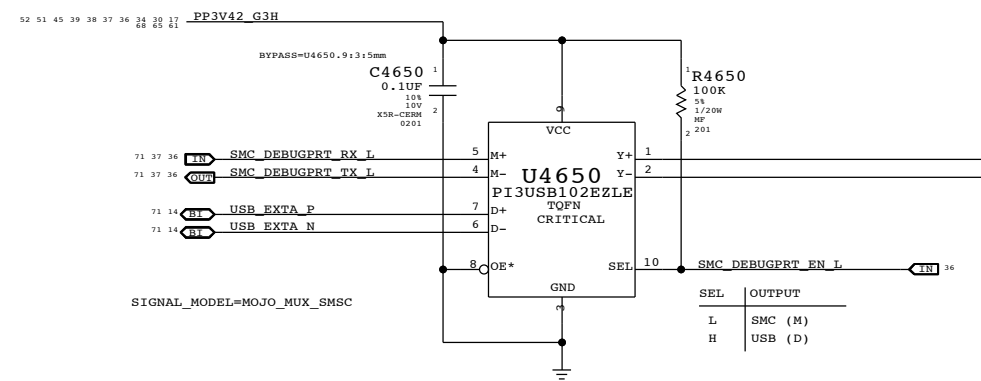
RIGHT USB PORT A

USB Port Power Switch



Mojo SMC Debug Mux

THE PI3USB102E CAN CLAMP VOLTAGE IN THE INTERNAL USB PINS

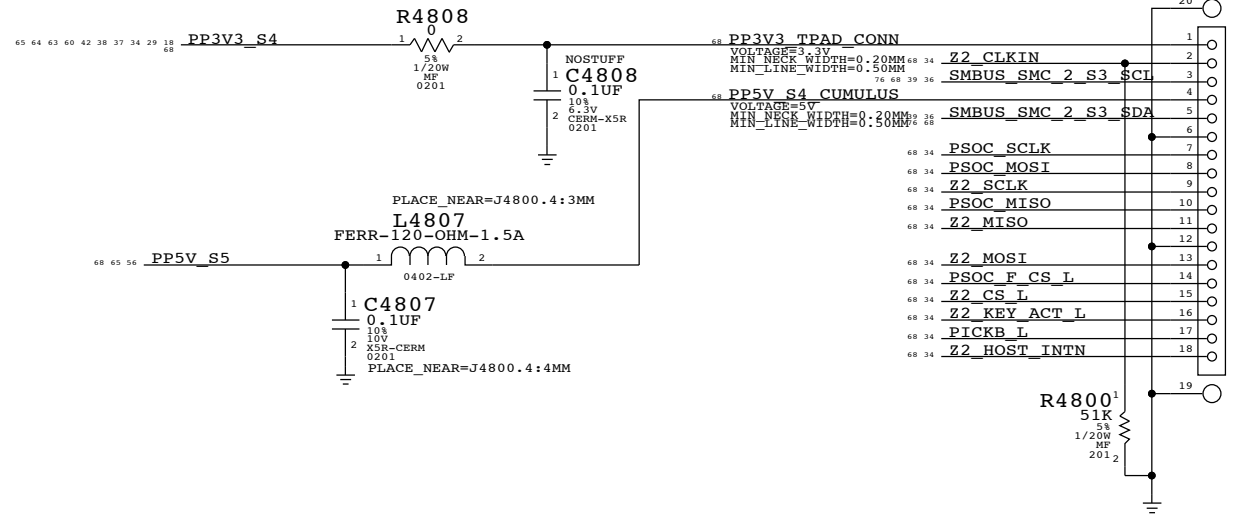


SYNC MASTER=J44		SYNC DATE=08/12/2013	
External A USB3 Connector			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH NUM>	D
		REVISION	
		<E4LABEL>	
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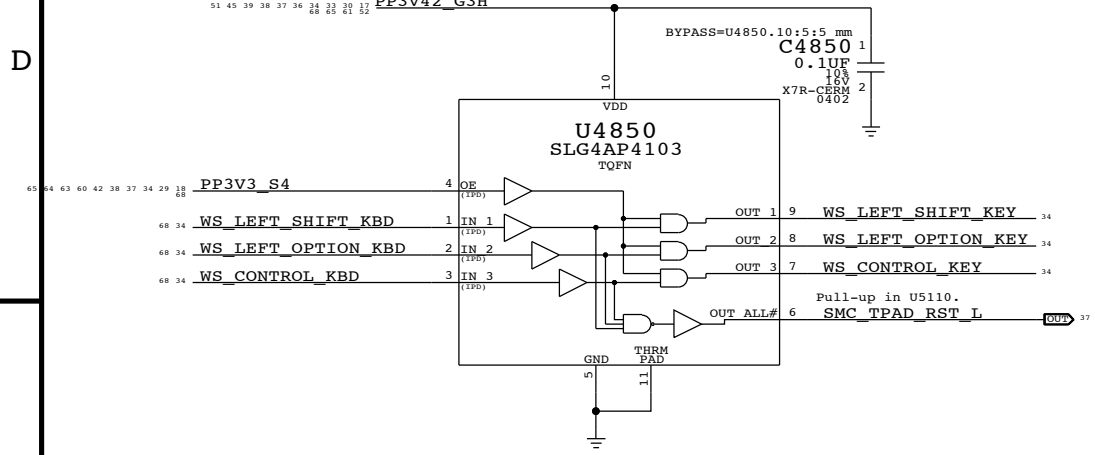
IPD Flex Connector

CRITICAL
J4800
FF14-18C-R11DL
F-RT-SM



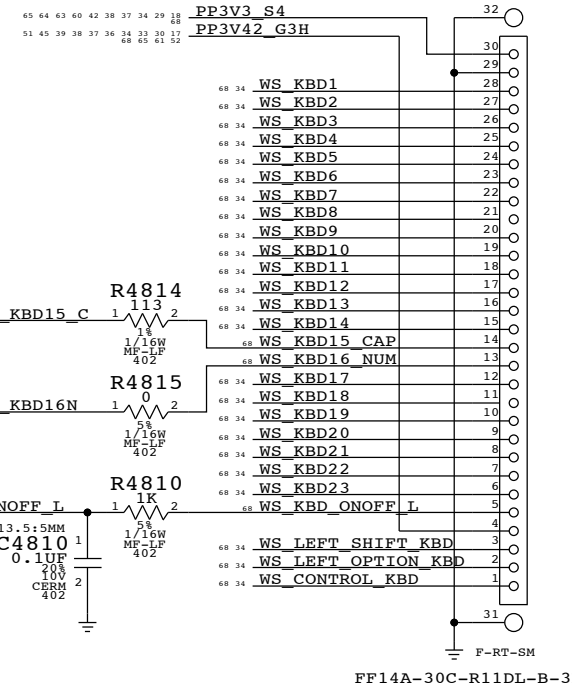
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



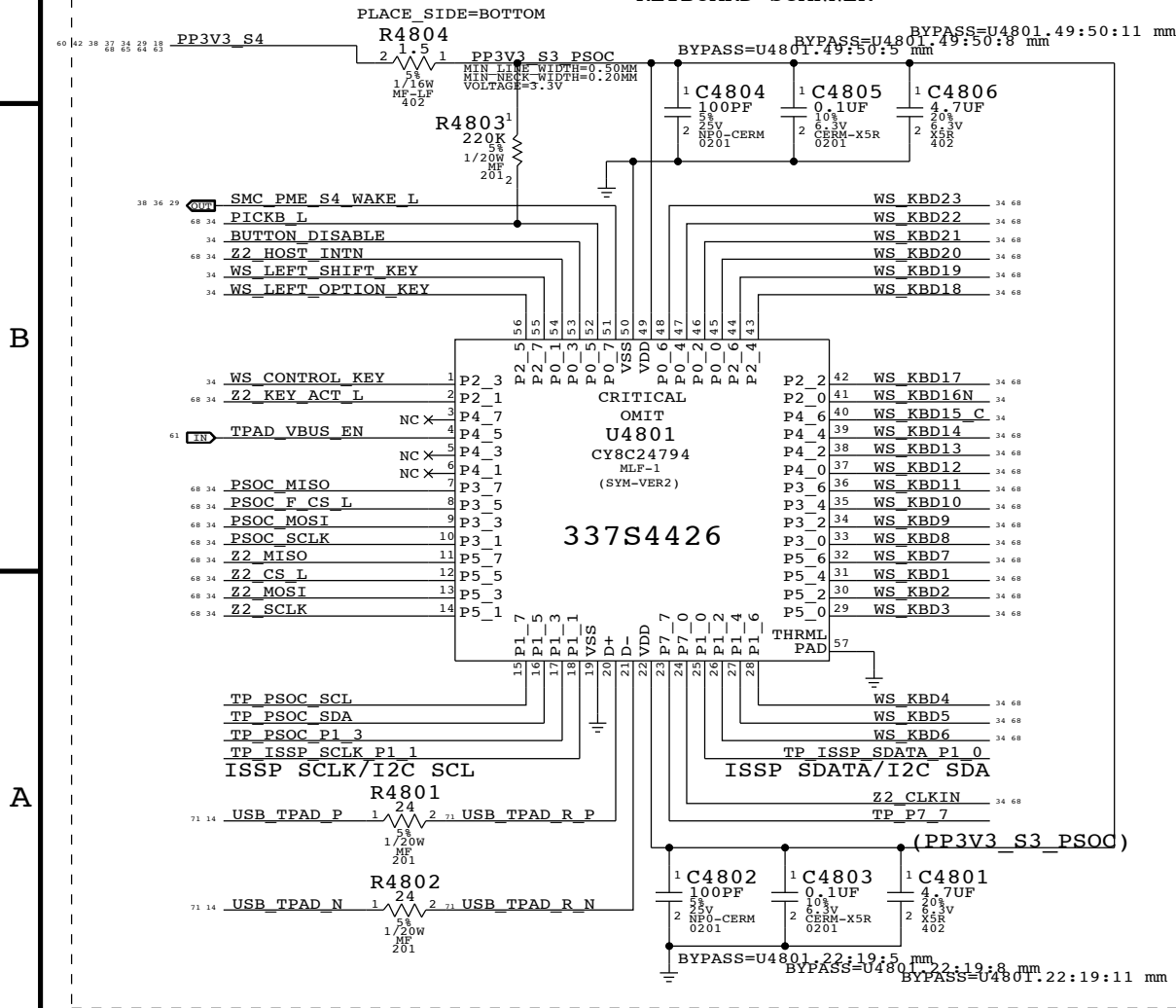
Keyboard Connector

CRITICAL
J4813
518S0752



PSOC USB CONTROLLER

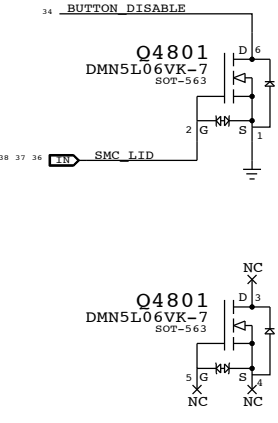
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J4800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V



IC	PIN	NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W	
		800A		0.204 V	16.32E-6 W	
		60MA (MAX)	10 OHM	0.6 V	36E-3 W	
3V3 LDO	VDD	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W	
		8MA (TYP)	1.5 OHM	0.012 V	96E-6 W	
		14MA (MAX)		0.021 V	294E-6 W	
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W	

SYNC MASTER=J44 SYNC DATE=08/12/2013
PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

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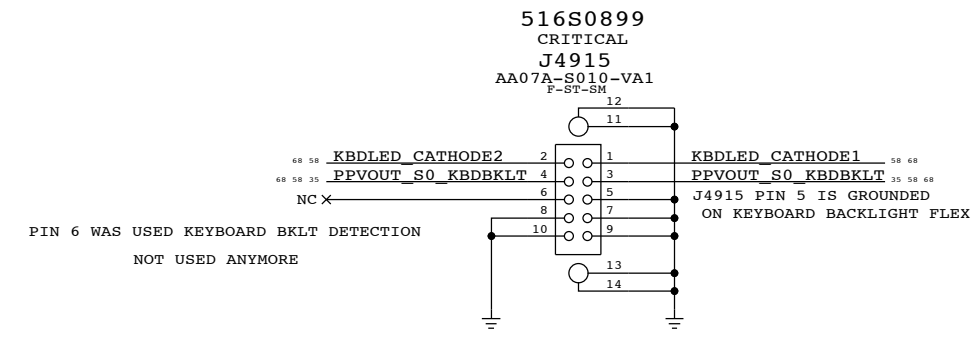
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8 7 6 5 4 3 2 1

D
C
B
A

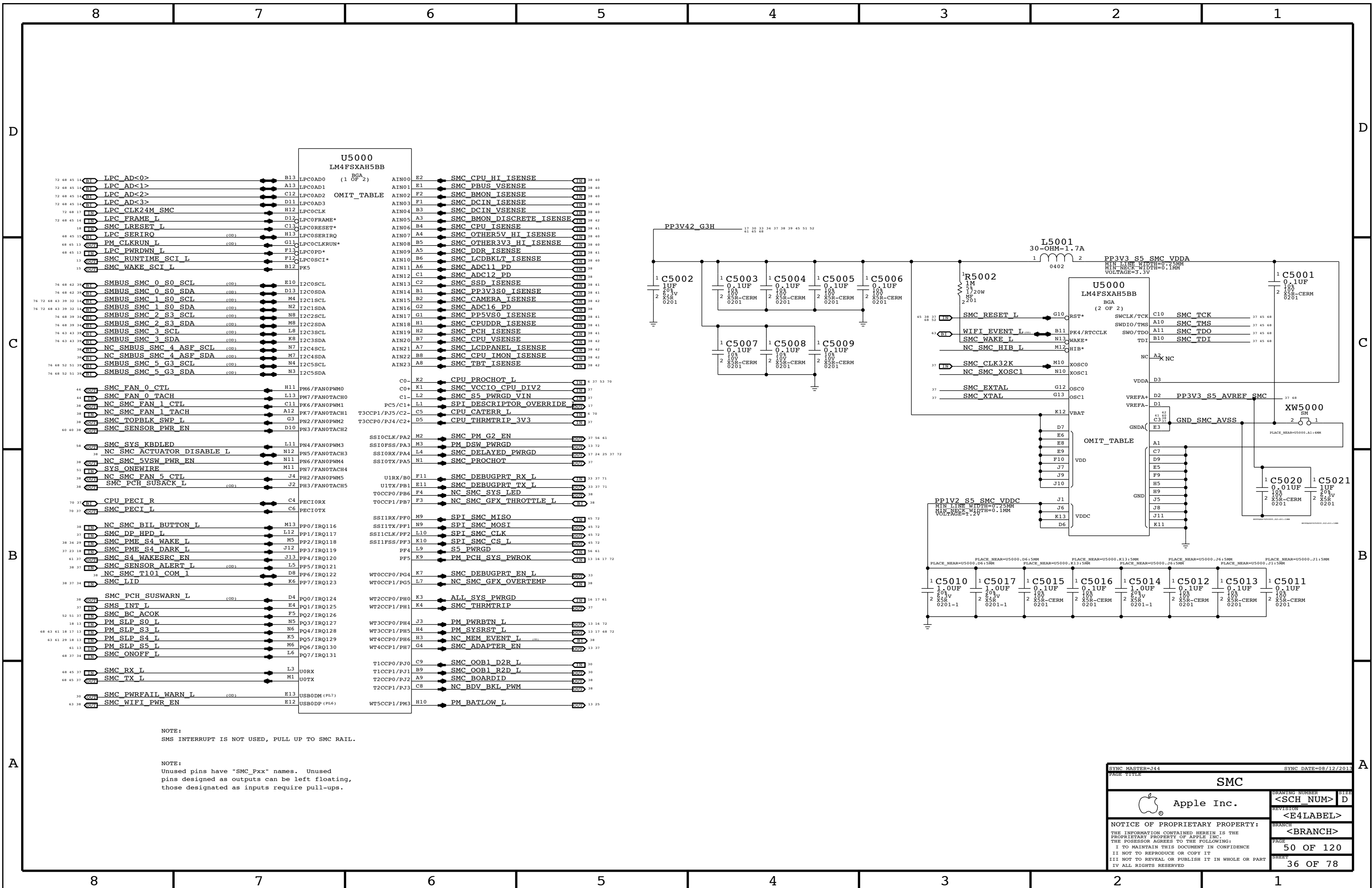
D
C
B
A

Keyboard Backlight Connector



SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE KEYBOARD/TRACKPAD (2 OF 2)			
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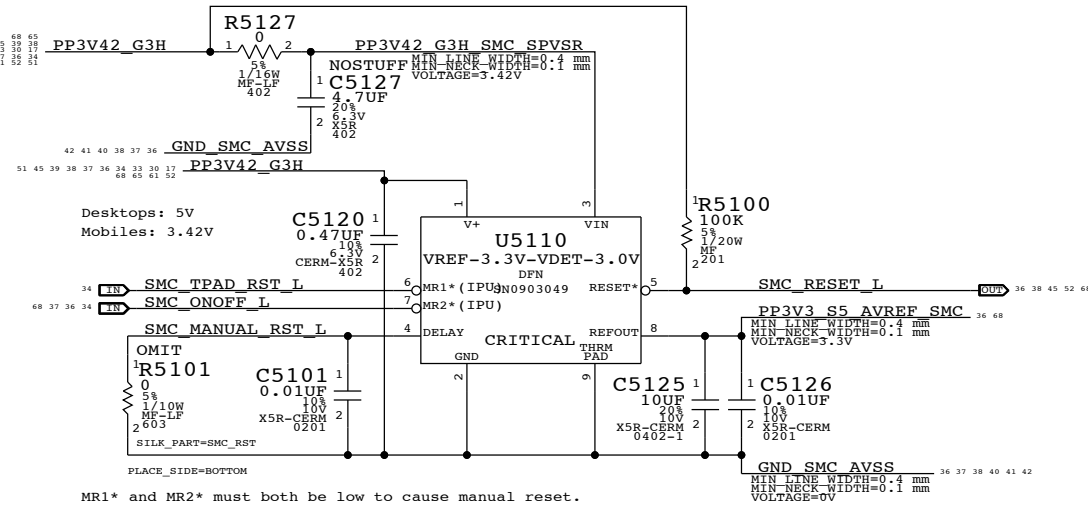


NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

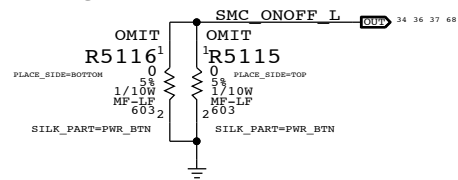
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SMC			
Apple Inc.		DRAWING NUMBER	SIZE
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SMC Reset "Button", Supervisor & AVREF Supply



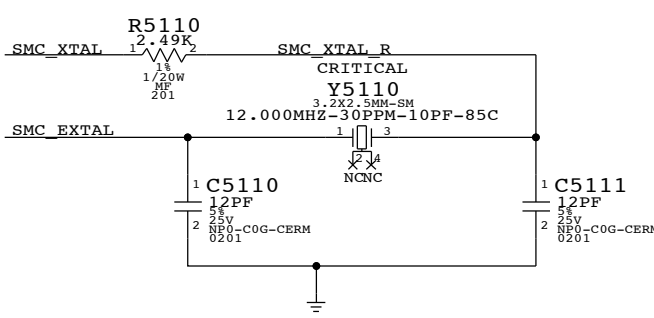
MR1* and MR2* must both be low to cause manual reset.
 Used on mobiles to support SMC reset via keyboard.
 NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

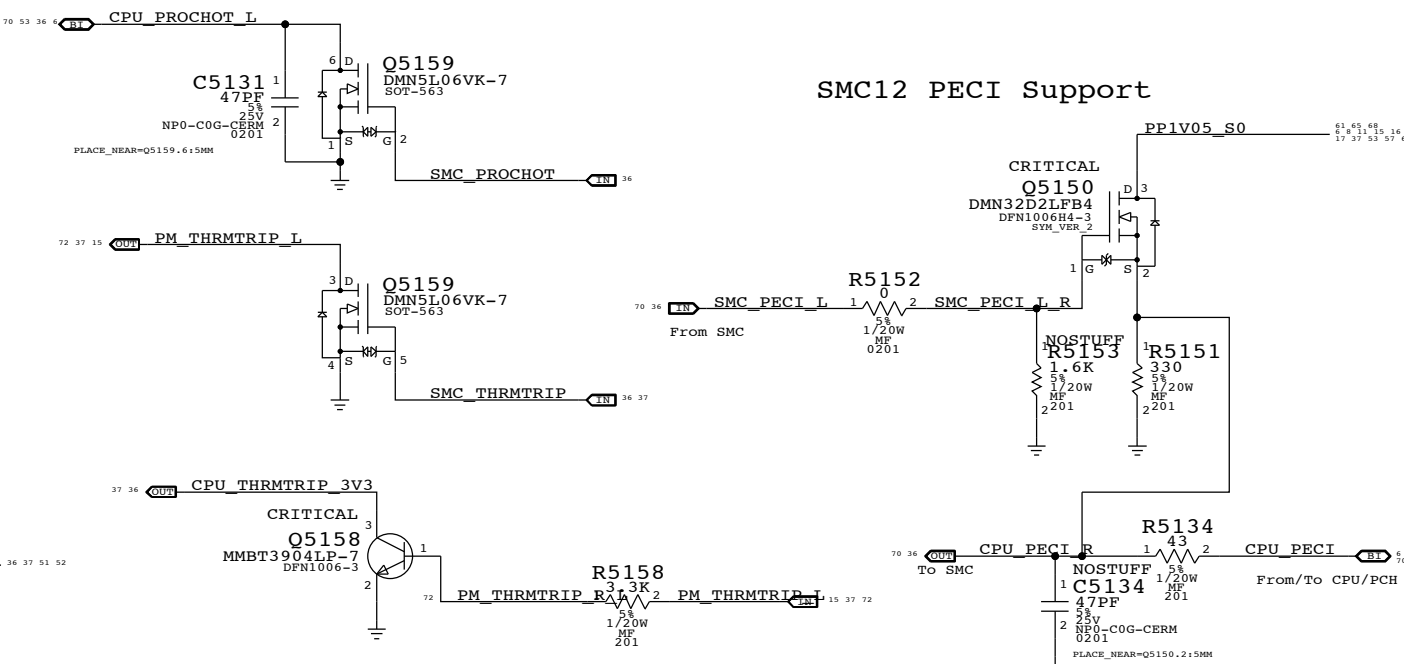


SMC Crystal Circuit

SMC USB Clock require these crystal values: 5, 6, 8, 10, 12, 16, 18, 20, 24, 25 MHz

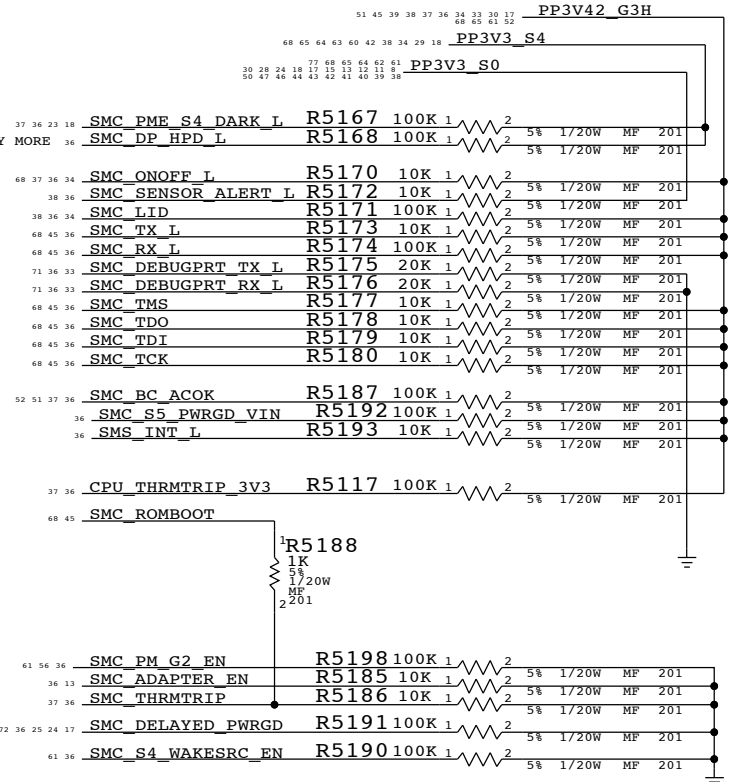


SMC12 PECI Support



SMC_BC_ACOK == SMC BC ACOK
 MAKE_BASE=TRUE

SMC_PME_S4_DARK_L == SMC_PME_S4_DARK_L
 MAKE_BASE=TRUE

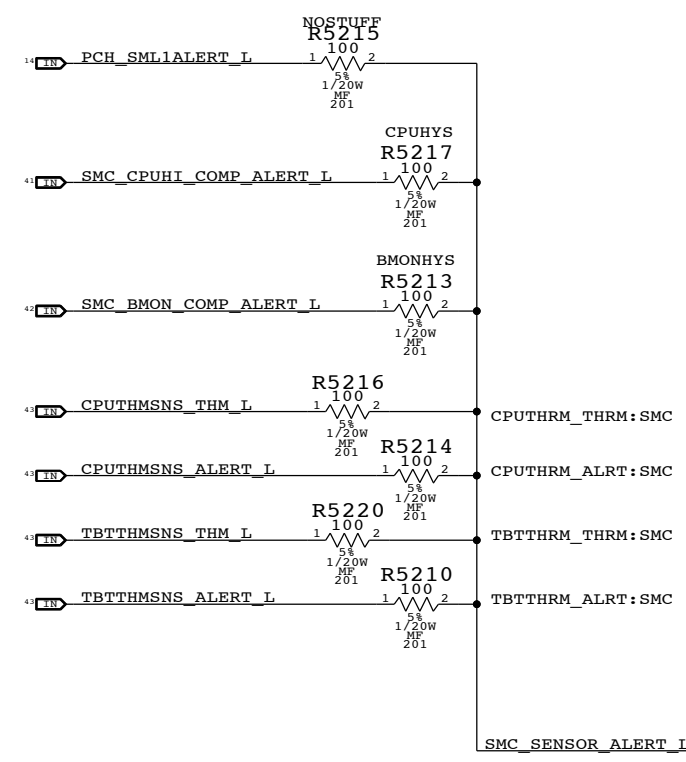


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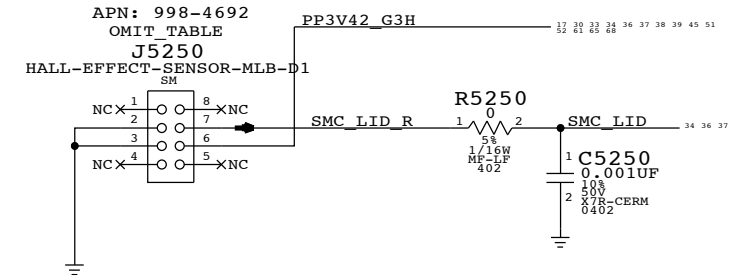
SMC12 ADC Assignments

40 38 36	SMC_CPU_HI_ISENSE	=	SMC_CPU_HI_ISENSE	36 38 40
40 38 36	SMC_PBUS_VSENSE	=	SMC_PBUS_VSENSE	36 38 40
40 38 36	SMC_BMON_ISENSE	=	SMC_BMON_ISENSE	36 38 40
40 38 36	SMC_DCIN_ISENSE	=	SMC_DCIN_ISENSE	36 38 40
40 38 36	SMC_DCIN_VSENSE	=	SMC_DCIN_VSENSE	36 38 40
42 38 36	SMC_BMON_DISCRETE_ISENSE	=	SMC_BMON_DISCRETE_ISENSE	36 38 42
42 38 36	SMC_CPU_ISENSE	=	SMC_CPU_ISENSE	36 38 41
40 38 36	SMC_OTHER5V_HI_ISENSE	=	SMC_OTHER5V_HI_ISENSE	36 38 40
40 38 36	SMC_OTHER3V3_HI_ISENSE	=	SMC_OTHER3V3_HI_ISENSE	36 38 40
41 38 36	SMC_DDR_ISENSE	=	SMC_DDR_ISENSE	36 38 41
40 38 36	SMC_LCDBKLT_ISENSE	=	SMC_LCDBKLT_ISENSE	36 38 40
38 36	SMC_ADC11_PD	=	SMC_ADC11_PD	36 38
38 36	SMC_ADC12_PD	=	SMC_ADC12_PD	36 38
41 38 36	SMC_SSD_ISENSE	=	SMC_SSD_ISENSE	36 38 41
42 38 36	SMC_PP3V3S0_ISENSE	=	SMC_PP3V3S0_ISENSE	36 38 41
42 38 36	SMC_CAMERA_ISENSE	=	SMC_CAMERA_ISENSE	36 38 42
38 36	SMC_ADC16_PD	=	SMC_ADC16_PD	36 38
41 38 36	SMC_PP5V50_ISENSE	=	SMC_PP5V50_ISENSE	36 38 41
41 38 36	SMC_CPUDDR_ISENSE	=	SMC_CPUDDR_ISENSE	36 38 41
41 38 36	SMC_PCH_ISENSE	=	SMC_PCH_ISENSE	36 38 41
42 38 36	SMC_CPU_VSENSE	=	SMC_CPU_VSENSE	36 38 42
42 38 36	SMC_LCDPANEL_ISENSE	=	SMC_LCDPANEL_ISENSE	36 38 42
42 38 36	SMC_CPU_IMON_ISENSE	=	SMC_CPU_IMON_ISENSE	36 38 42
42 38 36	SMC_TBT_ISENSE	=	SMC_TBT_ISENSE	36 38 42

Thermal Alerts



Hall Effect Pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-0912	1	SUBASSY,PCBA HALL EFFECT,J44	J5250	CRITICAL	

639-4502 (J44 HALL EFFECT BOARD) REPORTS TO 677-0912

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU
CPUTHRM:ALRT	CPUTHRM_THRM:PU,CPUTHRM_ALRT:SMC
CPUTHRM:NONE	CPUTHRM_THRM:PU,CPUTHRM_ALRT:PU

Specify one of these BOM GROUPS.

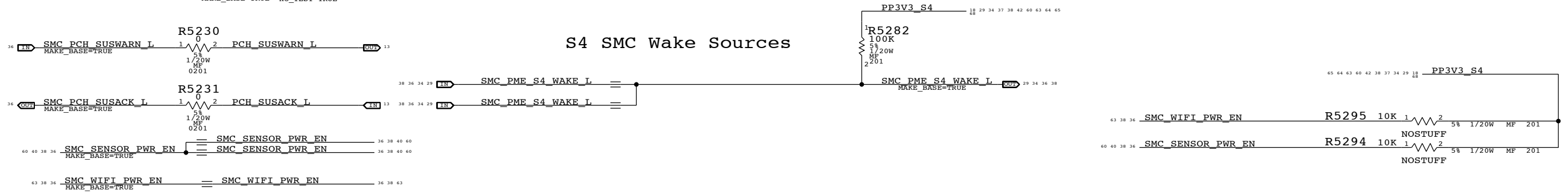
BOM GROUP	BOM OPTIONS
TBTHRM:BOTH	TBTHRM_THRM:SMC,TBTHRM_ALRT:SMC
TBTHRM:THRM	TBTHRM_THRM:SMC,TBTHRM_ALRT:PU
TBTHRM:ALRT	TBTHRM_THRM:PU,TBTHRM_ALRT:SMC
TBTHRM:NONE	TBTHRM_THRM:PU,TBTHRM_ALRT:PU
TBTHRM:GONE	

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

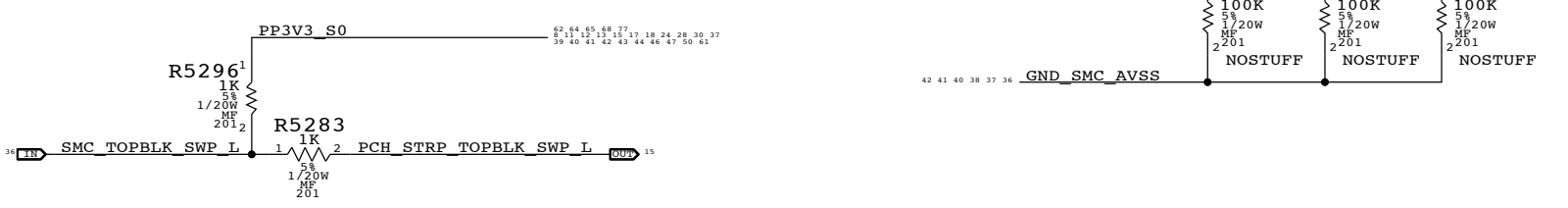
SMC12 Pin Assignments

38 36	NC_SMBUS_SMC_4_ASF_SCL	=	NC_SMBUS_SMC_4_ASF_SCL	36 38
38 36	NC_SMBUS_SMC_4_ASF_SDA	=	NC_SMBUS_SMC_4_ASF_SDA	36 38
38 36	NC_BDV_BKL_PWM	=	NC_BDV_BKL_PWM	36 38
38 36	NC_SMC_SYS_LED	=	NC_SMC_SYS_LED	36 38
38 36	NC_SMC_GFX_THROTTLE_L	=	NC_SMC_GFX_THROTTLE_L	36 38
38 36	NC_SMC_GFX_OVERTEMP	=	NC_SMC_GFX_OVERTEMP	36 38
38 36	NC_SMC_FAN_1_CTL	=	NC_SMC_FAN_1_CTL	36 38
38 36	NC_SMC_FAN_1_TACH	=	NC_SMC_FAN_1_TACH	36 38
38 36	NC_SMC_5VSW_PWR_EN	=	NC_SMC_5VSW_PWR_EN	36 38
38 36	NC_SMC_FAN_5_CTL	=	NC_SMC_FAN_5_CTL	36 38
38 36	NC_SMC_BIL_BUTTON_L	=	NC_SMC_BIL_BUTTON_L	36 38
38 36	NC_MEM_EVENT_L	=	NC_MEM_EVENT_L	36 38
38 36	NC_SMC_T101_COM_1	=	NC_SMC_T101_COM_1	36 38
38 36	NC_SMC_ACTUATOR_DISABLE_L	=	NC_SMC_ACTUATOR_DISABLE_L	36 38

S4 SMC Wake Sources



Top Block Swap

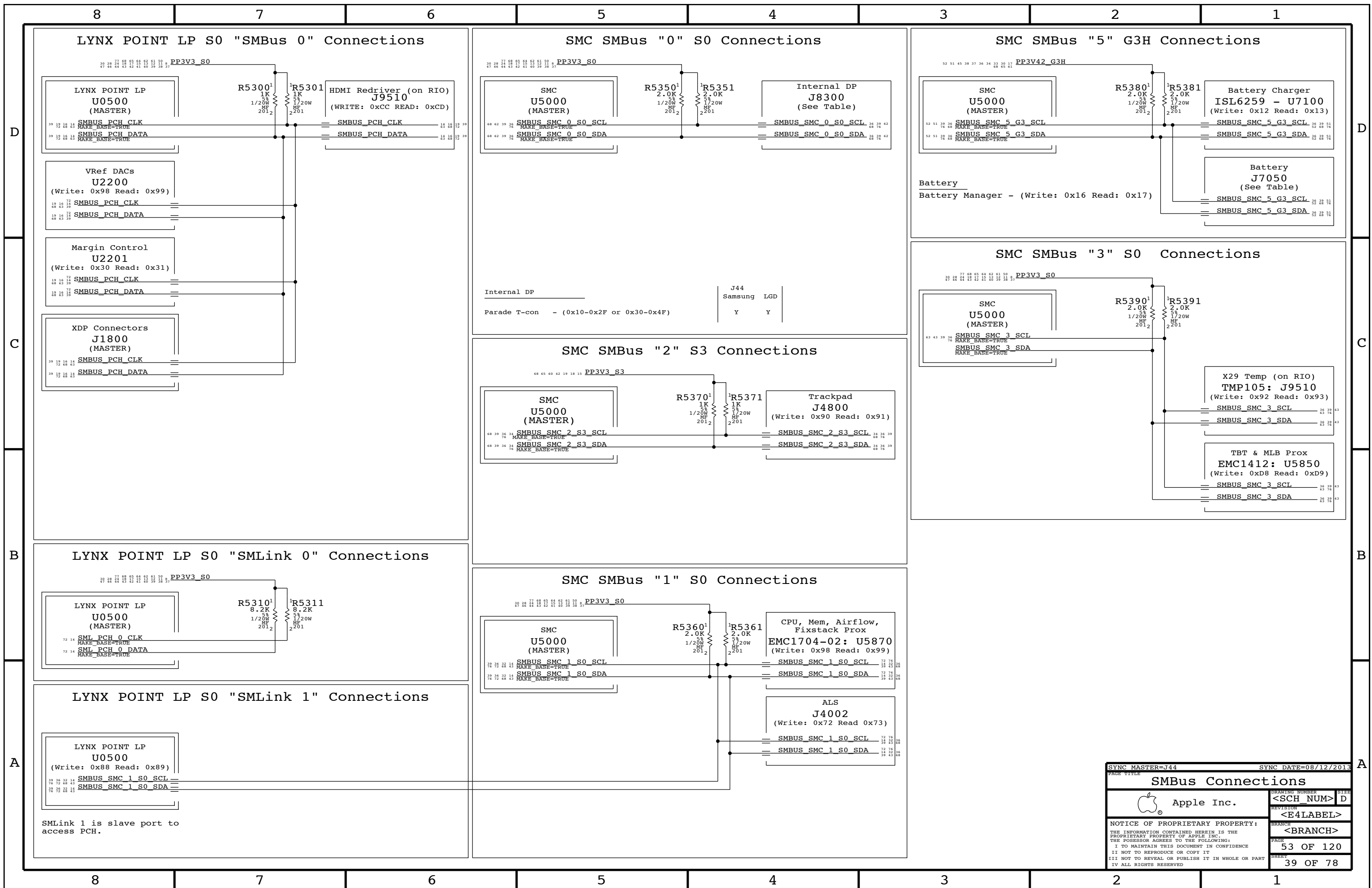


SMC Project Support

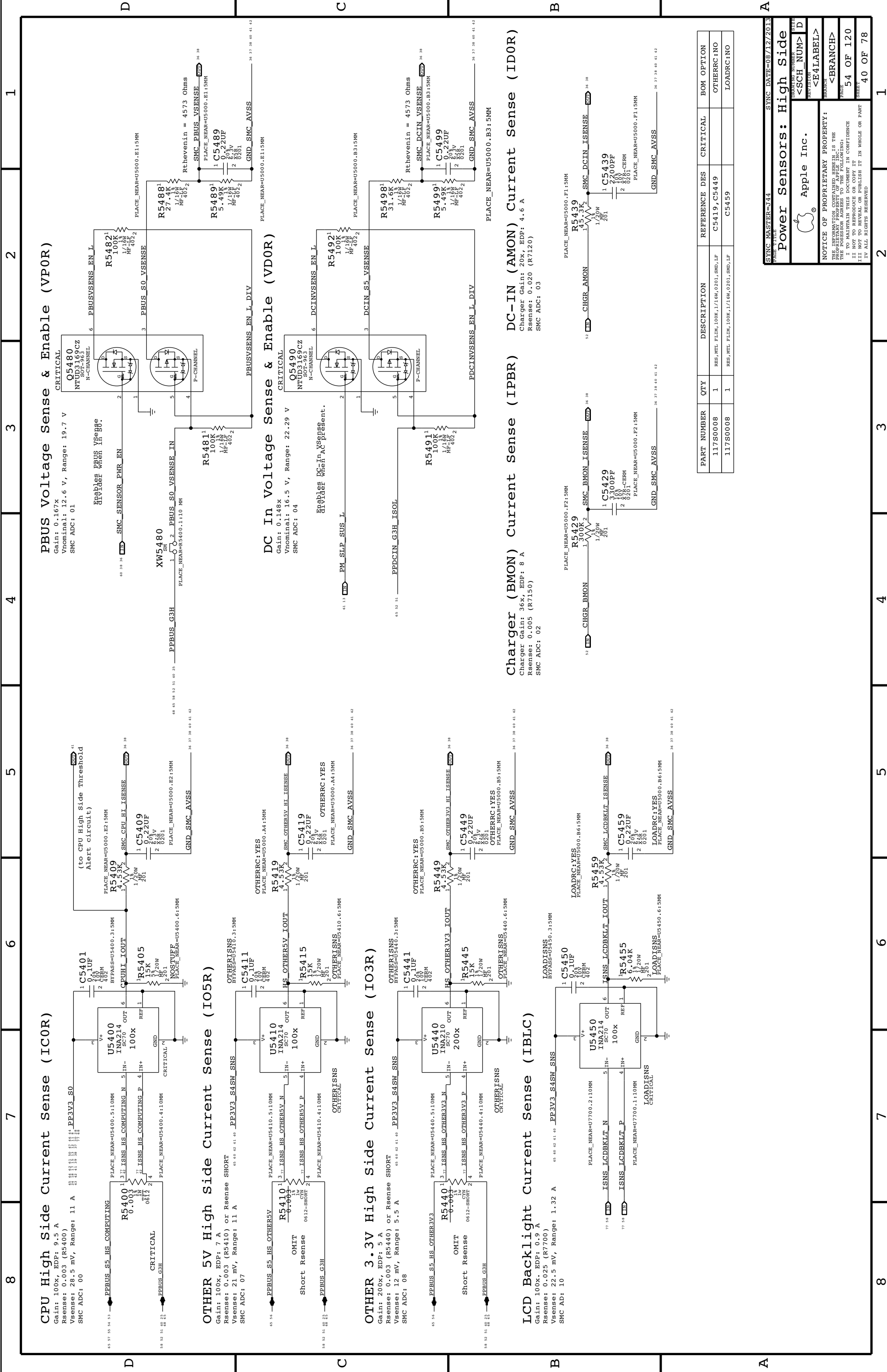
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SYNC MASTER=J44		SYNC DATE=08/12/2013	
SMBus Connections			
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CPU High Side Current Sense (IC0R)
 Gain: 100x, EDP: 9.5 A
 Rsense: 0.003 (R5400)
 Vsense: 28.5 mV, Range: 11 A
 SMC ADC: 00

OTHER 5V High Side Current Sense (IO5R)
 Gain: 100x, EDP: 7 A
 Rsense: 0.003 (R5410) or Rsense SHORT
 Vsense: 21 mV, Range: 11 A
 SMC ADC: 07

OTHER 3.3V High Side Current Sense (IO3R)
 Gain: 200x, EDP: 5 A
 Rsense: 0.003 (R5440) or Rsense SHORT
 Vsense: 12 mV, Range: 5.5 A
 SMC ADC: 08

LCD Backlight Current Sense (IBLC)
 Gain: 100x, EDP: 0.9 A
 Rsense: 0.025 (R7700)
 Vsense: 22.5 mV, Range: 1.32 A
 SMC AD: 10

PBUS Voltage Sense & Enable (VP0R)
 Gain: 0.167x
 Vnominal: 12.6 V, Range: 19.7 V
 SMC ADC: 01

DC In Voltage Sense & Enable (VD0R)
 Gain: 0.148x
 Vnominal: 16.5 V, Range: 22.29 V
 SMC ADC: 04

Charger (BMON) Current Sense (IPBR)
 Charger Gain: 36x, EDP: 8 A
 Rsense: 0.005 (R7150)
 SMC ADC: 02

DC-IN (AMON) Current Sense (ID0R)
 Charger Gain: 20x, EDP: 4.6 A
 Rsense: 0.020 (R7120)
 SMC ADC: 03

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, MET. FLIM, 100K, 1/16W, 0201, SMD, LF	C5419, C5449		OTHERRC:NO
117S0008	1	RES, MET. FLIM, 100K, 1/16W, 0201, SMD, LF	C5459		LOADRC:NO

SYNC MASTER=J44
 SYNC DATE=08/12/2018

Power Sensors: High Side

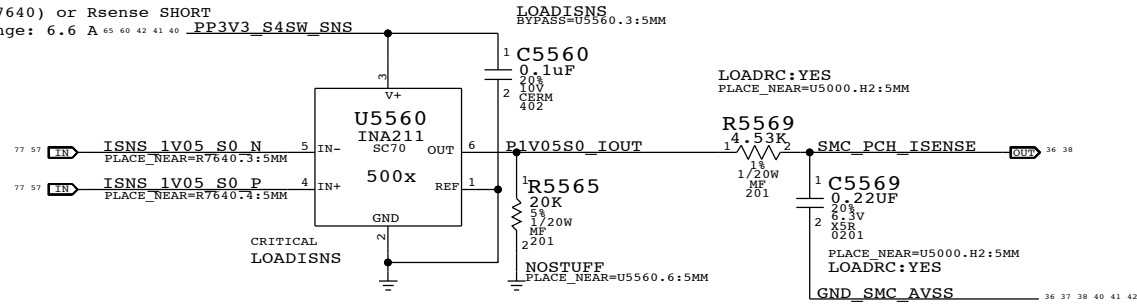
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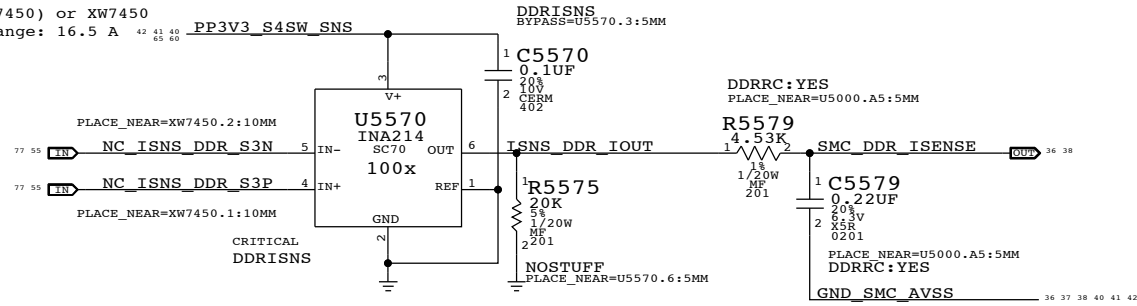
PCH 1.05V Current Sense (IC1C)

Gain: 500x, EDP: 5 A
Rsense: 0.001 (R7640) or Rsense SHORT
Vsense: 5 mV, Range: 6.6 A
SMC ADC: 19



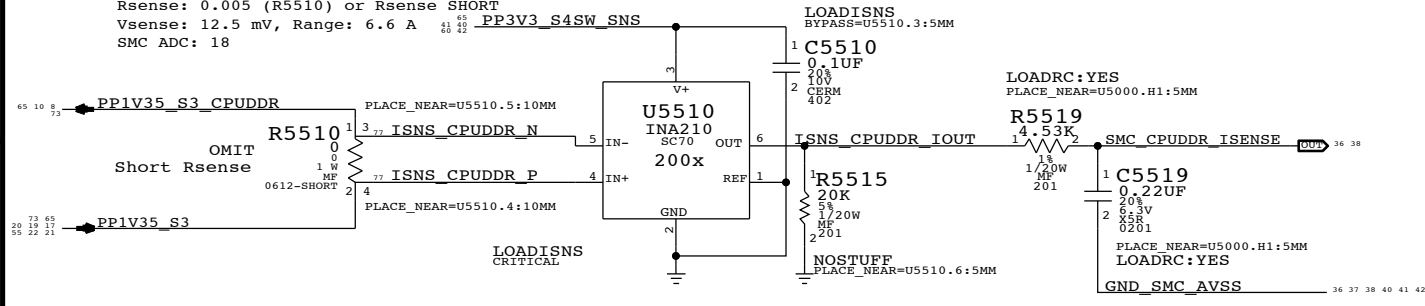
DDR 1.35V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 9 A
Rsense: 0.002 (R7450) or XW7450
Vsense: 21 mV, Range: 16.5 A
SMC ADC: 09



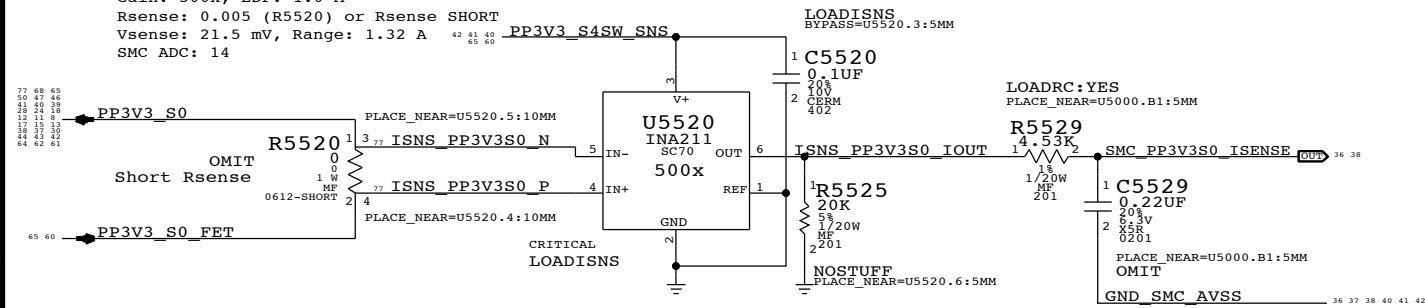
CPU DDR 1.35V S3 (CPU Only) Current Sense (IM1C)

Gain: 200x, EDP: 2.5 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 12.5 mV, Range: 6.6 A
SMC ADC: 18



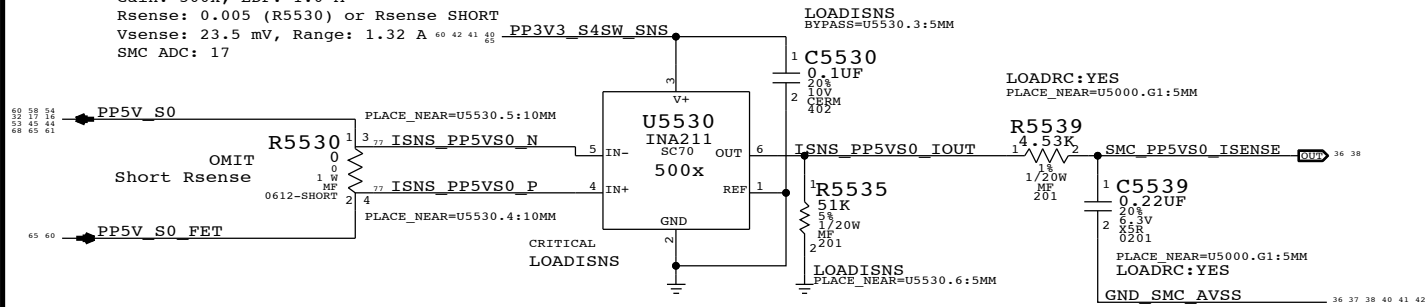
3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.0 A
Rsense: 0.005 (R5520) or Rsense SHORT
Vsense: 21.5 mV, Range: 1.32 A
SMC ADC: 14



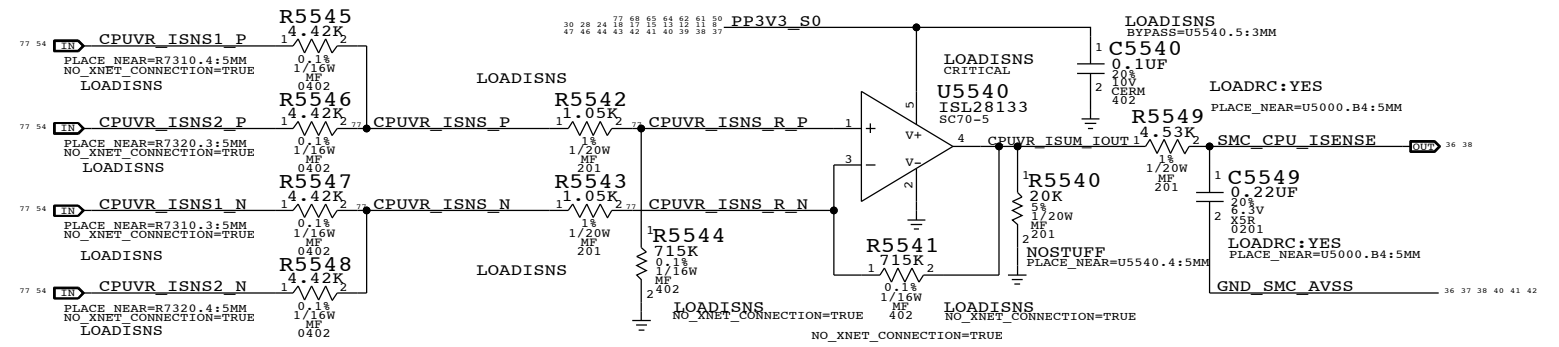
5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 23.5 mV, Range: 1.32 A
SMC ADC: 17



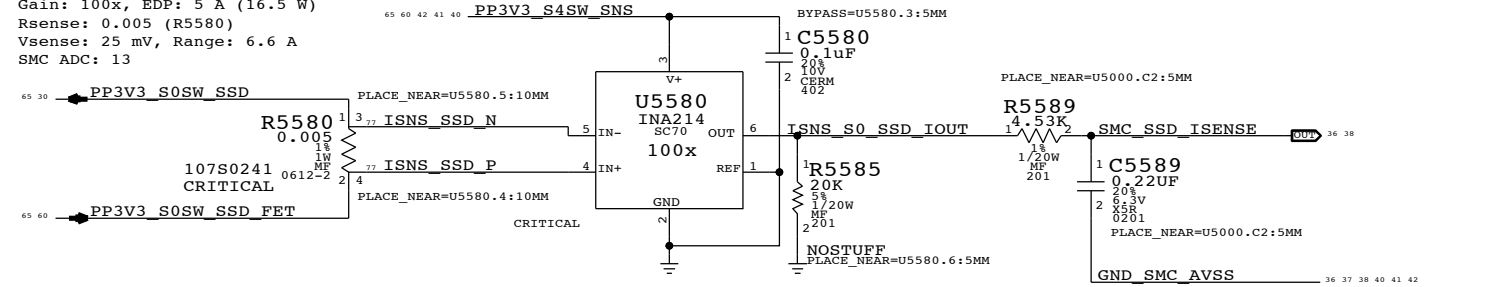
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 15 mV, Range: 40.12 A
SMC ADC: 06



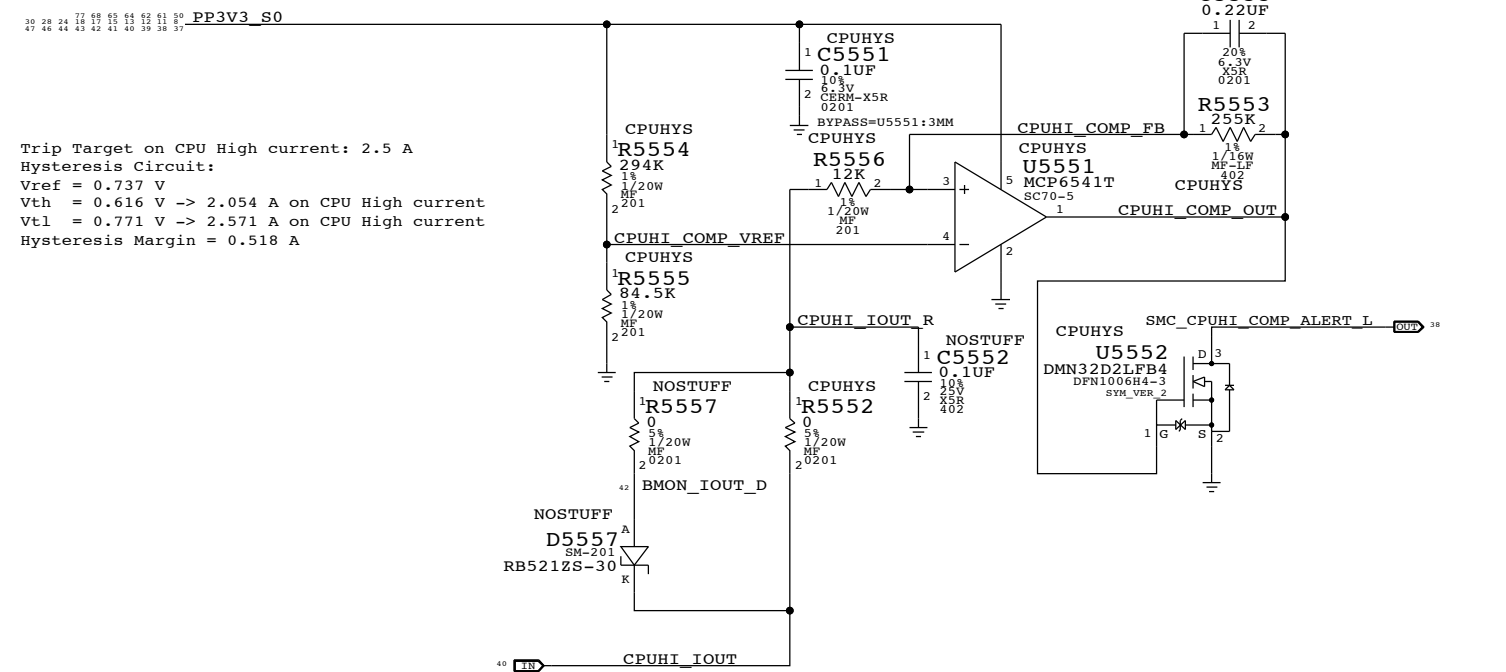
SSD Current Sense (ISDC)

Gain: 100x, EDP: 5 A (16.5 W)
Rsense: 0.005 (R5580)
Vsense: 25 mV, Range: 6.6 A
SMC ADC: 13



CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
Rsense: 0.003 (R5400)



Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRRC:NO

SYNC MASTER=J44 SYNC DATE=08/12/2013

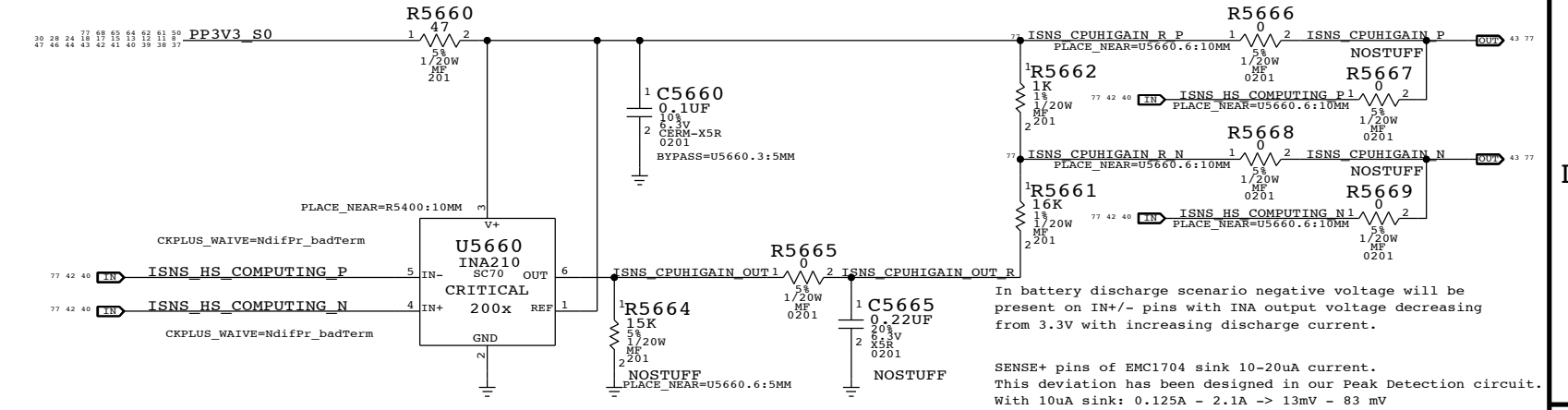
Power Sensors: Load Side

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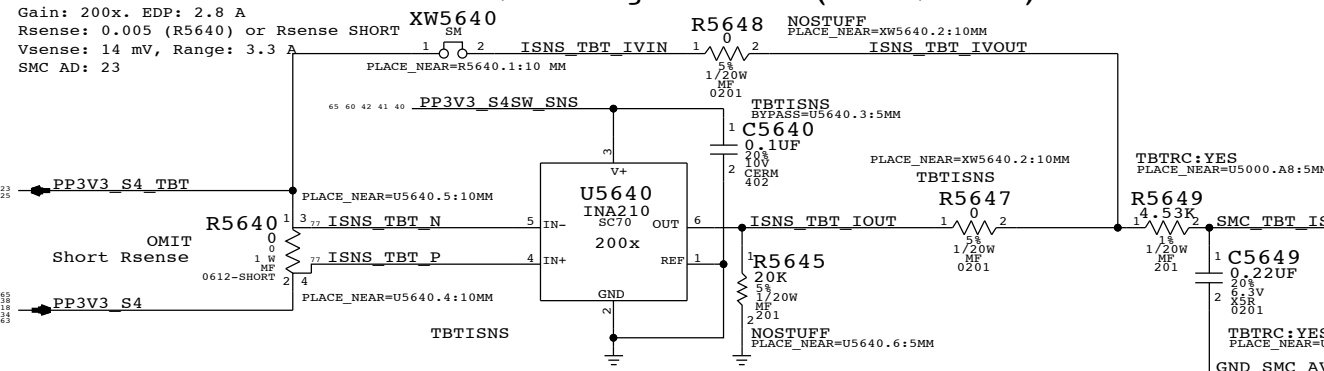
CPU High Side (IC0R) Peak Detection Support



In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

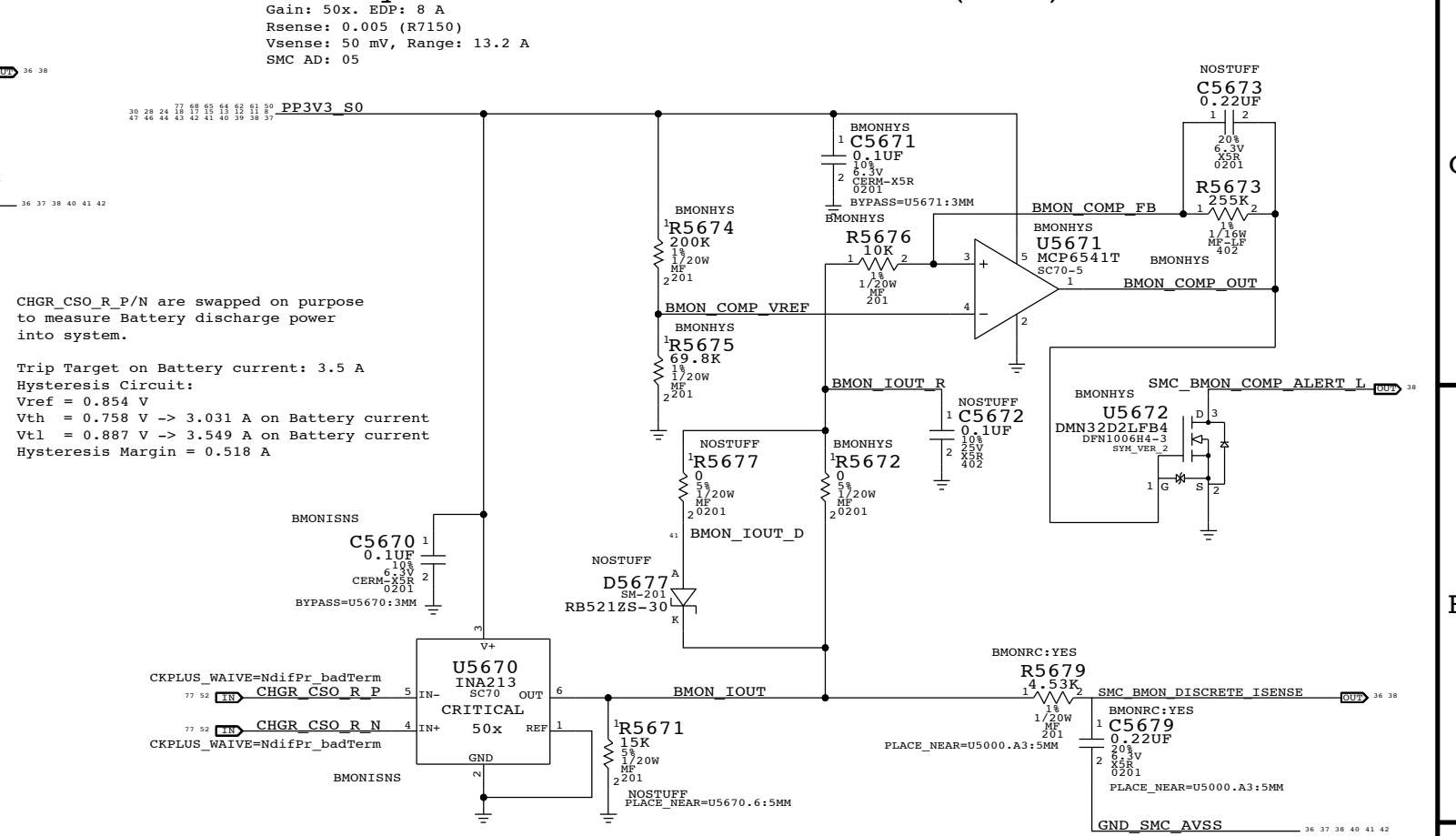
SENSE+ pins of EMC1704 sink 10-20uA current. This deviation has been designed in our Peak Detection circuit. With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)



Gain: 200x. EDP: 2.8 A
Rsense: 0.005 (R5640) or Rsense SHORT
Vsense: 14 mV, Range: 3.3 A
SMC AD: 23

Battery BMON Discrete Current Sense (IP0R) & Threshold Alert

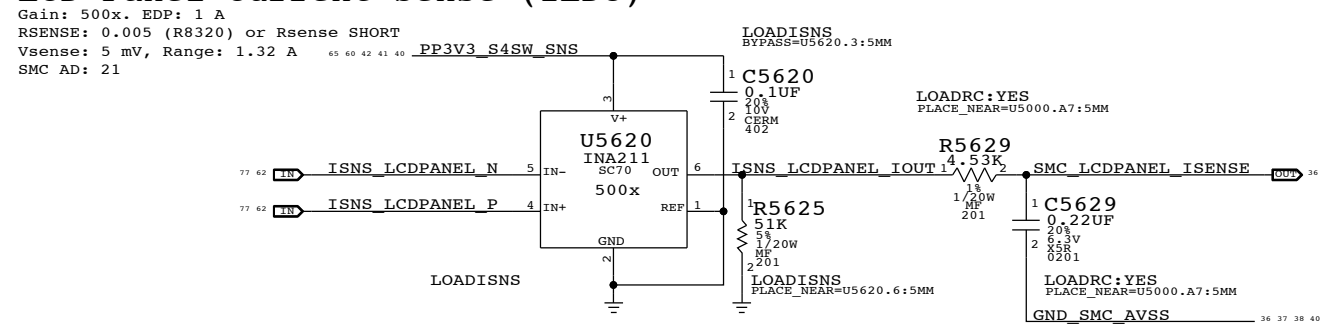


Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05

CHGR_CS0_R/P/N are swapped on purpose to measure Battery discharge power into system.

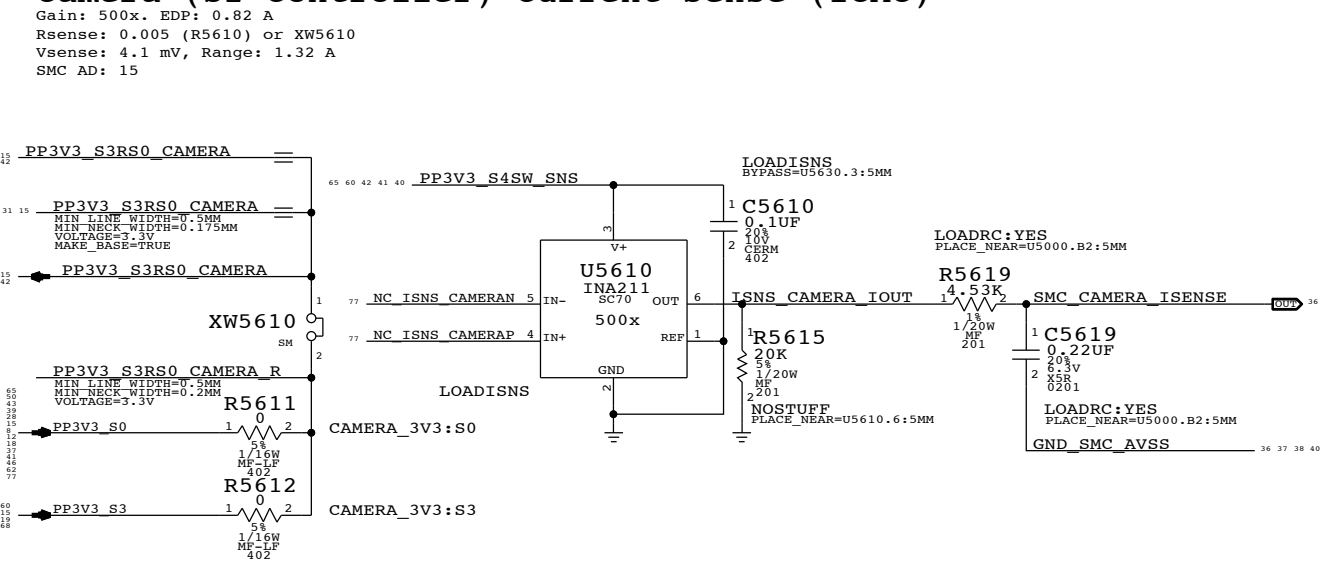
Trip Target on Battery current: 3.5 A
Hysteresis Circuit:
Vref = 0.854 V
Vth = 0.758 V -> 3.031 A on Battery current
Vtl = 0.887 V -> 3.549 A on Battery current
Hysteresis Margin = 0.518 A

LCD Panel Current Sense (ILDC)



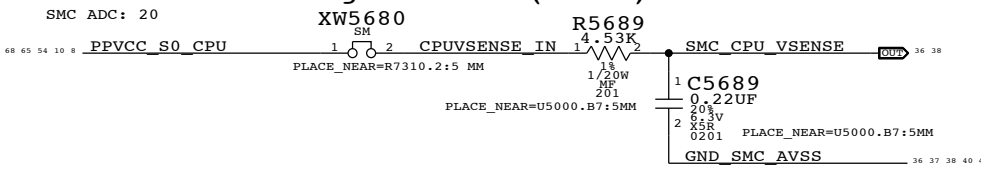
Gain: 500x. EDP: 1 A
RSENSE: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC AD: 21

Camera (S2 Controller) Current Sense (ICMC)



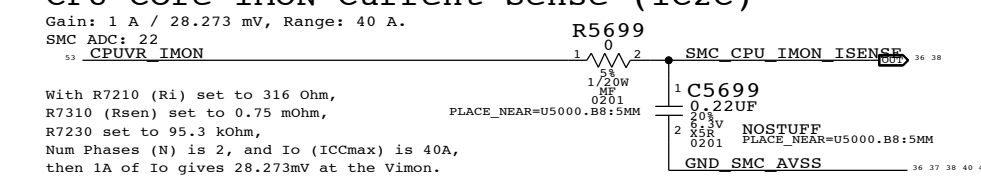
Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15

CPU Core Voltage Sense (VC0C)



SMC ADC: 20
XW5680

CPU Core IMON Current Sense (IC2C)



Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 22
CPUVR IMON

With R7210 (Ri) set to 316 Ohm, R7310 (Rsen) set to 0.75 mOhm, R7230 set to 95.3 kOhm, Num Phases (N) is 2, and Io (ICmax) is 40A, then 1A of Io gives 28.273mV at the Vimon.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5649		
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		

SYNC MASTER=144 SYNC DATE=08/12/2013

Power Sensors: Extended

Apple Inc.

Apple logo

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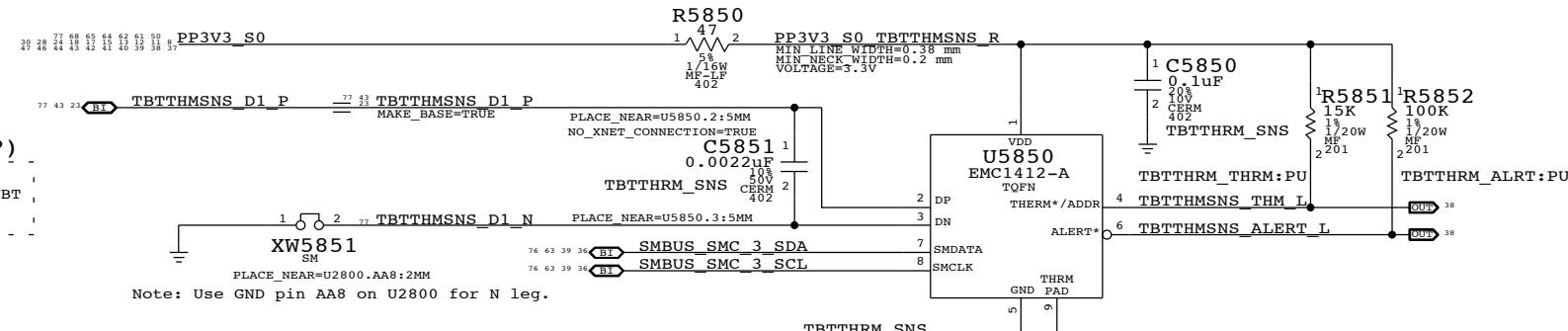
DRAWING NUMBER: <SCH NUM> D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 56 OF 120
SHEET: 42 OF 78

Thermal Sensor A: Thunderbolt Die, MLB Proximity

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (THSP)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.



U5850 I2C Address:
By setting R5851 to 15k, I2C address for U5850 is 0xD8/0xD9.

Thermal Diode: MLB Proximity (TMLB)

Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor B & CPU High Peak Detection: CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5871, Airflow thermal indicator, above the SSD, on the BOTTOM side.

Thermal Diode: Memory Proximity (TM0P)

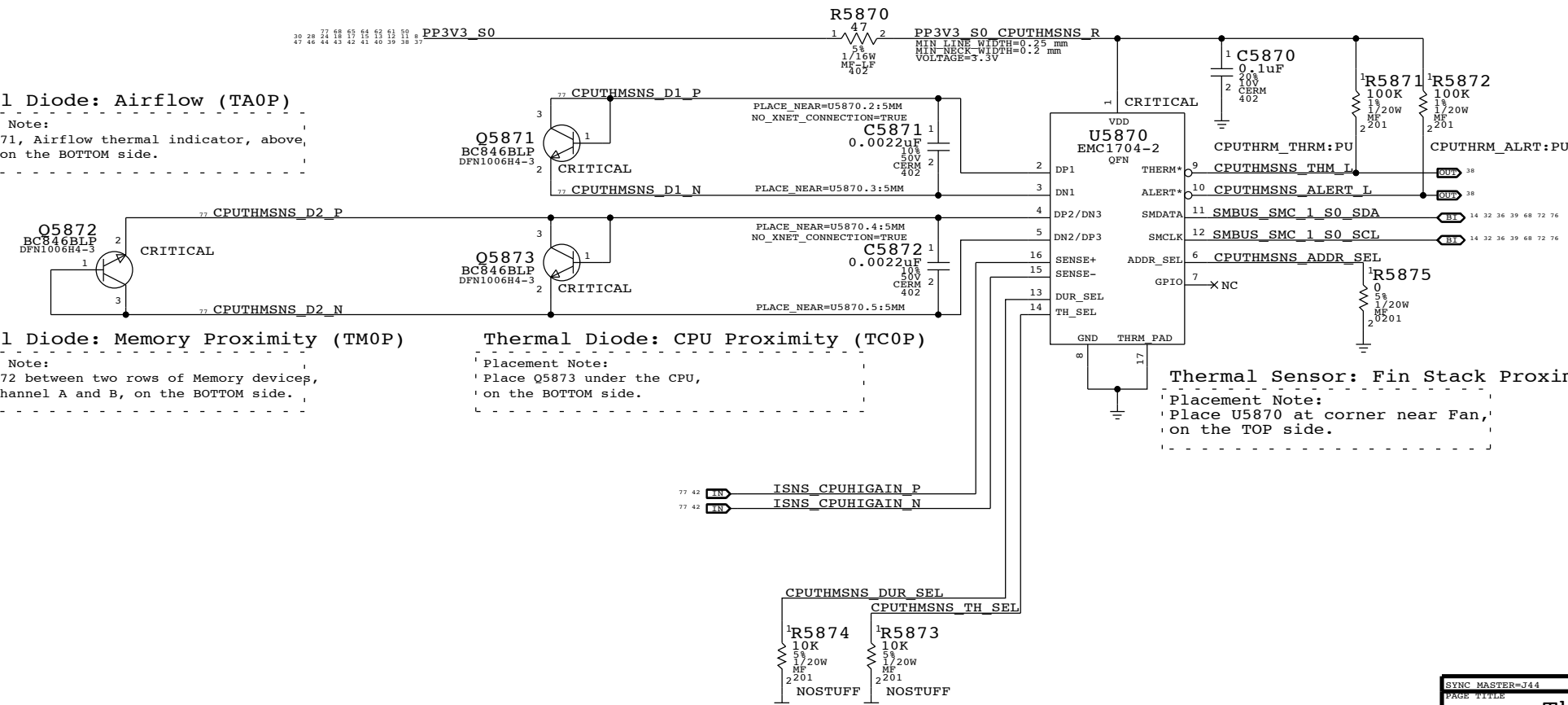
Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Diode: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Sensor: Fin Stack Proximity (Th1H)

Placement Note:
Place U5870 at corner near Fan, on the TOP side.

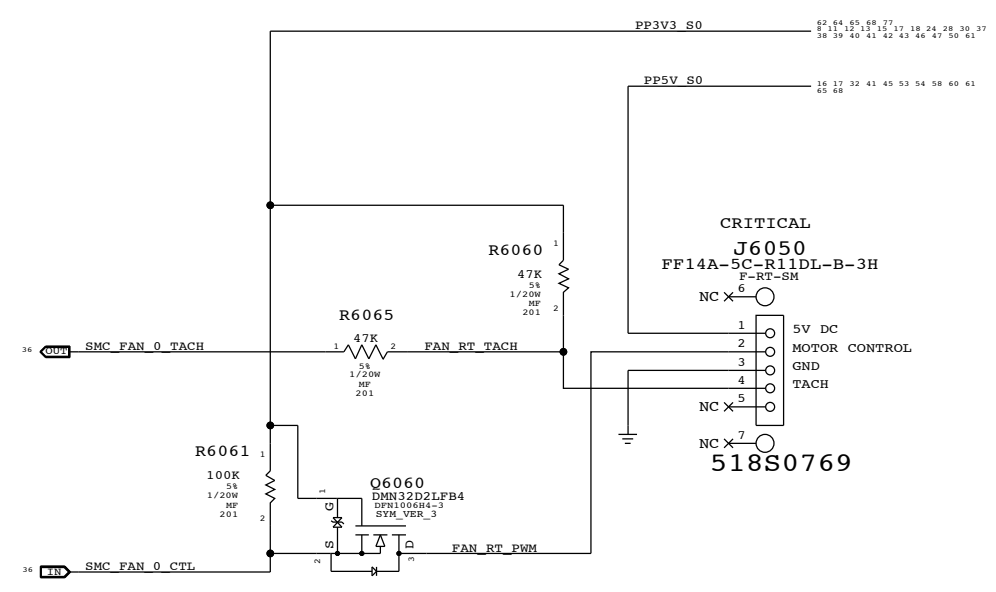


SYNC MASTER=144		SYNC DATE=08/12/2013	
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Thermal Sensors		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
		REVISION	<E4LABEL>
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8 7 6 5 4 3 2 1

FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1



D
C
B
A

D
C
B
A

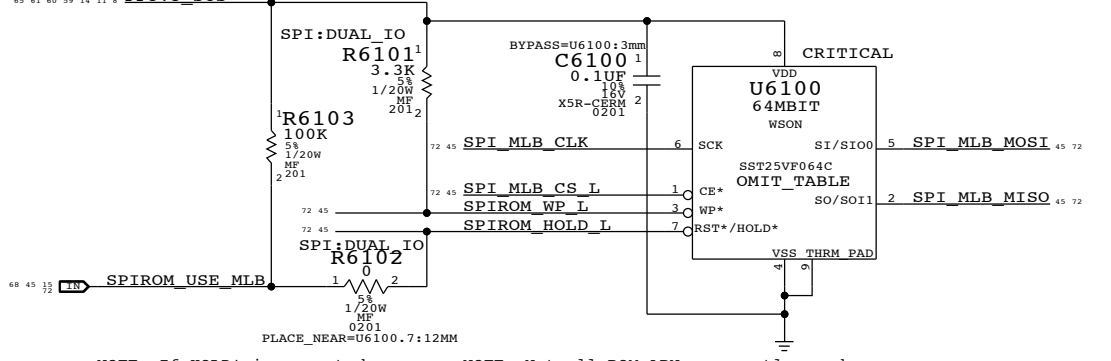
8 7 6 5 4 3 2 1

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
Fan			
	DRAWING NUMBER	SIZE	
	<SCH_NUM>	D	
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	<E4LABEL>	<BRANCH>	
	PAGE	SHEET	
	60 OF 120	44 OF 78	

8 7 6 5 4 3 2 1

SPI ROM

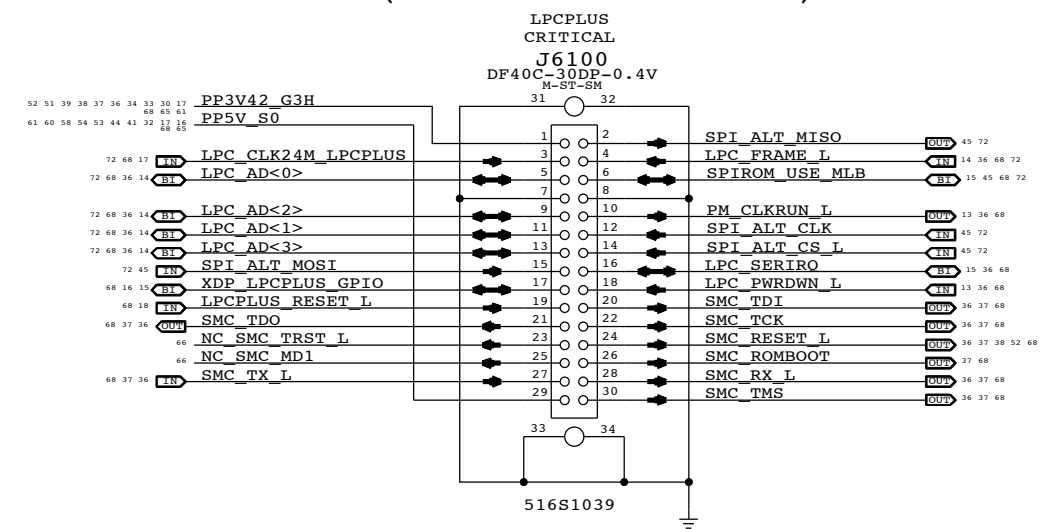
Dual-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



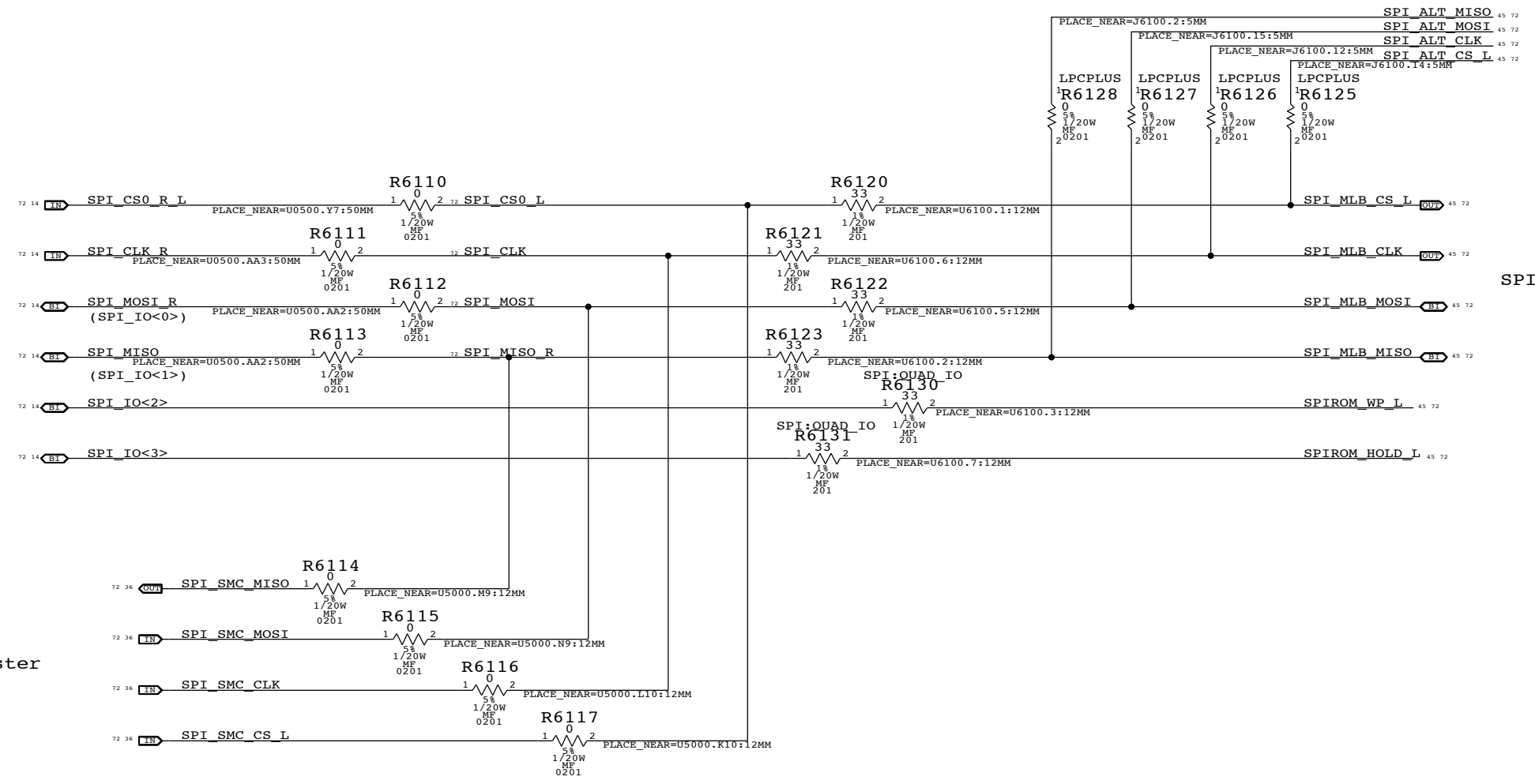
NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and Dual-IO modes.

NOTE: Not all ROM APNs currently used support Quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

LPC+SPI Connector (Matt Card Connector)



SPI Bus Series Termination



Matt Card ROM Slave

SPI ROM Slave

CPU Master

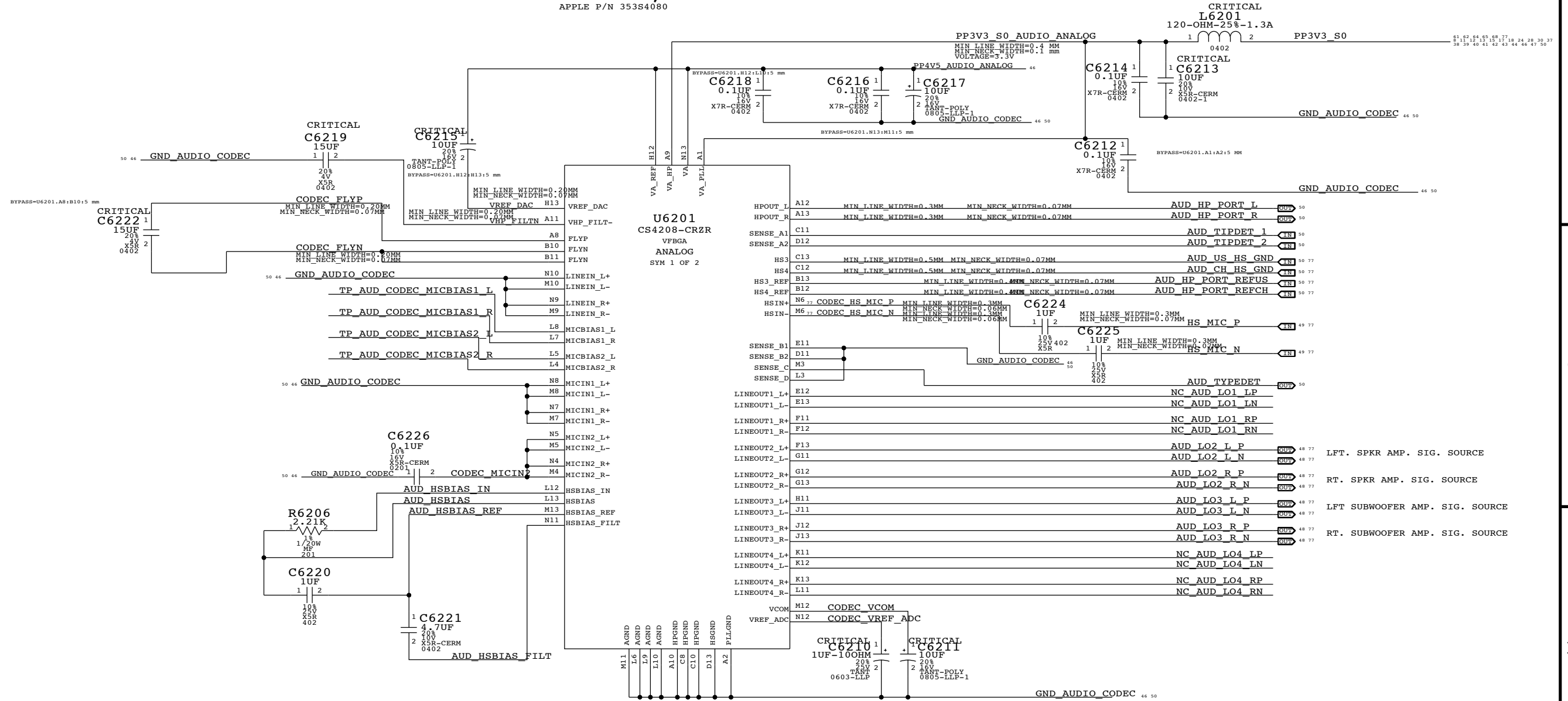
SMC12 Master

SYNC MASTER=J44		SYNC DATE=08/12/2013	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
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		SHEET	45 OF 78

8 7 6 5 4 3 2 1

AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080

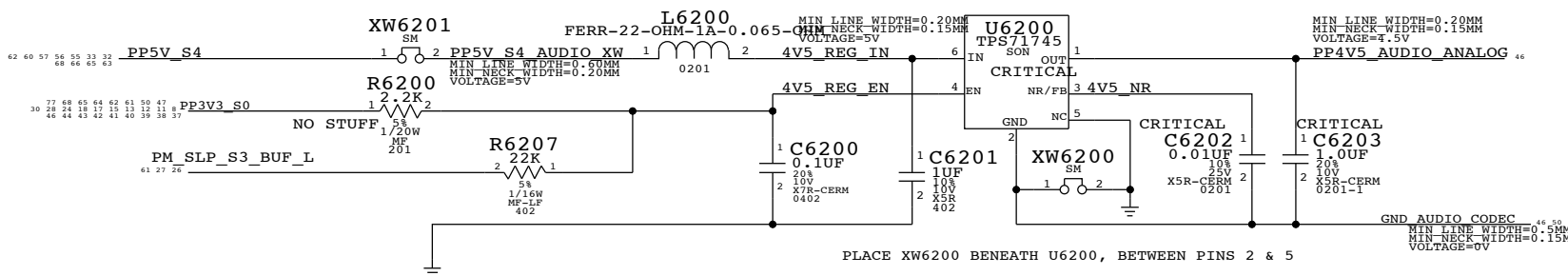


4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE

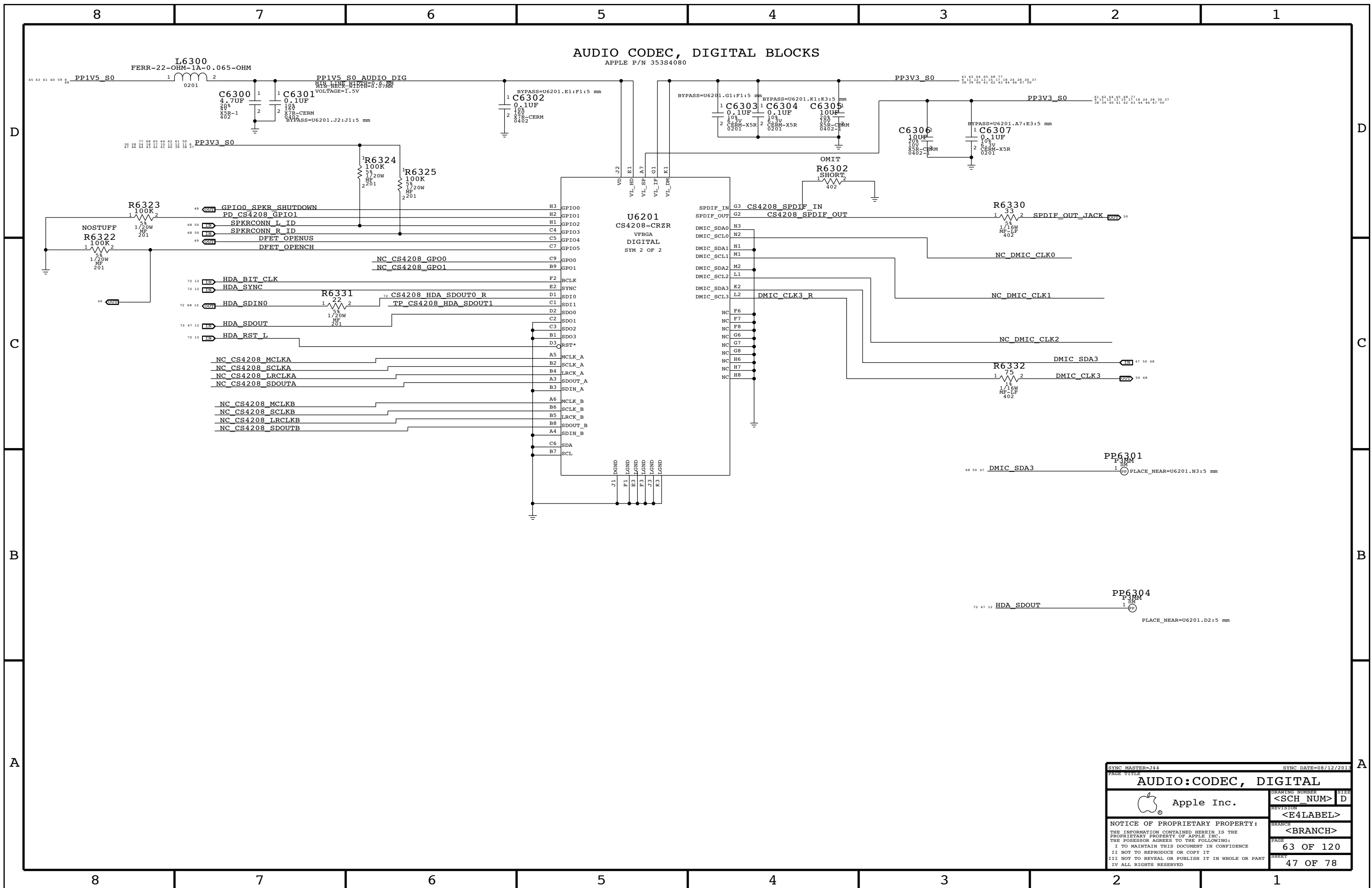
PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5



SYNC MASTER=144		SYNC DATE=08/12/2011	
PAGE TITLE			
AUDIO:CODEC, ANALOG		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
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AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
AUDIO:CODEC, DIGITAL			
Apple Inc.	DRAWING NUMBER		SIZE
	<SCH NUM>		D
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	<E4LABEL>		<BRANCH>
	PAGE		63 OF 120
SHEET		47 OF 78	

8

7

6

5

4

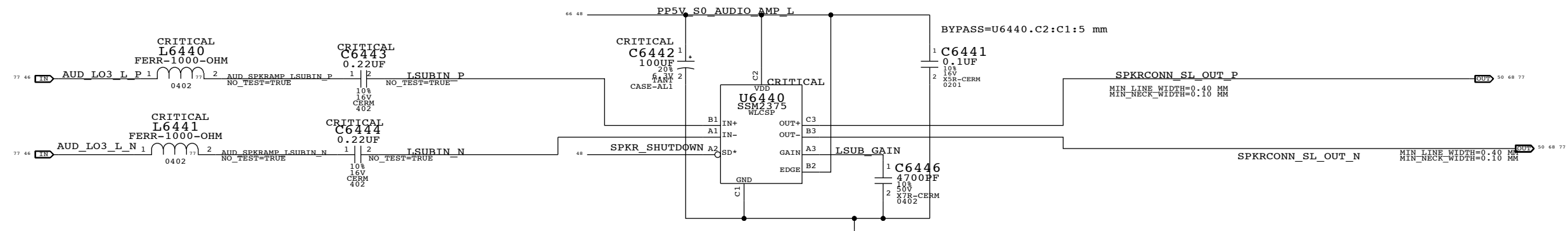
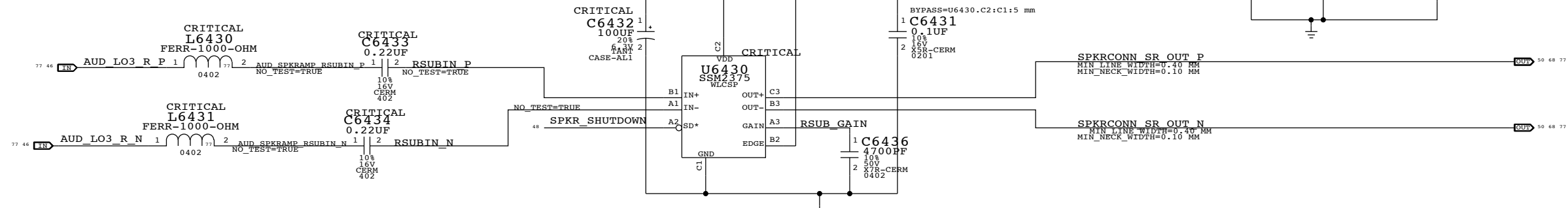
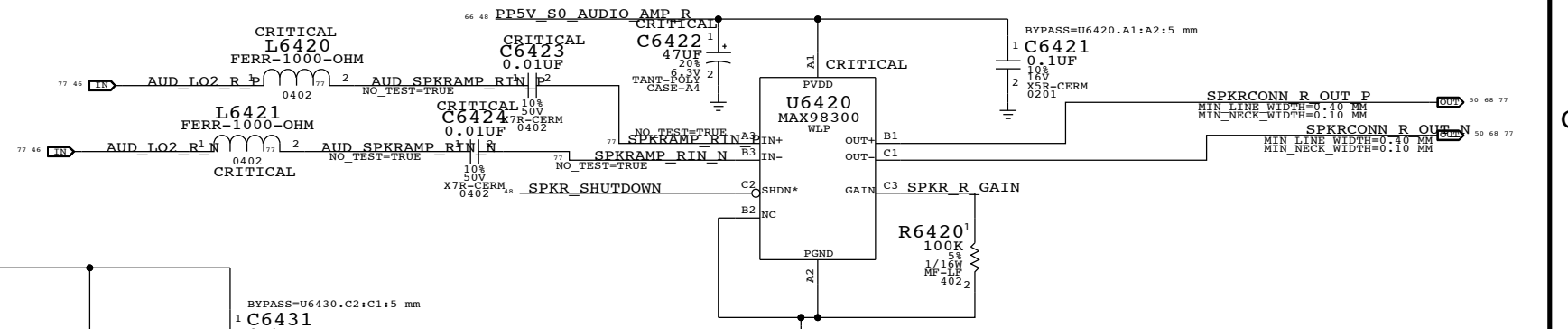
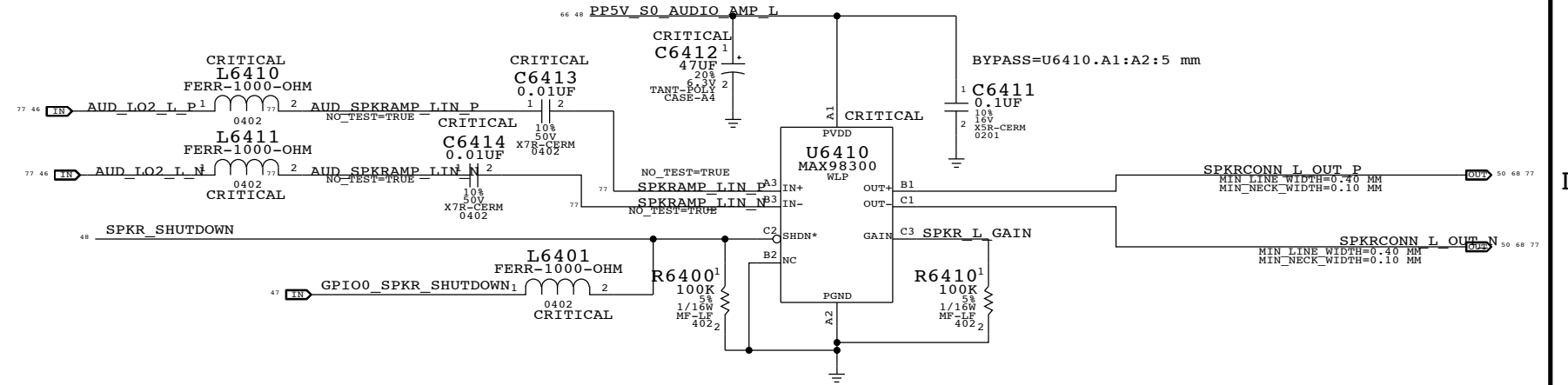
3

2

1

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
 GAIN = +3 DB
 1ST ORDER FC (L&R) = NOM 569 HZ
 1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
		REVISION	
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		PAGE	64 OF 120
		SHEET	48 OF 78

8

7

6

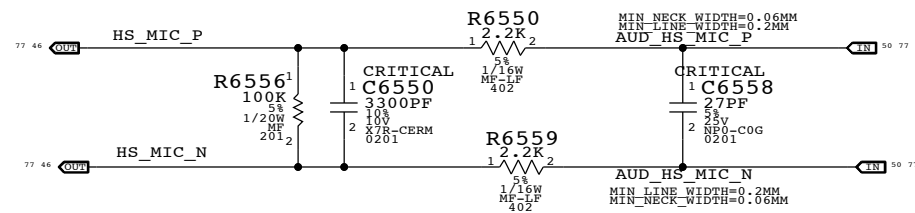
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4

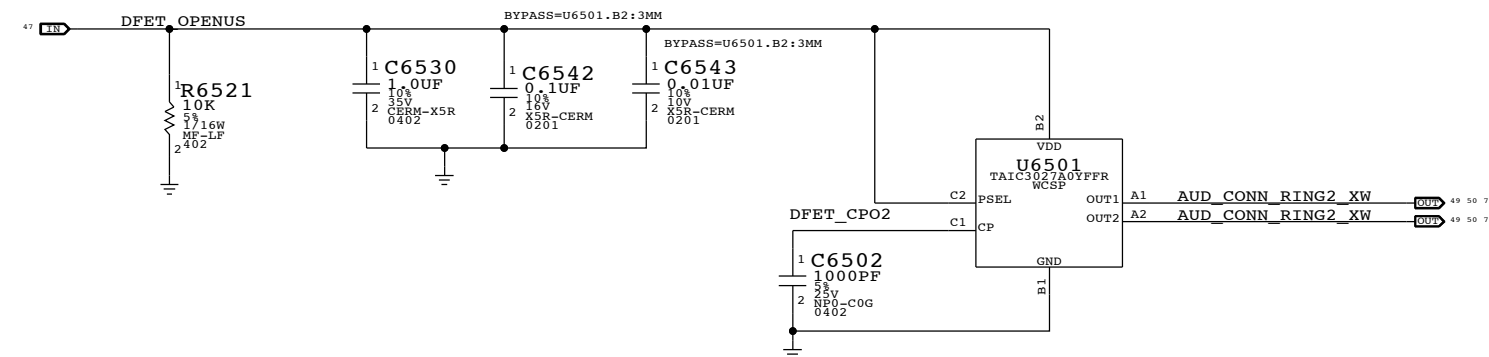
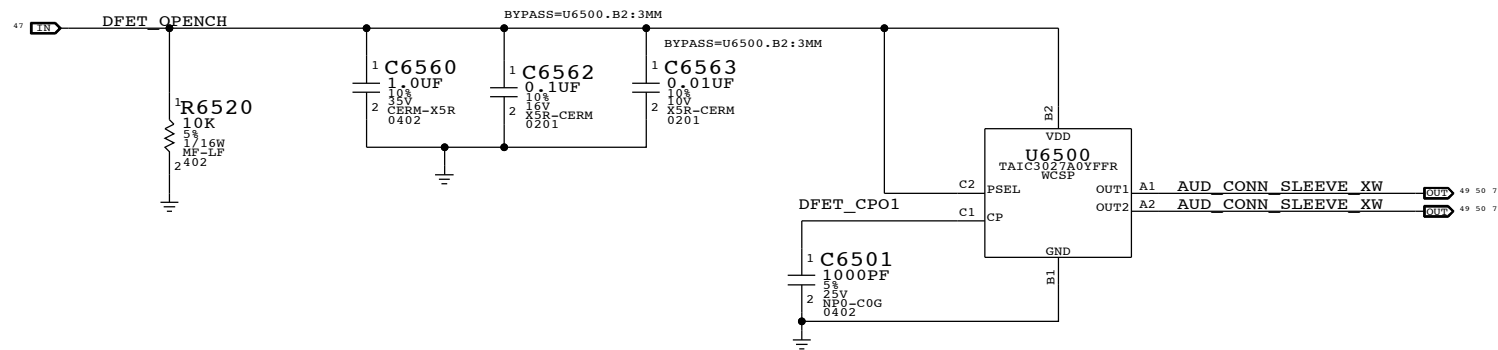
3

2

1



R/C6550 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)



SYNC MASTER=J44		SYNC DATE=08/12/2013	
AUDIO: JACK			
Apple Inc.		DRAWING NUMBER	SIZE
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		BRANCH	<E4LABEL>
		PAGE	<BRANCH>
		SHEET	65 OF 120
			49 OF 78

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETS OPEN

SPEAKER CONNECTOR

HP=80HZ
APN: 518S0672

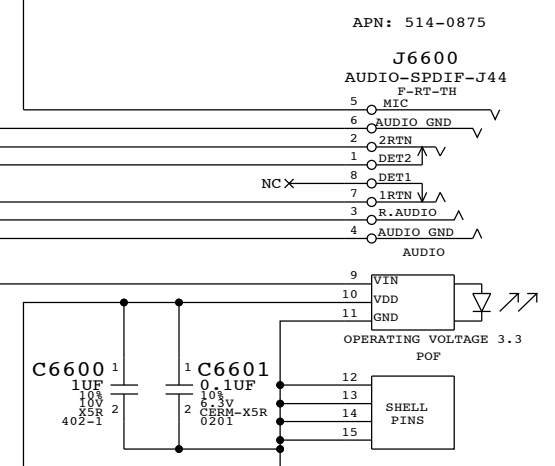
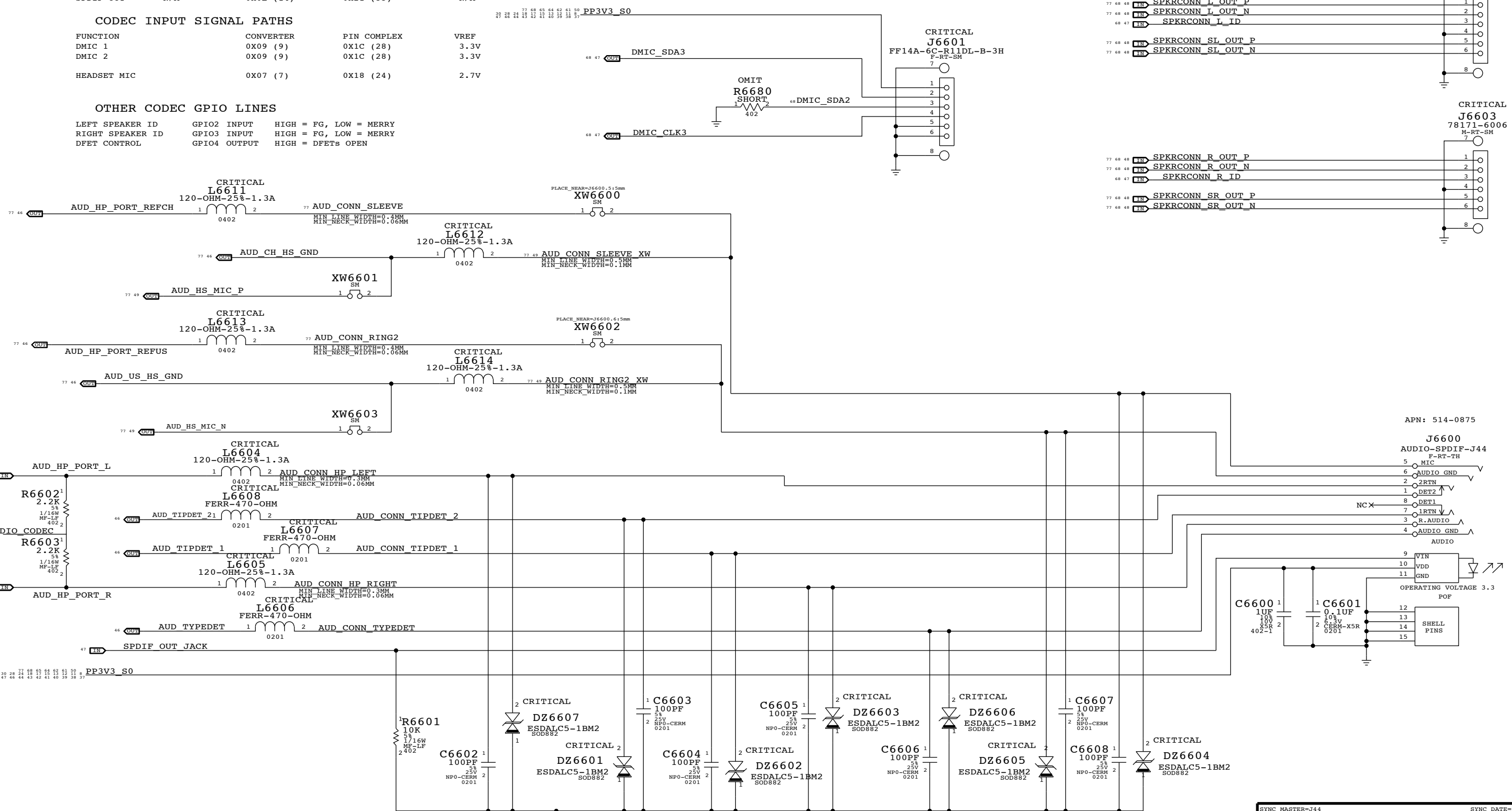
CRITICAL
J6602
78171-6006
M-RT-SM

2-MIC CONNECTOR

APN: 518S0818

CRITICAL
J6601
FF14A-6C-R11DL-B-3H
F-RT-SM

CRITICAL
J6603
78171-6006
M-RT-SM



SYNC MASTER=J44 SYNC DATE=08/12/2011

AUDIO: JACK TRANSLATORS

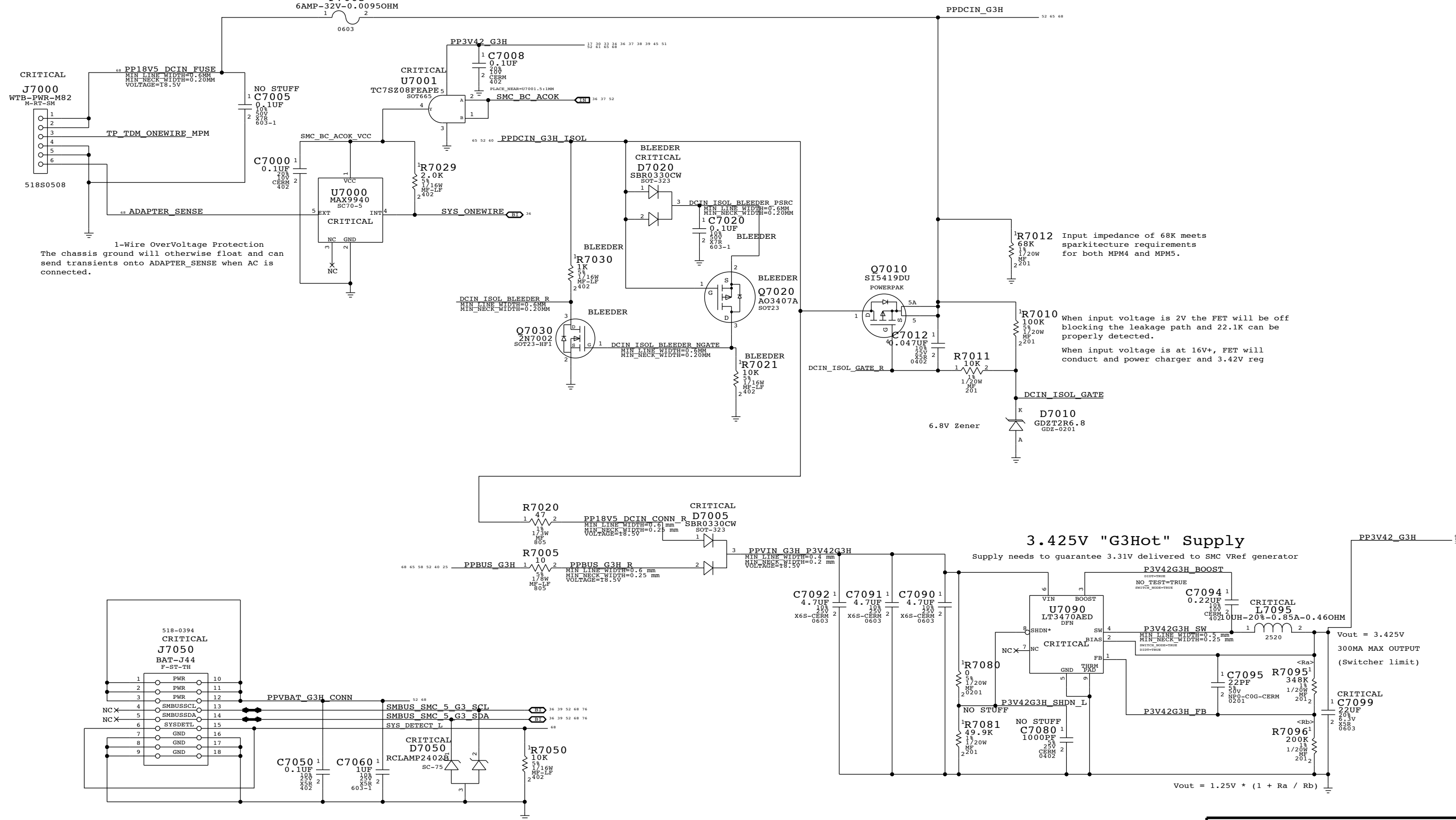
Apple Inc.

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<SCH_NUM>	D
REVISION	
<E4LABEL>	
BRANCH	
<BRANCH>	
PAGE	
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8 7 6 5 4 3 2 1

MagSafe DC Power Jack



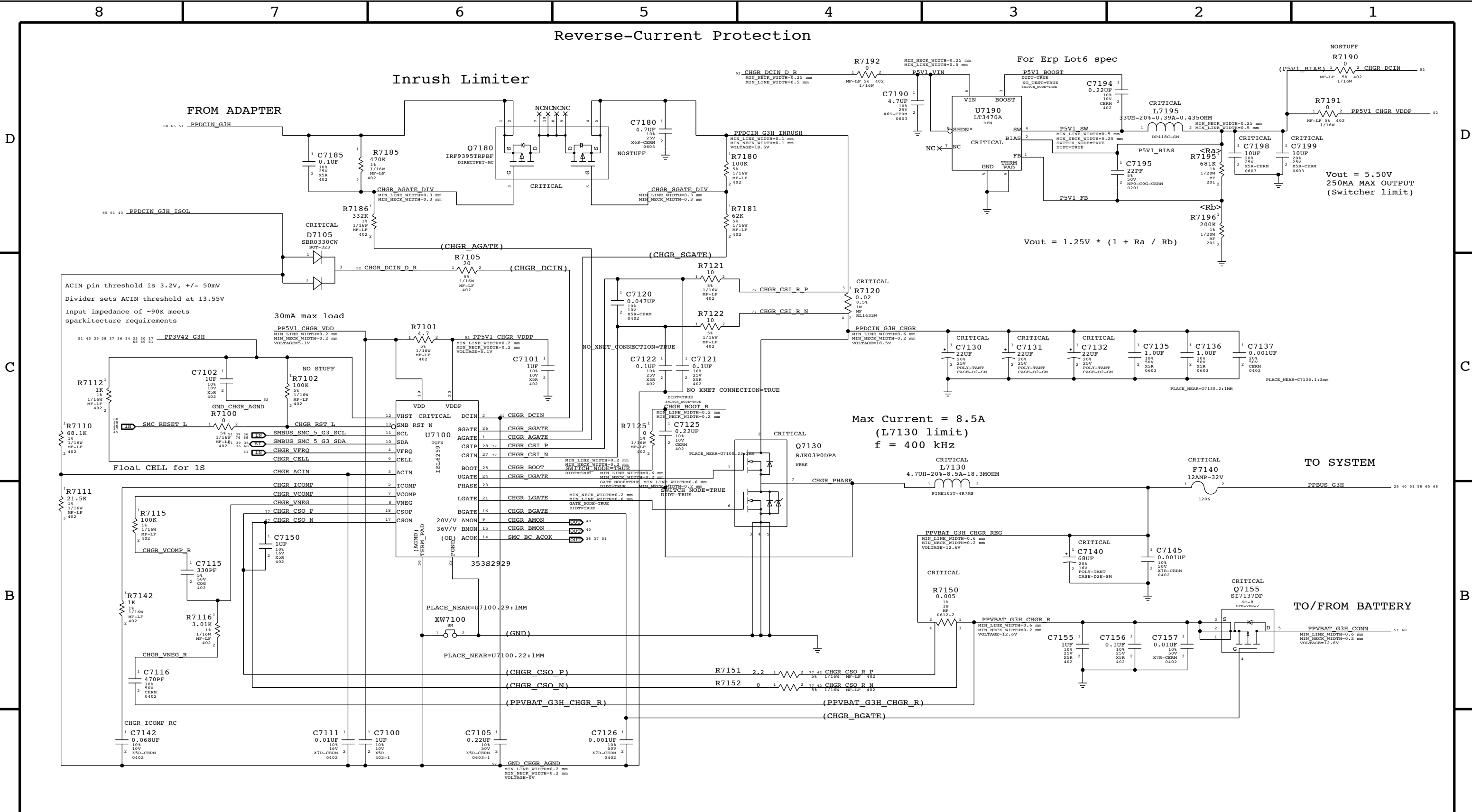
DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: <SCH NUM> D
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Reverse-Current Protection

Inrush Limiter

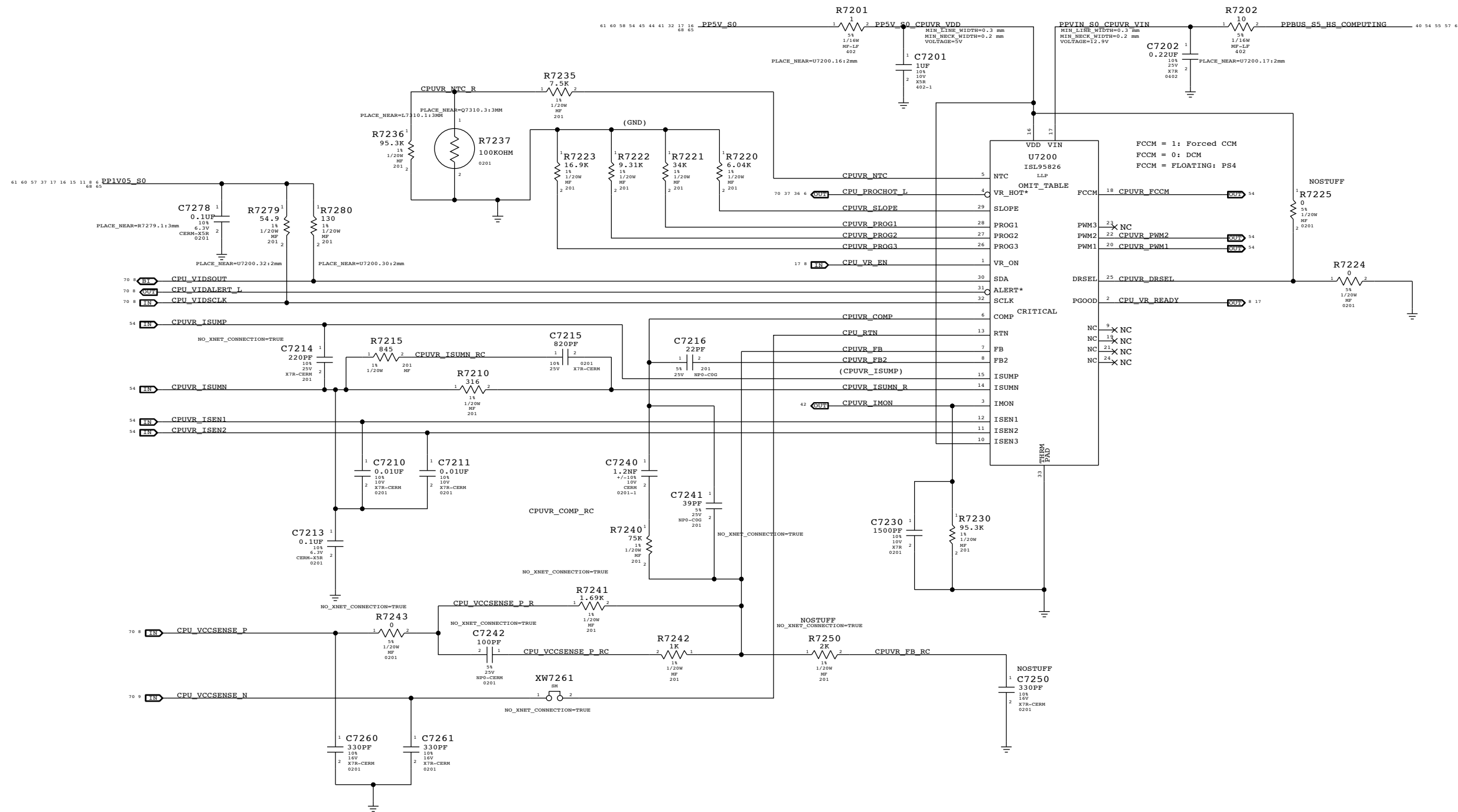
For Erp Lot6 spec

NOSTUFF

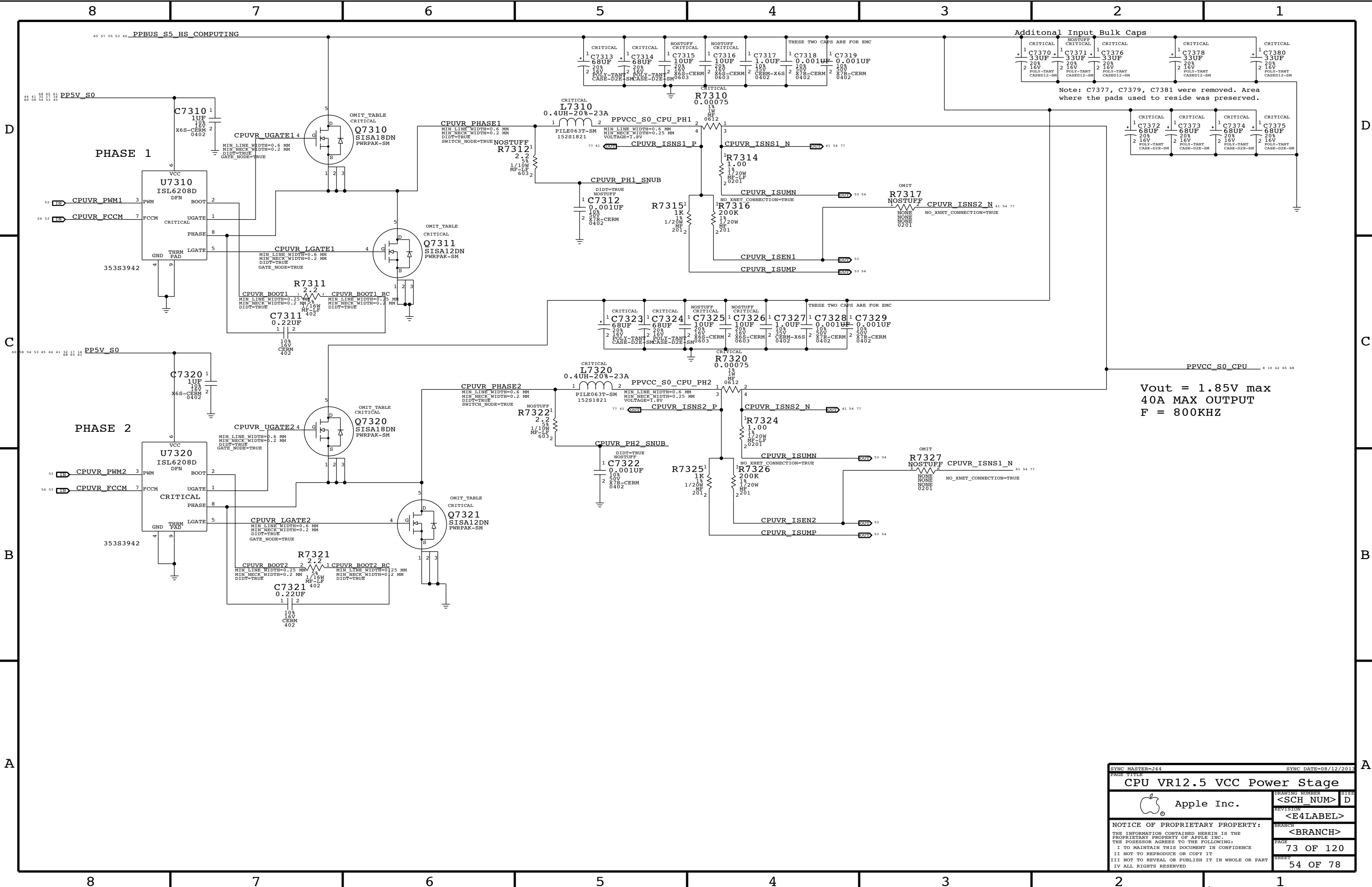


SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
PBus Supply & Battery Charger			
Apple Inc.	DRAWING NUMBER	<SCH_NUM>	SIZE
	REVISION	<E4LABEL>	
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	PAGE	71 OF 120	
	SHEET	52 OF 78	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC, ISL95826R6200, PWM, PGOOD, SCREEN, 32P, QFN	U7200	CRITICAL	



SYNC MASTER=144		SYNC DATE=08/12/2013	
CPU VR12.6 VCC Regulator IC			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	<E4LABEL>
		BRANCH	<BRANCH>
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		SHEET	53 OF 78



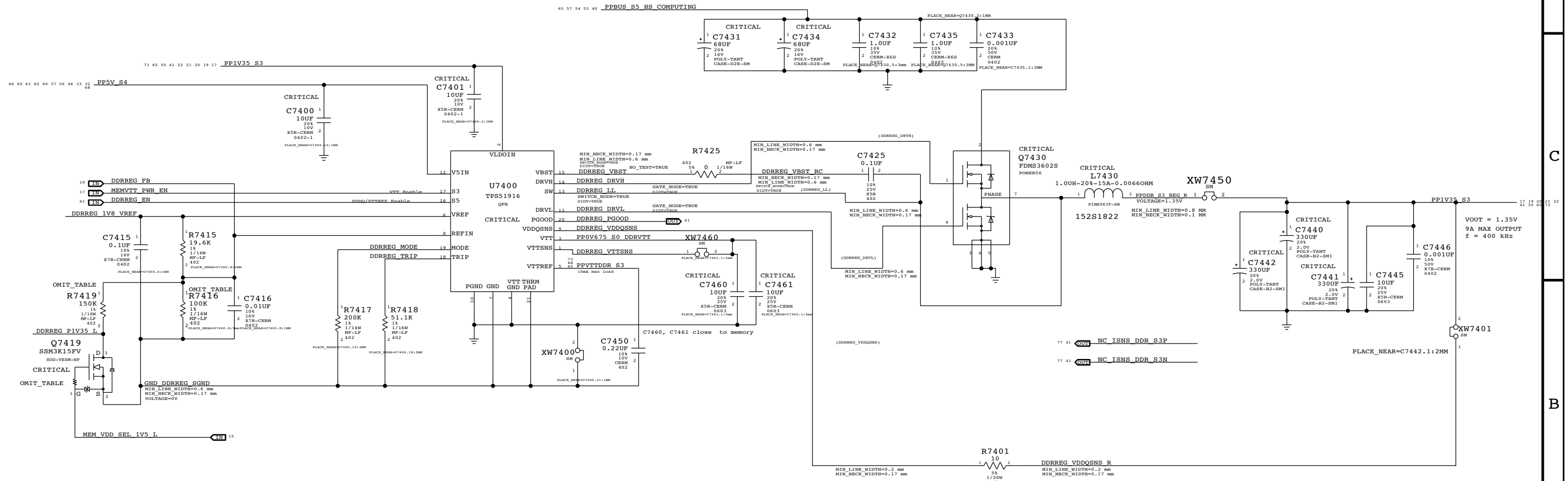
Additional Input Bulk Caps

Note: C7377, C7379, C7381 were removed. Area where the pads used to reside was preserved.

Vout = 1.85V max
40A MAX OUTPUT
F = 800KHZ

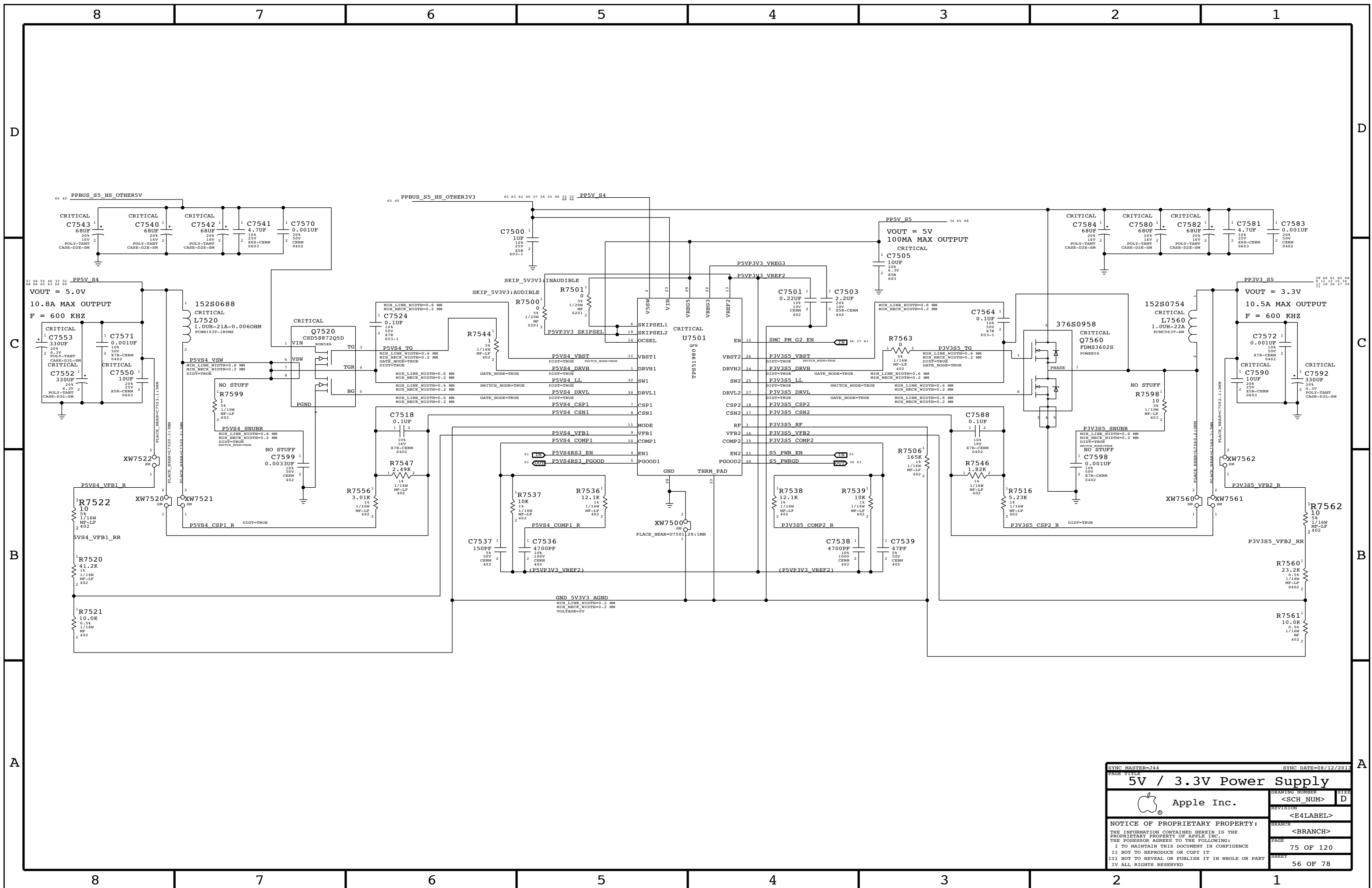
SYNCH MASTER=144		SYNCH DATE=08/12/2013	
CPU VR12.5 VCC Power Stage			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		<E4LABEL>	
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DDR3L (1V35 S3) REGULATOR



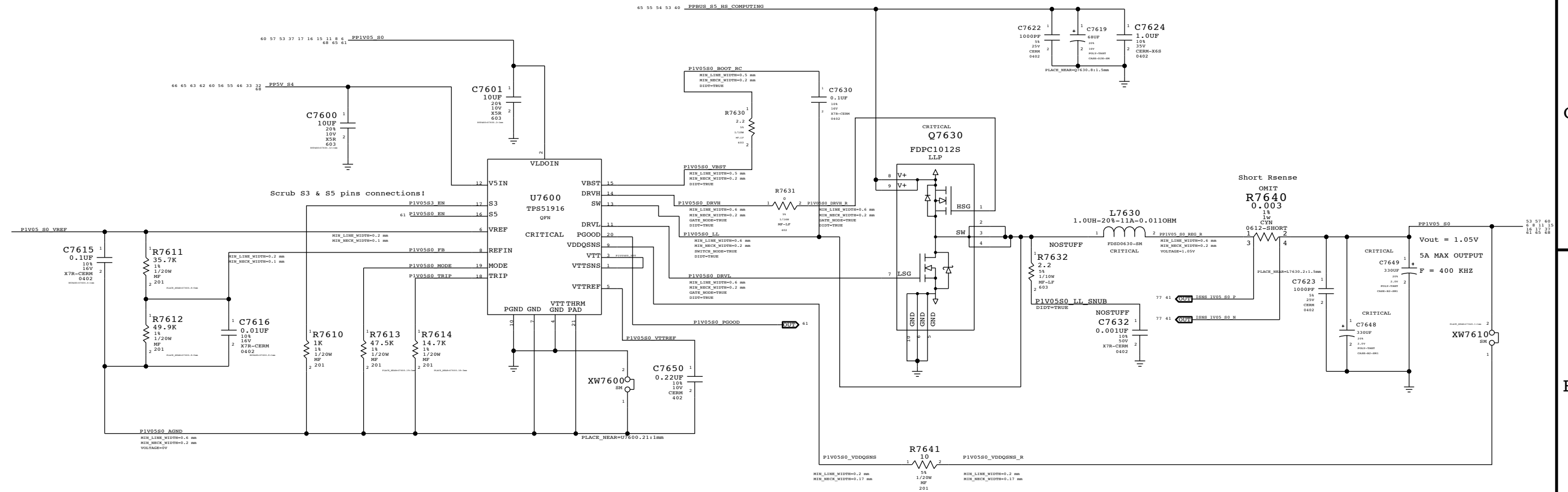
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.00HM,SOT-723,HF	Q7419	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150K,0402,SMD,LF	R7419	CRITICAL	PPDDR:1V5

SYNC MASTER/SLAVE PAGE TITLE		SYNC DATE/REV/12/2015	
1.35V DDR3 SUPPLY			
Apple Inc.		DRAWING NUMBER <SCH_NUM>	SIZE D
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		PAGE 74 OF 120	SHEET 55 OF 78



SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE			
5V / 3.3V Power Supply			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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		PAGE	75 OF 120
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1.05V S0 Regulator

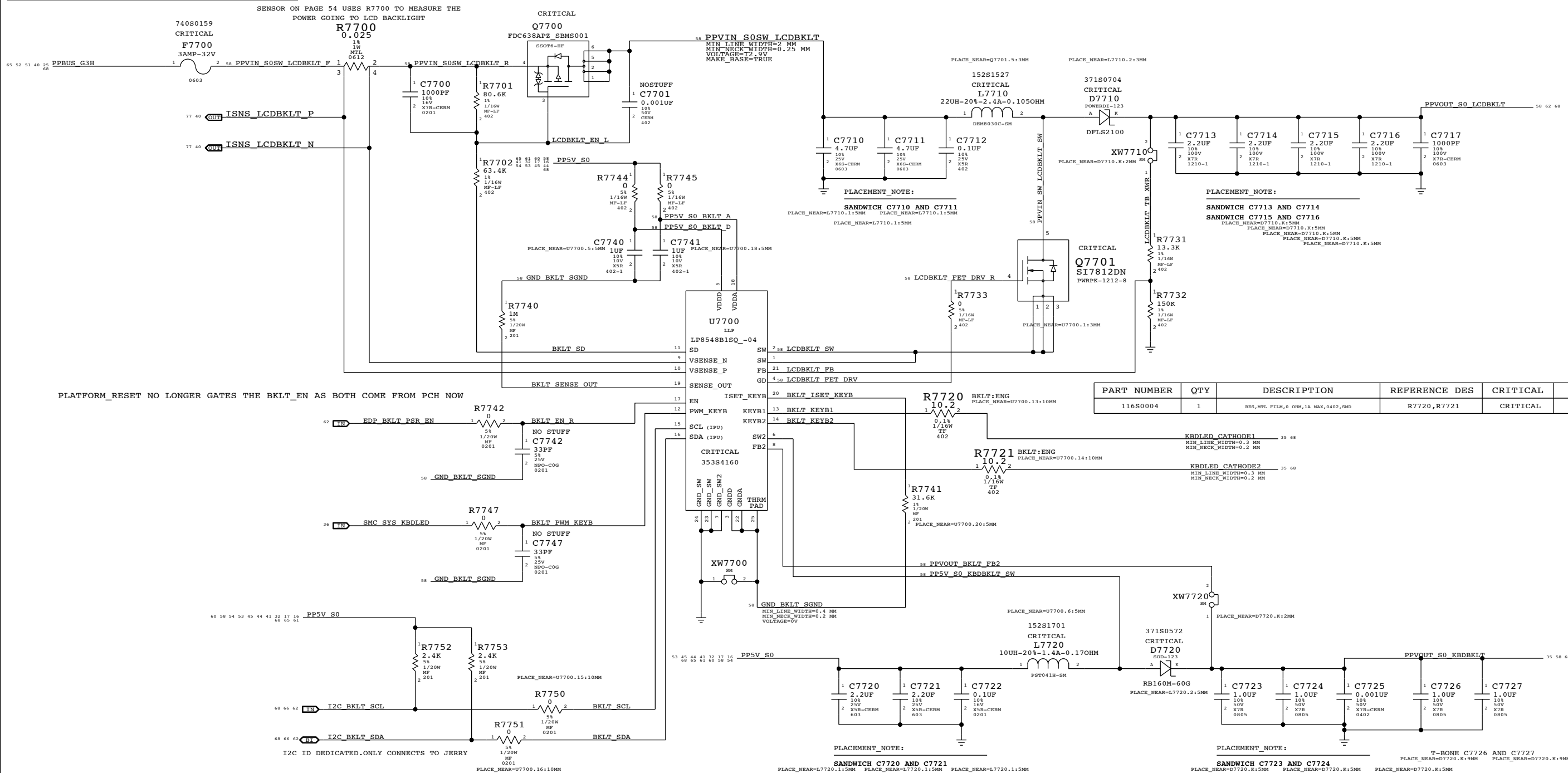


SYNC MASTER=144		SYNC DATE=08/12/2013	
PAGE TITLE: 1.05V S0 Power Supply			
DRAWING NUMBER: <SCH_NUM>		SIZE: D	
REVISION: <E4LABEL>		BRANCH: <BRANCH>	
PAGE: 76 OF 120		SHEET: 57 OF 78	
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Page Notes

Power aliases required by this page:
 - =PPVIN_S0SW_LCDBKLTFT (9-12.6V LCD BACKLIGHT INPUT)
 - =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
 - =PP5V_S0SW_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

BOM options provided by this page:
 BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
 BKLT:PROD - Stuffs 0 ohm series R for production



PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL,P1L,M,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PBUS LINE WIDTHS

LCD BKLT LINE WIDTHS

KBD BKLT LINE WIDTHS

- PP5V_S0_BKLT_A 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
- PP5V_S0_BKLT_D 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
- PPVIN_S0SW_LCDBKLT_F 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT_R 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT_FET 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=12.9V
- LCDBKLT_FET_DRV_R 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
GATE_MODE=TRUE
DIDT=TRUE
- LCDBKLT_FET_DRV 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
GATE_MODE=TRUE
DIDT=TRUE
- LCDBKLT_SW 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
SWITCH_MODE=TRUE
DIDT=TRUE
- PPVIN_SW_LCDBKLT_SW 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
SWITCH_MODE=TRUE
DIDT=TRUE
- PP5V_S0_KBDBKLT_SW 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
SWITCH_MODE=TRUE
DIDT=TRUE
- PPVOUT_S0_LCDBKLT 58 62 68
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=40V
- PPVOUT_BKLT_FB2 58
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=40V

SYNC MASTER=144 SYNC DATE=08/12/2013

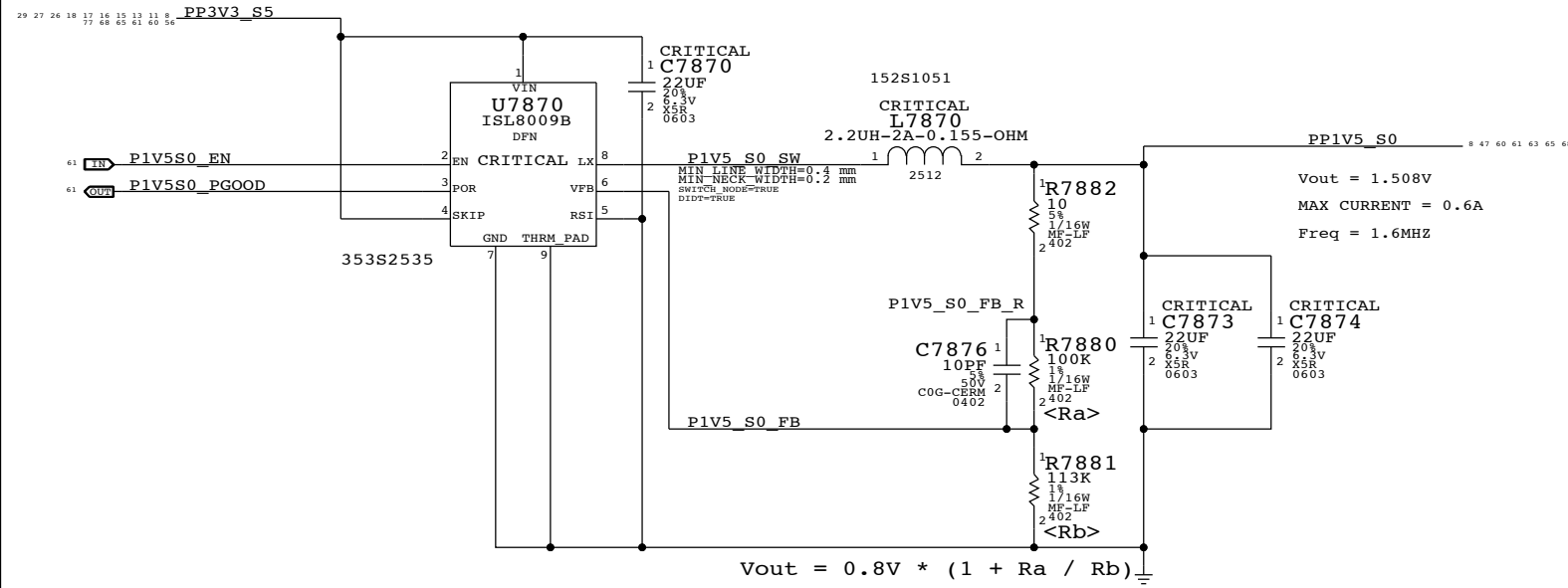
LCD AND KBD BKLT DRIVER

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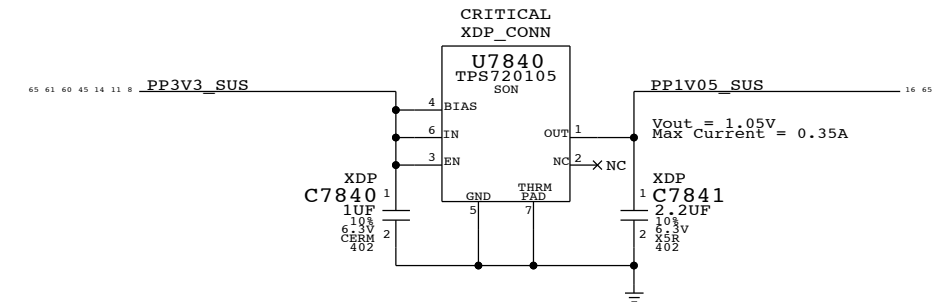
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 REVISION: <E4LABEL>
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1.5V S0 Switcher



1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

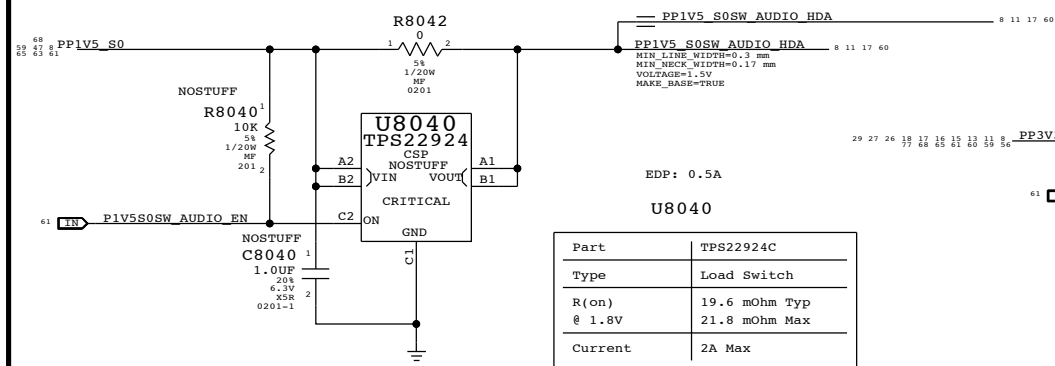


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Apple Inc.	DRAWING NUMBER	<SCH_NUM>	SIZE
	REVISION	<E4LABEL>	
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	SHEET	59 OF 78	

1.5V S0 Audio Switch (BYPASSED)

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

3.3V SUS Switch



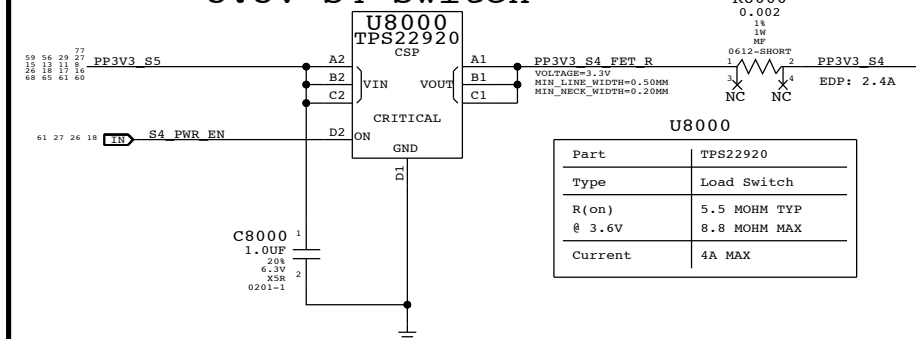
Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

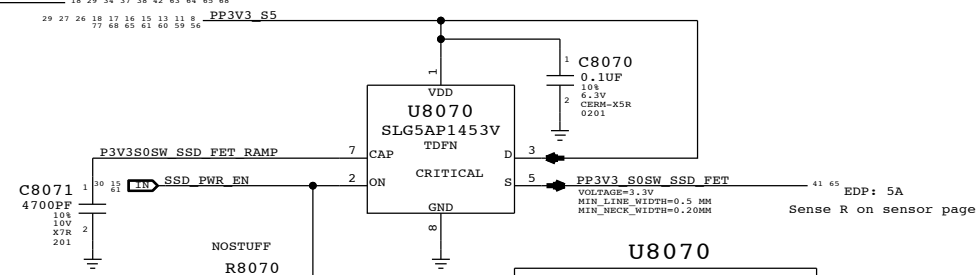
3.3V S4 Switch

3.3V SSD Switch

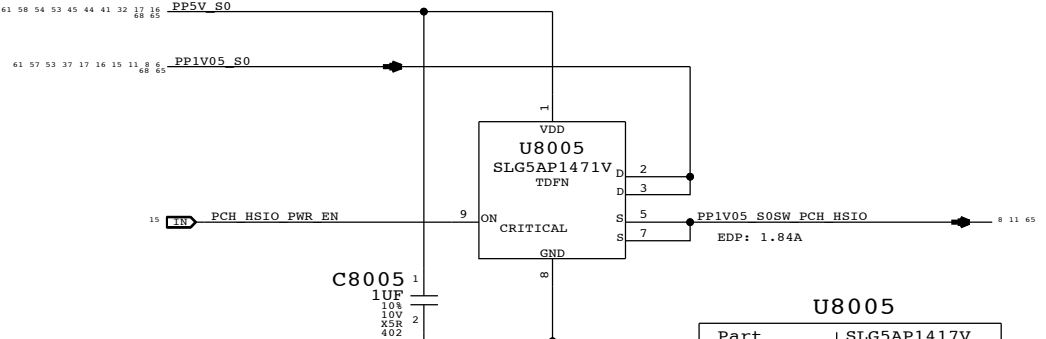
1.05V PCH HSIO Switch



Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.5 MOHM TYP 8.8 MOHM MAX
Current	4A MAX

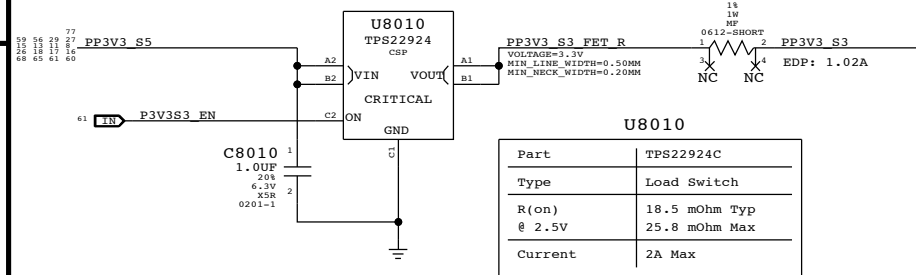


Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max



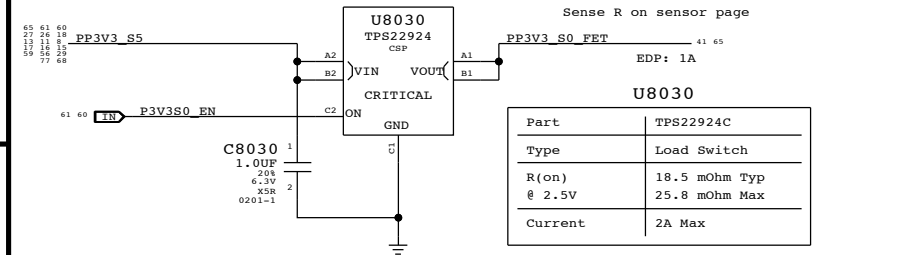
Part	SLG5AP1471V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

3.3V S3 Switch



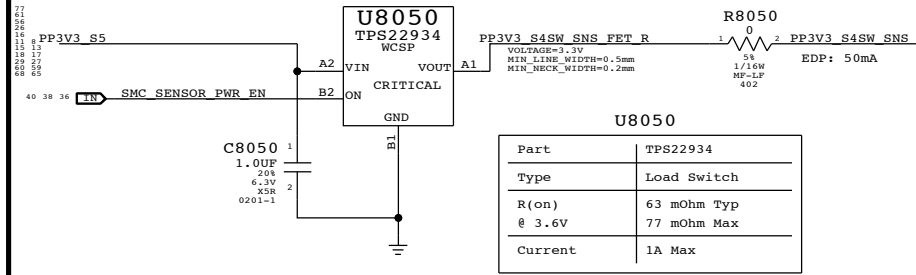
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V S0 Switch



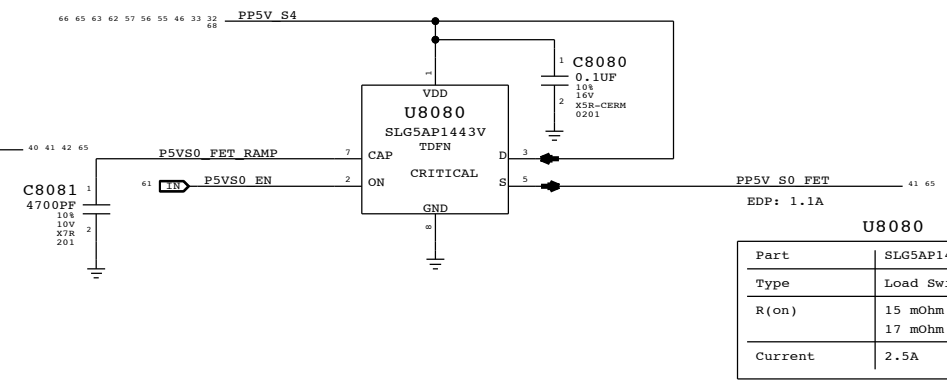
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V Sensor Switch



Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

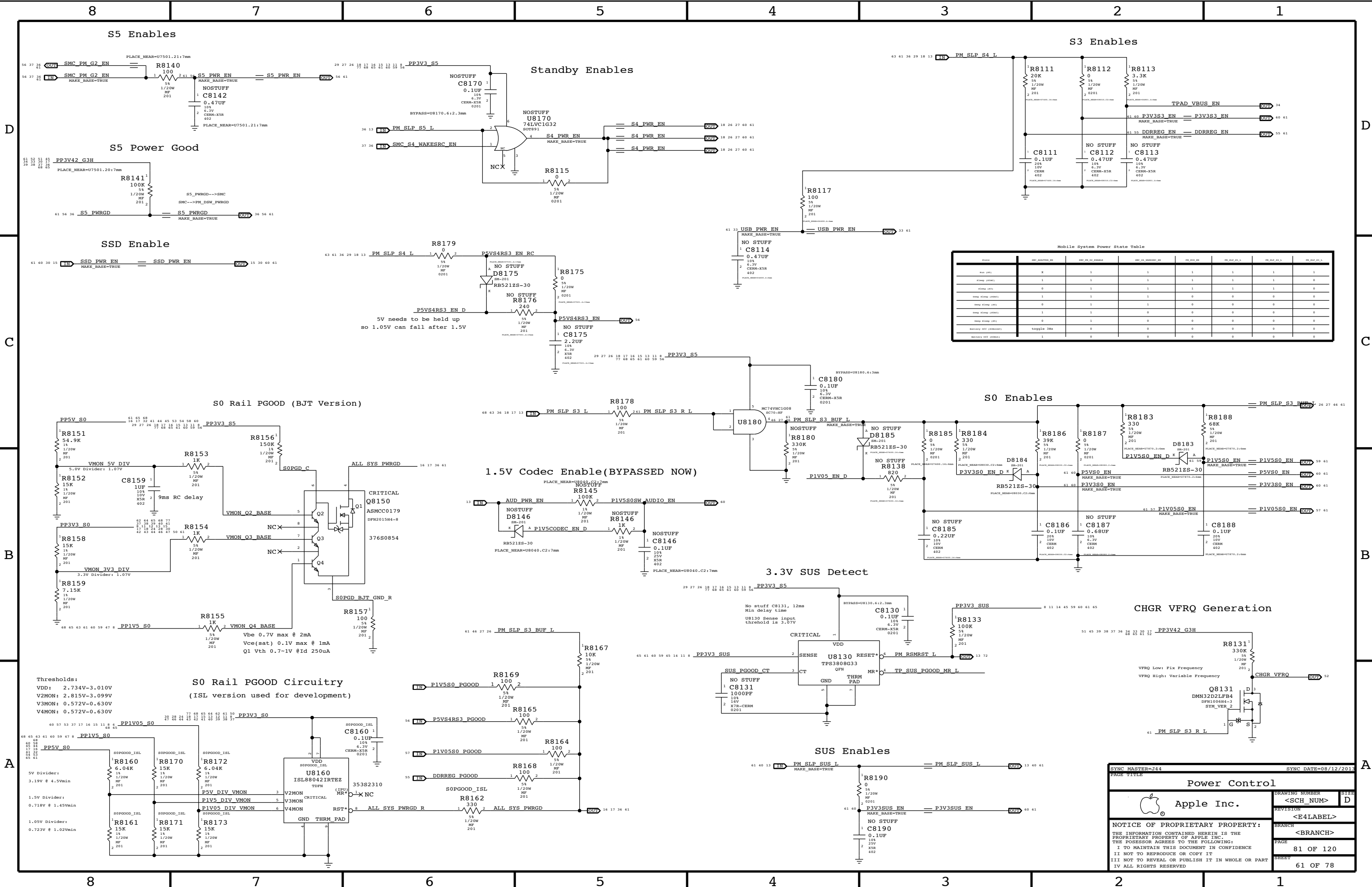
5V S0 Switch



Part	SLG5AP1443V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

SYNC MASTER=J44		SYNC DATE=08/12/2013	
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Power FETs		<SCH_NUM> D	
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Mobile System Power State Table

State	PM_SLP_S0	PM_SLP_S1	PM_SLP_S2	PM_SLP_S3	PM_SLP_S4	PM_SLP_S5
Full (ON)	X	1	1	1	1	1
Standby (S0)	1	1	1	1	1	0
Standby (S1)	0	1	1	1	1	0
Standby (S2)	0	0	1	1	1	0
Standby (S3)	0	0	0	1	1	0
Standby (S4)	0	0	0	0	1	0
Standby (S5)	0	0	0	0	0	1
Standby off (Suspend)	0	0	0	0	0	0
Standby off (Shutdown)	0	0	0	0	0	0
Standby off (Deep Sleep)	0	0	0	0	0	0

Thresholds:
 VDD: 2.734V-3.010V
 V2MON: 2.815V-3.099V
 V3MON: 0.572V-0.630V
 V4MON: 0.572V-0.630V

S0 Rail PGOOD Circuitry (ISL version used for development)

Power Control

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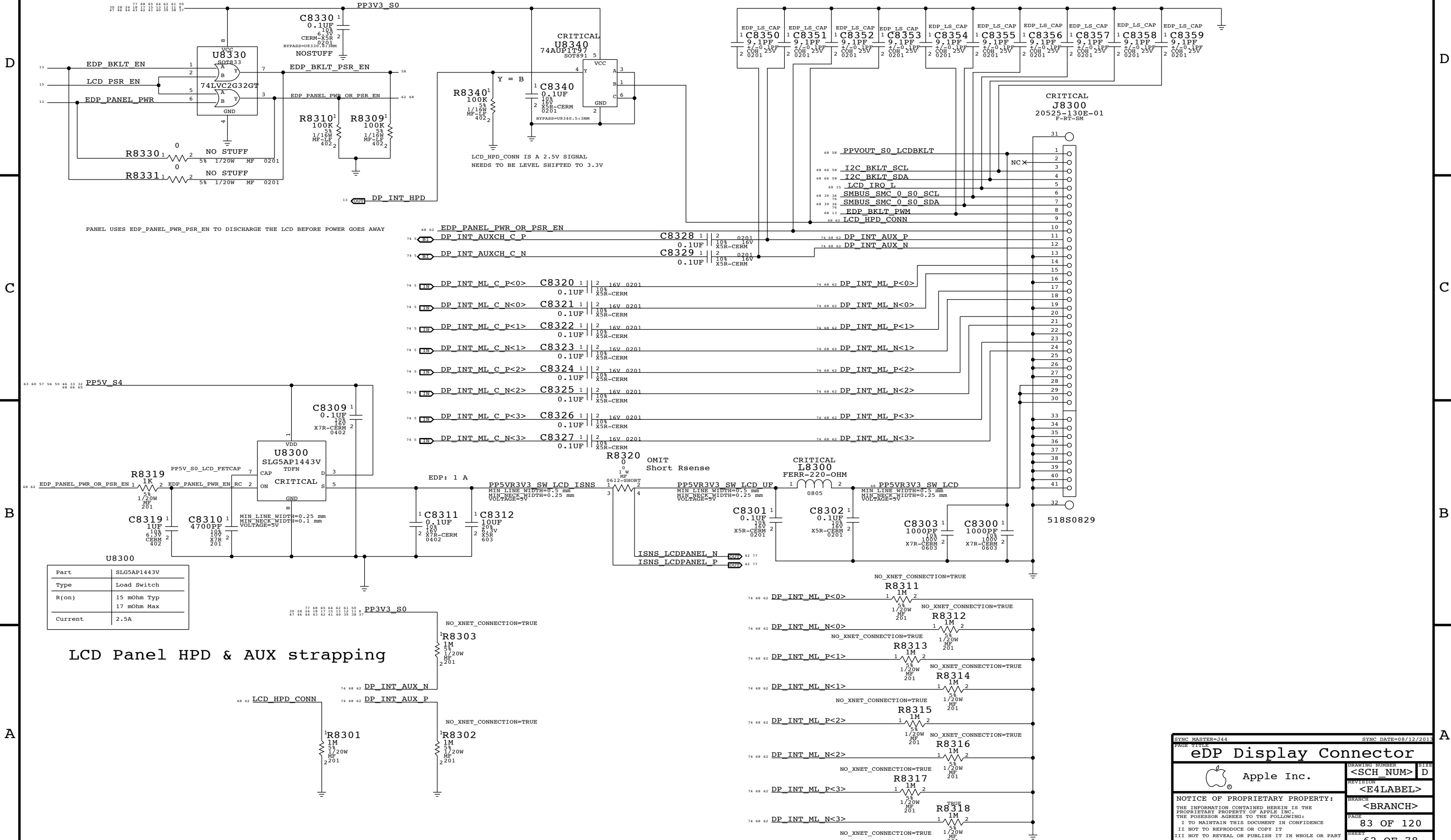
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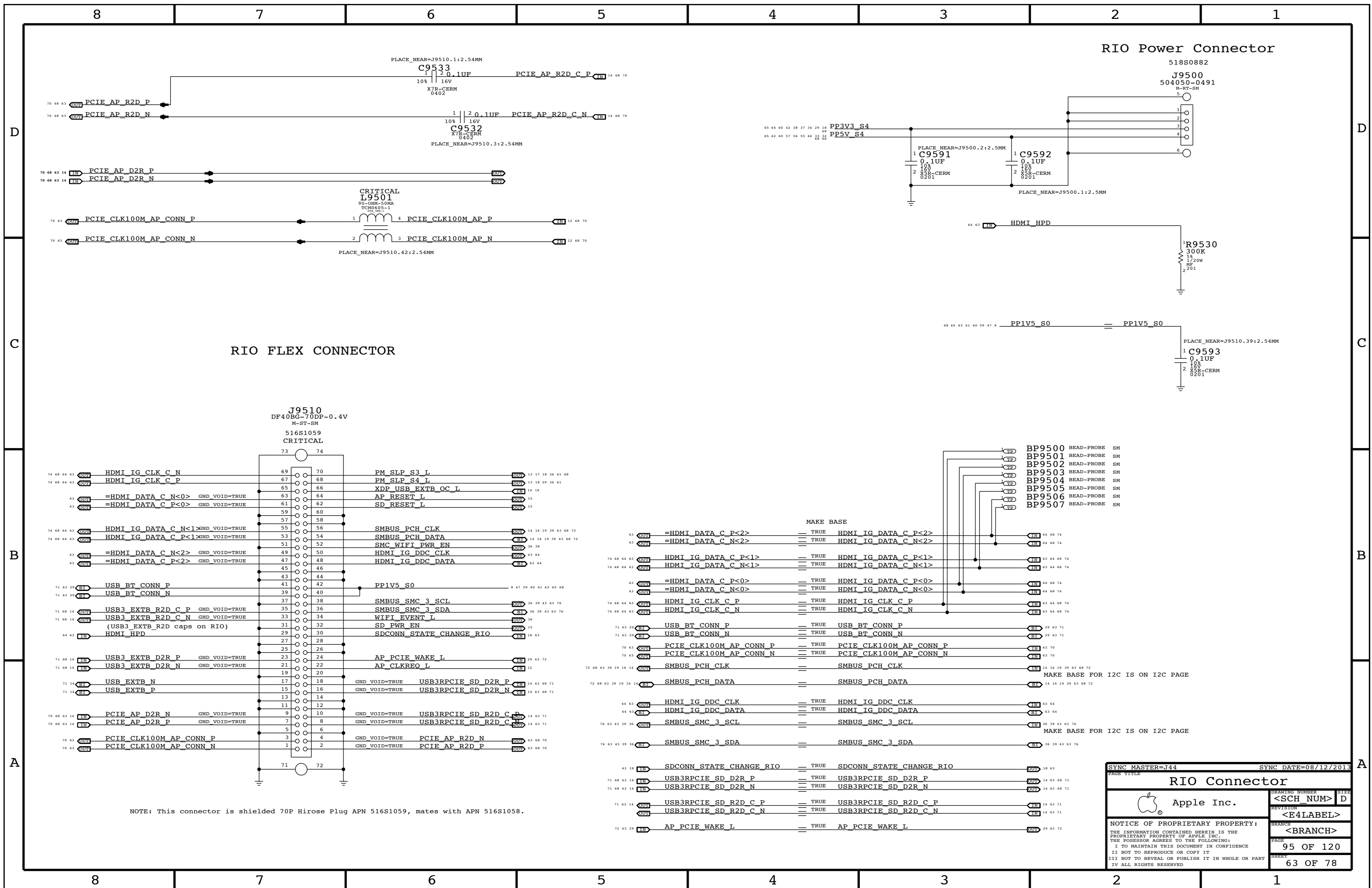
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LCD PANEL INTERFACE (eDP) NEEDS FINAL CHECK AGAINST UPDATE FOR NEW PANEL



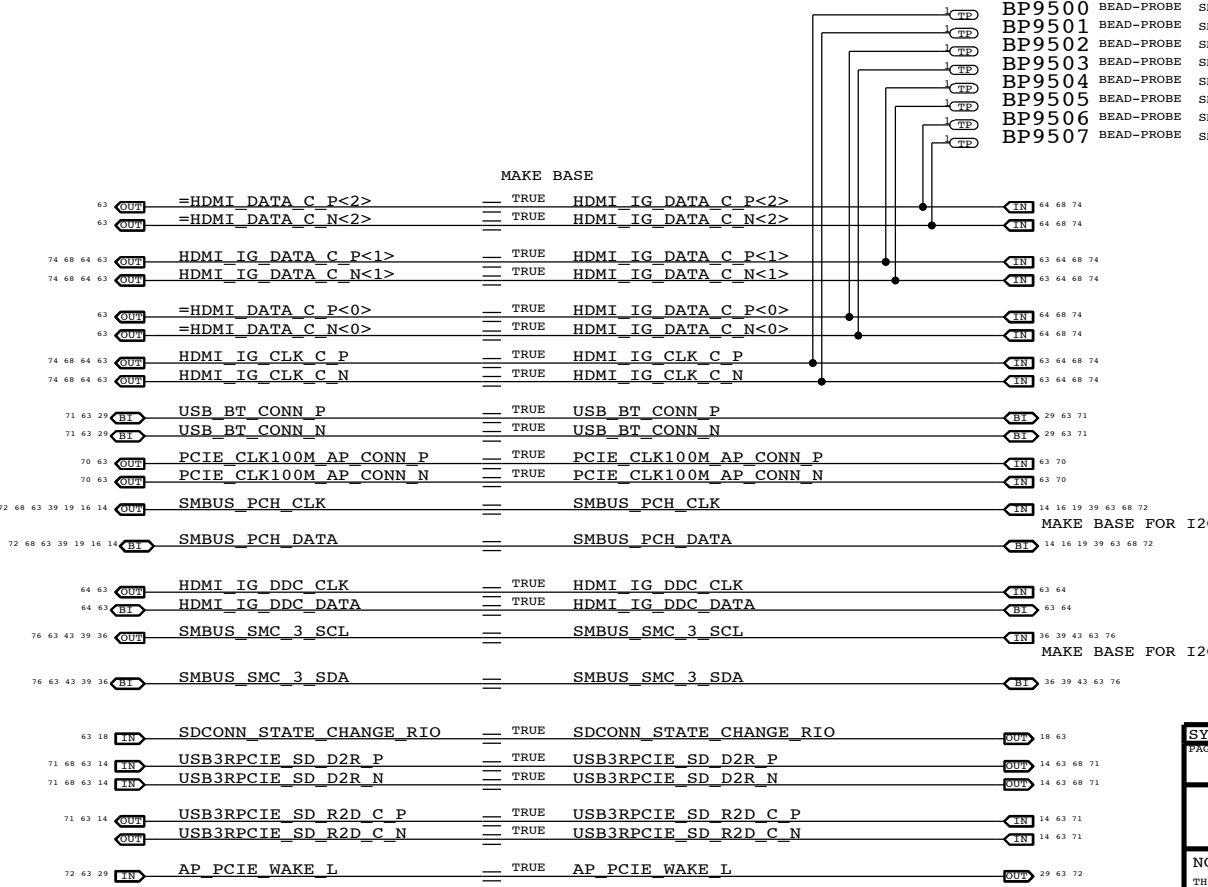
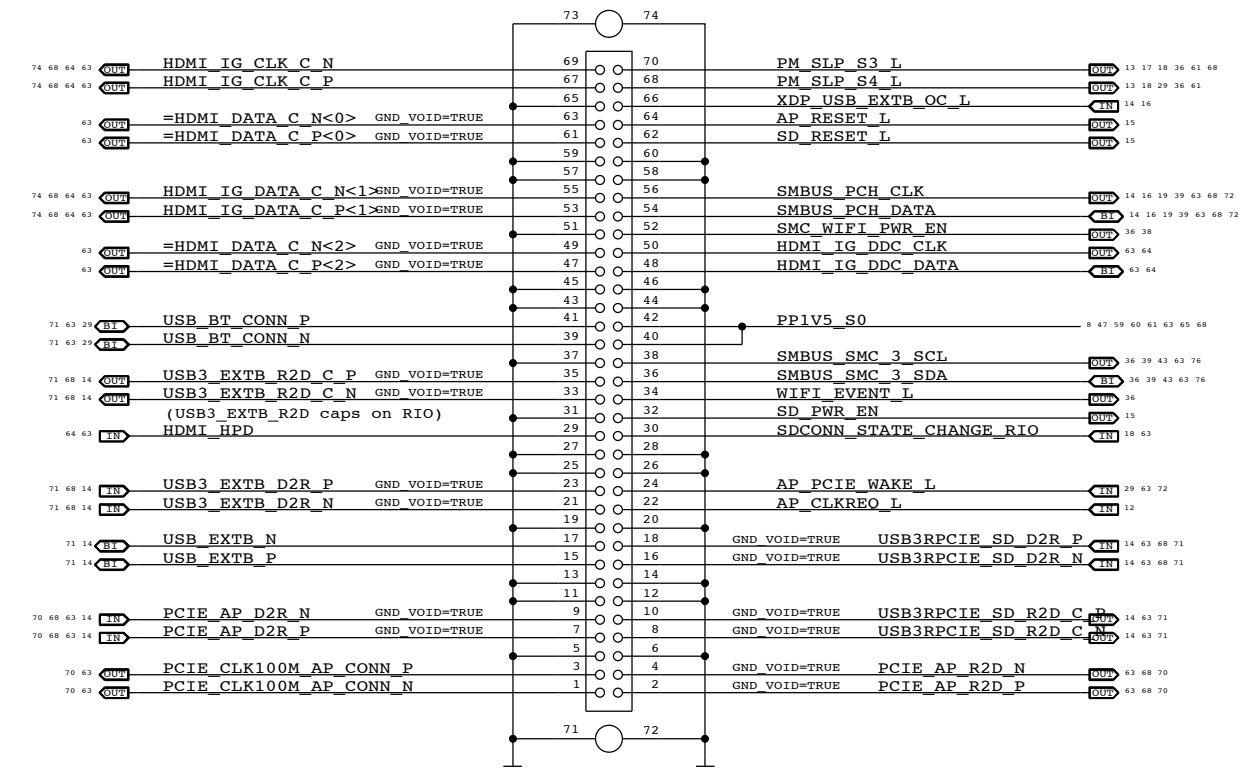
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RIO FLEX CONNECTOR

RIO Power Connector

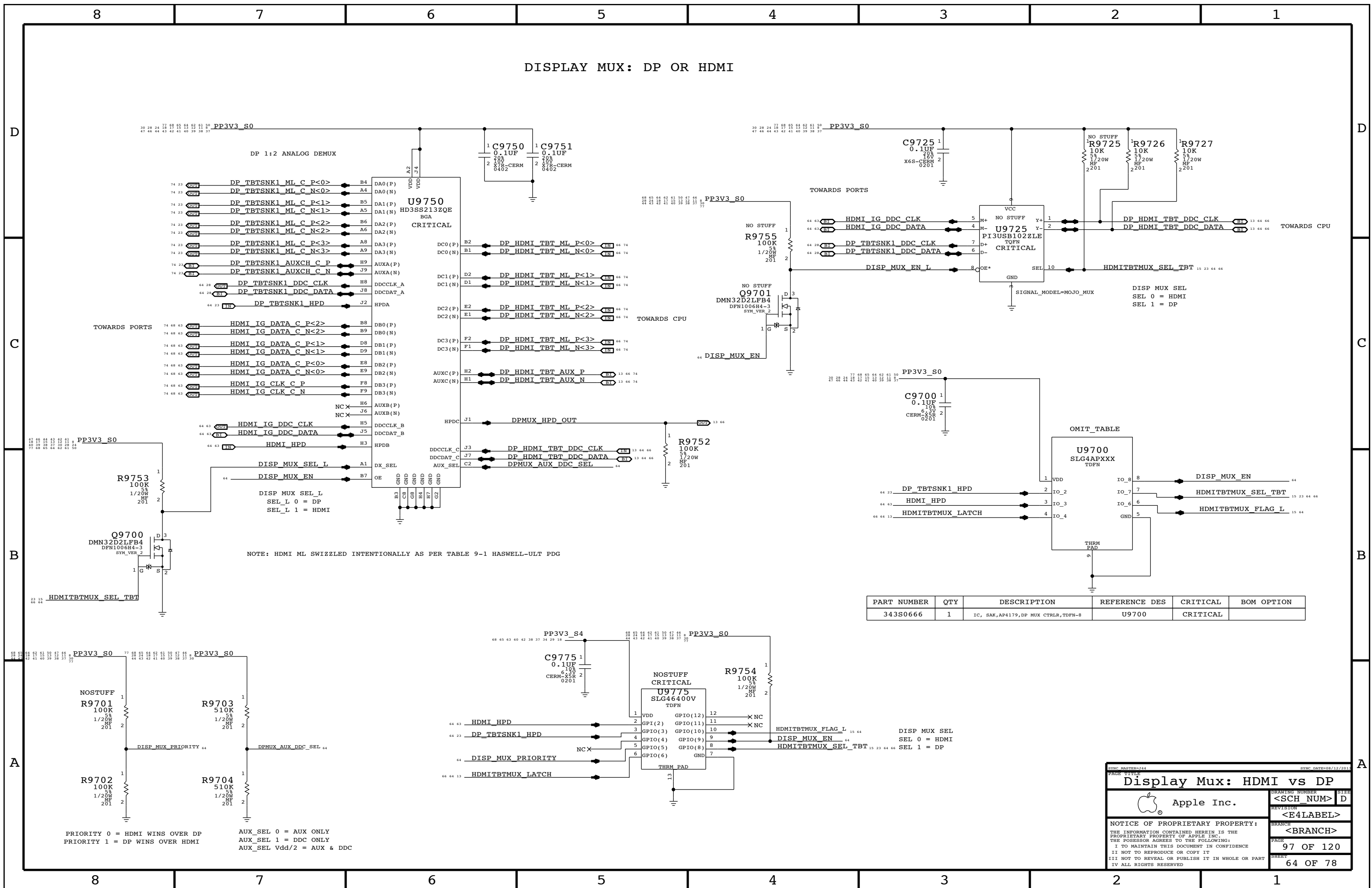
J9510
DF40BG-70DP-0.4V
M-ST-SM
516S1059
CRITICAL



NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.

SYNC MASTER=J44		SYNC DATE=08/12/2013	
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RIO Connector			
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DISPLAY MUX: DP OR HDMI



NOTE: HDMI ML SWIZZLED INTENTIONALLY AS PER TABLE 9-1 HASWELL-ULT PDG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0666	1	IC, SAK,AP4179,DP MUX CTRLR,TDFN-8	U9700	CRITICAL	

PRIORITY 0 = HDMI WINS OVER DP
 PRIORITY 1 = DP WINS OVER HDMI

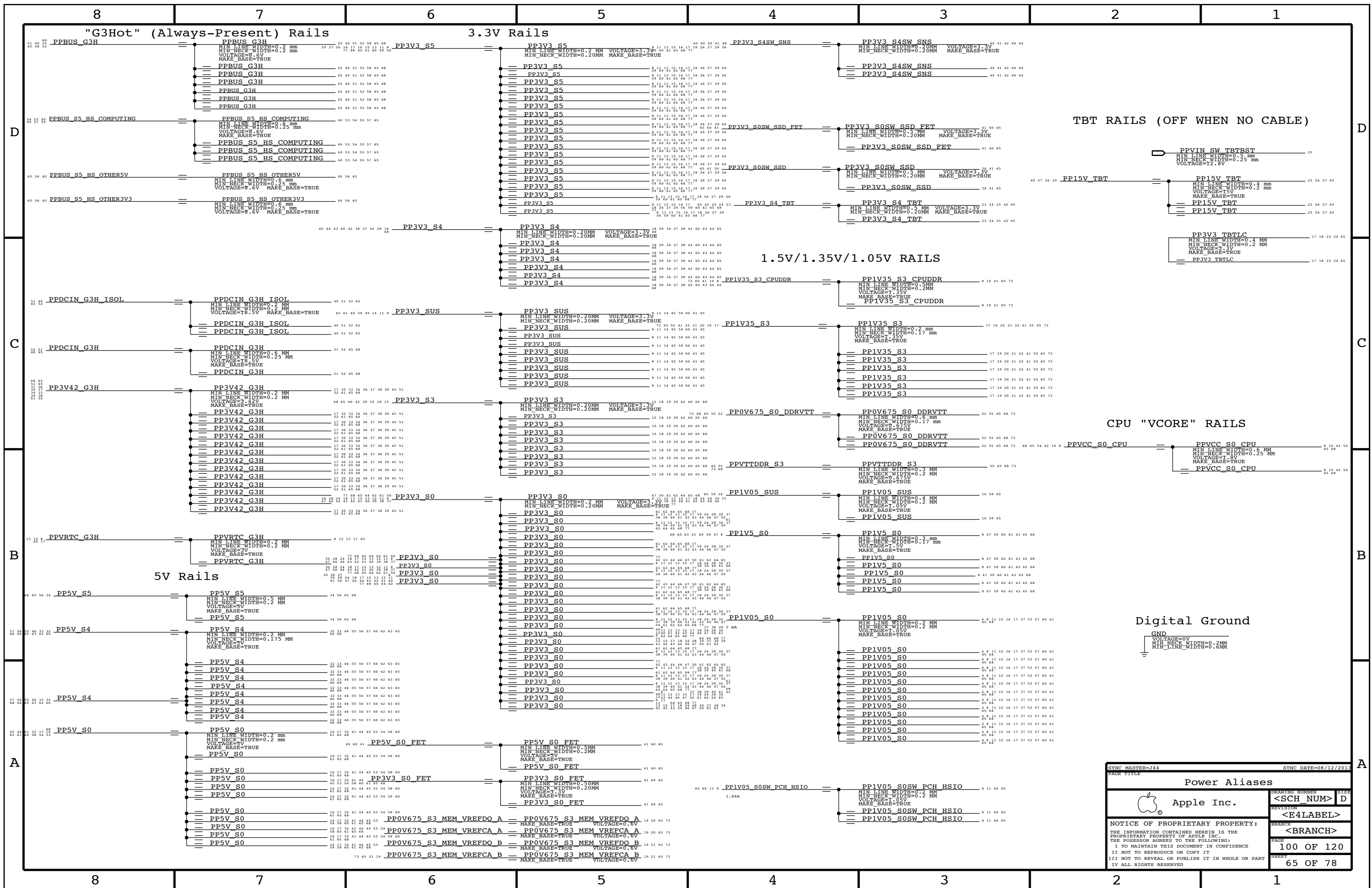
AUX_SEL 0 = AUX ONLY
 AUX_SEL 1 = DDC ONLY
 AUX_SEL Vdd/2 = AUX & DDC

Display Mux: HDMI vs DP

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TBT RAILS (OFF WHEN NO CABLE)

1.5V/1.35V/1.05V RAILS

CPU "VCORE" RAILS

Digital Ground

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Power Aliases

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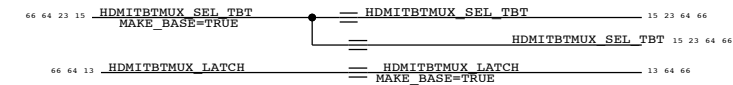
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MEMORY ADDRESS/CTRL

HDMI VS TBT

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MEM A A<1>	MEM A A<1>	20 22 73
MEM A A<2>	MEM A A<2>	20 22 73
MEM A A<3>	MEM A A<3>	20 22 73
MEM A A<4>	MEM A A<4>	20 22 73
MEM A A<5>	MEM A A<5>	20 22 73
MEM A A<6>	MEM A A<6>	7 20 22 66 73
MEM A A<7>	MEM A A<7>	20 22 73
MEM A A<8>	MEM A A<8>	20 22 73
MEM A A<9>	MEM A A<9>	20 22 73
MEM A A<10>	MEM A A<10>	20 22 73
MEM A A<11>	MEM A A<11>	20 22 73
MEM A A<12>	MEM A A<12>	20 22 73
MEM A A<13>	MEM A A<13>	20 22 73
MEM A A<14>	MEM A A<14>	20 22 73

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DP TBTSNK1 ML C P<0>	DP HDMI TBT ML P<0>	DP TBTSNK1 ML C N<0>	DP HDMI TBT ML N<0>
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DP TBTSNK1 ML C P<3>	DP HDMI TBT ML P<3>	DP TBTSNK1 ML C N<3>	DP HDMI TBT ML N<3>
DP HDMI TBT AUX P	DP HDMI TBT AUX P	DP HDMI TBT AUX N	DP HDMI TBT AUX N
DP HDMI TBT DDC CLK	DP HDMI TBT DDC CLK	DP HDMI TBT DDC DATA	DP HDMI TBT DDC DATA
DPMUX HPD_OUT	DPMUX HPD_OUT		



EPD PANEL

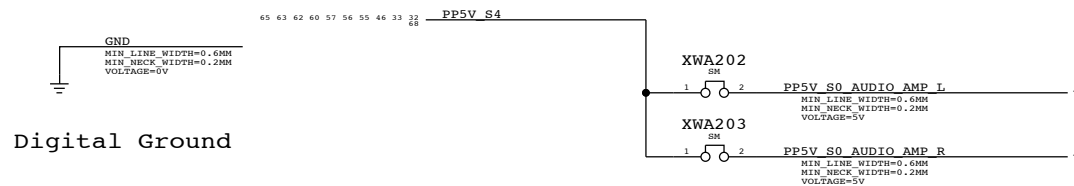
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I2C BKLT_SCL	I2C BKLT_SCL
I2C BKLT_SDA	I2C BKLT_SDA

UNUSED SIGNALS

NC_PCIE_CLK100M_FWP	NC_PCIE_CLK100M_FWN	NC_PCIE_FW_D2RP	NC_PCIE_FW_D2RN	NC_PCIE_FW_R2D_CP	NC_PCIE_FW_R2D_CN	NC_PCIE_CLK100M_ENETSDP	NC_PCIE_CLK100M_ENETSDN	NC_USB_IRP	NC_USB_IRN	NC_USB_CAMERAP	NC_USB_CAMERAN	NC_USB_SDP	NC_USB_SDN	NC_HDA_SDIN1	NC_PCI_PME_L	NC_CLINK_CLK	NC_CLINK_DATA	NC_CLINK_RESET_L
NC_PCIE_CLK100M_FWP	NC_PCIE_CLK100M_FWN	NC_PCIE_FW_D2RP	NC_PCIE_FW_D2RN	NC_PCIE_FW_R2D_CP	NC_PCIE_FW_R2D_CN	NC_PCIE_CLK100M_ENETSDP	NC_PCIE_CLK100M_ENETSDN	NC_USB_IRP	NC_USB_IRN	NC_USB_CAMERAP	NC_USB_CAMERAN	NC_USB_SDP	NC_USB_SDN	NC_HDA_SDIN1	NC_PCI_PME_L	NC_CLINK_CLK	NC_CLINK_DATA	NC_CLINK_RESET_L

UNUSED MEMORY SIGNALS

NC_MEM_A_CLKN<1>	NC_MEM_A_CLKP<1>	MEM_A_CKE<2>	NC_MEM_A_CKE<2>	MEM_A_CKE<3>	NC_MEM_A_CKE<3>	NC_MEM_B_CLKN<1>	NC_MEM_B_CLKP<1>	MEM_B_CKE<2>	NC_MEM_B_CKE<2>	MEM_B_CKE<3>	NC_MEM_B_CKE<3>
NC_MEM_A_CLKN<1>	NC_MEM_A_CLKP<1>	MEM_A_CKE<2>	NC_MEM_A_CKE<2>	MEM_A_CKE<3>	NC_MEM_A_CKE<3>	NC_MEM_B_CLKN<1>	NC_MEM_B_CLKP<1>	MEM_B_CKE<2>	NC_MEM_B_CKE<2>	MEM_B_CKE<3>	NC_MEM_B_CKE<3>



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8 7 6 5 4 3 2 1

D
C
B
A

D
C
B
A

Memory Bit/Byte Swizzle

```

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73 7 TRUE MEM A DQS P<5> ==MEM A DQS P<1> 20
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73 67 20 7 TRUE MEM A DQS N<6> ==MEM A DQS N<6> 7 20 67 73
73 7 TRUE MEM A DQS P<7> ==MEM A DQS P<0> 20
73 7 TRUE MEM A DQS N<7> ==MEM A DQS N<0> 20

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MAKE_BASE
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73 68 7 TRUE MEM B DQ<33> ==MEM B DQ<40> 21
73 68 7 TRUE MEM B DQ<34> ==MEM B DQ<45> 21
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73 7 TRUE MEM B DQS N<1> ==MEM B DQS N<3> 21
73 7 TRUE MEM B DQS P<2> ==MEM B DQS P<0> 21
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73 7 TRUE MEM B DQS P<3> ==MEM B DQS P<2> 21
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73 7 TRUE MEM B DQS N<5> ==MEM B DQS N<7> 21
73 67 21 7 TRUE MEM B DQS P<6> ==MEM B DQS P<6> 7 21 67 73
73 67 21 7 TRUE MEM B DQS N<6> ==MEM B DQS N<6> 7 21 67 73
73 7 TRUE MEM B DQS P<7> ==MEM B DQS P<6> 21
73 7 TRUE MEM B DQS N<7> ==MEM B DQS N<6> 21

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Memory Bit/Byte Swizzle

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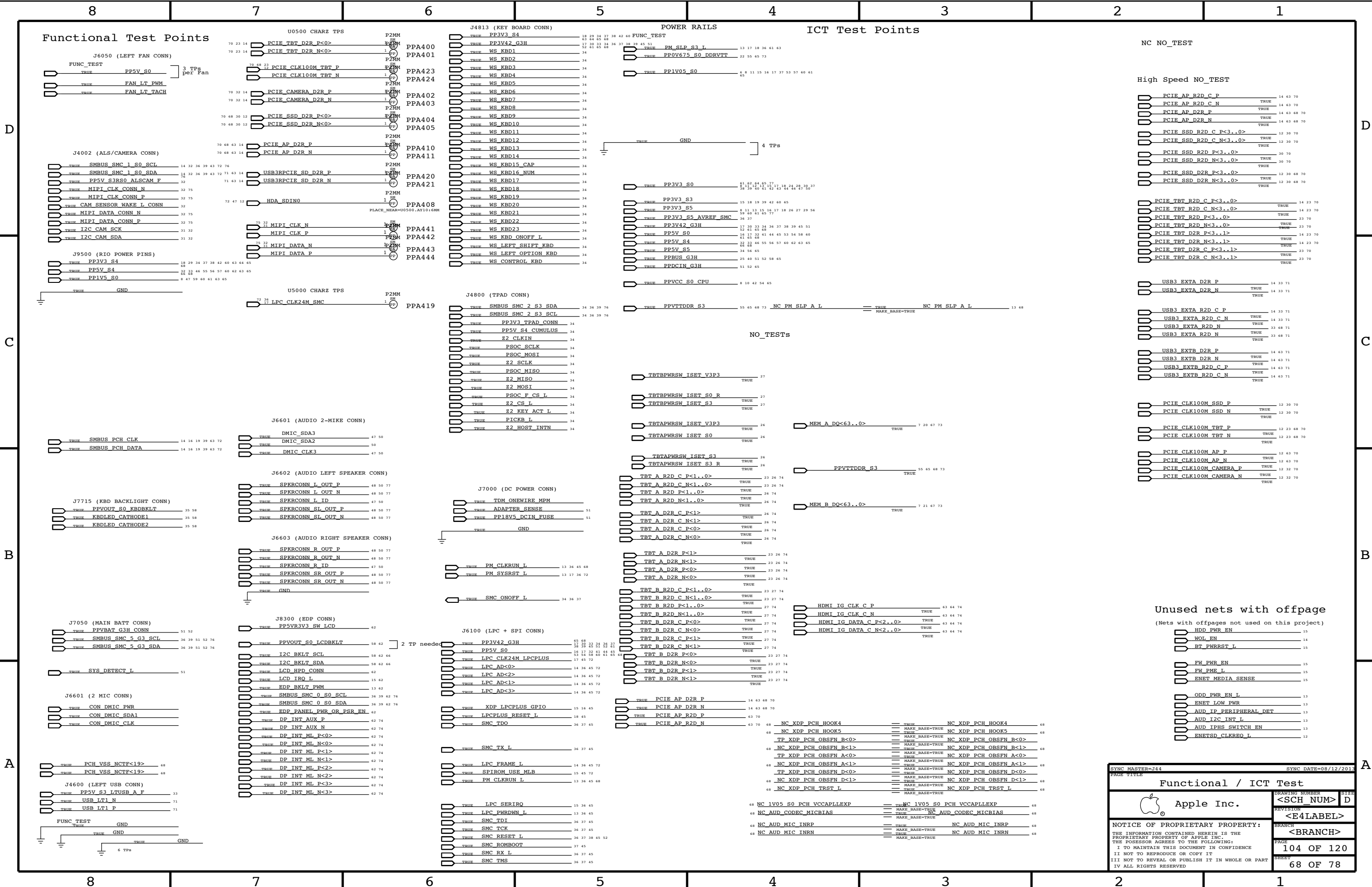
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Functional Test Points

ICT Test Points

NC NO_TEST

High Speed NO_TEST

NO_TESTS

Unused nets with offpage

(Nets with offpages not used on this project)

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J44 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, P65BGA, BGA_MEM			MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?


Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal, Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2, ISL11, ISL12, ISL13, ISL14	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
XDP_TCK0	CPU_45S	CPU_18MIL	XDP_CPU_TCK	6 16
XDP_TCK0	CPU_45S	CPU_18MIL	PCH_JTAGX	12 16
XDP_TCK1	CPU_45S	CPU_18MIL	XDP_PCH_TCK	12 16
XDP_TDO	CPU_45S	CPU_18MIL	XDP_CPU_TDO	6 16
XDP_TDO	CPU_45S	CPU_18MIL	XDP_PCH_TDO	12 16
XDP_TDI	CPU_45S	CPU_18MIL	XDP_CPU_TDI	6 16
XDP_TDI	CPU_45S	CPU_18MIL	XDP_PCH_TDI	12 16
XDP_TMS	CPU_45S	CPU_18MIL	XDP_CPU_TMS	6 16
XDP_TMS	CPU_45S	CPU_18MIL	XDP_PCH_TMS	12 16
XDP_TRST_I	CPU_45S	CPU_18MIL	XDP_TRST_L	16
XDP_TRST_I	CPU_45S	CPU_18MIL	XDP_CPUPCH_TRST_L	6 12 16
XDP_PRDY_I	CPU_45S	CPU_18MIL	XDP_CPU_PRDY_L	6 16
XDP_FREQ_I	CPU_45S	CPU_18MIL	XDP_CPU_FREQ_L	6 16
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	CPU_VCCST_PWRGD	8 16 17
CPU_VCCST_PWRGD	CPU_45S	CPU_08MIL	XDP_CPU_VCCST_PWRGD	16 17
CPU_BPM	CPU_45S	CPU_08MIL	XDP_BPM_L<1..0>	6 16
CPU_BPM_TP	CPU_45S	CPU_08MIL	XDP_BPM_L<7..2>	6 16
CPU_RCOMP_SM	CPU_27P4S	CPU_25MIL	CPU_SM_RCOMP<2..0>	6
CPU_RCOMP_FDP	CPU_27P4S	CPU_25MIL	MCP_EDP_RCOMP	6
CPU_RCOMP_OPT	CPU_27P4S	CPU_12MIL	CPU_OPT_RCOMP	6
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_L	6 36 37 53
CPU_PROCHOT	CPU_45S	CPU_08MIL	CPU_PROCHOT_R_L	6
CPU_CATERR	CPU_45S	CPU_08MIL	CPU_CATERR_L	6 36
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_L	8 53
CPU_VIDALERT	CPU_45S	CPU_18MIL	CPU_VIDALERT_R_L	8
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK	8 53
CPU_VIDSCLK	CPU_45S	CPU_18MIL	CPU_VIDSCLK_R	8
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT	8 53
CPU_VIDSOUT	CPU_45S	CPU_18MIL	CPU_VIDSOUT_R	8
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI	6 37
CPU_PECI	CPU_45S	CPU_18MIL	CPU_PECI_R	36 37
CPU_PECI_SMC	CPU_45S	CPU_18MIL	SMC_PECI_L	36 37
CPU_PECI_SMC	CPU_45S	CPU_18MIL	SMC_PECI_L_R	37
CPU_CFG	CPU_45S	CPU_18MIL	CPU_CFG<19..11>	6 16
CPU_CFG_PD	CPU_45S	CPU_18MIL	CPU_CFG<10..8>	6 16
CPU_CFG	CPU_45S	CPU_18MIL	CPU_CFG<7..5>	6 16
CPU_CFG_PD	CPU_45S	CPU_18MIL	CPU_CFG<4>	6 16
CPU_CFG_3	CPU_45S	CPU_18MIL	CPU_CFG<3>	6 16
CPU_CFG	CPU_45S	CPU_18MIL	CPU_CFG<2>	6 16
CPU_CFG_PD	CPU_45S	CPU_18MIL	CPU_CFG<1..0>	6 16
CPU_MEM_RESET	CPU_45S	CPU_08MIL	MEM_RESET_L	20 21 22
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 53
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 53

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<3..1>	12 30 68
PCIE_SSD_D2R	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<3..1>	12 30 68
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_P<0>	12 30 68
PCIE_SSD_D2R_PP	PCIE_85D	PCIE_RX	PCIE_SSD_D2R_N<0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_P<3..0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_C_N<3..0>	12 30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_P<3..0>	30 68
PCIE_SSD_R2D	PCIE_85D	PCIE_TX	PCIE_SSD_R2D_N<3..0>	30 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<0>	14 23 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<0>	14 23 68
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<0>	23
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<0>	23
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_P<3..1>	14 23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_N<3..1>	14 23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_P<3..1>	23 68
PCIE_TBT_D2R	PCIE_85D	PCIE_RX	PCIE_TBT_D2R_C_N<3..1>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_P<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_P<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_N<3..0>	23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_P<3..0>	14 23 68
PCIE_TBT_R2D	PCIE_85D	PCIE_TX	PCIE_TBT_R2D_C_N<3..0>	14 23 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_P	63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_N	63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_P	14 63 68
PCIE_AP_R2D	PCIE_85D	PCIE_TX	PCIE_AP_R2D_C_N	14 63 68
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_P	14 63 68
PCIE_AP_D2R	PCIE_85D	PCIE_RX	PCIE_AP_D2R_N	14 63 68
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	63
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	63
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	12 63 68
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	12 63 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32 68
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 68
PCIE_CLK100M_SSD	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 68
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 23 68
PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 23 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_P	14 32 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_N	14 32 68
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_C_P	31 32
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_N	31 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_C_P	14 32
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX	PCIE_CAMERA_R2D_C_N	14 32

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CPU & PCIe Constraints

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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIA	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIA	*	=6X_DIELECTRIC	?	USB_RBIA	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?	SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
USB_BT	USB_85D	USB	USB_BT_P	14 29
USB_BT	USB_85D	USB	USB_BT_N	14 29
USB_BT	USB_85D	USB	USB_BT_CONN_P	29 63
USB_BT	USB_85D	USB	USB_BT_CONN_N	29 63
USB_EXT_A	USB_85D	USB	USB_EXT_A_P	14 33
USB_EXT_A	USB_85D	USB	USB_EXT_A_N	14 33
DEFAULT	DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L	33 36 37
DEFAULT	DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L	33 36 37
USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_P	33
USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_N	33
USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_F_P	33
USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_F_N	33
USB_EXT_A	USB_85D	USB	USB_LT1_P	68
USB_EXT_A	USB_85D	USB	USB_LT1_N	68
USB_EXT_B	USB_85D	USB	USB_EXT_B_P	14 63
USB_EXT_B	USB_85D	USB	USB_EXT_B_N	14 63
USB_TPAD	USB_85D	USB	USB_TPAD_P	14 34
USB_TPAD	USB_85D	USB	USB_TPAD_N	14 34
USB_TPAD	USB_85D	USB	USB_TPAD_R_P	34
USB_TPAD	USB_85D	USB	USB_TPAD_R_N	34
USB3_EXT_A_D2R	USB_85D	USB3_RX	USB3_EXT_A_D2R_P	14 33 68
USB3_EXT_A_D2R	USB_85D	USB3_RX	USB3_EXT_A_D2R_N	14 33 68
USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_P	33
USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_N	33 68
USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_C_P	14 33 68
USB3_EXT_A_R2D	USB_85D	USB3_TX	USB3_EXT_A_R2D_C_N	14 33 68
USB3_EXT_B_D2R	USB_85D	USB3_RX	USB3_EXT_B_D2R_P	14 63 68
USB3_EXT_B_D2R	USB_85D	USB3_RX	USB3_EXT_B_D2R_N	14 63 68
USB3_EXT_B_R2D	USB_85D	USB3_TX	USB3_EXT_B_R2D_C_P	14 63 68
USB3_EXT_B_R2D	USB_85D	USB3_TX	USB3_EXT_B_R2D_C_N	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_P	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_N	14 63 68
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_P	14 63
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_N	14 63
USB_NC	USB_85D	USB	NC_USB_IRP	14 66
USB_NC	USB_85D	USB	NC_USB_IRN	14 66
USB_NC	USB_85D	USB	TP_USB_5P	14
USB_NC	USB_85D	USB	TP_USB_5N	14
USB_NC	USB_85D	USB	NC_USB_SDP	14 66
USB_NC	USB_85D	USB	NC_USB_SDN	14 66
USB_NC	USB_85D	USB	NC_USB_CAMERAP	14 66
USB_NC	USB_85D	USB	NC_USB_CAMERAN	14 66
PCH_USB_RBIA	PCH_USB_RBIA	USB_RBIA	PCH_USB_RBIA	14
SATA_85D	SATA_85D	SATA_RX	DUMMY_SATA_D2R_P	
SATA_85D	SATA_85D	SATA_RX	DUMMY_SATA_D2R_N	
SATA_85D	SATA_85D	SATA_TX	DUMMY_SATA_R2D_P	
SATA_85D	SATA_85D	SATA_TX	DUMMY_SATA_R2D_N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 23
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	23

Notes:
This is here to keep the SATA rules.

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PAGE TITLE: USB Constraints

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 36 45 68
LPC_AD	LPC_45S	LPC	LPC_FRAME_L	14 36 45 68
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 36 68
LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	17 45 68
LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	12 17
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	14 16 19 39 63 68
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	14 16 19 39 63 68
SML_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	14 39
SML_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	14 39
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 32 36 39 43 68 76
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 32 36 39 43 68 76
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 47
HDA_BIT_CLK_R	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 47
HDA_SYNC_R	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST	HDA_45S	HDA	HDA_RST_R_L	12
HDA_RST	HDA_45S	HDA	HDA_RST_L	12 47
HDA_SDIN	HDA_45S	HDA	HDA_SDIN0	12 47 68
HDA_SDIN	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	12 47
HDA_SDOIT	HDA_45S	HDA	HDA_SDOIT	12 47
HDA_SDOIT	HDA_45S	HDA	HDA_SDOIT_R	12 17
SPT_MLB	SPT_45S	SPT	SPI_ALT_CLK	45
SPT_MLB	SPT_45S	SPT	SPI_CLK	45
SPT_MLB	SPT_45S	SPT	SPI_CLK_R	14 45
SPT_MLB	SPT_45S	SPT	SPI_MLB_CLK	45
SPT_MLB	SPT_45S	SPT	SPI_SMC_CLK	36 45
SPT_MLB	SPT_45S	SPT	SPI_ALT_CS_L	45
SPT_MLB	SPT_45S	SPT	SPI_CS0_L	45
SPT_MLB	SPT_45S	SPT	SPI_CS0_R_L	14 45
SPT_MLB	SPT_45S	SPT	SPI_MLB_CS_L	45
SPT_MLB	SPT_45S	SPT	SPI_SMC_CS_L	36 45
SPT_MLB	SPT_45S	SPT	SPI_ALT_MISO	45
SPT_MLB	SPT_45S	SPT	SPI_MISO	14 45
SPT_MLB	SPT_45S	SPT	SPI_MISO_R	45
SPT_MLB	SPT_45S	SPT	SPI_MLB_MISO	45
SPT_MLB	SPT_45S	SPT	SPI_SMC_MISO	36 45
SPT_MLB	SPT_45S	SPT	SPI_ALT_MOSI	45
SPT_MLB	SPT_45S	SPT	SPI_MOSI	45
SPT_MLB	SPT_45S	SPT	SPI_MOSI_R	14 45
SPT_MLB	SPT_45S	SPT	SPI_MLB_MOSI	45
SPT_MLB	SPT_45S	SPT	SPI_SMC_MOSI	36 45
SPT_MLB_IO2	SPT_45S	SPT	SPI_IO<2>	14 45
SPT_MLB_IO2	SPT_45S	SPT	SPIROM_WP_L	45
SPT_MLB_IO3	SPT_45S	SPT	SPI_IO<3>	14 45
SPT_MLB_IO3	SPT_45S	SPT	SPIROM_HOLD_L	45
SPT_MLB_IO3	SPT_45S	SPT	SPIROM_USE_MLB	15 45 68
PCH_RTCX	PCH_45S	PCH_15MTL	PCH_CLK32K_RTCX1	12 17
PCH_SRTCST	PCH_45S	PCH_15MTL	PCH_SRTCST_L	12
PCH_RTCRST	PCH_45S	PCH_15MTL	RTC_RESET_L	12
PCH_THRMTRIP	PCH_45S	PCH_18MTL	PM_THRMTRIP_L	15 37
PCH_THRMTRIP	PCH_45S	PCH_18MTL	PM_THRMTRIP_R_L	37
	PCH_45S	PCH_15MTL	PCH_INTRUDER_L	12
	PCH_45S	PCH_15MTL	PCH_INTVRMEN	12
	PCH_45S	PCH_15MTL	PCH_DSWVRMEN	13
	PCH_45S	PCH_15MTL	PM_RSMRST_L	13 61
	PCH_45S	PCH_15MTL	PM_SYSRST_L	13 17 36 68
	PCH_45S	PCH_15MTL	XDP_DBRESET_L	16 17
	PCH_45S	PCH_15MTL	PM_PCH_SYS_PWROK	13 16 17 36
	PCH_45S	PCH_15MTL	XDP_SYS_PWROK	16
	PCH_45S	PCH_15MTL	SYS_PWROK_R	17
	PCH_45S	PCH_15MTL	PM_PCH_PWROK	13 17
	PCH_45S	PCH_15MTL	PM_S0_PGOOD	17
	PCH_45S	PCH_15MTL	SMC_DELAYED_PWRGD	17 24 25 36 37
	PCH_45S	PCH_15MTL	PM_DSW_PWRGD	13 36
	PCH_45S	PCH_15MTL	PM_PWRBTN_L	13 16 36
	PCH_45S	PCH_15MTL	XDP_CPU_PWRBTN_L	16
	PCH_45S	PCH_15MTL	PCIE_WAKE_L	13 29 31
	PCH_45S	PCH_15MTL	AP_PCIE_WAKE_L	29 63
	PCH_45S	PCH_15MTL	CAM_PCIE_WAKE_L	31
	PCH_45S	PCH_15MTL	TBT_CIO_PLUGIN_EVENT_L	15 18 23
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALIN	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT	12 17
PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT_R	17
PCH_RCOMP_PCIE	PCH_27P4S	PCH_12MTL	PCH_PCIE_RCOMP	14
PCH_RCOMP_OPT	PCH_27P4S	PCH_12MTL	PCH_OPT_COMP	15
PCH_RCOMP_SATA	PCH_27P4S	PCH_12MTL	PCH_SATA_RCOMP	12

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTL	*	=2x_DIELECTRIC	?
MEM_CTL2CTL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_BM	*	=2x_DIELECTRIC	?
MEM_CMD2CTL_BM	*	=2x_DIELECTRIC	?
MEM_CTL2CTL_BM	*	=2x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_BM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_BM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_BM

Haswell ULT Memory Down DDR3L 1x8 Length Matching

DDR3 Signal Group	Unit	Min Length	Max Length
CTLmax - CTLmin	mils	0	100
CTL to CLK	mils	CLK - 500	CLK + 500
CMDi to CMDj	mils	CMDj - 100	CMDj + 100
CMD to CLK	mils	CLK - 500	CLK + 500
(DQmax - DQmin) per byte	mils	0	250
(DQS - DQmax) per byte	mils	-100	150
DQS to DQS#	mils	-5	5
DQS to CLK (Rule 1)	mils	CLK - 6500	CLK + 500
Max(CLK-DQS) - Min(CLK-DQS)	mils	0	5500
CLK to CLK#	mils	-5	5

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	7 20 22
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CKE<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CS_L<0>	7 20 22
MEM_A_ODT0	MEM_40S	MEM_CTL	MEM_A_ODT<0>	20 22
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	7 20 22 66
MEM_A_DQBYTE0	MEM_45S	MEM_A_DQBYTE_0	MEM_A_DQ<7..0>	7 67 68
MEM_A_DQBYTE1	MEM_45S	MEM_A_DQBYTE_1	MEM_A_DQ<15..8>	7 67 68
MEM_A_DQBYTE2	MEM_45S	MEM_A_DQBYTE_2	MEM_A_DQ<23..16>	7 67 68
MEM_A_DQBYTE3	MEM_45S	MEM_A_DQBYTE_3	MEM_A_DQ<31..24>	7 67 68
MEM_A_DQBYTE4	MEM_45S	MEM_A_DQBYTE_4	MEM_A_DQ<39..32>	7 20 67 68
MEM_A_DQBYTE5	MEM_45S	MEM_A_DQBYTE_5	MEM_A_DQ<47..40>	7 67 68
MEM_A_DQBYTE6	MEM_45S	MEM_A_DQBYTE_6	MEM_A_DQ<55..48>	7 67 68
MEM_A_DQBYTE7	MEM_45S	MEM_A_DQBYTE_7	MEM_A_DQ<63..56>	7 67 68
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 67
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 67
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 67
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 67
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 67
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 67
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 67
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 67
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 67
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 67
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 67
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 67
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 20 67
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 20 67
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 67
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 67
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	7 21 22
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CKE<0>	7 21 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CS_L<0>	7 21 22
MEM_B_ODT0	MEM_40S	MEM_CTL	MEM_B_ODT<0>	21 22
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	7 21 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	7 21 22 66
MEM_B_DQBYTE0	MEM_45S	MEM_B_DQBYTE_0	MEM_B_DQ<7..0>	7 67 68
MEM_B_DQBYTE1	MEM_45S	MEM_B_DQBYTE_1	MEM_B_DQ<15..8>	7 67 68
MEM_B_DQBYTE2	MEM_45S	MEM_B_DQBYTE_2	MEM_B_DQ<23..16>	7 67 68
MEM_B_DQBYTE3	MEM_45S	MEM_B_DQBYTE_3	MEM_B_DQ<31..24>	7 67 68
MEM_B_DQBYTE4	MEM_45S	MEM_B_DQBYTE_4	MEM_B_DQ<39..32>	7 21 67 68
MEM_B_DQBYTE5	MEM_45S	MEM_B_DQBYTE_5	MEM_B_DQ<47..40>	7 67 68
MEM_B_DQBYTE6	MEM_45S	MEM_B_DQBYTE_6	MEM_B_DQ<55..48>	7 67 68
MEM_B_DQBYTE7	MEM_45S	MEM_B_DQBYTE_7	MEM_B_DQ<63..56>	7 67 68
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 67
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 67
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 67
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 67
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 67
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 67
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 67
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 67
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 67
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 67
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 67
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 67
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 21 67
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 21 67
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 67
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 67
MEM_PWR			PP1V35_S3	17 19 20 21 22 41 55 65
MEM_PWR			PP1V35_S3_CPUDDR	8 10 41 65
MEM_PWR			PP0V675_S0_DDRVTT	22 55 65 68
MEM_PWR			PPVTDDR_S3	55 65 68
MEM_12MIL			CPU_DIMMA_VREFDQ	7 19
MEM_12MIL			CPU_DIMMA_VREFDQ_A_ISOL	19
MEM_12MIL			CPU_DIMMB_VREFDQ	7 19
MEM_12MIL			CPU_DIMMB_VREFDQ_B_ISOL	19
MEM_12MIL			CPU_DIMM_VREFCA	7 19
MEM_12MIL			CPU_DIMM_VREFCA_A_ISOL	19
MEM_12MIL			CPU_DIMM_VREFCA_B_ISOL	19
MEM_12MIL			PP0V675_S3_MEM_VREFDQ_A	19 20 65
MEM_12MIL			PP0V675_S3_MEM_VREFDQ_B	19 21 65
MEM_12MIL			PP0V675_S3_MEM_VREFCA_A	19 20 65
MEM_12MIL			PP0V675_S3_MEM_VREFCA_B	19 21 65

SYNC MASTER=144 SYNC DATE=01/03/2013

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Memory Constraints

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Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3x_DIELECTRIC	?
TBTDP_TXRX	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
 DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
 SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
 MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

ELECTRICAL CONST SET	PHYSICAL	NET TYPE	SPACING
	DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N
	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK
	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI
	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO
	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L
	DP_85D	DISPLAYPORT	DP HDMI TBT ML P<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT ML N<3..0>
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX P
	DP_85D	DISPLAYPORT	DP HDMI TBT AUX N
	HDMI_85D	HDMI_CLK	HDMI IG CLK C P
	HDMI_85D	HDMI_CLK	HDMI IG CLK C N
	HDMI_85D	HDMI_DATA	HDMI IG DATA C P<2..0>
	HDMI_85D	HDMI_DATA	HDMI IG DATA C N<2..0>

Only used on hosts supporting Thunderbolt video-in

Thunderbolt, DP, HDMI Net Properties

ELECTRICAL CONST SET	PHYSICAL	NET TYPE	SPACING
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A R2D C P<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A R2D C N<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A R2D P<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_TX	TBT_A R2D N<1..0>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML N<1>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A D2R C P<0>
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A D2R C N<0>
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A D2R P<0>
TBT_A_D2R_0	TBTDP_85D	TBTDP_RX	TBT_A D2R N<0>
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A D2R C P<1>
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A D2R C N<1>
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A D2R P<1>
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A D2R N<1>
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A D2R1 AUXDDC P
TBT_A_D2R_1	TBTDP_85D	TBTDP_RX	TBT_A D2R1 AUXDDC N
DP_TBTPA_AUXCH	DP_85D		DP TBTPA AUXCH C P
DP_TBTPA_AUXCH	DP_85D		DP TBTPA AUXCH C N
DP_TBTPA_AUXCH	DP_85D		DP TBTPA AUXCH P
DP_TBTPA_AUXCH	DP_85D		DP TBTPA AUXCH N
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B R2D C P<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B R2D C N<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B R2D P<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_TX	TBT_B R2D N<1..0>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML N<1>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<3>
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B D2R C P<0>
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B D2R C N<0>
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B D2R P<0>
TBT_B_D2R_0	TBTDP_85D	TBTDP_RX	TBT_B D2R N<0>
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B D2R C P<1>
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B D2R C N<1>
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B D2R P<1>
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B D2R N<1>
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B D2R1 AUXDDC P
TBT_B_D2R_1	TBTDP_85D	TBTDP_RX	TBT_B D2R1 AUXDDC N
DP_TBTPB_AUXCH	DP_85D		DP TBTPB AUXCH C P
DP_TBTPB_AUXCH	DP_85D		DP TBTPB AUXCH C N
DP_TBTPB_AUXCH	DP_85D		DP TBTPB AUXCH P
DP_TBTPB_AUXCH	DP_85D		DP TBTPB AUXCH N
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH C P
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH C N
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH P
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH N
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH C P
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH C N
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH P
DP_TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH N
DP_INT_ML	DP_85D	DISPLAYPORT	DP INT ML C P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP INT ML C N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP INT ML P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP INT ML N<3..0>
DP_INT_AUXCH	DP_85D		DP INT AUXCH C P
DP_INT_AUXCH	DP_85D		DP INT AUXCH C N
DP_INT_AUXCH	DP_85D		DP INT AUXCH P
DP_INT_AUXCH	DP_85D		DP INT AUXCH N

Notes:
 AUX and DDC was removed from DISPLAYPORT or TBTDP_RX/TX because it's not high speed, and to save routing space.

Only used on dual-port hosts.

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TBT,DP,HDMI Constraints
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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?	MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?	MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?	MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2X_DIELECTRIC	?	S2_DATA2SELF	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2X_DIELECTRIC	?	S2_DQS2OWNDATA	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CMD	*	=2X_DIELECTRIC	?	S2_CMD2CMD	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CTRL	*	=2X_DIELECTRIC	?	S2_CMD2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CTRL2CTRL	*	=2X_DIELECTRIC	?	S2_CTRL2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_2OTHERMEM	*	=4X_DIELECTRIC	?	S2_2OTHERMEM	TOP,BOTTOM	=6X_DIELECTRIC	?
S2MEM_2PWR	*	=2X_DIELECTRIC	?	S2MEM_2PWR	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2GND	*	=2X_DIELECTRIC	?	S2MEM_2GND	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2OTHER	*	=6X_DIELECTRIC	?	S2MEM_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 31 32
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 31 32
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DOS_P<0> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DOS_N<0> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DOS_P<1> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DOS_N<1> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DO<7..0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DO<15..8> 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 32 68
		S2_MEM_PWR	PP1V35_CAM 31 32
		S2_MEM_PWR	PP0V675_CAM_VREF 31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFPO 32

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SMC SMBus & Charger Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	34 36 39 68
SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	34 36 39 68
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 32 36 39 43 68 72
SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 32 36 39 43 68 72
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	36 39 62 68
SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	36 39 62 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	36 39 51 52 68
SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	36 39 51 52 68
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	36 39 43 63
SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	36 39 43 63

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.070 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
MEM_40S	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
MEM_72D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
MEM_85D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
PCIE_85D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.090 MM	10 MM	OVERVERRIDE	OVERVERRIDE
USB_85D	TOP	OVERVERRIDE	OVERVERRIDE	0.100 MM	500 MIL	OVERVERRIDE	OVERVERRIDE
CPU_27P4S	BOTTOM	OVERVERRIDE	OVERVERRIDE	0.230 MM	100 MIL	OVERVERRIDE	OVERVERRIDE
USB3_85D	TOP	OVERVERRIDE	OVERVERRIDE	0.100 MM	500 MIL	OVERVERRIDE	OVERVERRIDE
USB3_85D	ISL10	OVERVERRIDE	OVERVERRIDE	0.075 MM			0.090 MM
DP_85D	ISL9	OVERVERRIDE	OVERVERRIDE	0.075 MM			0.090 MM
PCIE_85D	ISL10	OVERVERRIDE	OVERVERRIDE	0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_MEM	MEM_45S
MEM_72D	BGA_MEM	MEM_85D

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.100 MM	6.35 MM		

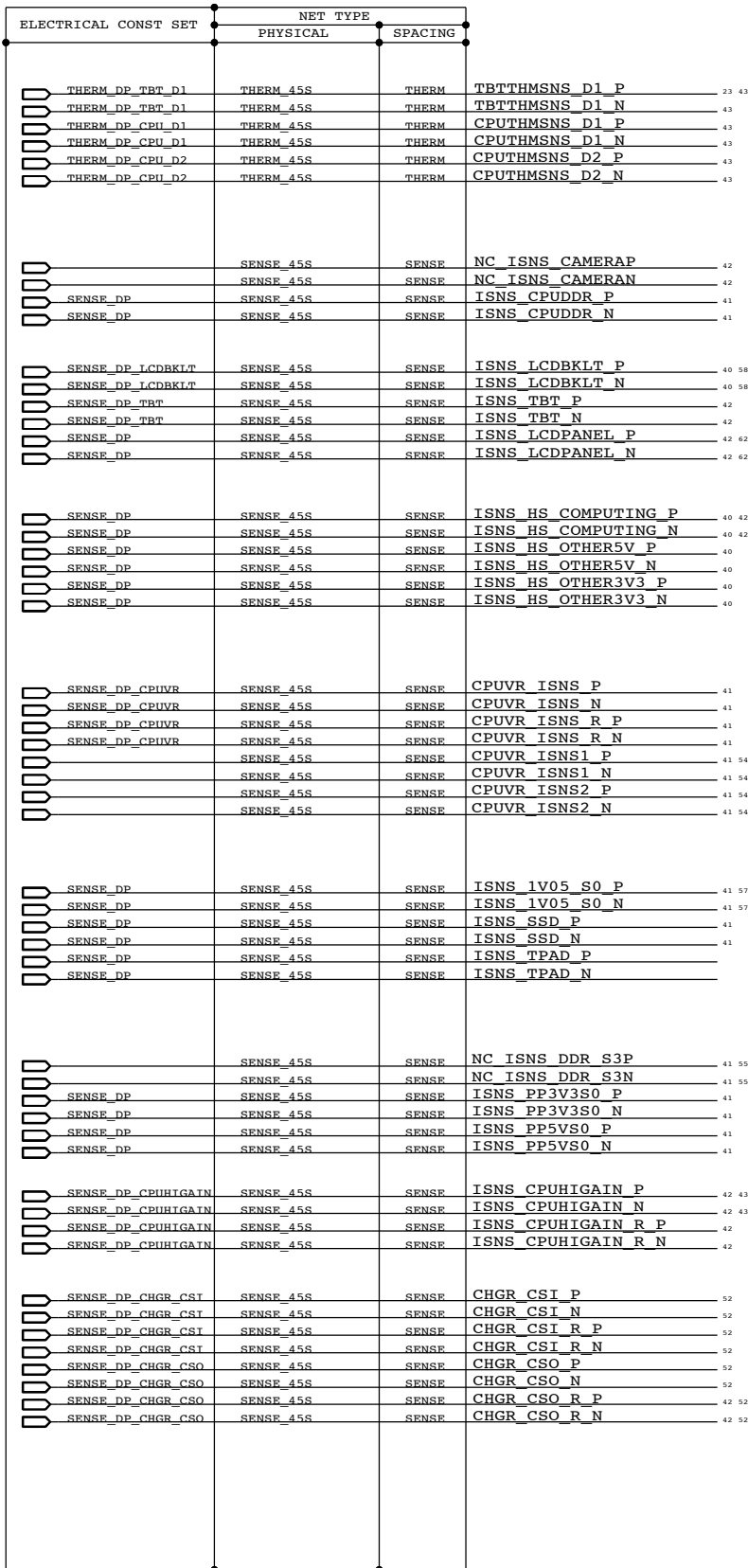
DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

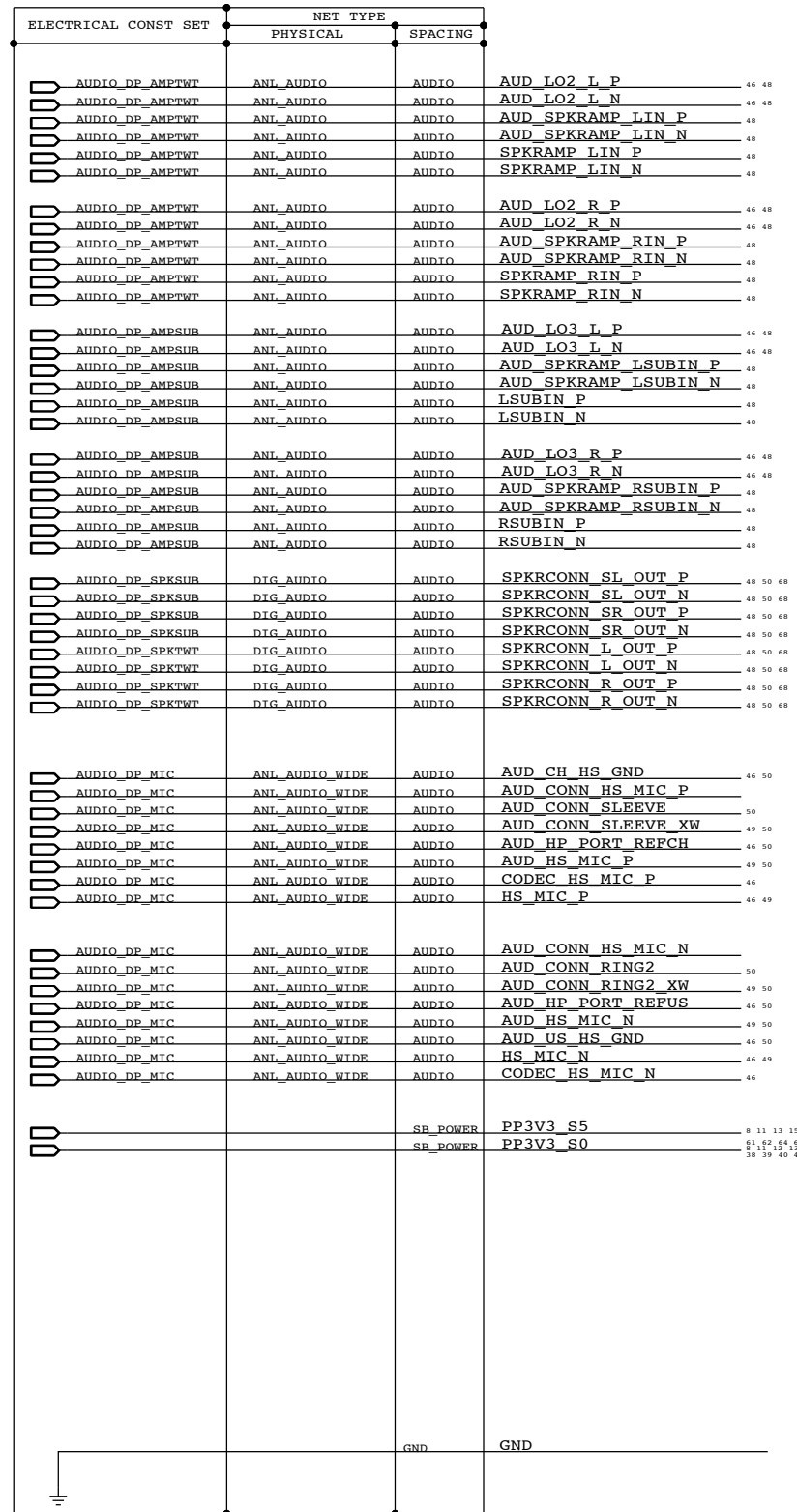
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO
1TO1_DIFFPAIR	*	1TO1_DIFFPAIR

J44 Specific Net Properties



J44 Specific Net Properties



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