1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-04-18

SCHEM,EVT,MLB,K21

04/18/11

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8870	1	SCHEM,MLB,K21	SCH	CRITICAL	
820-3023	1	PCBF,MLB,K21	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Apr 18 17:52:29 2011

PRODUCT SAFETY REQUIREMENTS:

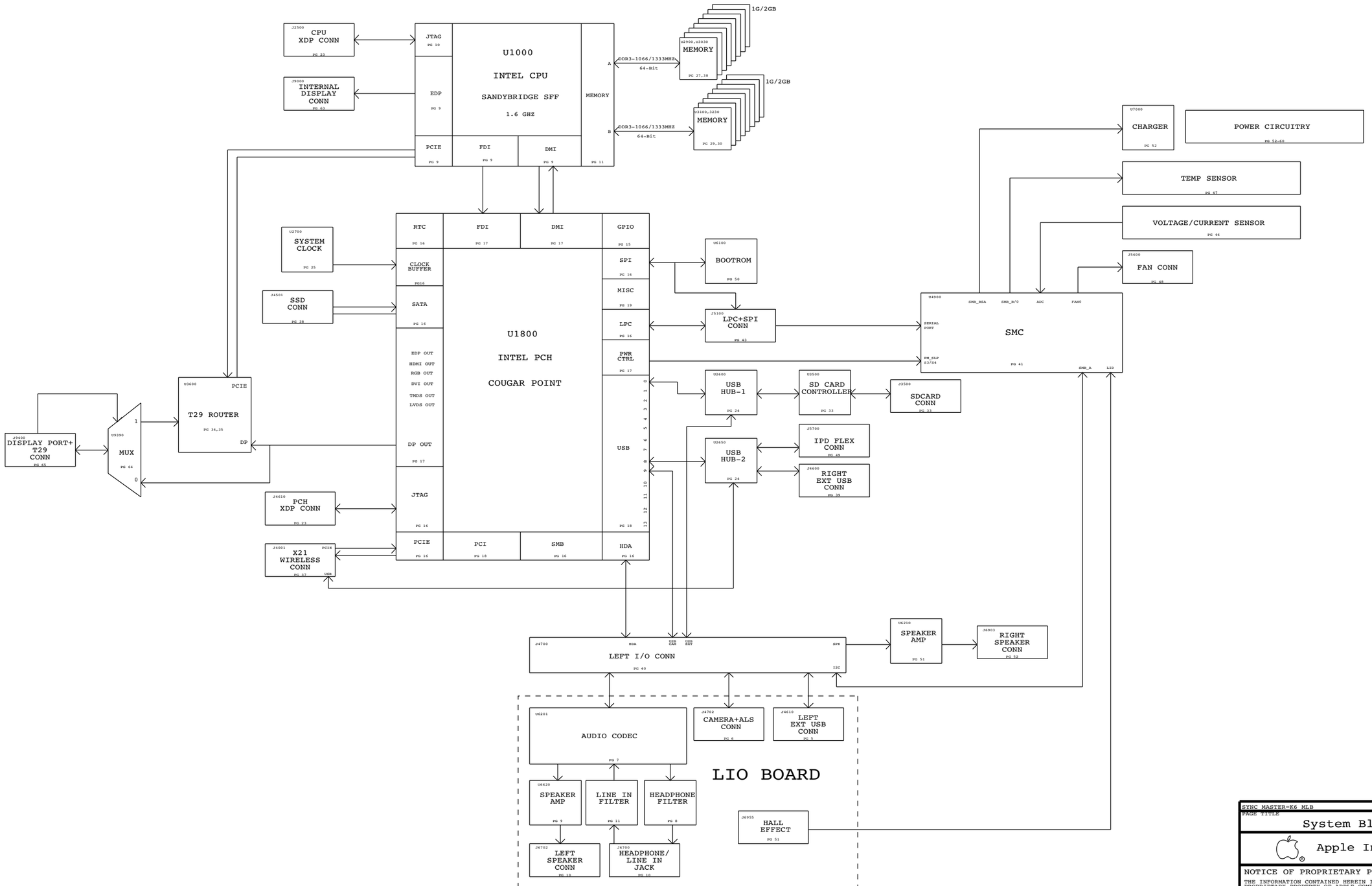
PCB,UL RECOGNIZED, MIN. 130-C TEMP RATING AND V-O FLAME RATING PER UL 796 & UL 94
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP RATING AND V-O FLAME RATING

DRAWING TITLE
SCHEM,MOCKUP,MLB,K21

Apple Inc.

DRAWING NUMBER 051-8870 | SIZE D
REVISION 3.13.0
BRANCH
PAGE 1 OF 109
SHEET 1 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=K6 MLB
SYNC DATE=12/11/2009

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 2 OF 109
SHEET 2 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

K78/K21 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN
DCIN(14.5V)
F6905 6A FUSE
SMC_DCIN_ISENSE
R7020
U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 53)
PPVBAT_G3H
SMC_RESET_L
R7050
SMC_BATT_ISENSE
Q7055
CHGR_BGATE
J6950 2S3P (6 TO 8.4V)
PPVBATT_G3H_CONN
PPVBAT_G3H_CHGR_R
PPDCIN_G3H_OR_PBUS
R6905
PPVIN_G3H_P3V42G3H
D6905
R6920
F7040
PPBUS_G3H
R5400
ENABLE 3.425V G3HOT LT3470A U6990 (PAGE 52)
PP3V42_G3H_REG
SMC POWER SN0903048 U5010 (PAGE 42)
SMC_RESET_L
PP5V_S0_CPUVCCIOS0
CPUVCCIOS0_EN
ISL95870 U7600 (PAGE 59)
R7640
PPCPUVCCIO_S0_REG
SMC_CPU_FSB_ISENSE
CPUVCCIOS0_PGOOD
TPS22924 U3816/U3815 (PAGE 36)
PP1V05_T29_FET
T29_PWR_EN
R5320 SMC_CPU_VSENSE
PPVCORE_S0_CPU_REG
CPU VCORE MAX15092GTL U7400 (PAGE 57)
CPUIMVP_VR_ON
R5330 SMC_GFX_VSENSE
PPVCORE_S0_AXG_REG
CPUIMVP_PGOOD
CPUIMVP_AXG_PGOOD
DDRREG_EN
DDRVTT_EN
1.5V 0.75V TPS51916 U7300 (PAGE 56)
R7350
PPDDR_S3_REG
PPVTT_S0_DDR_LDO
DDRREG_PGOOD
U7801
P1V5CPU_EN
PP1V5_S3RS0_FET
PP5V_S0_VCCSA
PVCCSA_EN
CPU_VCCSA_VID<1>
ISL95870A U7100 (PAGE 54)
R7140
PPVCCSA_S0_REG
PVCCSA_PGOOD
U2850
COUGAR-POINT (PCH) U1800 (PAGE 17~21)
PM_PCH_PWRGD
PM_PWRBTN_L
PM_SYSRST_L
PM_RSMRST_L
PM_DSW_PWRGD
PLT_RESET_L
CPU_PWRGD
PM_MEM_PWRGD
CPU U1000 (PAGE 9~15)
SM_DRAMPWROK
UNCOREPWRGOOD
RESET*
CPUIMVP_AXG_PGOOD
P1V8S0_PGOOD
P5VS3_PGOOD
P3V3S5_PGOOD
CPUVCCIOS0_PGOOD
PVCCSA_PGOOD
ALL_SYS_PWRGD
R7962
S5_PWRGD
SMC_ONOFF_L
SMC (PAGE 41)
PM_DSW_PWRGD
PM_RSMRST_L
CPUIMVP_VR_ON
PM_SYSRST_L
PM_PWRBTN_L
SMC_RESET_L
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
PP3V3_S0_VMON
PP5V_S0_VMON
PP1V5_S3RS0_VMON
PP1V05_S0_VMON
VDD U7960 ISL88042IRTEZ (PAGE 62)
SYNC_DATE=19/01/2011
SMC U4900 (PAGE 41)
SMC_PM_G2_EN
P3V3S5_EN
COUGAR-POINT (PCH) U1800 (PAGE 17~21)
SLP_S5#(E4)
PM_SLP_S5_L
PM_SLP_SUS_L
SLP_SUS#
U7940
P5V_3V3_SUS_EN
P3V3S3_EN
DDRREG_EN
P5VS3_EN
SLP_S4#(H4)
PM_SLP_S4_L
SLP_S3#(F4)
PM_SLP_S3_L
R7978
PM_SLP_S3_R_L
1V05_S0_LDO_EN
CPUVCCIOS0_EN
PVCCSA_EN
P1V5S0_EN
P1V8S0_EN
P5VS0_EN
P3V3S0_EN
PBUSVSENS_EN
PPVIN_S5_P5VP3V3
VIN 5V (L/H) 3.3V (R/H) TPS51980 U7201 (PAGE 55)
P5VS3_EN
P3V3S5_EN
PP5V_S3_REG
PP3V3_S5_REG
P5VS3_PGOOD
P3V3S5_PGOOD
Q7860
P5VS0_EN
PP5V_S0_FET
Q7820
TPS720105 U7740 (PAGE 60)
PP1V05_SUS_LDO
Q7810
Q7840
PP5V_SUS_FET
F9700
Q9706
LCD_BKLT_EN
&& BKLT_PLT_RST_L
VIN LP8550 U9701 (PAGE 66)
PPBUS_SW_LCDBKLT_PWR
PPVOUT_SW_LCDBKLT
Q5300
SMC_PBUS_VSENSE
PBUSVSENS_EN
Q3880
T29_A_HV_EN
T29BST_EN_UVLO
VIN LT3957 U3890 (PAGE 36)
PP15V_T29_REG
PP3V3_S0
P1V8S0_EN
ISL8014A U7720 (PAGE 60)
PP1V8_S0_REG
1V05_S0_LDO_EN
TPS720105 U7780 (PAGE 60)
PP1V05_S0_LDO.
U7770 TPS72015 (PAGE 60)
PP1V5_S0_REG
Q7830
T29_PWR_EN
TPS22924 U3810 (PAGE 36)
PP3V3_T29_FET
P3V3S0_EN

PAGE TITLE	Power Block Diagram
	Apple Inc.
DRAWING NUMBER	051-8870
SIZE	D
REVISION	3.13.0
BRANCH	
PAGE	3 OF 109
SHEET	3 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2684	K21i MLB DEVELOPMENT BOM	K21_DEVEL:ENG
607-8041	CMN PTS,PCBA,MLB,K21	K21_COMMON
639-2553	PCBA,MLB,1.8GHZ,HY 2GB,K21	K21_CMNPTS,EEEE:DP1F,CPU:1.8GHZ,DDR3:HYNIX_2GB
639-2554	PCBA,MLB,1.7GHZ,SA 4GB,K21	K21_CMNPTS,EEEE:DP1G,CPU:1.7GHZ,DDR3:SAMSUNG_4GB
639-2558	PCBA,MLB,1.8GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1H,CPU:1.8GHZ,DDR3:ELPIDA_4GB
639-2549	PCBA,MLB,1.7GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1J,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-2555	PCBA,MLB,1.8GHZ,HY 4GB,K21	K21_CMNPTS,EEEE:DP1K,CPU:1.8GHZ,DDR3:HYNIX_4GB
639-2557	PCBA,MLB,1.8GHZ,SA 4GB,K21	K21_CMNPTS,EEEE:DP1L,CPU:1.8GHZ,DDR3:SAMSUNG_4GB
639-2548	PCBA,MLB,1.7GHZ,HY 2GB,K21	K21_CMNPTS,EEEE:DP1M,CPU:1.7GHZ,DDR3:HYNIX_2GB
639-2550	PCBA,MLB,1.8GHZ,MI 2GB,K21	K21_CMNPTS,EEEE:DP1N,CPU:1.8GHZ,DDR3:MICRON_2GB
639-2551	PCBA,MLB,1.7GHZ,HY 4GB,K21	K21_CMNPTS,EEEE:DP1P,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-2552	PCBA,MLB,1.7GHZ,SA 2GB,K21	K21_CMNPTS,EEEE:DP1Q,CPU:1.7GHZ,DDR3:SAMSUNG_2GB
639-2556	PCBA,MLB,1.8GHZ,SA 2GB,K21	K21_CMNPTS,EEEE:DP1R,CPU:1.8GHZ,DDR3:SAMSUNG_2GB
639-2559	PCBA,MLB,1.7GHZ,MI 2GB,K21	K21_CMNPTS,EEEE:DP1T,CPU:1.7GHZ,DDR3:MICRON_2GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,LIO,K99	[EEEE_DP1F]	CRITICAL	EEEE:DP1F
825-7563	1	LABEL,LIO,K99	[EEEE_DP1G]	CRITICAL	EEEE:DP1G
825-7563	1	LABEL,LIO,K99	[EEEE_DP1H]	CRITICAL	EEEE:DP1H
825-7563	1	LABEL,LIO,K99	[EEEE_DP1J]	CRITICAL	EEEE:DP1J
825-7563	1	LABEL,LIO,K99	[EEEE_DP1K]	CRITICAL	EEEE:DP1K
825-7563	1	LABEL,LIO,K99	[EEEE_DP1L]	CRITICAL	EEEE:DP1L
825-7563	1	LABEL,LIO,K99	[EEEE_DP1M]	CRITICAL	EEEE:DP1M
825-7563	1	LABEL,LIO,K99	[EEEE_DP1N]	CRITICAL	EEEE:DP1N
825-7563	1	LABEL,LIO,K99	[EEEE_DP1P]	CRITICAL	EEEE:DP1P
825-7563	1	LABEL,LIO,K99	[EEEE_DP1Q]	CRITICAL	EEEE:DP1Q
825-7563	1	LABEL,LIO,K99	[EEEE_DP1R]	CRITICAL	EEEE:DP1R
825-7563	1	LABEL,LIO,K99	[EEEE_DP1T]	CRITICAL	EEEE:DP1T

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-2684	1	K21 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-8041	1	CMN PTS,PCBA,MLB,K21	CMNPTS	CRITICAL	K21_CMNPTS

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 4 OF 109

SHEET 4 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

K21 BOM GROUPS

BOM GROUP	BOM OPTIONS
K21_COMMON	ALTERNATE,COMMON,K21_MISC,K21_DEBUG:ENG,K21_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP,PCH:B3
K21_MISC	CPUMEM_SS,HUB1_2NONREM,HUB2_2NONREM,T29:YES,SDRVI2C:MCU,SDRV_PD,KB_BL
K21_PROGPARTS	BOOTROM_PROG,SMC_PROG,T29ROM:PROG,T29MCU:PROG
K21_DEVEL:ENG	BKLT:ENG,BMON:ENG,KDP_CONN,KDP_CPU:BPM,KDP_PCH,LPCPLUS,VREFMMGN,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
K21_DEVEL:PVT	LPCPLUS,KDP_CONN,KDP_PCH
K21_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,KDP
K21_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,KDP,VREFMMGN_HOT
K21_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,KDP,VREFMMGN_HOT,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33580550	1	IC,EEPROM,SERIAL,SPI,1Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341T0352	1	IC,T29-ROM,K21	U3690	CRITICAL	T29ROM:PROG
33783997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0353	1	IC,T29-MCU,K21	U9330	CRITICAL	T29MCU:PROG
33880895	1	IC,SMC,RENESAS,H8S/2117KP,9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341T0348	1	IC,SMC,K21	U4900	CRITICAL	SMC_PROG
33580809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
33580803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Numonyx	U6100	CRITICAL	BOOTROM_BLANK
341T0349	1	IC,EFI ROM,K21 K78	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Rohm alt to Toshiba
37780107	37780066		ALL	OKsemi alt to Semtech
13880676	13880691		ALL	Murata alt to Samsung
37180679	37180652		ALL	NXP alt to NXP
13880679	13880678		ALL	Murata/Samsung to Taiyo
13880671	13880673		ALL	Taiyo alt to Murata
33784092	33784100		ALL	EARLY 1.5GHZ CPU SAMPLES
33784093	33784101		ALL	EARLY 1.4GHZ CPU SAMPLES
35383312	35383055		ALL	NXP alt to Pericom
37680790	37680928		ALL	TI alt to Fairchild
12880333	12880294		ALL	Sanyo alt for Sanyo/Frederick
15281462	15281295		ALL	Toko alt for NEC inductor
10480035	10480011		ALL	Panasonic alt to Cyntec
15281085	15281307		ALL	Toko alt for Cyntec
514-0744	998-3941		ALL	Old J9400 alt to New J9400
37680874	37680895		ALL	FDMC0202S alt to RJK03E0DNS
13880703	13880648		ALL	Murata alt to Taiyo Yuden
13880684	13880660		ALL	Murata alt to Taiyo Yuden
33880721	33880923		ALL	SMSC USX2061 alt to USB2513B
15281493	15281300		ALL	Coilcraft alt to Murata

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4121	1	SNB,QAY8,QS,J1,1.8,17W,2+2,1.20,4M,BGA	U1000	CRITICAL	CPU:1.8GHZ
337S4119	1	SNB,QAYM,QS,J1,1.7,17W,2+2,1.20,3M,BGA	U1000	CRITICAL	CPU:1.7GHZ
337S4101	1	SNB,QAM1,QS,J1,1.6,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S4100	1	SNB,QAM2,QS,J1,1.5,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ
337S4099	1	SNB,QAM3,QS,J1,1.4,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S4098	1	SNB,QALV,QS,J1,1.3,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ
337S4080	1	COUGAR POINT,SLHAG,PRQ,BD82QS67	U1800	CRITICAL	PCH:B2
337S4091	1	COUGAR POINT,B3,SLJ4K,PRQ,BD82QS67	U1800	CRITICAL	PCH:B3
338S0976	1	IC,T29 Eagle Ridge,192 FCBGA,8x9MM	U3600	CRITICAL	T29:YES
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
353s2929	1	IC,ISL6259,BATCHARGER,3%,4X4MM,QFN28	U7000	CRITICAL	

PD Module Parts

806-2333	1	K21, T29 Fence	T29FENCE	CRITICAL	
806-2356	1	K21, T29 Can	T29CAN	CRITICAL	NOSTUFF
806-2347	1	K21, T29 Filter Can	T29FILTERCAN	CRITICAL	
806-2376	1	K78, mDP Can	MDPCAN	CRITICAL	
806-2377	1	K78, mDP Spring	MDPSPRING	CRITICAL	NOSTUFF

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 5 OF 109

SHEET: 5 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F	37	(Need 5 TPs)
TRUE	WIFI_EVENT_L	37 41	
TRUE	PCIE_AP_R2D_N	37 70	
TRUE	PCIE_AP_R2D_P	37 70	
TRUE	PCIE_CLK100M_AP_N	16 37 70	
TRUE	PCIE_CLK100M_AP_P	16 37 70	
TRUE	USB_BT_P	24 37 69	
TRUE	USB_BT_N	24 37 69	
TRUE	PCIE_AP_D2R_P	16 37 70	
TRUE	PCIE_AP_D2R_N	16 37 70	
TRUE	PCIE_WAKE_L	17 37	
TRUE	AP_RESET_CONN_L	37	
TRUE	AP_CLKREQ_O_L	37	
TRUE	=PP3V3_S3_BT	7 37	

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

TRUE	PP3V3_S0_HDD_R	38	(Need 5 TPs)
TRUE	SATA_HDD_D2R_C_P	38 69	
TRUE	SATA_HDD_D2R_C_N	38 69	
TRUE	SATA_HDD_R2D_N	38 69	
TRUE	SATA_HDD_R2D_P	38 69	
TRUE	SMC_HDD_OOB_TEMP_CONN	38	
TRUE	SMC_HDD_TEMP_CTL_CONN	38	

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	7 40	
TRUE	=PP3V3_S0_AUDIO	7 40	(Need 2 TPs)
TRUE	=PP3V3R1V5_S0_AUDIO	7 40	
TRUE	SYS_ONEWIRE	40 41	
TRUE	SMC_BC_ACOK	40 41 42	
TRUE	=USB_PWR_EN	39 40 62	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	=I2C_LIO_SDA	40 44	
TRUE	=I2C_LIO_SCL	40 44	
TRUE	=I2C_MIKEY_SCL	40 44	
TRUE	=I2C_MIKEY_SDA	40 44	
TRUE	AUD_IPHS_SWITCH_EN	19 40	
TRUE	AUD_IP_PERIPHERAL_DET	18 40	
TRUE	AUD_I2C_INT_L	18 40	
TRUE	AUD_GPIO_3	40 51	
TRUE	SPKRAMP_INR_N	40 51 74	
TRUE	SPKRAMP_INR_P	40 51 74	
TRUE	USB_EXTD_N	24 40 69	
TRUE	USB_EXTD_P	24 40 69	
TRUE	USB_CAMERA_N	18 40 69	
TRUE	USB_CAMERA_P	18 40 69	
TRUE	HDA_SDOUT	16 40 70	
TRUE	HDA_BIT_CLK	16 40 70	
TRUE	HDA_SDIN0	16 40 70	
TRUE	USB_EXTD_OC_L	24 40	
TRUE	HDA_RST_L	16 40 70	
TRUE	HDA_SYNC	16 40 70	

(Need to add 5 GND TPs)

J4800: SD Card Connector

FUNC_TEST

TRUE	PP3V3_SW_SD_PWR	33
TRUE	SD_CLK	33
TRUE	SD_CMD	33
TRUE	SD_D<7..0>	33
TRUE	SD_CD_L	33
TRUE	SD_WP	33

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	7 43
TRUE	=PP5V_S0_LPCPLUS	7 43
TRUE	LPC_AD<3..0>	16 41 43 70
TRUE	SPI_ALT_MOSI	43
TRUE	SPI_ALT_MISO	43
TRUE	LPC_FRAME_L	16 41 43 70
TRUE	PM_CLKRUN_L	17 41 43
TRUE	SMC_TMS	41 42 43
TRUE	LPCPLUS_RESET_L	25 43
TRUE	SMC_TDO	41 42 43
TRUE	SMC_TRST_L	41 43
TRUE	SMC_MD1	41 43
TRUE	SMC_TX_L	39 41 42 43
TRUE	LPC_CLK33M_LPCPLUS	25 43 70
TRUE	SPIROM_USE_MLB	19 43 50
TRUE	SPI_ALT_CLK	43
TRUE	SPI_ALT_CS_L	43
TRUE	LPC_SERIRQ	16 41 43
TRUE	LPC_PWRDWN_L	17 41 43
TRUE	SMC_TDI	41 42 43
TRUE	SMC_TCK	41 42 43
TRUE	SMC_RESET_L	41 42 43 53
TRUE	SMC_NMI	41 43
TRUE	SMC_RX_L	39 41 42 43
TRUE	LPCPLUS_GPIO	19 43

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	7 48	
TRUE	FAN_RT_TACH	48	
TRUE	FAN_RT_PWM	48	

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	PP3V3_TPAD_CONN	49	
TRUE	PP5V_TPAD_FILT	49	
TRUE	=PP3V42_G3H_TPAD	7 49	
TRUE	USB_TPAD_CONN_P	49 74	
TRUE	USB_TPAD_CONN_N	49 74	
TRUE	=I2C_TPAD_SDA	44 49	
TRUE	=I2C_TPAD_SCL	44 49	
TRUE	SMC_ONOFF_L	41 42 49	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	SMC_TPAD_RST_L	42 49	
TRUE	SMC_PME_S4_WAKE_L	41 42 49	

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	7 52	(Need 6 TPs)
TRUE	=PP5V_S3_LIO_CONN	7 52	

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_R_P_OUT	51 52 74	
TRUE	SPKRAMP_R_N_OUT	51 52 74	

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	52 53	(Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	44 52	
TRUE	=SMBUS_BATT_SDA	44 52	
TRUE	SYS_DETECT_L	52	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	63 66	(Need 2 TPs)
TRUE	PP3V3_SW_LCD	63	(Need 2 TPs)
TRUE	I2C_TCON_SDA_R	63	
TRUE	I2C_TCON_SCL_R	63	
TRUE	LED_RETURN_6	63 66	
TRUE	LED_RETURN_5	63 66	
TRUE	LED_RETURN_4	63 66	
TRUE	LED_RETURN_3	63 66	
TRUE	LED_RETURN_2	63 66	
TRUE	LED_RETURN_1	63 66	
TRUE	DP_INT_HPD_CONN	63	
TRUE	DP_INT_AUX_CH_C_N	63 70	
TRUE	DP_INT_AUX_CH_C_P	63 70	
TRUE	DP_INT_ML_F_P<0>	63 70	
TRUE	DP_INT_ML_F_N<0>	63 70	
TRUE	DP_INT_ML_F_P<1>	63 70	
TRUE	DP_INT_ML_F_N<1>	63 70	

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	7 52	
TRUE	PPVIN_SW_T29BST	7 36	
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7	
TRUE	PPDCIN_G3H	7	
TRUE	PP3V42_G3H	7	
TRUE	PPVRTC_G3H	7	
TRUE	PP5V_S5	7	
TRUE	PP5V_SUS	7	
TRUE	PP3V3_S5	7 74	
TRUE	PP3V3_SUS	7	
TRUE	PP3V3_S3	7	
TRUE	PP1V8_S0	7	
TRUE	PP3V3_S0	7 74	
TRUE	PP1V5_S3	7 68	
TRUE	PP1V5_S3RS0	7 68	
TRUE	PP1V5_S0	7	
TRUE	PP1V05_S0	7	
TRUE	PPVTTDDR_S3	7	
TRUE	PP0V75_S0_DDRVTT	7	
TRUE	PPVCCSA_S0_CPU	7	
TRUE	PP1V05_SUS	7	
TRUE	PP15V_T29	7	
TRUE	PP3V3_T29	7	
TRUE	PP1V05_T29	7 36	
TRUE	PP1V05_S0_PCH_VCCADPLL	7	
TRUE	PPVCORE_S0_CPU	7	
TRUE	PPVCORE_S0_AXG	7	
TRUE	PP1V5_S3_CPU_VCCDQ	7	
TRUE	PP1V05_S0_CPU_VCCPQE	7	
TRUE	PP1V8_S0_CPU_VCCPLL_R	7	

(Need to add 27 GND TPs)

J5715: KB BKLT CONNECTOR

FUNC_TEST

TRUE	KBDLED_FB	49	
TRUE	KBDLED_ANODE	49	

(Need to add 2 GND TP)

NO_TEST Nets

NO_TEST

17	TP_CRT_IG_BLUE	TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	TRUE	NC_CRT_IG_VSYNC
	TP_LVDS_IG_CTRL_CLK	TRUE	NC_LVDS_IG_CTRL_CLK
	TP_LVDS_IG_CTRL_DATA	TRUE	NC_LVDS_IG_CTRL_DATA
	TP_PCH_LVDS_VBG	TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	TRUE	NC_PCI_CLK33M_OUT3
16	TP_CLINK_CLK	TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	TRUE	NC_PCIE_CLK100M_PEBP

R592	XDP_PCH_AP_PWR_EN		
R593	XDP_PCH_USB_HUB_SOFT_RST_L	23	
R594	XDP_PCH_SDCONN_STATE_RST_L	23	
R595	XDP_PCH_ENET_PWR_EN	23	
R596	XDP_PCH_SDCONN_DET_L	23	
R597	XDP_PCH_S5_PWRGD	23	
R598	XDP_PCH_PWRBTN_L	23	
R599	XDP_PCH_ISOLATE_CPU_MEM_L	23	
R600	XDP_FW_CLKREQ_L		
R601	XDP_AP_CLKREQ_L	23	
R602	XDP_PCH_AUD_IPHS_SWITCH_EN	23	

17	TP_SDVO_TVCLKINN	TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	TRUE	NC_SDVO_INTP
23	TP_XDP_PCH_OBSFN_A<0..1>	TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDPPCH_HOOK2	TRUE	NC_TP_XDPPCH_HOOK2
23	TP_XDPPCH_HOOK3	TRUE	NC_TP_XDPPCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	TRUE	NC_TP_XDP_PCH_HOOK5
16	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

	NC_EDP_TXP<0..3>	TRUE	TP_EDP_TX_P<0..3> 9
	NC_EDP_TXN<0..3>	TRUE	TP_EDP_TX_N<0..3> 9
	NC_EDP_AUXP	TRUE	TP_EDP_AUX_P
	NC_EDP_AUXN	TRUE	TP_EDP_AUX_N
	NC_CPU_THERMDA	TRUE	TP_CPU_THERMDA
	NC_CPU_THERMDC	TRUE	TP_CPU_THERMDC
	NC_CPU_RSVD<30..45>	TRUE	TP_CPU_RSVD<30..45>
	NC_CPU_RSVD<8..27>	TRUE	TP_CPU_RSVD<8..27>
	NC_PEG_R2D_CP<15..4>	TRUE	=PEG_R2D_C_P<15..4> 9
	NC_PEG_R2D_CN<15..4>	TRUE	=PEG_R2D_C_N<15..4> 9
	NC_PEG_D2RP<15..4>	TRUE	=PEG_D2R_P<15..4> 9
	NC_PEG_D2RN<15..4>	TRUE	=PEG_D2R_N<15..4> 9

16	TP_PCIE_CLK100M_PE4N	TRUE	NC_PCIE_CLK100M_PE4N
16	TP_PCIE_CLK100M_PE4P	TRUE	NC_PCIE_CLK100M_PE4P
16	TP_PCIE_CLK100M_PE5N	TRUE	NC_PCIE_CLK100M_PE5N
16	TP_PCIE_CLK100M_PE5P	TRUE	NC_PCIE_CLK100M_PE5P
16	TP_PCIE_CLK100M_PE6N	TRUE	NC_PCIE_CLK100M_PE6N
16	TP_PCIE_CLK100M_PE6P	TRUE	NC_PCIE_CLK100M_PE6P
16	TP_PCIE_CLK100M_PE7N	TRUE	NC_PCIE_CLK100M_PE7N
16	TP_PCIE_CLK100M_PE7P	TRUE	NC_PCIE_CLK100M_PE7P
	TP_PROC_P1_3	TRUE	NC_PROC_P1_3
16	TP_SATA_B_D2RN	TRUE	NC_SATA_B_D2RN
16	TP_SATA_B_D2RP	TRUE	NC_SATA_B_D2RP
16	TP_SATA_B_R2D_CN	TRUE	NC_SATA_B_R2D_CN
16	TP_SATA_B_R2D_CP	TRUE	NC_SATA_B_R2D_CP
16	TP_SATA_D_D2RN	TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	TRUE	NC_SATA_F_R2D_CP

	TP_PCH_TP18	TRUE	NC_PCH_TP18
	TP_PCH_TP17	TRUE	NC_PCH_TP17
	TP_PCH_TP16	TRUE	NC_PCH_TP16
	TP_PCH_TP15	TRUE	NC_PCH_TP15
	TP_PCH_TP14	TRUE	NC_PCH_TP14
	TP_PCH_TP13	TRUE	NC_PCH_TP13
	TP_PCH_TP12	TRUE	NC_PCH_TP12
	TP_PCH_TP10	TRUE	NC_PCH_TP10
	TP_PCH_TP9	TRUE	NC_PCH_TP9
	TP_PCH_TP8	TRUE	NC_PCH_TP8
	TP_PCH_TP7	TRUE	NC_PCH_TP7
	TP_PCH_TP6	TRUE	NC_PCH_TP6
	TP_PCH_TP5	TRUE	NC_PCH_TP5
	TP_PCH_TP4	TRUE	NC_PCH_TP4
	TP_PCH_TP3	TRUE	NC_PCH_TP3
	TP_PCH_TP2	TRUE	NC_PCH_TP2
	TP_PCH_TP1	TRUE	NC_PCH_TP1

R562	PCH_VSS_NCTF<1>	70	
R563	PCH_VSS_NCTF<2>	70	
R564	PCH_VSS_NCTF<5>	70	
R570	PCH_VSS_NCTF<9>	70	
R571	PCH_VSS_NCTF<11>	70	
R560	PCH_VSS_NCTF<12>	70	
R500	PCH_VSS_NCTF<15>	70	
R495	PCH_VSS_NCTF<17>	70	
R501	PCH_VSS_NCTF<19>	6 70	
R502	PCH_VSS_NCTF<19>	6 70	
R503	PCH_VSS_NCTF<21>	70	
R504	PCH_VSS_NCTF<25>	70	
R505	PCH_VSS_NCTF<27>	70	
R506	PCH_VSS_NCTF<29>	70	

8	TP_LVDS_IG_B_CLKN	TRUE	NC_LVDS_IG_B_CLKN
8	TP_LVDS_IG_B_CLKP	TRUE	NC_LVDS_IG_B_CLKP
	TP_LVDS_IG_BKL_PWM	TRUE	NC_LVDS_IG_BKL_PWM
	SMC_BS_ALRT_L	TRUE	NC_SMC_BS_ALRT_L

SYNC_MASTER=(K99 MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE

Functional Test / No Test

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 7 OF 109

SHEET 6 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

"G3Hot" (Always-Present) Rails

53 =PPBUS_G3H
- PPBUS_G3H — 6 52
  - MIN_LINE_WIDTH=0.6 mm
  - MIN_NECK_WIDTH=0.25 mm
  - VOLTAGE=12.6V
  - MAKE_BASE=TRUE
  - =PPBUS_S0_LCDBKLT — 66
  - =PPBUS_S0_VSENSE — 45
  - =PPVIN_SW_T29BST — 8 36
  - =PPVIN_S5_HS_COMPUTING_ISNS_R — 46
  - =PPVIN_S5_P5VP3V3 — 55

36 6 PPVIN_SW_T29BST (VOLTAGE=12.6V)

46 =PPVIN_S5_HS_COMPUTING_ISNS
- PPBUS_S5_HS_COMPUTING_ISNS — 6
  - MIN_LINE_WIDTH=0.6 mm
  - MIN_NECK_WIDTH=0.25 mm
  - VOLTAGE=12.6V
  - MAKE_BASE=TRUE
  - =PPVIN_S0_CPUIMVP — 57 58
  - =PPVIN_S3_DDRREG — 56
  - =PPVIN_S0_CPUVCCIOS0 — 59
  - =PPVIN_S0_VCCSAS0 — 54
  - =PPVIN_S0_CPUAXG — 58

52 6 =PP18V5_DCIN_CONN
- PPDCIN_G3H — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.25 MM
  - VOLTAGE=18.5V
  - MAKE_BASE=TRUE
  - =PPDCIN_S5_CHGR — 53
  - =PPDCIN_S5_VSENSE — 45

52 =PP3V42_G3H_REG
- PP3V42_G3H — 6
  - MIN_LINE_WIDTH=0.3 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=3.42V
  - MAKE_BASE=TRUE
  - =PP3V3_S5_LPCPLUS — 6 43
  - =PP3V3_S5_SMC — 41 42
  - =PP3V42_G3H_CHGR — 53
  - =PP3V42_G3H_PWRCTL — 62
  - =PP3V42_G3H_SMBUS_SMC_BSA — 44
  - =PP3V42_G3H_SMCUSBMUX — 39
  - =PP3V42_G3H_TPAD — 6 49
  - =PPVIN_S5_SMCVREF — 42
  - =PPVBAT_G3_SYSCLK — 25
  - =PP3V42_G3H_ONEWIRE — 6 40

25 =PPVRTC_G3_OUT
- PPVRTC_G3H — 6
  - MIN_LINE_WIDTH=0.2 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=3V
  - MAKE_BASE=TRUE
  - =PPVRTC_G3_PCH — 16 17 20

5V Rails

55 =PP5V_S5_LDO
- PP5V_S5 — 6
  - MIN_LINE_WIDTH=0.5 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=5V
  - MAKE_BASE=TRUE
  - =PP5V_S5_P1V5DDRFET — 61
  - =PP5V_S5_P5VSUSFET — 61
  - =PP5V_S5_TPAD — 49

61 =PP5V_SUS_FET
- PP5V_SUS — 6
  - MIN_LINE_WIDTH=0.50MM
  - MIN_NECK_WIDTH=0.20MM
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
  - =PP5V_SUS_PCH — 22

55 =PP5V_S3_REG
- PP5V_S3 — 6
  - MIN_LINE_WIDTH=0.5 mm
  - MIN_NECK_WIDTH=0.2 mm
  - VOLTAGE=5V
  - MAKE_BASE=TRUE
  - =PP5V_S3_AUDIO_AMP — 51
  - =PP5V_S3_DDRREG — 56
  - =PP5V_S3_MEMRESET — 26
  - =PP5V_S3_P5VS0FET — 61
  - =PP5V_S3_RTUSB — 39
  - =PP5V_S3_LIO_CONN — 6 52

61 =PP5V_S0_FET
- PP5V_S0 — 6
  - MIN_LINE_WIDTH=0.4 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=5V
  - MAKE_BASE=TRUE
  - =PP5V_S0_BKL — 66
  - =PP5V_S0_CPUIMVP — 57
  - =PP5V_S0_CPUVCCIOS0 — 59
  - =PP5V_S0_FAN — 6 48
  - =PP5V_S0_LPCPLUS — 6 43
  - =PP5V_S0_VCCSA — 54
  - =PP5V_S0_PCH — 22
  - =PP5V_S0_VMON — 62
  - =PP5V_S0_KBDLED — 49

3.3V Rails

55 =PP3V3_S5_REG
- PP3V3_S5 — 6 74
  - MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
  - MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
  - =PP3V3_S5_XDP — 23
  - =PP3V3_S0_P3V3S0FET — 61
  - =PP3V3_S3_P3V3S3FET — 61
  - =PP3V3_S5_CPU_VCCDDR — 26
  - =PP3V3_S5_LCD — 63
  - =PP3V3_S5_PCH — 17 19
  - =PP3V3_S5_PCHPWRGD — 25
  - =PP3V3_S5_SMCBATLOW — 42
  - =PP3V3_S5_ROM — 50
  - =PP3V3_S5_USB_RESET — 24
  - =PP3V3_S5_PCH_VCCDSW — 20 22
  - =PP3V3_S5_SYSCLK — 25
  - =PP3V3_S5_VMON — 62
  - =PP3V3_S5_PWRCTL — 62
  - =PP3V3_S5_PCH_VCC_SPI — 20 22
  - =PP3V3_S5_P3V3SUSFET — 61
  - =PP3V3_S5_TPAD — 49
  - =PP3V3_S4_DPAPWRSW — 65
  - =PP3V3_S4_SMC — 42

61 =PP3V3_SUS_FET
- PP3V3_SUS — 6
  - MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
  - MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
  - =PP3V3_SUS_PCH_VCCSUS_USB — 20 22
  - =PP3V3_SUS_PCH_VCCSUS_GPIO — 20 22
  - =PP3V3_SUS_PCH_VCCSUS — 20
  - =PP3V3_SUS_GPIO — 16 17 18 19
  - =PP3V3_SUS_PCH — 22
  - =PP3V3_SUS_PWRCTL — 62
  - =PP3V3_SUS_P1V05SUSLDO — 60
  - =PP3V3_SUS_SMC — 42

61 =PP3V3_S3_FET
- PP3V3_S3 — 6
  - MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
  - MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
  - =PP3V3_S3_BT — 6 37
  - =PP3V3_S3_CARDREADER — 33
  - =PP3V3_S3_MEMRESET — 26
  - =PP3V3_S3_SMBUS_SMC_A_S3 — 44
  - =PP3V3_S3_SMBUS_SMC_MGMT — 44
  - =PP3V3_S3_USB_HUB — 8 24
  - =PP3V3_S3_USB_RESET — 24
  - =PP3V3_S3_VREFMRGN — 31
  - =PP3V3_S3_WLAN — 37
  - =PP3V3_S3_WLANISNS — 46
  - =PP3V3_S3_BMON_ISNS — 46
  - =PP3V3_S3_PCH_GPIO — 18 19
  - =PP3V3_S3_1V5S3ISNS — 46
  - =PP3V3_S3_DBGLEDS — 52

61 =PP3V3_S0_FET
- PP3V3_S0 — 6 74
  - MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
  - MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
  - =PP3V3_S0_CPUVCCIOISNS — 45
  - =PP3V3_S0_AUDIO — 6 40
  - =PP3V3_S0_BKL_VDDIO — 66
  - =PP3V3_S0_HS_COMPUTING_ISNS — 46
  - =PP3V3_S0_CPUTHMSNS — 47
  - =PP3V3_S0_CPU_VCCIO_SEL — 12
  - =PP3V3_S0_DP_DDC — 8
  - =PP3V3_S0_FAN — 48
  - =PP3V3_S0_P3V3T29FET — 36
  - =PP3V3_S0_P1V8S0 — 60
  - =PP3V3_S0_PCH — 16 19 22
  - =PP3V3_S0_PCH_GPIO — 18
  - =PP3V3_S0_PCH_VCC3_3_CLK — 22
  - =PP3V3_S0_PCH_VCC3_3_GPIO — 20 22
  - =PP3V3_S0_PCH_VCC3_3_HVCMOS — 20 22
  - =PP3V3_S0_PCH_VCC3_3_PCI — 20 22
  - =PP3V3_S0_PCH_VCC3_3_SATA — 20 22
  - =PP3V3_S0_PCH_VCCADAC — 22
  - =PP3V3_S0_PCH_STRAPS — 16 17 19
  - =PP3V3_S0_PWRCTL — 62
  - =PP3V3_S0_RSTBUF — 25
  - =PP3V3_S0_SB_PM — 25
  - =PP3V3_S0_SMBUS_PCH — 44
  - =PP3V3_S0_SMBUS_SMC_0_S0 — 44
  - =PP3V3_S0_SMBUS_SMC_B_S0 — 44
  - =PP3V3_S0_SMC — 42
  - =PP3V3_S0_HDD — 38
  - =PP3V3_S0_HDDISNS — 46
  - =PP3V3_S0_VMON — 62
  - =PP3V3_S0_P1V5S0 — 60
  - =PP3V3_S0_T29PWRCTL — 36
  - =PP3V3_S0_DPSDRVA — 64
  - =PP3V3_S0_P1V05S0LDO — 60
  - =PP3V3_S0_IMVPISNS — 45
  - =PP3V3_S0_XDP — 23
  - =PP3V3_S0_T29I2C — 44
  - =PP3V3_S0_BKLTISNS — 46
  - =PP3V3_S0_SYSCLKGEN — 25

1.8V/1.5V/1.2V/1.05V Rails

60 =PP1V8_S0_REG
2A max supply
- PP1V8_S0 — 6
  - MIN_LINE_WIDTH=0.5 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.8V
  - MAKE_BASE=TRUE
  - =PP1V8_S0_CPU_VCCPLL — 14
  - =PP1V8_S0_PCH_VCC_DFTERM — 18 20 22
  - =PP1V8_S0_P1V05S0LDO — 60
  - =PP1V8R1V5_S0_PCH_VCCVRM — 20
  - =PPVDDIO_S0_SBCLK — 25
  - =PP1V8_S0_P1V5S0 — 60

56 =PPDDR_S3_REG
- PP1V5_S3 — 6 68
  - MIN_LINE_WIDTH=0.8 MM
  - MIN_NECK_WIDTH=0.1 MM
  - VOLTAGE=1.5V
  - MAKE_BASE=TRUE
  - =PP1V5_S3_MEMRESET — 26
  - =PP1V5_S3_MEM_A — 27 28 32
  - =PP1V5_S3_MEM_B — 29 30 32
  - =PP1V5_S3_P1V5S3RS0_FET — 61
  - =PPVIN_S0_DDRREG_LDO — 56

61 =PP1V5_S3RS0_FET
- PP1V5_S3RS0 — 6 68
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.5V
  - MAKE_BASE=TRUE
  - =PP1V5_S3_CPU_VCCDDR — 10 12 15 26
  - =PP1V5_S3RS0_VMON — 62

60 =PP1V5_S0_REG
- PP1V5_S0 — 6
  - MIN_LINE_WIDTH=2 mm
  - MIN_NECK_WIDTH=0.17 mm
  - VOLTAGE=1.5V
  - MAKE_BASE=TRUE
  - =PP3V3R1V5_S0_AUDIO — 6 40
  - =PP3V3R1V5_S0_PCH_VCCSUSHDA — 16 20 22

56 31 =PPVTT_S3_DDR_BUF
- PPVTTDDR_S3 — 6
  - MIN_LINE_WIDTH=0.3 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=0.75V
  - MAKE_BASE=TRUE

56 =PPVTT_S0_DDR_LDO
- PP0V75_S0_DDRVTT — 6
  - MIN_LINE_WIDTH=2 mm
  - MIN_NECK_WIDTH=0.17 mm
  - VOLTAGE=0.75V
  - MAKE_BASE=TRUE
  - =PP0V75_S0_MEM_VTT_A — 32
  - =PP0V75_S0_MEM_VTT_B — 32
  - =PPVTT_S0_VTTCLAMP — 26

54 =PPVCCSA_S0_REG
- PPVCCSA_S0_CPU — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=0.9V
  - MAKE_BASE=TRUE
  - =PPVCCSA_S0_CPU — 12 15

60 =PP1V05_SUS_LDO
- PP1V05_SUS — 6
  - MIN_LINE_WIDTH=0.4 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.05V
  - MAKE_BASE=TRUE
  - =PP1V05_SUS_PCH_JTAG — 23

59 =PPCPUVCCIO_S0_REG
? mA
- PP1V05_S0 — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.05V
  - MAKE_BASE=TRUE
  - =PP1V05_S0_PCH_VCCIO_PLLPCIE — 20
  - =PP1V05_S0_CPU_VCCIO — 9 10 12 14
  - =PP1V05_S0_PCH — 16 22
  - =PP1V05_S0_PCH_VCCIO — 20 22
  - =PP1V05_S0_PCH_VCCIO_PCIE — 17
  - =PP1V05_S0_PCH_VCCIO_SATA — 16 20 22
  - =PP1V05_S0_PCH_VCCASW — 20 22
  - =PP1V05_S0_PCH_VCCIO_USB — 20 22
  - =PP1V05_S0_PCH_VCC_CORE — 20 22
  - =PP1V05_S0_VMON — 62
  - =PP1V05_S0_PCH_VCCIO_CLK — 20 22
  - =PPVCCIO_S0_CPUIMVP — 57
  - =PP1V05_S0_PCH_VCCDIFFCLK — 16 20 22
  - =PP1V05_S0_PCH_VCCSSC — 20 22
  - =PP1V05_S0_PCH_V_PROC_IO — 20 22
  - =PP1V05_S0_PCH_VCCIO_PLLUSB — 20
  - =PP1V05_S0_PCH_VCC_DMI — 20 22
  - =PP1V05_S0_PCH_VCCIO_PLLFDI — 20
  - =PP1V05_S0_PCH_VCCDMI_FDI — 20
  - =PPVCCIO_S0_XDP — 23
  - =PPVCCIO_S0_SMC — 41
  - =PP1V05_S0_P1V05T29FET — 36

T29 Rails (off when no cable)

36 8 =PP15V_T29_REG
- PP15V_T29 — 6
  - MIN_LINE_WIDTH=0.4 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=17.6V
  - MAKE_BASE=TRUE
  - =PPHV_SW_DPAPWRSW — 65

36 =PP3V3_T29_FET
- PP3V3_T29 — 6
  - MIN_LINE_WIDTH=0.4 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
  - =PPVDDIO_T29_CLK — 25
  - =PP3V3_T29_RTR — 34 35 36
  - =PP3V3_T29_PCH_GPIO — 16 19

36 =PP1V05_T29_FET
- PP1V05_T29 — 6 36
  - MIN_LINE_WIDTH=0.4 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.05V
  - MAKE_BASE=TRUE
  - =PP1V05_T29_RTR — 35

1V05 S0 LDO

60 =PP1V05_S0_LDO
- PP1V05_S0_PCH_VCCADPLL — 6
  - MIN_LINE_WIDTH=0.4 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.05V
  - MAKE_BASE=TRUE
  - =PP1V05_S0_PCH_VCCADPLL — 20

Chipset "VCore" Rails

58 =PPVCORE_S0_CPU_REG
- PPVCORE_S0_CPU — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.25 MM
  - VOLTAGE=1.25V
  - MAKE_BASE=TRUE
  - =PPVCORE_S0_CPU — 9 12 14
  - =PPCPUVCORE_S0_VSENSE — 45

58 =PPVCORE_S0_AXG_REG
- PPVCORE_S0_AXG — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.05V
  - MAKE_BASE=TRUE
  - =PPVCORE_S0_CPU_VCCAXG — 9 12 15
  - =PPGFXVCORE_S0_VSENSE — 45

15 12 =PP1V5_S3_CPU_VCCDQ
- PP1V5_S3_CPU_VCCDQ — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.5V
  - MAKE_BASE=TRUE

14 12 =PP1V05_S0_CPU_VCCPQE
- PP1V05_S0_CPU_VCCPQE — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.05V
  - MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R
- PP1V8_S0_CPU_VCCPLL_R — 6
  - MIN_LINE_WIDTH=0.6 MM
  - MIN_NECK_WIDTH=0.2 MM
  - VOLTAGE=1.8V
  - MAKE_BASE=TRUE

SYNC MASTER=K91 MLB — SYNC DATE=05/15/2010

PAGE TITLE: Power Aliases

Apple Inc.

DRAWING NUMBER: 051-8870 — SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 8 OF 109

SHEET: 7 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Plated Board Slot

SL0900
TH-NSP
SL-2.3X3.9-2.9X4.5

CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss

Z0905
STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0914
STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0915
STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

USB/SD Card Pogo

CRITICAL
ZS0906
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

DisplayPort PCB Stiffener

(Provides PCB support for small finger above J9400)

NO STUFF
MT0900
STIFFENER-K16-K99
SM-SP
806-1176

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

T29 Can Slots

SL0901 TH-NSP SL-1.1X0.4-1.4X0.7
SL0902 TH-NSP SL-1.1X0.4-1.4X0.7
SL0903 TH-NSP SL-1.1X0.45-1.4X0.75
SL0904 TH-NSP SL-1.1X0.45-1.4X0.75
SL0905 TH-NSP SL-1.1X0.45-1.4X0.75
SL0906 TH-NSP SL-1.1X0.45-1.4X0.75

CPU signals

MEMVTT_EN (26) MAKE_BASE=TRUE — =DDRVTT_EN (26 56)

DP_EXTA_ML_C_P<3..0> (69) MAKE_BASE=TRUE	DP_IG_ML_P<3..0>	TP_DP_IG_B_MLP<3..0> (17)
DP_EXTA_ML_C_N<3..0> (69) MAKE_BASE=TRUE	DP_IG_ML_N<3..0>	TP_DP_IG_B_MLN<3..0> (17)
DP_EXTA_AUXCH_C_P (69) MAKE_BASE=TRUE	DP_IG_AUX_CH_P	DP_IG_B_AUX_P (17)
DP_EXTA_AUXCH_C_N (69) MAKE_BASE=TRUE	DP_IG_AUX_CH_N	DP_IG_B_AUX_N (17)

PCIE_EXCARD_D2R_N (16)	75OHM MAKE_BASE=TRUE	NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_D2R_P (16)	75OHM MAKE_BASE=TRUE	NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_R2D_C_N (16)	75OHM MAKE_BASE=TRUE	NC_PCIE_EXCARD_R2D_CN
PCIE_EXCARD_R2D_C_P (16)	75OHM MAKE_BASE=TRUE	NC_PCIE_EXCARD_R2D_CP
PCIE_CLK100M_EXCARD_N (70 16)	75OHM MAKE_BASE=TRUE	NC_PCIE_CLK100M_EXCARDN
PCIE_CLK100M_EXCARD_P (70 16)	75OHM MAKE_BASE=TRUE	NC_PCIE_CLK100M_EXCARDP
PEG_CLK100M_P (70 16)	MAKE_BASE=TRUE	NC_PEG_CLK100MP
PEG_CLK100M_N (70 16)	MAKE_BASE=TRUE	NC_PEG_CLK100MN

MEM_A_CLK_P<1> (68 11)	MAKE_BASE=TRUE	TP_MEM_A_CLKP<1>
MEM_A_CLK_N<1> (68 11)	MAKE_BASE=TRUE	TP_MEM_A_CLKN<1>
MEM_A_CKE<1> (68 11)	MAKE_BASE=TRUE	NC_MEM_A_CKE<1>
MEM_A_CS_L<1> (68 11)	MAKE_BASE=TRUE	NC_MEM_A_CS_L<1>
MEM_A_ODT<1> (68 11)	MAKE_BASE=TRUE	NC_MEM_A_ODT<1>
MEM_B_CLK_P<1> (68 11)	MAKE_BASE=TRUE	TP_MEM_B_CLKP<1>
MEM_B_CLK_N<1> (68 11)	MAKE_BASE=TRUE	TP_MEM_B_CLKN<1>
MEM_B_CKE<1> (68 11)	MAKE_BASE=TRUE	NC_MEM_B_CKE<1>
MEM_B_CS_L<1> (68 11)	MAKE_BASE=TRUE	NC_MEM_B_CS_L<1>
MEM_B_ODT<1> (68 11)	MAKE_BASE=TRUE	NC_MEM_B_ODT<1>
MEM_A_A<15> (68 11)	MAKE_BASE=TRUE	TP_MEM_A_A<15>
MEM_B_A<15> (68 11)	MAKE_BASE=TRUE	TP_MEM_B_A<15>

TP_PCH_CLKOUT_DPN	DPLL_REF_CLK_N (MAKE_BASE=TRUE)	DPLL_REF_CLKN (10 67)
TP_PCH_CLKOUT_DPP (16)	DPLL_REF_CLK_P (MAKE_BASE=TRUE)	DPLL_REF_CLKP (10 67)

T29BST:N

R0960 0 5% 1/8W MF-LF 805
=PPVIN_SW_T29BST (36 7) — =PP15V_T29_REG (7 36)

T29_A_BIAS (65 64) — C0960 0.01UF 10% 10V X5R 201

T29_A_BIAS caps

T29_A_BIAS_R (65 8)	R0931 51 5% 1/20W MF 201	T29_A_BIAS_R2DP0 (64)	C0901 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY
T29_A_BIAS_R (65 8)	R0932 51 5% 1/20W MF 201	T29_A_BIAS_R2DN0 (64)	C0902 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY
T29_A_BIAS_R (65 8)	R0933 51 5% 1/20W MF 201	T29_A_BIAS_R2DP1 (64)	C0903 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY
T29_A_BIAS_R (65 8)	R0934 51 5% 1/20W MF 201	T29_A_BIAS_R2DN1 (64)	C0904 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

=PEG_R2D_C_P<3..0> (9)	PEG_R2D_C_P<3..0> (67)	PCIE_T29_R2D_C_P<3..0> (34 70) MAKE_BASE=TRUE
=PEG_R2D_C_N<3..0> (9)	PEG_R2D_C_N<3..0> (67)	PCIE_T29_R2D_C_N<3..0> (34 70) MAKE_BASE=TRUE
=PEG_D2R_P<3..0> (9)	PEG_D2R_P<3..0> (67)	PCIE_T29_D2R_P<3..0> (34 70) MAKE_BASE=TRUE
=PEG_D2R_N<3..0> (9)	PEG_D2R_N<3..0> (67)	PCIE_T29_D2R_N<3..0> (34 70) MAKE_BASE=TRUE

T29 DP Ports

TP_DP_IG_C_HPD (17)	MAKE_BASE=TRUE	DP_T29SNK0_HPD (34)
TP_DP_IG_C_MLP<3..0> (17)	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_P<3..0> (34 72)
TP_DP_IG_C_MLN<3..0> (17)	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_N<3..0> (34 72)
TP_DP_IG_C_AUXP (17)	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_P (34 72)
TP_DP_IG_C_AUXN (17)	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_N (34 72)
TP_DP_IG_D_HPD (17)	MAKE_BASE=TRUE	DP_IG_D_HPD

=PP3V3_S0_DP_DDC (8 7)
R0920 2.2K 5% 1/20W MF 201
R0921 2.2K 5% 1/20W MF 201
R0922 2.2K 5% 1/20W MF 201
R0923 2.2K 5% 1/20W MF 201

TP_DP_IG_C_CTRL_CLK (17)	MAKE_BASE=TRUE	DP_IG_C_CTRL_CLK
TP_DP_IG_C_CTRL_DATA (17)	MAKE_BASE=TRUE	DP_IG_C_CTRL_DATA
TP_DP_IG_D_CTRL_CLK (17)	MAKE_BASE=TRUE	DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA (17)	MAKE_BASE=TRUE	DP_IG_D_CTRL_DATA

R0909 100K 5% 1/20W MF 201

=PP3V3_S0_DP_DDC (8 7)
R0924 2.2K 5% 1/20W MF 201
R0925 2.2K 5% 1/20W MF 201

DP_EXTA_DDC_CLK (64) MAKE_BASE=TRUE	DP_IG_B_DDC_CLK	(17)
DP_EXTA_DDC_DATA (64) MAKE_BASE=TRUE	DP_IG_B_DDC_DATA	(17)
DP_EXTA_HPD (64) MAKE_BASE=TRUE	DP_IG_B_HPD	(17)

R0908 100K 5% 1/20W MF 201
CRITICAL
R0910 0.01 0.5% 1W MF 0612-1
PPBUS_SW_LCDBKLT_PWR (66) MAKE_BASE=TRUE — PPBUS_SW_BKL (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE)
ISNS_LCDBKLT_P (74 46 OUT)
ISNS_LCDBKLT_N (74 46 OUT) — =PPBUS_SW_BKL (66)

NC_USB_HUB1_OCS4 MAKE_BASE=TRUE	=USB_HUB1_OCS4 (24)
NC_USB_HUB2_OCS4 MAKE_BASE=TRUE	=USB_HUB2_OCS4 (24)

T29_A_BIAS caps

T29_A_BIAS_R (65 8) — R0926 51 5% 1/20W MF 201 — T29_A_BIAS_D2RP1 (65)
C0906 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

T29_A_BIAS_R (65 8) — R0927 51 5% 1/20W MF 201 — T29_A_BIAS_D2RN1 (65)
C0907 0.01UF 10% 10V X5R 201 SIGNAL_=EMPTY

DP_A_BIAS caps

DP_A_BIAS_P_2 (64)	C0962 0.01UF 10% 10V X5R 201	DP_A_BIAS_P_0 (64)	C0964 0.01UF 10% 10V X5R 201
DP_A_BIAS_N_2 (64) SIGNAL_MODEL=EMPTY	C0905 0.01UF 10% 10V X5R 201	DP_A_BIAS_N_0 (64) SIGNAL_MODEL=EMPTY	C0908 0.01UF 10% 10V X5R 201

T29 Aliases

Unused USB ports

=PP3V3_S3_USB_HUB (24 7)
R0915 10K 5% 1/20W MF 201 NO STUFF
R0916 10K 5% 1/20W MF 201

T29_A_RSVD_N (69 64)	R0917 0 5% 1/20W MF 201	USB_T29A_N	(24 69)
T29_A_RSVD_P (69 64)	R0918 0 5% 1/20W MF 201	USB_T29A_P	(24 69)

NO STUFF

LVDS Aliases

TP_LVDS_IG_B_CLKP (6) MAKE_BASE=TRUE	LVDS_IG_B_CLK_P	(69)
TP_LVDS_IG_B_CLKN (6) MAKE_BASE=TRUE	LVDS_IG_B_CLK_N	(69)
NC_LVDS_IG_B_DATAP<0..3> MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_B_DATA_P<0..3>	(69)
NC_LVDS_IG_B_DATAN<0..3> MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_B_DATA_N<0..3>	(69)
NC_LVDS_IG_A_DATAP<3> MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_A_DATA_P<3>	(69)
NC_LVDS_IG_A_DATAN<3> MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_A_DATA_N<3>	(69)
LCD_BKLT_PWM (66) MAKE_BASE=TRUE	LVDS_IG_BKL_PWM	(17)
LCD_IG_PWR_EN (63) MAKE_BASE=TRUE	LVDS_IG_PANEL_PWR	(17)
LCD_BKLT_EN (66) MAKE_BASE=TRUE	LVDS_IG_BKL_ON	(17)

SATA Aliases

Unused SATA ODD Signals

SATA_ODD_R2D_C_P (69 16 IN)	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_R2DCP
SATA_ODD_R2D_C_N (69 16 IN)	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_R2DCN
SATA_ODD_D2R_P (69 16 OUT)	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_D2RP
SATA_ODD_D2R_N (69 16 OUT)	MAKE_BASE=TRUE NO_TEST=TRUE	NC_SATA_ODD_D2RN

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE MAKE_BASE=TRUE	P1V5S3RS0_RAMP_DONE	(IN 61)
TP_DDRREG_PGOOD MAKE_BASE=TRUE	DDRREG_PGOOD	(IN 56)

T29 JTAG

JTAG_ISP_TCK (23 19 IN) MAKE_BASE=TRUE	JTAG_T29_TCK_R	JTAG_T29_TCK	(OUT 34)
JTAG_ISP_TDI (19 IN) MAKE_BASE=TRUE	JTAG_T29_TDI		(OUT 34)
JTAG_ISP_TDO (19 OUT) MAKE_BASE=TRUE	JTAG_T29_TDO		(IN 34)

R0990 0 5% 1/20W MF 201

SYNC MASTER=K91_MLB — SYNC DATE=05/15/2010
PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-8870 — SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 9 OF 109
SHEET: 8 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE
CRITICAL

U1000
SANDY-BRIDGE
MOBILE-2C-35W
BGA
(1 OF 9)

DMI

IN	DMI_S2N_N<0>	M2	DMI_RX_0*
IN	DMI_S2N_N<1>	P6	DMI_RX_1*
IN	DMI_S2N_N<2>	P1	DMI_RX_2*
IN	DMI_S2N_N<3>	P10	DMI_RX_3*
IN	DMI_S2N_P<0>	N3	DMI_RX_0
IN	DMI_S2N_P<1>	P7	DMI_RX_1
IN	DMI_S2N_P<2>	P3	DMI_RX_2
IN	DMI_S2N_P<3>	P11	DMI_RX_3
OUT	DMI_N2S_N<0>	K1	DMI_TX_0*
OUT	DMI_N2S_N<1>	M8	DMI_TX_1*
OUT	DMI_N2S_N<2>	N4	DMI_TX_2*
OUT	DMI_N2S_N<3>	R2	DMI_TX_3*
OUT	DMI_N2S_P<0>	K3	DMI_TX_0
OUT	DMI_N2S_P<1>	M7	DMI_TX_1
OUT	DMI_N2S_P<2>	P4	DMI_TX_2
OUT	DMI_N2S_P<3>	T3	DMI_TX_3

INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS

OUT	FDI_DATA_N<0>	U7	FDI0_TX_0*
OUT	FDI_DATA_N<1>	W11	FDI0_TX_1*
OUT	FDI_DATA_N<2>	W1	FDI0_TX_2*
OUT	FDI_DATA_N<3>	AA6	FDI0_TX_3*
OUT	FDI_DATA_N<4>	W6	FDI1_TX_0*
OUT	FDI_DATA_N<5>	V4	FDI1_TX_1*
OUT	FDI_DATA_N<6>	Y2	FDI1_TX_2*
OUT	FDI_DATA_N<7>	AC9	FDI1_TX_3*
OUT	FDI_DATA_P<0>	U6	FDI0_TX_0
OUT	FDI_DATA_P<1>	W10	FDI0_TX_1
OUT	FDI_DATA_P<2>	W3	FDI0_TX_2
OUT	FDI_DATA_P<3>	AA7	FDI0_TX_3
OUT	FDI_DATA_P<4>	W7	FDI1_TX_0
OUT	FDI_DATA_P<5>	T4	FDI1_TX_1
OUT	FDI_DATA_P<6>	AA3	FDI1_TX_2
OUT	FDI_DATA_P<7>	AC8	FDI1_TX_3
IN	FDI_FSYNC<0>	AA11	FDI0_FSYNC
IN	FDI_FSYNC<1>	AC12	FDI1_FSYNC
IN	FDI_INT	U11	FDI_INT
IN	FDI_LSYNC<0>	AA10	FDI0_LSYNC
IN	FDI_LSYNC<1>	AG8	FDI1_LSYNC

=PP1V05_S0_CPU_VCCIO

R1030
24.9
1% 1/20W MF 201
PLACE_NEAR=U1000.AF3:12.7MM

EDP_COMP

PCI EXPRESS BASED INTERFACE SIGNALS

	EDP_ICOMPO	AD2	
	EDP_COMPIO	AF3	
	FIXME: Pin should be EDP_HPD*		
9	EDP_HPD_L	AG11	EDP_HPD
70 63	DP_INT_AUX_CH_N	AG4	EDP_AUX*
70 63	DP_INT_AUX_CH_P	AF4	EDP_AUX
70 63	DP_INT_ML_N<0>	AC3	EDP_TX_0*
70 63	DP_INT_ML_N<1>	AC4	EDP_TX_1*
6	TP_EDP_TX_N<2>	AE11	EDP_TX_2*
6	TP_EDP_TX_N<3>	AE7	EDP_TX_3*
70 63	DP_INT_ML_P<0>	AC1	EDP_TX_0
70 63	DP_INT_ML_P<1>	AA4	EDP_TX_1
6	TP_EDP_TX_P<2>	AE10	EDP_TX_2
6	TP_EDP_TX_P<3>	AE6	EDP_TX_3

EMBEDDED DISPLAY PORT SIGNALS

Intel Doc 438297 Huron River SFF DG rev1.0 section 2.2.1 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if Internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

R1010
24.9
1% 1/20W MF 201
PLACE_NEAR=U1000.G3:12.7MM

67 CPU_PEG_COMP — =PP1V05_S0_CPU_VCCIO 7 9 10 12 14

	PEG_ICOMPI	G3	
	PEG_ICOMPO	G1	
	PEG_RCOMPO	G4	
IN	PEG_RX_0*	H22	=PEG_D2R_N<0>
IN	PEG_RX_1*	J21	=PEG_D2R_N<1>
IN	PEG_RX_2*	B22	=PEG_D2R_N<2>
IN	PEG_RX_3*	D21	=PEG_D2R_N<3>
IN	PEG_RX_4*	A19	=PEG_D2R_N<4>
IN	PEG_RX_5*	D17	=PEG_D2R_N<5>
IN	PEG_RX_6*	B14	=PEG_D2R_N<6>
IN	PEG_RX_7*	D13	=PEG_D2R_N<7>
IN	PEG_RX_8*	A11	=PEG_D2R_N<8>
IN	PEG_RX_9*	B10	=PEG_D2R_N<9>
IN	PEG_RX_10*	G8	=PEG_D2R_N<10>
IN	PEG_RX_11*	A8	=PEG_D2R_N<11>
IN	PEG_RX_12*	B6	=PEG_D2R_N<12>
IN	PEG_RX_13*	H8	=PEG_D2R_N<13>
IN	PEG_RX_14*	E5	=PEG_D2R_N<14>
IN	PEG_RX_15*	K7	=PEG_D2R_N<15>
IN	PEG_RX_0	K22	=PEG_D2R_P<0>
IN	PEG_RX_1	K19	=PEG_D2R_P<1>
IN	PEG_RX_2	C21	=PEG_D2R_P<2>
IN	PEG_RX_3	D19	=PEG_D2R_P<3>
IN	PEG_RX_4	C19	=PEG_D2R_P<4>
IN	PEG_RX_5	D16	=PEG_D2R_P<5>
IN	PEG_RX_6	C13	=PEG_D2R_P<6>
IN	PEG_RX_7	D12	=PEG_D2R_P<7>
IN	PEG_RX_8	C11	=PEG_D2R_P<8>
IN	PEG_RX_9	C9	=PEG_D2R_P<9>
IN	PEG_RX_10	F8	=PEG_D2R_P<10>
IN	PEG_RX_11	C8	=PEG_D2R_P<11>
IN	PEG_RX_12	C5	=PEG_D2R_P<12>
IN	PEG_RX_13	H6	=PEG_D2R_P<13>
IN	PEG_RX_14	F6	=PEG_D2R_P<14>
IN	PEG_RX_15	K6	=PEG_D2R_P<15>
OUT	PEG_TX_0*	G22	=PEG_R2D_C_N<0>
OUT	PEG_TX_1*	C23	=PEG_R2D_C_N<1>
OUT	PEG_TX_2*	D23	=PEG_R2D_C_N<2>
OUT	PEG_TX_3*	F21	=PEG_R2D_C_N<3>
OUT	PEG_TX_4*	H19	=PEG_R2D_C_N<4>
OUT	PEG_TX_5*	C17	=PEG_R2D_C_N<5>
OUT	PEG_TX_6*	K15	=PEG_R2D_C_N<6>
OUT	PEG_TX_7*	F17	=PEG_R2D_C_N<7>
OUT	PEG_TX_8*	F14	=PEG_R2D_C_N<8>
OUT	PEG_TX_9*	A15	=PEG_R2D_C_N<9>
OUT	PEG_TX_10*	J14	=PEG_R2D_C_N<10>
OUT	PEG_TX_11*	H13	=PEG_R2D_C_N<11>
OUT	PEG_TX_12*	M10	=PEG_R2D_C_N<12>
OUT	PEG_TX_13*	F10	=PEG_R2D_C_N<13>
OUT	PEG_TX_14*	D9	=PEG_R2D_C_N<14>
OUT	PEG_TX_15*	J4	=PEG_R2D_C_N<15>
OUT	PEG_TX_0	F22	=PEG_R2D_C_P<0>
OUT	PEG_TX_1	A23	=PEG_R2D_C_P<1>
OUT	PEG_TX_2	D24	=PEG_R2D_C_P<2>
OUT	PEG_TX_3	E21	=PEG_R2D_C_P<3>
OUT	PEG_TX_4	G19	=PEG_R2D_C_P<4>
OUT	PEG_TX_5	B18	=PEG_R2D_C_P<5>
OUT	PEG_TX_6	K17	=PEG_R2D_C_P<6>
OUT	PEG_TX_7	G17	=PEG_R2D_C_P<7>
OUT	PEG_TX_8	E14	=PEG_R2D_C_P<8>
OUT	PEG_TX_9	C15	=PEG_R2D_C_P<9>
OUT	PEG_TX_10	K13	=PEG_R2D_C_P<10>
OUT	PEG_TX_11	G13	=PEG_R2D_C_P<11>
OUT	PEG_TX_12	K10	=PEG_R2D_C_P<12>
OUT	PEG_TX_13	G10	=PEG_R2D_C_P<13>
OUT	PEG_TX_14	D8	=PEG_R2D_C_P<14>
OUT	PEG_TX_15	K4	=PEG_R2D_C_P<15>

=PPVCORE_S0_CPU 7 12 14
=PPVCORE_S0_CPU_VCCAXG 7 12 15 23 67

R1064 NOSTUFF 49.9 1% 1/20W MF 201
R1070 NOSTUFF 49.9 1% 1/20W MF 201
PLACE_NEAR=U1000.H45:50.8MM
PLACE_SIDE=BOTTOM

CPU_VCC_VALSENSE_P — Note. VOLTAGE=1.25V
CPU_VCC_VALSENSE_N — Note. VOLTAGE=0V
CPU_AXG_VALSENSE_P — Note. VOLTAGE=1.05V
CPU_AXG_VALSENSE_N — Note. VOLTAGE=0V

R1065 NOSTUFF 49.9 1% 1/20W MF 201
R1071 NOSTUFF 49.9 1% 1/20W MF 201
PLACE_NEAR=U1000.K45:50.8MM
PLACE_SIDE=BOTTOM
PLACE_NEAR=U1000.K43:50.8MM
PLACE_SIDE=BOTTOM

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.

OMIT_TABLE
CRITICAL

U1000
BGA
(5 OF 9)
RESERVED
SANDY-BRIDGE
MOBILE-2C-35W

67 23 9 IN	CPU_CFG<0>	B50	CFG_0
67 23 9 IN	CPU_CFG<1>	C51	CFG_1
67 23 9 IN	CPU_CFG<2>	B54	CFG_2
67 23 9 IN	CPU_CFG<3>	D53	CFG_3
67 23 9 IN	CPU_CFG<4>	A51	CFG_4
67 23 9 IN	CPU_CFG<5>	C53	CFG_5
67 23 9 IN	CPU_CFG<6>	C55	CFG_6
67 23 9 IN	CPU_CFG<7>	H49	CFG_7
67 23 9 IN	CPU_CFG<8>	A55	CFG_8
67 23 IN	CPU_CFG<9>	H51	CFG_9
67 23 IN	CPU_CFG<10>	K49	CFG_10
67 23 IN	CPU_CFG<11>	K53	CFG_11
67 23 IN	CPU_CFG<12>	F53	CFG_12
67 23 IN	CPU_CFG<13>	G53	CFG_13
67 23 IN	CPU_CFG<14>	L51	CFG_14
67 23 IN	CPU_CFG<15>	F51	CFG_15
23 9 IN	CPU_CFG<16>	D52	CFG_16
23 IN	CPU_CFG<17>	L53	CFG_17

	CPU_VCC_VALSENSE_P	H43	VCC_VAL_SENSE
	CPU_VCC_VALSENSE_N	K43	VSS_VAL_SENSE
	CPU_AXG_VALSENSE_P	H45	VAXG_VAL_SENSE
	CPU_AXG_VALSENSE_N	K45	VSSAXG_VAL_SENSE
	TP_CPU_VCC_DIE_SENSE	F48	VCC_DIE_SENSE
74 47 OUT	CPU_THERMD_P	H48	RSVD_6
74 47 OUT	CPU_THERMD_N	K48	RSVD_7
NCX		BA19	RSVD_8
NCX		AY19	RSVD_9
NCX		BA21	RSVD_10
NCX		AY21	RSVD_11
NCX		BA19	RSVD_12
NCX		AY21	RSVD_13
NCX		BA22	RSVD_14
NCX		AY22	RSVD_15
NCX		BA25	RSVD_16
NCX		AY21	RSVD_17
NCX		BA21	RSVD_18
NCX		BA22	RSVD_19
NCX		BA25	RSVD_20
NCX		BA26	RSVD_21
NCX		BA22	RSVD_22
NCX		BE22	RSVD_23
NCX		BA26	RSVD_24
NCX		BA26	RSVD_25
NCX		BE23	RSVD_26
NCX		BE24	RSVD_27

		BE7	CPU_MEM_VREFDQ_A 9
	RSVD_29	BG7	NC
	RSVD_30	N42	NC
	RSVD_31	L42	NC
	RSVD_32	L43	NC
	RSVD_33	L45	NC
	RSVD_34	M13	NC
	RSVD_35	M14	NC
	RSVD_36	U14	NC
	RSVD_37	W14	NC
	RSVD_38	P13	NC
	RSVD_39	AT49	NC
	RSVD_40	K23	NC
	RSVD_41	AH2	NC
	RSVD_42	AG13	NC
	RSVD_43	AM2	NC
	RSVD_44	AM15	NC
	RSVD_45	N50	NC

	DC_TEST_A4	A4	TP_CPU_DC_TEST_A4
	DC_TEST_C4	C4	CPU_DC_TEST_C4_D3
	DC_TEST_D3	D3	
	DC_TEST_D1	D1	TP_CPU_DC_TEST_D1
	DC_TEST_A58	A58	TP_CPU_DC_TEST_A58
	DC_TEST_A59	A59	CPU_DC_TEST_C59_A59
	DC_TEST_C59	C59	
	DC_TEST_A61	A61	CPU_DC_TEST_C61_A61
	DC_TEST_C61	C61	
	DC_TEST_D61	D61	TP_CPU_DC_TEST_D61
	DC_TEST_BD61	BD61	TP_CPU_DC_TEST_BD61
	DC_TEST_BE61	BE61	CPU_DC_TEST_BE59_BE61
	DC_TEST_BE59	BE59	
	DC_TEST_BG61	BG61	CPU_DC_TEST_BG59_BG61
	DC_TEST_BG59	BG59	
	DC_TEST_BG58	BG58	TP_CPU_DC_TEST_BG58
	DC_TEST_BG4	BG4	TP_CPU_DC_TEST_BG4
	DC_TEST_BG3	BG3	CPU_DC_TEST_C4_BE3_BG3
	DC_TEST_BE3	BE3	
	DC_TEST_BG1	BG1	CPU_DC_TEST_C4_BE1_BG1
	DC_TEST_BE1	BE1	
	DC_TEST_BD1	BD1	TP_CPU_DC_TEST_BD1

NOTE: Intel is investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls BE7 and BG7 for Sandy Bridge 2-core to SO-DIMM connectors directly. FETs are needed in order to avoid potential leakage while system is in S3 state.

68 31 30 29 28 27 PP0V75_S3_MEM_VREFDQ_A — R1021 NOSTUFF 0 5% 1/20W MF 201 — CPU_MEM_VREFDQ_A 9
R1020 NOSTUFF 1K 1% 1/20W MF 201

67 23 9 CPU_CFG<7>
67 23 9 CPU_CFG<6>
67 23 9 CPU_CFG<5>
67 23 9 CPU_CFG<4>
67 23 9 CPU_CFG<2>

R1042 NOSTUFF, R1044 EDP, R1045 NOSTUFF, R1046 NOSTUFF, R1047 NOSTUFF — 1K 1% 1/16W MF-LF 402

23 9 CPU_CFG<16>
67 23 9 CPU_CFG<3>
67 23 9 CPU_CFG<1>
67 23 9 CPU_CFG<0>

R1040 NOSTUFF, R1041 NOSTUFF, R1043 NOSTUFF, R1049 NOSTUFF — 1K 1% 1/16W MF-LF 402

These can be Placed close to J2500 and Only for debug access

14 12 10 9 7 =PP1V05_S0_CPU_VCCIO
PLACE_NEAR=U1000.AG11:12.7MM
R1031 1K 5% 1/20W MF 201
EDP_HPD_L 9

Q1031
SSM3K15FV
SOD-VESM-HF
D 3, G 1, S 2

63 DP_INT_HPD

FOR SANDYBRIDGE PROCESSOR

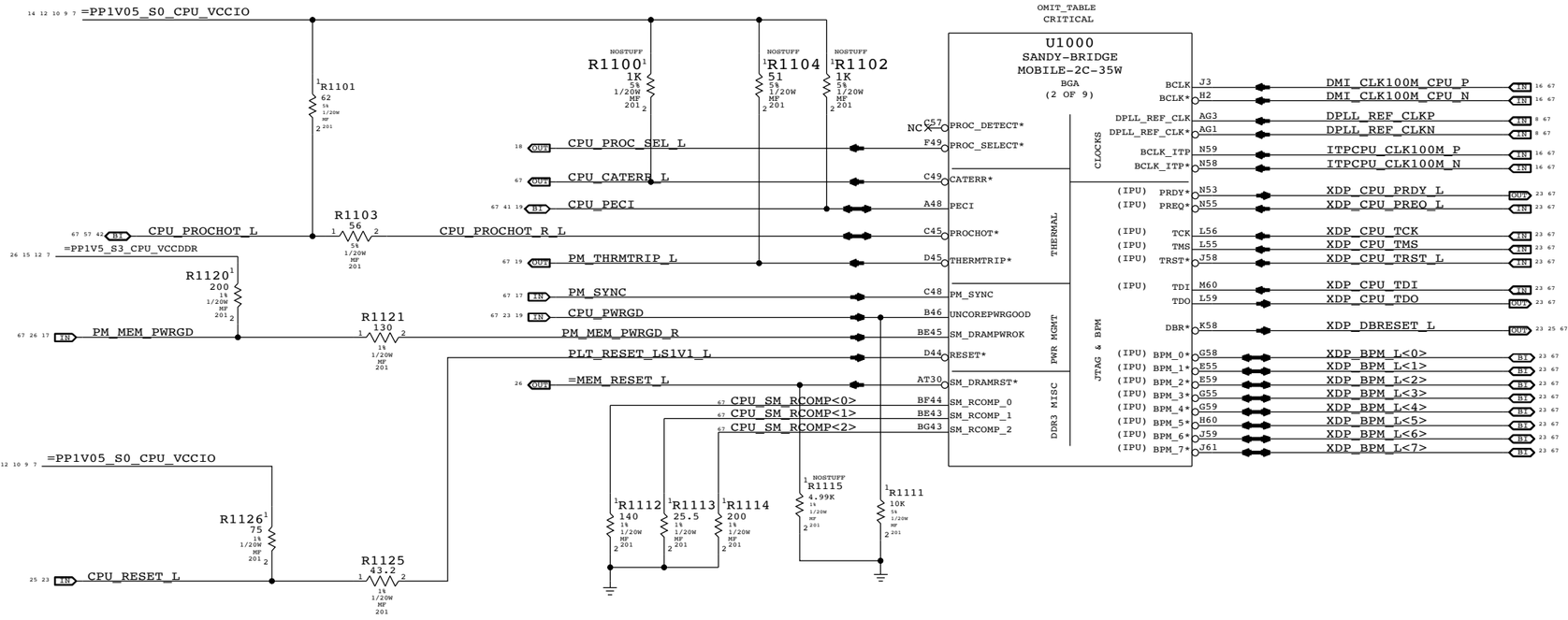
CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT)	10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 10 OF 109
SHEET 9 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER 051-8870 | SIZE D
REVISION 3.13.0
BRANCH
PAGE 11 OF 109
SHEET 10 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE
CRITICAL

U1000
BGA
(3 OF 9)
SANDY-BRIDGE
MOBILE-2C-35W

MEMORY CHANNEL A

MEM_A_DQ<0>	AG6	SA_DQ_0	
MEM_A_DQ<1>	AJ6	SA_DQ_1	
MEM_A_DQ<2>	AP11	SA_DQ_2	
MEM_A_DQ<3>	AL6	SA_DQ_3	
MEM_A_DQ<4>	AJ10	SA_DQ_4	
MEM_A_DQ<5>	AJ8	SA_DQ_5	
MEM_A_DQ<6>	AL8	SA_DQ_6	
MEM_A_DQ<7>	AL7	SA_DQ_7	
MEM_A_DQ<8>	AR11	SA_DQ_8	
MEM_A_DQ<9>	AP6	SA_DQ_9	
MEM_A_DQ<10>	AU6	SA_DQ_10	
MEM_A_DQ<11>	AV9	SA_DQ_11	
MEM_A_DQ<12>	AR6	SA_DQ_12	
MEM_A_DQ<13>	AP8	SA_DQ_13	
MEM_A_DQ<14>	AT13	SA_DQ_14	
MEM_A_DQ<15>	AU13	SA_DQ_15	
MEM_A_DQ<16>	BC7	SA_DQ_16	
MEM_A_DQ<17>	BB7	SA_DQ_17	
MEM_A_DQ<18>	BA13	SA_DQ_18	
MEM_A_DQ<19>	BB11	SA_DQ_19	
MEM_A_DQ<20>	BA7	SA_DQ_20	
MEM_A_DQ<21>	BA9	SA_DQ_21	
MEM_A_DQ<22>	BB9	SA_DQ_22	
MEM_A_DQ<23>	AY13	SA_DQ_23	
MEM_A_DQ<24>	AV14	SA_DQ_24	
MEM_A_DQ<25>	AR14	SA_DQ_25	
MEM_A_DQ<26>	AY17	SA_DQ_26	
MEM_A_DQ<27>	AR19	SA_DQ_27	
MEM_A_DQ<28>	BA14	SA_DQ_28	
MEM_A_DQ<29>	AU14	SA_DQ_29	
MEM_A_DQ<30>	BB14	SA_DQ_30	
MEM_A_DQ<31>	BB17	SA_DQ_31	
MEM_A_DQ<32>	BA45	SA_DQ_32	
MEM_A_DQ<33>	AR43	SA_DQ_33	
MEM_A_DQ<34>	AW48	SA_DQ_34	
MEM_A_DQ<35>	BC48	SA_DQ_35	
MEM_A_DQ<36>	BC45	SA_DQ_36	
MEM_A_DQ<37>	AR45	SA_DQ_37	
MEM_A_DQ<38>	AT48	SA_DQ_38	
MEM_A_DQ<39>	AY48	SA_DQ_39	
MEM_A_DQ<40>	BA49	SA_DQ_40	
MEM_A_DQ<41>	AV49	SA_DQ_41	
MEM_A_DQ<42>	BB51	SA_DQ_42	
MEM_A_DQ<43>	AY53	SA_DQ_43	
MEM_A_DQ<44>	BB49	SA_DQ_44	
MEM_A_DQ<45>	AU49	SA_DQ_45	
MEM_A_DQ<46>	BA53	SA_DQ_46	
MEM_A_DQ<47>	BB55	SA_DQ_47	
MEM_A_DQ<48>	BA55	SA_DQ_48	
MEM_A_DQ<49>	AV56	SA_DQ_49	
MEM_A_DQ<50>	AP50	SA_DQ_50	
MEM_A_DQ<51>	AP53	SA_DQ_51	
MEM_A_DQ<52>	AV54	SA_DQ_52	
MEM_A_DQ<53>	AT54	SA_DQ_53	
MEM_A_DQ<54>	AP56	SA_DQ_54	
MEM_A_DQ<55>	AP52	SA_DQ_55	
MEM_A_DQ<56>	AN57	SA_DQ_56	
MEM_A_DQ<57>	AN53	SA_DQ_57	
MEM_A_DQ<58>	AG56	SA_DQ_58	
MEM_A_DQ<59>	AG53	SA_DQ_59	
MEM_A_DQ<60>	AN55	SA_DQ_60	
MEM_A_DQ<61>	AN52	SA_DQ_61	
MEM_A_DQ<62>	AG55	SA_DQ_62	
MEM_A_DQ<63>	AK56	SA_DQ_63	
MEM_A_BA<0>	BD37	SA_BS_0	
MEM_A_BA<1>	BF36	SA_BS_1	
MEM_A_BA<2>	BA28	SA_BS_2	
MEM_A_CAS_L	BE39	SA_CAS*	
MEM_A_RAS_L	BD39	SA_RAS*	
MEM_A_WE_L	AT41	SA_WE*	

SA_CK_0	AU36	MEM_A_CLK_P<0>	OUT
SA_CK_0*	AV36	MEM_A_CLK_N<0>	OUT
SA_CKE_0	AY26	MEM_A_CKE<0>	OUT
SA_CK_1	AT40	MEM_A_CLK_P<1>	OUT
SA_CK_1*	AU40	MEM_A_CLK_N<1>	OUT
SA_CKE_1	BB26	MEM_A_CKE<1>	OUT
SA_CS_0*	BB40	MEM_A_CS_L<0>	OUT
SA_CS_1*	BC41	MEM_A_CS_L<1>	OUT
SA_ODT_0	AY40	MEM_A_ODT<0>	OUT
SA_ODT_1	BA41	MEM_A_ODT<1>	OUT
SA_DQS_0*	AL11	MEM_A_DQS_N<0>	BI
SA_DQS_1*	AR8	MEM_A_DQS_N<1>	BI
SA_DQS_2*	AV11	MEM_A_DQS_N<2>	BI
SA_DQS_3*	AT17	MEM_A_DQS_N<3>	BI
SA_DQS_4*	AV45	MEM_A_DQS_N<4>	BI
SA_DQS_5*	AY51	MEM_A_DQS_N<5>	BI
SA_DQS_6*	AT55	MEM_A_DQS_N<6>	BI
SA_DQS_7*	AK55	MEM_A_DQS_N<7>	BI
SA_DQS_0	AJ11	MEM_A_DQS_P<0>	BI
SA_DQS_1	AR10	MEM_A_DQS_P<1>	BI
SA_DQS_2	AY11	MEM_A_DQS_P<2>	BI
SA_DQS_3	AU17	MEM_A_DQS_P<3>	BI
SA_DQS_4	AW45	MEM_A_DQS_P<4>	BI
SA_DQS_5	AV51	MEM_A_DQS_P<5>	BI
SA_DQS_6	AT56	MEM_A_DQS_P<6>	BI
SA_DQS_7	AK54	MEM_A_DQS_P<7>	BI
SA_MA_0	BG35	MEM_A_A<0>	OUT
SA_MA_1	BB34	MEM_A_A<1>	OUT
SA_MA_2	BE35	MEM_A_A<2>	OUT
SA_MA_3	BD35	MEM_A_A<3>	OUT
SA_MA_4	AT34	MEM_A_A<4>	OUT
SA_MA_5	AU34	MEM_A_A<5>	OUT
SA_MA_6	BB32	MEM_A_A<6>	OUT
SA_MA_7	AT32	MEM_A_A<7>	OUT
SA_MA_8	AY32	MEM_A_A<8>	OUT
SA_MA_9	AV32	MEM_A_A<9>	OUT
SA_MA_10	BE37	MEM_A_A<10>	OUT
SA_MA_11	BA30	MEM_A_A<11>	OUT
SA_MA_12	BC30	MEM_A_A<12>	OUT
SA_MA_13	AW41	MEM_A_A<13>	OUT
SA_MA_14	AY28	MEM_A_A<14>	OUT
SA_MA_15	AU26	MEM_A_A<15>	OUT

OMIT_TABLE
CRITICAL

U1000
BGA
(4 OF 9)
SANDY-BRIDGE
MOBILE-2C-35W

MEMORY CHANNEL B

MEM_B_DQ<0>	AL4	SB_DQ_0	
MEM_B_DQ<1>	AL1	SB_DQ_1	
MEM_B_DQ<2>	AN3	SB_DQ_2	
MEM_B_DQ<3>	AR4	SB_DQ_3	
MEM_B_DQ<4>	AK4	SB_DQ_4	
MEM_B_DQ<5>	AK3	SB_DQ_5	
MEM_B_DQ<6>	AN4	SB_DQ_6	
MEM_B_DQ<7>	AR1	SB_DQ_7	
MEM_B_DQ<8>	AU4	SB_DQ_8	
MEM_B_DQ<9>	AT2	SB_DQ_9	
MEM_B_DQ<10>	AV4	SB_DQ_10	
MEM_B_DQ<11>	BA4	SB_DQ_11	
MEM_B_DQ<12>	AU3	SB_DQ_12	
MEM_B_DQ<13>	AR3	SB_DQ_13	
MEM_B_DQ<14>	AY2	SB_DQ_14	
MEM_B_DQ<15>	BA3	SB_DQ_15	
MEM_B_DQ<16>	BE9	SB_DQ_16	
MEM_B_DQ<17>	BD9	SB_DQ_17	
MEM_B_DQ<18>	BD13	SB_DQ_18	
MEM_B_DQ<19>	BF12	SB_DQ_19	
MEM_B_DQ<20>	BF8	SB_DQ_20	
MEM_B_DQ<21>	BD10	SB_DQ_21	
MEM_B_DQ<22>	BD14	SB_DQ_22	
MEM_B_DQ<23>	BE13	SB_DQ_23	
MEM_B_DQ<24>	BF16	SB_DQ_24	
MEM_B_DQ<25>	BE17	SB_DQ_25	
MEM_B_DQ<26>	BE18	SB_DQ_26	
MEM_B_DQ<27>	BE21	SB_DQ_27	
MEM_B_DQ<28>	BE14	SB_DQ_28	
MEM_B_DQ<29>	BG14	SB_DQ_29	
MEM_B_DQ<30>	BG18	SB_DQ_30	
MEM_B_DQ<31>	BF19	SB_DQ_31	
MEM_B_DQ<32>	BD50	SB_DQ_32	
MEM_B_DQ<33>	BF48	SB_DQ_33	
MEM_B_DQ<34>	BD53	SB_DQ_34	
MEM_B_DQ<35>	BF52	SB_DQ_35	
MEM_B_DQ<36>	BD49	SB_DQ_36	
MEM_B_DQ<37>	BE49	SB_DQ_37	
MEM_B_DQ<38>	BD54	SB_DQ_38	
MEM_B_DQ<39>	BE53	SB_DQ_39	
MEM_B_DQ<40>	BF56	SB_DQ_40	
MEM_B_DQ<41>	BE57	SB_DQ_41	
MEM_B_DQ<42>	BC59	SB_DQ_42	
MEM_B_DQ<43>	AY60	SB_DQ_43	
MEM_B_DQ<44>	BE54	SB_DQ_44	
MEM_B_DQ<45>	BG54	SB_DQ_45	
MEM_B_DQ<46>	BA58	SB_DQ_46	
MEM_B_DQ<47>	AW59	SB_DQ_47	
MEM_B_DQ<48>	AW58	SB_DQ_48	
MEM_B_DQ<49>	AU58	SB_DQ_49	
MEM_B_DQ<50>	AN61	SB_DQ_50	
MEM_B_DQ<51>	AN59	SB_DQ_51	
MEM_B_DQ<52>	AU59	SB_DQ_52	
MEM_B_DQ<53>	AU61	SB_DQ_53	
MEM_B_DQ<54>	AN58	SB_DQ_54	
MEM_B_DQ<55>	AR58	SB_DQ_55	
MEM_B_DQ<56>	AK58	SB_DQ_56	
MEM_B_DQ<57>	AL58	SB_DQ_57	
MEM_B_DQ<58>	AG58	SB_DQ_58	
MEM_B_DQ<59>	AG59	SB_DQ_59	
MEM_B_DQ<60>	AM60	SB_DQ_60	
MEM_B_DQ<61>	AL59	SB_DQ_61	
MEM_B_DQ<62>	AF61	SB_DQ_62	
MEM_B_DQ<63>	AH60	SB_DQ_63	
MEM_B_BA<0>	BG39	SB_BS_0	
MEM_B_BA<1>	BD42	SB_BS_1	
MEM_B_BA<2>	AT22	SB_BS_2	
MEM_B_CAS_L	AV43	SB_CAS*	
MEM_B_RAS_L	BF40	SB_RAS*	
MEM_B_WE_L	BD45	SB_WE*	

SB_CK_0	BA34	MEM_B_CLK_P<0>	OUT
SB_CK_0*	AY34	MEM_B_CLK_N<0>	OUT
SB_CKE_0	AR22	MEM_B_CKE<0>	OUT
SB_CK_1	BA36	MEM_B_CLK_P<1>	OUT
SB_CK_1*	BB36	MEM_B_CLK_N<1>	OUT
SB_CKE_1	BF27	MEM_B_CKE<1>	OUT
SB_CS_0*	BE41	MEM_B_CS_L<0>	OUT
SB_CS_1*	BE47	MEM_B_CS_L<1>	OUT
SB_ODT_0	AT43	MEM_B_ODT<0>	OUT
SB_ODT_1	BG47	MEM_B_ODT<1>	OUT
SB_DQS_0*	AL3	MEM_B_DQS_N<0>	BI
SB_DQS_1*	AV3	MEM_B_DQS_N<1>	BI
SB_DQS_2*	BG11	MEM_B_DQS_N<2>	BI
SB_DQS_3*	BD17	MEM_B_DQS_N<3>	BI
SB_DQS_4*	BG51	MEM_B_DQS_N<4>	BI
SB_DQS_5*	BA59	MEM_B_DQS_N<5>	BI
SB_DQS_6*	AT60	MEM_B_DQS_N<6>	BI
SB_DQS_7*	AK59	MEM_B_DQS_N<7>	BI
SB_DQS_0	AM2	MEM_B_DQS_P<0>	BI
SB_DQS_1	AV1	MEM_B_DQS_P<1>	BI
SB_DQS_2	BE11	MEM_B_DQS_P<2>	BI
SB_DQS_3	BD18	MEM_B_DQS_P<3>	BI
SB_DQS_4	BE51	MEM_B_DQS_P<4>	BI
SB_DQS_5	BA61	MEM_B_DQS_P<5>	BI
SB_DQS_6	AR59	MEM_B_DQS_P<6>	BI
SB_DQS_7	AK61	MEM_B_DQS_P<7>	BI
SB_MA_0	BF32	MEM_B_A<0>	OUT
SB_MA_1	BE33	MEM_B_A<1>	OUT
SB_MA_2	BD33	MEM_B_A<2>	OUT
SB_MA_3	AU30	MEM_B_A<3>	OUT
SB_MA_4	BD30	MEM_B_A<4>	OUT
SB_MA_5	AV30	MEM_B_A<5>	OUT
SB_MA_6	BG30	MEM_B_A<6>	OUT
SB_MA_7	BD29	MEM_B_A<7>	OUT
SB_MA_8	BE30	MEM_B_A<8>	OUT
SB_MA_9	BE28	MEM_B_A<9>	OUT
SB_MA_10	BD43	MEM_B_A<10>	OUT
SB_MA_11	AT28	MEM_B_A<11>	OUT
SB_MA_12	AV28	MEM_B_A<12>	OUT
SB_MA_13	BD46	MEM_B_A<13>	OUT
SB_MA_14	AT26	MEM_B_A<14>	OUT
SB_MA_15	AU22	MEM_B_A<15>	OUT

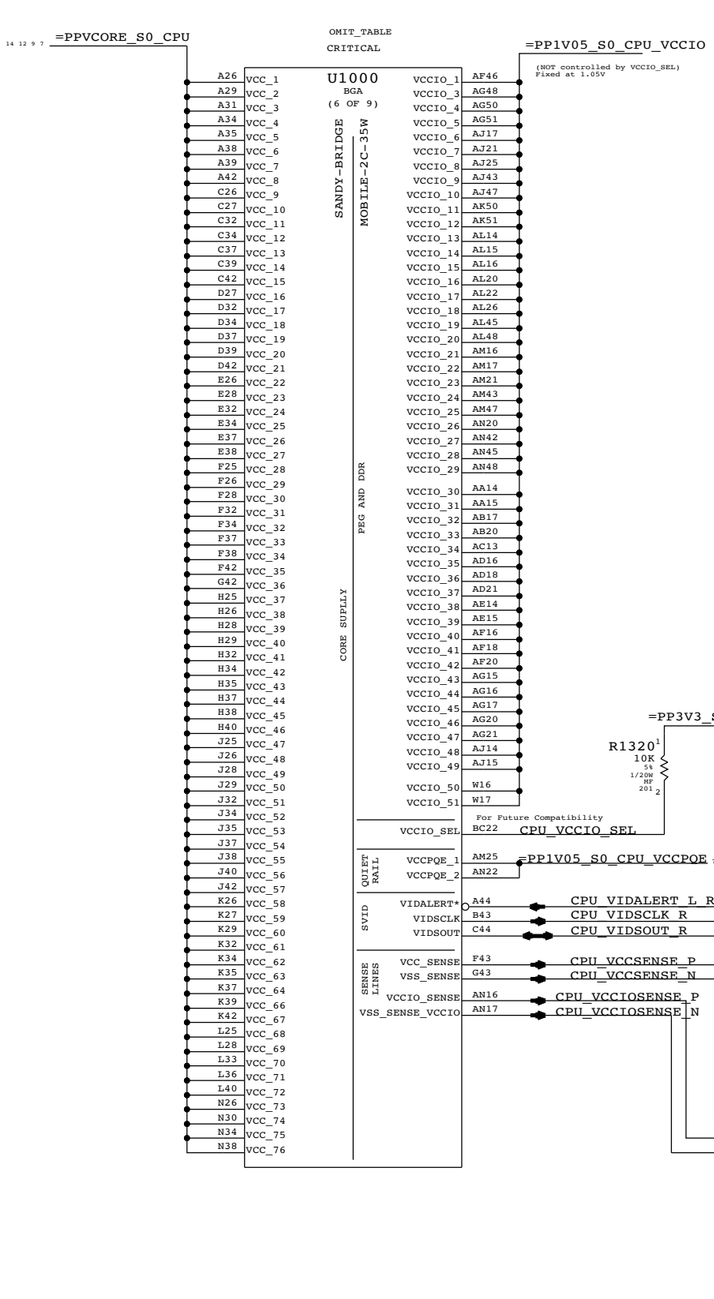
SYNC DATE=01/10/2011

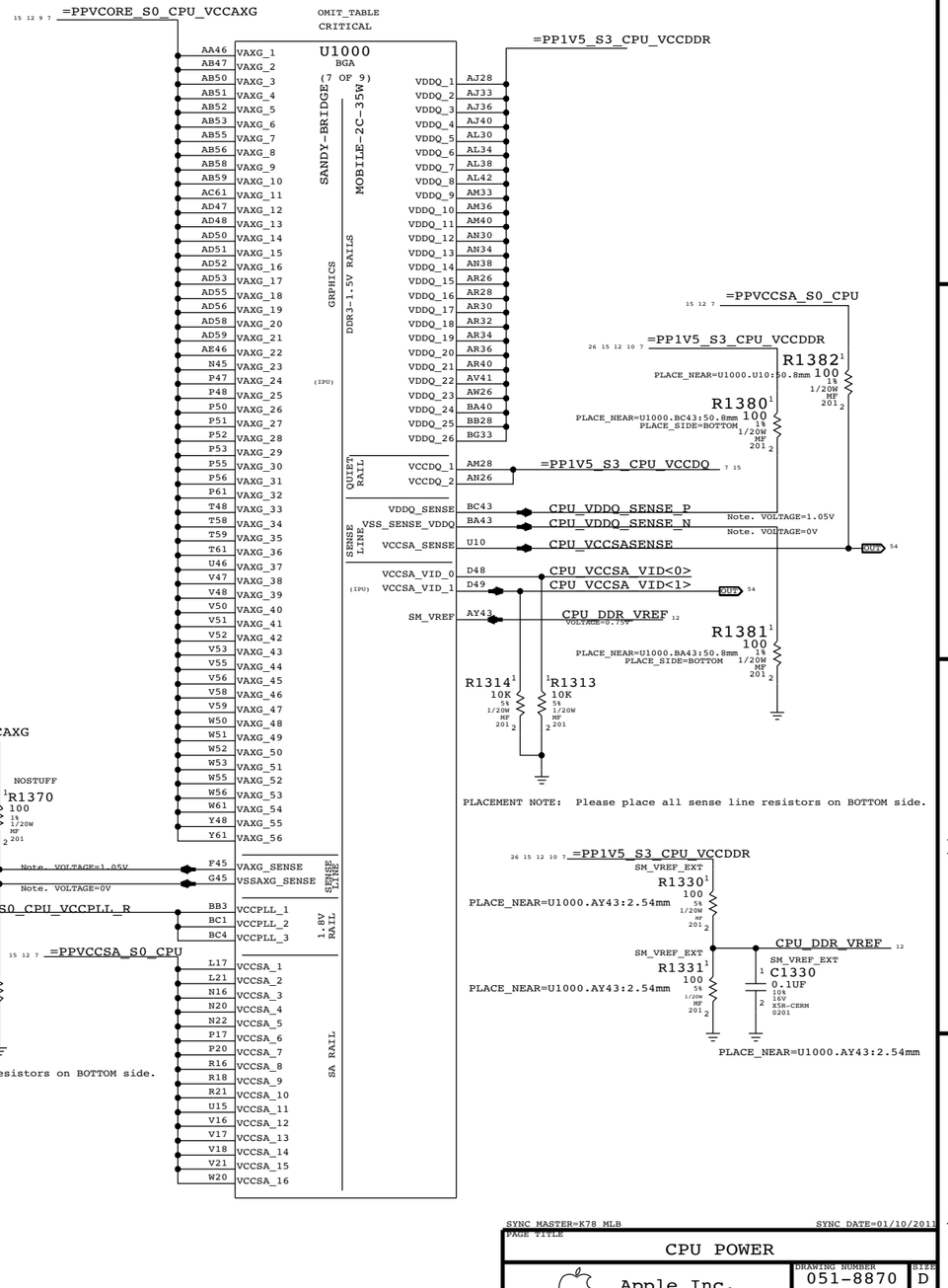
PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 12 OF 109
SHEET 11 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





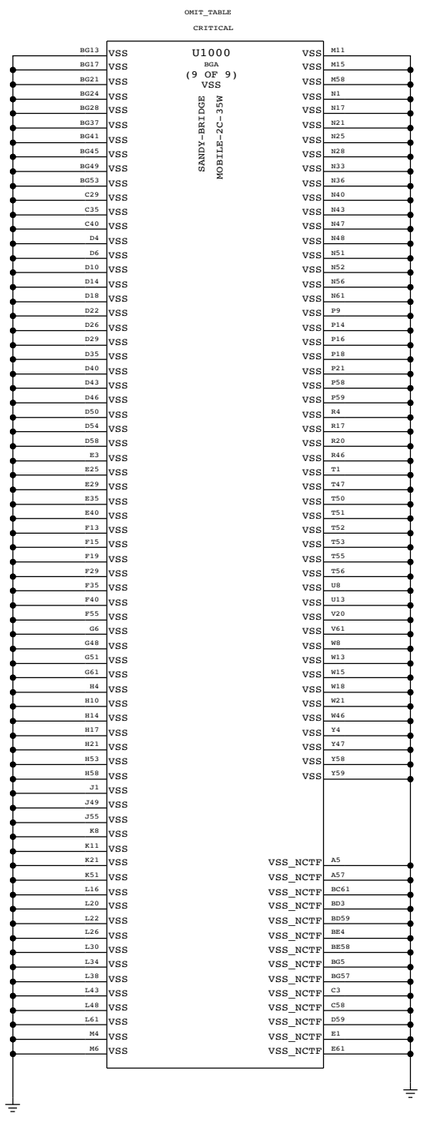
SYNC MASTER=K78 MLB
SYNC DATE=01/10/2011

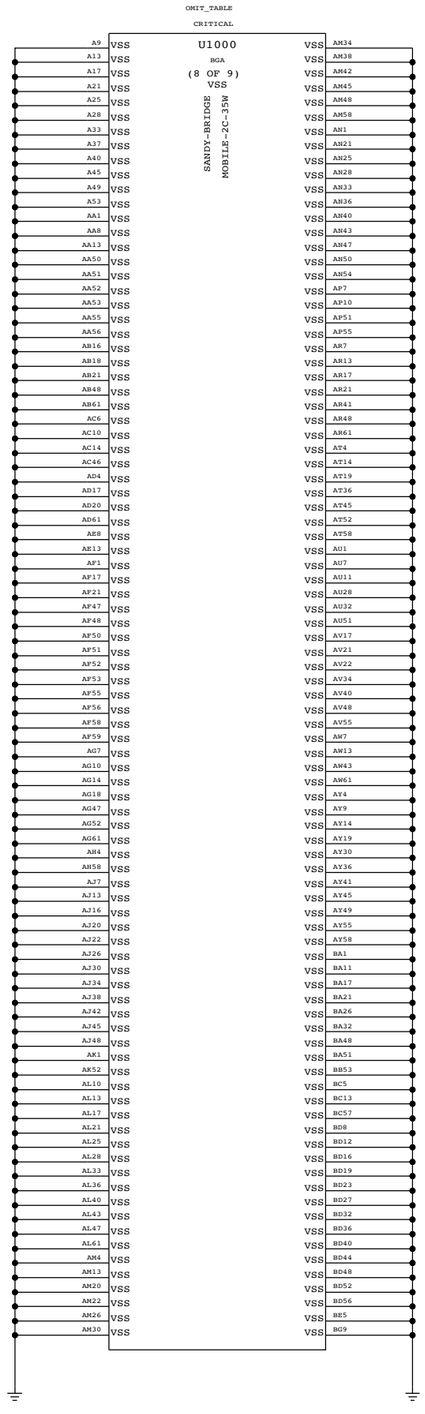
PAGE TITLE
CPU POWER

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 13 OF 109
SHEET 12 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





PAGE TITLE	CPU GROUNDS
	Apple Inc.
DRAWING NUMBER	051-8870
SIZE	D
REVISION	3.13.0
BRANCH	
PAGE	14 OF 109
SHEET	13 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Processor Load Line : -2.9 mOhms

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU

CRITICAL C1600 2.2UF 20% 4V X5R 402 | C1601 2.2UF | C1602 2.2UF | C1603 2.2UF | C1604 2.2UF | C1605 2.2UF | C1606 2.2UF | C1607 2.2UF | C1608 2.2UF | C1609 2.2UF | C1610 2.2UF | C1611 2.2UF | C1612 2.2UF | C1613 2.2UF | C1614 2.2UF | C1615 2.2UF

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1655 22UF 20% 4V X5R 402 | C1656 22UF | C1657 22UF | C1658 22UF | C1659 22UF | C1660 22UF | C1661 22UF | C1662 22UF | C1663 22UF | C1664 22UF | C1665 22UF | C1666 22UF

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 270UF 20% 2V TANT CASE-B2-SM | C1681 270UF | C1682 270UF | C1683 270UF | C1679 270UF

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1684 1UF 10% 10V X5R 402 | C1685 1UF | C1686 1UF | C1687 1UF | C1688 1UF | C1689 1UF | C1690 1UF | C1691 1UF | C1692 1UF | C1693 1UF | C1694 1UF | C1695 1UF | C1696 1UF

C1697 1UF 10% 10V X5R 402 | C1698 1UF | C1699 1UF | C169A 1UF | C169B 1UF | C169C 1UF | C169D 1UF | C169E 1UF | C169F 1UF | C161A 1UF | C161B 1UF | C161C 1UF | C161D 1UF

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM-X5R 0402-1 | C161F 10UF | C162A 10UF | C162B 10UF | C162C 10UF | C162D 10UF | C162E 10UF | C167A 10UF | C167B 10UF | C167C 10UF

C167D 270UF 20% 2V TANT CASE-B2-SM | C167E 270UF | C167G 270UF | C167H 270UF

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603 =PP1V05_S0_CPU_VCCPQE 7 12

C167F 1UF 10% 10V X5R 402 Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL

R1600 0 5% 1/16W MF-LF 402 =PP1V8_S0_CPU_VCCPLL_R 7 12

C160X 1UF 10% 10V X5R 402 | C160Y 1UF | C160Z 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

SYNC_MASTER=K78_MLB SYNC_DATE=02/08/2011

PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER 051-8870 | SIZE D
REVISION 3.13.0
BRANCH
PAGE 16 OF 109
SHEET 14 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 C1709 C1710
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL

C1711 C1712 C1713 C1714 C1715 C1716
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL

C1717 C1718 C1719 C1720 C1721 C1722
22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1723-C1724):

C1723 C1724 C1725
270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

Place on bottom side of U1000

C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747
1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 C1749 C1750 C1751 C1752 C1753 C1754 C1755
10UF 20% 6.3V CERM-X5R 0402-1

C1756
270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1702
0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757
1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 C1759 C1760 C1761 C1762
1UF 10% 10V X5R 402

C1763 C1764 C1765 C1766 C1767
10UF 20% 6.3V CERM-X5R 0402-1

C1768
270UF 20% 2V TANT CASE-B2-SM

SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

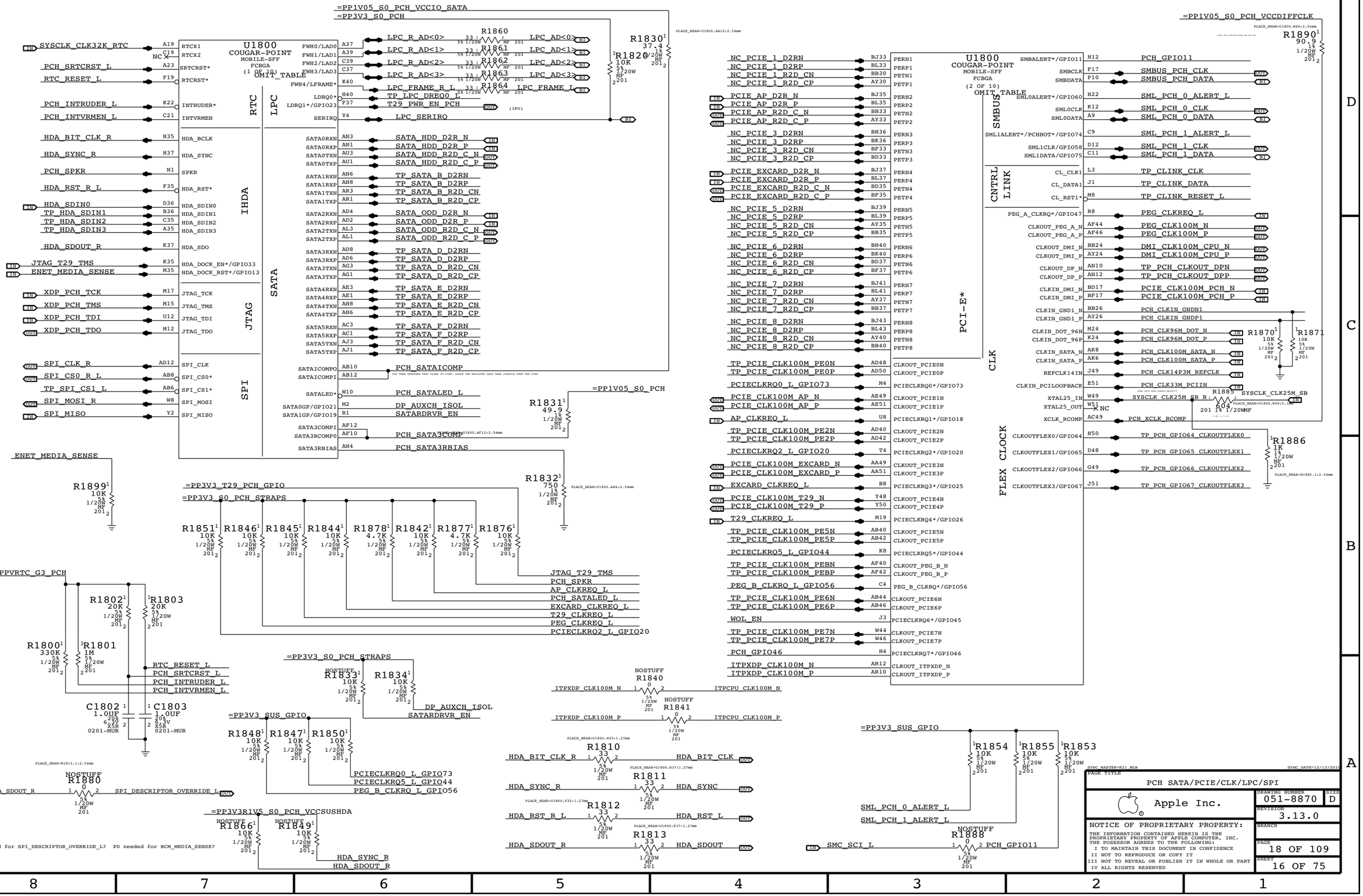
REVISION: 3.13.0

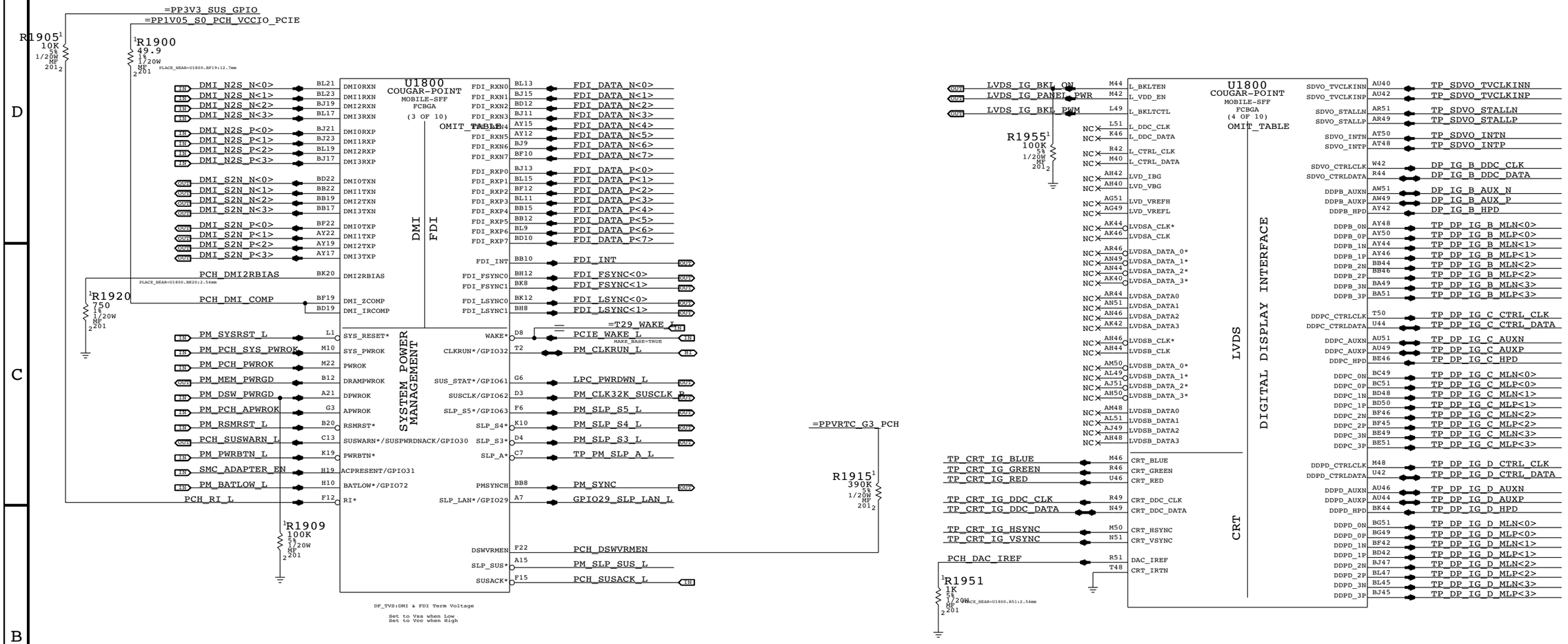
BRANCH:

PAGE: 17 OF 109

SHEET: 15 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


U1800
COUGAR-POINT
MOBILE-SFF
FCBGA
(1 OF 10)
OMIT_TABLE
RTC
LPC
IHDA
JTAG
SATA
SPI
SYSCLK_CLK32K_RTC
PCH_SRTCRST_L
RTC_RESET_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_T29_TMS
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LPC_FRAME_R_L
TP_LPC_DREQ0_L
T29_PWR_EN_PCH
LPC_SERIRQ
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
TP_SATA_B_D2RN
TP_SATA_B_D2RP
TP_SATA_B_R2D_CN
TP_SATA_B_R2D_CP
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
PCH_SATAICOMP
PCH_SATALED_L
DP_AUXCH_ISOL
SATARDRVR_EN
PCH_SATA3COMP
PCH_SATA3RBIAS
=PP1V05_S0_PCH_VCCIO_SATA
=PP3V3_S0_PCH
=PP1V05_S0_PCH
R1830 37.4
R1820 10K
R1860 R1861 R1862 R1863 R1864 33
R1831 49.9
R1832 750
R1899 10K
ENET_MEDIA_SENSE
=PP3V3_T29_PCH_GPIO
=PP3V3_S0_PCH_STRAPS
R1851 R1846 R1845 R1844 R1878 R1842 R1877 R1876 10K 4.7K
JTAG_T29_TMS
PCH_SPKR
AP_CLKREQ_L
PCH_SATALED_L
EXCARD_CLKREQ_L
T29_CLKREQ_L
PEG_CLKREQ_L
PCIECLKRQ2_L_GPIO20
=PPVRTC_G3_PCH
R1802 20K
R1803 20K
R1800 330K
R1801 1M
C1802 1.0UF
C1803 1.0UF
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
=PP3V3_S0_PCH_STRAPS
R1833 R1834 10K
DP_AUXCH_ISOL
SATARDRVR_EN
=PP3V3_SUS_GPIO
R1848 R1847 R1850 10K
PCIECLKRQ0_L_GPIO73
PCIECLKRQ5_L_GPIO44
PEG_B_CLKRQ_L_GPIO56
R1880 0
HDA_SDOUT_R
SPI_DESCRIPTOR_OVERRIDE_L
=PP3V5V1R1V5_S0_PCH_VCCSUSHDA
R1866 R1849 10K
HDA_SYNC_R
HDA_SDOUT_R
Pullup needed for SPI_DESCRIPTOR_OVERRIDE_L? PD needed for BCM_MEDIA_SENSE?
R1840 0
R1841 0
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
R1810 33
R1811 33
R1812 33
R1813 33
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
PCI-E*
CLK
CLOCK
FLEX
SMBUS
CNTRL
LINK
NC_PCIE_1_D2RN
NC_PCIE_1_D2RP
NC_PCIE_1_R2D_CN
NC_PCIE_1_R2D_CP
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
NC_PCIE_3_D2RN
NC_PCIE_3_D2RP
NC_PCIE_3_R2D_CN
NC_PCIE_3_R2D_CP
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
TP_PCIE_CLK100M_PE0N
TP_PCIE_CLK100M_PE0P
PCIECLKRQ0_L_GPIO73
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
TP_PCIE_CLK100M_PE2N
TP_PCIE_CLK100M_PE2P
PCIECLKRQ2_L_GPIO20
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
PCIE_CLK100M_T29_N
PCIE_CLK100M_T29_P
T29_CLKREQ_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCIECLKRQ5_L_GPIO44
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEG_B_CLKRQ_L_GPIO56
TP_PCIE_CLK100M_PE6N
TP_PCIE_CLK100M_PE6P
WOL_EN
TP_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P
PCH_GPIO46
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK1
CL_DATA1
CL_RST1*
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
PCH_GPIO11
SMBUS_PCH_CLK
SMBUS_PCH_DATA
SML_PCH_0_ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
SML_PCH_1_ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEG_CLKREQ_L
PEG_CLK100M_N
PEG_CLK100M_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB
PCH_XCLK_RCOMP
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
=PP1V05_S0_PCH_VCCDIFFCLK
R1890 90.9
R1870 R1871 10K
R1886 1K
R1885 604
R1854 R1855 R1853 10K
SML_PCH_0_ALERT_L
SML_PCH_1_ALERT_L
R1888 0
SMC_SCI_L
PCH_GPIO11
SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2011
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 18 OF 109
SHEET 16 OF 75
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PAGE TITLE: PCH DMI/FDI/GRAPHICS

Apple Inc.

DRAWING NUMBER: 051-8870 | SIZE: D

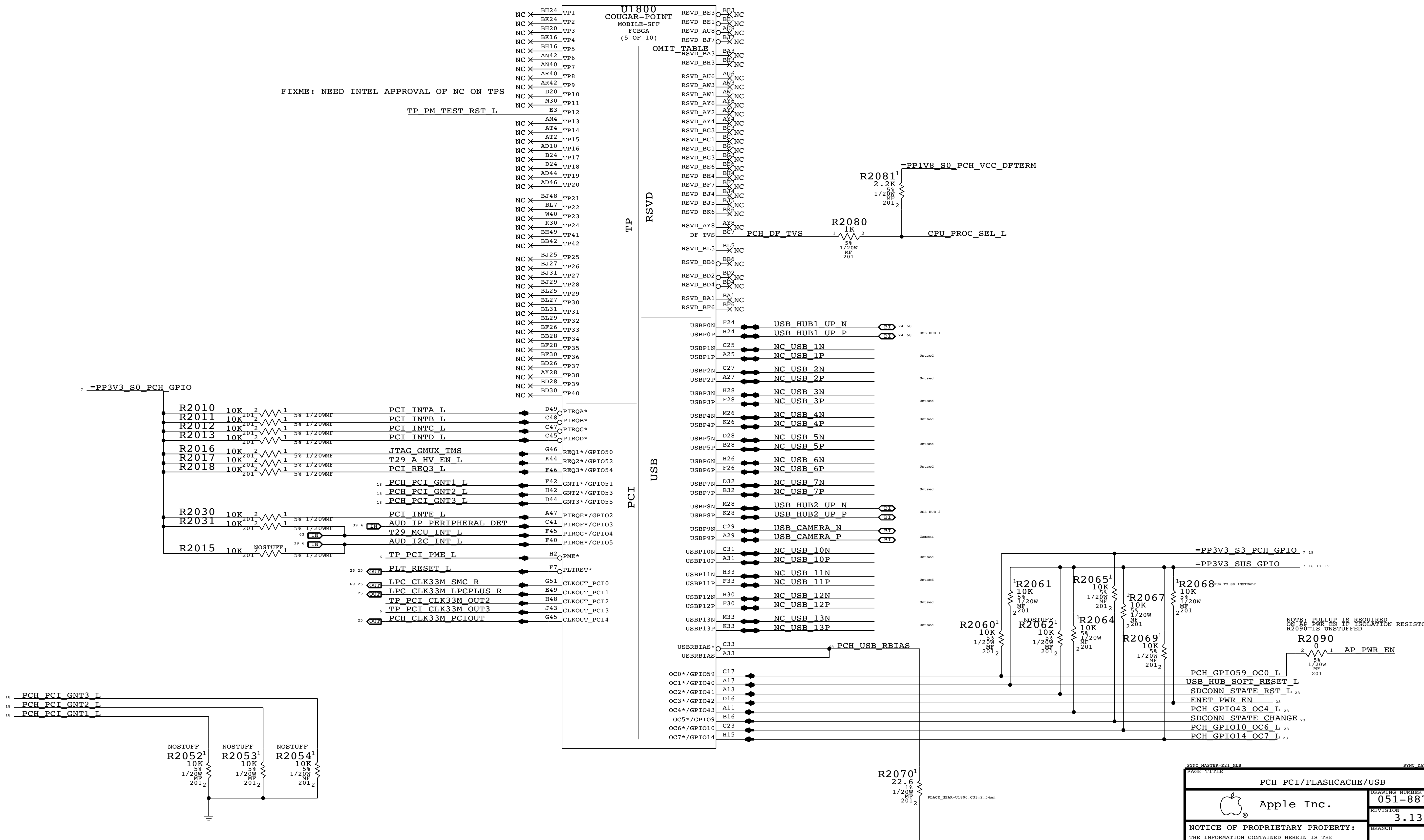
REVISION: 3.13.0

BRANCH:

PAGE: 19 OF 109

SHEET: 17 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


U1800
COUGAR-POINT
MOBILE-SFF
FCBGA
(5 OF 10)
OMIT_TABLE
TP
RSVD
PCI
USB
FIXME: NEED INTEL APPROVAL OF NC ON TPS
TP_PM_TEST_RST_L
=PP3V3_S0_PCH_GPIO
R2010
R2011
R2012
R2013
R2016
R2017
R2018
R2030
R2031
R2015
PCI_INTA_L
PCI_INTB_L
PCI_INTC_L
PCI_INTD_L
JTAG_GMUX_TMS
T29_A_HV_EN_L
PCI_REQ3_L
PCH_PCI_GNT1_L
PCH_PCI_GNT2_L
PCH_PCI_GNT3_L
PCI_INTE_L
AUD_IP_PERIPHERAL_DET
T29_MCU_INT_L
AUD_I2C_INT_L
TP_PCI_PME_L
PLT_RESET_L
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
TP_PCI_CLK33M_OUT2
TP_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
=PP1V8_S0_PCH_VCC_DFTERM
R2081
2.2K
R2080
1K
PCH_DF_TVS
CPU_PROC_SEL_L
USB_HUB1_UP_N
USB_HUB1_UP_P
NC_USB_1N
NC_USB_1P
NC_USB_2N
NC_USB_2P
NC_USB_3N
NC_USB_3P
NC_USB_4N
NC_USB_4P
NC_USB_5N
NC_USB_5P
NC_USB_6N
NC_USB_6P
NC_USB_7N
NC_USB_7P
USB_HUB2_UP_N
USB_HUB2_UP_P
USB_CAMERA_N
USB_CAMERA_P
NC_USB_10N
NC_USB_10P
NC_USB_11N
NC_USB_11P
NC_USB_12N
NC_USB_12P
NC_USB_13N
NC_USB_13P
PCH_USB_RBIAS
R2070
22.6
=PP3V3_S3_PCH_GPIO
=PP3V3_SUS_GPIO
R2060
R2061
R2062
R2064
R2065
R2067
R2068
R2069
NOTE: PULLUP IS REQUIRED ON AP_PWR_EN IF ISOLATION RESISTOR R2090 IS UNSTUFFED
R2090
AP_PWR_EN
PCH_GPIO59_OC0_L
USB_HUB_SOFT_RESET_L
SDCONN_STATE_RST_L
ENET_PWR_EN
PCH_GPIO43_OC4_L
SDCONN_STATE_CHANGE
PCH_GPIO10_OC6_L
PCH_GPIO14_OC7_L
NOSTUFF
R2052
R2053
R2054

PAGE TITLE

PCH PCI/FLASHCACHE/USB

Apple Inc.

DRAWING NUMBER	SIZE
051-8870	D

REVISION 3.13.0

BRANCH

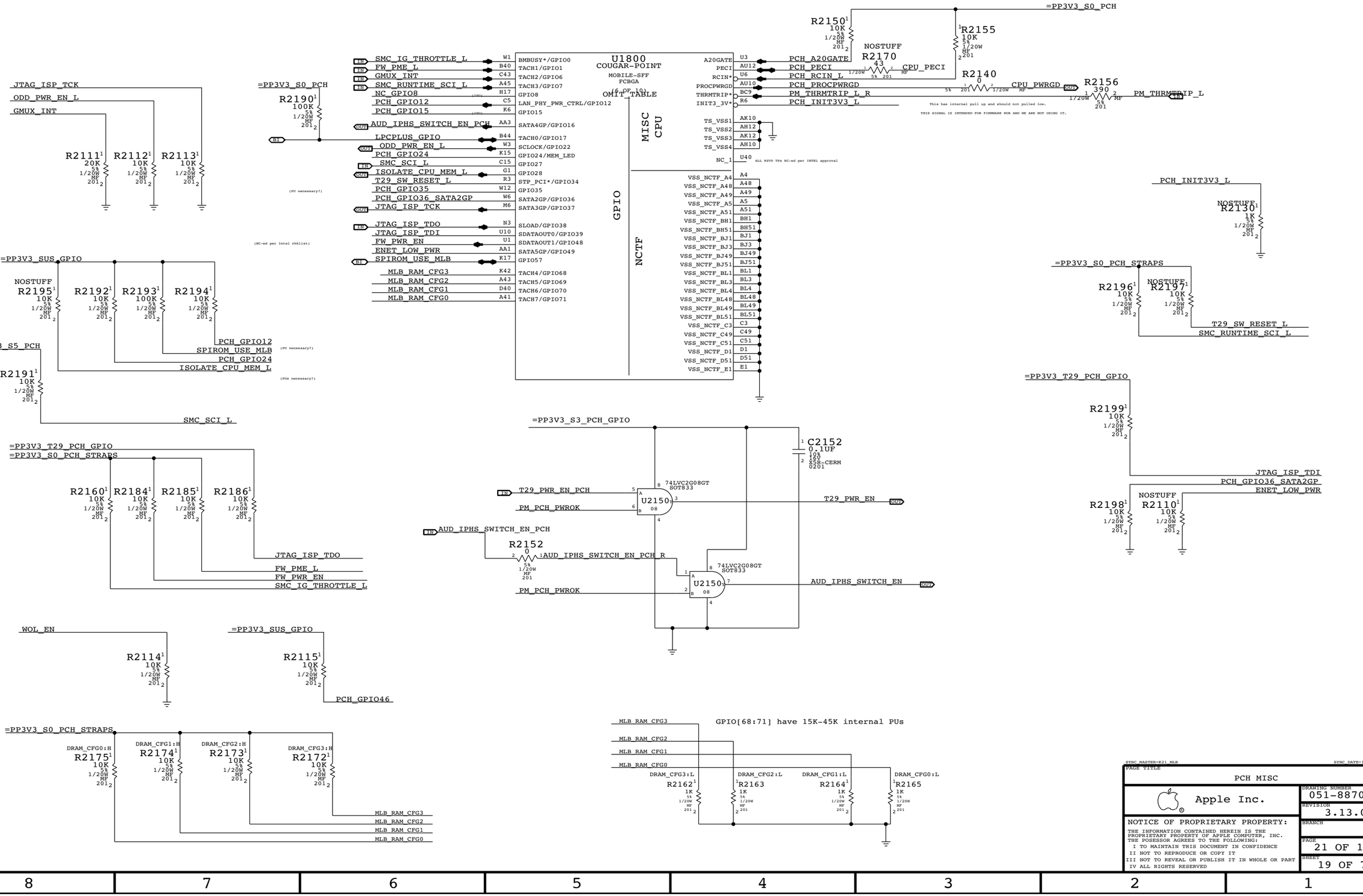
PAGE 20 OF 109

SHEET 18 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K21 MLB SYNC_DATE=12/13/2010

PAGE TITLE

PCH MISC

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

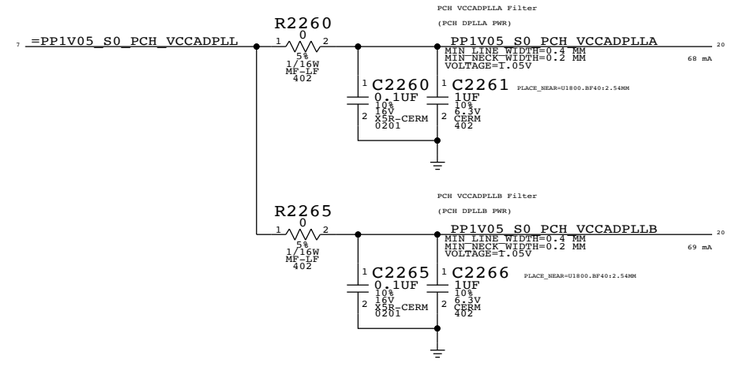
BRANCH

PAGE 21 OF 109

SHEET 19 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

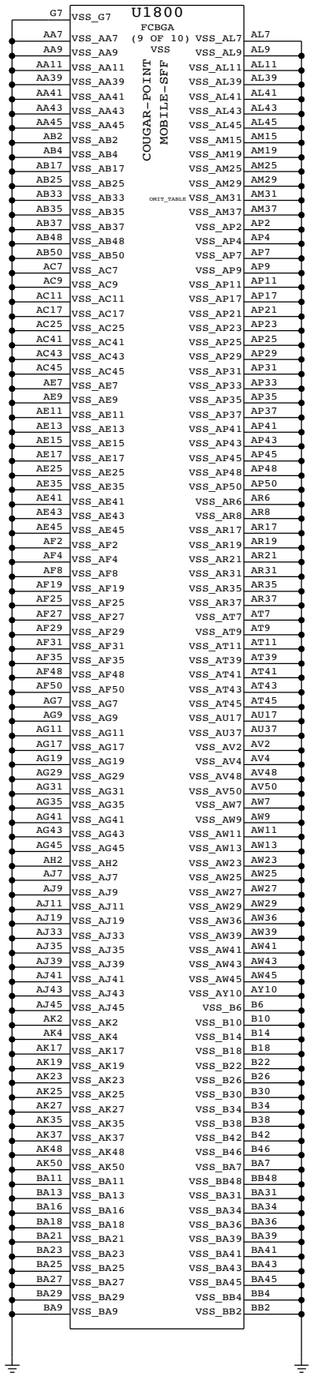


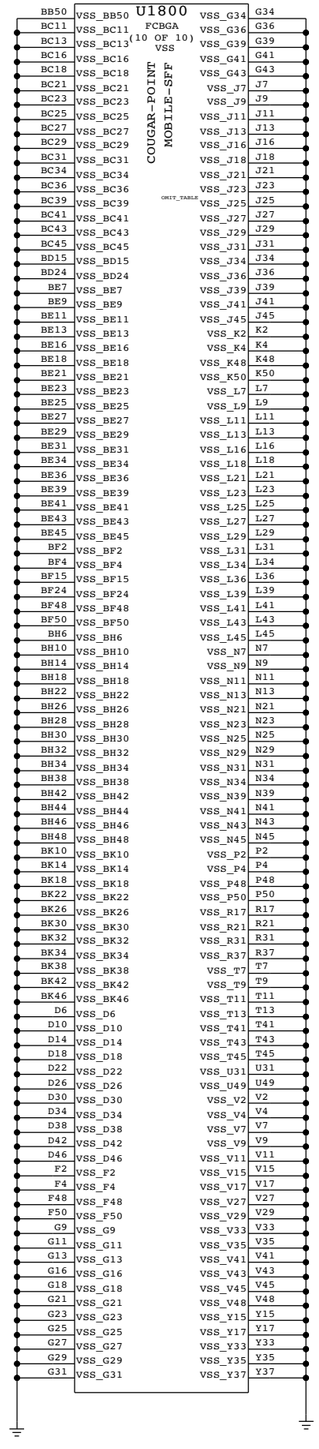
PAGE TITLE
PCH POWER

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 22 OF 109
SHEET 20 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

PAGE TITLE

PCH GROUNDS

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

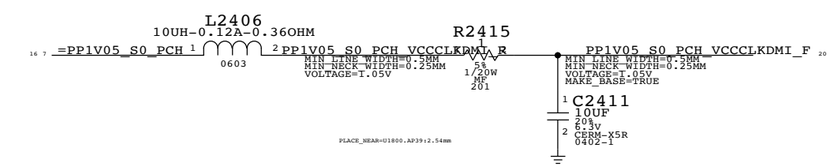
BRANCH

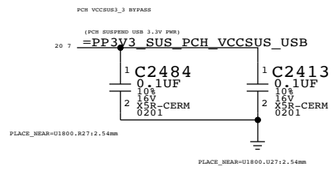
PAGE 23 OF 109

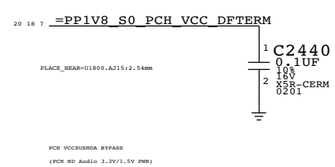
SHEET 21 OF 75

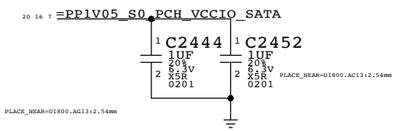
NOTICE OF PROPRIETARY PROPERTY:

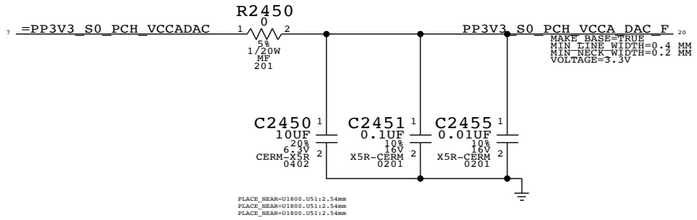
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

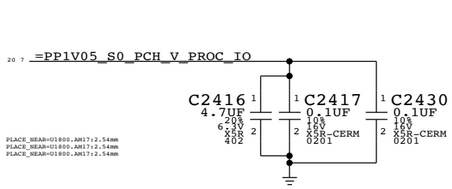


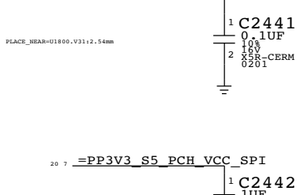


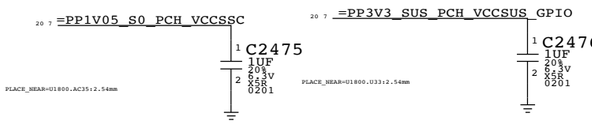


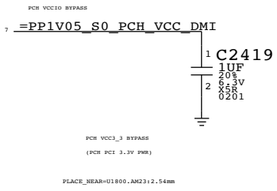


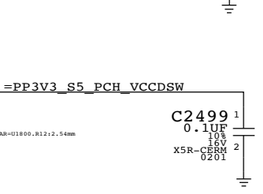


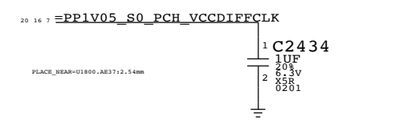


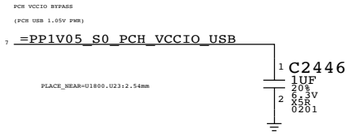


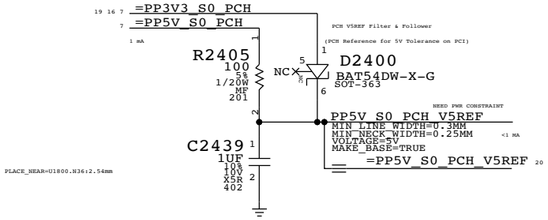


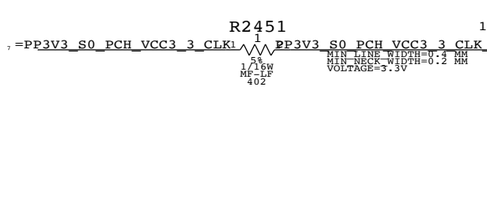


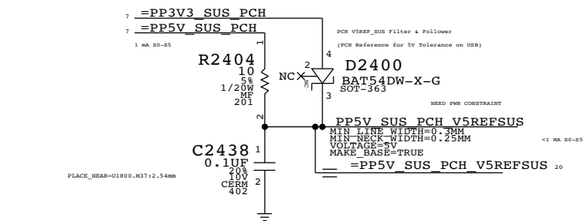


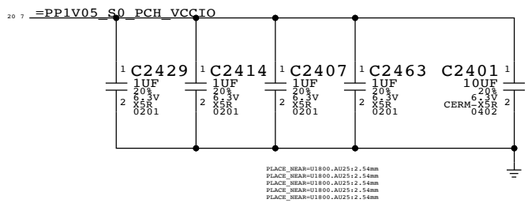


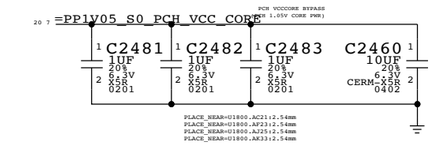


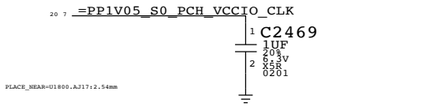


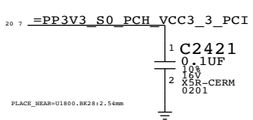


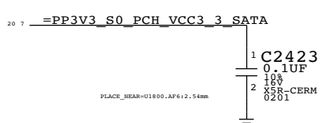


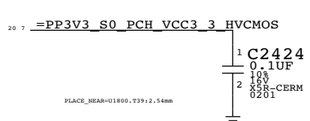


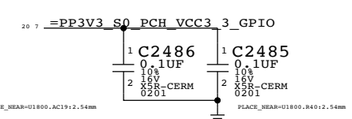


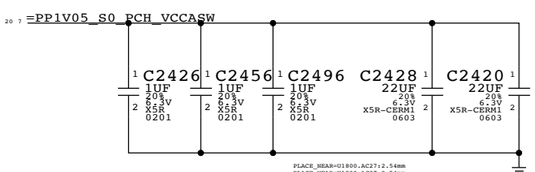












SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE: PCH DECOUPLING

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 24 OF 109

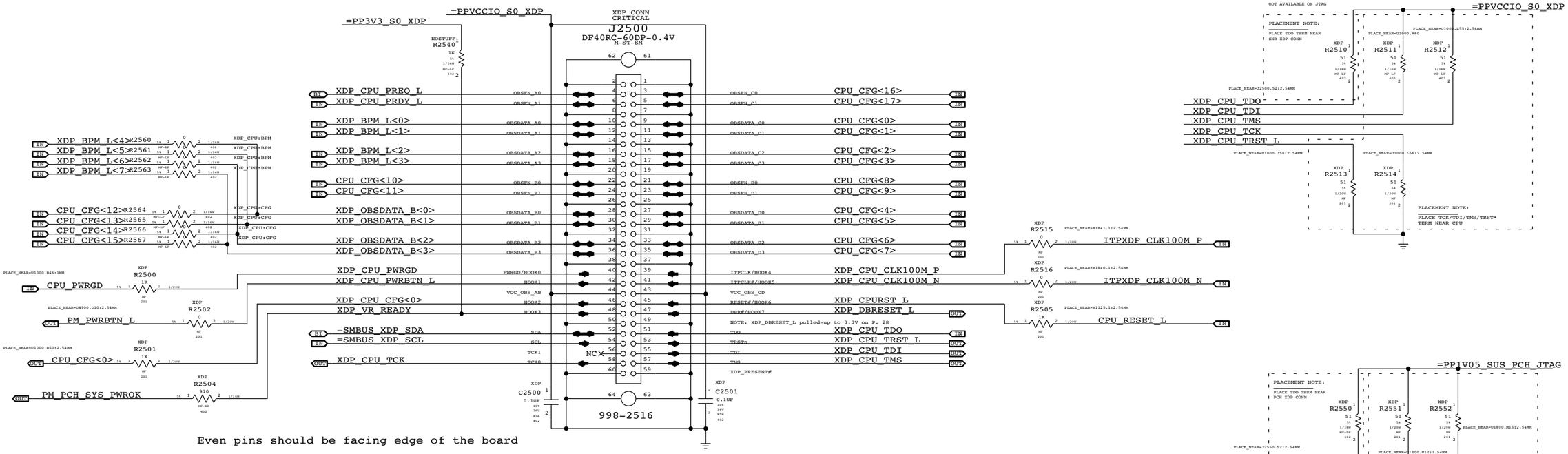
SHEET: 22 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

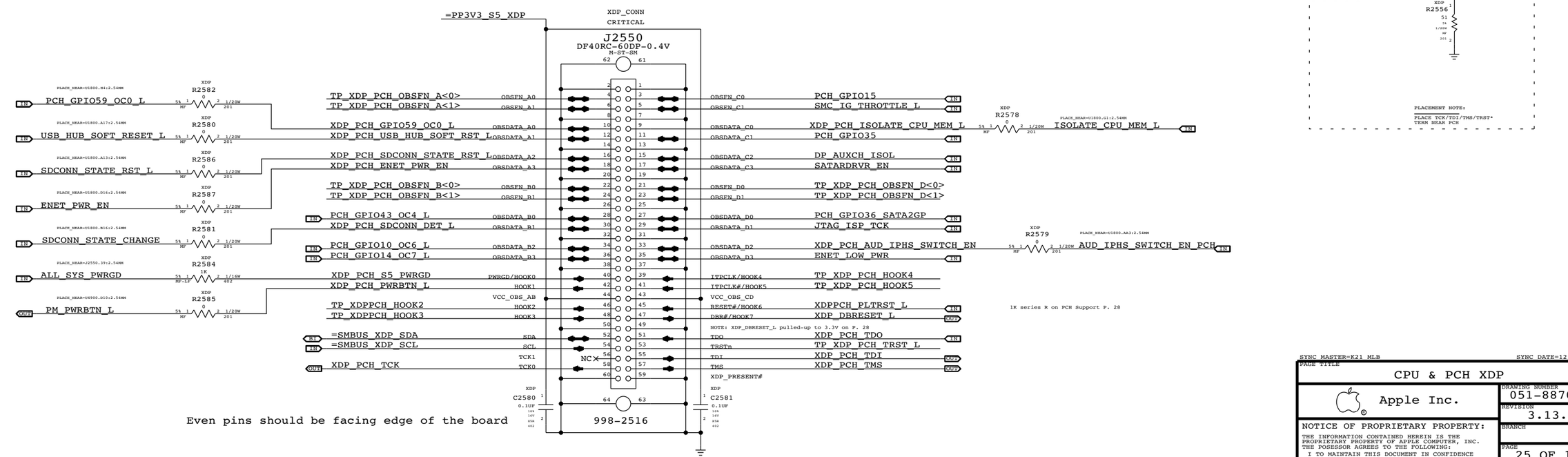
PROCESSOR MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



PCH MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



SYNC MASTER=K21 MLB
SYNC DATE=12/13/2010

PAGE TITLE
CPU & PCH XDP

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 25 OF 109
SHEET 23 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

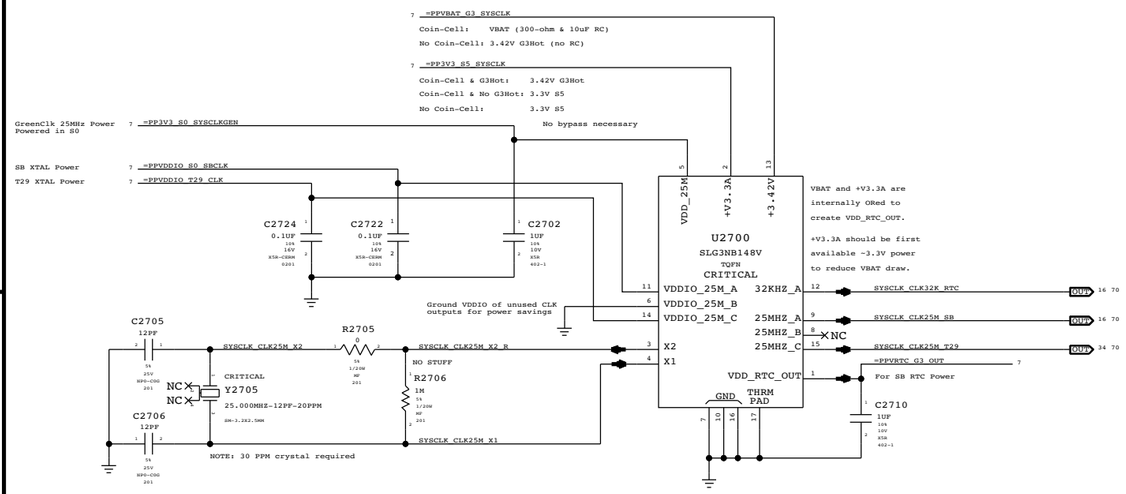
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

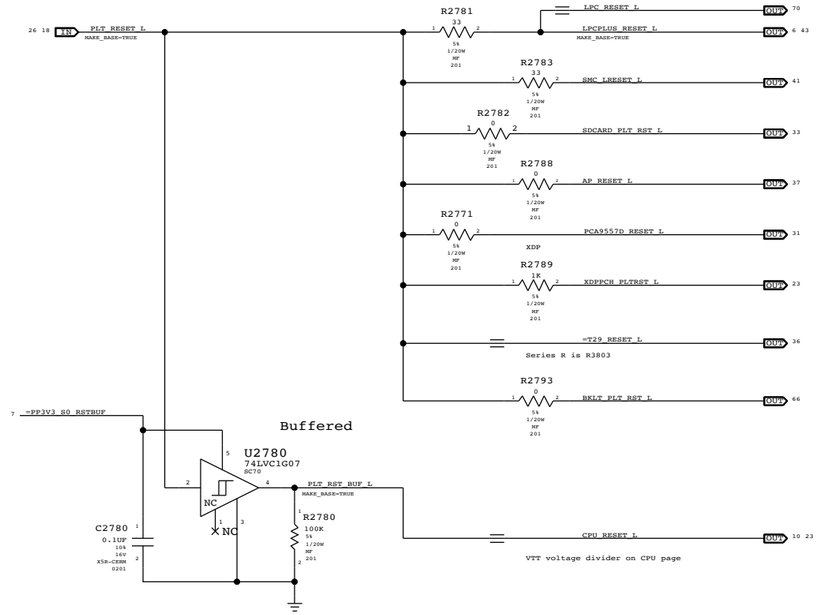
SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE	USB HUBS
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 26 OF 109
	SHEET 24 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

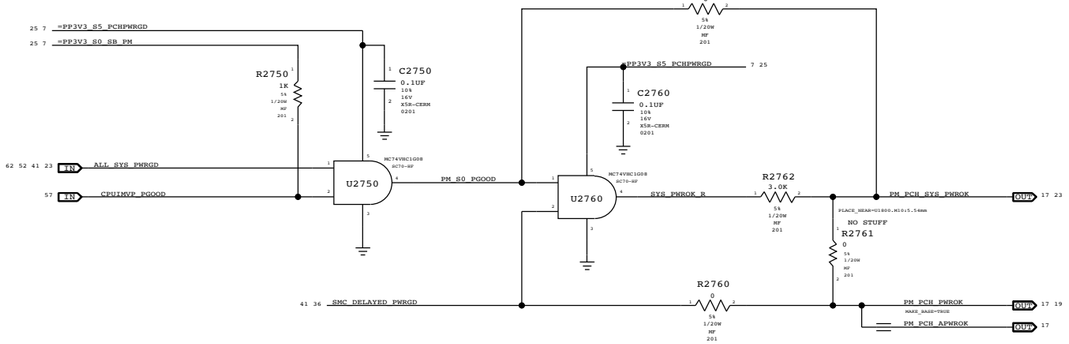
System RTC Power Source & 32kHz / 25MHz Clock Generator



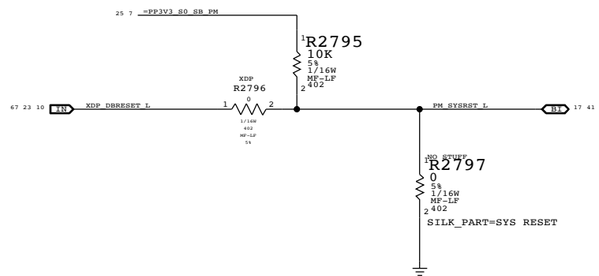
Platform Reset Connections



PCH S0 PWRGD

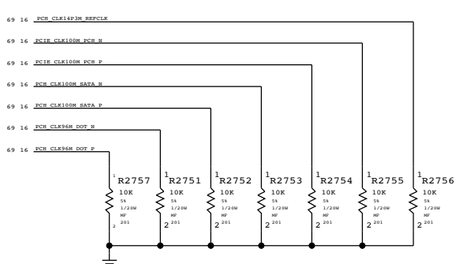


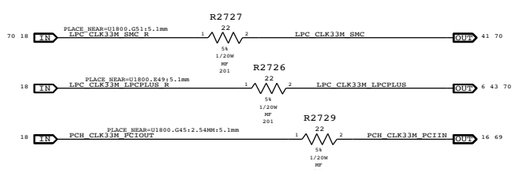
PCH Reset Button



CLOCK (CK505)

UNUSED clock terminations for FCIM MODE





SYNC_MASTER=K79_MLB SYNC_DATE=11/29/201

PAGE TITLE

Clock (CK505) and Chipset Support

Apple Inc.

DRAWING NUMBER 051-8870

SIZE D

REVISION 3.13.0

BRANCH

PAGE 27 OF 109

SHEET 25 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

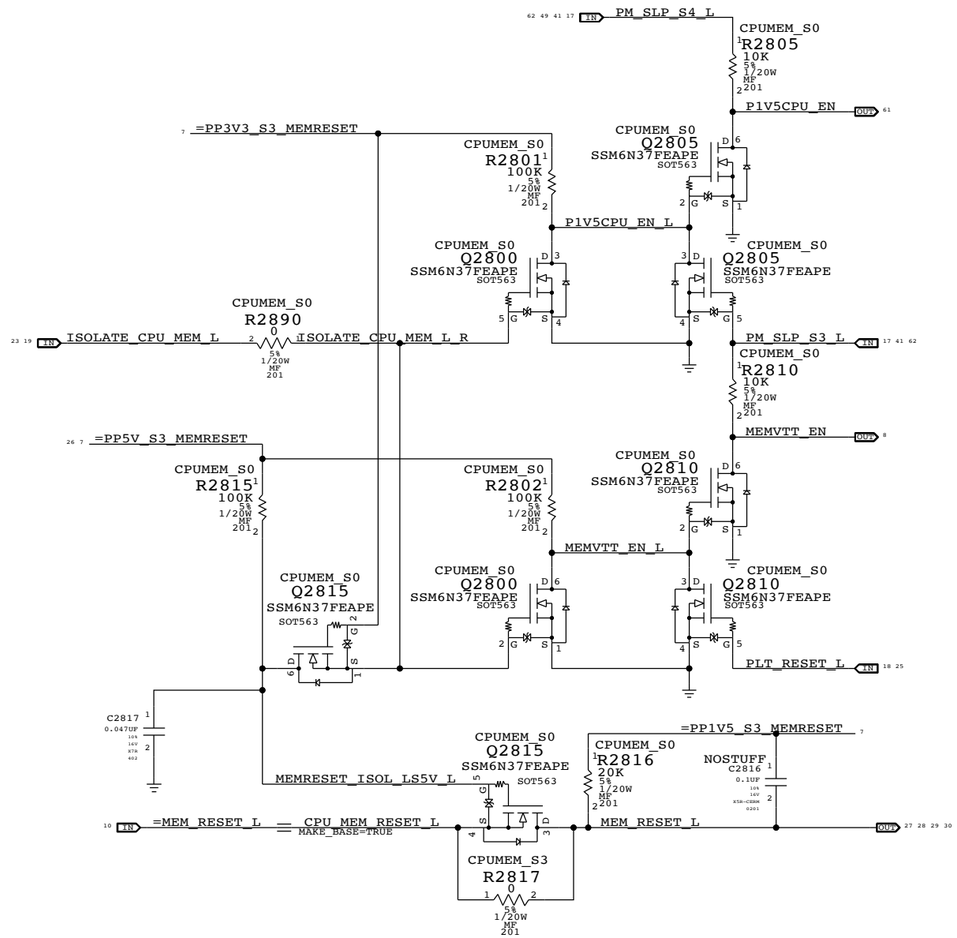
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

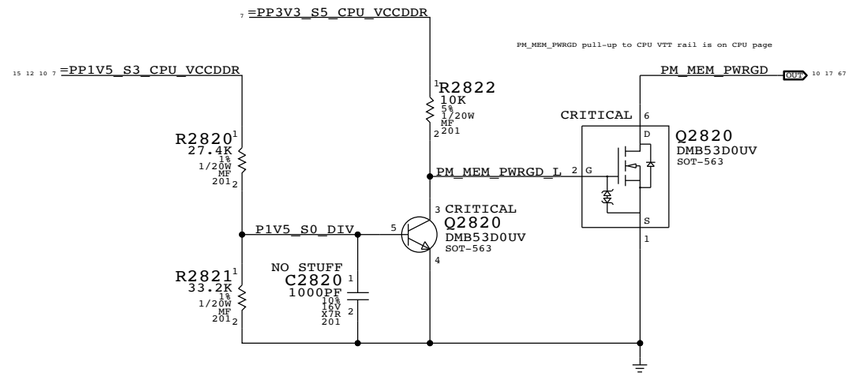


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1
to	2	0	0	1	1	1	0	1
	3	0	0	0	1	X	0	0
S3	4	0	0	1	1	X	0	1
	5	0	1	1	1	0 (*)	1	1
to	6	0	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

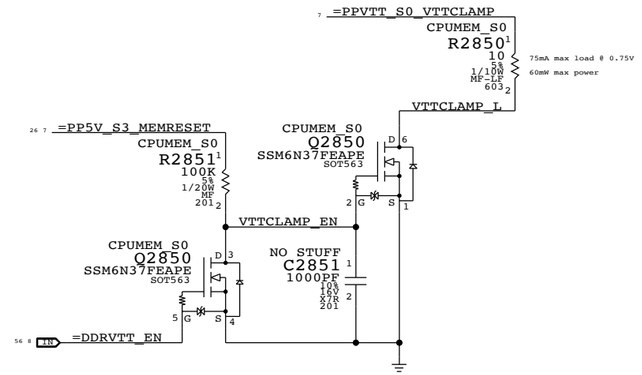
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

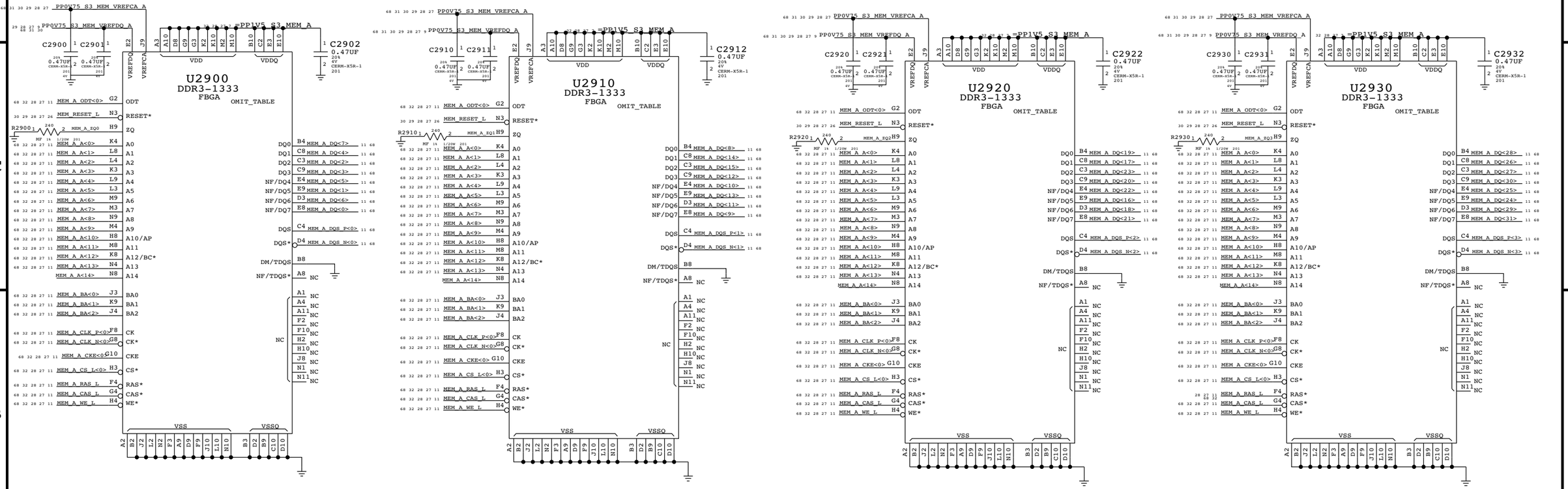
BRANCH:

PAGE: 28 OF 109

SHEET: 26 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K78 MLB SYNC DATE=12/07/2010

PAGE TITLE

DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

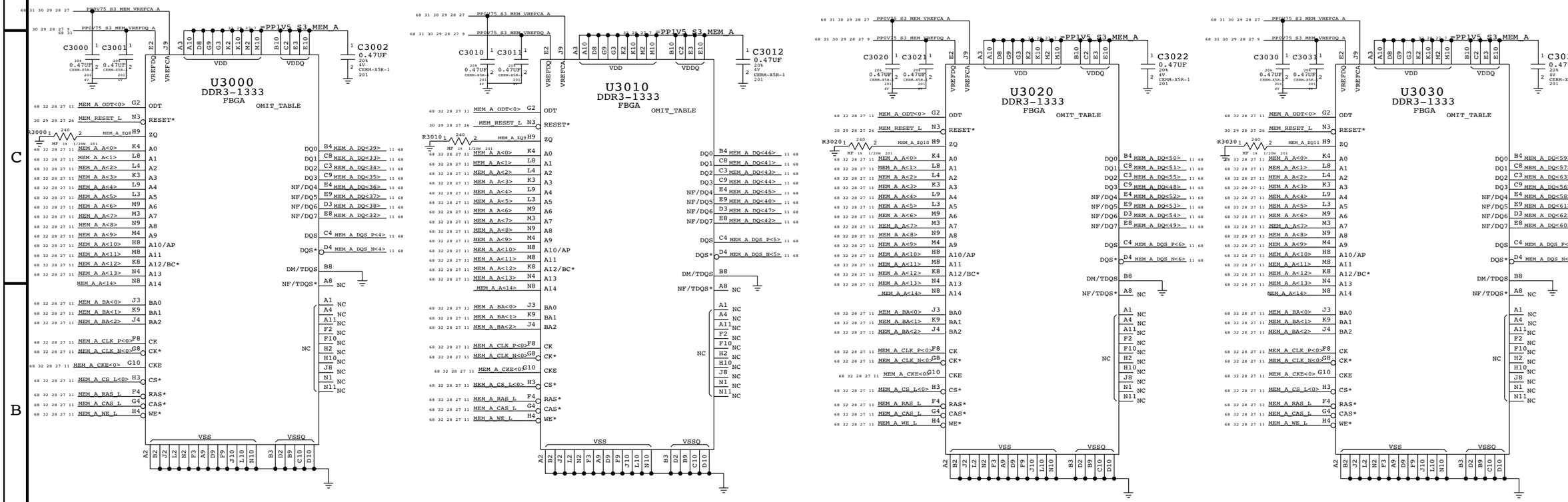
BRANCH

PAGE 29 OF 109

SHEET 27 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

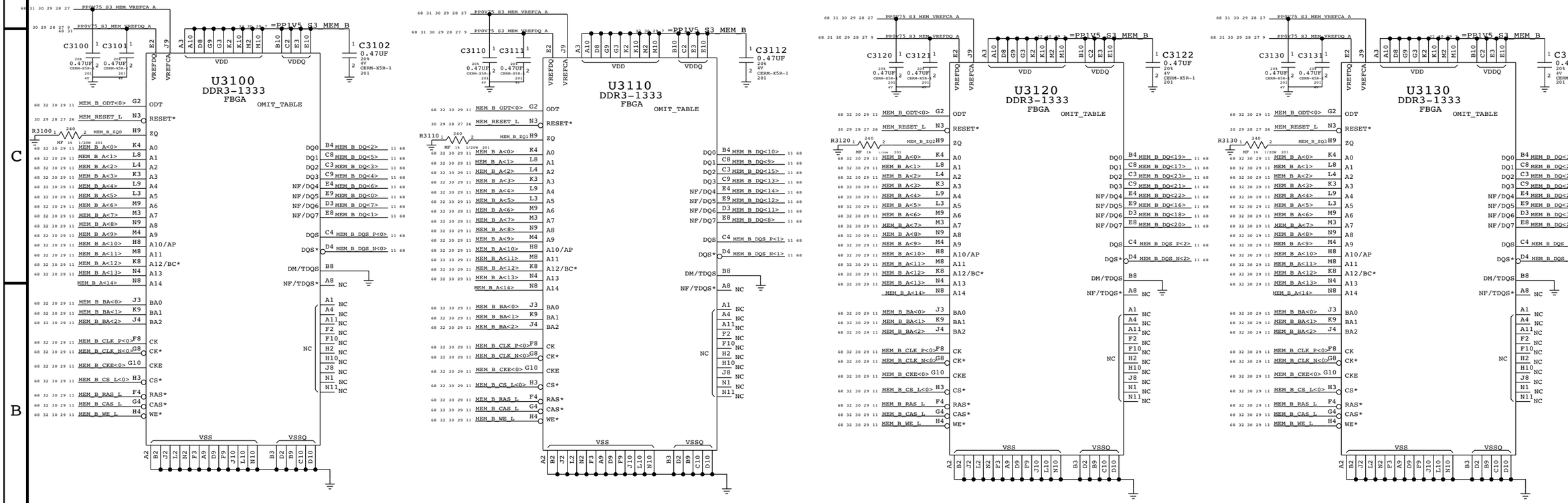
SYNC MASTER=K78 MLB SYNC DATE=12/07/2010

PAGE TITLE
DDR3 DRAM CHANNEL A (32-63)

Apple Inc.

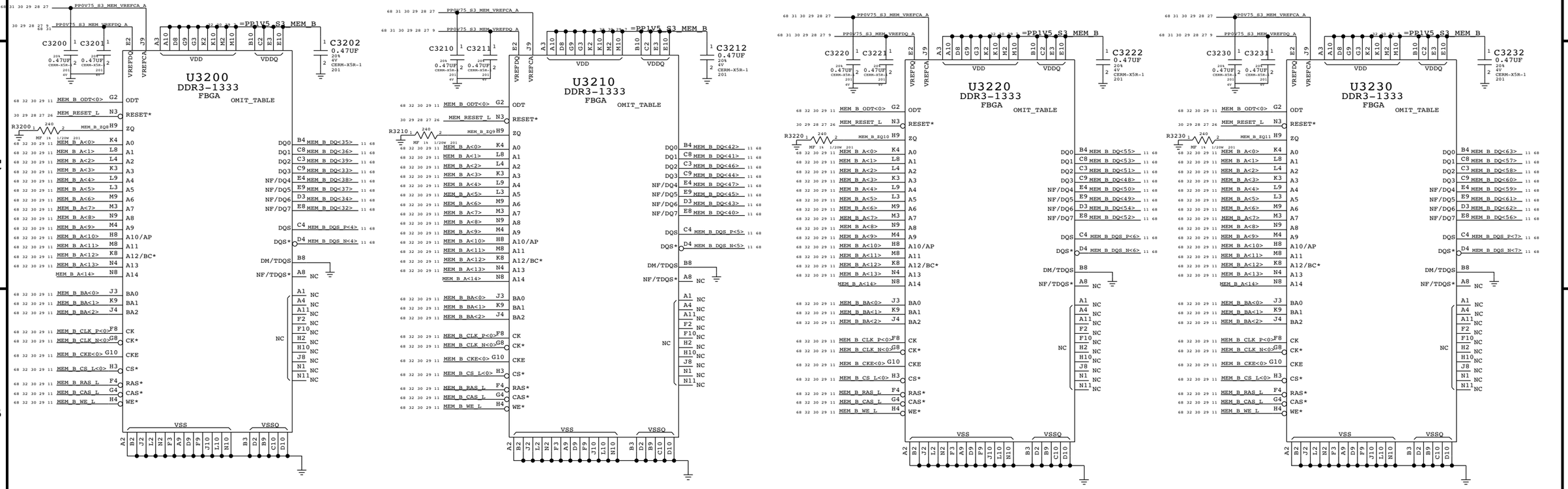
DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 30 OF 109
SHEET 28 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K78 MLB	SYNC DATE=12/07/2010
PAGE TITLE	DDR3 DRAM CHANNEL B (0-31)
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE 31 OF 109
	SHEET 29 OF 75



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K78_MLB SYNC_DATE=12/07/2011

PAGE TITLE

DDR3 DRAM CHANNEL B (32-63)

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

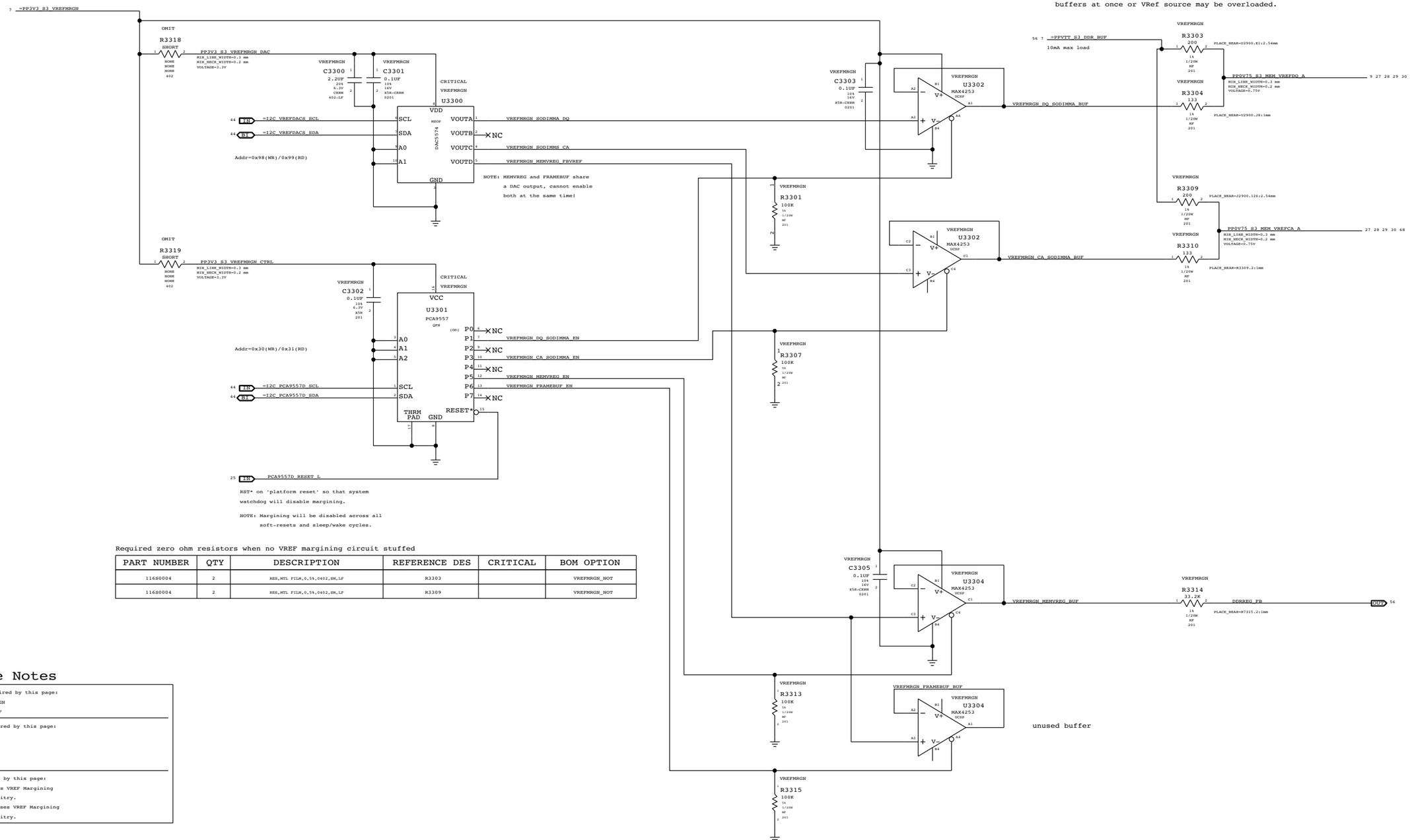
BRANCH

PAGE 32 OF 109

SHEET 30 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303		VREFMRGN_NOT
11680004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

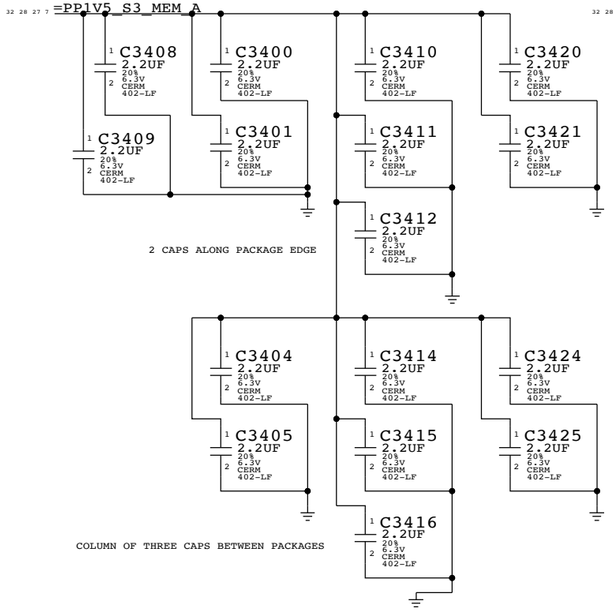
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

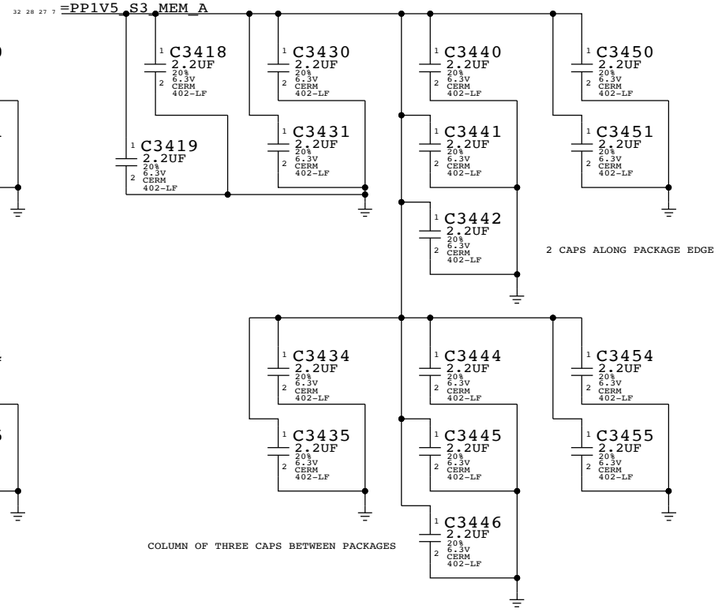
PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

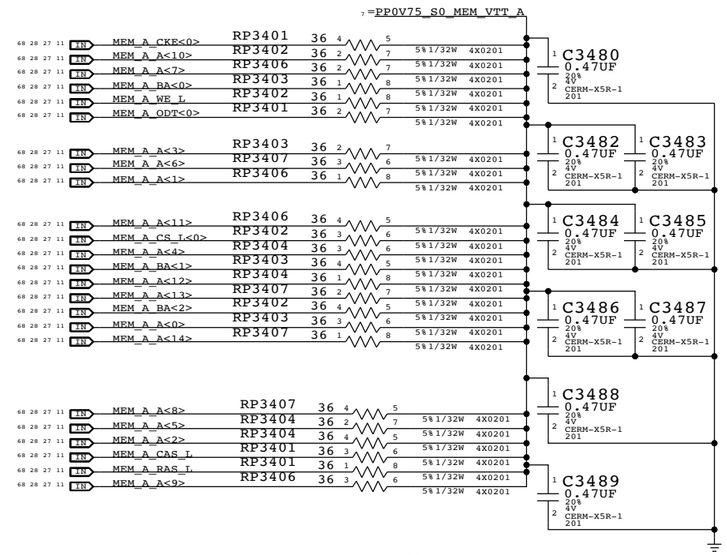
DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 33 OF 109
SHEET: 31 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



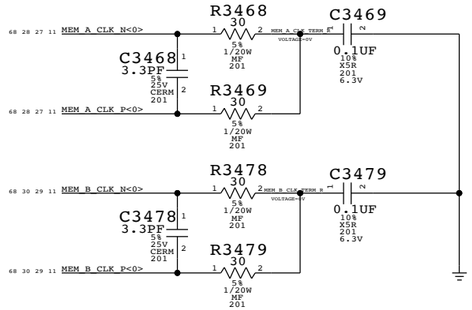


JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



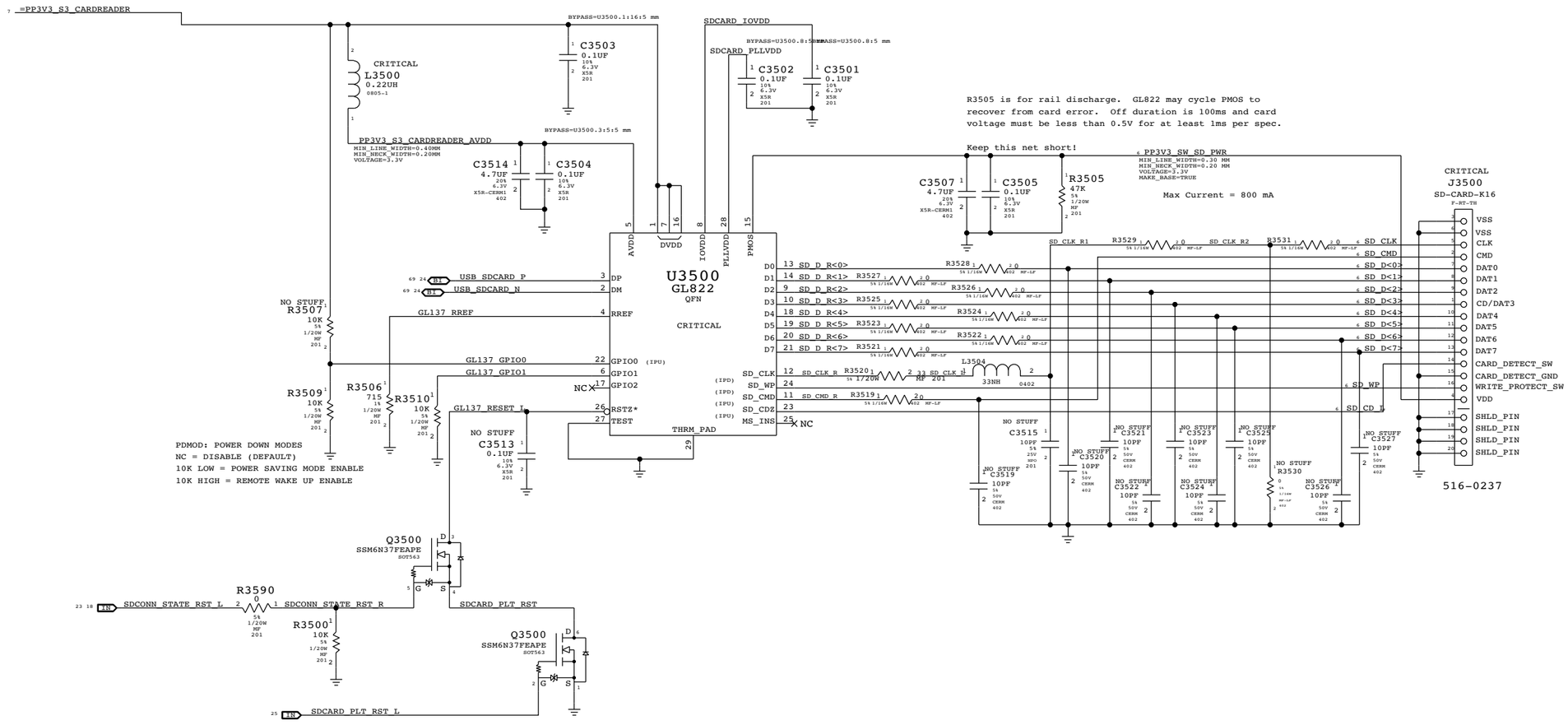
MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



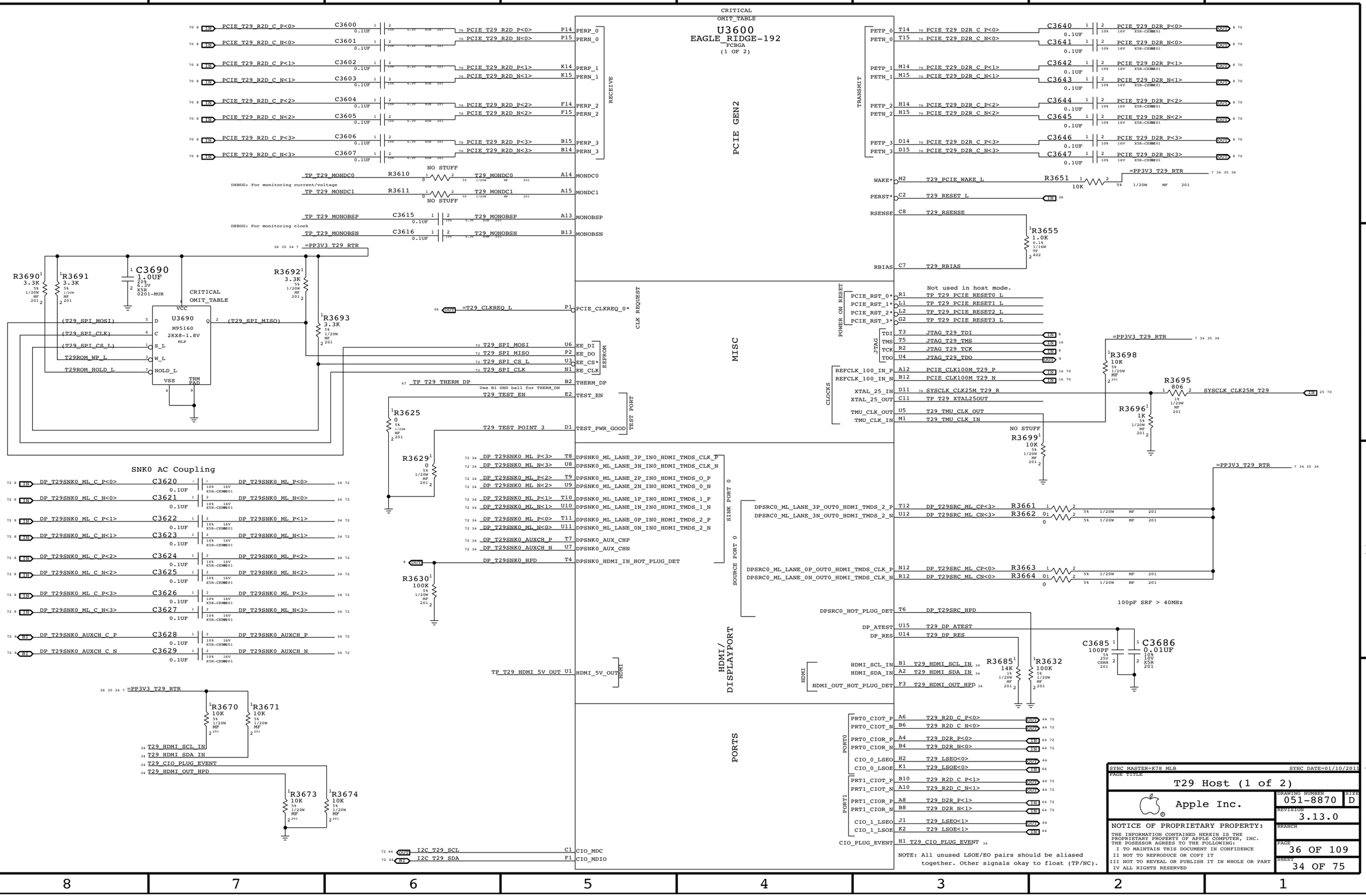
SYNC MASTER=K78 MLB	SYNC DATE=12/16/2010
PAGE TITLE: DDR3 DRAM Channel B (32-63)	
Apple Inc.	DRAWING NUMBER: 051-8870 SIZE: D
	REVISION: 3.13.0
	BRANCH:
	PAGE: 34 OF 109
	SHEET: 32 OF 75

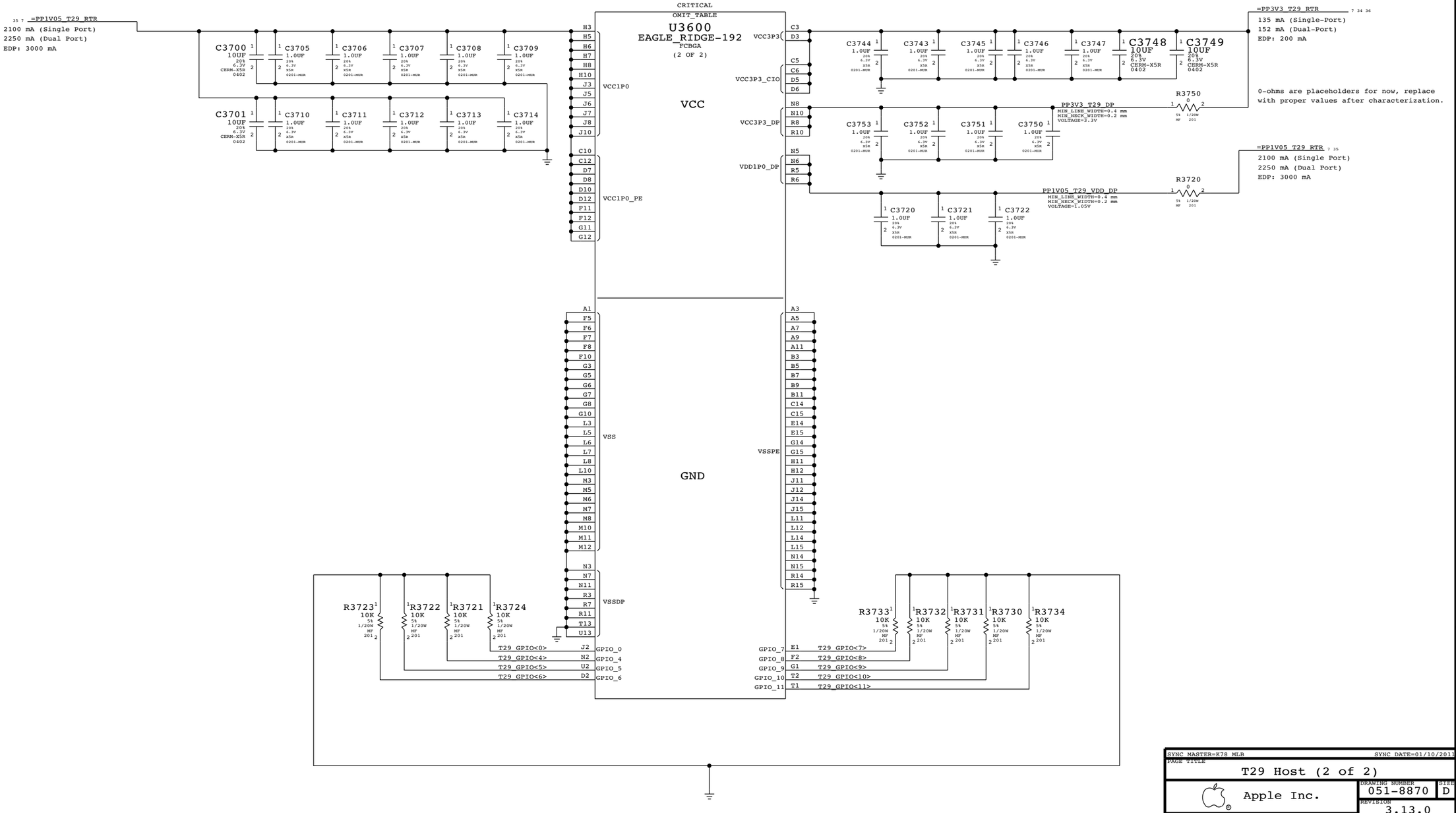
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=(MASTER)	SYNC DATE=(MASTER)
PAGE TITLE	SecureDigital Card Reader
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 35 OF 109
	SHEET 33 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


CRITICAL
OMIT_TABLE
U3600
EAGLE_RIDGE-192
PCBGA
(1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
PCIE_T29_R2D_C_P<0>
PCIE_T29_R2D_C_N<0>
PCIE_T29_R2D_C_P<1>
PCIE_T29_R2D_C_N<1>
PCIE_T29_R2D_C_P<2>
PCIE_T29_R2D_C_N<2>
PCIE_T29_R2D_C_P<3>
PCIE_T29_R2D_C_N<3>
PCIE_T29_R2D_P<0>
PCIE_T29_R2D_N<0>
PCIE_T29_R2D_P<1>
PCIE_T29_R2D_N<1>
PCIE_T29_R2D_P<2>
PCIE_T29_R2D_N<2>
PCIE_T29_R2D_P<3>
PCIE_T29_R2D_N<3>
PCIE_T29_D2R_C_P<0>
PCIE_T29_D2R_C_N<0>
PCIE_T29_D2R_C_P<1>
PCIE_T29_D2R_C_N<1>
PCIE_T29_D2R_C_P<2>
PCIE_T29_D2R_C_N<2>
PCIE_T29_D2R_C_P<3>
PCIE_T29_D2R_C_N<3>
PCIE_T29_D2R_P<0>
PCIE_T29_D2R_N<0>
PCIE_T29_D2R_P<1>
PCIE_T29_D2R_N<1>
PCIE_T29_D2R_P<2>
PCIE_T29_D2R_N<2>
PCIE_T29_D2R_P<3>
PCIE_T29_D2R_N<3>
NO STUFF
DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
TP_T29_MONDC0
TP_T29_MONDC1
TP_T29_MONOBSP
TP_T29_MONOBSN
R3610
R3611
C3615
C3616
T29_MONDC0
T29_MONDC1
T29_MONOBSP
T29_MONOBSN
MONDC0
MONDC1
MONOBSP
MONOBSN
=PP3V3_T29_RTR
WAKE*
PERST*
RSENSE
RBIAS
T29_PCIE_WAKE_L
T29_RESET_L
T29_RSENSE
T29_RBIAS
R3651
R3655
Not used in host mode.
POWER ON RESET
PCIE_RST_0*
PCIE_RST_1*
PCIE_RST_2*
PCIE_RST_3*
TP_T29_PCIE_RESET0_L
TP_T29_PCIE_RESET1_L
TP_T29_PCIE_RESET2_L
TP_T29_PCIE_RESET3_L
JTAG
TDI
TMS
TCK
TDO
JTAG_T29_TDI
JTAG_T29_TMS
JTAG_T29_TCK
JTAG_T29_TDO
CLOCKS
REFCLK_100_IN_P
REFCLK_100_IN_N
XTAL_25_IN
XTAL_25_OUT
TMU_CLK_OUT
TMU_CLK_IN
PCIE_CLK100M_T29_P
PCIE_CLK100M_T29_N
SYSCLK_CLK25M_T29_R
TP_T29_XTAL25OUT
T29_TMU_CLK_OUT
T29_TMU_CLK_IN
SYSCLK_CLK25M_T29
R3698
R3695
R3696
R3699
CLK REQUEST
PCIE_CLKREQ_0*
=T29_CLKREQ_L
MISC
EEPROM
T29_SPI_MOSI
T29_SPI_MISO
T29_SPI_CS_L
T29_SPI_CLK
EE_DI
EE_DO
EE_CS*
EE_CLK
C3690
1.0UF
U3690
M95160
2KX8-1.8V
R3690
R3691
R3692
R3693
CRITICAL
OMIT_TABLE
THERM_DP
TEST_EN
TEST_PWR_GOOD
TEST PORT
R3625
R3629
R3630
T29_TEST_EN
T29_TEST_POINT_3
DP_T29SNK0_HPD
DPSNK0_HDMI_IN_HOT_PLUG_DET
SINK PORT 0
SOURCE PORT 0
DPSNK0_ML_LANE_3P_IN0_HDMI_TMDS_CLK_P
DPSNK0_ML_LANE_3N_IN0_HDMI_TMDS_CLK_N
DPSNK0_ML_LANE_2P_IN0_HDMI_TMDS_0_P
DPSNK0_ML_LANE_2N_IN0_HDMI_TMDS_0_N
DPSNK0_ML_LANE_1P_IN0_HDMI_TMDS_1_P
DPSNK0_ML_LANE_1N_IN0_HDMI_TMDS_1_N
DPSNK0_ML_LANE_0P_IN0_HDMI_TMDS_2_P
DPSNK0_ML_LANE_0N_IN0_HDMI_TMDS_2_N
DPSNK0_AUX_CHP
DPSNK0_AUX_CHN
DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_N<3>
DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_N<0>
DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_N
DPSRC0_ML_LANE_3P_OUT0_HDMI_TMDS_2_P
DPSRC0_ML_LANE_3N_OUT0_HDMI_TMDS_2_N
DPSRC0_ML_LANE_0P_OUT0_HDMI_TMDS_CLK_P
DPSRC0_ML_LANE_0N_OUT0_HDMI_TMDS_CLK_N
DP_T29SRC_ML_CP<3>
DP_T29SRC_ML_CN<3>
DP_T29SRC_ML_CP<0>
DP_T29SRC_ML_CN<0>
R3661
R3662
R3663
R3664
100pF SRF > 40MHz
DPSRC0_HOT_PLUG_DET
DP_T29SRC_HPD
DP_ATEST
DP_RES
T29_DP_ATEST
T29_DP_RES
C3685
C3686
HDMI/
DISPLAYPORT
HDMI_5V_OUT
TP_T29_HDMI_5V_OUT_U1
HDMI_SCL_IN
HDMI_SDA_IN
HDMI_OUT_HOT_PLUG_DET
T29_HDMI_SCL_IN
T29_HDMI_SDA_IN
T29_HDMI_OUT_HPD
R3685
R3632
PORTS
PORT0
PORT1
PRT0_CIOT_P
PRT0_CIOT_N
PRT0_CIOR_P
PRT0_CIOR_N
CIO_0_LSEO
CIO_0_LSOE
PRT1_CIOT_P
PRT1_CIOT_N
PRT1_CIOR_P
PRT1_CIOR_N
CIO_1_LSEO
CIO_1_LSOE
CIO_PLUG_EVENT
T29_R2D_C_P<0>
T29_R2D_C_N<0>
T29_D2R_P<0>
T29_D2R_N<0>
T29_LSEO<0>
T29_LSOE<0>
T29_R2D_C_P<1>
T29_R2D_C_N<1>
T29_D2R_P<1>
T29_D2R_N<1>
T29_LSEO<1>
T29_LSOE<1>
T29_CIO_PLUG_EVENT
NOTE: All unused LSOE/EO pairs should be aliased
together. Other signals okay to float (TP/NC).
SNK0 AC Coupling
DP_T29SNK0_ML_C_P<0>
DP_T29SNK0_ML_C_N<0>
DP_T29SNK0_ML_C_P<1>
DP_T29SNK0_ML_C_N<1>
DP_T29SNK0_ML_C_P<2>
DP_T29SNK0_ML_C_N<2>
DP_T29SNK0_ML_C_P<3>
DP_T29SNK0_ML_C_N<3>
DP_T29SNK0_AUXCH_C_P
DP_T29SNK0_AUXCH_C_N
C3600
C3601
C3602
C3603
C3604
C3605
C3606
C3607
C3620
C3621
C3622
C3623
C3624
C3625
C3626
C3627
C3628
C3629
C3640
C3641
C3642
C3643
C3644
C3645
C3646
C3647
0.1UF
R3670
R3671
R3673
R3674
I2C_T29_SCL
I2C_T29_SDA
CIO_MDC
CIO_MDIO
SYNC MASTER=K78_MLB
SYNC DATE=01/10/2011
PAGE TITLE
T29 Host (1 of 2)
Apple Inc.
DRAWING NUMBER
051-8870
SIZE
D
REVISION
3.13.0
BRANCH
PAGE
36 OF 109
SHEET
34 OF 75
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC MASTER=K78 MLB SYNC DATE=01/10/2011

PAGE TITLE

T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 37 OF 109

SHEET 35 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8–13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 18V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_T29BST
8–13V Input
Changes required for 2S.

R3820 0.010 1% 1/4W MF 805
Q3880 SI8409DB BGA
C3880 0.1UF 10% 25V X5R 402
R3880 470K 5% 1/20W MF 201
R3881 150K 5% 1/20W MF 201
R3891 200K 1% 1/20W MF 201 <R1>
C3890 10UF 10% 25V X5R 805
C3891 10UF 10% 25V X5R 805
L3895 6.8UH-4.0A PIMB062D-SM
D3895 POWERDI-123 DFLS230L
R3889 0 5% 1/20W MF 201
XW3895 SH PLACE_NEAR=C3895.1:2 mm
U3890 LT3957 QFN
C3892 4.7UF 10% 10V X5R 805
C3887 47PF 5% 25V NPO-C0G 201
R3893 10K 1% 1/20W MF 201
R3892 73.2K 1% 1/20W MF 201 <R2>
C3893 3300PF 10% 10V X7R 201
R3894 41.2K 1% 1/20W MF 201
C3894 0.33UF 10% 6.3V CERM-X5R 402
C3888 10PF 5% 50V CERM 402
R3895 133K 1% 1/16W MF-LF 402 <Ra>
NO STUFF C3889 100PF 5% 50V CERM 402
R3896 15.8K 1% 1/16W MF-LF 402 <Rb>
C3895 4.7UF 10% 50V X7R-CERM 1206
C3896 4.7UF 10% 50V X7R-CERM 1206
C3897 4.7UF 10% 50V X7R-CERM 1206
C3898 4.7UF 10% 50V X7R-CERM 1206
C3899 0.001UF 10% 50V X7R 402

T29BST_PWREN_DIV_L, T29BST_PWREN_L, T29_A_HV_EN, T29BST_EN_UVLO, T29BST_INTVCC, T29BST_VC, T29BST_RT, T29BST_SS, T29BST_VC_RC, T29BST_SNS1, T29BST_SNS2, T29BST_VSNS, T29BST_FBX, GND_T29BST_SGND, SGND, GND

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

=PP15V_T29_REG
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

Vout = 1.6V * (1 + Ra / Rb)

SGND shorted to GND inside package, no XW necessary.

Q3888 SSM6N37FEAPE SOT563
R3888 330K 5% 1/20W MF 201
Max Vgs: 10V
T29BST_SHDN_DIV
R3887 330K 5% 1/20W MF 201
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

=PP3V3_S0_T29PWRCTL
C3800 0.1UF 10% 16V X5R-CERM 0201
Platform (PCIe) Reset
=T29_RESET_L
R3803 10K 5% 1/20W MF 201
Open-Drain GPIO
T29_SW_RESET_L
T29_CLKREQ_L
Pull-up provided by SB page.

U3800 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD

=PP3V3_T29_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_T29
T29_RESET_L
DLY = 60 ms +/- 20%
=T29_CLKREQ_L
T29_CLKREQ_ISOL_L MAKE_BASE=TRUE

3.3V T29 Switch

=PP3V3_S0_P3V3T29FET
U3810 TPS22924 CSP
VIN, VOUT, ON, GND
C3810 1UF 10% 6.3V CERM 402
=PP3V3_T29_FET
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

=PP1V05_S0_P1V05T29FET
U3815 TPS22924 CSP
C3815 1UF 10% 6.3V CERM 402
=PP1V05_T29_FET
Max Current = 3.4A (85C)

U3816 TPS22924 CSP
T29_PWR_EN
U3816.A2: PLACE_NEAR=U3815.B2:3 mm
Pull-up provided by SB page.

SYNC MASTER=K78 MLB
SYNC DATE=01/10/2011
PAGE TITLE: T29 Power Support
Apple Inc.
DRAWING NUMBER: 051-8870
SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 38 OF 109
SHEET: 36 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

AIRPORT

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L OUT 6 41

70 6 PCIE_AP_R2D_N — C4030 0.1UF 10% 6.3V X5R 201 — PCIE_AP_R2D_C_N IN 16 70
PLACEMENT_NOTE=Place close to J4001.

70 6 PCIE_AP_R2D_P — C4031 0.1UF 10% 6.3V X5R 201 — PCIE_AP_R2D_C_P IN 16 70
PLACEMENT_NOTE=Place close to J4001.

PCIE_CLK100M_AP_N IN 6 16 70
PCIE_CLK100M_AP_P IN 6 16 70

PCIE_AP_D2R_P OUT 6 16 70
PCIE_AP_D2R_N OUT 6 16 70

PCIE_WAKE_L OUT 6 17

BLUETOOTH

USB_BT_N BI 6 24 69
USB_BT_P BI 6 24 69

=PP3V3_S3_BT 6 7

C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.18:1.5mm

MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

PP3V3_WLAN_F 1 — R4052 0.020 1% 0.25W MF-LF 805 — 2 PP3V3_WLAN_R

C4021 0.1UF 10% 6.3V X5R 201
C4020 10UF 20% 10V X5R 603
PLACEMENT_NOTE=Place close to Q4050.

CRITICAL
Q4050
TPCP8102
23V1K-SM

C4050 0.1UF 10% 16V X5R-CERM 0201
C4051 0.033UF 10% 16V X5R 402
R4050 100K 5% 1/20W MF 201
R4051 10K 5% 1/20W MF 201

=PP3V3_S3_WLAN 7 37
P3V3WLAN_SS
PM_WLAN_EN_L IN 42

ISNS_AIRPORT_P OUT 46 74
ISNS_AIRPORT_N OUT 46 74

DLY = 60 MS +/- 20%

CRITICAL
U4002
SLG4AP016V
TDFN
VDD
SENSE
0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND

R4053 100K 1% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
R4055 100K 1% 1/20W MF 201

P3V3WLAN_VMON
6 AP_RESET_CONN_L
6 AP_CLKREQ_Q_L

AP_RESET_L IN 25
AP_PWR_EN IN 18 62
AP_CLKREQ_L_R — R4090 0 5% 1/20W MF 201 — AP_CLKREQ_L OUT 16 23

C4053 0.1UF 10% 6.3V X5R 201

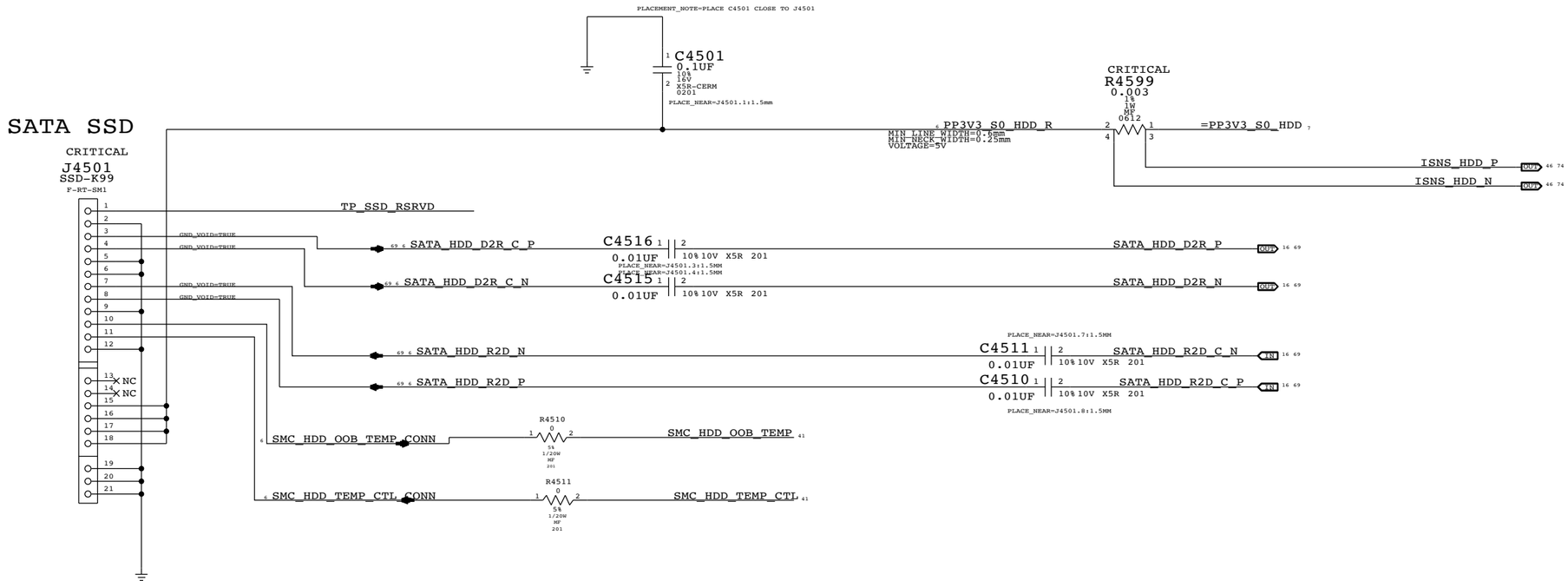
SYNC MASTER=K21 MLB
SYNC DATE=12/13/2010

PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 40 OF 109
SHEET 37 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=K78 MLB | SYNC DATE=01/10/2011

PAGE TITLE

SATA CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8870 | SIZE D

REVISION 3.13.0

BRANCH

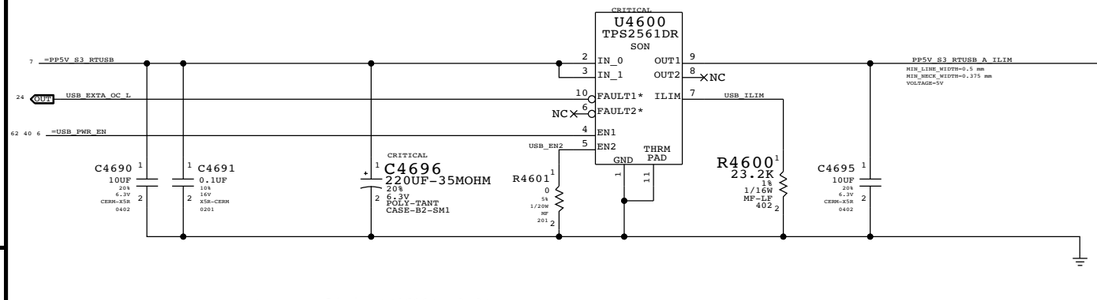
PAGE 45 OF 109

SHEET 38 OF 75

NOTICE OF PROPRIETARY PROPERTY:

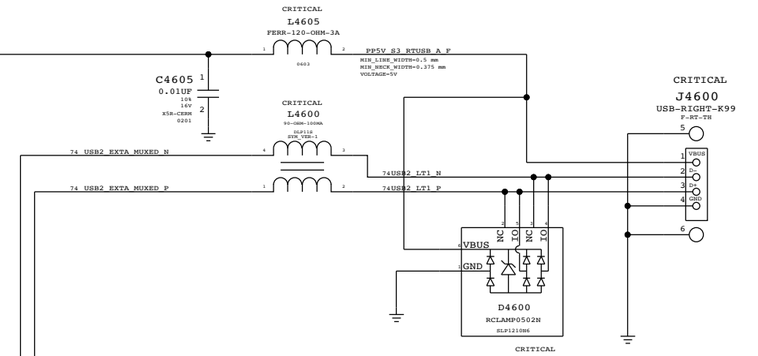
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

USB Port Power Switch



Current limit (R4600): 2.3A max

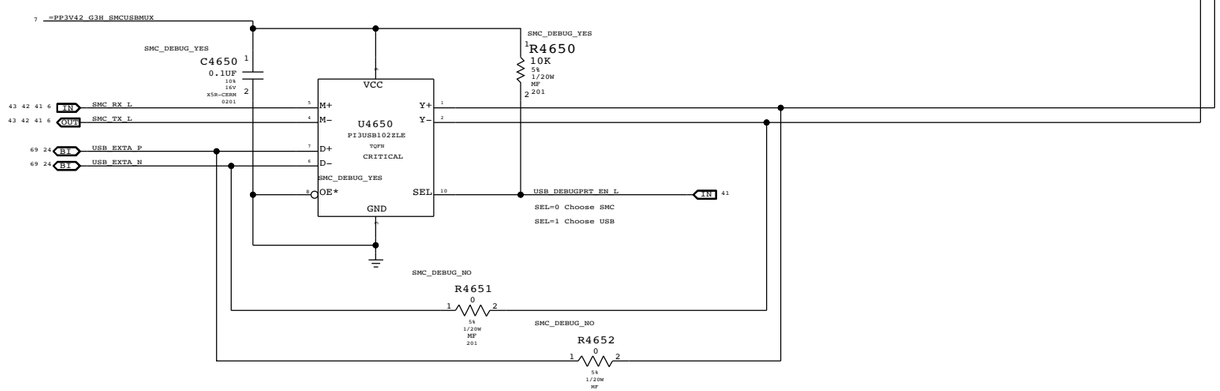
Right USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4605 at connector pin

USB/SMC Debug Mux



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

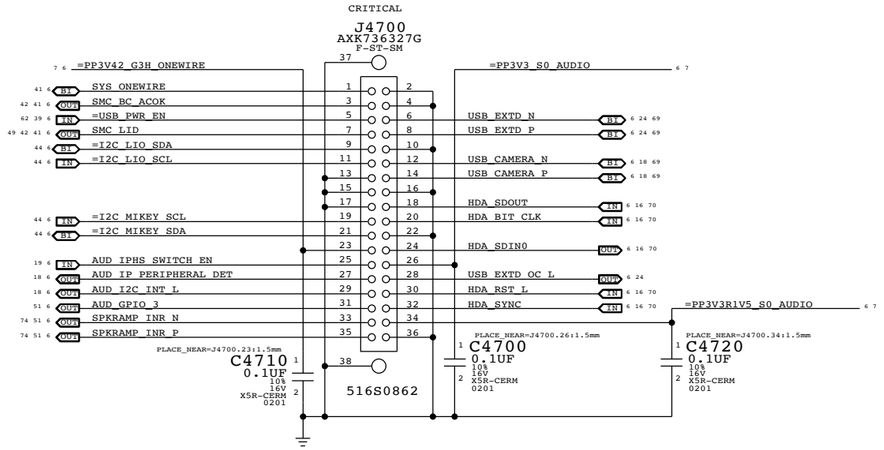
PAGE 46 OF 109

SHEET 39 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

(Right Speaker Enable)



SYNC MASTER=K21 MLB | SYNC DATE=11/09/2010

PAGE TITLE: Left I/O (LIO) Connector

Apple Inc.

DRAWING NUMBER: 051-8870 | SIZE: D

REVISION: 3.13.0

BRANCH:

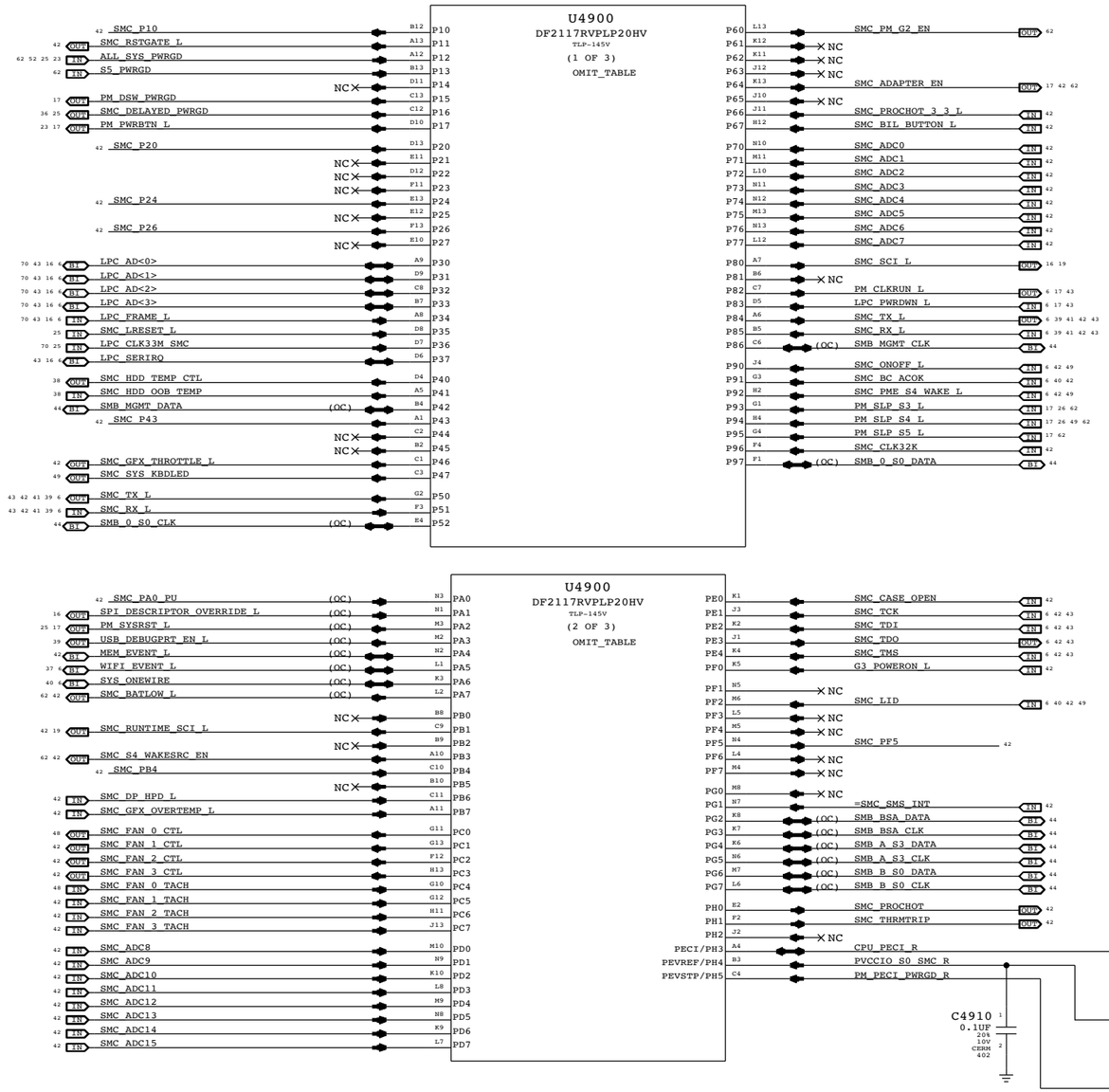
PAGE: 47 OF 109

SHEET: 40 OF 75

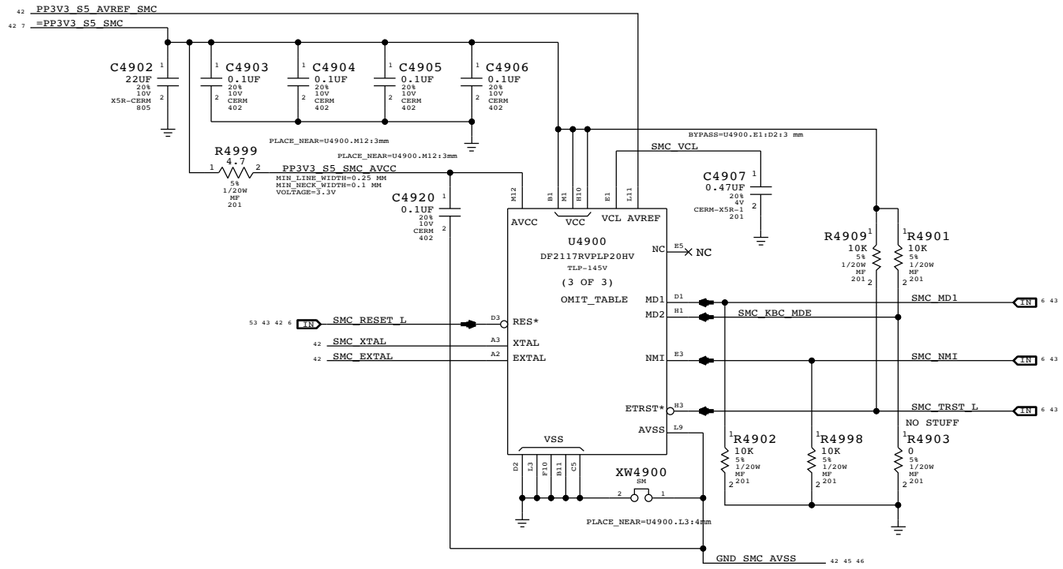
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



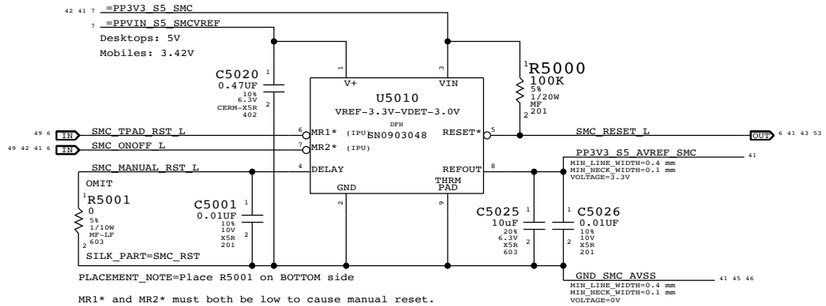
NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC MASTER=K78 MLB	SYNC DATE=01/10/2011
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 49 OF 109
	SHEET 41 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

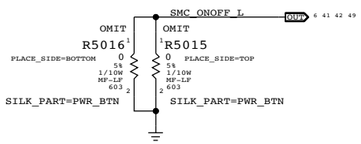
SMC Reset "Button", Supervisor & AVREF Supply



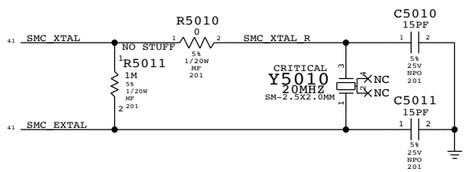
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

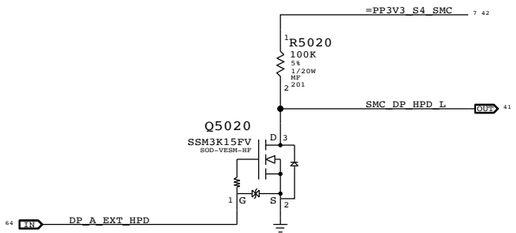
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

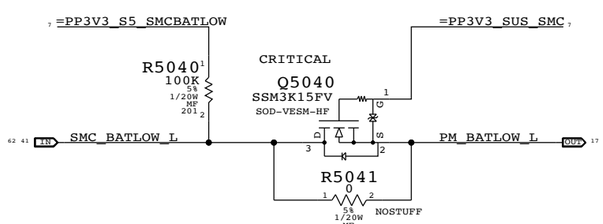


SMC Crystal Circuit





BATLOW# Isolation

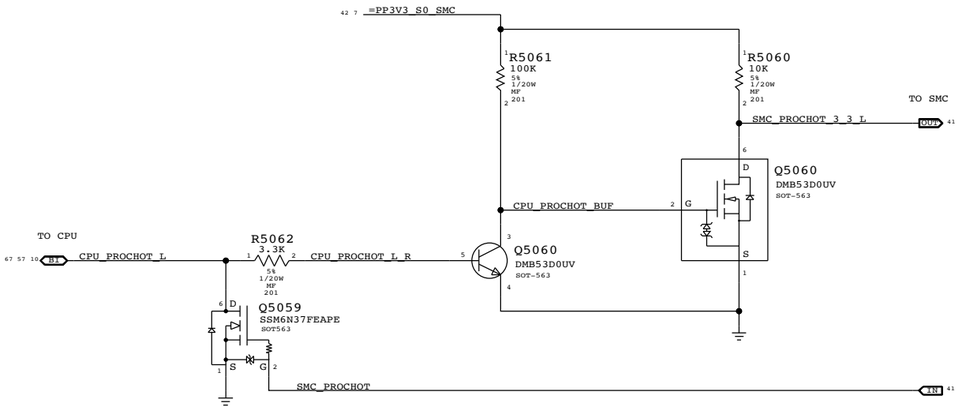


Internal 20K pull-up on PM_BATLOW_L in PCH.

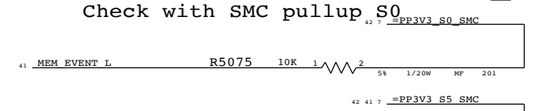
SMC Fan & Temp Signals

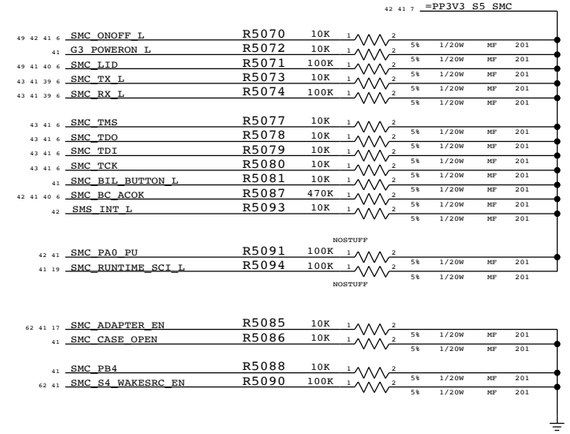
SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE
SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE
SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE
SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE
=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
=SMC_SMS_INT	SMS_INT_L	MAKE_BASE=TRUE
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_1V583_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_WLAN_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_HDD_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC13	TP_SMC_ADC13	MAKE_BASE=TRUE
SMC_ADC15	TP_SMC_ADC15	MAKE_BASE=TRUE
SMC_P10	TP_SMC_P10	MAKE_BASE=TRUE
SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE
SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE
SMC_P26	SMC_BMON_MUX_SEL	MAKE_BASE=TRUE
SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE
SMC_PF5	TP_SMC_PF5	MAKE_BASE=TRUE
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE

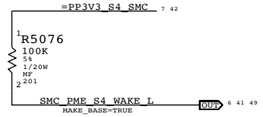
PROCHOT Level Shifting to 3V3



Check with SMC pullup S0

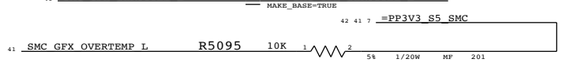






Below connections are different from K91

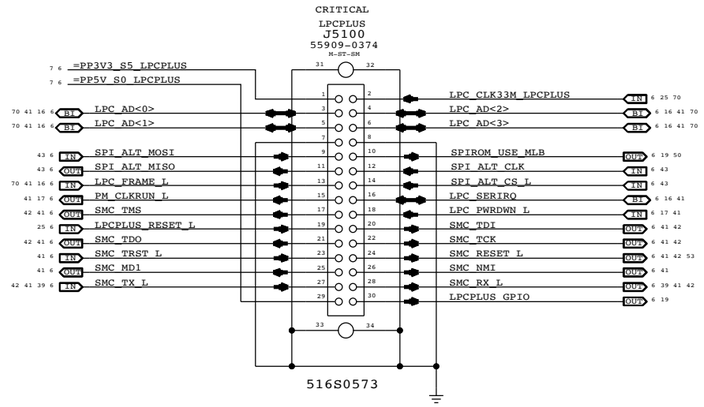
SMC_PA0_PU	HISIDE_ISENSE_OC	MAKE_BASE=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
SMC_ADC14	SMC_HS_COMPUTING_ISENSE	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	TP_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE



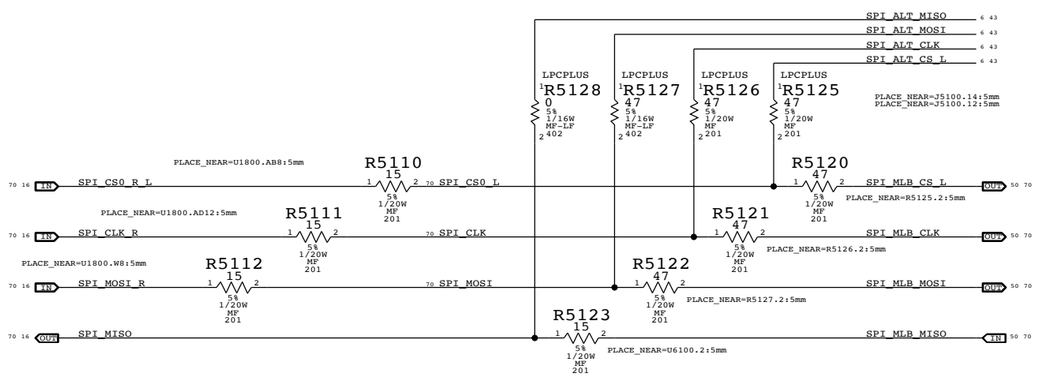
SYNC MASTER=K78 MLB	SYNC DATE=01/10/2011
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 50 OF 109
	SHEET 42 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=K78 MLB | SYNC DATE=01/10/2011

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8870 | SIZE: D

REVISION: 3.13.0

BRANCH:

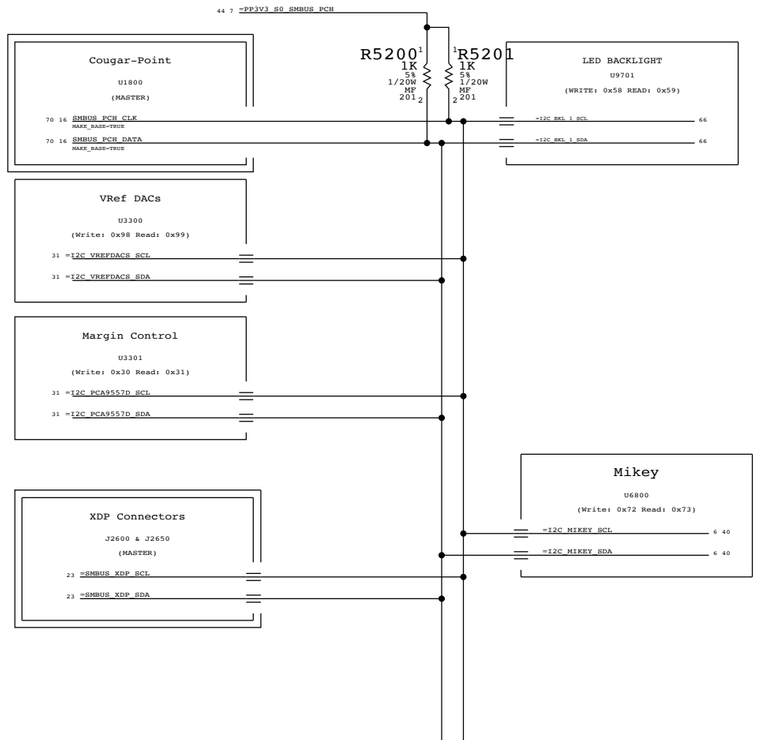
PAGE: 51 OF 109

SHEET: 43 OF 75

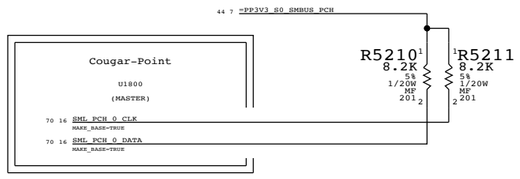
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

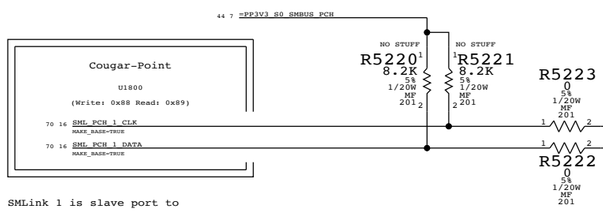
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

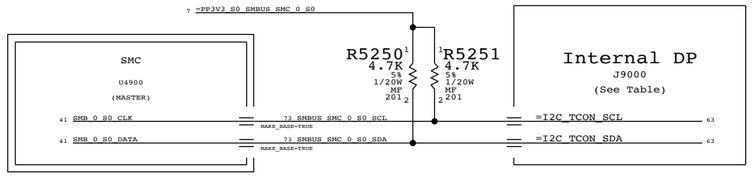


PCH "SMLink 1" Connections



SMLink 1 is slave port to
access PCH & CPU via PECI.

SMC "0" SMBus Connections



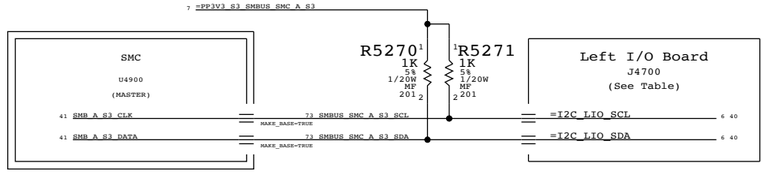
(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con – (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con – (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR – (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "A" SMBus Connections

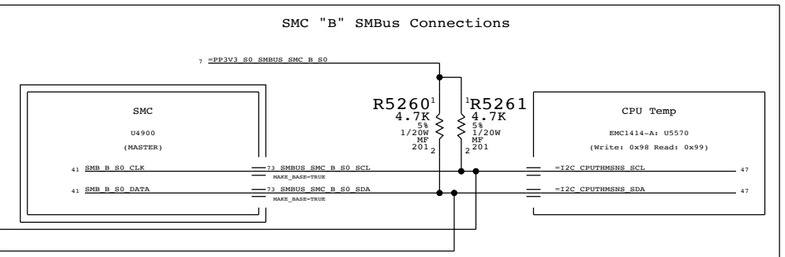
NOTE: SMC RMT bus remains powered and may be active in S3 state



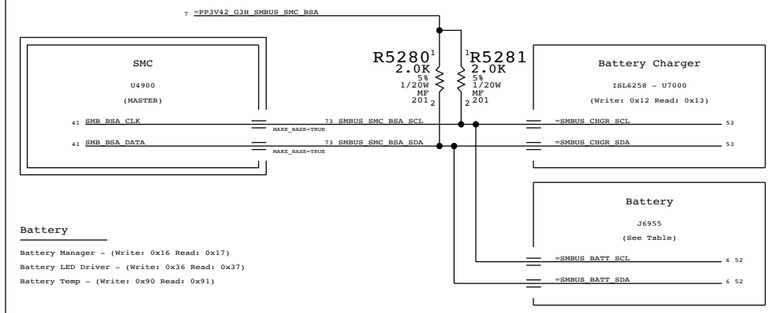
Left I/O Board

ALS – (write: 0x72 Read: 0x73)
Finstack Temp – (Write: 0x92 Read: 0x93)

SMC "B" SMBus Connections



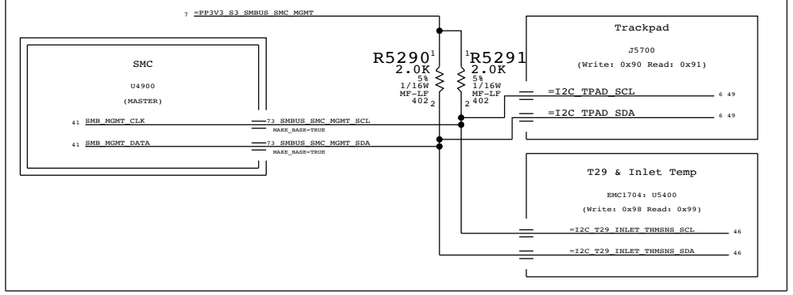
SMC "Battery A" SMBus Connections



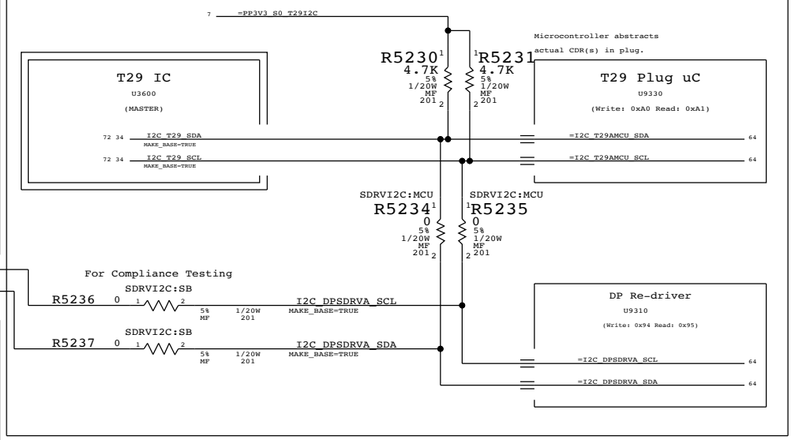
Battery

Battery Manager – (Write: 0x16 Read: 0x17)
Battery LED Driver – (Write: 0x36 Read: 0x37)
Battery Temp – (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections



T29 I2C Connections



SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

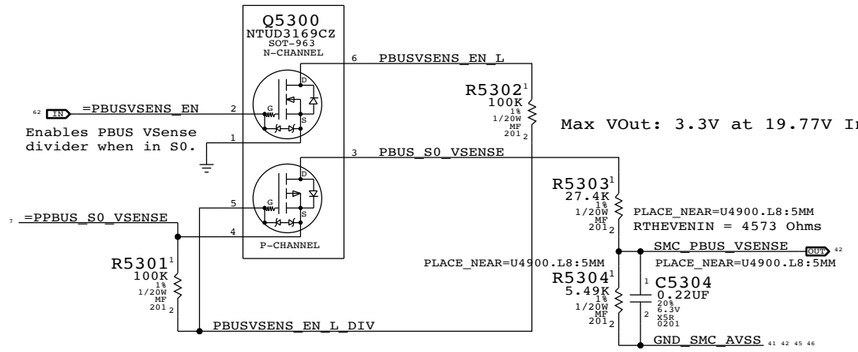
PAGE 52 OF 109

SHEET 44 OF 75

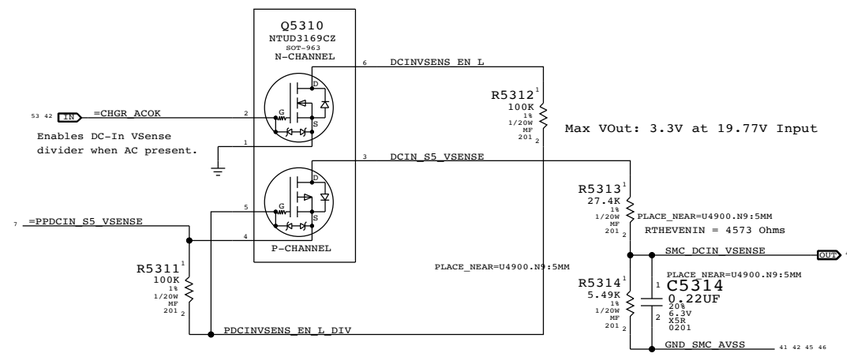
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

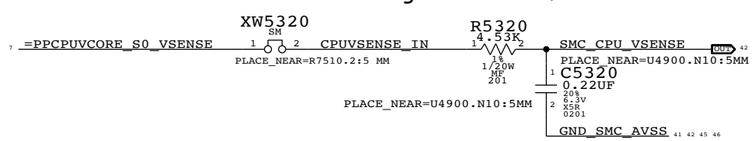
PBUS Voltage Sense Enable & Filter



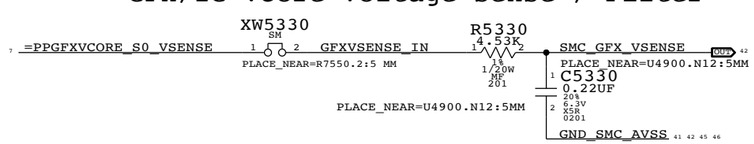
DC-In Voltage Sense Enable & Filter



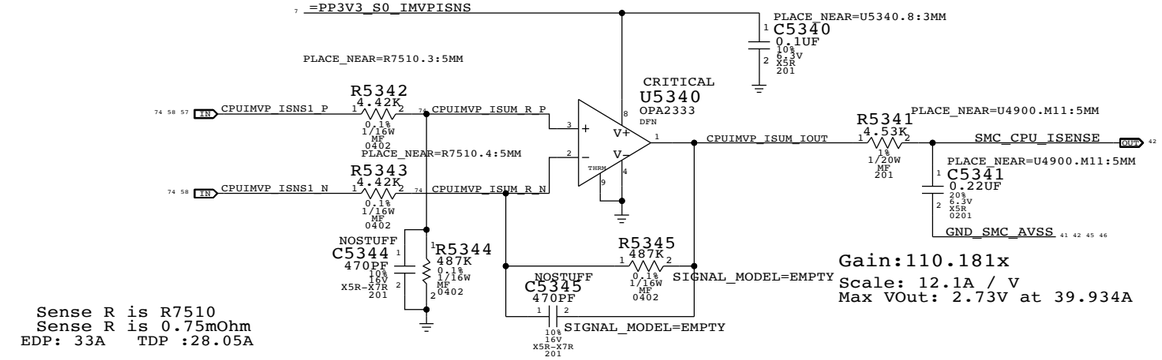
CPU Vcore Voltage Sense / Filter



GFX/IG Vcore Voltage Sense / Filter

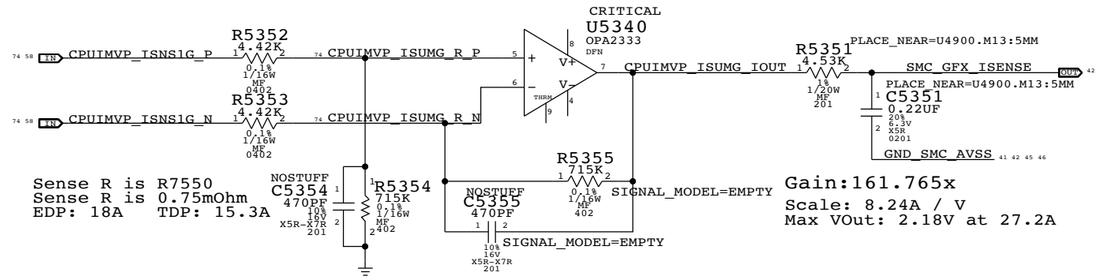


CPU VCore Load Side Current Sense / Filter



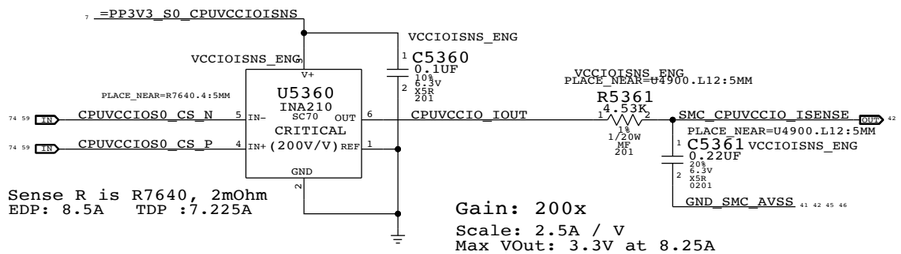
Sense R is R7510
Sense R is 0.75mOhm
EDP: 33A TDP :28.05A

GFX/IG Load Side Current Sense / Filter



Sense R is R7550
Sense R is 0.75mOhm
EDP: 18A TDP: 15.3A

CPU 1.05V VCCIO Current Sense / Filter



Sense R is R7640, 2mOhm
EDP: 8.5A TDP :7.225A

SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

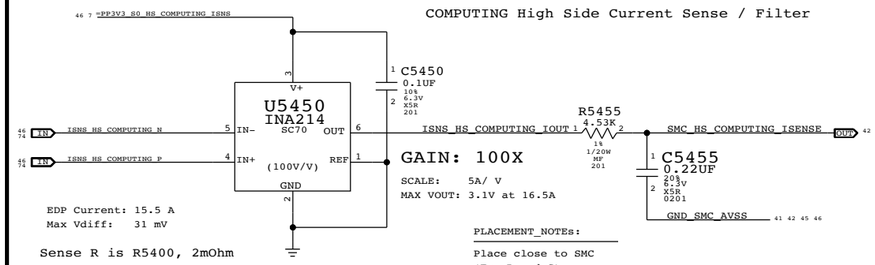
PAGE TITLE
Voltage & Load Side Current Sensing

Apple Inc.

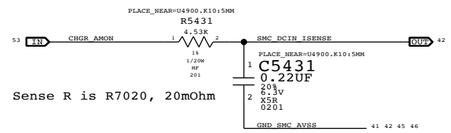
DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 53 OF 109
SHEET 45 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

COMPUTING High Side Current Sense / Filter



DC-IN (AMON) Current Sense Filter



DC-In AMON

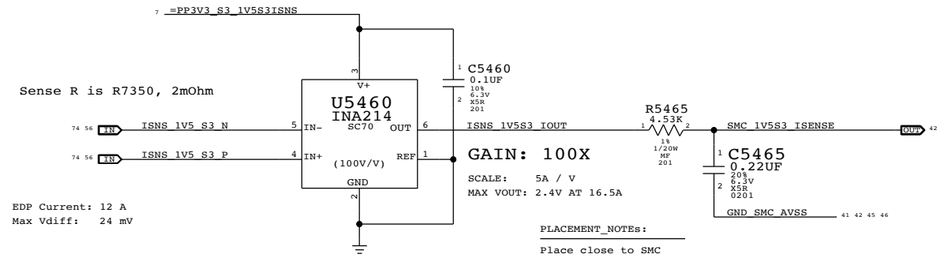
ISL6259 Gain: 20x

Scale: 2.5A / V

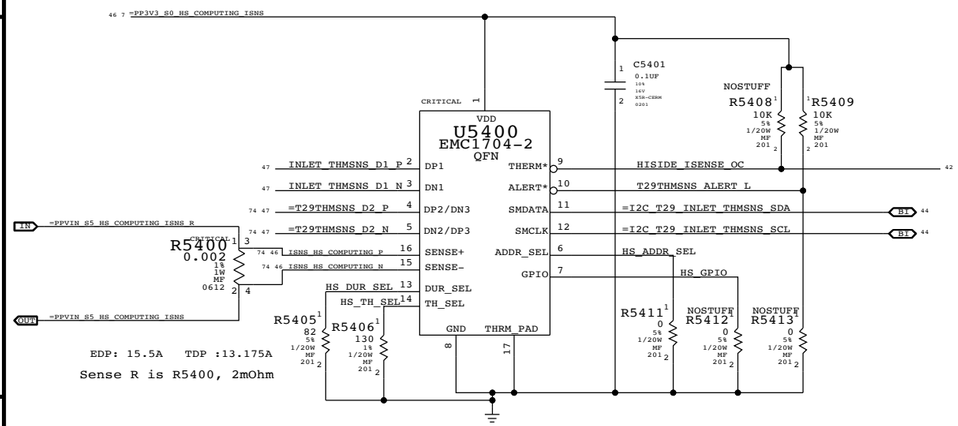
Max VOut: 1.4V at 8.25A

EDP Current: 3.5A

DDR3 1V5R1V35 Current Sense / Filter

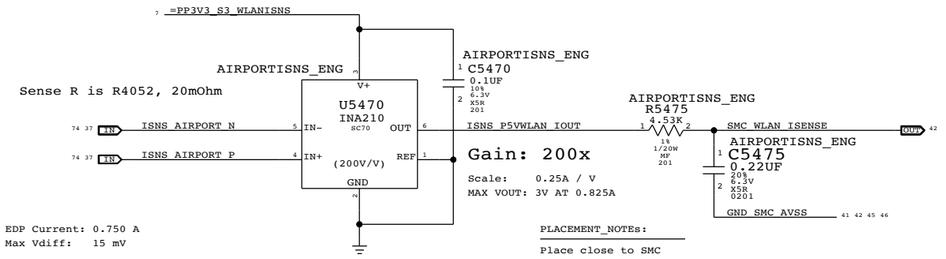


COMPUTING High Side Current Sense / Filter & T29/Inlet Temp Sensor

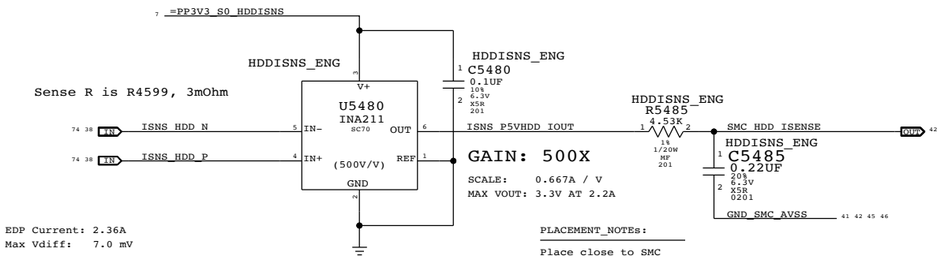


Write Address: 0x98
Read Address: 0x99

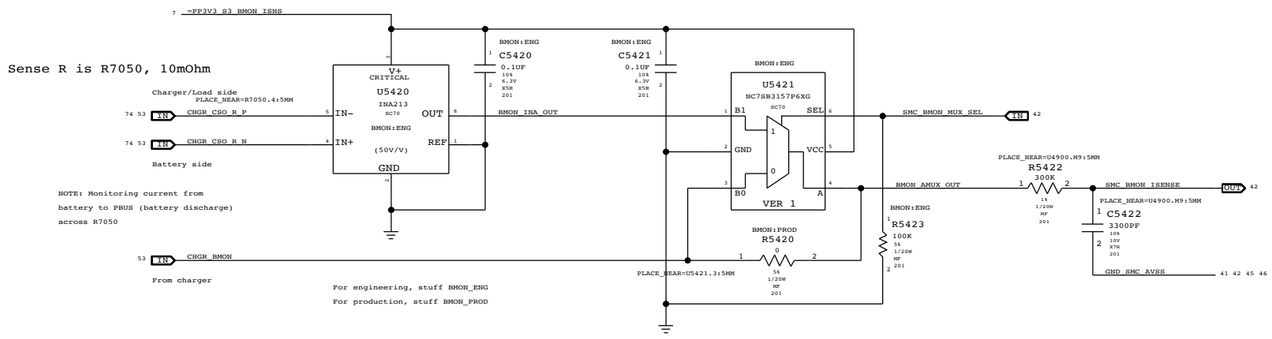
AirPort Current Sense / Filter



HDD Current Sense / Filter



CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



INA (Engineering) Solution

Gain: 50x

Scale: 2A / V

Max VOut: 3.3V at 6.6A

EDP Current: 10A

Charger BMON (Production) Solution

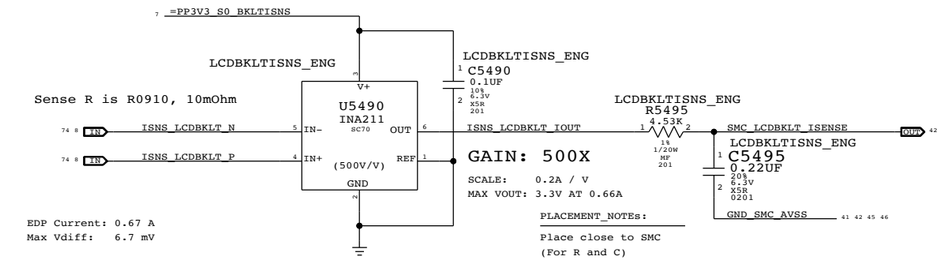
ISL6259 Gain: 36x

Scale: 2.78A / V

Max VOut: 3.3V at 9.167A

EDP Current: 310A

LCD Backlight Driver Input Current Sense / Filter



SYNC_MASTER=K78_MLB SYNC_DATE=01/16/2013

PAGE TITLE: High Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

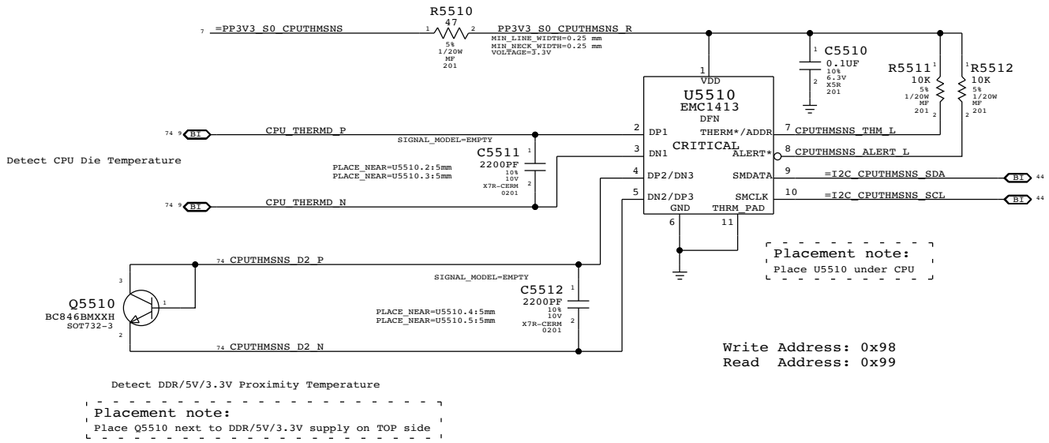
PAGE: 54 OF 109

SHEET: 46 OF 75

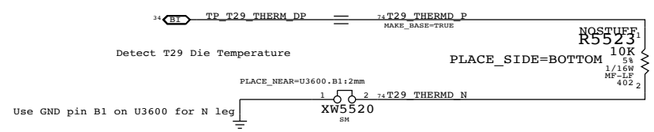
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU Proximity Sensor



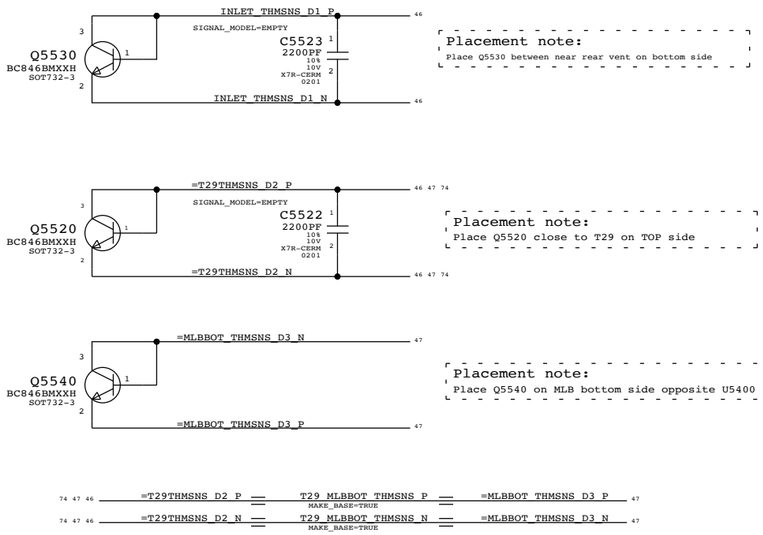
T29 Die



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

T29,MLB Bottom & Inlet Proximity Sensors



NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

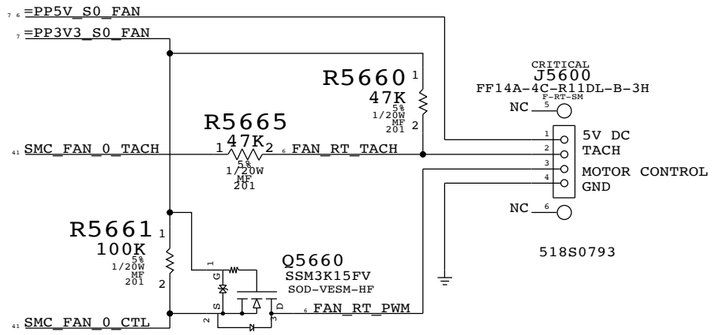
SYNC MASTER=K78 MLB
SYNC DATE=01/16/2011

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-8870
SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 55 OF 109
SHEET: 47 OF 75

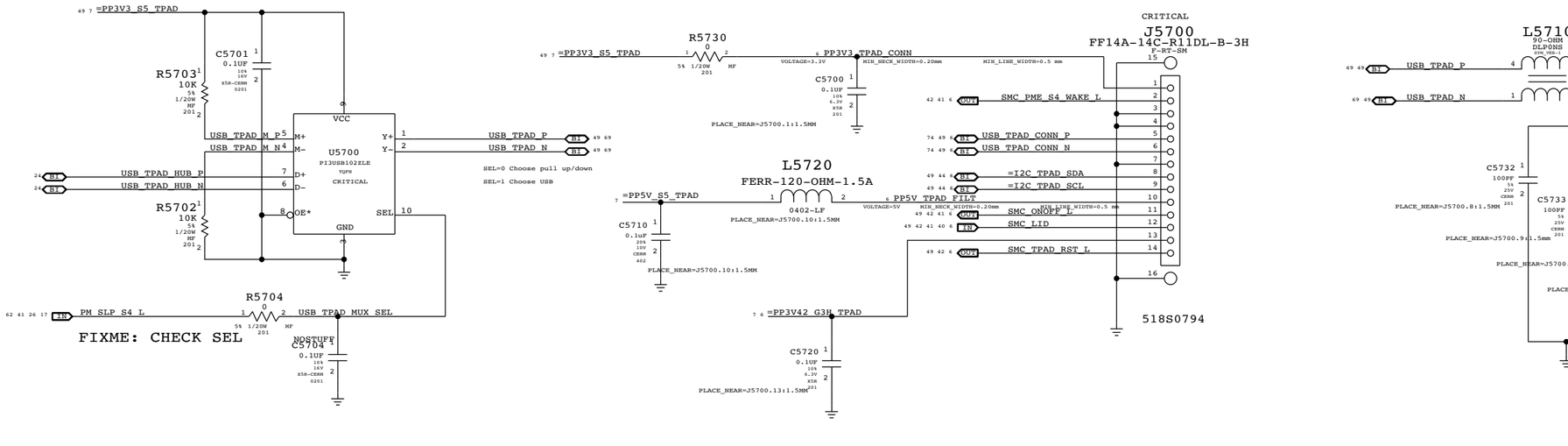
FAN CONNECTOR



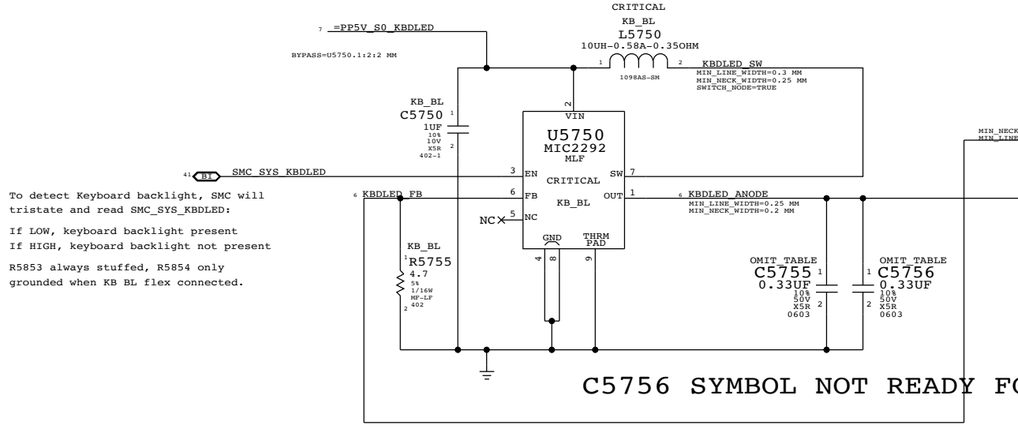
SYNC MASTER=K78 MLB	SYNC DATE=01/10/2011
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: 051-8870 SIZE: D
	REVISION: 3.13.0
	BRANCH:
	PAGE: 56 OF 109
	SHEET: 48 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

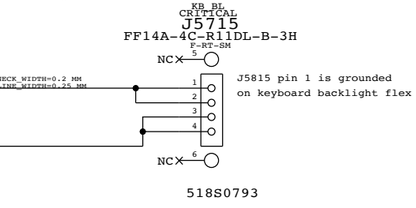
IPD Flex Connector



Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



C5756 SYMBOL NOT READY FOR 0.22UF

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP,CER,0.22UF,10%,50V,X5R,0603	C5755,C5756		KB_BL

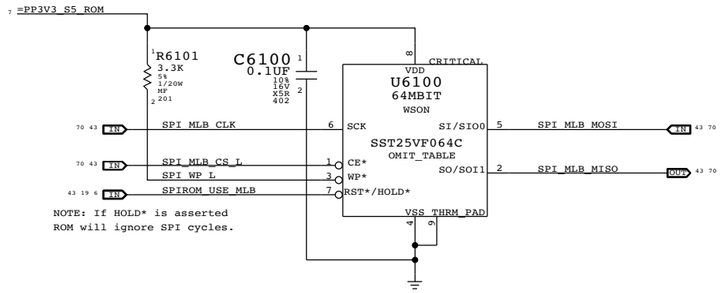
SYNC MASTER=K78 MLB
SYNC DATE=01/10/2011

PAGE TITLE
IPD / KBD Backlight

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 57 OF 109
SHEET 49 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



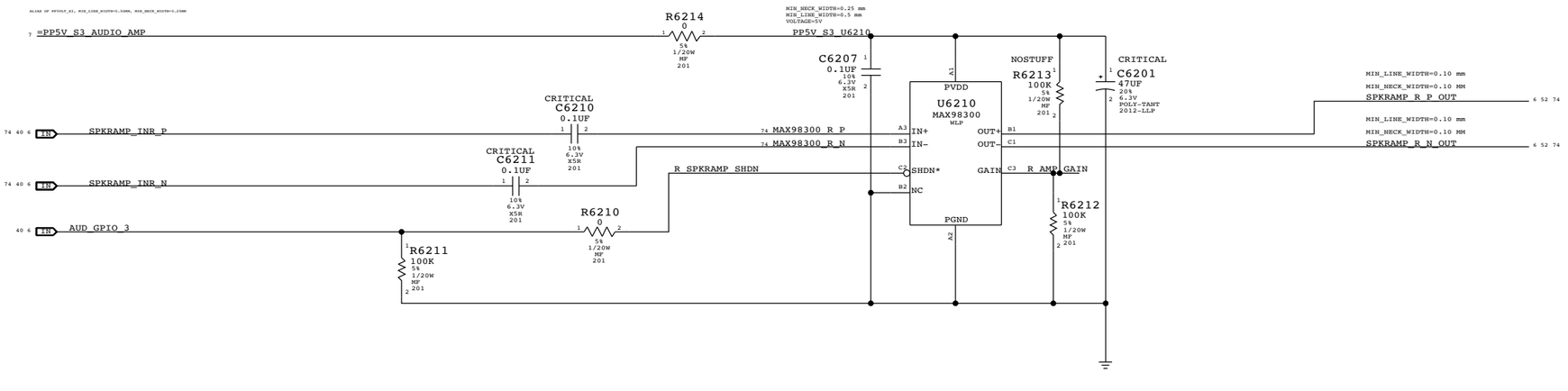
SYNC MASTER=K78 MLB	SYNC DATE=01/10/2011
PAGE TITLE: SPI ROM	
Apple Inc.	DRAWING NUMBER 051-8870 · SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 61 OF 109
	SHEET 50 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC MASTER=K78 MLB SYNC DATE=01/10/2011

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 62 OF 109

SHEET 51 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

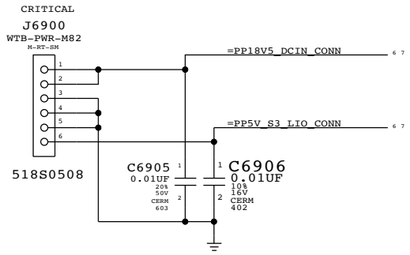
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

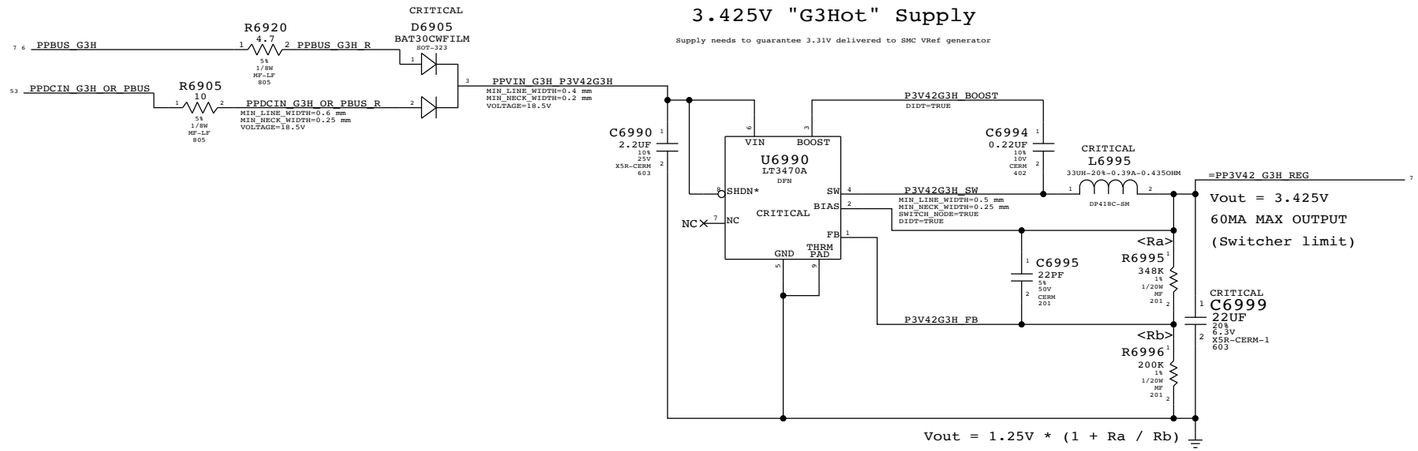
IV ALL RIGHTS RESERVED

MLB to LIO Power Cable Connector



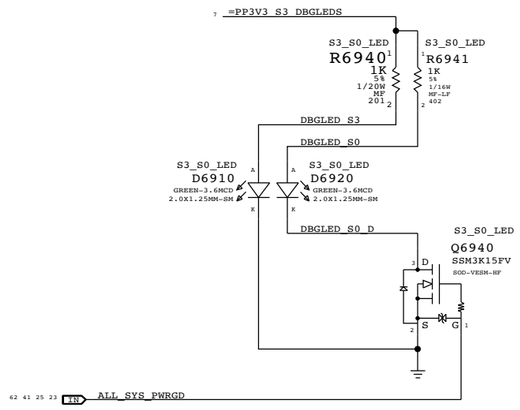
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

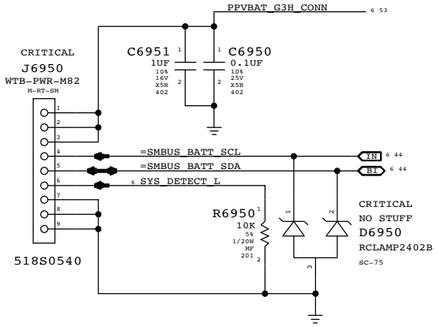


Debug LEDs

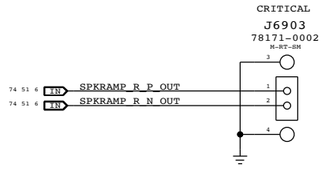
(For development only)



K16-Specific Battery Connector



Right Speaker Connector



SYNC_MASTER=JACK_K90I SYNC_DATE=08/20/2011

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

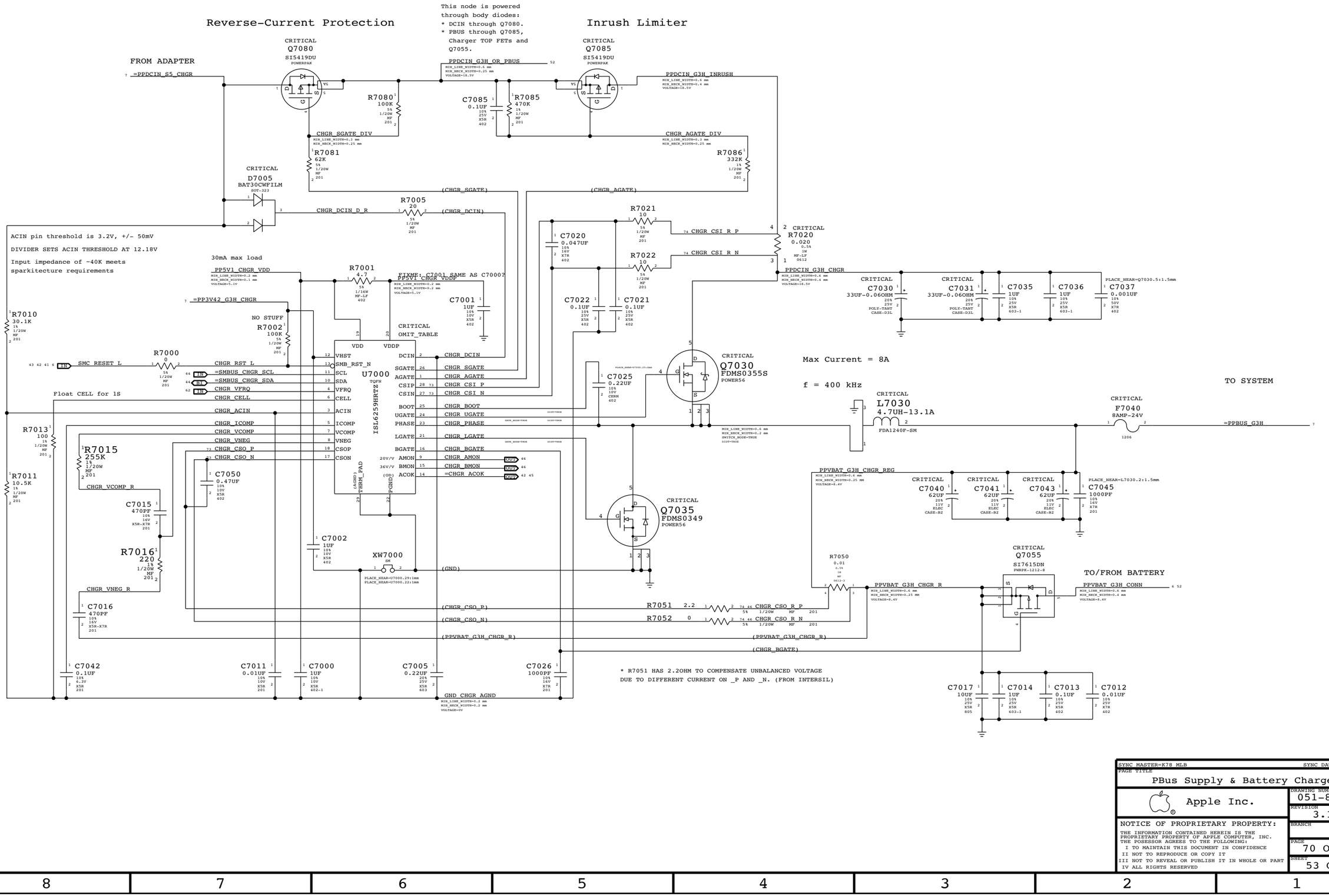
BRANCH

PAGE 69 OF 109

SHEET 52 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



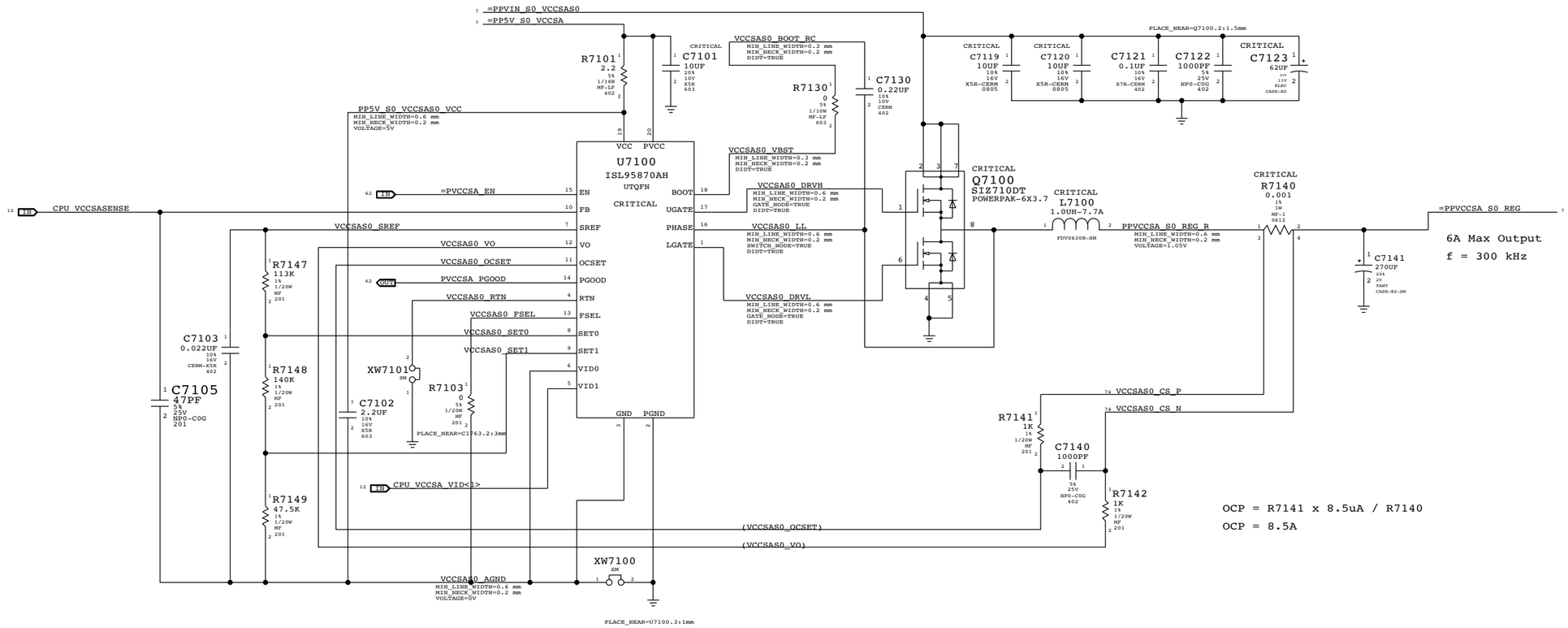
SYNC MASTER=K78 MLB
SYNC DATE=12/03/2010

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 70 OF 109
SHEET 53 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

SYNC MASTER=K78 MLB SYNC DATE=01/16/2011

PAGE TITLE

System Agent Supply

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

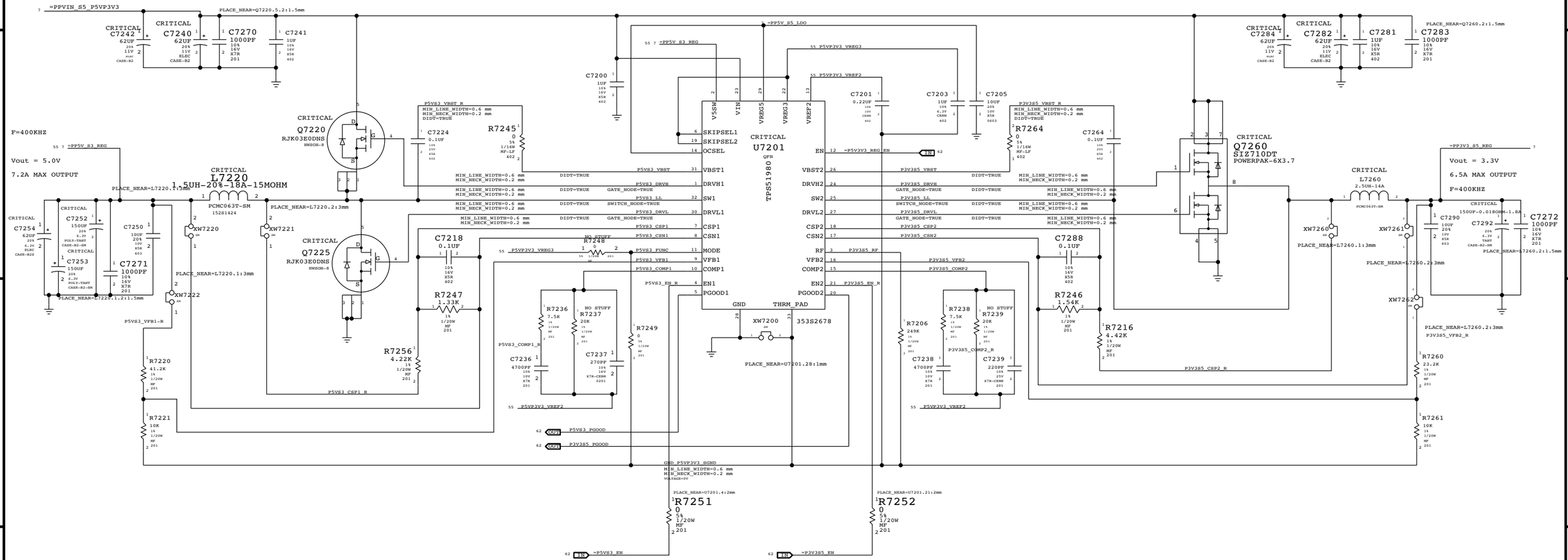
BRANCH

PAGE 71 OF 109

SHEET 54 OF 75

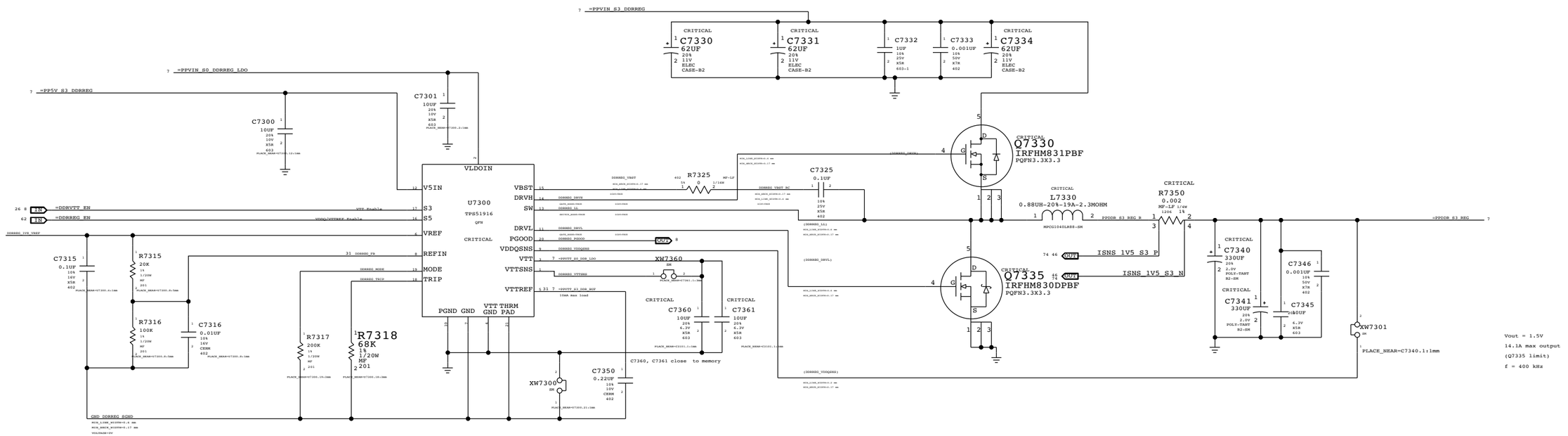
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



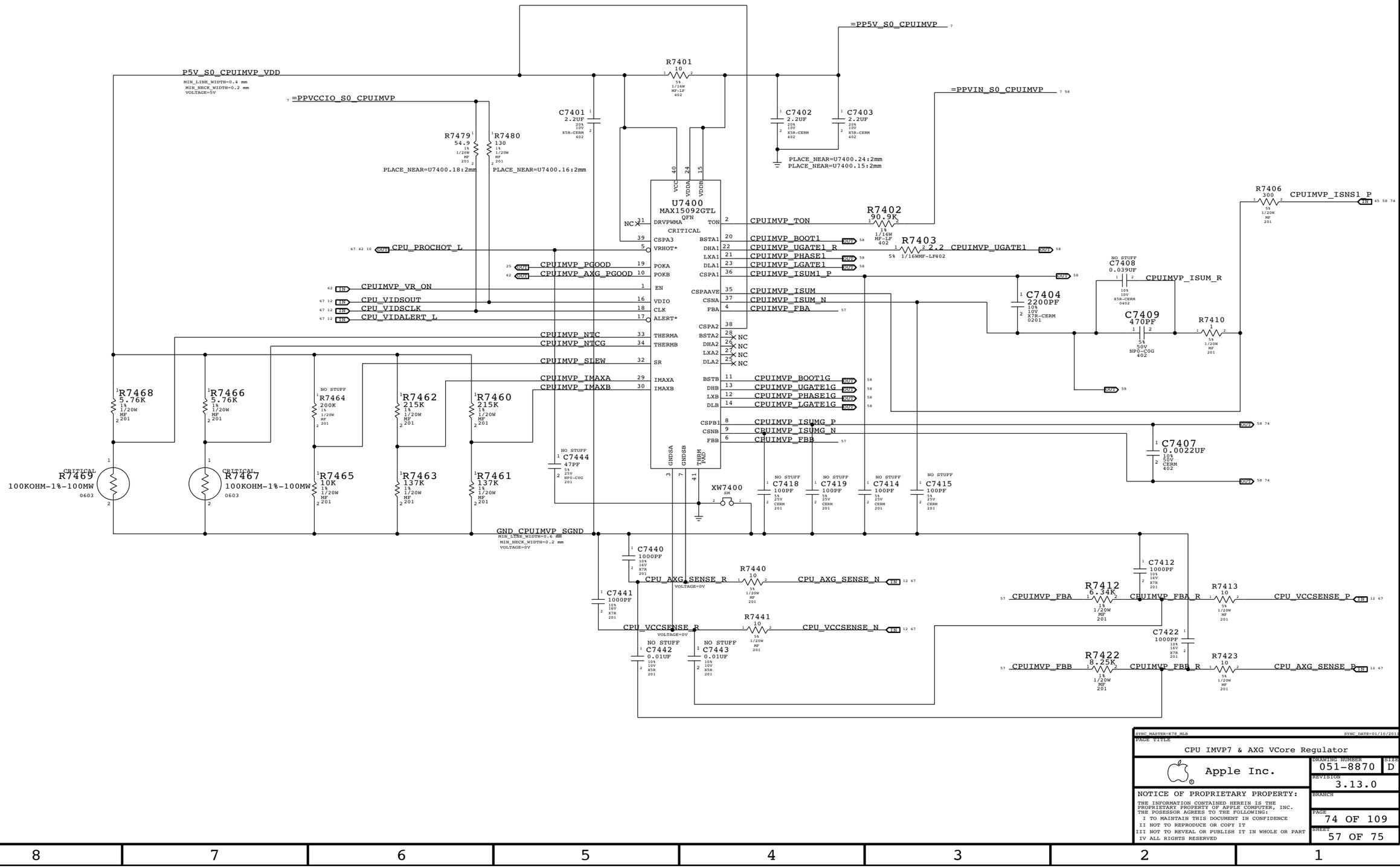
SYNC MASTER=K78_MLB	SYNC DATE=01/16/2011
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-8870 · SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 72 OF 109
	SHEET 55 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=K78_MLB	SYNC DATE=01/10/2012
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 73 OF 109
	SHEET 56 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 74 OF 109

SHEET 57 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

CPU=Sandy Bridge ULV, AXG=GT2

PHASE 1

=PPVIN_S0_CPUIMVP

C7513 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7514 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7515 10UF 20% 25V X5R-CERM 0603 — CRITICAL
C7516 10UF 20% 25V X5R-CERM 0603 — CRITICAL
C7517 1UF 10% 16V X5R 402 — THESE TWO CAPS ARE FOR EMC
C7518 0.001UF 10% 50V X7R 402
C7519 0.001UF 10% 50V X7R 402
C7540 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7541 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7510 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7520 62UF 20% 11V ELEC CASE-B2 — CRITICAL

CPUIMVP_BOOT1_RC
R7511 0 5% 1/16W MF-LF 402
C7511 0.22UF 10% 10V CERM 402

37680984 — CRITICAL
Q7510 IRF6811STRPBF SQ

CPUIMVP_BOOT1 (IN)
CPUIMVP_UGATE1 (IN)
CPUIMVP_PHASE1 (IN)
CPUIMVP_LGATE1 (IN)

L7510 — CRITICAL
0.36UH-20%-30A-1.2MOHM
PIMB104T-SM
15281323
PPVCORE_S0_CPU_PH1

R7510 0.00075 1% 1W MF 0612 — CRITICAL
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P (OUT)
R7513 46.4 1% 1/20W MF 201
R7514 10 1% 1/20W MF 201
CPUIMVP_ISUM_N (IN)
C7571 2200PF 10% 10V X7R-CERM 0201 — NO STUFF
CPUIMVP_ISUM1_P (IN)

37680985 — CRITICAL
Q7520 IRF6894MTRPBF DIRECTFET-MX

AXG PHASE

=PPVIN_S0_CPUAXG

C7553 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7554 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7555 10UF 20% 25V X5R-CERM 0603 — CRITICAL
C7556 10UF 20% 25V X5R-CERM 0603 — CRITICAL
C7557 1UF 10% 16V X5R 402 — THESE TWO CAPS ARE FOR EMC
C7558 0.001UF 10% 50V X7R 402
C7559 0.001UF 10% 50V X7R 402
C7560 62UF 20% 11V ELEC CASE-B2 — CRITICAL
C7561 62UF 20% 11V ELEC CASE-B2 — CRITICAL

CPUIMVP_UGATE1G_R
CPUIMVP_BOOT1G_RC
R7551 10 5% 1/16W MF-LF 402
C7551 0.22UF 10% 10V CERM 402

37680906 — CRITICAL
Q7550 CSD58864Q5D SON5X6
TG, TGR, BG, VIN, VSW, PGND

CPUIMVP_BOOT1G (IN)
CPUIMVP_UGATE1G (IN)
R7555 4.7 5% 1/16W MF-LF 402
CPUIMVP_PHASE1G (IN)
CPUIMVP_LGATE1G (IN)
CPUIMVP_VSWG

L7550 — CRITICAL
0.36UH-20%-30A-1.2MOHM
PIMB104T-SM
15281323
PPVCORE_S0_AXG_R

R7550 0.00075 1% 1W MF 0612 — CRITICAL
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
R7552 2.2 5% 1/10W MF-LF 603 — NOSTUFF
CPUIMVP_AXG_SNUB
C7552 0.001UF 10% 50V CERM 402 — NOSTUFF
R7553 46.4 1% 1/20W MF 201
R7554 10 1% 1/20W MF 201
CPUIMVP_ISUMG_N (IN)
C7574 1000PF 10% 16V X7R 201 — NO STUFF
CPUIMVP_ISUMG_P (IN)

SYNC_MASTER=K78_MLB — SYNC_DATE=12/07/2011

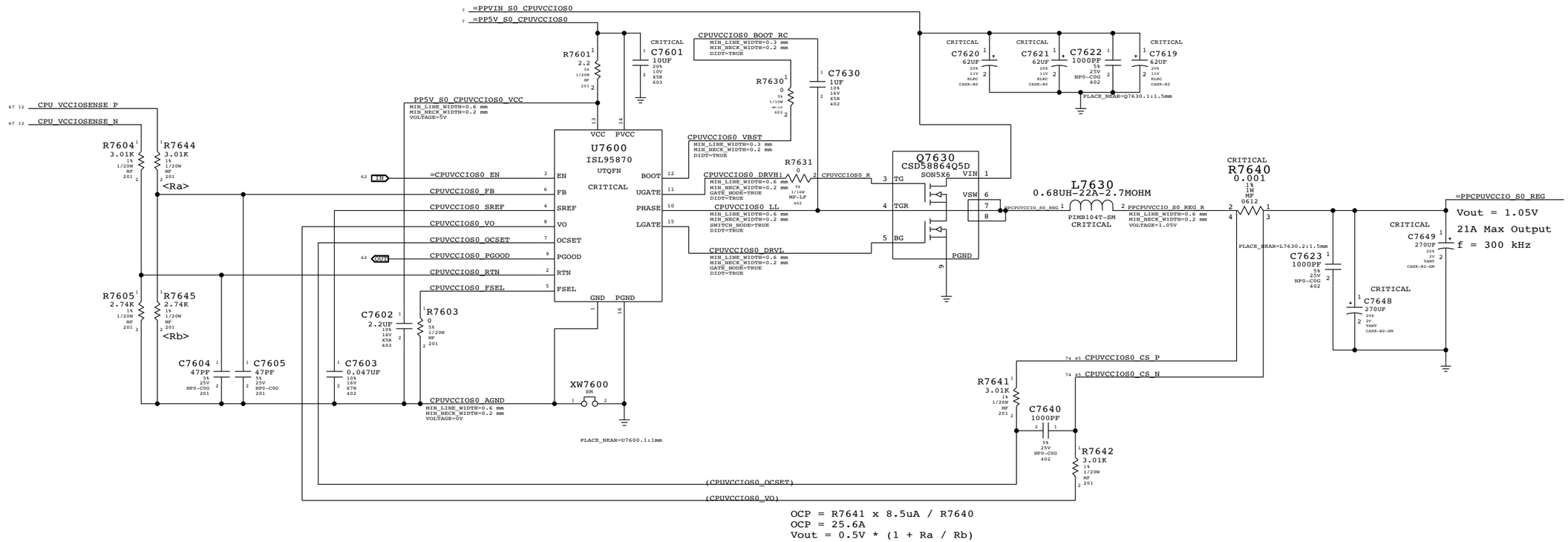
PAGE TITLE: CPU IMVP7 & AXG VCore Output

Apple Inc.

DRAWING NUMBER: 051-8870 — SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 75 OF 109
SHEET: 58 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE

CPU VCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

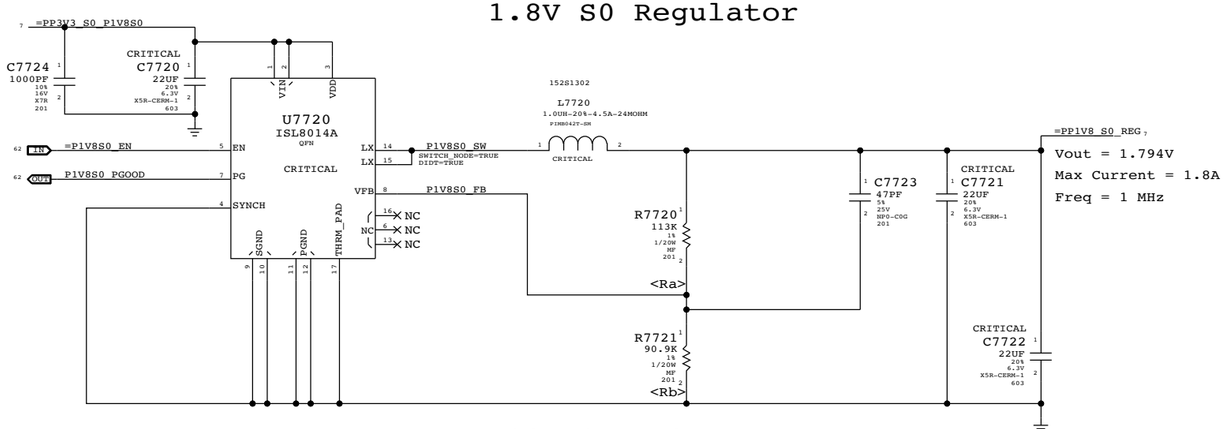
PAGE 76 OF 109

SHEET 59 OF 75

NOTICE OF PROPRIETARY PROPERTY:

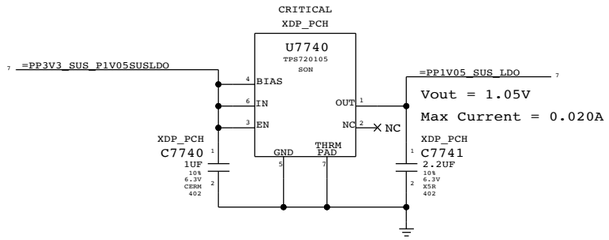
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.8V S0 Regulator

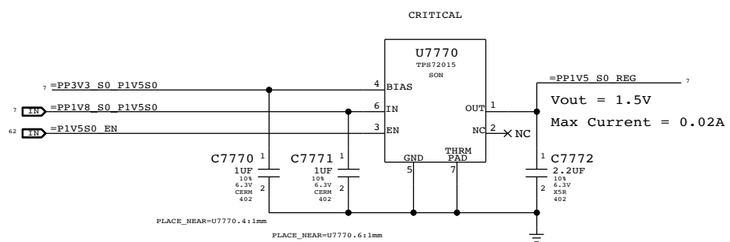


1.05V SUS LDO

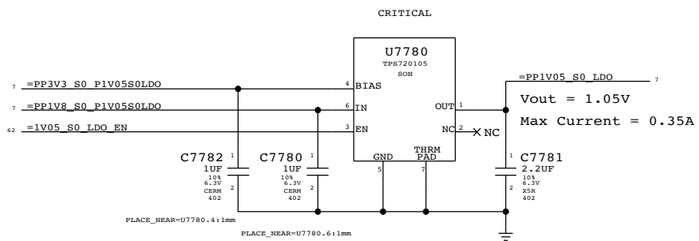
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC MASTER=K78 MLB
SYNC DATE=01/16/2011

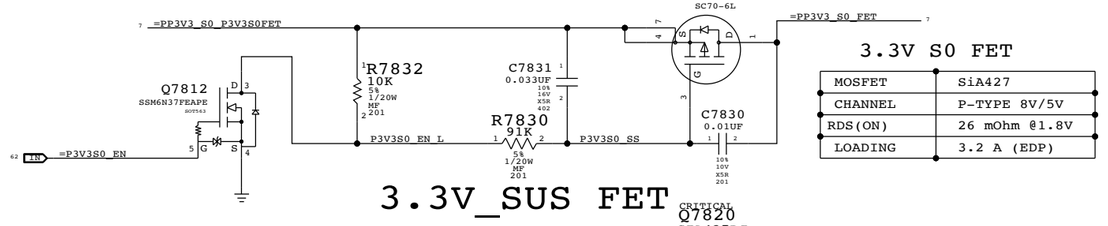
PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 77 OF 109
SHEET 60 OF 75

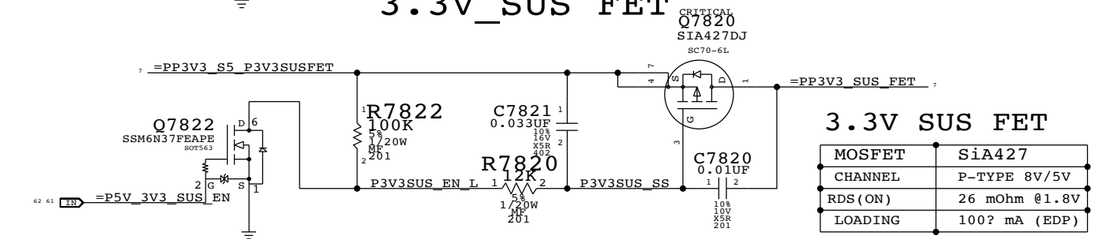
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

3.3V S0 FET



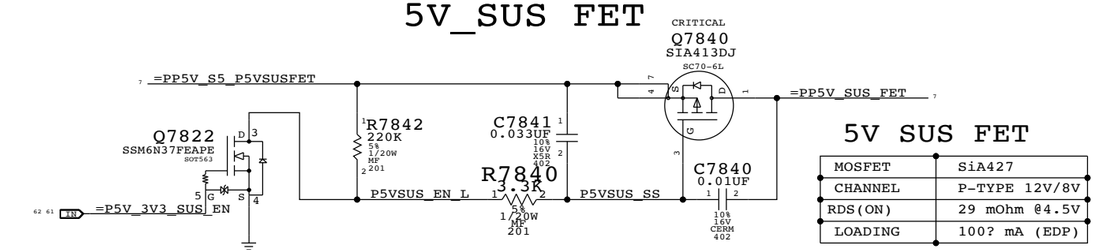
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V_SUS FET



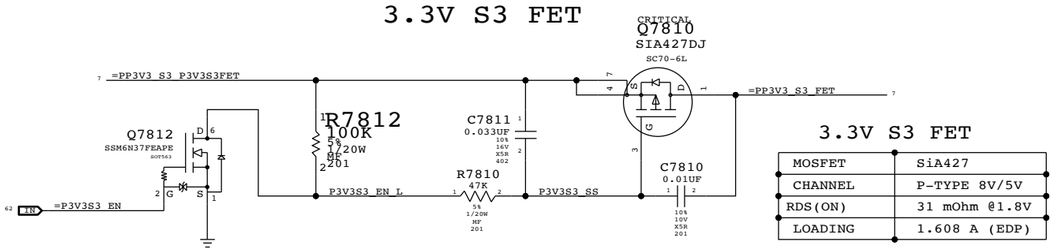
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



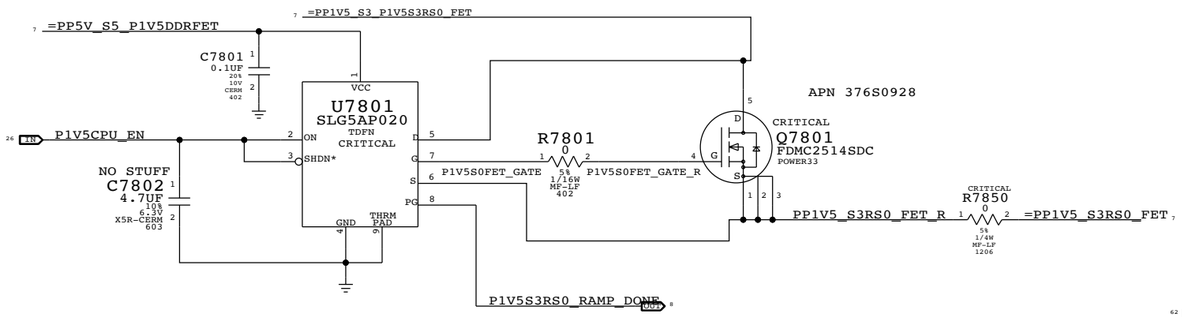
5V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

3.3V S3 FET



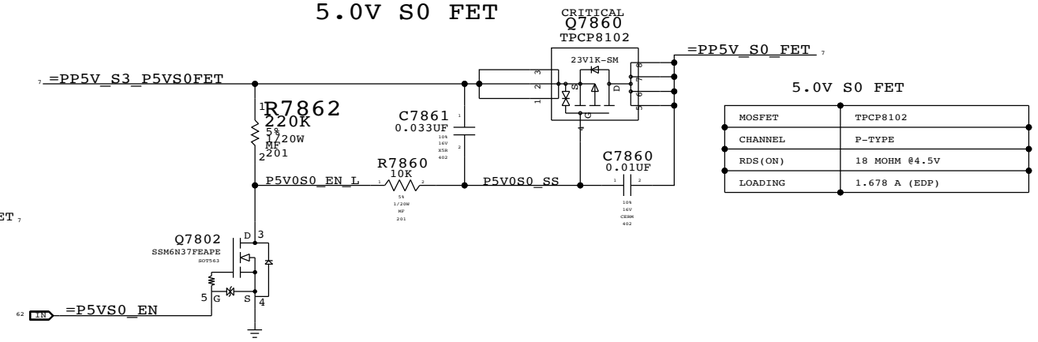
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET



1.5V S3/S0 FET	
MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=K78 MLB SYNC DATE=01/10/2011

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 78 OF 109

SHEET 61 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

S5 Rail Enables & PGOOD

Internal pull-ups 100K +/- 20%

=PP3V42_G3H_PWRCTL

C7940 0.1UF 10% 6.3V X5R 201

U7941 SLG4AP012 TDFN — CRITICAL 343S0497

SMC_PM_G2_EN (MAKE_BASE=TRUE)

=PP3V3_S5_PWRCTL

Threshold: ??

DLY > 10 ms

S5PGOOD_DLY

C7941 220PF 10% 25V X7R-CERM 201

R7941 100 5% 1/20W MF 201

C7942 0.033UF 10% 16V X5R 402 — NO STUFF

P3V3S5_EN (MAKE_BASE=TRUE) → =P3V3S5_EN OUT

P3V3_S5_REG_EN (MAKE_BASE=TRUE) → =P5V3V3_REG_EN OUT

S5_PWRGD (MAKE_BASE=TRUE) OUT

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V S4 ENABLE

PM_SLP_S5_L

R7915 100K 5% 1/20W MF 201

Delete R when pull-down added to PCH page

3.3V,5V S3 ENABLE

Delete R when pull-down added to PCH page

PM_SLP_S4_L (MAKE_BASE=TRUE)

R7910 100K 5% 1/20W MF 201

R7911 5.1K 5% 1/20W MF 201

R7912 9.1K 5% 1/20W MF 201

R7913 0 5% 1/20W MF 201 — P5VS3_EN (MAKE_BASE=TRUE) → =P5VS3_EN OUT

NO STUFF C7913 0.068UF 10% 10V CERM 402

PLACE_NEAR=U7300.16:6mm

PLACE_NEAR=Q7812.2:6mm

P3V3S3_EN (MAKE_BASE=TRUE) → =P3V3S3_EN OUT

DDRREG_EN (MAKE_BASE=TRUE) → =DDRREG_EN OUT

=USB_PWR_EN OUT

C7910 0.47UF 10% 6.3V CERM-X5R 402

C7912 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

ALL_SYS_PWRGD

R7974 0 5% 1/20W MF 201 — PLACE_NEAR=U7400.1:5mm

CPUIMVP_VR_ON OUT

PLACE_NEAR=U7400.1:5mm

R7976 0 5% 1/20W MF 201

NO STUFF R7975 0 5% 1/20W MF 201 — PLACE_NEAR=U7400.1:5mm

CPUVCCIOS0_PGOOD → PM_PECI_PWRGD OUT

S0 ENABLE

PM_SLP_S3_L

R7978 100 5% 1/20W MF 201

R7979 100K 5% 1/20W MF 201 — PLACE_NEAR=U1800.B4:5mm

Delete R when pull-down added to PCH page

(PM_SLP_S3_R_L)

PM_SLP_S3_R_L (MAKE_BASE=TRUE)

R7987 33K 5% 1/20W MF 201 — PLACE_NEAR=U7100.15:6mm

R7981 20K 5% 1/20W MF 201 — PLACE_NEAR=U7600.3:6mm

R7988 39K 5% 1/20W MF 201 — PLACE_NEAR=U7770.3:6mm

R7986 5.1K 5% 1/20W MF 201 — PLACE_NEAR=U7720.5:6mm

=P5VS0_EN OUT

=P3V3S0_EN OUT

=PBUSVSENS_EN OUT

P1V8S0_EN (MAKE_BASE=TRUE) → =P1V8S0_EN OUT

P1V5S0_EN (MAKE_BASE=TRUE) → =P1V5S0_EN OUT

=1V05_S0_LDO_EN OUT

CPUVCCIOS0_EN (MAKE_BASE=TRUE) → =CPUVCCIOS0_EN OUT

PVCCSA_EN (MAKE_BASE=TRUE) → =PVCCSA_EN OUT

C7987 0.47UF 10% 6.3V CERM-X5R 402

C7981 0.47UF 10% 6.3V CERM-X5R 402

C7988 0.47UF 10% 6.3V CERM-X5R 402

C7986 0.47UF 10% 6.3V CERM-X5R 402

S0 Rail PGOOD (BJT Version)

=PP3V3_S5_VMON

=PP3V3_S0_VMON

R7956 150K 1% 1/20W MF 201

R7951 15K 1% 1/20W MF 201

R7953 1K 5% 1/20W MF 201 — VMON_3V3_DIV — VMON_Q2_BASE

R7952 7.15K 1% 1/20W MF 201

R7954 1K 5% 1/20W MF 201 — =PP1V5_S3RS0_VMON — VMON_Q3_BASE

PP1V5_S3RS0

R7955 1K 5% 1/20W MF 201 — =PP1V05_S0_VMON — VMON_Q4_BASE

S0PGD_C

Q7950 ASMCC0179 DFN2015H4-8 (Q1, Q2, Q3, Q4)

NC, NC, CRITICAL

353S2809 S0PGD_BJT_GND_R

R7957 100 5% 1/20W MF 201

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL

PLACE_NEAR=U7940.5:2.3mm

C7943 0.1UF 10% 6.3V X5R 201

U7940 74AUP1G3208 SOT891

SMC_BATLOW_L:100K pull up on SMC page

SMC_BATLOW_L

ALL_SYS_PWRGD

PM_SLP_SUS_L

PM_SUS_EN (MAKE_BASE=TRUE) → =P5V_3V3_SUS_EN OUT

PLACE_NEAR=U1800.A15:5mm

R7918 100K 5% 1/20W MF 201 — Delete R when pull-down added to PCH page

NO STUFF R7917 0 5% 1/20W MF 201

CHGR VFRQ Generation

=PP3V42_G3H_PWRCTL

R7931 10K 5% 1/20W MF 201

CHGR_VFRQ OUT

Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

3.3V SUS Detect

=PP3V3_S5_PWRCTL

PLACE_NEAR=U7930.6:2.3mm

No stuff C7931, 12ms Min delay time

U7930 Sense input threhold is 3.07V

C7930 0.1UF 10% 6.3V X5R 201

CRITICAL

U7930 TPS3808G33DBVRG4 SOT23-6 (90K IP)

SENSE, RESET*, MR*, CT, S4_PGOOD, VDD, GND

=PP3V3_SUS_PWRCTL

R7933 100K 5% 1/20W MF 201

PM_RSMRST → PM_RSMRST OUT

PM_RSMRST_L goes to U1800.C21

C7931 1000PF 10% 16V X7R 201 — NO STUFF

S0 Rail PGOOD Circuitry

(ISL Version in development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

P1V5S0_PGOOD from U7710

=PP5V_S0_VMON

=PP3V3_S0_VMON

=PP1V5_S3RS0_VMON

=PP1V05_S0_VMON

S0PGOOD_ISL

R7960 6.04K 1% 1/20W MF 201

R7970 10K 1% 1/20W MF 201

R7972 6.04K 1% 1/20W MF 201

C7960 0.1UF 10% 6.3V X5R 201

U7960 ISL88042IRTEZ TDFN (TPU) — CRITICAL

V2MON, V3MON, V4MON, RST*, VDD, GND, THRM_PAD

P5V_DIV_VMON, P1V5_DIV_VMON, P1V05_DIV_VMON

R7961 15K 1% 1/20W MF 201

R7971 10K 1% 1/20W MF 201

R7973 15K 1% 1/20W MF 201

353S2310

ALL_SYS_PWRGD_R

R7962 330 5% 1/20W MF 201 — ALL_SYS_PWRGD OUT

R7967 10K 5% 1/20W MF 201

R7968 100 5% 1/20W MF 201 — CPUIMVP_AXG_PGOOD

R7966 100 5% 1/20W MF 201 — P1V8S0_PGOOD

R7965 100 5% 1/20W MF 201 — P3V3S5_PGOOD

R7901 100 5% 1/20W MF 201 — P5VS3_PGOOD

R7964 100 5% 1/20W MF 201 — CPUVCCIOS0_PGOOD

R7963 100 5% 1/20W MF 201 — PVCCSA_PGOOD

DP S4 Power Enable

SMC_S4_WAKESRC_EN (MAKE_BASE=TRUE) → =DPAPWRSW_EN OUT

PSOC USB Power Enable

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L OUT

Q7925 2N7002DW-X-G SOT-363

AP_PWR_EN

(AC_EN_L)

AC_EN_L

Q7920 2N7002DW-X-G SOT-363

R7929 0 5% 1/20W MF 201 — NO STUFF

SMC_ADAPTER_EN

(PM_SLP_S3_L)

PM_SLP_S3_L

Q7925 2N7002DW-X-G SOT-363 — NC, NC, NC

Unused fet

SYNC_MASTER=K78_MLB	SYNC_DATE=01/10/2011
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 79 OF 109
	SHEET 62 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

CRITICAL
U9000
FPF1009
MFET-2X2-8IN

=PP3V3_S5_LCD
LCD_IG_PWR_EN
ON
VIN_1
VIN_2
VOUT_1
VOUT_2
GND
THRM PAD

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9014 1K 5% 1/20W MF 201
C9009 0.1UF 10% 6.3V X5R 201
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603

LCD Connector

Internal DP Connector: 518S0787

CRITICAL
J9000
CABLINE-CA
F-RT-SM

Pull-ups on panel side,
4.7 kOhm to 3.3V

=I2C_TCON_SDA
R9061 0 5% 1/20W MF 201
I2C_TCON_SDA_R

=I2C_TCON_SCL
R9062 0 5% 1/20W MF 201
I2C_TCON_SCL_R

DP_INT_HPD
R9060 0 5% 1/20W MF 201
DP_INT_HPD_CONN

L9004
FERR-120-OHM-1.5A
0402-LF

C9015 1000PF 10% 16V X7R 201

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9070 100K 5% 1/20W MF 201

DP_INT_AUX_CH_N
C9024 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_N)
DP_INT_AUX_CH_C_N

DP_INT_AUX_CH_P
C9025 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_P)
DP_INT_AUX_CH_C_P

DP_INT_ML_P<0>
C9020 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_F_P<0>

DP_INT_ML_N<0>
C9021 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_F_N<0>

DP_INT_ML_P<1>
C9022 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_F_P<1>

DP_INT_ML_N<1>
C9023 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_F_N<1>

PPVOUT_SW_LCDBKLT

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

NC
NC
NC

LED Backlight I/F

DisplayPort I/F

PLACE_NEAR=J9000.25:1mm
R9017 1M 5% 1/20W MF 201

PLACE_NEAR=J9000.24:1mm
R9018 1M 5% 1/20W MF 201

PLACE_NEAR=J9000.3:2mm
C9017 1000PF 5% 50V COG-CERM 603

R9050 100K 5% 1/20W MF 201
R9080 100K 5% 1/20W MF 201

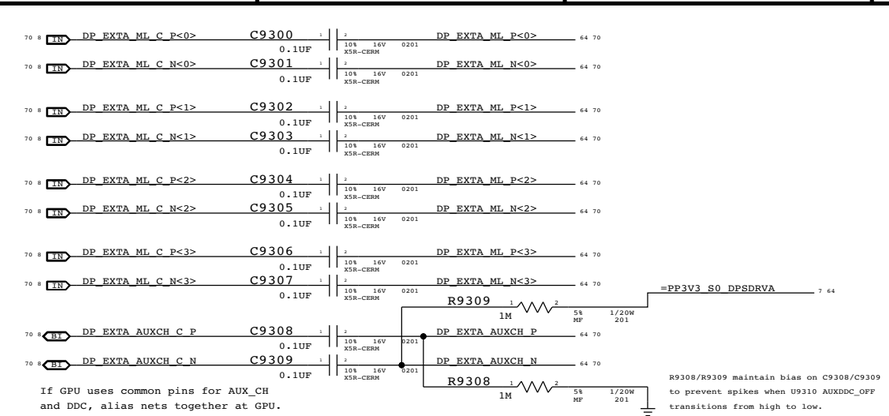
SYNC MASTER=K78 MLB
SYNC DATE=02/10/2011

PAGE TITLE
Internal DisplayPort Connector

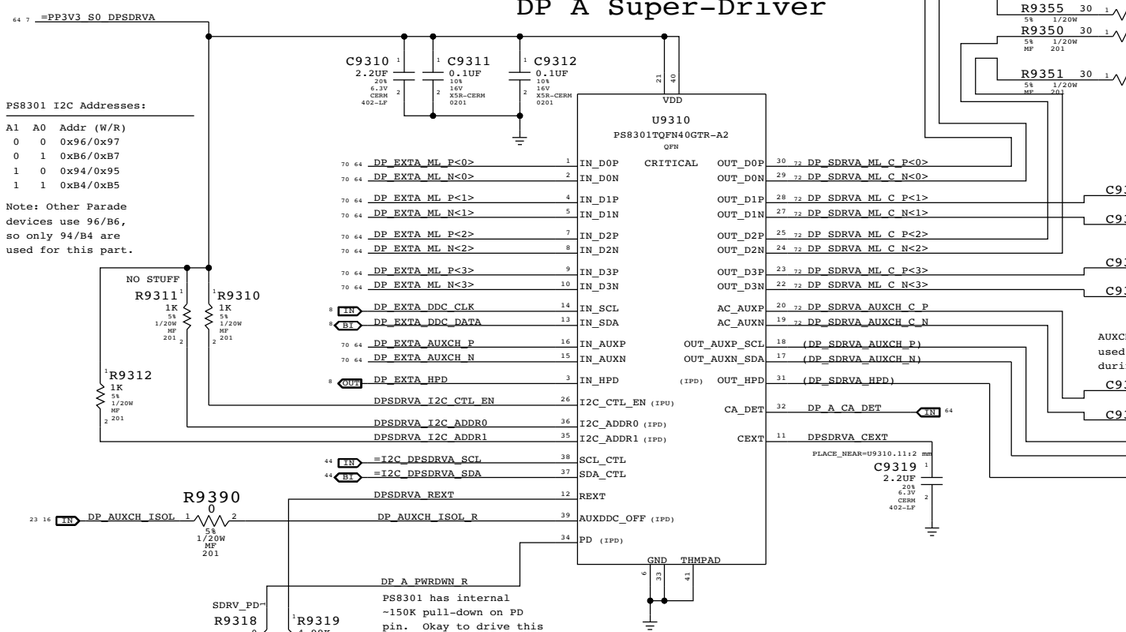
Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 90 OF 109
SHEET 63 OF 75

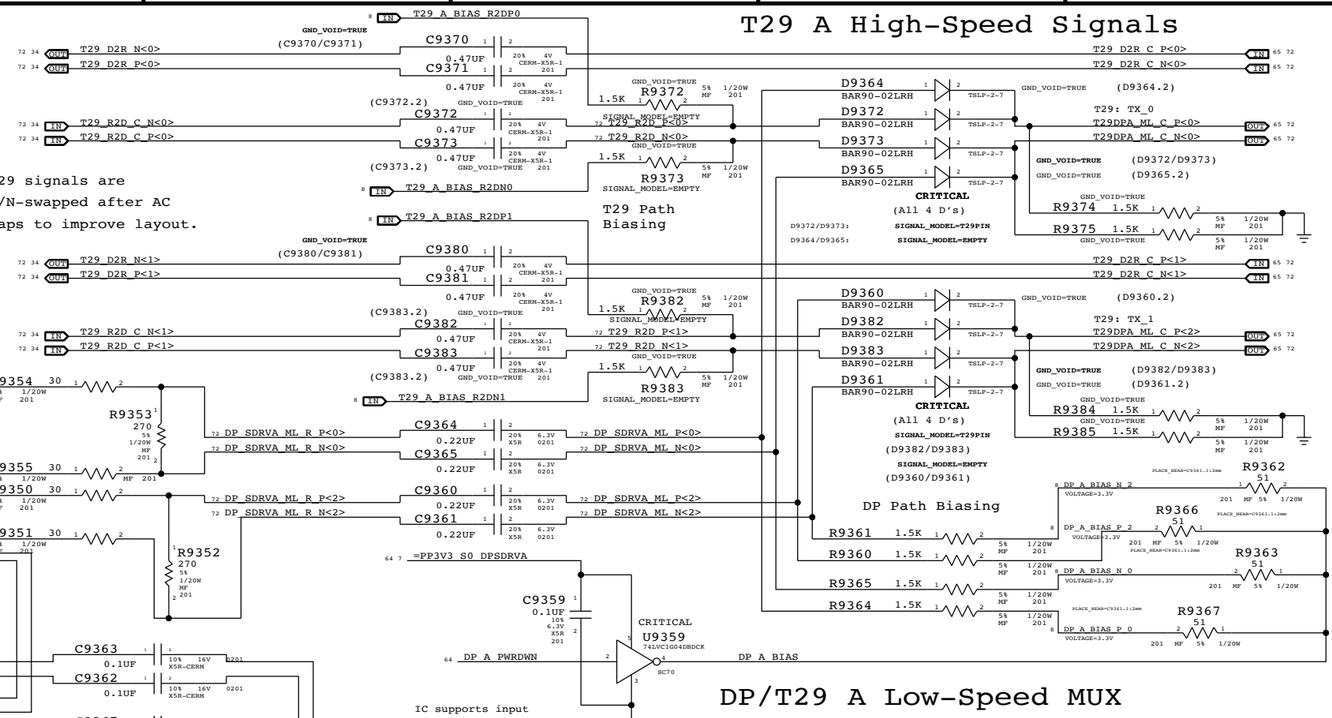
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



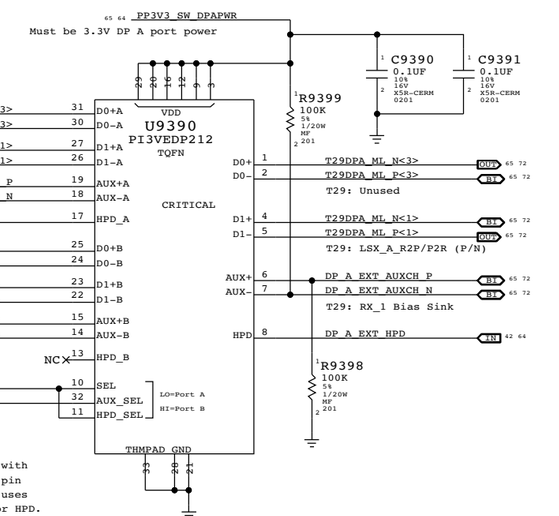
DP A Super-Driver



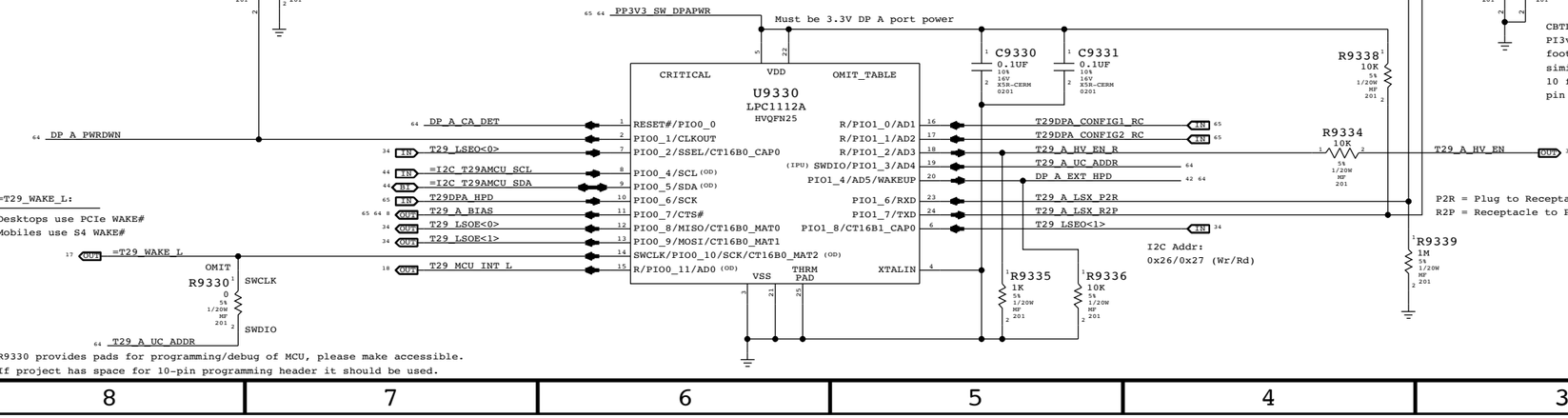
T29 A High-Speed Signals



DP/T29 A Low-Speed MUX



Port A MCU



Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC MASTER=K21 MLB	SYNC DATE=12/13/2010
PAGE TITLE	DisplayPort/T29 A MUXing
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 93 OF 109
	SHEET 64 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

3.3V/HV Power MUX

Port A HV Power Switch

64 PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

7 =PPHV_SW_DPAPWRSW
20V Max

R9416 470K 5% 1/20W MF 201

C9410 0.1UF 10% 50V X7R 603-1

SN1010017
CRITICAL
U9410
SN1010017
QFN
VIN VOUT EN* (IPU-Weak!) RTRY* CT ILIM IFLT GND THRM PAD FLT*

PPHV_SW_DPAPWR
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM

C9411 0.1UF 10% 50V X7R 603-1 VOLTAGE=15V

CRITICAL D9410 SM STPS2L30AF

DPAPWRSW_HVEN_L_R
TP_DPAPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT
DPAPWRSW_CT

R9412 0 5% 1/16W MF-LF 402 <CT>

R9410 100K 5% 1/20W MF 201

R9411 210K 1% 1/20W MF 201 <RFLT> <RLIM>

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	1A (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

Bleeder Resistor
2.5V / 249 ohm = 10mA
P = ~27mW

R9419 249 1% 1/20W MF 201

DPAPWR_BLDR_E
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Q9419 DMB53D0UV SOT-563

DPAPWR_BLDR_B

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

65 64 36 IN T29_A_HV_EN

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL D9425 POWERDI-123 DFLS1100

CRITICAL Q9425 SI8409DB BGA

3.3V/HV MUXed

R9425 4.7K 5% 1/20W MF 201

Blocking FET, off when Source >3.4V or HV_EN high.

DPAPWRSW_P3V3_ON_L

R9424 22 5% 1/20W MF 201

DPAPWR_ON_L_C

C9424 0.47UF 10% 6.3V CERM-X5R 402

R9427 100K 1% 1/20W MF 201

R9428 21.5K 1% 1/20W MF 201

DPAPWRSW_VREF

CRITICAL U9426 ZXRE060A SOT353 IN OUT FB GND PGND

C9426 0.1UF 10% 16V X5R-CERM 0201

DPAPWRSW_HV_DET_R_L

R9429 4.7K 5% 1/20W MF 201

DPAPWRSW_HV_DET_L

C9429 NO STUFF 0.1UF 10% 16V X5R-CERM 0201

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

R9418 1K 5% 1/20W MF 201

DPAPWRSW_HV_DET

Port A 3.3V Power Switch

CRITICAL U9480 TPS2065DBV SOT23 OUT IN OC* EN GND

DP_PWR must be S4/S5 to support wake from T29 devices.

=PP3V3_S4_DPAPWRSW

=DPAPWRSW_EN IN 62

65 64 36 T29_A_HV_EN

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 10% 16V X5R-CERM 0201
C9481 0.1UF 10% 16V X5R-CERM 0201
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

3.3V Always

R9426 1K 5% 1/20W MF 201

R9430 4.7K 5% 1/20W MF 201

65 64 8 T29_A_BIAS

CRITICAL U9435 ZXRE060A SOT353 IN OUT FB PGND GND

C9435 0.1UF 10% 16V X5R-CERM 0201

DPAPWRSW_P3V3_ON

Q9430 SSM6N37FEAPE SOT563

C9436 1UF 10% 10V X5R 402

DPAPWRSW_ON_C

R9437 82 5% 1/20W MF 201

Q9426 MMDT3946XG SOT363

DPAPWRSW_NPN_E

R9433 220 5% 1/20W MF 201

R9432 10K 5% 1/20W MF 201

T29_A_HV_EN 36 64 65

NO STUFF R9435 100K 1% 1/20W MF 201

DPAPWR_FB_DIV

R9436 24.9K 1% 1/20W MF 201

DisplayPort/T29 A Connector

Circuit threshold range: 2.877-2.941V (2.903V nominal)

L9400 FERR-120-OHM-3A 0603

PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C9400 0.01UF 10% 50V X7R 402

C9490 0.1UF 10% 6.3V X5R 201

65 64 8 IN T29_A_BIAS

PLACE_NEAR=C9490.1:2mm

R9490 51 5% 1/20W MF 201

T29_A_BIAS_R VOLTAGE=3.3V OUT 8

72 64 OUT T29_D2R_C_P<0>
72 64 OUT T29_D2R_C_N<0>

GND_VOID=TRUE
R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

T29 Dir DP Dir

CRITICAL J9400 MDP-K21-K78 F-RT-TH

2	HOT_PLUG_DETECT	GND	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
13	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	8
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19

SHIELD PINS 28 27 26 25 24 23 22 21

GND_DPACONN_1
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

C9405 0.1UF 10% 6.3V X5R 201

GND_DPA1_R_1

R9405 12 5% 1/20W MF 201

72 T29DPA_ML_P<0>
72 T29DPA_ML_N<0>

T29: TX_0

GND_DPACONN_7
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

C9406 0.1UF 10% 6.3V X5R 201

GND_DPA7_R_1

R9406 12 5% 1/20W MF 201

T29: LSX_R2P/P2R (P/N)

72 T29DPA_ML_P<1>
72 T29DPA_ML_N<1>

GND_VOID=TRUE (Both C's)

C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201

T29DPA_ML_C_P<0> IN 64 72
T29DPA_ML_C_N<0> IN 64 72

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201

72 64 OUT T29_D2R_C_P<0>
72 64 OUT T29_D2R_C_N<0>

72 64 OUT T29DPA_ML_P<3>
72 64 OUT T29DPA_ML_N<3>

T29: Unused

8 IN T29_A_BIAS_D2RP1
8 IN T29_A_BIAS_D2RN1

R9498 2.2K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9499 2.2K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY

CRITICAL L9498 650NH-5%-0.430MA-0.052OHM 0603 GND_VOID=TRUE

CRITICAL L9499 650NH-5%-0.430MA-0.052OHM 0603 GND_VOID=TRUE

SIGNAL_MODEL=EMPTY

D9498 BAR90-02LRH TBLP-2-7 SIGNAL_MODEL=T29PIN

D9499 BAR90-02LRH TBLP-2-7

CRITICAL GND_VOID=TRUE SIGNAL_MODEL=T29PIN (Both L's)

72 64 OUT T29_D2R_C_P<1>
72 64 OUT T29_D2R_C_N<1>

72 T29DPA_D2R1_AUXCH_P
72 T29DPA_D2R1_AUXCH_N

72 64 IN DP_A_EXT_AUXCH_P
72 64 IN DP_A_EXT_AUXCH_N

R9402 12 5% 1/20W MF 201

T29DPA_HPD_R

DPACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

R9401 12 5% 1/20W MF 201

C9498 30PF 5% 50V CERM 402

C9499 30PF 5% 50V CERM 402

C9402 0.01UF 10% 50V X7R 402

C9401 0.01UF 10% 50V X7R 402

GND_DPACONN_19
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

L9408 FERR-120-OHM-3A 0603

R9408 12 5% 1/20W MF 201

72 T29DPA_ML_P<2>
72 T29DPA_ML_N<2>

T29: TX_1

GND_VOID=TRUE (Both C's)

C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201

T29DPA_ML_C_P<2> IN 64 72
T29DPA_ML_C_N<2> IN 64 72

R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

64 OUT T29DPA_HPD
64 OUT T29DPA_CONFIG1_RC
64 OUT T29DPA_CONFIG2_RC

R9452 1M 5% 1/20W MF 201

R9451 1M 5% 1/20W MF 201

C9494 330PF 10% 16V X7R 201

C9495 330PF 10% 16V X7R 201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/20W MF 201

SYNC MASTER=K78 MLB	SYNC DATE=12/07/2010
PAGE TITLE	DisplayPort/T29 A Connector
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 94 OF 109
	SHEET 65 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

CRITICAL
Q9706
FDC638APZ_SSM6S01
SSOT6-MF

F9700
3AMP-32V-467
603-MF
BOTTOM

=PPBUS_S0_LCDBKLT
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

PPBUS_SW_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

R9788 301K 1% 1/20W MF 201
C9782 0.1UF 10% 16V X5R 402
LCDBKLT_EN_DIV
R9789 147K 1% 1/20W MF 201
LCDBKLT_EN_L
Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L

=PP5V_S0_BKL
=PPBUS_SW_BKL
CRITICAL L9701 15UH-2.8A PIMB053T-SM
PPBUS_SW_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
PLACE_NEAR=L9701.1:3mm

PLACE_NEAR=L9701.2:3mm
CRITICAL D9701 SOD-123 RB160M-60G
PLACE_NEAR=U9701.A5:3mm
C9796 220PF 10% 50V X7R-CERM 402
CRITICAL C9797 10UF 10% 50V X5R 1210-1
CRITICAL C9799 10UF 10% 50V X5R 1210-1
PPVOUT_SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm

PLACE_NEAR=U9701.D1:5mm
C9710 1UF 10% 25V X5R 603-1
PLACE_NEAR=U9701.D1:3mm
C9714 0.01UF 10% 10V X5R 201

=PP3V3_S0_BKL_VDDIO
PLACE_NEAR=U9701.C4:4mm
C9711 0.1UF 10% 6.3V X5R 201

XW9720 SM
PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
MIN_LINE_WIDTH=0.1 MM
MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=C9797.1:5mm

U9701
25-BUMP-MICRO
LP8550

VDDIO	C4	SW_0	B1
VLDO	D1	SW_1	B2
VIN	C1	FB	A5
VSYNC	D2	OUT1	E5
FILTER	C2	OUT2	D5
ISET	B3	OUT3	C5
FSET	B4	OUT4	E3
SCLK	D3	OUT5	E2
SDA	D4	OUT6	E1
PWM	A4	GND_S	B5
EN	A3	GND_L	E4
FAULT	C3	GND_SW	A1
		GND_SW	A2

BKL_VSYNC_R
BKL_FLTR
BKL_ISET
BKL_FSET
BKL_SCL
BKL_SDA
BKL_PWM
BKL_EN
TP_BKL_FAULT
PLACE_SIDE=BOTTOM
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6

R9741 10K 5% 1/20W MF 201
R9753 0 5% 1/20W MF 201
R9757 0 5% 1/20W MF 201
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA
Addr: 0x58(Wr)/0x59(Rd)
R9731 200K 1% 1/20W MF 201
R9715 100K 1% 1/20W MF 201
PPBUS_SW_LCDBKLT_PWR
R9704 33 5% 1/20W MF 201
LCD_BKLT_PWM
C9704 33PF 5% 25V MPO-C0G 201

Fpwm=9.62kHz
see spec for others

R9755 10K 1% 1/20W MF 201
R9716 90.9K 1% 1/20W MF 201
R9714 18.2K 1% 1/20W MF 201
I_LED=20.3mA

GND_BKL_SGND
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

XW9710 SM
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E5:10mm
LED_RETURN_1
R9718 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.D5:10mm
LED_RETURN_2
R9719 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.C5:10mm
LED_RETURN_3
R9720 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E3:10mm
LED_RETURN_4
R9721 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E2:10mm
LED_RETURN_5
R9722 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E1:10mm
LED_RETURN_6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
BOTTOM
OUT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K78 MLB
SYNC DATE=01/16/2011
PAGE TITLE
LCD Backlight Driver
Apple Inc.
DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 97 OF 109
SHEET 66 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_XDP_BPM	TOP,BOTTOM	100 MIL	100 MIL	100 MIL	100 MIL	=STANDARD	=STANDARD
CPU_XDP_BPM	*	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S

NOTE: CPU_XDP_BPM physical constraint is to prevent routing on outer layers.

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 41
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 42 57
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	10 16
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_XDP_BPM	CPU_ITP	XDP_BPM_L<7..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 57
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 59
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 57
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 57
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 57
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 57
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 57
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 100 OF 109

SHEET 67 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9,ISL10	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	?
MEM_CTRL2CTRL	*	0.2 MM	?
MEM_CMD2CMD	*	0.2 MM	?
MEM_CMD2CTRL	*	0.2 MM	?
MEM_DATA2DATA	*	0.14 MM	?
MEM_DQS2DQS	*	0.4 MM	?
MEM_MEM2OTHERMEM	*	0.4 MM	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	0.6 MM	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_2PWR
MEM_CTRL	MEM_PWR	*	MEM_2PWR
MEM_CMD	MEM_PWR	*	MEM_2PWR
MEM_DATA	MEM_PWR	*	MEM_2PWR
MEM_DQS	MEM_PWR	*	MEM_2PWR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_2GND
MEM_CTRL	GND	*	MEM_2GND
MEM_CMD	GND	*	MEM_2GND
MEM_DATA	GND	*	MEM_2GND
MEM_DQS	GND	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CMD2CTRL
MEM_CTRL	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines
per Huron River SFF DG rev1.0 (#438297).
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQ to DQS matching per byte lane should be within 0.127mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_CKE<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_CS_L<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_ODT<3..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<15..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_CKE<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_CS_L<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_ODT<3..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<15..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	7
		MEM_PWR	PP1V5_S3	7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 29 30 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	9 27 28 29 30 31

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/201

PAGE TITLE

Memory Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 101 OF 109

SHEET 68 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	
	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<3>	8
	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<3>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_P	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_N	8
	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 38
	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 38
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P	6 38
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_N	6 38
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 38
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	16 38
	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 38
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 38
	SATA_90D	SATA	SATA_ODD_R2D_C_P	8 16
	SATA_90D	SATA	SATA_ODD_R2D_C_N	8 16
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	8 16
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_N	8 16
	SATA_90D	SATA	SATA_HDD_R2D_RC_P	
	SATA_90D	SATA	SATA_HDD_R2D_RC_N	
	SATA_90D	SATA	SATA_HDD_D2R_RC_P	
	SATA_90D	SATA	SATA_HDD_D2R_RC_N	
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 39
USB_EXTA	USB_85D	USB	USB_EXTA_N	24 39
USB_EXTB	USB_85D	USB	USB_EXTB_P	
	USB_85D	USB	USB_EXTB_N	
USB_EXTC	USB_85D	USB	USB_EXTC_P	
	USB_85D	USB	USB_EXTC_N	
USB_EXTD	USB_85D	USB	USB_EXTD_P	6 24 40
	USB_85D	USB	USB_EXTD_N	6 24 40
USB_EXTD	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24
	USB_85D	USB	T29_A_RSVD_P	8 64
	USB_85D	USB	T29_A_RSVD_N	8 64
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	6 18 40
	USB_85D	USB	USB_CAMERA_N	6 18 40
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	
	USB_85D	USB	USB_CAMERA_CONN_N	
USB_BT	USB_85D	USB	USB_BT_P	6 24 37
USB_BT	USB_85D	USB	USB_BT_N	6 24 37
USB_TPAD	USB_85D	USB	USB_TPAD_P	49
	USB_85D	USB	USB_TPAD_N	49
USB_IR	USB_85D	USB	USB_IR_P	
	USB_85D	USB	USB_IR_N	
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	24 33
	USB_85D	USB	USB_SDCARD_N	24 33
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	8
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	8
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: PCH Constraints 1

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 102 OF 109

SHEET: 69 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 41 43
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 41 43
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	10 25
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 41
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 43
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 44
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 44
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 44
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 44
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 44
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 44
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	6 16 40
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	6 16 40
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	6 16 40
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	6 16 40
	HDA_50S	HDA	AUD_SDI_R	
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	6 16 40
	HDA_50S	HDA	HDA_SDOUT_R	16
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 43
	SPI_55S	SPI	SPI_CLK	43
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 43
	SPI_55S	SPI	SPI_MOSI	43
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 43
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 43
	SPI_55S	SPI	SPI_CS0_L	43
	SPI_55S	SPI	SPI_MLB_CLK	43 50
	SPI_55S	SPI	SPI_MLB_MOSI	43 50
	SPI_55S	SPI	SPI_MLB_MISO	43 50
	SPI_55S	SPI	SPI_MLB_CS_L	43 50
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 37
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 37
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 37
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 37
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 37
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 37
	PCIE_85D	PCIE	PCIE_FW_R2D_P	
	PCIE_85D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	
	PCIE_85D	PCIE	PCIE_FW_D2R_N	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 37
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	8 16
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 70
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 70
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	8 64
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 64
	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	64
	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	64
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 64
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 64
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	64
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	64
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	63
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	63
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	9 63
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	9 63
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	6 63
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	6 63
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_C_P	6 63
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_C_N	6 63
	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_P	9 63
	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_N	9 63
	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 34
	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 34
PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE	PCIE_T29_D2R_P<3>	8 34
PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE	PCIE_T29_D2R_P<2>	8
PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE	PCIE_T29_D2R_P<1>	8 34
PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE	PCIE_T29_D2R_P<0>	8
PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE	PCIE_T29_D2R_N<3>	8 34
PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE	PCIE_T29_D2R_N<2>	8 34
PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE	PCIE_T29_D2R_N<1>	8 34
PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE	PCIE_T29_D2R_N<0>	8 34
PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE	PCIE_T29_R2D_P<3>	34
PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE	PCIE_T29_R2D_P<2>	34
PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE	PCIE_T29_R2D_P<1>	34
PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE	PCIE_T29_R2D_P<0>	34
PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE	PCIE_T29_R2D_N<3>	34
PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE	PCIE_T29_R2D_N<2>	34
PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE	PCIE_T29_R2D_N<1>	34
PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE	PCIE_T29_R2D_N<0>	34
	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	34
	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	34
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 34
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 25
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	25 34
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	34

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/201

PAGE TITLE

PCH Constraints 2

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 103 OF 109

SHEET 70 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N

Port 2 Not Used

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: Ethernet/FW Constraints

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 104 OF 109

SHEET: 71 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2X_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2X_DIELECTRIC	?

DP/T29 Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 Net Properties

T29 IC Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP29		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	8 34
DN29		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	8 34
DP34	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	34
DN34	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	34
DP35		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	8 34
DN35		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	8 34
DP36	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	34
DN36	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	34
DP38		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	
DN38		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	
DP39	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	
DN39	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	
DP41		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	
DN41		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	
DP42	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	
DN42	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	
DN43		T29_I2C_55S	T29_I2C	I2C_T29_SCL	34 44
DP43		T29_I2C_55S	T29_I2C	I2C_T29_SDA	34 44
DP44	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	34
DN44	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	34
DP45	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	34
DN45	T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	34
DP46		T29DP_80D	T29DP	T29_R2D_C_P<3..0>	8 34 64
DN46		T29DP_80D	T29DP	T29_R2D_C_N<3..0>	8 34 64
DP47		T29DP_80D	T29DP	T29_D2R_P<3..0>	8 34 64
DN47		T29DP_80D	T29DP	T29_D2R_N<3..0>	8 34 64
DP48	T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	64
DN48	T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	64
DP49	T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	64
DN49	T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	64
DP27		T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	64
DN27		T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	64
DP54	T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_P<0>	64 65
DN54	T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_N<0>	64 65
DP53	T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_P<1>	64 65
DN53	T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_N<1>	64 65
DP68		T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_P	65
DN68		T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_N	65
DP63		T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	64
DN63		T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	64
DP62		T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	64
DN62		T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	64
DP64	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<0>	64
DN64	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<0>	64
DP65	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<1>	64
DN65	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<1>	64
DP67	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2>	64
DN67	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2>	64
DP66	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3>	64
DN66	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3>	64
DP69	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	64
DN69	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	64
DP61		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	64
DN61		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	64
DP26	T29DPA_ML_ODD			T29DPA_ML_P<1>	64 65
DN26	T29DPA_ML_ODD			T29DPA_ML_N<1>	64
DP25	T29DPA_ML_ODD			T29DPA_ML_P<3>	64 65
DN25	T29DPA_ML_ODD			T29DPA_ML_N<3>	64
DP24		T29DP_80D	T29DP	T29DPA_ML_P<3..0>	64 65
DN24		T29DP_80D	T29DP	T29DPA_ML_N<3..0>	64 65
DP23		T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	64 65
DN23		T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	64 65
DP58	DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	64 65
DN58	DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	64 65

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: T29 Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 105 OF 109
SHEET 72 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	44
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	44
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 44
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 44
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	53
	1TO1_DIFFPAIR		CHGR_CSI_N	53
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	53
	1TO1_DIFFPAIR		CHGR_CSO_N	53

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 106 OF 109

SHEET 73 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27948 OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_100D	ENETCONN	ENETCONN_P<3..0>
	ENET_100D	ENETCONN	ENETCONN_N<3..0>
	SATA_90D	SATA	SATA_ODD_D2R_UF_P
	SATA_90D	SATA	SATA_ODD_D2R_UF_N
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N
J295	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P
J296	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N
J297	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P
J294	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 47
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P 9 47
	THERM_1TO1_55S	THERM	CPU_THERMD_N 9 47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P 47
	THERM_1TO1_55S	THERM	T29_THERMD_N 47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_P 46 47
	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_N 46 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N 46
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N 45 59
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P 45 59
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P 45 57 58
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N 45 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P 45 58
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N 45 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P 45
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P 45
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P 54
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N 54
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P 57 58
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N 57 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N
	SENSE_1TO1_55S	SENSE	ISNS_CPU_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N 38 46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P 38 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N 8 46
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P 8 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N 46 56
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P 46 56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N 37 46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P 37 46
	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_N
	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_P

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P 6 40 51 74
	DIFFPAIR	AUDIO	SPKRAMP_INR_N 6 40 51 74
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P 51
	DIFFPAIR	AUDIO	MAX98300_R_N 51

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N
	1TO1_DIFFPAIR		CHGR_CSI_R_P 53
	1TO1_DIFFPAIR		CHGR_CSI_R_N 53
	1TO1_DIFFPAIR		CHGR_CSO_R_P 46 53
	1TO1_DIFFPAIR		CHGR_CSO_R_N 46 53
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P 39
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N 39
(USB_EXTA)	USB_85D	USB	USB2_LT1_P 39
(USB_EXTA)	USB_85D	USB	USB2_LT1_N 39
	USB_85D	USB	CONN_USB2_BT_P
	USB_85D	USB	CONN_USB2_BT_N
	USB_85D	USB	USB_LT2_P
	USB_85D	USB	USB_LT2_N
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT 6 51 52
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT 6 51 52
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P 6 40 51 74
AUD_DIFF	DIFFPAIR	AUDIO	SPKRAMP_INR_N 6 40 51 74
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N
	USB_85D	USB	USB_TPAD_R_P
	USB_85D	USB	USB_TPAD_R_N
	SB_POWER		PP3V3_S5 6 7
	SB_POWER		PP3V3_S0 6 7
	GND		GND

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_P
(USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_N
(USB_EXTA)	USB_85D	USB	USB_LT1_P
(USB_EXTA)	USB_85D	USB	USB_LT1_N
(USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_P 6 49
(USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_N 6 49
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R
	SMB_55S	SMB	I2C_TCON_SCL
	SMB_55S	SMB	I2C_TCON_SDA
	SMB_55S	SMB	I2C_TCON_SCL_CONN
	SMB_55S	SMB	I2C_TCON_SDA_CONN

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: Project Specific Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 108 OF 109

SHEET 74 OF 75

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.155MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4,ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

PCB Rule Definitions

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 109 OF 109

SHEET 75 OF 75

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED