

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2011-04-18

# SCHEM, EVT, MLB, K21

04/18/11

Page	Contents	Sync
1	Table of Contents	MASTER
2	System Block Diagram	X5_MLB 12/11/2009
3	Power Block Diagram	19/01/2011
4	Revision History	MASTER
5	BOM Configuration	X17_REF 05/28/2009
6	Functional Test / No Test	(K99_MLB) (02/16/2010)
7	Power Aliases	X91_MLB 05/15/2010
8	Signal Aliases	X91_MLB 05/15/2010
9	CPU DMI/PEG/FDI/RSVD	X78_MLB 01/10/2011
10	CPU CLOCK/MISC/JTAG	X78_MLB 01/10/2011
11	CPU DDR3 INTERFACES	X78_MLB 01/10/2011
12	CPU POWER	X78_MLB 01/10/2011
13	CPU GROUNDS	X78_MLB 01/10/2011
14	CPU DECOUPLING-I	X78_MLB 02/08/2011
15	CPU DECOUPLING-II	X78_MLB 01/10/2011
16	PCH SATA/PCIE/CLK/LPC/SPI	X21_MLB 12/13/2010
17	PCH DMI/FDI/GRAPHICS	X21_MLB 12/13/2010
18	PCH PCI/FLASHCACHE/USB	X21_MLB 12/13/2010
19	PCH MISC	X21_MLB 12/13/2010
20	PCH POWER	X21_MLB 12/13/2010
21	PCH GROUNDS	X78_MLB 01/10/2011
22	PCH DECOUPLING	X78_MLB 01/10/2011
23	CPU & PCH XDP	X21_MLB 12/13/2010
24	USB HUBS	X21_MLB 12/13/2010
25	Clock (CK505) and Chipset Support	X78_MLB 11/29/2010
26	CPU Memory S3 Support	X21_MLB 12/13/2010
27	DDR3 DRAM CHANNEL A (0-31)	X78_MLB 12/07/2010
28	DDR3 DRAM CHANNEL A (32-63)	X78_MLB 12/07/2010
29	DDR3 DRAM CHANNEL B (0-31)	X78_MLB 12/07/2010
30	DDR3 DRAM CHANNEL B (32-63)	X78_MLB 12/07/2010
31	FSB/DDR3/FRAMBUF Vref Margining	X78_MLB 01/10/2011
32	DDR3 DRAM Channel B (32-63)	X78_MLB 12/14/2010
33	SecureDigital Card Reader	(MASTER)
34	T29 Host (1 of 2)	X78_MLB 01/10/2011
35	T29 Host (2 of 2)	X78_MLB 01/10/2011
36	T29 Power Support	X78_MLB 01/10/2011
37	X21 WIRELESS CONNECTOR	X21_MLB 12/13/2010
38	SATA CONNECTOR	X78_MLB 01/10/2011
39	External USB Connectors	X21_MLB 12/13/2010
40	Left I/O (LIO) Connector	X21_MLB 11/09/2010
41	SMC	X78_MLB 01/10/2011
42	SMC Support	X78_MLB 01/10/2011
43	LPC+SPI Debug Connector	X78_MLB 01/10/2011
44	SMBus Connections	X78_MLB 01/10/2011
45	Voltage & Load Side Current Sensing	X78_MLB 01/10/2011

Page	Contents	Sync
46	High Side Current Sensing	X78_MLB 01/16/2011
47	Thermal Sensors	X78_MLB 01/16/2011
48	Fan	X78_MLB 01/10/2011
49	IPD / KBD Backlight	X78_MLB 01/10/2011
50	SPI ROM	X78_MLB 01/10/2011
51	AUDI0: SPEAKER AMP	X78_MLB 01/10/2011
52	DC-In & Battery Connectors	JACK_X901 08/20/2010
53	PBus Supply & Battery Charger	X78_MLB 12/03/2010
54	System Agent Supply	X78_MLB 01/16/2011
55	5V / 3.3V Power Supply	X78_MLB 01/16/2011
56	1.5V DDR3 Supply	X78_MLB 01/10/2011
57	CPU IMVP7 & AXG VCore Regulator	X78_MLB 01/10/2011
58	CPU IMVP7 & AXG VCore Output	X78_MLB 12/07/2010
59	CPU VCCIO (1.05V) Power Supply	X78_MLB 01/10/2011
60	Misc Power Supplies	X78_MLB 01/16/2011
61	Power FETs	X78_MLB 01/10/2011
62	Power Control 1/ENABLE	X78_MLB 01/10/2011
63	Internal DisplayPort Connector	X78_MLB 02/10/2011
64	DisplayPort/T29 A MUXing	X21_MLB 12/13/2010
65	DisplayPort/T29 A Connector	X78_MLB 12/07/2010
66	LCD Backlight Driver	X78_MLB 01/16/2011
67	CPU Constraints	X21_CONSTRAINTS 04/06/2011
68	Memory Constraints	X21_CONSTRAINTS 04/06/2011
69	PCH Constraints 1	X21_CONSTRAINTS 04/06/2011
70	PCH Constraints 2	X21_CONSTRAINTS 04/06/2011
71	Ethernet/FW Constraints	X21_CONSTRAINTS 04/06/2011
72	T29 Constraints	X21_CONSTRAINTS 04/06/2011
73	SMC Constraints	X21_CONSTRAINTS 04/06/2011
74	Project Specific Constraints	X21_CONSTRAINTS 04/06/2011
75	PCB Rule Definitions	X21_CONSTRAINTS 04/06/2011

Schematic / PCB #'s

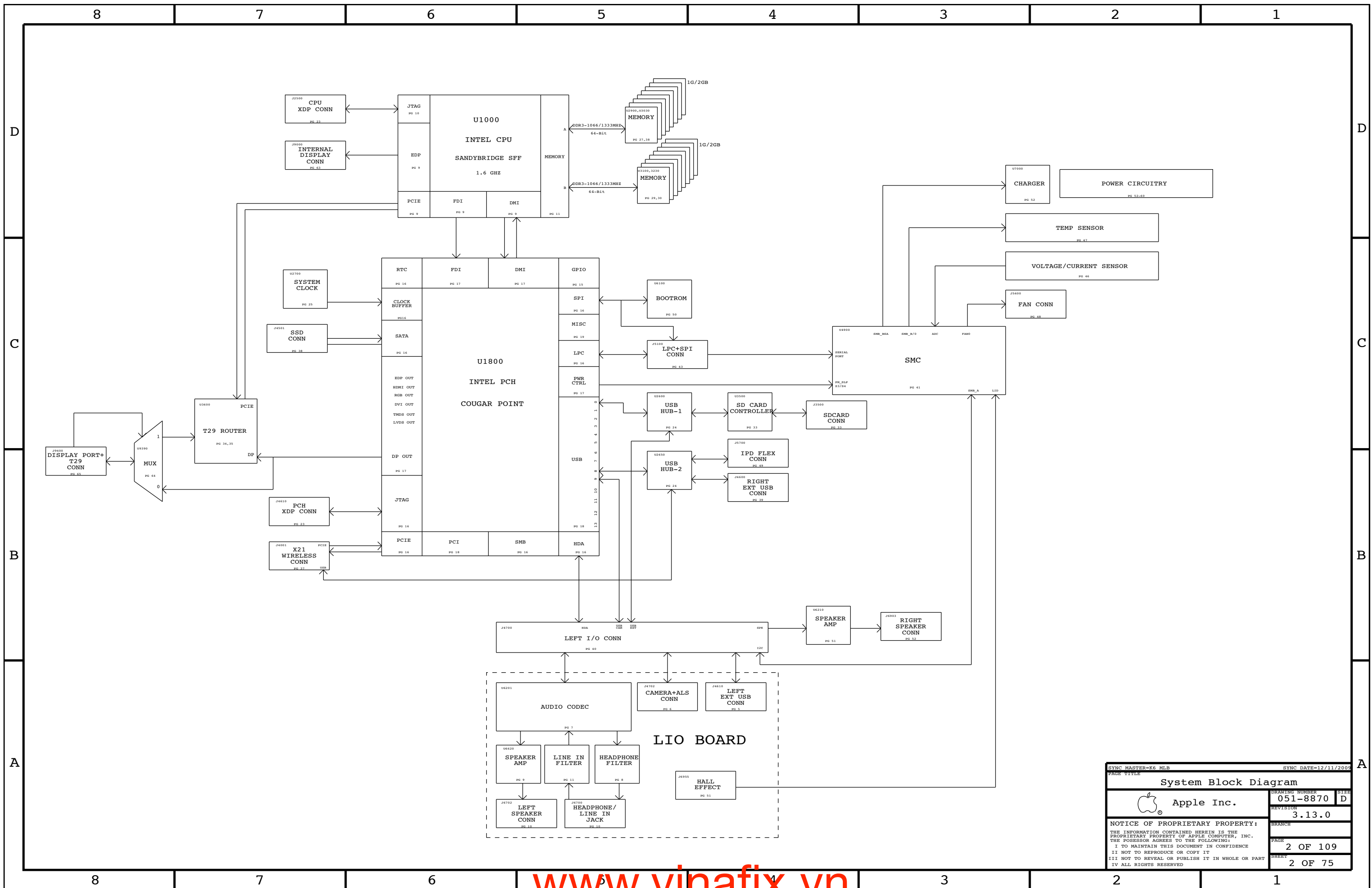
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8870	1	SCHEM,MLB,K21	SCH	CRITICAL	
020-3023	1	PCBF,MLB,K21	PCB	CRITICAL	

DRAWING  
TITLE-MLB  
ABBREV-DRAWING  
DATE: 04/18/2011

DRAWING TITLE		SCHEM,MOCKUP,MLB,K21	
Apple Inc.		DRAWING NUMBER	051-8870
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PCB,UL RECOGNIZED, MIN. 130-C TEMP RATING AND V-O FLAME RATING PER UL 796 & UL 94 PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP RATING AND V-O FLAME RATING



SYNC MASTER=K6 MLB		SYNC DATE=12/11/2009	
PAGE TITLE			
System Block Diagram			
DRAWING NUMBER		SIZE	
051-8870		D	
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PAGE		SHEET	
2 OF 109		2 OF 75	



BOM Variants


BOM NUMBER	BOM NAME	BOM OPTIONS
085-2684	K21i MLB DEVELOPMENT BOM	K21_DEVEL:ENG
607-8041	CHN FTS,PCBA,MLB,K21	K21_COMMON
639-2553	PCBA,MLB,1.8GHZ,HY 2GB,K21	K21_CHNPTS,EEEE:DP1F,CPU1.8GHZ,DDR3:HYNIX_2GB
639-2554	PCBA,MLB,1.7GHZ,SA 4GB,K21	K21_CHNPTS,EEEE:DP1G,CPU1.7GHZ,DDR3:SAMSUNG_4GB
639-2558	PCBA,MLB,1.8GHZ,EL 4GB,K21	K21_CHNPTS,EEEE:DP1H,CPU1.8GHZ,DDR3:ELPIDA_4GB
639-2549	PCBA,MLB,1.7GHZ,EL 4GB,K21	K21_CHNPTS,EEEE:DP1J,CPU1.7GHZ,DDR3:ELPIDA_4GB
639-2555	PCBA,MLB,1.8GHZ,HY 4GB,K21	K21_CHNPTS,EEEE:DP1K,CPU1.8GHZ,DDR3:HYNIX_4GB
639-2557	PCBA,MLB,1.8GHZ,SA 4GB,K21	K21_CHNPTS,EEEE:DP1L,CPU1.8GHZ,DDR3:SAMSUNG_4GB
639-2548	PCBA,MLB,1.7GHZ,HY 2GB,K21	K21_CHNPTS,EEEE:DP1M,CPU1.7GHZ,DDR3:HYNIX_2GB
639-2550	PCBA,MLB,1.8GHZ,MI 2GB,K21	K21_CHNPTS,EEEE:DP1N,CPU1.8GHZ,DDR3:MICRON_2GB
639-2551	PCBA,MLB,1.7GHZ,HY 4GB,K21	K21_CHNPTS,EEEE:DP1P,CPU1.7GHZ,DDR3:HYNIX_4GB
639-2552	PCBA,MLB,1.7GHZ,SA 2GB,K21	K21_CHNPTS,EEEE:DP1Q,CPU1.7GHZ,DDR3:SAMSUNG_2GB
639-2556	PCBA,MLB,1.8GHZ,SA 2GB,K21	K21_CHNPTS,EEEE:DP1R,CPU1.8GHZ,DDR3:SAMSUNG_2GB
639-2559	PCBA,MLB,1.7GHZ,MI 2GB,K21	K21_CHNPTS,EEEE:DP1T,CPU1.7GHZ,DDR3:MICRON_2GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,L10,K99	[EEEE_DP1F]	CRITICAL	EEEE:DP1F
825-7563	1	LABEL,L10,K99	[EEEE_DP1G]	CRITICAL	EEEE:DP1G
825-7563	1	LABEL,L10,K99	[EEEE_DP1H]	CRITICAL	EEEE:DP1H
825-7563	1	LABEL,L10,K99	[EEEE_DP1J]	CRITICAL	EEEE:DP1J
825-7563	1	LABEL,L10,K99	[EEEE_DP1K]	CRITICAL	EEEE:DP1K
825-7563	1	LABEL,L10,K99	[EEEE_DP1L]	CRITICAL	EEEE:DP1L
825-7563	1	LABEL,L10,K99	[EEEE_DP1M]	CRITICAL	EEEE:DP1M
825-7563	1	LABEL,L10,K99	[EEEE_DP1N]	CRITICAL	EEEE:DP1N
825-7563	1	LABEL,L10,K99	[EEEE_DP1P]	CRITICAL	EEEE:DP1P
825-7563	1	LABEL,L10,K99	[EEEE_DP1Q]	CRITICAL	EEEE:DP1Q
825-7563	1	LABEL,L10,K99	[EEEE_DP1R]	CRITICAL	EEEE:DP1R
825-7563	1	LABEL,L10,K99	[EEEE_DP1T]	CRITICAL	EEEE:DP1T

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-2684	1	K21 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-8041	1	CHN FTS,PCBA,MLB,K21	CHNPTS	CRITICAL	K21_COMMON

SYNC MASTER=MASTER		SYNC DATE=MASTER	
Revision History			
 Apple Inc.	DRAWING NUMBER	051-8870	SIZE D
	REVISION	3.13.0	
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PAGE		4 OF 109	
SHEET		4 OF 75	

K21 BOM GROUPS

BOM GROUP	BOM OPTIONS
K21_COMMON	ALTERNATE,COMMON,K21_MISC,K21_DEBUG;ENG,K21_PROGPARTS,USBHUB_2513B,T29BST;Y,EDP,PC;B3
K21_MISC	CPOMEN_S0,SUB1_ZHONREN,SUB2_ZHONREN,T29;YES,SERVIC;MCU,SDRV_PD,EB_EL
K21_PROGPARTS	BOOTROM_PROG,SBC_PROG,T29ROM;PROG,T29MCU;PROG
K21_DEVEL;ENG	BKLT;ENG,BMON;ENG,KDP_CONN,KDP_CPU;BPM,KDP_FCH,LPCPLUS,VREFPROM,SDPOOD_ISL,S3_S0_LED,VCCIOISS;ENG,AIRPORTISS;ENG,HDDIOISS;ENG,LCDKLTISS;ENG
K21_DEVEL;PVT	LPCPLUS,KDP_CONN,KDP_FCH
K21_DEBUG;ENG	DEVEL_ROM,SBC_DEBUG;YES,KDP
K21_DEBUG;PVT	DEVEL_ROM,BKLT;PROG,SBC_DEBUG;YES,KDP,VREFPROM;NOT
K21_DEBUG;PROD	BKLT;PROD,BMON;PROD,SBC_DEBUG;YES,KDP,VREFPROM;NOT,LPCPLUS,VCCIOISS;PROD,AIRPORTISS;PROD,HDDIOISS;PROD,LCDKLTISS;PROD
DDR3;HYNIX_2GB	DRAM_CFG0;L,DRAM_CFG1;L,DRAM_CFG2;L,DRAM_CFG3;L,DRAM_TYPE;HYNIX_2GB
DDR3;HYNIX_4GB	DRAM_CFG0;L,DRAM_CFG1;L,DRAM_CFG2;L,DRAM_CFG3;L,DRAM_TYPE;HYNIX_4GB
DDR3;SAMSUNG_2GB	DRAM_CFG0;L,DRAM_CFG1;H,DRAM_CFG2;L,DRAM_CFG3;L,DRAM_TYPE;SAMSUNG_2GB
DDR3;SAMSUNG_4GB	DRAM_CFG0;L,DRAM_CFG1;H,DRAM_CFG2;H,DRAM_CFG3;L,DRAM_TYPE;SAMSUNG_4GB
DDR3;MICRON_2GB	DRAM_CFG0;H,DRAM_CFG1;L,DRAM_CFG2;L,DRAM_CFG3;L,DRAM_TYPE;MICRON_2GB
DDR3;ELPIDA_4GB	DRAM_CFG0;H,DRAM_CFG1;H,DRAM_CFG2;H,DRAM_CFG3;L,DRAM_TYPE;ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33580550	1	IC,EEPROM,SERIAL,SPI,1Kbit,1.8V,MSP,LF	U3690	CRITICAL	T29ROM;BLANK
34170352	1	IC,T29-ROM,K21	U3690	CRITICAL	T29ROM;PROD
33783997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HWQFN25	U9330	CRITICAL	T29MCU;BLANK
34170353	1	IC,T29-MCU,K21	U9330	CRITICAL	T29MCU;PROD
33880895	1	IC,SBC,RENESAS,895/2117BP,9MM,TLP,RF	U4900	CRITICAL	SBC;BLANK
34170348	1	IC,SBC,K21	U4900	CRITICAL	SBC;PROD
33580809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM;BLANK
33580803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Samsung	U6100	CRITICAL	BOOTROM;BLANK
34170349	1	IC,SPI ROM,K21 K78	U6100	CRITICAL	BOOTROM;PROD

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Resist alt to Toshiba
37780107	37780066		ALL	OScont alt to Sontech
13880676	13880691		ALL	Murata alt to Samsung
37180679	37180652		ALL	NXP alt to NXP
13880679	13880678		ALL	Murata/Samsung to Taiyo
13880671	13880673		ALL	Taiyo alt to Murata
33764092	33764100		ALL	EARLY 1.5GHZ CPU SAMPLES
33784093	33784101		ALL	EARLY 1.4GHZ CPU SAMPLES
35383312	35383055		ALL	NXP alt to Pericom
37680790	37680928		ALL	TI alt to Fairchild
12880333	12880294		ALL	Sanyo alt for Sanyo/Fredrick
15281442	15281295		ALL	Toko alt for NEC inductor
10480035	10480011		ALL	Panasonic alt to Cytotec
15281085	15281307		ALL	Toko alt for Cytotec
514-0744	998-3941		ALL	Old J9400 alt to New J9400
37680874	37680895		ALL	F2MCU2025 alt to RJK0380085
13880703	13880648		ALL	Murata alt to Taiyo Yuden
13880684	13880640		ALL	Murata alt to Taiyo Yuden
33880721	33880923		ALL	SBC USX2061 alt to USB25138
15281493	15281300		ALL	Colicraft alt to Murata

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33784121	1	SMB,QATM,QS,J1,1.8,17W,2+2,1.20,4H,BGA	U1000	CRITICAL	CPU:1.8GHZ
33784119	1	SMB,QATM,QS,J1,1.7,17W,2+2,1.20,3H,BGA	U1000	CRITICAL	CPU:1.7GHZ
33784101	1	SMB,QATM,QS,J1,1.6,17W,2+2,1.1,4H,BGA	U1000	CRITICAL	CPU:1.6GHZ
33784100	1	SMB,QATM,QS,J1,1.5,17W,2+2,1.1,4H,BGA	U1000	CRITICAL	CPU:1.5GHZ
33784099	1	SMB,QATM,QS,J1,1.4,17W,2+2,1.05,3H,BGA	U1000	CRITICAL	CPU:1.4GHZ
33784098	1	SMB,QATM,QS,J1,1.3,17W,2+2,1.05,3H,BGA	U1000	CRITICAL	CPU:1.3GHZ
33784080	1	COUGAR POINT,SLBAG,PRO,8D920647	U1800	CRITICAL	PCB;B2
33784091	1	COUGAR POINT,B3,SL74K,PRO,8D920647	U1800	CRITICAL	PCB;B3
33880976	1	IC,T29 Eagle Ridge,192 PCBGA,8X9MM	U3600	CRITICAL	T29;YES
33380585	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE;HYNIX_2GB
33380585	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE;HYNIX_2GB
33380585	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE;HYNIX_2GB
33380585	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE;HYNIX_2GB
33380586	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE;HYNIX_4GB
33380586	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE;HYNIX_4GB
33380586	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE;HYNIX_4GB
33380586	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE;HYNIX_4GB
33380587	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE;SAMSUNG_2GB
33380587	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE;SAMSUNG_2GB
33380587	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE;SAMSUNG_2GB
33380587	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE;SAMSUNG_2GB
33380588	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE;SAMSUNG_4GB
33380588	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE;SAMSUNG_4GB
33380588	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE;SAMSUNG_4GB
33380588	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE;SAMSUNG_4GB
33380590	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE;MICRON_2GB
33380590	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE;MICRON_2GB
33380590	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE;MICRON_2GB
33380590	4	IC,SDRAM,1GBIT,DDR3-1333,7EP FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE;MICRON_2GB
33380589	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE;ELPIDA_4GB
33380589	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE;ELPIDA_4GB
33380589	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE;ELPIDA_4GB
33380589	4	IC,SDRAM,2GBIT,DDR3-1333,7EP FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE;ELPIDA_4GB
35382929	1	IC,1SL6259,BATCHARGER,3#,4X4MM,QFN28	U7000	CRITICAL	

PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-2333	1	K21, T29 Fence	T29FENCE	CRITICAL	
806-2356	1	K21, T29 Can	T29CAN	CRITICAL	NOSTUFF
806-2347	1	K21, T29 Filter Can	T29FILTERCAN	CRITICAL	
806-2376	1	K78, MDP Can	MDPCAN	CRITICAL	
806-2377	1	K78, MDP Spring	MDPSPRING	CRITICAL	NOSTUFF

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2	DIE REV	CFG 3
2GB	0	A	0
4GB	1	B	1

SYNC MASTER/REV REF SYNC DATE/REV/26/2008

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

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PAGE: 5 OF 109

SHEET: 5 OF 75

# Functional Test Points

## J4001: AirPort / BT Connector

FUNC_TEST	TP	NC
PP3V3 WLAN F	37	
WiFi_EVENT_I	37 41	
PCIE AP R2D N	37 70	
PCIE AP R2D P	37 70	
PCIE CLK100M AP N	16 37 70	
PCIE CLK100M AP P	16 37 70	
USB BT P	24 37 69	
USB BT N	24 37 69	
PCIE AP D2R P	16 37 70	
PCIE AP D2R N	16 37 70	
PCIE WAKE L	17 37	
AP_RESET_CONN_I	37	
AP_CLKREQ_O_L	37	
PP3V3 S3 BT	7 37	

(Need 5 TPs)

## J4501: SATA SSD Connector

FUNC_TEST	TP	NC
PP3V3 S0 HDD R	38	
SATA HDD D2R C P	38 69	
SATA HDD D2R C N	38 69	
SATA HDD R2D N	38 69	
SATA HDD R2D P	38 69	
SMC HDD_OOR_TEMP_CONN	38	
SMC HDD_TEMP_CTL_CONN	38	

(Need 5 TPs)

## J4700: LIO Connector

FUNC_TEST	TP	NC
PP3V42 G3H ONEWIRE	7 40	
PP3V3 S0 AUDIO	7 40	
PP3V3R1V5 S0 AUDIO	7 40	
SYS ONEWIRE	40 41	
SMC BC_AOK	40 41 42	
USB_PWR_EN	39 40 62	
SMC LID	6 40 41 42 49	
I2C LIO_SDA	40 44	
I2C LIO_SCL	40 44	
I2C MIKEY_SCL	40 44	
I2C MIKEY_SDA	40 44	
AUD_IPHS_SWITCH_EN	19 40	
AUD_IP_PERIPHERAL_DET	19 40	
AUD_I2C_INT_L	19 40	
AUD_GPIO_3	40 51	
SPKRAMP_INR_N	40 51 74	
SPKRAMP_INR_P	40 51 74	
USB_EXTD_N	24 40 69	
USB_EXTD_P	24 40 69	
USB_CAMERA_N	18 40 69	
USB_CAMERA_P	18 40 69	
HDA_SDOUT	16 40 70	
HDA_BIT_CLK	16 40 70	
HDA_SDIN0	16 40 70	
USB_EXTD_OC_L	24 40	
HDA_RST_L	16 40 70	
HDA_SYNC	16 40 70	

(Need 2 TPs)

## J4800: SD Card Connector

FUNC_TEST	TP	NC
PP3V3 SW_SD_PWR	33	
SD_CLK	33	
SD_CMD	33	
SD_D<7..0>	33	
SD_CD_L	33	
SD_WP	33	

(Need to add 2 GND TPs)

## J5100: LPC+SPI Connector

FUNC_TEST	TP	NC
PP3V3 S5 LPCPLUS	7 43	
PP5V S0 LPCPLUS	7 43	
LPC_AD<3..0>	16 41 43 70	
SPI_ALT_MOSI	43	
SPI_ALT_MISO	43	
LPC_FRAME_L	16 41 43 70	
PM_CLKRUN_L	17 41 43	
SMC_TMS	41 42 43	
LPCPLUS_RESET_L	25 43	
SMC_TDO	41 42 43	
SMC_TRST_L	41 42 43	
SMC_MD1	41 43	
SMC_TX_L	39 41 42 43	
LPC_CLK33M LPCPLUS	25 43 70	
SPIROM_USE_MLB	19 43 50	
SPI_ALT_CLK	43	
SPI_ALT_CS_L	43	
LPC_SERIRQ	16 41 43	
LPC_PWRDWN_L	17 41 43	
SMC_TDI	41 42 43	
SMC_TCK	41 42 43	
SMC_RESET_L	41 42 43 53	
SMC_NMI	41 43	
SMC_RX_L	39 41 42 43	
LPCPLUS_GPIO	19 43	

(Need to add 6 GND TPs)

## J5600: Fan Connector

FUNC_TEST	TP	NC
PP5V_S0_FAN	7 48	
FAN_RT_TACH	48	
FAN_RT_PWM	48	

(Need to add 1 GND TP)

## J5700: IPD Flex Connector

FUNC_TEST	TP	NC
PP3V3 TPAD_CONN	49	
PP5V TPAD_FILT	49	
PP3V42 G3H TPAD	7 49	
USB_TPAD_CONN_P	49 74	
USB_TPAD_CONN_N	49 74	
I2C_TPAD_SDA	44 49	
I2C_TPAD_SCL	44 49	
SMC_ONOFF_L	41 42 49	
SMC_LID	6 40 41 42 49	
SMC_TPAD_RST_L	42 49	
SMC_PME_S4_WAKE_L	41 42 49	

(Need to add 5 GND TPs)

## J6900: DC-In Connector

FUNC_TEST	TP	NC
PP18V5_DCIN_CONN	7 52	
PP5V_S3_LIO_CONN	7 52	

(Need 6 TPs)

## J6903: Speaker Connector

FUNC_TEST	TP	NC
SPKRAMP_R_P_OUT	51 52 74	
SPKRAMP_R_N_OUT	51 52 74	

(Need to add 3 GND TPs)

## J6950: Battery Connector

FUNC_TEST	TP	NC
PPVBAT_G3H_CONN	52 53	
SMBUS_BATT_SCL	44 52	
SMBUS_BATT_SDA	44 52	
SYS_DETECT_L	52	

(Need 4 TPs)

## J9000: Internal DP Connector

FUNC_TEST	TP	NC
PPVOUT_SW_LCDBKLT	63 66	
PP3V3_SW_LCD	63	
I2C_TCON_SDA_R	63	
I2C_TCON_SCL_R	63	
LED_RETURN_6	63 66	
LED_RETURN_5	63 66	
LED_RETURN_4	63 66	
LED_RETURN_3	63 66	
LED_RETURN_2	63 66	
LED_RETURN_1	63 66	
DP_INT_HPD_CONN	63	
DP_INT_AUX_CH_C_N	63 70	
DP_INT_AUX_CH_C_P	63 70	
DP_INT_ML_F_P<0>	63 70	
DP_INT_ML_F_N<0>	63 70	
DP_INT_ML_F_P<1>	63 70	
DP_INT_ML_F_N<1>	63 70	

(Need 2 TPs)  
(Need 2 TPs)

## Misc Voltages & Control Signals

FUNC_TEST	TP	NC
PPBUS_G3H	7 53	
PPVIN_SW_T29BST	7 36	
PPBUS_S5_HS_COMPUTING_ISNS	7	
PPDCIN_G3H	7	
PP3V42_G3H	7	
PPVRTC_G3H	7	
PP5V_S5	7	
PP5V_SUS	7	
PP3V3_S5	7 74	
PP3V3_SUS	7	
PP3V3_S3	7	
PP1V8_S0	7	
PP3V3_S0	7 74	
PP1V5_S3	7 68	
PP1V5_S3RS0	7 68	
PP1V5_S0	7	
PP1V05_S0	7	
PPVTTDDR_S3	7	
PP0V75_S0_DDRVTT	7	
PPVCCSA_S0_CPU	7	
PP1V05_SUS	7	
PP1V5_T29	7	
PP3V3_T29	7	
PP1V05_T29	7 36	
PP1V05_S0_PCH_VCCADPLL	7	
PPVCORE_S0_CPU	7	
PPVCORE_S0_AXG	7	
PP1V5_S3_CPU_VCCDQ	7	
PP1V05_S0_CPU_VCCPQE	7	
PP1V8_S0_CPU_VCCPLL_R	7	

(Need to add 27 GND TPs)

## J5715: KB BKLT CONNECTOR

FUNC_TEST	TP	NC
KBDLED_FB	49	
KBDLED_ANODE	49	

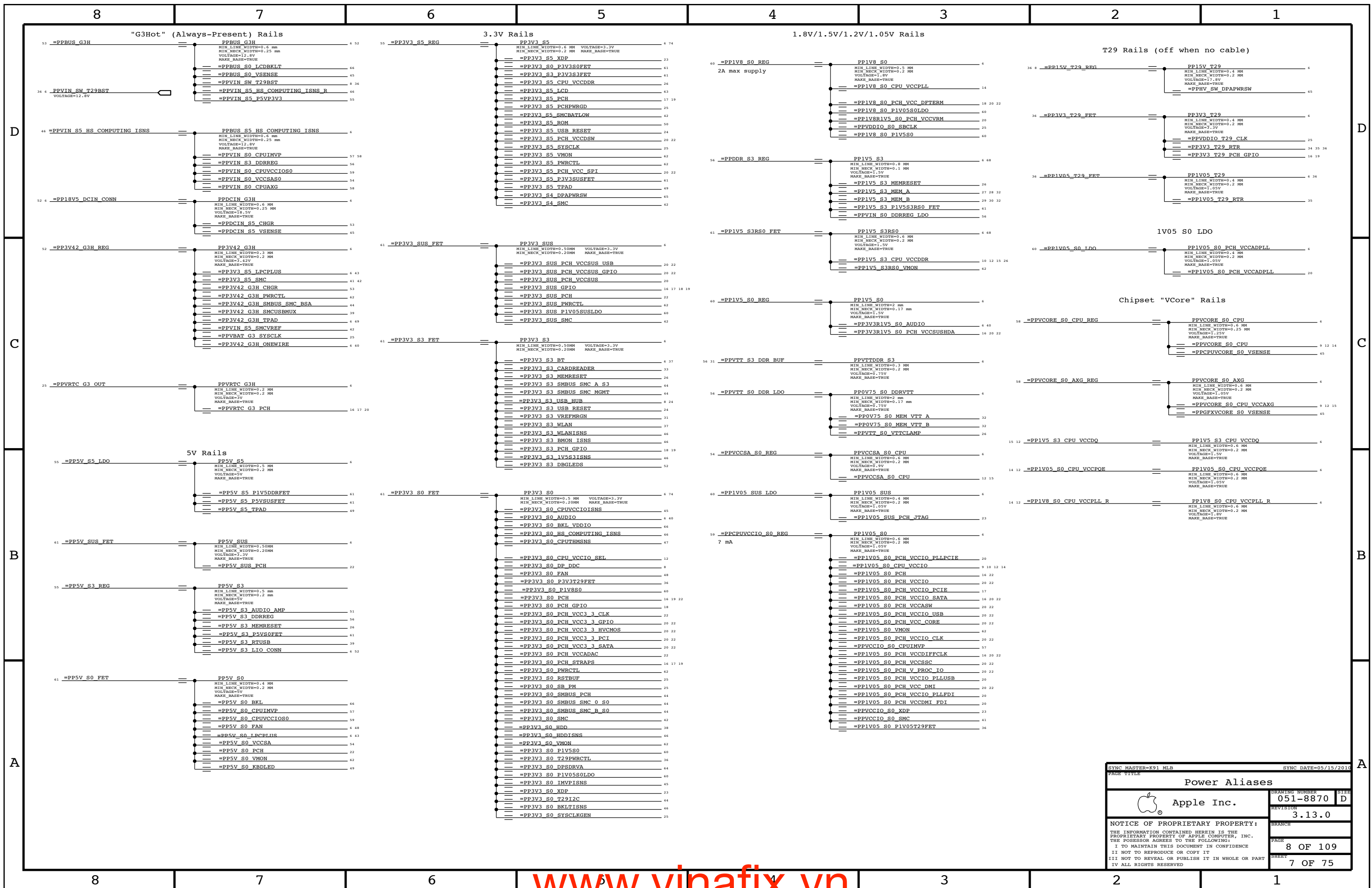
(Need to add 2 GND TP)

## NO\_TEST Nets

FUNC_TEST	TP	NC
TP_PROC_P1_3		NC_PROC_P1_3
TP_SATA_B_D2RN		NC_SATA_B_D2RN
TP_SATA_B_D2RP		NC_SATA_B_D2RP
TP_SATA_B_R2D_CN		NC_SATA_B_R2D_CN
TP_SATA_B_R2D_CP		NC_SATA_B_R2D_CP
TP_SATA_D_D2RN		NC_SATA_D_D2RN
TP_SATA_D_D2RP		NC_SATA_D_D2RP
TP_SATA_D_R2D_CN		NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP		NC_SATA_D_R2D_CP
TP_SATA_E_D2RN		NC_SATA_E_D2RN
TP_SATA_E_D2RP		NC_SATA_E_D2RP
TP_SATA_E_R2D_CN		NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP		NC_SATA_E_R2D_CP
TP_SATA_F_D2RN		NC_SATA_F_D2RN
TP_SATA_F_D2RP		NC_SATA_F_D2RP
TP_SATA_F_R2D_CN		NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP		NC_SATA_F_R2D_CP
TP_PCH_TP18		NC_PCH_TP18
TP_PCH_TP17		NC_PCH_TP17
TP_PCH_TP16		NC_PCH_TP16
TP_PCH_TP15		NC_PCH_TP15
TP_PCH_TP14		NC_PCH_TP14
TP_PCH_TP13		NC_PCH_TP13
TP_PCH_TP12		NC_PCH_TP12
TP_PCH_TP10		NC_PCH_TP10
TP_PCH_TP9		NC_PCH_TP9
TP_PCH_TP8		NC_PCH_TP8
TP_PCH_TP7		NC_PCH_TP7
TP_PCH_TP6		NC_PCH_TP6
TP_PCH_TP5		NC_PCH_TP5
TP_PCH_TP4		NC_PCH_TP4
TP_PCH_TP3		NC_PCH_TP3
TP_PCH_TP2		NC_PCH_TP2
TP_PCH_TP1		NC_PCH_TP1
PCH_VSS_NCTF<1>	70	PCH_VSS_NCTF<15>
PCH_VSS_NCTF<2>	70	PCH_VSS_NCTF<17>
PCH_VSS_NCTF<3>	70	PCH_VSS_NCTF<19>
PCH_VSS_NCTF<4>	70	PCH_VSS_NCTF<21>
PCH_VSS_NCTF<5>	70	PCH_VSS_NCTF<23>
PCH_VSS_NCTF<6>	70	PCH_VSS_NCTF<25>
PCH_VSS_NCTF<7>	70	PCH_VSS_NCTF<27>
PCH_VSS_NCTF<8>	70	PCH_VSS_NCTF<29>
TP_SVDO_TVCLKINH		NC_SVDO_TVCLKINH
TP_SVDO_TVCLKINP		NC_SVDO_TVCLKINP
TP_SVDO_STALIN		NC_SVDO_STALIN
TP_SVDO_STALIP		NC_SVDO_STALIP
TP_SVDO_INTN		NC_SVDO_INTN
TP_SVDO_INTP		NC_SVDO_INTP
TP_XDP_PCH_OBSPN_A<0..1>		NC_TP_XDP_PCH_OBSPN_A<0..1>
TP_XDP_PCH_OBSPN_B<0..1>		NC_TP_XDP_PCH_OBSPN_B<0..1>
TP_XDP_PCH_HOOK2		NC_TP_XDP_PCH_HOOK2
TP_XDP_PCH_HOOK3		NC_TP_XDP_PCH_HOOK3
TP_XDP_PCH_OBSPN_D<0..1>		NC_TP_XDP_PCH_OBSPN_D<0..1>
TP_XDP_PCH_HOOK4		NC_TP_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5		NC_TP_XDP_PCH_HOOK5
TP_PCH_GPI064_CLKOUTFLEX0		NC_PCH_GPI064_CLKOUTFLEX0
TP_PCH_GPI065_CLKOUTFLEX1		NC_PCH_GPI065_CLKOUTFLEX1
TP_PCH_GPI066_CLKOUTFLEX2		NC_PCH_GPI066_CLKOUTFLEX2
TP_PCH_GPI067_CLKOUTFLEX3		NC_PCH_GPI067_CLKOUTFLEX3

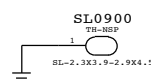
FUNC_TEST	TP	NC
NC_EDP_TXP<0..3>		TP_EDP_TX_P<0..3>
MAKE_BASE=TRUE		TP_EDP_TX_N<0..3>
NC_EDP_TXN<0..3>		TP_EDP_AUX_P
MAKE_BASE=TRUE		TP_EDP_AUX_N
NC_EDP_AUXN		TP_CPU_THERMDA
MAKE_BASE=TRUE		TP_CPU_THERMDC
NC_CPU_THERMDA		TP_CPU_RSVD<30..45>
MAKE_BASE=TRUE		TP_CPU_RSVD<30..45>
NC_CPU_THERMDC		TP_CPU_RSVD<8..27>
MAKE_BASE=TRUE		TP_PEG_R2D_CP<15..4>
NC_PEG_R2D_CP<15..4>		TP_PEG_R2D_CN<15..4>
MAKE_BASE=TRUE		TP_PEG_R2D_CN<15..4>
NC_PEG_R2D_CN<15..4>		TP_PEG_D2R_P<15..4>
MAKE_BASE=TRUE		TP_PEG_D2R_N<15..4>
NC_PEG_D2R_P<15..4>		
MAKE_BASE=TRUE		
TP_PCH_CLK100M_PEN4		NC_PCH_CLK100M_PEN4
TP_PCH_CLK100M_PEN5		NC_PCH_CLK100M_PEN5
TP_PCH_CLK100M_PEN6		NC_PCH_CLK100M_PEN6
TP_PCH_CLK100M_PEN7		NC_PCH_CLK100M_PEN7
TP_PCH_CLK100M_PEN8		NC_PCH_CLK100M_PEN8
TP_PCH_CLK100M_PEN9		NC_PCH_CLK100M_PEN9
TP_PCH_CLK100M_PEN10		NC_PCH_CLK100M_PEN10
TP_PCH_CLK100M_PEN11		NC_PCH_CLK100M_PEN11
TP_PCH_CLK100M_PEN12		NC_PCH_CLK100M_PEN12
TP_PCH_CLK100M_PEN13		NC_PCH_CLK100M_PEN13
TP_PCH_CLK100M_PEN14		NC_PCH_CLK100M_PEN14
TP_PCH_CLK100M_PEN15		NC_PCH_CLK100M_PEN15
TP_PCH_CLK100M_PEN16		NC_PCH_CLK100M_PEN16
TP_PCH_CLK100M_PEN17		NC_PCH_CLK100M_PEN17
TP_PCH_CLK100M_PEN18		NC_PCH_CLK100M_PEN18
TP_PCH_CLK100M_PEN19		NC_PCH_CLK100M_PEN19
TP_PCH_CLK100M_PEN20		NC_PCH_CLK100M_PEN20
TP_PCH_CLK100M_PEN21		NC_PCH_CLK100M_PEN21
TP_PCH_CLK100M_PEN22		NC_PCH_CLK100M_PEN22
TP_PCH_CLK100M_PEN23		NC_PCH_CLK100M_PEN23
TP_PCH_CLK100M_PEN24		NC_PCH_CLK100M_PEN24
TP_PCH_CLK100M_PEN25		NC_PCH_CLK100M_PEN25
TP_PCH_CLK100M_PEN26		NC_PCH_CLK100M_PEN26
TP_PCH_CLK100M_PEN27		NC_PCH_CLK100M_PEN27
TP_PCH_CLK100M_PEN28		NC_PCH_CLK100M_PEN28
TP_PCH_CLK100M_PEN29		NC_PCH_CLK100M_PEN29
TP_PCH_CLK100M_PEN30		NC_PCH_CLK100M_PEN30
TP_PCH_CLK100M_PEN31		NC_PCH_CLK100M_PEN31
TP_PCH_CLK100M_PEN32		NC_PCH_CLK100M_PEN32
TP_PCH_CLK100M_PEN33		NC_PCH_CLK100M_PEN33
TP_PCH_CLK100M_PEN34		NC_PCH_CLK100M_PEN34
TP_PCH_CLK100M_PEN35		NC_PCH_CLK100M_PEN35
TP_PCH_CLK100M_PEN36		NC_PCH_CLK100M_PEN36
TP_PCH_CLK100M_PEN37		NC_PCH_CLK100M_PEN37
TP_PCH_CLK100M_PEN38		NC_PCH_CLK100M_PEN38
TP_PCH_CLK100M_PEN39		NC_PCH_CLK100M_PEN39
TP_PCH_CLK100M_PEN40		NC_PCH_CLK100M_PEN40
TP_PCH_CLK100M_PEN41		NC_PCH_CLK100M_PEN41
TP_PCH_CLK100M_PEN42		NC_PCH_CLK100M_PEN42
TP_PCH_CLK100M_PEN43		NC_PCH_CLK100M_PEN43
TP_PCH_CLK100M_PEN44		NC_PCH_CLK100M_PEN44
TP_PCH_CLK100M_PEN45		NC_PCH_CLK100M_PEN45
TP_PCH_CLK100M_PEN46		NC_PCH_CLK100M_PEN46
TP_PCH_CLK100M_PEN47		NC_PCH_CLK100M_PEN47
TP_PCH_CLK100M_PEN48		NC_PCH_CLK100M_PEN48
TP_PCH_CLK100M_PEN49		NC_PCH_CLK100M_PEN49
TP_PCH_CLK100M_PEN50		NC_PCH_CLK100M_PEN50
TP_PCH_CLK100M_PEN51		NC_PCH_CLK100M_PEN51
TP_PCH_CLK100M_PEN52		NC_PCH_CLK100M_PEN52
TP_PCH_CLK100M_PEN53		NC_PCH_CLK100M_PEN53
TP_PCH_CLK100M_PEN54		NC_PCH_CLK100M_PEN54
TP_PCH_CLK100M_PEN55		NC_PCH_CLK100M_PEN55
TP_PCH_CLK100M_PEN56		NC_PCH_CLK100M_PEN56
TP_PCH_CLK100M_PEN57		NC_PCH_CLK100M_PEN57
TP_PCH_CLK100M_PEN58		NC_PCH_CLK100M_PEN58
TP_PCH_CLK100M_PEN59		NC_PCH_CLK100M_PEN59
TP_PCH_CLK100M_PEN60		NC_PCH_CLK100M_PEN60
TP_PCH_CLK100M_PEN61		NC_PCH_CLK100M_PEN61
TP_PCH_CLK100M_PEN62		NC_PCH_CLK100M_PEN62
TP_PCH_CLK100M_PEN63		NC_PCH_CLK100M_PEN63
TP_PCH_CLK100M_PEN64		NC_PCH_CLK100M_PEN64
TP_PCH_CLK100M_PEN65		NC_PCH_CLK100M_PEN65
TP_PCH_CLK100M_PEN66		NC_PCH_CLK100M_PEN66
TP_PCH_CLK100M_PEN67		NC_PCH_CLK100M_PEN67
TP_PCH_CLK100M_PEN68		NC_PCH_CLK100M_PEN68
TP_PCH_CLK100M_PEN69		NC_PCH_CLK100M_PEN69
TP_PCH_CLK100M_PEN70		NC_PCH_CLK100M_PEN70
TP_PCH_CLK100M_PEN71		NC_PCH_CLK100M_PEN71
TP_PCH_CLK100M_PEN72		NC_PCH_CLK100M_PEN72
TP_PCH_CLK100M_PEN73		NC_PCH_CLK100M_PEN73
TP_PCH_CLK100M_PEN74		NC_PCH_CLK100M_PEN74
TP_PCH_CLK100M_PEN75		NC_PCH_CLK100M_PEN75
TP_PCH_CLK100M_PEN76		NC_PCH_CLK100M_PEN76
TP_PCH_CLK100M_PEN77		



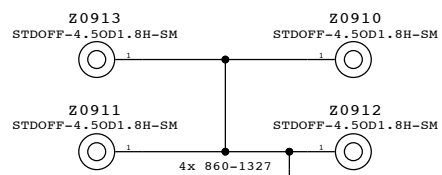


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 REVISION: 3.13.0  
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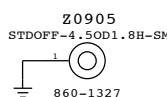
### Plated Board Slot



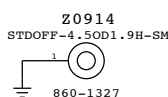
### CPU Heat Sink Mounting Bosses



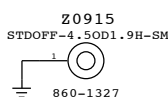
### Fan Boss



### X21 Boss

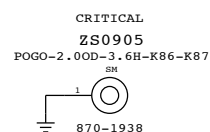


### SSD Boss

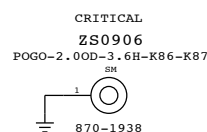


### EMI I/O Pogo Pins

#### DisplayPort Pogo

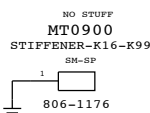


#### USB/SD Card Pogo

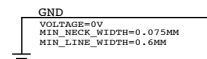


### DisplayPort PCB Stiffener

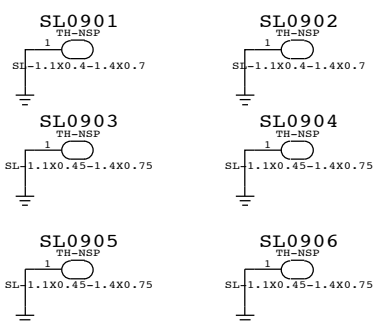
(Provides PCB support for small finger above J9400)



### Digital Ground



### T29 Can Slots



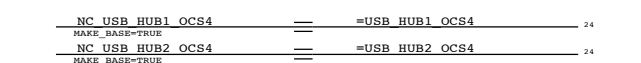
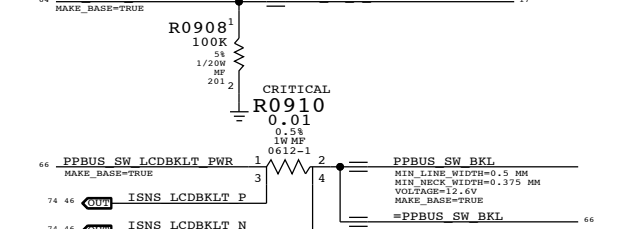
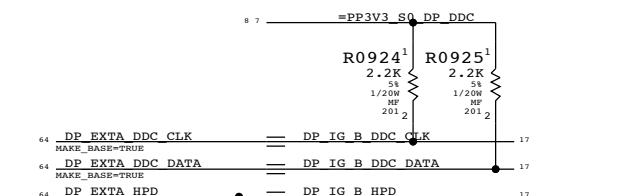
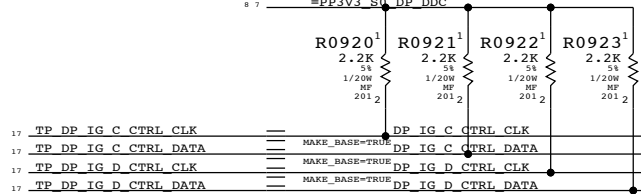
### CPU signals

26	MEMVTT EN	==	DDRVT EN	26	56
70	DP_EXTA_ML_C_P<3..0>	==	DP_IG_ML_P<3..0>	17	7
70	DP_EXTA_ML_C_N<3..0>	==	DP_IG_ML_N<3..0>	17	7
70	DP_EXTA_AUXCH_C_P	==	DP_IG_AUX_CH_P	17	7
70	DP_EXTA_AUXCH_C_N	==	DP_IG_AUX_CH_N	17	7
16	PCIE_EXCARD_D2R_N	==	NC_PCIE_EXCARD_D2RN	16	16
16	PCIE_EXCARD_D2R_P	==	NC_PCIE_EXCARD_D2RP	16	16
16	PCIE_EXCARD_R2D_C_N	==	NC_PCIE_EXCARD_R2D_CN	16	16
16	PCIE_EXCARD_R2D_C_P	==	NC_PCIE_EXCARD_R2D_CP	16	16
70	PCIE_CLK100M_EXCARD_N	==	NC_PCIE_CLK100M_EXCARDN	70	16
70	PCIE_CLK100M_EXCARD_P	==	NC_PCIE_CLK100M_EXCARDP	70	16
70	PEG_CLK100M_P	==	NC_PEG_CLK100MP	70	16
70	PEG_CLK100M_N	==	NC_PEG_CLK100MN	70	16
68	MEM_A_CLK_P<1>	==	TP_MEM_A_CLKP<1>	68	11
68	MEM_A_CLK_N<1>	==	TP_MEM_A_CLKN<1>	68	11
68	MEM_A_CKE<1>	==	NC_MEM_A_CKE<1>	68	11
68	MEM_A_CS_L<1>	==	NC_MEM_A_CS_L<1>	68	11
68	MEM_A_ODT<1>	==	NC_MEM_A_ODT<1>	68	11
68	MEM_B_CLK_P<1>	==	TP_MEM_B_CLKP<1>	68	11
68	MEM_B_CLK_N<1>	==	TP_MEM_B_CLKN<1>	68	11
68	MEM_B_CKE<1>	==	NC_MEM_B_CKE<1>	68	11
68	MEM_B_CS_L<1>	==	NC_MEM_B_CS_L<1>	68	11
68	MEM_B_ODT<1>	==	NC_MEM_B_ODT<1>	68	11
68	MEM_A_A<15>	==	TP_MEM_A_A<15>	68	11
68	MEM_B_A<15>	==	TP_MEM_B_A<15>	68	11
10	DP_PCH_CLKOUT_DPN	==	DP_PCH_CLK_N	10	67
10	DP_PCH_CLKOUT_DPP	==	DP_PCH_CLK_P	10	67

9	PEG_R2D_C_P<3..0>	==	PEG_R2D_C_P<3..0>	34	70
9	PEG_R2D_C_N<3..0>	==	PEG_R2D_C_N<3..0>	34	70
9	PEG_D2R_P<3..0>	==	PEG_D2R_P<3..0>	34	70
9	PEG_D2R_N<3..0>	==	PEG_D2R_N<3..0>	34	70

### T29 DP Ports

17	TP_DP_IG_C_HPD	==	DP_T29SNKO_HPD	34	70
17	TP_DP_IG_C_MLP<3..0>	==	DP_T29SNKO_ML_C_P<3..0>	34	70
17	TP_DP_IG_C_MLN<3..0>	==	DP_T29SNKO_ML_C_N<3..0>	34	70
17	TP_DP_IG_C_AUXP	==	DP_T29SNKO_AUXCH_C_P	34	70
17	TP_DP_IG_C_AUXN	==	DP_T29SNKO_AUXCH_C_N	34	70
17	TP_DP_IG_D_HPD	==	DP_IG_D_HPD	34	70



### LVDS Aliases

6	TP_LVDS_IG_B_CLKP	==	LVDS_IG_B_CLK_P	69	17
6	TP_LVDS_IG_B_CLKN	==	LVDS_IG_B_CLK_N	69	17
6	NC_LVDS_IG_B_DATAP<0..3>	==	LVDS_IG_B_DATA_P<0..3>	69	17
6	NC_LVDS_IG_B_DATAN<0..3>	==	LVDS_IG_B_DATA_N<0..3>	69	17
6	NC_LVDS_IG_A_DATAP<3>	==	LVDS_IG_A_DATA_P<3>	69	17
6	NC_LVDS_IG_A_DATAN<3>	==	LVDS_IG_A_DATA_N<3>	69	17
66	LCD_BKLT_PWM	==	LVDS_IG_BKL_PWM	17	17
63	LCD_IG_PWR_EN	==	LVDS_IG_PANEL_PWR	17	17
66	LCD_BKLT_EN	==	LVDS_IG_BKL_ON	17	17

### SATA Aliases

69	SATA_ODD_R2D_C_P	==	NC_SATA_ODD_R2DCP	NO_TEST=TRUE	69
69	SATA_ODD_R2D_C_N	==	NC_SATA_ODD_R2DCN	NO_TEST=TRUE	69
69	SATA_ODD_D2R_P	==	NC_SATA_ODD_D2RP	NO_TEST=TRUE	69
69	SATA_ODD_D2R_N	==	NC_SATA_ODD_D2RN	NO_TEST=TRUE	69

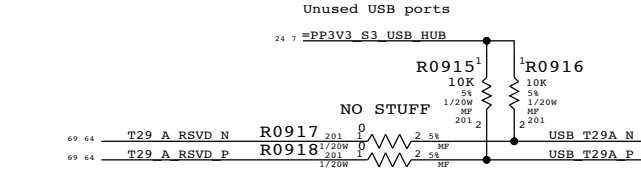
### Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE	==	P1V5S3RS0_RAMP_DONE	43
TP_DDRREG_PGOOD	==	DDRREG_PGOOD	56

### T29 JTAG

JTAG_ISP_TCK	==	JTAG_T29_TCK	24
JTAG_ISP_TDI	==	JTAG_T29_TDI	24
JTAG_ISP_TDO	==	JTAG_T29_TDO	24

### T29 Aliases



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051-8870

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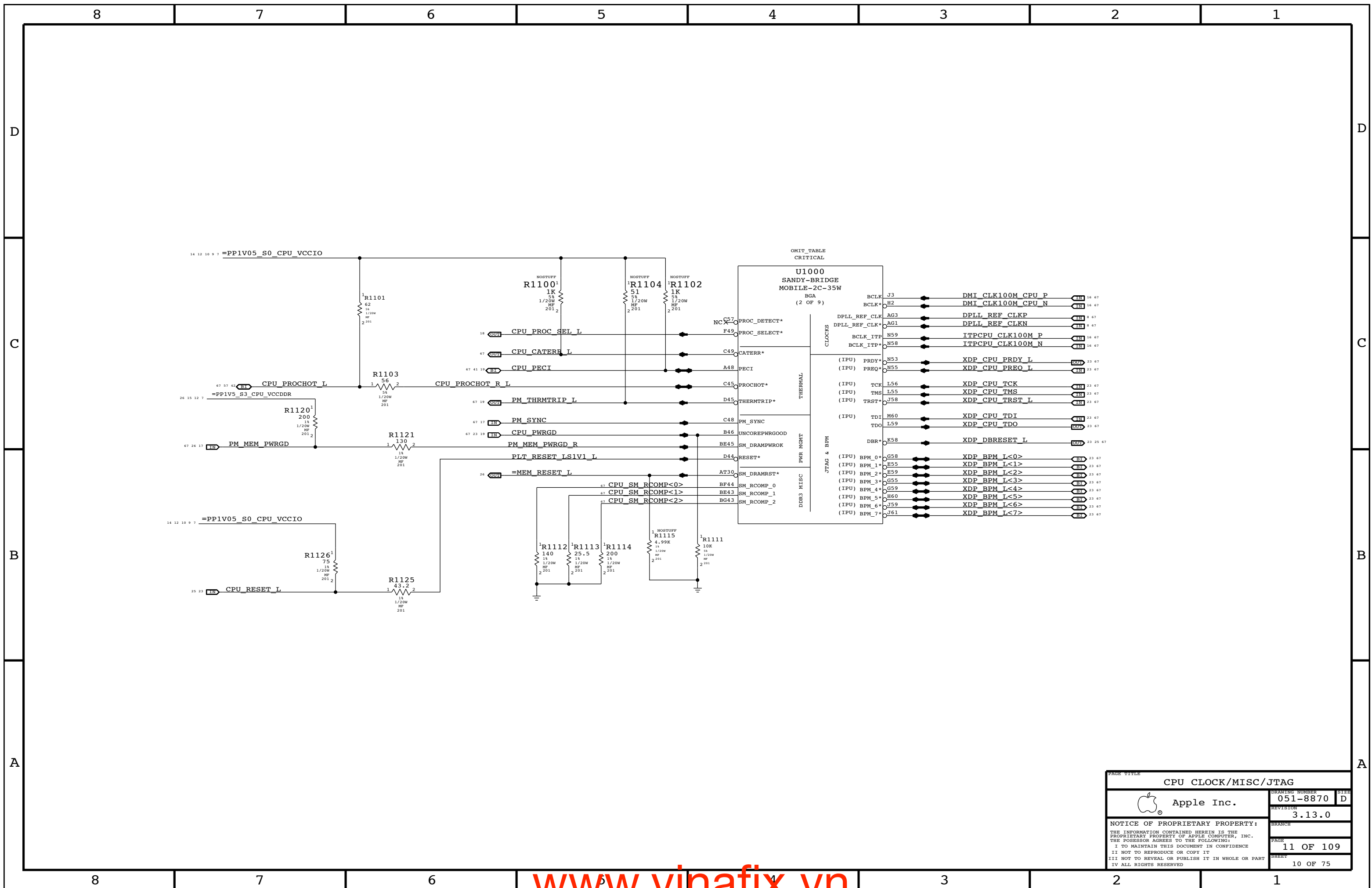
9 OF 109

8 OF 75

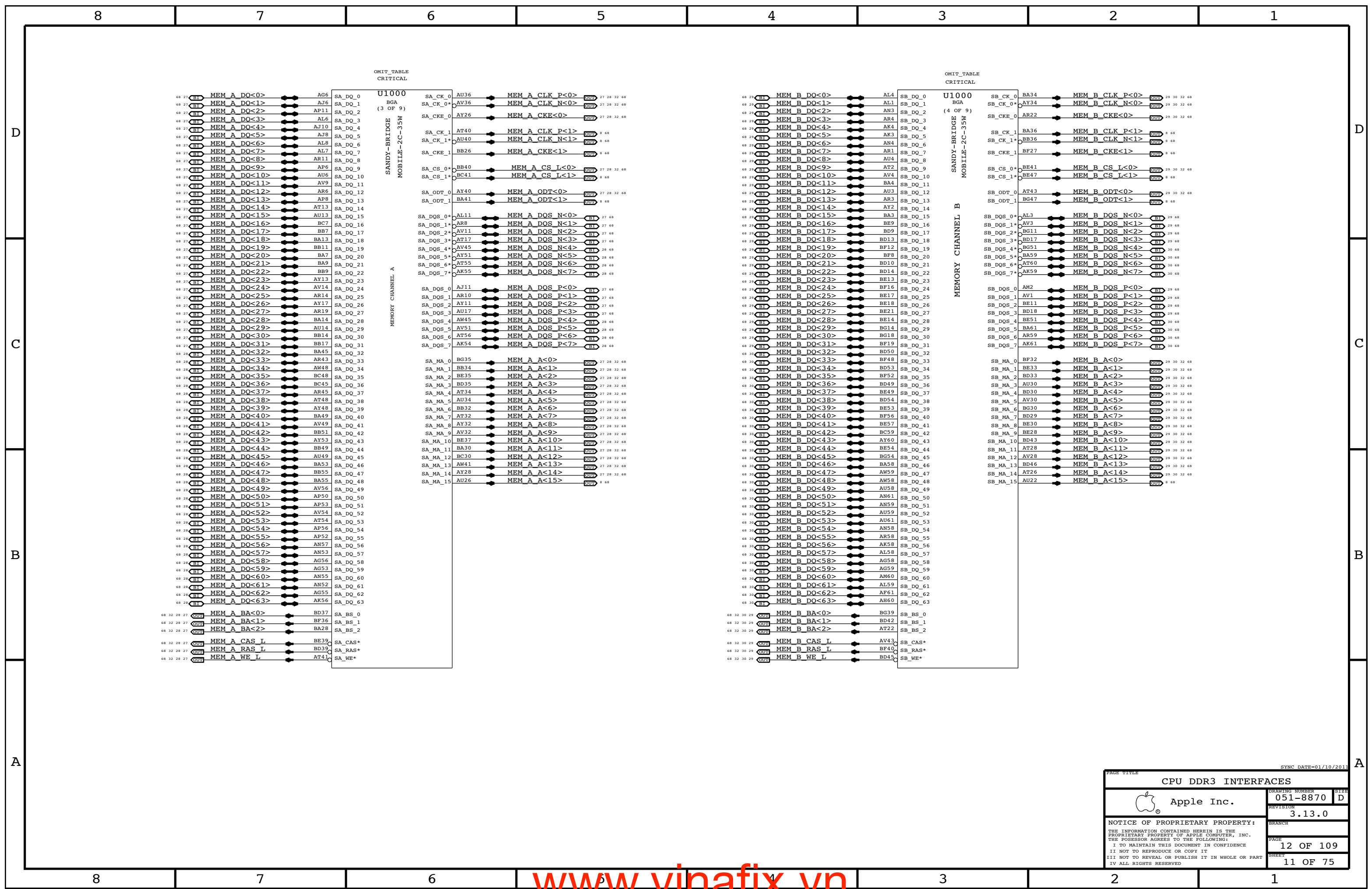
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PAGE TITLE CPU CLOCK/MISC/JTAG		
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PAGE	11 OF 109	
SHEET	10 OF 75	



OMIT TABLE  
CRITICAL

OMIT TABLE  
CRITICAL

U1000  
BGA  
(3 OF 9)

U1000  
BGA  
(4 OF 9)

SANDY-BRIDGE  
MOBILE-2C-35W

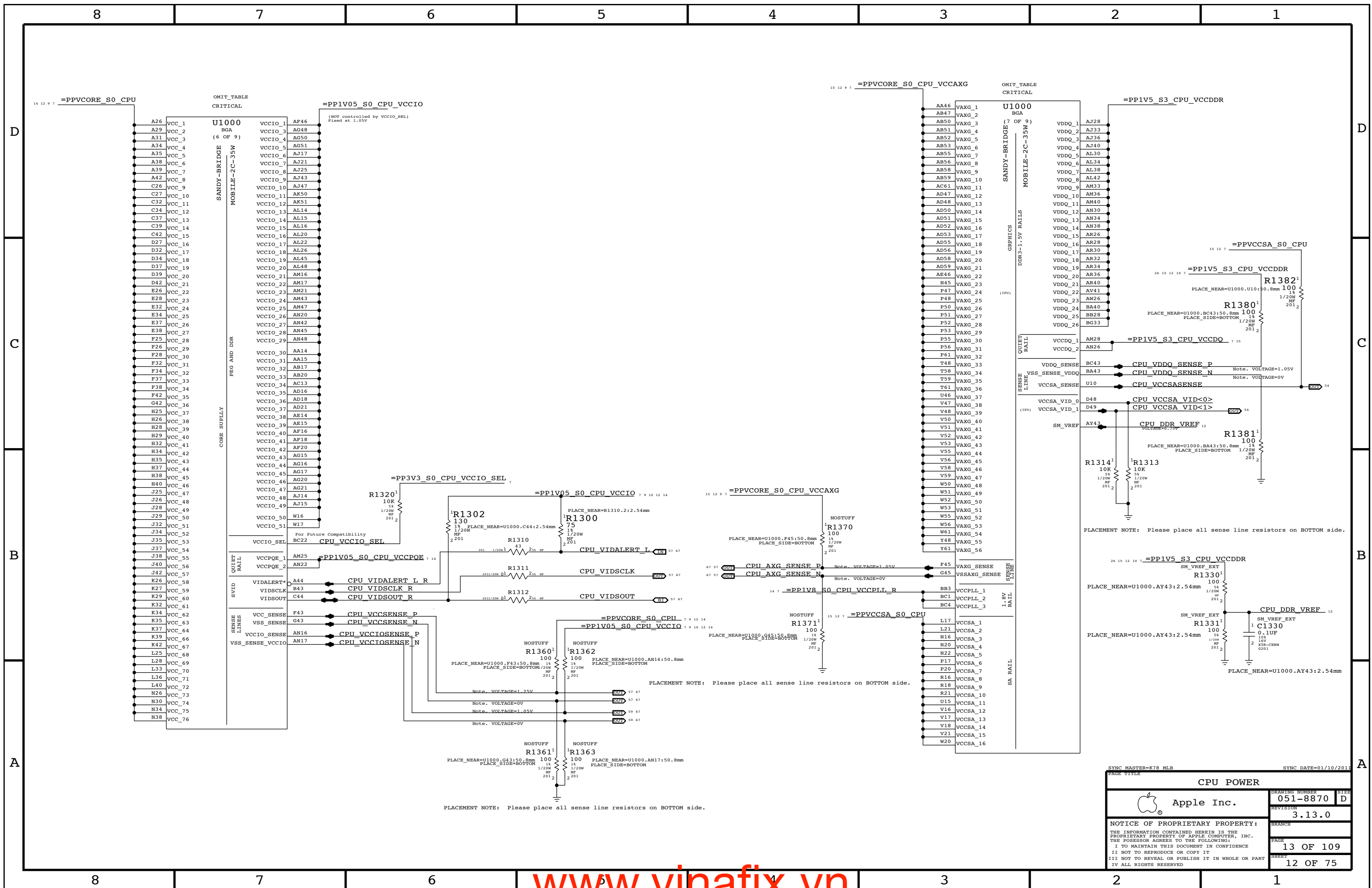
SANDY-BRIDGE  
MOBILE-2C-35W

MEMORY CHANNEL A

MEMORY CHANNEL B

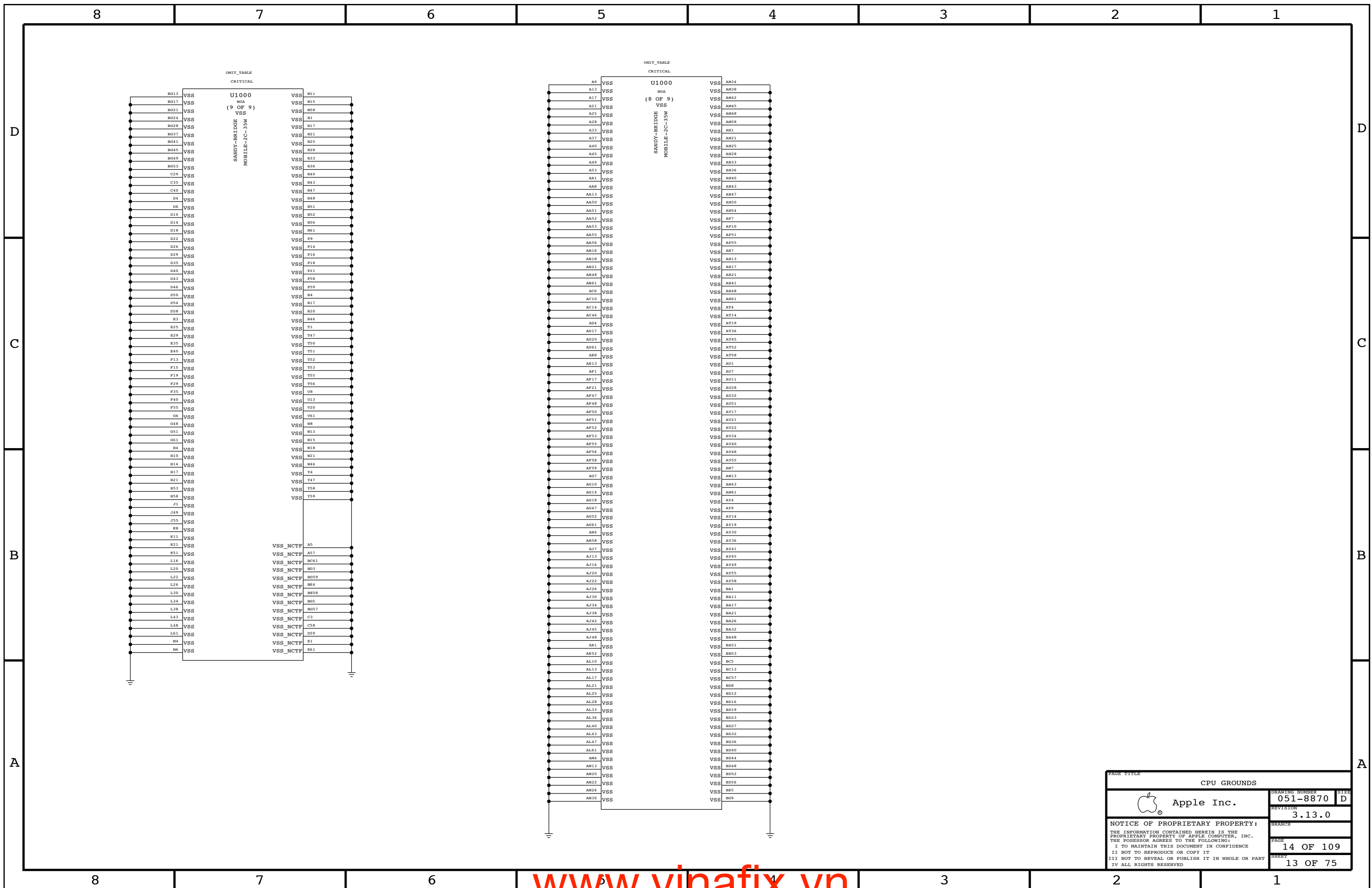
SYNC DATE=01/10/2011

<b>CPU DDR3 INTERFACES</b>		DRAWING NUMBER <b>051-8870</b>	SIZE <b>D</b>
Apple Inc.		REVISION <b>3.13.0</b>	
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PAGE TITLE		SYNC DATE=01/10/2011	
<b>CPU POWER</b>			
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		SHEET	12 OF 75





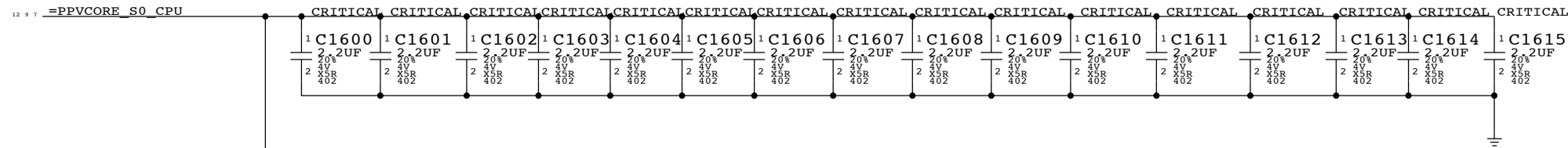
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CPU GROUNDS		
	DRAWING NUMBER	051-8870
	REVISION	3.13.0
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SHEET	13 OF 75	



Processor Load Line : -2.9 mOhms

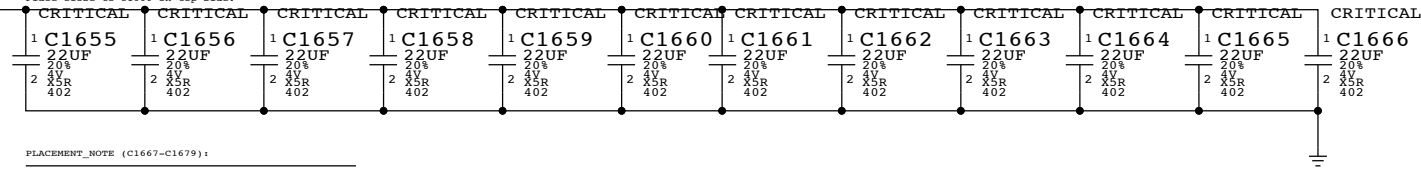
### CPU VCORE DECOUPLING

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF



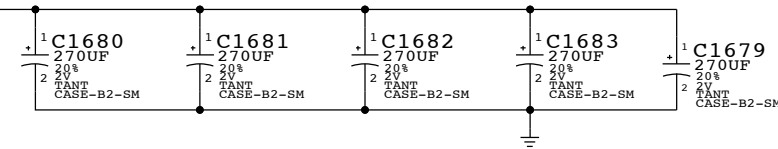
PLACEMENT\_NOTE (C1655-C1666):

Place close to U1000 on top side.



PLACEMENT\_NOTE (C1667-C1679):

PLACEMENT\_NOTE (C1640-C1645):

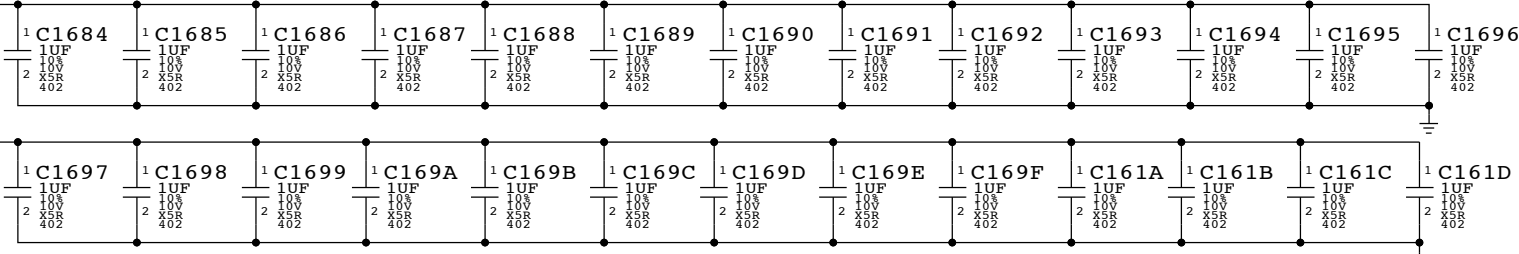


### CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

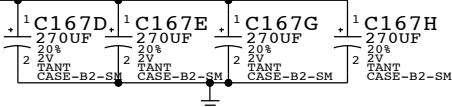
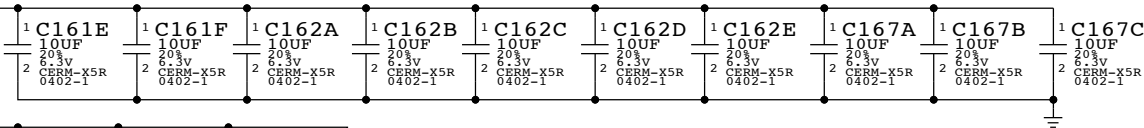
PLACEMENT\_NOTE (C1684-C1697):

Place on bottom side of U1000

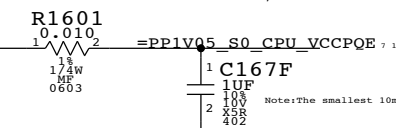


PLACEMENT\_NOTE (C1672-C1681):

Place near U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



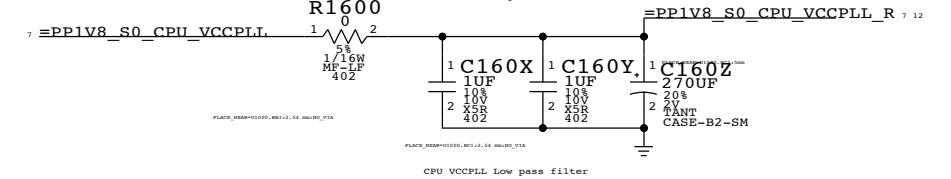
Note: The smallest 10mOhm available in the library are 0805a

### CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT\_NOTE (C1646-C1671):

Place near U1000 on top side



CPU VCCPLL Low pass filter

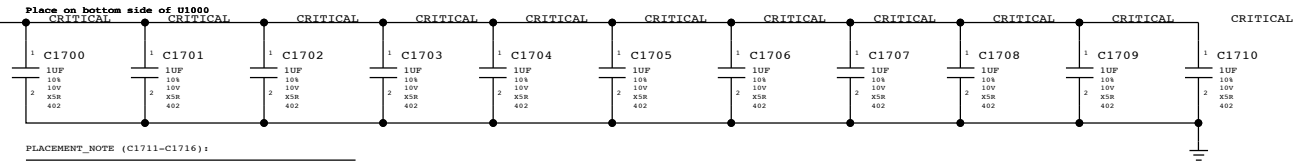
CPU DECOUPLING-I		DRAWING NUMBER	051-8870	SIZE	D
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VAXG DECOUPLING

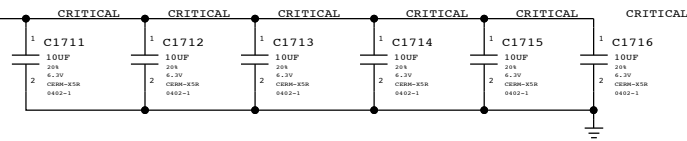
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

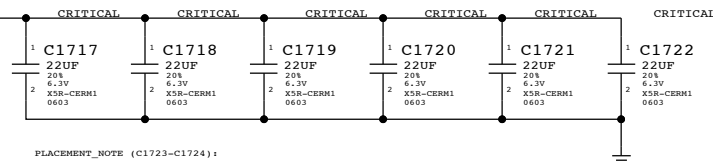
PLACEMENT\_NOTE (C1700-C1710):



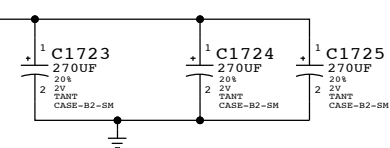
PLACEMENT\_NOTE (C1711-C1716):



PLACEMENT\_NOTE (C1717-C1722):



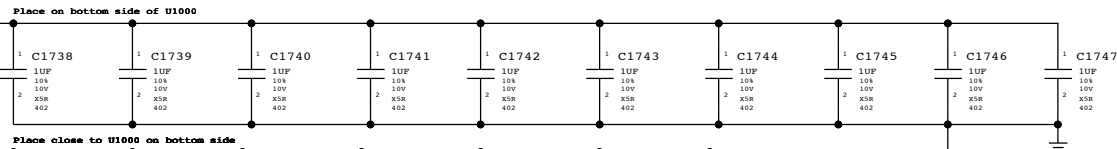
PLACEMENT\_NOTE (C1723-C1724):



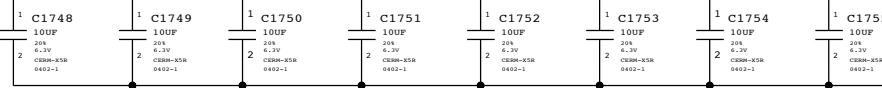
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

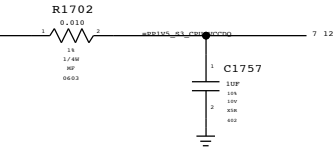
PLACEMENT\_NOTE (C1738-C1747):



Place close to U1000 on bottom side



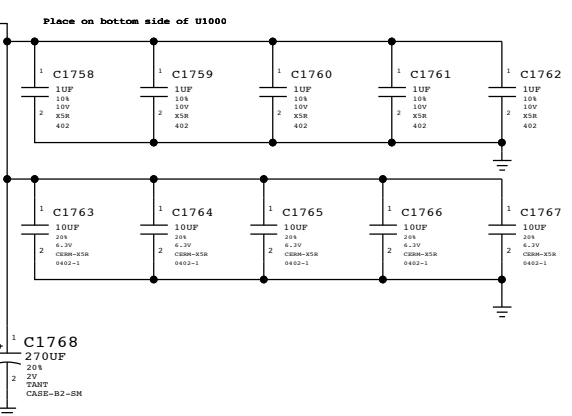
Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



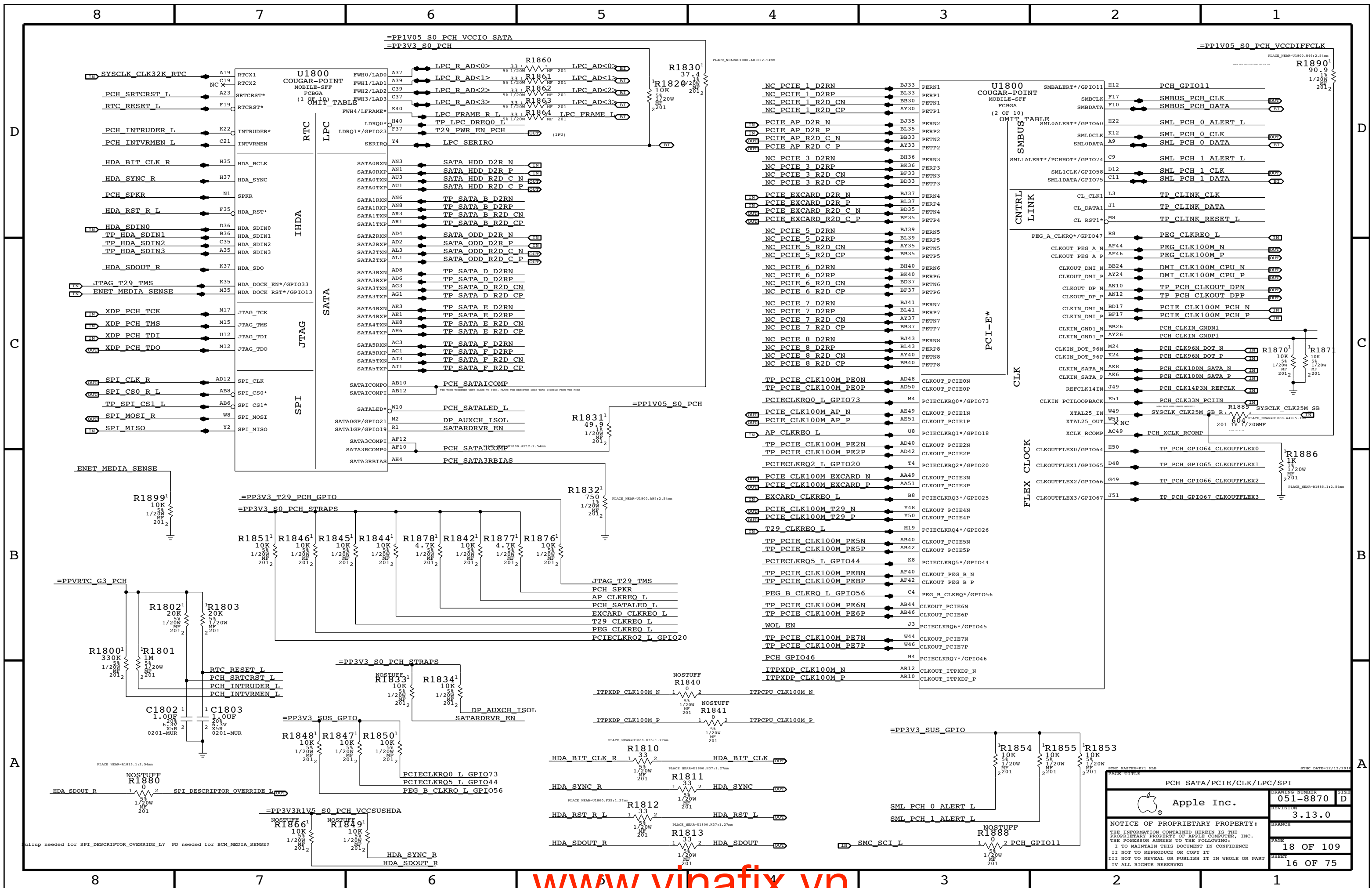
CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uF, 3x 10uF, 1x 330uF

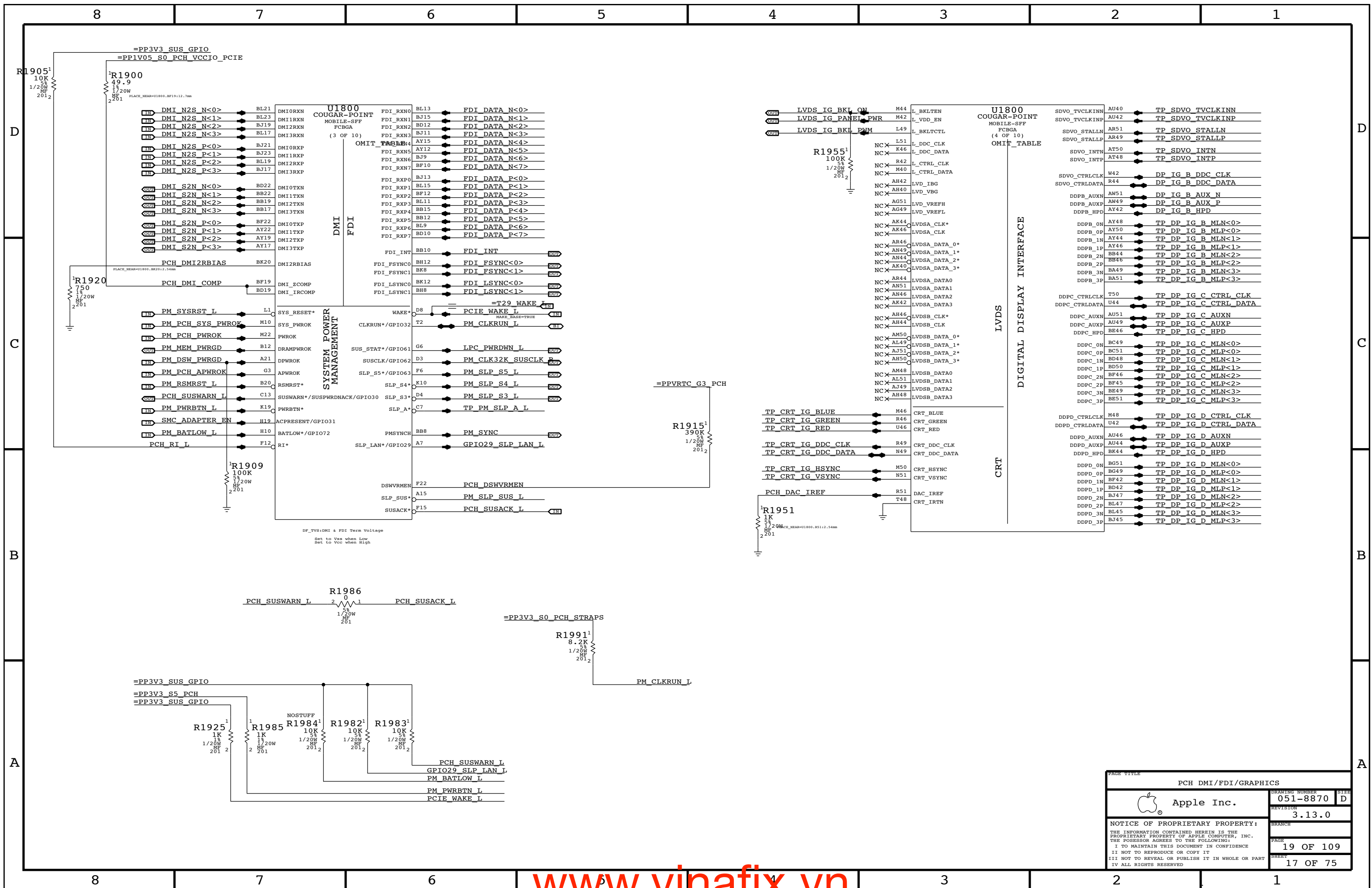
PLACEMENT\_NOTE (C1758-C1762):



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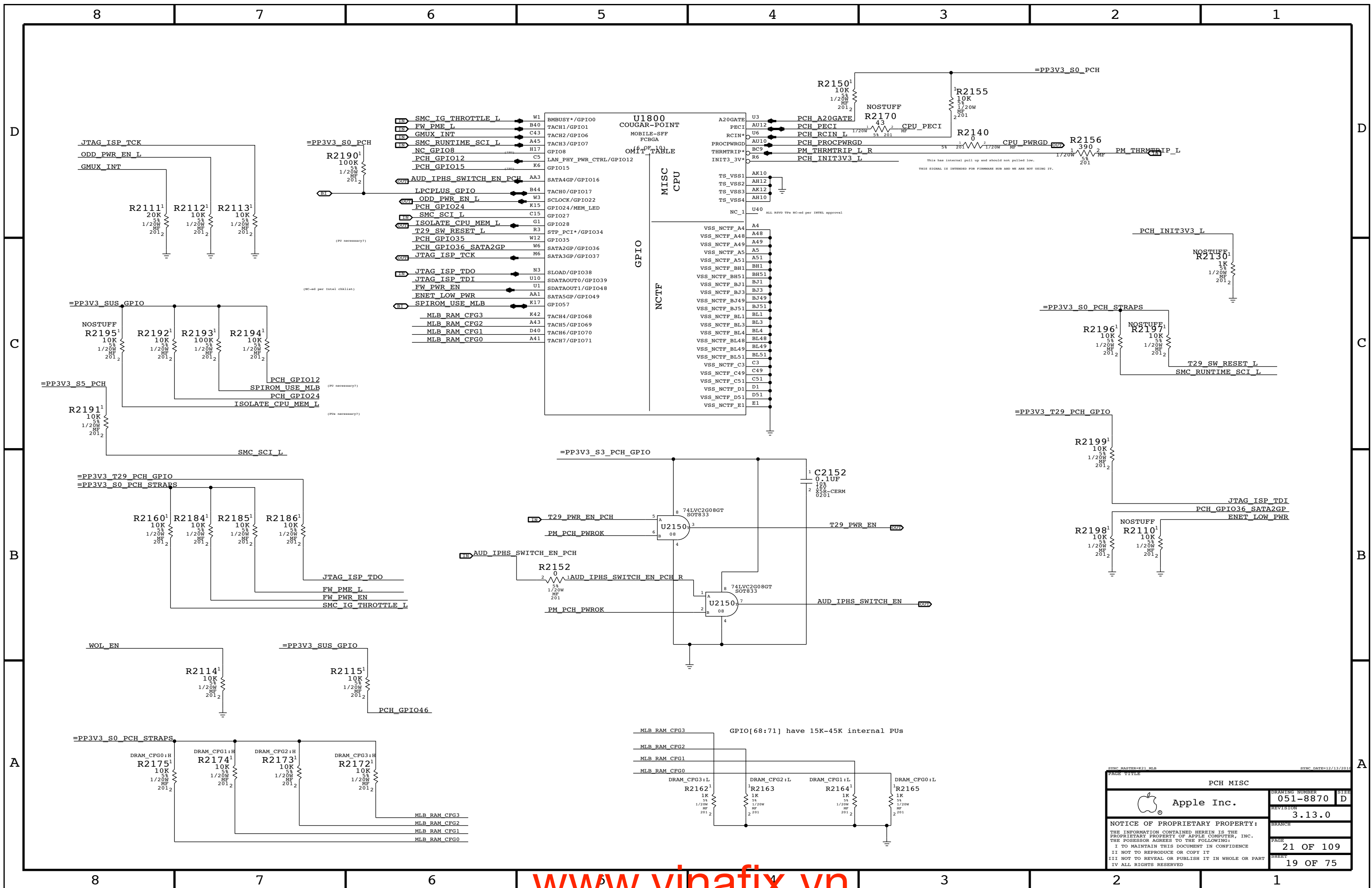
		<b>PCH SATA/PCIE/CLK/LPC/SPI</b>	
<b>Apple Inc.</b>		DRAWING NUMBER <b>051-8870</b>	SIZE <b>D</b>
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**U1800 COUGAR-POINT MOBILE-SFF PCBGA**

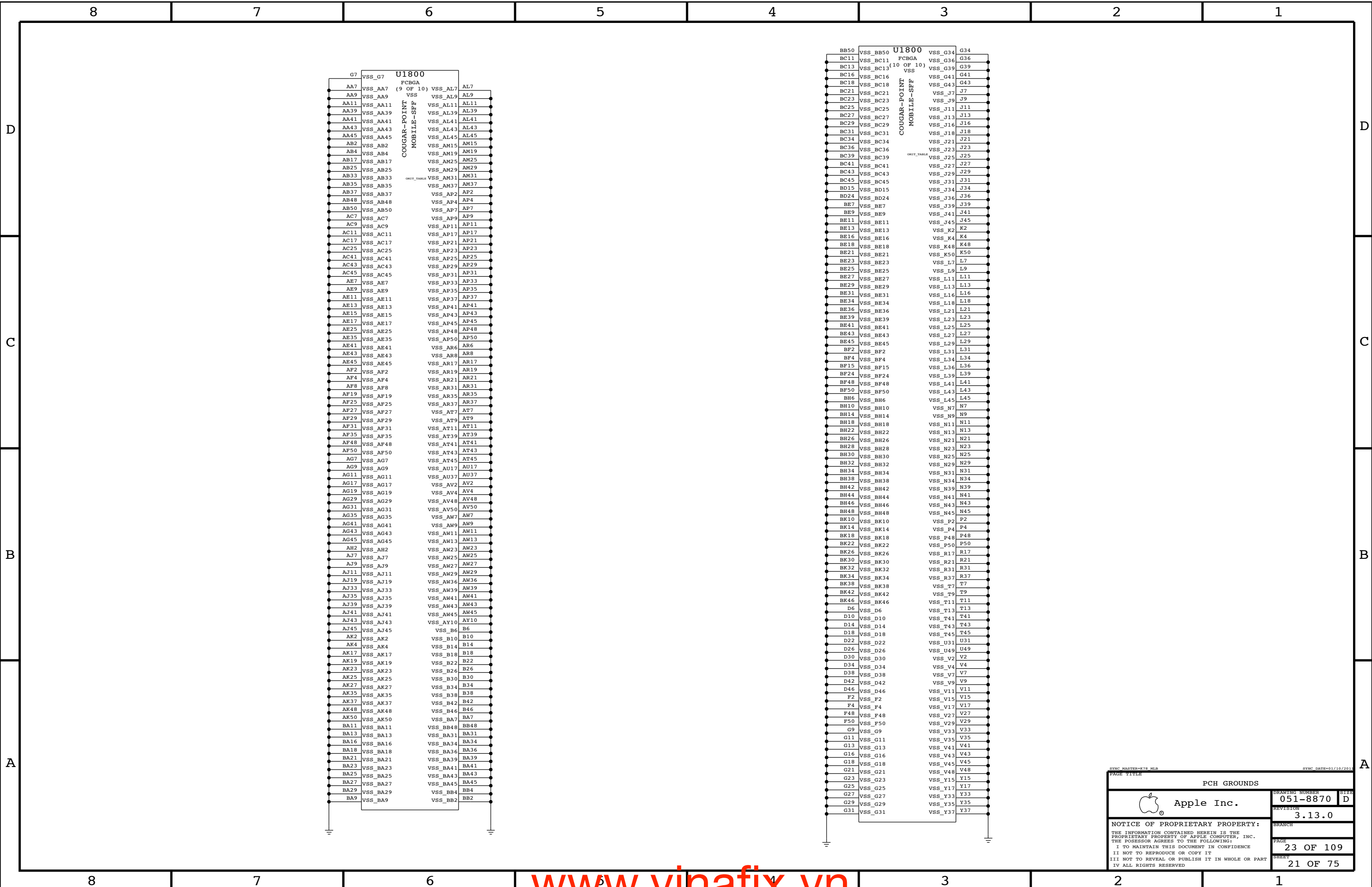
OMIT TABLE

Signal	Pin	Function
SMC_I2C_THROTTLE_L	W1	EMBUSY*/GPIO0
FW_PME_L	B40	TACH1/GPIO1
GMUX_INT	C43	TACH2/GPIO6
SMC_RUNTIME_SCI_L	A45	TACH3/GPIO7
NC_GPIO8	H17	GPIO8
PCH_GPIO12	C5	LAN_PHY_PWR_CTRL/GPIO12
PCH_GPIO15	K6	GPIO15
AUD_IPHS_SWITCH_EN_PCH	AA3	SATA4GP/GPIO16
LPCPLUS_GPIO	B44	TACH0/GPIO17
ODD_PWR_EN_L	W3	SCLOCK/GPIO22
PCH_GPIO24	K15	GPIO24/MEM_LED
SMC_SCI_L	C15	GPIO27
ISOLATE_CPU_MEM_L	G1	GPIO28
T29_SW_RESET_L	R3	STP_PCI*/GPIO34
PCH_GPIO35	W12	GPIO35
PCH_GPIO36_SATA2GP	W6	SATA2GP/GPIO36
JTAG_ISP_TCK	M6	SATA3GP/GPIO37
JTAG_ISP_TDO	N3	SLOAD/GPIO38
JTAG_ISP_TDI	U10	SDATAOUT0/GPIO39
FW_PWR_EN	U1	SDATAOUT1/GPIO48
ENET_LOW_PWR	AA1	SATA5GP/GPIO49
SPROM_USE_MLB	K17	GPIO57
MLB_RAM_CFG3	K42	TACH4/GPIO68
MLB_RAM_CFG2	A43	TACH5/GPIO69
MLB_RAM_CFG1	D40	TACH6/GPIO70
MLB_RAM_CFG0	A41	TACH7/GPIO71

GPIO[68:71] have 15K-45K internal PUs

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		3.13.0	21 OF 109
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			19 OF 75





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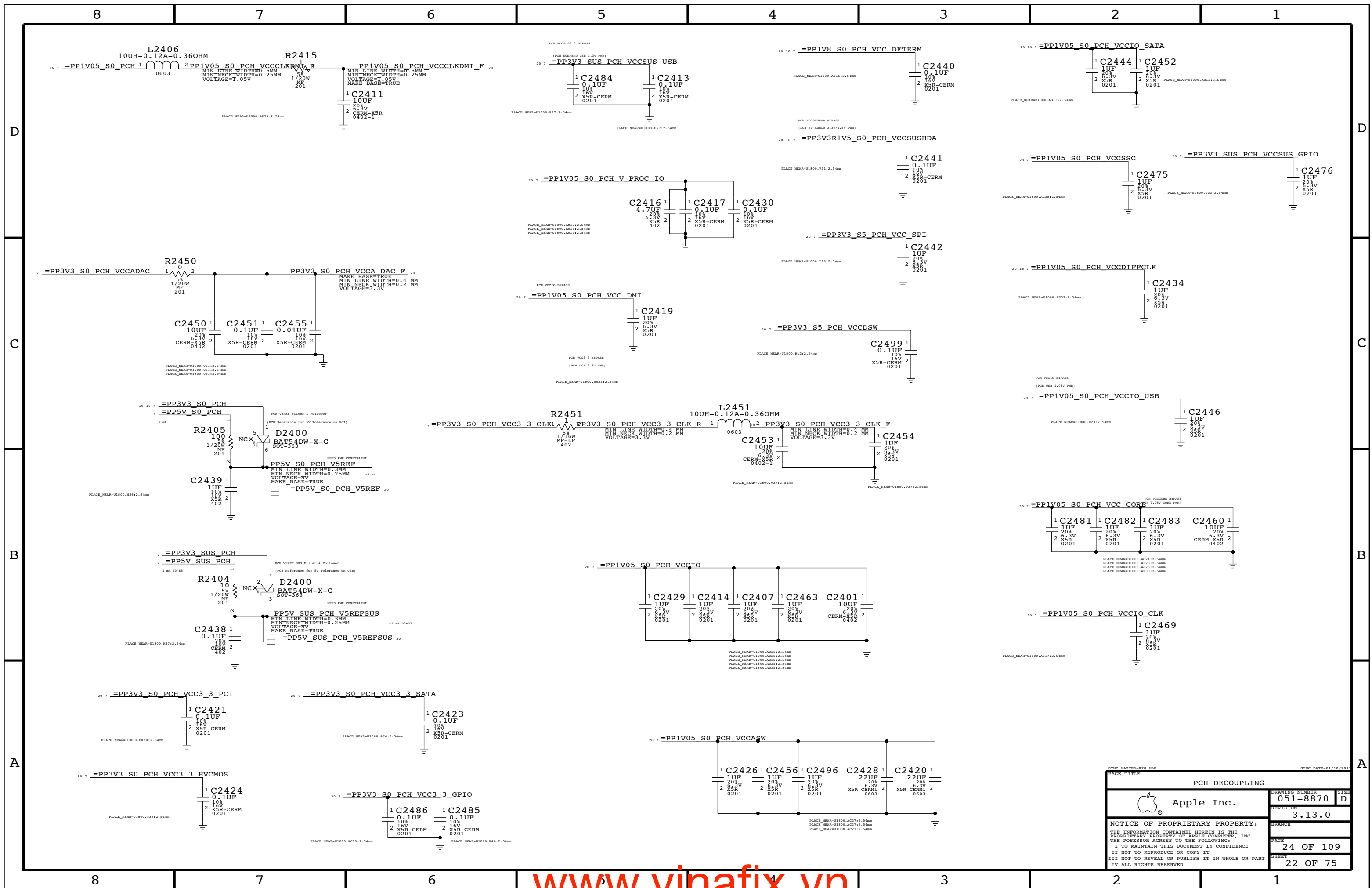
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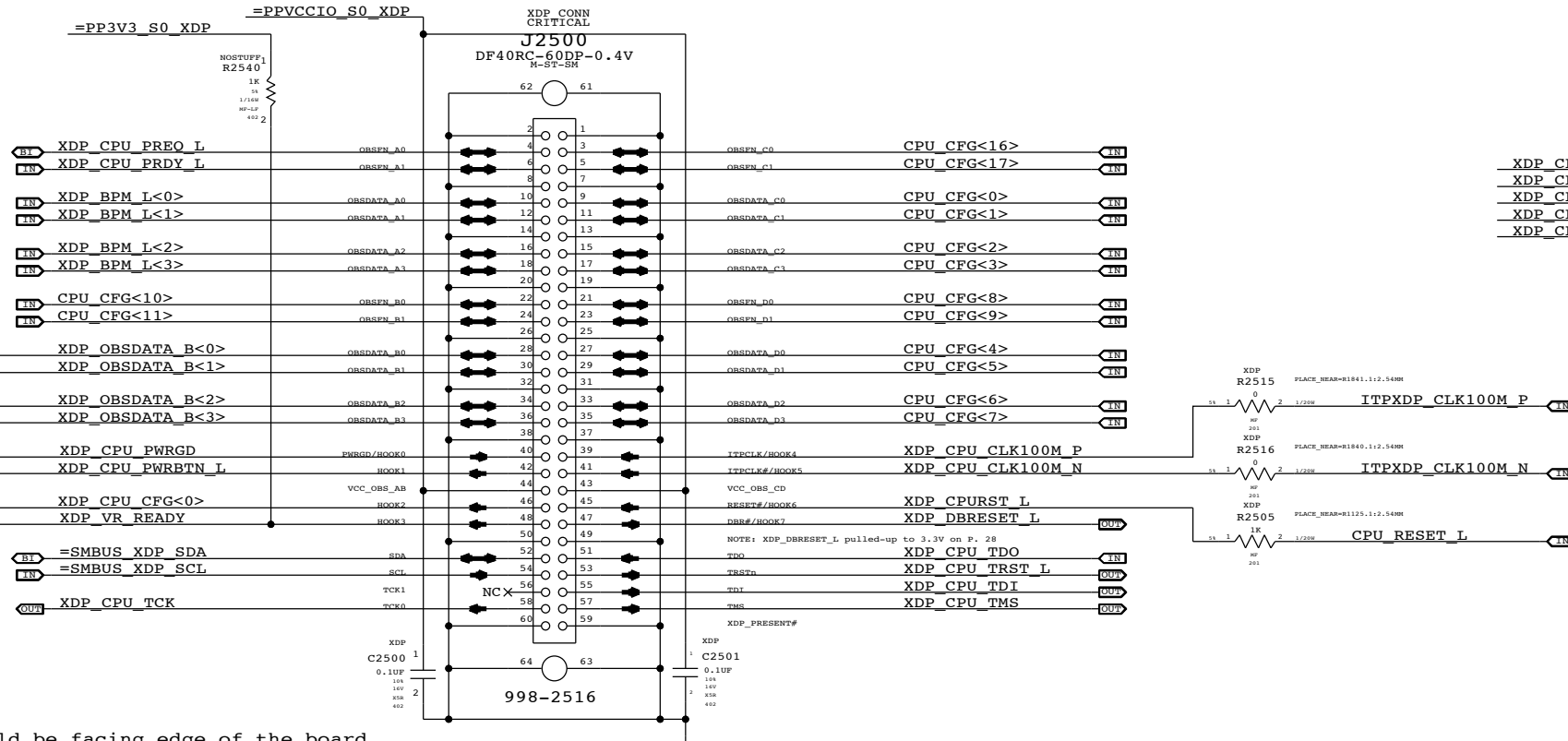
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### PROCESSOR MICRO2-XDP CONNECTOR

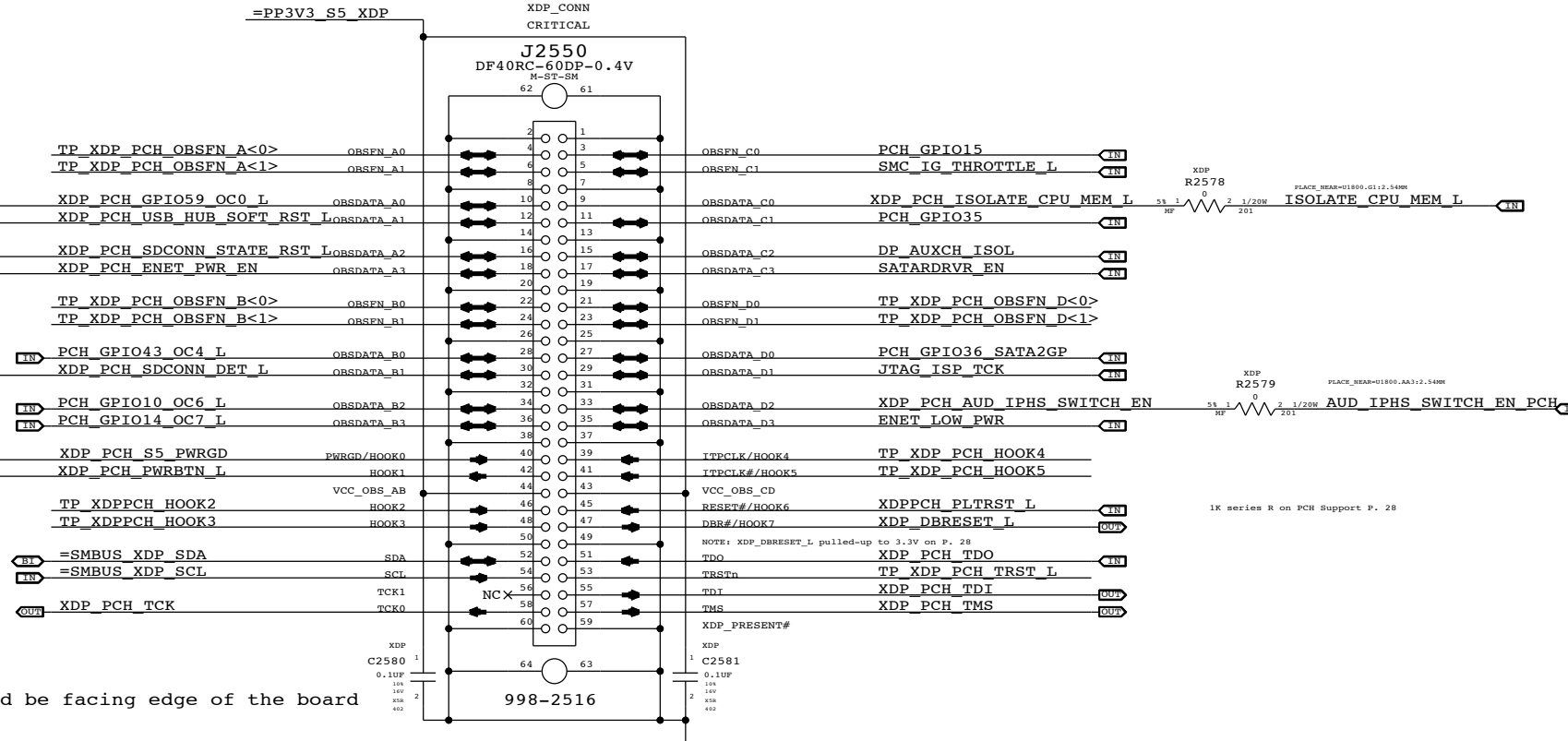
NOTE: This is not the standard XDP pinout  
Use with 920-0782 Adapter Flex to support chipset debug



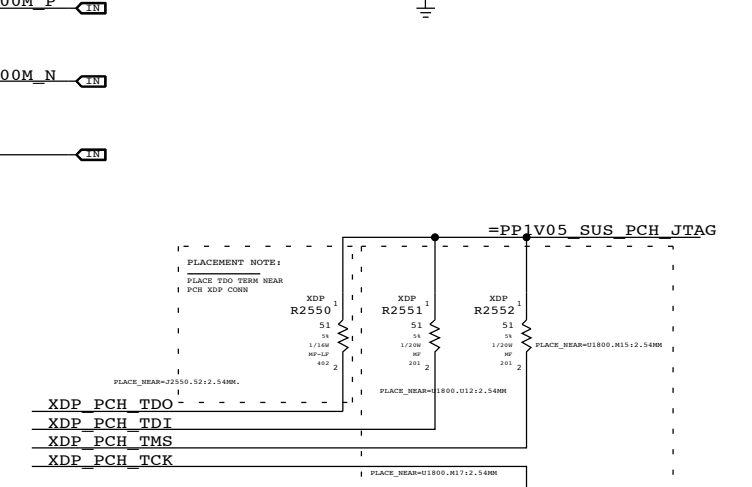
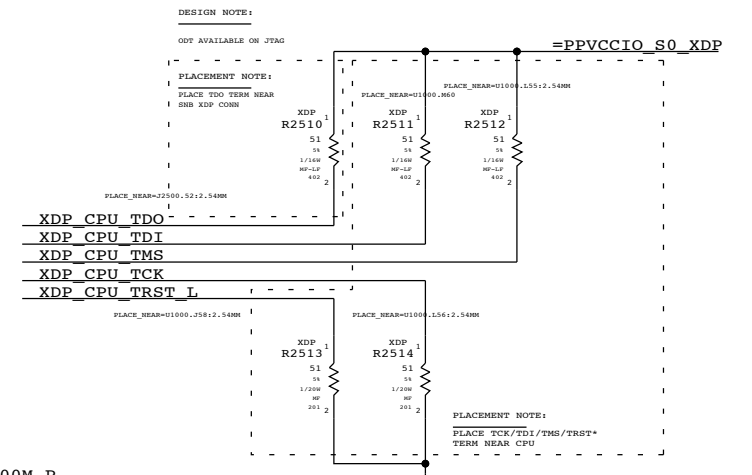
Even pins should be facing edge of the board

### PCH MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout  
Use with 920-0782 Adapter Flex to support chipset debug

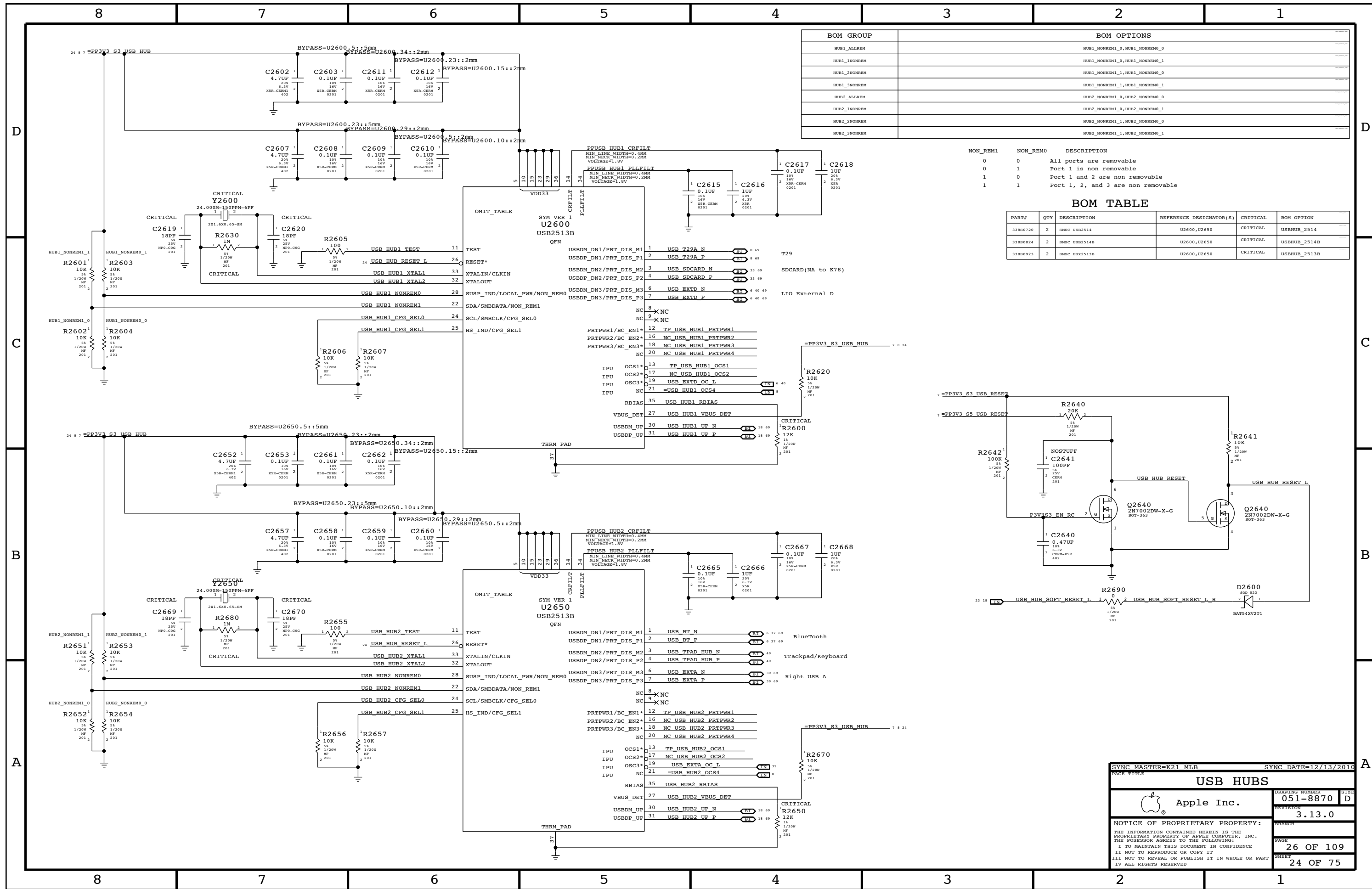


Even pins should be facing edge of the board



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
<b>CPU &amp; PCH XDP</b>			
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		PAGE	
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		SHEET	
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BOM GROUP		BOM OPTIONS	
HUB1_ALLREM		HUB1_NONREM0	HUB1_NONREM0_0
HUB1_1NONREM		HUB1_NONREM1_0	HUB1_NONREM1_1
HUB1_2NONREM		HUB1_NONREM1_1	HUB1_NONREM1_0
HUB1_3NONREM		HUB1_NONREM1_1	HUB1_NONREM1_1
HUB2_ALLREM		HUB2_NONREM0	HUB2_NONREM0_0
HUB2_1NONREM		HUB2_NONREM1_0	HUB2_NONREM1_1
HUB2_2NONREM		HUB2_NONREM1_1	HUB2_NONREM1_0
HUB2_3NONREM		HUB2_NONREM1_1	HUB2_NONREM1_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE					
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
33880824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
33880923	2	SMSC USB2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC MASTER=K21 MLB SYNC DATE=12/13/2010

**USB HUBS**

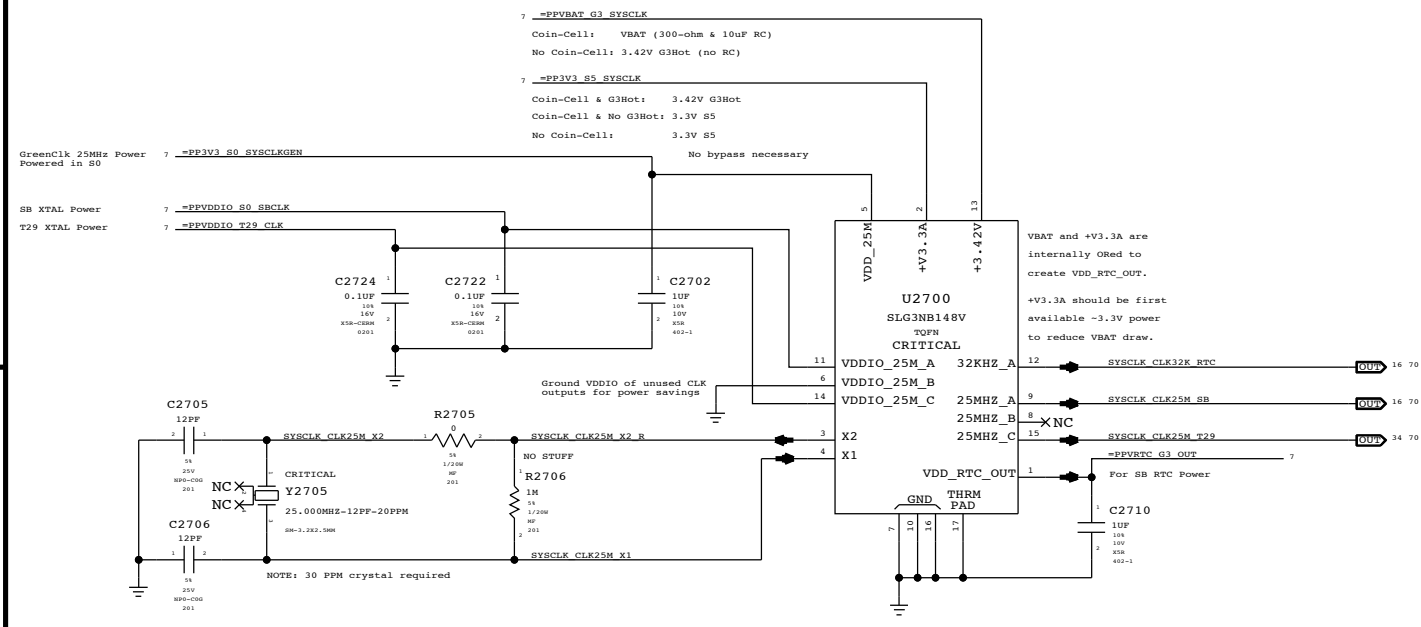
Apple Inc.

DRAWING NUMBER: 051-8870  
REVISION: 3.13.0

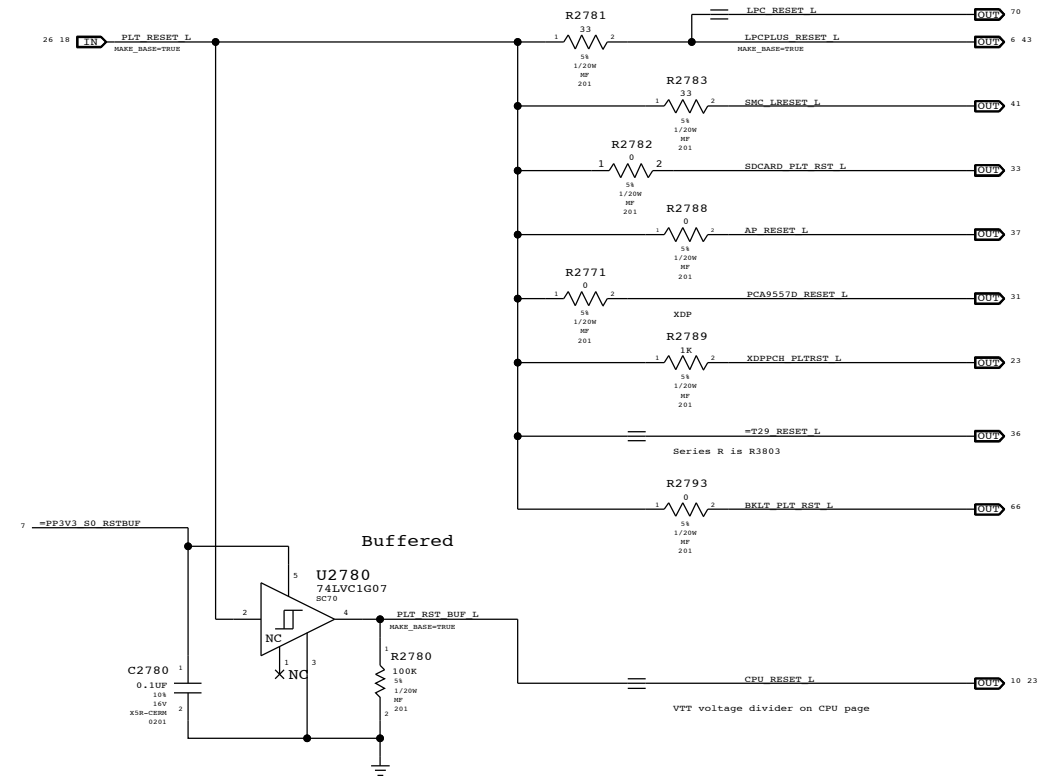
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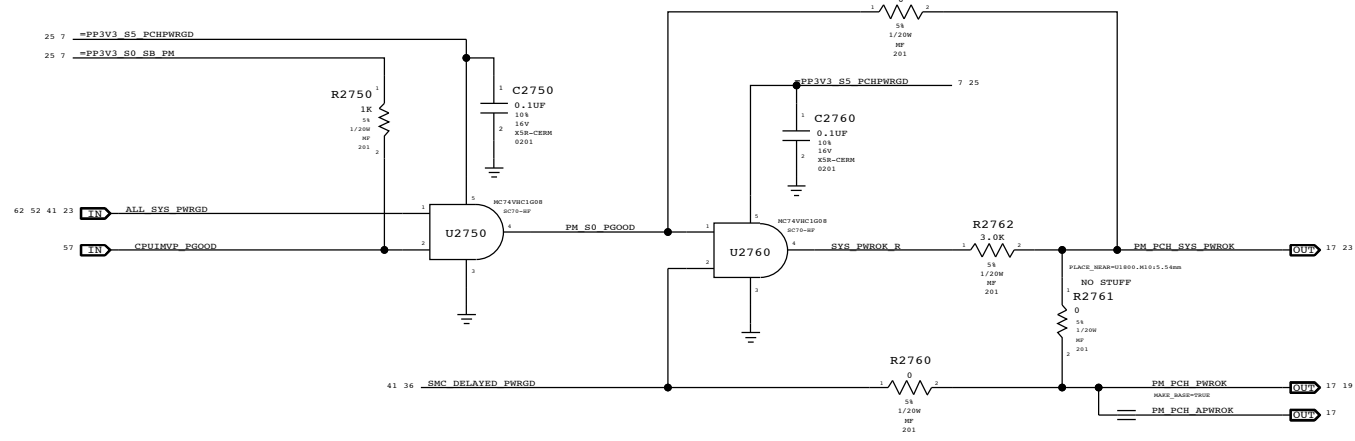
### System RTC Power Source & 32kHz / 25MHz Clock Generator



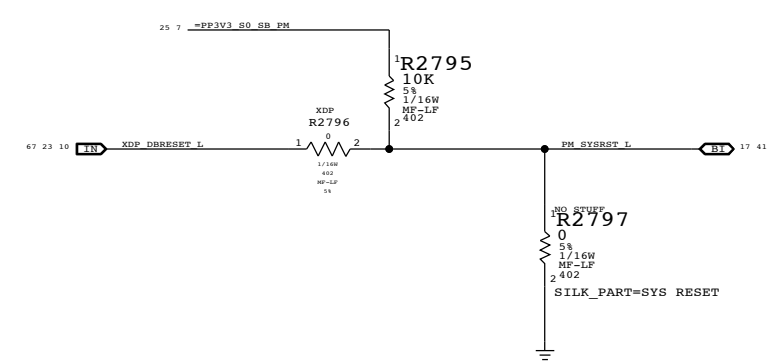
### Platform Reset Connections Unbuffered



### PCH S0 PWRGD

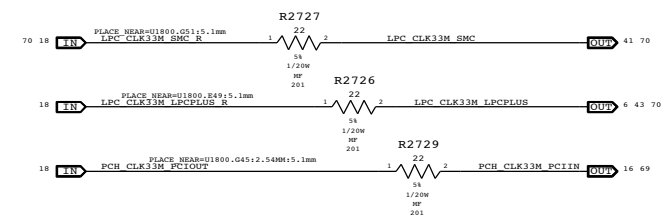
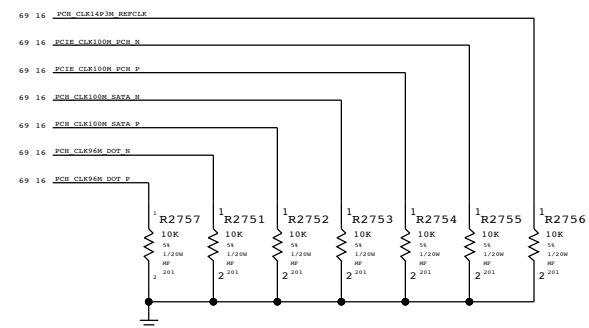


### PCH Reset Button



### CLOCK (CK505)

UNUSED clock terminations for PCIM MODE

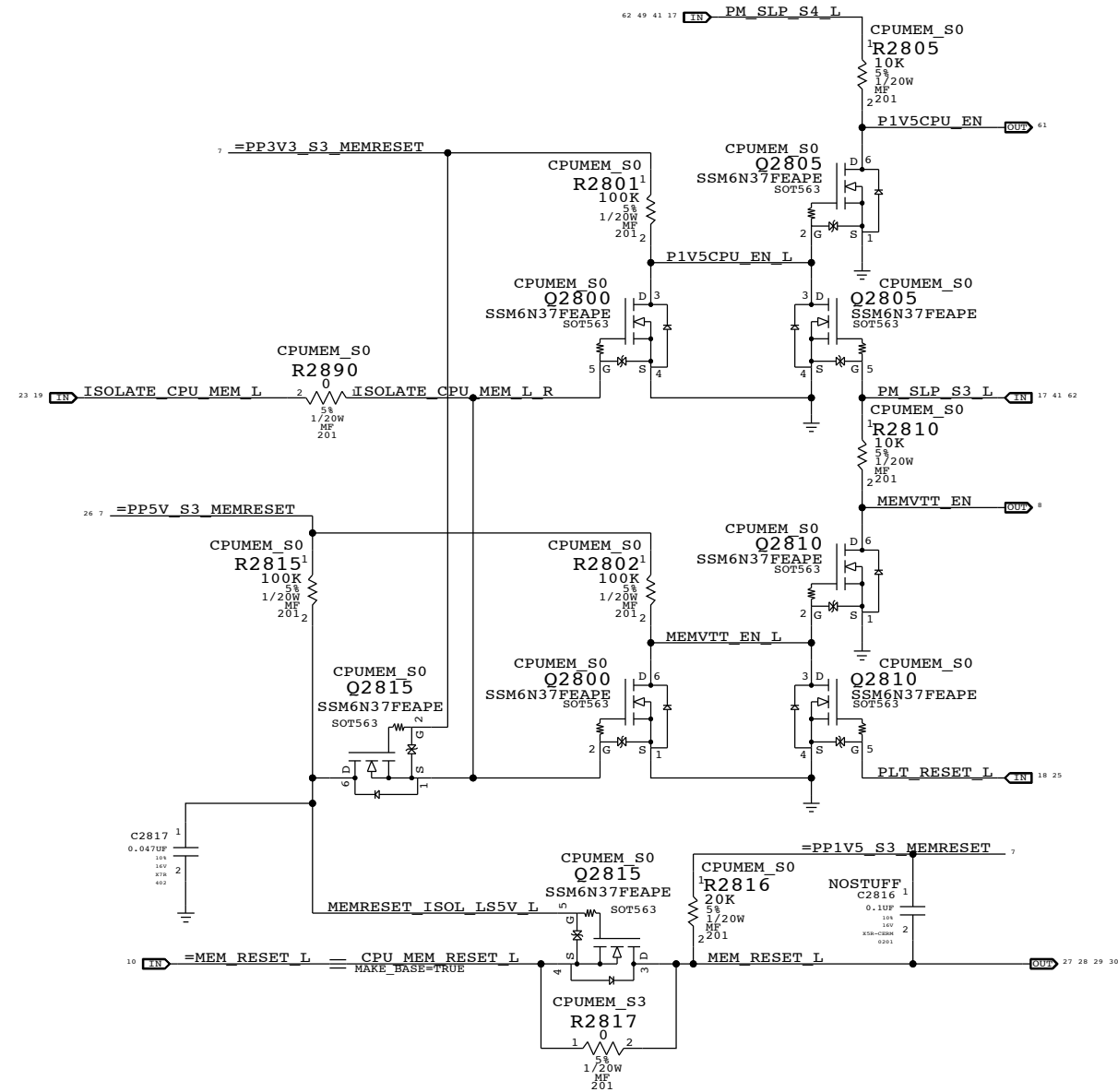


CLOCK (CK505) and Chipset Support		DRAWING NUMBER	051-8870	SIZE	D
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		BRANCH			
		PAGE	27 OF 109		
		SHEET	25 OF 75		

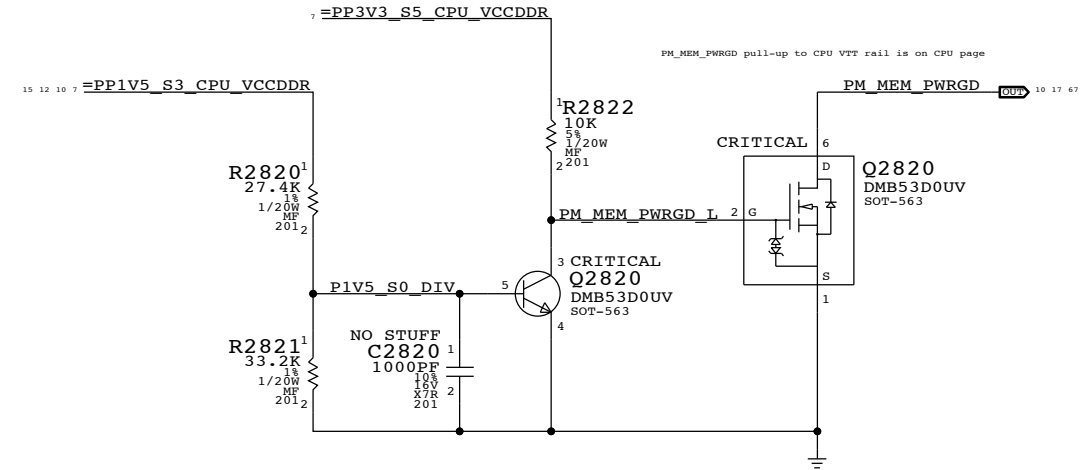
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.  
 WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
 WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

$P1V5CPU\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) * PM\_SLP\_S4\_L$   
 $MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) * PM\_SLP\_S3\_L$   
 $MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L$

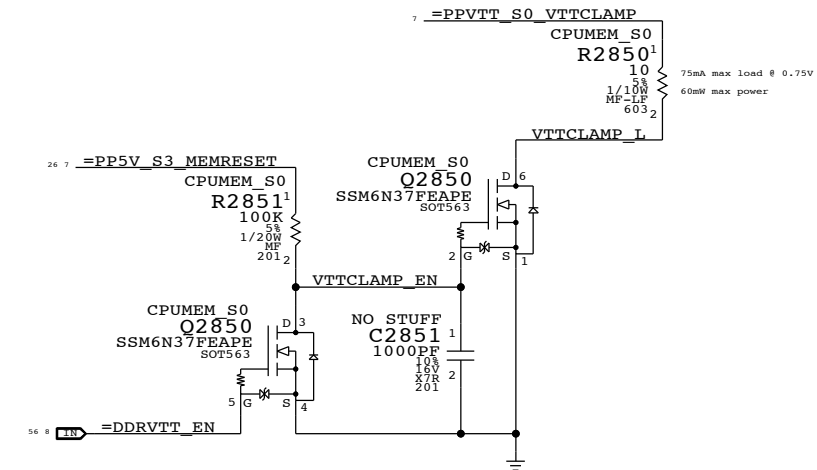


### 1V5 S0 "PGOOD" for CPU



### MEMVTT Clamp

Ensures CKE signals are held low in S3

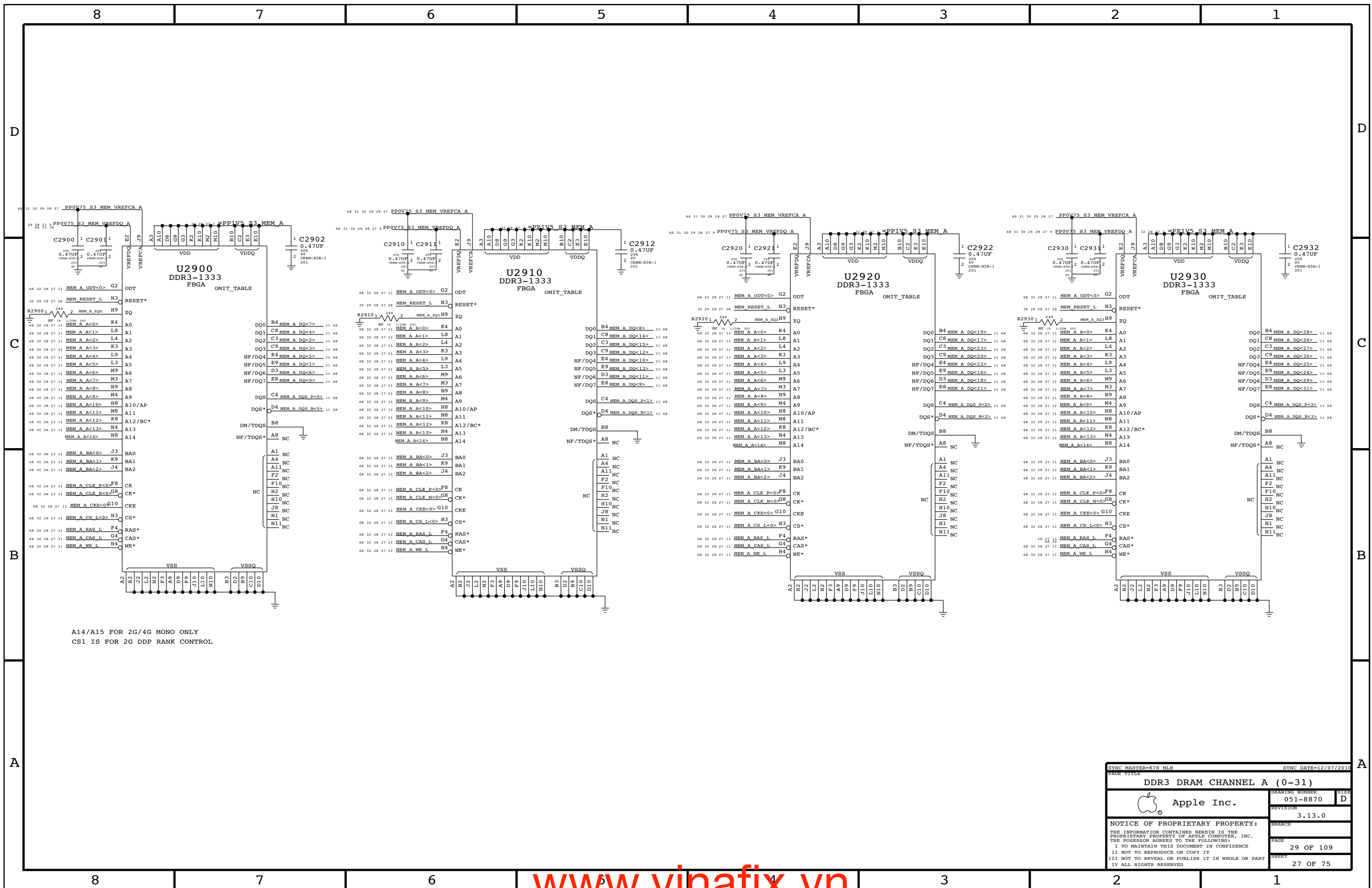


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPUMEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1		0	1
2	0	0	0	1	1		0	1
3	0	0	0	1	X		0	1
S3	4	0	0	1	X		0	1
to	5	0	1	1	0 (*)		1	1
6	0	1	1	1	1		1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

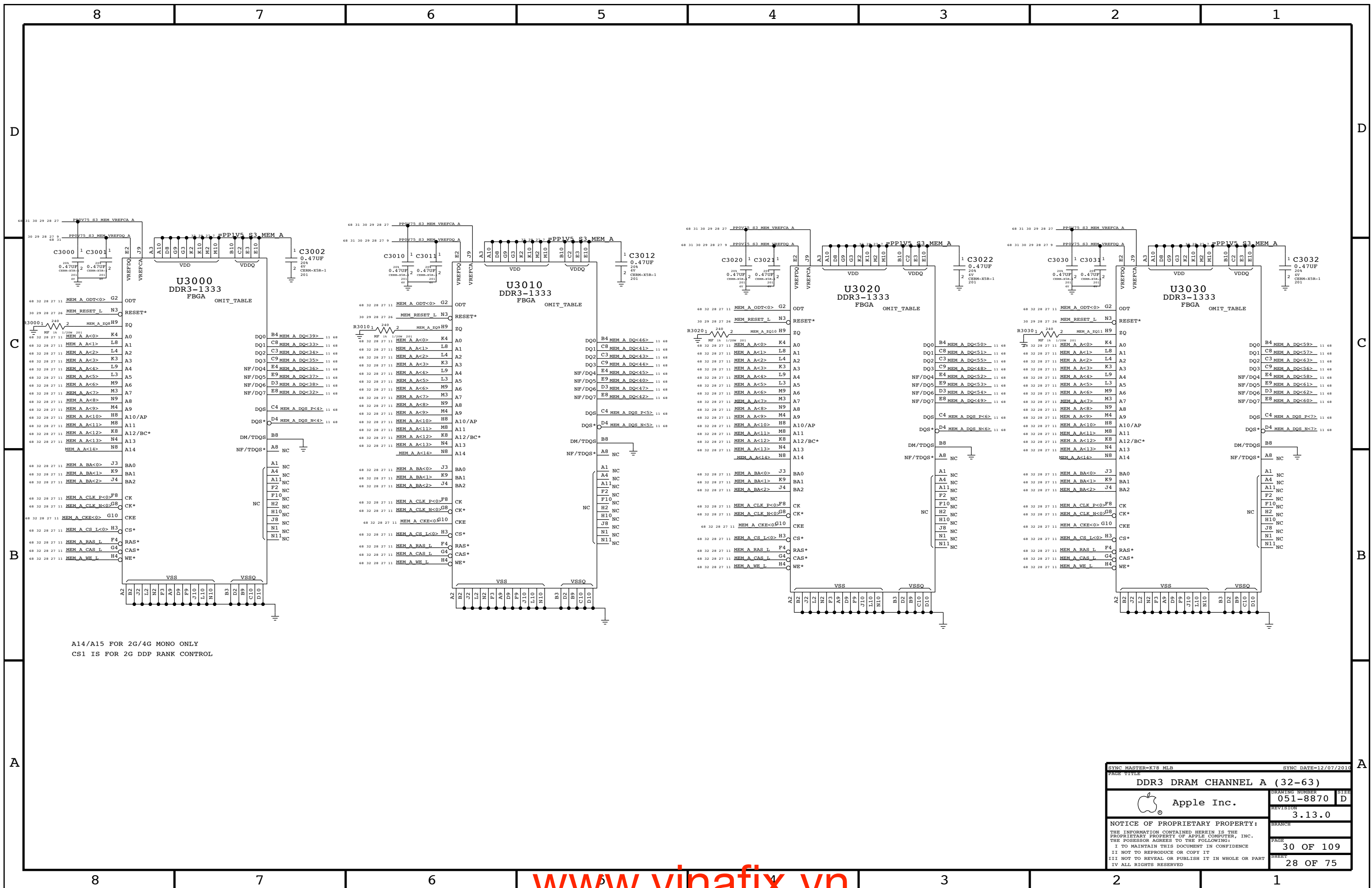
NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.

CPU Memory S3 Support		DRAWING NUMBER	051-8870	SIZE	D
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A14/A15 FOR 2G/4G MONO ONLY  
 CS1 IS FOR 2G DDP RANK CONTROL

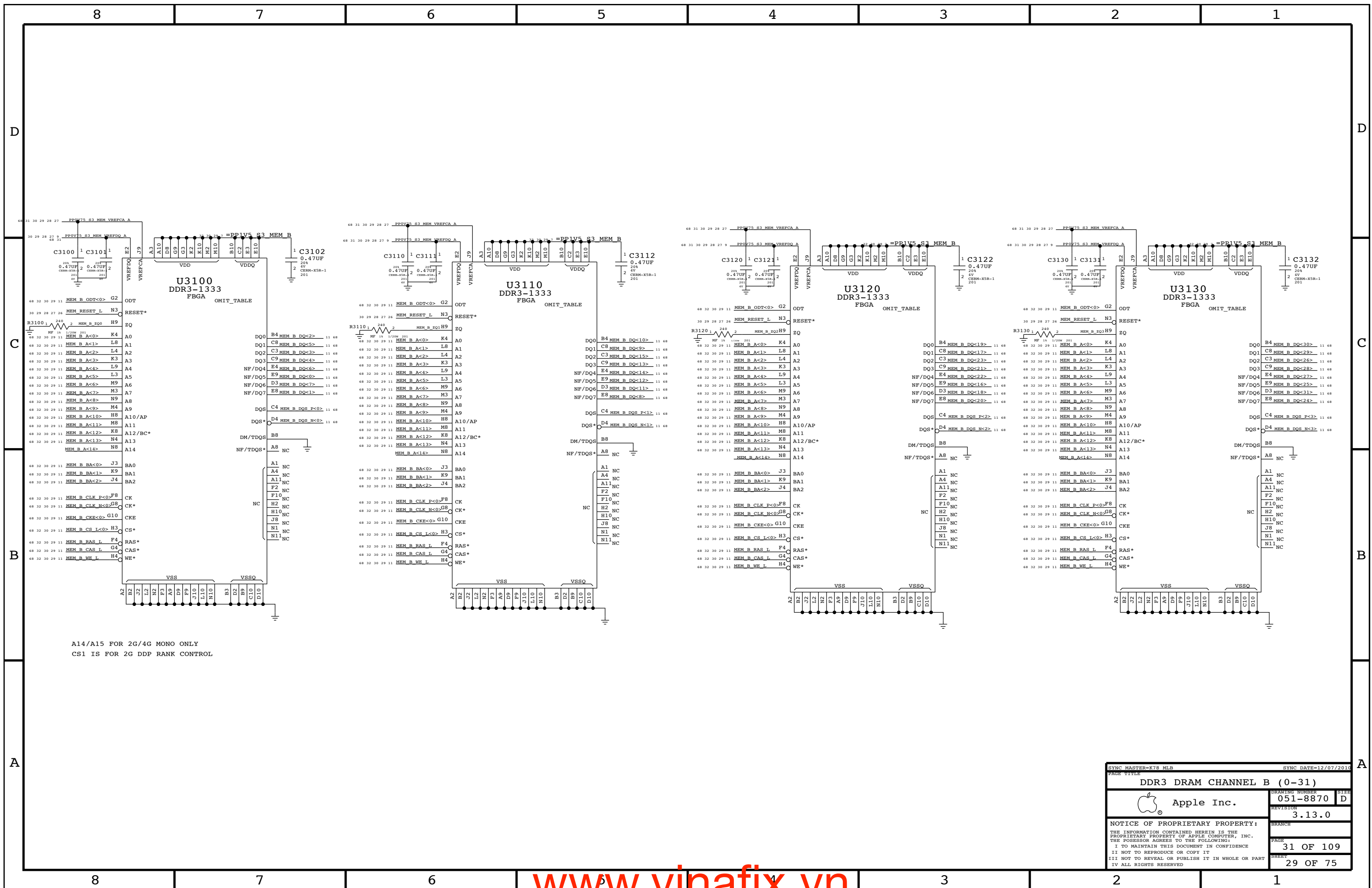
SYNC MASTER=K78 MLB		SYNC DATE=12/07/2010	
PAGE TITLE			
DDR3 DRAM CHANNEL A (0-31)			
Apple Inc.		DRAWING NUMBER	051-8870
		REVISION	3.13.0
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		PAGE	29 OF 109
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A14/A15 FOR 2G/4G MONO ONLY  
 CS1 IS FOR 2G DDP RANK CONTROL

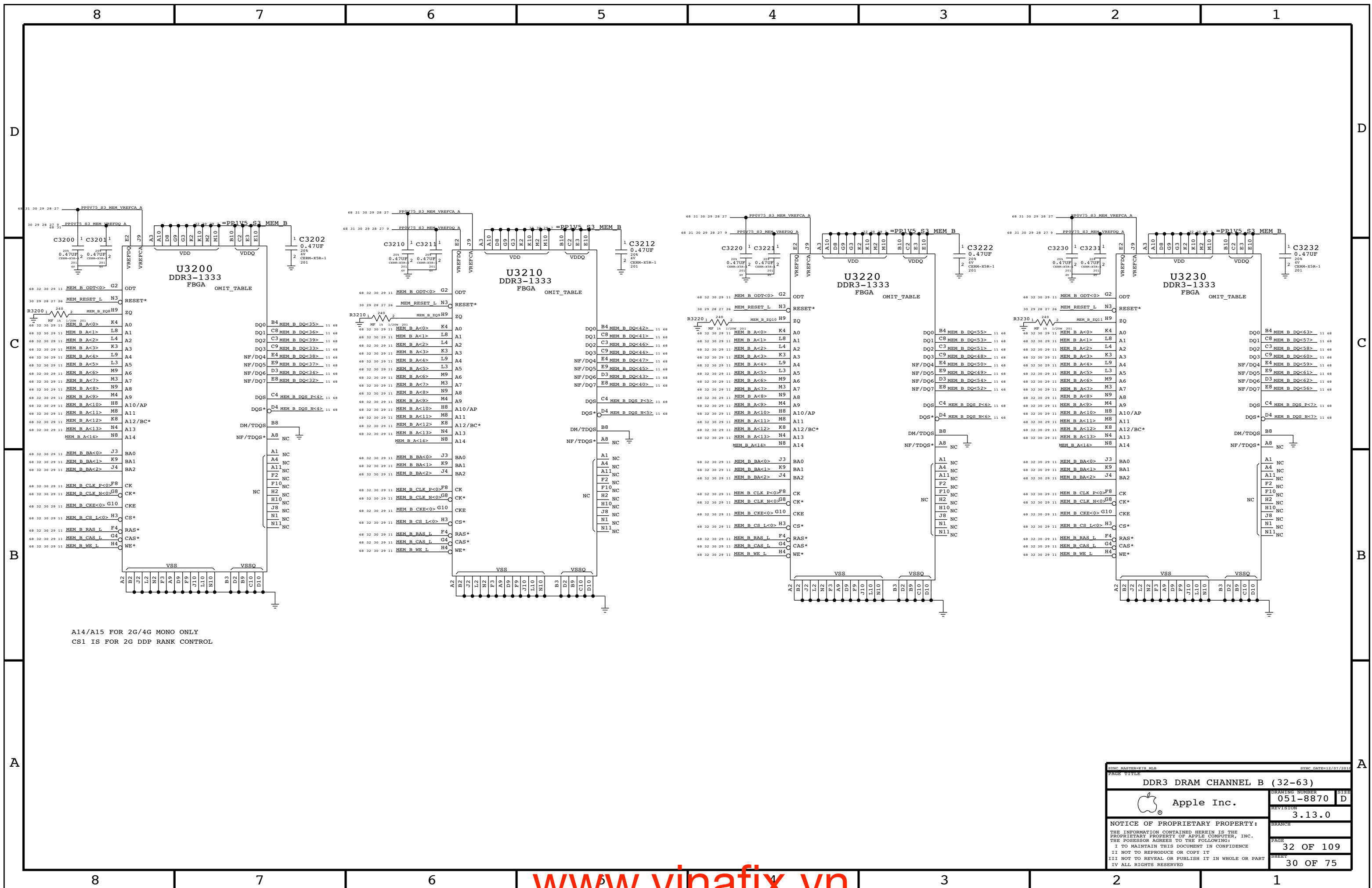
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Apple Inc.		DRAWING NUMBER	051-8870
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SHEET		28 OF 75	





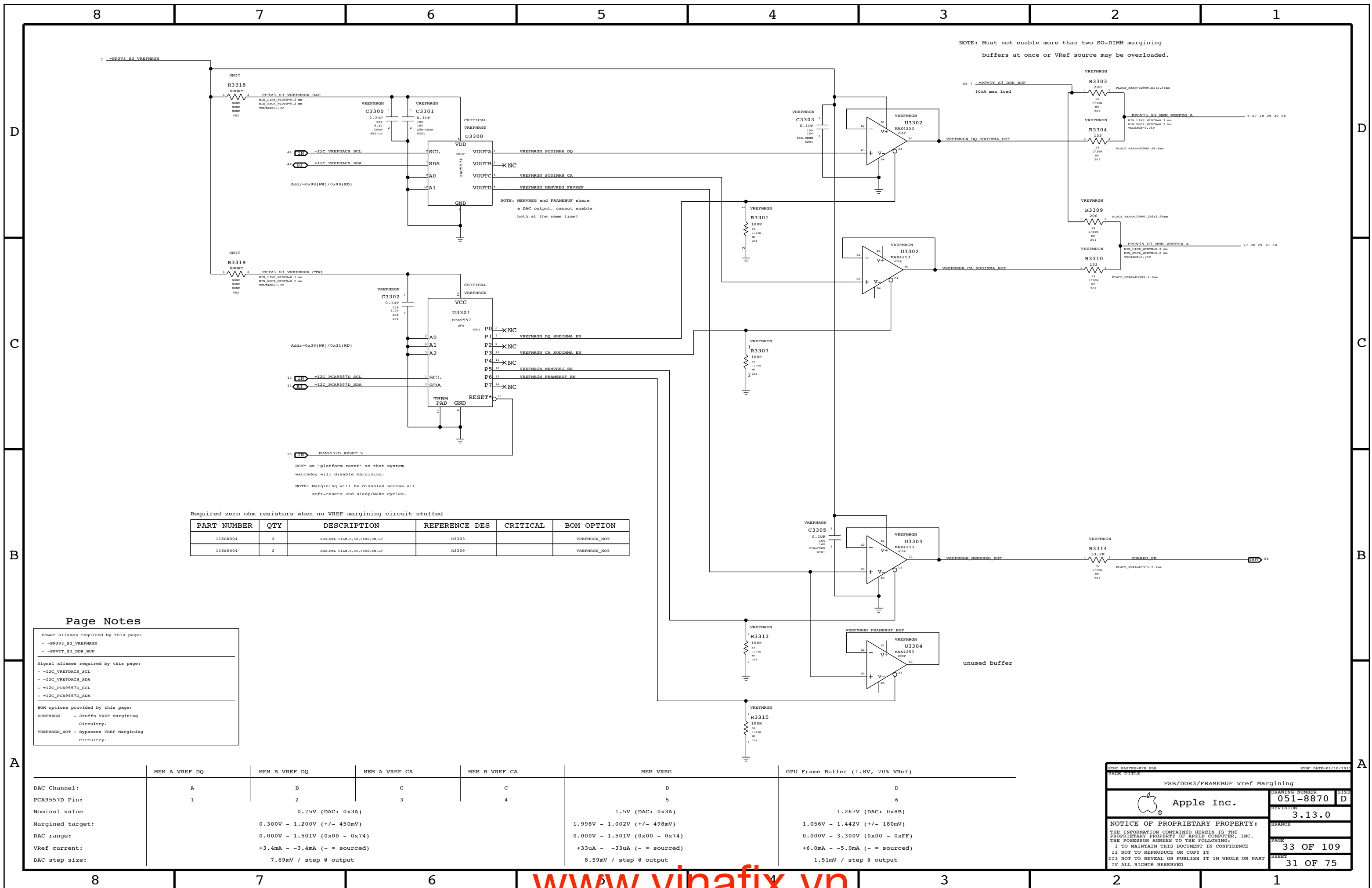
A14/A15 FOR 2G/4G MONO ONLY  
 CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K78 MLB		SYNC DATE=12/07/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (0-31)			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8870	D
		REVISION	
		3.13.0	
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		PAGE	31 OF 109
		SHEET	29 OF 75



A14/A15 FOR 2G/4G MONO ONLY  
 CS1 IS FOR 2G DDP RANK CONTROL

SYMC MASTER#123 MEM		SYMC DATE#12/07/2010	
PAGE TITLE			
<b>DDR3 DRAM CHANNEL B (32-63)</b>			
 Apple Inc.	DRAWING NUMBER	051-8870	SIZE
	REVISION	3.13.0	
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Required zero ohm resistors when no VREF margining circuitry stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680004	2	RES,HTL FILM,0.5%,0402,SM,LF	R3303		VREFMGRN_NOT
11680004	2	RES,HTL FILM,0.5%,0402,SM,LF	R3309		VREFMGRN_NOT

Page Notes

Power aliases required by this page:  
 - =PP3V3\_S3\_VREFMGRN  
 - =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
 - =I2C\_VREFDACS\_SCL  
 - =I2C\_VREFDACS\_SDA  
 - =I2C\_PCA9557D\_SCL  
 - =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
 VREFMGRN - Stuffs VREF Margining Circuitry.  
 VREFMGRN\_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNCH MASTER/SLAVE MGR      SYNCH DATE/REV/10/2015

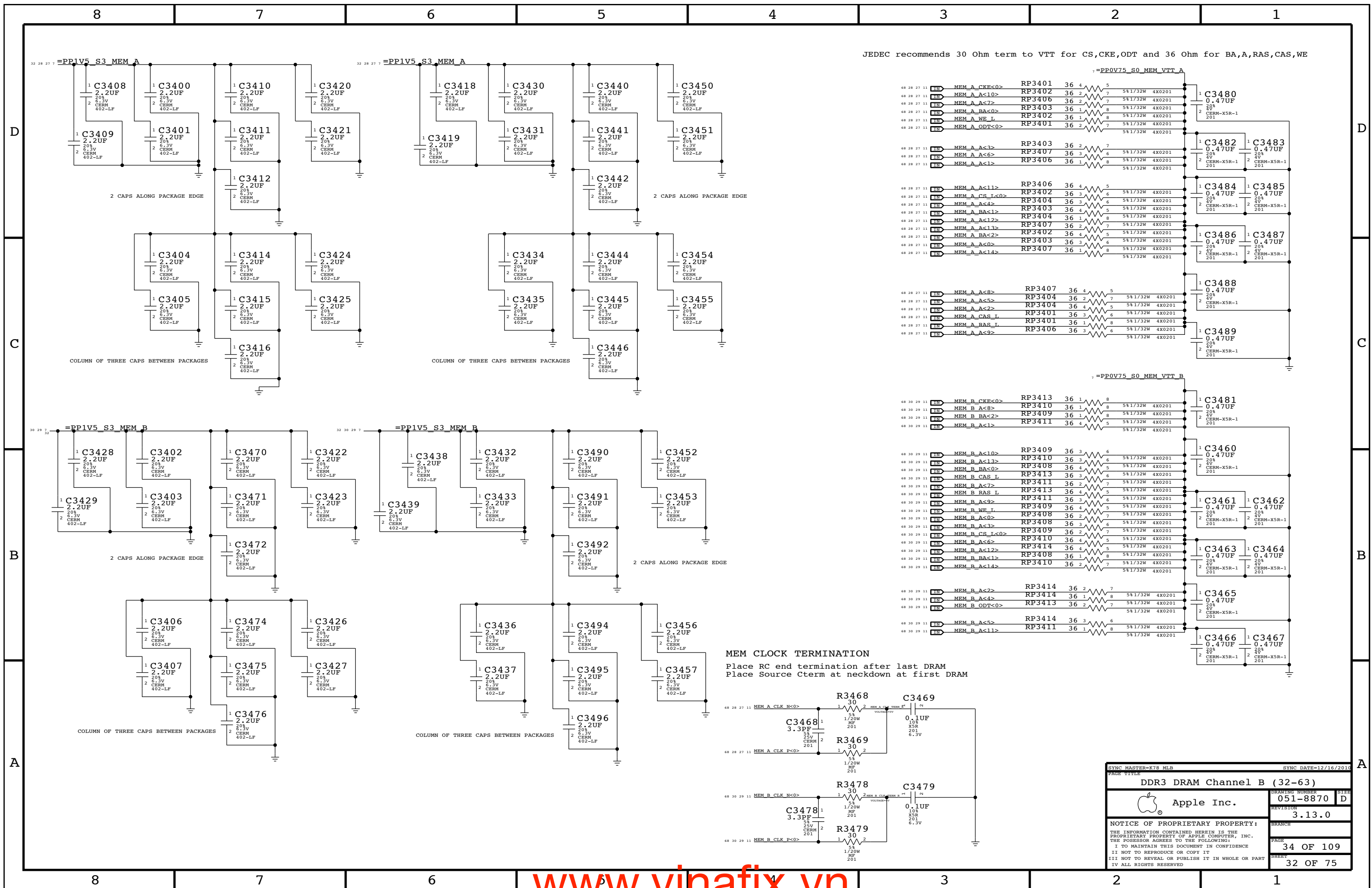
PAGE TITLE: FSB/DDR3/FRAMBUF Vref Margining

Apple Inc.      DRAWING NUMBER: 051-8870      SIZE: D

REVISION: 3.13.0

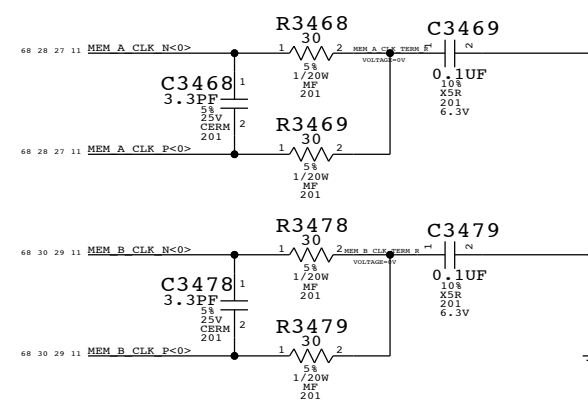
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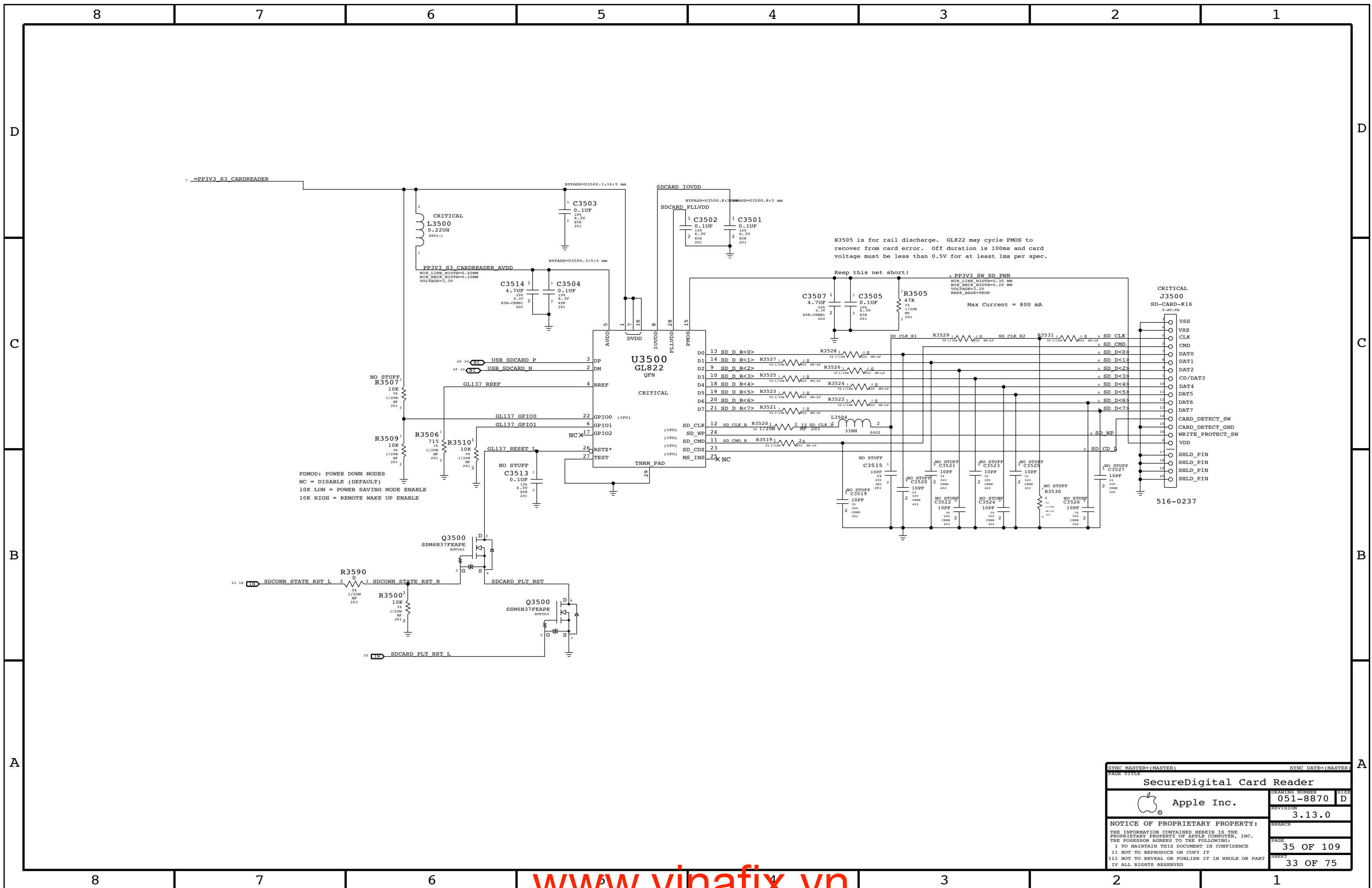


JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

**MEM CLOCK TERMINATION**  
 Place RC end termination after last DRAM  
 Place Source Cterm at neckdown at first DRAM



SYNC MASTER=K78 MLB		SYNC DATE=12/16/2011	
PAGE TITLE			
DDR3 DRAM Channel B (32-63)			SIZE
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REVISION			3.13.0
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PDMOD: POWER DOWN MODES  
 NC = DISABLE (DEFAULT)  
 10K LOW = POWER SAVING MODE ENABLE  
 10K HIGH = REMOTE WAKE UP ENABLE

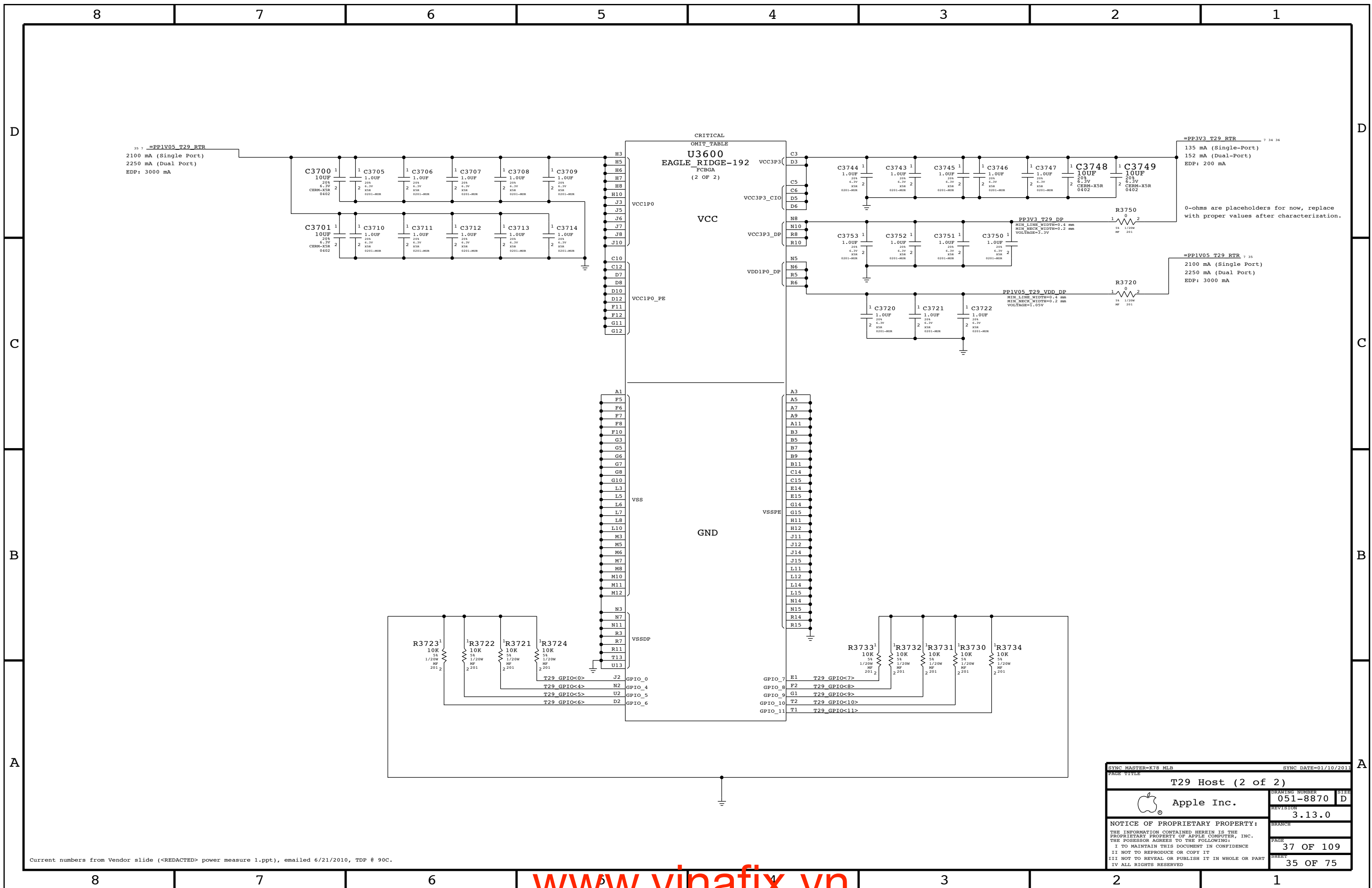
R3505 is for rail discharge. GL822 may cycle PMOS to recover from card error. Off duration is 100ms and card voltage must be less than 0.5V for at least 1ms per spec.

Keep this net short!  
 Max Current = 800 mA

SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
PAGE TITLE			
<b>SecureDigital Card Reader</b>			
		DRAWING NUMBER	051-8870
		REVISION	3.13.0
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		SHEET	33 OF 75







35 7 =PP1V05 T29 RTR  
 2100 mA (Single Port)  
 2250 mA (Dual Port)  
 EDP: 3000 mA

=PP3V3 T29 RTR 7 34 36  
 135 mA (Single-Port)  
 152 mA (Dual-Port)  
 EDP: 200 mA

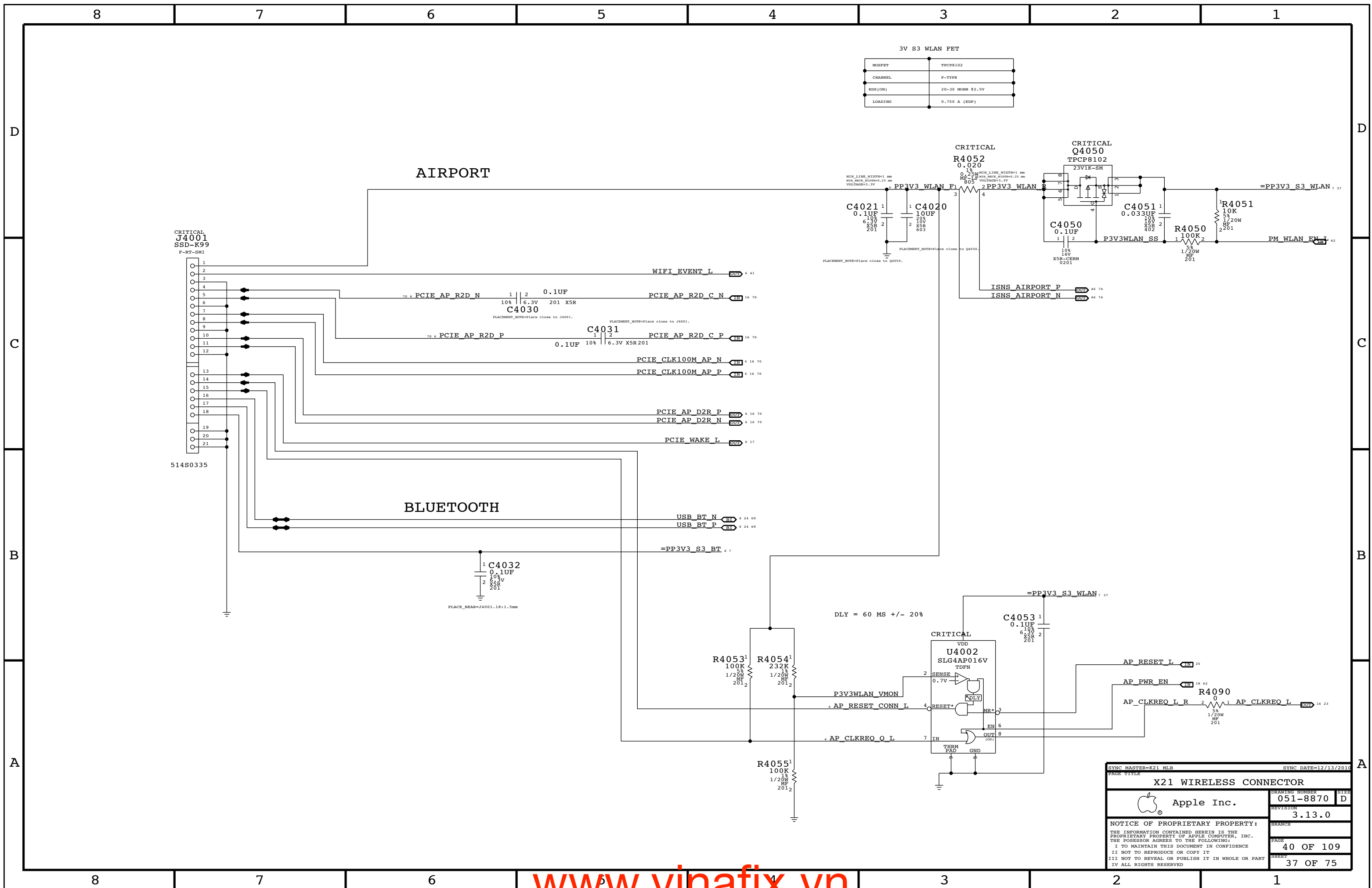
0-ohms are placeholders for now, replace with proper values after characterization.

=PP1V05 T29 RTR 7 35  
 2100 mA (Single Port)  
 2250 mA (Dual Port)  
 EDP: 3000 mA

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

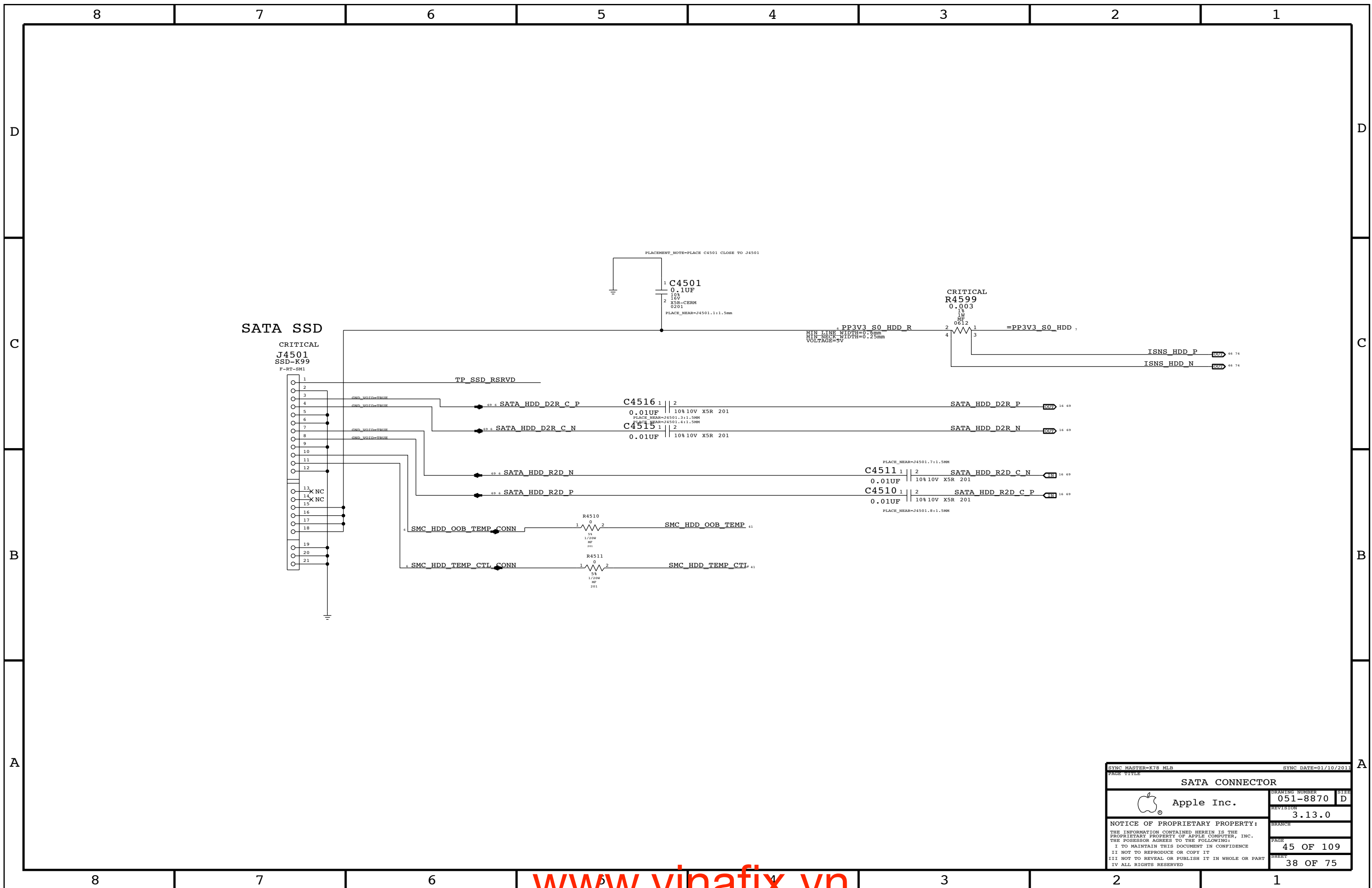
SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
PAGE TITLE T29 Host (2 of 2)			
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		35 OF 75	






3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	F-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (RDP)

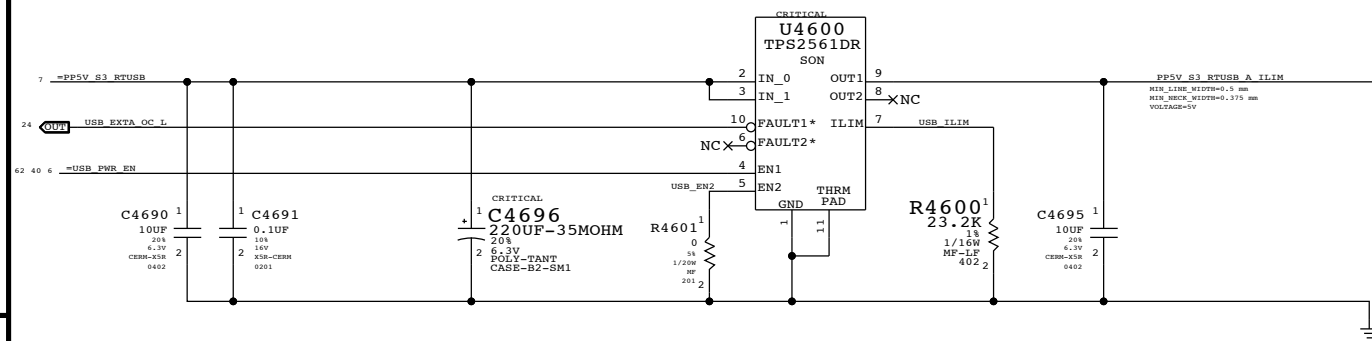
SYNC MASTER=K21.MLB		SYNC DATE=12/13/2010	
<b>X21 WIRELESS CONNECTOR</b>			
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		SHEET	37 OF 75



SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
PAGE TITLE			
<b>SATA CONNECTOR</b>			
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		REVISION	3.13.0
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		SHEET	38 OF 75

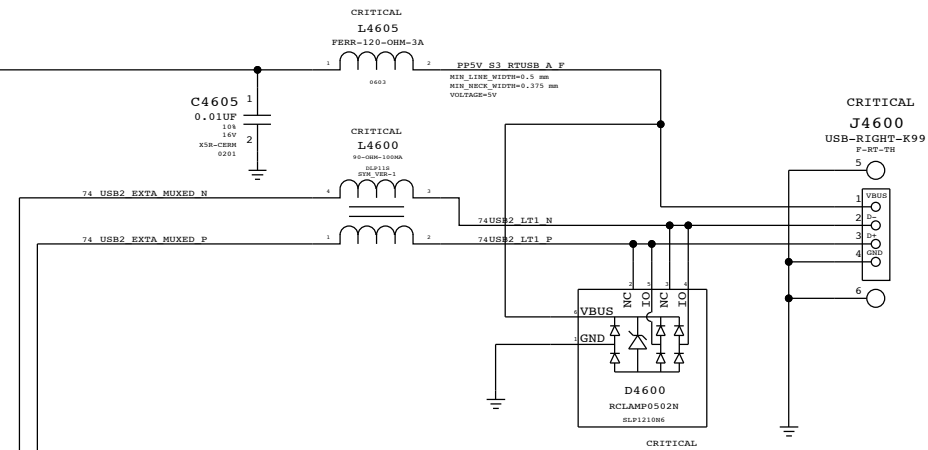


### USB Port Power Switch



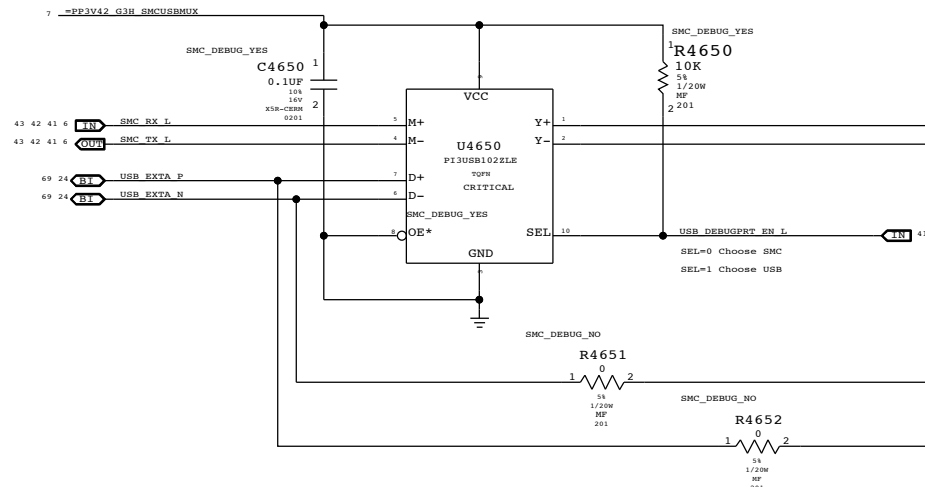
Current limit (R4600): 2.3A max

### Right USB Port A

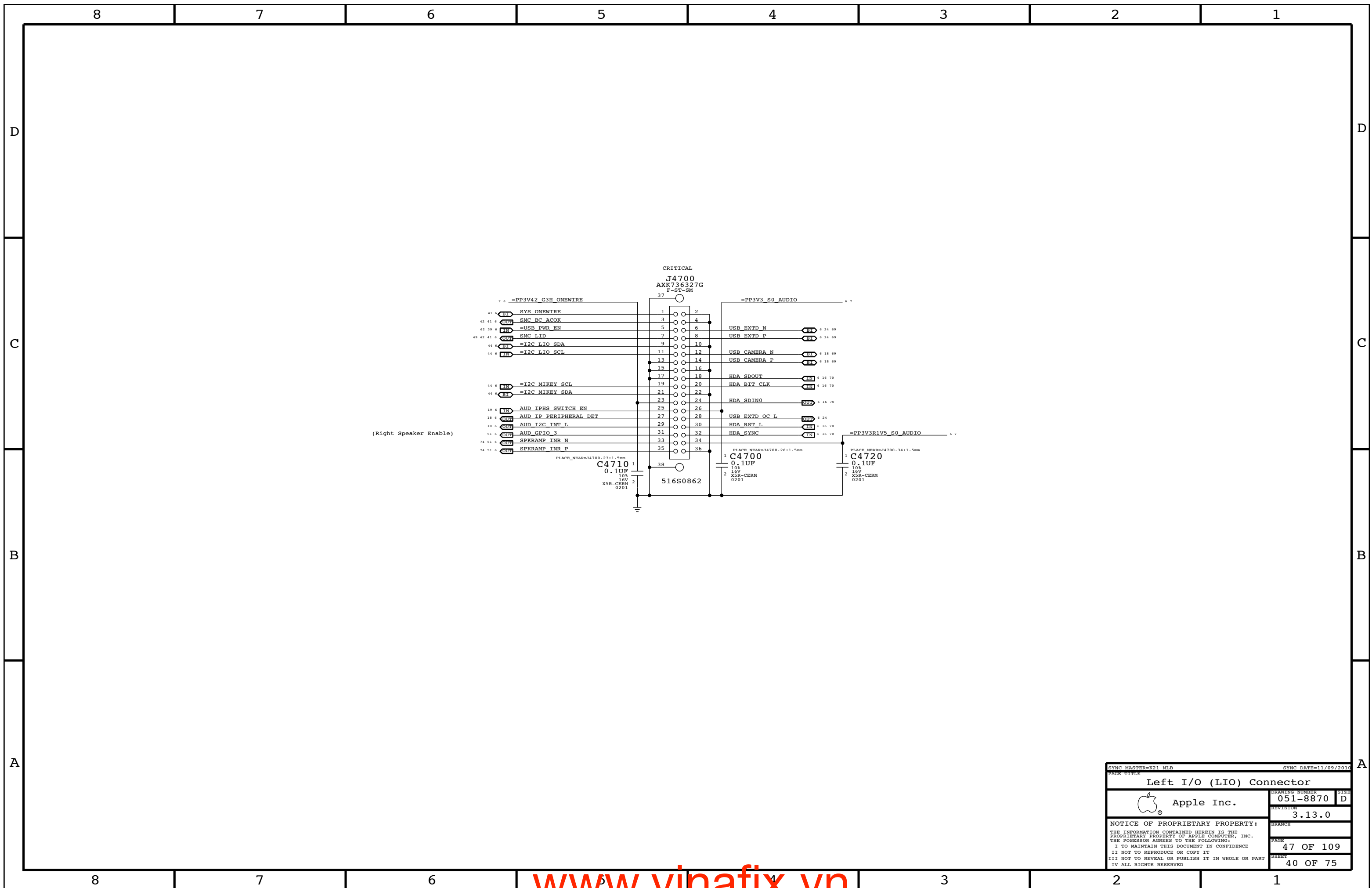


We can add protection to 5V if we want, but leaving NC for now  
Place L4605 at connector pin

### USB/SMC Debug Mux

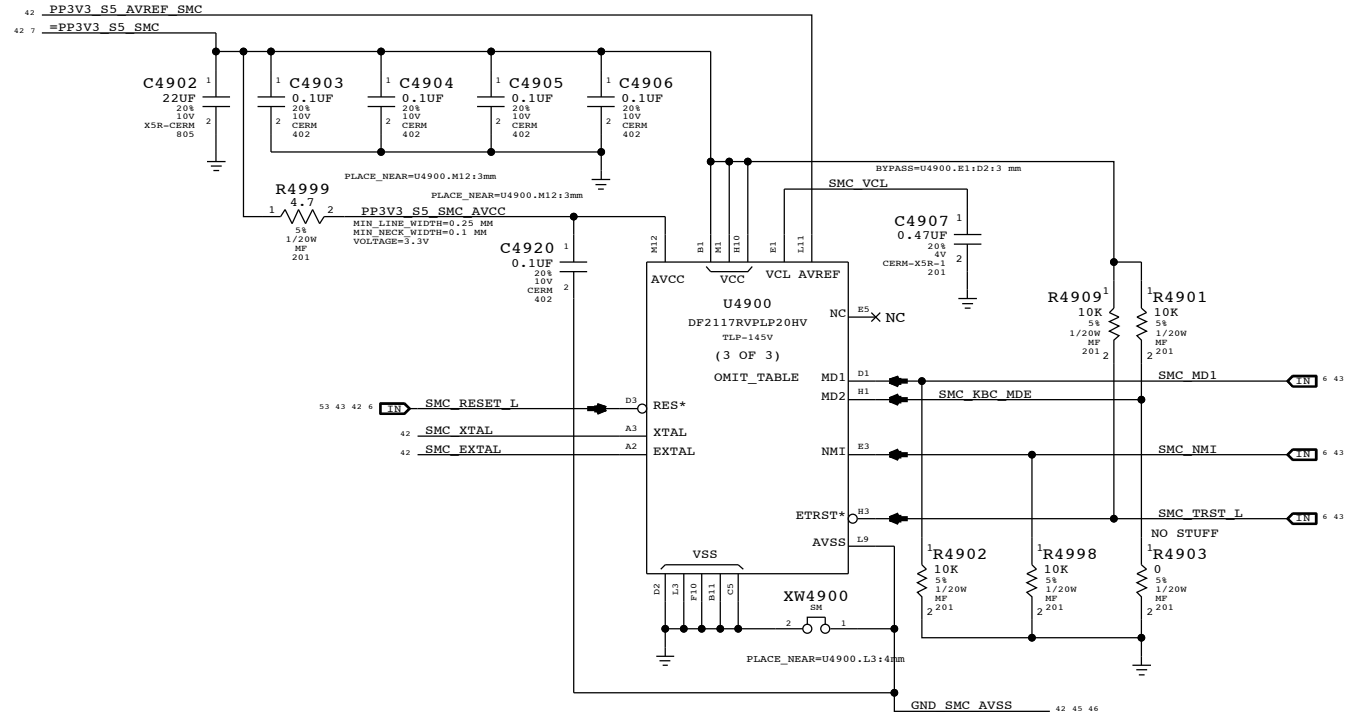
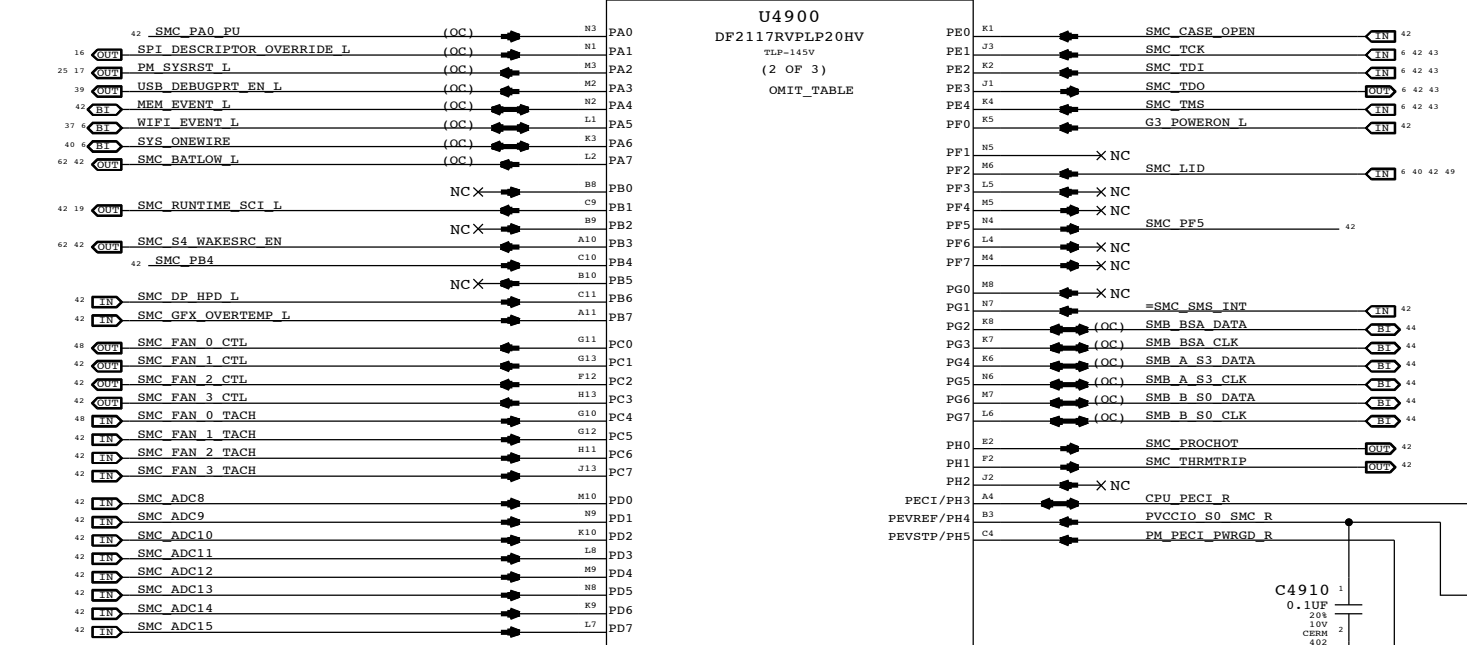
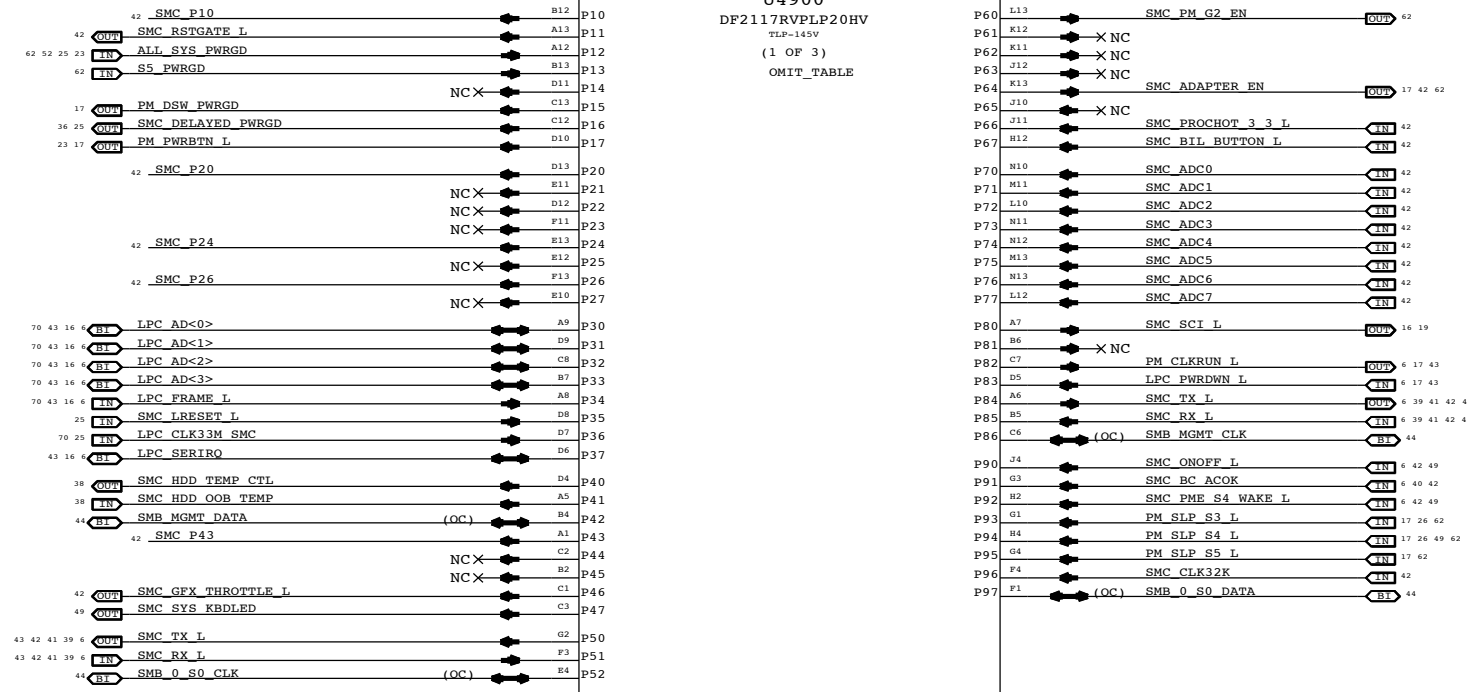


SYMC MASTER#11 MBR		SYMC DATE#12/15/2016	
External USB Connectors			
Apple Inc.	DRAWING NUMBER	051-8870	SIZE D
	REVISION	3.13.0	
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		SHEET	39 OF 75

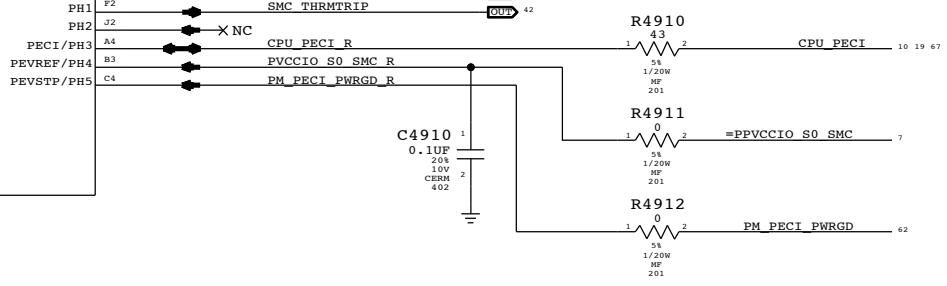


SYNC MASTER=K21 MLB		SYNC DATE=11/09/2010	
PAGE TITLE <b>Left I/O (LIO) Connector</b>			
DRAWING NUMBER <b>051-8870</b>		SIZE <b>D</b>	
REVISION <b>3.13.0</b>		BRANCH	
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NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

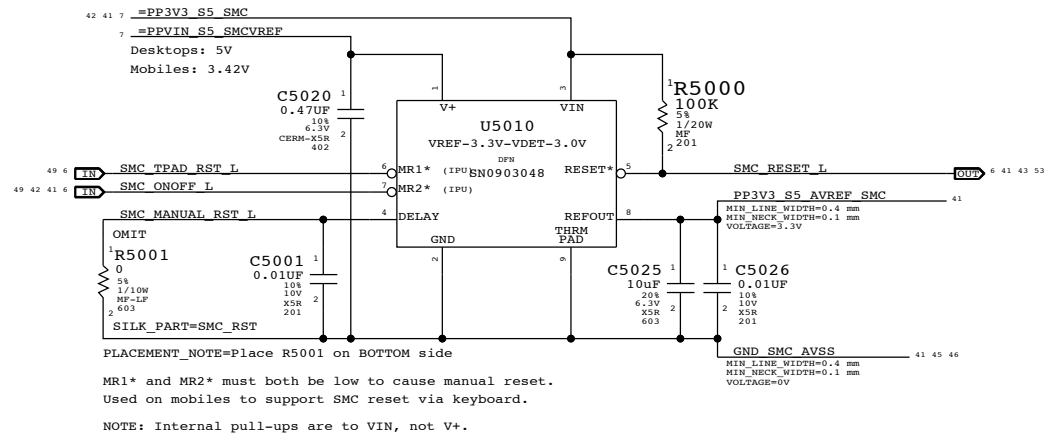


NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

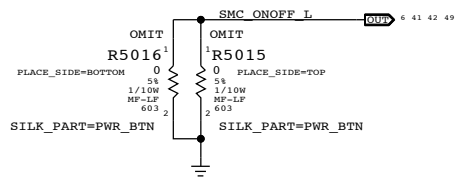


SYNC MASTER=K78_MLB		SYNC DATE=01/10/2011	
<b>SMC</b>			
Apple Inc.		DRAWING NUMBER	SIZE
051-8870		051-8870	D
REVISION		3.13.0	
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PAGE		49 OF 109	
SHEET		41 OF 75	

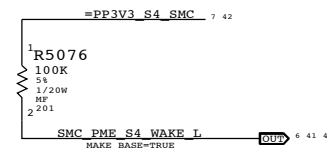
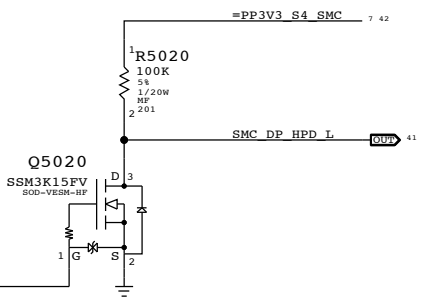
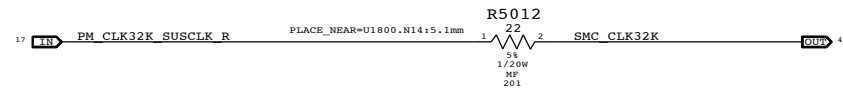
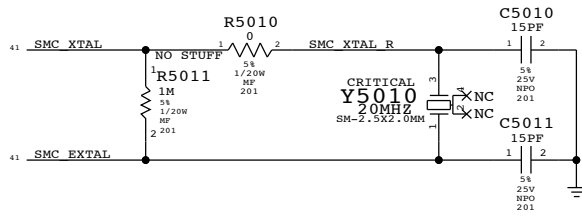
SMC Reset "Button", Supervisor & AVREF Supply



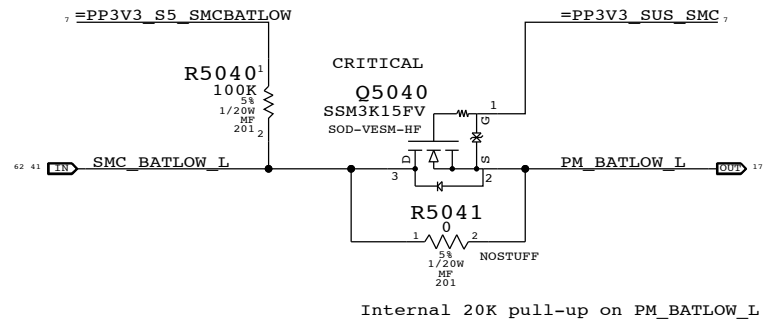
Debug Power "Buttons"



SMC Crystal Circuit



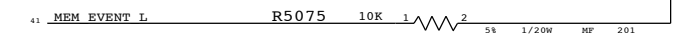
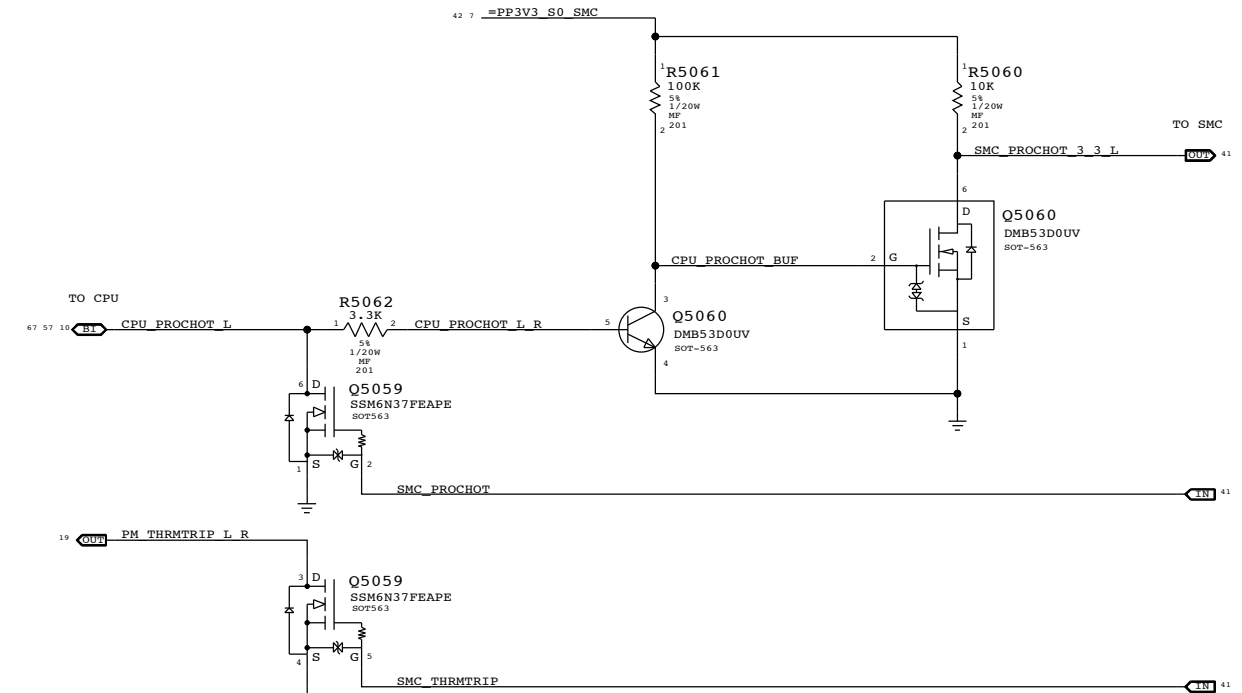
BATLOW# Isolation



Below connections are different from K91

- SMC\_PA0\_FU == HISIDE\_ISENSE\_OC
- SMC\_FAN\_1\_CTL == NC\_SMC\_FAN\_1\_CTL
- SMC\_FAN\_1\_TACH == NC\_SMC\_FAN\_1\_TACH
- SMC\_ADC14 == SMC\_HS\_COMPUTING\_ISENSE
- SMC\_GFX\_THROTTLE\_L == TP\_SMC\_GFX\_THROTTLE\_L
- SMC\_GFX\_OVERTEMP\_L == R5095

PROCHOT Level Shifting to 3V3



- SMC\_ONOFF\_L == R5070
- G3\_POWERON\_L == R5072
- SMC\_LID == R5071
- SMC\_TX\_L == R5073
- SMC\_RX\_L == R5074
- SMC\_TMS == R5077
- SMC\_TDO == R5078
- SMC\_TDI == R5079
- SMC\_TCK == R5080
- SMC\_BIL\_BUTTON\_L == R5081
- SMC\_BC\_ACOK == R5087
- SMS\_INT\_L == R5093
- SMC\_PA0\_PU == R5091
- SMC\_RUNTIME\_SCT\_L == R5094
- SMC\_ADAPTER\_EN == R5085
- SMC\_CASE\_OPEN == R5086
- SMC\_PB4 == R5088
- SMC\_S4\_WAKESRC\_EN == R5090

SYNC MASTER=K78.MLB SYNC DATE=01/10/2011

SMC Support

Apple Inc.

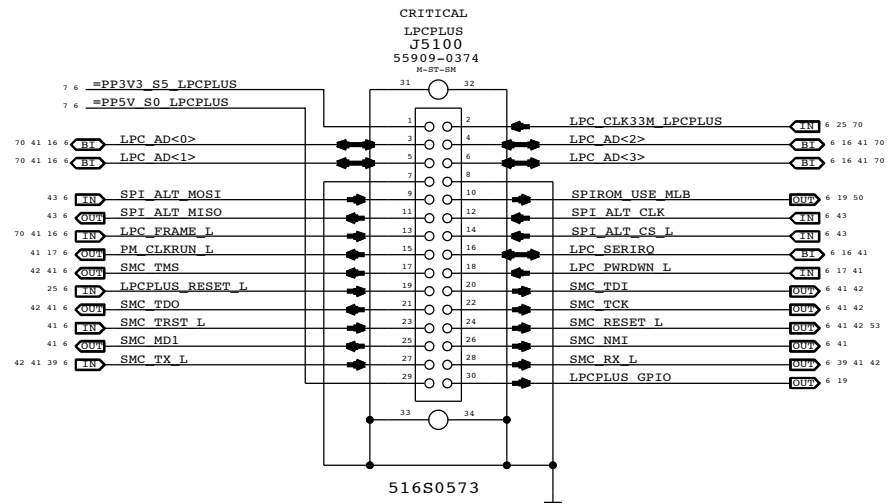
DRAWING NUMBER: 051-8870  
 REVISION: 3.13.0  
 PAGE: 50 OF 109  
 SHEET: 42 OF 75

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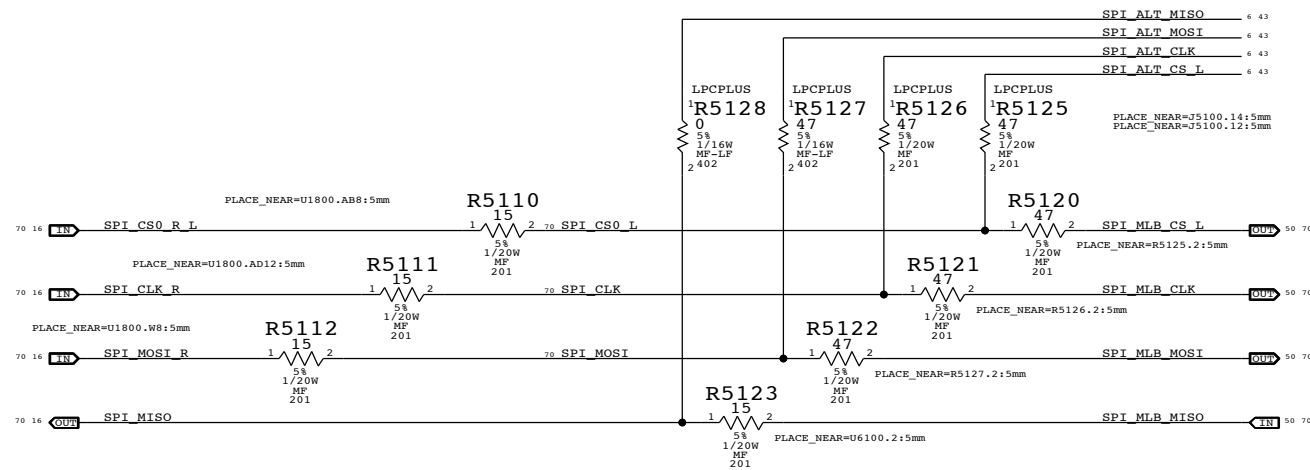
### LPC+SPI Connector



C

C

### SPI Bus Series Termination



B

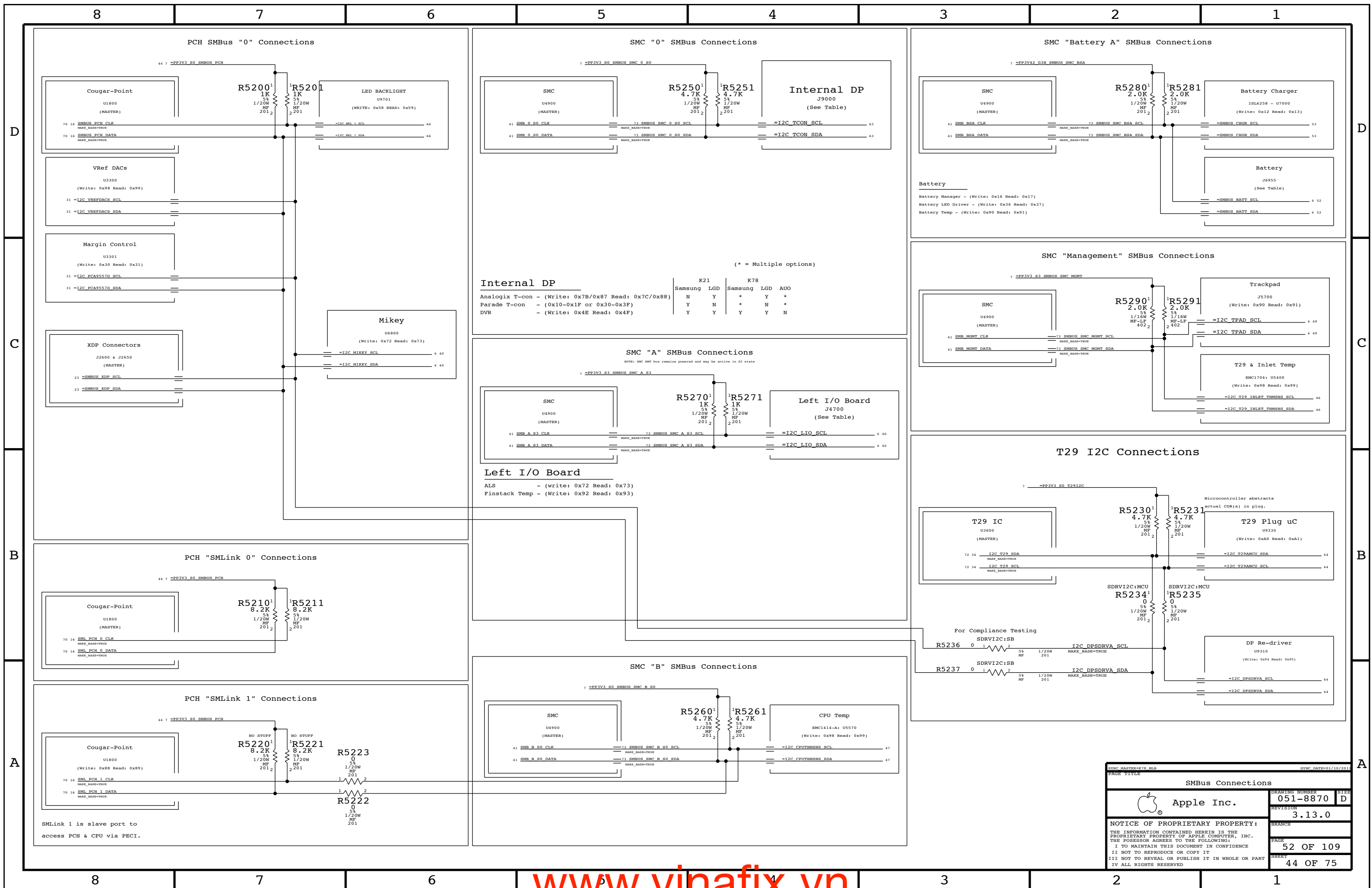
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SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
PAGE TITLE <b>LPC+SPI Debug Connector</b>			
DRAWING NUMBER <b>051-8870</b>		SIZE <b>D</b>	
REVISION <b>3.13.0</b>		BRANCH	
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		SHEET <b>43 OF 75</b>	





(\* = Multiple options)

	K21	K78		
Internal DP				
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y *
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N *
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y N

Apple Inc. logo

**SMBus Connections**

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

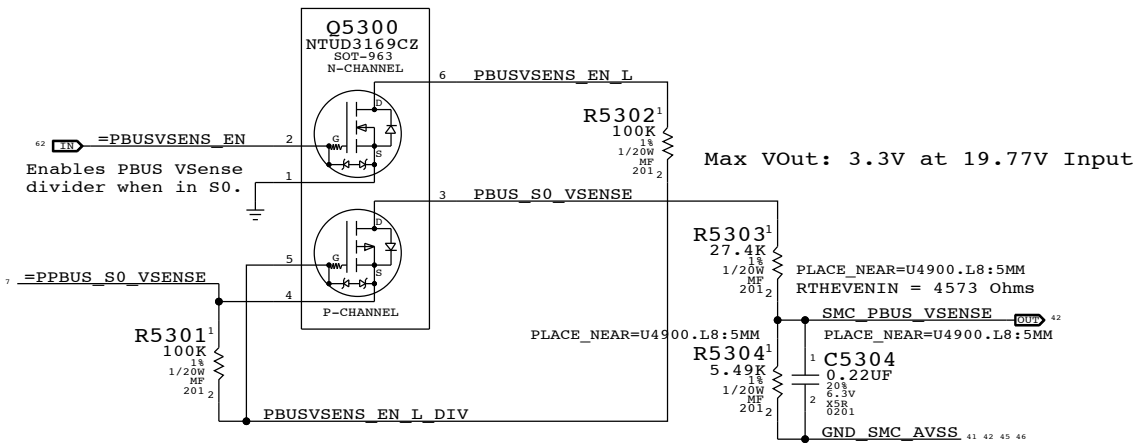
BRANCH:

PAGE: 52 OF 109

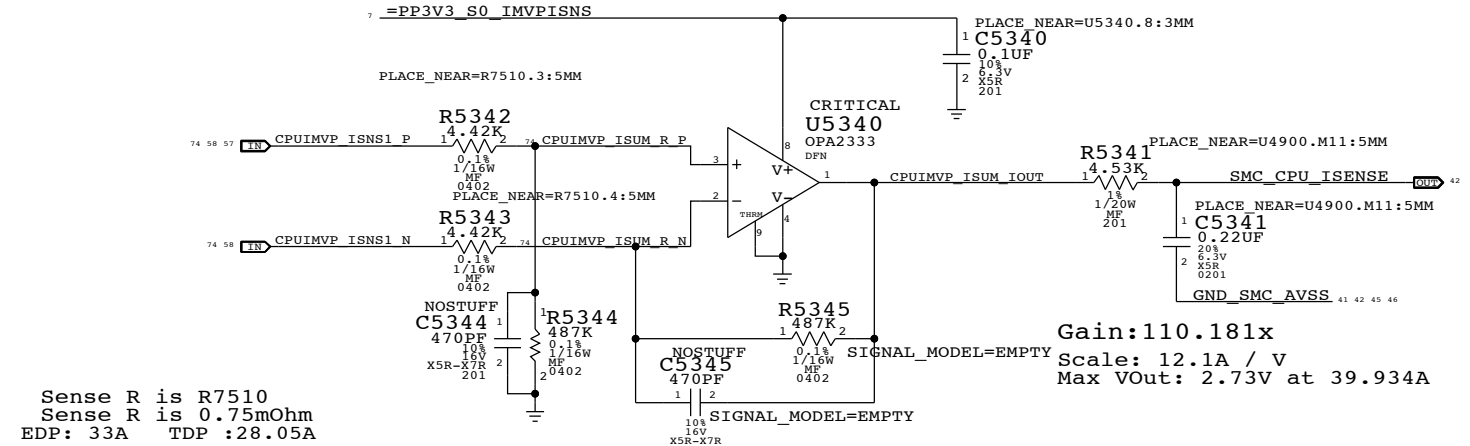
SHEET: 44 OF 75

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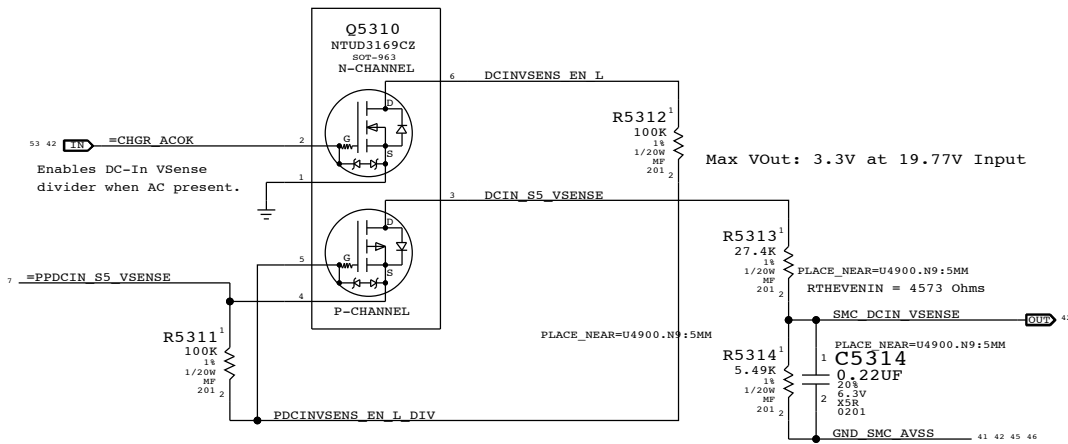
PBUS Voltage Sense Enable & Filter



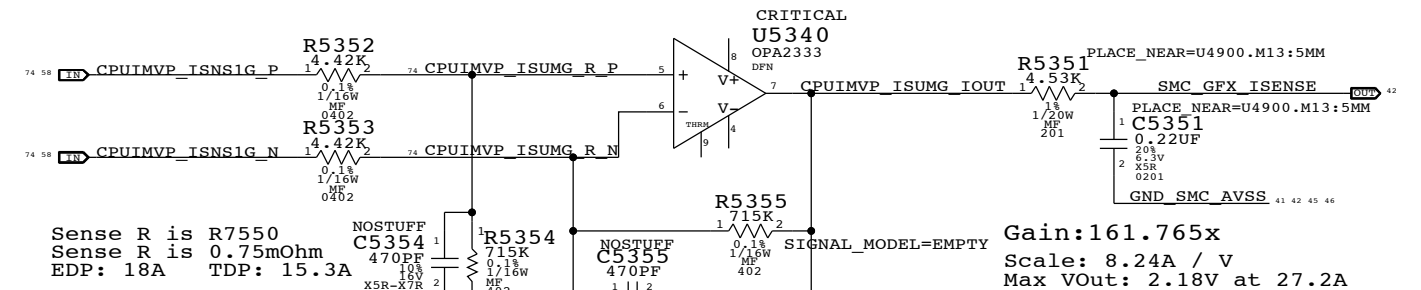
CPU VCore Load Side Current Sense / Filter



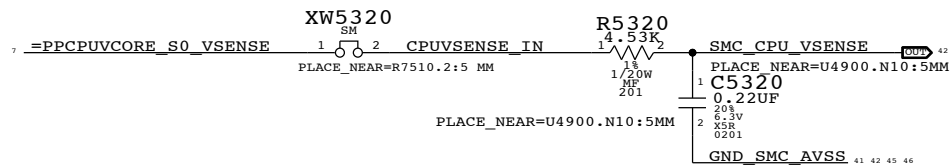
DC-In Voltage Sense Enable & Filter



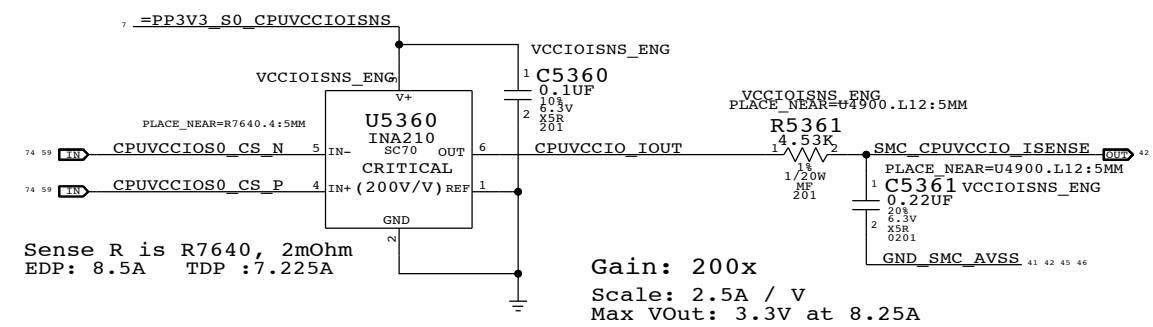
GFX/IG VCore Load Side Current Sense / Filter



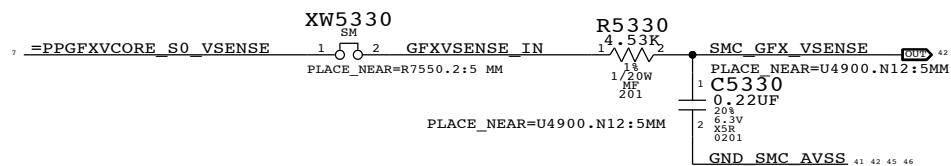
CPU Vcore Voltage Sense / Filter



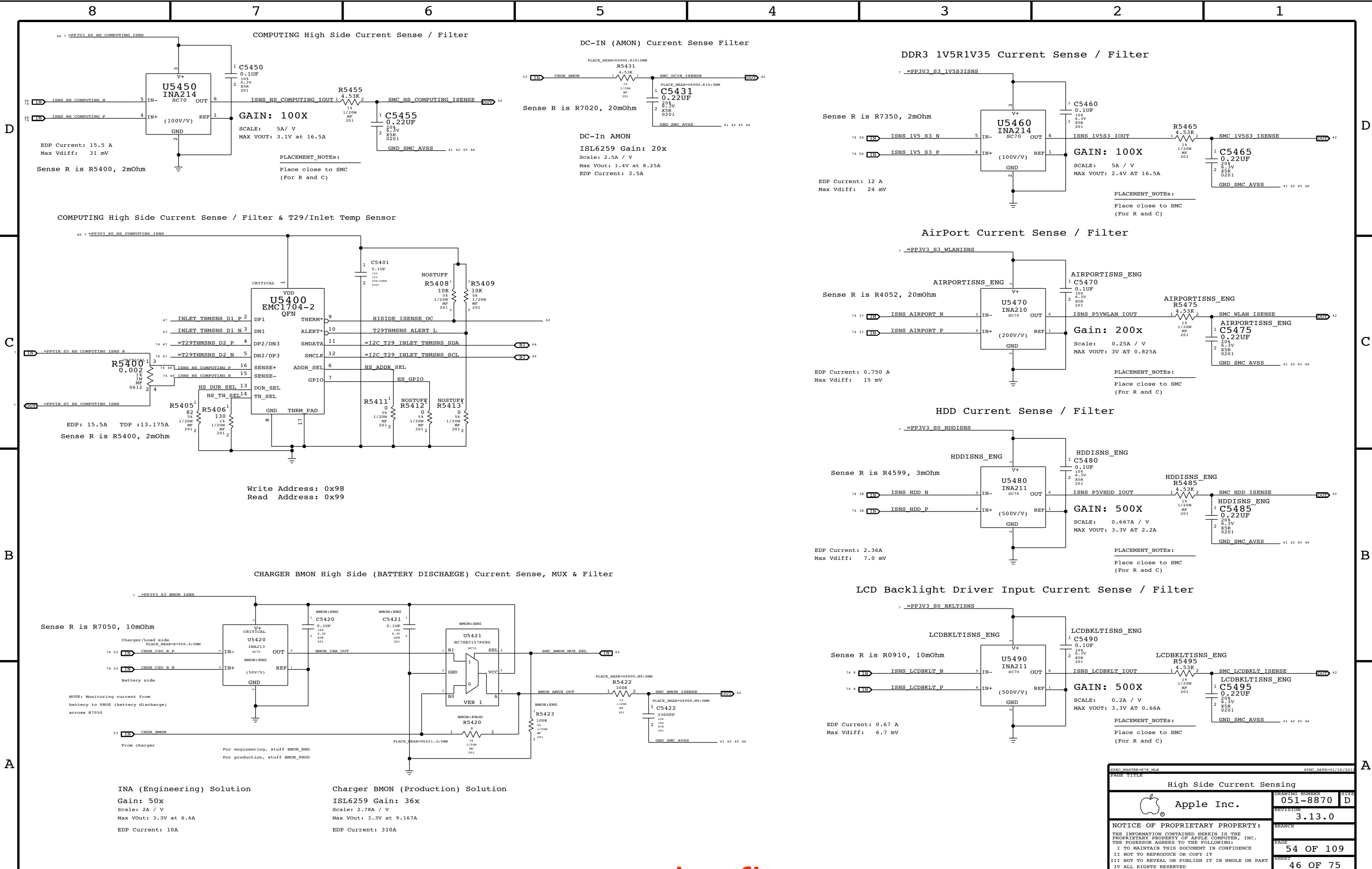
CPU 1.05V VCCIO Current Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
Voltage & Load Side Current Sensing			
Apple Inc.		DRAWING NUMBER	051-8870
		REVISION	3.13.0
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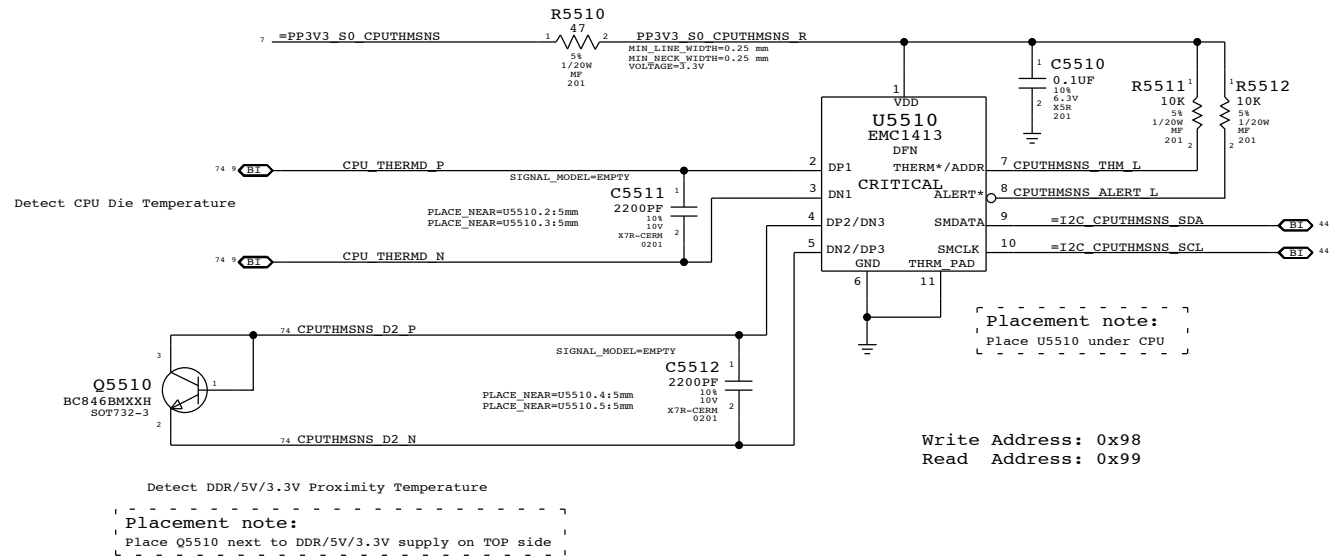


INA (Engineering) Solution  
 Gain: 50x  
 Scale: 2A / V  
 Max Vout: 3.3V at 6.6A  
 EDP Current: 10A

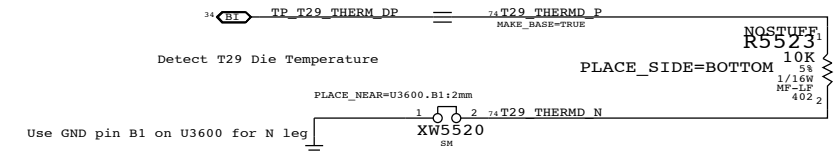
Charger BMON (Production) Solution  
 ISL6259 Gain: 36x  
 Scale: 2.78A / V  
 Max Vout: 3.3V at 9.167A  
 EDP Current: 310A

High Side Current Sensing	
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REVISION: 3.13.0	SIZE: D
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# CPU Proximity Sensor



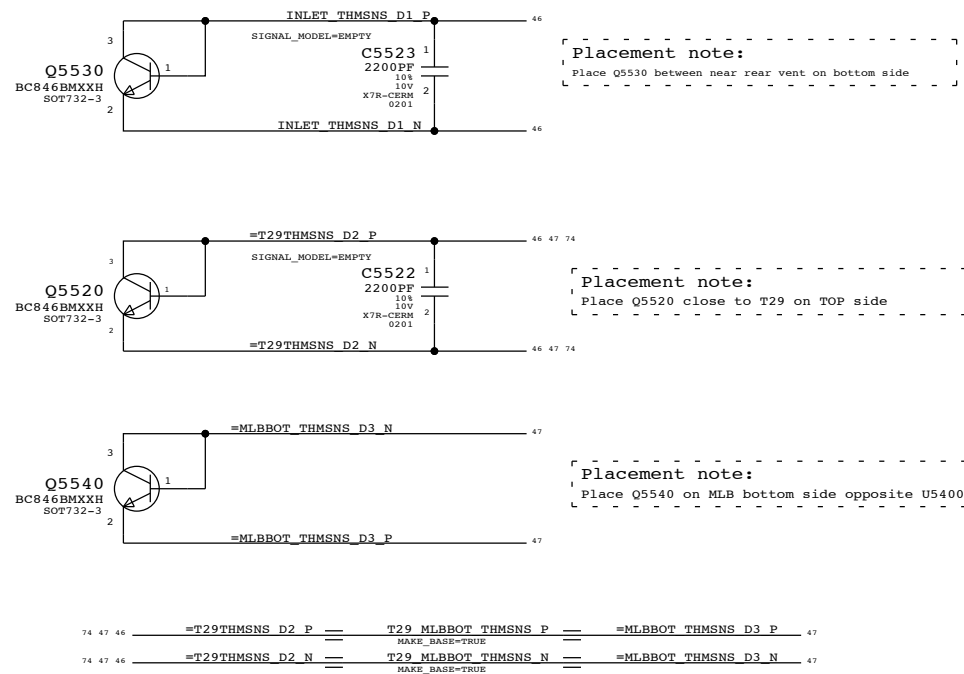
# T29 Die



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5485		HDDISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5495		LCDBKLTISNS_PROD

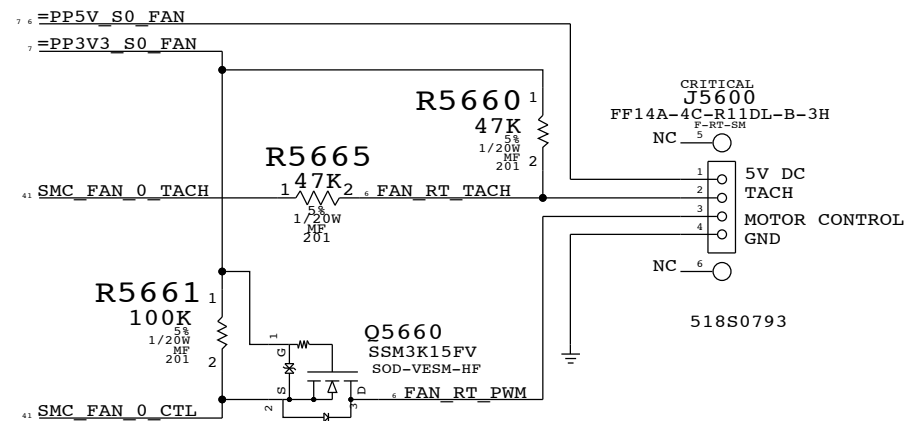
Replacing caps with 100K PD on ISENSE SMC inputs

# T29, MLB Bottom & Inlet Proximity Sensors



SYNC MASTER=K78 MLB		SYNC DATE=01/16/2011	
PAGE TITLE Thermal Sensors			
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	REVISION	3.13.0	
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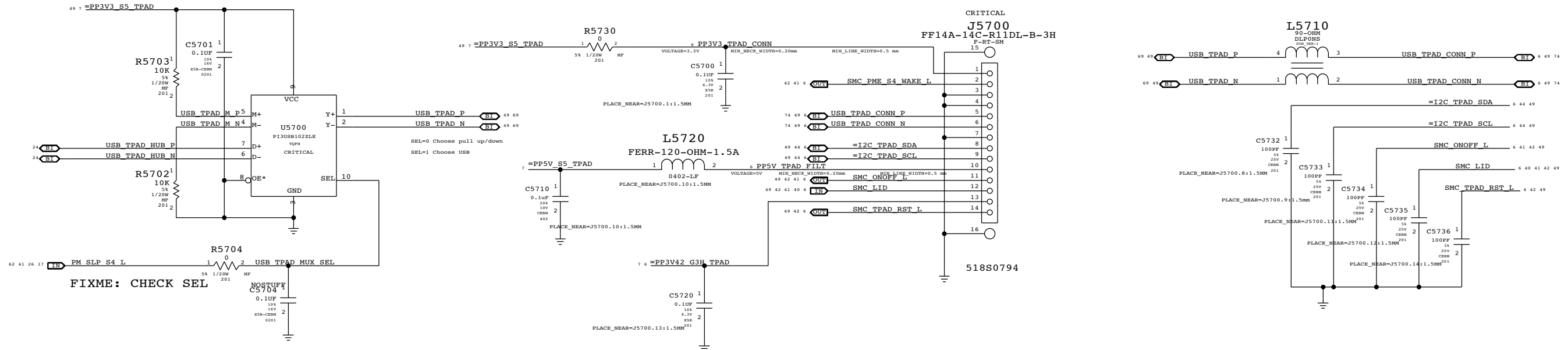
# FAN CONNECTOR



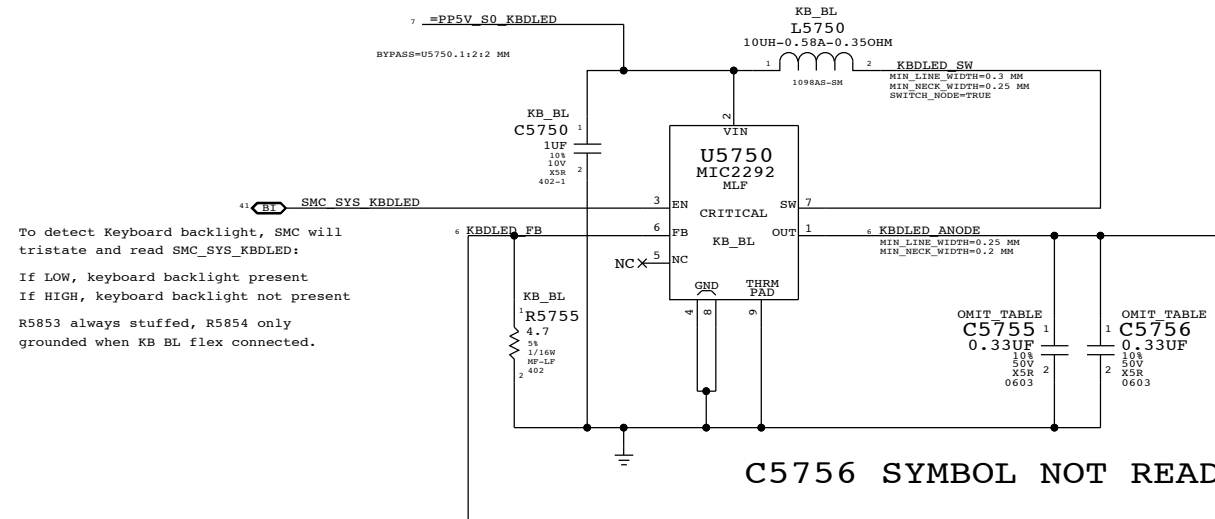
SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
PAGE TITLE			
Fan			
		DRAWING NUMBER	051-8870
		REVISION	3.13.0
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		PAGE	56 OF 109
		SHEET	48 OF 75
		SIZE	D



# IPD Flex Connector

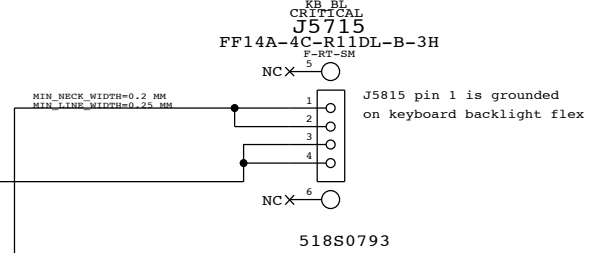


# Keyboard Backlight Driver & Detection



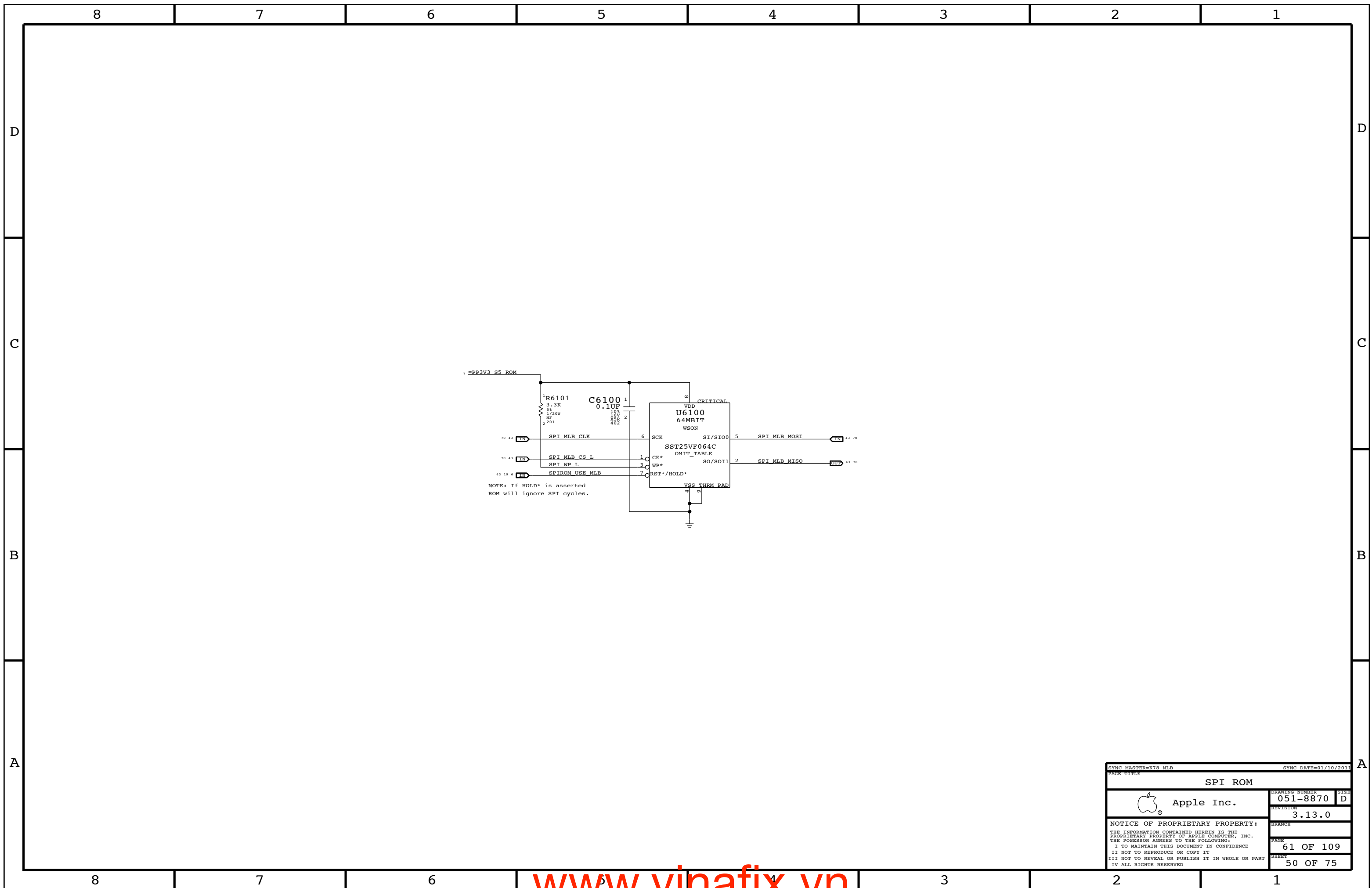
To detect Keyboard backlight, SMC will tristate and read SMC\_SYS\_KBDLED:  
 If LOW, keyboard backlight present  
 If HIGH, keyboard backlight not present  
 R5853 always stuffed, R5854 only grounded when KB BL flex connected.

# Keyboard Backlight Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
13880704	2	CAP, CER, 0.22UF, 10V, 50V, X5R, 0603	C5755, C5756		KB_BL

SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
PAGE TITLE			
IPD / KBD Backlight			SIZE
DRAWING NUMBER		051-8870	
Apple Inc.		D	
REVISION		3.13.0	
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BRANCH		PAGE	
57 OF 109		SHEET	
49 OF 75			



SYNC MASTER=K78_MLB		SYNC DATE=01/10/2011	
PAGE TITLE SPI ROM			
DRAWING NUMBER 051-8870		SIZE D	
REVISION 3.13.0		BRANCH	
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PAGE 61 OF 109		SHEET 50 OF 75	

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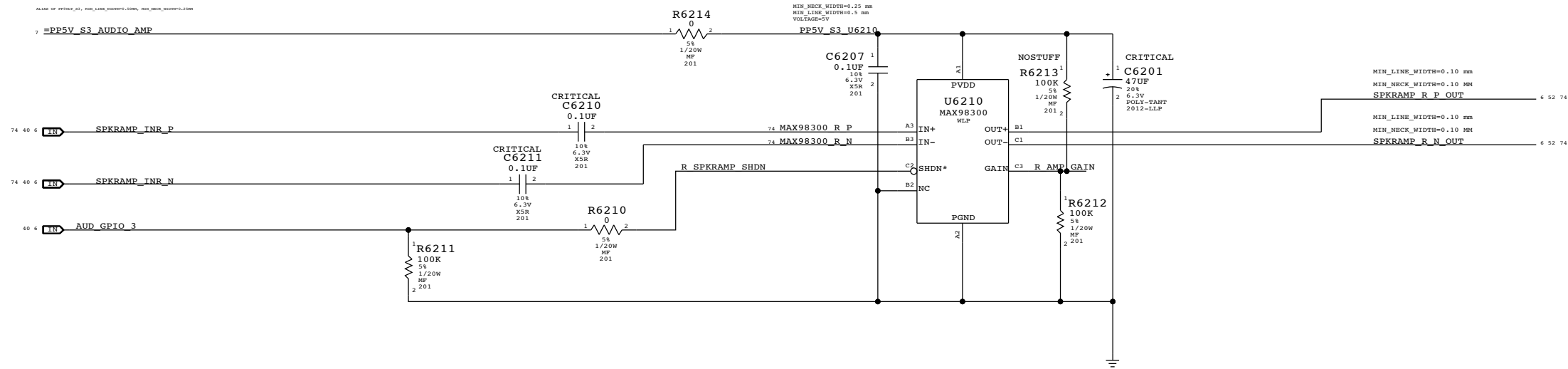
2

1

### SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ  
GAIN 6DB



D

D

C

C

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B

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SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
PAGE TITLE			
AUDIO: SPEAKER AMP			
DRAWING NUMBER		SIZE	
051-8870		D	
REVISION		PAGE	
3.13.0		62 OF 109	
BRANCH		SHEET	
		51 OF 75	
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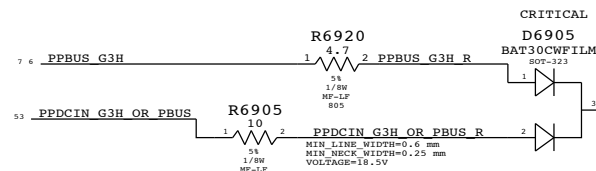
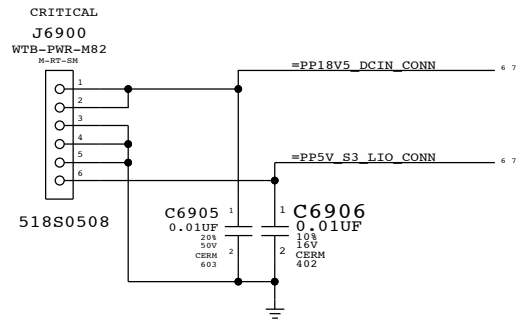
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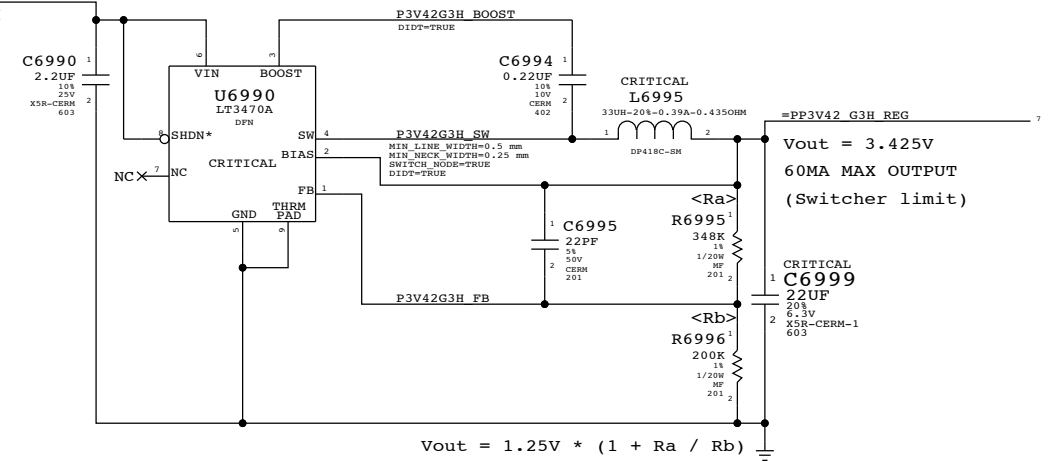
1

MLB to LIO Power Cable Connector



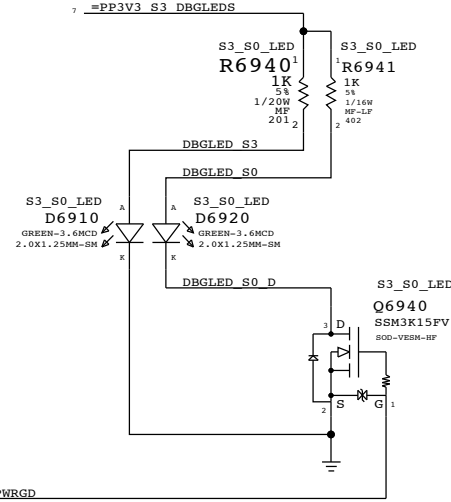
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

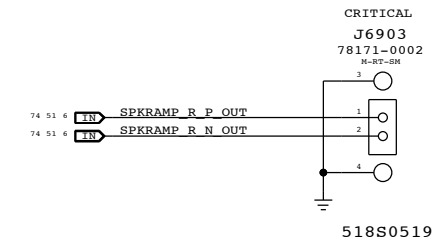


Debug LEDs

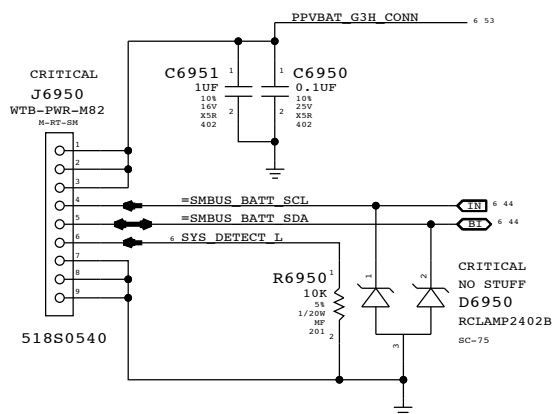
(For development only)



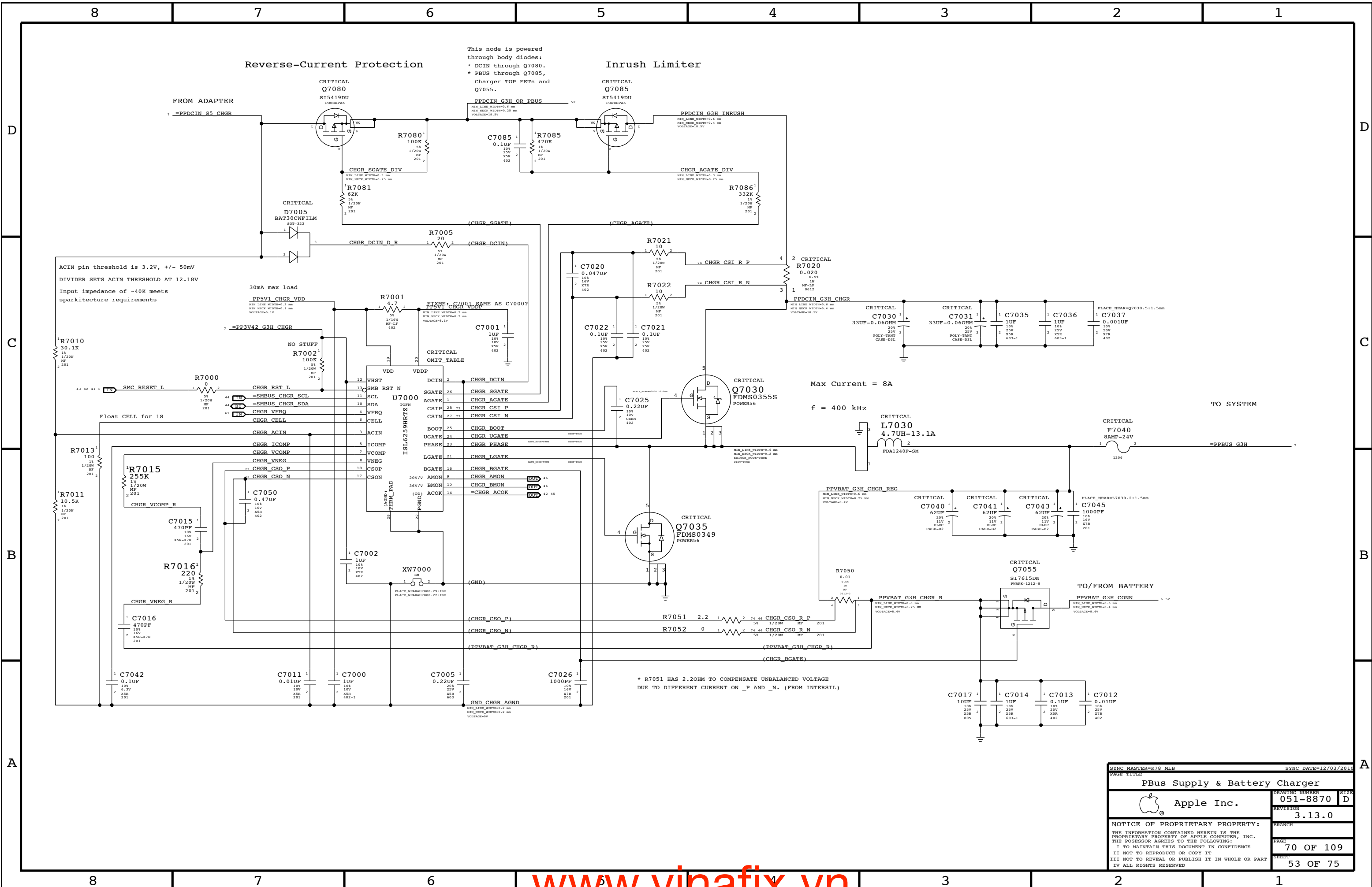
Right Speaker Connector



K16-Specific Battery Connector

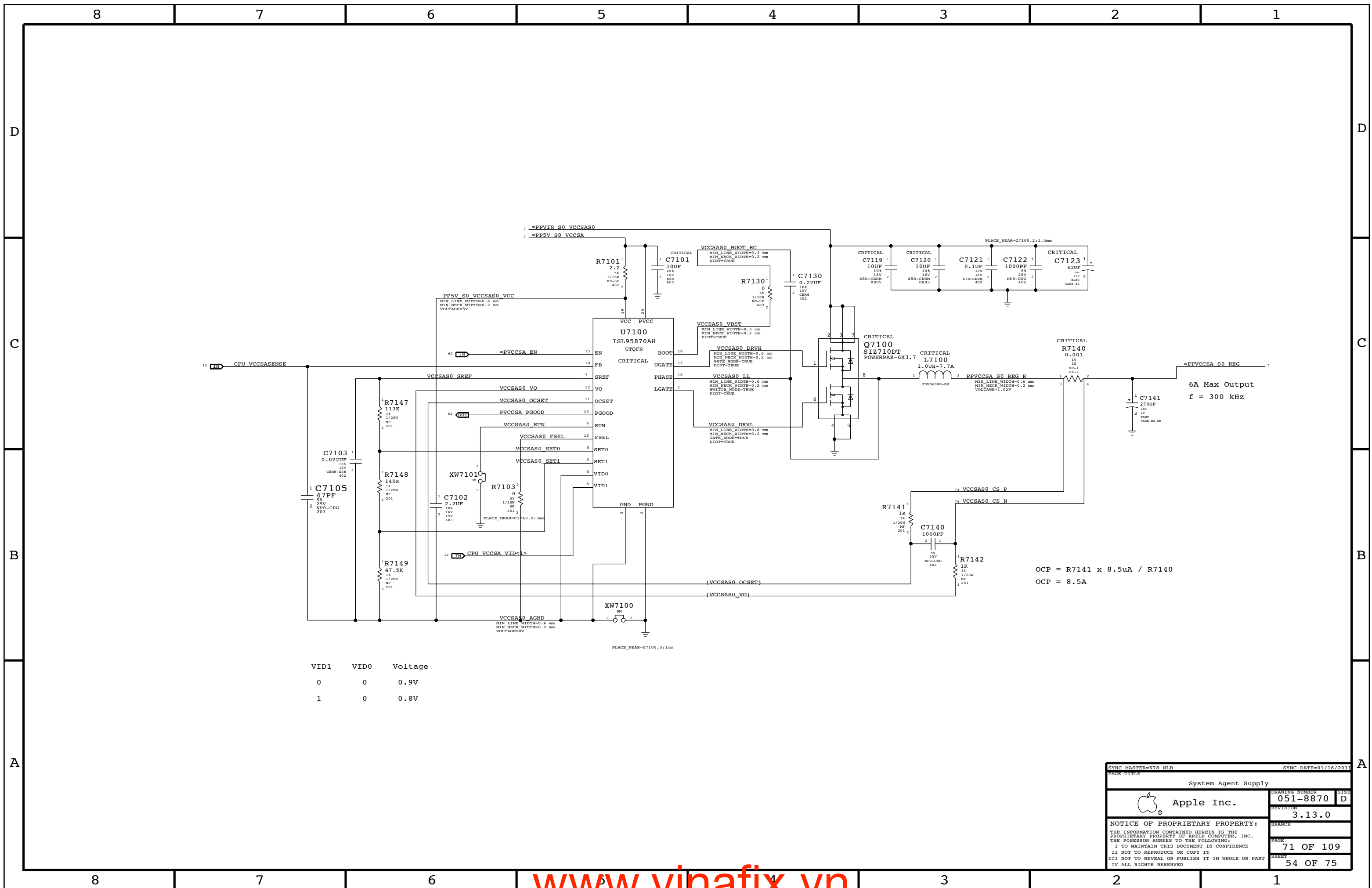


DC-In & Battery Connectors		DRAWING NUMBER	051-8870	SIZE	D
Apple Inc.		REVISION	3.13.0		
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SYNC MASTER=K78 MLB		SYNC DATE=12/03/2011	
PAGE TITLE			
PBus Supply & Battery Charger			
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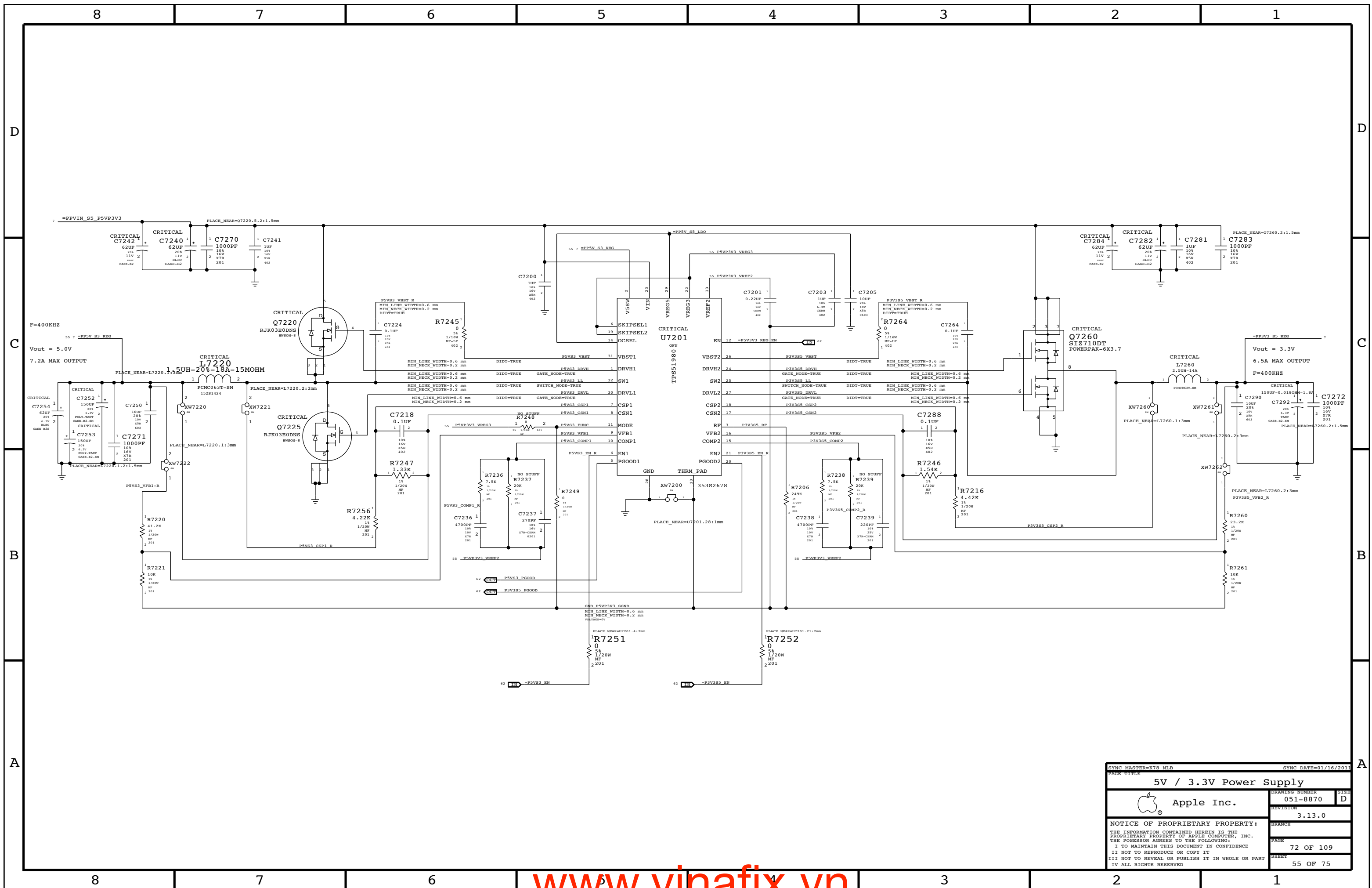




VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

OCP =  $R7141 \times 8.5\mu A / R7140$   
OCP = 8.5A

SYNC MASTER=K78 MLB		SYNC DATE=01/16/2011	
System Agent Supply			
Apple Inc.	DRAWING NUMBER	051-8870	SIZE D
	REVISION	3.13.0	
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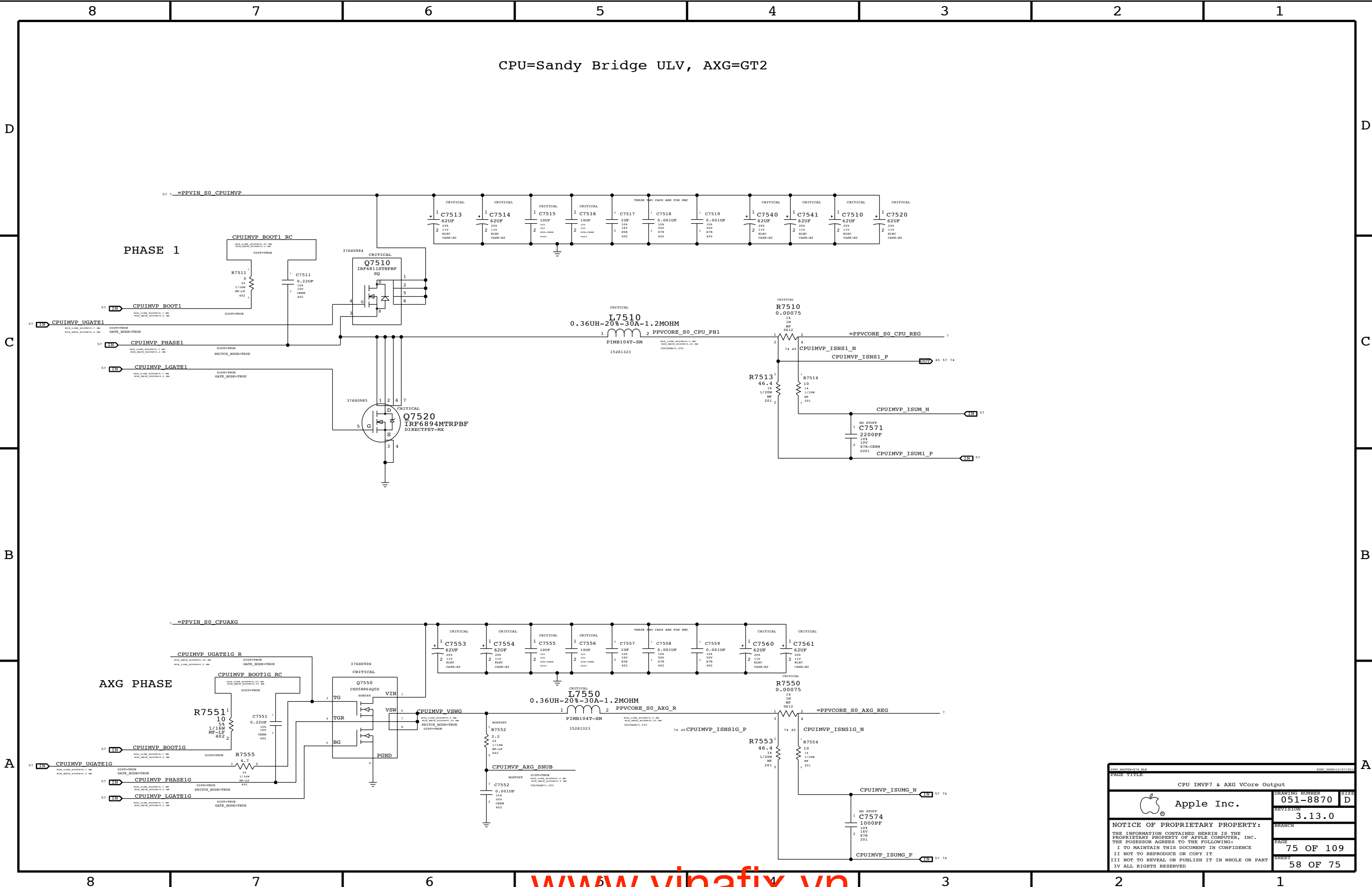


SYNC MASTER=K78 MLB		SYNC DATE=01/16/2011	
PAGE TITLE			
<b>5V / 3.3V Power Supply</b>			
Apple Inc.	DRAWING NUMBER	051-8870	SIZE
	REVISION	3.13.0	D
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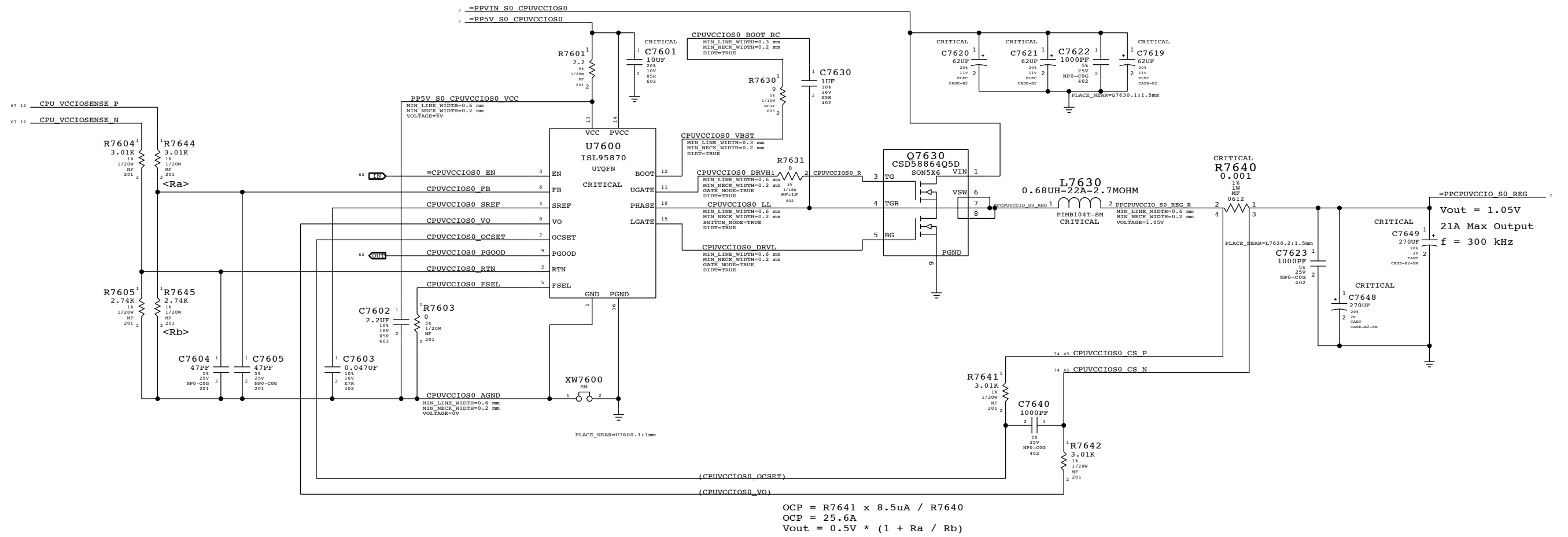
CPU=Sandy Bridge ULV, AXG=GT2



CPU INVP7 & AXG VCore Output		DRAWING NUMBER	051-8870	SIZE	D
Apple Inc.		REVISION	3.13.0		
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		SHEET	58 OF 75		

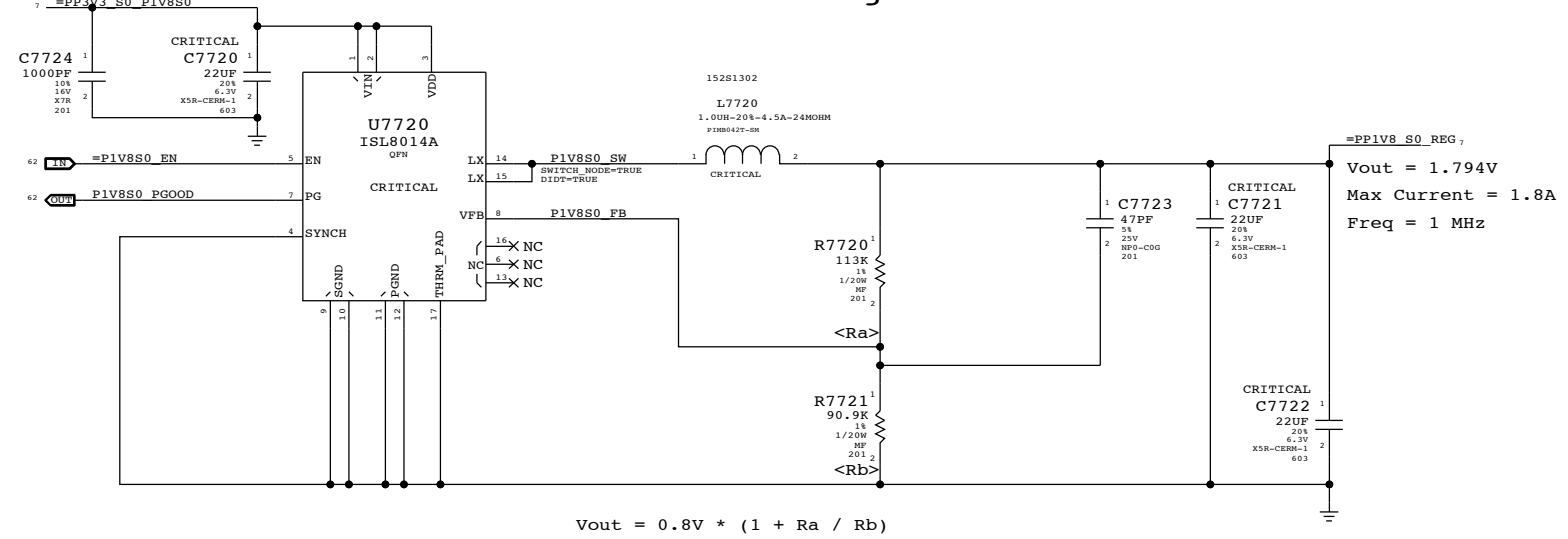


# CPU VCCIO (1.05V S0) Regulator



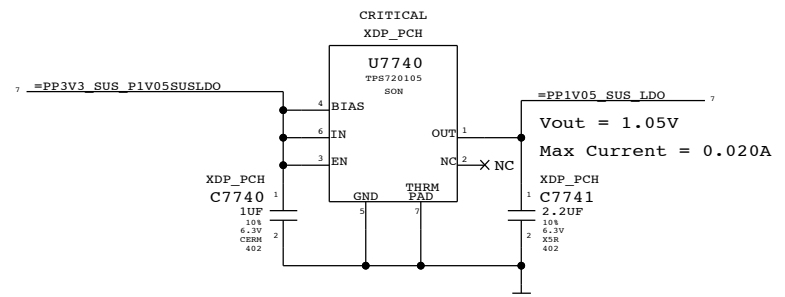
CPU VCCIO (1.05V) Power Supply	
Apple Inc.	DRAWING NUMBER: 051-8870
REVISION: 3.13.0	SIZE: D
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### 1.8V S0 Regulator

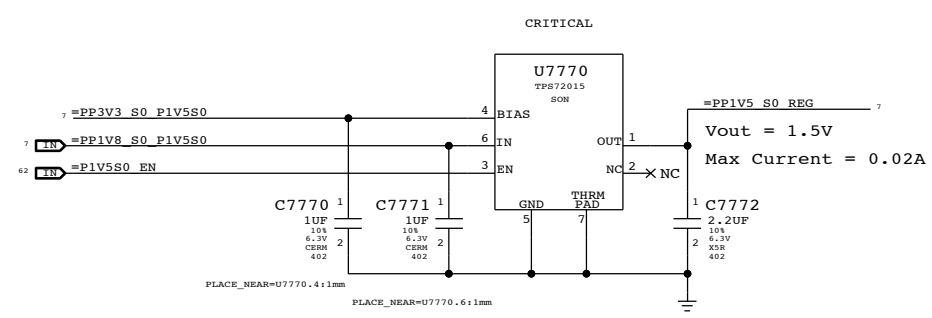


### 1.05V SUS LDO

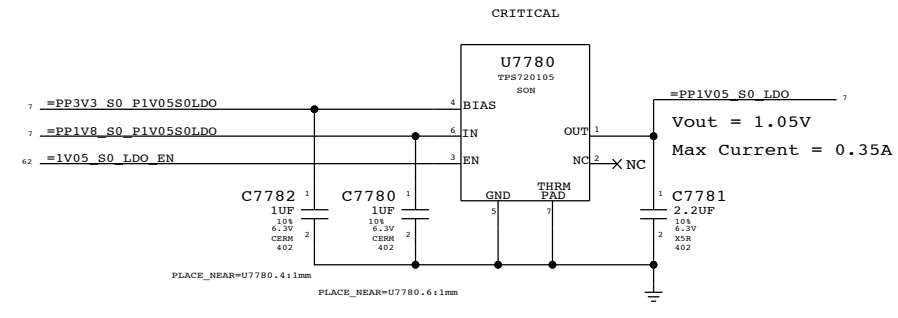
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



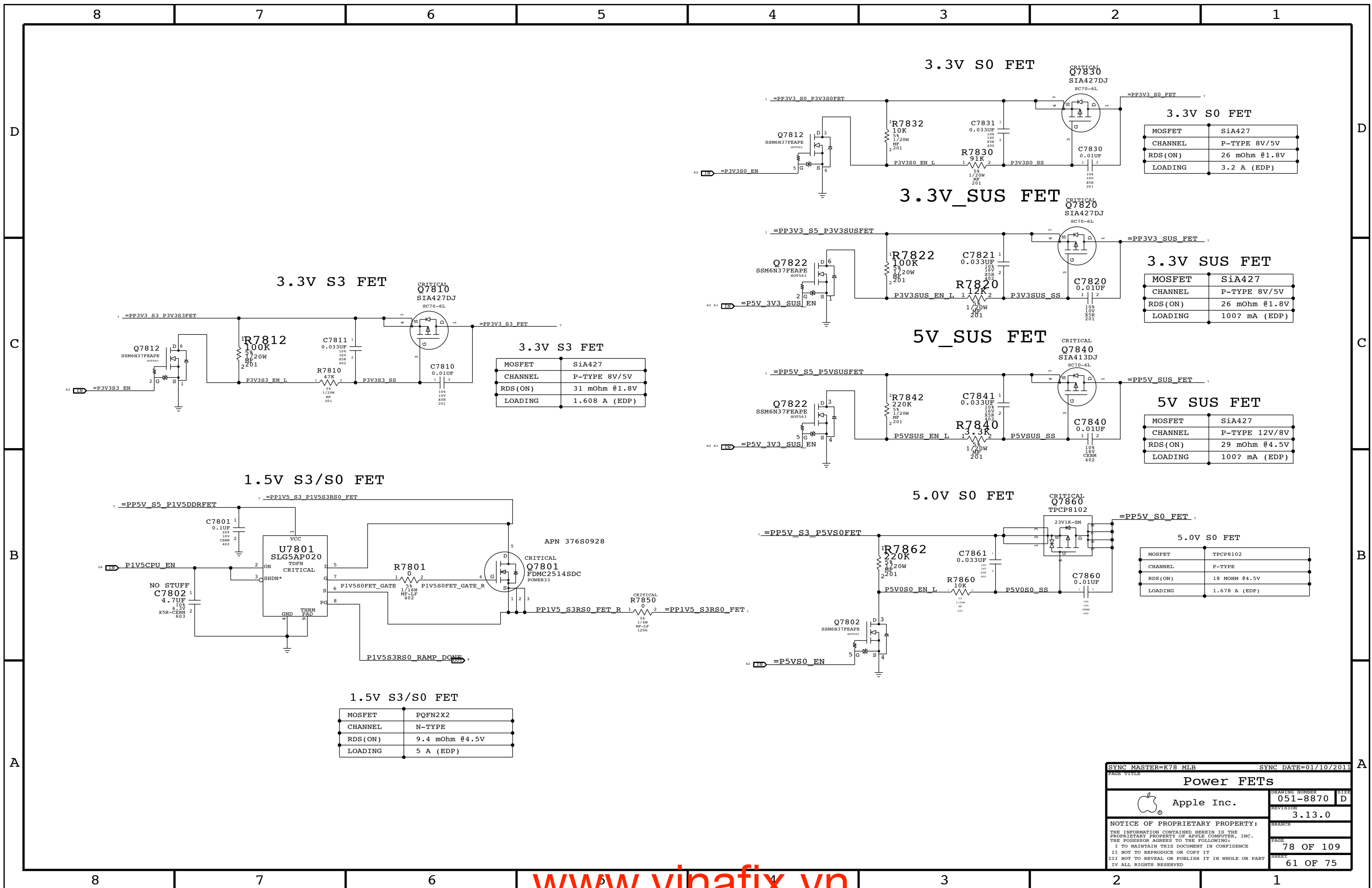
### 1.5V S0 LDO



### 1.05V S0 LDO



SYNC MASTER=K78_MLB		SYNC DATE=01/16/2011	
PAGE TITLE			
Misc Power Supplies			SIZE
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3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

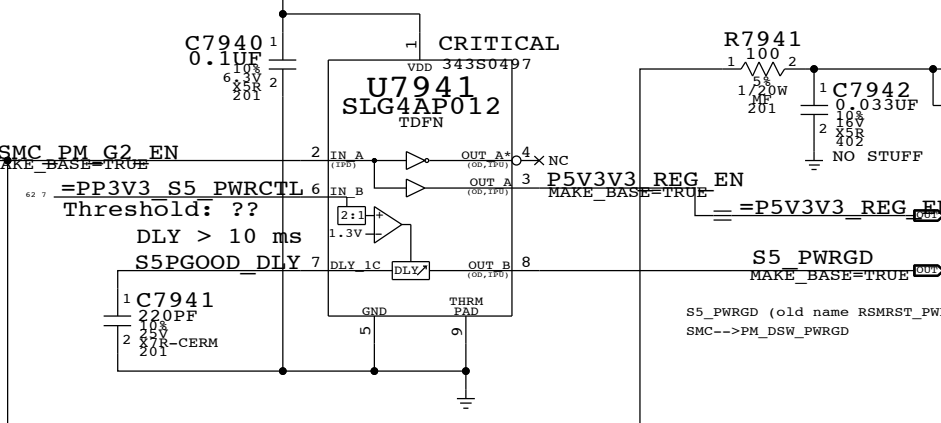
1.5V S3/S0 FET

MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
Power FETs			
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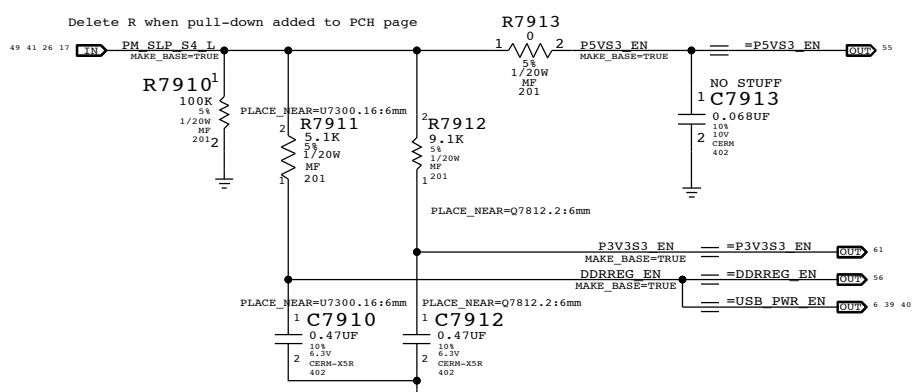
### S5 Rail Enables & PGOOD

=PP3V42\_G3H\_PWRCTL Internal pull-ups 100K +/- 20%

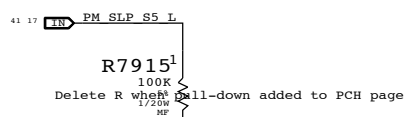


State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

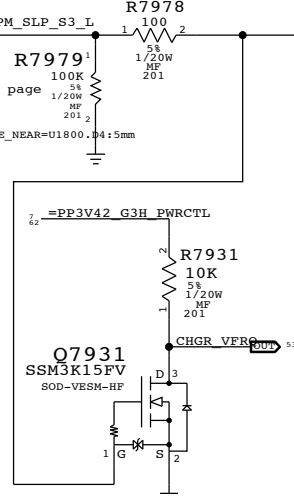
### 3.3V, 5V S3 ENABLE



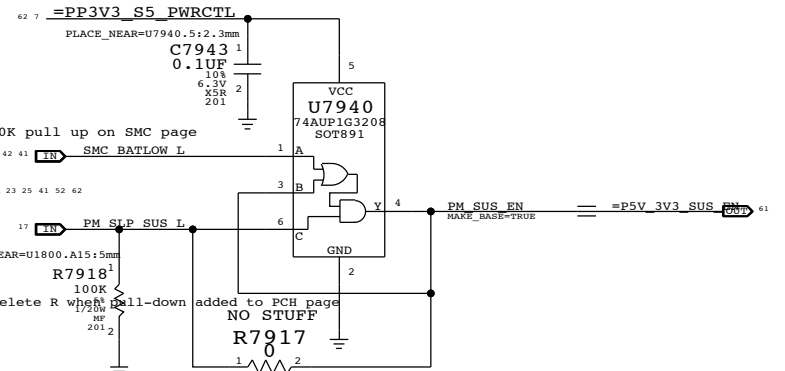
### 3.3V S4 ENABLE



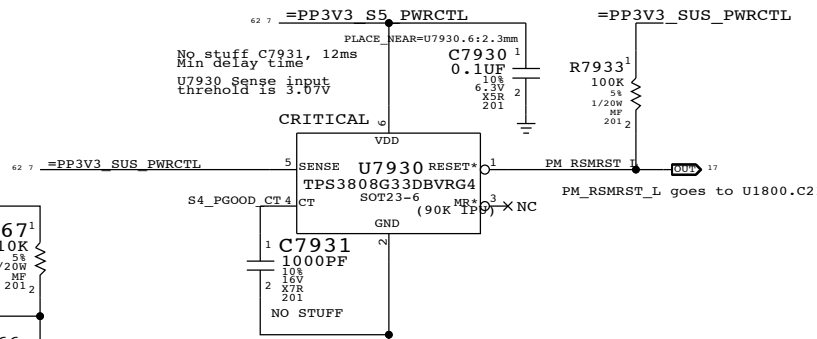
### S0 ENABLE



### 3.3V/5.0V Sus ENABLE

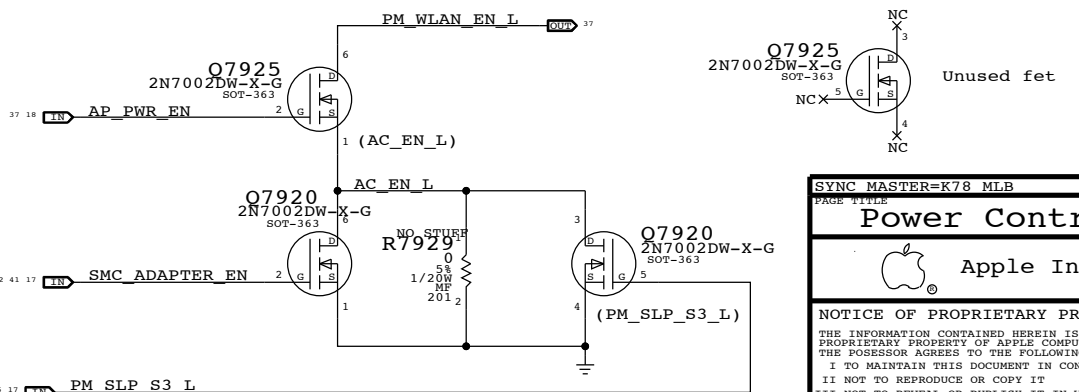


### 3.3V SUS Detect

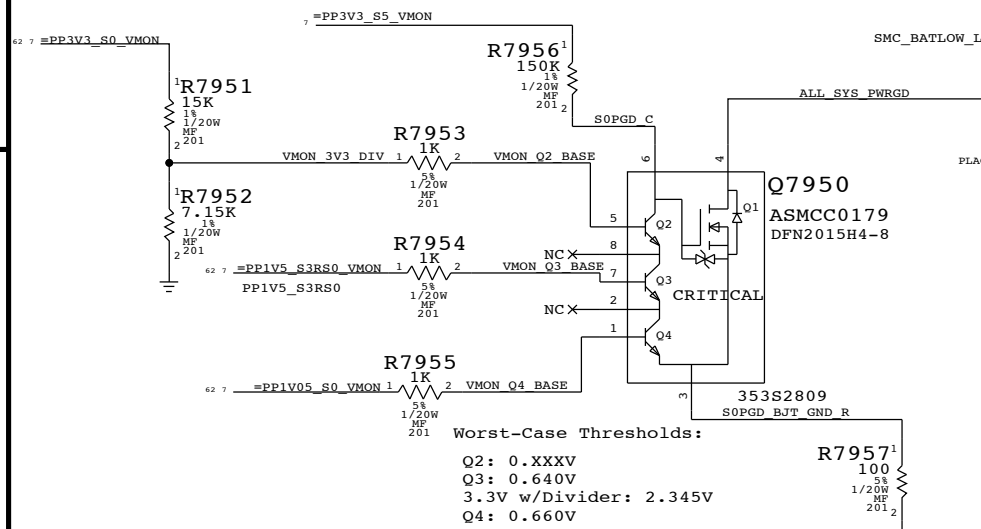


### WLAN Enable Generation

"WLAN" = ("S3" && "AP\_PWR\_EN" && ("AC" || "S0"))  
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.



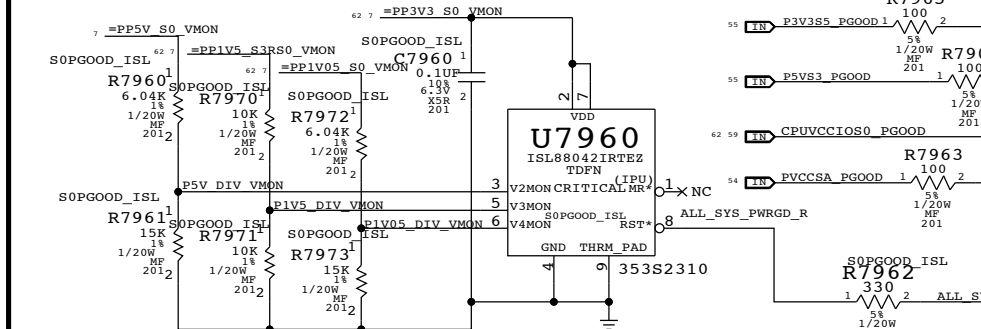
### S0 Rail PGOOD (BJT Version)



Worst-Case Thresholds:  
Q2: 0.XXXV  
Q3: 0.640V  
3.3V w/Divider: 2.345V  
Q4: 0.660V

### S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:  
VDD: 2.734V-3.010V  
V2MON: 2.815V-3.099V  
V3MON: 0.572V-0.630V  
V4MON: 0.572V-0.630V

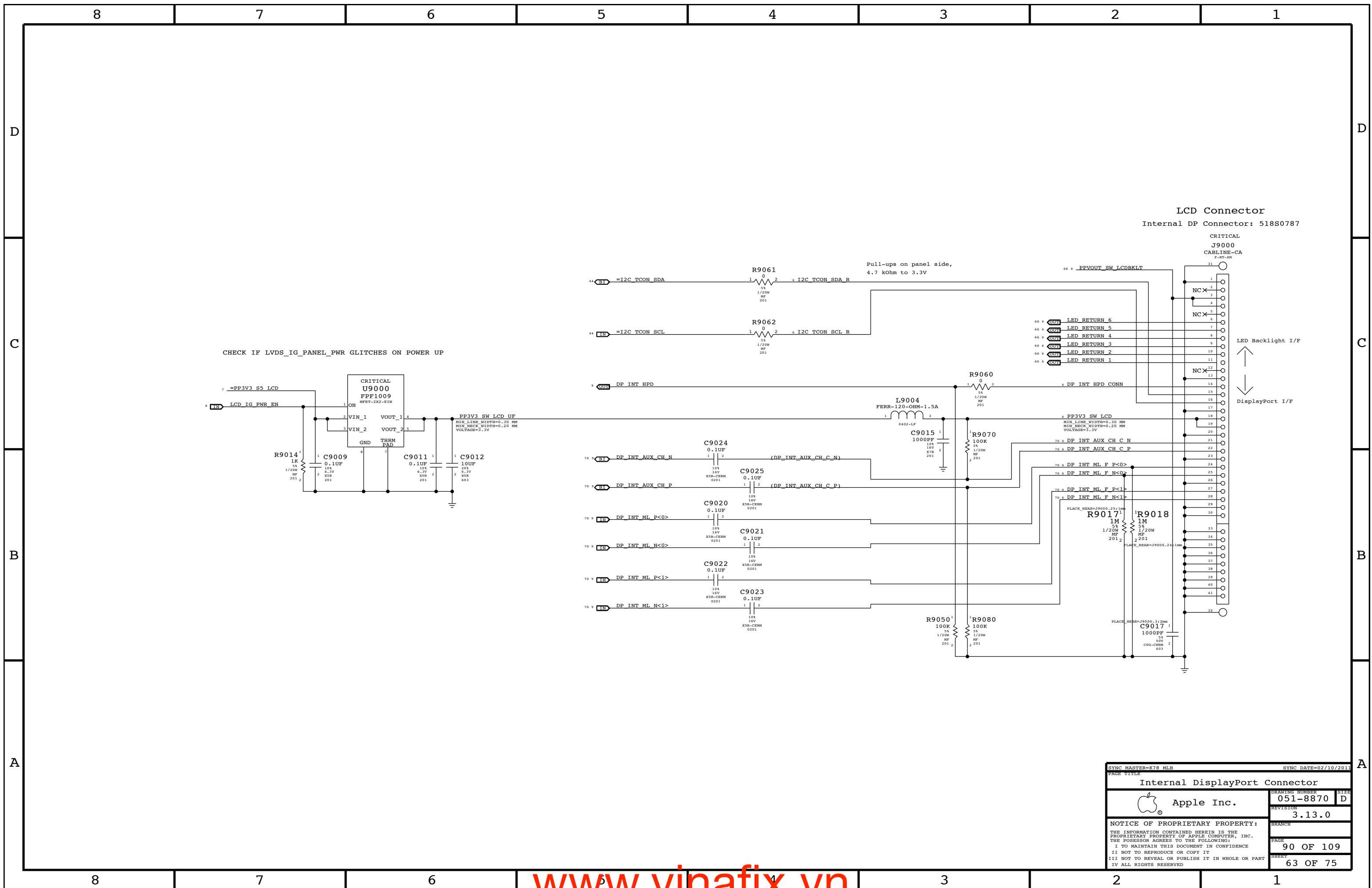


### DP S4 Power Enable

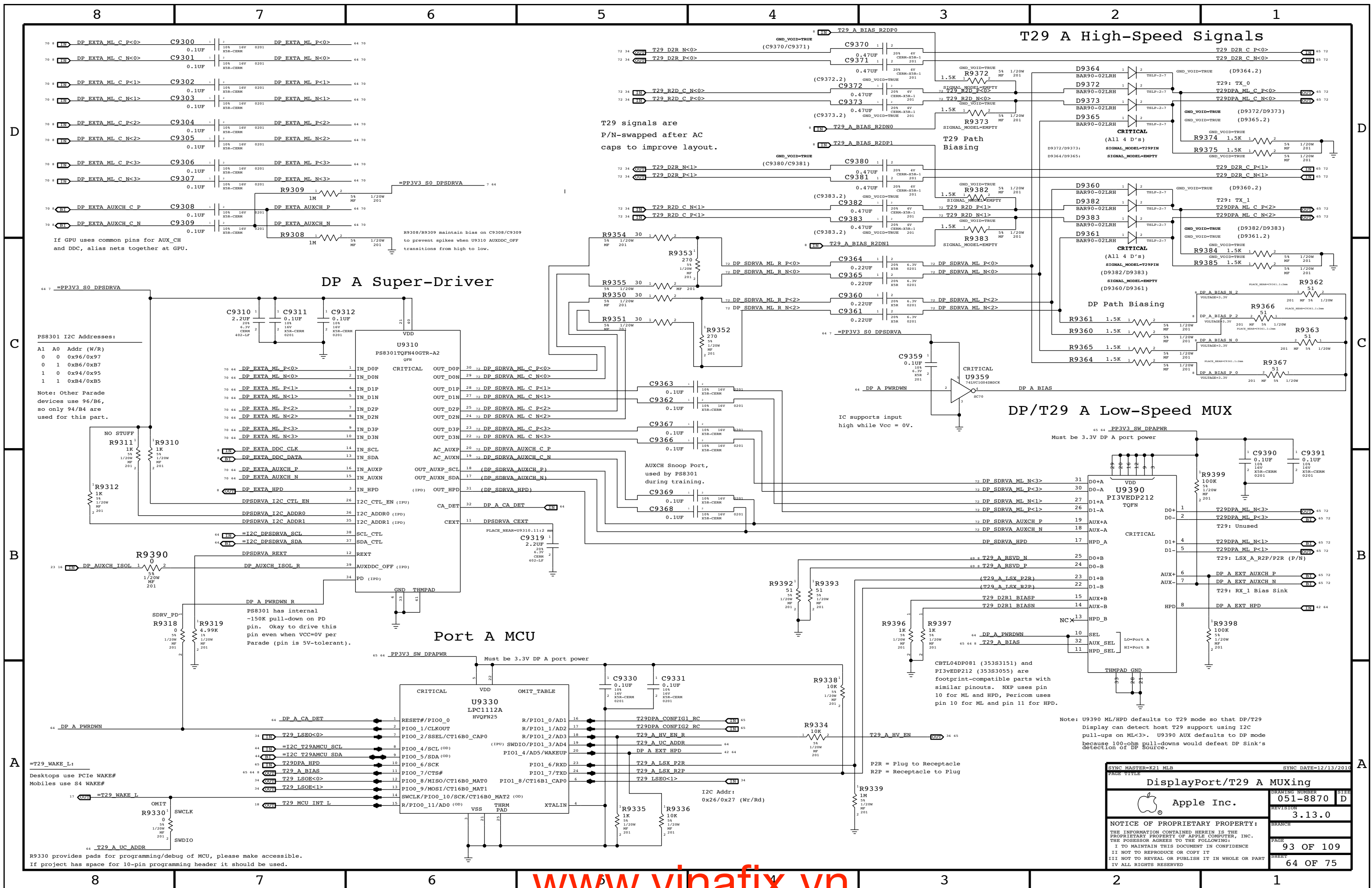
SMC S4 WAKESRC\_EN = DPAPWRSW\_EN

### PSOC USB Power Enable

SYNC MASTER=K78 MLB		SYNC DATE=01/10/2011	
<b>Power Control 1/ENABLE</b>			
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		REVISION	
		3.13.0	
		PAGE	
		79 OF 109	
		SHEET	
		62 OF 75	



SYNC MASTER=K78 MLB		SYNC DATE=02/10/2011	
Internal DisplayPort Connector			
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		SHEET	63 OF 75



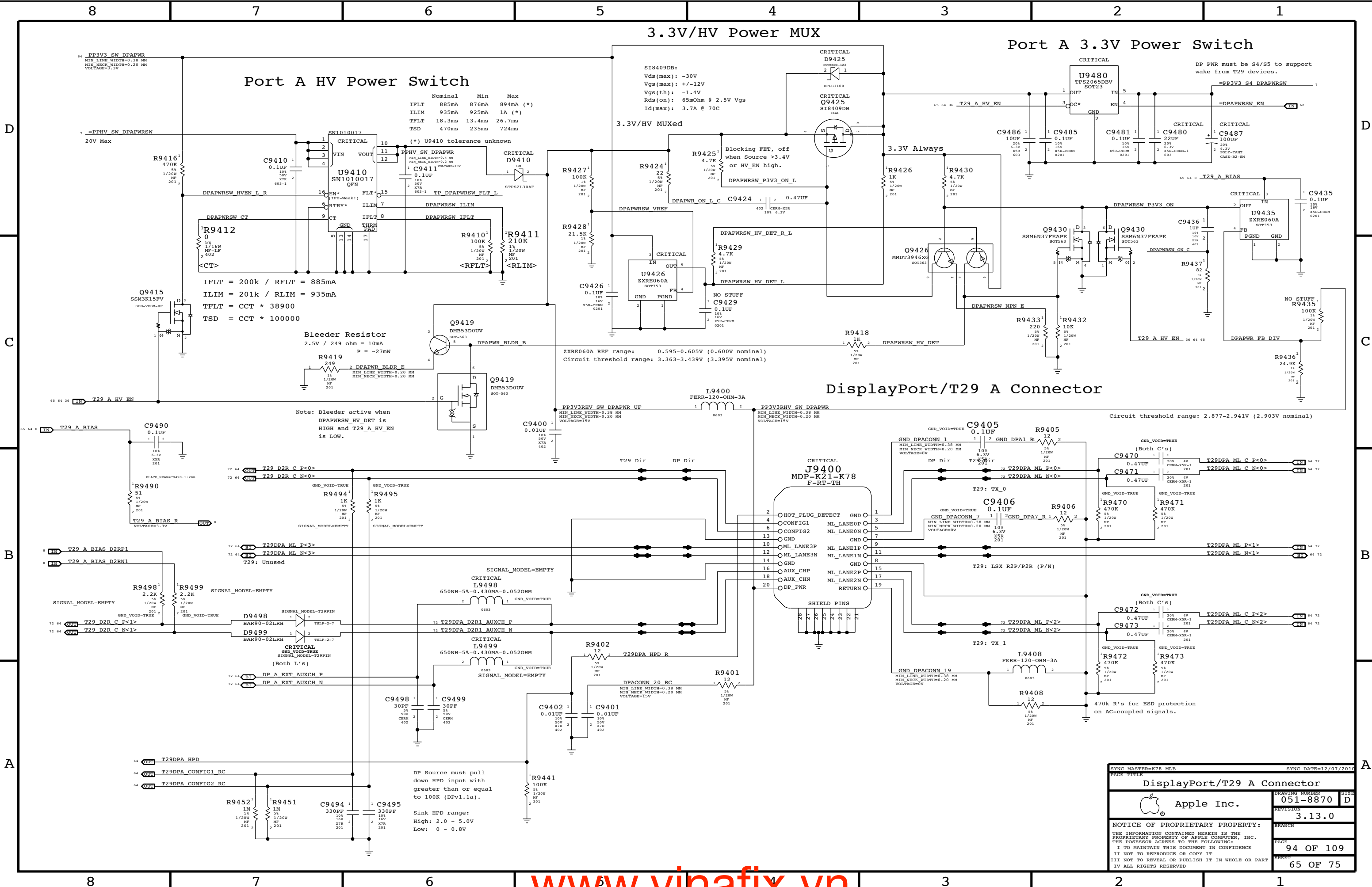
T29 signals are P/N-swapped after AC caps to improve layout.

IC supports input high while Vcc = 0V.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC MASTER=K21 MLB		SYNC DATE=12/13/2016	
PAGE TITLE		DRAWING NUMBER	
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		PAGE	
93 OF 109		SHEET	
64 OF 75		SIZE	
D		3.13.0	





**Port A HV Power Switch**

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	1A (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

**3.3V/HV Power MUX**

**Port A 3.3V Power Switch**

**DisplayPort/T29 A Connector**

IFLT = 200k / RFLT = 885mA  
 ILIM = 201k / RLIM = 935mA  
 TFLT = CCT \* 38900  
 TSD = CCT \* 100000

**Bleeder Resistor**  
 2.5V / 249 ohm = 10mA  
 P = -27mW

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)  
 Circuit threshold range: 3.363-3.439V (3.395V nominal)

Circuit threshold range: 2.877-2.941V (2.903V nominal)

Note: Bleeder active when DPAPWSW\_HV\_DET is HIGH and T29\_A\_HV\_EN is LOW.

SIGNAL\_MODEL=EMPTY

SIGNAL\_MODEL=T29PIN

SIGNAL\_MODEL=EMPTY

SIGNAL\_MODEL=T29PIN

(Both L's)

SIGNAL\_MODEL=EMPTY

SIGNAL\_MODEL=EMPTY

SIGNAL\_MODEL=EMPTY

SIGNAL\_MODEL=EMPTY

SIGNAL\_MODEL=EMPTY

SIGNAL\_MODEL=EMPTY

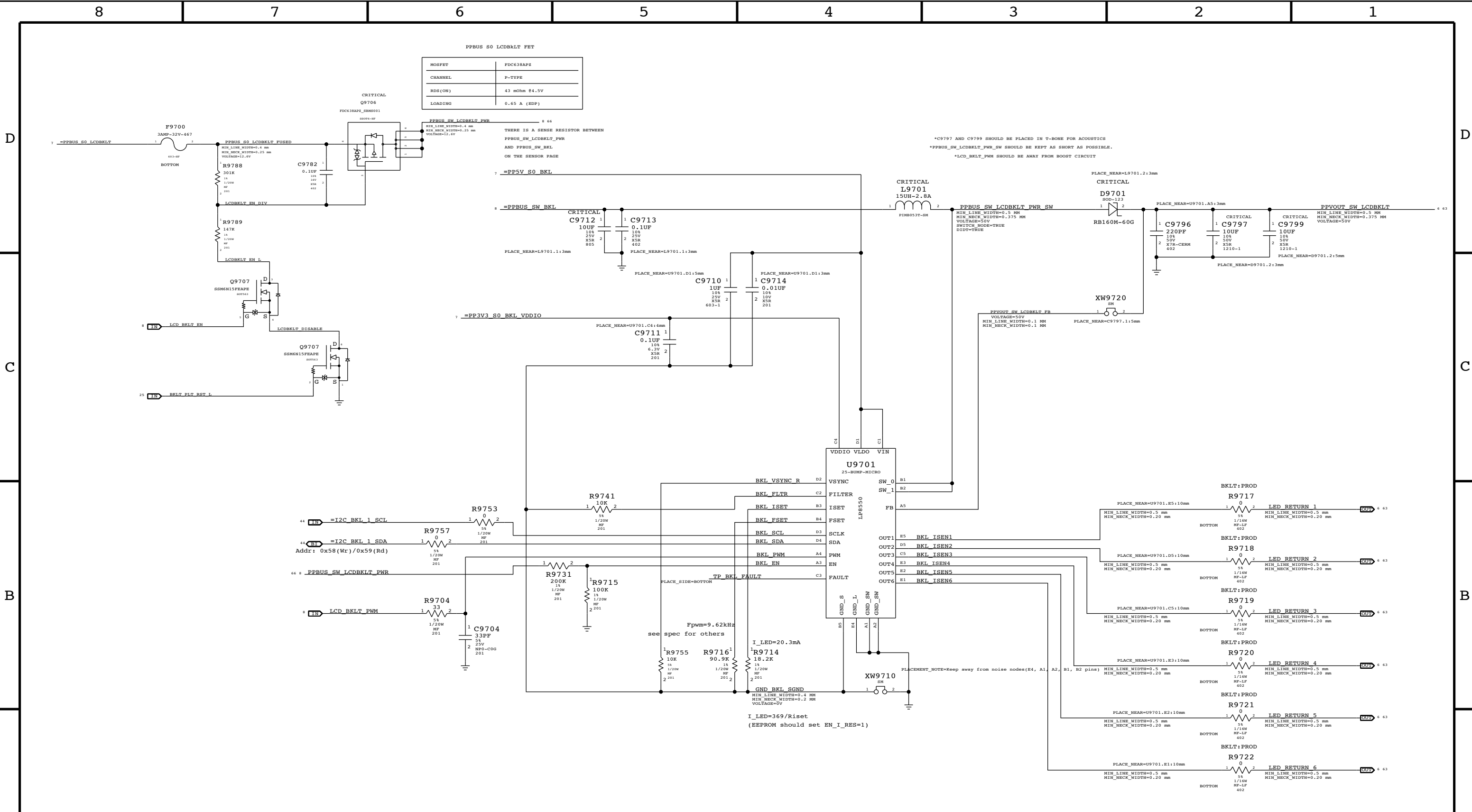
SIGNAL\_MODEL=EMPTY

DP Source must pull down HPD input with greater than or equal to 100k (DPv1.1a).

Sink HPD range:  
 High: 2.0 - 5.0V  
 Low: 0 - 0.8V

SYNC MASTER=K78 MLB		SYNC DATE=12/07/2011	
PAGE TITLE			
DisplayPort/T29 A Connector		DRAWING NUMBER	SIZE
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PPBUS SW LCDBKLT FET	
MOSFET	FDC638APE
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9717, R9718, R9719		BKLT:ENG
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K78 MLB SYNC DATE=01/16/2011

PAGE TITLE: LCD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_XDP_BPM	TOP,BOTTOM	100 MIL	100 MIL	100 MIL	100 MIL	=STANDARD	=STANDARD
CPU_XDP_BPM	*	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S

NOTE: CPU\_XDP\_BPM physical constraint is to prevent routing on outer layers.  
NOTE: 7 mil gap is for VCCsense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_BML	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297\_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SOURCE: Huron River SFF DG (DG-438297\_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>
CPU_50S	CPU_AGTL	CPU	FDI_FSYN<1..0>
CPU_50S	CPU_AGTL	CPU	FDI_LSYN<1..0>
CPU_50S	CPU_AGTL	CPU	FDI_INT
CPU_PECT	CPU_50S	PCIE	CPU_PECT
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD
CPU_50S	CPU_ITP	CPU	XDP_DBRESET_L
CPU_50S	CPU_ITP	CPU	XDP_CPU_PRDY_L
CPU_50S	CPU_ITP	CPU	XDP_CPU_PREQ_L
CPU_50S	CPU_AGTL	CPU	PM_EXT_TS_L<0>
CPU_50S	CPU_AGTL	CPU	PM_EXT_TS_L<1>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>
CPU_50S	CPU_ITP	CPU	CPU_CFG<11..0>
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L
CPU_50S	CPU_AGTL	CPU	CPU_VCCIO_SEL
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD
PM_THRMTRIP_L	CPU_50S	CPU_BMTL	PM_THRMTRIP_L
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N
ITPXDP_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P
ITPXDP_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N
XDP_CPU_CLK100M_P	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P
XDP_CPU_CLK100M_N	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N
CPU_27P4S	CPU_COMP	CPU	EDP_COMP
CPU_27P4S	CPU_COMP	CPU	CPU_PEG_COMP
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L
XDP_BPM_L	CPU_XDP_BPM	CPU_ITP	XDP_BPM_L<7..0>
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>
(ESB_CUREST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P
CPU_VCCXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT
PCIE_85D	PCIE	PCIE	PEG_R2D_P<15..0>
PCIE_85D	PCIE	PCIE	PEG_R2D_N<15..0>
PCIE_85D	PCIE	PCIE	PEG_R2D_C_P<15..0>
PCIE_85D	PCIE	PCIE	PEG_R2D_C_N<15..0>
PCIE_85D	PCIE	PCIE	PEG_D2R_P<15..0>
PCIE_85D	PCIE	PCIE	PEG_D2R_N<15..0>
PCIE_85D	PCIE	PCIE	PEG_D2R_C_P<15..0>
PCIE_85D	PCIE	PCIE	PEG_D2R_C_N<15..0>

CPU\_VCCSA\_VID<0>  
CPU\_VCCSA\_VID<1>

SYNCHMASTER11 CONSTRAINTS SYNCHDATE04/06/2011  
PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D  
REVISION 3.13.0

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PAGE 100 OF 109  
SHEET 67 OF 75

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_378	*	=37_OHM_RE	=37_OHM_RE	=37_OHM_RE	=37_OHM_RE	=STANDARD	=STANDARD
MEM_408	*	=40_OHM_RE	=40_OHM_RE	=40_OHM_RE	=40_OHM_RE	=STANDARD	=STANDARD
MEM_558	*	=55_OHM_RE	=55_OHM_RE	=55_OHM_RE	=55_OHM_RE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_508	TOP_BOTTOM	Y	=50_OHM_RE	=50_OHM_RE	=50_OHM_RE	=STANDARD	=STANDARD
MEM_85D	TOP_BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_508	18L3,18L4,18L9,18L10	Y	=50_OHM_RE	=50_OHM_RE	=50_OHM_RE	=STANDARD	=STANDARD
MEM_85D	18L3,18L4,18L9,18L10	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	7
MEM_CTRL2CTRL	*	0.2 MM	7
MEM_CMD2CTRL	*	0.2 MM	7
MEM_CMD2CMD	*	0.2 MM	7
MEM_DATA2DATA	*	0.14 MM	7
MEM_DQS2DQS	*	0.4 MM	7
MEM_MEM2OTHERMEM	*	0.4 MM	7
MEM_F2WR	=FWR_F2WR		7
MEM_GND	=GND_F2WR		7
MEM_OTHER	*	0.6 MM	7

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_F2WR
MEM_CTRL	MEM_PWR	*	MEM_F2WR
MEM_CMD	MEM_PWR	*	MEM_F2WR
MEM_DQS	MEM_PWR	*	MEM_F2WR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_GND
MEM_CTRL	GND	*	MEM_GND
MEM_CMD	GND	*	MEM_GND
MEM_DATA	GND	*	MEM_GND
MEM_DQS	GND	*	MEM_GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CMD	*	MEM_CMD2CTRL
MEM_CLK	MEM_DATA	*	MEM_DATA2DATA
MEM_CLK	MEM_DQS	*	MEM_DQS2DQS
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CMD2CTRL
MEM_CTRL	MEM_DATA	*	MEM_DATA2DATA
MEM_CTRL	MEM_DQS	*	MEM_DQS2DQS
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_DATA2DATA
MEM_CMD	MEM_DQS	*	MEM_DQS2DQS
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DQS2DQS
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS
MEM_DQS	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_DQS	MEM_CMD	*	MEM_CMD2CTRL
MEM_DQS	MEM_DATA	*	MEM_DATA2DATA
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

Need to support MEM\_\*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).  
 DQ intra-pair matching should be within 0.127mm, no inter-pair matching requirement.  
 DQ to DQS matching per byte lane should be within 0.127mm.  
 DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].  
 CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.  
 CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.  
 A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.  
 DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.  
 Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from processor ball to SODIMM pad is 88.9mm.  
 SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM_A_CLK P<5..0> 8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM_A_CLK N<5..0> 8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM_A_CKE<3..0> 8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM_A_CS L<3..0> 8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM_A_ODT<3..0> 8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A_A<15..0> 8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A_BA<2..0> 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A_RAS L 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A_CAS L 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_A_WE L 11 27 28 32
MEM_A_DO_BYTE0	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<7..0> 11 27
MEM_A_DO_BYTE1	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<15..8> 11 27
MEM_A_DO_BYTE2	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<23..16> 11 27
MEM_A_DO_BYTE3	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<31..24> 11 27
MEM_A_DO_BYTE4	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<39..32> 11 28
MEM_A_DO_BYTE5	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<47..40> 11 28
MEM_A_DO_BYTE6	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<55..48> 11 28
MEM_A_DO_BYTE7	MEM_50S	MEM_DATA	MEM_DATA	MEM_A_DO<63..56> 11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<0> 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<0> 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<1> 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<1> 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<2> 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<2> 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<3> 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<3> 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<4> 11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<4> 11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<5> 11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<5> 11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<6> 11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<6> 11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS P<7> 11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM_A_DQS N<7> 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM_B_CLK P<5..0> 8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM_B_CLK N<5..0> 8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM_B_CKE<3..0> 8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM_B_CS L<3..0> 8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM_B_ODT<3..0> 8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B_A<15..0> 8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B_BA<2..0> 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B_RAS L 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B_CAS L 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM_B_WE L 11 29 30 32
MEM_B_DO_BYTE0	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<7..0> 11 29
MEM_B_DO_BYTE1	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<15..8> 11 29
MEM_B_DO_BYTE2	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<23..16> 11 29
MEM_B_DO_BYTE3	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<31..24> 11 29
MEM_B_DO_BYTE4	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<39..32> 11 30
MEM_B_DO_BYTE5	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<47..40> 11 30
MEM_B_DO_BYTE6	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<55..48> 11 30
MEM_B_DO_BYTE7	MEM_50S	MEM_DATA	MEM_DATA	MEM_B_DO<63..56> 11 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<0> 11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<0> 11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<1> 11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<1> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<2> 11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<2> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<3> 11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<3> 11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<4> 11 30
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<4> 11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<5> 11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<5> 11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<6> 11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<6> 11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS P<7> 11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM_B_DQS N<7> 11 30
		MEM_FWR	PP1V5_S3RS0	7
		MEM_FWR	PP1V5_S3	7
		MEM_FWR	PP0V75_S3_MEM_VREFCA_A	9 27 28 29 30 31
		MEM_FWR	PP0V75_S3_MEM_VREFDO_A	9 27 28 29 30 31

SYNOPSIS: CONSTRAINTS PAGE TITLE SYNOPSIS: 06/2011

Memory Constraints

Apple Inc.

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PAGE: 101 OF 109 SHEET: 68 OF 75





LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_508	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_508	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	7
CLK_LPC	*	8 MIL	7

SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905\_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_508	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	7

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_508	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	7

SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905\_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	7

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	7

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	7

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3x_DIELECTRIC	7
CLK_PCIE	*	20 MIL	7

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	7
CLK_25M	*	=5x_DIELECTRIC	7

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
LPC_AD	LPC_50S	LPC	LPC AD<3..0>
LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L
LPC_RESET_L	LPC_50S	LPC	LPC RESET L
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC CLK33M LCPPLUS
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK
HDA_SYNC	HDA_50S	HDA	HDA_SYNC
HDA_RST_L	HDA_50S	HDA	HDA_RST_R L
HDA_RST_L	HDA_50S	HDA	HDA_RST_L
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K SUSCLK
SPT_CLK	SPT_55S	SPT	SPI_CLK R
SPT_CLK	SPT_55S	SPT	SPI_CLK
SPT_MOSI	SPT_55S	SPT	SPI_MOSI R
SPT_MOSI	SPT_55S	SPT	SPI_MOSI
SPT_MISO	SPT_55S	SPT	SPI_MISO
SPT_CS0	SPT_55S	SPT	SPI_CS0 R L
SPT_CS0	SPT_55S	SPT	SPI_CS0 L
SPT_ML0	SPT_55S	SPT	SPI_ML0 CLK
SPT_ML0	SPT_55S	SPT	SPI_ML0 MOSI
SPT_ML0	SPT_55S	SPT	SPI_ML0 MISO
SPT_ML0	SPT_55S	SPT	SPI_ML0 CS L
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D P
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C P
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R P
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R N
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R C P
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R C N
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D P
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C P
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R P
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R N
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D P
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D C P
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R P
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R N
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R C P
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R C N
PCIE_AP_D2R	PCIE_85D	PCIE	CONN PCIE AP D2R P
PCIE_AP_D2R	PCIE_85D	PCIE	CONN PCIE AP D2R N
PCIE_AP_R2D	PCIE_85D	PCIE	CONN PCIE AP R2D P
PCIE_AP_R2D	PCIE_85D	PCIE	CONN PCIE AP R2D N
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M P
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M N
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M ENET P
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M ENET N
MCP_PE1_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M AP P
MCP_PE1_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M AP N
MCP_PE2_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M FW P
MCP_PE2_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M FW N
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M EXCARD P
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M EXCARD N
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<1>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<2>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<5>
CPU_27P4S	CPU_COMP	CPU_COMP	TP_PCH_VSS_NCTF<7>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<9>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<9>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<11>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<12>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<15>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<17>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<19>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<21>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<22>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<25>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<27>
CPU_27P4S	CPU_COMP	CPU_COMP	PCH_VSS_NCTF<29>

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
DP_EXTM_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_C P<3..0>
DP_EXTM_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_C N<3..0>
DP_EXTM_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_P<3..0>
DP_EXTM_ML	DP_85D	DISPLAYPORT	DP_EXTM_ML_N<3..0>
DP_EXTM_AUXCH	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_C P
DP_EXTM_AUXCH	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_C N
DP_EXTM_AUXCH	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_P
DP_EXTM_AUXCH	DP_85D	DISPLAYPORT	DP_EXTM_AUXCH_N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F N<3..0>
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C P
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_P
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_N
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C P<3..0>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C N<3..0>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<2>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<1>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<0>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<2>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<1>
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<0>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<3>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<2>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<1>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<0>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<3>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<2>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<1>
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<0>
PCIE_T29_D2R_C	PCIE_85D	PCIE	PCIE_T29_D2R_C P<3..0>
PCIE_T29_D2R_C	PCIE_85D	PCIE	PCIE_T29_D2R_C N<3..0>
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R

SYNCH MASTERSET CONSTRAINTS  
PAGE TITLE

SYNCH DATUMS/REV/2011

PCH Constraints 2

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BRANCH: 103 OF 109  
PAGE: 70 OF 75



8

7

6

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L
	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>
	ENET_50S	ENET_CR_DATA	SDCONN_CMD
	ENET_50S	ENET_CR_DATA	SDCONN_CLK

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	FW_110D	FW_TP	FW_P0_TPA_P
	FW_110D	FW_TP	FW_P0_TPA_N
	FW_110D	FW_TP	FW_P0_TPB_P
	FW_110D	FW_TP	FW_P0_TPB_N
	FW_110D	FW_TP	FW_P1_TPA_P
	FW_110D	FW_TP	FW_P1_TPA_N
	FW_110D	FW_TP	FW_P1_TPB_P
	FW_110D	FW_TP	FW_P1_TPB_N
	Port 2 Not Used		

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Ethernet/FW Constraints		DRAWING NUMBER	051-8870	SIZE	D
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_558	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

DP/T29 Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=3x_DIELECTRIC	?	T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R233	DP_85D	DISPLAYPORT	DP_T29SNK0 ML C P<3..0> 8 34
R234	DP_85D	DISPLAYPORT	DP_T29SNK0 ML C N<3..0> 8 34
R235	DP_T29SNK0_MI	DP_85D	DP_T29SNK0 ML P<3..0> 34
R236	DP_T29SNK0_MI	DP_85D	DP_T29SNK0 ML N<3..0> 34
R237	DP_85D	DISPLAYPORT	DP_T29SNK0 AUXCH C P 8 34
R238	DP_85D	DISPLAYPORT	DP_T29SNK0 AUXCH C N 8 34
R239	DP_T29SNK0_AUXCH	DP_85D	DP_T29SNK0 AUXCH P 34
R240	DP_T29SNK0_AUXCH	DP_85D	DP_T29SNK0 AUXCH N 34
R241	DP_85D	DISPLAYPORT	DP_T29SNK1 ML C P<3..0> 8 34
R242	DP_85D	DISPLAYPORT	DP_T29SNK1 ML C N<3..0> 8 34
R243	DP_T29SNK1_MI	DP_85D	DP_T29SNK1 ML P<3..0> 34
R244	DP_T29SNK1_MI	DP_85D	DP_T29SNK1 ML N<3..0> 34
R245	DP_85D	DISPLAYPORT	DP_T29SNK1 AUXCH C P 8 34
R246	DP_85D	DISPLAYPORT	DP_T29SNK1 AUXCH C N 8 34
R247	DP_T29SNK1_AUXCH	DP_85D	DP_T29SNK1 AUXCH P 34
R248	DP_T29SNK1_AUXCH	DP_85D	DP_T29SNK1 AUXCH N 34
R249	T29_I2C_558	T29_I2C	I2C T29 SCL 34 44
R250	T29_I2C_558	T29_I2C	I2C T29 SDA 34 44
R251	T29_SPI_CLK	T29_SPI_558	T29_SPI_CLK 34
R252	T29_SPI_MOSTI	T29_SPI_558	T29_SPI MOSTI 34
R253	T29_SPI_MISO	T29_SPI_558	T29_SPI MISO 34
R254	T29_SPI_CS_L	T29_SPI_558	T29_SPI CS_L 34
R255	T29DP_80D	T29DP	T29_R2D C P<3..0> 8 34 64
R256	T29DP_80D	T29DP	T29_R2D C N<3..0> 8 34 64
R257	T29DP_80D	T29DP	T29_D2R P<3..0> 8 34 64
R258	T29DP_80D	T29DP	T29_D2R N<3..0> 8 34 64
R259	T29DP_80D	T29DP	T29_R2D P<0> 64
R260	T29DP_80D	T29DP	T29_R2D N<0> 64
R261	T29DP_80D	T29DP	T29_R2D P<1> 64
R262	T29DP_80D	T29DP	T29_R2D N<1> 64
R263	T29DP_80D	T29DP	T29_R2D C F P<1..0> 64
R264	T29DP_80D	T29DP	T29_R2D C F N<1..0> 64
R265	T29DP_80D	T29DP	T29_D2R C P<0> 64 65
R266	T29DP_80D	T29DP	T29_D2R C N<0> 64 65
R267	T29DP_80D	T29DP	T29_D2R C P<1> 64 65
R268	T29DP_80D	T29DP	T29_D2R C N<1> 64 65
R269	T29DP_80D	T29DP	T29DPA D2R1 AUXCH P 65
R270	T29DP_80D	T29DP	T29DPA D2R1 AUXCH N 65
R271	T29DP_80D	T29DP	DP_SDRVA ML C P<3..0> 64
R272	T29DP_80D	T29DP	DP_SDRVA ML C N<3..0> 64
R273	T29DP_80D	T29DP	DP_SDRVA ML R P<3..0> 64
R274	T29DP_80D	T29DP	DP_SDRVA ML R N<3..0> 64
R275	DP_SDRVA_MI_EVEN	T29DP_80D	DP_SDRVA ML P<0> 64
R276	DP_SDRVA_MI_EVEN	T29DP_80D	DP_SDRVA ML N<0> 64
R277	DP_SDRVA_MI_ODD	T29DP_80D	DP_SDRVA ML P<1> 64
R278	DP_SDRVA_MI_ODD	T29DP_80D	DP_SDRVA ML N<1> 64
R279	DP_SDRVA_MI_EVEN	T29DP_80D	DP_SDRVA ML P<2> 64
R280	DP_SDRVA_MI_EVEN	T29DP_80D	DP_SDRVA ML N<2> 64
R281	DP_SDRVA_MI_ODD	T29DP_80D	DP_SDRVA ML P<3> 64
R282	DP_SDRVA_MI_ODD	T29DP_80D	DP_SDRVA ML N<3> 64
R283	DP_SDRVA_AUXCH	T29DP_80D	DP_SDRVA AUXCH P 64
R284	DP_SDRVA_AUXCH	T29DP_80D	DP_SDRVA AUXCH N 64
R285	T29DP_80D	T29DP	DP_SDRVA AUXCH C P 64
R286	T29DP_80D	T29DP	DP_SDRVA AUXCH C N 64
R287	T29DPA_MI_ODD		T29DPA ML P<1> 64 65
R288	T29DPA_MI_ODD		T29DPA ML N<1> 64 65
R289	T29DPA_MI_ODD		T29DPA ML P<3> 64 65
R290	T29DPA_MI_ODD		T29DPA ML N<3> 64 65
R291	T29DP_80D	T29DP	T29DPA ML P<3..0> 64 65
R292	T29DP_80D	T29DP	T29DPA ML N<3..0> 64 65
R293	T29DP_80D	T29DP	T29DPA ML C P<3..0> 64 65
R294	T29DP_80D	T29DP	T29DPA ML C N<3..0> 64 65
R295	DP_A_EXT_AUXCH	T29DP_80D	DP_A_EXT_AUXCH P 64 65
R296	DP_A_EXT_AUXCH	T29DP_80D	DP_A_EXT_AUXCH N 64 65

T29 IC Net Properties

T29/DP Net Properties

T29 Constraints	
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8

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	44
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	44
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 44
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 44
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P	53
	1T01_DIFFPAIR		CHGR_CSI_N	53
CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P	53
	1T01_DIFFPAIR		CHGR_CSO_N	53

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SMC Constraints		DRAWING NUMBER	051-8870	SIZE	D
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		PAGE	106 OF 109		
		SHEET	73 OF 75		

8

7

6

5

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR		=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P20M	*	0.20 MM	1000
PWR_P20M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P20M
MEM_CMD	GND	*	GND_P20M
MEM_CTRL	GND	*	GND_P20M
MEM_DATA	GND	*	GND_P20M
MEM_DQS	GND	*	GND_P20M

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
MEM_72D	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
MEM_37S	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
MEM_85D	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
PCIE_85D	*	OVERWRITE	OVERWRITE	0.076 MM	10 MM	OVERWRITE	OVERWRITE
USB_85D	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
CPU_27P4S	TOP	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
CLK_PCIE_90D	TOP	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE

**A Memory Constraint Relaxations**

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOPTHM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

**A Memory Constraint Relaxations**

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOPTHM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

**K21/K78 Specific Net Properties**

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
ENET_100D	ENETCONN	ENETCONN	ENETCONN_P<3..0>
ENET_100D	ENETCONN	ENETCONN	ENETCONN_N<3..0>
SATA_90D	SATA	SATA	SATA_ODD_D2R_UF_P
SATA_90D	SATA	SATA	SATA_ODD_D2R_UF_N
SATA_90D	SATA	SATA	SATA_HDD_D2R_RDRVR_OUT_P
SATA_90D	SATA	SATA	SATA_HDD_D2R_RDRVR_OUT_N
SATA_90D	SATA	SATA	SATA_HDD_R2D_RDRVR_IN_P
SATA_90D	SATA	SATA	SATA_HDD_R2D_RDRVR_IN_N
SATA_90D	SATA	SATA	SATA_HDD_D2R_RDRVR_IN_P
SATA_90D	SATA	SATA	SATA_HDD_D2R_RDRVR_IN_N
SATA_90D	SATA	SATA	SATA_HDD_R2D_RDRVR_OUT_P
SATA_90D	SATA	SATA	SATA_HDD_R2D_RDRVR_OUT_N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THMSNS_D2_P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THMSNS_D2_N
CPU_THERMD	THERM_1T01_55S	THERM	CPU_THERMD_P
CPU_THERMD	THERM_1T01_55S	THERM	CPU_THERMD_N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29_THERMD_P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29_THERMD_N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29_MLBBOT_THMSNS_P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29_MLBBOT_THMSNS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_COMPUTING_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_COMPUTING_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_OTHER_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HS_OTHER_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVCCIOS0_CS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVCCIOS0_CS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS1_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS1_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS2_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS2_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS1G_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS1G_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISUM_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISUM_R_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISUMG_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISUMG_R_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISNS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	VCCSAS0_CS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	VCCSAS0_CS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISUMG_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP_ISUMG_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_CPU_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_CPU_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HDD_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HDD_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HDD_R_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_HDD_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_LCDBKLT_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_LCDBKLT_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_ODD_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_ODD_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_ODD_R_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_ODD_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_1V5_S3_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_1V5_S3_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_P1V8GPU_R_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_P1V8GPU_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_AIRPORT_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS_AIRPORT_P
LVDS_90D	LVDS	LVDS	LVDS_CONN_A_CLK_F_N
LVDS_90D	LVDS	LVDS	LVDS_CONN_A_CLK_F_P

**Audio Net Properties**

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_N
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_N

**K21/K78 Specific Net Properties**

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N
1T01_DIFFPAIR	1T01_DIFFPAIR	1T01_DIFFPAIR	CHGR_CSI_R_P
1T01_DIFFPAIR	1T01_DIFFPAIR	1T01_DIFFPAIR	CHGR_CSI_R_N
1T01_DIFFPAIR	1T01_DIFFPAIR	1T01_DIFFPAIR	CHGR_CSO_R_P
1T01_DIFFPAIR	1T01_DIFFPAIR	1T01_DIFFPAIR	CHGR_CSO_R_N
USB_EXTN	USB_85D	USB	USB2_EXTN_MUXED_P
USB_EXTN	USB_85D	USB	USB2_EXTN_MUXED_N
USB_EXTN	USB_85D	USB	USB2_LT1_P
USB_EXTN	USB_85D	USB	USB2_LT1_N
USB_85D	USB	USB	CONN_USB2_BT_P
USB_85D	USB	USB	CONN_USB2_BT_N
USB_85D	USB	USB	USB_LT2_P
USB_85D	USB	USB	USB_LT2_N
DP_85D	DISPLAYPORT	DP_85D	DP_IG_AUX_CH_C_P
DP_85D	DISPLAYPORT	DP_85D	DP_IG_AUX_CH_C_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_SUB_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_SUB_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_L_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_L_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_R_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_R_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_N_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_P_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO1_N_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO1_P_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_N_L
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_P_L
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INL_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INL_N
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N
USB_85D	USB	USB	USB_TPAD_R_P
USB_85D	USB	USB	USB_TPAD_R_N
SB_POWER	SB_POWER	SB_POWER	PP3V3_S5
SB_POWER	SB_POWER	SB_POWER	PP3V3_S0
GND	GND	GND	GND

**Misc Net Properties**

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
USB_EXTN	USB_85D	USB	USB_EXTN_MUXED_P
USB_EXTN	USB_85D	USB	USB_EXTN_MUXED_N
USB_EXTN	USB_85D	USB	USB_LT1_P
USB_EXTN	USB_85D	USB	USB_LT1_N
USB_TPAD	USB_85D	USB	USB_TPAD_CONN_P
USB_TPAD	USB_85D	USB	USB_TPAD_CONN_N
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R
SMB_55S	SMB	SMB	I2C_TCON_SCL
SMB_55S	SMB	SMB	I2C_TCON_SDA
SMB_55S	SMB	SMB	I2C_TCON_SCL_CONN
SMB_55S	SMB	SMB	I2C_TCON_SDA_CONN

Project Specific Constraints

Apple Inc.

DRAWING NUMBER: 051-8870

REVISION: 3.13.0

108 OF 109

74 OF 75

K901 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL. OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4, ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4, ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM

NOTE: 110\_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4, ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM

NOTE: These are Intel recommended impedances for PEG, unused on K901.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP, BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM


NOTE: 85\_DIFF\_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90\_DIFF\_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100\_DIFF\_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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