1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-04-18

SCHEM,EVT,MLB,K21

04/18/11

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8870	1	SCHEM,MLB,K21	SCH	CRITICAL	
820-3023	1	PCBF,MLB,K21	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Apr 18 17:52:39 2011

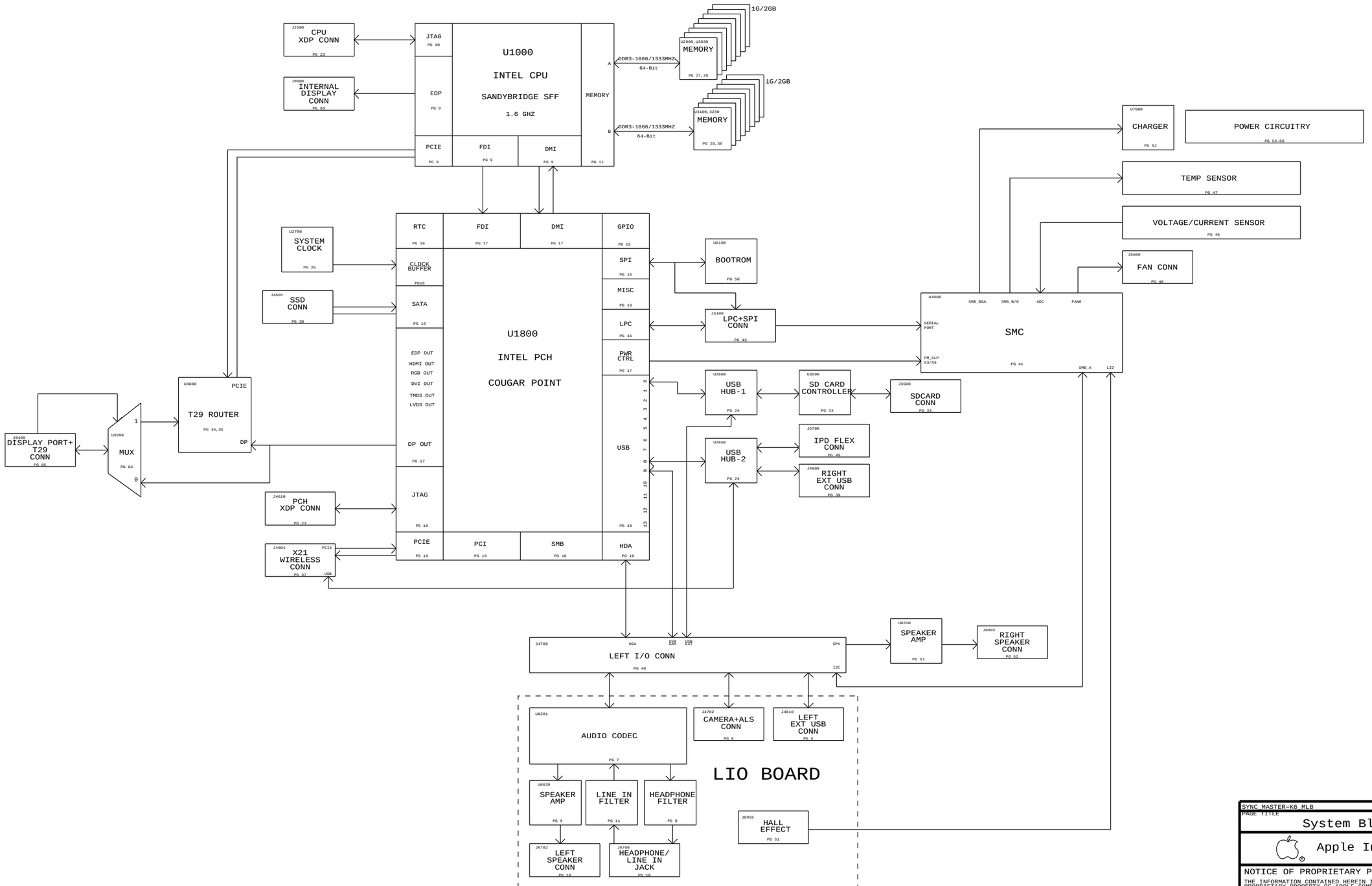
PRODUCT SAFETY REQUIREMENTS:

PCB,UL RECOGNIZED, MIN. 130-C TEMP RATING AND V-O FLAME RATING PER UL 796 & UL 94
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP RATING AND V-O FLAME RATING

DRAWING TITLE: SCHEM,MOCKUP,MLB,K21

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 1 OF 109
SHEET: 1 OF 75



SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

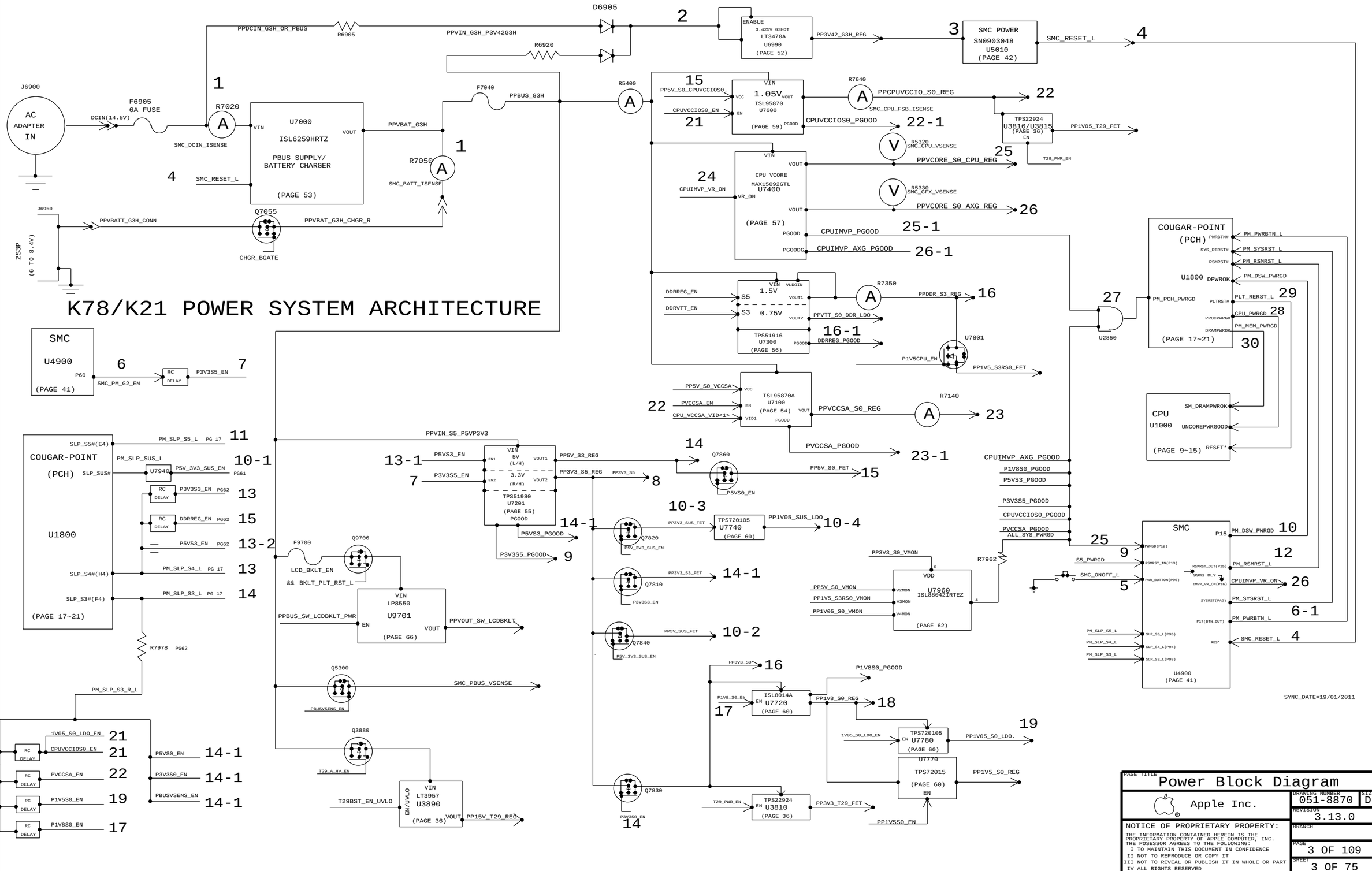
REVISION 3.13.0

BRANCH

PAGE 2 OF 109

SHEET 2 OF 75

K78/K21 POWER SYSTEM ARCHITECTURE



PAGE TITLE	Power Block Diagram
	Apple Inc.
DRAWING NUMBER	051-8870
SIZE	D
REVISION	3.13.0
BRANCH	
PAGE	3 OF 109
SHEET	3 OF 75

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2684	K21i MLB DEVELOPMENT BOM	K21_DEVEL:ENG
607-8041	CMN PTS,PCBA,MLB,K21	K21_COMMON
639-2553	PCBA,MLB,1.8GHZ,HY 2GB,K21	K21_CMNPTS,EEEE:DP1F,CPU:1.8GHZ,DDR3:HYNIX_2GB
639-2554	PCBA,MLB,1.7GHZ,SA 4GB,K21	K21_CMNPTS,EEEE:DP1G,CPU:1.7GHZ,DDR3:SAMSUNG_4GB
639-2558	PCBA,MLB,1.8GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1H,CPU:1.8GHZ,DDR3:ELPIDA_4GB
639-2549	PCBA,MLB,1.7GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1J,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-2555	PCBA,MLB,1.8GHZ,HY 4GB,K21	K21_CMNPTS,EEEE:DP1K,CPU:1.8GHZ,DDR3:HYNIX_4GB
639-2557	PCBA,MLB,1.8GHZ,SA 4GB,K21	K21_CMNPTS,EEEE:DP1L,CPU:1.8GHZ,DDR3:SAMSUNG_4GB
639-2548	PCBA,MLB,1.7GHZ,HY 2GB,K21	K21_CMNPTS,EEEE:DP1M,CPU:1.7GHZ,DDR3:HYNIX_2GB
639-2550	PCBA,MLB,1.8GHZ,MI 2GB,K21	K21_CMNPTS,EEEE:DP1N,CPU:1.8GHZ,DDR3:MICRON_2GB
639-2551	PCBA,MLB,1.7GHZ,HY 4GB,K21	K21_CMNPTS,EEEE:DP1P,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-2552	PCBA,MLB,1.7GHZ,SA 2GB,K21	K21_CMNPTS,EEEE:DP1Q,CPU:1.7GHZ,DDR3:SAMSUNG_2GB
639-2556	PCBA,MLB,1.8GHZ,SA 2GB,K21	K21_CMNPTS,EEEE:DP1R,CPU:1.8GHZ,DDR3:SAMSUNG_2GB
639-2559	PCBA,MLB,1.7GHZ,MI 2GB,K21	K21_CMNPTS,EEEE:DP1T,CPU:1.7GHZ,DDR3:MICRON_2GB

Bar Code Labels / EEEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,LIO,K99	[EEEE_DP1F]	CRITICAL	EEEE:DP1F
825-7563	1	LABEL,LIO,K99	[EEEE_DP1G]	CRITICAL	EEEE:DP1G
825-7563	1	LABEL,LIO,K99	[EEEE_DP1H]	CRITICAL	EEEE:DP1H
825-7563	1	LABEL,LIO,K99	[EEEE_DP1J]	CRITICAL	EEEE:DP1J
825-7563	1	LABEL,LIO,K99	[EEEE_DP1K]	CRITICAL	EEEE:DP1K
825-7563	1	LABEL,LIO,K99	[EEEE_DP1L]	CRITICAL	EEEE:DP1L
825-7563	1	LABEL,LIO,K99	[EEEE_DP1M]	CRITICAL	EEEE:DP1M
825-7563	1	LABEL,LIO,K99	[EEEE_DP1N]	CRITICAL	EEEE:DP1N
825-7563	1	LABEL,LIO,K99	[EEEE_DP1P]	CRITICAL	EEEE:DP1P
825-7563	1	LABEL,LIO,K99	[EEEE_DP1Q]	CRITICAL	EEEE:DP1Q
825-7563	1	LABEL,LIO,K99	[EEEE_DP1R]	CRITICAL	EEEE:DP1R
825-7563	1	LABEL,LIO,K99	[EEEE_DP1T]	CRITICAL	EEEE:DP1T

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-2684	1	K21 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-8041	1	CMN PTS,PCBA,MLB,K21	CMNPTS	CRITICAL	K21_CMNPTS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 4 OF 109

SHEET 4 OF 75

K21 BOM GROUPS

BOM GROUP	BOM OPTIONS
K21_COMMON	ALTERNATE,COMMON,K21_MISC,K21_DEBUG:ENG,K21_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP,PCH:B3
K21_MISC	CPUMEM_50,HUB1_2NONREM,HUB2_2NONREM,T29:YES,SDRV12C:MCU,SDRV_PD,KB_BL
K21_PROGPARTS	BOOTROM_PROG,SMC_PROG,T29ROM:PROG,T29MCU:PROG
K21_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,VREFMRGN,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
K21_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K21_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K21_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT
K21_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0550	1	IC,EEPROM,SERIAL,SPI,1Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341T0352	1	IC,T29-ROM,K21	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0353	1	IC,T29-MCU,K21	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC,SMC,RENESAS,H8S/2117RP,9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341T0348	1	IC,SMC,K21	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Numonyx	U6100	CRITICAL	BOOTROM_BLANK
341T0349	1	IC,EFI ROM,K21 K78	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
377S0107	377S0066		ALL	ONsemi alt to Semtech
138S0676	138S0691		ALL	Murata alt to Samsung
371S0679	371S0652		ALL	NXP alt to NXP
138S0679	138S0678		ALL	Murata/Samsung to Taiyo
138S0671	138S0673		ALL	Taiyo alt to Murata
337S4092	337S4100		ALL	EARLY 1.5GHZ CPU SAMPLES
337S4093	337S4101		ALL	EARLY 1.4GHZ CPU SAMPLES
353S3312	353S3055		ALL	NXP alt to Pericom
376S0790	376S0928		ALL	TI alt to Fairchild
128S0333	128S0294		ALL	Sanyo alt for Sanyo/Frederick
152S1462	152S1295		ALL	Toko alt for NEC inductor
104S0035	104S0011		ALL	Panasonic alt to Cyntec
152S1085	152S1307		ALL	Toko alt for Cyntec
514-0744	998-3941		ALL	Old J9400 alt to New J9400
376S0874	376S0895		ALL	FDMC0202S alt to RJK03E0DNS
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
338S0721	338S0923		ALL	SMSC USX2061 alt to USB2513B
152S1493	152S1300		ALL	Coilcraft alt to Murata

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4121	1	SNB,QAYS,QS,J1,1.8,17W,2+2,1.20,4M,BGA	U1000	CRITICAL	CPU:1.8GHZ
337S4119	1	SNB,QAYM,QS,J1,1.7,17W,2+2,1.20,3M,BGA	U1000	CRITICAL	CPU:1.7GHZ
337S4101	1	SNB,QAM1,QS,J1,1.6,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S4100	1	SNB,QAM2,QS,J1,1.5,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ
337S4099	1	SNB,QAM3,QS,J1,1.4,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S4098	1	SNB,QALV,QS,J1,1.3,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ
337S4080	1	COUGAR POINT,SLHAG,PRQ,BD82QS67	U1800	CRITICAL	PCH:B2
337S4091	1	COUGAR POINT,B3,SLJ4K,PRQ,BD82QS67	U1800	CRITICAL	PCH:B3
338S0976	1	IC,T29 Eagle Ridge,192 FCBGA,8x9MM	U3600	CRITICAL	T29:YES
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
353s2929	1	IC,ISL6259,BATCHARGER,3%,4X4MM,QFN28	U7000	CRITICAL	

PD Module Parts

806-2333	1	K21, T29 Fence	T29FENCE	CRITICAL	
806-2356	1	K21, T29 Can	T29CAN	CRITICAL	NOSTUFF
806-2347	1	K21, T29 Filter Can	T29FILTERCAN	CRITICAL	
806-2376	1	K78, mDP Can	MDPCAN	CRITICAL	
806-2377	1	K78, mDP Spring	MDPSPRING	CRITICAL	NOSTUFF

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 5 OF 109

SHEET 5 OF 75

Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F	37	(Need 5 TPs)
TRUE	WIFI_EVENT_L	37 41	
TRUE	PCIE_AP_R2D_N	37 70	
TRUE	PCIE_AP_R2D_P	37 70	
TRUE	PCIE_CLK100M_AP_N	16 37 70	
TRUE	PCIE_CLK100M_AP_P	16 37 70	
TRUE	USB_BT_P	24 37 69	
TRUE	USB_BT_N	24 37 69	
TRUE	PCIE_AP_D2R_P	16 37 70	
TRUE	PCIE_AP_D2R_N	16 37 70	
TRUE	PCIE_WAKE_L	17 37	
TRUE	AP_RESET_CONN_L	37	
TRUE	AP_CLKREQ_O_L	37	
TRUE	=PP3V3_S3_BT	7 37	

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

TRUE	PP3V3_S0_HDD_R	38	(Need 5 TPs)
TRUE	SATA_HDD_D2R_C_P	38 69	
TRUE	SATA_HDD_D2R_C_N	38 69	
TRUE	SATA_HDD_R2D_N	38 69	
TRUE	SATA_HDD_R2D_P	38 69	
TRUE	SMC_HDD_OOB_TEMP_CONN	38	
TRUE	SMC_HDD_TEMP_CTL_CONN	38	

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	7 40	
TRUE	=PP3V3_S0_AUDIO	7 40	(Need 2 TPs)
TRUE	=PP3V3R1V5_S0_AUDIO	7 40	
TRUE	SYS_ONEWIRE	40 41	
TRUE	SMC_BC_ACOK	40 41 42	
TRUE	=USB_PWR_EN	39 40 62	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	=I2C_LIO_SDA	40 44	
TRUE	=I2C_LIO_SCL	40 44	
TRUE	=I2C_MIKEY_SCL	40 44	
TRUE	=I2C_MIKEY_SDA	40 44	
TRUE	AUD_IPHS_SWITCH_EN	19 40	
TRUE	AUD_IP_PERIPHERAL_DET	18 40	
TRUE	AUD_I2C_INT_L	18 40	
TRUE	AUD_GPIO_3	40 51	
TRUE	SPKRAMP_INR_N	40 51 74	
TRUE	SPKRAMP_INR_P	40 51 74	
TRUE	USB_EXTD_N	24 40 69	
TRUE	USB_EXTD_P	24 40 69	
TRUE	USB_CAMERA_N	18 40 69	
TRUE	USB_CAMERA_P	18 40 69	
TRUE	HDA_SDOUT	16 40 70	
TRUE	HDA_BIT_CLK	16 40 70	
TRUE	HDA_SDIN0	16 40 70	
TRUE	USB_EXTD_OC_L	24 40	
TRUE	HDA_RST_L	16 40 70	
TRUE	HDA_SYNC	16 40 70	

(Need to add 5 GND TPs)

J4800: SD Card Connector

FUNC_TEST

TRUE	PP3V3_SW_SD_PWR	33
TRUE	SD_CLK	33
TRUE	SD_CMD	33
TRUE	SD_D<7..0>	33
TRUE	SD_CD_L	33
TRUE	SD_WP	33

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	7 43
TRUE	=PP5V_S0_LPCPLUS	7 43
TRUE	LPC_AD<3..0>	16 41 43 70
TRUE	SPI_ALT_MOSI	43
TRUE	SPI_ALT_MISO	43
TRUE	LPC_FRAME_L	16 41 43 70
TRUE	PM_CLKRUN_L	17 41 43
TRUE	SMC_TMS	41 42 43
TRUE	LPCPLUS_RESET_L	25 43
TRUE	SMC_TDO	41 42 43
TRUE	SMC_TRST_L	41 43
TRUE	SMC_MD1	41 43
TRUE	SMC_TX_L	39 41 42 43
TRUE	LPC_CLK33M_LPCPLUS	25 43 70
TRUE	SPIROM_USE_MLB	19 43 50
TRUE	SPI_ALT_CLK	43
TRUE	SPI_ALT_CS_L	43
TRUE	LPC_SERIRQ	16 41 43
TRUE	LPC_PWRDWN_L	17 41 43
TRUE	SMC_TDI	41 42 43
TRUE	SMC_TCK	41 42 43
TRUE	SMC_RESET_L	41 42 43 53
TRUE	SMC_NMI	41 43
TRUE	SMC_RX_L	39 41 42 43
TRUE	LPCPLUS_GPIO	19 43

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	7 48	
TRUE	FAN_RT_TACH	48	
TRUE	FAN_RT_PWM	48	

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	PP3V3_TPAD_CONN	49	
TRUE	PP5V_TPAD_FILT	49	
TRUE	=PP3V42_G3H_TPAD	7 49	
TRUE	USB_TPAD_CONN_P	49 74	
TRUE	USB_TPAD_CONN_N	49 74	
TRUE	=I2C_TPAD_SDA	44 49	
TRUE	=I2C_TPAD_SCL	44 49	
TRUE	SMC_ONOFF_L	41 42 49	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	SMC_TPAD_RST_L	42 49	
TRUE	SMC_PME_S4_WAKE_L	41 42 49	

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	7 52	(Need 6 TPs)
TRUE	=PP5V_S3_LIO_CONN	7 52	

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_R_P_OUT	51 52 74	
TRUE	SPKRAMP_R_N_OUT	51 52 74	

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	52 53	(Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	44 52	
TRUE	=SMBUS_BATT_SDA	44 52	
TRUE	SYS_DETECT_L	52	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	63 66	(Need 2 TPs)
TRUE	PP3V3_SW_LCD	63	(Need 2 TPs)
TRUE	I2C_TCON_SDA_R	63	
TRUE	I2C_TCON_SCL_R	63	
TRUE	LED_RETURN_6	63 66	
TRUE	LED_RETURN_5	63 66	
TRUE	LED_RETURN_4	63 66	
TRUE	LED_RETURN_3	63 66	
TRUE	LED_RETURN_2	63 66	
TRUE	LED_RETURN_1	63 66	
TRUE	DP_INT_HPD_CONN	63	
TRUE	DP_INT_AUX_CH_C_N	63 70	
TRUE	DP_INT_AUX_CH_C_P	63 70	
TRUE	DP_INT_ML_F_P<0>	63 70	
TRUE	DP_INT_ML_F_N<0>	63 70	
TRUE	DP_INT_ML_F_P<1>	63 70	
TRUE	DP_INT_ML_F_N<1>	63 70	

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	7 52	
TRUE	PPVIN_SW_T29BST	7 36	
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7	
TRUE	PPDCIN_G3H	7	
TRUE	PP3V42_G3H	7	
TRUE	PPVRTC_G3H	7	
TRUE	PP5V_S5	7	
TRUE	PP5V_SUS	7	
TRUE	PP3V3_S5	7 74	
TRUE	PP3V3_SUS	7	
TRUE	PP3V3_S3	7	
TRUE	PP1V8_S0	7	
TRUE	PP3V3_S0	7 74	
TRUE	PP1V5_S3	7 68	
TRUE	PP1V5_S3RS0	7 68	
TRUE	PP1V5_S0	7	
TRUE	PP1V05_S0	7	
TRUE	PPVTTDDR_S3	7	
TRUE	PP0V75_S0_DDRVTT	7	
TRUE	PPVCCSA_S0_CPU	7	
TRUE	PP1V05_SUS	7	
TRUE	PP15V_T29	7	
TRUE	PP3V3_T29	7	
TRUE	PP1V05_T29	7 36	
TRUE	PP1V05_S0_PCH_VCCADPLL	7	
TRUE	PPVCORE_S0_CPU	7	
TRUE	PPVCORE_S0_AXG	7	
TRUE	PP1V5_S3_CPU_VCCDQ	7	
TRUE	PP1V05_S0_CPU_VCCPQE	7	
TRUE	PP1V8_S0_CPU_VCCPLL_R	7	

(Need to add 27 GND TPs)

J5715: KB BKLT CONNECTOR

FUNC_TEST

TRUE	KBDLED_FB	49	
TRUE	KBDLED_ANODE	49	

(Need to add 2 GND TP)

NO_TEST Nets

NO_TEST

17	TP_CRT_IG_BLUE	TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	TRUE	NC_CRT_IG_VSYNC
	TP_LVDS_IG_CTRL_CLK	TRUE	NC_LVDS_IG_CTRL_CLK
	TP_LVDS_IG_CTRL_DATA	TRUE	NC_LVDS_IG_CTRL_DATA
	TP_PCH_LVDS_VBG	TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	TRUE	NC_PCI_CLK33M_OUT3
16	TP_CLINK_CLK	TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	TRUE	NC_PCIE_CLK100M_PEBP

J6930		TRUE	XDP_PCH_AP_PWR_EN
J6931		TRUE	XDP_PCH_USB_HUB_SOFT_RST_L 23
J6932		TRUE	XDP_PCH_SDCONN_STATE_RST_L 23
J6933		TRUE	XDP_PCH_ENET_PWR_EN 23
J6934		TRUE	XDP_PCH_SDCONN_DET_L 23
J6935		TRUE	XDP_PCH_S5_PWRGD 23
J6936		TRUE	XDP_PCH_PWRBTN_L 23
J6937		TRUE	XDP_PCH_ISOLATE_CPU_MEM_L 23
J6938		TRUE	XDP_FW_CLKREQ_L
J6939		TRUE	XDP_AP_CLKREQ_L 23
J6940		TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN 23

17	TP_SDVO_TVCLKINN	TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	TRUE	NC_SDVO_INTP
23	TP_XDP_PCH_OBSFN_A<0..1>	TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDPPCH_HOOK2	TRUE	NC_TP_XDPPCH_HOOK2
23	TP_XDPPCH_HOOK3	TRUE	NC_TP_XDPPCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	TRUE	NC_TP_XDP_PCH_HOOK5
16	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

	NC_EDP_TXP<0..3>	TRUE	TP_EDP_TX_P<0..3> 9
	NC_EDP_TXN<0..3>	TRUE	TP_EDP_TX_N<0..3> 9
	NC_EDP_AUXP	TRUE	TP_EDP_AUX_P
	NC_EDP_AUXN	TRUE	TP_EDP_AUX_N
	NC_CPU_THERMDA	TRUE	TP_CPU_THERMDA
	NC_CPU_THERMDC	TRUE	TP_CPU_THERMDC
	NC_CPU_RSVD<30..45>	TRUE	TP_CPU_RSVD<30..45>
	NC_CPU_RSVD<8..27>	TRUE	TP_CPU_RSVD<8..27>
	NC_PEG_R2D_CP<15..4>	TRUE	=PEG_R2D_C_P<15..4> 9
	NC_PEG_R2D_CN<15..4>	TRUE	=PEG_R2D_C_N<15..4> 9
	NC_PEG_D2RP<15..4>	TRUE	=PEG_D2R_P<15..4> 9
	NC_PEG_D2RN<15..4>	TRUE	=PEG_D2R_N<15..4> 9

16	TP_PCIE_CLK100M_PE4N	TRUE	NC_PCIE_CLK100M_PE4N
16	TP_PCIE_CLK100M_PE4P	TRUE	NC_PCIE_CLK100M_PE4P
16	TP_PCIE_CLK100M_PE5N	TRUE	NC_PCIE_CLK100M_PE5N
16	TP_PCIE_CLK100M_PE5P	TRUE	NC_PCIE_CLK100M_PE5P
16	TP_PCIE_CLK100M_PE6N	TRUE	NC_PCIE_CLK100M_PE6N
16	TP_PCIE_CLK100M_PE6P	TRUE	NC_PCIE_CLK100M_PE6P
16	TP_PCIE_CLK100M_PE7N	TRUE	NC_PCIE_CLK100M_PE7N
16	TP_PCIE_CLK100M_PE7P	TRUE	NC_PCIE_CLK100M_PE7P
	TP_PSOC_P1_3	TRUE	NC_PSOC_P1_3
16	TP_SATA_B_D2RN	TRUE	NC_SATA_B_D2RN
16	TP_SATA_B_D2RP	TRUE	NC_SATA_B_D2RP
16	TP_SATA_B_R2D_CN	TRUE	NC_SATA_B_R2D_CN
16	TP_SATA_B_R2D_CP	TRUE	NC_SATA_B_R2D_CP
16	TP_SATA_D_D2RN	TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	TRUE	NC_SATA_F_R2D_CP

	TP_PCH_TP18	TRUE	NC_PCH_TP18
	TP_PCH_TP17	TRUE	NC_PCH_TP17
	TP_PCH_TP16	TRUE	NC_PCH_TP16
	TP_PCH_TP15	TRUE	NC_PCH_TP15
	TP_PCH_TP14	TRUE	NC_PCH_TP14
	TP_PCH_TP13	TRUE	NC_PCH_TP13
	TP_PCH_TP12	TRUE	NC_PCH_TP12
	TP_PCH_TP10	TRUE	NC_PCH_TP10
	TP_PCH_TP9	TRUE	NC_PCH_TP9
	TP_PCH_TP8	TRUE	NC_PCH_TP8
	TP_PCH_TP7	TRUE	NC_PCH_TP7
	TP_PCH_TP6	TRUE	NC_PCH_TP6
	TP_PCH_TP5	TRUE	NC_PCH_TP5
	TP_PCH_TP4	TRUE	NC_PCH_TP4
	TP_PCH_TP3	TRUE	NC_PCH_TP3
	TP_PCH_TP2	TRUE	NC_PCH_TP2
	TP_PCH_TP1	TRUE	NC_PCH_TP1

J6580	PCH_VSS_NCTF<1>	70	
J6581	PCH_VSS_NCTF<2>	70	
J6582	PCH_VSS_NCTF<5>	70	
J6583	PCH_VSS_NCTF<9>	70	
J6584	PCH_VSS_NCTF<11>	70	
J6585	PCH_VSS_NCTF<12>	70	
J6586	PCH_VSS_NCTF<15>	70	
J6587	PCH_VSS_NCTF<17>	70	
J6588	PCH_VSS_NCTF<19>	6 70	
J6589	PCH_VSS_NCTF<19>	6 70	
J6590	PCH_VSS_NCTF<21>	70	
J6591	PCH_VSS_NCTF<25>	70	
J6592	PCH_VSS_NCTF<27>	70	
J6593	PCH_VSS_NCTF<29>	70	

8	TP_LVDS_IG_B_CLKN	TRUE	NC_LVDS_IG_B_CLKN
8	TP_LVDS_IG_B_CLKP	TRUE	NC_LVDS_IG_B_CLKP
	TP_LVDS_IG_BKL_PWM	TRUE	NC_LVDS_IG_BKL_PWM
	SMC_BS_ALRT_L	TRUE	NC_SMC_BS_ALRT_L

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE

Functional Test / No Test

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 7 OF 109

SHEET 6 OF 75

"G3Hot" (Always-Present) Rails

53 =PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_G0_LCDBKLT 66
=PPBUS_G0_VSENSE 45
=PPVIN_SW_T29BST 8 36
=PPVIN_S5_HS_COMPUTING_ISNS_R 46
=PPVIN_S5_P5VP3V3 55
6 52

36 6 PPVIN_SW_T29BST
VOLTAGE=12.6V

46 =PPVIN_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUIMVP 57 58
=PPVIN_S3_DDRREG 56
=PPVIN_S0_CPUVCCIOS0 59
=PPVIN_S0_VCCSAS0 54
=PPVIN_S0_CPUAXG 58
6

52 6 =PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 53
=PPDCIN_S5_VSENSE 45

52 =PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V3_S5_LPCPLUS 6 43
=PP3V3_S5_SMC 41 42
=PP3V42_G3H_CHGR 53
=PP3V42_G3H_PWRCTL 62
=PP3V42_G3H_SMBUS_SMC_BSA 44
=PP3V42_G3H_SMCUSBMUX 39
=PP3V42_G3H_TPAD 6 49
=PPVIN_S5_SMCVREF 42
=PPVBAT_G3_SYSCLK 25
=PP3V42_G3H_ONEWIRE 6 40
6

25 =PPVRTC_G3_OUT
PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
=PPVRTC_G3_PCH 16 17 20
6

5V Rails

55 =PP5V_S5_LDO
PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S5_P1V5DDRFET 61
=PP5V_S5_P5VSUSFET 61
=PP5V_S5_TPAD 49
6

61 =PP5V_SUS_FET
PP5V_SUS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP5V_SUS_PCH 22
6

55 =PP5V_S3_REG
PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_AUDIO_AMP 51
=PP5V_S3_DDRREG 56
=PP5V_S3_MEMRESET 26
=PP5V_S3_P5VS0FET 61
=PP5V_S3_RTUSB 39
=PP5V_S3_LIO_CONN 6 52
6

61 =PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_BKL 66
=PP5V_S0_CPUIMVP 57
=PP5V_S0_CPUVCCIOS0 59
=PP5V_S0_FAN 6 48
=PP5V_S0_LPCPLUS 6 43
=PP5V_S0_VCCSA 54
=PP5V_S0_PCH 22
=PP5V_S0_VMON 62
=PP5V_S0_KBDLED 49
6

3.3V Rails

55 =PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S5_XDP 23
=PP3V3_S0_P3V3S0FET 61
=PP3V3_S3_P3V3S3FET 61
=PP3V3_S5_CPU_VCCDDR 26
=PP3V3_S5_LCD 63
=PP3V3_S5_PCH 17 19
=PP3V3_S5_PCHPWRGD 25
=PP3V3_S5_SMCBATLOW 42
=PP3V3_S5_ROM 50
=PP3V3_S5_USB_RESET 24
=PP3V3_S5_PCH_VCCDSW 20 22
=PP3V3_S5_SYSCLK 25
=PP3V3_S5_VMON 62
=PP3V3_S5_PWRCTL 62
=PP3V3_S5_PCH_VCC_SPI 20 22
=PP3V3_S5_P3V3SUSFET 61
=PP3V3_S5_TPAD 49
=PP3V3_S4_DPAPWRSW 65
=PP3V3_S4_SMC 42
6 74

61 =PP3V3_SUS_FET
PP3V3_SUS
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_SUS_PCH_VCCSUS_USB 20 22
=PP3V3_SUS_PCH_VCCSUS_GPIO 20 22
=PP3V3_SUS_PCH_VCCSUS 20
=PP3V3_SUS_GPIO 16 17 18 19
=PP3V3_SUS_PCH 22
=PP3V3_SUS_PWRCTL 62
=PP3V3_SUS_P1V05SUSLDO 60
=PP3V3_SUS_SMC 42
6

61 =PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_S3_BT 6 37
=PP3V3_S3_CARDREADER 33
=PP3V3_S3_MEMRESET 26
=PP3V3_S3_SMBUS_SMC_A_S3 44
=PP3V3_S3_SMBUS_SMC_MGMT 44
=PP3V3_S3_USB_HUB 8 24
=PP3V3_S3_USB_RESET 24
=PP3V3_S3_VREFMRGN 31
=PP3V3_S3_WLAN 37
=PP3V3_S3_WLANISNS 46
=PP3V3_S3_BMON_ISNS 46
=PP3V3_S3_PCH_GPIO 18 19
=PP3V3_S3_1V5S3ISNS 46
=PP3V3_S3_DBGLEDS 52
6

61 =PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
=PP3V3_S0_CPUVCCIOISNS 45
=PP3V3_S0_AUDIO 6 40
=PP3V3_S0_BKL_VDDIO 66
=PP3V3_S0_HS_COMPUTING_ISNS 46
=PP3V3_S0_CPUTHMSNS 47
=PP3V3_S0_CPU_VCCIO_SEL 12
=PP3V3_S0_DP_DDC 8
=PP3V3_S0_FAN 48
=PP3V3_S0_P3V3T29FET 36
=PP3V3_S0_P1V8S0 60
=PP3V3_S0_PCH 16 19 22
=PP3V3_S0_PCH_GPIO 18
=PP3V3_S0_PCH_VCC3_3_CLK 22
=PP3V3_S0_PCH_VCC3_3_GPIO 20 22
=PP3V3_S0_PCH_VCC3_3_HVCMOS 20 22
=PP3V3_S0_PCH_VCC3_3_PCI 20 22
=PP3V3_S0_PCH_VCC3_3_SATA 20 22
=PP3V3_S0_PCH_VCCADAC 22
=PP3V3_S0_PCH_STRAPS 16 17 19
=PP3V3_S0_PWRCTL 62
=PP3V3_S0_RSTBUF 25
=PP3V3_S0_SB_PM 25
=PP3V3_S0_SMBUS_PCH 44
=PP3V3_S0_SMBUS_SMC_0_S0 44
=PP3V3_S0_SMBUS_SMC_B_S0 44
=PP3V3_S0_SMC 42
=PP3V3_S0_HDD 38
=PP3V3_S0_HDDISNS 46
=PP3V3_S0_VMON 62
=PP3V3_S0_P1V5S0 60
=PP3V3_S0_T29PWRCTL 36
=PP3V3_S0_DPSDRVA 64
=PP3V3_S0_P1V05S0LDO 60
=PP3V3_S0_IMVPISNS 45
=PP3V3_S0_XDP 23
=PP3V3_S0_T29I2C 44
=PP3V3_S0_BKLTISNS 46
=PP3V3_S0_SYSCLKGEN 25
6 74

1.8V/1.5V/1.2V/1.05V Rails

60 =PP1V8_S0_REG
2A max supply
PP1V8_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S0_CPU_VCCPLL 14
=PP1V8_S0_PCH_VCC_DFTERM 18 20 22
=PP1V8_S0_P1V05S0LDO 60
=PP1V8R1V5_S0_PCH_VCCVRM 20
=PPVDDIO_S0_SBCLK 25
=PP1V8_S0_P1V5S0 60
6

56 =PPDDR_S3_REG
PP1V5_S3
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_MEMRESET 26
=PP1V5_S3_MEM_A 27 28 32
=PP1V5_S3_MEM_B 29 30 32
=PP1V5_S3_P1V5S3RS0_FET 61
=PPVIN_S0_DDRREG_LDO 56
6 68

61 =PP1V5_S3RS0_FET
PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_CPU_VCCDDR 10 12 15 26
=PP1V5_S3RS0_VMON 62
6 68

60 =PP1V5_S0_REG
PP1V5_S0
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP3V3R1V5_S0_AUDIO 6 40
=PP3V3R1V5_S0_PCH_VCCSUSHDA 16 20 22
6

56 31 =PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE
6

56 =PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A 32
=PP0V75_S0_MEM_VTT_B 32
=PPVTT_S0_VTTCLAMP 26
6

54 =PPVCCSA_S0_REG
PPVCCSA_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVCCSA_S0_CPU 12 15
6

60 =PP1V05_SUS_LDO
PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG 23
6

59 =PPCPUVCCIO_S0_REG
? mA
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCCIO_PLLPCIE 20
=PP1V05_S0_CPU_VCCIO 9 10 12 14
=PP1V05_S0_PCH 16 22
=PP1V05_S0_PCH_VCCIO 20 22
=PP1V05_S0_PCH_VCCIO_PCIE 17
=PP1V05_S0_PCH_VCCIO_SATA 16 20 22
=PP1V05_S0_PCH_VCCASW 20 22
=PP1V05_S0_PCH_VCCIO_USB 20 22
=PP1V05_S0_PCH_VCC_CORE 20 22
=PP1V05_S0_VMON 62
=PP1V05_S0_PCH_VCCIO_CLK 20 22
=PPVCCIO_S0_CPUIMVP 57
=PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
=PP1V05_S0_PCH_VCCSSC 20 22
=PP1V05_S0_PCH_V_PROC_IO 20 22
=PP1V05_S0_PCH_VCCIO_PLLUSB 20
=PP1V05_S0_PCH_VCC_DMI 20 22
=PP1V05_S0_PCH_VCCIO_PLLFDI 20
=PP1V05_S0_PCH_VCCDMI_FDI 20
=PPVCCIO_S0_XDP 23
=PPVCCIO_S0_SMC 41
=PP1V05_S0_P1V05T29FET 36
6

T29 Rails (off when no cable)

36 8 =PP15V_T29_REG
PP15V_T29
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.0V
MAKE_BASE=TRUE
=PPHV_SW_DPAPWRSW 65
6

36 =PP3V3_T29_FET
PP3V3_T29
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PPVDDIO_T29_CLK 25
=PP3V3_T29_RTR 34 35 36
=PP3V3_T29_PCH_GPIO 16 19
6

36 =PP1V05_T29_FET
PP1V05_T29
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_T29_RTR 35
6 36

1V05 S0 LDO

60 =PP1V05_S0_LDO
PP1V05_S0_PCH_VCCADPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCCADPLL 20
6

Chipset "VCore" Rails

58 =PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 9 12 14
=PPCPUVCORE_S0_VSENSE 45
6

58 =PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU_VCCAXG 9 12 15
=PPGFXVCORE_S0_VSENSE 45
6

15 12 =PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
6

14 12 =PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
6

14 12 =PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
6

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010
PAGE TITLE
Power Aliases
Apple Inc.
DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 8 OF 109
SHEET 7 OF 75

Plated Board Slot

SL0900
TH-NSP
SL-2.3X3.9-2.9X4.5

CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss

Z0905
STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0914
STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0915
STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

USB/SD Card Pogo

CRITICAL
ZS0906
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

DisplayPort PCB Stiffener

(Provides PCB support for small finger above J9400)

NO STUFF
MT0900
STIFFENER-K16-K99
SM-SP
806-1176

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

T29 Can Slots

SL0901 TH-NSP SL-1.1X0.4-1.4X0.7
SL0902 TH-NSP SL-1.1X0.4-1.4X0.7
SL0903 TH-NSP SL-1.1X0.45-1.4X0.75
SL0904 TH-NSP SL-1.1X0.45-1.4X0.75
SL0905 TH-NSP SL-1.1X0.45-1.4X0.75
SL0906 TH-NSP SL-1.1X0.45-1.4X0.75

CPU signals

MEMVTT_EN (MAKE_BASE=TRUE) — =DDRVTT_EN

DP_EXTA_ML_C_P<3..0>	DP_IG_ML_P<3..0>	TP_DP_IG_B_MLP<3..0>
DP_EXTA_ML_C_N<3..0>	DP_IG_ML_N<3..0>	TP_DP_IG_B_MLN<3..0>
DP_EXTA_AUXCH_C_P	DP_IG_AUX_CH_P	DP_IG_B_AUX_P
DP_EXTA_AUXCH_C_N	DP_IG_AUX_CH_N	DP_IG_B_AUX_N

PCIE_EXCARD_D2R_N	TRUE	NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_D2R_P	TRUE	NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_R2D_C_N	TRUE	NC_PCIE_EXCARD_R2D_CN
PCIE_EXCARD_R2D_C_P	TRUE	NC_PCIE_EXCARD_R2D_CP
PCIE_CLK100M_EXCARD_N	TRUE	NC_PCIE_CLK100M_EXCARDN
PCIE_CLK100M_EXCARD_P	TRUE	NC_PCIE_CLK100M_EXCARDP
PEG_CLK100M_P		NC_PEG_CLK100MP
PEG_CLK100M_N		NC_PEG_CLK100MN

MEM_A_CLK_P<1>		TP_MEM_A_CLKP<1>
MEM_A_CLK_N<1>		TP_MEM_A_CLKN<1>
MEM_A_CKE<1>		NC_MEM_A_CKE<1>
MEM_A_CS_L<1>		NC_MEM_A_CS_L<1>
MEM_A_ODT<1>		NC_MEM_A_ODT<1>
MEM_B_CLK_P<1>		TP_MEM_B_CLKP<1>
MEM_B_CLK_N<1>		TP_MEM_B_CLKN<1>
MEM_B_CKE<1>		NC_MEM_B_CKE<1>
MEM_B_CS_L<1>		NC_MEM_B_CS_L<1>
MEM_B_ODT<1>		NC_MEM_B_ODT<1>
MEM_A_A<15>		TP_MEM_A_A<15>
MEM_B_A<15>		TP_MEM_B_A<15>

TP_PCH_CLKOUT_DPN — DPLL_REF_CLK_N — DPLL_REF_CLKN
TP_PCH_CLKOUT_DPP — DPLL_REF_CLK_P — DPLL_REF_CLKP
(MAKE_BASE=TRUE)

T29BST:N

=PPVIN_SW_T29BST — R0960 0 — =PP15V_T29_REG

T29_A_BIAS — C0960 0.01UF — GND

T29_A_BIAS caps

T29_A_BIAS_R	R0931 51	T29_A_BIAS_R2DP0 / C0901 0.01UF
T29_A_BIAS_R	R0932 51	T29_A_BIAS_R2DN0 / C0902 0.01UF
T29_A_BIAS_R	R0933 51	T29_A_BIAS_R2DP1 / C0903 0.01UF
T29_A_BIAS_R	R0934 51	T29_A_BIAS_R2DN1 / C0904 0.01UF

(SIGNAL_MODEL=EMPTY)

=PEG_R2D_C_P<3..0> — PEG_R2D_C_P<3..0> — PCIE_T29_R2D_C_P<3..0>
=PEG_R2D_C_N<3..0> — PEG_R2D_C_N<3..0> — PCIE_T29_R2D_C_N<3..0>
=PEG_D2R_P<3..0> — PEG_D2R_P<3..0> — PCIE_T29_D2R_P<3..0>
=PEG_D2R_N<3..0> — PEG_D2R_N<3..0> — PCIE_T29_D2R_N<3..0>
(MAKE_BASE=TRUE)

T29 DP Ports

TP_DP_IG_C_HPD	DP_T29SNK0_HPD
TP_DP_IG_C_MLP<3..0>	DP_T29SNK0_ML_C_P<3..0>
TP_DP_IG_C_MLN<3..0>	DP_T29SNK0_ML_C_N<3..0>
TP_DP_IG_C_AUXP	DP_T29SNK0_AUXCH_C_P
TP_DP_IG_C_AUXN	DP_T29SNK0_AUXCH_C_N
TP_DP_IG_D_HPD	DP_IG_D_HPD

(MAKE_BASE=TRUE)

=PP3V3_S0_DP_DDC — R0909 100K

DP_A_BIAS caps

=PP3V3_S0_DP_DDC — R0920 2.2K, R0921 2.2K, R0922 2.2K, R0923 2.2K

TP_DP_IG_C_CTRL_CLK	DP_IG_C_CTRL_CLK
TP_DP_IG_C_CTRL_DATA	DP_IG_C_CTRL_DATA
TP_DP_IG_D_CTRL_CLK	DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA	DP_IG_D_CTRL_DATA

(MAKE_BASE=TRUE)

=PP3V3_S0_DP_DDC — R0924 2.2K, R0925 2.2K

DP_EXTA_DDC_CLK	DP_IG_B_DDC_CLK
DP_EXTA_DDC_DATA	DP_IG_B_DDC_DATA
DP_EXTA_HPD	DP_IG_B_HPD

R0908 100K — CRITICAL R0910 0.01 0.5% 1W MF 0612-1

PPBUS_SW_LCDBKLT_PWR — PPBUS_SW_BKL (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE) — =PPBUS_SW_BKL
ISNS_LCDBKLT_P (OUT)
ISNS_LCDBKLT_N (OUT)

NC_USB_HUB1_OCS4 — =USB_HUB1_OCS4
NC_USB_HUB2_OCS4 — =USB_HUB2_OCS4
(MAKE_BASE=TRUE)

T29_A_BIAS caps

T29_A_BIAS_R — R0926 51 — T29_A_BIAS_D2RP1 / C0906 0.01UF
T29_A_BIAS_R — R0927 51 — T29_A_BIAS_D2RN1 / C0907 0.01UF
(SIGNAL_MODEL=EMPTY)

DP_A_BIAS caps

DP_A_BIAS_P_2 — C0962 0.01UF
DP_A_BIAS_P_0 — C0964 0.01UF
DP_A_BIAS_N_2 — C0905 0.01UF
DP_A_BIAS_N_0 — C0908 0.01UF
(SIGNAL_MODEL=EMPTY)

T29 Aliases

Unused USB ports

=PP3V3_S3_USB_HUB — R0915 10K, R0916 10K — NO STUFF

T29_A_RSVD_N — R0917 0 — USB_T29A_N
T29_A_RSVD_P — R0918 0 — USB_T29A_P
NO STUFF

LVDS Aliases

TP_LVDS_IG_B_CLKP	LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN	LVDS_IG_B_CLK_N
NC_LVDS_IG_B_DATAP<0..3> (NO_TEST=TRUE)	LVDS_IG_B_DATA_P<0..3>
NC_LVDS_IG_B_DATAN<0..3> (NO_TEST=TRUE)	LVDS_IG_B_DATA_N<0..3>
NC_LVDS_IG_A_DATAP<3> (NO_TEST=TRUE)	LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> (NO_TEST=TRUE)	LVDS_IG_A_DATA_N<3>
LCD_BKLT_PWM	LVDS_IG_BKL_PWM
LCD_IG_PWR_EN	LVDS_IG_PANEL_PWR
LCD_BKLT_EN	LVDS_IG_BKL_ON

(MAKE_BASE=TRUE)

SATA Aliases

Unused SATA ODD Signals

SATA_ODD_R2D_C_P (IN)	NC_SATA_ODD_R2DCP
SATA_ODD_R2D_C_N (IN)	NC_SATA_ODD_R2DCN
SATA_ODD_D2R_P (OUT)	NC_SATA_ODD_D2RP
SATA_ODD_D2R_N (OUT)	NC_SATA_ODD_D2RN

(MAKE_BASE=TRUE, NO_TEST=TRUE)

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE — P1V5S3RS0_RAMP_DONE (IN)
TP_DDRREG_PGOOD — DDRREG_PGOOD (IN)
(MAKE_BASE=TRUE)

T29 JTAG

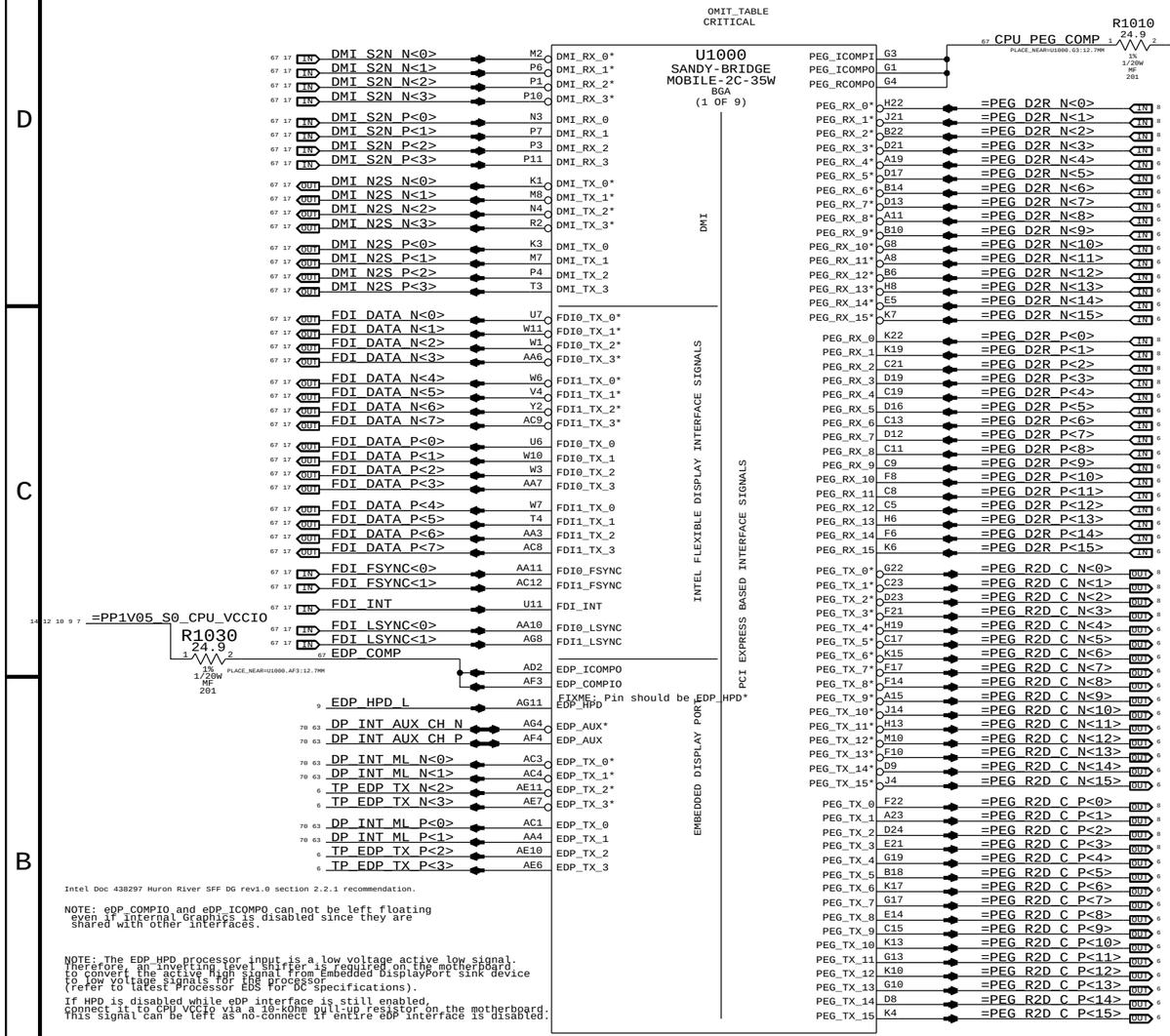
JTAG_ISP_TCK (IN) — R0990 0 — JTAG_T29_TCK (OUT)
JTAG_ISP_TDI (IN) — JTAG_T29_TDI (OUT)
JTAG_ISP_TDO (OUT) — JTAG_T29_TDO (IN)
(MAKE_BASE=TRUE)

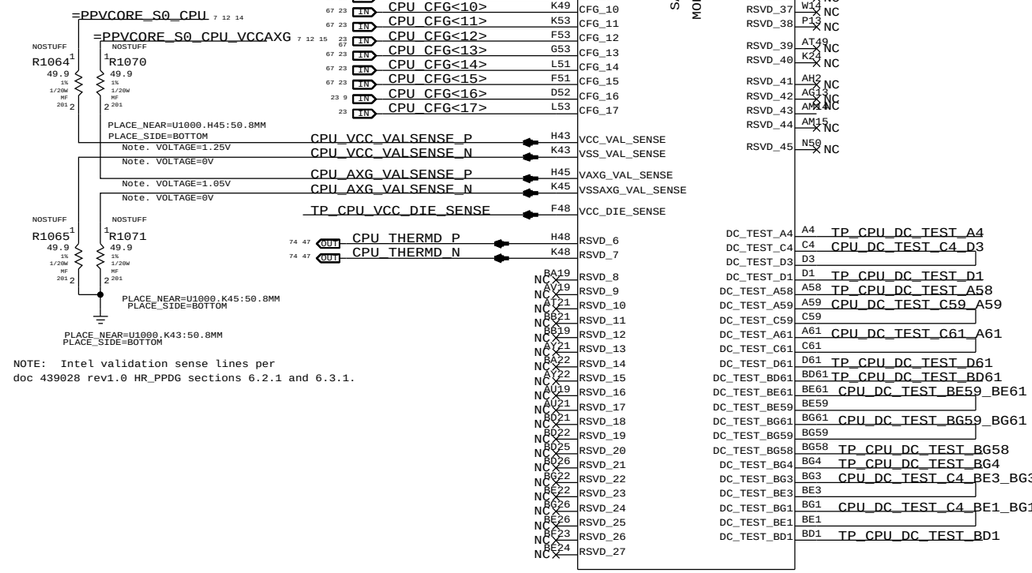
SYNC_MASTER=K91_MLB — SYNC_DATE=05/15/2016

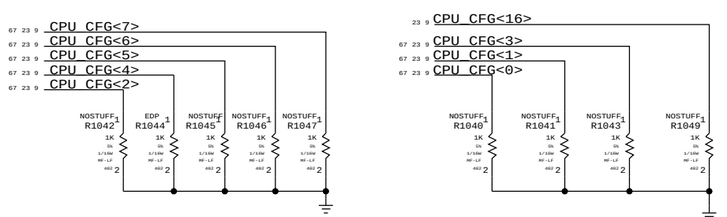
PAGE TITLE: Signal Aliases

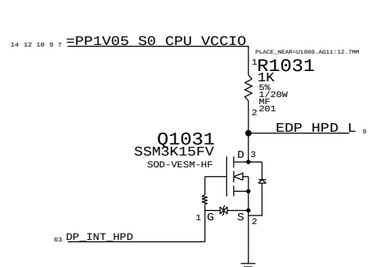
Apple Inc.

DRAWING NUMBER: 051-8870 — SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 9 OF 109
SHEET: 8 OF 75









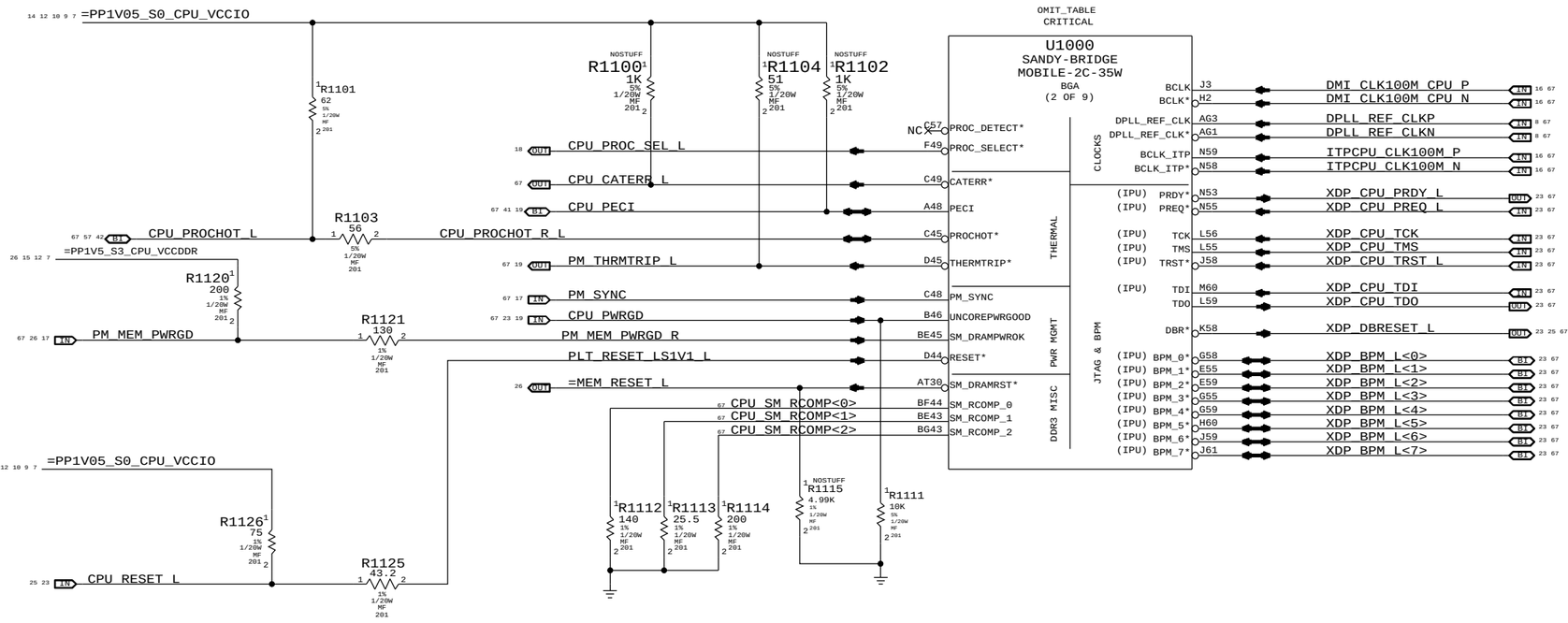
FOR SANDYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

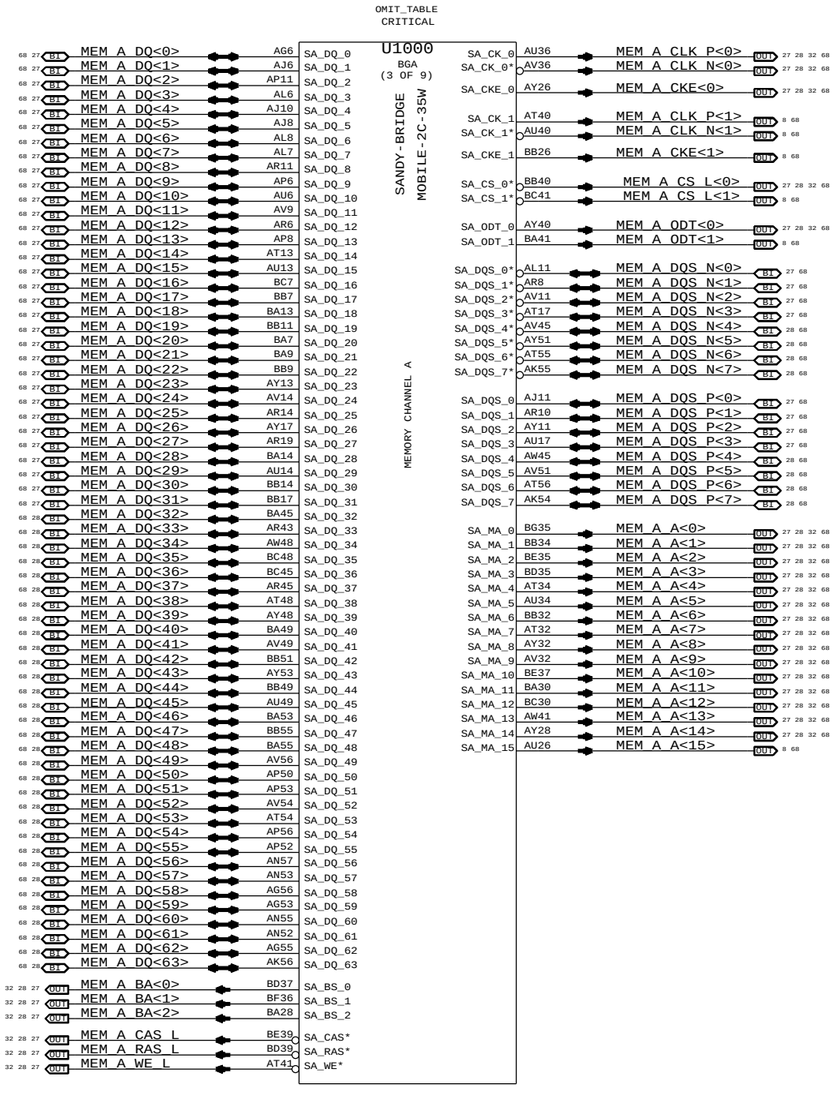
DRAWING NUMBER: 051-8870 | SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 10 OF 109
SHEET: 9 OF 75

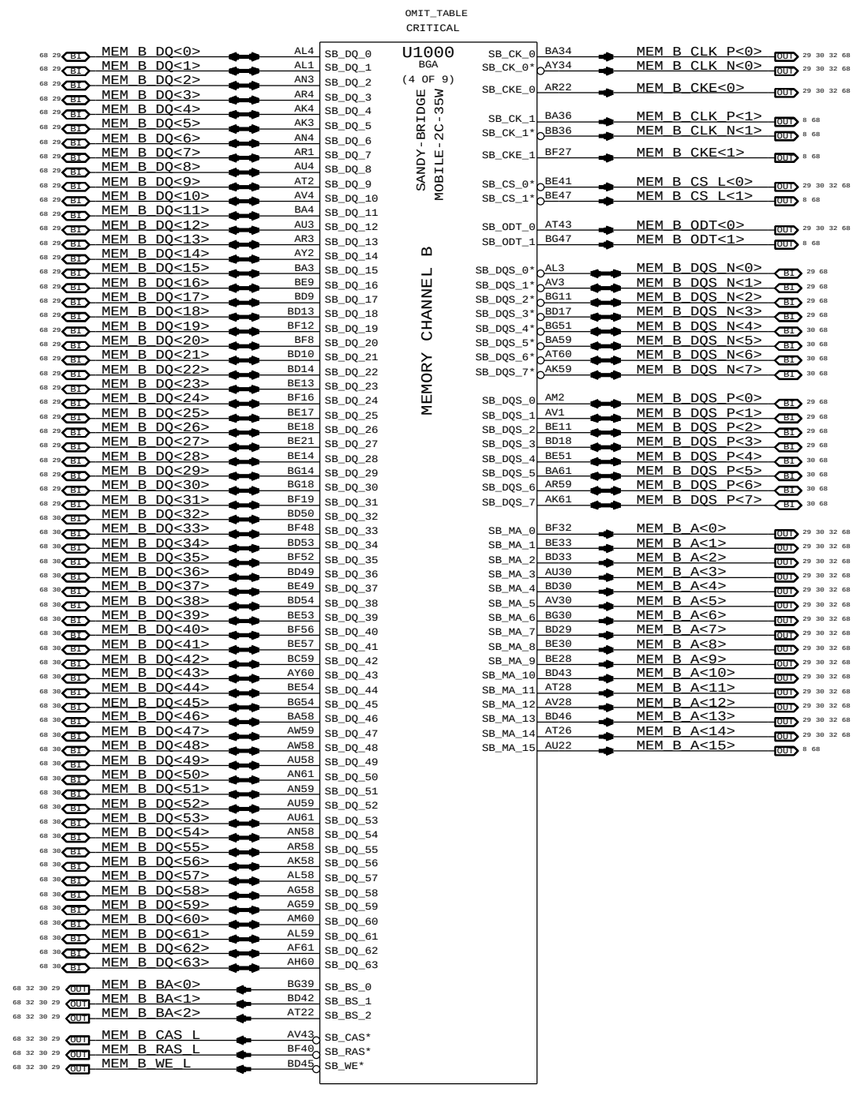


PAGE TITLE: CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 11 OF 109
SHEET: 10 OF 75





SYNC_DATE=01/10/2013

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

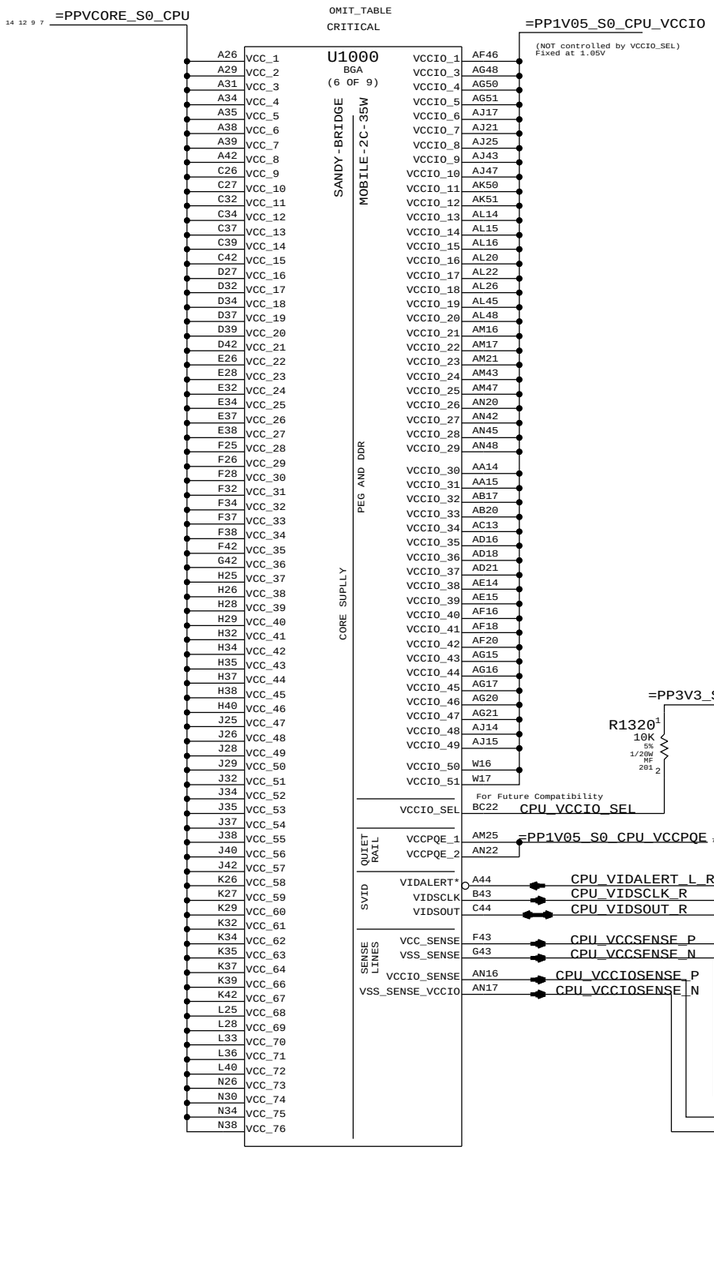
DRAWING NUMBER 051-8870 | SIZE D

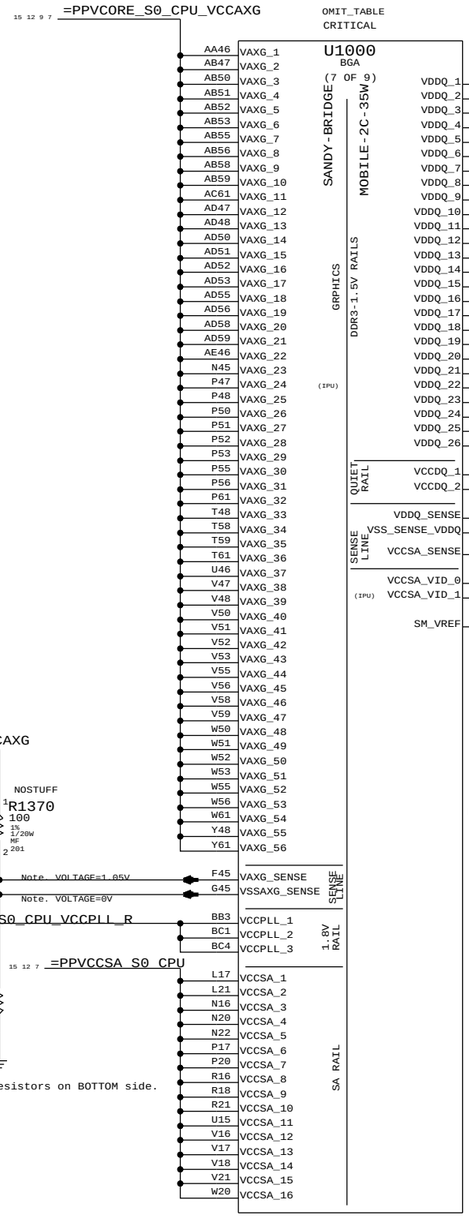
REVISION 3.13.0

BRANCH

PAGE 12 OF 109

SHEET 11 OF 75





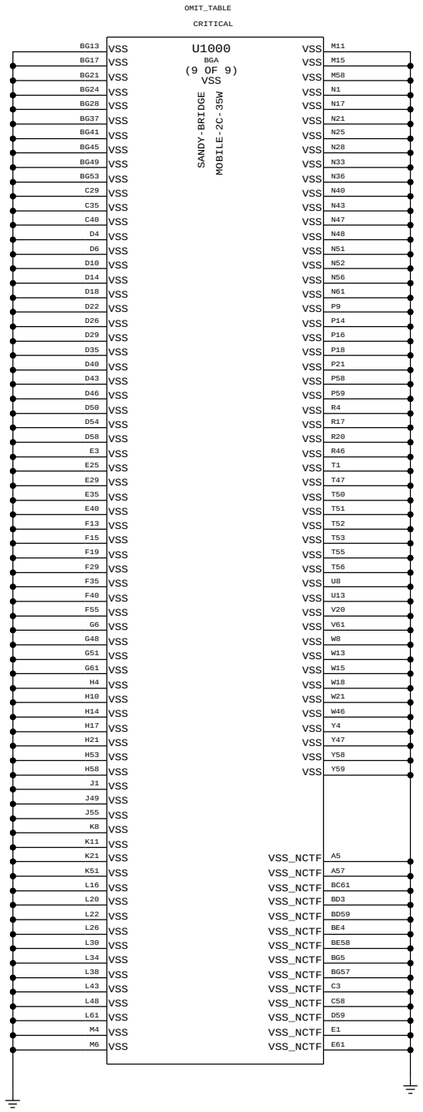
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

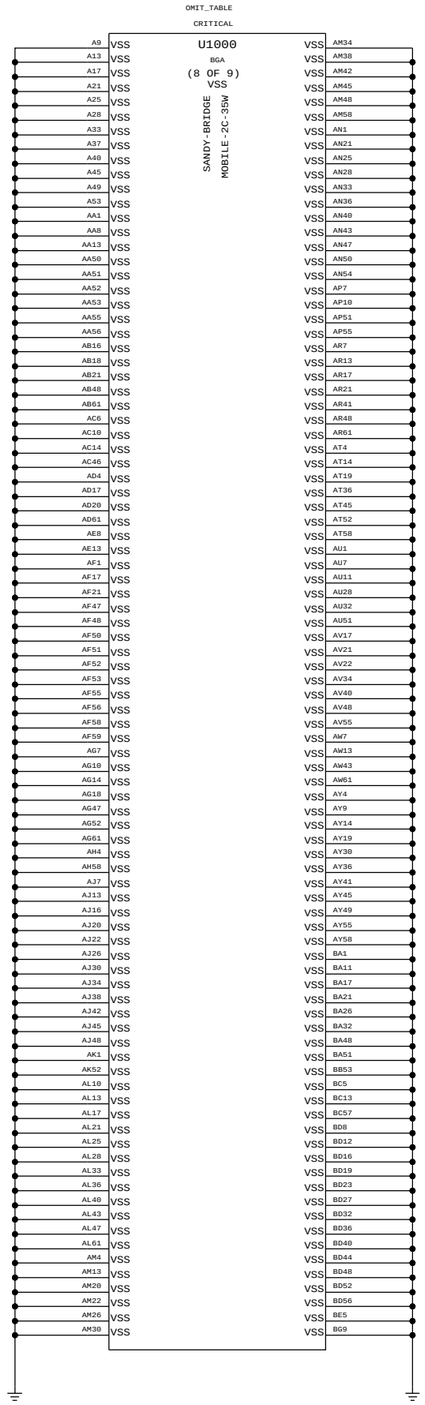
PAGE TITLE

CPU POWER

Apple Inc.

DRAWING NUMBER	051-8870
SIZE	D
REVISION	3.13.0
BRANCH	
PAGE	13 OF 109
SHEET	12 OF 75





PAGE TITLE
CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 14 OF 109
SHEET 13 OF 75

All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Processor Load Line : -2.9 mOhms

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU

CRITICAL C1600 2.2UF 20% 4V X5R 402
CRITICAL C1601 2.2UF 20% 4V X5R 402
CRITICAL C1602 2.2UF 20% 4V X5R 402
CRITICAL C1603 2.2UF 20% 4V X5R 402
CRITICAL C1604 2.2UF 20% 4V X5R 402
CRITICAL C1605 2.2UF 20% 4V X5R 402
CRITICAL C1606 2.2UF 20% 4V X5R 402
CRITICAL C1607 2.2UF 20% 4V X5R 402
CRITICAL C1608 2.2UF 20% 4V X5R 402
CRITICAL C1609 2.2UF 20% 4V X5R 402
CRITICAL C1610 2.2UF 20% 4V X5R 402
CRITICAL C1611 2.2UF 20% 4V X5R 402
CRITICAL C1612 2.2UF 20% 4V X5R 402
CRITICAL C1613 2.2UF 20% 4V X5R 402
CRITICAL C1614 2.2UF 20% 4V X5R 402
CRITICAL C1615 2.2UF 20% 4V X5R 402

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1655 22UF 20% 4V X5R 402
CRITICAL C1656 22UF 20% 4V X5R 402
CRITICAL C1657 22UF 20% 4V X5R 402
CRITICAL C1658 22UF 20% 4V X5R 402
CRITICAL C1659 22UF 20% 4V X5R 402
CRITICAL C1660 22UF 20% 4V X5R 402
CRITICAL C1661 22UF 20% 4V X5R 402
CRITICAL C1662 22UF 20% 4V X5R 402
CRITICAL C1663 22UF 20% 4V X5R 402
CRITICAL C1664 22UF 20% 4V X5R 402
CRITICAL C1665 22UF 20% 4V X5R 402
CRITICAL C1666 22UF 20% 4V X5R 402

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 270UF 20% 2V TANT CASE-B2-SM
C1681 270UF 20% 2V TANT CASE-B2-SM
C1682 270UF 20% 2V TANT CASE-B2-SM
C1683 270UF 20% 2V TANT CASE-B2-SM
C1679 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

12 10 9 7 =PP1V05_S0_CPU_VCCIO

Place on bottom side of U1000

C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402
C1687 1UF 10% 10V X5R 402
C1688 1UF 10% 10V X5R 402
C1689 1UF 10% 10V X5R 402
C1690 1UF 10% 10V X5R 402
C1691 1UF 10% 10V X5R 402
C1692 1UF 10% 10V X5R 402
C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1695 1UF 10% 10V X5R 402
C1696 1UF 10% 10V X5R 402
C1697 1UF 10% 10V X5R 402
C1698 1UF 10% 10V X5R 402
C1699 1UF 10% 10V X5R 402
C169A 1UF 10% 10V X5R 402
C169B 1UF 10% 10V X5R 402
C169C 1UF 10% 10V X5R 402
C169D 1UF 10% 10V X5R 402
C169E 1UF 10% 10V X5R 402
C169F 1UF 10% 10V X5R 402
C161A 1UF 10% 10V X5R 402
C161B 1UF 10% 10V X5R 402
C161C 1UF 10% 10V X5R 402
C161D 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM-X5R 0402-1
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C167G 270UF 20% 2V TANT CASE-B2-SM
C167H 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 7 12
C167F 1UF 10% 10V X5R 402 Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/10W MF-LF 402
=PP1V8_S0_CPU_VCCPLL_R 7 12
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

SYNC_MASTER=K78_MLB SYNC_DATE=02/08/2011

PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 16 OF 109
SHEET 14 OF 75

VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
C1709 1UF 10% 10V X5R 402
C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL

C1711 10UF 20% 6.3V CERM-X5R 0402-1
C1712 10UF 20% 6.3V CERM-X5R 0402-1
C1713 10UF 20% 6.3V CERM-X5R 0402-1
C1714 10UF 20% 6.3V CERM-X5R 0402-1
C1715 10UF 20% 6.3V CERM-X5R 0402-1
C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL

C1717 22UF 20% 6.3V X5R-CERM1 0603
C1718 22UF 20% 6.3V X5R-CERM1 0603
C1719 22UF 20% 6.3V X5R-CERM1 0603
C1720 22UF 20% 6.3V X5R-CERM1 0603
C1721 22UF 20% 6.3V X5R-CERM1 0603
C1722 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1723-C1724):

C1723 270UF 20% 2V TANT CASE-B2-SM
C1724 270UF 20% 2V TANT CASE-B2-SM
C1725 270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

12 7 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

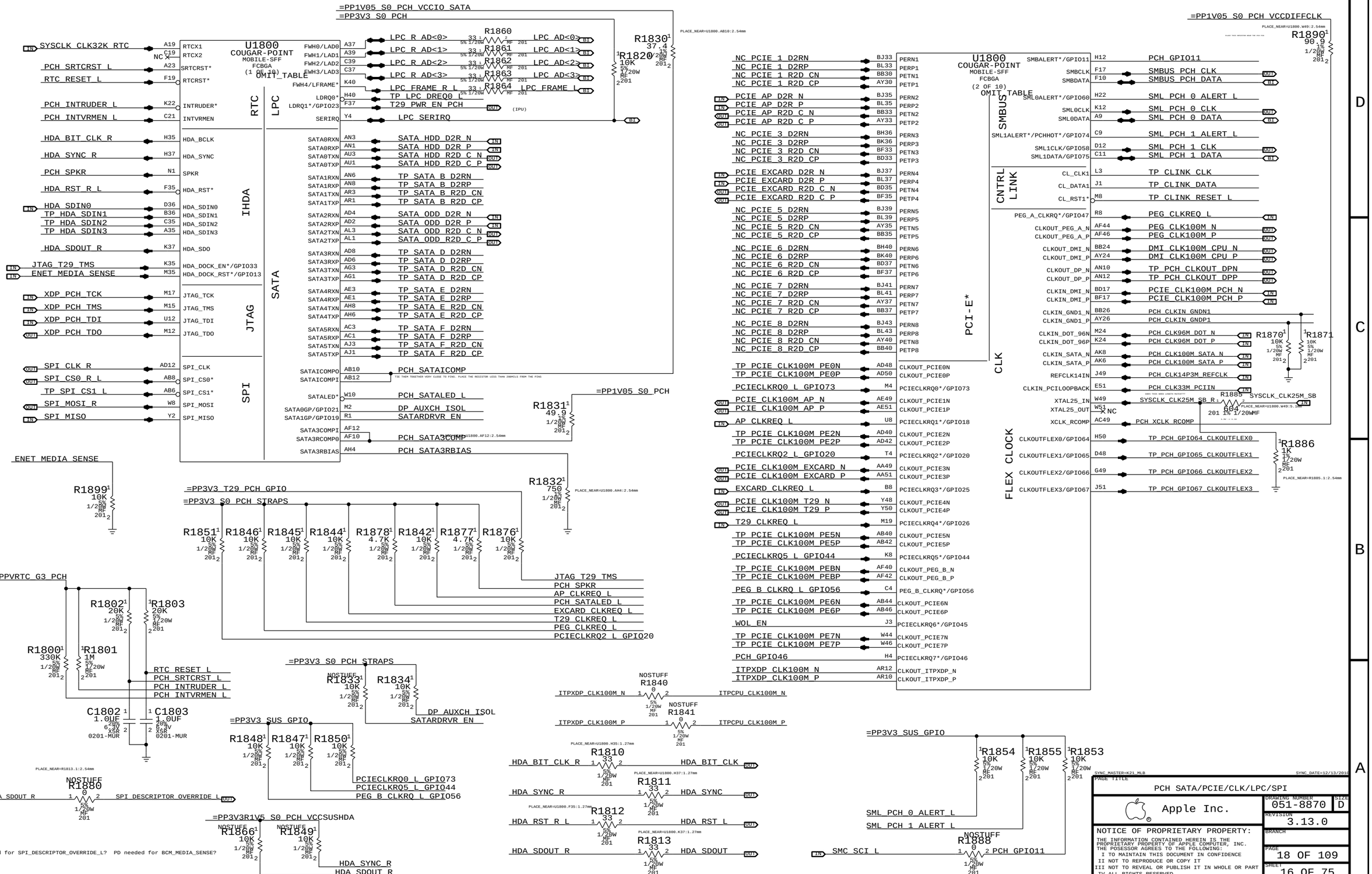
C1768 270UF 20% 2V TANT CASE-B2-SM

SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2012

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 17 OF 109
SHEET 15 OF 75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=PP3V3_S0_PCH
U1800
COUGAR-POINT
MOBILE-SFF
FCBGA
(1 OF 10)
OMIT_TABLE
SYSCLK_CLK32K_RTC
PCH_SRTCRST_L
RTC_RESET_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_T29_TMS
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
RTC
LPC
IHDA
JTAG
SPI
SATA
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_R_L
LPC_FRAME_L
TP_LPC_DREQ0_L
T29_PWR_EN_PCH
LPC_SERIRQ
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
TP_SATA_B_D2RN
TP_SATA_B_D2RP
TP_SATA_B_R2D_CN
TP_SATA_B_R2D_CP
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
PCH_SATAICOMP
PCH_SATALED_L
DP_AUXCH_ISOL
SATARDRVR_EN
PCH_SATA3COMP
PCH_SATA3RBIAS
=PP1V05_S0_PCH
R1831 49.9
R1820 10K
R1830 37.4
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
ENET_MEDIA_SENSE
R1899 10K
=PP3V3_T29_PCH_GPIO
=PP3V3_S0_PCH_STRAPS
R1832 750
R1851 10K
R1846 10K
R1845 10K
R1844 10K
R1878 4.7K
R1842 10K
R1877 4.7K
R1876 10K
JTAG_T29_TMS
PCH_SPKR
AP_CLKREQ_L
PCH_SATALED_L
EXCARD_CLKREQ_L
T29_CLKREQ_L
PEG_CLKREQ_L
PCIECLKRQ2_L_GPIO20
=PPVRTC_G3_PCH
R1802 20K
R1803 20K
R1800 330K
R1801 1M
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
C1802 1.0UF
C1803 1.0UF
=PP3V3_S0_PCH_STRAPS
R1833 10K
R1834 10K
DP_AUXCH_ISOL
SATARDRVR_EN
=PP3V3_SUS_GPIO
R1848 10K
R1847 10K
R1850 10K
PCIECLKRQ0_L_GPIO73
PCIECLKRQ5_L_GPIO44
PEG_B_CLKRQ_L_GPIO56
R1880 0
HDA_SDOUT_R
SPI_DESCRIPTOR_OVERRIDE_L
=PP3V3R1V5_S0_PCH_VCCSUSHDA
R1866 10K
R1849 10K
HDA_SYNC_R
HDA_SDOUT_R
pullup needed for SPI_DESCRIPTOR_OVERRIDE_L? PD needed for BCM_MEDIA_SENSE?
=PP1V05_S0_PCH_VCCDIFFCLK
R1890 90.9
U1800
COUGAR-POINT
MOBILE-SFF
FCBGA
(2 OF 10)
OMIT_TABLE
PCI-E*
CLK
SMBUS
CNTRL LINK
FLEX CLOCK
NC_PCIE_1_D2RN
NC_PCIE_1_D2RP
NC_PCIE_1_R2D_CN
NC_PCIE_1_R2D_CP
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
NC_PCIE_3_D2RN
NC_PCIE_3_D2RP
NC_PCIE_3_R2D_CN
NC_PCIE_3_R2D_CP
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
TP_PCIE_CLK100M_PE0N
TP_PCIE_CLK100M_PE0P
PCIECLKRQ0_L_GPIO73
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
TP_PCIE_CLK100M_PE2N
TP_PCIE_CLK100M_PE2P
PCIECLKRQ2_L_GPIO20
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
PCIE_CLK100M_T29_N
PCIE_CLK100M_T29_P
T29_CLKREQ_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCIECLKRQ5_L_GPIO44
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEG_B_CLKRQ_L_GPIO56
TP_PCIE_CLK100M_PE6N
TP_PCIE_CLK100M_PE6P
WOL_EN
TP_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P
PCH_GPIO46
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK1
CL_DATA1
CL_RST1*
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
PCH_GPIO11
SMBUS_PCH_CLK
SMBUS_PCH_DATA
SML_PCH_0_ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
SML_PCH_1_ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEG_CLKREQ_L
PEG_CLK100M_N
PEG_CLK100M_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB
PCH_XCLK_RCOMP
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
R1870 10K
R1871 10K
R1885 604
R1886 1K
=PP3V3_SUS_GPIO
R1854 10K
R1855 10K
R1853 10K
SML_PCH_0_ALERT_L
SML_PCH_1_ALERT_L
SMC_SCI_L
R1888 0
PCH_GPIO11
R1840 0
R1841 0
R1810 33
R1811 33
R1812 33
R1813 33
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
HDA_SDOUT_R
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
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DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 18 OF 109
SHEET 16 OF 75
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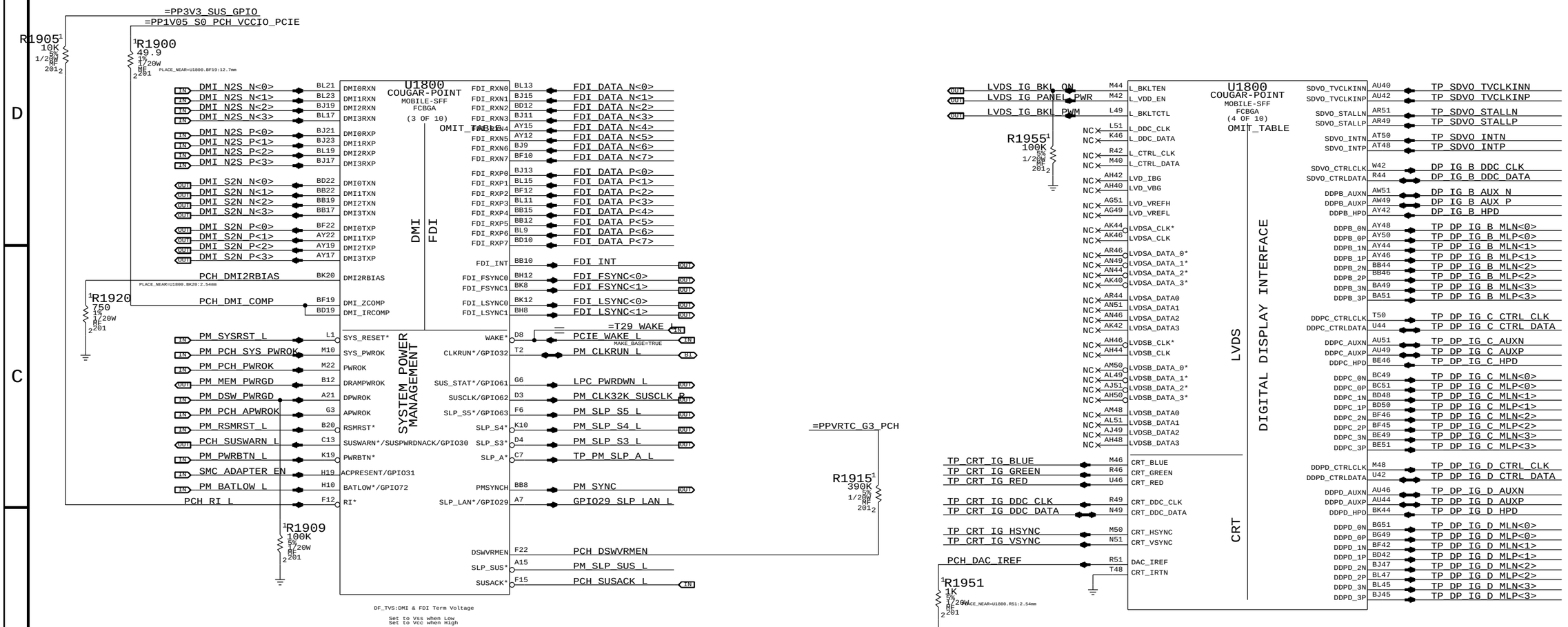

PAGE TITLE: PCH DMI/FDI/GRAPHICS

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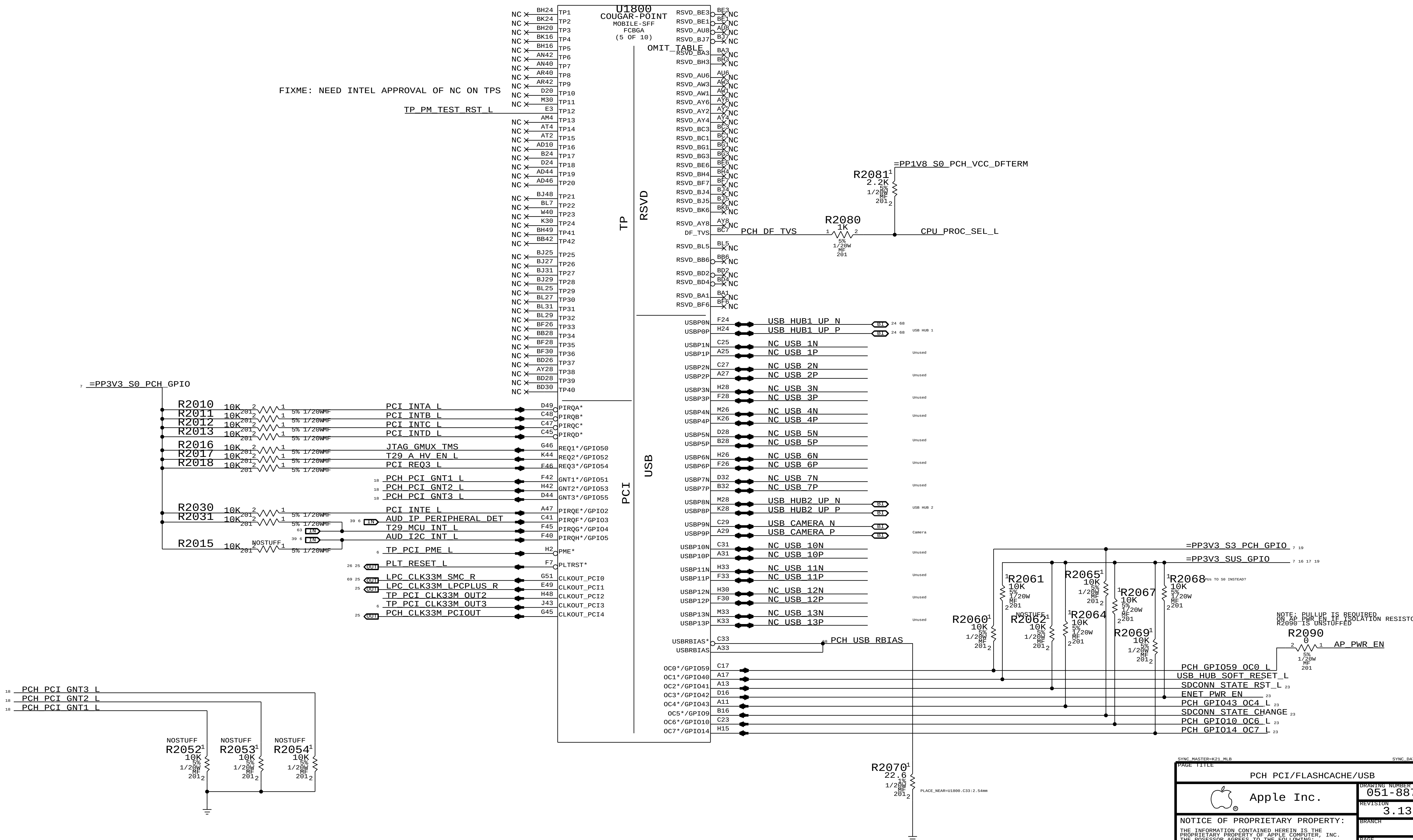
DRAWING NUMBER: 051-8870 | SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 19 OF 109

SHEET: 17 OF 75



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PAGE TITLE: PCH PCI/FLASHCACHE/USB

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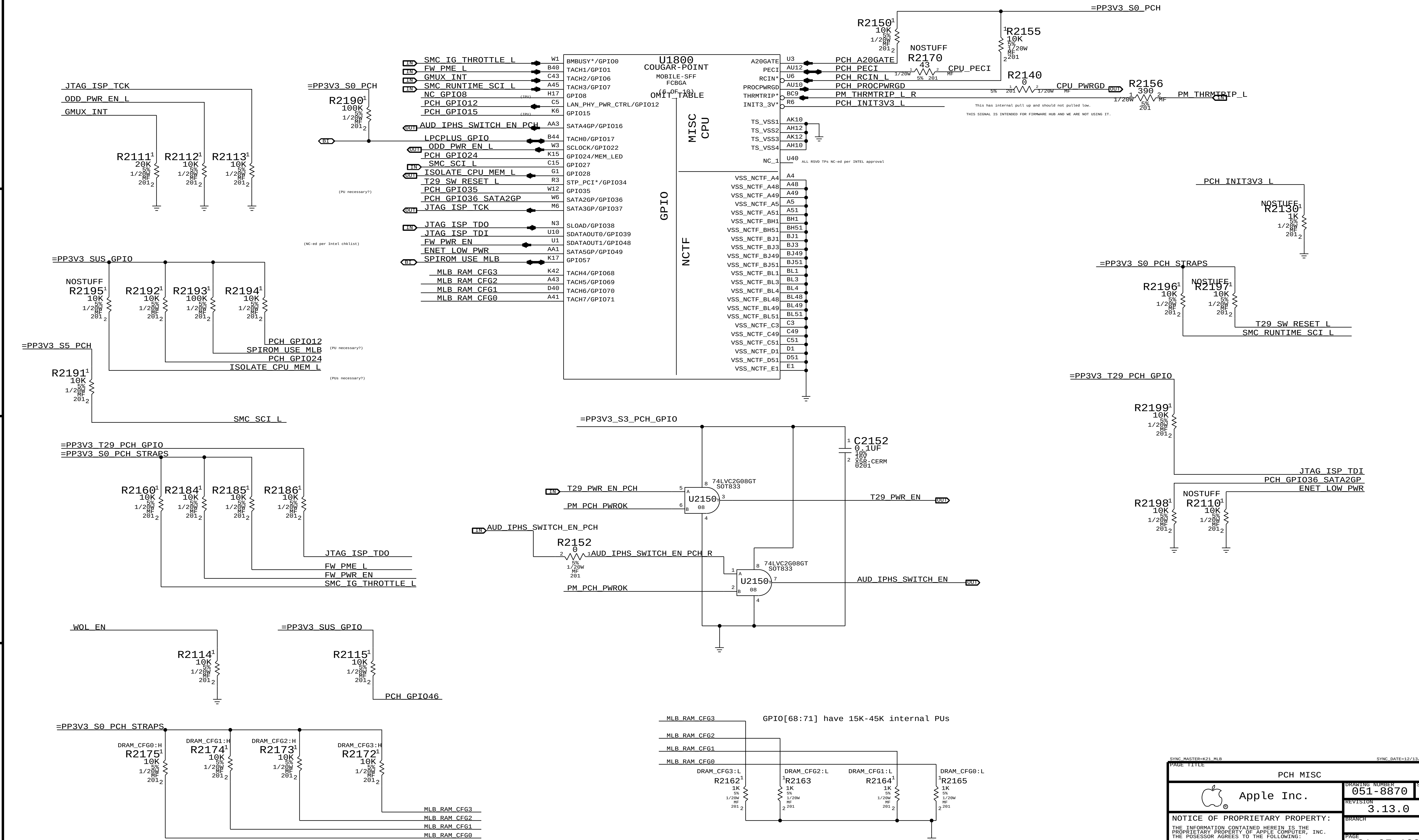
DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH

PAGE: 20 OF 109

SHEET: 18 OF 75



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PCH MISC

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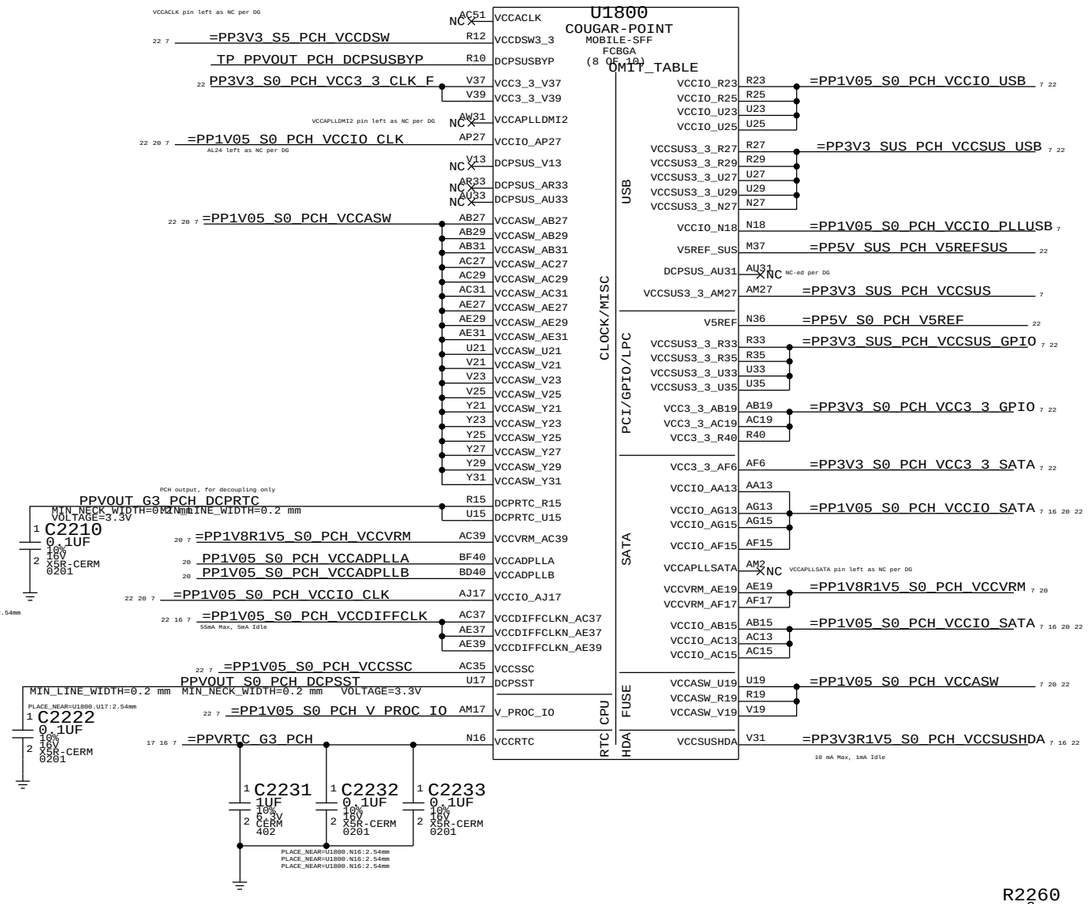

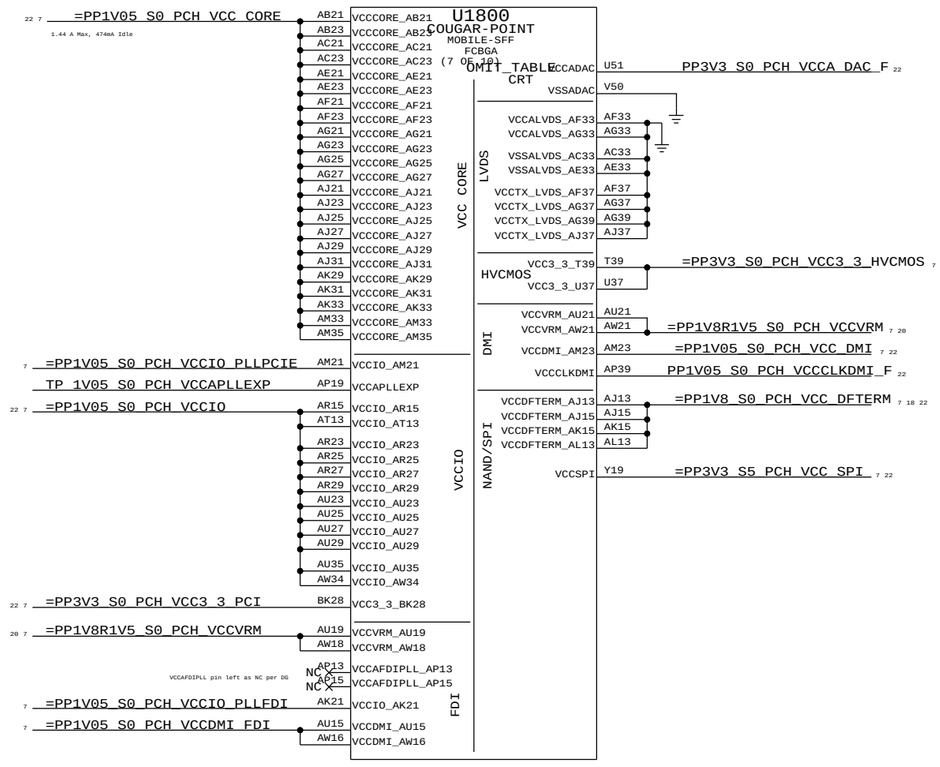

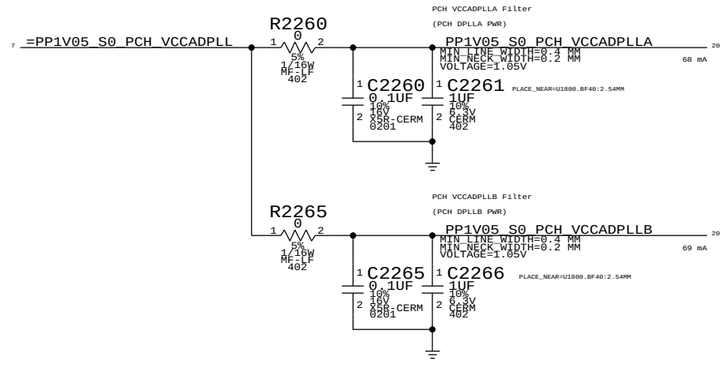

PAGE TITLE: PCH POWER

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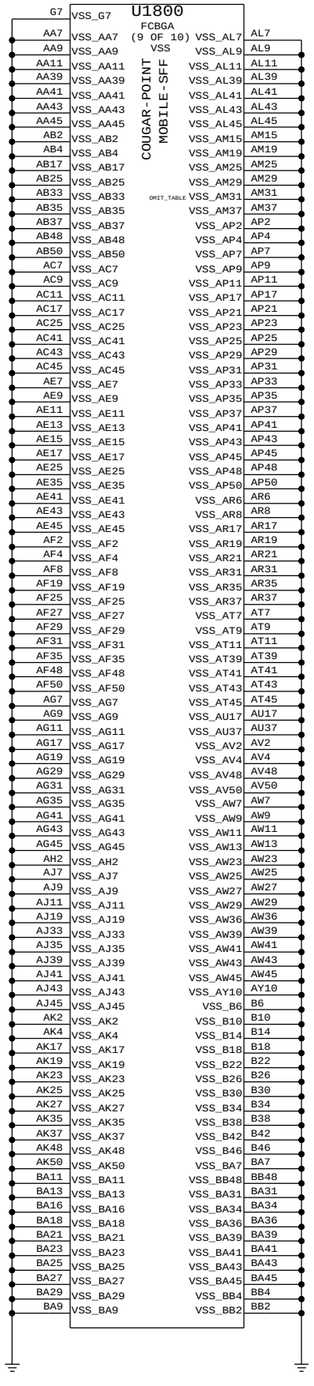
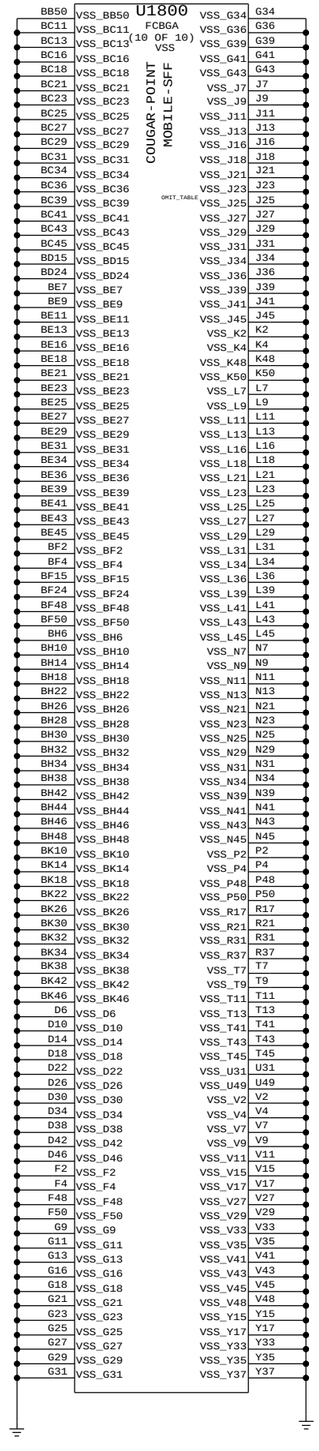
DRAWING NUMBER: 051-8870
SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 22 OF 109
SHEET: 20 OF 75





SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

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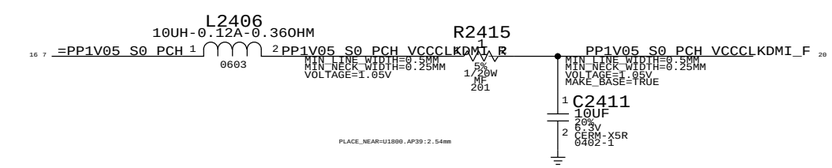
DRAWING NUMBER 051-8870 SIZE D

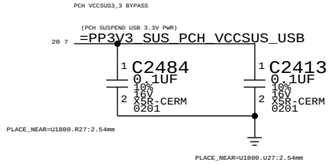
REVISION 3.13.0

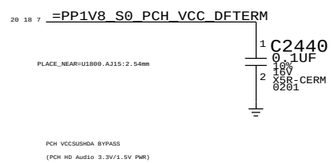
BRANCH

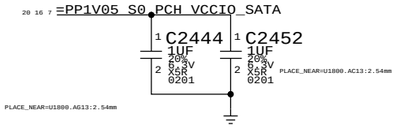
PAGE 23 OF 109

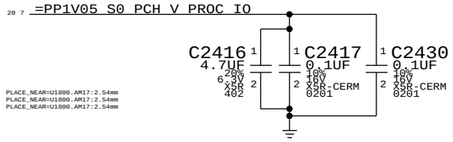
SHEET 21 OF 75

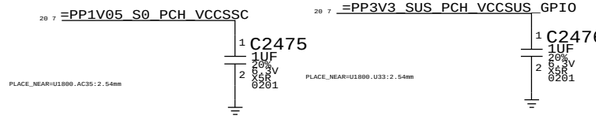


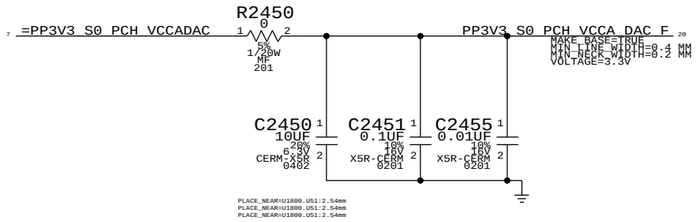


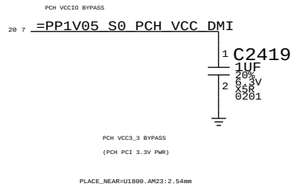


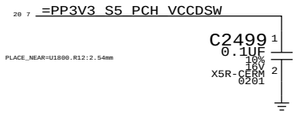


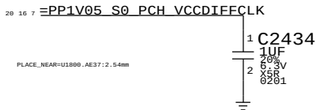


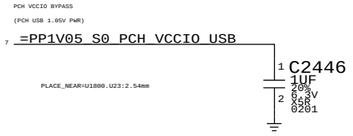


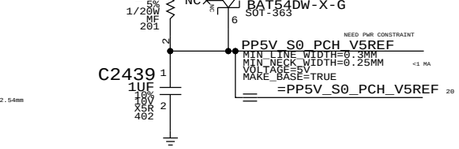


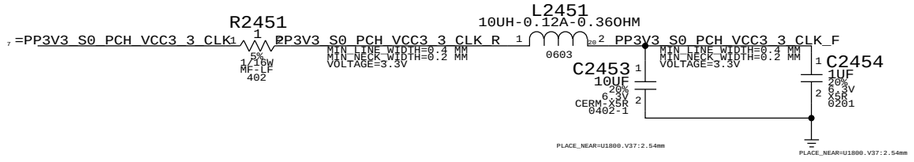


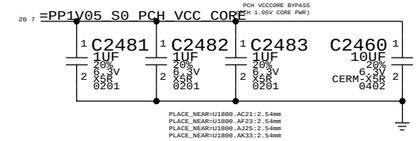


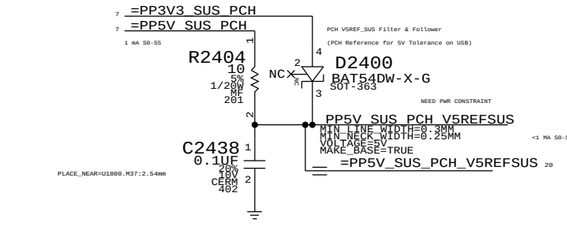


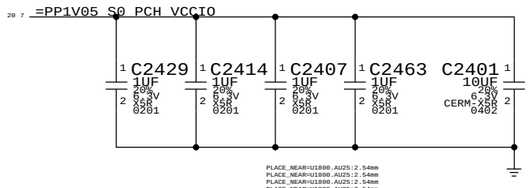


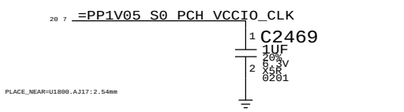


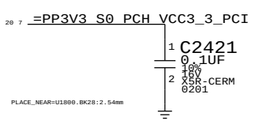


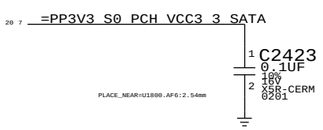


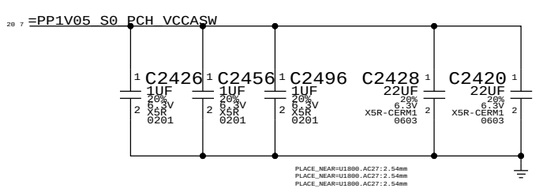


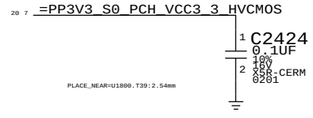


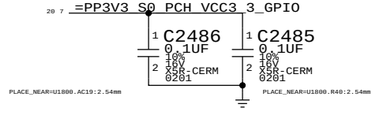












SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

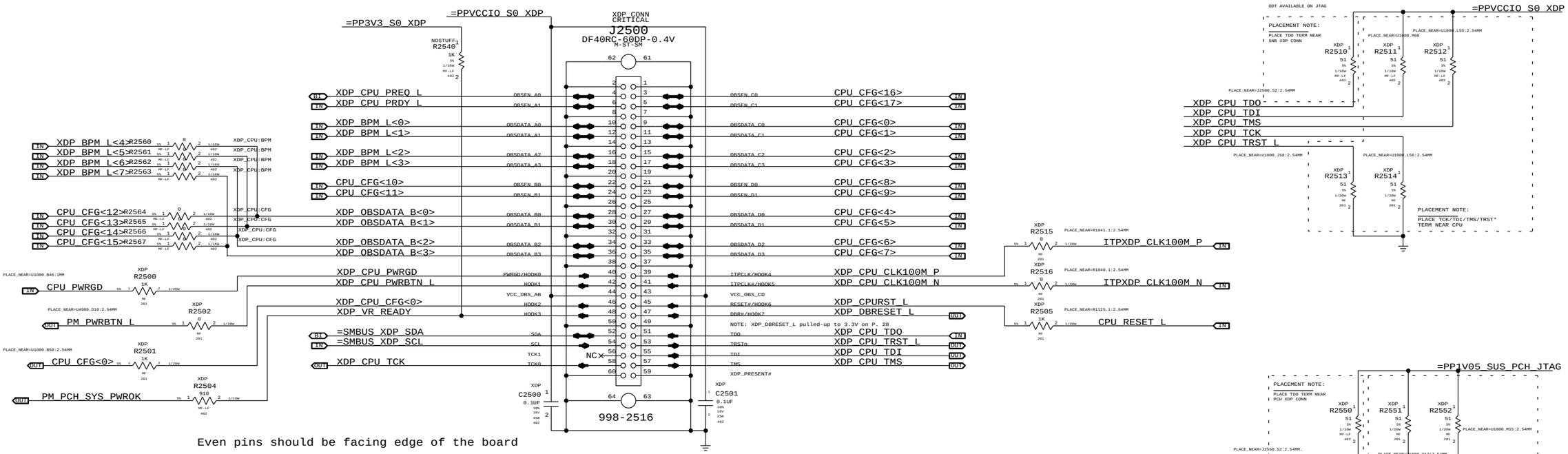
BRANCH

PAGE 24 OF 109

SHEET 22 OF 75

PROCESSOR MICRO2-XDP CONNECTOR

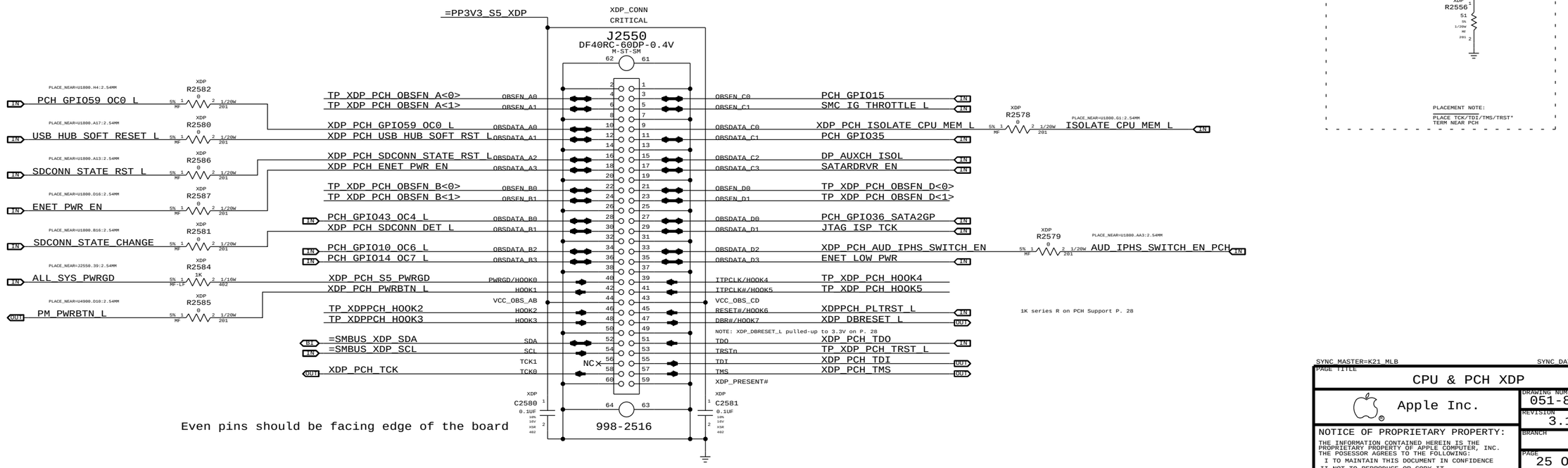
NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



Even pins should be facing edge of the board

PCH MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



Even pins should be facing edge of the board

SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2016

PAGE TITLE
CPU & PCH XDP

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 25 OF 109
SHEET 23 OF 75

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2016
PAGE TITLE: USB HUBS	
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	REVISION: 3.13.0
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	PAGE: 26 OF 109
	SHEET: 24 OF 75

System RTC Power Source & 32kHz / 25MHz Clock Generator

=PPVBAT_G3_SYSCLK
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

=PP3V3_S5_SYSCLK
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5

GreenClk 25MHz Power Powered in S0 =PP3V3_S0_SYSCLKGEN
No bypass necessary

SB XTAL Power =PPVDDIO_S0_SBCLK
T29 XTAL Power =PPVDDIO_T29_CLK

C2724 0.1UF 10% 16V X5R-CERM 0201
C2722 0.1UF 10% 16V X5R-CERM 0201
C2702 1UF 10% 10V X5R 402-1

U2700 SLG3NB148V TQFN CRITICAL
VDD_25M, +V3.3A, +3.42V
VDDIO_25M_A, VDDIO_25M_B, VDDIO_25M_C
32KHZ_A, 25MHZ_A, 25MHZ_B, 25MHZ_C, X2, X1, VDD_RTC_OUT, GND, THRM PAD

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.
+V3.3A should be first available ~3.3V power to reduce VBAT draw.

Ground VDDIO of unused CLK outputs for power savings

SYSCLK_CLK32K_RTC → OUT 16 70
SYSCLK_CLK25M_SB → OUT 16 70
SYSCLK_CLK25M_T29 → OUT 34 70
=PPVRTC_G3_OUT → 7 For SB RTC Power

C2705 12PF 5% 25V NP0-C0G 201
C2706 12PF 5% 25V NP0-C0G 201
SYSCLK_CLK25M_X2
SYSCLK_CLK25M_X2_R
SYSCLK_CLK25M_X1
R2705 0 5% 1/20W MF 201
NO STUFF
R2706 1M 5% 1/20W MF 201
NC
NC
CRITICAL
Y2705 25.000MHZ-12PF-20PPM SM-3.2X2.5MM
NOTE: 30 PPM crystal required
C2710 1UF 10% 10V X5R 402-1

Platform Reset Connections

Unbuffered

26 18 IN PLT_RESET_L MAKE_BASE=TRUE

R2781 33 5% 1/20W MF 201 — LPC_RESET_L → OUT 70
LPCPLUS_RESET_L MAKE_BASE=TRUE → OUT 6 43
R2783 33 5% 1/20W MF 201 — SMC_LRESET_L → OUT 41
R2782 0 5% 1/20W MF 201 — SDCARD_PLT_RST_L → OUT 33
R2788 0 5% 1/20W MF 201 — AP_RESET_L → OUT 37
R2771 0 5% 1/20W MF 201 — PCA9557D_RESET_L → OUT 31
XDP
R2789 1K 5% 1/20W MF 201 — XDPPCH_PLTRST_L → OUT 23
=T29_RESET_L → OUT 36
Series R is R3803
R2793 0 5% 1/20W MF 201 — BKLT_PLT_RST_L → OUT 66

Buffered

7 =PP3V3_S0_RSTBUF
U2780 74LVC1G07 SC70
C2780 0.1UF 10% 16V X5R-CER0M 0201
NC
NC
PLT_RST_BUF_L MAKE_BASE=TRUE
R2780 100K 5% 1/20W MF 201
CPU_RESET_L → OUT 10 23
VTT voltage divider on CPU page

PCH S0 PWRGD

25 7 =PP3V3_S5_PCHPWRGD
25 7 =PP3V3_S0_SB_PM
R2750 1K 5% 1/20W MF 201
C2750 0.1UF 10% 16V X5R-CERM 0201
62 52 41 22 IN ALL_SYS_PWRGD
57 IN CPUIMVP_PGOOD
U2750 MC74VHC1G08 SC70-mF
PM_S0_PGOOD
U2760 MC74VHC1G08 SC70-mF
SYS_PWROK_R
R2762 3.0K 5% 1/20W MF 201
PM_PCH_SYS_PWROK → OUT 17 23
PLACE_NEAR=U1800.M10:5.54mm
NO STUFF
R2761 0 5% 1/20W MF 201
R2763 0 5% 1/20W MF 201
=PP3V3_S5_PCHPWRGD 7 25
C2760 0.1UF 10% 16V X5R-CERM 0201
R2760 0 5% 1/20W MF 201
41 36 SMC_DELAYED_PWRGD
PM_PCH_PWROK → OUT 17 19
MAKE_BASE=TRUE
PM_PCH_APWROK → OUT 17

PCH Reset Button

25 7 =PP3V3_S0_SB_PM
R2795 10K 5% 1/16W MF-LF 402
XDP
R2796 0 1/16W 402 MF-LF 5%
67 23 10 IN XDP_DBRESET_L
PM_SYSRST_L → BI 17 41
NO STUFF
R2797 0 5% 1/10W MF-LF 402
SILK_PART=SYS RESET

CLOCK (CK505)

UNUSED clock terminations for FCIM MODE

69 16 PCH_CLK14P3M_REFCLK
69 16 PCIE_CLK100M_PCH_N
69 16 PCIE_CLK100M_PCH_P
69 16 PCH_CLK100M_SATA_N
69 16 PCH_CLK100M_SATA_P
69 16 PCH_CLK96M_DOT_N
69 16 PCH_CLK96M_DOT_P
R2757 10K 5% 1/20W MF 201
R2751 10K 5% 1/20W MF 201
R2752 10K 5% 1/20W MF 201
R2753 10K 5% 1/20W MF 201
R2754 10K 5% 1/20W MF 201
R2755 10K 5% 1/20W MF 201
R2756 10K 5% 1/20W MF 201

R2727 22 5% 1/20W MF 201
70 18 IN PLACE_NEAR=U1800.G51:5.1mm LPC_CLK33M_SMC_R
LPC_CLK33M_SMC → OUT 41 70
R2726 22 5% 1/20W MF 201
18 IN PLACE_NEAR=U1800.E49:5.1mm LPC_CLK33M_LPCPLUS_R
LPC_CLK33M_LPCPLUS → OUT 6 43 70
R2729 22 5% 1/20W MF 201
18 IN PLACE_NEAR=U1800.G45:2.54MM:5.1mm PCH_CLK33M_PCIOUT
PCH_CLK33M_PCIIN → OUT 16 69

SYNC_MASTER=K78_MLB SYNC_DATE=11/29/201

PAGE TITLE
Clock (CK505) and Chipset Support

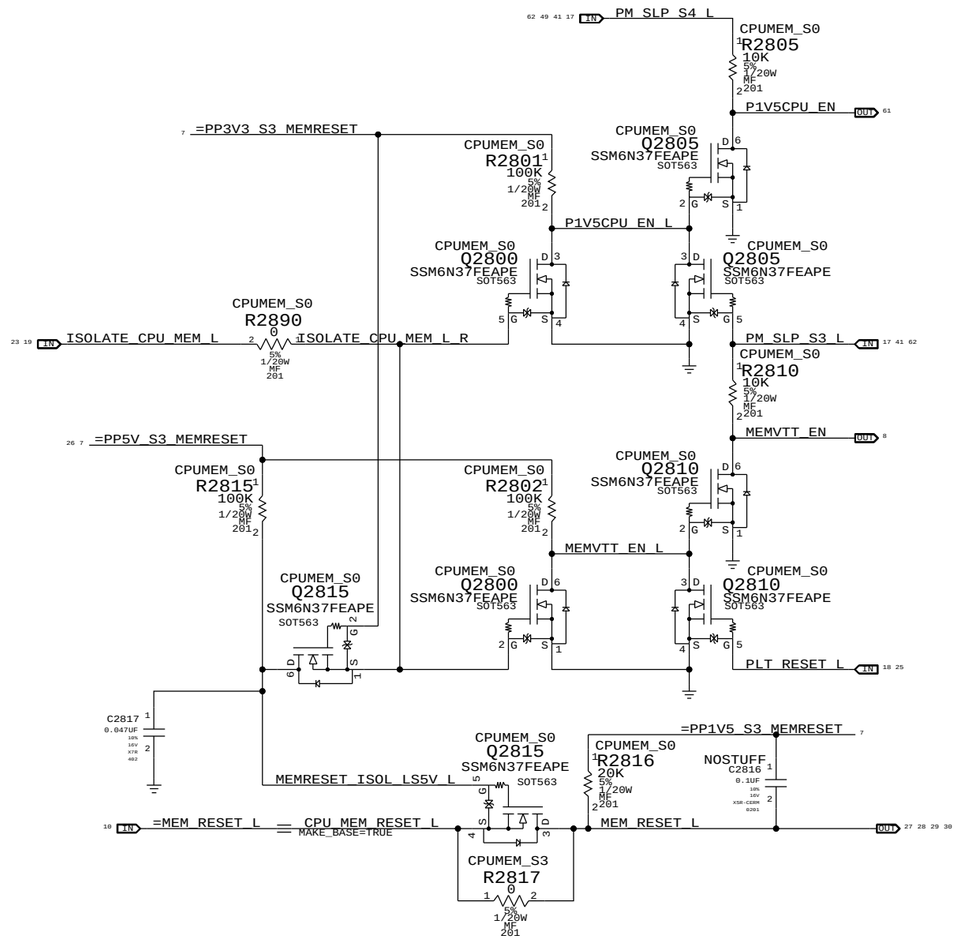
Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 27 OF 109
SHEET 25 OF 75

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well
as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

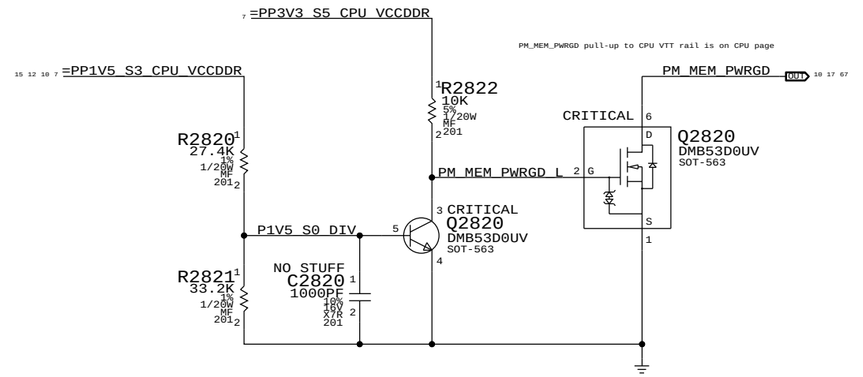


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3	4	0	0	1	1	X	1	0	1
	5	0	1	1	1	0 (*)	1	1	1
to	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

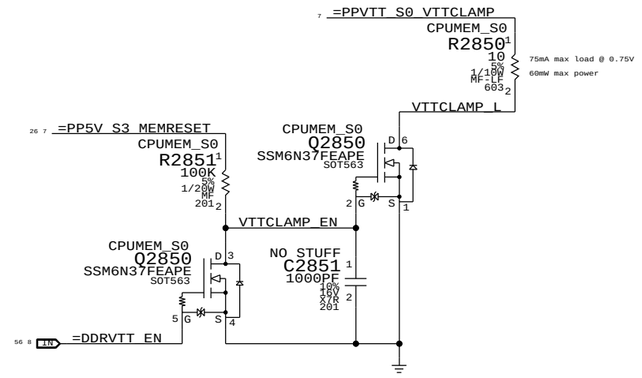
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3

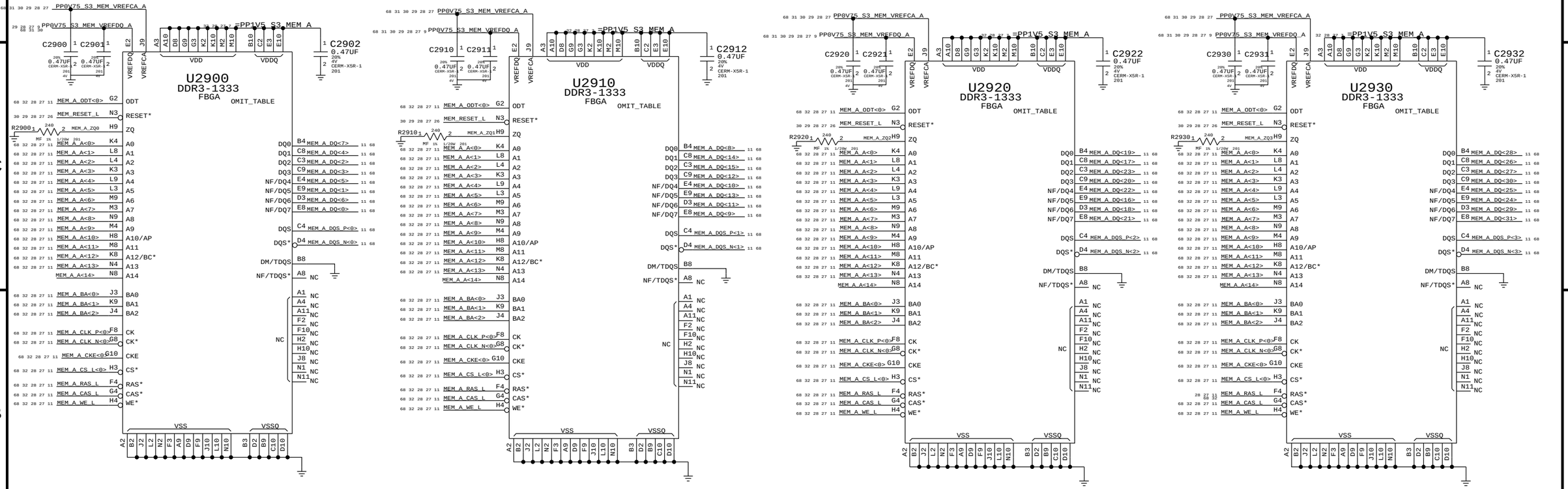


SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 28 OF 109
SHEET: 26 OF 75



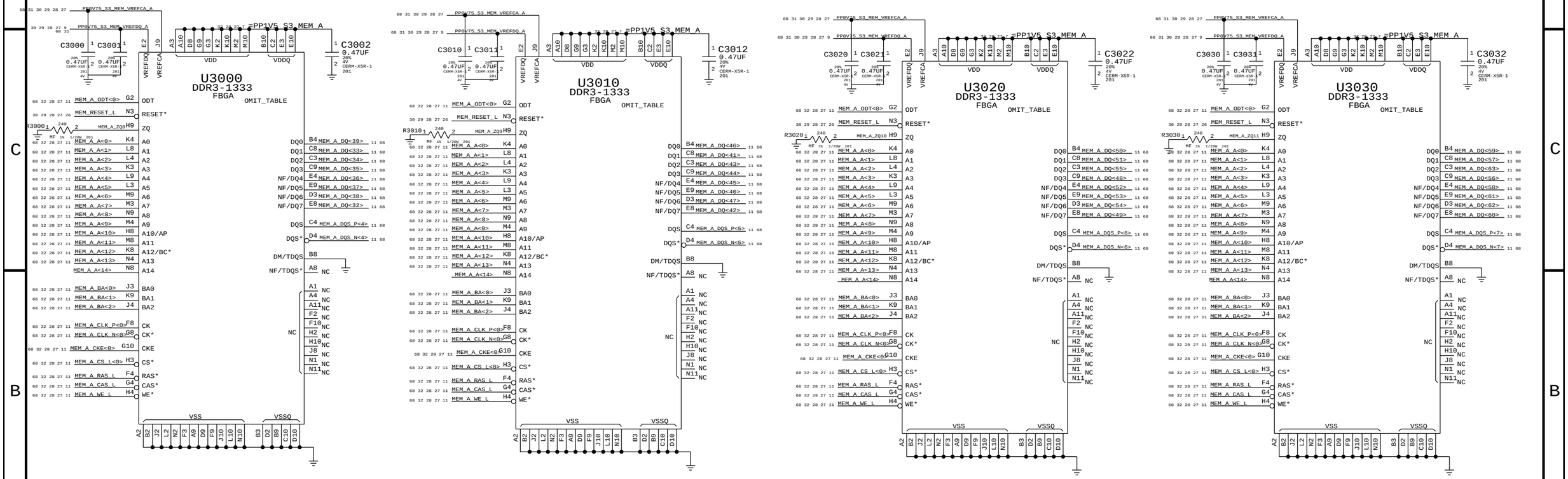
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K78_MLB SYNC_DATE=12/07/2010

PAGE TITLE
DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 29 OF 109
SHEET 27 OF 75



SYNC_MASTER=K78_MLB SYNC_DATE=12/07/2010

PAGE TITLE

DDR3 DRAM CHANNEL A (32-63)

Apple Inc.

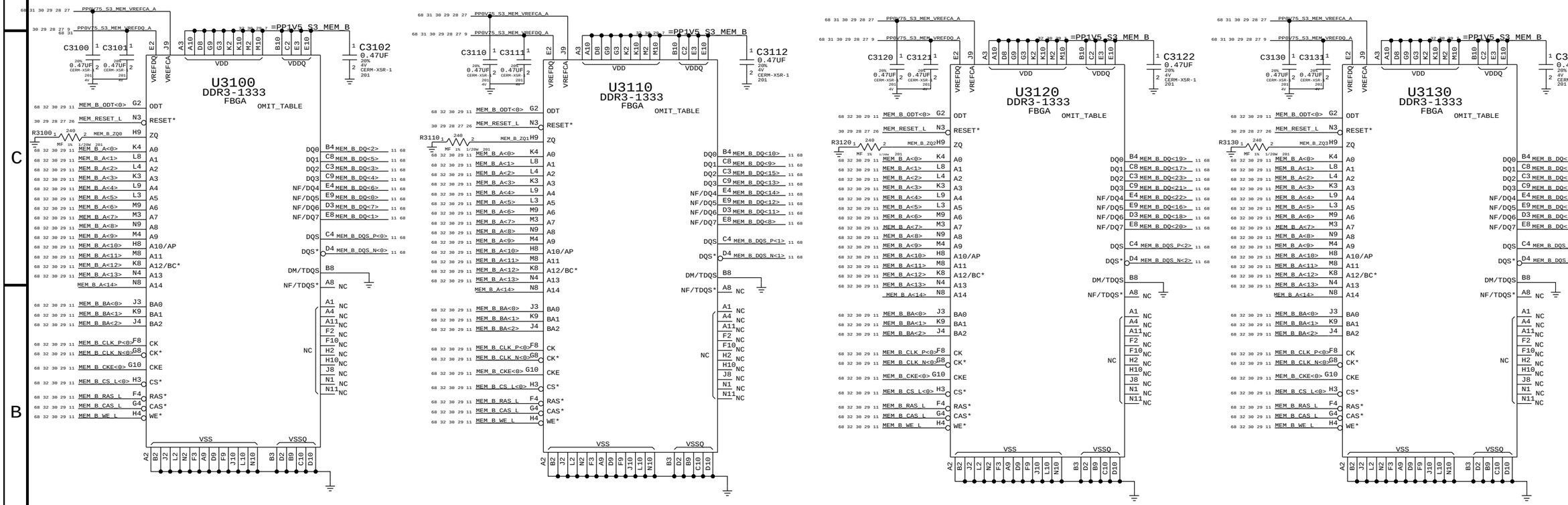
DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 30 OF 109

SHEET 28 OF 75



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K78_MLB SYNC_DATE=12/07/2010

PAGE TITLE
DDR3 DRAM CHANNEL B (0-31)

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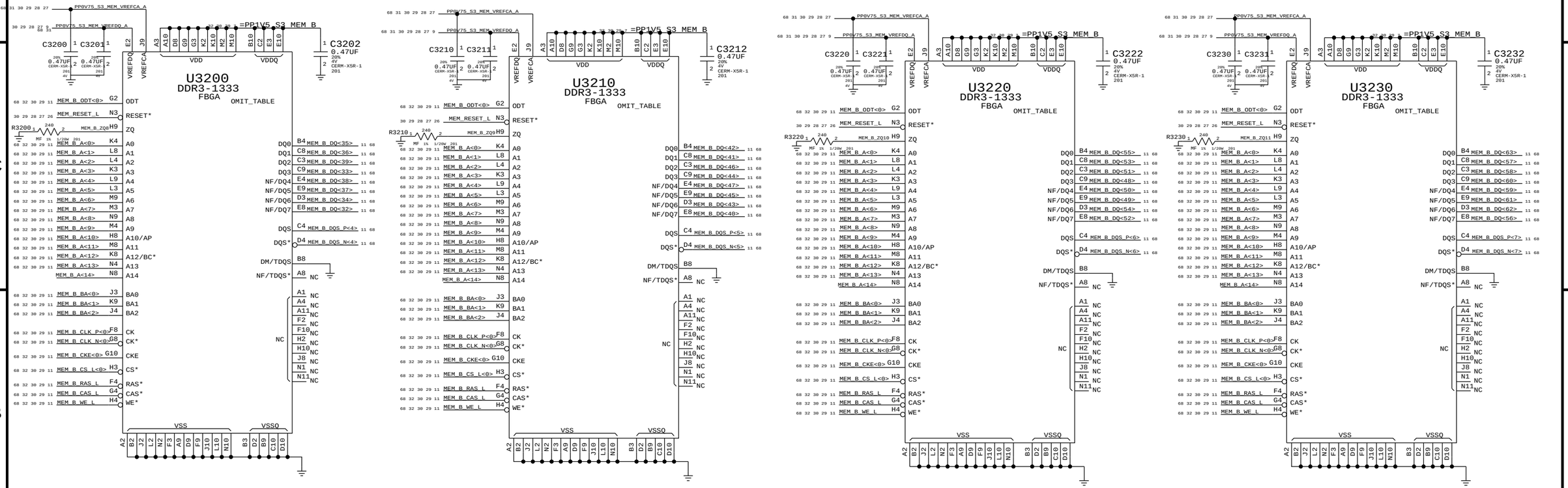
DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 31 OF 109
SHEET 29 OF 75



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K78_MLB SYNC_DATE=12/07/2010

PAGE TITLE
DDR3 DRAM CHANNEL B (32-63)

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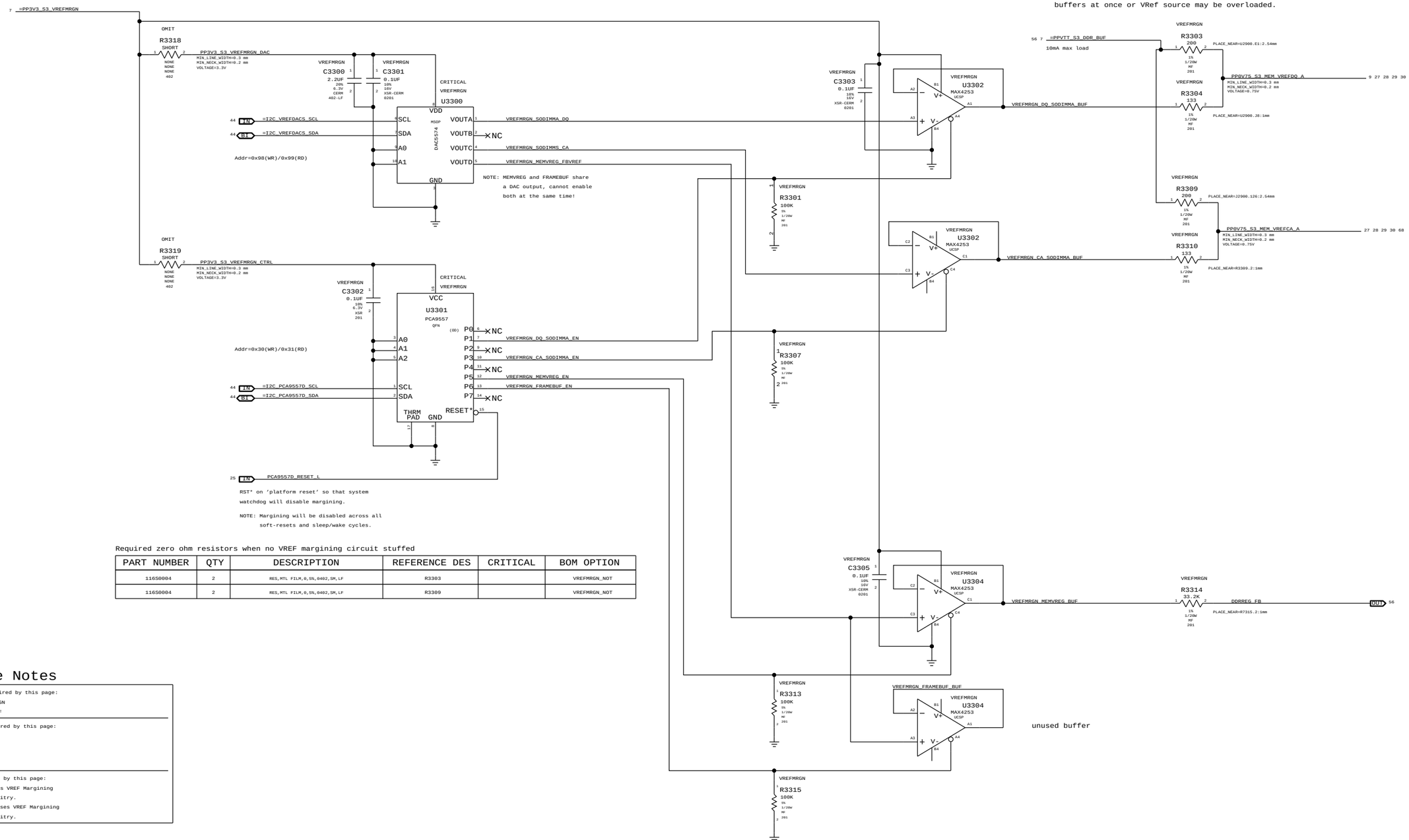
DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 32 OF 109
SHEET 30 OF 75



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

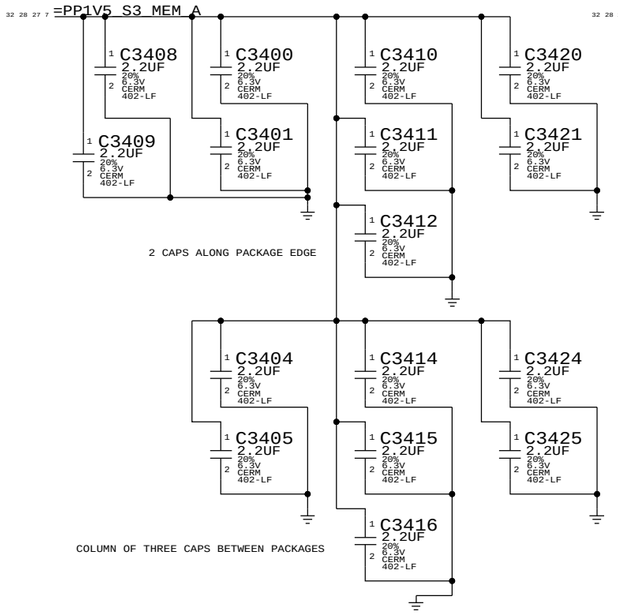
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

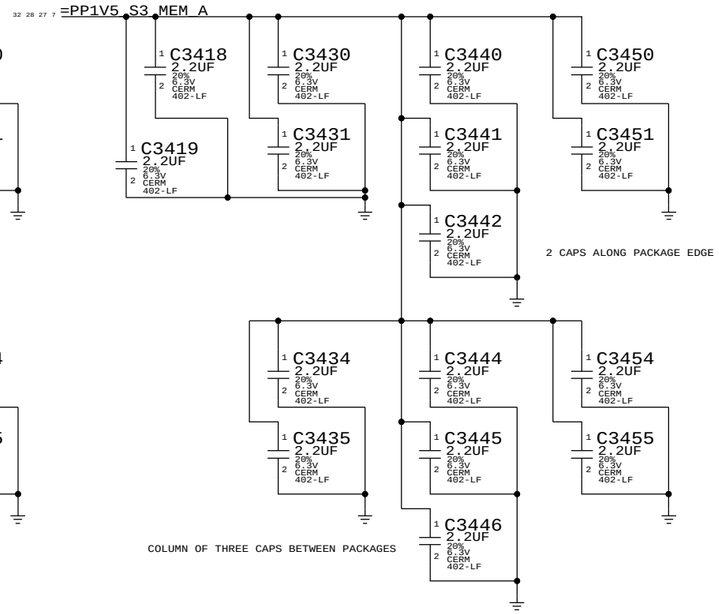
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2012

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

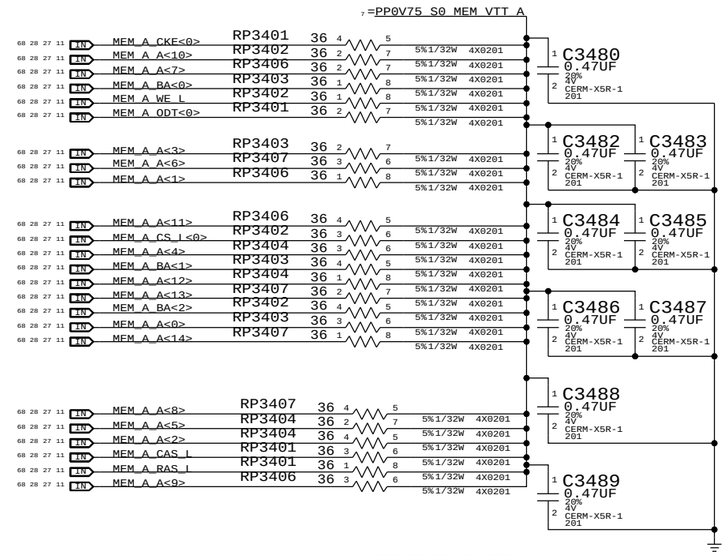
Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 33 OF 109
SHEET 31 OF 75



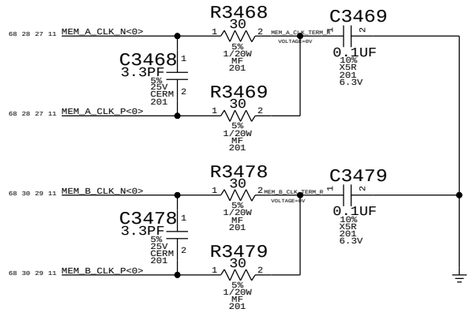


JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

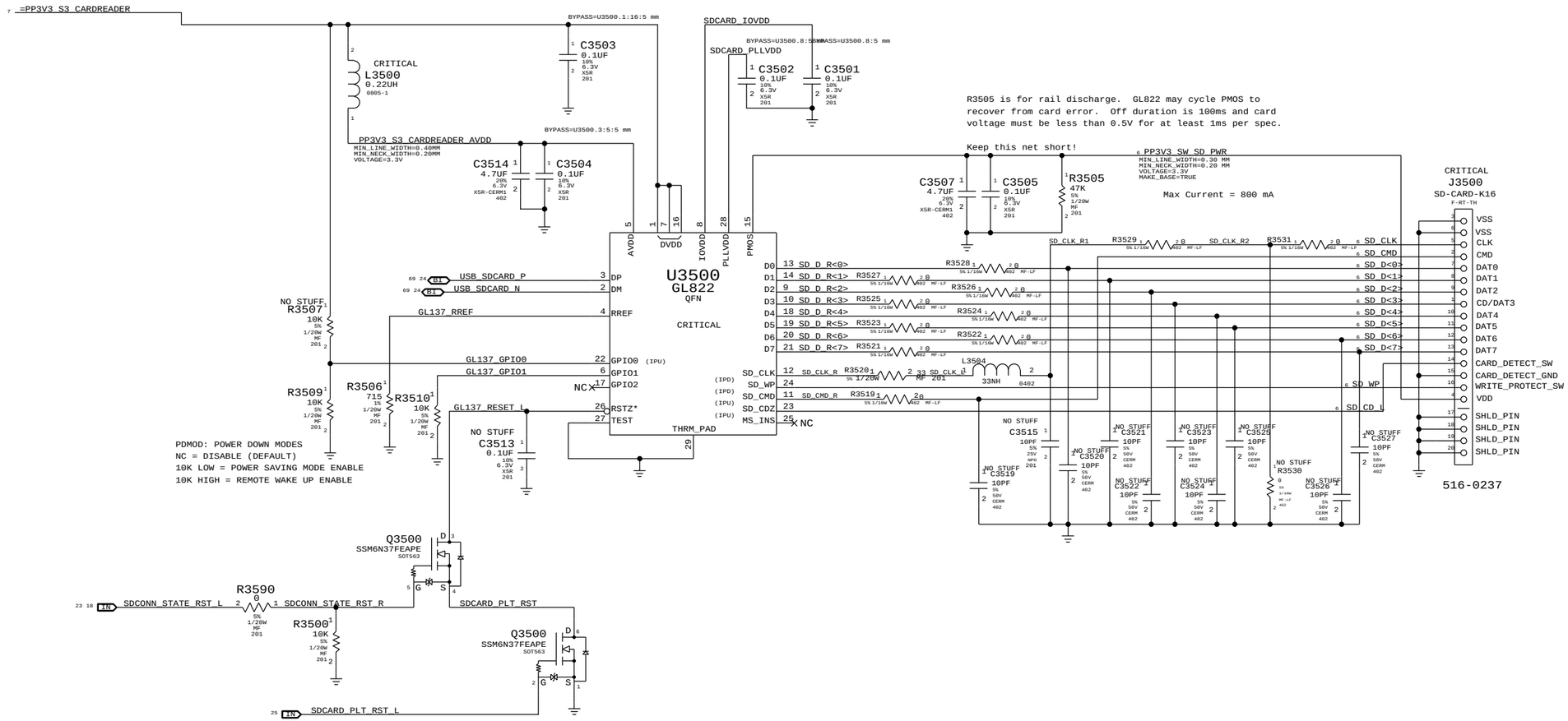


MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=K78_MLB	SYNC_DATE=12/16/2010
PAGE TITLE: DDR3 DRAM Channel B (32-63)	
Apple Inc.	DRAWING NUMBER: 051-8870 SIZE: D
	REVISION: 3.13.0
	BRANCH:
	PAGE: 34 OF 109
	SHEET: 32 OF 75



SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE

SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 35 OF 109

SHEET 33 OF 75

CRITICAL
OMIT_TABLE

U3600
EAGLE_RIDGE-192
FCBGA
(1 OF 2)

PCIE GEN2

RECEIVE

PCIE_T29_R2D_C_P<0>	C3600 0.1UF	PCIE_T29_R2D_P<0>	P14	PERP_0
PCIE_T29_R2D_C_N<0>	C3601 0.1UF	PCIE_T29_R2D_N<0>	P15	PERN_0
PCIE_T29_R2D_C_P<1>	C3602 0.1UF	PCIE_T29_R2D_P<1>	K14	PERP_1
PCIE_T29_R2D_C_N<1>	C3603 0.1UF	PCIE_T29_R2D_N<1>	K15	PERN_1
PCIE_T29_R2D_C_P<2>	C3604 0.1UF	PCIE_T29_R2D_P<2>	F14	PERP_2
PCIE_T29_R2D_C_N<2>	C3605 0.1UF	PCIE_T29_R2D_N<2>	F15	PERN_2
PCIE_T29_R2D_C_P<3>	C3606 0.1UF	PCIE_T29_R2D_P<3>	B15	PERP_3
PCIE_T29_R2D_C_N<3>	C3607 0.1UF	PCIE_T29_R2D_N<3>	B14	PERN_3

TRANSMIT

PETP_0	T14	PCIE_T29_D2R_C_P<0>	C3640 0.1UF	PCIE_T29_D2R_P<0>
PETN_0	T15	PCIE_T29_D2R_C_N<0>	C3641 0.1UF	PCIE_T29_D2R_N<0>
PETP_1	M14	PCIE_T29_D2R_C_P<1>	C3642 0.1UF	PCIE_T29_D2R_P<1>
PETN_1	M15	PCIE_T29_D2R_C_N<1>	C3643 0.1UF	PCIE_T29_D2R_N<1>
PETP_2	H14	PCIE_T29_D2R_C_P<2>	C3644 0.1UF	PCIE_T29_D2R_P<2>
PETN_2	H15	PCIE_T29_D2R_C_N<2>	C3645 0.1UF	PCIE_T29_D2R_N<2>
PETP_3	D14	PCIE_T29_D2R_C_P<3>	C3646 0.1UF	PCIE_T29_D2R_P<3>
PETN_3	D15	PCIE_T29_D2R_C_N<3>	C3647 0.1UF	PCIE_T29_D2R_N<3>

TP_T29_MONDC0 — R3610 0 (NO STUFF) — T29_MONDC0 — A14 MONDC0
DEBUG: For monitoring current/voltage
TP_T29_MONDC1 — R3611 0 (NO STUFF) — T29_MONDC1 — A15 MONDC1

TP_T29_MONOBSP — C3615 0.1UF — T29_MONOBSP — A13 MONOBSP
DEBUG: For monitoring clock
TP_T29_MONOBSN — C3616 0.1UF — T29_MONOBSN — B13 MONOBSN

WAKE* — M2 — T29_PCIE_WAKE_L — R3651 10K — =PP3V3_T29_RTR
PERST* — C2 — T29_RESET_L
RSENSE — C8 — T29_RSENSE — R3655 1.0K 0.1% 1/10W TF 402
RBIAS — C7 — T29_RBIAS

=PP3V3_T29_RTR

R3690 3.3K 5% 1/20W MF 201
R3691 3.3K 5% 1/20W MF 201
C3690 1.0UF 20% 6.3V X5R 0201-MUR
R3692 3.3K 5% 1/20W MF 201
R3693 3.3K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U3690
M95160
2KX8-1.8V
MLP

(T29_SPI_MOSI)	D	
(T29_SPI_CLK)	C	
(T29_SPI_CS_L)	S_L	
T29ROM_WP_L	W_L	
T29ROM_HOLD_L	HOLD_L	
VCC	8	
VSS	4	
THM PAD	9	
(T29_SPI_MISO)	Q	2

CLK REQUEST

=T29_CLKREQ_L — PCIE_CLKREQ_0* — P1

MISC

EEPROM

T29_SPI_MOSI	EE_DI	U6
T29_SPI_MISO	EE_DO	P2
T29_SPI_CS_L	EE_CS*	U3
T29_SPI_CLK	EE_CLK	N1

TP_T29_THERM_DP — THERM_DP — B2
Use B1 GND ball for THERM_DN

TEST PORT

T29_TEST_EN — TEST_EN — E2
R3625 0 5% 1/20W MF 201
T29_TEST_POINT_3 — TEST_PWR_GOOD — D1

R3629 0 5% 1/20W MF 201

POWER ON RESET

Not used in host mode.

PCIE_RST_0*	R1	TP_T29_PCIE_RESET0_L
PCIE_RST_1*	L1	TP_T29_PCIE_RESET1_L
PCIE_RST_2*	L2	TP_T29_PCIE_RESET2_L
PCIE_RST_3*	G2	TP_T29_PCIE_RESET3_L

JTAG

TDI	T3	JTAG_T29_TDI
TMS	T5	JTAG_T29_TMS
TCK	R2	JTAG_T29_TCK
TDO	U4	JTAG_T29_TDO

CLOCKS

REFCLK_100_IN_P	A12	PCIE_CLK100M_T29_P
REFCLK_100_IN_N	B12	PCIE_CLK100M_T29_N
XTAL_25_IN	D11	SYSCLK_CLK25M_T29_R
XTAL_25_OUT	C11	TP_T29_XTAL25OUT
TMU_CLK_OUT	U5	T29_TMU_CLK_OUT
TMU_CLK_IN	M1	T29_TMU_CLK_IN

=PP3V3_T29_RTR — R3698 10K — R3695 806 — SYSCLK_CLK25M_T29
R3696 1K
NO STUFF R3699 10K

SNK0 AC Coupling

DP_T29SNK0_ML_C_P<0>	C3620 0.1UF	DP_T29SNK0_ML_P<0>	T8	DPSNK0_ML_LANE_3P_IN0_HDMI_TMDS_CLK_P
DP_T29SNK0_ML_C_N<0>	C3621 0.1UF	DP_T29SNK0_ML_N<0>	U8	DPSNK0_ML_LANE_3N_IN0_HDMI_TMDS_CLK_N
DP_T29SNK0_ML_C_P<1>	C3622 0.1UF	DP_T29SNK0_ML_P<1>	T9	DPSNK0_ML_LANE_2P_IN0_HDMI_TMDS_O_P
DP_T29SNK0_ML_C_N<1>	C3623 0.1UF	DP_T29SNK0_ML_N<1>	U9	DPSNK0_ML_LANE_2N_IN0_HDMI_TMDS_0_N
DP_T29SNK0_ML_C_P<2>	C3624 0.1UF	DP_T29SNK0_ML_P<2>	T10	DPSNK0_ML_LANE_1P_IN0_HDMI_TMDS_1_P
DP_T29SNK0_ML_C_N<2>	C3625 0.1UF	DP_T29SNK0_ML_N<2>	U10	DPSNK0_ML_LANE_1N_IN0_HDMI_TMDS_1_N
DP_T29SNK0_ML_C_P<3>	C3626 0.1UF	DP_T29SNK0_ML_P<3>	T11	DPSNK0_ML_LANE_0P_IN0_HDMI_TMDS_2_P
DP_T29SNK0_ML_C_N<3>	C3627 0.1UF	DP_T29SNK0_ML_N<3>	U11	DPSNK0_ML_LANE_0N_IN0_HDMI_TMDS_2_N
DP_T29SNK0_AUXCH_C_P	C3628 0.1UF	DP_T29SNK0_AUXCH_P	T7	DPSNK0_AUX_CHP
DP_T29SNK0_AUXCH_C_N	C3629 0.1UF	DP_T29SNK0_AUXCH_N	U7	DPSNK0_AUX_CHN

SINK PORT 0

DPSRC0_ML_LANE_3P_OUT0_HDMI_TMDS_2_P	T12	DP_T29SRC_ML_CP<3>	R3661 0
DPSRC0_ML_LANE_3N_OUT0_HDMI_TMDS_2_N	U12	DP_T29SRC_ML_CN<3>	R3662 0
DPSRC0_ML_LANE_0P_OUT0_HDMI_TMDS_CLK_P	N12	DP_T29SRC_ML_CP<0>	R3663 0
DPSRC0_ML_LANE_0N_OUT0_HDMI_TMDS_CLK_N	R12	DP_T29SRC_ML_CN<0>	R3664 0

=PP3V3_T29_RTR
100pF SRF > 40MHz

SOURCE PORT 0

DP_T29SNK0_HPD — T4 — DPSNK0_HDMI_IN_HOT_PLUG_DET
R3630 100K 5% 1/20W MF 201

DPSRC0_HOT_PLUG_DET — T6 — DP_T29SRC_HPD
DP_ATEST — U15 — T29_DP_ATEST
DP_RES — U14 — T29_DP_RES
C3685 100PF 5% 25V CERM 201
C3686 0.01UF 10% 10V X5R 201

HDMI/
DISPLAYPORT

TP_T29_HDMI_5V_OUT — U1 — HDMI_5V_OUT

HDMI

HDMI_SCL_IN	B1	T29_HDMI_SCL_IN	R3685 14K 1% 1/20W MF 201
HDMI_SDA_IN	A2	T29_HDMI_SDA_IN	R3632 100K 5% 1/20W MF 201
HDMI_OUT_HOT_PLUG_DET	F3	T29_HDMI_OUT_HPD	

=PP3V3_T29_RTR
R3670 10K
R3671 10K
T29_HDMI_SCL_IN
T29_HDMI_SDA_IN
T29_CIO_PLUG_EVENT
T29_HDMI_OUT_HPD
R3673 10K
R3674 10K

PORTS

PORT0

PRT0_CIOT_P	A6	T29_R2D_C_P<0>	OUT
PRT0_CIOT_N	B6	T29_R2D_C_N<0>	OUT
PRT0_CIOR_P	A4	T29_D2R_P<0>	IN
PRT0_CIOR_N	B4	T29_D2R_N<0>	IN
CIO_0_LSEO	H2	T29_LSEO<0>	OUT
CIO_0_LSOE	K1	T29_LSOE<0>	IN

PORT1

PRT1_CIOT_P	B10	T29_R2D_C_P<1>	OUT
PRT1_CIOT_N	A10	T29_R2D_C_N<1>	OUT
PRT1_CIOR_P	A8	T29_D2R_P<1>	IN
PRT1_CIOR_N	B8	T29_D2R_N<1>	IN
CIO_1_LSEO	J1	T29_LSEO<1>	OUT
CIO_1_LSOE	K2	T29_LSOE<1>	IN

CIO_PLUG_EVENT — H1 — T29_CIO_PLUG_EVENT

I2C_T29_SCL — C1 — CIO_MDC
I2C_T29_SDA — F1 — CIO_MDIO

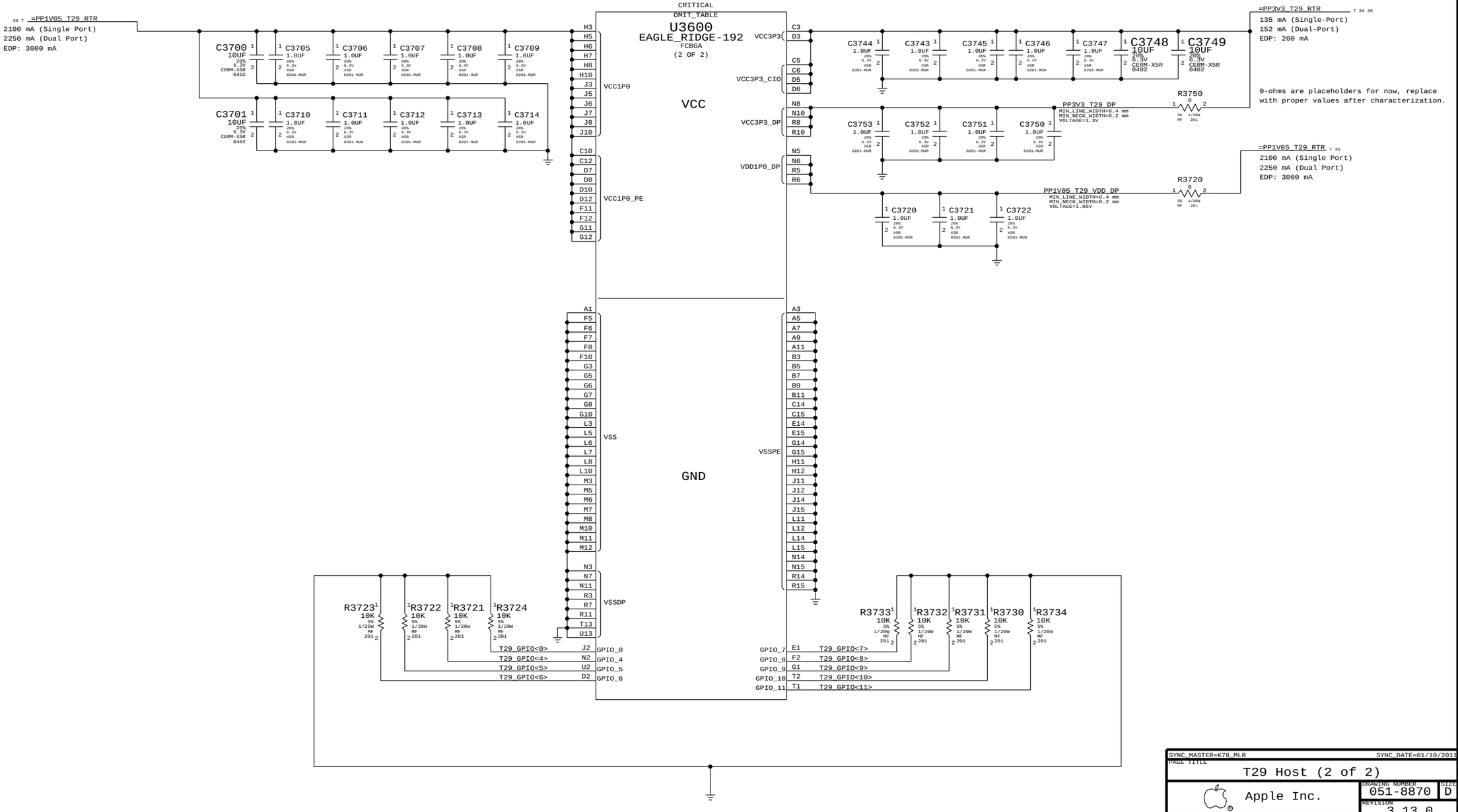
NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SYNC_MASTER=K78_MLB — SYNC_DATE=01/10/2013

PAGE TITLE: T29 Host (1 of 2)

Apple Inc.

DRAWING NUMBER: 051-8870 — SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 36 OF 109
SHEET: 34 OF 75



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 37 OF 109

SHEET: 35 OF 75

Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 18V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_T29BST
8-13V Input
Changes required for 2S.

R3820 0.010 1% 1/4W MF 805 (PPVIN_SW_T29BST_R)
Q3880 SI8409DB 8GA (CRITICAL)
=PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

R3880 470K 5% 1/20W MF 201
C3880 0.1UF 10% 25V X5R 402
T29BST_PWREN_DIV_L
R3881 150K 5% 1/20W MF 201
T29BST_PWREN_L
Q3805 SSM3K15FV SOD-VESM-HF
T29_A_HV_EN

R3891 200K 1% 1/20W MF 201 <R1>
C3890 10UF 10% 25V X5R 805
C3891 10UF 10% 25V X5R 805

L3895 6.8UH-4.0A (CRITICAL) PIMB062D-SM
T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

U3890 LT3957 QFN (CRITICAL)
VIN, SW
T29BST_SNS1, T29BST_SNS2
R3889 0 5% 1/20W MF 201
D3895 POWERDI-123 DFLS230L
XW3895 SM
PLACE_NEAR=C3895.1:2 mm

T29BST_EN_UVLO
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
T29BST_VC_RC
T29BST_FBX
GND_T29BST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

C3892 4.7UF 10% 10V X5R 805
C3887 47PF 5% 25V NP0-C0G 201
R3893 10K 1% 1/20W MF 201
R3892 73.2K 1% 1/20W MF 201 <R2>
C3893 3300PF 10% 10V X7R 201
R3894 41.2K 1% 1/20W MF 201
C3894 0.33UF 10% 6.3V CERM-X5R 402

NC, XNC
C3888 10PF 5% 50V CERM 402
R3895 133K 1% 1/10W MF-LF 402 <Ra>
NO STUFF
C3889 100PF 5% 50V CERM 402
R3896 15.8K 1% 1/10W MF-LF 402 <Rb>

=PP15V_T29_REG
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

C3895 4.7UF 10% 50V X7R-CERM 1206
C3896 4.7UF 10% 50V X7R-CERM 1206
C3897 4.7UF 10% 50V X7R-CERM 1206
C3898 4.7UF 10% 50V X7R-CERM 1206
C3899 0.001UF 10% 50V X7R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Vout = 1.6V * (1 + Ra / Rb)

SGND shorted to GND inside package, no XW necessary.

Q3888 SSM6N37FEAPE SOT563 (Max Vgs: 10V)
T29BST_SHDN_DIV
R3888 330K 5% 1/20W MF 201
R3887 330K 5% 1/20W MF 201
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

=PP3V3_S0_T29PWRCTL
C3800 0.1UF 10% 16V X5R-CERM 0201
U3800 SLG4AP016V TDFN (CRITICAL)
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD

Platform (PCIe) Reset
=T29_RESET_L
R3803 10K 5% 1/20W MF 201
Open-Drain GPIO
T29_SW_RESET_L
T29_CLKREQ_L
Pull-up provided by SB page.

=PP3V3_T29_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_T29
T29_RESET_L
DLY = 60 ms +/- 20%
=T29_CLKREQ_L
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V T29 Switch

=PP3V3_S0_P3V3T29FET
U3810 TPS22924 CSP (CRITICAL)
VIN, VOUT, ON, GND
C3810 1UF 10% 6.3V CERM 402
=PP3V3_T29_FET
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

=PP1V05_S0_P1V05T29FET
U3815 TPS22924 CSP (CRITICAL)
C3815 1UF 10% 6.3V CERM 402
=PP1V05_T29_FET
Max Current = 3.4A (85C)

U3816 TPS22924 CSP (CRITICAL)
T29_PWR_EN
U3816.A2: PLACE_NEAR=U3815.B2:3 mm
Pull-up provided by SB page.

SYNC_MASTER=K78_MLB
SYNC_DATE=01/10/2013
PAGE TITLE: T29 Power Support
Apple Inc.
DRAWING NUMBER: 051-8870
SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 38 OF 109
SHEET: 36 OF 75

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L OUT 6 41

70 6 PCIE_AP_R2D_N — C4030 0.1UF 10% 6.3V 201 X5R — PCIE_AP_R2D_C_N IN 16 70
PLACEMENT_NOTE=Place close to J4001.

70 6 PCIE_AP_R2D_P — C4031 0.1UF 10% 6.3V X5R 201 — PCIE_AP_R2D_C_P IN 16 70
PLACEMENT_NOTE=Place close to J4001.

PCIE_CLK100M_AP_N IN 6 16 70
PCIE_CLK100M_AP_P IN 6 16 70

PCIE_AP_D2R_P OUT 6 16 70
PCIE_AP_D2R_N OUT 6 16 70

PCIE_WAKE_L OUT 6 17

BLUETOOTH

USB_BT_N BI 6 24 69
USB_BT_P BI 6 24 69

=PP3V3_S3_BT 6 7

C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.18:1.5mm

MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

PP3V3_WLAN_F 5 — C4021 0.1UF 10% 6.3V X5R 201 — C4020 10UF 20% 6.3V X5R 603
PLACEMENT_NOTE=Place close to Q4050.

CRITICAL
R4052 0.020 1% 0.25W MF 805

PP3V3_WLAN_R 4

CRITICAL
Q4050
TPCP8102
23V1K-SM

C4050 0.1UF 10% 16V X5R-CERM 0201

P3V3WLAN_SS

C4051 0.033UF 10% 16V X5R 402

R4050 100K 5% 1/20W MF 201

R4051 10K 5% 1/20W MF 201

=PP3V3_S3_WLAN 7 37

PM_WLAN_EN_L IN 62

ISNS_AIRPORT_P OUT 46 74
ISNS_AIRPORT_N OUT 46 74

DLY = 60 MS +/- 20%

=PP3V3_S3_WLAN 7 37

C4053 0.1UF 10% 6.3V X5R 201

CRITICAL
U4002
SLG4AP016V
TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND

R4053 100K 1% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
R4055 100K 1% 1/20W MF 201

P3V3WLAN_VMON
AP_RESET_CONN_L 6
AP_CLKREQ_O_L 6

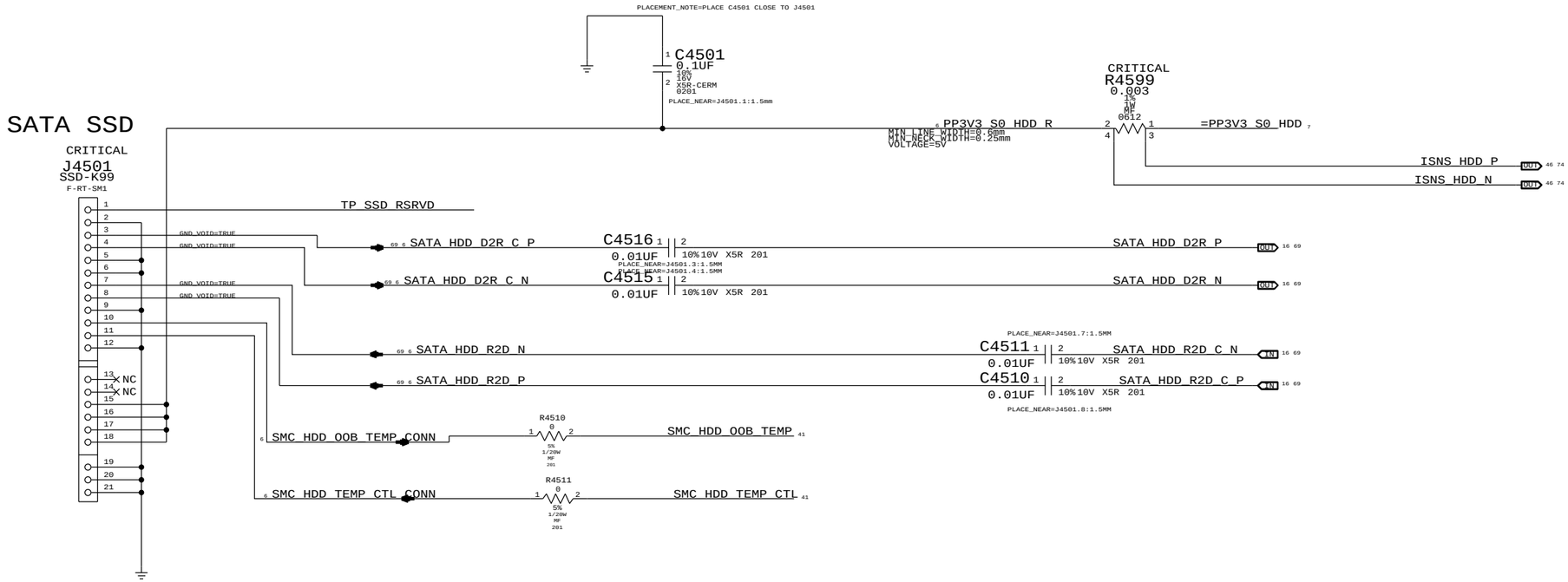
AP_RESET_L IN 25
AP_PWR_EN IN 18 62
AP_CLKREQ_L_R — R4090 0 5% 1/20W MF 201 — AP_CLKREQ_L OUT 16 23

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 40 OF 109
SHEET 37 OF 75



SYNC MASTER=K78_MLB SYNC DATE=01/10/2013

PAGE TITLE

SATA CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

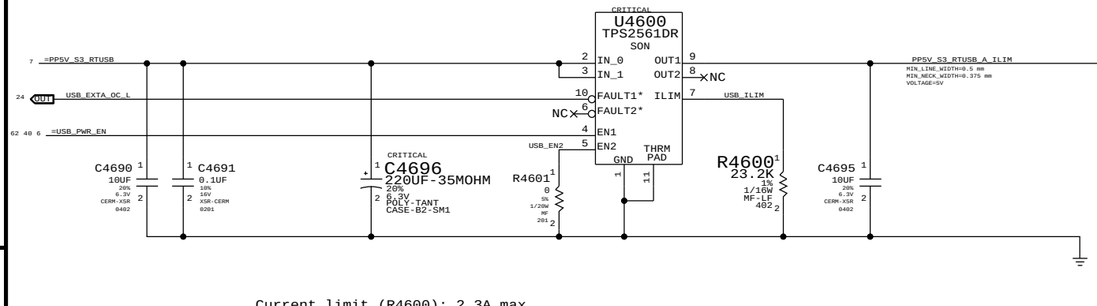
REVISION 3.13.0

BRANCH

PAGE 45 OF 109

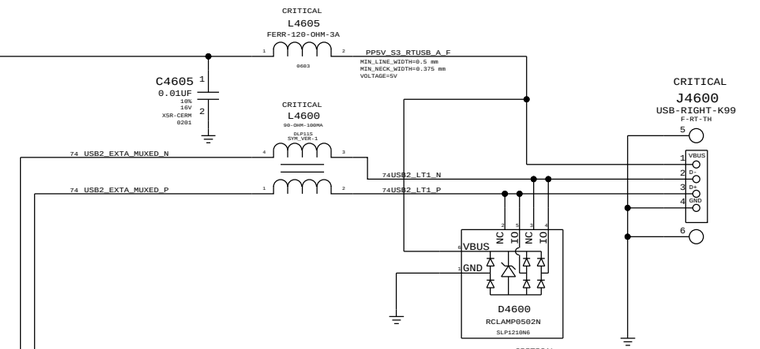
SHEET 38 OF 75

USB Port Power Switch



Current limit (R4600): 2.3A max

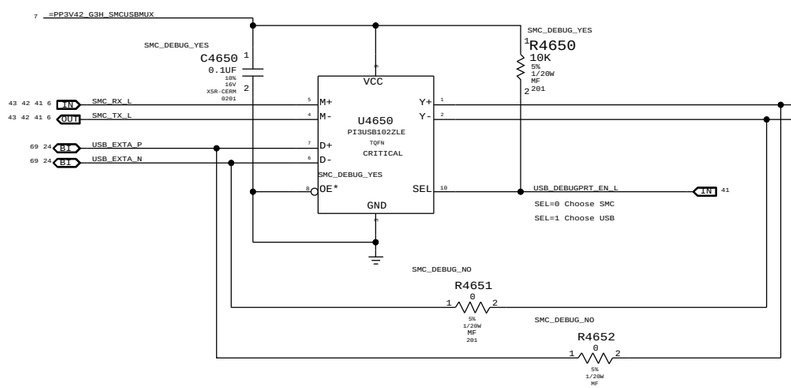
Right USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4605 at connector pin

USB/SMC Debug Mux



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

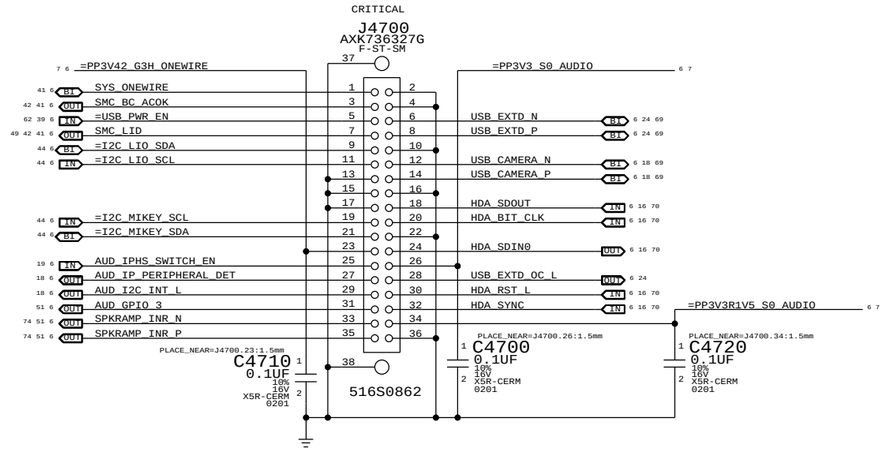
REVISION 3.13.0

BRANCH

PAGE 46 OF 109

SHEET 39 OF 75

(Right Speaker Enable)



SYNC_MASTER=K21_MLB SYNC_DATE=11/09/2010

PAGE TITLE

Left I/O (LIO) Connector

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

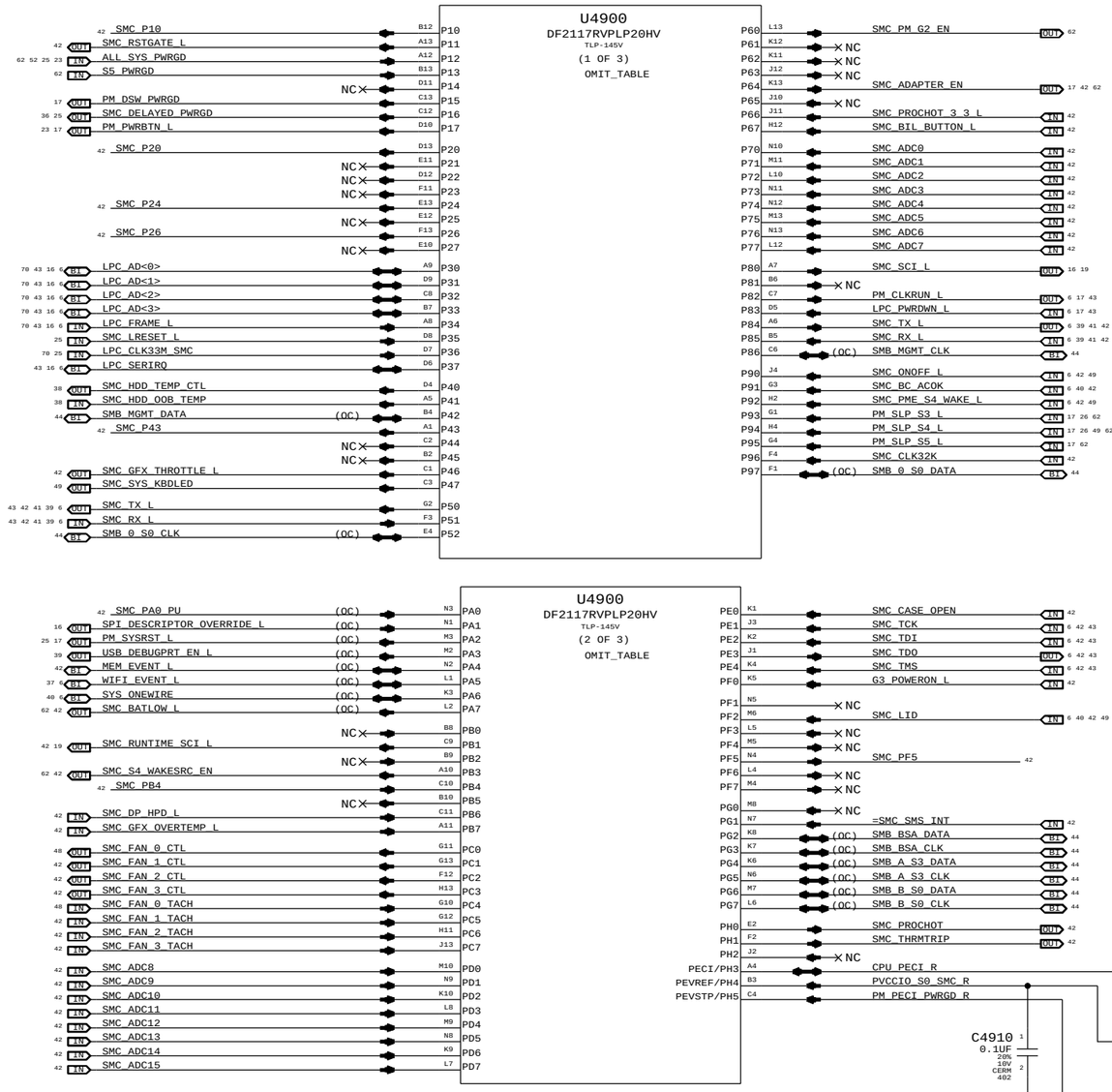
REVISION 3.13.0

BRANCH

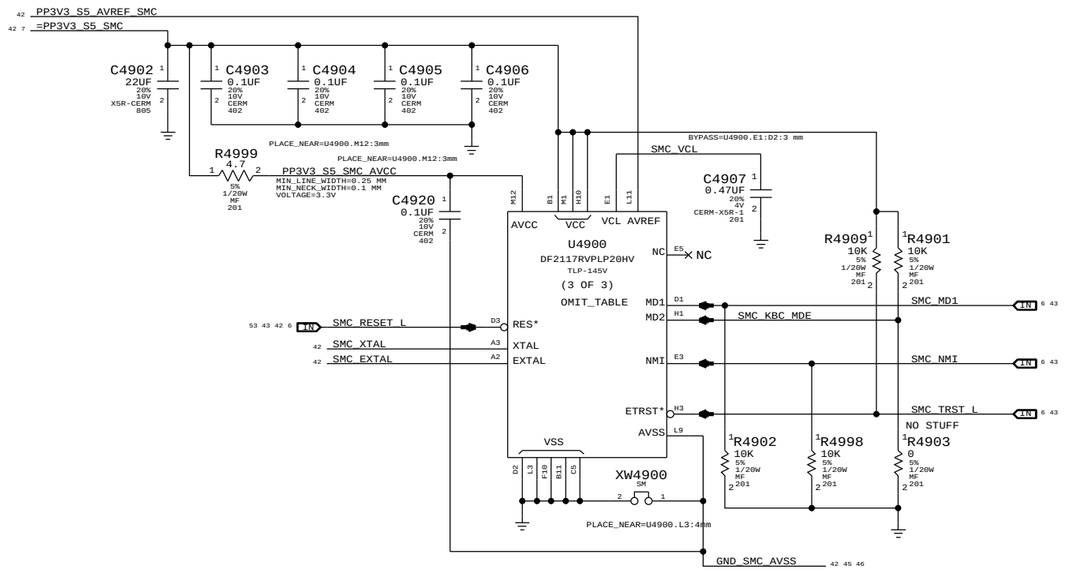
PAGE 47 OF 109

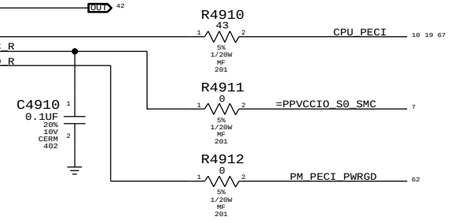
SHEET 40 OF 75

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.





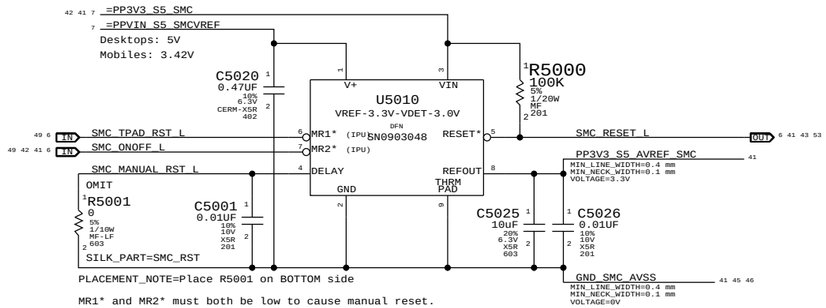
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 49 OF 109
SHEET: 41 OF 75

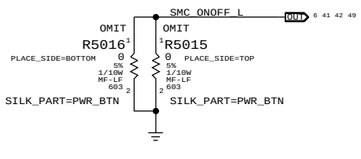
SMC Reset "Button", Supervisor & AVREF Supply



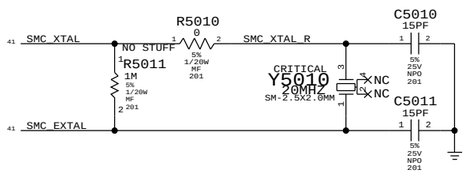
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

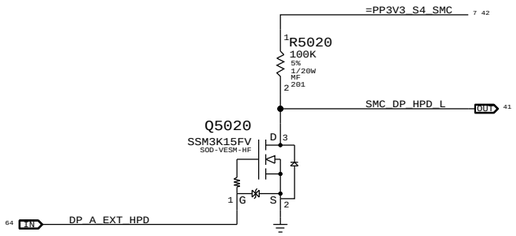
NOTE: Internal pull-ups are to VIN, not V+.

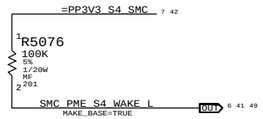
Debug Power "Buttons"

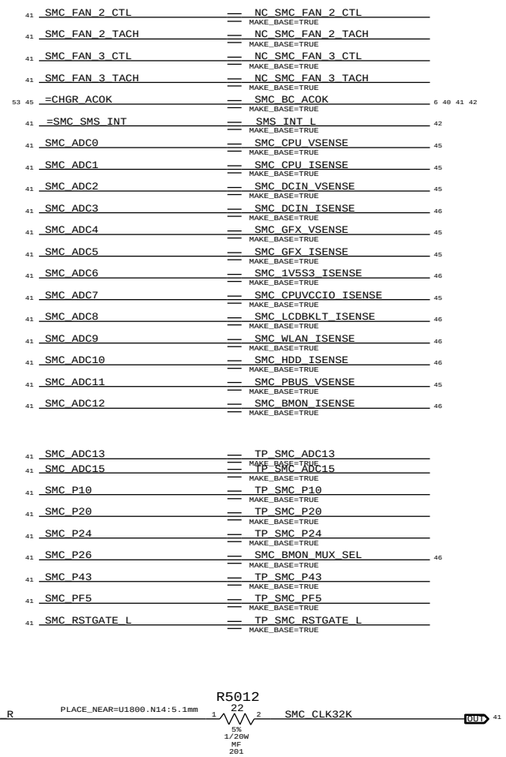


SMC Crystal Circuit

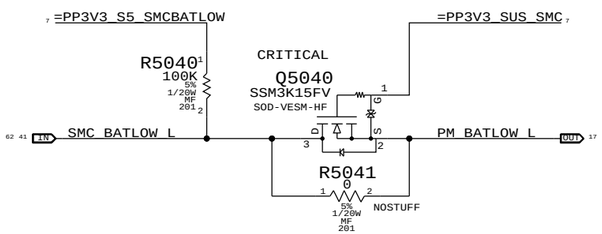






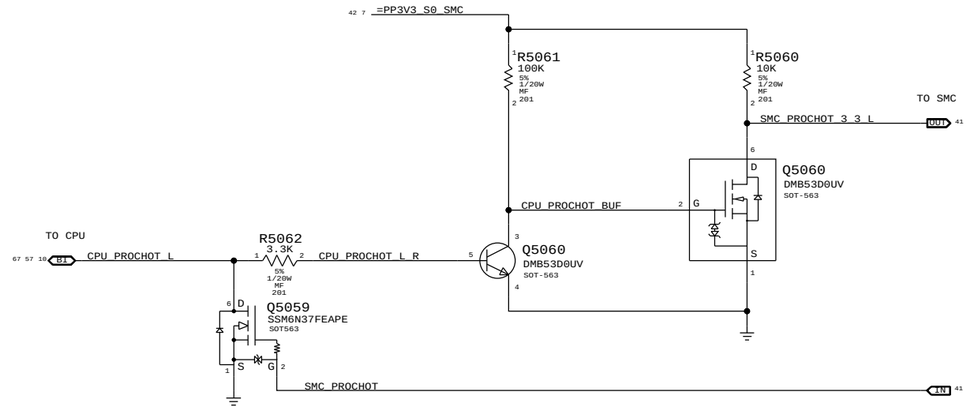


BATLOW# Isolation

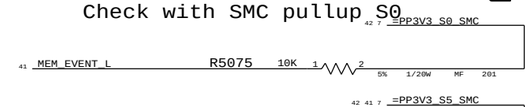


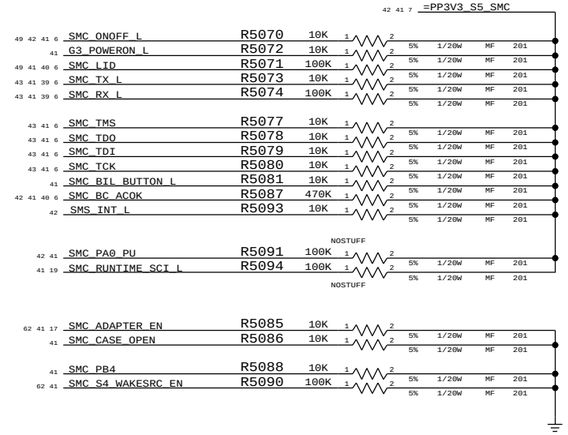
Internal 20K pull-up on PM_BATLOW_L in PCH.

PROCHOT Level Shifting to 3V3



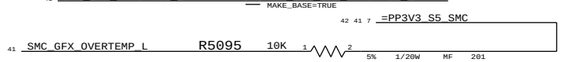
Check with SMC pullup S0





Below connections are different from K91

SMC_PA0_PU — HISIDE_ISENSE_OC (MAKE_BASE=TRUE)
SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL (MAKE_BASE=TRUE)
SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH (MAKE_BASE=TRUE)
SMC_ADC14 — SMC_HS_COMPUTING_ISENSE (MAKE_BASE=TRUE)
SMC_GFX_THROTTLE_L — TP_SMC_GFX_THROTTLE_L (MAKE_BASE=TRUE)



SMC_FAN_2_CTL — NC_SMC_FAN_2_CTL (MAKE_BASE=TRUE)
SMC_FAN_2_TACH — NC_SMC_FAN_2_TACH (MAKE_BASE=TRUE)
SMC_FAN_3_CTL — NC_SMC_FAN_3_CTL (MAKE_BASE=TRUE)
SMC_FAN_3_TACH — NC_SMC_FAN_3_TACH (MAKE_BASE=TRUE)
=CHGR_ACOK — SMC_BC_ACOK (MAKE_BASE=TRUE)
=SMC_SMS_INT — SMS_INT_L (MAKE_BASE=TRUE)
SMC_ADC0 — SMC_CPU_VSENSE (MAKE_BASE=TRUE)
SMC_ADC1 — SMC_CPU_ISENSE (MAKE_BASE=TRUE)
SMC_ADC2 — SMC_DCIN_VSENSE (MAKE_BASE=TRUE)
SMC_ADC3 — SMC_DCIN_ISENSE (MAKE_BASE=TRUE)
SMC_ADC4 — SMC_GFX_VSENSE (MAKE_BASE=TRUE)
SMC_ADC5 — SMC_GFX_ISENSE (MAKE_BASE=TRUE)
SMC_ADC6 — SMC_1V553_ISENSE (MAKE_BASE=TRUE)
SMC_ADC7 — SMC_CPUVCCIO_ISENSE (MAKE_BASE=TRUE)
SMC_ADC8 — SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE)
SMC_ADC9 — SMC_WLAN_ISENSE (MAKE_BASE=TRUE)
SMC_ADC10 — SMC_HDD_ISENSE (MAKE_BASE=TRUE)
SMC_ADC11 — SMC_PBUS_VSENSE (MAKE_BASE=TRUE)
SMC_ADC12 — SMC_BMON_ISENSE (MAKE_BASE=TRUE)
SMC_ADC13 — TP_SMC_ADC13 (MAKE_BASE=TRUE)
SMC_ADC15 — TP_SMC_ADC15 (MAKE_BASE=TRUE)
SMC_P10 — TP_SMC_P10 (MAKE_BASE=TRUE)
SMC_P20 — TP_SMC_P20 (MAKE_BASE=TRUE)
SMC_P24 — TP_SMC_P24 (MAKE_BASE=TRUE)
SMC_P26 — SMC_BMON_MUX_SEL (MAKE_BASE=TRUE)
SMC_P43 — TP_SMC_P43 (MAKE_BASE=TRUE)
SMC_PF5 — TP_SMC_PF5 (MAKE_BASE=TRUE)
SMC_RSTGATE_L — TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)

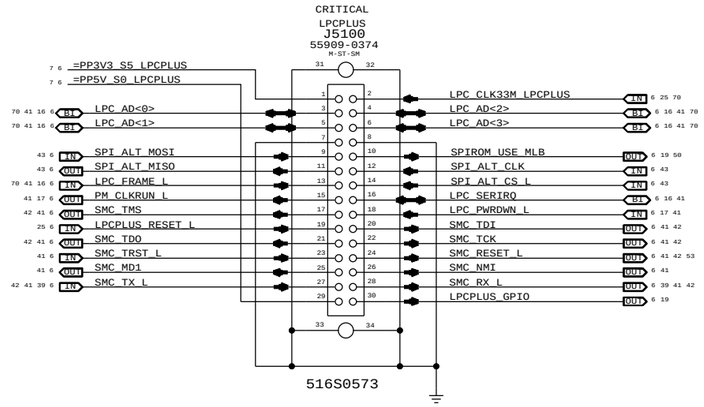
SYNC_MASTER=K78_MLB
SYNC_DATE=01/10/2013

PAGE TITLE: SMC Support

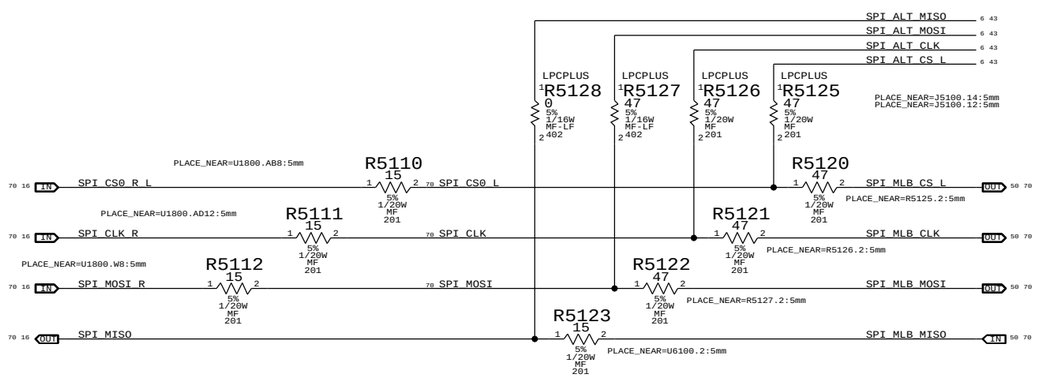
Apple Inc.

DRAWING NUMBER: 051-8870
SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 50 OF 109
SHEET: 42 OF 75

LPC+SPI Connector



SPI Bus Series Termination



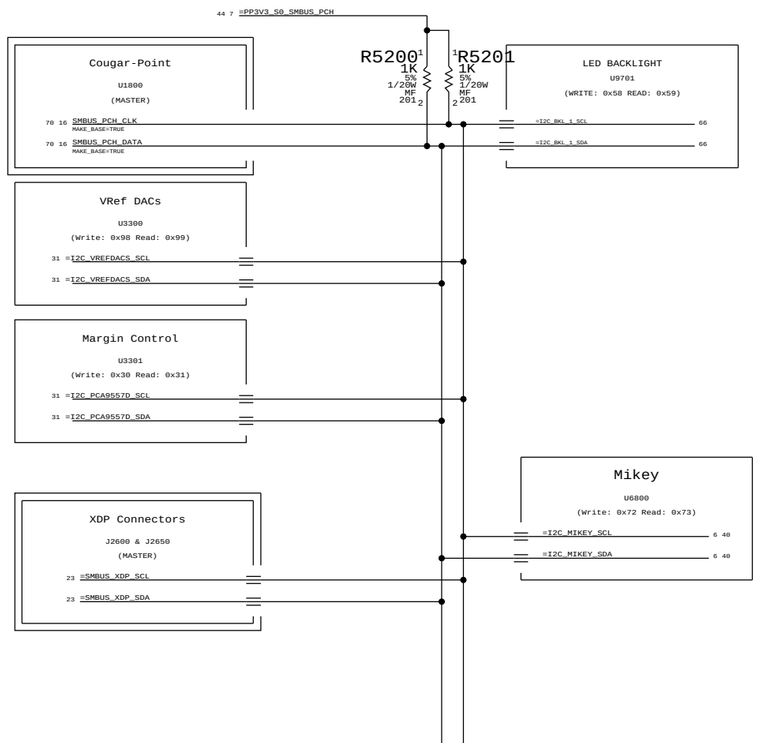
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE: LPC+SPI Debug Connector

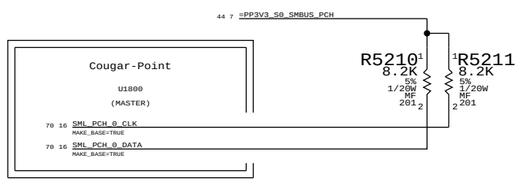
Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 51 OF 109
SHEET: 43 OF 75

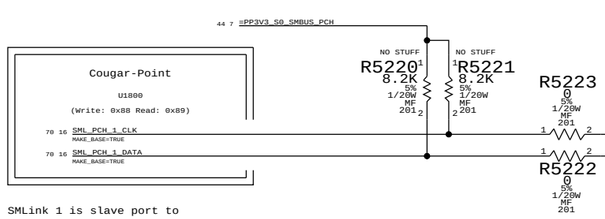
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

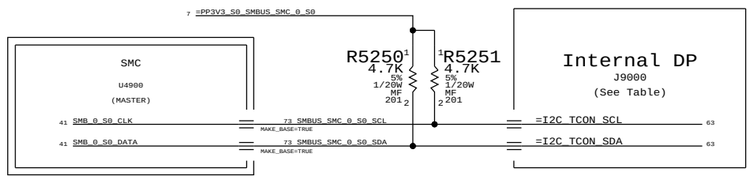


PCH "SMLink 1" Connections



SMLink 1 is slave port to
access PCH & CPU via PECI.

SMC "0" SMBus Connections



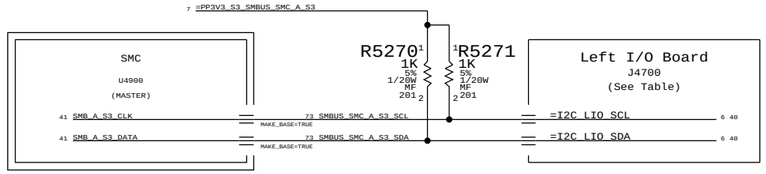
(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "A" SMBus Connections

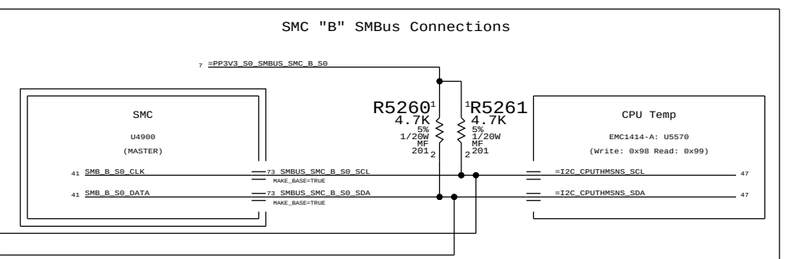
NOTE: SMC RMT bus remains powered and may be active in S3 state



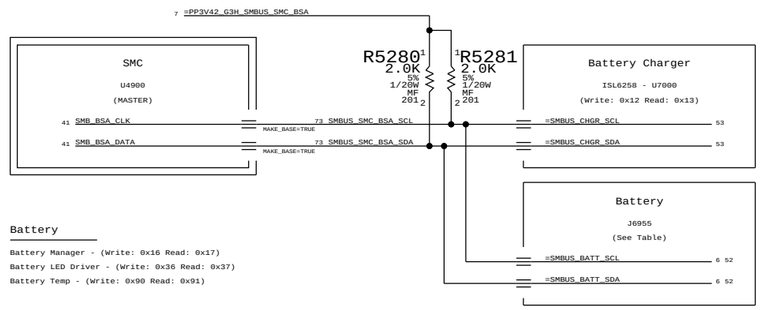
Left I/O Board

ALS - (write: 0x72 Read: 0x73)
Finstack Temp - (Write: 0x92 Read: 0x93)

SMC "B" SMBus Connections



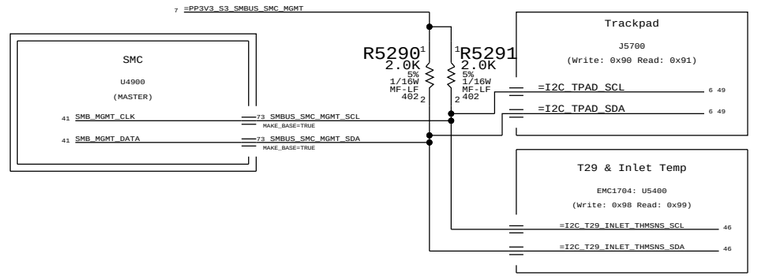
SMC "Battery A" SMBus Connections



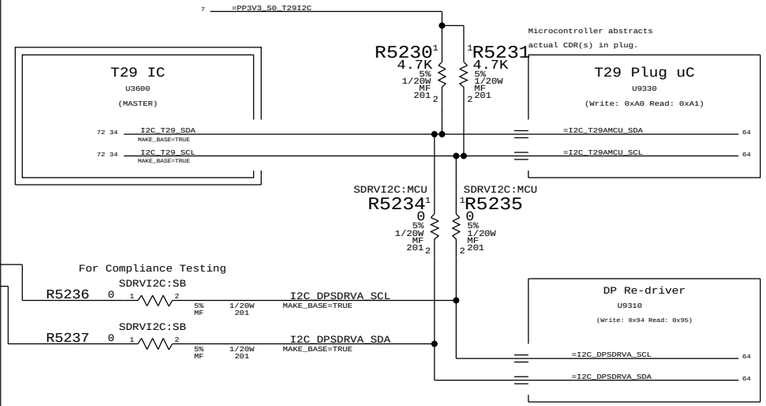
Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections



T29 I2C Connections



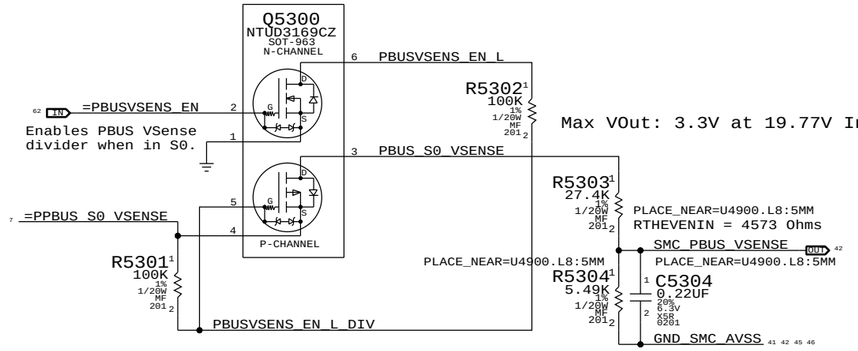
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2017

PAGE TITLE: SMBus Connections

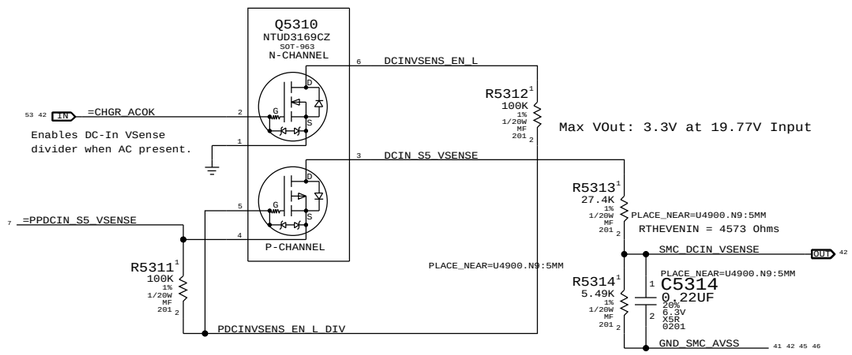
Apple Inc.

DRAWING NUMBER: 051-8870
SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 52 OF 109
SHEET: 44 OF 75

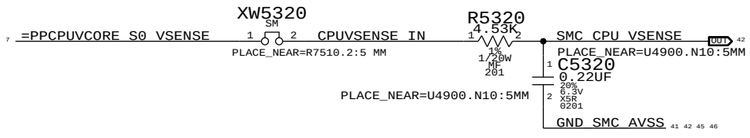
PBUS Voltage Sense Enable & Filter



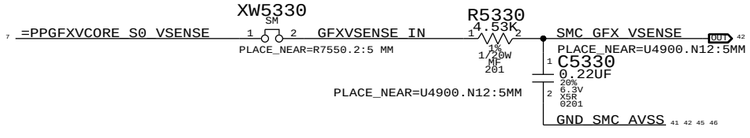
DC-In Voltage Sense Enable & Filter



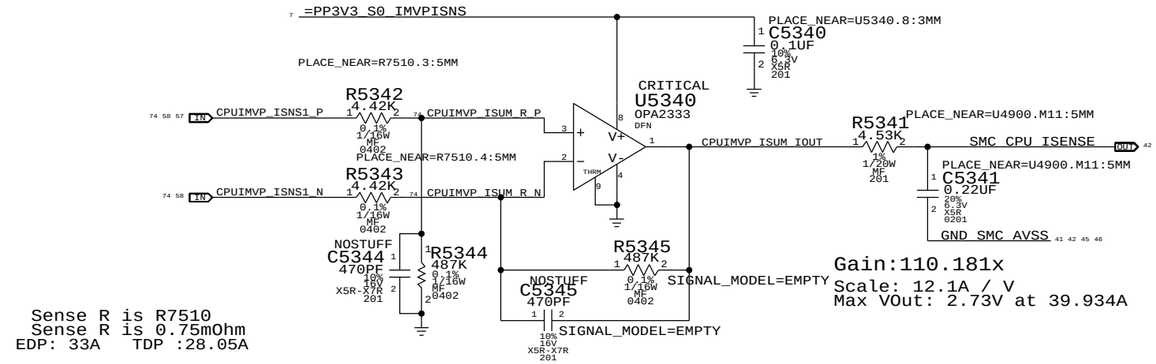
CPU Vcore Voltage Sense / Filter



GFX/IG Vcore Voltage Sense / Filter

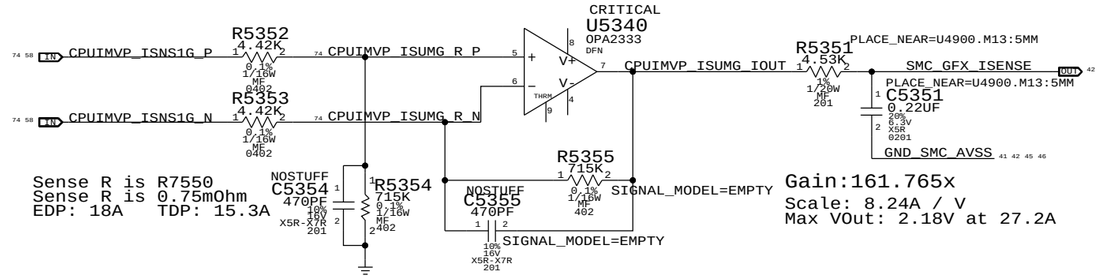


CPU VCore Load Side Current Sense / Filter



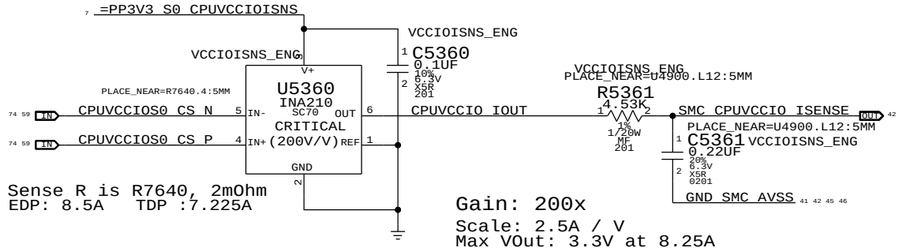
Sense R is R7510
Sense R is 0.75mOhm
EDP: 33A TDP :28.05A

GFX/IG VCore Load Side Current Sense / Filter



Sense R is R7550
Sense R is 0.75mOhm
EDP: 18A TDP: 15.3A

CPU 1.05V VCCIO Current Sense / Filter



Sense R is R7640, 2mOhm
EDP: 8.5A TDP :7.225A

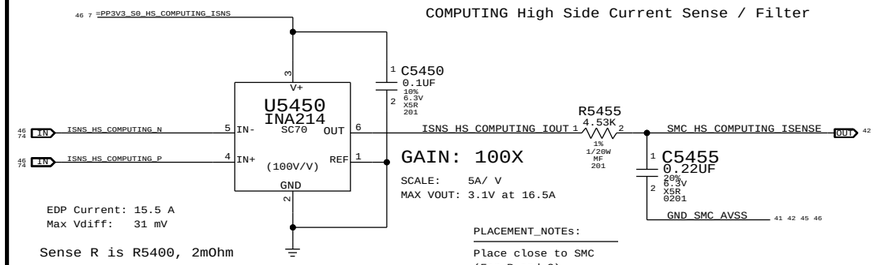
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE
Voltage & Load Side Current Sensing

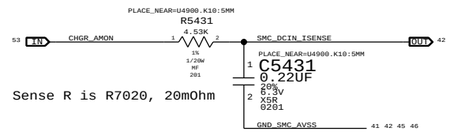
Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 53 OF 109
SHEET 45 OF 75

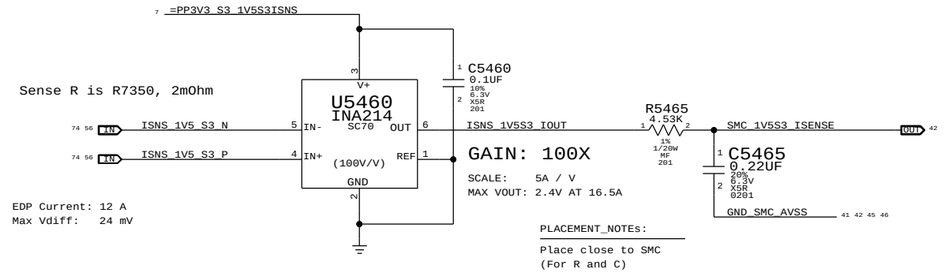
COMPUTING High Side Current Sense / Filter



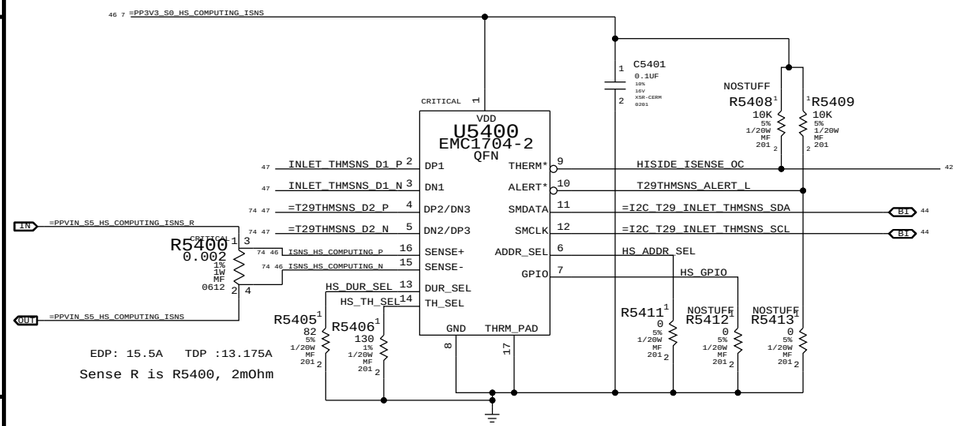
DC-IN (AMON) Current Sense Filter



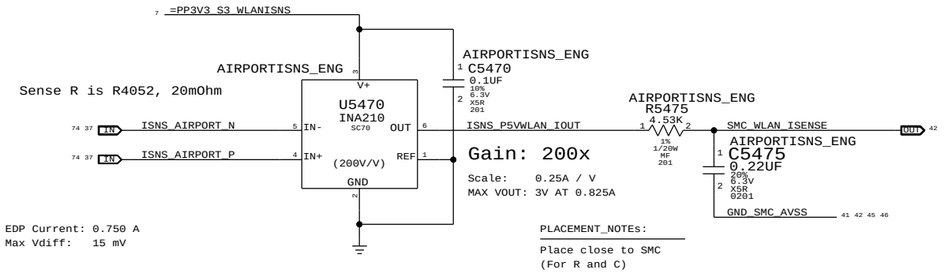
DDR3 1V5R1V35 Current Sense / Filter



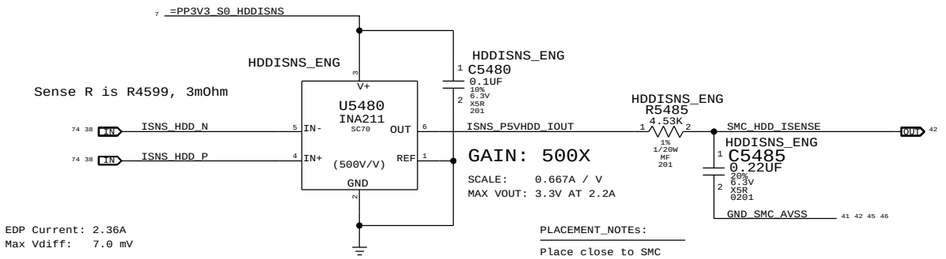
COMPUTING High Side Current Sense / Filter & T29/Inlet Temp Sensor



AirPort Current Sense / Filter

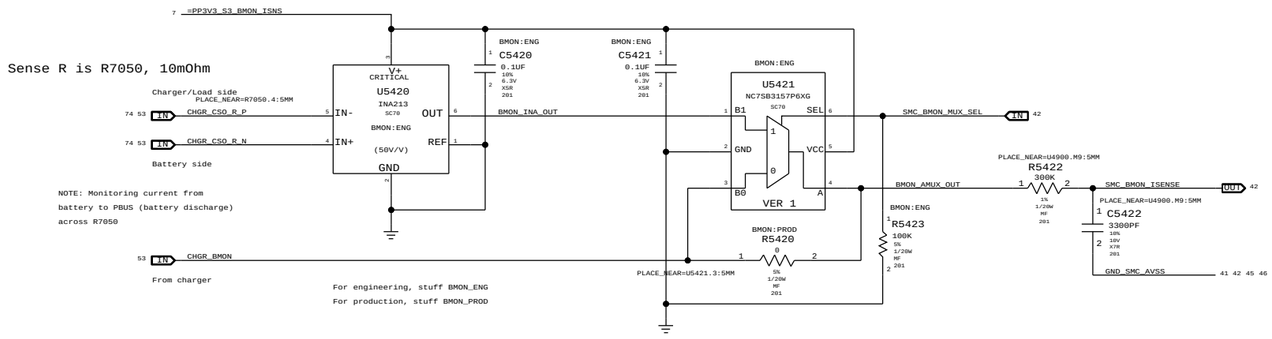


HDD Current Sense / Filter

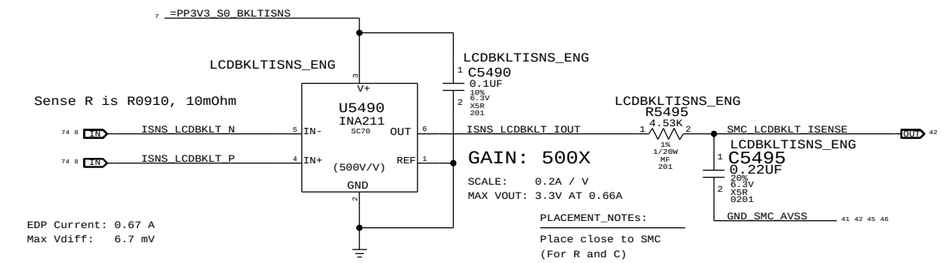


Write Address: 0x98
Read Address: 0x99

CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



LCD Backlight Driver Input Current Sense / Filter



INA (Engineering) Solution

Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

EDP Current: 10A

Charger BMON (Production) Solution

ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A

EDP Current: 310A

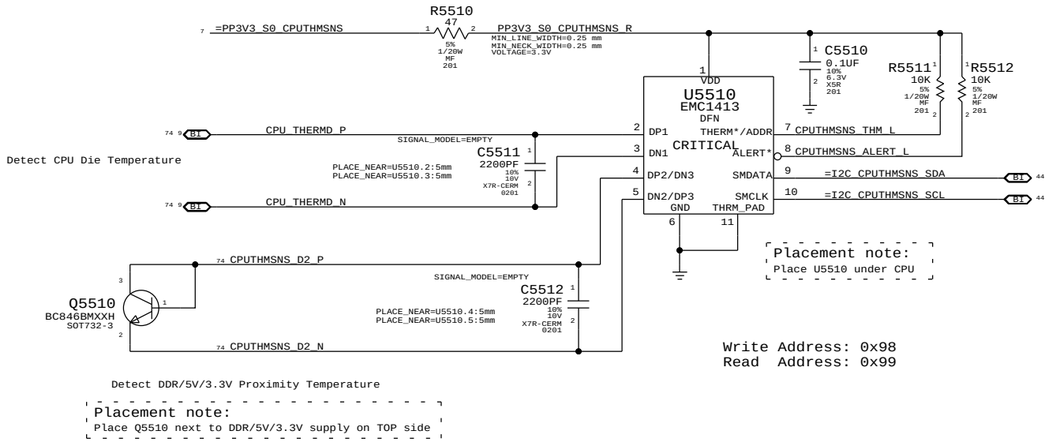
SYNC_MASTER=K78_MLB SYNC_DATE=01/16/2013

PAGE TITLE: High Side Current Sensing

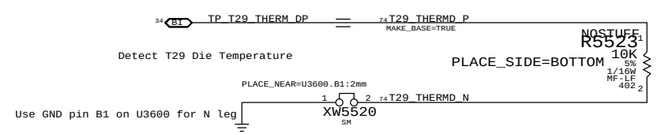
Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 54 OF 109
SHEET: 46 OF 75

CPU Proximity Sensor



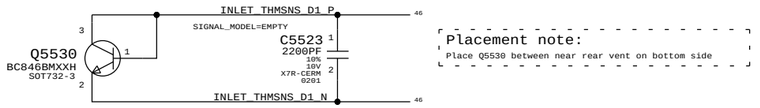
T29 Die

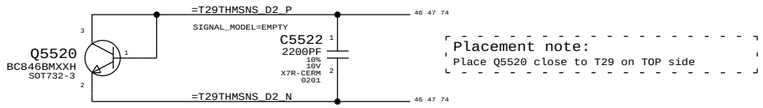


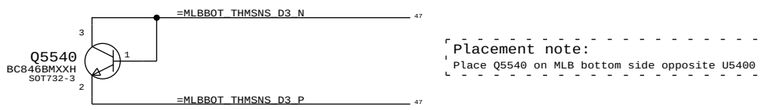
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

T29,MLB Bottom & Inlet Proximity Sensors







SYNC_MASTER=K78_MLB SYNC_DATE=01/16/2013

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

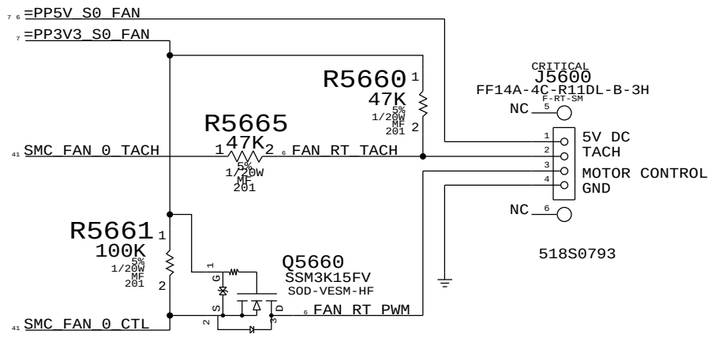
REVISION: 3.13.0

BRANCH:

PAGE: 55 OF 109

SHEET: 47 OF 75

FAN CONNECTOR



SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

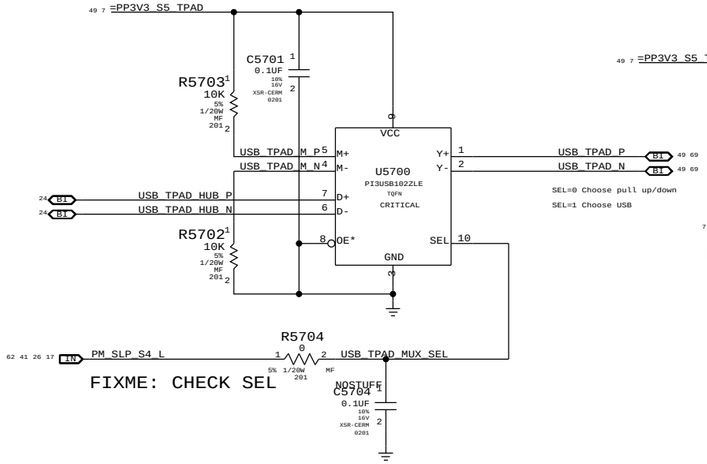
REVISION 3.13.0

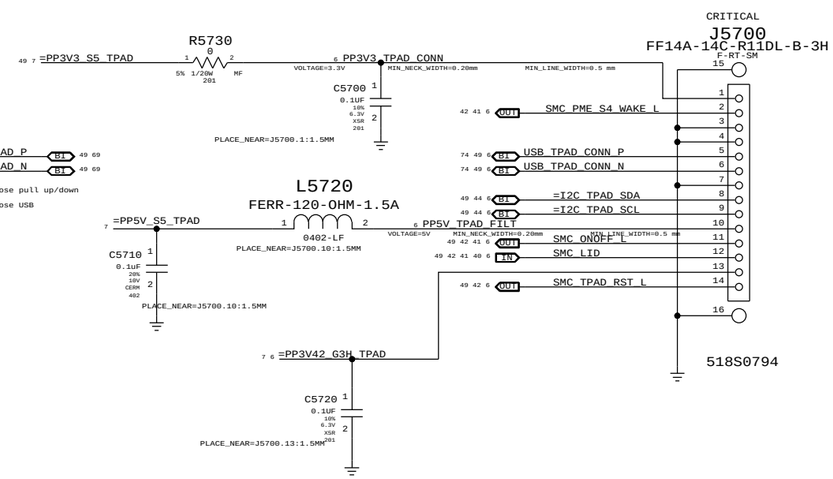
BRANCH

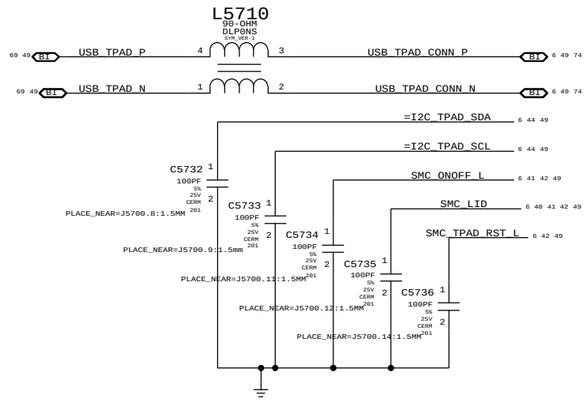
PAGE 56 OF 109

SHEET 48 OF 75

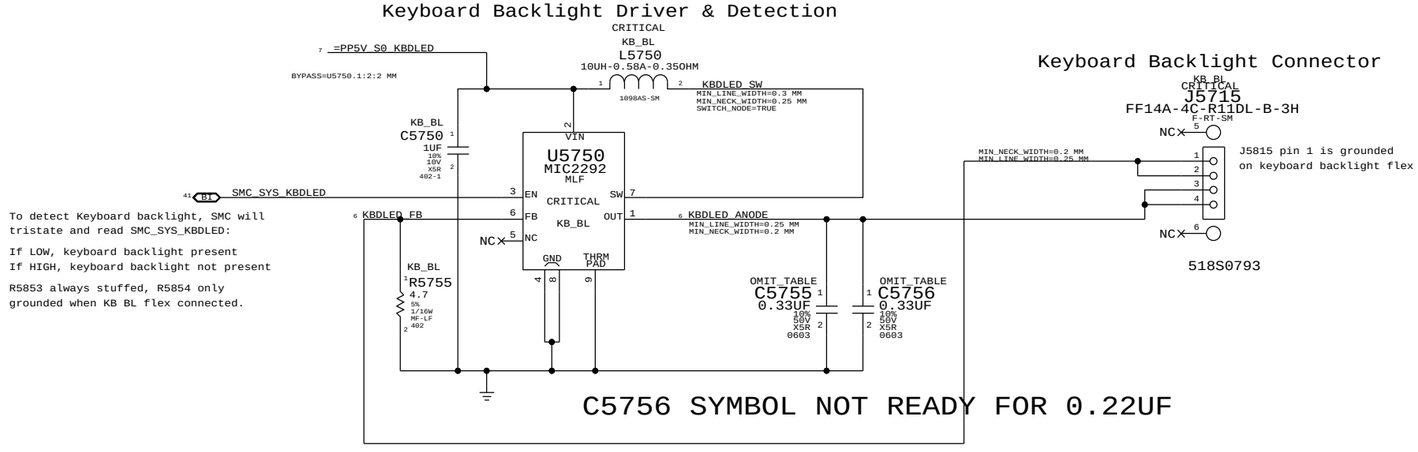
IPD Flex Connector







Keyboard Backlight Driver & Detection



Keyboard Backlight Connector

C5756 SYMBOL NOT READY FOR 0.22UF

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP,CER,0.22UF,10%,50V,X5R,0603	C5755,C5756		KB_BL

SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE: IPD / KBD Backlight

Apple Inc.

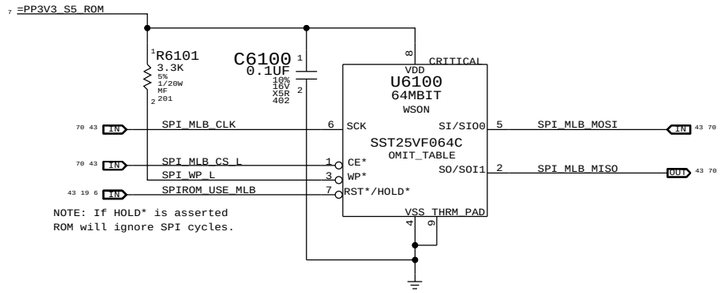
DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 57 OF 109

SHEET: 49 OF 75



SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2013

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

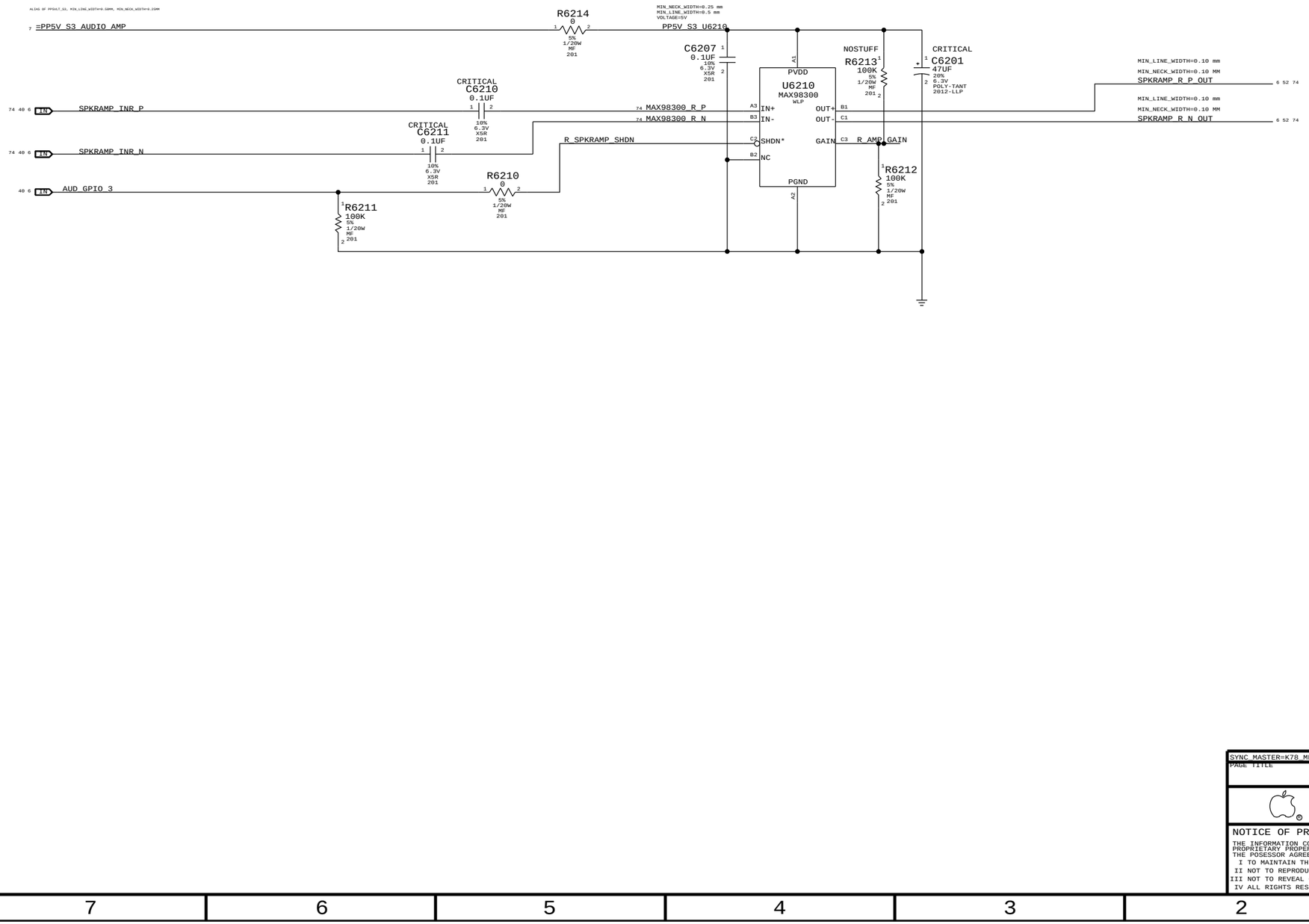
PAGE 61 OF 109

SHEET 50 OF 75

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

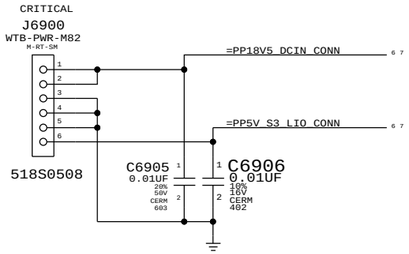
REVISION 3.13.0

BRANCH

PAGE 62 OF 109

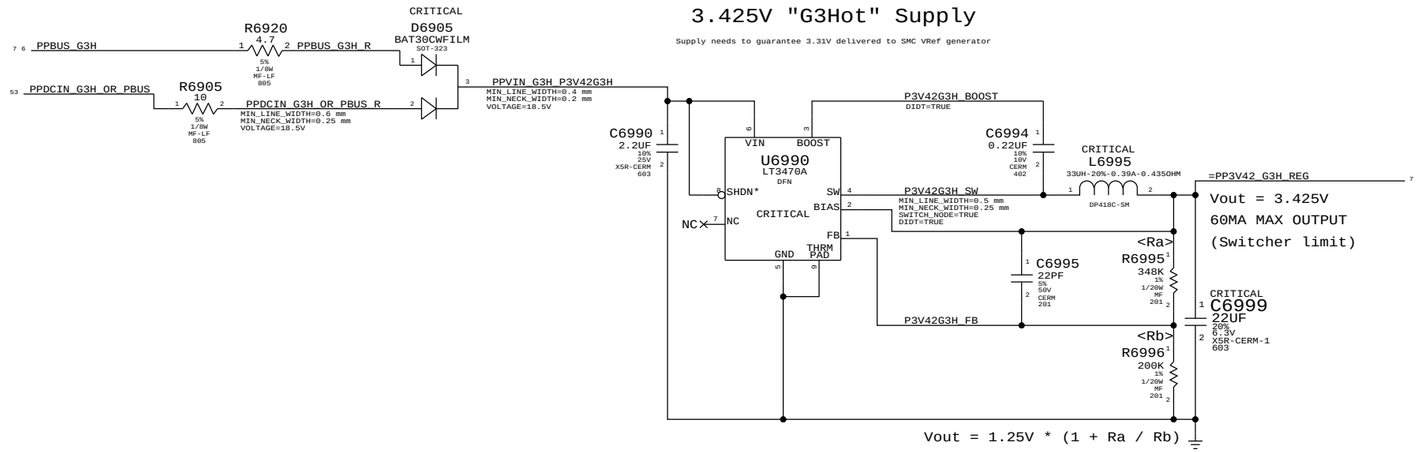
SHEET 51 OF 75

MLB to LIO Power Cable Connector



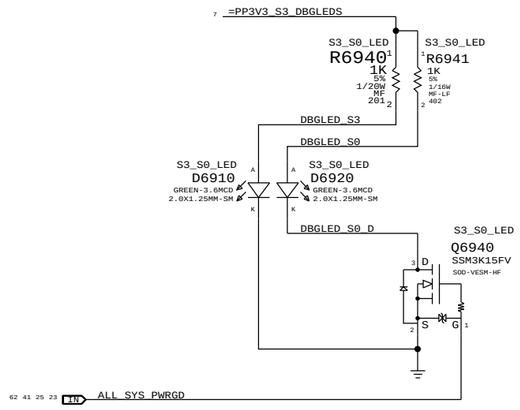
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

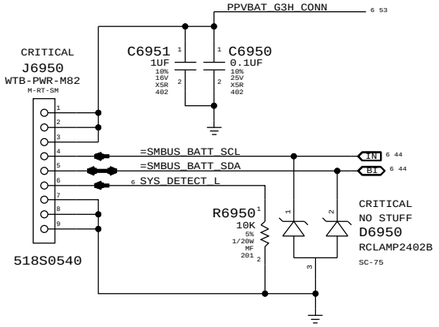


Debug LEDs

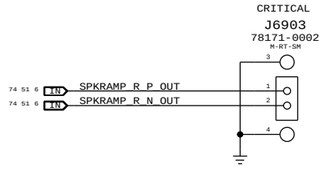
(For development only)



K16-Specific Battery Connector



Right Speaker Connector



SYNC_MASTER=JACK_K90I SYNC_DATE=08/20/2010

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

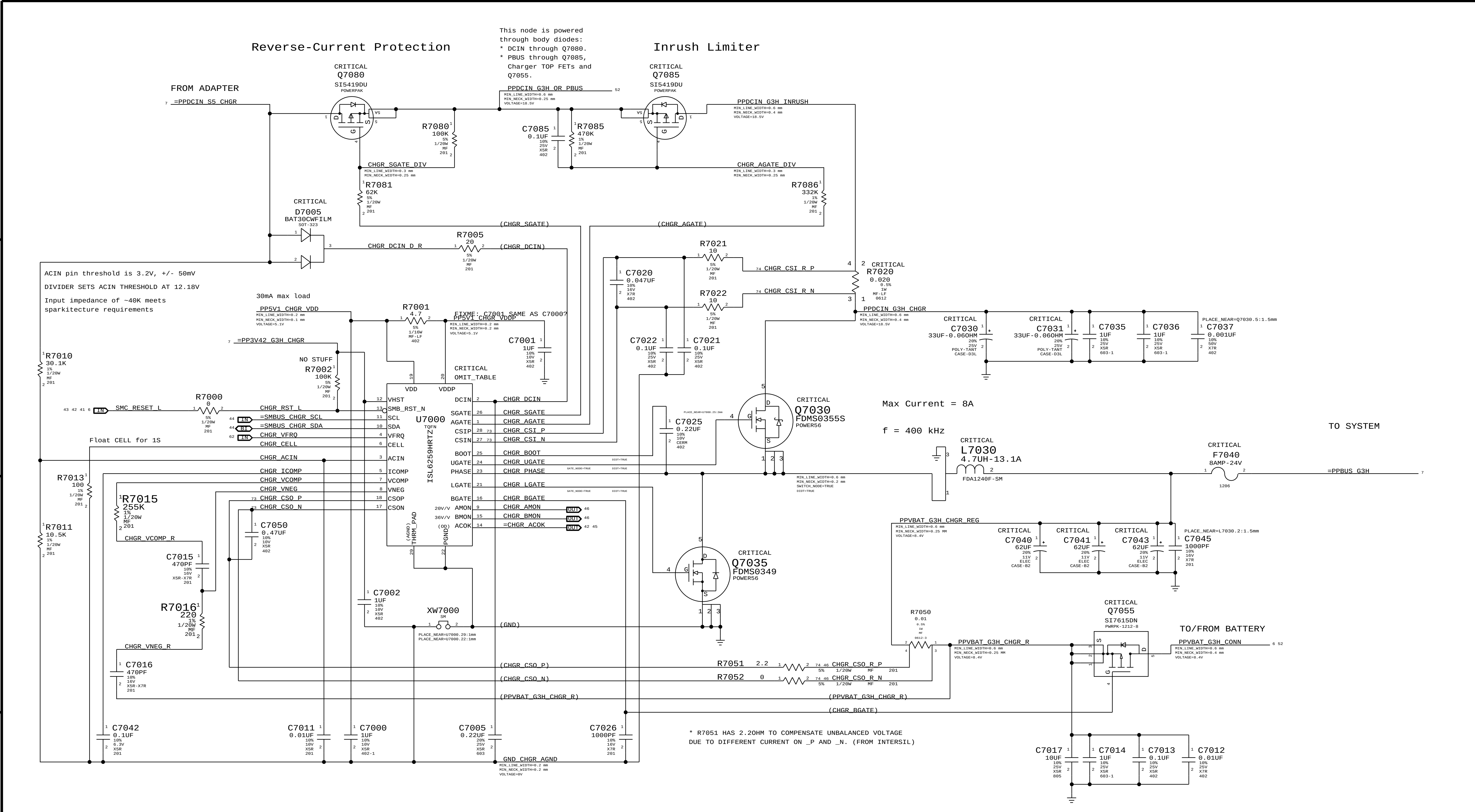
DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 69 OF 109

SHEET: 52 OF 75



Reverse-Current Protection
Inrush Limiter
This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.
FROM ADAPTER
=PPDCIN_S5_CHGR
CRITICAL
Q7080
SI5419DU
POWERPAK
Q7085
SI5419DU
PPDCIN_G3H_OR_PBUS
PPDCIN_G3H_INRUSH
CHGR_SGATE_DIV
CHGR_AGATE_DIV
R7080 100K 5% 1/20W MF 201
C7085 0.1UF 10% 25V X5R 402
R7085 470K 1% 1/20W MF 201
R7081 62K 5% 1/20W MF 201
R7086 332K 1% 1/20W MF 201
D7005
BAT30CWFILM
SOT-323
R7005 20 5% 1/20W MF 201
CHGR_DCIN_D_R
(CHGR_SGATE)
(CHGR_AGATE)
(CHGR_DCIN)
ACIN pin threshold is 3.2V, +/- 50mV
DIVIDER SETS ACIN THRESHOLD AT 12.18V
Input impedance of ~40K meets sparkitecture requirements
30mA max load
PP5V1_CHGR_VDD
R7001 4.7 5% 1/16W MF-LF 402
FIXME: C7001 SAME AS C7000?
PP5V1_CHGR_VDDP
C7001 1UF 10% 10V X5R 402
=PP3V42_G3H_CHGR
NO STUFF
R7002 100K 5% 1/20W MF 201
R7010 30.1K 1% 1/20W MF 201
R7000 0 5% 1/20W MF 201
SMC_RESET_L
CHGR_RST_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
Float CELL for 1S
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
CRITICAL
OMIT_TABLE
U7000
ISL6259HRTZ
TQFN
VDD VDDP
VHST SMB_RST_N SCL SDA VFRQ CELL ACIN ICOMP VCOMP VNEG CSOP CSON
DCIN SGATE AGATE CSIP CSIN BOOT UGATE PHASE LGATE BGATE AMON BMON ACOK
THRM_PAD PGND (AGND) 20V/V 36V/V (OD)
CHGR_DCIN CHGR_SGATE CHGR_AGATE CHGR_CSI_P CHGR_CSI_N CHGR_BOOT CHGR_UGATE CHGR_PHASE CHGR_LGATE CHGR_BGATE CHGR_AMON CHGR_BMON =CHGR_ACOK
R7013 100 1% 1/20W MF 201
R7015 255K 1% 1/20W MF 201
R7011 10.5K 1% 1/20W MF 201
CHGR_VCOMP_R
C7015 470PF 10% 16V X5R-X7R 201
R7016 220 1% 1/20W MF 201
CHGR_VNEG_R
C7016 470PF 10% 16V X5R-X7R 201
C7050 0.47UF 10% 10V X5R 402
C7002 1UF 10% 10V X5R 402
XW7000 SM
PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm
(GND)
(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)
C7042 0.1UF 10% 6.3V X5R 201
C7011 0.01UF 10% 10V X5R 201
C7000 1UF 10% 10V X5R 402-1
C7005 0.22UF 20% 25V X5R 603
C7026 1000PF 10% 16V X7R 201
GND_CHGR_AGND
R7021 10 5% 1/20W MF 201
R7022 10 5% 1/20W MF 201
C7020 0.047UF 10% 16V X7R 402
CHGR_CSI_R_P
CHGR_CSI_R_N
CRITICAL
R7020 0.020 0.5% 1W MF-LF 0612
PPDCIN_G3H_CHGR
C7022 0.1UF 10% 25V X5R 402
C7021 0.1UF 10% 25V X5R 402
C7025 0.22UF 10% 16V CERM 402
Q7030 FDMS0355S POWER56
Q7035 FDMS0349 POWER56
C7030 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L
C7031 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L
C7035 1UF 10% 25V X5R 603-1
C7036 1UF 10% 25V X5R 603-1
C7037 0.001UF 10% 50V X7R 402
PLACE_NEAR=Q7030.5:1.5mm
Max Current = 8A
f = 400 kHz
L7030 4.7UH-13.1A FDA1240F-SM
F7040 8AMP-24V 1206
TO SYSTEM
=PPBUS_G3H
PPVBAT_G3H_CHGR_REG
C7040 62UF 20% 11V ELEC CASE-B2
C7041 62UF 20% 11V ELEC CASE-B2
C7043 62UF 20% 11V ELEC CASE-B2
C7045 1000PF 10% 16V X7R 201
PLACE_NEAR=L7030.2:1.5mm
R7050 0.01 0.5% 1W MF 0612-3
PPVBAT_G3H_CHGR_R
Q7055 SI7615DN PWRPK-1212-8
TO/FROM BATTERY
PPVBAT_G3H_CONN
R7051 2.2 5% 1/20W MF 201
R7052 0 5% 1/20W MF 201
CHGR_CSO_R_P
CHGR_CSO_R_N
* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)
C7017 10UF 10% 25V X5R 805
C7014 1UF 10% 25V X5R 603-1
C7013 0.1UF 10% 25V X5R 402
C7012 0.01UF 10% 25V X7R 402

SYNC_MASTER=K78_MLB SYNC_DATE=12/03/2010

PAGE TITLE

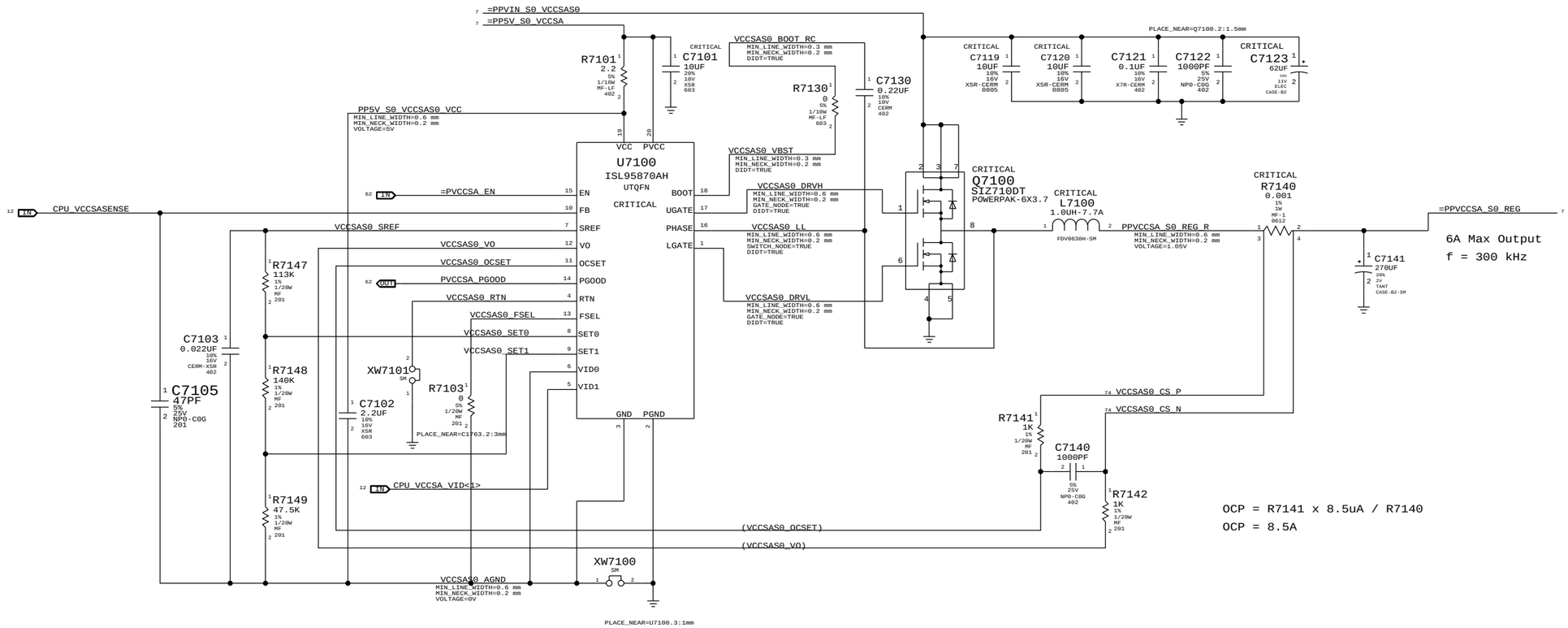
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH



VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

SYNC_MASTER=K78_MLB SYNC_DATE=01/16/2013

PAGE TITLE: System Agent Supply

Apple Inc.

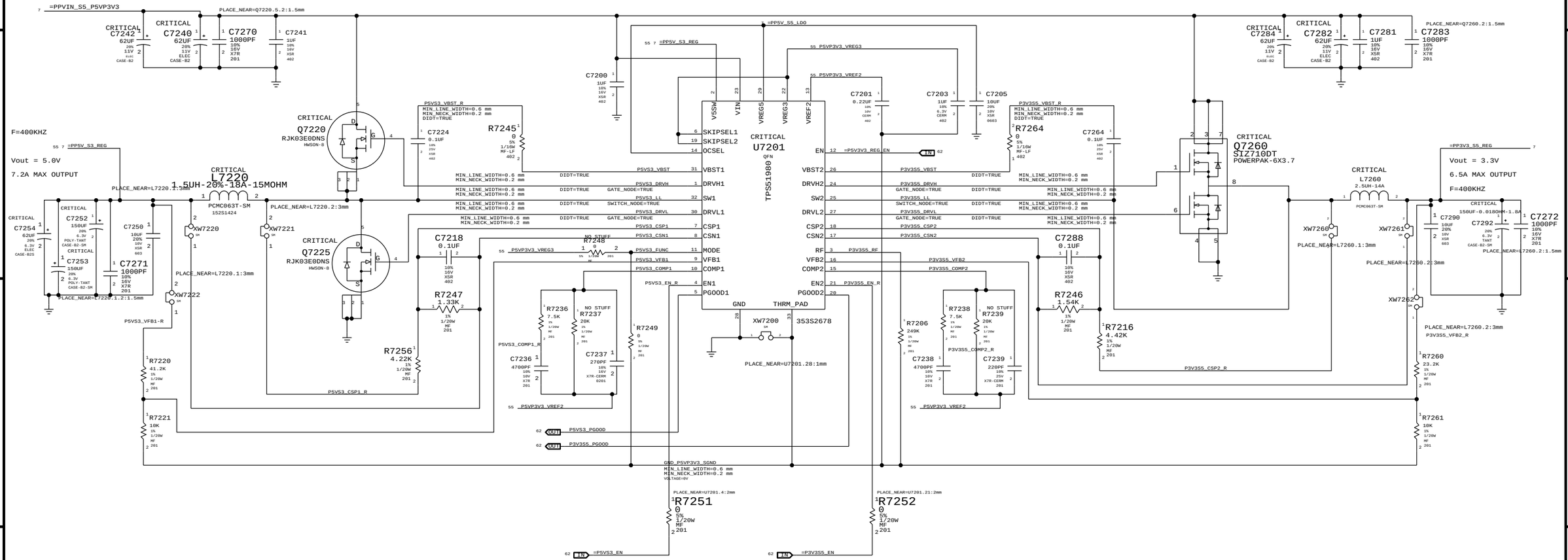
DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 71 OF 109

SHEET: 54 OF 75



SYNC_MASTER=K78_MLB SYNC_DATE=01/16/2013

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

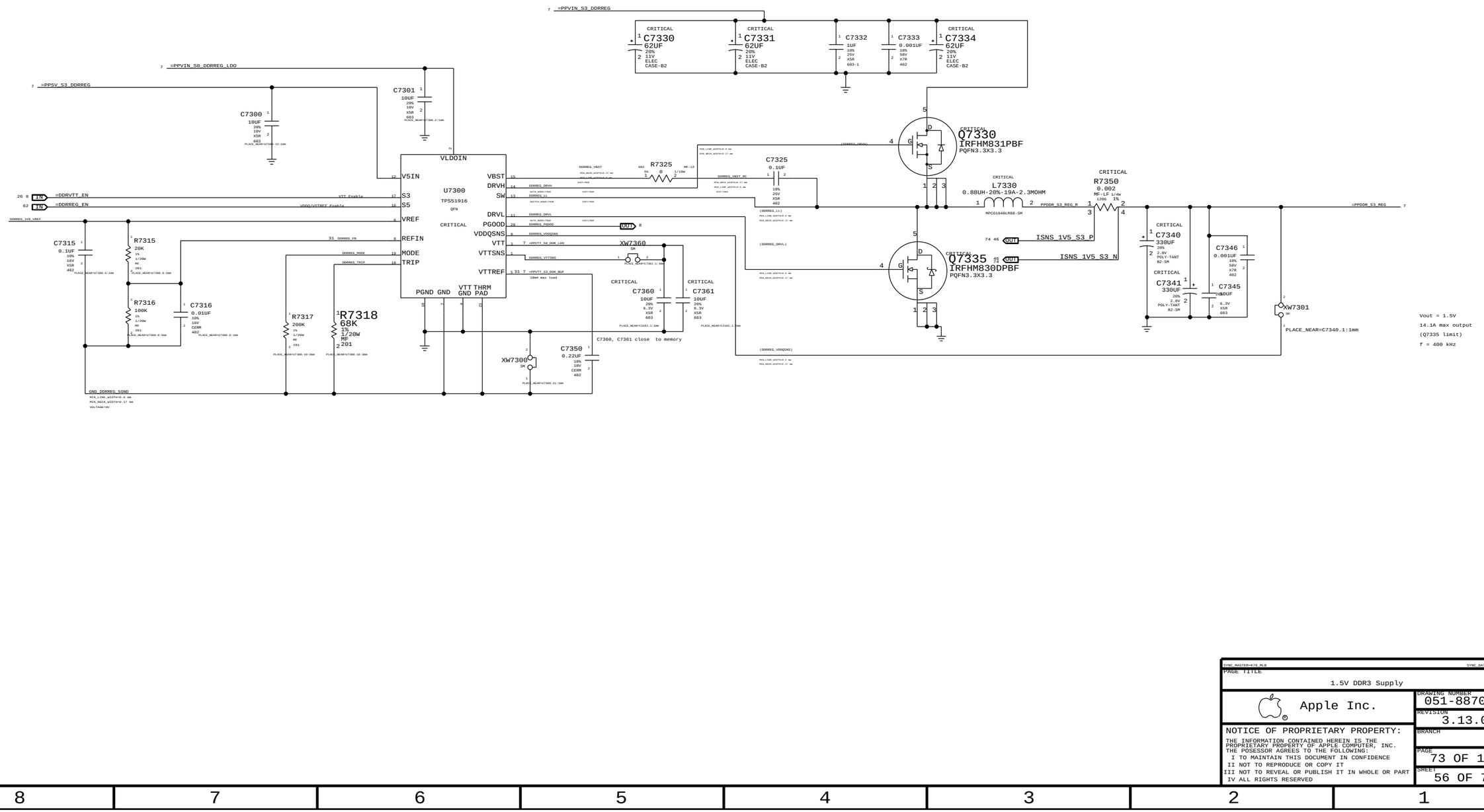
DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

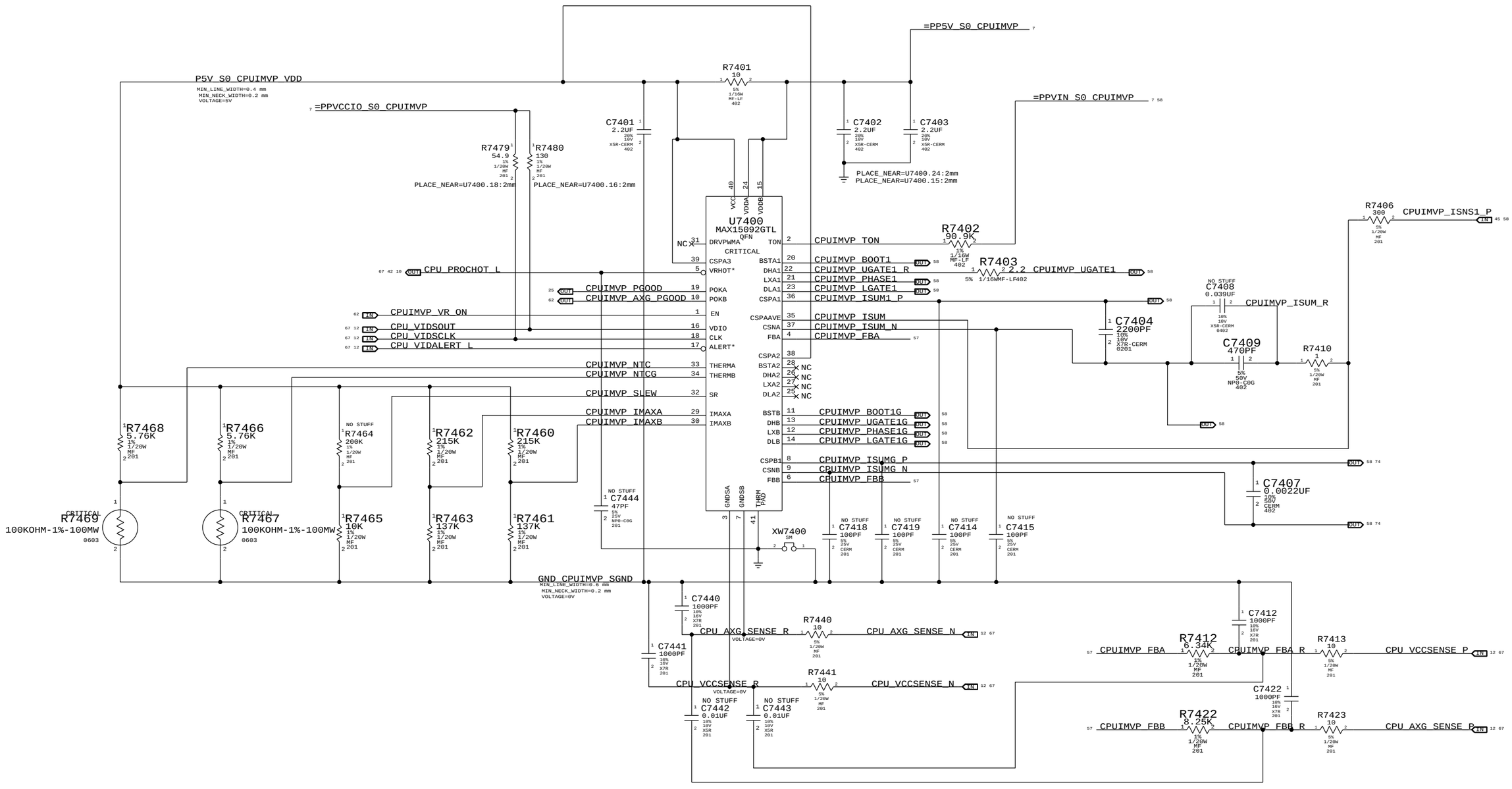
BRANCH

PAGE 72 OF 109

SHEET 55 OF 75



SYNC_MASTER=K78_MLB	SYNC_DATE=01/10/2013
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 73 OF 109
	SHEET 56 OF 75



SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

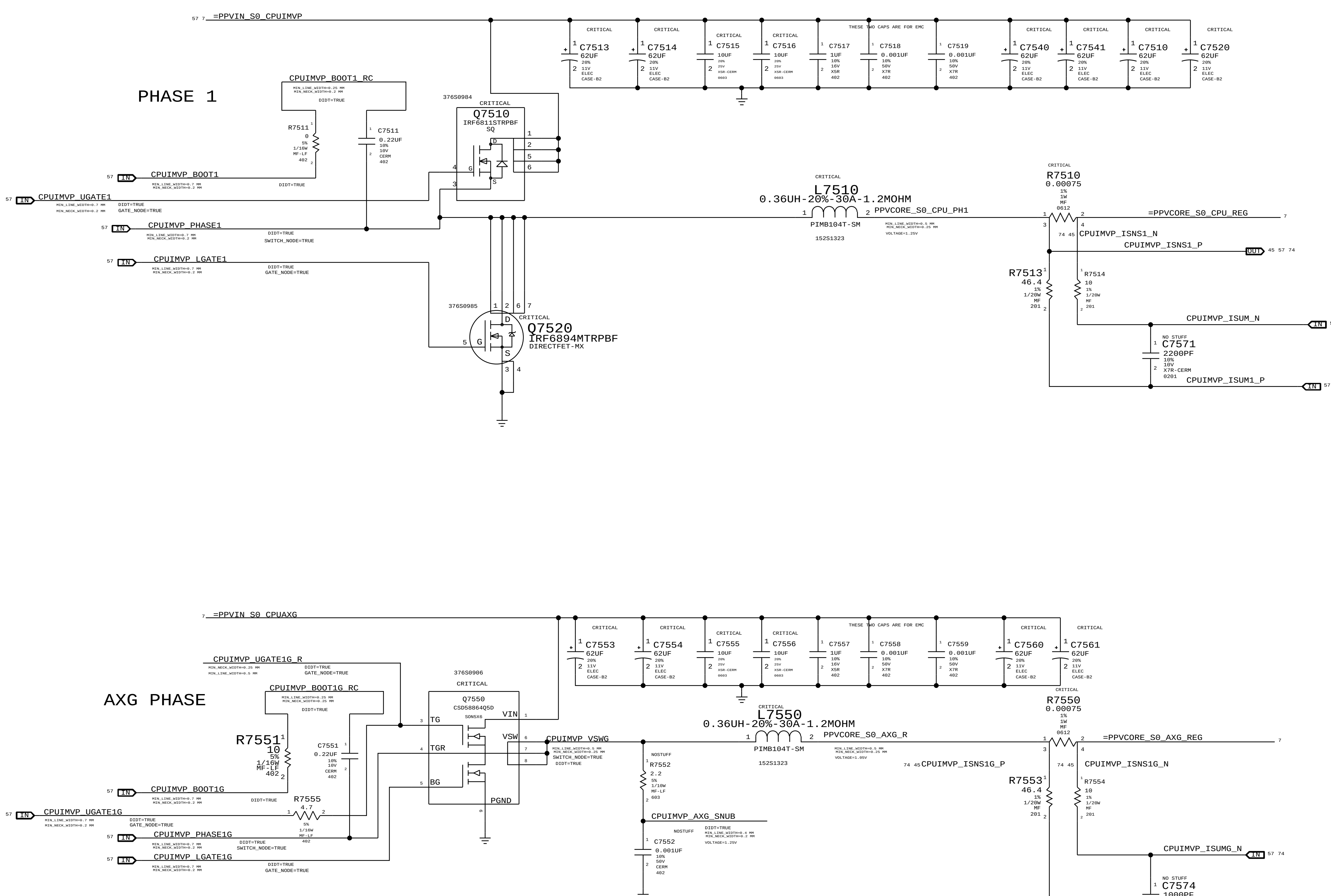
REVISION 3.13.0

BRANCH

PAGE 74 OF 109

SHEET 57 OF 75

CPU=Sandy Bridge ULV, AXG=GT2



=PPVIN_S0_CPUIMVP
PHASE 1
CPUIMVP_BOOT1_RC
R7511
C7511
0.22UF
Q7510
IRF6811STRPBF
376S0984
CRITICAL
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
Q7520
IRF6894MTRPBF
DIRECTFET-MX
376S0985
C7513
C7514
C7515
C7516
C7517
C7518
C7519
C7540
C7541
C7510
C7520
62UF
10UF
1UF
0.001UF
THESE TWO CAPS ARE FOR EMC
L7510
0.36UH-20%-30A-1.2MOHM
PIMB104T-SM
152S1323
PPVCORE_S0_CPU_PH1
R7510
0.00075
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P
OUT
R7513
46.4
R7514
10
CPUIMVP_ISUM_N
NO STUFF
C7571
2200PF
CPUIMVP_ISUM1_P
IN
=PPVIN_S0_CPUAXG
CPUIMVP_UGATE1G_R
AXG PHASE
CPUIMVP_BOOT1G_RC
R7551
10
C7551
0.22UF
Q7550
CSD58864Q5D
376S0906
TG
TGR
BG
VIN
VSW
PGND
CPUIMVP_VSWG
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
R7555
4.7
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
C7553
C7554
C7555
C7556
C7557
C7558
C7559
C7560
C7561
L7550
0.36UH-20%-30A-1.2MOHM
PIMB104T-SM
152S1323
PPVCORE_S0_AXG_R
R7552
2.2
NOSTUFF
CPUIMVP_AXG_SNUB
C7552
0.001UF
R7550
0.00075
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
R7553
46.4
R7554
10
CPUIMVP_ISUMG_N
C7574
1000PF
CPUIMVP_ISUMG_P

PAGE TITLE

CPU IMVP7 & AXG VCore Output

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

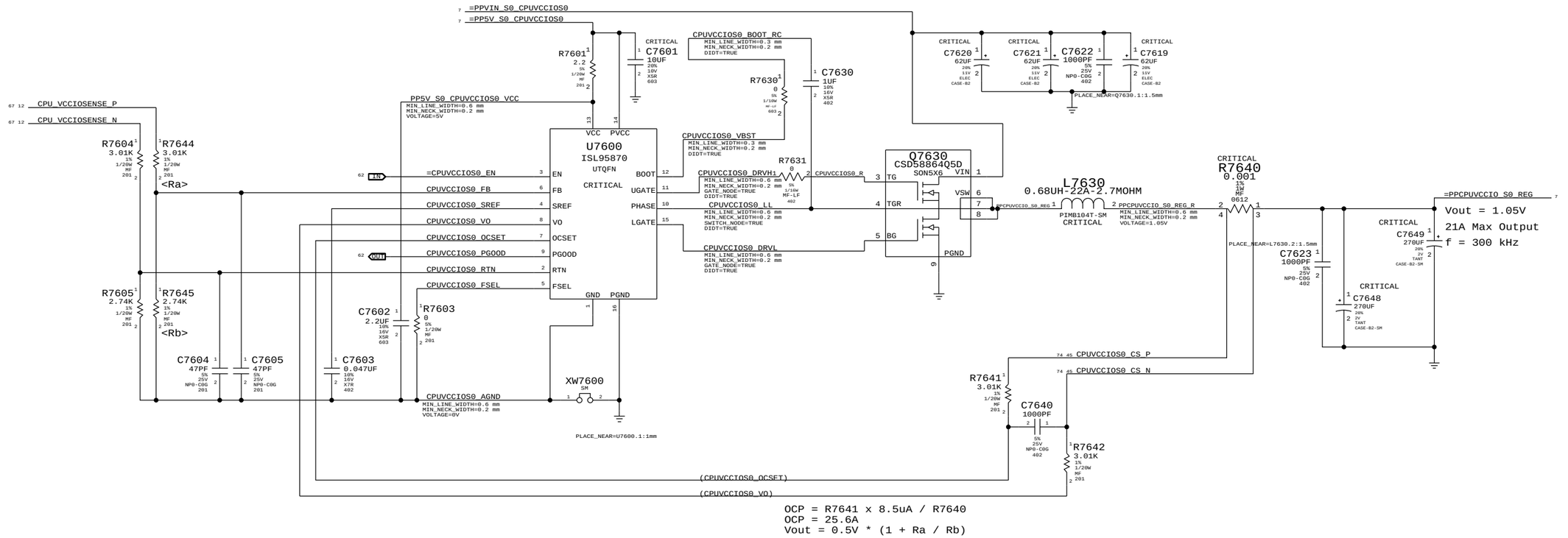
REVISION 3.13.0

BRANCH

PAGE 75 OF 109

SHEET 58 OF 75

CPU VCCIO (1.05V S0) Regulator



OCP = R7641 x 8.5uA / R7640
OCP = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

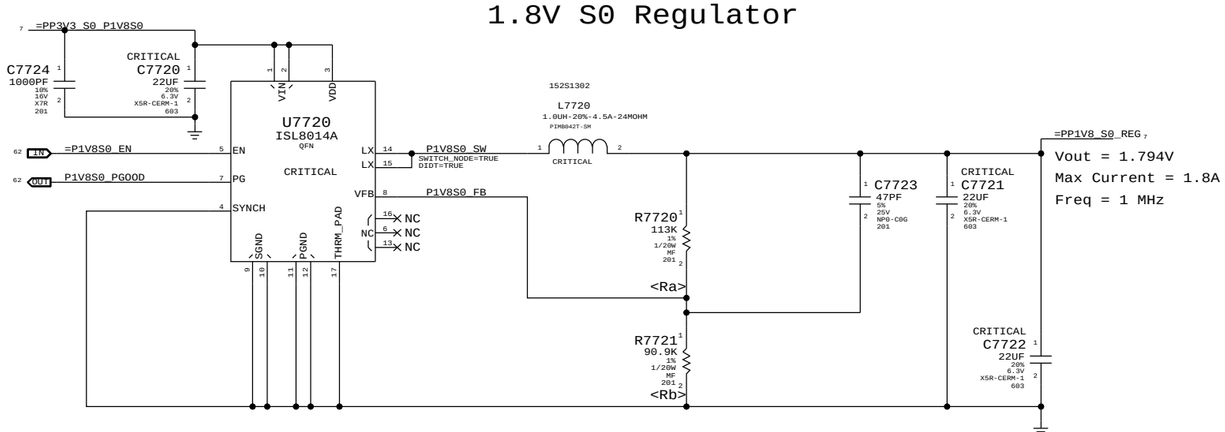
SYNC_MASTER=K78_MLB SYNC_DATE=01/10/2011

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

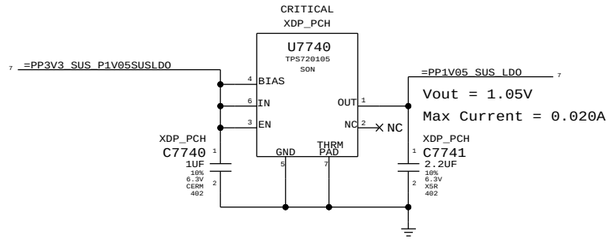
DRAWING NUMBER: 051-8870 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 76 OF 109
SHEET: 59 OF 75

1.8V S0 Regulator

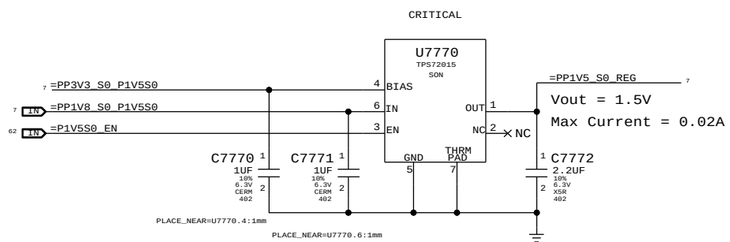


1.05V SUS LDO

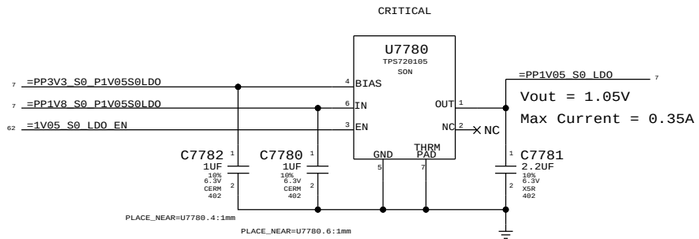
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC_MASTER=K78_MLB SYNC_DATE=01/16/2011

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

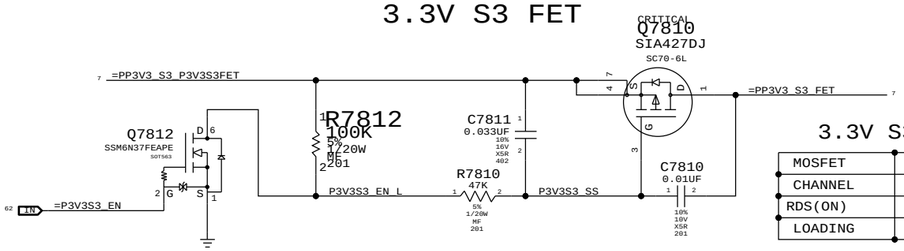
REVISION: 3.13.0

BRANCH:

PAGE: 77 OF 109

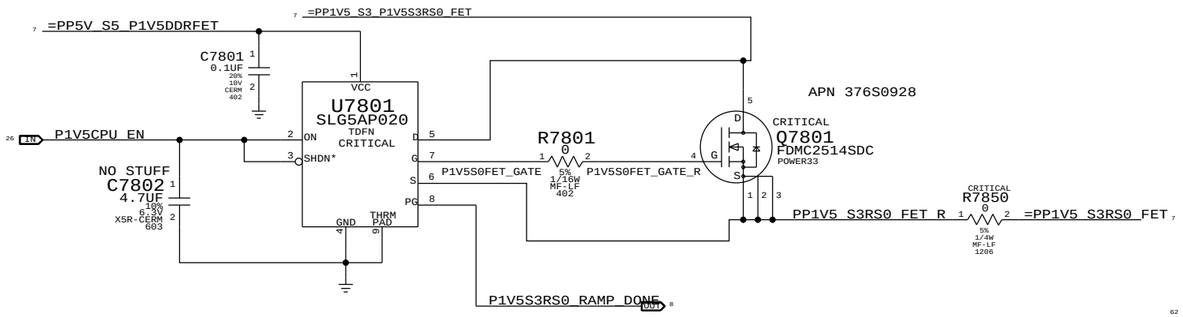
SHEET: 60 OF 75

3.3V S3 FET



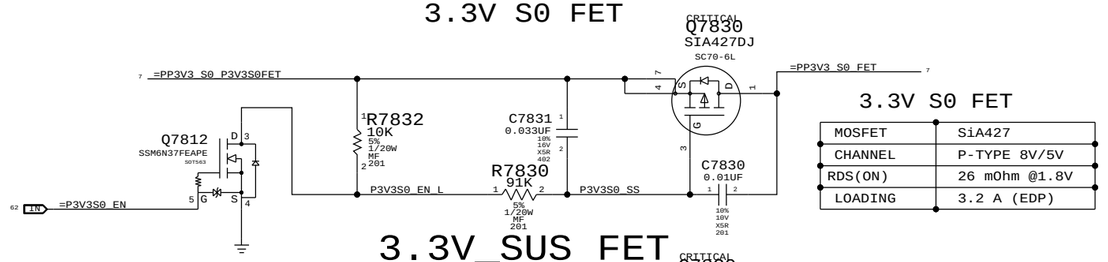
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET



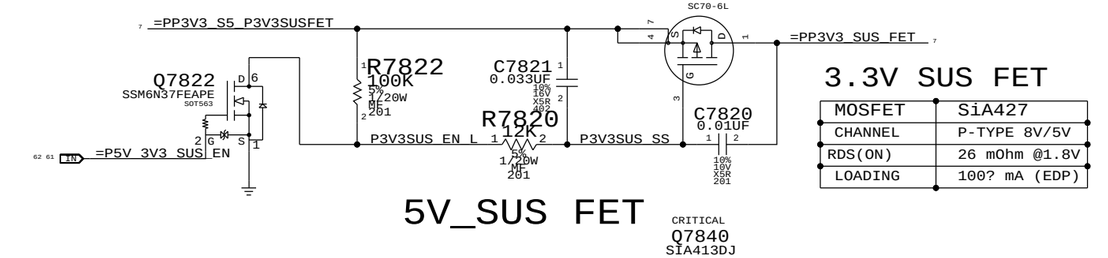
1.5V S3/S0 FET	
MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 FET



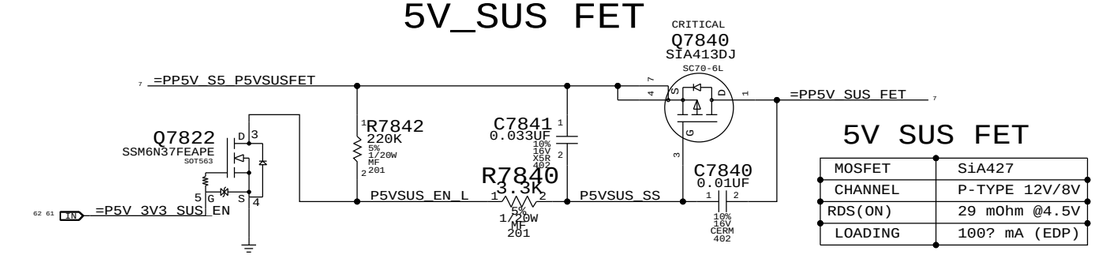
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V_SUS FET



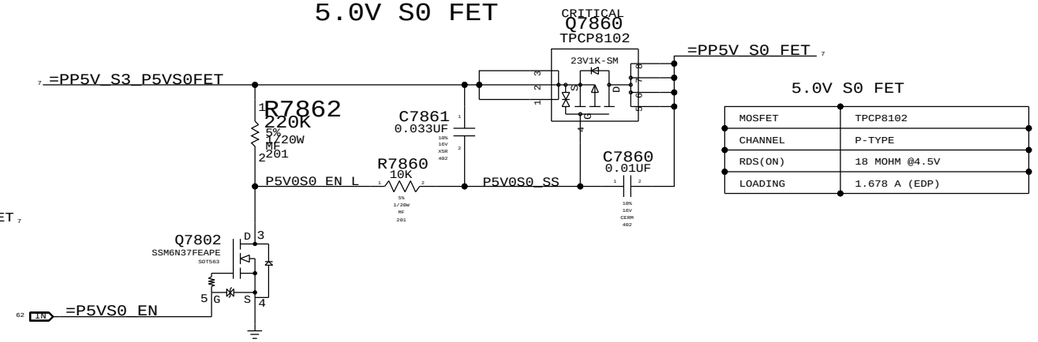
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



5V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=K78 MLB SYNC DATE=01/10/2011

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 78 OF 109

SHEET 61 OF 75

S5 Rail Enables & PGOOD

=PP3V42_G3H_PWRCTL

Internal pull-ups 100K +/- 20%

C7940 0.1UF 10% 6.3V X5R 201

U7941 SLG4AP012 TDFN — CRITICAL 343S0497

SMC_PM_G2_EN (IN) MAKE_BASE=TRUE

=PP3V3_S5_PWRCTL

Threshold: ??

DLY > 10 ms

S5PGOOD_DLY

C7941 220PF 10% 25V X7R-CERM 201

R7941 100 5% 1/20W MF 201

C7942 0.033UF 10% 16V X5R 402 — NO STUFF

P3V3S5_EN MAKE_BASE=TRUE =P3V3S5_EN (OUT) 55

P5V3V3_REG_EN MAKE_BASE=TRUE =P5V3V3_REG_EN (OUT) 55

S5_PWRGD MAKE_BASE=TRUE (OUT) 41

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V S4 ENABLE

PM_SLP_S5_L (IN) 41 17

R7915 100K 5% 1/20W MF 201

Delete R when pull-down added to PCH page

3.3V,5V S3 ENABLE

Delete R when pull-down added to PCH page

PM_SLP_S4_L (IN) MAKE_BASE=TRUE 49 41 26 17

R7910 100K 5% 1/20W MF 201

PLACE_NEAR=U7300.16:6mm

R7911 5.1K 5% 1/20W MF 201

R7912 9.1K 5% 1/20W MF 201

R7913 0 5% 1/20W MF 201

P5VS3_EN MAKE_BASE=TRUE =P5VS3_EN (OUT) 55

NO STUFF C7913 0.068UF 10% 16V CERM 402

PLACE_NEAR=Q7812.2:6mm

P3V3S3_EN MAKE_BASE=TRUE =P3V3S3_EN (OUT) 61

DDRREG_EN MAKE_BASE=TRUE =DDRREG_EN (OUT) 56

=USB_PWR_EN (OUT) 6 39 40

PLACE_NEAR=U7300.16:6mm C7910 0.47UF 10% 6.3V CERM-X5R 402

PLACE_NEAR=Q7812.2:6mm C7912 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

ALL_SYS_PWRGD 62 52 41 25 23

R7974 0 5% 1/20W MF 201

PLACE_NEAR=U7400.1:5mm

CPUIMVP_VR_ON (OUT) 57

PLACE_NEAR=U7400.1:5mm

R7976 0 5% 1/20W MF 201

NO STUFF

PLACE_NEAR=U7400.1:5mm

R7975 0 5% 1/20W MF 201

CPUVCCIOS0_PGOOD 62 59

PM_PECI_PWRGD (OUT) 41

S0 ENABLE

PM_SLP_S3_L (IN) 62 41 26 17

R7978 100 5% 1/20W MF 201

R7979 100K 5% 1/20W MF 201

Delete R when pull-down added to PCH page

PLACE_NEAR=U1800.04:5mm

(PM_SLP_S3_R_L)

PM_SLP_S3_R_L MAKE_BASE=TRUE

R7987 33K 5% 1/20W MF 201 — PLACE_NEAR=U7100.15:6mm

R7981 20K 5% 1/20W MF 201 — PLACE_NEAR=U7600.3:6mm

R7988 39K 5% 1/20W MF 201 — PLACE_NEAR=U7770.3:6mm

R7986 5.1K 5% 1/20W MF 201 — PLACE_NEAR=U7720.5:6mm

=P5VS0_EN (OUT) 61

=P3V3S0_EN (OUT) 61

=PBUSVSENS_EN (OUT) 45

P1V8S0_EN MAKE_BASE=TRUE =P1V8S0_EN (OUT) 60

P1V5S0_EN MAKE_BASE=TRUE =P1V5S0_EN (OUT) 60

=1V05_S0_LDO_EN (OUT) 60

CPUVCCIOS0_EN MAKE_BASE=TRUE =CPUVCCIOS0_EN (OUT) 59

PVCCSA_EN MAKE_BASE=TRUE =PVCCSA_EN (OUT) 54

C7987 0.47UF 10% 6.3V CERM-X5R 402

C7981 0.47UF 10% 6.3V CERM-X5R 402

C7988 0.47UF 10% 6.3V CERM-X5R 402

C7986 0.47UF 10% 6.3V CERM-X5R 402

=PP3V42_G3H_PWRCTL 7 62

R7931 10K 5% 1/20W MF 201

CHGR_VFRQ (OUT) 53

Q7931 SSM3K15FV SOD-VESM-HF

CHGR VFRQ Generation

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON 62 7

=PP3V3_S5_VMON 7

R7951 15K 1% 1/20W MF 201

R7952 7.15K 1% 1/20W MF 201

R7956 150K 1% 1/20W MF 201

R7953 1K 1% 1/20W MF 201

VMON_3V3_DIV

VMON_Q2_BASE

R7954 1K 1% 1/20W MF 201

NC

VMON_Q3_BASE

=PP1V5_S3RS0_VMON 62 7

PP1V5_S3RS0

NC

R7955 1K 1% 1/20W MF 201

=PP1V05_S0_VMON 62 7

VMON_Q4_BASE

Q7950 ASMCC0179 DFN2015H4-8 — CRITICAL

353S2809 S0PGD_BJT_GND_R

R7957 100 5% 1/20W MF 201

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL 62 7

PLACE_NEAR=U7940.5:2.3mm

C7943 0.1UF 10% 6.3V X5R 201

U7940 74AUP1G3208 SOT891

SMC_BATLOW_L:100K pull up on SMC page

SMC_BATLOW_L (IN) 42 41

ALL_SYS_PWRGD 23 25 41 52 62

PM_SUS_EN MAKE_BASE=TRUE =P5V_3V3_SUS_EN (OUT) 61

PM_SLP_SUS_L (IN) 17

PLACE_NEAR=U1800.A15:5mm

R7918 100K 5% 1/20W MF 201

Delete R when pull-down added to PCH page

NO STUFF

R7917 0 5% 1/20W MF 201

3.3V SUS Detect

=PP3V3_S5_PWRCTL 62 7

PLACE_NEAR=U7930.6:2.3mm

No stuff C7931, 12ms Min delay time, U7930 Sense input threhold is 3.07v

C7930 0.1UF 10% 6.3V X5R 201

=PP3V3_SUS_PWRCTL

R7933 100K 5% 1/20W MF 201

CRITICAL

U7930 TPS3808G33DBVRG4 SOT23-6 (90K IN)

SENSE RESET* MR* CT GND VDD

=PP3V3_SUS_PWRCTL 62 7

PM_RSMRST (OUT) 17

PM_RSMRST_L goes to U1800.C21

C7931 1000PF 10% 16V X7R 201 — NO STUFF

S0 Rail PGOOD Circuitry

(ISL Version in development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

P1V5S0_PGOOD from U7710

=PP5V_S0_VMON 7

=PP1V5_S3RS0_VMON 62 7

=PP1V05_S0_VMON 62 7

=PP3V3_S0_VMON 62 7

S0PGOOD_ISL

R7960 6.04K 1% 1/20W MF 201

R7970 10K 1% 1/20W MF 201

R7972 6.04K 1% 1/20W MF 201

C7960 0.1UF 10% 6.3V X5R 201

U7960 ISL88042IRTEZ TDFN (TPU) — CRITICAL

VDD V2MON V3MON V4MON RST* GND THRM_PAD

P5V_DIV_VMON

P1V5_DIV_VMON

P1V05_DIV_VMON

R7961 15K 1% 1/20W MF 201

R7971 10K 1% 1/20W MF 201

R7973 15K 1% 1/20W MF 201

353S2310

ALL_SYS_PWRGD_R

R7962 330 5% 1/20W MF 201

ALL_SYS_PWRGD (IN) 23 25 41 52 62

R7967 10K 5% 1/20W MF 201

R7968 100 5% 1/20W MF 201 — NO STUFF

CPUIMVP_AXG_PGOOD (IN) 57

R7966 100 5% 1/20W MF 201

P1V8S0_PGOOD (IN) 60

R7965 100 5% 1/20W MF 201

P3V3S5_PGOOD (IN) 55

R7901 100 5% 1/20W MF 201

P5VS3_PGOOD (IN) 55

R7964 100 5% 1/20W MF 201

CPUVCCIOS0_PGOOD (IN) 62 59

R7963 100 5% 1/20W MF 201

PVCCSA_PGOOD (IN) 54

DP S4 Power Enable

SMC_S4_WAKESRC_EN (IN) 42 41

MAKE_BASE=TRUE

=DPAPWRSW_EN (OUT) 65

PSOC USB Power Enable

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L (OUT) 37

Q7925 2N7002DW-X-G SOT-363

AP_PWR_EN (IN) 37 18

(AC_EN_L) 1

AC_EN_L

Q7920 2N7002DW-X-G SOT-363

R7929 0 5% 1/20W MF 201 — NO STUFF

SMC_ADAPTER_EN (IN) 42 41 17

(PM_SLP_S3_L) 4

PM_SLP_S3_L (IN) 62 41 26 17

Q7925 2N7002DW-X-G SOT-363 — NC

Unused fet

SYNC_MASTER=K78_MLB	SYNC_DATE=01/10/2011
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 79 OF 109
	SHEET 62 OF 75

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

=PP3V3_S5_LCD
LCD_IG_PWR_EN

CRITICAL
U9000
FPF1009
MFET-2X2-81N
ON
VIN_1
VIN_2
VOUT_1
VOUT_2
GND
THRM PAD

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9014 1K 5% 1/20W MF 201
C9009 0.1UF 10% 6.3V XSR 201
C9011 0.1UF 10% 6.3V XSR 201
C9012 10UF 20% 6.3V XSR 603

=I2C_TCON_SDA
=I2C_TCON_SCL
R9061 0 5% 1/20W MF 201
R9062 0 5% 1/20W MF 201
I2C_TCON_SDA_R
I2C_TCON_SCL_R

Pull-ups on panel side,
4.7 kOhm to 3.3V

DP_INT_HPD
R9060 0 5% 1/20W MF 201
DP_INT_HPD_CONN

L9004
FERR-120-OHM-1.5A
0402-LF

C9015 1000PF 10% 16V X7R 201
R9070 100K 5% 1/20W MF 201

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

DP_INT_AUX_CH_N
DP_INT_AUX_CH_P
DP_INT_ML_P<0>
DP_INT_ML_N<0>
DP_INT_ML_P<1>
DP_INT_ML_N<1>

C9024 0.1UF 10% 16V X5R-CERM 0201
C9025 0.1UF 10% 16V X5R-CERM 0201
C9020 0.1UF 10% 16V X5R-CERM 0201
C9021 0.1UF 10% 16V X5R-CERM 0201
C9022 0.1UF 10% 16V X5R-CERM 0201
C9023 0.1UF 10% 16V X5R-CERM 0201

(DP_INT_AUX_CH_C_N)
(DP_INT_AUX_CH_C_P)

DP_INT_AUX_CH_C_N
DP_INT_AUX_CH_C_P
DP_INT_ML_F_P<0>
DP_INT_ML_F_N<0>
DP_INT_ML_F_P<1>
DP_INT_ML_F_N<1>

R9050 100K 5% 1/20W MF 201
R9080 100K 5% 1/20W MF 201

PPVOUT_SW_LCDBKLT

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

R9017 1M 5% 1/20W MF 201
PLACE_NEAR=J9000.25:1mm
R9018 1M 5% 1/20W MF 201
PLACE_NEAR=J9000.24:1mm
C9017 1000PF 5% 50V C0G-CERM 603
PLACE_NEAR=J9000.3:2mm

LCD Connector

Internal DP Connector: 518S0787

CRITICAL
J9000
CABLINE-CA
F-RT-SM

NC
NC
NC

LED Backlight I/F

DisplayPort I/F

SYNC_MASTER=K78_MLB
SYNC_DATE=02/10/2011

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 90 OF 109
SHEET 63 OF 75

DP A Super-Driver

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

=T29_WAKE_L:

Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

Port A MCU

Must be 3.3V DP A port power

T29 A High-Speed Signals

T29 signals are P/N-swapped after AC caps to improve layout.

T29 Path Biasing

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

IC supports input high while Vcc = 0V.

AUXCH Snoop Port, used by PS8301 during training.

CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN
SIGNAL_MODEL=EMPTY

CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN
SIGNAL_MODEL=EMPTY
(D9382/D9383)
SIGNAL_MODEL=EMPTY
(D9360/D9361)

DP Path Biasing

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

P2R = Plug to Receptacle
R2P = Receptacle to Plug

I2C Addr:
0x26/0x27 (Wr/Rd)

DP/T29 A Low-Speed MUX

Must be 3.3V DP A port power

T29: Unused
T29: LSX_A_R2P/P2R (P/N)
T29: RX_1 Bias Sink
T29: TX_0
T29: TX_1

LO=Port A
HI=Port B

SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2010
PAGE TITLE
DisplayPort/T29 A MUXing
Apple Inc.
DRAWING NUMBER 051-8870
SIZE D
REVISION 3.13.0
BRANCH
PAGE 93 OF 109
SHEET 64 OF 75

3.3V/HV Power MUX

Port A HV Power Switch

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	1A (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

IFLT = 200k / RFLT = 885mA

ILIM = 201k / RLIM = 935mA

TFLT = CCT * 38900

TSD = CCT * 100000

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

3.3V/HV MUXed

Blocking FET, off when Source >3.4V or HV_EN high.

3.3V Always

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

Bleeder Resistor
2.5V / 249 ohm = 10mA
P = ~27mW

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

Port A 3.3V Power Switch

DP_PWR must be S4/S5 to support wake from T29 devices.

DisplayPort/T29 A Connector

Circuit threshold range: 2.877-2.941V (2.903V nominal)

T29: Unused

T29: TX_0

T29: LSX_R2P/P2R (P/N)

T29: TX_1

470k R's for ESD protection on AC-coupled signals.

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=K78_MLB	SYNC_DATE=12/07/2010
PAGE TITLE	DdisplayPort/T29 A Connector
Apple Inc.	DRAWING NUMBER 051-8870 SIZE D
	REVISION 3.13.0
	BRANCH
	PAGE 94 OF 109
	SHEET 65 OF 75

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

CRITICAL
Q9706
FDC638APZ_SBMS001
SSOT6-HF

F9700
3AMP-32V-467
603-HF
BOTTOM

=PPBUS_S0_LCDBKLT
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

PPBUS_SW_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE

R9788 301K 1% 1/20W MF 201
C9782 0.1UF 10% 16V X5R 402
LCDBKLT_EN_DIV
R9789 147K 1% 1/20W MF 201
LCDBKLT_EN_L

Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

=PP5V_S0_BKL
=PPBUS_SW_BKL
CRITICAL
C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm

CRITICAL
L9701
15UH-2.8A
PIMB053T-SM

PPBUS_SW_LCDBKLT_PWR_SW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
SWITCH_NODE=TRUE
DIDT=TRUE

PLACE_NEAR=L9701.2:3mm
CRITICAL
D9701
SOD-123
RB160M-60G
PLACE_NEAR=U9701.A5:3mm

C9796 220PF 10% 50V X7R-CERM 402
CRITICAL
C9797 10UF 10% 50V X5R 1210-1
CRITICAL
C9799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=D9701.2:5mm
PLACE_NEAR=D9701.2:3mm

PPVOUT_SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V

PLACE_NEAR=U9701.D1:5mm
C9710 1UF 10% 25V X5R 603-1
PLACE_NEAR=U9701.D1:3mm
C9714 0.01UF 10% 10V X5R 201

=PP3V3_S0_BKL_VDDIO
PLACE_NEAR=U9701.C4:4mm
C9711 0.1UF 10% 6.3V X5R 201

XW9720
SM
PLACE_NEAR=C9797.1:5mm

PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
MIN_LINE_WIDTH=0.1 MM
MIN_NECK_WIDTH=0.1 MM

U9701
25-BUMP-MICRO
LP8550

	VDDIO	VLDO	VIN
	C4	D1	C1
BKL_VSYNC_R	D2	VSYNC	
BKL_FLTR	C2	FILTER	
BKL_ISET	B3	ISET	
BKL_FSET	B4	FSET	
BKL_SCL	D3	SCLK	
BKL_SDA	D4	SDA	
BKL_PWM	A4	PWM	
BKL_EN	A3	EN	
TP_BKL_FAULT	C3	FAULT	
		SW_0	B1
		SW_1	B2
		FB	A5
BKL_ISEN1	E5	OUT1	
BKL_ISEN2	D5	OUT2	
BKL_ISEN3	C5	OUT3	
BKL_ISEN4	E3	OUT4	
BKL_ISEN5	E2	OUT5	
BKL_ISEN6	E1	OUT6	
	B5	GND_S	
	E4	GND_L	
	A1	GND_SW	
	A2	GND_SW	

R9741 10K 5% 1/20W MF 201
R9753 0 5% 1/20W MF 201
=I2C_BKL_1_SCL
R9757 0 5% 1/20W MF 201
=I2C_BKL_1_SDA
Addr: 0x58(Wr)/0x59(Rd)
PPBUS_SW_LCDBKLT_PWR
R9731 200K 1% 1/20W MF 201
R9715 100K 1% 1/20W MF 201
PLACE_SIDE=BOTTOM
R9704 33 5% 1/20W MF 201
LCD_BKLT_PWM
C9704 33PF 5% 25V NP0-C0G 201

Fpwm=9.62kHz
see spec for others
R9755 10K 1% 1/20W MF 201
R9716 90.9K 1% 1/20W MF 201
I_LED=20.3mA
R9714 18.2K 1% 1/20W MF 201
GND_BKL_SGND
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

XW9710
SM
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD
R9717 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E5:10mm
LED_RETURN_1
BKLT:PROD
R9718 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.D5:10mm
LED_RETURN_2
BKLT:PROD
R9719 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.C5:10mm
LED_RETURN_3
BKLT:PROD
R9720 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E3:10mm
LED_RETURN_4
BKLT:PROD
R9721 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E2:10mm
LED_RETURN_5
BKLT:PROD
R9722 0 5% 1/16W MF-LF 402
PLACE_NEAR=U9701.E1:10mm
LED_RETURN_6

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
BOTTOM
OUT 6 63

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K78_MLB SYNC_DATE=01/16/2011
PAGE TITLE
LCD Backlight Driver
Apple Inc.
DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 97 OF 109
SHEET 66 OF 75

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_XDP_BPM	TOP,BOTTOM	100 MIL	100 MIL	100 MIL	100 MIL	=STANDARD	=STANDARD
CPU_XDP_BPM	*	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S

NOTE: CPU_XDP_BPM physical constraint is to prevent routing on outer layers.
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 41
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 42 57
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	10 16
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_XDP_BPM	CPU_ITP	XDP_BPM_L<7..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 57
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 59
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 57
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 57
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 57
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 57
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 57
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE
CPU Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D
REVISION 3.13.0
BRANCH
PAGE 100 OF 109
SHEET 67 OF 75

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP_BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP_BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9,ISL10	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	?
MEM_CTRL2CTRL	*	0.2 MM	?
MEM_CMD2CTRL	*	0.2 MM	?
MEM_CMD2CMD	*	0.2 MM	?
MEM_DATA2DATA	*	0.14 MM	?
MEM_DQS2DQS	*	0.4 MM	?
MEM_MEM2OTHERMEM	*	0.4 MM	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	0.6 MM	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_2PWR
MEM_CTRL	MEM_PWR	*	MEM_2PWR
MEM_CMD	MEM_PWR	*	MEM_2PWR
MEM_DATA	MEM_PWR	*	MEM_2PWR
MEM_DQS	MEM_PWR	*	MEM_2PWR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_2GND
MEM_CTRL	GND	*	MEM_2GND
MEM_CMD	GND	*	MEM_2GND
MEM_DATA	GND	*	MEM_2GND
MEM_DQS	GND	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CMD2CTRL
MEM_CTRL	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQ to DQS matching per byte lane should be within 0.127mm.

DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.

CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.

SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_CKE<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_CS_L<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_A_ODT<3..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<15..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_CKE<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_CS_L<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_B_ODT<3..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<15..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	7
		MEM_PWR	PP1V5_S3	7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 29 30 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	9 27 28 29 30 31

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2012

PAGE TITLE

Memory Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 101 OF 109

SHEET 68 OF 75

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	
	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<3>	8
	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<3>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_P	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_N	8
	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 38
	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 38
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P	6 38
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_N	6 38
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 38
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	16 38
	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 38
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 38
	SATA_90D	SATA	SATA_ODD_R2D_C_P	8 16
	SATA_90D	SATA	SATA_ODD_R2D_C_N	8 16
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	8 16
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_N	8 16
	SATA_90D	SATA	SATA_HDD_R2D_RC_P	
	SATA_90D	SATA	SATA_HDD_R2D_RC_N	
	SATA_90D	SATA	SATA_HDD_D2R_RC_P	
	SATA_90D	SATA	SATA_HDD_D2R_RC_N	
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 39
USB_EXTA	USB_85D	USB	USB_EXTA_N	24 39
USB_EXTB	USB_85D	USB	USB_EXTB_P	
	USB_85D	USB	USB_EXTB_N	
USB_EXTC	USB_85D	USB	USB_EXTC_P	
	USB_85D	USB	USB_EXTC_N	
USB_EXTD	USB_85D	USB	USB_EXTD_P	6 24 40
	USB_85D	USB	USB_EXTD_N	6 24 40
USB_EXTD	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24
	USB_85D	USB	T29_A_RSVD_P	8 64
	USB_85D	USB	T29_A_RSVD_N	8 64
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	6 18 40
	USB_85D	USB	USB_CAMERA_N	6 18 40
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	
	USB_85D	USB	USB_CAMERA_CONN_N	
USB_BT	USB_85D	USB	USB_BT_P	6 24 37
USB_BT	USB_85D	USB	USB_BT_N	6 24 37
USB_TPAD	USB_85D	USB	USB_TPAD_P	49
	USB_85D	USB	USB_TPAD_N	49
USB_IR	USB_85D	USB	USB_IR_P	
	USB_85D	USB	USB_IR_N	
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	24 33
	USB_85D	USB	USB_SDCARD_N	24 33
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	8
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	8
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

PCH Constraints 1

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 102 OF 109

SHEET 69 OF 75

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 41 43
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 41 43
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 41
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 43
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 44
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 44
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 44
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 44
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 44
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 44
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	6 16 40
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	6 16 40
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	6 16 40
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	6 16 40
	HDA_50S	HDA	AUD_SDI_R	
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	6 16 40
	HDA_50S	HDA	HDA_SDOUT_R	16
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 43
	SPI_55S	SPI	SPI_CLK	43
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 43
	SPI_55S	SPI	SPI_MOSI	43
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 43
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 43
	SPI_55S	SPI	SPI_CS0_L	43
	SPI_55S	SPI	SPI_MLB_CLK	43 50
	SPI_55S	SPI	SPI_MLB_MOSI	43 50
	SPI_55S	SPI	SPI_MLB_MISO	43 50
	SPI_55S	SPI	SPI_MLB_CS_L	43 50
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 37
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 37
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 37
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 37
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 37
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 37
	PCIE_85D	PCIE	PCIE_FW_R2D_P	
	PCIE_85D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	
	PCIE_85D	PCIE	PCIE_FW_D2R_N	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 37
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	8 16
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 70
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 70
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	8 64
DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 64
	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	64
	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	64
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 64
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 64
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	64
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	64
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	63
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	63
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	9 63
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	9 63
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	6 63
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	6 63
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_C_P	6 63
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_C_N	6 63
	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_P	9 63
	DP_85D	DISPLAYPORT	DP_INT_AUX_CH_N	9 63
	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 34
	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 34
PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE	PCIE_T29_D2R_P<3>	8 34
PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE	PCIE_T29_D2R_P<2>	8
PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE	PCIE_T29_D2R_P<1>	8 34
PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE	PCIE_T29_D2R_P<0>	8
PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE	PCIE_T29_D2R_N<3>	8 34
PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE	PCIE_T29_D2R_N<2>	8 34
PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE	PCIE_T29_D2R_N<1>	8 34
PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE	PCIE_T29_D2R_N<0>	8 34
PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE	PCIE_T29_R2D_P<3>	34
PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE	PCIE_T29_R2D_P<2>	34
PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE	PCIE_T29_R2D_P<1>	34
PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE	PCIE_T29_R2D_P<0>	34
PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE	PCIE_T29_R2D_N<3>	34
PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE	PCIE_T29_R2D_N<2>	34
PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE	PCIE_T29_R2D_N<1>	34
PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE	PCIE_T29_R2D_N<0>	34
	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	34
	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	34
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 34
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 25
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	25 34
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	34

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 103 OF 109

SHEET: 70 OF 75

CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N
Port 2 Not Used			

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: Ethernet/FW Constraints

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 104 OF 109

SHEET: 71 OF 75

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

DP/T29 Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 Net Properties

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	8 34
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	8 34
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	34
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	34
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	8 34
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	8 34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	34
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	34 44
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	34 44
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	34
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	34
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	34
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	34
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	8 34 64
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	8 34 64
	T29DP_80D	T29DP	T29_D2R_P<3..0>	8 34 64
	T29DP_80D	T29DP	T29_D2R_N<3..0>	8 34 64
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	64
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	64
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	64
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	64
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	64
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	64
T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_P<0>	64 65
T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_N<0>	64 65
T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_P<1>	64 65
T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_N<1>	64 65
	T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_P	65
	T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_N	65
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	64
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	64
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	64
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	64
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<0>	64
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<0>	64
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<1>	64
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<1>	64
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2>	64
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2>	64
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3>	64
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3>	64
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	64
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	64
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	64
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	64
T29DPA_ML_ODD			T29DPA_ML_P<1>	64 65
T29DPA_ML_ODD			T29DPA_ML_N<1>	64
T29DPA_ML_ODD			T29DPA_ML_P<3>	64 65
T29DPA_ML_ODD			T29DPA_ML_N<3>	64
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	64 65
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	64 65
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	64 65
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	64 65
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	64 65
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	64 65

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: T29 Constraints

Apple Inc.

DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 105 OF 109

SHEET: 72 OF 75

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	44
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	44
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 44
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 44
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	53
	1TO1_DIFFPAIR		CHGR_CSI_N	53
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	53
	1TO1_DIFFPAIR		CHGR_CSO_N	53

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

BRANCH

PAGE 106 OF 109

SHEET 73 OF 75

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
MEM_72D	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
MEM_37S	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
MEM_85D	*	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
PCIE_85D	*	OVERRIDE	OVERRIDE	0.076 MM	10 mm	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
USB_85D	TOP	OVERRIDE	OVERRIDE	0.1 MM	500 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
CPU_27P4S	TOP	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		
CLK_PCIE_90D	TOP	OVERRIDE	OVERRIDE	0.09 MM	400 MIL	OVERRIDE	OVERRIDE
	OVERRIDE			OVERRIDE	OVERRIDE		

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_100D	ENETCONN	ENETCONN P<3..0>
	ENET_100D	ENETCONN	ENETCONN N<3..0>
	SATA_90D	SATA	SATA_ODD_D2R_UF_P
	SATA_90D	SATA	SATA_ODD_D2R_UF_N
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N
P295	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P
P296	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N
P297	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P
P298	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P 47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N 47
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P 9 47
	THERM_1TO1_55S	THERM	CPU_THERMD_N 9 47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P 47
	THERM_1TO1_55S	THERM	T29_THERMD_N 47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_P 46 47
	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_N 46 47
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N 46
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N 45 59
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P 45 59
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P 45 57 58
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N 45 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P 45 58
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N 45 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P 45
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P 45
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P 54
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N 54
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P 57 58
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N 57 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N
	SENSE_1TO1_55S	SENSE	ISNS_CPU_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N 38 46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P 38 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N 8 46
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P 8 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N 46 56
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P 46 56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N 37 46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P 37 46
	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_N
	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_P

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P 6 40 51 74
	DIFFPAIR	AUDIO	SPKRAMP_INR_N 6 40 51 74
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P 51
	DIFFPAIR	AUDIO	MAX98300_R_N 51

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N
	1TO1_DIFFPAIR		CHGR_CSI_R_P 53
	1TO1_DIFFPAIR		CHGR_CSI_R_N 53
	1TO1_DIFFPAIR		CHGR_CSO_R_P 46 53
	1TO1_DIFFPAIR		CHGR_CSO_R_N 46 53
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P 39
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N 39
(USB_EXTA)	USB_85D	USB	USB2_LT1_P 39
(USB_EXTA)	USB_85D	USB	USB2_LT1_N 39
	USB_85D	USB	CONN_USB2_BT_P
	USB_85D	USB	CONN_USB2_BT_N
	USB_85D	USB	USB_LT2_P
	USB_85D	USB	USB_LT2_N
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT 6 51 52
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT 6 51 52
P299	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SSM2315_SUB_N
P300	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SSM2315_SUB_P
P301	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SSM2315_L_N
P302	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SSM2315_L_P
P303	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SSM2315_R_N
P304	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SSM2315_R_P
P305	AUD_DIFF	1TO1_DIFFPAIR	AUDIO AUD_LO2_N_R
P306	AUD_DIFF	1TO1_DIFFPAIR	AUDIO AUD_LO2_P_R
P307	AUD_DIFF	1TO1_DIFFPAIR	AUDIO AUD_LO1_N_R
P308	AUD_DIFF	1TO1_DIFFPAIR	AUDIO AUD_LO1_P_R
P309	AUD_DIFF	1TO1_DIFFPAIR	AUDIO AUD_LO2_N_L
P310	AUD_DIFF	1TO1_DIFFPAIR	AUDIO AUD_LO2_P_L
P311	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SPKRAMP_INL_P
P312	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SPKRAMP_INL_N
P313	SPKRAMP_INR	DIFFPAIR	AUDIO SPKRAMP_INR_P 6 40 51 74
P314	AUD_DIFF	DIFFPAIR	AUDIO SPKRAMP_INR_N 6 40 51 74
P315	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SPKRAMP_INSUB_P
P316	AUD_DIFF	1TO1_DIFFPAIR	AUDIO SPKRAMP_INSUB_N
	USB_85D	USB	USB_TPAD_R_P
	USB_85D	USB	USB_TPAD_R_N
	SB_POWER		PP3V3_S5 6 7
	SB_POWER		PP3V3_S0 6 7
	GND		GND

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_P
(USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_N
(USB_EXTA)	USB_85D	USB	USB_LT1_P
(USB_EXTA)	USB_85D	USB	USB_LT1_N
(USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_P 6 49
(USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_N 6 49
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R
	SMB_55S	SMB	I2C_TCON_SCL
	SMB_55S	SMB	I2C_TCON_SDA
	SMB_55S	SMB	I2C_TCON_SCL_CONN
	SMB_55S	SMB	I2C_TCON_SDA_CONN

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2017

PAGE TITLE

Project Specific Constraints

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DRAWING NUMBER 051-8870 SIZE D

REVISION 3.13.0

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PAGE 108 OF 109

SHEET 74 OF 75

K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.155MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4,ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC_MASTER=K21_CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: PCB Rule Definitions

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DRAWING NUMBER: 051-8870 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 109 OF 109

SHEET: 75 OF 75