1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2009-05-19

SCHEM,BLACK_PEARL,MLB,K92

pre-evt 11/22/10 rev3.11.3

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8618	1	SCHEM,BLACK_PEARL,MLB,K92	SCH	CRITICAL	
820-2914	1	PCBF,BLACK_PEARL,MLB,K92	PCB	CRITICAL	

DRAWING

TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Nov 23 20:44:38 2010

DRAWING TITLE: SCHEM,MLB,K92

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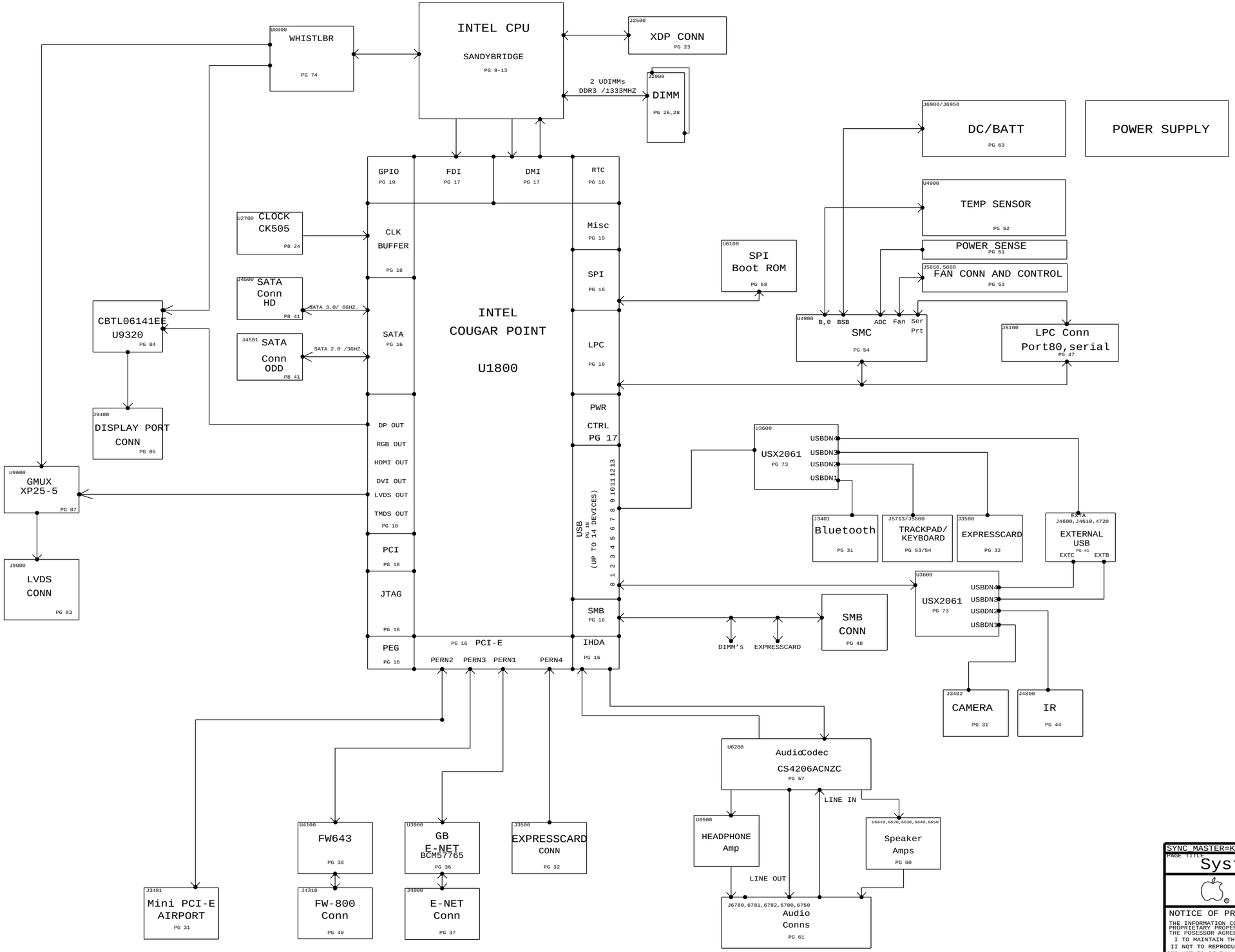

SYNC_MASTER=K60_MLB SYNC_DATE=04/26/2010

PAGE TITLE

System Block Diagram

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K92 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN — DCIN(16.5V) — F6905 6A FUSE — PPDCIN_G3H_OR_PBUS_R — R6990 — D6990

R7020 — SMC_DCIN_ISENSE — U7000 ISL6259HRTZ PBUS SUPPLY/ BATTERY CHARGER (PAGE 64) — VIN — VOUT — PPVBAT_G3H_CHGR_REG

F7040 / F7041 8A FUSE — PPBUS_G3H

R7050 — SMC_BATT_ISENSE

J6950 2S4P (6 TO 8.4V) — PPVBATT_G3H_CONN — Q7055 — CHGR_BGATE — PPVBAT_G3H_CHGR_R

SMC_PBUS_VSENSE — Q5315 — ENABLE 3.425V G3HOT PM6640 U6990 (PAGE 63) — PP3V42_G3H

SMC PWRGD NCP303LSN U5000 (PAGE 46) — SMC_RESET_L

SMC AVREF SUPPLY REF3333 (PAGE 46) — VIN — VOUT — PP3V3_S5_AVREF_SMC

PP3V42_G3H — SMC_TPAD_RST_L — SMC_ONOFF_L — U5001

PP5V_S3_GFXIMVP6_VDD — GPU VCORE ISL6263C U8900 (PAGE 82) — VR_ON — PGOOD — GPUVCORE_EN — GPUVCORE_PGOOD

SMC_GPU_VSENSE — U5410 — SMC_GPU_ISENSE — PPVCORE_GPU

PP5V_S0_CPUVTTS0 — 1.05V ISL95870 U7600 (PAGE 70) — CPUVTTS0_EN — CPUVTTS0_PGOOD

R7640 — PPCPUVTT_S0 — SMC_CPU_FSB_ISENSE

PPCPUVCCIO_S3 — TPS22924 U4202 (PAGE 39) — PP1V0_FW — FW_PWR_EN

SMC_CPU_HI_ISENSE — R5388 — CPU VCORE ISL95831 U7400 (PAGE 68) — CPUIMVP7_VR_ON — SMC_CPU_ISENSE — SMC_CPU_VSENSE — PPVCORE_S0_CPU

CPUIMVP7_PGOOD

COUGAR_POINT — PM_PWRBTN_L — PWRBTN — SYS_RESET# — RSMRST# — ACPRESET# — PLTRST# — PROCPWRGD — DRAMPWRGK — PLT_RERST_L — CPU_PWRGD — PM_MEM_PWRGD — PM_PCH_PWRGD — PS_PWRGD — U1800 (PAGE 16-21) — U2850

CPU U1000 (PAGE 9-14) — SM_DRAMPWRGK — VCCCPUPWRGD — RESET#

GMUX U9600 XP25-5 (PAGE 87) — PB16B EG_RAIL1_EN — PB17A EG_RAIL2_EN — P3V3GPU_EN — PB17B EG_RAIL3_EN — GPUVCORE_EN — PB18A EG_RAIL4_EN — PL32A PM_ALL_GPU_PGOOD

SMC U4900 (PAGE 45) — P60 — SMC_PM_G2_EN — RC DELAY — P3V3S5_EN

COUGAR_POINT U1800 (PAGE 16-21) — SLP_S5#(F4) — PM_SLP_S5_L — SLP_S4#(H7) — PM_SLP_S4_L — SLP_S3#(P12) — PM_SLP_S3_L — R7978 — PM_SLP_S3_L_R

RC DELAY — P1V8S0_EN — P1V2S0_EN — CPUVTTS0_EN — P1V5CPU_EN — P5VS0_EN — P3V3S0_EN — PBUSVSENS_EN

P1V0GPU_EN — P1V5FB_EN — EN1 1.103V(L/H) EN2 1.8V(R/H) ISL6236 U9500 (PAGE 86) — VOUT1 — VOUT2 — POK1 — POK2 — P1V0GPU_PGOOD — P1V5FB_PGOOD

R5410 — PP1V0_S0GPU — PP1V5R1V35_GPU_FB_ISNS — SMC_GPU_1V5_ISENSE

PP5V_S3 — DDRREG_EN — MEMVTT_EN — S5 S3 TPS51916 U7300 (PAGE 67) — VIN VLDOIN — 1.5V 0.75V — VOUT1 — VOUT2 — PGOOD

R7350/U5440 — SMC_DDR_ISENSE — PPDDR_S3_REG — PP1V5_S3 — PPVTT_S0_DDR_LDO — DDRREG_PGOOD

PP5V_S5 — P1V5CPU_EN — SLG5AP020 U7801 (PAGE 54) — ON — VOUT — PP1V5_S3RS0

Q7860 — PP5V_S0_FET — PP3V3_S0 — MAX8840 U6201 (PAGE 57) — EN — VIN — VOUT — PP4V5_AUDIO_ANALOG

P5VS3_EN — P3V3S5_EN — VIN VREG5 EN1 5V (L/H) EN2 3.3V (R/H) TPS51980 U7201 (PAGE 66) — VOUT1 — VOUT2 — PGOOD1 PGOOD2 — RD220 — PP5V_S3 — P3V3_S5 — P3V3S5_PGOOD — P5VS3_PGOOD

P5VS0_EN — TPS61045 U5805 (PAGE 54) — PP18V5_S3

PM_ALL_GPU_PGOOD — U7980 — ALL_SYS_PWRGD — RSMRST_PWRGD — SMC_ONOFF_L

SMC — PWRGD(P12) — RSMRST_IN(P13) — PWR_BUTTON(P90) — RSMRST_OUT(P86) — 99ms DLY — SMC_ADAPTER_EN — PM_RSMRST_L — IMVP_VR_ON — PM_SYSRST_L — PM_PWRBTN_L — SMC_RESET_L — SLP_S5_L(P95) — SLP_S4_L(P94) — SLP_S3_L(P93) — H8S2117 U4900 (PAGE 45)

Q9806 — BKLT_PLT_RST_L && LCD_BKLT_EN — BKLT_EN — VIN LP8545SQX U9701 (PAGE 88) — ENA — VOUT — PPVOUT_S0_LCDBKLT

Q4260 — SMC_ADAPTER_EN&&PM_SLP_S3_L — VIN LTC1872 U7790 (PAGE 71) — VOUT — PP10V_FW

Q7870 — P3V3_S0_GPU — P3V3GPU_EN

Q7810 — P3V3_S3 — P3V3S3_EN

Q7830 — P3V3_S0_FET — P3V3S0_EN — TPS22924 U4201 (PAGE 39) — PP3V3_FW_FWPHY — FW_PWR_EN

P1V5_S0_EN — ISL8009B U7710 (PAGE 71) — PP1V5_S0

Q7922 — PP3V3_ENET — PM_SLP_S3_L&&WOL_EN||SMC_ADAPTER_EN

PP3V3_S0_PWRCTL — P1V8S0_PGOOD — P5VS3_PGOOD — S0PGOOD_PWROK

PP3V3_S0 — U7971 ISL88042IRTJJZ — VCC — V2MON — V3MON — V4MON — RST — PG — (PAGE 73) — TRST = 200mS — P1V2ENET_PGOOD

PP3V3_S0_VMON — PP1V5_S0_VMON — PP1V05_S0_VMON

P1V8_S0_EN — ISL8014 U7720 (PAGE 70) — EN — VIN — VOUT — PGOOD — PP1V8_S0 — P1V8S0_PGOOD — PP3V3_FW_FET

Q7850 — P1V2_S0 — P1V2GMUX_EN

P1V2ENET_EN — ISL8014A U7760 (PAGE 71) — PP1V2_ENET

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PROTO2/EVT 11/11/10 rev3.0 for board 820-2914-05.brd release
PROTO2/EVT 11/15/10 rev3.6 for board 820-2914-06.brd release
PROTO2/EVT 11/19/10 rev3.7 for board 820-2914-07.brd release
EVT 11/22/10 rev3.9 for board 820-2914-07.brd release

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Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1303	PCBA,MLB,K92	K92_COMMON,CPU:2_2GHZ,FB_1G_SAMSUNG,EEEE_DG5Y
639-1464	PCBA,MLB,CFG2,K92	K92_COMMON,CPU:2_2GHZ,FB_1G_HYNIX,VRAM_HYNIX,EEEE_DG60
639-1466	PCBA,MLB,CFG3,K92	K92_COMMON,CPU:2_3GHZ,FB_1G_SAMSUNG,EEEE_DG62
639-1465	PCBA,MLB,CFG4,K92	K92_COMMON,CPU:2_3GHZ,FB_1G_HYNIX,VRAM_HYNIX,EEEE_DG61
085-1898	K92 MLB DEVELOPMENT BOM	K92_DEVEL:ENG

K92 BOM GROUPS

BOM GROUP	BOM OPTIONS
K92_COMMON	ALTERNATE,COMMON,K92_COMMON1,K92_COMMON2,K92_PROGPARTS
K92_COMMON1	CPUMEM_S0,EXT_HP_AMP,SMC_DEBUG_YES,USBHUB_2514B
K92_COMMON2	GPUVID_1P11V,HUB1_2NONREM,HUB2_2NONREM,KB_BL,ENET:B0,T29BST:Y,T29:YES,T29_DP_HPD:ALL_OR
K92_DEVEL:ENG	SNB_CPT_XDP,DEBUG_ADC,LPCPLUS:YES,VREFMRGN,GMUX_JTAG_CONN,S0PGOOD_ISL,BMON:ENG,CPURIPPLE_ENG,IMVPISNS_ENG,SDRVI2C:MCU
K92_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS:YES,VREFMRGN_NOT
K92_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:EVT,ENETROM_PROG:B0_NOSD,TPAD_PROG:EVT,T29ROM:PROG,GMUX_PROG,T29MCU:PROG
K92_PVT	VREFMRGN_NOT,XDP,XDP_CPU_BPM,BMON:PROD
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Y]	CRITICAL	EEEE_DG5Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG60]	CRITICAL	EEEE_DG60
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG61]	CRITICAL	EEEE_DG61
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG62]	CRITICAL	EEEE_DG62

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ.D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT SLH9D,PRQ,BD82HM63	U1800	CRITICAL	
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	
338S0945	1	Light Ridge,S LHAJ,FCBGA,15x15mmm	U3600	CRITICAL	T29:YES
353S3055	1	IC, P13VEDP212,x2 DISPLAYPORT 2:1 MUX, QFN	U9390	CRITICAL	

Programmed Parts-All Builds

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S2899	1	IC,T29 EEPROM,K92	U3690	CRITICAL	T29ROM:PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
335S0724	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2996	1	IC,GMUX,K92	U9600	CRITICAL	GMUX_PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGRAMMED MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:PROG

GPUROM will NOSUFFED @EVT

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
157S0058	157S0055		ALL	Delta alt to TDK Magnetics	
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC	
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC	
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA	
516S0805	516S0806		ALL	FOXCONN ALT TO MOLEX	
353S2805	353S2603		ALL	Fairchild 8' alt to 6'wafer	
127S0111	127S0060		ALL	Rohm alt to Kemet	
353S3085	353S1658		ALL	ST Micro alt to LT	(U5850)
152S0905	152S1307		ALL	Cyntec (used on K90i) as alt	(L7630)
353S3055	353S3151		ALL	Pericom alt to NXP DP Mux	(U9390)
376S0855	376S0613		ALL	radar8515240 Toshiba FET	(Q3200, etc)
870-1939	870-1698		ALL	Silver alt to Gold tall pogo pins	
870-2015	870-1699		ALL	Silver alt to Gold short pogo pins	
376S0972	376S0612		ALL	add ROHM part as 2nd source	
138S0676	138S0691		ALL	add Murata part as 2nd source	
128S0327	128S0264		ALL	add NEC part as 2nd source	
376S0977	376S0859		ALL	add new part as 2nd source	
138S0681	138S0638		ALL	add new part as 2nd source	(Q3888,Q9430)

SMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0895	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2855	1	IC,SMC,DEVELOPMENT-PROTO,K92	U4900	CRITICAL	SMC_PROG:PROTO0
341S2855	1	IC,SMC,DEVELOPMENT-PROTO1,K92	U4900	CRITICAL	SMC_PROG:PROTO1
341S2995	1	IC,SMC,DEVELOPMENT-PROTO2,K92	U4900	CRITICAL	SMC_PROG:PROTO2
341S2862	1	IC,SMC,DEVELOPMENT-EVT,K92	U4900	CRITICAL	SMC_PROG:EVT
341S2865	1	IC,SMC,DEVELOPMENT-DVT,K92	U4900	CRITICAL	SMC_PROG:DVT
341S2868	1	IC,SMC,DEVELOPMENT-PVT,K92	U4900	CRITICAL	SMC_PROG:PVT

EFI

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

Ethernet

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0539	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET ROM,PROTO1,K92	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S3027	1	IC,ENET ROM, PROTO2, EVT,DVT,PVT,K92	U3990	CRITICAL	ENETROM_PROG:B0_NOSD

PSOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S2902	1	IC,TP PSOC,PROTO,K90,K90i,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3024	1	IC,TP PSOC,proto2,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,proto1,EVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:EVT
341S3024	1	IC,TP PSOC,proto1,DVT,pVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:DVTPVT

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PAGE TITLE: BOM Configuration

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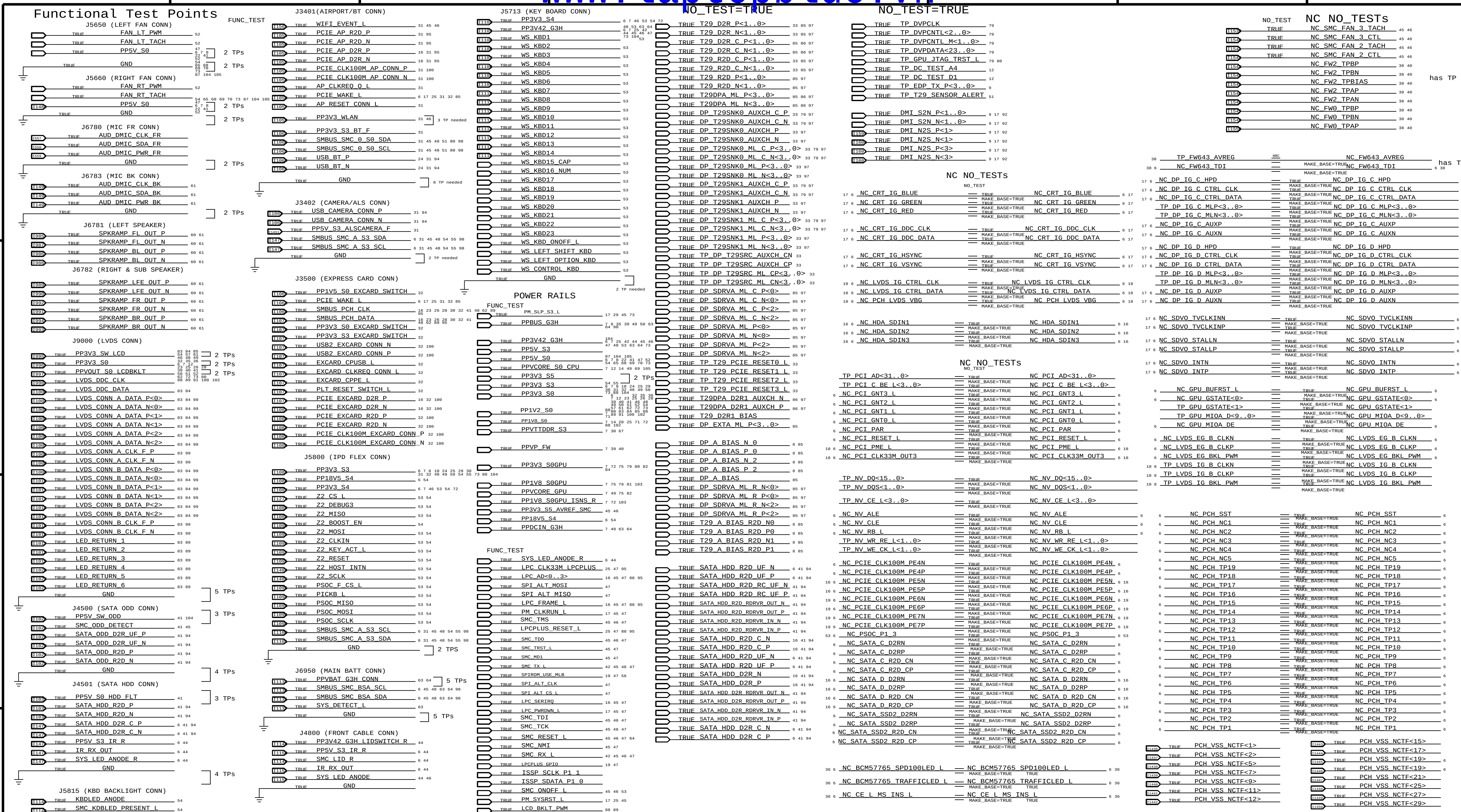

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Functional / ICT Test

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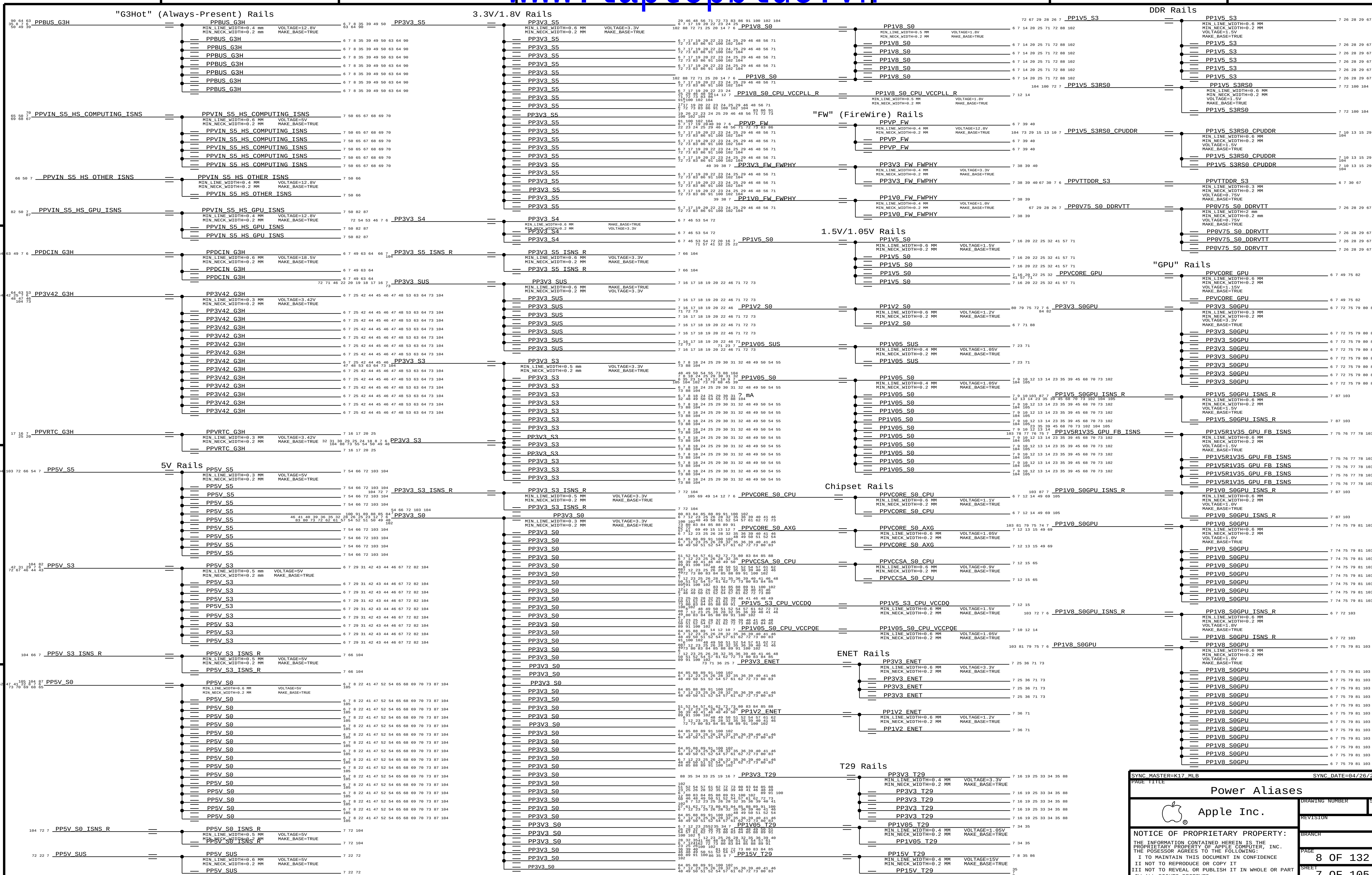

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Thermal Module Holes

Bottom GPU Right TM Hole — ZT0982 STDOFF-4.5OD.98H-1.1-3.48-TH
Right CPU TM Hole — ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0983 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
Left CPU TM Hole
Bottom CPU Left TM Hole
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
Bottom GPU Left TM Hole
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
Top GPU Center TM Hole
ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND
ZT0932 3R2P5
ZT0960 3R2P5
ZT0971 3R2P5
ZT0940 3R2P5
ZT0970 3R2P5

SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0936 1.4DIA-SHORT-EMI-MLB-M97-M98
GND_CHASSIS_AUDIO_JACK
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0924 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98
SH0931 2.0DIA-TALL-EMI-MLB-M97-M98
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98

ZT0934 STDOFF-4.0OD3.35H-TH
ZT0931 STDOFF-4.0OD3.35H-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Bosses for Flex Protector Bracket

ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35

GMUX ALIASES

PM_ALL_GPU_PGOOD — MAKE_BASE=TRUE — 91 88 87 82 74 8 — PM_ALL_GPU_PGOOD — 8 74 82 87 88 91
TP_LVDS_MUX_SEL_EG — MAKE_BASE=TRUE — 88 8 — TP_LVDS_MUX_SEL_EG — 8 88
EG_RESET_L — MAKE_BASE=TRUE — 88 74 8 — EG_RESET_L — 8 74 88
LVDS_IG_BKL_ON — MAKE_BASE=TRUE — 88 18 8 — LVDS_IG_BKL_ON — 8 18 88
LVDS_IG_PANEL_PWR — MAKE_BASE=TRUE — 88 18 8 — LVDS_IG_PANEL_PWR — 8 18 88
LCD_BKLT_EN — MAKE_BASE=TRUE — 90 88 8 — LCD_BKLT_EN — 8 88 90
PEX_CLKREQ_L — MAKE_BASE=TRUE — 88 80 8 — PEX_CLKREQ_L — 8 80 88
PEG_CLKREQ_L — MAKE_BASE=TRUE — 88 16 8 — PEG_CLKREQ_L — 8 16 88
GND — GND — MAKE_BASE=TRUE
FW_PLUG_DET_L — MAKE_BASE=TRUE — 39 19 8 — FW_PLUG_DET_L — 8 19 39
FW643_WAKE_L — MAKE_BASE=TRUE — 39 38 8 — FW643_WAKE_L — 8 38 39

Unused SD card signals

TP_SDCONN_DATA<0..7> — MAKE_BASE=TRUE — 36 — SDCONN_DATA<0..7> — 8 36
TP_SDCONN_CLK — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_CLK — 8 36
TP_SDCONN_CMD — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_CMD — 8 36
TP_SDCONN_DETECT_L — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_DETECT_L — 8 36
TP_SDCONN_WP — MAKE_BASE=TRUE — 36 8 — TP_SDCONN_WP — 8 36
TP_ENET_CR_PWREN — MAKE_BASE=TRUE — 36 8 — TP_ENET_CR_PWREN — 8 36

AUDIO ALIASES

PP5V_S0 — 91 88 87 82 74 70 69 68 65 54 52 47 41 22 7 6 105 104
XW0900 — PP5V_S0_AUDIO — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V — 57
XW0901 — PP5V_S0_AUDIO_AMP_R — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V — 60
XW0902 — PP5V_S0_AUDIO_AMP_L — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V — 60

Digital Ground

GND — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.11MM, VOLTAGE=0V
LVDS_IG_PANEL_PWR — 88 18 8 — R0902 100K 5% 1/16W MF-LF 402 2

Unused USB ports

PP3V3_S3 — 6 7 18 24 25 29 30 31 32 48 49 50 54 55 73 88 104
R0915 10K 5% 1/16W MF-LF 402 2
R0916 10K 5% 1/16W MF-LF 402 2
USB_T29A_N — 24 94
USB_T29A_P — 24 94

Heat spreader mounting boss for T29 router

SH0940 STDOFF-4.0OD1.85H-SM
SH0941 STDOFF-4.0OD1.85H-SM

Heat spreader mounting boss for PCH

SH0942 STDOFF-4.0OD2.23H-SM
SH0943 STDOFF-4.0OD2.23H-SM

CPU signals

CPU_VID<0..6> — MAKE_BASE=TRUE — 92 — CPUIMVP_VID<0..6> — 8
GFX_VID<0..6> — MAKE_BASE=TRUE — 92 — GFXIMVP_VID<0..6> — 8
MEMVTT_EN — MAKE_BASE=TRUE — 67 29 8 — MEMVTT_EN — 8 29 67

Unused PEG lanes

NC_PEG_D2R_P<15..12> — MAKE_BASE=TRUE — 9 — =PEG_D2R_P<15..12> — 9
NC_PEG_D2R_N<15..12> — MAKE_BASE=TRUE — 9 — =PEG_D2R_N<15..12> — 9
NC_PEG_R2D_C_P<15..12> — MAKE_BASE=TRUE — 9 — =PEG_R2D_C_P<15..12> — 9
NC_PEG_R2D_C_N<15..12> — MAKE_BASE=TRUE — 9 — =PEG_R2D_C_N<15..12> — 9

GPU signals

PEG_D2R_P<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_D2R_P<7..0> — 9
PEG_D2R_N<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_D2R_N<7..0> — 9
PEG_R2D_C_P<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_R2D_C_P<7..0> — 9
PEG_R2D_C_N<7..0> — MAKE_BASE=TRUE — 92 74 — =PEG_R2D_C_N<7..0> — 9
DP_IG_AUX_CH_P — MAKE_BASE=TRUE — 94 84 17 8 — DP_IG_AUX_CH_P — 8 17 84 94
DP_IG_AUX_CH_N — MAKE_BASE=TRUE — 94 84 17 8 — DP_IG_AUX_CH_N — 8 17 84 94
DP_IG_DDC_CLK — MAKE_BASE=TRUE — 84 80 17 8 — DP_IG_DDC_CLK — 8 17 80 84
DP_IG_DDC_DATA — MAKE_BASE=TRUE — 84 80 17 8 — DP_IG_DDC_DATA — 8 17 80 84
DP_IG_HPD — MAKE_BASE=TRUE — 84 17 8 — DP_IG_HPD — 8 17 84

T29 Signals

PCIE_T29_D2R_P<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_D2R_P<11..8> — 9
PCIE_T29_D2R_N<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_D2R_N<11..8> — 9
PCIE_T29_R2D_C_P<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_R2D_C_P<11..8> — 9
PCIE_T29_R2D_C_N<3..0> — MAKE_BASE=TRUE — 95 33 — =PEG_R2D_C_N<11..8> — 9

Unused T29 Ports

T29_D2R_P<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_D2RP<2..3> — 33
T29_D2R_N<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_D2RN<2..3> — 33
T29_R2D_C_P<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_R2D_CP<2..3> — 33
T29_R2D_C_N<2..3> — MAKE_BASE=TRUE NO_TEST=TRUE — 97 — NC_T29_R2D_CN<2..3> — 33
T29_LSE0_LSOE3 — MAKE_BASE=TRUE NO_TEST=TRUE — 33 8 — T29_LSE0_LSOE3 — T29_LSE0_LSOE3 — 8 33
T29_LSE0_LSOE2 — MAKE_BASE=TRUE NO_TEST=TRUE — 33 8 — T29_LSE0_LSOE2 — T29_LSE0_LSOE2 — 8 33

T29 / GMUX JTAG Signals

JTAG_ISP_TCK — MAKE_BASE=TRUE — 88 33 23 19 8 — JTAG_ISP_TCK — 8 19 23 33 88
JTAG_ISP_TDI — MAKE_BASE=TRUE — 88 33 19 8 — JTAG_ISP_TDI — 8 19 33 88
JTAG_ISP_TDO — MAKE_BASE=TRUE — 88 33 19 8 — JTAG_ISP_TDO — 8 19 33 88

T29_A_BIAS caps

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0926 51 5% 1/20W MF 201 — T29_A_BIAS_D2R_P1 — 86
C0906 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0927 51 5% 1/20W MF 201 — T29_A_BIAS_D2R_N1 — 86
C0907 0.01UF 10% 10V X5R 201 SIGNAL_=EMPTY

DP_A_BIAS caps

DP_A_BIAS_P_2 — 85 6 — SIGNAL_MODEL=EMPTY — C0910 0.01UF 10% 10V X5R 201
DP_A_BIAS_P_0 — 85 6 — SIGNAL_MODEL=EMPTY — C0911 0.01UF 10% 10V X5R 201

T29BST:N
PPBUS_G3H — 90 64 63 50 49 39 35 7 6 — R0950 0 5% 1/8W MF-LF 805 — PP15V_T29 — 7 35 86

USB Hub Aliases

EXCARD_OC_L — MAKE_BASE=TRUE — 32 24 8 — EXCARD_OC_L — 8 24 32
USB_EXTC_OC_L — MAKE_BASE=TRUE — 43 24 8 — USB_EXTC_OC_L — 8 24 43
USB_EXCARD_N — MAKE_BASE=TRUE — 100 32 24 8 — USB_EXCARD_N — 8 24 32 100
USB_EXCARD_P — MAKE_BASE=TRUE — 100 32 24 8 — USB_EXCARD_P — 8 24 32 100

Rev. A NCs

NC_ISNS_P1V05S0PCH_N — MAKE_BASE=TRUE — 8 — NC_ISNS_P1V05S0PCH_N — 8
NC_ISNS_P1V05S0PCH_P — MAKE_BASE=TRUE — 8 — NC_ISNS_P1V05S0PCH_P — 8
NC_ISNS_P3V3S0MPCH_N — MAKE_BASE=TRUE — 8 — NC_ISNS_P3V3S0MPCH_N — 8
NC_ISNS_P3V3S0MPCH_P — MAKE_BASE=TRUE — 8 — NC_ISNS_P3V3S0MPCH_P — 8
NC_ISNS_PVTTS0PCH_N — MAKE_BASE=TRUE — 8 — NC_ISNS_PVTTS0PCH_N — 8
NC_ISNS_PVTTS0PCH_P — MAKE_BASE=TRUE — 8 — NC_ISNS_PVTTS0PCH_P — 8

T29_A_BIAS caps

SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_P0 — 6 85
C0901 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_N0 — 6 85
C0902 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_P1 — 6 85
C0903 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY
T29_A_BIAS_R — 86 8 — R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_N1 — 6 85
C0904 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

DP_A_BIAS caps

DP_A_BIAS_N_2 — 85 6 — SIGNAL_MODEL=EMPTY — C0905 0.01UF 10% 10V X5R 201
DP_A_BIAS_N_0 — 85 6 — SIGNAL_MODEL=EMPTY — C0908 0.01UF 10% 10V X5R 201

SYNC_MASTER=K17_MLB — SYNC_DATE=04/26/2010
PAGE TITLE: Signal Aliases
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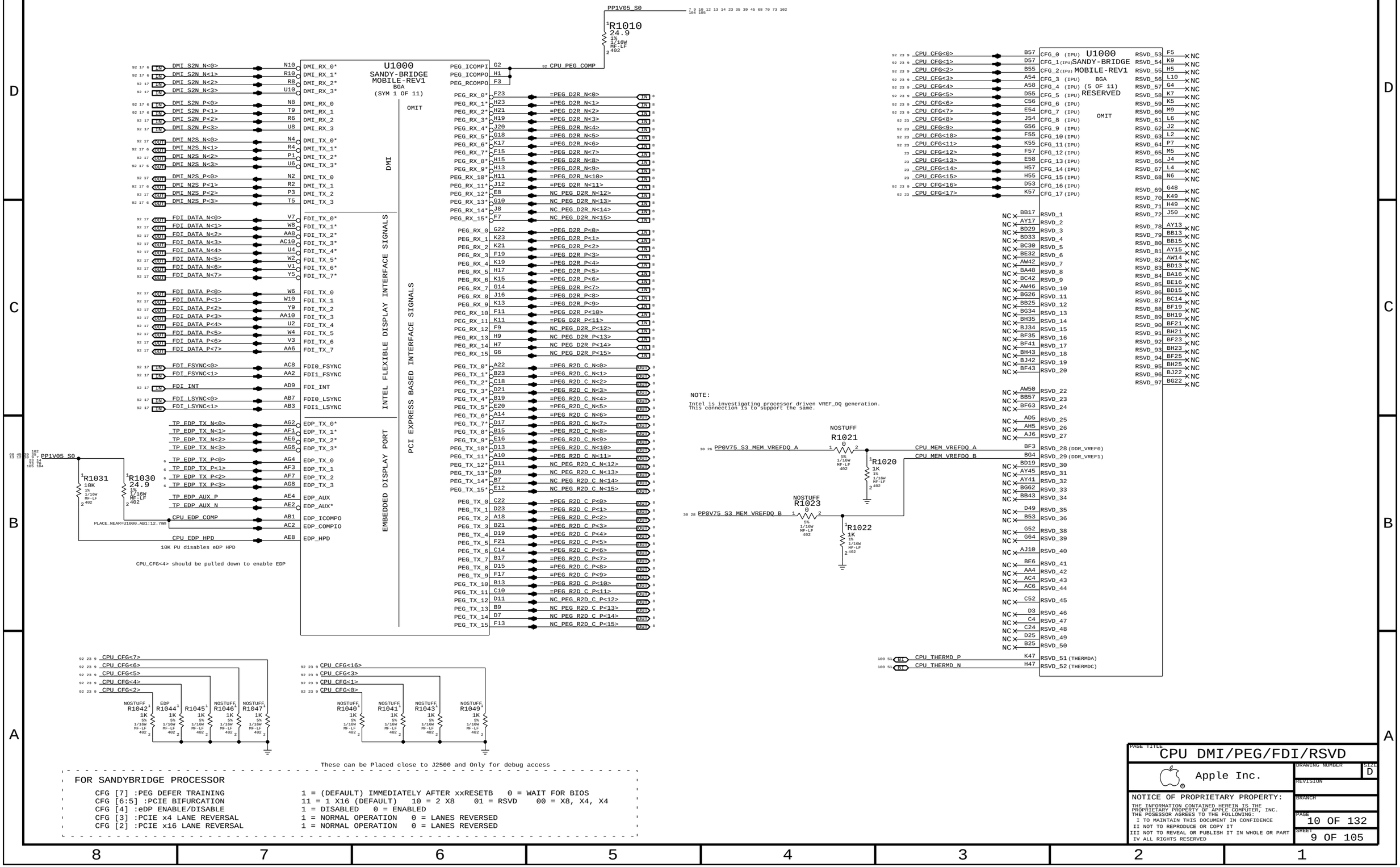

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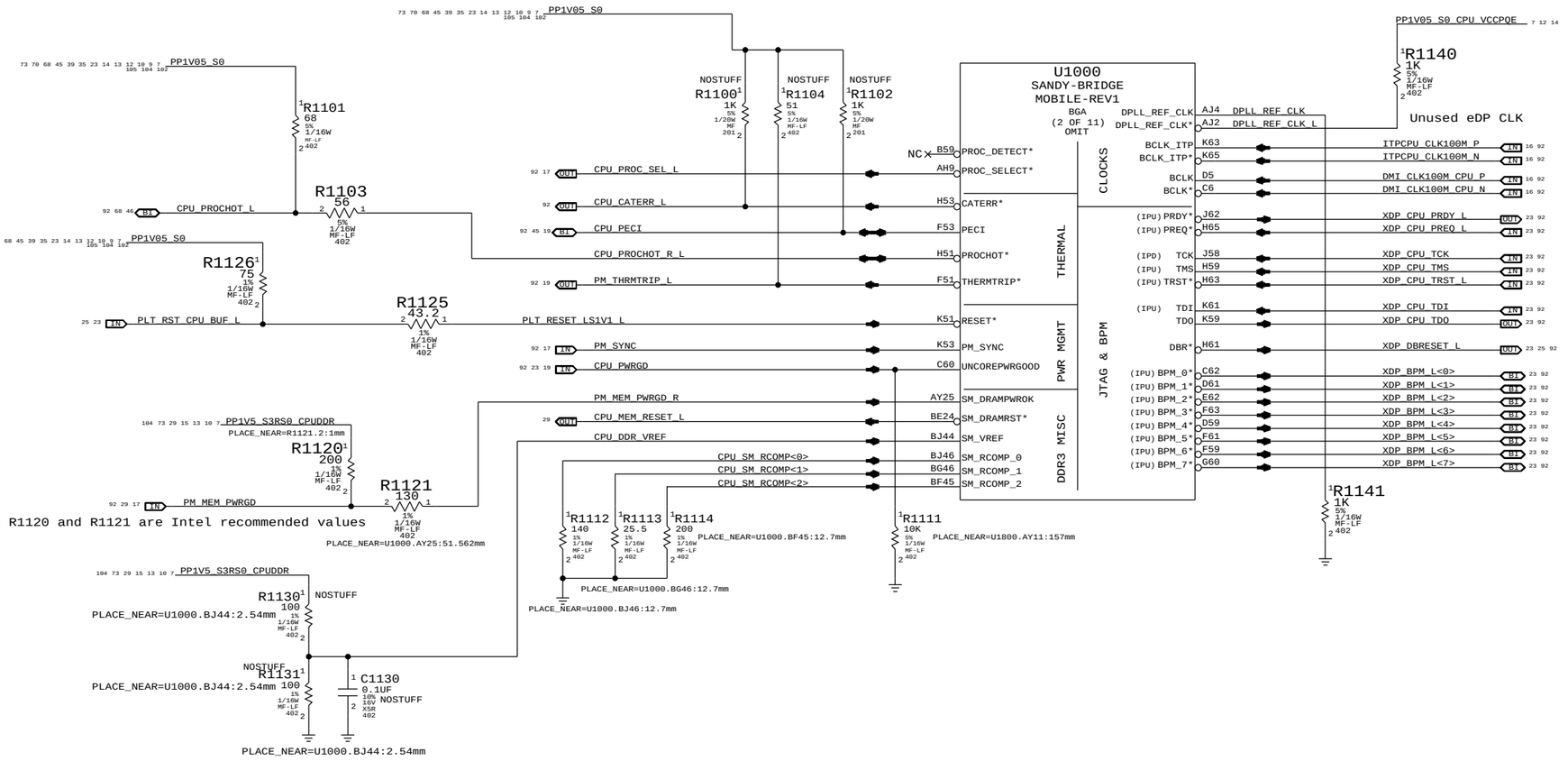

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CPU CLOCK/MISC/JTAG

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OMIT

MEMORY CHANNEL A

MEM_A_DQ<0>	AL6	SA_DQ_0	SA_CK_0	BB31	MEM_A_CLK_P<0>	26 93
MEM_A_DQ<1>	AL8	SA_DQ_1	SA_CK_0*	BA32	MEM_A_CLK_N<0>	26 93
MEM_A_DQ<2>	AP7	SA_DQ_2	SA_CKE_0	BC18	MEM_A_CKE<0>	26 93
MEM_A_DQ<3>	AM5	SA_DQ_3				
MEM_A_DQ<4>	AK7	SA_DQ_4	SA_CK_1	AW34	MEM_A_CLK_P<1>	26 93
MEM_A_DQ<5>	AL10	SA_DQ_5	SA_CK_1*	AY33	MEM_A_CLK_N<1>	26 93
MEM_A_DQ<6>	AN10	SA_DQ_6	SA_CKE_1	BD17	MEM_A_CKE<1>	26 93
MEM_A_DQ<7>	AM9	SA_DQ_7				
MEM_A_DQ<8>	AR10	SA_DQ_8	SA_CS_0*	BD41	MEM_A_CS_L<0>	26 93
MEM_A_DQ<9>	AR8	SA_DQ_9	SA_CS_1*	BD45	MEM_A_CS_L<1>	26 93
MEM_A_DQ<10>	AV7	SA_DQ_10				
MEM_A_DQ<11>	AY5	SA_DQ_11	SA_ODT_0	BB41	MEM_A_ODT<0>	26 93
MEM_A_DQ<12>	AT5	SA_DQ_12	SA_ODT_1	BC46	MEM_A_ODT<1>	26 93
MEM_A_DQ<13>	AR6	SA_DQ_13				
MEM_A_DQ<14>	AW6	SA_DQ_14	SA_DQS_0*	AN8	MEM_A_DQS_N<0>	26 27 93
MEM_A_DQ<15>	AT9	SA_DQ_15	SA_DQS_1*	AU6	MEM_A_DQS_N<1>	27 93
MEM_A_DQ<16>	BA6	SA_DQ_16	SA_DQS_2*	BC6	MEM_A_DQS_N<2>	27 93
MEM_A_DQ<17>	BA8	SA_DQ_17	SA_DQS_3*	BD9	MEM_A_DQS_N<3>	27 93
MEM_A_DQ<18>	BG6	SA_DQ_18	SA_DQS_4*	BC50	MEM_A_DQS_N<4>	27 93
MEM_A_DQ<19>	AY9	SA_DQ_19	SA_DQS_5*	BB55	MEM_A_DQS_N<5>	27 93
MEM_A_DQ<20>	AW8	SA_DQ_20	SA_DQS_6*	BD59	MEM_A_DQS_N<6>	27 93
MEM_A_DQ<21>	BB7	SA_DQ_21	SA_DQS_7*	AU60	MEM_A_DQS_N<7>	27 93
MEM_A_DQ<22>	BC8	SA_DQ_22				
MEM_A_DQ<23>	BE4	SA_DQ_23	SA_DQS_0	AN6	MEM_A_DQS_P<0>	27 93
MEM_A_DQ<24>	AW12	SA_DQ_24	SA_DQS_1	AU8	MEM_A_DQS_P<1>	27 93
MEM_A_DQ<25>	AV11	SA_DQ_25	SA_DQS_2	BD5	MEM_A_DQS_P<2>	27 93
MEM_A_DQ<26>	BB11	SA_DQ_26	SA_DQS_3	BC10	MEM_A_DQS_P<3>	27 93
MEM_A_DQ<27>	BA12	SA_DQ_27	SA_DQS_4	BB51	MEM_A_DQS_P<4>	27 93
MEM_A_DQ<28>	BE8	SA_DQ_28	SA_DQS_5	BD55	MEM_A_DQS_P<5>	27 93
MEM_A_DQ<29>	BA10	SA_DQ_29	SA_DQS_6	BD61	MEM_A_DQS_P<6>	27 93
MEM_A_DQ<30>	BD11	SA_DQ_30	SA_DQS_7	AV61	MEM_A_DQS_P<7>	27 93
MEM_A_DQ<31>	BE12	SA_DQ_31				
MEM_A_DQ<32>	BB49	SA_DQ_32	SA_MA_0	BD27	MEM_A_A<0>	26 93
MEM_A_DQ<33>	AY49	SA_DQ_33	SA_MA_1	BA28	MEM_A_A<1>	26 93
MEM_A_DQ<34>	BE52	SA_DQ_34	SA_MA_2	BB27	MEM_A_A<2>	26 93
MEM_A_DQ<35>	BD51	SA_DQ_35	SA_MA_3	AW26	MEM_A_A<3>	26 93
MEM_A_DQ<36>	BD49	SA_DQ_36	SA_MA_4	BB23	MEM_A_A<4>	26 93
MEM_A_DQ<37>	BE48	SA_DQ_37	SA_MA_5	BA24	MEM_A_A<5>	26 93
MEM_A_DQ<38>	BA52	SA_DQ_38	SA_MA_6	AY21	MEM_A_A<6>	26 93
MEM_A_DQ<39>	AY51	SA_DQ_39	SA_MA_7	BD21	MEM_A_A<7>	26 93
MEM_A_DQ<40>	BC54	SA_DQ_40	SA_MA_8	BC22	MEM_A_A<8>	26 93
MEM_A_DQ<41>	AY53	SA_DQ_41	SA_MA_9	BB21	MEM_A_A<9>	26 93
MEM_A_DQ<42>	AW54	SA_DQ_42	SA_MA_10	AW38	MEM_A_A<10>	26 93
MEM_A_DQ<43>	AY55	SA_DQ_43	SA_MA_11	AW22	MEM_A_A<11>	26 93
MEM_A_DQ<44>	BD53	SA_DQ_44	SA_MA_12	BA20	MEM_A_A<12>	26 93
MEM_A_DQ<45>	BB53	SA_DQ_45	SA_MA_13	BB45	MEM_A_A<13>	26 93
MEM_A_DQ<46>	BE56	SA_DQ_46	SA_MA_14	BE20	MEM_A_A<14>	26 93
MEM_A_DQ<47>	BA56	SA_DQ_47	SA_MA_15	AW18	MEM_A_A<15>	26 93
MEM_A_DQ<48>	BD57	SA_DQ_48				
MEM_A_DQ<49>	BF61	SA_DQ_49				
MEM_A_DQ<50>	BA60	SA_DQ_50				
MEM_A_DQ<51>	BB61	SA_DQ_51				
MEM_A_DQ<52>	BE60	SA_DQ_52				
MEM_A_DQ<53>	BD63	SA_DQ_53				
MEM_A_DQ<54>	BB59	SA_DQ_54				
MEM_A_DQ<55>	BC58	SA_DQ_55				
MEM_A_DQ<56>	AW58	SA_DQ_56				
MEM_A_DQ<57>	AY59	SA_DQ_57				
MEM_A_DQ<58>	AL60	SA_DQ_58				
MEM_A_DQ<59>	AP61	SA_DQ_59				
MEM_A_DQ<60>	AW60	SA_DQ_60				
MEM_A_DQ<61>	AY57	SA_DQ_61				
MEM_A_DQ<62>	AN60	SA_DQ_62				
MEM_A_DQ<63>	AR60	SA_DQ_63				
MEM_A_BA<0>	BA36	SA_BS_0				
MEM_A_BA<1>	BC38	SA_BS_1				
MEM_A_BA<2>	BB19	SA_BS_2				
MEM_A_CAS_L	BE44	SA_CAS*				
MEM_A_RAS_L	BE36	SA_RAS*				
MEM_A_WE_L	BA44	SA_WE*				

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OMIT

MEMORY CHANNEL B

MEM_B_DQ<0>	AL4	SB_DQ_0	SB_CK_0	BF33	MEM_B_CLK_P<0>	28 93
MEM_B_DQ<1>	AK3	SB_DQ_1	SB_CK_0*	BH33	MEM_B_CLK_N<0>	28 93
MEM_B_DQ<2>	AP3	SB_DQ_2	SB_CKE_0	BD25	MEM_B_CKE<0>	28 93
MEM_B_DQ<3>	AR2	SB_DQ_3				
MEM_B_DQ<4>	AL2	SB_DQ_4	SB_CK_1	BF37	MEM_B_CLK_P<1>	28 93
MEM_B_DQ<5>	AK1	SB_DQ_5	SB_CK_1*	BH37	MEM_B_CLK_N<1>	28 93
MEM_B_DQ<6>	AP1	SB_DQ_6	SB_CKE_1	BJ26	MEM_B_CKE<1>	28 93
MEM_B_DQ<7>	AR4	SB_DQ_7				
MEM_B_DQ<8>	AV3	SB_DQ_8	SB_CS_0*	BE40	MEM_B_CS_L<0>	28 93
MEM_B_DQ<9>	AU4	SB_DQ_9	SB_CS_1*	BH41	MEM_B_CS_L<1>	28 93
MEM_B_DQ<10>	BA4	SB_DQ_10				
MEM_B_DQ<11>	BB1	SB_DQ_11	SB_ODT_0	BG42	MEM_B_ODT<0>	28 93
MEM_B_DQ<12>	AV1	SB_DQ_12	SB_ODT_1	BH45	MEM_B_ODT<1>	28 93
MEM_B_DQ<13>	AU2	SB_DQ_13				
MEM_B_DQ<14>	BA2	SB_DQ_14	SB_DQS_0*	AN4	MEM_B_DQS_N<0>	27 28 93
MEM_B_DQ<15>	BB3	SB_DQ_15	SB_DQS_1*	AW2	MEM_B_DQS_N<1>	27 93
MEM_B_DQ<16>	BC2	SB_DQ_16	SB_DQS_2*	BH9	MEM_B_DQS_N<2>	27 93
MEM_B_DQ<17>	BF7	SB_DQ_17	SB_DQS_3*	BF15	MEM_B_DQS_N<3>	27 93
MEM_B_DQ<18>	BF11	SB_DQ_18	SB_DQS_4*	BF51	MEM_B_DQS_N<4>	27 93
MEM_B_DQ<19>	BJ10	SB_DQ_19	SB_DQS_5*	BH57	MEM_B_DQS_N<5>	27 93
MEM_B_DQ<20>	BC4	SB_DQ_20	SB_DQS_6*	AY63	MEM_B_DQS_N<6>	27 93
MEM_B_DQ<21>	BH7	SB_DQ_21	SB_DQS_7*	AN62	MEM_B_DQS_N<7>	27 93
MEM_B_DQ<22>	BH11	SB_DQ_22				
MEM_B_DQ<23>	BG10	SB_DQ_23	SB_DQS_0	AN2	MEM_B_DQS_P<0>	27 28 93
MEM_B_DQ<24>	BJ14	SB_DQ_24	SB_DQS_1	AW4	MEM_B_DQS_P<1>	27 93
MEM_B_DQ<25>	BG14	SB_DQ_25	SB_DQS_2	BF9	MEM_B_DQS_P<2>	27 93
MEM_B_DQ<26>	BF17	SB_DQ_26	SB_DQS_3	BH15	MEM_B_DQS_P<3>	27 93
MEM_B_DQ<27>	BJ18	SB_DQ_27	SB_DQS_4	BH51	MEM_B_DQS_P<4>	27 93
MEM_B_DQ<28>	BF13	SB_DQ_28	SB_DQS_5	BF57	MEM_B_DQS_P<5>	27 93
MEM_B_DQ<29>	BH13	SB_DQ_29	SB_DQS_6	AY65	MEM_B_DQS_P<6>	27 93
MEM_B_DQ<30>	BH17	SB_DQ_30	SB_DQS_7	AN64	MEM_B_DQS_P<7>	27 93
MEM_B_DQ<31>	BG18	SB_DQ_31				
MEM_B_DQ<32>	BH49	SB_DQ_32	SB_MA_0	BF31	MEM_B_A<0>	28 93
MEM_B_DQ<33>	BF47	SB_DQ_33	SB_MA_1	BH31	MEM_B_A<1>	28 93
MEM_B_DQ<34>	BH53	SB_DQ_34	SB_MA_2	BB37	MEM_B_A<2>	28 93
MEM_B_DQ<35>	BG50	SB_DQ_35	SB_MA_3	BC34	MEM_B_A<3>	28 93
MEM_B_DQ<36>	BF49	SB_DQ_36	SB_MA_4	BF27	MEM_B_A<4>	28 93
MEM_B_DQ<37>	BH47	SB_DQ_37	SB_MA_5	BB33	MEM_B_A<5>	28 93
MEM_B_DQ<38>	BF53	SB_DQ_38	SB_MA_6	BH27	MEM_B_A<6>	28 93
MEM_B_DQ<39>	BJ50	SB_DQ_39	SB_MA_7	BG30	MEM_B_A<7>	28 93
MEM_B_DQ<40>	BF55	SB_DQ_40	SB_MA_8	BH29	MEM_B_A<8>	28 93
MEM_B_DQ<41>	BH55	SB_DQ_41	SB_MA_9	BF29	MEM_B_A<9>	28 93
MEM_B_DQ<42>	BJ58	SB_DQ_42	SB_MA_10	AY37	MEM_B_A<10>	28 93
MEM_B_DQ<43>	BH59	SB_DQ_43	SB_MA_11	BJ30	MEM_B_A<11>	28 93
MEM_B_DQ<44>	BJ54	SB_DQ_44	SB_MA_12	AW30	MEM_B_A<12>	28 93
MEM_B_DQ<45>	BG54	SB_DQ_45	SB_MA_13	BA40	MEM_B_A<13>	28 93
MEM_B_DQ<46>	BG58	SB_DQ_46	SB_MA_14	BB29	MEM_B_A<14>	28 93
MEM_B_DQ<47>	BF59	SB_DQ_47	SB_MA_15	BE28	MEM_B_A<15>	28 93
MEM_B_DQ<48>	BA64	SB_DQ_48				
MEM_B_DQ<49>	BC62	SB_DQ_49				
MEM_B_DQ<50>	AU62	SB_DQ_50				
MEM_B_DQ<51>	AW64	SB_DQ_51				
MEM_B_DQ<52>	BA62	SB_DQ_52				
MEM_B_DQ<53>	BC64	SB_DQ_53				
MEM_B_DQ<54>	AU64	SB_DQ_54				
MEM_B_DQ<55>	AW62	SB_DQ_55				
MEM_B_DQ<56>	AR64	SB_DQ_56				
MEM_B_DQ<57>	AT65	SB_DQ_57				
MEM_B_DQ<58>	AL64	SB_DQ_58				
MEM_B_DQ<59>	AM65	SB_DQ_59				
MEM_B_DQ<60>	AR62	SB_DQ_60				
MEM_B_DQ<61>	AT63	SB_DQ_61				
MEM_B_DQ<62>	AL62	SB_DQ_62				
MEM_B_DQ<63>	AM63	SB_DQ_63				
MEM_B_BA<0>	BJ38	SB_BS_0				
MEM_B_BA<1>	BD37	SB_BS_1				
MEM_B_BA<2>	AY29	SB_BS_2				
MEM_B_CAS_L	BH39	SB_CAS*				
MEM_B_RAS_L	BG38	SB_RAS*				
MEM_B_WE_L	BF39	SB_WE*				

SYNC_DATE=04/26/2010

PAGE TITLE: CPU DDR3 INTERFACES

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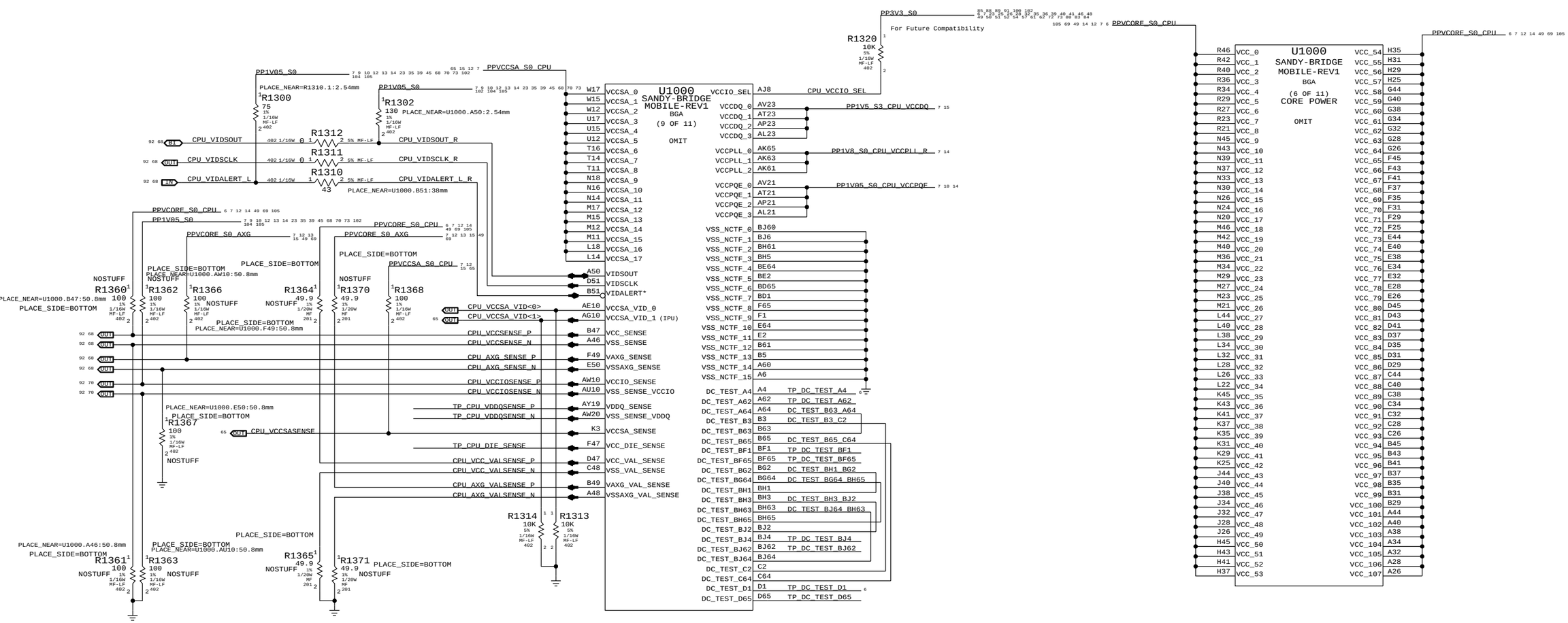

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K91_MLB SYNC_DATE=07/16/2010

PAGE TITLE: CPU POWER

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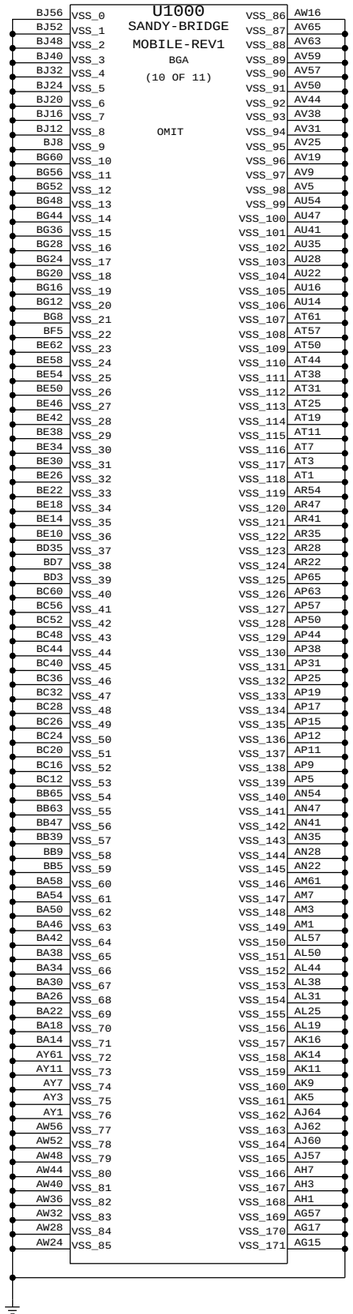
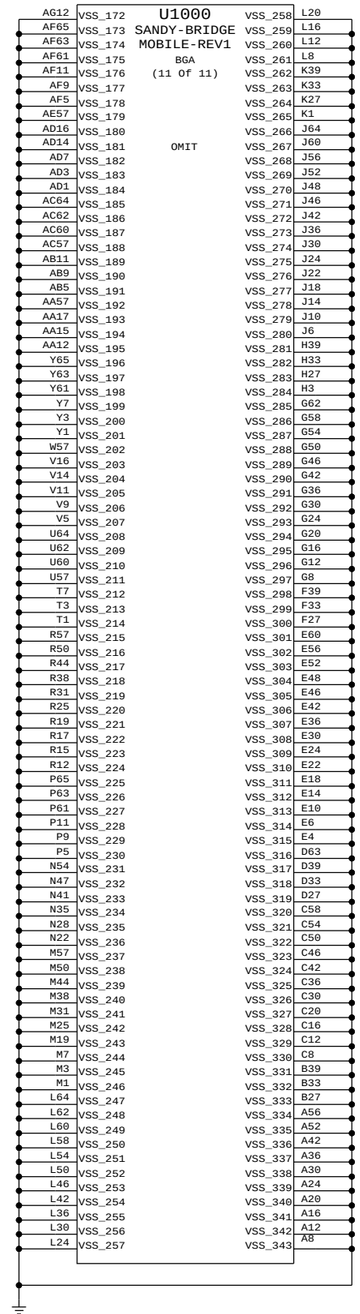
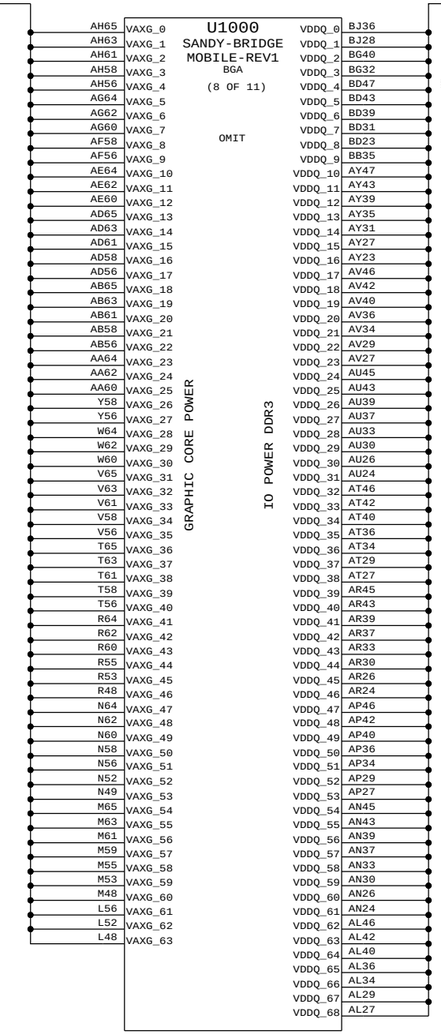


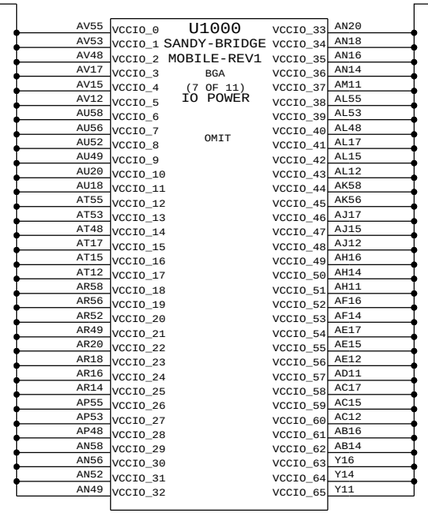


PPVCORE_S0_AXG (69 49 15 12 7)



PP1V5_S3RS0_CPUDDR (7 10 15 29 73 104)

PP1V05_S0 (39 23 14 13 12 10 9 8 106 104 102 73 70 68 45 39)



PP1V05_S0 (7 9 10 12 13 14 23 35 39 45 66 70 73 102 104 105)

PP1V05_S0 (39 23 14 13 12 10 9 8 106 104 102 73 70 68 45 39)

PAGE TITLE
CPU POWER AND GND

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

105 69 49 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 20% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5R CERM 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3
22UF 20% 6.3V X5R CERM 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CRITICAL C1640 C1641 C1642 C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NOSTUFF C1643
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

13 73 70 68 45 39 35 22 105 104 102 PP1V05_S0

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 20% 10V X5R 402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 20% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603
CRITICAL

Place near inductors on bottom side

C1682 C1683
330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W MF 0603

PP1V05_S0_CPU_VCCPQE 7 10 12

C1684
1UF 10% 10V X5R 402

CPU VCCPLL DECOUPLING

102 88 72 71 25 20 7 6 PP1V8_S0

R1600
0
5% 1/16W MF-LF 402

PP1V8_S0_CPU_VCCPLL_R 7 12

C1685
1UF 10% 10V X5R 402
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C1686
1UF 10% 10V X5R 402
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CRITICAL C1687
330UF-0.006OHM 20% 2V POLY CASE-D2-SM
PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

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CPU DECOUPLING-I

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VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

69 49 13 12 7 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 C1709 C1710 C1711 C1712 C1713 C1714 C1715 C1716 C1717
1UF 10% 10V X5R 402 (NOSTUFF on C1709–C1717)

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 C1719 C1720 C1721 C1722 C1723 C1724 C1725
10UF 20% 6.3V CERM-X5R 0402-1 (NOSTUFF on C1724, C1725)

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 C1727 C1728 C1729 C1730 C1731 C1732 C1733
22UF 20% 6.3V X5R-CERM1 0603 (NOSTUFF on C1732, C1733)

PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.

C1734 C1735 C1737
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM (NOSTUFF on C1737)

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

104 73 29 13 10 7 PP1V5_S3RS0_CPUDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747
1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 C1749 C1750 C1751 C1752 C1753 C1754 C1755
10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL
C1756
330UF-0.0060HM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700
0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757
1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

65 12 7 PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 C1759 C1760 C1761 C1762
1UF 10% 10V X5R 402

C1763 C1764 C1765 C1766 C1767
10UF 20% 6.3V X5R 603

C1768
270UF 20% 2V TANT CASE-B4-SM

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

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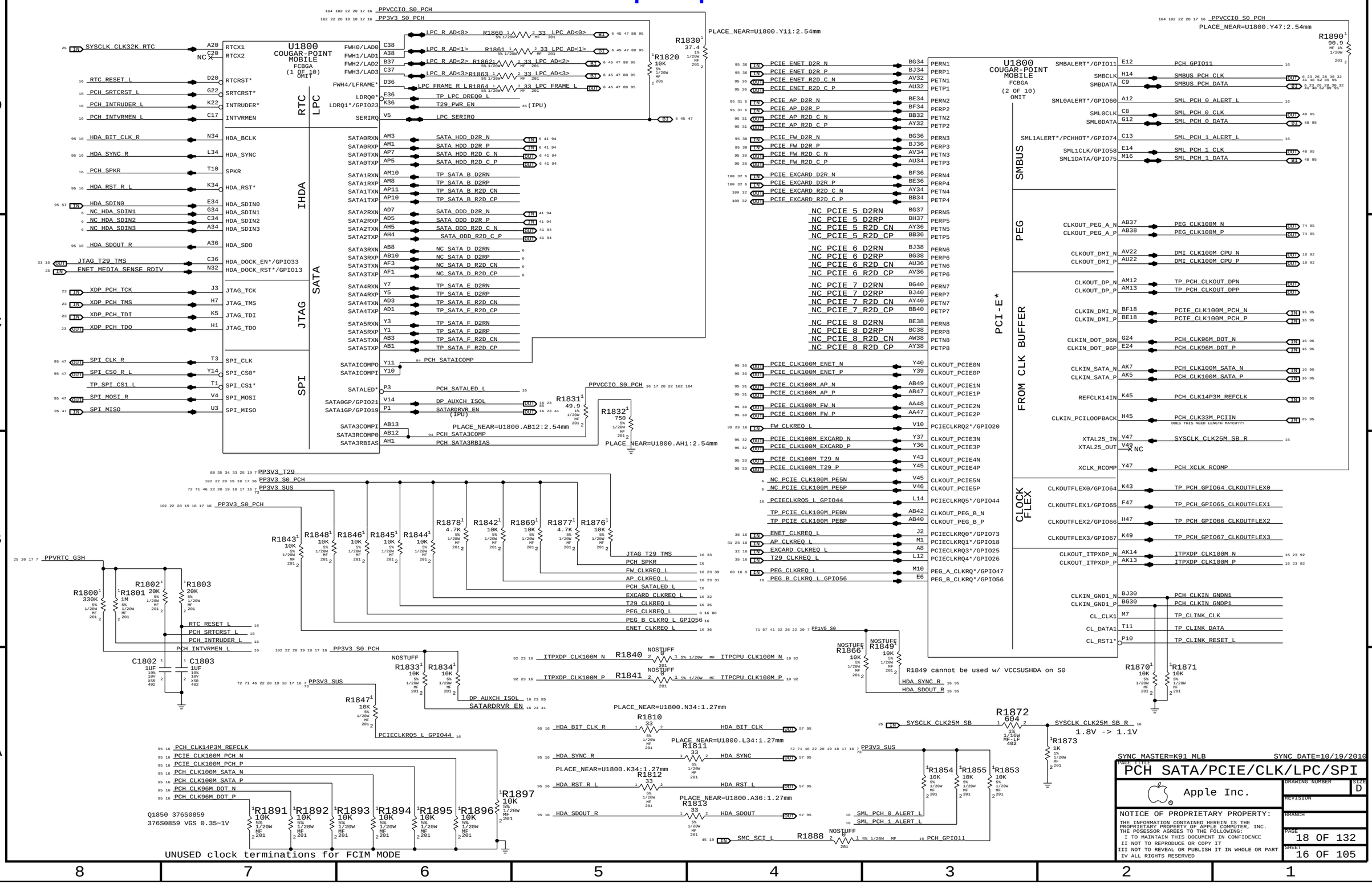

PP3V3_SUS
PPVCCIO_S0_PCH
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201 PLACE_NEAR=U1800.BJ24:12.7mm

U1800 COUGAR-POINT MOBILE FCBGA (3 OF 10) OMIT

DMI / FDI

DMI_N2S_N<0>	BC24	DMI0RXN	
DMI_N2S_N<1>	BE20	DMI1RXN	
DMI_N2S_N<2>	BG18	DMI2RXN	
DMI_N2S_N<3>	BG20	DMI3RXN	
DMI_N2S_P<0>	BE24	DMI0RXP	
DMI_N2S_P<1>	BC20	DMI1RXP	
DMI_N2S_P<2>	BJ18	DMI2RXP	
DMI_N2S_P<3>	BJ20	DMI3RXP	
DMI_S2N_N<0>	AW24	DMI0TXN	
DMI_S2N_N<1>	AW20	DMI1TXN	
DMI_S2N_N<2>	BB18	DMI2TXN	
DMI_S2N_N<3>	AV18	DMI3TXN	
DMI_S2N_P<0>	AY24	DMI0TXP	
DMI_S2N_P<1>	AY20	DMI1TXP	
DMI_S2N_P<2>	AY18	DMI2TXP	
DMI_S2N_P<3>	AU18	DMI3TXP	
PCH_DMI2RBIAS	BH21	DMI2RBIAS	
PCH_DMI_COMP	BJ24	DMI_ZCOMP	
	BG25	DMI_IRCOMP	

R1920 750 1% 1/20W MF 201 PLACE_NEAR=U1800.BH21:2.54mm

FDI_RXN0	BJ14	FDI_DATA_N<0>	9 92
FDI_RXN1	AY14	FDI_DATA_N<1>	9 92
FDI_RXN2	BE14	FDI_DATA_N<2>	9 92
FDI_RXN3	BH13	FDI_DATA_N<3>	9 92
FDI_RXN4	BC12	FDI_DATA_N<4>	9 92
FDI_RXN5	BJ12	FDI_DATA_N<5>	9 92
FDI_RXN6	BG10	FDI_DATA_N<6>	9 92
FDI_RXN7	BG9	FDI_DATA_N<7>	9 92
FDI_RXP0	BG14	FDI_DATA_P<0>	9 92
FDI_RXP1	BB14	FDI_DATA_P<1>	9 92
FDI_RXP2	BF14	FDI_DATA_P<2>	9 92
FDI_RXP3	BG13	FDI_DATA_P<3>	9 92
FDI_RXP4	BE12	FDI_DATA_P<4>	9 92
FDI_RXP5	BG12	FDI_DATA_P<5>	9 92
FDI_RXP6	BJ10	FDI_DATA_P<6>	9 92
FDI_RXP7	BH9	FDI_DATA_P<7>	9 92
FDI_INT	AW16	FDI_INT	OUT 9 92
FDI_FSYNC0	AV12	FDI_FSYNC<0>	OUT 9 92
FDI_FSYNC1	BC10	FDI_FSYNC<1>	OUT 9 92
FDI_LSYNC0	AV14	FDI_LSYNC<0>	OUT 9 92
FDI_LSYNC1	BB10	FDI_LSYNC<1>	OUT 9 92

SYSTEM POWER MANAGEMENT

PM_SYSRST_L	K3	SYS_RESET*	
PM_PCH_SYS_PWROK	P12	SYS_PWROK	
PM_PCH_PWROK	L22	PWROK	
PM_MEM_PWRGD	B13	DRAMPWROK	
PM_DSW_PWRGD	E22	DPWROK	
PM_PCH_PWROK	L10	APWROK	
PM_RSMRST_L	C21	RSMRST*	
SUSWARN_L	K16	SUSWARN*/SUSPWRDNACK/GPIO30	
PM_PWRBTN_L	E20	PWRBTN*	
SMC_ADAPTER_EN	H20	ACPRESENT/GPIO31	
PM_BATLOW_L	E10	BATLOW*/GPIO72	
PCH_RI_L	A10	RI*	
		WAKE*	B9 PCIE_WAKE_L IN 6 17 25 31 32 85
		CLKRUN*/GPIO32	N3 PM_CLKRUN_L BI 6 17 45 47
		SUS_STAT*/GPIO61	G8 LPC_PWRDWN_L OUT 6 45 47
		SUSCLK/GPIO62	N14 PM_CLK32K_SUSCLK_R OUT 46
		SLP_S5*/GPIO63	D10 PM_SLP_S5_L OUT 17 45 73
		SLP_S4*	H4 PM_SLP_S4_L OUT 17 29 42 45 66 73
		SLP_S3*	F4 PM_SLP_S3_L OUT 6 17 29 45 73
		SLP_A*	G10 TP_PM_SLP_A_L
		TP23	AY16 TP_PCH_TP23
		PMSYNCH	AP14 PM_SYNC OUT 10 92
		SLP_LAN*/GPIO29	K14 GPIO29_SLP_LAN_L 17
		DF_TVS	AY1 PCH_DF_TVS
		DSWVRMEN	A18 PCH_DSWVRMEN
		SLP_SUS*	G16 PM_SLP_SUS_L OUT 17 73
		SUSACK*	C12 PCH_SUSACK_L IN 17

PD on SMC page

R1909 100K 5% 1/20W MF 201

DF_TVS:DMI & FDI Term Voltage
Set to Vss when low
Set to Vcc when high

PPVRTC_G3H
R1981 2.2K 5% 1/20W MF 201
PP1V8_S0_PCH
R1980 1K 1% 1/20W MF 201
R1915 390K 5% 1/20W MF 201
CPU_PROC_SEL_L 10 92

R1951 1K 5% 1/20W MF 201 PLACE_NEAR=U1800.T43:2.54mm

R1986 0 5% 1/20W MF
SUSWARN_L 17 — PCH_SUSACK_L 17

U1800 COUGAR-POINT MOBILE FCBGA (4 OF 10) OMIT

DIGITAL DISPLAY INTERFACE

NC	AT1	RSVD	
NC	AT3	RSVD	
NC	AT4	RSVD	
NC	AT5	RSVD	
NC	AT8	RSVD	
NC	AT10	RSVD	
NC	AT12	RSVD	
NC	AU2	RSVD	
NC	AU3	RSVD	
NC	AV1	RSVD	
NC	AV3	RSVD	
NC	AV5	RSVD	
NC	AV7	RSVD	
NC	AV10	RSVD	
NC	AY3	RSVD	
NC	AY5	RSVD	
NC	AY7	RSVD	
NC	BA2	RSVD	
NC	BA3	RSVD	
NC	BB1	RSVD	
NC	BB3	RSVD	
NC	BB5	RSVD	
NC	BB7	RSVD	
NC	BC8	RSVD	
NC	BD4	RSVD	
NC	BE8	RSVD	
NC	BF3	RSVD	
NC	BF6	RSVD	
NC	BG4	RSVD	

CRT

NC_CRT_IG_BLUE	N48	CRT_BLUE	
NC_CRT_IG_GREEN	P49	CRT_GREEN	
NC_CRT_IG_RED	T49	CRT_RED	
NC_CRT_IG_DDC_CLK	T39	CRT_DDC_CLK	
NC_CRT_IG_DDC_DATA	M40	CRT_DDC_DATA	
NC_CRT_IG_HSYNC	M47	CRT_HSYNC	
NC_CRT_IG_VSYNC	M49	CRT_VSYNC	
PCH_DAC_IREF	T43	DAC_IREF	
	T42	CRT_IRTN	

SDVO_TVCLKINN	AP43	NC_SDVO_TVCLKINN	6
SDVO_TVCLKINP	AP45	NC_SDVO_TVCLKINP	6
SDVO_STALLN	AM42	NC_SDVO_STALLN	6
SDVO_STALLP	AM40	NC_SDVO_STALLP	6
SDVO_INTN	AP39	NC_SDVO_INTN	6
SDVO_INTP	AP40	NC_SDVO_INTP	6
SDVO_CTRLCLK	P38	DP_IG_DDC_CLK	8 80 84
SDVO_CTRLDATA	M39	DP_IG_DDC_DATA	8 80 84
DDPB_AUXN	AT49	DP_IG_AUX_CH_N	8 84 94
DDPB_AUXP	AT47	DP_IG_AUX_CH_P	8 84 94
DDPB_HPD	AT40	DP_IG_HPD	8 84
DDPB_0N	AV42	TP_DP_IG_B_MLN<0>	
DDPB_0P	AV40	TP_DP_IG_B_MLP<0>	
DDPB_1N	AV45	TP_DP_IG_B_MLN<1>	
DDPB_1P	AV46	TP_DP_IG_B_MLP<1>	
DDPB_2N	AU48	TP_DP_IG_B_MLN<2>	
DDPB_2P	AU47	TP_DP_IG_B_MLP<2>	
DDPB_3N	AV47	TP_DP_IG_B_MLN<3>	
DDPB_3P	AV49	TP_DP_IG_B_MLP<3>	
DDPC_CTRLCLK	P46	NC_DP_IG_C_CTRL_CLK	6
DDPC_CTRLDATA	P42	NC_DP_IG_C_CTRL_DATA	6
DDPC_AUXN	AP47	NC_DP_IG_C_AUXN	6
DDPC_AUXP	AP49	NC_DP_IG_C_AUXP	6
DDPC_HPD	AT38	NC_DP_IG_C_HPD	6
DDPC_0N	AY47	NC_DP_IG_C_MLN<0>	6
DDPC_0P	AY49	NC_DP_IG_C_MLP<0>	6
DDPC_1N	AY43	NC_DP_IG_C_MLN<1>	6
DDPC_1P	AY45	NC_DP_IG_C_MLP<1>	6
DDPC_2N	BA47	NC_DP_IG_C_MLN<2>	6
DDPC_2P	BA48	NC_DP_IG_C_MLP<2>	6
DDPC_3N	BB47	NC_DP_IG_C_MLN<3>	6
DDPC_3P	BB49	NC_DP_IG_C_MLP<3>	6
DDPD_CTRLCLK	M43	NC_DP_IG_D_CTRL_CLK	6
DDPD_CTRLDATA	M36	NC_DP_IG_D_CTRL_DATA	6
DDPD_AUXN	AT45	NC_DP_IG_D_AUXN	6
DDPD_AUXP	AT43	NC_DP_IG_D_AUXP	6
DDPD_HPD	BH41	NC_DP_IG_D_HPD	6
DDPD_0N	BB43	NC_DP_IG_D_MLN<0>	6
DDPD_0P	BB45	NC_DP_IG_D_MLP<0>	6
DDPD_1N	BF44	NC_DP_IG_D_MLN<1>	6
DDPD_1P	BE44	NC_DP_IG_D_MLP<1>	6
DDPD_2N	BF42	NC_DP_IG_D_MLN<2>	6
DDPD_2P	BE42	NC_DP_IG_D_MLP<2>	6
DDPD_3N	BJ42	NC_DP_IG_D_MLN<3>	6
DDPD_3P	BG42	NC_DP_IG_D_MLP<3>	6

T29 WAKE
PCIE_WAKE_L (IN) — PCIE_WAKE_L (OUT) 6 17 25 31 32 85
MAKE_BASE=TRUE

PP3V3_SUS
PP3V3_S5
PP3V3_SUS
R1925 1K 1% 1/20W MF 201
R1985 1K 1% 1/20W MF 201
R1982 10K 5% 1/20W MF 201
R1983 10K 5% 1/20W MF 201
SUSWARN_L 17
GPIO29_SLP_LAN_L 17
PM_PWRBTN_L 17 23 45
PCIE_WAKE_L 6 17 25 31 32 85

PP3V3_S0_PCH
R1991 8.2K 5% 1/20W MF 201
PM_CLKRUN_L 6 17 45 47

PM_SLP_S3_L
PM_SLP_SUS_L
PM_SLP_S5_L
PM_SLP_S4_L
R1921 100K 5% 1/20W MF 201
R1922 100K 5% 1/20W MF 201
R1923 100K 5% 1/20W MF 201
R1924 100K 5% 1/20W MF 201

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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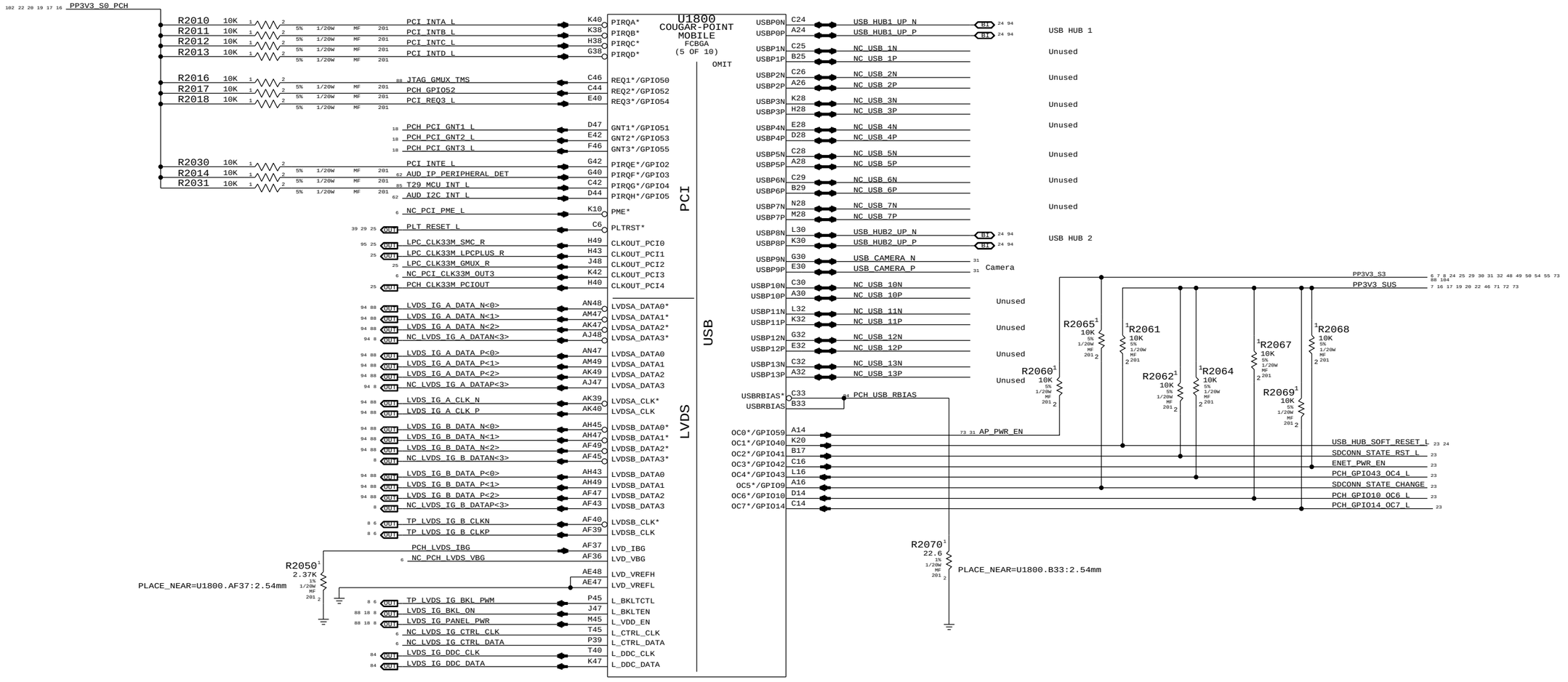

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PCH PCI/FLASHCACHE/USB

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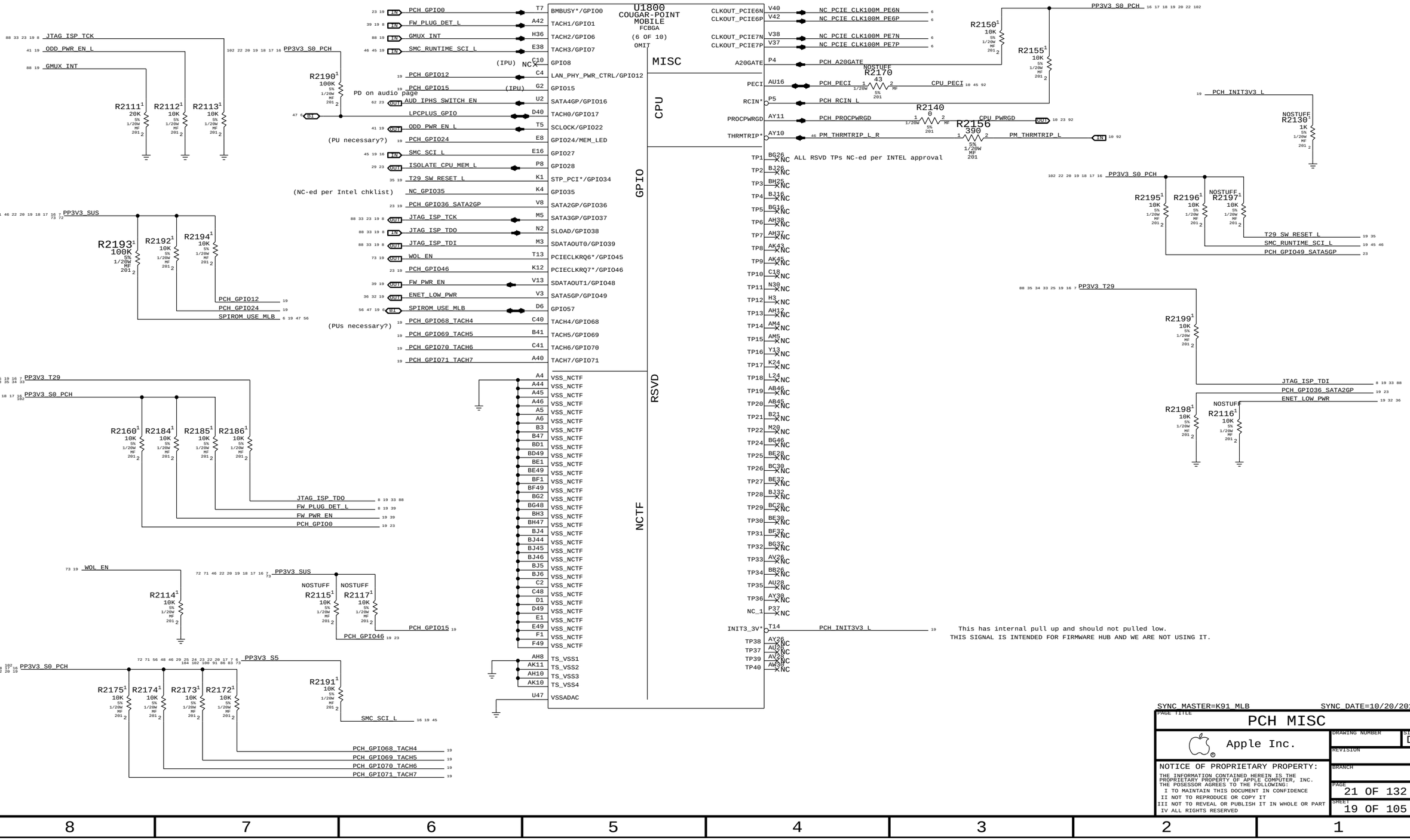

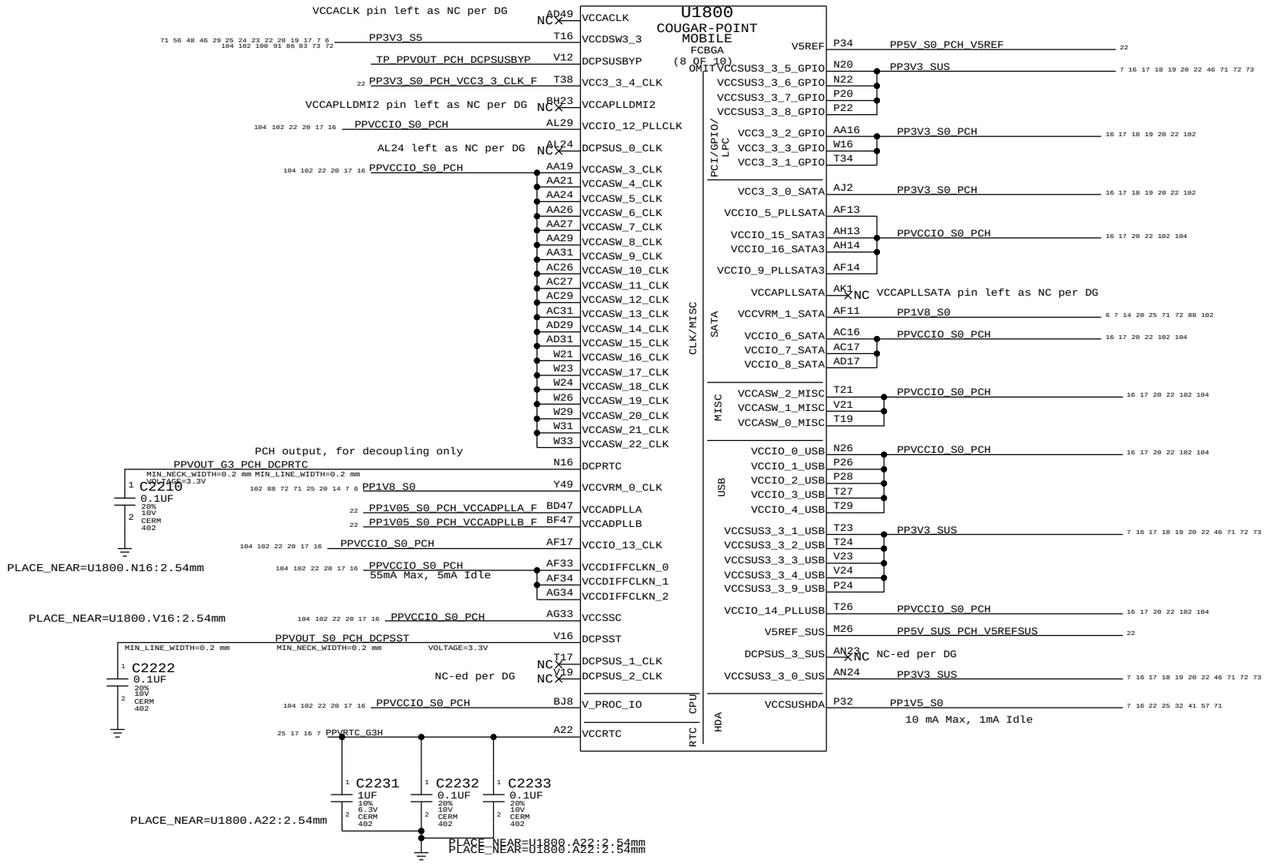

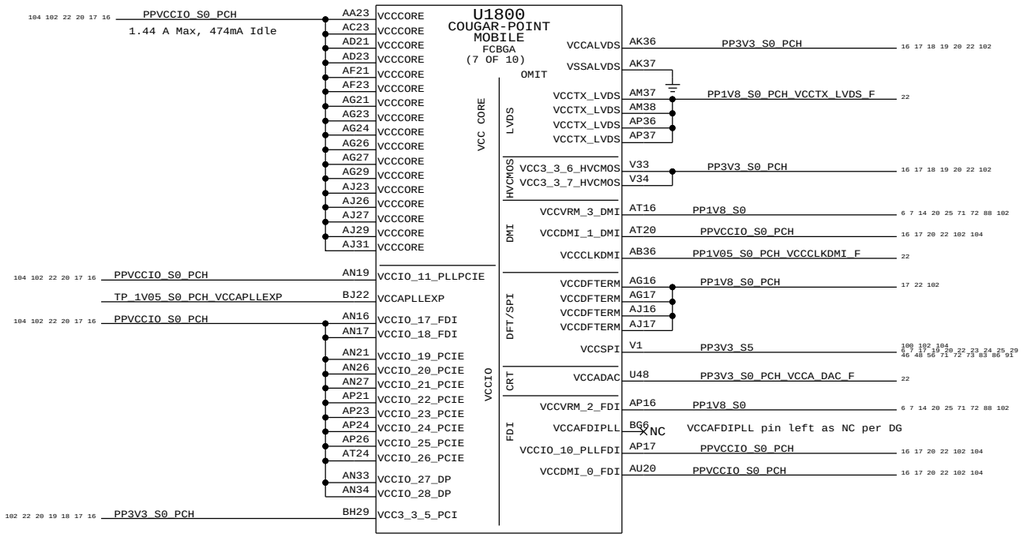

PAGE TITLE	PCH POWER
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
	BRANCH:
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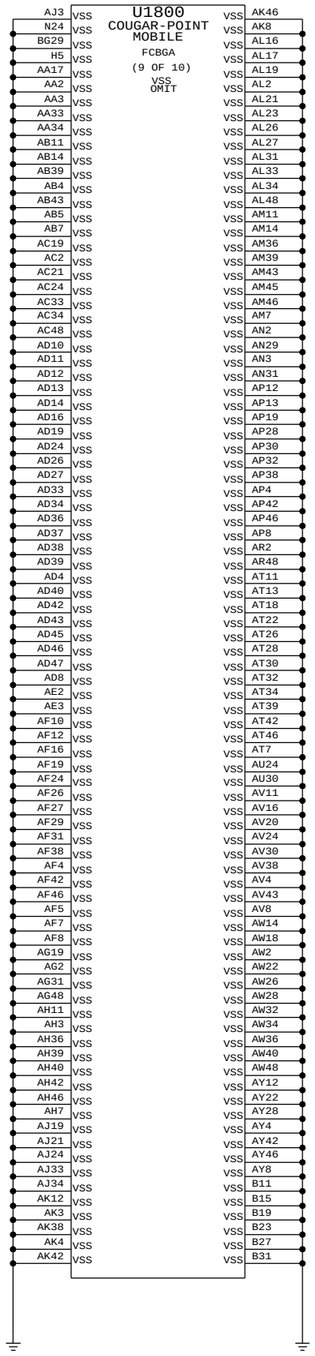
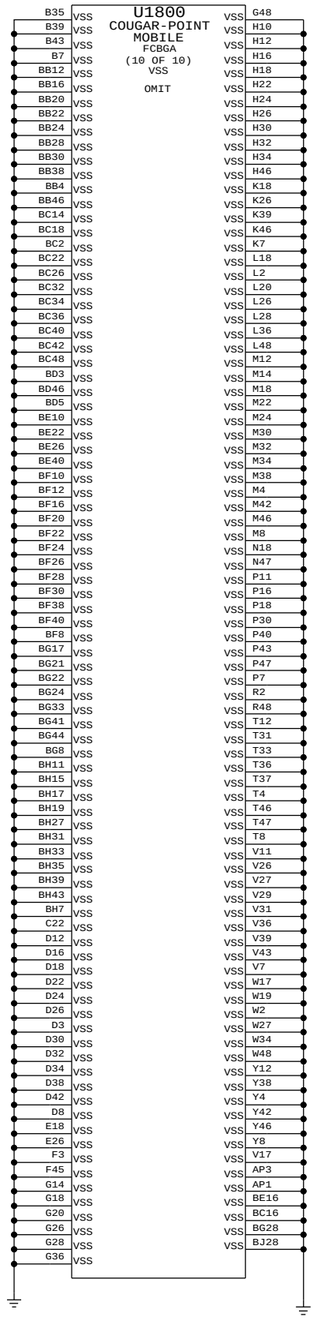
	SHEET: 20 OF 105





SYNC_MASTER=K92_YUN SYNC_DATE=05/20/2010

PAGE TITLE

PCH GROUNDS

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

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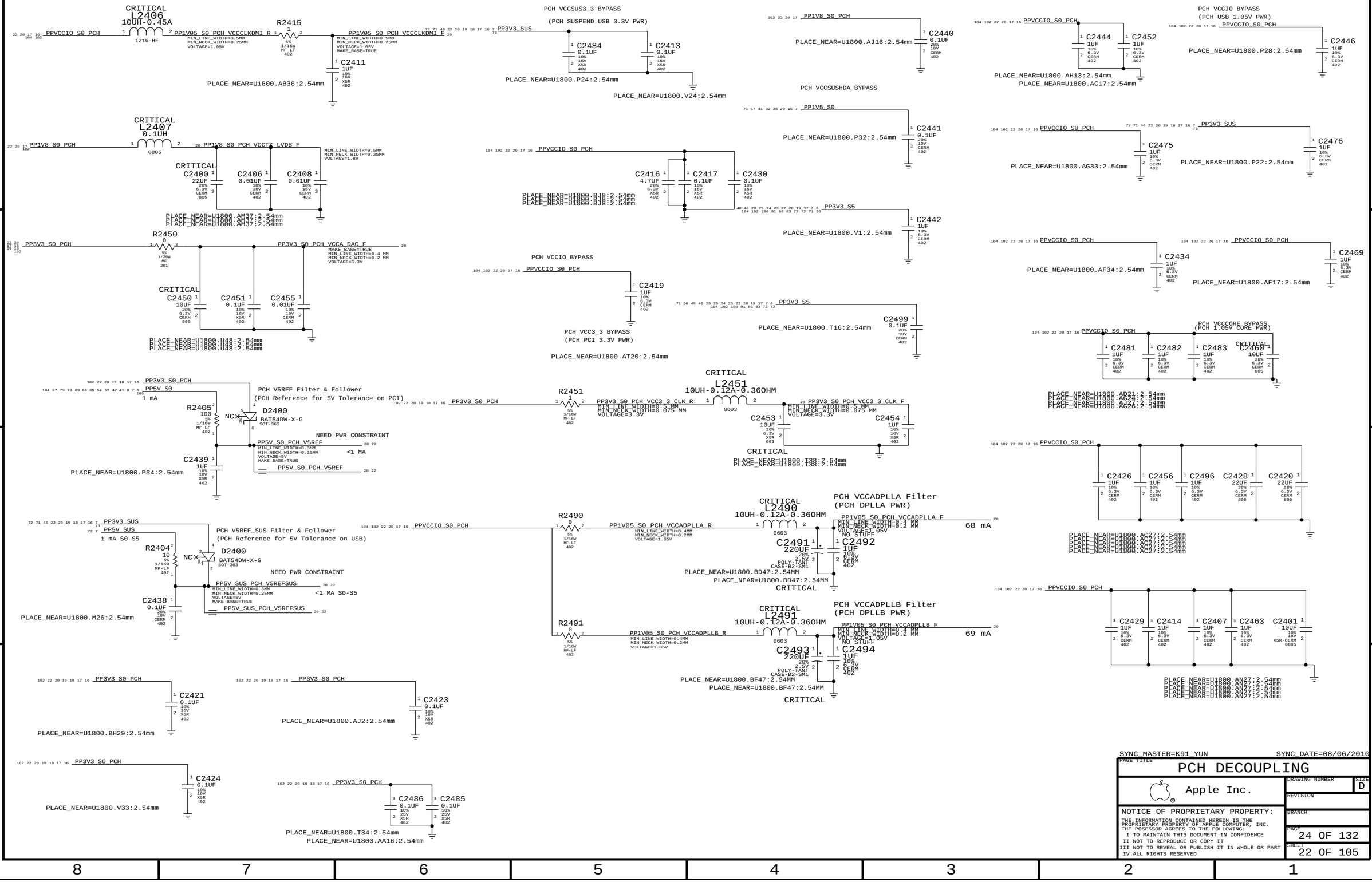

SYNC_MASTER=K91_YUN SYNC_DATE=08/06/2010

PAGE TITLE

PCH DECOUPLING

Apple Inc.

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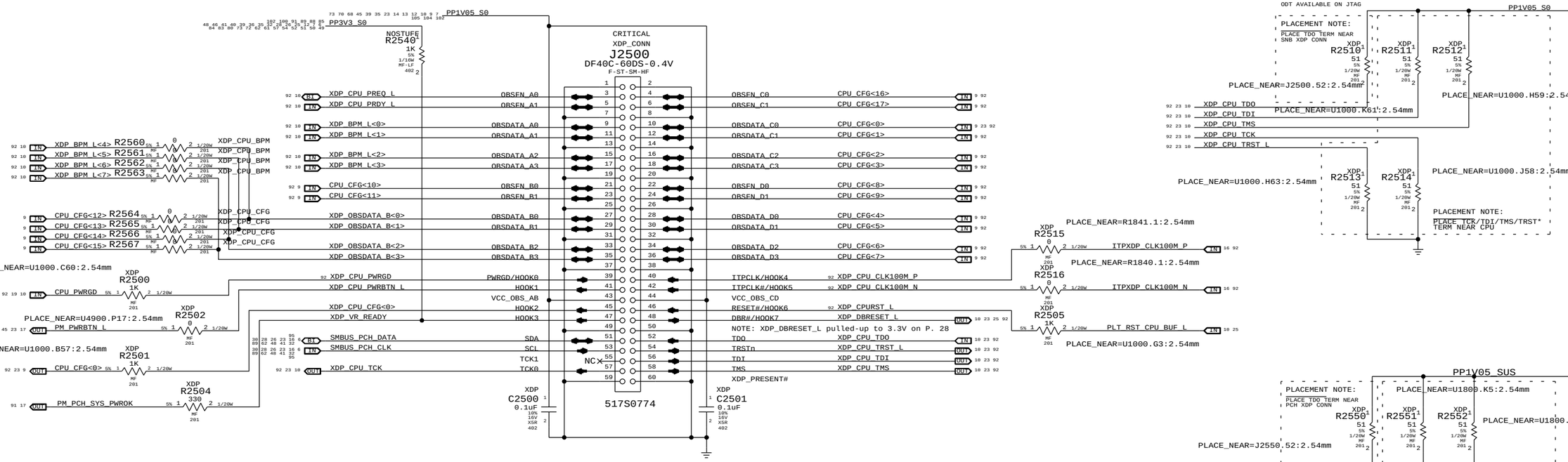
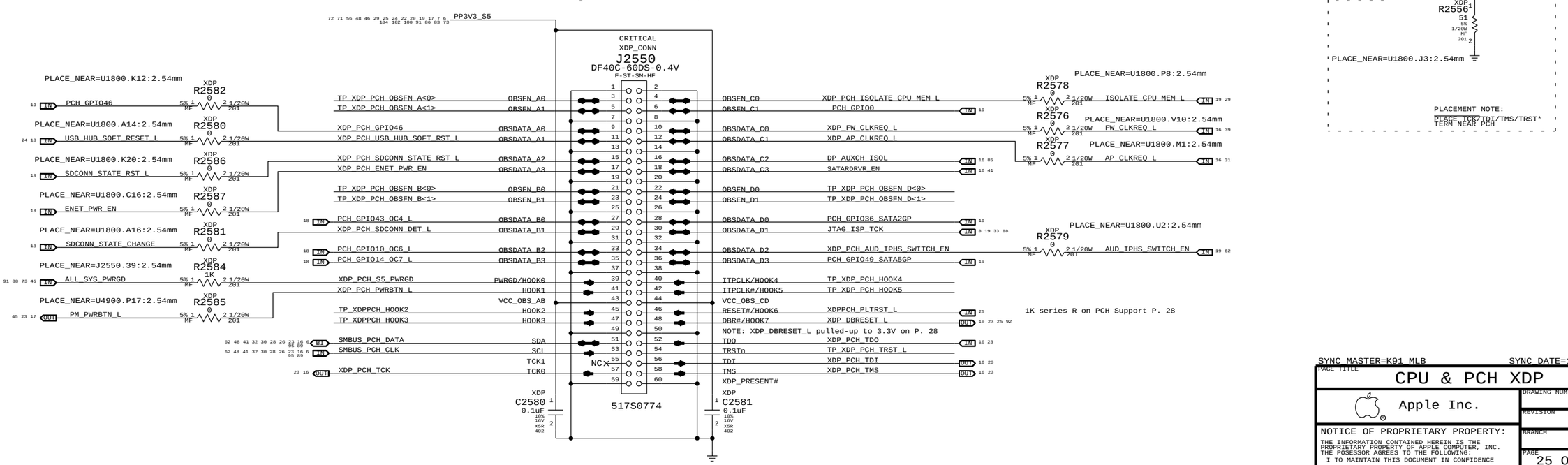
PROCESSOR MINI XDP



PCH MINI XDP



SYNC_MASTER=K91_MLB SYNC_DATE=10/17/2010

PAGE TITLE: CPU & PCH XDP

Apple Inc.

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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061

T29 unused USB port, only has pull up

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

External A

SD Card/Express Card

SYNC MASTER=K92_BEN SYNC DATE=06/29/2010

PAGE TITLE: USB HUBS

Apple Inc.

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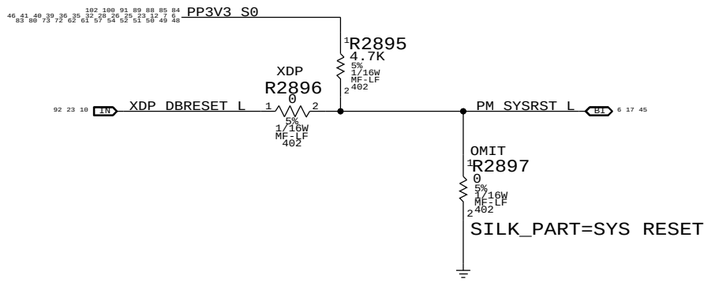
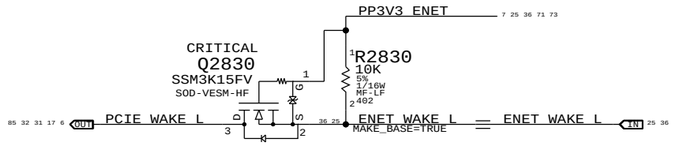
PCH Reset Button

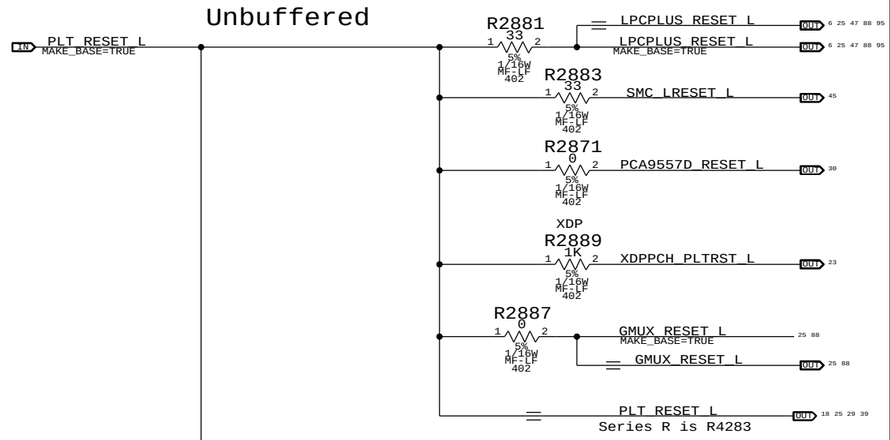


Ethernet WAKE# Isolation

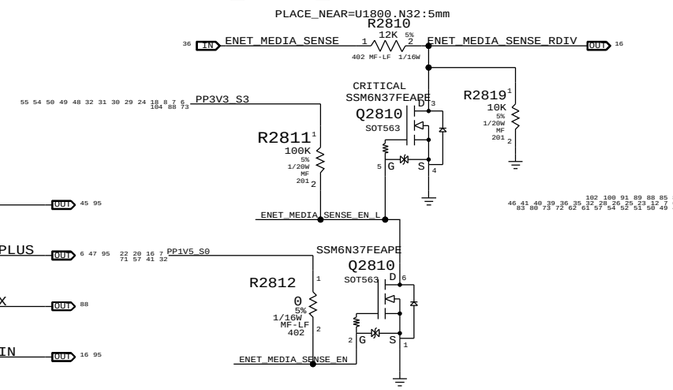


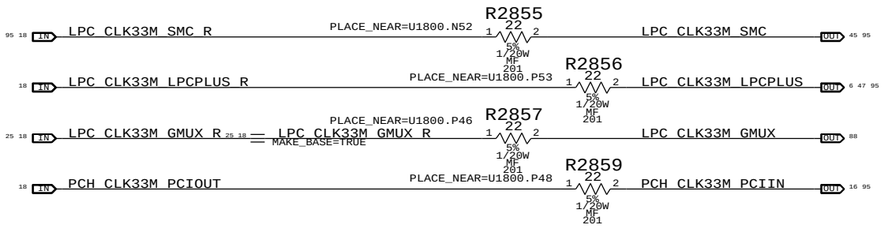
Platform Reset Connections

Unbuffered



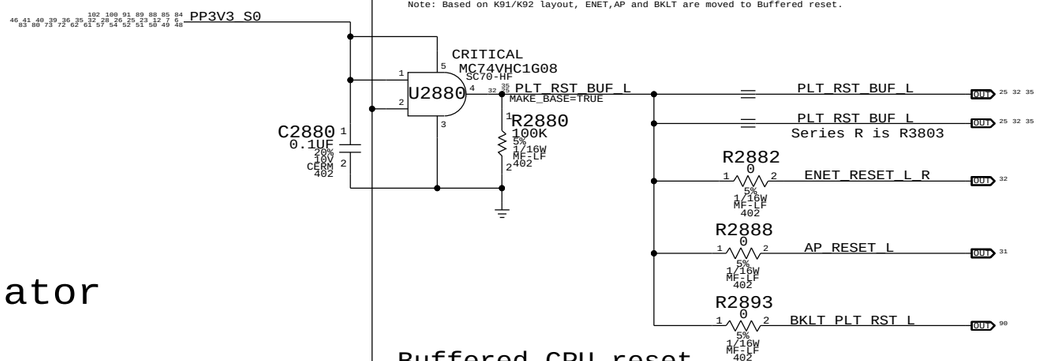
ENET_MEDIA_SENSE ISOLATION CIRCUIT





Buffered

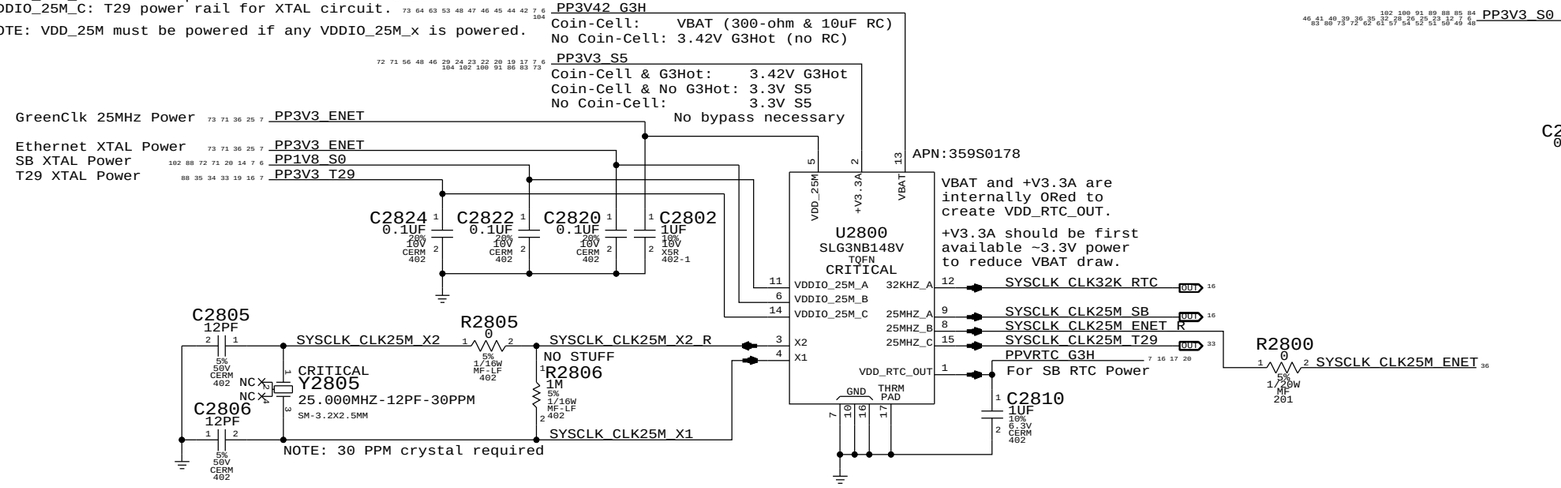
Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.



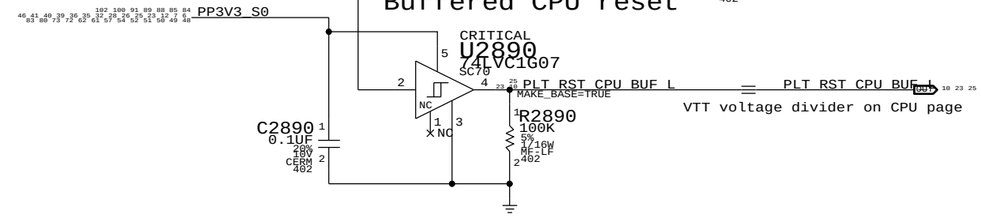
System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



Buffered CPU reset



SYNC_MASTER=K91_MLB	SYNC_DATE=06/29/2010
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER / SIZE D
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_A_VTT_A
- =PP5PD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2900 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm
C2901 10UF 20% 6.3V X6S 603 — PLACE_NEAR=J2900.75:2.54mm

C2910 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2911 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2912 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2913 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2914 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2915 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2916 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2917 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2918 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2919 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2920 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2921 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2922 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm
C2923 0.1UF 20% 10V CERM 402 — PLACE_NEAR=J2900.75:2.54mm

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 F-RT-THB — DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2)

		KEY			
		CKE0	73	CKE1	
	NC	VDD	75	VDD	
NC		NC	77	A15	MEM_A_A<15>
	MEM_A_BA<2>	BA2	79	A14	MEM_A_A<14>
		VDD	81	VDD	
	MEM_A_A<12>	A12/BC*	83	A11	MEM_A_A<11>
	MEM_A_A<9>	A9	85	A7	MEM_A_A<7>
		VDD	87	VDD	
	MEM_A_A<8>	A8	89	A6	MEM_A_A<6>
	MEM_A_A<5>	A5	91	A4	MEM_A_A<4>
		VDD	93	VDD	
	MEM_A_A<3>	A3	95	A2	MEM_A_A<2>
	MEM_A_A<1>	A1	97	A0	MEM_A_A<0>
		VDD	99	VDD	
	MEM_A_CLK_P<0>	CK0	101	CK1	MEM_A_CLK_P<1>
	MEM_A_CLK_N<0>	CK0*	103	CK1*	MEM_A_CLK_N<1>
		VDD	105	VDD	
	MEM_A_A<10>	A10/AP	107	BA1	MEM_A_BA<1>
	MEM_A_BA<0>	BA0	109	RAS*	MEM_A_RAS_L
		VDD	111	VDD	
	MEM_A_WE_L	WE*	113	S0*	MEM_A_CS_L<0>
	MEM_A_CAS_L	CAS*	115	ODT0	MEM_A_ODT<0>
		VDD	117	VDD	
	MEM_A_A<13>	A13	119	ODT1	MEM_A_ODT<1>
	MEM_A_CS_L<1>	S1*	121	NC	NC
		VDD	123	VDD	
NC		TEST	125	VREFCA	
		VSS	127	VSS	
	=MEM_A_DQ<32>	DQ32	129	DQ36	=MEM_A_DQ<36>
	=MEM_A_DQ<33>	DQ33	131	DQ37	MEM_A_DQ<37>
		VSS	133	VSS	
	=MEM_A_DQS_N<4>	DQS4*	135	DM4	
	=MEM_A_DQS_P<4>	DQS4	137	VSS	
		VSS	139	DQ38	=MEM_A_DQ<38>
	=MEM_A_DQ<34>	DQ34	141	DQ39	=MEM_A_DQ<39>
	=MEM_A_DQ<35>	DQ35	143	VSS	
		VSS	145	DQ44	=MEM_A_DQ<44>
	=MEM_A_DQ<40>	DQ40	147	DQ45	=MEM_A_DQ<45>
	=MEM_A_DQ<41>	DQ41	149	VSS	
		VSS	151	DQS5*	=MEM_A_DQS_N<5>
		DM5	153	DQS5	=MEM_A_DQS_P<5>
		VSS	155	VSS	
	=MEM_A_DQ<42>	DQ42	157	DQ46	=MEM_A_DQ<46>
	=MEM_A_DQ<43>	DQ43	159	DQ47	=MEM_A_DQ<47>
		VSS	161	VSS	
	=MEM_A_DQ<48>	DQ48	163	DQ52	=MEM_A_DQ<52>
	=MEM_A_DQ<49>	DQ49	165	DQ53	=MEM_A_DQ<53>
		VSS	167	VSS	
	=MEM_A_DQS_N<6>	DQS6*	169	DM6	
	=MEM_A_DQS_P<6>	DQS6	171	VSS	
		VSS	173	DQ54	=MEM_A_DQ<54>
	=MEM_A_DQ<50>	DQ50	175	DQ55	=MEM_A_DQ<55>
	=MEM_A_DQ<51>	DQ51	177	VSS	
		VSS	179	DQ60	=MEM_A_DQ<60>
	=MEM_A_DQ<56>	DQ56	181	DQ61	=MEM_A_DQ<61>
	=MEM_A_DQ<57>	DQ57	183	VSS	
		VSS	185	DQS7*	=MEM_A_DQS_N<7>
		DM7	187	DQS7	=MEM_A_DQS_P<7>
		VSS	189	VSS	
	=MEM_A_DQ<58>	DQ58	191	DQ62	=MEM_A_DQ<62>
	=MEM_A_DQ<59>	DQ59	193	DQ63	=MEM_A_DQ<63>
		VSS	195	VSS	
	MEM_A_SA<0>	SA0	197	EVENT*	MEM_EVENT_L
		VDDSPD	199	SDA	SMBUS_PCH_DATA
	MEM_A_SA<1>	SA1	201	SCL	SMBUS_PCH_CLK
		VTT	203	VTT	
					KEY

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

J2900 F-RT-THB — DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) — CRITICAL

		KEY			
		VREFDQ	1	VSS	
	=MEM_A_DQ<0>	VSS	3	DQ4	=MEM_A_DQ<4>
	=MEM_A_DQ<1>	DQ0	5	DQ5	=MEM_A_DQ<5>
		DQ1	7	VSS	
		VSS	9	DQS0*	MEM_A_DQS_N<0>
		DM0	11	DQS0	=MEM_A_DQS_P<0>
		VSS	13	VSS	
	=MEM_A_DQ<2>	DQ2	15	DQ6	=MEM_A_DQ<6>
	=MEM_A_DQ<3>	DQ3	17	DQ7	=MEM_A_DQ<7>
		VSS	19	VSS	
	=MEM_A_DQ<8>	DQ8	21	DQ12	=MEM_A_DQ<12>
	=MEM_A_DQ<9>	DQ9	23	DQ13	=MEM_A_DQ<13>
		VSS	25	VSS	
	=MEM_A_DQS_N<1>	DQS1*	27	DM1	
	=MEM_A_DQS_P<1>	DQS1	29	RESET*	MEM_RESET_L
		VSS	31	VSS	
	=MEM_A_DQ<10>	DQ10	33	DQ14	=MEM_A_DQ<14>
	=MEM_A_DQ<11>	DQ11	35	DQ15	=MEM_A_DQ<15>
		VSS	37	VSS	
	=MEM_A_DQ<16>	DQ16	39	DQ20	=MEM_A_DQ<20>
	=MEM_A_DQ<17>	DQ17	41	DQ21	=MEM_A_DQ<21>
		VSS	43	VSS	
	=MEM_A_DQS_N<2>	DQS2*	45	DM2	
	=MEM_A_DQS_P<2>	DQS2	47	VSS	
		VSS	49	DQ22	=MEM_A_DQ<22>
	=MEM_A_DQ<18>	DQ18	51	DQ23	=MEM_A_DQ<23>
	=MEM_A_DQ<19>	DQ19	53	VSS	
		VSS	55	DQ28	=MEM_A_DQ<28>
	=MEM_A_DQ<24>	DQ24	57	DQ29	=MEM_A_DQ<29>
	=MEM_A_DQ<25>	DQ25	59	VSS	
		VSS	61	DQS3*	=MEM_A_DQS_N<3>
		DM3	63	DQS3	=MEM_A_DQS_P<3>
		VSS	65	VSS	
	=MEM_A_DQ<26>	DQ26	67	DQ30	=MEM_A_DQ<30>
	=MEM_A_DQ<27>	DQ27	69	DQ31	=MEM_A_DQ<31>
		VSS	71	VSS	
					KEY

516-0229

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

PP3V3_S0

R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

C2940 2.2UF 20% 6.3V CERM 402-LF

PP0V75_S0_DDRVTT

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

"Factory" (top) slot

SYNC_MASTER=K92_YUN SYNC_DATE=06/14/2010

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

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BRANCH:
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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

93 27 26 11 MEM_A_DQS_N<0> MAKE_BASE=TRUE =MEM_A_DQS_N<0> 11 26 27 93 93 28 11
93 11 MEM_A_DQS_P<0> MAKE_BASE=TRUE =MEM_A_DQS_P<0> 26

93 11 MEM_A_DQ<7> MAKE_BASE=TRUE =MEM_A_DQ<7> 26
93 11 MEM_A_DQ<6> MAKE_BASE=TRUE =MEM_A_DQ<6> 26
93 11 MEM_A_DQ<5> MAKE_BASE=TRUE =MEM_A_DQ<5> 26
93 11 MEM_A_DQ<4> MAKE_BASE=TRUE =MEM_A_DQ<4> 26
93 11 MEM_A_DQ<3> MAKE_BASE=TRUE =MEM_A_DQ<3> 26
93 11 MEM_A_DQ<2> MAKE_BASE=TRUE =MEM_A_DQ<2> 26
93 11 MEM_A_DQ<1> MAKE_BASE=TRUE =MEM_A_DQ<1> 26
93 11 MEM_A_DQ<0> MAKE_BASE=TRUE =MEM_A_DQ<0> 26

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

93 11 MEM_A_DQS_N<1> MAKE_BASE=TRUE =MEM_A_DQS_N<1> 26
93 11 MEM_A_DQS_P<1> MAKE_BASE=TRUE =MEM_A_DQS_P<1> 26

93 11 MEM_A_DQ<15> MAKE_BASE=TRUE =MEM_A_DQ<15> 26
93 11 MEM_A_DQ<14> MAKE_BASE=TRUE =MEM_A_DQ<14> 26
93 11 MEM_A_DQ<13> MAKE_BASE=TRUE =MEM_A_DQ<13> 26
93 11 MEM_A_DQ<12> MAKE_BASE=TRUE =MEM_A_DQ<12> 26
93 11 MEM_A_DQ<11> MAKE_BASE=TRUE =MEM_A_DQ<11> 26
93 11 MEM_A_DQ<10> MAKE_BASE=TRUE =MEM_A_DQ<10> 26
93 11 MEM_A_DQ<9> MAKE_BASE=TRUE =MEM_A_DQ<9> 26
93 11 MEM_A_DQ<8> MAKE_BASE=TRUE =MEM_A_DQ<8> 26

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

93 11 MEM_A_DQS_N<2> MAKE_BASE=TRUE =MEM_A_DQS_N<2> 26
93 11 MEM_A_DQS_P<2> MAKE_BASE=TRUE =MEM_A_DQS_P<2> 26

93 11 MEM_A_DQ<23> MAKE_BASE=TRUE =MEM_A_DQ<23> 26
93 11 MEM_A_DQ<22> MAKE_BASE=TRUE =MEM_A_DQ<22> 26
93 11 MEM_A_DQ<21> MAKE_BASE=TRUE =MEM_A_DQ<21> 26
93 11 MEM_A_DQ<20> MAKE_BASE=TRUE =MEM_A_DQ<20> 26
93 11 MEM_A_DQ<19> MAKE_BASE=TRUE =MEM_A_DQ<19> 26
93 11 MEM_A_DQ<18> MAKE_BASE=TRUE =MEM_A_DQ<18> 26
93 11 MEM_A_DQ<17> MAKE_BASE=TRUE =MEM_A_DQ<17> 26
93 11 MEM_A_DQ<16> MAKE_BASE=TRUE =MEM_A_DQ<16> 26

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

93 11 MEM_A_DQS_N<3> MAKE_BASE=TRUE =MEM_A_DQS_N<3> 26
93 11 MEM_A_DQS_P<3> MAKE_BASE=TRUE =MEM_A_DQS_P<3> 26

93 11 MEM_A_DQ<31> MAKE_BASE=TRUE =MEM_A_DQ<31> 26
93 11 MEM_A_DQ<30> MAKE_BASE=TRUE =MEM_A_DQ<30> 26
93 11 MEM_A_DQ<29> MAKE_BASE=TRUE =MEM_A_DQ<29> 26
93 11 MEM_A_DQ<28> MAKE_BASE=TRUE =MEM_A_DQ<28> 26
93 11 MEM_A_DQ<27> MAKE_BASE=TRUE =MEM_A_DQ<27> 26
93 11 MEM_A_DQ<26> MAKE_BASE=TRUE =MEM_A_DQ<26> 26
93 11 MEM_A_DQ<25> MAKE_BASE=TRUE =MEM_A_DQ<25> 26
93 11 MEM_A_DQ<24> MAKE_BASE=TRUE =MEM_A_DQ<24> 26

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

93 11 MEM_A_DQS_N<4> MAKE_BASE=TRUE =MEM_A_DQS_N<4> 26
93 11 MEM_A_DQS_P<4> MAKE_BASE=TRUE =MEM_A_DQS_P<4> 26

93 11 MEM_A_DQ<39> MAKE_BASE=TRUE =MEM_A_DQ<39> 26
93 11 MEM_A_DQ<38> MAKE_BASE=TRUE =MEM_A_DQ<38> 26
93 27 26 11 MEM_A_DQ<37> MAKE_BASE=TRUE =MEM_A_DQ<37> 11 26 27 93 93 28 11
93 11 MEM_A_DQ<36> MAKE_BASE=TRUE =MEM_A_DQ<36> 26
93 11 MEM_A_DQ<35> MAKE_BASE=TRUE =MEM_A_DQ<35> 26
93 11 MEM_A_DQ<34> MAKE_BASE=TRUE =MEM_A_DQ<34> 26
93 11 MEM_A_DQ<33> MAKE_BASE=TRUE =MEM_A_DQ<33> 26
93 11 MEM_A_DQ<32> MAKE_BASE=TRUE =MEM_A_DQ<32> 26

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

93 11 MEM_A_DQS_N<5> MAKE_BASE=TRUE =MEM_A_DQS_N<5> 26
93 11 MEM_A_DQS_P<5> MAKE_BASE=TRUE =MEM_A_DQS_P<5> 26

93 11 MEM_A_DQ<47> MAKE_BASE=TRUE =MEM_A_DQ<47> 26
93 11 MEM_A_DQ<46> MAKE_BASE=TRUE =MEM_A_DQ<46> 26
93 11 MEM_A_DQ<45> MAKE_BASE=TRUE =MEM_A_DQ<45> 26
93 11 MEM_A_DQ<44> MAKE_BASE=TRUE =MEM_A_DQ<44> 26
93 11 MEM_A_DQ<43> MAKE_BASE=TRUE =MEM_A_DQ<43> 26
93 11 MEM_A_DQ<42> MAKE_BASE=TRUE =MEM_A_DQ<42> 26
93 11 MEM_A_DQ<41> MAKE_BASE=TRUE =MEM_A_DQ<41> 26
93 11 MEM_A_DQ<40> MAKE_BASE=TRUE =MEM_A_DQ<40> 26

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

93 11 MEM_A_DQS_N<6> MAKE_BASE=TRUE =MEM_A_DQS_N<6> 26
93 11 MEM_A_DQS_P<6> MAKE_BASE=TRUE =MEM_A_DQS_P<6> 26

93 11 MEM_A_DQ<55> MAKE_BASE=TRUE =MEM_A_DQ<55> 26
93 11 MEM_A_DQ<54> MAKE_BASE=TRUE =MEM_A_DQ<54> 26
93 11 MEM_A_DQ<53> MAKE_BASE=TRUE =MEM_A_DQ<53> 26
93 11 MEM_A_DQ<52> MAKE_BASE=TRUE =MEM_A_DQ<52> 26
93 11 MEM_A_DQ<51> MAKE_BASE=TRUE =MEM_A_DQ<51> 26
93 11 MEM_A_DQ<50> MAKE_BASE=TRUE =MEM_A_DQ<50> 26
93 11 MEM_A_DQ<49> MAKE_BASE=TRUE =MEM_A_DQ<49> 26
93 11 MEM_A_DQ<48> MAKE_BASE=TRUE =MEM_A_DQ<48> 26

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

93 11 MEM_A_DQS_N<7> MAKE_BASE=TRUE =MEM_A_DQS_N<7> 26
93 11 MEM_A_DQS_P<7> MAKE_BASE=TRUE =MEM_A_DQS_P<7> 26

93 11 MEM_A_DQ<63> MAKE_BASE=TRUE =MEM_A_DQ<63> 26
93 11 MEM_A_DQ<62> MAKE_BASE=TRUE =MEM_A_DQ<62> 26
93 11 MEM_A_DQ<61> MAKE_BASE=TRUE =MEM_A_DQ<61> 26
93 11 MEM_A_DQ<60> MAKE_BASE=TRUE =MEM_A_DQ<60> 26
93 11 MEM_A_DQ<59> MAKE_BASE=TRUE =MEM_A_DQ<59> 26
93 11 MEM_A_DQ<58> MAKE_BASE=TRUE =MEM_A_DQ<58> 26
93 11 MEM_A_DQ<57> MAKE_BASE=TRUE =MEM_A_DQ<57> 26
93 11 MEM_A_DQ<56> MAKE_BASE=TRUE =MEM_A_DQ<56> 26

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

93 27 26 11 MEM_B_DQS_N<0> MAKE_BASE=TRUE =MEM_B_DQS_N<0> 11 27 28 93
93 28 27 11 MEM_B_DQS_P<0> MAKE_BASE=TRUE =MEM_B_DQS_P<0> 11 27 28 93

93 11 MEM_B_DQ<7> MAKE_BASE=TRUE =MEM_B_DQ<7> 28
93 11 MEM_B_DQ<6> MAKE_BASE=TRUE =MEM_B_DQ<6> 28
93 11 MEM_B_DQ<5> MAKE_BASE=TRUE =MEM_B_DQ<5> 28
93 11 MEM_B_DQ<4> MAKE_BASE=TRUE =MEM_B_DQ<4> 28
93 11 MEM_B_DQ<3> MAKE_BASE=TRUE =MEM_B_DQ<3> 28
93 11 MEM_B_DQ<2> MAKE_BASE=TRUE =MEM_B_DQ<2> 28
93 11 MEM_B_DQ<1> MAKE_BASE=TRUE =MEM_B_DQ<1> 28
93 11 MEM_B_DQ<0> MAKE_BASE=TRUE =MEM_B_DQ<0> 28

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

93 11 MEM_B_DQS_N<1> MAKE_BASE=TRUE =MEM_B_DQS_N<1> 28
93 11 MEM_B_DQS_P<1> MAKE_BASE=TRUE =MEM_B_DQS_P<1> 28

93 11 MEM_B_DQ<15> MAKE_BASE=TRUE =MEM_B_DQ<15> 28
93 11 MEM_B_DQ<14> MAKE_BASE=TRUE =MEM_B_DQ<14> 28
93 11 MEM_B_DQ<13> MAKE_BASE=TRUE =MEM_B_DQ<13> 28
93 11 MEM_B_DQ<12> MAKE_BASE=TRUE =MEM_B_DQ<12> 28
93 11 MEM_B_DQ<11> MAKE_BASE=TRUE =MEM_B_DQ<11> 28
93 11 MEM_B_DQ<10> MAKE_BASE=TRUE =MEM_B_DQ<10> 28
93 11 MEM_B_DQ<9> MAKE_BASE=TRUE =MEM_B_DQ<9> 28
93 11 MEM_B_DQ<8> MAKE_BASE=TRUE =MEM_B_DQ<8> 28

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

93 11 MEM_B_DQS_N<2> MAKE_BASE=TRUE =MEM_B_DQS_N<2> 28
93 11 MEM_B_DQS_P<2> MAKE_BASE=TRUE =MEM_B_DQS_P<2> 28

93 11 MEM_B_DQ<23> MAKE_BASE=TRUE =MEM_B_DQ<23> 28
93 11 MEM_B_DQ<22> MAKE_BASE=TRUE =MEM_B_DQ<22> 28
93 11 MEM_B_DQ<21> MAKE_BASE=TRUE =MEM_B_DQ<21> 28
93 11 MEM_B_DQ<20> MAKE_BASE=TRUE =MEM_B_DQ<20> 28
93 11 MEM_B_DQ<19> MAKE_BASE=TRUE =MEM_B_DQ<19> 28
93 11 MEM_B_DQ<18> MAKE_BASE=TRUE =MEM_B_DQ<18> 28
93 11 MEM_B_DQ<17> MAKE_BASE=TRUE =MEM_B_DQ<17> 28
93 11 MEM_B_DQ<16> MAKE_BASE=TRUE =MEM_B_DQ<16> 28

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

93 11 MEM_B_DQS_N<3> MAKE_BASE=TRUE =MEM_B_DQS_N<3> 28
93 11 MEM_B_DQS_P<3> MAKE_BASE=TRUE =MEM_B_DQS_P<3> 28

93 11 MEM_B_DQ<31> MAKE_BASE=TRUE =MEM_B_DQ<31> 28
93 11 MEM_B_DQ<30> MAKE_BASE=TRUE =MEM_B_DQ<30> 28
93 11 MEM_B_DQ<29> MAKE_BASE=TRUE =MEM_B_DQ<29> 28
93 11 MEM_B_DQ<28> MAKE_BASE=TRUE =MEM_B_DQ<28> 28
93 11 MEM_B_DQ<27> MAKE_BASE=TRUE =MEM_B_DQ<27> 28
93 11 MEM_B_DQ<26> MAKE_BASE=TRUE =MEM_B_DQ<26> 28
93 11 MEM_B_DQ<25> MAKE_BASE=TRUE =MEM_B_DQ<25> 28
93 11 MEM_B_DQ<24> MAKE_BASE=TRUE =MEM_B_DQ<24> 28

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

93 11 MEM_B_DQS_N<4> MAKE_BASE=TRUE =MEM_B_DQS_N<4> 28
93 11 MEM_B_DQS_P<4> MAKE_BASE=TRUE =MEM_B_DQS_P<4> 28

93 11 MEM_B_DQ<39> MAKE_BASE=TRUE =MEM_B_DQ<39> 28
93 11 MEM_B_DQ<38> MAKE_BASE=TRUE =MEM_B_DQ<38> 28
93 27 26 11 MEM_B_DQ<37> MAKE_BASE=TRUE =MEM_B_DQ<37> 11 27 28 93
93 11 MEM_B_DQ<36> MAKE_BASE=TRUE =MEM_B_DQ<36> 28
93 11 MEM_B_DQ<35> MAKE_BASE=TRUE =MEM_B_DQ<35> 28
93 11 MEM_B_DQ<34> MAKE_BASE=TRUE =MEM_B_DQ<34> 28
93 11 MEM_B_DQ<33> MAKE_BASE=TRUE =MEM_B_DQ<33> 28
93 11 MEM_B_DQ<32> MAKE_BASE=TRUE =MEM_B_DQ<32> 28

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

93 11 MEM_B_DQS_N<5> MAKE_BASE=TRUE =MEM_B_DQS_N<5> 28
93 11 MEM_B_DQS_P<5> MAKE_BASE=TRUE =MEM_B_DQS_P<5> 28

93 11 MEM_B_DQ<47> MAKE_BASE=TRUE =MEM_B_DQ<47> 28
93 11 MEM_B_DQ<46> MAKE_BASE=TRUE =MEM_B_DQ<46> 28
93 11 MEM_B_DQ<45> MAKE_BASE=TRUE =MEM_B_DQ<45> 28
93 11 MEM_B_DQ<44> MAKE_BASE=TRUE =MEM_B_DQ<44> 28
93 11 MEM_B_DQ<43> MAKE_BASE=TRUE =MEM_B_DQ<43> 28
93 11 MEM_B_DQ<42> MAKE_BASE=TRUE =MEM_B_DQ<42> 28
93 11 MEM_B_DQ<41> MAKE_BASE=TRUE =MEM_B_DQ<41> 28
93 11 MEM_B_DQ<40> MAKE_BASE=TRUE =MEM_B_DQ<40> 28

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

93 11 MEM_B_DQS_N<6> MAKE_BASE=TRUE =MEM_B_DQS_N<6> 28
93 11 MEM_B_DQS_P<6> MAKE_BASE=TRUE =MEM_B_DQS_P<6> 28

93 11 MEM_B_DQ<55> MAKE_BASE=TRUE =MEM_B_DQ<55> 28
93 11 MEM_B_DQ<54> MAKE_BASE=TRUE =MEM_B_DQ<54> 28
93 11 MEM_B_DQ<53> MAKE_BASE=TRUE =MEM_B_DQ<53> 28
93 11 MEM_B_DQ<52> MAKE_BASE=TRUE =MEM_B_DQ<52> 28
93 11 MEM_B_DQ<51> MAKE_BASE=TRUE =MEM_B_DQ<51> 28
93 11 MEM_B_DQ<50> MAKE_BASE=TRUE =MEM_B_DQ<50> 28
93 11 MEM_B_DQ<49> MAKE_BASE=TRUE =MEM_B_DQ<49> 28
93 11 MEM_B_DQ<48> MAKE_BASE=TRUE =MEM_B_DQ<48> 28

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

93 11 MEM_B_DQS_N<7> MAKE_BASE=TRUE =MEM_B_DQS_N<7> 28
93 11 MEM_B_DQS_P<7> MAKE_BASE=TRUE =MEM_B_DQS_P<7> 28

93 11 MEM_B_DQ<63> MAKE_BASE=TRUE =MEM_B_DQ<63> 28
93 11 MEM_B_DQ<62> MAKE_BASE=TRUE =MEM_B_DQ<62> 28
93 11 MEM_B_DQ<61> MAKE_BASE=TRUE =MEM_B_DQ<61> 28
93 11 MEM_B_DQ<60> MAKE_BASE=TRUE =MEM_B_DQ<60> 28
93 11 MEM_B_DQ<59> MAKE_BASE=TRUE =MEM_B_DQ<59> 28
93 11 MEM_B_DQ<58> MAKE_BASE=TRUE =MEM_B_DQ<58> 28
93 11 MEM_B_DQ<57> MAKE_BASE=TRUE =MEM_B_DQ<57> 28
93 11 MEM_B_DQ<56> MAKE_BASE=TRUE =MEM_B_DQ<56> 28

SYNC_MASTER=K92_YUN SYNC_DATE=05/14/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

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SHEET 27 OF 105

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C3100 10UF 20% 6.3V X6S CERM 603
C3101 10UF 20% 6.3V X6S CERM 603
PLACE_NEAR=J3100.75:2.54mm

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123
0.1UF 20% 10V CERM 402
PLACE_NEAR=J3100.75:2.54mm
PLACE_NEAR=J3100.75:2.54mm

PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-BGA6 DDR3-SODIMM (2 OF 2)

MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>
NC	75	VDD	VDD	76	
	77	NC	A15	78	MEM_B_A<15>
MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>
	81	VDD	VDD	82	
MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>
MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>
	87	VDD	VDD	88	
MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>
MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>
	93	VDD	VDD	94	
MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>
MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>
	99	VDD	VDD	100	
MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>
MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>
	105	VDD	VDD	106	
MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>
MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L
	111	VDD	VDD	112	
MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>
MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>
	117	VDD	VDD	118	
MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>
MEM_B_CS_L<1>	121	S1*	NC	122	
	123	VDD	VDD	124	
NC	125	TEST	VREFCA	126	
	127	VSS	VSS	128	
=MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>
=MEM_B_DQ<33>	131	DQ33	DQ37	132	MEM_B_DQ<37>
	133	VSS	VSS	134	
=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	
=MEM_B_DQS_P<4>	137	DQS4	VSS	138	
	139	VSS	DQ38	140	=MEM_B_DQ<38>
=MEM_B_DQ<34>	141	DQ34	DQ39	142	=MEM_B_DQ<39>
=MEM_B_DQ<35>	143	DQ35	VSS	144	
	145	VSS	DQ44	146	=MEM_B_DQ<44>
=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>
=MEM_B_DQ<41>	149	DQ41	VSS	150	
	151	VSS	DQS5*	152	=MEM_B_DQS_N<5>
	153	DM5	DQS5	154	=MEM_B_DQS_P<5>
	155	VSS	VSS	156	
=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>
=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>
	161	VSS	VSS	162	
=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>
=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>
	167	VSS	VSS	168	
=MEM_B_DQS_N<6>	169	DQS6*	DM6	170	
=MEM_B_DQS_P<6>	171	DQS6	VSS	172	
	173	VSS	DQ54	174	=MEM_B_DQ<54>
=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>
=MEM_B_DQ<51>	177	DQ51	VSS	178	
	179	VSS	DQ60	180	=MEM_B_DQ<60>
=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>
=MEM_B_DQ<57>	183	DQ57	VSS	184	
	185	VSS	DQS7*	186	=MEM_B_DQS_N<7>
	187	DM7	DQS7	188	=MEM_B_DQS_P<7>
	189	VSS	VSS	190	
=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>
=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>
	195	VSS	VSS	196	
MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L
	199	VDDSPD	SDA	200	SMBUS_PCH_DATA
MEM_B_SA<1>	201	SA1	SCL	202	SMBUS_PCH_CLK
	203	VTT	VTT	204	PP0V75_S0_DDRVTT
	205	MTG PIN	MTG PIN	206	
	207	MTG PIN	MTG PIN	208	
	209	MTG PIN	MTG PIN	210	
	211	MTG PIN	MTG PIN	212	

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

PP3V3_S0

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

J3100 F-RT-BGA6 DDR3-SODIMM (1 OF 2) CRITICAL

VREFDQ	1		VSS	2	
VSS	3		DQ4	4	=MEM_B_DQ<4>
=MEM_B_DQ<0>	5	DQ0	DQ5	6	=MEM_B_DQ<5>
=MEM_B_DQ<1>	7	DQ1	VSS	8	
	9	VSS	DQS0*	10	MEM_B_DQS_N<0>
	11	DM0	DQS0	12	MEM_B_DQS_P<0>
	13	VSS	VSS	14	
=MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6>
=MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7>
	19	VSS	VSS	20	
=MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12>
=MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13>
	25	VSS	VSS	26	
=MEM_B_DQS_N<1>	27	DQS1*	DM1	28	
=MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L
	31	VSS	VSS	32	
=MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14>
=MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15>
	37	VSS	VSS	38	
=MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20>
=MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21>
	43	VSS	VSS	44	
=MEM_B_DQS_N<2>	45	DQS2*	DM2	46	
=MEM_B_DQS_P<2>	47	DQS2	VSS	48	
	49	VSS	DQ22	50	=MEM_B_DQ<22>
=MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23>
=MEM_B_DQ<19>	53	DQ19	VSS	54	
	55	VSS	DQ28	56	=MEM_B_DQ<28>
=MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29>
=MEM_B_DQ<25>	59	DQ25	VSS	60	
	61	VSS	DQS3*	62	=MEM_B_DQS_N<3>
	63	DM3	DQS3	64	=MEM_B_DQS_P<3>
	65	VSS	VSS	66	
=MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30>
=MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31>
	71	VSS	VSS	72	

516S0806

PP0V75_S3_MEM_VREFCA_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

C3150 C3151 C3152 C3153
1UF 10% 10V X5R 402

"Expansion" (bottom) slot

SYNC_MASTER=K92_YUN SYNC_DATE=06/14/2010
PAGE TITLE: DDR3 SO-DIMM Connector B
Apple Inc.
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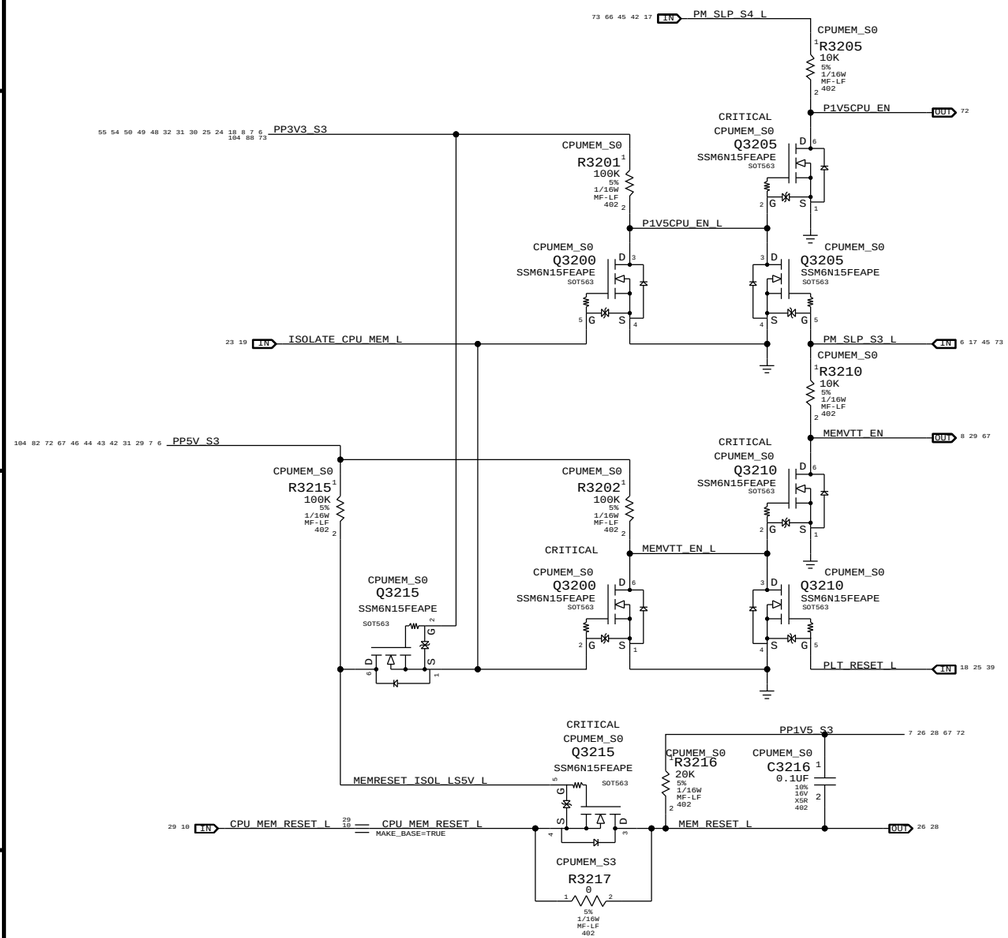
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

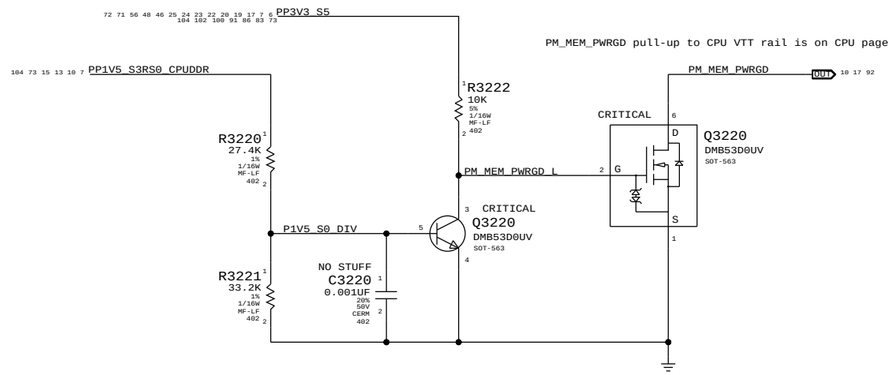


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

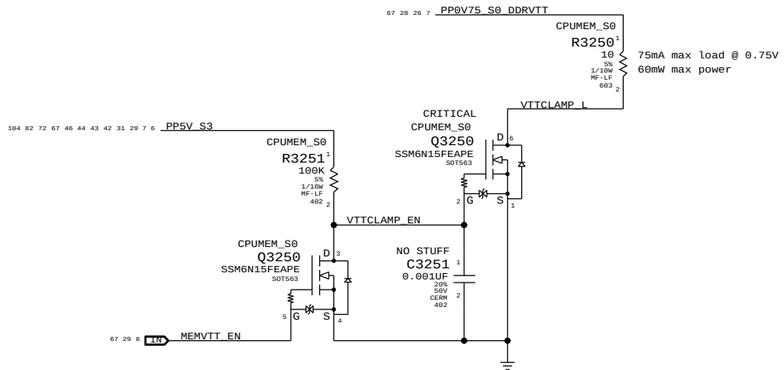
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K17_MLB	SYNC_DATE=04/26/2010
PAGE TITLE	CPU Memory S3 Support
Apple Inc.	DRAWING NUMBER / SIZE: D
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	BRANCH
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Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K91_YUN SYNC_DATE=08/26/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

OMIT_TABLE
L3470
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_R2D_PI_P
PLACE_NEAR=J3401.15:2.54mm
C3431 0.1UF 10% 16V X5R 402-1
PCIE_AP_R2D_C_P
NOSTUFF C3470 0.1UF 10% 16V X5R-CERM 0201
NOSTUFF C3471 0.1UF 10% 16V X5R-CERM 0201

L3471
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_R2D_PI_N
C3430 0.1UF 10% 16V X5R 402-1
PCIE_AP_R2D_C_N
NOSTUFF C3472 0.1UF 10% 16V X5R-CERM 0201
OMIT_TABLE
NOSTUFF C3473 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=J3401.17:2.54mm

SMBUS_SMC_0_S0_SDA
SMBUS_SMC_0_S0_SCL
WIFI_EVENT_L
PCIE_AP_R2D_P
PCIE_AP_R2D_N

OMIT_TABLE
L3473
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_P
NOSTUFF C3474 0.1UF 10% 16V X5R-CERM 0201
NOSTUFF C3475 0.1UF 10% 16V X5R-CERM 0201

L3474
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_N
NOSTUFF C3476 0.1UF 10% 16V X5R-CERM 0201
OMIT_TABLE
NOSTUFF C3477 0.1UF 10% 16V X5R-CERM 0201

516S0582
CRITICAL
J3401
500913-0302
F-ST-SM
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N

CRITICAL
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
PLACE_NEAR=J3401.11:2.54mm

AIRPORT

BLUETOOTH
USB_BT_P
USB_BT_N
PP3V3_S3_BT_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
C3432 0.01UF 10% 10V CERM 402
L3406
FERR-120-OHM-1.5A
0402-LF
PLACE_NEAR=J3401.27:2.54MM
PP3V3_S3

AP_RESET_CONN_L
AP_CLKREQ_Q_L
PCIE_WAKE_L

1A PEAK
155S0367
L3404
FERR-120-OHM-3A
0603
PP3V3_WLAN
PP3V3_WLAN_F
MIN_NECK_WIDTH=0.4 mm
MIN_LINE_WIDTH=1 mm
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.5 mm
C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 20% 10V CERM 402
PLACE_NEAR=J3401.29:2.54MM
107S0137
CRITICAL
R3452
0.005
1% 1W MF 0612
PP3V3_WLAN_R
CRITICAL
Q3450
TPCP8102
23V1K-SM
C3450 0.1UF 10% 16V X5R 402-1
C3451 0.033UF 10% 16V X5R 402
R3450 33K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402
PP3V3_S3
P3V3WLAN_SS
PM_WLAN_EN_L
ISNS_AIRPORT_P
ISNS_AIRPORT_N

Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

PP3V3_WLAN_F
PP3V3_S3
R3453 100K 1% 1/10W MF-LF 402
R3454 232K 1% 1/10W MF-LF 402
P3V3WLAN_VMON
CRITICAL
U3440
SLG4AP016V
TDFN
VDD
SENSE
0.7V
KDLY
RESET*
MR*
EN
OUT
IN
THRM PAD
GND
C3440 0.1uF 20% 10V CERM 402
AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L
R3455 100K 1% 1/10W MF-LF 402

518S0816
CRITICAL
J3402
CCR20-6K710S
F-RT-SM
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_A_S3_SCL
SMBUS_SMC_A_S3_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

ALS
CAMERA

275 mA peak
206 mA nominal max

CRITICAL
L3407
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACE_NEAR=J3402.3:2.54MM

PLACE_NEAR=J3402.6:2.54MM
L3408
FERR-120-OHM-1.5A
0402-LF
PP5V_S3
C3452 0.1uF 20% 10V CERM 402

SYNC_MASTER=K91_MLB	SYNC_DATE=10/21/2016
PAGE TITLE	X19/ALS/CAMERA CONNECTOR
Apple Inc.	DRAWING NUMBER: SIZE: D
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	BRANCH:
	PAGE: 34 OF 132
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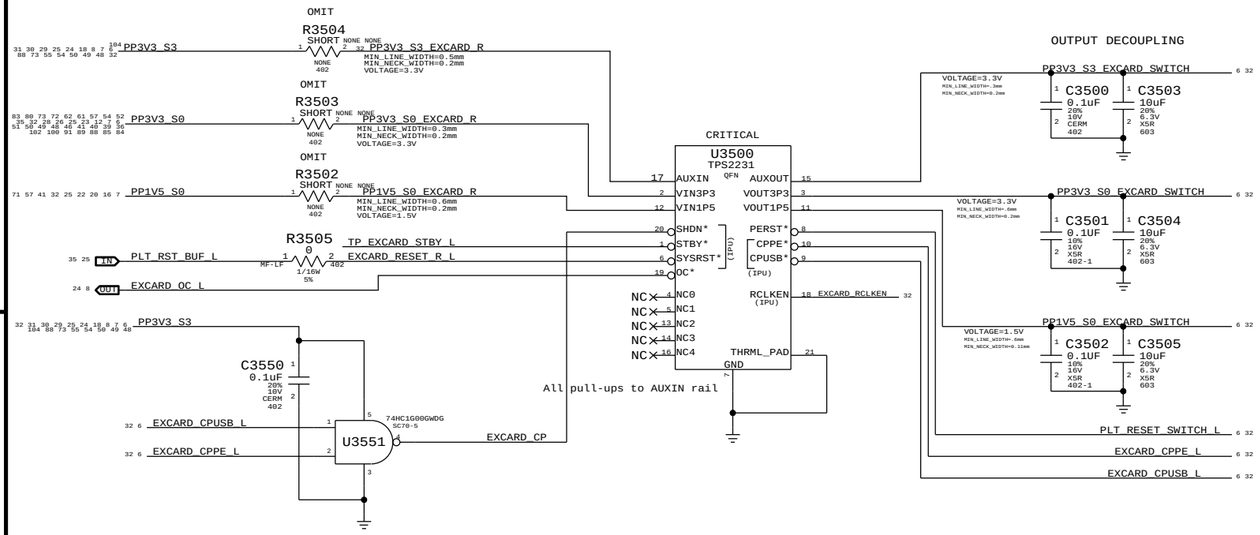

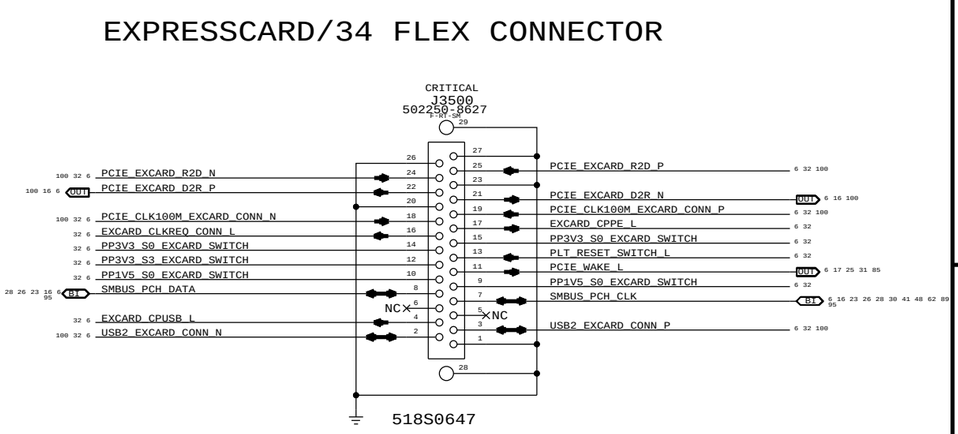

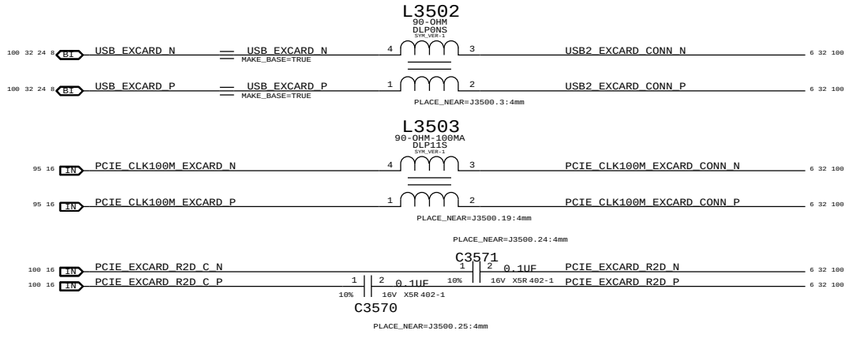

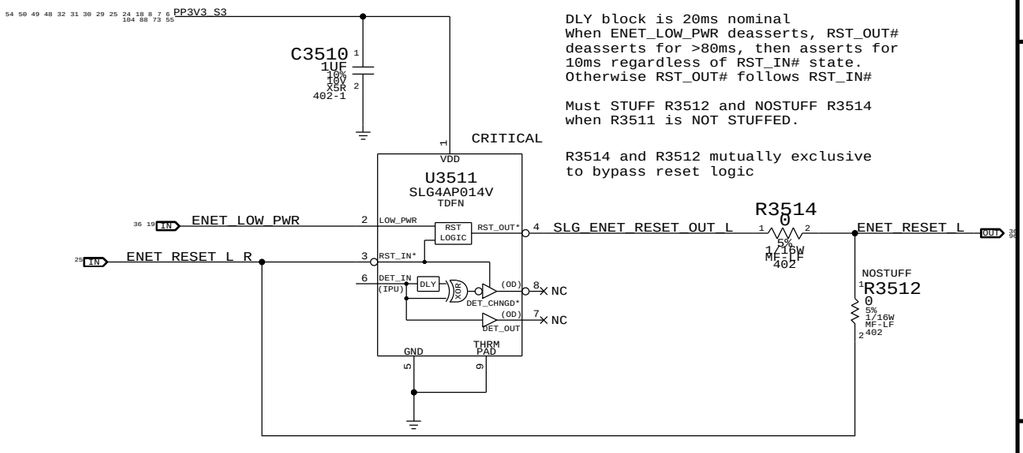

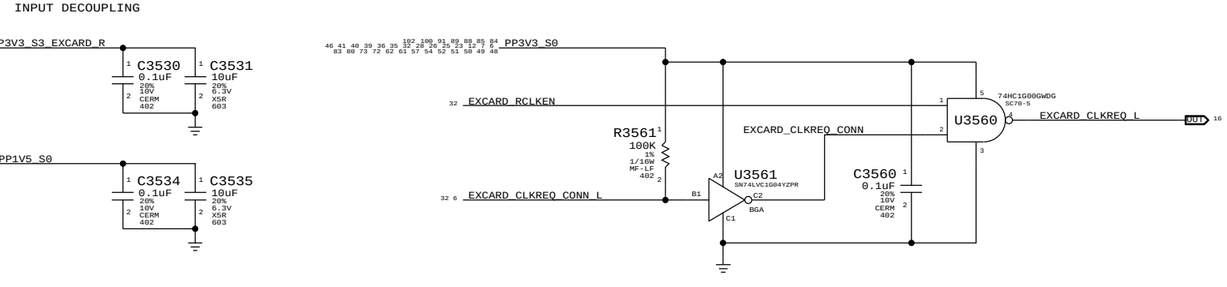

SYNC_MASTER=K92_ERIC SYNC_DATE=07/27/2010

PAGE TITLE: ExpressCard Connector

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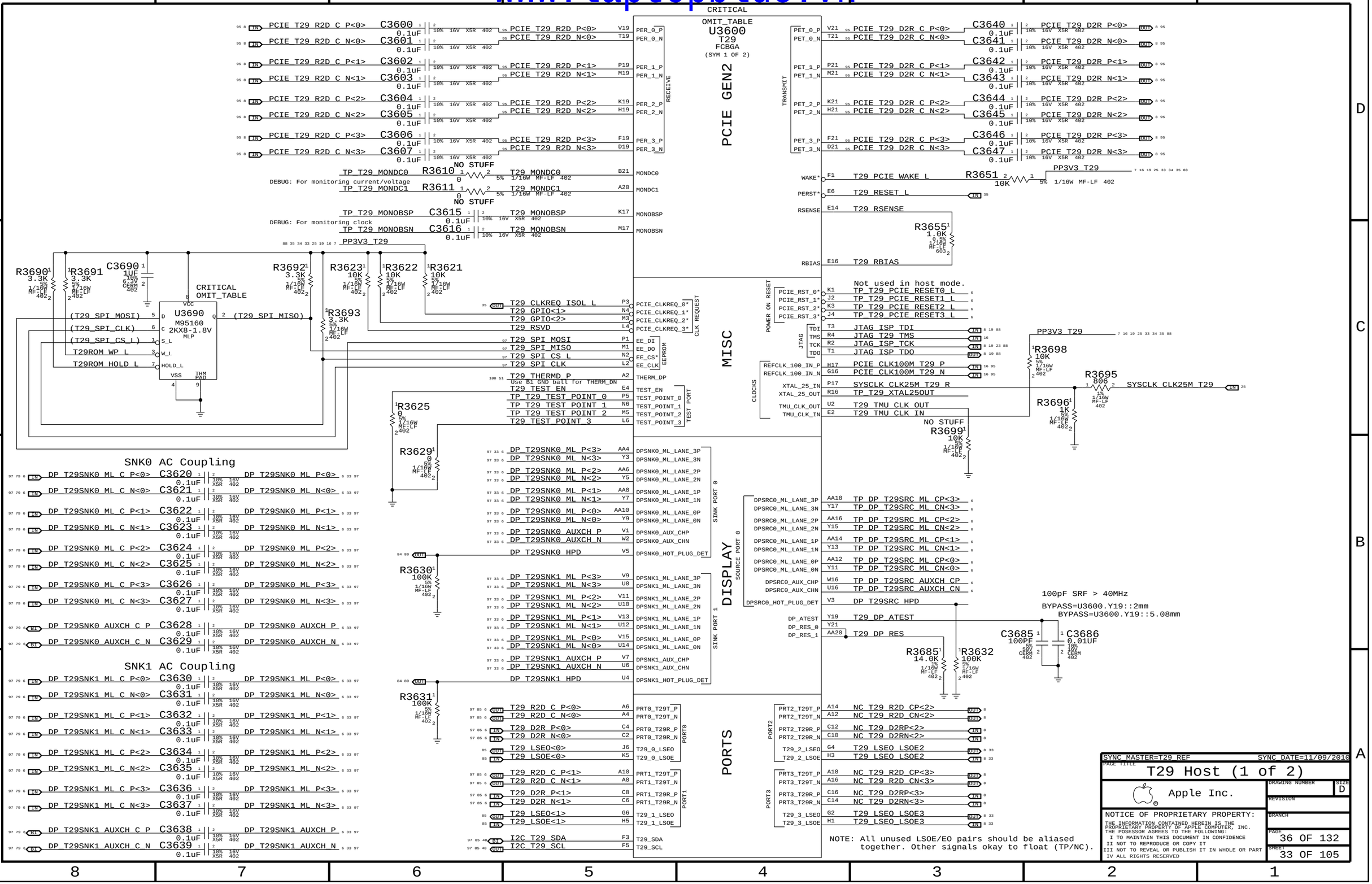

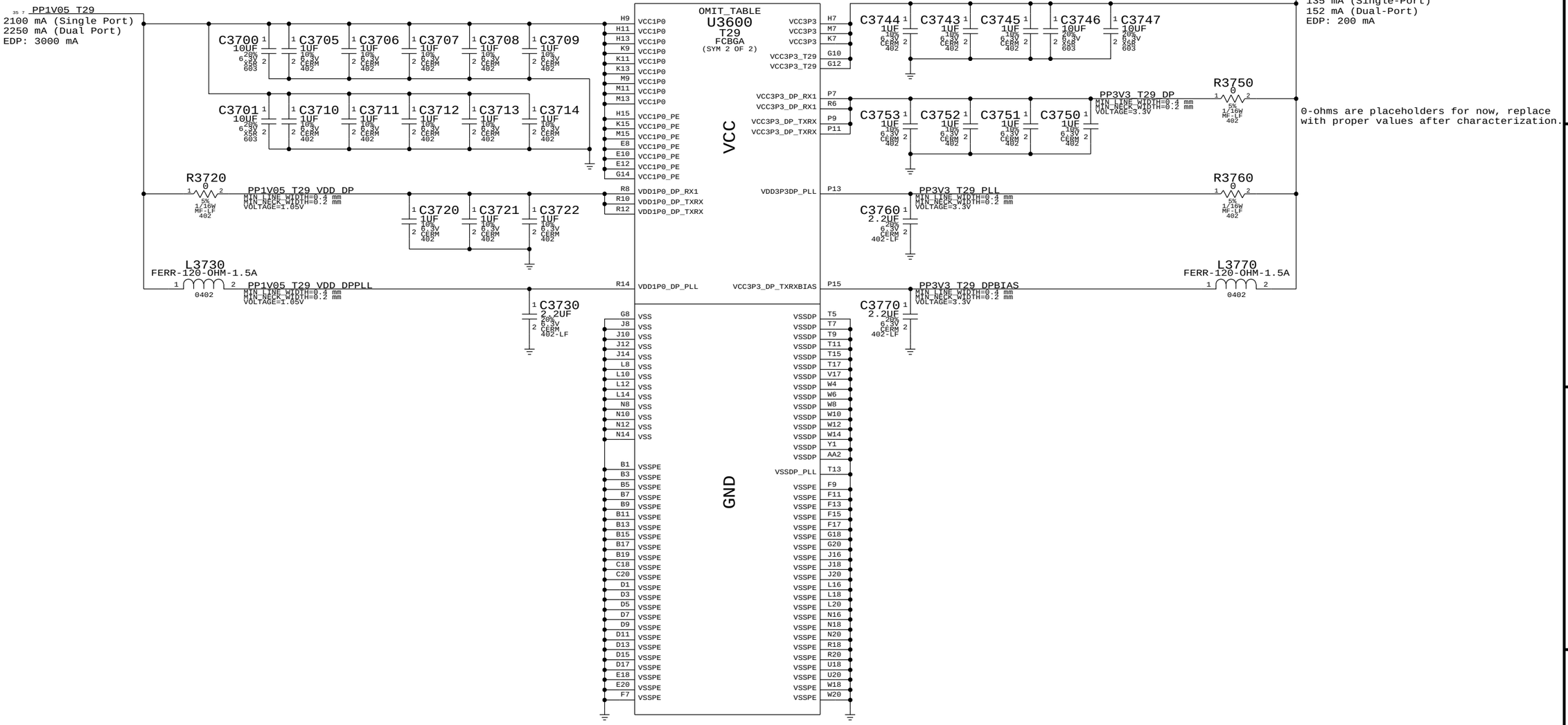

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required for 2S.

CRITICAL T29BST:Y Q3880 SI8409DB 86A

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

CRITICAL T29BST:Y L3895 10UH-4A-68-MOHM PCMB063T-100MS

T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL T29BST:Y U3890 LT3957 QFN

T29BST_EN_UVLO
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
GND_T29BST_SGND
T29BST_SNS1
T29BST_SNS2
T29BST_VSNS
T29BST_FBX
SGND
GND

CRITICAL T29BST:Y D3895 POWERDI-123 DFLS230L

XW3895 SM PLACE_NEAR=C3895.1:2 mm

PP15V_T29
Vout = 15.47V
Max Current = 1A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

T29BST:Y Q3888 SSM6N37FEAPE SOT563 Max Vgs: 10V

T29BST_SHDN_DIV

SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

PP3V3_S0

Platform (PCIe) Reset
PLT_RST_BUF_L

CRITICAL U3800 SLG4AP016V TDFN

PP3V3_T29
PP1V05_T29
T29_RESET_L
DLY = 60 ms +/- 20%
T29_CLKREQ_ISOL_L

T29_SW_RESET_L
T29_CLKREQ_L

Open-Drain GPIO
Pull-up provided by SB page.

3.3V T29 Switch

U3810 TPS22924 CSP CRITICAL

PP3V3_S0
PP3V3_T29
Max Current = 1.7A (85C)

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch

U3815 TPS22924 CSP CRITICAL

PP1V05_S0
PP1V05_T29
Max Current = 3.4A (85C)

U3816 TPS22924 CSP CRITICAL

T29_PWR_EN
U3816.A2: PLACE_NEAR=U3815.B2:3 mm
Pull-up provided by SB page.

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Power Support

Apple Inc.

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

PP1V2_ENET
???mA (1000base-T, Caesar V)

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG

ENET_SR_LX

Internal 1.2V Switching Regulator pins.

CRITICAL
L3900
FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_XTALVDDH
C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3905
FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_BIASVDDH
C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3910
FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_AVDDH
R3910 4.7K 5% 1/10W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3920
FERR-600-OHM-0.5A
PP1V2_ENET_PHY_AVDDL
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3925
FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3930
FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

R3940 4.7K 5% 1/10W MF-LF 402
R3941 4.7K 5% 1/10W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

C3936 0.1UF 10% 16V X7R-CERM 402
CRITICAL
C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3_S0
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402
C3951 0.1uF 10% 16V X5R 402
C3955 0.1uF 10% 16V X5R 402
C3956 0.1uF 10% 16V X5R 402

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

R3943 0 5% 1/16W MF-LF 402
ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT
U3900
BCM57765B0
QFN-8X8
CRITICAL

	ENET_VMAIN_PRSNT	VMAIN_PRSNT(IPD)
PCIE_ENET_D2R_C_N	PCIE_ENET_D2R_C_N	PCIE_TXD_N
PCIE_ENET_D2R_C_P	PCIE_ENET_D2R_C_P	PCIE_TXD_P
	PCIE_ENET_R2D_P	PCIE_RXD_P
	PCIE_ENET_R2D_N	PCIE_RXD_N
	PCIE_CLK100M_ENET_P	PCIE_REFCLK_P
	PCIE_CLK100M_ENET_N	PCIE_REFCLK_N
	ENET_RESET_L	PERST* (IPD)
	ENET_CLKREQ_L	CLKREQ* (OD)
	ENET_WAKE_R_L	WAKE* (OD)
	ENET_LOW_PWR	LOW_PWR (IPD)
	BCM57765_SMB_CLK	SMB_CLK
	BCM57765_SMB_DATA	SMD_DATA (IPD)
BCM57765_SCLK	BCM57765_SCLK	SCLK
BCM57765_MISO	BCM57765_MISO	SI/LINKLED*
BCM57765_MOSI	BCM57765_MOSI	SO
BCM57765_CS_L	BCM57765_CS_L	CS*
NC_BCM57765_SPD100LED_L		SPD100LED*/SERIAL_DO (OD)
NC_BCM57765_TRAFFICLED_L		TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET		XTALI
		XTALO
BCM57765_RDAC		RDAC

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

	GPIO_0	NC
	GPIO_1/CR_BUS_PWR	
	RE*/GPIO_2	
	SD_DETECT/WE*	TP_SDCONN_DETECT_L
	CR_CMD/CLE	TP_SDCONN_CMD
	CR_CLK/RY_BY*	TP_SDCONN_CLK
	CR_DATA0	TP_SDCONN_DATA<0>
	CR_DATA1	TP_SDCONN_DATA<1>
	CR_DATA2	TP_SDCONN_DATA<2>
	CR_DATA3	TP_SDCONN_DATA<3>
	CR_DATA4	TP_SDCONN_DATA<4>
	CR_DATA5	TP_SDCONN_DATA<5>
	CR_DATA6	TP_SDCONN_DATA<6>
	CR_DATA7	TP_SDCONN_DATA<7>
NC_CE_L_MS_INS_L	CE*/MS_INS*	
TP_ENET_CR_PWREN	CR_LED/ALE	
	CR_WP*/XD_WP*	TP_SDCONN_WP
BDM57765_SR_DISABLE	XD_DETECT	

ENET_MDI_P<0>	TRD0_P	ENET_MDI_P<0>
ENET_MDI_N<0>	TRD0_N	ENET_MDI_N<0>
ENET_MDI_P<1>	TRD1_P	ENET_MDI_P<1>
ENET_MDI_N<1>	TRD1_N	ENET_MDI_N<1>
ENET_MDI_P<2>	TRD2_P	ENET_MDI_P<2>
ENET_MDI_N<2>	TRD2_N	ENET_MDI_N<2>
ENET_MDI_P<3>	TRD3_P	ENET_MDI_P<3>
ENET_MDI_N<3>	TRD3_N	ENET_MDI_N<3>

ENET_MEDIA_SENSE

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3980 1K 5% 1/16W MF-LF 402

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET
C3990 0.1UF 10% 16V X5R-CERM 402
U3990
AT45DB011D
SOIC-8S1
OMIT
VCC
SCK
CS*
WP*
RESET*
SI
SO
GND
BCM57765_SCLK
BCM57765_CS_L
BCM57765_MOSI
BCM57765_MISO
NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K92_ERIC SYNC_DATE=10/19/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

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SIZE D
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Place one of 0.1uf cap close to each centertap pin of transformer

ENETCONN_CTAP

C4000 C4002 C4004 C4006
0.1UF 10% 10V X5R 402-1

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_N<1>
ENET_MDI_P<1>
ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_N<3>
ENET_MDI_P<3>

CRITICAL
T4000
SM
TX
TLA-6T213HF

CRITICAL
T4001
SM
TX
TLA-6T213HF

ENETCONN_P<0>
ENETCONN_N<0>
ENET_CTAP0
ENET_CTAP1
ENETCONN_N<1>
ENETCONN_P<1>
ENETCONN_N<2>
ENETCONN_P<2>
ENET_CTAP2
ENET_CTAP3
ENETCONN_N<3>
ENETCONN_P<3>

Transformers should be mirrored on opposite sides of the board

R4000 R4001 R4002 R4003
75 5% 1/16W MF-LF 402-2

CRITICAL
J4000
RJ45-M97-3
F-RT-TH
514-0636

CRITICAL
C4008
1000PF 10% 2KV CERM 1206

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm

PLACE_NEAR=T4001.1:5mm
PLACE_NEAR=T4000.5:5mm

D4001
RCLAMP0524P
SLP2510P8
CRITICAL
NOSTUFF

D4000
RCLAMP0524P
SLP2510P8
CRITICAL
NOSTUFF

SYNC_MASTER=K92_ERIC SYNC_DATE=08/24/2010

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER
SIZE: D
REVISION
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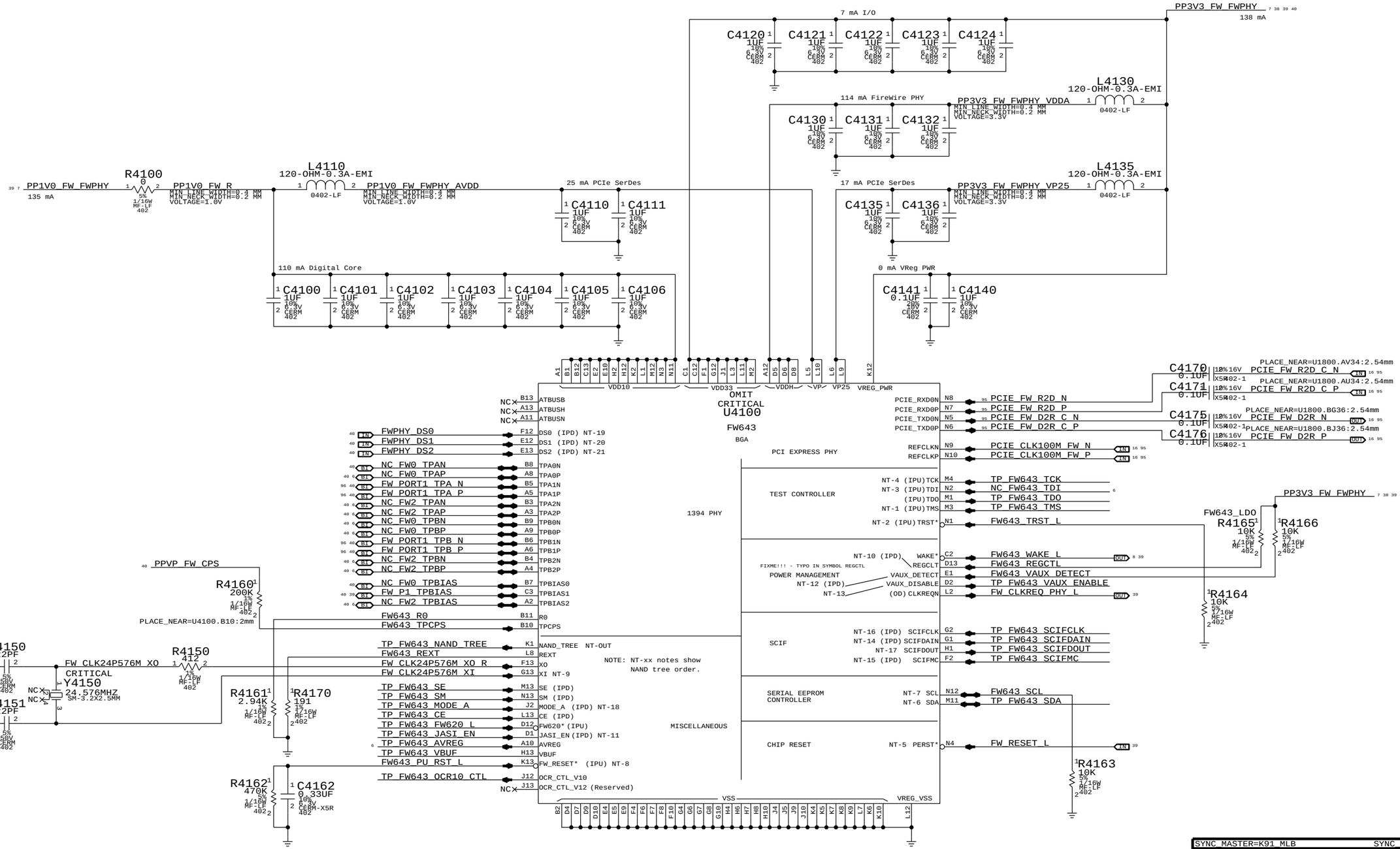

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

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Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

PPBUS_G3H

Q4262 provides for fast-off of Q4260 in S0 (Late-VG detection)

CRITICAL Q4260 FDC638P_G SM

PPBUS_FW_FWPWRSW_F — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V

CRITICAL F4260 1.1A-24V MINISMDC110H24

PPBUS_FW_FWPWRSW_D — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V

CRITICAL D4260 SM CRS08-1.5A-30V

PPVP_FW

R4262 10K 5% 1/10W MF-LF 402

R4263 10 5% 1/10W MF-LF 402

FWPORT_FASTOFF_L_DIV

CRITICAL Q4262 BSS8402DW SOT-363 (SYM-VER1)

FWPORT_PWREN_L_DIV

R4260 300K 5% 1/10W MF-LF 402

C4260 0.1UF 10% 16V X5R 402

FWPORT_FASTOFF_L

PP3V3_S0

CRITICAL Q4262 BSS8402DW SOT-363 (SYM-VER1)

R4261 470K 5% 1/10W MF-LF 402

FWPORT_PWREN_L

CRITICAL Q4261 SSM3K15FV SOD-VESM-HF

NO STUFF C4261 0.1UF 10% 25V X5R 402

FWPORT_PWR_EN (IN)

Supervisor & CLKREQ# Isolation

PP3V3_S0

PP3V3_FW_FWPHY

C4290 0.1UF 10% 16V X5R 402

CRITICAL U4290 SLG4AP016V TDFN

R4290 100K 5% 1/16W MF-LF 402

PLT_RESET_L (IN)

R4283 10K 5% 1/10W MF-LF 402

PP1V0_FW_FWPHY

SENSE 0.7V

DLY

RESET*

FW_RESET_L (OUT) — DLY = 60 ms +/- 20%

FW_RESET_R_L

MR*

FW_PWR_EN (IN)

FW_CLKREQ_L (OUT)

EN

OUT (OD)

IN

FW_CLKREQ_PHY_L (IN) — MAKE_BASE=TRUE

GND

THRM PAD

Pull-up provided by another page.

FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

PP1V05_S0

R4275 1K 5% 1/10W MF-LF 402

FW_PWR_EN_L

FW_PWR_EN (IN)

CRITICAL Q4275 DMB53D0UV SOT-563

R4270 330K 5% 1/16W MF-LF 402

R4271 56K 5% 1/16W MF-LF 402

FW_5KPD_DET_L — MAKE_BASE=TRUE

FW_5KPD_DET_RC

CRITICAL Q4275 DMB53D0UV SOT-563

CRITICAL Q4270 BC847CDXV6TXG SOT563

FWDET_MIRROR

CRITICAL Q4270 BC847CDXV6TXG SOT563

C4270 0.1UF 10% 16V X5R 402

FW_P1_TPBIAS_R

FWDET_EMIT

R4272 1K 5% 1/10W MF-LF 402

R4273 12K 5% 1/10W MF-LF 402

PLACE_NEAR=C4360.1:2 mm

FW_P1_TPBIAS (IN)

FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

PP3V3_FW_FWPHY

R4277 10K 5% 1/10W MF-LF 402

R4276 100K 5% 1/16W MF-LF 402

FW_WAKE

NO STUFF C4276 0.1UF 10% 16V X5R 402

FW643_WAKE_L (IN) — FW643_WAKE_L — MAKE_BASE=TRUE

CRITICAL Q4276 DMB53D0UV SOT-563

Dual-purpose output:
1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

FW_PLUG_DET_L (OUT)

Pull-up provided on another page.

3.3V FW Switch

PP3V3_S0

U4201 TPS22924 CSP

CRITICAL

C4201 1UF 10% 6.3V CERM 402

PP3V3_FW_FWPHY

Max Current = 1.7A (85C)

U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch

PP1V05_S0

U4202 TPS22924 CSP

CRITICAL

C4202 1UF 10% 6.3V CERM 402

PP1V05_FW_FET — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V

R4202 0.549 1% 1/16W MF 402

PP1V0_FW_FWPHY

LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE: FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER: — SIZE: D
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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

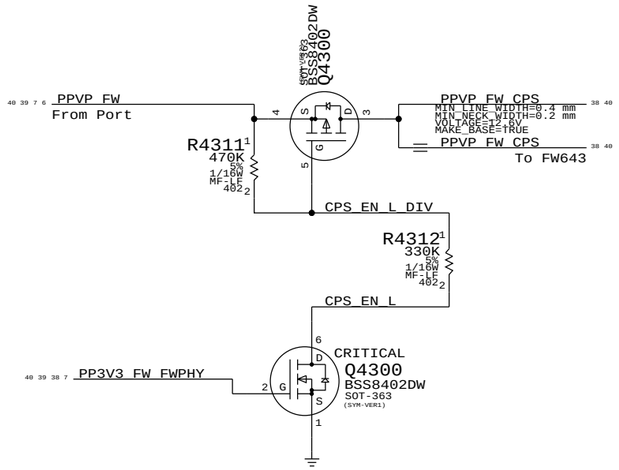
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

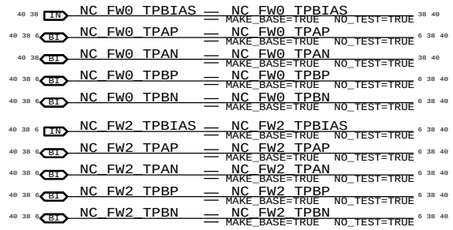
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



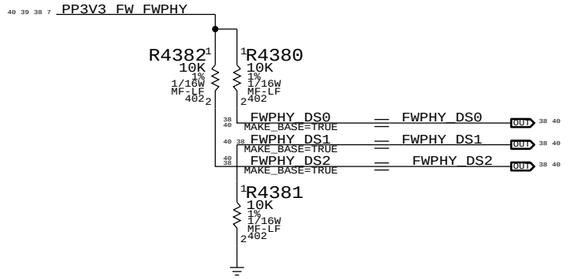
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



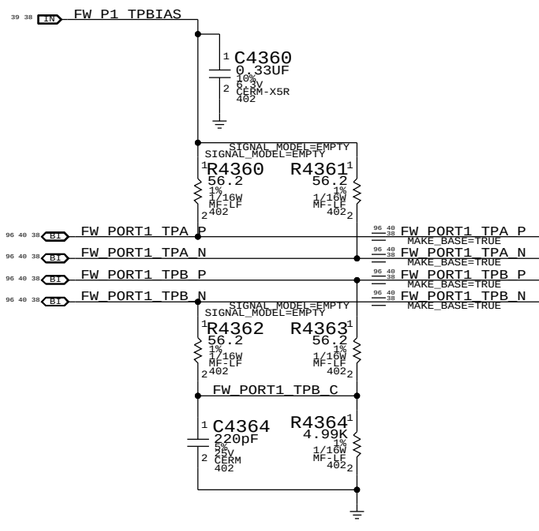
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

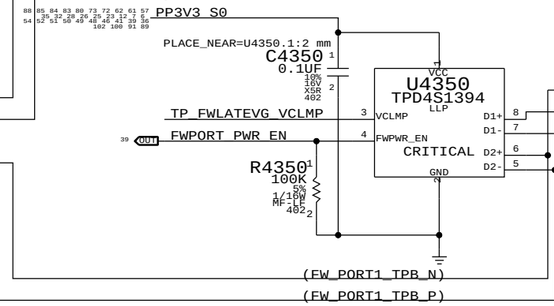


Termination

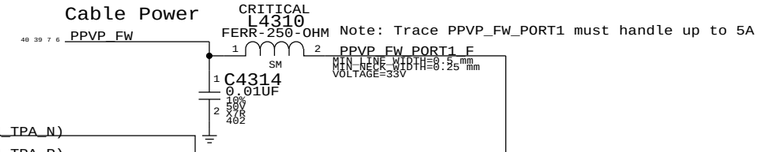
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



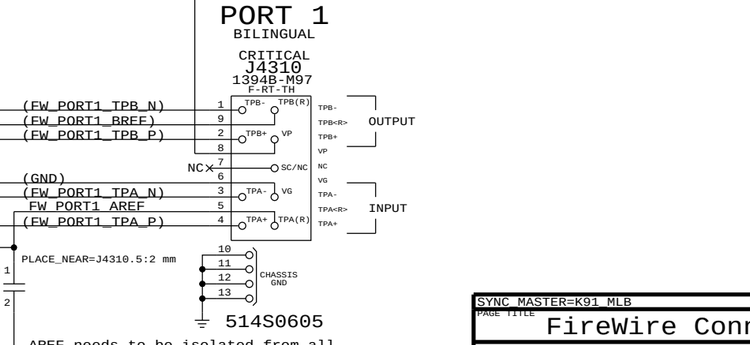
Cable Power



Note: Trace PPVP_FW_PORT1 must handle up to 5A

PORT 1

BILINGUAL



AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: FireWire Connector

Apple Inc.

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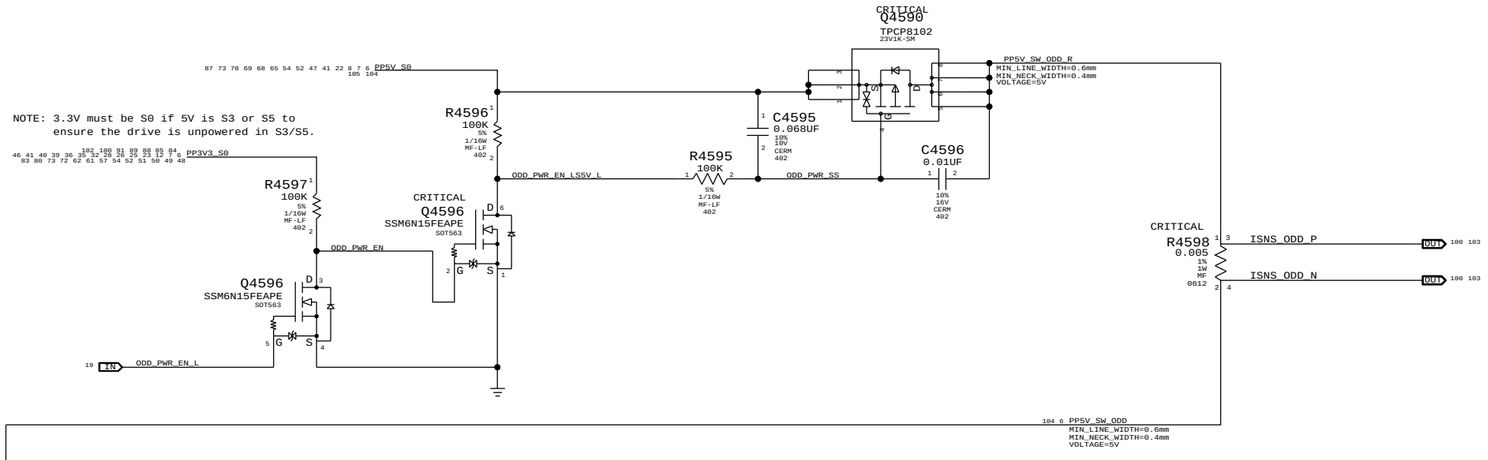
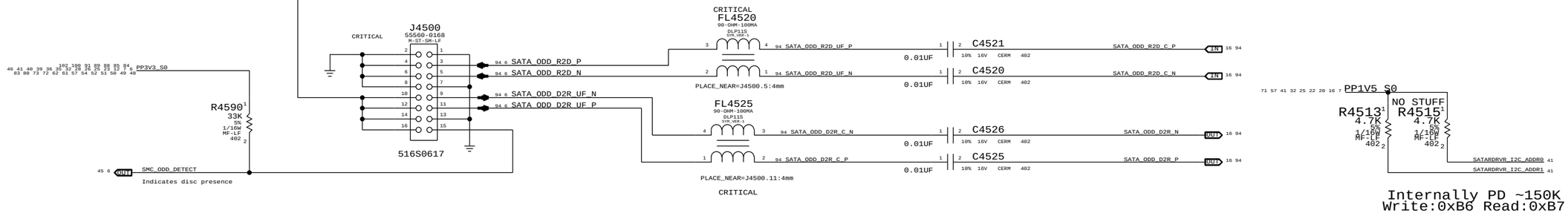
ODD Power Control



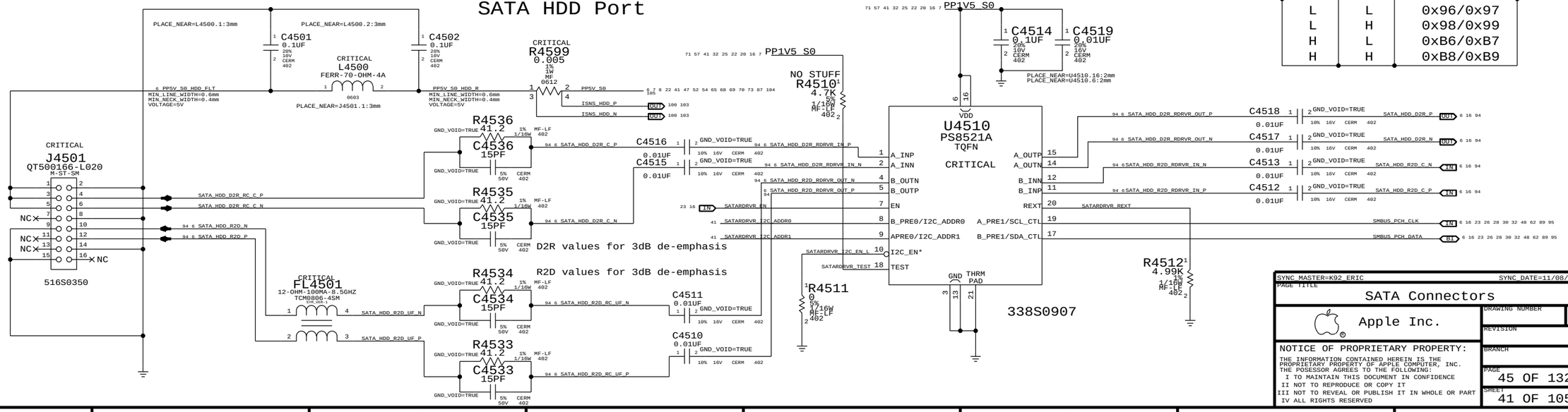
SATA ODD Port



Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADDR0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD Port



SYNC_MASTER=K92_ERIC	SYNC_DATE=11/08/2010
PAGE TITLE	SATA Connectors
Apple Inc.	DRAWING NUMBER: SIZE D
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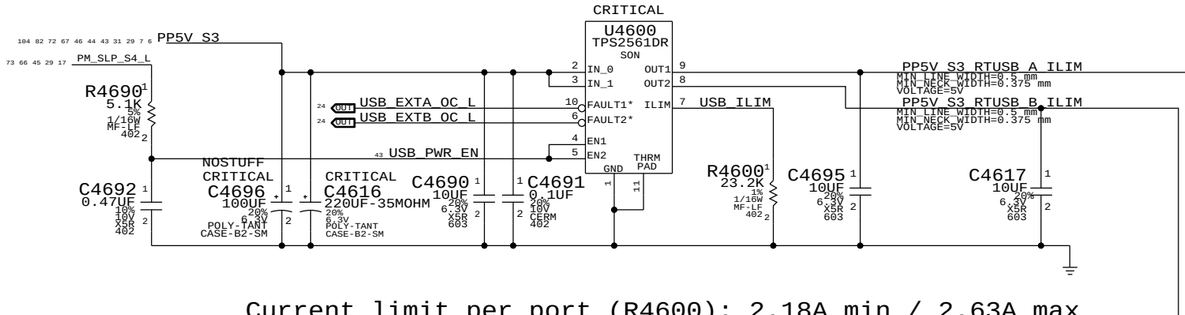
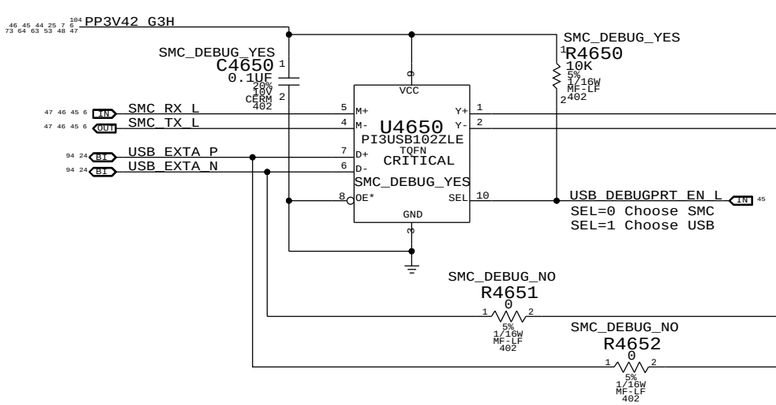
USB Port Power Switch

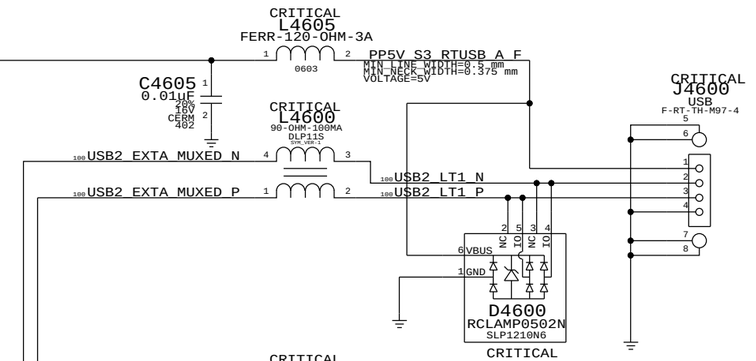


Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux

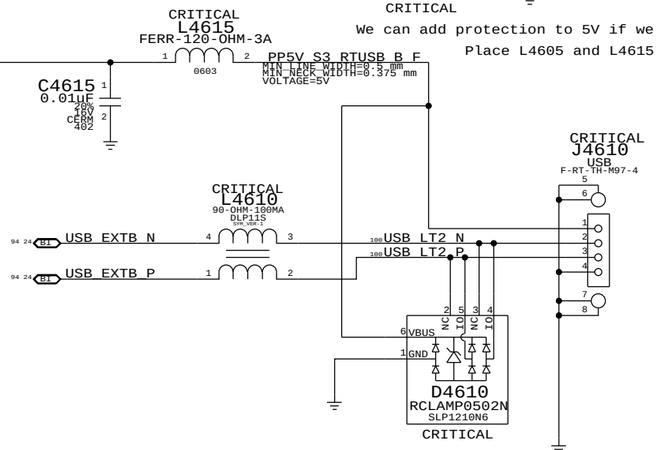


Left USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



Left USB Port B

SYNC_MASTER=K92_ERIC SYNC_DATE=08/24/2010

PAGE TITLE: External USB Connectors

Apple Inc.

DRAWING NUMBER: SIZE D

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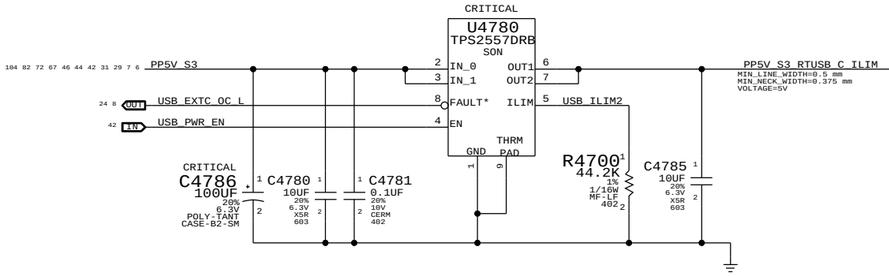
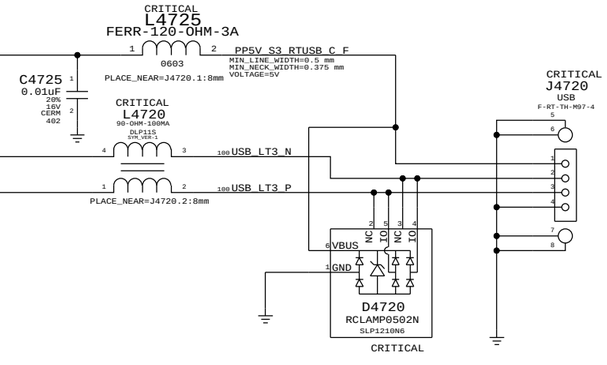
USB Port Power Switch



Current limit (R4700): 2.19A min / 2.76A max

94 24 B7 USB_EXTC_N
94 24 B7 USB_EXTC_P

LEFT USB PORT C



SYNC_MASTER=K92_ERIC	SYNC_DATE=07/22/2010
PAGE TITLE: PROJECT SPECIFIC CONNS	
Apple Inc.	DRAWING NUMBER / SIZE: D
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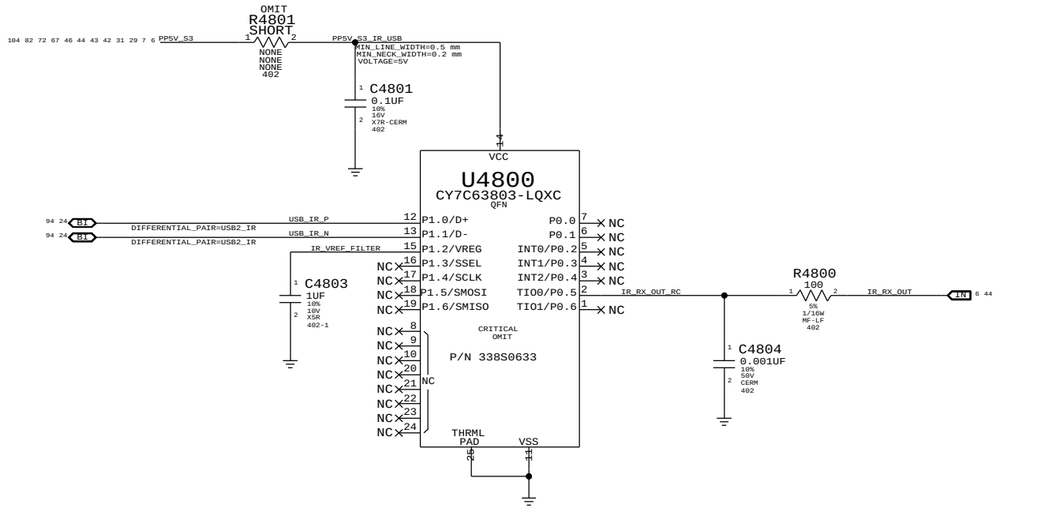

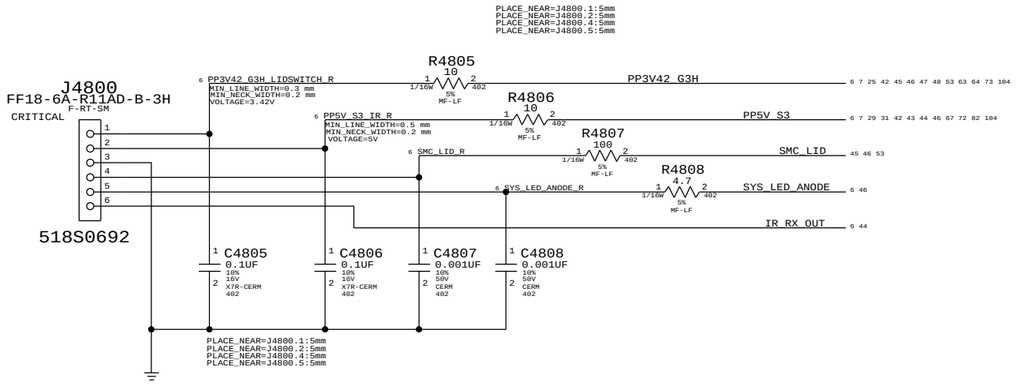

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

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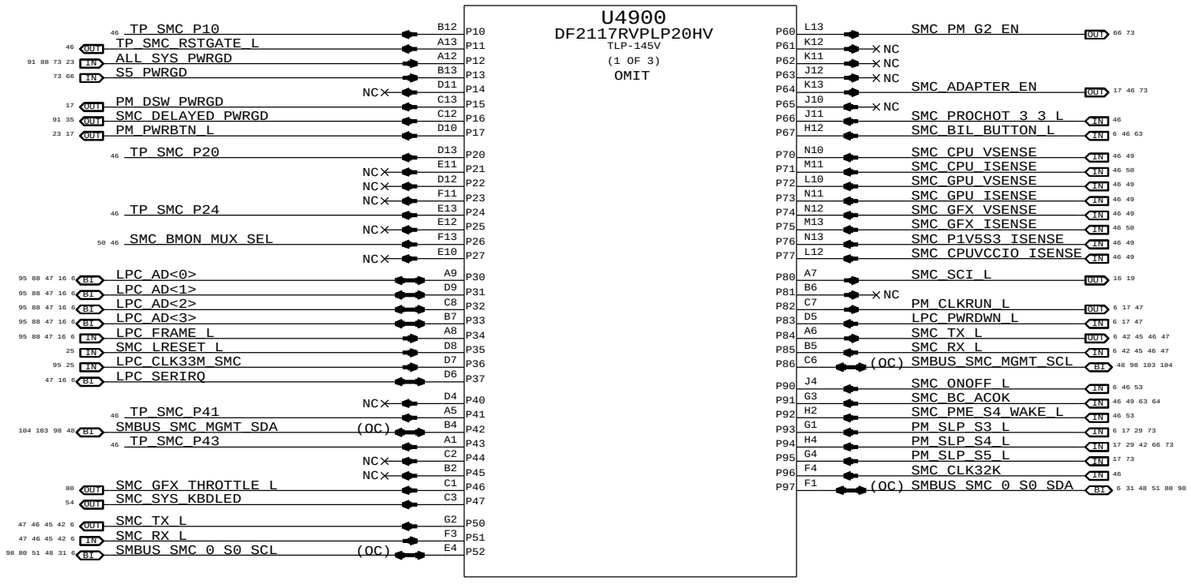
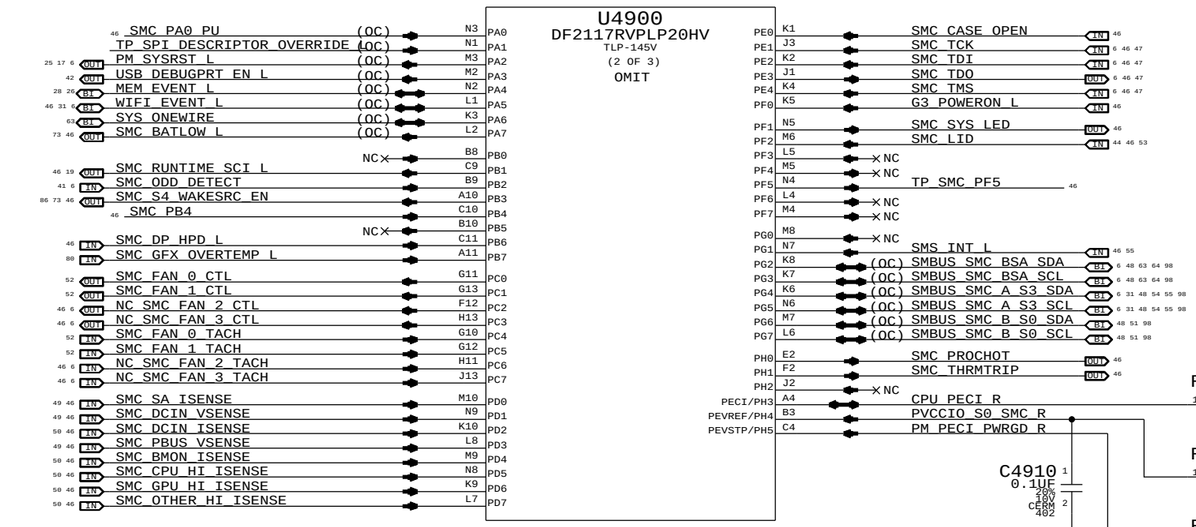
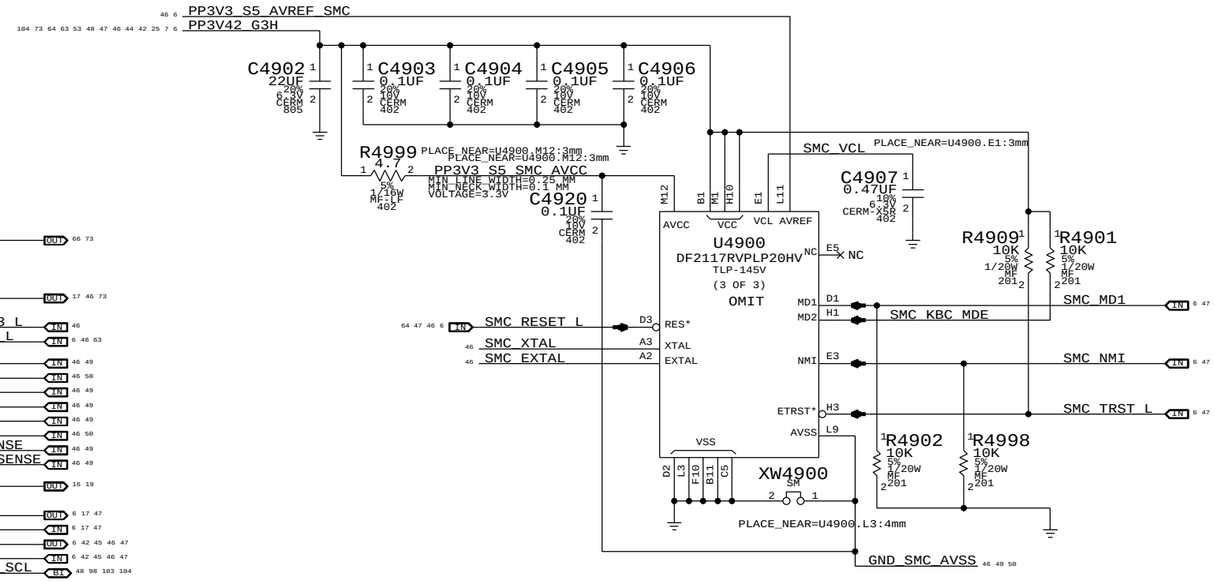
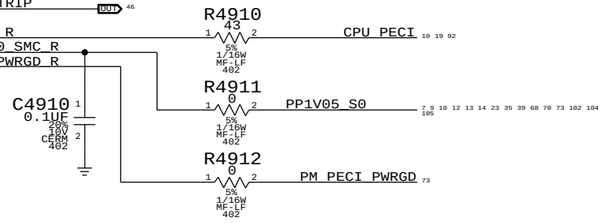
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.





SYNC_MASTER=K91_BEN	SYNC_DATE=07/12/2010
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: D; SIZE: D
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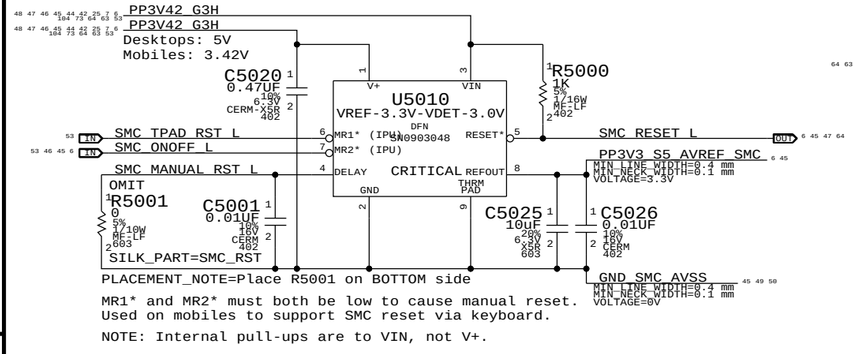
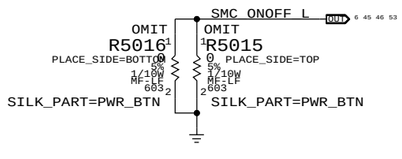
SMC Reset "Button", Supervisor & AVREF Supply



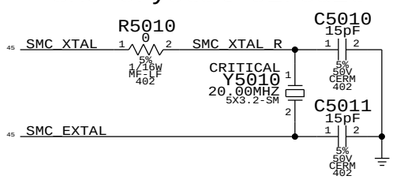
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

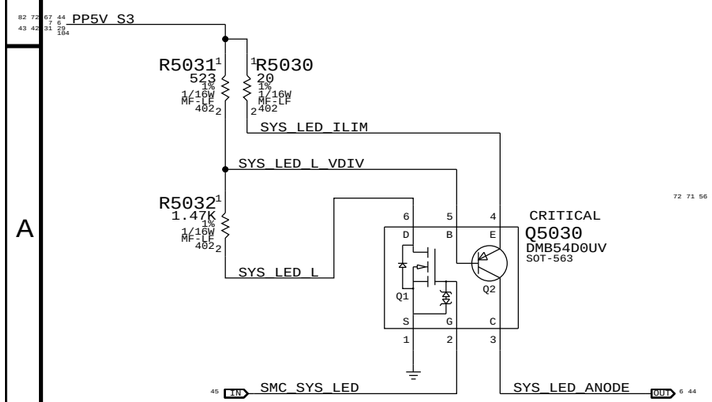
Debug Power "Buttons"



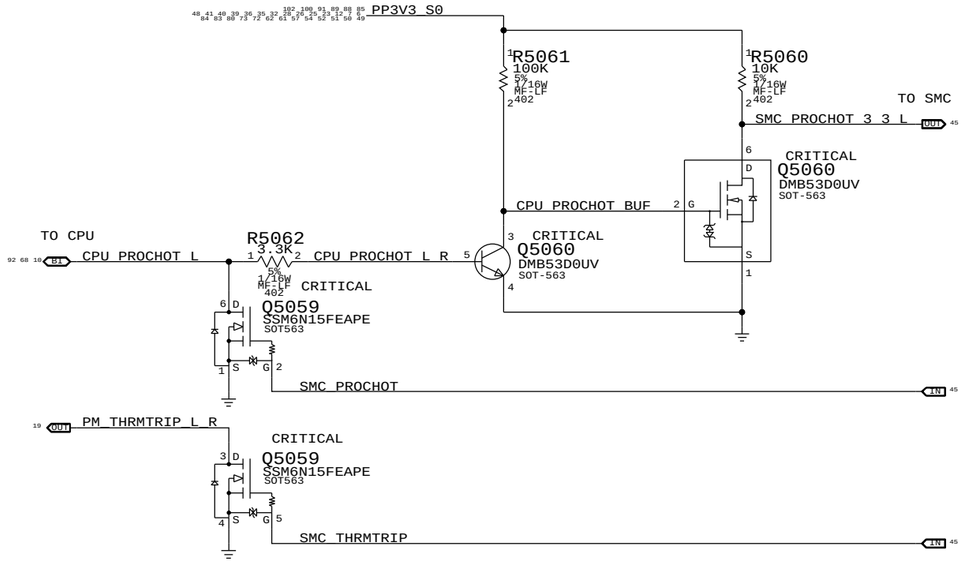
SMC Crystal Circuit



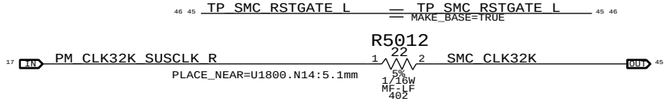
System (Sleep) LED Circuit

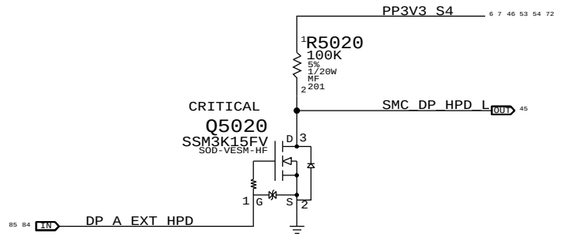


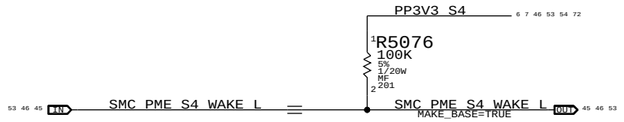
SMC FSB to 3.3V Level Shifting



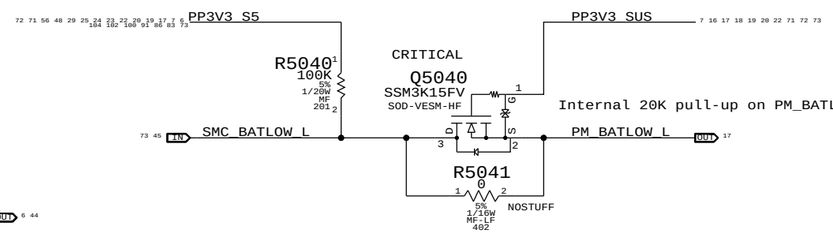
NC_SMC_FAN_2_CTL	=	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE				
NC_SMC_FAN_2_TACH	=	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE				
NC_SMC_FAN_3_CTL	=	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE				
NC_SMC_FAN_3_TACH	=	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE				
SMC_BC_ACOK	=	SMC_BC_ACOK	MAKE_BASE=TRUE				
SMS_INT_L	=	SMS_INT_L	MAKE_BASE=TRUE				
SMC_CPU_VSENSE	=	SMC_CPU_VSENSE	MAKE_BASE=TRUE				
SMC_CPU_ISENSE	=	SMC_CPU_ISENSE	MAKE_BASE=TRUE				
SMC_GPU_VSENSE	=	SMC_GPU_VSENSE	MAKE_BASE=TRUE				
SMC_GPU_ISENSE	=	SMC_GPU_ISENSE	MAKE_BASE=TRUE				
SMC_GFX_VSENSE	=	SMC_GFX_VSENSE	MAKE_BASE=TRUE				
SMC_GFX_ISENSE	=	SMC_GFX_ISENSE	MAKE_BASE=TRUE				
SMC_P1V5S3_ISENSE	=	SMC_P1V5S3_ISENSE	MAKE_BASE=TRUE				
SMC_CPUVCCIO_ISENSE	=	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE				
SMC_SA_ISENSE	=	SMC_SA_ISENSE	MAKE_BASE=TRUE				
SMC_DCIN_VSENSE	=	SMC_DCIN_VSENSE	MAKE_BASE=TRUE				
SMC_DCIN_ISENSE	=	SMC_DCIN_ISENSE	MAKE_BASE=TRUE				
SMC_PBUS_VSENSE	=	SMC_PBUS_VSENSE	MAKE_BASE=TRUE				
SMC_BMON_ISENSE	=	SMC_BMON_ISENSE	MAKE_BASE=TRUE				
SMC_CPU_HI_ISENSE	=	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE				
SMC_GPU_HI_ISENSE	=	SMC_GPU_HI_ISENSE	MAKE_BASE=TRUE				
SMC_OTHER_HI_ISENSE	=	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE				
TP_SMC_P10	=	TP_SMC_P10	MAKE_BASE=TRUE				
TP_SMC_P20	=	TP_SMC_P20	MAKE_BASE=TRUE				
TP_SMC_P24	=	TP_SMC_P24	MAKE_BASE=TRUE				
SMC_BMON_MUX_SEL	=	SMC_BMON_MUX_SEL	MAKE_BASE=TRUE				
TP_SMC_P41	=	TP_SMC_P41	MAKE_BASE=TRUE				
TP_SMC_P43	=	TP_SMC_P43	MAKE_BASE=TRUE				
TP_SMC_PF5	=	TP_SMC_PF5	MAKE_BASE=TRUE				
TP_SMC_RSTGATE_L	=	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE				







BATLOW# Isolation



PP3V42_G3H							
SMC_ONOFF_L	R5070	10K	5%	1/20W	MF	201	
G3_POWERON_L	R5072	10K	5%	1/20W	MF	201	
SMC_LID	R5071	100K	5%	1/20W	MF	201	
SMC_TX_L	R5073	10K	5%	1/20W	MF	201	
SMC_RX_L	R5074	100K	5%	1/20W	MF	201	
SMC_TMS	R5077	10K	5%	1/20W	MF	201	
SMC_TDO	R5078	10K	5%	1/20W	MF	201	
SMC_TDI	R5079	10K	5%	1/20W	MF	201	
SMC_TCK	R5080	10K	5%	1/20W	MF	201	
SMC_BIL_BUTTON_L	R5081	10K	5%	1/20W	MF	201	
SMC_BC_ACOK	R5087	470K	5%	1/20W	MF	201	
SMS_INT_L	R5093	10K	5%	1/20W	MF	201	
			NOSTUFF				
SMC_PA0_PU	R5091	100K	5%	1/20W	MF	201	
SMC_ADAPTER_EN	R5085	10K	5%	1/20W	MF	201	
SMC_CASE_OPEN	R5086	10K	5%	1/20W	MF	201	
SMC_PB4	R5088	10K	5%	1/20W	MF	201	
SMC_S4_WAKESRC_EN	R5090	100K	5%	1/20W	MF	201	
PP3V3_WLAN							
WIFI_EVENT_L	R5089	10K	5%	1/20W	MF	201	
PP3V42_G3H							
			NOSTUFF				
SMC_RUNTIME_SCI_L	R5094	100K	5%	1/20W	MF	201	

SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC Support

Apple Inc.

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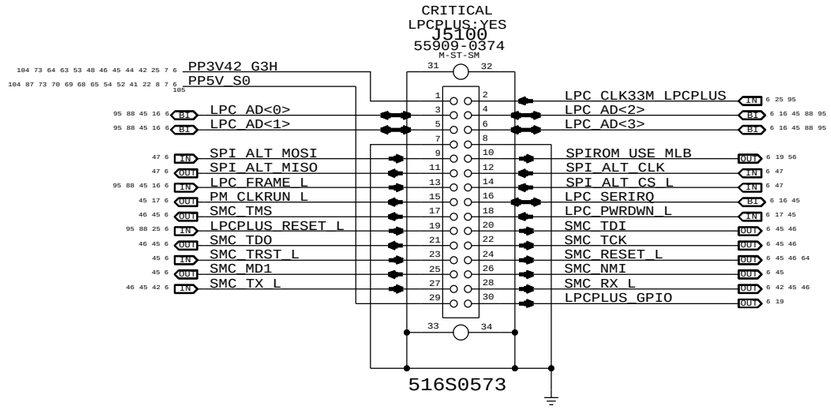
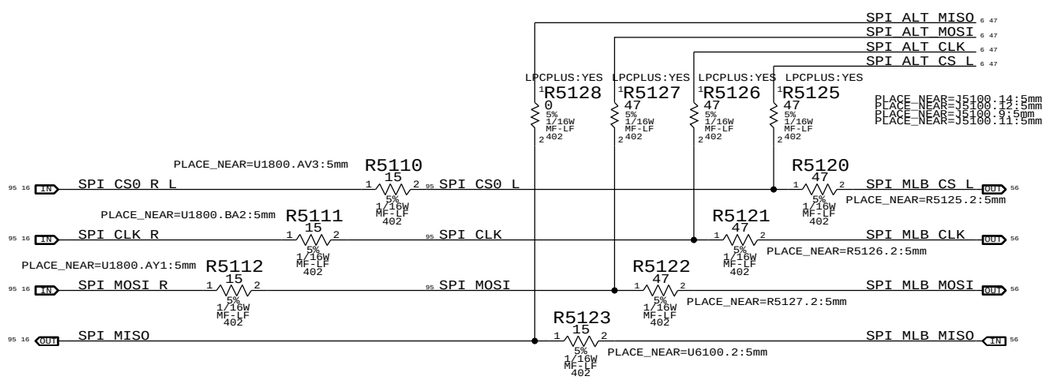
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K91_YUN SYNC_DATE=09/23/2010

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

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PCH SMBus "0" Connections

PP3V3_S0

PCH — U1800 (MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

VRef DACs — U2900 (Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control — U2901 (Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors — J2600 & J2650 (MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT — U9701 (WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SDRVI2C:SB
- R5237 0 5% 1/10W MF-LF 402
- R5236 0 5% 1/16W MF-LF 402

SO-DIMM "A" — J2900 (Write: 0xA0 Read: 0xA1)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B" — J3100 (Write: 0xA4 Read: 0xA5)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SATA Redriver — U4510 (Write: 0xB6 Read: 0xB7)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

ExpressCard Slot — J3500 (Address via ARP)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey — U6800 (Write: 0x72 Read: 0x73)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

DP SDRV "A" — U9310 (Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL (MAKE_BASE=TRUE)
- I2C_DPSDRVA_SDA (MAKE_BASE=TRUE)

PCH "SMLink 0" Connections

PP3V3_S0

PCH — U1800 (MASTER)
- SML_PCH_0_CLK (MAKE_BASE=TRUE)
- SML_PCH_0_DATA (MAKE_BASE=TRUE)

- R5210 8.2K 5% 1/10W MF-LF 402
- R5211 8.2K 5% 1/10W MF-LF 402

PCH "SMLink 1" Connections

PP3V3_S0

PCH — U1800 (Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK (MAKE_BASE=TRUE)
- SML_PCH_1_DATA (MAKE_BASE=TRUE)

NO STUFF
- R5220 8.2K 5% 1/10W MF-LF 402
- R5221 8.2K 5% 1/10W MF-LF 402
- R5223 0 5% 1/10W MF-LF 402
- R5222 0 5% 1/10W MF-LF 402

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

SMC — U4900 (MASTER)
- SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

- R5250 4.7K 5% 1/16W MF-LF 402
- R5251 4.7K 5% 1/16W MF-LF 402

GPU Temp (Ext) — EMC1414: U5550 (Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int) — Whistler: U8000 (Write: 0x82 Read: 0x83)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

X19 Temp — J3401 (Write: 0x90 Read: 0x91)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

SMC — U4900 (MASTER)
- SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

- R5270 1K 5% 1/16W MF-LF 402
- R5271 1K 5% 1/16W MF-LF 402

Trackpad — J5800 (Write: 0x90 Read: 0x91)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

J3401 ALS (Write: 0x72 Read: 0x73)

Lid Angle detect, SMS (Write: 0x32 Read: 0x33)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMS — U5920 (Write: 0x30 Read: 0x31)
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

SMC — U4900 (MASTER)
- SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

- R5260 4.7K 5% 1/16W MF-LF 402
- R5261 4.7K 5% 1/16W MF-LF 402

CPU Temp — EMC1414: U5570 (Write: 0x98 Read: 0x99)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

T29 Temp — EMC1412: U5520 (Write: 0x90 Read: 0x91)
- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

SMC — U4900 (MASTER)
- SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

- R5280 2.0K 5% 1/16W MF-LF 402
- R5281 2.0K 5% 1/16W MF-LF 402

Battery Charger — ISL6258 - U7000 (Write: 0x12 Read: 0x13)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery — J6955 (See Table)
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x92 Read: 0x93)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S5

SMC — U4900 (MASTER)
- SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

- R5290 4.7K 5% 1/16W MF-LF 402
- R5291 4.7K 5% 1/16W MF-LF 402

Sensor ADC A — UD100 (Write: 0x10 Read: 0x11)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

Sensor ADC B — UD210 (Write: 0x32 Read: 0x33)
- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

T29 SMBus Connections

PP3V3_S0

T29 — U3600 (MASTER)
- I2C_T29_SCL (MAKE_BASE=TRUE)
- I2C_T29_SDA (MAKE_BASE=TRUE)

- R5230 4.7K 5% 1/16W MF-LF 402
- R5231 4.7K 5% 1/16W MF-LF 402

T29 PortA MCU — U9330 (Write: 0x26 Read: 0x27)
- I2C_T29_SCL
- I2C_T29_SDA

SDRVI2C:MCU
- R5234 0 5% 1/16W MF-LF 402
- R5235 0 5% 1/16W MF-LF 402

DP SDRV "A" — U9310 (Write: 0x94 Read: 0x95)
- I2C_DPSDRVA_SCL (MAKE_BASE=TRUE)
- I2C_DPSDRVA_SDA (MAKE_BASE=TRUE)

SYNC_MASTER=K17_MLB
SYNC_DATE=04/26/2010

PAGE TITLE
K92 SMBus Connections

Apple Inc.

DRAWING NUMBER — SIZE: D
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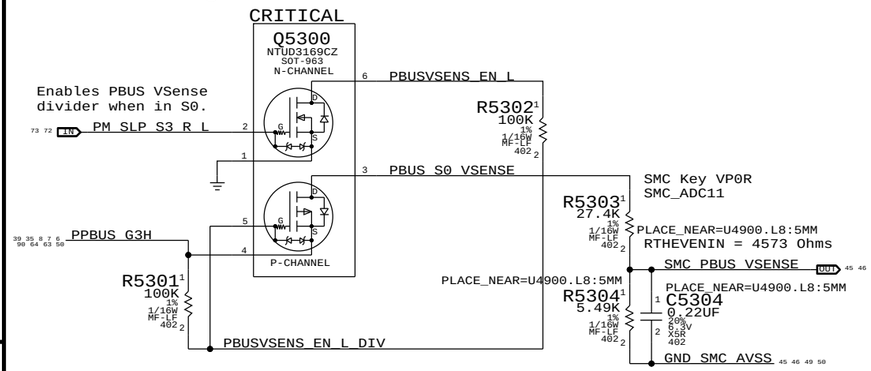
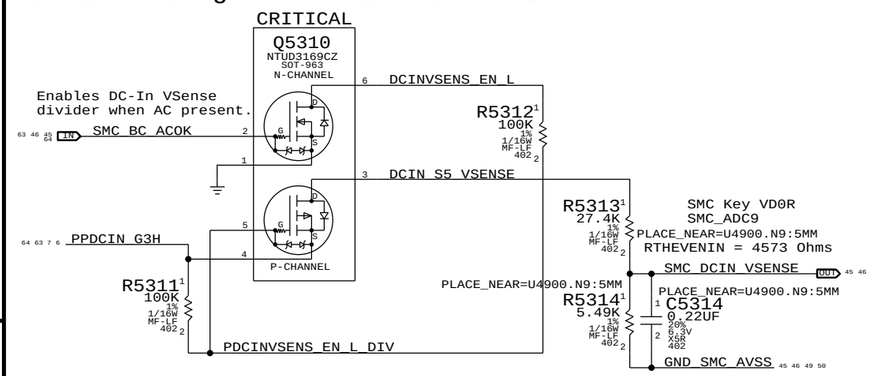
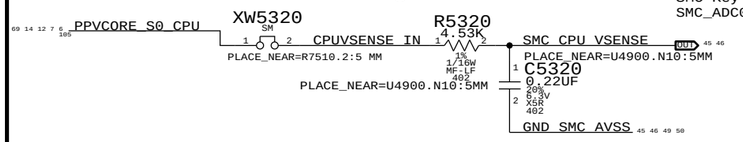
PBUS Voltage Sense Enable & Filter



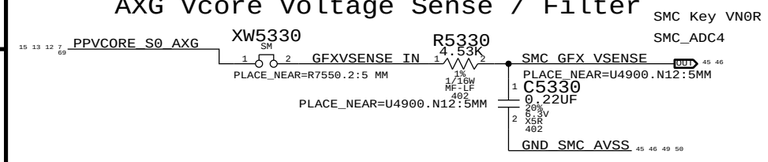
DC-In Voltage Sense Enable & Filter



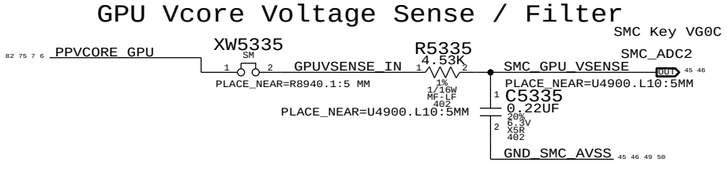
CPU Vcore Voltage Sense / Filter



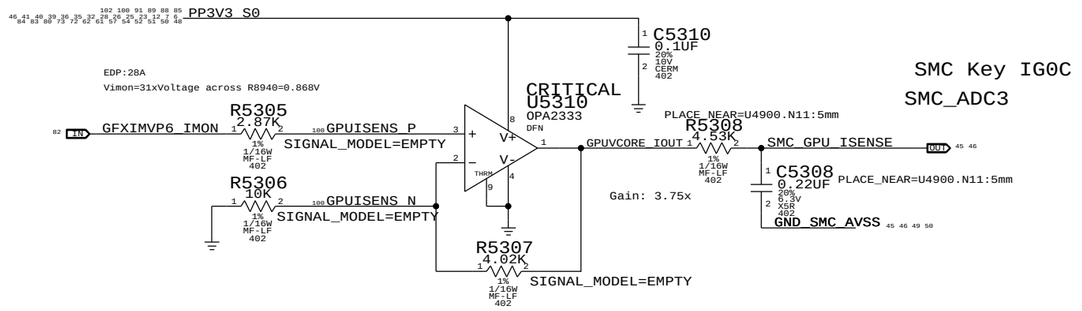
AXG Vcore Voltage Sense / Filter



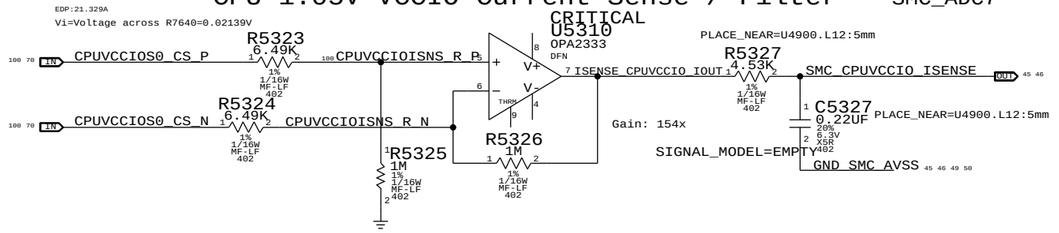
GPU Vcore Voltage Sense / Filter



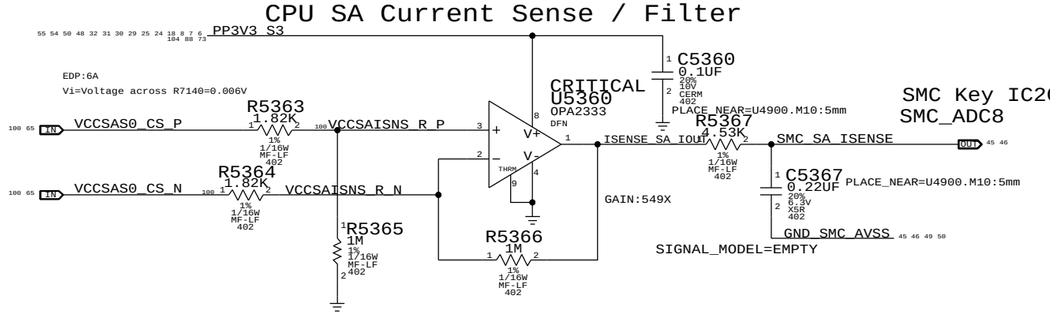
GPU VCore Load Side Current Sense / Filter



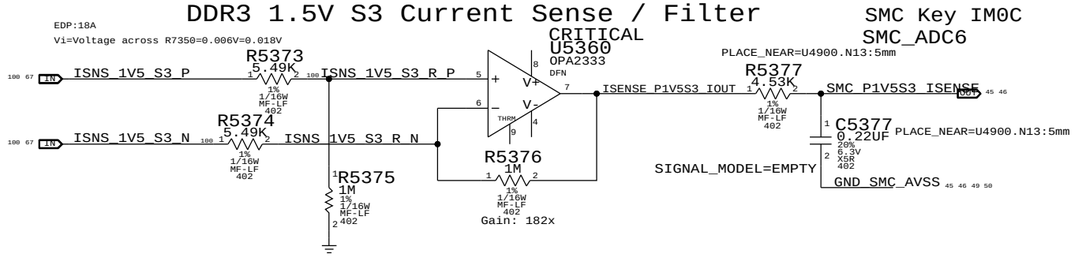
CPU 1.05V VCCIO Current Sense / Filter



CPU SA Current Sense / Filter



DDR3 1.5V S3 Current Sense / Filter



SYNC_MASTER=K92_DINESH SYNC_DATE=09/24/2010

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER | SIZE: D

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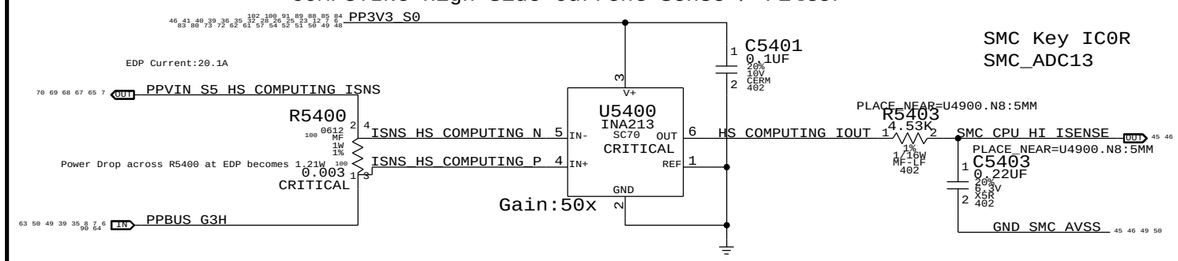
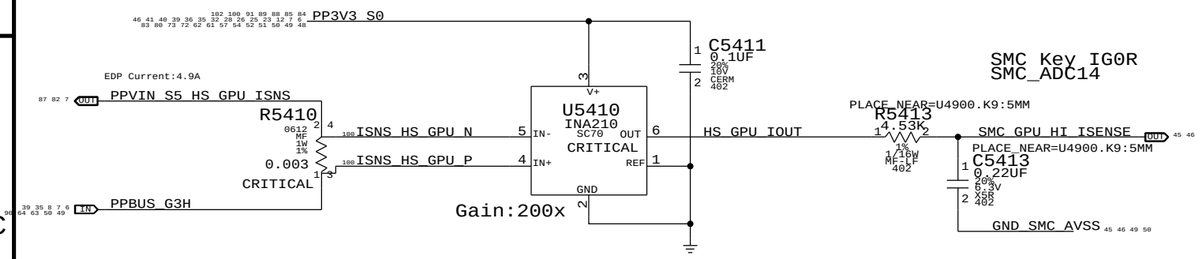
Rsense value and INA gain need to be scrubbed!!

COMPUTING High Side Current Sense / Filter



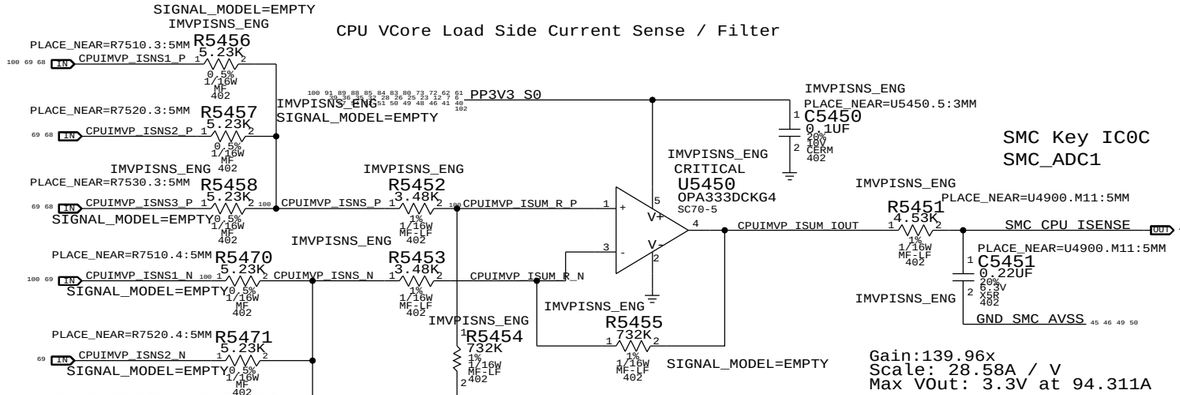
SMC Key IC0R
SMC_ADC13

GRAPHICS High Side Current Sense / Filter



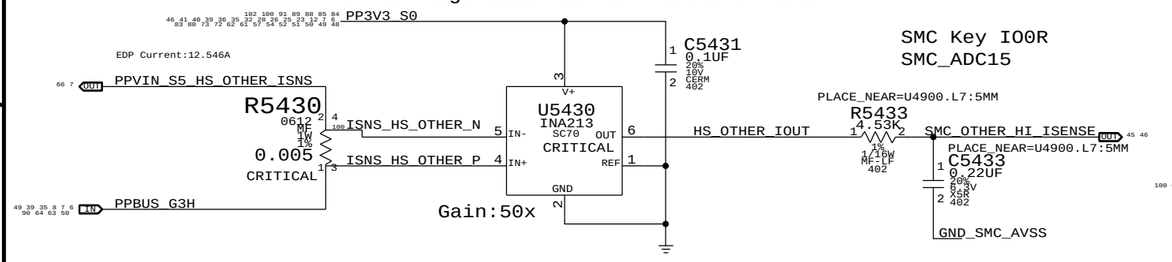
SMC Key IG0R
SMC_ADC14

CPU VCore Load Side Current Sense / Filter



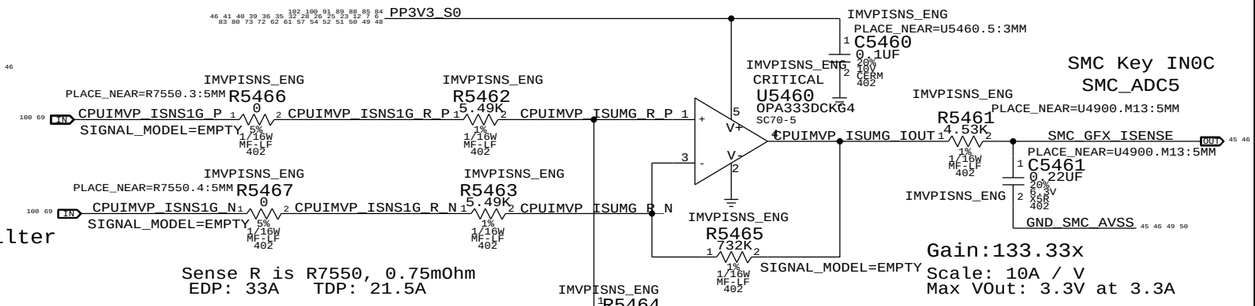
SMC Key IC0C
SMC_ADC1

OTHER High Side Current Sense / Filter



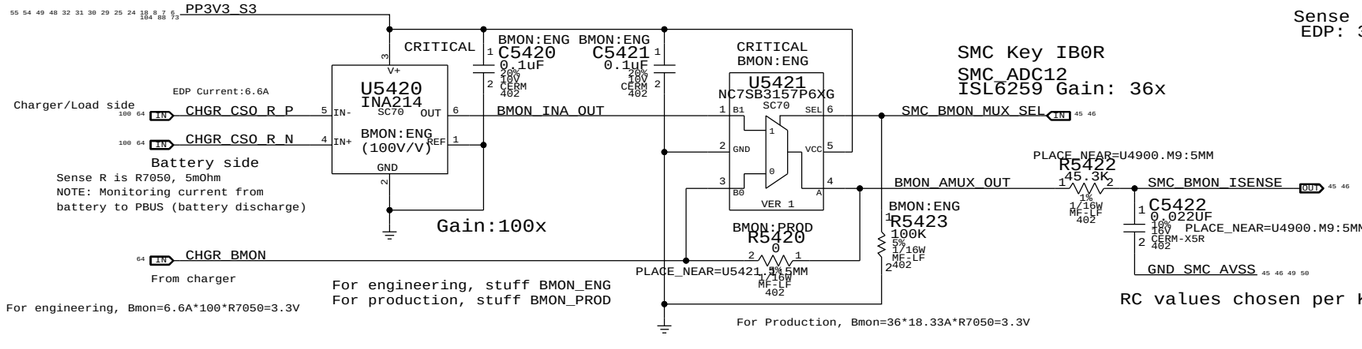
SMC Key IO0R
SMC_ADC15

GFX/IG VCore Load Side Current Sense / Filter



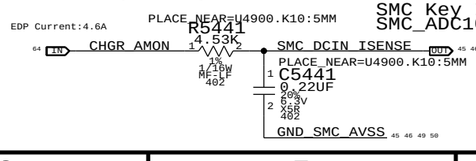
SMC Key IN0C
SMC_ADC5

CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter



SMC Key IB0R
SMC_ADC12
ISL6259 Gain: 36x

DC-IN (AMON) Current Sense Filter



SMC Key ID0R
SMC_ADC10

SYNC_MASTER=K92_DINESH	SYNC_DATE=10/29/2016
PAGE TITLE: High Side and CPU/AXG Current Sensing	
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	REVISION:
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	PAGE: 54 OF 132
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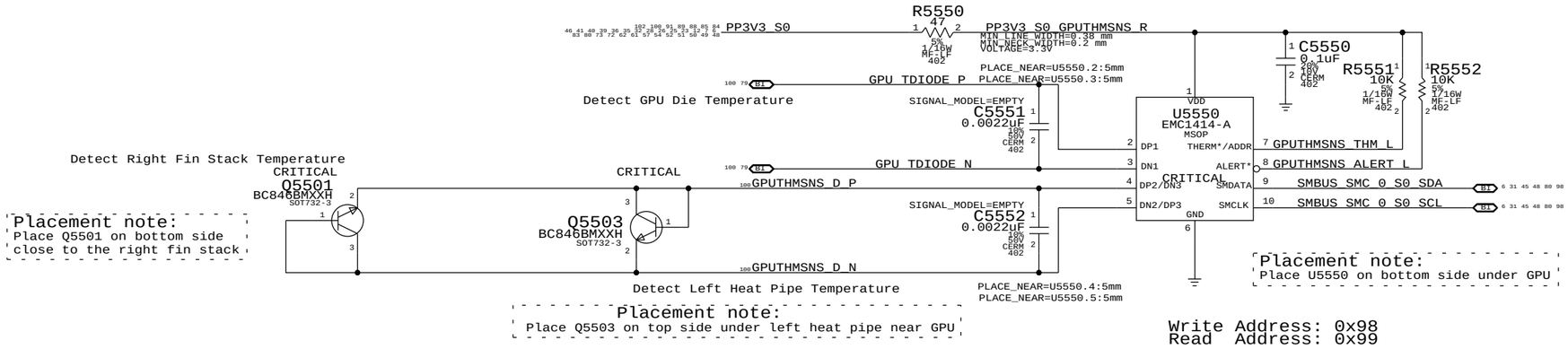
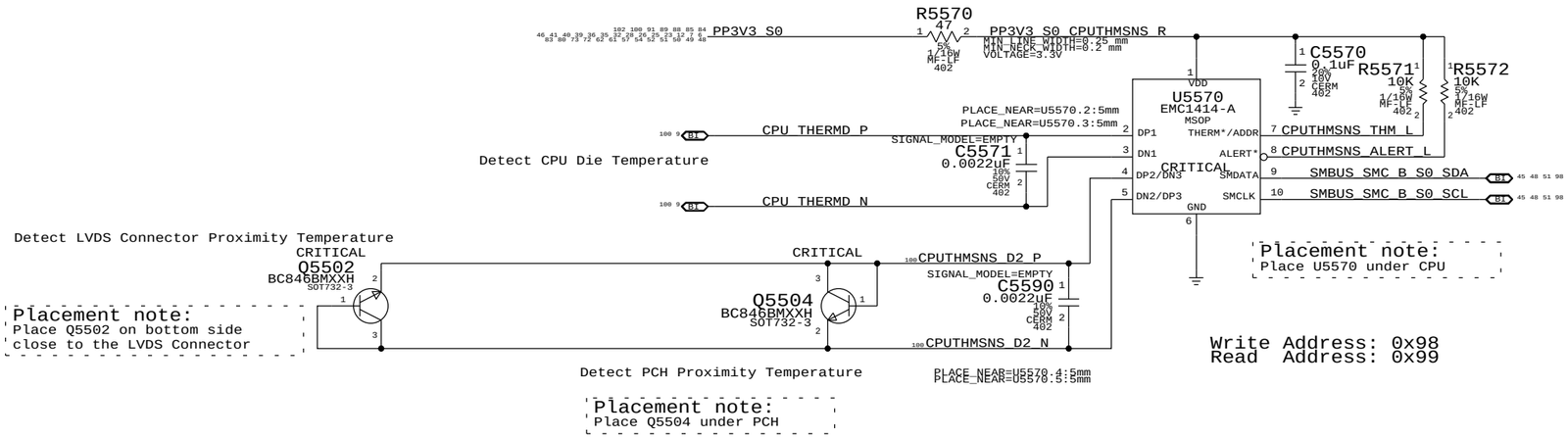
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

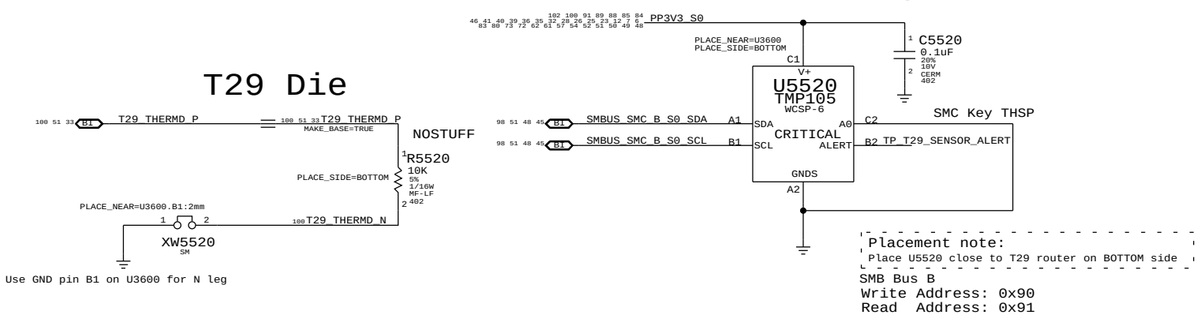


CPU Proximity/CPU Die/PCH Proximity/LVDS Connector Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

T29 Proximity



SYNC_MASTER=K92_DINESH SYNC_DATE=09/24/2010

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER | SIZE: D

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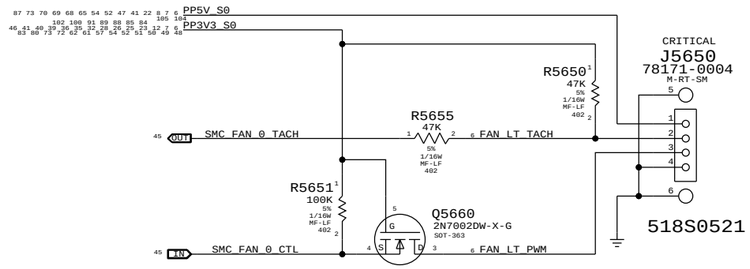
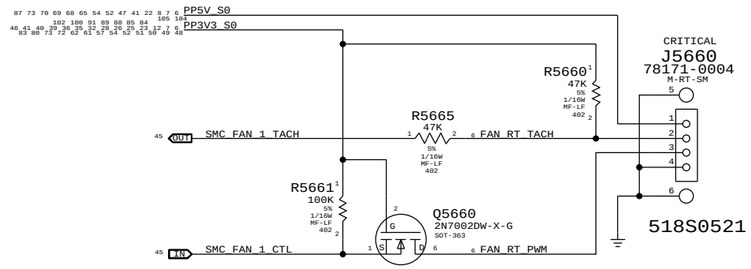
Left Fan



Right Fan



SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: SIZE D

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PAGE: 56 OF 132

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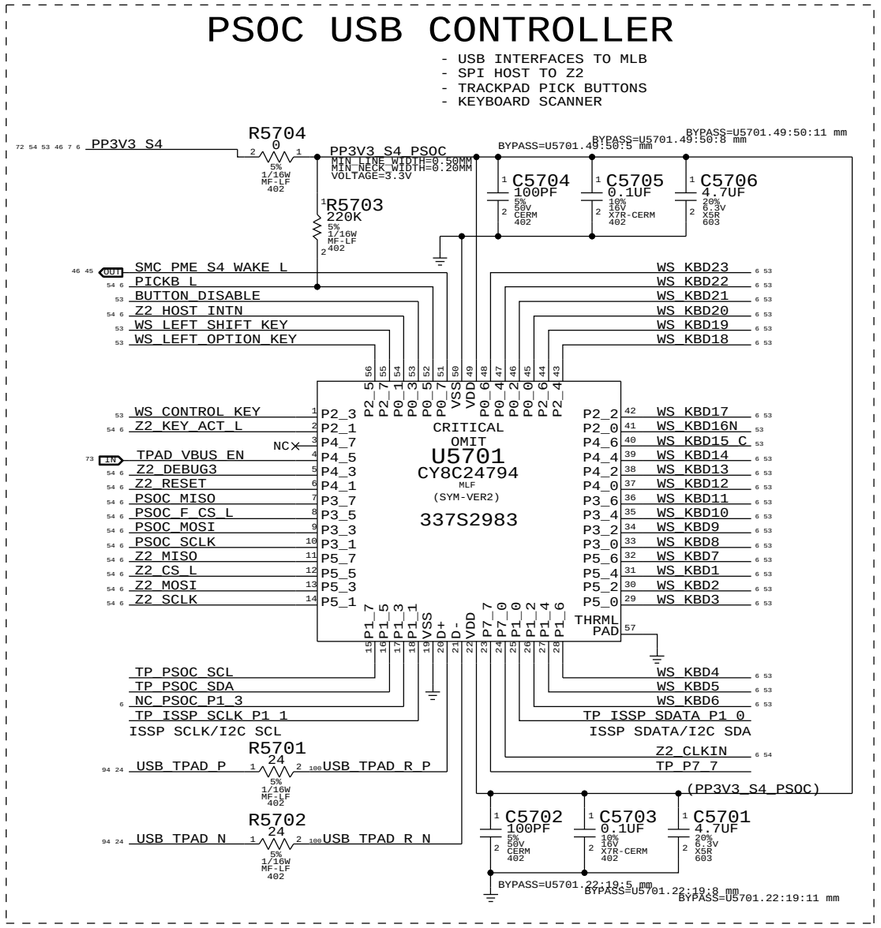
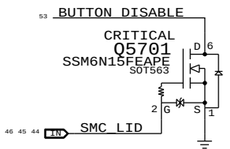
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

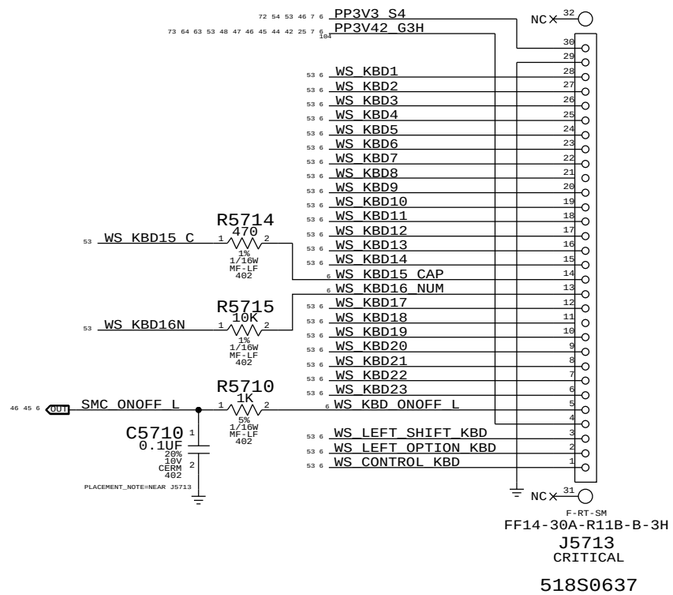


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

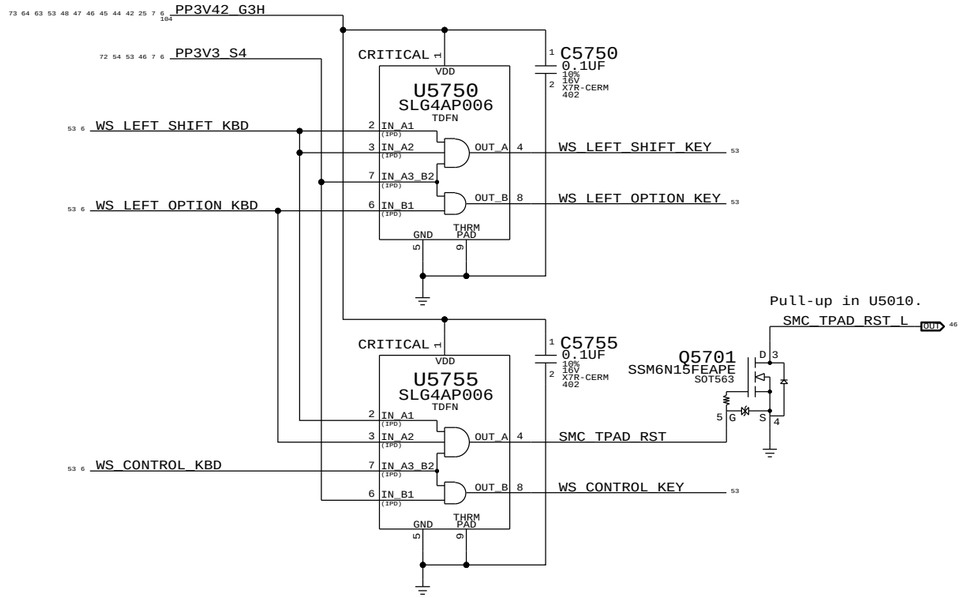
Keyboard Connector



518S0637

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC_MASTER=K92_ERIC	SYNC_DATE=10/11/2010
PAGE TITLE	WELLSPRING 1
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
	BRANCH:
	PAGE: 57 OF 132
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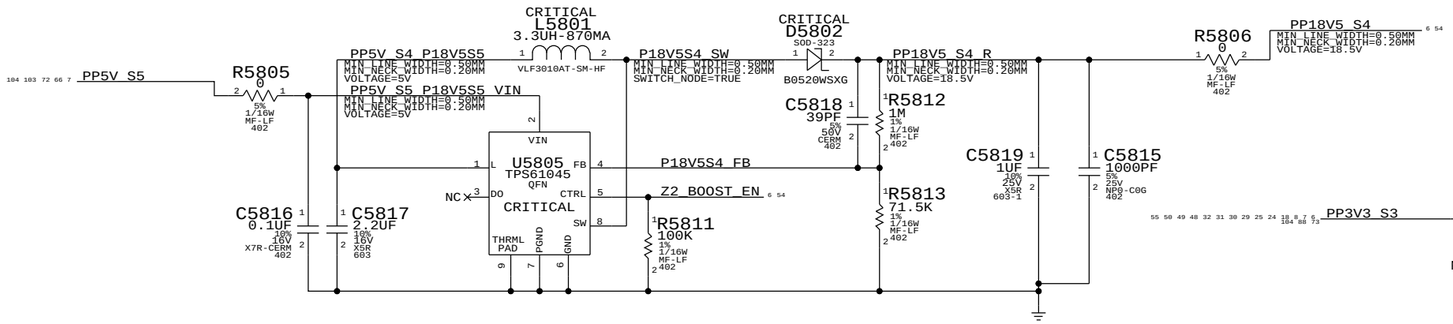
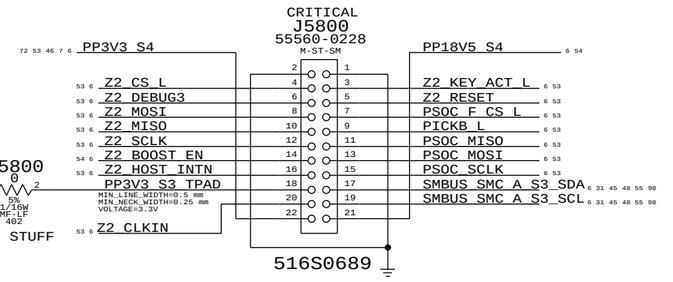
BOOSTER +18.5VDC FOR SENSORS

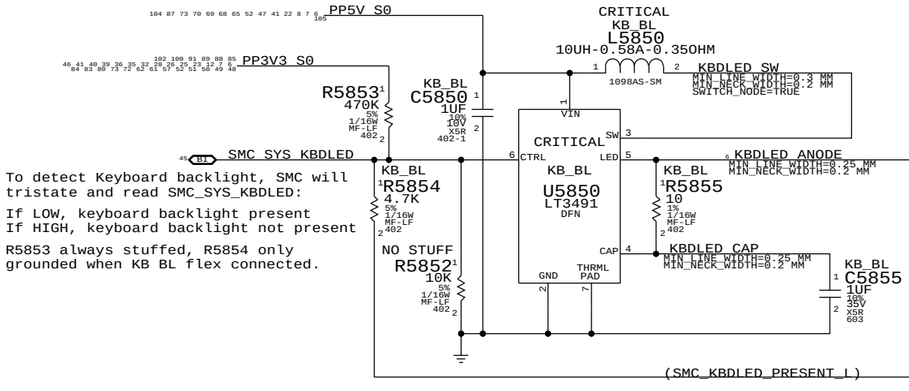
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

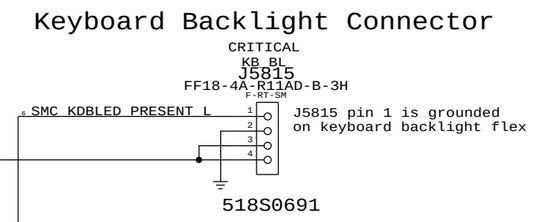


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



SYNC_MASTER=K92_ERIC SYNC_DATE=07/27/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER | SIZE: D

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PAGE: 58 OF 132

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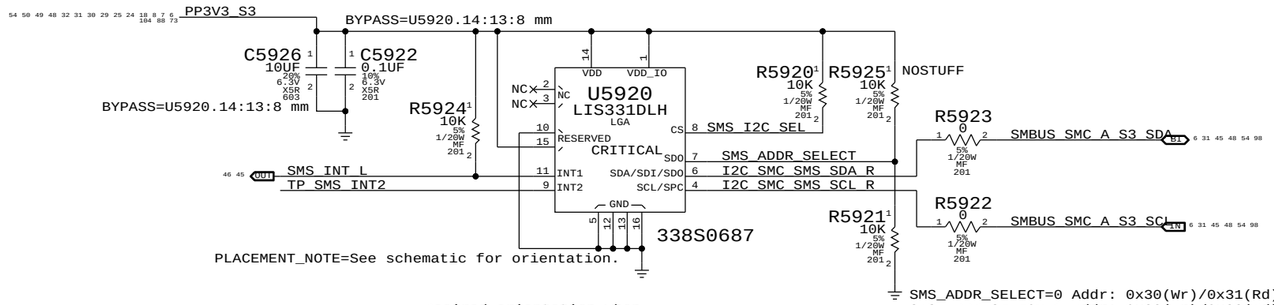
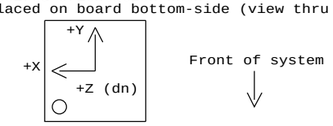


Desired orientation when
placed on board bottom-side (view thru top):



Circle indicates pin 1 location when placed
in correct orientation

SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

SYNC_MASTER=K92_DINESH SYNC_DATE=06/02/2010

PAGE TITLE
Digital Accelerometer

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
BRANCH
PAGE 59 OF 132
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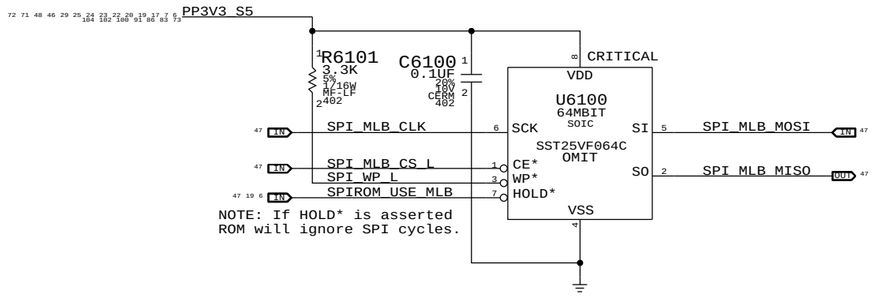

SYNC_MASTER=K92_BEN SYNC_DATE=05/27/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

SIZE D

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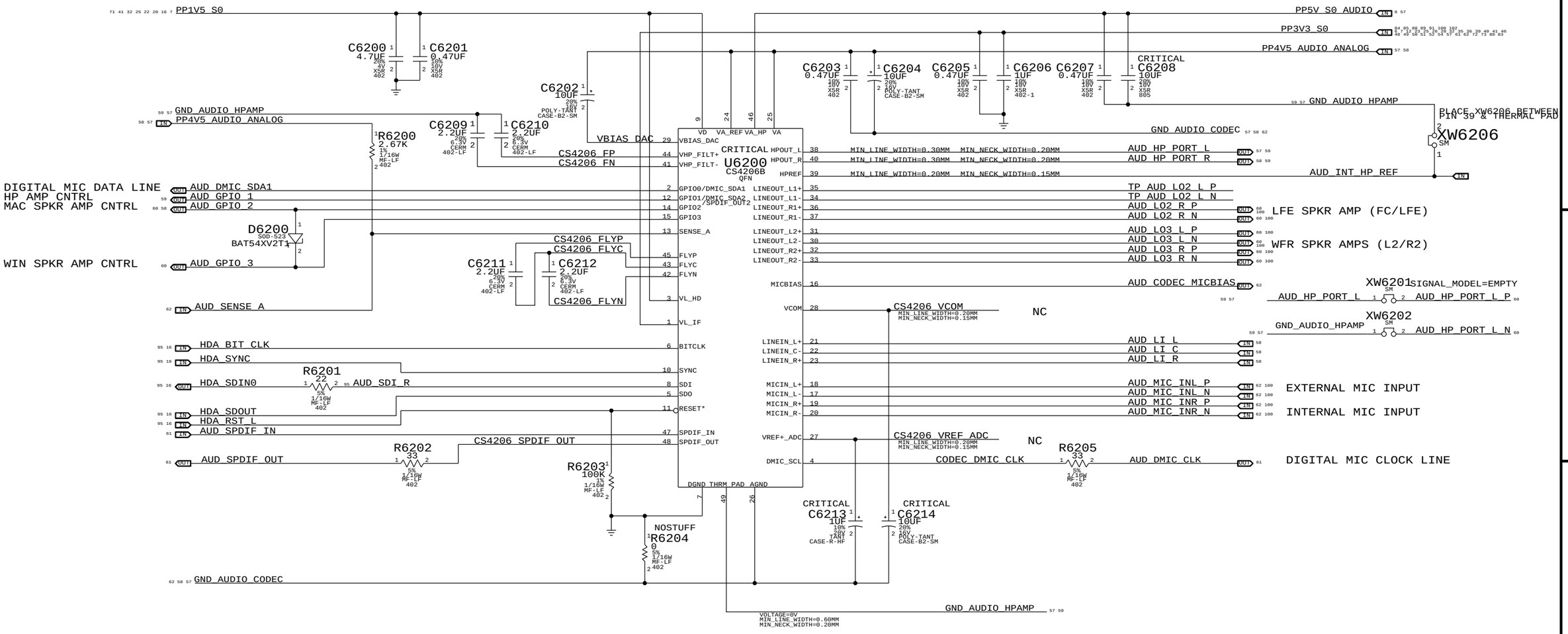
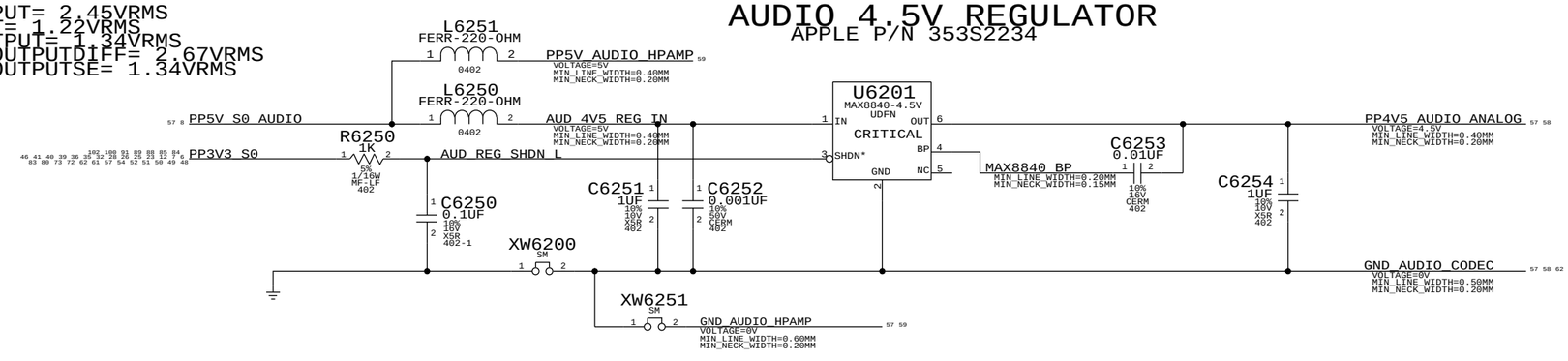
AUDIO CODEC
APPLE P/N 353S3199



DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR
APPLE P/N 353S2234



SYNC_MASTER=K92_KAVITHA	SYNC_DATE=07/30/2010
PAGE TITLE	AUDIO:CODEC
Apple Inc.	DRAWING NUMBER: SIZE: D
	REVISION:
	BRANCH:
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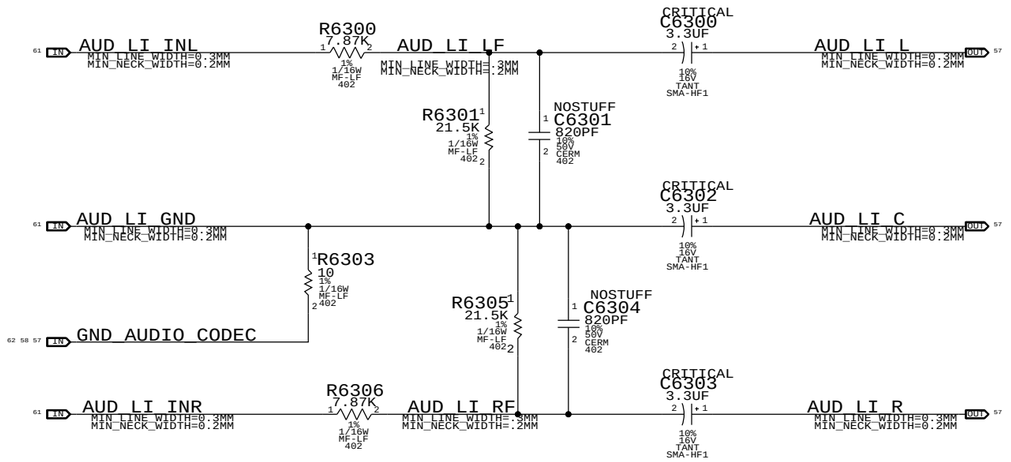
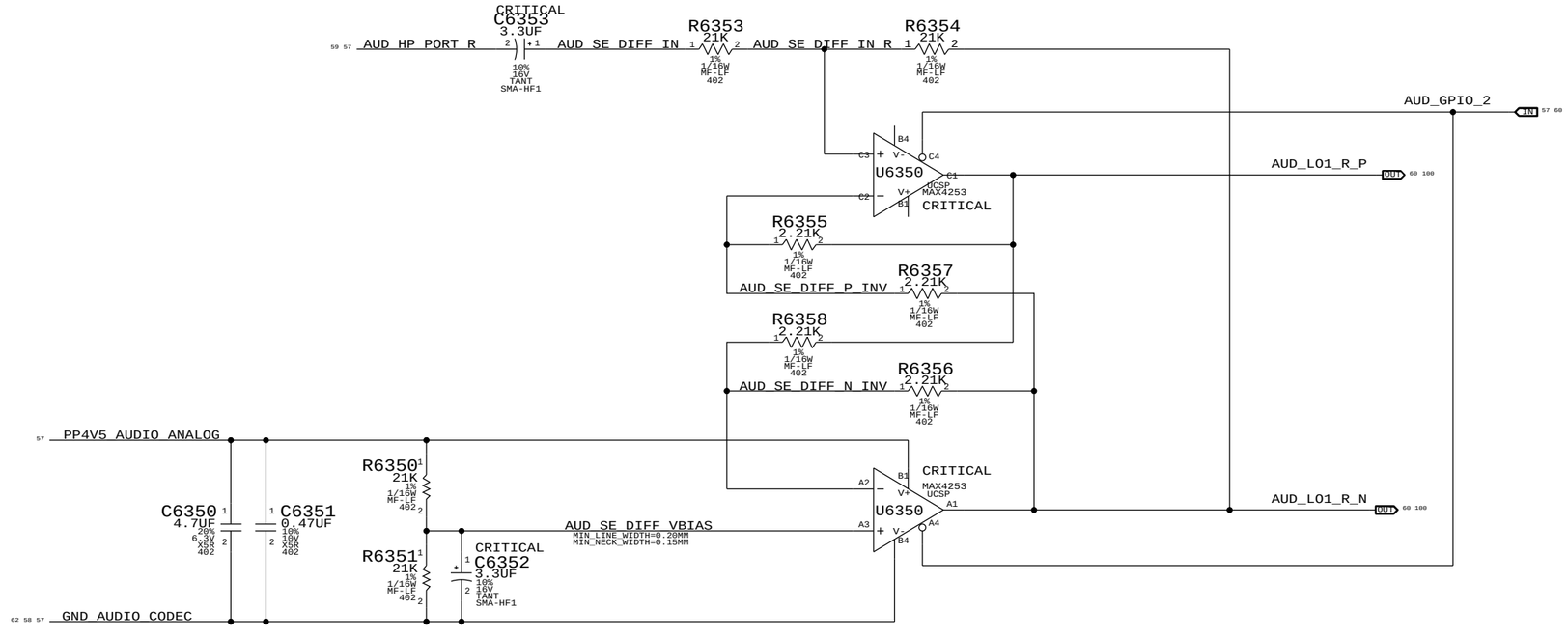
	SHEET: 57 OF 105

CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SE-TO-DIFF CONVERTER



SYNC_MASTER=K92_AUDIO	SYNC_DATE=06/16/2010
PAGE TITLE: AUDIO: LINE IN	
Apple Inc.	DRAWING NUMBER / SIZE: D
	REVISION
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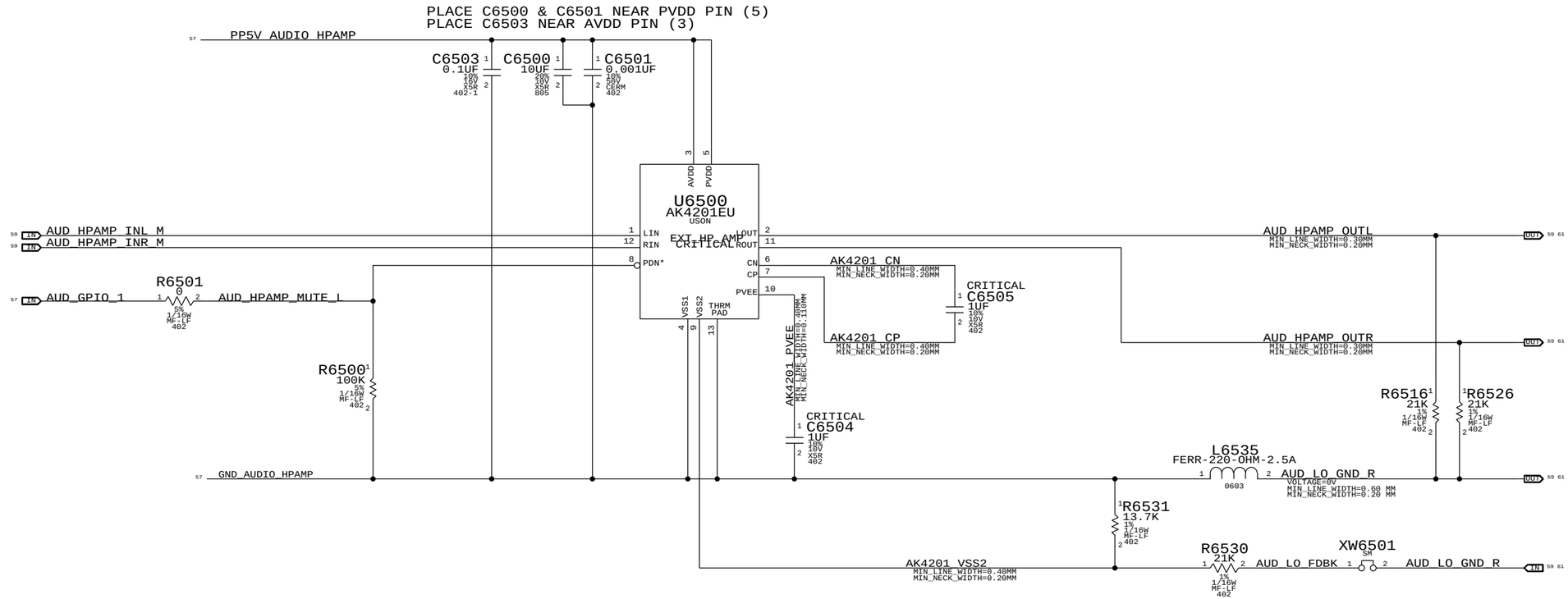
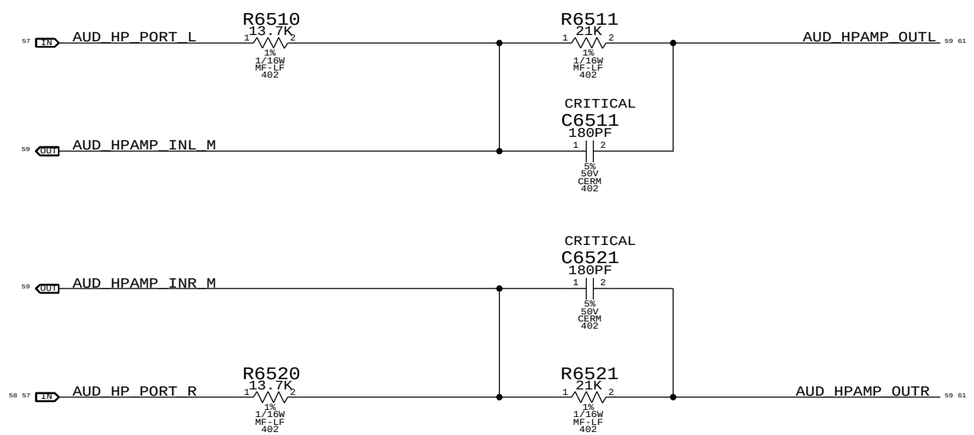
	PAGE: 63 OF 132
	SHEET: 58 OF 105

HEADPHONE AMPLIFIER (AK4201)
APN:353S2347
VOLTAGE GAIN:1.53



1ST ORDER DAC FILTER
LP:42.10 KHZ



SYNC_MASTER=K92_KAVITHA SYNC_DATE=10/22/2010

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

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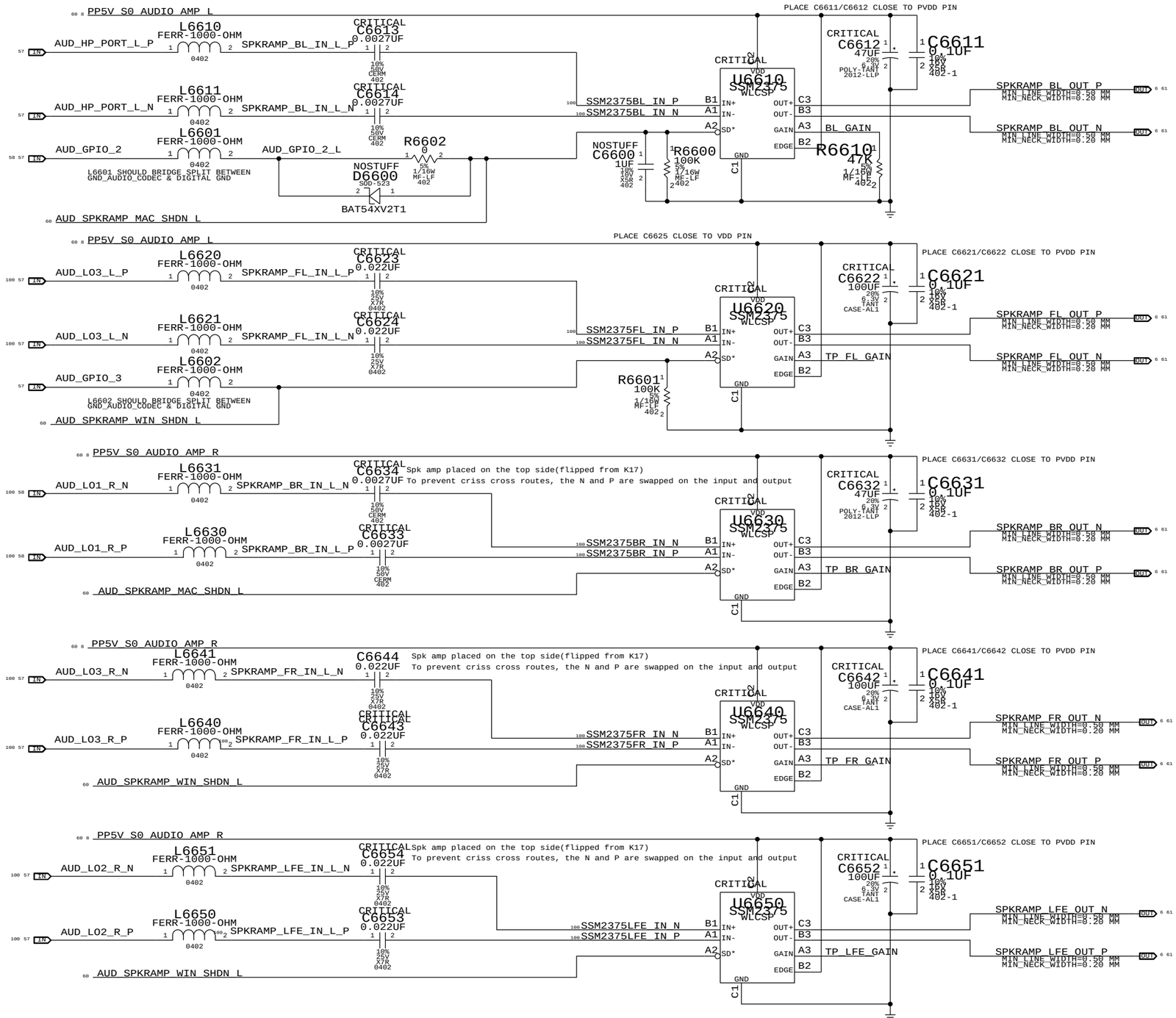
5X MONO SPEAKER AMPLIFIERS (SSM2375)

APN: 353S2958
GAIN = +3 DB (BR, FL, FR, LFE), +9 DB (BL)

FC (SPEAKERS BL/BR) = ~737 HZ
FC (SPEAKERS FL/FR/LFE) = ~90 HZ



SYNC_MASTER=K92_KAVITHA SYNC_DATE=10/22/2010

PAGE TITLE: AUDIO:SPEAKER AMP

Apple Inc.

DRAWING NUMBER | SIZE: D
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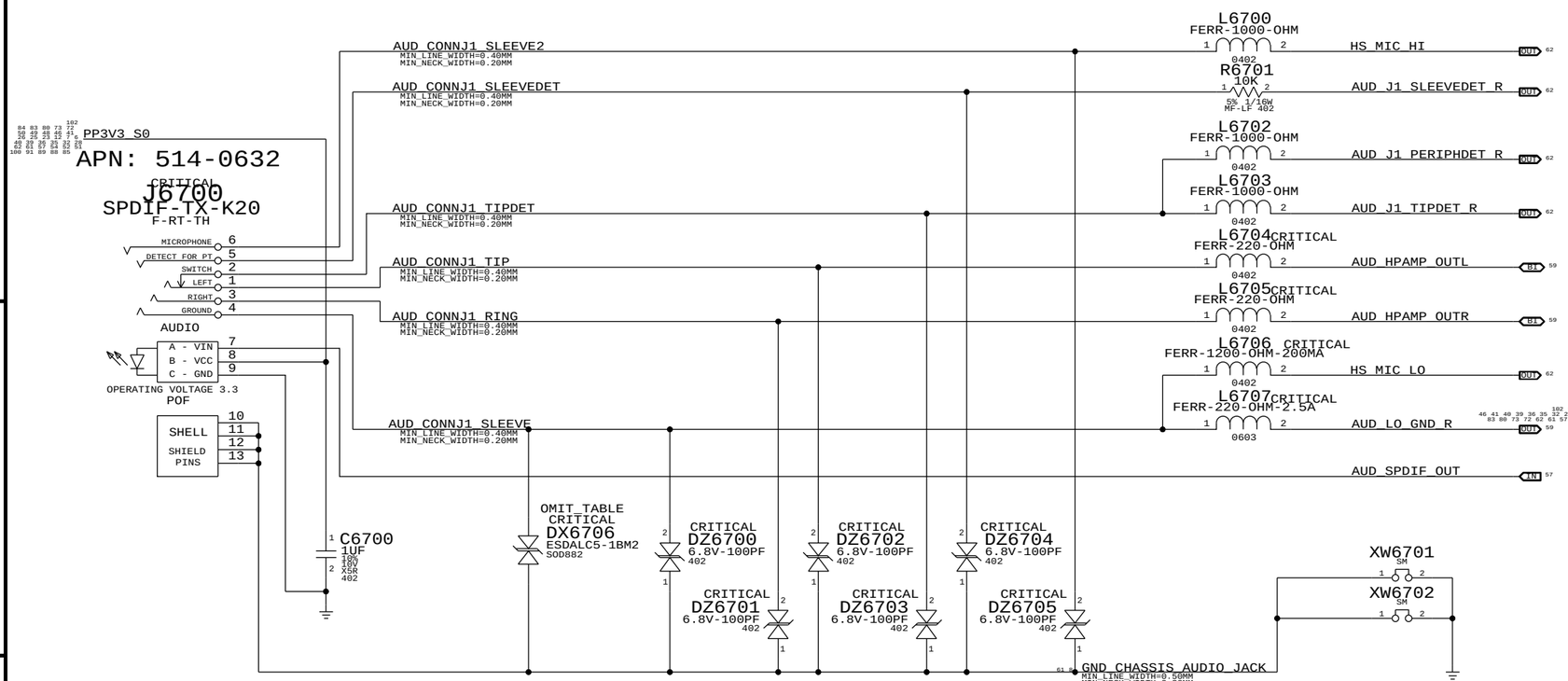
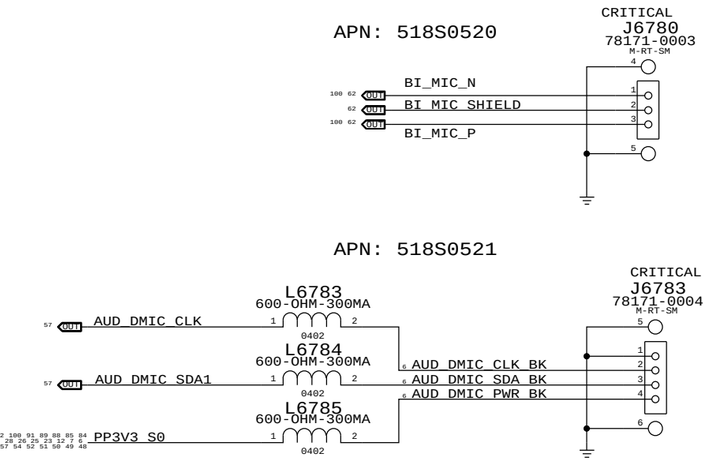
AUDIO JACK 1 LO/HP JACK, SPDIF TX

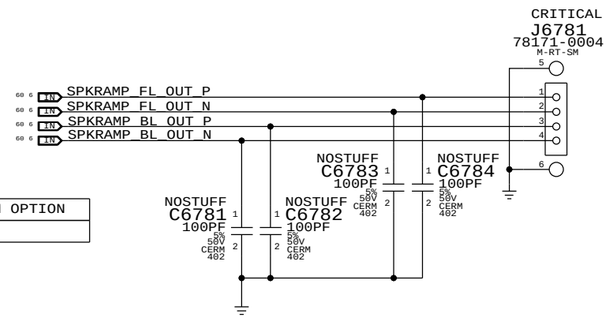


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S0112	1	EMC supressor	DX6706		

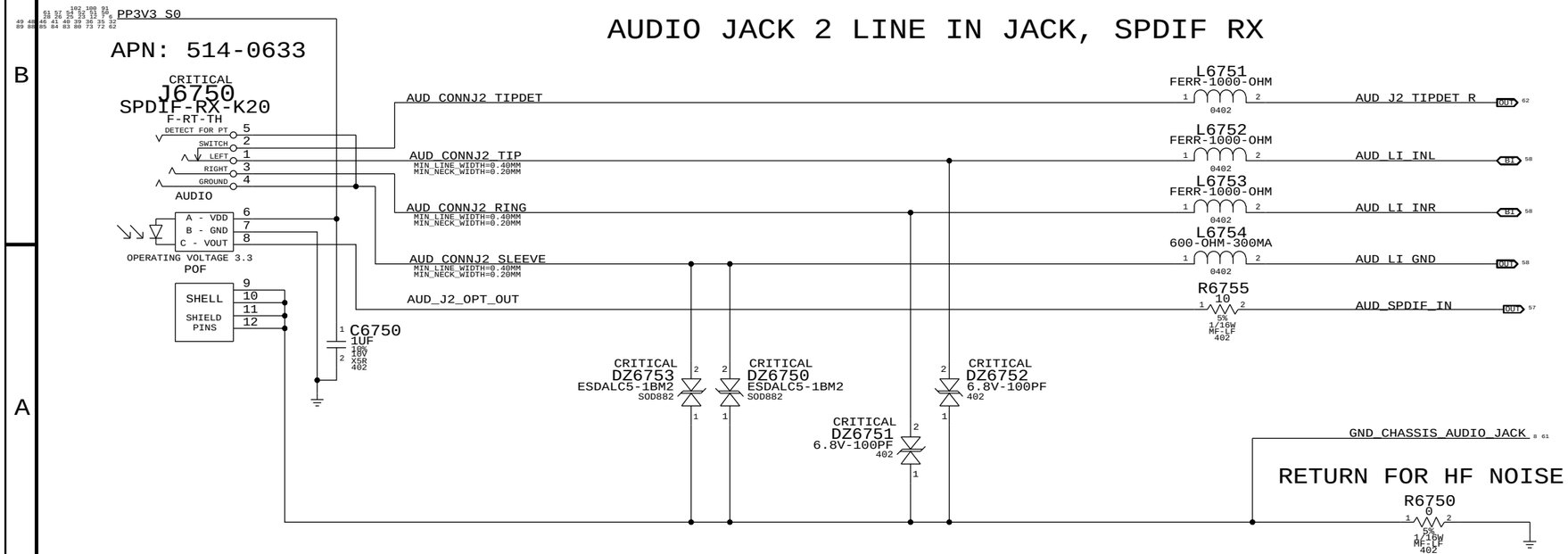
MIC CONNECTORS: single anlg mic + 1 dig mic



SPEAKER CONNECTORS
APN: 518S0521



AUDIO JACK 2 LINE IN JACK, SPDIF RX



SYNC_MASTER=K92_KAVITHA	SYNC_DATE=11/02/2010
PAGE TITLE: AUDIO: JACKS	
Apple Inc.	DRAWING NUMBER: — SIZE: D
	REVISION: —
	BRANCH: —
	PAGE: 67 OF 132
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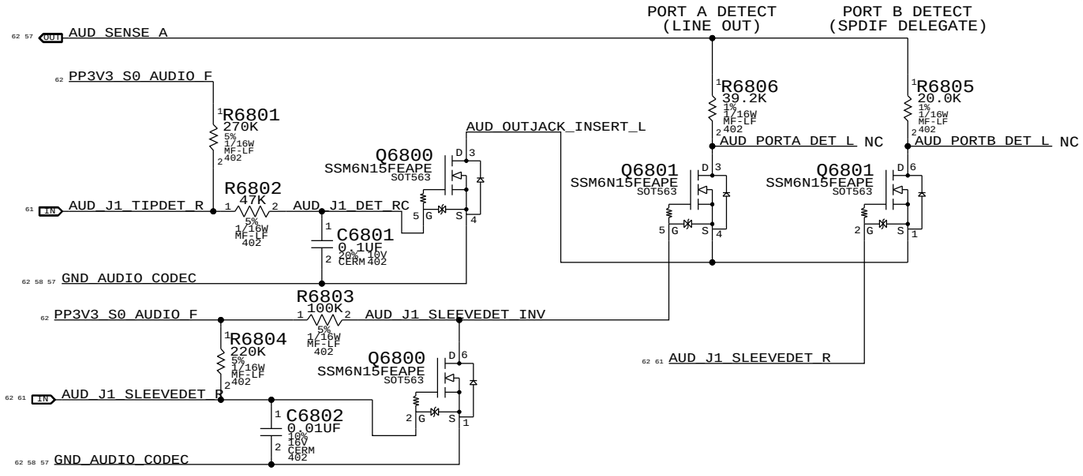
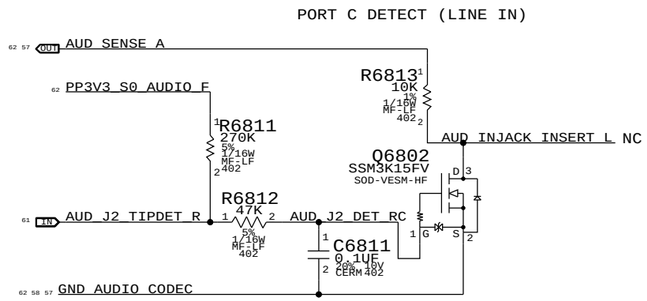
CODEC OUTPUT SIGNAL PATHS

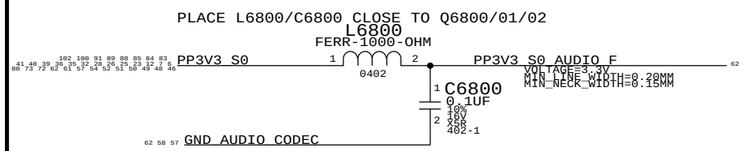
FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC OS SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	N/A	0X09 (A)
SPEAKERS BL/BR	0X02 (2)	0X02 (2)	0X09 (9,V23)	GPIO_2	N/A	N/A
SPEAKERS FL/FR	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_2	GPIO_3	N/A
SPEAKER LFE	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (B)

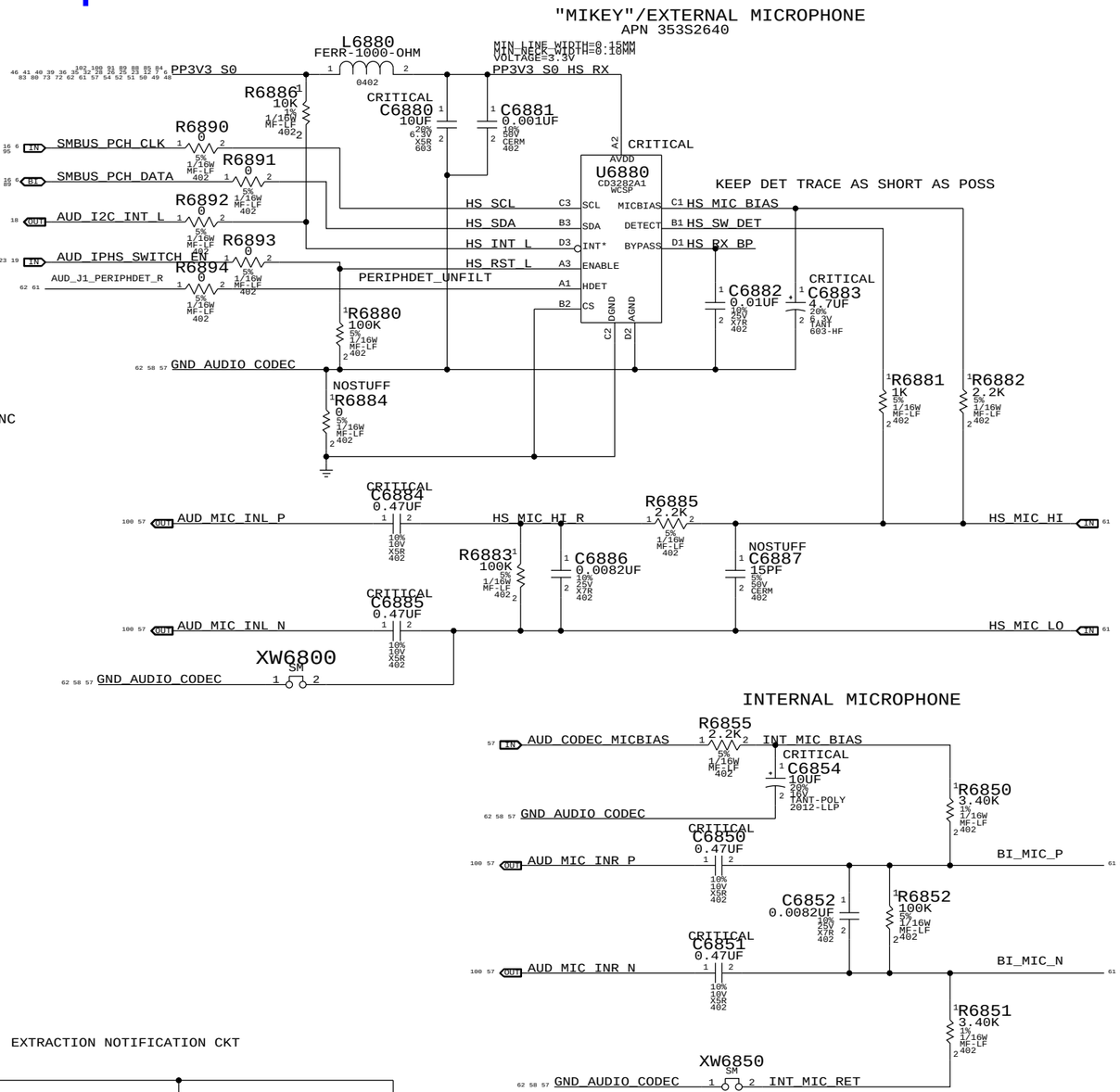
CODEC INPUT SIGNAL PATHS

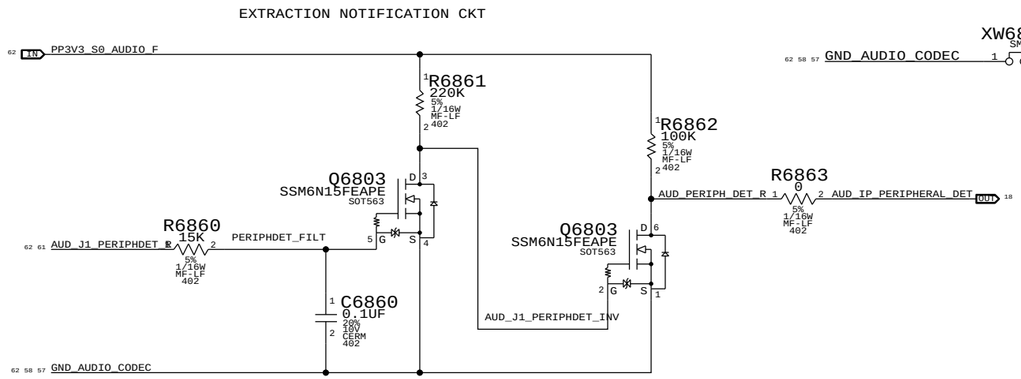
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0D (13,B,RIGHT)	MICBIAS (80%)	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY











SYNC MASTER=K92 KAVITHA SYNC DATE=11/22/2010

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER — SIZE D

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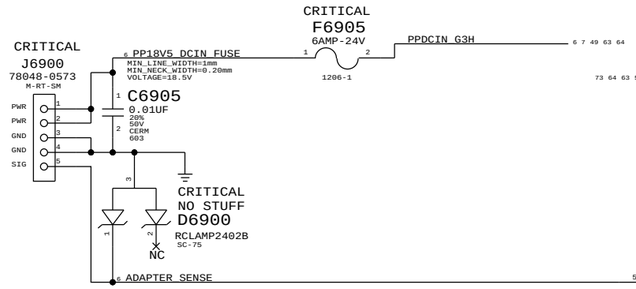
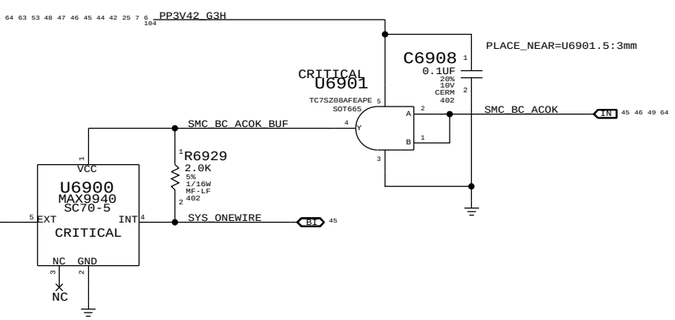
MagSafe DC Power Jack

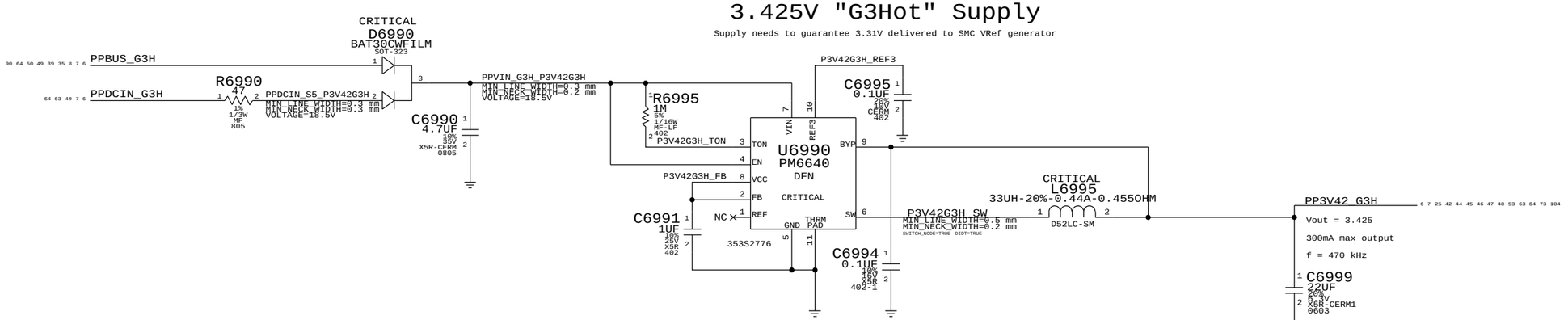


1-Wire OverVoltage & ESD Protection



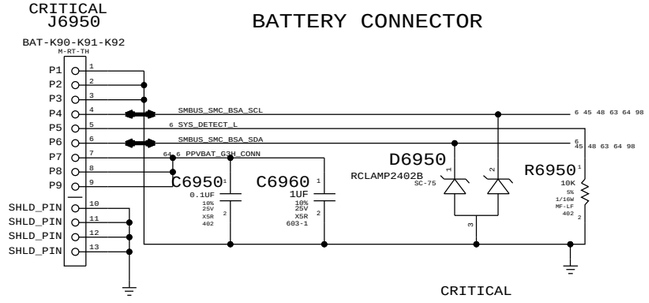
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



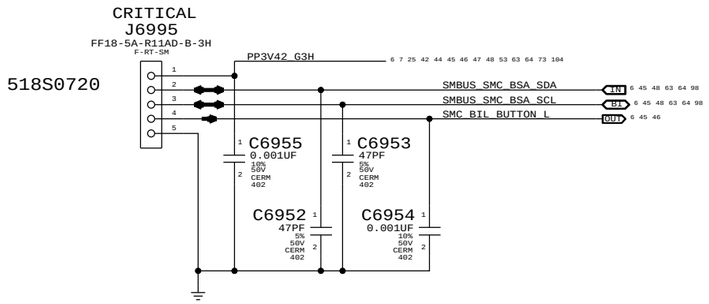
518-0375

BATTERY CONNECTOR



BIL Connector

518S0720



SYNC_MASTER=K92_CHANG SYNC_DATE=06/28/2010

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

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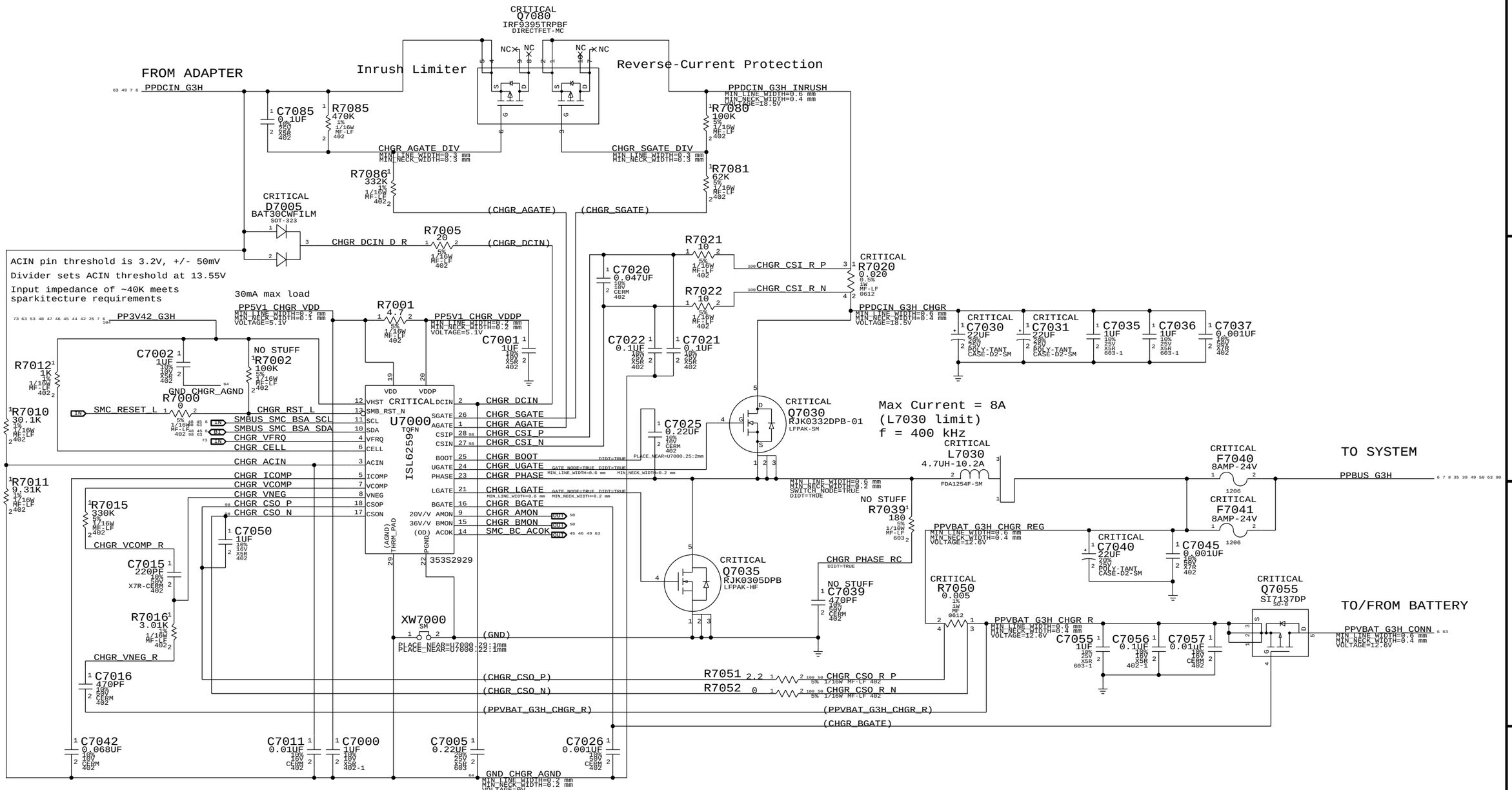
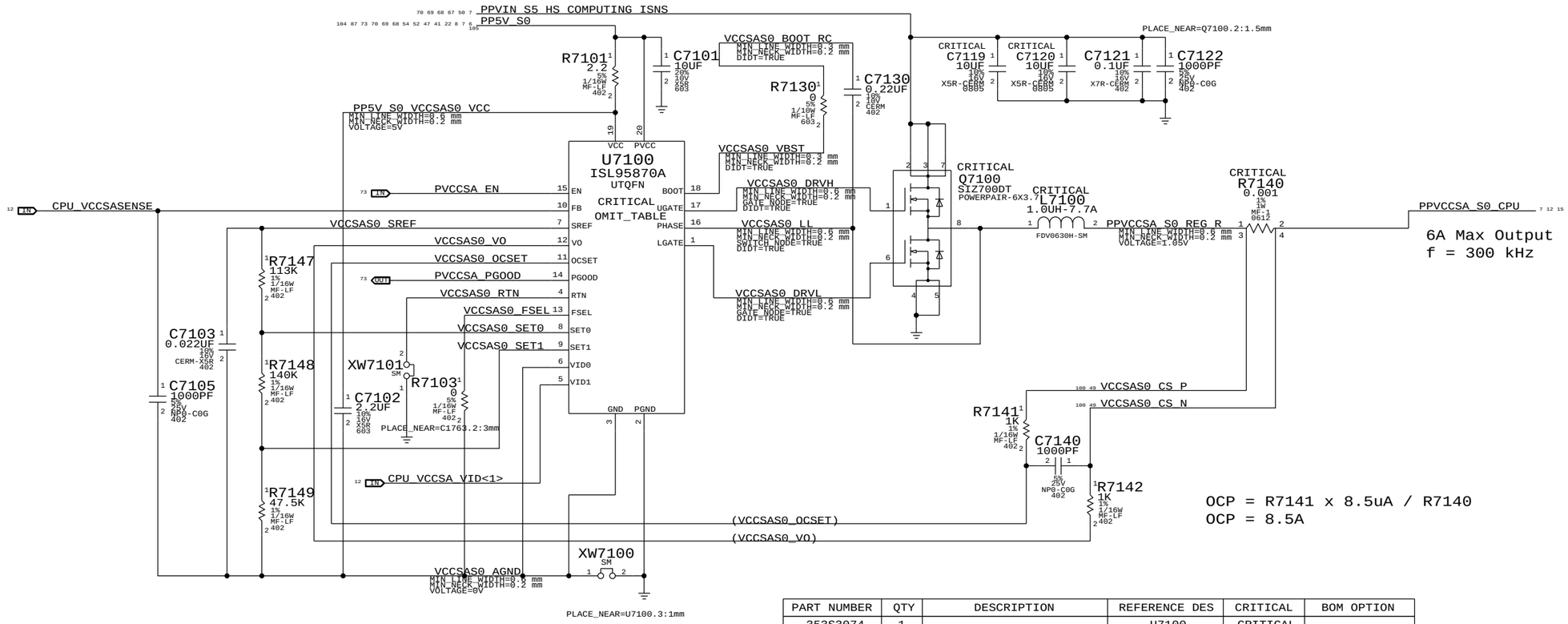


SYNC_MASTER=K91_CHANG	SYNC_DATE=07/21/2016
PAGE TITLE: PBus Supply & Battery Charger	
Apple Inc.	DRAWING NUMBER: SIZE D
	REVISION:
	BRANCH:
	PAGE: 70 OF 132
	SHEET: 64 OF 105



VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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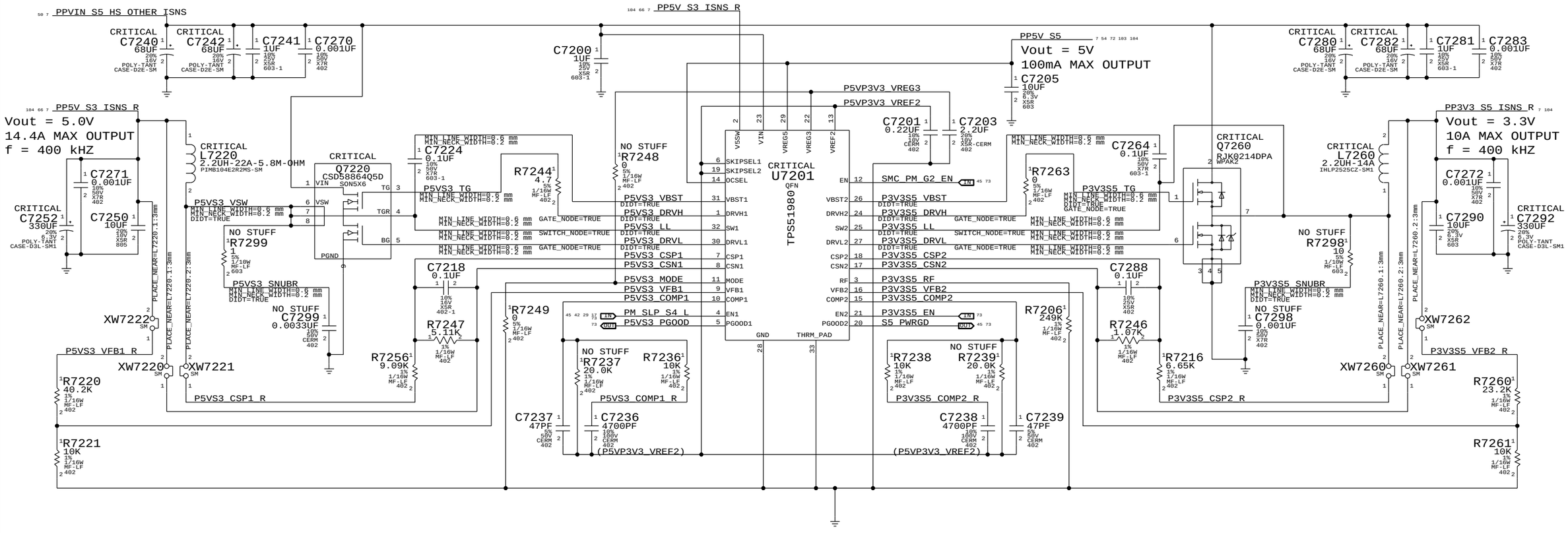

SYNC_MASTER=K92_ERIC SYNC_DATE=08/30/2010

PAGE TITLE
5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

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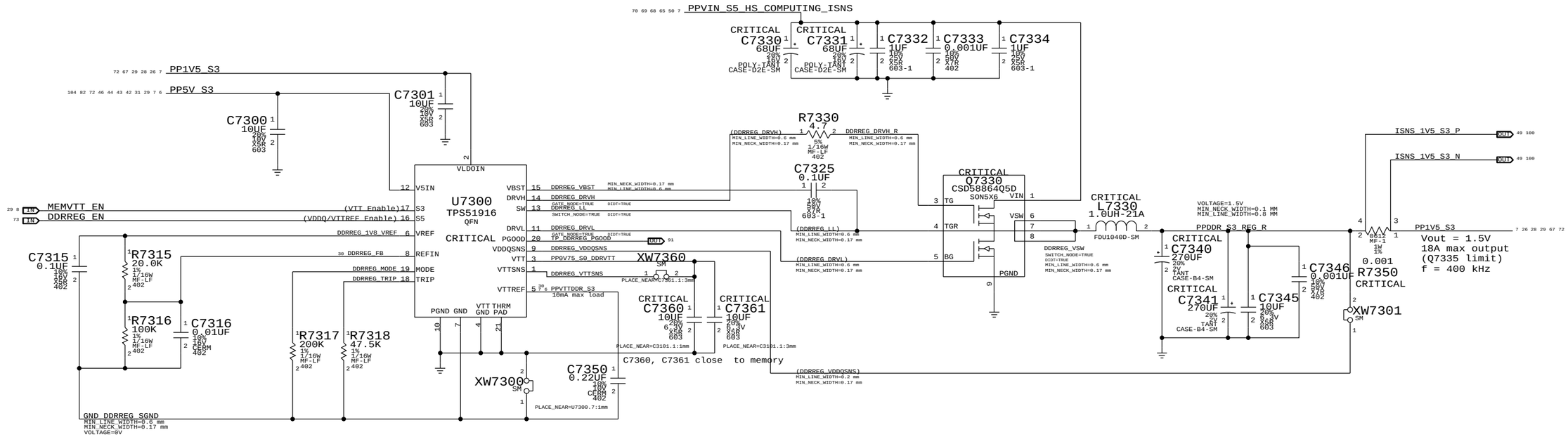

SYNC_MASTER=K91_CHANG	SYNC_DATE=07/21/2010
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER: D
	REVISION:
	BRANCH:
	PAGE: 73 OF 132
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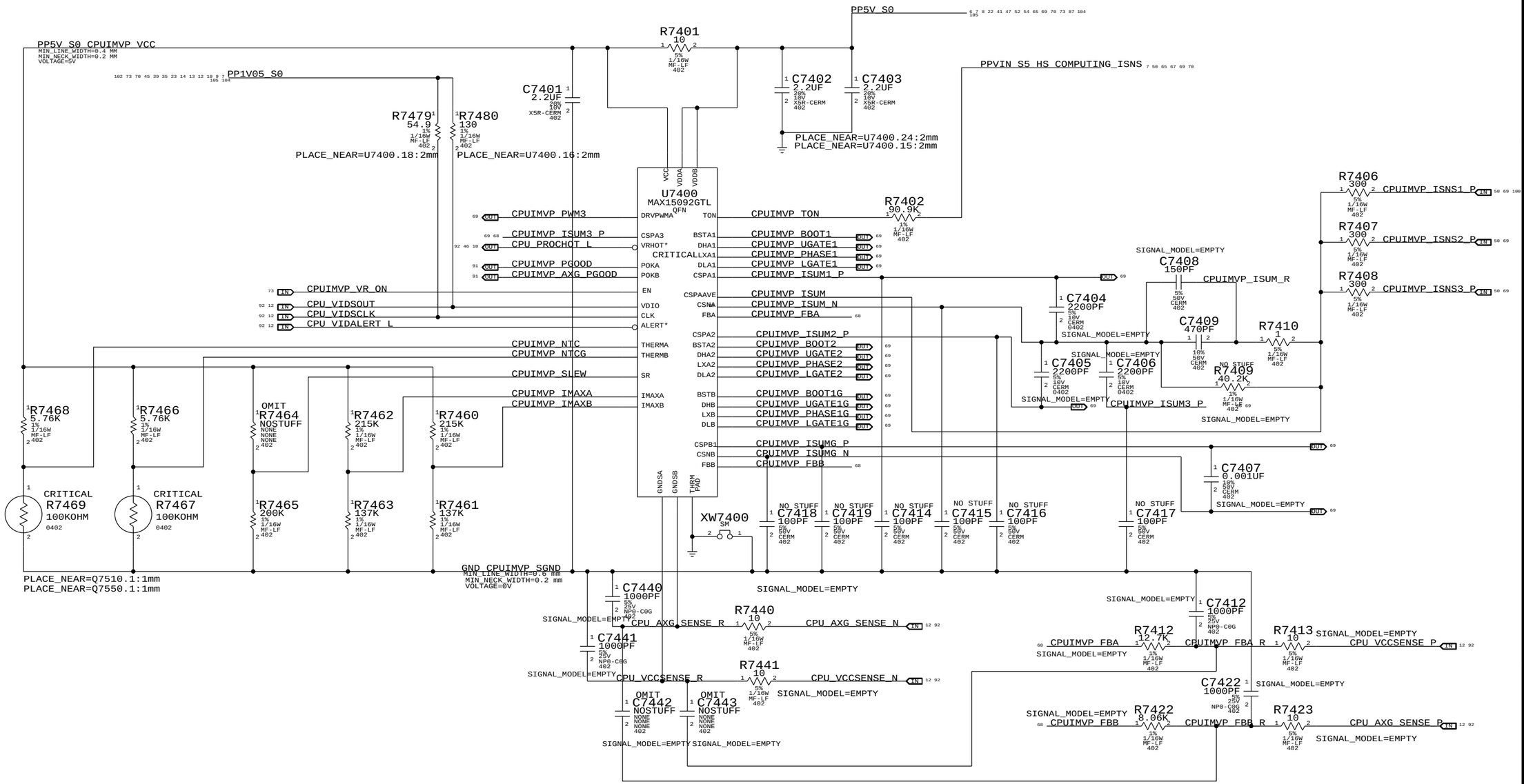

SYNC_MASTER=K92_ERIC	SYNC_DATE=11/09/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Regulator
Apple Inc.	DRAWING NUMBER: D
	REVISION:
	BRANCH:
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PHASE 1

PPVIN_S5_HS_COMPUTING_ISNS

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7510 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7510 0.00075 1% 1W MF 0612

CRITICAL Q7515 IRF6798MTRPBF DIRECTFET-MX

376S0930

THESE TWO CAPS ARE FOR EMC

CRITICAL C7513 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7514 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7515 10UF 10% 16V X5R-CERM 0805

CRITICAL C7516 10UF 10% 16V X5R-CERM 0805

CRITICAL C7517 1UF 10% 16V X5R 402

CRITICAL C7518 0.001UF 10% 50V X7R 402

C7519 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT1_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7511 0 5% 1/16W MF-LF 402

C7511 0.22UF 10% 16V CERM 402

CPUIMVP_BOOT1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

CPUIMVP_UGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE1 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

PPVCORE_S0_CPU_PH1_L

PPVCORE_S0_CPU_PH1

PPVCORE_S0_CPU

NOSTUFF R7512 2.2 5% 1/10W MF-LF 603

CPUIMVP_ISNS1_P

CPUIMVP_ISNS1_N

R7513 46.4 1% 1/16W MF-LF 402

R7514 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

CPUIMVP_PH1_SNUB DIDT=TRUE

NOSTUFF C7512 0.001UF 10% 50V CERM 402

NOSTUFF C7571 330PF 10% 50V CERM 402

CPUIMVP_ISUM1_P

PHASE 2

376S0872

CRITICAL Q7510 IRF6723M2DPBF DIRECTFET-MA

CRITICAL L7520 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7520 0.00075 1% 1W MF 0612

CRITICAL Q7525 IRF6798MTRPBF DIRECTFET-MX

376S0930

THESE TWO CAPS ARE FOR EMC

CRITICAL C7523 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7524 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7525 10UF 10% 16V X5R-CERM 0805

CRITICAL C7526 10UF 10% 16V X5R-CERM 0805

CRITICAL C7527 1UF 10% 16V X5R 402

CRITICAL C7528 0.001UF 10% 50V X7R 402

C7529 0.001UF 10% 50V X7R 402

CPUIMVP_BOOT2_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7521 0 5% 1/16W MF-LF 402

C7521 0.22UF 10% 16V CERM 402

CPUIMVP_BOOT2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE2 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

PPVCORE_S0_CPU_PH2_L

PPVCORE_S0_CPU_PH2

PPVCORE_S0_CPU

NOSTUFF R7522 2.2 5% 1/10W MF-LF 603

CPUIMVP_ISNS2_P

CPUIMVP_ISNS2_N

R7523 46.4 1% 1/16W MF-LF 402

R7524 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

CPUIMVP_PH2_SNUB DIDT=TRUE

NOSTUFF C7522 0.001UF 10% 50V CERM 402

NOSTUFF C7572 330PF 10% 50V CERM 402

CPUIMVP_ISUM2_P

PHASE 3

376S0772

CRITICAL Q7530 IRF6710 S1

CRITICAL L7530 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7530 0.00075 1% 1W MF 0612

CRITICAL Q7535 IRF6798MTRPBF DIRECTFET-MX

376S0930

THESE TWO CAPS ARE FOR EMC

CRITICAL C7533 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7534 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7535 10UF 10% 16V X5R-CERM 0805

CRITICAL C7536 10UF 10% 16V X5R-CERM 0805

CRITICAL C7537 1UF 10% 16V X5R 402

CRITICAL C7538 0.001UF 10% 50V X7R 402

C7539 0.001UF 10% 50V X7R 402

PP5V_S0

R7547 10K 5% 1/16W MF-LF 402

U7541 MAX17491 TQFN CRITICAL

VDD PWN SKIP* BST DH LX DL GND THRM PAD

CPUIMVP_PWM3

CPUIMVP_SKIP

C7541 1UF 10% 16V X5R 402

CPUIMVP_BOOT3 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE3 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE3 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE3 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_BOOT3_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE

R7531 0 5% 1/10W MF-LF 402

C7531 0.22UF 10% 16V CERM 402

SWITCH_NODE=TRUE

PPVCORE_S0_CPU_PH3_L

PPVCORE_S0_CPU_PH3

PPVCORE_S0_CPU

NOSTUFF R7532 2.2 5% 1/10W MF-LF 603

CPUIMVP_ISNS3_P

CPUIMVP_ISNS3_N

R7533 46.4 1% 1/16W MF-LF 402

R7534 10.2 1% 1/16W MF-LF 402

CPUIMVP_ISUM_N

CPUIMVP_PH3_SNUB DIDT=TRUE

NOSTUFF C7532 0.001UF 10% 50V CERM 402

NOSTUFF C7573 330PF 10% 50V CERM 402

CPUIMVP_ISUM3_P

CRITICAL C7561 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7562 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7563 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7564 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7565 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7566 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7567 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7568 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7569 68UF 20% 16V POLY-TANT CASE-D2E-SM

Additonal Input Bulk Caps

AXG PHASE

PPVIN_S5_HS_COMPUTING_ISNS

THESE TWO CAPS ARE FOR EMC

CRITICAL C7553 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7554 68UF 20% 16V POLY-TANT CASE-D2E-SM

CRITICAL C7555 10UF 10% 16V X5R-CERM 0805

CRITICAL C7556 10UF 10% 16V X5R-CERM 0805

CRITICAL C7557 1UF 10% 16V X5R 402

CRITICAL C7558 0.001UF 10% 50V X7R 402

C7559 0.001UF 10% 50V X7R 402

CRITICAL Q7550 CSD58864Q5D SON5X6

CRITICAL L7550 0.36UH-20%-40A-0.000750HM PIMA104E-SM 152S1019

CRITICAL R7550 0.00075 1% 1W MF 0612

376S0906

R7556 0 5% 1/16W MF-LF 402

CPUIMVP_BOOT1G_R MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

C7551 0.22UF 10% 16V CERM 402

R7555 4.7 5% 1/10W MF-LF 402

CPUIMVP_UGATE1G_R MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_BOOT1G MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE

CPUIMVP_UGATE1G MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_PHASE1G MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE SWITCH_NODE=TRUE

CPUIMVP_LGATE1G MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM DIDT=TRUE GATE_NODE=TRUE

CPUIMVP_VSWG MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM SWITCH_NODE=TRUE

PPVCORE_S0_AXG_L

PPVCORE_S0_AXG

NOSTUFF R7552 2.2 5% 1/10W MF-LF 603

CPUIMVP_ISNS1G_P

CPUIMVP_ISNS1G_N

R7553 46.4 1% 1/16W MF-LF 402

R7554 10.2 1% 1/16W MF-LF 402

CPUIMVP_AXG_SNUB DIDT=TRUE

NOSTUFF C7552 0.001UF 10% 50V CERM 402

CPUIMVP_ISUMG_N

NOSTUFF C7574 330PF 10% 50V CERM 402

CPUIMVP_ISUMG_P

SYNC_MASTER=K92_ERIC	SYNC_DATE=09/27/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
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	BRANCH:
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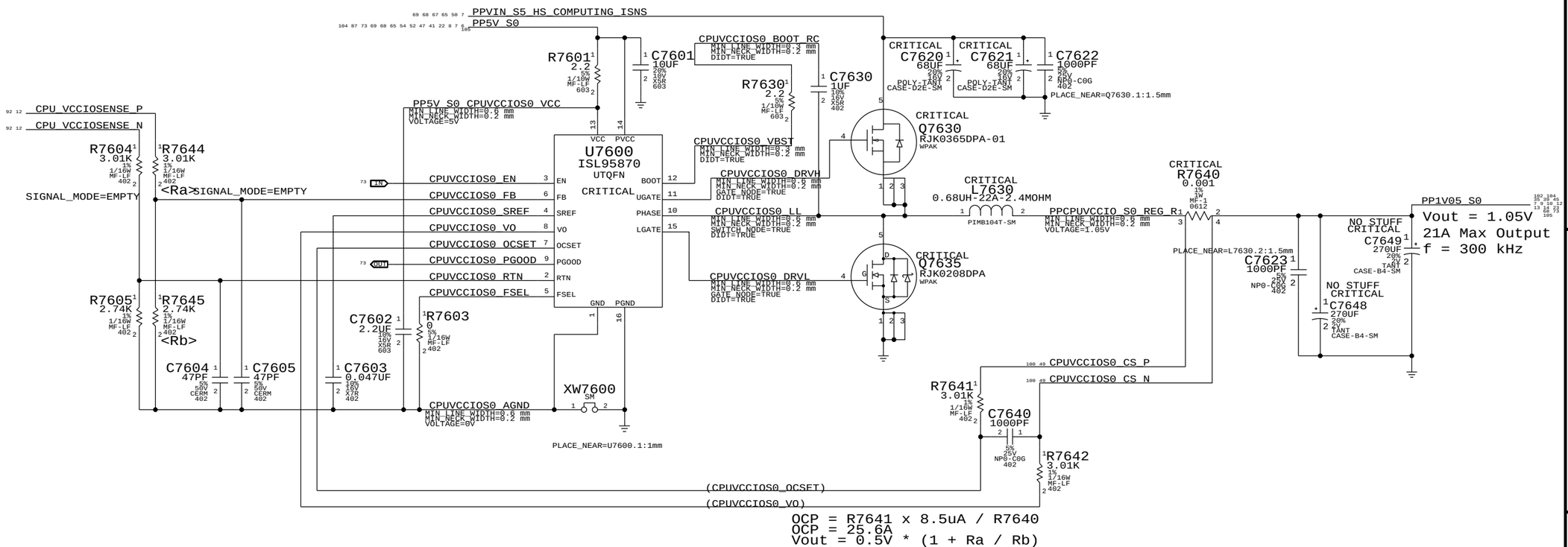
	SHEET: 69 OF 105

CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K92_ERIC SYNC_DATE=09/23/2010

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER | SIZE: D

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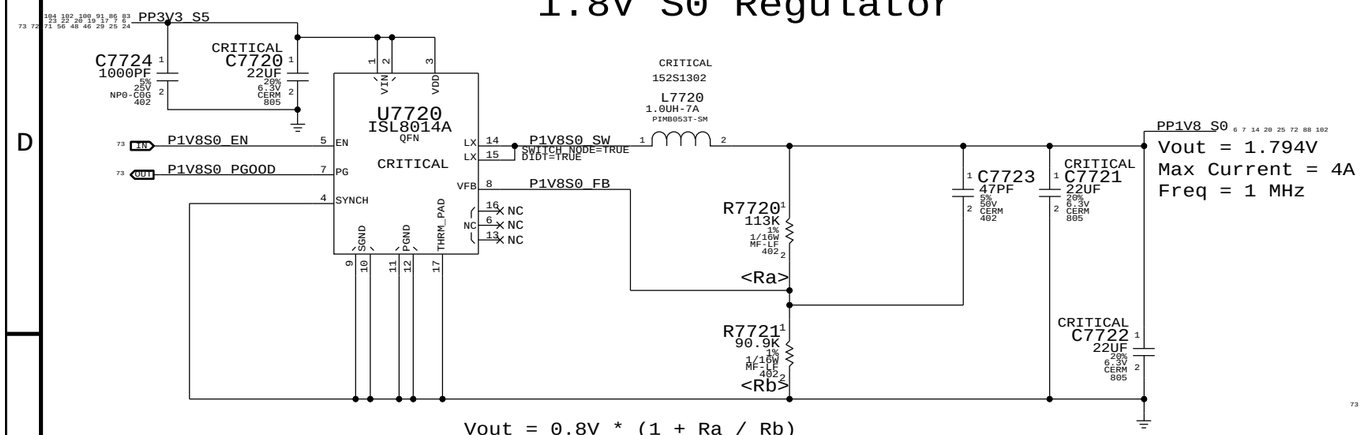
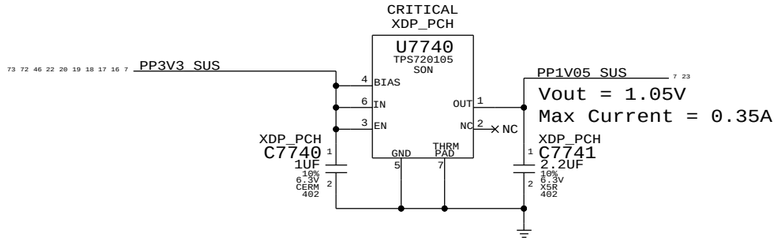
1.8V S0 Regulator



Vout = 0.8V * (1 + Ra / Rb)

1.05V S5 LDO

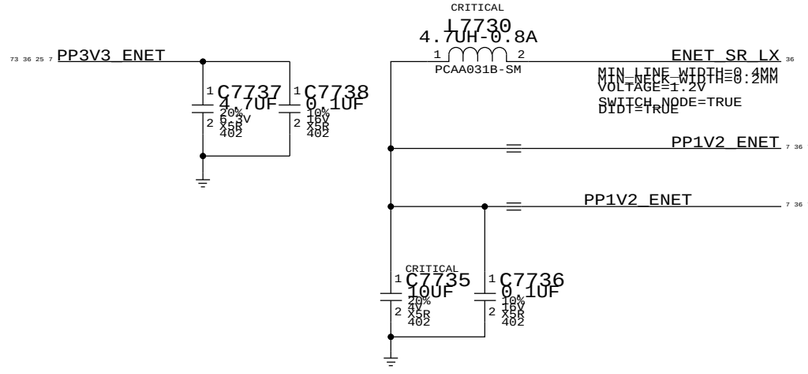
Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



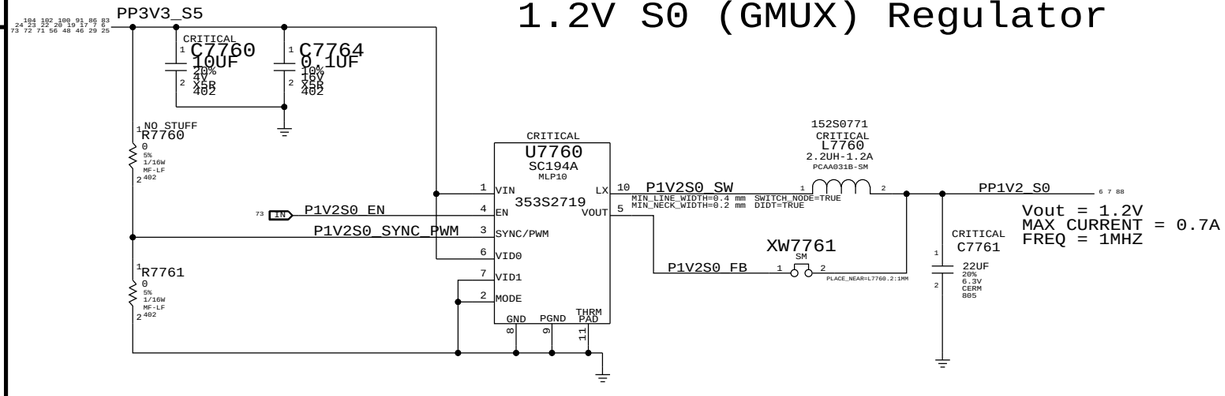
1.5V S0 Regulator

Vout = 0.8V * (1 + Ra / Rb)

CAESAR IV 1.2V INT.VR CMPTS



1.2V S0 (GMUX) Regulator



SYNC_MASTER=K91_CHANG	SYNC_DATE=07/21/2010
PAGE TITLE	Misc Power Supplies
	Apple Inc.
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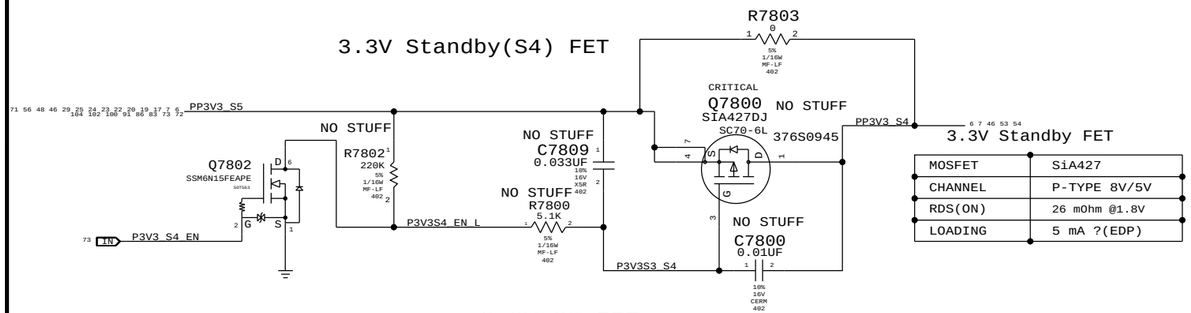
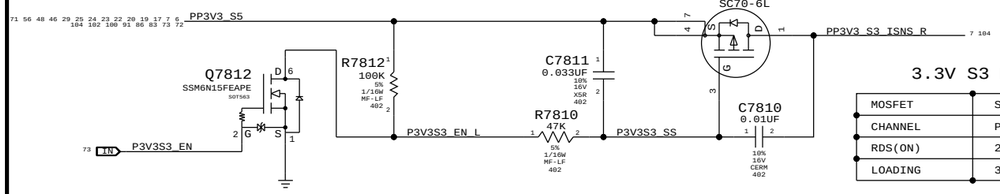
3.3V Standby(S4) FET



3.3V Standby FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	5 mA ?(EDP)

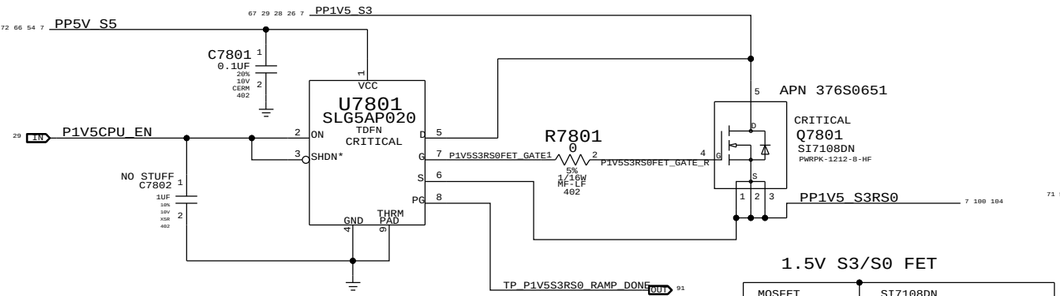
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

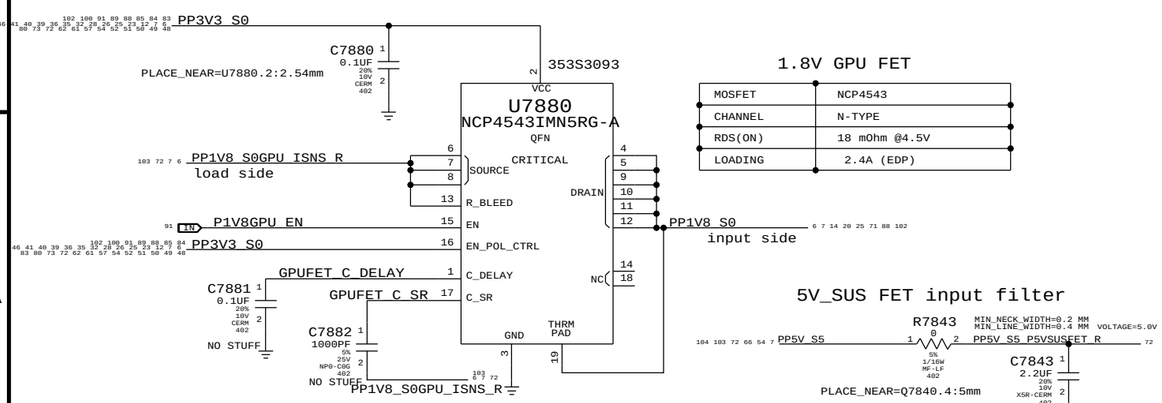
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

1.8V GPU FET

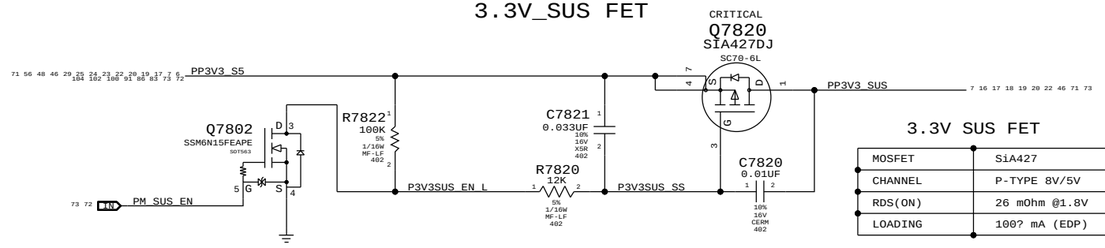


1.8V GPU FET

MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET input filter

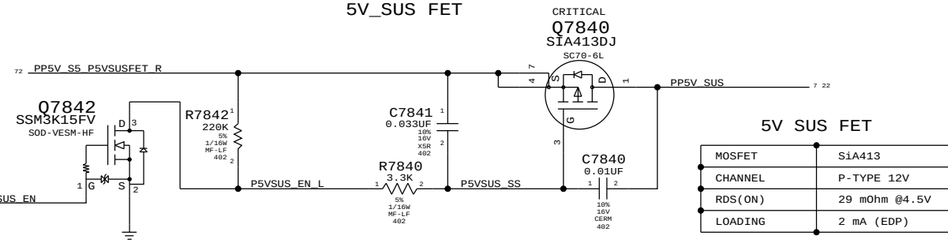
3.3V_SUS FET



3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

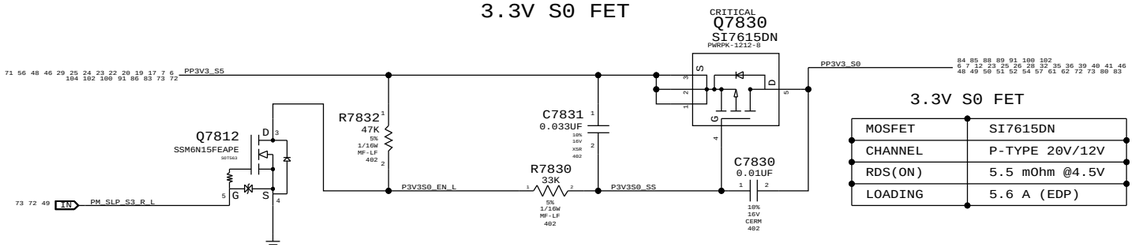
5V_SUS FET



5V SUS FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

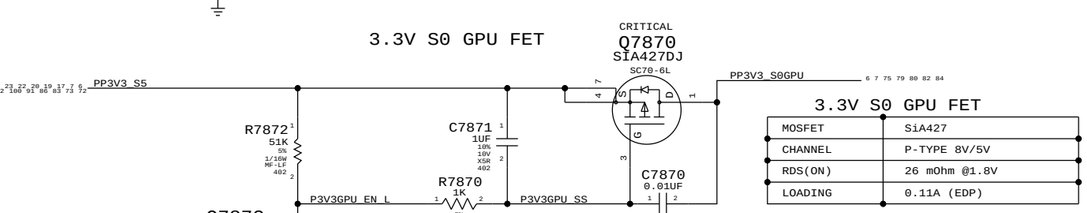
3.3V S0 FET



3.3V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

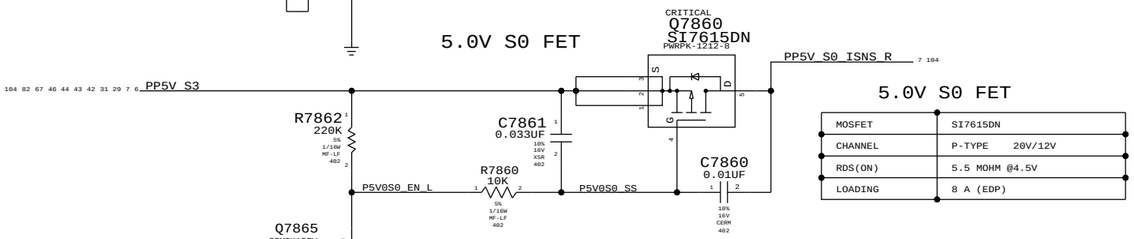
3.3V S0 GPU FET



3.3V S0 GPU FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

U7880 default Turn on delay EN--> on is 200~650us.

SYNC_MASTER=K91_MLB SYNC_DATE=10/18/2010

PAGE TITLE: Power FETs

Apple Inc.

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S5 Rail Enables & PGOOD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

SMC_PM_G2_EN → R7940 100 → P3V3S5_EN

PP3V42_G3H → R7941 100K → S5_PWRGD

C7942 0.0033UF (NO STUFF) — PLACE_NEAR=U7201.21:7mm

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

3.3V,5V S3 ENABLE

PM_SLP_S4_L:100K pull down in PCH page

PM_SLP_S4_L → R7911 5.1K (PLACE_NEAR=U7300.16:6mm) → C7910 0.47UF

R7912 0 (PLACE_NEAR=Q7812.2:6mm) → C7912 0.47UF (NO STUFF)

R7913 3.3K → TPAD_VBUS_EN

P3V3S3_EN, DDRREG_EN

3.3V/5.0V S4 ENABLE

NO STUFF R7916 0 — PM_SLP_S5_L → P3V3_S4_EN — PLACE_NEAR=U1800.G18:5mm

PM_SLP_S5_L:100K pull down on PCH page

3.3V/5.0V Sus ENABLE

PP3V3_S5 — PLACE_NEAR=U7940.1:2.3mm

C7940 0.1uF

U7940 74AUP1G3208 SOT891

SMC_BATLOW_L:100K pull up on SMC page

SMC_BATLOW_L

PM_SLP_SUS_L:100K pull down on PCH page

PM_SLP_SUS_L → PM_SUS_EN

NO STUFF R7917 0

S0 ENABLE

PM_SLP_S3_L → R7978 100

PM_SLP_S3_L:100K pull down in PCH page

(PM_SLP_S3_R_L)

R7987 33K (PLACE_NEAR=U7100.15:6mm)

R7981 20K (PLACE_NEAR=U7600.3:6mm)

R7985 20K (PLACE_NEAR=U7760.4:6mm)

R7988 10K (PLACE_NEAR=U7710.2:6mm)

R7986 5.1K (PLACE_NEAR=U7720.5:6mm)

PM_SLP_S3_R_L, P1V8S0_EN, P1V5S0_EN, P1V2S0_EN, CPUVCCIOS0_EN, PVCCSA_EN

C7987 0.47UF, C7981 0.47UF, C7985 1UF, C7988 0.47UF, C7986 0.47UF

CHGR VFRQ Generation

PP3V42_G3H → R7931 100K → CHGR_VFRQ

Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

CPUVCORE ENABLE

ALL_SYS_PWRGD → R7974 0 → CPUIMVP_VR_ON

NO STUFF R7976 0 (PLACE_NEAR=U7400.7:5mm)

CPUVCCIOS0_PGOOD → R7975 0 → PM_PECI_PWRGD

S0 Rail PGOOD (BJT Version)

PP3V3_S5 → R7956 150K

PP3V3_S0 → R7951 15.0K

R7953 1K (VMON_3V3_DIV) — R7952 7.15K

R7954 1K (VMON_Q2_BASE) — PP1V5_S3RS0_CPUDDR → PP1V5_S3RS0

R7955 1K (VMON_Q3_BASE) — PP1V05_S0 → VMON_Q4_BASE

S0PGD_C

Q7950 ASMCC0179 DFN2015H4-8 (Q1, Q2, Q3, Q4) CRITICAL

NC, NC

353S2809 S0PGD_BJT_GND_R

R7957 100 → ALL_SYS_PWRGD

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V SUS Detect

PP3V3_S5 — PLACE_NEAR=U7930.6:2.3mm

C7930 0.1uF

No stuff C7931, 12ms Min delay time

U7930 Sense input threhold is 3.07V

U7930 TPS3808G33DBVRG4 SOT23-6 (SENSE, RESET*, MR*, VDD, GND, CT) CRITICAL

R7933 100K → PP3V3_SUS

C7931 0.001UF (NO STUFF)

PM_RSMRST_L → PM_RSMRST_L goes to U1800.C21

ENET Enable Generation

3.3V ENET FET

Q7922 NTR4101P SOT-23-HF (CRITICAL)

PP3V3_S3 → R7921 10K → PM_SLP_S3_ENET

R7922 100K → P3V3ENET_SS

C7921 0.033UF → PP3V3_ENET

C7922 0.01UF

Q7921 SSM3K15FV SOD-VESM-HF

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_SLP_S3_L → Q7925 2N7002DW-X-G SOT-363 → PM_WLAN_EN_L

WOL_EN → Q7925 2N7002DW-X-G SOT-363 → AP_PWR_EN

AC_EN_L → Q7920 2N7002DW-X-G SOT-363 (AC_EN_L)

SMC_ADAPTER_EN → Q7920 2N7002DW-X-G SOT-363 (PM_SLP_S3_L)

R7929 0 (NO STUFF)

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

PP5V_S0, PP3V3_S0, PP1V5_S3RS0_CPUDDR, PP1V05_S0

R7960 6.04K, R7970 10K, R7972 6.04K, R7961 15.0K, R7971 10K, R7973 15.0K

S0PGOOD_ISL → C7960 0.1uF

U7960 ISL88042IRTEZ TDFN (IPU) CRITICAL (VDD, V2MON, V3MON, V4MON, MR*, RST*, GND, THRM_PAD)

VMON_PP5V_DIV, VMON_PP1V5_DIV, VMON_PP1V05_DIV

353S2310

R7962 330 → ALL_SYS_PWRGD

P1V5S0_PGOOD from U7710

R7967 10K, R7968 100, R7966 100, R7965 100, R7964 100, R7963 100

P1V5S0_PGOOD, P5VS3_PGOOD, CPUVCCIOS0_PGOOD, PVCCSA_PGOOD

SMC_S4_WAKESRC_EN

SYNC_MASTER=K92_YUAN SYNC_DATE=07/22/2010

PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEG_R2D_C_P<0>	C8020 0.1UF	PEG_R2D_P<0>	PEG_D2R_C_P<0>	C8055 0.1UF	PEG_D2R_P<0>	PEG_R2D_P<0>	PEG_D2R_C_P<0>
PEG_R2D_C_N<0>	C8021 0.1UF	PEG_R2D_N<0>	PEG_D2R_C_N<0>	C8056 0.1UF	PEG_D2R_N<0>	PEG_R2D_N<0>	PEG_D2R_C_N<0>
PEG_R2D_C_P<1>	C8022 0.1UF	PEG_R2D_P<1>	PEG_D2R_C_P<1>	C8057 0.1UF	PEG_D2R_P<1>	PEG_R2D_P<1>	PEG_D2R_C_P<1>
PEG_R2D_C_N<1>	C8023 0.1UF	PEG_R2D_N<1>	PEG_D2R_C_N<1>	C8058 0.1UF	PEG_D2R_N<1>	PEG_R2D_N<1>	PEG_D2R_C_N<1>
PEG_R2D_C_P<2>	C8024 0.1UF	PEG_R2D_P<2>	PEG_D2R_C_P<2>	C8059 0.1UF	PEG_D2R_P<2>	PEG_R2D_P<2>	PEG_D2R_C_P<2>
PEG_R2D_C_N<2>	C8025 0.1UF	PEG_R2D_N<2>	PEG_D2R_C_N<2>	C8060 0.1UF	PEG_D2R_N<2>	PEG_R2D_N<2>	PEG_D2R_C_N<2>
PEG_R2D_C_P<3>	C8026 0.1UF	PEG_R2D_P<3>	PEG_D2R_C_P<3>	C8061 0.1UF	PEG_D2R_P<3>	PEG_R2D_P<3>	PEG_D2R_C_P<3>
PEG_R2D_C_N<3>	C8027 0.1UF	PEG_R2D_N<3>	PEG_D2R_C_N<3>	C8062 0.1UF	PEG_D2R_N<3>	PEG_R2D_N<3>	PEG_D2R_C_N<3>
PEG_R2D_C_P<4>	C8028 0.1UF	PEG_R2D_P<4>	PEG_D2R_C_P<4>	C8063 0.1UF	PEG_D2R_P<4>	PEG_R2D_P<4>	PEG_D2R_C_P<4>
PEG_R2D_C_N<4>	C8029 0.1UF	PEG_R2D_N<4>	PEG_D2R_C_N<4>	C8064 0.1UF	PEG_D2R_N<4>	PEG_R2D_N<4>	PEG_D2R_C_N<4>
PEG_R2D_C_P<5>	C8030 0.1UF	PEG_R2D_P<5>	PEG_D2R_C_P<5>	C8065 0.1UF	PEG_D2R_P<5>	PEG_R2D_P<5>	PEG_D2R_C_P<5>
PEG_R2D_C_N<5>	C8031 0.1UF	PEG_R2D_N<5>	PEG_D2R_C_N<5>	C8066 0.1UF	PEG_D2R_N<5>	PEG_R2D_N<5>	PEG_D2R_C_N<5>
PEG_R2D_C_P<6>	C8032 0.1UF	PEG_R2D_P<6>	PEG_D2R_C_P<6>	C8067 0.1UF	PEG_D2R_P<6>	PEG_R2D_P<6>	PEG_D2R_C_P<6>
PEG_R2D_C_N<6>	C8033 0.1UF	PEG_R2D_N<6>	PEG_D2R_C_N<6>	C8068 0.1UF	PEG_D2R_N<6>	PEG_R2D_N<6>	PEG_D2R_C_N<6>
PEG_R2D_C_P<7>	C8034 0.1UF	PEG_R2D_P<7>	PEG_D2R_C_P<7>	C8069 0.1UF	PEG_D2R_P<7>	PEG_R2D_P<7>	PEG_D2R_C_P<7>
PEG_R2D_C_N<7>	C8035 0.1UF	PEG_R2D_N<7>	PEG_D2R_C_N<7>	C8070 0.1UF	PEG_D2R_N<7>	PEG_R2D_N<7>	PEG_D2R_C_N<7>

All 0.1UF: 10%6.3V X5R 201

PM_ALL_GPU_PGOOD → R8003 NOSTUFF 0 5% 1/16W MF-LF 402 → R8004 10K 5% 1/16W MF-LF 402

EG_RESET_L → R8000 0 5% 1/16W MF-LF 402 → GPU_RESET_R_L

PEG_R2D_C_P<0>	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_D2R_C_P<0>
PEG_R2D_C_N<0>	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_D2R_C_N<0>
PEG_R2D_C_P<1>	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_D2R_C_P<1>
PEG_R2D_C_N<1>	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_D2R_C_N<1>
PEG_R2D_C_P<2>	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_D2R_C_P<2>
PEG_R2D_C_N<2>	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_D2R_C_N<2>
PEG_R2D_C_P<3>	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_D2R_C_P<3>
PEG_R2D_C_N<3>	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_D2R_C_N<3>
PEG_R2D_C_P<4>	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_D2R_C_P<4>
PEG_R2D_C_N<4>	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_D2R_C_N<4>
PEG_R2D_C_P<5>	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_D2R_C_P<5>
PEG_R2D_C_N<5>	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_D2R_C_N<5>
PEG_R2D_C_P<6>	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_D2R_C_P<6>
PEG_R2D_C_N<6>	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_D2R_C_N<6>
PEG_R2D_C_P<7>	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_D2R_C_P<7>
PEG_R2D_C_N<7>	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_D2R_C_N<7>
NC	N38	PCIE_RX8P	PCIE_TX8P	N33	NC
NC	M37	PCIE_RX8N	PCIE_TX8N	N32	NC
NC	M35	PCIE_RX9P	PCIE_TX9P	N30	NC
NC	L36	PCIE_RX9N	PCIE_TX9N	N29	NC
NC	L38	PCIE_RX10P	PCIE_TX10P	L33	NC
NC	K37	PCIE_RX10N	PCIE_TX10N	L32	NC
NC	K35	PCIE_RX11P	PCIE_TX11P	L30	NC
NC	J36	PCIE_RX11N	PCIE_TX11N	L29	NC
NC	J38	PCIE_RX12P	PCIE_TX12P	K33	NC
NC	H37	PCIE_RX12N	PCIE_TX12N	K32	NC
NC	H35	PCIE_RX13P	PCIE_TX13P	J33	NC
NC	G36	PCIE_RX13N	PCIE_TX13N	J32	NC
NC	G38	PCIE_RX14P	PCIE_TX14P	K30	NC
NC	F37	PCIE_RX14N	PCIE_TX14N	K29	NC
NC	F35	PCIE_RX15P	PCIE_TX15P	H33	NC
NC	E37	PCIE_RX15N	PCIE_TX15N	H32	NC
PEG_CLK100M_P	AB35	PCIE_REFCLKP	PCIE_CALRP	Y30	PEG_CALRP
PEG_CLK100M_N	AA36	PCIE_REFCLKN	PCIE_CALRN	Y29	PEG_CALRN
GPU_PWRGOOD	AH16	PWRGOOD			
GPU_RESET_R_L	AA30	PERST*			

U8000 — FCBGA (1 OF 9) PCIE WHISTLER 40NM-ES — OMIT

R8001 2.0K 1% 1/16W MF-LF 402 — R8002 1.27K 1% 1/16W MF-LF 402 — PP1V0_S0GPU

SYNC_MASTER=K91_MLB SYNC_DATE=10/19/2010

PAGE TITLE: Whistler PCI-E

Apple Inc.

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Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

U8000 WHISTLER 40NM-ES FCBGA (7 OF 9)

MEM I/O: PP1V5R1V35_GPU_FB_ISNS, TBD mA, C8100–C8104 10UF; C8105–C8114 1UF; C8115–C8124 0.1UF; L8120 120OHM-0.3A CRITICAL; PP1V8_S0GPU; VDDR1_AC7, VDDR1_AD11, VDDR1_AF7, VDDR1_AG10, VDDR1_AJ7, VDDR1_AK8, VDDR1_AL9, VDDR1_G11, VDDR1_G14, VDDR1_G17, VDDR1_G20, VDDR1_G23, VDDR1_G26, VDDR1_G29, VDDR1_H10, VDDR1_J7, VDDR1_J9, VDDR1_K8, VDDR1_K11, VDDR1_K13, VDDR1_L7, VDDR1_L12, VDDR1_L16, VDDR1_L21, VDDR1_L23, VDDR1_L26, VDDR1_M11, VDDR1_N11, VDDR1_P7, VDDR1_R11, VDDR1_U7, VDDR1_U11, VDDR1_Y7, VDDR1_Y11

CORE: PP1V8_GPU_VDD_CT, 219mA, C8125–C8129; L8130 470OHM-1A-150MOHM CRITICAL; PP1V0_S0GPU; PP1V0_GPU_PLL; GND_GPU_PLL; C8130–C8132; VDD_CT_AF26, VDD_CT_AF27, VDD_CT_AG26, VDD_CT_AG27

LEVEL TRNSL: PP3V3_S0GPU, 60 mA, C8133–C8136; VDDR3_AF23, VDDR3_AF24, VDDR3_AG23, VDDR3_AG24

I/O: L8131 470OHM-1A-150MOHM CRITICAL; PP1V8_S0GPU; PP1V8_GPU_MEM_PLL; C8137–C8141; PP1V8_GPU_VDDR4, TBD mA; VDDR4_AF13, VDDR4_AF15, VDDR4_AG13, VDDR4_AG15, VDDR4_AD12, VDDR4_AF11, VDDR4_AF12, VDDR4_AG11

PLL: L8132 120OHM-0.3A CRITICAL; PP1V8_S0GPU; PP1V8_GPU_PLL; C8142–C8144; XW8100 SM; L8140 FERR-220-OHM-2A CRITICAL; PP1V8_S0GPU; PP1V8_GPU_PCIE_VDDR, 504mA, C8145–C8150; L8155 FERR-120-OHM-3A CRITICAL; PP1V0_S0GPU; PP1V0_GPU_PCIE_VDDC, 1920mA, C8151–C8158; NC/VDDRHA, NC/VSSRHA, NC/VSSRHB, NC/VDDRHB, MPV18_H7, MPV18_H8, SPV18 75mA, SPV10 120mA, SPVSS, FB_VDDC, FB_VDDCI, FB_GND, PCIE_VDDR_AA31, PCIE_VDDR_AA32, PCIE_VDDR_AA33, PCIE_VDDR_AA34, PCIE_VDDR_AB37, PCIE_VDDR_V28, PCIE_VDDR_W29, PCIE_VDDR_W30, PCIE_VDDR_Y31, PCIE_VDDC_G30, PCIE_VDDC_G31, PCIE_VDDC_H29, PCIE_VDDC_H30, PCIE_VDDC_J29, PCIE_VDDC_J30, PCIE_VDDC_L28, PCIE_VDDC_M28, PCIE_VDDC_N28, PCIE_VDDC_R28, PCIE_VDDC_T28, PCIE_VDDC_U28

VOLT SENSE: GPU_VDD_SENSE, GPU_GND_SENSE

ISOLATED CORE I/O

OMIT

CRITICAL L8150 120OHM-0.3A 0402: PP1V8_S0GPU → PP1V8_GPU_VDDR4; MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V; C81C0 1UF, C81C1 0.1UF

PPVCORE_GPU: VDDC_AA15, VDDC_AA17, VDDC_AA20, VDDC_AA22, VDDC_AA24, VDDC_AA27, VDDC_AB16, VDDC_AB18, VDDC_AB21, VDDC_AB23, VDDC_AB26, VDDC_AB28, VDDC_AC17, VDDC_AC20, VDDC_AC22, VDDC_AC24, VDDC_AC27, VDDC_AD18, VDDC_AD21, VDDC_AD23, VDDC_AD26, VDDC_AF17, VDDC_AF20, VDDC_AF22, VDDC_AG16, VDDC_AG18, VDDC_AG21, VDDC_AH22, VDDC_AH27, VDDC_AH28, VDDC_M26, VDDC_N24, BIF_VDDC_N27, VDDC_R18, VDDC_R21, VDDC_R23, VDDC_R26, VDDC_T17, VDDC_T20, VDDC_T22, VDDC_T24, BIF_VDDC_T27, VDDC_U16, VDDC_U18, VDDC_U21, VDDC_U23, VDDC_U26, VDDC_V17, VDDC_V20, VDDC_V22, VDDC_V24, VDDC_V27, VDDC_Y16, VDDC_Y18, VDDC_Y21, VDDC_Y23, VDDC_Y26, VDDC_Y28

- C8160–C8169 1UF
- C8170–C8179 1UF
- C8180–C8189 1UF
- C8190–C8199 10UF
- C81A0–C81A9 1UF
- C81B0–C81B2 10UF

VDDCI_AA13, VDDCI_AB13, VDDCI_AC12, VDDCI_AC15, VDDCI_AD13, VDDCI_AD16, VDDCI_M15, VDDCI_M16, VDDCI_M18, VDDCI_M23, VDDCI_N13, VDDCI_N15, VDDCI_N17, VDDCI_N20, VDDCI_N22, VDDCI_R12, VDDCI_R13, VDDCI_R16, VDDCI_T12, VDDCI_T15, VDDCI_V15, VDDCI_Y13

SYNC_MASTER=K92_BEN	SYNC_DATE=06/03/2010
PAGE TITLE	Whistler CORE/FB POWER
Apple Inc.	DRAWING NUMBER: D; SIZE: D
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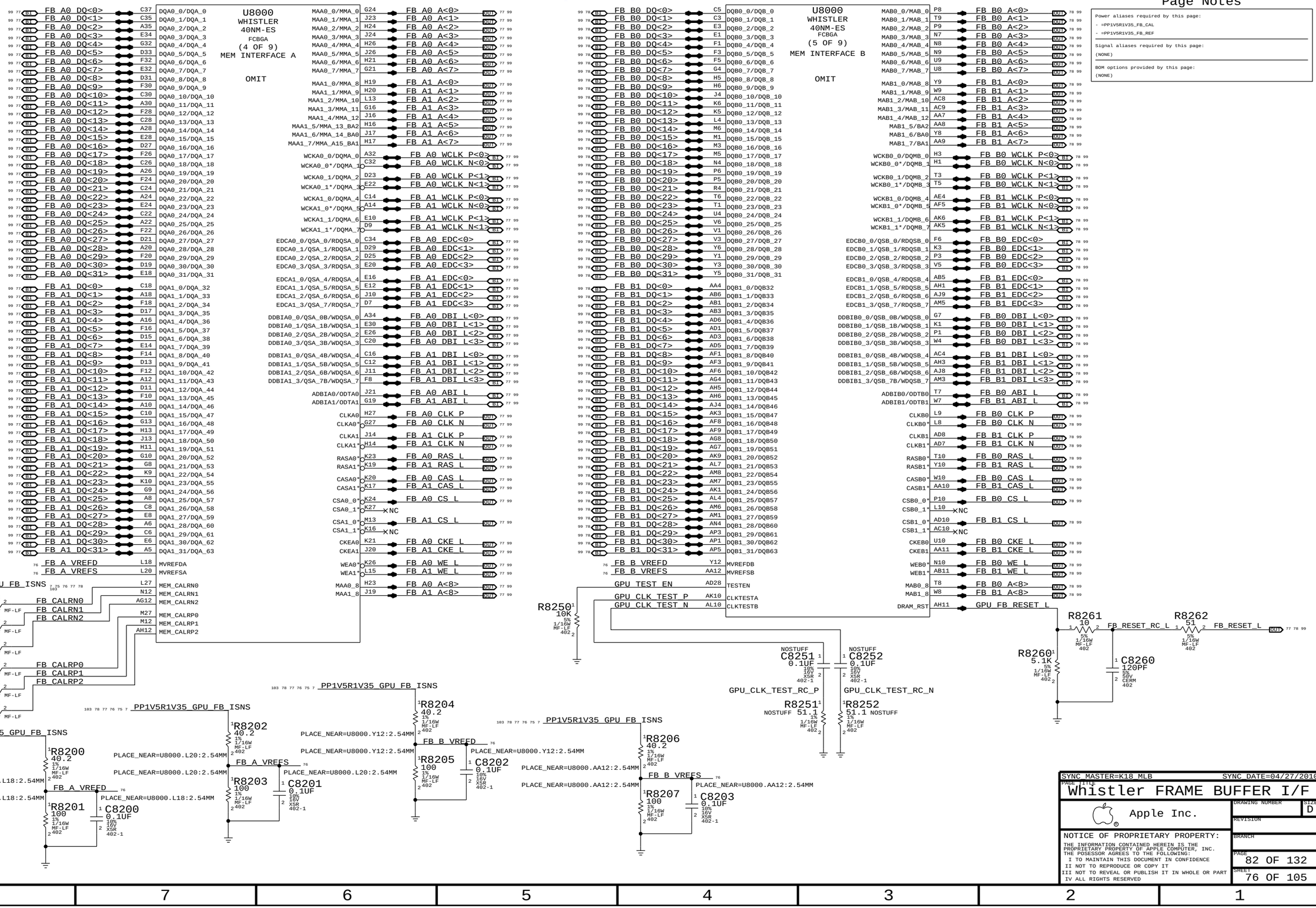

Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT

PP1V5R1V35_GPU_FB_ISNS

R8400 120 1% 1/20W MF 201
R8404 120 1% 1/20W MF 201
R8403 120 1% 1/20W MF 201
R8401 60.4 1% 1/16W MF-LF 402
R8402 60.4 1% 1/16W MF-LF 402
R8450 120 1% 1/20W MF 201
R8454 120 1% 1/20W MF 201
R8453 120 1% 1/20W MF 201
R8451 60.4 1% 1/16W MF-LF 402
R8452 60.4 1% 1/16W MF-LF 402

C8400 C8401 C8402 C8403 C8404 C8405 4.7UF 20% 6.3V X5R 402
C8406 C8407 C8408 C8409 C8410 C8411 C8412 C8413 1UF 10% 6.3V CERM-X5R 402
C8414 C8415 1UF 10% 6.3V CERM-X5R 402
C8416 C8417 0.1UF 10% 6.3V X5R 201
C8418 C8419 C8420 C8421 C8422 C8423 C8424 C8425 0.1UF 10% 6.3V X5R 201
C8450 C8451 C8452 C8453 C8454 C8455 4.7UF 20% 6.3V X5R 402
C8456 C8457 C8458 C8459 C8460 C8461 C8462 C8463 1UF 10% 6.3V CERM-X5R 402
C8464 C8465 C8466 C8467 C8468 C8469 C8470 C8471 C8472 C8473 C8474 C8475 0.1UF 10% 6.3V X5R 201

R8430 2.37K 1% 1/16W MF-LF 402
R8431 5.49K 1% 1/16W MF-LF 402
R8432 2.37K 1% 1/16W MF-LF 402
R8433 5.49K 1% 1/16W MF-LF 402
R8434 2.37K 1% 1/16W MF-LF 402
R8435 5.49K 1% 1/16W MF-LF 402
C8430 C8431 C8432 C8433 C8434 C8435 1UF 10% 6.3V CERM-X5R 402

R8480 2.37K 1% 1/16W MF-LF 402
R8481 5.49K 1% 1/16W MF-LF 402
R8482 2.37K 1% 1/16W MF-LF 402
R8483 5.49K 1% 1/16W MF-LF 402
R8484 2.37K 1% 1/16W MF-LF 402
R8485 5.49K 1% 1/16W MF-LF 402
C8480 C8481 C8482 C8483 C8484 C8485 1UF 10% 6.3V CERM-X5R 402

SYNC_MASTER=K91_YUN	SYNC_DATE=08/23/2010
PAGE TITLE: GDDR5 Frame Buffer A	
Apple Inc.	DRAWING NUMBER / SIZE D
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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

U8500 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (1 OF 2) OMIT

U8500 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (2 OF 2) OMIT

U8550 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (1 OF 2) OMIT

U8550 32MX32-1.25GHZ-MFL BGA H5GQ1H24AFR-T2C (2 OF 2) OMIT

PP1V5R1V35_GPU_FB_ISNS

R8501 60.4 1% 1/16W MF-LF 402

R8502 60.4 1% 1/16W MF-LF 402

R8551 60.4 1% 1/16W MF-LF 402

R8552 60.4 1% 1/16W MF-LF 402

R8500 120 1% 1/20W MF 201

R8504 120 1% 1/20W MF 201

R8503 120 1% 1/20W MF 201

R8550 120 1% 1/20W MF 201

R8554 120 1% 1/20W MF 201

R8553 120 1% 1/20W MF 201

C8500 4.7UF 20% 6.3V X5R 402

C8501 4.7UF 20% 6.3V X5R 402

C8502 4.7UF 20% 6.3V X5R 402

C8503 4.7UF 20% 6.3V X5R 402

C8504 4.7UF 20% 6.3V X5R 402

C8505 4.7UF 20% 6.3V X5R 402

C8506 1UF 10% 6.3V CERM-X5R 402

C8507 1UF 10% 6.3V CERM-X5R 402

C8508 1UF 10% 6.3V CERM-X5R 402

C8509 1UF 10% 6.3V CERM-X5R 402

C8510 1UF 10% 6.3V CERM-X5R 402

C8511 1UF 10% 6.3V CERM-X5R 402

C8512 1UF 10% 6.3V CERM-X5R 402

C8513 1UF 10% 6.3V CERM-X5R 402

C8514 1UF 10% 6.3V CERM-X5R 402

C8515 1UF 10% 6.3V CERM-X5R 402

C8516 0.1UF 10% 6.3V X5R 201

C8517 0.1UF 10% 6.3V X5R 201

C8518 0.1UF 10% 6.3V X5R 201

C8519 0.1UF 10% 6.3V X5R 201

C8520 0.1UF 10% 6.3V X5R 201

C8521 0.1UF 10% 6.3V X5R 201

C8522 0.1UF 10% 6.3V X5R 201

C8523 0.1UF 10% 6.3V X5R 201

C8524 0.1UF 10% 6.3V X5R 201

C8525 0.1UF 10% 6.3V X5R 201

C8550 4.7UF 20% 6.3V X5R 402

C8551 4.7UF 20% 6.3V X5R 402

C8552 4.7UF 20% 6.3V X5R 402

C8553 4.7UF 20% 6.3V X5R 402

C8554 4.7UF 20% 6.3V X5R 402

C8555 4.7UF 20% 6.3V X5R 402

C8556 1UF 10% 6.3V CERM-X5R 402

C8557 1UF 10% 6.3V CERM-X5R 402

C8558 1UF 10% 6.3V CERM-X5R 402

C8559 1UF 10% 6.3V CERM-X5R 402

C8560 1UF 10% 6.3V CERM-X5R 402

C8561 1UF 10% 6.3V CERM-X5R 402

C8562 1UF 10% 6.3V CERM-X5R 402

C8563 1UF 10% 6.3V CERM-X5R 402

C8564 1UF 10% 6.3V CERM-X5R 402

C8565 1UF 10% 6.3V CERM-X5R 402

C8566 0.1UF 10% 6.3V X5R 201

C8567 0.1UF 10% 6.3V X5R 201

C8568 0.1UF 10% 6.3V X5R 201

C8569 0.1UF 10% 6.3V X5R 201

C8570 0.1UF 10% 6.3V X5R 201

C8571 0.1UF 10% 6.3V X5R 201

C8572 0.1UF 10% 6.3V X5R 201

C8573 0.1UF 10% 6.3V X5R 201

C8574 0.1UF 10% 6.3V X5R 201

C8575 0.1UF 10% 6.3V X5R 201

R8530 2.37K 1% 1/16W MF-LF 402

C8530 1UF 10% 6.3V CERM-X5R 402

R8531 5.49K 1% 1/16W MF-LF 402

C8531 1UF 10% 6.3V CERM-X5R 402

R8532 2.37K 1% 1/16W MF-LF 402

C8532 1UF 10% 6.3V CERM-X5R 402

R8533 5.49K 1% 1/16W MF-LF 402

C8533 1UF 10% 6.3V CERM-X5R 402

R8534 2.37K 1% 1/16W MF-LF 402

C8534 1UF 10% 6.3V CERM-X5R 402

R8535 5.49K 1% 1/16W MF-LF 402

C8535 1UF 10% 6.3V CERM-X5R 402

R8580 2.37K 1% 1/16W MF-LF 402

C8580 1UF 10% 6.3V CERM-X5R 402

R8581 5.49K 1% 1/16W MF-LF 402

C8581 1UF 10% 6.3V CERM-X5R 402

R8582 2.37K 1% 1/16W MF-LF 402

C8582 1UF 10% 6.3V CERM-X5R 402

R8583 5.49K 1% 1/16W MF-LF 402

C8583 1UF 10% 6.3V CERM-X5R 402

R8584 2.37K 1% 1/16W MF-LF 402

C8584 1UF 10% 6.3V CERM-X5R 402

R8585 5.49K 1% 1/16W MF-LF 402

C8585 1UF 10% 6.3V CERM-X5R 402

SYNC_MASTER=K91_YUN	SYNC_DATE=08/23/2010
PAGE TITLE: GDDR5 Frame Buffer B	
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION
	BRANCH
	PAGE 85 OF 132
	SHEET 78 OF 105

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE:

AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

PP1V8_S0GPU
OMIT R8610 10K 5% 1/16W MF-LF 402
R8611 10K 5% 1/16W MF-LF 402
NOSTUFF R8612 10K 5% 1/16W MF-LF 402
VRAM_HYNIX R8613 10K 5% 1/16W MF-LF 402

PP3V3_S0GPU
R8600 4.7K 5% 1/16W MF-LF 402
R8601 4.7K 5% 1/16W MF-LF 402

PP1V8_S0GPU
R8602 499 1% 1/16W MF-LF 402
C8600 0.1UF 10% 16V X5R 402-1
R8603 249 1% 1/16W MF-LF 402

CRITICAL L8600 470OHM-1A-150MOHM 0603
PP1V8_S0GPU VOLTAGE=1.8V
C8601 10UF 20% 10V X5R 603
C8602 1UF 10% 25V X5R 402
C8603 0.1UF 10% 16V X5R 402-1
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V

CRITICAL L8601 470OHM-1A-150MOHM 0603
PP1V0_S0GPU
C8604 10UF 20% 10V X5R 603
C8605 1UF 10% 25V X5R 402
C8606 0.1UF 10% 16V X5R 402-1
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1V

XW8600 SM
GND_GPU_DPLL
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

L8602 120OHM-0.3A 0402
PP1V8_S0GPU
C8607 10UF 20% 10V X5R 603
C8608 1UF 10% 25V X5R 402
C8609 0.1UF 10% 16V X5R 402-1
XW8601 SM
GND_GPU_TSVSS
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

PP1V8_GPU_DPLL 75mA (GND_GPU_DPLL)
PP1V0_GPU_DPLL 125mA
PP1V8_GPU_TSVDD 20mA (GND_GPU_TSVSS)

U8000 WHISTLER 40NM-ES FCBGA (2 OF 9)

TP_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0	DPA
TP_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1	
TP_DVPCNTL<0>	AP8	DVPCNTL_0	
TP_DVPCNTL<1>	AW8	DVPCNTL_1	
TP_DVPCNTL<2>	AR3	DVPCNTL_2	
TP_DVPCLK	AR1	DVPCLK	
DVPDATA<0>	AU1	DVPDATA_0	OMIT
DVPDATA<1>	AU3	DVPDATA_1	
DVPDATA<2>	AW3	DVPDATA_2	
DVPDATA<3>	AP6	DVPDATA_3	
TP_DVPDATA<4>	AW5	DVPDATA_4	
TP_DVPDATA<5>	AU5	DVPDATA_5	
TP_DVPDATA<6>	AR6	DVPDATA_6	
TP_DVPDATA<7>	AW6	DVPDATA_7	
TP_DVPDATA<8>	AU6	DVPDATA_8	
TP_DVPDATA<9>	AT7	DVPDATA_9	
TP_DVPDATA<10>	AV7	DVPDATA_10	
TP_DVPDATA<11>	AN7	DVPDATA_11	
TP_DVPDATA<12>	AV9	DVPDATA_12	
TP_DVPDATA<13>	AT9	DVPDATA_13	
TP_DVPDATA<14>	AR10	DVPDATA_14	
TP_DVPDATA<15>	AW10	DVPDATA_15	
TP_DVPDATA<16>	AU10	DVPDATA_16	
TP_DVPDATA<17>	AP10	DVPDATA_17	
TP_DVPDATA<18>	AV11	DVPDATA_18	
TP_DVPDATA<19>	AT11	DVPDATA_19	
TP_DVPDATA<20>	AR12	DVPDATA_20	
TP_DVPDATA<21>	AW12	DVPDATA_21	
TP_DVPDATA<22>	AU12	DVPDATA_22	
TP_DVPDATA<23>	AP12	DVPDATA_23	
NC	AJ21	SWAPLOCKA	MULTI GFX
NC	AK21	SWAPLOCKB	
GPU_I2C_SCL	AK26	SCL	I2C
GPU_I2C_SDA	AJ26	SDA	
GPU_PCIE_TX_PWR	AH20	GPIO_0	GPIO
GPU_GPIO_TX_DEEMP	AH18	GPIO_1	
GPU_PCIE_GEN2	AN16	GPIO_2	
GPU_SMB_DAT	AH23	GPIO_3_SMBDATA	
GPU_SMB_CLK	AJ23	GPIO_4_SMBCLK	
GPU_AC_BATT	AH17	GPIO_5_AC_BATT	
GPU_VCORE_VID0	AJ17	GPIO_6	
EG_BKLT_EN	AK17	GPIO_7_BLON	
GPU_ROM_SO	AJ13	GPIO_8_ROMSO	
GPU_ROM_SI	AH15	GPIO_9_ROMSI	
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK	
GPU_CONFIG_0	AK16	GPIO_11	
GPU_CONFIG_1	AL16	GPIO_12	
GPU_CONFIG_2	AM16	GPIO_13	
DP_T29SNK0_HPD_GPU	AM14	GPIO_14_HPD2	
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0	
GPU_VCORE_VID2	AK14	GPIO_16	
SMC_GFX_THROTTLE_R_L	AG30	GPIO_17_THERMAL_INT	
DP_T29SNK1_HPD_GPU	AN14	GPIO_18_HPD3	
SMC_GFX_OVERTEMP_R_L	AM17	GPIO_19_CTF	
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1	
FBVDD_ALTVO	AJ14	GPIO_21_BB_EN	
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*	
PEX_CLKREQ_L_R	AN13	GPIO_23_CLKREQ*	
TP_GPU_JTAG_TRST_L	AM23	JTAG_TRST*	
TP_GPU_JTAG_TDI	AN23	JTAG_TDI	
TP_GPU_JTAG_TCK	AK23	JTAG_TCK	
TP_GPU_JTAG_TMS	AL24	JTAG_TMS	
TP_GPU_JTAG_TDO	AM24	JTAG_TDO	
NC_GPU_GENERICA	AJ19	GENERICA	
NC_GPU_GENERICB	AK19	GENERICB	
NC_GPU_GENERICC	AJ20	GENERICC	
DP_CA_DET_EG_R	AK20	GENERICD	
NC_GPU_GENERICE	AJ24	GENERICE_HPD4	
NC_GPU_GENERICF	AH26	GENERICF_HPD5	
NC_GPU_GENERICG	AH24	GENERICG_HPD6	
DP_EG_HPD	AK24	HPD1	
GPU_VREFG	AH13	VREFG	
	AM32	DPLL_PVDD	PLL/CLK
(GND_GPU_DPLL)	AN32	DPLL_PVSS	
	AN31	DPLL_VDDC	
NC	AV33	XTALIN	
NC	AU34	XTALOUT	
GPU_CLK27M	AW34	XO_IN	
GPU_CLK100M	AW35	XO_IN2	
GPU_TDIODE_P	AF29	DPLUS	THERMAL
GPU_TDIODE_N	AG29	DMINUS	
NC	AK32	TS_FDO	
NC	AL31	TSA/NC	
	AJ32	TSVDD	
(GND_GPU_TSVSS)	AJ33	TSVSS	

TXCAP_DPA3P	AU24	DP_EXTA_ML_C_P<3>	DPA
TXCAM_DPA3N	AV23	DP_EXTA_ML_C_N<3>	
TX0P_DPA2P	AT25	DP_EXTA_ML_C_P<2>	
TX0M_DPA2N	AR24	DP_EXTA_ML_C_N<2>	
TX1P_DPA1P	AU26	DP_EXTA_ML_C_P<1>	
TX1M_DPA1N	AV25	DP_EXTA_ML_C_N<1>	
TX2P_DPA0P	AT27	DP_EXTA_ML_C_P<0>	
TX2M_DPA0N	AR26	DP_EXTA_ML_C_N<0>	
TXCBP_DPB3P	AR30	DP_T29SNK0_ML_C_P<3>	DPB
TXCBM_DPB3N	AT29	DP_T29SNK0_ML_C_N<3>	
TX3P_DPB2P	AV31	DP_T29SNK0_ML_C_P<2>	
TX3M_DPB2N	AU30	DP_T29SNK0_ML_C_N<2>	
TX4P_DPB1P	AR32	DP_T29SNK0_ML_C_P<1>	
TX4M_DPB1N	AT31	DP_T29SNK0_ML_C_N<1>	
TX5P_DPB0P	AT33	DP_T29SNK0_ML_C_P<0>	
TX5M_DPB0N	AU32	DP_T29SNK0_ML_C_N<0>	
TXCCP_DPC3P	AU14	DP_T29SNK1_ML_C_P<3>	DPC
TXCCM_DPC3N	AV13	DP_T29SNK1_ML_C_N<3>	
TX0P_DPC2P	AT15	DP_T29SNK1_ML_C_P<2>	
TX0M_DPC2N	AR14	DP_T29SNK1_ML_C_N<2>	
TX1P_DPC1P	AU16	DP_T29SNK1_ML_C_P<1>	
TX1M_DPC1N	AV15	DP_T29SNK1_ML_C_N<1>	
TX2P_DPC0P	AT17	DP_T29SNK1_ML_C_P<0>	
TX2M_DPC0N	AR16	DP_T29SNK1_ML_C_N<0>	
TXCDP_DPD3P	AU20	NC	DPD
TXCDM_DPD3N	AT19	NC	
TX3P_DPD2P	AT21	NC	
TX3M_DPD2N	AR20	NC	
TX4P_DPD1P	AU22	NC	
TX4M_DPD1N	AV21	NC	
TX5P_DPD0P	AT23	NC	
TX5M_DPD0N	AR22	NC	
R	AD39	NC	DAC1
R*	AD37	NC	
G	AE36	NC	
G*	AD35	NC	
B	AF37	NC	
B*	AE38	NC	
HSYNC	AC36	GPU_AUD_1	
VSYNC	AC38	GPU_AUD_0	
RSET	AB34	NC	
AVDD	AD34	PP1V8_S0GPU	DAC2
AVSSQ	AE34		
VDD1DI	AC33		
VSS1DI	AC34		
R2/NC	AC30	NC	
R2*/NC	AC31	NC	
G2/NC	AD30	NC	
G2*/NC	AD31	NC	
B2/NC	AF30	NC	
B2*/NC	AF31	NC	
C/NC	AC32	NC	
Y/NC	AD32	NC	
COMP/NC	AF32	NC	
H2SYNC/GENLK_CLK	AD29	NC	
V2SYNC/GENLK_VSYNC	AC29	NC	
VDD2DI/NC	AG31	NC	
VSS2DI/NC	AG32	NC	
A2VDD/NC	AG33	NC	
A2VDDQ/NC	AD33	NC	
A2VSSQ/TSVSSQ	AF33	GND_GPU_TVSSQ	
R2SET/NC	AA29	NC	
DDC1CLK	AM26	DP_EG_DDC_CLK	DDC/AUX
DDC1DATA	AM26	DP_EG_DDC_DATA	
AUX1P	AM27	DP_EG_AUX_CH_P	
AUX1N	AL27	DP_EG_AUX_CH_N	
DDC2CLK	AM19	NC	
DDC2DATA	AL19	NC	
AUX2P	AN20	DP_T29SNK0_AUXCH_C_P	
AUX2N	AM20	DP_T29SNK0_AUXCH_C_N	
DDCCLK_AUX3P	AL30	DP_T29SNK1_AUXCH_C_P	
DDCDATA_AUX3N	AM30	DP_T29SNK1_AUXCH_C_N	
DDCCLK_AUX4P	AL29	NC	
DDCDATA_AUX4N	AM29	NC	
DDCCLK_AUX5P	AN21	LVDS_EG_DDC_CLK	
DDCDATA_AUX5N	AM21	LVDS_EG_DDC_DATA	
DDC6CLK	AJ30	NC	
DDC6DATA	AJ31	NC	
DDCCLK_AUX7P	AK30	NC	
DDCDATA_AUX7N	AK29	NC	

XW8602 SM
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

PP3V3_S0GPU
Straps for audio on DP and HDMI
R8604 10K 5% 1/16W MF-LF 402
R8605 10K 5% 1/16W MF-LF 402

U8000 WHISTLER 40NM-ES FCBGA (3 OF 9)

LVDS_CNTL	AK27	LVDS_EG_BLK_PWM	LVTMDP
	AJ27	EG_LCD_PWR_EN	
TXCLK_UP_DPF3P	AK35	NC_LVDS_EG_B_CLK_P	
TXCLK_UN_DPF3N	AL36	NC_LVDS_EG_B_CLK_N	
TXOUT_U0P_DPF2P	AJ38	LVDS_EG_B_DATA_P<0>	
TXOUT_U0N_DPF2N	AK37	LVDS_EG_B_DATA_N<0>	
TXOUT_U1P_DPF1P	AH35	LVDS_EG_B_DATA_P<1>	OMIT
TXOUT_U1N_DPF1N	AJ36	LVDS_EG_B_DATA_N<1>	
TXOUT_U2P_DPF0P	AG38	LVDS_EG_B_DATA_P<2>	
TXOUT_U2N_DPF0N	AH37	LVDS_EG_B_DATA_N<2>	
TXOUT_U3P	AF35	NC_LVDS_EG_B_DATA_P<3>	
TXOUT_U3N	AG36	NC_LVDS_EG_B_DATA_N<3>	
TXCLK_LP_DPE3P	AP34	LVDS_EG_A_CLK_P	
TXCLK_LN_DPE3N	AR34	LVDS_EG_A_CLK_N	
TXOUT_L0P_DPE2P	AW37	LVDS_EG_A_DATA_P<0>	
TXOUT_L0N_DPE2N	AU35	LVDS_EG_A_DATA_N<0>	
TXOUT_L1P_DPE1P	AR37	LVDS_EG_A_DATA_P<1>	
TXOUT_L1N_DPE1N	AU39	LVDS_EG_A_DATA_N<1>	
TXOUT_L2P_DPE0P	AP35	LVDS_EG_A_DATA_P<2>	
TXOUT_L2N_DPE0N	AR35	LVDS_EG_A_DATA_N<2>	
TXOUT_L3P	AN36	NC_LVDS_EG_A_DATA_P<3>	
TXOUT_L3N	AP37	NC_LVDS_EG_A_DATA_N<3>	

R8606 10K 5% 1/16W MF-LF 402

SYNC_MASTER=K92_SUMA SYNC_DATE=10/21/2010
PAGE TITLE: Whistler LVDS/DP/GPIO

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GPIOs

GPU_PCIE_TX_PWR	GP	GPU_PCIE_TX_PWR	MAKE_BASE=TRUE
GPU_GPIO_TX_DEEMP	GP	GPU_GPIO_TX_DEEMP	MAKE_BASE=TRUE
GPU_PCIE_GEN2	GP	GPU_PCIE_GEN2	MAKE_BASE=TRUE
GPU_SMB_DAT	GP	GPU_SMB_DAT	MAKE_BASE=TRUE
GPU_SMB_CLK	GP	GPU_SMB_CLK	MAKE_BASE=TRUE
GPU_AC_BATT	GP	GPU_AC_BATT	MAKE_BASE=TRUE
GPU_VCORE_VID0	GP	GPU_VCORE_VID0	MAKE_BASE=TRUE
EG_BKLT_EN	GP	EG_BKLT_EN	MAKE_BASE=TRUE
GPU_ROM_SO	GP	GPU_ROM_SO	MAKE_BASE=TRUE
GPU_ROM_SI	GP	GPU_ROM_SI	MAKE_BASE=TRUE
GPU_ROM_SCLK	GP	GPU_ROM_SCLK	MAKE_BASE=TRUE
GPU_CONFIG_0	GP	GPU_CONFIG_0	MAKE_BASE=TRUE
GPU_CONFIG_1	GP	GPU_CONFIG_1	MAKE_BASE=TRUE
GPU_CONFIG_2	GP	GPU_CONFIG_2	MAKE_BASE=TRUE
DP_T29SNK0_HPD_GPU	GP	DP_T29SNK0_HPD_GPU	MAKE_BASE=TRUE
GPU_VCORE_VID1	GP	GPU_VCORE_VID1	MAKE_BASE=TRUE

GPIOs

GPU_VCORE_VID2	GP	GPU_VCORE_VID2	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_R_L	GP	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE
DP_T29SNK1_HPD_GPU	GP	DP_T29SNK1_HPD_GPU	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP_R_L	GP	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE
GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE
FBVDD_ALTVO	GP	FBVDD_ALTVO	MAKE_BASE=TRUE
GPU_ROM_CS_L	GP	GPU_ROM_CS_L	MAKE_BASE=TRUE
PEX_CLKREQ_L_R	GP	PEX_CLKREQ_L_R	MAKE_BASE=TRUE
NC_GPU_GENERICA	GP	NC_GPU_GENERICA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICB	GP	NC_GPU_GENERICB	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICC	GP	NC_GPU_GENERICC	MAKE_BASE=TRUE NO_TEST=TRUE
DP_CA_DET_EG_R	GP	DP_CA_DET_EG_R	MAKE_BASE=TRUE
NC_GPU_GENERICE	GP	NC_GPU_GENERICE	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICF	GP	NC_GPU_GENERICF	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_GENERICG	GP	NC_GPU_GENERICG	MAKE_BASE=TRUE NO_TEST=TRUE
DP_EG_HPD	GP	DP_EG_HPD	MAKE_BASE=TRUE

T29 HPD GPU isolation

CRITICAL

PP3V3_S0 — C8741 0.1UF 20% 10V X5R CERM 402

DP_T29SNK0_HPD → U8741 (74LVC2G08GT SOT833) → DP_T29SNK0_HPD_GPU

PP3V3_GPU_VDD33_R — R8741 0 5% 1/16W MF-LF 402 — PP3V3_S0GPU

PP3V3_S0 — U8741 (74LVC2G08GT SOT833)

DP_T29SNK1_HPD → U8741 → DP_T29SNK1_HPD_GPU

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK	
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI	
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO	
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS	
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L	
NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_CLK_P	
NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_CLK_N	
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_P<3>	
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_A_DATA_N<3>	
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_P<3>	
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE	NC_LVDS_EG_B_DATA_N<3>	

Config Straps

PP3V3_S0GPU

R8700 10K, R8701 10K, R8702 10K — NOSTUFF

- GPU_PCIE_TX_PWR
- GPU_GPIO_TX_DEEMP
- GPU_PCIE_GEN2

R8703 10K, R8704 10K, R8705 10K — NOSTUFF

- GPU_SMB_DAT
- GPU_SMB_CLK
- GPU_AC_BATT

R8706 10K, R8707 10K, R8708 10K — NOSTUFF

- EG_BKLT_EN
- GPU_ROM_SO
- GPU_ROM_SI

R8709 10K, R8710 10K, R8711 10K — NOSTUFF

- GPU_ROM_SCLK
- GPU_CONFIG_0
- GPU_CONFIG_1

R8712 10K, R8713 10K, R8714 10K — GPU_ROM:YES / NOSTUFF

- GPU_CONFIG_2
- FBVDD_ALTVO
- PEX_CLKREQ_L_R

PP3V3_S0GPU

R8723 33 — GPU_ROM_SI — GPU_ROM:YES — GPU_ROM_SI_R

R8724 33 — GPU_ROM_SCLK — GPU_ROM:YES — GPU_ROM_SCLK_R

R8725 33 — GPU_ROM_CS_L — GPU_ROM:YES — GPU_ROM_CS_L_R

R8720 10K, R8721 0 — GPU_ROM:YES

C8721 0.1UF 20% 10V CERM 402 — GPU_ROM:YES

R8722 0 — NO STUFF — GPU_ROM_WP_L

U8701 M25P10A UFDFPN8 — CRITICAL — OMIT_TABLE

GPU_ROM_SO_R — R8726 33 — GPU_ROM_SO — GPU_ROM:YES

? BOM OPTION NEED CONFIRMATION HERE!

PP3V3_S0

R8750 2.2K, R8751 2.2K — NO STUFF

R8752 4.7K, R8753 4.7K

- DP_EG_DDC_CLK
- DP_EG_DDC_DATA
- DP_IG_DDC_CLK
- DP_IG_DDC_DATA

PP3V3_S0GPU

R8796 2.2K — NO STUFF

R8797 2.2K

- SMC_GFX_OVERTEMP_R_L
- SMC_GFX_THROTTLE_R_L

R8798 0 — SMC_GFX_OVERTEMP_R_L → SMC_GFX_OVERTEMP_L

R8799 0 — SMC_GFX_THROTTLE_R_L → SMC_GFX_THROTTLE_L

- EG_LCD_PWR_EN
- EG_BKLT_EN
- FBVDD_ALTVO

R8792 10K, R8793 10K, R8794 10K

ISOLATION R's for GPU Int Temp Sense

GPU_SMB_DAT — R8780 0 — SMBUS_SMC_0_S0_SDA

GPU_SMB_CLK — R8781 0 — SMBUS_SMC_0_S0_SCL

NOSTUFF

PP3V3_S0GPU

L8703 120OHM-0.3A — PP3V3_GPU_OSC_27M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

L8702 120OHM-0.3A — PP3V3_GPU_OSC_100M (MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C8702 0.1UF, C8703 0.1UF

GPU Reference Clocks

U8700 SL16010DC DFN — CRITICAL

- GPU_OSC_27M_XTALIN
- GPU_OSC_27M_XTALOUT

CRITICAL Y8700 SM-2.5X2.0MM 27MHZ-15PPM-18PF

C8700 30PF, C8701 30PF

- GPU_CLK100M_R → R8730 0 → GPU_CLK100M
- GPU_CLK27M_R → R8731 0 → GPU_CLK27M

SYNC_MASTER=K91_MLB	SYNC_DATE=07/17/2010
PAGE TITLE	Whistler GPIOs & STRAPs
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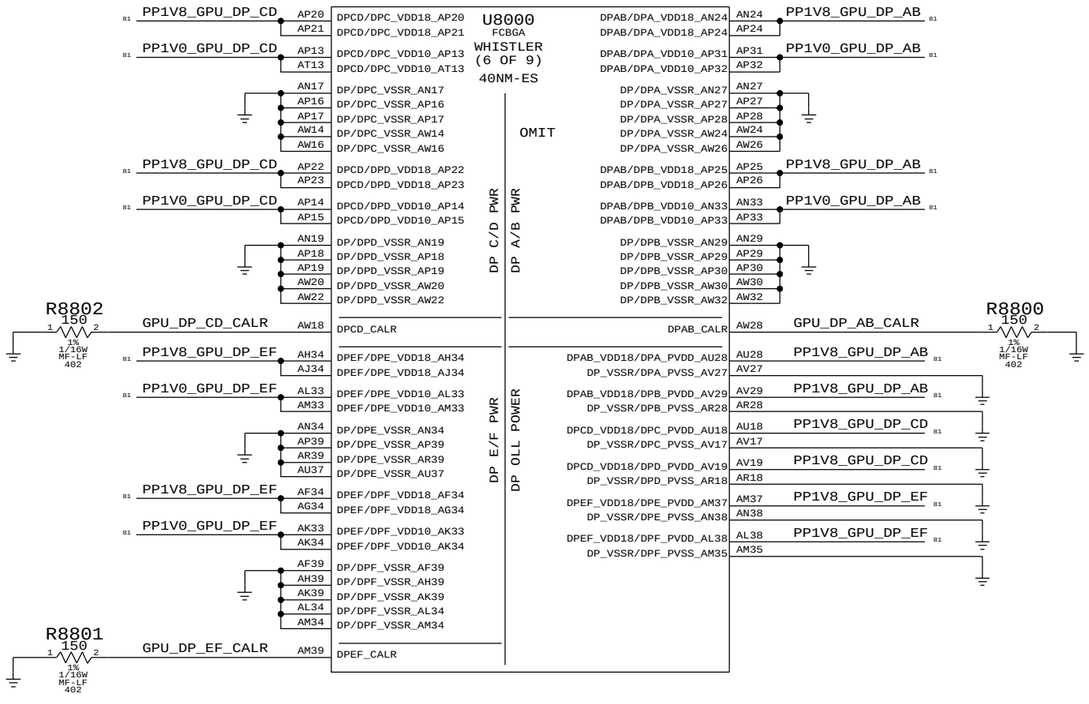

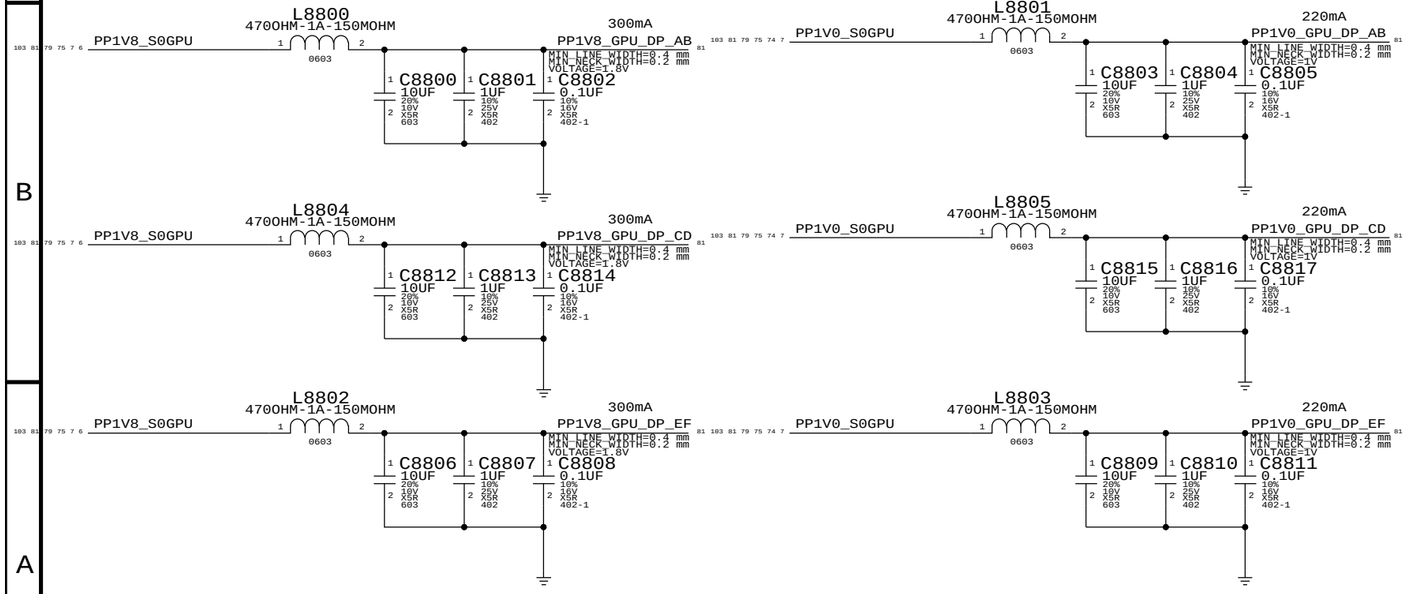

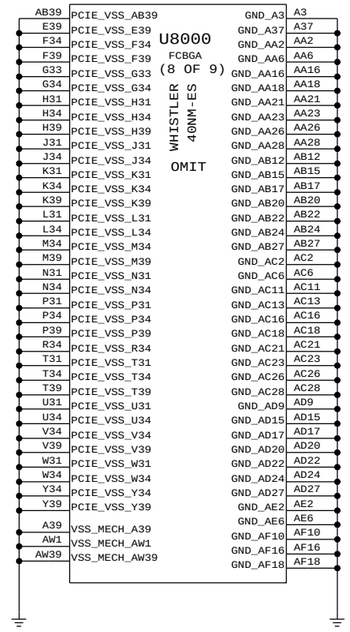

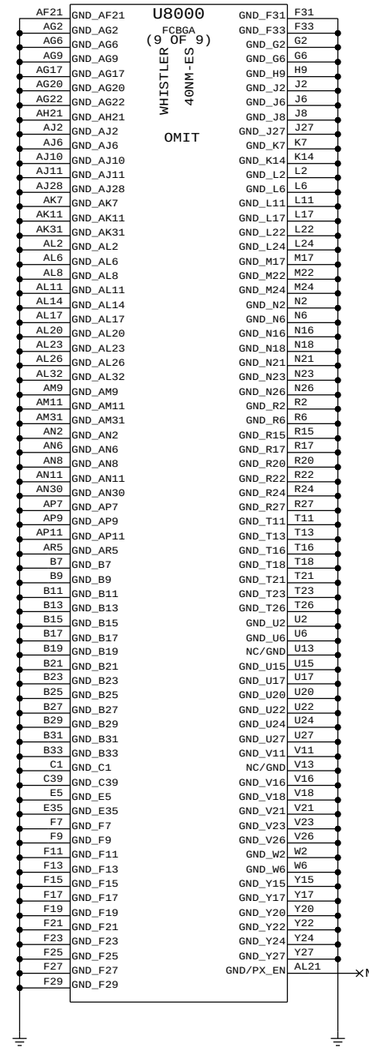

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_BEN SYNC_DATE=06/01/2010

PAGE TITLE: Whistler DP PWR/GNDs

Apple Inc.

DRAWING NUMBER: D
SIZE: D
REVISION:
BRANCH:
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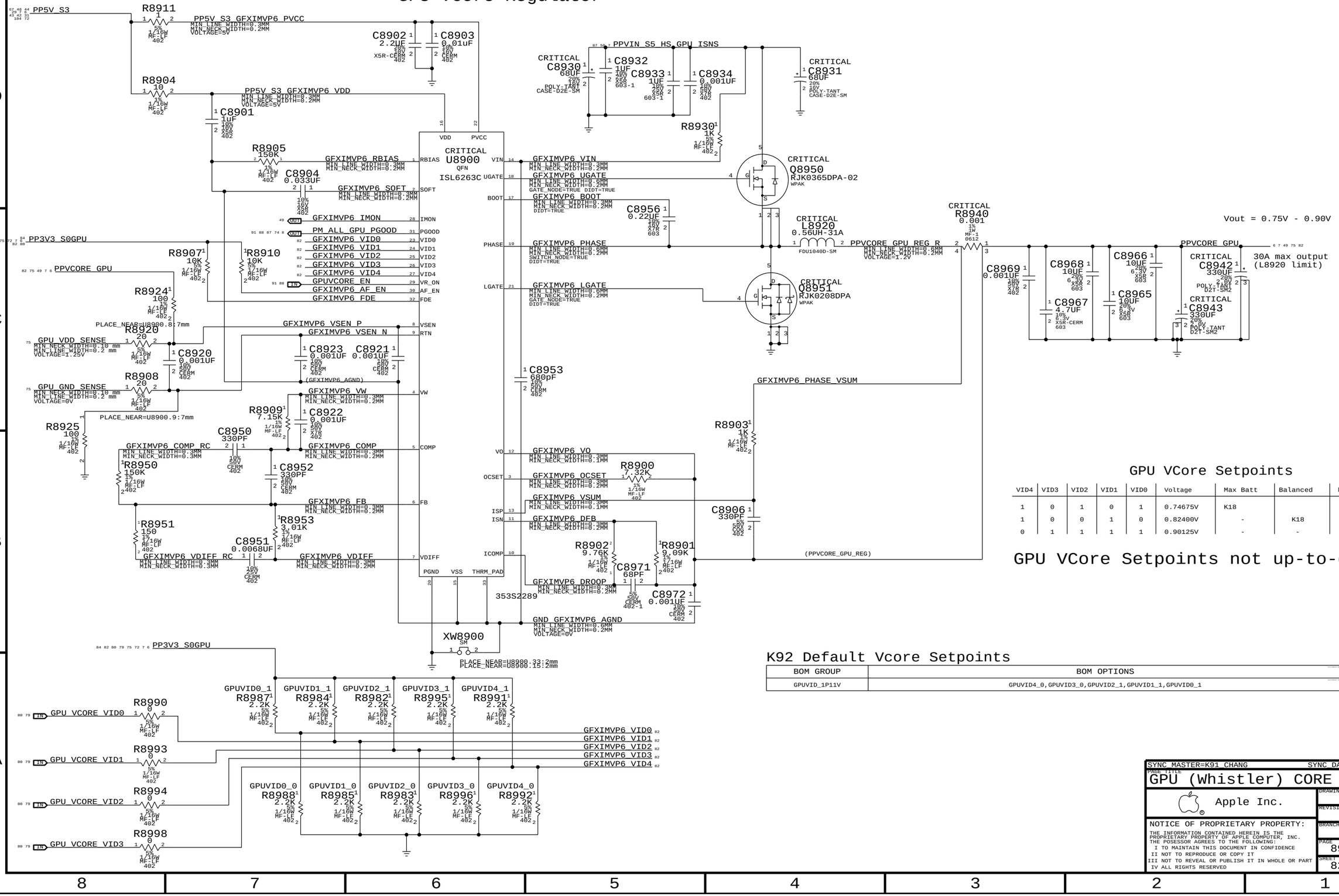
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K92 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE: GPU (Whistler) CORE SUPPLY

Apple Inc.

DRAWING NUMBER | SIZE: D

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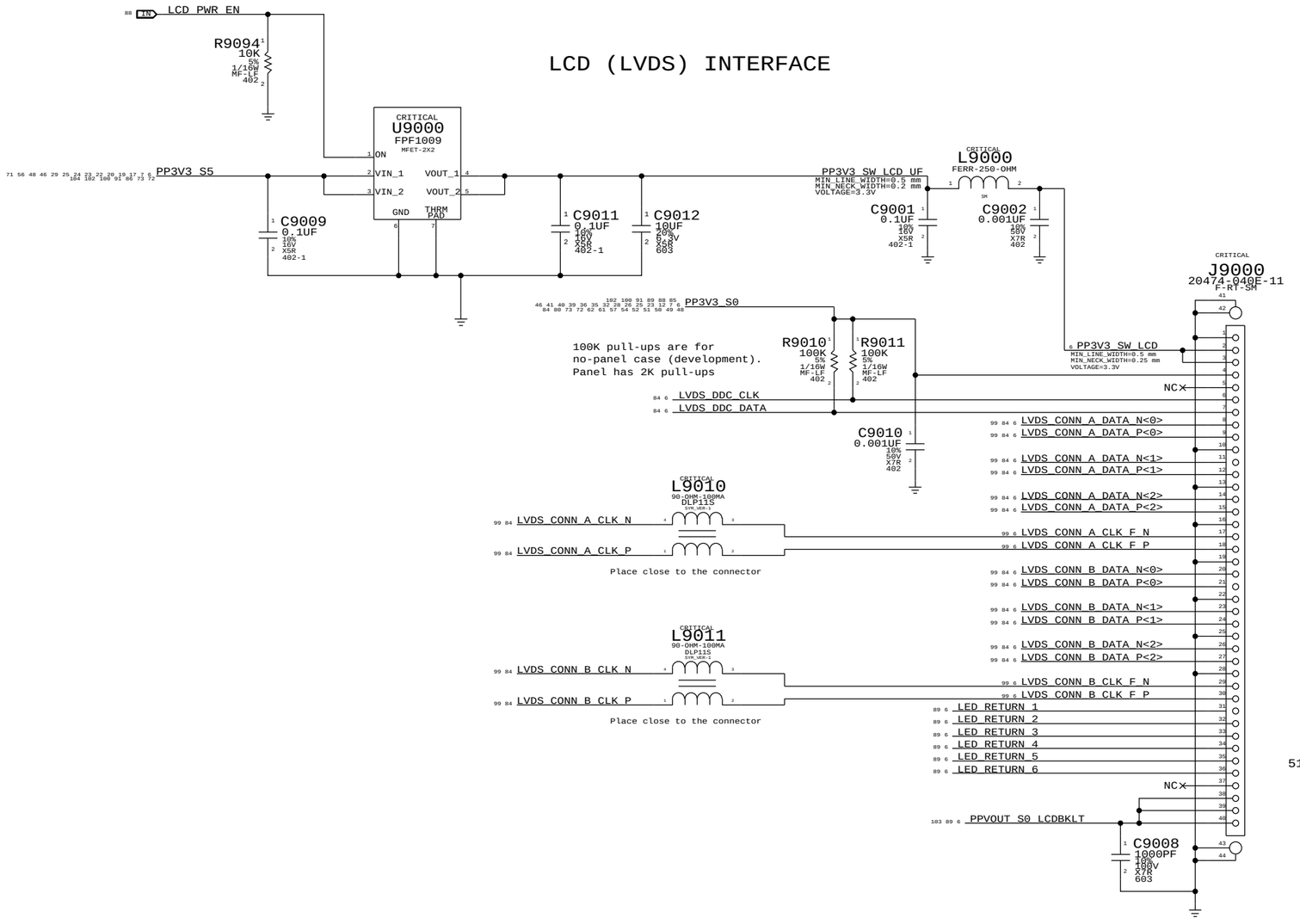
LCD (LVDS) INTERFACE



518S0651

SYNC_MASTER=K17_MLB	SYNC_DATE=04/26/2010
PAGE TITLE	LVDS Display Connector
Apple Inc.	DRAWING NUMBER / SIZE: D
	REVISION
	BRANCH
	PAGE: 90 OF 132
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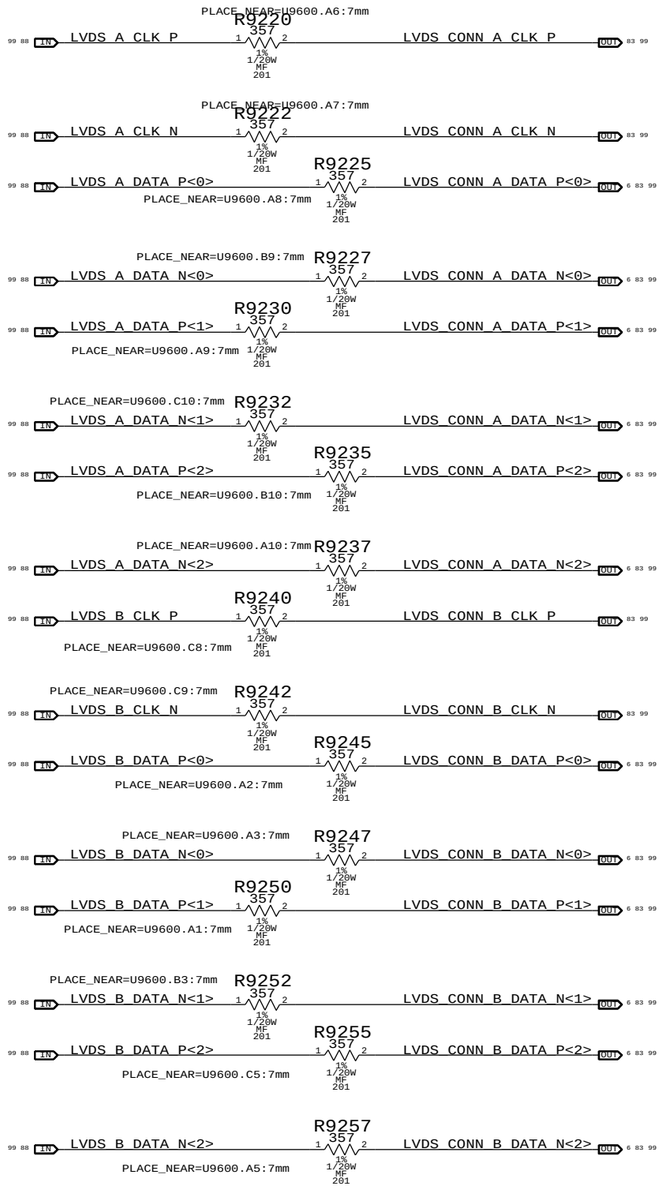
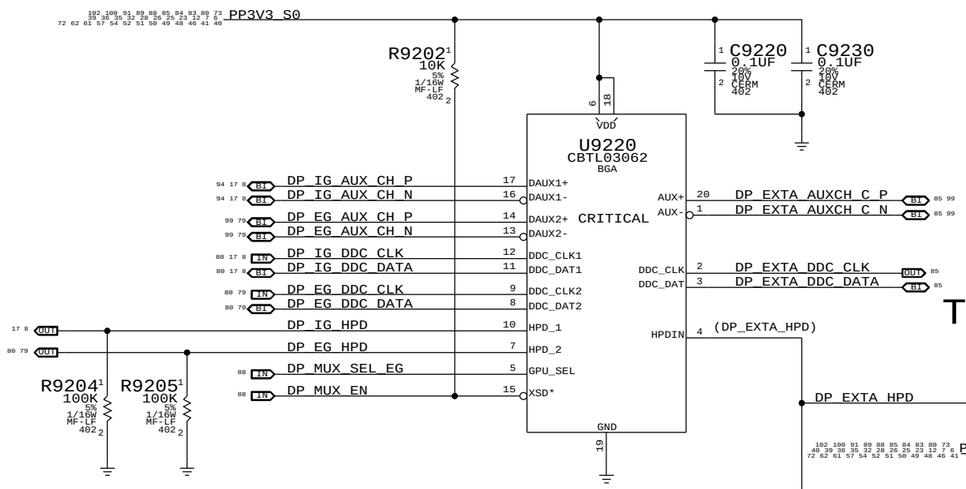
LVDS Transmitter Termination

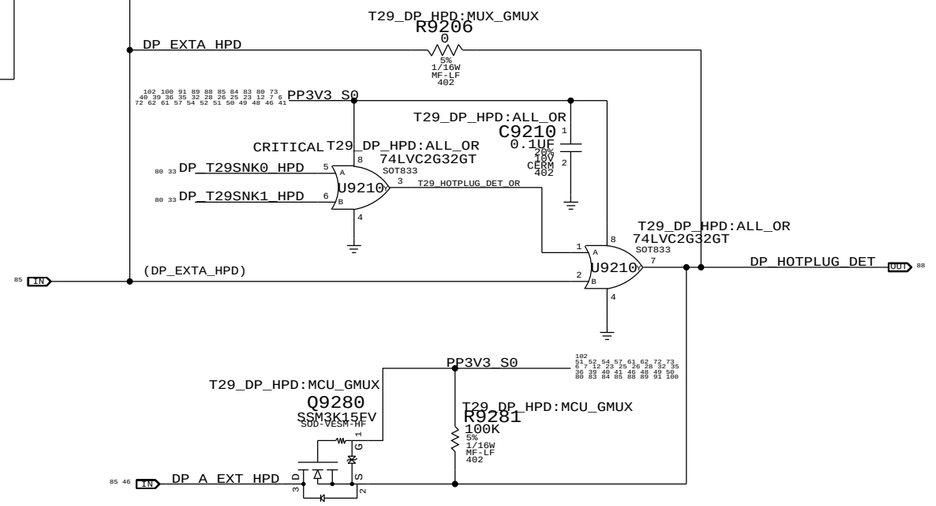
All emulated LVDS outputs require this termination



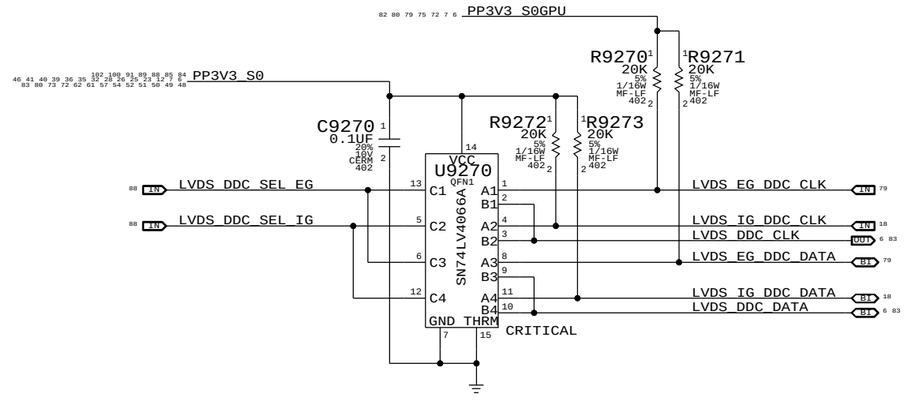
DP AUX, DDC, & HPD muxing to IG/EG



T29/DP HOT PLUG IN



LVDS DDC MUX



SYNC_MASTER=K92_YUN	SYNC_DATE=06/25/2010
PAGE TITLE	Muxed Graphics Support
Apple Inc.	DRAWING NUMBER: D; SIZE: D
	REVISION:
	BRANCH:
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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1uF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1uF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1uF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1uF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1uF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1uF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1uF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1uF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1uF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1uF DP_EXTA_AUXCH_N

PP3V3_S0 R9309 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_P
R9308 1M 5% MF-LF 1/16W 402 DP_EXTA_AUXCH_N

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

T29_D2R_C_N<0> T29_D2R_C_P<0>
T29_R2D_C_N<0> L9372 1.0NH+/-0.1NH 0201-1 CRITICAL T29_R2D_C_F_N<0>
T29_R2D_C_P<0> L9373 1.0NH+/-0.1NH 0201-1 CRITICAL T29_R2D_C_F_P<0>
OVERSIZE_PAD=0.875 mm^2 (Both L 153S1376)

T29_A_BIAS_R2D_P0
GND_VOID=TRUE (C9370/C9371)
C9370 0.47uF 20% 4V CERM-X5R-1 201
C9371 0.47uF 20% 4V CERM-X5R-1 201
(C9372.2) GND_VOID=TRUE C9372 0.47uF 10% 6.3V CERM-X5R 402
(C9373.2) GND_VOID=TRUE C9373 0.47uF 10% 6.3V CERM-X5R 402
T29_A_BIAS_R2D_N0

GND_VOID=TRUE R9372 1.5K 5% 1/20W MF 201 T29_R2D_P<0>
SIGNAL_MODEL=EMPTY
GND_VOID=TRUE R9373 1.5K 5% 1/20W MF 201 T29_R2D_N<0>
SIGNAL_MODEL=EMPTY

T29 signals are P/N-swapped after AC caps to improve layout.

T29_D2R_N<1> T29_D2R_P<1>
T29_R2D_C_N<1> L9382 1.0NH+/-0.1NH 0201-1 CRITICAL T29_R2D_C_F_N<1>
T29_R2D_C_P<1> L9383 1.0NH+/-0.1NH 0201-1 CRITICAL T29_R2D_C_F_P<1>
OVERSIZE_PAD=0.875 mm^2 (Both L 153S1376) (All 4 L's)

T29_A_BIAS_R2D_P1
GND_VOID=TRUE (C9380/C9381)
C9380 0.47uF 20% 4V CERM-X5R-1 201
C9381 0.47uF 20% 4V CERM-X5R-1 201
(C9383.2) GND_VOID=TRUE C9382 0.47uF 10% 6.3V CERM-X5R 402
(C9383.2) GND_VOID=TRUE C9383 0.47uF 10% 6.3V CERM-X5R 402
T29_A_BIAS_R2D_N1

GND_VOID=TRUE R9382 1.5K 5% 1/20W MF 201 T29_R2D_P<1>
SIGNAL_MODEL=EMPTY
GND_VOID=TRUE R9383 1.5K 5% 1/20W MF 201 T29_R2D_N<1>
SIGNAL_MODEL=EMPTY

T29 Path Biasing

T29_D2R_C_P<0> T29_D2R_C_N<0>
D9364 D9372 D9373 D9365 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9364.2)
T29: TX_0
T29DPA_ML_C_P<0> T29DPA_ML_C_N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K 5% 1/20W MF 201 GND_VOID=TRUE
R9375 1.5K 5% 1/20W MF 201 GND_VOID=TRUE
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY

T29_D2R_C_P<1> T29_D2R_C_N<1>
D9360 D9382 D9383 D9361 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9360.2)
T29: TX_1
T29DPA_ML_C_P<2> T29DPA_ML_C_N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K 5% 1/20W MF 201 GND_VOID=TRUE
R9385 1.5K 5% 1/20W MF 201 GND_VOID=TRUE
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)

DP Path Biasing

R9361 1.5K 5% 1/20W MF 201 DP_A_BIAS_P_2
R9360 1.5K 5% 1/20W MF 201 DP_A_BIAS_N_2
R9365 1.5K 5% 1/20W MF 201 DP_A_BIAS_P_0
R9364 1.5K 5% 1/20W MF 201 DP_A_BIAS_N_0
R9362 51 5% 1/20W MF 201 DP_A_BIAS_N_2 VOLTAGE=3.3V
R9366 51 5% 1/20W MF 201 DP_A_BIAS_P_2 VOLTAGE=3.3V
R9363 51 5% 1/20W MF 201 DP_A_BIAS_N_0 VOLTAGE=3.3V
R9367 51 5% 1/20W MF 201 DP_A_BIAS_P_0 VOLTAGE=3.3V

DP A Super-Driver

PP3V3_S0
C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 20% 10V CERM 402
C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K 5% 1/16W MF-LF 402
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL VDD

DP_EXTA_ML_P<0>	IN_D0P	OUT_D0P	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	IN_D0N	OUT_D0N	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	IN_D1P	OUT_D1P	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	IN_D1N	OUT_D1N	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	IN_D2P	OUT_D2P	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	IN_D2N	OUT_D2N	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	IN_D3P	OUT_D3P	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	IN_D3N	OUT_D3N	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	IN_SCL	AC_AUXP	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	IN_SDA	AC_AUXN	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	IN_AUXP	OUT_AUXP_SCL	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	IN_AUXN	OUT_AUXN_SDA	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	IN_HPD	(IPD) OUT_HPD	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	I2C_CTL_EN (IPU)	CA_DET	DP_A_CA_DET
DPSDRVA_I2C_ADDR0	I2C_ADDR0 (IPD)	CEXT	DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	I2C_ADDR1 (IPD)		
I2C_DPSDRVA_SCL	SCL_CTL		
I2C_DPSDRVA_SDA	SDA_CTL		
DPSDRVA_REXT	REXT		
DP_AUXCH_ISOL	AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	PD (IPD)		

PLACE_NEAR=U9310.11:2 mm
C9319 2.2UF 20% 6.3V CERM 402-LF
GND THMPAD

SDRV_PD R9318 0 5% 1/16W MF-LF 402
R9319 4.99K 1% 1/16W MF-LF 402
PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9354 30 5% 1/20W MF 201
R9353 270 5% 1/20W MF 201
R9355 30 5% 1/20W MF 201
R9350 30 5% 1/20W MF 201
R9351 30 5% 1/20W MF 201
R9352 270 5% 1/20W MF 201
R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

DP_SDRVA_ML_R_P<0> C9364 0.22uF 20% 6.3V X5R 201 DP_SDRVA_ML_P<0>
DP_SDRVA_ML_R_N<0> C9365 0.22uF 20% 6.3V X5R 201 DP_SDRVA_ML_N<0>
DP_SDRVA_ML_R_P<2> C9360 0.22uF 20% 6.3V X5R 201 DP_SDRVA_ML_P<2>
DP_SDRVA_ML_R_N<2> C9361 0.22uF 20% 6.3V X5R 201 DP_SDRVA_ML_N<2>

PP3V3_S0
C9359 0.1UF 10% 16V X5R 402
DP_A_PWRDWN
CRITICAL U9359 74LVC1G04DBDCK SC70
DP_A_BIAS
IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power
C9390 0.1UF 10% 16V CERM 402
C9391 0.1UF 10% 16V CERM 402
R9399 100K 5% 1/16W MF-LF 402

U9390 CBTL04DP081 HVQFN CRITICAL OMIT_TABLE

DP_SDRVA_ML_N<3>	DIN1_0+	DOUT_0+	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	DIN1_0-	DOUT_0-	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	DIN1_1+	DOUT_1+	T29DPA_ML_N<1>
DP_SDRVA_ML_P<1>	DIN1_1-	DOUT_1-	T29DPA_ML_P<1>
DP_SDRVA_AUXCH_P	AUX1+	AUX+	DP_A_EXT_AUXCH_P
DP_SDRVA_AUXCH_N	AUX1-	AUX-	DP_A_EXT_AUXCH_N
DP_SDRVA_HPD	HPD_1	HPD_IN	DP_A_EXT_HPD
(T29_A_LSX_P2R)	DIN2_1+		
(T29_A_LSX_R2P)	DIN2_1-		
T29_D2R1_BIASP	AUX2+		
T29_D2R1_BIASN	AUX2-		
NC	HPD_2		
DP_A_PWRDWN	GPU_SEL		
T29_A_BIAS	AUX_SEL		
	NC		

T29: Unused
T29: LSX_A_R2P/P2R (P/N)
T29: RX_1 Bias Sink
LO=Port A HI=Port B
THMPAD GND
SIGNAL_MODEL=T29DP_MUX

T29_A_RSVD_N T29_A_RSVD_P
R9392 51 5% 1/16W MF-LF 402
R9393 51 5% 1/16W MF-LF 402
R9396 1K 5% 1/16W MF-LF 402
R9397 1K 5% 1/16W MF-LF 402
R9398 100K 5% 1/16W MF-LF 402

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

U9390 BOM table in csa 5!!!

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100 ohm pull-downs would defeat DP Sink's detection of DP Source.

Port A MCU

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power
C9330 0.1UF 20% 10V CERM 402
C9331 0.1UF 20% 10V CERM 402

U9330 LPC1112A HVQFN25 CRITICAL VDD OMIT_TABLE

DP_A_CA_DET	RESET#/PIO0_0	R/PIO1_0/AD1	T29DPA_CONFIG1_RC
	PIO0_1/CLKOUT	R/PIO1_1/AD2	T29DPA_CONFIG2_RC
T29_LSEO<0>	PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3	T29_A_HV_EN_R
I2C_T29_SCL	PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4	T29_A_UC_ADDR
I2C_T29_SDA	PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP	DP_A_EXT_HPD
T29DPA_HPD	PIO0_6/SCK	PIO1_6/RXD	T29_A_LSX_P2R
T29_A_BIAS	PIO0_7/CTS#	PIO1_7/TXD	T29_A_LSX_R2P
T29_LSOE<0>	PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0	T29_LSEO<1>
T29_LSOE<1>	PIO0_9/MOSI/CT16B0_MAT1		
	SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
T29_MCU_INT_L	R/PIO0_11/AD0 (OD)	XTALIN	
	VSS THRM PAD		

R9338 10K 5% 1/16W MF-LF 402
R9334 10K 5%
T29_A_HV_EN
P2R = Plug to Receptacle
R2P = Receptacle to Plug
I2C Addr: 0x26/0x27 (Wr/Rd)
R9339 1M 5% 1/16W MF-LF 402
R9335 1K 5% 1/16W MF-LF 402
R9336 10K 5% 1/16W MF-LF 402

=T29_WAKE_L:
use PCIe WAKE#
PCIE_WAKE_L
OMIT R9330 0 5% 1/16W MF-LF 402
SWCLK
SWDIO
T29_A_UC_ADDR
R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

AUXCH Snoop Port, used by PS8301 during training.
C9363 0.1uF C9362 0.1uF C9367 0.1uF C9366 0.1uF C9369 0.1uF C9368 0.1uF
10% 16V X5R 402

SYNC_MASTER=K91_MLB SYNC_DATE=10/22/2010
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Port A HV Power Switch

PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP15V_T29
20V Max

R9416 470K 5% 1/16W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 TPS2590 QFN (CRITICAL)
VIN VOUT EN* (IPU-Weak!) FLT* RTRY* ILIM CT IFLT THRM GND PAD

C9411 0.1UF 10% 50V X7R 603-1

PPHV_SW_DPAPWR
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=15V

CRITICAL D9410 SM STPS2L30AF

TP_DPAPWRSW_FLT_L

DPAPWRSW_HVEN_L_R

DPAPWRSW_CT

C9412 0.47UF 10% 16V CERM-X5R 402

<CT>

DPAPWRSW_ILIM

DPAPWRSW_IFLT

R9410 100K 5% 1/10W MF-LF 402

R9411 200K 1% 1/10W MF-LF 402

<RFLT>

<RLIM>

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

Q9415 SSM3K15FV SOD-VESM-HF

Bleeder Resistor
2.5V / 249 ohm = 10mA
P = ~27mW

R9419 249 1% 1/16W MF-LF 402

DPAPWR_BLDR_E
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Q9419 DMB53D0UV SOT-563

DPAPWR_BLDR_B

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

T29_A_HV_EN

3.3V/HV Power MUX

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL D9425 POWERDI-123 DFLS1100

CRITICAL Q9425 SI8409DB BGA

3.3V/HV MUXed

R9425 4.7K 5% 1/16W MF-LF 402

Blocking FET, off when Source >3.4V or HV_EN high.

DPAPWRSW_P3V3_ON_L

R9424 22 5% 1/16W MF-LF 402

DPAPWR_ON_L_C

C9424 0.47UF 10% 6.3V CERM-X5R 402

R9427 100K 1% 1/16W MF-LF 402

R9428 21.5K 1% 1/16W MF-LF 402

DPAPWRSW_VREF

C9426 0.1UF 20% 10V CERM 402

CRITICAL U9426 ZXRE060A SOT353 (GND PGND FB)

DPAPWRSW_HV_DET_R_L

R9429 4.7K 5% 1/10W MF-LF 402

DPAPWRSW_HV_DET_L

NO STUFF C9429 0.1UF 20% 10V CERM 402

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

R9418 1K 5% 1/10W MF-LF 402

DPAPWRSW_HV_DET

L9400 FERR-120-OHM-3A 0603

PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C9400 0.01UF 10% 50V X7R 402

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

Port A 3.3V Power Switch

CRITICAL U9480 TPS2051B SOT23 (OUT IN OC* EN GND)

T29_A_HV_EN

SMC_S4_WAKESRC_EN

DP_PWR must be S4/S5 to support wake from T29 devices.

PP3V3_S5

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 10% 16V CERM 402
C9481 0.1UF 10% 16V CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

3.3V Always

R9426 1K 5% 1/16W MF-LF 402

R9430 4.7K 5% 1/16W MF-LF 402

T29_A_BIAS

CRITICAL U9435 ZXRE060A SOT353 (PGND GND FB)

C9435 0.1UF 20% 10V CERM 402

DPAPWRSW_P3V3_ON

C9436 1UF 10% 10V X5R 402

Q9430 SSM6N37FEAPE SOT563

Q9426 MMDT3946XG SOT363

R9437 82 5% 1/16W MF-LF 402

DPAPWRSW_NPN_E

R9433 220 5% 1/16W MF-LF 402

R9432 10K 5% 1/16W MF-LF 402

R9435 100K 1% 1/16W MF-LF 402

DPAPWR_FB_DIV

R9436 24.9K 1% 1/16W MF-LF 402

T29_A_HV_EN

DisplayPort/T29 A Connector

Circuit threshold range: 2.877-2.941V (2.903V nominal)

For J9400 T29 SMT pads (3, 5, 7, 8, 19):
GND_VOID=TRUE

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	GND 1
4	CONFIG1	ML_LANE0P 3
6	CONFIG2	ML_LANE0N 5
8	GND	GND 7
10	ML_LANE3P	ML_LANE1P 9
12	ML_LANE3N	ML_LANE1N 11
14	GND	GND 13
16	AUX_CHP	ML_LANE2P 15
18	AUX_CHN	ML_LANE2N 17
20	DP_PWR	RETURN 19
SHIELD PINS		22 21

T29 Dir DP Dir

T29_D2R_C_P<0>
T29_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9403 12 5% 1/16W MF-LF 402 GND_DPACONN_8

R9404 12 5% 1/16W MF-LF 402 GND_DPACONN_14

T29: Unused

T29_A_BIAS_D2R_P1
T29_A_BIAS_D2R_N1

R9498 2.2K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

R9499 2.2K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

T29_D2R_C_P<1>
T29_D2R_C_N<1>

D9498 BAR90-02LRH TSLP-2-7 SIGNAL_MODEL=T29PIN

D9499 BAR90-02LRH TSLP-2-7 SIGNAL_MODEL=T29PIN

CRITICAL L9498 650NH-5%-0.430MA-0.052OHM 0603

CRITICAL L9499 650NH-5%-0.430MA-0.052OHM 0603

T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N

R9402 12 5% 1/16W MF-LF 402 T29DPA_HPD_R

R9401 12 5% 1/16W MF-LF 402 DPACONN_20_RC

DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

C9498 30PF 5% 50V CERM 402

C9499 30PF 5% 50V CERM 402

C9402 0.01UF 10% 50V X7R 402

C9401 0.01UF 10% 50V X7R 402

T29DPA_HPD

T29DPA_CONFIG1_RC

T29DPA_CONFIG2_RC

R9452 1M 5% 1/20W MF 201

R9451 1M 5% 1/20W MF 201

C9494 330PF 10% 16V X7R 201

C9495 330PF 10% 16V X7R 201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/16W MF-LF 402

R9405 12 5% 1/20W MF 201 GND_DPACONN_1

R9406 12 5% 1/20W MF 201 GND_DPACONN_7

R9407 12 5% 1/20W MF 201 GND_DPACONN_13

GND_DPACONN_19

R9408 12 5% 1/20W MF 201

DP Dir T29 Dir

T29: TX_0

T29DPA_ML_P<0>
T29DPA_ML_N<0>

T29: LSX_R2P/P2R (P/N)

T29DPA_ML_P<1>
T29DPA_ML_N<1>

T29: TX_1

T29DPA_ML_P<2>
T29DPA_ML_N<2>

C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201

C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201

T29DPA_ML_C_P<0>
T29DPA_ML_C_N<0>
T29DPA_ML_C_P<2>
T29DPA_ML_C_N<2>

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)

L9408 FERR-120-OHM-3A 0603

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=K91_MLB SYNC_DATE=10/22/2010

PAGE TITLE: DisplayPort/T29 A Connector

Apple Inc.

DRAWING NUMBER: SIZE: D
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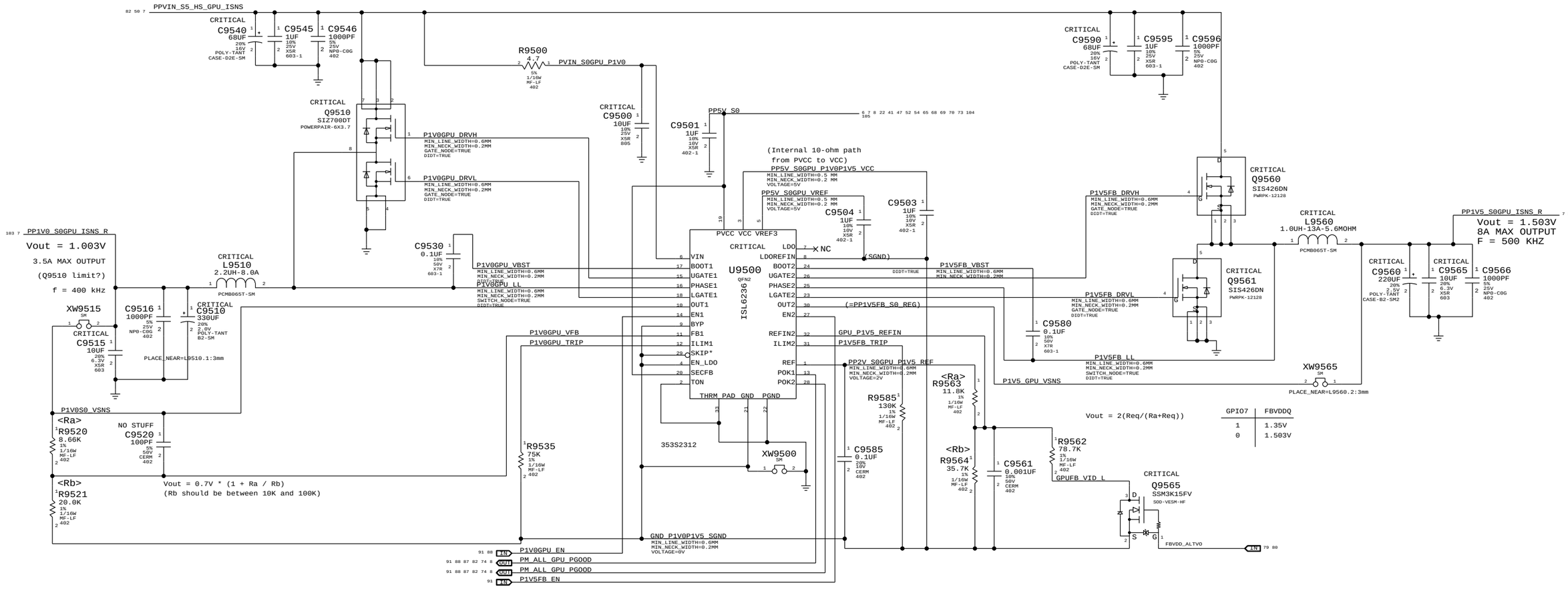

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE
1V0 GPU / 1V5 FB Power Supply

Apple Inc.

DRAWING NUMBER | SIZE D

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GMUX CPLD

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.E1:5mm	LVDS_IG_A_DATA_N<0>	
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>	
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>	
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>	
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>	
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.B2:5mm	LVDS_IG_B_DATA_N<2>	
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N	
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>	
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>	
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.F12:5mm	LVDS_EG_A_DATA_N<2>	
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>	
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>	
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>	

Required Pullups

SIGNAL_MODEL=EMPTY

PP3V3_S0

EG_PWRSEQ_EN	R9684	1K	
JTAG_GMUX_TDI	R9685	10K	
JTAG_GMUX_TDO	R9686	10K	
GMUX_DEBUG_RESET_L	R9680	1K	

NO STUFF R9679 10K (SILK_PART=GMUX_RST)

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K
LVDS_DDC_SEL_IG	R9682	10K
LVDS_DDC_SEL_EG	R9683	10K
EG_RESET_L	R9691	100K
LCD_BKLT_PWM	R9693	100K

NO STUFF

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

PP3V3_S0_GMUX_R: MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V
PP1V8_S0_GMUX_R: MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=1.8V
PP3V3_S0_GMUX_ULC_VCCPLL: MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V
PP3V3_S0_GMUX_LRC_VCCPLL: MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V

R9600 0 5% 1/16W MF-LF 402
R9610 0 5% 1/16W MF-LF 402

C9610–C9629 0.1UF 20% 10V CERM 402
C9600 4.7UF 20% 4V X5R 402
C9604–C9609 0.1UF 20% 10V CERM 402
L9621 FERR-220-OHM 0402
L9620 FERR-220-OHM 0402
C9631 0.1UF 20% 10V CERM 402
C9630 0.1UF 20% 10V CERM 402

R9645 10K 1% 1/20W MF 201
R9640 10K 1% 1/20W MF 201
NO STUFF R9646 10K 1% 1/20W MF 201
NO STUFF R9641 10K 1% 1/20W MF 201
NO STUFF R9647 10K 1% 1/20W MF 201

CRITICAL J9600 1909782 M-RT-SM — GMUX_JTAG_CONN

1	PP3V3_S0
2	JTAG_GMUX_TDO
3	JTAG_GMUX_TDI
4	JTAG_GMUX_TMS
5	
6	JTAG_ISP_TCK
8	

OMIT CRITICAL
U9600 XP25-5 CSBGA

JTAG_ISP_TCK	K14	TCK
JTAG_GMUX_TDI	L13	TDI
JTAG_GMUX_TDO	K13	TDO
JTAG_GMUX_TMS	L12	TMS
GMUX_TOE	K2	TOE
GMUX_CFG0	K1	CFG0

BANK5

LCD_BKLT_EN	P2	PB7A
LCD_BKLT_PWM	N2	PB7B
LVDS_DDC_SEL_EG	P4	PB14A
LVDS_DDC_SEL_IG	N4	PB14B
DP_MUX_EN	N3	PB15A (OD)
DP_MUX_SEL_EG	M4	PB15B
EG_RESET_L	P5	PB16A
P3V3GPU_EN	M5	PB16B
GPUVCORE_EN	P6	PB17A
P1V0GPU_EN	M6	PB17B
P1V5FB1V8GPU_R_EN	P7	PB18A
PEG_CLKREQ_L	M7	PB18B (OD)
DP_CA_DET_EG	N7	PB19A
LCD_PWR_EN	N8	PB19B

BANK4

LPC_AD<0>	P9	PB20A
LPC_AD<1>	N9	PB20B
LPC_AD<2>	P10	PB26A
LPC_AD<3>	M10	PB26B
LPC_FRAME_L	P12	PB27A
LPCPLUS_RESET_L	P13	PB27B
LPC_CLK33M_GMUX	N12	PB28A
GMUX_INT	P14	PB28B

BANK7

LVDS_IG_B_DATA_P<2>	B1	PL2A
LVDS_IG_B_DATA_N<2>	B2	PL2B
GMUX_PL6A	C2	PL6A
TP_GMUX_PL6B	D3	PL6B
LVDS_IG_A_DATA_P<0>	D1	PL7A
LVDS_IG_A_DATA_N<0>	E1	PL7B
LVDS_IG_A_DATA_P<1>	D2	PL8A
LVDS_IG_A_DATA_N<1>	E3	PL8B
LVDS_IG_A_DATA_P<2>	F1	PL9A
LVDS_IG_A_DATA_N<2>	G1	PL9B
LVDS_IG_B_DATA_P<0>	F3	PL10A
LVDS_IG_B_DATA_N<0>	G2	PL10B
LVDS_IG_B_DATA_P<1>	H2	PL11A
LVDS_IG_B_DATA_N<1>	G3	PL11B
LVDS_IG_A_CLK_P	H1	PL12A
LVDS_IG_A_CLK_N	H3	PL12B
TP_LVDS_MUX_SEL_EG	L1	PL14A
TP_GMUX_PL14B	L3	PL14B
GMUX_RESET_L	K3	PL15A
GMUX_VSYNC	L2	PL15B
PM_ALL_GPU_PGOOD	N1	PL25A
PEX_CLKREQ_L	P1	PL25B

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

BANK6

PT7A	A2	LVDS_B_DATA_P<0>
PT7B	A3	LVDS_B_DATA_N<0>
PT8A	A1	LVDS_B_DATA_P<1>
PT8B	B3	LVDS_B_DATA_N<1>
PT9A	C5	LVDS_B_DATA_P<2>
PT9B	A5	LVDS_B_DATA_N<2>
PT14A	B6	EG_PWRSEQ_EN
PT14B	C7	GMUX_DEBUG_RESET_L
PT15A	A6	LVDS_A_CLK_P
PT15B	A7	LVDS_A_CLK_N
PT16A	C8	LVDS_B_CLK_P
PT16B	C9	LVDS_B_CLK_N
PT17A	A8	LVDS_A_DATA_P<0>
PT17B	B9	LVDS_A_DATA_N<0>
PT18A	A9	LVDS_A_DATA_P<1>
PT18B	C10	LVDS_A_DATA_N<1>
PT19A	B10	LVDS_A_DATA_P<2>
PT19B	A10	LVDS_A_DATA_N<2>
PT20A	A11	GND
PT20B	B12	GND
PT28A	B13	GND
PT28B	A13	GND

BANK1

BANK2

PR2A	A14	DP_A_CA_DET
PR2B	B14	DP_HOTPLUG_DET
PR6A	D12	LVDS_EG_A_DATA_P<0>
PR6B	D13	LVDS_EG_A_DATA_N<0>
PR7A	D14	LVDS_EG_A_DATA_P<1>
PR7B	E14	LVDS_EG_A_DATA_N<1>
PR8A	E12	LVDS_EG_A_DATA_P<2>
PR8B	F12	LVDS_EG_A_DATA_N<2>
PR9A	F14	LVDS_EG_B_DATA_P<0>
PR9B	G14	LVDS_EG_B_DATA_N<0>
PR10A	G12	LVDS_EG_B_DATA_P<1>
PR10B	G13	LVDS_EG_B_DATA_N<1>
PR11A	H13	LVDS_EG_B_DATA_P<2>
PR11B	H12	LVDS_EG_B_DATA_N<2>
PR12A	H14	LVDS_EG_A_CLK_P
PR12B	J12	LVDS_EG_A_CLK_N

BANK3

PR14A	L14	LVDS_IG_PANEL_PWR
PR14B	M13	EG_LCD_PWR_EN
PR24A	N14	LVDS_IG_BKL_ON
PR24B	N13	EG_BKLT_EN

R9670 10K 1% 1/20W MF 201 — GMUX_VSYNC

Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDI, JTAG_GMUX_TDO

R9605 1K 5% 1/10W MF-LF 402 — PP3V3_T29, T29_JTAG_FET

JTAG_ISP_TDI, JTAG_ISP_TDO

R9676 100K 5% 1/20W MF 201 — GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563 — ALL_SYS_PWRGD

R9678 4.7K 5% 1/20W MF 201
R9671 4.7K 5% 1/20W MF 201
R9672 4.7K 5% 1/20W MF 201
R9673 4.7K 5% 1/20W MF 201
R9674 4.7K 5% 1/20W MF 201

NO STUFF R9675 0 5% 1/10W MF-LF 402 — GMUX_S3_PD_GND

SYNC_MASTER=K92_YUAN	SYNC_DATE=07/28/2016
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*L9710, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.
*PPVOUT_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719
C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE

0.020 Ohm is place holder for 0.025 Ohm in 0612 package

OMIT
CRITICAL
R9700 0.020 1% MF-LF 0612

PPBUS_S0_LCDBKLT_PWR
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
PLACE_NEAR=L9710.1:5MM
CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=8.4V
PLACE_NEAR=L9710.1:3MM

CRITICAL L9710 33UH-1.8A-110MOHM 1217AS-2SM
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=50V SWITCH_NODE=TRUE
PPVIN_BKL

PLACE_NEAR=D9710.2:3MM
CRITICAL D9701 POWERDI-123 DFLS260
PPBUS_S0_LCDBKLT_PWR_SW

PLACE_NEAR=D9701.2:5MM
CRITICAL C9715 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9716 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9718 2.2UF 10% 100V X7R-CERM 1210
CRITICAL C9719 2.2UF 10% 100V X7R-CERM 1210
C9717 1000PF 10% 100V X7R 603
PLACE_NEAR=D9701.2:3MM
PLACE_NEAR=R9708.1:5MM
PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=50V

PP3V3_S0
PLACE_NEAR=U9701.22:5MM
C9714 0.01UF 10% 16V CERM 402
BKL_VLDO
PLACE_NEAR=U9701.8:3MM
C9710 1UF 10% 25V X5R 603-1
C9711 0.1UF 10% 16V X5R 402
PLACE_NEAR=U9701.22:3MM

U9701
LP8545SQX-EXTF
LLP1

BKL_FET_CNTL
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.4 MM
CRITICAL Q9701 SI7308DN PWRPK-1212-8
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.4 MM

R9708 63.4K 1% 1/10W MF-LF 402
R9709 59.0K 1% 1/10W MF-LF 402
PLACE_NEAR=U9701.12:10MM

R9717 10.2 0.1% 1/16W TF 402
R9718 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.13:10MM
R9719 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.14:10MM
R9720 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.16:10MM
R9721 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.17:10MM
R9722 10.2 0.1% 1/16W TF 402
PLACE_NEAR=U9701.18:10MM

LED_RETURN_1
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

SMBUS_PCH_CLK R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA R9757 0 5% 1/16W MF-LF 402

R9731 301K 1% 1/16W MF-LF 402
PPBUS_S0_LCDBKLT_PWR

NO STUFF C9723 0.1UF 10% 25V X5R 402
R9715 100K 1% 1/16W MF-LF 402

R9704 0 5% 1/16W MF-LF 402
LCD_BKLT_PWM
LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT
R9704 SHOULD BE 47K IF RC FILTER IS USED

NO STUFF C9704 33PF 5% 50V CERM 402

(EEPROM should set EN_I_RES=1)
R9714 14.7K 1% 1/10W MF-LF 402
I_LED=25.1ma
I_LED=369/Riset

R9765 10K 5% 1/16W MF-LF 402
R9716 90.9K 1% 1/16W MF-LF 402
Fpwm=9.62Khz
details in spec

R9755 10K 5% 1/16W MF-LF 402
(APN: 353S3218)

BKL_ISET
BKL_SCL
BKL_SDA
LVDS_BKL_PWM_RC
TP_BKL_FAULT
BKLT_EN
BKL_FSET
BKL_FLT
BKL_SW
BKL_FB
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_VSYNC_R

XW9710 SM
BKL_SGND
PLACE_NEAR=U9701.9:10MM
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V
PLACE XW9710 AWAY FROM U9701.1 AND U9701.15

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0196	1	0.025OHM,1W,0612,MTL FILM RES	R9700	CRITICAL	

SYNC_MASTER=K92_DINESH SYNC_DATE=09/07/2010

PAGE TITLE
LCD Backlight Driver (LP8545)

Apple Inc.

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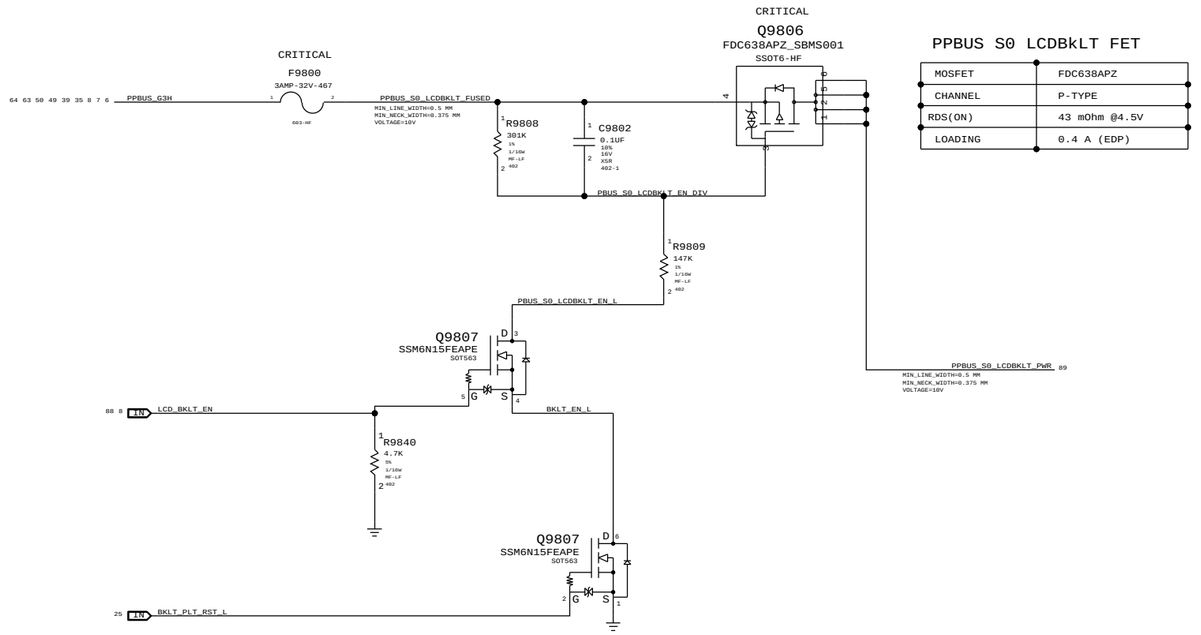

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

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LCD Backlight Support

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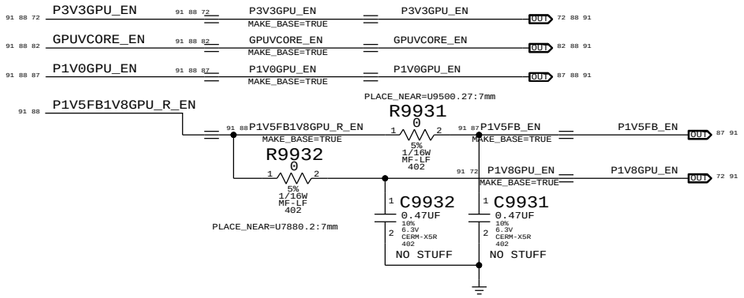
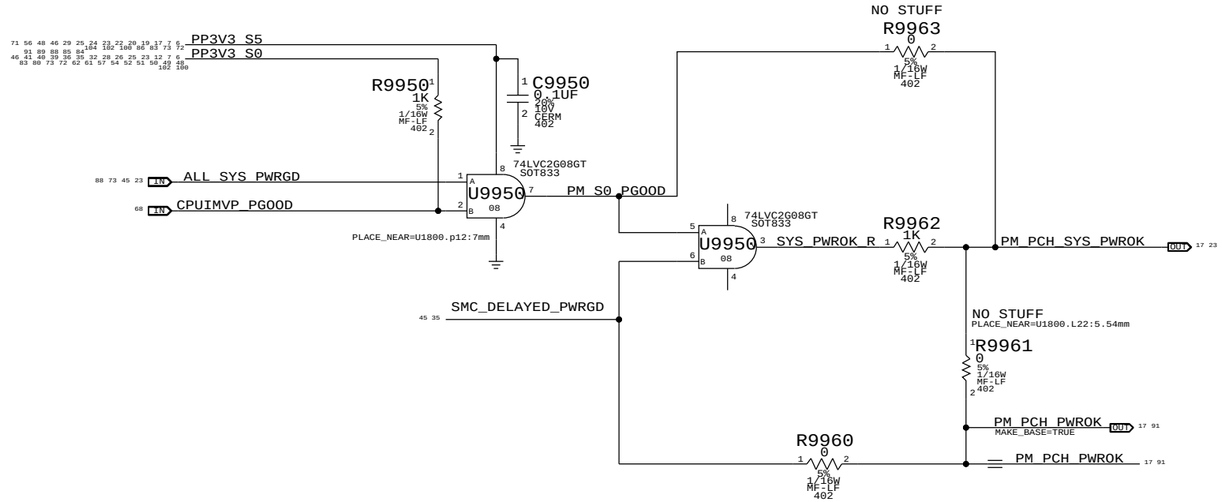
GPU Rail Sequencing

Whistler GPU requires rails to come up in the following order:

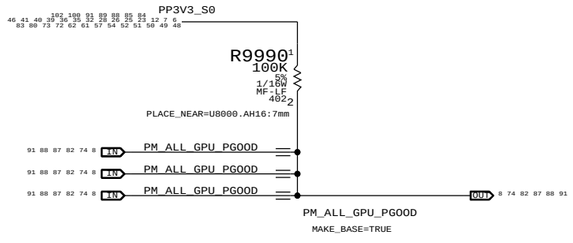
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V;GDDR5 1.5/1.35V



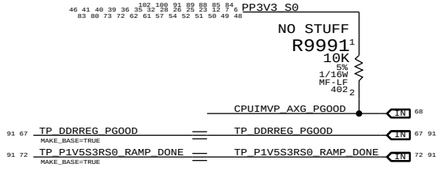
PCH S0 PWRGD



EXT GPU PWRGD Pullup



Unused PGOOD signal



SYNC_MASTER=K92_YUAN SYNC_DATE=07/30/2010

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Power Sequencing EG/PCH S0

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 74
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	74
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 68
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 68
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 68

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0> 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0> 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0> 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0> 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0> 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0> 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8> 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16> 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24> 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32> 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40> 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48> 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56> 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 11 26 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0> 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0> 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0> 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0> 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0> 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0> 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8> 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16> 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24> 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32> 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40> 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48> 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56> 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 11 27 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 11 27 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 11 27

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PAGE TITLE: Memory Constraints

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 17 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 17 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 88
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 88
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 88
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 88
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 6 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N 6 16 41
SATA_HDD_RDVR_R2D	SATA_90D	SATA	SATA_HDD_R2D_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_UF_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N 6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_P 6 41
	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_N 6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 6 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N 6 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N 6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N 6 41
SATA_HDD_RDVR_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N 16 41
	SATA_90D	SATA	SATA_ODD_R2D_P 6 41
	SATA_90D	SATA	SATA_ODD_R2D_N 6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_UF_P 41
	SATA_90D	SATA	SATA_ODD_R2D_UF_N 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 16 41
	SATA_90D	SATA	SATA_ODD_D2R_N 16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_C_P 41
	SATA_90D	SATA	SATA_ODD_D2R_C_N 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P 6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N 6 41
PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 18 24
	USB_85D	USB	USB_HUB1_UP_N 18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 18 24
	USB_85D	USB	USB_HUB2_UP_N 18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P 24 42
	USB_85D	USB	USB_EXTA_N 24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P 24 42
	USB_85D	USB	USB_EXTB_N 24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P 24 43
	USB_85D	USB	USB_EXTC_N 24 43
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 31
	USB_85D	USB	USB_CAMERA_CONN_N 6 31
USB_BT	USB_85D	USB	USB_BT_P 6 24 31
	USB_85D	USB	USB_BT_N 6 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P 24 53
	USB_85D	USB	USB_TPAD_N 24 53
USB_IR	USB_85D	USB	USB_IR_P 24 44
	USB_85D	USB	USB_IR_N 24 44
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 18
USB_T29A	USB_85D	USB	USB_T29A_P 8 24
	USB_85D	USB	USB_T29A_N 8 24

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
	LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47 88
	LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47 88
	LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 25 47 88
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 45
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 47
	SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	6 16 23 26 28 30 32 41 48 62 89
	SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	6 16 23 26 28 30 32 41 48 62 89
	SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
	SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
	SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
	SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
	HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
		HDA_50S	HDA	HDA_BIT_CLK_R	16
	HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
		HDA_50S	HDA	HDA_SYNC_R	16
	HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
		HDA_50S	HDA	HDA_RST_L	16 57
	HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
		HDA_50S	HDA	AUD_SDI_R	57
	HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
		HDA_50S	HDA	HDA_SDOUT_R	16
	SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
	SPI_CLK	SPI_55S	SPI	SPI_CLK	47
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI	47
	SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
		SPI_55S	SPI	SPI_CS0_L	47
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	31
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	31
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	31
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
125	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
125	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
126	PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
126	PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
125		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
125		CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
124	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
124	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
125		CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
126		CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 74
		CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 74
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	16 32
		CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	16 32
126	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 33
126	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 33
126	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
126	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
126	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 33
126	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 33
127	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
126	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L 32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0> 36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0> 36 37

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P 38 40
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N 38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P 38 40
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N 38 40

Port 0 and 2 Not Used

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 85
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 85
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 85
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 85
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	85
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 85 86
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 85 86
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 86
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 86
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	6 85
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 85 97
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 85 97
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	85
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	85
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	85
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	85
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	85 86
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	85 86
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	85 86
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	85 86
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	97
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	97
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 79
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 79
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 79
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 79
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 79
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 48 85
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 48 85
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 85
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 85

Only used on hosts supporting T29 video-in

SYNC_MASTER=T29_REF SYNC_DATE=10/20/2010

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T29 Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 31 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 31 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	6 31 45 48 51 80
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	6 31 45 48 51 80
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 45 48 63 64
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 45 48 63 64
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	45 48 103 104
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	45 48 103 104

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	64
	1TO1_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	64
	1TO1_DIFFPAIR		CHGR_CSO_N	64

SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

PAGE TITLE: SMC Constraints

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P 76 77
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N 76 77
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P 76 77
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N 76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0> 76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0> 76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L 76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L 76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L 76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L 76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L 76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L 76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L 76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L 76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L 76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L 76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L 76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L 76 77
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0> 76 77
L295 FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1> 76 77
L293 FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2> 76 77
L291 FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3> 76 77
L290 FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0> 76 77
L292 FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1> 76 77
L294 FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2> 76 77
L296 FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3> 76 77
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0> 76 77
L299 FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1> 76 77
L300 FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2> 76 77
L301 FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3> 76 77
L302 FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0> 76 77
L303 FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1> 76 77
L304 FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2> 76 77
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3> 76 77
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0> 76 77
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0> 76 77
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1> 76 77
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1> 76 77
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0> 76 77
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0> 76 77
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1> 76 77
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1> 76 77
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0> 76 77
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8> 76 77
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16> 76 77
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24> 76 77
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0> 76 77
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8> 76 77
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16> 76 77
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24> 76 77
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L 76 77 78

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P 76 78
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N 76 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P 76 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N 76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0> 76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0> 76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L 76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L 76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L 76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L 76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L 76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L 76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L 76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L 76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L 76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L 76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L 76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L 76 78
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0> 76 78
L305 FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1> 76 78
L306 FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2> 76 78
L307 FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3> 76 78
L310 FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0> 76 78
L308 FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1> 76 78
L309 FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2> 76 78
L311 FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3> 76 78
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0> 76 78
L314 FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1> 76 78
L312 FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2> 76 78
L313 FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3> 76 78
L316 FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0> 76 78
L315 FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1> 76 78
L317 FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2> 76 78
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3> 76 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0> 76 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0> 76 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1> 76 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1> 76 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0> 76 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0> 76 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1> 76 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1> 76 78
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0> 76 78
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8> 76 78
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16> 76 78
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24> 76 78
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0> 76 78
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8> 76 78
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16> 76 78
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24> 76 78

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P 84 88
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N 84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0> 84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0> 84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P 84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N 84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0> 84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0> 84 88
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P 6 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N 6 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P 6 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N 6 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P 83 84
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N 83 84
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0> 6 83 84
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0> 6 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0> 6 83 84
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0> 6 83 84

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 79 80
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M 79 80
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P 79 88
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N 79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0> 79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0> 79 88
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3> 79 80
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3> 79 80
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0> 79 88
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0> 79 88
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3> 79 80
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3> 79 80
DP_MI	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0> 79 85
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0> 79 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P 84 85
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N 84 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P 79 84
	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N 79 84

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

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GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	49 65
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	49 65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	49
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	49
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	49
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	49
	SENSE_1TO1_55S	SENSE	GPUISENS_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	49 67
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	49 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	31 103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	31 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	89 103
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	89 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	50 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	50 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	103
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	BI_MIC_P	61 62
	AUDIODIFF	AUDIO	BI_MIC_N	61 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	58 60
	AUDIODIFF	AUDIO	AUD_LO1_R_N	58 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO2_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_L_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INR_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INL_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375LFE_IN_P	60
	AUDIODIFF	AUDIO	SSM2375LFE_IN_N	60

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_N	6 32
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_P	6 16 32
	PCIE_85D	PCIE	PCIE_EXCARD_D2R_N	6 16 32
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_N	16 32
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	6 32
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	50 64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	50 64
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	42
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
(USB_EXTB)	USB_85D	USB	USB_LT2_P	42
	USB_85D	USB	USB_LT2_N	42
USB_EXCARD	USB_85D	USB	USB_EXCARD_P	8 24 32
	USB_85D	USB	USB_EXCARD_N	8 24 32
USB_EXCARD	USB_85D	USB	USB2_EXCARD_CONN_P	6 32
	USB_85D	USB	USB2_EXCARD_CONN_N	6 32
(USB_EXTC)	USB_85D	USB	USB_LT3_P	43
	USB_85D	USB	USB_LT3_N	43
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	48 56 71 72 73 83 86 91 102 104 6 7 17 19 20 22 23 24 25 35 46
		SB_POWER	PP3V3_S0	63 62 72 73 80 83 84 86 88 89 6 7 12 23 25 26 28 32 35 36 39 49 41 46 48 49 50 51 52 54 57
		SB_POWER	PP1V5_S3RS0	7 72 104 91 102
		GND	GND	

K92 Specific Net Properties
K91 does not have

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 79
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 79
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	33 51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51

K92 Specific Net Properties
K91 does not have

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_N	104
	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_P	104

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: Project Specific Constraints

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K92 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

NOTE: Based on K92 mlb stackup.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

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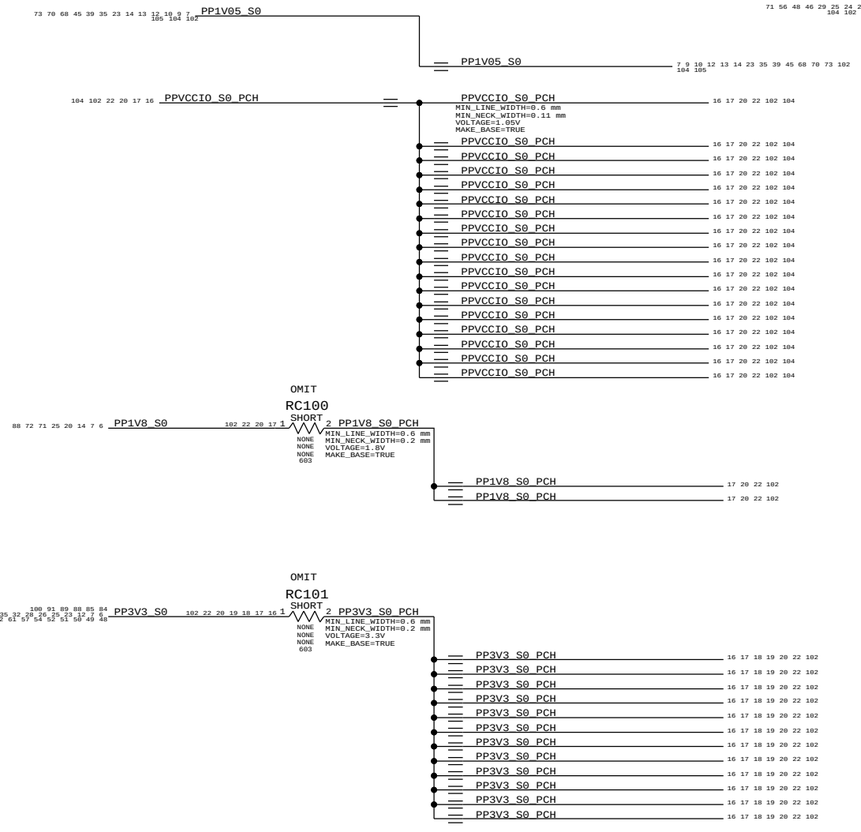
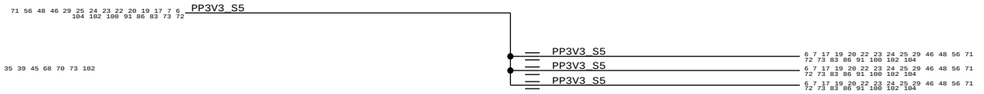
PCH "S0" Rails



PCH "S5" Rail



SYNC_MASTER=K17_MLB	SYNC_DATE=04/27/2010
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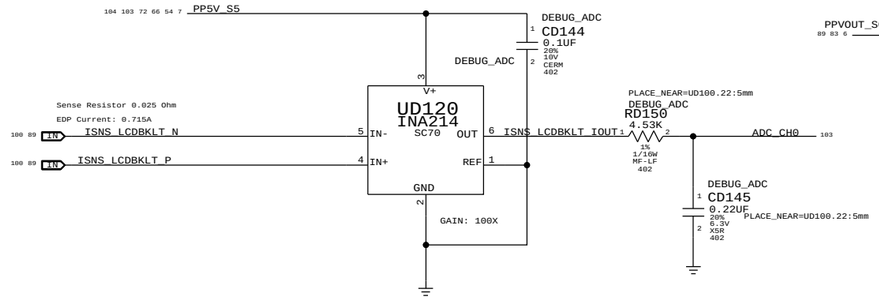
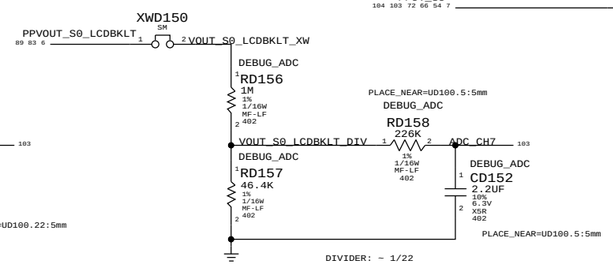
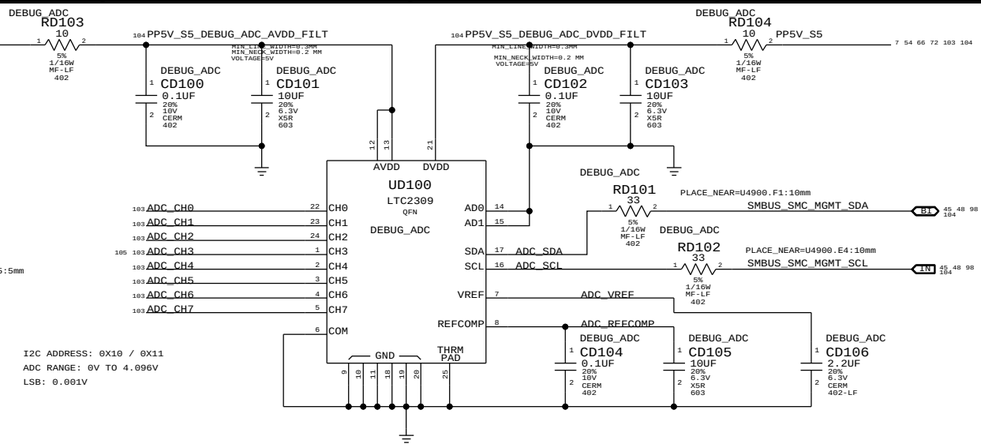
LCD BKLT Current Sense

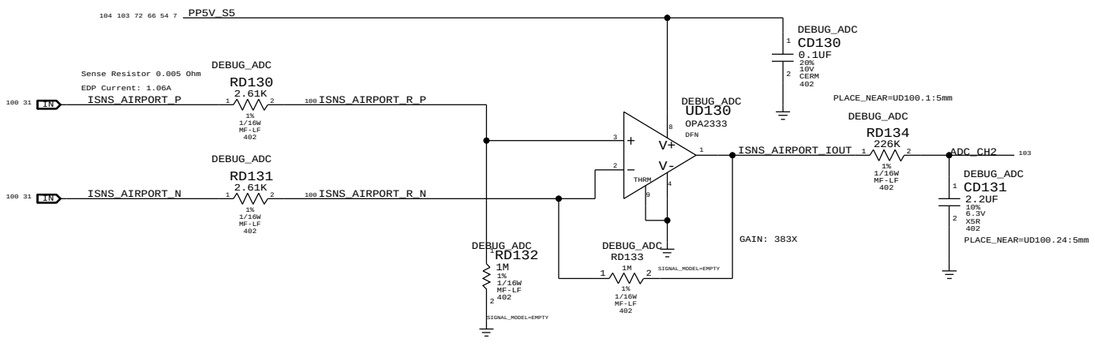


LCD BKLT Voltage Sense

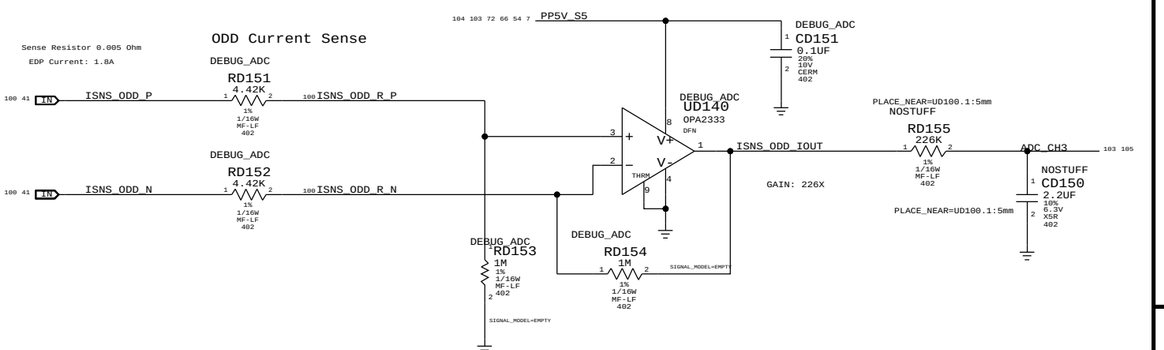




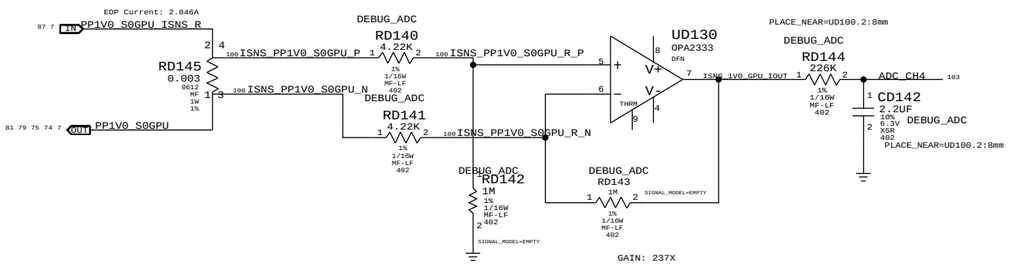
AIRPORT Current Sense



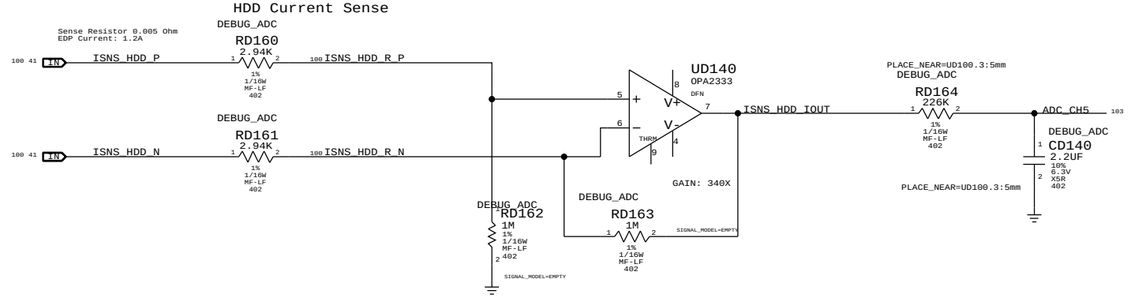
ODD Current Sense



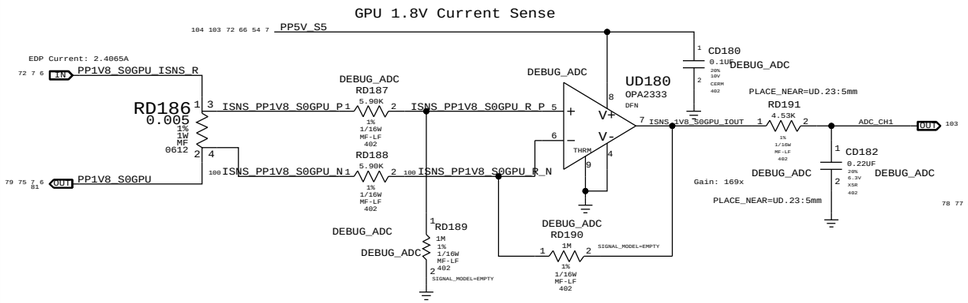
GPU 1.0V Current Sense



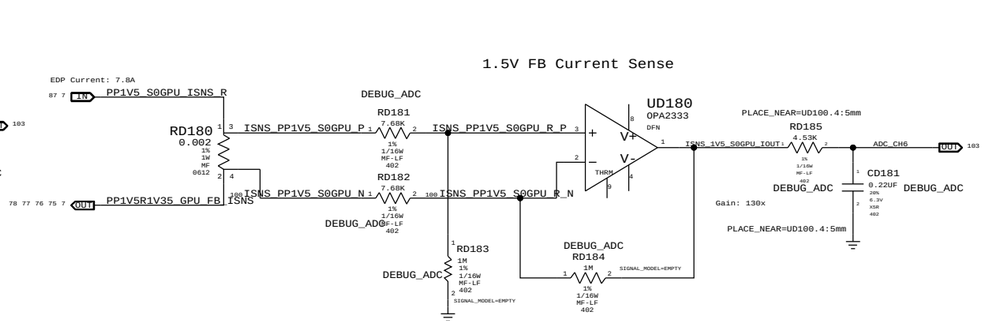
HDD Current Sense



GPU 1.8V Current Sense



1.5V FB Current Sense



SYNC_MASTER=K92_DINESH	SYNC_DATE=09/07/2010
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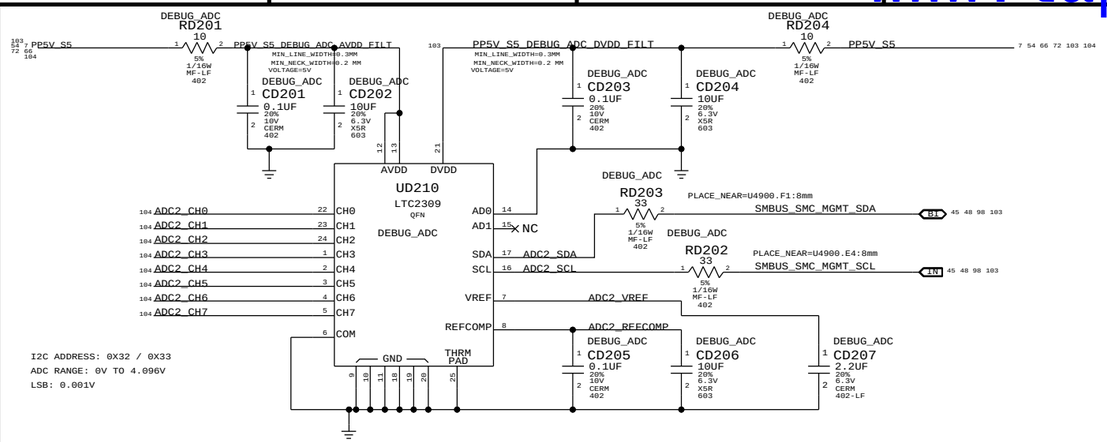

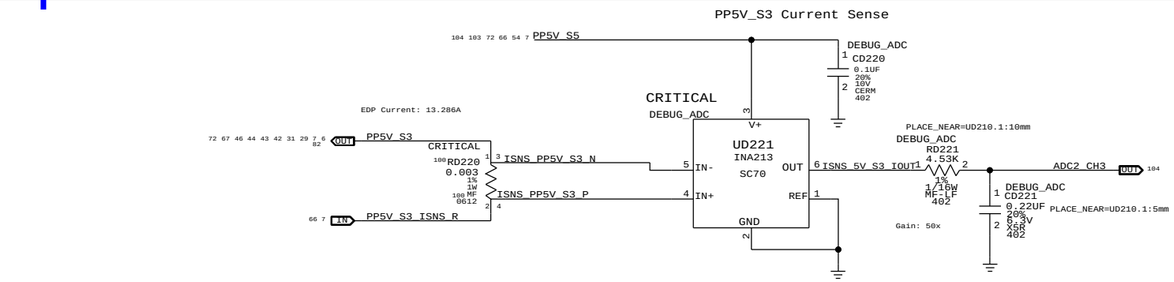

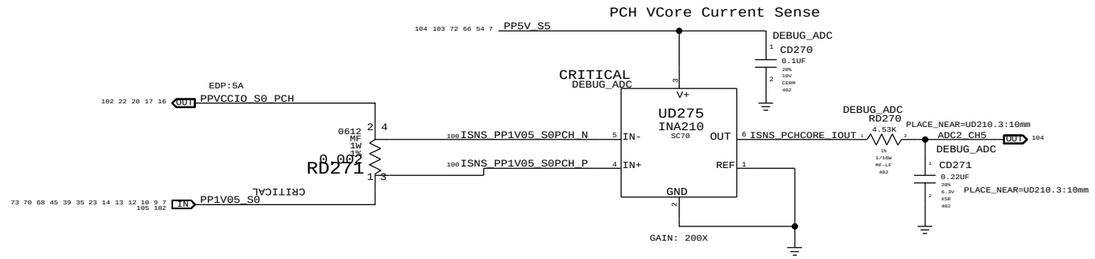

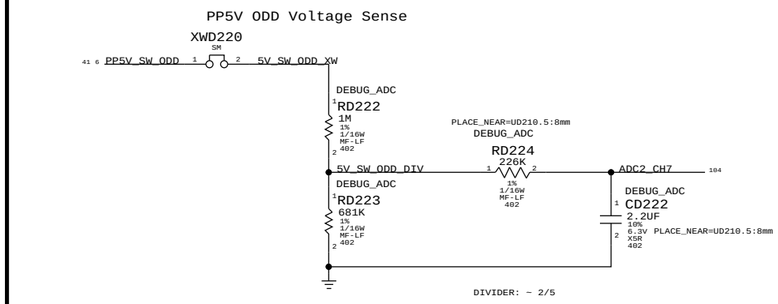

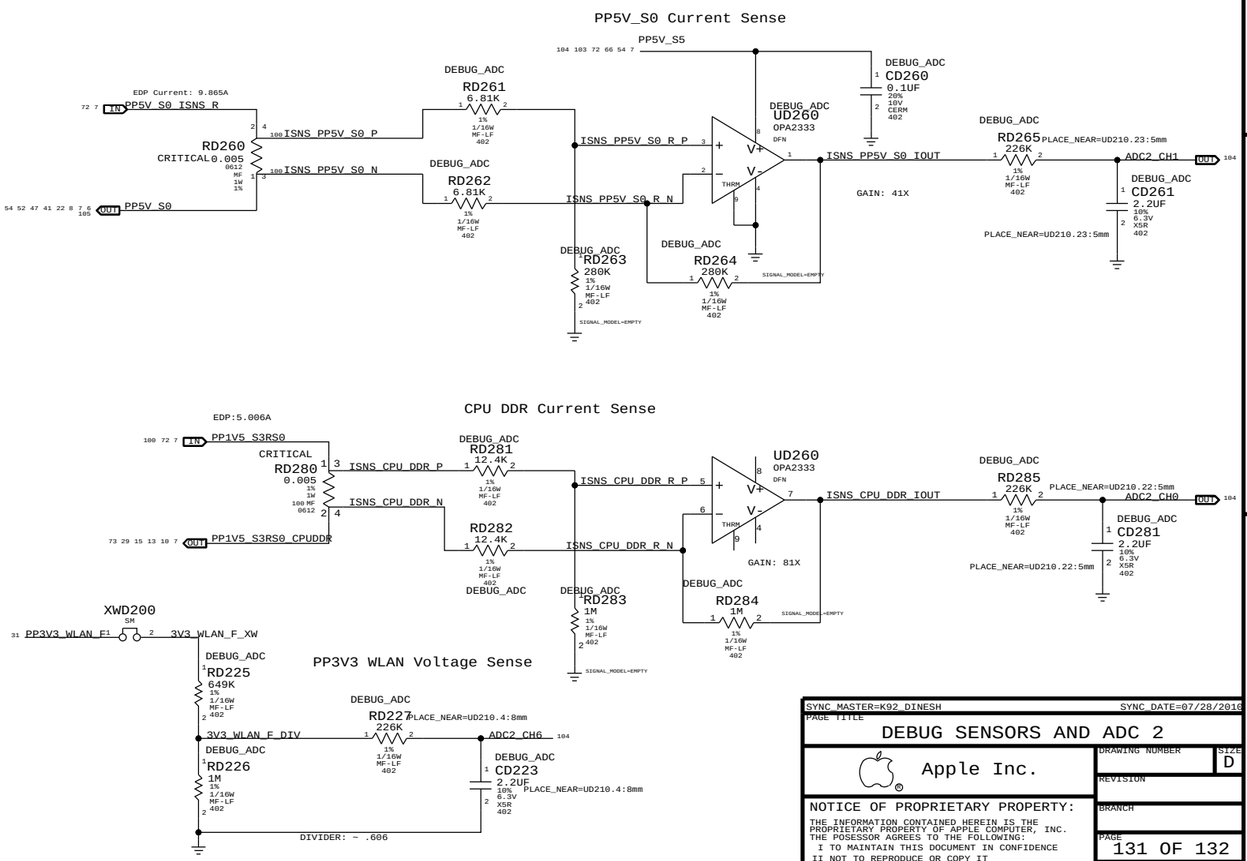

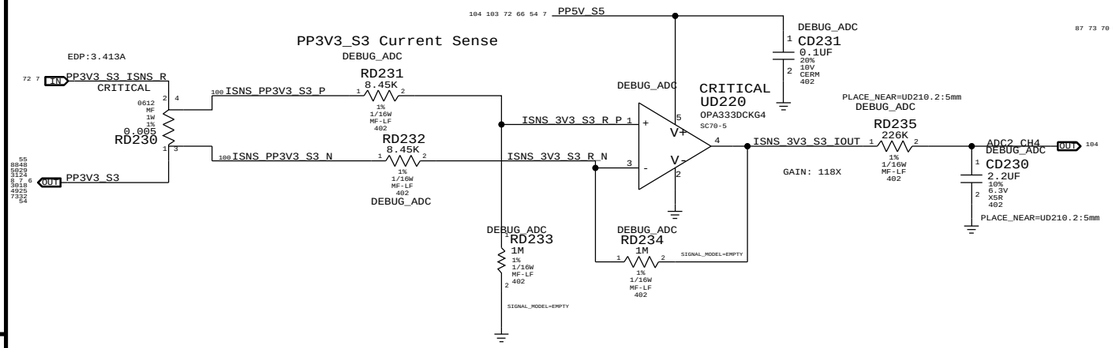

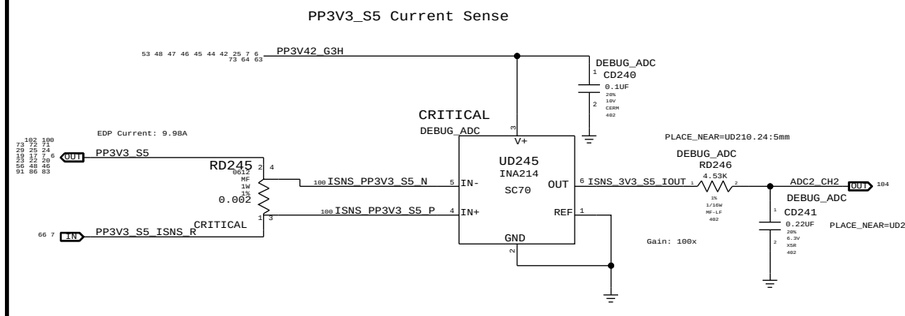

SYNC_MASTER=K92_DINESH	SYNC_DATE=07/28/2010
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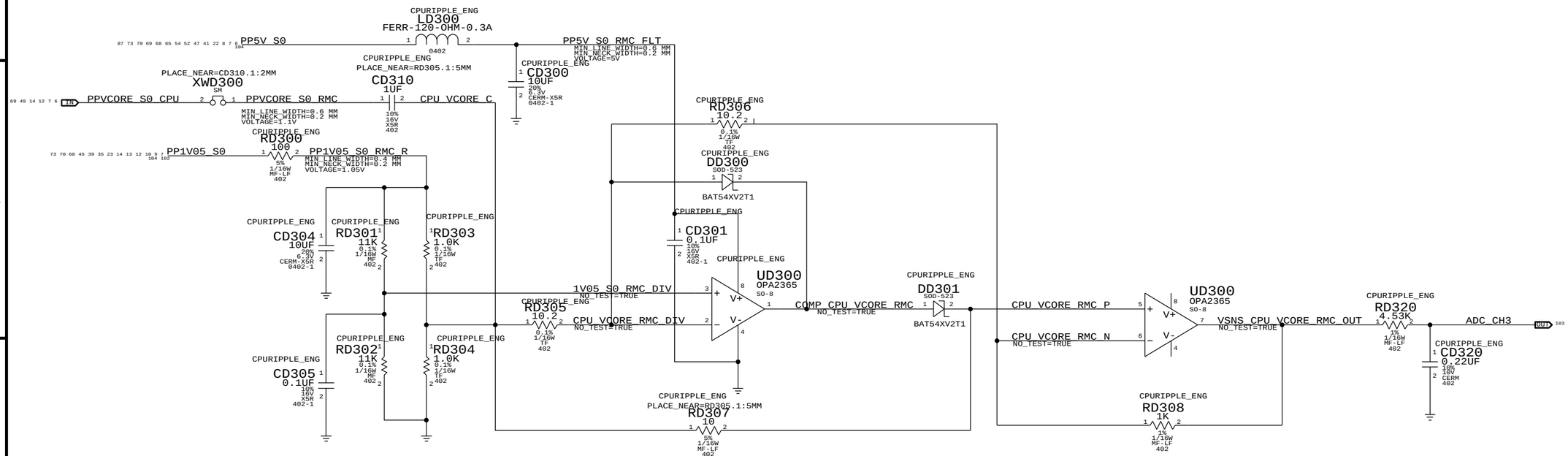

SYNC_MASTER=K92_DINESH	SYNC_DATE=08/23/2010
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