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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
C	0000897412	PRODUCTION RELEASED		2010-04-26

SCHEMATIC, SCRATCHO_MLB

04/28/2010

Page	Contents	Sync	Date	Page	Contents	Sync	Date
1	Table of Contents	NA	NA	39	Voltage Sensing	T27_MLB	02/16/2010
2	System Block Diagram	MASTER	MASTER	40	Current Sensing	T27_MLB	02/02/2010
3	Power Block Diagram	MASTER	MASTER	41	Thermal Sensors	MASTER	MASTER
4	BOM Configuration	(K84_MLB)	(01/19/2009)	42	Fan Connector	T27_MLB	02/16/2010
5	Revision History	MASTER	MASTER	43	WELLSPRING 1	T27_MLB	02/16/2010
6	Revision History	MASTER	MASTER	44	WELLSPRING 2	MASTER	MASTER
7	FUNC TEST	MASTER	MASTER	45	SMS	MASTER	MASTER
8	Power Aliases	MASTER	MASTER	46	DEBUG SENSORS AND ADC	MASTER	MASTER
9	SIGNAL ALIAS	(K84_MLB)	(02/04/2009)	47	SPI ROM	T27_MLB	02/16/2010
10	CPU FSB	T27_MLB	02/16/2010	48	AUDIO: CODEC/REGULATOR	AUDIO	02/16/2010
11	CPU Power & Ground	T27_MLB	02/16/2010	49	AUDIO: LINE INPUT FILTER	AUDIO	02/16/2010
12	CPU Decoupling	T27_MLB	02/16/2010	50	AUDIO: HEADPHONE FILTER	AUDIO	02/16/2010
13	eXtended Debug Port(MiniXDP)	(K84_MLB)	(02/25/2009)	51	AUDIO: SPEAKER AMP	AUDIO	02/16/2010
14	MCP CPU Interface	T27_MLB	02/16/2010	52	AUDIO: JACK	AUDIO	02/16/2010
15	MCP Memory Interface	T27_MLB	02/16/2010	53	AUDIO: JACK TRANSLATORS	AUDIO	02/16/2010
16	MCP PCIe Interfaces	T27_MLB	02/16/2010	54	DC-In & Battery Connectors	MASTER	MASTER
17	MCP Graphics	T27_MLB	02/16/2010	55	PBus Supply & Battery Charger	(K6_MLB)	(11/06/2009)
18	MCP SATA, USB & Ethernet	T27_MLB	02/16/2010	56	5V/3.3V SUPPLY	(K6_MLB)	(10/27/2009)
19	MCP HDA, LPC & MISC	T27_MLB	02/16/2010	57	1.5V/0.75V DDR3 SUPPLY	(K6_MLB)	(11/06/2009)
20	MCP Power & Ground	T27_MLB	02/16/2010	58	IMVP6 CPU VCore Regulator	(K84_MLB)	(11/18/2009)
21	MCP89 Memory Rail Gating	K6_MLB	02/16/2010	59	MCP VCore Regulator	(K6_MLB)	(10/27/2009)
22	MCP89 GFX Core Rail Gating	T27_MLB	12/15/2009	60	CPU VTT(1.05V) SUPPLY	(K84_MLB)	(02/04/2009)
23	MCP Standard Decoupling	(T27_MLB)	(11/16/2009)	61	Misc Power Supplies	MASTER	MASTER
24	MCP Graphics Support	T27_MLB	02/16/2010	62	Power Sequencing	(T27_MLB)	(10/27/2009)
25	SB Misc	(T27_MLB)	(10/07/2009)	63	POWER FETS	MASTER	MASTER
26	DDR3 SO-DIMM Connector A	T27_MLB	02/16/2010	64	LVDS CONNECTOR	(K84_MLB)	(10/19/2009)
27	DDR3 SO-DIMM Connector B	T27_MLB	02/16/2010	65	DISPLAYPORT SUPPORT	K6_MLB	02/16/2010
28	SO-DIMM Pinswaps	MASTER	MASTER	66	DisplayPort Connector	MASTER	MASTER
29	FSB/DDR3 Vref Margining	T27_MLB	02/16/2010	67	LCD Backlight Driver (MC34845)	MASTER	MASTER
30	X16 WIRELESS CONNECTOR	MASTER	MASTER	68	LCD Backlight Support	(K84_MLB)	(10/19/2009)
31	Ethernet PHY (RTL8211CL)	MASTER	MASTER	69	CPU/FSB Constraints	T27_MLB	02/16/2010
32	ETHERNET CONNECTOR	MASTER	MASTER	70	Memory Constraints	T27_MLB	02/16/2010
33	SATA Connectors	MASTER	MASTER	71	MCP Constraints 1	T27_MLB	02/16/2010
34	External USB Connectors	(K84_MLB)	(10/03/2009)	72	MCP Constraints 2	T27_MLB	02/16/2010
35	SMC	T27_MLB	02/16/2010	73	Ethernet Constraints	MASTER	MASTER
36	SMC Support	(T27_MLB)	(10/27/2009)	74	SMC Constraints	T27_MLB	02/16/2010
37	LPC+SPI Debug Connector	(T27_MLB)	(12/15/2009)	75	K87 SPECIFIC CONSTRAINTS	MASTER	MASTER
38	K87 SMBus Connections	MASTER	MASTER	76	K87 RULE DEFINITIONS	MASTER	MASTER

DRAWING TITLE		DRAWING NUMBER	SIZE
SCHEM, MLB_LDO, SCRATCHO		051-8561	D
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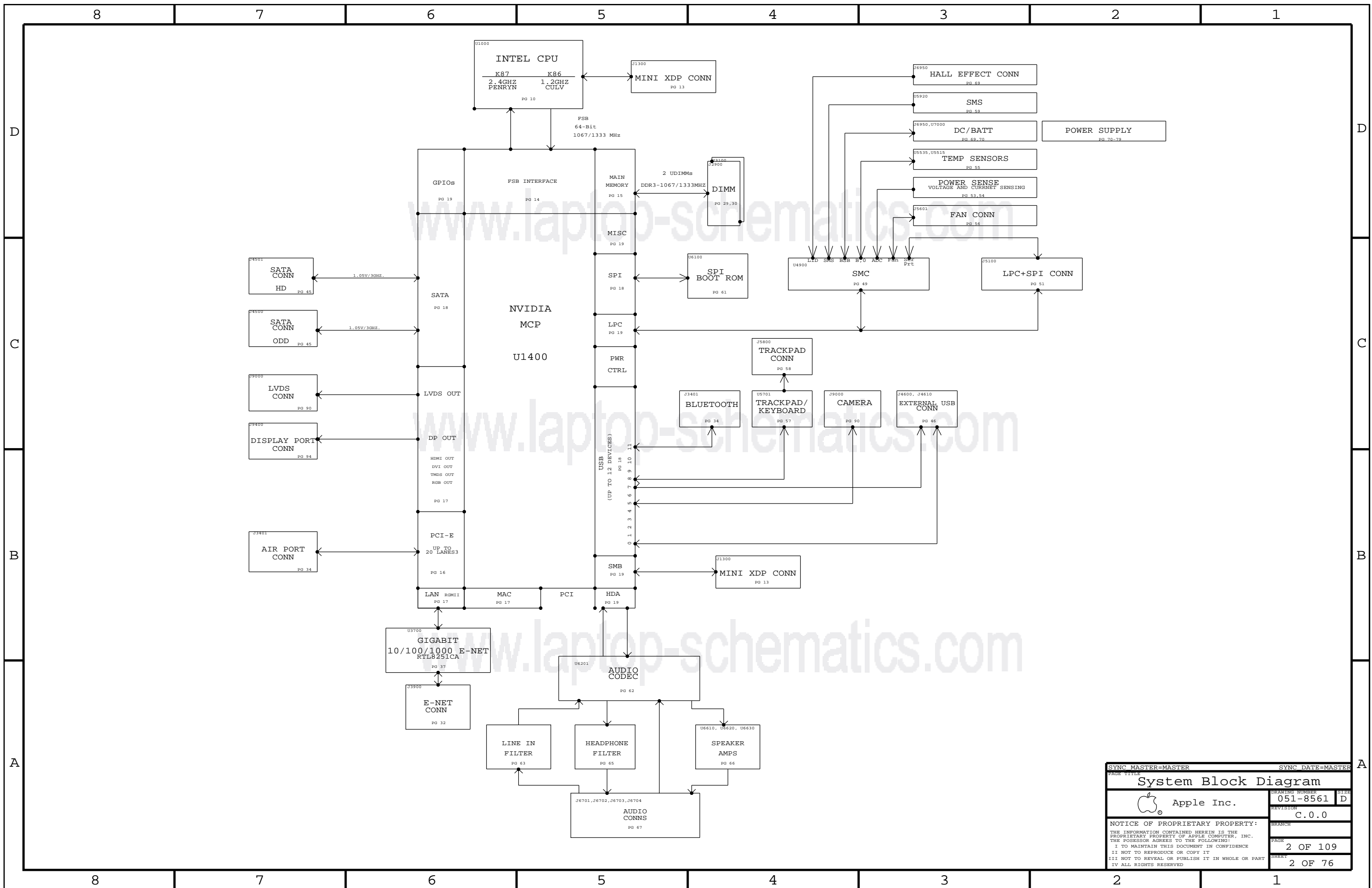
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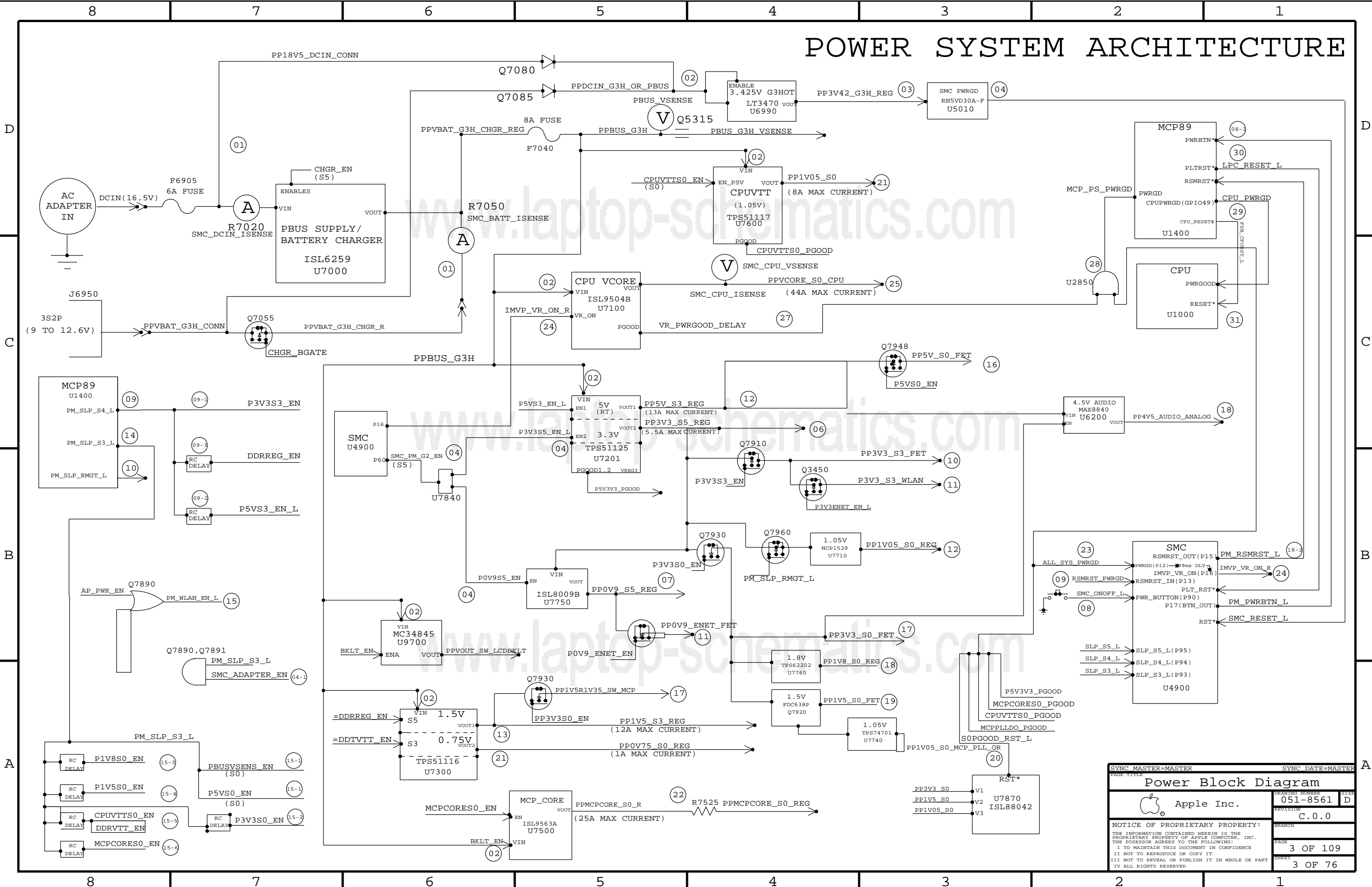
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POWER SYSTEM ARCHITECTURE



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Power Block Diagram			
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		PAGE	3 OF 109
		SHEET	3 OF 76

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1115	PCBA,MLB_LDO,FOXCONN,K87	K87_COMMON,K87_SPECIFIC,FOX_DDR_CONN,EEEE:DD16
639-1116	PCBA,MLB_LDO,MOLEX,K87	K87_COMMON,K87_SPECIFIC,MOLEX_DDR_CONN,EEEE:DD17
085-1799	K87 MLB_LDO DEVELOPMENT BOM	K87_DEVELOPMENT_PVT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1632	1	K87 MLB_LDO DEVELOPMENT BOM	DEVEL	CRITICAL	DEVELOPMENT_BOM

BOM GROUP	BOM OPTIONS
K86_K87_COMMON	K86_K87_COMMON1,PROJECT_PHASE:PROD,COMMON,ALTERNATE,BOOTROM:PROG,WELLSPRING:PROG,MCP_T_DIODE_SENSOR
K86_K87_COMMON1	DP_ESD,MIKEY,MCPPLL_R:REG,ENET1V05:INT,LED:K86_K87,S0PGOOD_BJT,ENET_ESD,VFRQ:SLP53,SMC_DEBUG:YES,SPI:25MHZ,XDP_OLD_AUDIO_SWITCH
K87_SPECIFIC	CPU:2.4GHZ,IMVP6:2PHASE,SMC:PROG_K87,MCP89M:A02
K86_SPECIFIC	CPU:1.2GHZ,IMVP6:1PHASE,SMC:PROG_K86,MCP83M

BOM GROUP	BOM OPTIONS
PROJECT_PHASE:DEV	DEVELOPMENT_BOM
PROJECT_PHASE:PROD	K86_K87_DEBUG:PROD
K86_K87_DEVELOPMENT_ONLY	DEBUG_ADC,LPCPLUS_CON,S0PGOOD_ISL,EFI_DEBUG,MCPPLL_LDO,EXT1V05,XDP_CON,LPCPLUS
K86_K87_DEVELOPMENT_PVT	LPCPLUS_CON,XDP_CON,VREFMRGN:YES,LPCPLUS
K86_K87_DEBUG:DEV	VREFMRGN:YES,BMON:ENG,BKLT:ENG,SENS_R:ENG
K86_K87_DEBUG:PROD	VREFMRGN:NO,BMON:PROD,BKLT:PROD,SENS_R:PROD,MCPHVDD:P2V5,LDO:FIXED,HTOL_SENSE:YES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33783680	1	PCD,LGDS,FRQ,2.40,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU:2.4GHZ
33783792	1	CDL,SLOW,FRQ,1.2,10W,800,R0,1M,BGA	U1000	CRITICAL	CPU:1.2GHZ
33783797	1	IC,MCP89M-A01,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A01
33783866	1	IC,MCP89M-A02,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A02
33783876	1	IC,MCP83M-A02,31X31MM,BGA1168	U1400	CRITICAL	MCP83M
51680706	1	CONN,204P,SOD1MM,SOCKET,DDR3,RAM,BGA	J3100	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SOD1MM,P=0.6MM	J2900	CRITICAL	FOX_DDR_CONN
51680790	1	CONN,204P,SOD1MM,SOCKET,DDR3,RAM,BGA	J3100	CRITICAL	MOLEX_DDR_CONN
516-0213	1	CONN,204P,SOD1MM,P=0.6MM	J2900	CRITICAL	MOLEX_DDR_CONN
452-1708	4	SCR,M1,6X0.35X6.0,D4,HO.3,BLK,M97	SCREEN1,SCREEN2,SCREEN3,SCREEN4	CRITICAL	
870-1940	4	POGO PIN,MED,NOISE-IMPROVED,SILVER,K87	ZS0900,ZS0901,ZS0902,ZS0903	CRITICAL	
870-1940	3	POGO PIN,MED,NOISE-IMPROVED,SILVER,K87	ZS0908,ZS0909,ZS0911	CRITICAL	
870-1939	5	POGO PIN,TALL,NOISE-IMPROVED,SILVER,K87	ZS0904,ZS0905,ZS0906,ZS0907,ZS0910	CRITICAL	
870-1939	5	POGO PIN,TALL,NOISE-IMPROVED,SILVER,K87	ZS0912,ZS0913,ZS0914,ZS0915,ZS0916	CRITICAL	
870-1938	3	POGO PIN,THIN,NOISE-IMPROVED,SILVER,K87	ZS0917,ZS0918,ZS0916	CRITICAL	

353S2718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE
 514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR
 514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS
 514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR
 514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0563	1	IC,SMC,HSB/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0252	1	SUBASSY, IC, SMC, K87	U4900	CRITICAL	SMC:PROG_K87
341T0250	1	SUBASSY, IC, SMC, K86	U4900	CRITICAL	SMC:PROG_K86
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0251	1	SUBASSY, IC, BOOT ROM, K86/K87	U6100	CRITICAL	BOOTROM:PROG
337S2983	1	IC,PSOC+ W/ USB,S6 PIN,MFP,CY8C24794	U5701	CRITICAL	WELLSPRING:BLANK
341S2677	1	IC,WELLSPRING CONTROLLER,K87	U5701	CRITICAL	WELLSPRING:PROG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	DATE/VERSION, MAGLAYERS AS ALTERNATE
152S0796	152S0685		ALL	CONTACT AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
138S0603	138S0602		ALL	MURATA AS ALTERNATE
128S0093	128S0218		ALL	RENAT AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
104S0018	104S0023		ALL	DATE/VERSION AS ALTERNATE
353S2811	353S1832		ALL	NEW IMPROVED INTERNAL PART AS ALTERNATE
353S2988	353S2987		ALL	MURATA AS ALTERNATE
376S0908	376S0634		ALL	VERONA AS ALTERNATE
376S0907	376S0634		ALL	FAHRENHEIT AS ALTERNATE
376S0912	376S0868		ALL	SHENYI (NEW SPEC) AS ALTERNATE

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8561	1	SCHEM,MLB_LDO,K87	SCN	CRITICAL	
820-2877	1	PCB,F,MLB_LDO,K87	PCB	CRITICAL	

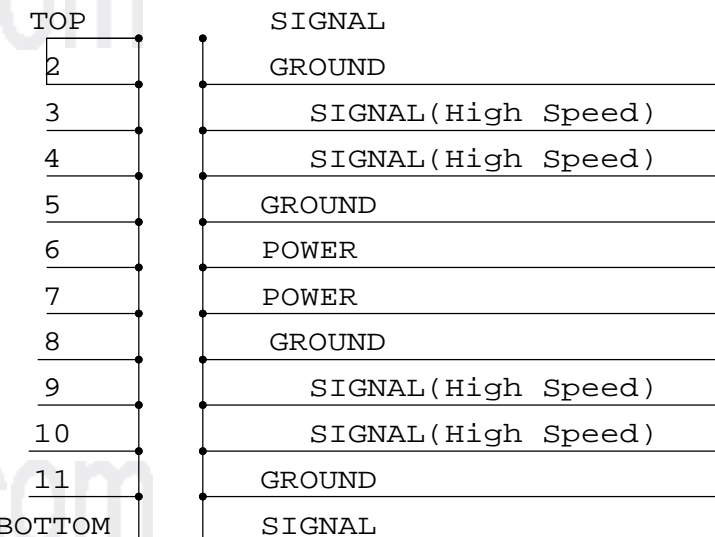
Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEEE_DD16]	CRITICAL	EEEE:DD16
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEEE_DD17]	CRITICAL	EEEE:DD17
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEEE_DD18]	CRITICAL	EEEE:DD18
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEEE_DD19]	CRITICAL	EEEE:DD19

Part Substitutions (differences with K6/K69)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0125	1	RES,MTL FILM,1/16W,113 OHM,1.0402,SMD,LF	R5714		LED:K86_K87

BOARD STACK-UP



SYNC MASTER=(K84 MLB)		SYNC DATE=(01/19/2009)	
BOM Configuration			
Apple Inc.		DRAWING NUMBER 051-8561	SIZE D
		REVISION C.0.0	BRANCH
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10/1/2009:INITIAL RELEASE 0.0.1- ALL PAGES SYNC'ED FROM K84 REF:ADD K87 AND CPU PAGES WITH K6 PAGES - UPDATED SCHEMATIC AND PCB PART NUMBER INFO
2009-12-03: Proto 0 release 1.0.0
2009-12-04: 1.1.0 csa 4: Updated CPU block text to include CPU description for both K86 and K87
csa 3: Added note to include K86 in title
csa 4: Added BOM entry under Module Parts table to include CULV processor (33783779) to minimize delta on this page between K86 and K87 per Diana

2010-01-19: 2.5.0 csa 37: Per <rdar://problem/7554342> K86/K87: Change L3720 to 152S1182 Changed L3720 to 152S1182 (IND,PWR,SHD,4.7UH,20V,0.91A,31X31X12MM) for lower ESR
2010-01-22: 2.6.0 csa 4: Per <rdar://problem/751786> K86/K87: Add E3T EEE code for K86 to schematic Added row to EEE table for E3T changed BOMPTIONS to be mutually exclusive (changed "_" to "*")
2010-01-28: 2.7.0 *** Resynced with T27 and K6 (no differences) *** Resynced Audio pages with the following changes: pg. 62: changed R6211 to 22 Ohms pg. 67: no stuffed R6712 and R6713
csa 45: Per <rdar://problem/751001> K87: SMC: Radiated Emissions: Right Audio emissions fail Added L4530, L4531 (APN 155S0137) to SIL connector pins
csa 97: Per <rdar://problem/7589365> K86/K87: Compensation settings change to provide more phase margin, reduce ripple Changed C9705 from 8.2nF to 33nF (132S0131) Changed C9706 from 120pF to 220pF (131S2225)

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Revision History table with columns: SYNC MASTER=MASTER, SYNC DATE=MASTER, DRAWING NUMBER: 051-8561, REVISION: C.0.0, PAGE: 5 OF 109, SHEET: 5 OF 76. Includes Apple Inc. logo and a notice of proprietary property.

8

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4

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D

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		PAGE	6 OF 109
		SHEET	6 OF 76

8

7

6

5

4

3

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Functional Test Points

FAN CONNECTORS FUNC_TEST

TEST	TRUE	PP5V_S0	7 8 62
TEST	TRUE	FAN_RT_PWM	42
TEST	TRUE	FAN_RT_TACH	42

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

TEST	TRUE	BI_MIC_N	52 53 75
TEST	TRUE	BI_MIC_P	52 53 75
TEST	TRUE	BI_MIC_SHIELD	52 53

SPEAKER FUNC_TEST

TEST	TRUE	SPKRAMP_L_N_OUT	51 52
TEST	TRUE	SPKRAMP_L_P_OUT	51 52
TEST	TRUE	SPKRAMP_R_N_OUT	51 52
TEST	TRUE	SPKRAMP_R_P_OUT	51 52
TEST	TRUE	SPKRAMP_SUB_N_OUT	51 52
TEST	TRUE	SPKRAMP_SUB_P_OUT	51 52

LVDS FUNC_TEST

TEST	TRUE	PP3V3_S0_LCD_DDC_F	64
TEST	TRUE	PP3V3_SW_LCD_PANEL_F	24 (NEED 2 TP)
TEST	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67 (NEED 2 TP)
TEST	TRUE	LVDS_IG_DDC_CLK	9 64
TEST	TRUE	LVDS_IG_DDC_DATA	9 64
TEST	TRUE	LVDS_IG_A_DATA_N<0>	9 64 71
TEST	TRUE	LVDS_IG_A_DATA_P<0>	9 64 71
TEST	TRUE	LVDS_IG_A_DATA_N<1>	9 64 71
TEST	TRUE	LVDS_IG_A_DATA_P<1>	9 64 71
TEST	TRUE	LVDS_IG_A_DATA_N<2>	9 64 71
TEST	TRUE	LVDS_IG_A_DATA_P<2>	9 64 71
TEST	TRUE	LVDS_IG_A_CLK_F_N	64 75
TEST	TRUE	LVDS_IG_A_CLK_F_P	64 75
TEST	TRUE	LED_RETURN_1	44 67
TEST	TRUE	LED_RETURN_2	44 67
TEST	TRUE	LED_RETURN_3	44 67
TEST	TRUE	LED_RETURN_4	44 67
TEST	TRUE	LED_RETURN_5	44 67
TEST	TRUE	LED_RETURN_6	44 67
TEST	TRUE	PP5V_S3_CAMERA_F	7 64
TEST	TRUE	USB_CAMERA_CONN_P	64 75
TEST	TRUE	USB_CAMERA_CONN_N	64 75

(NEED TO ADD 5 GND TP)

SATA ODD CONN FUNC_TEST

TEST	TRUE	PP5V_SW_ODD	7 33 46 (NEED 4 TP)
TEST	TRUE	SMC_ODD_DETECT	33 35
TEST	TRUE	SATA_ODD_D2R_C_P	33 71
TEST	TRUE	SATA_ODD_D2R_C_N	33 71
TEST	TRUE	SATA_ODD_R2D_P	33 71
TEST	TRUE	SATA_ODD_R2D_N	33 71

(NEED TO ADD 4 GND TP)

SATA HDD/SIL FUNC_TEST

TEST	TRUE	PP5V_S0_HDD_FLT	7 33 (NEED 4 TP)
TEST	TRUE	SATA_HDD_R2D_P	33 71
TEST	TRUE	SATA_HDD_R2D_N	33 71
TEST	TRUE	SATA_HDD_D2R_C_P	33 71
TEST	TRUE	SATA_HDD_D2R_C_N	33 71
TEST	TRUE	SYS_LED_ANODE_R	33

(NEED TO ADD 4 GND TP)

BATT POWER CONN FUNC_TEST

TEST	TRUE	PPVBAT_G3H_CONN	34 55 (NEED 3 TP)
TEST	TRUE	SMBUS_SMC_BSA_SCL	38 74
TEST	TRUE	SMBUS_SMC_BSA_SDA	38 74
TEST	TRUE	SYS_DETECT_L	54

(NEED TO ADD 3 GND TP)

HALL EFFECT CONNECTOR FUNC_TEST

TEST	TRUE	PP3V42_G3H	7 8 (NEED 2 TP)
TEST	TRUE	SMC_LID_R	54

(NEED TO ADD 3 GND TP)

X16 WIRELESS CONN FUNC_TEST

TEST	TRUE	PP3V3_S3_BT_F	30
TEST	TRUE	CONN_PCIE_MINI_D2R_P	9 30 75
TEST	TRUE	CONN_PCIE_MINI_D2R_N	9 30 75
TEST	TRUE	CONN_PCIE_MINI_R2D_P	9 30 75
TEST	TRUE	CONN_PCIE_MINI_R2D_N	9 30 75
TEST	TRUE	PCIE_CLK100M_MINI_CONN_P	30 75
TEST	TRUE	PCIE_CLK100M_MINI_CONN_N	30 75
TEST	TRUE	PP3V3_WLAN (NEED 4 TP)	7 30
TEST	TRUE	PCIE_WAKE_L	16 30
TEST	TRUE	CONN_USB2_BT_P	30 75
TEST	TRUE	CONN_USB2_BT_N	30 75
TEST	TRUE	AP_CLKREQ_O_L	30
TEST	TRUE	AP_RESET_CONN_L	30

(NEED TO ADD 4 GND TP)

IPD_FLEX_CONN FUNC_TEST

TEST	TRUE	PP3V3_S3	7 8
TEST	TRUE	PP18V5_S3	7 44
TEST	TRUE	Z2_CS_L	43 44
TEST	TRUE	Z2_DEBUG3	43 44
TEST	TRUE	Z2_MOSI	43 44
TEST	TRUE	Z2_MISO	43 44
TEST	TRUE	Z2_SCLK	43 44
TEST	TRUE	Z2_BOOST_EN	44
TEST	TRUE	Z2_HOST_INTN	43 44
TEST	TRUE	Z2_CLKIN	43 44
TEST	TRUE	Z2_KEY_ACT_L	43 44
TEST	TRUE	Z2_RESET	43 44
TEST	TRUE	PSOC_MISO	43 44
TEST	TRUE	PSOC_MOSI	43 44
TEST	TRUE	PSOC_SCLK	43 44
TEST	TRUE	SMBUS_SMC_A_S3_SDA	38 74
TEST	TRUE	SMBUS_SMC_A_S3_SCL	38 74
TEST	TRUE	PSOC_F_CS_L	43 44
TEST	TRUE	PICKB_L	43 44

(NEED TO ADD 2 GND TP)

KEYBOARD CONN FUNC_TEST

TEST	TRUE	PP3V3_S3	7 8
TEST	TRUE	PP3V42_G3H	7 8
TEST	TRUE	WS_KBD1	43
TEST	TRUE	WS_KBD2	43
TEST	TRUE	WS_KBD3	43
TEST	TRUE	WS_KBD4	43
TEST	TRUE	WS_KBD5	43
TEST	TRUE	WS_KBD6	43
TEST	TRUE	WS_KBD7	43
TEST	TRUE	WS_KBD8	43
TEST	TRUE	WS_KBD9	43
TEST	TRUE	WS_KBD10	43
TEST	TRUE	WS_KBD11	43
TEST	TRUE	WS_KBD12	43
TEST	TRUE	WS_KBD13	43
TEST	TRUE	WS_KBD14	43
TEST	TRUE	WS_KBD15_CAP	43
TEST	TRUE	WS_KBD16_NUM	43
TEST	TRUE	WS_KBD17	43
TEST	TRUE	WS_KBD18	43
TEST	TRUE	WS_KBD19	43
TEST	TRUE	WS_KBD20	43
TEST	TRUE	WS_KBD21	43
TEST	TRUE	WS_KBD22	43
TEST	TRUE	WS_KBD23	43
TEST	TRUE	WS_KBD_ONOFF_L	43
TEST	TRUE	WS_LEFT_SHIFT_KBD	43
TEST	TRUE	WS_LEFT_OPTION_KBD	43
TEST	TRUE	WS_CONTROL_KBD	43

(NEED TO ADD 1 GND TP)

DC POWER CONN FUNC_TEST

TEST	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	54
TEST	TRUE	ADAPTER_SENSE	54

(NEED TO ADD 2 GND TP)

POWER NETS FUNC_TEST

TEST	TRUE	PPVCORE_S0_CPU	8 39
TEST	TRUE	PPVCORE_S0_MCP	8 39
TEST	TRUE	PP1V05_S0	8 62
TEST	TRUE	PP1V5_S0	8 62 75
TEST	TRUE	PP1V8_S0	8
TEST	TRUE	PP5V_S0	7 8 62
TEST	TRUE	PP5V_S0	7 8 62
TEST	TRUE	PP3V3_S0	8 62 75
TEST	TRUE	PP1V5R1V35_S3	8 75
TEST	TRUE	PP3V3_S3	7 8
TEST	TRUE	PP5V_S3	8
TEST	TRUE	PP3V3_S5	8 62 75
TEST	TRUE	PP3V42_G3H	7 8
TEST	TRUE	PPBUS_G3H	8 39
TEST	TRUE	PP0V9_ENET	8
TEST	TRUE	PP3V3_ENET	8
TEST	TRUE	PP3V3_G3_RTC	8 19 20 23
TEST	TRUE	PP3V3_WLAN	7 30
TEST	TRUE	PP5V_SW_ODD	7 33 46
TEST	TRUE	PP5V_S0_HDD_FLT	7 33
TEST	TRUE	PP3V3_S5_AVREF_SMC	35 36
TEST	TRUE	PP18V5_S3	7 44
TEST	TRUE	PP3V3_SW_LCD_PANEL_F	7 44
TEST	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67
TEST	TRUE	PP4V5_AUDIO_ANALOG	48
TEST	TRUE	SMC_PM_G2_EN	35 62
TEST	TRUE	PM_SLP_S4_L	19 35 36 62
TEST	TRUE	PM_SLP_S3_L	19 35 62 66
TEST	TRUE	PP5V_S3_CAMERA_F	7 44
TEST	TRUE	PP0V9_S5	8
TEST	TRUE	PPDDRVTT_S0	8
TEST	TRUE	PP1V05_S0_MCP_PLL_UP	8
TEST	TRUE	PPVTT_S3_DDR_BUF	8

(NEED TO ADD 6 GND TP)

FSB SIGNALS WITH NOTEST

TEST	NO TEST	FSB_A_L<35..3>	10 14 69
TEST	NO TEST	FSB_ADS_L	10 14 69
TEST	NO TEST	FSB_ADSTB_L<1..0>	10 14 69
TEST	NO TEST	FSB_D_L<63..0>	10 14 69
TEST	NO TEST	FSB_DINV_L<3..0>	10 14 69
TEST	NO TEST	FSB_DSTB_L_N<3..0>	10 14 69
TEST	NO TEST	FSB_DSTB_L_P<3..0>	10 14 69
TEST	NO TEST	FSB_HIT_L	10 14 69
TEST	NO TEST	FSB_HITM_L	10 14 69
TEST	NO TEST	FSB_LOCK_L	10 14 69
TEST	NO TEST	FSB_REQ_L<4..0>	10 14 69

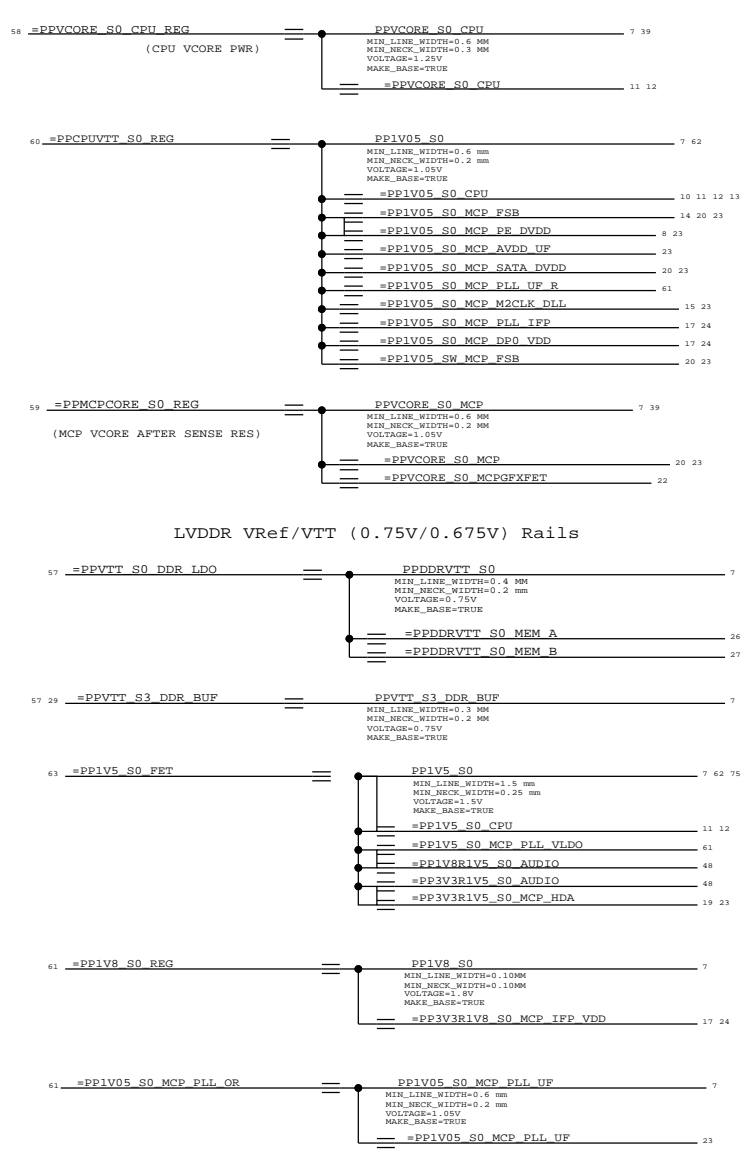
J5100 LPC+SPI CONN FUNC_TEST

TEST	TRUE	PP3V42_G3H	7 8
TEST	TRUE	SPI_CLK	37 72
TEST	TRUE	SPI_CS0_L	37 72
TEST	TRUE	SPI_MISO	19 37 72
TEST	TRUE	SPI_MOSI	37 72
TEST	TRUE	SPIROM_USE_MLB	19 37 47
TEST	TRUE	LPPLUS_GPIO	19 37
TEST	TRUE	LPC_SERIRO	19 35 37
TEST	TRUE	SMC_TMS	35 36 37

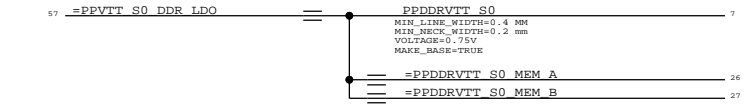
(NEED TO ADD 2 GND TP)

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
FUNC TEST			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		SHEET	7 OF 76

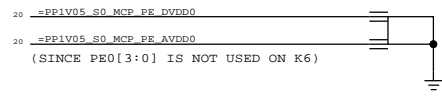
"S0,S0M" RAILS



LVDDR VRef/VTT (0.75V/0.675V) Rails

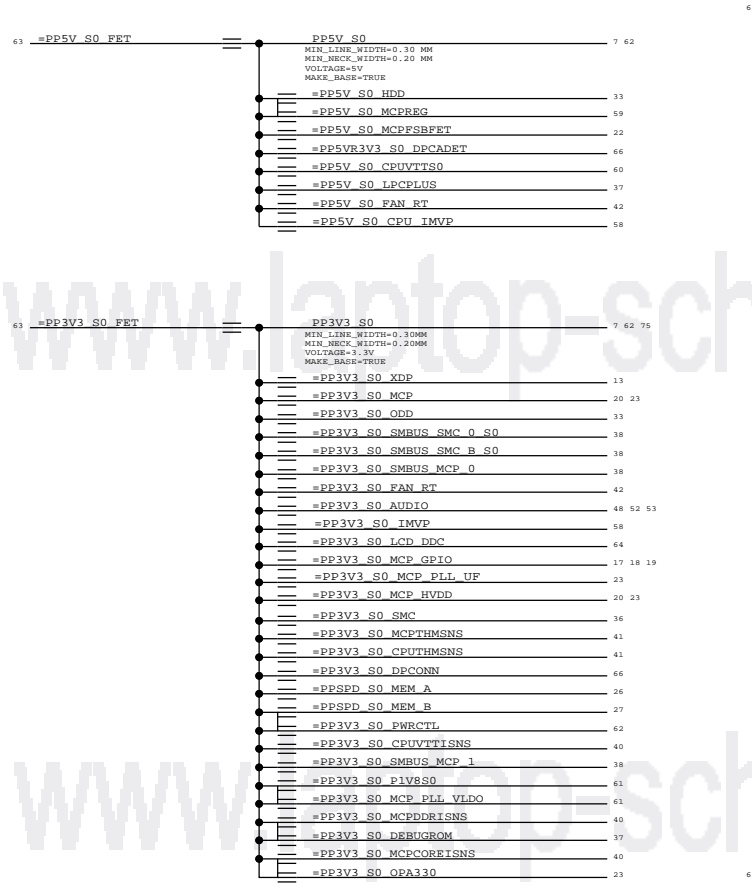


UNUSED MCP PE0[3:0] AVDD/DVDD

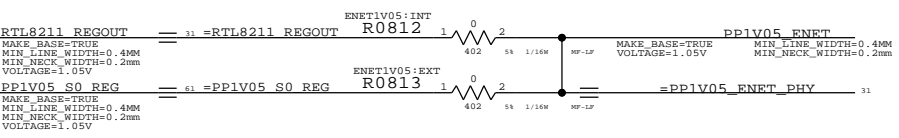
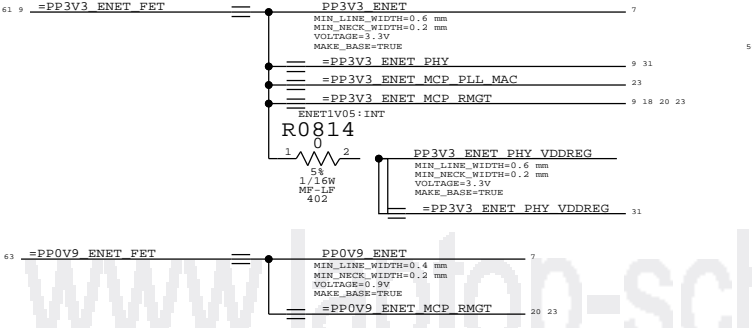


(CONNECTS TO MCP BALLS) 20 =PPIV05_S0 MCP PE DVDD1 ... (CONNECTS TO THE DECAPS) 21

"S3" RAILS

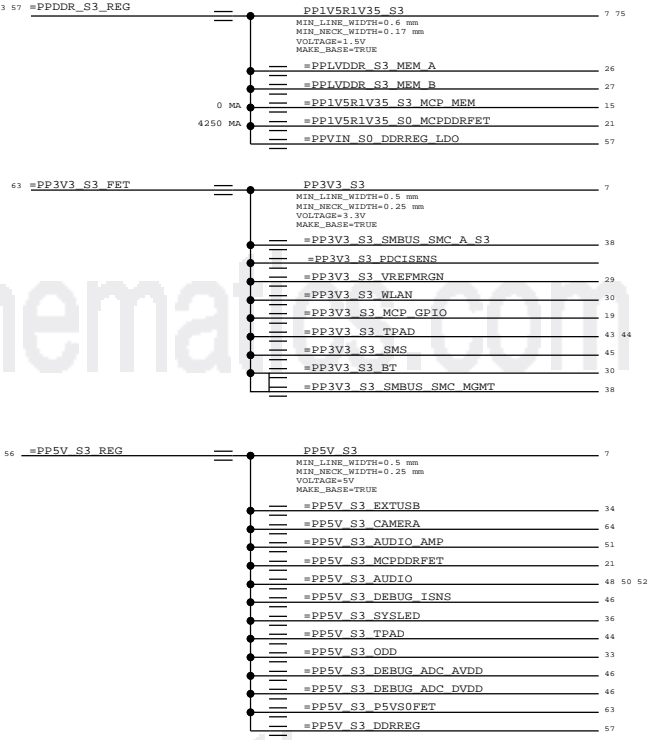


"ENET" RAILS

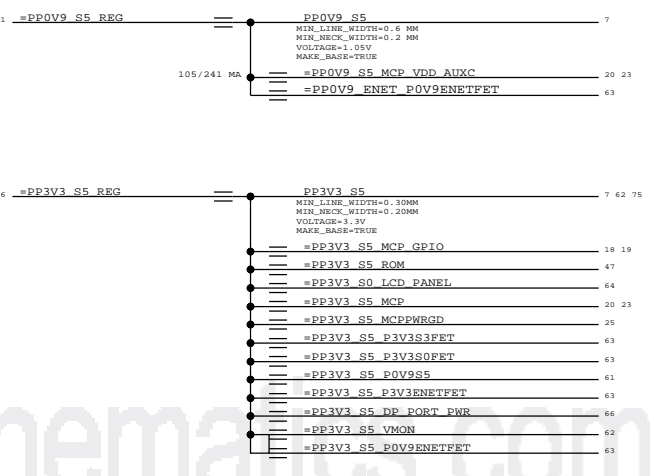


FIX ME!! OUTPUT OF REGULATOR VALUES

"S3" RAILS



"S5" RAILS



"G3H" RAILS

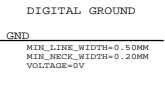
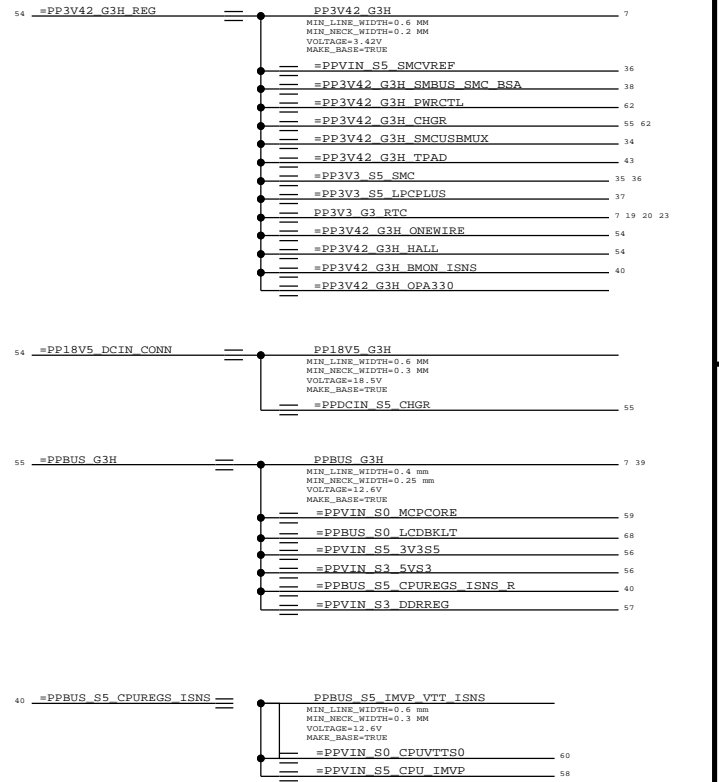
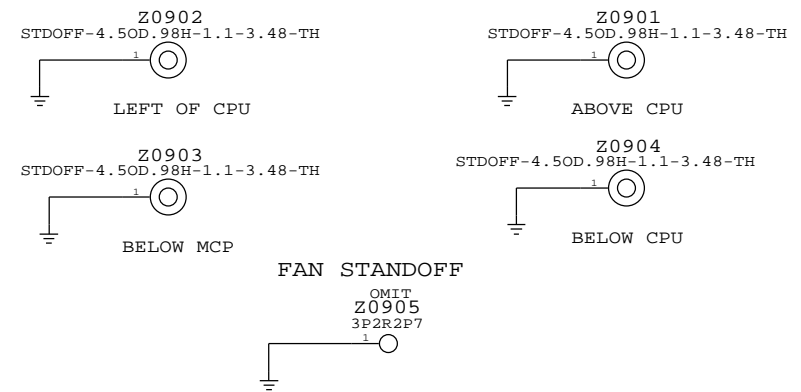


Table with drawing information: SYNC MASTER=MASTER, SYNC DATE=MASTER, Power Aliases, Apple Inc., DRAWING NUMBER 051-8561, REVISION C.0.0, PAGE 8 OF 109, SHEET 8 OF 76.

HEATSINK STANDOFFS



PCI-E ALIASES

Table of PCI-E aliases including PCIE MINI R2D C P, PCIE AP R2D C P, PCIE MINI R2D C N, PCIE AP R2D C N, and various unused GPU lanes.

USB ALIASES

Table of USB aliases including USB EXTD P, USB EXTD N, USB EXTC P, USB EXTC N, USB MINI P, USB MINI N, USB SDCARD P, USB SDCARD N, USB WM P, USB WM N, USB IR P, USB IR N, USB T57 P, and USB T57 N.

ETHERNET ALIASES

Table of Ethernet aliases including TP ENET RESET L, TP MCP CLK25M BUFO_R, TP ENET MDC, TP ENET TX_CTRL, TP ENET CLK125M TXCLK, and TP ENET TXD<0..3>.

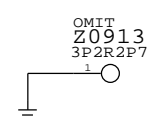
MLB MOUNTING (TO C. BRACKET) SCREW HOLES



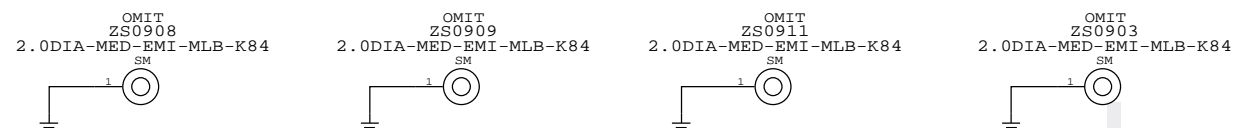
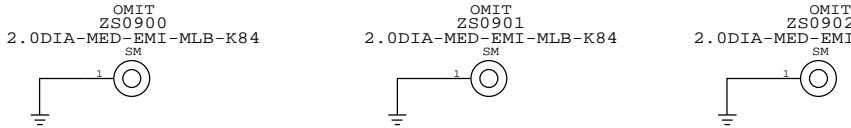
MLB MOUNTING (TO TOPCASE) SCREW HOLES



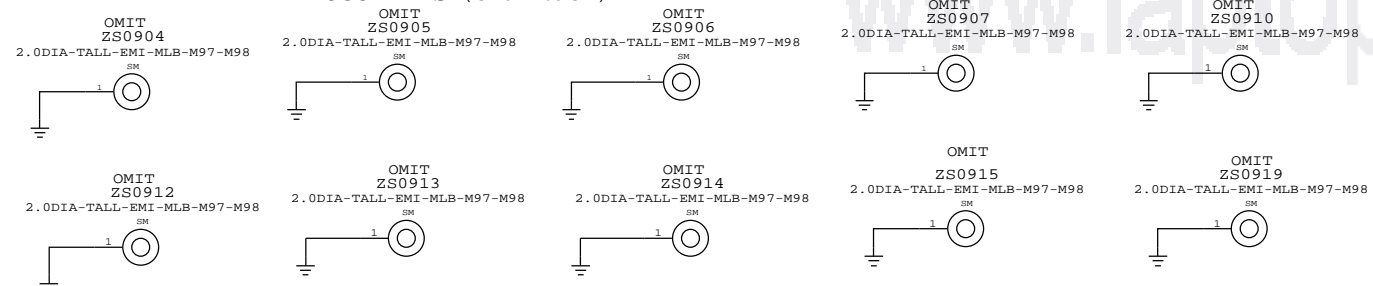
LVDS CONNECTOR HOLE



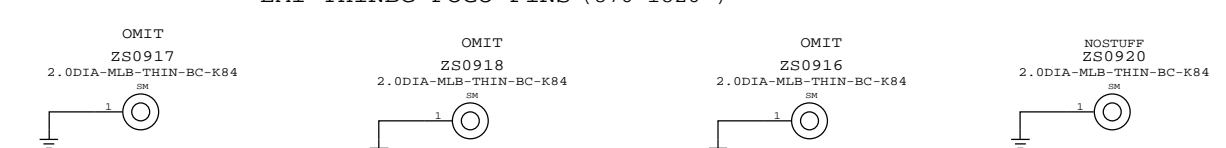
EMI IO MEDIUM POGO PINS (870-1794)



EMI TALL POGO PINS (870-1698)



EMI THINBC POGO PINS (870-1820)



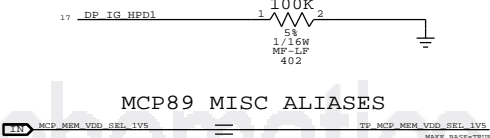
LVDS ALIASES

Table of LVDS aliases including MCP IFPA TXD P<0..2>, MCP IFPA TXD N<0..2>, MCP IFPA DDC CLK, MCP IFPA DDC DATA, MCP IFPA TXD P<3>, MCP IFPA TXD N<3>, MCP IFPB TXC P, MCP IFPB TXC N, MCP IFPB TXD P<0..3>, MCP IFPB TXD N<0..3>, LCD IG BKLT PWM, LCD IG BKLT EN, LCD IG PWR EN, MCP IFPA TXC P, MCP IFPA TXC N, and various LVDS IG A and B data and clock signals.

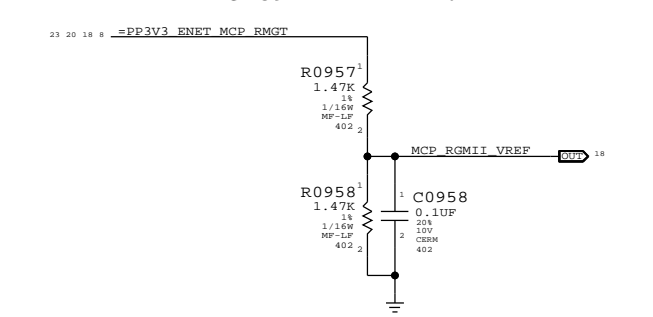
DISPLAY PORT ALIASES

Table of Display Port aliases including DP IG ML0 P<0..3>, DP IG ML0 N<0..3>, DP IG AUX CH0 P, DP IG AUX CH0 N, DP IG MLI P<0..3>, DP IG MLI N<0..3>, DP IG AUX CH1 P, DP IG AUX CH1 N, DP IG HPD0, DP AUX CH C N, DP AUX CH C P, DP CA DET, DP EXT ML P<0..3>, DP EXT ML N<0..3>, DP EXT HPD, DP EXT AUX CH C N, DP EXT AUX CH C P, and DP EXT CA DET.

MCP89 MISC ALIASES



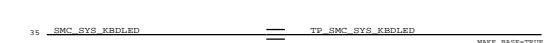
MCP89 ETHERNET VREF



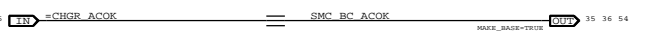
CPU FSB FREQUENCY STRAPS

Table for CPU FSB FREQUENCY STRAPS showing CPU_BSEL<0:2>, CPU_PECI_MCP, and BSEL<2..0> with corresponding FSB MHz values.

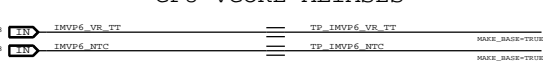
SMC ALIASES



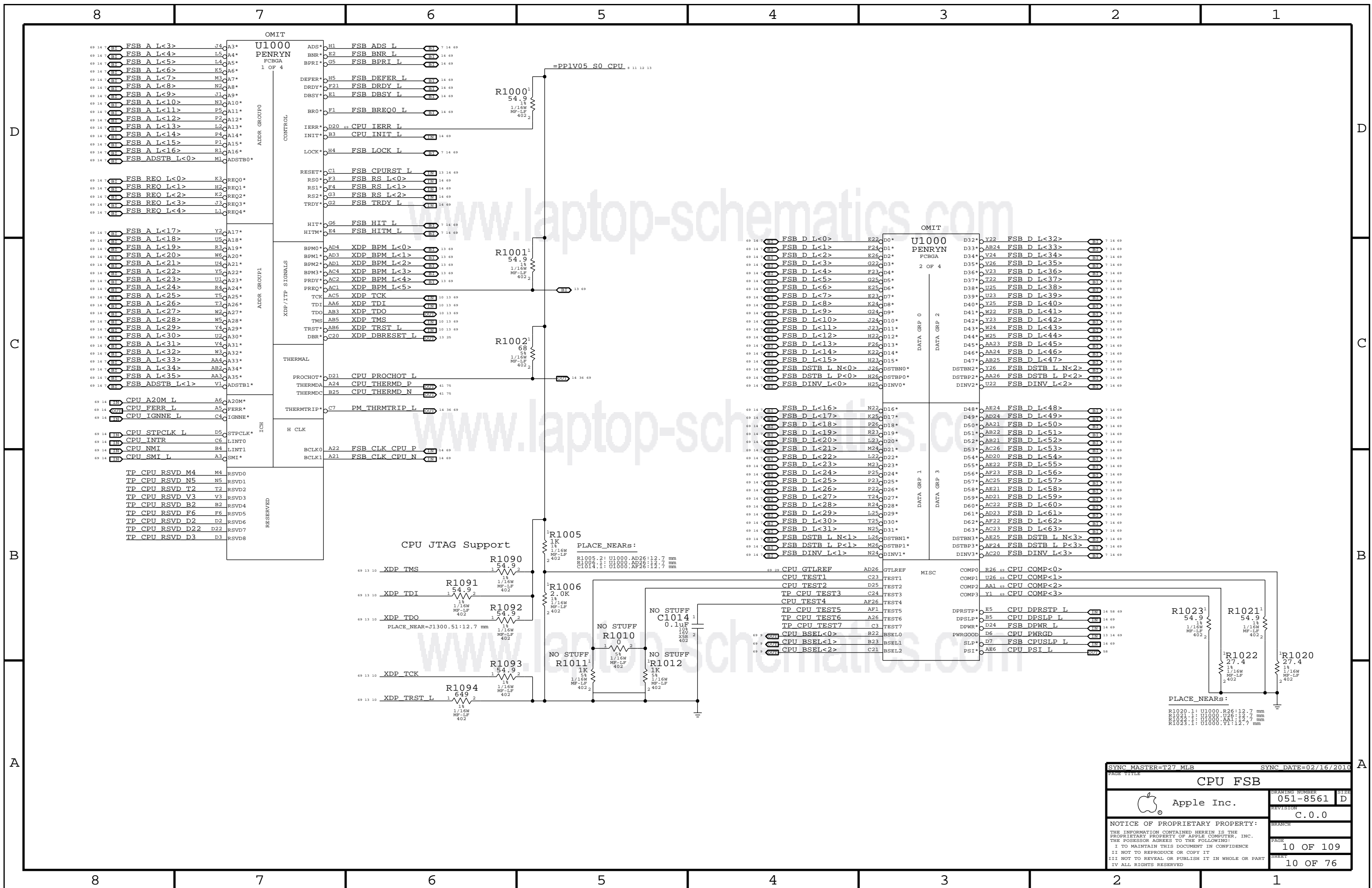
CHARGER SIGNAL



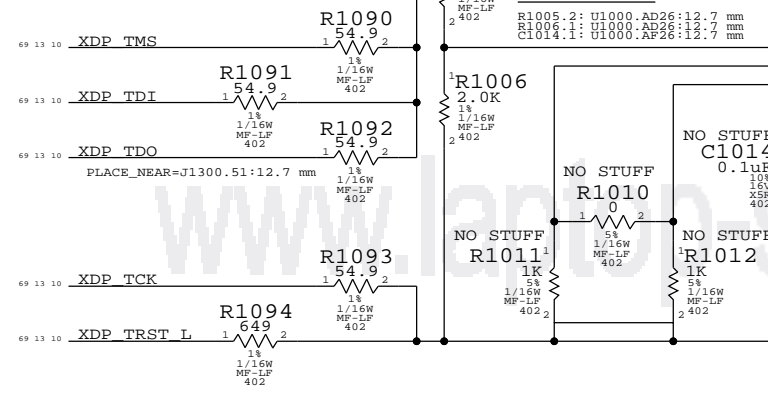
CPU VCORE ALIASES



Metadata block containing SYNC MASTER, SYNC DATE, SIGNAL ALIAS, Apple Inc. logo, DRAWING NUMBER (051-8561), REVISION (C.0.0), and NOTICE OF PROPRIETARY PROPERTY.



CPU JTAG Support



PLACE_NEARS:

R1020.1: U1000.R26:12.7 mm
 R1021.1: U1000.U26:12.7 mm
 R1022.1: U1000.AA1:12.7 mm
 R1023.1: U1000.Y1:12.7 mm

SYNC MASTER=T27 MLB SYNC DATE=02/16/2010

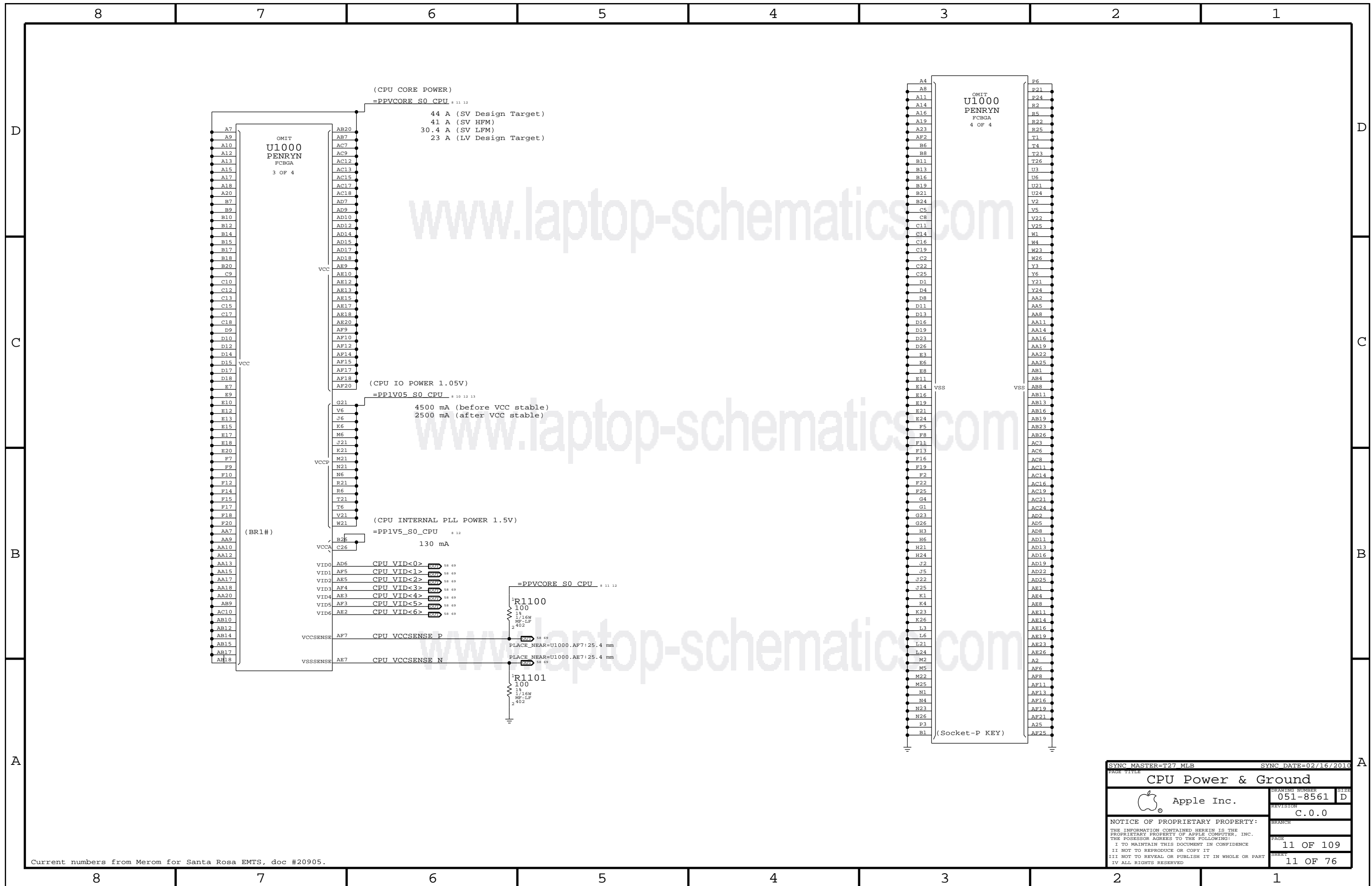
CPU FSB

Apple Inc. DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

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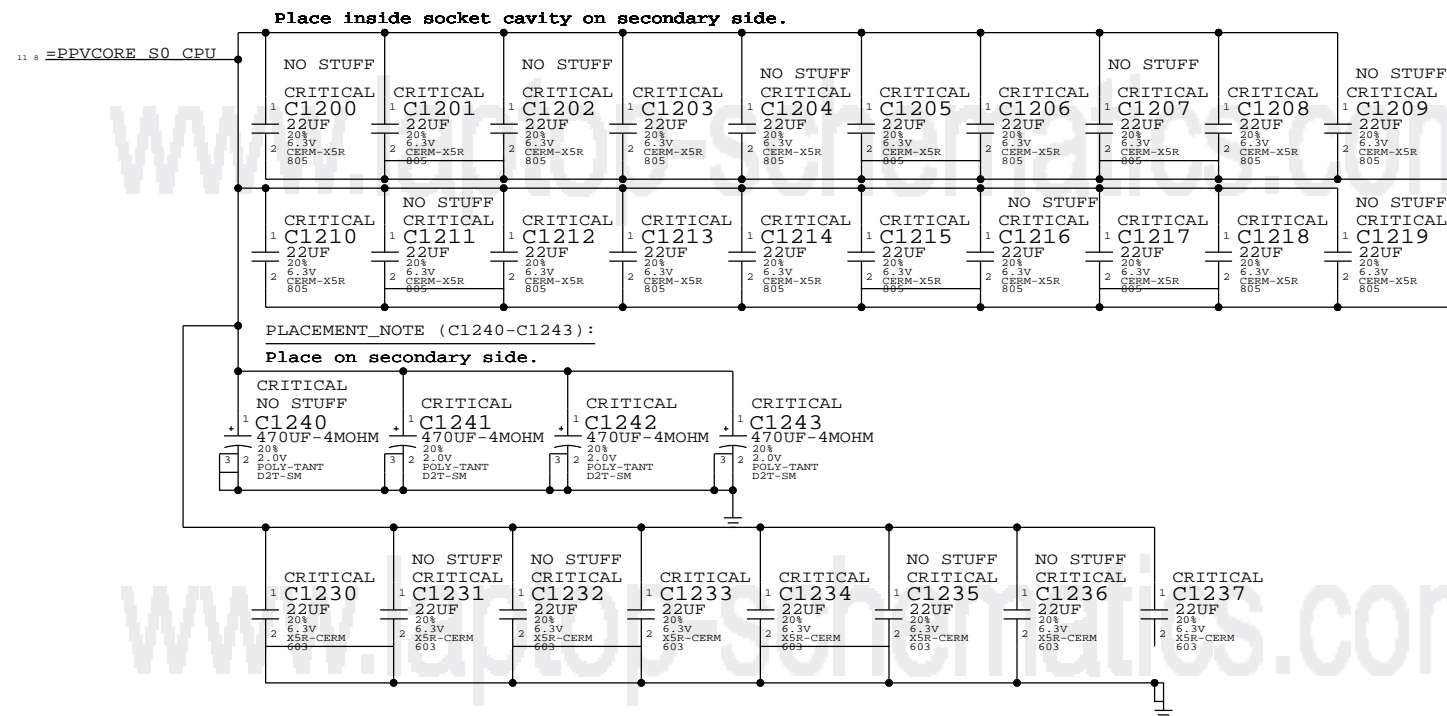
www.laptop-schematics.com

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
CPU Power & Ground			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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CPU VCore HF and Bulk Decoupling

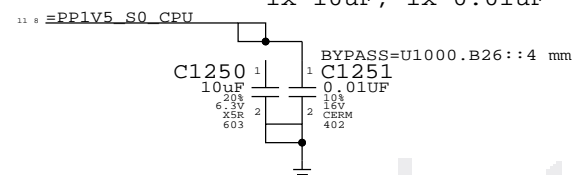
4X 330UF, 20X 22UF 0805

PLACEMENT_NOTE (C1200-C1219):



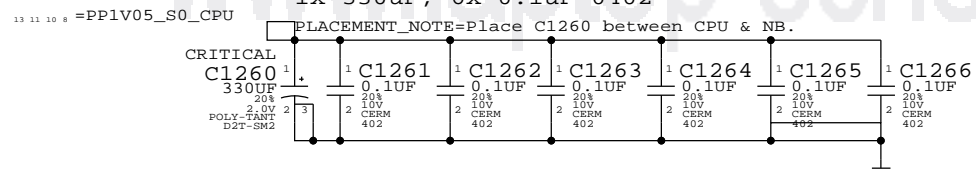
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

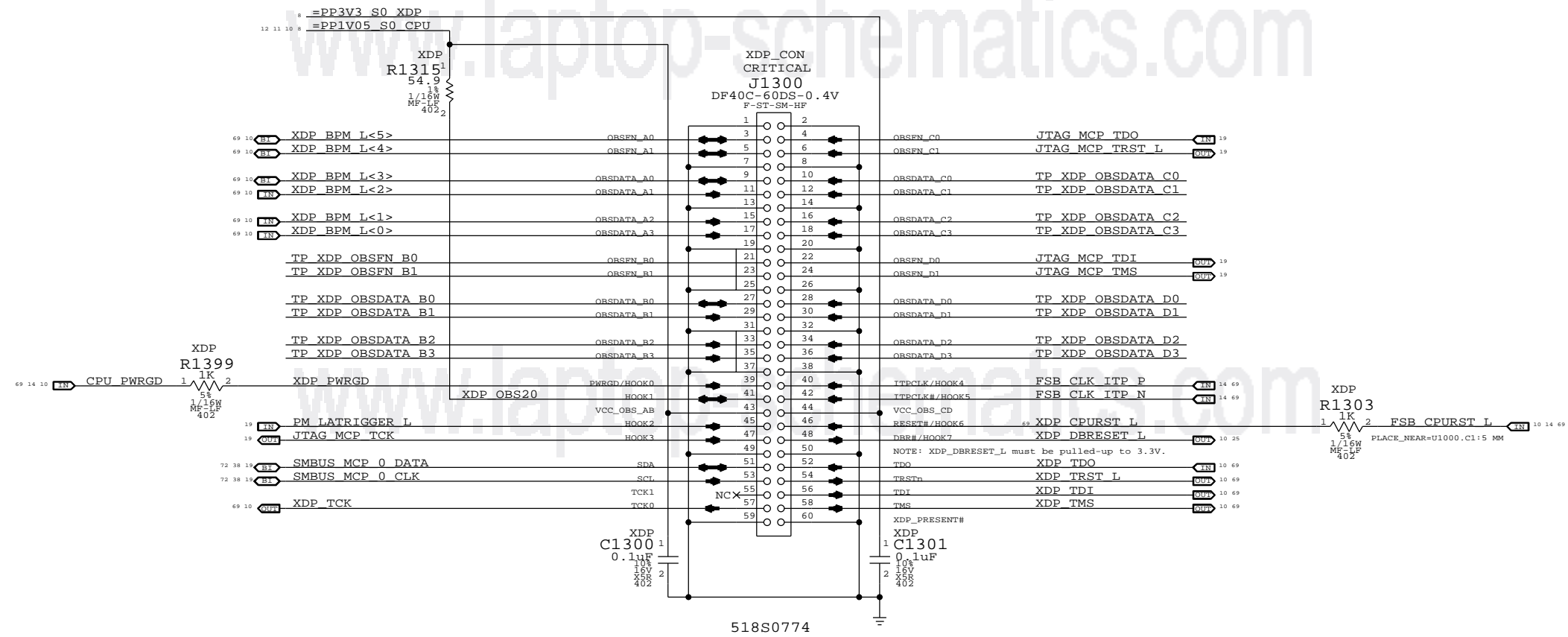


SYNC_MASTER=T27_MLB		SYNC_DATE=02/16/2010	
PAGE TITLE CPU Decoupling			
Apple Inc.	DRAWING NUMBER	051-8561	SIZE D
	REVISION	C.0.0	
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		SHEET	12 OF 76

Mini-XDP Connector

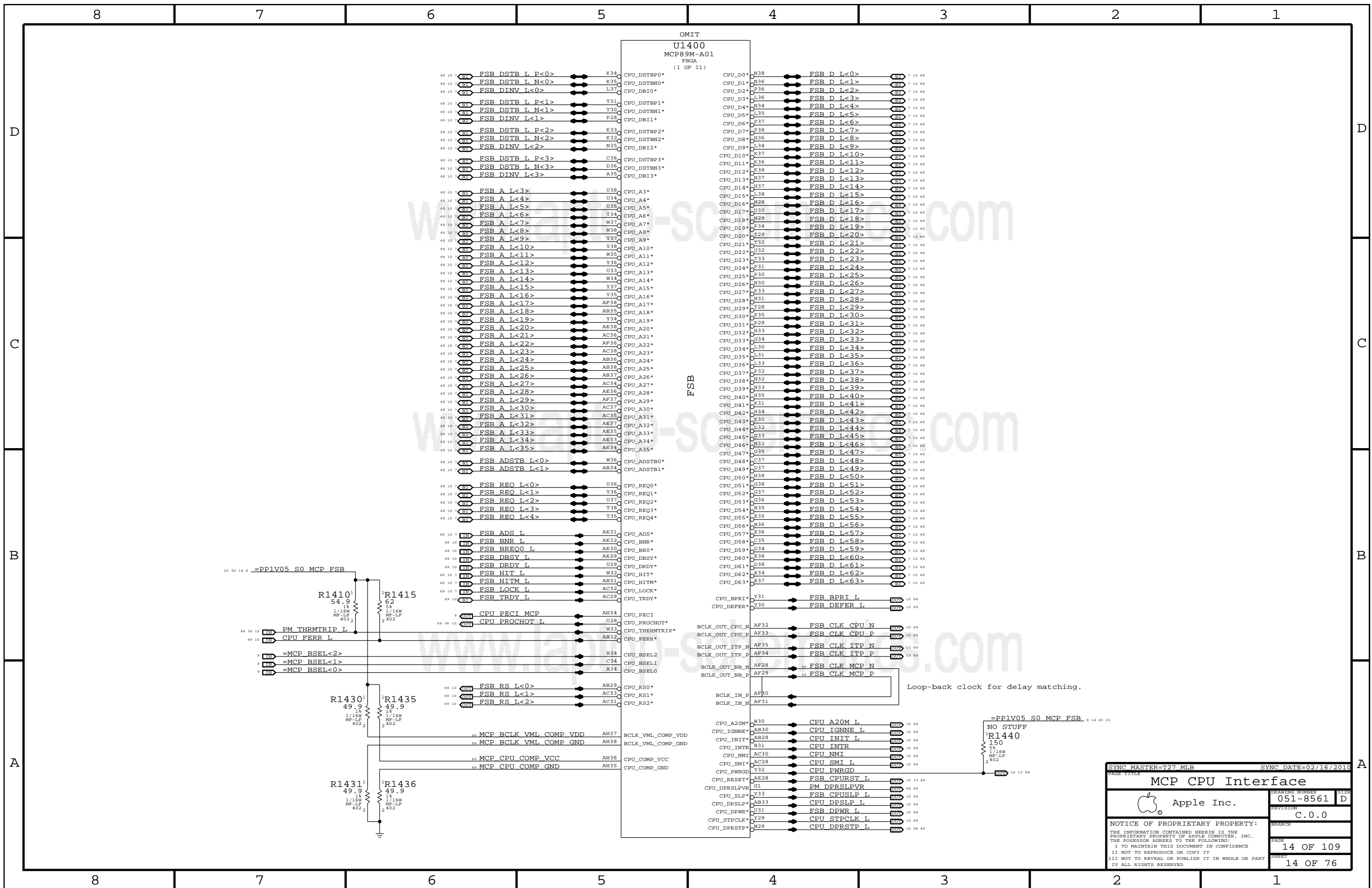
NOTE: This is not the standard XDP pinout.
USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP89-SPECIFIC PINOUT

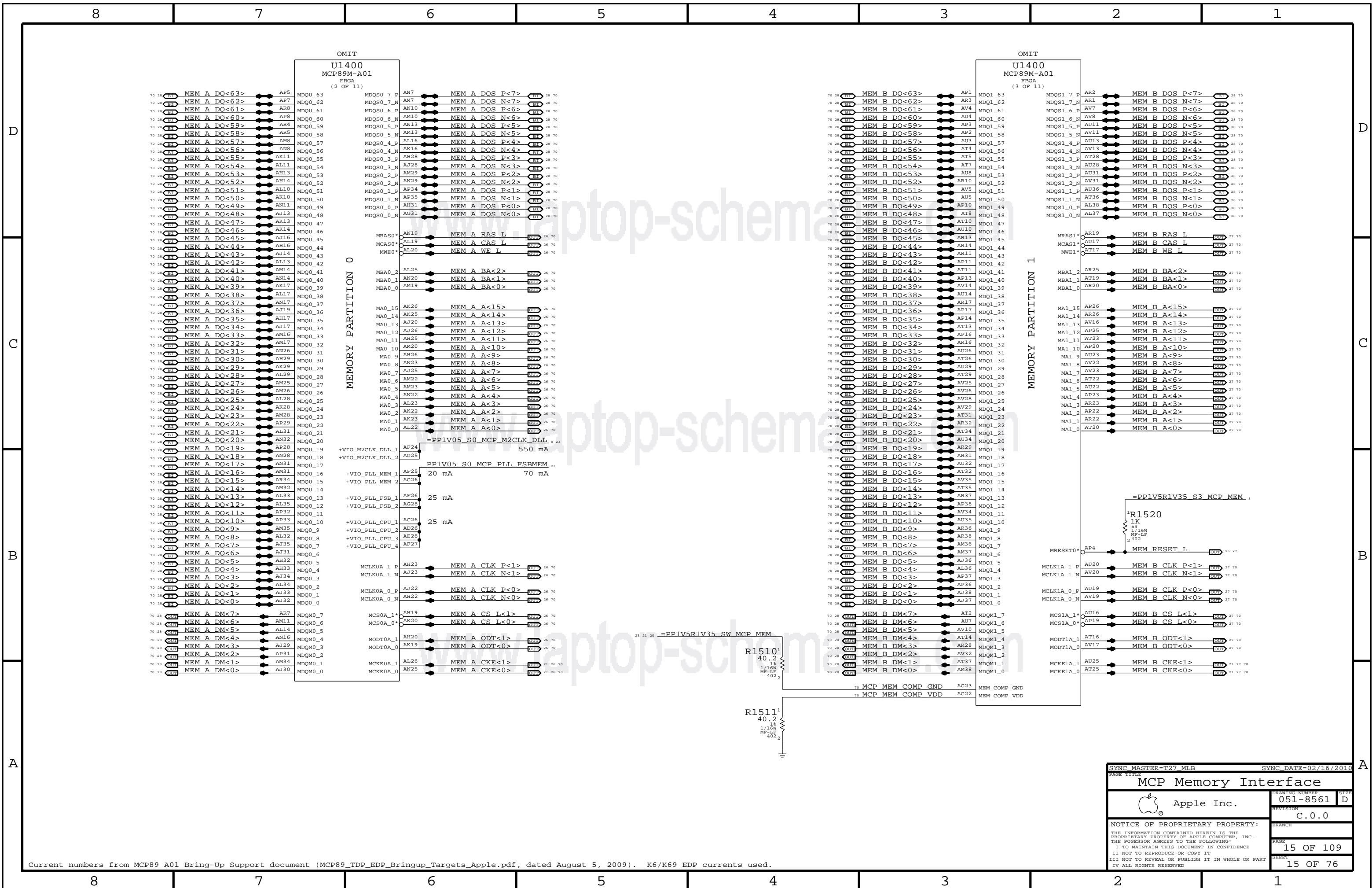


← Direction of XDP module
Please avoid any obstructions
ON ODD-NUMBERED SIDE OF J1300

SYNC MASTER=(K84 MLB)		SYNC DATE=(02/25/2009)	
eXtended Debug Port (MiniXDP)			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		SHEET	13 OF 76

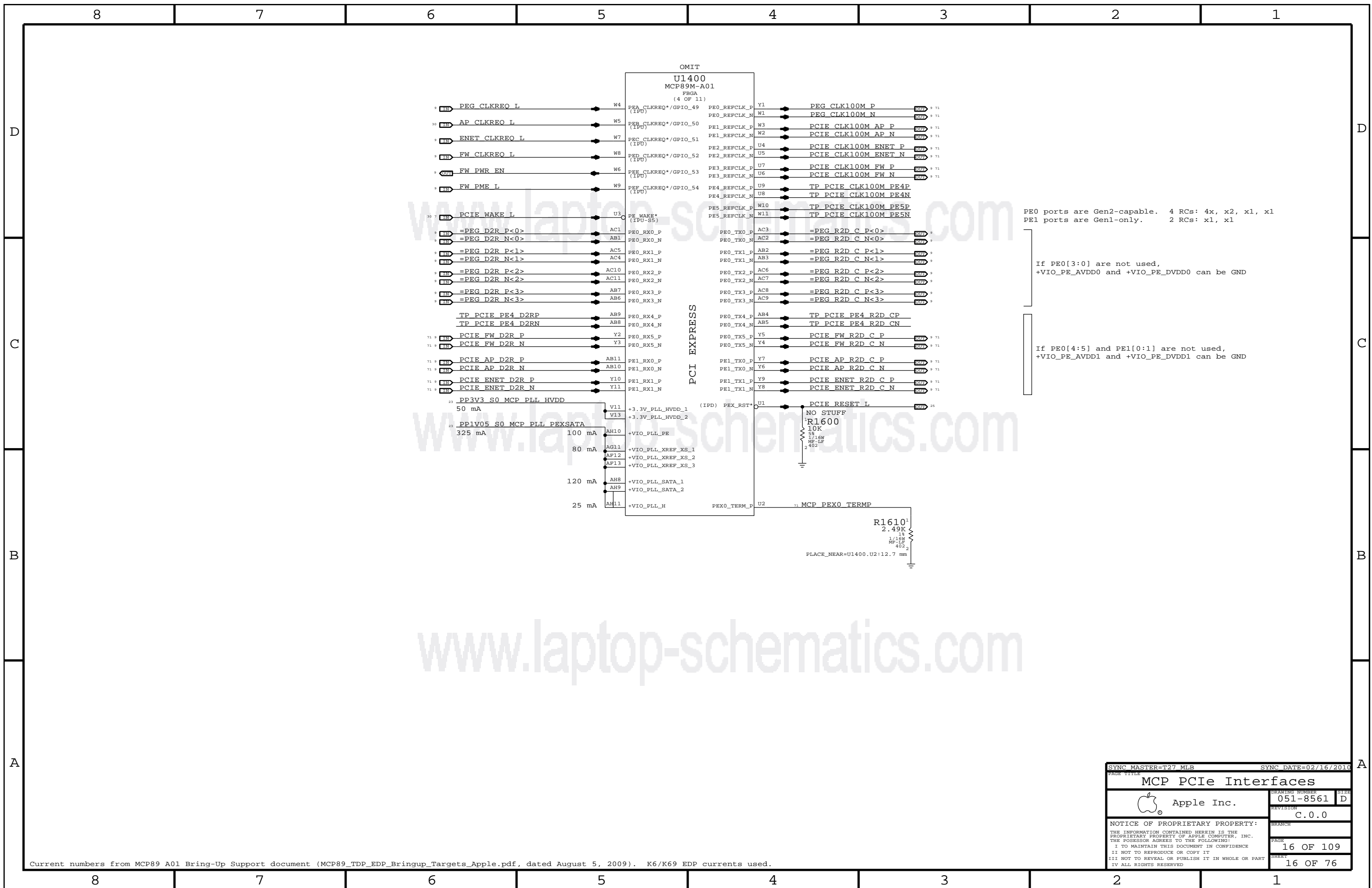


PAGE TITLE		SYNC DATE=02/16/2010	
MCP CPU Interface		DRAWING NUMBER	051-8561
Apple Inc.		REVISION	C.0.0
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Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
MCP Memory Interface		DRAWING NUMBER	SIZE
Apple Inc.		051-8561	D
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		PAGE	SHEET
		15 OF 109	15 OF 76



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SYNC_MASTER=T27_MLB		SYNC_DATE=02/16/2010	
MCP PCIe Interfaces			
Apple Inc.		DRAWING NUMBER	051-8561
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D

D

C

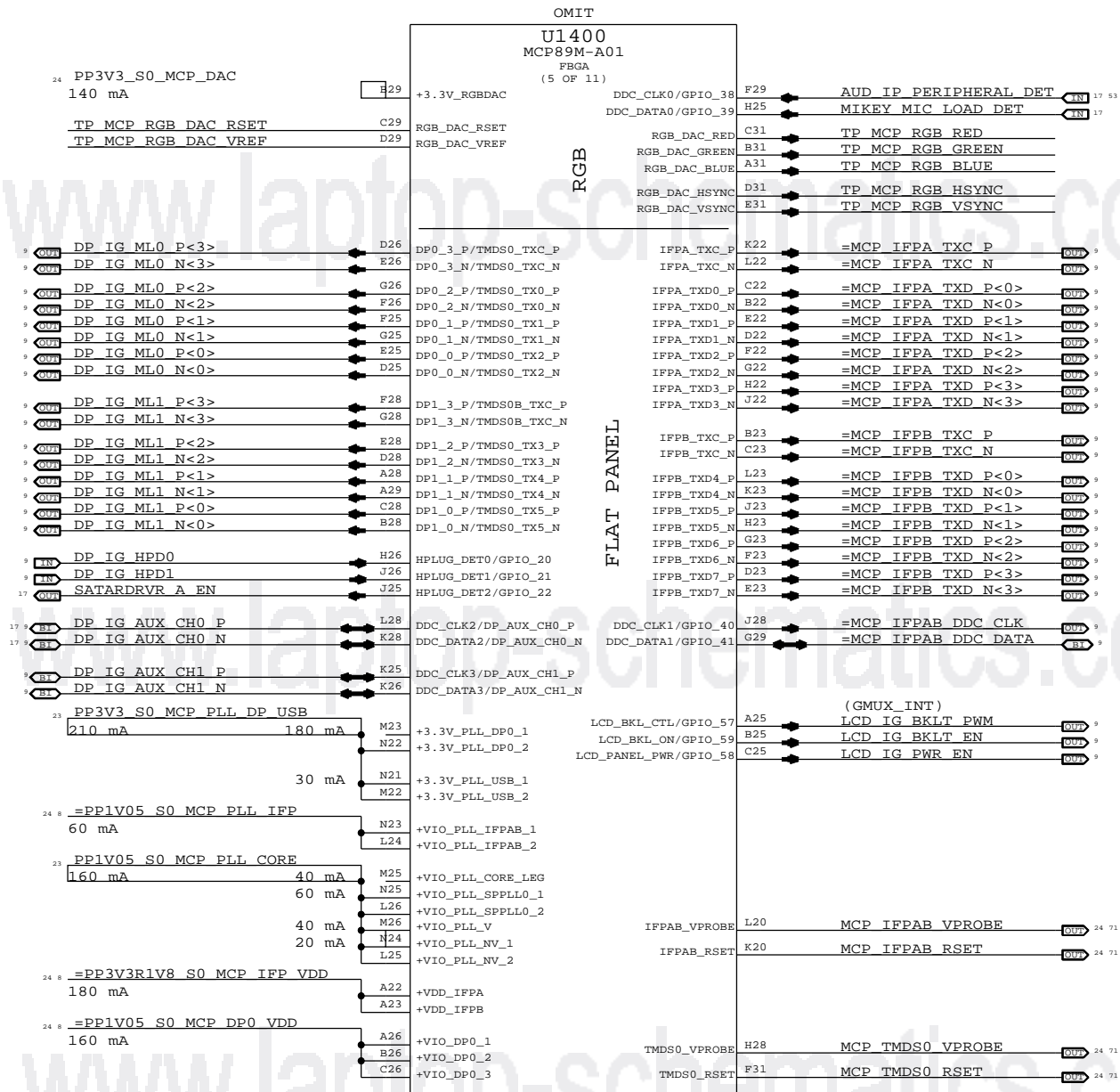
C

B

B

A

A



RGB DAC Disable:
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
 Connect +3.3V_RGBDAC pin to GND.
 NOTE: No Composite/S-Video/Component Video support on MCP89

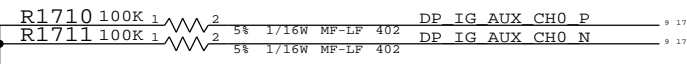
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
 TMDS: Power +VDD_IFPx at 3.3V
 NOTE: TMDS/HDMI not supported on IFPA/B for MCP89 A01.

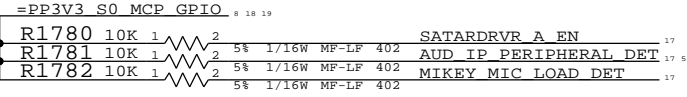
NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

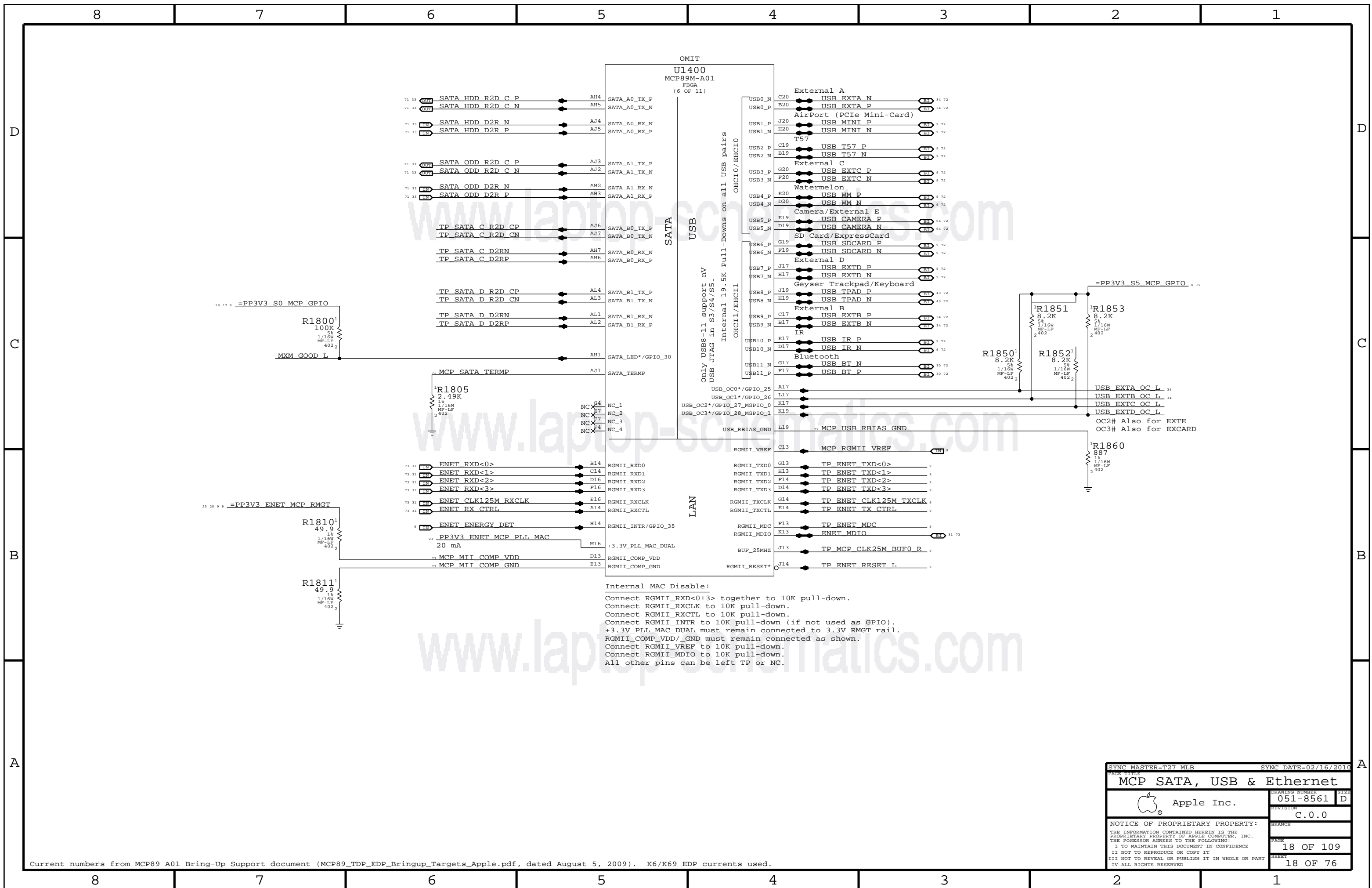


GPIO Pull-Ups



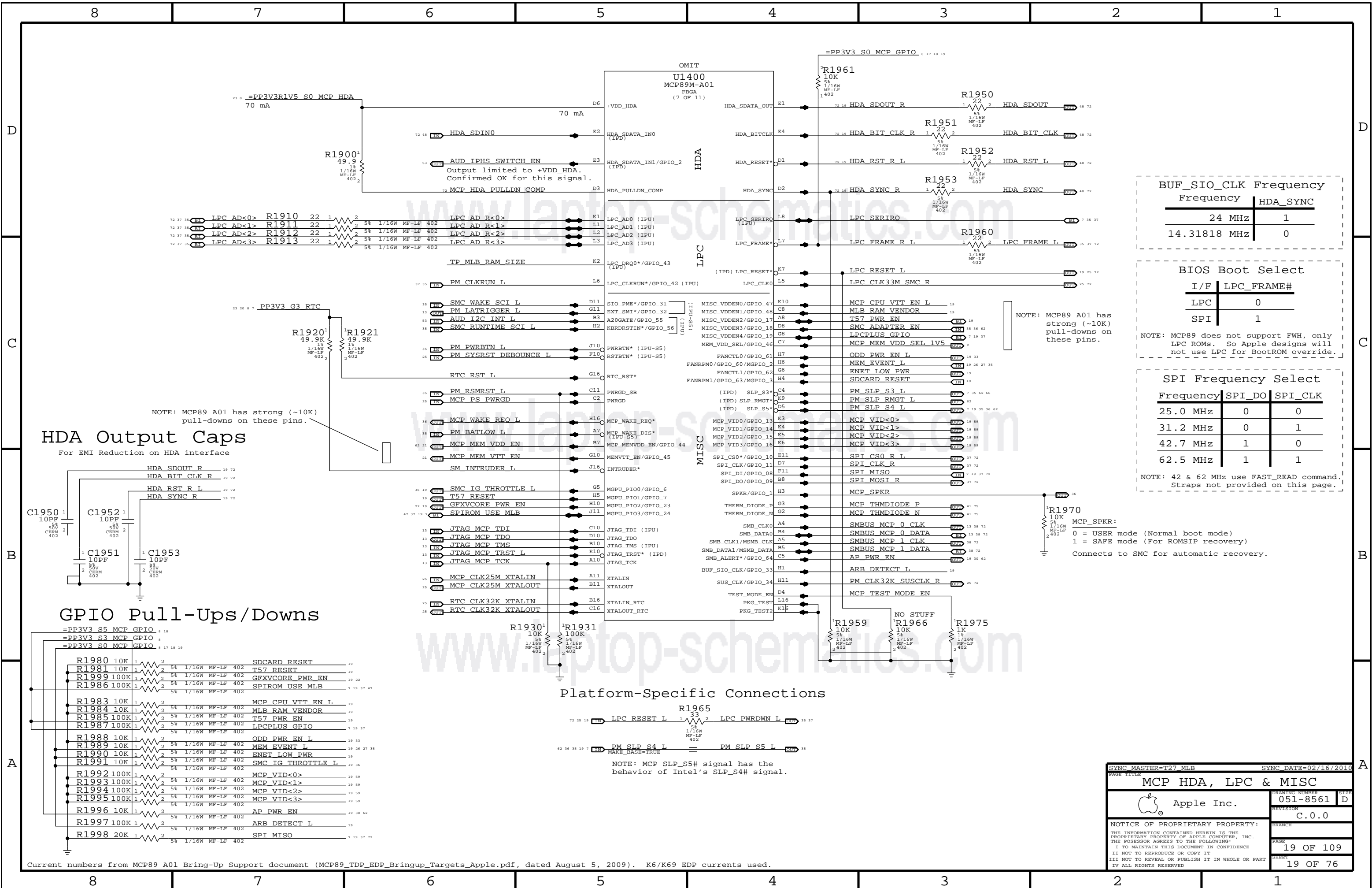
Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
MCP Graphics			
Apple Inc.		DRAWING NUMBER 051-8561	SIZE D
		REVISION C.0.0	BRANCH
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		PAGE 17 OF 109	SHEET 17 OF 76



Internal MAC Disable:
 Connect RGMII_RXD<0:3> together to 10K pull-down.
 Connect RGMII_RXCLK to 10K pull-down.
 Connect RGMII_RXCTL to 10K pull-down.
 Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
 +3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
 RGMII_COMP_VDD/_GND must remain connected as shown.
 Connect RGMII_VREF to 10K pull-down.
 Connect RGMII_MDIO to 10K pull-down.
 All other pins can be left TP or NC.

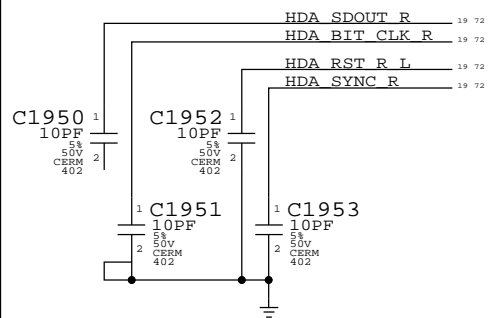
SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE MCP SATA, USB & Ethernet			
Apple Inc.	DRAWING NUMBER	051-8561	SIZE D
	REVISION	C.0.0	
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		SHEET	18 OF 76



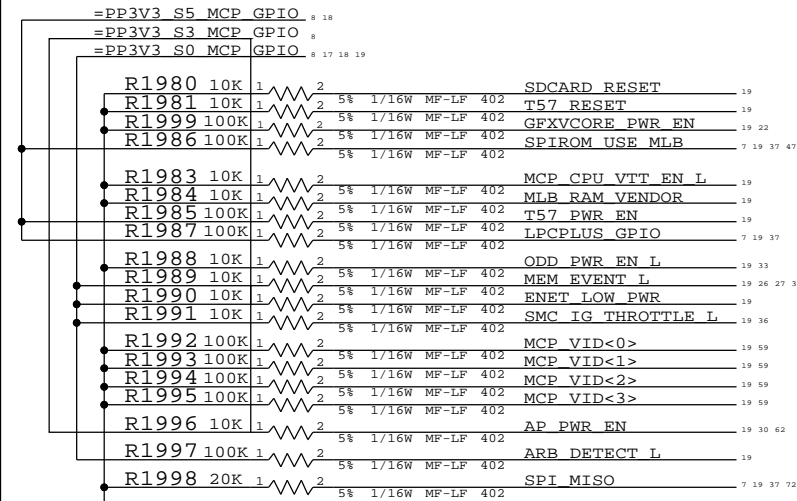
NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

HDA Output Caps

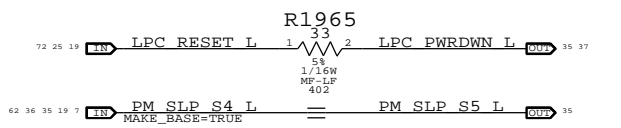
For EMI Reduction on HDA interface



GPIO Pull-Ups/Downs



Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Intel's SLP_S4# signal.

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select	
I/F	LPC_FRAME#
LPC	0
SPI	1

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

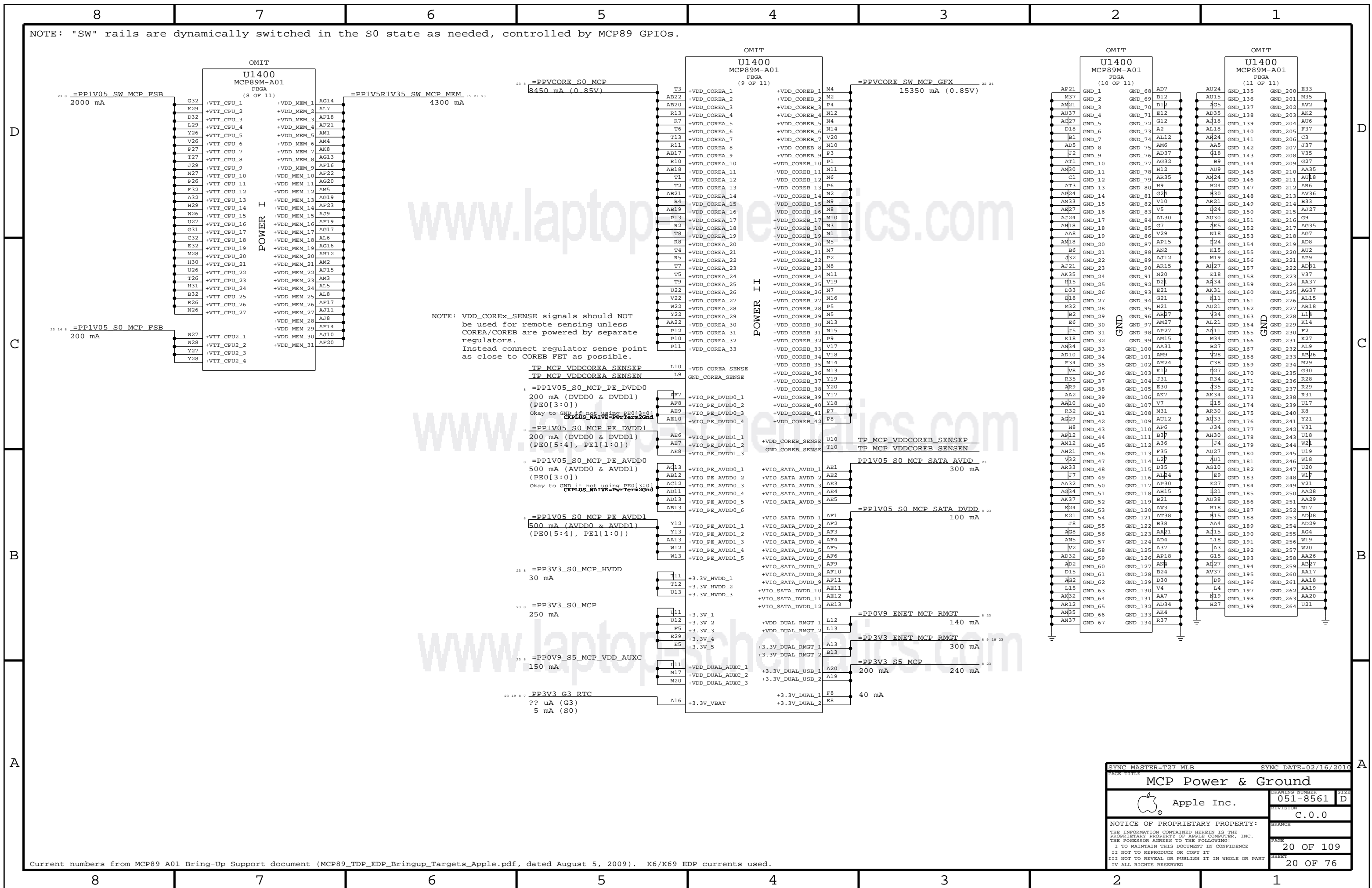
NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

SYNC MASTER=T27_MLB		SYNC DATE=02/16/2010	
MCP HDA, LPC & MISC			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		SHEET	19 OF 76

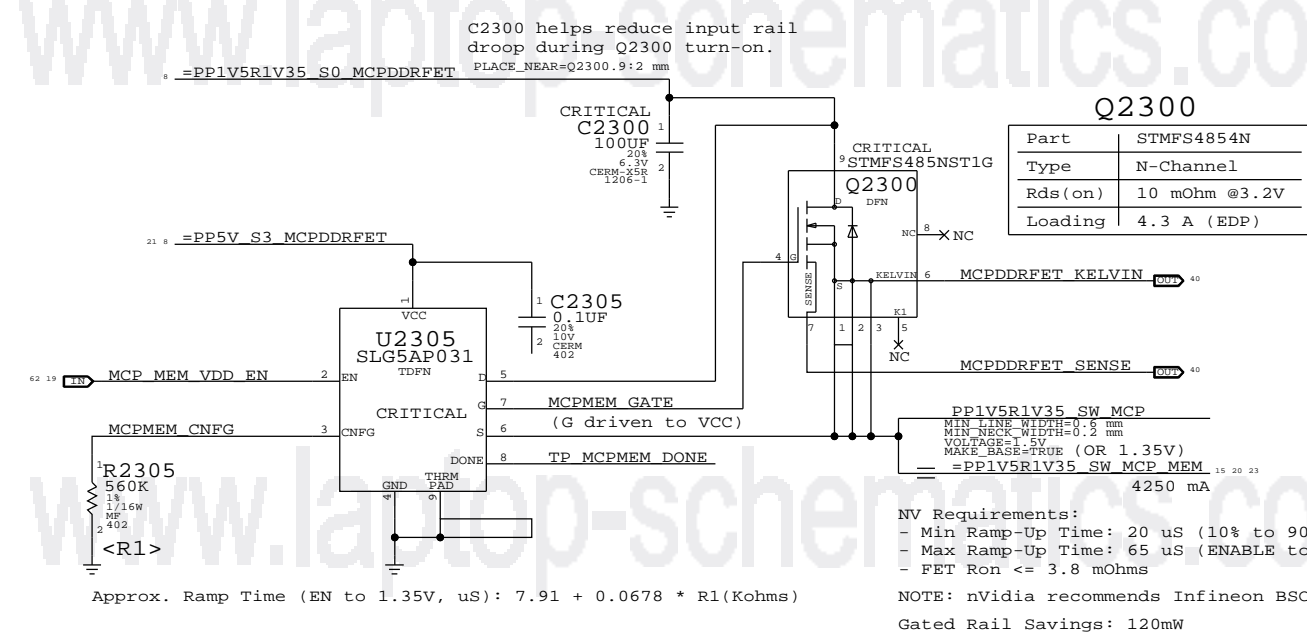
NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.



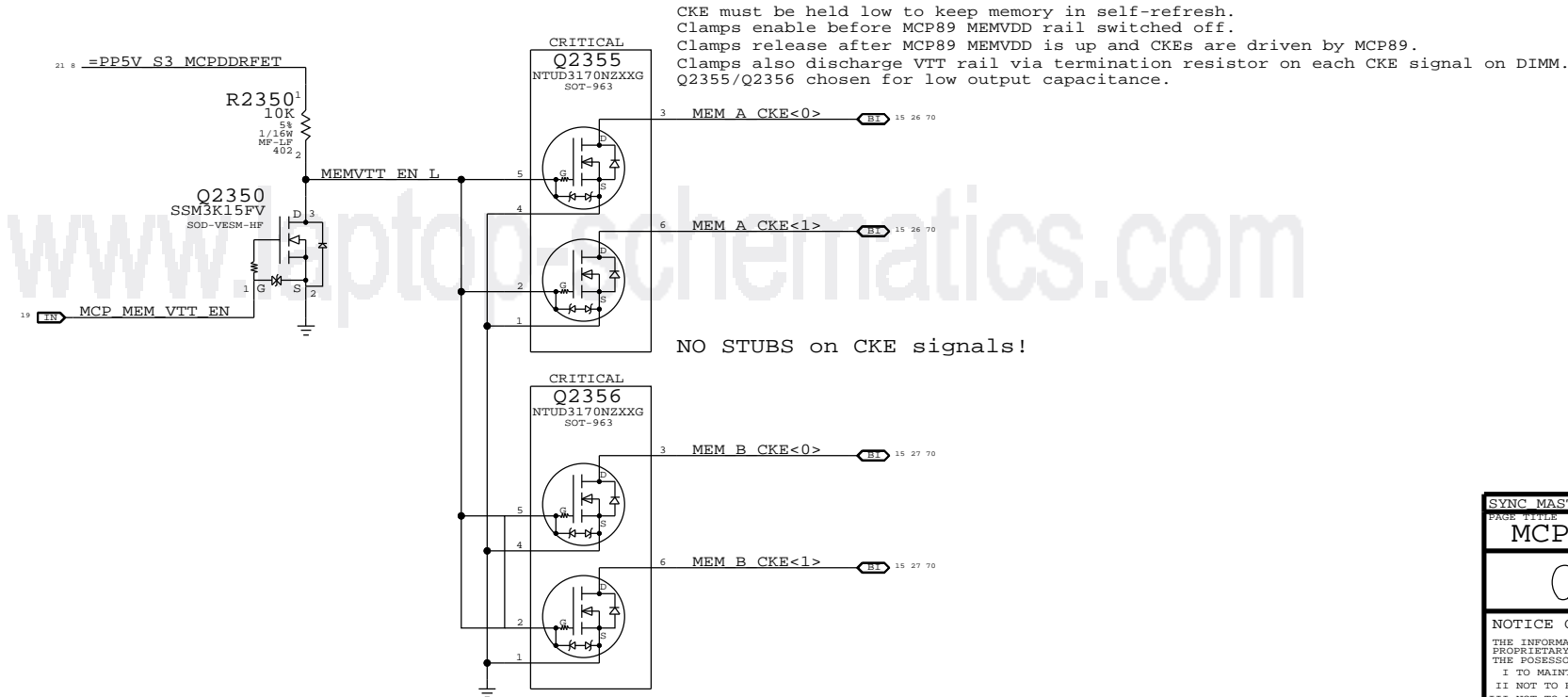
NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators. Instead connect regulator sense point as close to COREB FET as possible.

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
MCP Power & Ground			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		SHEET	20 OF 76

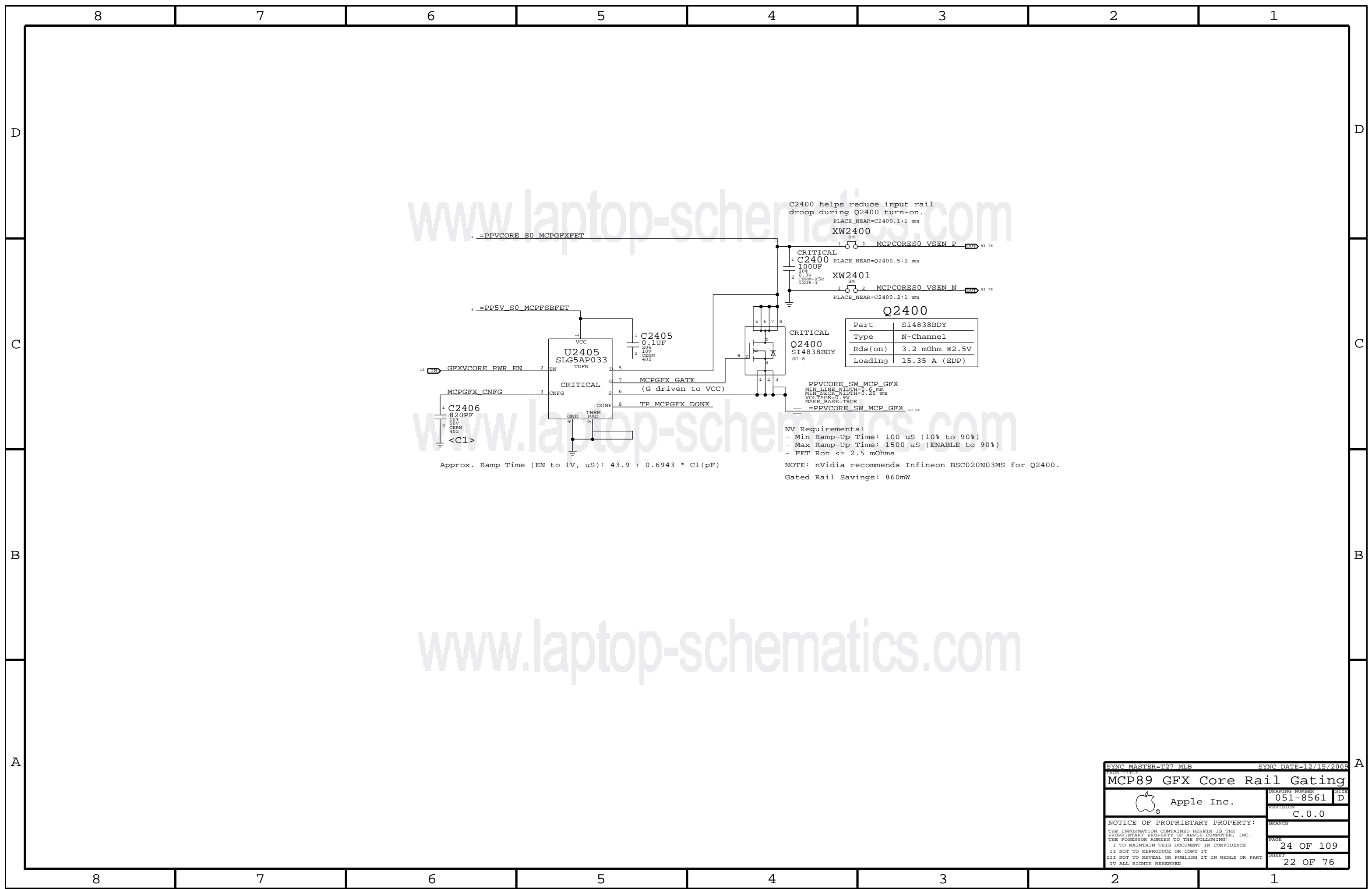
www.laptop-schematics.com



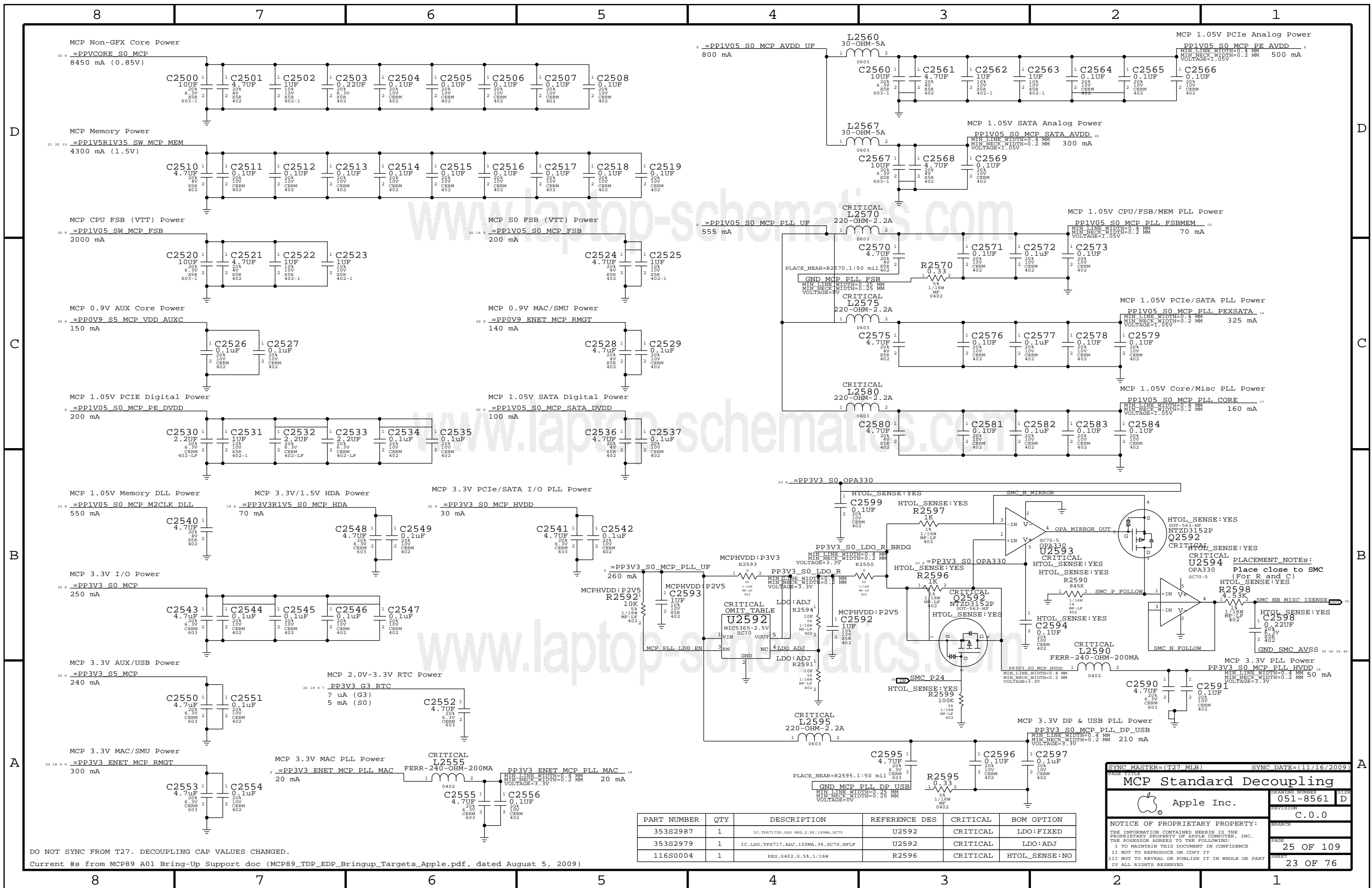
DIMM CKE Clamps



SYNC MASTER=K6 MLB		SYNC DATE=02/16/2010	
MCP89 Memory Rail Gating			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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SYNC MASTER=T27_MLB		SYNC DATE=12/15/2009	
MCP89 GFX Core Rail Gating			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		SHEET	22 OF 76



DO NOT SYNC FROM T27. DECOUPLING CAP VALUES CHANGED.

Current #s from MCP89 A01 Bring-Up Support doc (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2987	1	IC,TP971725,LDO REG,2.5V,150MA,SC70	U2592	CRITICAL	LDO:FIXED
353S2979	1	IC,LDO,TP9717,ADJ,150MA,3%,SC70,HFLF	U2592	CRITICAL	LDO:ADJ
116S0004	1	RES,0402,0.5%,1/16W	R2596	CRITICAL	HTOL_SENSE:NO

SYNC MASTER=(T27_MLB) SYNC DATE=(11/16/2009)

MCP Standard Decoupling

Apple Inc.

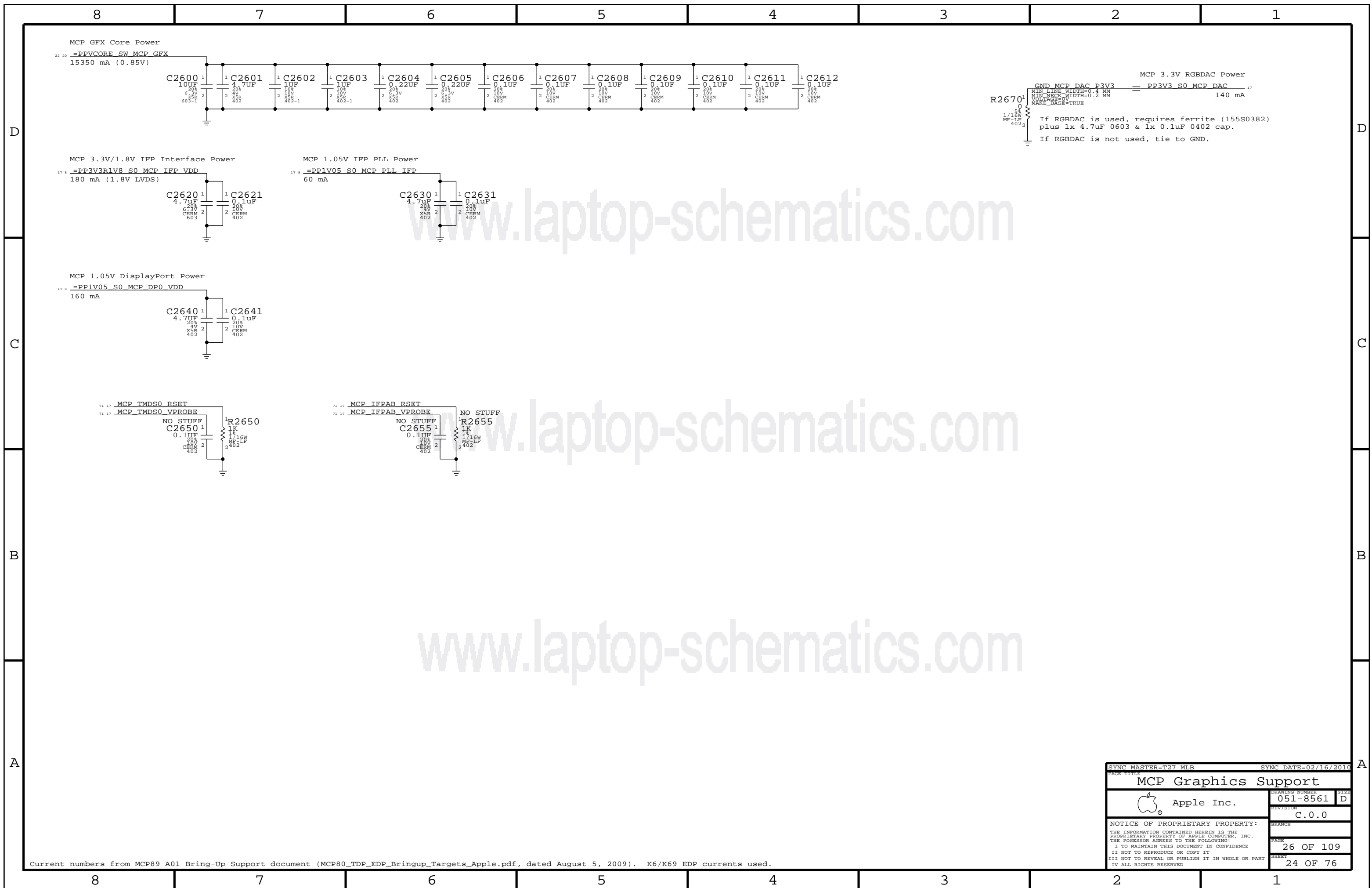
DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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SHEET: 23 OF 76



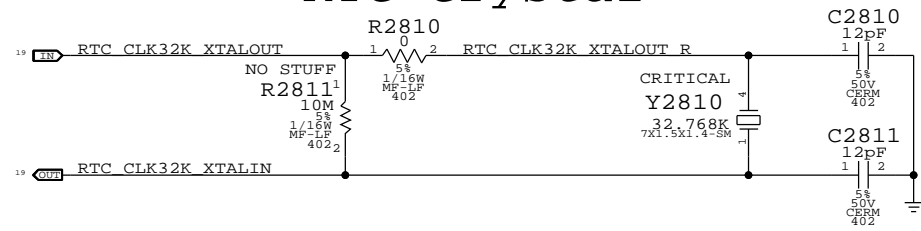
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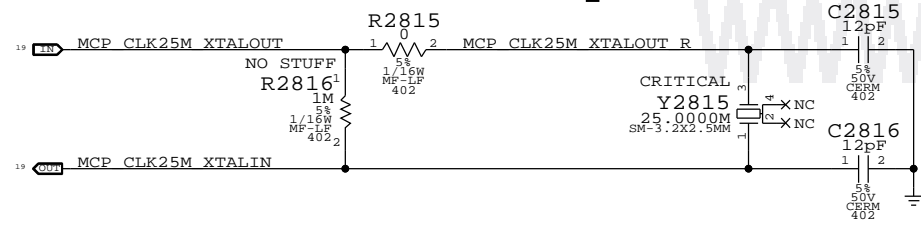
www.laptop-schematics.com

SYNC_MASTER=T27_MLB		SYNC_DATE=02/16/2010	
MCP Graphics Support			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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RTC Crystal

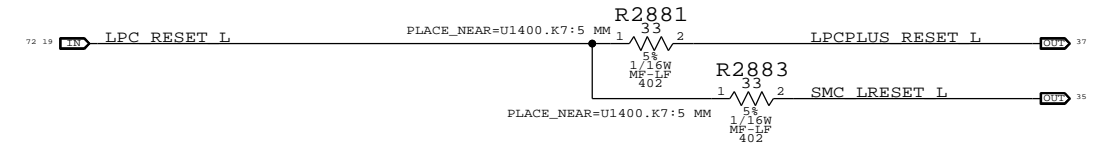


MCP 25MHz Crystal

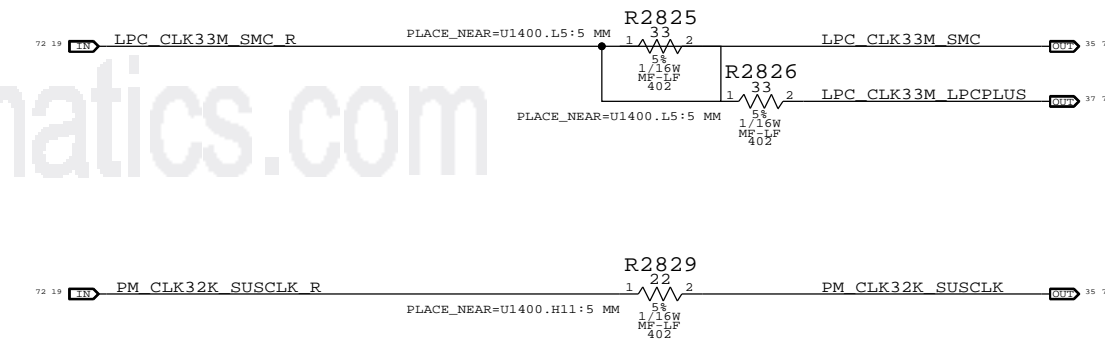
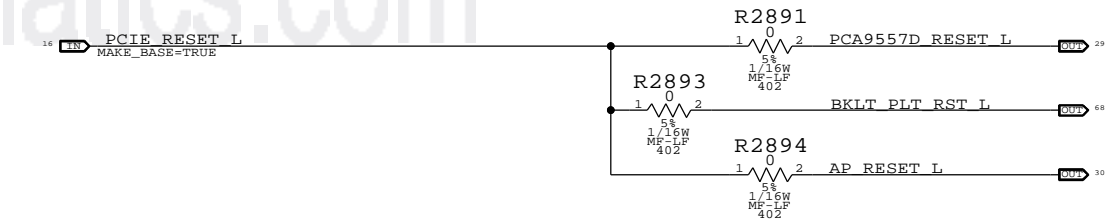


Platform Reset Connections

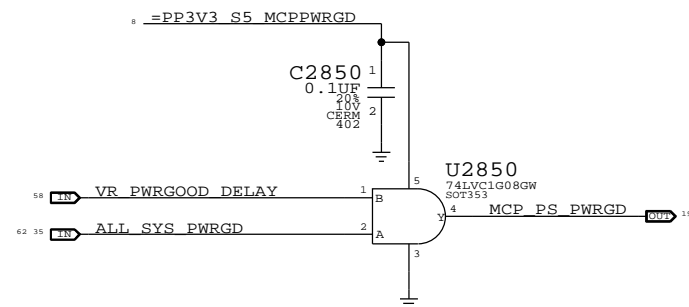
LPC Reset (Unbuffered)



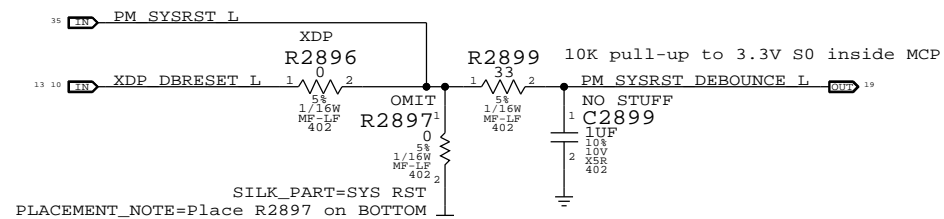
PCIE Reset (Unbuffered)



MCP S0 PWRGD & CPU_VLD



System Reset Circuit



PAGE TITLE		SYNC MASTER=(T27_MLB)		SYNC DATE=(10/07/2009)	
SB Misc					
		DRAWING NUMBER	051-8561	SIZE	D
		REVISION	C.0.0		
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		PAGE	28 OF 109		
		SHEET	25 OF 76		

DO NOT SYNC WITH T27. REMOVED PCIE RESET SIGNALS +CAESAR XTAL

Page Notes

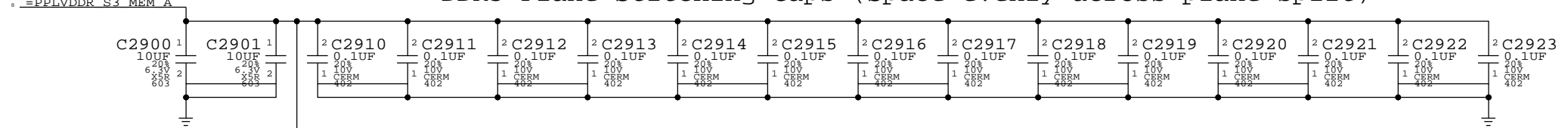
Power aliases required by this page:
- =PPLVDDR_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

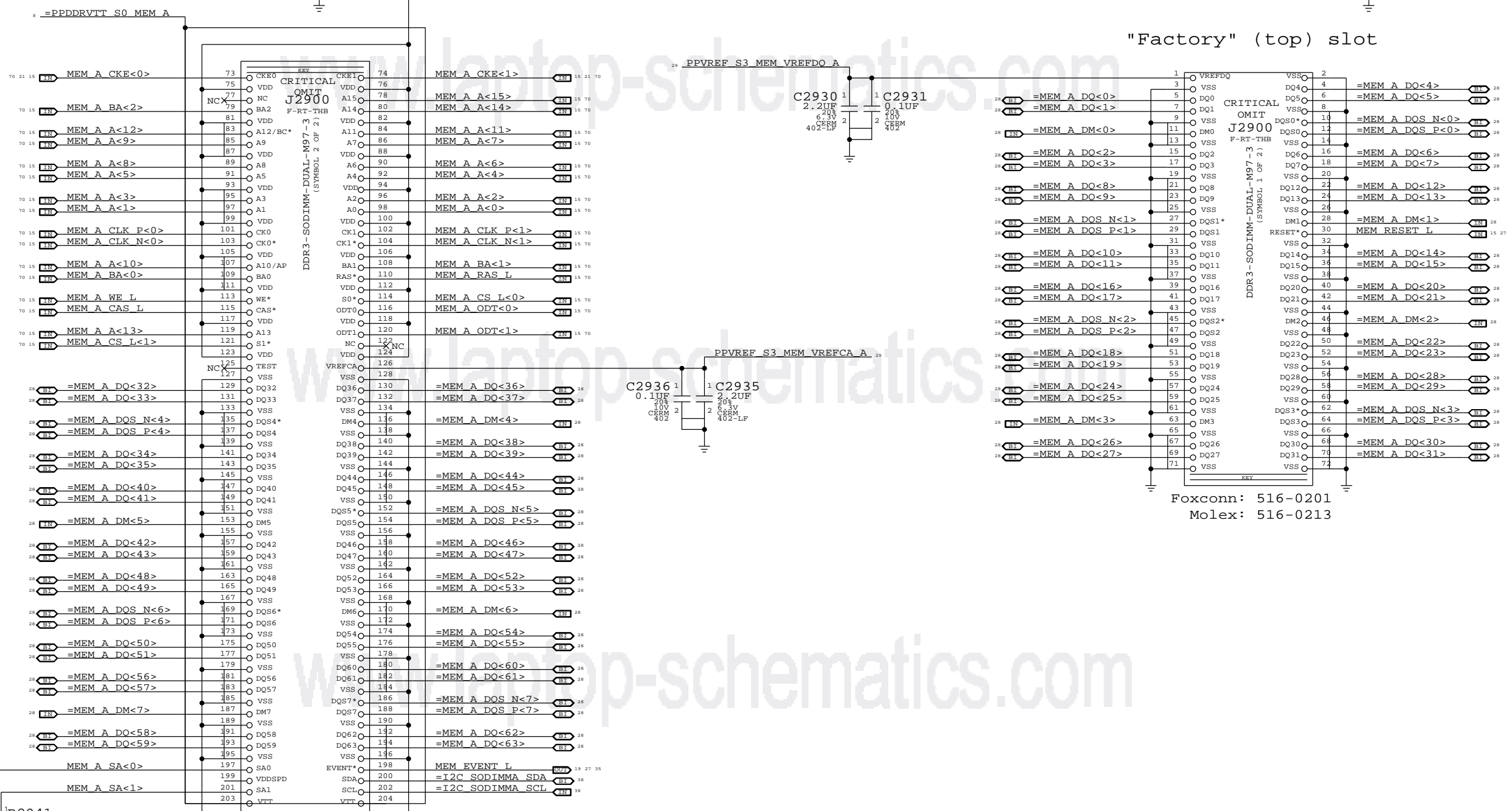
BOM options provided by this page:
(NONE)

NOTE: J3100 is OMITTED on this page.
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)



"Factory" (top) slot



Foxconn: 516-0201
Molex: 516-0213

Foxconn: 516-0201
Molex: 516-0213

SYNC MASTER=T27_MLB		SYNC DATE=02/16/2010	
DDR3 SO-DIMM Connector A			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		SHEET	26 OF 76

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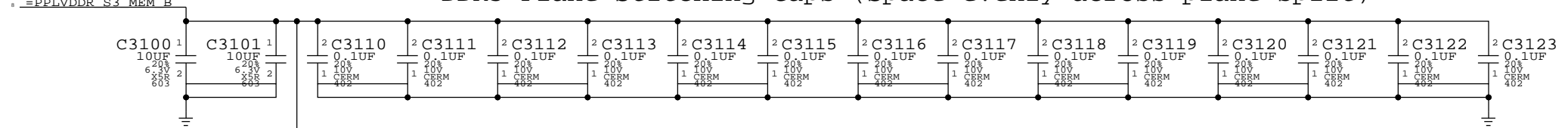
Power aliases required by this page:
- =PPLVDDR_S3_MEM_B
- =PPDDRVT S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM_SCL
- =I2C_SODIMM_SDA

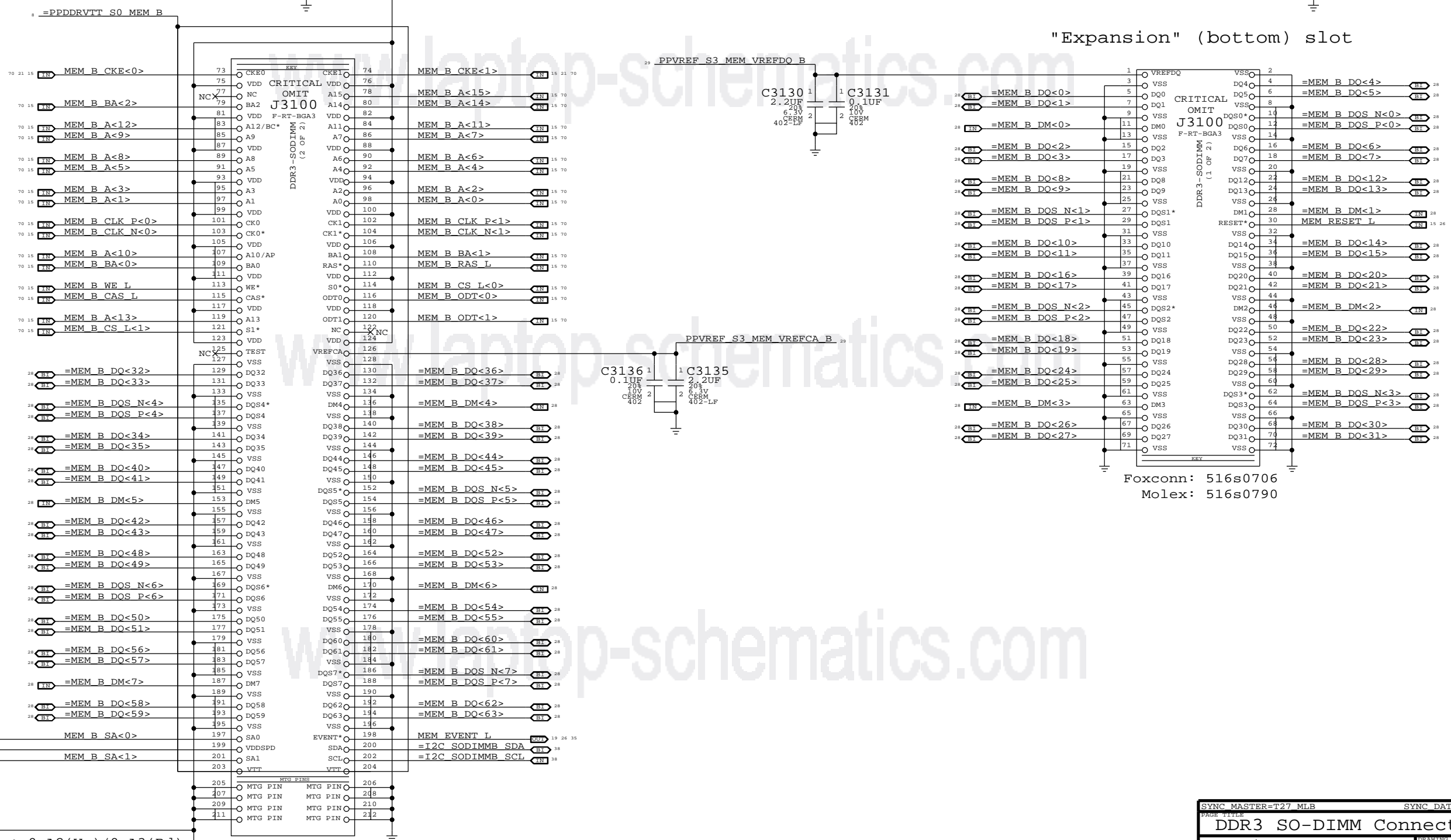
BOM options provided by this page:
(NONE)

NOTE: J3100 is OMITTED on this page.
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)



"Expansion" (bottom) slot

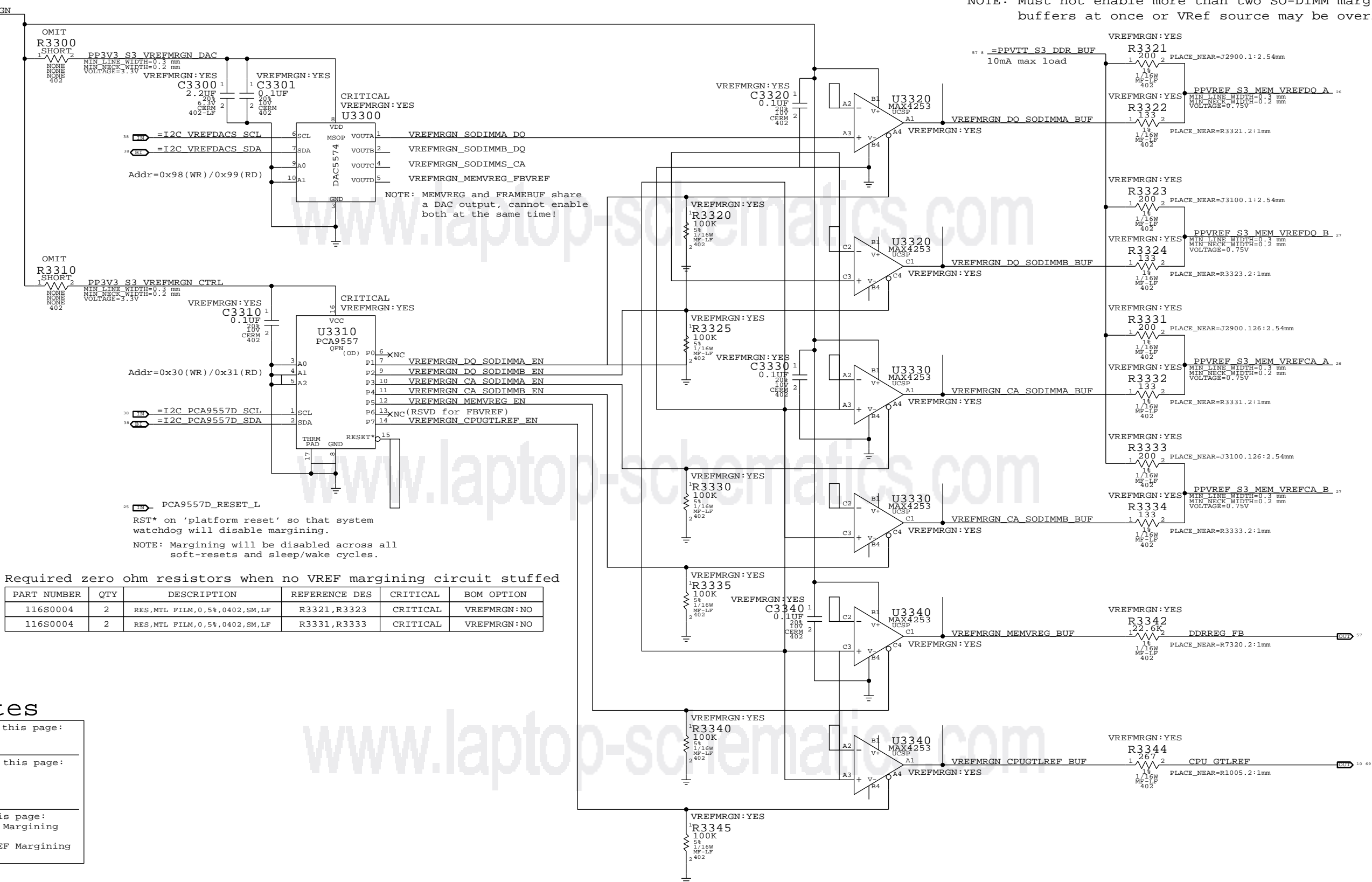


Foxconn: 516s0706
Molex: 516s0790

SPD Addr: 0xA2(Wr)/0xA3(Rd)
Foxconn: 516s0706
Molex: 516s0790

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
DDR3 SO-DIMM Connector B			
Apple Inc.		DRAWING NUMBER	051-8561
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		SHEET	27 OF 76

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES, MTL FILM, 0, 5%, 0402, SM, LF	R3321, R3323	CRITICAL	VREFMRGN: NO
116S0004	2	RES, MTL FILM, 0, 5%, 0402, SM, LF	R3331, R3333	CRITICAL	VREFMRGN: NO

Page Notes

- Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPVTT_S3_DDR_BUF
- Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA
- BOM options provided by this page:
 - VREFMRGN: YES - Stuffs VREF Margining Circuitry.
 - VREFMRGN: NO - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=T27_MLB SYNC DATE=02/16/2010

FSB/DDR3 Vref Margining

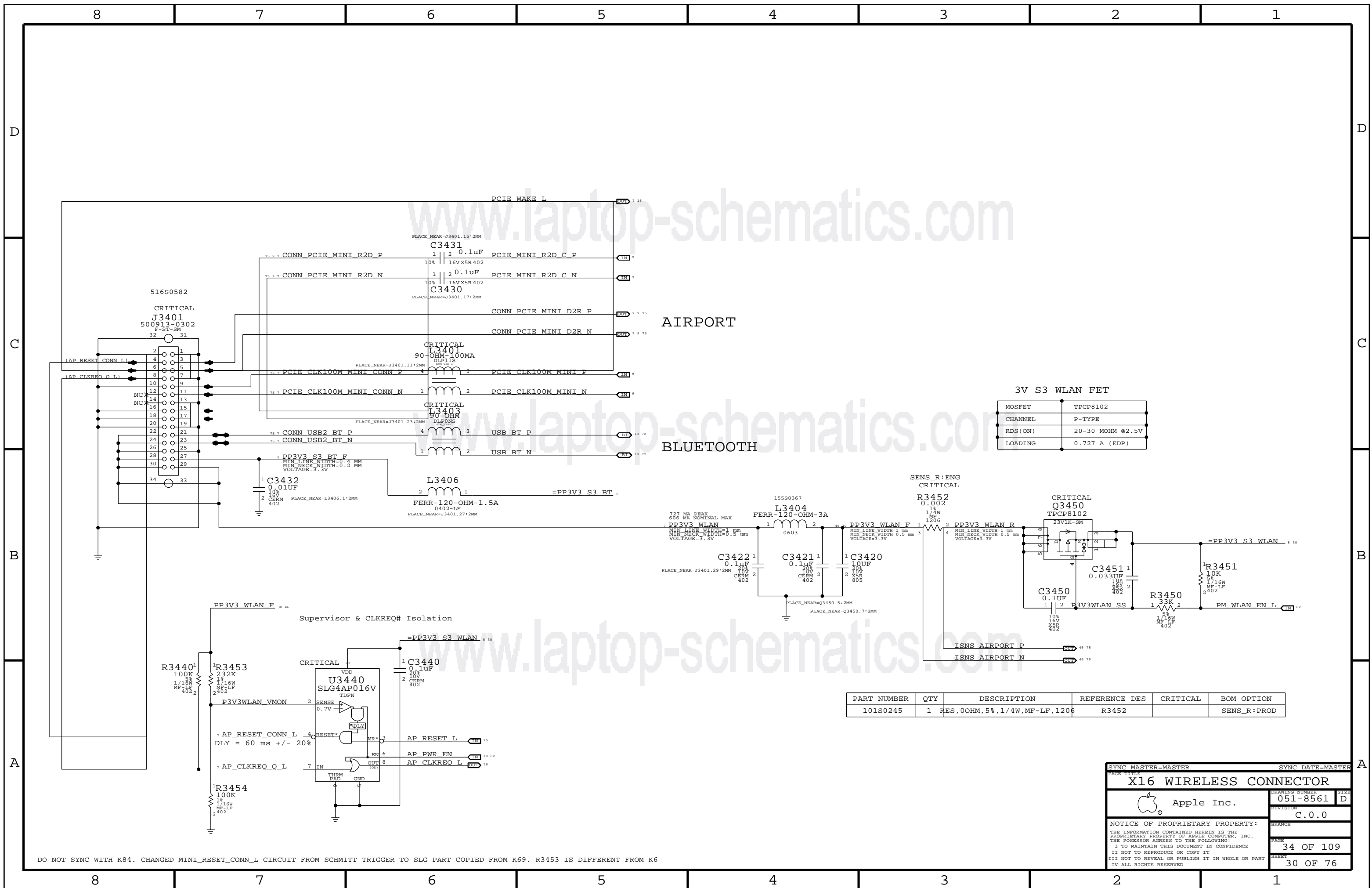
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REVISION: C.0.0

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AIRPORT

BLUETOOTH

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (EDP)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	1	RES,0OHM,5%,1/4W,MF-LF,1206	R3452		SENS_R:PROD

SYNC MASTER=MASTER SYNC DATE=MASTER

X16 WIRELESS CONNECTOR

Apple Inc.

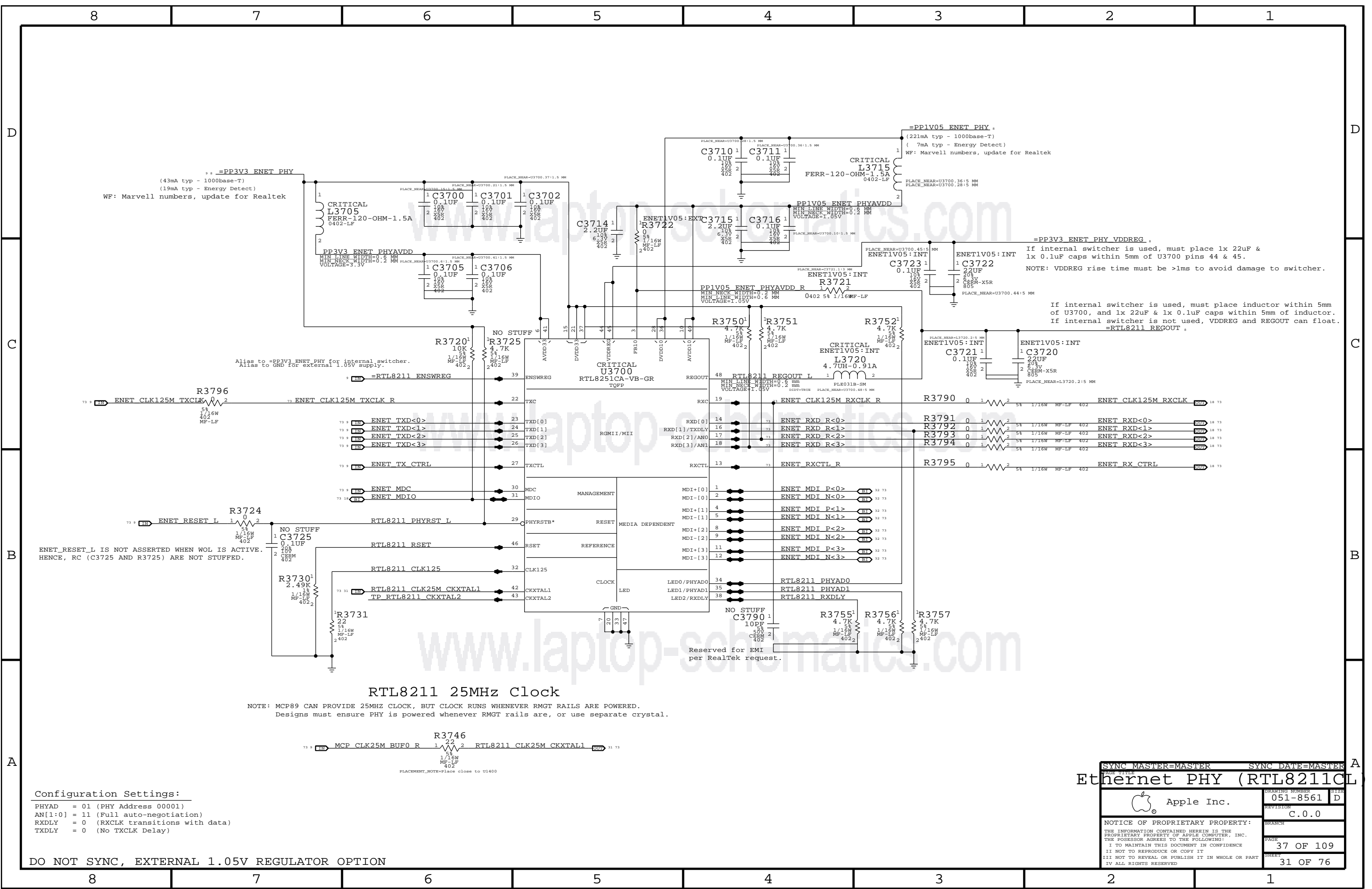
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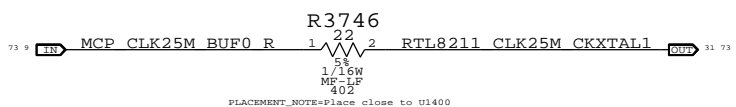
PAGE: 34 OF 109
 SHEET: 30 OF 76

DO NOT SYNC WITH K84. CHANGED MINI_RESET_CONN_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6



RTL8211 25MHz Clock

NOTE: MCP89 CAN PROVIDE 25MHZ CLOCK, BUT CLOCK RUNS WHENEVER RMGT RAILS ARE POWERED. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



- Configuration Settings:**
- PHYAD = 01 (PHY Address 00001)
 - AN[1:0] = 11 (Full auto-negotiation)
 - RXDLY = 0 (RXCLK transitions with data)
 - TXDLY = 0 (No TXCLK Delay)

DO NOT SYNC, EXTERNAL 1.05V REGULATOR OPTION

SYNC MASTER=MASTER		SYNC DATE=MASTER	
Ethernet PHY (RTL8211CL)			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8561	D
		REVISION	
		C.0.0	
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PAGE	37 OF 109		SHEET
			31 OF 76

D

D

C

C

B

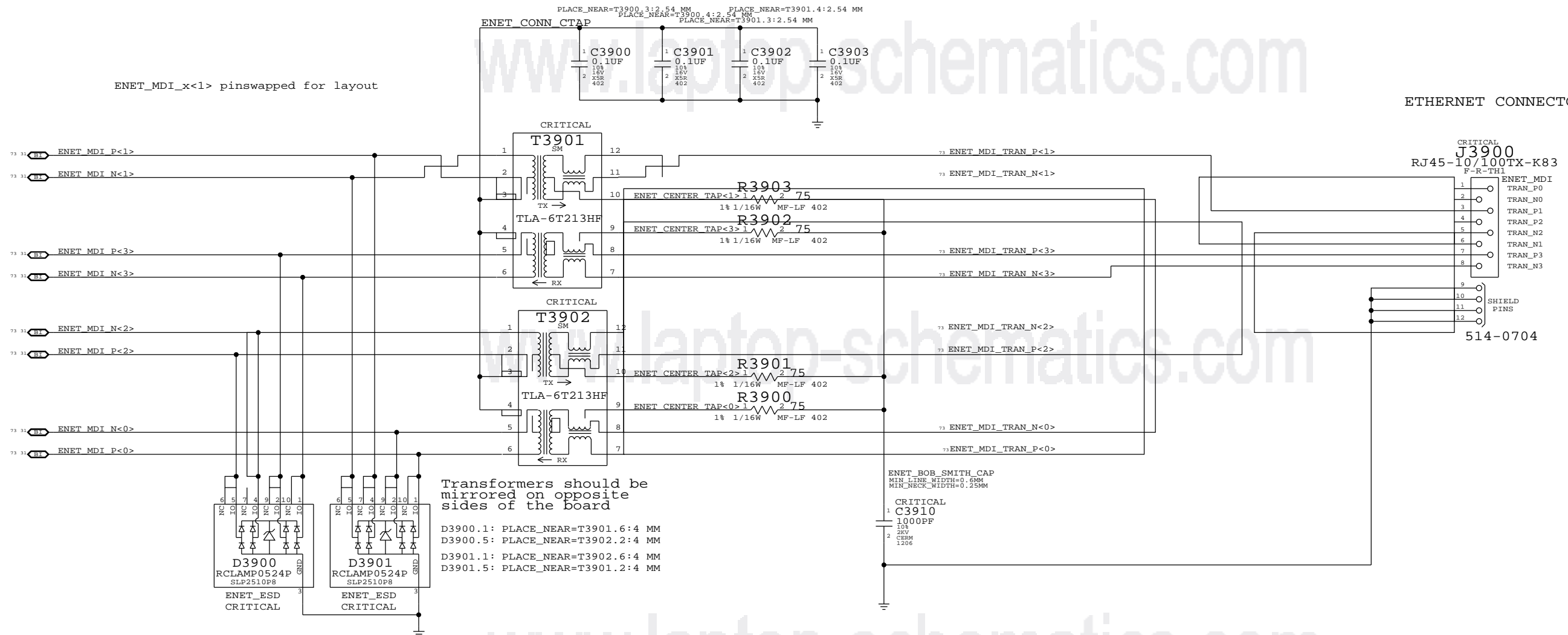
B

A

A

ENET_MDI_x<1> pinswapped for layout

ETHERNET CONNECTOR



Transformers should be mirrored on opposite sides of the board

- D3900.1: PLACE_NEAR=T3901.6:4 MM
- D3900.5: PLACE_NEAR=T3902.2:4 MM
- D3901.1: PLACE_NEAR=T3902.6:4 MM
- D3901.5: PLACE_NEAR=T3901.2:4 MM

ENET_BOB_SMITH_CAP
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.25MM

CRITICAL
 C3910
 1000PF
 10V
 0603
 1206

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www.laptop-schematics.com

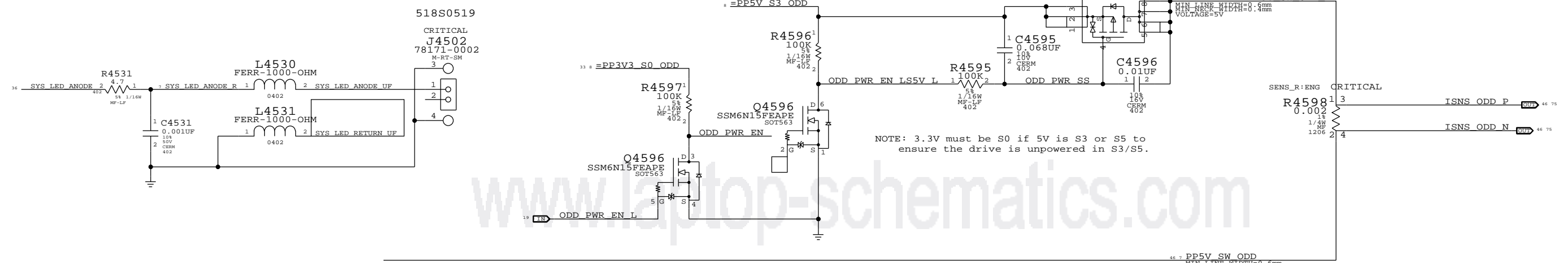
www.laptop-schematics.com

DO NOT SYNC FROM K6, WITH K84'S CONNECTOR

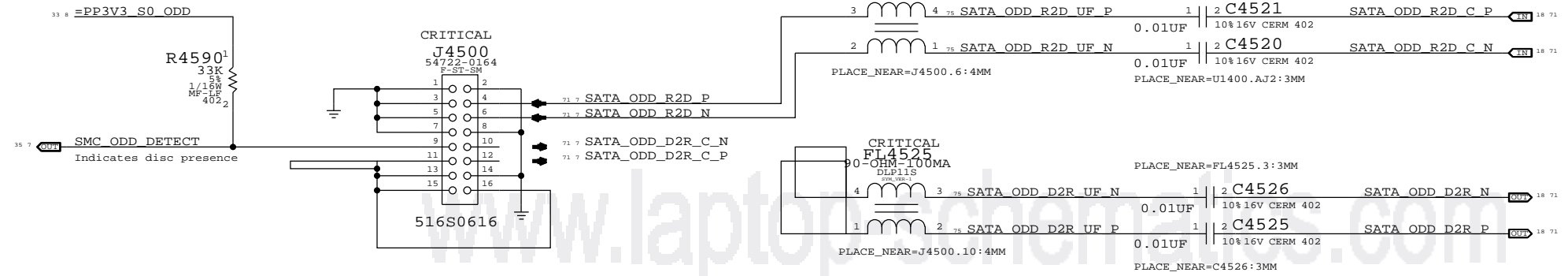
SYNC MASTER=MASTER		SYNC DATE=MASTER	
ETHERNET CONNECTOR			
Apple Inc.		DRAWING NUMBER	051-8561
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		PAGE	39 OF 109
		SHEET	32 OF 76

SIL

ODD Power Control



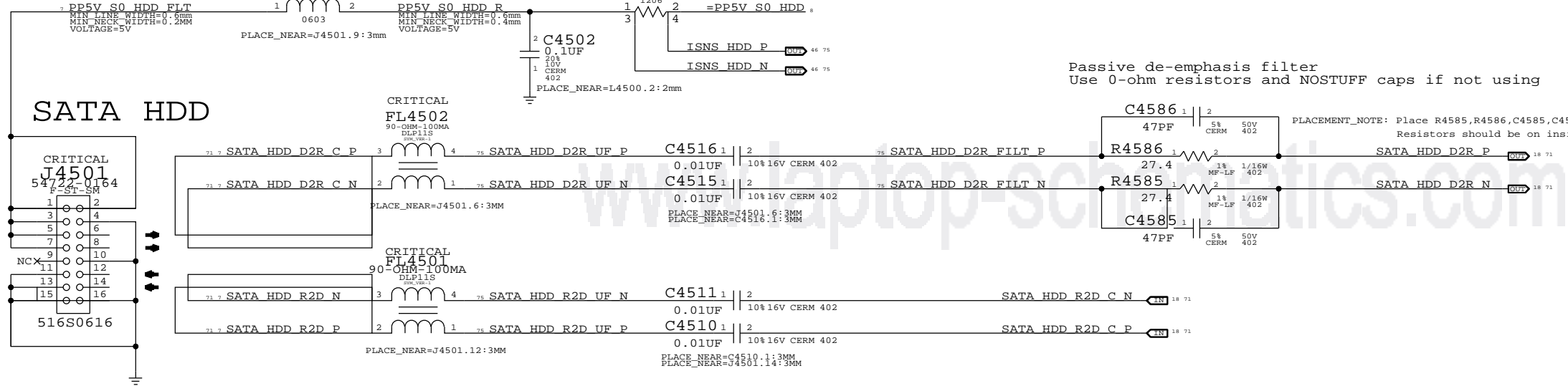
SATA ODD



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	2	RES, 0OHM, 5%, 1/4W, MF-LP, 1206	R4599, R4598		SENS_R: PROD

Passive de-emphasis filter
Use 0-ohm resistors and NOSTUFF caps if not using

SATA HDD



SYNC MASTER=MASTER SYNC DATE=MASTER

SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

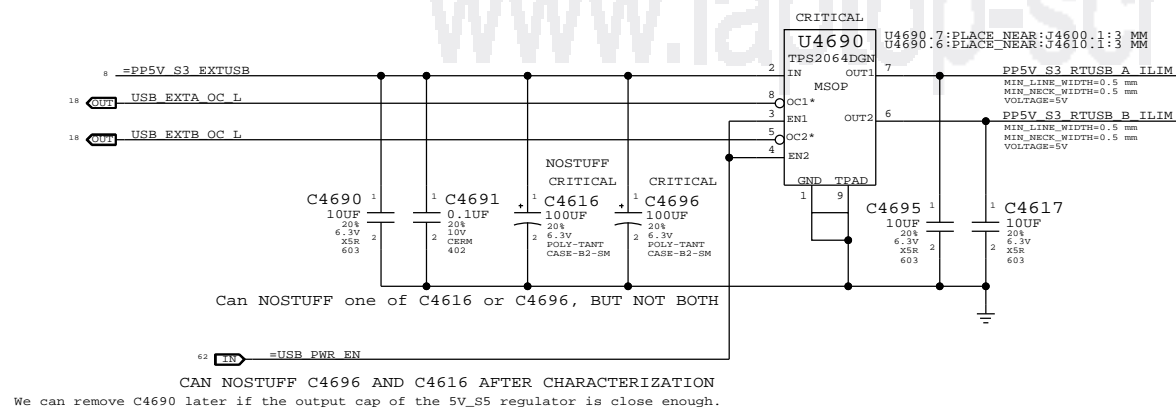
REVISION: C.0.0

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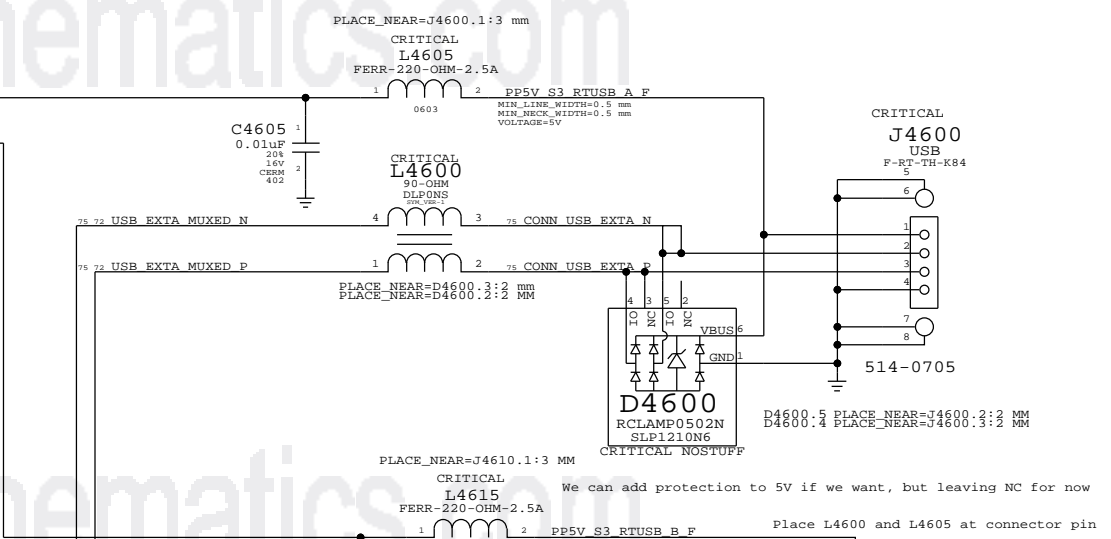
PAGE: 45 OF 109
SHEET: 33 OF 76

POR IS METAL USB CONNECTOR PARTS

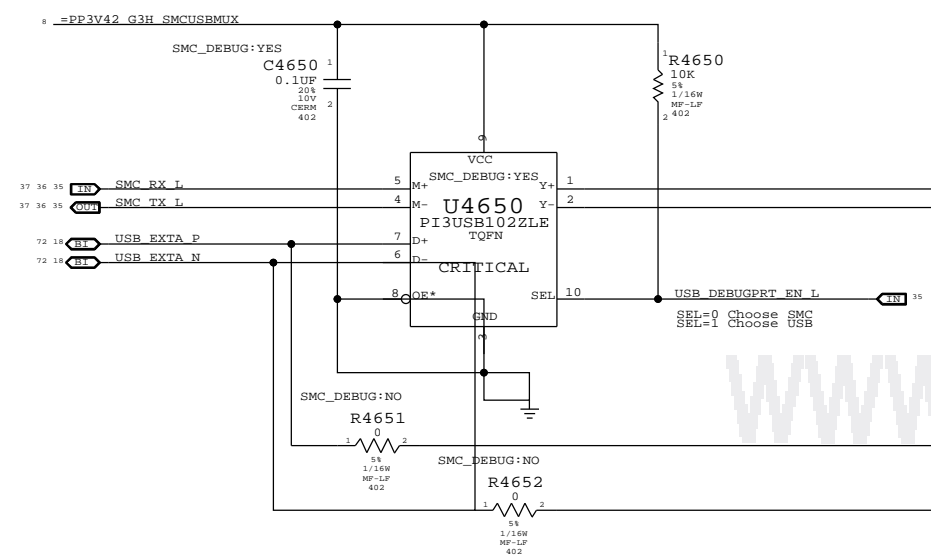
Port Power Switch



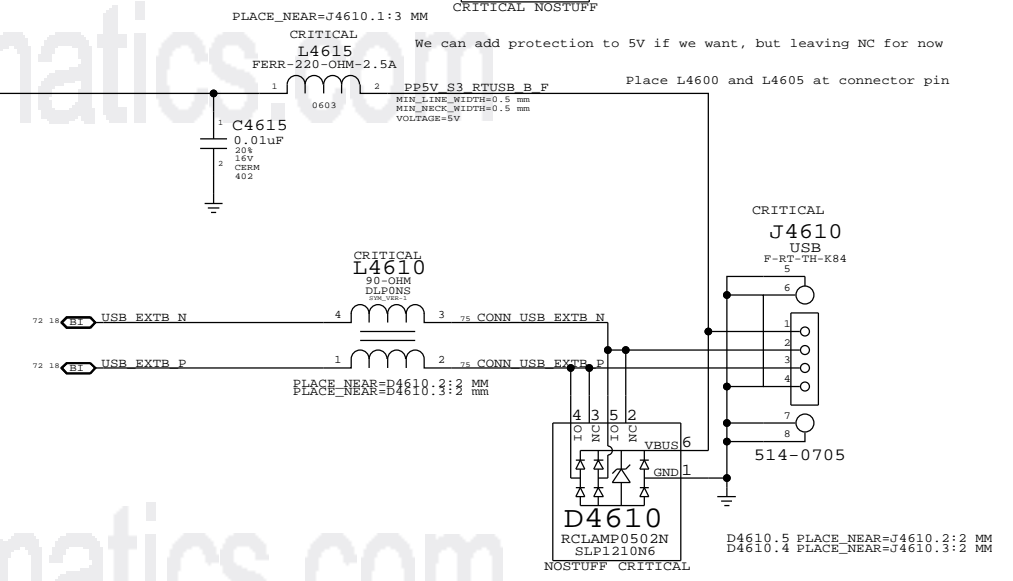
USB PORT A (FRONT PORT)



USB/SMC Debug Mux



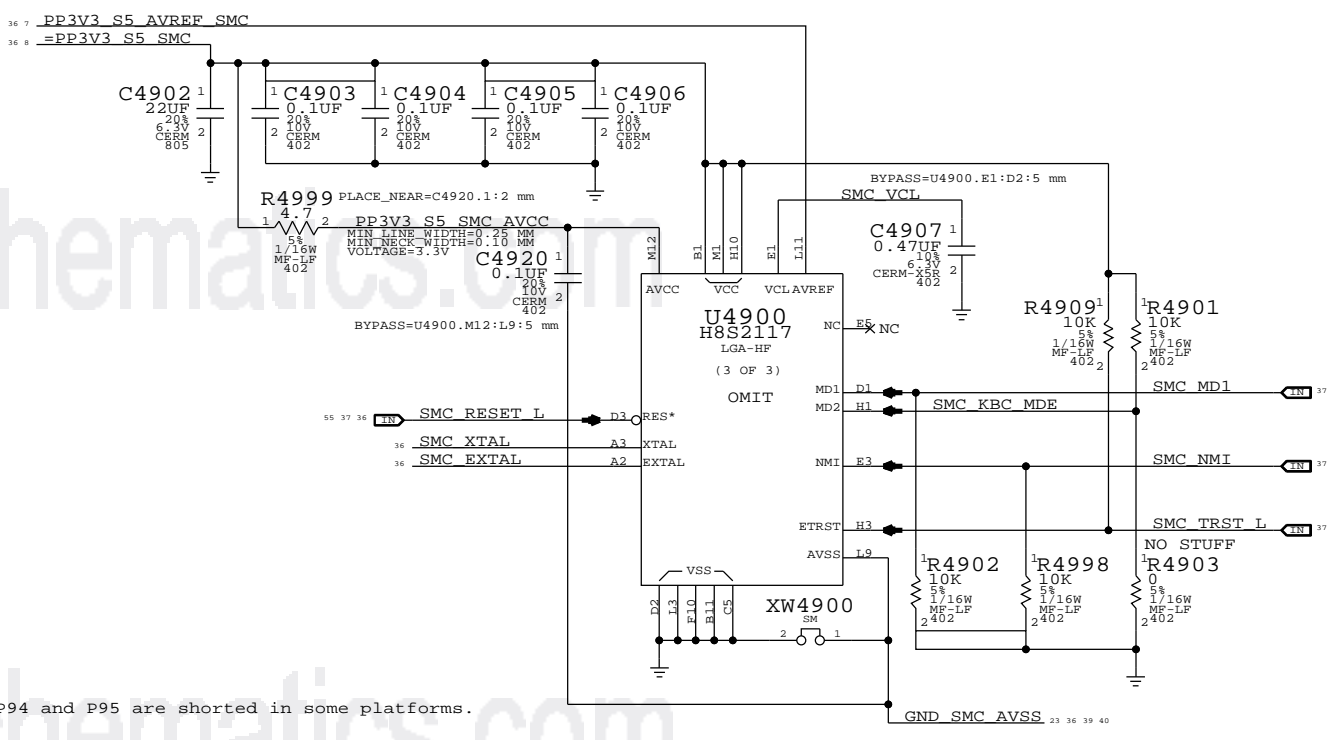
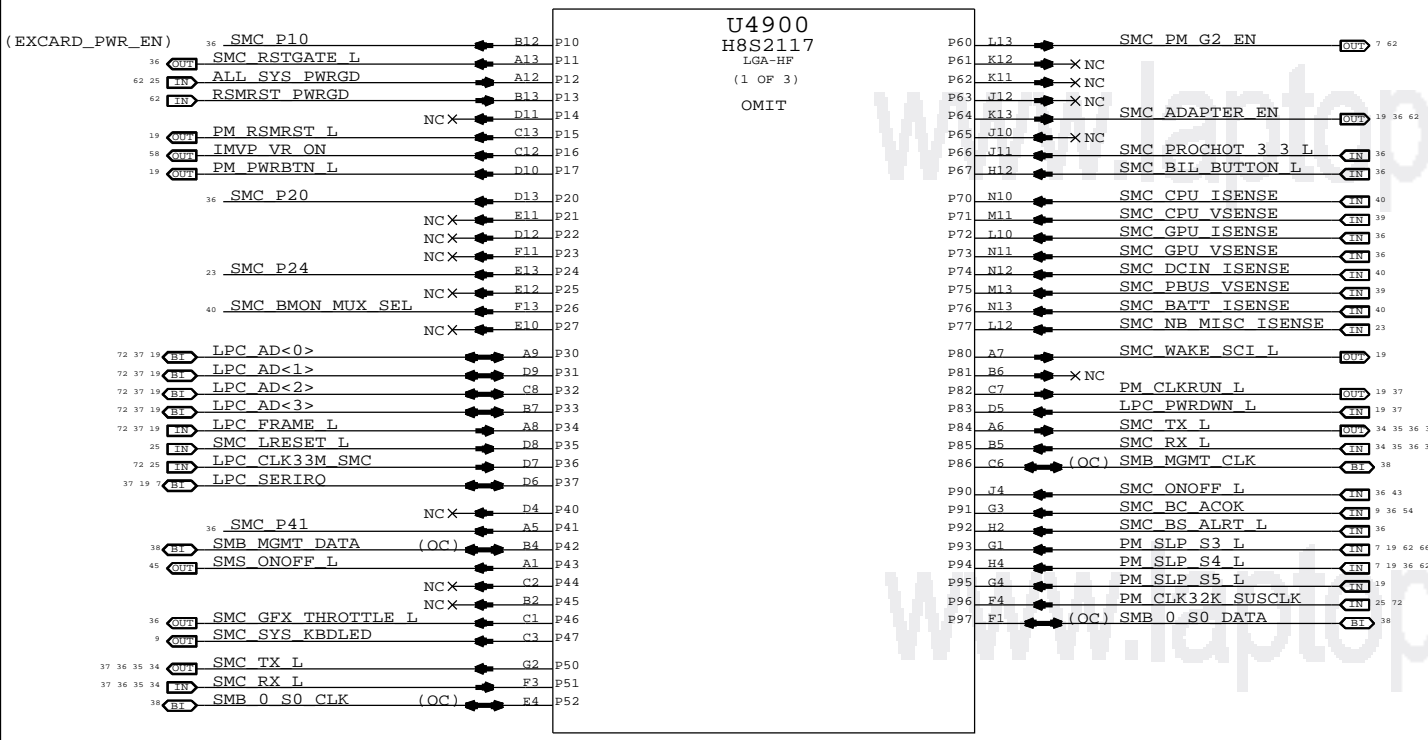
USB PORT B (BACK PORT)



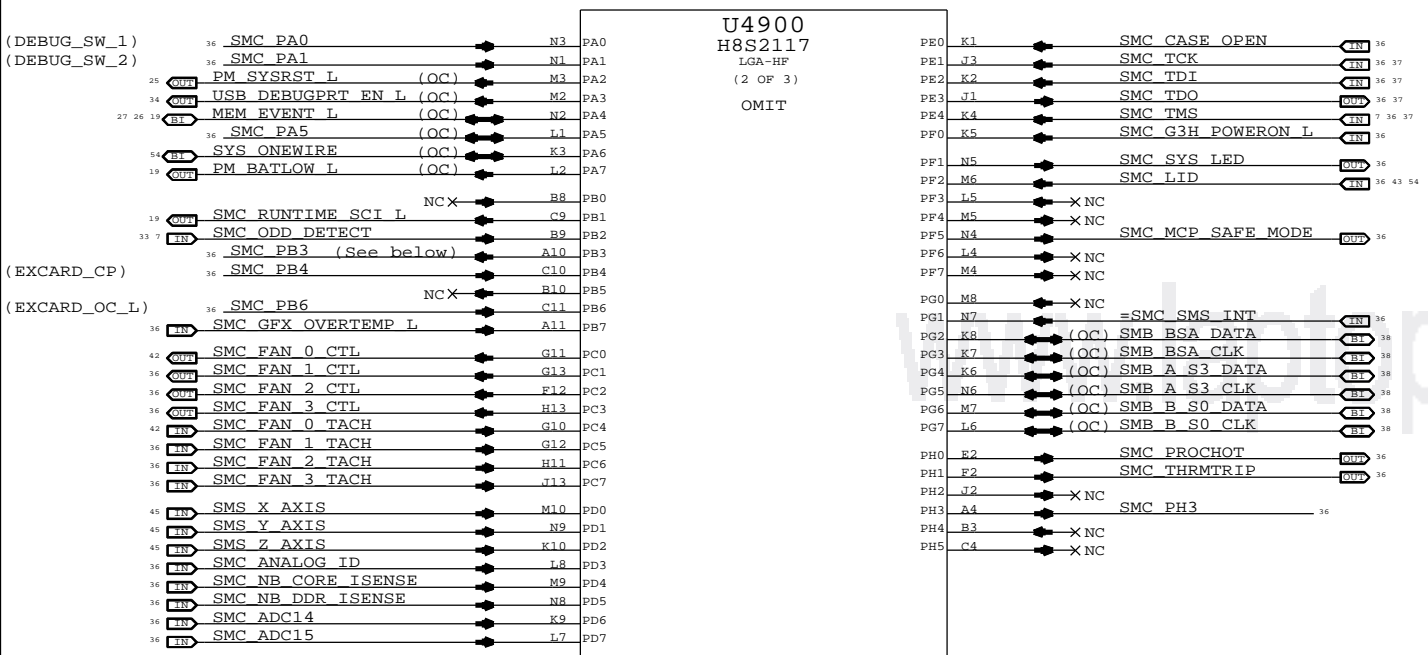
DO NOT SYNC WITH K84. UPDATED PLACE NEAR NOTES
UPDATED SMC_DEBUG BOMOPTION, STUFFED C4690

SYNC MASTER=(K84_MLB)		SYNC DATE=(10/03/2009)	
External USB Connectors			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted in some platforms.



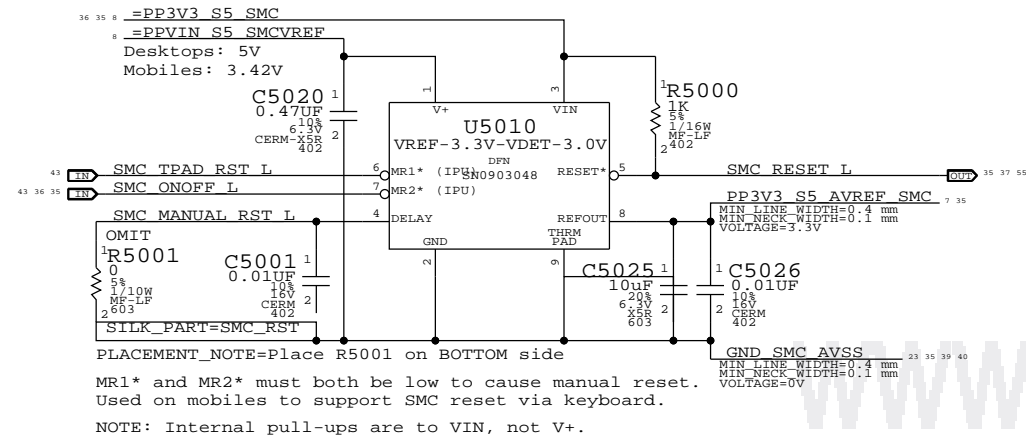
NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

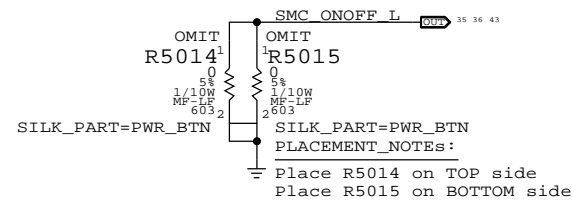
SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay.

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8561	D
		REVISION	
		C.0.0	
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		PAGE	
		49 OF 109	
		SHEET	
		35 OF 76	

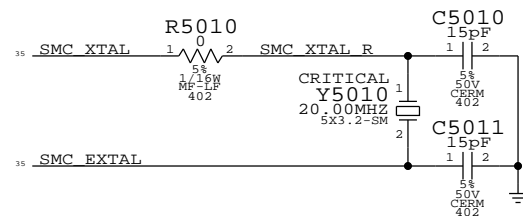
SMC Reset "Button", Supervisor & AVREF Supply



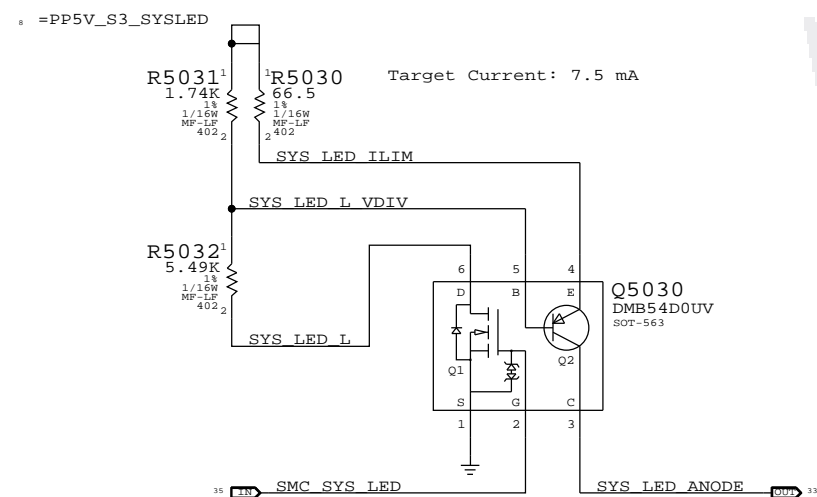
Debug Power "Buttons"



SMC Crystal Circuit

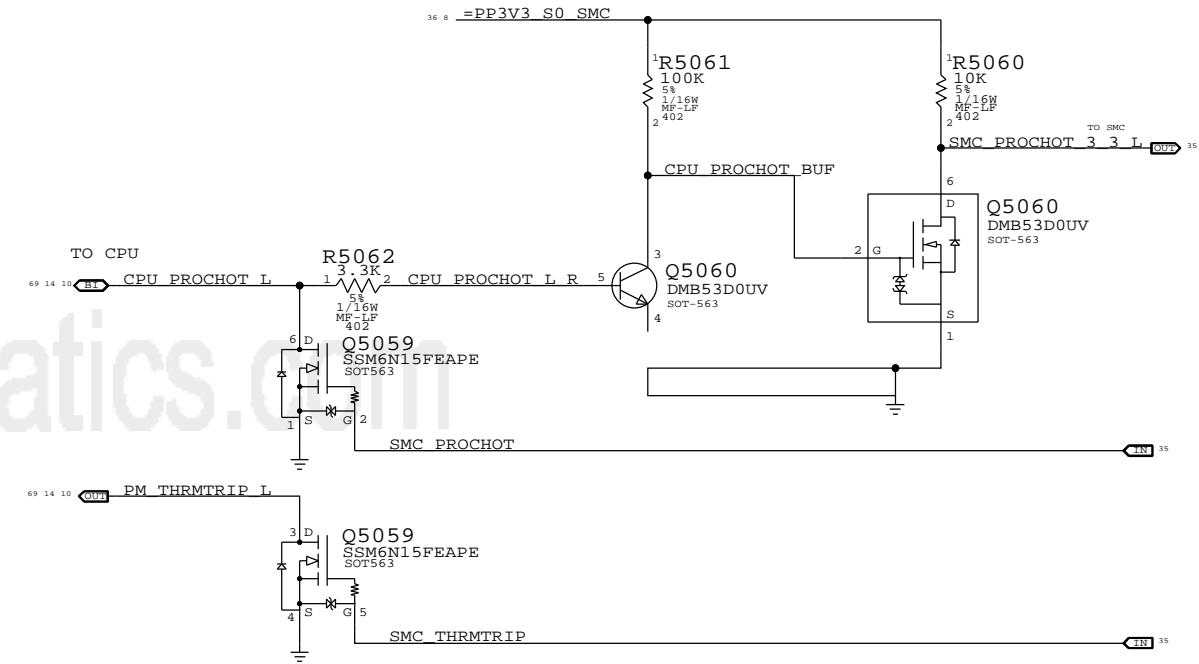


System (Sleep) LED Circuit

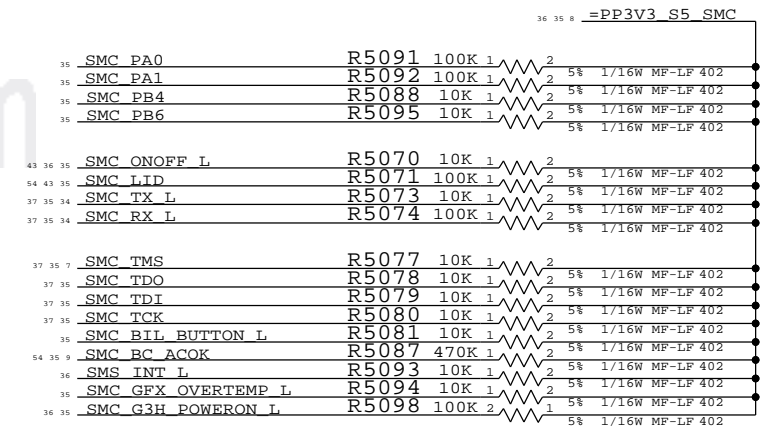


R5030,R5031,R5032 CHANGED FOR DIMMER LED

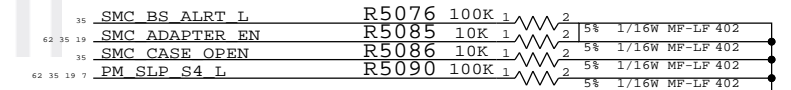
SMC FSB to 3.3V Level Shifting



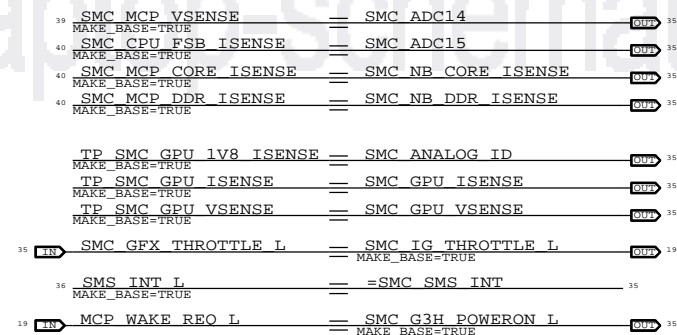
SMC Pull-ups



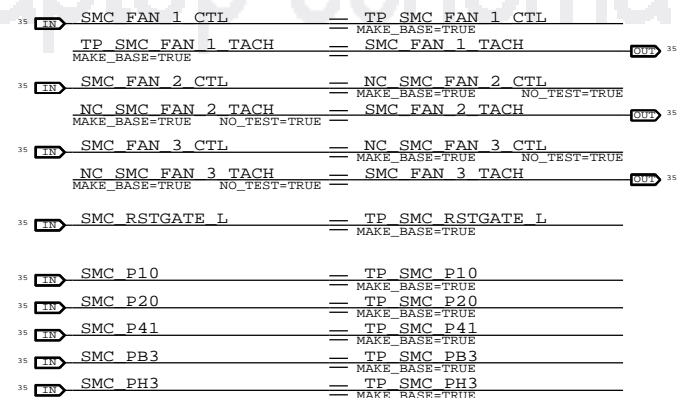
SMC Pull-downs



SMC Aliases



Unused Pins



SYNC MASTER=(T27_MLB) SYNC DATE=(10/27/2009)

SMC Support

Apple Inc.

DRAWING NUMBER: 051-8561

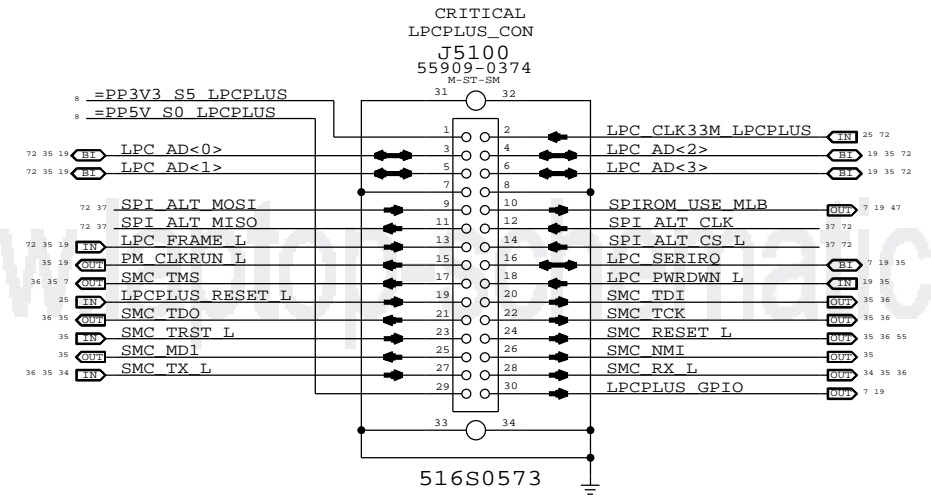
REVISION: C.0.0

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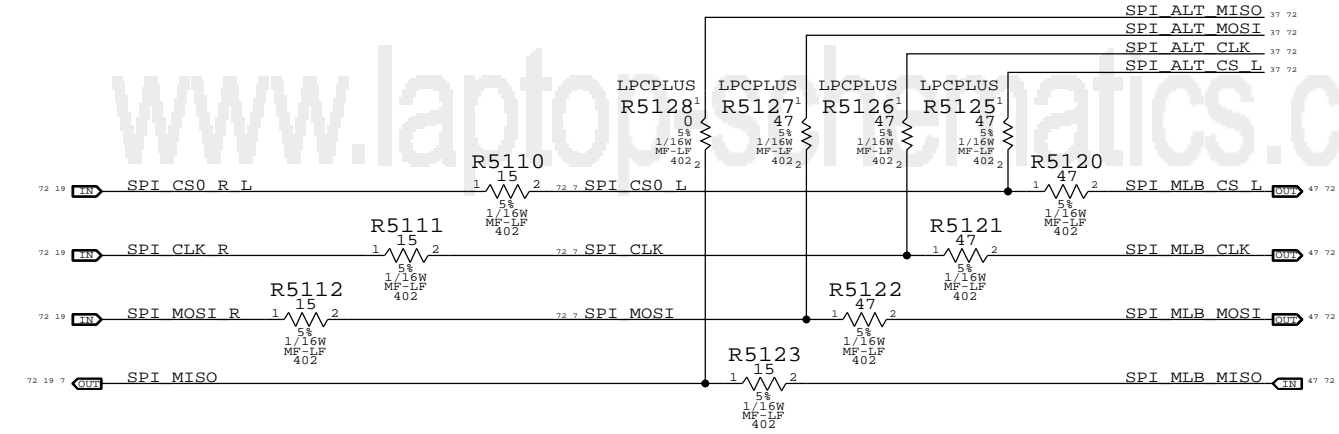
PAGE: 50 OF 109

SHEET: 36 OF 76

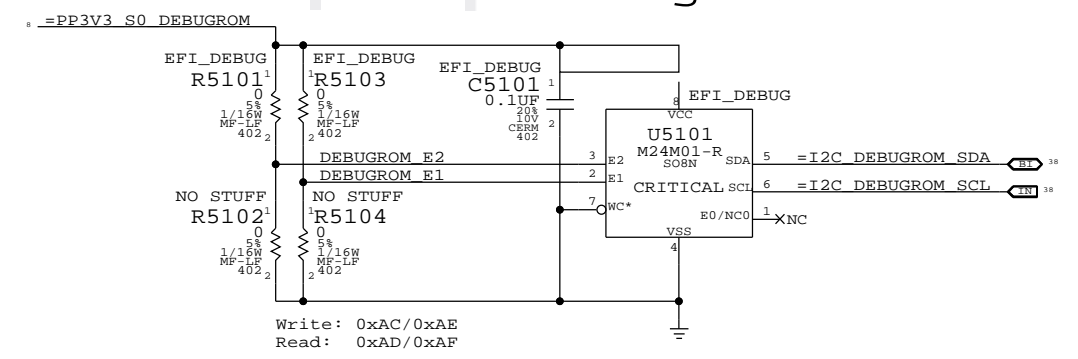
LPC+SPI Connector



SPI Bus Series Termination

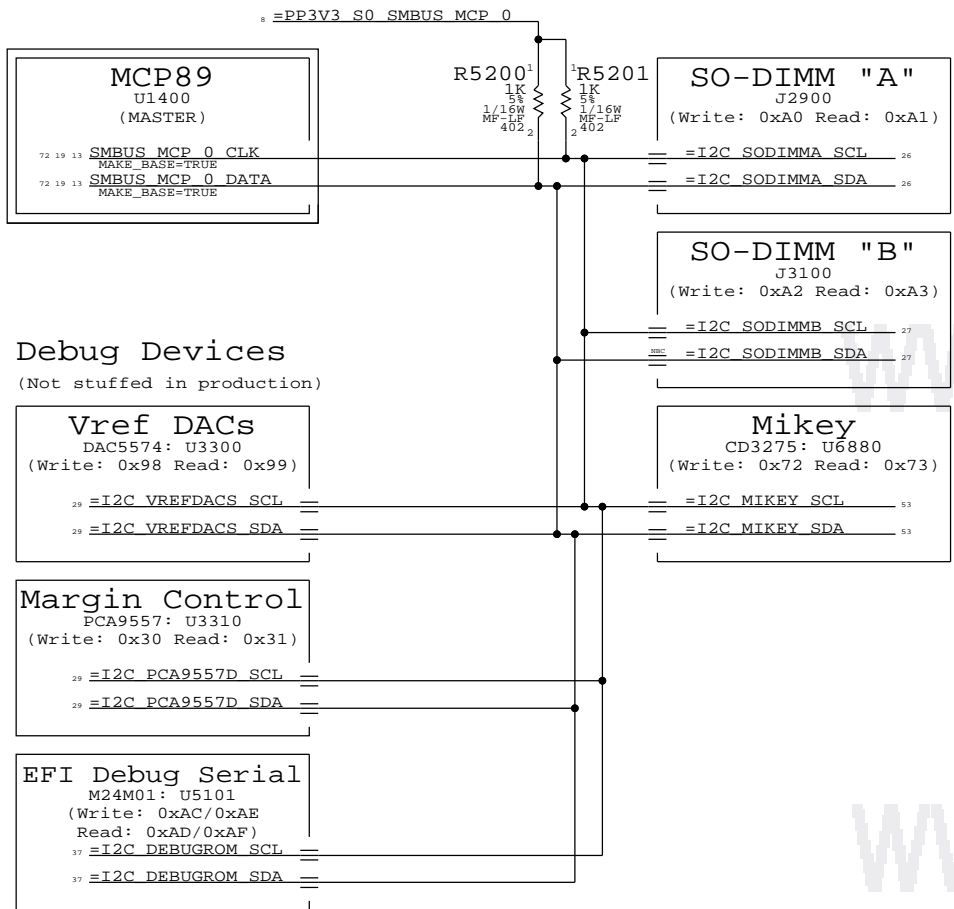


EFI Debug ROM

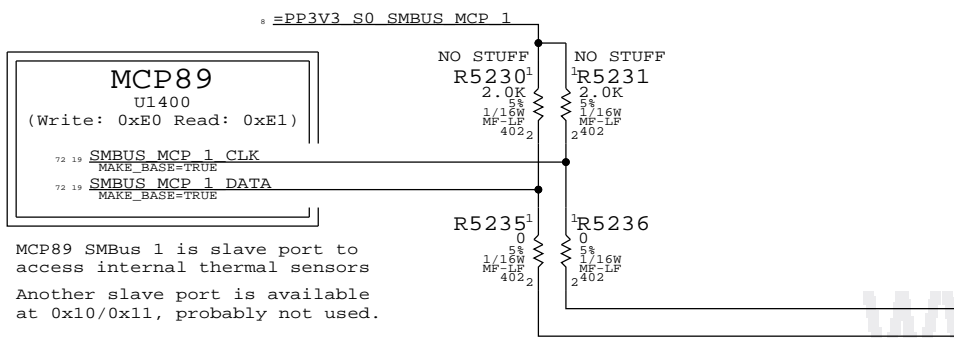


PAGE TITLE		SYNC DATE=(12/15/2009)	
LPC+SPI Debug Connector			
Apple Inc.	DRAWING NUMBER	051-8561	SIZE
	REVISION	C.0.0	
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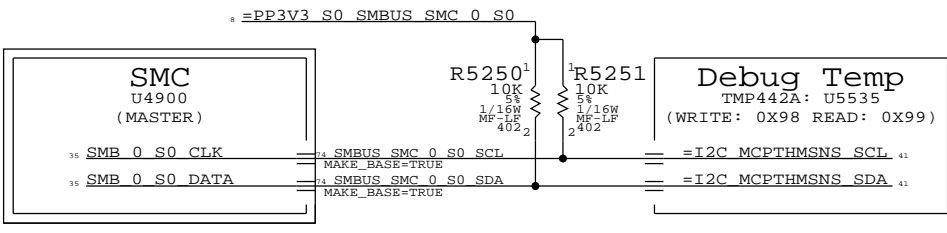
MCP89 SMBus "0" Connections



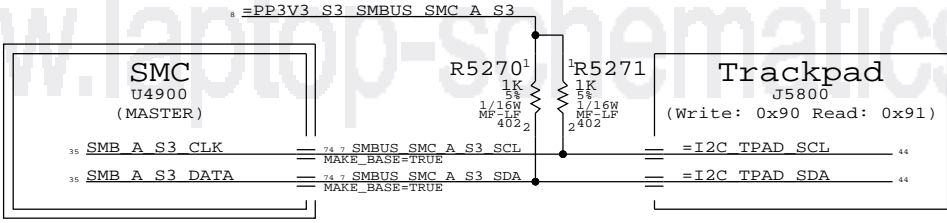
MCP89 SMBus "1" Connections



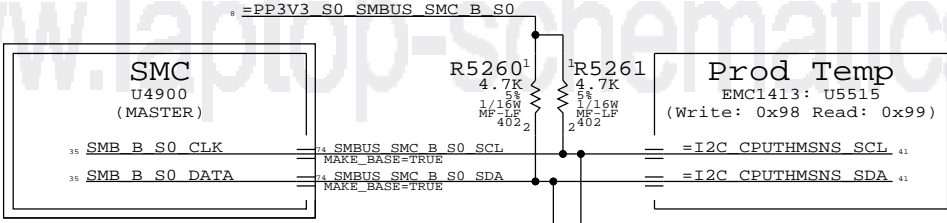
SMC "0" SMBus Connections



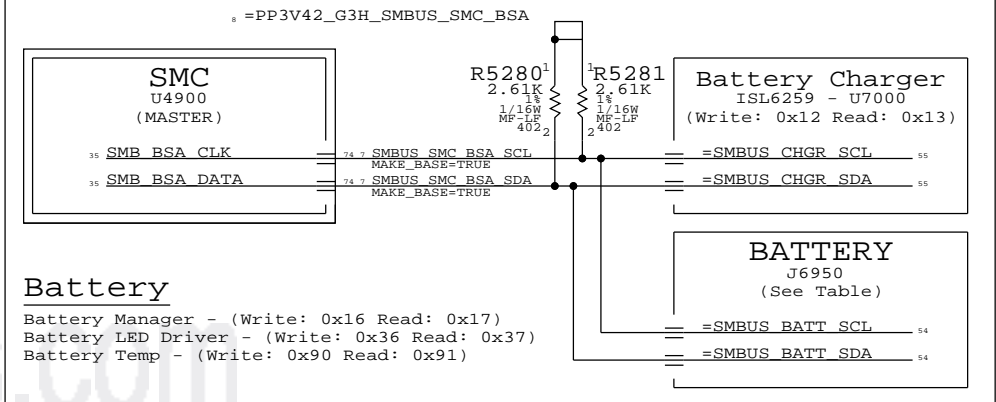
SMC "A" SMBus Connections



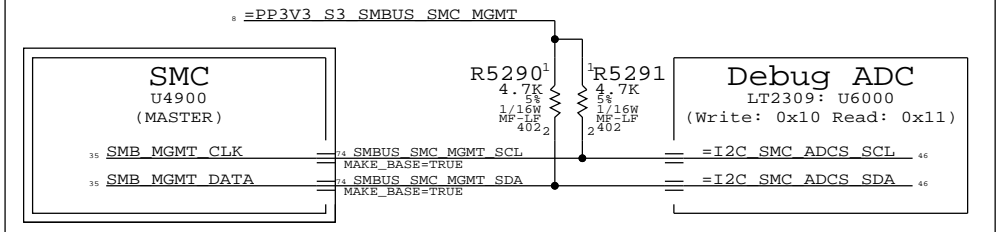
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections

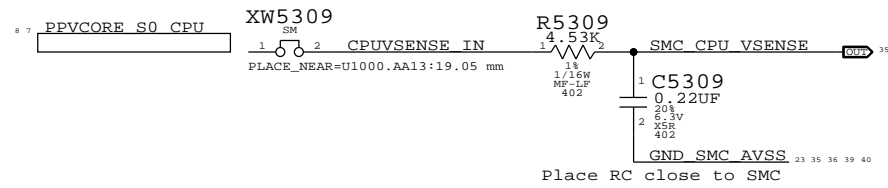


SMC "Management" SMBus Connections

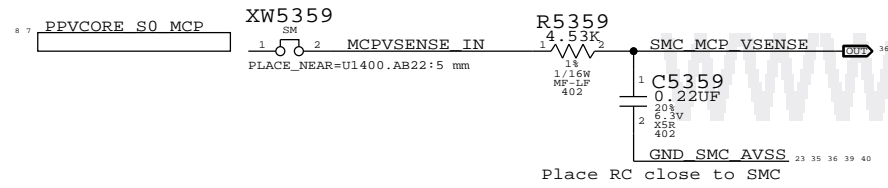


SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE K87 SMBus Connections			
Apple Inc.		DRAWING NUMBER 051-8561	SIZE D
		REVISION C.0.0	BRANCH
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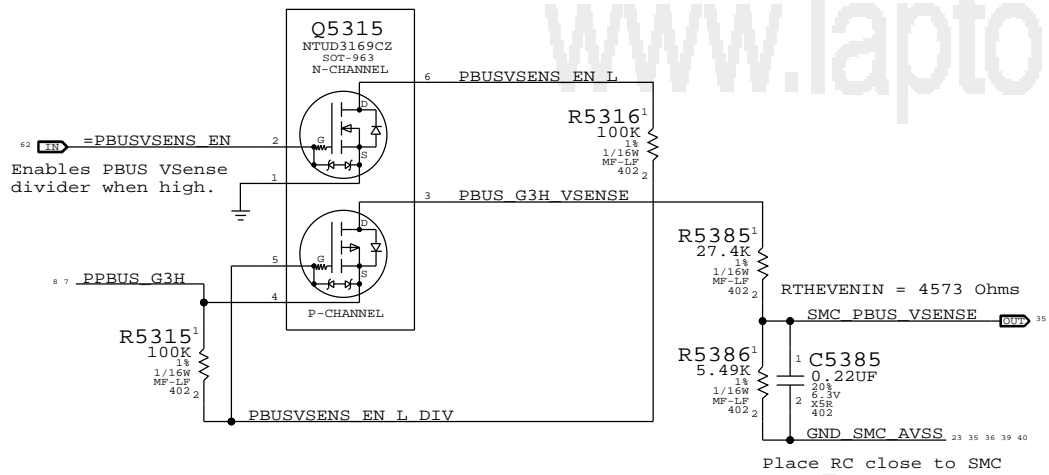
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS Voltage Sense Enable & Filter



SYNC MASTER=T27_MLB		SYNC DATE=02/16/2010	
Voltage Sensing			
DRAWING NUMBER		SIZE	
051-8561		D	
REVISION		PAGE	
C.0.0		53 OF 109	
BRANCH		SHEET	
		39 OF 76	
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D

C

B

A

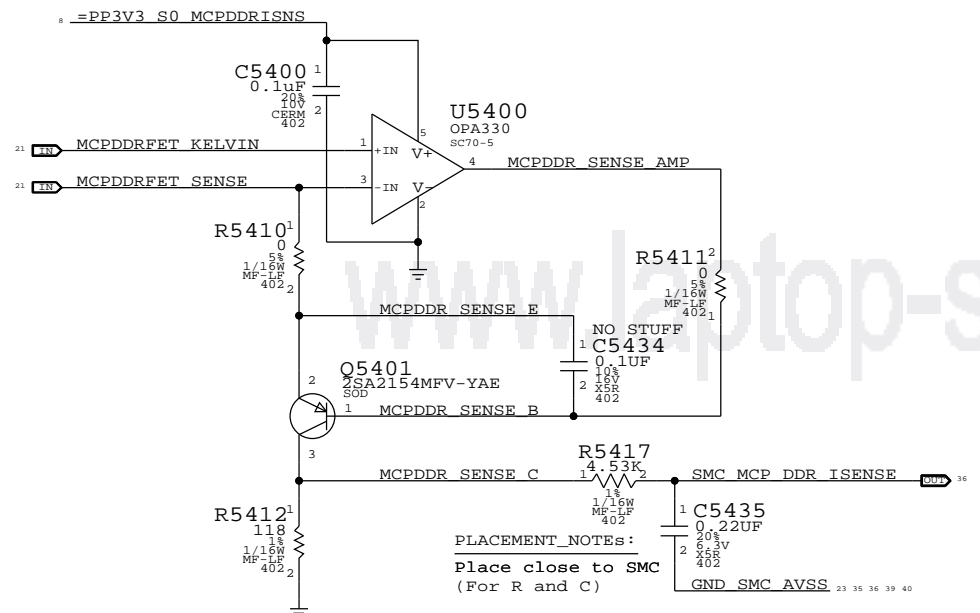
D

C

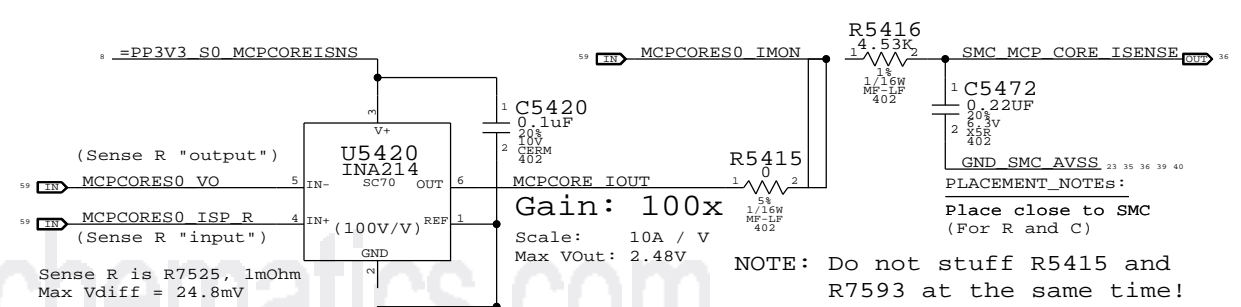
B

A

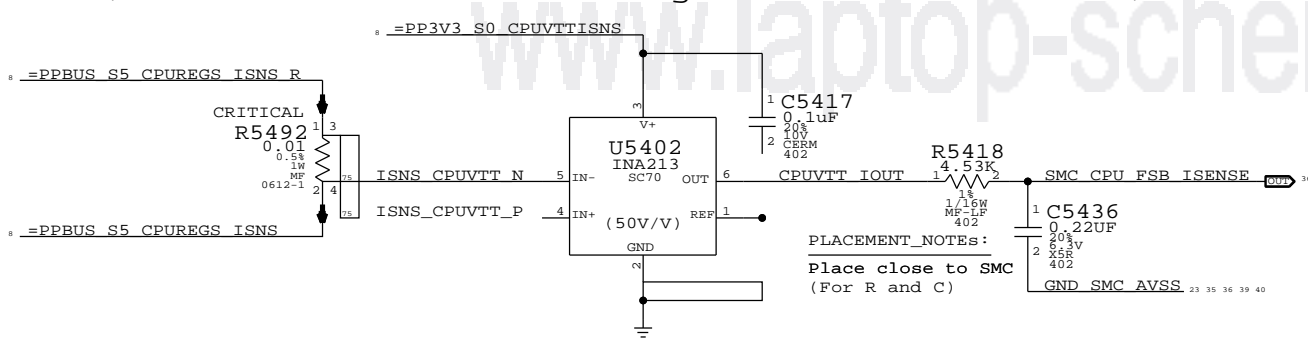
MCP MEM VDD Current Sense / Filter



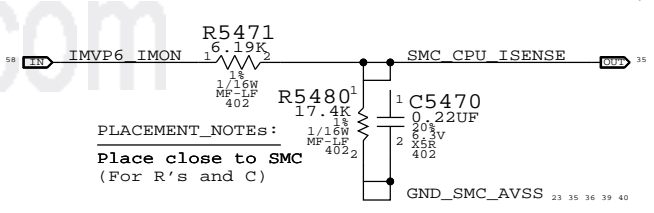
MCP VCore Current Sense Filter



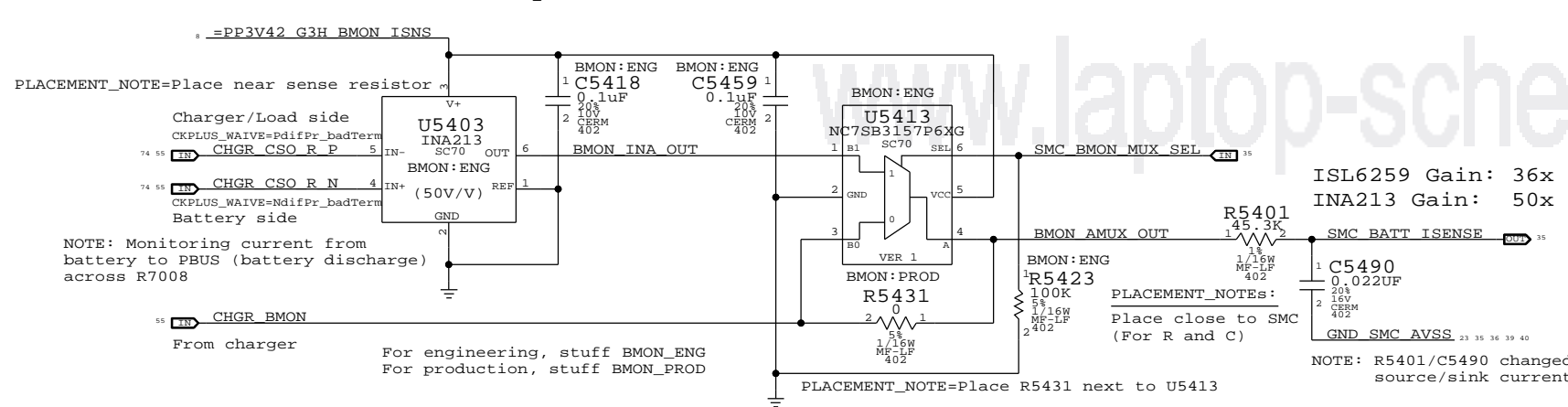
MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



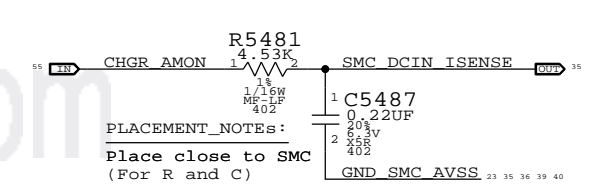
CPU VCore Load Side Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter

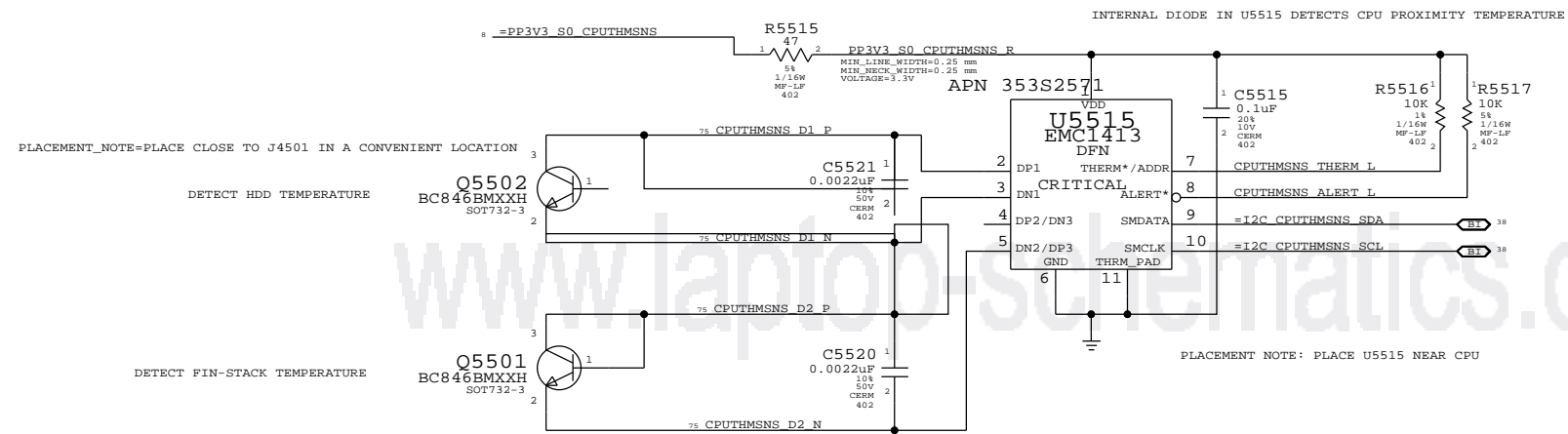


DC-IN (AMON) Current Sense Filter

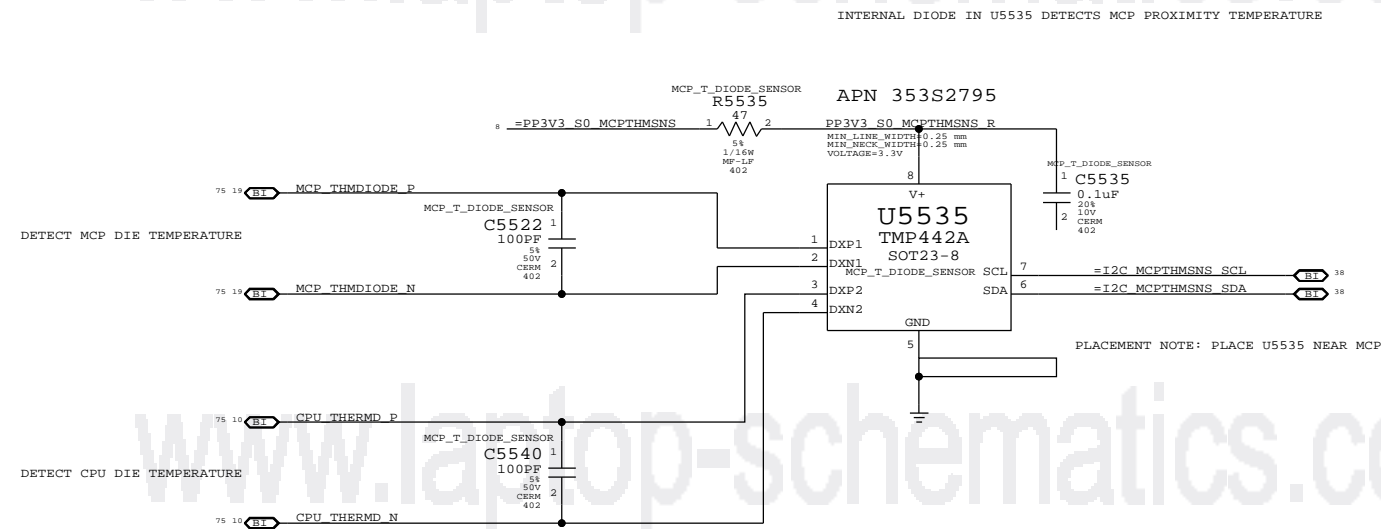


PAGE TITLE		SYNC MASTER=T27 MLB		SYNC DATE=02/02/2010	
Current Sensing					
Apple Inc.		DRAWING NUMBER	051-8561	SIZE	D
		REVISION	C.0.0	BRANCH	
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PAGE		54 OF 109		SHEET	
				40 OF 76	

CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR



MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR

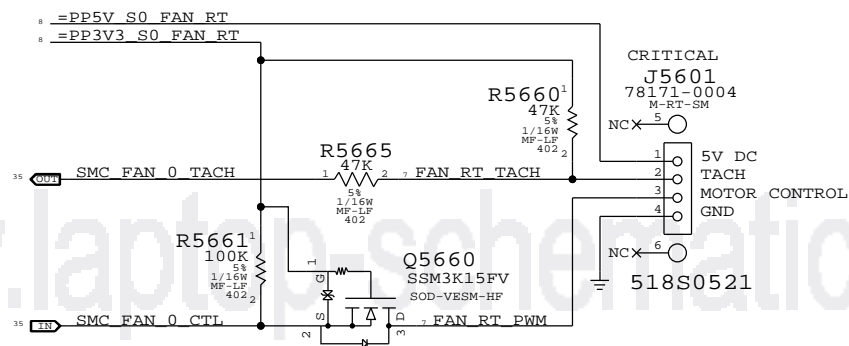


SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE Thermal Sensors			
DRAWING NUMBER 051-8561		SIZE D	
REVISION C.0.0		BRANCH	
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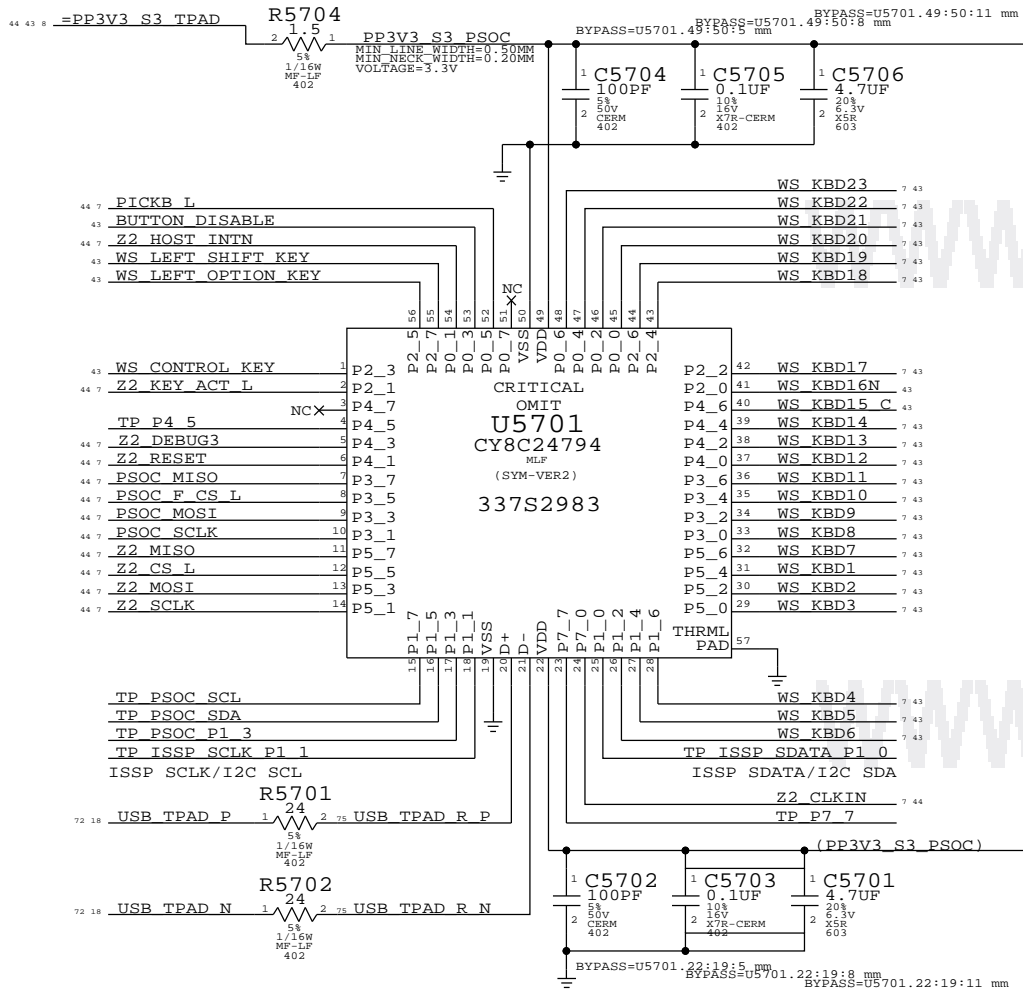
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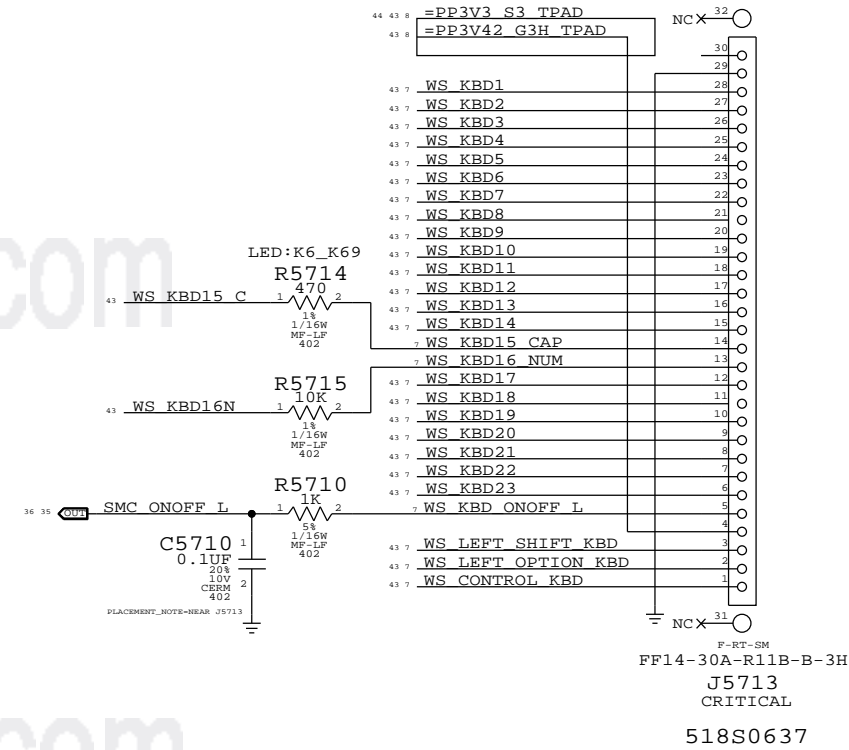
SYNC_MASTER=T27_MLB		SYNC_DATE=02/16/2010	
PAGE TITLE Fan Connector			
DRAWING NUMBER 051-8561		SIZE D	
REVISION C.0.0		BRANCH	
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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

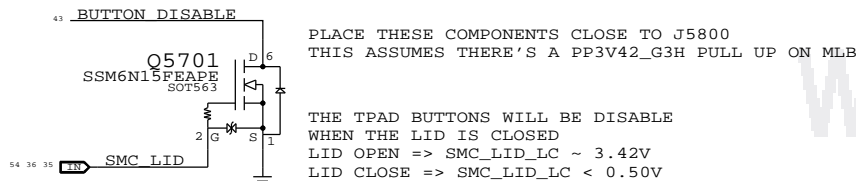


Keyboard Connector



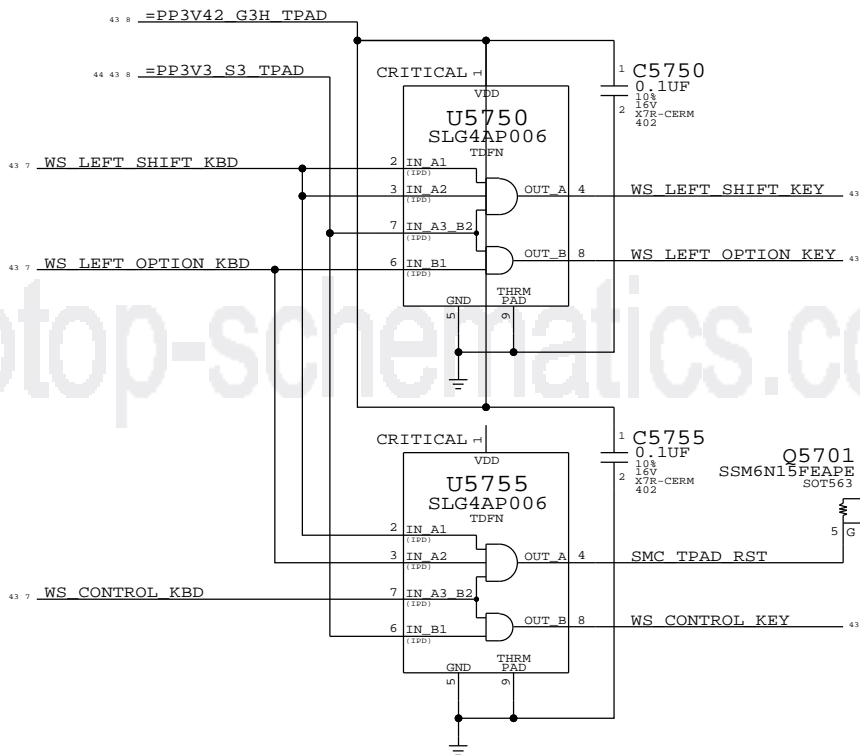
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	80UA			0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	14MA (MAX)			0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

TPAD Buttons Disable



SMC Manual Reset & Isolation

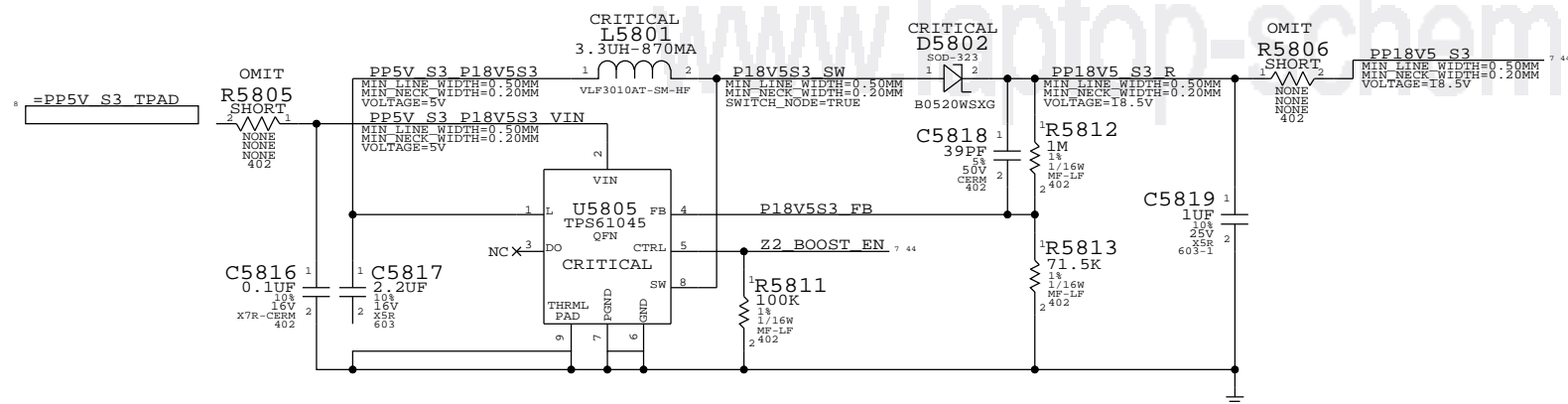
Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.



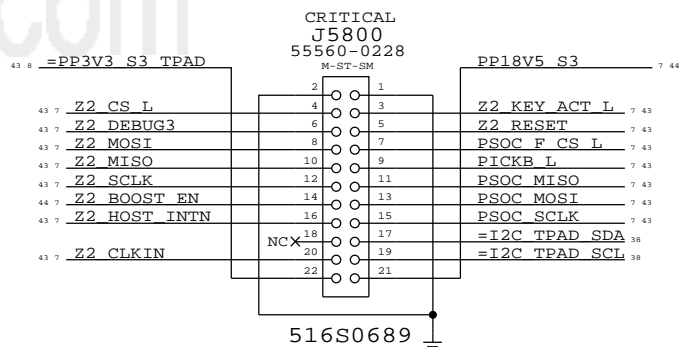
SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
WELLSPRING 1			
Apple Inc.		DRAWING NUMBER	051-8561
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		PAGE	57 OF 109
		SHEET	43 OF 76

BOOSTER +18.5VDC FOR SENSORS

- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED



IPD Flex Connector



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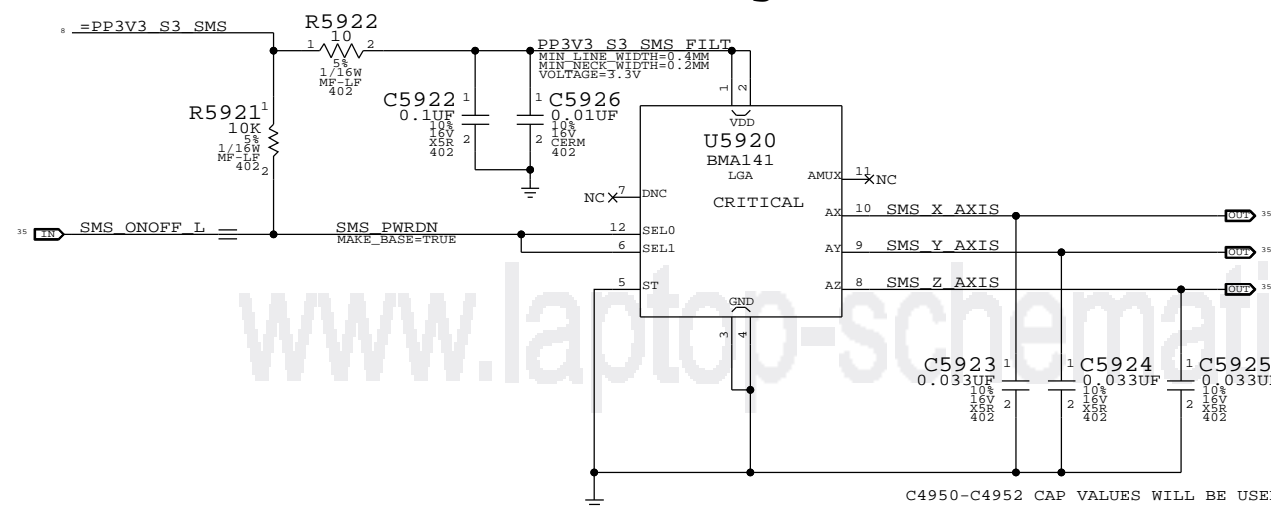
DO NOT SYNC FROM T27. REMOVED KEYBOARD BKLIGHT CIRCUIT

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE WELLSPRING 2			
Apple Inc.	DRAWING NUMBER	051-8561	SIZE D
	REVISION	C.0.0	
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		SHEET	44 OF 76

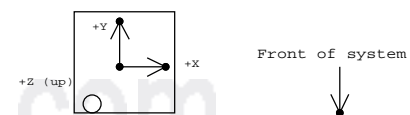
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R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC

Analog SMS



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

C4950-C4952 CAP VALUES WILL BE USED TO GET CUT-OFF FREQUENCY OF ~146HZ

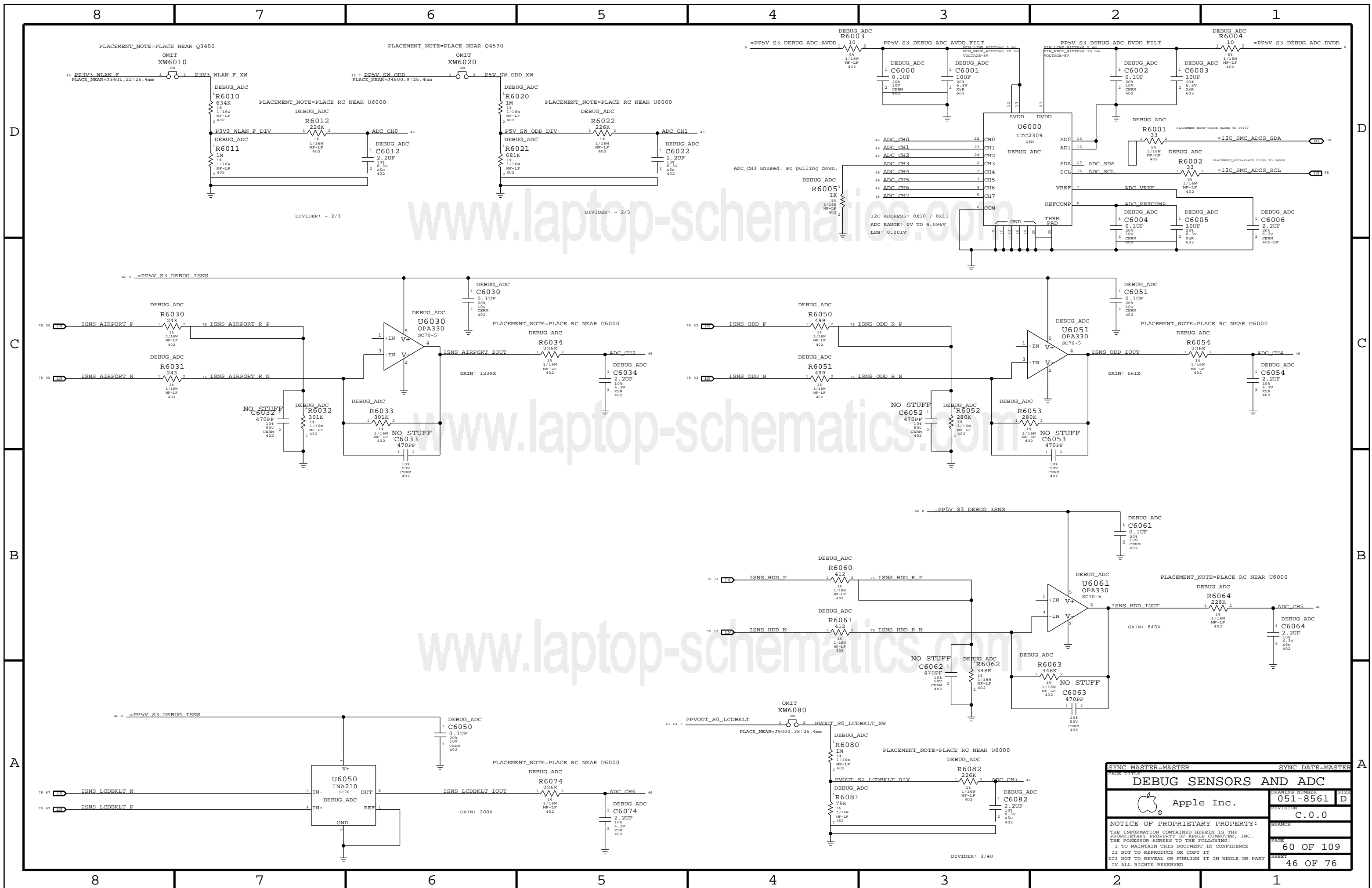
PLACE_NEARs:

C5923:1:PLACE_NEAR=U4900.M10:2.54MM
C5924:1:PLACE_NEAR=U4900.N9:2.54MM
C5925:1:PLACE_NEAR=U4900.K10:2.54MM

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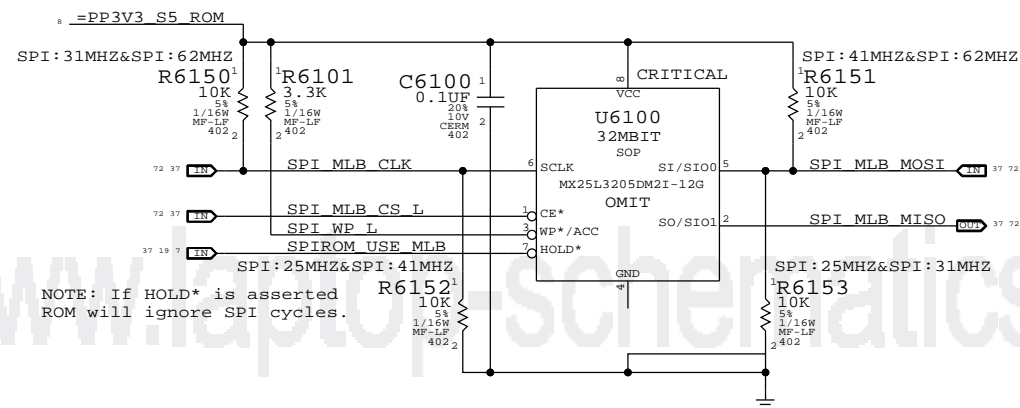
DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923,C5924,C5925. ADDED PLACE NEARS

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE SMS			
DRAWING NUMBER 051-8561		SIZE D	
REVISION C.0.0		BRANCH	
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SYNC MASTER=MASTER		SYNC DATE=MASTER	
DEBUG SENSORS AND ADC			
Apple Inc.		DRAWING NUMBER	051-8561
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		PAGE	60 OF 109
		SHEET	46 OF 76

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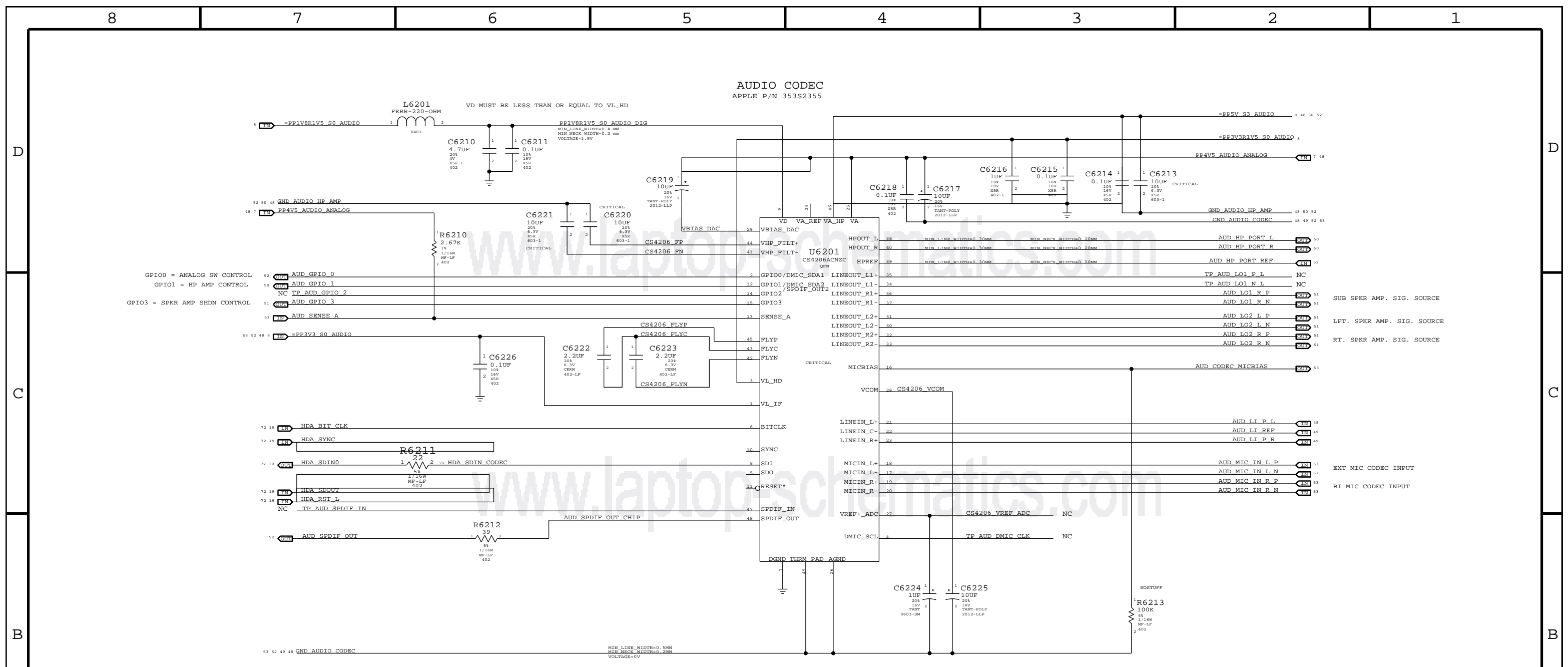
MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

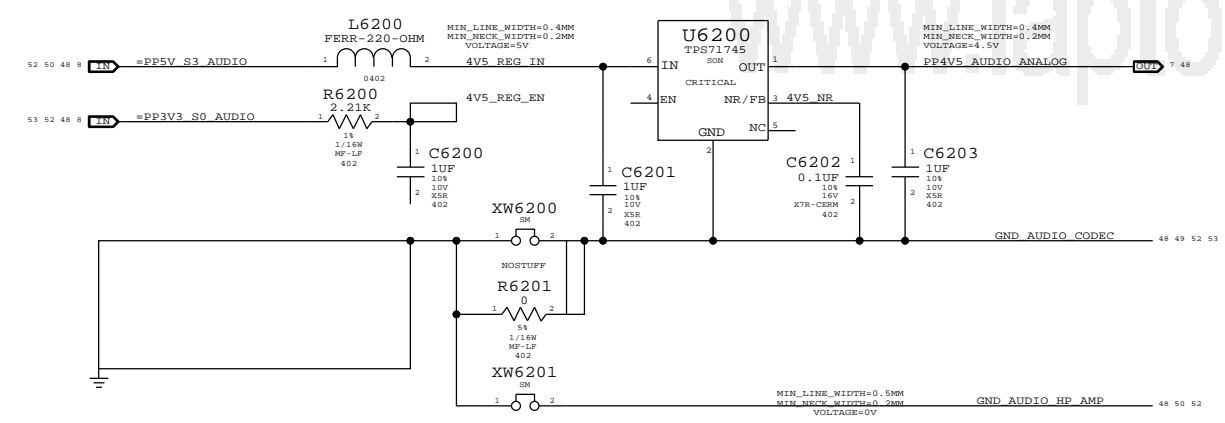
NOTE: 42 & 62 MHz use FAST_READ command.

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SYNC_MASTER=T27_MLB		SYNC_DATE=02/16/2010	
PAGE TITLE SPI ROM			
Apple Inc.		DRAWING NUMBER 051-8561	SIZE D
		REVISION C.0.0	
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		PAGE	61 OF 109
		SHEET	47 OF 76



4.5V POWER SUPPLY FOR CODEC APPLE P/N 353S2281



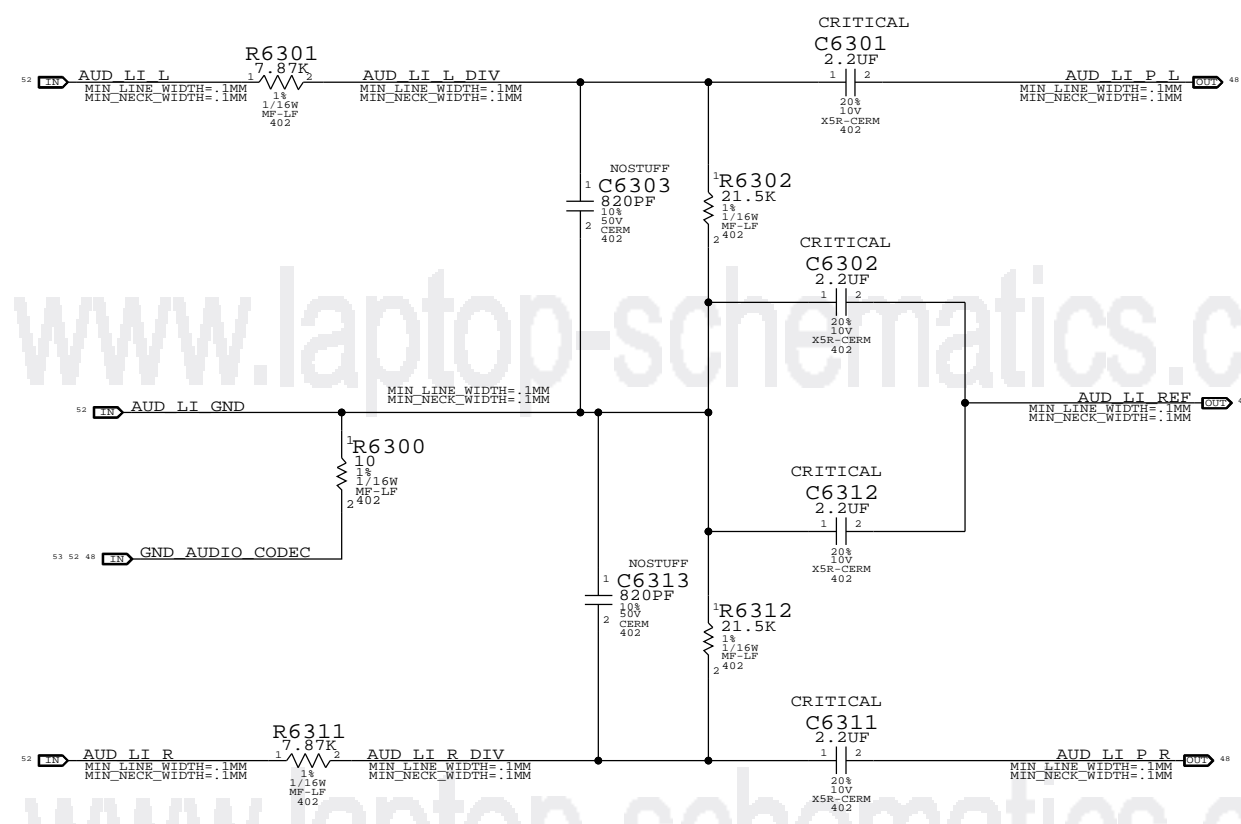
NOTES ON CODEC I/O

- DIFF FSINPUT= 2.45VRMS
- SE FSINPUT= 1.22VRMS
- DAC1 FSOUTPUT= 1.34VRMS
- DAC2/3 FSOUTPUTDIFF= 2.67VRMS
- DAC2/3 FSOUTPUTSE= 1.34VRMS

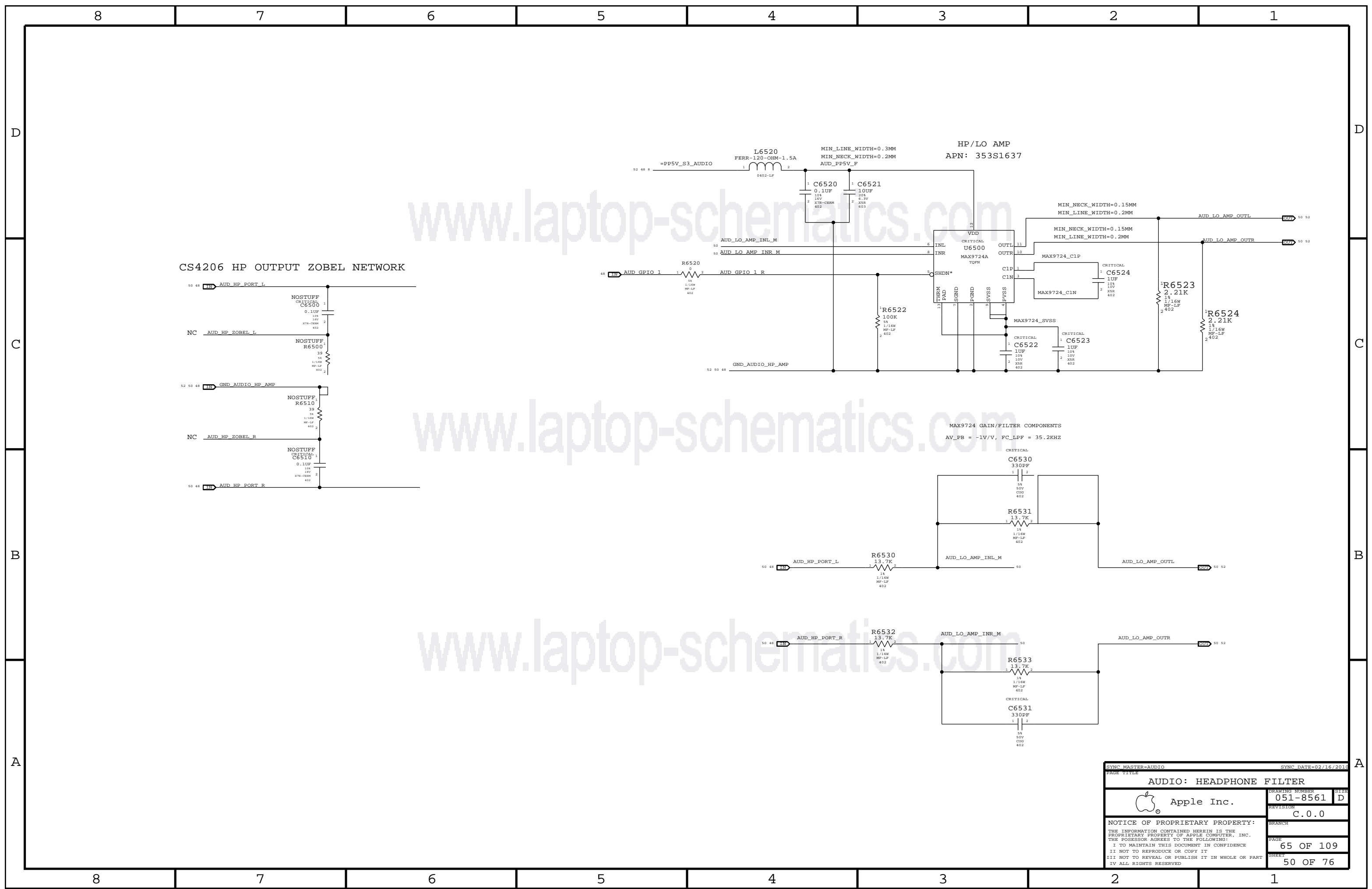
SYNC MASTER=AUDIO		SYNC DATE=02/16/2011	
AUDIO: CODEC/REGULATOR			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		PAGE	62 OF 109
		SHEET	48 OF 76
		SIZE	D

LINE INPUT VOLTAGE DIVIDER

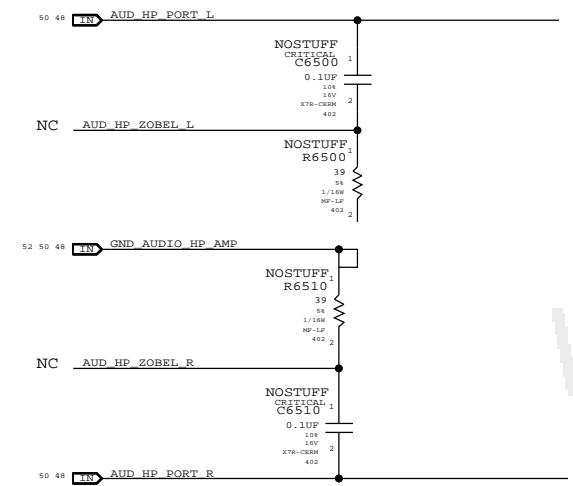
CODEC RIN = 20K OHMS
 NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
 FC_HP = 3.6 HZ
 FC_LP = 43KHZ
 VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE AUDIO: LINE INPUT FILTER		
Apple Inc.	DRAWING NUMBER 051-8561	SIZE D
	REVISION C.0.0	BRANCH
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	PAGE 63 OF 109	SHEET 49 OF 76



CS4206 HP OUTPUT ZOBEL NETWORK



HP/LO AMP
APN: 353S1637

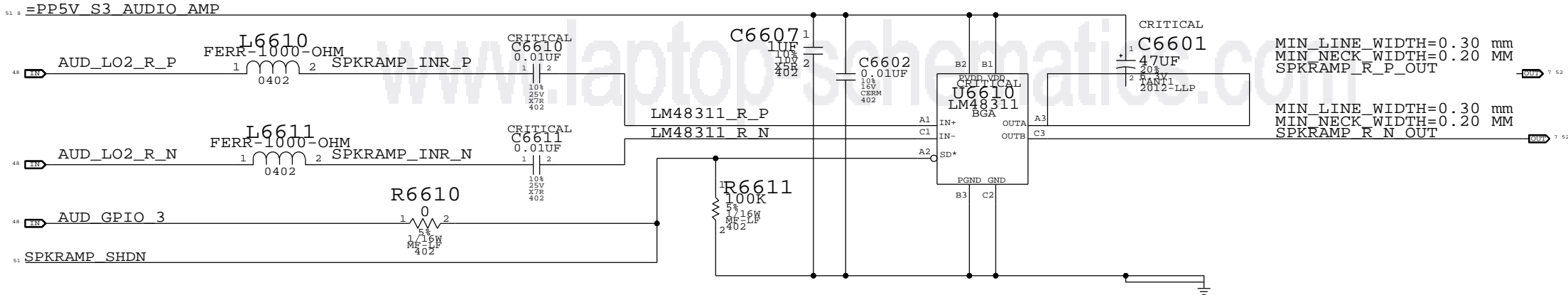
MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ

SYNC MASTER=AUDIO		SYNC DATE=02/16/2011	
AUDIO: HEADPHONE FILTER			
 Apple Inc.	DRAWING NUMBER	051-8561	SIZE
	REVISION	C.0.0	
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SATELLITE 796Hz < HPF FC < 936Hz
 SUB 80 Hz < HPF FC < 94 Hz
 GAIN 6DB (2V/V)
 SPRK AMP. INPUT REFERRED CLIP POINT = ~-6dBFS

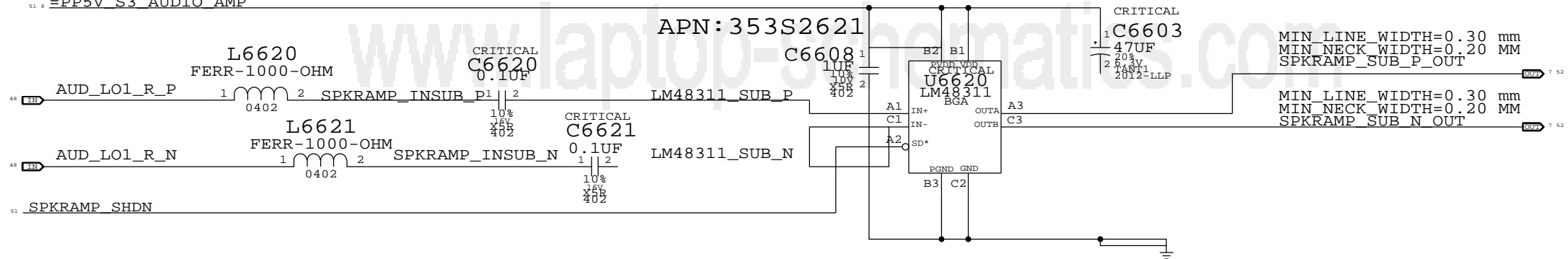
ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

APN: 353S2621



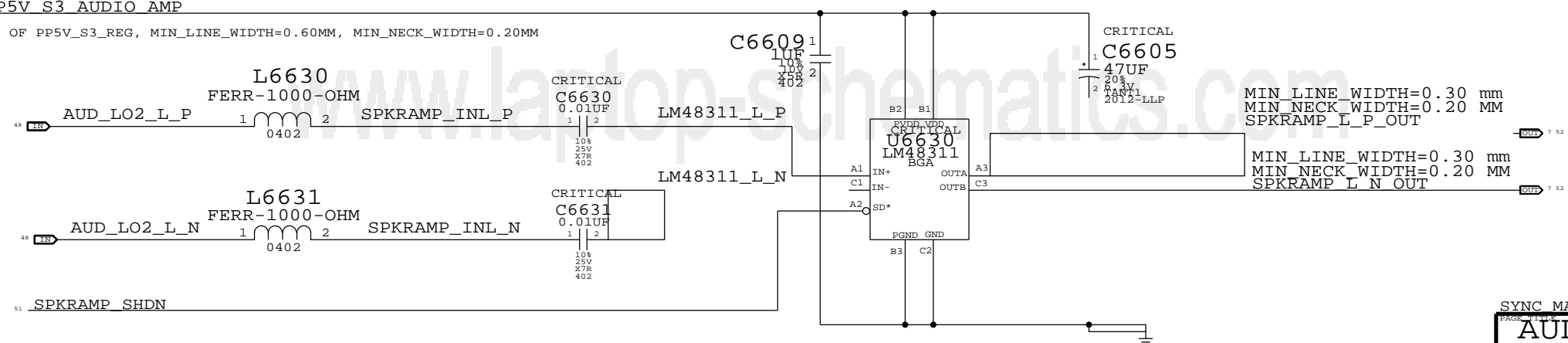
ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

APN: 353S2621



ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

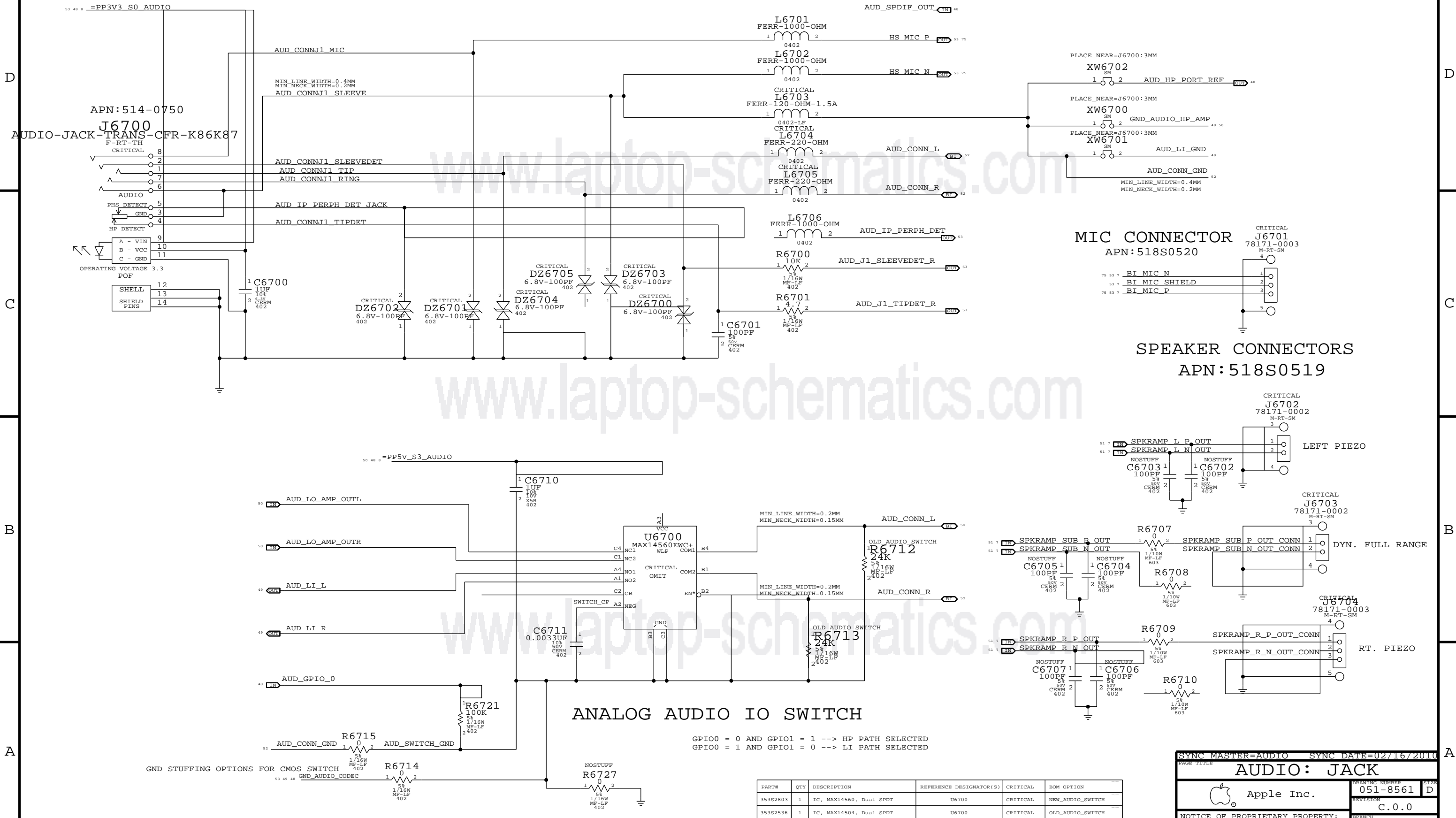
APN: 353S2621



SYNC MASTER=AUDIO SYNC DATE=02/16/2010

AUDIO: SPEAKER AMP		
Apple Inc.	DRAWING NUMBER 051-8561	SIZE D
	REVISION C.0.0	
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AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



PAGE TITLE		SYNC MASTER=AUDIO SYNC DATE=02/16/2010	
AUDIO: JACK		DRAWING NUMBER	SIZE
Apple Inc.		051-8561	D
		REVISION	
		C.0.0	
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2803	1	IC, MAX14560, Dual SPDT	U6700	CRITICAL	NEW_AUDIO_SWITCH
353S2536	1	IC, MAX14504, Dual SPDT	U6700	CRITICAL	OLD_AUDIO_SWITCH

GPI00 = 0 AND GPI01 = 1 --> HP PATH SELECTED
 GPI00 = 1 AND GPI01 = 0 --> LI PATH SELECTED

DO NOT SYNC K84. UPDATED PLACE NEARS

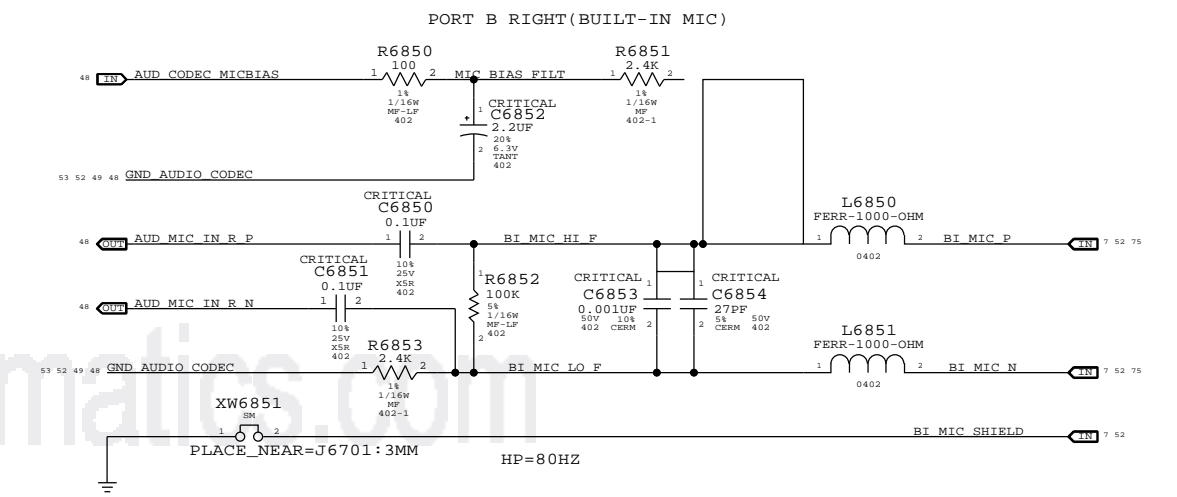
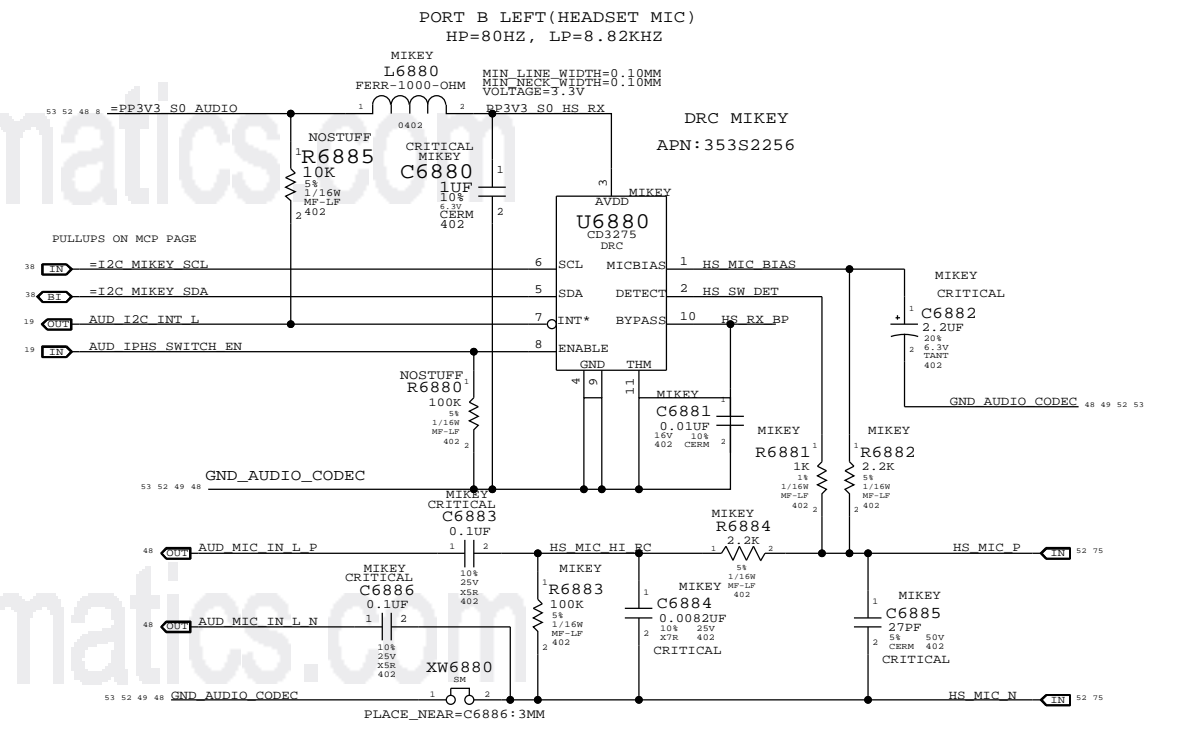
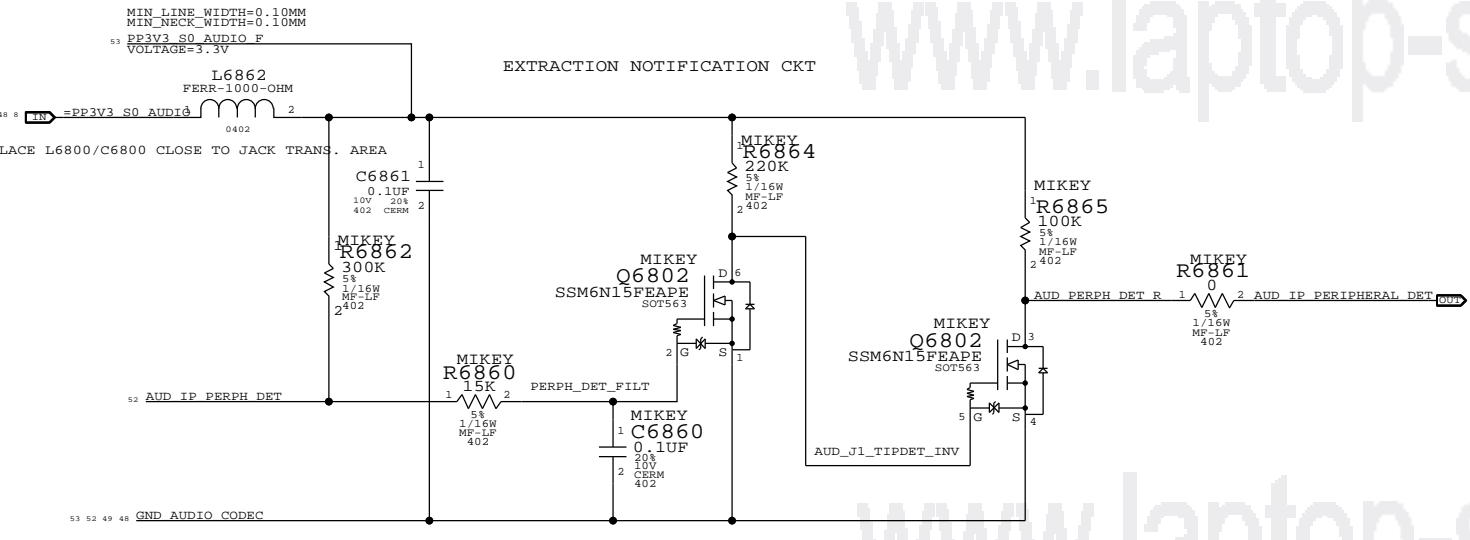
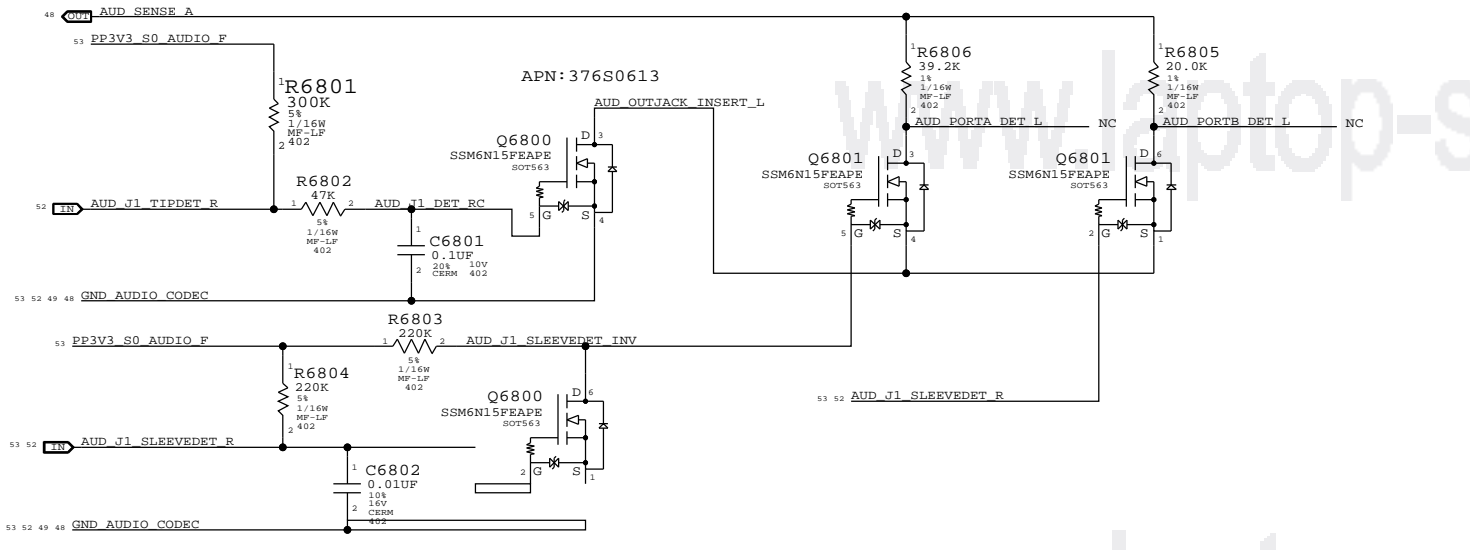
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF/ENABLE	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MCP79 GPIO_38	MCP79 GPIO_17 (PERIPH_DETECT) MCP79 GPIO_4 (LOAD_DETECT)

PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)

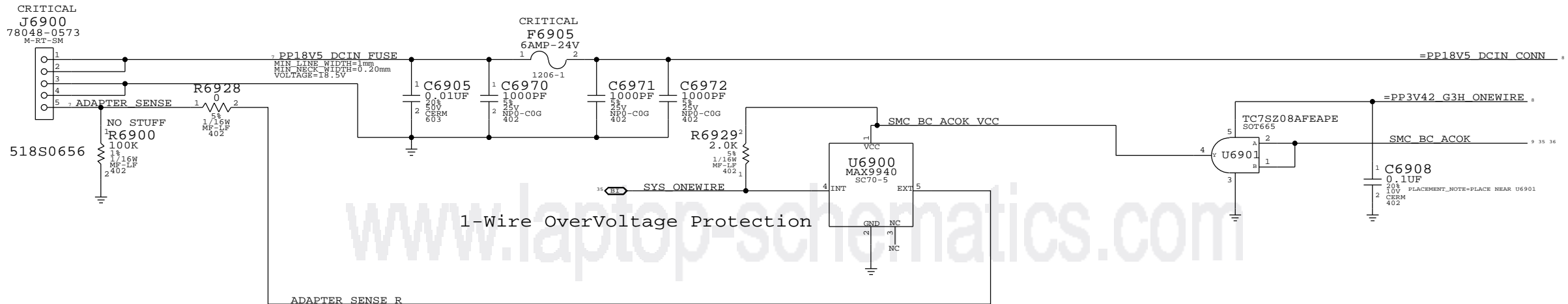


SYNC MASTER=AUDIO SYNC DATE=02/16/2010

AUDIO: JACK TRANSLATORS

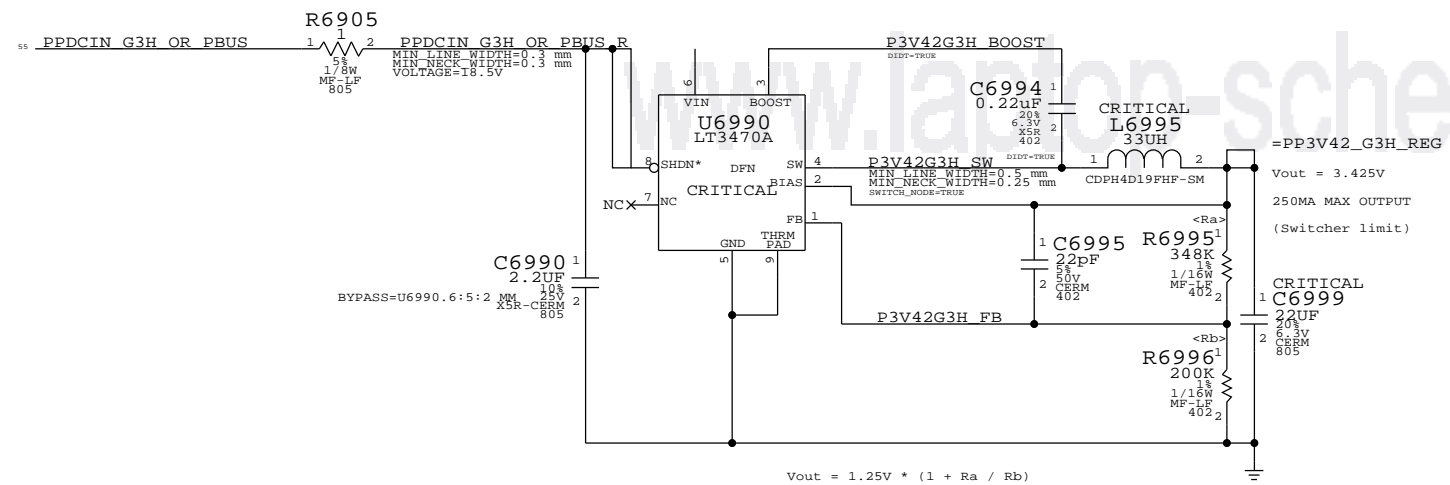
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	REVISION	C.0.0		
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SHEET	53 OF 76			

MagSafe DC Power Jack



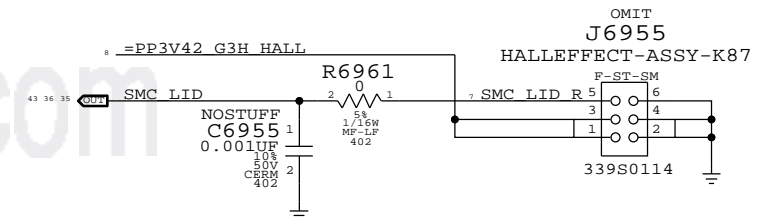
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator



HALL EFFECT ASSEMBLY

- Assembly APN: 339S0114
- BOM: 639-0680
- PCBF: 820-2801
- MCO: 056-3515
- Conn APN: 518S0788

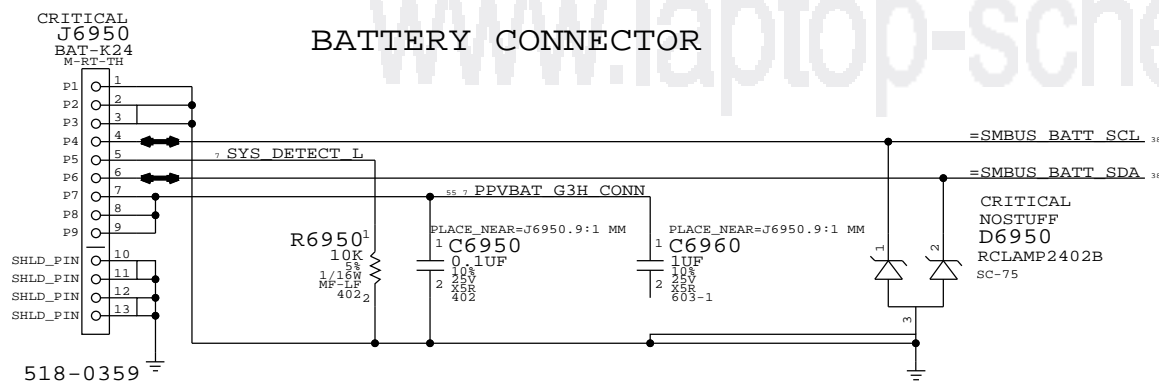


PROTO 0: STUFFING K84 CONNECTOR ONTO MODIFIED K84 PADS
 PROTO 1: STUFFING K87 HALL EFFECT ASSEMBLY ONTO K87 PADS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6831	1	SUB ASSY - HALL EFFECT, K86 K87	J6955	CRITICAL	

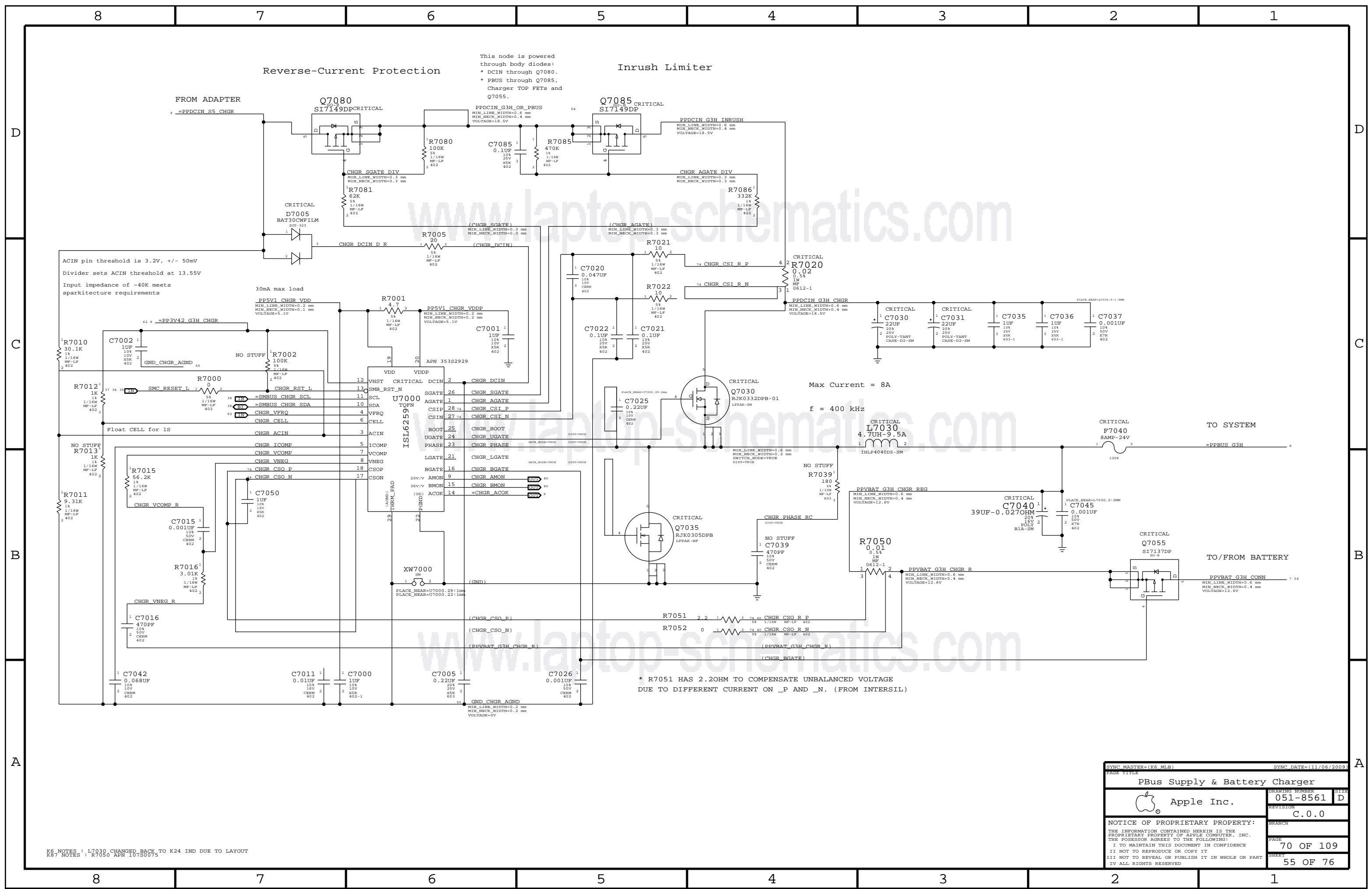
PN: 607-6831 for WCPM. PN: 339S0114 for schematic/board layout

BATTERY CONNECTOR



DO NOT SYNC WITH K84. R6900,C6960,SIGNAL NAMES CHANGED. HALL EFFECT CONNECTOR CHANGED.

PAGE TITLE		SYNC DATE=MASTER	
DC-In & Battery Connectors		DRAWING NUMBER	051-8561
Apple Inc.		REVISION	C.0.0
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Reverse-Current Protection

Inrush Limiter

This node is powered through body diodes:
 * DCIN through Q7080.
 * PBUS through Q7085, Charger TOP FETs and Q7055.

ACIN pin threshold is 3.2V, +/- 50mV
 Divider sets ACIN threshold at 13.55V
 Input impedance of ~40K meets sparkitecture requirements

30mA max load

Max Current = 8A

f = 400 kHz

* R7051 HAS 2.20HM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT
 K67 NOTES : R7050 APN 10750075

SYNC MASTER=(K6_MLB)		SYNC DATE=(11/06/2009)	
PAGE TITLE			
PBus Supply & Battery Charger			
Apple Inc.	DRAWING NUMBER	051-8561	SIZE D
	REVISION	C.0.0	
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		55 OF 76	

5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

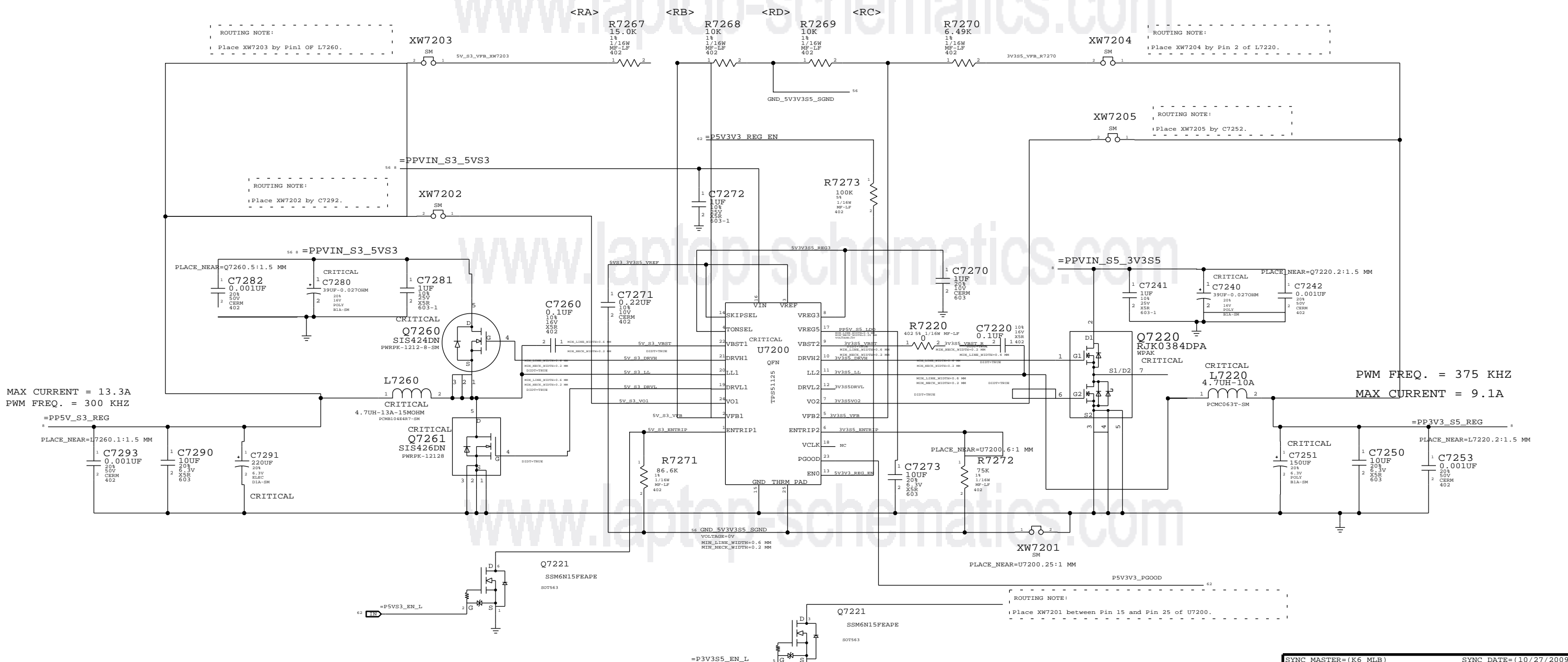
$$V_{OUT} = (2 * R_C / R_D) + 2$$

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MAX CURRENT = 13.3A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 9.1A

NOTE: DONT SYNC THIS PAGE FROM T27

SEPARATED MASTER PGOOD FOR BOTH 5V AND 3V3.

SYNC MASTER=(K6 MLB)		SYNC DATE=(10/27/2009)	
PAGE TITLE 5V/3.3V SUPPLY			
DRAWING NUMBER 051-8561		SIZE D	
REVISION C.0.0		BRANCH	
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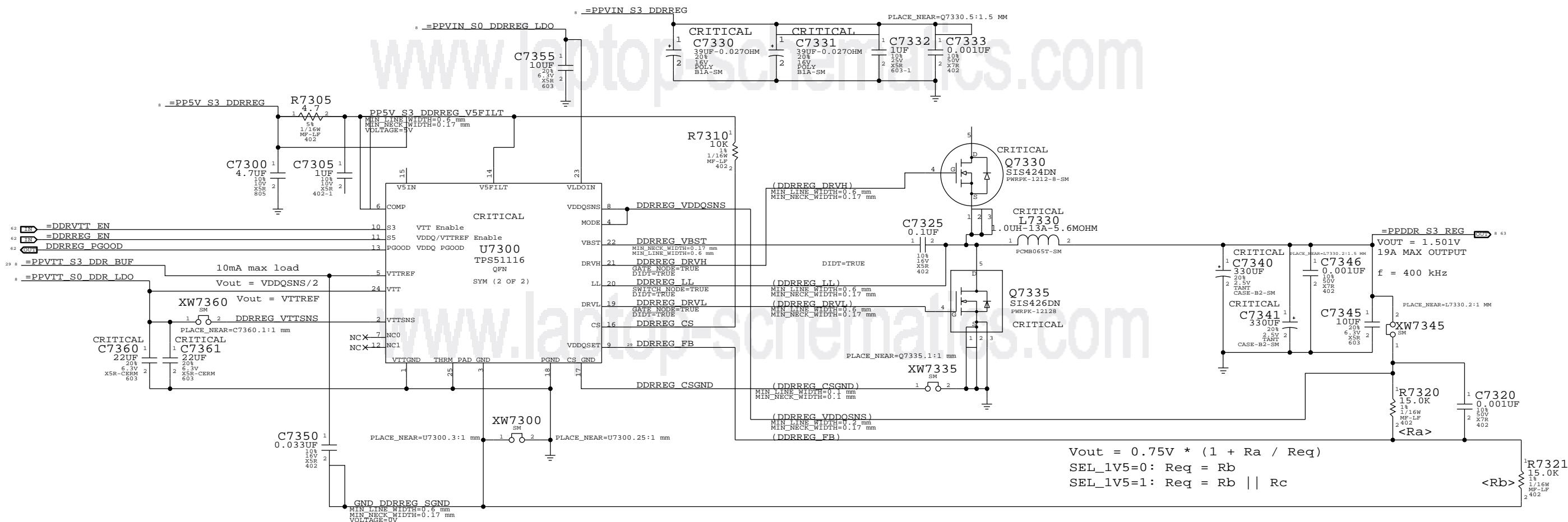
D
C
B
A

D
C
B
A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

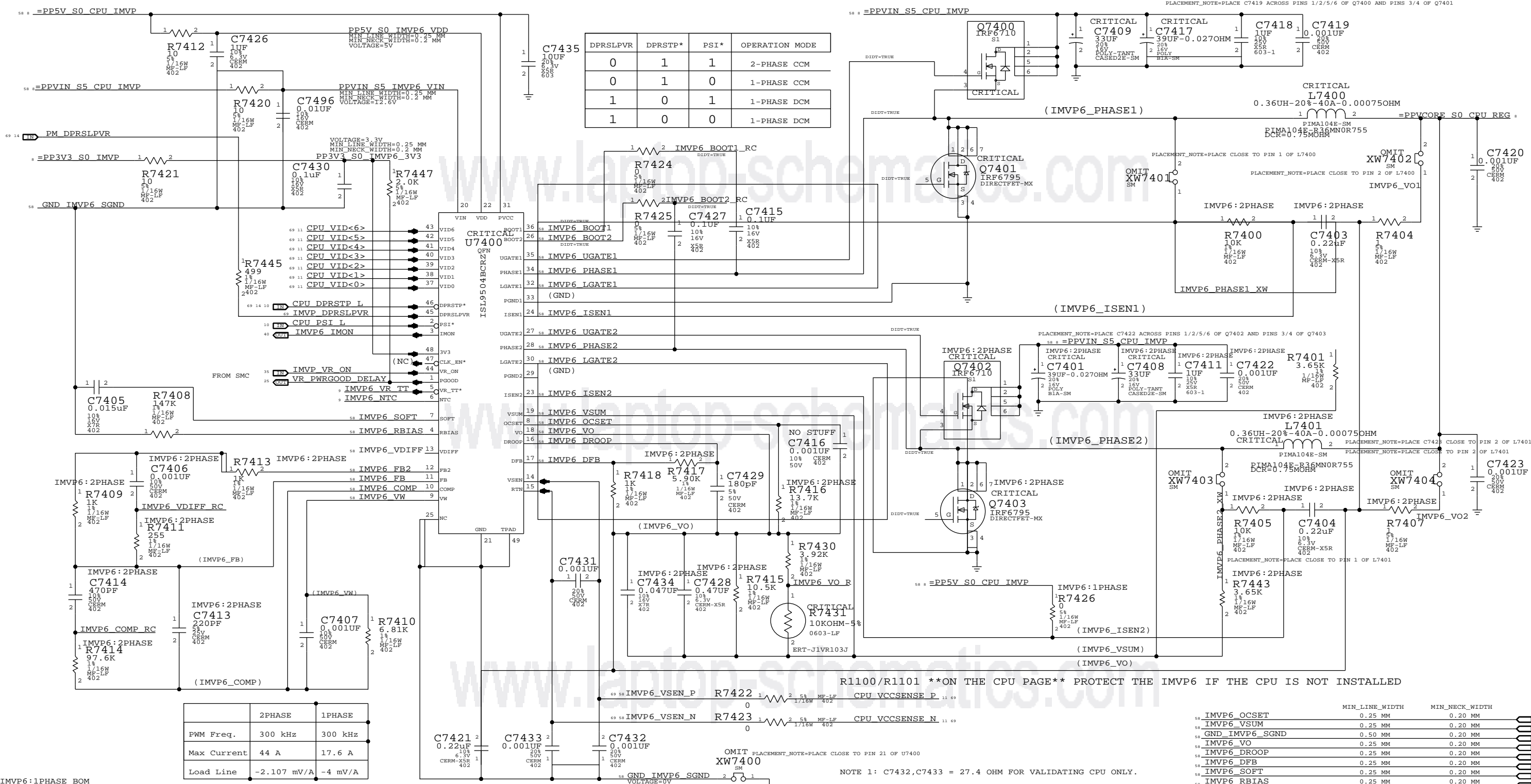
1.5V/0.75 DDR3 POWER SUPPLY



NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS
 NOTE: DONT SYNC THIS PAGE FROM K6 REMOVED R7380

SYNC MASTER=(K6 MLB)		SYNC DATE=(11/06/2009)	
1.5V/0.75V DDR3 SUPPLY			
Apple Inc.		DRAWING NUMBER	051-8561
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IMVP6 CPU VCORE REGULATOR



	2PHASE	1PHASE
PWM Freq.	300 kHz	300 kHz
Max Current	44 A	17.6 A
Load Line	-2.107 mV/A	-4 mV/A

IMVP6:1PHASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES.MTL.FILM,1/16W,8.25K,1.0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES.MTL.FILM,1/16W,16.9K,1.0402,SMD,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER.,.220P,20.6.3V,XSR,0402	C7428		IMVP6:1PHASE
114S0236	1	RES.MTL.FILM,1/16W,1.58K,1.0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES.MTL.FILM,1/16W,255 OHM,1.0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP CER 470PF,+-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES.MTL.FILM,1/16W,97.6K,1.0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,100PF,50V,50V,CC0402	C7413		IMVP6:1PHASE

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_VSEN_P	0.25 MM	0.25 MM
IMVP6_VSEN_N	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_PHASE2	1.5 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

SYNC MASTER=(K84 MLB) SYNC DATE=(11/18/2009)

IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8561

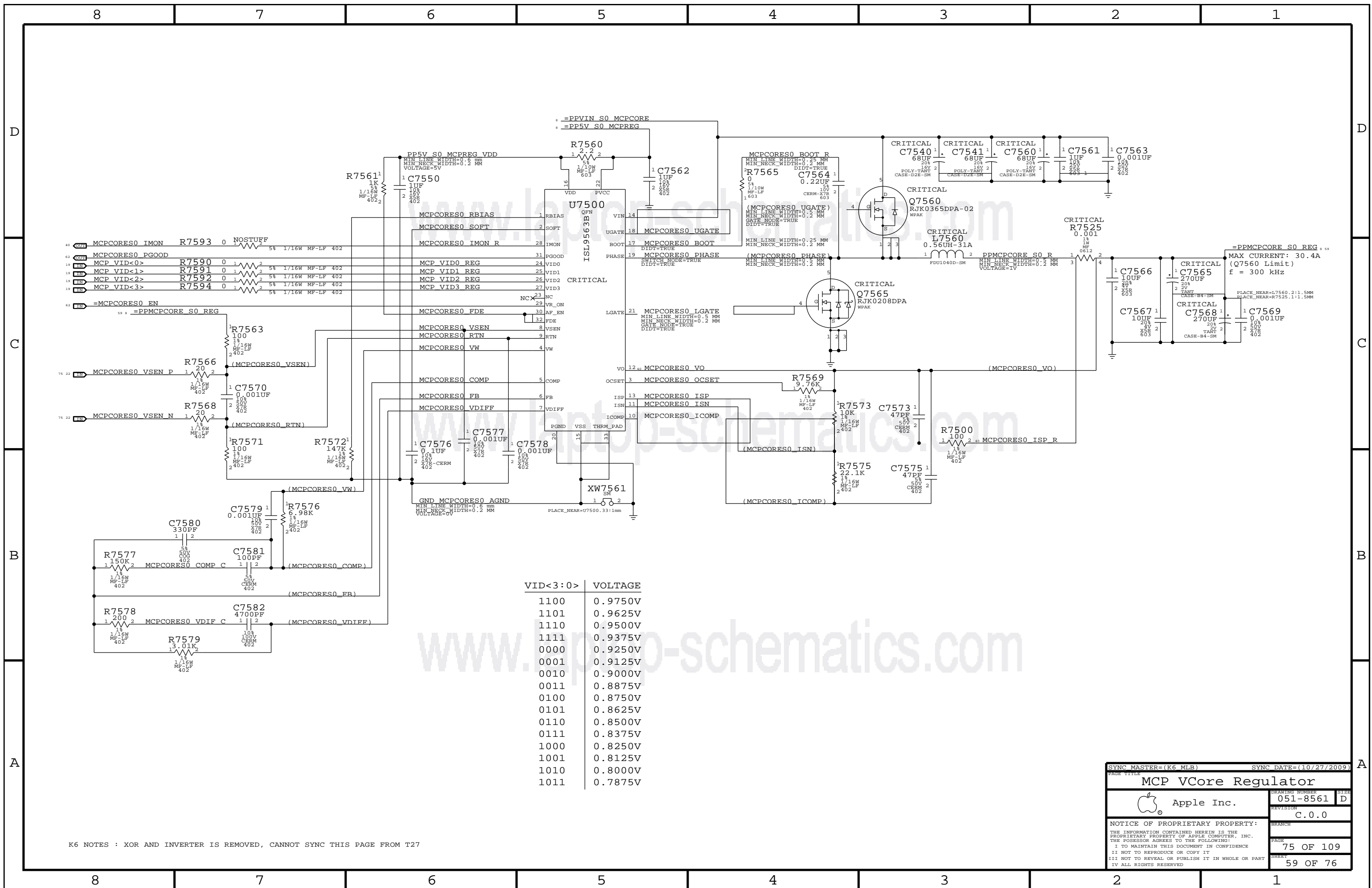
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NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED



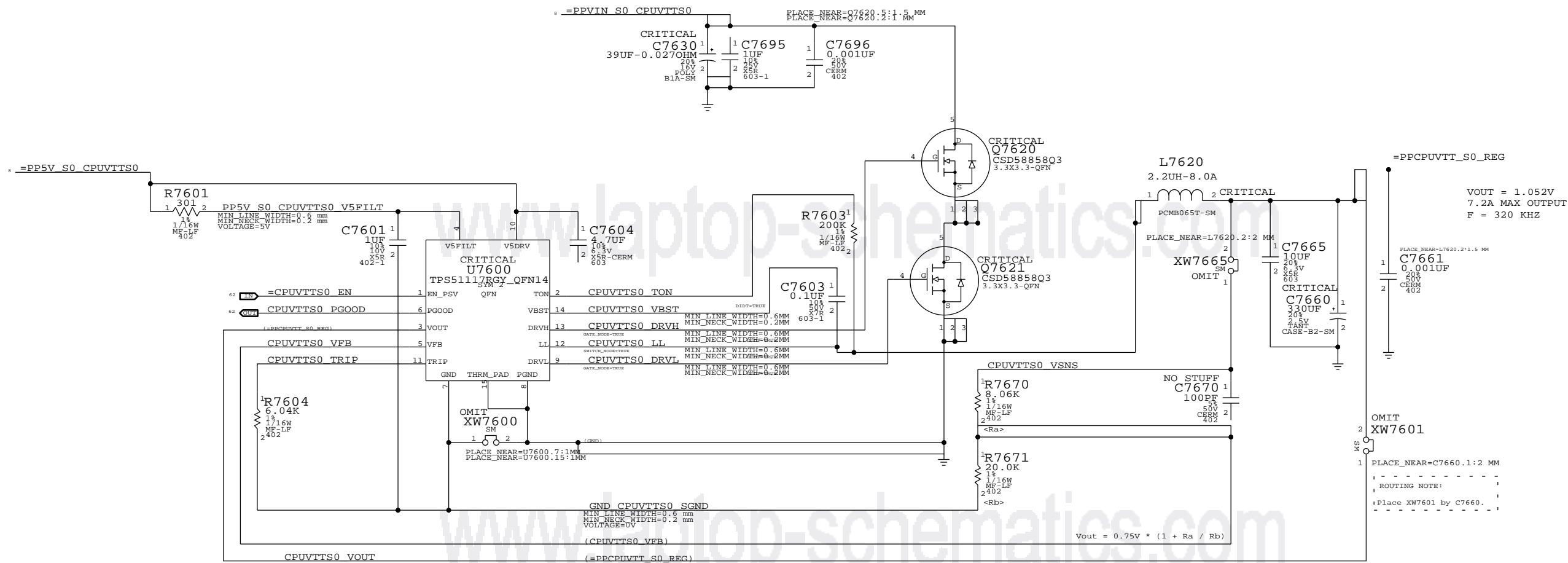
VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=(K6 MLB)		SYNC DATE=(10/27/2009)	
MCP VCore Regulator			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		PAGE	75 OF 109
		SHEET	59 OF 76

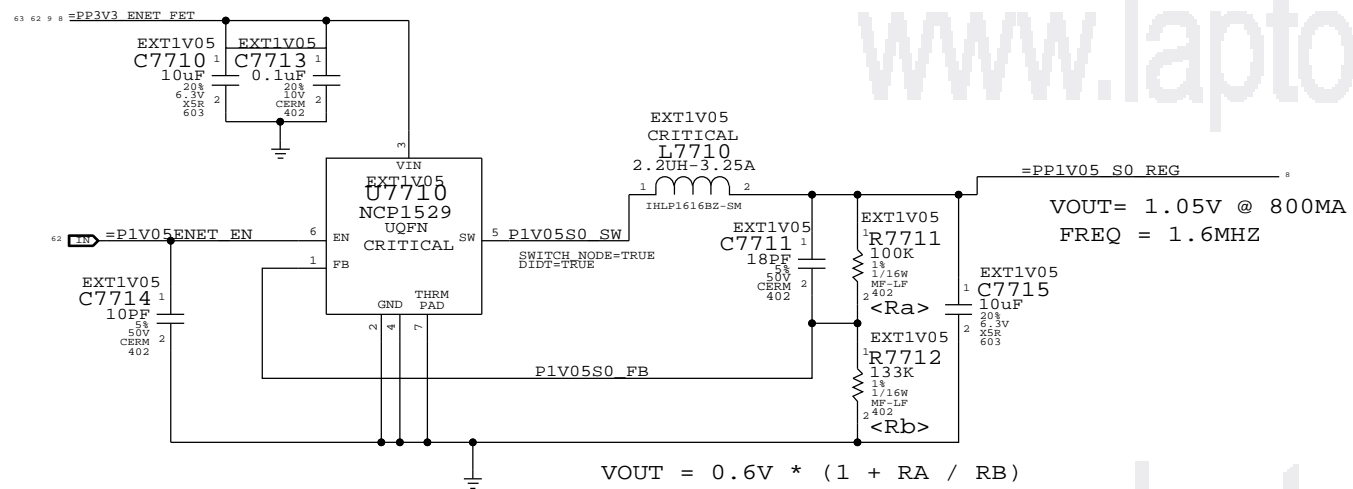
CPUVTT POWER SUPPLY

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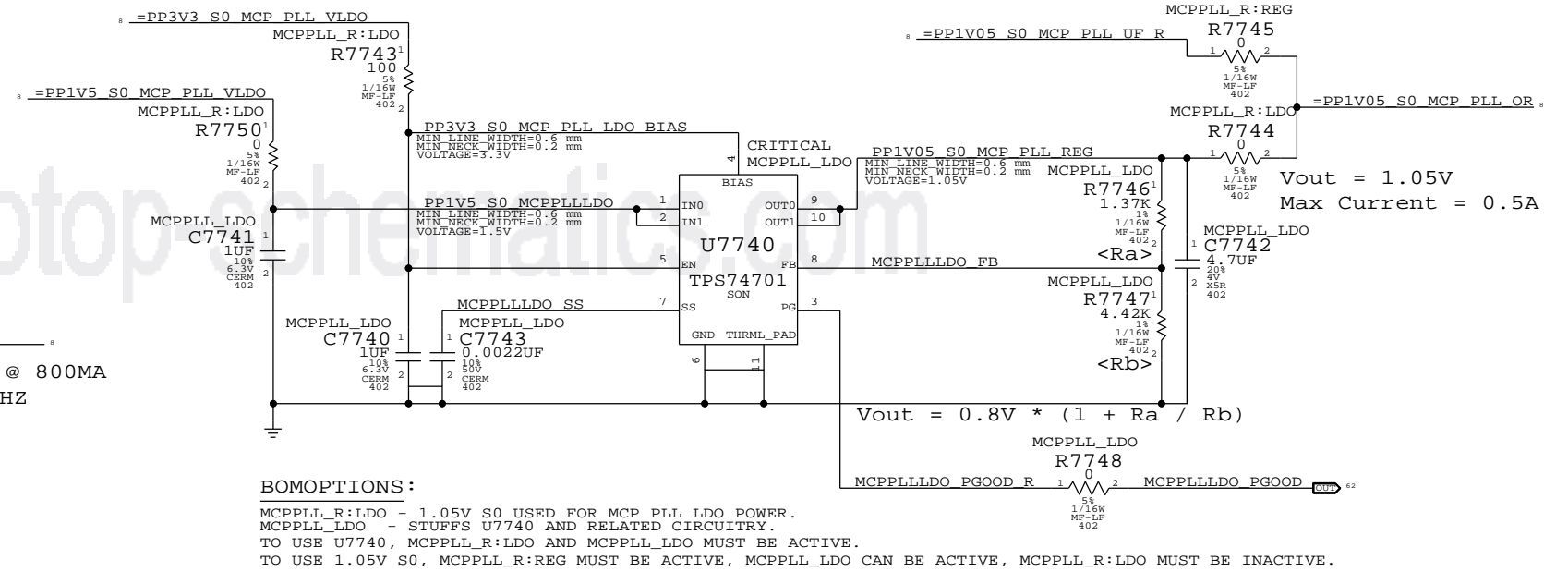


SYNC MASTER=(K84_MLB)		SYNC DATE=(02/04/2009)	
CPU VTT(1.05V) SUPPLY			
DRAWING NUMBER		SIZE	
051-8561		D	
REVISION		BRANCH	
C.0.0			
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PAGE		SHEET	
76 OF 109		60 OF 76	

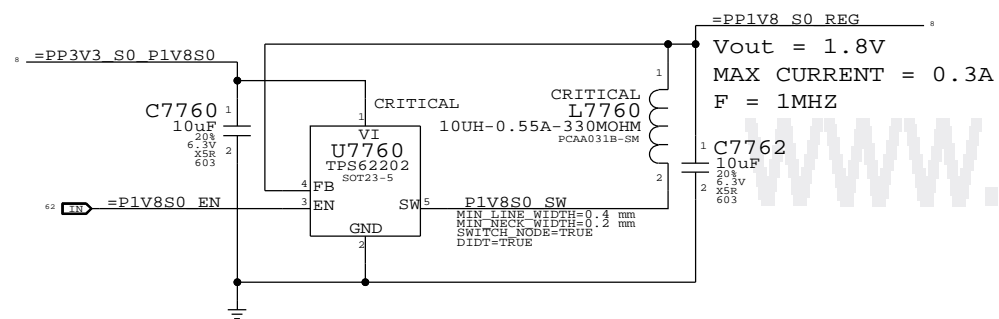
1.05V ENET Switcher



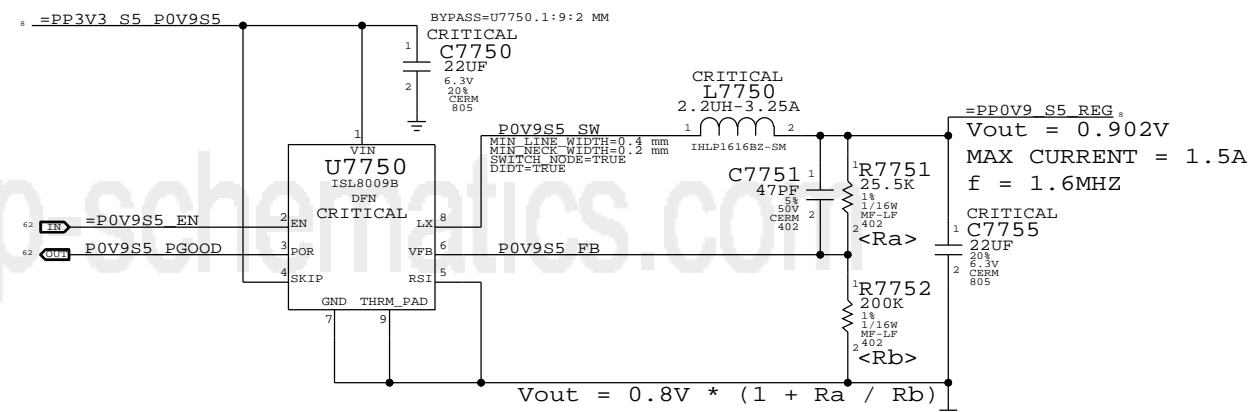
1.05V S0 MCP PLL LDO



1.8V S0 Switcher



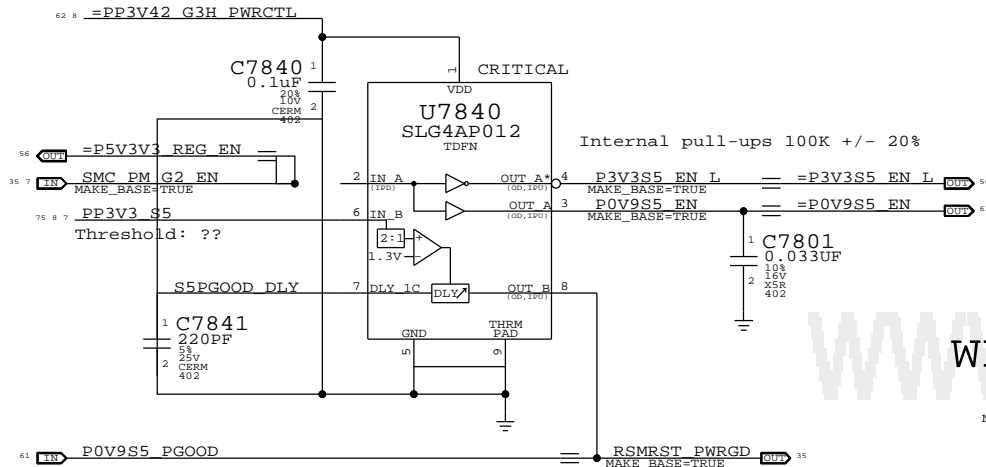
MCP 0.9V S5 (AUXC) Switcher



K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=MASTER		SYNC DATE=MASTER	
Misc Power Supplies			
Apple Inc.		DRAWING NUMBER	SIZE
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PAGE		77 OF 109	
SHEET		61 OF 76	

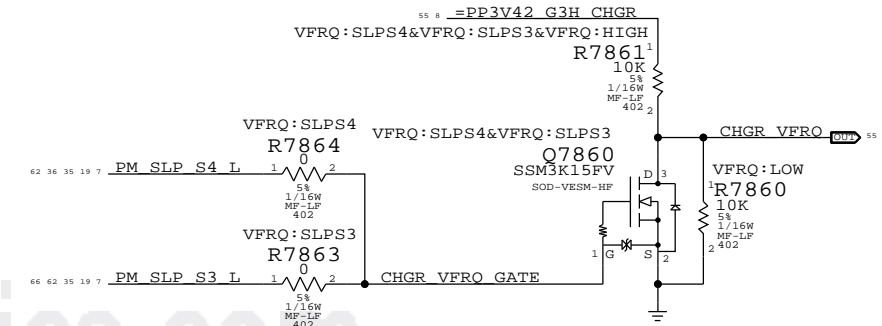
S5 Rail Enables & PGOOD



Power Control Signals

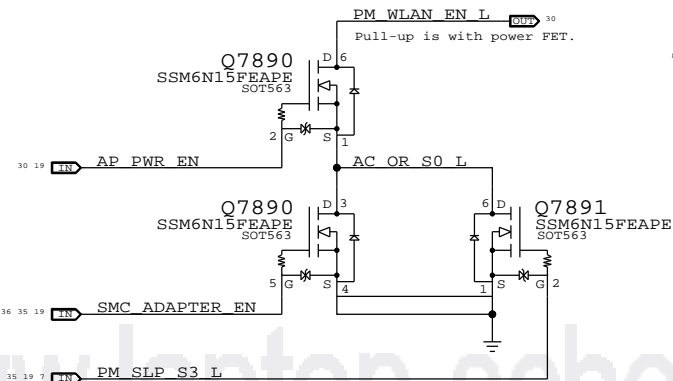
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select



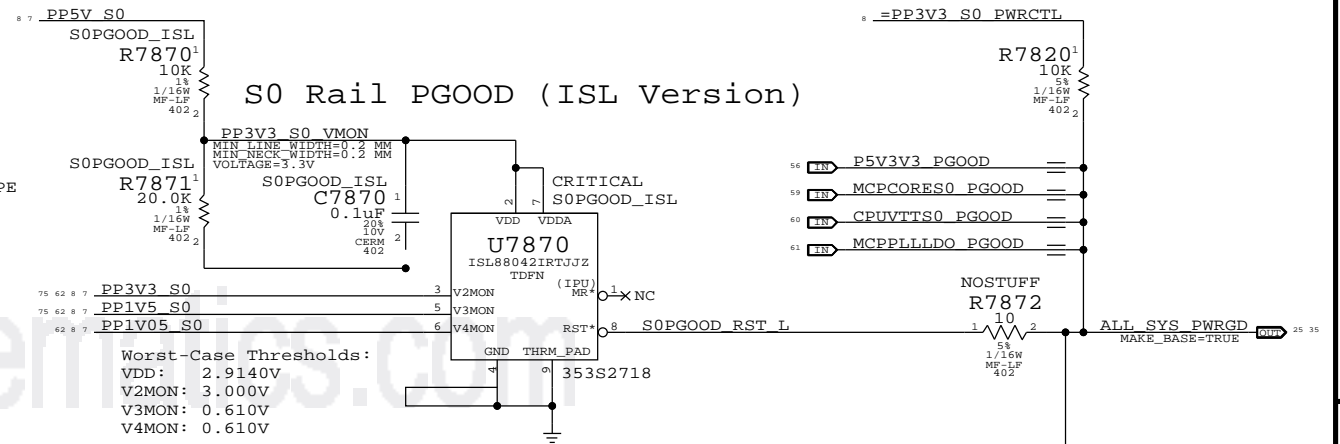
WLAN Enable Generation

WLAN = (*S3* && *AP_PWR_EN* && (*AC* || *S0*))
 NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.
 Pull-up is with power FET.

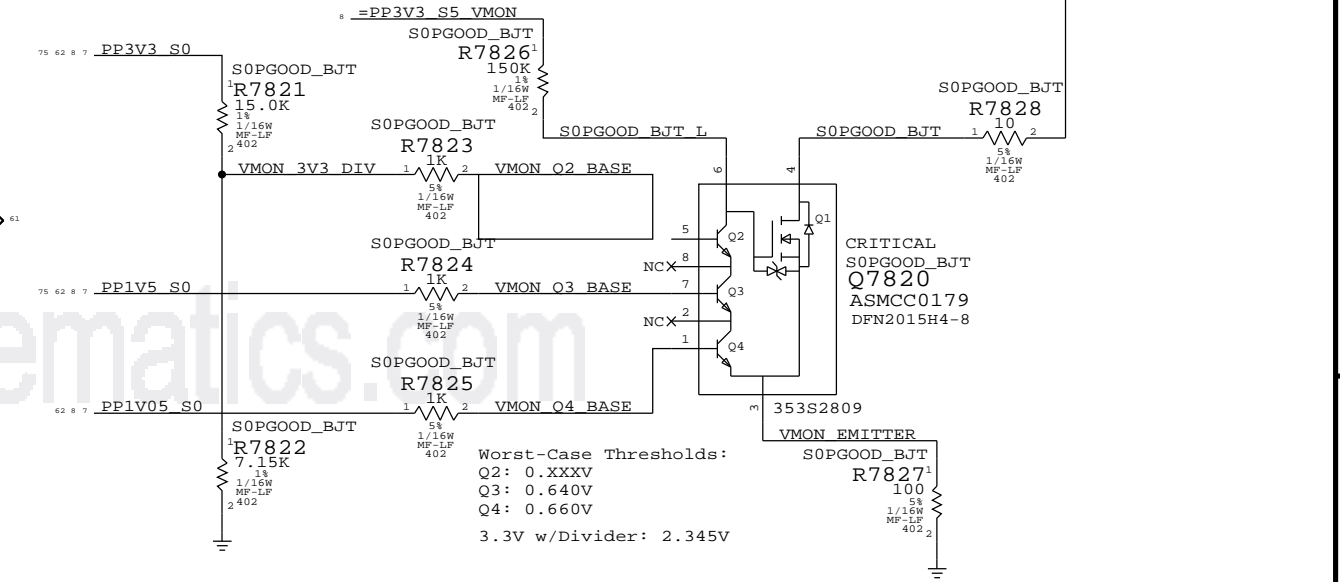


S0 Rail PGOOD Circuitry

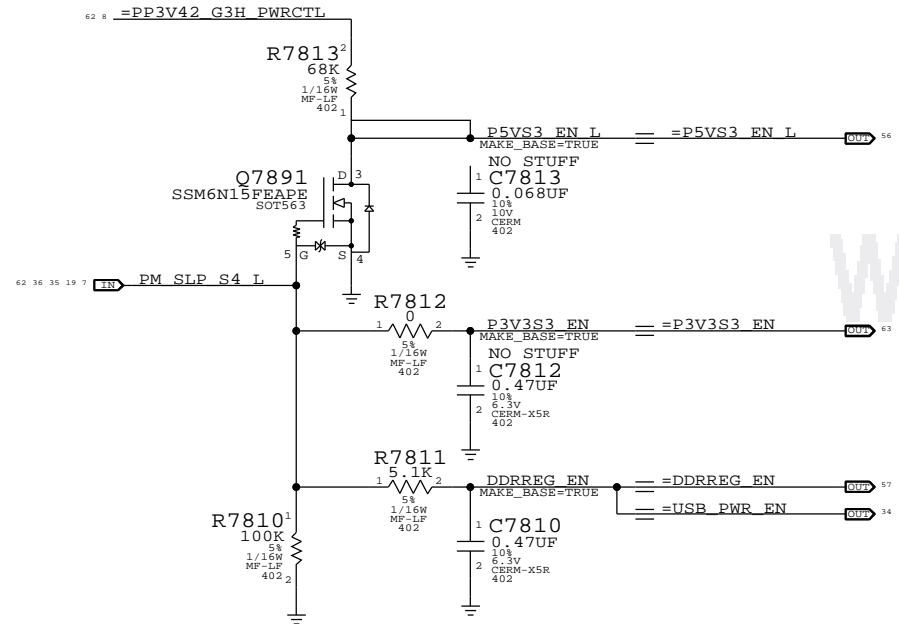
S0 Rail PGOOD (ISL Version)



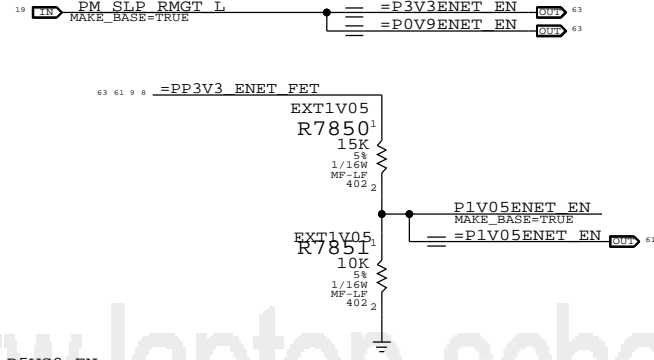
S0 Rail PGOOD (BJT Version)



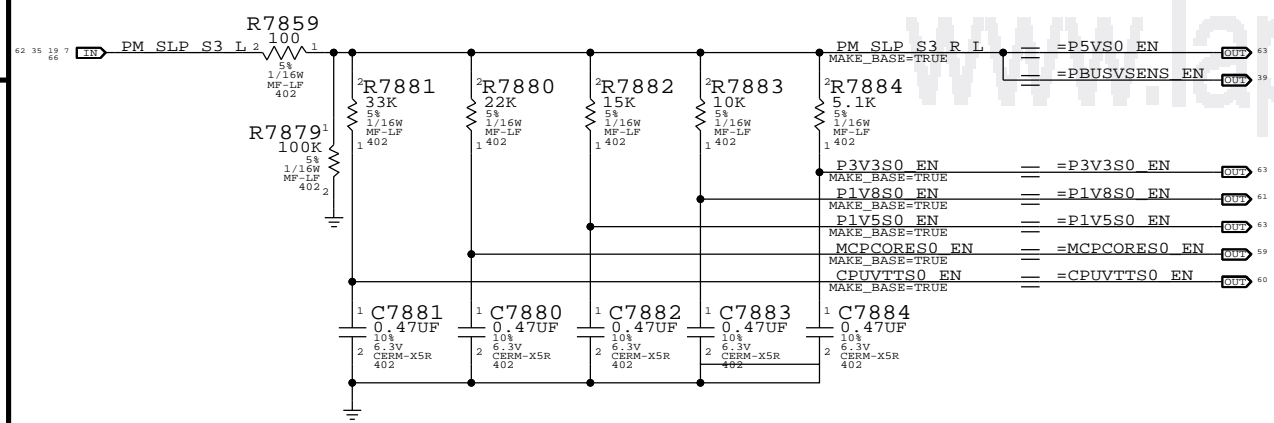
S3 Rail Enables



ENET Rail Enables



S0 Rail Enables



VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

Unused PGOOD signal



SYNC_MASTER=(T27_MLB) SYNC_DATE=(10/27/2009)

Power Sequencing

Apple Inc.

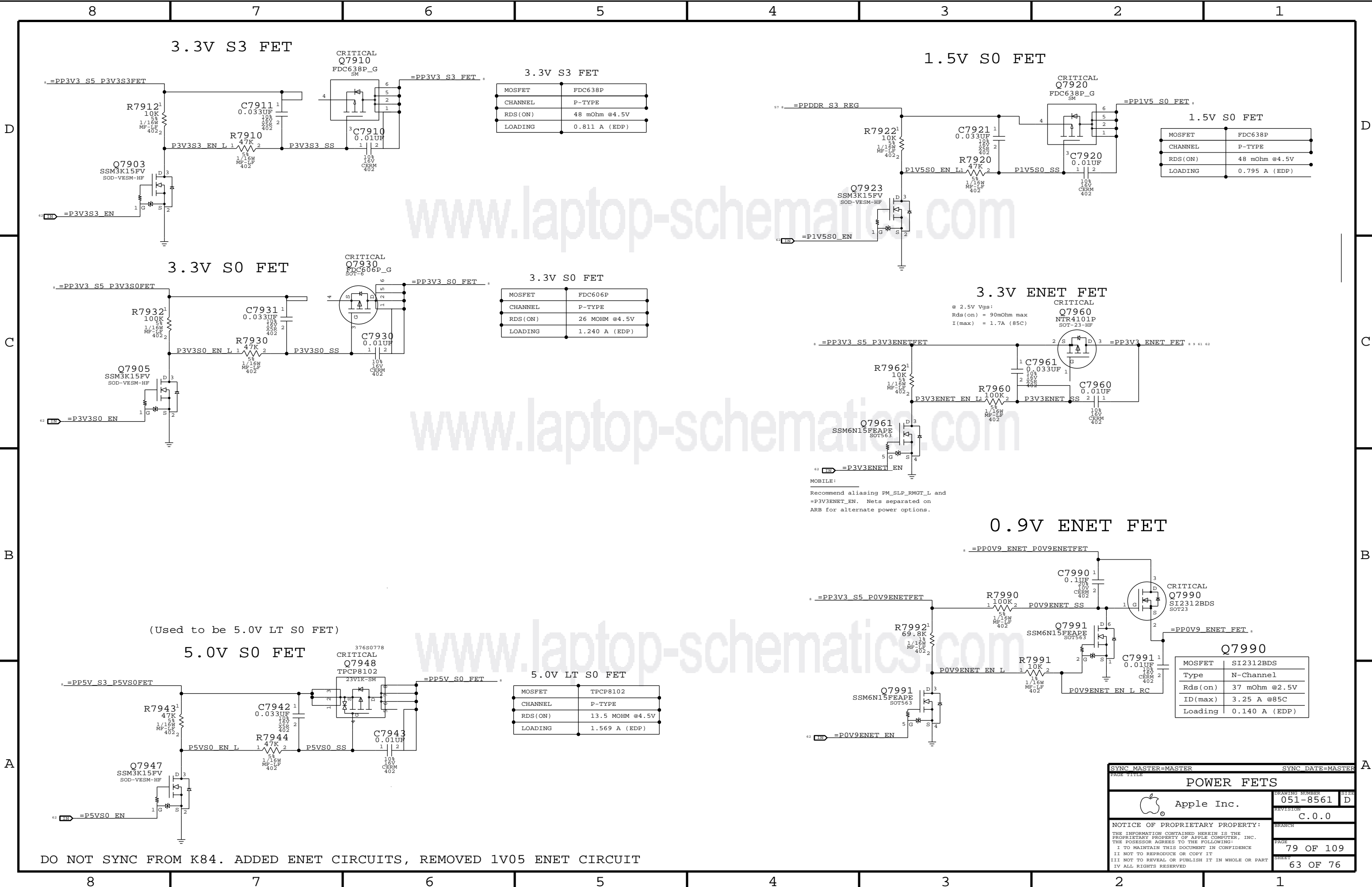
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REVISION: C.0.0

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PAGE: 78 OF 109 SHEET: 62 OF 76

DO NOT SYNC T27, ENET RAILS CHANGED



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3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.811 A (EDP)

1.5V S0 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.795 A (EDP)

3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.240 A (EDP)

3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL Q7960

MOSFET	NTR4101P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.795 A (EDP)

MOBILE:
Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

Q7990

MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

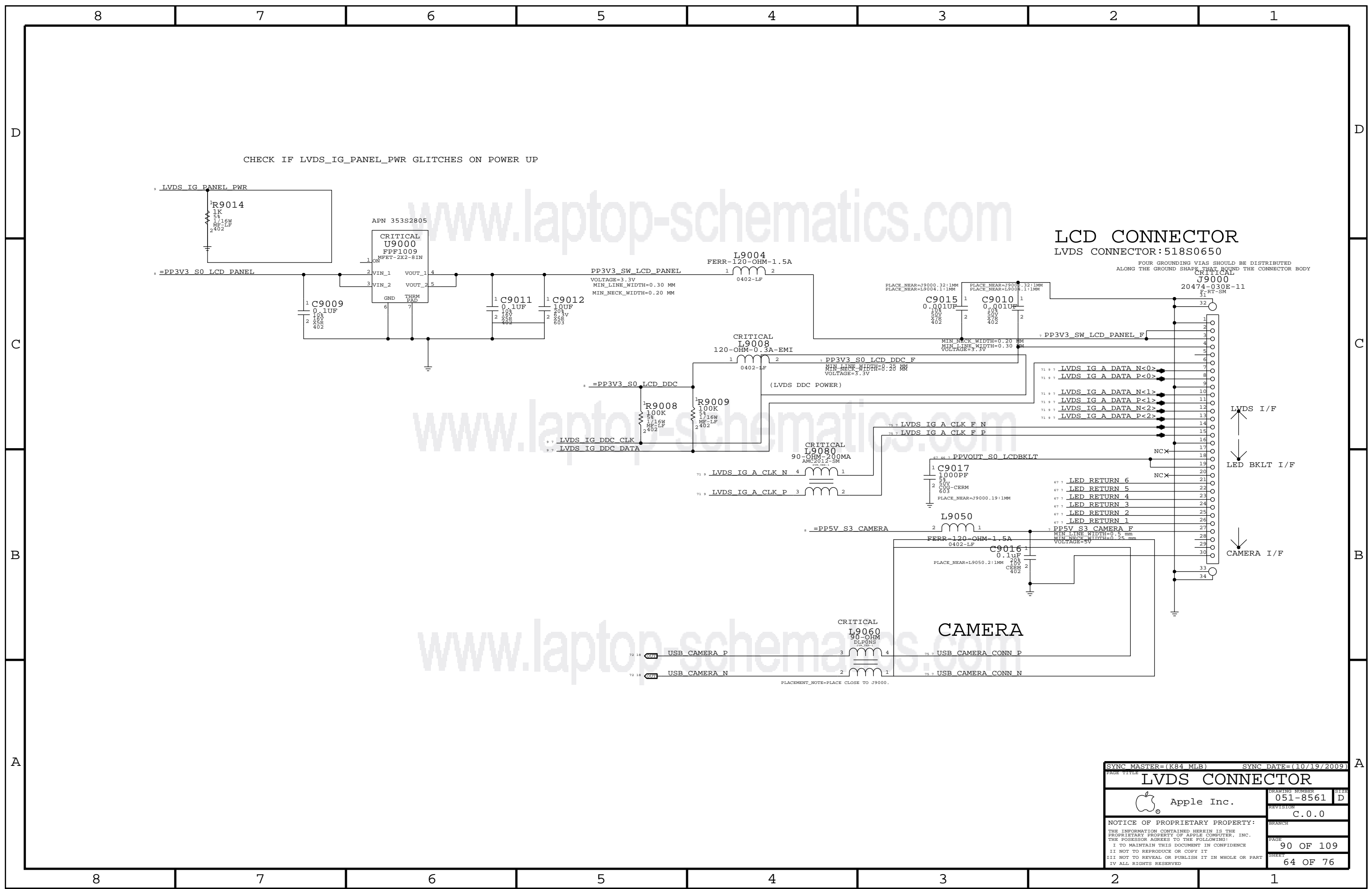
5.0V LT S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.569 A (EDP)

(Used to be 5.0V LT S0 FET)

SYNC MASTER=MASTER		SYNC DATE=MASTER	
POWER FETS			
Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		SHEET	63 OF 76

DO NOT SYNC FROM K84. ADDED ENET CIRCUITS, REMOVED 1V05 ENET CIRCUIT



CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

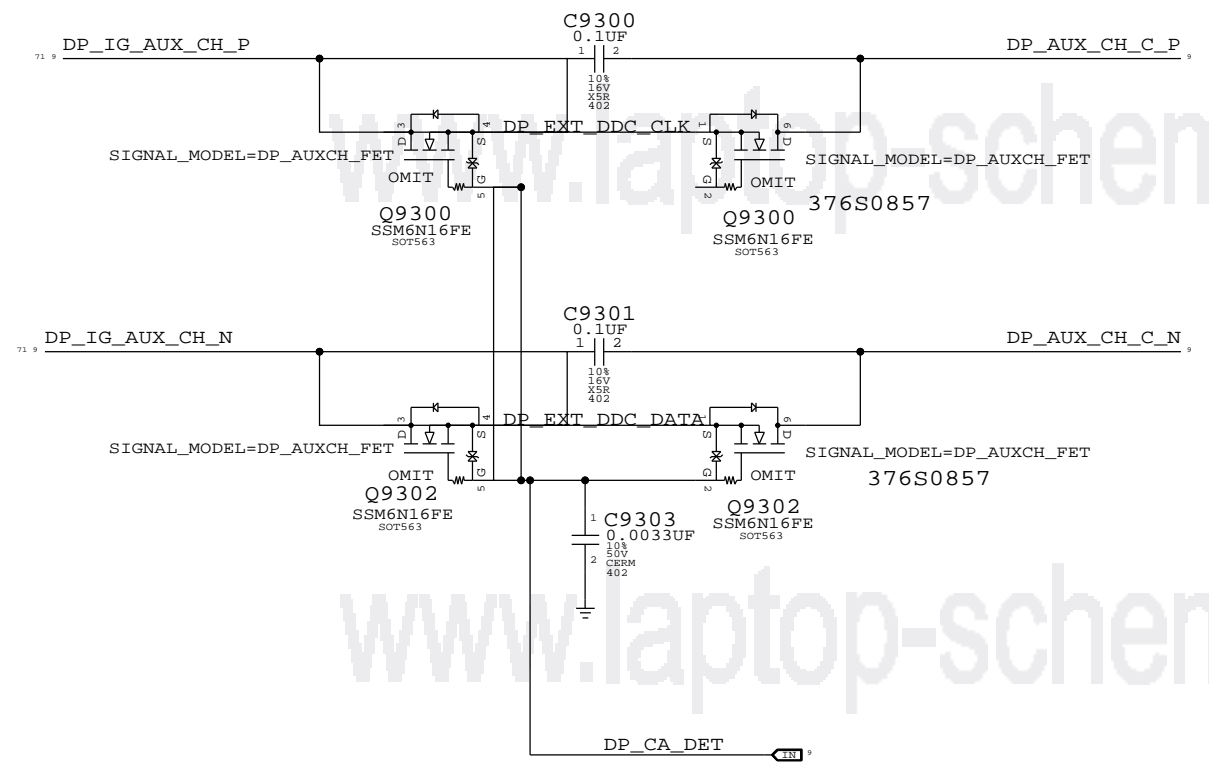
LCD CONNECTOR

LVDS CONNECTOR: 518S0650

FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY

↓ LVDS I/F
 ↓ LED BKLT I/F
 ↓ CAMERA I/F

SYNC MASTER=(K84 MLB)		SYNC DATE=(10/19/2009)	
LVDS CONNECTOR			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8561	D
		REVISION	
		C.0.0	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0859	2	XSTR, FT, N-CH, DUAL, SOT-563	Q9300, Q9302	CRITICAL	

SYNC MASTER=K6_MLB SYNC DATE=02/16/2010

DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

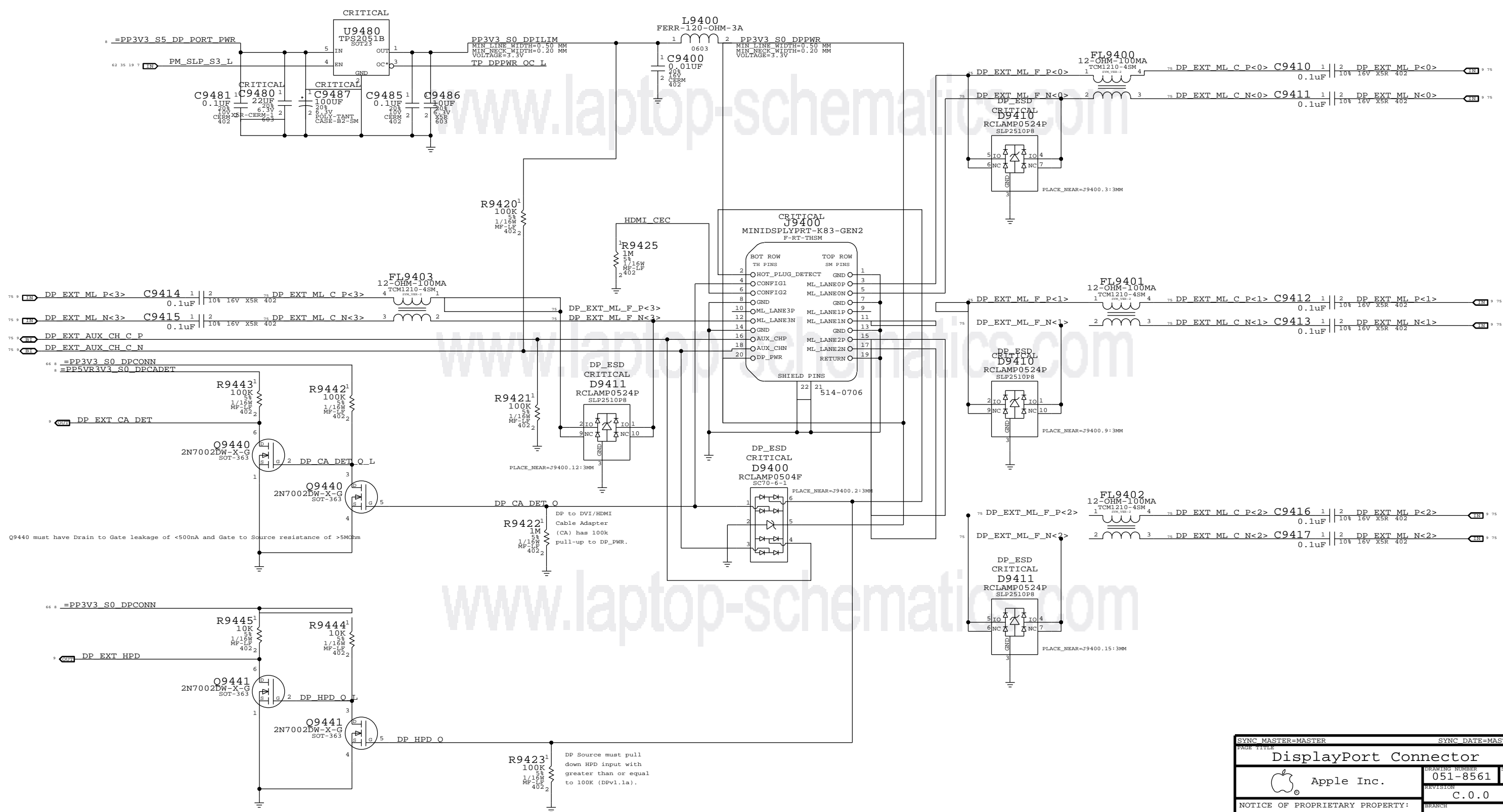
REVISION: C.0.0

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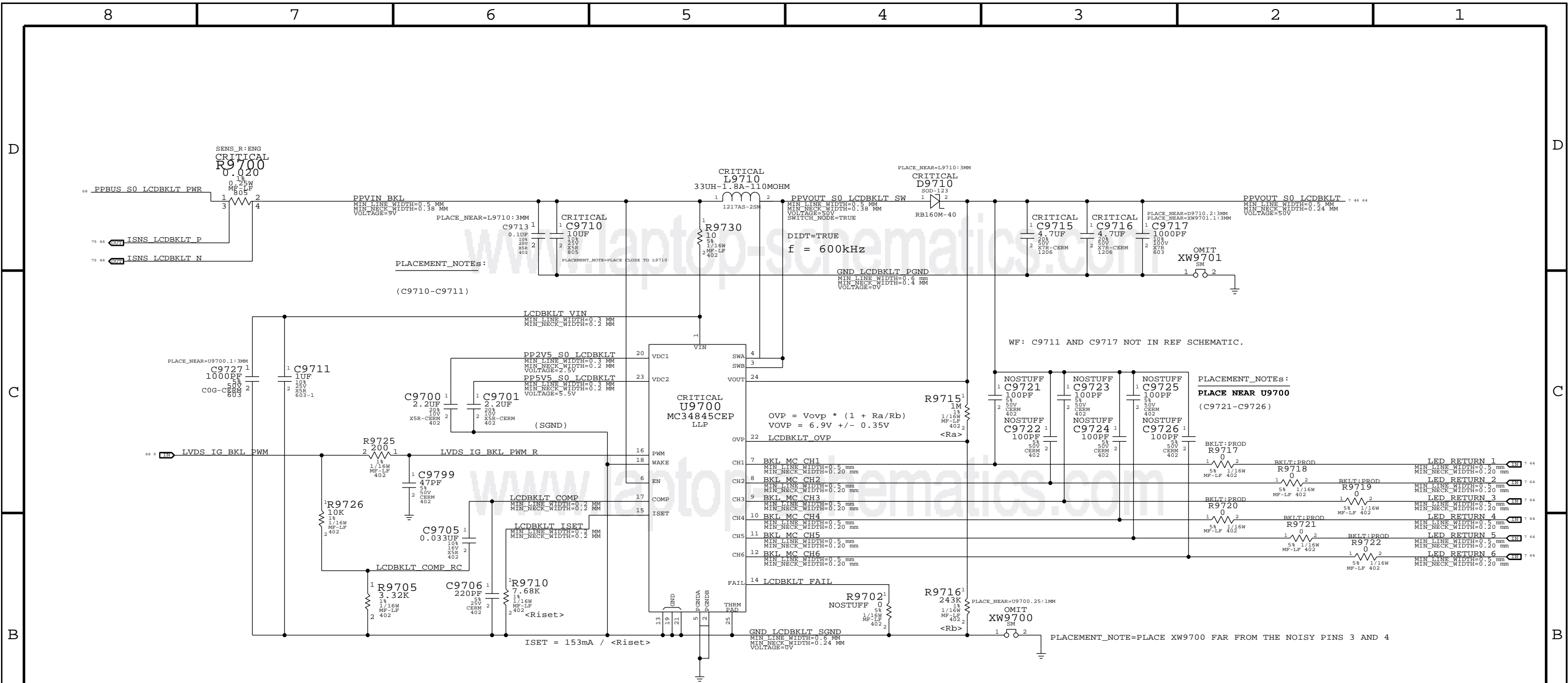
PAGE: 93 OF 109
 SHEET: 65 OF 76

Port Power Switch



DO NOT SYNC. K6 PAGE WITH K84 CONNECTOR

SYNC MASTER=MASTER		SYNC DATE=MASTER	
DisplayPort Connector			
Apple Inc.		DRAWING NUMBER	051-8561
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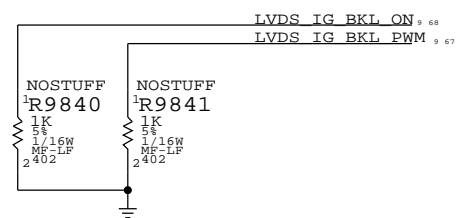
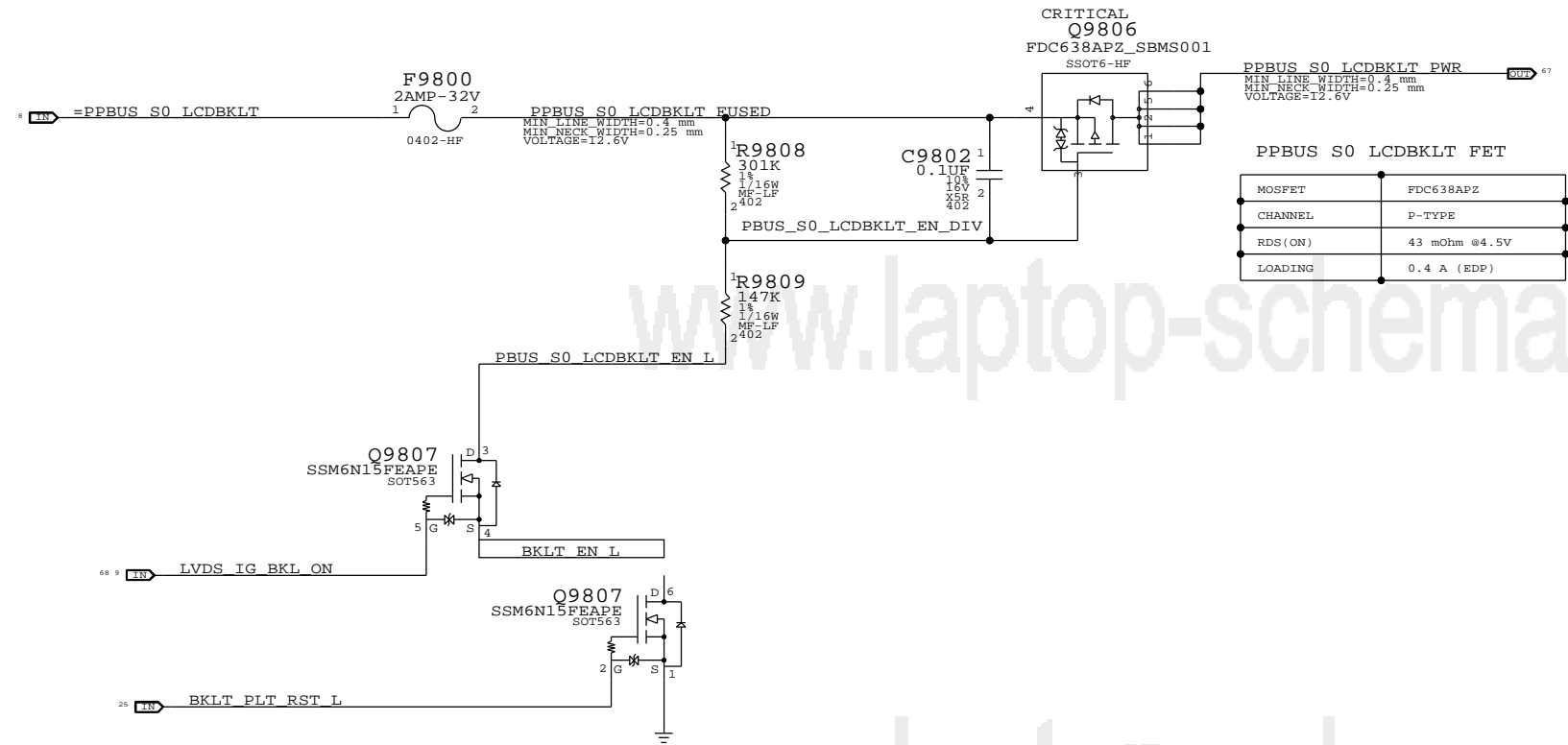
13.3 Inch, K84 Panel (9 LEDs per string)
 TARGET: ISET = 20mA, OVP = 35V
 ACTUAL: ISET = 19.9mA, OVP = 35.2V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0.402, SM	R9717, R9718, R9719		BKLT: PROD
103S0198	3	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0.402, SM	R9720, R9721, R9722		BKLT: ENG
101S0075	1	RES, MF, 0 OHM, 5%, 1/8W, SMD, LF, 0805	R9700		SENS_R: PROD

10.2 ohm resistors for current measurement on LED strings.

DO NOT SYNC FROM K84. L9710 CHANGED TO K6/K69

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE LCD Backlight Driver (MC34845)			
DRAWING NUMBER 051-8561		SIZE D	
REVISION C.0.0		BRANCH	
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MCP79 HAD INTERNAL 10K PULL-UP FOR THESE SIGNALS
MCP89 DRIVES THEM LOW

SYNC MASTER=(K84_MLB)		SYNC DATE=(10/19/2009)	
LCD Backlight Support			
Apple Inc.		DRAWING NUMBER	051-8561
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		PAGE	98 OF 109
		SHEET	68 OF 76

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCsense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE	UNIT
	PHYSICAL	SPACING			
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	7	14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	7	14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	7	14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	7	14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	7	14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	7	14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	7	14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	7	14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	7	14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	7	14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	7	14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	7	14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	7	14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	7	14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	7	14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	7	14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	7	14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	7	14
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	7	14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	7	14
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	7	14
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	7	14
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB BREQ0 L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	7	14
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	7	14
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	7	14
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	10	13
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10	14
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10	14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10	14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9	10
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	10	14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	10	14
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	10	14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	10	14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	10	14
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10	14
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10	13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	10	14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	10	14
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM THERMTRIP L	10	14
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	10	14
CPU_PROM_SB	CPU_50S	CPU_AGTL	CPU DPSLP L	10	14
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	10	14
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	10	14
FSB_CLK_CPUH	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10	14
FSB_CLK_CPUN	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10	14
FSB_CLK_ITP_P	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13	14
FSB_CLK_ITP_N	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13	14
FSB_CLK_MCP_P	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14	
FSB_CLK_MCP_N	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14	
CPU_IERR_L	CPU_50S		CPU IERR L	10	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	14	58
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	58	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14	
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10	29
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10	
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10	
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	10	33
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	10	33
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	10	33
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	10	33
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	10	33
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	10	33
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	10	33
(FSB_CPURST_I)	CPU_50S	CPU_ITP	XDP CPURST L	13	
	CPU_50S	CPU_8MIL	CPU VID<6..0>	11	58
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>	11	58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11	58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11	58
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	58	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	58	

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

CPU/FSB Constraints	
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PAGE 100 OF 109	SHEET 69 OF 76

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NV DG says 3x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 4x inner, 5x outer

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM*-style wildcards!
DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 CMD/CTRL signals should be matched within 150 ps.
 All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM A CKE<3..0>
MEM_A_CNVL	MEM_40S	MEM_CTRL	MEM A CS L<3..0>
MEM_A_CNVL	MEM_40S	MEM_CTRL	MEM A ODT<3..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DOS P<0>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DOS N<0>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DOS P<1>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DOS N<1>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DOS P<2>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DOS N<2>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DOS P<3>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DOS N<3>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DOS P<4>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DOS N<4>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DOS P<5>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DOS N<5>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DOS P<6>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DOS N<6>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DOS P<7>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DOS N<7>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM B CKE<3..0>
MEM_B_CNVL	MEM_40S	MEM_CTRL	MEM B CS L<3..0>
MEM_B_CNVL	MEM_40S	MEM_CTRL	MEM B ODT<3..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DOS P<0>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DOS N<0>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DOS P<1>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DOS N<1>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DOS P<2>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DOS N<2>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DOS P<3>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DOS N<3>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DOS P<4>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DOS N<4>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DOS P<5>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DOS N<5>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DOS P<6>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DOS N<6>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DOS P<7>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DOS N<7>
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND

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051-8561

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Memory Constraints

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101 OF 109

70 OF 76

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				
MCP_PEX_COMP	*	8 MIL	?				

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	*	20 MIL	?	CRT	CRT	*	CRT_2CRT
CRT_2CRT	*	15 MIL	?				
CRT_2CLK	*	50 MIL	?				
CRT_2SWITCHER	*	250 MIL	?				
CRT_SYNC	*	=4x_DIELECTRIC	?				
MCP_DAC_COMP	*	=2x_DIELECTRIC	?				

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?	SATA	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?				

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_90D	PCIE	PEG R2D P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C N<15..0>
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX0 TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP TV DAC RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP TV DAC VREF
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC P
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC N
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD P<5..0>
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD N<5..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP TMDS0 RSET
MCP_TMDS0_VPROBE			MCP TMDS0 VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C N
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMP		SATA_TERMP	MCP SATA TERMP

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MCP Constraints 1

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102 OF 109 SHEET 71 OF 76

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	19 35 37
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	19 35 37
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 35
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	25 37
USB_EXTN	USB_90D	USB	USB EXTN P	18 34
	USB_90D	USB	USB EXTN N	18 34
	USB_90D	USB	USB EXTN MUXED P	34 75
	USB_90D	USB	USB EXTN MUXED N	34 75
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXTD P	9 18
	USB_90D	USB	USB EXTD N	9 18
USB_CAMERA	USB_90D	USB	USB CAMERA P	18 64
	USB_90D	USB	USB CAMERA N	18 64
USB_BT	USB_90D	USB	USB BT P	18 30
	USB_90D	USB	USB BT N	18 30
USB_TPAD	USB_90D	USB	USB TPAD P	18 43
	USB_90D	USB	USB TPAD N	18 43
USB_IR	USB_90D	USB	USB IR P	9 18
	USB_90D	USB	USB IR N	9 18
USB_EXTR	USB_90D	USB	USB EXTB P	18 34
	USB_90D	USB	USB EXTB N	18 34
USB_T57	USB_90D	USB	USB T57 P	9 18
	USB_90D	USB	USB T57 N	9 18
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	9 18
	USB_90D	USB	USB SDCARD N	9 18
USB_WM	USB_90D	USB	USB WM P	9 18
	USB_90D	USB	USB WM N	9 18
MCP_USB_RBIA5	MCP_USB_RBIA5		MCP USB RBIA5 GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	13 19 38
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	13 19 38
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 38
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 38
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	19 48
	HDA_55S	HDA	HDA BIT CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	19 48
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST L	19 48
	HDA_55S	HDA	HDA RST L	19 48
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	19 48
	HDA_55S	HDA	HDA SDIN CODEC	48
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	19 48
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 35
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 37
	SPI_55S	SPI	SPI CLK	7 37
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 37
	SPI_55S	SPI	SPI MOSI	7 37
SPI_MISO	SPI_55S	SPI	SPI MISO	7 19 37
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 37
	SPI_55S	SPI	SPI CS0 L	7 37
	SPI_55S	SPI	SPI MLB CLK	37 47
	SPI_55S	SPI	SPI MLB MOSI	37 47
	SPI_55S	SPI	SPI MLB MISO	37 47
	SPI_55S	SPI	SPI MLB CS L	37 47
	SPI_55S	SPI	SPI ALT CLK	37
	SPI_55S	SPI	SPI ALT MOSI	37
	SPI_55S	SPI	SPI ALT MISO	37
	SPI_55S	SPI	SPI ALT CS L	37

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	-STANDARD	7.5 MIL	7.5 MIL	-STANDARD	-STANDARD	-STANDARD
ENET_MII_55S	*	-55_OHM_SE	-55_OHM_SE	-55_OHM_SE	-55_OHM_SE	-STANDARD	-STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_WFP0_CLK	*	-3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	-100_OHM_DIFF	-100_OHM_DIFF	-100_OHM_DIFF	-100_OHM_DIFF	-100_OHM_DIFF	-100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO
ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN L
	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK
	ENET_MII_55S	ENET_MII	ENET RXD R<3..0>
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<0>
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<3..1>
ENET_RXD	ENET_MII_55S	ENET_MII	ENET RX CTRL
	ENET_MII_55S	ENET_MII	ENET RXCTL R
	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK R
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET TXD<0>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TXD<3..1>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TX CTRL
	ENET_MII_55S	ENET_MII	ENET RESET L
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0>
	ENET_MDI_100D	ENET_MDI	ENET MDI TRAN P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET MDI TRAN N<3..0>

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8

7

6

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IT01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	7 38
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	7 38
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	38
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	38
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	38
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	38
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 38
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 38
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	38
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	38


SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P	55
	1T01_DIFFPAIR		CHGR_CSI_N	55
	1T01_DIFFPAIR		CHGR_CSI_R_P	55
	1T01_DIFFPAIR		CHGR_CSI_R_N	55
CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P	55
	1T01_DIFFPAIR		CHGR_CSO_N	55
	1T01_DIFFPAIR		CHGR_CSO_R_P	40 55
	1T01_DIFFPAIR		CHGR_CSO_R_N	40 55

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		PAGE	106 OF 109
		SHEET	74 OF 76

8

7

6

5

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	*	VERRIDE	VERRIDE	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MEM_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MII_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_USB_RBIA_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	*_OVERRIDE	VERRIDE	VERRIDE	0.25 MM_OVERRIDE	250 MIL_OVERRIDE	VERRIDE	VERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
(PCIE_AP)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP CONN P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP CONN N
(USB_EXT_A)	USR_90D	USR	USB EXT_A MUXED P
(USB_EXT_A)	USR_90D	USR	USB EXT_A MUXED N
(USB_EXT_A)	USR_90D	USR	USB LT1 P
(USB_EXT_A)	USR_90D	USR	USB LT1 N
(USB_TPAD)	USR_90D	USR	USB TPAD R P
(USB_TPAD)	USR_90D	USR	USB TPAD R N
(USB_CAMERA)	USR_90D	USR	USB CAMERA CONN P
(USB_CAMERA)	USR_90D	USR	USB CAMERA CONN N
	USR_90D	USR	USB LT2 P
	USR_90D	USR	USB LT2 N
	ENET_MDI_100D	ENETCONN	ENETCONN P<3..0>
	ENET_MDI_100D	ENETCONN	ENETCONN N<3..0>
	SATA_90D	SATA	SATA ODD R2D UF P
	SATA_90D	SATA	SATA ODD R2D UF N
	SATA_90D	SATA	SATA ODD D2R UF P
	SATA_90D	SATA	SATA ODD D2R UF N
	SATA_90D	SATA	SATA HDD D2R FILT P
	SATA_90D	SATA	SATA HDD D2R FILT N
	SATA_90D	SATA	SATA HDD D2R UF P
	SATA_90D	SATA	SATA HDD D2R UF N
	SATA_90D	SATA	SATA HDD R2D UF P
	SATA_90D	SATA	SATA HDD R2D UF N
	SATA_90D	SATA	SATA HDD D2R RDRV IN P
	SATA_90D	SATA	SATA HDD D2R RDRV IN N
	SATA_90D	SATA	SATA HDD R2D RDRV IN P
	SATA_90D	SATA	SATA HDD R2D RDRV IN N
	SATA_90D	SATA	SATA HDD D2R RDRV OUT P
	SATA_90D	SATA	SATA HDD D2R RDRV OUT N
	SATA_90D	SATA	SATA HDD R2D RDRV OUT P
	SATA_90D	SATA	SATA HDD R2D RDRV OUT N
	SATA_90D	SATA	SATA HDD D2R NORDRV P
	SATA_90D	SATA	SATA HDD R2D NORDRV P
	SATA_90D	SATA	SATA HDD R2D NORDRV N
	SATA_90D	SATA	SATA HDD R2D NORDRV N
PCIE_AP_D2R	PCIE_90D	PCIE	CONN PCIE MINI D2R P
PCIE_AP_D2R	PCIE_90D	PCIE	CONN PCIE MINI D2R N
PCIE_AP_R2D	PCIE_90D	PCIE	CONN PCIE MINI R2D P
PCIE_AP_R2D	PCIE_90D	PCIE	CONN PCIE MINI R2D N
USB_BT	USR_90D	USR	CONN USB2 BT P
USB_BT	USR_90D	USR	CONN USB2 BT N
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK F P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK F N
MCP_PEL_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN P
MCP_PEL_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN N
USB_EXT_A	USR_90D	USR	CONN USB EXT_A P
USB_EXT_A	USR_90D	USR	CONN USB EXT_A N
USB_EXTB	USR_90D	USR	CONN USB EXT_B P
USB_EXTB	USR_90D	USR	CONN USB EXT_B N

Power Net Properties


ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
CPUTHMSNS_D2	THERM_1T01_55S	THERM	CPUTHMSNS D1 P
CPUTHMSNS_D2	THERM_1T01_55S	THERM	CPUTHMSNS D1 N
CPUTHMSNS_D2	THERM_1T01_55S	THERM	CPUTHMSNS D2 P
CPUTHMSNS_D2	THERM_1T01_55S	THERM	CPUTHMSNS D2 N
CPU_THERMD	THERM_1T01_55S	THERM	CPU_THERMD P
CPU_THERMD	THERM_1T01_55S	THERM	CPU_THERMD N
MCPTHMSNS_D2	THERM_1T01_55S	THERM	MCPTHMSNS D2 P
MCPTHMSNS_D2	THERM_1T01_55S	THERM	MCPTHMSNS D2 N
MCP_THMDIODE	THERM_1T01_55S	THERM	MCP_THMDIODE P
MCP_THMDIODE	THERM_1T01_55S	THERM	MCP_THMDIODE N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS LV5 S3 P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS LV5 S3 R P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS LV5 S3 R N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS AIRPORT P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS AIRPORT N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS AIRPORT R P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS AIRPORT R N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS HDD P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS HDD N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS HDD R P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS HDD R N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT R P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT R N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS ODD P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS ODD N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS ODD R P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS ODD R N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS CPUVTT P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	ISNS CPUVTT N
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	MCPCORES0 VSEN P
SENSE_DIFFPATR	SENSE_1T01_55S	SENSE	MCPCORES0 VSEN N
	MEM_POWER		PP1V5R1V35 S3
	SR_POWER		PP3V3 S5
	SR_POWER		PP3V3 S0
	SR_POWER		PP1V5 S0
	GND		GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
	DIFFPATR	AUDIO	AUD_SPKRAMP LIN P
	DIFFPATR	AUDIO	AUD_SPKRAMP LIN N
	DIFFPATR	AUDIO	AUD_SPKRAMP SUBIN P
	DIFFPATR	AUDIO	AUD_SPKRAMP SUBIN N
	DIFFPATR	AUDIO	AUD_SPKRAMP RIN P
	DIFFPATR	AUDIO	AUD_SPKRAMP RIN N
	DIFFPATR	AUDIO	SSM2315L P
	DIFFPATR	AUDIO	SSM2315L N
	DIFFPATR	AUDIO	SSM2315S P
	DIFFPATR	AUDIO	SSM2315S N
	DIFFPATR	AUDIO	SSM2315R P
	DIFFPATR	AUDIO	SSM2315R N
SPK_OUT	DIFFPATR	AUDIO	SPKRCONN L OUT P
SPK_OUT	DIFFPATR	AUDIO	SPKRCONN L OUT N
SPK_OUT	DIFFPATR	AUDIO	SPKRCONN S OUT P
SPK_OUT	DIFFPATR	AUDIO	SPKRCONN S OUT N
SPK_OUT	DIFFPATR	AUDIO	SPKRCONN R OUT P
SPK_OUT	DIFFPATR	AUDIO	SPKRCONN R OUT N
	DIFFPATR	AUDIO	BI MIC P
	DIFFPATR	AUDIO	BI MIC N
	DIFFPATR	AUDIO	HS MIC P
	DIFFPATR	AUDIO	HS MIC N

GRAPHICS NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML N<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0>
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P
	DP_90D	DISPLAYPORT	DP EXT AUX CH C N
	DP_90D	DISPLAYPORT	DP EXT DDC DATA
	DP_90D	DISPLAYPORT	DP EXT DDC CLK

SYNC MASTER=MASTER		SYNC DATE=MASTER	
K87 SPECIFIC CONSTRAINTS			
 Apple Inc.		DRAWING NUMBER	051-8561
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K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, BOTTOM				NO_TYPE, BGA_P10M				MM	16.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
DEFAULT	*	Y	$+50_{\text{OHR_SE}}$	0.100MM	30 MM	0 MM	0 MM		
STANDARD	*	Y	-DEFAULT	-DEFAULT	12.7 MM	-DEFAULT	-DEFAULT		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
55_OHR_SE	TOP, BOTTOM	Y	0.590 MM	0.090 MM					
55_OHR_SE	*	Y	0.576 MM	0.076 MM	-STANDARD	-STANDARD	-STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
50_OHR_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM					
50_OHR_SE	*	Y	0.076 MM	0.076 MM	-STANDARD	-STANDARD	-STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
40_OHR_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM					
40_OHR_SE	*	Y	0.126 MM	0.100 MM	-STANDARD	-STANDARD	-STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
2704_OHR_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM					
2704_OHR_SE	*	Y	0.222 MM	0.222 MM	-STANDARD	-STANDARD	-STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
70_OHR_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD		
70_OHR_DIFF	103, 104, 109, 110, 111	Y	0.151 MM	0.100 MM	-STANDARD	0.234 MM	0.234 MM		
70_OHR_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
90_OHR_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD		
90_OHR_DIFF	103, 104, 109, 110, 111	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM		
90_OHR_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
100_OHR_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD		
100_OHR_DIFF	103, 104, 109, 110, 111	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM		
100_OHR_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
1:1_DIFFPAIR	*	Y	-STANDARD	-STANDARD	-STANDARD	0.1 MM	0.1 MM		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	-DEFAULT	?
BGA_P10M	*	-DEFAULT	?
BGA_P20M	*	-DEFAULT	?
BGA_P30M	*	-DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5K_DIELECTRIC	TOP, BOTTOM	0.105 MM	?
2K_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3K_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4K_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5K_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
1.5K_DIELECTRIC	*	0.095 MM	?
2K_DIELECTRIC	*	0.126 MM	?
3K_DIELECTRIC	*	0.189 MM	?
4K_DIELECTRIC	*	0.252 MM	?
5K_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P10M	BGA_P10M
MEM_CLK	*	BGA_P10M	BGA_P20M
CLK_PSB	*	BGA_P10M	BGA_P20M
CLK_LPC	*	BGA_P10M	BGA_P20M
CLK_PCIE	*	BGA_P10M	BGA_P20M
CLK_SLOW	*	BGA_P10M	BGA_P20M
FSB_D5TB	FSB_D5TB	BGA_P10M	BGA_P30M

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P10M	STANDARD

SYNC MASTER=MASTER		SYNC DATE=MASTER	
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		PAGE	109 OF 109
		SHEET	76 OF 76