1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000897412	PRODUCTION RELEASED	2010-04-26

SCHEM MLB_LDO K87

SCRATCHO

04/26/2010

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1	1	Table of Contents	NA	NA
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14	14	MCP CPU Interface	T27_MLB	02/16/2010
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17	17	MCP Graphics	T27_MLB	02/16/2010
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19	19	MCP HDA, LPC & MISC	T27_MLB	02/16/2010
20	20	MCP Power & Ground	T27_MLB	02/16/2010
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24	26	MCP Graphics Support	T27_MLB	02/16/2010
25	28	SB Misc	(T27_MLB)	(10/07/2009)
26	29	DDR3 SO-DIMM Connector A	T27_MLB	02/16/2010
27	31	DDR3 SO-DIMM Connector B	T27_MLB	02/16/2010
28	32	SO-DIMM Pinswaps	MASTER	MASTER
29	33	FSB/DDR3 Vref Margining	T27_MLB	02/16/2010
30	34	X16 WIRELESS CONNECTOR	MASTER	MASTER
31	37	Ethernet PHY (RTL8211CL)	MASTER	MASTER
32	39	ETHERNET CONNECTOR	MASTER	MASTER
33	45	SATA Connectors	MASTER	MASTER
34	46	External USB Connectors	(K84_MLB)	(10/03/2009)
35	49	SMC	T27_MLB	02/16/2010
36	50	SMC Support	(T27_MLB)	(10/27/2009)
37	51	LPC+SPI Debug Connector	(T27_MLB)	(12/15/2009)
38	52	K87 SMBus Connections	MASTER	MASTER

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39	53	Voltage Sensing	T27_MLB	02/16/2010
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45	59	SMS	MASTER	MASTER
46	60	DEBUG SENSORS AND ADC	MASTER	MASTER
47	61	SPI ROM	T27_MLB	02/16/2010
48	62	AUDIO: CODEC/REGULATOR	AUDIO	02/16/2010
49	63	AUDIO: LINE INPUT FILTER	AUDIO	02/16/2010
50	65	AUDIO: HEADPHONE FILTER	AUDIO	02/16/2010
51	66	AUDI0: SPEAKER AMP	AUDIO	02/16/2010
52	67	AUDIO: JACK	AUDIO	02/16/2010
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54	69	DC-In & Battery Connectors	MASTER	MASTER
55	70	PBus Supply & Battery Charger	(K6_MLB)	(11/06/2009)
56	72	5V/3.3V SUPPLY	(K6_MLB)	(10/27/2009)
57	73	1.5V/0.75V DDR3 SUPPLY	(K6_MLB)	(11/06/2009)
58	74	IMVP6 CPU VCore Regulator	(K84_MLB)	(11/18/2009)
59	75	MCP VCore Regulator	(K6_MLB)	(10/27/2009)
60	76	CPU VTT(1.05V) SUPPLY	(K84_MLB)	(02/04/2009)
61	77	Misc Power Supplies	MASTER	MASTER
62	78	Power Sequencing	(T27_MLB)	(10/27/2009)
63	79	POWER FETS	MASTER	MASTER
64	90	LVDS CONNECTOR	(K84_MLB)	(10/19/2009)
65	93	DISPLAYPORT SUPPORT	K6_MLB	02/16/2010
66	94	DisplayPort Connector	MASTER	MASTER
67	97	LCD Backlight Driver (MC34845)	MASTER	MASTER
68	98	LCD Backlight Support	(K84_MLB)	(10/19/2009)
69	100	CPU/FSB Constraints	T27_MLB	02/16/2010
70	101	Memory Constraints	T27_MLB	02/16/2010
71	102	MCP Constraints 1	T27_MLB	02/16/2010
72	103	MCP Constraints 2	T27_MLB	02/16/2010
73	104	Ethernet Constraints	MASTER	MASTER
74	106	SMC Constraints	T27_MLB	02/16/2010
75	108	K87 SPECIFIC CONSTRAINTS	MASTER	MASTER
76	109	K87 RULE DEFINITIONS	MASTER	MASTER

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8561	1	SCHEM,MLB_LDO,K87	SCH	CRITICAL	
820-2877	1	PCBF,MLB_LDO,K87	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB_LDO,SCRATCHO,K87

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DRAWING NUMBER: 051-8561 | SIZE: D

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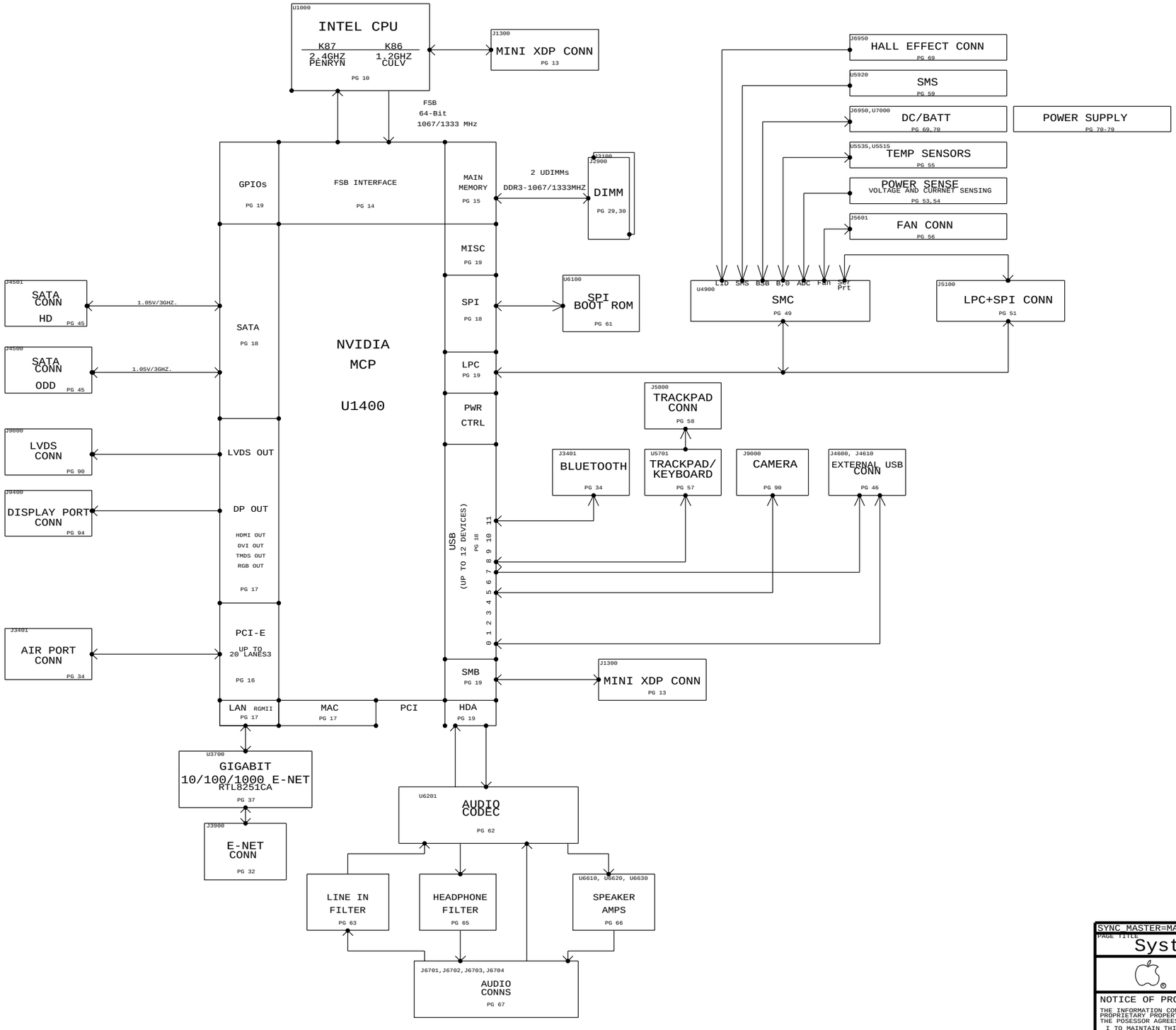

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

System Block Diagram

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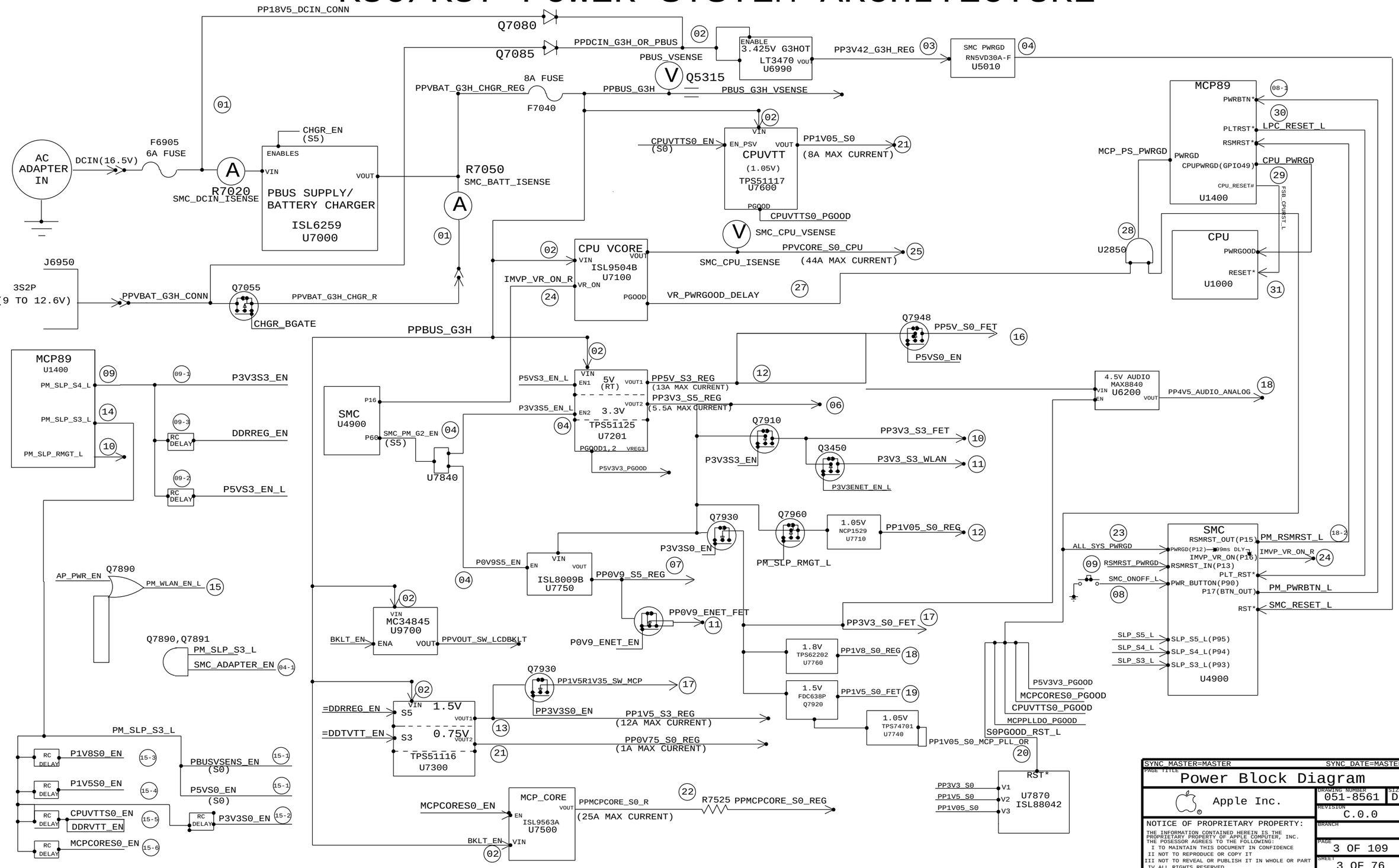
K86/K87 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1115	PCBA,MLB_LDO,FOXCONN,K87	K86_K87_COMMON,K87_SPECIFIC,FOX_DDR_CONN,EEEE:DD16
639-1116	PCBA,MLB_LDO,MOLEX,K87	K86_K87_COMMON,K87_SPECIFIC,MOLEX_DDR_CONN,EEEE:DD17
085-1799	K87 MLB_LDO DEVELOPMENT BOM	K86_K87_DEVELOPMENT_PVT

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1632	1	K87 MLB_LDO DEVELOPMENT BOM	DEVEL	CRITICAL	DEVELOPMENT_BOM

BOM Groups (always-present)

BOM GROUP	BOM OPTIONS
K86_K87_COMMON	K86_K87_COMMON1,PROJECT_PHASE:PROD,COMMON,ALTERNATE,BOOTROM:PROG,WELLSPRING:PROG,MCP_T_DIODE_SENSOR
K86_K87_COMMON1	DP_ESD,MIKEY,MCPPLL_R:REG,ENET1V05:INT,LED:K86_K87,S0PGOOD_BJT,ENET_ESD,VFRQ:SLPS3,SMC_DEBUG:YES,SPI:25MHZ,XDP,OLD_AUDIO_SWITCH
K87_SPECIFIC	CPU:2.4GHZ,IMVP6:2PHASE,SMC:PROG_K87,MCP89M:A02
K86_SPECIFIC	CPU:1.2GHZ,IMVP6:1PHASE,SMC:PROG_K86,MCP83M

BOM Groups (project phase-dependent)

BOM GROUP	BOM OPTIONS
PROJECT_PHASE:DEV	DEVELOPMENT_BOM
PROJECT_PHASE:PROD	K86_K87_DEBUG:PROD
K86_K87_DEVELOPMENT_ONLY	DEBUG_ADC,LPCPLUS_CON,S0PGOOD_ISL,EFI_DEBUG,MCPPLL_LDO,EXT1V05,XDP_CON,LPCPLUS
K86_K87_DEVELOPMENT_PVT	LPCPLUS_CON,XDP_CON,VREFMRGN:YES,LPCPLUS
K86_K87_DEBUG:DEV	VREFMRGN:YES,BMON:ENG,BKLT:ENG,SENS_R:ENG
K86_K87_DEBUG:PROD	VREFMRGN:NO,BMON:PROD,BKLT:PROD,SENS_R:PROD,MCPHVDD:P2V5,LDO:FIXED,HTOL_SENSE:YES

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3680	1	PDC,LGDZ,PRQ,2.40,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU:2.4GHZ
337S3792	1	CDC,SLGYW,PRQ,1.2,10W,800,R0,1M,BGA	U1000	CRITICAL	CPU:1.2GHZ
337S3797	1	IC,MCP89M-A01,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A01
337S3866	1	IC,MCP89M-A02,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A02
337S3876	1	IC,MCP83M-A02,31X31MM,BGA1168	U1400	CRITICAL	MCP83M
516S0706	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA	J3100	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SODIMM,P=0.6MM	J2900	CRITICAL	FOX_DDR_CONN
516S0790	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA	J3100	CRITICAL	MOLEX_DDR_CONN
516-0213	1	CONN,204P,SODIMM,P=0.6MM	J2900	CRITICAL	MOLEX_DDR_CONN
452-1708	4	SCR.M1.6X0.35X6.0,D4,HO.3,BLK,M97	SCREW1,SCREW2,SCREW3,SCREW4	CRITICAL	
870-1940	4	POGO PIN,MED,NOISE-IMPROVED,SILVER,K87	ZS0900,ZS0901,ZS0902,ZS0903	CRITICAL	
870-1940	3	POGO PIN,MED,NOISE-IMPROVED,SILVER,K87	ZS0908,ZS0909,ZS0911	CRITICAL	
870-1939	5	POGO PIN,TALL,NOISE-IMPROVED,SILVER,K87	ZS0904,ZS0905,ZS0906,ZS0907,ZS0910	CRITICAL	
870-1939	5	POGO PIN,TALL,NOISE-IMPROVED,SILVER,K87	ZS0912,ZS0913,ZS0914,ZS0915,ZS0919	CRITICAL	
870-1938	3	POGO PIN,THIN,NOISE-IMPROVED,SILVER,K87	ZS0917,ZS0918,ZS0916	CRITICAL	

353S2718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE
514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR
514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS
514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR
514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

Programmable Parts

LOCKED BOOTROM APN IS 341S24B8 (QL: old info?)

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0252	1	SUBASSY, IC, SMC, K87	U4900	CRITICAL	SMC:PROG_K87
341T0250	1	SUBASSY, IC, SMC, K86	U4900	CRITICAL	SMC:PROG_K86
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0251	1	SUBASSY, IC, BOOT ROM, K86/K87	U6100	CRITICAL	BOOTROM:PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING:BLANK
341S2677	1	IC,WELLSPRING CONTROLLER,K87	U5701	CRITICAL	WELLSPRING:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	DALE/VISHAY, MAGLAYERS AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
138S0603	138S0602		ALL	MURATA AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
353S2811	353S1832		ALL	NEW IMPROVED INTERSIL PART AS ALTERNATE
353S2988	353S2987		ALL	MICS36S AS ALTERNATE
376S0908	376S0634		ALL	TOSHIBA AS ALTERNATE
376S0907	376S0634		ALL	FAIRCHILD AS ALTERNATE
376S0912	376S0868		ALL	ONSEMI(NEW SPEC) AS ALTERNATE

Bar Code Labels / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD16]	CRITICAL	EEEE:DD16
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD17]	CRITICAL	EEEE:DD17
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD18]	CRITICAL	EEEE:DD18
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD19]	CRITICAL	EEEE:DD19

Part Substitutions (differences with K6/K69)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0125	1	RES,MTL FILM,1/16W,113 OHM,1,0402,SMD,LF	R5714		LED:K86_K87

K86/K87 BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC_MASTER=(K84_MLB) SYNC_DATE=(01/19/2009)

PAGE TITLE: BOM Configuration

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DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

10/1/2009:INTITIAL RELEASE 0.0.1
- ALL PAGES SYNC'ED FROM K94
- REPLACED K94 MCP AND CPU PAGES WITH K6 PAGES
- UPDATED SCHEMATIC AND PCB PART NUMBER INFO

2009-12-03: Proto 0 release 1.0.0

2009-12-04: 1.1.0
csa 3: Updated CPU block text to include CPU description for both K86 and K87
csa 3: Updated text note to include "K86" in title
csa 4: Added BOM entry under Module Parts table to include CULV processor (337S3779) to minimize delta on this page between K86 and K87 per Diana

2009-12-07: 1.2.0
csa 74: Component value changes per Leo (Intersil):
R7417 from 5.36k => 6.34k, 1% (114S0296)
C7434 from 0.12uF => 0.022uF, 10% (132S0102)
Implemented different stuffing options for 1-phase vs 2-phase:
Added IMVP6:2PHASE to the following components:
R7417, C7428, R7409, R7411, C7406, R7414, C7414, C7413
Added BOM table to insert the following APNs for IMVP6:1PHASE:
R7417 = 7.68k 1% (114S0304)
C7428 = 0.22uF 10% (132S0192)
R7409 = 1.58k 1% (114S0236)
R7411 = 255 1% (114S0160)
C7406 = 470pF 10% (132S4720)
R7414 = 97.6k 1% (114S0410)
C7414 = 1000pF 10% (132S0045)
C7413 = 100pF 5% (131S1027)
Updated table to add new values for 1phase (PWM freq., Max current, Load line)

STILL NEED TO UPDATE VALUE OF C7428!

2009-12-08: 1.3.0
csa 45: Added passive deemphasis to SATA_HDD_D2R lines:
Added R4585, R4586 (5.1 ohm, 1%, 114S0093) and OMITted
Added C4585, C4586 (10pF, 5%, 131S0029) and NOSTUFFed
Added BOM table to stuff 0-ohms until we get go-ahead for filter

2009-12-08: 1.4.0
csa 8: Deleted net properties for the following nets:
=PP3V3_S0_CPUVTTISNS'
=PP5V_S0_HDD'
=PP5V_S0_MCPREG'
=PP1V05_S0_MCP_AVDD_UF'
=PPSPD_S0_MEM_B'
=PP3V3_S0_PWRCTL'
=PP3V3_S0_DPCONN'
Deleted net properties for =PP3V3_S3_WLAN
csa 74: Changed C7434 from NOSTUFF to IMVP6:2PHASE per Intersil
Added IMVP6:2PHASE to R7413 per Intersil
Changed C7428 from 0.47uF => 0.33uF (132S0101) per Intersil
Changed component color to Green
Cosmetic cleanup
csa 90: Deleted net properties for =PP5V_S3_CAMERA
csa 98: Deleted net properties for =PPBUS_S0_LCDBKLT
csa 108: Added NET_PHYSICAL property to SATA_HDD_D2R_FILT_P and _N

2009-12-09: 1.5.0
multiple: Added parentheses for SYNC_DATE property on all pages that have broken sync.
csa 4: Deleted entry in Module Parts table for R6612, R6617, R6630, R6633 since they were removed when we switched from piezo to dynamic speakers
csa 69: Changed J6955 symbol to K87 Hall effect assembly (339S0114)

2009-12-10: 1.6.0
csa 69: Added OMIT to J6955, BOM table to stuff K84 Hall effect connector

2009-12-11: 1.7.0
csa 45: Added PLACEMENT_NOTE for passive deemphasis circuit.
csa 74: Changed 1PHASE BOM table to correctly call out 132S0080 (0.22uF) instead of 0.022uF

2009-12-16: 1.8.0
*** Resynced all synced pages and picked up the following (change notes from T27):
csa 18: T27: Swapped USB_EXTB and USB_EXTD for NVRN-612340 (pg. 18). <radar:7416825> Ensure USB_EXTB is on ports 8-11 (NVRN-612340)
T27: Changed USB_RBIAS from 931-ohms to 887-ohms per DG v1.3 (pg. 18). <radar:7459260> Design Guide v1.3 updates
csa 20: T27: Added CKPLUS_WAIVE properties to dismiss false errors (pg. 20). <radar:7368529> TASK: Waive false CheckPlus errors
*** Started syncing the following pages:
csa 29,31: Began syncing from T27 per <radar:7424246 > BOM: K87 needs omit on J3100 and J2900 from T27
T27: Added BOMOPTIONs and APNs for Foxconn and Molex SO-DIMM connectors (pg. 29, 31).
csa 54: Began syncing from T27 per <radar:7432091 > BATT_ISENSE filter change to address lower max sink current on ISL6259 BMON pin (K17 auto-shutdown issue)
C5490 changed from CAP_402-0.022UF-10%-16V-CERM-X5R to CAP_402-0.022UF-20%-16V-CERM
T27: Added CKPLUS_WAIVE properties to dismiss false errors (pg. 54).
T27: Added gain note for US402 and SMC_BATT_ISENSE (pg. 54).
T27: Changed RC balance on BATT_ISENSE, same time constant (pg. 54).
csa 57: Began syncing from T27 per <radar:7304029 > T27 schematic bom option for R5714 & R5030 to keep K87 in sync
R5714 has BOMOPTION:LED:K6_K69, and we need to substitute a different part on csa 4
*** Made the following changes to follow T27 on the following unsynced pages :
csa 25: T27: Removed R2575 & R2580 per DG v1.3 (pg. 25). per <radar:7459260 > Design Guide v1.3 updates
*** Other changes
csa 4: Added BOM table to substitute in parts that have BOMOPTION xxx:K6_K69 (to allow sync with T27)
Added R5714 (114S0125) to table with BOMOPTION:LED:K86_K87

2009-12-17: 1.9.0
csa 4: Added BOM table entry for MCP89-A02 per <radar:7416858 > Task: Get part numbers for A02 rev.
Changed K87 MCP BOM group to call out MCP89-A02
csa 34: Changed U3440 from AP802 part to AP816 (343S0511) per <radar:7459498> BOM: APN updates for FPF1009 and SAK parts
Changed R3454 to 100k, 1% (114S0411) to match T27 and K69
Updated DLY text note for U3440 to match T27
Changed R3440 color to green, deleted WF text note about needing PU
csa 72: Changed L7220 from 152S0693 to 152S0778 per <rdar://problem/7347216> K69 L7260 combo footprint
Alternates table on csa 4 already has 152S0778 as alternate to 152S0693

2009-12-22: 1.10.0
csa 4: Per <rdar://problem/7473229> K86: Move to MCP83
Added BOM table entry for MCP83M (337S3876)
This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86
BOMOPTION is "MCP83M"
Per <rdar://problem/7495072> K87: Call out LED:K86_K87 BOMOPTION in the K87_MISC BOM group
Added LED:K86_K87 BOMOPTION to the K87_MISC BOM group
Per <rdar://problem/7495116> K87: remove ON Semi alternate for Q2300 (376S0624)
Removed table entry that says 376S0868 is an alternate for 376S0624
Per <rdar://problem/7495021> K86/K87: Replace "S" APNs with "T" APNs for programmed SMC and BR
Changed BOOTROM:PROG to call out 341T0251 (SUBASSY, IC, BOOT ROM, K86/K87)
Created SMC:PROG_K87 pointing to 341T0252 (SUBASSY, IC, SMC, K87)
Created SMC:PROG_K86 pointing to 341T0250 (SUBASSY, IC, SMC, K86)
Changed K87.PROGPARTS BOM group to point to SMC:PROG_K87
csa 69: Per <rdar://problem/7494087> K87: remove OMIT from J6955 and delete BOM table
Deleted BOM table for Hall effect assembly
Changed text note to say "HALL EFFECT ASSEMBLY"
Deleted OMIT BOMOPTION from J6955
Added text note with part numbers for components of the assembly
"Assembly APN: 339S0114
- BOM: 639-0680
- PCB#: 820-2801
- MCO: 056-3515.
- Conn APN:51850788"
csa 74: Cosmetic change, moved R7413, C7406 BOMOPTION label so they don't look like wire name
csa 78: Per <rdar://problem/7495000> K87: Add NOSTUFF to R7872 to disconnect U7870 from ALL_SYS_PWRGD
Changed BOMOPTION for R7872 from S0PGOOD_ISL to NOSTUFF

2010-01-06: 1.11.0
csa 7: Per <rdar://problem/7517432> K86/K87 functional net property needed on signals in schematics
Added the following functional test points under the J5100 LPC+SPI CONN FUNC_TEST group
LPCPLUS_GPIO
LPC_SERIRQ
SMC_TMS

2010-01-07: 1.12.0
csa 23: *** BROKE SYNC WITH T27
Per <rdar://problem/7519025> K86/K87: update all instances of 376S0786 schematic symbols
Updated Q2355 and Q2356 with new schematic symbols
Need to resync with T27 once the change has been made there
csa 70: Per <rdar://problem/7519048> K86/K87: Change U7000 to 353S2929
Changed U7000 from 353S2392 to 353S2929
Updated APN text note

2010-01-08: 2.0.0
csa 45: Per <rdar://problem/7524364> K86/K87: change SATA HDD D2R passive EQ values
Removed NOSTUFF from C4585, C4586
Removed OMIT from R4585, R4586
Deleted BOM table that stuffsdel the bypass option
Changed R4585, R4586 to 114S0065 (27.4 ohm, 1%)
Changed C4585, C4586 to 131S4713 (47pF, 5%)

2010-01-13: 2.1.0
csa 4: Per <rdar://problem/7540383> K86: Update CPU part number to 337S3792
Changed U1000 CPU:1.2GHz BOMOPTION from 337S3779 to 337S3792

2010-01-13: 2.2.0
csa 4: Cosmetic: changed text sizes and alignment
Per <rdar://problem/7540522> K86/K87: Production Debug Components
Changed 085-1093 to call out K87_DEVEL_PVT instead of K87_DEVEL_ENG
Changed K87_COMMON to call out K87_DEBUG_PVT instead of K87_DEBUG_ENG
Diff from the two changes above:
Toggled:
VREFMRGN:YES ==> VREFMRGN:NO
BMON:ENG ==> BMON:PROD
BKLT:ENG ==> BKLT:PROD
SENS_R:ENG ==> SENS_R:PROD
Removed:
DEBUG_ADC, S0PGOOD_ISL, EFI_DEBUG, MCPPLL_LDO, EXT1V05, MCP_T_DIODE_SENSOR, XDP_CON
Unchanged:
LPCPLUS, DEVEL_BOM, SMC_DEBUG:YES, XDP
Added LPCPLUS_CON to K87_DEVEL_ENG (does not change BOM for DVT)
Changed all instances of K87_DEBUG_xxxx to to K87_DEBUG:xxxx
Changed all instances of K87_DEVEL_xxxx to K87_DEVEL:xxxx
csa 51: (Per <rdar://problem/7540522> K86/K87: Production Debug Components)
Changed J5100 BOMOPTION from LPCPLUS to LPCPLUS_CON to unstuff connector at DVT

2010-01-15: 2.3.0
csa 74: Per <rdar://7525313 > K86 CPU loadline, OCP update
Keeping K86 and K87 pgs identical for CSA 74, modifying BOM table for IMVP 1 phase on K87's schematic to reflect changes for K86.
IMVP6:1PHASE BOM Table:
R7417 changed to 7.87K (APN 114S0305)
R7416 added to BOM Table, 16.9K, (APN 114S0336)
Added IMVP6:2PHASE BOM option to R7416 for K87's 13.7K
csa 74, csa 79: Per <rdar://7542674 > K86/K87 Text note change
Cleaned up text notes for 1phase, 2phase, and edp #s per radar request.

2010-01-18: 2.4.0
csa 4: Per <rdar://problem/7549122> K86/K87: Switch to new BOM group structure
Reverted back to ENG BOM, no longer PROD BOM (i.e. reverted much of 2.2.0 changes)
Changed BOM group structure to match that in the radar (see PDF attached to radar)
Net change was to move LPCPLUS to the 639 (from the 085)
Switching from Engineering to Production BOM should only require changing PROJECT_PHASE:DEV to PROJECT_PHASE:PROD
Per <rdar://problem/7544629> K86/K87: Update MCP83 description on csa 4
Changed description for 337S3876 to "IC,MCP83M-A02,31X31MM,BGA116A"
csa 23: Per <rdar://problem/7544657> K86/K87: Fix schematic symbol for Q2355, Q2356
*** Started syncing with K6
Syncing with K6 to pick up new symbols for Q2355 and Q2356
Should switch syncing back to T27 once it is updated there
csa 37: Per <rdar://problem/7548726> K86/K87 Ethernet series R's need to be 0 ohmed
Changed R3790-R3795 to 116S0004 (0-ohm, 0402) from 22-ohm

2010-01-19: 2.5.0
csa 37: Per <rdar://problem/7554342> K86/K87: Change L3720 to 152S1182
Changed L3720 to 152S1182 (IND,PWR,SHD,4.7UH,20%,0.91A,31X31X12MM) for lower ESR

2010-01-22: 2.6.0
csa 4: Per <rdar://problem/7571786> K86/K87: Add E3T EEE code for K86 to schematic
Added row to EEE table for E3T
Changed BOMOPTIONs to be mutually exclusive (changed "_" to ":")

2010-01-29: 2.7.0
*** Resynced with T27 and K6 (no differences)
*** Resynced Audio pages with the following changes:
-pg. 62, Changed R6211 to 22 Ohms
-pg. 66, added C6602
-pg. 67, no stuffed R6712 and R6713
csa 45: Per <rdar://problem/7561001> K87:EMC: Radiated Emissions: Right Audio emissions fail
Changed L4530, L4531 (APN 155S0137) to SIL connector pins
csa 97: Per <rdar://problem/7589365> K86/K87: Compensation settings change to provide more phase margin, reduce ripple
Changed R9726 from 22k to 10k (114S0315), and removed NOSTUFF
Changed C9705 from 8.2nF to 33nF (132S0131)
Changed C9706 from 120pF to 220pF (131S2225)

2010-02-02: 2.8.0
*** Resynced with T27 and K6 (no differences)
*** Resynced Audio pages with the following changes:
-pg. 67, added BOM options for U6700, R6712, and R6713 to support MAX14560 and MAX14504
csa 97: Changed R9710 from 7.32K 0402 1% to 7.68K (APN 114S0304) to support old K84 panel
csa 4: Added OLD_AUDIO_SWITCH BOM OPTION to K86_K87_COMMON1

2010-02-15: 2.9.0
2010-02-15: 2.10.0
csa 54: Broke sync with T27. Per <rdar://problem/7605797> K69/K86/K87 sensor IN1C unreliable
U5400 changed from OPA348 to OPA330. C5434 changed to NOSTUFF

2010-02-16: 2.11.0
Resync with T27 and K6. Clean up and rerelease schematic.

2010-02-18: 2.12.0
Per <rdar://7644836> K87 power component update
CSA 74: R7417 changed to 5.90K, C7428 changed to 0.47uF, C7434 changed to 0.033uF
CSA 75: R7572 changed to 147k.
CSA 70: R7015 changed to 56.2K, C7015 changed to 1000pF, C7042 changed to 0.068uF

Per <rdar://7634730> K86/K87: add an RC on the LVDS_IG_BKL_PWM
CSA 97: R9725 changed to 200ohm, C9799 of 47pF added. R9726.1 connection moved to LVDS_IG_BKLPWM

2010-02-18: 2.16.0
Per <rdar://7676934> K86/K87: Hall eff documentation change. Substitute 607-6831 for doc purposes
CSA 69: J6955 BOMOPTION change to OMIT. Added BOM table with 607-6831 for J6955

Per <rdar://7488543> K86/K86 Task: Measure each Power supply in MLB
CSA 74: For K86 only: C7434 = 0.1uF added. R7417 changed to 8.25kohm
CSA 12: For K86 only: C1272 = 330uF added.

Per <rdar://7685202> K86/K87 schematic: change U9700 to 353S2965 for Freescale backlight issue
CSA 97: U9700 changed to APN 353S2965

2010-02-18: 2.17.0
Per <rdar://7696179> K86/K87 schematic: Change audio jack part number for new connector cap
CSA 67: J6700 changed from APN 514-0718 to 514-0750

2010-02-25: 2.18.0
Per <rdar://7685811> K86/K87 schematic: add additional 639 for differentiation between Foxconn and Molex_DIMM connectors
CSA 4: MOLEX_DDR_CONN added to Module Parts, removed from Alternate table. Added second 639 and EEEE # to BOM table

2010-02-25: 2.19.0 2.20.0
Per <rdar://7678515> K87:EMC:ESD: System hangs on air/contact discharge to MPM connector
CSA 69: C6970, C6971, C6972 of 1000pF (APN 131S0222) added

2010-02-26: 2.21.0
Per <rdar://7488543> K87/K86 Task Measure each power supply in mlb.
CSA 12: C1200, C1204, C1207, C1209, C1211, C1219, C1202, C1216 NOSTUFFED
CSA 12: Added matching 0603 caps (APN 138S0635). Components C1230, C1231, C1232, C1233, C1234, C1235, C1236, C1237.
CSA 74: Changed C7434 from 0.033uF to 0.047uF (APN 132S0189) per Liang

2010-03-04: B.0.0
Per <rdar://7683852> K87 Proto1: 5 of 6 systems failing graphics noise (Underwater) acoustic spec by up to 3.1dB
CSA 12: C1233, C1230, C1237, C1234 changed from NOSTUFF to STUFFED.

** MLB_LDO branch

2010-03-09: 0.8.0
Summary of changes for MLB_LDO:
CSA 25: U2590 added, APN 353S2971. R2592 of 10K and C2592 of 1UF, C2593 of 1UF added.
Nets MCP_PLL_LDO_EN and PP3V3_S0_LDO_R added.

2010-03-22: A.1.0
CSA 25: Copied from K6
Added C2599, R2597, R2596, U2593, Q2592, R2599, C2594, U2594, R2598, C2598 with BOMOPTION HTOL_SENSE:YES
Added R2594 and R2591 with LDO:ADJ BOMOPTION
Changed BOMOPTION names from LDO:YES and LDO:NO to MCPHVDD:P2V5 and MCPHVDD:P3V3
Added BOM TABLE with LDO:FIXED, LDO:ADJ, and HTOL_SENSE:NO stuffing options
CSA 50: Removed SMC alias to TP for SMC_NB_MISC_ISENSE to enable sense circuitry connection to SMC
Removed SMC_P10 alias to TP_SMC_P10
CSA 8: Added =PP3V42_G3H_OPA330 alias to power U2594
Added =PP3V3_S0_OPA330 alias to power U2593
CSA 4: Added MCPHVDD:P2V5, LDO:FIXED, HTOL_SENSE:YES to BOM Group K86_K87_DEBUG:PROD

2010-03-22: A.2.0
Per <rdar://7703507> K87: Add cap to DDC line to avoid DDC line glitch issue
CSA 93: Added C9303 3300pF cap on DP_CA_DET.
CSA 25: Changed U2594 power to 3V3_S0 from 3V42_G3H.

2010-03-22: A.3.0
CSA 77: Deleted U7740 1.05V LDO circuit to free space for U2592 and current mirror circuit.

2010-03-22: A.4.0
Reverted the changes and synced back to A.0.0
Per <rdar://7703507> K87: Add cap to DDC line to avoid DDC line glitch issue
CSA 93: Added C9303 3300pF cap on DP_CA_DET.

2010-03-22: A.5.0
CSA 25: Added R2591,R2594 for LDO:ADJ option. Changed U2592 to LDO:FIXED option.
CSA 4: Added Alternate part for U2592 LDO. 353S2987(TI), 353S2988(Micrel) to 353S2986(Intersil).
LDO:FIXED, MCPHVDD:P2V5 added in bom table.

2010-03-30: A.7.0
Reverted the changes and synced back to A.2.0.
CSA 4: Added Alternate part for U2592 LDO. 353S2987(TI), 353S2988(Micrel) to 353S2986(Intersil).
LDO:FIXED, MCPHVDD:P2V5 added in bom table.

2010-03-31: A.8.0
CSA 25,49,50: Changed Q2592 gate control pin to SMC_P24 from SMC_P10.

2010-04-1: A.9.0
CSA 25: Added R2600 0ohm resistor to help layout change.

2010-04-1: A.10.0
CSA 25: Changed R2600 refdes to R2550 to match with page#.

2010-04-14: B.0.0
rdar://7822714
CSA 69: R6905 kept same 1ohm.
C6900 changed to 2.2uF. 138S0592.
CSA 4: Devel BOM# changed to 085-1799. And BOM OPTIONS to K86_K87_DEVELOPMENT_PVT.
Removed Intersil LDO(353S2986).

2010-04-14: C.0.0
CSA 4: Added Toshiba(376S0908), Fairchild(376S0907) as an alternate to 376S0634.
Added ONsemi new spec part(376S0912) as an alternate to Q2300(376S0868).

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Functional Test Points

FAN CONNECTORS FUNC_TEST

J12	TRUE	PP5V_S0	7 8 62
J15	TRUE	FAN_RT_PWM	42
J16	TRUE	FAN_RT_TACH	42

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

J231	TRUE	BI_MIC_N	52 53 75
J232	TRUE	BI_MIC_P	52 53 75
J230	TRUE	BI_MIC_SHIELD	52 53

SPEAKER FUNC_TEST

J227	TRUE	SPKRAMP_L_N_OUT	51 52
J226	TRUE	SPKRAMP_L_P_OUT	51 52
J228	TRUE	SPKRAMP_R_N_OUT	51 52
J238	TRUE	SPKRAMP_R_P_OUT	51 52
J229	TRUE	SPKRAMP_SUB_N_OUT	51 52
J231	TRUE	SPKRAMP_SUB_P_OUT	51 52

LVDS FUNC_TEST

J258	TRUE	PP3V3_S0_LCD_DDC_F	64
U417	TRUE	PP3V3_SW_LCD_PANEL_F	7 64 (NEED 2 TP)
J260	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67 (NEED 2 TP)
J245	TRUE	LVDS_IG_DDC_CLK	9 64
J262	TRUE	LVDS_IG_DDC_DATA	9 64
J261	TRUE	LVDS_IG_A_DATA_N<0>	9 64 71
J256	TRUE	LVDS_IG_A_DATA_P<0>	9 64 71
J257	TRUE	LVDS_IG_A_DATA_N<1>	9 64 71
J255	TRUE	LVDS_IG_A_DATA_P<1>	9 64 71
J252	TRUE	LVDS_IG_A_DATA_N<2>	9 64 71
J253	TRUE	LVDS_IG_A_DATA_P<2>	9 64 71
J254	TRUE	LVDS_IG_A_CLK_F_N	64 75
J250	TRUE	LVDS_IG_A_CLK_F_P	64 75
J251	TRUE	LED_RETURN_1	64 67
J313	TRUE	LED_RETURN_2	64 67
J246	TRUE	LED_RETURN_3	64 67
J247	TRUE	LED_RETURN_4	64 67
J248	TRUE	LED_RETURN_5	64 67
J249	TRUE	LED_RETURN_6	64 67
J305	TRUE	PP5V_S3_CAMERA_F	7 64
J297	TRUE	USB_CAMERA_CONN_P	64 75
J294	TRUE	USB_CAMERA_CONN_N	64 75

(NEED TO ADD 5 GND TP)

SATA ODD CONN FUNC_TEST

J264	TRUE	PP5V_SW_ODD	7 33 46 (NEED 4 TP)
J268	TRUE	SMC_ODD_DETECT	33 35
J269	TRUE	SATA_ODD_D2R_C_P	33 71
J267	TRUE	SATA_ODD_D2R_C_N	33 71
J265	TRUE	SATA_ODD_R2D_P	33 71
J266	TRUE	SATA_ODD_R2D_N	33 71

(NEED TO ADD 4 GND TP)

SATA HDD/SIL FUNC_TEST

J312	TRUE	PP5V_S0_HDD_FLT	7 33 (NEED 4 TP)
J314	TRUE	SATA_HDD_R2D_P	33 71
J315	TRUE	SATA_HDD_R2D_N	33 71
J316	TRUE	SATA_HDD_D2R_C_P	33 71
J317	TRUE	SATA_HDD_D2R_C_N	33 71
J307	TRUE	SYS_LED_ANODE_R	33

(NEED TO ADD 4 GND TP)

BATT POWER CONN FUNC_TEST

J322	TRUE	PPVBAT_G3H_CONN	54 55 (NEED 3 TP)
J321	TRUE	SMBUS_SMC_BSA_SCL	38 74
J320	TRUE	SMBUS_SMC_BSA_SDA	38 74
J305	TRUE	SYS_DETECT_L	54

(NEED TO ADD 3 GND TP)

HALL EFFECT CONNECTOR FUNC_TEST

J330	TRUE	PP3V42_G3H	7 8 (NEED 2 TP)
J335	TRUE	SMC_LID_R	54

(NEED TO ADD 3 GND TP)

X16 WIRELESS CONN FUNC_TEST

J383	TRUE	PP3V3_S3_BT_F	30
J381	TRUE	CONN_PCIE_MINI_D2R_P	9 30 75
J382	TRUE	CONN_PCIE_MINI_D2R_N	9 30 75
J386	TRUE	CONN_PCIE_MINI_R2D_P	9 30 75
J385	TRUE	CONN_PCIE_MINI_R2D_N	9 30 75
J226	TRUE	PCIE_CLK100M_MINI_CONN_P	30 75
J227	TRUE	PCIE_CLK100M_MINI_CONN_N	30 75
J388	TRUE	PP3V3_WLAN (NEED 4 TP)	7 30
J387	TRUE	PCIE_WAKE_L	16 30
J384	TRUE	CONN_USB2_BT_P	30 75
J390	TRUE	CONN_USB2_BT_N	30 75
J273	TRUE	AP_CLKREQ_Q_L	30
J389	TRUE	AP_RESET_CONN_L	30

(NEED TO ADD 4 GND TP)

IPD_FLEX_CONN FUNC_TEST

U410	TRUE	PP3V3_S3	7 8
J374	TRUE	PP18V5_S3	7 44
J372	TRUE	Z2_CS_L	43 44
J370	TRUE	Z2_DEBUG3	43 44
J371	TRUE	Z2_MOSI	43 44
J369	TRUE	Z2_MISO	43 44
J368	TRUE	Z2_SCLK	43 44
J361	TRUE	Z2_BOOST_EN	44
J366	TRUE	Z2_HOST_INTN	43 44
J365	TRUE	Z2_CLKIN	43 44
J363	TRUE	Z2_KEY_ACT_L	43 44
J364	TRUE	Z2_RESET	43 44
J362	TRUE	PSOC_MISO	43 44
J360	TRUE	PSOC_MOSI	43 44
J359	TRUE	PSOC_SCLK	43 44
J357	TRUE	SMBUS_SMC_A_S3_SDA	38 74
J358	TRUE	SMBUS_SMC_A_S3_SCL	38 74
J377	TRUE	PSOC_F_CS_L	43 44
J376	TRUE	PICKB_L	43 44

(NEED TO ADD 2 GND TP)

KEYBOARD CONN FUNC_TEST

J354	TRUE	PP3V3_S3	7 8
J355	TRUE	PP3V42_G3H	7 8
J344	TRUE	WS_KBD1	43
J345	TRUE	WS_KBD2	43
J346	TRUE	WS_KBD3	43
J347	TRUE	WS_KBD4	43
J348	TRUE	WS_KBD5	43
J349	TRUE	WS_KBD6	43
J350	TRUE	WS_KBD7	43
J352	TRUE	WS_KBD8	43
J351	TRUE	WS_KBD9	43
J353	TRUE	WS_KBD10	43
J327	TRUE	WS_KBD11	43
J328	TRUE	WS_KBD12	43
J329	TRUE	WS_KBD13	43
J343	TRUE	WS_KBD14	43
J342	TRUE	WS_KBD15_CAP	43
J341	TRUE	WS_KBD16_NUM	43
J339	TRUE	WS_KBD17	43
J340	TRUE	WS_KBD18	43
J338	TRUE	WS_KBD19	43
J336	TRUE	WS_KBD20	43
J337	TRUE	WS_KBD21	43
J331	TRUE	WS_KBD22	43
J332	TRUE	WS_KBD23	43
J334	TRUE	WS_KBD_ONOFF_L	43
J333	TRUE	WS_LEFT_SHIFT_KBD	43
J326	TRUE	WS_LEFT_OPTION_KBD	43
J325	TRUE	WS_CONTROL_KBD	43

(NEED TO ADD 1 GND TP)

DC POWER CONN FUNC_TEST

J312	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	54
J304	TRUE	ADAPTER_SENSE	54

(NEED TO ADD 2 GND TP)

POWER NETS FUNC_TEST

J287	TRUE	PPVCORE_S0_CPU	8 39
J285	TRUE	PPVCORE_S0_MCP	8 39
J280	TRUE	PP1V05_S0	8 62
J281	TRUE	PP1V5_S0	8 62 75
J282	TRUE	PP1V8_S0	8
J275	TRUE	PP5V_S0	7 8 62
J302	TRUE	PP5V_S0	7 8 62
J283	TRUE	PP3V3_S0	8 62 75
J279	TRUE	PP1V5R1V35_S3	8 75
J278	TRUE	PP3V3_S3	7 8
J276	TRUE	PP5V_S3	8
J270	TRUE	PP3V3_S5	8 62 75
J273	TRUE	PP3V42_G3H	7 8
J274	TRUE	PPBUS_G3H	8 39
J275	TRUE	PP0V9_ENET	8
J276	TRUE	PP3V3_ENET	8
U410	TRUE	PP3V3_G3_RTC	8 19 20 23
J393	TRUE	PP3V3_WLAN	7 30
J392	TRUE	PP5V_SW_ODD	7 33 46
J391	TRUE	PP5V_S0_HDD_FLT	7 33
J390	TRUE	PP3V3_S5_AVREF_SMC	35 36
J389	TRUE	PP18V5_S3	7 44
J388	TRUE	PP3V3_SW_LCD_PANEL_F	7 64
J386	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67
J385	TRUE	PP4V5_AUDIO_ANALOG	48
J383	TRUE	SMC_PM_G2_EN	35 62
J382	TRUE	PM_SLP_S4_L	19 35 36 62
J381	TRUE	PM_SLP_S3_L	19 35 62 66
J380	TRUE	PP5V_S3_CAMERA_F	7 64
U409	TRUE	PP0V9_S5	8
U412	TRUE	PPDDRVTT_S0	8
U411	TRUE	PP1V05_S0_MCP_PLL_UF	8
U413	TRUE	PPVTT_S3_DDR_BUF	8

(NEED TO ADD 6 GND TP)

J5100 LPC+SPI CONN FUNC_TEST

J423	TRUE	PP3V42_G3H	7 8
J442	TRUE	SPI_CLK	37 72
J440	TRUE	SPI_CS0_L	37 72
J445	TRUE	SPI_MISO	19 37 72
J444	TRUE	SPI_MOSI	37 72
J443	TRUE	SPIROM_USE_MLB	19 37 47
J447	TRUE	LPCPLUS_GPIO	19 37
J448	TRUE	LPC_SERIRQ	19 35 37
J446	TRUE	SMC_TMS	35 36 37

(NEED TO ADD 2 GND TP)

FSB SIGNALS WITH NOTEST

R490	NO_TEST=TRUE	FSB_A_L<35..3>	10 14 69
R489	NO_TEST=TRUE	FSB_ADS_L	10 14 69
R488	NO_TEST=TRUE	FSB_ADSTB_L<1..0>	10 14 69
R493	NO_TEST=TRUE	FSB_D_L<63..0>	10 14 69
R492	NO_TEST=TRUE	FSB_DINV_L<3..0>	10 14 69
R494	NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	10 14 69
R495	NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	10 14 69
R496	NO_TEST=TRUE	FSB_HIT_L	10 14 69
R486	NO_TEST=TRUE	FSB_HITM_L	10 14 69
R497	NO_TEST=TRUE	FSB_LOCK_L	10 14 69
R498	NO_TEST=TRUE	FSB_REQ_L<4..0>	10 14 69

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: FUNC TEST

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"S0,S0M" RAILS

58 =PPVCORE_S0_CPU_REG
(CPU VCORE PWR)
PPVCORE_S0_CPU 7 39
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 11 12

60 =PPCPUVTT_S0_REG
PP1V05_S0 7 62
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU 10 11 12 13
=PP1V05_S0_MCP_FSB 14 20 23
=PP1V05_S0_MCP_PE_DVDD 8 23
=PP1V05_S0_MCP_AVDD_UF 23
=PP1V05_S0_MCP_SATA_DVDD 20 23
=PP1V05_S0_MCP_PLL_UF_R 61
=PP1V05_S0_MCP_M2CLK_DLL 15 23
=PP1V05_S0_MCP_PLL_IFP 17 24
=PP1V05_S0_MCP_DP0_VDD 17 24
=PP1V05_SW_MCP_FSB 20 23

59 =PPMCPCORE_S0_REG
(MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP 7 39
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 20 23
=PPVCORE_S0_MCPGFXFET 22

LVDDR VRef/VTT (0.75V/0.675V) Rails

57 =PPVTT_S0_DDR_LDO
PPDDRVTT_S0 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPDDRVTT_S0_MEM_A 26
=PPDDRVTT_S0_MEM_B 27

57 29 =PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF 7
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

63 =PP1V5_S0_FET
PP1V5_S0 7 62 75
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU 11 12
=PP1V5_S0_MCP_PLL_VLDO 61
=PP1V8R1V5_S0_AUDIO 48
=PP3V3R1V5_S0_AUDIO 48
=PP3V3R1V5_S0_MCP_HDA 19 23

61 =PP1V8_S0_REG
PP1V8_S0 7
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD 17 24

61 =PP1V05_S0_MCP_PLL_OR
PP1V05_S0_MCP_PLL_UF 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PLL_UF 23

UNUSED MCP PE0[3:0] AVDD/DVDD

20 =PP1V05_S0_MCP_PE_DVDD0
20 =PP1V05_S0_MCP_PE_AVDD0
(SINCE PE0[3:0] IS NOT USED ON K6)

(CONNECTS TO MCP BALLS) 20 =PP1V05_S0_MCP_PE_DVDD1 =PP1V05_S0_MCP_PE_DVDD 8 23 (CONNECTS TO THE DECAPS)
(CONNECTS TO MCP BALLS) 20 =PP1V05_S0_MCP_PE_AVDD1 PP1V05_S0_MCP_PE_AVDD 23 (CONNECTS TO THE DECAPS)
MAKE_BASE=TRUE

63 =PP5V_S0_FET
PP5V_S0 7 62
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_HDD 33
=PP5V_S0_MCPREG 59
=PP5V_S0_MCPFSBFET 22
=PP5VR3V3_S0_DPCADET 66
=PP5V_S0_CPUVTTS0 60
=PP5V_S0_LPCPLUS 37
=PP5V_S0_FAN_RT 42
=PP5V_S0_CPU_IMVP 58

63 =PP3V3_S0_FET
PP3V3_S0 7 62 75
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP 13
=PP3V3_S0_MCP 20 23
=PP3V3_S0_ODD 33
=PP3V3_S0_SMBUS_SMC_0_S0 38
=PP3V3_S0_SMBUS_SMC_B_S0 38
=PP3V3_S0_SMBUS_MCP_0 38
=PP3V3_S0_FAN_RT 42
=PP3V3_S0_AUDIO 48 52 53
=PP3V3_S0_IMVP 58
=PP3V3_S0_LCD_DDC 64
=PP3V3_S0_MCP_GPIO 17 18 19
=PP3V3_S0_MCP_PLL_UF 23
=PP3V3_S0_MCP_HVDD 20 23
=PP3V3_S0_SMC 36
=PP3V3_S0_MCPTHMSNS 41
=PP3V3_S0_CPUTHMSNS 41
=PP3V3_S0_DPCONN 66
=PPSPD_S0_MEM_A 26
=PPSPD_S0_MEM_B 27
=PP3V3_S0_PWRCTL 62
=PP3V3_S0_CPUVTTISNS 40
=PP3V3_S0_SMBUS_MCP_1 38
=PP3V3_S0_P1V8S0 61
=PP3V3_S0_MCP_PLL_VLDO 61
=PP3V3_S0_MCPDDRISNS 40
=PP3V3_S0_DEBUGROM 37
=PP3V3_S0_MCPCOREISNS 40
=PP3V3_S0_OPA330 23

"ENET" RAILS

63 62 61 9 =PP3V3_ENET_FET
PP3V3_ENET 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_PHY 9 31
=PP3V3_ENET_MCP_PLL_MAC 23
=PP3V3_ENET_MCP_RMGT 9 18 20 23
ENET1V05:INT
R0814
0
1 2
5%
1/10W
MF-LF
402
PP3V3_ENET_PHY_VDDREG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_PHY_VDDREG 31

63 =PP0V9_ENET_FET
PP0V9_ENET 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_ENET_MCP_RMGT 20 23

RTL8211_REGOUT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
31 =RTL8211_REGOUT
ENET1V05:INT
R0812
0
1 2
402 5% 1/10W MF-LF
PP1V05_ENET
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2mm

PP1V05_S0_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
61 =PP1V05_S0_REG
ENET1V05:EXT
R0813
0
1 2
402 5% 1/10W MF-LF
=PP1V05_ENET_PHY 31

FIX ME!! OUTPUT OF REGULATOR VALUES

"S3" RAILS

63 57 =PPDDR_S3_REG
PP1V5R1V35_S3 7 75
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PPLVDDR_S3_MEM_A 26
=PPLVDDR_S3_MEM_B 27
0 MA =PP1V5R1V35_S3_MCP_MEM 15
4250 MA =PP1V5R1V35_S0_MCPDDRFET 21
=PPVIN_S0_DDRREG_LDO 57

63 =PP3V3_S3_FET
PP3V3_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 38
=PP3V3_S3_PDCISENS
=PP3V3_S3_VREFMRGN 29
=PP3V3_S3_WLAN 30
=PP3V3_S3_MCP_GPIO 19
=PP3V3_S3_TPAD 43 44
=PP3V3_S3_SMS 45
=PP3V3_S3_BT 30
=PP3V3_S3_SMBUS_SMC_MGMT 38

56 =PP5V_S3_REG
PP5V_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB 34
=PP5V_S3_CAMERA 64
=PP5V_S3_AUDIO_AMP 51
=PP5V_S3_MCPDDRFET 21
=PP5V_S3_AUDIO 48 50 52
=PP5V_S3_DEBUG_ISNS 46
=PP5V_S3_SYSLED 36
=PP5V_S3_TPAD 44
=PP5V_S3_ODD 33
=PP5V_S3_DEBUG_ADC_AVDD 46
=PP5V_S3_DEBUG_ADC_DVDD 46
=PP5V_S3_P5VS0FET 63
=PP5V_S3_DDRREG 57

"S5" RAILS

61 =PP0V9_S5_REG
PP0V9_S5 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
105/241 MA =PP0V9_S5_MCP_VDD_AUXC 20 23
=PP0V9_ENET_P0V9ENETFET 63

56 =PP3V3_S5_REG
PP3V3_S5 7 62 75
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO 18 19
=PP3V3_S5_ROM 47
=PP3V3_S0_LCD_PANEL 64
=PP3V3_S5_MCP 20 23
=PP3V3_S5_MCPPWRGD 25
=PP3V3_S5_P3V3S3FET 63
=PP3V3_S5_P3V3S0FET 63
=PP3V3_S5_P0V9S5 61
=PP3V3_S5_P3V3ENETFET 63
=PP3V3_S5_DP_PORT_PWR 66
=PP3V3_S5_VMON 62
=PP3V3_S5_P0V9ENETFET 63

"G3H" RAILS

54 =PP3V42_G3H_REG
PP3V42_G3H 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF 36
=PP3V42_G3H_SMBUS_SMC_BSA 38
=PP3V42_G3H_PWRCTL 62
=PP3V42_G3H_CHGR 55 62
=PP3V42_G3H_SMCUSBMUX 34
=PP3V42_G3H_TPAD 43
=PP3V3_S5_SMC 35 36
=PP3V3_S5_LPCPLUS 37
PP3V3_G3_RTC 7 19 20 23
=PP3V42_G3H_ONEWIRE 54
=PP3V42_G3H_HALL 54
=PP3V42_G3H_BMON_ISNS 40
=PP3V42_G3H_OPA330

54 =PP18V5_DCIN_CONN
PP18V5_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 55

55 =PPBUS_G3H
PPBUS_G3H 7 39
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_MCPCORE 59
=PPBUS_S0_LCDBKLT 68
=PPVIN_S5_3V3S5 56
=PPVIN_S3_5VS3 56
=PPBUS_S5_CPUREGS_ISNS_R 40
=PPVIN_S3_DDRREG 57

40 =PPBUS_S5_CPUREGS_ISNS
PPBUS_S5_IMVP_VTT_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 60
=PPVIN_S5_CPU_IMVP 58

DIGITAL GROUND
GND
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V

SYNC_MASTER=MASTER SYNC_DATE=MASTER
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Power Aliases
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HEATSINK STANDOFFS

Z0902
STDOFF-4.50D.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.50D.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.50D.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

OMIT
Z0905
3P2R2P7

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT
Z0906
3P2R2P7

OMIT
Z0907
3P2R2P7

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT
Z0911
3P2R2P7

OMIT
Z0910
3P2R2P7

LVDS CONNECTOR HOLE

OMIT
Z0913
3P2R2P7

EMI IO MEDIUM POGO PINS (870-1794)

OMIT
ZS0900
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0901
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0902
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0908
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0909
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0911
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0903
2.0DIA-MED-EMI-MLB-K84
SM

EMI TALL POGO PINS (870-1698)

OMIT
ZS0904
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0905
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0906
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0907
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0910
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0912
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0913
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0914
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0915
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0919
2.0DIA-TALL-EMI-MLB-M97-M98
SM

EMI THINBC POGO PINS (870-1820)

OMIT
ZS0917
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0918
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0916
2.0DIA-MLB-THIN-BC-K84
SM

NOSTUFF
ZS0920
2.0DIA-MLB-THIN-BC-K84
SM

PCI-E ALIASES

30	PCIE_MINI_R2D_C_P	PCIE_AP_R2D_C_P	16 71
30	PCIE_MINI_R2D_C_N	PCIE_AP_R2D_C_N	16 71
75 30 7	CONN_PCIE_MINI_D2R_P	PCIE_AP_D2R_P	16 71
75 30 7	CONN_PCIE_MINI_D2R_N	PCIE_AP_D2R_N	16 71
30	PCIE_CLK100M_MINI_P	PCIE_CLK100M_AP_P	16 71
30	PCIE_CLK100M_MINI_N	PCIE_CLK100M_AP_N	16 71
75 30 7	CONN_PCIE_MINI_R2D_P	PCIE_AP_R2D_P	71
75 30 7	CONN_PCIE_MINI_R2D_N	PCIE_AP_R2D_N	71

MAKE_BASE=TRUE

UNUSED GPU LANES

16	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	
16	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	
16	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	
16	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	
71 16	PEG_CLK100M_P	TP_PEG_CLK100M_P	
71 16	PEG_CLK100M_N	TP_PEG_CLK100M_N	
16	PEG_CLKREQ_L	TP_PCIE_CLKREQ_L	

NO_TEST=TRUE
MAKE_BASE=TRUE

UNUSED FIREWIRE LANE

71 16	PCIE_FW_D2R_P	TP_PCIE_FW_D2R_P
71 16	PCIE_FW_D2R_N	TP_PCIE_FW_D2R_N
71 16	PCIE_FW_R2D_C_P	TP_PCIE_FW_R2D_C_P
71 16	PCIE_FW_R2D_C_N	TP_PCIE_FW_R2D_C_N
16	FW_PWR_EN	TP_FW_PWR_EN
16	FW_CLKREQ_L	TP_FW_CLKREQ_L
16	FW_PME_L	TP_FW_PME_L
71 16	PCIE_CLK100M_FW_P	TP_PCIE_CLK100M_FW_P
71 16	PCIE_CLK100M_FW_N	TP_PCIE_CLK100M_FW_N

MAKE_BASE=TRUE

UNUSED ETHERNET LANE

16	ENET_CLKREQ_L	TP_ENET_CLKREQ_L
71 16	PCIE_CLK100M_ENET_P	TP_PCIE_CLK100M_ENET_P
71 16	PCIE_CLK100M_ENET_N	TP_PCIE_CLK100M_ENET_N
71 16	PCIE_ENET_D2R_P	TP_PCIE_ENET_D2R_P
71 16	PCIE_ENET_D2R_N	TP_PCIE_ENET_D2R_N
71 16	PCIE_ENET_R2D_C_P	TP_PCIE_ENET_R2D_C_P
71 16	PCIE_ENET_R2D_C_N	TP_PCIE_ENET_R2D_C_N

MAKE_BASE=TRUE

R0970
100K
5%
1/16W
MF-LF
402

18 IN ENET_ENERGY_DET — 1 2 — =PP3V3_ENET_FET OUT 8 61 62 63

USB ALIASES

UNUSED USB PORTS

72 18	USB_EXTD_P	TP_USB_EXTD_P	
72 18	USB_EXTD_N	TP_USB_EXTD_N	
72 18	USB_EXTC_P	TP_USB_EXTC_P	
72 18	USB_EXTC_N	TP_USB_EXTC_N	
72 18	USB_MINI_P	TP_USB_MINI_P	
72 18	USB_MINI_N	TP_USB_MINI_N	
72 18	USB_SDCARD_P	TP_USB_SDCARD_P	
72 18	USB_SDCARD_N	TP_USB_SDCARD_N	
72 18	USB_WM_P	TP_USB_WM_P	
72 18	USB_WM_N	TP_USB_WM_N	
72 18	USB_IR_N	TP_USB_IR_N	
72 18	USB_IR_P	TP_USB_IR_P	
72 18	USB_T57_P	TP_USB_T57_P	
72 18	USB_T57_N	TP_USB_T57_N	

MAKE_BASE=TRUE

LVDS ALIASES

17	IN =MCP_IFPA_TXD_P<0..2>	LVDS_IG_A_DATA_P<0..2>	OUT 7 64 71
17	IN =MCP_IFPA_TXD_N<0..2>	LVDS_IG_A_DATA_N<0..2>	OUT 7 64 71
17	IN =MCP_IFPAB_DDC_CLK	LVDS_IG_DDC_CLK	OUT 7 64
17	BI =MCP_IFPAB_DDC_DATA	LVDS_IG_DDC_DATA	BI 7 64
17	IN =MCP_IFPA_TXD_P<3>	NC_LVDS_IG_A_DATA_P3	
17	IN =MCP_IFPA_TXD_N<3>	NC_LVDS_IG_A_DATA_N3	
17	IN =MCP_IFPB_TXC_P	NC_LVDS_IG_B_CLK_P	
17	IN =MCP_IFPB_TXC_N	NC_LVDS_IG_B_CLK_N	
17	IN =MCP_IFPB_TXD_P<0..3>	NC_LVDS_IG_B_DATA_P<0..3>	
17	IN =MCP_IFPB_TXD_N<0..3>	NC_LVDS_IG_B_DATA_N<0..3>	
17	IN LCD_IG_BKLT_PWM	LVDS_IG_BKL_PWM	OUT 67 68
17	IN LCD_IG_BKLT_EN	LVDS_IG_BKL_ON	OUT 68
17	IN LCD_IG_PWR_EN	LVDS_IG_PANEL_PWR	OUT 64
17	IN =MCP_IFPA_TXC_P	LVDS_IG_A_CLK_P	OUT 64 71
17	IN =MCP_IFPA_TXC_N	LVDS_IG_A_CLK_N	OUT 64 71

NO_TEST=TRUE
MAKE_BASE=TRUE

DISPLAY PORT ALIASES

17	IN DP_IG_ML0_P<0..3>	DP_EXT_ML_P<0..3>	OUT 66 75
		DP_IG_ML_P<0..3>	OUT 71
17	IN DP_IG_ML0_N<0..3>	DP_EXT_ML_N<0..3>	OUT 66 75
		DP_IG_ML_N<0..3>	OUT 71
17	BI DP_IG_AUX_CH0_P	DP_IG_AUX_CH_P	BI 65 71
17	BI DP_IG_AUX_CH0_N	DP_IG_AUX_CH_N	BI 65 71
17	IN DP_IG_ML1_P<0..3>	TP_DP_IG_ML1P<0..3>	
17	IN DP_IG_ML1_N<0..3>	TP_DP_IG_ML1N<0..3>	
17	BI DP_IG_AUX_CH1_P	TP_DP_IG_AUX_CH1P	
17	BI DP_IG_AUX_CH1_N	TP_DP_IG_AUX_CH1N	
17	OUT DP_IG_HPD0	DP_EXT_HPD	IN 66
65	BI DP_AUX_CH_C_N	DP_EXT_AUX_CH_C_N	BI 66 75
65	BI DP_AUX_CH_C_P	DP_EXT_AUX_CH_C_P	BI 66 75
65	OUT DP_CA_DET	DP_EXT_CA_DET	IN 66

MAKE_BASE=TRUE

R0940
100K
5%
1/16W
MF-LF
402

17 DP_IG_HPD1 — 1 2

MCP89 MISC ALIASES

19 IN MCP_MEM_VDD_SEL_1V5 — TP_MCP_MEM_VDD_SEL_1V5
MAKE_BASE=TRUE

ETHERNET ALIASES

18	TP_ENET_RESET_L	ENET_RESET_L	31 73
18	TP_MCP_CLK25M_BUF0_R	MCP_CLK25M_BUF0_R	31 73
18	TP_ENET_MDC	ENET_MDC	31 73
18	TP_ENET_TX_CTRL	ENET_TX_CTRL	31 73
18	TP_ENET_CLK125M_TXCLK	ENET_CLK125M_TXCLK	31 73
18	TP_ENET_TXD<0..3>	ENET_TXD<0..3>	31 73

MAKE_BASE=TRUE

31 8 =PP3V3_ENET_PHY

ENET1V05:INT
R0915
0
5%
1/16W
MF-LF
402

ENET1V05:EXT
R0916
0
5%
1/16W
MF-LF
402

RTL8211_ENSWREG
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2mm MAKE_BASE=TRUE
=RTL8211_ENSWREG OUT 31

MCP89 ETHERNET VREF

23 20 18 8 =PP3V3_ENET_MCP_RMGT

R0957
1.47K
1%
1/16W
MF-LF
402

MCP_RGMII_VREF OUT 18

R0958
1.47K
1%
1/16W
MF-LF
402

C0958
0.1UF
20%
10V
CERM
402

CPU FSB FREQUENCY STRAPS

69 10 IN CPU_BSEL<0:2> — =MCP_BSEL<0:2> OUT 14
MAKE_BASE=TRUE

14 CPU_PECI_MCP — TP_CPU_PECI_MCP
MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

SMC ALIASES

35 SMC_SYS_KBDLED — TP_SMC_SYS_KBDLED
MAKE_BASE=TRUE

CHARGER SIGNAL

55 IN =CHGR_ACOK — SMC_BC_ACOK
MAKE_BASE=TRUE OUT 35 36 54

CPU VCORE ALIASES

58 IN IMVP6_VR_TT — TP_IMVP6_VR_TT
58 IN IMVP6_NTC — TP_IMVP6_NTC
MAKE_BASE=TRUE

SYNC_MASTER=(K84_MLB) SYNC_DATE=(02/04/2009)

PAGE TITLE
SIGNAL ALIAS

Apple Inc.

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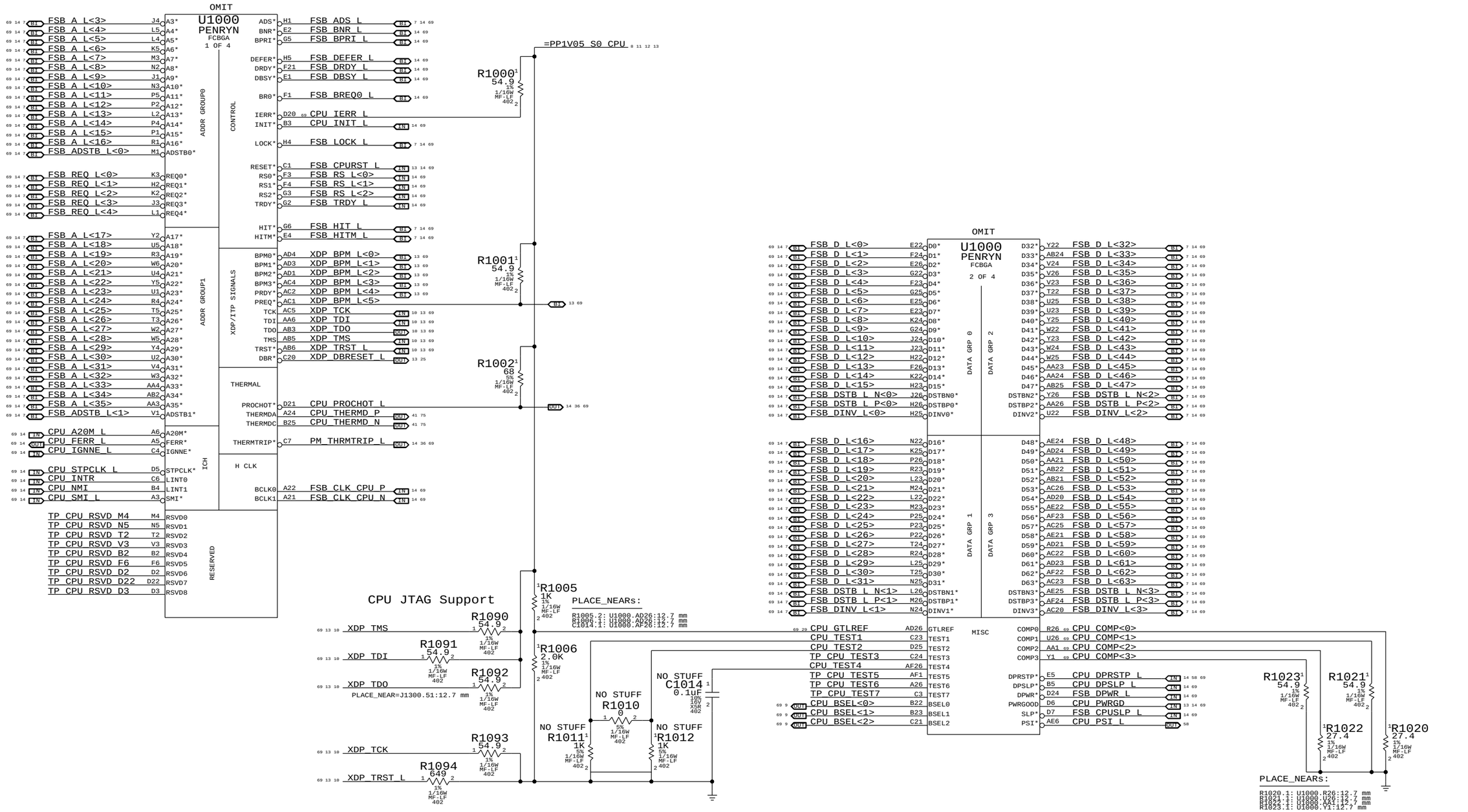

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

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Apple Inc.

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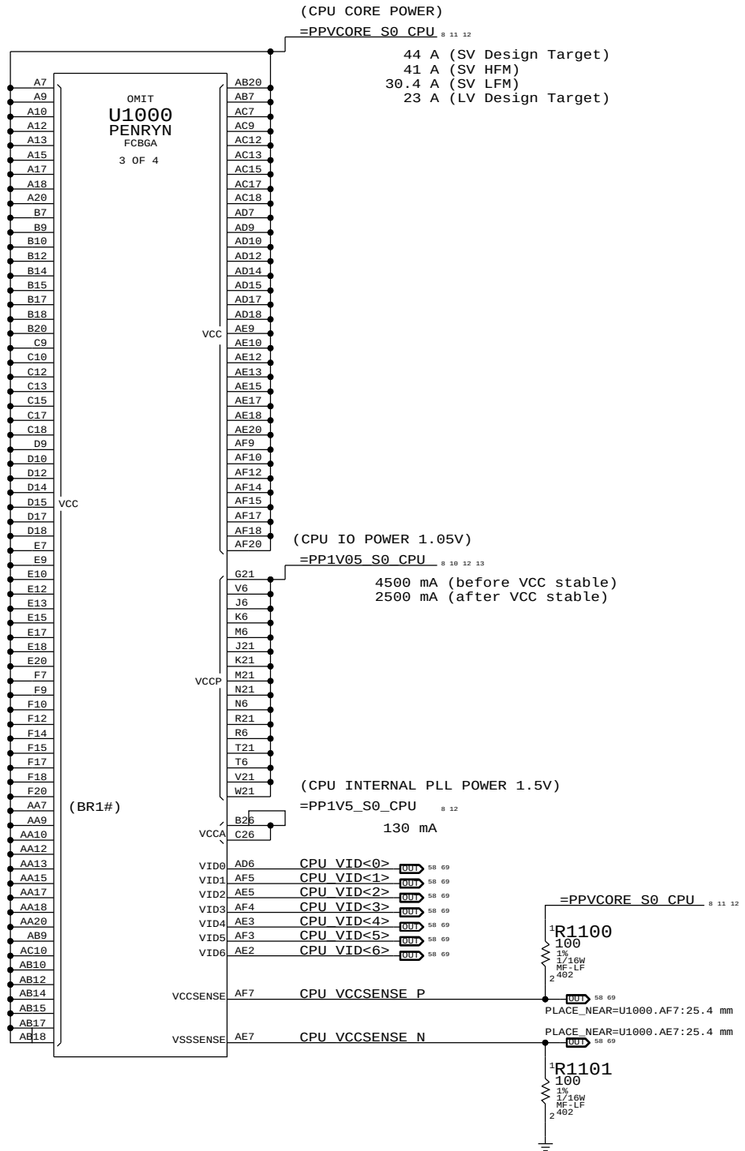

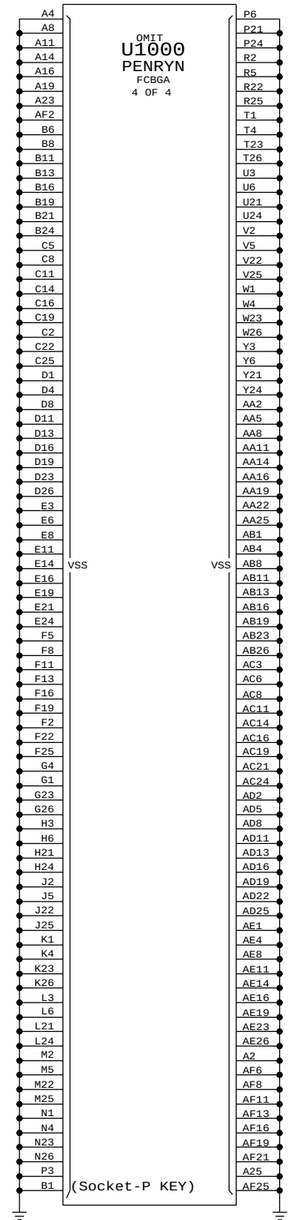

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE
CPU Power & Ground

Apple Inc.

DRAWING NUMBER 051-8561
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REVISION C.0.0
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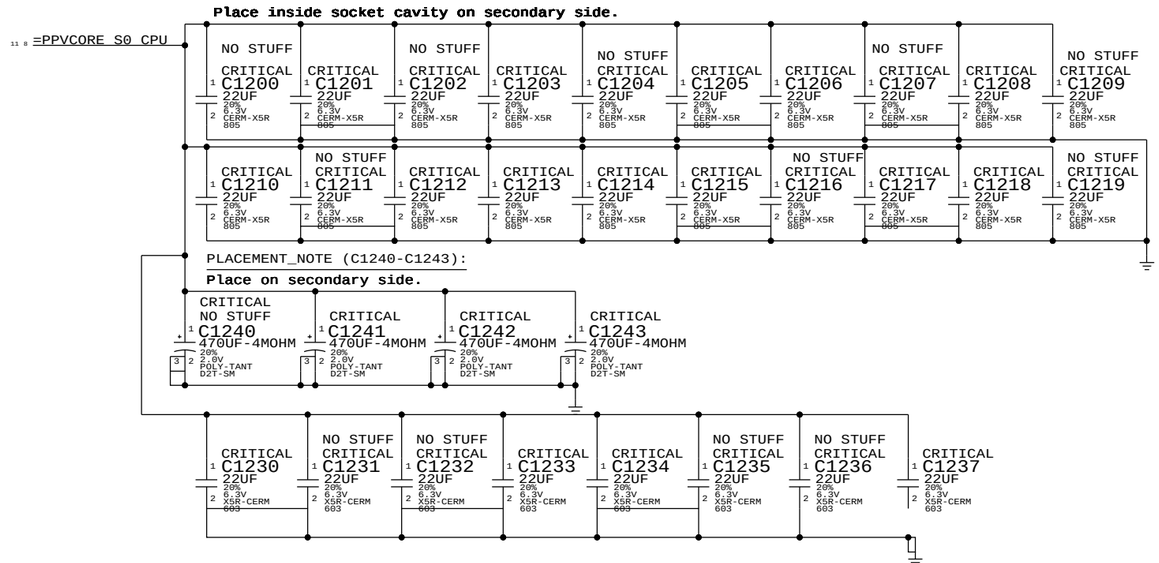
CPU VCore HF and Bulk Decoupling

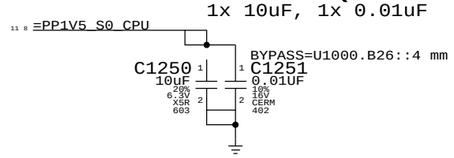
4X 330UF. 20X 22UF 0805

PLACEMENT_NOTE (C1200-C1219):



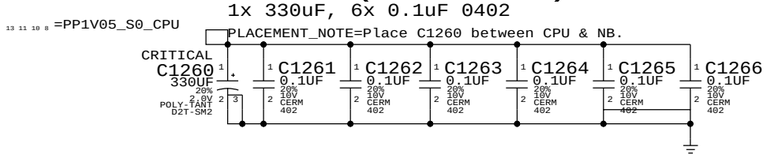
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

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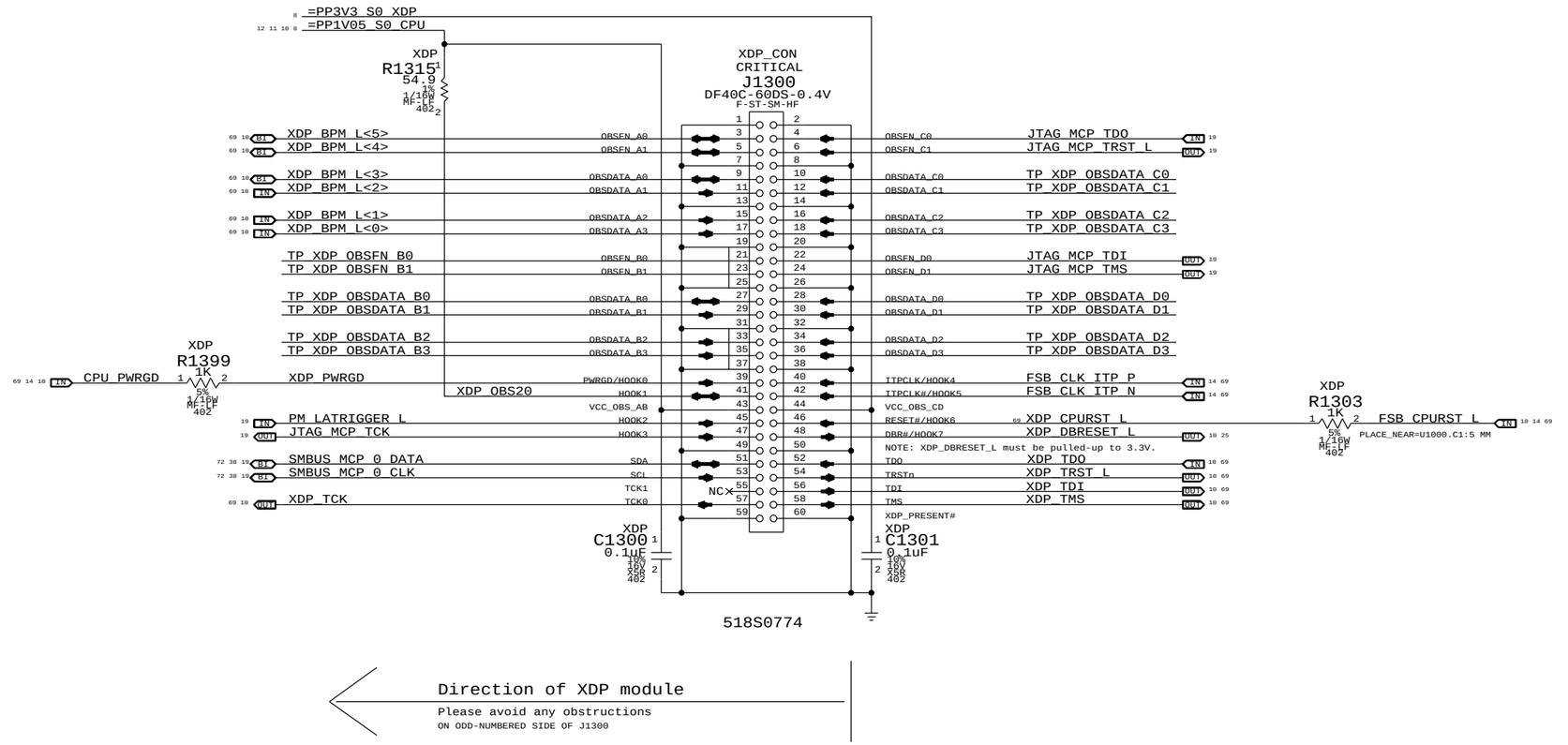
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP89-SPECIFIC PINOUT



Direction of XDP module

Please avoid any obstructions

ON ODD-NUMBERED SIDE OF J1300

SYNC_MASTER=(K84_MLB) SYNC_DATE=(02/25/2009)

PAGE TITLE: eXtended Debug Port(MiniXDP)

Apple Inc.

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FSB

FSB_DSTB_L_P<0>	K34	CPU_DSTBP0*	
FSB_DSTB_L_N<0>	K35	CPU_DSTBN0*	
FSB_DINV_L<0>	L37	CPU_DBI0*	
FSB_DSTB_L_P<1>	T31	CPU_DSTBP1*	
FSB_DSTB_L_N<1>	T30	CPU_DSTBN1*	
FSB_DINV_L<1>	P28	CPU_DBI1*	
FSB_DSTB_L_P<2>	K33	CPU_DSTBP2*	
FSB_DSTB_L_N<2>	K32	CPU_DSTBN2*	
FSB_DINV_L<2>	N35	CPU_DBI2*	
FSB_DSTB_L_P<3>	C36	CPU_DSTBP3*	
FSB_DSTB_L_N<3>	D36	CPU_DSTBN3*	
FSB_DINV_L<3>	A35	CPU_DBI3*	
FSB_A_L<3>	U38	CPU_A3*	
FSB_A_L<4>	U34	CPU_A4*	
FSB_A_L<5>	U35	CPU_A5*	
FSB_A_L<6>	T34	CPU_A6*	
FSB_A_L<7>	W37	CPU_A7*	
FSB_A_L<8>	W38	CPU_A8*	
FSB_A_L<9>	T37	CPU_A9*	
FSB_A_L<10>	Y38	CPU_A10*	
FSB_A_L<11>	W35	CPU_A11*	
FSB_A_L<12>	Y36	CPU_A12*	
FSB_A_L<13>	U33	CPU_A13*	
FSB_A_L<14>	W34	CPU_A14*	
FSB_A_L<15>	Y37	CPU_A15*	
FSB_A_L<16>	Y35	CPU_A16*	
FSB_A_L<17>	AF38	CPU_A17*	
FSB_A_L<18>	AB35	CPU_A18*	
FSB_A_L<19>	Y34	CPU_A19*	
FSB_A_L<20>	AE38	CPU_A20*	
FSB_A_L<21>	AC36	CPU_A21*	
FSB_A_L<22>	AF36	CPU_A22*	
FSB_A_L<23>	AC38	CPU_A23*	
FSB_A_L<24>	AB36	CPU_A24*	
FSB_A_L<25>	AB38	CPU_A25*	
FSB_A_L<26>	AB37	CPU_A26*	
FSB_A_L<27>	AC34	CPU_A27*	
FSB_A_L<28>	AE36	CPU_A28*	
FSB_A_L<29>	AF37	CPU_A29*	
FSB_A_L<30>	AC37	CPU_A30*	
FSB_A_L<31>	AC35	CPU_A31*	
FSB_A_L<32>	AE37	CPU_A32*	
FSB_A_L<33>	AE35	CPU_A33*	
FSB_A_L<34>	AE33	CPU_A34*	
FSB_A_L<35>	AE34	CPU_A35*	
FSB_ADSTB_L<0>	W36	CPU_ADSTB0*	
FSB_ADSTB_L<1>	AB34	CPU_ADSTB1*	
FSB_REQ_L<0>	U36	CPU_REQ0*	
FSB_REQ_L<1>	T36	CPU_REQ1*	
FSB_REQ_L<2>	U37	CPU_REQ2*	
FSB_REQ_L<3>	T38	CPU_REQ3*	
FSB_REQ_L<4>	T35	CPU_REQ4*	
FSB_ADS_L	AE31	CPU_ADS*	
FSB_BNR_L	AE32	CPU_BNR*	
FSB_BREQ0_L	AE30	CPU_BR0*	
FSB_DBSY_L	AE29	CPU_DBSY*	
FSB_DRDY_L	U29	CPU_DRDY*	
FSB_HIT_L	W32	CPU_HIT*	
FSB_HITM_L	AB31	CPU_HITM*	
FSB_LOCK_L	AC32	CPU_LOCK*	
FSB_TRDY_L	AC29	CPU_TRDY*	
CPU_PECI_MCP	AH34	CPU_PECI	
CPU_PROCHOT_L	U28	CPU_PROCHOT*	
	W33	CPU_THERMTRIP*	
PM_THRMTRIP_L	AB32	CPU_FERR*	
CPU_FERR_L			
=MCP_BSEL<2>	B34	CPU_BSEL2	
=MCP_BSEL<1>	C34	CPU_BSEL1	
=MCP_BSEL<0>	A34	CPU_BSEL0	
FSB_RS_L<0>	AB29	CPU_RS0*	
FSB_RS_L<1>	AC33	CPU_RS1*	
FSB_RS_L<2>	AC31	CPU_RS2*	
MCP_BCLK_VML_COMP_VDD	AH37	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AH38	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AH36	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AH35	CPU_COMP_GND	

CPU_D0*	N38	FSB_D_L<0>	
CPU_D1*	N36	FSB_D_L<1>	
CPU_D2*	P36	FSB_D_L<2>	
CPU_D3*	L36	FSB_D_L<3>	
CPU_D4*	N34	FSB_D_L<4>	
CPU_D5*	L35	FSB_D_L<5>	
CPU_D6*	P37	FSB_D_L<6>	
CPU_D7*	P38	FSB_D_L<7>	
CPU_D8*	N36	FSB_D_L<8>	
CPU_D9*	L34	FSB_D_L<9>	
CPU_D10*	K37	FSB_D_L<10>	
CPU_D11*	K36	FSB_D_L<11>	
CPU_D12*	K38	FSB_D_L<12>	
CPU_D13*	N37	FSB_D_L<13>	
CPU_D14*	H37	FSB_D_L<14>	
CPU_D15*	L38	FSB_D_L<15>	
CPU_D16*	N28	FSB_D_L<16>	
CPU_D17*	U30	FSB_D_L<17>	
CPU_D18*	N29	FSB_D_L<18>	
CPU_D19*	P34	FSB_D_L<19>	
CPU_D20*	T29	FSB_D_L<20>	
CPU_D21*	T32	FSB_D_L<21>	
CPU_D22*	U32	FSB_D_L<22>	
CPU_D23*	T33	FSB_D_L<23>	
CPU_D24*	P31	FSB_D_L<24>	
CPU_D25*	P30	FSB_D_L<25>	
CPU_D26*	N30	FSB_D_L<26>	
CPU_D27*	P33	FSB_D_L<27>	
CPU_D28*	N31	FSB_D_L<28>	
CPU_D29*	T28	FSB_D_L<29>	
CPU_D30*	P35	FSB_D_L<30>	
CPU_D31*	P29	FSB_D_L<31>	
CPU_D32*	H33	FSB_D_L<32>	
CPU_D33*	G34	FSB_D_L<33>	
CPU_D34*	L30	FSB_D_L<34>	
CPU_D35*	L31	FSB_D_L<35>	
CPU_D36*	L33	FSB_D_L<36>	
CPU_D37*	P32	FSB_D_L<37>	
CPU_D38*	N32	FSB_D_L<38>	
CPU_D39*	N33	FSB_D_L<39>	
CPU_D40*	H35	FSB_D_L<40>	
CPU_D41*	K31	FSB_D_L<41>	
CPU_D42*	H34	FSB_D_L<42>	
CPU_D43*	K30	FSB_D_L<43>	
CPU_D44*	L32	FSB_D_L<44>	
CPU_D45*	G33	FSB_D_L<45>	
CPU_D46*	H32	FSB_D_L<46>	
CPU_D47*	G35	FSB_D_L<47>	
CPU_D48*	C37	FSB_D_L<48>	
CPU_D49*	D37	FSB_D_L<49>	
CPU_D50*	H38	FSB_D_L<50>	
CPU_D51*	G38	FSB_D_L<51>	
CPU_D52*	G37	FSB_D_L<52>	
CPU_D53*	G36	FSB_D_L<53>	
CPU_D54*	B35	FSB_D_L<54>	
CPU_D55*	E35	FSB_D_L<55>	
CPU_D56*	B36	FSB_D_L<56>	
CPU_D57*	E36	FSB_D_L<57>	
CPU_D58*	C35	FSB_D_L<58>	
CPU_D59*	D34	FSB_D_L<59>	
CPU_D60*	E38	FSB_D_L<60>	
CPU_D61*	D38	FSB_D_L<61>	
CPU_D62*	E34	FSB_D_L<62>	
CPU_D63*	E37	FSB_D_L<63>	
CPU_BPRI*	Y31	FSB_BPRI_L	
CPU_DEFER*	Y30	FSB_DEFER_L	
BCLK_OUT_CPU_N	AF32	FSB_CLK_CPU_N	
BCLK_OUT_CPU_P	AF33	FSB_CLK_CPU_P	
BCLK_OUT_ITP_N	AF35	FSB_CLK_ITP_N	
BCLK_OUT_ITP_P	AF34	FSB_CLK_ITP_P	
BCLK_OUT_NB_N	AF28	FSB_CLK_MCP_N	
BCLK_OUT_NB_P	AF29	FSB_CLK_MCP_P	
BCLK_IN_P	AF30		
BCLK_IN_N	AF31		
CPU_A20M*	W30	CPU_A20M_L	
CPU_IGNNE*	AB30	CPU_IGNNE_L	
CPU_INIT*	AB28	CPU_INIT_L	
CPU_INTR	W31	CPU_INTR	
CPU_NMI	AC30	CPU_NMI	
CPU_SMI*	AC28	CPU_SMI_L	
CPU_PWRGD	Y32	CPU_PWRGD	
CPU_RESET*	AE28	FSB_CPURST_L	
CPU_DPRSLPVR	G1	PM_DPRSLPVR	
CPU_SLP*	Y33	FSB_CPUSLP_L	
CPU_DPSLP*	AB33	CPU_DPSLP_L	
CPU_DPWR*	U31	FSB_DPWR_L	
CPU_STPCLK*	Y29	CPU_STPCLK_L	
CPU_DPRSTP*	W29	CPU_DPRSTP_L	

23 20 14 8 =PP1V05_S0_MCP_FSB

R1410[1] 54.9 1% 1/16W MF-LF 402 [2]
[1]R1415 62 5% 1/16W MF-LF 402 [2]

R1430[1] 49.9 1% 1/16W MF-LF 402 [2]
[1]R1435 49.9 1% 1/16W MF-LF 402 [2]

R1431[1] 49.9 1% 1/16W MF-LF 402 [2]
[1]R1436 49.9 1% 1/16W MF-LF 402 [2]

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB 8 14 20 23
NO STUFF
[1]R1440 150 5% 1/16W MF-LF 402 [2]

SYNC_MASTER=T27_MLB	SYNC_DATE=02/16/2010
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MEMORY PARTITION 0

MEM_A_DQ<63>	AP5	MDQ0_63	
MEM_A_DQ<62>	AP7	MDQ0_62	
MEM_A_DQ<61>	AR8	MDQ0_61	
MEM_A_DQ<60>	AP8	MDQ0_60	
MEM_A_DQ<59>	AR4	MDQ0_59	
MEM_A_DQ<58>	AR5	MDQ0_58	
MEM_A_DQ<57>	AM8	MDQ0_57	
MEM_A_DQ<56>	AN8	MDQ0_56	
MEM_A_DQ<55>	AK11	MDQ0_55	
MEM_A_DQ<54>	AL11	MDQ0_54	
MEM_A_DQ<53>	AH13	MDQ0_53	
MEM_A_DQ<52>	AH14	MDQ0_52	
MEM_A_DQ<51>	AL10	MDQ0_51	
MEM_A_DQ<50>	AK10	MDQ0_50	
MEM_A_DQ<49>	AN11	MDQ0_49	
MEM_A_DQ<48>	AJ13	MDQ0_48	
MEM_A_DQ<47>	AK13	MDQ0_47	
MEM_A_DQ<46>	AK14	MDQ0_46	
MEM_A_DQ<45>	AJ16	MDQ0_45	
MEM_A_DQ<44>	AH16	MDQ0_44	
MEM_A_DQ<43>	AJ14	MDQ0_43	
MEM_A_DQ<42>	AL13	MDQ0_42	
MEM_A_DQ<41>	AM14	MDQ0_41	
MEM_A_DQ<40>	AN14	MDQ0_40	
MEM_A_DQ<39>	AK17	MDQ0_39	
MEM_A_DQ<38>	AL17	MDQ0_38	
MEM_A_DQ<37>	AN17	MDQ0_37	
MEM_A_DQ<36>	AJ19	MDQ0_36	
MEM_A_DQ<35>	AH17	MDQ0_35	
MEM_A_DQ<34>	AJ17	MDQ0_34	
MEM_A_DQ<33>	AM16	MDQ0_33	
MEM_A_DQ<32>	AM17	MDQ0_32	
MEM_A_DQ<31>	AN26	MDQ0_31	
MEM_A_DQ<30>	AH29	MDQ0_30	
MEM_A_DQ<29>	AK29	MDQ0_29	
MEM_A_DQ<28>	AL29	MDQ0_28	
MEM_A_DQ<27>	AM25	MDQ0_27	
MEM_A_DQ<26>	AM26	MDQ0_26	
MEM_A_DQ<25>	AL28	MDQ0_25	
MEM_A_DQ<24>	AK28	MDQ0_24	
MEM_A_DQ<23>	AM28	MDQ0_23	
MEM_A_DQ<22>	AP29	MDQ0_22	
MEM_A_DQ<21>	AL31	MDQ0_21	
MEM_A_DQ<20>	AN32	MDQ0_20	
MEM_A_DQ<19>	AP28	MDQ0_19	
MEM_A_DQ<18>	AN28	MDQ0_18	
MEM_A_DQ<17>	AN31	MDQ0_17	
MEM_A_DQ<16>	AM31	MDQ0_16	
MEM_A_DQ<15>	AR34	MDQ0_15	
MEM_A_DQ<14>	AM32	MDQ0_14	
MEM_A_DQ<13>	AL33	MDQ0_13	
MEM_A_DQ<12>	AL35	MDQ0_12	
MEM_A_DQ<11>	AP32	MDQ0_11	
MEM_A_DQ<10>	AP33	MDQ0_10	
MEM_A_DQ<9>	AM35	MDQ0_9	
MEM_A_DQ<8>	AL32	MDQ0_8	
MEM_A_DQ<7>	AJ35	MDQ0_7	
MEM_A_DQ<6>	AJ31	MDQ0_6	
MEM_A_DQ<5>	AH32	MDQ0_5	
MEM_A_DQ<4>	AH33	MDQ0_4	
MEM_A_DQ<3>	AJ34	MDQ0_3	
MEM_A_DQ<2>	AL34	MDQ0_2	
MEM_A_DQ<1>	AJ33	MDQ0_1	
MEM_A_DQ<0>	AJ32	MDQ0_0	
MEM_A_DM<7>	AR7	MDQM0_7	
MEM_A_DM<6>	AM11	MDQM0_6	
MEM_A_DM<5>	AL14	MDQM0_5	
MEM_A_DM<4>	AN16	MDQM0_4	
MEM_A_DM<3>	AJ29	MDQM0_3	
MEM_A_DM<2>	AP31	MDQM0_2	
MEM_A_DM<1>	AM34	MDQM0_1	
MEM_A_DM<0>	AJ30	MDQM0_0	

MDQS0_7_P	AN7	MEM_A_DQS_P<7>	
MDQS0_7_N	AM7	MEM_A_DQS_N<7>	
MDQS0_6_P	AN10	MEM_A_DQS_P<6>	
MDQS0_6_N	AM10	MEM_A_DQS_N<6>	
MDQS0_5_P	AN13	MEM_A_DQS_P<5>	
MDQS0_5_N	AM13	MEM_A_DQS_N<5>	
MDQS0_4_P	AL16	MEM_A_DQS_P<4>	
MDQS0_4_N	AK16	MEM_A_DQS_N<4>	
MDQS0_3_P	AH28	MEM_A_DQS_P<3>	
MDQS0_3_N	AJ28	MEM_A_DQS_N<3>	
MDQS0_2_P	AM29	MEM_A_DQS_P<2>	
MDQS0_2_N	AN29	MEM_A_DQS_N<2>	
MDQS0_1_P	AP34	MEM_A_DQS_P<1>	
MDQS0_1_N	AP35	MEM_A_DQS_N<1>	
MDQS0_0_P	AH31	MEM_A_DQS_P<0>	
MDQS0_0_N	AG31	MEM_A_DQS_N<0>	

MRAS0*	AN19	MEM_A_RAS_L	
MCAS0*	AL19	MEM_A_CAS_L	
MWE0*	AL20	MEM_A_WE_L	
MBA0_2	AL25	MEM_A_BA<2>	
MBA0_1	AN20	MEM_A_BA<1>	
MBA0_0	AM19	MEM_A_BA<0>	
MA0_15	AK26	MEM_A_A<15>	
MA0_14	AK25	MEM_A_A<14>	
MA0_13	AJ20	MEM_A_A<13>	
MA0_12	AJ26	MEM_A_A<12>	
MA0_11	AH25	MEM_A_A<11>	
MA0_10	AM20	MEM_A_A<10>	
MA0_9	AH26	MEM_A_A<9>	
MA0_8	AN23	MEM_A_A<8>	
MA0_7	AJ25	MEM_A_A<7>	
MA0_6	AM22	MEM_A_A<6>	
MA0_5	AM23	MEM_A_A<5>	
MA0_4	AN22	MEM_A_A<4>	
MA0_3	AL23	MEM_A_A<3>	
MA0_2	AK22	MEM_A_A<2>	
MA0_1	AK23	MEM_A_A<1>	
MA0_0	AL22	MEM_A_A<0>	

=PP1V05_S0_MCP_M2CLK_DLL

+VIO_M2CLK_DLL_1	AF24	550 mA
+VIO_M2CLK_DLL_2	AG25	

PP1V05_S0_MCP_PLL_FSBMEM

+VIO_PLL_MEM_1	AF25	20 mA
+VIO_PLL_MEM_2	AG26	
+VIO_PLL_FSB_1	AF26	70 mA
+VIO_PLL_FSB_2	AG28	25 mA
+VIO_PLL_CPU_1	AC26	
+VIO_PLL_CPU_2	AD26	25 mA
+VIO_PLL_CPU_3	AE26	
+VIO_PLL_CPU_4	AF27	

MCLK0A_1_P	AH23	MEM_A_CLK_P<1>	
MCLK0A_1_N	AJ23	MEM_A_CLK_N<1>	
MCLK0A_0_P	AJ22	MEM_A_CLK_P<0>	
MCLK0A_0_N	AH22	MEM_A_CLK_N<0>	
MCS0A_1*	AH19	MEM_A_CS_L<1>	
MCS0A_0*	AK20	MEM_A_CS_L<0>	
MODT0A_1	AH20	MEM_A_ODT<1>	
MODT0A_0	AK19	MEM_A_ODT<0>	
MCKE0A_1	AL26	MEM_A_CKE<1>	
MCKE0A_0	AN25	MEM_A_CKE<0>	

OMIT

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MEMORY PARTITION 1

MEM_B_DQ<63>	AP1	MDQ1_63	
MEM_B_DQ<62>	AR3	MDQ1_62	
MEM_B_DQ<61>	AV4	MDQ1_61	
MEM_B_DQ<60>	AU4	MDQ1_60	
MEM_B_DQ<59>	AP3	MDQ1_59	
MEM_B_DQ<58>	AP2	MDQ1_58	
MEM_B_DQ<57>	AU3	MDQ1_57	
MEM_B_DQ<56>	AT4	MDQ1_56	
MEM_B_DQ<55>	AT5	MDQ1_55	
MEM_B_DQ<54>	AT7	MDQ1_54	
MEM_B_DQ<53>	AU8	MDQ1_53	
MEM_B_DQ<52>	AR10	MDQ1_52	
MEM_B_DQ<51>	AV5	MDQ1_51	
MEM_B_DQ<50>	AU5	MDQ1_50	
MEM_B_DQ<49>	AP10	MDQ1_49	
MEM_B_DQ<48>	AT8	MDQ1_48	
MEM_B_DQ<47>	AT10	MDQ1_47	
MEM_B_DQ<46>	AU10	MDQ1_46	
MEM_B_DQ<45>	AR13	MDQ1_45	
MEM_B_DQ<44>	AR14	MDQ1_44	
MEM_B_DQ<43>	AR11	MDQ1_43	
MEM_B_DQ<42>	AP11	MDQ1_42	
MEM_B_DQ<41>	AT11	MDQ1_41	
MEM_B_DQ<40>	AP13	MDQ1_40	
MEM_B_DQ<39>	AV14	MDQ1_39	
MEM_B_DQ<38>	AU14	MDQ1_38	
MEM_B_DQ<37>	AR17	MDQ1_37	
MEM_B_DQ<36>	AP17	MDQ1_36	
MEM_B_DQ<35>	AP14	MDQ1_35	
MEM_B_DQ<34>	AT13	MDQ1_34	
MEM_B_DQ<33>	AP16	MDQ1_33	
MEM_B_DQ<32>	AR16	MDQ1_32	
MEM_B_DQ<31>	AU26	MDQ1_31	
MEM_B_DQ<30>	AT26	MDQ1_30	
MEM_B_DQ<29>	AU29	MDQ1_29	
MEM_B_DQ<28>	AT29	MDQ1_28	
MEM_B_DQ<27>	AV25	MDQ1_27	
MEM_B_DQ<26>	AV26	MDQ1_26	
MEM_B_DQ<25>	AV28	MDQ1_25	
MEM_B_DQ<24>	AV29	MDQ1_24	
MEM_B_DQ<23>	AT31	MDQ1_23	
MEM_B_DQ<22>	AR32	MDQ1_22	
MEM_B_DQ<21>	AT34	MDQ1_21	
MEM_B_DQ<20>	AU34	MDQ1_20	
MEM_B_DQ<19>	AR29	MDQ1_19	
MEM_B_DQ<18>	AR31	MDQ1_18	
MEM_B_DQ<17>	AU32	MDQ1_17	
MEM_B_DQ<16>	AT32	MDQ1_16	
MEM_B_DQ<15>	AV35	MDQ1_15	
MEM_B_DQ<14>	AT35	MDQ1_14	
MEM_B_DQ<13>	AR37	MDQ1_13	
MEM_B_DQ<12>	AP38	MDQ1_12	
MEM_B_DQ<11>	AV34	MDQ1_11	
MEM_B_DQ<10>	AU35	MDQ1_10	
MEM_B_DQ<9>	AR36	MDQ1_9	
MEM_B_DQ<8>	AR38	MDQ1_8	
MEM_B_DQ<7>	AM36	MDQ1_7	
MEM_B_DQ<6>	AM37	MDQ1_6	
MEM_B_DQ<5>	AJ36	MDQ1_5	
MEM_B_DQ<4>	AL36	MDQ1_4	
MEM_B_DQ<3>	AP37	MDQ1_3	
MEM_B_DQ<2>	AP36	MDQ1_2	
MEM_B_DQ<1>	AJ38	MDQ1_1	
MEM_B_DQ<0>	AJ37	MDQ1_0	
MEM_B_DM<7>	AT2	MDQM1_7	
MEM_B_DM<6>	AU7	MDQM1_6	
MEM_B_DM<5>	AV10	MDQM1_5	
MEM_B_DM<4>	AT14	MDQM1_4	
MEM_B_DM<3>	AR28	MDQM1_3	
MEM_B_DM<2>	AV32	MDQM1_2	
MEM_B_DM<1>	AT37	MDQM1_1	
MEM_B_DM<0>	AM38	MDQM1_0	

MDQS1_7_P	AR2	MEM_B_DQS_P<7>	
MDQS1_7_N	AR1	MEM_B_DQS_N<7>	
MDQS1_6_P	AV7	MEM_B_DQS_P<6>	
MDQS1_6_N	AV8	MEM_B_DQS_N<6>	
MDQS1_5_P	AU11	MEM_B_DQS_P<5>	
MDQS1_5_N	AV11	MEM_B_DQS_N<5>	
MDQS1_4_P	AU13	MEM_B_DQS_P<4>	
MDQS1_4_N	AV13	MEM_B_DQS_N<4>	
MDQS1_3_P	AT28	MEM_B_DQS_P<3>	
MDQS1_3_N	AU28	MEM_B_DQS_N<3>	
MDQS1_2_P	AU31	MEM_B_DQS_P<2>	
MDQS1_2_N	AV31	MEM_B_DQS_N<2>	
MDQS1_1_P	AU36	MEM_B_DQS_P<1>	
MDQS1_1_N	AT36	MEM_B_DQS_N<1>	
MDQS1_0_P	AL38	MEM_B_DQS_P<0>	
MDQS1_0_N	AL37	MEM_B_DQS_N<0>	

MRAS1*	AR19	MEM_B_RAS_L	
MCAS1*	AU17	MEM_B_CAS_L	
MWE1*	AT17	MEM_B_WE_L	
MBA1_2	AR25	MEM_B_BA<2>	
MBA1_1	AT19	MEM_B_BA<1>	
MBA1_0	AR20	MEM_B_BA<0>	
MA1_15	AP26	MEM_B_A<15>	
MA1_14	AR26	MEM_B_A<14>	
MA1_13	AV16	MEM_B_A<13>	
MA1_12	AP25	MEM_B_A<12>	
MA1_11	AT23	MEM_B_A<11>	
MA1_10	AP20	MEM_B_A<10>	
MA1_9	AU23	MEM_B_A<9>	
MA1_8	AV22	MEM_B_A<8>	
MA1_7	AV23	MEM_B_A<7>	
MA1_6	AT22	MEM_B_A<6>	
MA1_5	AU22	MEM_B_A<5>	
MA1_4	AP23	MEM_B_A<4>	
MA1_3	AR23	MEM_B_A<3>	
MA1_2	AP22	MEM_B_A<2>	
MA1_1	AR22	MEM_B_A<1>	
MA1_0	AT20	MEM_B_A<0>	

=PP1V5R1V35_S3_MCP_MEM

R1520 1K 5% 1/16W MF-LF 402

MRESET0*	AP4	MEM_RESET_L
MCLK1A_1_P	AU20	MEM_B_CLK_P<1>
MCLK1A_1_N	AV20	MEM_B_CLK_N<1>
MCLK1A_0_P	AU19	MEM_B_CLK_P<0>
MCLK1A_0_N	AV19	MEM_B_CLK_N<0>
MCS1A_1*	AU16	MEM_B_CS_L<1>
MCS1A_0*	AP19	MEM_B_CS_L<0>
MODT1A_1	AT16	MEM_B_ODT<1>
MODT1A_0	AV17	MEM_B_ODT<0>
MCKE1A_1	AU25	MEM_B_CKE<1>
MCKE1A_0	AT25	MEM_B_CKE<0>

=PP1V5R1V35_SW_MCP_MEM

R1510 40.2 1% 1/16W MF-LF 402

R1511 40.2 1% 1/16W MF-LF 402

MCP_MEM_COMP_GND	AG23	MEM_COMP_GND
MCP_MEM_COMP_VDD	AG22	MEM_COMP_VDD

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: MCP Memory Interface

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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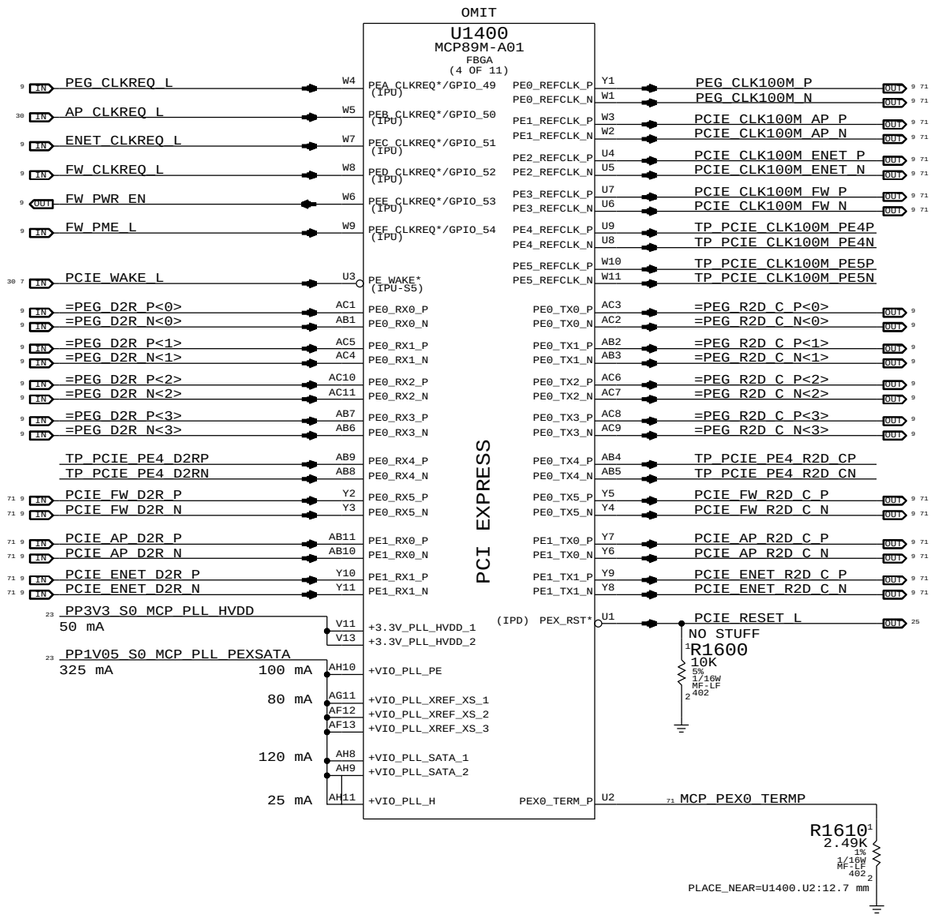

PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-8561 SIZE D
REVISION C.0.0
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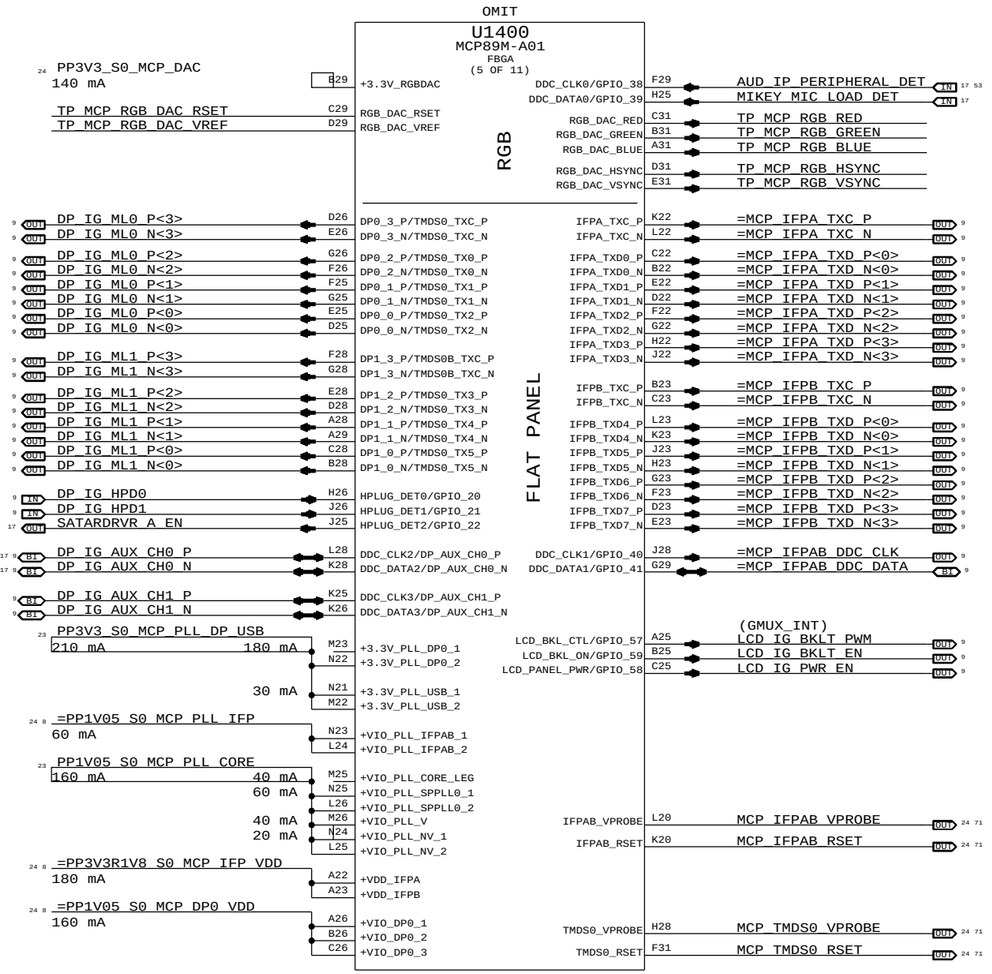


NOTE: 100K pull-downs required if
HPLUG_DET0/HPLUG_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode

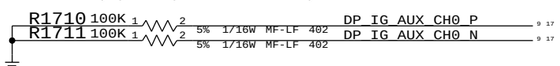
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

NOTE: TMDS/HDMI not supported on IFPA/B for MCP89 A01.

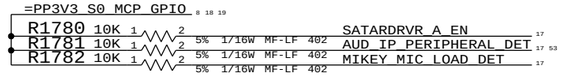
DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.



GPIO Pull-Ups

=PP3V3_S0_MCP_GPIO



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: MCP Graphics

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D
REVISION: C.0.0
BRANCH:
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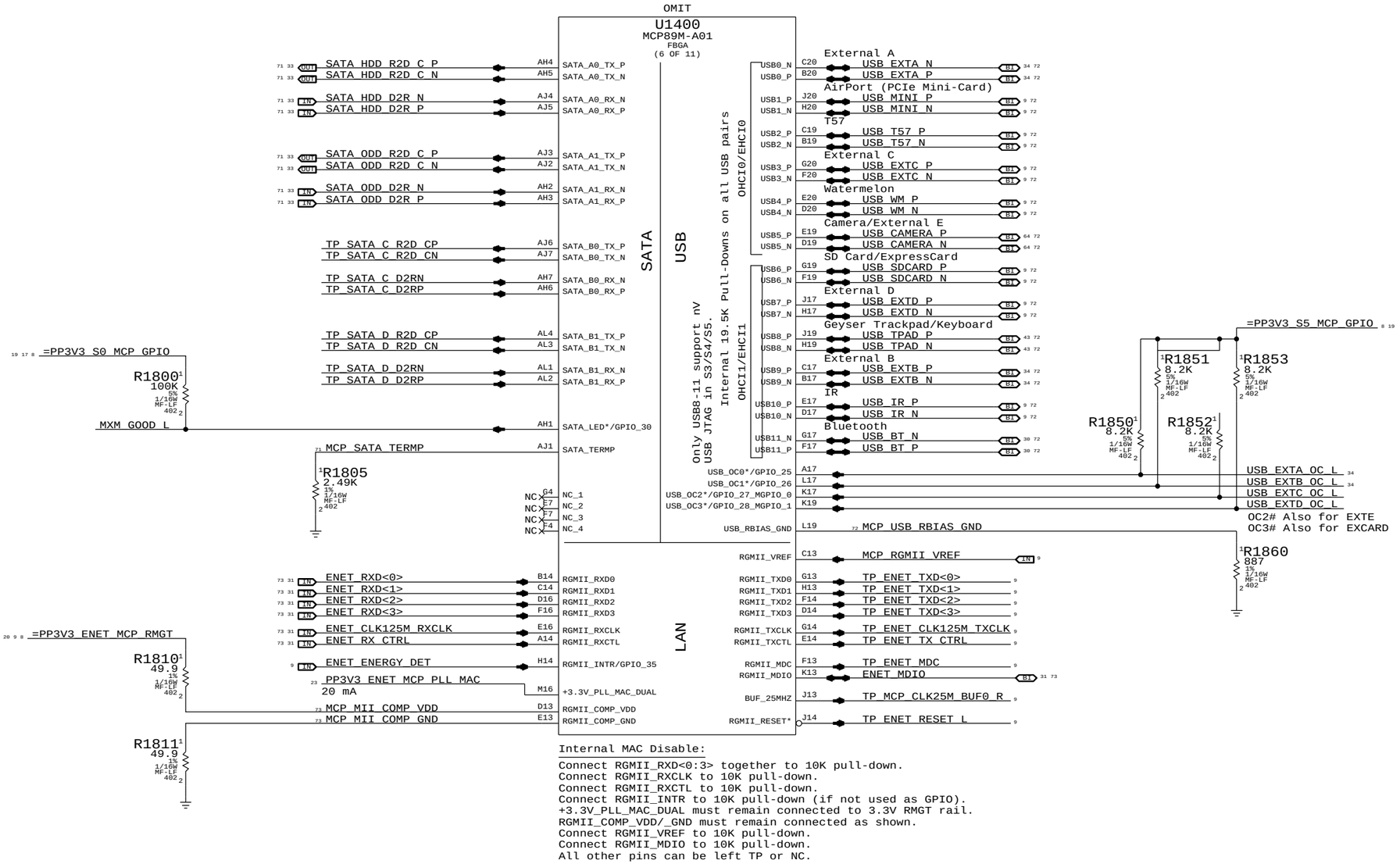

Internal MAC Disable:

Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE
MCP SATA, USB & Ethernet

Apple Inc.

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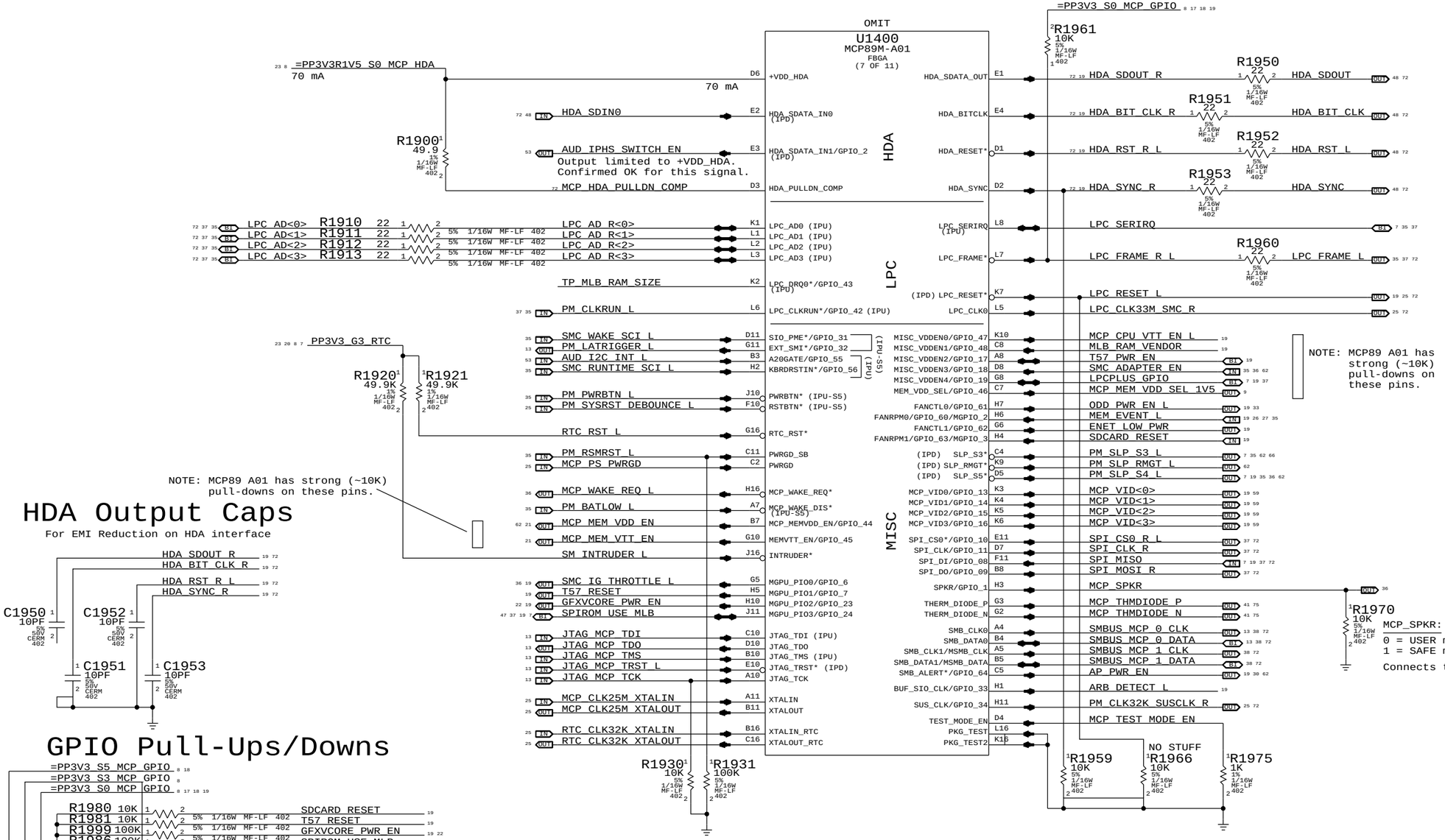

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: MCP HDA, LPC & MISC

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

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NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.

OMIT

U1400
MCP89M-A01
FBGA
(8 OF 11)
POWER I

G32	+VTT_CPU_1	+VDD_MEM_1	AG14
K29	+VTT_CPU_2	+VDD_MEM_2	AL7
D32	+VTT_CPU_3	+VDD_MEM_3	AF18
L29	+VTT_CPU_4	+VDD_MEM_4	AF21
Y26	+VTT_CPU_5	+VDD_MEM_5	AM1
V26	+VTT_CPU_6	+VDD_MEM_6	AM4
P27	+VTT_CPU_7	+VDD_MEM_7	AK8
T27	+VTT_CPU_8	+VDD_MEM_8	AG13
J29	+VTT_CPU_9	+VDD_MEM_9	AF16
N27	+VTT_CPU_10	+VDD_MEM_10	AF22
P26	+VTT_CPU_11	+VDD_MEM_11	AG20
F32	+VTT_CPU_12	+VDD_MEM_12	AM5
A32	+VTT_CPU_13	+VDD_MEM_13	AG19
H29	+VTT_CPU_14	+VDD_MEM_14	AF23
W26	+VTT_CPU_15	+VDD_MEM_15	AJ9
U27	+VTT_CPU_16	+VDD_MEM_16	AF19
G31	+VTT_CPU_17	+VDD_MEM_17	AG17
C32	+VTT_CPU_18	+VDD_MEM_18	AL6
E32	+VTT_CPU_19	+VDD_MEM_19	AG16
M28	+VTT_CPU_20	+VDD_MEM_20	AH12
H30	+VTT_CPU_21	+VDD_MEM_21	AM2
U26	+VTT_CPU_22	+VDD_MEM_22	AF15
T26	+VTT_CPU_23	+VDD_MEM_23	AM3
H31	+VTT_CPU_24	+VDD_MEM_24	AL5
B32	+VTT_CPU_25	+VDD_MEM_25	AL8
R26	+VTT_CPU_26	+VDD_MEM_26	AF17
N26	+VTT_CPU_27	+VDD_MEM_27	AJ11
		+VDD_MEM_28	AJ8
		+VDD_MEM_29	AF14
W27	+VTT_CPU2_1	+VDD_MEM_30	AJ10
W28	+VTT_CPU2_2	+VDD_MEM_31	AF20
Y27	+VTT_CPU2_3		
Y28	+VTT_CPU2_4		

23 8 =PP1V05_SW_MCP_FSB
2000 mA

=PP1V5R1V35_SW_MCP_MEM 15 21 23
4300 mA

23 14 8 =PP1V05_S0_MCP_FSB
200 mA

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators.
Instead connect regulator sense point as close to COREB FET as possible.

OMIT

U1400
MCP89M-A01
FBGA
(9 OF 11)
POWER II

23 8 =PPVCORE_S0_MCP
8450 mA (0.85V)

T3	+VDD_COREA_1	+VDD_COREB_1	M4
AB22	+VDD_COREA_2	+VDD_COREB_2	M2
AB20	+VDD_COREA_3	+VDD_COREB_3	P4
R13	+VDD_COREA_4	+VDD_COREB_4	N12
R7	+VDD_COREA_5	+VDD_COREB_5	N4
T6	+VDD_COREA_6	+VDD_COREB_6	N14
T13	+VDD_COREA_7	+VDD_COREB_7	V20
R11	+VDD_COREA_8	+VDD_COREB_8	N10
AB17	+VDD_COREA_9	+VDD_COREB_9	P3
R10	+VDD_COREA_10	+VDD_COREB_10	P1
AB18	+VDD_COREA_11	+VDD_COREB_11	N11
T1	+VDD_COREA_12	+VDD_COREB_12	N6
T2	+VDD_COREA_13	+VDD_COREB_13	P6
AB21	+VDD_COREA_14	+VDD_COREB_14	N2
R4	+VDD_COREA_15	+VDD_COREB_15	N9
AB19	+VDD_COREA_16	+VDD_COREB_16	N8
P13	+VDD_COREA_17	+VDD_COREB_17	M10
R2	+VDD_COREA_18	+VDD_COREB_18	N3
T8	+VDD_COREA_19	+VDD_COREB_19	N1
R8	+VDD_COREA_20	+VDD_COREB_20	M5
T4	+VDD_COREA_21	+VDD_COREB_21	M7
R5	+VDD_COREA_22	+VDD_COREB_22	P2
T7	+VDD_COREA_23	+VDD_COREB_23	M8
T5	+VDD_COREA_24	+VDD_COREB_24	M11
T9	+VDD_COREA_25	+VDD_COREB_25	V19
U22	+VDD_COREA_26	+VDD_COREB_26	N7
V22	+VDD_COREA_27	+VDD_COREB_27	N16
W22	+VDD_COREA_28	+VDD_COREB_28	P5
Y22	+VDD_COREA_29	+VDD_COREB_29	N5
AA22	+VDD_COREA_30	+VDD_COREB_30	N13
P12	+VDD_COREA_31	+VDD_COREB_31	N15
P10	+VDD_COREA_32	+VDD_COREB_32	P9
P11	+VDD_COREA_33	+VDD_COREB_33	V17
		+VDD_COREB_34	V18
		+VDD_COREB_35	M14
		+VDD_COREB_36	M13
		+VDD_COREB_37	Y19
		+VDD_COREB_38	Y20
		+VDD_COREB_39	Y17
		+VDD_COREB_40	Y18
		+VDD_COREB_41	P7
		+VDD_COREB_42	P8

=PPVCORE_SW_MCP_GFX 22 24
15350 mA (0.85V)

TP_MCP_VDDCOREA_SENSEP L10 +VDD_COREA_SENSE
TP_MCP_VDDCOREA_SENSEN L9 GND_COREA_SENSE

8 =PP1V05_S0_MCP_PE_DVDD0
200 mA (DVDD0 & DVDD1)
(PE0[3:0])
Okay to GND if not using PE0[3:0]
CKPLUS_WAIVE=PwrTerm2Gnd

AF7	+VIO_PE_DVDD0_1	
AF8	+VIO_PE_DVDD0_2	
AE9	+VIO_PE_DVDD0_3	
AE10	+VIO_PE_DVDD0_4	

8 =PP1V05_S0_MCP_PE_DVDD1
200 mA (DVDD0 & DVDD1)
(PE0[5:4], PE1[1:0])

AE6	+VIO_PE_DVDD1_1	
AE7	+VIO_PE_DVDD1_2	
AE8	+VIO_PE_DVDD1_3	

8 =PP1V05_S0_MCP_PE_AVDD0
500 mA (AVDD0 & AVDD1)
(PE0[3:0])
Okay to GND if not using PE0[3:0]
CKPLUS_WAIVE=PwrTerm2Gnd

AC13	+VIO_PE_AVDD0_1	
AB12	+VIO_PE_AVDD0_2	
AC12	+VIO_PE_AVDD0_3	
AD11	+VIO_PE_AVDD0_4	
AD13	+VIO_PE_AVDD0_5	
AB13	+VIO_PE_AVDD0_6	

8 =PP1V05_S0_MCP_PE_AVDD1
500 mA (AVDD0 & AVDD1)
(PE0[5:4], PE1[1:0])

Y12	+VIO_PE_AVDD1_1	
Y13	+VIO_PE_AVDD1_2	
AA13	+VIO_PE_AVDD1_3	
W12	+VIO_PE_AVDD1_4	
W13	+VIO_PE_AVDD1_5	

23 8 =PP3V3_S0_MCP_HVDD
30 mA

T11	+3.3V_HVDD_1	
T12	+3.3V_HVDD_2	
U13	+3.3V_HVDD_3	

23 8 =PP3V3_S0_MCP
250 mA

U11	+3.3V_1	
U12	+3.3V_2	
F5	+3.3V_3	
E29	+3.3V_4	
E5	+3.3V_5	

23 8 =PP0V9_S5_MCP_VDD_AUXC
150 mA

U11	+VDD_DUAL_AUXC_1	
M17	+VDD_DUAL_AUXC_2	
M20	+VDD_DUAL_AUXC_3	

23 19 8 7 PP3V3_G3_RTC
?? uA (G3)
5 mA (S0)

A16	+3.3V_VBAT	

AE1	+VIO_SATA_AVDD_1	
AE2	+VIO_SATA_AVDD_2	
AE3	+VIO_SATA_AVDD_3	
AE4	+VIO_SATA_AVDD_4	
AE5	+VIO_SATA_AVDD_5	
AF1	+VIO_SATA_DVDD_1	
AF2	+VIO_SATA_DVDD_2	
AF3	+VIO_SATA_DVDD_3	
AF4	+VIO_SATA_DVDD_4	
AF5	+VIO_SATA_DVDD_5	
AF6	+VIO_SATA_DVDD_6	
AF9	+VIO_SATA_DVDD_7	
AF10	+VIO_SATA_DVDD_8	
AF11	+VIO_SATA_DVDD_9	
AE11	+VIO_SATA_DVDD_10	
AE12	+VIO_SATA_DVDD_11	
AE13	+VIO_SATA_DVDD_12	
L12	+VDD_DUAL_RMGT_1	
L13	+VDD_DUAL_RMGT_2	
A13	+3.3V_DUAL_RMGT_1	
B13	+3.3V_DUAL_RMGT_2	
A20	+3.3V_DUAL_USB_1	
A19	+3.3V_DUAL_USB_2	
F8	+3.3V_DUAL_1	
E8	+3.3V_DUAL_2	
U10	+VDD_COREB_SENSE	TP_MCP_VDDCOREB_SENSEP
T10	GND_COREB_SENSE	TP_MCP_VDDCOREB_SENSEN

PP1V05_S0_MCP_SATA_AVDD 23
300 mA

=PP1V05_S0_MCP_SATA_DVDD 8 23
100 mA

=PP0V9_ENET_MCP_RMGT 8 23
140 mA

=PP3V3_ENET_MCP_RMGT 8 9 18 23
300 mA

=PP3V3_S5_MCP 8 23
200 mA 240 mA

40 mA

OMIT

U1400
MCP89M-A01
FBGA
(10 OF 11)
GND

AP21	GND_1	GND_68	AD7
M37	GND_2	GND_69	B12
AM21	GND_3	GND_70	D12
AU37	GND_4	GND_71	E12
AC27	GND_5	GND_72	G12
D18	GND_6	GND_73	A2
B1	GND_7	GND_74	AL12
AD5	GND_8	GND_75	AM6
J2	GND_9	GND_76	AD37
AT1	GND_10	GND_77	AG32
AM30	GND_11	GND_78	H12
C1	GND_12	GND_79	AR35
AT3	GND_13	GND_80	H9
AP24	GND_14	GND_81	G24
AM33	GND_15	GND_82	V10
AE27	GND_16	GND_83	V5
AJ24	GND_17	GND_84	AL30
AH18	GND_18	GND_85	G7
AA8	GND_19	GND_86	V29
AM18	GND_20	GND_87	AP15
B6	GND_21	GND_88	AN2
J32	GND_22	GND_89	AJ12
AJ21	GND_23	GND_90	AR15
AK35	GND_24	GND_91	N20
H15	GND_25	GND_92	D21
D33	GND_26	GND_93	E21
E18	GND_27	GND_94	G21
M32	GND_28	GND_95	H21
B2	GND_29	GND_96	AR27
E6	GND_30	GND_97	AM27
J5	GND_31	GND_98	AP27
K18	GND_32	GND_99	AM15
AN34	GND_33	GND_100	AA31
AD10	GND_34	GND_101	AM9
F34	GND_35	GND_102	AH24
V8	GND_36	GND_103	K12
R35	GND_37	GND_104	J31
AR9	GND_38	GND_105	E30
AA2	GND_39	GND_106	AK7
AA10	GND_40	GND_107	V7
R32	GND_41	GND_108	M31
AG29	GND_42	GND_109	AU12
H8	GND_43	GND_110	AP6
AP12	GND_44	GND_111	B37
AM12	GND_45	GND_112	A36
AH21	GND_46	GND_113	F35
V32	GND_47	GND_114	L27
AR33	GND_48	GND_115	D35
J7	GND_49	GND_116	AL24
AA32	GND_50	GND_117	AP30
AG34	GND_51	GND_118	AH15
AK37	GND_52	GND_119	B21
K24	GND_53	GND_120	AV3
K21	GND_54	GND_121	AT38
J8	GND_55	GND_122	B38
AG8	GND_56	GND_123	AA21
AN5	GND_57	GND_124	AD4
V2	GND_58	GND_125	A37
AD32	GND_59	GND_126	AP18
AD2	GND_60	GND_127	AN4
D15	GND_61	GND_128	B24
AG2	GND_62	GND_129	D30
L15	GND_63	GND_130	V4
AK32	GND_64	GND_131	AA7
AR12	GND_65	GND_132	AD34
AN35	GND_66	GND_133	AK4
AN37	GND_67	GND_134	R37

OMIT

U1400
MCP89M-A01
FBGA
(11 OF 11)
GND

AU24	GND_135	GND_200	E33
AU15	GND_136	GND_201	M35
AG5	GND_137	GND_202	AV2
AD35	GND_138	GND_203	AK2
AJ18	GND_139	GND_204	AU6
AL18	GND_140	GND_205	F37
AR24	GND_141	GND_206	C3
AA5	GND_142	GND_207	J37
G18	GND_143	GND_208	V35
B9	GND_144	GND_209	G27
AU9	GND_145	GND_210	AA35
AM24	GND_146	GND_211	AU18
H24	GND_147	GND_212	AR6
B30	GND_148	GND_213	AV36
AR21	GND_149	GND_214	B33
D24	GND_150	GND_215	AJ27
AU30	GND_151	GND_216	G9
AK5	GND_152	GND_217	AG35
N18	GND_153	GND_218	AG7
E24	GND_154	GND_219	AD8
K15	GND_155	GND_220	AU2
M19	GND_156	GND_221	AP9
AH27	GND_157	GND_222	AD31
E18	GND_158	GND_223	V37
AA34	GND_159	GND_224	AA37
AK31	GND_160	GND_225	AG37
K11	GND_161	GND_226	AL15
AU21	GND_162	GND_227	AR18
V34	GND_163	GND_228	L14
AL21	GND_164	GND_229	K14
AA11	GND_165	GND_230	F2
M34	GND_166	GND_231	K27
B27	GND_167	GND_232	AL9
V28	GND_168	GND_233	AB26
C38	GND_169	GND_234	M29
D27	GND_170	GND_235	G30
R34	GND_171	GND_236	R28
J35	GND_172	GND_237	R29
AK34	GND_173	GND_238	R31
E15	GND_174	GND_239	U17
AR30	GND_175	GND_240	K8
AU33	GND_176	GND_241	Y21
J34	GND_177	GND_242	V31
AH30	GND_178	GND_243	U18
J4	GND_179	GND_244	W21
AU27	GND_180	GND_245	U19
AU1	GND_181	GND_246	W18
AG10	GND_182	GND_247	U20
E9	GND_183	GND_248	W17
E27	GND_184	GND_249	V21
L21	GND_185	GND_250	AA28
AU38	GND_186	GND_251	AA29
H18	GND_187	GND_252	N17
E15	GND_188	GND_253	AD28
AA4	GND_189	GND_254	AD29
AJ15	GND_190	GND_255	AG4
L18	GND_191	GND_256	W19
A3	GND_192	GND_257	W20
G15	GND_193	GND_258	AA26
AU27	GND_194	GND_259	AB27
AV37	GND_195	GND_260	AA17
D9	GND_196	GND_261	AA18
L4	GND_197	GND_262	AA19
N19	GND_198	GND_263	AA20
H27	GND_199	GND_264	U21

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE
MCP Power & Ground

Apple Inc.

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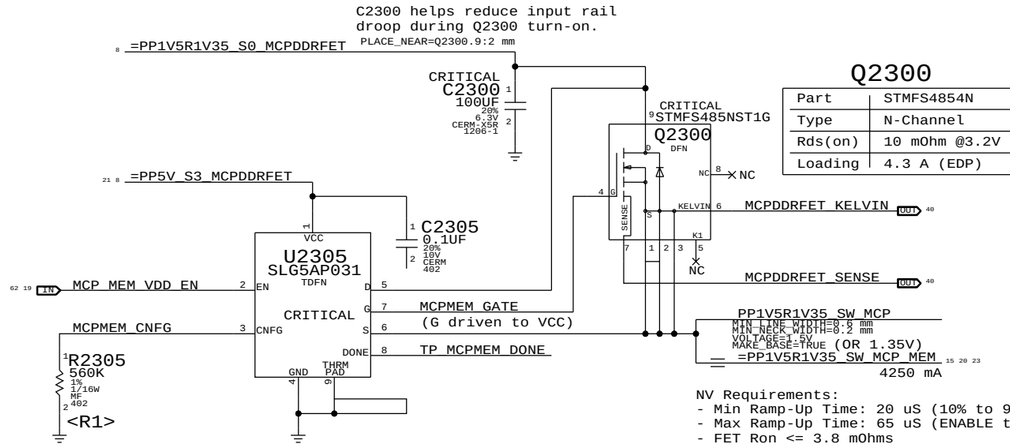


Q2300

Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

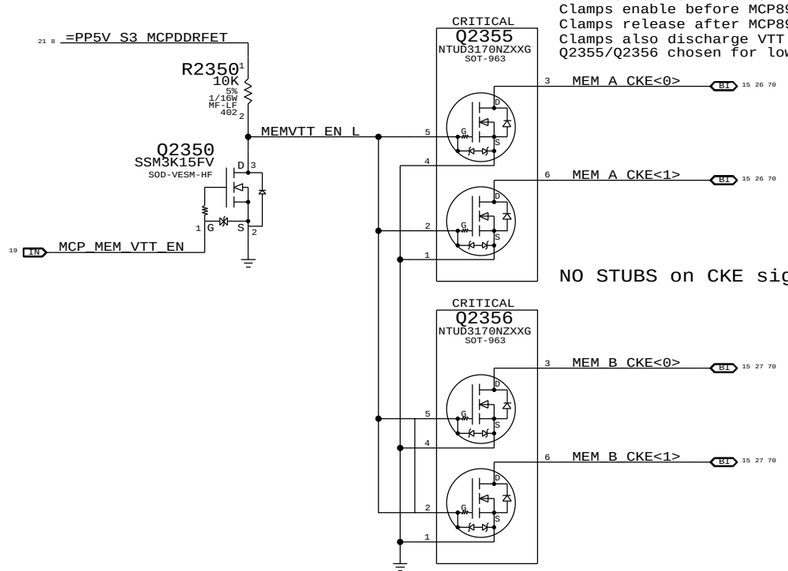
NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.



SYNC_MASTER=K6_MLB SYNC_DATE=02/16/2010

PAGE TITLE: MCP89 Memory Rail Gating

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

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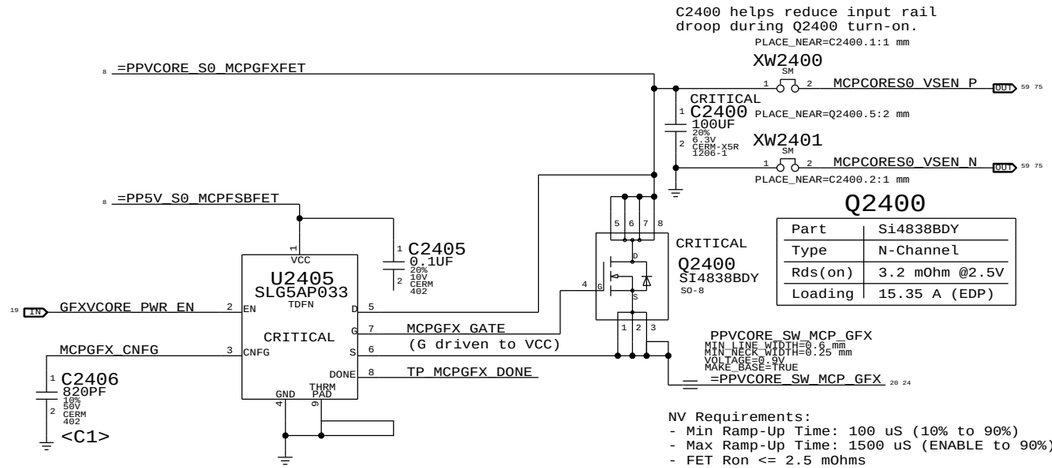

C2400 helps reduce input rail droop during Q2400 turn-on.

Q2400	
Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC_MASTER=T27_MLB SYNC_DATE=12/15/2009

PAGE TITLE
MCP89 GFX Core Rail Gating

Apple Inc.

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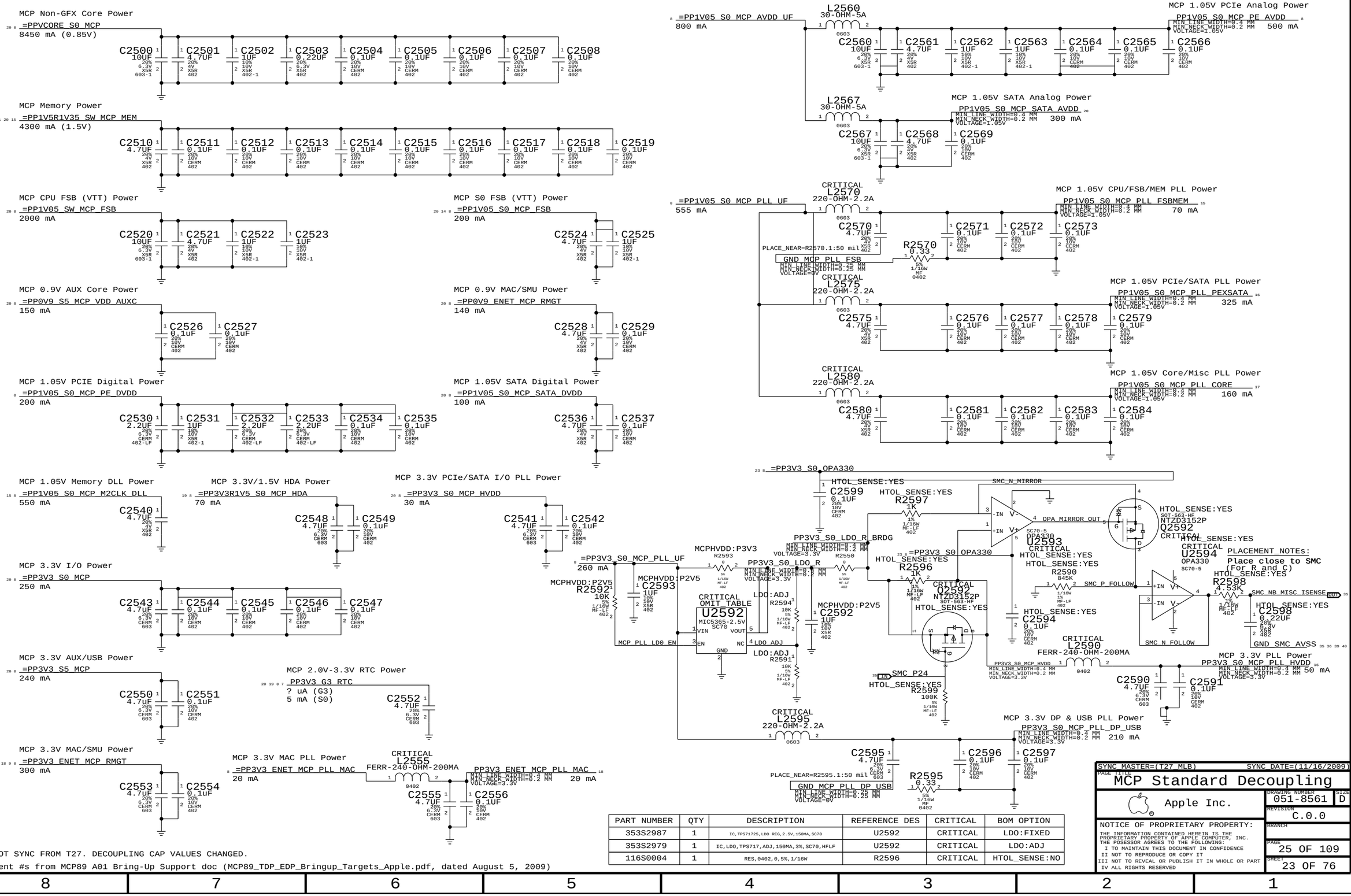

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2987	1	IC,TPS71725,LDO REG,2.5V,150MA,SC70	U2592	CRITICAL	LDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HFLF	U2592	CRITICAL	LDO:ADJ
116S0004	1	RES,0402,0,5%,1/16W	R2596	CRITICAL	HTOL_SENSE:NO

MCP GFX Core Power

22 20 =PPVCORE_SW_MCP_GFX
15350 mA (0.85V)

C2600 10UF 20% 6.3V X5R 603-1
C2601 4.7UF 20% 4V X5R 402
C2602 1UF 10% 10V X5R 402-1
C2603 1UF 10% 10V X5R 402-1
C2604 0.22UF 20% 6.3V X5R 402
C2605 0.22UF 20% 6.3V X5R 402
C2606 0.1UF 20% 10V CERM 402
C2607 0.1UF 20% 10V CERM 402
C2608 0.1UF 20% 10V CERM 402
C2609 0.1UF 20% 10V CERM 402
C2610 0.1UF 20% 10V CERM 402
C2611 0.1UF 20% 10V CERM 402
C2612 0.1UF 20% 10V CERM 402

MCP 3.3V RGBDAC Power

GND_MCP_DAC_P3V3 = PP3V3_S0_MCP_DAC 17
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
MAKE_BASE=TRUE
140 mA

R2670 0 5% 1/16W MF-LF 402

If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.

If RGBDAC is not used, tie to GND.

MCP 3.3V/1.8V IFP Interface Power

17 8 =PP3V3R1V8_S0_MCP_IFP_VDD
180 mA (1.8V LVDS)

C2620 4.7UF 20% 6.3V CERM 603
C2621 0.1UF 20% 10V CERM 402

MCP 1.05V IFP PLL Power

17 8 =PP1V05_S0_MCP_PLL_IFP
60 mA

C2630 4.7UF 20% 4V X5R 402
C2631 0.1UF 20% 10V CERM 402

MCP 1.05V DisplayPort Power

17 8 =PP1V05_S0_MCP_DP0_VDD
160 mA

C2640 4.7UF 20% 4V X5R 402
C2641 0.1UF 20% 10V CERM 402

71 17 MCP_TMDS0_RSET
71 17 MCP_TMDS0_VPROBE

NO STUFF
C2650 0.1UF 20% 10V CERM 402
R2650 1K 1% 1/16W MF-LF 402

71 17 MCP_IFPAB_RSET
71 17 MCP_IFPAB_VPROBE

NO STUFF
C2655 0.1UF 20% 10V CERM 402
NO STUFF
R2655 1K 1% 1/16W MF-LF 402

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE
MCP Graphics Support

Apple Inc.

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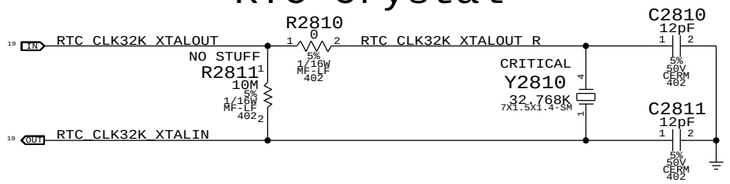
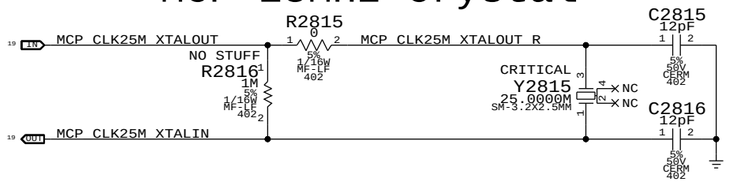
RTC Crystal

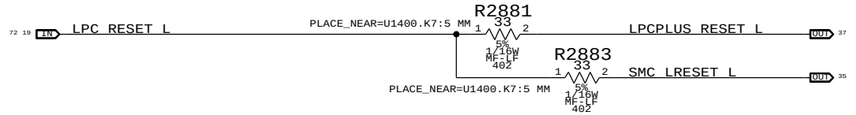


MCP 25MHz Crystal

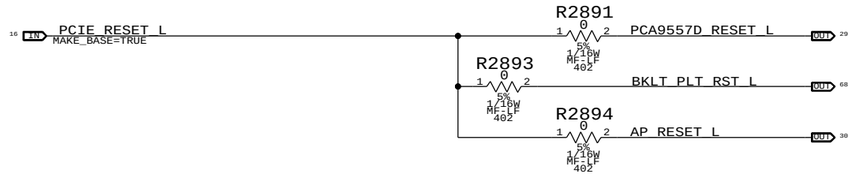


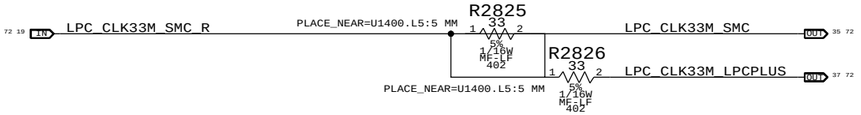
Platform Reset Connections

LPC Reset (Unbuffered)

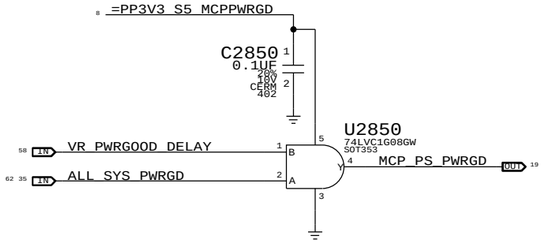


PCIE Reset (Unbuffered)

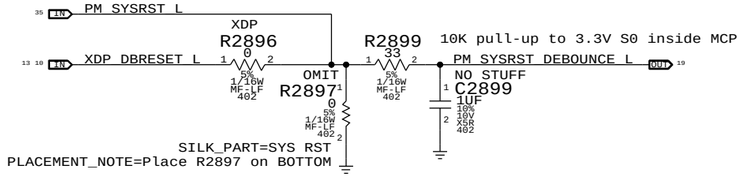




MCP S0 PWRGD & CPU_VLD



System Reset Circuit



DO NOT SYNC WTIH T27. REMOVED PCIE RESET SIGNALS +CAESAR XTAL

SYNC_MASTER=(T27_MLB) SYNC_DATE=(10/07/2009)

PAGE TITLE: SB Misc

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPLVDDR_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)
NOTE: J3100 is OMITted on this page.
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)

=PPLVDDR_S3_MEM_A

C2900 10UF 20% 6.3V X5R 603 1 2
C2901 10UF 20% 6.3V X5R 603 1 2
C2910 0.1UF 20% 10V CERM 402 2 1
C2911 0.1UF 20% 10V CERM 402 2 1
C2912 0.1UF 20% 10V CERM 402 2 1
C2913 0.1UF 20% 10V CERM 402 2 1
C2914 0.1UF 20% 10V CERM 402 2 1
C2915 0.1UF 20% 10V CERM 402 2 1
C2916 0.1UF 20% 10V CERM 402 2 1
C2917 0.1UF 20% 10V CERM 402 2 1
C2918 0.1UF 20% 10V CERM 402 2 1
C2919 0.1UF 20% 10V CERM 402 2 1
C2920 0.1UF 20% 10V CERM 402 2 1
C2921 0.1UF 20% 10V CERM 402 2 1
C2922 0.1UF 20% 10V CERM 402 2 1
C2923 0.1UF 20% 10V CERM 402 2 1

=PPDDRVTT_S0_MEM_A

PPVREF_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF 1 2
C2931 0.1UF 20% 10V CERM 402 1 2

PPVREF_S3_MEM_VREFCA_A

C2936 0.1UF 20% 10V CERM 402 1 2
C2935 2.2UF 20% 6.3V CERM 402-LF 1 2

=PPSPD_S0_MEM_A

C2940 2.2UF 20% 6.3V CERM 402-LF 1 2
R2940 10K 5% 1/16W MF-LF 402 1 2
R2941 10K 5% 1/16W MF-LF 2402 1 2

SPD Addr: 0xA0(Wr)/0xA1(Rd)

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

KEY
CRITICAL
OMIT
J2900
F-RT-THB

MEM_A_CKE<0>	73 CKE0	CKE1 74	MEM_A_CKE<1>
	75 VDD	VDD 76	
NCX	77 NC	A15 78	MEM_A_A<15>
MEM_A_BA<2>	79 BA2	A14 80	MEM_A_A<14>
	81 VDD	VDD 82	
MEM_A_A<12>	83 A12/BC*	A11 84	MEM_A_A<11>
MEM_A_A<9>	85 A9	A7 86	MEM_A_A<7>
	87 VDD	VDD 88	
MEM_A_A<8>	89 A8	A6 90	MEM_A_A<6>
MEM_A_A<5>	91 A5	A4 92	MEM_A_A<4>
	93 VDD	VDD 94	
MEM_A_A<3>	95 A3	A2 96	MEM_A_A<2>
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	99 VDD	VDD 100	
MEM_A_CLK_P<0>	101 CK0	CK1 102	MEM_A_CLK_P<1>
MEM_A_CLK_N<0>	103 CK0*	CK1* 104	MEM_A_CLK_N<1>
	105 VDD	VDD 106	
MEM_A_A<10>	107 A10/AP	BA1 108	MEM_A_BA<1>
MEM_A_BA<0>	109 BA0	RAS* 110	MEM_A_RAS_L
	111 VDD	VDD 112	
MEM_A_WE_L	113 WE*	S0* 114	MEM_A_CS_L<0>
MEM_A_CAS_L	115 CAS*	ODT0 116	MEM_A_ODT<0>
	117 VDD	VDD 118	
MEM_A_A<13>	119 A13	ODT1 120	MEM_A_ODT<1>
MEM_A_CS_L<1>	121 S1*	NC 122 NC	
	123 VDD	VDD 124	
NCX	125 TEST	VREFCA 126	PPVREF_S3_MEM_VREFCA_A
	127 VSS	VSS 128	
=MEM_A_DQ<32>	129 DQ32	DQ36 130	=MEM_A_DQ<36>
=MEM_A_DQ<33>	131 DQ33	DQ37 132	=MEM_A_DQ<37>
	133 VSS	VSS 134	
=MEM_A_DQS_N<4>	135 DQS4*	DM4 136	=MEM_A_DM<4>
=MEM_A_DQS_P<4>	137 DQS4	VSS 138	
	139 VSS	DQ38 140	=MEM_A_DQ<38>
=MEM_A_DQ<34>	141 DQ34	DQ39 142	=MEM_A_DQ<39>
=MEM_A_DQ<35>	143 DQ35	VSS 144	
	145 VSS	DQ44 146	=MEM_A_DQ<44>
=MEM_A_DQ<40>	147 DQ40	DQ45 148	=MEM_A_DQ<45>
=MEM_A_DQ<41>	149 DQ41	VSS 150	
	151 VSS	DQS5* 152	=MEM_A_DQS_N<5>
=MEM_A_DM<5>	153 DM5	DQS5 154	=MEM_A_DQS_P<5>
	155 VSS	VSS 156	
=MEM_A_DQ<42>	157 DQ42	DQ46 158	=MEM_A_DQ<46>
=MEM_A_DQ<43>	159 DQ43	DQ47 160	=MEM_A_DQ<47>
	161 VSS	VSS 162	
=MEM_A_DQ<48>	163 DQ48	DQ52 164	=MEM_A_DQ<52>
=MEM_A_DQ<49>	165 DQ49	DQ53 166	=MEM_A_DQ<53>
	167 VSS	VSS 168	
=MEM_A_DQS_N<6>	169 DQS6*	DM6 170	=MEM_A_DM<6>
=MEM_A_DQS_P<6>	171 DQS6	VSS 172	
	173 VSS	DQ54 174	=MEM_A_DQ<54>
=MEM_A_DQ<50>	175 DQ50	DQ55 176	=MEM_A_DQ<55>
=MEM_A_DQ<51>	177 DQ51	VSS 178	
	179 VSS	DQ60 180	=MEM_A_DQ<60>
=MEM_A_DQ<56>	181 DQ56	DQ61 182	=MEM_A_DQ<61>
=MEM_A_DQ<57>	183 DQ57	VSS 184	
	185 VSS	DQS7* 186	=MEM_A_DQS_N<7>
=MEM_A_DM<7>	187 DM7	DQS7 188	=MEM_A_DQS_P<7>
	189 VSS	VSS 190	
=MEM_A_DQ<58>	191 DQ58	DQ62 192	=MEM_A_DQ<62>
=MEM_A_DQ<59>	193 DQ59	DQ63 194	=MEM_A_DQ<63>
	195 VSS	VSS 196	
MEM_A_SA<0>	197 SA0	EVENT* 198	MEM_EVENT_L
	199 VDDSPD	SDA 200	=I2C_SODIMMA_SDA
MEM_A_SA<1>	201 SA1	SCL 202	=I2C_SODIMMA_SCL
	203 VTT	VTT 204	

Foxconn: 516-0201
Molex: 516-0213

"Factory" (top) slot

DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)

CRITICAL
OMIT
J2900
F-RT-THB

	VREFDQ 1	VSS 2	
	VSS 3	DQ4 4	=MEM_A_DQ<4>
=MEM_A_DQ<0>	DQ0 5	DQ5 6	=MEM_A_DQ<5>
=MEM_A_DQ<1>	VSS 7	VSS 8	
	DQ1 9	DQS0* 10	=MEM_A_DQS_N<0>
=MEM_A_DM<0>	VSS 11	DQS0 12	=MEM_A_DQS_P<0>
	DM0 13	VSS 14	
=MEM_A_DQ<2>	VSS 15	DQ6 16	=MEM_A_DQ<6>
=MEM_A_DQ<3>	DQ2 17	DQ7 18	=MEM_A_DQ<7>
	DQ3 19	VSS 20	
=MEM_A_DQ<8>	VSS 21	DQ12 22	=MEM_A_DQ<12>
=MEM_A_DQ<9>	DQ8 23	DQ13 24	=MEM_A_DQ<13>
	DQ9 25	VSS 26	
=MEM_A_DQS_N<1>	VSS 27	DM1 28	=MEM_A_DM<1>
=MEM_A_DQS_P<1>	DQS1* 29	RESET* 30	MEM_RESET_L
	DQS1 31	VSS 32	
=MEM_A_DQ<10>	VSS 33	DQ14 34	=MEM_A_DQ<14>
=MEM_A_DQ<11>	DQ10 35	DQ15 36	=MEM_A_DQ<15>
	DQ11 37	VSS 38	
=MEM_A_DQ<16>	VSS 39	DQ20 40	=MEM_A_DQ<20>
=MEM_A_DQ<17>	DQ16 41	DQ21 42	=MEM_A_DQ<21>
	DQ17 43	VSS 44	
=MEM_A_DQS_N<2>	VSS 45	DM2 46	=MEM_A_DM<2>
=MEM_A_DQS_P<2>	DQS2* 47	VSS 48	
	DQS2 49	DQ22 50	=MEM_A_DQ<22>
=MEM_A_DQ<18>	VSS 51	DQ23 52	=MEM_A_DQ<23>
=MEM_A_DQ<19>	DQ18 53	VSS 54	
	DQ19 55	DQ28 56	=MEM_A_DQ<28>
=MEM_A_DQ<24>	VSS 57	DQ29 58	=MEM_A_DQ<29>
=MEM_A_DQ<25>	DQ24 59	VSS 60	
	DQ25 61	DQS3* 62	=MEM_A_DQS_N<3>
=MEM_A_DM<3>	VSS 63	DQS3 64	=MEM_A_DQS_P<3>
	DM3 65	VSS 66	
=MEM_A_DQ<26>	VSS 67	DQ30 68	=MEM_A_DQ<30>
=MEM_A_DQ<27>	DQ26 69	DQ31 70	=MEM_A_DQ<31>
	DQ27 71	VSS 72	

KEY

Foxconn: 516-0201
Molex: 516-0213

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE
DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER 051-8561 SIZE D
REVISION C.0.0
BRANCH
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SHEET 26 OF 76

Page Notes

Power aliases required by this page:
- =PPLVDDR_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)
NOTE: J3100 is OMITted on this page.
Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)

=PPLVDDR_S3_MEM_B

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 10% 16V CERM 402
C3111 0.1UF 10% 16V CERM 402
C3112 0.1UF 10% 16V CERM 402
C3113 0.1UF 10% 16V CERM 402
C3114 0.1UF 10% 16V CERM 402
C3115 0.1UF 10% 16V CERM 402
C3116 0.1UF 10% 16V CERM 402
C3117 0.1UF 10% 16V CERM 402
C3118 0.1UF 10% 16V CERM 402
C3119 0.1UF 10% 16V CERM 402
C3120 0.1UF 10% 16V CERM 402
C3121 0.1UF 10% 16V CERM 402
C3122 0.1UF 10% 16V CERM 402
C3123 0.1UF 10% 16V CERM 402

=PPDDRVTT_S0_MEM_B

PPVREF_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 10% 16V CERM 402

PPVREF_S3_MEM_VREFCA_B

C3136 0.1UF 10% 16V CERM 402
C3135 2.2UF 20% 6.3V CERM 402-LF

=PPSPD_S0_MEM_B

R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402
C3140 2.2UF 20% 6.3V CERM 402-LF

SPD Addr: 0xA2(Wr)/0xA3(Rd)

DDR3-SODIMM (2 OF 2) — J3100 CRITICAL OMIT F-RT-BGA3

73	CKE0	MEM_B_CKE<0>		74	CKE1	MEM_B_CKE<1>	
75	VDD			76	VDD		
77	NC	NCX		78	A15	MEM_B_A<15>	
79	BA2	MEM_B_BA<2>		80	A14	MEM_B_A<14>	
81	VDD			82	VDD		
83	A12/BC*	MEM_B_A<12>		84	A11	MEM_B_A<11>	
85	A9	MEM_B_A<9>		86	A7	MEM_B_A<7>	
87	VDD			88	VDD		
89	A8	MEM_B_A<8>		90	A6	MEM_B_A<6>	
91	A5	MEM_B_A<5>		92	A4	MEM_B_A<4>	
93	VDD			94	VDD		
95	A3	MEM_B_A<3>		96	A2	MEM_B_A<2>	
97	A1	MEM_B_A<1>		98	A0	MEM_B_A<0>	
99	VDD			100	VDD		
101	CK0	MEM_B_CLK_P<0>		102	CK1	MEM_B_CLK_P<1>	
103	CK0*	MEM_B_CLK_N<0>		104	CK1*	MEM_B_CLK_N<1>	
105	VDD			106	VDD		
107	A10/AP	MEM_B_A<10>		108	BA1	MEM_B_BA<1>	
109	BA0	MEM_B_BA<0>		110	RAS*	MEM_B_RAS_L	
111	VDD			112	VDD		
113	WE*	MEM_B_WE_L		114	S0*	MEM_B_CS_L<0>	
115	CAS*	MEM_B_CAS_L		116	ODT0	MEM_B_ODT<0>	
117	VDD			118	VDD		
119	A13	MEM_B_A<13>		120	ODT1	MEM_B_ODT<1>	
121	S1*	MEM_B_CS_L<1>		122	NC	NCX	
123	VDD			124	VDD		
125	TEST	NCX		126	VREFCA	PPVREF_S3_MEM_VREFCA_B	
127	VSS			128	VSS		
129	DQ32	=MEM_B_DQ<32>		130	DQ36	=MEM_B_DQ<36>	
131	DQ33	=MEM_B_DQ<33>		132	DQ37	=MEM_B_DQ<37>	
133	VSS			134	VSS		
135	DQS4*	=MEM_B_DQS_N<4>		136	DM4	=MEM_B_DM<4>	
137	DQS4	=MEM_B_DQS_P<4>		138	VSS		
139	VSS			140	DQ38	=MEM_B_DQ<38>	
141	DQ34	=MEM_B_DQ<34>		142	DQ39	=MEM_B_DQ<39>	
143	DQ35	=MEM_B_DQ<35>		144	VSS		
145	VSS			146	DQ44	=MEM_B_DQ<44>	
147	DQ40	=MEM_B_DQ<40>		148	DQ45	=MEM_B_DQ<45>	
149	DQ41	=MEM_B_DQ<41>		150	VSS		
151	VSS			152	DQS5*	=MEM_B_DQS_N<5>	
153	DM5	=MEM_B_DM<5>		154	DQS5	=MEM_B_DQS_P<5>	
155	VSS			156	VSS		
157	DQ42	=MEM_B_DQ<42>		158	DQ46	=MEM_B_DQ<46>	
159	DQ43	=MEM_B_DQ<43>		160	DQ47	=MEM_B_DQ<47>	
161	VSS			162	VSS		
163	DQ48	=MEM_B_DQ<48>		164	DQ52	=MEM_B_DQ<52>	
165	DQ49	=MEM_B_DQ<49>		166	DQ53	=MEM_B_DQ<53>	
167	VSS			168	VSS		
169	DQS6*	=MEM_B_DQS_N<6>		170	DM6	=MEM_B_DM<6>	
171	DQS6	=MEM_B_DQS_P<6>		172	VSS		
173	VSS			174	DQ54	=MEM_B_DQ<54>	
175	DQ50	=MEM_B_DQ<50>		176	DQ55	=MEM_B_DQ<55>	
177	DQ51	=MEM_B_DQ<51>		178	VSS		
179	VSS			180	DQ60	=MEM_B_DQ<60>	
181	DQ56	=MEM_B_DQ<56>		182	DQ61	=MEM_B_DQ<61>	
183	DQ57	=MEM_B_DQ<57>		184	VSS		
185	VSS			186	DQS7*	=MEM_B_DQS_N<7>	
187	DM7	=MEM_B_DM<7>		188	DQS7	=MEM_B_DQS_P<7>	
189	VSS			190	VSS		
191	DQ58	=MEM_B_DQ<58>		192	DQ62	=MEM_B_DQ<62>	
193	DQ59	=MEM_B_DQ<59>		194	DQ63	=MEM_B_DQ<63>	
195	VSS			196	VSS		
197	SA0	MEM_B_SA<0>		198	EVENT*	MEM_EVENT_L	U971 19 26 35
199	VDDSPD			200	SDA	=I2C_SODIMMB_SDA	B 38
201	SA1	MEM_B_SA<1>		202	SCL	=I2C_SODIMMB_SCL	B 38
203	VTT			204	VTT		
205	MTG PIN			206	MTG PIN		
207	MTG PIN			208	MTG PIN		
209	MTG PIN			210	MTG PIN		
211	MTG PIN			212	MTG PIN		

Foxconn: 516s0706
Molex: 516s0790

"Expansion" (bottom) slot

DDR3-SODIMM (1 OF 2) — J3100 CRITICAL OMIT F-RT-BGA3

1	VREFDQ			2	VSS		
3	VSS			4	DQ4	=MEM_B_DQ<4>	
5	DQ0	=MEM_B_DQ<0>		6	DQ5	=MEM_B_DQ<5>	
7	DQ1	=MEM_B_DQ<1>		8	VSS		
9	VSS			10	DQS0*	=MEM_B_DQS_N<0>	
11	DM0	=MEM_B_DM<0>		12	DQS0	=MEM_B_DQS_P<0>	
13	VSS			14	VSS		
15	DQ2	=MEM_B_DQ<2>		16	DQ6	=MEM_B_DQ<6>	
17	DQ3	=MEM_B_DQ<3>		18	DQ7	=MEM_B_DQ<7>	
19	VSS			20	VSS		
21	DQ8	=MEM_B_DQ<8>		22	DQ12	=MEM_B_DQ<12>	
23	DQ9	=MEM_B_DQ<9>		24	DQ13	=MEM_B_DQ<13>	
25	VSS			26	VSS		
27	DQS1*	=MEM_B_DQS_N<1>		28	DM1	=MEM_B_DM<1>	
29	DQS1	=MEM_B_DQS_P<1>		30	RESET*	MEM_RESET_L	
31	VSS			32	VSS		
33	DQ10	=MEM_B_DQ<10>		34	DQ14	=MEM_B_DQ<14>	
35	DQ11	=MEM_B_DQ<11>		36	DQ15	=MEM_B_DQ<15>	
37	VSS			38	VSS		
39	DQ16	=MEM_B_DQ<16>		40	DQ20	=MEM_B_DQ<20>	
41	DQ17	=MEM_B_DQ<17>		42	DQ21	=MEM_B_DQ<21>	
43	VSS			44	VSS		
45	DQS2*	=MEM_B_DQS_N<2>		46	DM2	=MEM_B_DM<2>	
47	DQS2	=MEM_B_DQS_P<2>		48	VSS		
49	VSS			50	DQ22	=MEM_B_DQ<22>	
51	DQ18	=MEM_B_DQ<18>		52	DQ23	=MEM_B_DQ<23>	
53	DQ19	=MEM_B_DQ<19>		54	VSS		
55	VSS			56	DQ28	=MEM_B_DQ<28>	
57	DQ24	=MEM_B_DQ<24>		58	DQ29	=MEM_B_DQ<29>	
59	DQ25	=MEM_B_DQ<25>		60	VSS		
61	VSS			62	DQS3*	=MEM_B_DQS_N<3>	
63	DM3	=MEM_B_DM<3>		64	DQS3	=MEM_B_DQS_P<3>	
65	VSS			66	VSS		
67	DQ26	=MEM_B_DQ<26>		68	DQ30	=MEM_B_DQ<30>	
69	DQ27	=MEM_B_DQ<27>		70	DQ31	=MEM_B_DQ<31>	
71	VSS			72	VSS		

Foxconn: 516s0706
Molex: 516s0790

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D
REVISION: C.0.0
BRANCH:
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Host Partition A 0 -> SO-DIMM A 0

MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<0>	B1	26
MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<0>	B1	26
	MAKE_BASE=TRUE	=			
MEM_A_DM<0>		=	=MEM_A_DM<0>	OUT	26
MEM_A_DQ<0>	MAKE_BASE=TRUE	=	=MEM_A_DQ<0>	B1	26
MEM_A_DQ<1>	MAKE_BASE=TRUE	=	=MEM_A_DQ<1>	B1	26
MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>	B1	26
MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>	B1	26
MEM_A_DQ<4>	MAKE_BASE=TRUE	=	=MEM_A_DQ<4>	B1	26
MEM_A_DQ<5>	MAKE_BASE=TRUE	=	=MEM_A_DQ<5>	B1	26
MEM_A_DQ<6>	MAKE_BASE=TRUE	=	=MEM_A_DQ<6>	B1	26
MEM_A_DQ<7>	MAKE_BASE=TRUE	=	=MEM_A_DQ<7>	B1	26
	MAKE_BASE=TRUE	=			

HOST PARTITION A 1 -> SO-DIMM A 1

MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<1>	B1	26
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<1>	B1	26
MEM_A_DM<1>	MAKE_BASE=TRUE	=	=MEM_A_DM<1>	OUT	26
	MAKE_BASE=TRUE	=			
MEM_A_DQ<8>		=	=MEM_A_DQ<12>	B1	26
MEM_A_DQ<9>	MAKE_BASE=TRUE	=	=MEM_A_DQ<8>	B1	26
MEM_A_DQ<10>	MAKE_BASE=TRUE	=	=MEM_A_DQ<15>	B1	26
MEM_A_DQ<11>	MAKE_BASE=TRUE	=	=MEM_A_DQ<10>	B1	26
MEM_A_DQ<12>	MAKE_BASE=TRUE	=	=MEM_A_DQ<13>	B1	26
MEM_A_DQ<13>	MAKE_BASE=TRUE	=	=MEM_A_DQ<9>	B1	26
MEM_A_DQ<14>	MAKE_BASE=TRUE	=	=MEM_A_DQ<11>	B1	26
MEM_A_DQ<15>	MAKE_BASE=TRUE	=	=MEM_A_DQ<14>	B1	26
	MAKE_BASE=TRUE	=			

HOST PARTITION A 2 -> SO-DIMM A 3

MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<3>	B1	26
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>	B1	26
MEM_A_DM<2>	MAKE_BASE=TRUE	=	=MEM_A_DM<3>	OUT	26
	MAKE_BASE=TRUE	=			
MEM_A_DQ<16>		=	=MEM_A_DQ<24>	B1	26
MEM_A_DQ<17>	MAKE_BASE=TRUE	=	=MEM_A_DQ<30>	B1	26
MEM_A_DQ<18>	MAKE_BASE=TRUE	=	=MEM_A_DQ<26>	B1	26
MEM_A_DQ<19>	MAKE_BASE=TRUE	=	=MEM_A_DQ<27>	B1	26
MEM_A_DQ<20>	MAKE_BASE=TRUE	=	=MEM_A_DQ<29>	B1	26
MEM_A_DQ<21>	MAKE_BASE=TRUE	=	=MEM_A_DQ<28>	B1	26
MEM_A_DQ<22>	MAKE_BASE=TRUE	=	=MEM_A_DQ<25>	B1	26
MEM_A_DQ<23>	MAKE_BASE=TRUE	=	=MEM_A_DQ<31>	B1	26
	MAKE_BASE=TRUE	=			

HOST PARTITION A 3 -> SO-DIMM A 2

MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<2>	B1	26
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<2>	B1	26
MEM_A_DM<3>	MAKE_BASE=TRUE	=	=MEM_A_DM<2>	OUT	26
	MAKE_BASE=TRUE	=			
MEM_A_DQ<24>		=	=MEM_A_DQ<17>	B1	26
MEM_A_DQ<25>	MAKE_BASE=TRUE	=	=MEM_A_DQ<20>	B1	26
MEM_A_DQ<26>	MAKE_BASE=TRUE	=	=MEM_A_DQ<23>	B1	26
MEM_A_DQ<27>	MAKE_BASE=TRUE	=	=MEM_A_DQ<18>	B1	26
MEM_A_DQ<28>	MAKE_BASE=TRUE	=	=MEM_A_DQ<22>	B1	26
MEM_A_DQ<29>	MAKE_BASE=TRUE	=	=MEM_A_DQ<21>	B1	26
MEM_A_DQ<30>	MAKE_BASE=TRUE	=	=MEM_A_DQ<16>	B1	26
MEM_A_DQ<31>	MAKE_BASE=TRUE	=	=MEM_A_DQ<19>	B1	26
	MAKE_BASE=TRUE	=			

Host Partition A 4 -> SO-DIMM A 4

MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<4>	B1	26
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>	B1	26
MEM_A_DM<4>	MAKE_BASE=TRUE	=	=MEM_A_DM<4>	OUT	26
	MAKE_BASE=TRUE	=			
MEM_A_DQ<32>		=	=MEM_A_DQ<33>	B1	26
MEM_A_DQ<33>	MAKE_BASE=TRUE	=	=MEM_A_DQ<32>	B1	26
MEM_A_DQ<34>	MAKE_BASE=TRUE	=	=MEM_A_DQ<34>	B1	26
MEM_A_DQ<35>	MAKE_BASE=TRUE	=	=MEM_A_DQ<35>	B1	26
MEM_A_DQ<36>	MAKE_BASE=TRUE	=	=MEM_A_DQ<36>	B1	26
MEM_A_DQ<37>	MAKE_BASE=TRUE	=	=MEM_A_DQ<37>	B1	26
MEM_A_DQ<38>	MAKE_BASE=TRUE	=	=MEM_A_DQ<38>	B1	26
MEM_A_DQ<39>	MAKE_BASE=TRUE	=	=MEM_A_DQ<39>	B1	26
	MAKE_BASE=TRUE	=			

Host Partition A 5 -> SO-DIMM A 5

MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<5>	B1	26
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<5>	B1	26
MEM_A_DM<5>	MAKE_BASE=TRUE	=	=MEM_A_DM<5>	OUT	26
	MAKE_BASE=TRUE	=			
MEM_A_DQ<40>		=	=MEM_A_DQ<45>	B1	26
MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>	B1	26
MEM_A_DQ<42>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>	B1	26
MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<47>	B1	26
MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<40>	B1	26
MEM_A_DQ<45>	MAKE_BASE=TRUE	=	=MEM_A_DQ<42>	B1	26
MEM_A_DQ<46>	MAKE_BASE=TRUE	=	=MEM_A_DQ<46>	B1	26
MEM_A_DQ<47>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>	B1	26
	MAKE_BASE=TRUE	=			

Host Partition A 6 -> SO-DIMM A 6

MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<6>	B1	26
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<6>	B1	26
MEM_A_DM<6>	MAKE_BASE=TRUE	=	=MEM_A_DM<6>	OUT	26
	MAKE_BASE=TRUE	=			
MEM_A_DQ<48>		=	=MEM_A_DQ<52>	B1	26
MEM_A_DQ<49>	MAKE_BASE=TRUE	=	=MEM_A_DQ<55>	B1	26
MEM_A_DQ<50>	MAKE_BASE=TRUE	=	=MEM_A_DQ<54>	B1	26
MEM_A_DQ<51>	MAKE_BASE=TRUE	=	=MEM_A_DQ<49>	B1	26
MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<48>	B1	26
MEM_A_DQ<53>	MAKE_BASE=TRUE	=	=MEM_A_DQ<53>	B1	26
MEM_A_DQ<54>	MAKE_BASE=TRUE	=	=MEM_A_DQ<51>	B1	26
MEM_A_DQ<55>	MAKE_BASE=TRUE	=	=MEM_A_DQ<50>	B1	26
	MAKE_BASE=TRUE	=			

Host Partition A 7 -> SO-DIMM A 7

MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<7>	B1	26
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<7>	B1	26
MEM_A_DM<7>	MAKE_BASE=TRUE	=	=MEM_A_DM<7>	OUT	26
	MAKE_BASE=TRUE	=			
MEM_A_DQ<56>		=	=MEM_A_DQ<61>	B1	26
MEM_A_DQ<57>	MAKE_BASE=TRUE	=	=MEM_A_DQ<60>	B1	26
MEM_A_DQ<58>	MAKE_BASE=TRUE	=	=MEM_A_DQ<58>	B1	26
MEM_A_DQ<59>	MAKE_BASE=TRUE	=	=MEM_A_DQ<59>	B1	26
MEM_A_DQ<60>	MAKE_BASE=TRUE	=	=MEM_A_DQ<57>	B1	26
MEM_A_DQ<61>	MAKE_BASE=TRUE	=	=MEM_A_DQ<56>	B1	26
MEM_A_DQ<62>	MAKE_BASE=TRUE	=	=MEM_A_DQ<62>	B1	26
MEM_A_DQ<63>	MAKE_BASE=TRUE	=	=MEM_A_DQ<63>	B1	26
	MAKE_BASE=TRUE	=			

Host Partition B 0 -> SO-DIMM B 0

MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<0>	B1	27
MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<0>	B1	27
MEM_B_DM<0>	MAKE_BASE=TRUE	=	=MEM_B_DM<0>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<0>		=	=MEM_B_DQ<0>	B1	27
MEM_B_DQ<1>	MAKE_BASE=TRUE	=	=MEM_B_DQ<1>	B1	27
MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>	B1	27
MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>	B1	27
MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>	B1	27
MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>	B1	27
MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>	B1	27
MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>	B1	27
	MAKE_BASE=TRUE	=			

Host Partition B 1 -> SO-DIMM B 2

MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<2>	B1	27
MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<2>	B1	27
MEM_B_DM<1>	MAKE_BASE=TRUE	=	=MEM_B_DM<2>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<8>		=	=MEM_B_DQ<17>	B1	27
MEM_B_DQ<9>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>	B1	27
MEM_B_DQ<10>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>	B1	27
MEM_B_DQ<11>	MAKE_BASE=TRUE	=	=MEM_B_DQ<23>	B1	27
MEM_B_DQ<12>	MAKE_BASE=TRUE	=	=MEM_B_DQ<21>	B1	27
MEM_B_DQ<13>	MAKE_BASE=TRUE	=	=MEM_B_DQ<20>	B1	27
MEM_B_DQ<14>	MAKE_BASE=TRUE	=	=MEM_B_DQ<22>	B1	27
MEM_B_DQ<15>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>	B1	27
	MAKE_BASE=TRUE	=			

Host Partition B 2 -> SO-DIMM B 3

MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<3>	B1	27
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>	B1	27
MEM_B_DM<2>	MAKE_BASE=TRUE	=	=MEM_B_DM<3>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<16>		=	=MEM_B_DQ<29>	B1	27
MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>	B1	27
MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>	B1	27
MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>	B1	27
MEM_B_DQ<20>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>	B1	27
MEM_B_DQ<21>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>	B1	27
MEM_B_DQ<22>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>	B1	27
MEM_B_DQ<23>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>	B1	27
	MAKE_BASE=TRUE	=			

Host Partition B 3 -> SO-DIMM B 1

MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<1>	B1	27
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<1>	B1	27
MEM_B_DM<3>	MAKE_BASE=TRUE	=	=MEM_B_DM<1>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<24>		=	=MEM_B_DQ<9>	B1	27
MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<13>	B1	27
MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<14>	B1	27
MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<15>	B1	27
MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<8>	B1	27
MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<12>	B1	27
MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<11>	B1	27
MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<10>	B1	27
	MAKE_BASE=TRUE	=			

Host Partition B 4 -> SO-DIMM B 4

MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<4>	B1	27
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>	B1	27
MEM_B_DM<4>	MAKE_BASE=TRUE	=	=MEM_B_DM<4>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<32>		=	=MEM_B_DQ<32>	B1	27
MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>	B1	27
MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<34>	B1	27
MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>	B1	27
MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>	B1	27
MEM_B_DQ<37>	MAKE_BASE=TRUE	=	=MEM_B_DQ<33>	B1	27
MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>	B1	27
MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>	B1	27
	MAKE_BASE=TRUE	=			

Host Partition B 5 -> SO-DIMM B 5

MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<5>	B1	27
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>	B1	27
MEM_B_DM<5>	MAKE_BASE=TRUE	=	=MEM_B_DM<5>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<40>		=	=MEM_B_DQ<41>	B1	27
MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>	B1	27
MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>	B1	27
MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>	B1	27
MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>	B1	27
MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>	B1	27
MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>	B1	27
MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>	B1	27
	MAKE_BASE=TRUE	=			

Host Partition B 6 -> SO-DIMM B 6

MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<6>	B1	27
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>	B1	27
MEM_B_DM<6>	MAKE_BASE=TRUE	=	=MEM_B_DM<6>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<48>		=	=MEM_B_DQ<52>	B1	27
MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>	B1	27
MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>	B1	27
MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>	B1	27
MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>	B1	27
MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>	B1	27
MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>	B1	27
MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>	B1	27
	MAKE_BASE=TRUE	=			

Host Partition B 7 -> SO-DIMM B 7

MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<7>	B1	27
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>	B1	27
MEM_B_DM<7>	MAKE_BASE=TRUE	=	=MEM_B_DM<7>	OUT	27
	MAKE_BASE=TRUE	=			
MEM_B_DQ<56>		=	=MEM_B_DQ<56>	B1	27
MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>	B1	27
MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>	B1	27
MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>	B1	27
MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>	B1	27
MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>	B1	27
MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>	B1	27
MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>	B1	27
	MAKE_BASE=TRUE	=			

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

SO-DIMM Pinswaps

Apple Inc.

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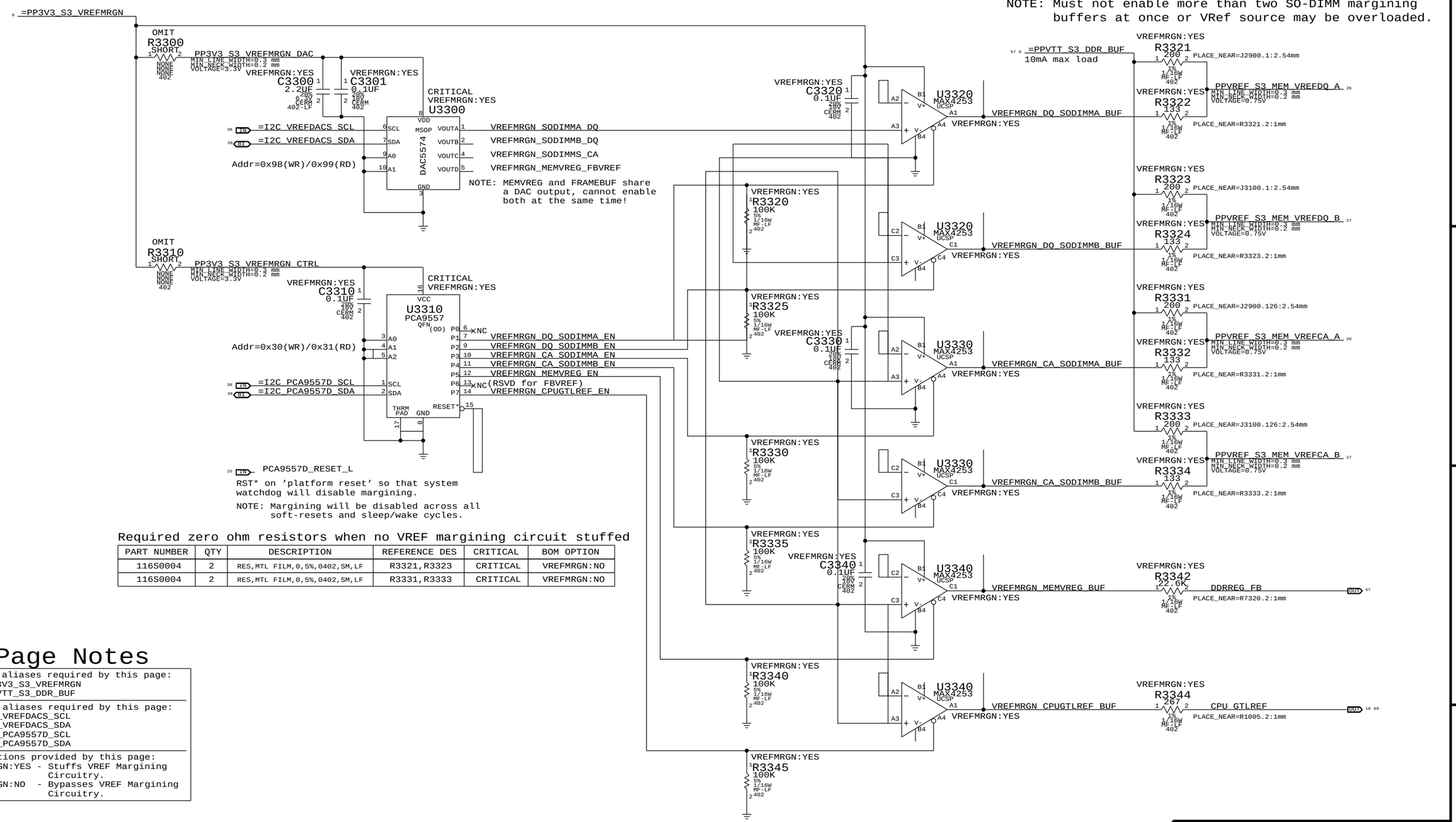

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3321,R3323	CRITICAL	VREFMRGN:NO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3331,R3333	CRITICAL	VREFMRGN:NO

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	9.24mV / step @ output

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010
PAGE TITLE
FSB/DDR3 Vref Margining

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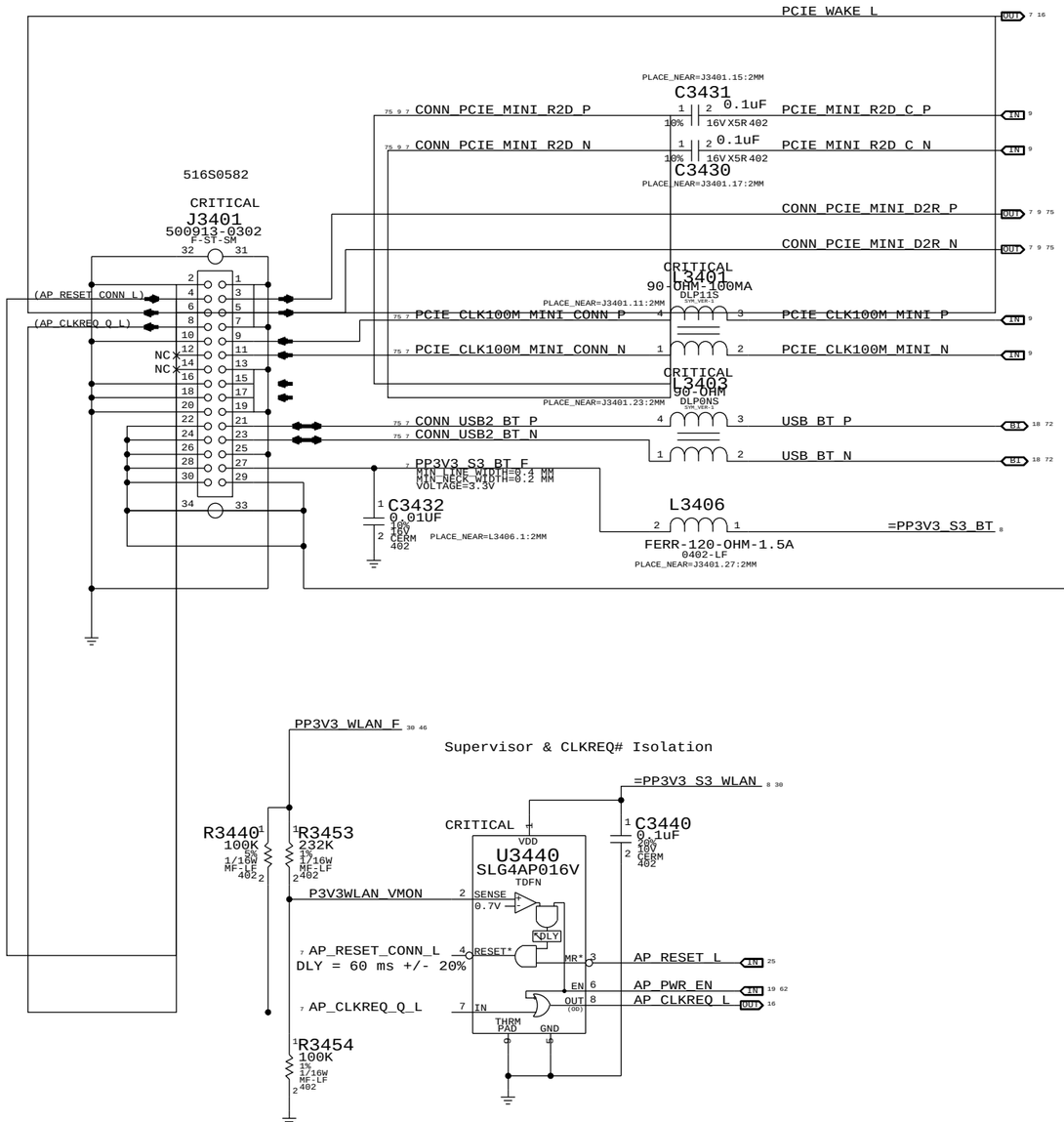

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	1	RES,0OHM,5%,1/4W,MF-LF,1206	R3452		SENS_R:PROD

DO NOT SYNC WITH K84. CHANGED MINI_RESET_CONN_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
X16 WIRELESS CONNECTOR

Apple Inc.

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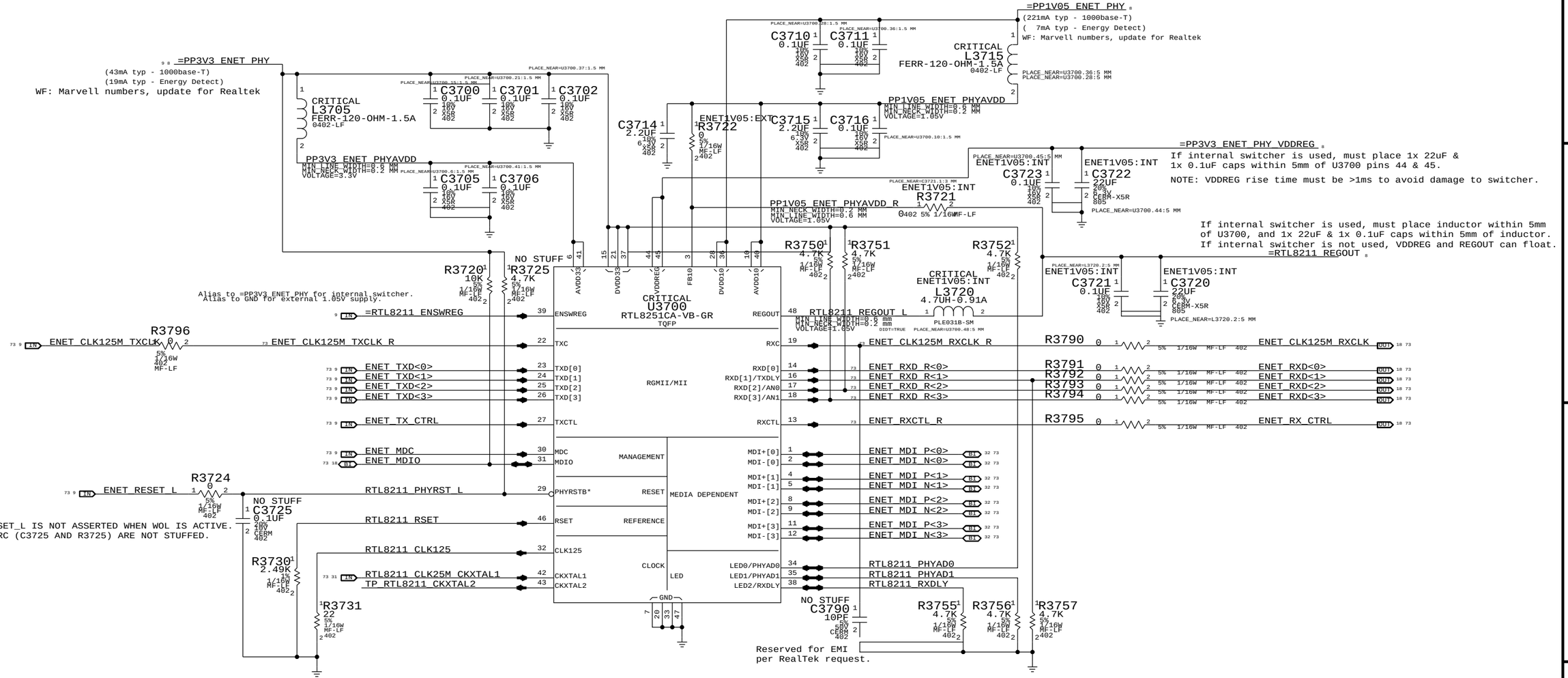
=PP3V3_ENET_PHY
(43mA typ - 1000base-T)
(19mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek
CRITICAL
L3705
FERR-120-OHM-1.5A
0402-LF
PP3V3_ENET_PHYAVDD
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C3700 0.1UF
C3701 0.1UF
C3702 0.1UF
C3705 0.1UF
C3706 0.1UF
=PP1V05_ENET_PHY
(221mA typ - 1000base-T)
(7mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek
CRITICAL
L3715
FERR-120-OHM-1.5A
0402-LF
C3710 0.1UF
C3711 0.1UF
PP1V05_ENET_PHYAVDD
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
C3714 2.2UF
ENET1V05:EXT
R3722 0
C3715 2.2UF
C3716 0.1UF
=PP3V3_ENET_PHY_VDDREG
If internal switcher is used, must place 1x 22uF &
1x 0.1uF caps within 5mm of U3700 pins 44 & 45.
NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.
ENET1V05:INT
C3723 0.1UF
C3722 22UF
PP1V05_ENET_PHYAVDD_R
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6 MM
VOLTAGE=1.05V
R3721 0402 5% 1/16W MF-LF
If internal switcher is used, must place inductor within 5mm
of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.
=RTL8211_REGOUT
ENET1V05:INT
C3721 0.1UF
C3720 22UF
CRITICAL
ENET1V05:INT
L3720
4.7UH-0.91A
PLE031B-SM
R3720 10K
NO STUFF
R3725 4.7K
Alias to =PP3V3_ENET_PHY for internal switcher.
Alias to GND for external 1.05V supply.
R3750 4.7K
R3751 4.7K
R3752 4.7K
CRITICAL
U3700
RTL8251CA-VB-GR
TQFP
AVDD33
DVDD33
VDDREG
FB10
DVDD10
AVDD10
REGOUT
=RTL8211_ENSWREG
ENSWREG
RTL8211_REGOUT_L
R3796 0
ENET_CLK125M_TXCLK
ENET_CLK125M_TXCLK_R
TXC
ENET_TXD<0>
ENET_TXD<1>
ENET_TXD<2>
ENET_TXD<3>
TXD[0]
TXD[1]
TXD[2]
TXD[3]
RGMII/MII
ENET_TX_CTRL
TXCTL
ENET_MDC
ENET_MDIO
MDC
MDIO
MANAGEMENT
RXC
RXD[0]
RXD[1]/TXDLY
RXD[2]/AN0
RXD[3]/AN1
RXCTL
ENET_CLK125M_RXCLK_R
ENET_RXD_R<0>
ENET_RXD_R<1>
ENET_RXD_R<2>
ENET_RXD_R<3>
ENET_RXCTL_R
R3790 0
R3791 0
R3792 0
R3793 0
R3794 0
R3795 0
ENET_CLK125M_RXCLK
ENET_RXD<0>
ENET_RXD<1>
ENET_RXD<2>
ENET_RXD<3>
ENET_RX_CTRL
MDI+[0]
MDI-[0]
MDI+[1]
MDI-[1]
MDI+[2]
MDI-[2]
MDI+[3]
MDI-[3]
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
MEDIA DEPENDENT
ENET_RESET_L
R3724 0
RTL8211_PHYRST_L
PHYRSTB*
RESET
NO STUFF
C3725 0.1UF
ENET_RESET_L IS NOT ASSERTED WHEN WOL IS ACTIVE.
HENCE, RC (C3725 AND R3725) ARE NOT STUFFED.
RTL8211_RSET
RSET
REFERENCE
RTL8211_CLK125
CLK125
R3730 2.49K
R3731 22
CLOCK
RTL8211_CLK25M_CKXTAL1
TP_RTL8211_CKXTAL2
CKXTAL1
CKXTAL2
LED
LED0/PHYAD0
LED1/PHYAD1
LED2/RXDLY
RTL8211_PHYAD0
RTL8211_PHYAD1
RTL8211_RXDLY
GND
NO STUFF
C3790 10PF
R3755 4.7K
R3756 4.7K
R3757 4.7K
Reserved for EMI
per RealTek request.
RTL8211 25MHz Clock
NOTE: MCP89 CAN PROVIDE 25MHZ CLOCK, BUT CLOCK RUNS WHENEVER RMGT RAILS ARE POWERED.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.
R3746 22
MCP_CLK25M_BUF0_R
RTL8211_CLK25M_CKXTAL1
PLACEMENT_NOTE=Place close to U1400
Configuration Settings:
PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)
DO NOT SYNC, EXTERNAL 1.05V REGULATOR OPTION
SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE
Ethernet PHY (RTL8211CL)
Apple Inc.
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REVISION C.0.0
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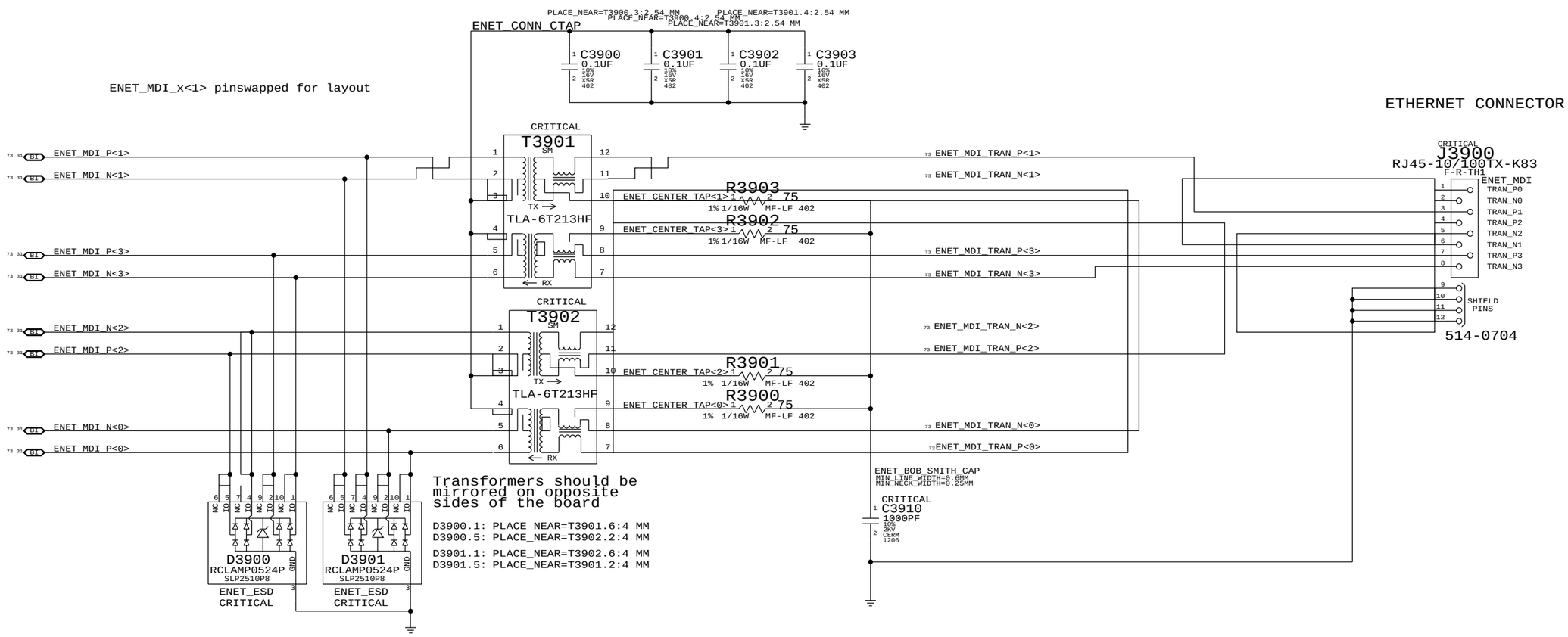
- COPY THIS PAGE FROM K36 CSA.39

ENET_MDI_x<1> pinswapped for layout



Transformers should be mirrored on opposite sides of the board

D3900.1: PLACE_NEAR=T3901.6:4 MM
D3900.5: PLACE_NEAR=T3902.2:4 MM

D3901.1: PLACE_NEAR=T3902.6:4 MM
D3901.5: PLACE_NEAR=T3901.2:4 MM

DO NOT SYNC FROM K6, WITH K84’S CONNECTOR

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE_TITLE

ETHERNET CONNECTOR

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SIL

518S0519

CRITICAL
J4502
78171-0002
M-RT-SM

R4531
4.7
5% 1/16W
MF-LF
402

L4530
FERR-1000-OHM
0402

L4531
FERR-1000-OHM
0402

C4531
0.001UF
10%
50V
CERM
402

SYS_LED_ANODE
SYS_LED_ANODE_R
SYS_LED_ANODE_UF
SYS_LED_RETURN_UF

ODD Power Control

=PP5V_S3_ODD
=PP3V3_S0_ODD

R4596
100K
5%
1/16W
MF-LF
402

R4597
100K
5%
1/16W
MF-LF
402

Q4596
SSM6N15FEAPE
SOT563

Q4596
SSM6N15FEAPE
SOT563

ODD_PWR_EN
ODD_PWR_EN_L
ODD_PWR_EN_LS5V_L

R4595
100K
5%
1/16W
MF-LF
402

CRITICAL
Q4590
TPCP8102
23V1K-SM

C4595
0.068UF
10%
16V
CERM
402

C4596
0.01UF
10%
16V
CERM
402

ODD_PWR_SS

PP5V_SW_ODD_R
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=5V

NOTE: 3.3V must be S0 if 5V is S3 or S5 to
ensure the drive is unpowered in S3/S5.

SENS_R:ENG
CRITICAL
R4598
0.002
1%
1/4W
MF
1206

ISNS_ODD_P
ISNS_ODD_N

PP5V_SW_ODD
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=5V

SATA ODD

=PP3V3_S0_ODD

R4590
33K
5%
1/16W
MF-LF
402

SMC_ODD_DETECT
Indicates disc presence

CRITICAL
J4500
54722-0164
F-ST-SM

516S0616

CRITICAL
FL4520
90-OHM-100MA
DLP11S

SATA_ODD_R2D_UF_P
SATA_ODD_R2D_UF_N
SATA_ODD_R2D_P
SATA_ODD_R2D_N
SATA_ODD_D2R_C_N
SATA_ODD_D2R_C_P

PLACE_NEAR=J4500.6:4MM

C4521
0.01UF
10%16V CERM 402

C4520
0.01UF
10%16V CERM 402

PLACE_NEAR=C4520:3MM
PLACE_NEAR=U1400.AJ2:3MM

SATA_ODD_R2D_C_P
SATA_ODD_R2D_C_N

CRITICAL
FL4525
90-OHM-100MA
DLP11S

SATA_ODD_D2R_UF_N
SATA_ODD_D2R_UF_P

PLACE_NEAR=J4500.10:4MM

C4526
0.01UF
10%16V CERM 402

C4525
0.01UF
10%16V CERM 402

PLACE_NEAR=FL4525.3:3MM
PLACE_NEAR=C4526:3MM

SATA_ODD_D2R_N
SATA_ODD_D2R_P

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	2	RES,0OHM,5%,1/4W,MF-LF,1206	R4599,R4598		SENS_R:PROD

SENS_R:ENG
CRITICAL
R4599
0.002
1%
1/4W
MF
1206

PP5V_S0_HDD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=5V

CRITICAL
L4500
FERR-70-OHM-4A
0603

PLACE_NEAR=J4501.9:3mm

PP5V_S0_HDD_R
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.4mm
VOLTAGE=5V

=PP5V_S0_HDD

C4502
0.1UF
20%
10V
CERM
402

PLACE_NEAR=L4500.2:2mm

ISNS_HDD_P
ISNS_HDD_N

Passive de-emphasis filter
Use 0-ohm resistors and NOSTUFF caps if not using

SATA HDD

CRITICAL
J4501
54722-0164
F-ST-SM

NCX

516S0616

CRITICAL
FL4502
90-OHM-100MA
DLP11S

SATA_HDD_D2R_C_P
SATA_HDD_D2R_C_N
SATA_HDD_D2R_UF_P
SATA_HDD_D2R_UF_N

PLACE_NEAR=J4501.6:3MM

C4516
0.01UF
10%16V CERM 402

C4515
0.01UF
10%16V CERM 402

PLACE_NEAR=J4501.6:3MM
PLACE_NEAR=C4516.1:3MM

SATA_HDD_D2R_FILT_P
SATA_HDD_D2R_FILT_N

C4586
47PF
5%
CERM
50V
402

R4586
27.4
1%
MF-LF
1/16W
402

R4585
27.4
1%
MF-LF
1/16W
402

C4585
47PF
5%
CERM
50V
402

PLACEMENT_NOTE: Place R4585,R4586,C4585,C4586 on the same side.
Resistors should be on inside, with SATA passing straight through.

SATA_HDD_D2R_P
SATA_HDD_D2R_N

CRITICAL
FL4501
90-OHM-100MA
DLP11S

SATA_HDD_R2D_N
SATA_HDD_R2D_P
SATA_HDD_R2D_UF_N
SATA_HDD_R2D_UF_P

PLACE_NEAR=J4501.12:3MM

C4511
0.01UF
10%16V CERM 402

C4510
0.01UF
10%16V CERM 402

PLACE_NEAR=C4510.1:3MM
PLACE_NEAR=J4501.14:3MM

SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SATA Connectors

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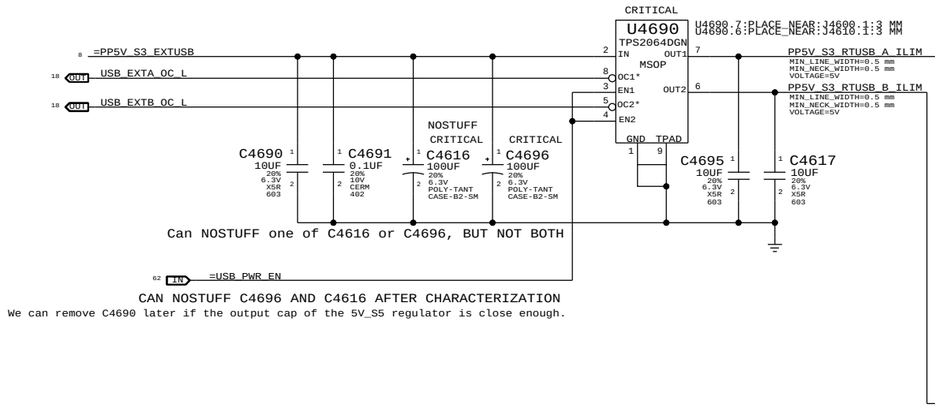
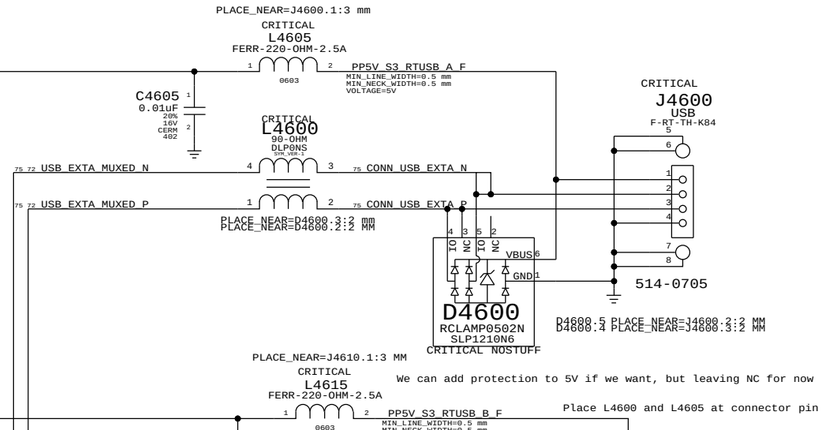
POR IS METAL USB CONNECTOR PARTS

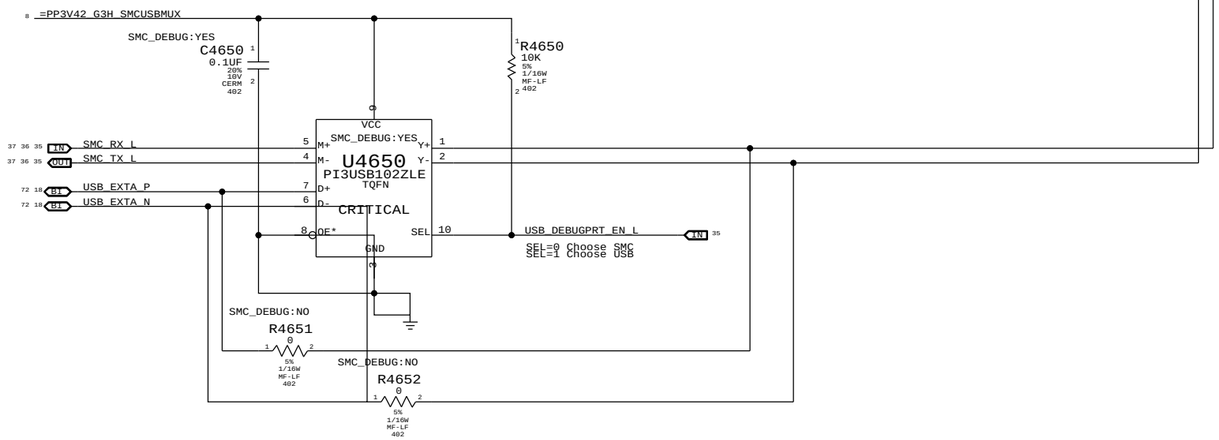
Port Power Switch



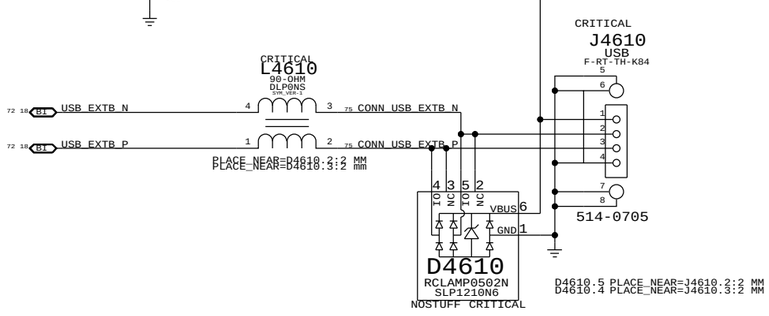
USB PORT A (FRONT PORT)



USB/SMC Debug Mux



USB PORT B (BACK PORT)



DO NOT SYNC WITH K84. UPDATED PLACE NEAR NOTES
UPDATED SMC_DEBUG BOMOPTION, STUFFED C4690

SYNC_MASTER=(K84 MLB) SYNC_DATE=(10/03/2009)

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External USB Connectors

Apple Inc.

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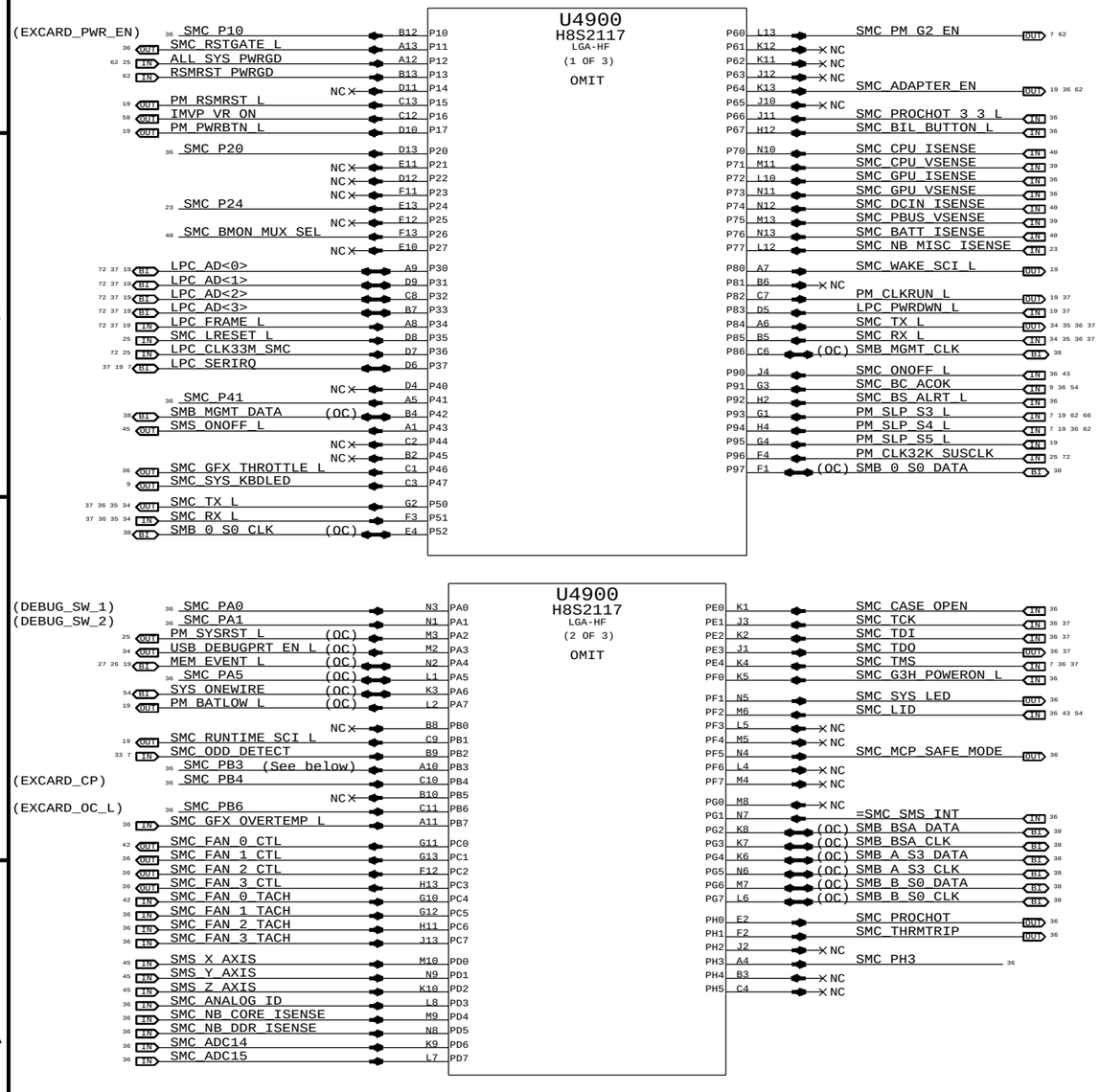
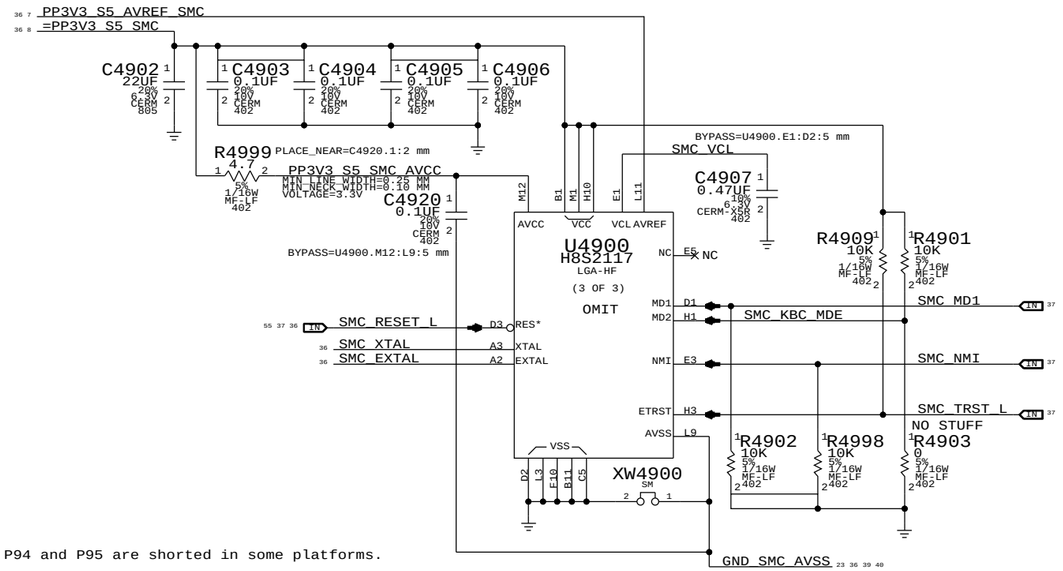
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay.



NOTE: P94 and P95 are shorted in some platforms.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

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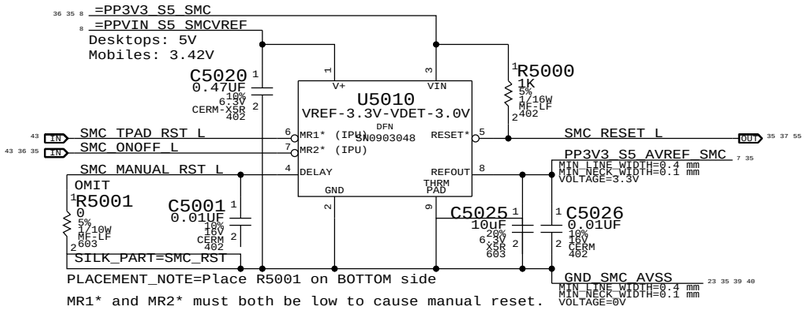
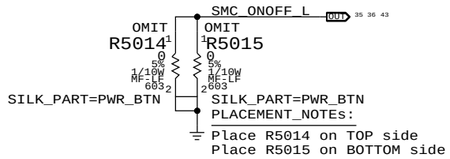
SMC Reset "Button", Supervisor & AVREF Supply



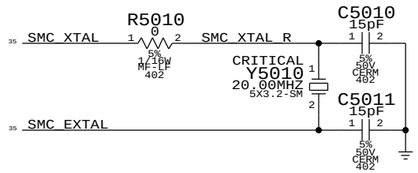
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

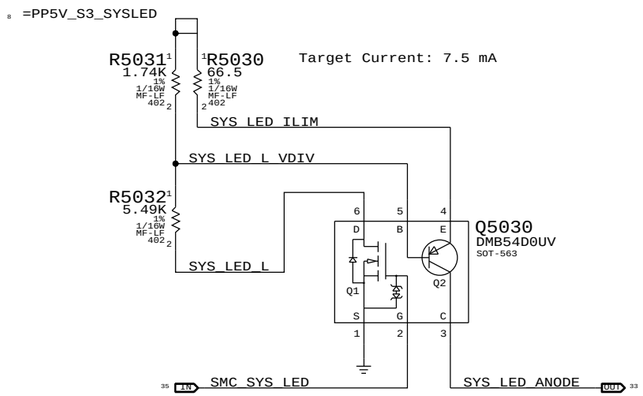
Debug Power "Buttons"



SMC Crystal Circuit

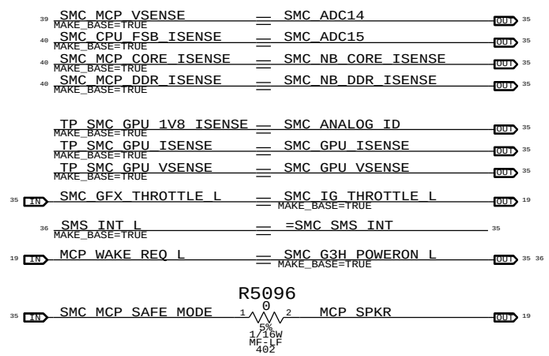


System (Sleep) LED Circuit

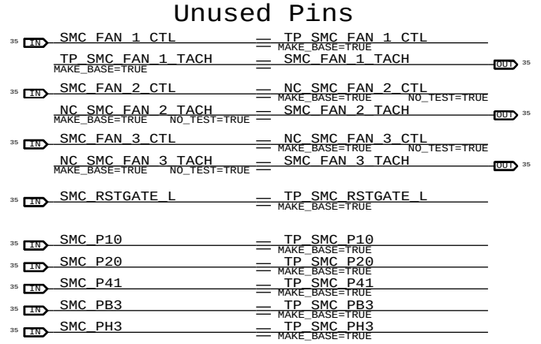


R5030,R5031,R5032 CHANGED FOR DIMMER LED

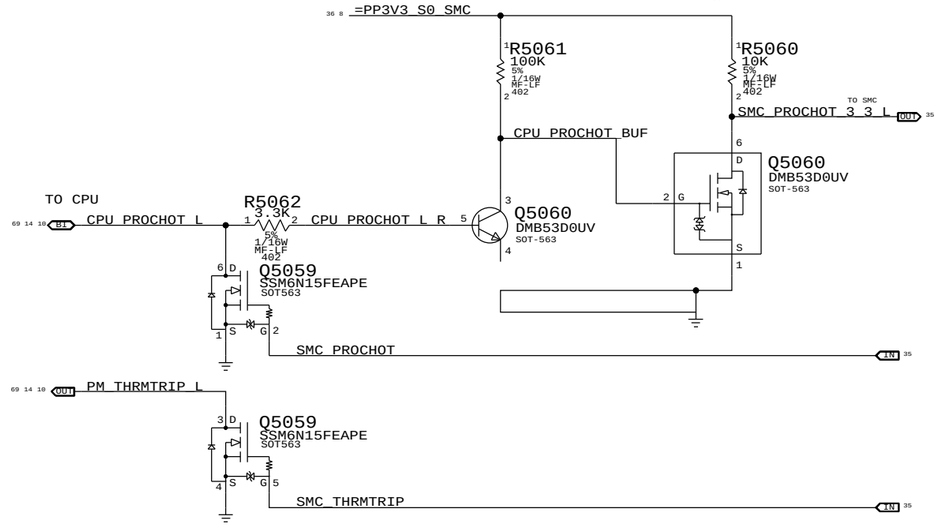
SMC Aliases



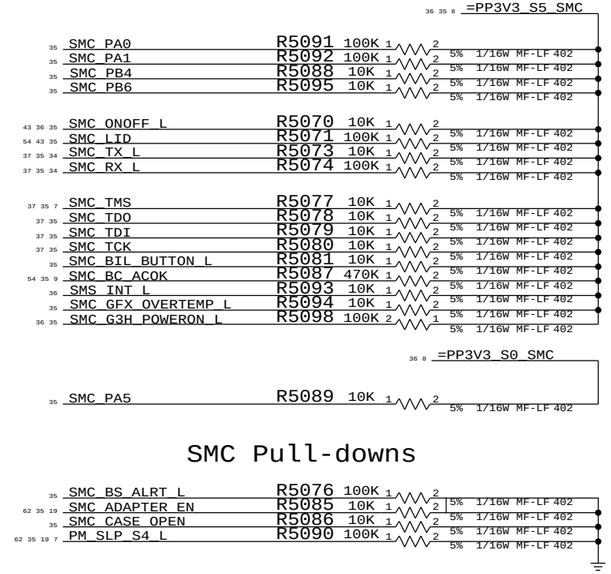
Unused Pins



SMC FSB to 3.3V Level Shifting



SMC Pull-ups



SMC Pull-downs

SYNC_MASTER=(T27 MLB) SYNC_DATE=(10/27/2009)

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SMC Support

Apple Inc.

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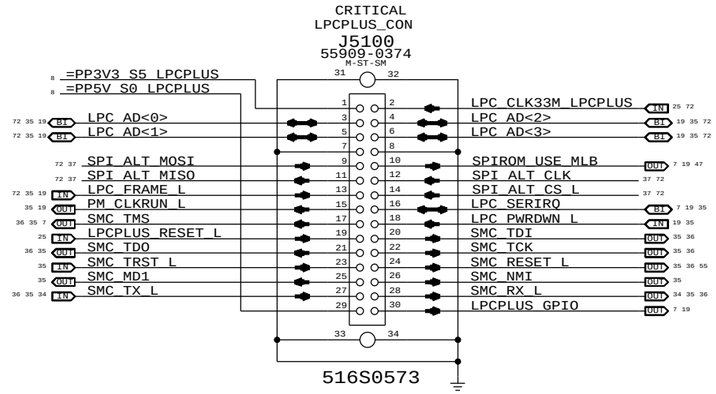
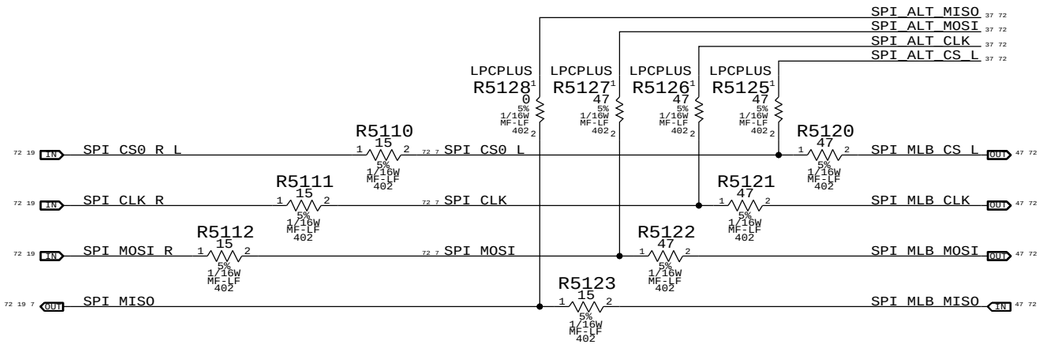
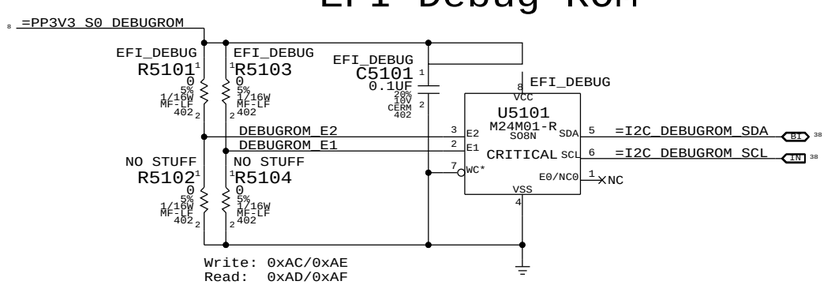
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=(T27_MLB) SYNC_DATE=(12/15/2009)

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

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MCP89 SMBus "0" Connections

=PP3V3_S0_SMBUS_MCP_0

MCP89
U1400
(MASTER)

SMBUS_MCP_0_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_0_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA

SO-DIMM "B"
J3100
(Write: 0xA2 Read: 0xA3)
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA

Debug Devices
(Not stuffed in production)

Vref DACs
DAC5574: U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

Mikey
CD3275: U6880
(Write: 0x72 Read: 0x73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

Margin Control
PCA9557: U3310
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

EFI Debug Serial
M24M01: U5101
(Write: 0xAC/0xAE
Read: 0xAD/0xAF)
=I2C_DEBUGROM_SCL
=I2C_DEBUGROM_SDA

MCP89 SMBus "1" Connections

=PP3V3_S0_SMBUS_MCP_1

MCP89
U1400
(Write: 0xE0 Read: 0xE1)

SMBUS_MCP_1_CLK (MAKE_BASE=TRUE)
SMBUS_MCP_1_DATA (MAKE_BASE=TRUE)

NO STUFF
R5230 2.0K 5% 1/16W MF-LF 402
NO STUFF
R5231 2.0K 5% 1/16W MF-LF 402

R5235 0 5% 1/16W MF-LF 402
R5236 0 5% 1/16W MF-LF 402

MCP89 SMBus 1 is slave port to access internal thermal sensors

Another slave port is available at 0x10/0x11, probably not used.

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)

SMB_0_S0_CLK
SMB_0_S0_DATA

R5250 10K 5% 1/16W MF-LF 402
R5251 10K 5% 1/16W MF-LF 402

SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

Debug Temp
TMP442A: U5535
(WRITE: 0x98 READ: 0x99)
=I2C_MCPTHMSNS_SCL
=I2C_MCPTHMSNS_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)

SMB_A_S3_CLK
SMB_A_S3_DATA

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

Trackpad
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

SMC "B" SMBus Connections

=PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)

SMB_B_S0_CLK
SMB_B_S0_DATA

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

Prod Temp
EMC1413: U5515
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

SMC "Battery A" SMBus Connections

=PP3V42_G3H_SMBUS_SMC_BSA

SMC
U4900
(MASTER)

SMB_BSA_CLK
SMB_BSA_DATA

R5280 2.61K 1% 1/16W MF-LF 402
R5281 2.61K 1% 1/16W MF-LF 402

SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

Battery Charger
ISL6259 - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

BATTERY
J6950
(See Table)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

=PP3V3_S3_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

SMB_MGMT_CLK
SMB_MGMT_DATA

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

Debug ADC
LT2309: U6000
(Write: 0x10 Read: 0x11)
=I2C_SMC_ADCS_SCL
=I2C_SMC_ADCS_SDA

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
K87 SMBus Connections

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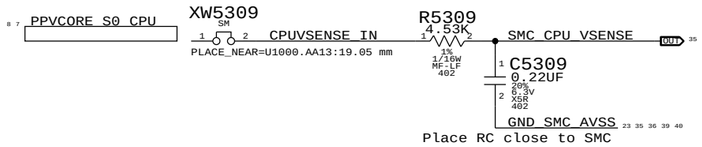
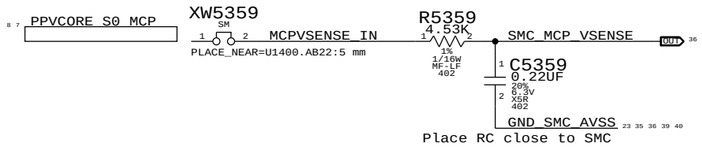
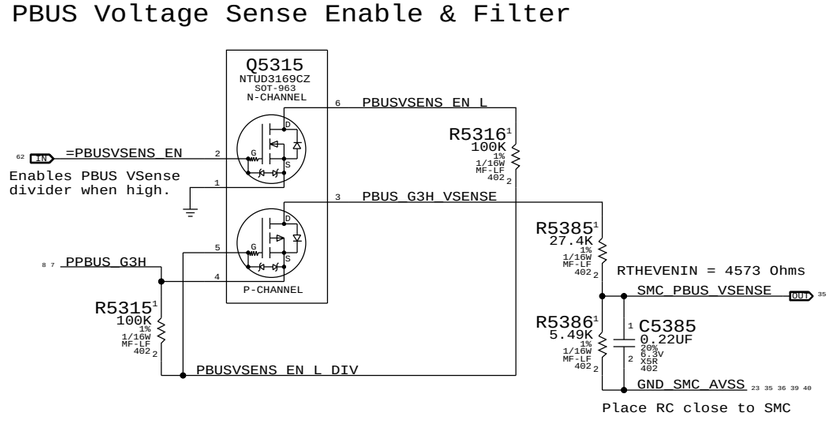
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS Voltage Sense Enable & Filter



SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

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Voltage Sensing

Apple Inc.

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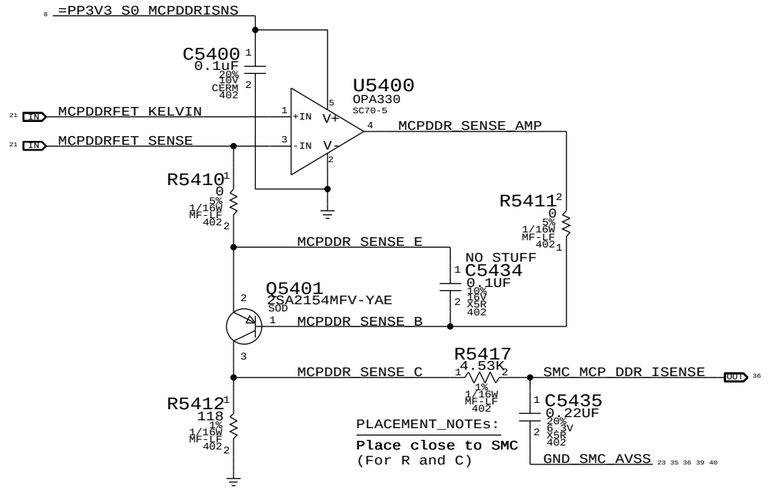
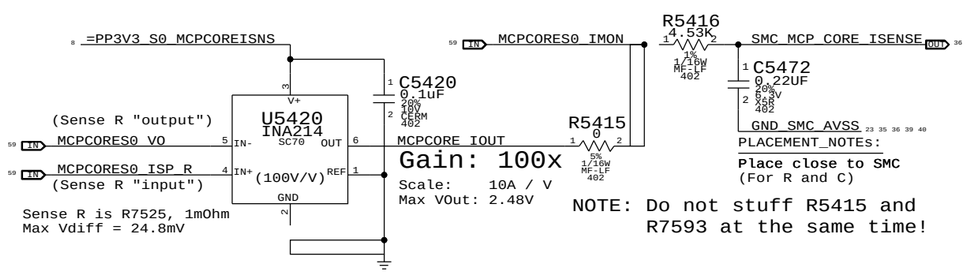
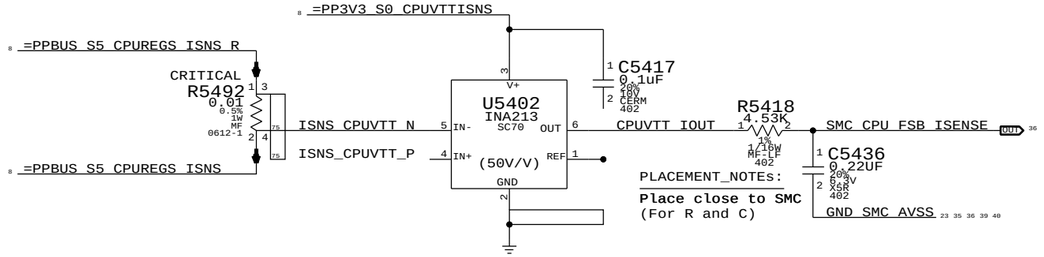
MCP MEM VDD Current Sense / Filter



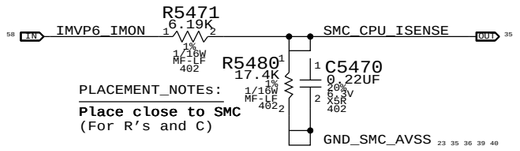
MCP VCore Current Sense Filter



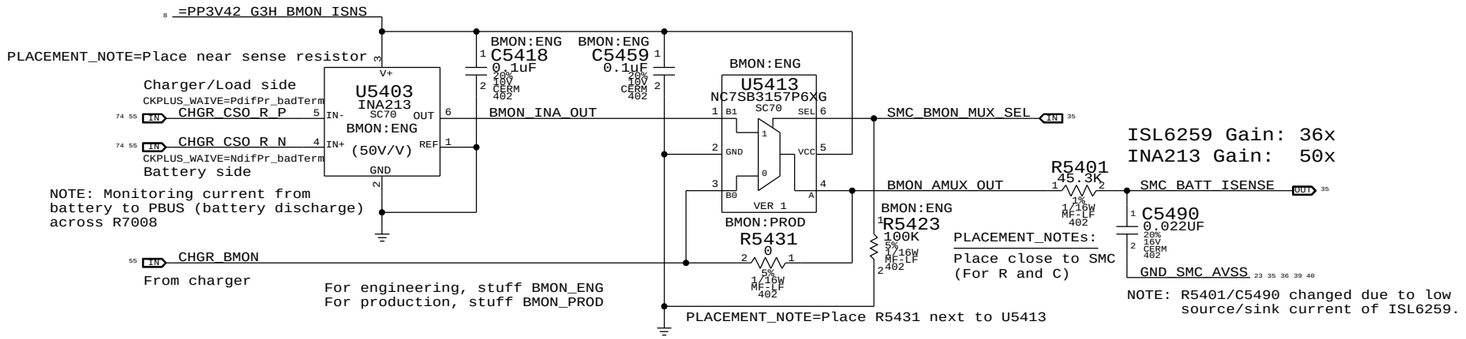
MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



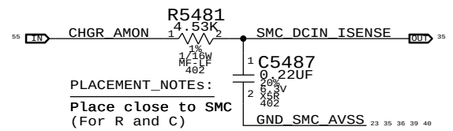
CPU VCore Load Side Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=T27_MLB SYNC_DATE=02/02/2010

PAGE TITLE: Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

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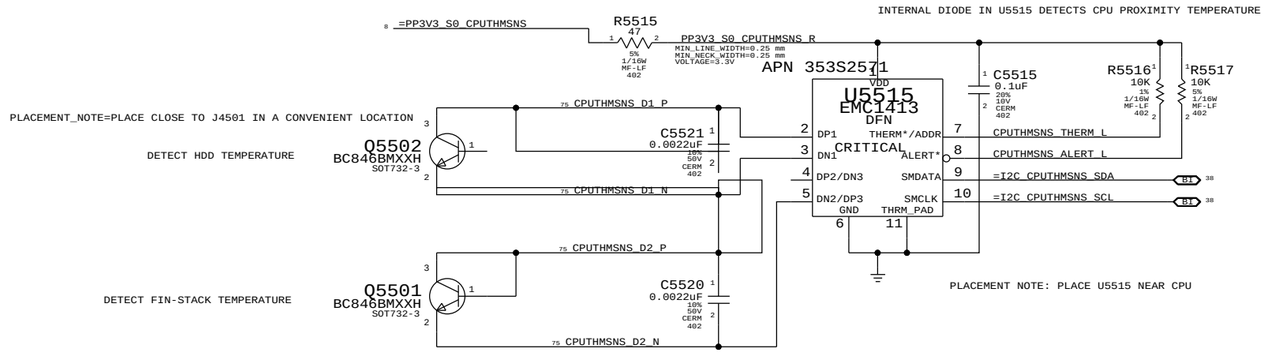
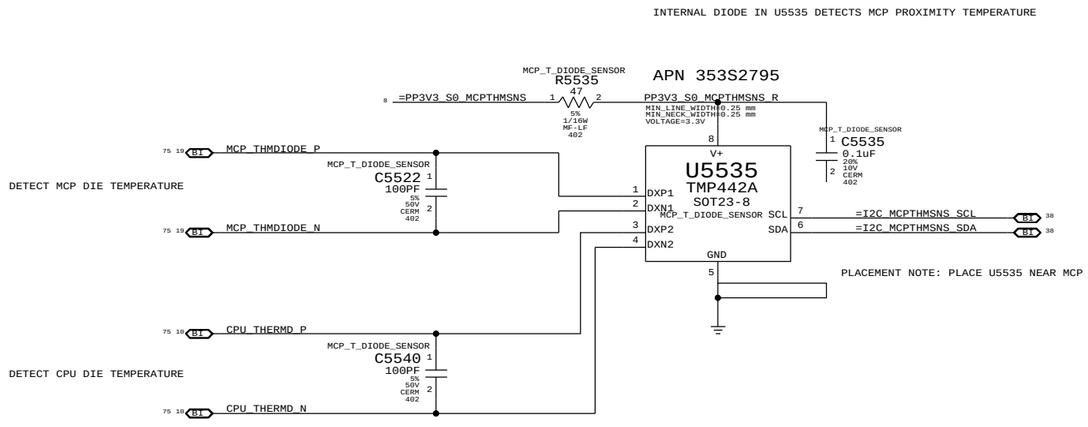
CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR



MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR



SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE: Thermal Sensors

Apple Inc.

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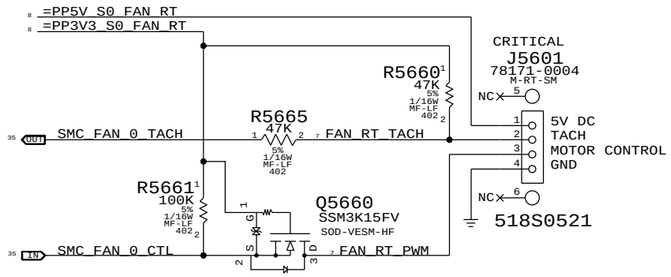

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

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Fan Connector

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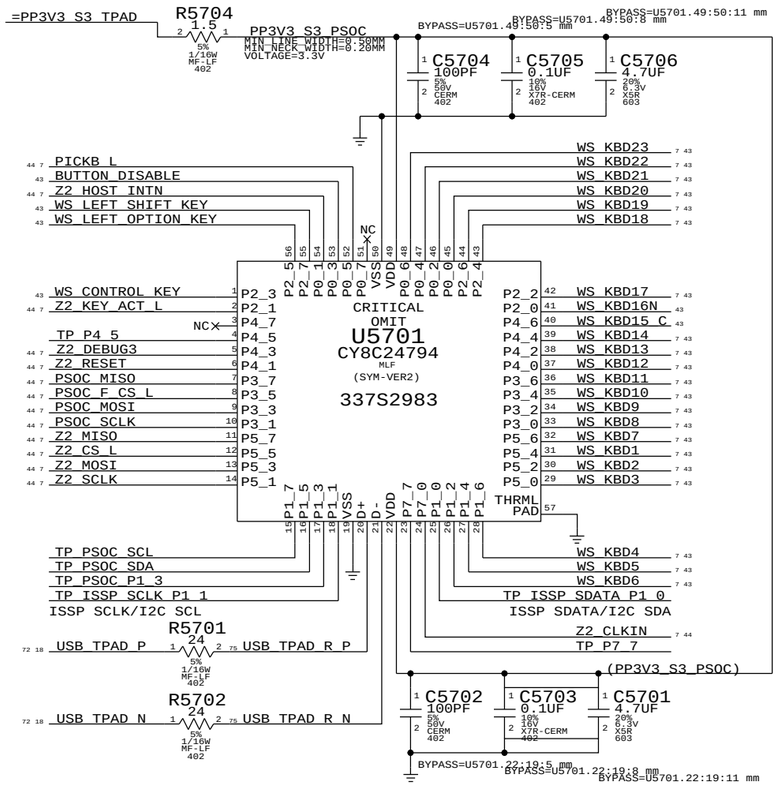
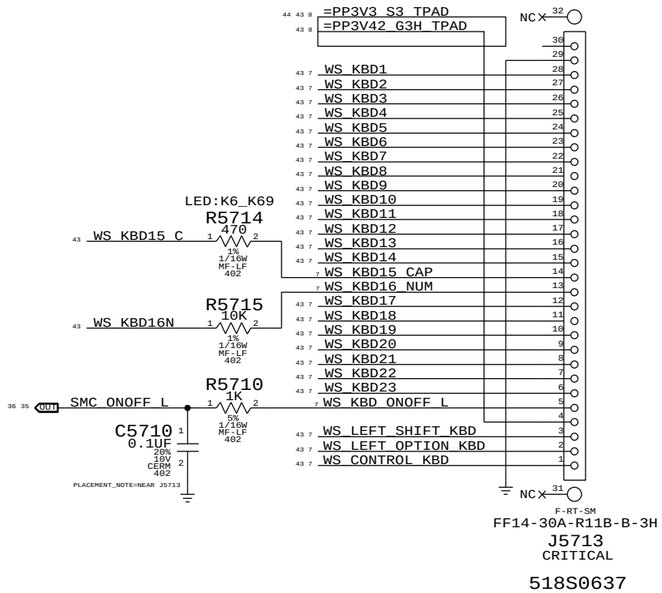
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



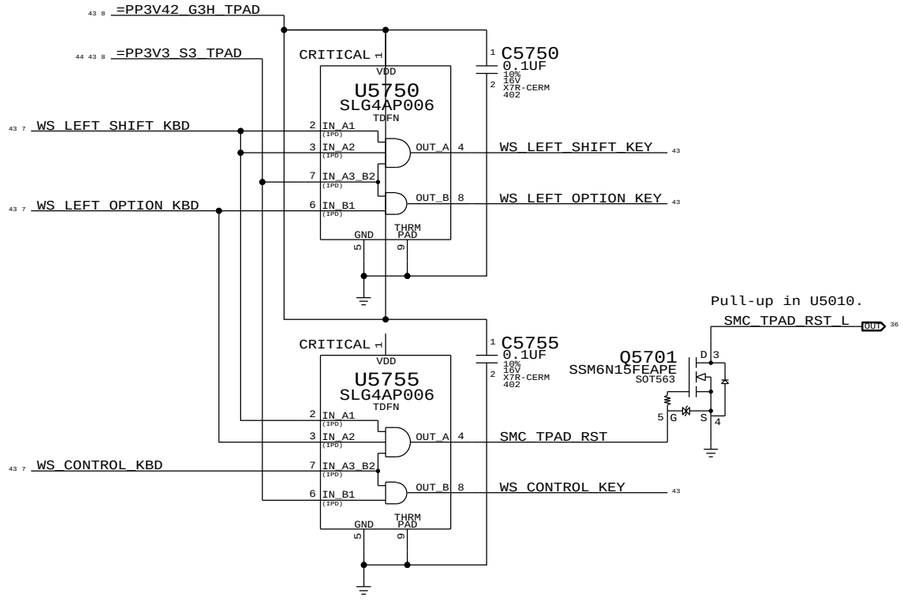
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

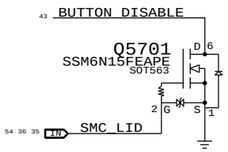


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: WELLSPRING 1

Apple Inc.

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BRANCH:
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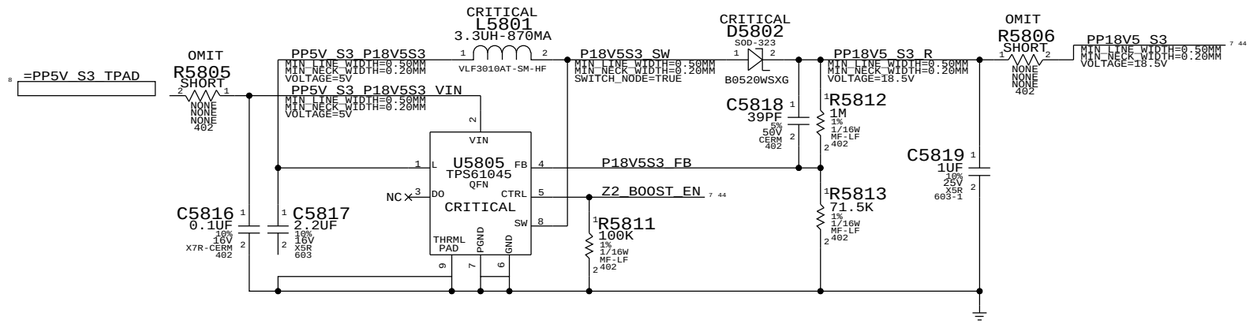
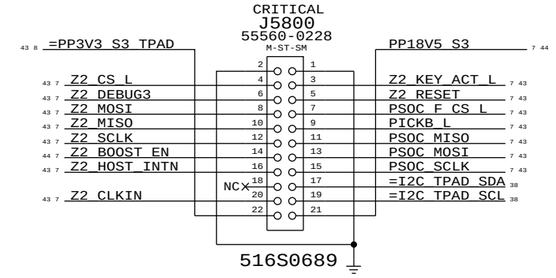
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



DO NOT SYNC FROM T27. REMOVED KEYBOARD BKLIGHT CIRCUIT

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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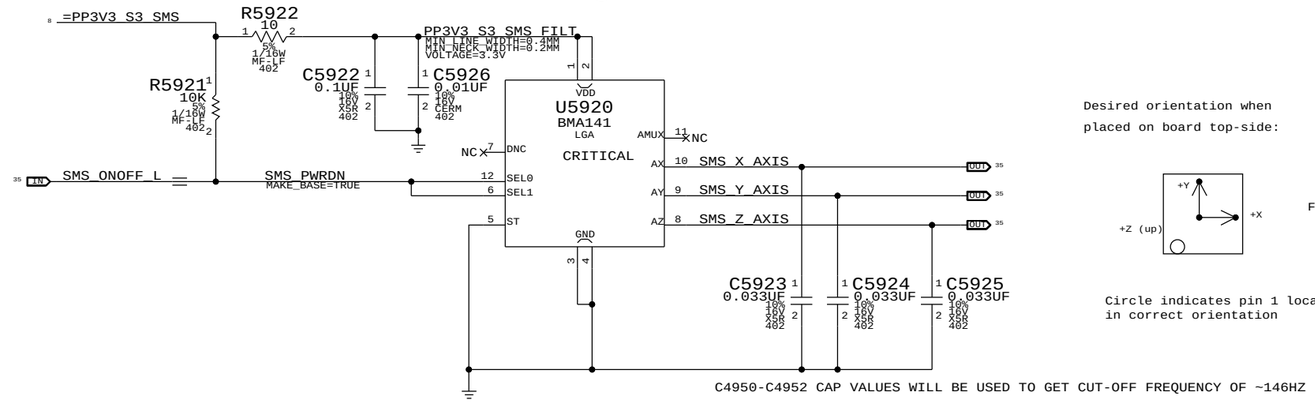
R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC

Analog SMS



Desired orientation when placed on board top-side:

Front of system

Circle indicates pin 1 location when placed in correct orientation

C4950-C4952 CAP VALUES WILL BE USED TO GET CUT-OFF FREQUENCY OF ~146HZ

PLACE_NEARs:

C5923.1:PLACE_NEAR=U4900.M10;2.54MM
C5924.1:PLACE_NEAR=U4900.N9;2.54MM
C5925.1:PLACE_NEAR=U4900.K10;2.54MM

DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923,C5924,C5925. ADDED PLACE NEARS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: SMS

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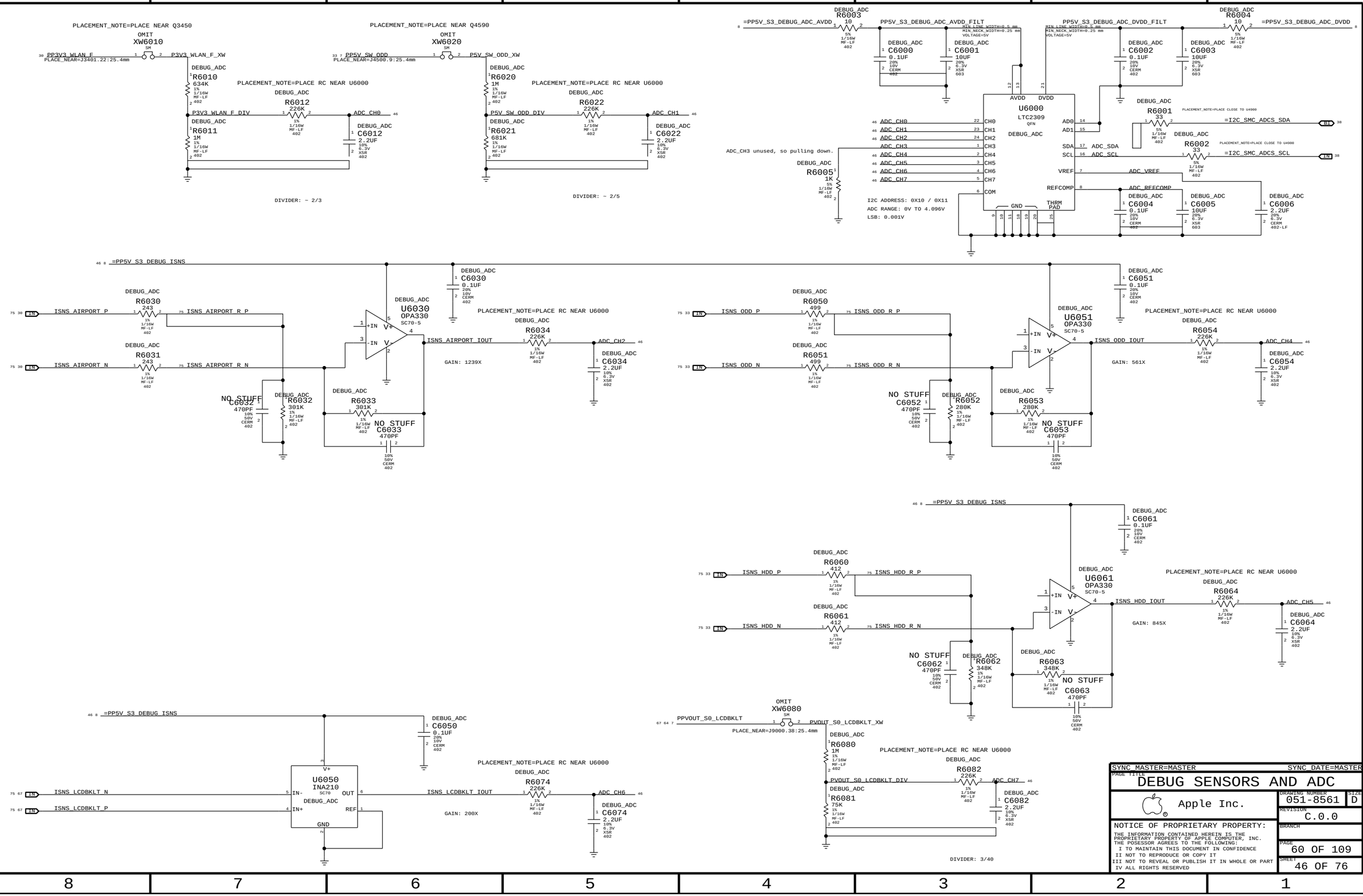
PLACEMENT_NOTE=PLACE NEAR Q3450
OMIT
XW6010
PP3V3_WLAN_F
PLACE_NEAR=J3401.22:25.4mm
P3V3_WLAN_F_XW
R6010 634K
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6012 226K
P3V3_WLAN_F_DIV
ADC_CH0
C6012 2.2UF
R6011 1M
DIVIDER: ~ 2/3
PLACEMENT_NOTE=PLACE NEAR Q4590
OMIT
XW6020
PP5V_SW_ODD
PLACE_NEAR=J4500.9:25.4mm
P5V_SW_ODD_XW
R6020 1M
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6022 226K
P5V_SW_ODD_DIV
ADC_CH1
C6022 2.2UF
R6021 681K
DIVIDER: ~ 2/5
=PP5V_S3_DEBUG_ADC_AVDD
R6003 10
PP5V_S3_DEBUG_ADC_AVDD_FILT
C6000 0.1UF
C6001 10UF
=PP5V_S3_DEBUG_ADC_DVDD
R6004 10
PP5V_S3_DEBUG_ADC_DVDD_FILT
C6002 0.1UF
C6003 10UF
U6000
LTC2309
QFN
AVDD
DVDD
GND
THRM PAD
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
COM
ADC_CH3 unused, so pulling down.
R6005 1K
I2C ADDRESS: 0X10 / 0X11
ADC RANGE: 0V TO 4.096V
LSB: 0.001V
R6001 33
R6002 33
=I2C_SMC_ADCS_SDA
=I2C_SMC_ADCS_SCL
ADC_SDA
ADC_SCL
ADC_VREF
ADC_REFCOMP
C6004 0.1UF
C6005 10UF
C6006 2.2UF
=PP5V_S3_DEBUG_ISNS
ISNS_AIRPORT_P
ISNS_AIRPORT_N
R6030 243
R6031 243
U6030
OPA330
SC70-5
C6030 0.1UF
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6034 226K
ISNS_AIRPORT_IOUT
ADC_CH2
C6034 2.2UF
GAIN: 1239X
NO STUFF
C6032 470PF
R6032 301K
R6033 301K
NO STUFF
C6033 470PF
ISNS_AIRPORT_R_P
ISNS_AIRPORT_R_N
ISNS_ODD_P
ISNS_ODD_N
R6050 499
R6051 499
C6051 0.1UF
U6051
OPA330
SC70-5
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6054 226K
ISNS_ODD_IOUT
ADC_CH4
C6054 2.2UF
GAIN: 561X
NO STUFF
C6052 470PF
R6052 280K
R6053 280K
NO STUFF
C6053 470PF
ISNS_ODD_R_P
ISNS_ODD_R_N
=PP5V_S3_DEBUG_ISNS
C6061 0.1UF
ISNS_HDD_P
ISNS_HDD_N
R6060 412
R6061 412
U6061
OPA330
SC70-5
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6064 226K
ISNS_HDD_IOUT
ADC_CH5
C6064 2.2UF
GAIN: 845X
NO STUFF
C6062 470PF
R6062 348K
R6063 348K
NO STUFF
C6063 470PF
ISNS_HDD_R_P
ISNS_HDD_R_N
=PP5V_S3_DEBUG_ISNS
C6050 0.1UF
U6050
INA210
SC70
ISNS_LCDBKLT_N
ISNS_LCDBKLT_P
ISNS_LCDBKLT_IOUT
ADC_CH6
C6074 2.2UF
R6074 226K
GAIN: 200X
PLACEMENT_NOTE=PLACE RC NEAR U6000
OMIT
XW6080
PPVOUT_S0_LCDBKLT
PLACE_NEAR=J9000.38:25.4mm
PVOUT_S0_LCDBKLT_XW
R6080 1M
R6081 75K
PLACEMENT_NOTE=PLACE RC NEAR U6000
R6082 226K
PVOUT_S0_LCDBKLT_DIV
ADC_CH7
C6082 2.2UF
DIVIDER: 3/40
SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE
DEBUG SENSORS AND ADC
Apple Inc.
DRAWING NUMBER 051-8561
SIZE D
REVISION C.0.0
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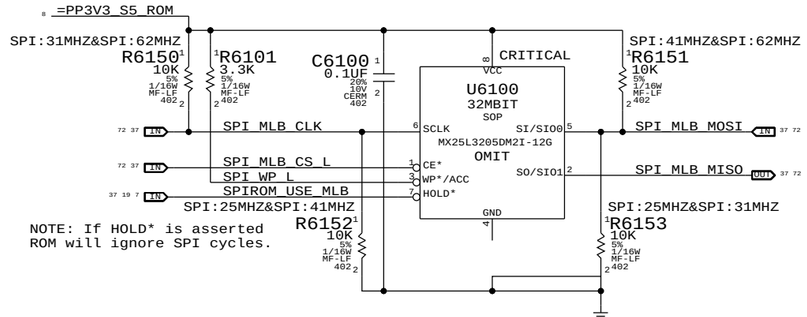

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: SPI ROM

Apple Inc.

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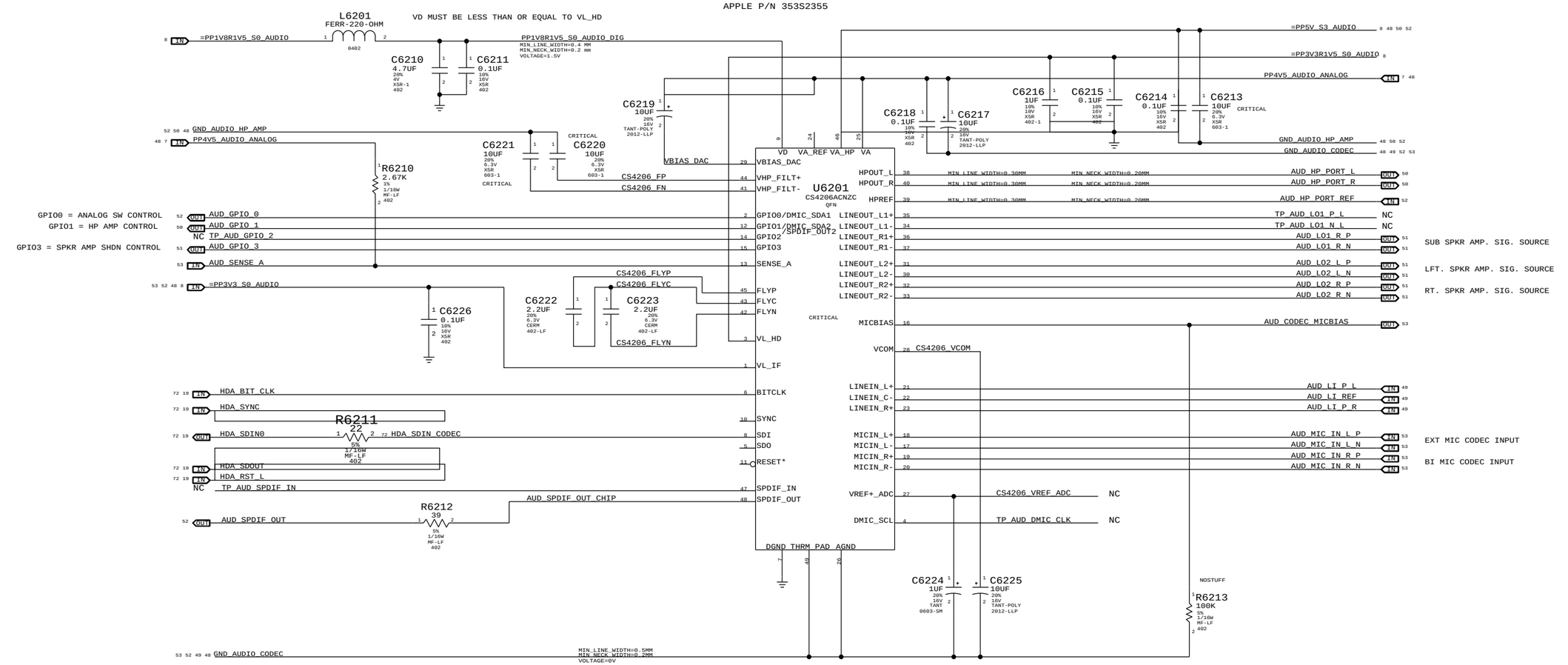
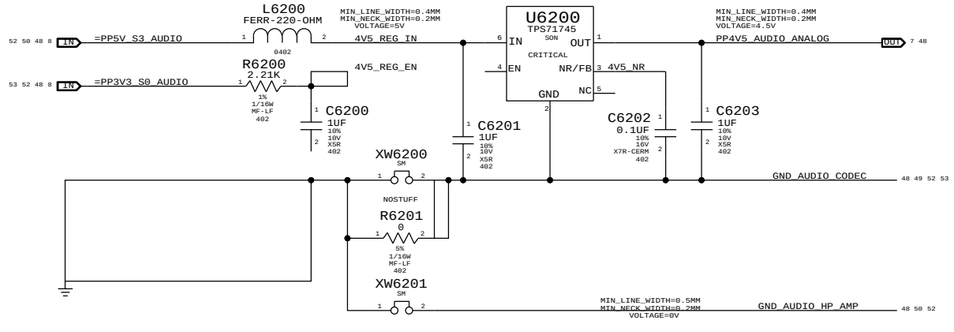
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2281



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=AUDIO
SYNC_DATE=02/16/2010

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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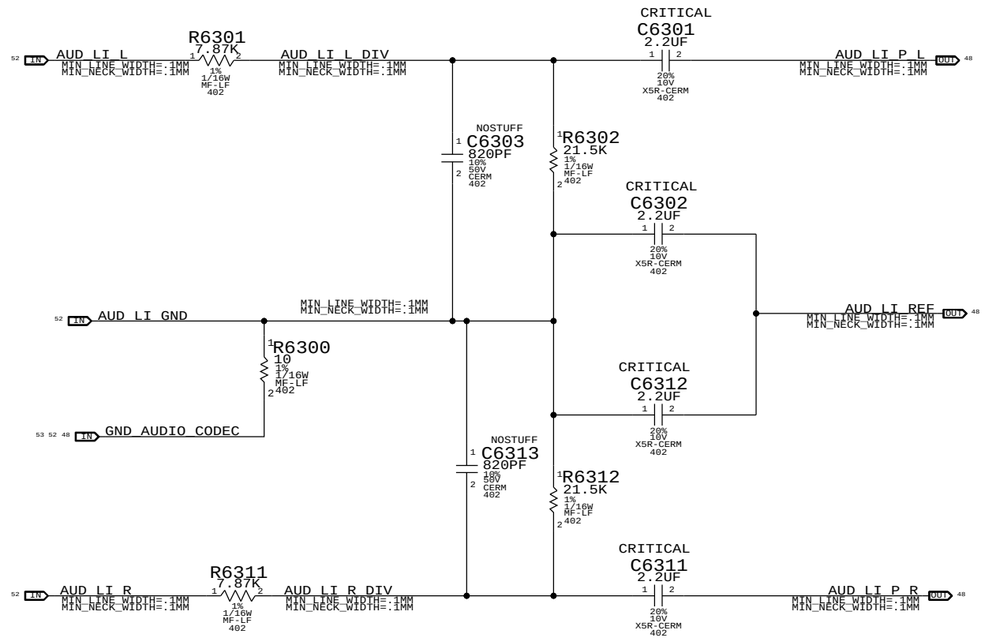
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

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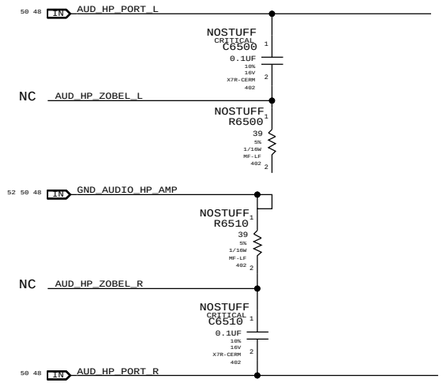
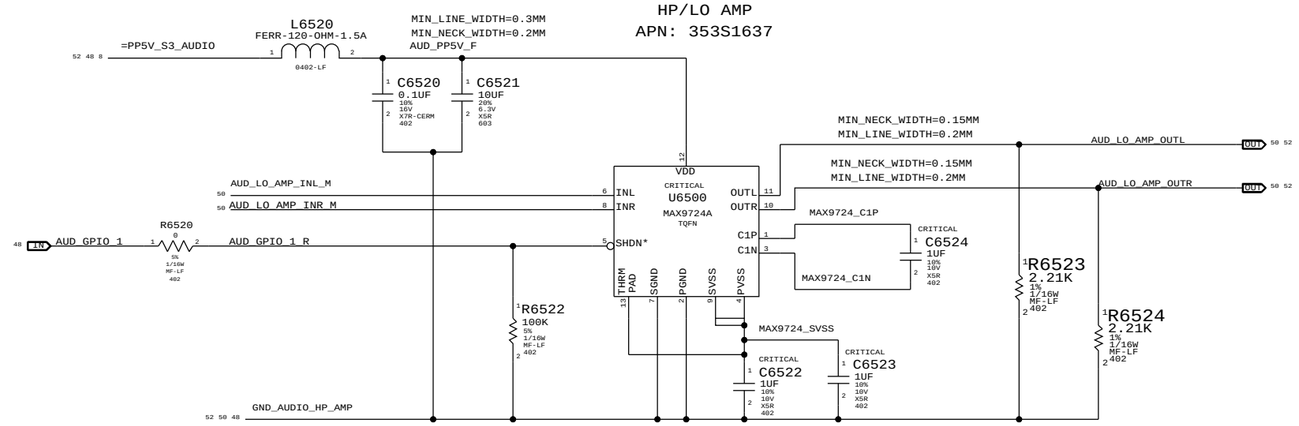
CS4206 HP OUTPUT ZOBEL NETWORK

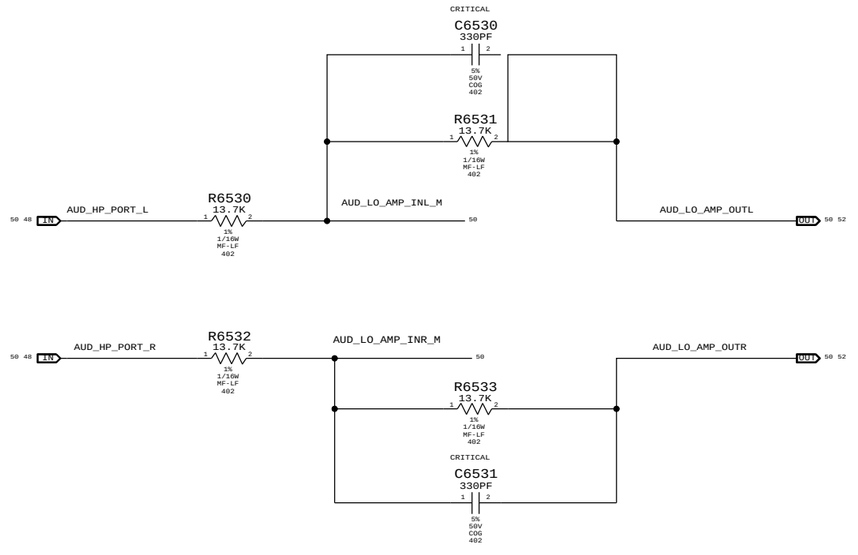


HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC_MASTER=AUDIO SYNC_DATE=02/16/2010

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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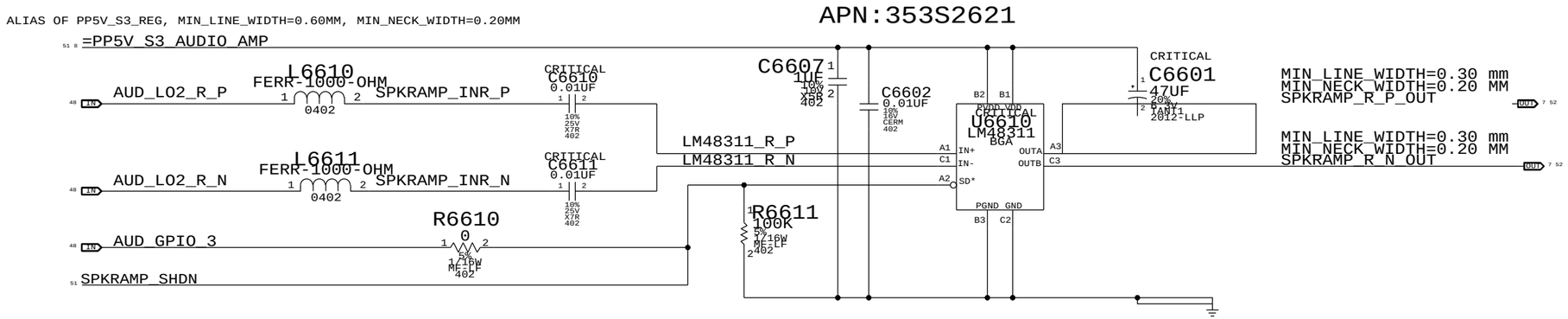
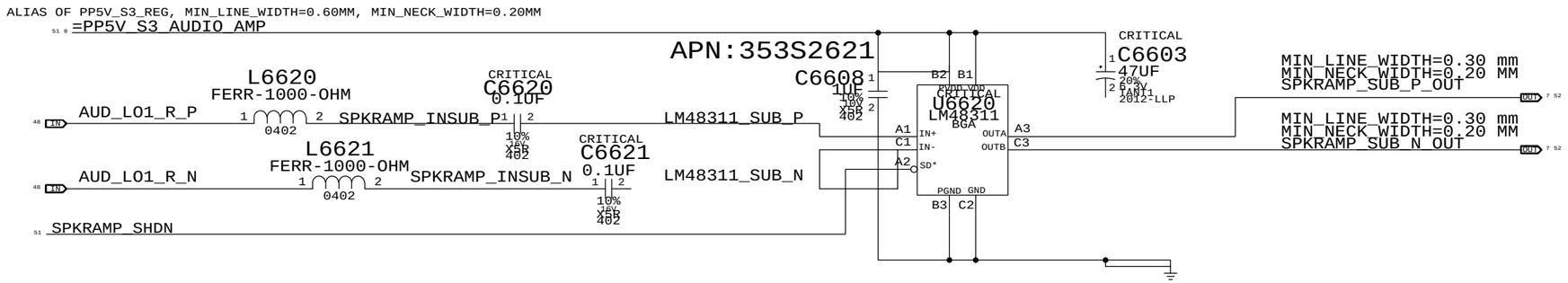
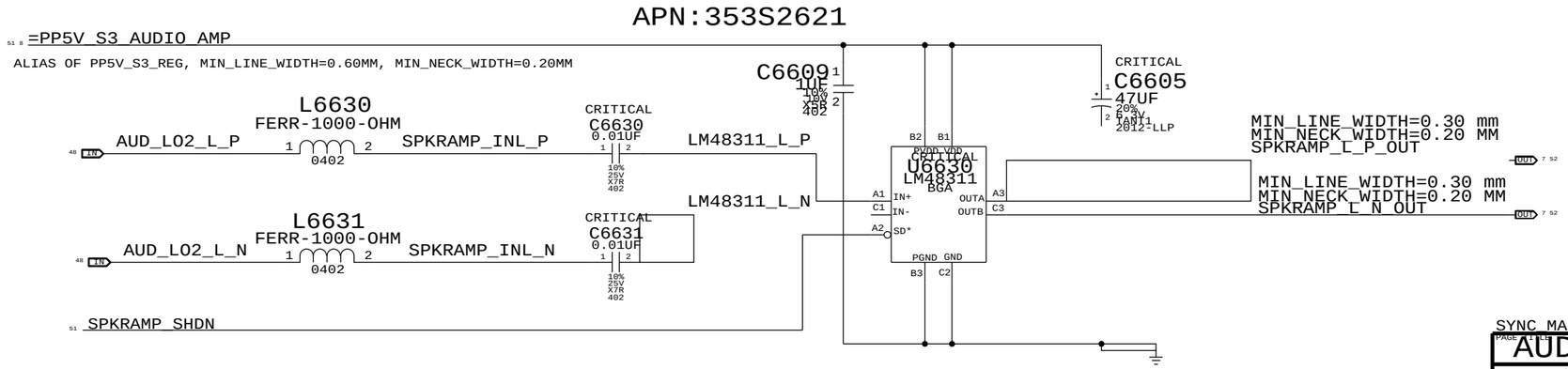
SATELLITE 796Hz < HPF FC < 936Hz
SUB 80 Hz < HPF FC < 94 Hz
GAIN 6DB (2V/V)
SPRK AMP. INPUT REFERRED CLIP POINT = ~-6dBFS







SYNC_MASTER=AUDIO SYNC_DATE=02/16/2010

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

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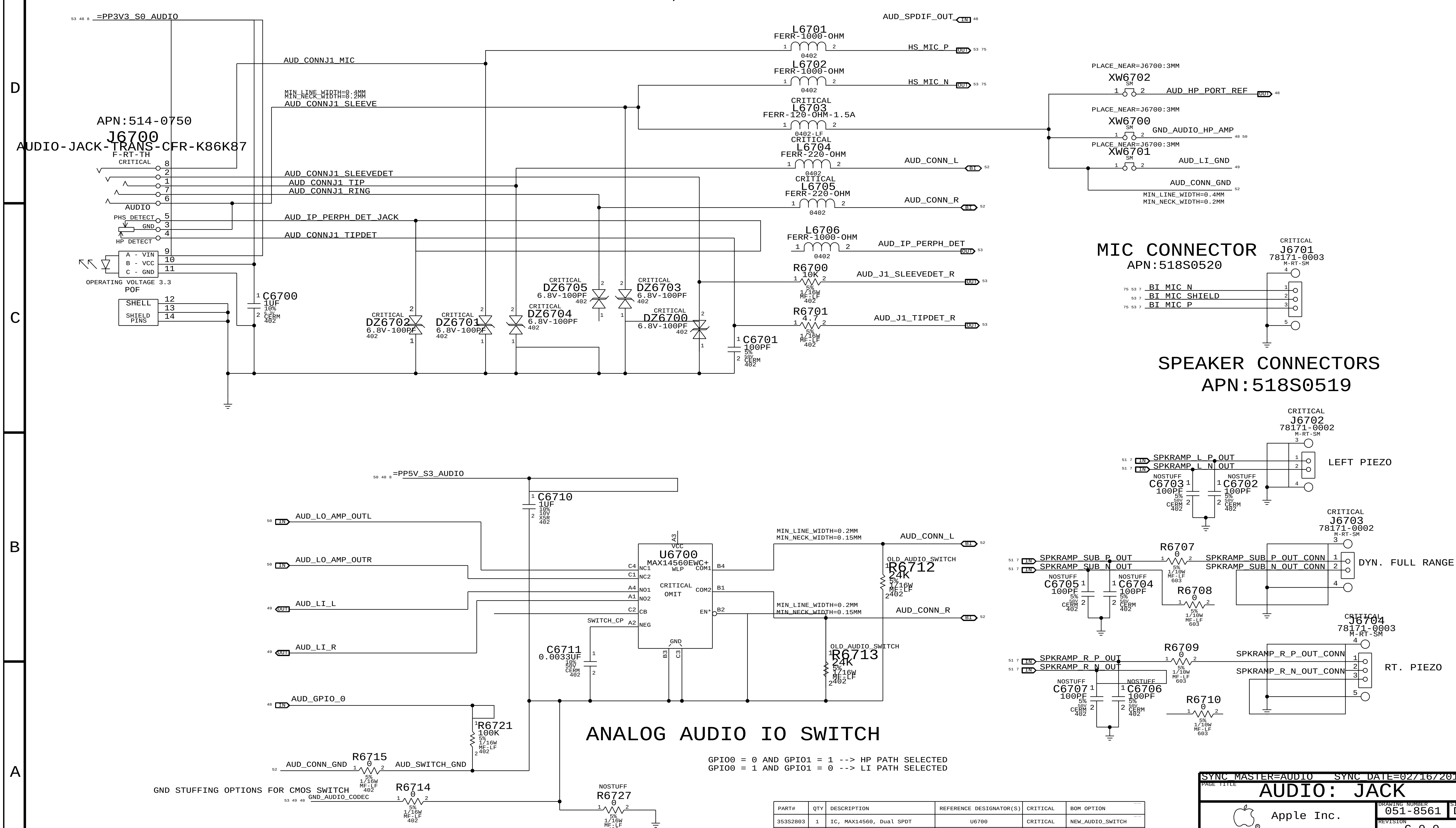
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



=PP3V3_S0_AUDIO
AUD_SPDIF_OUT
AUD_CONNJ1_MIC
L6701 FERR-1000-OHM 0402
HS_MIC_P
L6702 FERR-1000-OHM 0402
HS_MIC_N
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONNJ1_SLEEVE
CRITICAL L6703 FERR-120-OHM-1.5A 0402-LF
CRITICAL L6704 FERR-220-OHM 0402
AUD_CONN_L
CRITICAL L6705 FERR-220-OHM 0402
AUD_CONN_R
L6706 FERR-1000-OHM 0402
AUD_IP_PERPH_DET
APN:514-0750
J6700
AUDIO-JACK-TRANS-CFR-K86K87
F-RT-TH
CRITICAL
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUDIO
PHS DETECT
GND
HP DETECT
AUD_IP_PERPH_DET_JACK
AUD_CONNJ1_TIPDET
A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
C6700 1UF 10% 6.3V CERM 402
CRITICAL DZ6702 6.8V-100PF 402
CRITICAL DZ6701 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6700 6.8V-100PF 402
C6701 100PF 5% 50V CERM 402
R6700 10K 5% 1/16W MF-LF 402
AUD_J1_SLEEVEDET_R
R6701 4.7 5% 1/16W MF-LF 402
AUD_J1_TIPDET_R
PLACE_NEAR=J6700:3MM
XW6702 SM
AUD_HP_PORT_REF
XW6700 SM
GND_AUDIO_HP_AMP
XW6701 SM
AUD_LI_GND
AUD_CONN_GND
MIC CONNECTOR
APN:518S0520
CRITICAL J6701 78171-0003 M-RT-SM
BI_MIC_N
BI_MIC_SHIELD
BI_MIC_P
SPEAKER CONNECTORS
APN:518S0519
CRITICAL J6702 78171-0002 M-RT-SM
SPKRAMP_L_P_OUT
SPKRAMP_L_N_OUT
LEFT PIEZO
NOSTUFF C6703 100PF 5% 50V CERM 402
NOSTUFF C6702 100PF 5% 50V CERM 402
CRITICAL J6703 78171-0002 M-RT-SM
SPKRAMP_SUB_P_OUT
SPKRAMP_SUB_N_OUT
R6707 0 5% 1/10W MF-LF 603
SPKRAMP_SUB_P_OUT_CONN
SPKRAMP_SUB_N_OUT_CONN
DYN. FULL RANGE
NOSTUFF C6705 100PF 5% 50V CERM 402
NOSTUFF C6704 100PF 5% 50V CERM 402
R6708 0 5% 1/10W MF-LF 603
CRITICAL J6704 78171-0003 M-RT-SM
SPKRAMP_R_P_OUT
SPKRAMP_R_N_OUT
R6709 0 5% 1/10W MF-LF 603
SPKRAMP_R_P_OUT_CONN
SPKRAMP_R_N_OUT_CONN
RT. PIEZO
NOSTUFF C6707 100PF 5% 50V CERM 402
NOSTUFF C6706 100PF 5% 50V CERM 402
R6710 0 5% 1/10W MF-LF 603
=PP5V_S3_AUDIO
C6710 1UF 10% 10V X5R 402
AUD_LO_AMP_OUTL
AUD_LO_AMP_OUTR
AUD_LI_L
AUD_LI_R
U6700 MAX14560EWC+ WLP
CRITICAL OMIT
VCC NC1 NC2 NO1 NO2 CB NEG COM1 COM2 EN* GND
SWITCH_CP
C6711 0.0033UF 10% 50V CERM 402
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_CONN_L
AUD_CONN_R
OLD_AUDIO_SWITCH R6712 24K 5% 1/16W MF-LF 402
OLD_AUDIO_SWITCH R6713 24K 5% 1/16W MF-LF 402
AUD_GPIO_0
R6721 100K 5% 1/16W MF-LF 402
AUD_CONN_GND
R6715 0 5% 1/16W MF-LF 402
AUD_SWITCH_GND
GND STUFFING OPTIONS FOR CMOS SWITCH
GND_AUDIO_CODEC
R6714 0 5% 1/16W MF-LF 402
NOSTUFF R6727 0 5% 1/16W MF-LF 402
ANALOG AUDIO IO SWITCH
GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2803	1	IC, MAX14560, Dual SPDT	U6700	CRITICAL	NEW_AUDIO_SWITCH
353S2536	1	IC, MAX14504, Dual SPDT	U6700	CRITICAL	OLD_AUDIO_SWITCH

DO NOT SYNC K84. UPDATED PLACE NEARS

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2010

PAGE TITLE: AUDIO: JACK

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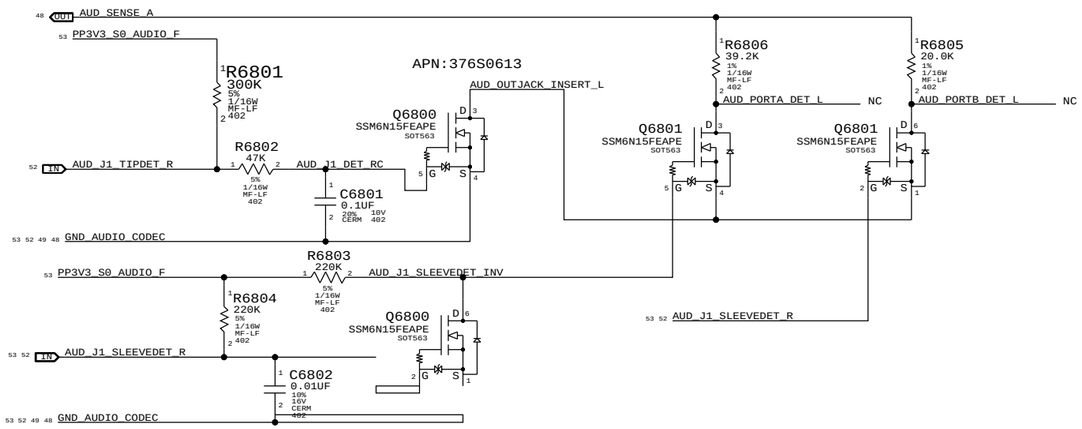
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

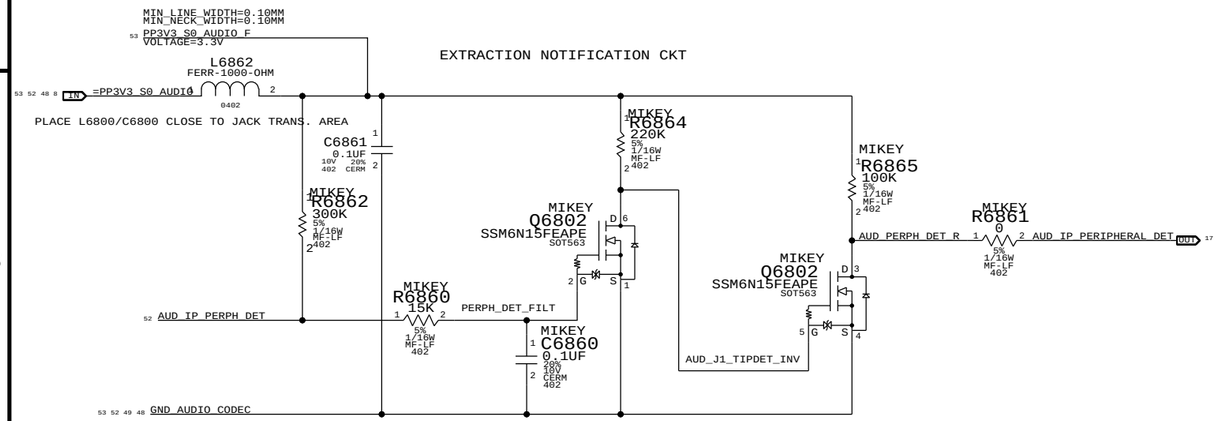
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF/ENABLE	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MCP79 GPIO_38	MCP79 GPIO_17 (PERIPH DETECT) MCP79 GPIO_4 (LOAD DETECT)

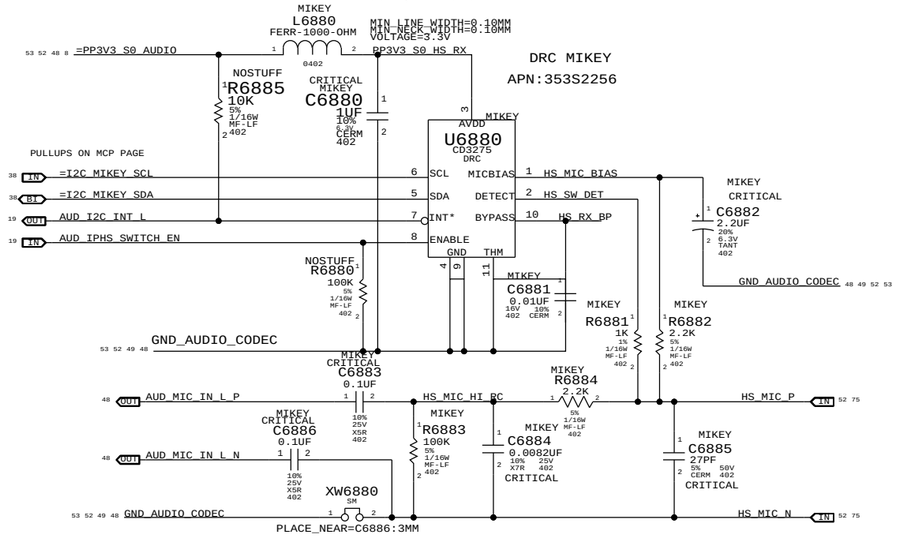
PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



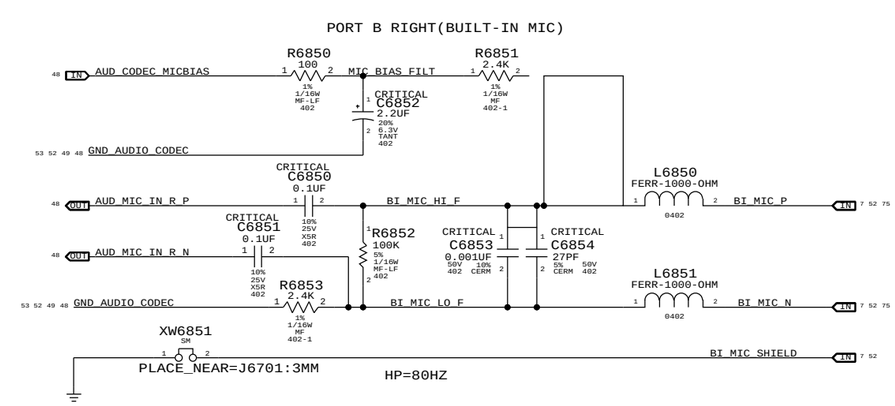
EXTRACTION NOTIFICATION CKT



PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



SYNC MASTER=AUDIO SYNC DATE=02/16/2010

AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER	051-8561
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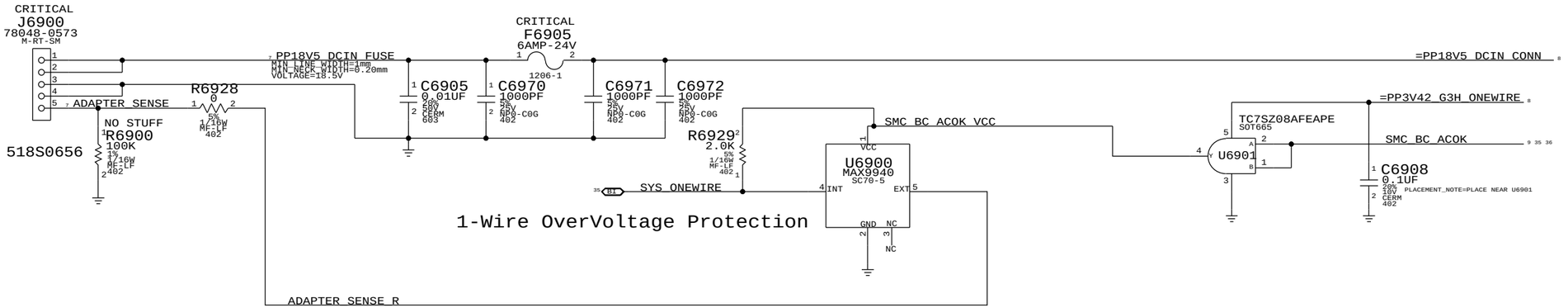
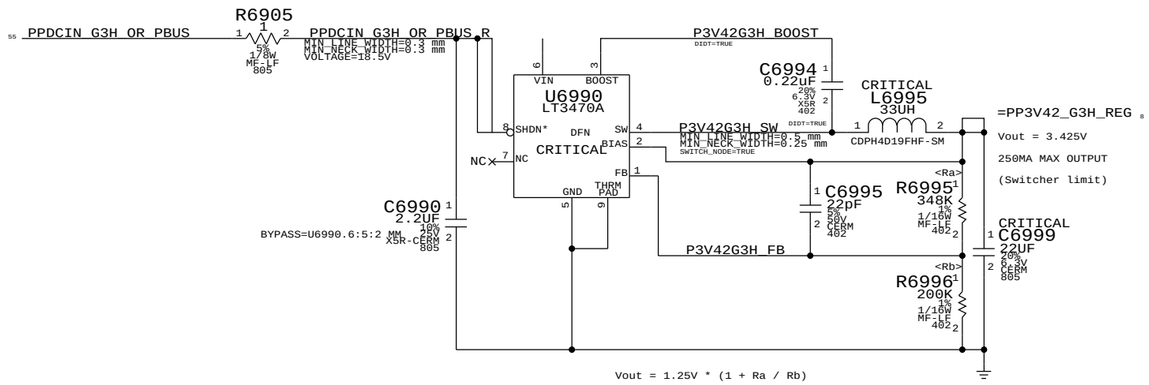
MagSafe DC Power Jack



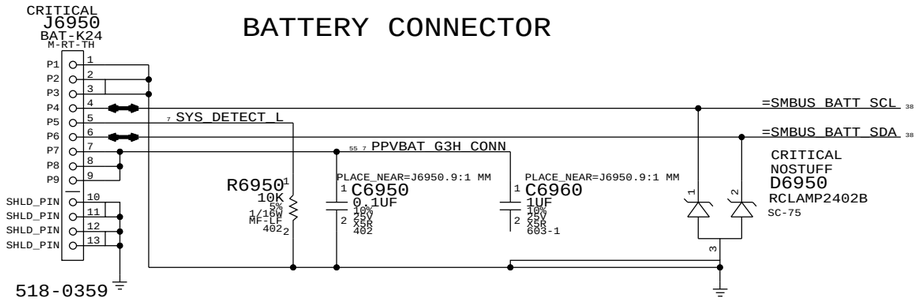
1-Wire OverVoltage Protection

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

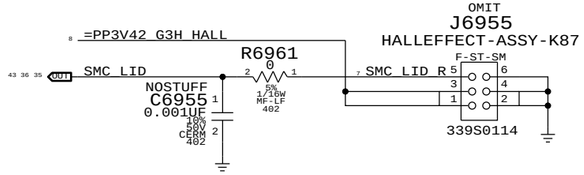


BATTERY CONNECTOR



HALL EFFECT ASSEMBLY

Assembly APN: 339S0114
- BOM: 639-0680
- PCBF: 820-2801
- MCO: 056-3515
- Conn APN:518S0788



PROTO 0: STUFFING K84 CONNECTOR ONTO MODIFIED K84 PADS
PROTO 1: STUFFING K87 HALL EFFECT ASSEMBLY ONTO K87 PADS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6831	1	SUB ASSY - HALL EFFECT, K86 K87	J6955	CRITICAL	

PN: 607-6831 for WCPM. PN: 339S0114 for schematic/board layout

DO NOT SYNC WITH K84. R6900,C6960,SIGNAL NAMES CHANGED. HALL EFFECT CONNECTOR CHANGED.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D
REVISION: C.0.0
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PAGE: 69 OF 109
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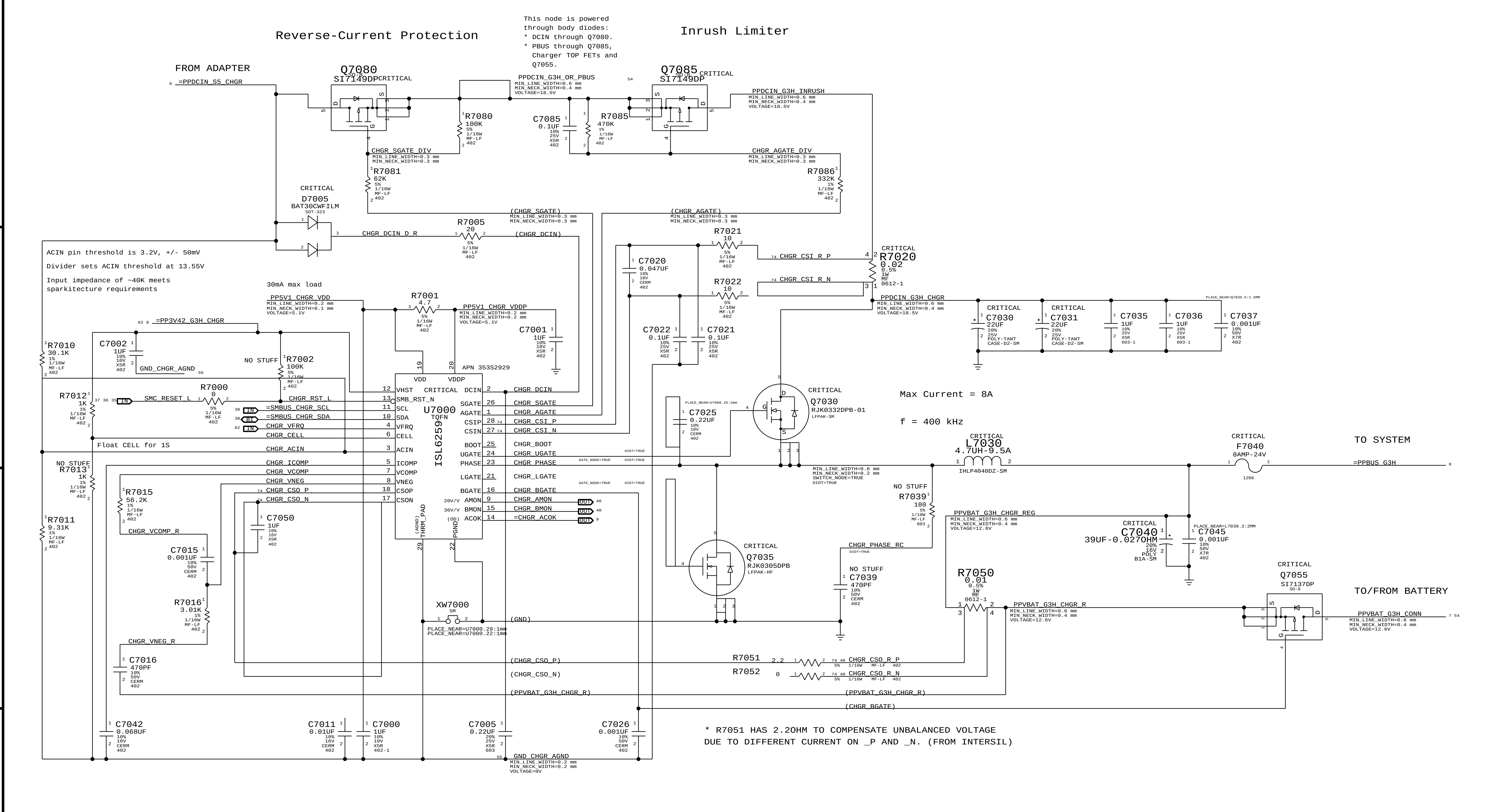

Reverse-Current Protection
Inrush Limiter
This node is powered
through body diodes:
* DCIN through Q7080.
* PBUS through Q7085,
Charger TOP FETs and
Q7055.
FROM ADAPTER
=PPDCIN_S5_CHGR
Q7080
SI7149DP
CRITICAL
Q7085
SI7149DP
CRITICAL
PPDCIN_G3H_OR_PBUS
PPDCIN_G3H_INRUSH
CHGR_SGATE_DIV
CHGR_AGATE_DIV
R7080
100K
C7085
0.1UF
R7085
470K
R7081
62K
R7086
332K
CRITICAL
D7005
BAT30CWFILM
SOT-323
R7005
20
CHGR_DCIN_D_R
(CHGR_DCIN)
(CHGR_SGATE)
(CHGR_AGATE)
ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Input impedance of ~40K meets
sparkitecture requirements
30mA max load
PP5V1_CHGR_VDD
R7001
4.7
PP5V1_CHGR_VDDP
C7001
1UF
=PP3V42_G3H_CHGR
R7010
30.1K
C7002
1UF
GND_CHGR_AGND
NO STUFF
R7002
100K
R7012
1K
R7000
0
SMC_RESET_L
CHGR_RST_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
Float CELL for 1S
CHGR_ACIN
NO STUFF
R7013
1K
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
R7015
56.2K
R7011
9.31K
C7050
1UF
CHGR_VCOMP_R
C7015
0.001UF
R7016
3.01K
CHGR_VNEG_R
C7016
470PF
APN 353S2929
U7000
ISL6259
TQFN
CRITICAL
VDD
VDDP
VHST
SMB_RST_N
SCL
SDA
VFRQ
CELL
ACIN
ICOMP
VCOMP
VNEG
CSOP
CSON
DCIN
SGATE
AGATE
CSIP
CSIN
BOOT
UGATE
PHASE
LGATE
BGATE
AMON
BMON
ACOK
THRM_PAD
PGND
CHGR_DCIN
CHGR_SGATE
CHGR_AGATE
CHGR_CSI_P
CHGR_CSI_N
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_BGATE
CHGR_AMON
CHGR_BMON
=CHGR_ACOK
XW7000
SM
PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm
(GND)
R7021
10
R7022
10
C7020
0.047UF
C7022
0.1UF
C7021
0.1UF
CRITICAL
R7020
0.02
0612-1
PPDCIN_G3H_CHGR
CRITICAL
C7030
22UF
CRITICAL
C7031
22UF
C7035
1UF
C7036
1UF
C7037
0.001UF
C7025
0.22UF
CRITICAL
Q7030
RJK0332DPB-01
LFPAK-SM
Max Current = 8A
f = 400 kHz
CRITICAL
L7030
4.7UH-9.5A
IHLP4040DZ-SM
CRITICAL
F7040
8AMP-24V
TO SYSTEM
=PPBUS_G3H
NO STUFF
R7039
180
CRITICAL
Q7035
RJK0305DPB
LFPAK-HF
CHGR_PHASE_RC
NO STUFF
C7039
470PF
PPVBAT_G3H_CHGR_REG
CRITICAL
C7040
39UF-0.027OHM
C7045
0.001UF
R7050
0.01
0612-1
PPVBAT_G3H_CHGR_R
CRITICAL
Q7055
SI7137DP
TO/FROM BATTERY
PPVBAT_G3H_CONN
R7051
2.2
R7052
0
CHGR_CSO_R_P
CHGR_CSO_R_N
(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)
C7042
0.068UF
C7011
0.01UF
C7000
1UF
C7005
0.22UF
C7026
0.001UF
GND_CHGR_AGND
* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE
DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT
K87 NOTES : R7050 APN 107S0075

SYNC_MASTER=(K6_MLB) SYNC_DATE=(11/06/2009)

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8561 SIZE D

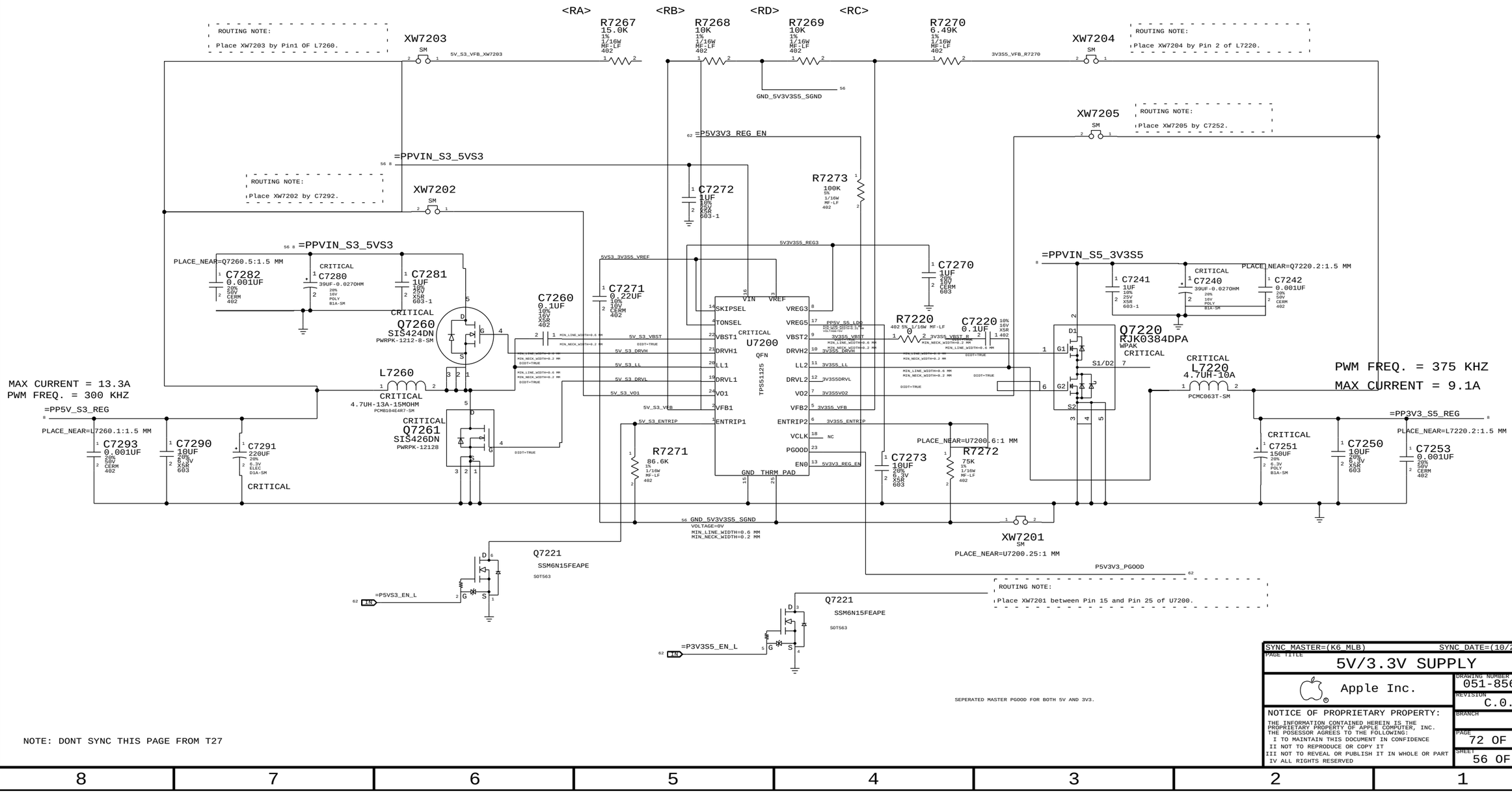
REVISION C.0.0

BRANCH

5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



SYNC MASTER=(K6_MLB)	SYNC DATE=(10/27/2009)
PAGE TITLE	5V/3.3V SUPPLY
Apple Inc.	DRAWING NUMBER 051-8561 SIZE D
	REVISION C.0.0
	BRANCH
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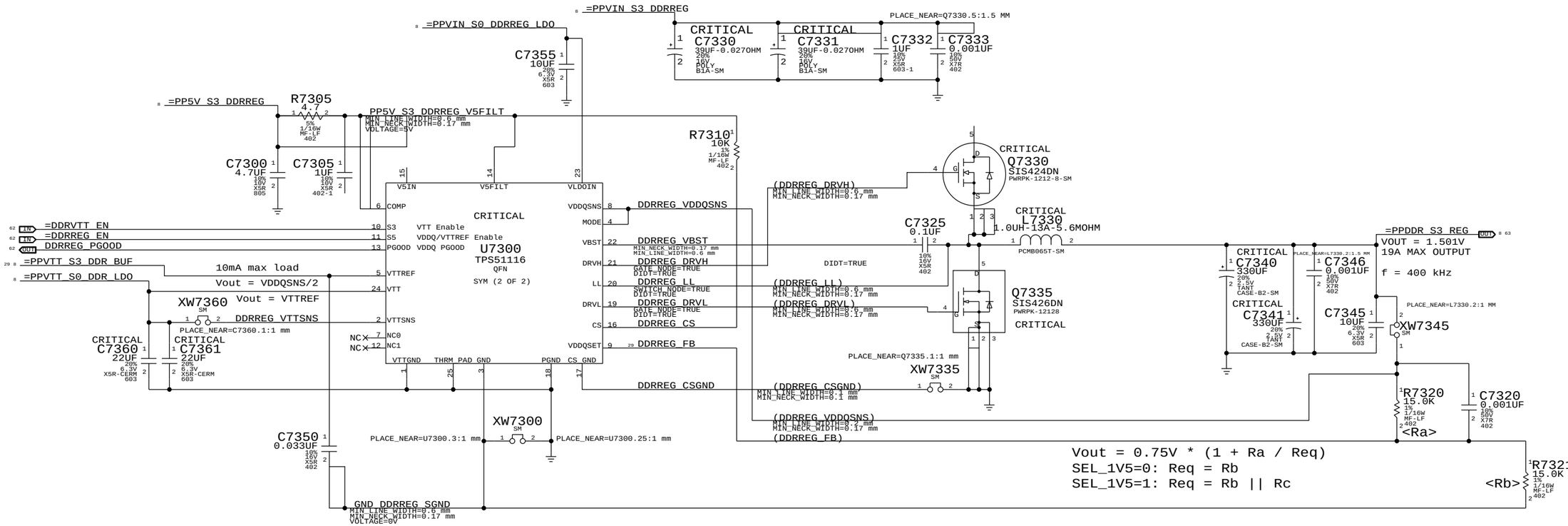
1.5V/0.75 DDR3 POWER SUPPLY



NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS
NOTE: DONT SYNC THIS PAGE FROM K6 REMOVED R7380

SYNC_MASTER=(K6_MLB) SYNC_DATE=(11/06/2009)

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

	2PHASE	1PHASE
PWM Freq.	300 kHz	300 kHz
Max Current	44 A	17.6 A
Load Line	-2.107 mV/A	-4 mV/A

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

IMVP6:1PHASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES,MTL FILM,1/16W,8.25K,1,0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES,MTL FILM,1/16W, 16.9K, 1,0402,SM,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER, .22UF,20,6.3V,X5R,0402	C7428		IMVP6:1PHASE
114S0236	1	RES,MTL FILM,1/16W,1.58K,1,0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES,MTL FILM,1/16W,255 OHM,1,0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP CER 470PF,+/-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES,MTL FILM,1/16W,97.6K,1,0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X7R,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,100PF,5%,50V,CC0402	C7413		IMVP6:1PHASE
132S0099	1	CAP,X5R,0.1UF,10%,16V,0402	C7434		IMVP6:1PHASE

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_VSEN_P	0.25 MM	0.25 MM
IMVP6_VSEN_N	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	1.5 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

SYNC_MASTER=(K84_MLB) SYNC_DATE=(11/18/2009)

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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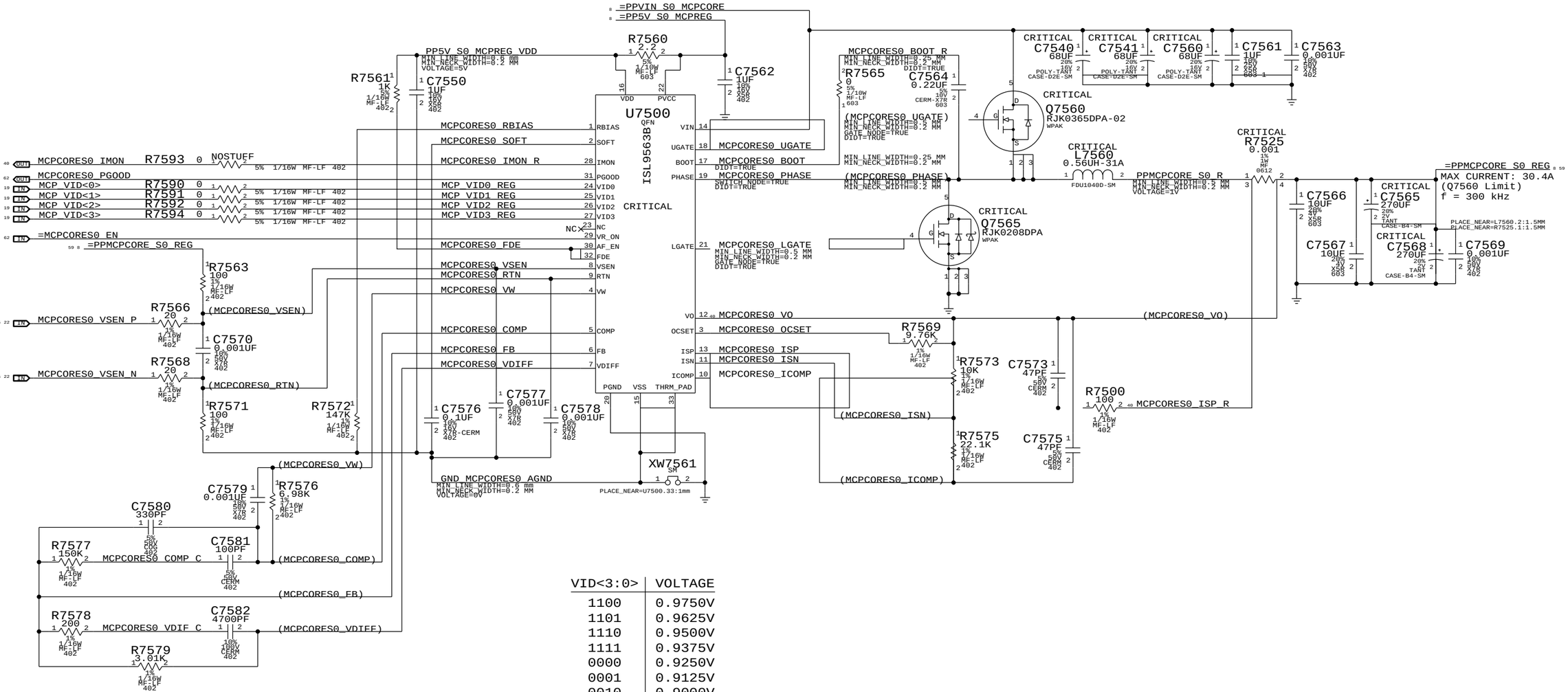

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC_MASTER=(K6_MLB) SYNC_DATE=(10/27/2009)

PAGE TITLE: MCP VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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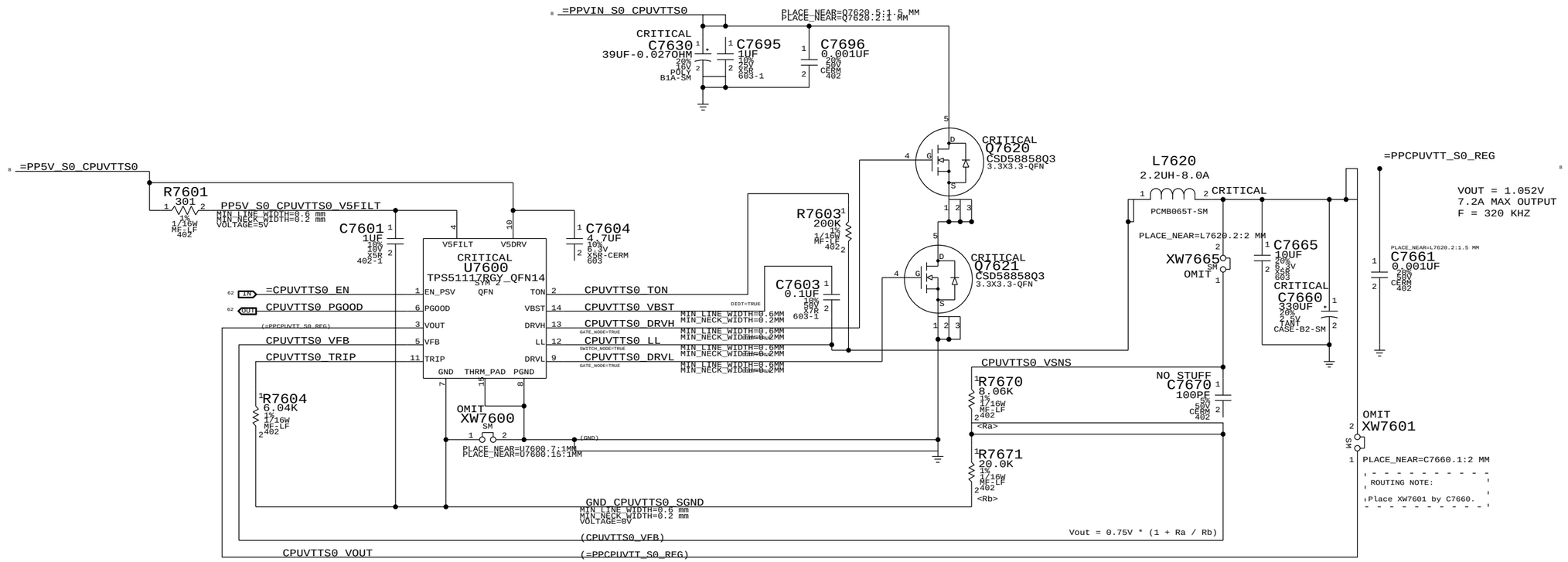
CPUVTT POWER SUPPLY



SYNC_MASTER=(K84 MLB)	SYNC_DATE=(02/04/2009)
PAGE TITLE	CPU VTT(1.05V) SUPPLY
Apple Inc.	DRAWING NUMBER 051-8561 · SIZE D
	REVISION C.0.0
	BRANCH
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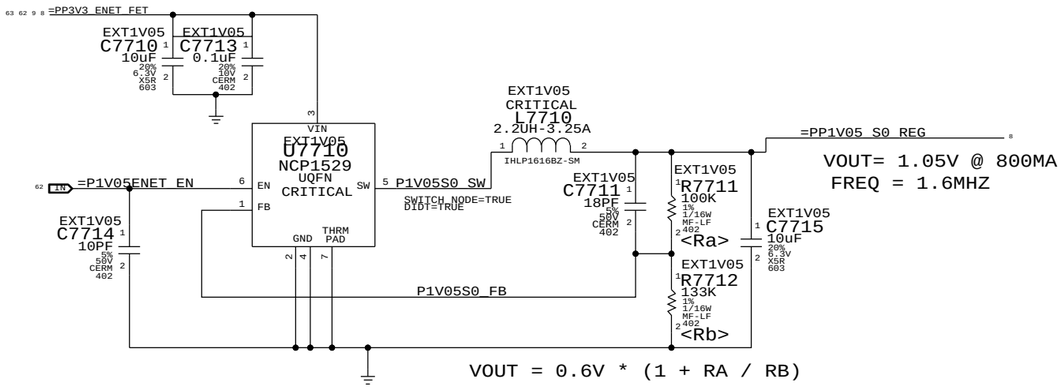
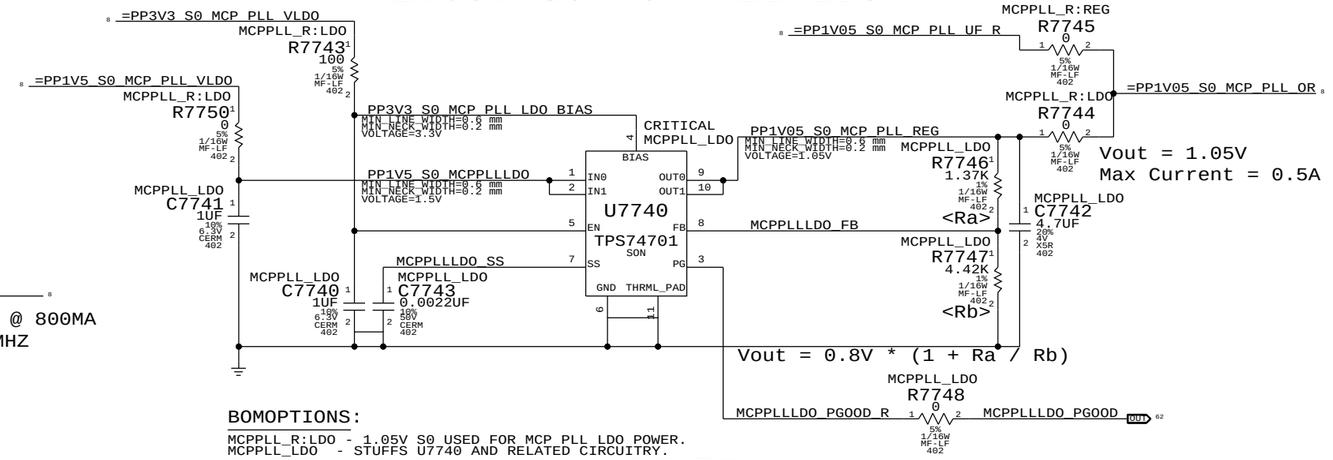
1.05V ENET Switcher



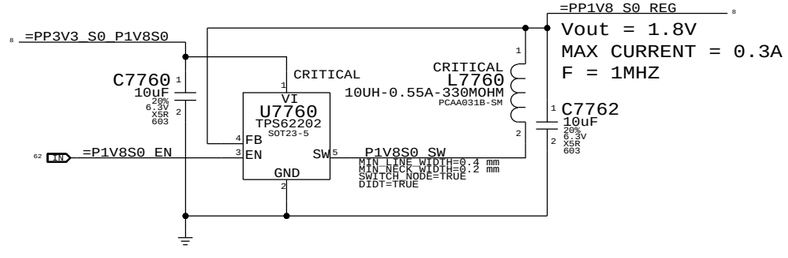
1.05V S0 MCP PLL LDO



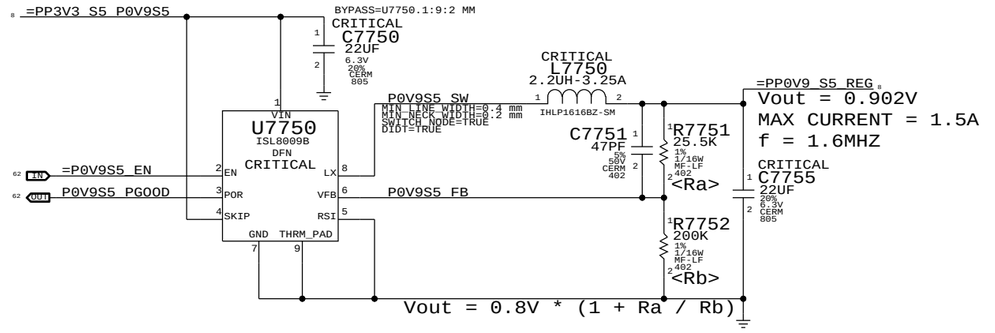
BOMOPTIONS:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

1.8V S0 Switcher



MCP 0.9V S5 (AUXC) Switcher



K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 77 OF 109
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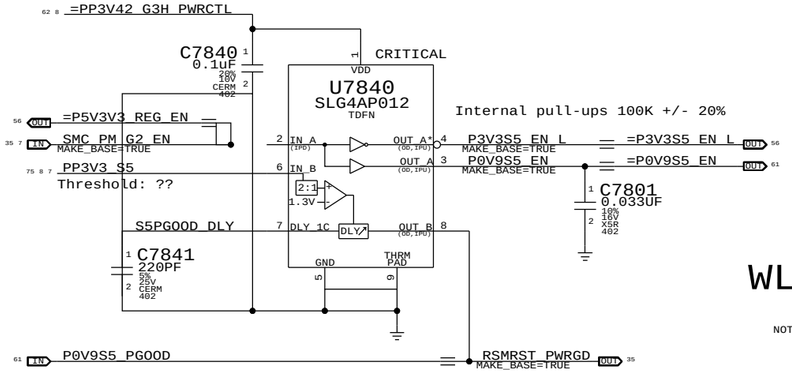
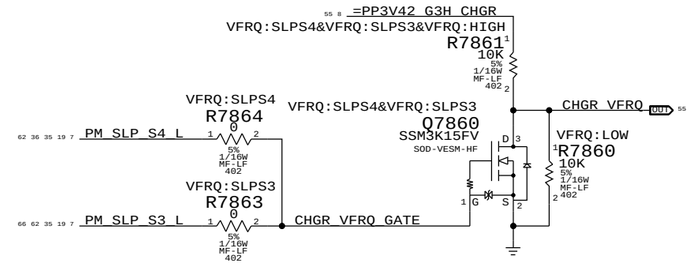
S5 Rail Enables & PGOOD



Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

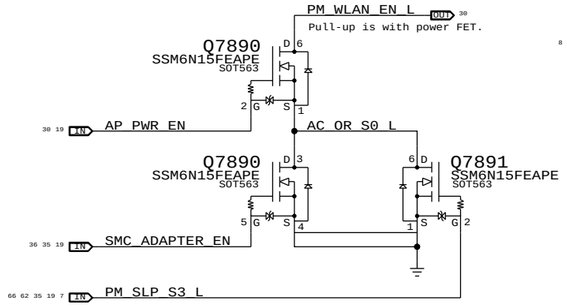
ISL6259 Frequency Select



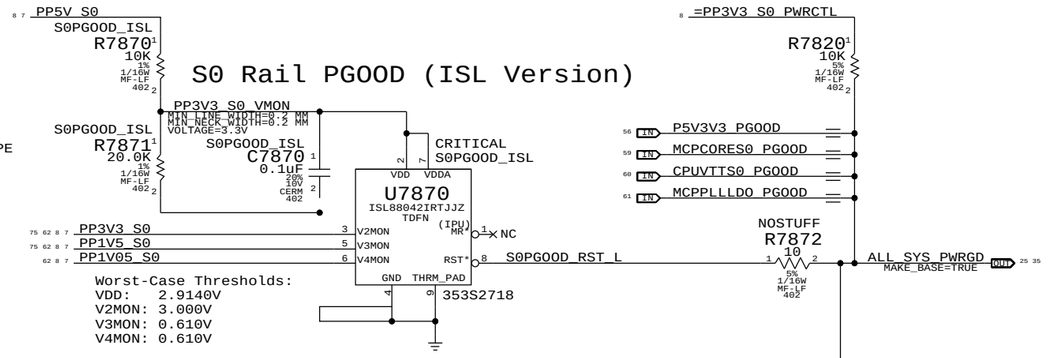
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

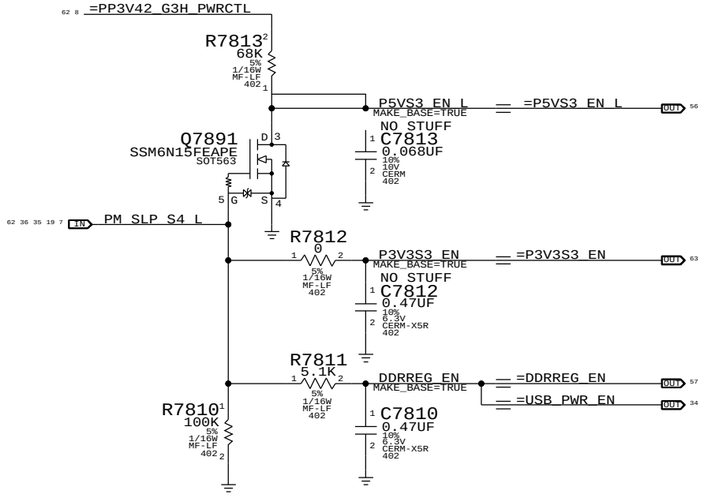
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



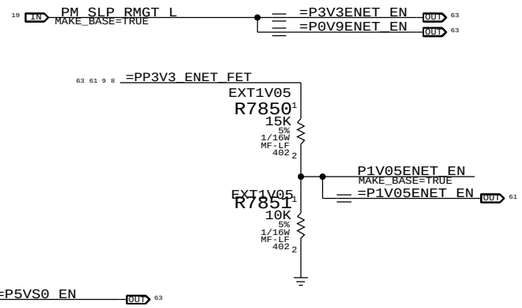
S0 Rail PGOOD Circuitry



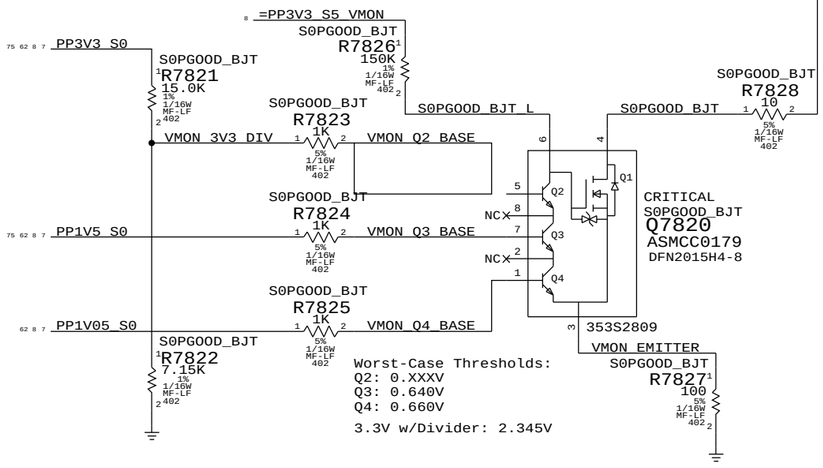
S3 Rail Enables



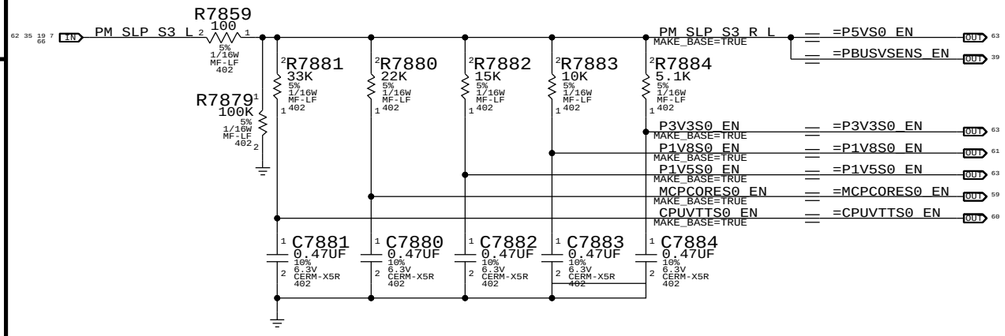
ENET Rail Enables



S0 Rail PGOOD (BJT Version)



S0 Rail Enables



VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

DO NOT SYNC T27, ENET RAILS CHANGED

Unused PGOOD signal

SYNC MASTER=(T27 MLB) SYNC DATE=(10/27/2009)

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

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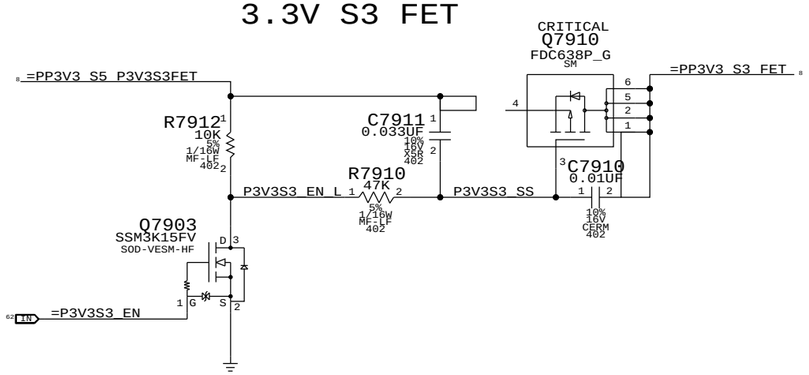
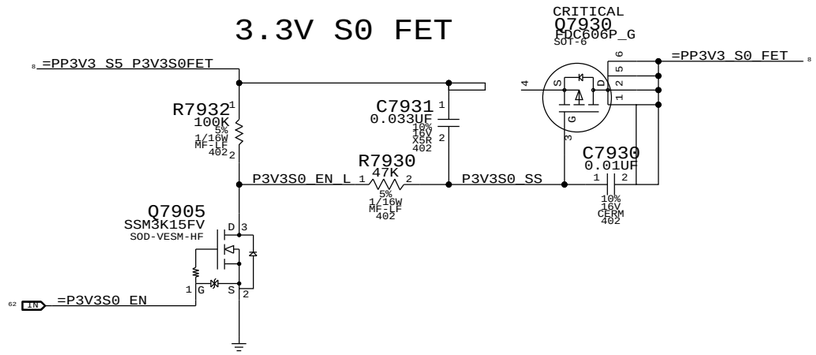
3.3V S3 FET



3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.811 A (EDP)

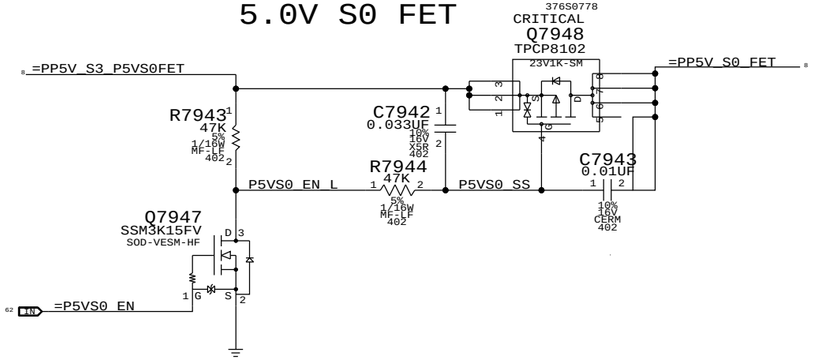
3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.240 A (EDP)

(Used to be 5.0V LT S0 FET)

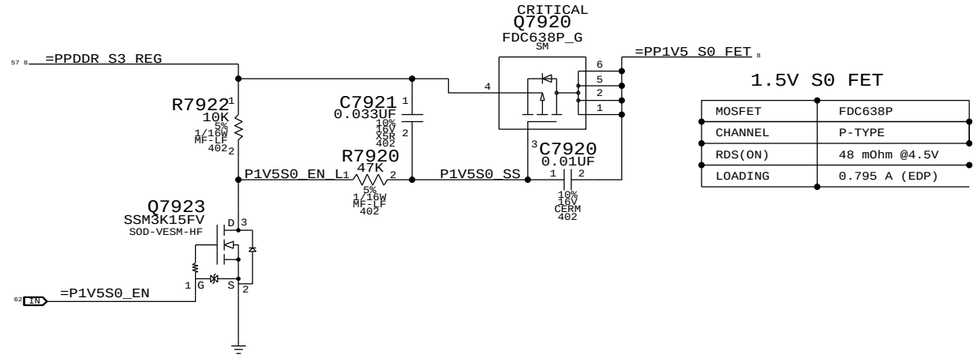
5.0V S0 FET



5.0V LT S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.569 A (EDP)

DO NOT SYNC FROM K84. ADDED ENET CIRCUITS, REMOVED 1V05 ENET CIRCUIT

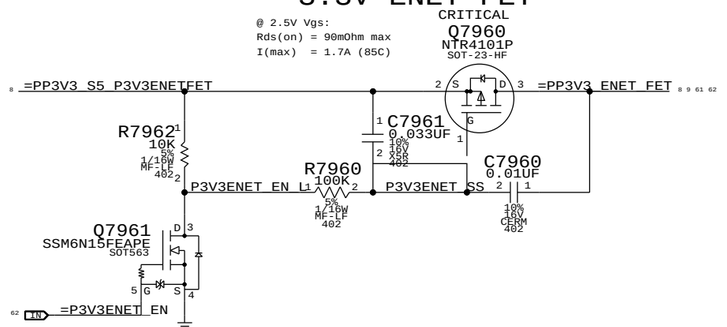
1.5V S0 FET



1.5V S0 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.795 A (EDP)

3.3V ENET FET

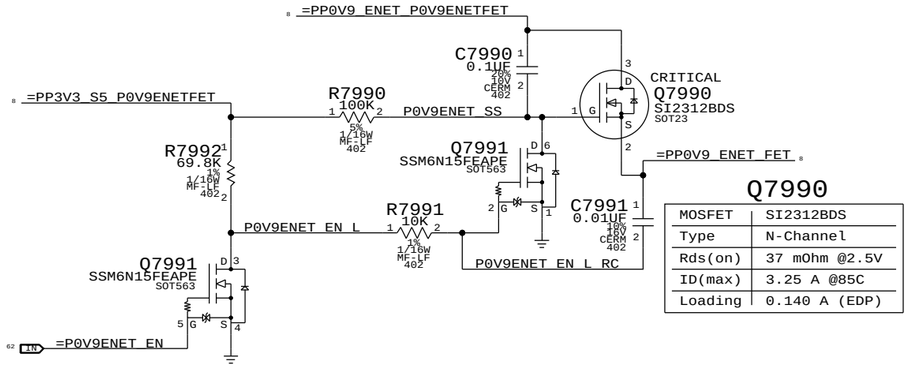
@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

0.9V ENET FET



Q7990	
MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: POWER FETS

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D

REVISION: C.0.0

BRANCH:

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CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

LCD CONNECTOR

LVDS CONNECTOR:518S0650

FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY

CRITICAL J9000 20474-030E-11 F-RT-SM

LVDS I/F

LED BKLT I/F

CAMERA I/F

CAMERA

PLACEMENT_NOTE=PLACE CLOSE TO J9000.

SYNC MASTER=(K84 MLB)	SYNC DATE=(10/19/2009)
PAGE TITLE	LVDS CONNECTOR
Apple Inc.	DRAWING NUMBER 051-8561 SIZE D
	REVISION C.0.0
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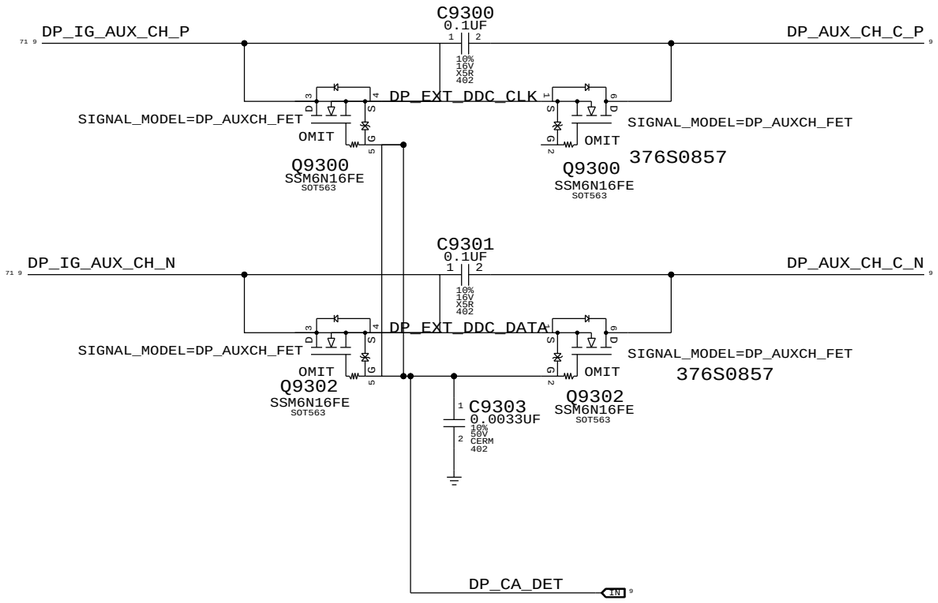

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0859	2	XSTR,FT,N-CH,DUAL,SOT-563	Q9300,Q9302	CRITICAL	

SYNC_MASTER=K6_MLB SYNC_DATE=02/16/2010

PAGE TITLE
DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER 051-8561 SIZE D
REVISION C.0.0
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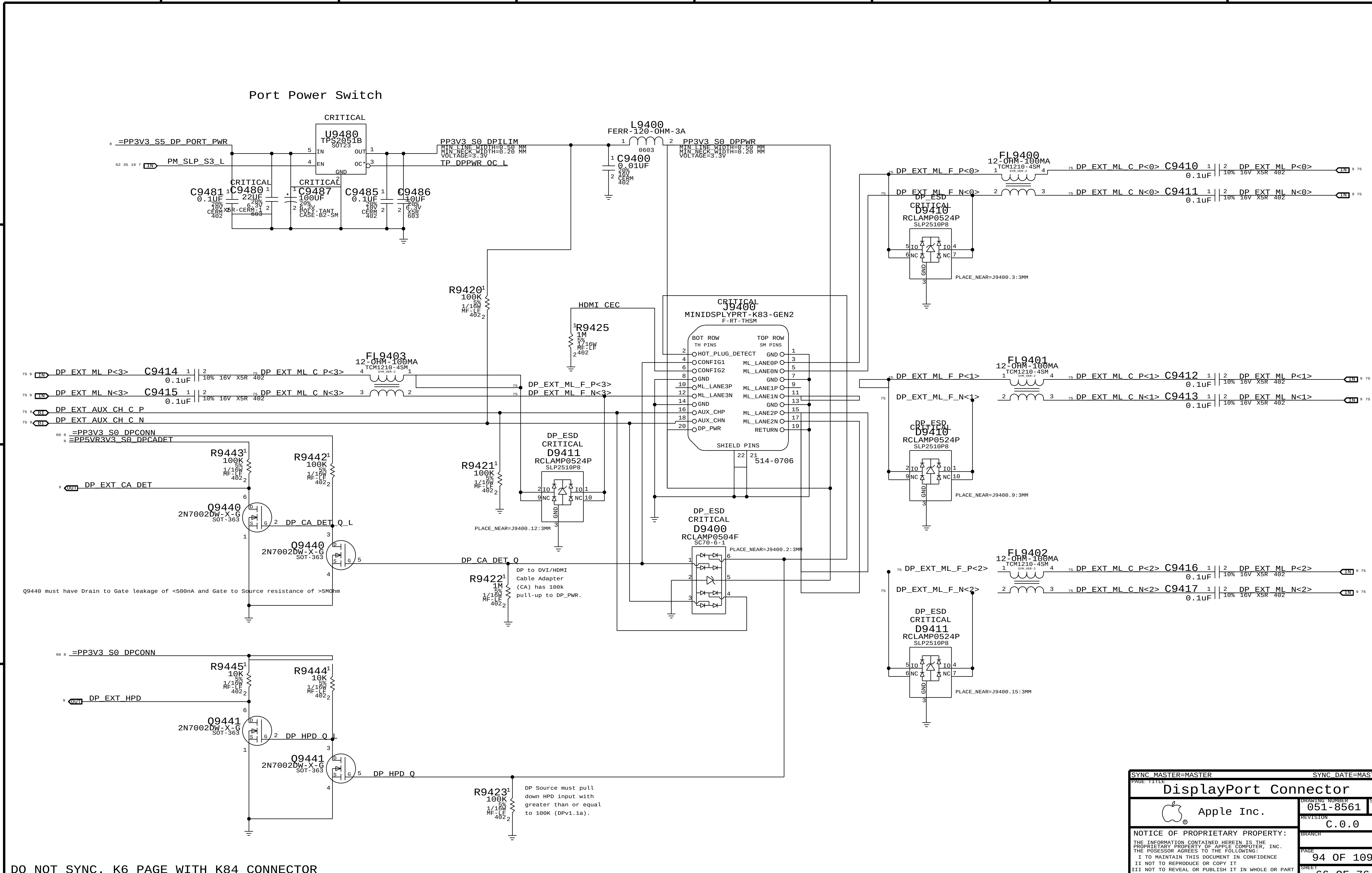
Port Power Switch
CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TP_DPPWR_OC_L
L9400
FERR-120-OHM-3A
0603
PP3V3_S0_DPPWR
C9400
0.01UF
C9481
0.1UF
C9480
22UF
C9487
100UF
POLY-TANT
CASE-B2-SM
C9485
0.1UF
C9486
10UF
FL9400
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_F_P<0>
DP_EXT_ML_F_N<0>
DP_EXT_ML_C_P<0>
DP_EXT_ML_C_N<0>
C9410
C9411
DP_EXT_ML_P<0>
DP_EXT_ML_N<0>
DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8
PLACE_NEAR=J9400.3:3MM
R9420
100K
HDMI_CEC
R9425
1M
CRITICAL
J9400
MINIDSPLYPRT-K83-GEN2
F-RT-THSM
BOT ROW
TH PINS
TOP ROW
SM PINS
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
514-0706
FL9403
12-OHM-100MA
DP_EXT_ML_P<3>
DP_EXT_ML_N<3>
C9414
C9415
0.1uF
DP_EXT_ML_C_P<3>
DP_EXT_ML_C_N<3>
DP_EXT_ML_F_P<3>
DP_EXT_ML_F_N<3>
DP_EXT_AUX_CH_C_P
DP_EXT_AUX_CH_C_N
FL9401
DP_EXT_ML_F_P<1>
DP_EXT_ML_F_N<1>
DP_EXT_ML_C_P<1>
DP_EXT_ML_C_N<1>
C9412
C9413
DP_EXT_ML_P<1>
DP_EXT_ML_N<1>
PLACE_NEAR=J9400.9:3MM
=PP3V3_S0_DPCONN
=PP5VR3V3_S0_DPCADET
R9443
100K
R9442
100K
DP_EXT_CA_DET
Q9440
2N7002DW-X-G
SOT-363
DP_CA_DET_Q_L
DP_CA_DET_Q
R9421
100K
D9411
PLACE_NEAR=J9400.12:3MM
D9400
RCLAMP0504F
SC70-6-1
PLACE_NEAR=J9400.2:3MM
R9422
1M
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm
FL9402
DP_EXT_ML_F_P<2>
DP_EXT_ML_F_N<2>
DP_EXT_ML_C_P<2>
DP_EXT_ML_C_N<2>
C9416
C9417
DP_EXT_ML_P<2>
DP_EXT_ML_N<2>
PLACE_NEAR=J9400.15:3MM
R9445
10K
R9444
10K
DP_EXT_HPD
Q9441
DP_HPD_Q_L
DP_HPD_Q
R9423
100K
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
DO NOT SYNC. K6 PAGE WITH K84 CONNECTOR

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-8561 SIZE D

REVISION C.0.0

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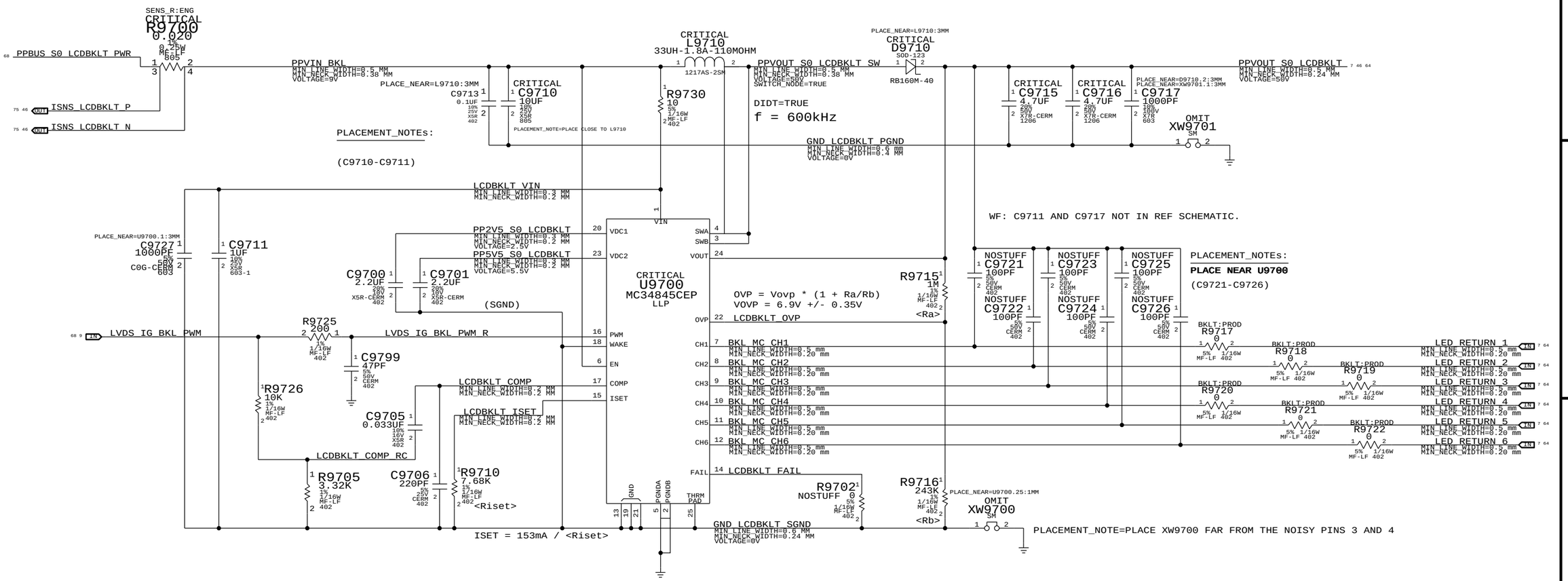


13.3 Inch, K84 Panel (9 LEDs per string)

TARGET: ISET = 20mA, OVP = 35V
ACTUAL: ISET = 19.9mA, OVP = 35.2V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
101S0075	1	RES,MF,0 OHM,5%,1/8W,SMD,LF,0805	R9700		SENS_R:PROD

10.2 ohm resistors for current measurement on LED strings.

DO NOT SYNC FROM K84. L9710 CHANGED TO K6/K69

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: LCD Backlight Driver (MC34845)

Apple Inc.

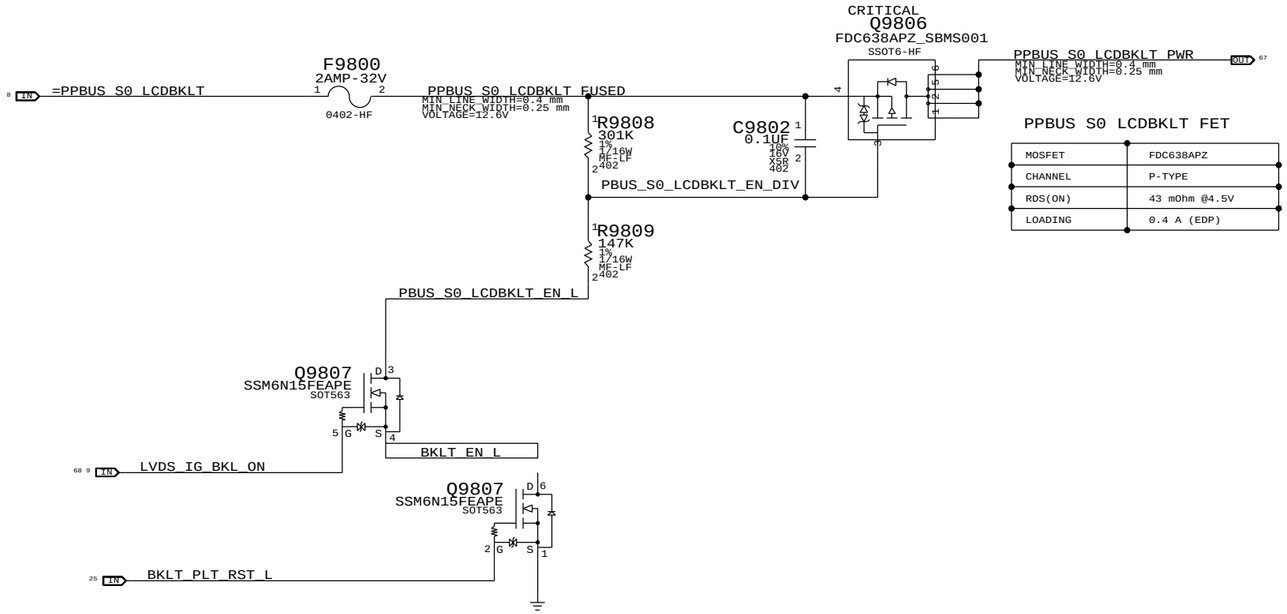
DRAWING NUMBER: 051-8561 SIZE: D

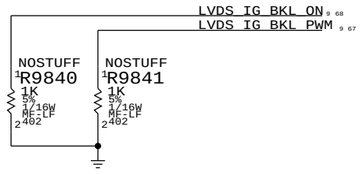
REVISION: C.0.0

BRANCH:

PAGE: 97 OF 109

SHEET: 67 OF 76





MCP79 HAD INTERNAL 10K PULL-UP FOR THESE SIGNALS
MCP89 DRIVES THEM LOW

SYNC_MASTER=(K84_MLB) SYNC_DATE=(10/19/2009)

PAGE TITLE
LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-8561 SIZE D
REVISION C.0.0
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 36
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 36
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	10 14 58
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	14 58
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	58
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 29
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	10 13
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	11 58
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 58
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	58
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	58

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	15 26
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	15 26
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM_A_CKE<3..0>	15 21 26
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_CS_L<3..0>	15 26
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM_A_ODT<3..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	15 26
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 28
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	15 27
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM_B_CKE<3..0>	15 21 27
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_CS_L<3..0>	15 27
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM_B_ODT<3..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	15 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

SYNC_MASTER=T27_MLB SYNC_DATE=02/16/2010

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-8561 SIZE: D
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_AP_R2D_P	9
	PCIE_90D	PCIE	PCIE_AP_R2D_N	9
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P	9 16
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N	9 16
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P	9 16
	PCIE_90D	PCIE	PCIE_AP_D2R_N	9 16
	PCIE_90D	PCIE	PCIE_ENET_R2D_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P	9 16
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N	9 16
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P	9 16
	PCIE_90D	PCIE	PCIE_ENET_D2R_N	9 16
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	9 16
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	9 16
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	9 16
	PCIE_90D	PCIE	PCIE_FW_D2R_N	9 16
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N	9 16
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	9 16
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	9 16
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP	16
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS_IG_TXD_P<5..0>	
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS_IG_TXD_N<5..0>	
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML_P<3..0>	9
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML_N<3..0>	9
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH_P	9 65
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH_N	9 65
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET	17 24
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE	17 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	9 64
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	9 64
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	7 9 64
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	7 9 64
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 24
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 33
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 33
	SATA_90D	SATA	SATA_HDD_R2D_P	7 33
	SATA_90D	SATA	SATA_HDD_R2D_N	7 33
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	18 33
	SATA_90D	SATA	SATA_HDD_D2R_N	18 33
	SATA_90D	SATA	SATA_HDD_D2R_C_P	7 33
	SATA_90D	SATA	SATA_HDD_D2R_C_N	7 33
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	18 33
	SATA_90D	SATA	SATA_ODD_R2D_C_N	18 33
	SATA_90D	SATA	SATA_ODD_R2D_P	7 33
	SATA_90D	SATA	SATA_ODD_R2D_N	7 33
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	18 33
	SATA_90D	SATA	SATA_ODD_D2R_N	18 33
	SATA_90D	SATA	SATA_ODD_D2R_C_P	7 33
	SATA_90D	SATA	SATA_ODD_D2R_C_N	7 33
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	18

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	19 35 37
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	19 35 37
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 35
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	25 37
USB_EXTA	USB_90D	USB	USB EXTA P	18 34
	USB_90D	USB	USB EXTA N	18 34
	USB_90D	USB	USB EXTA MUXED P	34 75
	USB_90D	USB	USB EXTA MUXED N	34 75
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXTD P	9 18
	USB_90D	USB	USB EXTD N	9 18
USB_CAMERA	USB_90D	USB	USB CAMERA P	18 64
	USB_90D	USB	USB CAMERA N	18 64
USB_BT	USB_90D	USB	USB BT P	18 30
	USB_90D	USB	USB BT N	18 30
USB_TPAD	USB_90D	USB	USB TPAD P	18 43
	USB_90D	USB	USB TPAD N	18 43
USB_IR	USB_90D	USB	USB IR P	9 18
	USB_90D	USB	USB IR N	9 18
USB_EXTB	USB_90D	USB	USB EXTB P	18 34
	USB_90D	USB	USB EXTB N	18 34
USB_T57	USB_90D	USB	USB T57 P	9 18
	USB_90D	USB	USB T57 N	9 18
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	9 18
	USB_90D	USB	USB SDCARD N	9 18
USB_WM	USB_90D	USB	USB WM P	9 18
	USB_90D	USB	USB WM N	9 18
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP USB RBIAS GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	13 19 38
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	13 19 38
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 38
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 38
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	19 48
	HDA_55S	HDA	HDA BIT CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	19 48
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST R L	19
	HDA_55S	HDA	HDA RST L	19 48
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	19 48
	HDA_55S	HDA	HDA SDIN CODEC	48
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	19 48
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 35
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 37
	SPI_55S	SPI	SPI CLK	7 37
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 37
	SPI_55S	SPI	SPI MOSI	7 37
SPI_MISO	SPI_55S	SPI	SPI MISO	7 19 37
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 37
	SPI_55S	SPI	SPI CS0 L	7 37
	SPI_55S	SPI	SPI MLB CLK	37 47
	SPI_55S	SPI	SPI MLB MOSI	37 47
	SPI_55S	SPI	SPI MLB MISO	37 47
	SPI_55S	SPI	SPI MLB CS L	37 47
	SPI_55S	SPI	SPI ALT CLK	37
	SPI_55S	SPI	SPI ALT MOSI	37
	SPI_55S	SPI	SPI ALT MISO	37
	SPI_55S	SPI	SPI ALT CS L	37

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	9 31
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 31
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	9 31
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 31
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	9 31
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	9 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	9 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	9 31
	ENET_MII_55S	ENET_MII	ENET_RESET_L	9 31
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 32
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 32
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	32
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	32

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 7 38
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 7 38
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 38
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 38
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 38
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 38
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 7 38
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 7 38
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 38
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 38

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 55
	1TO1_DIFFPAIR		CHGR_CSI_N 55
	1TO1_DIFFPAIR		CHGR_CSI_R_P 55
	1TO1_DIFFPAIR		CHGR_CSI_R_N 55
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 55
	1TO1_DIFFPAIR		CHGR_CSO_N 55
	1TO1_DIFFPAIR		CHGR_CSO_R_P 40 55
	1TO1_DIFFPAIR		CHGR_CSO_R_N 40 55

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	5.8 MM		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(PCIE_AP)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P	34 72
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N	34 72
(USB_EXTA)	USB_90D	USB	USB_LT1_P	
(USB_EXTA)	USB_90D	USB	USB_LT1_N	
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_P	43
(USB_TPAD)	USB_90D	USB	USB_TPAD_R_N	43
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 64
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 64
	USB_90D	USB	USB_LT2_P	
	USB_90D	USB	USB_LT2_N	
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	
	SATA_90D	SATA	SATA_ODD_R2D_UF_P	33
	SATA_90D	SATA	SATA_ODD_R2D_UF_N	33
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	33
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	33
	SATA_90D	SATA	SATA_HDD_D2R_FILT_P	33
	SATA_90D	SATA	SATA_HDD_D2R_FILT_N	33
	SATA_90D	SATA	SATA_HDD_D2R_UF_P	33
	SATA_90D	SATA	SATA_HDD_D2R_UF_N	33
	SATA_90D	SATA	SATA_HDD_R2D_UF_P	33
	SATA_90D	SATA	SATA_HDD_R2D_UF_N	33
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P	
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N	
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P	
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N	
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P	
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N	
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P	
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N	
	SATA_90D	SATA	SATA_HDD_D2R_NORDRV_P	
	SATA_90D	SATA	SATA_HDD_D2R_NORDRV_N	
	SATA_90D	SATA	SATA_HDD_R2D_NORDRV_P	
	SATA_90D	SATA	SATA_HDD_R2D_NORDRV_N	
PCIE_AP_D2R	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_P	7 9 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_N	7 9 30
PCIE_AP_R2D	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_P	7 9 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_N	7 9 30
USB_BT	USB_90D	USB	CONN_USB2_BT_P	7 30
	USB_90D	USB	CONN_USB2_BT_N	7 30
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	7 64
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	7 64
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
(129) USB_EXTA	USB_90D	USB	CONN_USB_EXTA_P	34
(129)	USB_90D	USB	CONN_USB_EXTA_N	34
(129) USB_EXTB	USB_90D	USB	CONN_USB_EXTB_P	34
(129)	USB_90D	USB	CONN_USB_EXTB_N	34

GRAPHICS NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0>	9 66
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0>	9 66
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0>	66
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0>	66
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0>	66
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0>	66
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P	9 66
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N	9 66
	DP_90D	DISPLAYPORT	DP_EXT_DDC_DATA	65
	DP_90D	DISPLAYPORT	DP_EXT_DDC_CLK	65

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	CPUTHMSNS_D1_P	41
	THERM_1TO1_55S	THERM	CPUTHMSNS_D1_N	41
(1380) CPUTHMSNS_D2	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	41
(1383)	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	41
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 41
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 41
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_P	
	THERM_1TO1_55S	THERM	MCPTHMSNS_D2_N	
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	19 41
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	19 41
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	30 46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	30 46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	46
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	33 46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	33 46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	46 67
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	46 67
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_P	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	33 46
	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	33 46
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	46
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_P	40
	SENSE_1TO1_55S	SENSE	ISNS_CPUVTT_N	40
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P	22 59
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N	22 59
PWR		MEM_POWER	PP1V5R1V35_S3	7 8
		SB_POWER	PP3V3_S5	7 8 62
		SB_POWER	PP3V3_S0	7 8 62
		SB_POWER	PP1V5_S0	7 8 62
		GND	GND	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR	AUDIO	AUD_SPKRAMP_LIN_P	
	DIFFPAIR	AUDIO	AUD_SPKRAMP_LIN_N	
	DIFFPAIR	AUDIO	AUD_SPKRAMP_SUBIN_P	
	DIFFPAIR	AUDIO	AUD_SPKRAMP_SUBIN_N	
	DIFFPAIR	AUDIO	AUD_SPKRAMP_RIN_P	
	DIFFPAIR	AUDIO	AUD_SPKRAMP_RIN_N	
	DIFFPAIR	AUDIO	SSM2315L_P	
	DIFFPAIR	AUDIO	SSM2315L_N	
	DIFFPAIR	AUDIO	SSM2315S_P	
	DIFFPAIR	AUDIO	SSM2315S_N	
	DIFFPAIR	AUDIO	SSM2315R_P	
	DIFFPAIR	AUDIO	SSM2315R_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	
	DIFFPAIR	AUDIO	BI_MIC_P	7 52 53
	DIFFPAIR	AUDIO	BI_MIC_N	7 52 53
	DIFFPAIR	AUDIO	HS_MIC_P	52 53
	DIFFPAIR	AUDIO	HS_MIC_N	52 53

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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K87 SPECIFIC CONSTRAINTS

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K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5X_DIELECTRIC	TOP,BOTTOM	0.105 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
1.5X_DIELECTRIC	*	0.095 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_405	BGA_P1MM	STANDARD

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