1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,WHITE_ARROW,MLB,K18

02/01/10

ALIASES RESOLVED

Schematic / PCB #'s

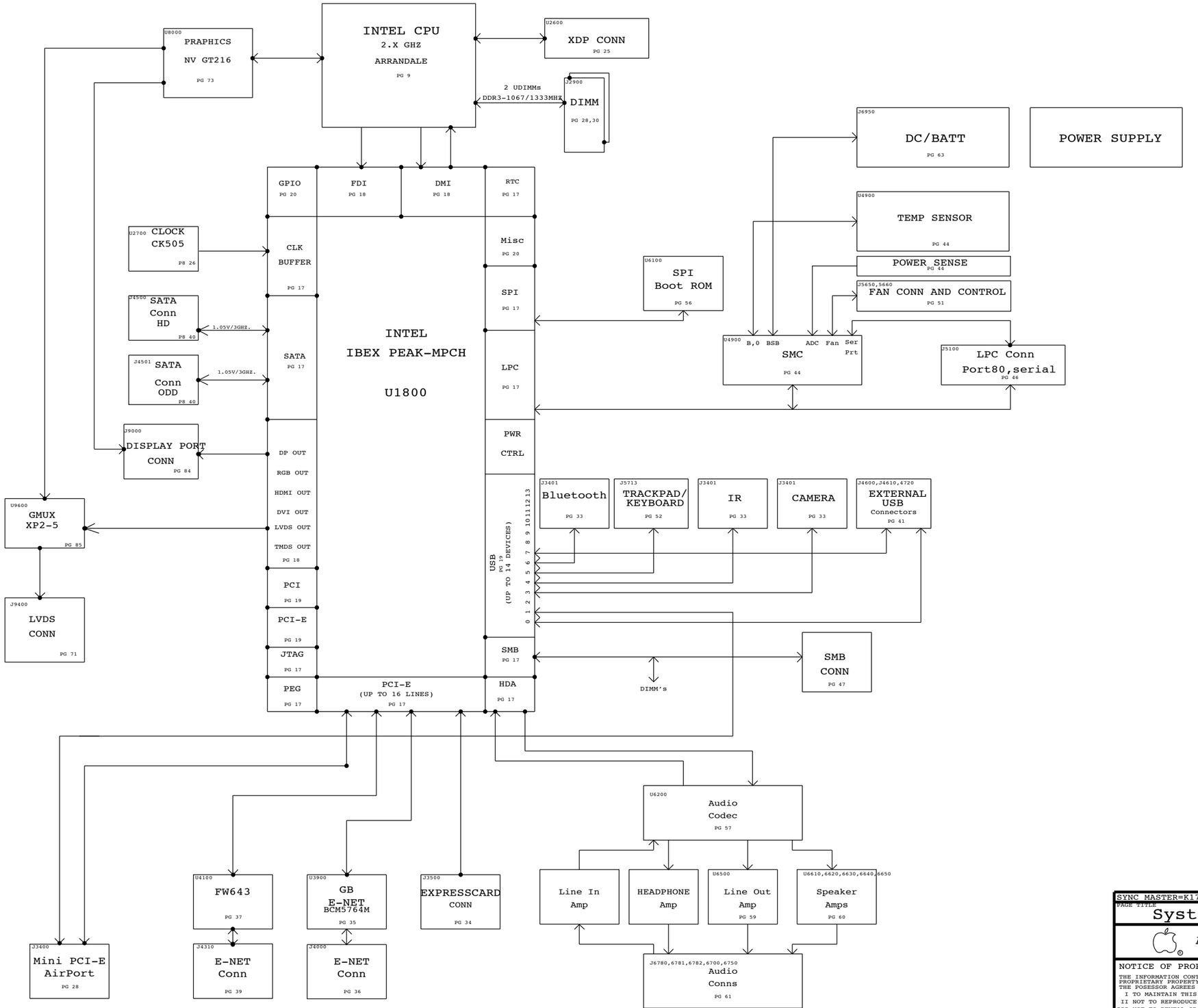
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8504	1	SCHEM,WHITE_ARROW,MLB,K18	SCH	CRITICAL	
820-2850	1	PCBF,WHITE_ARROW,MLB,K18	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Feb 1 10:13:48 2010

DRAWING TITLE: SCHEM,WHITE_ARROW,MLB,K18

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 132
SHEET: 1 OF 101



SYNC MASTER=K17 REF SYNC DATE=06/30/2009

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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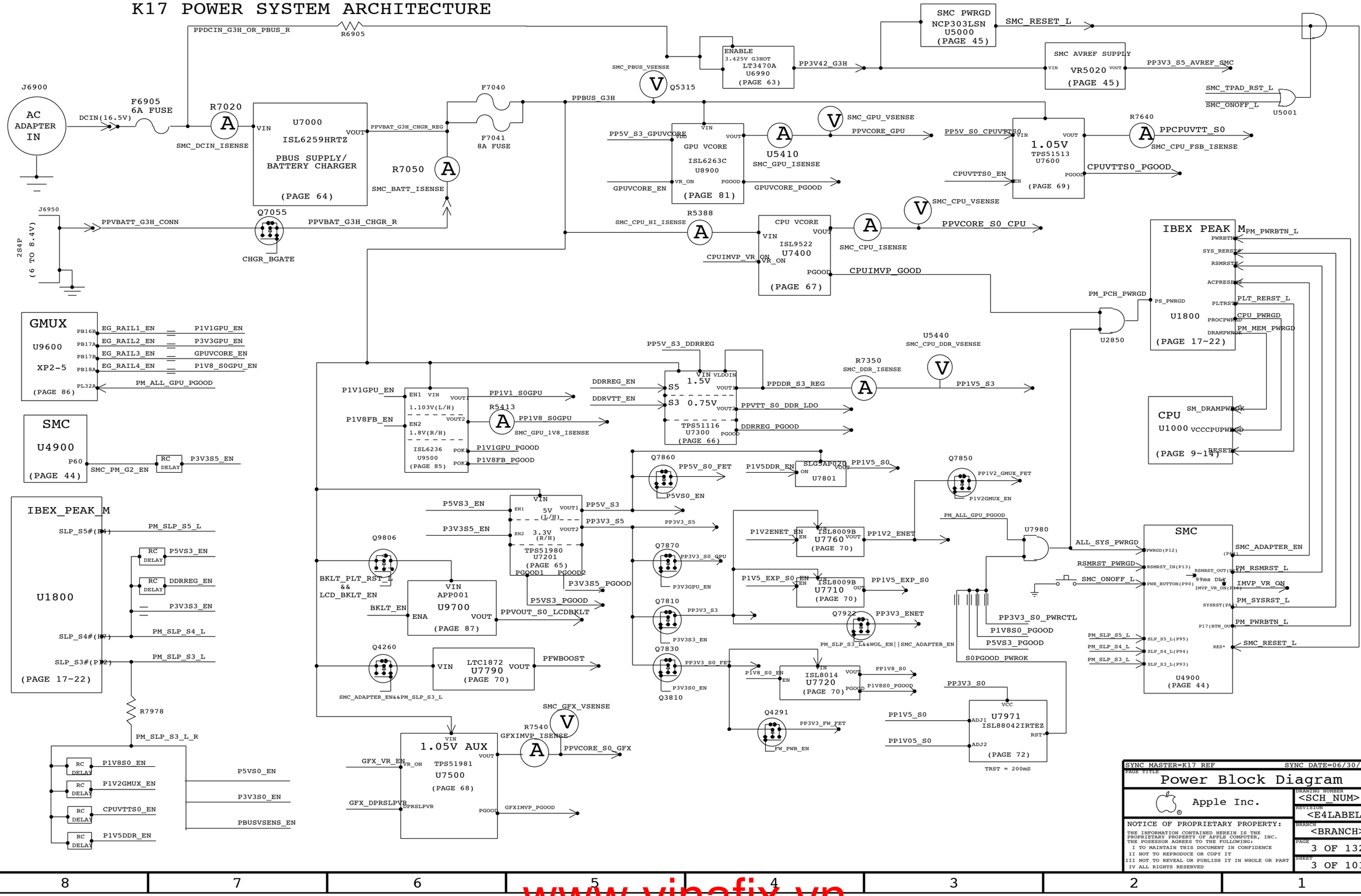
K17 POWER SYSTEM ARCHITECTURE



PROTO:

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0952	PCBA,2.0G,512SAM_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_SAMSUNG,K18_PVT,EEEE_DCJ7
639-0953	PCBA,2.0G,512HYN_VRAM,K18	K18_COMMON,CPU_2_4GHZ,FB_256_HYNIX,K18_PVT,EEEE_DCJ8
639-0954	PCBA,2.13G,512SAM_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJ9
639-0955	PCBA,2.13G,512HYN_VRAM,K18	K18_COMMON,CPU_2_53GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJC
639-0956	PCBA,2.4G,512SAM_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_SAMSUNG,K18_PVT,EEEE_DCJD
639-0957	PCBA,2.4G,512HYN_VRAM,K18	K18_COMMON,CPU_2_66GHZ,FB_512_HYNIX,K18_PVT,EEEE_DCJF
085-1404	K18 DEVELOPMENT BOM	

K18 BOM GROUPS

BOM GROUP	BOM OPTIONS
K18_COMMON	ALTERNATE,COMMON,K18_COMMON1,K18_COMMON2,K18_PROGPARTS,USBHUB_2061,RDRV:8515A2,DCI
K18_COMMON1	BATT_3S,BCM5764M,GL137,CPUPOC_IMAX_40_50,CPUMEM_S0,SMC_EXCARD_NOT,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM
K18_COMMON2	GMUXPLL_3V3,GPU_SS_INT,MIKEY,GPUVID_0P90V,DPMUX_EN_PLD,DP_CA_DET_EG_PLD,DP_ESD,VFRQ_SLPS3,SMC_OSC_YES,RAIL_MON
K18_PVT	BMON_PROD,VREFMRGN_NOT,XDP,XDP_NORMAL,XDP_CPU_BPM
K18_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG,FB1V55
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX,FB1V55
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG,FB1V35
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX,FB1V35

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
333S0506	333S0535		ALL	Hynix 900M alt to 1000M
516S0805	516S0806		ALL	Molex alt to Foxconn
152S1102	152S1088		ALL	Mag layer alt to Vishay
353S2805	353S2603		ALL	Fairchild wafer option
333S0542	333S0507		ALL	Samsung I die alt to H
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
337S3808	337S3839		ALL	A02 alt to A03 GPU
128S0305	128S0294		ALL	6.3V alt to 11V Sanyo

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ7]	CRITICAL	EEEE_DCJ7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ8]	CRITICAL	EEEE_DCJ8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJ9]	CRITICAL	EEEE_DCJ9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJC]	CRITICAL	EEEE_DCJC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJD]	CRITICAL	EEEE_DCJD
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DCJF]	CRITICAL	EEEE_DCJF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3848	1	ARD,SLBPE,PRQ,2.66G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3847	1	ARD,SLBPF,PRQ,2.53G,35W,C2,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3846	1	ARD,SLBNA,PRQ,2.4G,35W,C2,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IC,PCH,IBEX PEAK-M,SLGZS,PRQ,B3,BGA	U1800	CRITICAL	
337S3839	1	IC,GPU,NV GT216 LP++,969BGA,40NM,A03	U8000	CRITICAL	
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER,8x8,64 QFN	U3900	CRITICAL	BCM5764M
341S2731	1	IC,1MBIT,SPI FLASH,K17/K18	U3990	CRITICAL	
338S0753	1	IC,FW643-E2,1394b PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0233	1	IC,SMC,K18	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2562	1	IC,EFI ROM,DEVELOPMENT,K18	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC,PSOC +W/USB,56PIN,MLF,K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2566	1	IC,CPLD,LATTICE,132CSBGA,K18	U9600	CRITICAL	GMUX_PROG
333S0507	4	IC,SGRAM,GDDR3,16MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SDRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0533	4	IC,SGRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC,SDRAM,GDDR3,32MX32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1404	1	K18 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=K17_REF SYNC DATE=05/28/2009

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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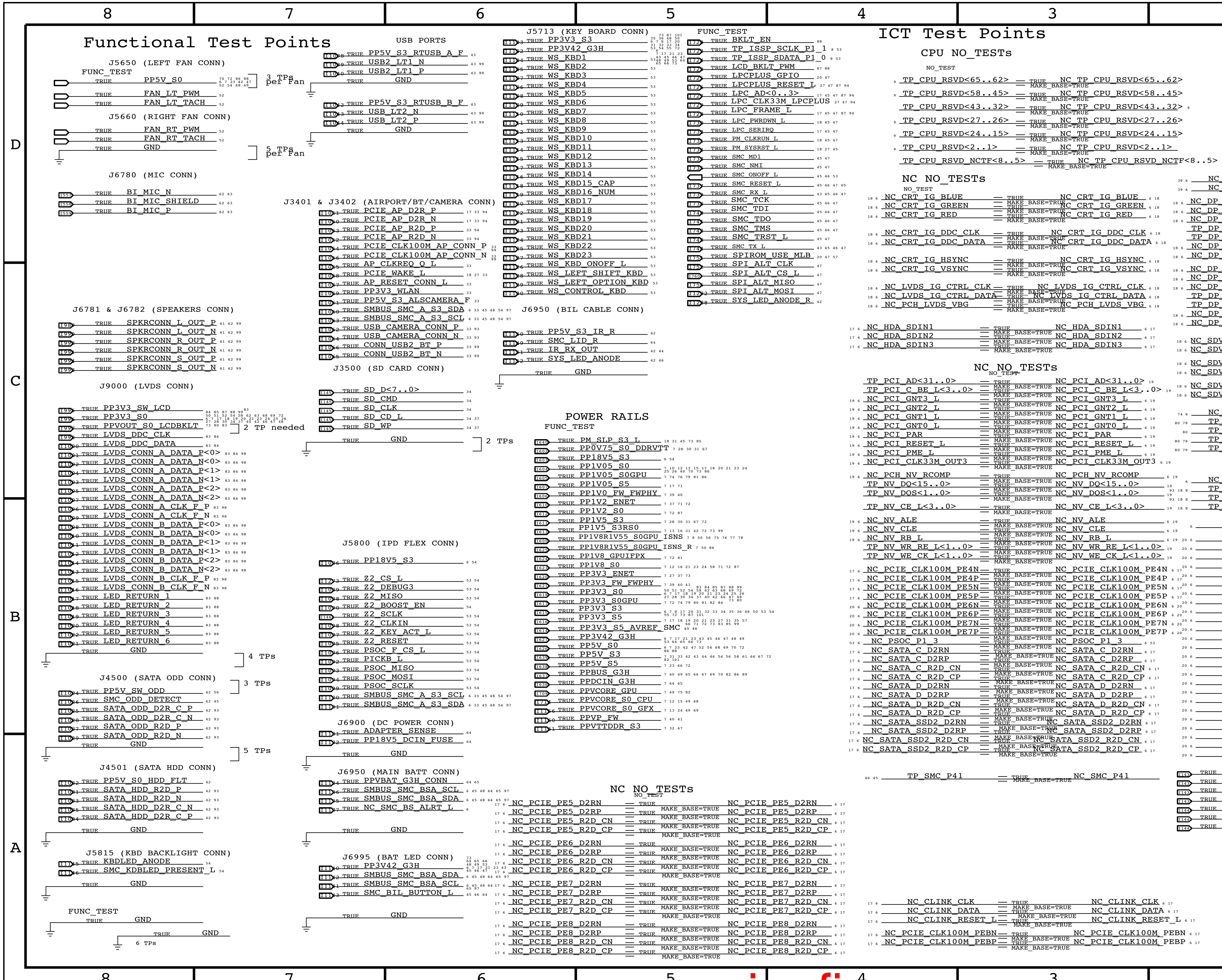

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Functional / ICT Test

Apple Inc.

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPBUS_CPU_IMVP_ISNS

PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H

PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP3V42_G3H (×16)

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S5
PP5V_S5
PP5V_S5

PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S3 (×16)

PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0 (×16)

3.3V Rails

PP3V_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S5 (×24)

PP3V_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3 (×24)

PP3V_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0 (×40)

PP1V8_S0
2A max supply

PP1V8_S0
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S0 (×8)

PP1V5_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V5_S3 (×6)

PP1V5_S3RS0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V5_S3RS0 (×4)

PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP0V75_S0_DDRVTT (×3)

PP1V2_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.09 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S0

PP1V05_S5
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S5

PP1V05_S0
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0 (×24)

ENET Rails

PP3V3_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_ENET

PP1V2_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_ENET (×2)

1.8V/1.5V/1.2V/1.05V Rails

"FW" (FireWire) Rails

PPVP_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPVP_FW (×2)

PP3V3_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_FW_FWPHY (×2)

PP1V0_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V0_FW_FWPHY

"GPU" Rails

PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0GPU (×4)

PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_GPUIFPX

PP1V8R1V55_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.85V
MAKE_BASE=TRUE

PP1V8R1V55_S0GPU_ISNS (×4)

PP1V8R1V55_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.85V
MAKE_BASE=TRUE

PP1V8R1V55_S0GPU_ISNS_R

PP1V05_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0GPU (×12)

PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.6V
MAKE_BASE=TRUE

PPVCORE_GPU

Chipset "VCore" Rails

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU

PPVCORE_S0_GFX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVCORE_S0_GFX

PPVCORE_S0_CPU_VCAP0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP0

PPVCORE_S0_CPU_VCAP1
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP1

PPVCORE_S0_CPU_VCAP2
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE

PPVCORE_S0_CPU_VCAP2

SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM>
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Thermal Module Holes

ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH

Fan Holes

ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND
ZT0940 3R2P5 — GND
ZT0950 TH — GND — SL-3.1X2.7-6CIR-NSP
ZT0960 3R2P5 — GND
ZT0990 3R2P5 — GND

Left Speaker Holes

ZT0934 STDOFF-4.0OD3.0H-TH
ZT0935 STDOFF-4.0OD3.0H-TH

Keyboard / IPD Conn Protect

ZT0952 4.0OD1.85H-M1.6X0.35
ZT0953 4.0OD1.85H-M1.6X0.35

Tall EMI pogo pins

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0904 2.0DIA-TALL-EMI-MLB-M97-M98

Short (IO Row) EMI pogo pins

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0901 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0917 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
GND_CHASSIS_AUDIO_JACK

GMUX ALIASES

PM_ALL_GPU_PGOOD — PM_ALL_GPU_PGOOD
TP_LVDS_MUX_SEL_EG — TP_LVDS_MUX_SEL_EG
EG_RESET_L — EG_RESET_L
LVDS_IG_BKL_ON — LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR — LVDS_IG_PANEL_PWR
LCD_BKLT_EN — LCD_BKLT_EN
PEX_CLKREQ_L — PEX_CLKREQ_L
PEG_CLKREQ_L — PEG_CLKREQ_L
PM_ENET_EN — PM_ENET_EN
FW_PLUG_DET_L — FW_PLUG_DET_L
FW643_WAKE_L — FW643_WAKE_L
TP_SMC_EXCARD_PWR_EN — TP_SMC_EXCARD_PWR_EN
NC_SATA_EXTA_D2R_N — NC_SATA_EXTA_D2R_N
NC_SATA_EXTA_D2R_P — NC_SATA_EXTA_D2R_P
NC_SATA_EXTA_R2D_C_N — NC_SATA_EXTA_R2D_C_N
NC_SATA_EXTA_R2D_C_P — NC_SATA_EXTA_R2D_C_P
NC_PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2R_N
NC_PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2R_P
NC_PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_C_N
NC_PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARD_P
TP_ISSP_SCLK_P1_1 — TP_ISSP_SCLK_P1_1
TP_ISSP_SDATA_P1_0 — TP_ISSP_SDATA_P1_0

GND
GND
GND
GND
GND

CPU signals

CPU_VID<0..6> — CPUIMVP_VID<0..6>
GFX_VID<0..6> — GFXIMVP_VID<0..6>
MEMVTT_EN — MEMVTT_EN
TP_CPU_VTT_SELECT — TP_CPU_VTT_SELECT

GPU signals

PEG_D2R_P<15..0> — =PEG_D2R_P<0..15>
PEG_D2R_N<15..0> — =PEG_D2R_N<0..15>
PEG_R2D_C_P<15..0> — =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<15..0> — =PEG_R2D_C_N<0..15>

** PEG LANES REVERSED. ARD STRAP REQ'D. **

R0902 3.0K 5% 1/16W MF-LF 402
CPU_CFG<3>

DP_IG_ML_P<3..0> — DP_IG_B_ML_P<3..0>
DP_IG_ML_N<3..0> — DP_IG_B_ML_N<3..0>
DP_IG_AUX_CH_P — DP_IG_AUX_CH_P
DP_IG_AUX_CH_N — DP_IG_AUX_CH_N
DP_IG_DDC_CLK — DP_IG_DDC_CLK
DP_IG_DDC_DATA — DP_IG_DDC_DATA
DP_IG_HPD — DP_IG_HPD

TP_LVDS_IG_B_CLKP — TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN — TP_LVDS_IG_B_CLKN
TP_LVDS_IG_BKL_PWM — TP_LVDS_IG_BKL_PWM
NC_GPU_XTALOUT — NC_GPU_XTALOUT (NO_TEST=TRUE)
NC_LVDS_IG_A_DATAP<3> — NC_LVDS_IG_A_DATAP<3>
NC_LVDS_IG_A_DATAN<3> — NC_LVDS_IG_A_DATAN<3>
NC_LVDS_IG_B_DATAP<3> — NC_LVDS_IG_B_DATAP<3>
NC_LVDS_IG_B_DATAN<3> — NC_LVDS_IG_B_DATAN<3>
NC_USB_HUB1_OCS4 — NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS3 — NC_USB_HUB2_OCS3
USB_SDCARD_P — USB_SDCARD_P
USB_SDCARD_N — USB_SDCARD_N

PP3V3_S3
R0903 10K 5% 1/16W MF-LF 402
R0904 10K 5% 1/16W MF-LF 402
USB_EXTC_N
USB_EXTC_P

PP1V8R1V55_S0GPU_ISNS
R0900 10 1% 1/16W MF-LF 402 — GPU_FB_A_VREF_DIV
R0901 10 1% 1/16W MF-LF 402 — GPU_FB_B_VREF_DIV

Digital Ground

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.095 mm
VOLTAGE=0V

SYNC_MASTER=K17_REF SYNC_DATE=06/11/2009

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 9 OF 132
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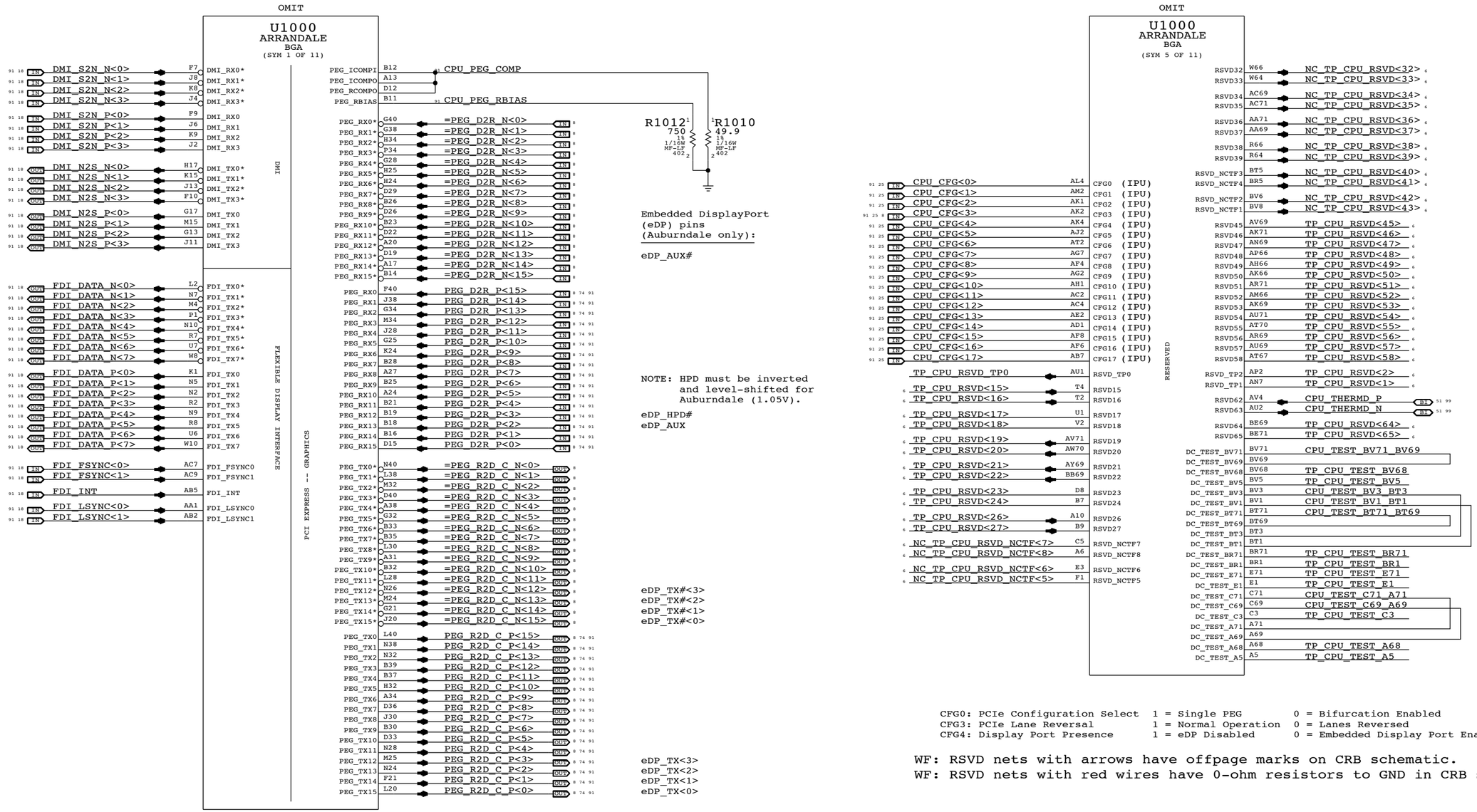

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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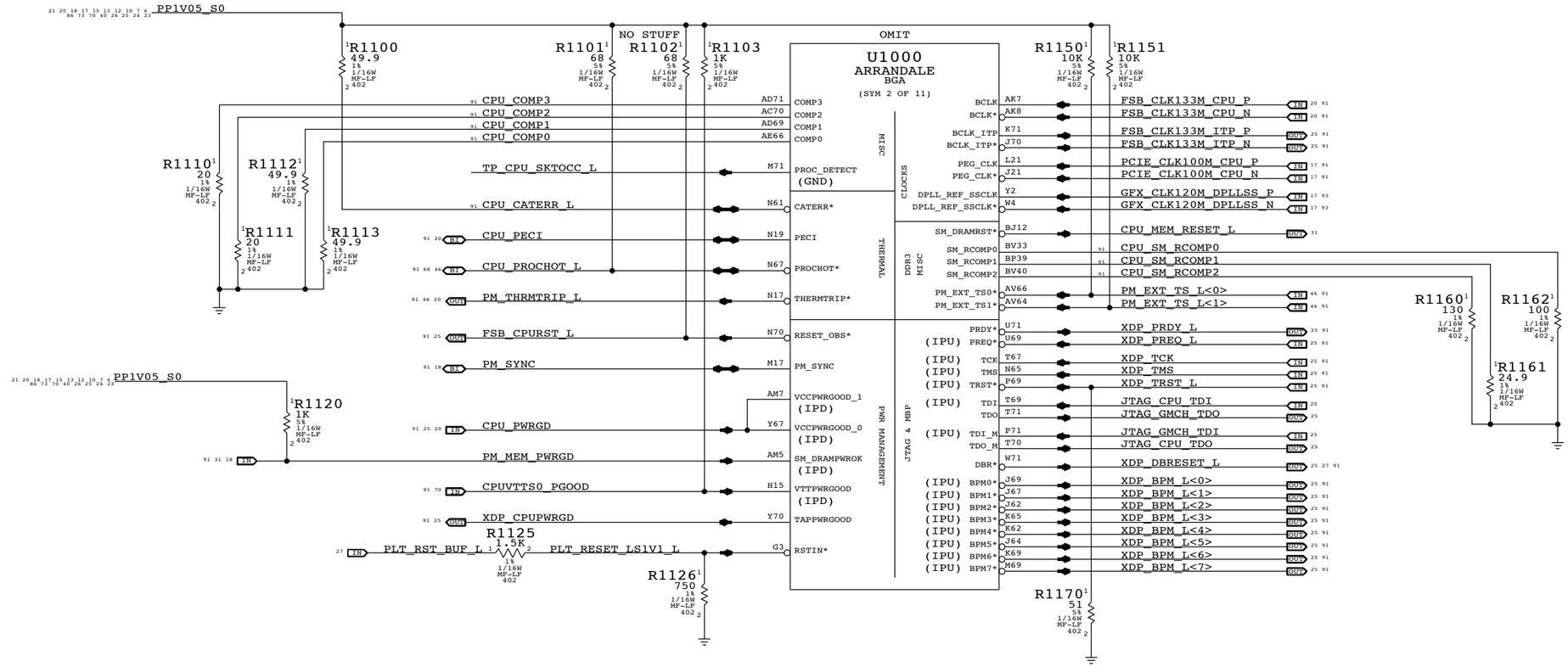

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

CPU Clock/Misc/JTAG

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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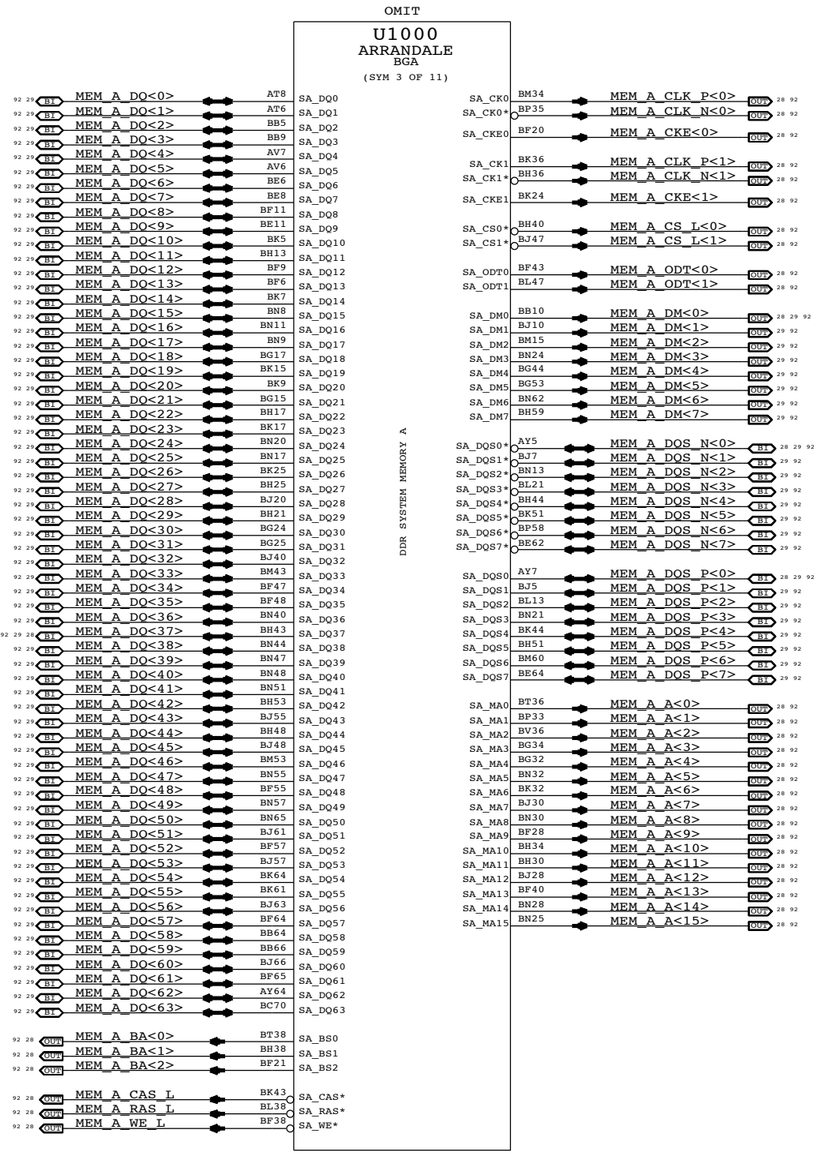

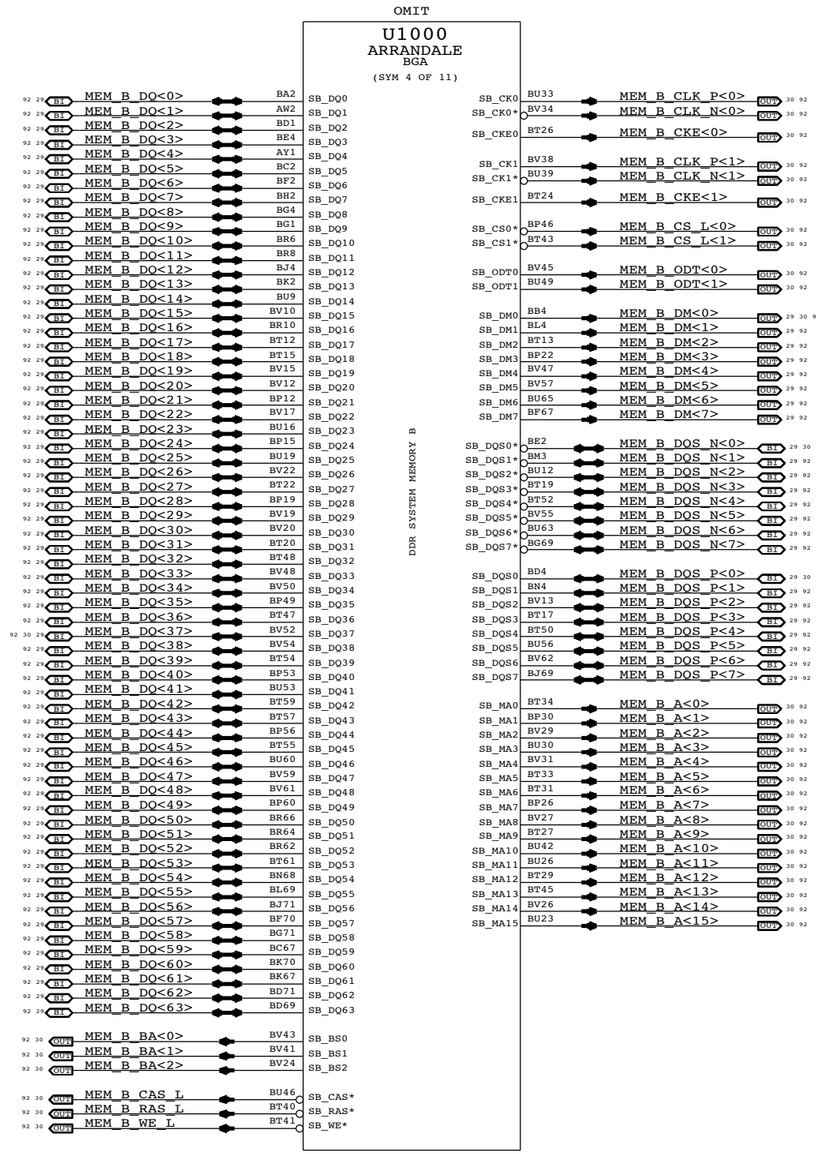

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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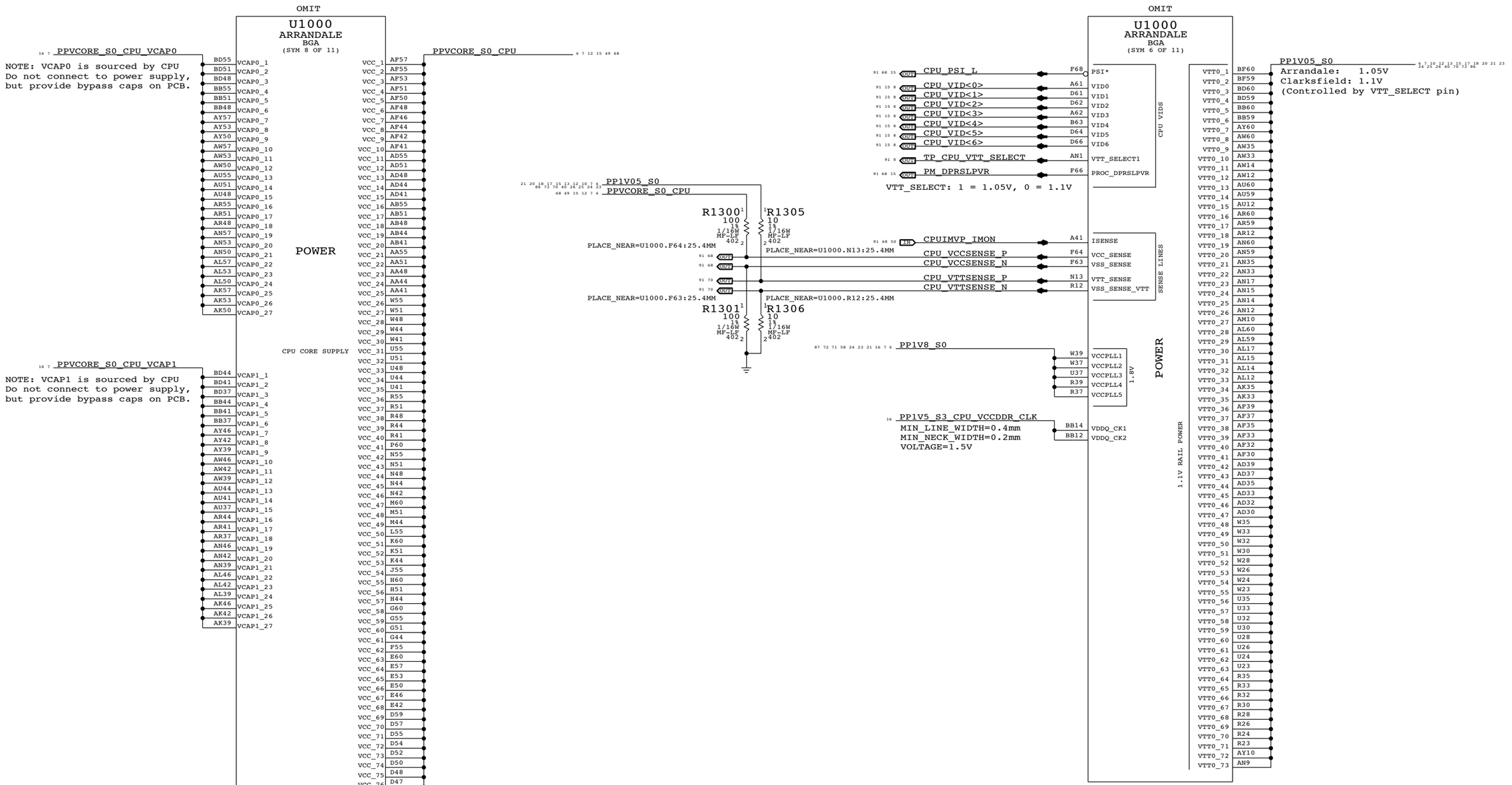

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU Power (1 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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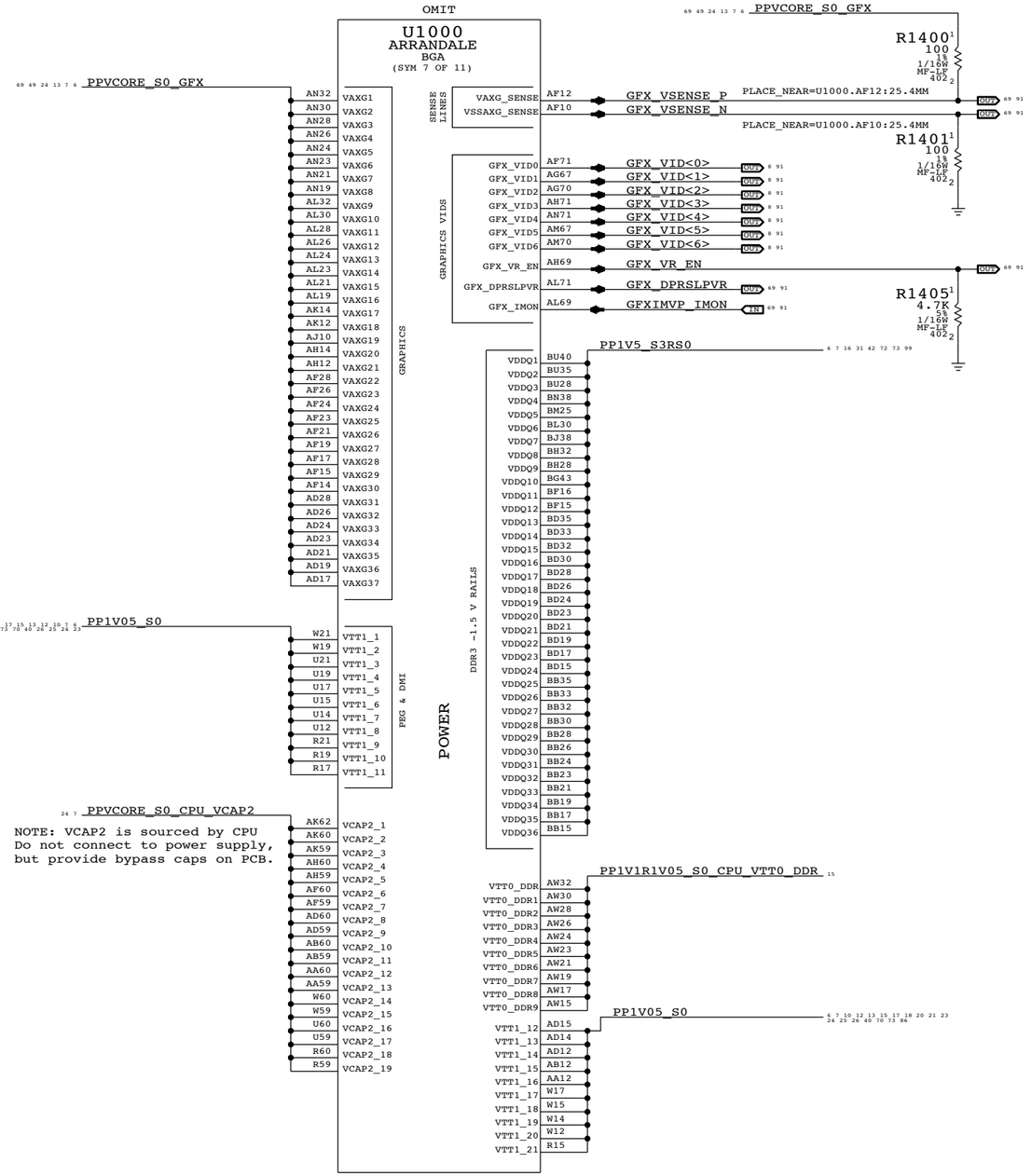

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

CPU Power (2 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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BRANCH <BRANCH>

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OMIT

U1000
ARRANDALE
BGA
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BU62	VSS1	VSS76	AY62
BU58	VSS2	VSS77	AY59
BU55	VSS3	VSS78	AY55
BU51	VSS4	VSS79	AY51
BU48	VSS5	VSS80	AY48
BU44	VSS6	VSS81	AY44
BU37	VSS7	VSS82	AY41
BU32	VSS8	VSS83	AY37
BU25	VSS9	VSS84	AY35
BU21	VSS10	VSS85	AY33
BU18	VSS11	VSS86	AY32
BU14	VSS12	VSS87	AY30
BU11	VSS13	VSS88	AY28
BU7	VSS14	VSS89	AY26
BP42	VSS15	VSS90	AY24
BN64	VSS16	VSS91	AY23
BN6	VSS17	VSS92	AY21
BM70	VSS18	VSS93	AY19
BM51	VSS19	VSS94	AY17
BM44	VSS20	VSS95	AY15
BM32	VSS21	VSS96	AY14
BM24	VSS22	VSS97	AY12
BM17	VSS23	VSS98	AY8
BL57	VSS24	VSS99	AY4
BL55	VSS25	VSS100	AW67
BL48	VSS26	VSS101	AW62
BL40	VSS27	VSS102	AW59
BL28	VSS28	VSS103	AW55
BL20	VSS29	VSS104	AW51
BK63	VSS30	VSS105	AW48
BK60	VSS31	VSS106	AW44
BK53	VSS32	VSS107	AW41
BK34	VSS33	VSS108	AW37
BK10	VSS34	VSS109	AV9
BJ64	VSS35	VSS110	AV1
BJ21	VSS36	VSS111	AU70
BJ9	VSS37	VSS112	AU62
BJ1	VSS38	VSS113	AU57
BH70	VSS39	VSS114	AU53
BH57	VSS40	VSS115	AU50
BH55	VSS41	VSS116	AU46
BH47	VSS42	VSS117	AU42
BH24	VSS43	VSS118	AU39
BH20	VSS44	VSS119	AU35
BH15	VSS45	VSS120	AU33
BG51	VSS46	VSS121	AU32
BG36	VSS47	VSS122	AU30
BF62	VSS48	VSS123	AU28
BF30	VSS49	VSS124	AU26
BF13	VSS50	VSS125	AU24
BF8	VSS51	VSS126	AU23
BE70	VSS52	VSS127	AU21
BE65	VSS53	VSS128	AU19
BE9	VSS54	VSS129	AU17
BE1	VSS55	VSS130	AU15
BD57	VSS56	VSS131	AU14
BD53	VSS57	VSS132	AU4
BD50	VSS58	VSS133	AT64
BD46	VSS59	VSS134	AT10
BD42	VSS60	VSS135	AR62
BD39	VSS61	VSS136	AR57
BD14	VSS62	VSS137	AR53
BB71	VSS63	VSS138	AR50
BB62	VSS64	VSS139	AR46
BB57	VSS65	VSS140	AR42
BB53	VSS66	VSS141	AR39
BB50	VSS67	VSS142	AR35
BB46	VSS68	VSS143	AR33
BB42	VSS69	VSS144	AR32
BB39	VSS70	VSS145	AR30
BB7	VSS71	VSS146	AR28
BB1	VSS72	VSS147	AR26
BA70	VSS73	VSS148	AR24
AY71	VSS74	VSS149	AR23
AY66	VSS75	VSS150	AR21

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U1000
ARRANDALE
BGA
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AR19	VSS151	VSS226	BN71
AR17	VSS152	VSS227	E68
AR15	VSS153	VSS228	AH28
AR14	VSS154	VSS229	AH41
AR4	VSS155	VSS230	A66
AR1	VSS156	VSS231	AH26
AP70	VSS157	VSS232	BN1
AP64	VSS158	VSS233	A64
AN62	VSS159	VSS234	AH24
AN55	VSS160	VSS235	AH39
AN51	VSS161	VSS236	E5
AN48	VSS162	VSS237	AH23
AN44	VSS163	VSS238	C68
AN41	VSS164	VSS239	AH21
AN37	VSS165	VSS240	AH19
AN5	VSS166	VSS241	AH17
AN4	VSS167	VSS242	AH15
AM64	VSS168	VSS243	AH4
AM8	VSS169	VSS244	AG64
AL62	VSS170	VSS245	AG9
AL55	VSS171	VSS246	AG6
AL51	VSS172	VSS247	AF69
AL48	VSS173	VSS248	AF62
AL44	VSS174	VSS249	AF1
AL41	VSS175	VSS250	AE70
AL37	VSS176	VSS251	AE64
AL35	VSS177	VSS252	AD62
AL33	VSS178	VSS253	AD57
AL1	VSS179	VSS254	AD53
AK70	VSS180	VSS255	AD50
AK64	VSS181	VSS256	AD46
AK55	VSS182	VSS257	AD42
AK51	VSS183	VSS258	AD4
AK48	VSS184	VSS259	AC67
AK44	VSS185	VSS260	AC64
AK41	VSS186	VSS261	AC10
AK37	VSS187	VSS262	AC5
AK32	VSS188	VSS263	AC1
AK30	VSS189	VSS264	AB70
AK28	VSS190	VSS265	AB62
AK26	VSS191	VSS266	AB57
AK24	VSS192	VSS267	AB53
AK23	VSS193	VSS268	AB50
AK21	VSS194	VSS269	AB46
AK19	VSS195	VSS270	AB42
AK17	VSS196	VSS271	AB39
AK15	VSS197	VSS272	AB37
AJ70	VSS198	VSS273	AB35
AH62	VSS199	VSS274	AB33
AH57	VSS200	VSS275	AB32
AH55	VSS201	VSS276	AB30
AH53	VSS202	VSS277	AB28
BV66	VSS203	VSS278	AB26
AH51	VSS204	VSS279	AB24
BV64	VSS205	VSS280	AB23
AH50	VSS206	VSS281	AB21
BT68	VSS207	VSS282	AB19
AH48	VSS208	VSS283	AB17
BR69	VSS209	VSS284	AB15
BL71	VSS210	VSS285	AB14
AH46	VSS211	VSS286	AB9
BL1	VSS212	VSS287	AA66
AH37	VSS213	VSS288	AA64
BR68	VSS214	VSS289	AA62
R14	VSS215	VSS290	AA57
AH35	VSS216	VSS291	AA53
AH44	VSS217	VSS292	AA50
H71	VSS218	VSS293	AA46
AH33	VSS219	VSS294	AA42
BR3	VSS220	VSS295	AA39
F71	VSS221	VSS296	AA37
AH32	VSS222	VSS297	AA35
AH42	VSS223	VSS298	AA33
E69	VSS224	VSS299	AA32
AH30	VSS225	VSS300	AA30

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U1000
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AA28	VSS301	VSS367	K6
AA26	VSS302	VSS368	K4
AA24	VSS303	VSS369	J65
AA23	VSS304	VSS370	J57
AA21	VSS305	VSS371	J48
AA19	VSS306	VSS372	J47
AA17	VSS307	VSS373	J40
AA15	VSS308	VSS374	J9
AA14	VSS309	VSS375	H53
AA4	VSS310	VSS376	H43
W69	VSS311	VSS377	H36
W62	VSS312	VSS378	H1
W57	VSS313	VSS379	G70
W53	VSS314	VSS380	G57
W50	VSS315	VSS381	G53
W46	VSS316	VSS382	G48
W42	VSS317	VSS383	G47
W6	VSS318	VSS384	G43
W1	VSS319	VSS385	G30
V70	VSS320	VSS386	G24
U64	VSS321	VSS387	G20
U62	VSS322	VSS388	G15
U57	VSS323	VSS389	F61
U53	VSS324	VSS390	F48
U50	VSS325	VSS391	F47
U46	VSS326	VSS392	F28
U42	VSS327	VSS393	F20
U39	VSS328	VSS394	F4
U9	VSS329	VSS395	E37
U4	VSS330	VSS396	E33
T1	VSS331	VSS397	E30
R70	VSS332	VSS398	E16
R62	VSS333	VSS399	E12
R57	VSS334	VSS400	D41
R53	VSS335	VSS401	D38
R50	VSS336	VSS402	D34
R46	VSS337	VSS403	D31
R42	VSS338	VSS404	D27
R5	VSS339	VSS405	D24
P4	VSS340	VSS406	D20
N63	VSS341	VSS407	D17
N57	VSS342	VSS408	D13
N53	VSS343	VSS409	D10
N50	VSS344	VSS410	D6
N46	VSS345	VSS411	B65
N30	VSS346	VSS412	B62
N21	VSS347	VSS413	B58
N15	VSS348	VSS414	B55
M53	VSS349	VSS415	B51
M42	VSS350	VSS416	B48
M36	VSS351	VSS417	B44
M1	VSS352	VSS418	A59
L70	VSS353	VSS419	A55
L57	VSS354	VSS420	A52
L48	VSS355	VSS421	A48
L47	VSS356	VSS422	A45
L13	VSS357	VSS423	A40
K64	VSS358	VSS424	A36
K53	VSS359	VSS425	A33
K43	VSS360	VSS426	A29
K36	VSS361	VSS427	A26
K34	VSS362	VSS428	A22
K32	VSS363	VSS429	A19
K25	VSS364	VSS430	A15
K17	VSS365	VSS431	A12
K11	VSS366	VSS432	A8
		VSS433	B40

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

CPU Grounds

Apple Inc.

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CPU VCore HF and Bulk Decoupling

4x 470uF 4.5mOhm, 3x 62uF B2, 10x 22uF 0603, 25x 1uF 0402

PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C1624):

Place on bottom side of U1000..

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612
C1613 C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1625-C1634):

Place near U1000 on bottom side.

NO STUFF C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1634 C1691 C1692 C1693 C1694 C1698
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1635-C1648):

Place near inductors on bottom side.

NO STUFF C1635 C1636 C1637 C1638 C1640 C1641 C1642 C1643 C1644 C1645 C1646 C1648
22UF 20% 6.3V X5R-CERM 603

C1649 C1650 C1651 C1652
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

NO STUFF C16A0 C16A1 C16A2 C16A3 C16A4
62UF 20% 11V ELEC CASE-B2

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

PP1V05_S0

R1600 R1602 CPUPOC4U R1604 NO STUFF R1606 NO STUFF R1608
R1601 CPUPOC3U R1603 CPUPOC5U R1605 R1607
1K 5% 1/16W MF-LF 402

CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
PM_DPRSLPVR
CPU_PSI_L

NO STUFF R1610 CPUPOC4D R1614 R1616 R1618
NO STUFF R1611 CPUPOC3D R1613 CPUPOC5D R1615 NO STUFF R1617

VID[2:0] = Reserved (111)
VID[5:3] = GPU Gain Setting (See below)
VID[6] = Reserved (0)
DPRSLPVR = 1 - IMVP-6.5 compliant controller
PSI# = Reserved (0)

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_20	20A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_20_30	30A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_30_40	40A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_40_50	50A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_50_60	60A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_60_70	70A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_70_90	90A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly. Instead call out appropriate BOM GROUP defined in tables above.

VTT (CPU Uncore) DECOUPLING

3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

PP1V05_S0

PLACEMENT_NOTE (C1653-C1656):

Place on bottom side of U1000.

C1653 C1654 C1655 C1656
22UF 20% 6.3V X5R-CERM 603

PLACEMENT_NOTE (C1657-C1663):

Place on bottom side of U1000..

C1657 C1658 C1659 C1660 C1661 C1662 C1663
10UF 20% 6.3V X5R 603

PLACEMENT_NOTE (C1664-C1687):

Place on bottom side of U1000.

C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675
C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686 C1687
1UF 10% 10V X5R 402

C1688 C1689 C1690
330UF 20% 2.0V POLY-TANT D2T-SM2

VTT0_DDR DECOUPLING

3x 1uF 0402

L1695 30-OHM-5A 0603

PLACEMENT_NOTE (C1695-C1697):

Place on bottom side of U1000.

C1695 C1696 C1697
1UF 10% 10V X5R 402

PP1V1R1V05_S0_CPU_VTT0_DDR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form Factor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU Non-GFX Decoupling (1 of 2)

Apple Inc.

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VCAP0 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1700-C1711):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP0

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 C1709 C1710 C1711
1UF 10% 10V X5R 402

VCAP1 (CPU BSC Package) DECOUPLING

12x 1uF 0402

PLACEMENT_NOTE (C1712-C1723):

Place on bottom side of U1000.

12 7 PPVCORE_S0_CPU_VCAP1

C1712 C1713 C1714 C1715 C1716 C1717 C1718 C1719 C1720 C1721 C1722 C1723
1UF 10% 10V X5R 402

Memory (CPU VCCDDR) DECOUPLING

5x 1uF 0402

NOTE: 3x 330uF 6 mOhm caps to be shared between CPU and SO-DIMMs. DG recommends 2x 22uF at SO_DIMM not provided. Decoupling caps at SO-DIMMs on CSA 29 and CSA 31.

42 31 16 9 7 3 2 PP1V5_S3RS0

C1724 C1725 C1726 C1727 C1728
1UF 10% 10V X5R 402

NOTE: 19x 1uF 0402 caps per Apple SI for CMD and CNTRL lines.

C1735 C1736 C1737 C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747 C1748 C1749 C1750 C1751 C1752 C1753
1UF 10% 10V X5R 402

C1729
330UF 20% 2.0V POLY-TANT D2T-SM2

PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603

24 23 21 12 7 6 PP1V8_S0

C1732 22uF 20% 6.3V CERM-X5R 805
C1733 4.7UF 10% 6.3V X5R-CERM 603

DDR Clock (CPU VDDQ_CK) DECOUPLING

1x 1uF 0402

42 31 16 9 7 3 2 PP1V5_S3RS0

L1734 30-OHM-5A 0603

PP1V5_S3_CPU_VCCDDR_CLK 12

C1734 1UF 10% 10V X5R 402

Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form Factor Schematic Check List Rev 1.1 (doc #395914) table 3.26.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU Non-GFX Decoupling (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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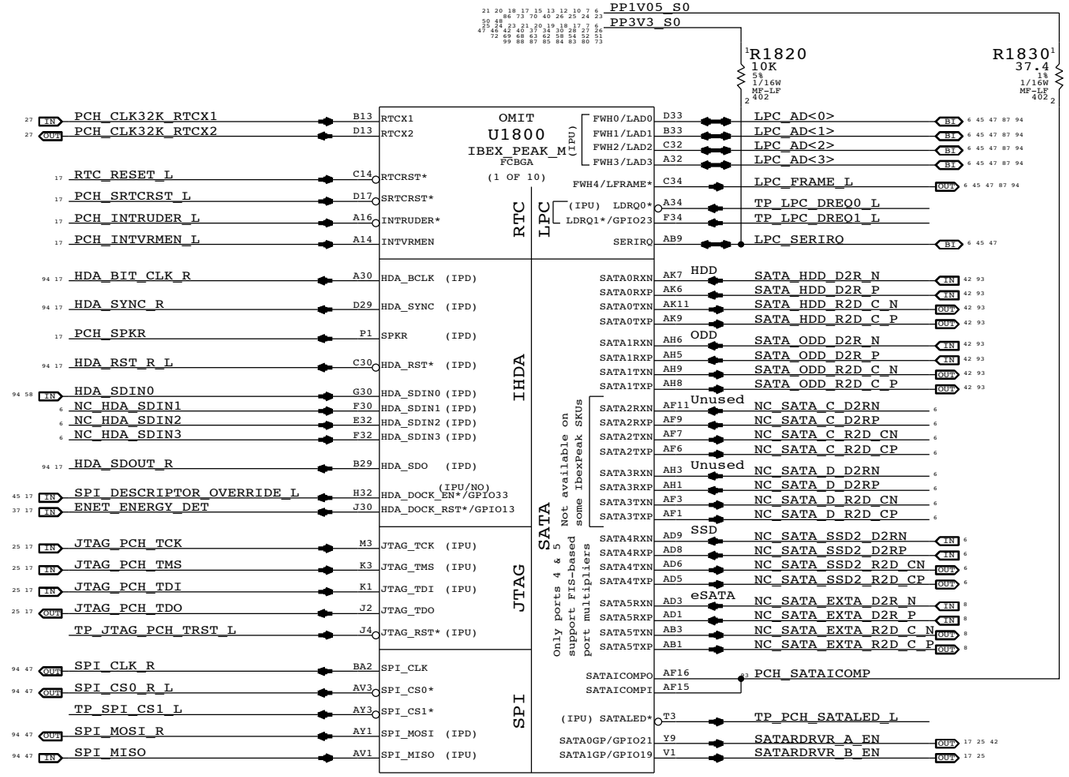

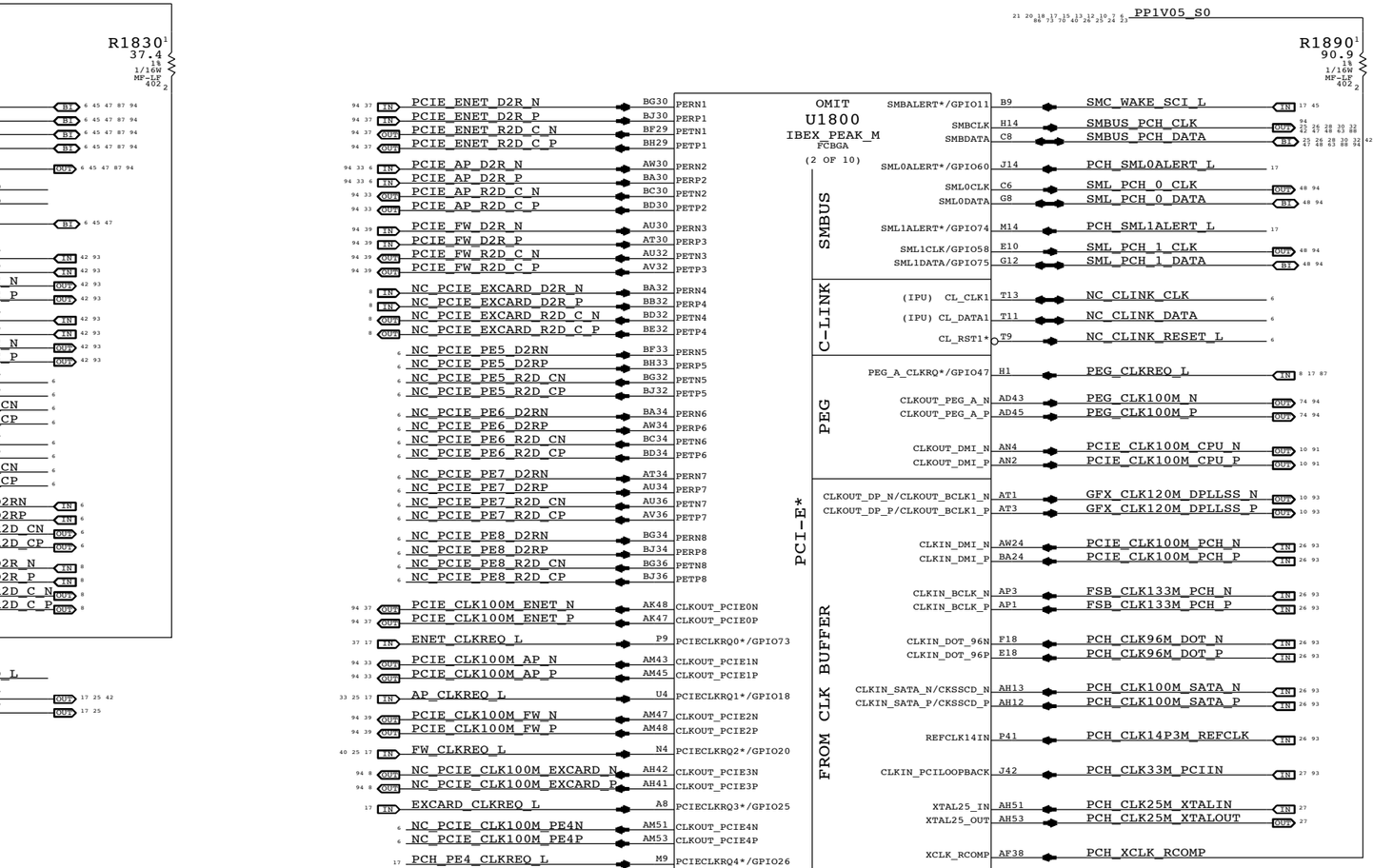

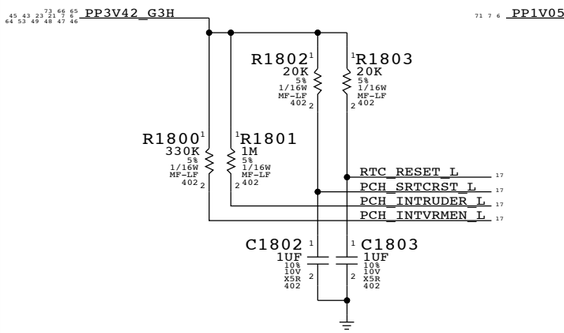

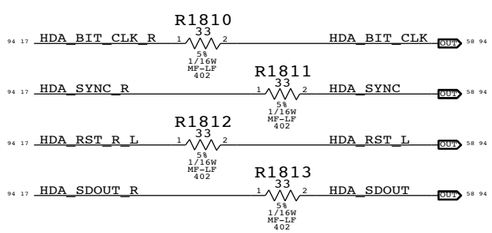

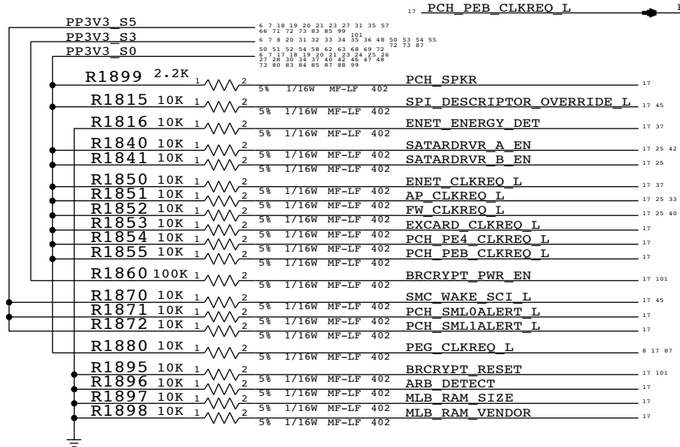

SYNC_MASTER=K17_REF SYNC_DATE=08/24/2009

PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

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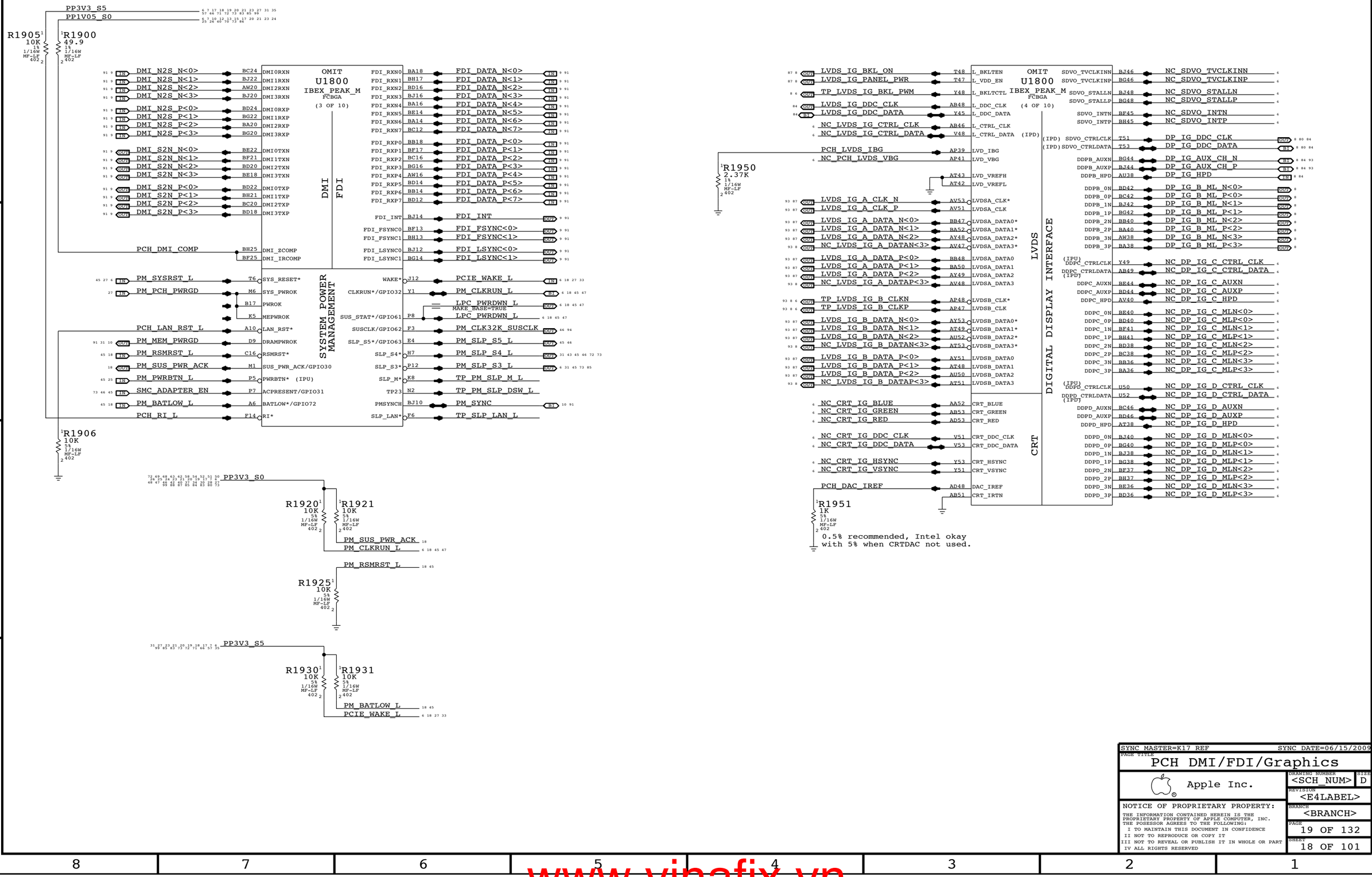

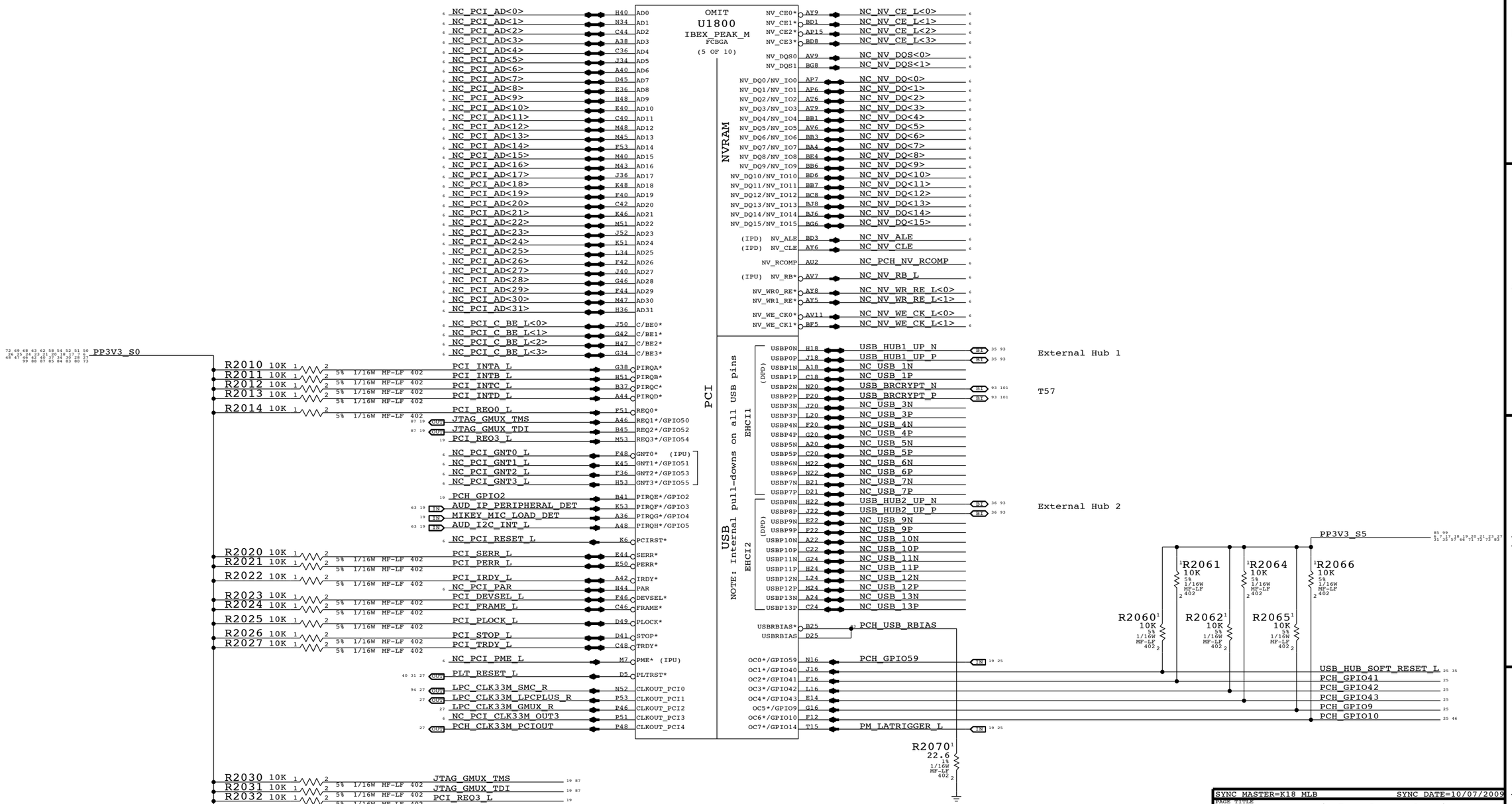

SYNC MASTER=K18 MLB SYNC DATE=10/07/2009

PAGE TITLE
PCH PCI/FlashCache/USB

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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IPU* = Only on TACH function.

U1800 IBEX_PEAK_M
FCBGA
(6 OF 10)

GPIO
SMC_IG_THROTTLE_L	Y3	BMBUSY*/GPIO0	
FW_PLUG_DET_L	C38	TACH1/GPIO1 (IPU*)	
GMUX_INT	D37	TACH2/GPIO6 (IPU*)	
SMC_RUNTIME_SCI_L	J32	TACH3/GPIO7 (IPU*)	
PCH_FCIM_EN_L	F10	GPIO8 (IPU)	
ENET_LOW_PWR	K9	LAN_PHY_PWR_CTRL/GPIO12	
PCH_GPIO15	T7	GPIO15 (IPD)	
AUD_IPHS_SWITCH_EN	AA2	SATA4GP/GPIO16	
LPCPLUS_GPIO	F38	TACH0/GPIO17 (IPU*)	
ODD_PWR_EN_L	Y7	SCLOCK/GPIO22	
PCH_GPIO24	H10	MEM_LED/GPIO24	
PCH_VRM_EN	AB12	GPIO27	
ISOLATE_CPU_MEM_L	V13	GPIO28 (IPU)	
TP_PCH_STP_PCI_L	M11	STP_PCI*/GPIO34	
MXM_GOOD	V6	SATACLKREQ*/GPIO35	
SDCARD_RESET	AB7	SATA2GP/GPIO36	
JTAG_GMUX_TCK	AB13	SATA3GP/GPIO37	
JTAG_GMUX_TDO	V3	SLOAD/GPIO38	
PCH_GPIO39	P3	SDATAOUT0/GPIO39	
WOL_EN	H3	PCIECLKRQ6*/GPIO45	
AP_PWR_EN	F1	PCIECLKRQ7*/GPIO46	
FW_PWR_EN	AB6	SDATAOUT1/GPIO48	
ME_TEMP_ALERT_L	AA4	SATA5GP/GPIO49	
SPIROM_USE_MLB	F8	GPIO57	

NCTF
PCH_VSS_NCTF<1>	A4	VSS_NCTF1
PCH_VSS_NCTF<2>	A49	VSS_NCTF2
	A5	VSS_NCTF3
	A50	VSS_NCTF4
PCH_VSS_NCTF<5>	A52	VSS_NCTF5
	A53	VSS_NCTF6
TP_PCH_VSS_NCTF<7>	B2	VSS_NCTF7
	B4	VSS_NCTF8
PCH_VSS_NCTF<9>	B52	VSS_NCTF9
	B53	VSS_NCTF10
PCH_VSS_NCTF<11>	BE1	VSS_NCTF11
PCH_VSS_NCTF<12>	BE53	VSS_NCTF12
	BF1	VSS_NCTF13
	BF53	VSS_NCTF14
PCH_VSS_NCTF<15>	BH1	VSS_NCTF15
	BH2	VSS_NCTF16
PCH_VSS_NCTF<17>	BH52	VSS_NCTF17
	BH53	VSS_NCTF18
PCH_VSS_NCTF<19>	BJ1	VSS_NCTF19
	BJ2	VSS_NCTF20
PCH_VSS_NCTF<21>	BJ4	VSS_NCTF21
PCH_VSS_NCTF<22>	BJ49	VSS_NCTF22
	BJ5	VSS_NCTF23
	BJ50	VSS_NCTF24
PCH_VSS_NCTF<25>	BJ52	VSS_NCTF25
	BJ53	VSS_NCTF26
PCH_VSS_NCTF<27>	D1	VSS_NCTF27
	D2	VSS_NCTF28
PCH_VSS_NCTF<29>	D53	VSS_NCTF29
	E1	VSS_NCTF30
	E53	VSS_NCTF31

CPU
CLKOUT_PCIE6N	AH45	NC_PCIE_CLK100M_PE6N	
CLKOUT_PCIE6P	AH46	NC_PCIE_CLK100M_PE6P	
CLKOUT_PCIE7N	AF48	NC_PCIE_CLK100M_PE7N	
CLKOUT_PCIE7P	AF47	NC_PCIE_CLK100M_PE7P	
A20GATE	U2	PCH_A20GATE	
CLKOUT_BCLK0_N/CLKOUT_PCIE8N	AM3	FSB_CLK133M_CPU_N	OUT 10 91
CLKOUT_BCLK0_P/CLKOUT_PCIE8P	AM1	FSB_CLK133M_CPU_P	OUT 10 91
PECI	BG10	CPU_PECI	BI 10 91
RCIN*	T1	PCH_RCIN_L	
PROCPWRGD	BE10	CPU_PWRGD	OUT 10 25 91
THRMTRIP*	BD10	PCH_THRMTRIP_L	

MISC
TP1	BA22	NC_PCH_TP1
TP2	AW22	NC_PCH_TP2
TP3	BB22	NC_PCH_TP3
TP4	AY45	NC_PCH_TP4 (DPL_B_MON1_N)
TP5	AY46	NC_PCH_TP5 (DPL_B_MON1_P)
TP6	AV43	NC_PCH_TP6 (DPL_B_MON2_N)
TP7	AV45	NC_PCH_TP7 (DPL_B_MON2_P)
TP8	AF13	NC_PCH_TP8 (SATA_OB_ANA)
TP9	M18	NC_PCH_TP9
TP10	N18	NC_PCH_TP10
TP11	AJ24	NC_PCH_TP11
TP12	AK41	NC_PCH_TP12 (XCKPLL_MON1_N)
TP13	AK42	NC_PCH_TP13 (XCKPLL_MON1_P)
TP14	M32	NC_PCH_TP14
TP15	N32	NC_PCH_TP15
TP16	M30	NC_PCH_TP16
TP17	N30	NC_PCH_TP17
TP18	H12	NC_PCH_TP18
TP19	AA23	NC_PCH_TP19
NC_1	AB45	NC_PCH_NC1
NC_2	AB38	NC_PCH_NC2
NC_3	AB42	NC_PCH_NC3
NC_4	AB41	NC_PCH_NC4
NC_5	T39	NC_PCH_NC5
(IPD) INIT3_3V*	P6	TP_PCH_INIT3V3_L
TP24	C10	NC_PCH_SST

RSVD
OMIT

OMIT
PP3V3_S0

R2150 10K 5% 1/16W MF-LF 402 — PP3V3_S0
R2155 10K 5% 1/16W MF-LF 402 — PP3V3_S0
R2160 56 5% 1/16W MF-LF 402 — PP1V05_S0
R2161 56 5% 1/16W MF-LF 402 — PM_THRMTRIP_L (IN 10 46 91)

PP3V3_S5
PP3V3_S3
PP3V3_S0

R2110	10K	SMC_IG_THROTTLE_L	20 25 45 46
R2111	10K	FW_PLUG_DET_L	8 20 40
R2112	20K	GMUX_INT	20 87
R2113	10K	SMC_RUNTIME_SCI_L	20 45
R2114	10K	PCH_FCIM_EN_L	20
R2115	2.2K	ENET_LOW_PWR	20 37
R2116	10K	PCH_GPIO15	20
R2120	10K	AUD_IPHS_SWITCH_EN	20 25 63
R2121	10K	LPCPLUS_GPIO	6 20 47
R2122	10K	ODD_PWR_EN_L	20 42
R2123	10K	PCH_GPIO24	20
R2124	10K	PCH_VRM_EN	20
R2130	10K	MXM_GOOD	20
R2131	10K	SDCARD_RESET	20 25 34
R2132	10K	JTAG_GMUX_TCK	20 25 87
R2133	10K	JTAG_GMUX_TDO	20 87
R2134	10K	PCH_GPIO39	20
R2135	10K	WOL_EN	20 73
R2136	10K	AP_PWR_EN	20 33 73
R2137	10K	FW_PWR_EN	20 40
R2138	10K	ME_TEMP_ALERT_L	20 25
R2139	100K	SPIROM_USE_MLB	6 20 47 57

All: 5% 1/16W MF-LF 402

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: PCH MISC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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BRANCH: <BRANCH>
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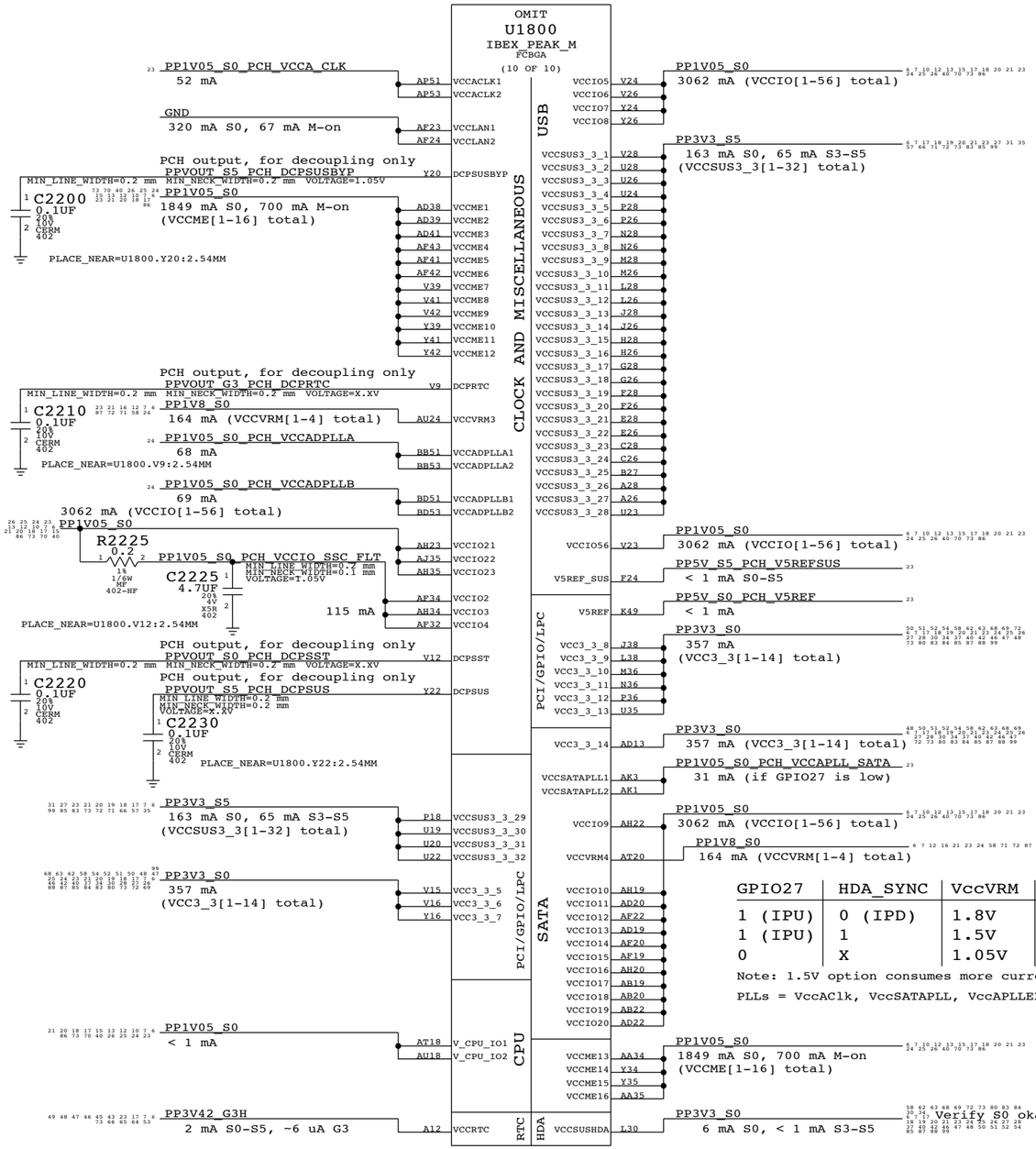

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: PCH Power

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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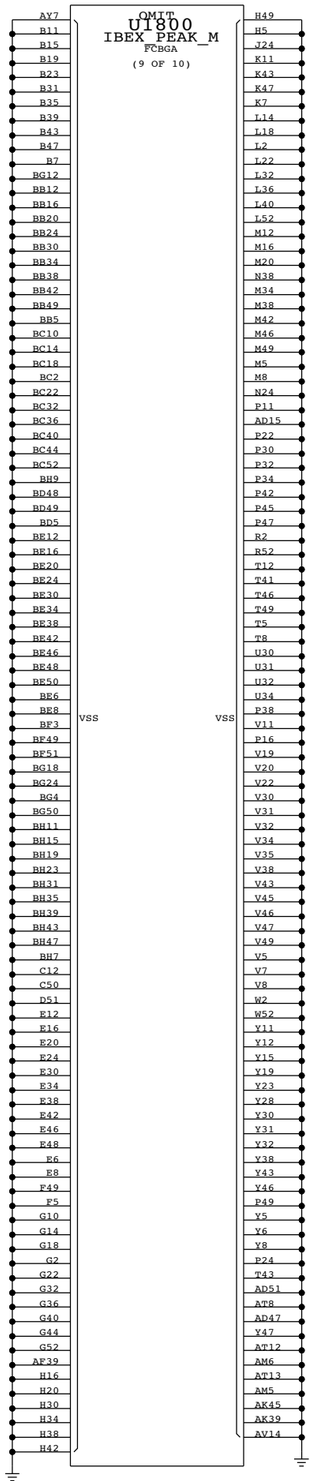

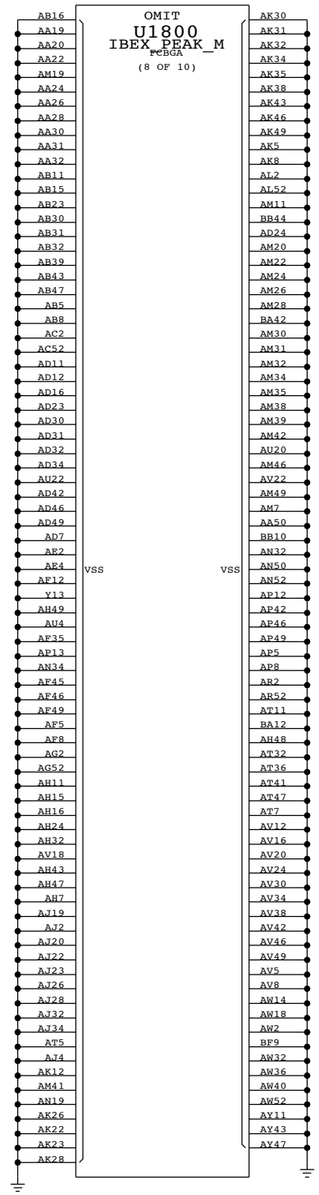

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)

PP3V3_S5
PP5V_S5
1 mA S0-S5
R2400 10 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PP5V_S5_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
1 mA S0-S5
C2400 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.P24:2.54MM

PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)

PP3V3_S0
PP5V_S0
1 mA
R2401 100 5% 1/16W MF-LF 402
D2400 BAT54DW-X-G SOT-363
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
1 mA
C2401 1UF 10% 10V X5R 402
PLACE_NEAR=U1800.K49:2.54MM

PCH VCCRTC BYPASS
(PCH RTC 3.3V PWR)

PP3V42_G3H
2 mA S0-S5 /
6 uA G3
C2420 1UF 10% 6.3V CERM 402
C2421 0.1UF 10% 16V X5R 402
C2422 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.A12:2.54MM
PLACE_NEAR=U1800.A12:2.54MM
PLACE_NEAR=U1800.A12:2.54MM

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND PCI 3.3V PWR)

PP3V3_S5
C2425 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.P18:2.54MM

(VCCSUS3_3_Total)

PCH USB/VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)

163 mA S0 /
65 mA S3-S5
PP3V3_S5
C2426 0.1UF 10% 16V X5R 402
C2427 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.A26:2.54MM
PLACE_NEAR=U1800.U23:2.54MM

PCH VCCME3_3 BYPASS
(PCH ME 3.3V PWR)

PP3V3_S0
C2430 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AM8:2.54MM

PCH CORE/VCC3_3 BYPASS
(PCH MISC 3.3V PWR)

PP3V3_S0
C2435 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.V15:2.54MM

PCH VCCAPLLEXP Filter
(PCH PCIe PLL PWR)

PP1V05_S0_PCH_VCCAPLL_EXP
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
OMIT WF: C2311 not in DG or CRB
C2413 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.BJ24:2.54MM

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)

PP3V3_S0
C2436 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.J38:2.54MM

PCH VCCFDIPLL Filter
(PCH FDI PLL PWR)

PP1V05_S0_PCH_VCCAPLL_FDI
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
OMIT WF: C2413 not in DG or CRB
C2415 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.BJ18:2.54MM

PCH VCC3_3 BYPASS
(PCH SATA 3.3V PWR)

PP3V3_S0
C2437 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AD13:2.54MM

PCH VCCSATAPLL Filter
(PCH SATA PLL PWR)

PP1V05_S0_PCH_VCCAPLL_SATA
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
BB: C2417 removed from DG
NO STUFF
C2417 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AK1:2.54MM

PCH VCC3_3 BYPASS
(PCH PCIe/DMI 3.3V PWR)

PP3V3_S0
C2438 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AN35:2.54MM

PCH VCCACLK Filter
(PCH Misc PLL PWR)

PP1V05_S0_PCH_VCCA_CLK
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.05V
BB: C2419 removed from DG
NO STUFF
C2419 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AP51:2.54MM

PCH VCC3_3 BYPASS
(PCH CLK/HVCMOS 3.3V PWR)

PP3V3_S0
C2439 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AB34:2.54MM

PCH VCCPNAND BYPASS
(PCH NAND 1.8V/3.3V PWR)

PP1V8_S0
C2440 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AK13:2.54MM

PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)

PP3V3_S0
C2445 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.L30:2.54MM

PCH V_CPU_IO BYPASS
(PCH 1.1V/1.05V CPU I/O PWR)

PP1V05_S0
C2450 4.7UF 20% 6.3V X5R 603
C2451 0.1UF 10% 16V X5R 402
C2452 0.1UF 10% 16V X5R 402
PLACE_NEAR=U1800.AT18:2.54MM
PLACE_NEAR=U1800.AT18:2.54MM
PLACE_NEAR=U1800.AT18:2.54MM

PCH VCCIO BYPASS
(PCH DMI 1.05V PWR)

PP1V05_S0
C2455 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AT16:2.54MM

PCH VCCLAN BYPASS
(PCH 1.05V LAN Core PWR)

GND
NO STUFF
C2460 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF23:2.54MM

PCH VCCME BYPASS
(PCH 1.05V ME Core PWR)

PP1V05_S0
C2465 22UF 20% 6.3V X5R-CERM 603
C2466 22UF 20% 6.3V X5R-CERM 603
C2467 22UF 20% 6.3V X5R-CERM 603
C2468 1UF 10% 6.3V CERM 402
C2469 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.V39:2.54MM
PLACE_NEAR=U1800.AD38:2.54MM
PLACE_NEAR=U1800.V39:2.54MM

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)

PP1V05_S0
C2470 10UF 20% 6.3V X5R 603
C2471 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AB24:2.54MM
PLACE_NEAR=U1800.AB24:2.54MM

PCH VCCIO BYPASS
(PCH CLK 1.05V PWR)

PP1V05_S0
C2475 1UF 10% 6.3V CERM 402
C2476 1UF 10% 6.3V CERM 402
C2477 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AF32:2.54MM
PLACE_NEAR=U1800.AH23:2.54MM
PLACE_NEAR=U1800.AH35:2.54MM

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)

PP1V05_S0
C2480 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.V24:2.54MM

PCH VCCIO BYPASS
(PCH SATA 1.05V PWR)

PP1V05_S0
C2485 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AB19:2.54MM

PCH VCCIO BYPASS
(PCH PCIE 1.05V PWR)

PP1V05_S0
C2490 10UF 20% 6.3V X5R 603
C2491 1UF 10% 6.3V CERM 402
C2492 1UF 10% 6.3V CERM 402
C2493 1UF 10% 6.3V CERM 402
C2494 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM
PLACE_NEAR=U1800.AN20:2.54MM

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
PCH Non-GFX Decoupling

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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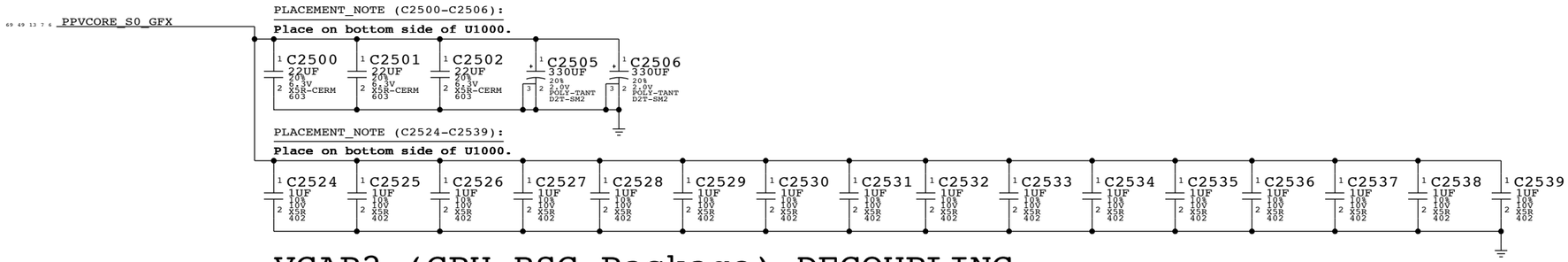
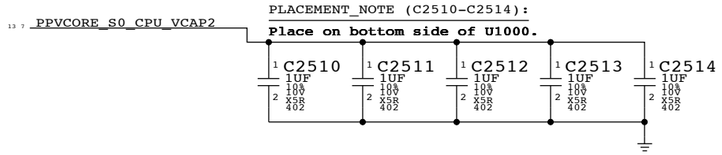
GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603, 16x 1uF 0402

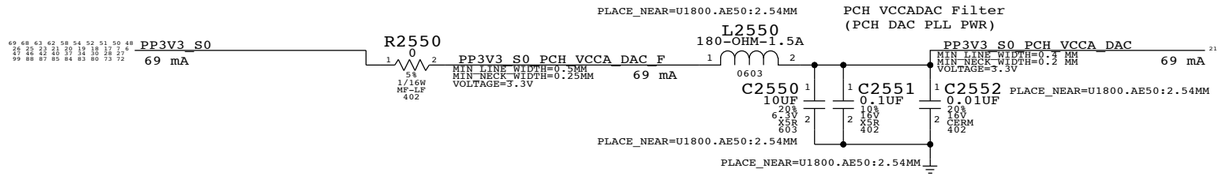


VCAP2 (CPU BSC Package) DECOUPLING

5x 1uF 0402



Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.



Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
CPU/PCH GFX Decoupling

Apple Inc.

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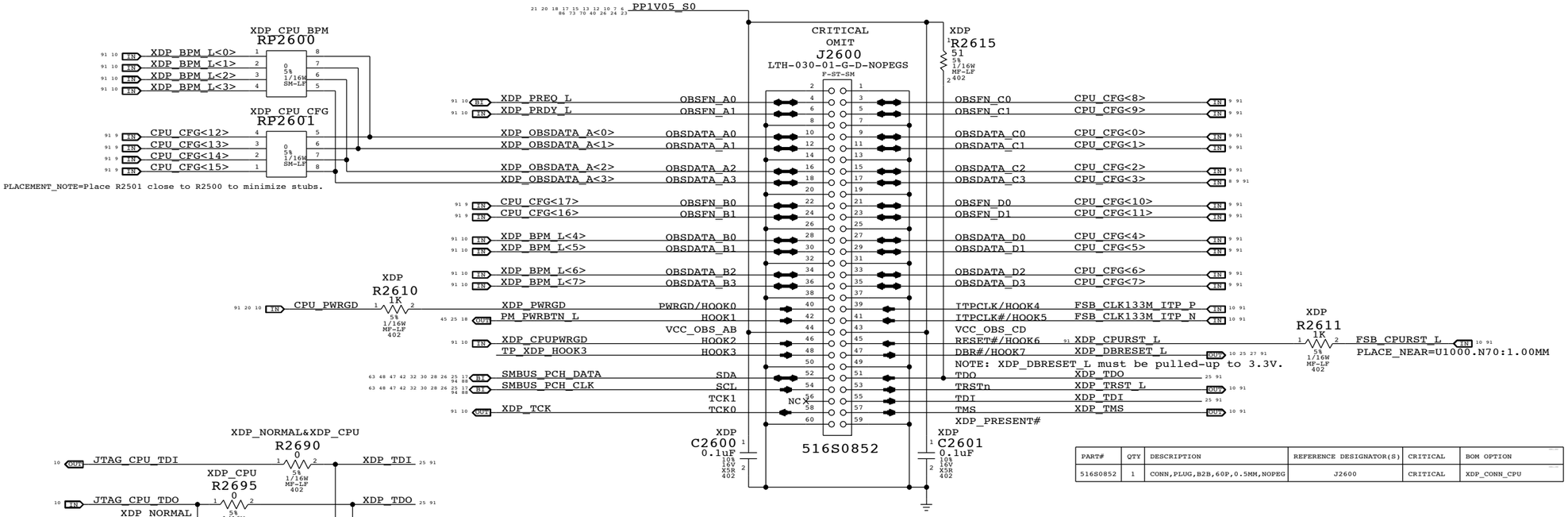
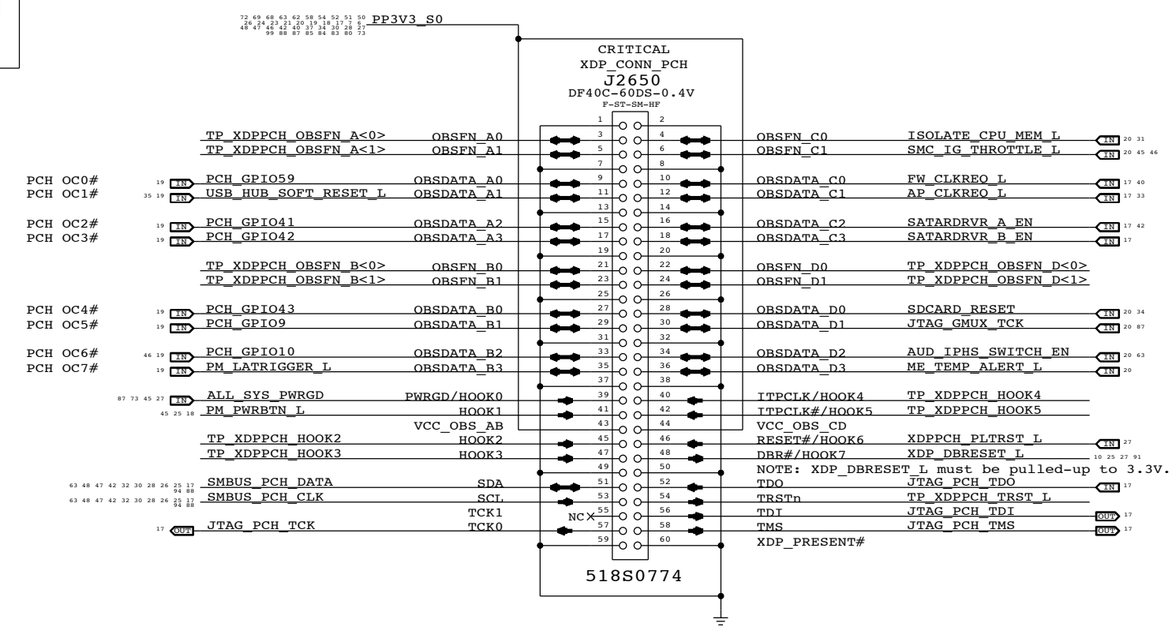
Calpella Processor mini XDP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0852	1	CONN,PLUG,B2B,60P,0.5MM,NOPEG	J2600	CRITICAL	XDP_CONN_CPU

Calpella PCH mini XDP



SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

eXtended Debug Port (XDP)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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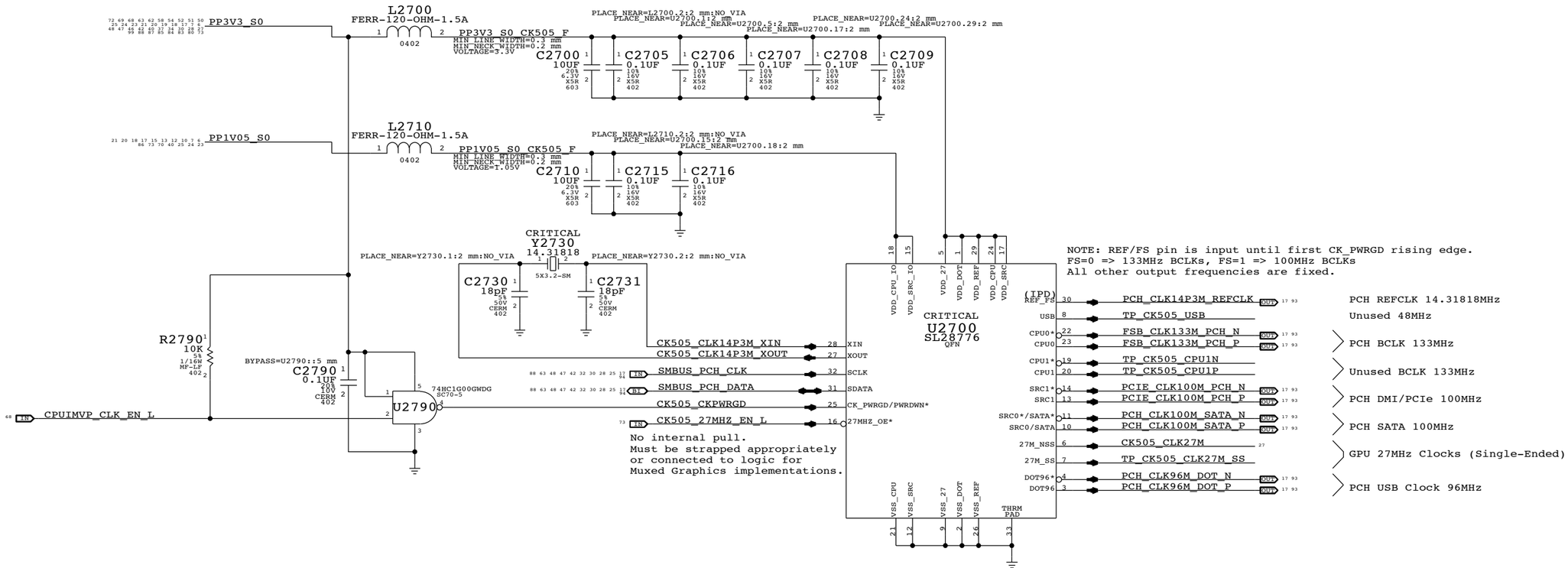

SYNC_MASTER=K17_MLB SYNC_DATE=06/23/2009

PAGE TITLE: Clock (CK505)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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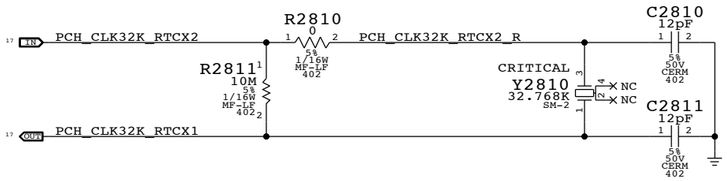
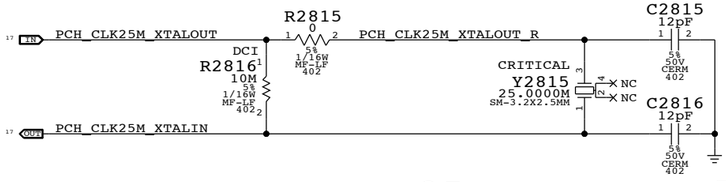
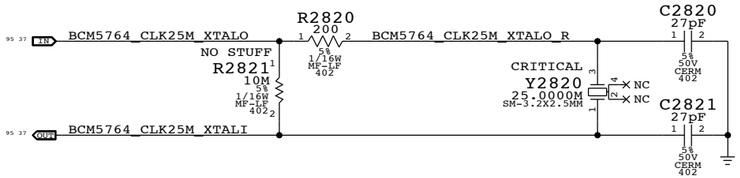
PCH RTC Crystal



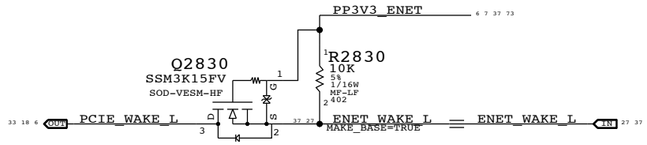
PCH 25MHz Crystal



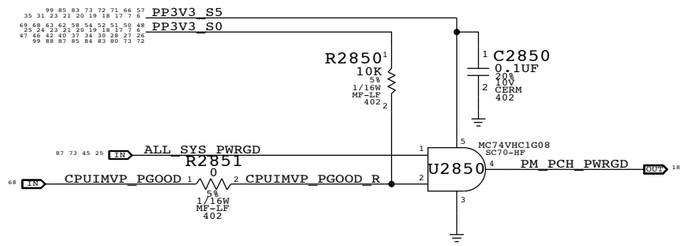
Caesar II (ENET) 25MHz Crystal



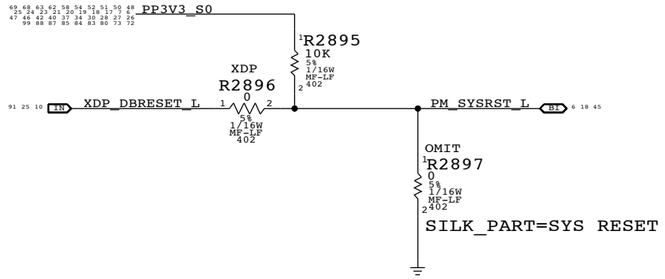
Ethernet WAKE# Isolation



PCH S0 PWRGD

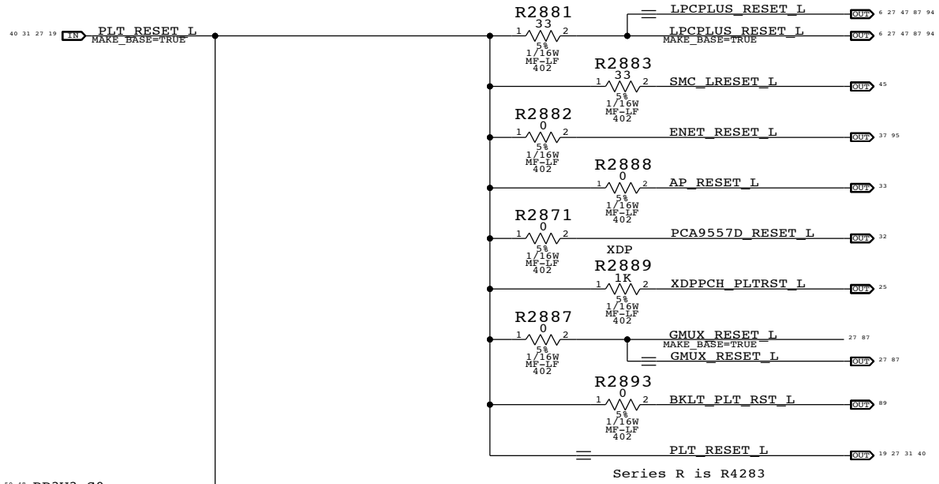


PCH Reset Button



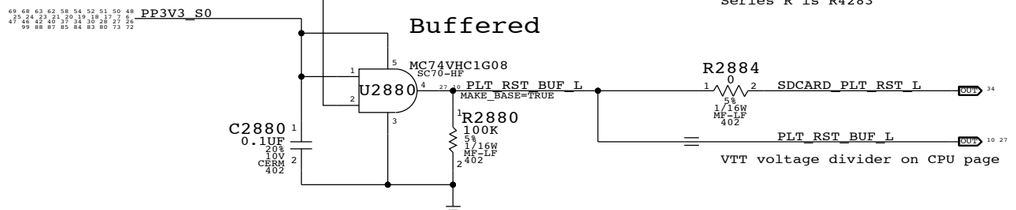
Platform Reset Connections

Unbuffered

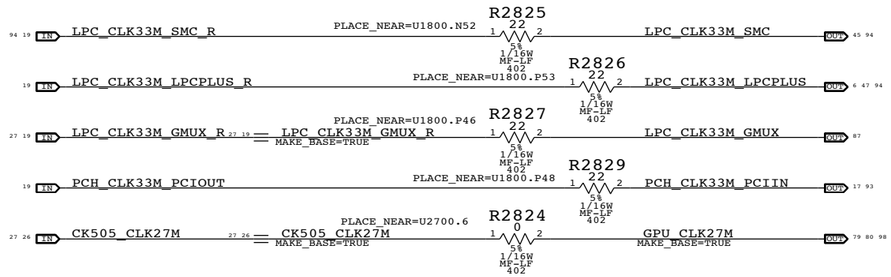


Series R is R4283

Buffered



VTT voltage divider on CPU page



SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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SHEET 27 OF 101

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) F-RT-THB

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

KEY

NC_CKE0 NC_BA2 NC_A12/BC* NC_A9 NC_A8 NC_A5 NC_A3 NC_A1 NC_CK0 NC_CK0* NC_A10/AP NC_BA0 NC_WE* NC_CAS* NC_A13 NC_S1* NC_TEST NC_DM5 NC_DM7 NC_SA0 NC_SA1

MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_BA<2> MEM_A_A<15> MEM_A_A<14>
MEM_A_A<12> MEM_A_A<11>
MEM_A_A<9> MEM_A_A<7>
MEM_A_A<8> MEM_A_A<6>
MEM_A_A<5> MEM_A_A<4>
MEM_A_A<3> MEM_A_A<2>
MEM_A_A<1> MEM_A_A<0>
MEM_A_CLK_P<0> MEM_A_CLK_P<1>
MEM_A_CLK_N<0> MEM_A_CLK_N<1>
MEM_A_A<10> MEM_A_BA<1>
MEM_A_BA<0> MEM_A_RAS_L
MEM_A_WE_L MEM_A_CS_L<0>
MEM_A_CAS_L MEM_A_ODT<0>
MEM_A_A<13> MEM_A_ODT<1>
MEM_A_CS_L<1>

=MEM_A_DQ<32> =MEM_A_DQ<36>
=MEM_A_DQ<33> MEM_A_DQ<37>
=MEM_A_DQS_N<4> =MEM_A_DM<4>
=MEM_A_DQS_P<4>
=MEM_A_DQ<34> =MEM_A_DQ<38>
=MEM_A_DQ<35> =MEM_A_DQ<39>
=MEM_A_DQ<40> =MEM_A_DQ<44>
=MEM_A_DQ<41> =MEM_A_DQ<45>
=MEM_A_DM<5>
=MEM_A_DQ<42> =MEM_A_DQ<46>
=MEM_A_DQ<43> =MEM_A_DQ<47>
=MEM_A_DQ<48> =MEM_A_DQ<52>
=MEM_A_DQ<49> =MEM_A_DQ<53>
=MEM_A_DQS_N<6> =MEM_A_DM<6>
=MEM_A_DQS_P<6>
=MEM_A_DQ<50> =MEM_A_DQ<54>
=MEM_A_DQ<51> =MEM_A_DQ<55>
=MEM_A_DQ<56> =MEM_A_DQ<60>
=MEM_A_DQ<57> =MEM_A_DQ<61>
=MEM_A_DM<7>
=MEM_A_DQ<58> =MEM_A_DQ<62>
=MEM_A_DQ<59> =MEM_A_DQ<63>
MEM_A_SA<0>
MEM_A_SA<1>
MEM_EVENT_A_L
SMBUS_PCH_DATA
SMBUS_PCH_CLK

516-0229
SPD ADDR=0xA0(WR)/0xA1(RD)

PP3V3_S0

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) F-RT-THB CRITICAL

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

KEY

516-0229

=MEM_A_DQ<0> =MEM_A_DQ<4>
=MEM_A_DQ<1> =MEM_A_DQ<5>
MEM_A_DM<0>
=MEM_A_DQ<2> =MEM_A_DQS_N<0>
=MEM_A_DQ<3> =MEM_A_DQS_P<0>
=MEM_A_DQ<8> =MEM_A_DQ<6>
=MEM_A_DQ<9> =MEM_A_DQ<7>
=MEM_A_DQS_N<1> =MEM_A_DQ<12>
=MEM_A_DQS_P<1> =MEM_A_DQ<13>
=MEM_A_DQ<10> =MEM_A_DM<1>
=MEM_A_DQ<11> MEM_RESET_L
=MEM_A_DQ<16> =MEM_A_DQ<14>
=MEM_A_DQ<17> =MEM_A_DQ<15>
=MEM_A_DQS_N<2> =MEM_A_DQ<20>
=MEM_A_DQS_P<2> =MEM_A_DQ<21>
=MEM_A_DQ<18> =MEM_A_DM<2>
=MEM_A_DQ<19>
=MEM_A_DQ<24> =MEM_A_DQ<22>
=MEM_A_DQ<25> =MEM_A_DQ<23>
=MEM_A_DM<3> =MEM_A_DQS_N<3>
=MEM_A_DQS_P<3>
=MEM_A_DQ<26> =MEM_A_DQ<28>
=MEM_A_DQ<27> =MEM_A_DQ<29>
=MEM_A_DQ<30>
=MEM_A_DQ<31>

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

PP0V75_S0_DDRVTT

"Factory" (top) slot

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 29 OF 132
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8	7	6	5	4	3	2	1

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	==	MEM_A_DQS_N<0>	11 28 29 92 92 30 29 11	28
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	==	MEM_A_DQS_P<0>	11 28 29 92 92 30 29 11	28
MEM_A_DM<0>	MAKE_BASE=TRUE	==	MEM_A_DM<0>	11 28 29 92 92 30 29 11	28
MEM_A_DQ<7>	MAKE_BASE=TRUE	==	=MEM_A_DQ<7>	92 11	28
MEM_A_DQ<6>	MAKE_BASE=TRUE	==	=MEM_A_DQ<6>	92 11	28
MEM_A_DQ<5>	MAKE_BASE=TRUE	==	=MEM_A_DQ<1>	92 11	28
MEM_A_DQ<4>	MAKE_BASE=TRUE	==	=MEM_A_DQ<0>	92 11	28
MEM_A_DQ<3>	MAKE_BASE=TRUE	==	=MEM_A_DQ<2>	92 11	28
MEM_A_DQ<2>	MAKE_BASE=TRUE	==	=MEM_A_DQ<3>	92 11	28
MEM_A_DQ<1>	MAKE_BASE=TRUE	==	=MEM_A_DQ<5>	92 11	28
MEM_A_DQ<0>	MAKE_BASE=TRUE	==	=MEM_A_DQ<4>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	==	=MEM_A_DQS_N<1>	92 11	28
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	==	=MEM_A_DQS_P<1>	92 11	28
MEM_A_DM<1>	MAKE_BASE=TRUE	==	=MEM_A_DM<1>	92 11	28
MEM_A_DQ<15>	MAKE_BASE=TRUE	==	=MEM_A_DQ<11>	92 11	28
MEM_A_DQ<14>	MAKE_BASE=TRUE	==	=MEM_A_DQ<10>	92 11	28
MEM_A_DQ<13>	MAKE_BASE=TRUE	==	=MEM_A_DQ<8>	92 11	28
MEM_A_DQ<12>	MAKE_BASE=TRUE	==	=MEM_A_DQ<9>	92 11	28
MEM_A_DQ<11>	MAKE_BASE=TRUE	==	=MEM_A_DQ<15>	92 11	28
MEM_A_DQ<10>	MAKE_BASE=TRUE	==	=MEM_A_DQ<14>	92 11	28
MEM_A_DQ<9>	MAKE_BASE=TRUE	==	=MEM_A_DQ<13>	92 11	28
MEM_A_DQ<8>	MAKE_BASE=TRUE	==	=MEM_A_DQ<12>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	==	=MEM_A_DQS_N<2>	92 11	28
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	==	=MEM_A_DQS_P<2>	92 11	28
MEM_A_DM<2>	MAKE_BASE=TRUE	==	=MEM_A_DM<2>	92 11	28
MEM_A_DQ<23>	MAKE_BASE=TRUE	==	=MEM_A_DQ<23>	92 11	28
MEM_A_DQ<22>	MAKE_BASE=TRUE	==	=MEM_A_DQ<19>	92 11	28
MEM_A_DQ<21>	MAKE_BASE=TRUE	==	=MEM_A_DQ<20>	92 11	28
MEM_A_DQ<20>	MAKE_BASE=TRUE	==	=MEM_A_DQ<22>	92 11	28
MEM_A_DQ<19>	MAKE_BASE=TRUE	==	=MEM_A_DQ<21>	92 11	28
MEM_A_DQ<18>	MAKE_BASE=TRUE	==	=MEM_A_DQ<18>	92 11	28
MEM_A_DQ<17>	MAKE_BASE=TRUE	==	=MEM_A_DQ<17>	92 11	28
MEM_A_DQ<16>	MAKE_BASE=TRUE	==	=MEM_A_DQ<16>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	==	=MEM_A_DQS_N<3>	92 11	28
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	==	=MEM_A_DQS_P<3>	92 11	28
MEM_A_DM<3>	MAKE_BASE=TRUE	==	=MEM_A_DM<3>	92 11	28
MEM_A_DQ<31>	MAKE_BASE=TRUE	==	=MEM_A_DQ<27>	92 11	28
MEM_A_DQ<30>	MAKE_BASE=TRUE	==	=MEM_A_DQ<26>	92 11	28
MEM_A_DQ<29>	MAKE_BASE=TRUE	==	=MEM_A_DQ<25>	92 11	28
MEM_A_DQ<28>	MAKE_BASE=TRUE	==	=MEM_A_DQ<24>	92 11	28
MEM_A_DQ<27>	MAKE_BASE=TRUE	==	=MEM_A_DQ<31>	92 11	28
MEM_A_DQ<26>	MAKE_BASE=TRUE	==	=MEM_A_DQ<30>	92 11	28
MEM_A_DQ<25>	MAKE_BASE=TRUE	==	=MEM_A_DQ<28>	92 11	28
MEM_A_DQ<24>	MAKE_BASE=TRUE	==	=MEM_A_DQ<29>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	==	=MEM_A_DQS_N<4>	92 11	28
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	==	=MEM_A_DQS_P<4>	92 11	28
MEM_A_DM<4>	MAKE_BASE=TRUE	==	=MEM_A_DM<4>	92 11	28
MEM_A_DQ<39>	MAKE_BASE=TRUE	==	=MEM_A_DQ<33>	92 11	28
MEM_A_DQ<38>	MAKE_BASE=TRUE	==	=MEM_A_DQ<39>	92 11	28
MEM_A_DQ<37>	MAKE_BASE=TRUE	==	MEM_A_DQ<37>	92 29 28 11	11 28 29 92 92 30 29 11
MEM_A_DQ<36>	MAKE_BASE=TRUE	==	=MEM_A_DQ<38>	92 11	28
MEM_A_DQ<35>	MAKE_BASE=TRUE	==	=MEM_A_DQ<35>	92 11	28
MEM_A_DQ<34>	MAKE_BASE=TRUE	==	=MEM_A_DQ<34>	92 11	28
MEM_A_DQ<33>	MAKE_BASE=TRUE	==	=MEM_A_DQ<32>	92 11	28
MEM_A_DQ<32>	MAKE_BASE=TRUE	==	=MEM_A_DQ<36>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	==	=MEM_A_DQS_N<5>	92 11	28
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	==	=MEM_A_DQS_P<5>	92 11	28
MEM_A_DM<5>	MAKE_BASE=TRUE	==	=MEM_A_DM<5>	92 11	28
MEM_A_DQ<47>	MAKE_BASE=TRUE	==	=MEM_A_DQ<43>	92 11	28
MEM_A_DQ<46>	MAKE_BASE=TRUE	==	=MEM_A_DQ<42>	92 11	28
MEM_A_DQ<45>	MAKE_BASE=TRUE	==	=MEM_A_DQ<45>	92 11	28
MEM_A_DQ<44>	MAKE_BASE=TRUE	==	=MEM_A_DQ<44>	92 11	28
MEM_A_DQ<43>	MAKE_BASE=TRUE	==	=MEM_A_DQ<47>	92 11	28
MEM_A_DQ<42>	MAKE_BASE=TRUE	==	=MEM_A_DQ<46>	92 11	28
MEM_A_DQ<41>	MAKE_BASE=TRUE	==	=MEM_A_DQ<40>	92 11	28
MEM_A_DQ<40>	MAKE_BASE=TRUE	==	=MEM_A_DQ<41>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	==	=MEM_A_DQS_N<6>	92 11	28
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	==	=MEM_A_DQS_P<6>	92 11	28
MEM_A_DM<6>	MAKE_BASE=TRUE	==	=MEM_A_DM<6>	92 11	28
MEM_A_DQ<55>	MAKE_BASE=TRUE	==	=MEM_A_DQ<49>	92 11	28
MEM_A_DQ<54>	MAKE_BASE=TRUE	==	=MEM_A_DQ<50>	92 11	28
MEM_A_DQ<53>	MAKE_BASE=TRUE	==	=MEM_A_DQ<54>	92 11	28
MEM_A_DQ<52>	MAKE_BASE=TRUE	==	=MEM_A_DQ<53>	92 11	28
MEM_A_DQ<51>	MAKE_BASE=TRUE	==	=MEM_A_DQ<55>	92 11	28
MEM_A_DQ<50>	MAKE_BASE=TRUE	==	=MEM_A_DQ<51>	92 11	28
MEM_A_DQ<49>	MAKE_BASE=TRUE	==	=MEM_A_DQ<48>	92 11	28
MEM_A_DQ<48>	MAKE_BASE=TRUE	==	=MEM_A_DQ<52>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	==	=MEM_A_DQS_N<7>	92 11	28
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	==	=MEM_A_DQS_P<7>	92 11	28
MEM_A_DM<7>	MAKE_BASE=TRUE	==	=MEM_A_DM<7>	92 11	28
MEM_A_DQ<63>	MAKE_BASE=TRUE	==	=MEM_A_DQ<62>	92 11	28
MEM_A_DQ<62>	MAKE_BASE=TRUE	==	=MEM_A_DQ<63>	92 11	28
MEM_A_DQ<61>	MAKE_BASE=TRUE	==	=MEM_A_DQ<56>	92 11	28
MEM_A_DQ<60>	MAKE_BASE=TRUE	==	=MEM_A_DQ<61>	92 11	28
MEM_A_DQ<59>	MAKE_BASE=TRUE	==	=MEM_A_DQ<59>	92 11	28
MEM_A_DQ<58>	MAKE_BASE=TRUE	==	=MEM_A_DQ<58>	92 11	28
MEM_A_DQ<57>	MAKE_BASE=TRUE	==	=MEM_A_DQ<57>	92 11	28
MEM_A_DQ<56>	MAKE_BASE=TRUE	==	=MEM_A_DQ<60>	92 11	28
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	==	MEM_B_DQS_N<0>	11 29 30 92	
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	==	MEM_B_DQS_P<0>	11 29 30 92	
MEM_B_DM<0>	MAKE_BASE=TRUE	==	MEM_B_DM<0>	11 29 30 92	
MEM_B_DQ<7>	MAKE_BASE=TRUE	==	=MEM_B_DQ<7>	92 11	30
MEM_B_DQ<6>	MAKE_BASE=TRUE	==	=MEM_B_DQ<6>	92 11	30
MEM_B_DQ<5>	MAKE_BASE=TRUE	==	=MEM_B_DQ<2>	92 11	30
MEM_B_DQ<4>	MAKE_BASE=TRUE	==	=MEM_B_DQ<4>	92 11	30
MEM_B_DQ<3>	MAKE_BASE=TRUE	==	=MEM_B_DQ<3>	92 11	30
MEM_B_DQ<2>	MAKE_BASE=TRUE	==	=MEM_B_DQ<1>	92 11	30
MEM_B_DQ<1>	MAKE_BASE=TRUE	==	=MEM_B_DQ<5>	92 11	30
MEM_B_DQ<0>	MAKE_BASE=TRUE	==	=MEM_B_DQ<0>	92 11	30
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	==	=MEM_B_DQS_N<1>	92 11	30
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	==	=MEM_B_DQS_P<1>	92 11	30
MEM_B_DM<1>	MAKE_BASE=TRUE	==	=MEM_B_DM<1>	92 11	30
MEM_B_DQ<15>	MAKE_BASE=TRUE	==	=MEM_B_DQ<15>	92 11	30
MEM_B_DQ<14>	MAKE_BASE=TRUE	==	=MEM_B_DQ<14>	92 11	30
MEM_B_DQ<13>	MAKE_BASE=TRUE	==	=MEM_B_DQ<13>	92 11	30
MEM_B_DQ<12>	MAKE_BASE=TRUE	==	=MEM_B_DQ<8>	92 11	30
MEM_B_DQ<11>	MAKE_BASE=TRUE	==	=MEM_B_DQ<11>	92 11	30
MEM_B_DQ<10>	MAKE_BASE=TRUE	==	=MEM_B_DQ<10>	92 11	30
MEM_B_DQ<9>	MAKE_BASE=TRUE	==	=MEM_B_DQ<12>	92 11	30
MEM_B_DQ<8>	MAKE_BASE=TRUE	==	=MEM_B_DQ<9>	92 11	30
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	==	=MEM_B_DQS_N<2>	92 11	30
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	==	=MEM_B_DQS_P<2>	92 11	30
MEM_B_DM<2>	MAKE_BASE=TRUE	==	=MEM_B_DM<2>	92 11	30
MEM_B_DQ<23>	MAKE_BASE=TRUE	==	=MEM_B_DQ<23>	92 11	30
MEM_B_DQ<22>	MAKE_BASE=TRUE	==	=MEM_B_DQ<18>	92 11	30
MEM_B_DQ<21>	MAKE_BASE=TRUE	==	=MEM_B_DQ<20>	92 11	30
MEM_B_DQ<20>	MAKE_BASE=TRUE	==	=MEM_B_DQ<17>	92 11	30
MEM_B_DQ<19>	MAKE_BASE=TRUE	==	=MEM_B_DQ<19>	92 11	30
MEM_B_DQ<18>	MAKE_BASE=TRUE	==	=MEM_B_DQ<22>	92 11	30
MEM_B_DQ<17>	MAKE_BASE=TRUE	==	=MEM_B_DQ<21>	92 11	30
MEM_B_DQ<16>	MAKE_BASE=TRUE	==	=MEM_B_DQ<16>	92 11	30
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	==	=MEM_B_DQS_N<3>	92 11	30
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	==	=MEM_B_DQS_P<3>	92 11	30
MEM_B_DM<3>	MAKE_BASE=TRUE	==	=MEM_B_DM<3>	92 11	30
MEM_B_DQ<31>	MAKE_BASE=TRUE	==	=MEM_B_DQ<27>	92 11	30
MEM_B_DQ<30>	MAKE_BASE=TRUE	==	=MEM_B_DQ<26>	92 11	30
MEM_B_DQ<29>	MAKE_BASE=TRUE	==	=MEM_B_DQ<24>	92 11	30
MEM_B_DQ<28>	MAKE_BASE=TRUE	==	=MEM_B_DQ<30>	92 11	30
MEM_B_DQ<27>	MAKE_BASE=TRUE	==	=MEM_B_DQ<28>	92 11	30
MEM_B_DQ<26>	MAKE_BASE=TRUE	==	=MEM_B_DQ<29>	92 11	30
MEM_B_DQ<25>	MAKE_BASE=TRUE	==	=MEM_B_DQ<31>	92 11	30
MEM_B_DQ<24>	MAKE_BASE=TRUE	==	=MEM_B_DQ<25>	92 11	30
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	==	=MEM_B_DQS_N<4>	92 11	30
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	==	=MEM_B_DQS_P<4>	92 11	30
MEM_B_DM<4>	MAKE_BASE=TRUE	==	=MEM_B_DM<4>	92 11	30
MEM_B_DQ<39>	MAKE_BASE=TRUE	==	=MEM_B_DQ<35>	92 11	30
MEM_B_DQ<38>	MAKE_BASE=TRUE	==	=MEM_B_DQ<38>	92 11	30
MEM_B_DQ<37>	MAKE_BASE=TRUE	==	MEM_B_DQ<37>	11 29 30 92	
MEM_B_DQ<36>	MAKE_BASE=TRUE	==	=MEM_B_DQ<32>	92 11	30
MEM_B_DQ<35>	MAKE_BASE=TRUE	==	=MEM_B_DQ<33>	92 11	30
MEM_B_DQ<34>	MAKE_BASE=TRUE	==	=MEM_B_DQ<39>	92 11	30
MEM_B_DQ<33>	MAKE_BASE=TRUE	==	=MEM_B_DQ<37>	92 11	30
MEM_B_DQ<32>	MAKE_BASE=TRUE	==	=MEM_B_DQ<36>	92 11	30
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	==	=MEM_B_DQS_N<5>	92 11	30
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	==	=MEM_B_DQS_P<5>	92 11	30
MEM_B_DM<5>	MAKE_BASE=TRUE	==	=MEM_B_DM<5>	92 11	30
MEM_B_DQ<47>	MAKE_BASE=TRUE	==	=MEM_B_DQ<47>	92 11	30
MEM_B_DQ<46>	MAKE_BASE=TRUE	==	=MEM_B_DQ<43>	92 11	30
MEM_B_DQ<45>	MAKE_BASE=TRUE	==	=MEM_B_DQ<45>	92 11	30
MEM_B_DQ<44>	MAKE_BASE=TRUE	==	=MEM_B_DQ<41>	92 11	30
MEM_B_DQ<43>	MAKE_BASE=TRUE	==	=MEM_B_DQ<46>	92 11	30
MEM_B_DQ<42>	MAKE_BASE=TRUE	==	=MEM_B_DQ<42>	92 11	30
MEM_B_DQ<41>	MAKE_BASE=TRUE	==	=MEM_B_DQ<44>	92 11	30
MEM_B_DQ<40>	MAKE_BASE=TRUE	==	=MEM_B_DQ<40>	92 11	30
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	==	=MEM_B_DQS_N<6>	92 11	30
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	==	=MEM_B_DQS_P<6>	92 11	30
MEM_B_DM<6>	MAKE_BASE=TRUE	==	=MEM_B_DM<6>	92 11	30
MEM_B_DQ<55>	MAKE_BASE=TRUE	==	=MEM_B_DQ<50>	92 11	30
MEM_B_DQ<54>	MAKE_BASE=TRUE	==	=MEM_B_DQ<55>	92 11	30
MEM_B_DQ<53>	MAKE_BASE=TRUE	==	=MEM_B_DQ<54>	92 11	30
MEM_B_DQ<52>	MAKE_BASE=TRUE	==	=MEM_B_DQ<53>	92 11	30
MEM_B_DQ<51>	MAKE_BASE=TRUE	==	=MEM_B_DQ<49>	92 11	30
MEM_B_DQ<50>	MAKE_BASE=TRUE	==	=MEM_B_DQ<51>	92 11	30
MEM_B_DQ<49>	MAKE_BASE=TRUE	==	=MEM_B_DQ<48>	92 11	30
MEM_B_DQ<48>	MAKE_BASE=TRUE	==	=MEM_B_DQ<52>	92 11	30
	MAKE_BASE=TRUE	==			

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	==	=MEM_B_DQS_N<7>	92 11	30
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	==	=MEM_B_DQS_P<7>	92 11	30
MEM_B_DM<7>	MAKE_BASE=TRUE	==	=MEM_B_DM<7>	92 11	30
MEM_B_DQ<63>	MAKE_BASE=TRUE	==	=MEM_B_DQ<63>	92 11	30
MEM_B_DQ<62>	MAKE_BASE=TRUE	==	=MEM_B_DQ<62>	92 11	30
MEM_B_DQ<61>	MAKE_BASE=TRUE	==	=MEM_B_DQ<57>	92 11	30
MEM_B_DQ<60>	MAKE_BASE=TRUE	==	=MEM_B_DQ<56>	92 11	30
MEM_B_DQ<59>	MAKE_BASE=TRUE	==	=MEM_B_DQ<59>	92 11	30
MEM_B_DQ<58>	MAKE_BASE=TRUE	==	=MEM_B_DQ<58>	92 11	30
MEM_B_DQ<57>	MAKE_BASE=TRUE	==	=MEM_B_DQ<60>	92 11	30
MEM_B_DQ<56>	MAKE_BASE=TRUE	==	=MEM_B_DQ<61>	92 11	30
	MAKE_BASE=TRUE	==			

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

PP1V5_S3

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603

PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 DDR3-SODIMM (2 OF 2) F-RT-BGA6

MEM_B_CKE<0>	73 CKE0	CKE1 74	MEM_B_CKE<1>
NC	75 VDD	VDD 76	
	77 NC	A15 78	MEM_B_A<15>
MEM_B_BA<2>	79 BA2	A14 80	MEM_B_A<14>
	81 VDD	VDD 82	
MEM_B_A<12>	83 A12/BC*	A11 84	MEM_B_A<11>
MEM_B_A<9>	85 A9	A7 86	MEM_B_A<7>
	87 VDD	VDD 88	
MEM_B_A<8>	89 A8	A6 90	MEM_B_A<6>
MEM_B_A<5>	91 A5	A4 92	MEM_B_A<4>
	93 VDD	VDD 94	
MEM_B_A<3>	95 A3	A2 96	MEM_B_A<2>
MEM_B_A<1>	97 A1	A0 98	MEM_B_A<0>
	99 VDD	VDD 100	
MEM_B_CLK_P<0>	101 CK0	CK1 102	MEM_B_CLK_P<1>
MEM_B_CLK_N<0>	103 CK0*	CK1* 104	MEM_B_CLK_N<1>
	105 VDD	VDD 106	
MEM_B_A<10>	107 A10/AP	BA1 108	MEM_B_BA<1>
MEM_B_BA<0>	109 BA0	RAS* 110	MEM_B_RAS_L
	111 VDD	VDD 112	
MEM_B_WE_L	113 WE*	S0* 114	MEM_B_CS_L<0>
MEM_B_CAS_L	115 CAS*	ODT0 116	MEM_B_ODT<0>
	117 VDD	VDD 118	
MEM_B_A<13>	119 A13	ODT1 120	MEM_B_ODT<1>
MEM_B_CS_L<1>	121 S1*	NC 122 NC	
	123 VDD	VDD 124	
NC	125 TEST	VREFCA 126	
	127 VSS	VSS 128	
=MEM_B_DQ<32>	129 DQ32	DQ36 130	=MEM_B_DQ<36>
=MEM_B_DQ<33>	131 DQ33	DQ37 132	=MEM_B_DQ<37>
	133 VSS	VSS 134	
=MEM_B_DQS_N<4>	135 DQS4*	DM4 136	=MEM_B_DM<4>
=MEM_B_DQS_P<4>	137 DQS4	VSS 138	
	139 VSS	DQ38 140	=MEM_B_DQ<38>
MEM_B_DQ<37>	141 DQ34	DQ39 142	=MEM_B_DQ<39>
=MEM_B_DQ<35>	143 DQ35	VSS 144	
	145 VSS	DQ44 146	=MEM_B_DQ<44>
=MEM_B_DQ<40>	147 DQ40	DQ45 148	=MEM_B_DQ<45>
=MEM_B_DQ<41>	149 DQ41	VSS 150	
	151 VSS	DQS5* 152	=MEM_B_DQS_N<5>
=MEM_B_DM<5>	153 DM5	DQS5 154	=MEM_B_DQS_P<5>
	155 VSS	VSS 156	
=MEM_B_DQ<42>	157 DQ42	DQ46 158	=MEM_B_DQ<46>
=MEM_B_DQ<43>	159 DQ43	DQ47 160	=MEM_B_DQ<47>
	161 VSS	VSS 162	
=MEM_B_DQ<48>	163 DQ48	DQ52 164	=MEM_B_DQ<52>
=MEM_B_DQ<49>	165 DQ49	DQ53 166	=MEM_B_DQ<53>
	167 VSS	VSS 168	
=MEM_B_DQS_N<6>	169 DQS6*	DM6 170	=MEM_B_DM<6>
=MEM_B_DQS_P<6>	171 DQS6	VSS 172	
	173 VSS	DQ54 174	=MEM_B_DQ<54>
=MEM_B_DQ<50>	175 DQ50	DQ55 176	=MEM_B_DQ<55>
=MEM_B_DQ<51>	177 DQ51	VSS 178	
	179 VSS	DQ60 180	=MEM_B_DQ<60>
=MEM_B_DQ<56>	181 DQ56	DQ61 182	=MEM_B_DQ<61>
=MEM_B_DQ<57>	183 DQ57	VSS 184	
	185 VSS	DQS7* 186	=MEM_B_DQS_N<7>
=MEM_B_DM<7>	187 DM7	DQS7 188	=MEM_B_DQS_P<7>
	189 VSS	VSS 190	
=MEM_B_DQ<58>	191 DQ58	DQ62 192	=MEM_B_DQ<62>
=MEM_B_DQ<59>	193 DQ59	DQ63 194	=MEM_B_DQ<63>
	195 VSS	VSS 196	
MEM_B_SA<0>	197 SA0	EVENT* 198	MEM_EVENT_A_L
PP3V3_S0	199 VDDSPD	SDA 200	SMBUS_PCH_DATA
MEM_B_SA<1>	201 SA1	SCL 202	SMBUS_PCH_CLK
	203 VTT	VTT 204	PP0V75_S0_DDRVTT
	205 MTG PIN	MTG PIN 206	
	207 MTG PIN	MTG PIN 208	
	209 MTG PIN	MTG PIN 210	
	211 MTG PIN	MTG PIN 212	

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

J3100 DDR3-SODIMM (1 OF 2) F-RT-BGA6 CRITICAL

	1 VREFDQ	VSS 2	
=MEM_B_DQ<0>	3 VSS	DQ4 4	=MEM_B_DQ<4>
=MEM_B_DQ<1>	5 DQ0	DQ5 6	=MEM_B_DQ<5>
	7 DQ1	VSS 8	
MEM_B_DM<0>	9 VSS	DQS0* 10	MEM_B_DQS_N<0>
	11 DM0	DQS0 12	MEM_B_DQS_P<0>
	13 VSS	VSS 14	
=MEM_B_DQ<2>	15 DQ2	DQ6 16	=MEM_B_DQ<6>
=MEM_B_DQ<3>	17 DQ3	DQ7 18	=MEM_B_DQ<7>
	19 VSS	VSS 20	
=MEM_B_DQ<8>	21 DQ8	DQ12 22	=MEM_B_DQ<12>
=MEM_B_DQ<9>	23 DQ9	DQ13 24	=MEM_B_DQ<13>
	25 VSS	VSS 26	
=MEM_B_DQS_N<1>	27 DQS1*	DM1 28	=MEM_B_DM<1>
=MEM_B_DQS_P<1>	29 DQS1	RESET* 30	MEM_RESET_L
	31 VSS	VSS 32	
=MEM_B_DQ<10>	33 DQ10	DQ14 34	=MEM_B_DQ<14>
=MEM_B_DQ<11>	35 DQ11	DQ15 36	=MEM_B_DQ<15>
	37 VSS	VSS 38	
=MEM_B_DQ<16>	39 DQ16	DQ20 40	=MEM_B_DQ<20>
=MEM_B_DQ<17>	41 DQ17	DQ21 42	=MEM_B_DQ<21>
	43 VSS	VSS 44	
=MEM_B_DQS_N<2>	45 DQS2*	DM2 46	=MEM_B_DM<2>
=MEM_B_DQS_P<2>	47 DQS2	VSS 48	
	49 VSS	DQ22 50	=MEM_B_DQ<22>
=MEM_B_DQ<18>	51 DQ18	DQ23 52	=MEM_B_DQ<23>
=MEM_B_DQ<19>	53 DQ19	VSS 54	
	55 VSS	DQ28 56	=MEM_B_DQ<28>
=MEM_B_DQ<24>	57 DQ24	DQ29 58	=MEM_B_DQ<29>
=MEM_B_DQ<25>	59 DQ25	VSS 60	
	61 VSS	DQS3* 62	=MEM_B_DQS_N<3>
=MEM_B_DM<3>	63 DM3	DQS3 64	=MEM_B_DQS_P<3>
	65 VSS	VSS 66	
=MEM_B_DQ<26>	67 DQ26	DQ30 68	=MEM_B_DQ<30>
=MEM_B_DQ<27>	69 DQ27	DQ31 70	=MEM_B_DQ<31>
	71 VSS	VSS 72	

KEY

516S0806

PP0V75_S3_MEM_VREFCA_B

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

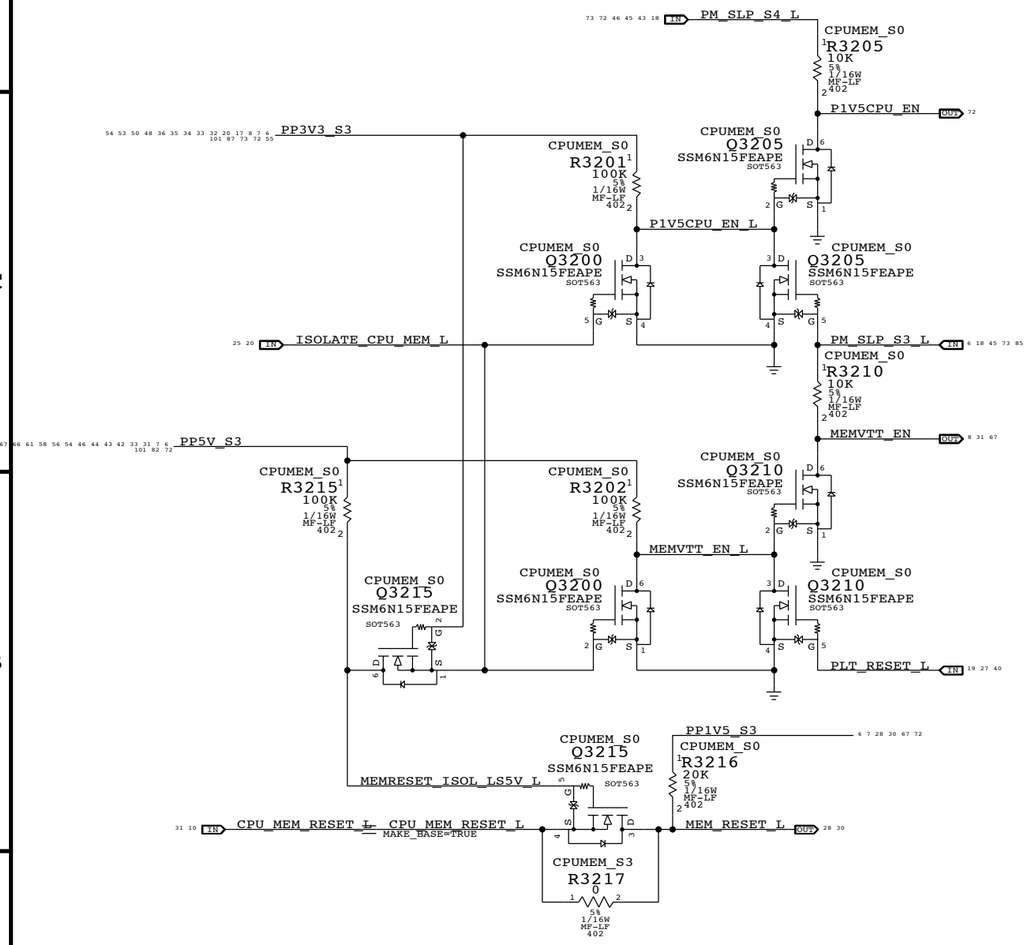
"Expansion" (bottom) slot

SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE: DDR3 SO-DIMM Connector B	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH: <BRANCH>
	PAGE: 31 OF 132
	SHEET: 30 OF 101

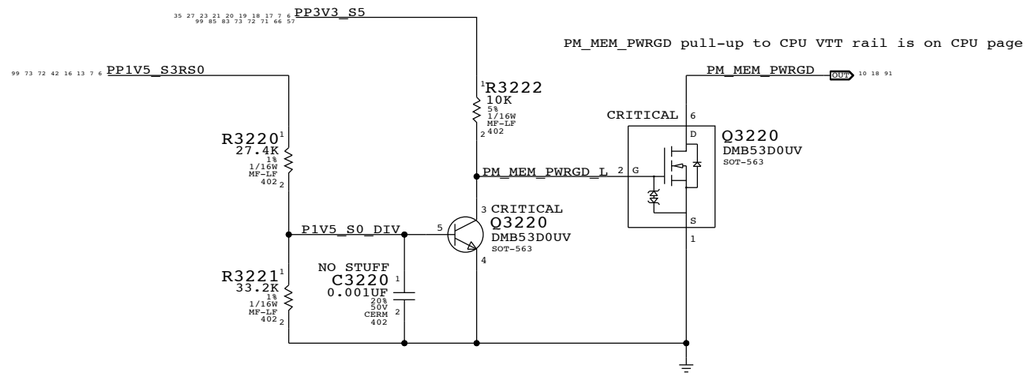
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

```
P1V5CPU_EN  = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN   = (ISOLATE_CPU_MEM_L + PLT_RST_L)   * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
```

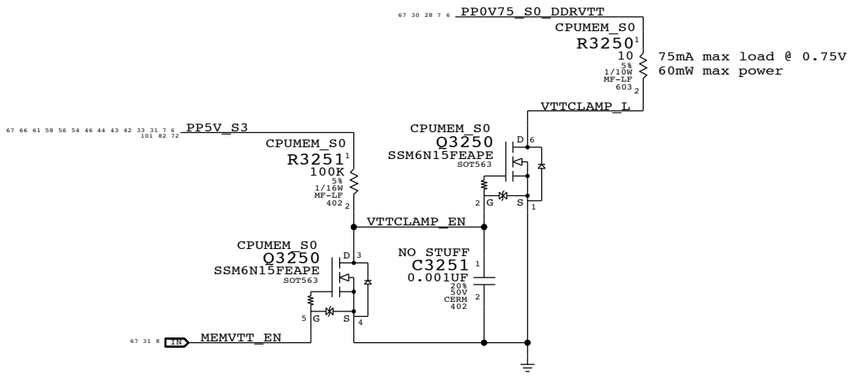


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

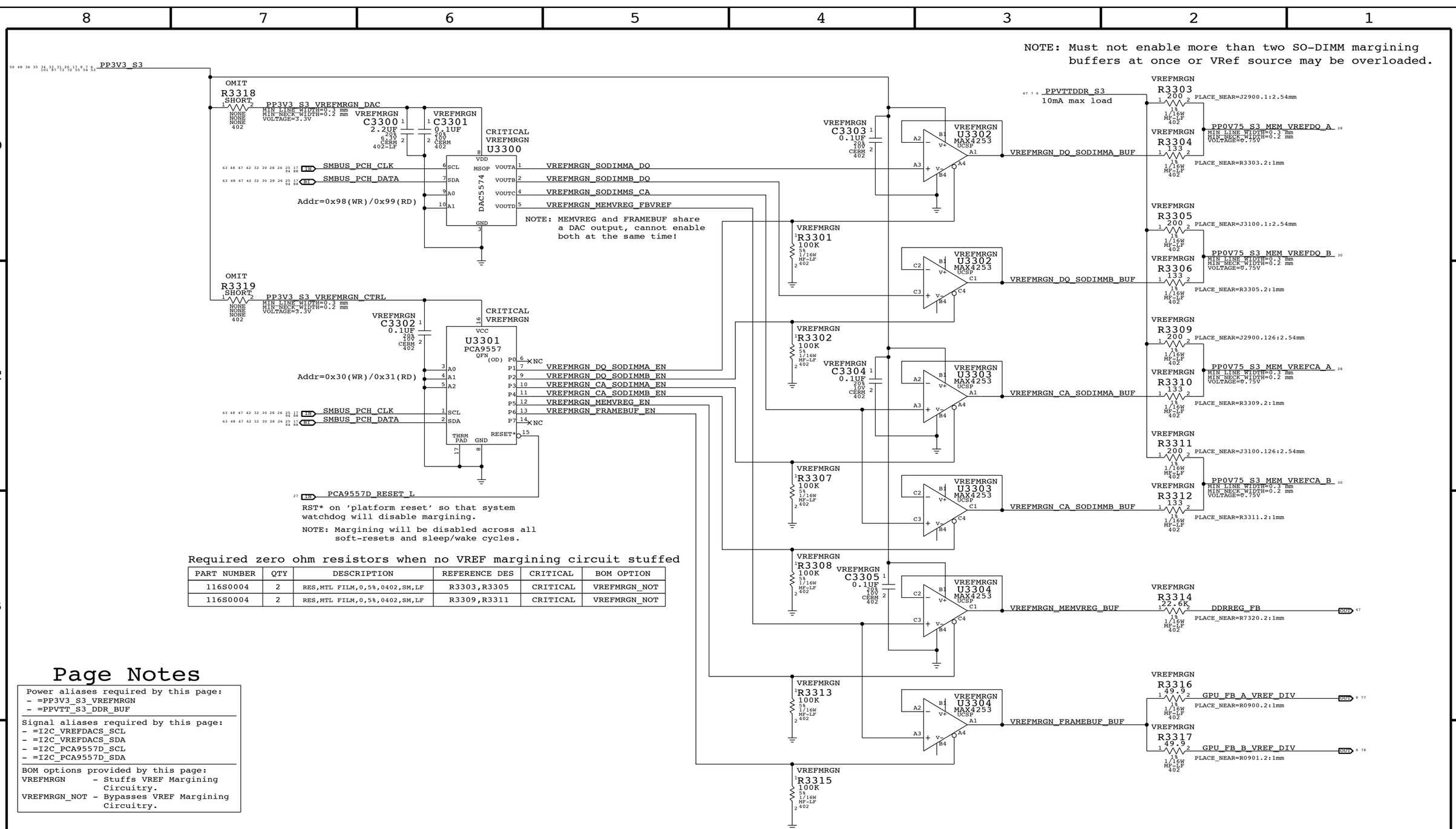
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 32 OF 132
SHEET: 31 OF 101



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305	CRITICAL	VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311	CRITICAL	VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- VREFMRGN – Stuffs VREF Margining Circuitry.
- VREFMRGN_NOT – Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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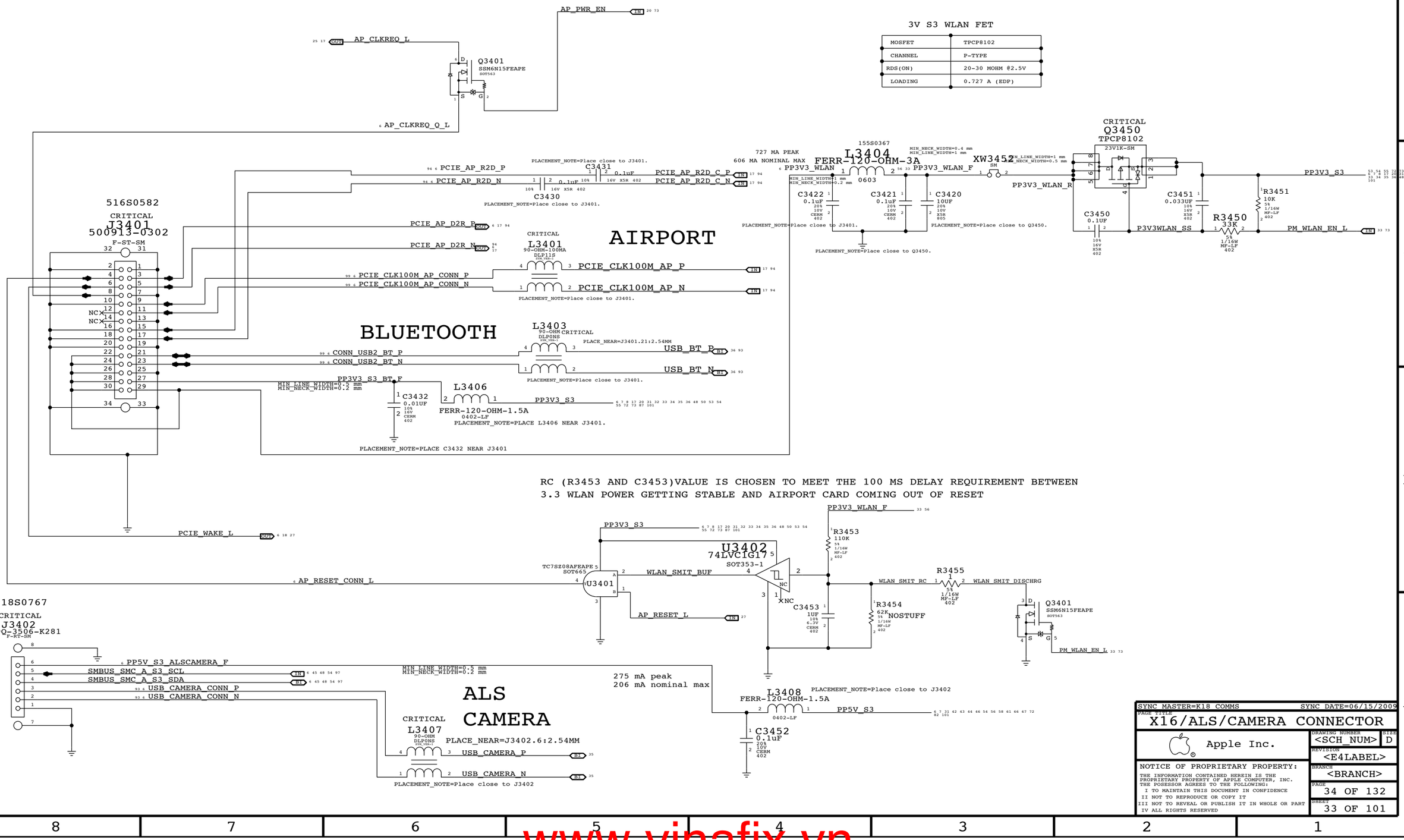

SYNC_MASTER=K18_COMMS SYNC_DATE=06/15/2009

PAGE TITLE
X16/ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Caesar IV Support

PP3V3_S3

GL137 R3511 0 5% 1/16W MF-LF 402

PP3V3_S3_CARDREADER_DVDD
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

BYPASS=U3500.15:16:5 mm
BYPASS=U3500.26:27:5 mm
BYPASS=U3500.35:34:5 mm

GL137 C3500 10UF 20% 6.3V X5R 603
GL137 C3501 0.1UF 20% 10V CERM 402
GL137 C3502 0.1UF 20% 10V CERM 402
GL137 C3503 0.1UF 20% 10V CERM 402

GL137 L3500 0.22UH 0805-1

PP3V3_S3_CARDREADER_AVDD
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

BYPASS=U3500.6:5:5 mm
BYPASS=U3500.11:12:5 mm

GL137 C3514 10UF 20% 6.3V X5R 603
GL137 C3504 0.1UF 20% 10V CERM 402
GL137 C3508 0.1UF 20% 10V CERM 402

PP1V8_S3_CARDREADER
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=1.8V

BYPASS=U3500.4:5:5 mm
GL137 C3506 0.1UF 20% 10V CERM 402

GL137 R3507 10K 5% 1/16W MF-LF 402
NO STUFF R3508 10K 5% 1/16W MF-LF 402
NO STUFF R3509 10K 5% 1/16W MF-LF 402
GL137 R3510 10K 5% 1/16W MF-LF 402

NO STUFF R3503 1M 5% 1/16W MF-LF 402
GL137 CRITICAL Y3500 12.000M-100PPM 8X4.5X1.4-SM
GL137 C3511 33PF 5% 50V CERM 402
GL137 C3512 33PF 5% 50V CERM 402

GL137 R3506 715 1% 1/16W MF-LF 402
GL137 R3502 0 5% 1/16W MF-LF 402
NO STUFF C3513 0.1UF 20% 10V CERM 402

GL137 Q3500 SSM6N15FEAPE SOT563
GL137 Q3500 SSM6N15FEAPE SOT563

SDCARD_RESET
SDCARD_PLT_RST
SDCARD_PLT_RST_L

U3500 GL137A LQFP
CRITICAL GL137

USB_SDCARD_N	7	DM
USB_SDCARD_P	8	DP
GL137_GPIO1	48	GPIO1
GL137_GPIO2	47	GPIO2
	46	GPIO3
	19	SK
	20	CS
	21	DO
	22	DI (IPD)
GL137_CLK12M_X1	13	X1
GL137_CLK12M_X2	14	X2
GL137_RREF	10	RREF
GL137_TESTMOD	17	TESTMOD (IPD)
GL137_RESET_L	18	EXTRSTZ* (IPU)

VDD18O, AVDD, DVDD, VDD5V, PMOSO

D0	40	
D1	43	
D2	37	
D3	29	
D4	28	
D5	30	
D6	32	
D7	38	
CLK	39	SD_CLK_R
(IPD) SD_WP	3	
(IPD) SD_CMD	41	
(IPU) PDMOD	2	GL137_PDMOD
(IPU) SD_CDZ	23	
(IPU) XD_CDZ	1	NC
XD_CE	31	NC
(IPD) XD_WEZ	42	NC
(IPD) XD_RBZ	44	NC
(IPD) XD_WPZ	45	NC
(IPU) MS_INS	24	NC
(IPD) MS_BS	33	NC

GND: 5, 9, 12, 16, 27, 34

GL137 R3512 10K 5% 1/16W MF-LF 402
NO STUFF R3513 10K 5% 1/16W MF-LF 402

GL137 C3507 2.2UF 20% 6.3V CERM1 603
GL137 C3505 0.1UF 20% 10V CERM 402
GL137 R3505 39K 5% 1/16W MF-LF 402

Keep this net short!

PP3V3_SW_SD_PWR
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
Max Current = 250 mA

PP3V3_S0
BCM57765 R3555 0 5% 1/10W MF-LF 603

BCM57765 R3550 0 5% 1/16W MF-LF 402
SDCONN_DATA<0> — SD_D<0>

BCM57765 R3551 0 5% 1/16W MF-LF 402
SDCONN_DATA<1> — SD_D<1>

BCM57765 R3552 0 5% 1/16W MF-LF 402
SDCONN_DATA<2> — SD_D<2>

BCM57765 R3553 0 5% 1/16W MF-LF 402
SDCONN_DATA<3> — SD_D<3>

SDCONN_DATA<4..7> — SD_D<4..7> MAKE_BASE=TRUE

BCM57765 R3554 0 5% 1/16W MF-LF 402
SDCONN_CLK — SD_CLK

BCM57765 R3556 0 5% 1/16W MF-LF 402
SDCONN_CMD — SD_CMD

SD_WP — SD_WP MAKE_BASE=TRUE

SD_CD_L — SD_CD_L MAKE_BASE=TRUE

GL137 R3504 0 5% 1/16W MF-LF 402
NO STUFF C3515 10PF 5% 50V CERM 402-1

CRITICAL
J3500
SD-CARD-K19-K24
F-RT-TH

3	VSS
6	VSS
5	CLK
2	CMD
7	DAT0
8	DAT1
9	DAT2
1	CD/DAT3
10	DAT4
11	DAT5
12	DAT6
13	DAT7
14	CARD_DETECT_SW
15	CARD_DETECT_GND
16	WRITE_PROTECT_SW
4	VDD
17	SHLD_PIN
18	SHLD_PIN
19	SHLD_PIN
20	SHLD_PIN

516-0225

PDMOD: POWER DOWN MODES
NC = DISABLE (DEFAULT)
10K LOW = POWER SAVING MODE ENABLE
10K HIGH = REMOTE WAKE UP ENABLE

SYNC_MASTER=T27_REF SYNC_DATE=08/26/2009

PAGE TITLE: SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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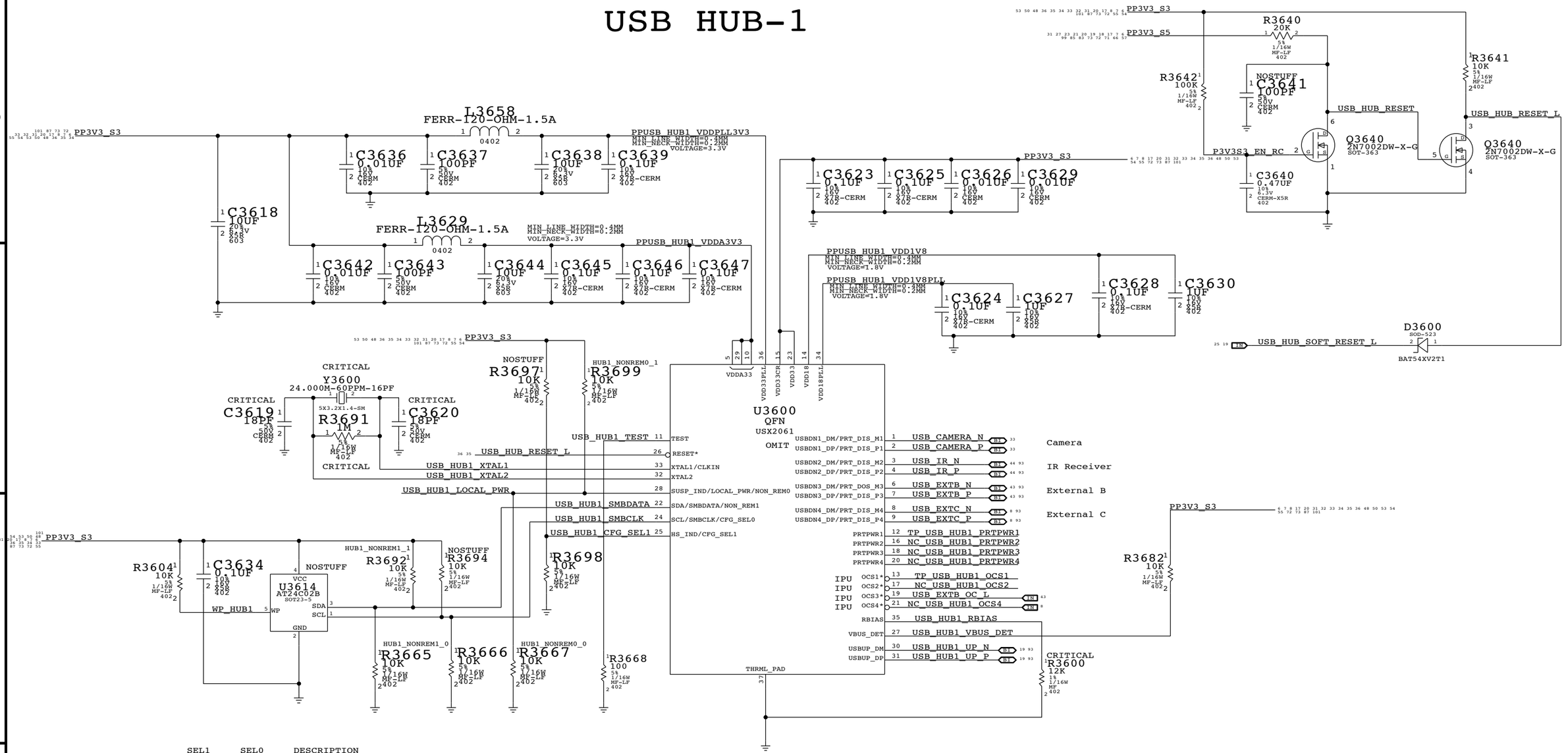
USB HUB-1



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U3600,U3700	CRITICAL	USBHUB_2061

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

SYNC MASTER=K18 MLB SYNC DATE=10/07/2009

PAGE TITLE: USB HUB 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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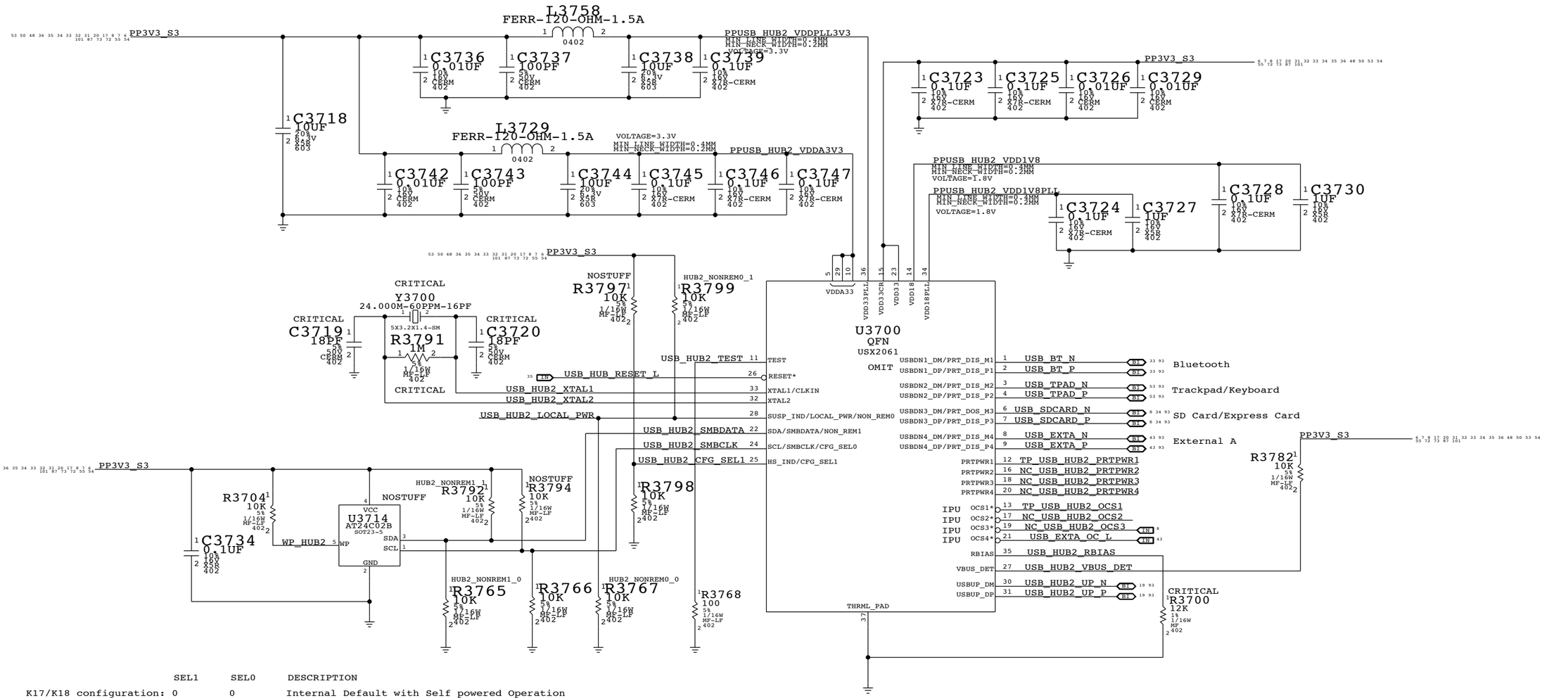
USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

SYNC_MASTER=K23F SYNC_DATE=10/06/2009

PAGE TITLE: USB HUB 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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BCM57765 SR pins are internal 1.2V switching regulator.
If unused: Okay to float all 4 pins. (Broadcom not so sure now)
If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY

PP3V3_ENET
86mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-0.5A
CRITICAL L3905 FERR-600-OHM-0.5A
CRITICAL L3910 FERR-600-OHM-0.5A

PP3V3_ENET_PHY_XTALVDDH
PP3V3_ENET_PHY_BIASVDDH
PP3V3_ENET_PHY_AVDDH

BCM57765 R3915 0 5% 1/16W MF-LF 402
BCM57765 R3900 0 5% 1/16W MF-LF 402
C3900 0.1UF 10% 16V X7R-CERM 402
C3905 0.1UF 10% 16V X7R-CERM 402
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

TP_BCM57765_SR_VDDP
BCM57765_SR_VDD
BCM57765_VDDO_PIN20
BCM57765_XTALVDDH
BCM57765_SR_LX
BCM57765_SR_VFB

CRITICAL L3920 FERR-600-OHM-0.5A PP1V2_ENET
396mA (1000base-T, Caesar II)
CRITICAL L3925 FERR-600-OHM-0.5A
CRITICAL L3930 FERR-600-OHM-0.5A

PP1V2_ENET_PHY_AVDDL
PP1V2_ENET_PHY_PCIEPLL
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603
C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

BCM57765 R3940 4.7K 5% 1/16W MF-LF 402
BCM57765 R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

PP3V3_S0
BCM57765 R3942 1K 5% 1/16W MF-LF 402

AVDDH, BIASVDDH, VDDC, VDDIO, XTALVDDH, VDDIO, VDDIO, VDDC, REGCTL12, VDDIO, WAKE*, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC, VDDC

CRITICAL OMIT U3900 BCM5764M QFN-8X8 VERSION 2

C3950 0.1uF
C3951 0.1uF
C3955 0.1uF
C3956 0.1uF

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

BCM57765 R3943 0 5% 1/16W MF-LF 402
ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
BCM57765_WAKE_L
ENET_LOW_PWR
BCM57765_SMB_CLK
BCM57765_SMB_DATA
BCM5764_SCLK
BCM5764_MISO
BCM5764_MOSI
BCM5764_CS_L
TP_BCM5764_SPD100LED_L
TP_BCM5764_TRAFFICLED_L
BCM5764_CLK25M_XTALI
BCM5764_CLK25M_XTALO
BCM5764_RDAC

SMB_DATA (IPD)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
LINKLED* (OD)
LOW_PWR (IPD)
VDDC
UART_MODE (IPD-BCM5764M)
SCLK
SI
SO
CS*
(IPD)
SPD100LED*
TRAFFICLED*
XTALI
XTALO
RDAC

R3965 1.24K 1% 1/16W MF-LF 402

THRM_PAD 69

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
TRD0_P, TRD0_N, TRD1_P, TRD1_N, TRD2_P, TRD2_N, TRD3_P, TRD3_N

CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.
BCM57765 C3970 4.7UF 10% 6.3V X5R-CERM 603
BCM57765 C3971 0.1UF 10% 16V X7R-CERM 402
BCM57765 C3972 0.1UF 10% 16V X7R-CERM 402

PP3V3R1V8_SW_SD_VIO
GPIO_0/SERIAL_DO (IPD)
GPIO_1/SERIAL_DI (IPD)
NC
GPIO_2
NC
PCIE_VDDL
DC0
DC4
DC3
DC2
DC1
NC
VMAIN_PRSNT
VAUX_PRSNT
VDDC
SMB_CLK
ENERGY_DET
DC5
SPD1000LED*

BCM57765_MEDIA_SENSE R3972 0 5% 1/16W MF-LF 402 ENET_ENERGY_DET
BCM57765_SD_DETECT R3973 0 5% 1/16W MF-LF 402 SD_CD_L
BCM57765_CR_CMD R3974 0 5% 1/16W MF-LF 402 SDCONN_CMD
PLACE_NEAR=L3999.1:1 mm
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>
BCM57765_CR_DATA<4> R3975 0
BCM57765_CR_DATA<5> R3976 0
BCM57765_CR_DATA<6> R3977 0
BCM57765_CR_DATA<7> R3978 0
BCM57765_CE_L_MS_INS_L
BCM57765_CR_LED
TP_BCM57765_XD_DET
SD_WP

BCM57765 All resistors above BOMOPTIONed BCM57765
BCM57765 supports both active-levels for WP.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)

PP3V3_ENET
U3990 AT45DB011D SOIC-8S1 OMIT
VCC, SCK, CS*, WP*, RESET*, GND, SI, SO
C3990 0.1UF 10% 16V X7R-CERM 402
BCM5764_SCLK
BCM5764_CS_L
BCM5764_MOSI
BCM5764_MISO
BCM57765 R3990 4.7K 5% 1/16W MF-LF 402
BCM5764M R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M pin-function

60-ENERGY_DET	BCM57765_CR_LED	R3980	0		ENET_ENERGY_DET
13-WAKE*	BCM57765_SR_VFB	R3981	0		ENET_WAKE_L (See note)
53-VMAIN_PRSNT	BCM57765_CR_DATA<5>	R3982	1K		PP3V3_S0
59-SMB_CLK	BCM57765_CE_L_MS_INS_L	R3983	4.7K		PP3V3_ENET
58-SMB_DATA	BCM57765_VMAIN_PRSNT	R3984	4.7K		
54-VAUX_PRSNT	BCM57765_CR_DATA<6>	R3985	1K		
16-VDDIO	BCM57765_SR_LX	R3986	0		
20-XTALVDDH	BCM57765_VDDO_PIN20	R3987	0		PP3V3_ENET_PHY_XTALVDDH
55-VDDC	BCM57765_CR_DATA<7>	R3988	0		PP1V2_ENET
17-VDDC	BCM57765_XTALVDDH	R3989	0		
14-VDDC	BCM57765_SR_VDD	R3998	0		
06-VDDC	BCM57765_SMB_CLK	R3999	0		

All resistors 5% 1/16W MF-LF 402

L3999 FERR-600-OHM-0.5A SM CRITICAL
26-PCIE_VDDL — BCM57765_CR_CMD — PLACE_NEAR=U3900.26:2 mm
BCM5764M C3999 0.1UF 10% 16V X7R-CERM 402 — PLACE_NEAR=U3900.26:1 mm
BCM5764M C3998 4.7UF 10% 6.3V X5R-CERM 603 — PLACE_NEAR=L3999.1:1 mm

Keep net short, with no stubs.

SYNC_MASTER=T27_REF SYNC_DATE=08/20/2009
PAGE TITLE: Ethernet PHY (Caesar II/IV)
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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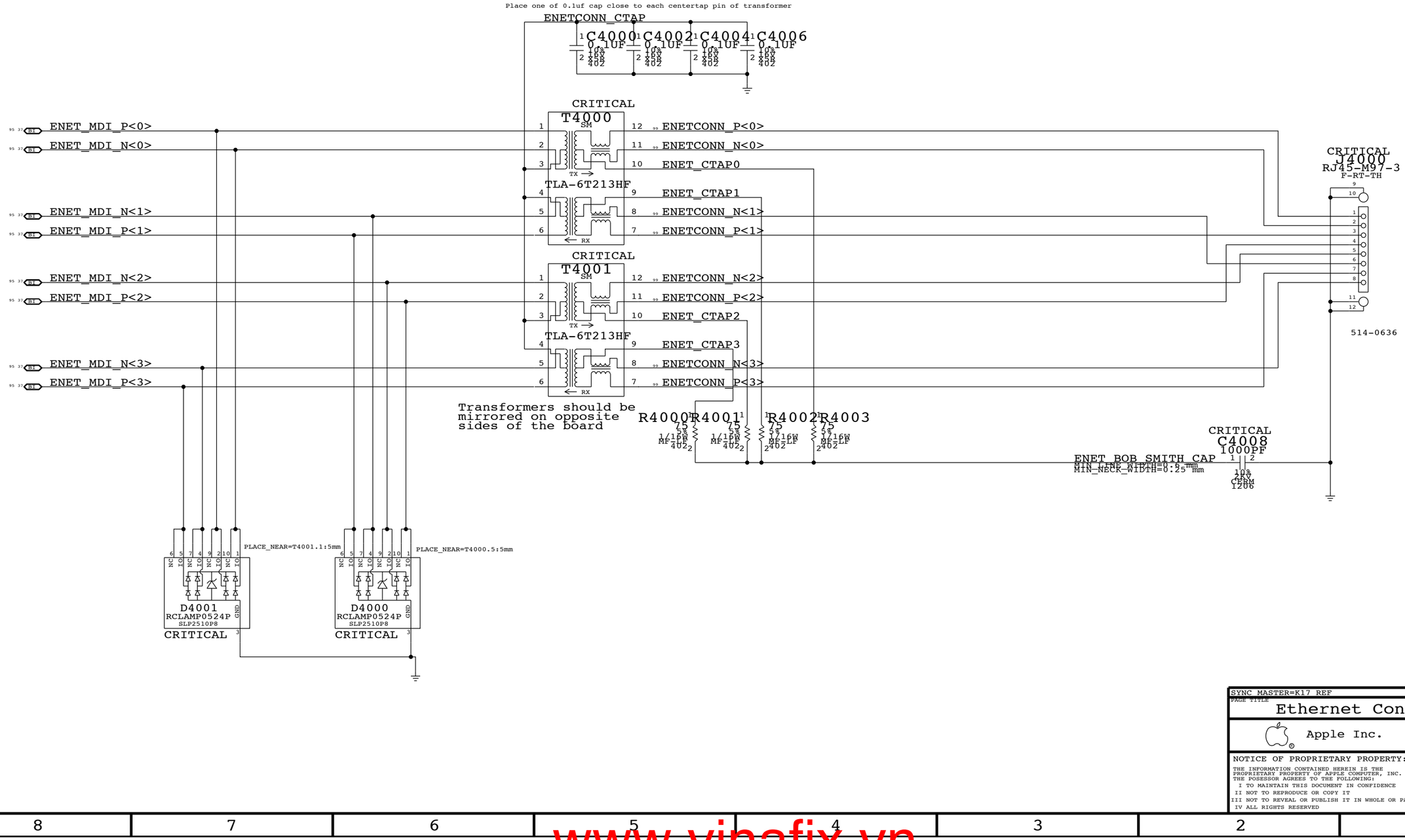
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	

OMIT
R4100 0.2 1% 1/16W MF-LF 402

PP1V0_FW_FWPHY 40 7 6
135 mA
PP1V0_FW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

L4110 120-OHM-0.3A-EMI 0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402

PP3V3_FW_FWPHY 6 7 39 40 41
138 mA

L4130 120-OHM-0.3A-EMI 0402-LF
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

114 mA FireWire PHY
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402

L4135 120-OHM-0.3A-EMI 0402-LF
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

17 mA PCIe SerDes
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402

0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

A1 B1 B12 C13 E2 E10 H2 H12 K2 L1 M12 N3 N11 — VDD10
C1 C12 F1 G12 J1 L3 L11 M2 — VDD33
A12 D5 D6 D8 — VDDH
L5 — VP
L10 — VP25
L6 L9 — VREG_PWR
K12

OMIT
CRITICAL
U4100
FW643
BGA

NC B13 ATBUSB
NC A13 ATBUSH
NC A11 ATBUSN

41 IN FWPHY_DS0 F12 DS0 (IPD) NT-19
41 IN FWPHY_DS1 E12 DS1 (IPD) NT-20
41 IN FWPHY_DS2 E13 DS2 (IPD) NT-21

96 41 B1 NC_FW0_TPAN B8 TPA0N
96 41 B1 NC_FW0_TPAP A8 TPA0P
96 41 B1 FW_PORT1_TPA_N B5 TPA1N
96 41 B1 FW_PORT1_TPA_P A5 TPA1P
41 B1 NC_FW2_TPAN B3 TPA2N
41 B1 NC_FW2_TPAP A3 TPA2P
96 41 B1 NC_FW0_TPBN B9 TPB0N
96 41 B1 NC_FW0_TPBP A9 TPB0P
96 41 B1 FW_PORT1_TPB_N B6 TPB1N
96 41 B1 FW_PORT1_TPB_P A6 TPB1P
41 B1 NC_FW2_TPBN B4 TPB2N
41 B1 NC_FW2_TPBP A4 TPB2P

41 B1 NC_FW0_TPBIAS B7 TPBIAS0
41 B1 FW_P1_TPBIAS C3 TPBIAS1
41 B1 NC_FW2_TPBIAS A2 TPBIAS2

FW643_R0 B11 R0
FW643_TPCPS B10 TPCPS

TP_FW643_NAND_TREE K1 NAND_TREE NT-OUT
FW643_REXT L8 REXT
FW643_CLK24P576M_XO_R F13 XO
FW643_CLK24P576M_XI G13 XI NT-9

NOTE: NT-xx notes show NAND tree order.

TP_FW643_SE M13 SE (IPD)
TP_FW643_SM N13 SM (IPD)
TP_FW643_MODE_A J2 MODE_A (IPD) NT-18
TP_FW643_CE L13 CE (IPD)
TP_FW643_FW620_L D12 FW620*(IPU)
TP_FW643_JASI_EN D1 JASI_EN (IPD) NT-11
6 NC_FW643_AVREG A10 AVREG
TP_FW643_VBUF H13 VBUF
FW643_PU_RST_L K13 FW_RESET* (IPU) NT-8
TP_FW643_OCR10_CTL J12 OCR_CTL_V10
NC J13 OCR_CTL_V12 (Reserved)

VSS — B2 D4 D7 D9 D10 E4 E5 E9 F4 F6 F7 F8 F10 G4 G6 G7 G8 G10 H4 H6 H7 H8 H10 J4 J5 J9 J10 K4 K5 K7 K8 K9 L7 K6 K10 L12 — VREG_VSS

PCI EXPRESS PHY
PCIE_RXD0N N8 94 PCIE_FW_R2D_N
PCIE_RXD0P N7 94 PCIE_FW_R2D_P
PCIE_TXD0N N5 94 PCIE_FW_D2R_C_N
PCIE_TXD0P N6 94 PCIE_FW_D2R_C_P
REFCLKN N9 PCIE_CLK100M_FW_N IN 17 94
REFCLKP N10 PCIE_CLK100M_FW_P IN 17 94

C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N IN 17 94
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P IN 17 94
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N OUT 17 94
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P OUT 17 94
PLACEMENT_NOTE=Place C4170 close to U1800
PLACEMENT_NOTE=Place C4171 close to U1800
PLACEMENT_NOTE=Place C4175 close to U4100
PLACEMENT_NOTE=Place C4176 close to U4100

1394 PHY

TEST CONTROLLER
NT-4 (IPU) TCK M4 TP_FW643_TCK
NT-3 (IPU) TDI N2 NC_FW643_TDI 6
(IPU) TDO M1 TP_FW643_TDO
NT-1 (IPU) TMS M3 TP_FW643_TMS
NT-2 (IPU) TRST* N1 FW643_TRST_L

POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE* C2 FW643_WAKE_L OUT 8 40
REGCLT D13 FW643_REGCTL
NT-12 (IPD) VAUX_DETECT E1 FW643_VAUX_DETECT
NT-13 VAUX_DISABLE D2 TP_FW643_VAUX_ENABLE
(OD) CLKREQN L2 FW_CLKREQ_PHY_L OUT 40

SCIF
NT-16 (IPD) SCIFCLK G2 TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN G1 TP_FW643_SCIFDAIN
NT-17 SCIFDOUT H1 TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC F2 TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
NT-7 SCL N12 FW643_SCL
NT-6 SDA M11 TP_FW643_SDA

MISCELLANEOUS
CHIP RESET
NT-5 PERST* N4 FW_RESET_L IN 40

PP3V3_FW_FWPHY 6 7 39 40 41
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402

PPVP_FW_CPS 41
R4160 200K 1% 1/16W MF-LF 402
PLACE_NEAR=U4100.B10:2mm

C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
R4150 412 1% 1/16W MF-LF 402
CRITICAL
Y4150 24.576MHZ SM-3.2X2.5MM
NC 1 NC 3 2 G

R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009
PAGE TITLE
FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 41 OF 132
SHEET 39 OF 101

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW FET

I(max) = 1.7A (85C)

PP3V3_S0 → C4201 1UF 10% 6.3V CERM 402 → U4201 TPS22924 CSP (CRITICAL) → PP3V3_FW_FWPHY

FW_PWR_EN → U4201 ON

1.05V FW FET

PP1V05_S0 → C4202 1UF 10% 6.3V CERM 402 → U4202 TPS22924 CSP (CRITICAL) → PP1V0_FW_FWPHY

FW_CLKREQ_L → Q4261 SSM6N15FEAPE SOT563 → FW_CLKREQ_PHY_L

FireWire Port Power Switch

PPBUS_G3H

R4262 10K 5% 1/16W MF-LF 402 → FWPWR_EN_TRI

R4263 10 5% 1/16W MF-LF 402 → FWPWR_EN_TRI_R

Q4262 BSS8402DW SOT-363 (SYM-VER1)

R4260 470K 5% 1/16W MF-LF 402

C4260 0.1UF 10% 25V X5R 402

Q4260 NDS9407 SOI-HF

PPBUS_FW_FWPWRSW_F → F4260 1.1A-24V MINISMDC110H24 → PPBUS_FW_FWPWRSW_D

PPBUS_FW_FWPWRSW_D → D4260 CRS08-1.5A-30V → PPVP_FW

R4261 330K 5% 1/16W MF-LF 402

Q4261 SSM6N15FEAPE SOT563

NOSTUFF C4261 0.1UF 10% 25V X5R 402

Late-VG Protection

PP3V3_S0 → C4200 0.1UF 10% 25V X5R 402 (PLACE_NEAR=U4200.1:2mm)

U4200 TPD4S1394 LLP

FW_PORT1_TPB_P
FW_PORT1_TPB_N
FW_PORT1_TPA_P
FW_PORT1_TPA_N

TP_FW_LATEVG_VCLMP

FWPWR_EN → R4201 100K 5% 1/16W MF-LF 402

PP1V05_S0

R4275 1K 5% 1/16W MF-LF 402 → FW_PWR_EN_L

R4270 330K 5% 1/16W MF-LF 402 → FW_DET_MIRROR

R4271 56K 5% 1/16W MF-LF 402 → FW_PLUG_DET

Q4270 BC847CDXV6TXG SOT563

C4270 0.1UF 10% 25V X5R 402

FW_PLUG_DET_L

Q4275 DMB53D0UV SOT-563

FW_P1_TPBIAS_R

R4272 1K 5% 1/16W MF-LF 402 (PLACE_NEAR=C4360.1:2mm)

R4273 12K 5% 1/16W MF-LF 402

FW_DET_EMIT

FW_PWR_EN

FW_P1_TPBIAS

PP3V3_FW_FWPHY

R4277 10K 5% 1/16W MF-LF 402

R4276 100K 5% 1/16W MF-LF 402

FW_WAKE

NOSTUFF C4276 0.1UF 10% 10V X5R 402

Q4276 DMB53D0UV SOT-563

FW643_WAKE_L

FW_PLUG_DET_L

PP3V3_S0 → R4281 100K 5% 1/16W MF-LF 402

PP1V0_FW_FWPHY → R4280 10K 5% 1/16W MF-LF 402

P1V0_FW_RC

C4281 1UF 10% 6.3V CERM 402

Q4299 DMB53D0UV SOT-563

P1V0_RESET_GATE

R4283 10K 5% 1/16W MF-LF 402 → PLT_RESET_L

FW_RESET_L

PP1V05_FW PGOOD/FW_RESET_L

SYNC_MASTER=K19_MLB	SYNC_DATE=05/29/2009
PAGE TITLE	FireWire Port Power
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	BRANCH <BRANCH>
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	SHEET 40 OF 101

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

41 40 39 7 6 PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402

R4380 10K 1% 1/16W MF-LF 402

41 39 FWPHY_DS0 = FWPHY_DS0 39 41 (MAKE_BASE=TRUE)

41 39 FWPHY_DS2 = FWPHY_DS2 39 41 (MAKE_BASE=TRUE)

41 39 FWPHY_DS1 = FWPHY_DS1 39 41 (MAKE_BASE=TRUE)

R4381 10K 1% 1/16W MF-LF 402

41 39 NC_FW0_TPBIAS = NC_FW0_TPBIAS MAKE_BASE=TRUE 39 41

41 39 6 NC_FW2_TPBIAS = NC_FW2_TPBIAS MAKE_BASE=TRUE 6 39 41

96 41 39 NC_FW0_TPAN = NC_FW0_TPAN MAKE_BASE=TRUE 39 41 96

96 41 39 6 NC_FW0_TPAP = NC_FW0_TPAP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPAN = NC_FW2_TPAN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPAP = NC_FW2_TPAP MAKE_BASE=TRUE 6 39 41

96 41 39 6 NC_FW0_TPBN = NC_FW0_TPBN MAKE_BASE=TRUE 6 39 41 96

96 41 39 6 NC_FW0_TPBP = NC_FW0_TPBP MAKE_BASE=TRUE 6 39 41 96

41 39 6 NC_FW2_TPBN = NC_FW2_TPBN MAKE_BASE=TRUE 6 39 41

41 39 6 NC_FW2_TPBP = NC_FW2_TPBP MAKE_BASE=TRUE 6 39 41

Termination

Place close to FireWire PHY

40 39 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.A5:2mm

PLACE_NEAR=U4100.B5:2mm

96 41 40 39 FW_PORT1_TPA_P = FW_PORT1_TPA_P 39 40 41 96 (MAKE_BASE=TRUE)

96 41 40 39 FW_PORT1_TPA_N = FW_PORT1_TPA_N 39 40 41 96 (MAKE_BASE=TRUE)

96 41 40 39 FW_PORT1_TPB_P = FW_PORT1_TPB_P 39 40 41 96 (MAKE_BASE=TRUE)

96 41 40 39 FW_PORT1_TPB_N = FW_PORT1_TPB_N 39 40 41 96 (MAKE_BASE=TRUE)

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

PLACE_NEAR=U4100.B6:4mm

PLACE_NEAR=U4100.A6:4mm

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

41 40 7 6 PPVP_FW

Q4300 BSS8402DW SOT-363 (SYM-VER1)

R4311 470K 5% 1/16W MF-LF 402

41 39 PPVP_FW_CPS = PPVP_FW_CPS 39 41 (MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=12.6V)

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

Cable Power

41 40 7 6 PPVP_FW

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F (MIN_LINE_WIDTH=0.2 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=33V)

C4314 0.01UF 10% 50V X7R 402

96 41 40 39 FW_PORT1_TPB_N

96 41 40 39 FW_PORT1_TPB_P

96 41 40 39 FW_PORT1_TPA_N

96 41 40 39 FW_PORT1_TPA_P

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

CRITICAL J4310 1394B-M97 F-RT-TH

OUTPUT: TPB- (TPB(R)), TPB+ (TPB<R>), VP, VG, NC, VP

INPUT: TPA- (TPA<R>), TPA+ (TPA(R)), VG, VP

CHASSIS GND

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

PORT 1
BILINGUAL

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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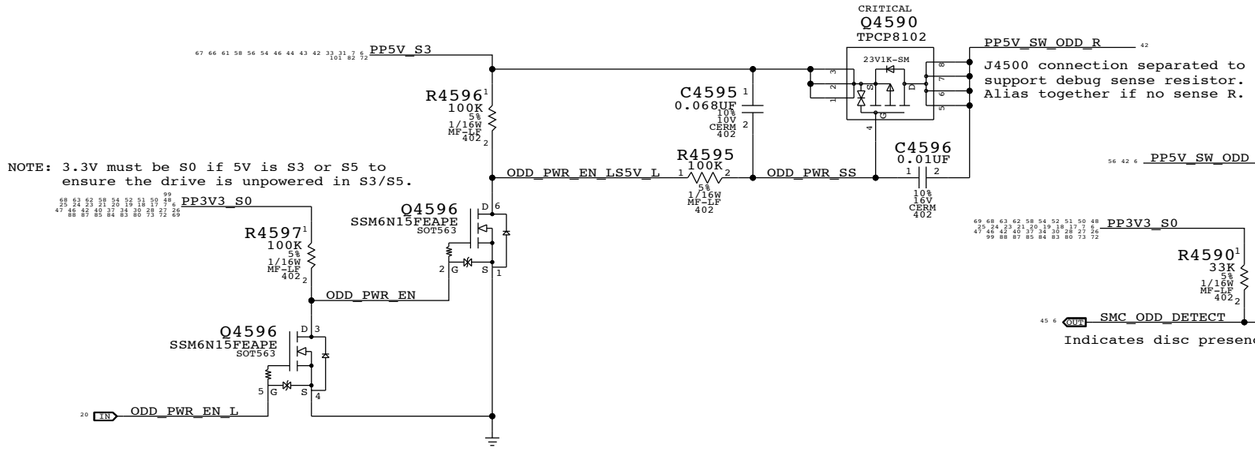
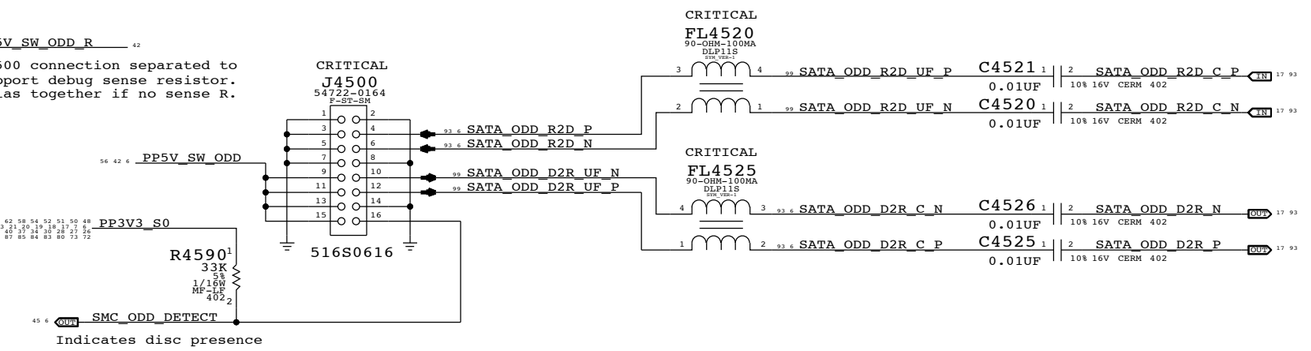
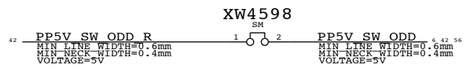
ODD Power Control

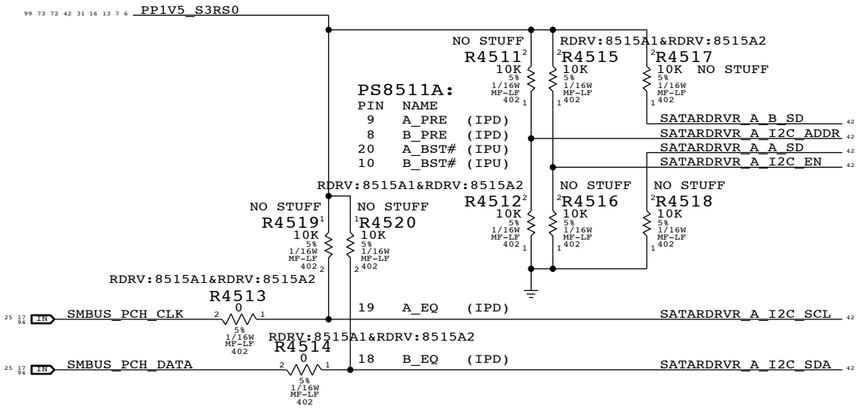




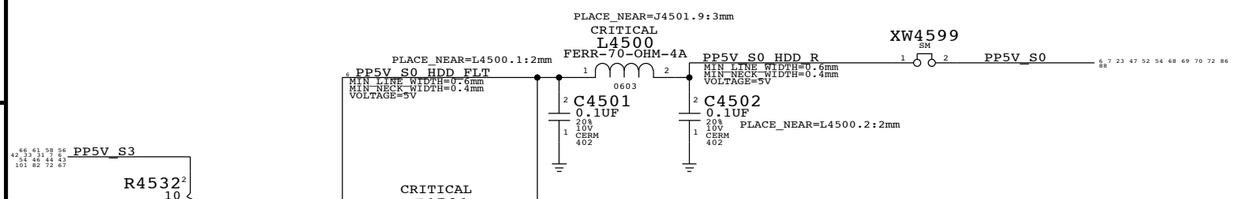
SATA ODD Connector



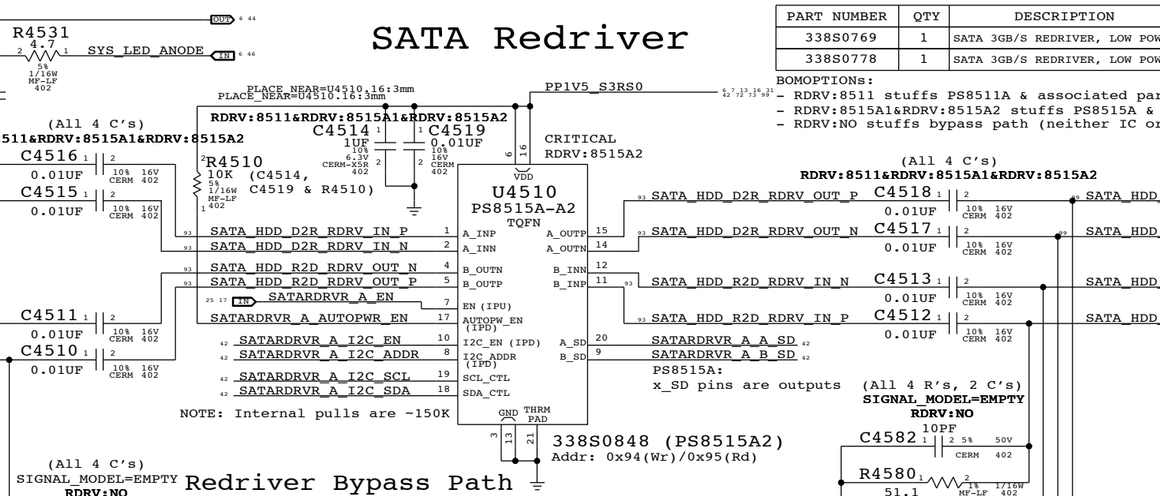
PS8511A / PS8515A Straps



SATA HDD/IR/SIL Connector



SATA Redriver



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8515A1

BOMOPTIONs:
- RDRV:8511 stuffs PS8511A & associated parts (STRAPS TBD!!!)
- RDRV:8515A1&RDRV:8515A2 stuffs PS8515A & associated parts
- RDRV:NO stuffs bypass path (neither IC or associated parts stuffed)

SYNC MASTER=T27 REF SYNC DATE=10/01/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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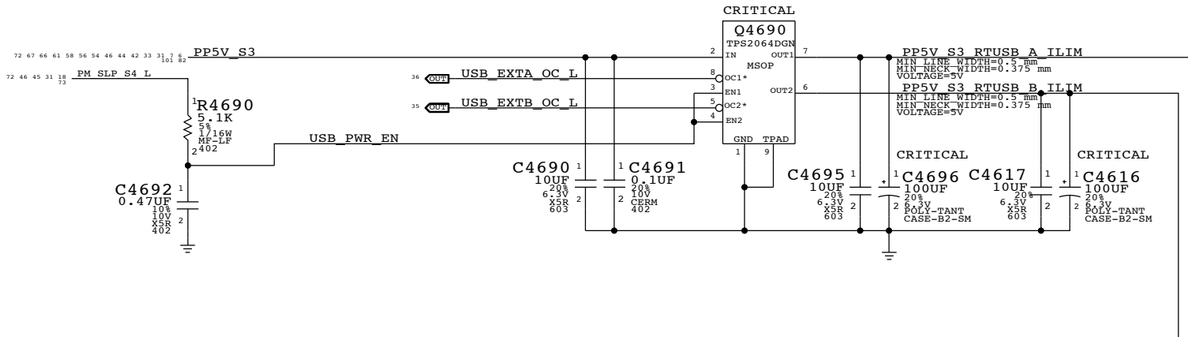
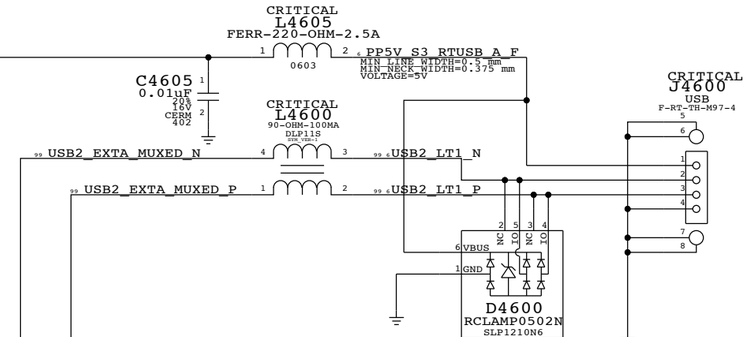
Port Power Switch

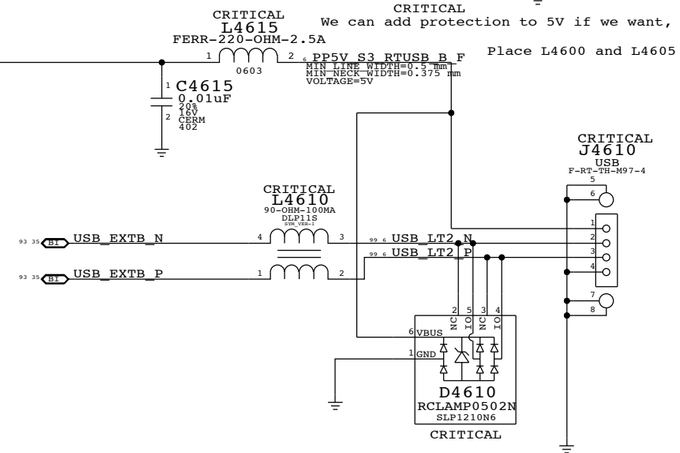


Left USB Port A

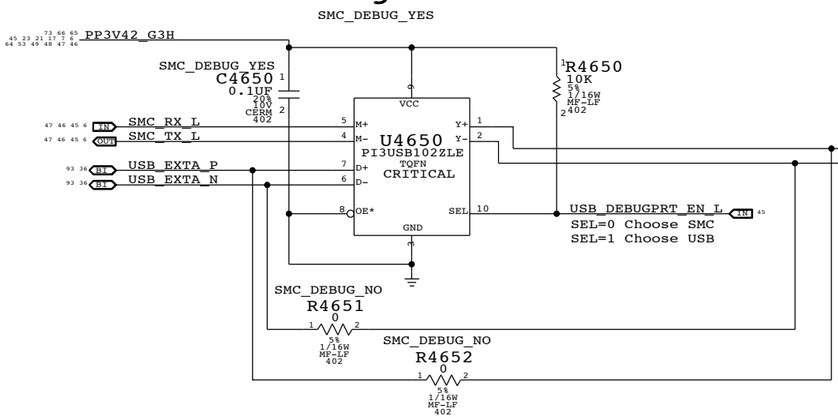


We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin



USB/SMC Debug Mux



Left USB Port B

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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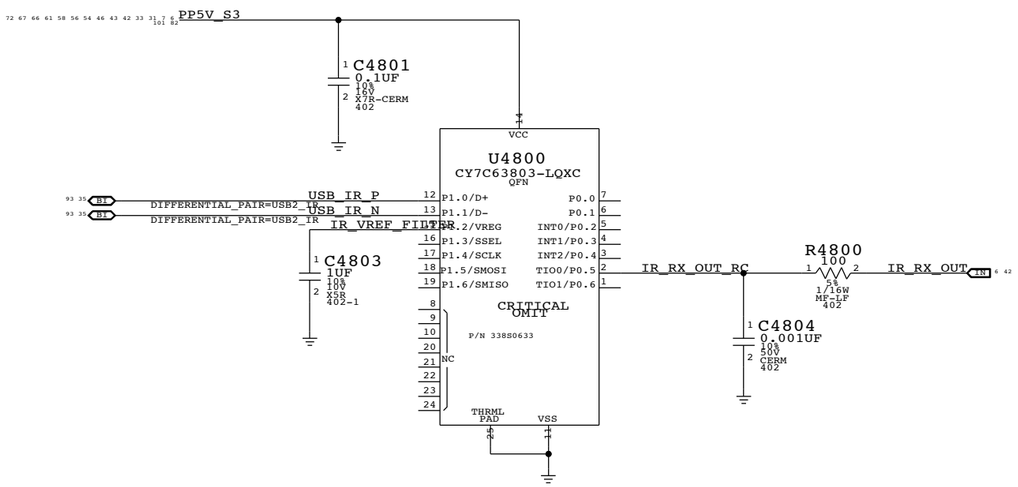
IR SUPPORT



SYNC MASTER=K19 MLB	SYNC DATE=05/29/2009
PAGE TITLE: Front Flex Support	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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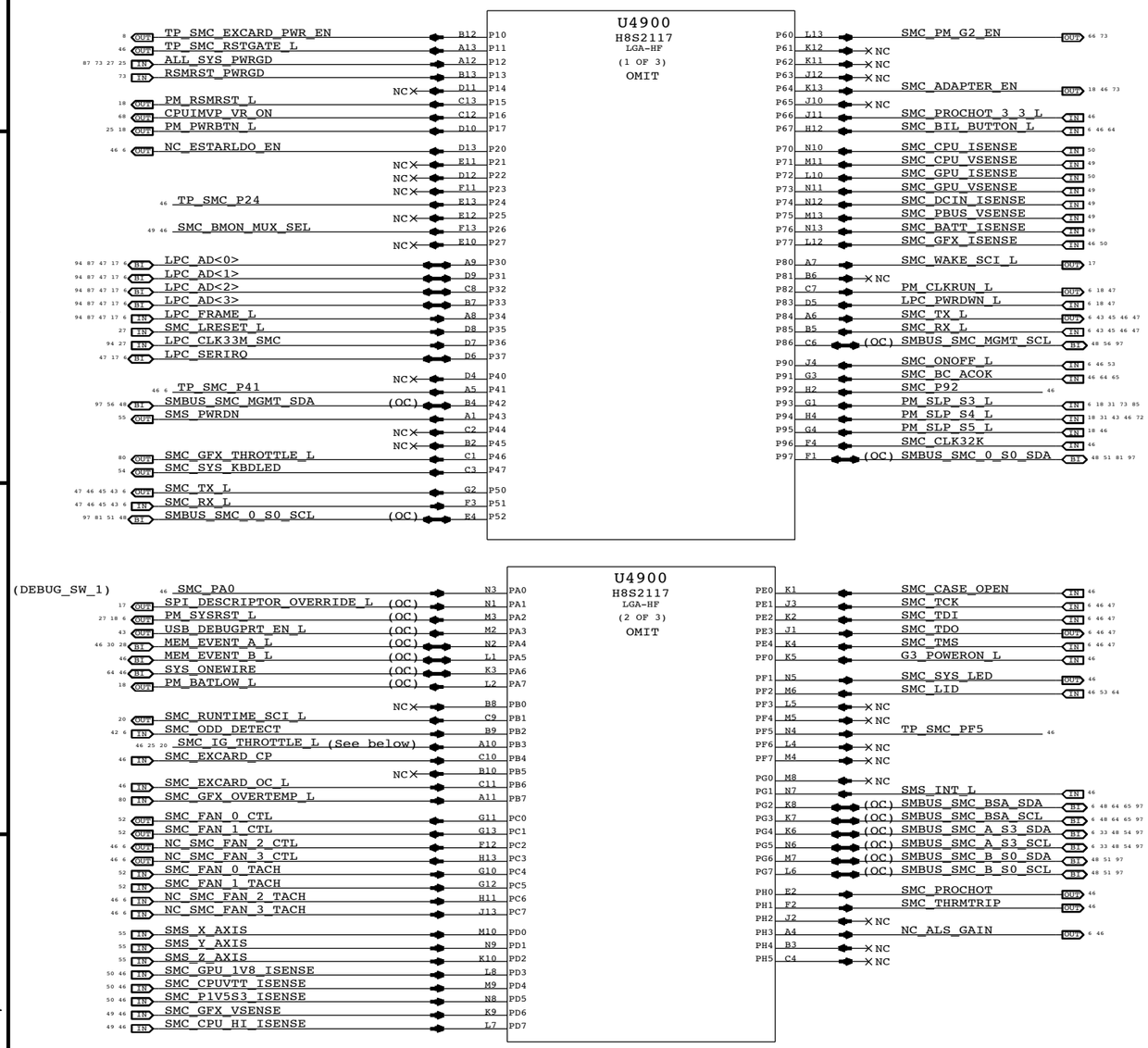
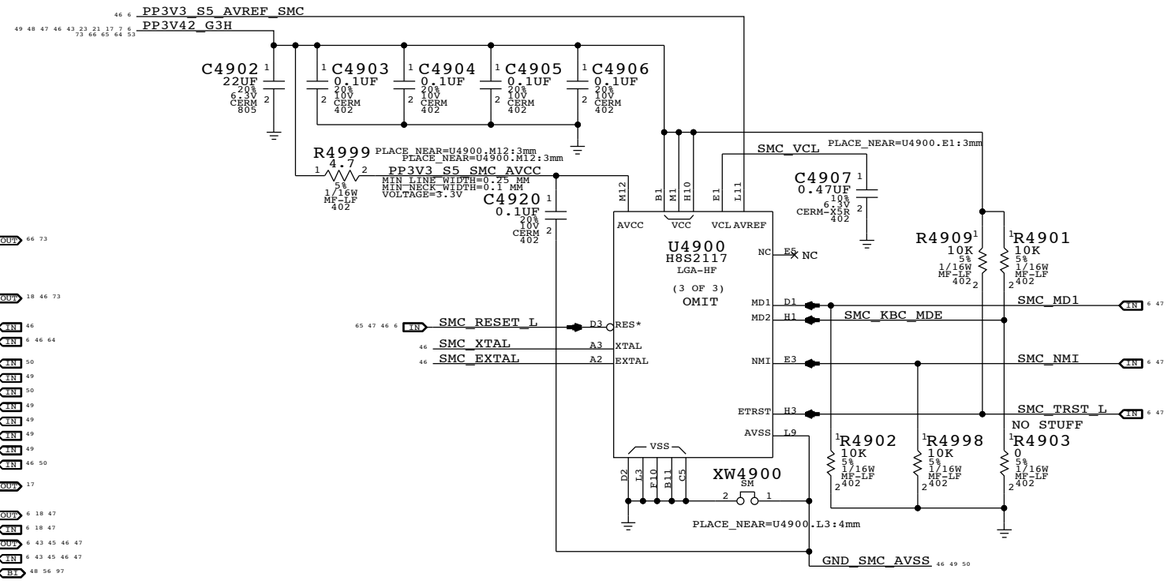
	PAGE: 48 OF 132
	SHEET: 44 OF 101

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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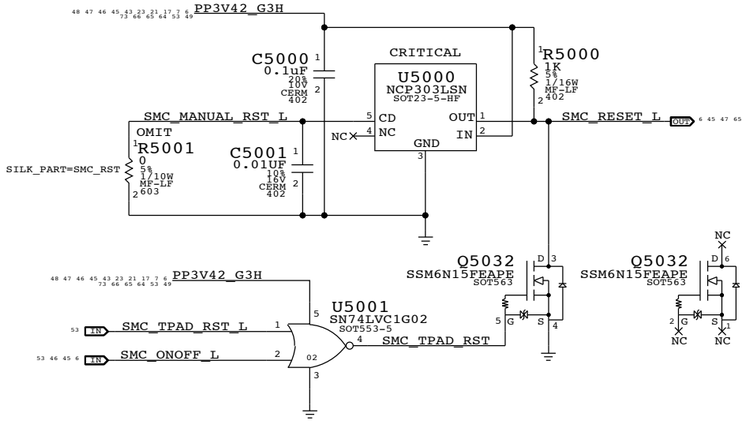
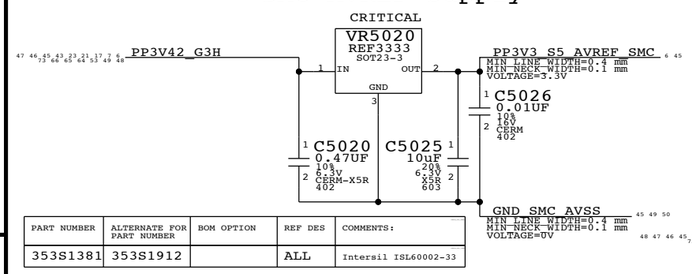
SMC Reset "Button" / Brownout Detect

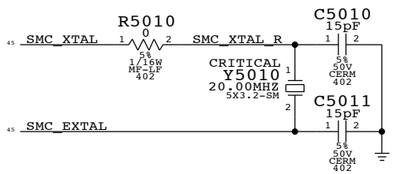


SMC AVREF Supply



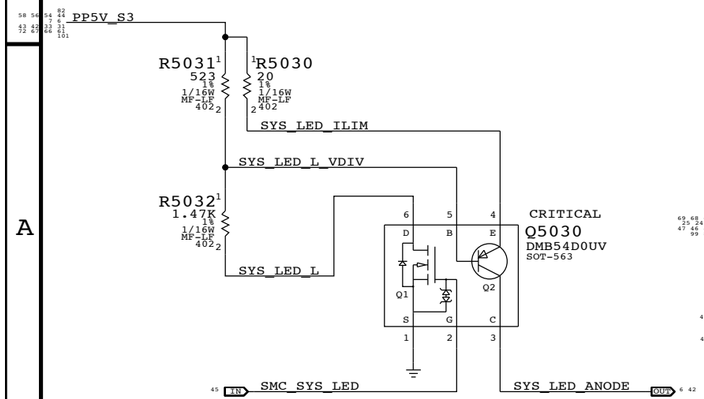
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

SMC Crystal Circuit

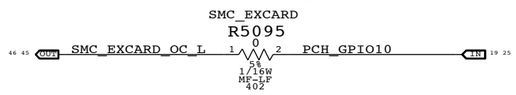


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0350	1	OSC,XTAL,32.768KHZ,LF,HF	U5010	CRITICAL	SMC_OSC_YES

System (Sleep) LED Circuit

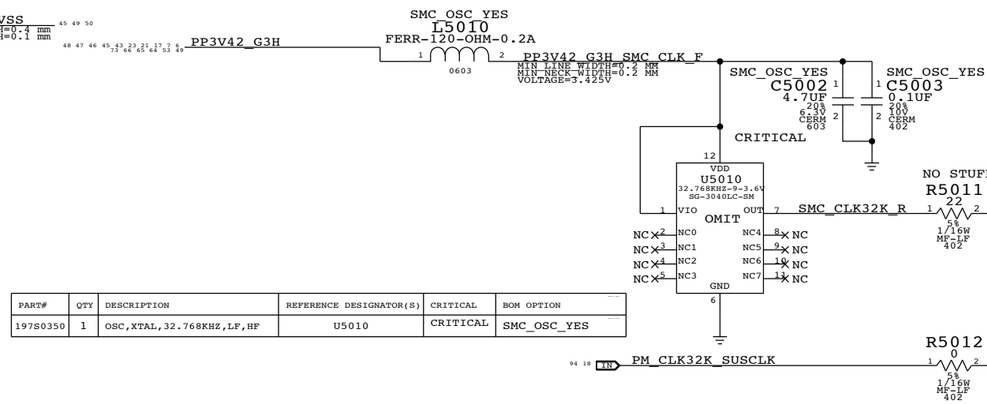


SMC_EXCARD

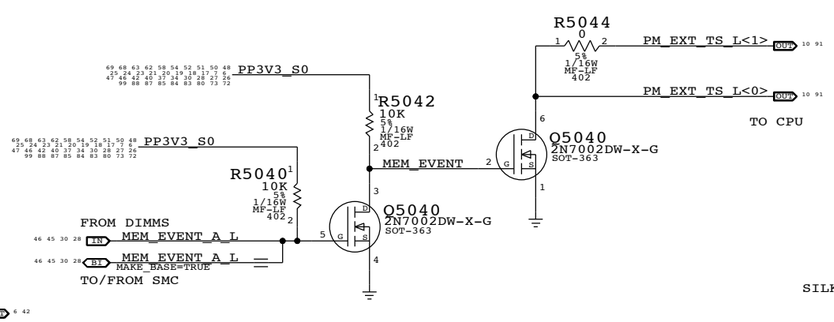


SMC G3Hot 32kHz Oscillator

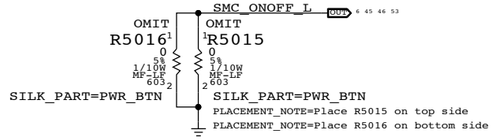
To support timed wake-up events in G3Hot



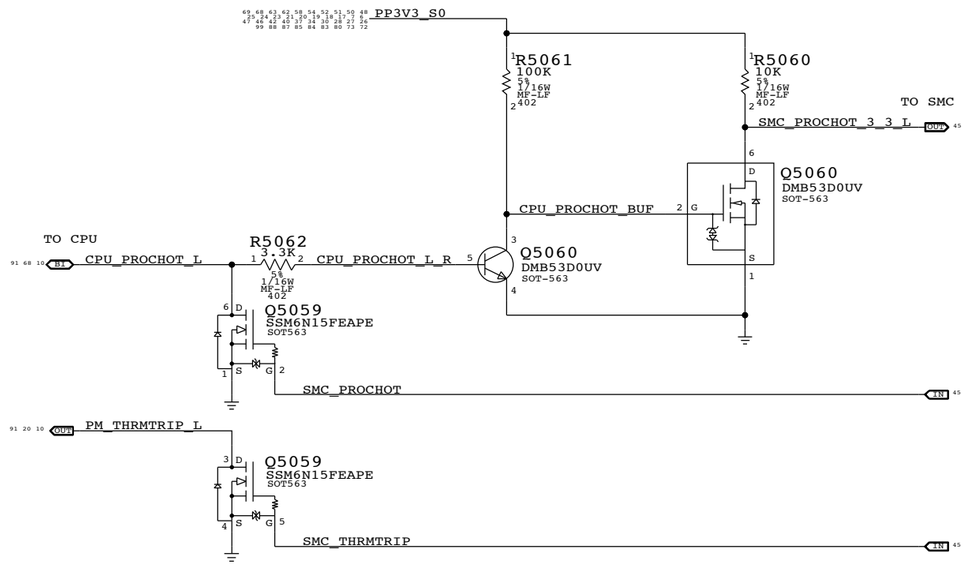
CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting



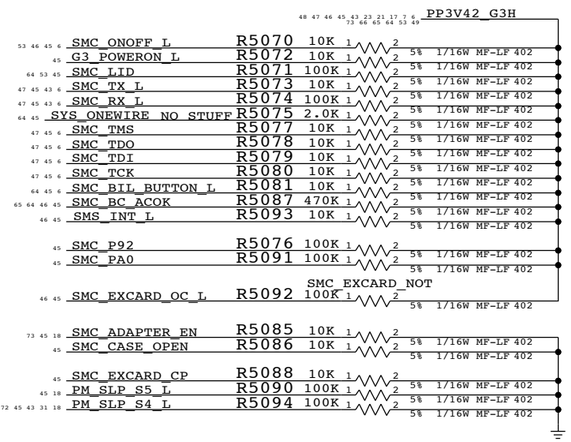
Debug Power "Buttons"



SMC FSB to 3.3V Level Shifting



SMC_EXCARD_NOT



SMC_MAKE_BASE=TRUE

NC_SMC_FAN_2_CTL	=	NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH	=	NC_SMC_FAN_2_TACH
NC_SMC_FAN_3_CTL	=	NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH	=	NC_SMC_FAN_3_TACH
NC_ESTARLDO_EN	=	NC_ESTARLDO_EN
NC_ALS_GAIN	=	NC_ALS_GAIN
TP_SMC_RSTGATE_L	=	TP_SMC_RSTGATE_L
SMC_BC_ACOK	=	SMC_BC_ACOK
SMC_BMON_MUX_SEL	=	SMC_BMON_MUX_SEL
SMC_IG_THROTTLE_L	=	SMC_IG_THROTTLE_L
SMS_INT_L	=	SMS_INT_L
SMC_GFX_VSENSE	=	SMC_GFX_VSENSE
SMC_CPU_HI_ISENSE	=	SMC_CPU_HI_ISENSE
SMC_CPUVTT_ISENSE	=	SMC_CPUVTT_ISENSE
SMC_P1V5S3_ISENSE	=	SMC_P1V5S3_ISENSE
SMC_GFX_ISENSE	=	SMC_GFX_ISENSE
SMC_GPU_1V8_ISENSE	=	SMC_GPU_1V8_ISENSE
TP_SMC_P24	=	TP_SMC_P24
TP_SMC_P41	=	TP_SMC_P41
TP_SMC_PF5	=	TP_SMC_PF5

SYNC_MASTER=K18_SENSORS		SYNC_DATE=06/29/2009
PAGE TITLE	SMC Support	
Apple Inc.	DRAWING NUMBER <SCH_NUM>	SIZE D
	REVISION <E4LABEL>	
	BRANCH <BRANCH>	
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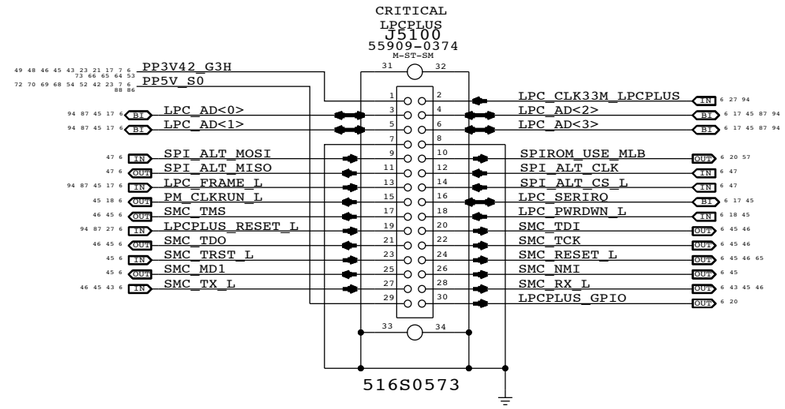
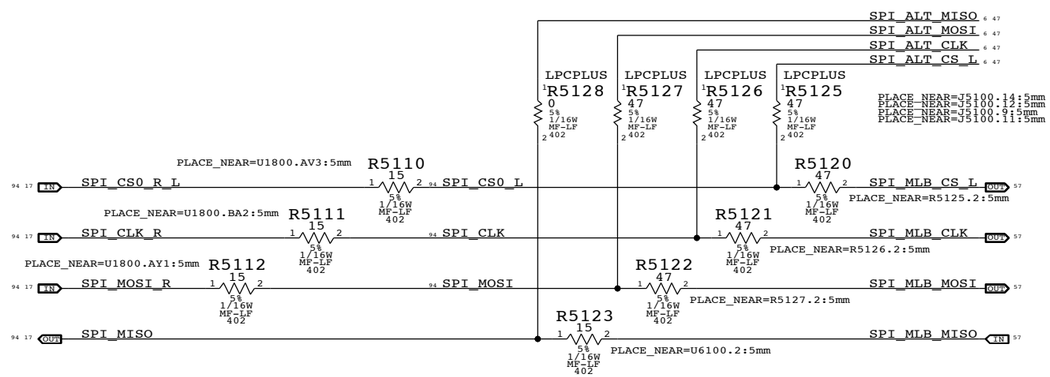
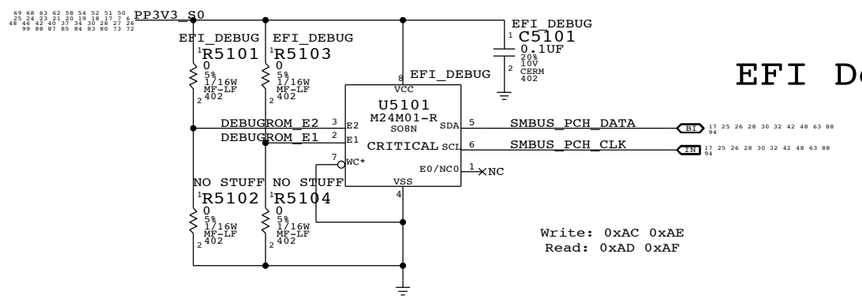
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=K17_MLB SYNC_DATE=06/23/2009

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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PCH SMBus "0" Connections

PP3V3_S0

R5200 1K 5% 1/16W MF-LF 402
R5201 1K 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)

- SMBUS_PCH_CLK — MAKE_BASE=TRUE
- SMBUS_PCH_DATA — MAKE_BASE=TRUE

VRef DACs
U2900
(Write: 0x98 Read: 0x99)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U2901
(Write: 0x30 Read: 0x31)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

EFI Debug Serial
U5101
(Write: 0xAC/AE Read: 0xAD/AF)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J2600 & J2650
(MASTER)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "A"
J2900
(Write: 0xA0 Read: 0xA1)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

SO-DIMM "B"
J3100
(Write: 0xA4 Read: 0xA5)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

CK505 (Clock)
U2700
(Write: 0xD2 Read: 0xD3)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U9701
(WRITE: 0x58 READ: 0x59)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Mikey
U6800
(Write: 0x72 Read: 0x73)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

HDD Redriver Control A
U4510
(Write: 0x94 Read: 0x95)

- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

R5210 8.2K 5% 1/16W MF-LF 402
R5211 8.2K 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(MASTER)

- SML_PCH_0_CLK — MAKE_BASE=TRUE
- SML_PCH_0_DATA — MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5220 8.2K 5% 1/16W MF-LF 402
NO STUFF
R5221 8.2K 5% 1/16W MF-LF 402
R5223 0 5% 1/16W MF-LF 402
R5222 0 5% 1/16W MF-LF 402

Ibex Peak-M
U1800
(Write: 0x90 Read: 0x91)

- SML_PCH_1_CLK — MAKE_BASE=TRUE
- SML_PCH_1_DATA — MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_0_S0_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_0_S0_SDA — MAKE_BASE=TRUE

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)

- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

GPU Temp (Int)
GT216: U8000
(Write: 0x9E Read: 0x9F)

- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5270 1K 5% 1/16W MF-LF 402
R5271 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_A_S3_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_A_S3_SDA — MAKE_BASE=TRUE

Trackpad
J5800
(Write: 0x90 Read: 0x91)

- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

ALS
J3401
(Write: 0x72 Read: 0x73)

- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

SMC "B" SMBus Connections

PP3V3_S0

R5260 4.7K 5% 1/16W MF-LF 402
R5261 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_B_S0_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_B_S0_SDA — MAKE_BASE=TRUE

CPU Temp
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)

- SMBUS_SMC_B_S0_SCL
- SMBUS_SMC_B_S0_SDA

SMC "Battery A" SMBus Connections

PP3V42_G3H

R5280 1K 5% 1/16W MF-LF 402
R5281 1K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_BSA_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_BSA_SDA — MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)

- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery
J6955
(See Table)

- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

PP3V3_S3

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

SMC
U4900
(MASTER)

- SMBUS_SMC_MGMT_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_MGMT_SDA — MAKE_BASE=TRUE

Sensor ADC A
U5930
(Write: 0x10 Read: 0x11)

- SMBUS_SMC_MGMT_SCL
- SMBUS_SMC_MGMT_SDA

SYNC_MASTER=K18 SENSORS SYNC_DATE=06/18/2009

PAGE TITLE: K18 SMBus Connections

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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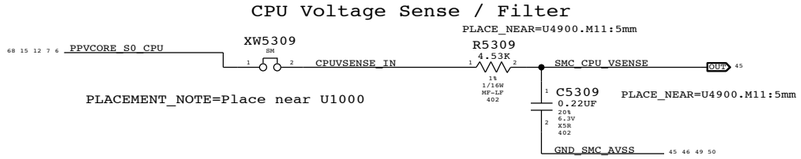
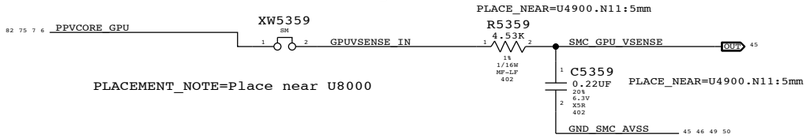
CPU Voltage Sense / Filter



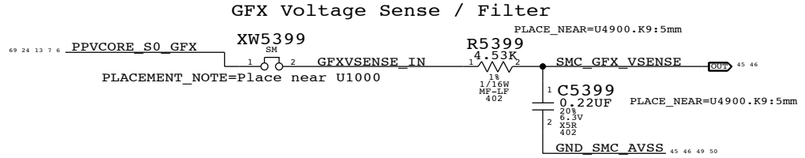
PLACEMENT_NOTE=Place near U1000

GPU Voltage Sense / Filter



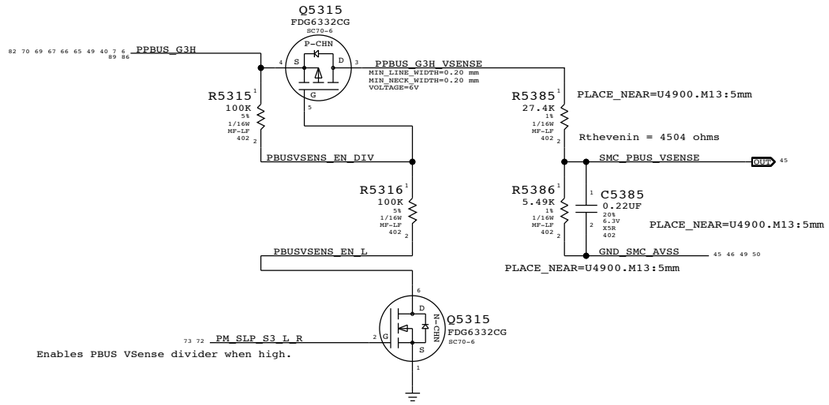
PLACEMENT_NOTE=Place near U8000

GFX Voltage Sense / Filter



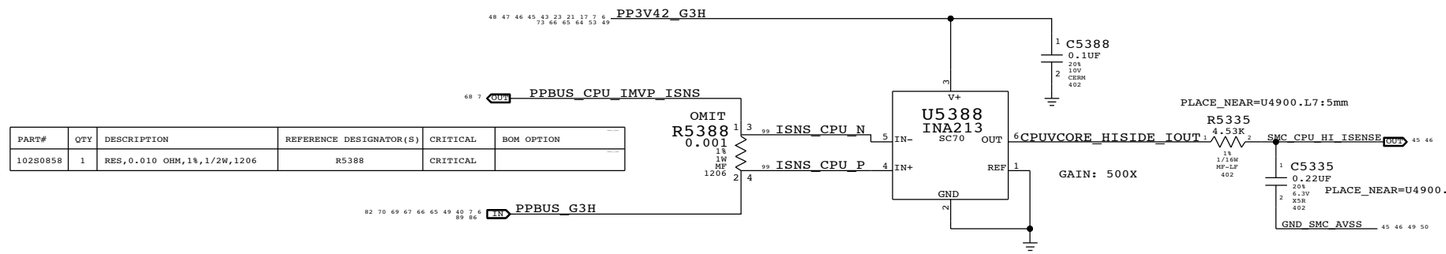
PLACEMENT_NOTE=Place near U1000

PBUS Voltage Sense & Filter



Enables PBUS VSense divider when high.

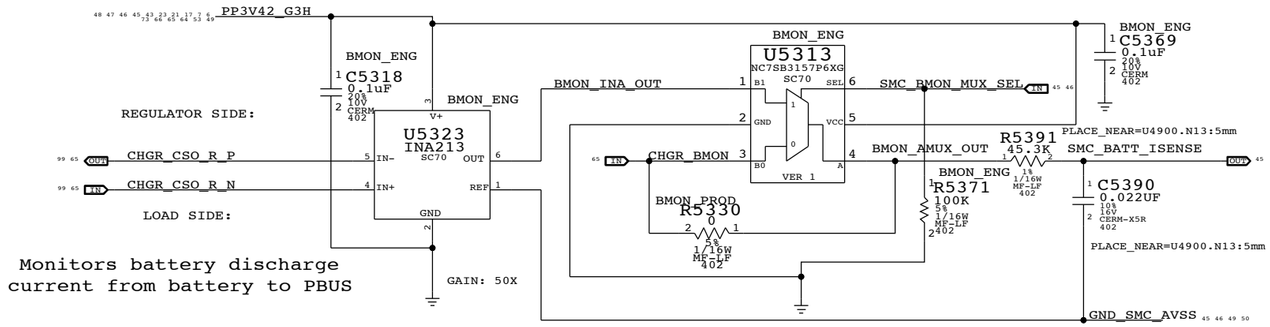
CPU VCore High Side Current Sensor



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
102S0858	1	RES,0.010 OHM,1%,1/2W,1206	R5388	CRITICAL	

EDP for PPVIN_S5_CPU_IMVP_ISNS_R = 5.867 amps for K18.

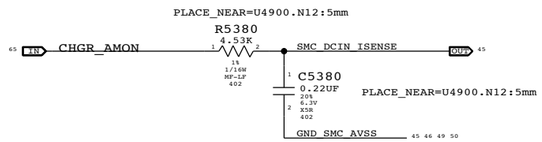
BMON Current Sense - Entire circuit must be near SMC (U4900)



Monitors battery discharge current from battery to PBUS

U5303 only senses current up to 6.6A

DCIN Current Sense Filter



SYNC MASTER=K18 SENSORS	SYNC DATE=06/29/2009
PAGE TITLE: Current & Voltage Sensing	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
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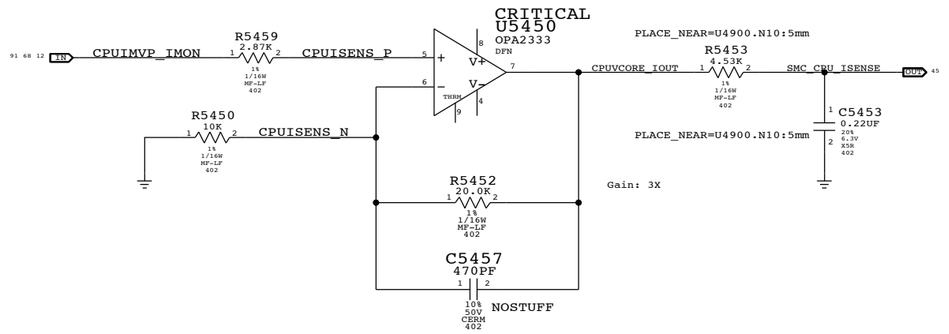
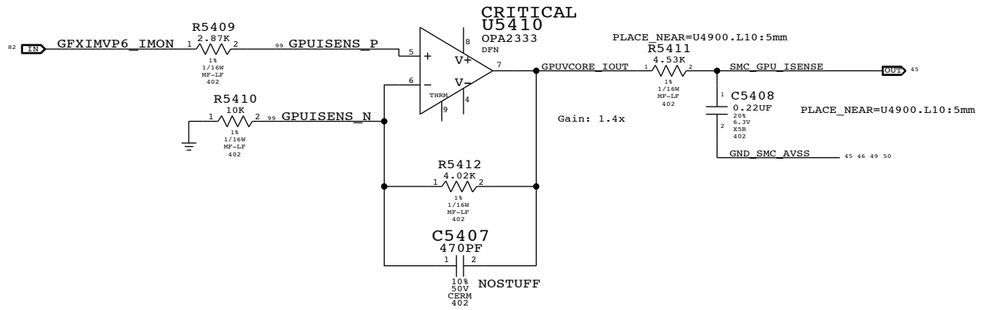
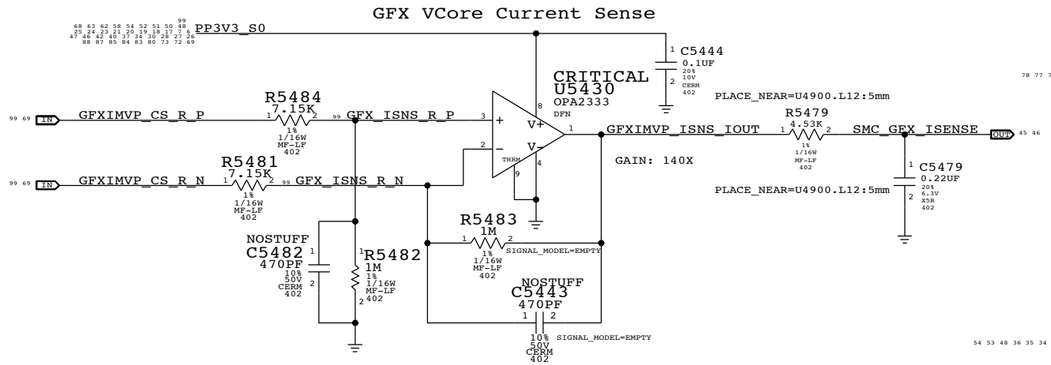
CPU VCore Load Side Current Sense / Filter



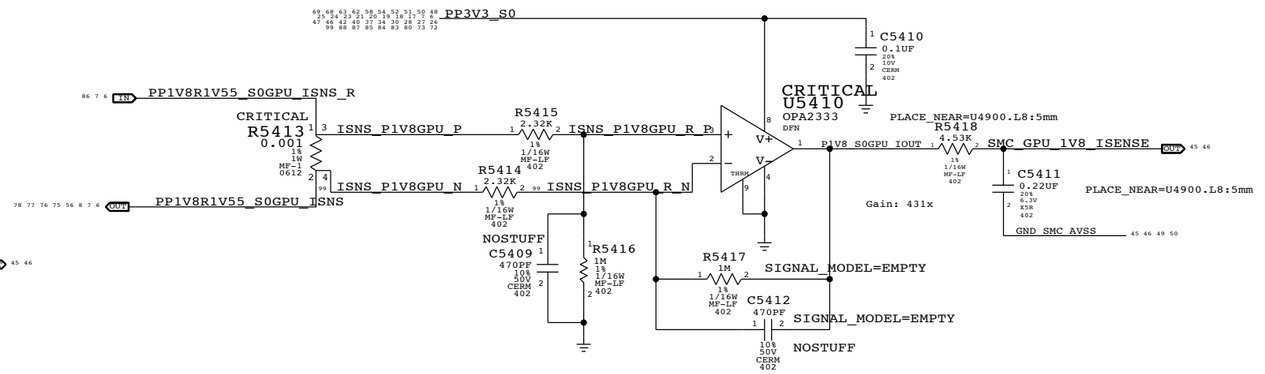
GPU VCore Current Sense



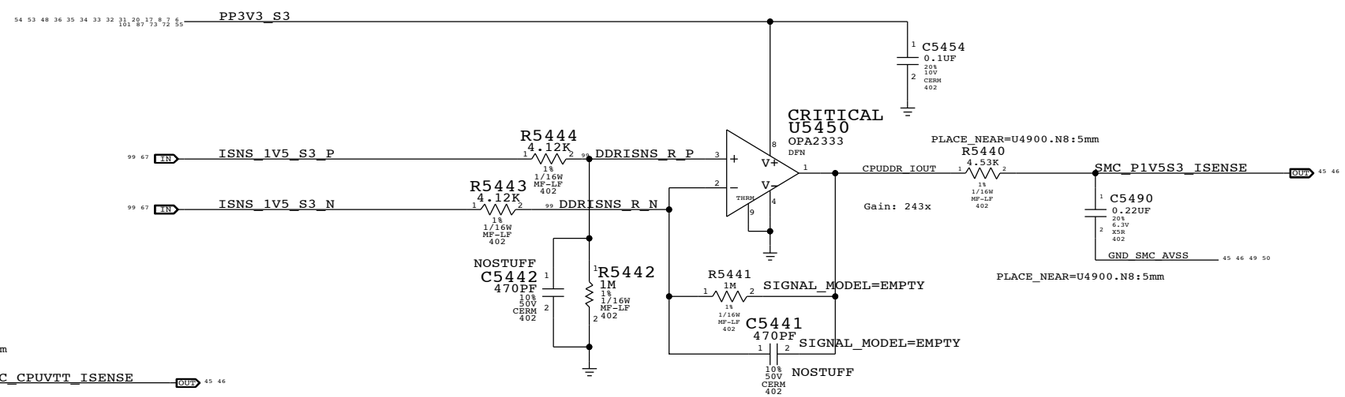
GFX VCore Current Sense



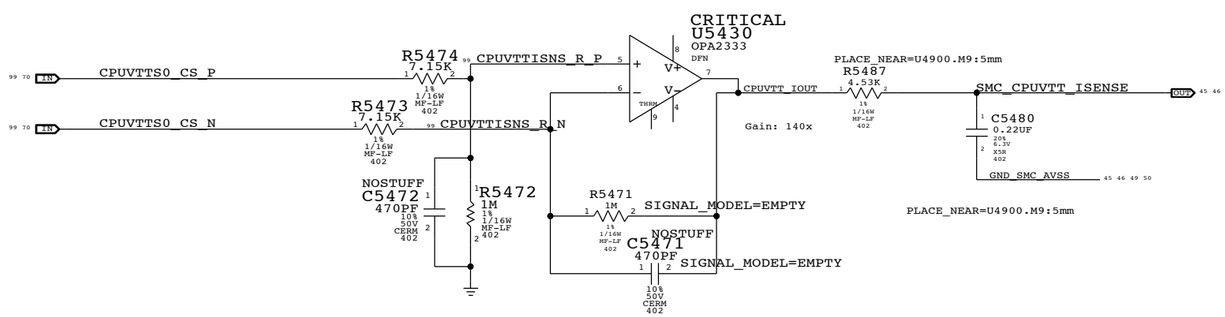
1.8V FB Current Sense



CPU & MEM 1.5V S3 (DDR) Current Sense



CPUVTT 1.05V Current Sense



SYNC_MASTER=K18_SENSORS SYNC_DATE=07/02/2009

PAGE TITLE

Current Sensing

Apple Inc.

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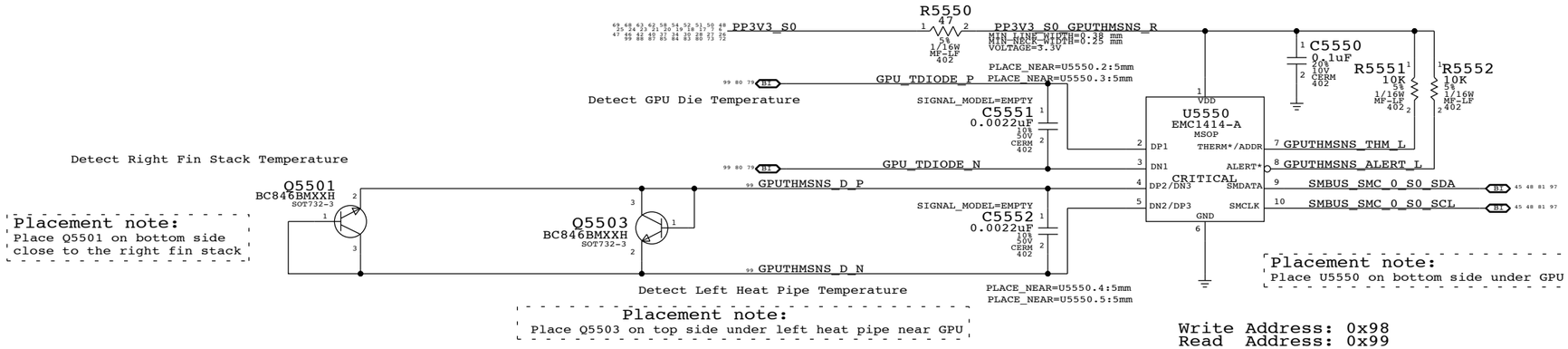
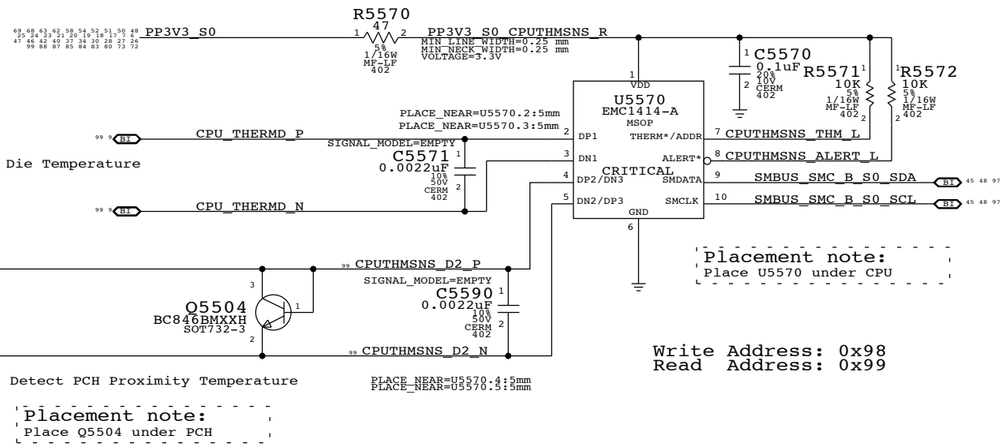
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



Write Address: 0x98
Read Address: 0x99

CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Write Address: 0x98
Read Address: 0x99

Note: EMC1414 can perform Beta
Compensation for External Diode 1 only

SYNC_MASTER=K18_SENSORS SYNC_DATE=06/18/2009

PAGE TITLE

Thermal Sensors

Apple Inc.

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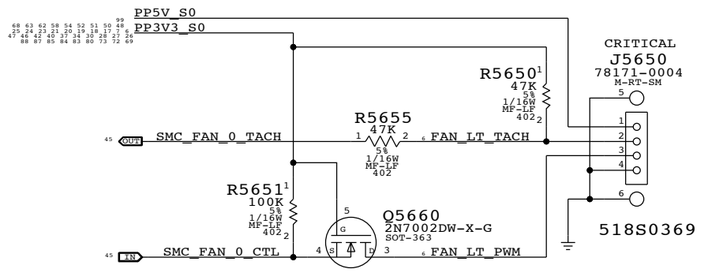
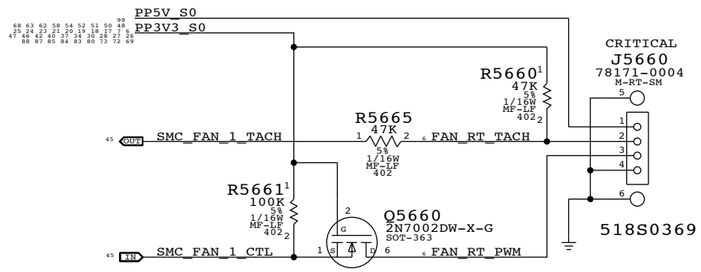
Left Fan



Right Fan



SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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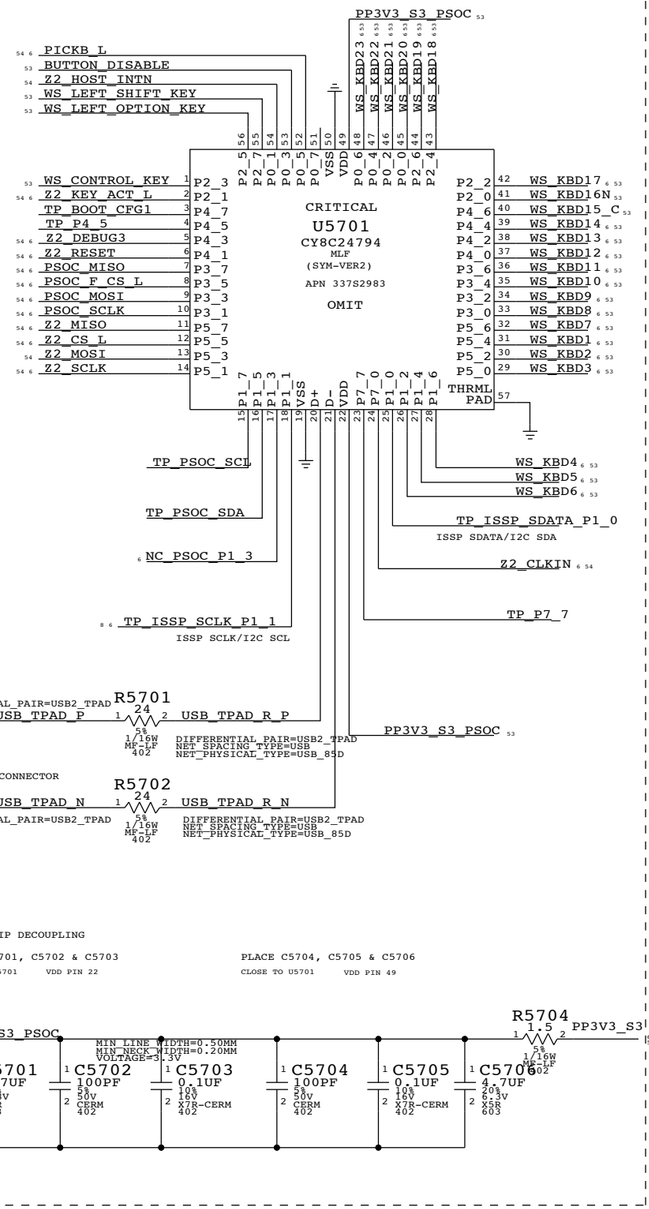
PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



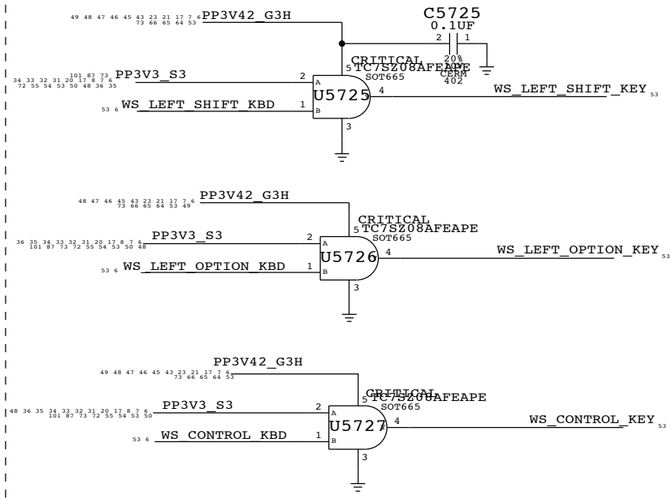
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

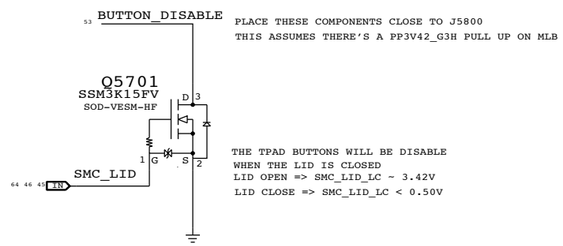
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

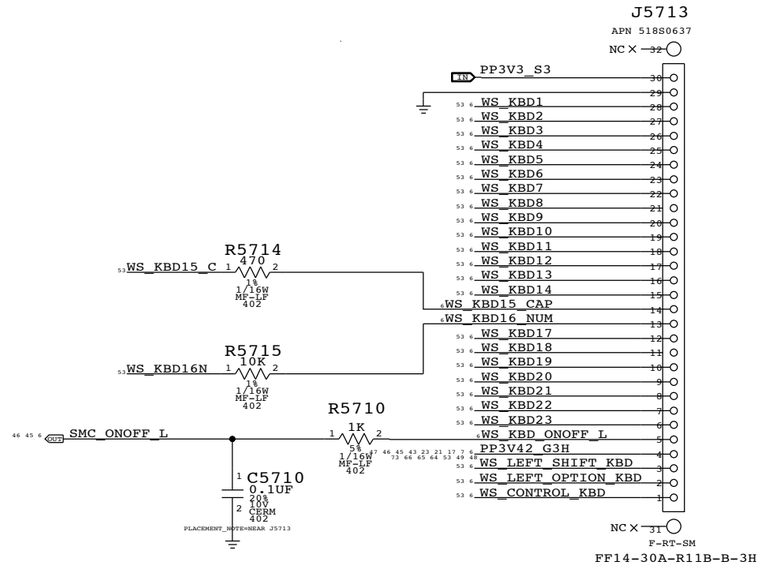
ISOLATION CIRCUIT



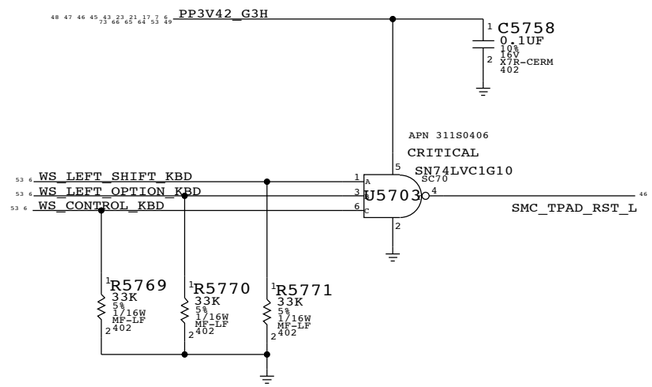
TPAD BUTTONS DISABLE



KEYBOARD CONNECTOR



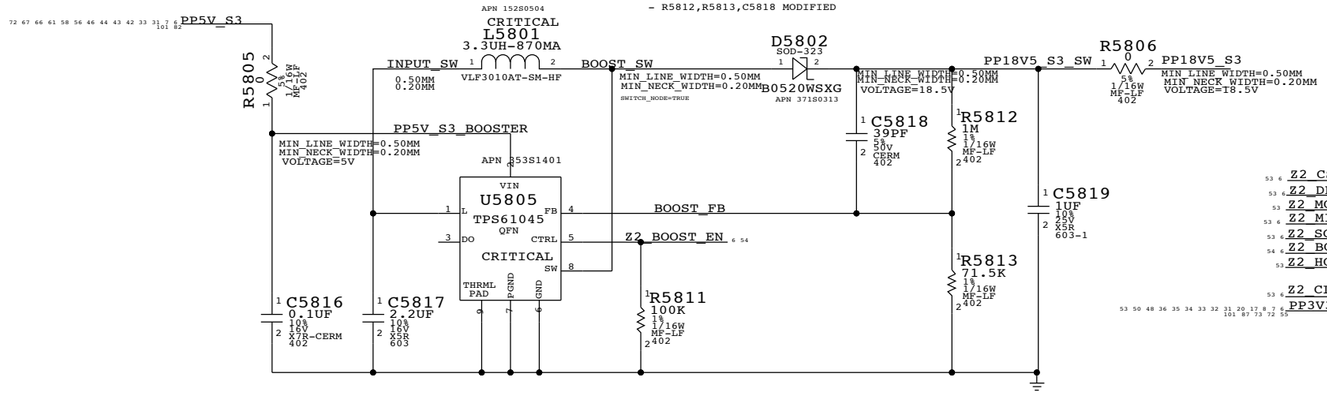
SMC_MANUAL_RESET LOGIC



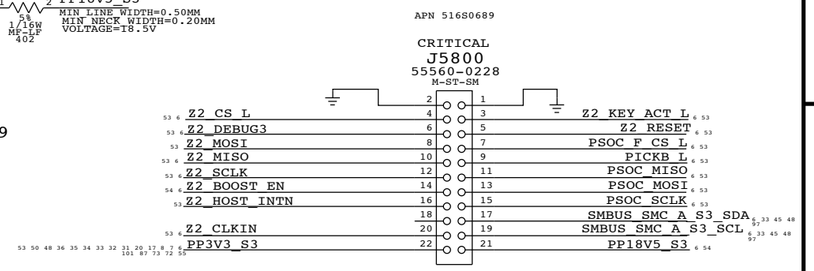
SYNC MASTER=K19 MLB	SYNC DATE=05/29/2009
PAGE TITLE	WELLSPRING 1
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 57 OF 132
	SHEET 53 OF 101

BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



Keyboard LED Driver

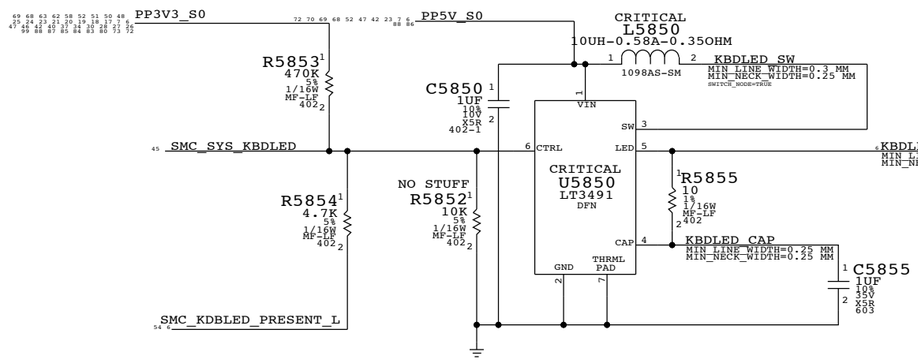
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

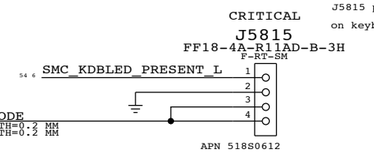
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT



KBD BACKLIGHT CONNECTOR

J5815 pin 1 is grounded on keyboard backlight flex



SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

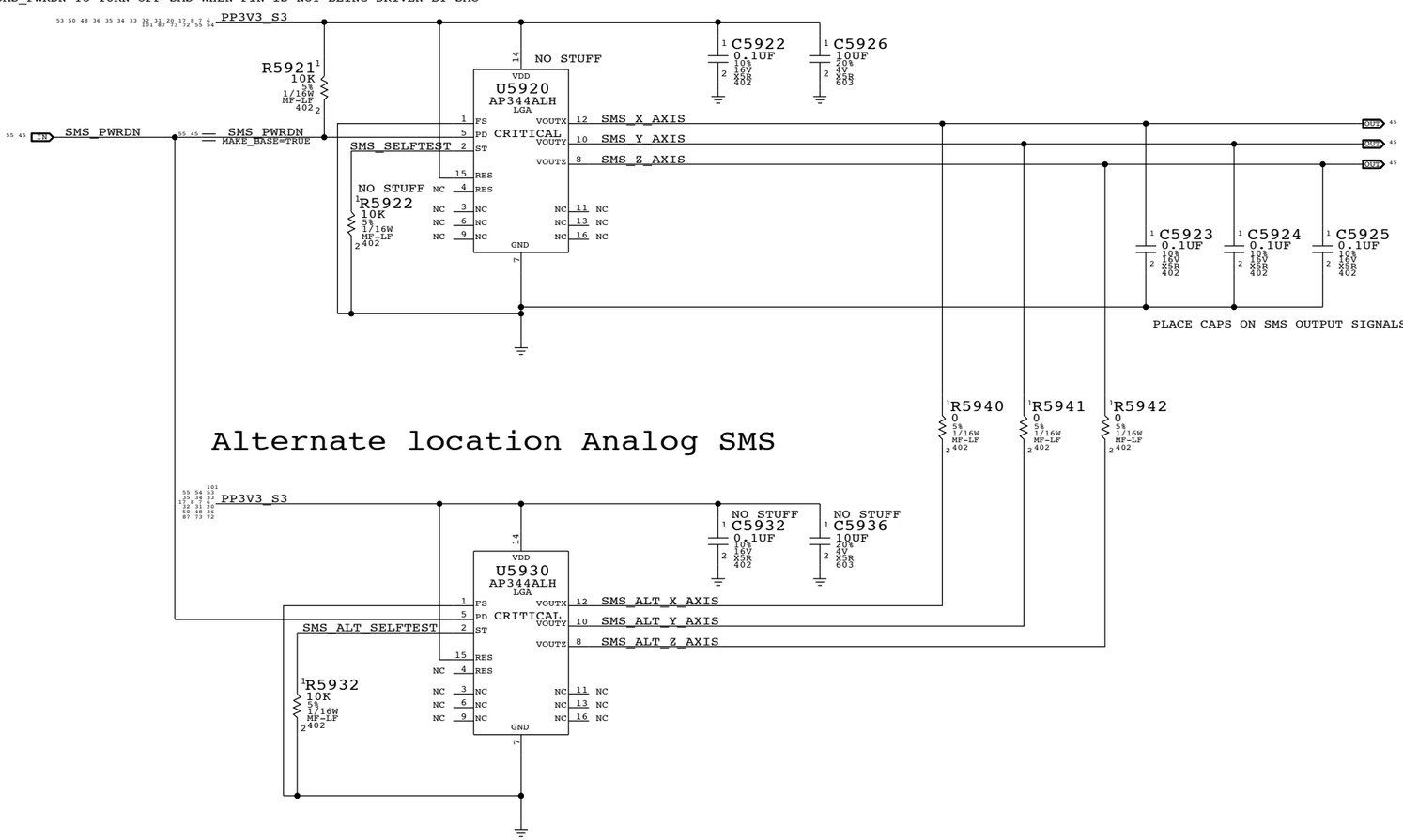
BRANCH: <BRANCH>

PAGE: 58 OF 132

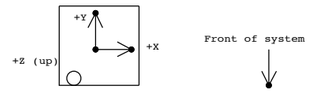
SHEET: 54 OF 101

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



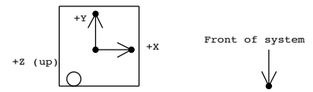
Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

Alternate location Analog SMS

Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC MASTER=K19 MLB SYNC DATE=05/29/2009

PAGE TITLE: Sudden Motion Sensor (SMS)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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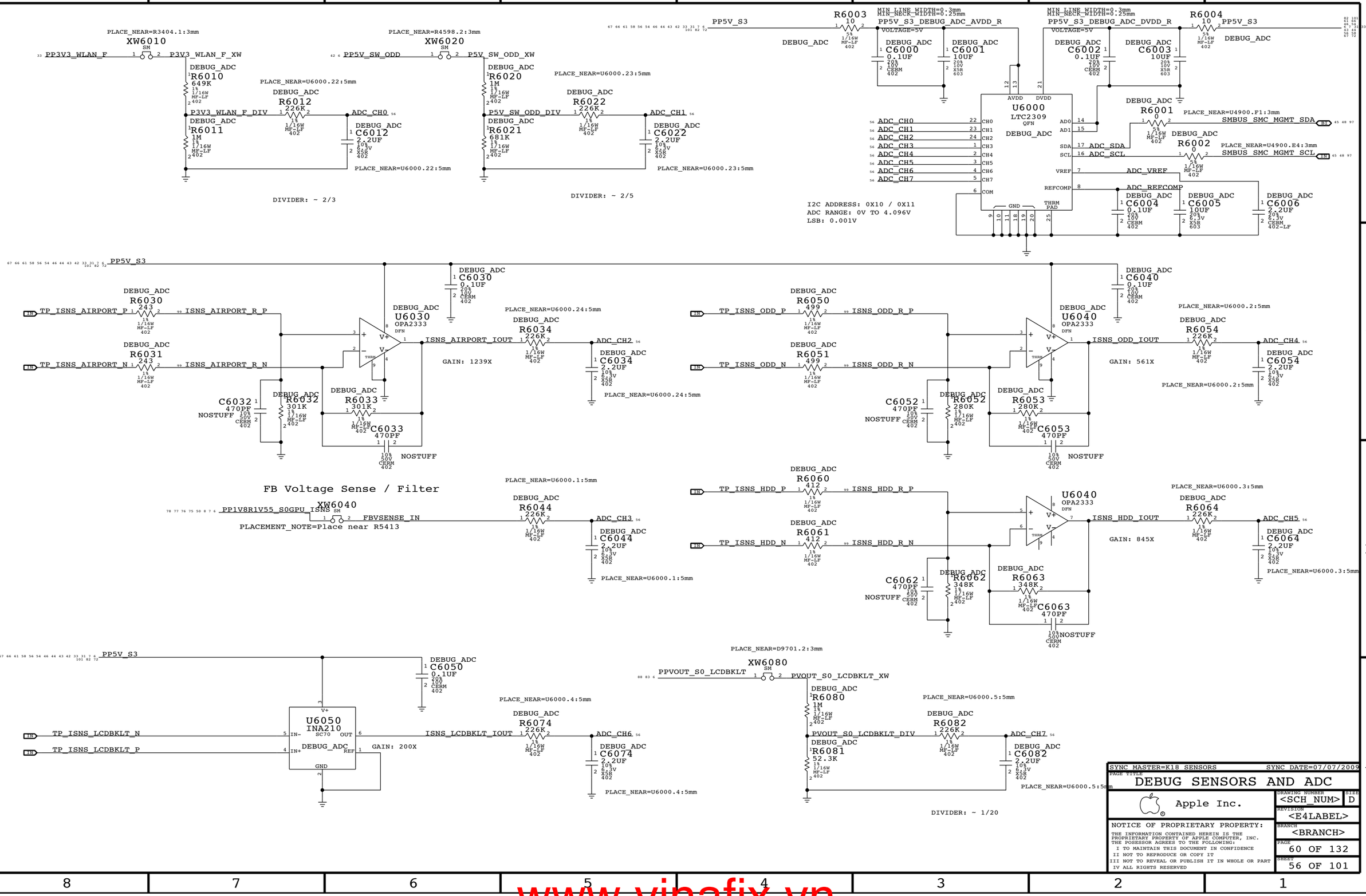

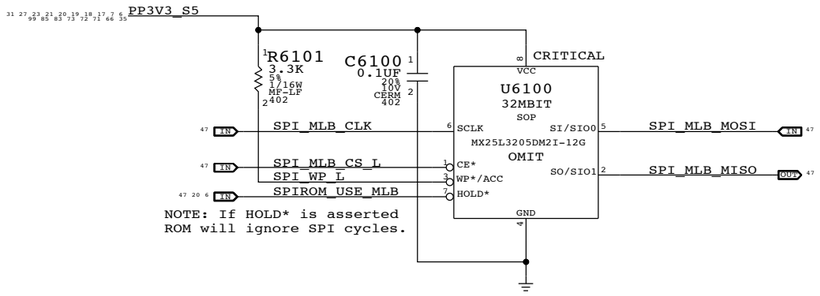

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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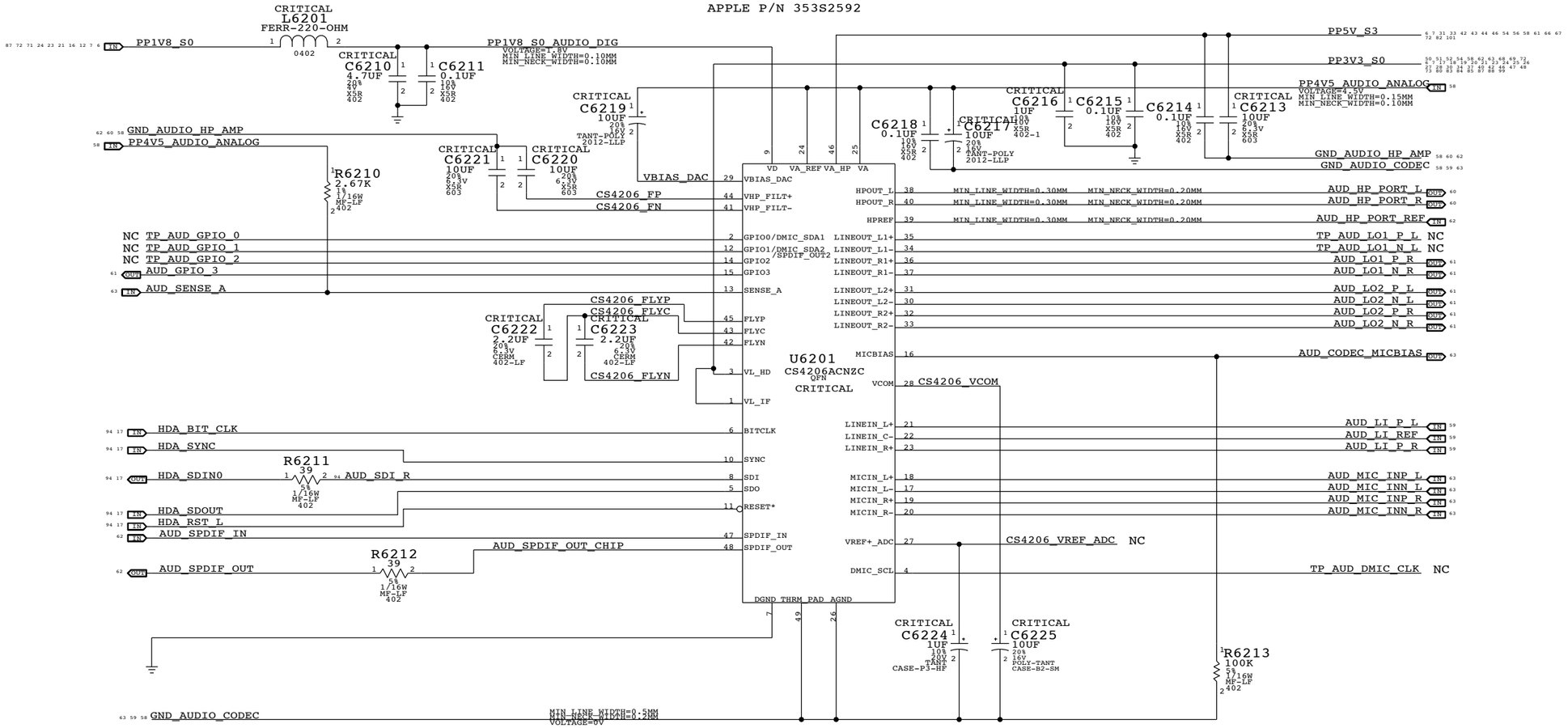
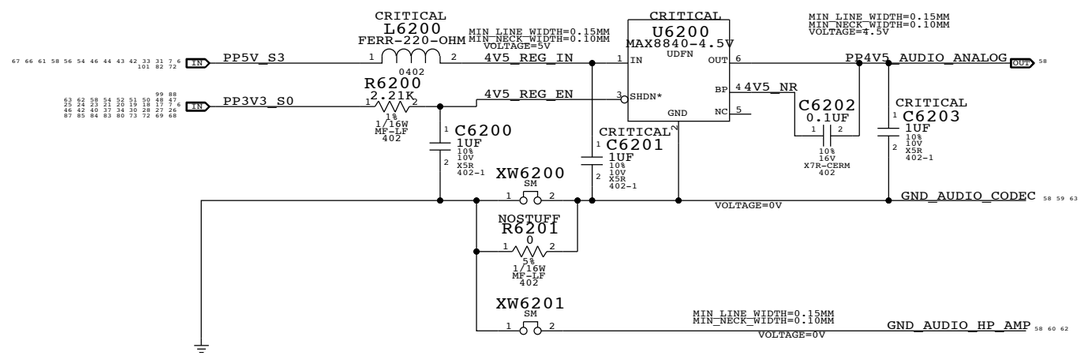
AUDIO CODEC
APPLE P/N 353S2592



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K18_AUDIO SYNC_DATE=09/21/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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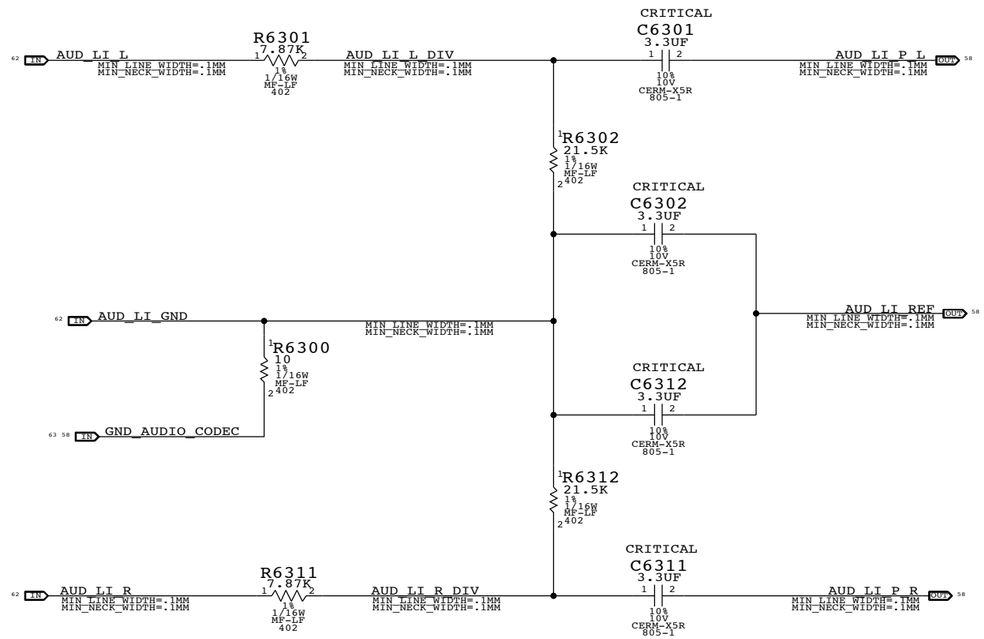
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC MASTER=K18 AUDIO SYNC DATE=07/29/2009

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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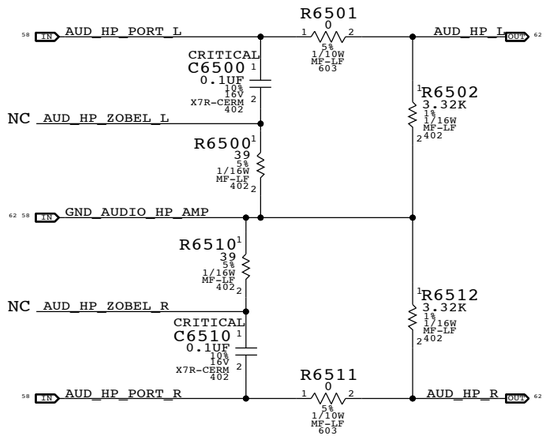
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC MASTER=K18_AUDIO SYNC DATE=07/29/2009

PAGE TITLE
AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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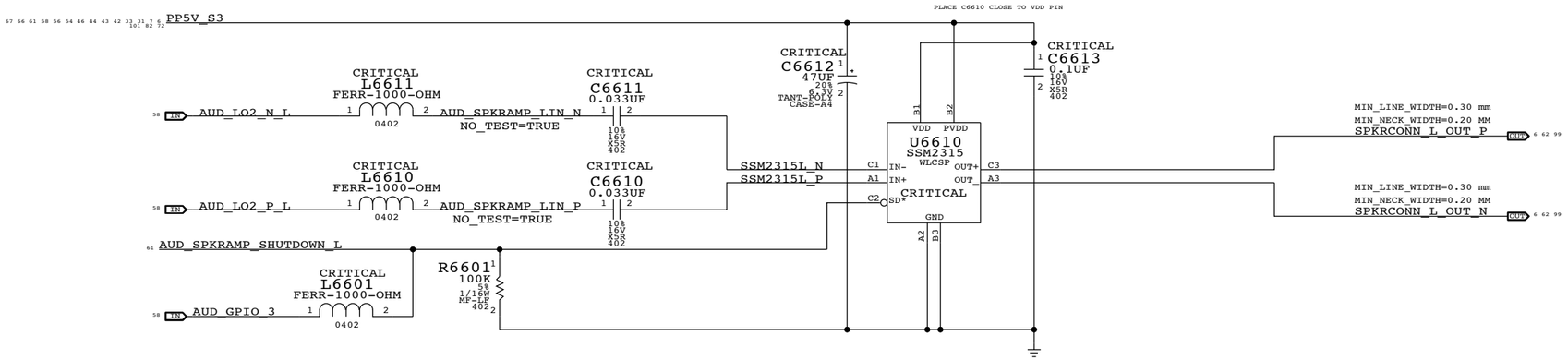
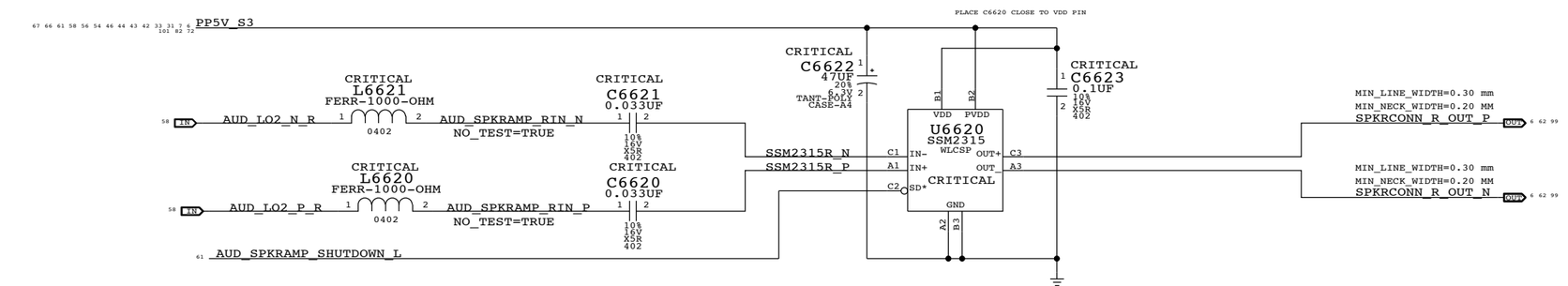
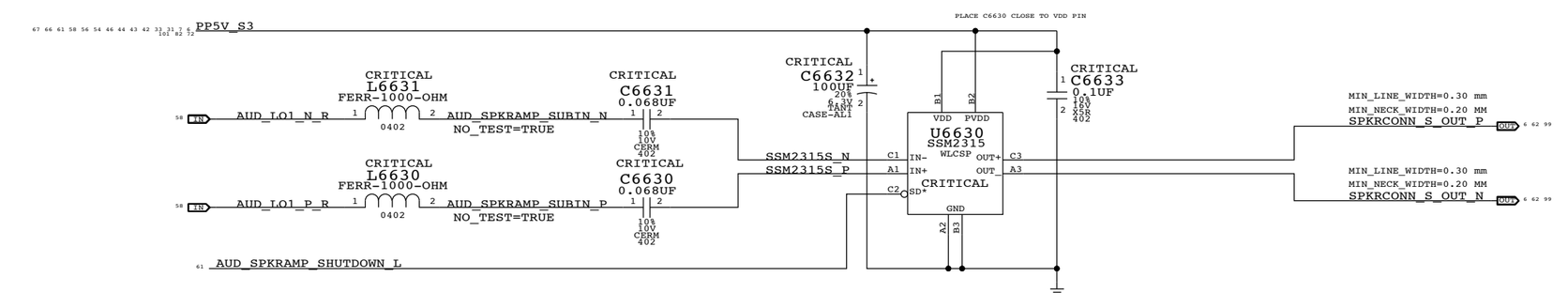
3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500

GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%







SYNC MASTER=K18 AUDIO SYNC DATE=07/29/2009

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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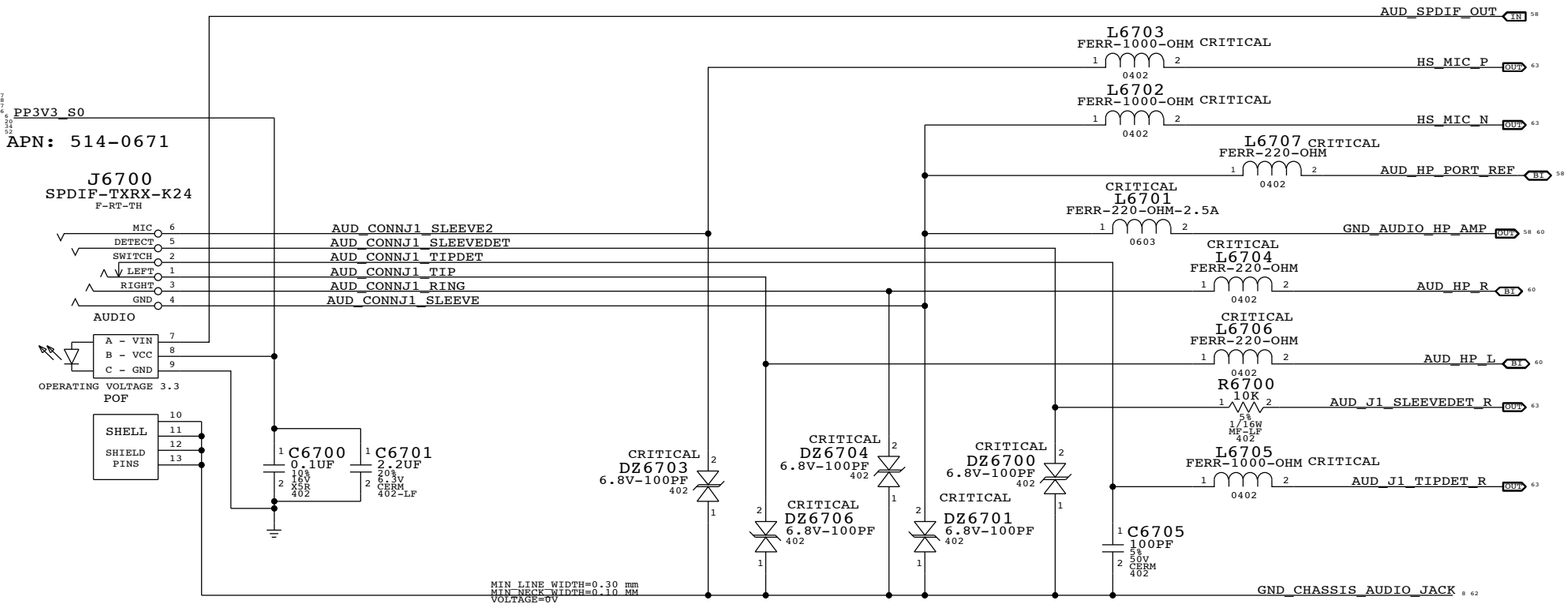
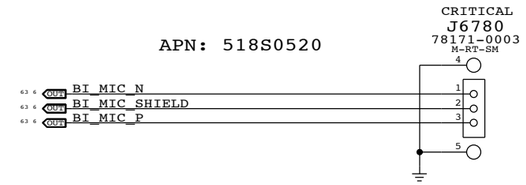
AUDIO JACK 1 LO/HP JACK, SPDIF TX



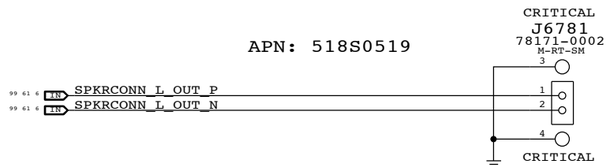
MIC CONNECTOR

APN: 518S0520

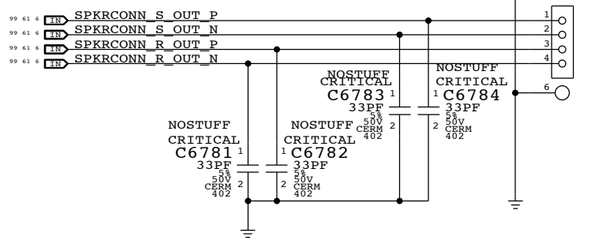


SPEAKER CONNECTOR

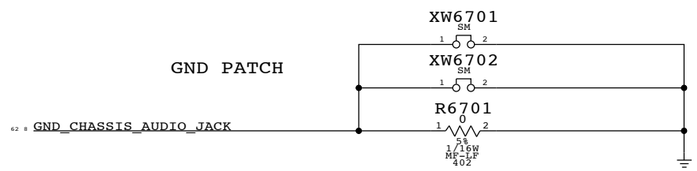
APN: 518S0519



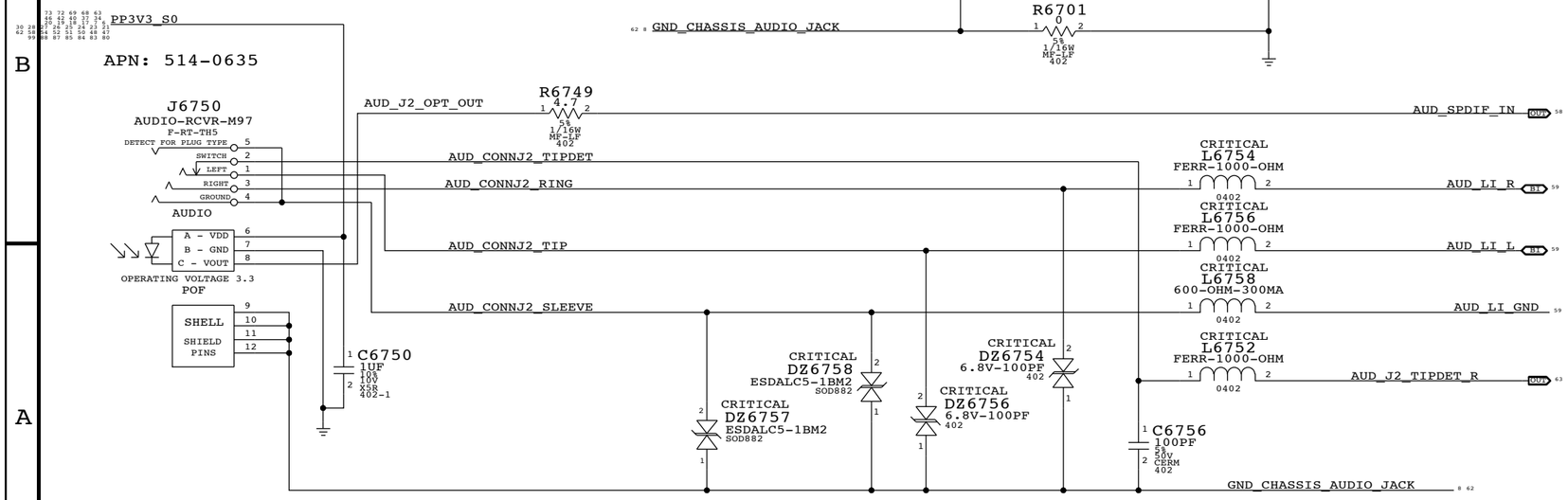
APN: 518S0521



GND PATCH



AUDIO JACK 2 LINE IN JACK, SPDIF RX



SYNC MASTER=K18 AUDIO	SYNC DATE=07/29/2009
PAGE TITLE	AUDIO: JACKS
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 67 OF 132
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

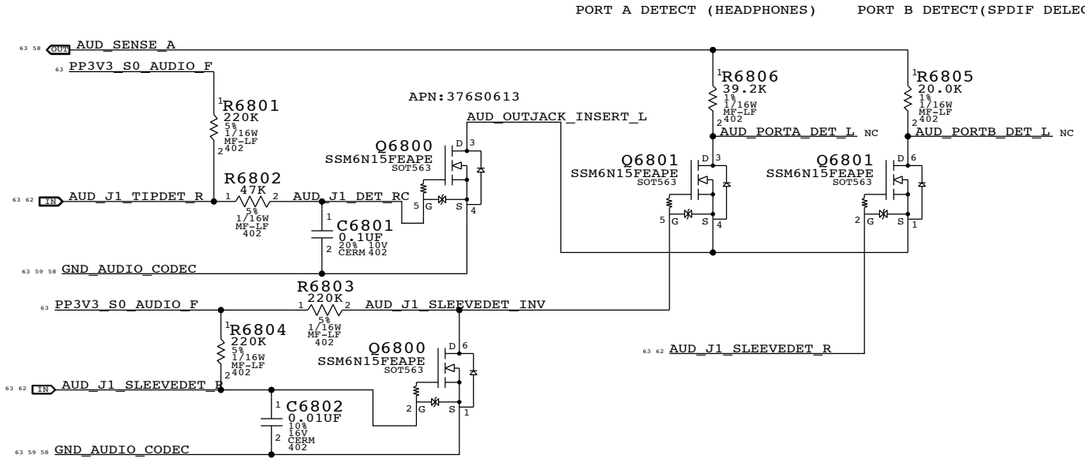
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

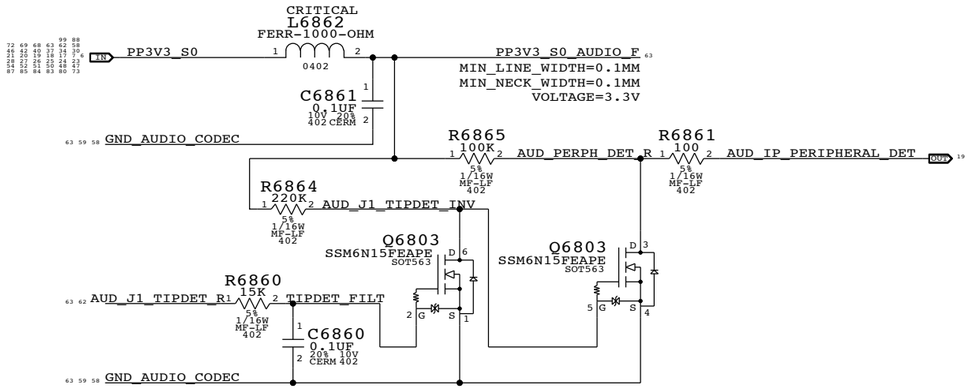
SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

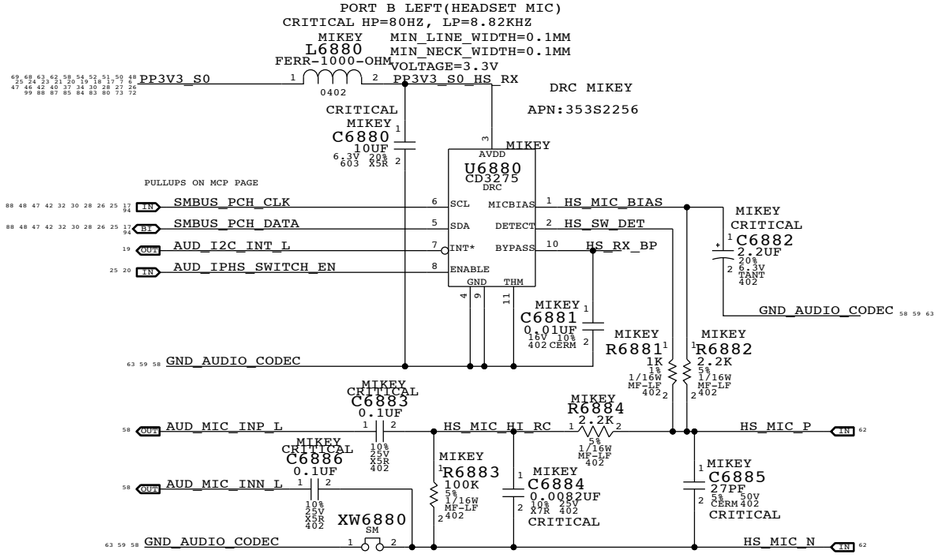
PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



EXTRACTION NOTIFICATION

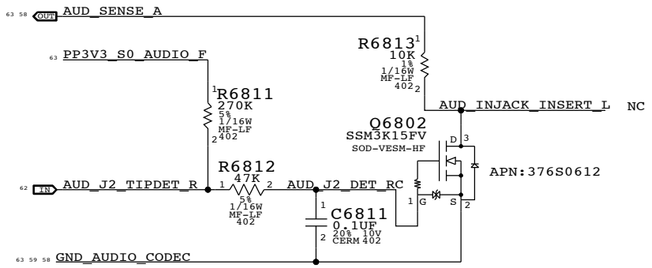


PORT B LEFT(HEADSET MIC)
CRITICAL HP=80HZ, LP=8.82KHZ
MIN_LINE_WIDTH=0.1MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=3.3V



PORT B RIGHT(BUILT-IN MIC)

PORT C DETECT (LINE-IN)



SYNC MASTER=K18 AUDIO	SYNC DATE=07/29/2009
PAGE TITLE: AUDIO: JACK TRANSLATORS	
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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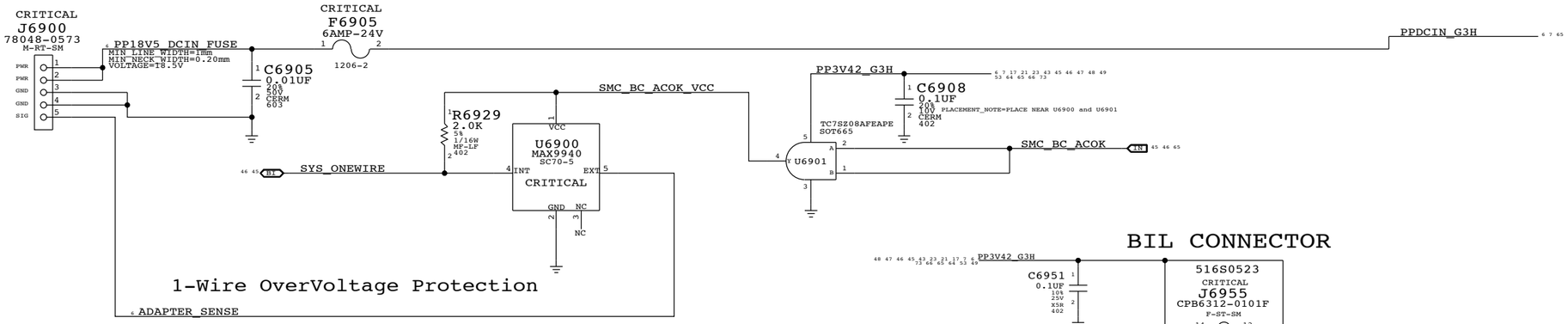
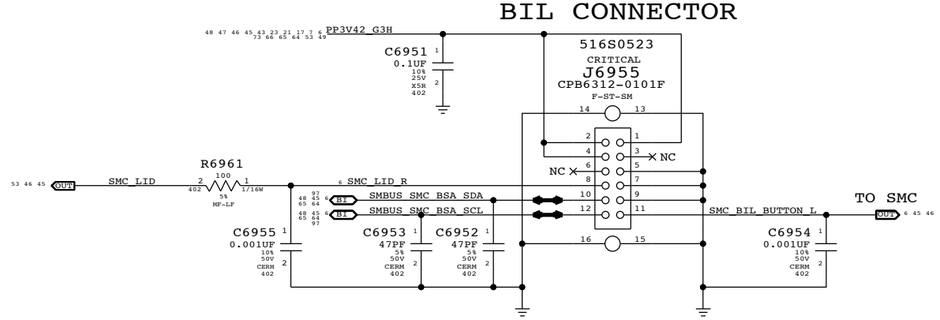
MagSafe DC Power Jack



1-Wire OverVoltage Protection

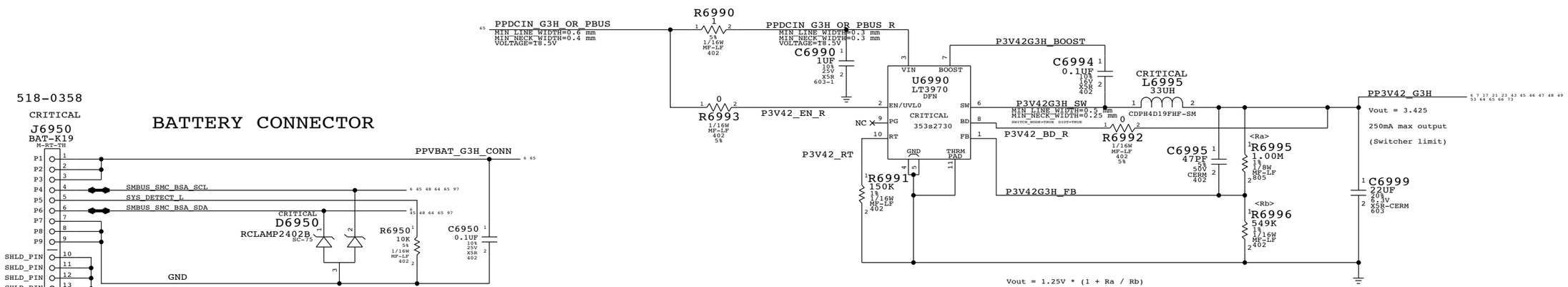
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Reverse-Current Protection

Inrush Limiter

This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.

FROM ADAPTER

PPDCIN_G3H

CRITICAL Q7080 HAT1128R01 SOI

CRITICAL Q7085 HAT1128R01 SOI

PPDCIN_G3H_OR_PBUS

PPDCIN_G3H_INRUSH

R7080 100K 5% 1/16W MF-LF 402

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/16W MF-LF 402

CHGR_SGATE_DIV

CHGR_AGATE_DIV

R7081 62K 5% 1/16W MF-LF 402

R7086 332K 1% 1/16W MF-LF 402

CRITICAL D7005 BAT30CWFILM SOT-323

R7005 20 5% 1/16W MF-LF 402

CHGR_DCIN_D_R

(CHGR_SGATE)

(CHGR_AGATE)

(CHGR_DCIN)

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.55V

Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP

C7001 1UF 10% 10V X5R 402

PP3V42_G3H

BATT_3S R7012 1K 1% 1/16W MF-LF 402

C7002 1UF 10% 10V X5R 402

NO STUFF R7002 100K 5% 1/16W MF-LF 402

GND_CHGR_AGND

R7000 0 5% 1/16W MF-LF 402

R7010 30.1K 1% 1/16W MF-LF 402

SMC_RESET_L

CHGR_RST_L

SMBUS_SMC_BSA_SCL

SMBUS_SMC_BSA_SDA

CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

CHGR_CSO_P

CHGR_CSO_N

R7011 9.31K 1% 1/16W MF-LF 402

R7015 220K 1% 1/16W MF-LF 402

BATT_2S R7013 1K 1% 1/16W MF-LF 402

C7050 1UF 10% 16V X5R 402

C7015 470PF 10% 50V CERM 402

CHGR_VCOMP_R

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 50V CERM 402

U7000 ISL6259HRTZ TQFN

VDD	19		
VDDP	20		
VHST	12	CRITICAL DCIN	2 CHGR_DCIN
SMB_RST_N	13	SGATE	26 CHGR_SGATE
SCL	11	AGATE	1 CHGR_AGATE
SDA	10	CSIP	28 CHGR_CSI_P
VFRQ	4	CSIN	27 CHGR_CSI_N
CELL	6	BOOT	25 CHGR_BOOT
ACIN	3	UGATE	24 CHGR_UGATE
ICOMP	5	PHASE	23 CHGR_PHASE
VCOMP	7	LGATE	21 CHGR_LGATE
VNEG	8	BGATE	16 CHGR_BGATE
CSOP	18	20V/V AMON	9 CHGR_AMON
CSON	17	36V/V BMON	15 CHGR_BMON
(AGND) THRM_PAD	29	(OD) ACOK	14 SMC_BC_ACOK
PGND	22		

353S2392

XW7000 SM

(GND)

PLACE_NEAR=U7000.29:1mm

PLACE_NEAR=U7000.22:1mm

C7042 0.033UF 10% 16V X5R 402

C7011 0.01UF 10% 16V CERM 402

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 20% 25V X5R 603

C7026 0.001UF 10% 50V CERM 402

GND_CHGR_AGND

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

R7021 10 5% 1/16W MF-LF 402

R7022 10 5% 1/16W MF-LF 402

CHGR_CSI_R_P

CHGR_CSI_R_N

CRITICAL R7020 0.020 0.5% 1W MF-LF 0612

PPDCIN_G3H_CHGR

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

C7020 0.047UF 10% 10V CERM 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

CRITICAL C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

C7037 0.001UF 10% 50V X7R 402

C7025 0.22UF 10% 10V CERM 402

PLACE_NEAR=U7000.25:2mm

CRITICAL Q7030 RJK0332DPB-01 LFPAK-SM

Max Current = 8A
(L7030 limit)
f = 400 kHz

CRITICAL L7030 4.7UH-10.2A FDA1254F-SM

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL F7040 8AMP-24V 1206

TO SYSTEM

PPBUS_G3H

NO STUFF R7039 180 5% 1/10W MF-LF 603

CRITICAL Q7035 RJK0305DPB LFPAK-HF

CHGR_PHASE_RC

NO STUFF C7039 470PF 10% 50V CERM 402

PPVBAT_G3H_CHGR_REG

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

CRITICAL C7040 22UF 20% 25V POLY-TANT CASE-D2-SM

C7045 0.001UF 10% 50V X7R 402

BATT_2S R7050 0.005 1% 1W MF 0612

PPVBAT_G3H_CHGR_R

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7055 1UF 10% 25V X5R 603-1

C7056 0.1UF 10% 16V X5R 402

C7057 0.01UF 10% 16V CERM 402

CRITICAL Q7055 SI7137DP SO-8

TO/FROM BATTERY

PPVBAT_G3H_CONN

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

R7051 2.2 5% 1/16W MF-LF 402

R7052 0 5% 1/16W MF-LF 402

CHGR_CSO_R_P

CHGR_CSO_R_N

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0139	1	RES,0.010,0.5%,1W,0612-1	R7050	CRITICAL	BATT_3S

SYNC_MASTER=K18_POWER SYNC_DATE=06/30/2009

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

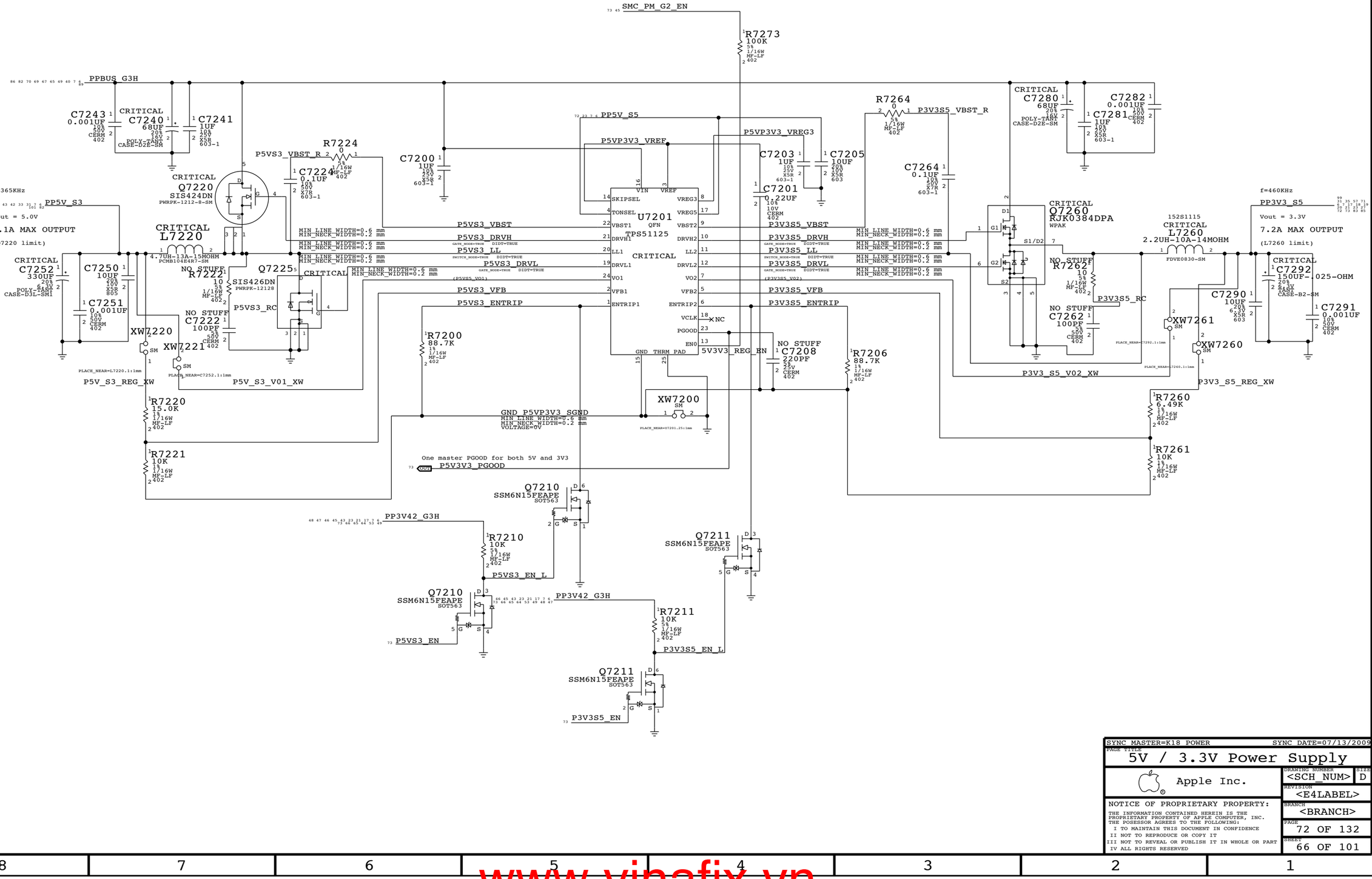
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 70 OF 132

SHEET: 65 OF 101



SYNC_MASTER=K18_POWER SYNC_DATE=07/13/2009

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

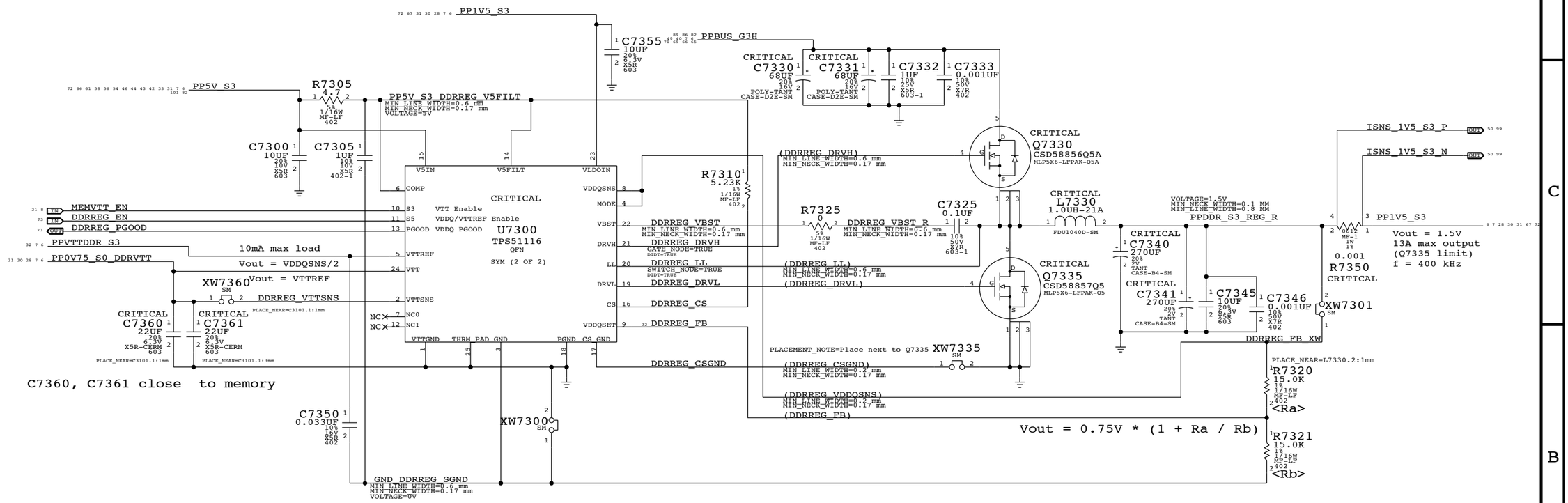
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

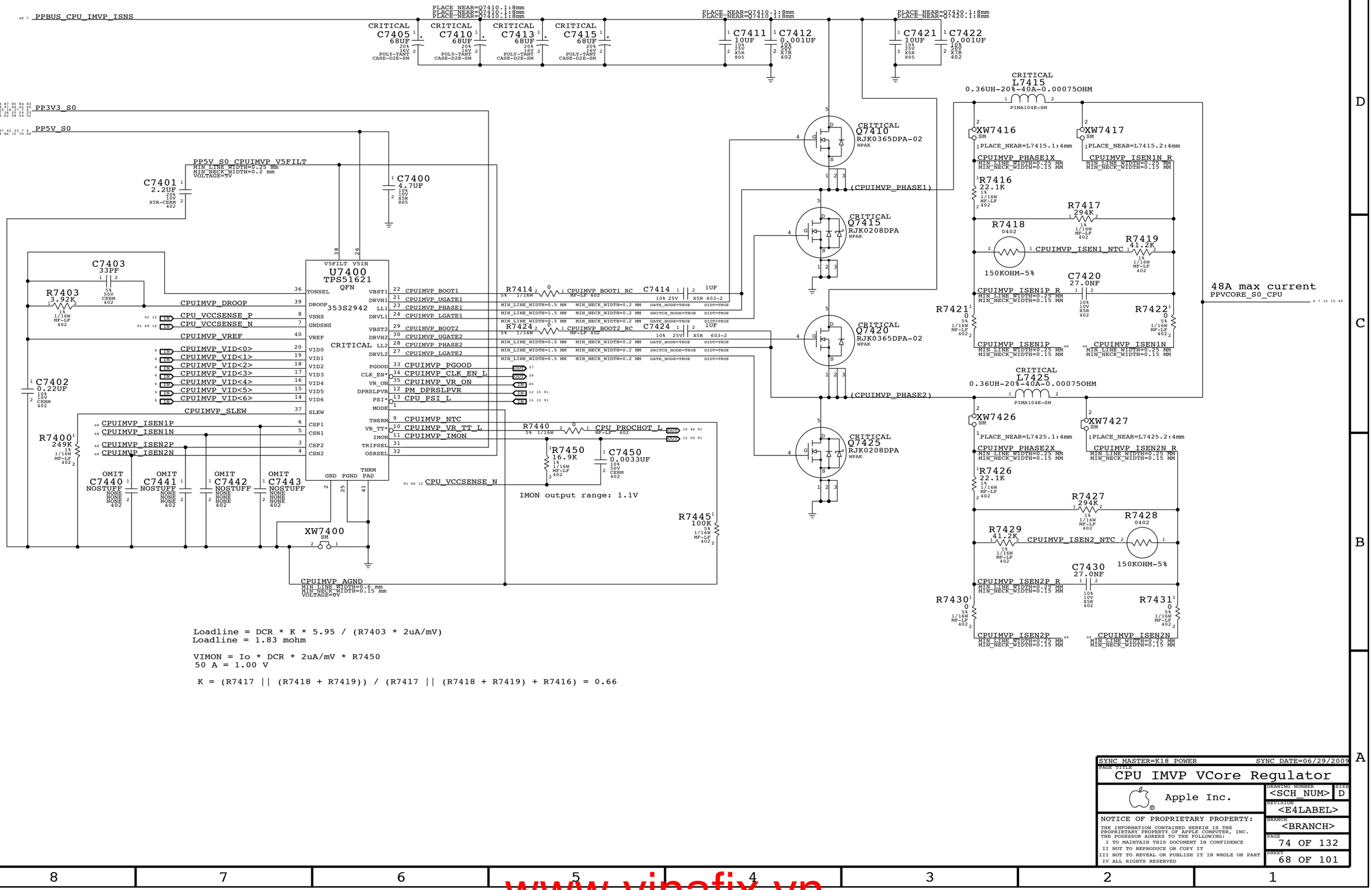
BRANCH <BRANCH>

PAGE 72 OF 132

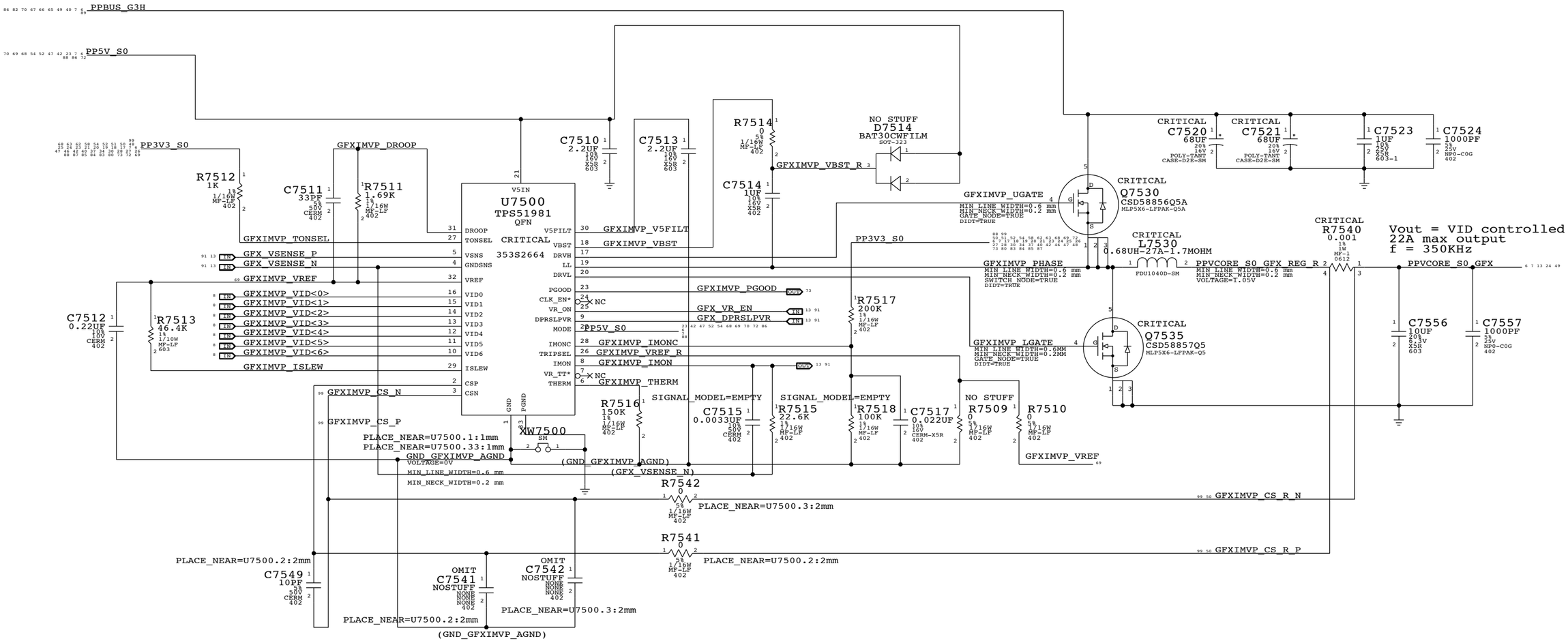
SHEET 66 OF 101



SYNC MASTER=K18 POWER	SYNC DATE=07/14/2009
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 73 OF 132
	SHEET 67 OF 101



GFX IMVP VCORE



Imon= Io xR7540 x2uA/mV x R7515

Imon= Io x45.2mV/A

22A => 1V

SYNC MASTER=K18 POWER	SYNC DATE=07/08/2009
PAGE TITLE: GFX IMVP VCore Regulator	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 75 OF 132
	SHEET: 69 OF 101

CPU VTT (1.05V S0) Regulator

PP5V_S0
PPBUS_G3H
R7601 2.2 5% 1/10W MF-LF 603
C7601 10UF 20% 10V X5R 603
PP5V_S0_CPUVTTS0_VCC
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
CPUVTTS0_BOOT_RC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
R7630 0 5% 1/16W MF-LF 402
C7630 1UF 10% 16V X5R 402
CRITICAL C7620 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7621 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7623 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7622 0.001UF 10% 50V X7R 402
U7600 ISL95870 UTQFN
VCC PVCC
EN BOOT
FB UGATE
SREF PHASE
VO LGATE
OCSET CRITICAL
PGOOD
RTN
FSEL
GND PGND
CPUVTTS0_EN
CPUVTTS0_FB
CPUVTTS0_SREF
CPUVTTS0_PGOOD
CPU_VTTSENSE_P
CPU_VTTSENSE_N
CPUVTTS0_VO
CPUVTTS0_OCSET
CPUVTTS0_RTN
CPUVTTS0_FSEL
CPUVTTS0_VBST
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
CPUVTTS0_DRVH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
DIDT=TRUE
CRITICAL Q7630 CSD58856Q5A MLP5X6-LFPAK-Q5A
CPUVTTS0_LL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE
CPUVTTS0_DRVL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
DIDT=TRUE
CRITICAL Q7635 CSD58857Q5 MLP5X6-LFPAK-Q5
152S1085
CRITICAL
L7630
0.68UH-27A-1.7MOHM
FDU1040D-SM
PPCPUVTT_S0_REG_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
CRITICAL R7640 0.001 1% 1W MF-1 0612
PP1V05_S0
Vout = 1.05V
27A max output
f = 300 kHz
C7647 10UF 20% 6.3V X5R 603
CPUVTTS0_CS_P
CPUVTTS0_CS_N
R7641 3.48K 1% 1/16W MF-LF 402
C7640 1000PF 5% 25V NP0-C0G 402
R7642 3.48K 1% 1/16W MF-LF 402
R7604 3.01K 1% 1/16W MF-LF 402
R7605 2.74K 1% 1/16W MF-LF 402
C7602 2.2UF 10% 16V X5R 603
C7604 0.001UF 10% 50V X7R 402
C7605 0.001UF 10% 50V X7R 402
C7603 0.047UF 10% 10V CERM 402
R7603 0 5% 1/16W MF-LF 402
XW7600 SM
CPUVTTS0_AGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V
(CPUVTTS0_OCSET)
(CPUVTTS0_VO)
SIGNAL_MODEL=EMPTY
NO STUFF
C7641 0.0022UF 10% 50V CERM 402
CPUVTTS0_FB_RC
SIGNAL_MODEL=EMPTY
NO STUFF
R7643 100 1% 1/16W MF-LF 402
R7644 3.01K 1% 1/16W MF-LF 402
<Ra>
Vout = 0.5V * (1 + Ra / Rb)
(CPUVTTS0_FB)
<Rb>
R7645 2.74K 1% 1/16W MF-LF 402
(CPUVTTS0_AGND)

SYNC_MASTER=K18_POWER SYNC_DATE=07/14/2009

PAGE TITLE
CPUVTT (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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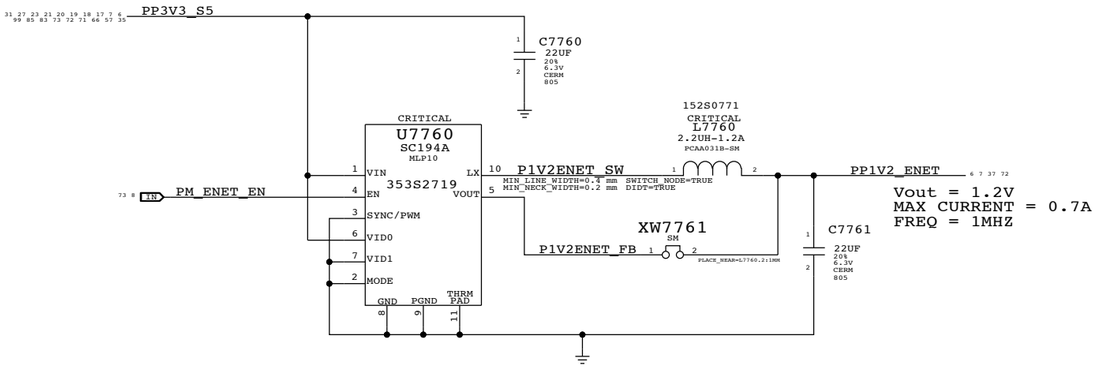
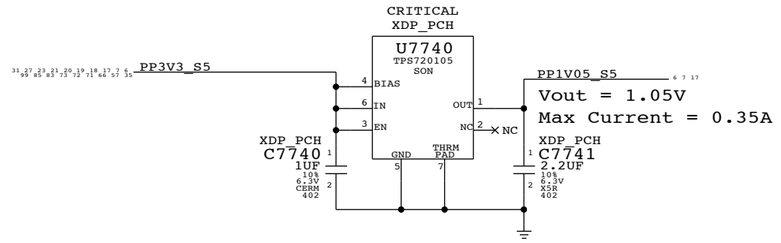
1.2V S3 Regulator

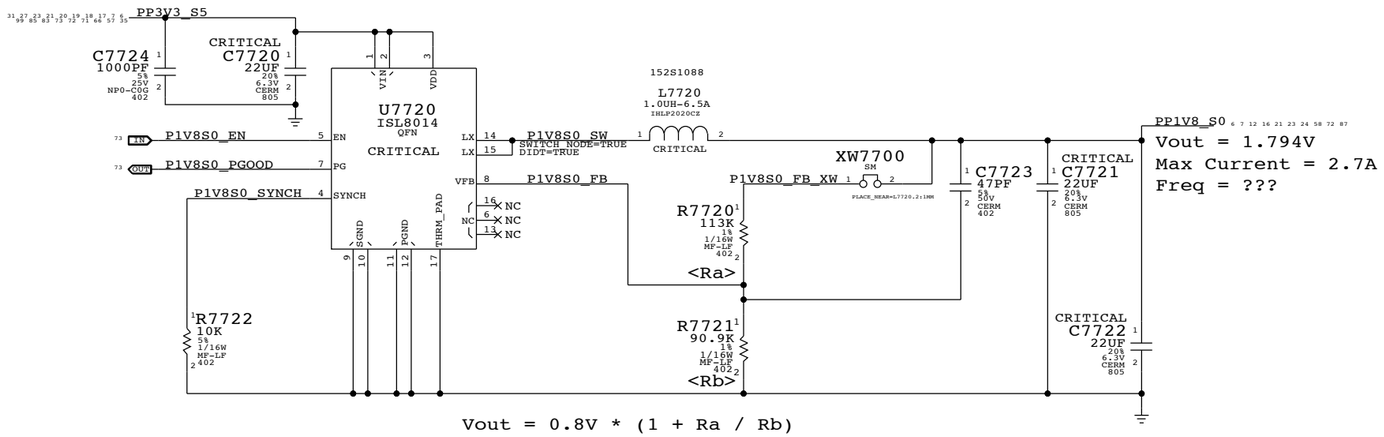


1.05V S5 LDO

Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.8V S0 Regulator



Vout = 0.8V * (1 + Ra / Rb)

SYNC MASTER=K18 POWER SYNC DATE=06/29/2009

PAGE TITLE

Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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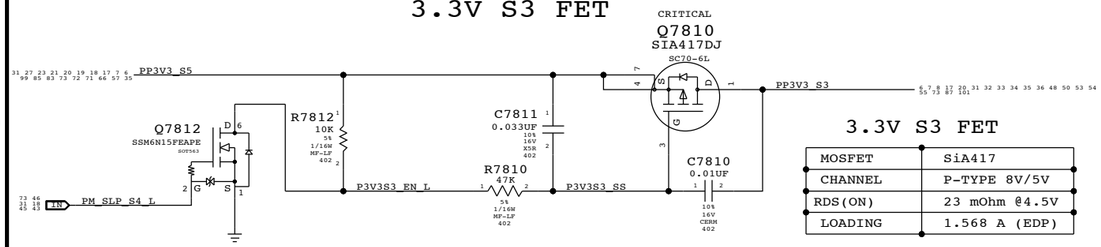
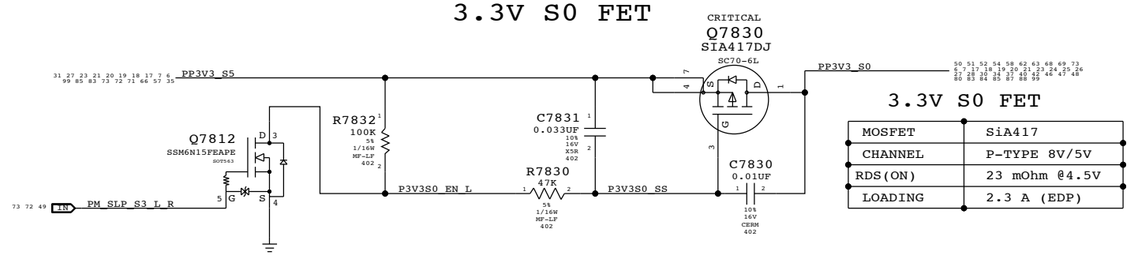
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	1.568 A (EDP)

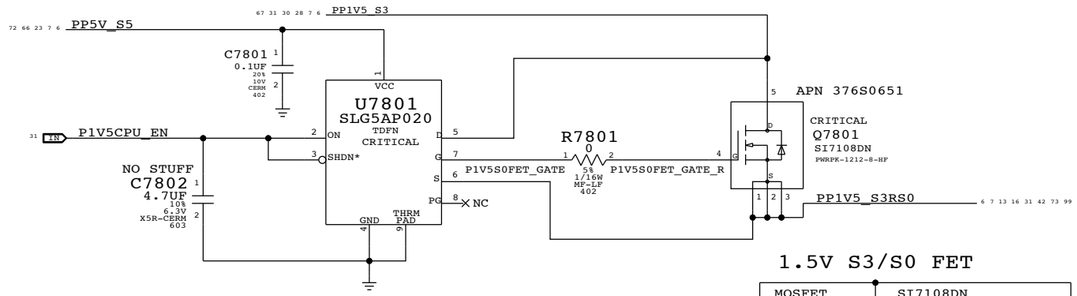
3.3V S0 FET



3.3V S0 FET

MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	2.3 A (EDP)

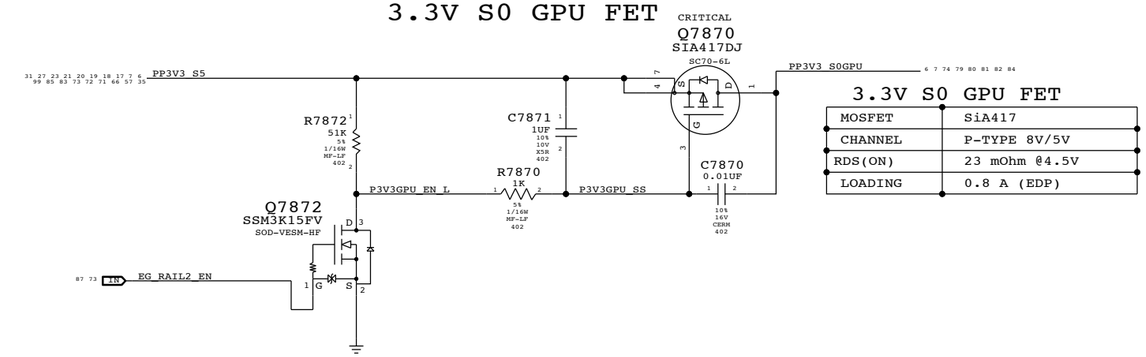
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	3.2 A (EDP)

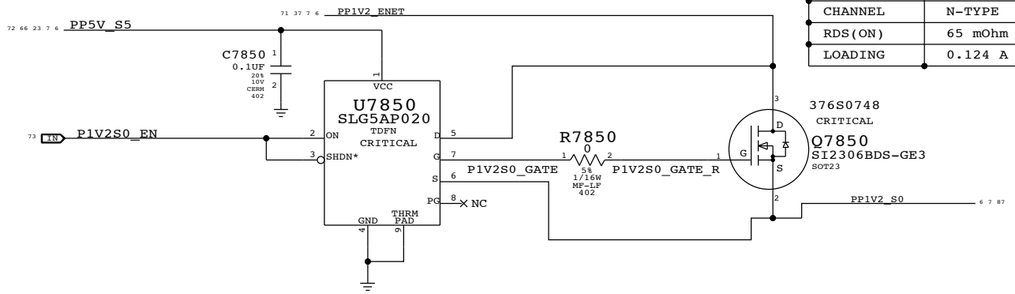
3.3V S0 GPU FET



3.3V S0 GPU FET

MOSFET	SiA417
CHANNEL	P-TYPE 8V/5V
RDS(ON)	23 mOhm @4.5V
LOADING	0.8 A (EDP)

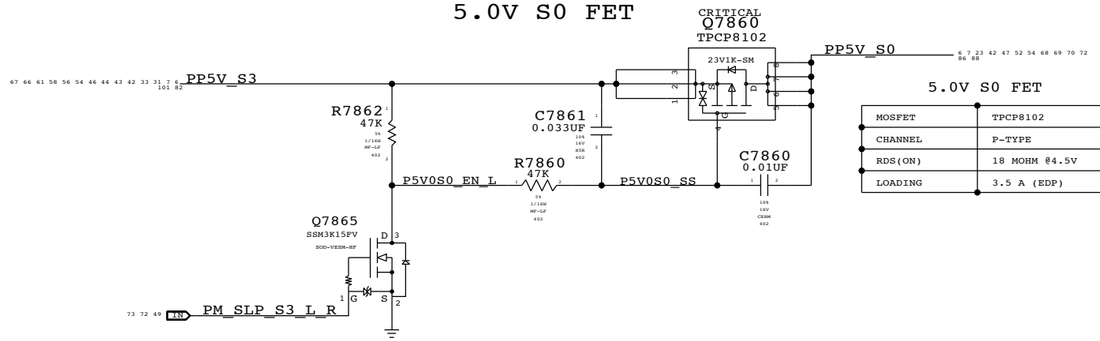
1.2V S0 FET



1.2V S0 FET

MOSFET	SI2306BDS-GE3
CHANNEL	N-TYPE
RDS(ON)	65 mOhm @4.5V
LOADING	0.124 A (EDP)

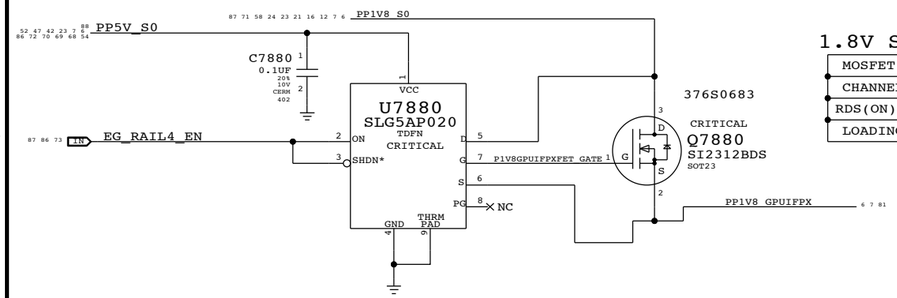
5.0V S0 FET



5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	3.5 A (EDP)

1.8V S0 GPU_IFPX FET



1.8V S0 GPU_IFPX FET

MOSFET	SI2312BDS
CHANNEL	N-TYPE
RDS(ON)	31 mOhm @4.5V
LOADING	0.3 A (EDP)

SYNC_MASTER=K18_POWER SYNC_DATE=06/10/2009

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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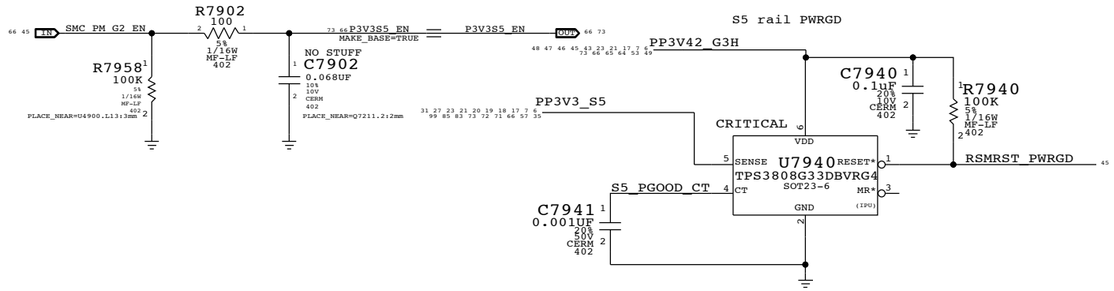
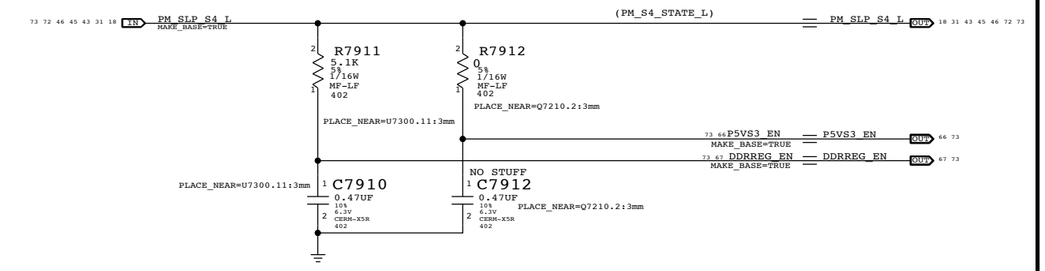
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.3V S5 ENABLE

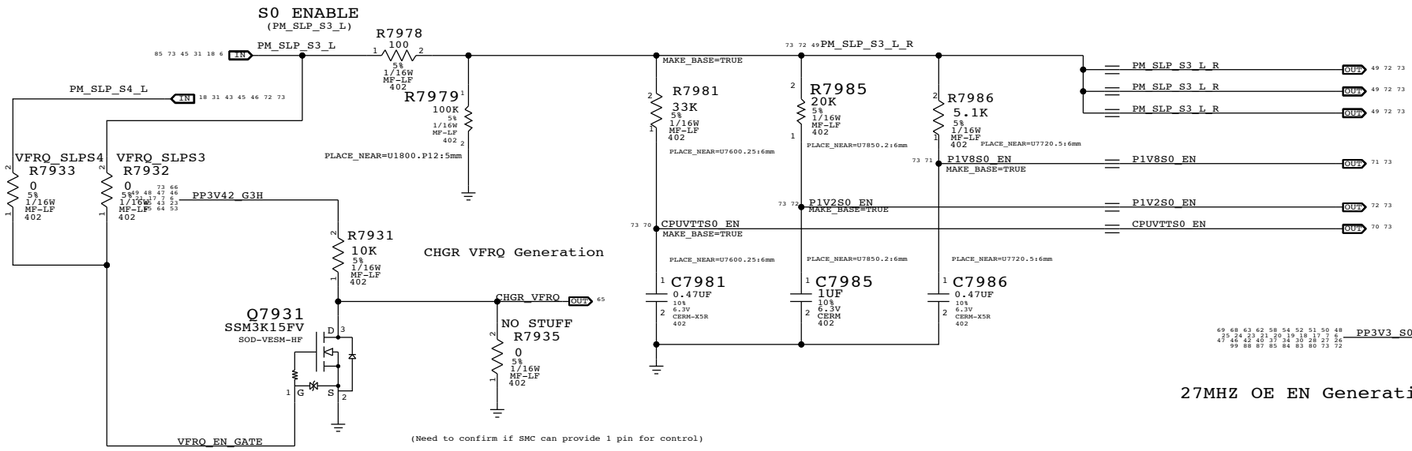


3.3V,5V S3 ENABLE

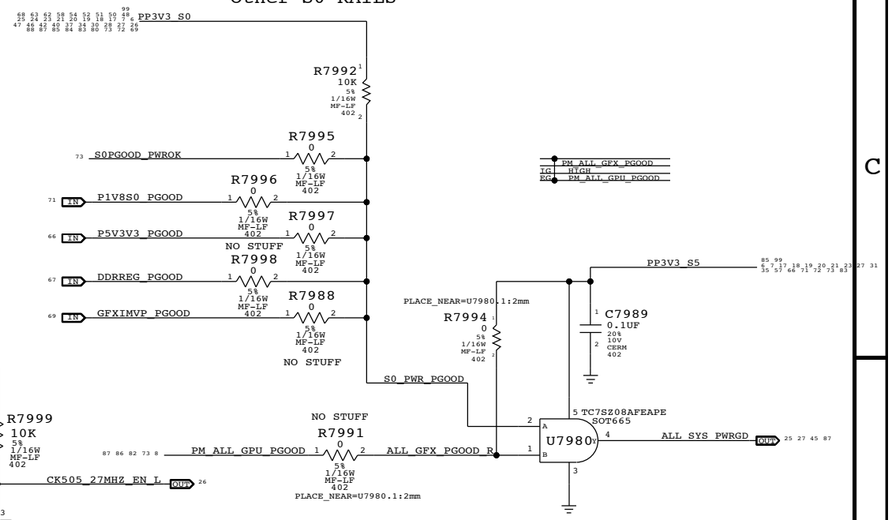


S0 ENABLE

(PM_SLP_S3_L)



Other S0 RAILS



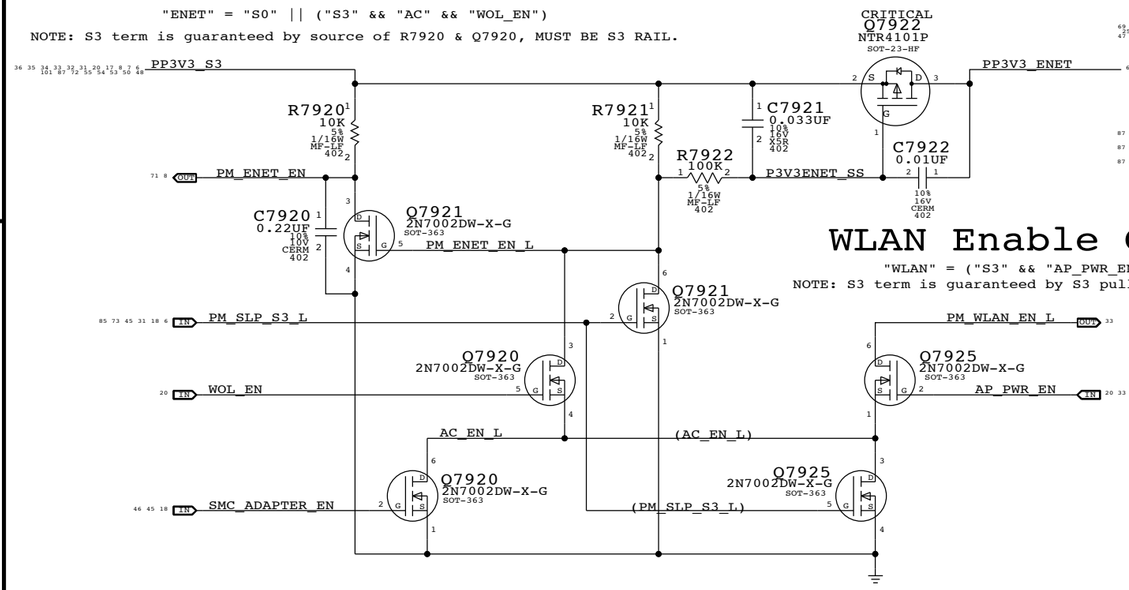
27MHZ OE EN Generation

ENET Enable Generation

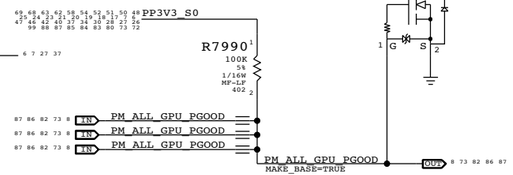
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R7920 & Q7920, MUST BE S3 RAIL.

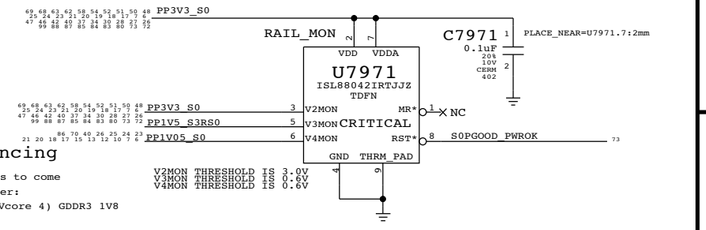
3.3V ENET FET



EXT GPU PWRGD Pullup



3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

GPU Rail Sequencing

GT216 GPU requires rails to come up in the following order:

1) 1.05V 2) GPU 3V3 3) GPU Vcore 4) GDDR3 1V8

EG_RAIL1_EN — EG_RAIL1_EN (MAKE_BASE=TRUE)

EG_RAIL2_EN — EG_RAIL2_EN (MAKE_BASE=TRUE)

EG_RAIL3_EN — EG_RAIL3_EN (MAKE_BASE=TRUE)

EG_RAIL4_EN — EG_RAIL4_EN (MAKE_BASE=TRUE)

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 79 OF 132

SHEET: 73 OF 101

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEX 1.1V Current = 2A

250mA

1500mA

120 mA: GT216 A01 DG v3 01/09

NC_GPU_DFM
NO_TEST=TRUE

OMIT

U8000
NV-GT216
BGA
(2 OF 9)

U8000
NV-GT216
BGA
(1 OF 9)

OMIT

L8015
100NH-700MA-0.14OHM
0603

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.1V

NO STUFF

PP3V3R1V1_GPU_PEX_SVDD
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

SYNC_MASTER=K17_REF	SYNC_DATE=06/15/2009
PAGE TITLE	NV GT216 PCI-E
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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	SHEET 74 OF 101

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPVCORE_GPU

777A @ 777/777MHz Core/Mem Clk for VDD

C8100 1UF 10% 16V X5R 402
C8101 0.22UF 10% 6.3V CERM-X5R 402
C8102 0.22UF 10% 6.3V CERM-X5R 402
C8103 0.1UF 10% 16V X7R-CERM 402
C8104 0.047UF 10% 16V X7R 402
C8105 0.047UF 10% 16V X7R 402
C8106 0.047UF 10% 16V X7R 402
C8107 0.022UF 10% 16V CERM-X5R 402
C8108 0.022UF 10% 16V CERM-X5R 402
C8109 0.022UF 10% 16V CERM-X5R 402
C8110 0.015UF 10% 16V X7R 402
C8111 0.015UF 10% 25V X7R 402
C8112 0.01UF 10% 25V X7R 402
C8113 0.01UF 10% 25V X7R 402
C8114 0.01UF 10% 25V X7R 402
C8115 0.01UF 10% 25V X7R 402
C8116 0.01UF 10% 25V X7R 402
C8117 0.01UF 10% 25V X7R 402
C8118 0.0068UF 10% 25V CERM 402
C8119 0.0047UF 10% 25V CERM 402

U8000 NV-GT216 BGA (9 OF 9) OMIT

VDD

U8000 NV-GT216 BGA (8 OF 9) OMIT

GND

PP1V8R1V55_S0GPU_ISNS

Nvidia PRD for GB-128 umes 4x4.7uF, 8x0.47uF, 16x0.1uF

777A @ 777MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8156 4.7UF 20% 6.3V CERM 603
C8157 0.1UF 10% 16V CERM 402
C8158 0.1UF 10% 16V CERM 402
C8159 0.1UF 10% 16V CERM 402
C8160 0.047UF 10% 16V X7R 402
C8162 0.047UF 10% 16V X7R 402
C8163 0.047UF 10% 16V X7R 402
C8164 0.01UF 10% 25V X7R 402
C8165 0.01UF 10% 25V X7R 402
C8166 0.01UF 10% 25V X7R 402

OMIT

U8000 NV-GT216 BGA (7 OF 9)

FBVDDQ

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 CORE/FB POWER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 75 OF 101

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NV-GT216
BGA
(3 OF 9)

FB_A_DQ<0>	L32	FBA_D00	FBA_CMD0	V32	FB_A_LMA<4>
FB_A_DQ<1>	N33	FBA_D01	FBA_CMD1	W31	FB_A_RAS_L
FB_A_DQ<2>	L33	FBA_D02	FBA_CMD2	U31	FB_A_LMA<5>
FB_A_DQ<3>	N34	FBA_D03	FBA_CMD3	Y32	FB_A_BA<1>
FB_A_DQ<4>	N35	FBA_D04	FBA_CMD4	AB35	FB_A_UMA<2>
FB_A_DQ<5>	P35	FBA_D05	FBA_CMD5	AB34	FB_A_UMA<4>
FB_A_DQ<6>	P33	FBA_D06	FBA_CMD6	W35	FB_A_UMA<3>
FB_A_DQ<7>	P34	FBA_D07	FBA_CMD7	W33	FB_A_UCKE
FB_A_DQ<8>	K35	FBA_D08	FBA_CMD8	W30	FB_A_UCS0_L
FB_A_DQ<9>	K33	FBA_D09	FBA_CMD9	T34	FB_A_MA<11>
FB_A_DQ<10>	K34	FBA_D10	FBA_CMD10	T35	FB_A_LCAS_L
FB_A_DQ<11>	H33	FBA_D11	FBA_CMD11	AB31	FB_A_WE_L
FB_A_DQ<12>	G34	FBA_D12	FBA_CMD12	Y30	FB_A_BA<0>
FB_A_DQ<13>	G33	FBA_D13	FBA_CMD13	Y34	FB_A_UMA<5>
FB_A_DQ<14>	E34	FBA_D14	FBA_CMD14	W32	FB_A_MA<12>
FB_A_DQ<15>	E33	FBA_D15	FBA_CMD15	AA30	FB_A_DRAM_RST
FB_A_DQ<16>	G31	FBA_D16	FBA_CMD16	AA32	FB_A_MA<7>
FB_A_DQ<17>	F30	FBA_D17	FBA_CMD17	Y33	FB_A_MA<10>
FB_A_DQ<18>	G30	FBA_D18	FBA_CMD18	U32	FB_A_LCKE
FB_A_DQ<19>	G32	FBA_D19	FBA_CMD19	Y31	FB_A_MA<0>
FB_A_DQ<20>	K30	FBA_D20	FBA_CMD20	U34	FB_A_MA<9>
FB_A_DQ<21>	K32	FBA_D21	FBA_CMD21	Y35	FB_A_MA<6>
FB_A_DQ<22>	H30	FBA_D22	FBA_CMD22	W34	FB_A_LMA<2>
FB_A_DQ<23>	K31	FBA_D23	FBA_CMD23	V30	FB_A_MA<8>
FB_A_DQ<24>	L31	FBA_D24	FBA_CMD24	U35	FB_A_LMA<3>
FB_A_DQ<25>	L30	FBA_D25	FBA_CMD25	U30	FB_A_MA<1>
FB_A_DQ<26>	M32	FBA_D26	FBA_CMD26	U33	NC_FBA_MA<13>
FB_A_DQ<27>	N30	FBA_D27	FBA_CMD27	AB30	FB_A_BA<2>
FB_A_DQ<28>	M30	FBA_D28	FBA_CMD28	AB33	NC_FB_A_UCS1_L
FB_A_DQ<29>	P31	FBA_D29	FBA_CMD29	T33	FB_A_LCS0_L
FB_A_DQ<30>	R32	FBA_D30	FBA_CMD30	W29	NC_FB_A_LCS1_L
FB_A_DQ<31>	R30	FBA_D31			
FB_A_DQ<32>	AG30	FBA_D32	FBA_CLK0	T32	FB_A_CLK_P<0>
FB_A_DQ<33>	AG32	FBA_D33	FBA_CLK0*	T31	FB_A_CLK_N<0>
FB_A_DQ<34>	AH31	FBA_D34	FBA_CLK1	AC31	FB_A_CLK_P<1>
FB_A_DQ<35>	AF31	FBA_D35	FBA_CLK1*	AC30	FB_A_CLK_N<1>
FB_A_DQ<36>	AF30	FBA_D36			
FB_A_DQ<37>	AE30	FBA_D37	FBA_DQM0	P32	FB_A_DQM_L<0>
FB_A_DQ<38>	AC32	FBA_D38	FBA_DQM1	H34	FB_A_DQM_L<1>
FB_A_DQ<39>	AD30	FBA_D39	FBA_DQM2	J30	FB_A_DQM_L<2>
FB_A_DQ<40>	AN33	FBA_D40	FBA_DQM3	P30	FB_A_DQM_L<3>
FB_A_DQ<41>	AL31	FBA_D41	FBA_DQM4	AF32	FB_A_DQM_L<4>
FB_A_DQ<42>	AM33	FBA_D42	FBA_DQM5	AL32	FB_A_DQM_L<5>
FB_A_DQ<43>	AL33	FBA_D43	FBA_DQM6	AL34	FB_A_DQM_L<6>
FB_A_DQ<44>	AK30	FBA_D44	FBA_DQM7	AF35	FB_A_DQM_L<7>
FB_A_DQ<45>	AK32	FBA_D45			
FB_A_DQ<46>	AJ30	FBA_D46	FBA_DQS_RN0	L35	FB_A_RDQS<0>
FB_A_DQ<47>	AH30	FBA_D47	FBA_DQS_RN1	G35	FB_A_RDQS<1>
FB_A_DQ<48>	AH33	FBA_D48	FBA_DQS_RN2	H31	FB_A_RDQS<2>
FB_A_DQ<49>	AH35	FBA_D49	FBA_DQS_RN3	N32	FB_A_RDQS<3>
FB_A_DQ<50>	AH34	FBA_D50	FBA_DQS_RN4	AD32	FB_A_RDQS<4>
FB_A_DQ<51>	AH32	FBA_D51	FBA_DQS_RN5	AJ31	FB_A_RDQS<5>
FB_A_DQ<52>	AJ33	FBA_D52	FBA_DQS_RN6	AJ35	FB_A_RDQS<6>
FB_A_DQ<53>	AL35	FBA_D53	FBA_DQS_RN7	AC34	FB_A_RDQS<7>
FB_A_DQ<54>	AM34	FBA_D54			
FB_A_DQ<55>	AM35	FBA_D55	FBA_DQS_WP0	L34	FB_A_WDQS<0>
FB_A_DQ<56>	AF33	FBA_D56	FBA_DQS_WP1	H35	FB_A_WDQS<1>
FB_A_DQ<57>	AE32	FBA_D57	FBA_DQS_WP2	J32	FB_A_WDQS<2>
FB_A_DQ<58>	AF34	FBA_D58	FBA_DQS_WP3	N31	FB_A_WDQS<3>
FB_A_DQ<59>	AE35	FBA_D59	FBA_DQS_WP4	AE31	FB_A_WDQS<4>
FB_A_DQ<60>	AE34	FBA_D60	FBA_DQS_WP5	AJ32	FB_A_WDQS<5>
FB_A_DQ<61>	AE33	FBA_D61	FBA_DQS_WP6	AJ34	FB_A_WDQS<6>
FB_A_DQ<62>	AB32	FBA_D62	FBA_DQS_WP7	AC33	FB_A_WDQS<7>
FB_A_DQ<63>	AC35	FBA_D63			
			FB_DLLAVDD	AG27	PP1V1_GPU_FBPLLAVDD_F
			FB_PLLAVDD	AF27	
			FBA_DEBUG	T30	FB_A_UCAS_L
			FB_CAL_PD_VDDQ	K27	FBCAL_PD_VDDQ
			FB_CAL_PU_GND	L27	FBCAL_PU_GND
			FB_CAL_TERM_GND	M27	FBCAL_TERM_GND

NC: R29, R29, R29, R29, R29, R29, R29, R29

R8203 10K 5% 1/16W MF-LF 402
R8200 10K 5% 1/16W MF-LF 402
R8201 10K 5% 1/16W MF-LF 402

PP1V05_S0GPU
CRITICAL
L8200 300-OHM-0.5A 0603-1
C8202 1UF 10% 6.3V CERM 402
C8200 4.7UF 10% 6.3V X5R-CERM 603
C8201 4.7UF 10% 6.3V X5R-CERM 603

PP1V8R1V55_S0GPU_ISNS
R8290 56.2 1% 1/16W MF-LF 402
PLACE_NEAR=U8000.K27:3mm
R8292 40.2 1% 1/16W MF-LF 402
PLACE_NEAR=U8000.M27:3mm
R8291 31.6 1% 1/16W MF-LF 402
PLACE_NEAR=U8000.L27:3mm

MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V

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FB_B_DQ<0>	B13	FBC_D00	FBC_CMD0	C17	FB_B_LMA<4>
FB_B_DQ<1>	D13	FBC_D01	FBC_CMD1	B19	FB_B_RAS_L
FB_B_DQ<2>	A13	FBC_D02	FBC_CMD2	D18	FB_B_LMA<5>
FB_B_DQ<3>	A14	FBC_D03	FBC_CMD3	F21	FB_B_BA<1>
FB_B_DQ<4>	C16	FBC_D04	FBC_CMD4	A23	FB_B_UMA<2>
FB_B_DQ<5>	B16	FBC_D05	FBC_CMD5	D21	FB_B_UMA<4>
FB_B_DQ<6>	A17	FBC_D06	FBC_CMD6	B23	FB_B_UMA<3>
FB_B_DQ<7>	D16	FBC_D07	FBC_CMD7	E20	FB_B_UCKE
FB_B_DQ<8>	C13	FBC_D08	FBC_CMD8	G21	FB_B_UCS0_L
FB_B_DQ<9>	B11	FBC_D09	FBC_CMD9	F20	FB_B_MA<11>
FB_B_DQ<10>	C11	FBC_D10	FBC_CMD10	F19	FB_B_LCAS_L
FB_B_DQ<11>	A11	FBC_D11	FBC_CMD11	F23	FB_B_WE_L
FB_B_DQ<12>	C10	FBC_D12	FBC_CMD12	A22	FB_B_BA<0>
FB_B_DQ<13>	C8	FBC_D13	FBC_CMD13	C22	FB_B_UMA<5>
FB_B_DQ<14>	B8	FBC_D14	FBC_CMD14	B17	FB_B_MA<12>
FB_B_DQ<15>	A8	FBC_D15	FBC_CMD15	F24	FB_B_DRAM_RST
FB_B_DQ<16>	E8	FBC_D16	FBC_CMD16	C25	FB_B_MA<7>
FB_B_DQ<17>	F8	FBC_D17	FBC_CMD17	E22	FB_B_MA<10>
FB_B_DQ<18>	F10	FBC_D18	FBC_CMD18	C20	FB_B_LCKE
FB_B_DQ<19>	F9	FBC_D19	FBC_CMD19	B22	FB_B_MA<0>
FB_B_DQ<20>	F12	FBC_D20	FBC_CMD20	A19	FB_B_MA<9>
FB_B_DQ<21>	D8	FBC_D21	FBC_CMD21	D22	FB_B_MA<6>
FB_B_DQ<22>	D11	FBC_D22	FBC_CMD22	D20	FB_B_LMA<2>
FB_B_DQ<23>	E11	FBC_D23	FBC_CMD23	E19	FB_B_MA<8>
FB_B_DQ<24>	D12	FBC_D24	FBC_CMD24	D19	FB_B_LMA<3>
FB_B_DQ<25>	E13	FBC_D25	FBC_CMD25	F18	FB_B_MA<1>
FB_B_DQ<26>	F13	FBC_D26	FBC_CMD26	C19	NC_FBB_MA<13>
FB_B_DQ<27>	F14	FBC_D27	FBC_CMD27	F22	FB_B_BA<2>
FB_B_DQ<28>	F15	FBC_D28	FBC_CMD28	C23	NC_FB_B_UCS1_L
FB_B_DQ<29>	E16	FBC_D29	FBC_CMD29	B20	FB_B_LCS0_L
FB_B_DQ<30>	F16	FBC_D30	FBC_CMD30	A20	NC_FB_B_LCS1_L
FB_B_DQ<31>	F17	FBC_D31			
FB_B_DQ<32>	D29	FBC_D32	FBC_CLK0	E17	FB_B_CLK_P<0>
FB_B_DQ<33>	F27	FBC_D33	FBC_CLK0*	D17	FB_B_CLK_N<0>
FB_B_DQ<34>	F28	FBC_D34	FBC_CLK1	D23	FB_B_CLK_P<1>
FB_B_DQ<35>	E28	FBC_D35	FBC_CLK1*	E23	FB_B_CLK_N<1>
FB_B_DQ<36>	D26	FBC_D36			
FB_B_DQ<37>	F25	FBC_D37	FBC_DQM0	A16	FB_B_DQM_L<0>
FB_B_DQ<38>	D24	FBC_D38	FBC_DQM1	D10	FB_B_DQM_L<1>
FB_B_DQ<39>	E25	FBC_D39	FBC_DQM2	F11	FB_B_DQM_L<2>
FB_B_DQ<40>	E32	FBC_D40	FBC_DQM3	D15	FB_B_DQM_L<3>
FB_B_DQ<41>	F32	FBC_D41	FBC_DQM4	D27	FB_B_DQM_L<4>
FB_B_DQ<42>	D33	FBC_D42	FBC_DQM5	D34	FB_B_DQM_L<5>
FB_B_DQ<43>	E31	FBC_D43	FBC_DQM6	A34	FB_B_DQM_L<6>
FB_B_DQ<44>	C33	FBC_D44	FBC_DQM7	D28	FB_B_DQM_L<7>
FB_B_DQ<45>	F29	FBC_D45			
FB_B_DQ<46>	D30	FBC_D46	FBC_DQS_RN0	B14	FB_B_RDQS<0>
FB_B_DQ<47>	E29	FBC_D47	FBC_DQS_RN1	B10	FB_B_RDQS<1>
FB_B_DQ<48>	B29	FBC_D48	FBC_DQS_RN2	D9	FB_B_RDQS<2>
FB_B_DQ<49>	C31	FBC_D49	FBC_DQS_RN3	E14	FB_B_RDQS<3>
FB_B_DQ<50>	C29	FBC_D50	FBC_DQS_RN4	F26	FB_B_RDQS<4>
FB_B_DQ<51>	B31	FBC_D51	FBC_DQS_RN5	D31	FB_B_RDQS<5>
FB_B_DQ<52>	C32	FBC_D52	FBC_DQS_RN6	A31	FB_B_RDQS<6>
FB_B_DQ<53>	B32	FBC_D53	FBC_DQS_RN7	A26	FB_B_RDQS<7>
FB_B_DQ<54>	B35	FBC_D54			
FB_B_DQ<55>	B34	FBC_D55	FBC_DQS_WP0	C14	FB_B_WDQS<0>
FB_B_DQ<56>	A29	FBC_D56	FBC_DQS_WP1	A10	FB_B_WDQS<1>
FB_B_DQ<57>	B28	FBC_D57	FBC_DQS_WP2	E10	FB_B_WDQS<2>
FB_B_DQ<58>	A28	FBC_D58	FBC_DQS_WP3	D14	FB_B_WDQS<3>
FB_B_DQ<59>	C28	FBC_D59	FBC_DQS_WP4	E26	FB_B_WDQS<4>
FB_B_DQ<60>	C26	FBC_D60	FBC_DQS_WP5	D32	FB_B_WDQS<5>
FB_B_DQ<61>	D25	FBC_D61	FBC_DQS_WP6	A32	FB_B_WDQS<6>
FB_B_DQ<62>	B25	FBC_D62	FBC_DQS_WP7	B26	FB_B_WDQS<7>
FB_B_DQ<63>	A25	FBC_D63			
			FBC_DEBUG	G19	FB_B_UCAS_L
			FB_VREF	J27	GPU_FB_VREF

NC: C11, C12, C14, C15, C24, C25, C27, C28

R8252 10K 5% 1/16W MF-LF 402
R8251 10K 5% 1/16W MF-LF 402
R8250 10K 5% 1/16W MF-LF 402

PP1V8R1V55_S0GPU_ISNS
R8295 1.07K 1% 1/16W MF-LF 402
GPU_FB_VREF
R8296 2.49K 1% 1/16W MF-LF 402

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009
PAGE TITLE
NV GT216 FRAME BUFFER I/F

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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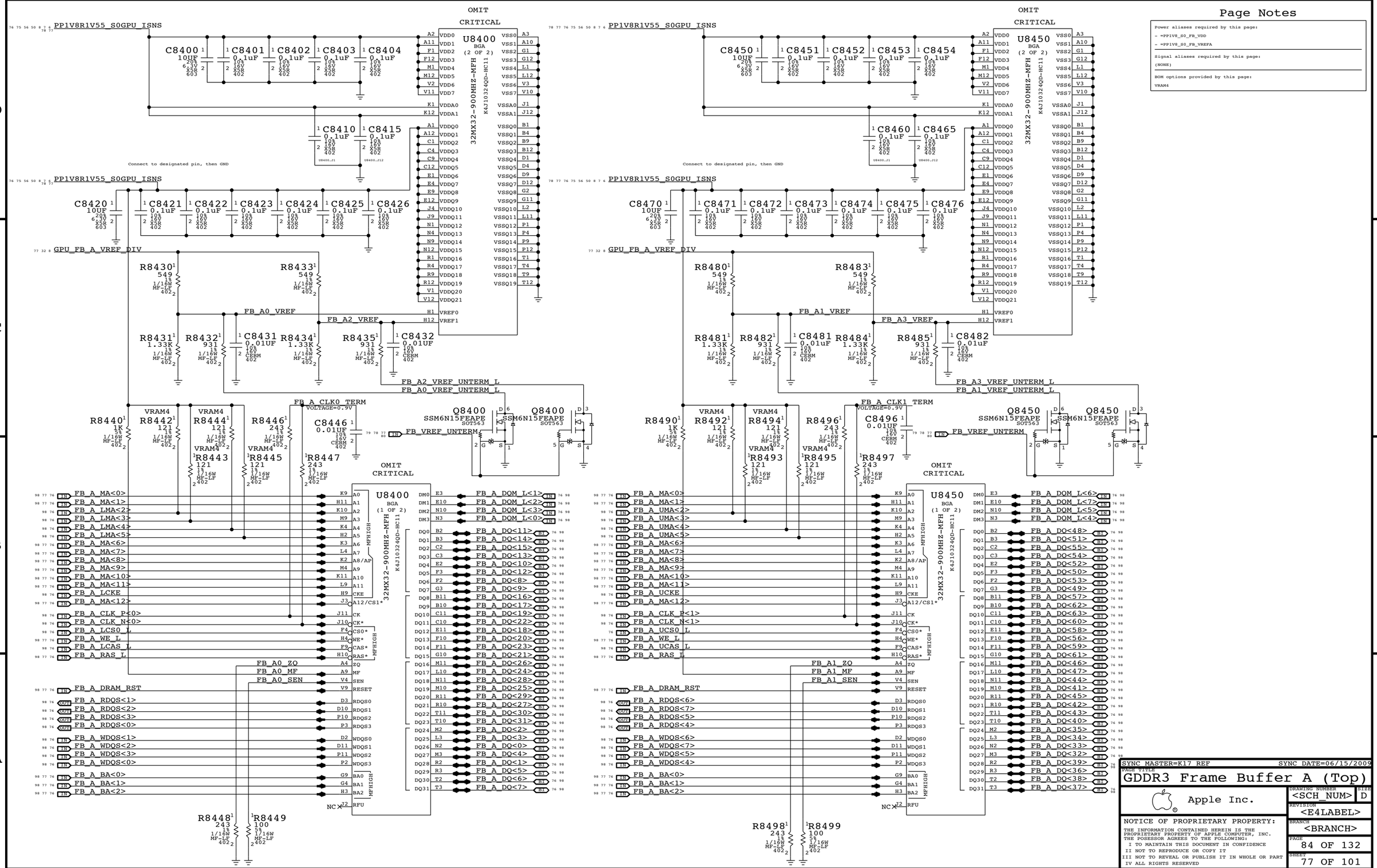

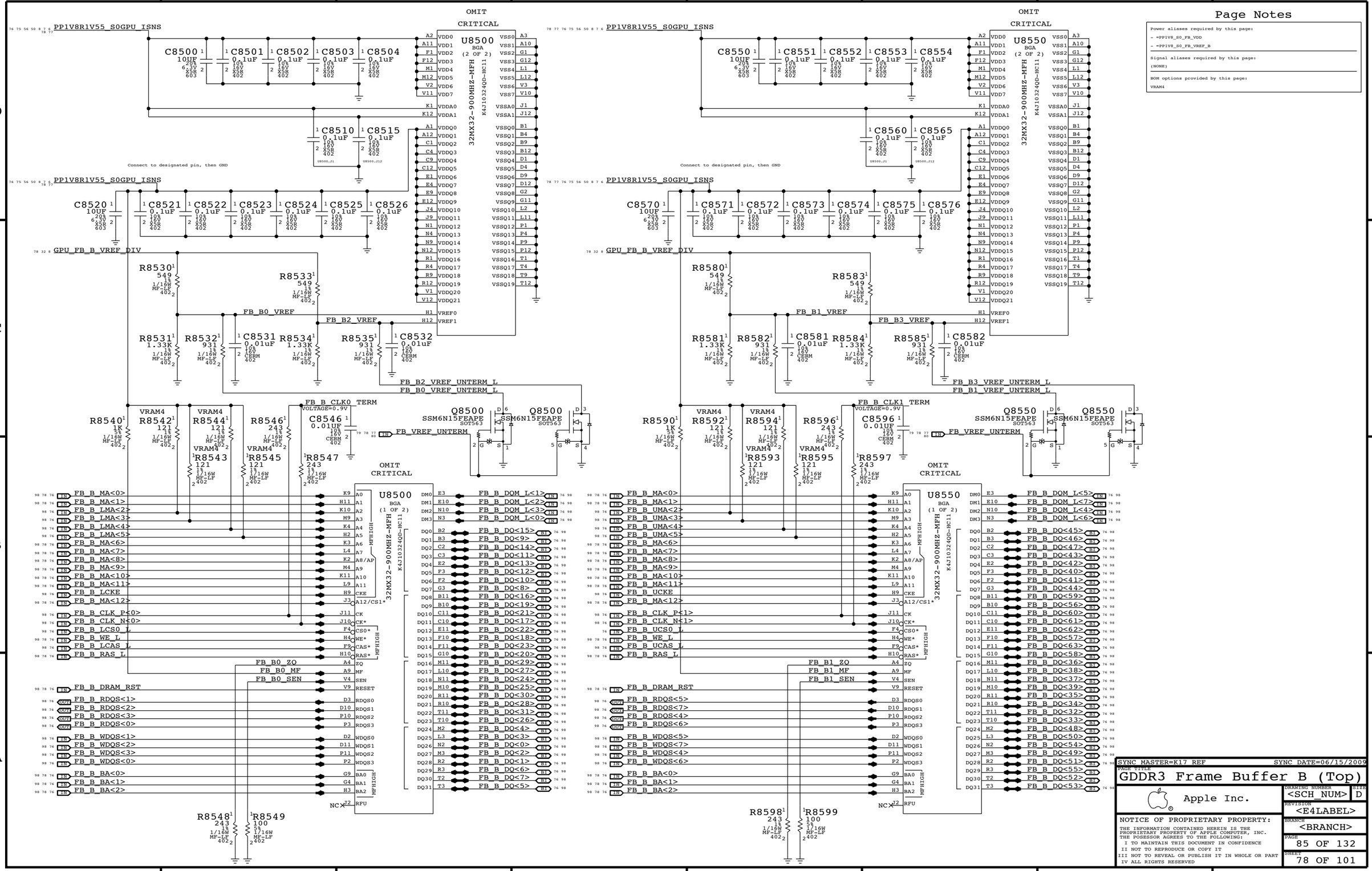

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
GDDR3 Frame Buffer B (Top)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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PP3V3_S0GPU (110mA) → J9, J10, J11, J12, J13 (VDD33)
C8694 0.1UF 20% 10V CERM 402
C8696 1UF 10% 6.3V X5R 402
C8698 4.7UF 20% 6.3V X5R-CERM1 402

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

NC_GPU_ROM_CS_L	C3	ROM_CS*
GPU_ROM_SCLK	D4	ROM_SCLK
GPU_ROM_SI	D3	ROM_SI
GPU_ROM_SO	C4	ROM_SO
GPU_STRAP_REF_3V3_PD	N9	MULTI_STRAP_REF0_GND
GPU_STRAP_REF_MIOB_PD	P9	MULTI_STRAP_REF1_GND

PP3V3_S0GPU

R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ

R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
R8619 10K 5% 1/16W MF-LF 402
R8660 10K 5% 1/16W MF-LF 402
C8617 0.1uF 10% 16V X5R 402
C8619 0.1uF 10% 16V X5R 402

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

	P9	MIOA_VDDQ_1
	R9	MIOA_VDDQ_2
	T9	MIOA_VDDQ_3
	U9	MIOA_VDDQ_4
	AA9	MIOB_VDDQ_1
	AB9	MIOB_VDDQ_2
	W9	MIOB_VDDQ_3
	Y9	MIOB_VDDQ_4
GPU_TESTMODE_PD	AP35	TESTMODE
GPU_MIOA_VREF	N5	MIOA_VREF
GPU_MIOB_VREF	AF1	MIOB_VREF
GPU_MIOA_PD_VDDQ	U5	MIOA_CAL_PD_VDDQ
GPU_MIOA_PU_GND	T5	MIOA_CAL_PU_GND
GPU_MIOB_PD_VDDQ	AA7	MIOB_CAL_PD_VDDQ
GPU_MIOB_PU_GND	AA6	MIOB_CAL_PU_GND
	AF9	SP_PLLVDD
	AE9	PLLVDD (65mA)
	AD9	VID_PLLVDD

L8635 100NH-700MA-0.14OHM 0603
PP1V05_S0GPU → PP1V1_GPU_H_PLLVDD_F (25mA)
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 1UF 10% 6.3V X5R 402

L8640 100NH-700MA-0.14OHM 0603
PP1V05_S0GPU → PP1V1_GPU_VID_PLLVDD_F (50mA)
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 1UF 10% 6.3V X5R 402
C8631 0.1uF 10% 16V X5R 402

GPU_CLK27M	B1	XTAL_IN
NC_GPU_XTALOUT	B2	XTAL_OUT
GPU_XTALOUTBUFF	D1	XTAL_OUTBUFF
GPU_CLK27M_SS	D2	XTAL_SSIN

GPU_STRAP<0>	W5	STRAP0
GPU_STRAP<1>	W7	STRAP1
GPU_STRAP<2>	V7	STRAP2

GPIO0	K1	GPU_VCORE_VID3
GPIO1	K2	DP_EG_HPD
GPIO2	K3	GPU_VCORE_VID4
GPIO3	H3	EG_LCD_PWR_EN
GPIO4	H2	EG_BKLT_EN
GPIO5	H1	GPU_VCORE_VID0
GPIO6	H4	GPU_VCORE_VID1
GPIO7	H5	GPU_VCORE_VID2
GPIO8	H6	SMC_GFX_OVERTEMP_R
GPIO9	J7	TP_GPU_GSTATE<0>
GPIO10	K4	FB_VREF_UNTERM
GPIO11	K5	GPU_GPIO_11
GPIO12	H7	SMC_GFX_THROTTLE_R
GPIO13	J4	FBVDD_ALTVO
GPIO14	J6	NC_GPU_GPIO_14
GPIO15	L1	NC_GPU_GPIO_15
GPIO16	L2	GPU_GPIO_16
GPIO17	L4	NC_GPU_GPIO_17
GPIO18	M4	NC_GPU_GPIO_18
GPIO19	L7	NC_GPU_GPIO_19
GPIO20	L5	NC_GPU_GPIO_20
GPIO21	K6	NC_GPU_GPIO_21
GPIO22	L6	NC_GPU_GPIO_22
GPIO23	M6	NC_GPU_GPIO_23

JTAG_TCK	AP14	TP_GPU_JTAG_TCK
JTAG_TDI	AN14	TP_GPU_JTAG_TDI
JTAG_TDO	AN16	TP_GPU_JTAG_TDO
JTAG_TMS	AR14	TP_GPU_JTAG_TMS
JTAG_TRST*	AP16	TP_GPU_JTAG_TRST_L
MIOA_CLKIN	N4	NC_GPU_MIOA_CLKIN
MIOA_CLKOUT	R4	NC_GPU_MIOA_CLKOUT
MIOA_CLKOUT*	T4	NC_GPU_MIOA_CLKOUT
MIOA_CTL3	P5	NC_GPU_MIOA_CTL3
MIOA_DE	N2	TP_GPU_MIOA_DE
MIOA_D0	N1	TP_GPU_MIOA_D<0>
MIOA_D1	P4	TP_GPU_MIOA_D<1>
MIOA_D2	P1	TP_GPU_MIOA_D<2>
MIOA_D3	P2	TP_GPU_MIOA_D<3>
MIOA_D4	P3	TP_GPU_MIOA_D<4>
MIOA_D5	T3	TP_GPU_MIOA_D<5>
MIOA_D6	T2	TP_GPU_MIOA_D<6>
MIOA_D7	T1	TP_GPU_MIOA_D<7>
MIOA_D8	U4	TP_GPU_MIOA_D<8>
MIOA_D9	U1	TP_GPU_MIOA_D<9>
MIOA_D10	U2	GPU_MIOA_D<10>
MIOA_D11	U3	GPU_MIOA_D<11>
MIOA_D12	R6	GPU_MIOA_D<12>
MIOA_D13	T6	GPU_MIOA_D<13>
MIOA_D14	N6	GPU_MIOA_D<14>
MIOA_HSYNC	N3	NC_GPU_MIOA_HSYNC
MIOA_VSYNC	L3	NC_GPU_MIOA_VSYNC
MIOB_CLKIN	AE1	NC_GPU_MIOB_CLKIN
MIOB_CLKOUT	V4	NC_GPU_MIOB_CLKOUT
MIOB_CLKOUT*	W4	NC_GPU_MIOB_CLKOUT
MIOB_CTL3	W3	NC_GPU_MIOB_CTL3
MIOB_DE	Y5	NC_GPU_MIOB_DE
MIOB_D0	Y1	NC_GPU_MIOB_D<0>
MIOB_D1	Y2	NC_GPU_MIOB_D<1>
MIOB_D2	Y3	NC_GPU_MIOB_D<2>
MIOB_D3	AB3	NC_GPU_MIOB_D<3>
MIOB_D4	AB2	NC_GPU_MIOB_D<4>
MIOB_D5	AB1	NC_GPU_MIOB_D<5>
MIOB_D6	AC4	NC_GPU_MIOB_D<6>
MIOB_D7	AC1	NC_GPU_MIOB_D<7>
MIOB_D8	AC2	NC_GPU_MIOB_D<8>
MIOB_D9	AC3	NC_GPU_MIOB_D<9>
MIOB_D10	AE3	NC_GPU_MIOB_D<10>
MIOB_D11	AE2	NC_GPU_MIOB_D<11>
MIOB_D12	U6	NC_GPU_MIOB_D<12>
MIOB_D13	W6	NC_GPU_MIOB_D<13>
MIOB_D14	Y6	NC_GPU_MIOB_D<14>
MIOB_HSYNC	W1	NC_GPU_MIOB_HSYNC
MIOB_VSYNC	W2	NC_GPU_MIOB_VSYNC
THERMDP	B5	GPU_TDIODE_P
THERMDN	B4	GPU_TDIODE_N

SYNC_MASTER=K17_REF
SYNC_DATE=06/15/2009

PAGE TITLE
NV GT216 GPIO/MIO/MISC

Apple Inc.

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GPIOs

GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE	79 80 82
DP_EG_HPD	HPDC	DP_EG_HPD	MAKE_BASE=TRUE	IN 79 80 84
GPU_VCORE_VID4	LCD0_BL_PWM	GPU_VCORE_VID4	MAKE_BASE=TRUE	79 80 82
EG_LCD_PWR_EN	LCD0_VDD	EG_LCD_PWR_EN	MAKE_BASE=TRUE	79 80 87
EG_BKLT_EN	LCD0_BL_EN	EG_BKLT_EN	MAKE_BASE=TRUE	79 80 87
GPU_VCORE_VID0	VID0	GPU_VCORE_VID0	MAKE_BASE=TRUE	79 80 82
GPU_VCORE_VID1	VID1	GPU_VCORE_VID1	MAKE_BASE=TRUE	79 80 82
GPU_VCORE_VID2	VID2/MEM_VID	GPU_VCORE_VID2	MAKE_BASE=TRUE	79 80 82
SMC_GFX_OVERTEMP_R_L	OVERTEMP	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE	79 80
TP_GPU_GSTATE<0>	FAN_PWM	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE	6 79 80
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM	MAKE_BASE=TRUE	77 78 79 80
GPU_GPIO_11	SLI_SYNC	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE	OUT 6
SMC_GFX_THROTTLE_R_L	PWR_CTL7	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE	OUT 79 80
FBVDD_ALTVO	PWR_CTL0	FBVDD_ALTVO	MAKE_BASE=TRUE	OUT 79 80 86
NC_GPU_GPIO_14	PWR_CTL1	NC_GPU_GPIO_14	MAKE_BASE=TRUE	79 80

GPIOs

NC_GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE	79 80
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET		80
NC_GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE	79 80
NC_GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE	79 80
NC_GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE	79 80
NC_GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE	79 80
NC_GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE	79 80
NC_GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE	79 80
NC_GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE NO_TEST=TRUE	79 80

Renamed signals

GPU_CLK27M	MAKE_BASE=TRUE	GPU_CLK27M		27 79 80 98
GPU_CLK27M_SS	MAKE_BASE=TRUE	GPU_CLK27M_SS		79 80 98
GPU_TDIODE_P	MAKE_BASE=TRUE	GPU_TDIODE_P		51 79 80 99
GPU_TDIODE_N	MAKE_BASE=TRUE	GPU_TDIODE_N		51 79 80 99
LVDS_EG_DDC_CLK	MAKE_BASE=TRUE	LVDS_EG_DDC_CLK		80 81 84
LVDS_EG_DDC_DATA	MAKE_BASE=TRUE	LVDS_EG_DDC_DATA		80 81 84
DP_EG_DDC_CLK	MAKE_BASE=TRUE	DP_EG_DDC_CLK		80 81 84
DP_EG_DDC_DATA	MAKE_BASE=TRUE	DP_EG_DDC_DATA		80 81 84

Unused signals

TP_GPU_JTAG_TCK	MAKE_BASE=TRUE	TP_GPU_JTAG_TCK		79 80
TP_GPU_JTAG_TDI	MAKE_BASE=TRUE	TP_GPU_JTAG_TDI		79 80
TP_GPU_JTAG_TDO	MAKE_BASE=TRUE	TP_GPU_JTAG_TDO		79 80
TP_GPU_JTAG_TMS	MAKE_BASE=TRUE	TP_GPU_JTAG_TMS		79 80
TP_GPU_JTAG_TRST_L	MAKE_BASE=TRUE	TP_GPU_JTAG_TRST_L		79 80
NC_FBA_MA<13>	MAKE_BASE=TRUE	NC_FBA_MA<13>	NO_TEST=TRUE	76 80
NC_FBB_MA<13>	MAKE_BASE=TRUE	NC_FBB_MA<13>	NO_TEST=TRUE	76 80

Unused I2C Buses

NC_GPU_I2CC_SCL	MAKE_BASE=TRUE	NC_GPU_I2CC_SCL	NO_TEST=TRUE	80 81
NC_GPU_I2CC_SDA	MAKE_BASE=TRUE	NC_GPU_I2CC_SDA	NO_TEST=TRUE	80 81
NC_GPU_I2CH_SCL	MAKE_BASE=TRUE	NC_GPU_I2CH_SCL	NO_TEST=TRUE	80 81
NC_GPU_I2CH_SDA	MAKE_BASE=TRUE	NC_GPU_I2CH_SDA	NO_TEST=TRUE	80 81

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

NC_FB_B_UCS1_L	MAKE_BASE=TRUE	NC_FB_B_UCS1_L	NO_TEST=TRUE	76 80
NC_FB_B_LCS1_L	MAKE_BASE=TRUE	NC_FB_B_LCS1_L	NO_TEST=TRUE	76 80
NC_GPU_ROM_CS_L	MAKE_BASE=TRUE	NC_GPU_ROM_CS_L	NO_TEST=TRUE	79 80
NC_FB_A_UCS1_L	MAKE_BASE=TRUE	NC_FB_A_UCS1_L	NO_TEST=TRUE	76 80
NC_FB_A_LCS1_L	MAKE_BASE=TRUE	NC_FB_A_LCS1_L	NO_TEST=TRUE	76 80
NC_LVDS_EG_B_CLK_P	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_P		80 81
NC_LVDS_EG_B_CLK_N	MAKE_BASE=TRUE	NC_LVDS_EG_B_CLK_N		80 81
NC_LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE	NC_LVDS_EG_A_DATA_P<3>	NO_TEST=TRUE	80 81 98
NC_LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE	NC_LVDS_EG_A_DATA_N<3>	NO_TEST=TRUE	80 81 98
NC_LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE	NC_LVDS_EG_B_DATA_P<3>	NO_TEST=TRUE	80 81 98
NC_LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE	NC_LVDS_EG_B_DATA_N<3>	NO_TEST=TRUE	80 81 98

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKOUT_P	NO_TEST=TRUE	79 80
NC_GPU_MIOA_CLKOUT_N	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKOUT_N	NO_TEST=TRUE	79 80
NC_GPU_MIOA_CTL3	MAKE_BASE=TRUE	NC_GPU_MIOA_CTL3	NO_TEST=TRUE	79 80
TP_GPU_MIOA_DE	MAKE_BASE=TRUE	TP_GPU_MIOA_DE		6 79 80
TP_GPU_MIOA_D<9..0>	MAKE_BASE=TRUE	GPU_MIOA_D<9..0>		6 79
NC_GPU_MIOA_CLKIN	MAKE_BASE=TRUE	NC_GPU_MIOA_CLKIN	NO_TEST=TRUE	79 80
NC_GPU_MIOA_D<14..10>	MAKE_BASE=TRUE	GPU_MIOA_D<14..10>	NO_TEST=TRUE	79
NC_GPU_MIOA_HSYNC	MAKE_BASE=TRUE	NC_GPU_MIOA_HSYNC	NO_TEST=TRUE	79 80
NC_GPU_MIOA_VSYNC	MAKE_BASE=TRUE	NC_GPU_MIOA_VSYNC	NO_TEST=TRUE	79 80
NC_GPU_MIOB_CLKIN	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKIN	NO_TEST=TRUE	79 80
NC_GPU_MIOB_CLKOUT_P	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKOUT_P	NO_TEST=TRUE	79 80
NC_GPU_MIOB_CLKOUT_N	MAKE_BASE=TRUE	NC_GPU_MIOB_CLKOUT_N	NO_TEST=TRUE	79 80
NC_GPU_MIOB_CTL3	MAKE_BASE=TRUE	NC_GPU_MIOB_CTL3	NO_TEST=TRUE	79 80
NC_GPU_MIOB_DE	MAKE_BASE=TRUE	NC_GPU_MIOB_DE	NO_TEST=TRUE	79 80
NC_GPU_MIOB_D<14..0>	MAKE_BASE=TRUE	GPU_MIOB_D<14..0>	NO_TEST=TRUE	
NC_GPU_MIOB_VSYNC	MAKE_BASE=TRUE	NC_GPU_MIOB_VSYNC	NO_TEST=TRUE	79 80
NC_GPU_MIOB_HSYNC	MAKE_BASE=TRUE	NC_GPU_MIOB_HSYNC	NO_TEST=TRUE	79 80

Config Straps

PP3V3_S0GPU

R8707[1] 2.0K 5% 1/16W MF-LF 402 — OMIT
R8709[1] 4.99K 1% 1/16W MF-LF 402 — NO STUFF
R8711[1] 15.0K 1% 1/16W MF-LF 402 — NO STUFF

79 OUT GPU_ROM_SI
79 IN GPU_ROM_SO
79 IN GPU_ROM_SCLK

R8708[1] 45.3K 1% 1/16W MF-LF 402 — OMIT
R8710[1] 10K 1% 1/16W MF-LF 402
R8712[1] 15.0K 1% 1/16W MF-LF 402

Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0]	PU/PD	Rval
0 0000	PD	5k
1 0001	PD	10k
2 0010	PD	15k (HYN 256)
3 0011	PD	20k (SAM 256)
4 0100	PD	25k (SAM 512)
5 0101	PD	30k
6 0110	PD	35k (HYN 512)
7 0111	PD	45k

Strap S1/S2 Bit[3:0]	PU/PD	Rval
8 1000	PU	5k
9 1001	PU	10k
A 1010	PU	15k
B 1011	PU	20k
C 1100	PU	25k
D 1101	PU	30k
E 1110	PU	35k
F 1111	PU	45k

PCI_DEVID[4:0]=0x14

PP3V3_S0GPU

R8701[1] 45.3K 1% 1/16W MF-LF 402 — GPU_STRAP<0>
R8703[1] 34.8K 1% 1/16W MF-LF 402 — GPU_STRAP<1>
R8705[1] 10K 1% 1/16W MF-LF 402 — GPU_STRAP<2>

R8702[1] 2.0K 5% 1/16W MF-LF 402 — NO STUFF
R8704[1] 10K 1% 1/16W MF-LF 402 — NO STUFF
R8706[1] 24.9K 1% 1/16W MF-LF 402 — NO STUFF

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0353	1	RES,MTL FILM,1/16W,24.9K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX

PP3V3_S0

PP3V3_S0GPU

R8750[1] 2.2K 5% 1/16W MF-LF 402
R8751[1] 2.2K 5% 1/16W MF-LF 402
R8752[1] 4.7K 5% 1/16W MF-LF 402
R8753[1] 4.7K 5% 1/16W MF-LF 402

84 81 80 IN DP_EG_DDC_CLK
84 81 80 IN DP_EG_DDC_DATA
84 18 8 IN DP_IG_DDC_CLK
84 18 8 IN DP_IG_DDC_DATA

PP3V3_S0GPU

DP_CA_DET_EG_FET
R8742[1] 100K 1% 1/16W MF-LF 402
Q8742 SOD-VESM-HF SSM3K15FV

80 EG_DP_CA_DET — DP_CA_DET — IN 84 85 87

R8743 0 5% 1/16W MF-LF 402 — DP_CA_DET_EG — IN 87

DP_CA_DET_EG_PLD

Isolation FETs for DP MUX inputs

PP3V3_S0GPU

R8796[1] 2.2K 5% 1/16W MF-LF 402
R8797[1] 2.2K 5% 1/16W MF-LF 402

80 79 SMC_GFX_OVERTEMP_R_L — R8798 0 5% 1/16W MF-LF 402 NO STUFF — SMC_GFX_OVERTEMP_L OUT 45
80 79 SMC_GFX_THROTTLE_R_L — R8799 0 5% 1/16W MF-LF 402 — SMC_GFX_THROTTLE_L OUT 45

EG_LCD_PWR_EN OUT 79 80 87
EG_BKLT_EN OUT 79 80 87
FBVDD_ALTVO OUT 79 80 86
FB_VREF_UNTERM OUT 77 78 79 80

R8792[1] 10K 5% 1/16W MF-LF 402
R8793[1] 10K 5% 1/16W MF-LF 402
R8794[1] 10K 5% 1/16W MF-LF 402
R8795[1] 10K 5% 1/16W MF-LF 402 — NO STUFF

Unused Clocks

98 80 79 GPU_CLK27M_SS
79 GPU_XTALOUTBUFF

R8780[1] 10K 5% 1/16W MF-LF 402 — GPU_SS_INT
R8781[1] 10K 5% 1/16W MF-LF 402

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GT216 GPIOS & STRAPS

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

72 7 6 PP1V8_GPUIFPX → L8800 CRITICAL 300-OHM-0.5A 0603-1
7mA peak per diff pair
7mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402 — Place at AG9
C8803 0.1UF 20% 10V CERM 402 — Place at AG10
PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

81 79 76 74 7 6 PP1V05_S0GPU → L8805 180-OHM-1.5A 0603
80mA peak
C8805 4.7UF 20% 6.3V CERM 603
C8806 1UF 20% 6.3V CERM 402
PP1V1_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V

GPU_IFPEF_RSET 81
GPU_IFPC_RSET 81
GPU_IFPAB_RSET 81
GPU_IFPD_RSET 81

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402
R8858 1K 1% 1/16W MF-LF 402

86 81 79 76 74 7 6 PP1V05_S0GPU → L8810 180-OHM-1.5A 0603
7mA peak per diff pair
7mA peak for all pairs
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402 — Place at AJ8
C8813 0.1UF 20% 10V CERM 402 — Place at AK8
PP1V1_GPU_IFPCD_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

84 82 81 80 79 74 72 7 6 PP3V3_S0GPU → L8815 CRITICAL 300-OHM-0.5A 0603-1
160mA peak
C8815 4.7UF 20% 6.3V CERM 603
C8816 1UF 20% 6.3V CERM 402
PP3V3_GPU_IFPC_PLLVDD_F 81
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

PP1V8_GPU_IFPD_PLLVDD_F 81
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V
Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT

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AG9	IFPA_IOVDD		
AG10	IFPB_IOVDD		
AJ8	IFPC_IOVDD	← 81 PP1V1_GPU_IFPCD_IOVDD_F	
AK8	IFPD_IOVDD		
AE7	IFPE_IOVDD	← 81 PP1V1_GPU_IFPEF_IOVDD_F	
AD7	IFPF_IOVDD		
AK9	IFPAB_PLLVDD		
AJ11	IFPAB_RSET	← 81 GPU_IFPAB_RSET	
AJ9	IFPC_PLLVDD	← 81 PP3V3_GPU_IFPC_PLLVDD_F	
AK7	IFPC_RSET	← 81 GPU_IFPC_RSET	
AJ6	IFPEF_PLLVDD	← 81 PP1V8_GPU_IFPEF_PLLVDD_F	
AL1	IFPEF_RSET	← 81 GPU_IFPEF_RSET	
G1	I2CA_SCL	← 84 86 B1 LVDS_EG_DDC_CLK	
G4	I2CA_SDA	← 84 86 B1 LVDS_EG_DDC_DATA	
E3	I2CC_SCL	← 85 B1 NC_GPU_I2CC_SCL	
E4	I2CC_SDA	← 85 B1 NC_GPU_I2CC_SDA	
E2	I2CS_SCL	← 97 51 48 45 B1 SMBUS_SMC_0_S0_SCL	
E1	I2CS_SDA	← 97 51 48 45 B1 SMBUS_SMC_0_S0_SDA	
F6	I2CH_SCL	← 85 B1 NC_GPU_I2CH_SDA	
G6	I2CH_SDA	← 85 B1 NC_GPU_I2CH_SCL	
G3	I2CB_SCL	← 84 86 B1 DP_EG_DDC_CLK	
G2	I2CB_SDA	← 84 86 B1 DP_EG_DDC_DATA	
AJ12	DACA_VDD		
AK12	DACA_VREF		
AK13	DACA_RSET		
AG7	DACB_VDD		
AK6	DACB_VREF		
AJ7	DACB_RSET		
AC6	IFPD_PLLVDD		
AB6	IFPD_RSET	← 81 GPU_IFPD_RSET	

AM11	IFPA_TXC	→ LVDS_EG_A_CLK_P 87 98
AM12	IFPA_TXC*	→ LVDS_EG_A_CLK_N 87 98
AM8	IFPA_TXD0	→ LVDS_EG_A_DATA_P<0> 87 98
AL8	IFPA_TXD0*	→ LVDS_EG_A_DATA_N<0> 87 98
AM10	IFPA_TXD1	→ LVDS_EG_A_DATA_P<1> 87 98
AM9	IFPA_TXD1*	→ LVDS_EG_A_DATA_N<1> 87 98
AK10	IFPA_TXD2	→ LVDS_EG_A_DATA_P<2> 87 98
AL10	IFPA_TXD2*	→ LVDS_EG_A_DATA_N<2> 87 98
AK11	IFPA_TXD3	→ NC_LVDS_EG_A_DATA_P<3> 80 98
AL11	IFPA_TXD3*	→ NC_LVDS_EG_A_DATA_N<3> 80 98
AP13	IFPB_TXC	→ NC_LVDS_EG_B_CLK_P 80
AN13	IFPB_TXC*	→ NC_LVDS_EG_B_CLK_N 80
AN8	IFPB_TXD4	→ LVDS_EG_B_DATA_P<0> 87 98
AP8	IFPB_TXD4*	→ LVDS_EG_B_DATA_N<0> 87 98
AP10	IFPB_TXD5	→ LVDS_EG_B_DATA_P<1> 87 98
AN10	IFPB_TXD5*	→ LVDS_EG_B_DATA_N<1> 87 98
AR11	IFPB_TXD6	→ LVDS_EG_B_DATA_P<2> 87 98
AR10	IFPB_TXD6*	→ LVDS_EG_B_DATA_N<2> 87 98
AN11	IFPB_TXD7	→ NC_LVDS_EG_B_DATA_P<3> 80 98
AP11	IFPB_TXD7*	→ NC_LVDS_EG_B_DATA_N<3> 80 98
AP2	IFPC_AUX_I2CW_SCL	→ DP_EG_AUX_CH_P 84 98
AN3	IFPC_AUX_I2CW_SDA*	→ DP_EG_AUX_CH_N 84 98
AM7	IFPC_L0	→ DP_EG_ML_P<0> 84 98
AM6	IFPC_L0*	→ DP_EG_ML_N<0> 84 98
AL5	IFPC_L1	→ DP_EG_ML_P<1> 84 98
AM5	IFPC_L1*	→ DP_EG_ML_N<1> 84 98
AM3	IFPC_L2	→ DP_EG_ML_P<2> 84 98
AM4	IFPC_L2*	→ DP_EG_ML_N<2> 84 98
AP1	IFPC_L3	→ DP_EG_ML_P<3> 84 98
AR2	IFPC_L3*	→ DP_EG_ML_N<3> 84 98
AR4	IFPD_AUX_I2CX_SCL	→ NC
AN4	IFPD_AUX_I2CX_SDA*	→ NC
AR8	IFPD_L0	→ NC
AR7	IFPD_L0*	→ NC
AP7	IFPD_L1	→ NC
AP6	IFPD_L1*	→ NC
AR5	IFPD_L2	→ NC
AR6	IFPD_L2*	→ NC
AP5	IFPD_L3	→ NC
AR3	IFPD_L3*	→ NC
AK4	IFPE_AUX_I2CY_SCL	→ NC
AK3	IFPE_AUX_I2CY_SDA*	→ NC
AK2	IFPE_L0	→ NC
AK1	IFPE_L0*	→ NC
AJ4	IFPE_L1	→ NC
AJ3	IFPE_L1*	→ NC
AJ2	IFPE_L2	→ NC
AJ1	IFPE_L2*	→ NC
AH2	IFPE_L3	→ NC
AH1	IFPE_L3*	→ NC
AF4	IFPF_AUX_I2CZ_SCL	→ NC
AF3	IFPF_AUX_I2CZ_SDA*	→ NC
AF2	IFPF_L0	→ NC
AF1	IFPF_L0*	→ NC
AE2	IFPF_L1	→ NC
AE1	IFPF_L1*	→ NC
AD2	IFPF_L2	→ NC
AD1	IFPF_L2*	→ NC
AC2	IFPF_L3	→ NC
AC1	IFPF_L3*	→ NC
AM15	DACA_RED	→ NC
AM14	DACA_GREEN	→ NC
AL14	DACA_BLUE	→ NC
AM13	DACA_HSYNC	→ NC
AL13	DACA_VSYNC	→ NC
AK5	DACB_RED	→ NC
AL4	DACB_GREEN	→ NC
AL3	DACB_BLUE	→ NC
AB5	CEC	→ GPU_CEC
AH4	DACB_HSYNC	→ NC
AH3	DACB_VSYNC	→ NC

NO STUFF R8861 1K 5% 1/16W MF-LF 402
NO STUFF R8860 1K 5% 1/16W MF-LF 402

PP3V3_S0GPU → R8859 10K 5% 1/16W MF-LF 402 → GPU_CEC

GPU_DACA_VDD
GPU_DACB_VDD
PP1V8_GPU_IFPD_PLLVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.8V

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009
PAGE TITLE
NV GT216 VIDEO INTERFACES

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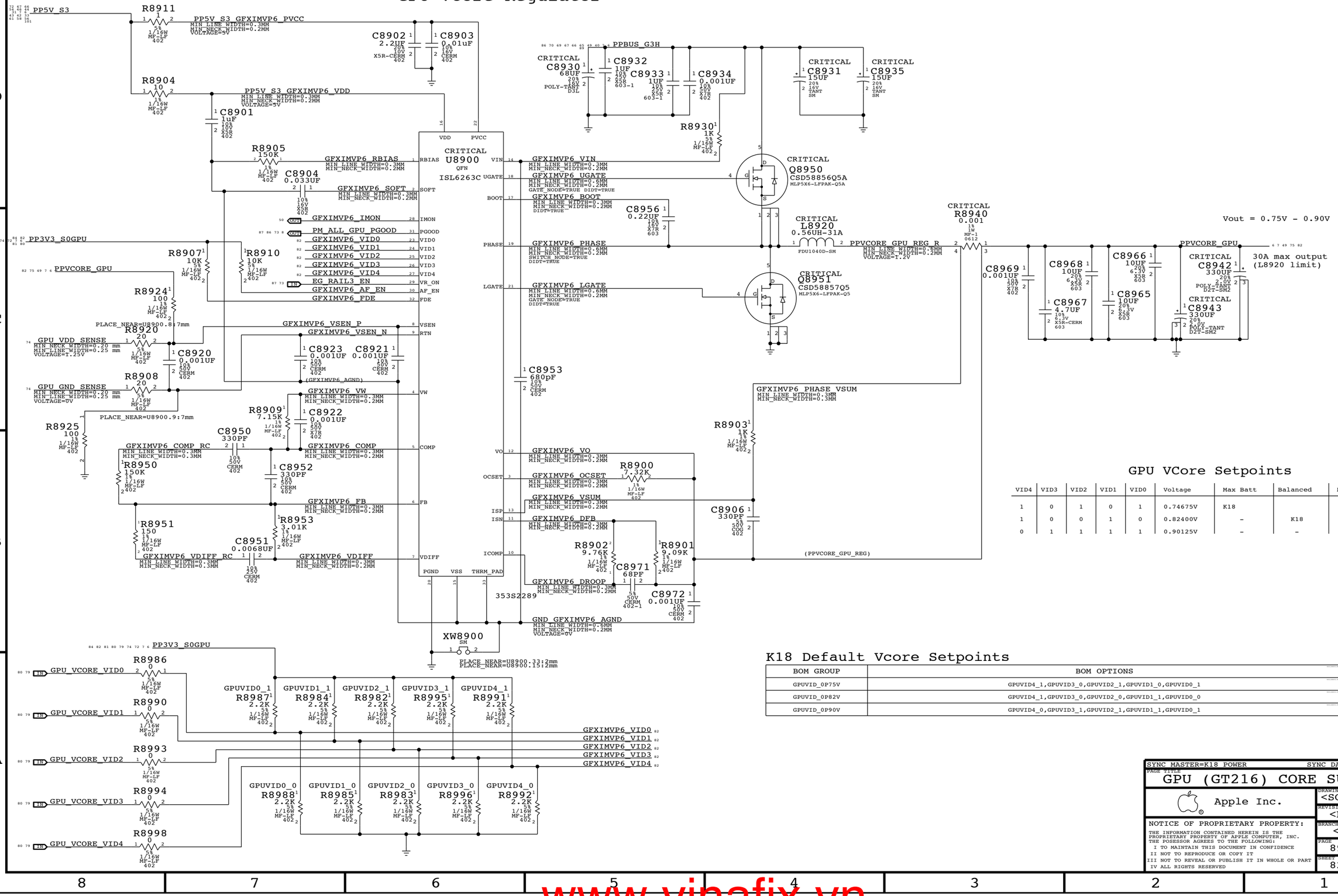
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

K18 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P75V	GPUVID4_1,GPUVID3_0,GPUVID2_1,GPUVID1_0,GPUVID0_1
GPUVID_0P82V	GPUVID4_1,GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_0P90V	GPUVID4_0,GPUVID3_1,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K18_POWER SYNC_DATE=07/14/2009

PAGE TITLE

GPU (GT216) CORE SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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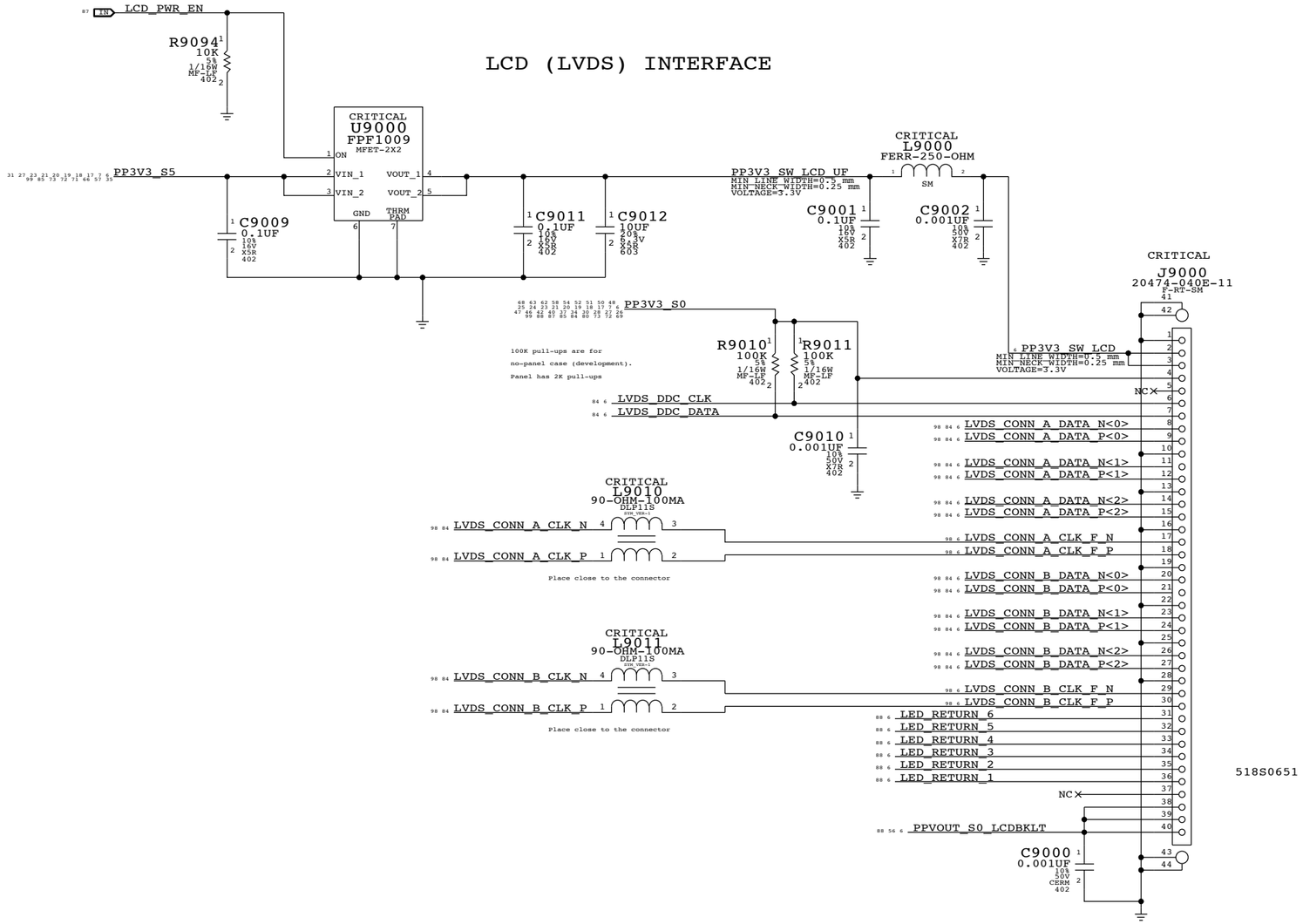
LCD (LVDS) INTERFACE



518S0651

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE: LVDS Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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LVDS Transmitter Termination

All emulated LVDS outputs require this termination

PLACE_NEAR=U9600.A6:7mm
R9320 357 1% 1/16W MF-LF 402
LVDS_A_CLK_P → LVDS_CONN_A_CLK_P

PLACE_NEAR=U9600.A7:7mm
R9322 357 1% 1/16W MF-LF 402
LVDS_A_CLK_N → LVDS_CONN_A_CLK_N

PLACE_NEAR=U9600.A8:7mm
R9325 357 1% 1/16W MF-LF 402
LVDS_A_DATA_P<0> → LVDS_CONN_A_DATA_P<0>

PLACE_NEAR=U9600.B9:7mm
R9327 357 1% 1/16W MF-LF 402
LVDS_A_DATA_N<0> → LVDS_CONN_A_DATA_N<0>

PLACE_NEAR=U9600.A9:7mm
R9330 357 1% 1/16W MF-LF 402
LVDS_A_DATA_P<1> → LVDS_CONN_A_DATA_P<1>

PLACE_NEAR=U9600.C10:7mm
R9332 357 1% 1/16W MF-LF 402
LVDS_A_DATA_N<1> → LVDS_CONN_A_DATA_N<1>

PLACE_NEAR=U9600.B10:7mm
R9335 357 1% 1/16W MF-LF 402
LVDS_A_DATA_P<2> → LVDS_CONN_A_DATA_P<2>

PLACE_NEAR=U9600.A10:7mm
R9337 357 1% 1/16W MF-LF 402
LVDS_A_DATA_N<2> → LVDS_CONN_A_DATA_N<2>

PLACE_NEAR=U9600.C8:7mm
R9340 357 1% 1/16W MF-LF 402
LVDS_B_CLK_P → LVDS_CONN_B_CLK_P

PLACE_NEAR=U9600.C9:7mm
R9342 357 1% 1/16W MF-LF 402
LVDS_B_CLK_N → LVDS_CONN_B_CLK_N

PLACE_NEAR=U9600.A2:7mm
R9345 357 1% 1/16W MF-LF 402
LVDS_B_DATA_P<0> → LVDS_CONN_B_DATA_P<0>

PLACE_NEAR=U9600.A3:7mm
R9347 357 1% 1/16W MF-LF 402
LVDS_B_DATA_N<0> → LVDS_CONN_B_DATA_N<0>

PLACE_NEAR=U9600.A1:7mm
R9350 357 1% 1/16W MF-LF 402
LVDS_B_DATA_P<1> → LVDS_CONN_B_DATA_P<1>

PLACE_NEAR=U9600.B3:7mm
R9352 357 1% 1/16W MF-LF 402
LVDS_B_DATA_N<1> → LVDS_CONN_B_DATA_N<1>

PLACE_NEAR=U9600.C5:7mm
R9355 357 1% 1/16W MF-LF 402
LVDS_B_DATA_P<2> → LVDS_CONN_B_DATA_P<2>

PLACE_NEAR=U9600.A5:7mm
R9357 357 1% 1/16W MF-LF 402
LVDS_B_DATA_N<2> → LVDS_CONN_B_DATA_N<2>

DisplayPort Mux

PP3V3_S0

U9320 CBTL06141EE BGA CRITICAL

DP_IG_ML_P<0> → DIN1_0+ (B4)
DP_IG_ML_N<0> → DIN1_0- (A4)
DP_IG_ML_P<1> → DIN1_1+ (B5)
DP_IG_ML_N<1> → DIN1_1- (A5)
DP_IG_ML_P<2> → DIN1_2+ (B6)
DP_IG_ML_N<2> → DIN1_2- (A6)
DP_IG_ML_P<3> → DIN1_3+ (A8)
DP_IG_ML_N<3> → DIN1_3- (A9)
DP_IG_AUX_CH_P → C9330 0.1uF → DAUX1+ (H9)
DP_IG_AUX_CH_N → C9331 0.1uF → DAUX1- (J9)
DP_IG_DDC_CLK → DDC_CLK1 (H8)
DP_IG_DDC_DATA → DDC_DAT1 (J8)
DP_IG_HPD → R9304 100K → HPD_1 (J2)

DP_EG_ML_P<0> → DIN2_0+ (B8)
DP_EG_ML_N<0> → DIN2_0- (B9)
DP_EG_ML_P<1> → DIN2_1+ (D8)
DP_EG_ML_N<1> → DIN2_1- (D9)
DP_EG_ML_P<2> → DIN2_2+ (E8)
DP_EG_ML_N<2> → DIN2_2- (E9)
DP_EG_ML_P<3> → DIN2_3+ (F8)
DP_EG_ML_N<3> → DIN2_3- (F9)
DP_EG_AUX_CH_P → C9335 0.1uF → DAUX2+ (H6)
DP_EG_AUX_CH_N → C9336 0.1uF → DAUX2- (J6)
DP_EG_DDC_CLK → DDC_CLK2 (H5)
DP_EG_DDC_DATA → DDC_DAT2 (J5)
DP_EG_HPD → R9305 100K → HPD_2 (H3)

LO=PORT1 HI=PORT2 → GPU_SEL (A1)
DP_MUX_SEL_EG
DP_MUX_XSD_L → XSD* (B7)
LO=AUX_CH HI=DDC → DDC_AUX_SEL (C2)
DP_CA_DET
TST0 (G2)

DPMUX_EN_HPD
R9301 10K 1% 1/16W MF-LF 402
C9301 1UF 10% 6.3V CERM-X5R 402

PP3V3_S0
DPMUX_EN_S0&DPMUX_EN_PLD
R9302 10K 1% 1/16W MF-LF 402
DPMUX_EN_PLD
R9303 0 5% 1/16W MF-LF 402
DP_MUX_EN
DP_HOTPLUG_DET
MAKE_BASE=TRUE

C9320 0.1UF 20% 10V CERM 402
C9321 0.1UF 20% 10V CERM 402
VDD

DOUT_0+ (B2) → DP_ML_P<0>
DOUT_0- (B1) → DP_ML_N<0>
DOUT_1+ (D2) → DP_ML_P<1>
DOUT_1- (D1) → DP_ML_N<1>
DOUT_2+ (E2) → DP_ML_P<2>
DOUT_2- (E1) → DP_ML_N<2>
DOUT_3+ (F2) → DP_ML_P<3>
DOUT_3- (F1) → DP_ML_N<3>
AUX+ (H2) → DP_AUX_CH_C_P
AUX- (H1) → DP_AUX_CH_C_N
PLACE_NEAR=U9320.J1:3mm

HPDIN (J1) ← DP_HPD_R ← R9307 1K 5% 1/16W MF-LF 402 ← DP_HOTPLUG_DET

GND: B3, C8, G8, H4, H7

LVDS DDC MUX

PP3V3_S0GPU
PP3V3_S0

R9370 20K 5% 1/16W MF-LF 402
R9371 20K 5% 1/16W MF-LF 402
R9372 20K 5% 1/16W MF-LF 402
R9373 20K 5% 1/16W MF-LF 402
C9370 0.1UF 20% 10V CERM 402

U9370 SN74LV4066A QFN1 CRITICAL
VCC (14), GND (7), THRM (15)

LVDS_DDC_SEL_EG → C1
LVDS_DDC_SEL_IG → C2
C3
C4

A1/B1 ↔ LVDS_EG_DDC_CLK
A2/B2 ↔ LVDS_IG_DDC_CLK / LVDS_DDC_CLK
A3/B3 ↔ LVDS_EG_DDC_DATA
A4/B4 ↔ LVDS_IG_DDC_DATA / LVDS_DDC_DATA

SYNC_MASTER=K17_REF	SYNC_DATE=06/15/2009
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Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23

PP3V3_S5
PM_SLP_S3_L
TP_DPPWR_OC_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

L9400
FERR-120-OHM-3A
0603

PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

C9400 0.01UF 20% 50V CERM 603

C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 10V CERM 402
C9485 0.1UF 20% 10V CERM 402
CRITICAL C9486 22UF 20% 6.3V X5R-CERM 603
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

R9420 100K 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402
R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402

HDMI_CEC

R9425 1M 5% 1/16W MF-LF 402

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402

CRITICAL FL9403 12-OHM-100MA TCM1210-4SM

DP_ML_P<3> C9414 0.1uF 10% 16V X5R 402 DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF 10% 16V X5R 402 DP_ML_C_N<3>

DP_ML_CONN_P<3>
DP_ML_CONN_N<3>

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
	HOT_PLUG_DETECT	GND
	CONFIG1	ML_LANE0P
	CONFIG2	ML_LANE0N
	GND	GND
	ML_LANE3P	ML_LANE1P
	ML_LANE3N	ML_LANE1N
	GND	GND
	AUX_CHP	ML_LANE2P
	AUX_CHN	ML_LANE2N
	DP_PWR	RETURN
	SHIELD PINS	

DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

FL9401 12-OHM-100MA TCM1210-4SM
FL9402 12-OHM-100MA TCM1210-4SM
CRITICAL FL9400 12-OHM-100MA TCM1210-4SM

DP_ML_C_P<0> C9410 0.1uF 10% 16V X5R 402 DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF 10% 16V X5R 402 DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF 10% 16V X5R 402 DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF 10% 16V X5R 402 DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF 10% 16V X5R 402 DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF 10% 16V X5R 402 DP_ML_N<2>

DP_AUX_CH_C_P
DP_AUX_CH_C_N

PP3V3_S0

R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
R9421 100K 5% 1/16W MF-LF 402

DP_CA_DET

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q

Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1

R9422 1M 5% 1/16W MF-LF 402

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

PP3V3_S0

R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402

DP_HOTPLUG_DET

Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q

Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/16W MF-LF 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

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DisplayPort Connector

Apple Inc.

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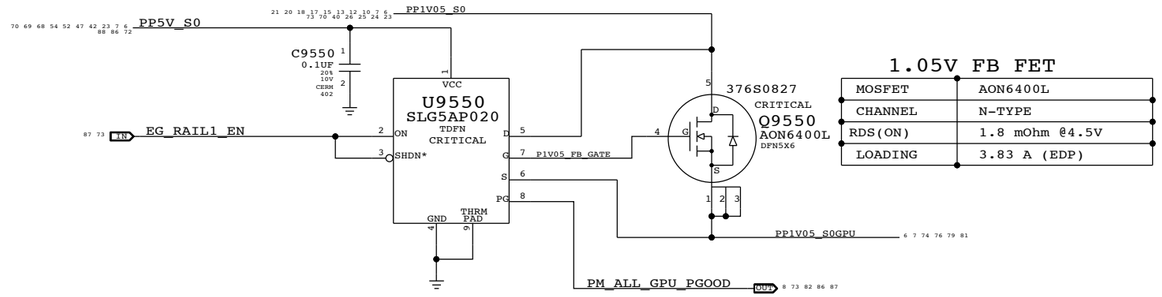
1V05 S0 GPU FET

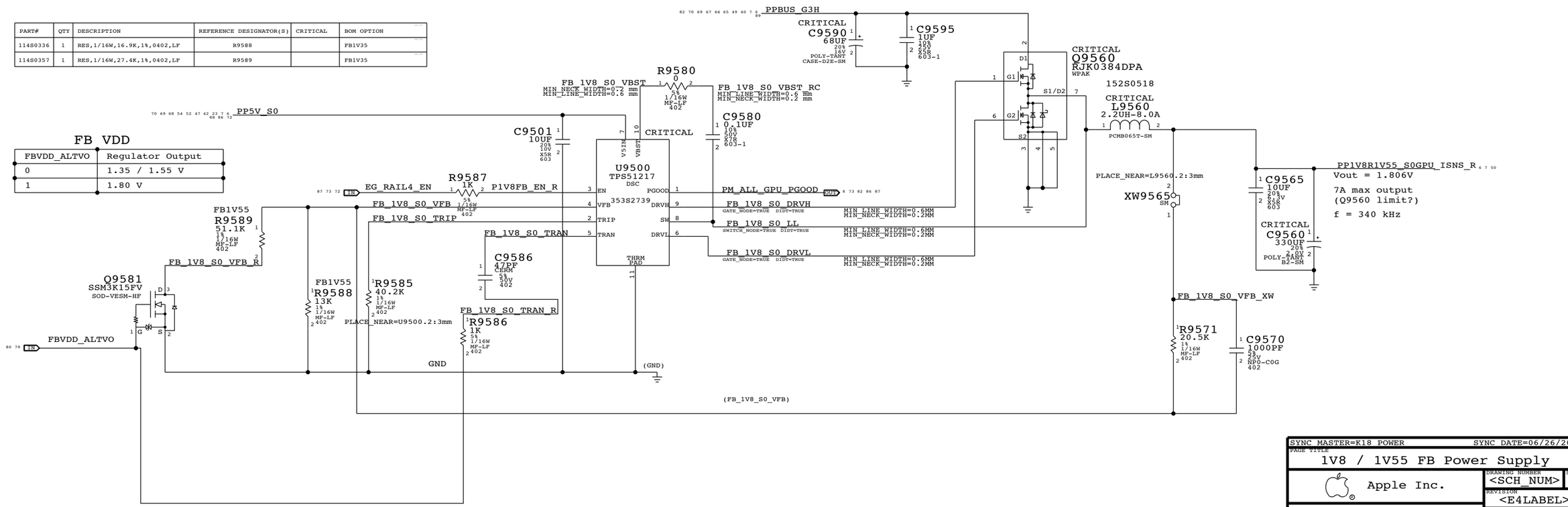


1.05V FB FET	
MOSFET	AON6400L
CHANNEL	N-TYPE
RDS(ON)	1.8 mOhm @4.5V
LOADING	3.83 A (EDP)

1V8 / 1V55 / 1V35 S0 FRAMEBUFFER REGULATOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0336	1	RES,1/16W,16.9K,1%,0402,LF	R9588		FB1V35
114S0357	1	RES,1/16W,27.4K,1%,0402,LF	R9589		FB1V35

FB_VDD	
FBVDD_ALTVO	Regulator Output
0	1.35 / 1.55 V
1	1.80 V



SYNC_MASTER=K18_POWER SYNC_DATE=06/26/2009

PAGE TITLE

1V8 / 1V55 FB Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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GMUX CPLD

R9600 0 5% 1/16W MF-LF 402 — PP3V3_S0

C9610 0.1UF 20% 10V CERM 402 — PP3V3_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V)

C9621 0.1UF 20% 10V CERM 402

C9622 0.1UF 20% 10V CERM 402

C9623 0.1UF 20% 10V CERM 402

C9624 0.1UF 20% 10V CERM 402

C9625 0.1UF 20% 10V CERM 402

C9626 0.1UF 20% 10V CERM 402

C9627 0.1UF 20% 10V CERM 402

C9628 0.1UF 20% 10V CERM 402

C9629 0.1UF 20% 10V CERM 402

R9610 0 5% 1/16W MF-LF 402 — PP1V8_S0

C9611 0.1UF 20% 10V CERM 402 — PP1V8_S0_GMUX_R (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=1.8V)

C9612 0.1UF 20% 10V CERM 402

C9613 0.1UF 20% 10V CERM 402

C9614 0.1UF 20% 10V CERM 402

C9615 0.1UF 20% 10V CERM 402

C9616 0.1UF 20% 10V CERM 402

C9617 0.1UF 20% 10V CERM 402

PP1V2_S0

C9600 4.7UF 20% 10V X5R 402 — C9604 0.1UF 20% 10V CERM 402 — C9605 0.1UF 20% 10V CERM 402 — C9606 0.1UF 20% 10V CERM 402 — C9607 0.1UF 20% 10V CERM 402 — C9608 0.1UF 20% 10V CERM 402 — C9609 0.1UF 20% 10V CERM 402

PP3V3_S0

R9640 10K 1% 1/16W MF-LF 402

R9645 10K 1% 1/16W MF-LF 402

NO STUFF R9641 10K 1% 1/16W MF-LF 402

NO STUFF R9646 10K 1% 1/16W MF-LF 402

CRITICAL
J9600
1909782
M-RT-SM
GMUX_JTAG_CONN

1	PP3V3_S0	
2	JTAG_GMUX_TDO	87
3	JTAG_GMUX_TDI	19 87
4	JTAG_GMUX_TMS	19 87
5		
6	JTAG_GMUX_TCK	20 25 87
7		
8		

NO STUFF R9647 10K 1% 1/16W MF-LF 402

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

PP3V3_S0 — NO STUFF R9670 10K 1% 1/16W MF-LF 402 — GMUX_VSYNC 87 88

U9600 XP25-5 CSBGA

OMIT CRITICAL

VCC: B11 C4 J3 J13 N11 P8
VCCAUX: C11 J2 J14 M8
VCCIO00: B5
VCCIO01: B7
VCCIO02: A12
VCCIO03: C14
VCCIO04: F13
VCCIO05: M12
VCCIO06: M9
VCCIO07: M3
VCCJ: N5 M1 C3 F2 K12
ULC_VCCPLL: A4
LRC_VCCPLL: P11

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	
JTAG_GMUX_TDO	K13	TDO	
JTAG_GMUX_TMS	L12	TMS	
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB7A	BANK5
LCD_BKLT_PWM	N2	PB7B	
LVDS_DDC_SEL_EG	P4	PB14A	
LVDS_DDC_SEL_IG	N4	PB14B	
DP_MUX_EN	N3	PB15A (OD)	
DP_MUX_SEL_EG	M4	PB15B	
EG_RESET_L	P5	PB16A	
EG_RAIL1_EN	M5	PB16B	
EG_RAIL2_EN	P6	PB17A	
EG_RAIL3_EN	M6	PB17B	
EG_RAIL4_EN	P7	PB18A	
PEG_CLKREQ_L	M7	PB18B (OD)	
DP_CA_DET_EG	N7	PB19A	
LCD_PWR_EN	N8	PB19B	
LPC_AD<0>	P9	PB20A	BANK4
LPC_AD<1>	N9	PB20B	
LPC_AD<2>	P10	PB26A	
LPC_AD<3>	M10	PB26B	
LPC_FRAME_L	P12	PB27A	
LPCPLUS_RESET_L	P13	PB27B	
LPC_CLK33M_GMUX	N12	PB28A	
GMUX_INT	P14	PB28B	
LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK6
LVDS_IG_B_DATA_N<2>	B2	PL2B	
GMUX_PL10A	C2	PL6A	
TP_GMUX_PL10B	D3	PL6B	
LVDS_IG_A_DATA_P<0>	D1	PL7A	BANK7
LVDS_IG_A_DATA_N<0>	E1	PL7B	
LVDS_IG_A_DATA_P<1>	D2	PL8A	
LVDS_IG_A_DATA_N<1>	E3	PL8B	
LVDS_IG_A_DATA_P<2>	F1	PL9A	
LVDS_IG_A_DATA_N<2>	G1	PL9B	
LVDS_IG_B_DATA_P<0>	F3	PL10A	
LVDS_IG_B_DATA_N<0>	G2	PL10B	
LVDS_IG_B_DATA_P<1>	H2	PL11A	
LVDS_IG_B_DATA_N<1>	G3	PL11B	
LVDS_IG_A_CLK_P	H1	PL12A	
LVDS_IG_A_CLK_N	H3	PL12B	
TP_LVDS_MUX_SEL_EG	L1	PL14A	
GMUX_VSYNC	L3	PL14B	
GMUX_RESET_L	K3	PL15A	
GMUX_VSYNC	L2	PL15B	
PM_ALL_GPU_PGOOD	N1	PL25A	
PEX_CLKREQ_L	P1	PL25B	

GND: J1 B8 C6 C12 C13 H13 M14 N10 N6 F3 M2 C1 E2 B4 M11
GNDIO00 GNDIO01 GNDIO02 GNDIO03 GNDIO04 GNDIO05 GNDIO06 GNDIO07 ULC_GNDPLL LRC_GNDPLL

LVDS_B_DATA_P<0>	A2	PT7A	BANK0
LVDS_B_DATA_N<0>	A3	PT7B	
LVDS_B_DATA_P<1>	A1	PT8A	
LVDS_B_DATA_N<1>	B3	PT8B	
LVDS_B_DATA_P<2>	C5	PT9A	
LVDS_B_DATA_N<2>	A5	PT9B	
EG_PWRSEQ_EN	B6	PT14A	
GMUX_DEBUG_RESET_L	C7	PT14B	
LVDS_A_CLK_P	A6	PT15A	
LVDS_A_CLK_N	A7	PT15B	
LVDS_B_CLK_P	C8	PT16A	
LVDS_B_CLK_N	C9	PT16B	
LVDS_A_DATA_P<0>	A8	PT17A	
LVDS_A_DATA_N<0>	B9	PT17B	
LVDS_A_DATA_P<1>	A9	PT18A	
LVDS_A_DATA_N<1>	C10	PT18B	
LVDS_A_DATA_P<2>	B10	PT19A	
LVDS_A_DATA_N<2>	A10	PT19B	
GND	A11	PT20A	BANK1
GND	B12	PT20B	
GND	B13	PT28A	
GND	A13	PT28B	
DP_CA_DET	A14	PR2A	BANK2
DP_HOTPLUG_DET	B14	PR2B	
LVDS_EG_A_DATA_P<0>	D12	PR6A	
LVDS_EG_A_DATA_N<0>	D13	PR6B	
LVDS_EG_A_DATA_P<1>	D14	PR7A	
LVDS_EG_A_DATA_N<1>	E14	PR7B	
LVDS_EG_A_DATA_P<2>	E12	PR8A	
LVDS_EG_A_DATA_N<2>	F12	PR8B	
LVDS_EG_B_DATA_P<0>	F14	PR9A	
LVDS_EG_B_DATA_N<0>	G14	PR9B	
LVDS_EG_B_DATA_P<1>	G12	PR10A	
LVDS_EG_B_DATA_N<1>	G13	PR10B	
LVDS_EG_B_DATA_P<2>	H13	PR11A	
LVDS_EG_B_DATA_N<2>	H12	PR11B	
LVDS_EG_A_CLK_P	H14	PR12A	
LVDS_EG_A_CLK_N	J12	PR12B	
LVDS_IG_PANEL_PWR	L14	PR14A	BANK3
EG_LCD_PWR_EN	M13	PR14B	
LVDS_IG_BKL_ON	N14	PR24A	
EG_BKLT_EN	N13	PR24B	

PP3V3_S3

R9676 100K 5% 1/16W MF-LF 402 — GMUX_S3_PD_EN

Q9607 SSM6N15FEAPE SOT563 — ALL_SYS_PWRGD

R9678 4.7K 5% 1/16W MF-LF 402 — R9671 4.7K 5% 1/16W MF-LF 402 — R9672 4.7K 5% 1/16W MF-LF 402 — R9673 4.7K 5% 1/16W MF-LF 402 — R9674 4.7K 5% 1/16W MF-LF 402 — GMUX_S3_PD_GND

NO STUFF R9675 0 5% 1/16W MF-LF 402

EG_RAIL1_EN, EG_RAIL2_EN, EG_RAIL3_EN, EG_RAIL4_EN, LCD_PWR_EN

GMUXPLL_1V8 R9611 0 5% 1/16W MF-LF 402 — PP1V8_S0 — PP3V3R1V8_S0_GMUX (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

GMUXPLL_3V3 R9612 0 5% 1/16W MF-LF 402 — PP3V3_S0

PP3V3R1V8_S0_GMUX_ULC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V) — L9621 FERR-220-OHM 0402 — C9631 0.1UF 20% 10V CERM 402

PP3V3R1V8_S0_GMUX_LRC_VCCPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.09 mm, VOLTAGE=3.3V) — L9620 FERR-220-OHM 0402 — C9630 0.1UF 20% 10V CERM 402

LVDS Receiver Termination

LVDS_IG_A_CLK_P	R9650	100	PLACE_NEAR=U9600.H3:5mm	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>	R9651	100	PLACE_NEAR=U9600.F1:5mm	LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>	R9652	100	PLACE_NEAR=U9600.E3:5mm	LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>	R9653	100	PLACE_NEAR=U9600.G1:5mm	LVDS_IG_A_DATA_N<2>
LVDS_IG_B_DATA_P<0>	R9654	100	PLACE_NEAR=U9600.G2:5mm	LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>	R9655	100	PLACE_NEAR=U9600.G3:5mm	LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>	R9656	100	PLACE_NEAR=U9600.H2:5mm	LVDS_IG_B_DATA_N<2>
LVDS_EG_A_CLK_P	R9660	100	PLACE_NEAR=U9600.J12:5mm	LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>	R9661	100	PLACE_NEAR=U9600.D13:5mm	LVDS_EG_A_DATA_N<0>
LVDS_EG_A_DATA_P<1>	R9662	100	PLACE_NEAR=U9600.E14:5mm	LVDS_EG_A_DATA_N<1>
LVDS_EG_A_DATA_P<2>	R9663	100	PLACE_NEAR=U9600.F12:5mm	LVDS_EG_A_DATA_N<2>
LVDS_EG_B_DATA_P<0>	R9664	100	PLACE_NEAR=U9600.G14:5mm	LVDS_EG_B_DATA_N<0>
LVDS_EG_B_DATA_P<1>	R9665	100	PLACE_NEAR=U9600.G13:5mm	LVDS_EG_B_DATA_N<1>
LVDS_EG_B_DATA_P<2>	R9666	100	PLACE_NEAR=U9600.H12:5mm	LVDS_EG_B_DATA_N<2>

All: 1% 1/16W MF-LF 402

SIGNAL_MODEL=EMPTY

Required Pullups

PP3V3_S0

GMUX_DEBUG_RESET_L — R9680 1K 5% 1/16W MF-LF 402

EG_PWRSEQ_EN — R9684 1K 5% 1/16W MF-LF 402

NO STUFF R9679 10K 1% 1/16W MF-LF 402 — SILK_PART=GMUX_RST

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_IG	R9682	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_EG	R9683	10K	5% 1/16W MF-LF 402
EG_RESET_L	R9691	100K	5% 1/16W MF-LF 402
LCD_BKLT_PWM	R9693	100K	5% 1/16W MF-LF 402

NO STUFF

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

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*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

PP5V_S0
R9701 0 5% 1/16W MF-LF 402 MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V
R9702 0 5% 1/16W MF-LF 402
XW9700 SM
PPBUS_S0_LCDBKLT_PWR
CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
L9701 22UH-2.5A IHLP2525CZ-SM
PPVIN_BKL MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=8.4V
NO STUFF R9703 0 5% 1/16W MF-LF 402
PPBUS_S0_LCDBKLT_PWR_SW MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=50V SWITCH_NODE=TRUE
D9701 SOD-123 RB160M-60G
C9796 220PF 10% 50V X7R-CERM 402
C9797 10UF 10% 50V X5R 1210-1
C9799 10UF 10% 50V X5R 1210-1
PPVOUT_S0_LCDBKLT MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=50V

PP3V3_S0
BKL_VLDO
C9714 0.01UF 10% 16V CERM 402
C9710 1UF 10% 25V X5R 603-1
C9711 0.1UF 10% 16V X5R 402
PPVIN_BKL_R MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM
NO STUFF C9741 1UF 10% 6.3V X5R 402
NO STUFF C9740 10UF 20% 6.3V X5R 603
R9740 47.0K 1% 1/16W MF-LF 402
BKL_FLTR_RC
R9741 10K 5% 1/16W MF-LF 402
VOLTAGE=5V

U9701 LLP LP8545SQX
CRITICAL
VDDIO VLDO VIN
NCX GD SW
BKL_FSET FSET FB
BKL_FLTR FILTER OUT1 BKL_ISEN1
BKL_ISET ISET OUT2 BKL_ISEN2
BKL_SCL SCLK OUT3 BKL_ISEN3
BKL_SDA SDA OUT4 BKL_ISEN4
LVDS_BKL_PWM_RC PWM OUT5 BKL_ISEN5
TP_BKL_FAULT FAULT OUT6 BKL_ISEN6
BKLT_EN EN VSYNC BKL_VSYNC_R
GND_SW GND_S GND_L THRM PAD

SMBUS_PCH_CLK R9753 0 5% 1/16W MF-LF 402
SMBUS_PCH_DATA R9757 0 5% 1/16W MF-LF 402
R9731 301K 1% 1/16W MF-LF 402
NO STUFF C9723 0.1UF 10% 25V X5R 402
R9715 100K 1% 1/16W MF-LF 402
(EEPROM should set EN_I_RES=1)
R9714 16.2K 1% 1/16W MF-LF 402
I_LED=23.2Ma
I_LED=369/Riset
R9716 90.9K 1% 1/16W MF-LF 402
Fpwm=9.62Khz
details in spec
R9755 10K 5% 1/16W MF-LF 402
NO STUFF R9754 0 5% 1/16W MF-LF 402
R9704 0 5% 1/16W MF-LF 402
LCD_BKLT_PWM
NO STUFF C9704 33PF 5% 50V CERM 402
R9704 SHOULD BE 47K IF RC FILTER IS USED
XW9710 SM
BKL_SGND
GMUX_VSYNC

R9717 10.2 0.1% 1/16W TF 402 LED_RETURN_1
R9718 10.2 0.1% 1/16W TF 402 LED_RETURN_2
R9719 10.2 0.1% 1/16W TF 402 LED_RETURN_3
R9720 10.2 0.1% 1/16W TF 402 LED_RETURN_4
R9721 10.2 0.1% 1/16W TF 402 LED_RETURN_5
R9722 10.2 0.1% 1/16W TF 402 LED_RETURN_6
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

SYNC_MASTER=K18_BKLT SYNC_DATE=07/29/2009
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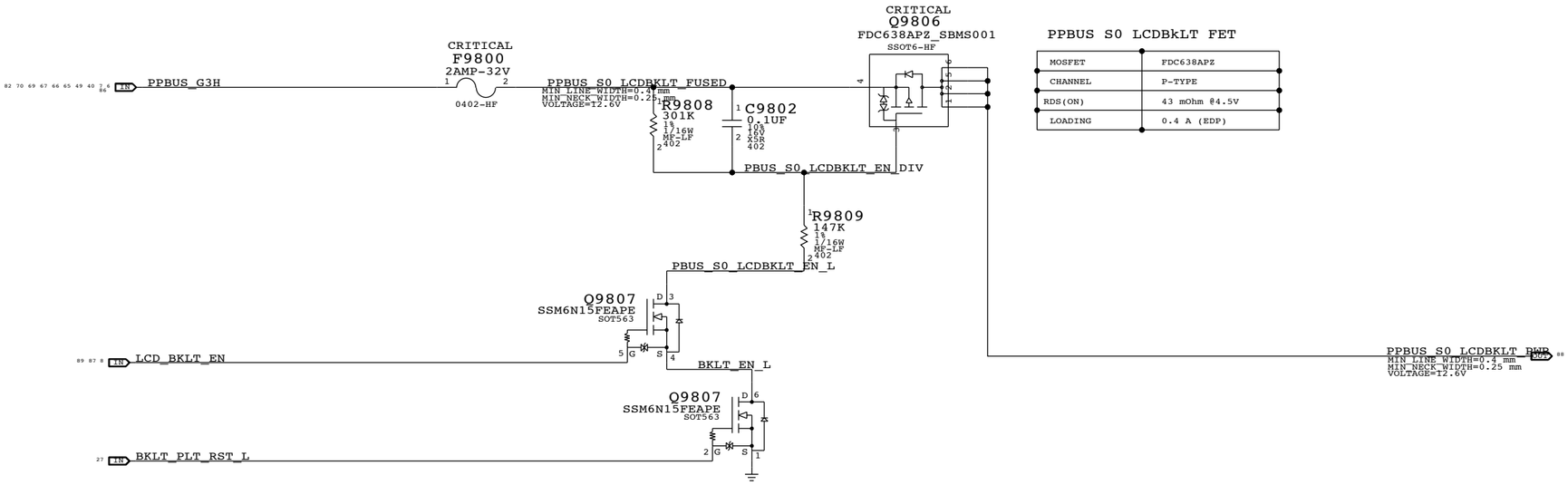

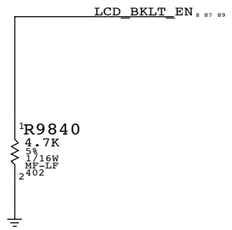

SYNC_MASTER=K19_MLB SYNC_DATE=05/29/2009

PAGE TITLE
LCD Backlight Support

Apple Inc.

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Blank Page, was 1.2V/1.8V in K19

SYNC MASTER=K18 POWER SYNC DATE=06/10/2009

PAGE TITLE

Misc Power Supplies

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.1 and Table 4-184.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI_INT	9 18
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB_CPURST_L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTTS0_PGOOD	10 70
XDP_XPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPUPWRGD	10 25
XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_PRDY_L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_PREQ_L	10 25
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	10 46
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	10 46
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 20 46
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU_PSI_L	12 15 68
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	12 15 68
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 25
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	25
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8 12 15
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	12 50 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VTTSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_P	13 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX_VSENSE_N	13 69
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8 13
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	13 69
	CPU_50S	CPU_AGTL	GFX_VR_EN	13 69
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	13 69
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8 9 74
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	74

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PAGE TITLE: CPU Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:

DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 28
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0>	11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4>	11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7>	11 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 29 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0>	11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4>	11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 29 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 29 30
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 29

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0> 8 84
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0> 8 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P 8 18 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N 8 18 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P 18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0> 18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0> 18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3> 8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3> 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKP 6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP_LVDS_IG_B_CLKN 6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0> 18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0> 18 87
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAP<3> 8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_B_DATAN<3> 8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 17 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N 17 42
	SATA_90D	SATA	SATA_HDD_R2D_P 6 42
	SATA_90D	SATA	SATA_HDD_R2D_N 6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 17 42
	SATA_90D	SATA	SATA_HDD_D2R_N 17 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P 6 42
	SATA_90D	SATA	SATA_HDD_D2R_C_N 6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P 17 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N 17 42
	SATA_90D	SATA	SATA_ODD_R2D_P 6 42
	SATA_90D	SATA	SATA_ODD_R2D_N 6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P 17 42
	SATA_90D	SATA	SATA_ODD_D2R_N 17 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P 6 42
	SATA_90D	SATA	SATA_ODD_D2R_C_N 6 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P 42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N 42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P 42
	SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N 42
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP 17
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P 19 35
	USB_85D	USB	USB_HUB1_UP_N 19 35
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P 19 36
	USB_85D	USB	USB_HUB2_UP_N 19 36
USB_EXTA	USB_85D	USB	USB_EXTA_P 36 43
	USB_85D	USB	USB_EXTA_N 36 43
USB_EXTB	USB_85D	USB	USB_EXTB_P 35 43
	USB_85D	USB	USB_EXTB_N 35 43
USB_EXTC	USB_85D	USB	USB_EXTC_P 8 35
	USB_85D	USB	USB_EXTC_N 8 35
USB_EXTD	USB_85D	USB	USB_EXTD_P
	USB_85D	USB	USB_EXTD_N
USB_MINI	USB_85D	USB	USB_MINI_P
	USB_85D	USB	USB_MINI_N
USB_WM	USB_85D	USB	USB_WM_P
	USB_85D	USB	USB_WM_N
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 6 33
	USB_85D	USB	USB_CAMERA_CONN_N 6 33
USB_BT	USB_85D	USB	USB_BT_P 33 36
	USB_85D	USB	USB_BT_N 33 36
USB_TPAD	USB_85D	USB	USB_TPAD_P 36 53
	USB_85D	USB	USB_TPAD_N 36 53
USB_IR	USB_85D	USB	USB_IR_P 35 44
	USB_85D	USB	USB_IR_N 35 44
USB_SDCARD	USB_85D	USB	USB_SDCARD_P 8 34 36
	USB_85D	USB	USB_SDCARD_N 8 34 36
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P 19 101
	USB_85D	USB	USB_BRCRYPT_N 19 101
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS 19
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P 17 26
PCH_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N 17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P 17 26
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N 17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P 17 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N 17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P 17 26
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N 17 26
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK 17 26
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN 17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P 10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N 10 17

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 45 47 87
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 45 47 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 47 87
MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	17 25 26 28 30 32 42 47 48 63 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 58
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 58
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 58
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 58
	HDA_50S	HDA	AUD_SDI_R	58
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 58
	HDA_50S	HDA	HDA_SDOUT_R	17
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 46
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 33
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	
MCP_PE0_REFCLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 74
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 74
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
MCP_PE3_REFCLK	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 17
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 17
1233	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6 20
1233	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6 20
1233	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6 20
1233	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	20
1233	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
1240	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 20 94
1241	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6 20
1242	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6 20
1243	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6 20
1244	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6 20
1245	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6 20
1246	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6 20
1247	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	20
1248	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6 20
1249	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6 20
1250	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6 20

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	27 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	27 37
	ENET_50S	ENET_3X	ENET_RESET_L	27 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 40 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 40 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 40 41
Port 2 Not Used				

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL 6 33 45 48 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA 6 33 45 48 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL 45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA 45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 45 48 51 81
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 45 48 51 81
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL 6 45 48 64 65
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA 6 45 48 64 65
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL 45 48 56
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA 45 48 56

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P 65
	1TO1_DIFFPAIR		CHGR_CSI_N 65
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P 65
	1TO1_DIFFPAIR		CHGR_CSO_N 65

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J147 LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P 84 87
J147 LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N 84 87
J150 LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0> 84 87
J150 LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0> 84 87
J157 LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P 84 87
J157 LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N 84 87
J200 LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0> 84 87
J200 LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0> 84 87
J132	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P 6 83
J133	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N 6 83
J134	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P 6 83
J135	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N 6 83
J136	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P 83 84
J137	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N 83 84
J138	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0> 6 83 84
J139	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0> 6 83 84
J194	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P 83 84
J195	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N 83 84
J196	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0> 6 83 84
J197	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0> 6 83 84
J142 DP_ML	DP_85D	DISPLAYPORT	DP_ML_C_P<3..0> 85
J140	DP_85D	DISPLAYPORT	DP_ML_C_N<3..0> 85
J153 DP_ML	DP_85D	DISPLAYPORT	DP_ML_P<3..0> 84 85
J152	DP_85D	DISPLAYPORT	DP_ML_N<3..0> 84 85
J205 DP_ML	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0> 85
J206	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0> 85
J151 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_P 84 85
J150 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_AUX_CH_C_N 84 85

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0> 76 77
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0> 76 77
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1> 76 77
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1> 76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0> 76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6> 76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0> 76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L 76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCAS_L 76 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L 76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE 76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE 76 77
J205 FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L 76 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST 76 77
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2> 76 77
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2> 76 77
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0> 76 77
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1> 76 77
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2> 76 77
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3> 76 77
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0> 76 77
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1> 76 77
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2> 76 77
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3> 76 77
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0> 76 77
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8> 76 77
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16> 76 77
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24> 76 77
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0> 76 77
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1> 76 77
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2> 76 77
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3> 76 77
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4> 76 77
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5> 76 77
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6> 76 77
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7> 76 77
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4> 76 77
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5> 76 77
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6> 76 77
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7> 76 77
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32> 76 77
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40> 76 77
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48> 76 77
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56> 76 77
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4> 76 77
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5> 76 77
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6> 76 77
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7> 76 77

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_MATRIX)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 27 79 80
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS 79 80
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P 81 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N 81 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0> 81 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0> 81 87
J209 LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3> 80 81
J210 LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3> 80 81
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0> 81 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0> 81 87
J208 LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3> 80 81
J207 LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3> 80 81
J142 DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_P<3..0> 81 84
J144 DP_ML	DP_85D	DISPLAYPORT	DP_EG_ML_N<3..0> 81 84
J145 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_P 81 84
J143 DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_N 81 84
J155	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_P 84
J156	DP_85D	DISPLAYPORT	DP_EG_AUX_CH_C_N 84

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0> 76 78
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0> 76 78
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1> 76 78
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1> 76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0> 76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6> 76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0> 76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L 76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCAS_L 76 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L 76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE 76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE 76 78
J204 FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L 76 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST 76 78
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2> 76 78
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2> 76 78
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0> 76 78
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1> 76 78
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2> 76 78
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3> 76 78
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0> 76 78
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1> 76 78
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2> 76 78
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3> 76 78
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0> 76 78
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8> 76 78
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16> 76 78
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24> 76 78
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0> 76 78
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1> 76 78
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2> 76 78
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3> 76 78
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4> 76 78
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5> 76 78
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6> 76 78
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7> 76 78
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4> 76 78
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5> 76 78
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6> 76 78
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7> 76 78
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32> 76 78
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40> 76 78
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48> 76 78
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56> 76 78
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4> 76 78
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5> 76 78
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6> 76 78
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7> 76 78
J210 FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCAS_L 76 77
J213 FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCAS_L 76 78

SYNC_MASTER=K17_REF SYNC_DATE=06/15/2009

PAGE TITLE
GPU (GT216) CONSTRAINTS

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

K18 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
		ENET_100D	ENETCONN	ENETCONN_P<3..0>	38
		ENET_100D	ENETCONN	ENETCONN_N<3..0>	38
		SATA_90D	SATA	SATA_ODD_R2D_UF_P	42
		SATA_90D	SATA	SATA_ODD_R2D_UF_N	42
		SATA_90D	SATA	SATA_ODD_D2R_UF_P	42
		SATA_90D	SATA	SATA_ODD_D2R_UF_N	42
		SATA_90D	SATA	SATA_HDD_D2R_UF_P	42
		SATA_90D	SATA	SATA_HDD_D2R_UF_N	42
		SATA_90D	SATA	SATA_HDD_R2D_UF_P	42
		SATA_90D	SATA	SATA_HDD_R2D_UF_N	42
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
		THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
I287	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
I288		THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
		THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 79 80
		THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 79 80
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_N	50
		SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_P	50
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	50 70
		SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	50 70
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	50
		SENSE_1TO1_55S	SENSE	DDRISNS_R_P	50
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_N	69
		SENSE_1TO1_55S	SENSE	GFXIMVP_CS_P	69
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_N	50 69
		SENSE_1TO1_55S	SENSE	GFXIMVP_CS_R_P	50 69
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFX_ISNS_R_N	50
		SENSE_1TO1_55S	SENSE	GFX_ISNS_R_P	50
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	50
		SENSE_1TO1_55S	SENSE	GPUISENS_P	50
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	50 67
		SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	50 67
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	99
		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	99
I249	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	99
I250		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	99
I252	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	56
I251		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	56
I253	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	49
I254		SENSE_1TO1_55S	SENSE	ISNS_CPU_P	49
I256	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
I255		SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
I281	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	56
I282		SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	56
I283	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
I284		SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
I285	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
I286		SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	56
		SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	56
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N	50
		SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P	50
I292	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	50
I291		SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	50

K18 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 33
	1TO1_DIFFPAIR		CHGR_CSI_R_P	65
	1TO1_DIFFPAIR		CHGR_CSI_R_N	65
	1TO1_DIFFPAIR		CHGR_CSO_R_P	49 65
	1TO1_DIFFPAIR		CHGR_CSO_R_N	49 65
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 43
	USB_85D	USB	CONN_USB2_BT_P	6 33
	USB_85D	USB	CONN_USB2_BT_N	6 33
	USB_85D	USB	USB_LT2_P	6 43
	USB_85D	USB	USB_LT2_N	6 43
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	84
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	84
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 61 62
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 61 62
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 61 62
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	6 7 17 18 19 20 21 23 27 31 35 57 66 71 72 73 83 85
		SB_POWER	PP3V3_S0	6 7 17 18 19 20 21 23 24 25 26 27 28 30 34 37 40 42 46 47 48 50 51 52 54 58 62 63 68 87 69 72 73 84 80 88 83 85
		SB_POWER	PP1V5_S3RS0	6 7 13 16 31 42 72 73
		GND	GND	

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

SYNC MASTER=K17 REF SYNC DATE=06/15/2009

PAGE TITLE
Project Specific Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

K18 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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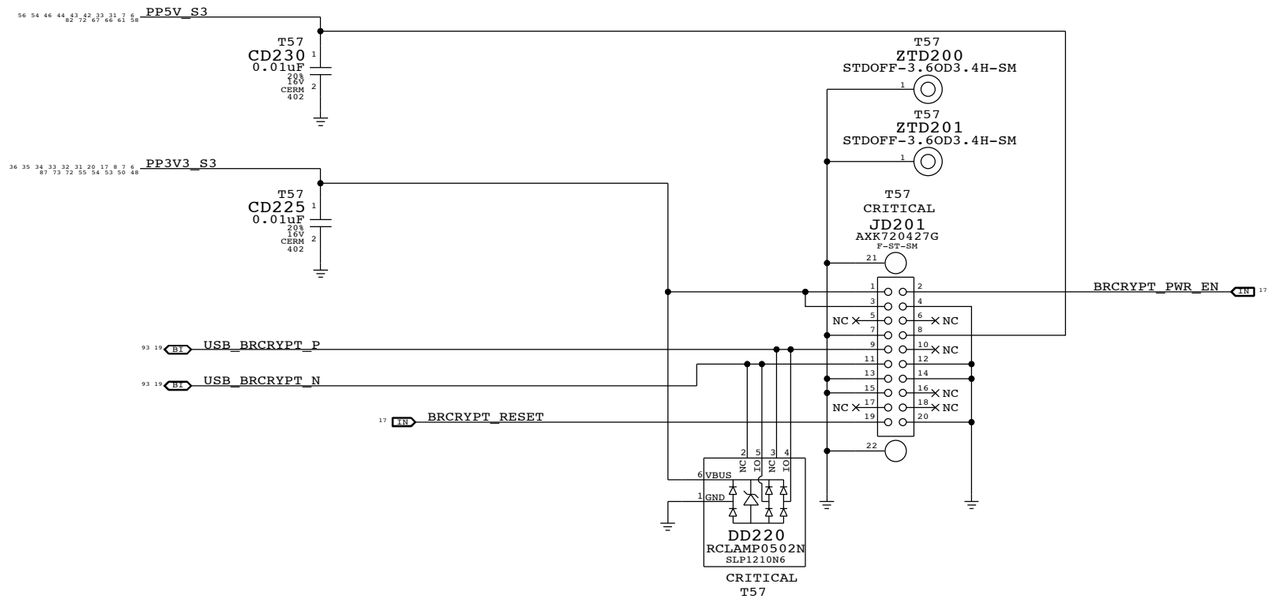

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