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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2010-07-22

SCHEM, MLB DVT, K99

07/22/10

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8379	1	SCHEM, MLB, K99	SCH	CRITICAL	
820-2796	1	PCBF, MLB, K99	PCB	CRITICAL	

DRAWING TITLE		SCHEM, MLB, K99	
DRAWING NUMBER		051-8379	SIZE D
REVISION		4.4.0	
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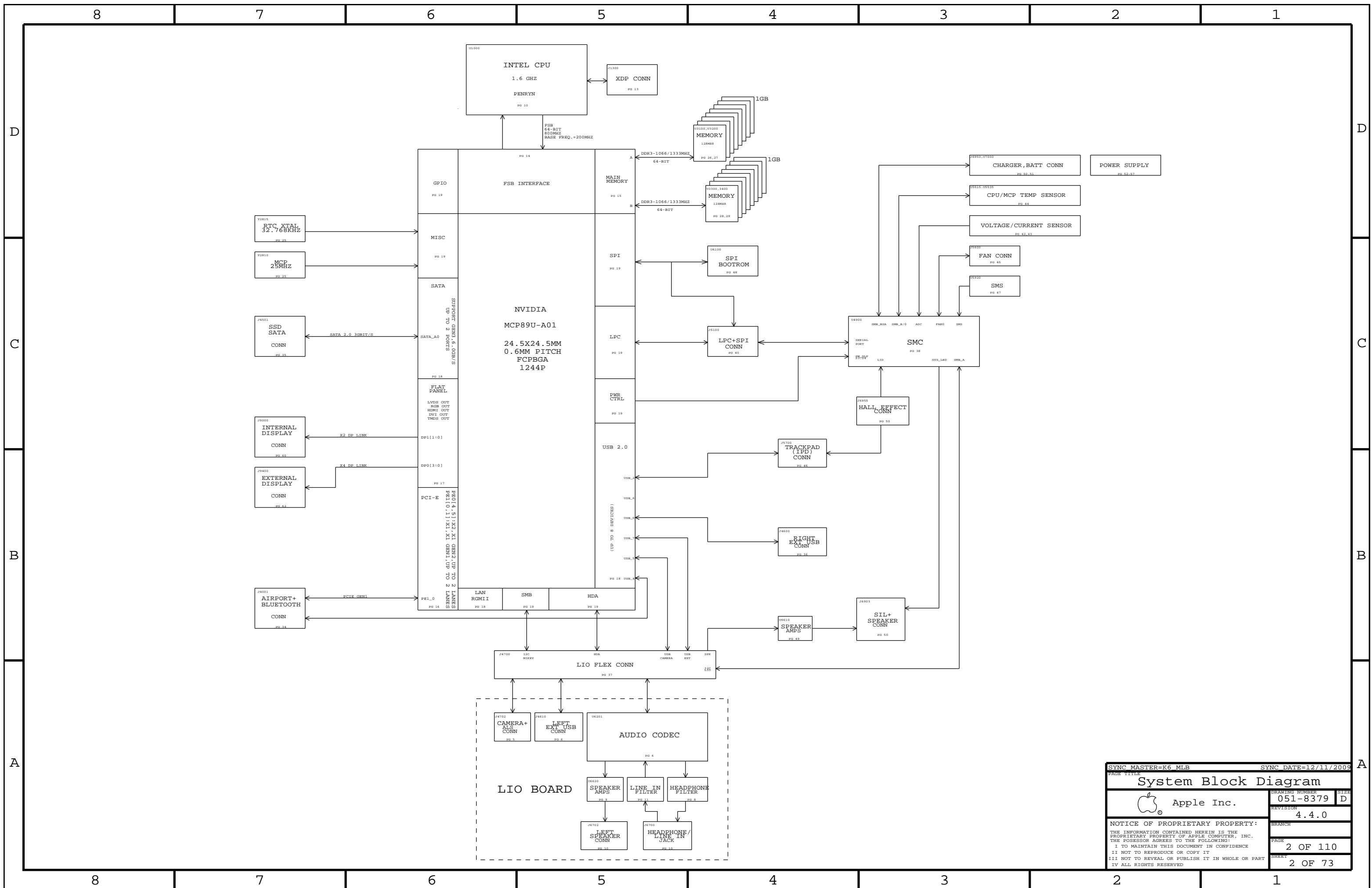
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SYNC MASTER=K6 MLB		SYNC DATE=12/11/2009	
System Block Diagram			
Apple Inc.		DRAWING NUMBER	SIZE
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BOM Variants		BOM OPTIONS	
BOM NUMBER	BOM NAME		
639-0651	PCBA,MLB,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DX7,DDR3:HYNIX_2GB,CAPS:SS	
639-1055	PCBA,MLB,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD15,DDR3:HYNIX_2GB,CAPS:MU	
639-1048	PCBA,MLB,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0X,DDR3:HYNIX_2GB,CAPS:TY	
639-1043	PCBA,MLB,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Q,DDR3:HYNIX_4GB,CAPS:SS	
639-1044	PCBA,MLB,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0R,DDR3:HYNIX_4GB,CAPS:MU	
639-1039	PCBA,MLB,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0L,DDR3:HYNIX_4GB,CAPS:TY	
639-1045	PCBA,MLB,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0T,DDR3:SAMSUNG_2GB,CAPS:SS	
639-1054	PCBA,MLB,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD14,DDR3:SAMSUNG_2GB,CAPS:MU	
639-1049	PCBA,MLB,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Y,DDR3:SAMSUNG_2GB,CAPS:TY	
639-1052	PCBA,MLB,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD12,DDR3:SAMSUNG_4GB,CAPS:SS	
639-1046	PCBA,MLB,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0V,DDR3:SAMSUNG_4GB,CAPS:MU	
639-1040	PCBA,MLB,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0W,DDR3:SAMSUNG_4GB,CAPS:TY	
639-1042	PCBA,MLB,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0P,DDR3:MICRON_2GB,CAPS:SS	
639-1053	PCBA,MLB,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD13,DDR3:MICRON_2GB,CAPS:MU	
639-1047	PCBA,MLB,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0U,DDR3:MICRON_2GB,CAPS:TY	
639-1051	PCBA,MLB,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD11,DDR3:MICRON_4GB,CAPS:SS	
639-1041	PCBA,MLB,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0N,DDR3:MICRON_4GB,CAPS:MU	
639-1050	PCBA,MLB,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD10,DDR3:MICRON_4GB,CAPS:TY	
639-1446	PCBA,MLB,1.6GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4Q,DDR3:ELPIDA_2GB,CAPS:SS	
639-1438	PCBA,MLB,1.6GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4G,DDR3:ELPIDA_2GB,CAPS:MU	
639-1444	PCBA,MLB,1.6GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4N,DDR3:ELPIDA_2GB,CAPS:TY	
639-1449	PCBA,MLB,1.6GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4V,DDR3:ELPIDA_4GB,CAPS:SS	
639-1448	PCBA,MLB,1.6GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4T,DDR3:ELPIDA_4GB,CAPS:MU	
639-1445	PCBA,MLB,1.6GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4P,DDR3:ELPIDA_4GB,CAPS:TY	
607-6999	CMN PTS,PCBA,MLB,K99	K99_CMNPTS	
085-1121	K99 MLB DEVELOPMENT BOM	K99_DEVEL:ENG	
639-1355	PCBA,MLB,1.4GHZ,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8L,DDR3:HYNIX_2GB,CAPS:SS	
639-1341	PCBA,MLB,1.4GHZ,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8J,DDR3:HYNIX_2GB,CAPS:MU	
639-1353	PCBA,MLB,1.4GHZ,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8K,DDR3:HYNIX_2GB,CAPS:TY	
639-1350	PCBA,MLB,1.4GHZ,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8P,DDR3:HYNIX_4GB,CAPS:SS	
639-1356	PCBA,MLB,1.4GHZ,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8M,DDR3:HYNIX_4GB,CAPS:MU	
639-1348	PCBA,MLB,1.4GHZ,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8N,DDR3:HYNIX_4GB,CAPS:TY	
639-1349	PCBA,MLB,1.4GHZ,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8D,DDR3:SAMSUNG_2GB,CAPS:SS	
639-1351	PCBA,MLB,1.4GHZ,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8G,DDR3:SAMSUNG_2GB,CAPS:MU	
639-1357	PCBA,MLB,1.4GHZ,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8N,DDR3:SAMSUNG_2GB,CAPS:TY	
639-1344	PCBA,MLB,1.4GHZ,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF86,DDR3:SAMSUNG_4GB,CAPS:SS	
639-1352	PCBA,MLB,1.4GHZ,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8H,DDR3:SAMSUNG_4GB,CAPS:MU	
639-1354	PCBA,MLB,1.4GHZ,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8K,DDR3:SAMSUNG_4GB,CAPS:TY	
639-1342	PCBA,MLB,1.4GHZ,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF84,DDR3:MICRON_2GB,CAPS:SS	
639-1346	PCBA,MLB,1.4GHZ,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF88,DDR3:MICRON_2GB,CAPS:MU	
639-1343	PCBA,MLB,1.4GHZ,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF85,DDR3:MICRON_2GB,CAPS:TY	
639-1347	PCBA,MLB,1.4GHZ,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF89,DDR3:MICRON_4GB,CAPS:SS	
639-1345	PCBA,MLB,1.4GHZ,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF87,DDR3:MICRON_4GB,CAPS:MU	
639-1340	PCBA,MLB,1.4GHZ,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF82,DDR3:MICRON_4GB,CAPS:TY	
639-1442	PCBA,MLB,1.4GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4L,DDR3:ELPIDA_2GB,CAPS:SS	
639-1443	PCBA,MLB,1.4GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4M,DDR3:ELPIDA_2GB,CAPS:MU	
639-1447	PCBA,MLB,1.4GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4R,DDR3:ELPIDA_2GB,CAPS:TY	
639-1441	PCBA,MLB,1.4GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4K,DDR3:ELPIDA_4GB,CAPS:SS	
639-1439	PCBA,MLB,1.4GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4H,DDR3:ELPIDA_4GB,CAPS:MU	
639-1440	PCBA,MLB,1.4GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4J,DDR3:ELPIDA_4GB,CAPS:TY	

Bar Code Labels / EEE #'s						
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DX7]	CRITICAL	EEE:DX7	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0L]	CRITICAL	EEE:DD0L	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0M]	CRITICAL	EEE:DD0M	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0N]	CRITICAL	EEE:DD0N	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0P]	CRITICAL	EEE:DD0P	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Q]	CRITICAL	EEE:DD0Q	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0R]	CRITICAL	EEE:DD0R	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0T]	CRITICAL	EEE:DD0T	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0V]	CRITICAL	EEE:DD0V	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0W]	CRITICAL	EEE:DD0W	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0X]	CRITICAL	EEE:DD0X	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Y]	CRITICAL	EEE:DD0Y	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD10]	CRITICAL	EEE:DD10	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD11]	CRITICAL	EEE:DD11	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD12]	CRITICAL	EEE:DD12	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD13]	CRITICAL	EEE:DD13	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD14]	CRITICAL	EEE:DD14	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD15]	CRITICAL	EEE:DD15	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF82]	CRITICAL	EEE:DF82	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF83]	CRITICAL	EEE:DF83	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF84]	CRITICAL	EEE:DF84	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF85]	CRITICAL	EEE:DF85	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF86]	CRITICAL	EEE:DF86	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF87]	CRITICAL	EEE:DF87	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF88]	CRITICAL	EEE:DF88	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF89]	CRITICAL	EEE:DF89	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8C]	CRITICAL	EEE:DF8C	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8D]	CRITICAL	EEE:DF8D	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8F]	CRITICAL	EEE:DF8F	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8G]	CRITICAL	EEE:DF8G	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8H]	CRITICAL	EEE:DF8H	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8J]	CRITICAL	EEE:DF8J	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8K]	CRITICAL	EEE:DF8K	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8L]	CRITICAL	EEE:DF8L	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8M]	CRITICAL	EEE:DF8M	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8N]	CRITICAL	EEE:DF8N	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4G]	CRITICAL	EEE:DG4G	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4H]	CRITICAL	EEE:DG4H	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4J]	CRITICAL	EEE:DG4J	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4K]	CRITICAL	EEE:DG4K	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4M]	CRITICAL	EEE:DG4M	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4N]	CRITICAL	EEE:DG4N	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4P]	CRITICAL	EEE:DG4P	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4Q]	CRITICAL	EEE:DG4Q	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4R]	CRITICAL	EEE:DG4R	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4L]	CRITICAL	EEE:DG4L	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4T]	CRITICAL	EEE:DG4T	
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4V]	CRITICAL	EEE:DG4V	

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1121	1	K99 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-6999	1	CMN PTS,PCBA,MLB,K99	CMNPTS	CRITICAL	K99_CMNPTS

SYNC MASTER=K6.MLB SYNC DATE=12/11/2009

K99 BOM Variants

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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Programmable Parts

33850563	1	IC,SMC,H89/2117,8X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0261	1	IC ASSY,SMC EXTERNAL,K99	U4900	CRITICAL	SMC:PROG
33550610	1	IC,FLASH,SPI,128MBIT,5.7V,866MS,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0262	1	IC ASSY,EFI UNLOCKED,K99	U6100	CRITICAL	BOOTROM:UNLOCKED
341T0263	1	IC ASSY,EFI,LOCKED,K99	U6100	CRITICAL	BOOTROM:LOCKED

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
13850681	13850638		ALL	TATVO VIDEN AS ALTERNATE
15250874	15250516		ALL	MANLAVEN AS ALTERNATE
15250847	15250586		ALL	MANLAVEN AS ALTERNATE
35352987	35352988	HYDELO:FIXED	ALL	YOUTIUSON AS ALTERNATE FOR U250
10450023	10450018		ALL	CONTRIC AS ALTERNATE
10750139	10750075		ALL	CONTRIC AS ALTERNATE
13850671	13850673		ALL	TATVO AS ALTERNATE
15550578	15550367		ALL	TATVO AS ALTERNATE
37650926	37650610		ALL	FAISGULL AS ALTERNATE
15550457	15550329		ALL	MANLAVEN AS ALTERNATE
37750107	37750066		ALL	SHIBBI AS ALTERNATE

BOM Groups

BOM GROUP	BOM OPTIONS
K99_COMMON	COMMON,ALTERNATE,PROJ:K99,K99_MISC,MCP89U:A03,K99_DEBUG:ENG,K99_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K99_MISC	DP_ESD,DP_PWR:SMC,VPRQ:SLP93,HYDELO:FIXED,MCPHYD:P2V5,MCPPLL_R:REG,SOPGOOD_AFF,ISL6259_SCREENED:YES,DP12C:SMC
K99_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K99_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPPLUS,VREFMRGN:YES,EFI_DEBUG,SOPGOOD_IS1,MCPPLL_LDO,S3_S0_LED
K99_DEVEL:PVT	LPPLUS
K99_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K99_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K99_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33753792	1	CDC,CPM6,QR,1,2,10M,800,80,1M,80A	U1000	CRITICAL	CPU:1.2GHZ
33753947	1	REG,REGFB,FQ,1,6,10V,80,3M,80A	U1000	CRITICAL	CPU:1.6GHZ
33753954	1	REG,REGFB,FQ,1,4,10V,80,3M,80A	U1000	CRITICAL	CPU:1.4GHZ
33753820	1	IC,MCP89U-A01,24,500K24,50M,1244FC05A	U1400	CRITICAL	MCP89U:A01
33753868	1	IC,MCP89U-A02,24,500K24,50M,1244FC05A	U1400	CRITICAL	MCP89U:A02
33753939	1	IC,MCP89U-A03,24,500K24,50M,1244FC05A	U1400	CRITICAL	MCP89U:A03
33350552	4	HYNIX,LVDDR3,1GBIT,7,5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
33350552	4	HYNIX,LVDDR3,1GBIT,7,5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
33350552	4	HYNIX,LVDDR3,1GBIT,7,5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_2GB
33350552	4	HYNIX,LVDDR3,1GBIT,7,5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_2GB
33350553	4	SAMSUNG,LVDDR3,1GBIT,7,5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
33350553	4	SAMSUNG,LVDDR3,1GBIT,7,5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
33350553	4	SAMSUNG,LVDDR3,1GBIT,7,5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
33350553	4	SAMSUNG,LVDDR3,1GBIT,7,5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
33350554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
33350554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
33350554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_2GB
33350554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_2GB
33350565	4	ELPIDA,LVDDR3,1GBIT,7,5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_2GB
33350565	4	ELPIDA,LVDDR3,1GBIT,7,5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_2GB
33350565	4	ELPIDA,LVDDR3,1GBIT,7,5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_2GB
33350565	4	ELPIDA,LVDDR3,1GBIT,7,5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_2GB
33350555	4	HYNIX,LVDDR3,2GBIT,8X11.1	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
33350555	4	HYNIX,LVDDR3,2GBIT,8X11.1	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
33350555	4	HYNIX,LVDDR3,2GBIT,8X11.1	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_4GB
33350555	4	HYNIX,LVDDR3,2GBIT,8X11.1	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_4GB
33350556	4	SAMSUNG,LVDDR3,2GBIT,7,5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33350556	4	SAMSUNG,LVDDR3,2GBIT,7,5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33350556	4	SAMSUNG,LVDDR3,2GBIT,7,5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33350556	4	SAMSUNG,LVDDR3,2GBIT,7,5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33350557	4	MICRON,LVDDR3,2GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_4GB
33350557	4	MICRON,LVDDR3,2GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_4GB
33350557	4	MICRON,LVDDR3,2GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_4GB
33350557	4	MICRON,LVDDR3,2GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_4GB
33350566	4	ELPIDA,LVDDR3,2GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
33350566	4	ELPIDA,LVDDR3,2GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
33350566	4	ELPIDA,LVDDR3,2GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_4GB
33350566	4	ELPIDA,LVDDR3,2GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_4GB
35352392	1	IC,ISL6259,BATCHADDER,4040M,0P25	U7000	CRITICAL	ISL6259_SCREENED:NO
35352929	1	IC,ISL6259,BATCHADDER,34,4040M,0P25	U7000	CRITICAL	ISL6259_SCREENED:YES
607-6811	1	ASSEMBLY,STRAPKIT,PCBA,800,800,800,800	J6955	CRITICAL	

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A

SYNC MASTER=K24 MLB		SYNC DATE=07/20/2009	
PAGE TITLE			
BOM Configuration			
		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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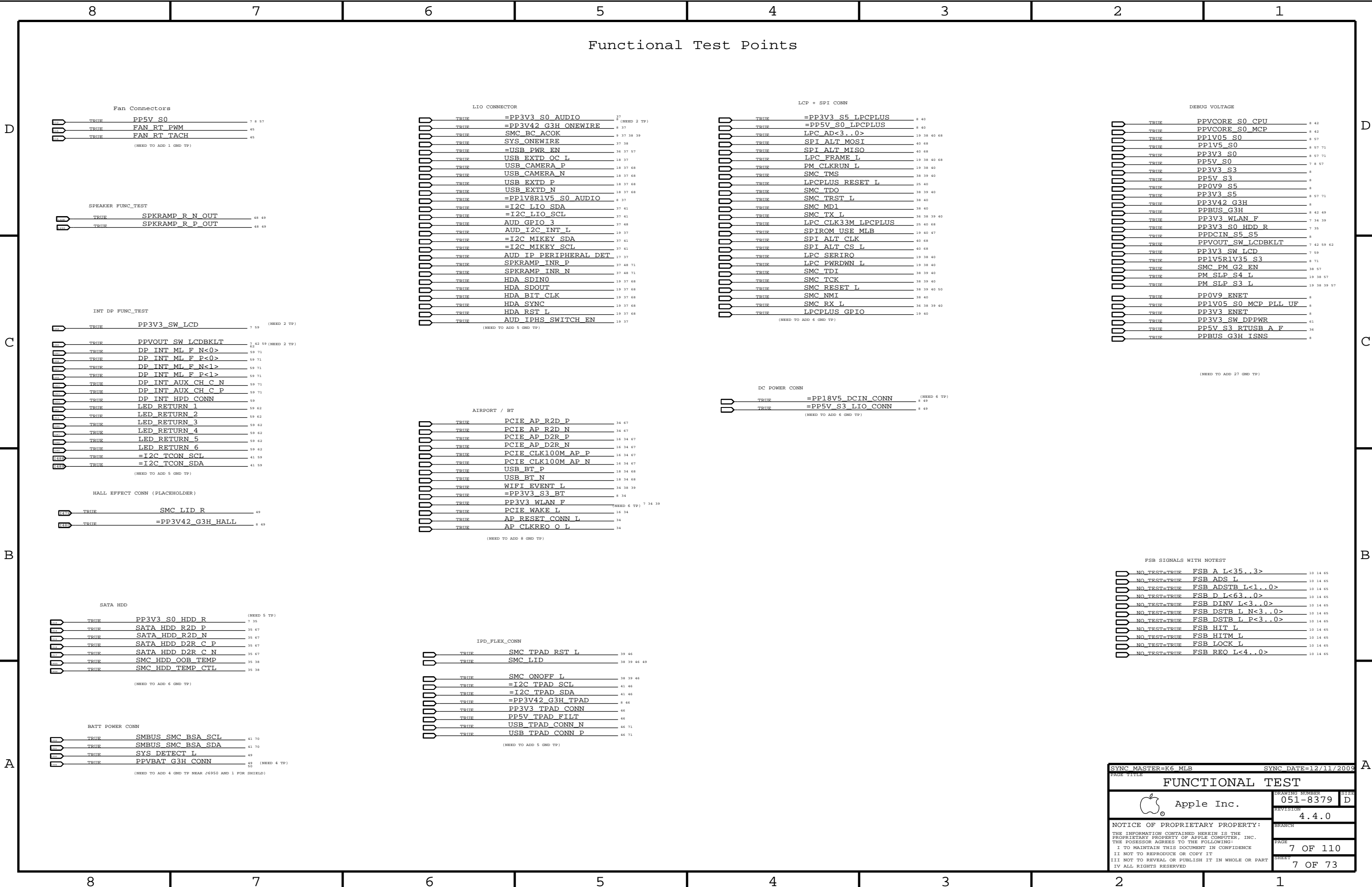
4

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1

Functional Test Points



Fan Connectors

TRUE PP5V S0 7 8 57
 TRUE FAN RT PWM 45
 TRUE FAN RT TACH 45
 (NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

TRUE SPKRAMP R N OUT 48 49
 TRUE SPKRAMP R P OUT 48 49

INT DP FUNC_TEST

TRUE PP3V3_SW_LCD 7 59 (NEED 2 TP)

TRUE PPVOUT_SW_LCDBKLT 7 42 59 (NEED 2 TP)
 TRUE DP INT ML F N<0> 59 71
 TRUE DP INT ML F P<0> 59 71
 TRUE DP INT ML F N<1> 59 71
 TRUE DP INT ML F P<1> 59 71
 TRUE DP INT AUX CH C N 59 71
 TRUE DP INT AUX CH C P 59 71
 TRUE DP INT HPD CONN 59
 TRUE LED RETURN 1 59 62
 TRUE LED RETURN 2 59 62
 TRUE LED RETURN 3 59 62
 TRUE LED RETURN 4 59 62
 TRUE LED RETURN 5 59 62
 TRUE LED RETURN 6 59 62
 TRUE =I2C_TCON_SCL 41 59
 TRUE =I2C_TCON_SDA 41 59
 (NEED TO ADD 5 GND TP)

HALL EFFECT CONN (PLACEHOLDER)

TRUE SMC LID R 49
 TRUE =PP3V42_G3H_HALL 8 49

SATA HDD

TRUE PP3V3_S0_HDD_R (NEED 5 TP) 7 35
 TRUE SATA_HDD_R2D_P 35 67
 TRUE SATA_HDD_R2D_N 35 67
 TRUE SATA_HDD_D2R_C_P 35 67
 TRUE SATA_HDD_D2R_C_N 35 67
 TRUE SMC_HDD_OOB_TEMP 35 38
 TRUE SMC_HDD_TEMP_CTL 35 38
 (NEED TO ADD 6 GND TP)

BATT POWER CONN

TRUE SMBUS_SMC_BSA_SCL 41 70
 TRUE SMBUS_SMC_BSA_SDA 41 70
 TRUE SYS_DETECT_L 49
 TRUE PPVBAT_G3H_CONN (NEED 4 TP) 88 89
 (NEED TO ADD 4 GND TP NEAR J6950 AND 1 FOR SHIELD)

LIO CONNECTOR

TRUE =PP3V3_S0_AUDIO 37 (NEED 2 TP)
 TRUE =PP3V42_G3H_ONEWIRE 8 37
 TRUE SMC_BC_ACOK 9 37 38 39
 TRUE SYS_ONEWIRE 37 38
 TRUE =USB_PWR_EN 36 37 57
 TRUE USB_EXTD_OC_L 18 37
 TRUE USB_CAMERA_P 18 37 68
 TRUE USB_CAMERA_N 18 37 68
 TRUE USB_EXTD_P 18 37 68
 TRUE USB_EXTD_N 18 37 68
 TRUE =PP1V8R1V5_S0_AUDIO 8 37
 TRUE =I2C_LIO_SDA 37 41
 TRUE =I2C_LIO_SCL 37 41
 TRUE AUD_GPIO_3 37 48
 TRUE AUD_I2C_INT_L 19 37
 TRUE =I2C_MIKEY_SDA 37 41
 TRUE =I2C_MIKEY_SCL 37 41
 TRUE AUD_IP_PERIPHERAL_DET 17 37
 TRUE SPKRAMP_INR_P 37 48 71
 TRUE SPKRAMP_INR_N 37 48 71
 TRUE HDA_SDIN0 19 37 68
 TRUE HDA_SDOUT 19 37 68
 TRUE HDA_BIT_CLK 19 37 68
 TRUE HDA_SYNC 19 37 68
 TRUE HDA_RST_L 19 37 68
 TRUE AUD_IPHS_SWITCH_EN 19 37
 (NEED TO ADD 5 GND TP)

AIRPORT / BT

TRUE PCIE_AP_R2D_P 34 67
 TRUE PCIE_AP_R2D_N 34 67
 TRUE PCIE_AP_D2R_P 16 34 67
 TRUE PCIE_AP_D2R_N 16 34 67
 TRUE PCIE_CLK100M_AP_P 16 34 67
 TRUE PCIE_CLK100M_AP_N 16 34 67
 TRUE USB_BT_P 18 34 68
 TRUE USB_BT_N 18 34 68
 TRUE WIFI_EVENT_L 34 38 39
 TRUE =PP3V3_S3_BT 8 34
 TRUE PP3V3_WLAN_F (NEED 6 TP) 7 34 39
 TRUE PCIE_WAKE_L 16 34
 TRUE AP_RESET_CONN_L 34
 TRUE AP_CLKREQ_O_L 34
 (NEED TO ADD 8 GND TP)

IPD_FLEX_CONN

TRUE SMC_TPAD_RST_L 39 46
 TRUE SMC_LID 38 39 46 49

TRUE SMC_ONOFF_L 38 39 46
 TRUE =I2C_TPAD_SCL 41 46
 TRUE =I2C_TPAD_SDA 41 46
 TRUE =PP3V42_G3H_TPAD 8 46
 TRUE PP3V3_TPAD_CONN 46
 TRUE PP5V_TPAD_FILT 46
 TRUE USB_TPAD_CONN_N 46 71
 TRUE USB_TPAD_CONN_P 46 71
 (NEED TO ADD 5 GND TP)

LCP + SPI CONN

TRUE =PP3V3_S5_LPCPLUS 8 40
 TRUE =PP5V_S0_LPCPLUS 8 40
 TRUE LPC_AD<3..0> 19 38 40 68
 TRUE SPI_ALT_MOSI 40 68
 TRUE SPI_ALT_MISO 40 68
 TRUE LPC_FRAME_L 19 38 40 68
 TRUE PM_CLKRUN_L 19 38 40
 TRUE SMC_TMS 38 39 40
 TRUE LPCPLUS_RESET_L 25 40
 TRUE SMC_TDO 38 39 40
 TRUE SMC_TRST_L 38 40
 TRUE SMC_MD1 38 40
 TRUE SMC_TX_L 36 38 39 40
 TRUE LPC_CLK33M_LPCPLUS 25 40 68
 TRUE SPIROM_USE_MLB 19 40 47
 TRUE SPI_ALT_CLK 40 68
 TRUE SPI_ALT_CS_L 40 68
 TRUE LPC_SERIRO 19 38 40
 TRUE LPC_PWRDWN_L 19 38 40
 TRUE SMC_TDI 38 39 40
 TRUE SMC_TCK 38 39 40
 TRUE SMC_RESET_L 38 39 40 50
 TRUE SMC_NMI 38 40
 TRUE SMC_RX_L 36 38 39 40
 TRUE LPCPLUS_GPIO 19 40
 (NEED TO ADD 6 GND TP)

DC POWER CONN

TRUE =PP18V5_DCIN_CONN (NEED 6 TP) 8 49
 TRUE =PP5V_S3_LIO_CONN (NEED 6 GND TP) 8 49

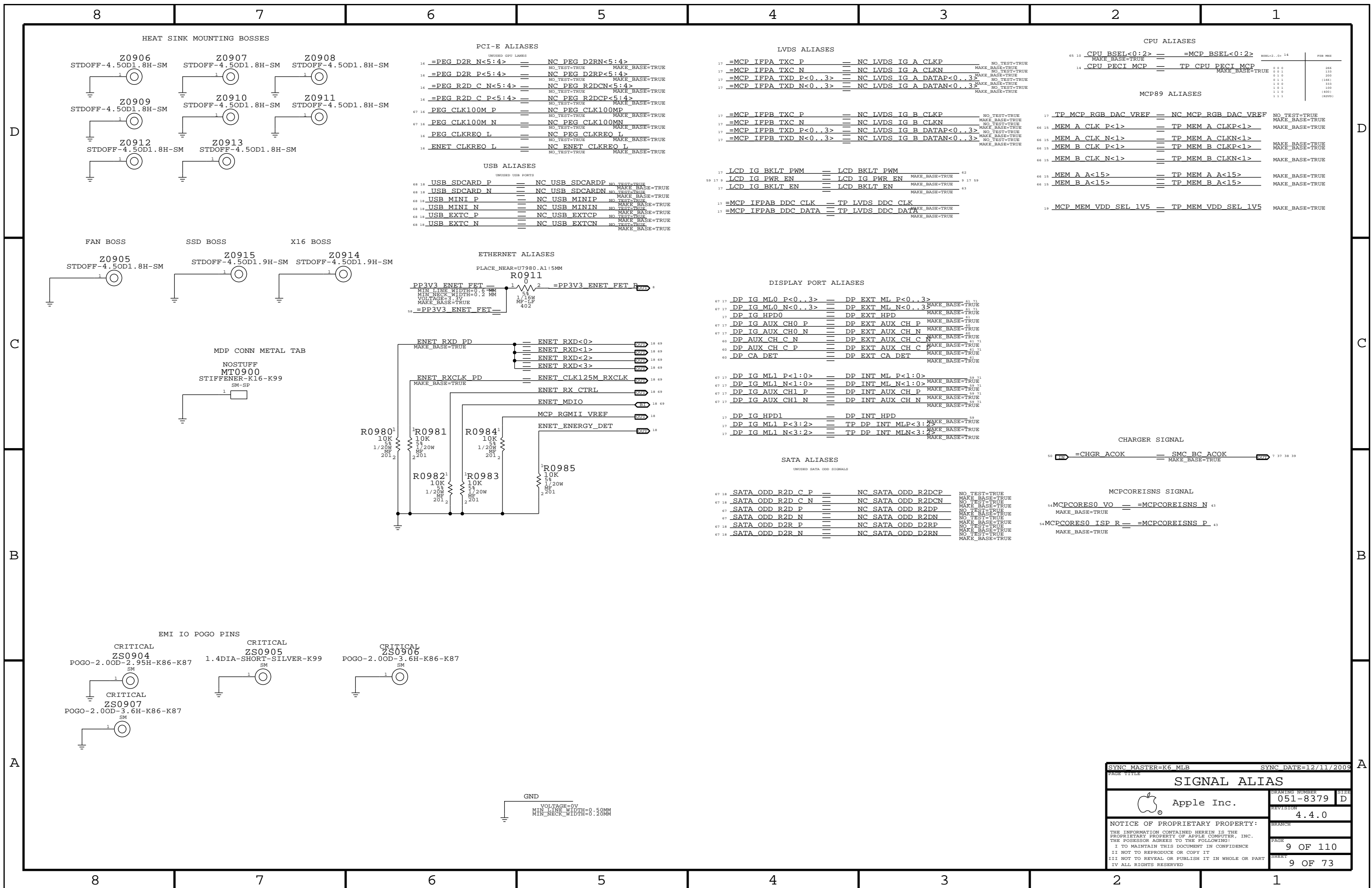
DEBUG VOLTAGE

TRUE PPVCORE_S0_CPU 8 42
 TRUE PPVCORE_S0_MCP 8 42
 TRUE PP1V05_S0 8 57
 TRUE PP1V5_S0 8 57 71
 TRUE PP3V3_S0 8 57 71
 TRUE PP5V_S0 7 8 57
 TRUE PP3V3_S3 8
 TRUE PP5V_S3 8
 TRUE PP0V9_S5 8
 TRUE PP3V3_S5 8 57 71
 TRUE PP3V42_G3H 8
 TRUE PPBUS_G3H 8 42 49
 TRUE PP3V3_WLAN_F 7 34 39
 TRUE PP3V3_S0_HDD_R 7 35
 TRUE PPDCIN_S5_S5 8
 TRUE PPVOUT_SW_LCDBKLT 7 42 59 62
 TRUE PP3V3_SW_LCD 7 59
 TRUE PP1V5R1V35_S3 8 71
 TRUE SMC_PM_G2_EN 38 57
 TRUE PM_SLP_S4_L 19 38 57
 TRUE PM_SLP_S3_L 19 38 57
 TRUE PP0V9_ENET 8
 TRUE PP1V05_S0_MCP_PLL_UP 8
 TRUE PP3V3_ENET 8
 TRUE PP3V3_SW_DPPWR 61
 TRUE PP5V_S3_RTUSB_A_F 36
 TRUE PPBUS_G3H_ISNS 8
 (NEED TO ADD 27 GND TP)

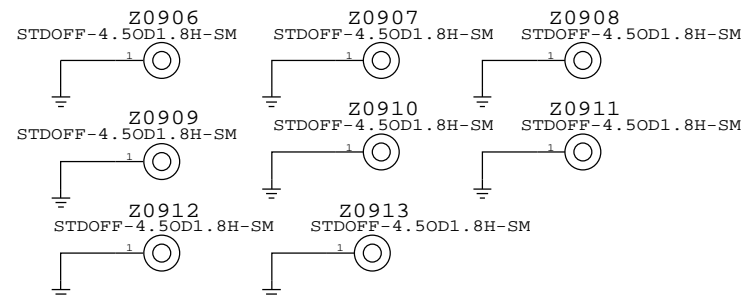
FSB SIGNALS WITH NOTEST

NO_TEST=TRUE FSB_A_L<35..3> 10 14 65
 NO_TEST=TRUE FSB_ADS_L 10 14 65
 NO_TEST=TRUE FSB_ADSTB_L<1..0> 10 14 65
 NO_TEST=TRUE FSB_D_L<63..0> 10 14 65
 NO_TEST=TRUE FSB_DINV_L<3..0> 10 14 65
 NO_TEST=TRUE FSB_DSTB_L_N<3..0> 10 14 65
 NO_TEST=TRUE FSB_DSTB_L_P<3..0> 10 14 65
 NO_TEST=TRUE FSB_HIT_L 10 14 65
 NO_TEST=TRUE FSB_HITM_L 10 14 65
 NO_TEST=TRUE FSB_LOCK_L 10 14 65
 NO_TEST=TRUE FSB_REO_L<4..0> 10 14 65

SYNC MASTER=K6_MLB		SYNC DATE=12/11/2009	
FUNCTIONAL TEST			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8379	D
		REVISION	
		4.4.0	
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HEAT SINK MOUNTING BOSSSES



PCI-E ALIASES

- UNUSED GPU LANES
- =PEG D2R N<5:4> == NC_PEG_D2RN<5:4> NO_TEST=TRUE MAKE_BASE=TRUE
 - =PEG D2R P<5:4> == NC_PEG_D2RP<5:4> NO_TEST=TRUE MAKE_BASE=TRUE
 - =PEG R2D C N<5:4> == NC_PEG_R2DCN<5:4> NO_TEST=TRUE MAKE_BASE=TRUE
 - =PEG R2D C P<5:4> == NC_PEG_R2DCP<5:4> NO_TEST=TRUE MAKE_BASE=TRUE
 - PEG CLK100M P == NC_PEG_CLK100MP NO_TEST=TRUE MAKE_BASE=TRUE
 - PEG CLK100M N == NC_PEG_CLK100MN NO_TEST=TRUE MAKE_BASE=TRUE
 - PEG CLKREQ L == NC_PEG_CLKREQ_L NO_TEST=TRUE MAKE_BASE=TRUE
 - ENET CLKREQ L == NC_ENET_CLKREQ_L NO_TEST=TRUE MAKE_BASE=TRUE

USB ALIASES

- UNUSED USB PORTS
- USB_SDCARD_P == NC_USB_SDCARDP NO_TEST=TRUE MAKE_BASE=TRUE
 - USB_SDCARD_N == NC_USB_SDCARDN NO_TEST=TRUE MAKE_BASE=TRUE
 - USB_MINI_P == NC_USB_MINIP NO_TEST=TRUE MAKE_BASE=TRUE
 - USB_MINI_N == NC_USB_MININ NO_TEST=TRUE MAKE_BASE=TRUE
 - USB_EXTC_P == NC_USB_EXTCP NO_TEST=TRUE MAKE_BASE=TRUE
 - USB_EXTC_N == NC_USB_EXTCN NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

- =MCP_IFPA_TXC_P == NC_LVDS_IG_A_CLKP NO_TEST=TRUE MAKE_BASE=TRUE
- =MCP_IFPA_TXC_N == NC_LVDS_IG_A_CLKN NO_TEST=TRUE MAKE_BASE=TRUE
- =MCP_IFPA_TXD_P<0..3> == NC_LVDS_IG_A_DATAP<0..3> NO_TEST=TRUE MAKE_BASE=TRUE
- =MCP_IFPA_TXD_N<0..3> == NC_LVDS_IG_A_DATAN<0..3> NO_TEST=TRUE MAKE_BASE=TRUE
- =MCP_IFPB_TXC_P == NC_LVDS_IG_B_CLKP NO_TEST=TRUE MAKE_BASE=TRUE
- =MCP_IFPB_TXC_N == NC_LVDS_IG_B_CLKN NO_TEST=TRUE MAKE_BASE=TRUE
- =MCP_IFPB_TXD_P<0..3> == NC_LVDS_IG_B_DATAP<0..3> NO_TEST=TRUE MAKE_BASE=TRUE
- =MCP_IFPB_TXD_N<0..3> == NC_LVDS_IG_B_DATAN<0..3> NO_TEST=TRUE MAKE_BASE=TRUE

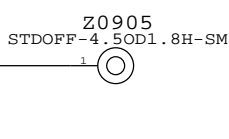
CPU ALIASES

- CPU_BSEL<0:2> == MCP_BSEL<0:2> NO_TEST=TRUE MAKE_BASE=TRUE
- CPU_PECI_MCP == TP_CPU_PECI_MCP NO_TEST=TRUE MAKE_BASE=TRUE

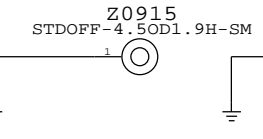
MCP89 ALIASES

- TP_MCP_RGB_DAC_VREF == NC_MCP_RGB_DAC_VREF NO_TEST=TRUE MAKE_BASE=TRUE
- MEM_A_CLK_P<1> == TP_MEM_A_CLKP<1> NO_TEST=TRUE MAKE_BASE=TRUE
- MEM_A_CLK_N<1> == TP_MEM_A_CLKN<1> NO_TEST=TRUE MAKE_BASE=TRUE
- MEM_B_CLK_P<1> == TP_MEM_B_CLKP<1> NO_TEST=TRUE MAKE_BASE=TRUE
- MEM_B_CLK_N<1> == TP_MEM_B_CLKN<1> NO_TEST=TRUE MAKE_BASE=TRUE
- MEM_A_A<15> == TP_MEM_A_A<15> NO_TEST=TRUE MAKE_BASE=TRUE
- MEM_B_A<15> == TP_MEM_B_A<15> NO_TEST=TRUE MAKE_BASE=TRUE
- MCP_MEM_VDD_SEL_1V5 == TP_MEM_VDD_SEL_1V5 NO_TEST=TRUE MAKE_BASE=TRUE

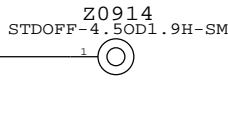
FAN BOSS



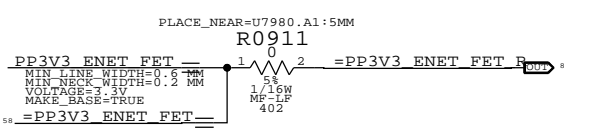
SSD BOSS



X16 BOSS



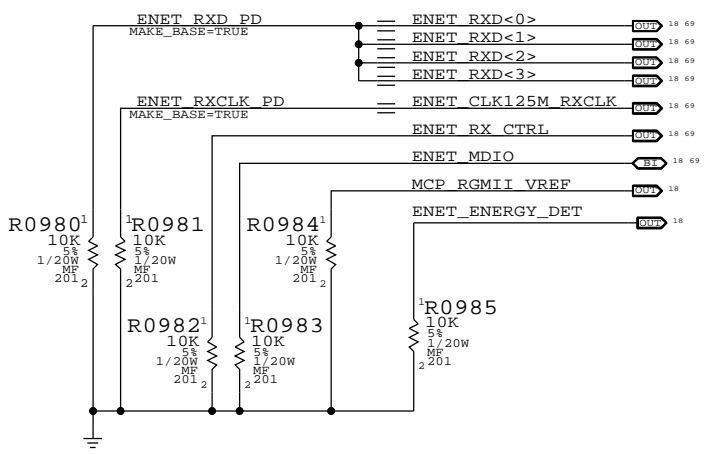
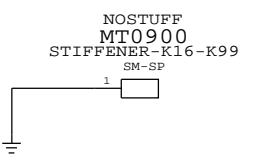
ETHERNET ALIASES



DISPLAY PORT ALIASES

- DP_IG_ML0_P<0..3> == DP_EXT_ML_P<0..3> NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_ML0_N<0..3> == DP_EXT_ML_N<0..3> NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_HPDP0 == DP_EXT_HPDP NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_AUX_CH0_P == DP_EXT_AUX_CH_P NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_AUX_CH0_N == DP_EXT_AUX_CH_N NO_TEST=TRUE MAKE_BASE=TRUE
- DP_AUX_CH_C_N == DP_EXT_AUX_CH_C_N NO_TEST=TRUE MAKE_BASE=TRUE
- DP_AUX_CH_C_P == DP_EXT_AUX_CH_C_P NO_TEST=TRUE MAKE_BASE=TRUE
- DP_CA_DET == DP_EXT_CA_DET NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_ML1_P<1:0> == DP_INT_ML_P<1:0> NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_ML1_N<1:0> == DP_INT_ML_N<1:0> NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_AUX_CH1_P == DP_INT_AUX_CH_P NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_AUX_CH1_N == DP_INT_AUX_CH_N NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_HPDP1 == DP_INT_HPDP NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_ML1_P<3:2> == TP_DP_INT_MLP<3:2> NO_TEST=TRUE MAKE_BASE=TRUE
- DP_IG_ML1_N<3:2> == TP_DP_INT_MLN<3:2> NO_TEST=TRUE MAKE_BASE=TRUE

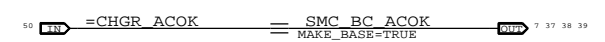
MDP CONN METAL TAB



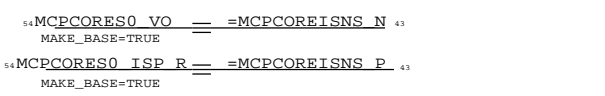
SATA ALIASES

- UNUSED SATA ODD SIGNALS
- SATA_ODD_R2D_C_P == NC_SATA_ODD_R2DCP NO_TEST=TRUE MAKE_BASE=TRUE
 - SATA_ODD_R2D_C_N == NC_SATA_ODD_R2DCN NO_TEST=TRUE MAKE_BASE=TRUE
 - SATA_ODD_R2D_P == NC_SATA_ODD_R2DP NO_TEST=TRUE MAKE_BASE=TRUE
 - SATA_ODD_R2D_N == NC_SATA_ODD_R2DN NO_TEST=TRUE MAKE_BASE=TRUE
 - SATA_ODD_D2R_P == NC_SATA_ODD_D2RP NO_TEST=TRUE MAKE_BASE=TRUE
 - SATA_ODD_D2R_N == NC_SATA_ODD_D2RN NO_TEST=TRUE MAKE_BASE=TRUE

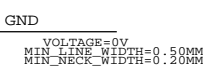
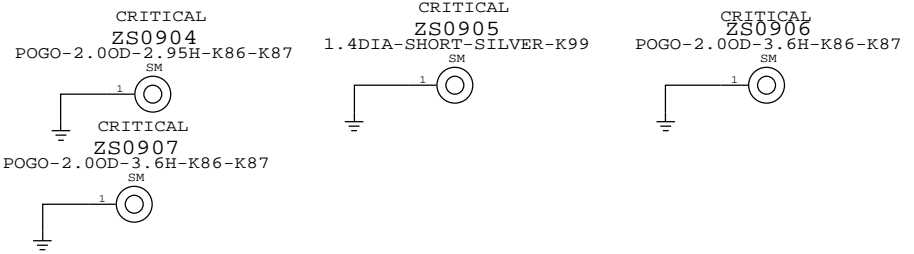
CHARGER SIGNAL



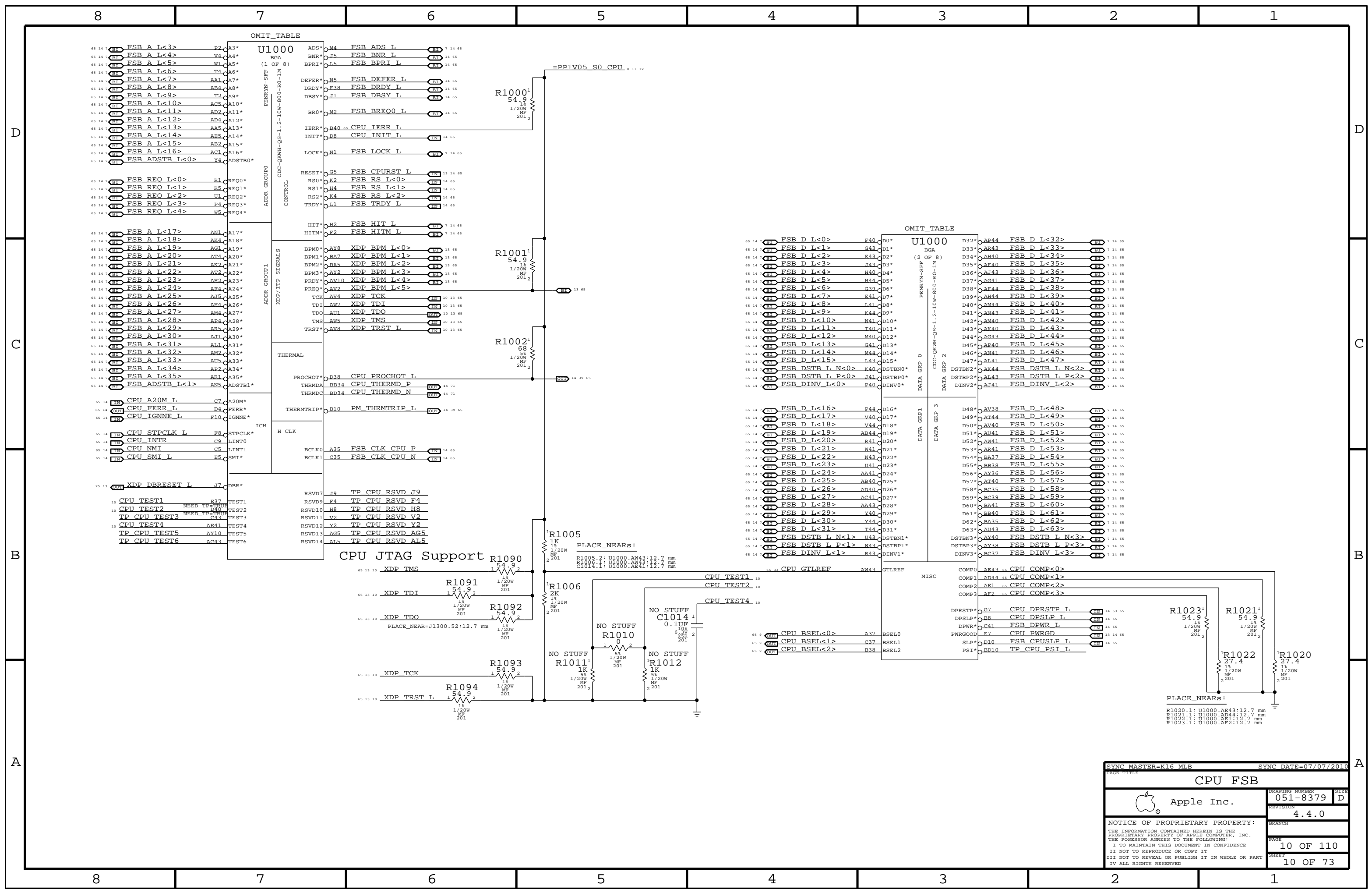
MCPCOREISNS SIGNAL



EMI IO POGO PINS



SYNC MASTER=K6 MLB		SYNC DATE=12/11/2009	
SIGNAL ALIAS			
Apple Inc.		DRAWING NUMBER	051-8379
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		PAGE	9 OF 110
		SHEET	9 OF 73

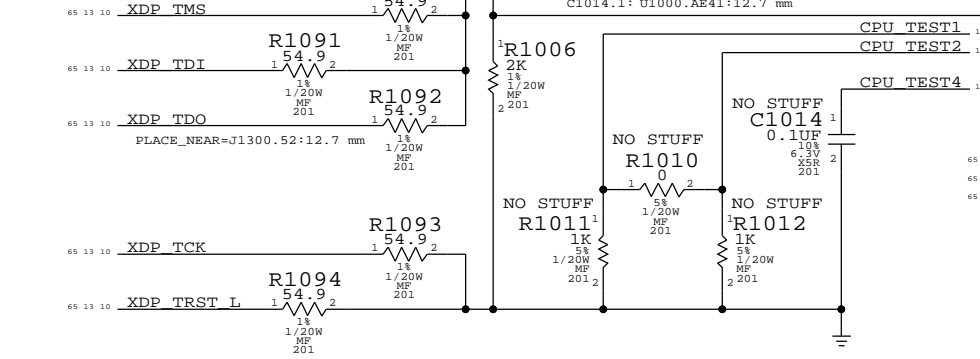


OMIT_TABLE

Pin	Signal	Processor Pin	Processor Pin
65 14	FSB A L<3>	P2	A3*
65 14	FSB A L<4>	Y4	A4*
65 14	FSB A L<5>	W1	A5*
65 14	FSB A L<6>	T4	A6*
65 14	FSB A L<7>	AA1	A7*
65 14	FSB A L<8>	AB4	A8*
65 14	FSB A L<9>	T2	A9*
65 14	FSB A L<10>	AC5	A10*
65 14	FSB A L<11>	AD2	A11*
65 14	FSB A L<12>	AD4	A12*
65 14	FSB A L<13>	AA5	A13*
65 14	FSB A L<14>	AE5	A14*
65 14	FSB A L<15>	AB2	A15*
65 14	FSB A L<16>	AC1	A16*
65 14	FSB ADSTB L<0>	Y4	ADSTB0*
65 14	FSB REQ L<0>	R1	REQ0*
65 14	FSB REQ L<1>	R5	REQ1*
65 14	FSB REQ L<2>	U1	REQ2*
65 14	FSB REQ L<3>	P4	REQ3*
65 14	FSB REQ L<4>	W5	REQ4*
65 14	FSB A L<17>	AN1	A17*
65 14	FSB A L<18>	AK4	A18*
65 14	FSB A L<19>	AG1	A19*
65 14	FSB A L<20>	AT4	A20*
65 14	FSB A L<21>	AK2	A21*
65 14	FSB A L<22>	AT2	A22*
65 14	FSB A L<23>	AH2	A23*
65 14	FSB A L<24>	AF4	A24*
65 14	FSB A L<25>	AV5	A25*
65 14	FSB A L<26>	AH4	A26*
65 14	FSB A L<27>	AM4	A27*
65 14	FSB A L<28>	AP4	A28*
65 14	FSB A L<29>	AR5	A29*
65 14	FSB A L<30>	AT1	A30*
65 14	FSB A L<31>	AL1	A31*
65 14	FSB A L<32>	AM2	A32*
65 14	FSB A L<33>	AU5	A33*
65 14	FSB A L<34>	AP2	A34*
65 14	FSB A L<35>	AR1	A35*
65 14	FSB ADSTB L<1>	AN5	ADSTB1*
65 14	CPU A20M L	C7	A20M*
65 14	CPU FERR L	D4	FERR*
65 14	CPU IGNNE L	F10	IGNNE*
65 14	CPU STPCLK L	F8	STPCLK*
65 14	CPU INTR	C9	LINT0
65 14	CPU NMI	C5	LINT1
65 14	CPU SMI L	R5	SMI*
65 14	XDP DBRESET L	J7	DBR*
10	CPU TEST1	E37	TEST1
10	CPU TEST2	NEED_TP=TRUE D10	TEST2
10	TP CPU TEST3	NEED_TP=TRUE C13	TEST3
10	CPU TEST4	AE41	TEST4
10	TP CPU TEST5	AY10	TEST5
10	TP CPU TEST6	AC43	TEST6

Pin	Signal	Processor Pin	Processor Pin
65 14	ADS*	M4	FSB ADS L
65 14	BNR*	J5	FSB BNR L
65 14	BPRI*	L5	FSB BPRI L
65 14	DEFER*	N5	FSB DEFER L
65 14	DRDY*	F38	FSB DRDY L
65 14	DBSY*	J1	FSB DBSY L
65 14	BR0*	M2	FSB BRE00 L
65 14	IERR*	B40	CPU IERR L
65 14	INIT*	DB8	CPU INIT L
65 14	LOCK*	W1	FSB LOCK L
65 14	RESET*	G5	FSB CPURST L
65 14	RS0*	X2	FSB RS L<0>
65 14	RS1*	H4	FSB RS L<1>
65 14	RS2*	K4	FSB RS L<2>
65 14	TRDY*	L1	FSB TRDY L
65 14	HIT*	H2	FSB HIT L
65 14	HITM*	F2	FSB HITM L
65 14	BPM0*	AY8	XDP BPM L<0>
65 14	BPM1*	BA7	XDP BPM L<1>
65 14	BPM2*	BA5	XDP BPM L<2>
65 14	BPM3*	AY2	XDP BPM L<3>
65 14	PRDY*	AV10	XDP BPM L<4>
65 14	PREQ*	AV2	XDP BPM L<5>
65 14	TCK	AV4	XDP TCK
65 14	TDI	AM7	XDP TDI
65 14	TDO	AM1	XDP TDO
65 14	TMS	AM5	XDP TMS
65 14	TRST*	AV8	XDP TRST L
65 14	PROCHOT*	D38	CPU PROCHOT L
65 14	THRMDA	BB34	CPU THERMD P
65 14	THRMDC	BD34	CPU THERMD N
65 14	THERMTRIP*	R10	PM THERMTRIP L
65 14	BCLK0	A35	FSB CLK CPU P
65 14	BCLK1	C35	FSB CLK CPU N
65 14	RSVD7	J9	TP CPU RSVD J9
65 14	RSVD9	F4	TP CPU RSVD F4
65 14	RSVD10	H8	TP CPU RSVD H8
65 14	RSVD11	V2	TP CPU RSVD V2
65 14	RSVD12	Y2	TP CPU RSVD Y2
65 14	RSVD13	AG5	TP CPU RSVD AG5
65 14	RSVD14	AL5	TP CPU RSVD AL5

CPU JTAG Support

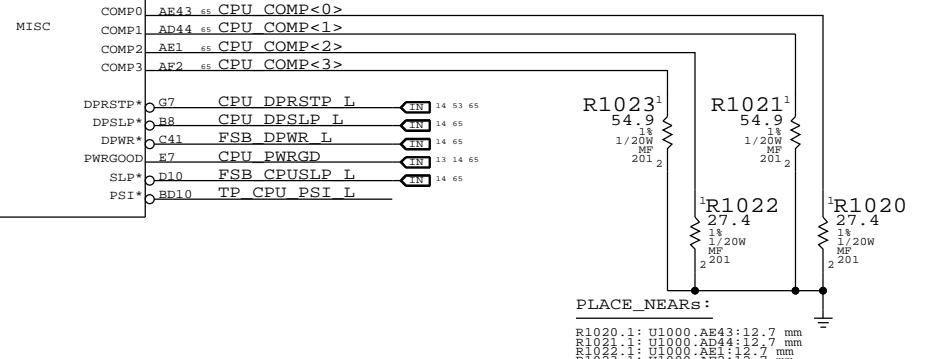


PLACE_NEARS:

R1005.2:	U1000.AW43:12.7	mm
R1006.1:	U1000.AW43:12.7	mm
C1014.1:	U1000.AE41:12.7	mm

OMIT_TABLE

Pin	Signal	Processor Pin	Processor Pin
65 14	FSB D L<0>	F40	D0*
65 14	FSB D L<1>	G43	D1*
65 14	FSB D L<2>	E43	D2*
65 14	FSB D L<3>	F43	D3*
65 14	FSB D L<4>	H40	D4*
65 14	FSB D L<5>	H44	D5*
65 14	FSB D L<6>	G39	D6*
65 14	FSB D L<7>	E41	D7*
65 14	FSB D L<8>	L41	D8*
65 14	FSB D L<9>	K44	D9*
65 14	FSB D L<10>	N41	D10*
65 14	FSB D L<11>	T40	D11*
65 14	FSB D L<12>	M40	D12*
65 14	FSB D L<13>	G41	D13*
65 14	FSB D L<14>	M44	D14*
65 14	FSB D L<15>	L43	D15*
65 14	FSB DSTB L N<0>	K40	DSTBN0*
65 14	FSB DSTB L P<0>	J41	DSTBP0*
65 14	FSB DINV L<0>	P40	DINV0*
65 14	FSB D L<16>	P44	D16*
65 14	FSB D L<17>	V40	D17*
65 14	FSB D L<18>	V44	D18*
65 14	FSB D L<19>	AB44	D19*
65 14	FSB D L<20>	R41	D20*
65 14	FSB D L<21>	M41	D21*
65 14	FSB D L<22>	N43	D22*
65 14	FSB D L<23>	U41	D23*
65 14	FSB D L<24>	AA41	D24*
65 14	FSB D L<25>	AB40	D25*
65 14	FSB D L<26>	AD40	D26*
65 14	FSB D L<27>	AC41	D27*
65 14	FSB D L<28>	AA43	D28*
65 14	FSB D L<29>	Y40	D29*
65 14	FSB D L<30>	Y44	D30*
65 14	FSB D L<31>	T44	D31*
65 14	FSB DSTB L N<1>	U43	DSTBN1*
65 14	FSB DSTB L P<1>	W43	DSTBP1*
65 14	FSB DINV L<1>	R43	DINV1*
65 14	AP44	FSB D L<32>	D32*
65 14	AR43	FSB D L<33>	D33*
65 14	AH40	FSB D L<34>	D34*
65 14	AF40	FSB D L<35>	D35*
65 14	AT43	FSB D L<36>	D36*
65 14	AG41	FSB D L<37>	D37*
65 14	AF44	FSB D L<38>	D38*
65 14	AH44	FSB D L<39>	D39*
65 14	AM44	FSB D L<40>	D40*
65 14	AW43	FSB D L<41>	D41*
65 14	AM40	FSB D L<42>	D42*
65 14	AK40	FSB D L<43>	D43*
65 14	AG43	FSB D L<44>	D44*
65 14	AP40	FSB D L<45>	D45*
65 14	AN41	FSB D L<46>	D46*
65 14	AL41	FSB D L<47>	D47*
65 14	AV40	FSB DSTB L N<2>	DSTBN2*
65 14	AL43	FSB DSTB L P<2>	DSTBP2*
65 14	AW41	FSB DINV L<2>	DINV2*
65 14	AV38	FSB D L<48>	D48*
65 14	AT44	FSB D L<49>	D49*
65 14	AV40	FSB D L<50>	D50*
65 14	AU41	FSB D L<51>	D51*
65 14	AW41	FSB D L<52>	D52*
65 14	AR41	FSB D L<53>	D53*
65 14	BA37	FSB D L<54>	D54*
65 14	BB38	FSB D L<55>	D55*
65 14	AY36	FSB D L<56>	D56*
65 14	AT40	FSB D L<57>	D57*
65 14	BC35	FSB D L<58>	D58*
65 14	BC39	FSB D L<59>	D59*
65 14	BA41	FSB D L<60>	D60*
65 14	BB40	FSB D L<61>	D61*
65 14	BA35	FSB D L<62>	D62*
65 14	AU43	FSB D L<63>	D63*
65 14	AY40	FSB DSTB L N<3>	DSTBN3*
65 14	AY38	FSB DSTB L P<3>	DSTBP3*
65 14	BC37	FSB DINV L<3>	DINV3*
65 14	AE43	CPU COMP<0>	COMP0
65 14	AD44	CPU COMP<1>	COMP1
65 14	AE1	CPU COMP<2>	COMP2
65 14	AF2	CPU COMP<3>	COMP3
65 14	G7	CPU DPRSTP L	DPRSTP*
65 14	B8	CPU DPSP L	DPSP*
65 14	C41	FSB DPWR L	DPWR*
65 14	E7	CPU PWRGD	PWRGD*
65 14	D10	FSB CPUSLP L	SLP*
65 14	BD10	TP CPU PSI L	PSI*



PLACE_NEARS:

R1020.1:	U1000.AE43:12.7	mm
R1021.1:	U1000.AE44:12.7	mm
R1022.1:	U1000.AE1:12.7	mm
R1023.1:	U1000.AE2:12.7	mm

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

CPU FSB

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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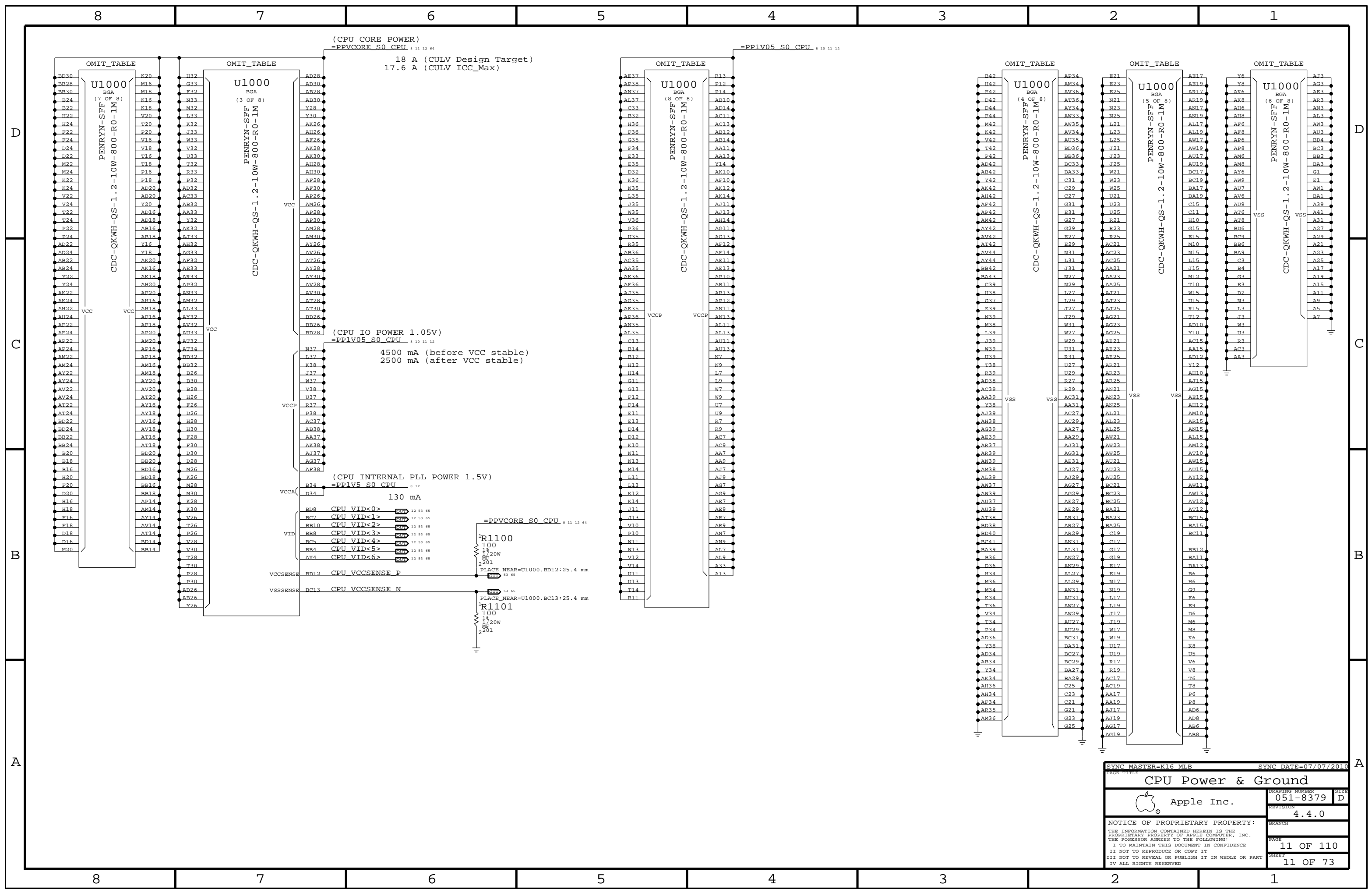
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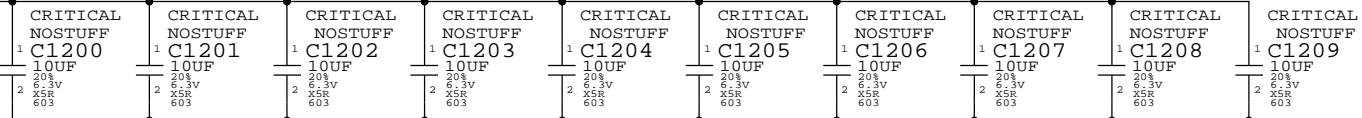


SYNC MASTER=K16.MLB		SYNC DATE=07/07/2010	
CPU Power & Ground			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8379	D
		REVISION	
		4.4.0	
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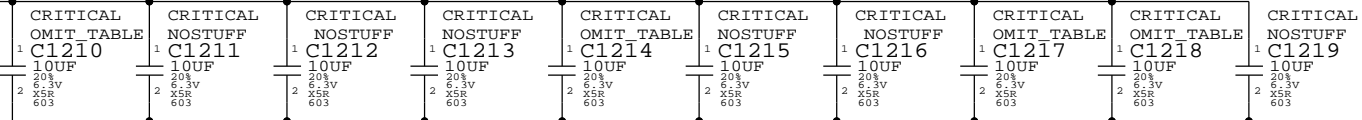
CPU VCORE HF AND BULK DECOUPLING

4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

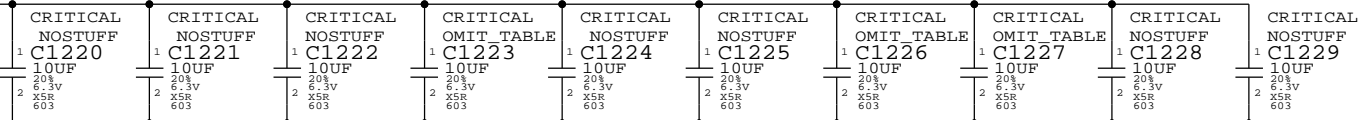
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



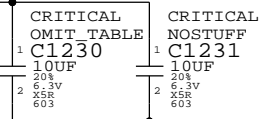
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



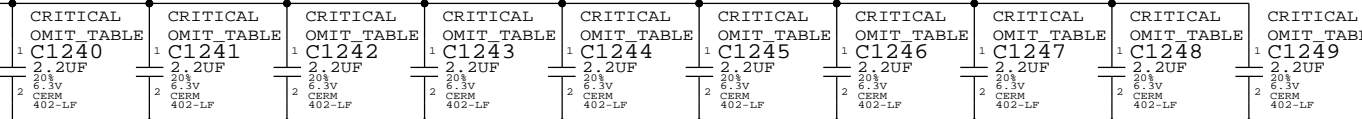
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



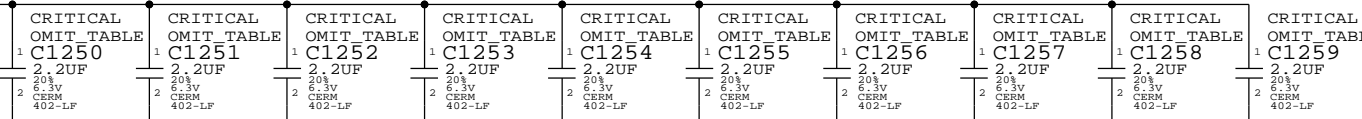
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



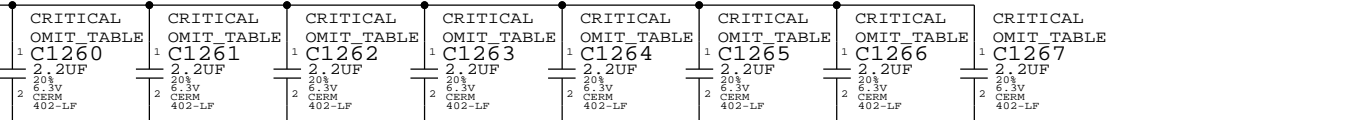
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



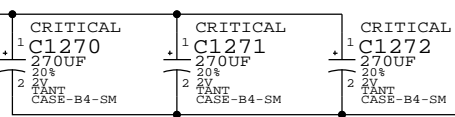
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

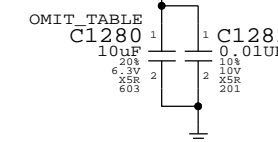


CPU VCORE VID CONNECTIONS

CPU VID<0..6> = IMVP6 VID<0..6>

VCCA (CPU AVdd) DECOUPLING

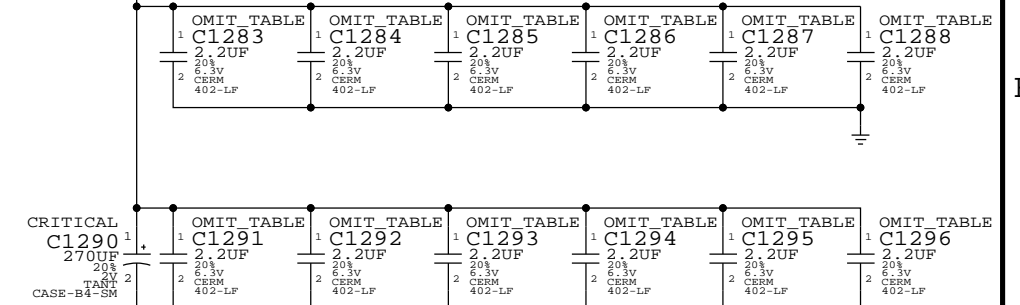
1x 10uF, 1x 0.01uF



LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

1x 270uF, 12x 2.2uF

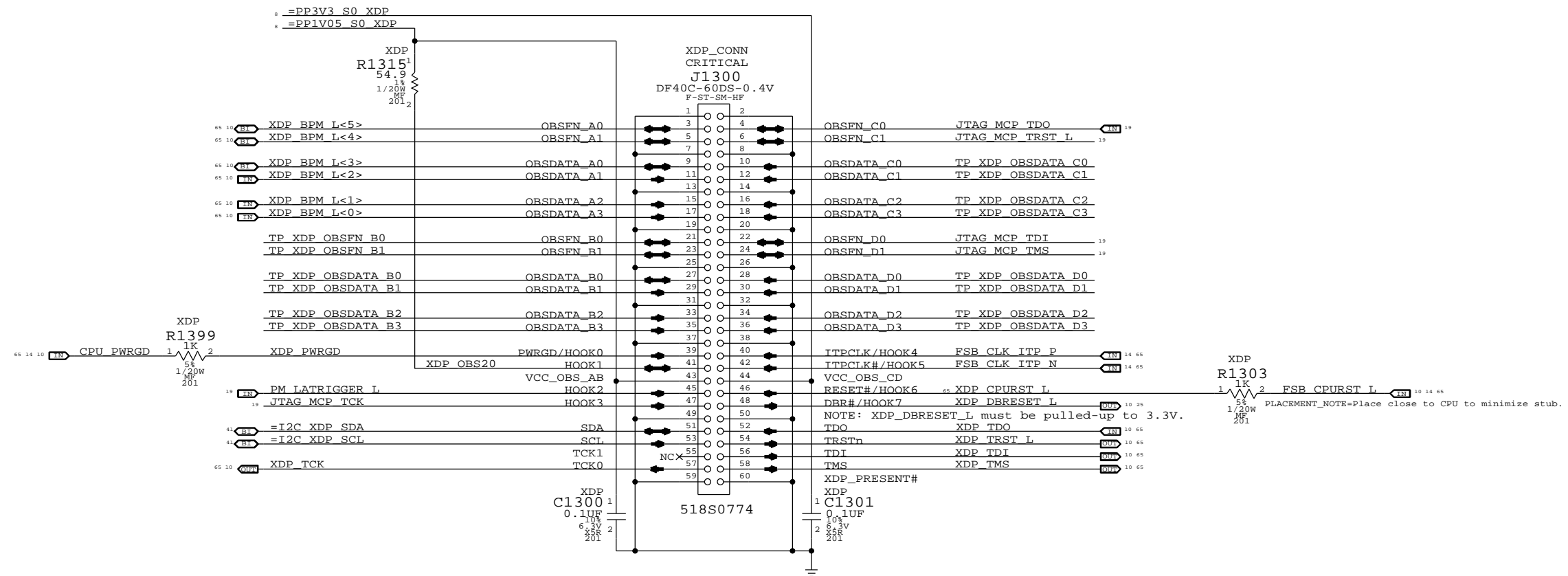


LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

SYNC MASTER=K16 MLB		SYNC DATE=03/24/2010	
CPU Decoupling & VID			
Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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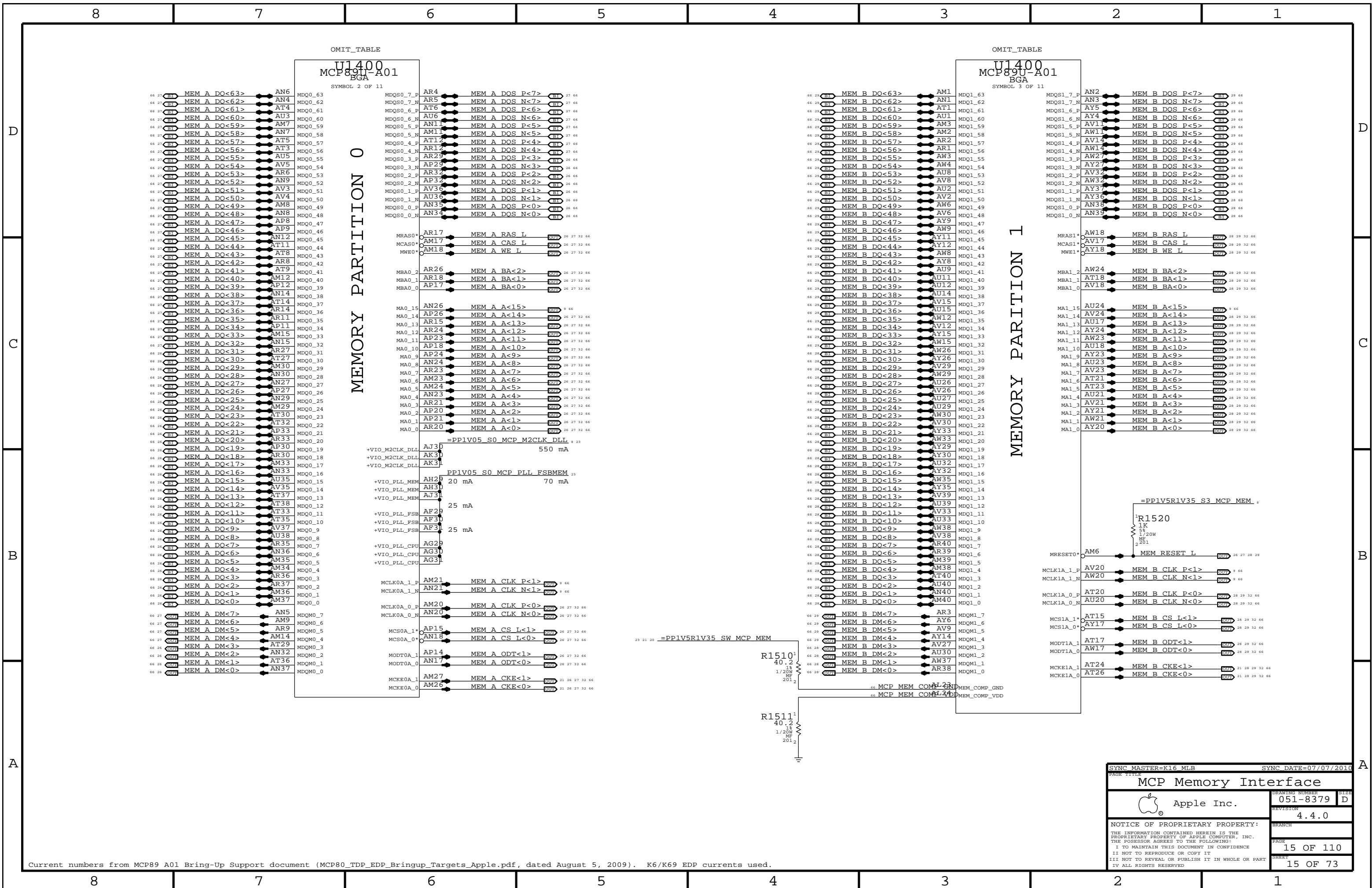
Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0782 Adapter Flex to support chipset debug.



← Direction of XDP adapter flex
Please place J1300 within 1" of board edge with odd-numbered pins facing edge. Avoid any tall components between J1300 and edge.

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
eXtended Debug Port (Micro-XDP)			
Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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OMIT_TABLE

U1400
MCP89U-A01
BGA

SYMBOL 2 OF 11

MEMORY PARTITION 0

OMIT_TABLE

U1400
MCP89U-A01
BGA

SYMBOL 3 OF 11

MEMORY PARTITION 1

MDQS0_7_P	AR4	MEM A DOS P<7>	27	66
MDQS0_7_N	AR5	MEM A DOS N<7>	27	66
MDQS0_6_P	AT6	MEM A DOS P<6>	27	66
MDQS0_6_N	AU6	MEM A DOS N<6>	27	66
MDQS0_5_P	AN11	MEM A DOS P<5>	27	66
MDQS0_5_N	AM11	MEM A DOS N<5>	27	66
MDQS0_4_P	AT12	MEM A DOS P<4>	27	66
MDQS0_4_N	AR12	MEM A DOS N<4>	27	66
MDQS0_3_P	AP29	MEM A DOS P<3>	26	66
MDQS0_3_N	AM29	MEM A DOS N<3>	26	66
MDQS0_2_P	AR32	MEM A DOS P<2>	26	66
MDQS0_2_N	AP32	MEM A DOS N<2>	26	66
MDQS0_1_P	AV36	MEM A DOS P<1>	26	66
MDQS0_1_N	AU36	MEM A DOS N<1>	26	66
MDQS0_0_P	AN35	MEM A DOS P<0>	26	66
MDQS0_0_N	AM34	MEM A DOS N<0>	26	66
MRAS0*	AR17	MEM A RAS L	26	32 66
MCAS0*	AM17	MEM A CAS L	26	32 66
MWE0*	AM18	MEM A WE L	26	32 66
MBA0_2	AR26	MEM A BA<2>	26	32 66
MBA0_1	AR18	MEM A BA<1>	26	32 66
MBA0_0	AP17	MEM A BA<0>	26	32 66
MA0_15	AN26	MEM A A<15>	9	66
MA0_14	AP26	MEM A A<14>	26	32 66
MA0_13	AR15	MEM A A<13>	26	32 66
MA0_12	AR24	MEM A A<12>	26	32 66
MA0_11	AP23	MEM A A<11>	26	32 66
MA0_10	AP18	MEM A A<10>	26	32 66
MA0_9	AP24	MEM A A<9>	26	32 66
MA0_8	AN24	MEM A A<8>	26	32 66
MA0_7	AR23	MEM A A<7>	26	32 66
MA0_6	AM23	MEM A A<6>	26	32 66
MA0_5	AM24	MEM A A<5>	26	32 66
MA0_4	AM23	MEM A A<4>	26	32 66
MA0_3	AR21	MEM A A<3>	26	32 66
MA0_2	AP20	MEM A A<2>	26	32 66
MA0_1	AP21	MEM A A<1>	26	32 66
MA0_0	AR20	MEM A A<0>	26	32 66
+VIO_M2CLK_DLL	AJ30	=PP1V05 S0 MCP M2CLK_DLL	8	23
+VIO_M2CLK_DLL	AK30	550 mA		
+VIO_M2CLK_DLL	AK31			
+VIO_PLL_MEM	AH29	PP1V05 S0 MCP PLL FSBMEM	23	
+VIO_PLL_MEM	AH30	20 mA	70 mA	
+VIO_PLL_MEM	AJ31			
+VIO_PLL_FSB	AF29	25 mA		
+VIO_PLL_FSB	AF30			
+VIO_PLL_FSB	AF31	25 mA		
+VIO_PLL_CPU	AG29			
+VIO_PLL_CPU	AG30			
+VIO_PLL_CPU	AG31			
MCLK0A_1_P	AM21	MEM A CLK P<1>	26	32 66
MCLK0A_1_N	AN21	MEM A CLK N<1>	26	32 66
MCLK0A_0_P	AM20	MEM A CLK P<0>	26	32 66
MCLK0A_0_N	AN20	MEM A CLK N<0>	26	32 66
MCS0A_1*	AP15	MEM A CS L<1>	26	32 66
MCS0A_0*	AN18	MEM A CS L<0>	26	32 66
MODT0A_1	AP14	MEM A ODT<1>	26	32 66
MODT0A_0	AN17	MEM A ODT<0>	26	32 66
MCKE0A_1	AM27	MEM A CKE<1>	21	28 32 66
MCKE0A_0	AM26	MEM A CKE<0>	21	28 32 66

MDQS1_7_P	AN2	MEM B DOS P<7>	29	66
MDQS1_7_N	AN3	MEM B DOS N<7>	29	66
MDQS1_6_P	AY5	MEM B DOS P<6>	29	66
MDQS1_6_N	AY4	MEM B DOS N<6>	29	66
MDQS1_5_P	AV11	MEM B DOS P<5>	29	66
MDQS1_5_N	AW11	MEM B DOS N<5>	29	66
MDQS1_4_P	AV14	MEM B DOS P<4>	29	66
MDQS1_4_N	AW14	MEM B DOS N<4>	29	66
MDQS1_3_P	AW27	MEM B DOS P<3>	29	66
MDQS1_3_N	AY27	MEM B DOS N<3>	29	66
MDQS1_2_P	AV32	MEM B DOS P<2>	29	66
MDQS1_2_N	AW32	MEM B DOS N<2>	29	66
MDQS1_1_P	AY37	MEM B DOS P<1>	29	66
MDQS1_1_N	AV36	MEM B DOS N<1>	29	66
MDQS1_0_P	AN38	MEM B DOS P<0>	29	66
MDQS1_0_N	AN39	MEM B DOS N<0>	29	66
MRAS1*	AW18	MEM B RAS L	28	32 66
MCAS1*	AV17	MEM B CAS L	28	32 66
MWE1*	AY18	MEM B WE L	28	32 66
MBA1_2	AW24	MEM B BA<2>	28	32 66
MBA1_1	AT18	MEM B BA<1>	28	32 66
MBA1_0	AV18	MEM B BA<0>	28	32 66
MA1_15	AU24	MEM B A<15>	9	66
MA1_14	AV24	MEM B A<14>	28	32 66
MA1_13	AU17	MEM B A<13>	28	32 66
MA1_12	AY24	MEM B A<12>	28	32 66
MA1_11	AW23	MEM B A<11>	28	32 66
MA1_10	AU18	MEM B A<10>	28	32 66
MA1_9	AY23	MEM B A<9>	28	32 66
MA1_8	AU23	MEM B A<8>	28	32 66
MA1_7	AV23	MEM B A<7>	28	32 66
MA1_6	AT21	MEM B A<6>	28	32 66
MA1_5	AT23	MEM B A<5>	28	32 66
MA1_4	AU21	MEM B A<4>	28	32 66
MA1_3	AV21	MEM B A<3>	28	32 66
MA1_2	AY21	MEM B A<2>	28	32 66
MA1_1	AW21	MEM B A<1>	28	32 66
MA1_0	AY20	MEM B A<0>	28	32 66
MRES0*	AM6	MEM RESET L	26	27 28 29
MCLK1A_1_P	AV20	MEM B CLK P<1>	26	66
MCLK1A_1_N	AW20	MEM B CLK N<1>	26	66
MCLK1A_0_P	AT20	MEM B CLK P<0>	28	32 66
MCLK1A_0_N	AU20	MEM B CLK N<0>	28	32 66
MCS1A_1*	AT15	MEM B CS L<1>	28	32 66
MCS1A_0*	AY17	MEM B CS L<0>	28	32 66
MODT1A_1	AT17	MEM B ODT<1>	28	32 66
MODT1A_0	AW17	MEM B ODT<0>	28	32 66
MCKE1A_1	AT24	MEM B CKE<1>	21	28 32 66
MCKE1A_0	AT26	MEM B CKE<0>	21	28 32 66

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

MCP Memory Interface

Apple Inc.

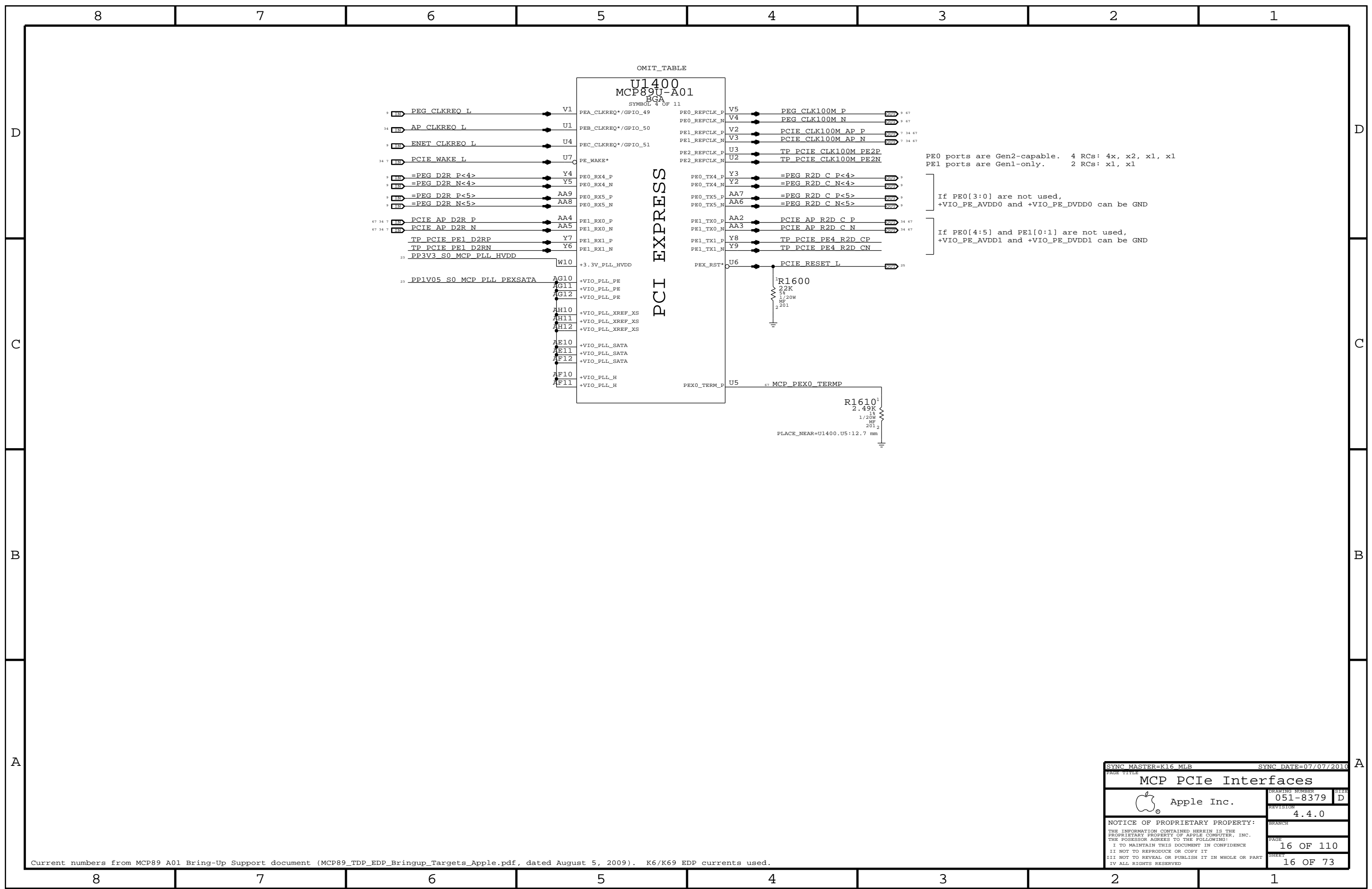
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Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
MCP PCIe Interfaces			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8379	D
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D

D

C

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B

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A

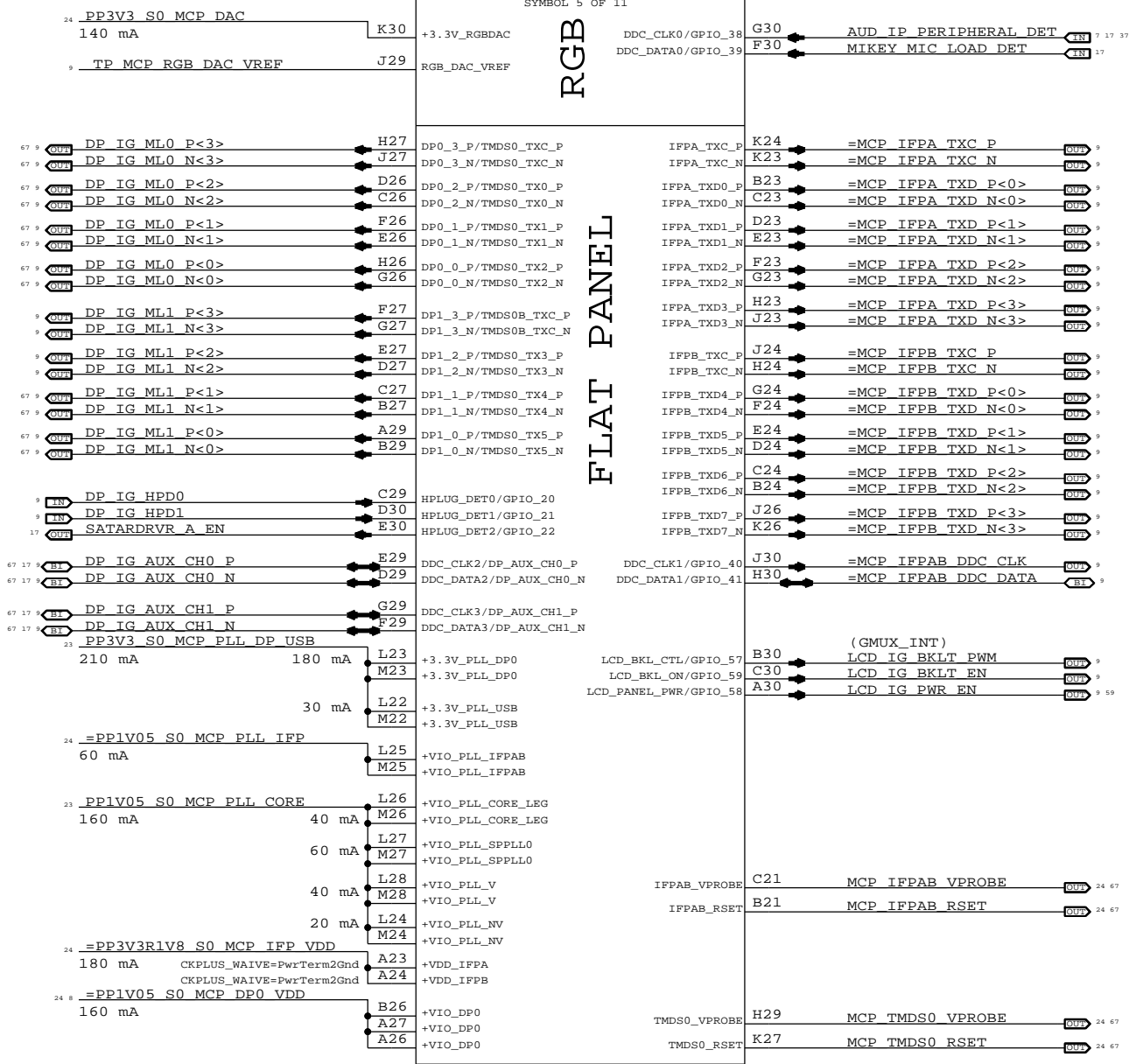
A

OMIT_TABLE

U1400
MCP890-A01
BGA
SYMBOL 5 OF 11

RGB

FLAT PANEL



RGB DAC Disable:
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
 Connect +3.3V_RGBDAC pin to GND.
 NOTE: No Composite/S-Video/Component Video support on MCP89

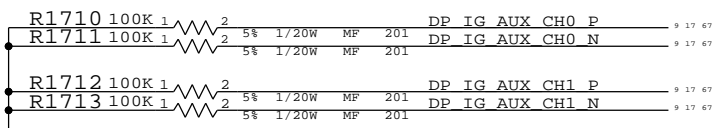
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
 TMDS: Power +VDD_IFPx at 3.3V

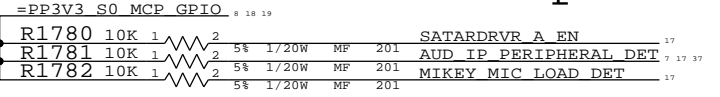
NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

DDC Mode Pull-downs

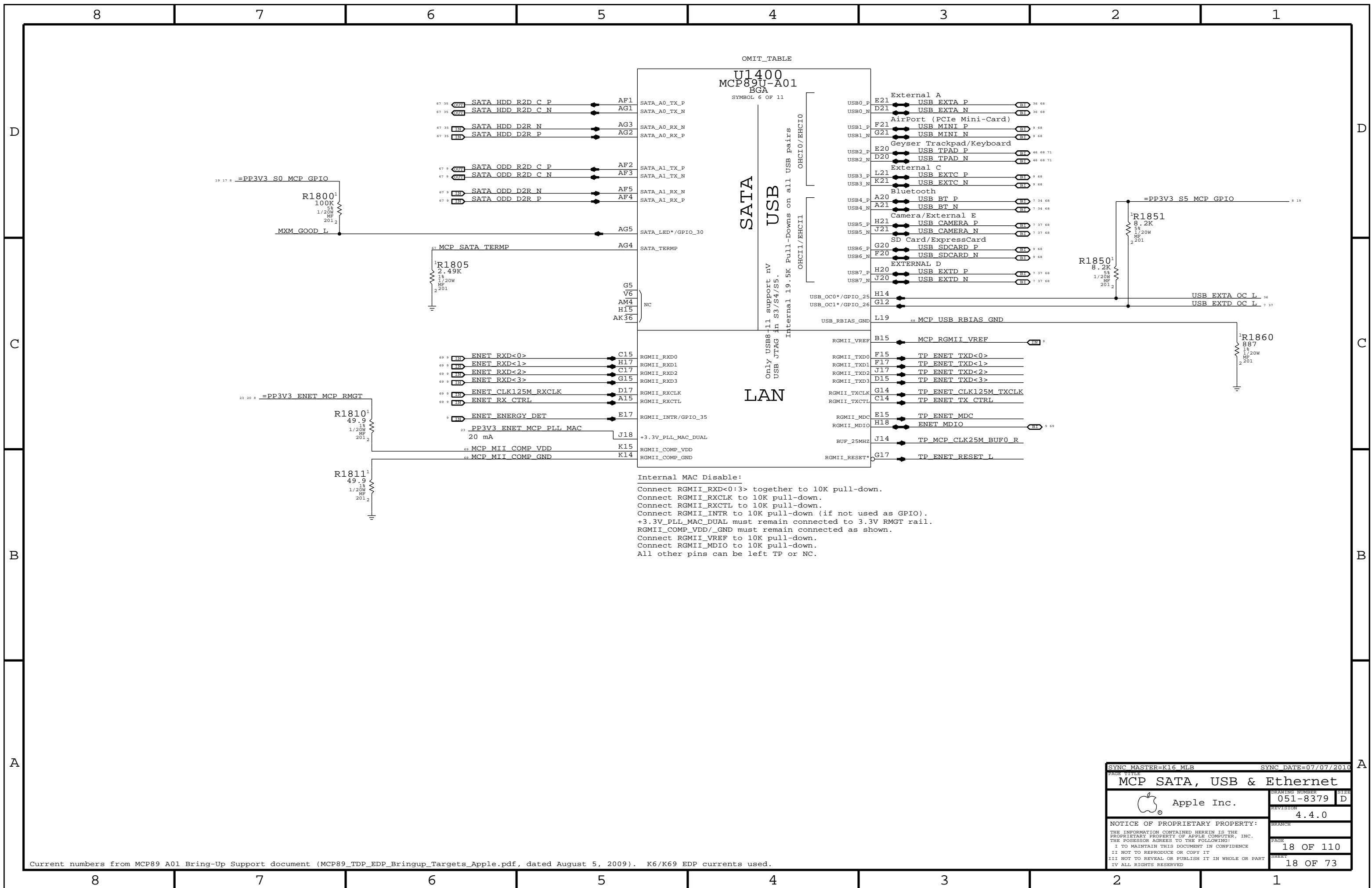
NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.



GPIO Pull-Ups



PAGE TITLE		SYNC DATE=07/07/2010	
MCP Graphics			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	4.4.0
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OMIT TABLE

U1400
MCP89U-A01
BGA
SYMBOL 6 OF 11

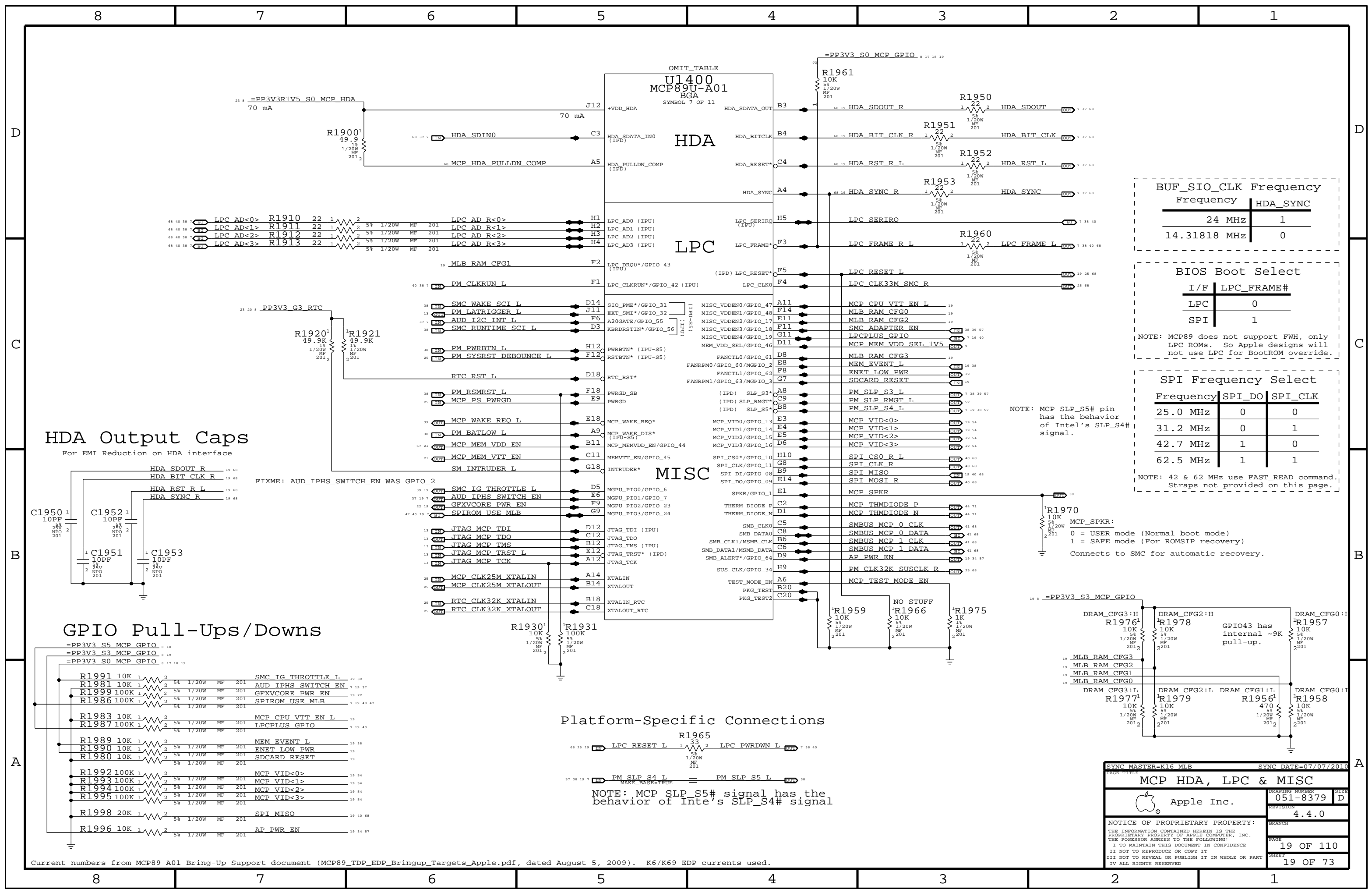
SATA
USB

LAN

Only USB8+11 support nv
USB JTAG in S3/S4/S5.
Internal 19.5K Pull-Downs on all USB pairs
OHCI0/EHCIO
OHCI1/EHC11

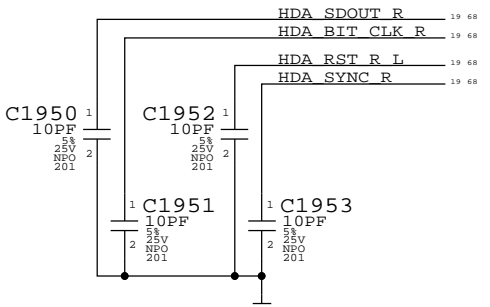
Internal MAC Disable:
Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE MCP SATA, USB & Ethernet			
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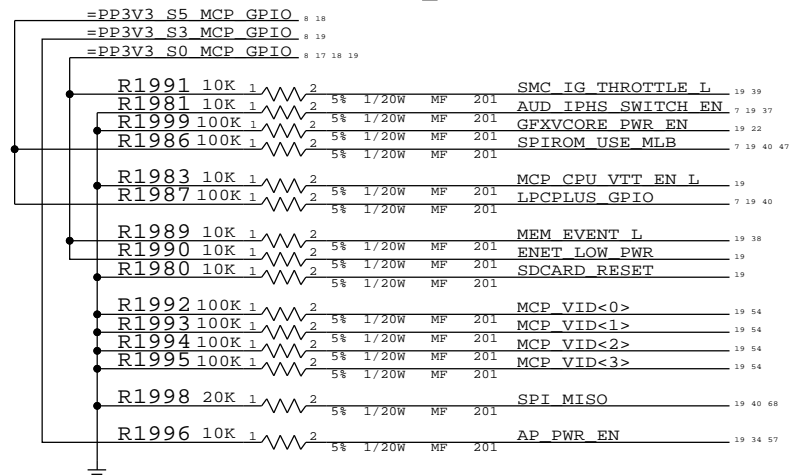


HDA Output Caps

For EMI Reduction on HDA interface

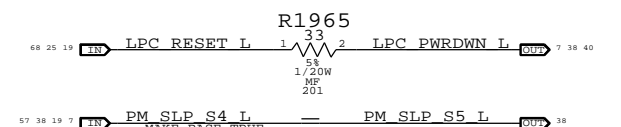


GPIO Pull-Ups/Downs



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Intel's SLP_S4# signal

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select	
I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

NOTE: MCP SLP_S5# pin has the behavior of Intel's SLP_S4# signal.

R1970 MCP_SPKR:
 0 = USER mode (Normal boot mode)
 1 = SAFE mode (For ROMSIP recovery)
 Connects to SMC for automatic recovery.

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

MCP HDA, LPC & MISC

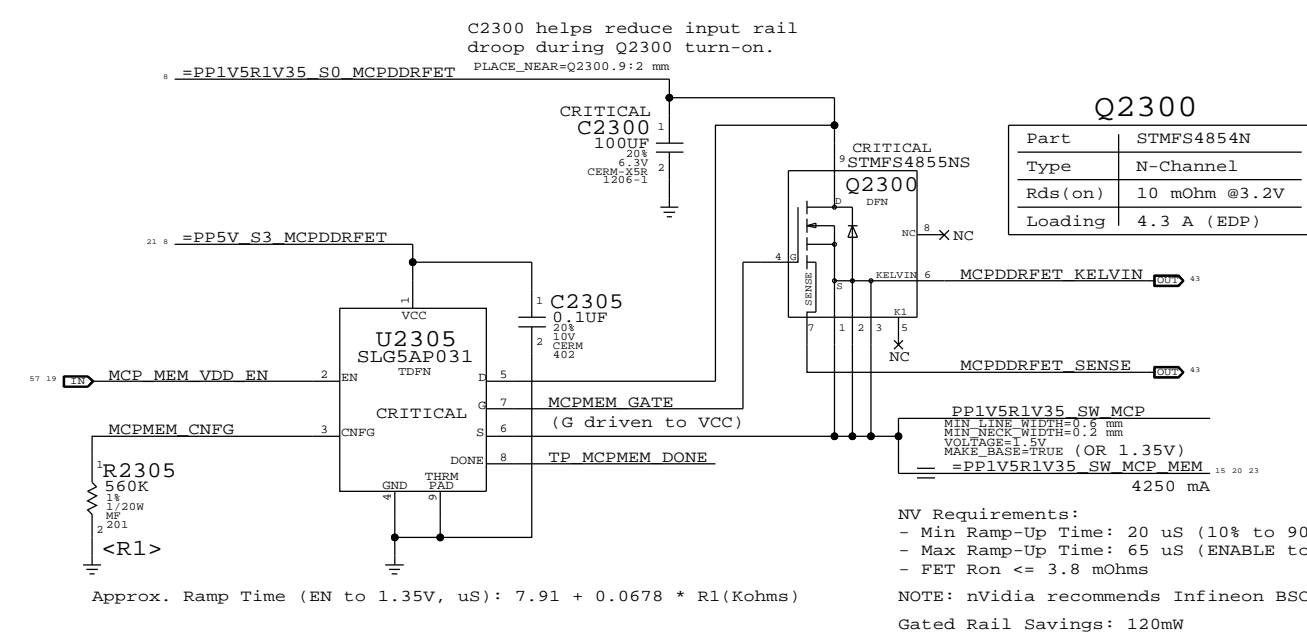
Apple Inc.

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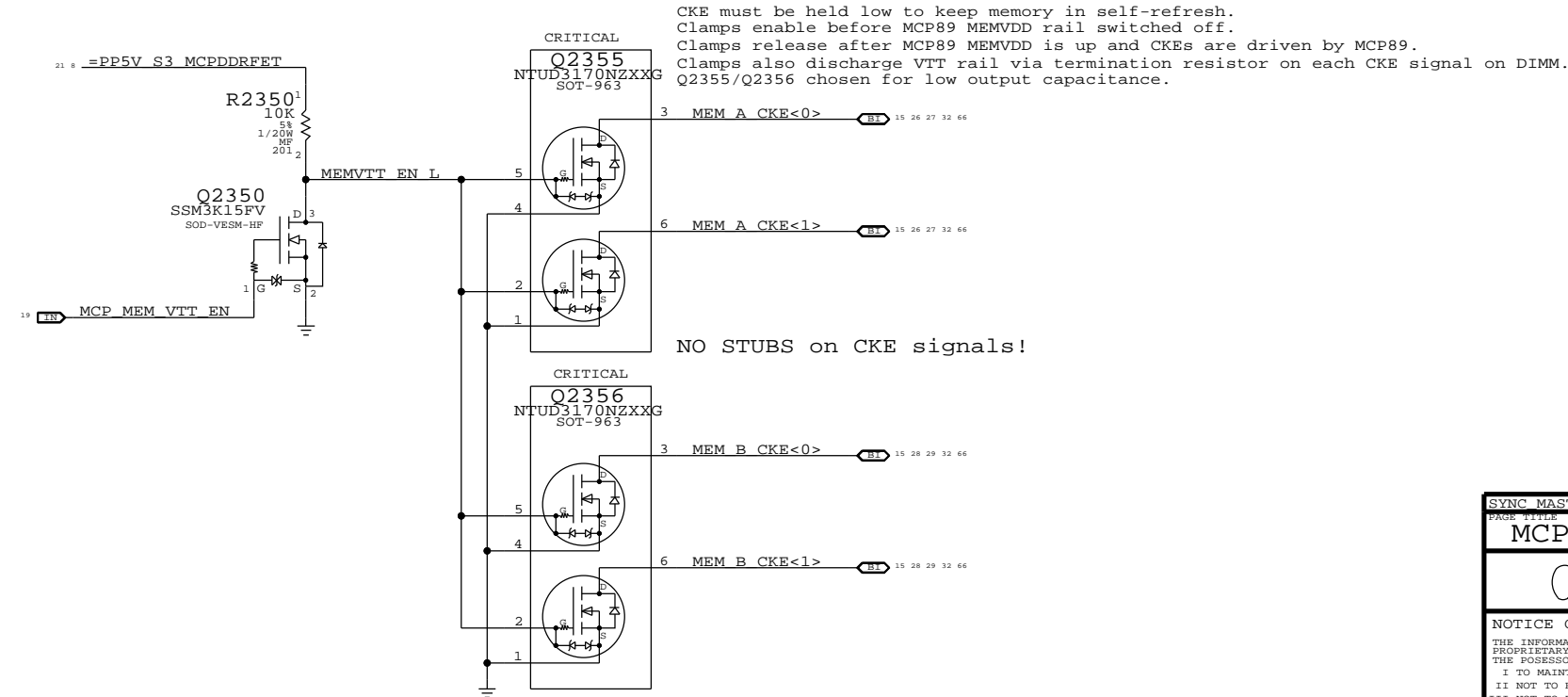
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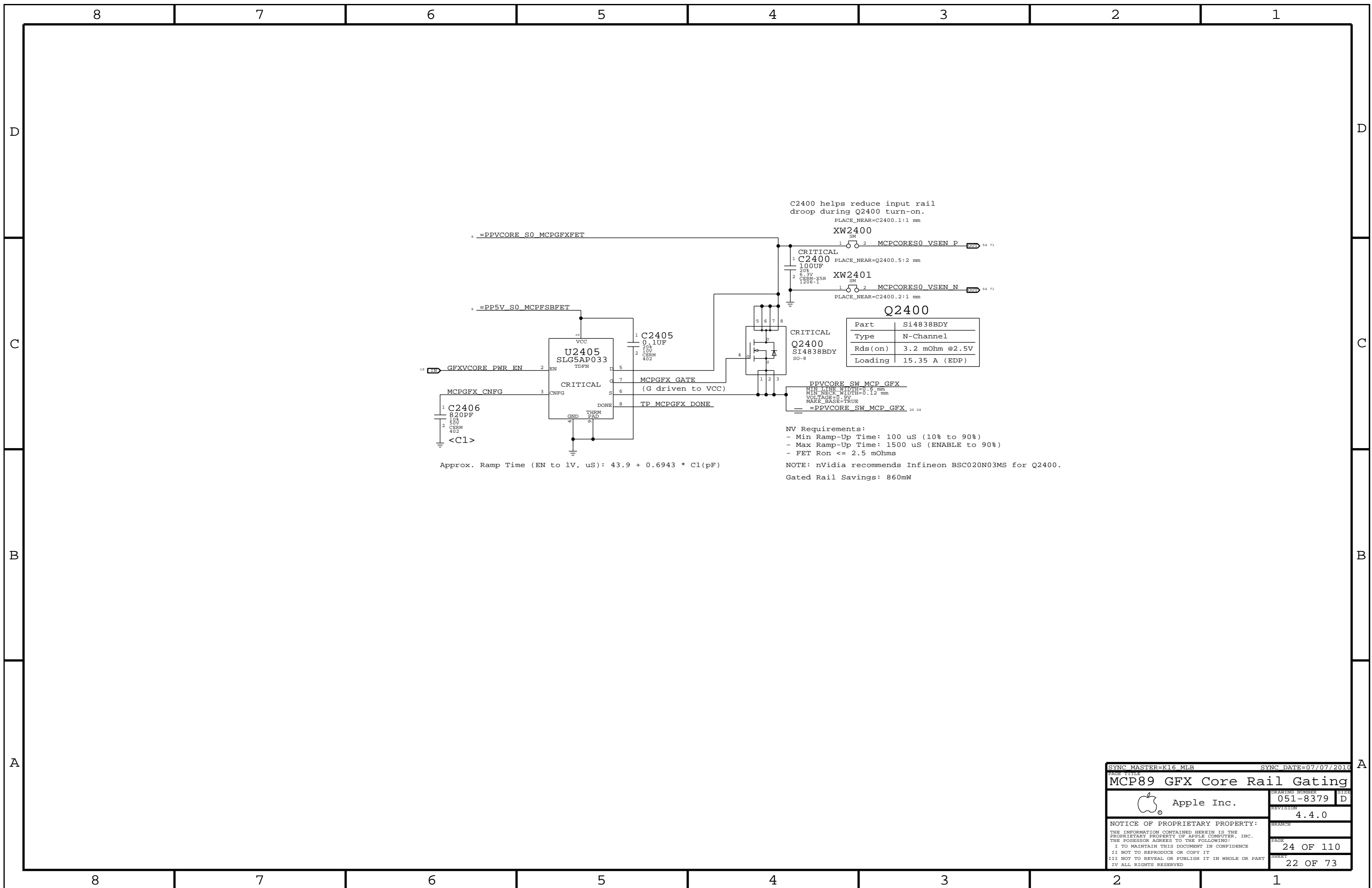
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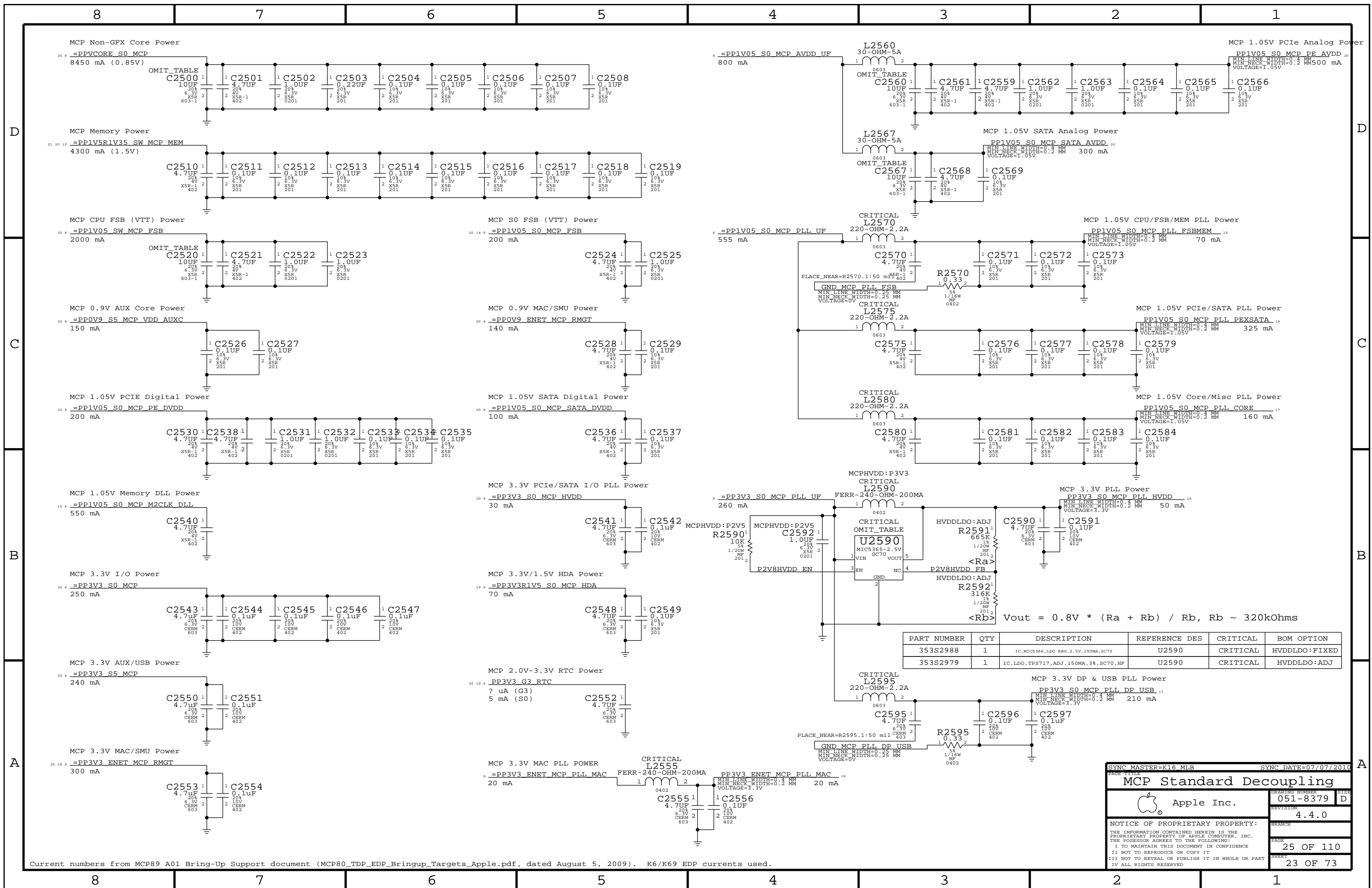
DIMM CKE Clamps



SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
MCP89 Memory Rail Gating			
Apple Inc.		DRAWING NUMBER	051-8379
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SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE MCP89 GFX Core Rail Gating			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC, MIC5366, LDO REG, 2.5V, 150mA, SC70	U2590	CRITICAL	HVDDLDO: FIXED
353S2979	1	IC, LDO, TPS717, ADJ, 150mA, 3%, SC70, HF	U2590	CRITICAL	HVDDLDO: ADJ

$$V_{out} = 0.8V * (R_a + R_b) / R_b, R_b \sim 320k\Omega$$

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

MCP Standard Decoupling

Apple Inc.

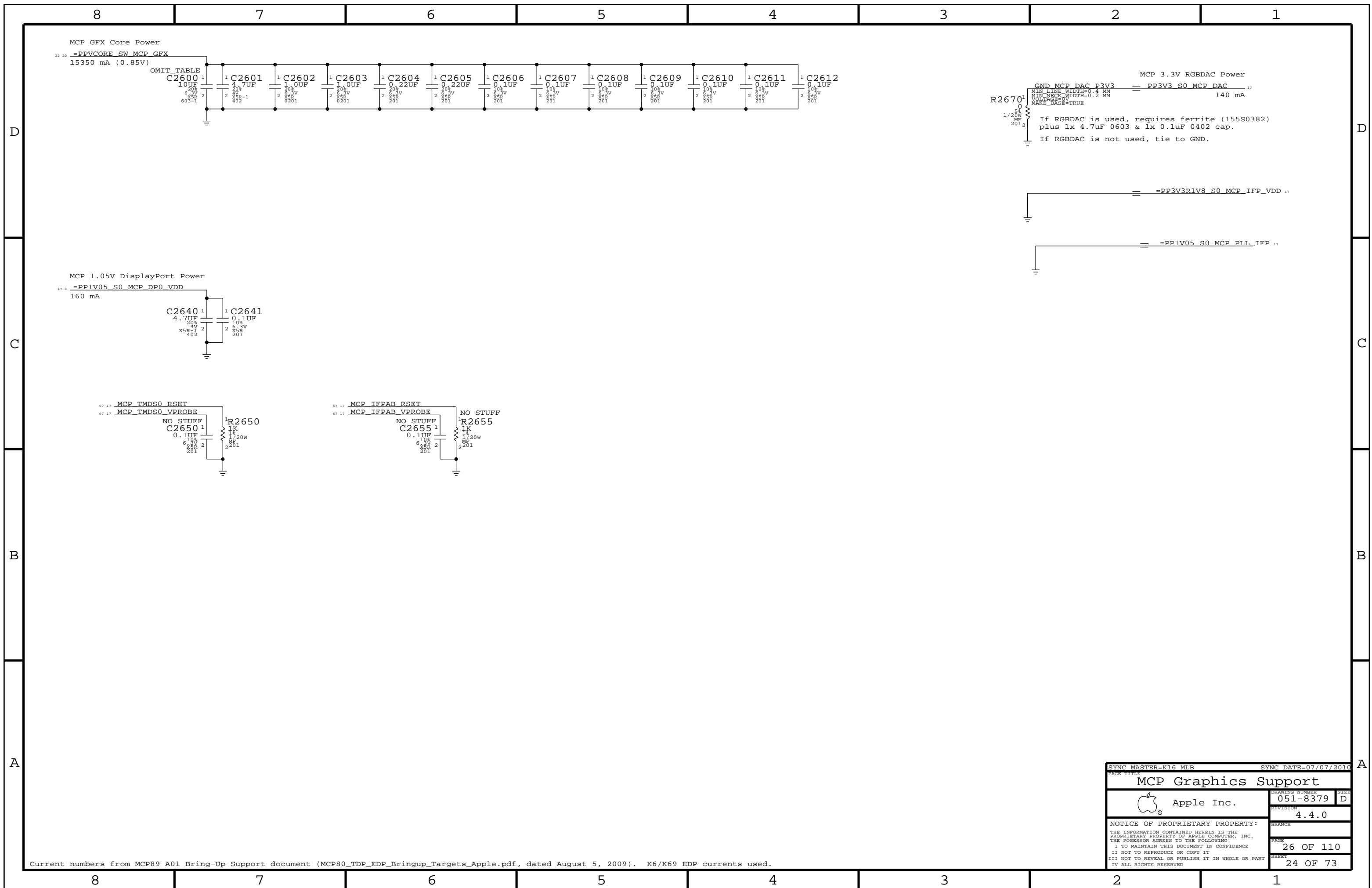
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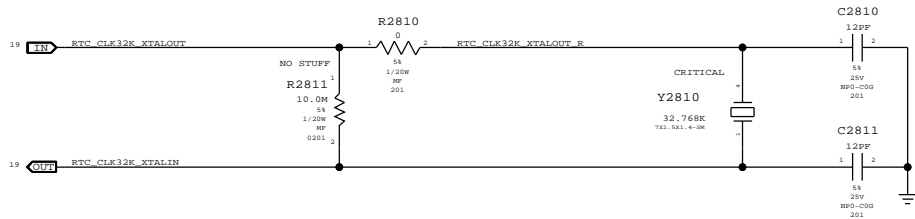
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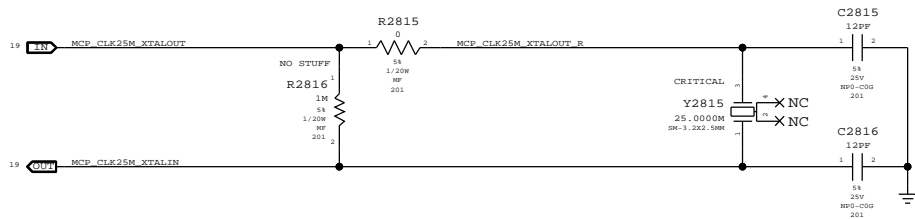
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PAGE TITLE MCP Graphics Support			
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RTC Crystal

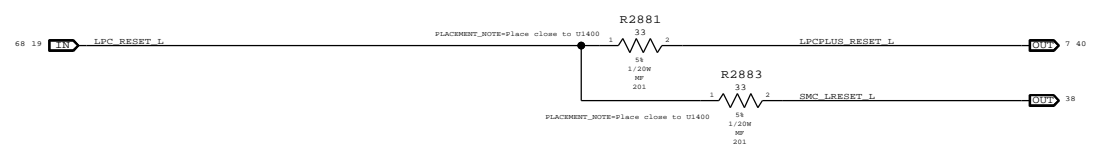


MCP 25MHz Crystal

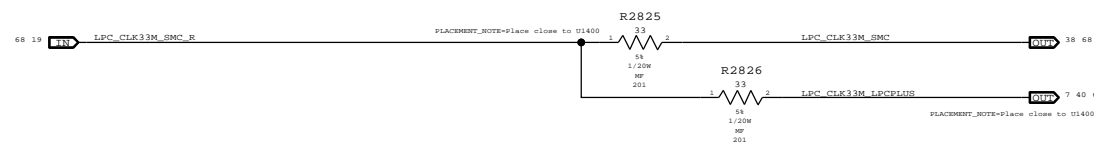
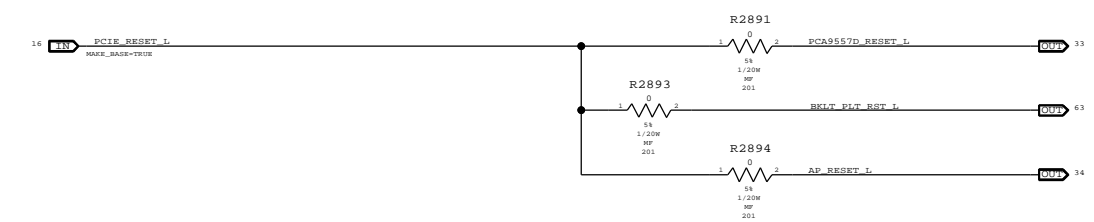


Platform Reset Connections

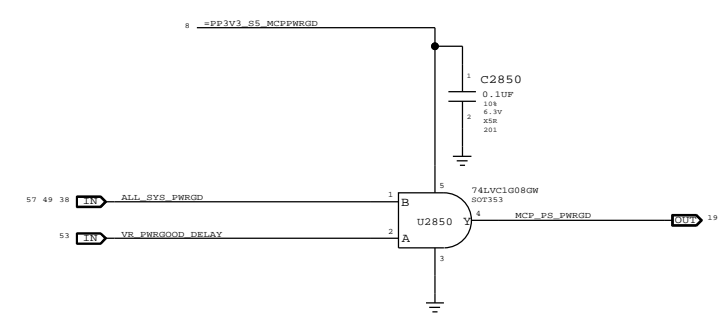
LPC Reset (Unbuffered)



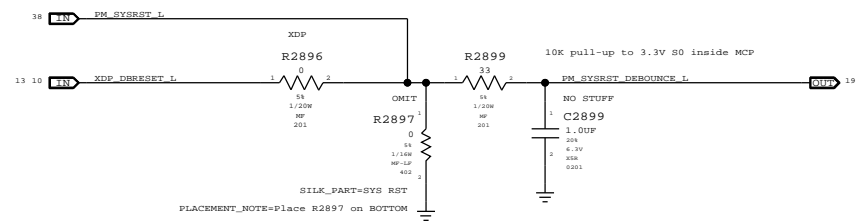
PCIE Reset (Unbuffered)



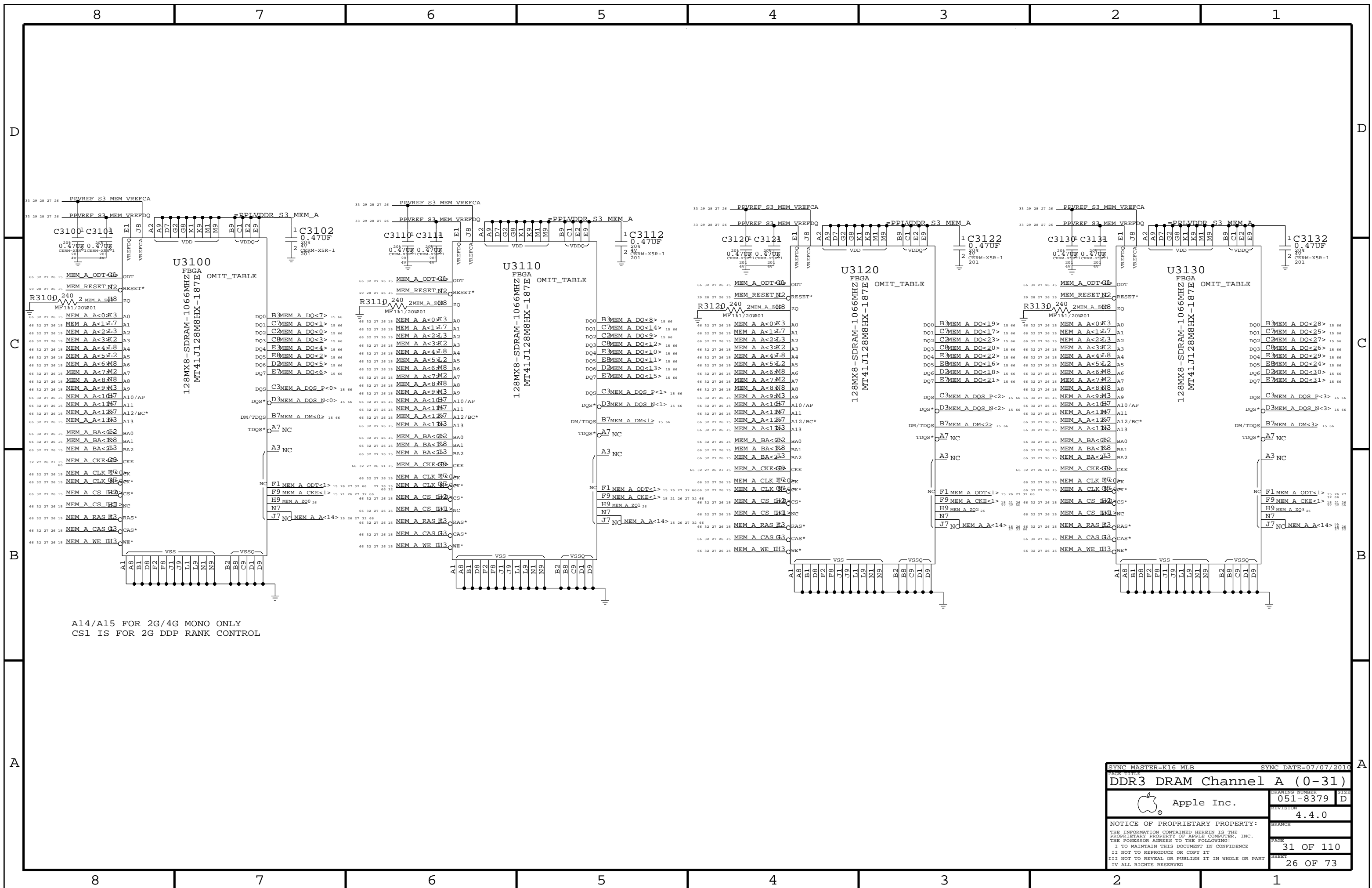
MCP S0 PWRGD & CPU_VLD



System Reset Circuit

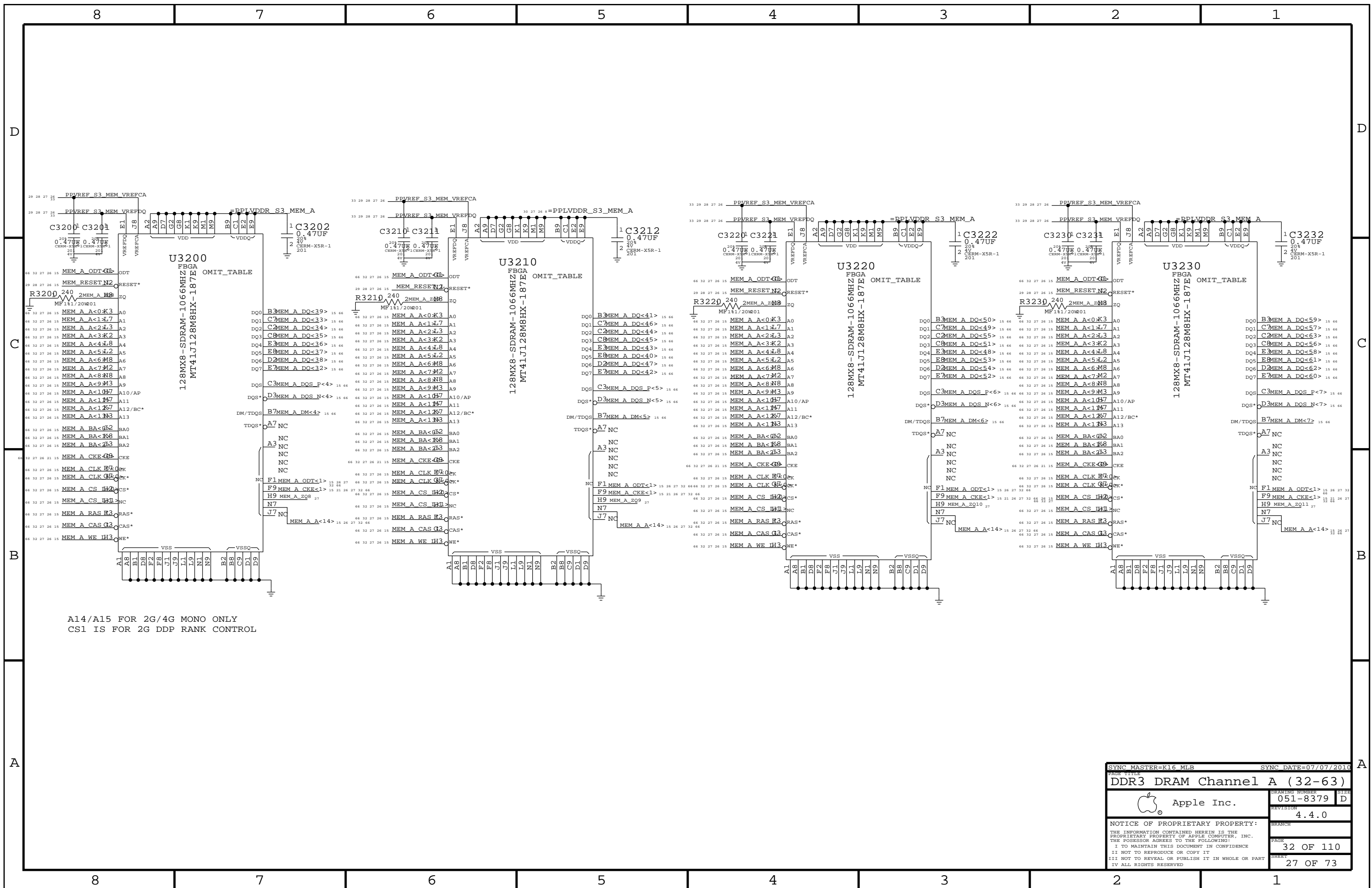


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SB Misc		DRAWING NUMBER	SIZE
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		PAGE	SHEET
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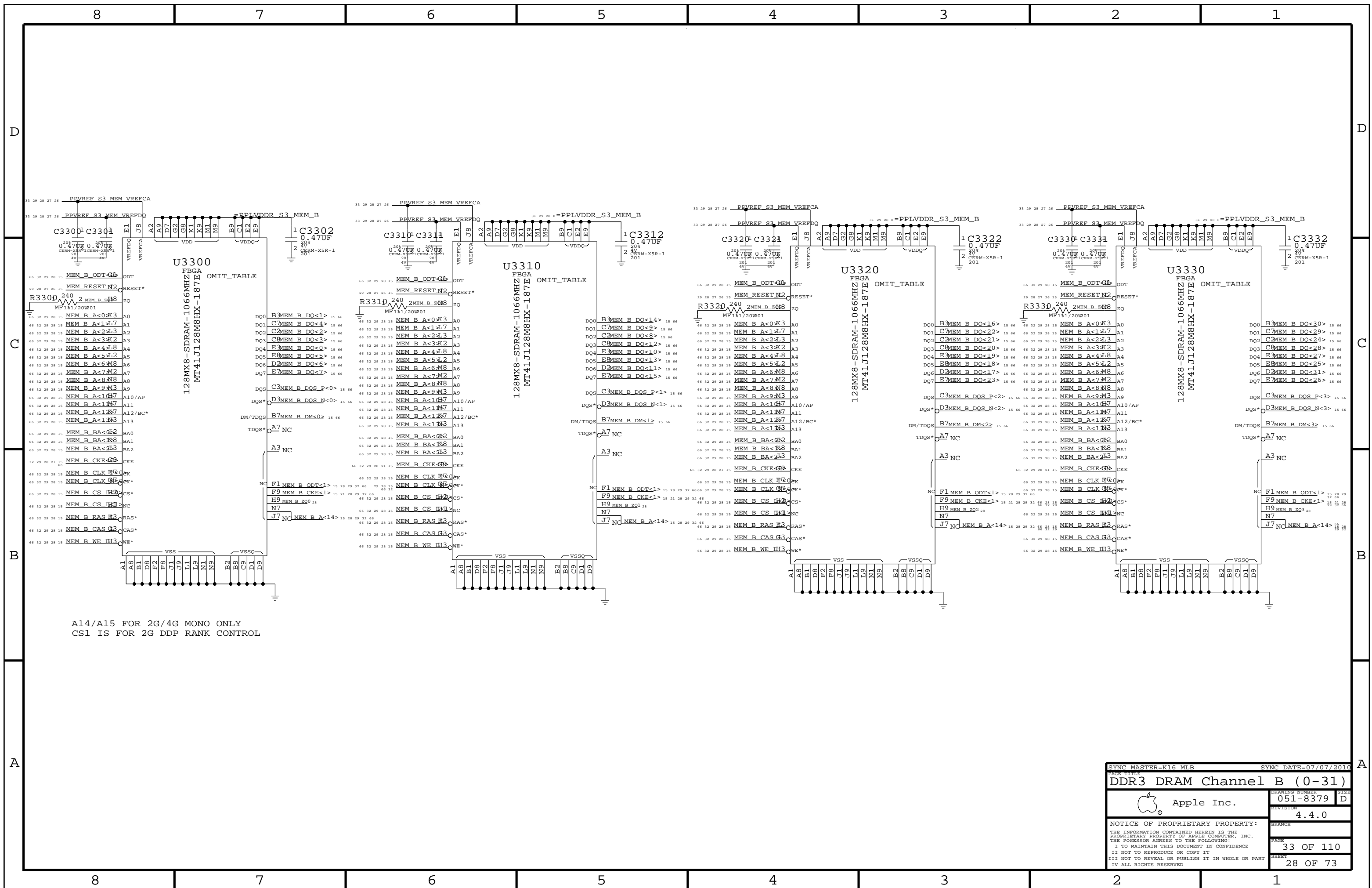
A14/A15 FOR 2G/4G MONO ONLY
 CS1 IS FOR 2G DDP RANK CONTROL

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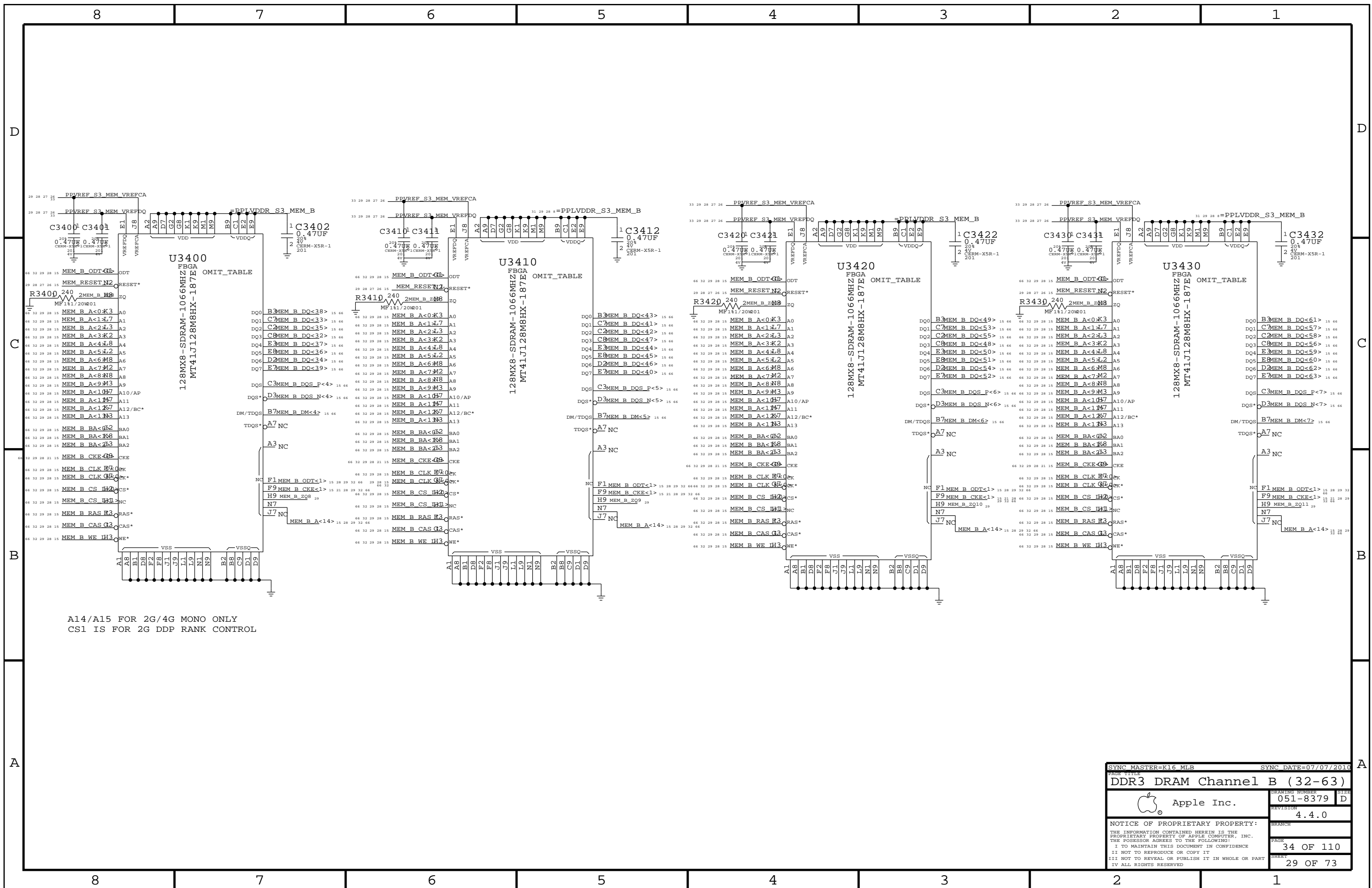
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 CS1 IS FOR 2G DDP RANK CONTROL

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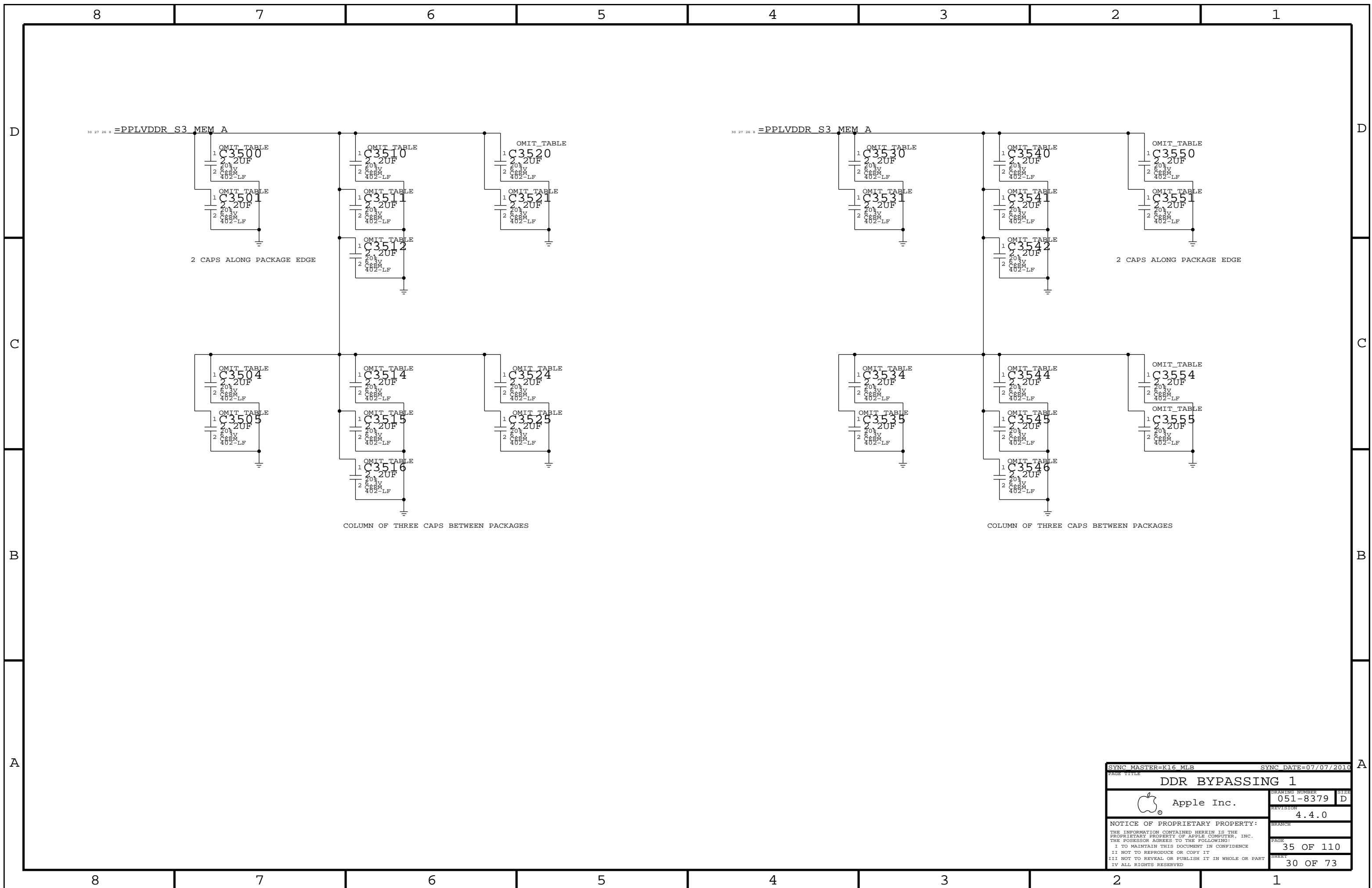
A14/A15 FOR 2G/4G MONO ONLY
 CS1 IS FOR 2G DDP RANK CONTROL


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PAGE 33 OF 110		SHEET 28 OF 73	

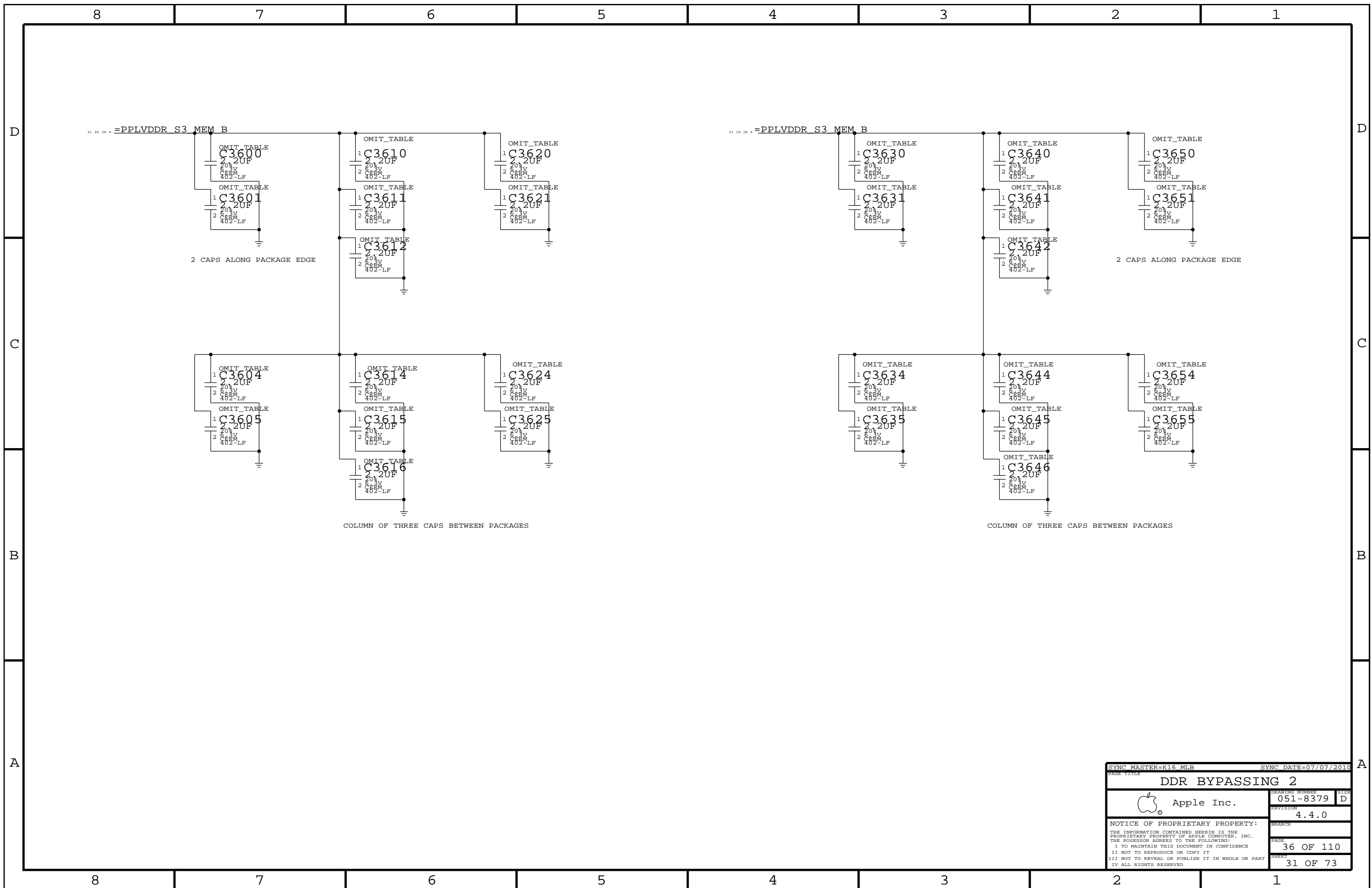



A14/A15 FOR 2G/4G MONO ONLY
 CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE DDR3 DRAM Channel B (32-63)			
Apple Inc.	DRAWING NUMBER	051-8379	SIZE D
	REVISION	4.4.0	
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		SHEET	29 OF 73



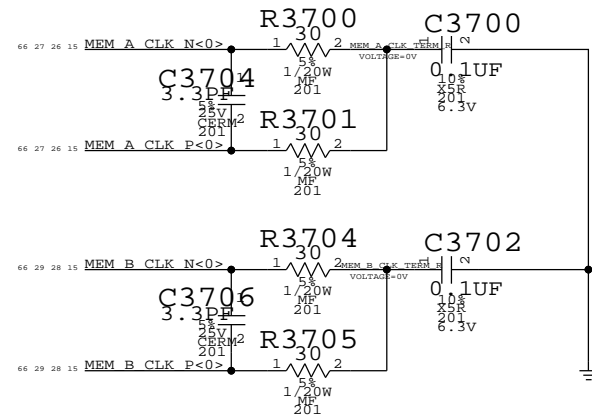
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DDR BYPASSING 1			
 Apple Inc.		DRAWING NUMBER	051-8379
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		PAGE	35 OF 110
		SHEET	30 OF 73



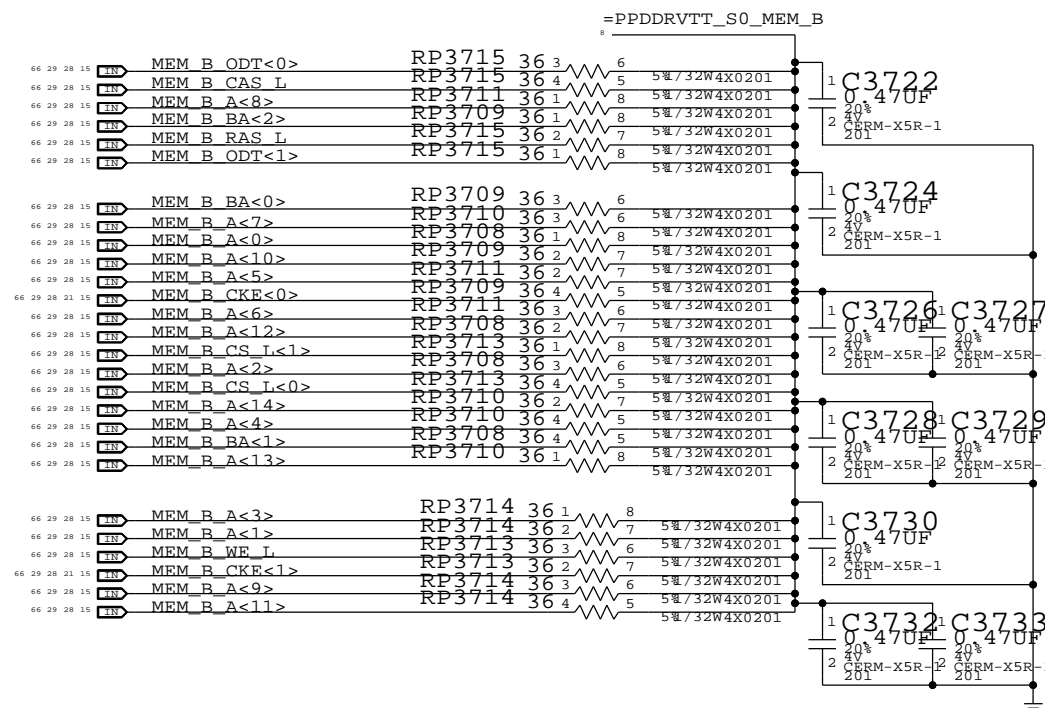
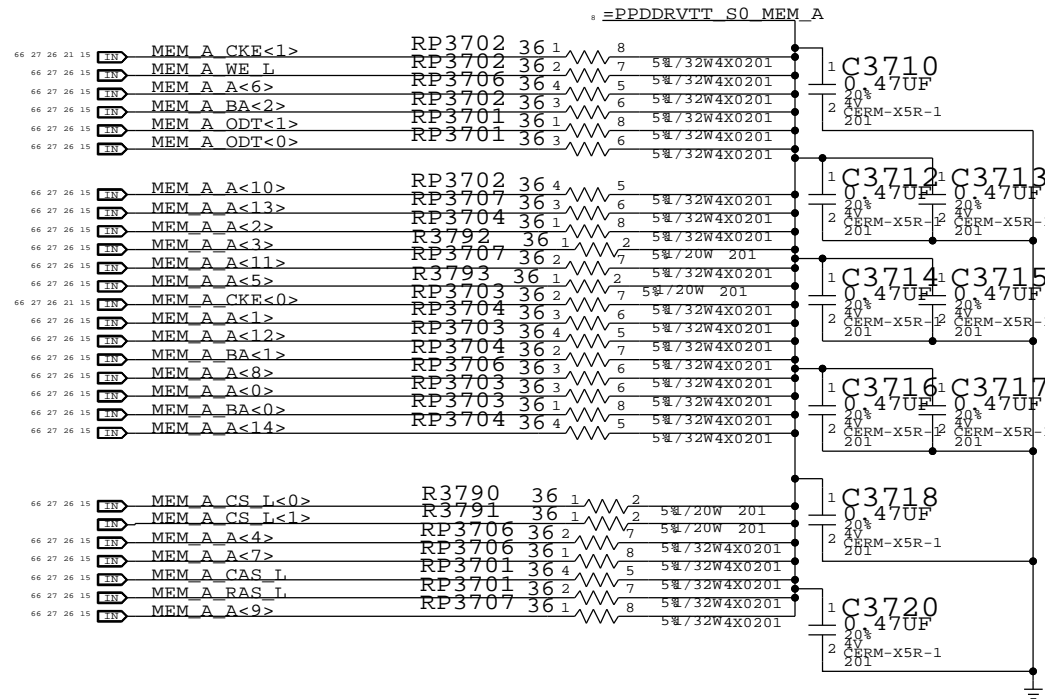
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 Apple Inc.		DRAWING NUMBER	051-8379
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		PAGE	36 OF 110
		SHEET	31 OF 73

MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

Memory Active Termination

Apple Inc.

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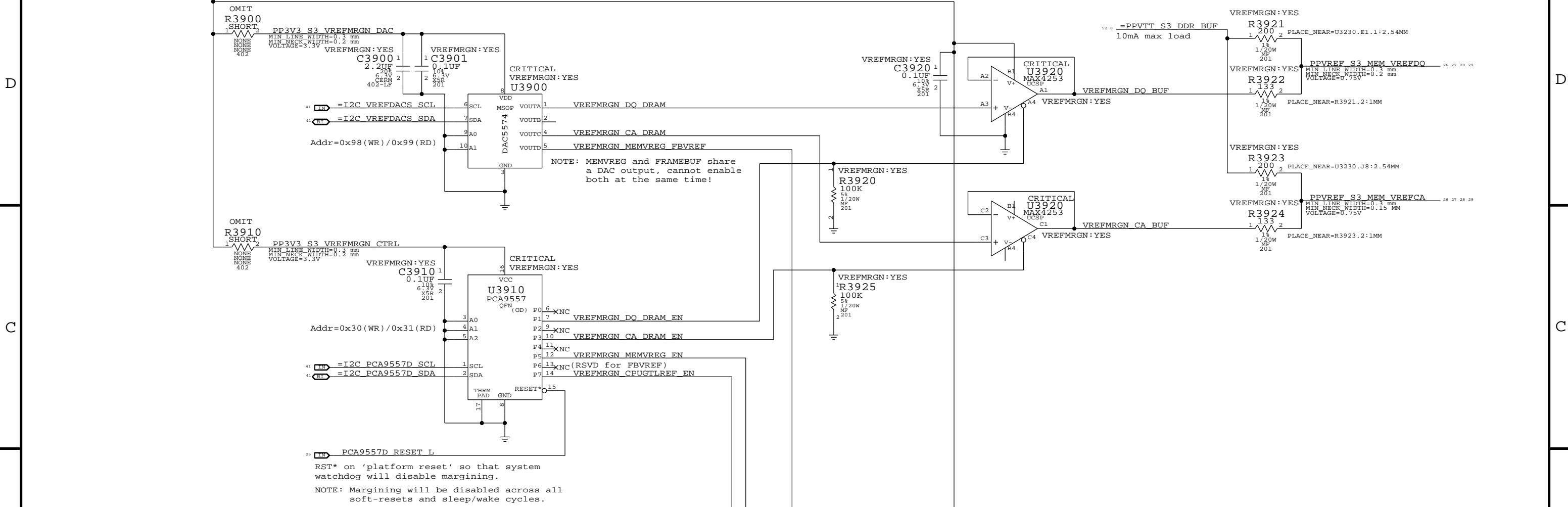
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



PCA9557D RESET L
RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES, MF, 1/20W, 0.0 OHM, 5, 0201, SMD	R3921, R3923		VREFMRGN:NO

Page Notes

- Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPVTT_S3_DDR_BUF
- Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA
- BOM options provided by this page:
 - VREFMRGN:YES - Stuffs VREF Margining Circuitry.
 - VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

FSB/DDR3 Vref Margining

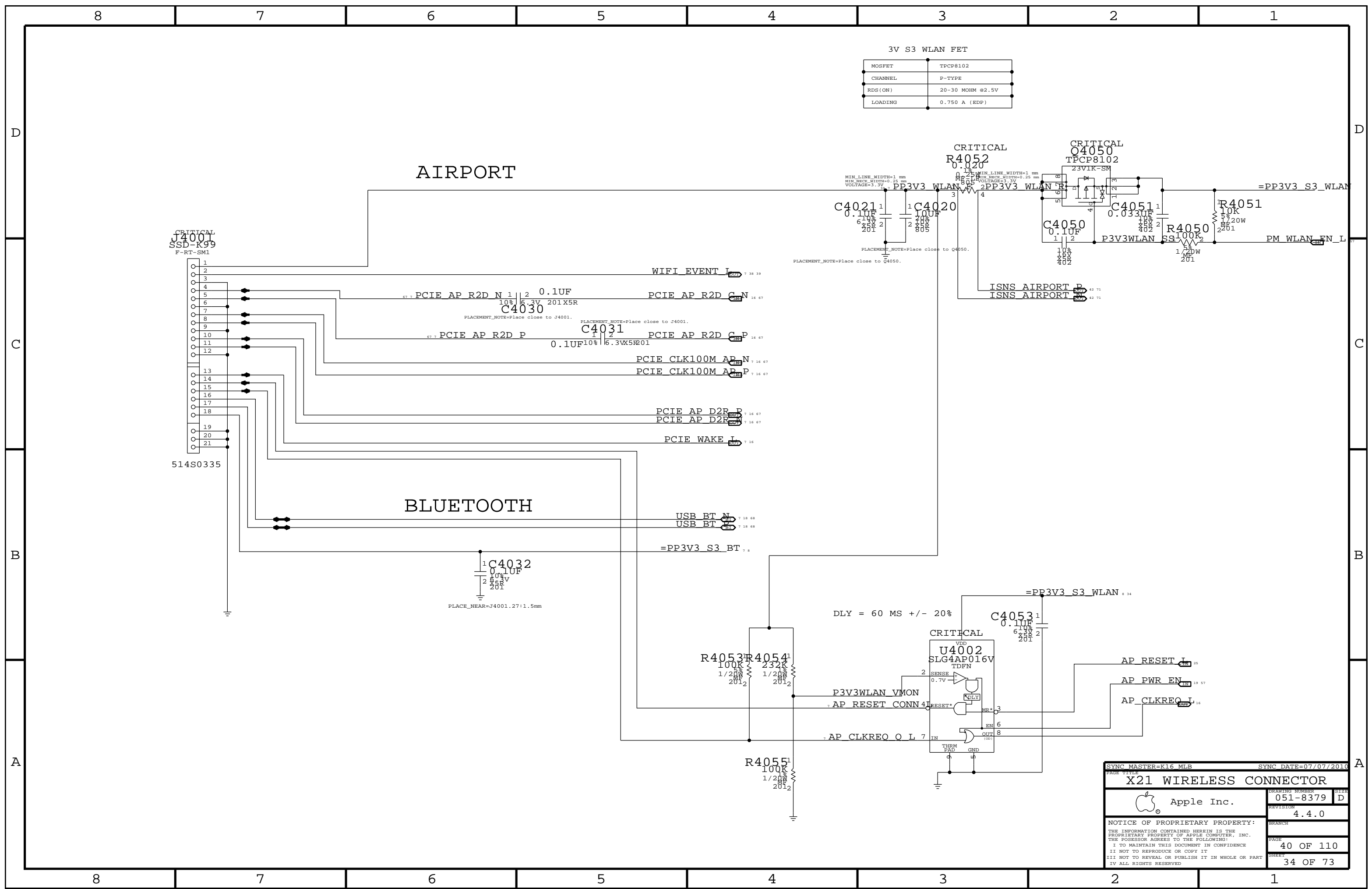
Apple Inc.


DRAWING NUMBER: 051-8379 SIZE: D

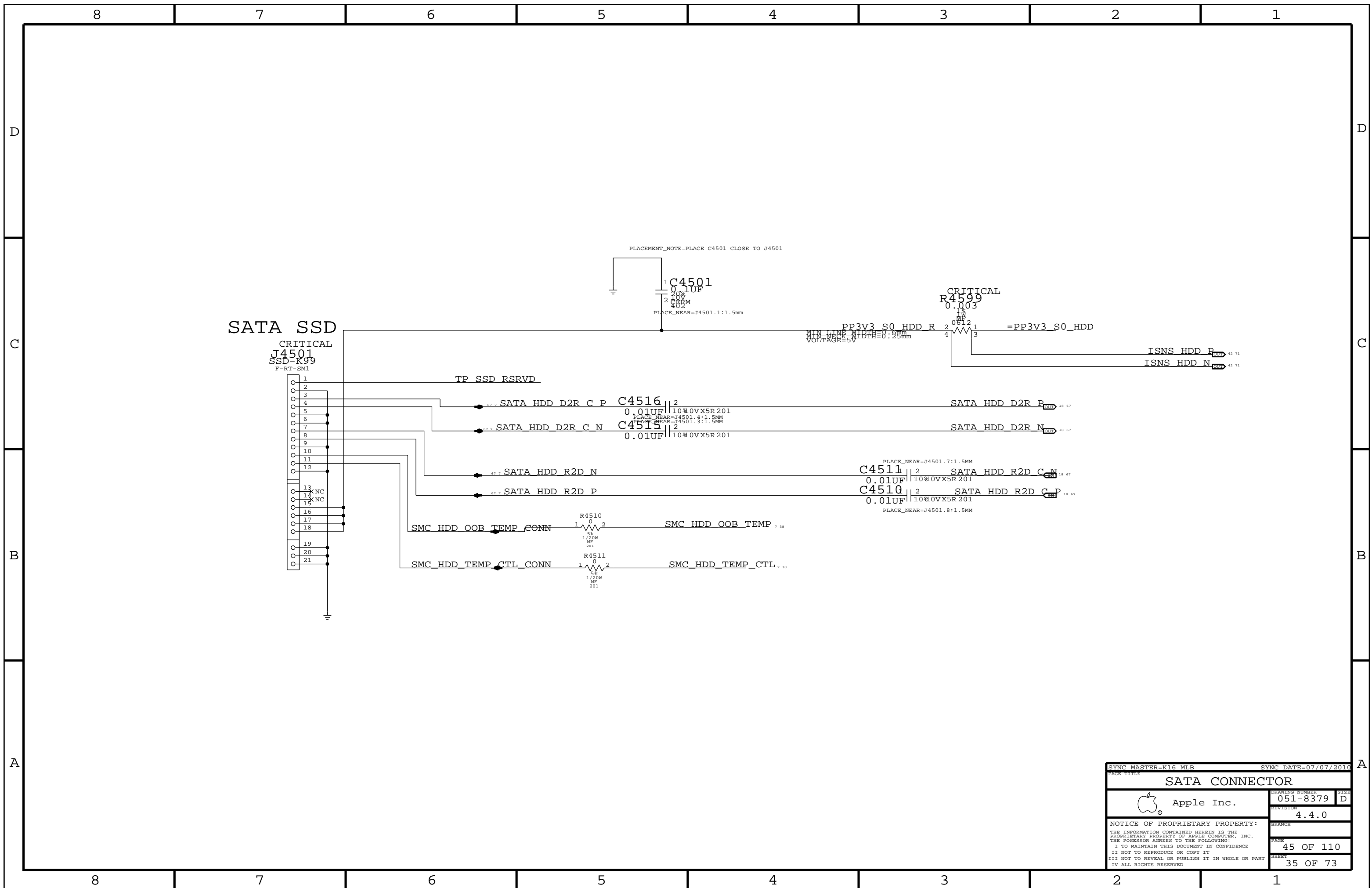
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PAGE: 39 OF 110 SHEET: 33 OF 73

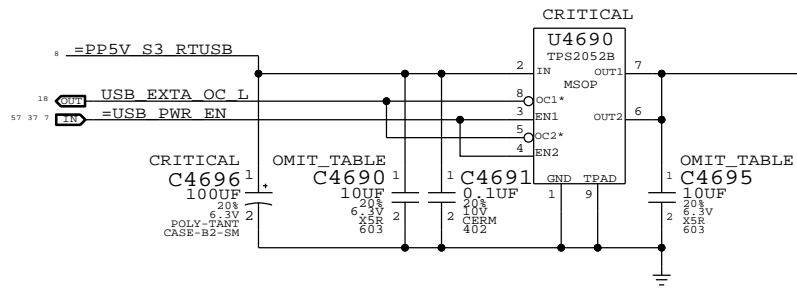


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
X21 WIRELESS CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8379
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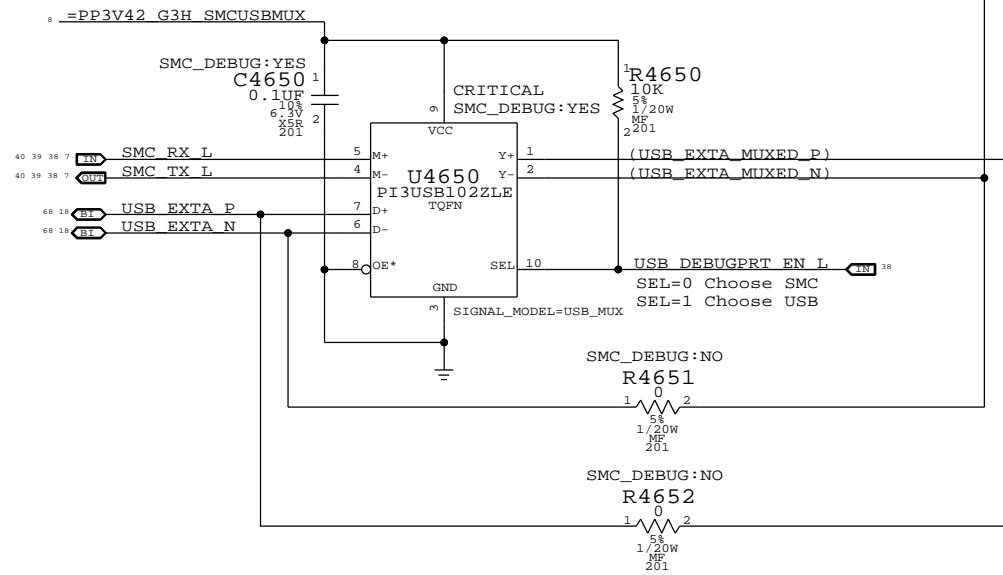


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
SATA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8379
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		PAGE	45 OF 110
		SHEET	35 OF 73
		SIZE	D

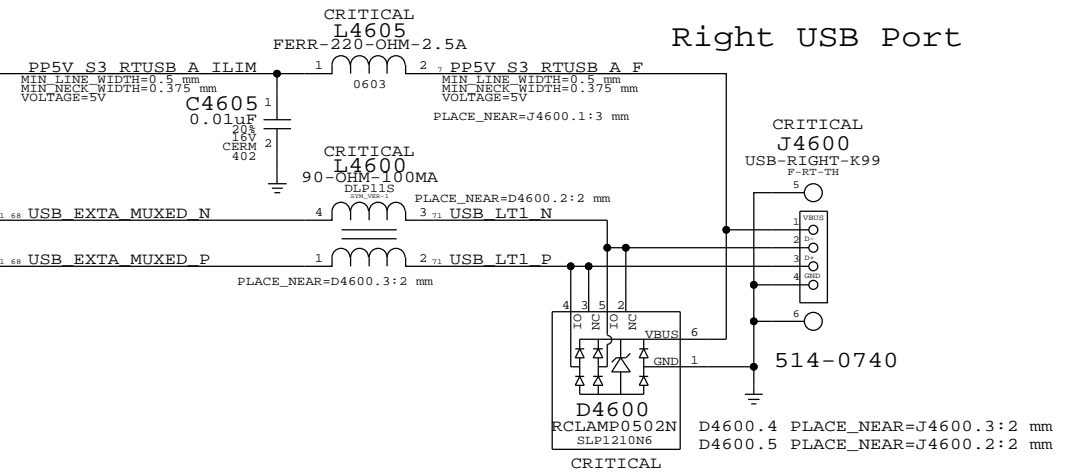
Port Power Switch



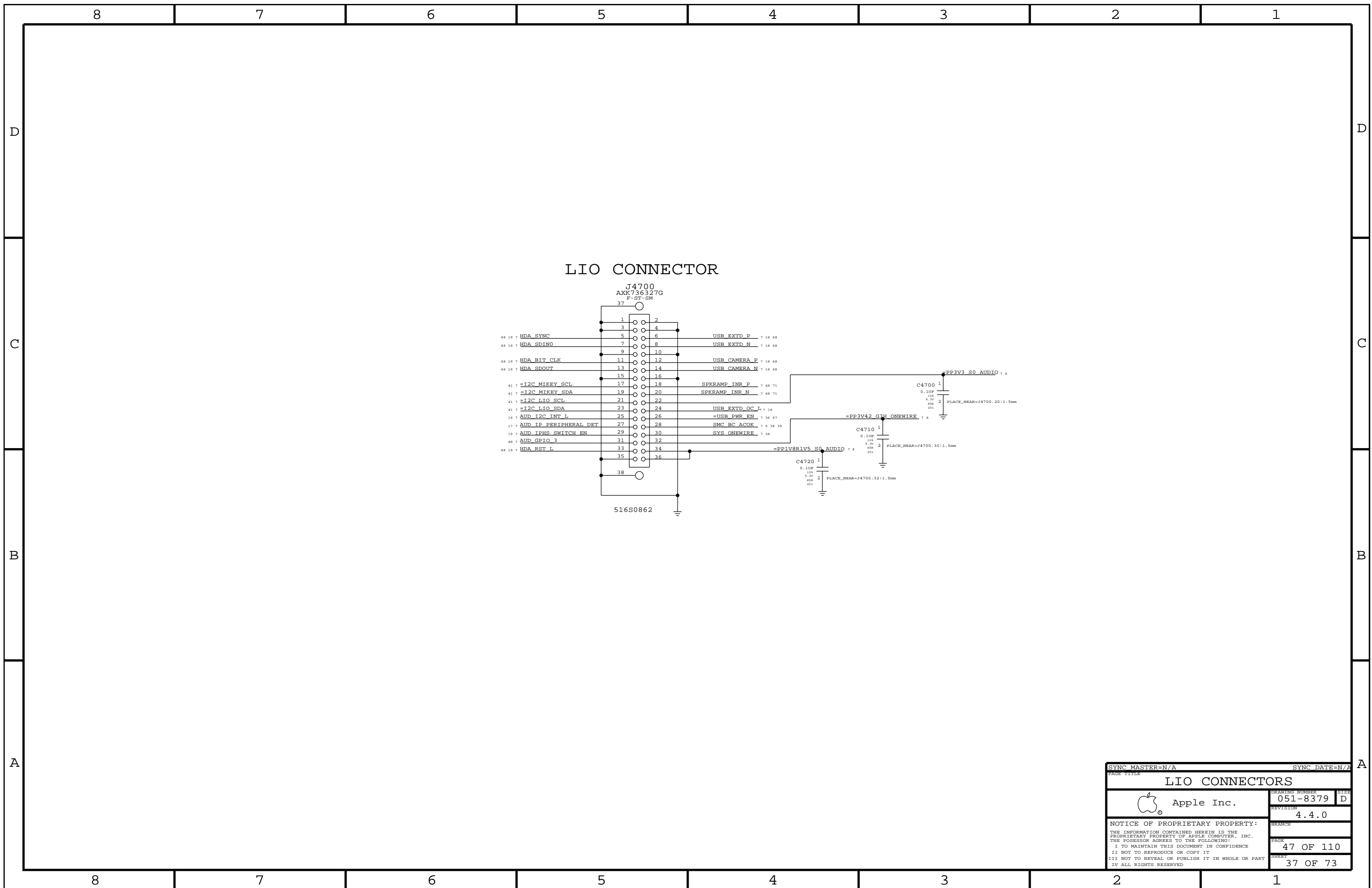
USB/SMC Debug Mux



Right USB Port

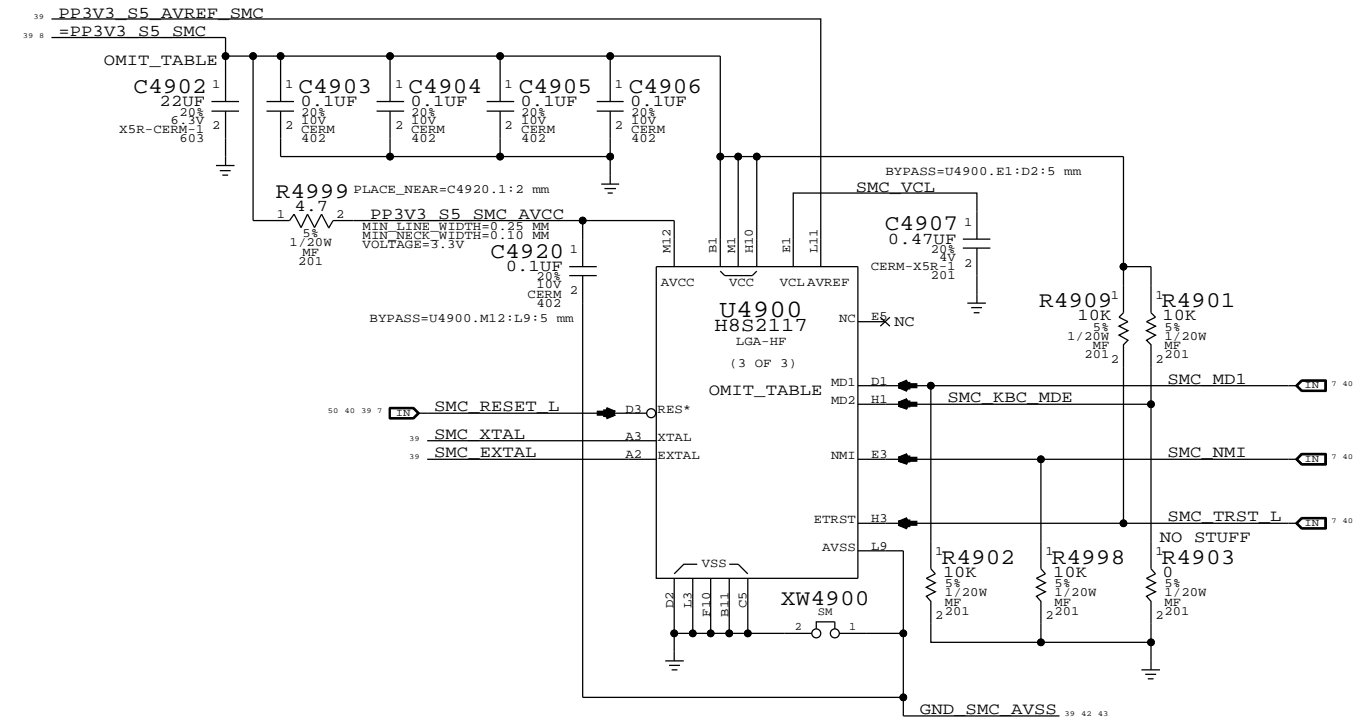
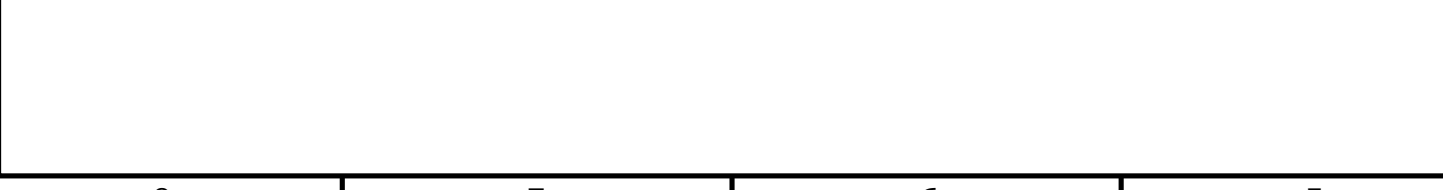
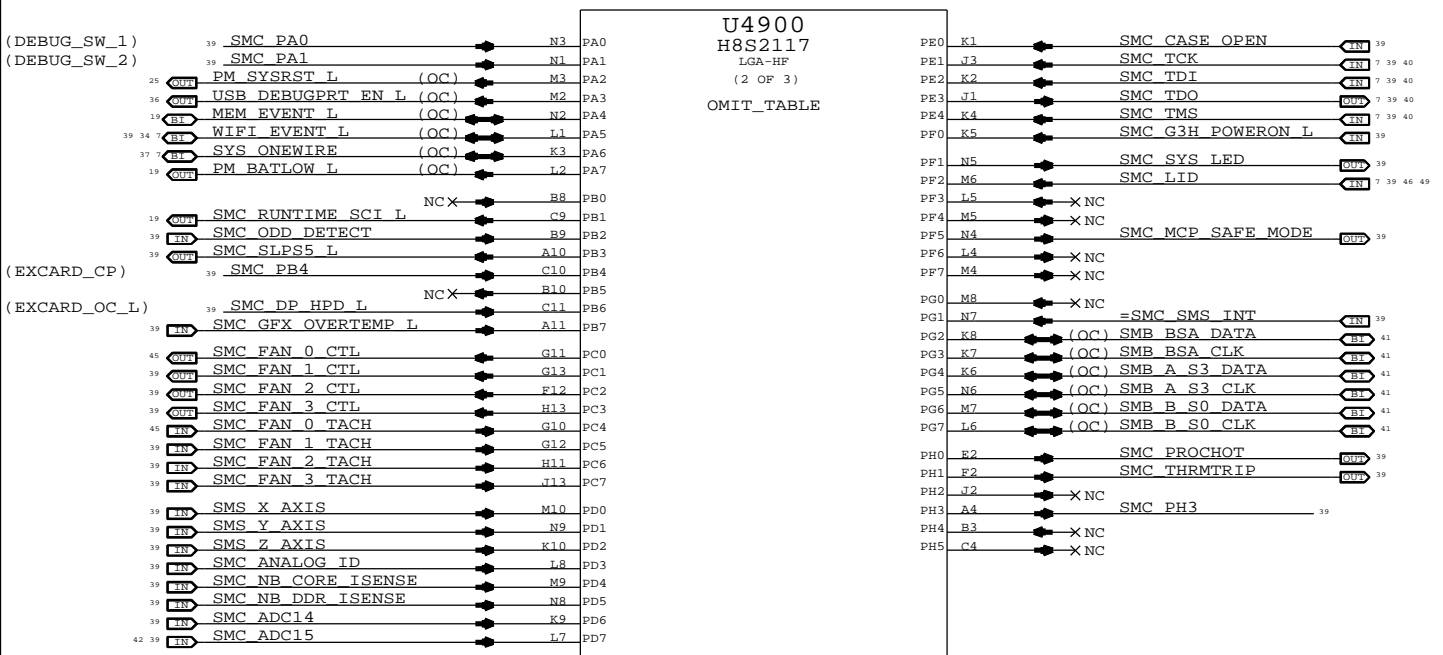
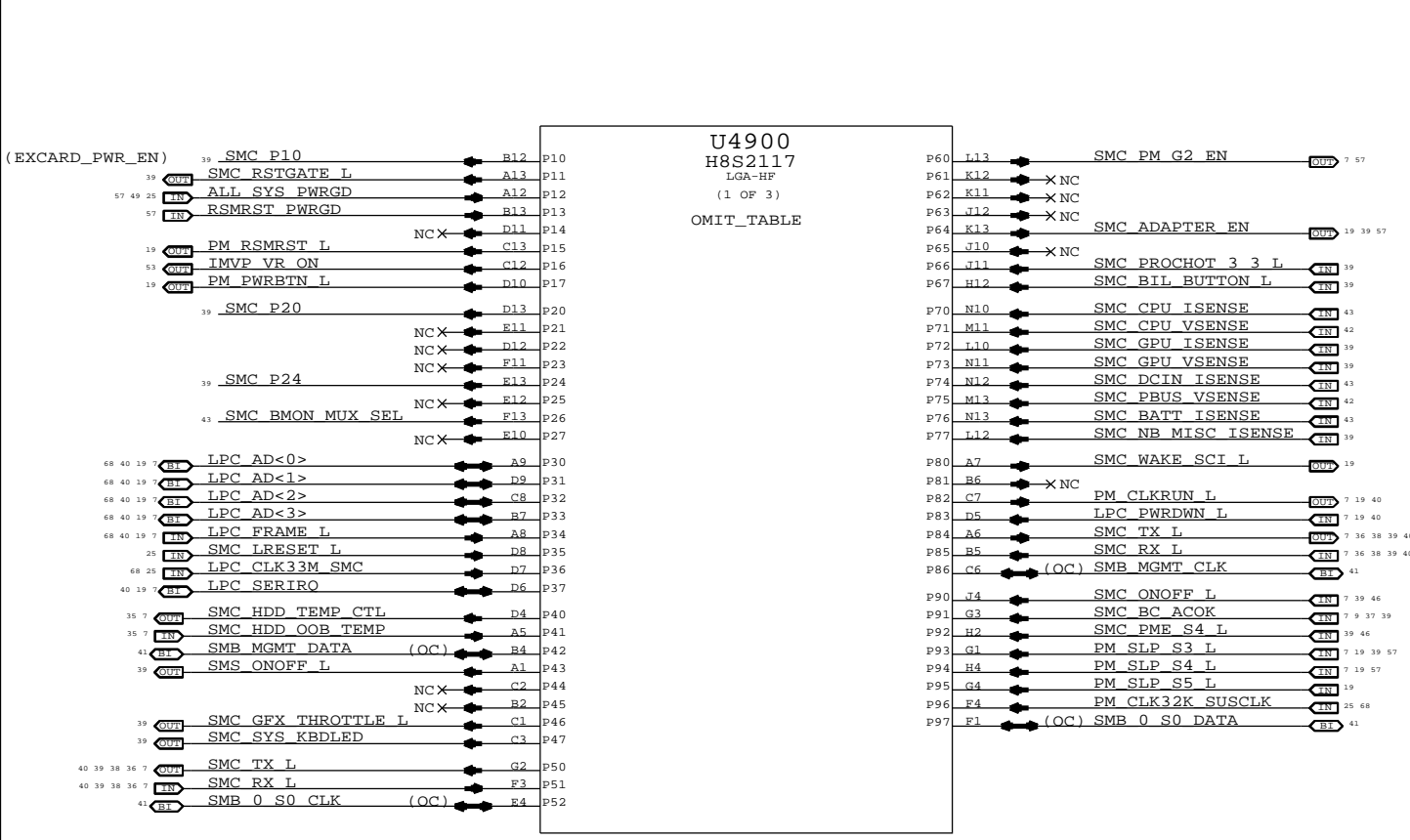


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
External USB Connectors			
Apple Inc.		DRAWING NUMBER	051-8379
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LIO CONNECTORS			
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		PAGE	47 OF 110
		SHEET	37 OF 73

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

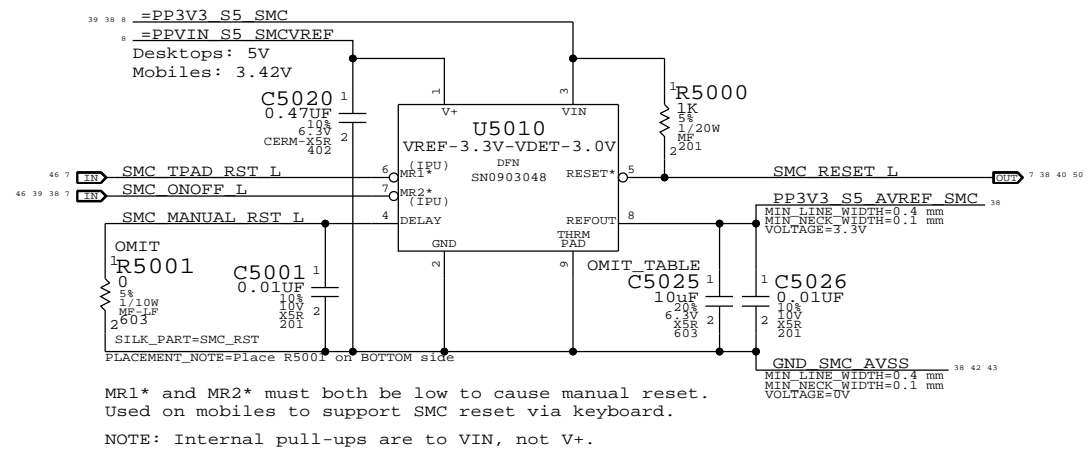


NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

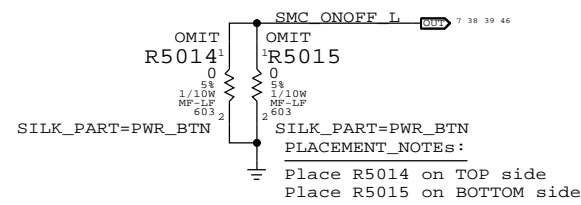
H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
051-8379		REVISION	D
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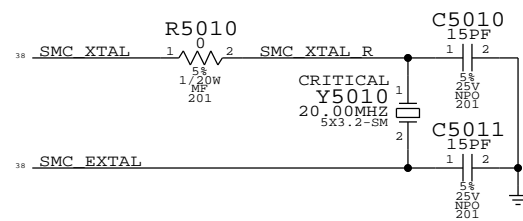
SMC Reset "Button", Supervisor & AVREF Supply



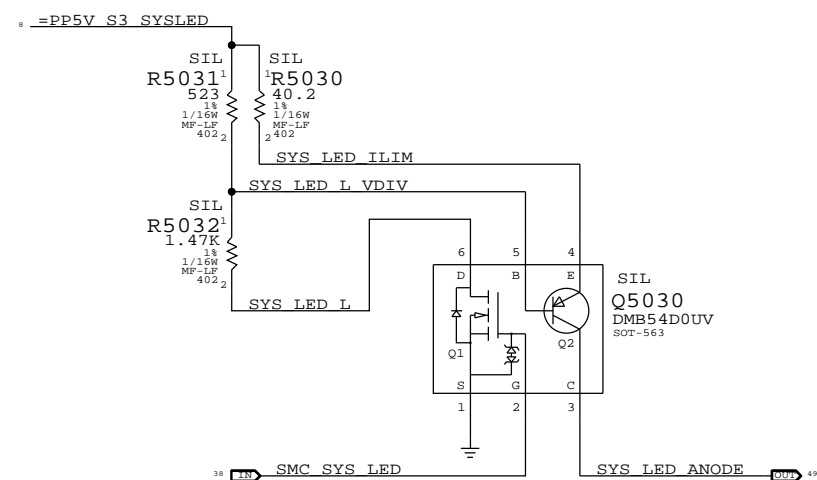
Debug Power "Buttons"



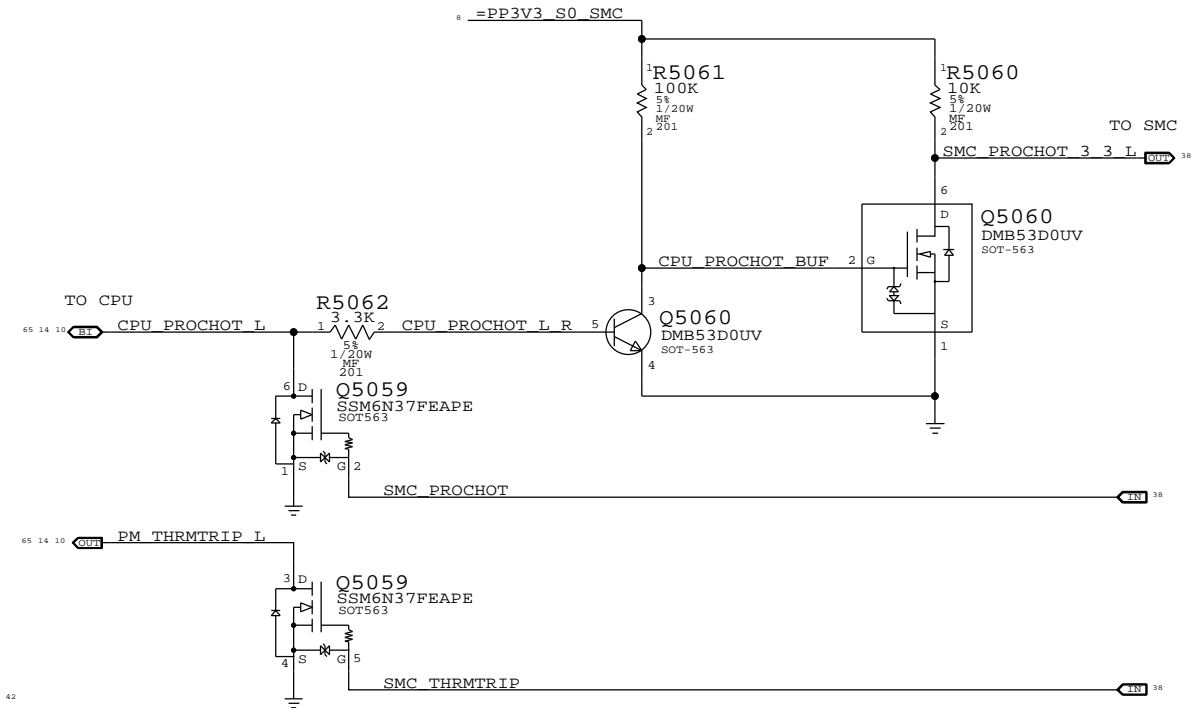
SMC Crystal Circuit



System (Sleep) LED Circuit



SMC FSB to 3.3V Level Shifting



SMC Aliases

SMC_LCDBKLT_ISENSE	=	SMS_X_AXIS
SMC_WLAN_ISENSE	=	SMS_Y_AXIS
SMC_HDD_ISENSE	=	SMS_Z_AXIS
SMC_CSREG_ISENSE	=	SMC_ADC14
SMC_LCDBKLT_VSENSE	=	SMC_ADC15
SMC_MCP_CORE_ISENSE	=	SMC_NB_CORE_ISENSE
SMC_MCP_DDR_ISENSE	=	SMC_NB_DDR_ISENSE
SMC_1V5S3_ISENSE	=	SMC_NB_MISC_ISENSE
TP_SMC_ANALOG_ID	=	SMC_ANALOG_ID
TP_SMC_GPU_ISENSE	=	SMC_GPU_ISENSE
SMC_MCP_VSENSE	=	SMC_GPU_VSENSE
SMC_GFX_THROTTLE_L	=	SMC_IG_THROTTLE_L
SMS_INT_L	=	SMC_SMS_INT
MCP_WAKE_REO_L	=	SMC_G3H_POWERON_L
SMC_MCP_SAFE_MODE	=	MCP_SPKR
PM_SLP_S3_L	=	DP_PWR:S0
SMC_SLPS5_L	=	DP_PWR:SMC
SMC_DP_HPD_L	=	DP_EXT_HPD_L

Unused Pins

SMS_ONOFF_L	=	TP_SMS_ONOFF_L
SMC_SYS_KBDLED	=	TP_SMC_SYS_KBDLED
SMC_FAN_1_CTL	=	TP_SMC_FAN_1_CTL
TP_SMC_FAN_1_TACH	=	SMC_FAN_1_TACH
SMC_FAN_2_CTL	=	NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH	=	SMC_FAN_2_TACH
SMC_FAN_3_CTL	=	NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH	=	SMC_FAN_3_TACH
SMC_RSTGATE_L	=	TP_SMC_RSTGATE_L
SMC_P10	=	TP_SMC_P10
SMC_P20	=	TP_SMC_P20
SMC_P24	=	TP_SMC_P24
SMC_PH3	=	TP_SMC_PH3

SMC Pull-ups

SMC_PA0	R5091	100K	1	2	5%	1/20W	MF	201
SMC_PA1	R5092	100K	1	2	5%	1/20W	MF	201
SMC_PB4	R5088	10K	1	2	5%	1/20W	MF	201
SMC_ONOFF_L	R5070	10K	1	2	5%	1/20W	MF	201
SMC_LID	R5071	100K	1	2	5%	1/20W	MF	201
SMC_TX_L	R5073	10K	1	2	5%	1/20W	MF	201
SMC_RX_L	R5074	100K	1	2	5%	1/20W	MF	201
SMC_TMS	R5077	10K	1	2	5%	1/20W	MF	201
SMC_TDO	R5078	10K	1	2	5%	1/20W	MF	201
SMC_TDI	R5079	10K	1	2	5%	1/20W	MF	201
SMC_TCK	R5080	10K	1	2	5%	1/20W	MF	201
SMC_ODD_DETECT	R5040	10K	1	2	5%	1/20W	MF	201
SMC_BIL_BUTTON_L	R5081	10K	1	2	5%	1/20W	MF	201
SMC_BC_ACOK	R5087	470K	1	2	5%	1/20W	MF	201
SMC_GFX_OVERTEMP_L	R5094	10K	1	2	5%	1/20W	MF	201
SMC_G3H_POWERON_L	R5098	100K	2	1	5%	1/20W	MF	201
SMS_INT_L	R5093	10K	1	2	5%	1/20W	MF	201
WIFI_EVENT_L	R5089	10K	1	2	5%	1/20W	MF	201
SMC_PME_S4_L	R5076	100K	1	2	5%	1/20W	MF	201

SMC Pull-downs

SMC_ADAPTER_EN	R5085	10K	1	2	5%	1/20W	MF	201
SMC_CASE_OPEN	R5086	10K	1	2	5%	1/20W	MF	201
SMC_DP_HPD_L	R5090	100K	1	2	5%	1/20W	MF	201

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

SMC Support

Apple Inc.

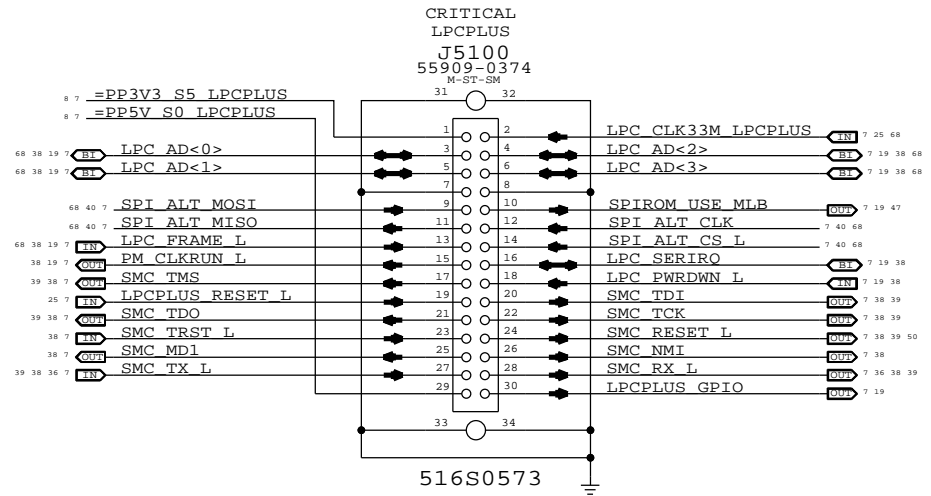
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REVISION: 4.4.0

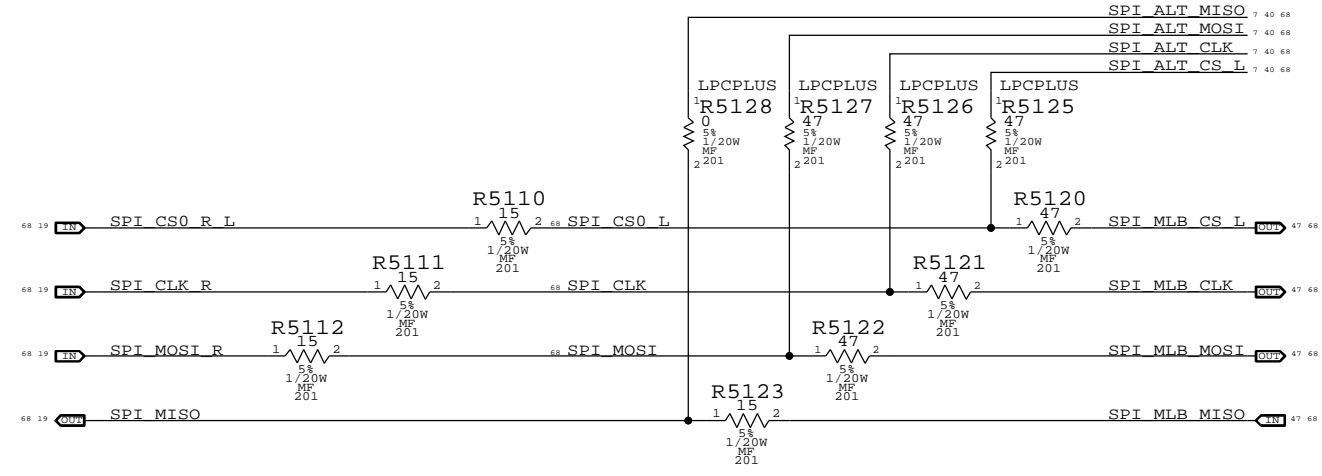
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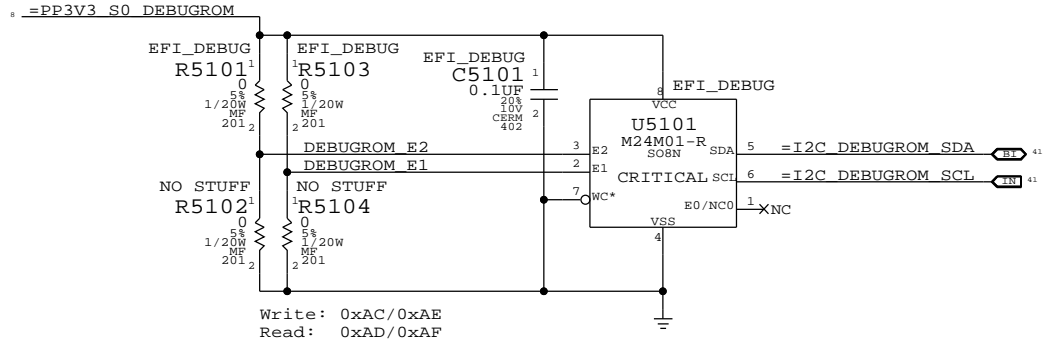
LPC+SPI Connector



SPI Bus Series Termination

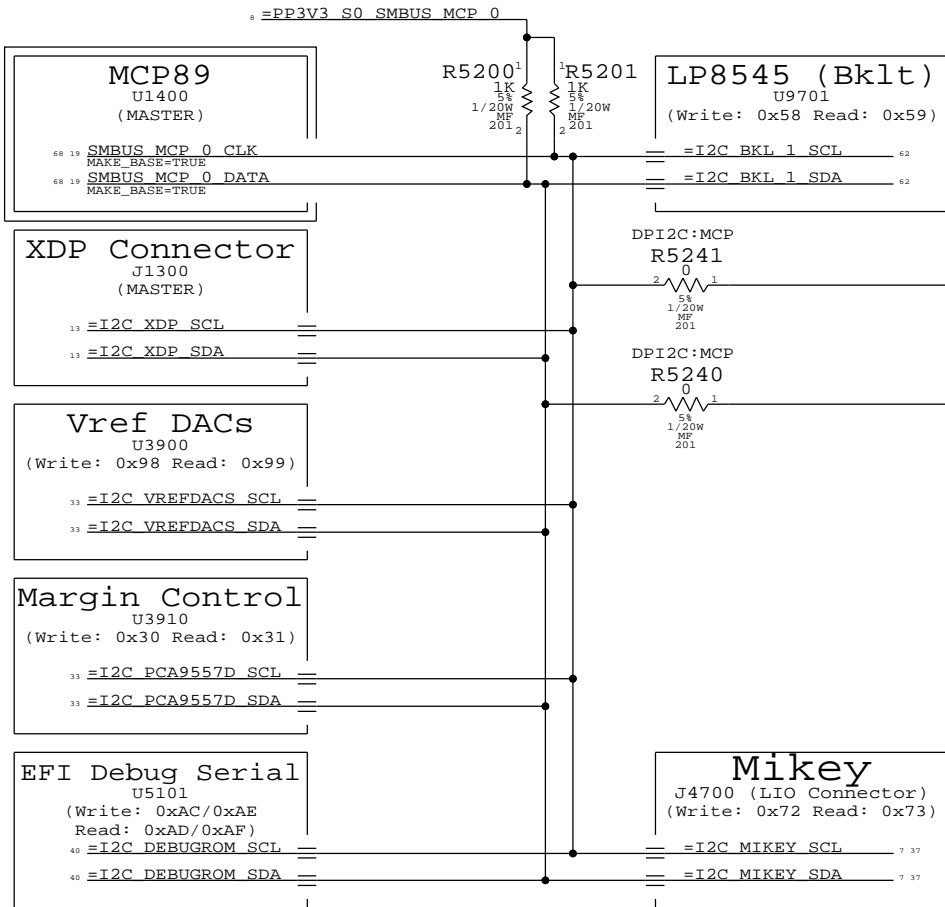


EFI Debug ROM

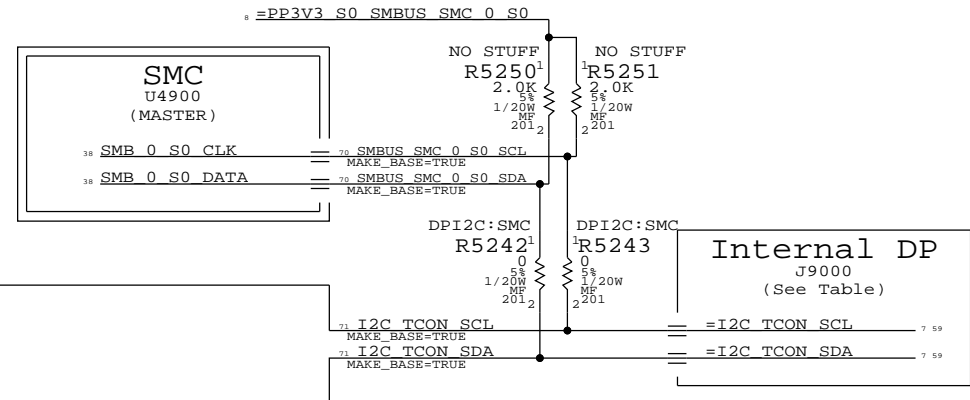


PAGE TITLE		SYNC DATE=07/07/2010	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8379	D
		REVISION	
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MCP89 SMBus "0" Connections



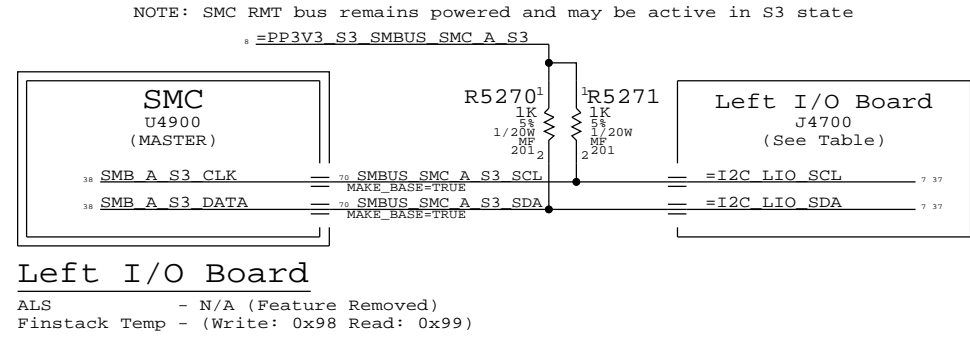
SMC "0" SMBus Connections



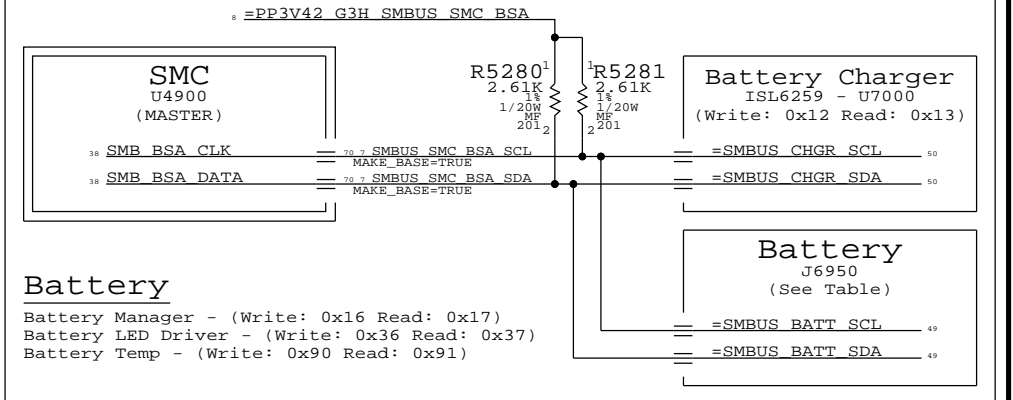
(* = Multiple options)

	K16	Samsung	LGD	K99	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	Y	*	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	Y	Y	N

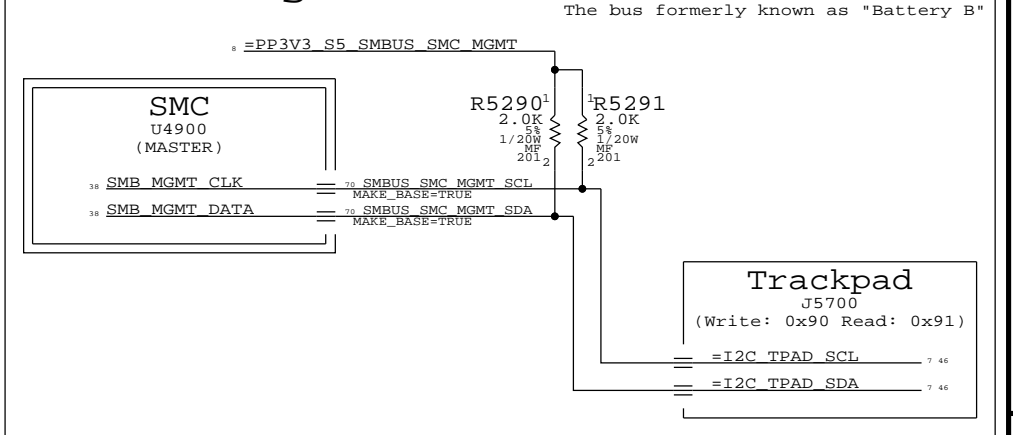
SMC "A" SMBus Connections



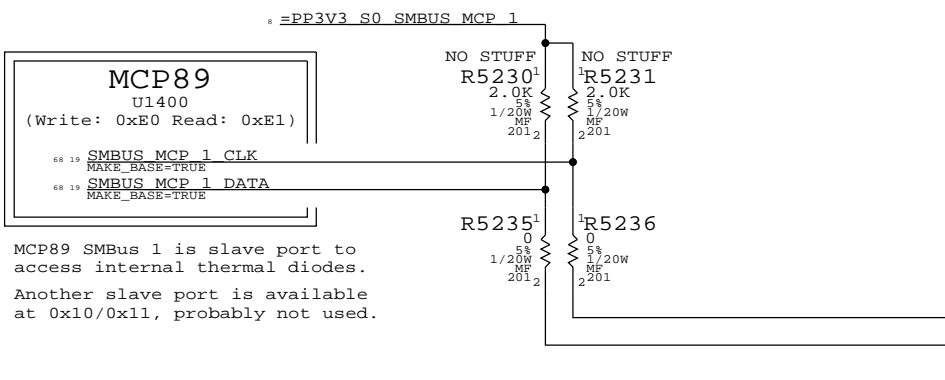
SMC "Battery A" SMBus Connections



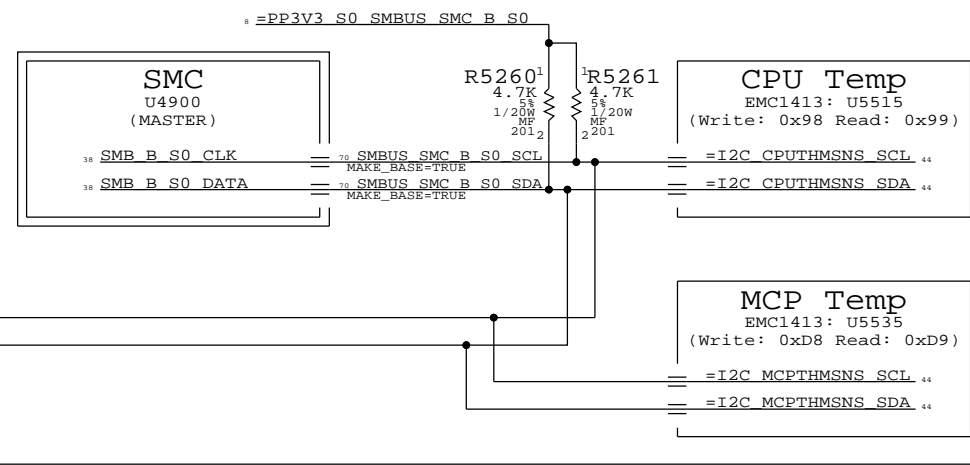
SMC "Management" SMBus Connections



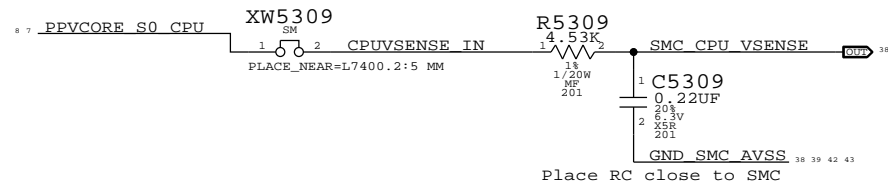
MCP89 SMBus "1" Connections



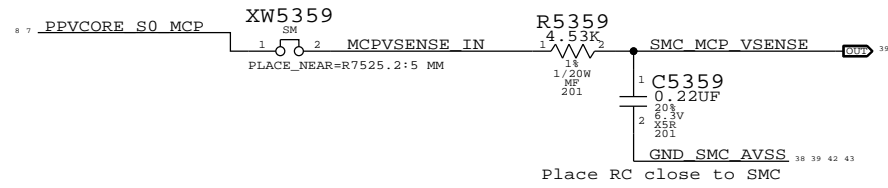
SMC "B" SMBus Connections



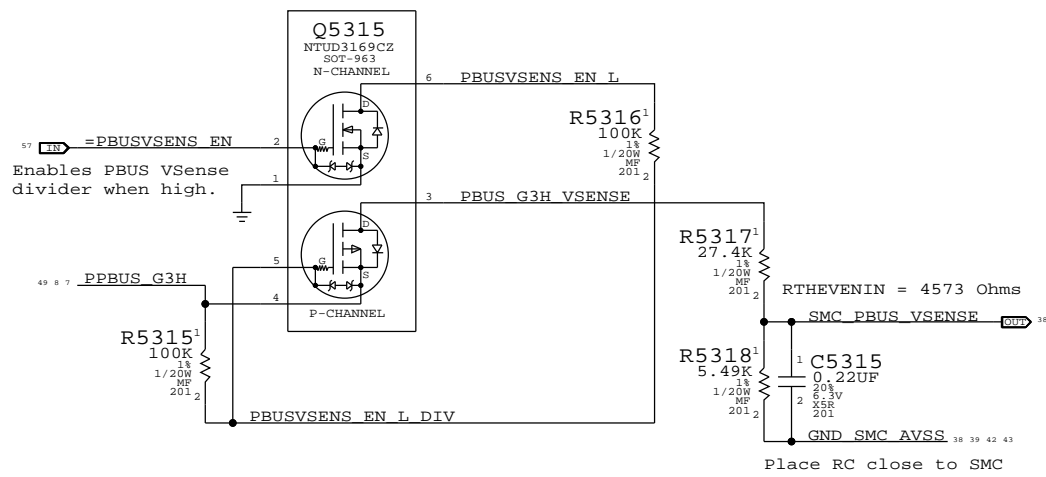
CPU Voltage Sense / Filter



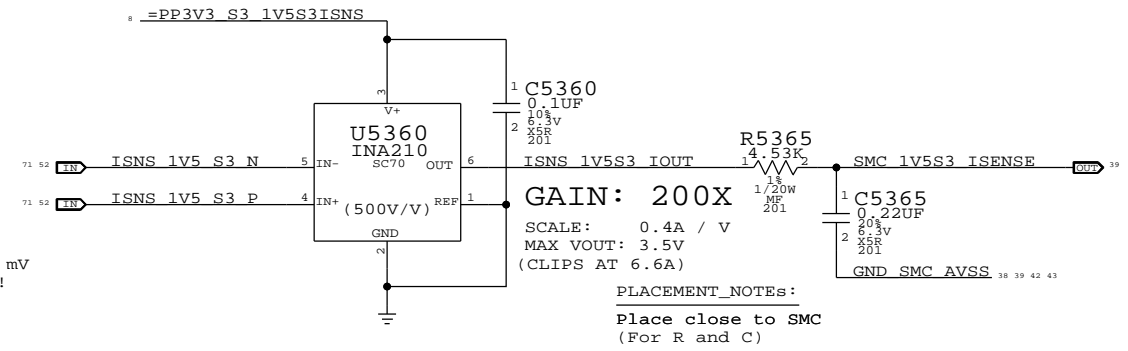
MCP Voltage Sense / Filter



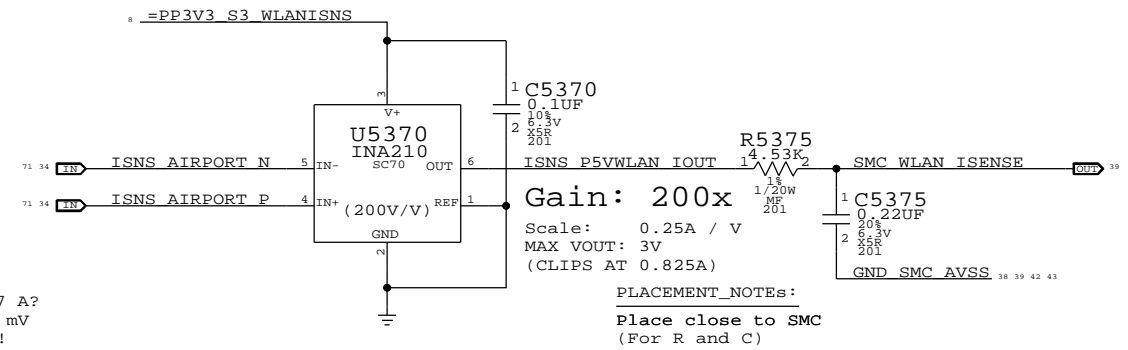
PBUS Voltage Sense Enable & Filter



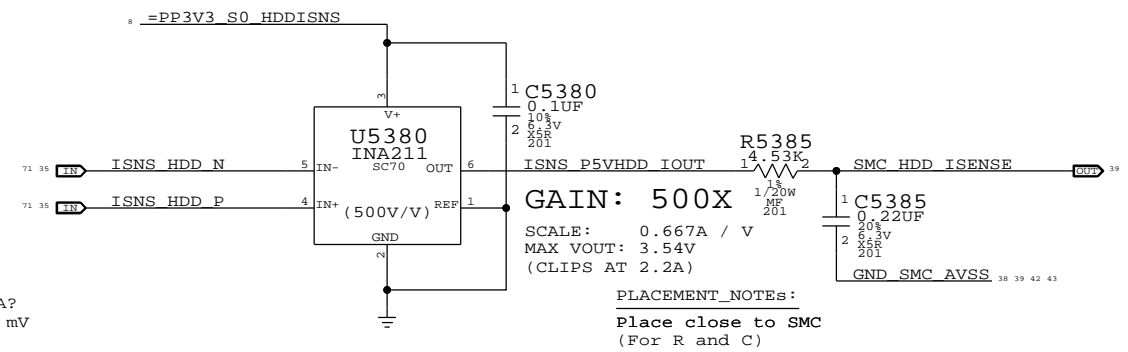
DDR3 1V5R1V35 Current Sense / Filter



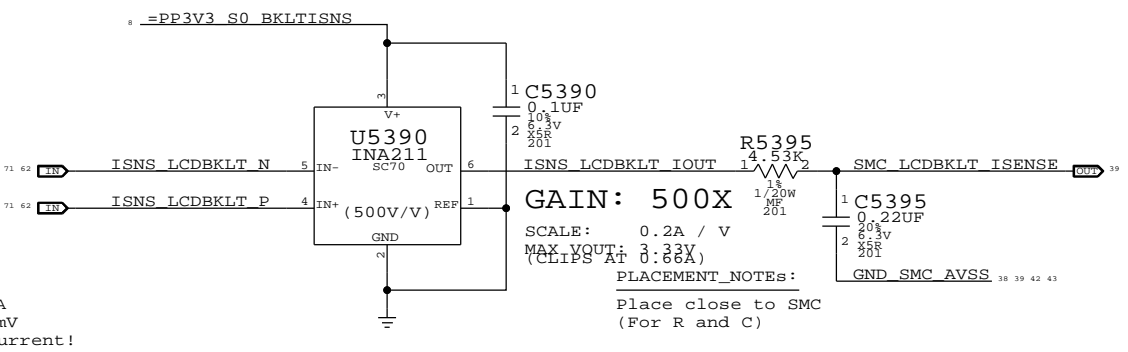
AirPort Current Sense / Filter



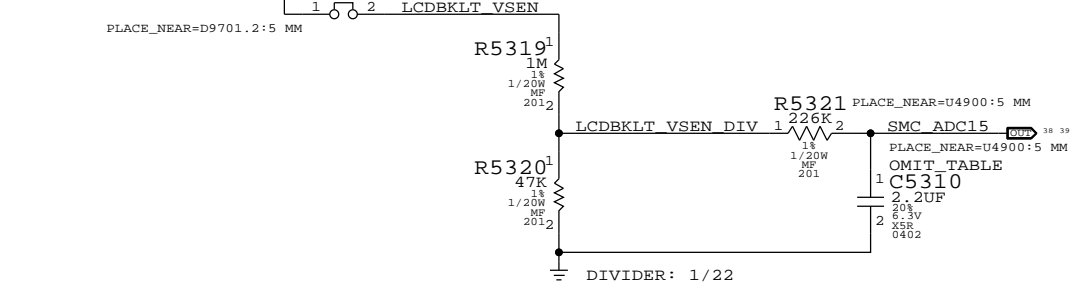
HDD Current Sense / Filter



LCD Backlight Driver Input Current Sense / Filter

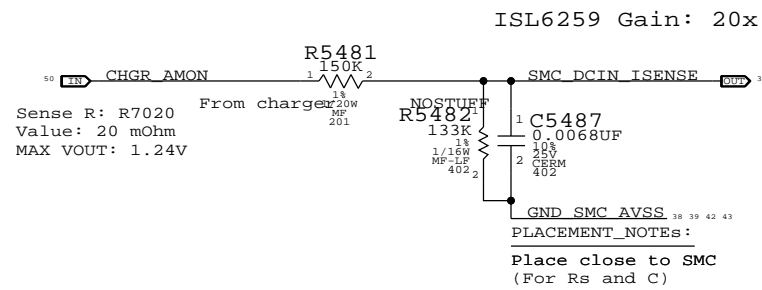


PPVOUT SW LCDBKLT

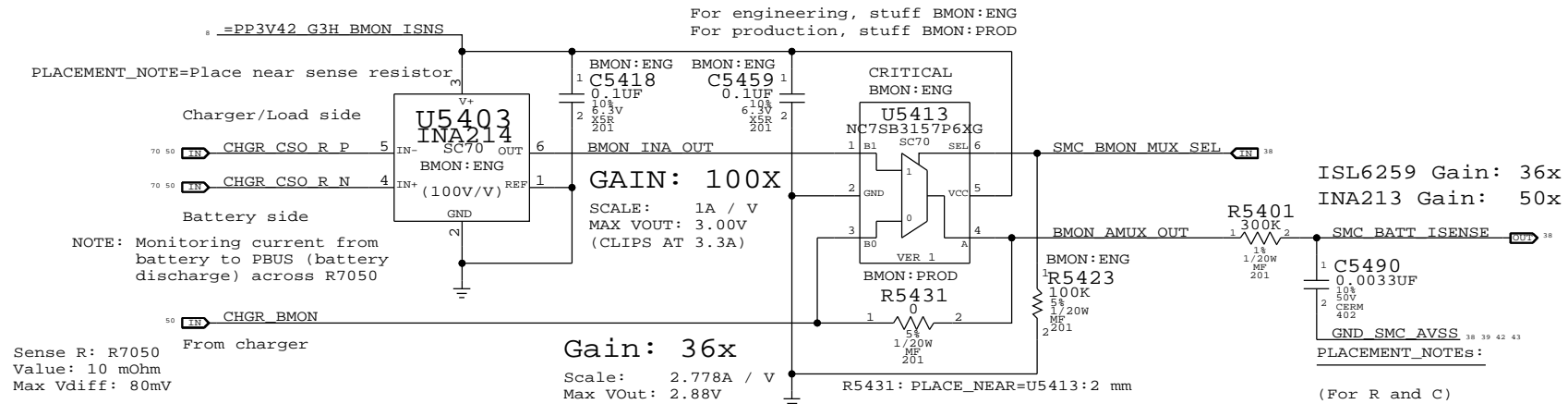


PAGE TITLE		DRAWING NUMBER	
Voltage & Current Sensing		051-8379	
Apple Inc.		REVISION	
		4.4.0	
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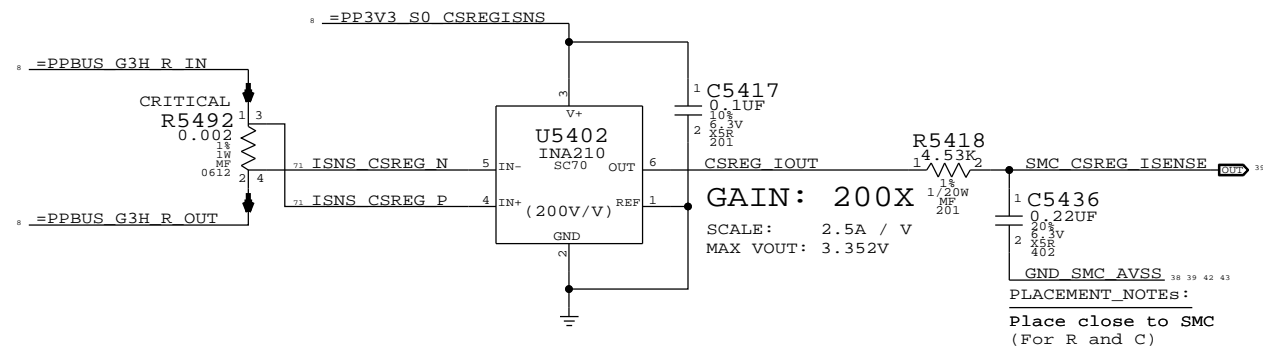
DCIN (AMON) Current Sense, RMUX & Filter



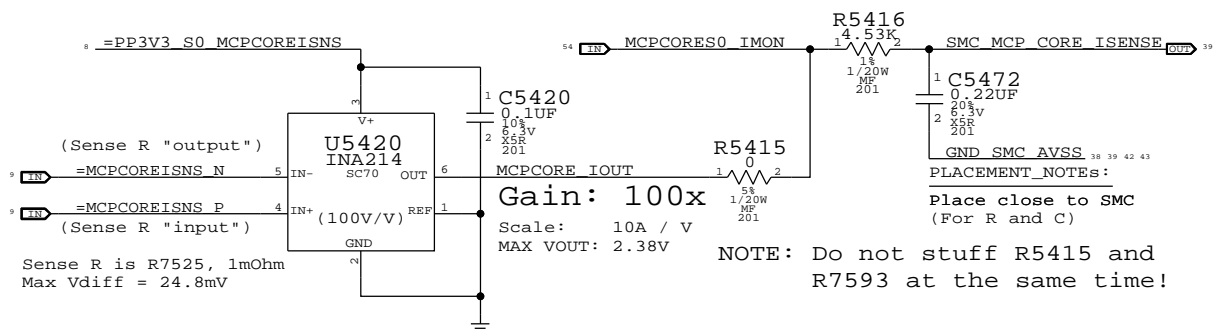
Battery (BMON) Current Sense, MUX & Filter



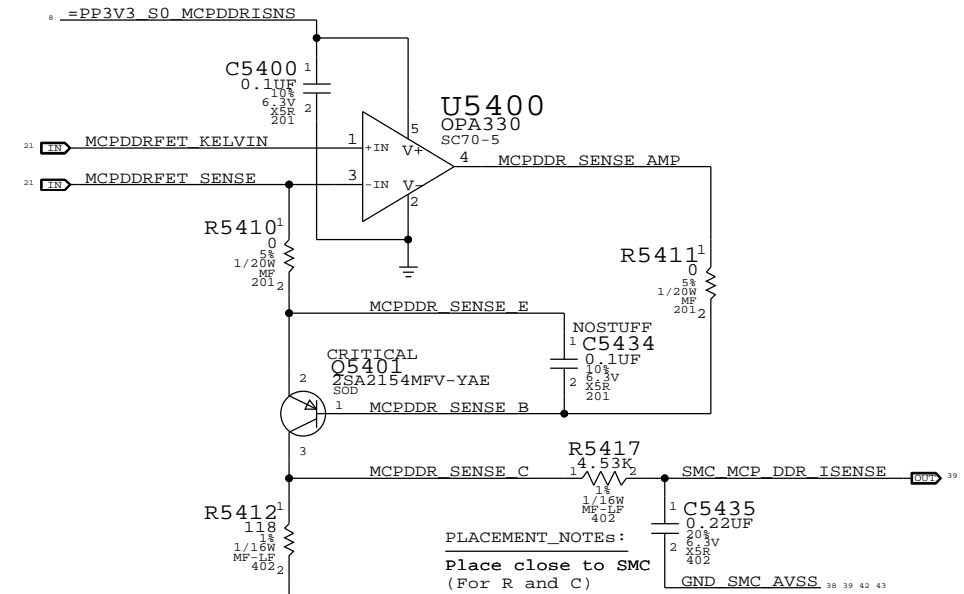
Chipset Regulators High-Side Current Sense / Filter



MCP VCore Current Sense Filter

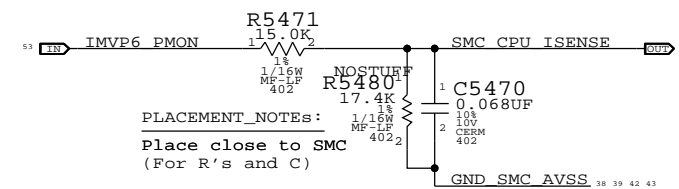


MCP MEM VDD Current Sense / Filter



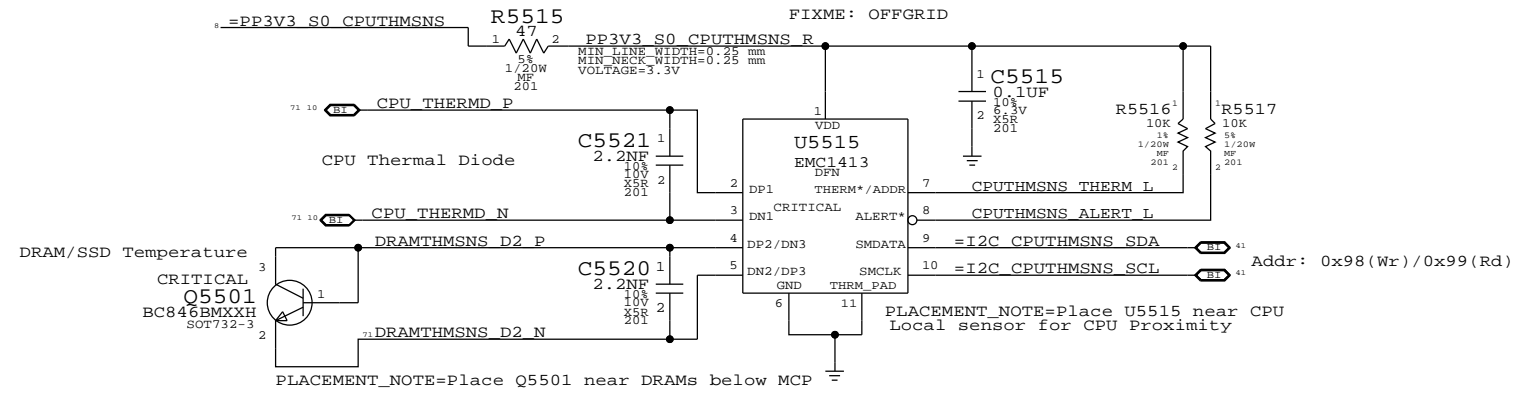
VERIFY ALL RESISTOR AND GAINS

CPU VCore Load Side Current Sense / Filter

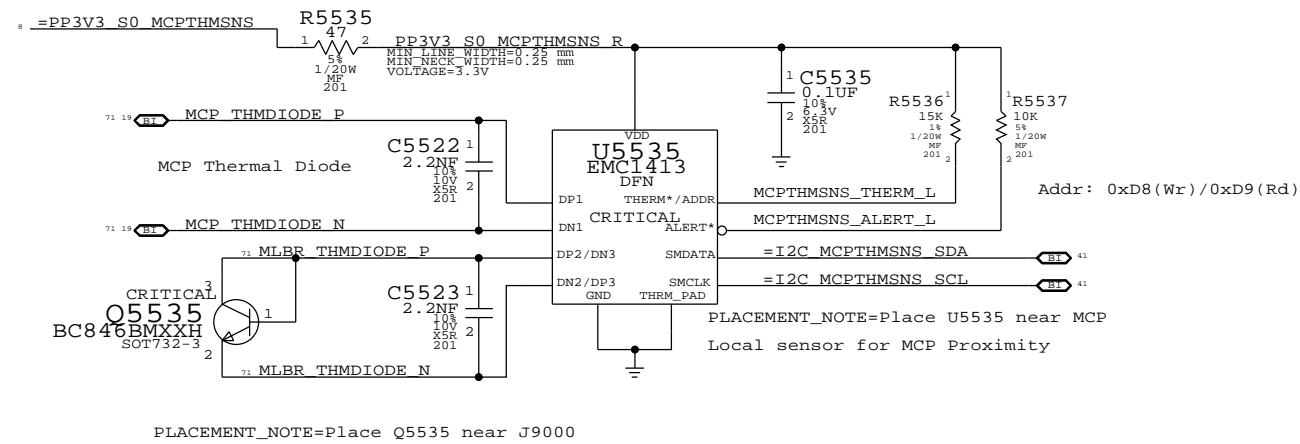


PAGE TITLE		DRAWING NUMBER		SIZE	
Current Sensing		051-8379		D	
Apple Inc.		REVISION		4.4.0	
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CPU T-Diode Thermal Sensor

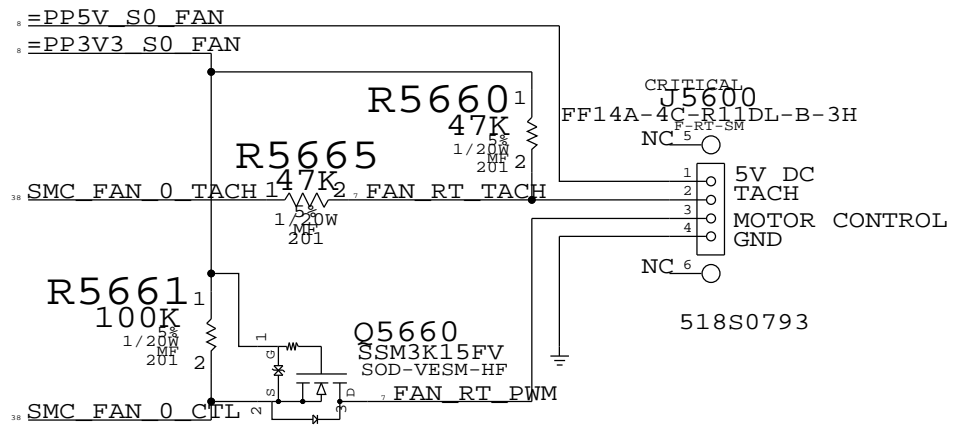


MCP T-Diode Thermal Sensor



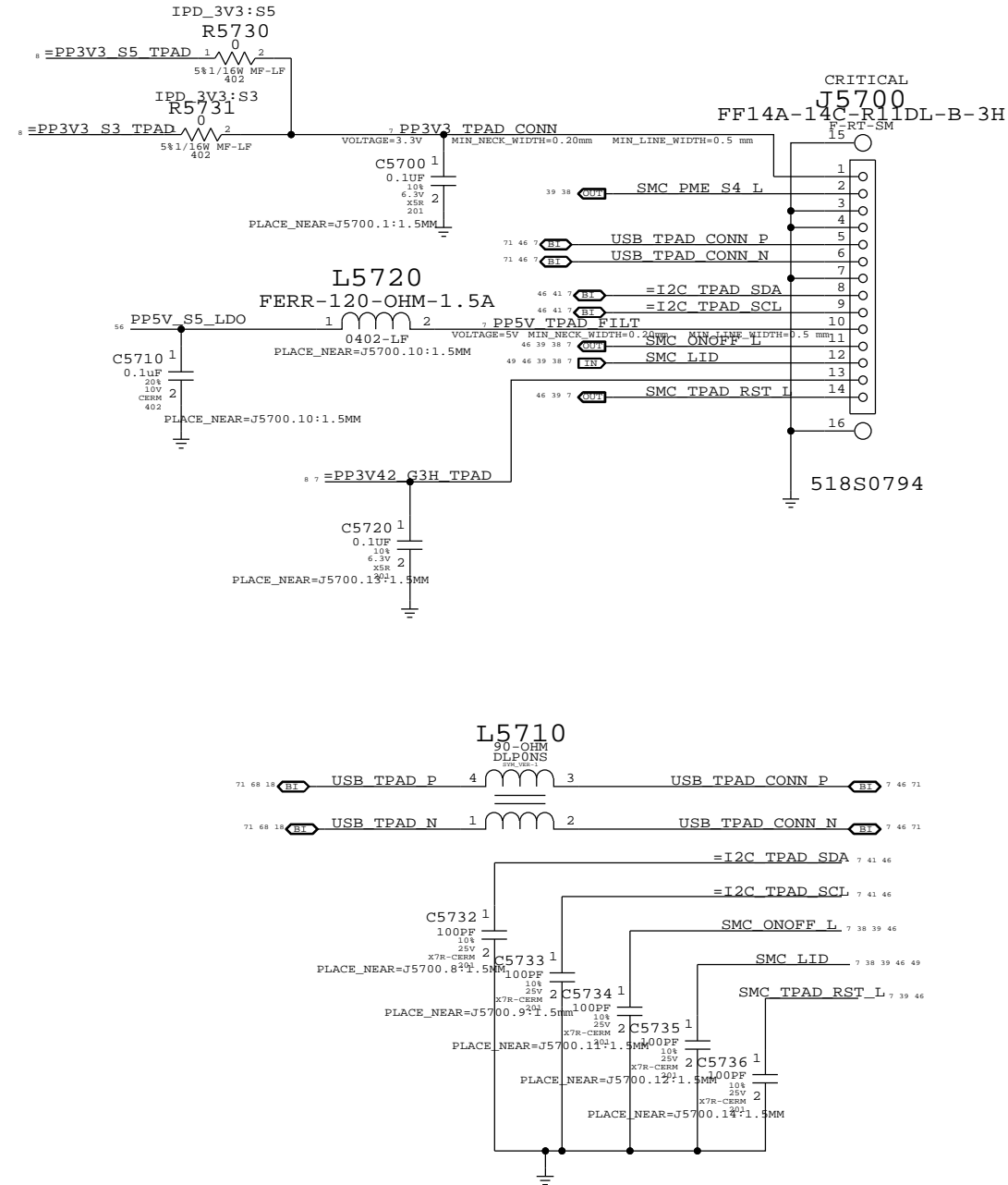
SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
Thermal Sensors			
Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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FAN CONNECTOR

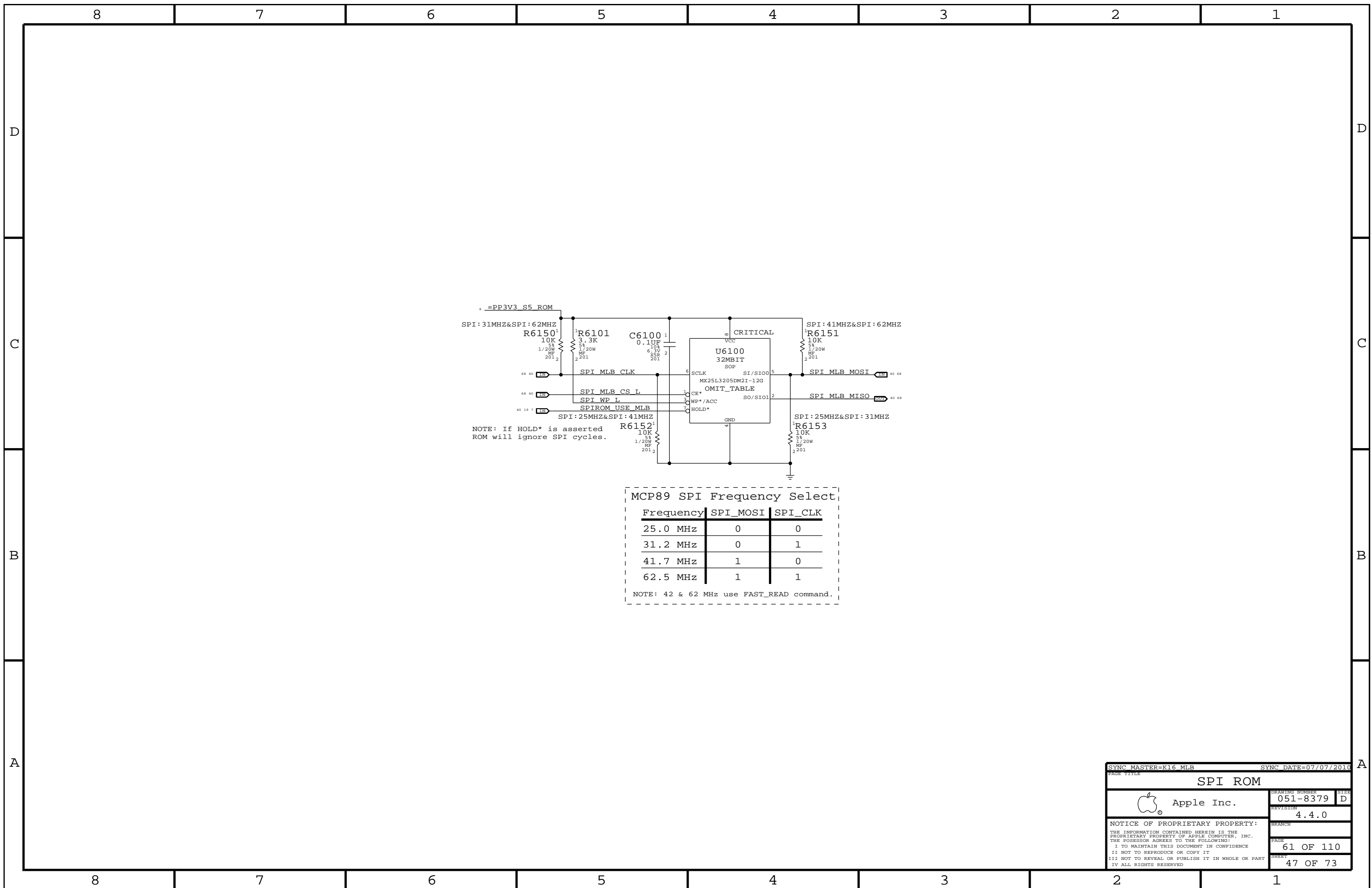


SYNC MASTER=K16_MLB		SYNC DATE=07/07/2010	
PAGE TITLE Fan			
DRAWING NUMBER 051-8379		SIZE D	
REVISION 4.4.0		BRANCH	
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IPD Flex Connector



SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
WELLSPRING 1			
Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: SPI ROM

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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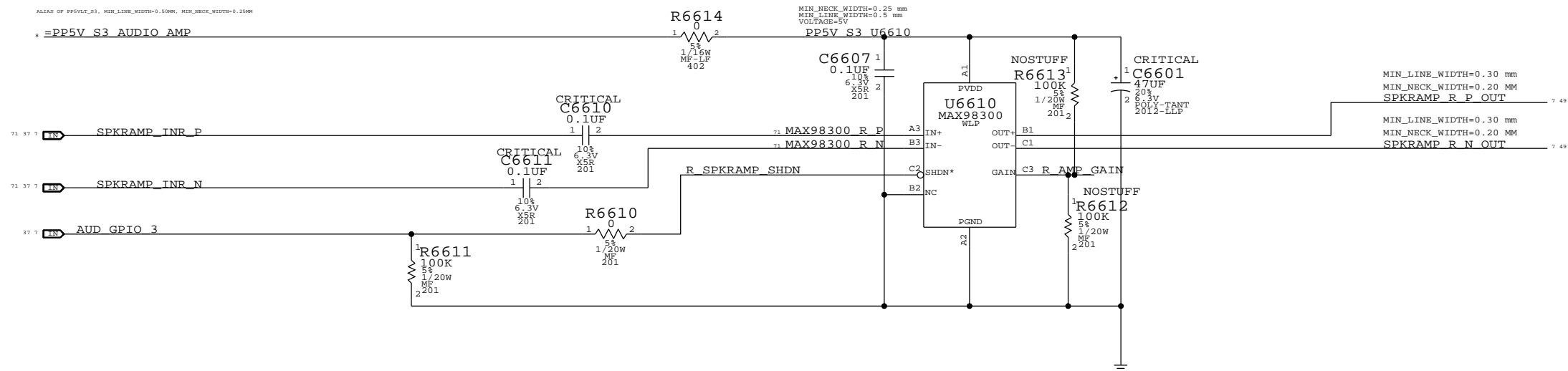
SHEET: 47 OF 73

SPEAKER AMPLIFIERS

APN: 353S2888

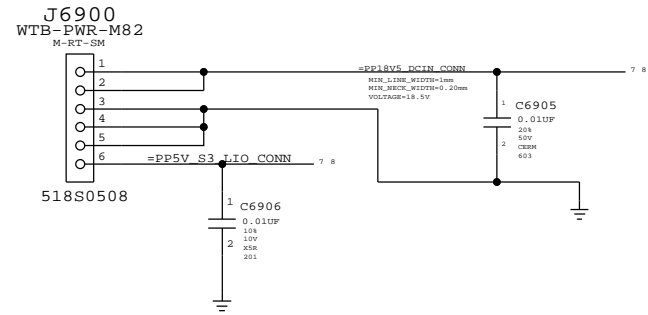
SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB

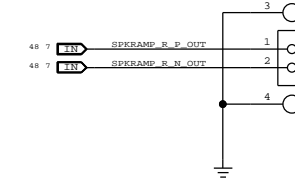


SYNC_MASTER=AUDIO		SYNC_DATE=02/09/2010	
PAGE TITLE AUDIO: SPEAKER AMP			
DRAWING NUMBER 051-8379		SIZE D	
REVISION 4.4.0		BRANCH	
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PAGE 66 OF 110		SHEET 48 OF 73	

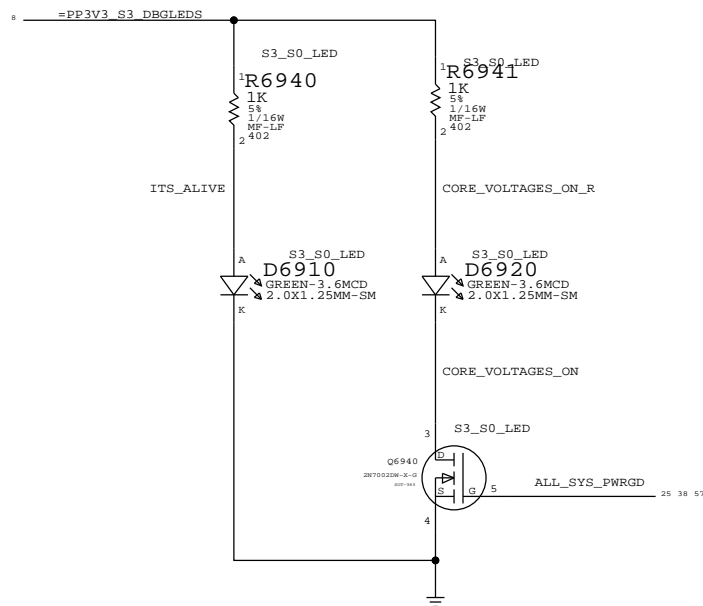
MLB TO LIO POWER CABLE CONNECTOR



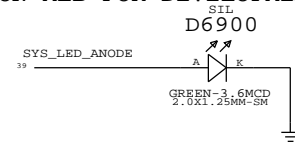
APN: 518S0519
CRITICAL
J6903
78171-0002
M-RT-SM



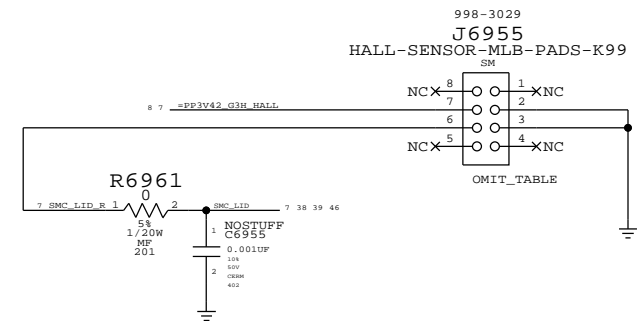
SPKR



SIL ON MLB FOR DEVELOPMENT ONLY

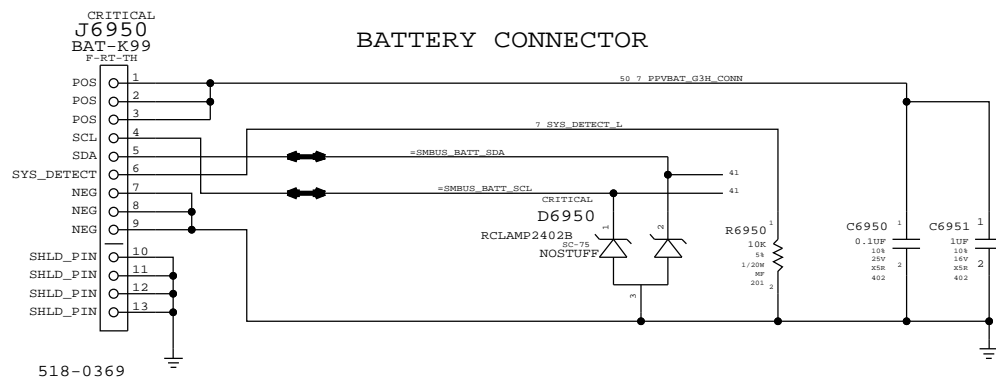


S3 AND S0 INDICATOR LEDS FOR DEVELOPMENT ONLY



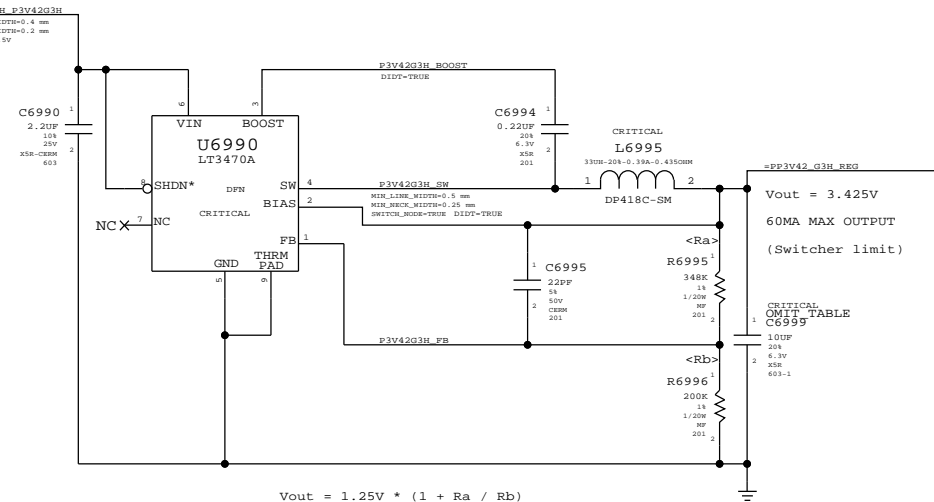
HALL EFFECT PADS

BATTERY CONNECTOR



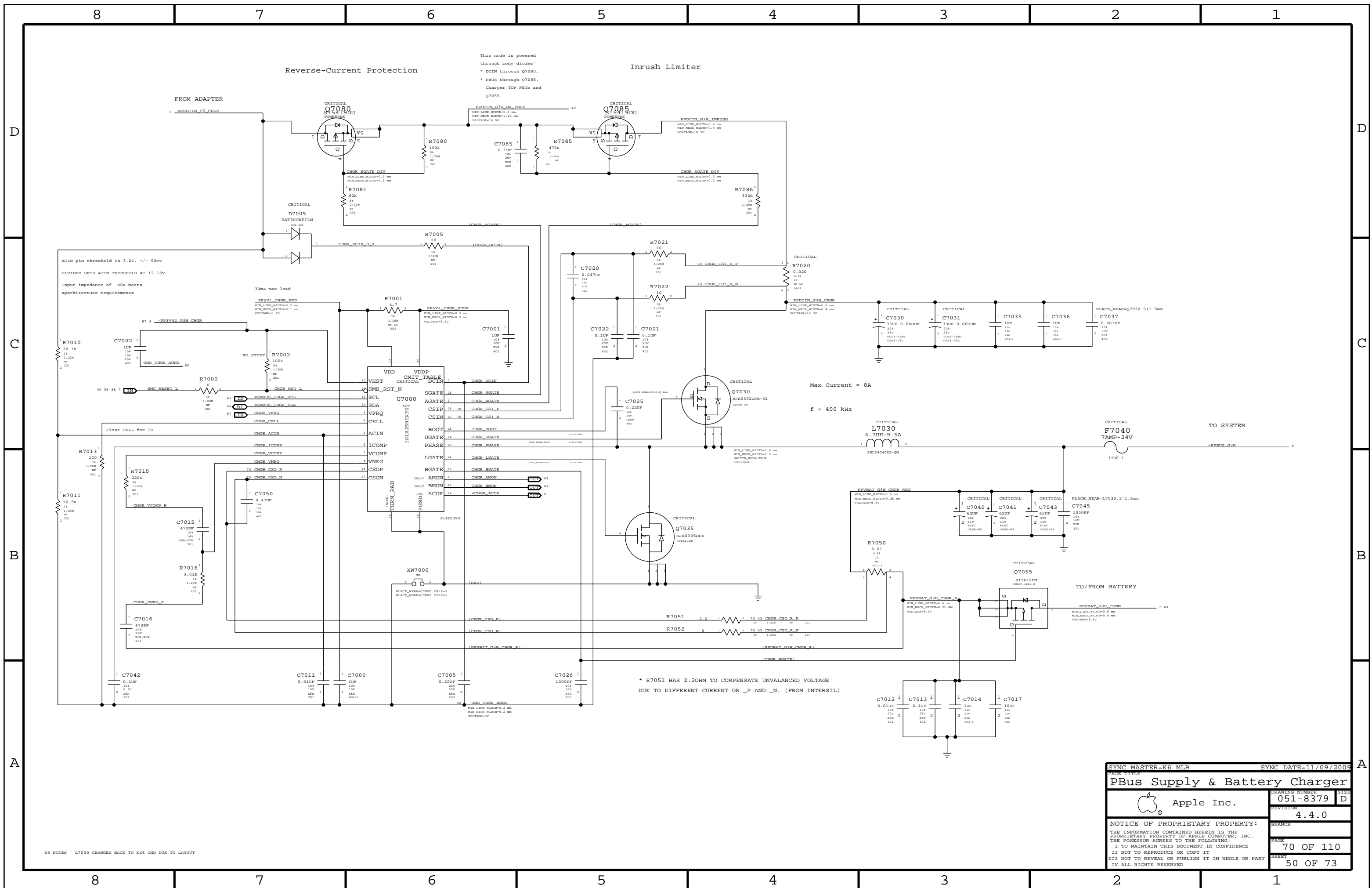
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator



$$V_{out} = 1.25V * (1 + R_a / R_b)$$

SYNC MASTER=K84 MLB		SYNC DATE=11/09/2009	
DC-In & Battery Connectors			
Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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		PAGE	69 OF 110
		SHEET	49 OF 73



This node is powered through body diodes:
 * DCIN through Q7080.
 * FBUS through Q7085.
 * Charger TOP FETs and Q7055.

Reverse-Current Protection

Inrush Limiter

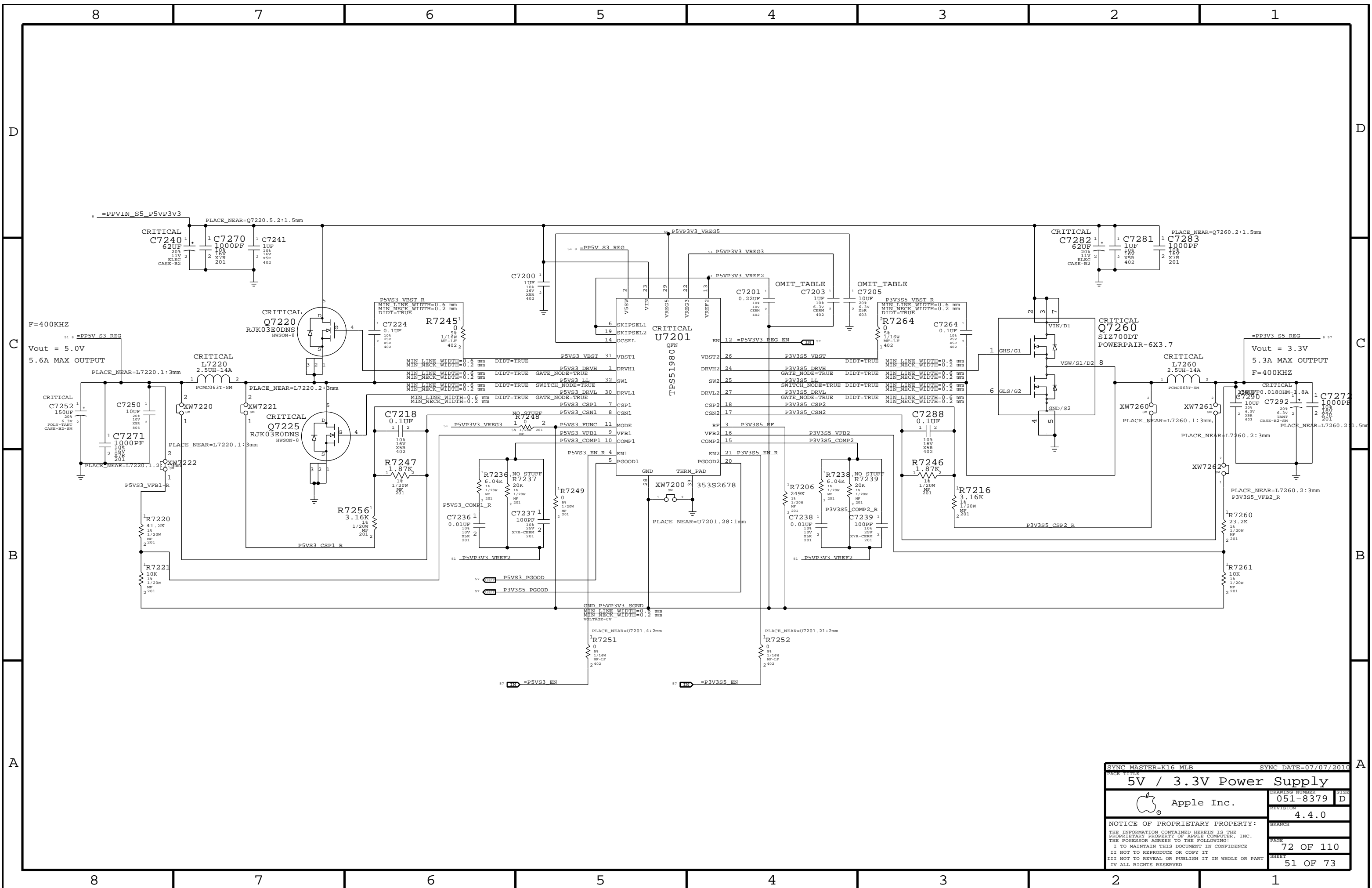
Max Current = 8A

f = 400 kHz

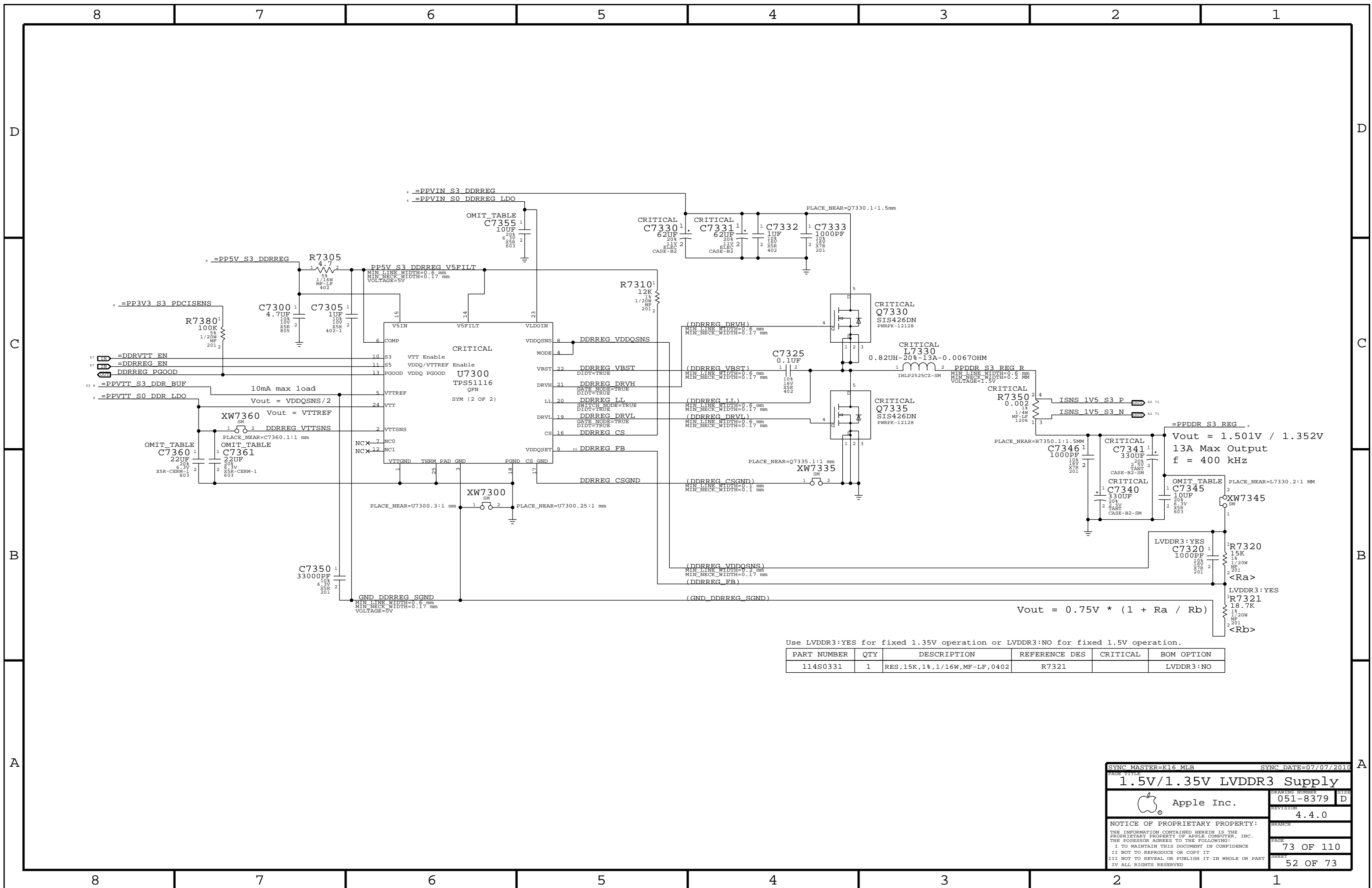
* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

PAGE TITLE		SYNC DATE=11/09/2009	
PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8379	D
		REVISION	
		4.4.0	
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PAGE		SHEET	
70 OF 110		50 OF 73	

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT



SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
5V / 3.3V Power Supply			
DRAWING NUMBER	051-8379	SIZE	D
REVISION	4.4.0	BRANCH	
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PAGE	72 OF 110	SHEET	51 OF 73



Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321	CRITICAL	LVDDR3:NO

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

1.5V/1.35V LVDDR3 Supply

Apple Inc.

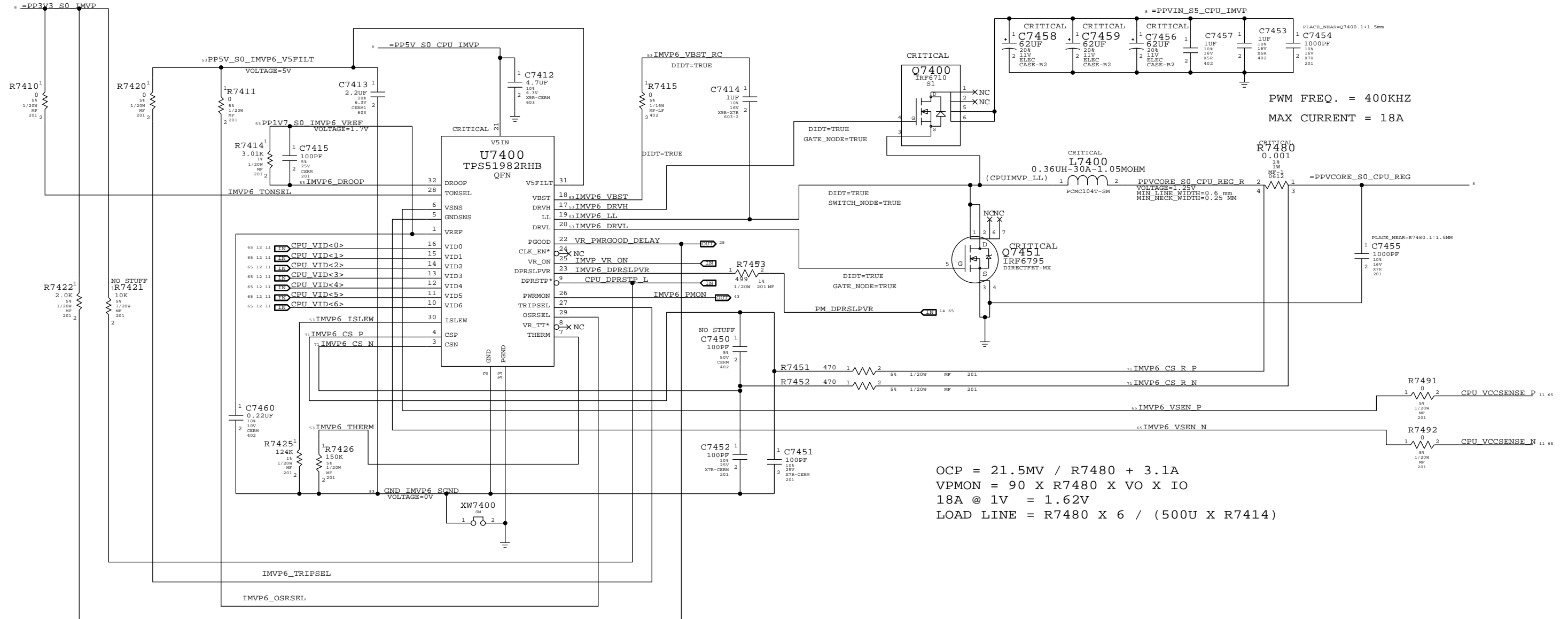
DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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 SHEET: 52 OF 73

IMVP6 CPU VCore REGULATOR



$$OCP = 21.5MV / R7480 + 3.1A$$

$$VPMON = 90 \times R7480 \times VO \times IO$$

$$18A @ 1V = 1.62V$$

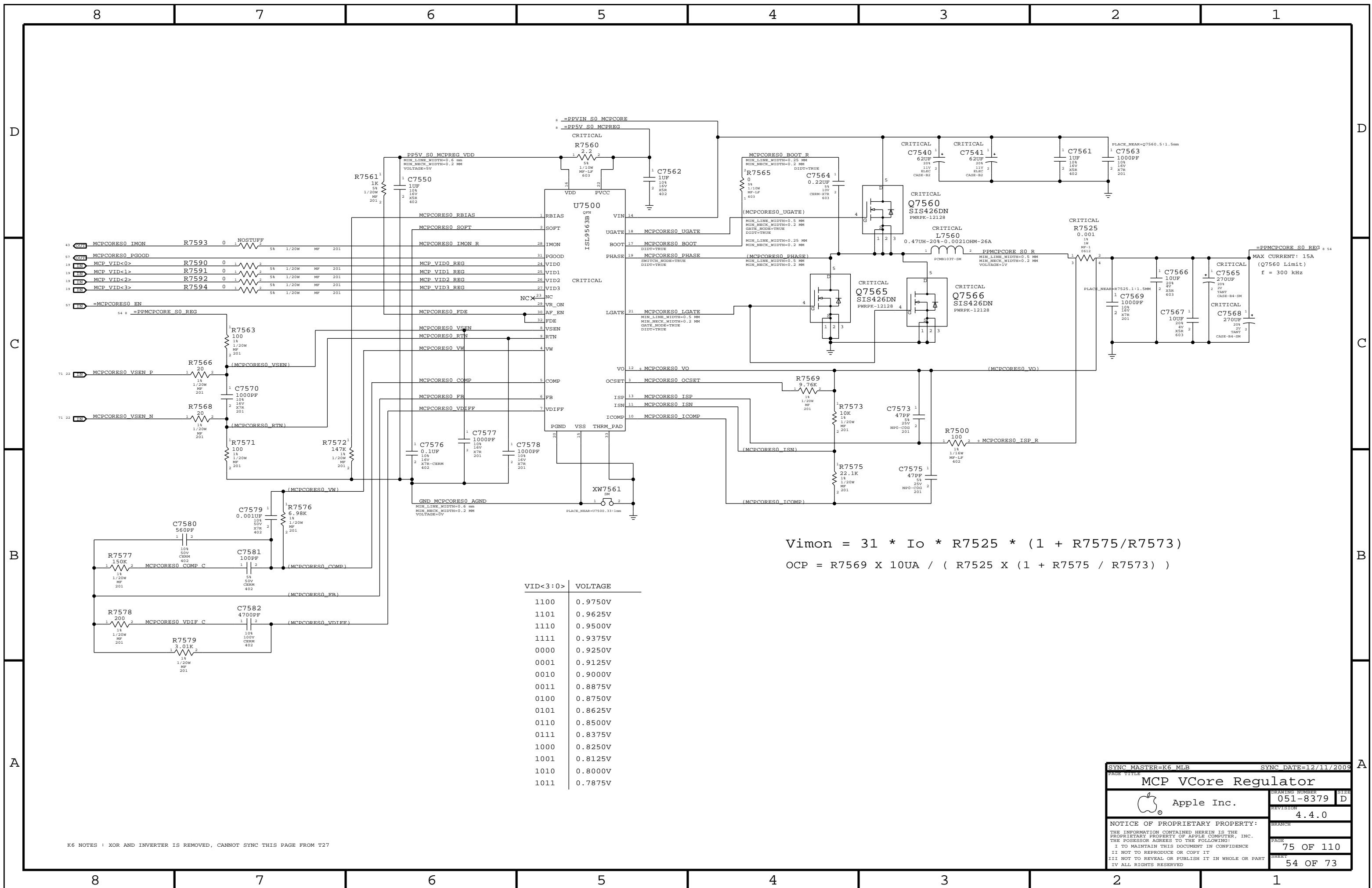
$$LOAD LINE = R7480 \times 6 / (500U \times R7414)$$

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
53 IMVP6_LL	1.5 MM	0.20 MM
53 IMVP6_VBST	0.25 MM	0.20 MM
53 IMVP6_DRVH	1.5 MM	0.20 MM
53 IMVP6_DRVL	1.5 MM	0.20 MM
53 IMVP6_VBST_RC	1.5 MM	0.20 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
53 GND_IMVP6_SGND	0.50 MM	0.20 MM
53 IMVP6_DROOP	0.25 MM	0.20 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
53 IMVP6_THERM	0.25 MM	0.20 MM
53 IMVP6_ISLEW	0.25 MM	0.20 MM
53 PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
53 PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM

SYNC MASTER=POWER		SYNC DATE=07/13/2005	
IMVP6 CPU VCore Regulator			
Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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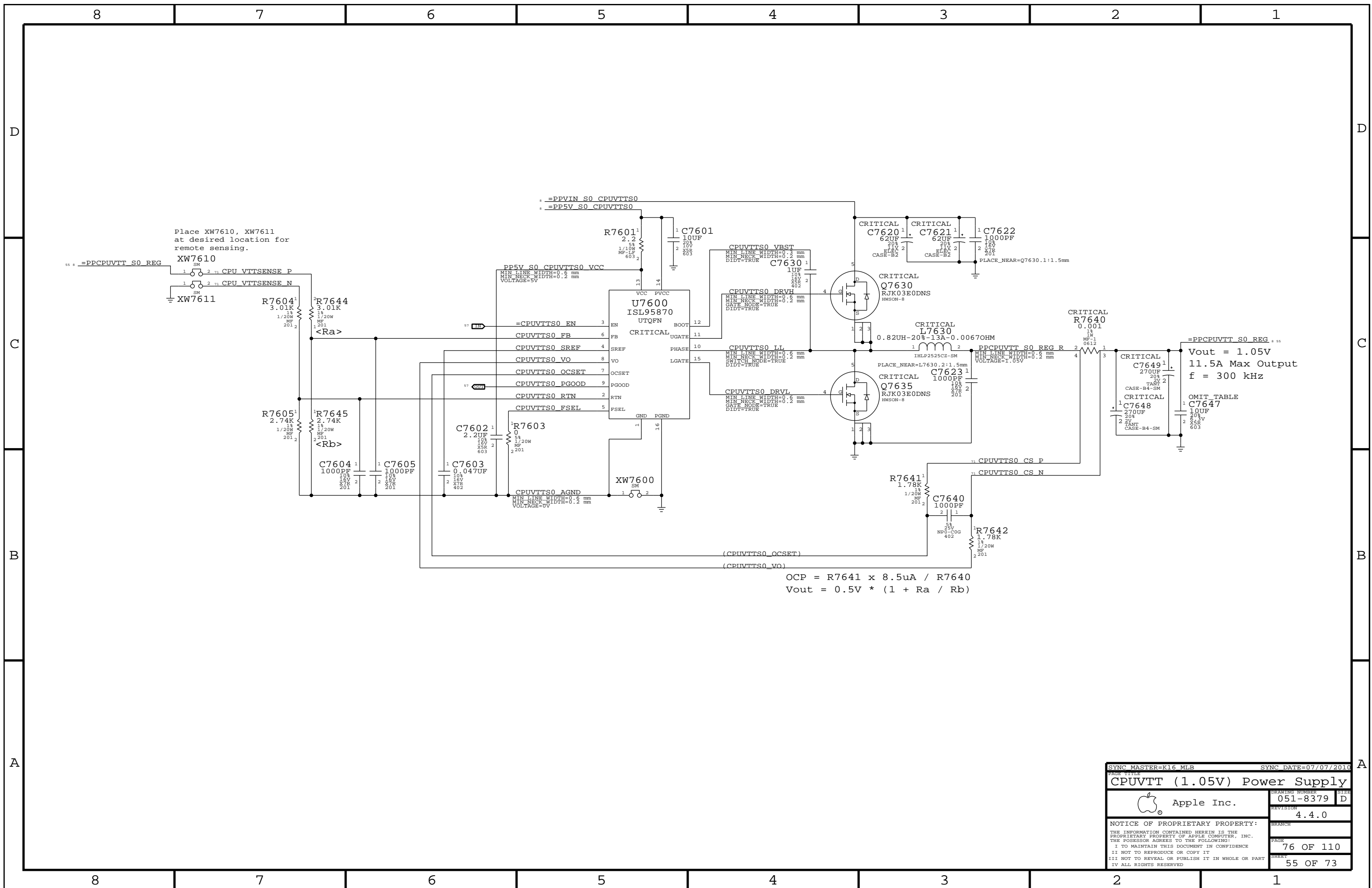
$$V_{im} = 31 * I_o * R_{7525} * (1 + R_{7575}/R_{7573})$$

$$OCP = R_{7569} * 10UA / (R_{7525} * (1 + R_{7575} / R_{7573}))$$

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

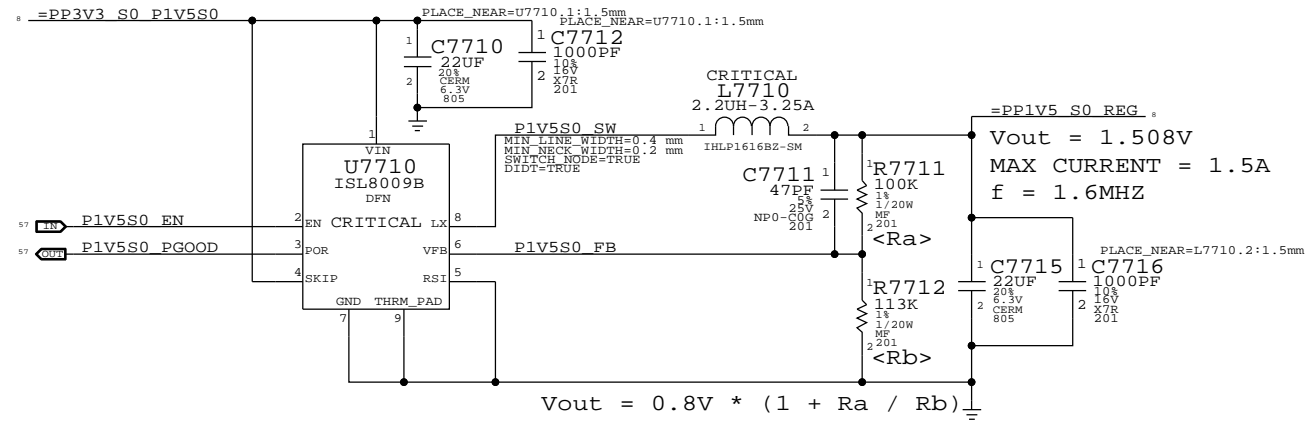
K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=K6.MLB		SYNC DATE=12/11/2009	
MCP VCore Regulator			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	BRANCH
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		PAGE	75 OF 110
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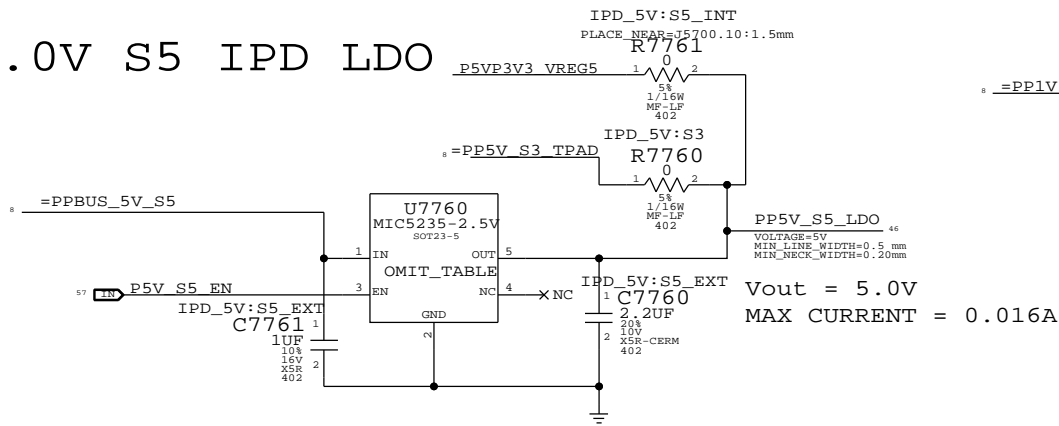


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
CPUVTT (1.05V) Power Supply			
Apple Inc.		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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1.5V S0 Regulator

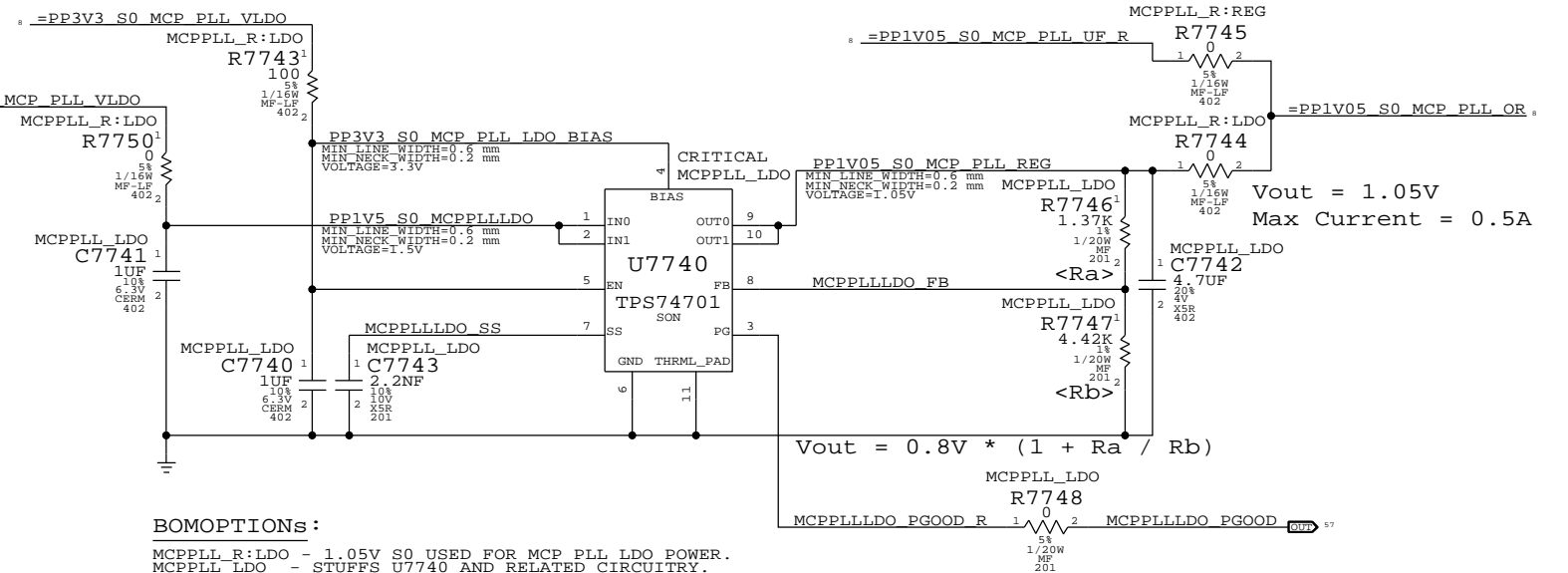


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1A,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

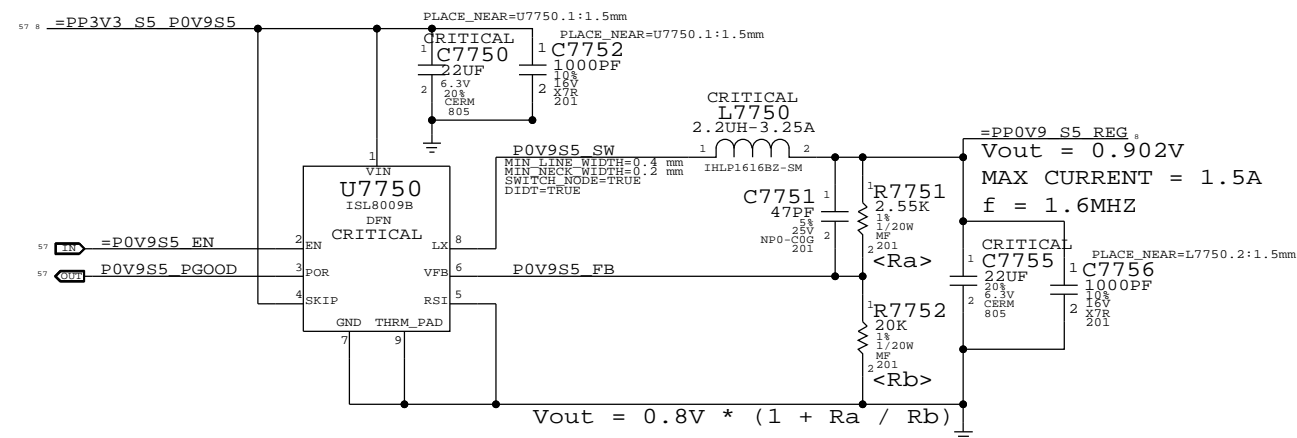
1.05V S0 MCP PLL LDO



BOMOPTIONS:

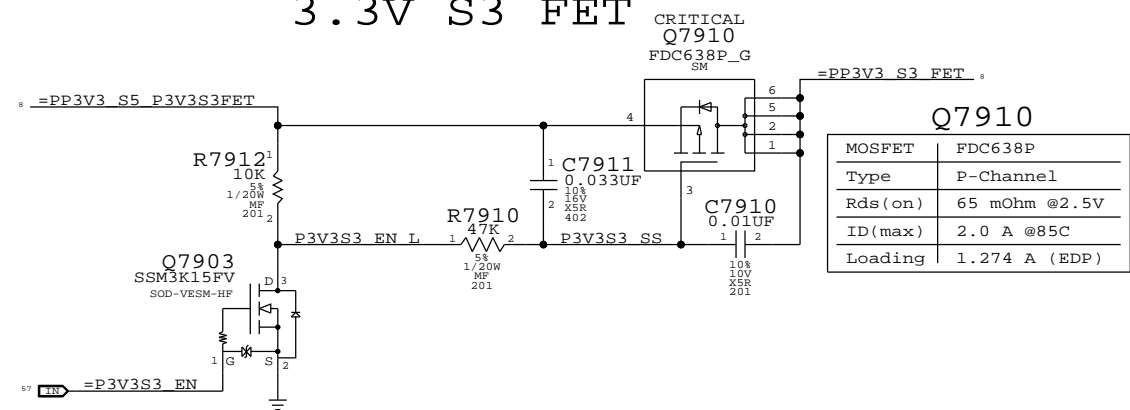
MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
Misc Power Supplies			
Apple Inc.		DRAWING NUMBER	051-8379
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		PAGE	77 OF 110
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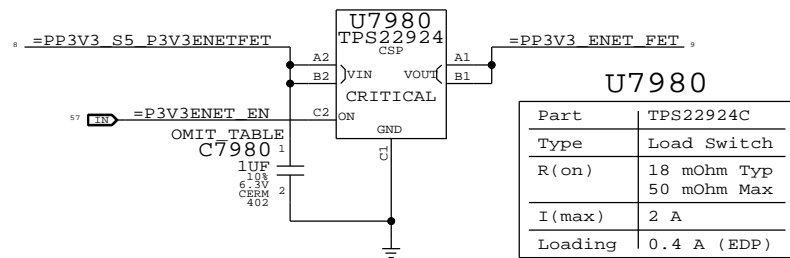
3.3V S3 FET



Q7910

Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	1.274 A (EDP)

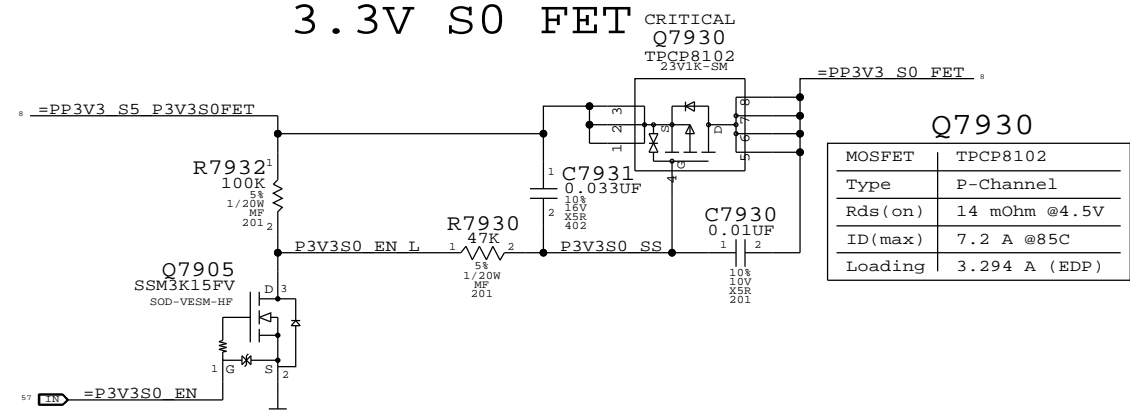
3.3V ENET Switch



U7980

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ
	50 mOhm Max
I(max)	2 A
Loading	0.4 A (EDP)

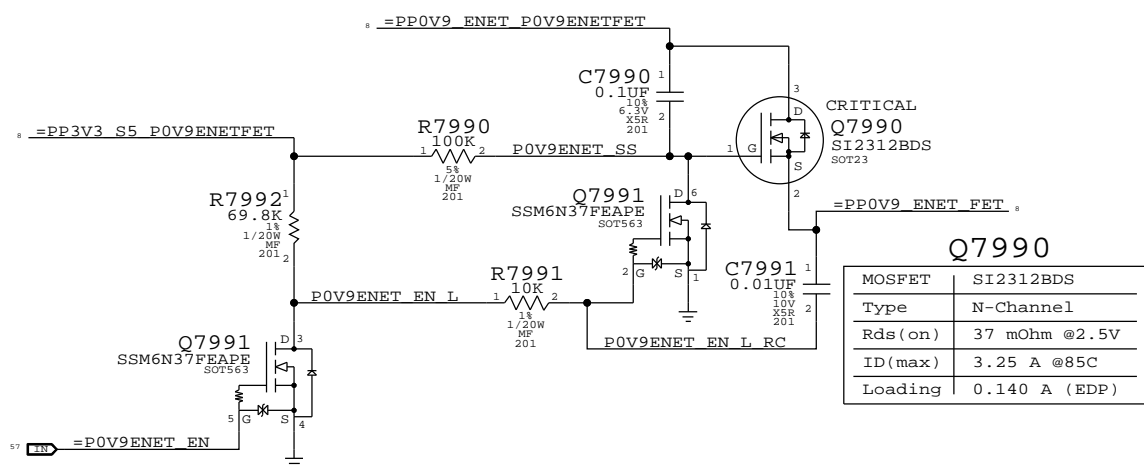
3.3V S0 FET



Q7930

Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
ID(max)	7.2 A @85C
Loading	3.294 A (EDP)

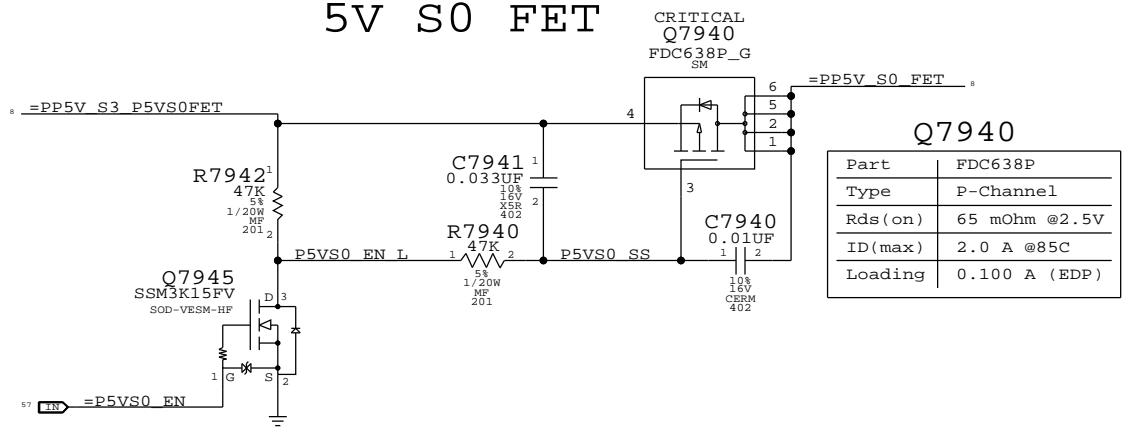
0.9V ENET FET



Q7990

Part	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

5V S0 FET



Q7940

Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.100 A (EDP)

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
Power FETs			
Apple Inc.		DRAWING NUMBER	051-8379
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		PAGE	79 OF 110
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8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

5

4

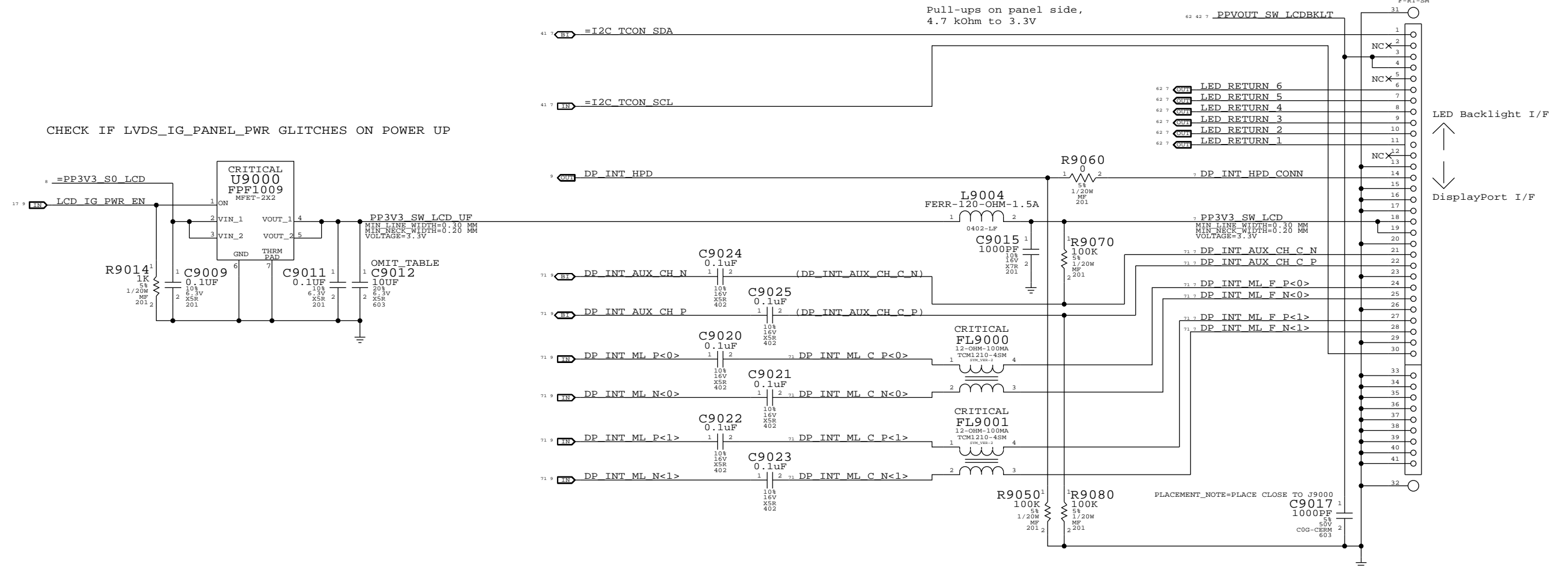
3

2

1

LCD Connector
Internal DP Connector: 518S0787

CRITICAL
J9000
CABLINE-CA
P-RT-SM



CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

Pull-ups on panel side,
4.7 kohm to 3.3V

PP3V3 SW LCD UP

PP3V3 SW LCD
MIN LINE WIDTH=0.30 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=3.3V

PLACEMENT_NOTE=PLACE CLOSE TO J9000
C9017
1000PF
50V
COG-CERM
603

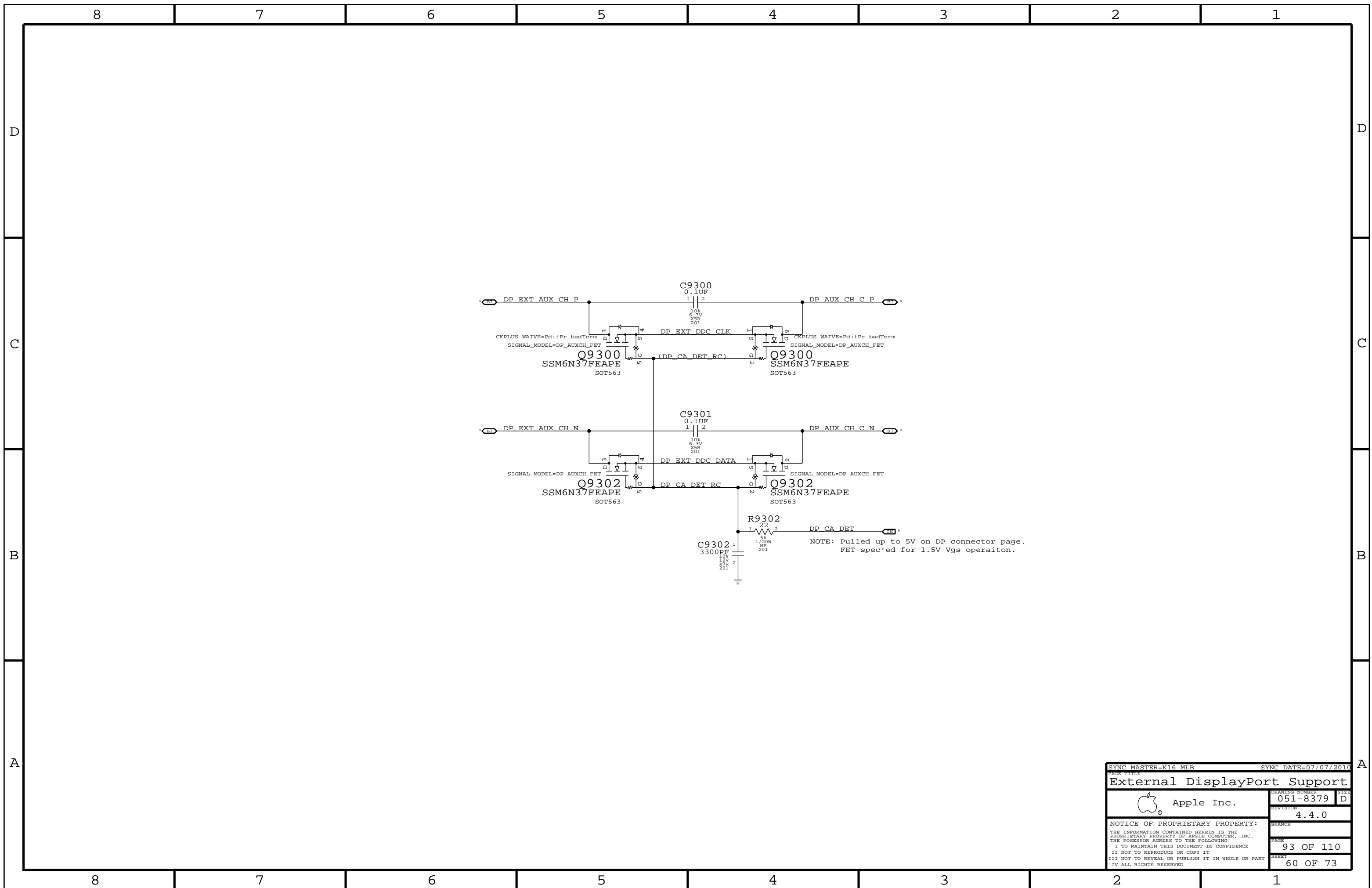
SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

Internal DisplayPort Connector

Apple Inc.	DRAWING NUMBER	051-8379	SIZE	D
	REVISION	4.4.0		

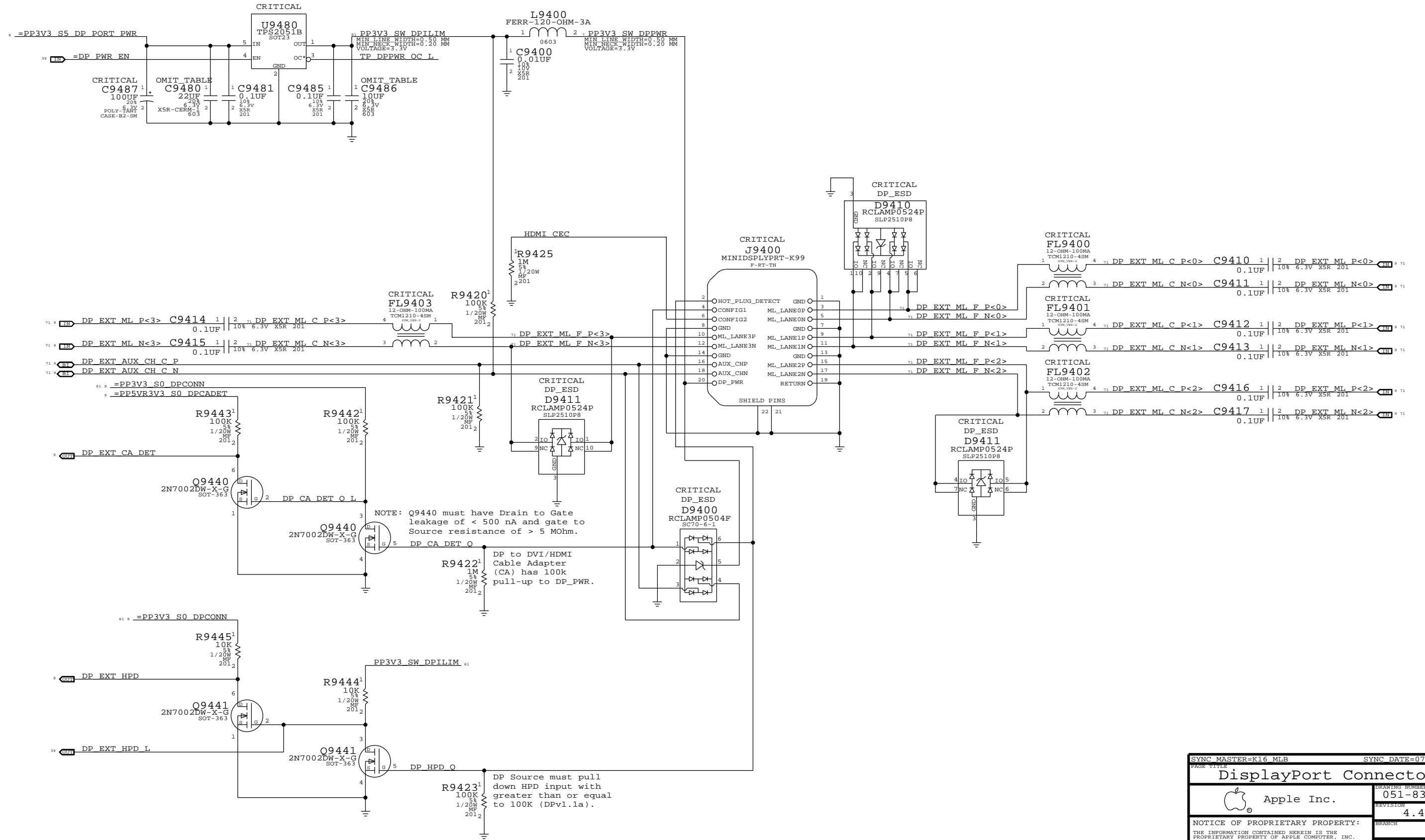
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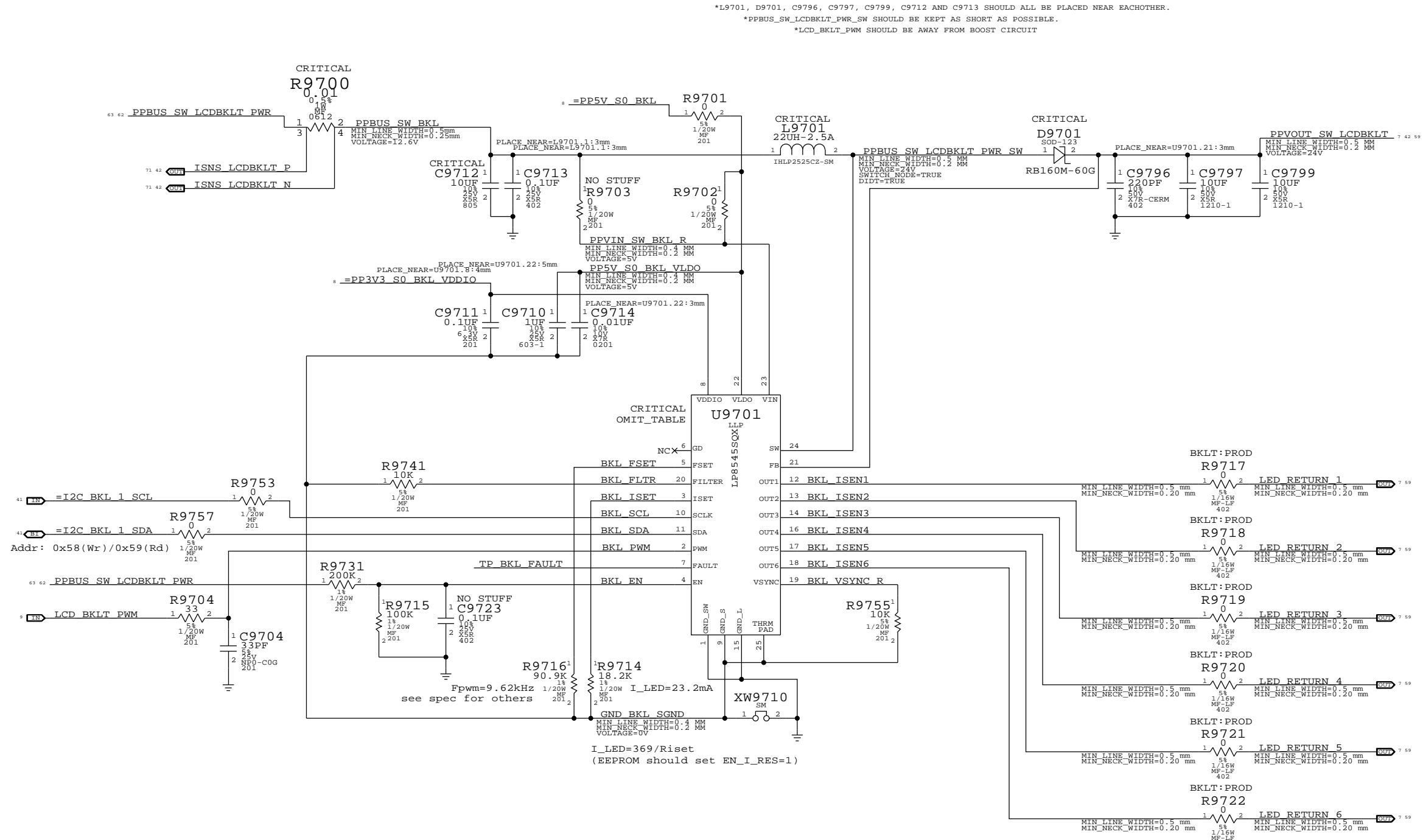


SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
External DisplayPort Support			
Apple Inc.		DRAWING NUMBER	SIZE
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Port Power Switch



SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
DisplayPort Connector			
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*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
 *PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
 *LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

FOR LP8543:
 STUFF R9741
 NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K16 MLB SYNC DATE=03/31/2010

LCD Backlight Driver

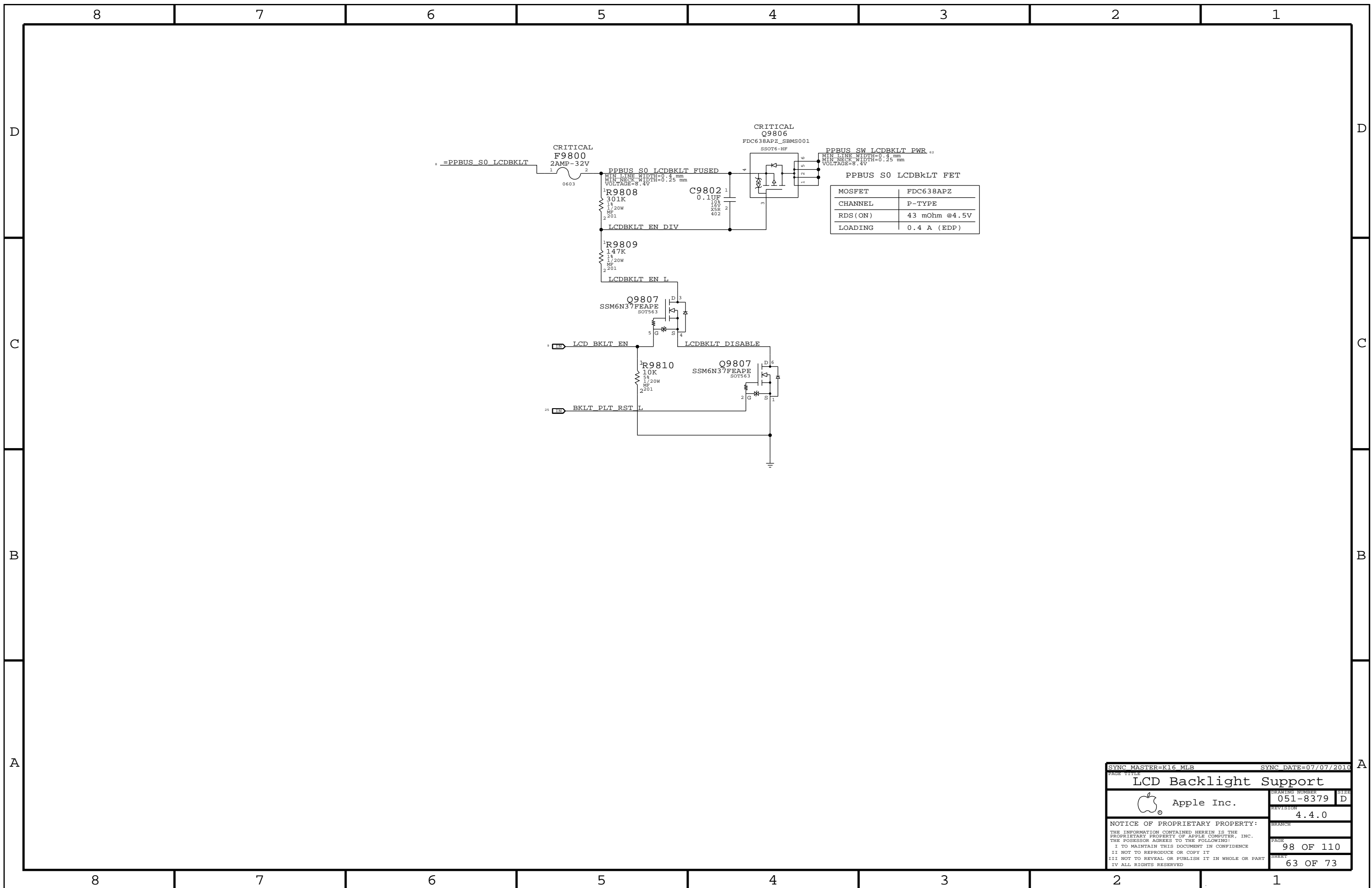
Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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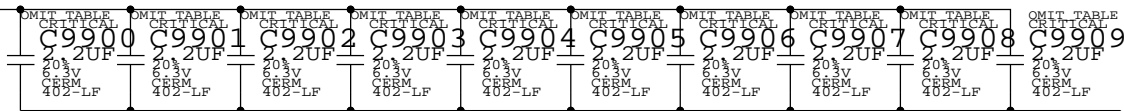
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PAGE TITLE LCD Backlight Support			
DRAWING NUMBER 051-8379		SIZE D	
REVISION 4.4.0		BRANCH	
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ADDITIONAL CPU VCORE HF DECOUPLING

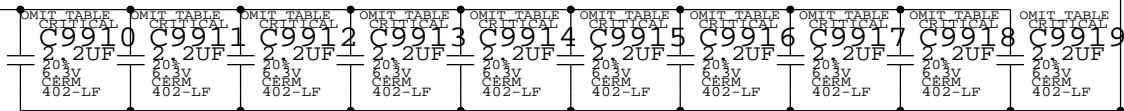
40x 1uF 0402

12 11 # =PPVCORE_S0_CPU

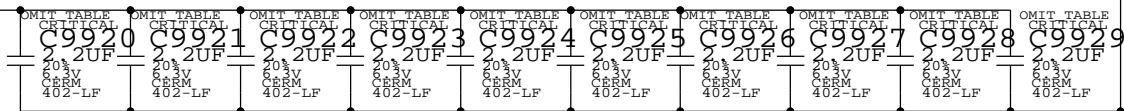
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



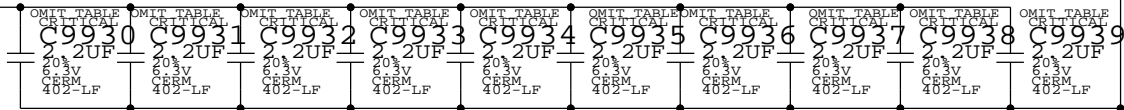
LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU



SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
Additional CPU/GPU Decoupling			
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCsense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE	ID
	PHYSICAL	SPACING			
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7	10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7	10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7	10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7	10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7	10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7	10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7	10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7	10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7	10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7	10 14
FSB_ADSTR0	FSB_55S	FSB_ADSTR	FSB ADSTR L<0>	7	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7	10 14
FSB_ADSTR1	FSB_55S	FSB_ADSTR	FSB ADSTR L<1>	7	10 14
FSB_1X	FSB_55S	FSB_1X	FSB ADS L	7	10 14
FSB_BREQ0_L	FSB_55S	FSB_1X	FSB BREQ0 L	10	14
FSB_1X	FSB_55S	FSB_1X	FSB BNR L	10	14
FSB_1X	FSB_55S	FSB_1X	FSB BPRI L	10	14
FSB_1X	FSB_55S	FSB_1X	FSB DBSY L	10	14
FSB_1X	FSB_55S	FSB_1X	FSB DEFER L	10	14
FSB_1X	FSB_55S	FSB_1X	FSB DRDY L	10	14
FSB_1X	FSB_55S	FSB_1X	FSB HIT L	7	10 14
FSB_1X	FSB_55S	FSB_1X	FSB HITM L	7	10 14
FSB_1X	FSB_55S	FSB_1X	FSB LOCK L	7	10 14
FSB_CPURST_L	FSB_55S	FSB_1X	FSB CPURST L	10	13 14
FSB_1X	FSB_55S	FSB_1X	FSB RS L<2..0>	10	14
FSB_1X	FSB_55S	FSB_1X	FSB TRDY L	10	14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU A20M L	10	14
CPU_BSEL	CPU_55S	CPU_AGTL	CPU BSEL<2..0>	9	10
CPU_FERR_L	CPU_55S	CPU_8MIL	CPU FERR L	10	14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU IGNE L	10	14
CPU_INIT_L	CPU_55S	CPU_AGTL	CPU INIT L	10	14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU INTR	10	14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU NMI	10	14
CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU PROCHOT L	10	14 39
CPU_PWRGD	CPU_55S	CPU_AGTL	CPU PWRGD	10	13 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU SMI L	10	14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU STPCLK L	10	14
PM_THERMTRIP_L	CPU_55S	CPU_8MIL	PM THERMTRIP L	10	14 39
FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB CPUSLP L	10	14
CPU_PROM_SB	CPU_55S	CPU_AGTL	CPU DPSLP L	10	14
CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU DPRSTP L	10	14 53
CPU_ASYNC	CPU_55S	CPU_AGTL	FSB DPWR L	10	14
FSB_CLK_CPUH	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10	14
FSB_CLK_CPUN	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10	14
FSB_CLK_ITP_P	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13	14
FSB_CLK_ITP_N	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13	14
FSB_CLK_MCP_P	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14	
FSB_CLK_MCP_N	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14	
CPU_IERR_L	CPU_55S	CPU_55S	CPU IERR L	10	
PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM DPRSLPVR	14	53
(See above)	CPU_55S	CPU_AGTL	IMVP DPRSLPVR		
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14	
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10	33
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10	
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10	
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10	33
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10	33
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10	33
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10	33
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10	33
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10	33
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10	33
(FSB_CPURST_I)	CPU_55S	CPU_ITP	XDP CPURST L	13	
	CPU_55S	CPU_8MIL	CPU VID<6..0>	11	12 53
	CPU_55S	CPU_8MIL	IMVP6 VID<6..0>	12	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11	53
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11	53
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	53	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	53	

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NV DG says 3x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 4x inner, 5x outer

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 CMD/CTRL signals should be matched within 150 ps.
 All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM A CKE<3..0>
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A CS L<3..0>
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A ODT<3..0>
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A A<15..0>
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A BA<2..0>
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A RAS L
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A CAS L
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A WE L
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DM<0>
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DM<1>
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DM<2>
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DM<3>
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DM<4>
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DM<5>
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DM<6>
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DM<7>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM B CKE<3..0>
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B CS L<3..0>
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B ODT<3..0>
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B A<15..0>
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B BA<2..0>
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B RAS L
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B CAS L
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B WE L
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DM<0>
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DM<1>
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DM<2>
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DM<3>
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DM<4>
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DM<5>
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DM<6>
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DM<7>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
PAGE TITLE			
Memory Constraints			
DRAWING NUMBER		SIZE	
051-8379		D	
REVISION		BRANCH	
4.4.0			
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
 NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max trace length: LVDS 10 inches, DP 8.5 inches.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.

Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_90D	PCIE	PEG R2D P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C N<15..0>
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX0 TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP TV DAC RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP TV DAC VREF
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 P<1..0>
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 N<1..0>
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 P
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 N
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP TMDS0 RSET
MCP_TMDS0_VPROBE			MCP TMDS0 VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C N
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMP	SATA_90D	SATA_TERMP	MCP SATA TERMP

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

MCP Constraints 1

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAIS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 38 40
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	7 19 38 40
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 38
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 40
USB_EXTN	USB_90D	USB	USB EXTN P	18 36
	USB_90D	USB	USB EXTN N	18 36
	USB_90D	USB	USB EXTN MUXED P	36 71
	USB_90D	USB	USB EXTN MUXED N	36 71
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXTD P	7 18 37
	USB_90D	USB	USB EXTD N	7 18 37
USB_CAMERA	USB_90D	USB	USB CAMERA P	7 18 37
	USB_90D	USB	USB CAMERA N	7 18 37
USB_BT	USB_90D	USB	USB BT P	7 18 34
	USB_90D	USB	USB BT N	7 18 34
USB_TPAD	USB_90D	USB	USB TPAD P	18 46 71
	USB_90D	USB	USB TPAD N	18 46 71
USB_IR	USB_90D	USB	USB IR P	
	USB_90D	USB	USB IR N	
USB_EXTR	USB_90D	USB	USB EXTB P	
	USB_90D	USB	USB EXTB N	
USB_T57	USB_90D	USB	USB T57 P	
	USB_90D	USB	USB T57 N	
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	9 18
	USB_90D	USB	USB SDCARD N	9 18
USB_WM	USB_90D	USB	USB WM P	
	USB_90D	USB	USB WM N	
MCP_USB_RBIAIS	MCP_USB_RBIAIS		MCP USB RBIAIS GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	19 41
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	19 41
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 41
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 41
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	7 19 37
	HDA_55S	HDA	HDA BIT CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST R L	19
	HDA_55S	HDA	HDA RST L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	7 19 37
	HDA_55S	HDA	HDA SDIN CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	7 19 37
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 38
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 40
	SPI_55S	SPI	SPI CLK	40
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 40
	SPI_55S	SPI	SPI MOSI	40
SPI_MISO	SPI_55S	SPI	SPI MISO	19 40
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 40
	SPI_55S	SPI	SPI CS0 L	40
	SPI_55S	SPI	SPI MLB CLK	40 47
	SPI_55S	SPI	SPI MLB MOSI	40 47
	SPI_55S	SPI	SPI MLB MISO	40 47
	SPI_55S	SPI	SPI MLB CS L	40 47
	SPI_55S	SPI	SPI ALT CLK	7 40
	SPI_55S	SPI	SPI ALT MOSI	7 40
	SPI_55S	SPI	SPI ALT MISO	7 40
	SPI_55S	SPI	SPI ALT CS L	7 40

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R
	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK
	ENET_MII_55S	ENET_MII	ENET_RXD R<3..0>
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL
	ENET_MII_55S	ENET_MII	ENET_RESET_L

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0>

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SD_DATA	SD_55S	SD_INTERFACE	SD D<4..0>
	SD_55S	SD_INTERFACE	SDCONN DATA<4..0>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>
SD_DATA_B	SD_55S	SD_INTERFACE	SD D<7..5>
	SD_55S	SD_INTERFACE	SDCONN DATA<7..5>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK
	SD_55S	SD_INTERFACE	SD_CLK R
	SD_55S	SD_INTERFACE	SDCONN_CLK
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD
	SD_55S	SD_INTERFACE	SDCONN_CMD
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
Ethernet Constraints			
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB 550	0300	SMBUS_SMC_A_S3_SCL	41
SMBUS_SMC_A_S3_SDA	SMB 550	0300	SMBUS_SMC_A_S3_SDA	41
SMBUS_SMC_B_S0_SCL	SMB 550	0300	SMBUS_SMC_B_S0_SCL	41
SMBUS_SMC_B_S0_SDA	SMB 550	0300	SMBUS_SMC_B_S0_SDA	41
SMBUS_SMC_O_S0_SCL	SMB 550	0300	SMBUS_SMC_O_S0_SCL	41
SMBUS_SMC_O_S0_SDA	SMB 550	0300	SMBUS_SMC_O_S0_SDA	41
SMBUS_SMC_BSA_SCL	SMB 550	0300	SMBUS_SMC_BSA_SCL	7 41
SMBUS_SMC_BSA_SDA	SMB 550	0300	SMBUS_SMC_BSA_SDA	7 41
SMBUS_SMC_MGMT_SCL	SMB 550	0300	SMBUS_SMC_MGMT_SCL	41
SMBUS_SMC_MGMT_SDA	SMB 550	0300	SMBUS_SMC_MGMT_SDA	41

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	50
	1TO1_DIFFPAIR		CHGR_CSI_N	50
	1TO1_DIFFPAIR		CHGR_CSI_R_P	50
	1TO1_DIFFPAIR		CHGR_CSI_R_N	50
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	50
	1TO1_DIFFPAIR		CHGR_CSO_N	50
	1TO1_DIFFPAIR		CHGR_CSO_R_P	43 50
	1TO1_DIFFPAIR		CHGR_CSO_R_N	43 50

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SYNC_MASTER=K16_MLB		SYNC_DATE=07/07/2010	
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S_OVERRIDE	*	ON LAYER?	=STANDARD_OVERRIDE	ON LAYER?	ON LAYER?	ON LAYER?	ON LAYER?

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	*	ON LAYER?	ON LAYER?	0.09 MM_OVERRIDE	5.8 MM_OVERRIDE	ON LAYER?	ON LAYER?
MCP_DV_COMP_OVERRIDE	TOP_OVERRIDE	ON LAYER?	ON LAYER?	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	ON LAYER?	ON LAYER?
MCP_MEM_COMP_OVERRIDE	TOP_OVERRIDE	ON LAYER?	ON LAYER?	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	ON LAYER?	ON LAYER?
MCP_MII_COMP_OVERRIDE	TOP_OVERRIDE	ON LAYER?	ON LAYER?	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	ON LAYER?	ON LAYER?
MCP_USB_RBIA_OVERRIDE	TOP_OVERRIDE	ON LAYER?	ON LAYER?	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	ON LAYER?	ON LAYER?
MCP_DV_COMP_OVERRIDE	*	ON LAYER?	ON LAYER?	0.25 MM_OVERRIDE	250 MIL_OVERRIDE	ON LAYER?	ON LAYER?

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
(USB_EXT_A)	USB_90D	USB	USB_EXT_A MUXED P
(USB_EXT_A)	USB_90D	USB	USB_EXT_A MUXED N
(USB_EXT_A)	USB_90D	USB	USB LT1 P
(USB_EXT_A)	USB_90D	USB	USB LT1 N
(USB_TPAD)	USB_90D	USB	USB TPAD P
(USB_TPAD)	USB_90D	USB	USB TPAD N
(USB_TPAD)	USB_90D	USB	USB TPAD CONN P
(USB_TPAD)	USB_90D	USB	USB TPAD CONN N
(SMBUS_SMC_MNET_SDA)	SMB_55S	SMB	I2C SMC SMS SDA R
(SMBUS_SMC_MNET_SCL)	SMB_55S	SMB	I2C SMC SMS SCL R
	SMB_55S	SMB	I2C TCON SCL
	SMB_55S	SMB	I2C TCON SDA
	SMB_55S	SMB	I2C TCON SCL CONN
	SMB_55S	SMB	I2C TCON SDA CONN

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
	DP_90D	DISPLAYPORT	DP INT ML P<1..0>
	DP_90D	DISPLAYPORT	DP INT ML N<1..0>
	DP_90D	DISPLAYPORT	DP INT ML C P<1..0>
	DP_90D	DISPLAYPORT	DP INT ML C N<1..0>
	DP_90D	DISPLAYPORT	DP INT ML F P<1..0>
	DP_90D	DISPLAYPORT	DP INT ML F N<1..0>
	DP_90D	DISPLAYPORT	DP INT AUX CH C P
	DP_90D	DISPLAYPORT	DP INT AUX CH C N
	DP_90D	DISPLAYPORT	DP INT AUX CH P
	DP_90D	DISPLAYPORT	DP INT AUX CH N
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML N<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0>
	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0>
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P
	DP_90D	DISPLAYPORT	DP EXT AUX CH C N

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
	THERM_1T01_55S	THERM	DRAMTHMSNS D2 P
	THERM_1T01_55S	THERM	DRAMTHMSNS D2 N
	THERM_1T01_55S	THERM	CPU_THERMD P
	THERM_1T01_55S	THERM	CPU_THERMD N
	THERM_1T01_55S	THERM	MLBR_THMDIODE P
	THERM_1T01_55S	THERM	MLBR_THMDIODE N
	THERM_1T01_55S	THERM	MCP_THMDIODE P
	THERM_1T01_55S	THERM	MCP_THMDIODE N
	THERM_1T01_55S	THERM	ISNS_1V5_S3 P
	THERM_1T01_55S	THERM	ISNS_1V5_S3 N
	THERM_1T01_55S	THERM	ISNS_AIRPORT P
	THERM_1T01_55S	THERM	ISNS_AIRPORT N
	THERM_1T01_55S	THERM	ISNS_CSREG P
	THERM_1T01_55S	THERM	ISNS_CSREG N
	THERM_1T01_55S	THERM	ISNS_HDD P
	THERM_1T01_55S	THERM	ISNS_HDD N
	THERM_1T01_55S	THERM	ISNS_LCDBKLT P
	THERM_1T01_55S	THERM	ISNS_LCDBKLT N
	THERM_1T01_55S	THERM	CPUVTT50_CS P
	THERM_1T01_55S	THERM	CPUVTT50_CS N
	THERM_1T01_55S	THERM	IMVP6_CS P
	THERM_1T01_55S	THERM	IMVP6_CS N
	THERM_1T01_55S	THERM	IMVP6_CS_R P
	THERM_1T01_55S	THERM	IMVP6_CS_R N
	THERM_1T01_55S	THERM	CPU_VTTSENSE P
	THERM_1T01_55S	THERM	CPU_VTTSENSE N
	THERM_1T01_55S	THERM	MCPCORES0_VSEN P
	THERM_1T01_55S	THERM	MCPCORES0_VSEN N
	MEM_POWER		PP1V5R1V35_S3
	SB_POWER		PP3V3_S5
	SB_POWER		PP3V3_S0
	SB_POWER		PP1V5_S0
	GND		GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
	DIFFPAIR	AUDIO	SPKRAMP_INR P
	DIFFPAIR	AUDIO	SPKRAMP_INR N
	DIFFPAIR	AUDIO	MAX98300_R P
	DIFFPAIR	AUDIO	MAX98300_R N

SYNC MASTER=K16_MLB SYNC DATE=07/07/2010

PAGE TITLE: K16/K99 Specific Constraints

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3, ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4, ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP, BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3, ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4, ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3, ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

SYNC MASTER=K16 MLB		SYNC DATE=07/07/2010	
K99 RULE DEFINITIONS			
		DRAWING NUMBER	051-8379
		REVISION	4.4.0
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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C1203,C1240	CRITICAL	SS_CAP_1UF	138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C1203,C1240	CRITICAL	MU_CAP_1UF	138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C1203,C1240	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1203,C1240,C1241,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1200	CRITICAL	SS_CAP_10UF	138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1200	CRITICAL	MU_CAP_10UF	138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1200	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209,C1210	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209,C1210	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209,C1210	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209,C1210	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209,C1210	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209,C1210	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

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TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	SS_CAP_22UF	138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	MU_CAP_22UF	138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	TY_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	SS_CAP_22UF	138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	MU_CAP_22UF	138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213	CRITICAL	TY_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215	CRITICAL	SS_CAP_22UF	138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215	CRITICAL	MU_CAP_22UF	138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215	CRITICAL	TY_CAP_22UF

SYNC MASTER=K16 MLB SYNC DATE=07/07/2010

Acoustic Cap BOM Config Tables

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