

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# SCHEM, CORNHOLIO, K19

a.k.a. K19i 4/24/2009 - PVT -

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	N/A	N/A
3	Power Block Diagram	DRAGON	03/13/2008
4	BOM Configuration	N/A	N/A
5	Revision History	N/A	N/A
6	Functional / ICT Test	N/A	N/A
7	Power Aliases	N/A	N/A
8	Signal Aliases	WFERRY_K19i	01/13/2009
9	CPU FSB	K24_MLB	02/05/2009
10	CPU Power & Ground	K24_MLB	02/05/2009
11	CPU Decoupling	K24_MLB	02/05/2009
12	eXtended Debug Port (MiniXDP)	K19_MLB	02/05/2009
13	MCP CPU Interface	T18_MLB	02/05/2009
14	MCP Memory Interface	T18_MLB	02/05/2009
15	MCP Memory Misc	T18_MLB	02/05/2009
16	MCP PCIe Interfaces	T18_MLB	02/05/2009
17	MCP Ethernet & Graphics	T18_MLB	02/05/2009
18	MCP PCI & LPC	T18_MLB	02/05/2009
19	MCP SATA & USB	T18_MLB	02/05/2009
20	MCP HDA & MISC	T18_MLB	02/05/2009
21	MCP Power & Ground	T18_MLB	02/05/2009
22	MCP Standard Decoupling	T18_MLB	02/05/2009
23	MCP Graphics Support	K19_MLB	02/05/2009
24	SB Misc	WFERRY_K19i	01/06/2009
25	FSB/DDR3 Vref Margining	K24_MLB	02/05/2009
26	DDR3 SO-DIMM Connector A	K19_MLB	02/05/2009
27	DDR3 SO-DIMM Connector B	K19_MLB	02/05/2009
28	DDR3 Support	T18_MLB	02/05/2009
29	Right Clutch Connector	K19_MLB	03/04/2009
30	SECUREDIGITAL CARD READER	K19_MLB	03/23/2009
31	Ethernet PHY (RTL8211CL)	(K19_MLB)	02/05/2009
32	Ethernet & AirPort Support	K19_MLB	02/05/2009
33	Ethernet Connector	K19_MLB	03/13/2009
34	FireWire LLC/PHY (FW643E)	T18_MLB	02/05/2009
35	FireWire Port Power	K19_MLB	03/18/2009
36	FireWire Ports	K19_MLB	02/05/2009
37	SATA Connectors	K19_MLB	03/23/2009
38	External USB Connectors	K19_MLB	02/05/2009
39	Front Flex Support	K19_MLB	02/05/2009
40	SMC	T18_MLB	02/05/2009
41	SMC Support	(K19_MLB)	(11/25/2008)
42	LPC+SPI Debug Connector	K19_MLB	02/05/2009

Page	Contents	Sync	Date
43	K19i SMBus Connections	WFERRY_K19i	12/12/2008
44	VOLTAGE SENSING	K24_MLB	02/05/2009
45	Current Sensing	WFERRY_K19i	12/16/2008
46	Thermal Sensors	K24_MLB	02/05/2009
47	Fan	K24_MLB	02/05/2009
48	WELLSRING 1	K24_MLB	02/05/2009
49	WELLSRING 2	K24_MLB	02/25/2009
50	Sudden Motion Sensor (SMS)	K19_MLB	02/05/2009
51	DEBUG SENSORS AND ADC	K19_MLB	03/25/2009
52	SPI ROM	K19_MLB	02/05/2009
53	AUDIO: CODEC/REGULATOR	K19_MLB	03/17/2009
54	AUDIO: LINE INPUT FILTER	K19_MLB	03/02/2009
55	AUDIO: HEADPHONE FILTER	K19_MLB	02/05/2009
56	AUDIO:SPEAKER AMP	K19_MLB	02/05/2009
57	AUDIO: JACKS	CASEYHARDY_K19	03/20/2009
58	AUDIO: JACK TRANSLATORS	K19_MLB	03/17/2009
59	DC-In & Battery Connectors	K19_MLB	03/18/2009
60	PBus Supply & Battery Charger	K19_MLB	03/18/2009
61	IMVP6 CPU VCore Regulator	K19_MLB	02/05/2009
62	5V / 3.3V Power Supply	WFERRY_K19i	01/13/2009
63	1.5V DDR3 Supply	K19_MLB	02/04/2009
64	MCP CORE REGULATOR	K19_MLB	02/03/2009
65	CPU VTT Power Supply	(K19_MLB)	(12/05/2008)
66	MISC POWER SUPPLIES	K24_MLB	02/25/2009
67	POWER SEQUENCING	K24_MLB	02/05/2009
68	POWER FETS	K24_MLB	03/12/2009
69	LVDS Display Connector	K19_MLB	02/05/2009
70	DISPLAYPORT SUPPORT	K24_MLB	12/19/2008
71	DisplayPort Connector	K19_MLB	02/05/2009
72	LCD BACKLIGHT DRIVER	K19_MLB	02/10/2009
73	LCD Backlight Support	K24_MLB	03/16/2009
74	LCD Backlight Driver (MC34845)	VEMURI_K19i	02/09/2009
75	CPU/FSB Constraints	T18_MLB	02/05/2009
76	Memory Constraints	T18_MLB	02/05/2009
77	MCP Constraints 1	T18_MLB	02/05/2009
78	MCP Constraints 2	T18_MLB	02/05/2009
79	Ethernet Constraints	T18_MLB	02/05/2009
80	FireWire Constraints	T18_MLB	02/05/2009
81	SMC Constraints	T18_MLB	02/05/2009
82	K19i Specific Constraints	WFERRY_K19i	01/08/2009
83	K19i PCB Rule Definitions	WFERRY_K19i	12/12/2008

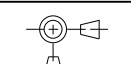
Integration Issues to be Resolved

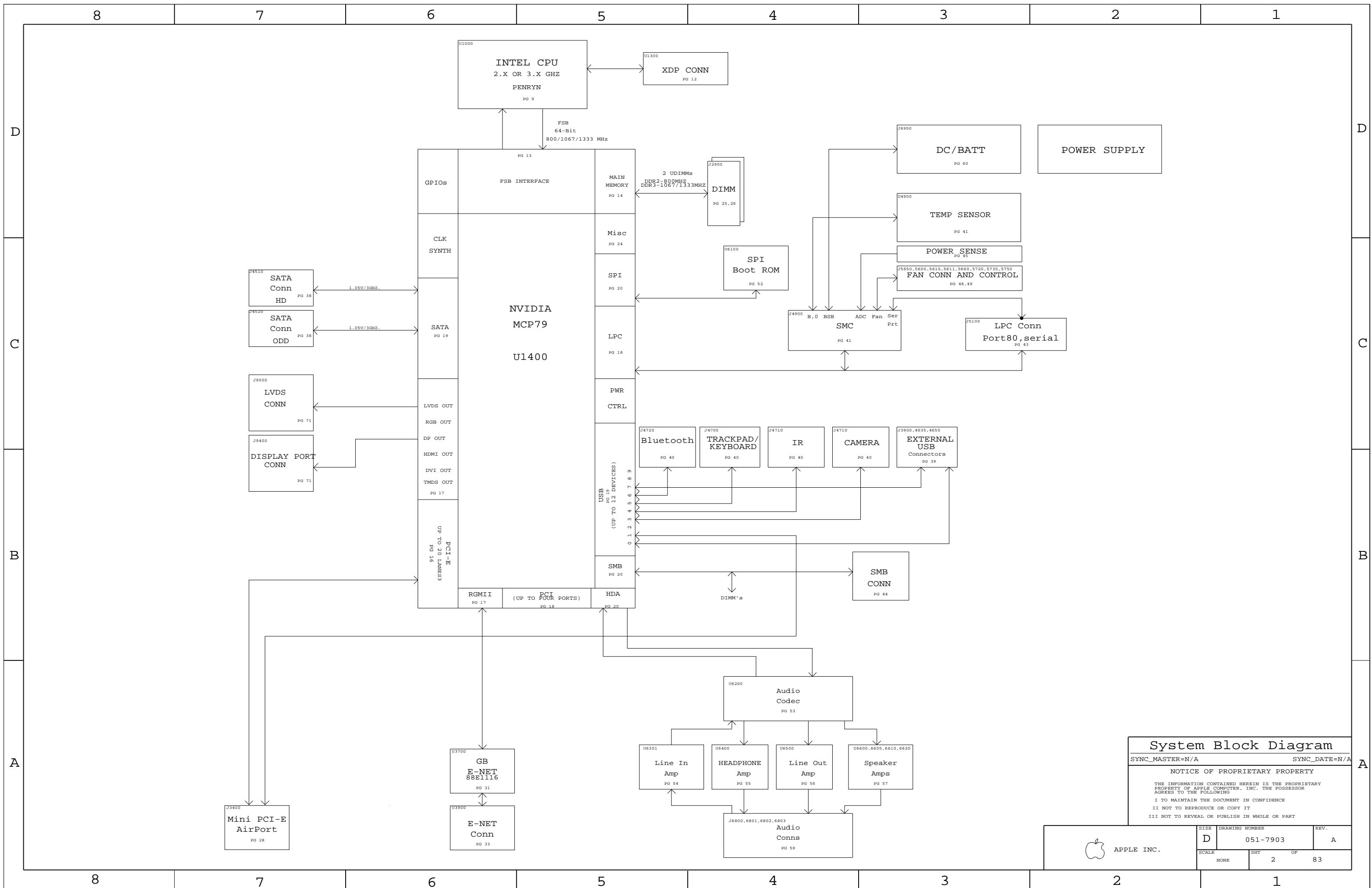
JTAG MCP TDO  
 JTAG MCP TDO  
 Should come J1300 net that JTAG level after is gone

# ALIASES RESOLVED

## Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7903	1	SCHEM, CORNHOLIO, K19	SCH	CRITICAL	
820-2533	1	PCBF,MLB IG,K19	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS		METRIC		APPLE INC.	
XX :	_____	DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX :	_____	ENG APPD	MFG APPD		
X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D DRAWING NUMBER 051-7903 REV. A	
				SHT 1 OF 83	



### System Block Diagram

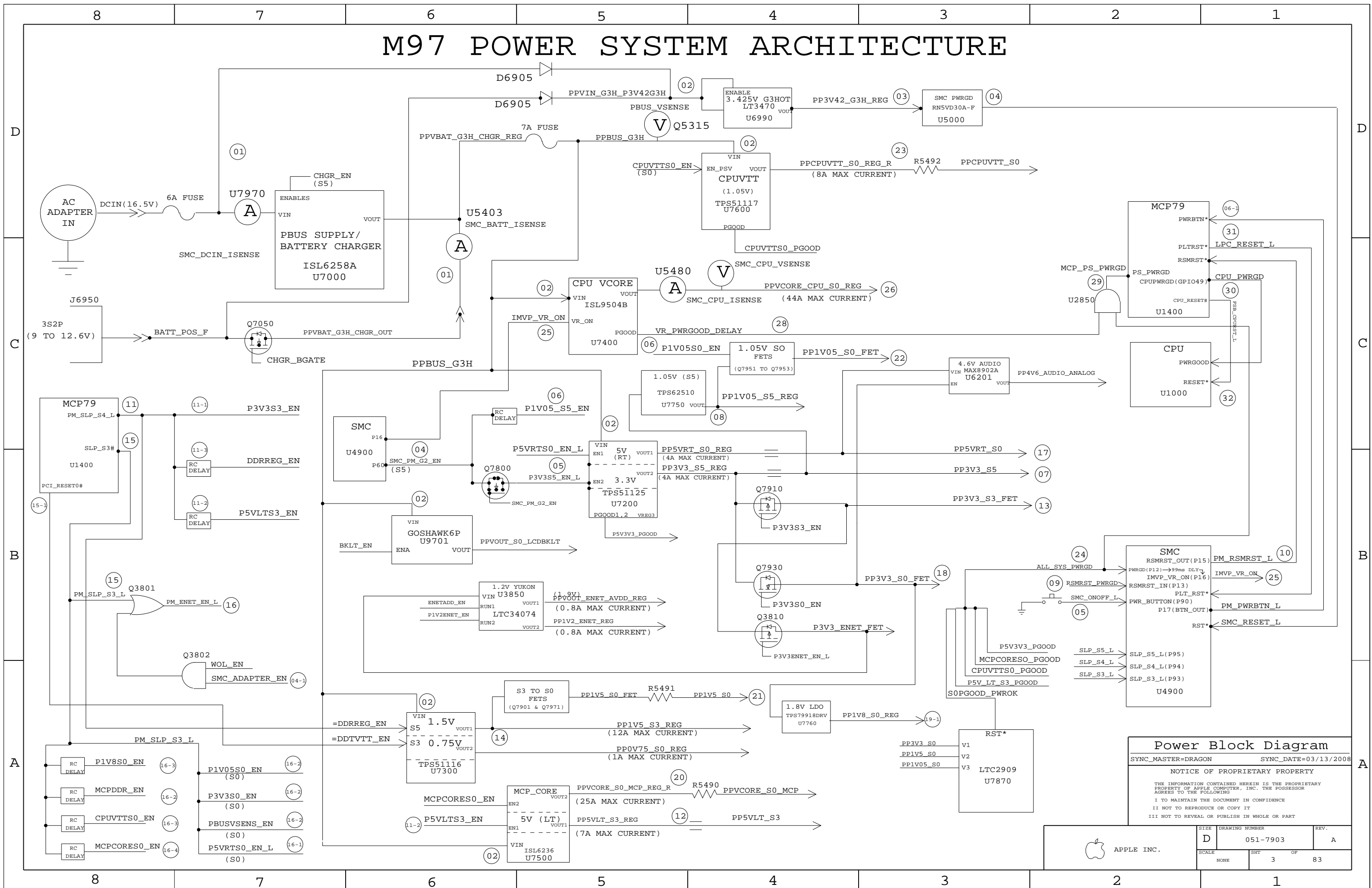
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NONE	2	83	

# M97 POWER SYSTEM ARCHITECTURE



**Power Block Diagram**  
 SYNC\_MASTER=DRAGON SYNC\_DATE=03/13/2008

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BOM Variant

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9977	PCBA, CORNHOLIO, MLB, K19I	K19_COMMON, CPU_2_53GHZ, EEE_6Z9
085-0737	K19I MLB DEVELOPMENT	K19_DEVEL_PVT

Bar Code Label / EEE #

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6Z9]	CRITICAL	EEE_6Z9

BOM Groups

BOM GROUP	BOM OPTIONS
K19_COMMON	COMMON, ALTERNATE, K19_MCP, K19_MISC, K19_DEBUG_PVT, K19_PROGPARTS
K19_MCP	MCP_B03, BOOT_MODE_USER
K19_MISC	DP_ESD, EXTRACT_BUFF, ISL6258A, K19I, KB_BL, MIKEY, LDO_YES
K19_PROGPARTS	BOOTROM_PROG, SMC_PROG, IR_PROG, WELLSRING_PROG
K19_DEVEL_ENG	BMON_ENG, DEBUG_ADC, XDP_CONN, LPCPLUS, VREFMRGN, BKLT_FS
K19_DEVEL_PVT	LPCPLUS
K19_DEBUG_ENG	DEVEL_BOM, SMC_DEBUG_YES, XDP
K19_DEBUG_PVT	DEVEL_BOM, BMON_PROD, SMC_DEBUG_YES, XDP, NO_VREFMRGN
K19_DEBUG_PROD	BMON_PROD, SMC_DEBUG_YES, XDP, LPCPLUS_NOT, NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3693	1	PDC, SLGE3, PRQ, 2.00, 25W, 1066, R0, 3M, BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC, SLGE2, PRQ, 2.26, 25W, 1066, R0, 3M, BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3680	1	PDC, LGDZ, PRQ, 2.40, 25W, 1066, R0, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3640	1	PDC, SL3BX, PRQ, 2.5, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_5GHZ
337S3756	1	PDC, SLCFG, PRQ, 2.53, 25W, 1066, R0, 3M, BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3641	1	PDC, SLB43, PRQ, 2.8, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_8GHZ
338S0710	1	IC, MCP79MKT-B3, 35x35MM, BGA1437	U1400	CRITICAL	MCP_B03
338S0694	1	IC, RTL8251CA-VB-GR, GIGE TRANSCEIVER, 48P	U3700	CRITICAL	
338S0654	1	IC-FW643-E, 1394B PHY/ORCI LINK/PCI-E, 12	U4100	CRITICAL	

Programmable Parts

338S0563	1	IC, SMC, HS8/2117, 9X9MM, TLF, HF	U4900	CRITICAL	SMC_BLANK
341S2460	1	IC, PRGRM, SMC EXTERNAL, K19I	U4900	CRITICAL	SMC_PROG
335S0610	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2458	1	IC, PRGRM, UNLOCK, K19I	U6100	CRITICAL	BOOTROM_PROG
338S0633	1	IC, CYPRS, CY7C63803-LQXC, 4X4MM, USB, 24-QFN	U4800	CRITICAL	IR_BLANK
341S2384	1	IR, ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	IR_PROG
337S2983	1	IC, PSOC+ W/ USB, 56 PIN, MLP, CY8C24794	U5701	CRITICAL	WELLSRING_BLANK
341S2503	1	IC, TP PSOC, M97, M98	U5701	CRITICAL	WELLSRING_PROG

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0737	1	K19I MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
152S0968	152S0966		ALL	Maglayer alt to Delta
128S0220	128S0262		ALL	KEMET alt to SANYO
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE

BOM Configuration

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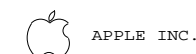
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D	051-7903	A
SCALE	SHT	OF
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Revision History

D

D

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C


B

B

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A

Revision History		
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NONE	5	83	

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

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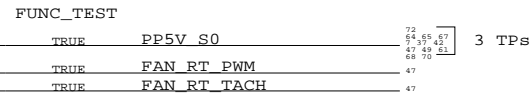
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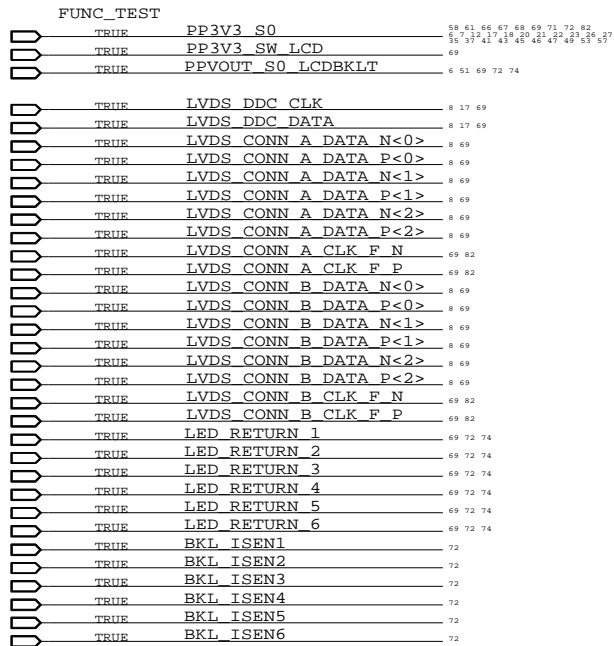
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# Functional Test Points

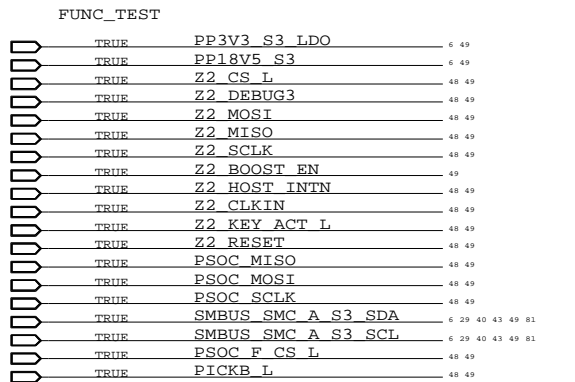
## Fan Connectors



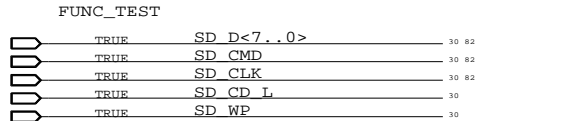
## LVDS Connector



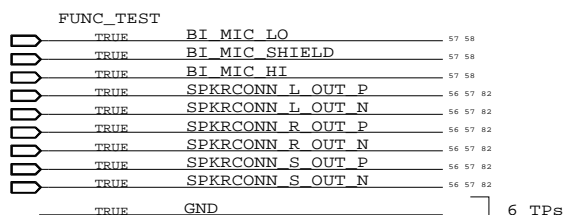
## IPD Flex Connector



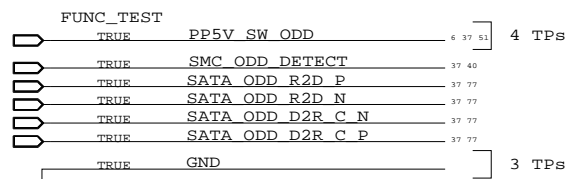
## SD Card Connector



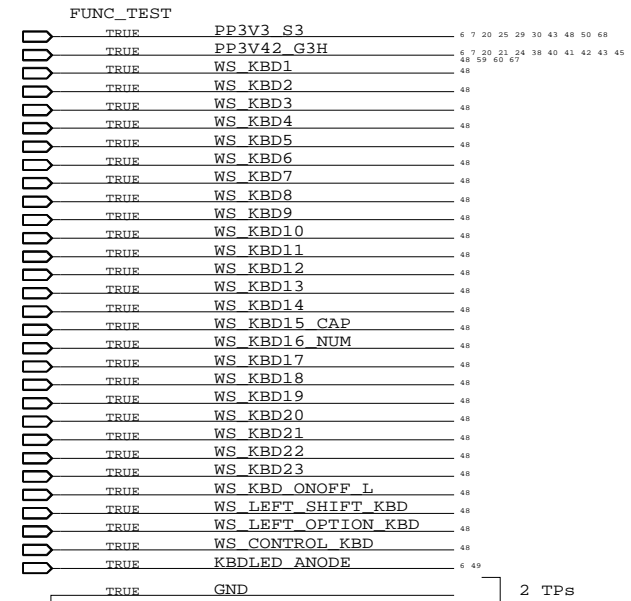
## Speaker Connectors



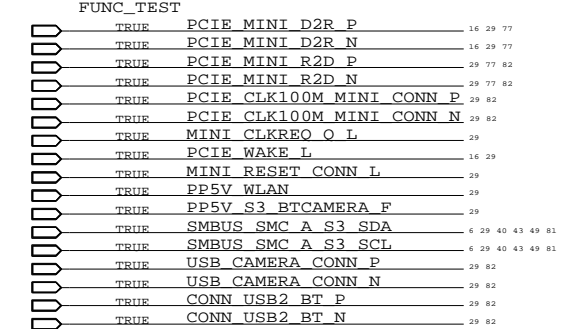
## SATA ODD Connectors



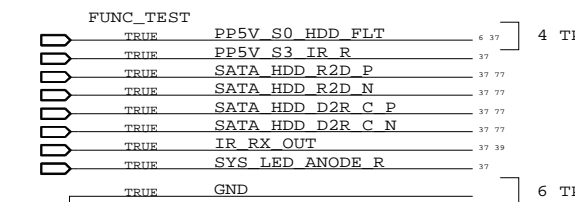
## Keyboard Connector



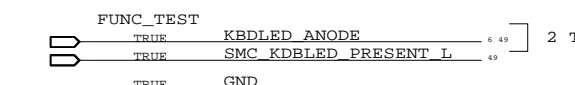
## Airport/BT/Camera Conn.



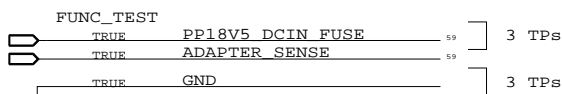
## SATA HDD Connector



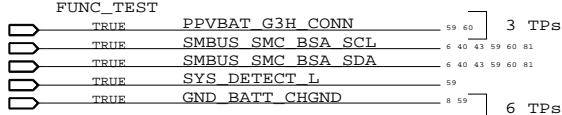
## KBD Backlight Conn.



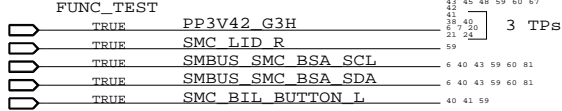
## DC Power Connector



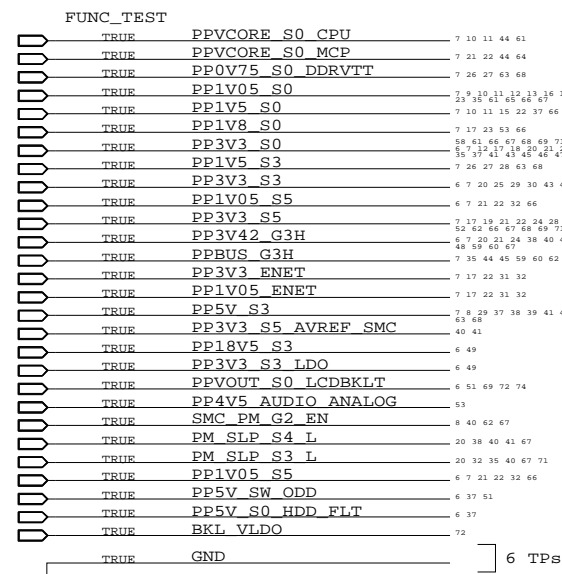
## Battery Connector



## BIL Connector



## Power Nets



## ICT Test Points

NO_TEST	NO_TEST	NO_TEST
NC_AUD_LO1_N_L	NC_AUD_LO1_P_L	MAKE_BASE=TRUE TRUE
NC_USB_10N	NC_USB_10P	MAKE_BASE=TRUE TRUE
NC_ENET_INTR_L	NC_ENET_INTR_P_L	MAKE_BASE=TRUE TRUE
NC_ISSP_SCLK_P1_1	NC_ISSP_SCLK_P1_0	MAKE_BASE=TRUE TRUE
NC_LCDBKLT_FAIL	NC_LCDBKLT_FAIL	MAKE_BASE=TRUE TRUE
NC_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE TRUE
TP_MEM_A_CKE<3..2>	NC_MEM_A_CKE<3..2>	MAKE_BASE=TRUE TRUE
NC_MEM_A_CLK2N	NC_MEM_A_CLK3N	MAKE_BASE=TRUE TRUE
NC_MEM_A_CLK3P	NC_MEM_A_CLK4P	MAKE_BASE=TRUE TRUE
NC_MEM_A_CLK4P	NC_MEM_A_CS_L<3>	MAKE_BASE=TRUE TRUE
TP_MEM_A_ODT<3..2>	NC_MEM_A_ODT<3..2>	MAKE_BASE=TRUE TRUE
NC_MEM_B_CKE<2>	NC_MEM_B_CLK3P	MAKE_BASE=TRUE TRUE
NC_MEM_B_CLK4N	NC_MEM_B_CLK4P	MAKE_BASE=TRUE TRUE
NC_MEM_B_CLK4P	NC_MEM_B_CLK5N	MAKE_BASE=TRUE TRUE
NC_MEM_B_CLK5N	NC_MEM_B_ODT<2>	MAKE_BASE=TRUE TRUE
NC_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE TRUE
NC_P7_7	NC_P7_7	MAKE_BASE=TRUE TRUE
TP_PCI_AD<31..8>	NC_PCI_AD<31..8>	MAKE_BASE=TRUE TRUE
TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE TRUE
NC_PCI_CLK0	NC_PCI_CLK1	MAKE_BASE=TRUE TRUE
NC_PCI_DEVSEL_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE TRUE
NC_PCI_FRAME_L	NC_PCI_GNT0_L	MAKE_BASE=TRUE TRUE
NC_PCI_GNT0_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE TRUE
NC_PCI_INTX_L	NC_PCI_INTW_L	MAKE_BASE=TRUE TRUE
NC_PCI_INTW_L	NC_PCI_INTX_L	MAKE_BASE=TRUE TRUE
NC_PCI_INTZ_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE TRUE
NC_PCI_IRDY_L	NC_PCI_PERR_L	MAKE_BASE=TRUE TRUE
NC_PCI_PERR_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE TRUE
NC_PCI_RESET1_L	NC_PCI_SERR_L	MAKE_BASE=TRUE TRUE
NC_PCI_SERR_L	NC_PCI_STOP_L	MAKE_BASE=TRUE TRUE
NC_PCI_STOP_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE TRUE
NC_PCI_TRDY_L	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE TRUE
NC_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE TRUE
NC_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE TRUE
NC_PCIE_CLK100M_PE6P	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE TRUE
NC_PCIE_PE4_D2RN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE TRUE
NC_PCIE_PE4_R2D_CN	NC_PCIE_PRSENT_L	MAKE_BASE=TRUE TRUE
NC_PCIE_PRSENT_L	NC_PSOC_P1_3	MAKE_BASE=TRUE TRUE
NC_PSOC_P1_3	NC_PSOC_SDA	MAKE_BASE=TRUE TRUE
NC_PSOC_SDA	NC_SATA_C_D2RP	MAKE_BASE=TRUE TRUE
NC_SATA_C_D2RP	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE TRUE
NC_SATA_C_R2D_CN	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE TRUE
NC_SATA_C_R2D_CP	NC_SATA_D_D2RN	MAKE_BASE=TRUE TRUE
NC_SATA_D_D2RN	NC_SATA_D_D2RP	MAKE_BASE=TRUE TRUE
NC_SATA_D_D2RP	NC_SB_A20GATE	MAKE_BASE=TRUE TRUE
NC_SB_A20GATE		

Note. NO\_TEST properties are also on page 9, 26, 43, 50

## Functional / ICT Test

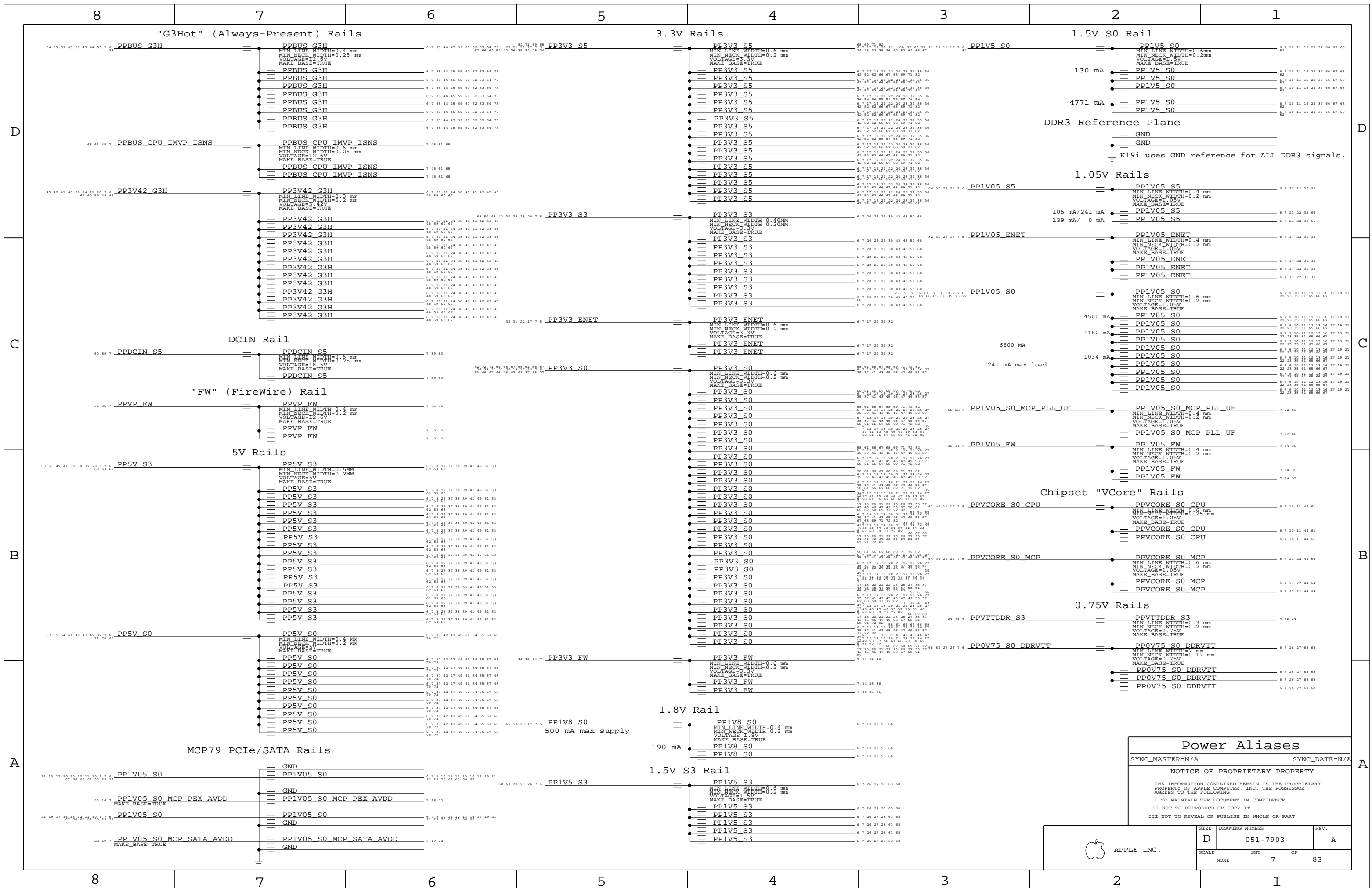
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NONE	6	83



Power Aliases		
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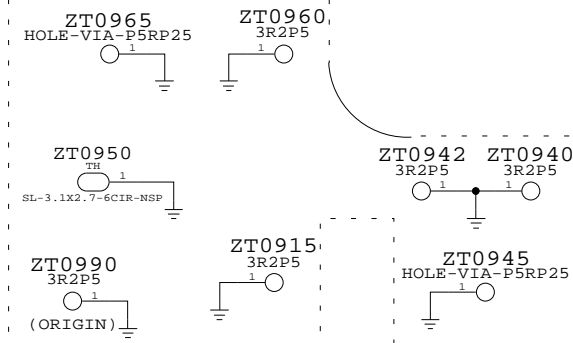
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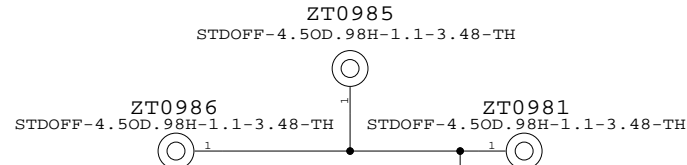
APPLE INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
NONE	7		83

### Board Mounting Holes

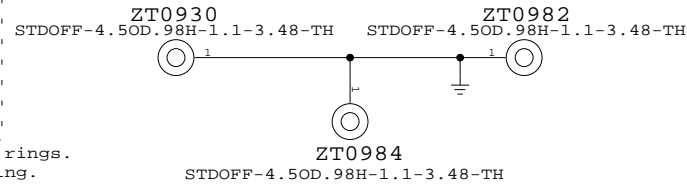
(Not to scale)



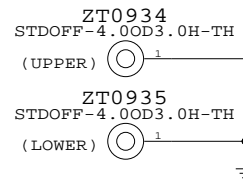
### CPU Thermal Module Holes



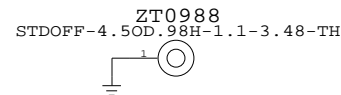
### MCP Thermal Module Holes



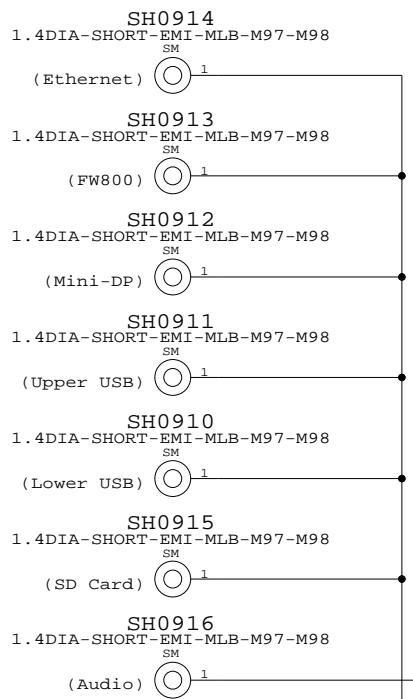
### Left Speaker Standoffs



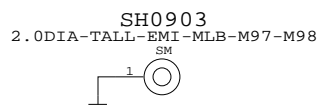
### Fan Screw Hole



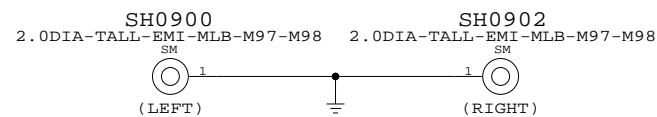
### I/O Row Pogos



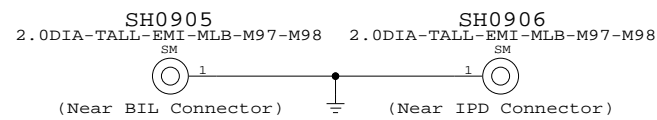
### CPU Pogo



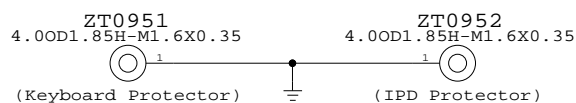
### SO-DIMM Pogos



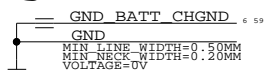
### Other Board Pogos



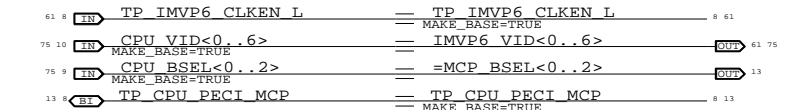
### Bosses



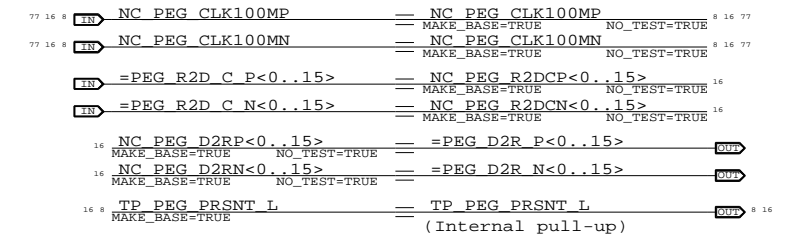
### Digital Ground



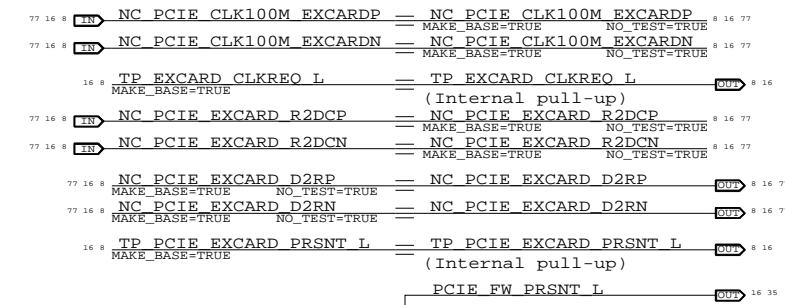
### CPU Signals



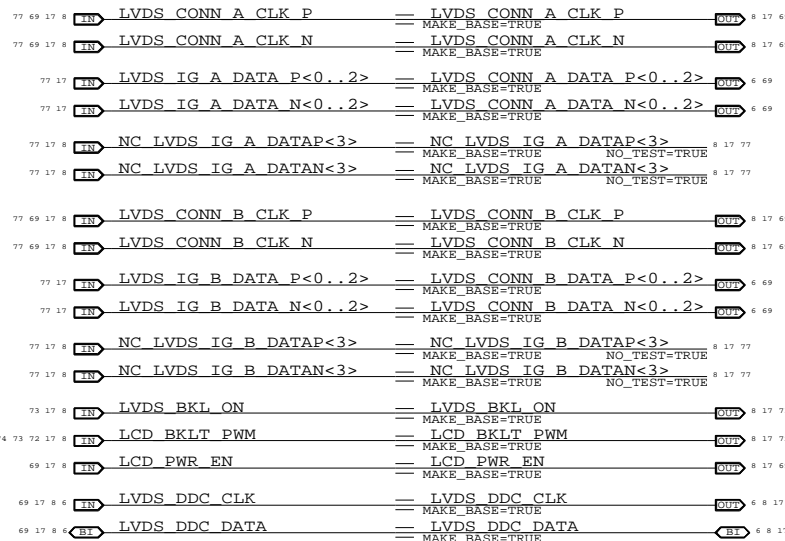
### PEG Signals



### PCIe Signals



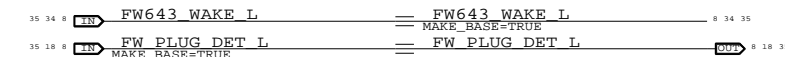
### LVDS Signals



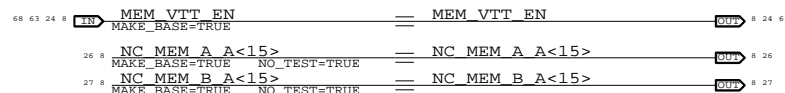
### DisplayPort Signals

(Aliases on page70.csa)

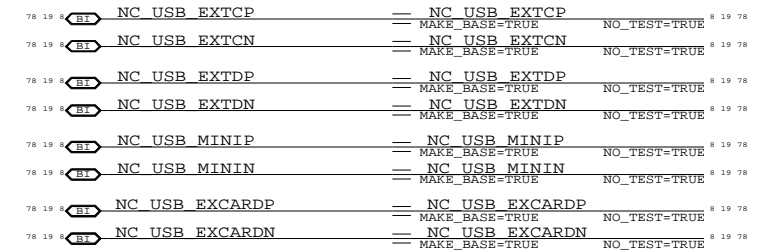
### FireWire Signals



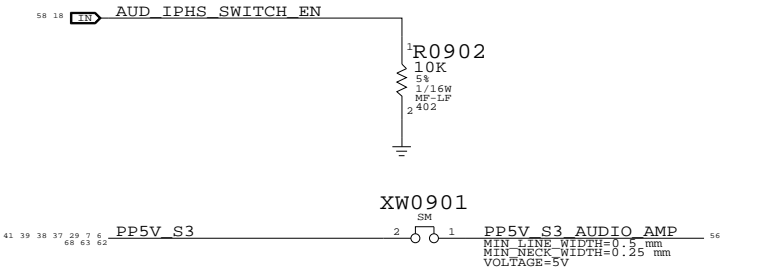
### Memory Signals



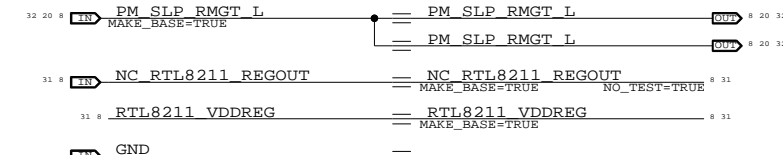
### USB Signals



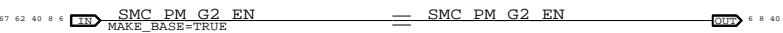
### Audio Signals



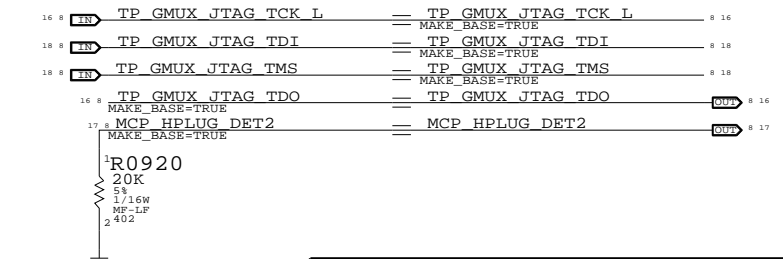
### Ethernet Signals



### Power Signals



### GMUX Signals



### Signal Aliases

SYNC\_MASTER=WFERRY\_K19I SYNC\_DATE=01/13/2009

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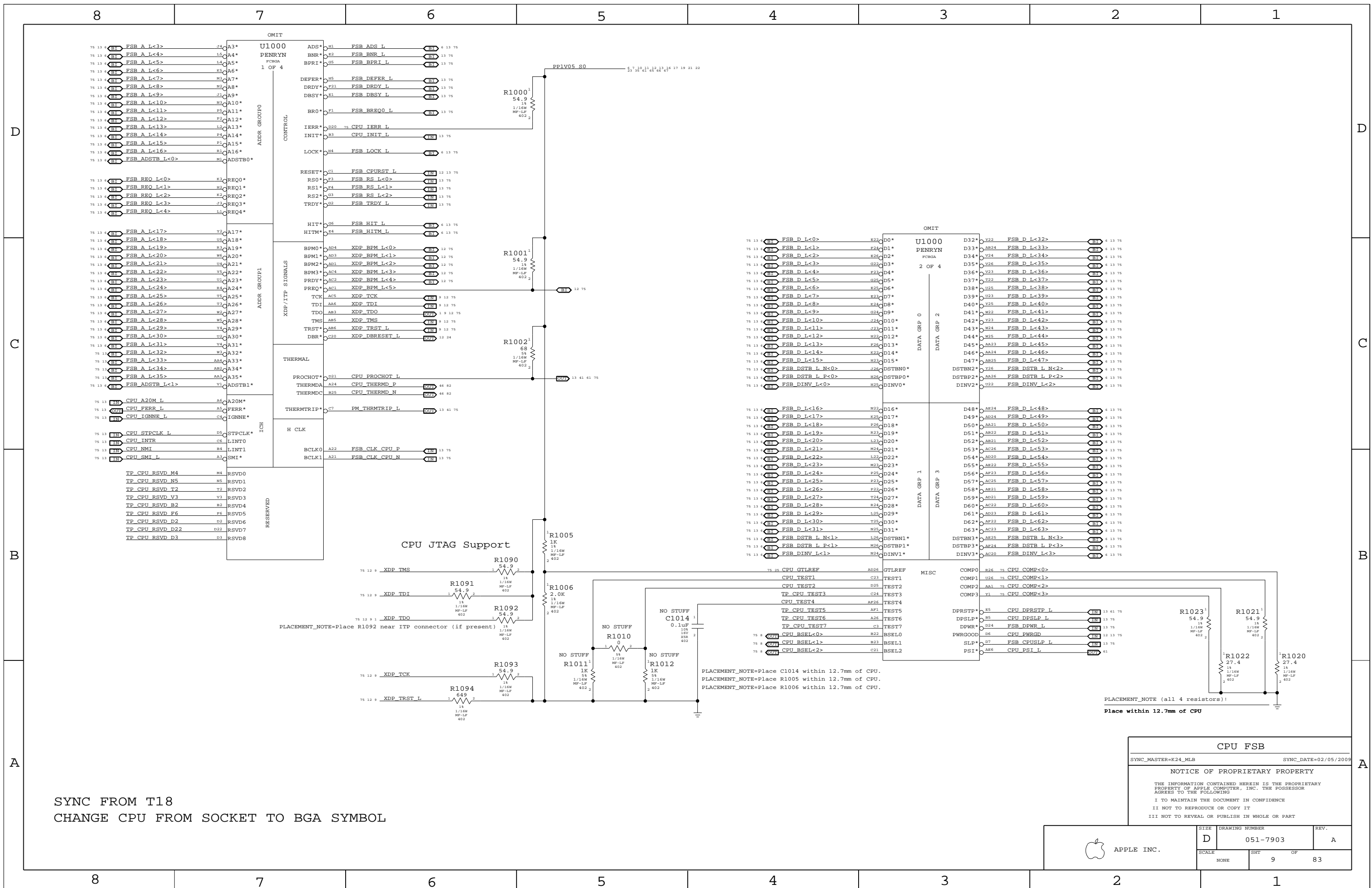
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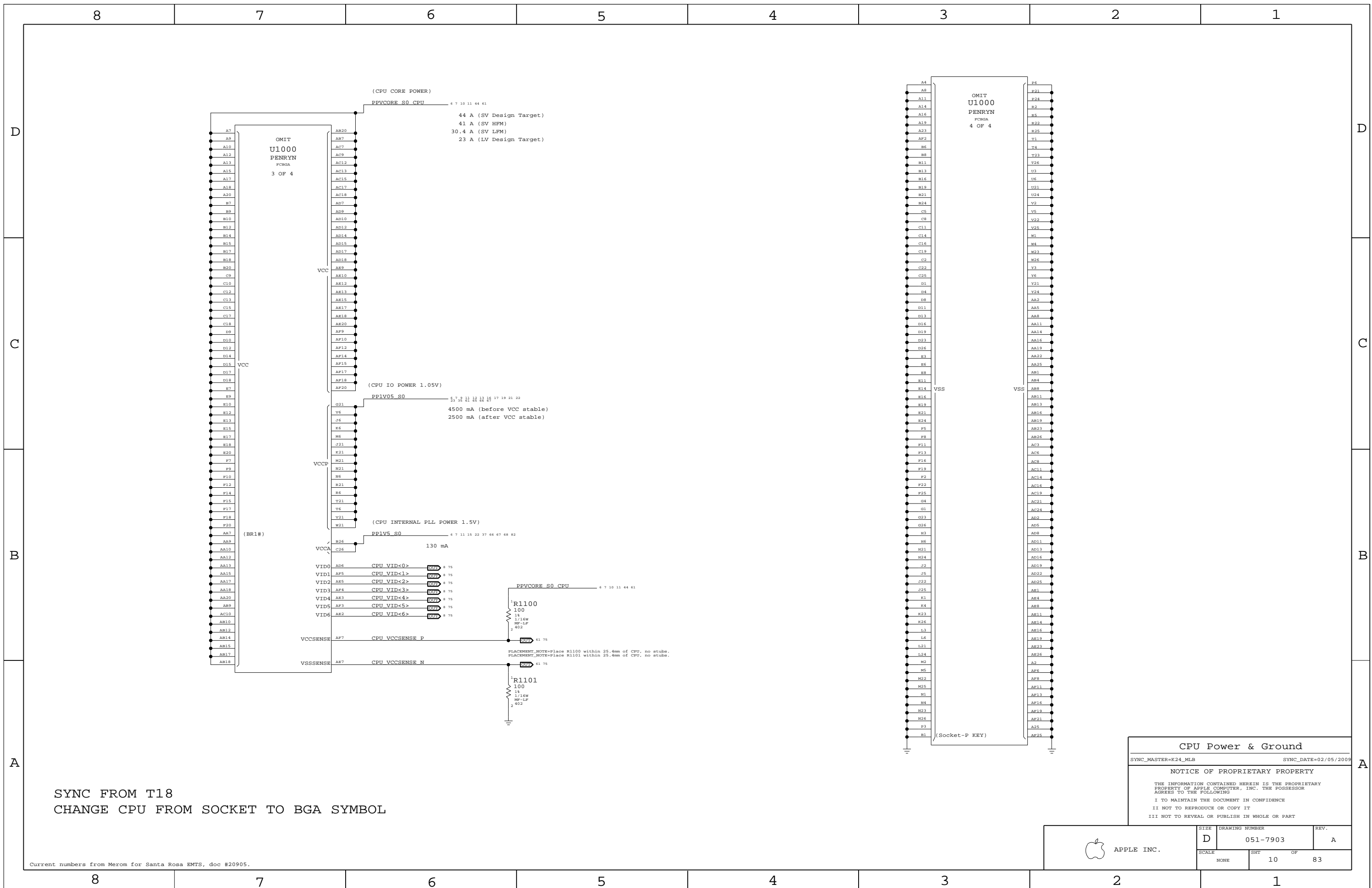




SYNC FROM T18  
 CHANGE CPU FROM SOCKET TO BGA SYMBOL

**CPU FSB**  
 SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/05/2009  
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SCALE	NONE	SHT	OF 83



SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

**CPU Power & Ground**

SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/05/2009

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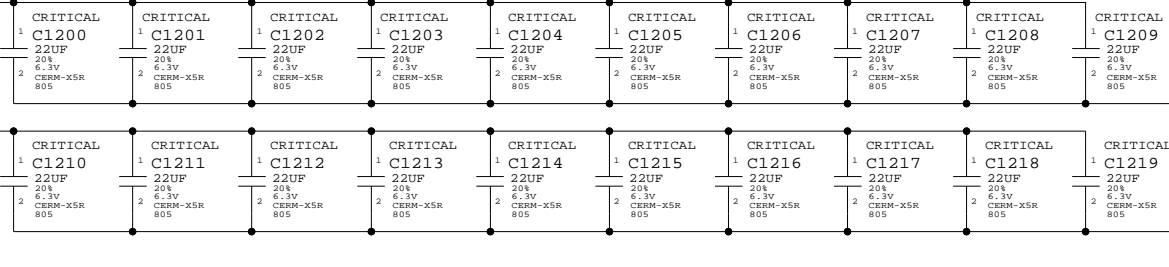
### CPU VCore HF and Bulk Decoupling

4X 330UF, 20X 22UF 0805

61 44 10 7 6 PPVCORE\_S0\_CPU

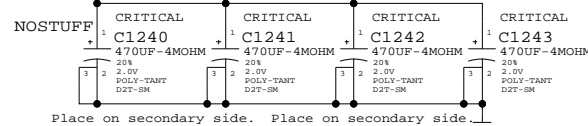
PLACEMENT\_NOTE (C1200-C1219):

Place inside socket cavity on secondary side.



PLACEMENT\_NOTE (C1240-C1243):

Place on secondary side. Place on secondary side.

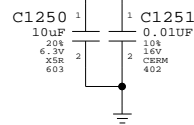


### VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF

82 48 47 66 37 22 15 10 7 6 PP1V5\_S0

PLACEMENT\_NOTE=Place C1281 near CPU pin B26.

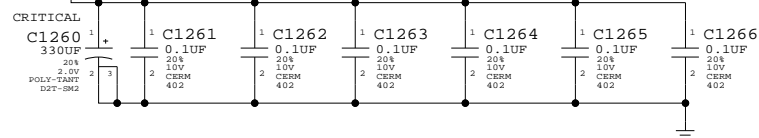


### VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

22 21 19 17 16 13 12 10 9 7 5 PP1V05\_S0

PLACEMENT\_NOTE=Place C1260 between CPU & NB.



SYNC FROM T18  
 REMOVE NO STUFF CAPS C1220 TO C1231  
 REMOVE C1244 & C1245  
 CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

CPU Decoupling		
SYNC_MASTER=K24_MLB	SYNC_DATE=02/05/2009	
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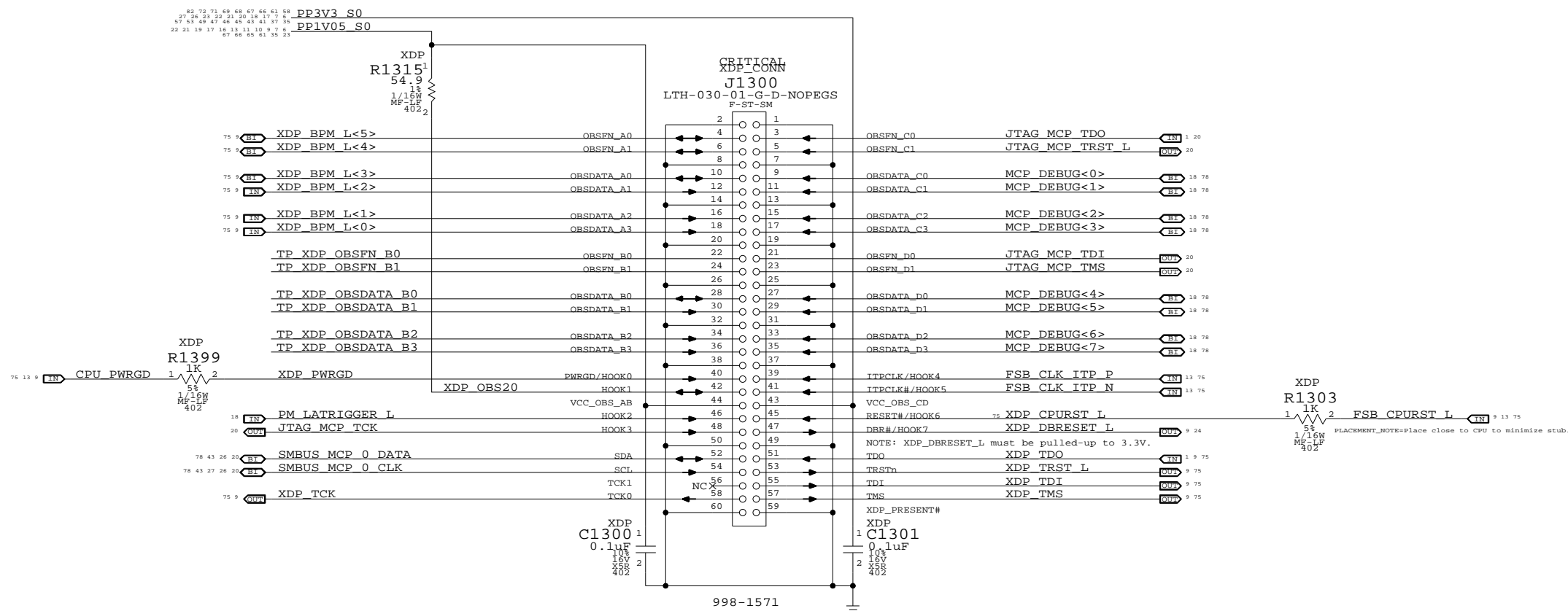
2

1

### Mini-XDP Connector

NOTE: This is not the standard XDP pinout.  
Use with 920-0620 adapter board to support CPU, MCP debugging.

### MCP79-specific pinout



← Direction of XDP module  
Please avoid any obstructions on even-numbered side of J1300

eXtended Debug Port (MiniXDP)  
 SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009  
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NONE	12 OF		83

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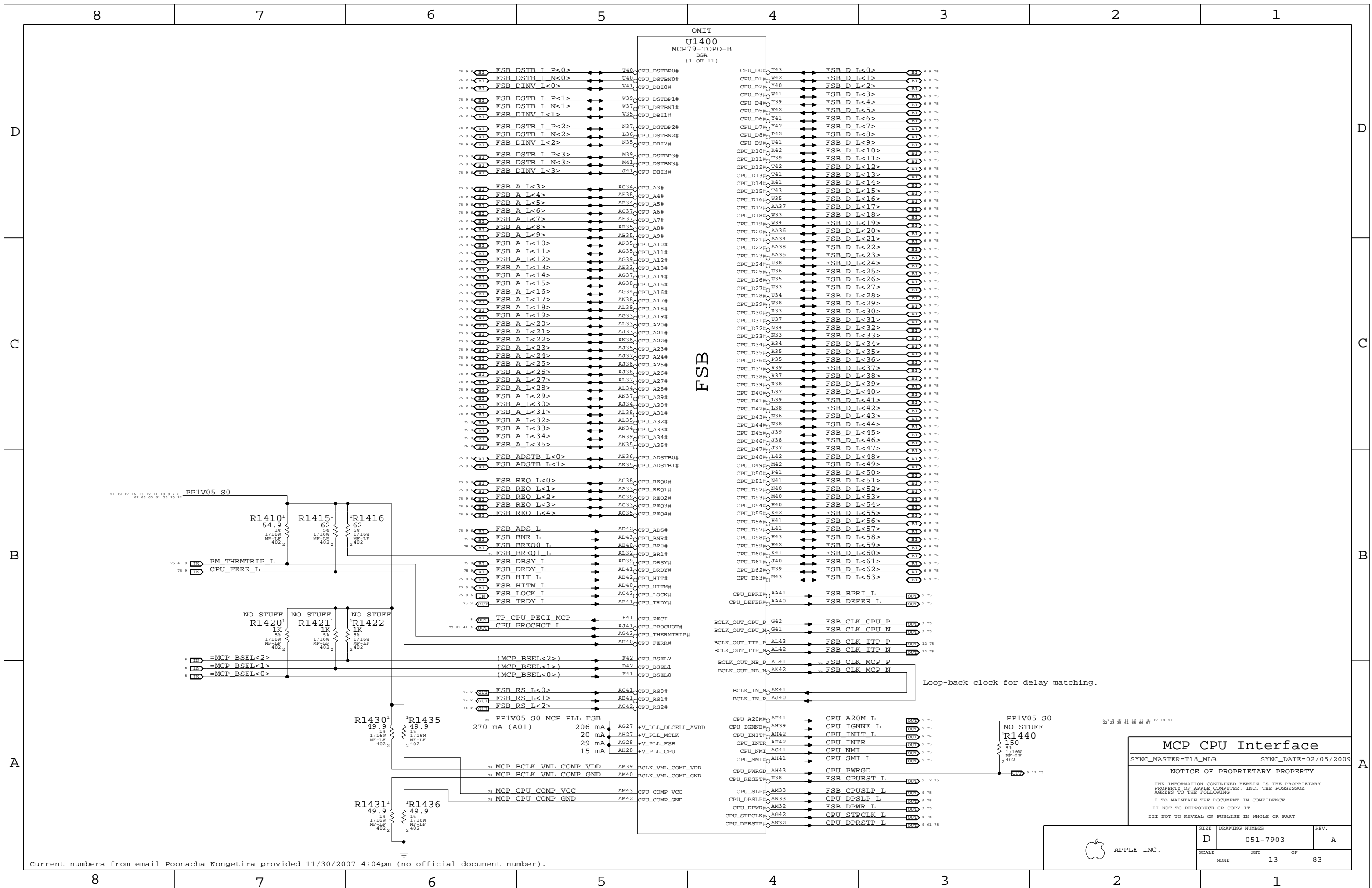
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U1400  
MCP79-TOPO-B  
BGA  
(1 OF 11)

75 9	FSB DSTB L P<0>	T40	CPU_DSTBP0#
75 9	FSB DSTB L N<0>	U40	CPU_DSTBN0#
75 9	FSB DINV L<0>	V41	CPU_DBI0#
75 9	FSB DSTB L P<1>	W39	CPU_DSTBP1#
75 9	FSB DSTB L N<1>	W37	CPU_DSTBN1#
75 9	FSB DINV L<1>	V35	CPU_DBI1#
75 9	FSB DSTB L P<2>	N37	CPU_DSTBP2#
75 9	FSB DSTB L N<2>	L36	CPU_DSTBN2#
75 9	FSB DINV L<2>	N35	CPU_DBI2#
75 9	FSB DSTB L P<3>	M39	CPU_DSTBP3#
75 9	FSB DSTB L N<3>	M41	CPU_DSTBN3#
75 9	FSB DINV L<3>	J41	CPU_DBI3#
75 9	FSB A L<3>	AC34	CPU_A3#
75 9	FSB A L<4>	AE38	CPU_A4#
75 9	FSB A L<5>	AE34	CPU_A5#
75 9	FSB A L<6>	AC37	CPU_A6#
75 9	FSB A L<7>	AE37	CPU_A7#
75 9	FSB A L<8>	AE35	CPU_A8#
75 9	FSB A L<9>	AB35	CPU_A9#
75 9	FSB A L<10>	AF35	CPU_A10#
75 9	FSB A L<11>	AG35	CPU_A11#
75 9	FSB A L<12>	AG39	CPU_A12#
75 9	FSB A L<13>	AE33	CPU_A13#
75 9	FSB A L<14>	AG37	CPU_A14#
75 9	FSB A L<15>	AG38	CPU_A15#
75 9	FSB A L<16>	AG34	CPU_A16#
75 9	FSB A L<17>	AN38	CPU_A17#
75 9	FSB A L<18>	AL39	CPU_A18#
75 9	FSB A L<19>	AG33	CPU_A19#
75 9	FSB A L<20>	AL33	CPU_A20#
75 9	FSB A L<21>	AJ33	CPU_A21#
75 9	FSB A L<22>	AN36	CPU_A22#
75 9	FSB A L<23>	AJ35	CPU_A23#
75 9	FSB A L<24>	AJ37	CPU_A24#
75 9	FSB A L<25>	AJ36	CPU_A25#
75 9	FSB A L<26>	AJ38	CPU_A26#
75 9	FSB A L<27>	AL37	CPU_A27#
75 9	FSB A L<28>	AL34	CPU_A28#
75 9	FSB A L<29>	AN37	CPU_A29#
75 9	FSB A L<30>	AJ34	CPU_A30#
75 9	FSB A L<31>	AL38	CPU_A31#
75 9	FSB A L<32>	AL35	CPU_A32#
75 9	FSB A L<33>	AN34	CPU_A33#
75 9	FSB A L<34>	AR39	CPU_A34#
75 9	FSB A L<35>	AN35	CPU_A35#
75 9	FSB ADSTB L<0>	AE36	CPU_ADSTB0#
75 9	FSB ADSTB L<1>	AK35	CPU_ADSTB1#
75 9	FSB REQ L<0>	AC38	CPU_REQ0#
75 9	FSB REQ L<1>	AA33	CPU_REQ1#
75 9	FSB REQ L<2>	AC39	CPU_REQ2#
75 9	FSB REQ L<3>	AC33	CPU_REQ3#
75 9	FSB REQ L<4>	AC35	CPU_REQ4#
75 9	FSB ADS L	AD42	CPU_ADS#
75 9	FSB BNR L	AD43	CPU_BNR#
75 9	FSB BREO L	AE40	CPU_BR0#
75 9	FSB BREO1 L	AL32	CPU_BR1#
75 9	FSB DBSY L	AD39	CPU_DBSY#
75 9	FSB DRDY L	AD41	CPU_DRDY#
75 9	FSB HIT L	AB42	CPU_HIT#
75 9	FSB HITM L	AD40	CPU_HITM#
75 9	FSB LOCK L	AC43	CPU_LOCK#
75 9	FSB TRDY L	AE41	CPU_TRDY#
75 9	TP CPU PECCI MCP	E41	CPU_PECCI
75 9	CPU PROCHOT L	AJ41	CPU_PROCHOT#
75 9		AG43	CPU_THERMTRIP#
75 9		AH40	CPU_FERR#
75 9	FSB RS L<0>	AC41	CPU_RS0#
75 9	FSB RS L<1>	AB41	CPU_RS1#
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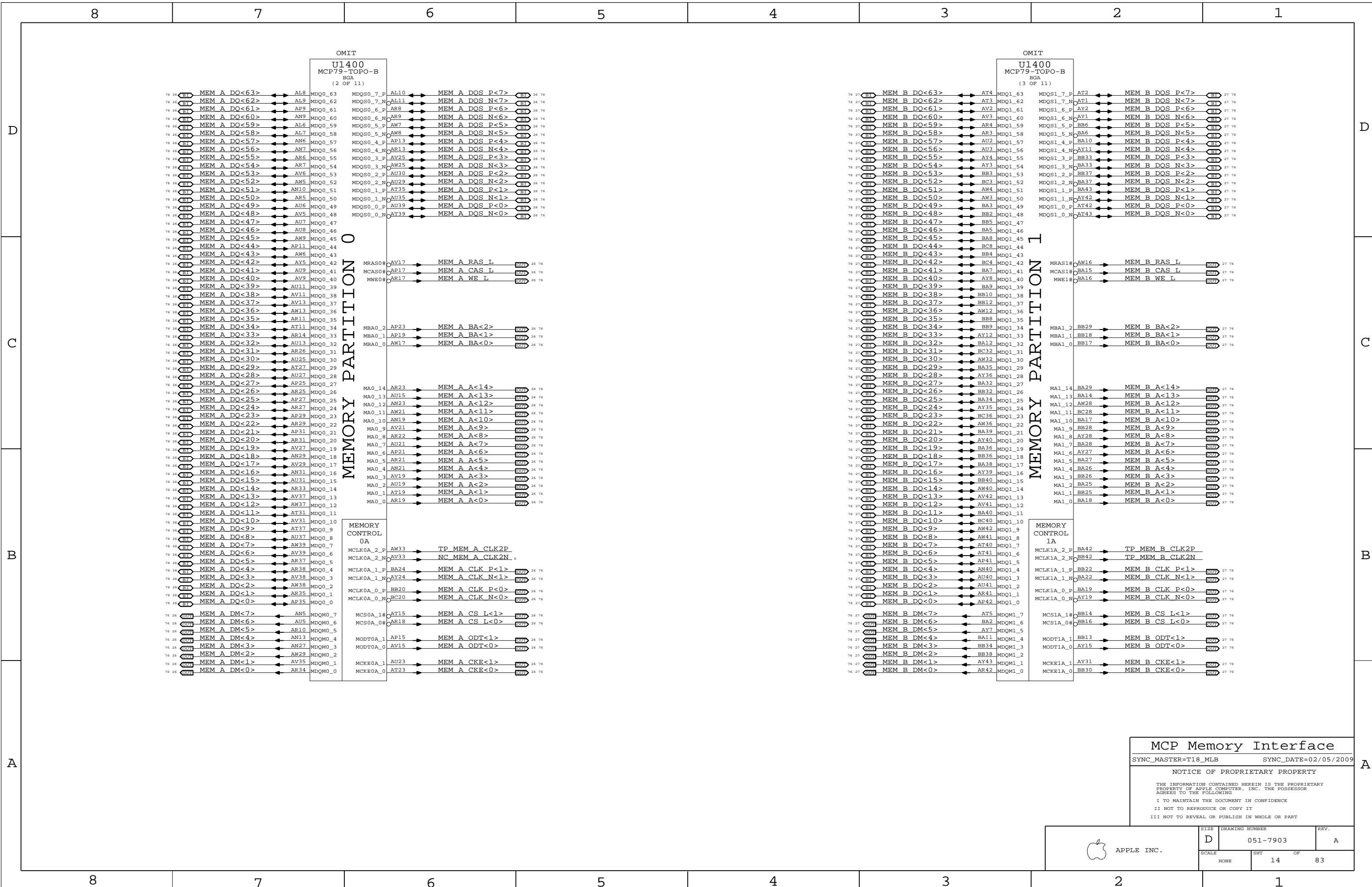
FSB

Loop-back clock for delay matching.

**MCP CPU Interface**  
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MCP Memory Interface

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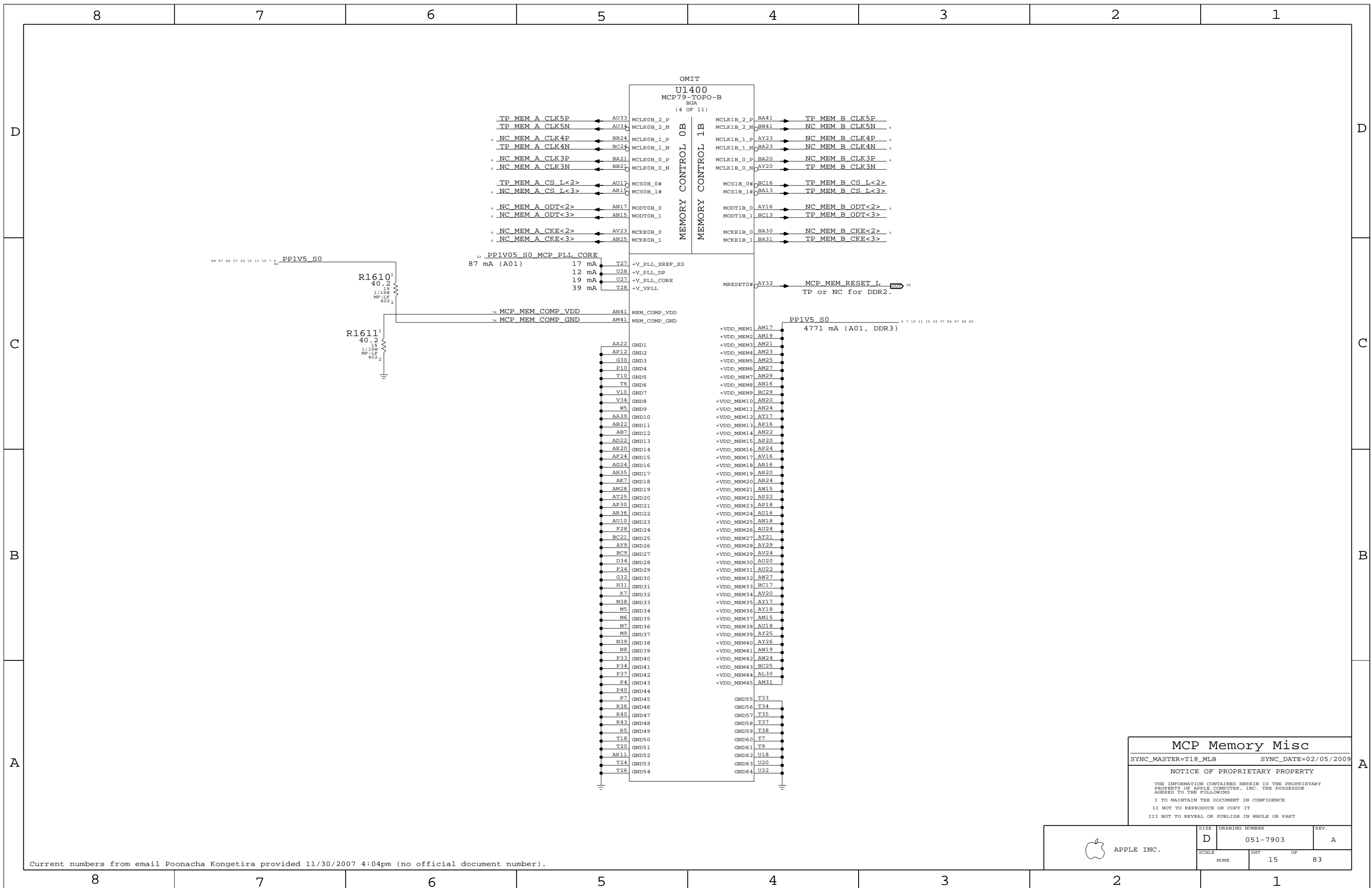
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**MCP Memory Misc**

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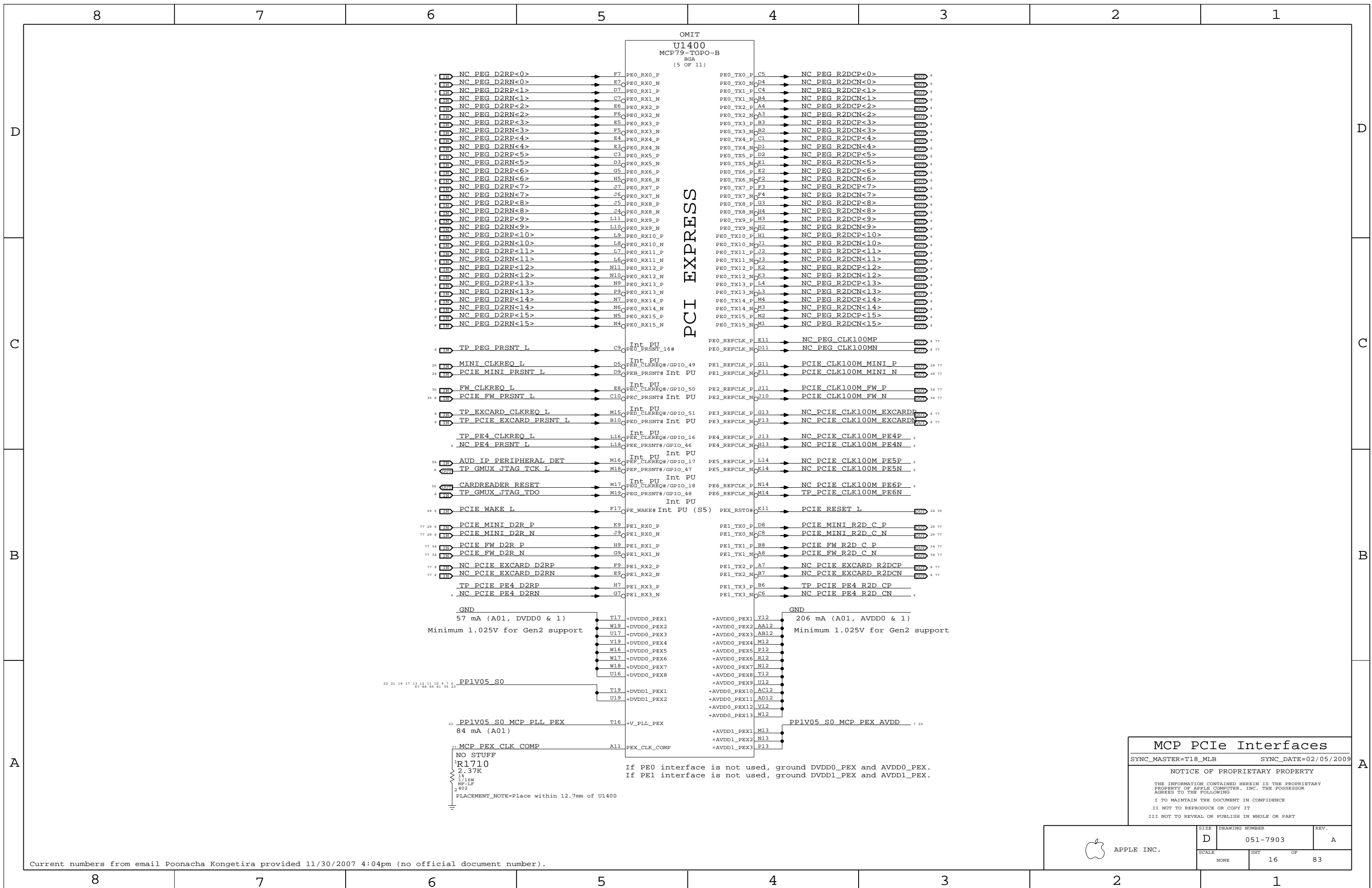
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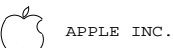


**MCP PCIe Interfaces**

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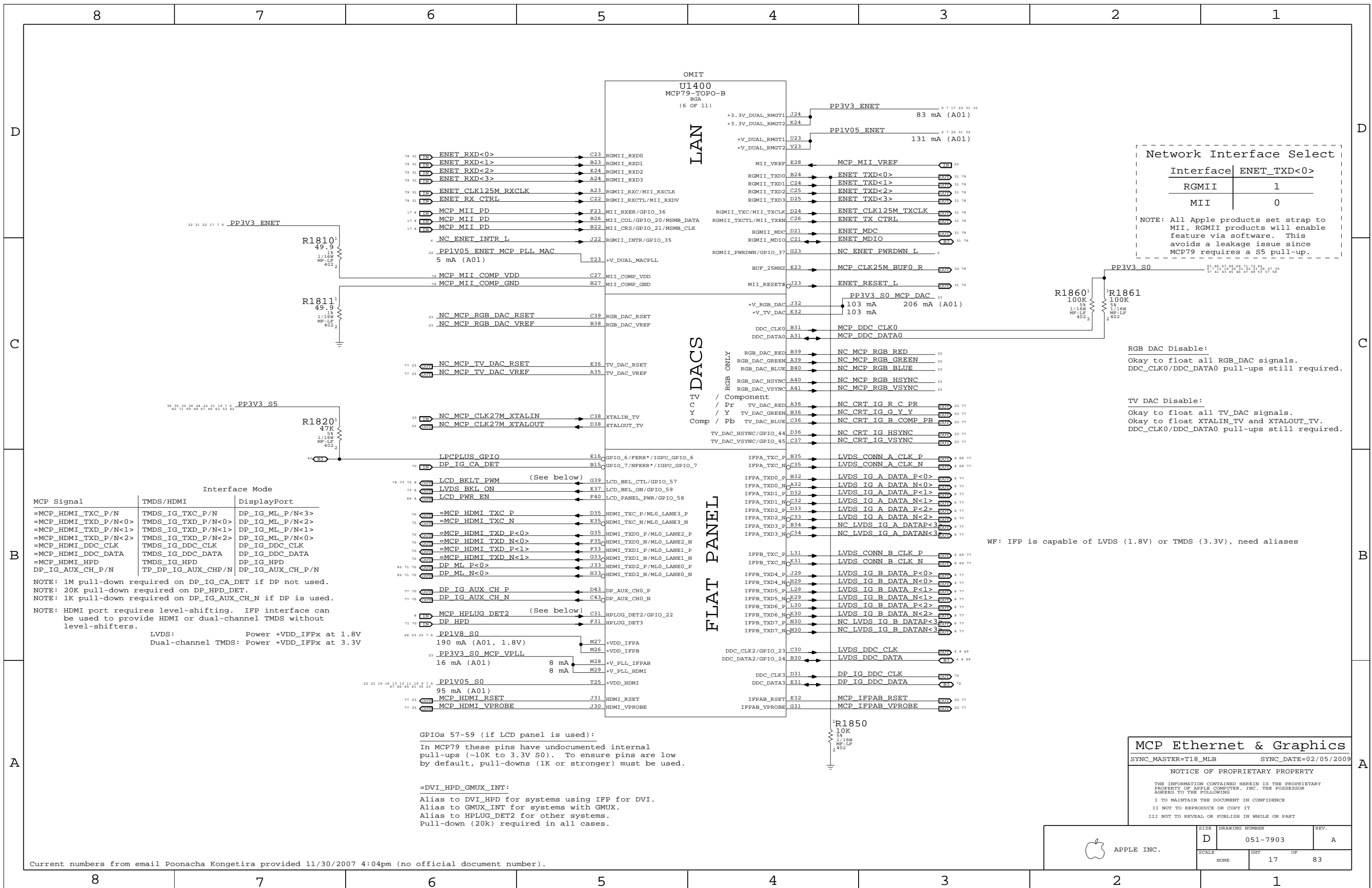
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NONE	16	83





Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:  
Okay to float all RGB\_DAC signals.  
DDC\_CLK0/DDC\_DATA0 pull-ups still required.

TV DAC Disable:  
Okay to float all TV\_DAC signals.  
Okay to float XTALIN\_TV and XTALOUT\_TV.  
DDC\_CLK0/DDC\_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
NOTE: 20K pull-down required on DP\_HPD\_DET.  
NOTE: 1K pull-down required on DP\_IG\_AUX\_CH\_N if DP is used.  
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS:  
Power +VDD\_IFP<sub>x</sub> at 1.8V  
Dual-channel TMDS: Power +VDD\_IFP<sub>x</sub> at 3.3V

GPIOs 57-59 (if LCD panel is used):  
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI\_HPD\_GMUX\_INT:  
Alias to DVI\_HPD for systems using IFP for DVI.  
Alias to GMUX\_INT for systems with GMUX.  
Alias to HPLUG\_DET2 for other systems.  
Pull-down (20k) required in all cases.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

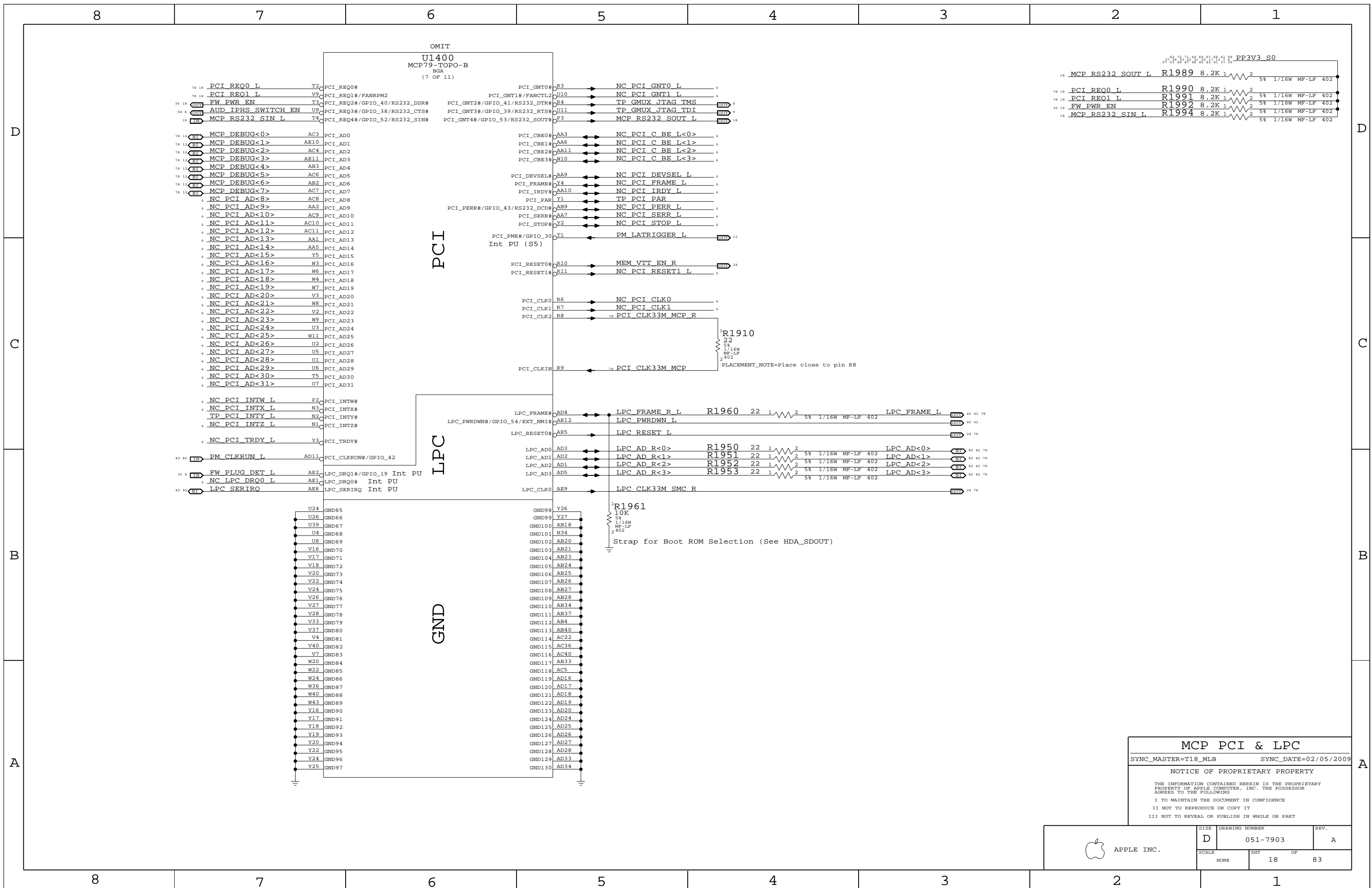
MCP Ethernet & Graphics

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NONE	17	83	



**MCP PCI & LPC**

SYNC\_MASTER=T18\_MLB      SYNC\_DATE=02/05/2009

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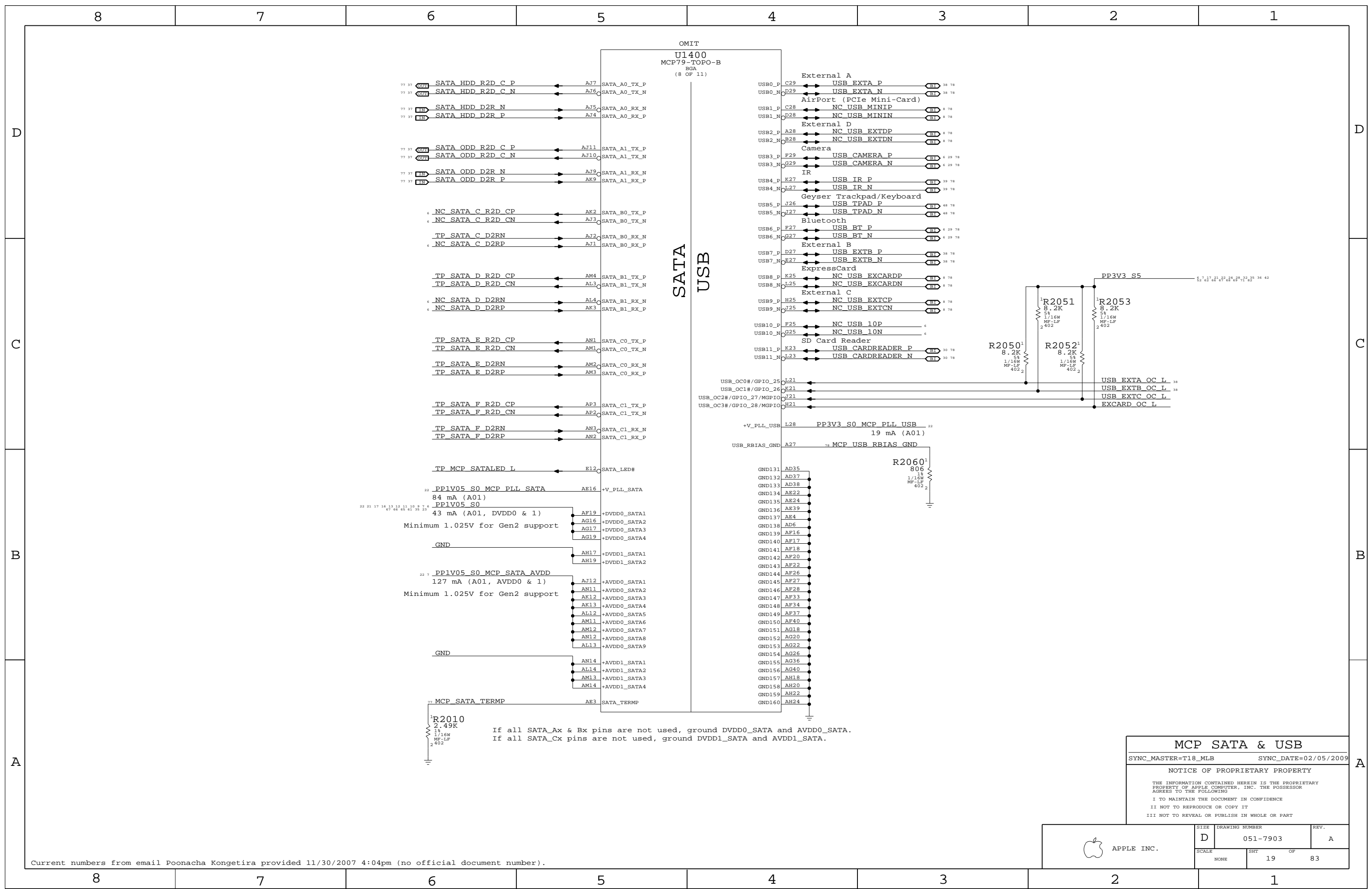
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APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7903	REV. A
	SCALE NONE	SHEET 18	OF 83

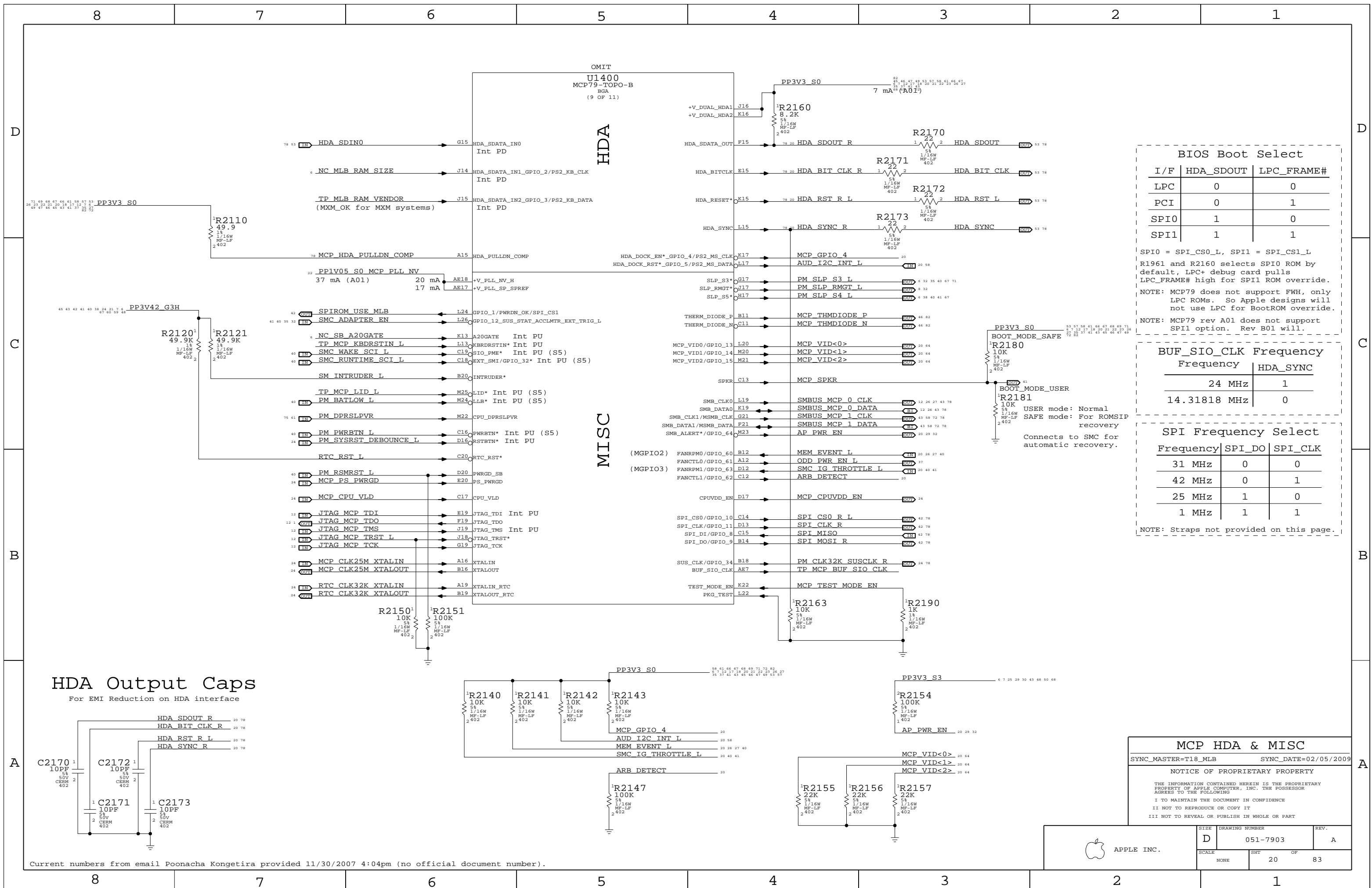


If all SATA\_Ax & Bx pins are not used, ground DVDD0\_SATA and AVDD0\_SATA.  
 If all SATA\_Cx pins are not used, ground DVDD1\_SATA and AVDD1\_SATA.

**MCP SATA & USB**  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	19		83

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



**BIOS Boot Select**

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L  
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC\_FRAME# high for SPI1 ROM override.  
 NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.  
 NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

**BUF\_SIO\_CLK Frequency**

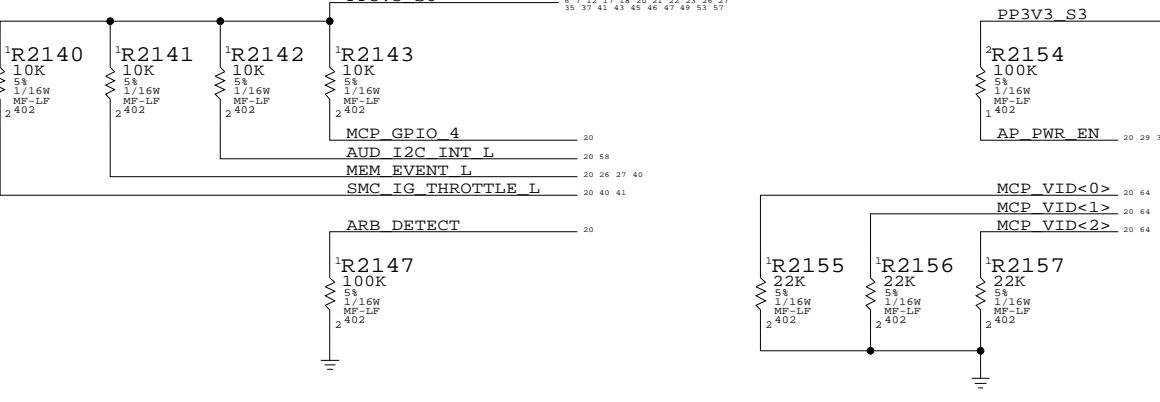
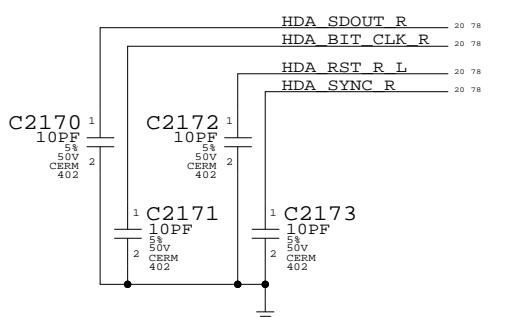
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

**SPI Frequency Select**

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

**HDA Output Caps**  
 For EMI Reduction on HDA interface



**MCP HDA & MISC**

SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009

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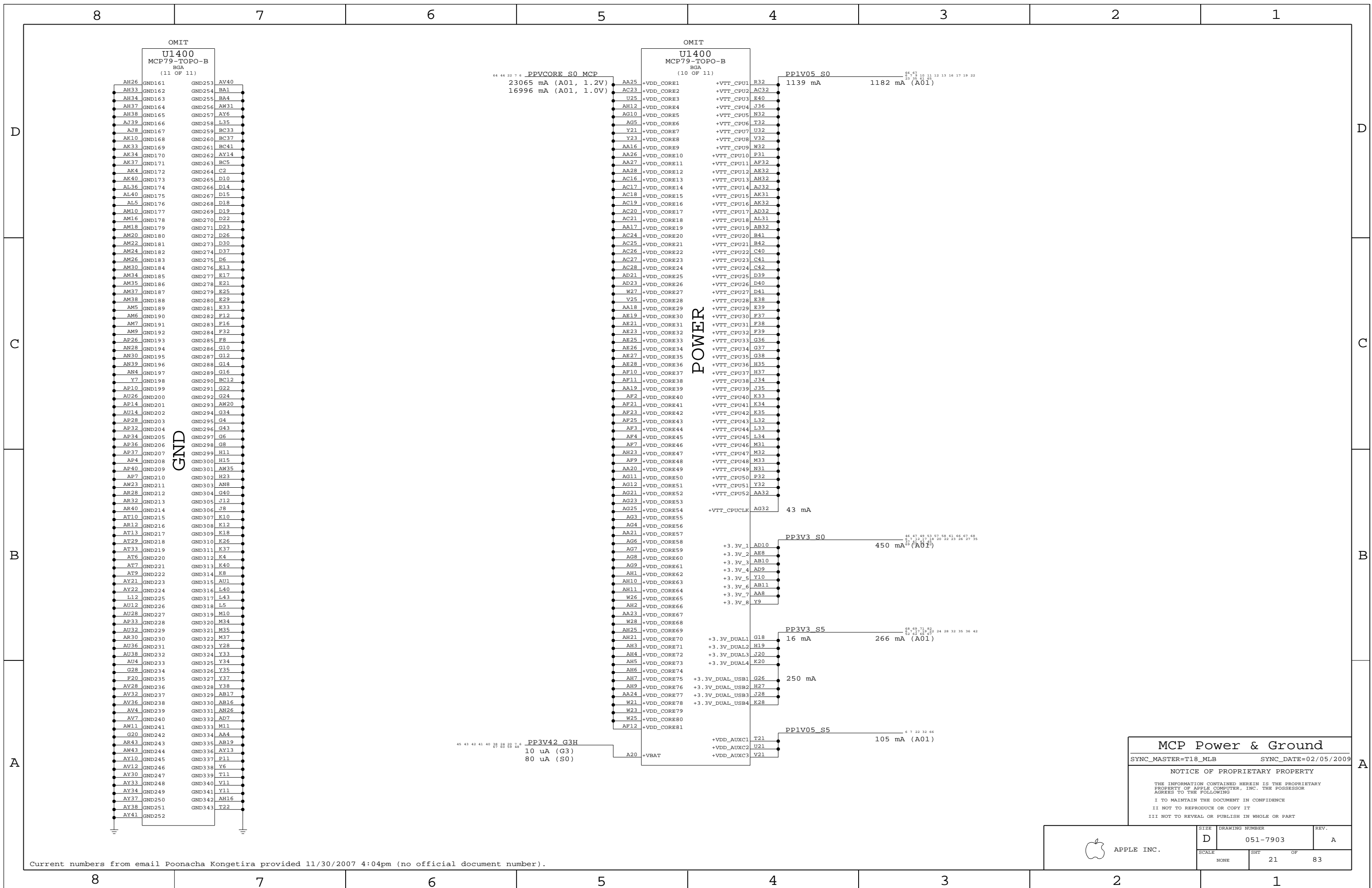
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	20		83

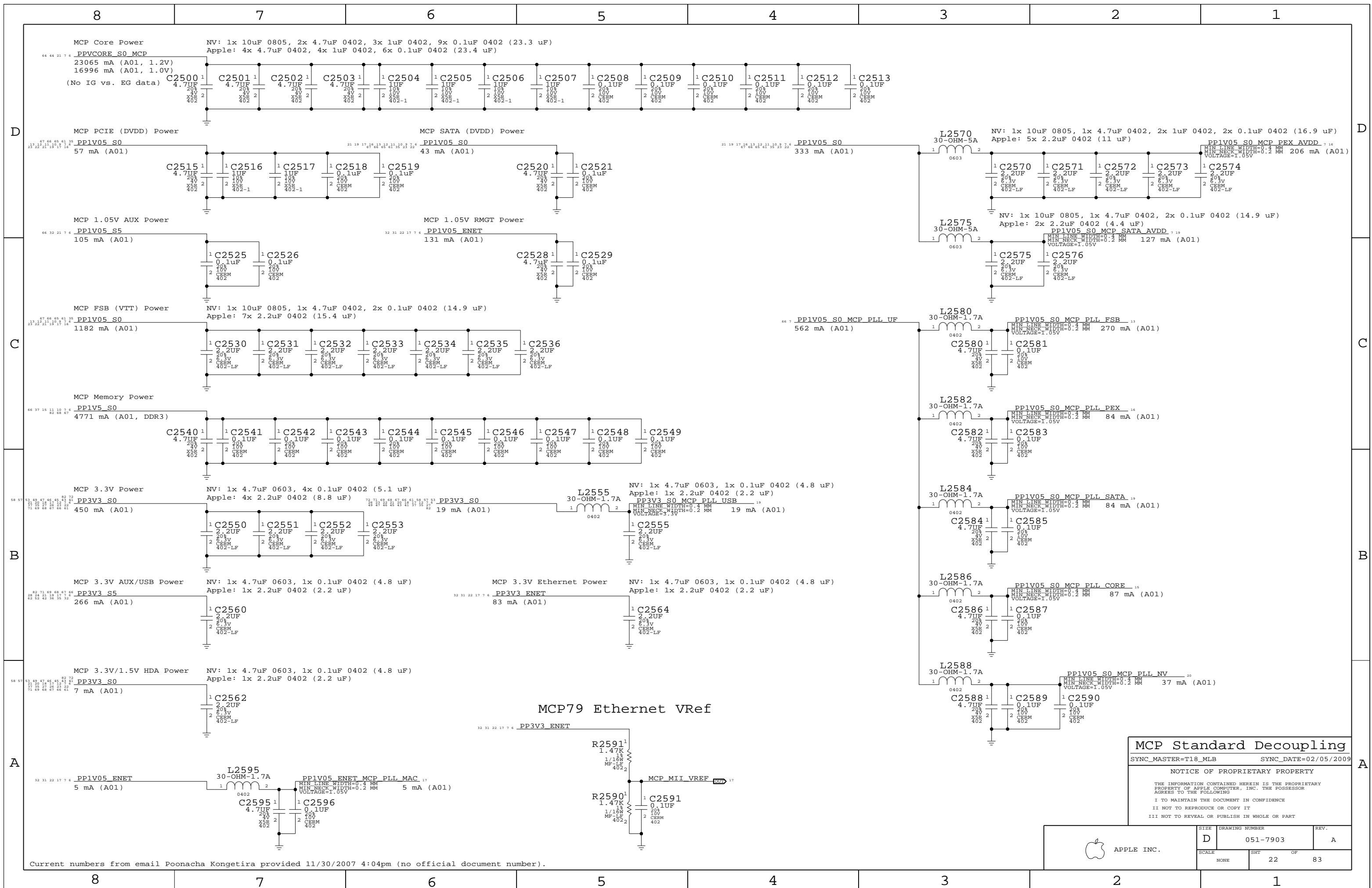
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

**MCP Power & Ground**  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	21		83



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

### MCP Standard Decoupling

SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	22	83

8

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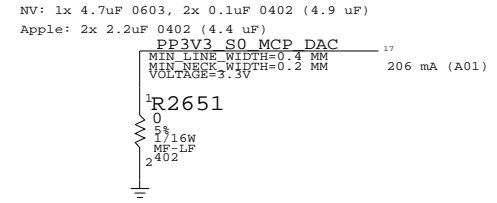
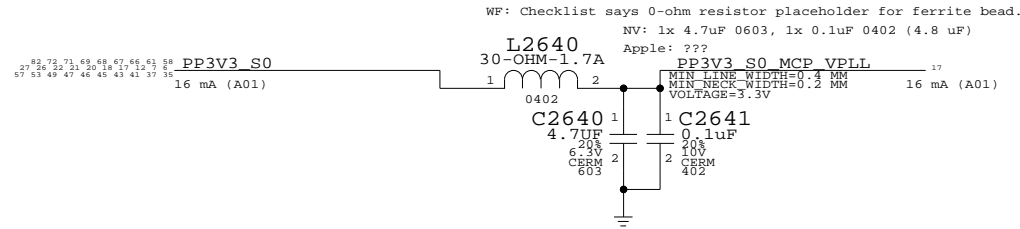
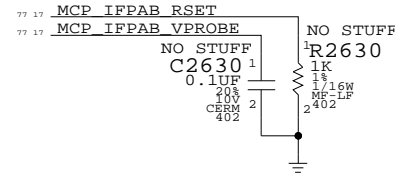
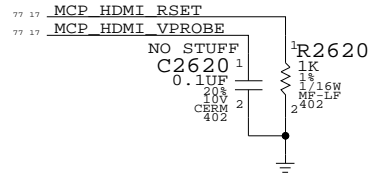
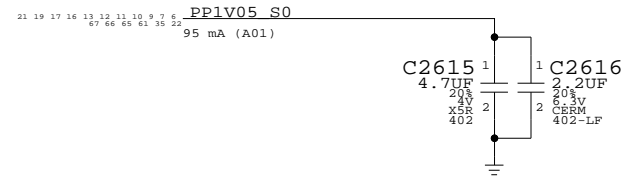
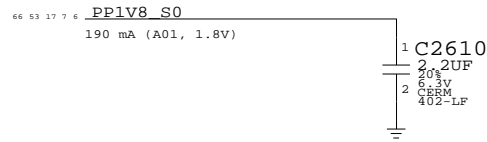
3

2

1

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)  
Apple: 1x 2.2uF 0402 (2.2 uF)



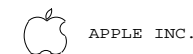
23 17	NC MCP RGB RED	==	NC MCP RGB RED	17 23
23 17	NC MCP RGB GREEN	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP RGB GREEN	17 23
23 17	NC MCP RGB BLUE	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP RGB BLUE	17 23
23 17	NC MCP RGB HSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP RGB HSYNC	17 23
23 17	NC MCP RGB VSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP RGB VSYNC	17 23
77 23 17	NC CRT IG R C PR	==	MAKE_BASE=TRUE NO_TEST=TRUE NC CRT IG R C PR	17 23 77
77 23 17	NC CRT IG G Y Y	==	MAKE_BASE=TRUE NO_TEST=TRUE NC CRT IG G Y Y	17 23 77
77 23 17	NC CRT IG B COMP PB	==	MAKE_BASE=TRUE NO_TEST=TRUE NC CRT IG B COMP PB	17 23 77
77 23 17	NC CRT IG HSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE NC CRT IG HSYNC	17 23 77
77 23 17	NC CRT IG VSYNC	==	MAKE_BASE=TRUE NO_TEST=TRUE NC CRT IG VSYNC	17 23 77
23 17	NC MCP RGB DAC RSET	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP RGB DAC RSET	17 23
23 17	NC MCP RGB DAC VREF	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP RGB DAC VREF	17 23
77 23 17	NC MCP TV DAC RSET	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP TV DAC RSET	17 23 77
77 23 17	NC MCP TV DAC VREF	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP TV DAC VREF	17 23 77
23 17	NC MCP CLK27M XTALIN	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP CLK27M XTALIN	17 23
23 17	NC MCP CLK27M XTALOUT	==	MAKE_BASE=TRUE NO_TEST=TRUE NC MCP CLK27M XTALOUT	17 23

MCP Graphics Support

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009

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APPLE INC.

SIZE	D	DRAWING NUMBER	051-7903	REV.	A
SCALE	NONE	SHT	23	OF	83

8

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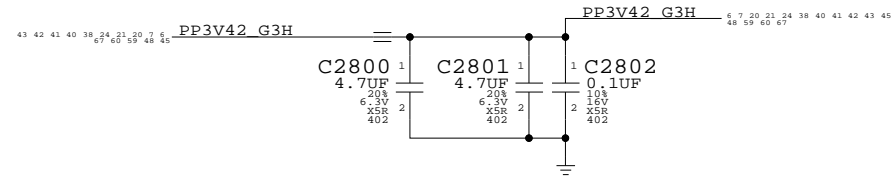
4

3

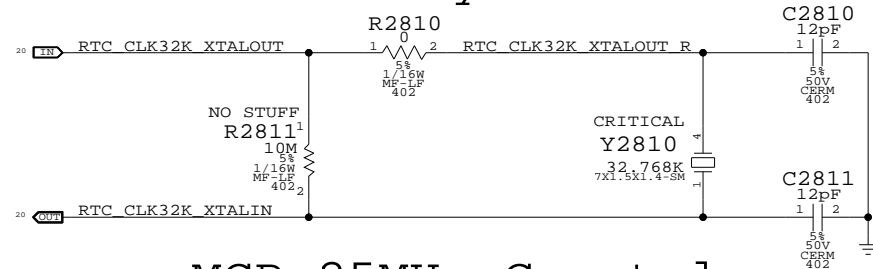
2

1

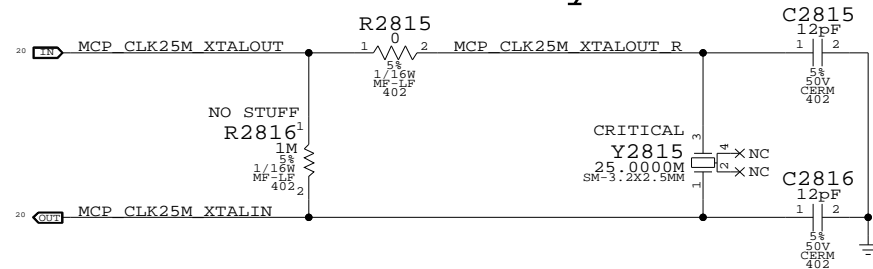
### RTC Power Source



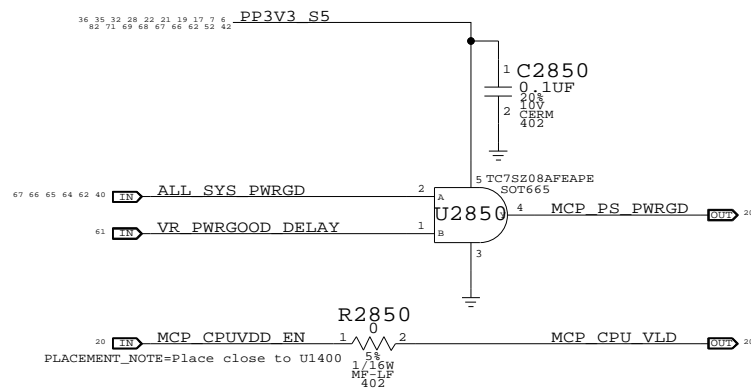
### RTC Crystal



### MCP 25MHz Crystal

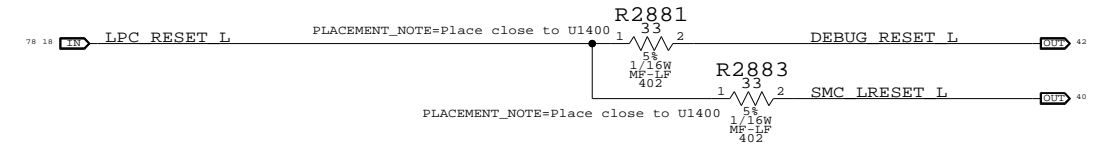


### MCP S0 PWRGD & CPU\_VLD

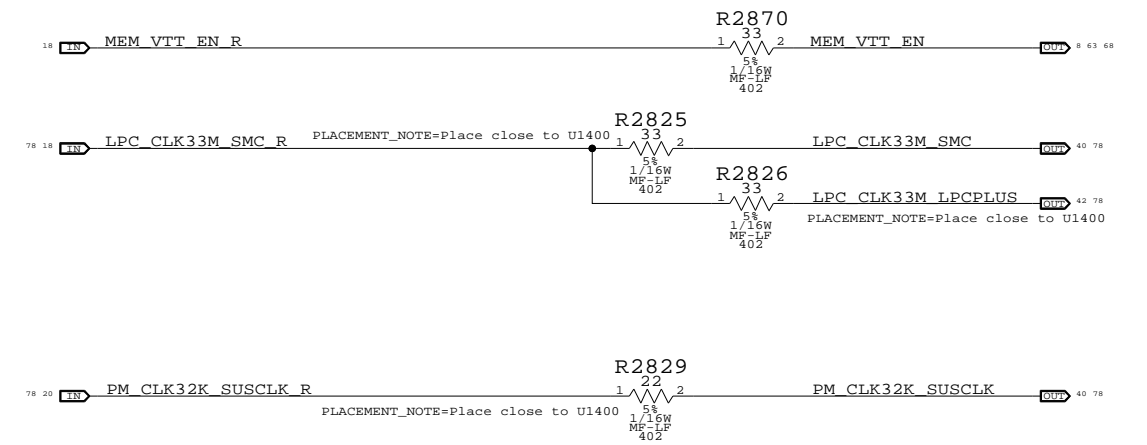
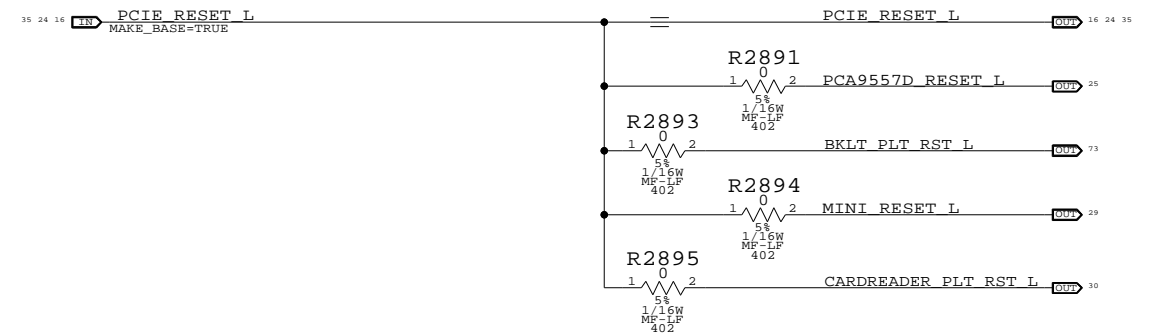


### Platform Reset Connections

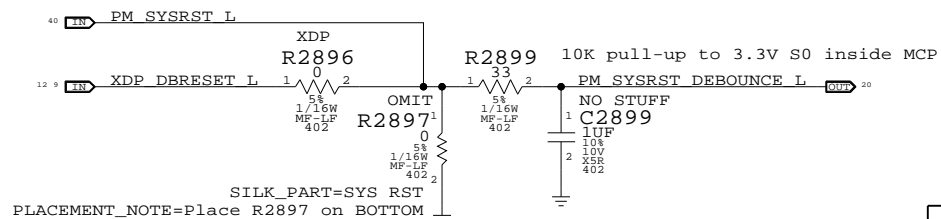
#### LPC Reset (Unbuffered)



#### PCIE Reset (Unbuffered)



### System Reset Circuit



#### SB Misc

SYNC\_MASTER=WFERRY\_K19I SYNC\_DATE=01/06/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	24	83



# Page Notes

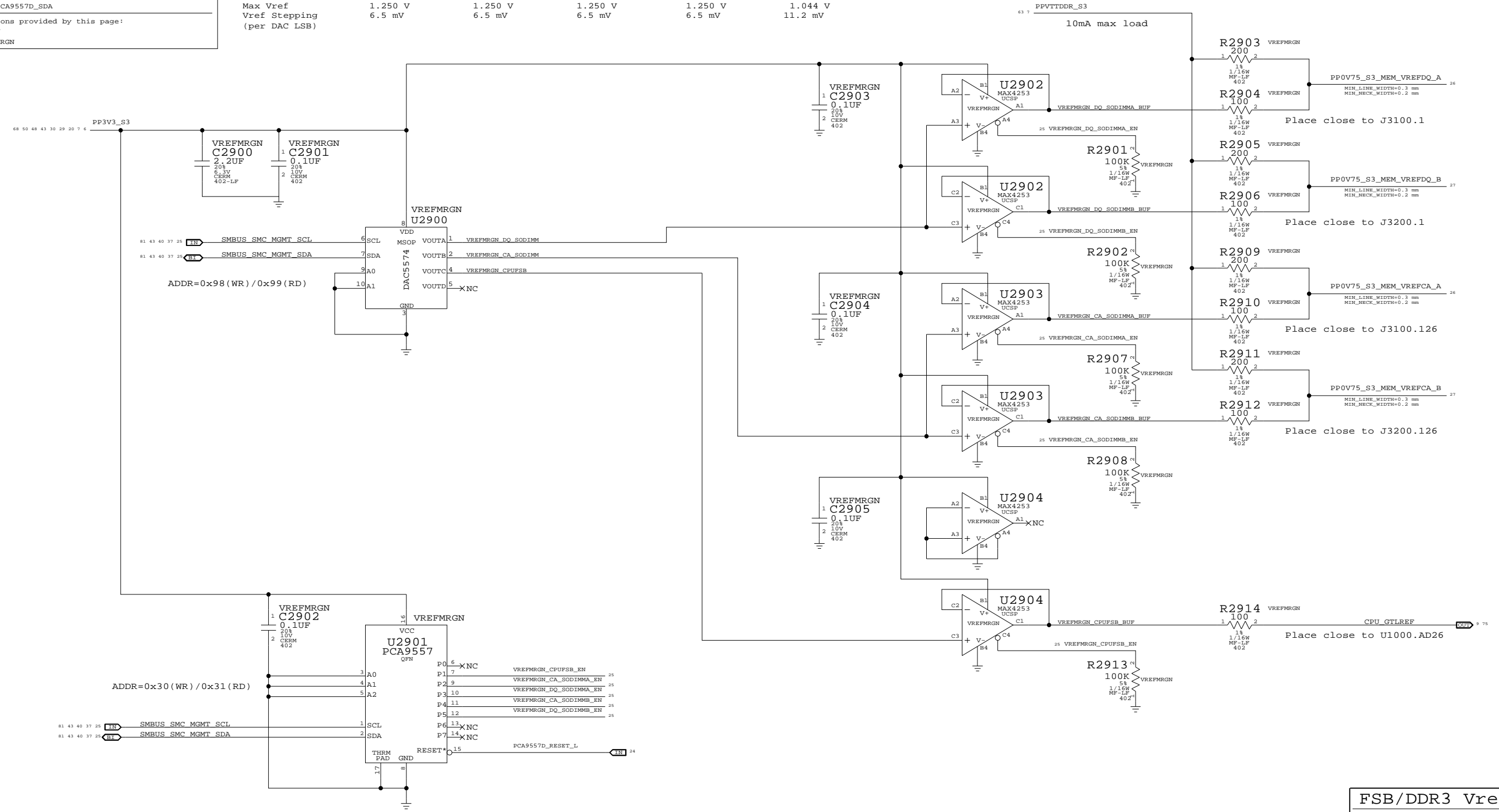
Power aliases required by this page:  
 - =PP3V3\_S3\_VREFMRGN  
 - =PP3V3\_S5\_VREFMRGN  
 - =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
 - =I2C\_VREFDACS\_SCL  
 - =I2C\_VREFDACS\_SDA  
 - =I2C\_PCA9557D\_SCL  
 - =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
 VREFMRGN  
 NO\_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2911	CRITICAL	NO_VREFMRGN

## FSB/DDR3 Vref Margining

SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/05/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	83
NONE	25		

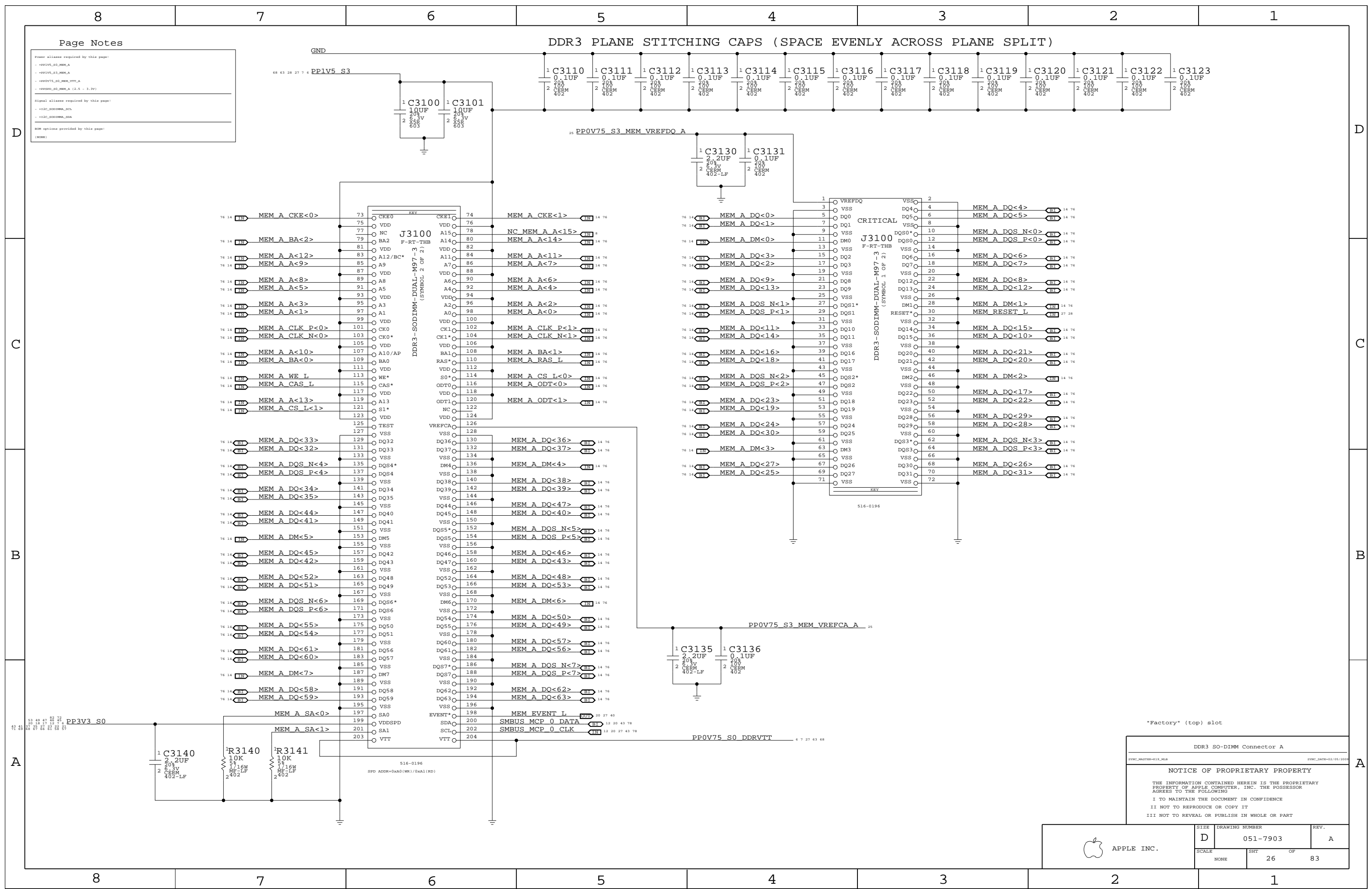
Page Notes

Power aliases required by this page:  
 - PPIV5\_S3\_MEM\_A  
 - PPIV5\_S3\_MEM\_A  
 - PPIV5\_S3\_MEM\_VTT\_A  
 - PPIV5\_S3\_MEM\_A (2.5 - 3.3V)

Signal aliases required by this page:  
 - I2C\_S0D0MMA\_SCL  
 - I2C\_S0D0MMA\_SDA

DRM options provided by this page:  
 (NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYMC\_MASTER=K19\_MLS SYMC\_DATE=02/09/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	26		83

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

**Page Notes**

Power aliases required by this page:

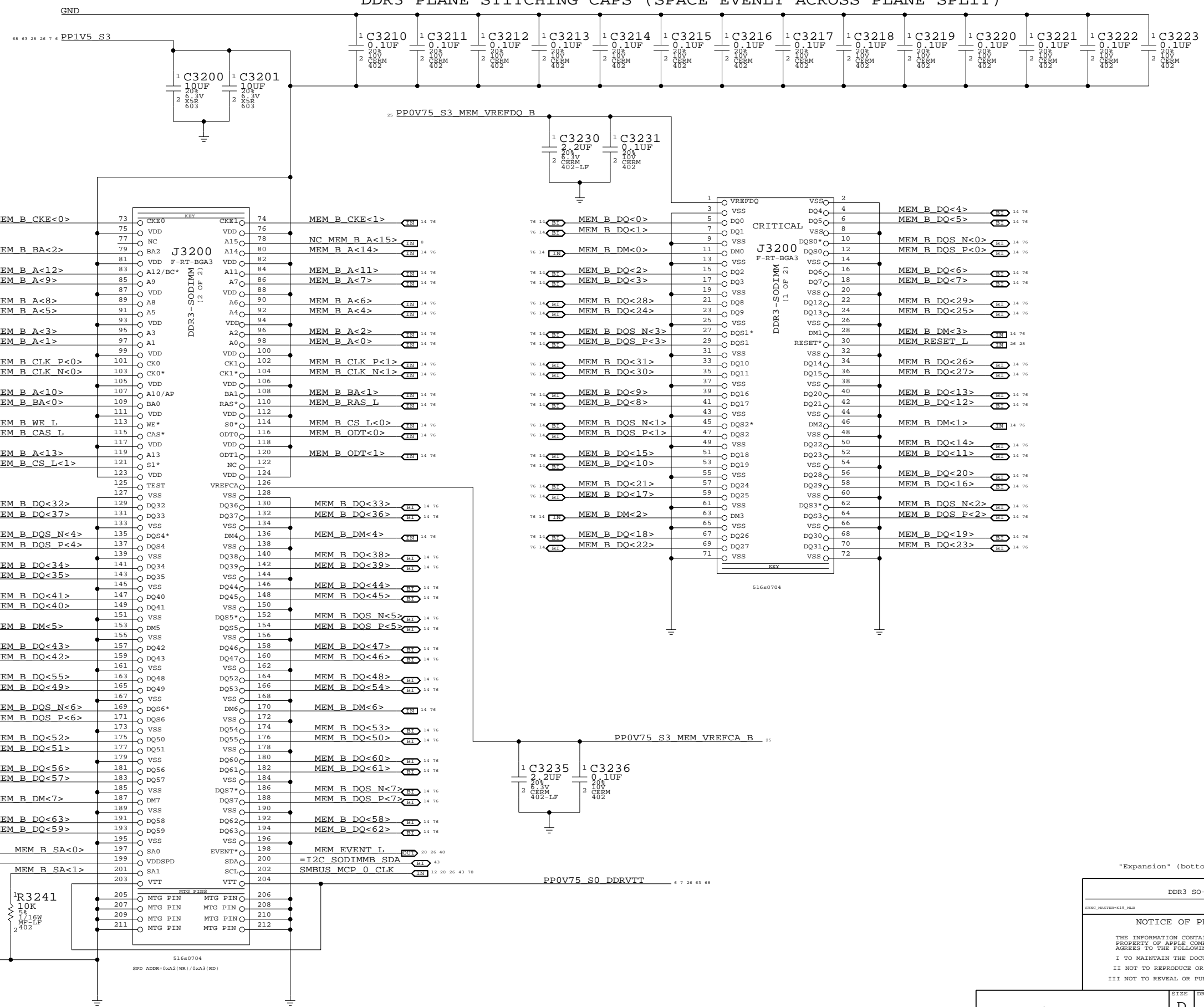
- >PP1V5\_S3\_MEM\_B
- >PP1V5\_S3\_MEM\_L
- >PP0V75\_S3\_MEM\_VTT\_B
- >PP0V75\_S3\_MEM\_VTT\_L
- >PP0V75\_S3\_MEM\_B (2.5 - 3.3V)

Signal aliases required by this page:

- >I2C\_SODIMM\_SCL
- >I2C\_SODIMM\_SDA

DRM options provided by this page:

- (NONE)



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYMC\_MASTER=K19\_MEM SYMC\_DATE=02/09/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	27		83

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D

D

C

C

B

B

A

A

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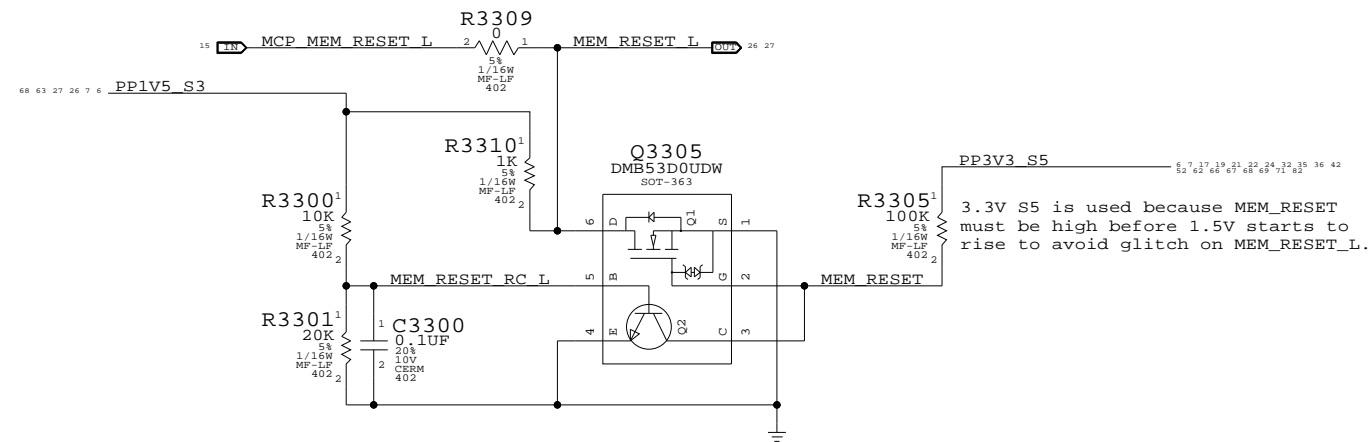
3

2

1

# DDR3 RESET Support

Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.



## DDR3 Support

SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009

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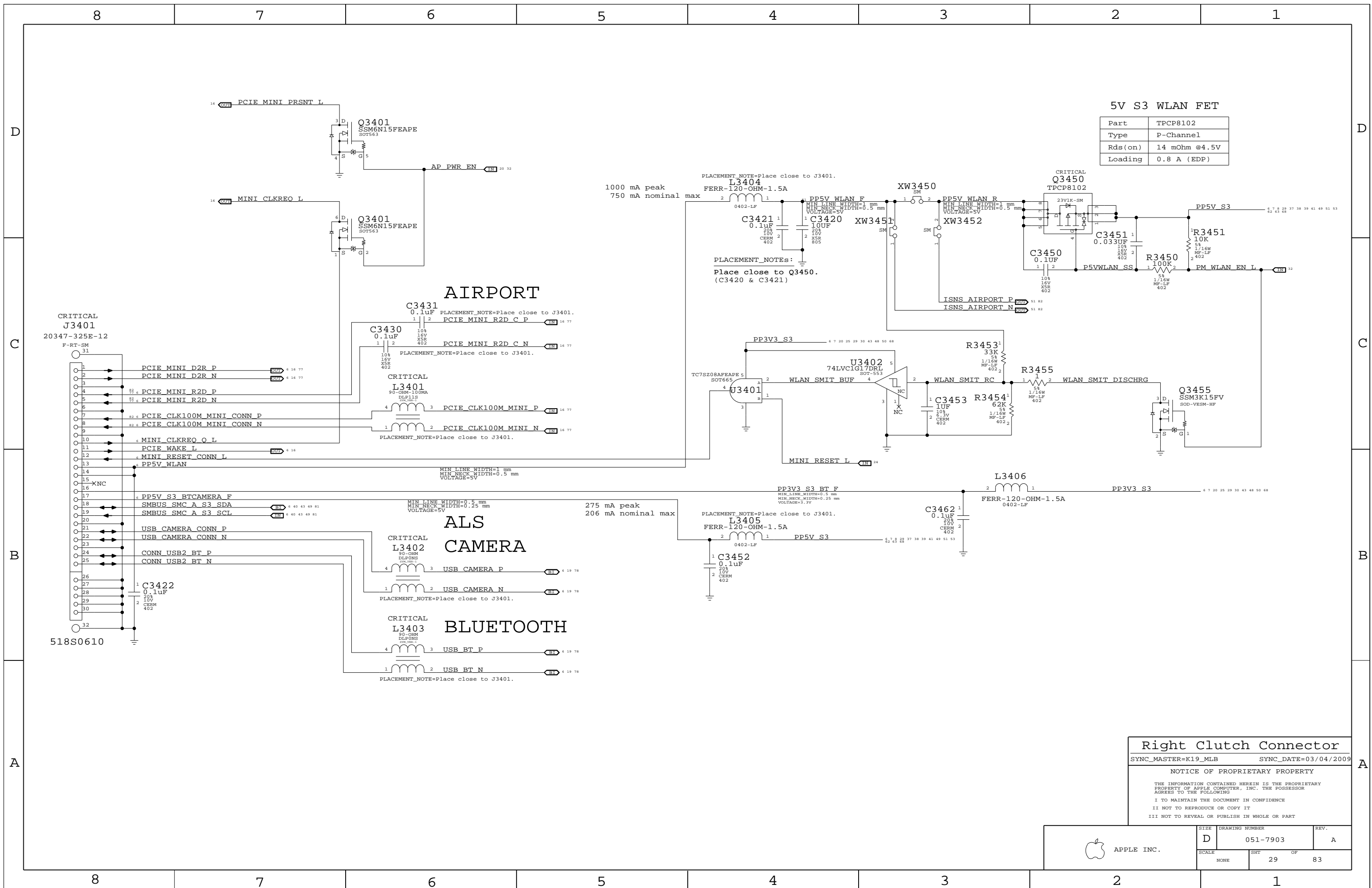
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	28	83



**5V S3 WLAN FET**

Part	TPCP8102
Type	P-Channel
R <sub>ds(on)</sub>	14 mOhm @4.5V
Loading	0.8 A (EDP)

**AIRPORT**

**ALS CAMERA**

**BLUETOOTH**

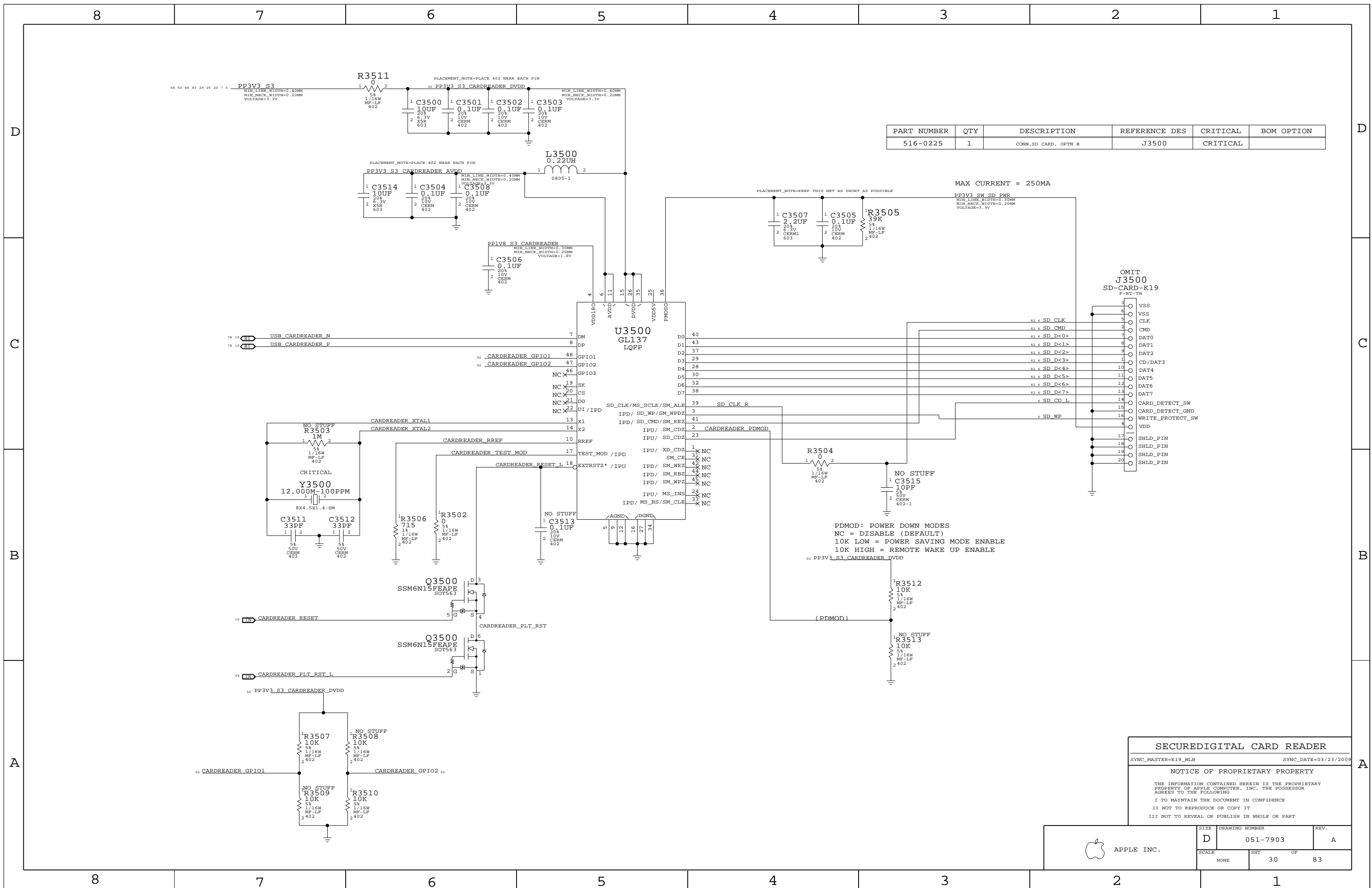
**Right Clutch Connector**

SYNC\_MASTER=K19\_MLB SYNC\_DATE=03/04/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	REV.
NONE	29	83	



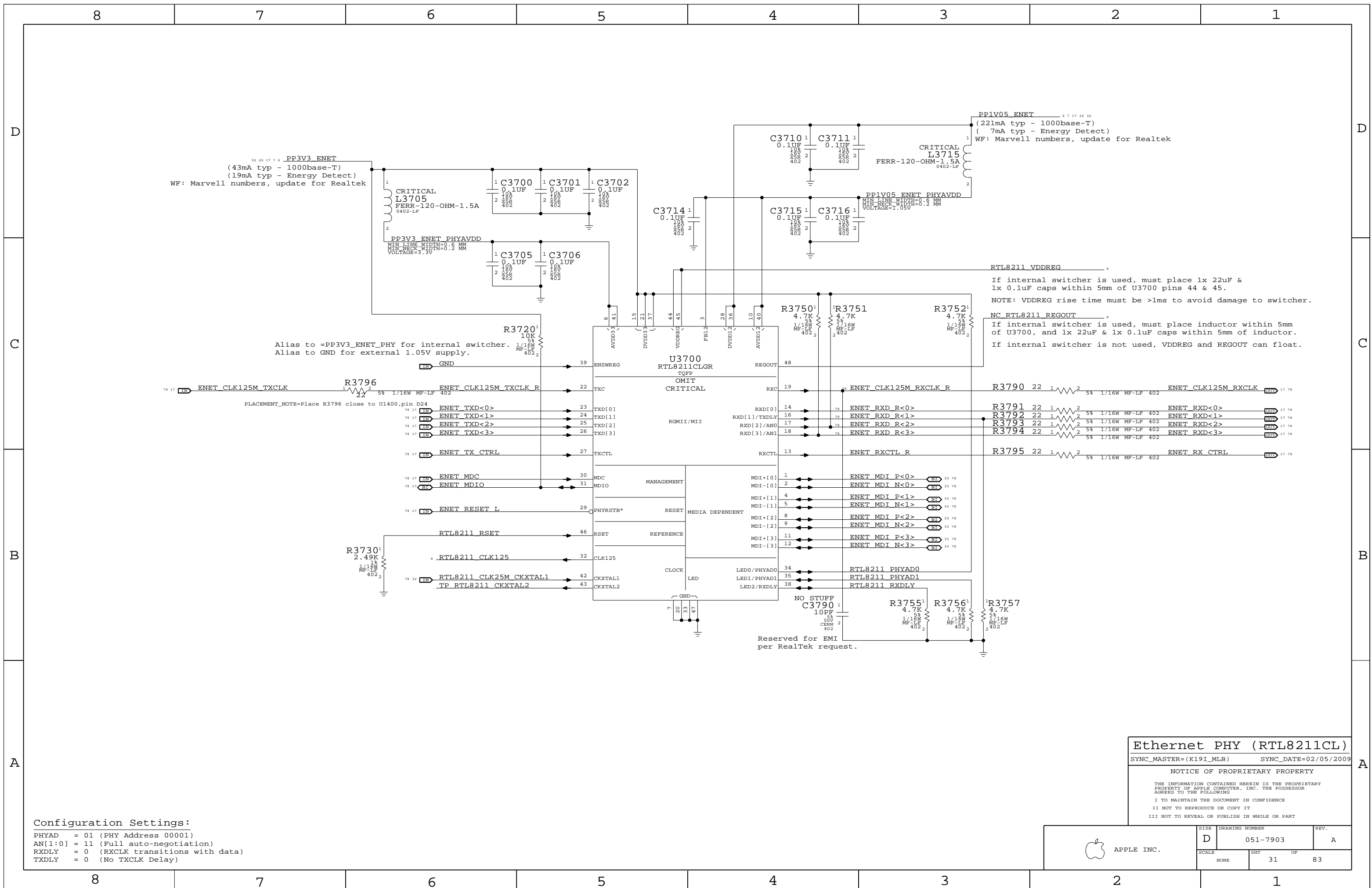
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CORN, SD CARD, OPTN B	J3500	CRITICAL	

MAX CURRENT = 250MA

PDMOD: POWER DOWN MODES  
 NC = DISABLE (DEFAULT)  
 10K LOW = POWER SAVING MODE ENABLE  
 10K HIGH = REMOTE WAKE UP ENABLE

**SECUREDIGITAL CARD READER**  
 SYNC\_MASTER=K19\_MLB SYNC\_DATE=03/23/2009  
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	D	051-7903	A
SCALE	SHT	OF	83
NONE	30		



PP3V3\_ENET  
(43mA typ - 1000base-T)  
(19mA typ - Energy Detect)  
WF: Marvell numbers, update for Realtek

PPIV05\_ENET  
(221mA typ - 1000base-T)  
(7mA typ - Energy Detect)  
WF: Marvell numbers, update for Realtek

Alias to =PP3V3\_ENET\_PHY for internal switcher.  
Alias to GND for external 1.05V supply.

RTL8211\_VDDREG  
If internal switcher is used, must place 1x 22uF & 1x 0.1uF caps within 5mm of U3700 pins 44 & 45.  
NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

NC RTL8211\_REGOUT  
If internal switcher is used, must place inductor within 5mm of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.  
If internal switcher is not used, VDDREG and REGOUT can float.

PLACEMENT\_NOTE=Place R3796 close to U1400, pin D24

Reserved for EMI per RealTek request.

**Configuration Settings:**  
PHYAD = 01 (PHY Address 00001)  
AN[1:0] = 11 (Full auto-negotiation)  
RXDLY = 0 (RXCLK transitions with data)  
TXDLY = 0 (No TXCLK Delay)

**Ethernet PHY (RTL8211CL)**  
SYNC\_MASTER=(K19I\_MLB) SYNC\_DATE=02/05/2009

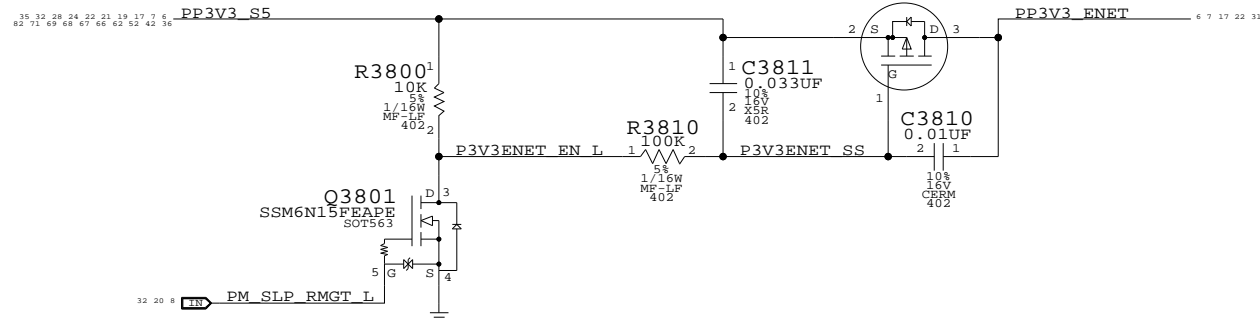
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	REV.
NONE	31	83	

### 3.3V ENET FET

@ 2.5V Vgs:  
 Rds(on) = 90mOhm max  
 I(max) = 1.7A (85C)

CRITICAL  
**Q3810**  
 NTR4101P  
 SOT-23-HF

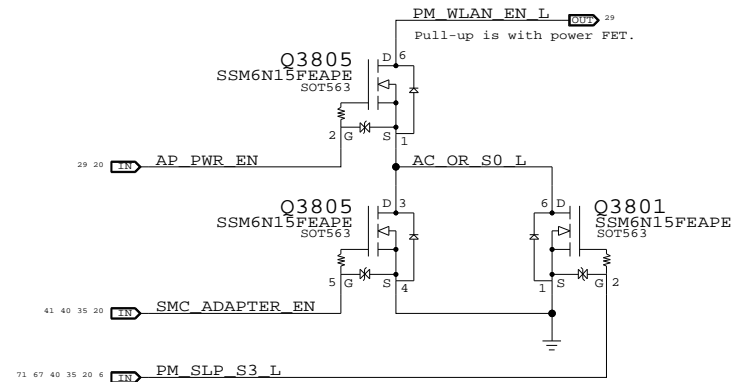


MOBILE:  
 Recommend aliasing PM\_SLP\_RMGT\_L and =P3V3ENET\_EN. Nets separated on ARB for alternate power options.

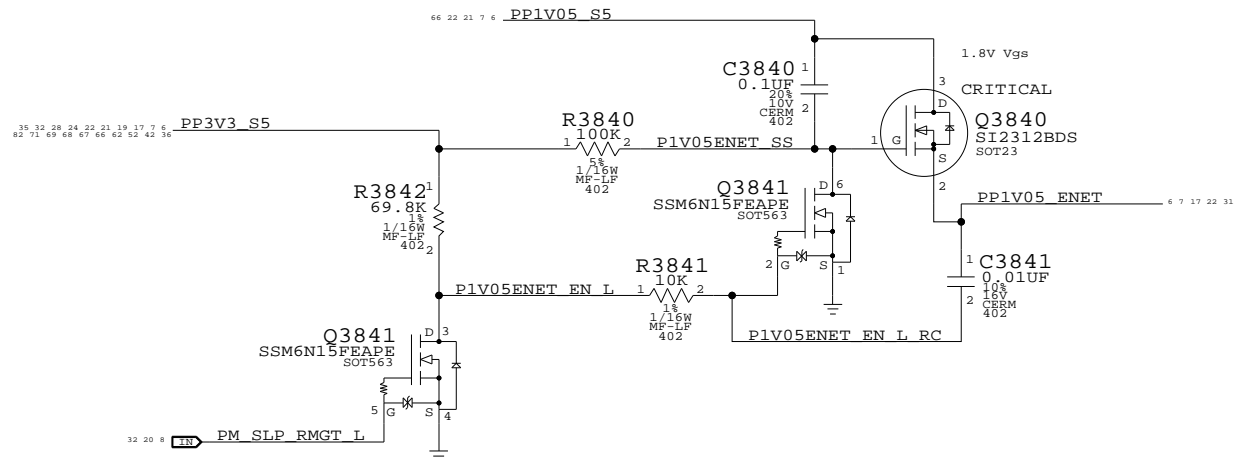
### WLAN Enable Generation

"WLAN" = ("S3" && "AP\_PWR\_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.



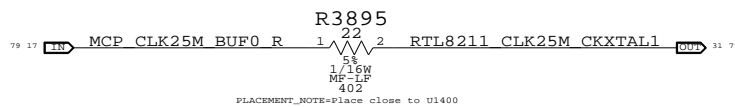
### 1.05V ENET FET



Non-ARB:  
 Recommend aliasing PM\_SLP\_RMGT\_L and =P1V05ENET\_EN. Nets separated on ARB for alternate power options.

### RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMTG rails are powered.  
 Designs must ensure PHY is powered whenever RMTG rails are, or use separate crystal.



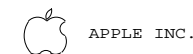
PLACEMENT\_NOTE=Place close to U1400

### Ethernet & AirPort Support

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	32	83

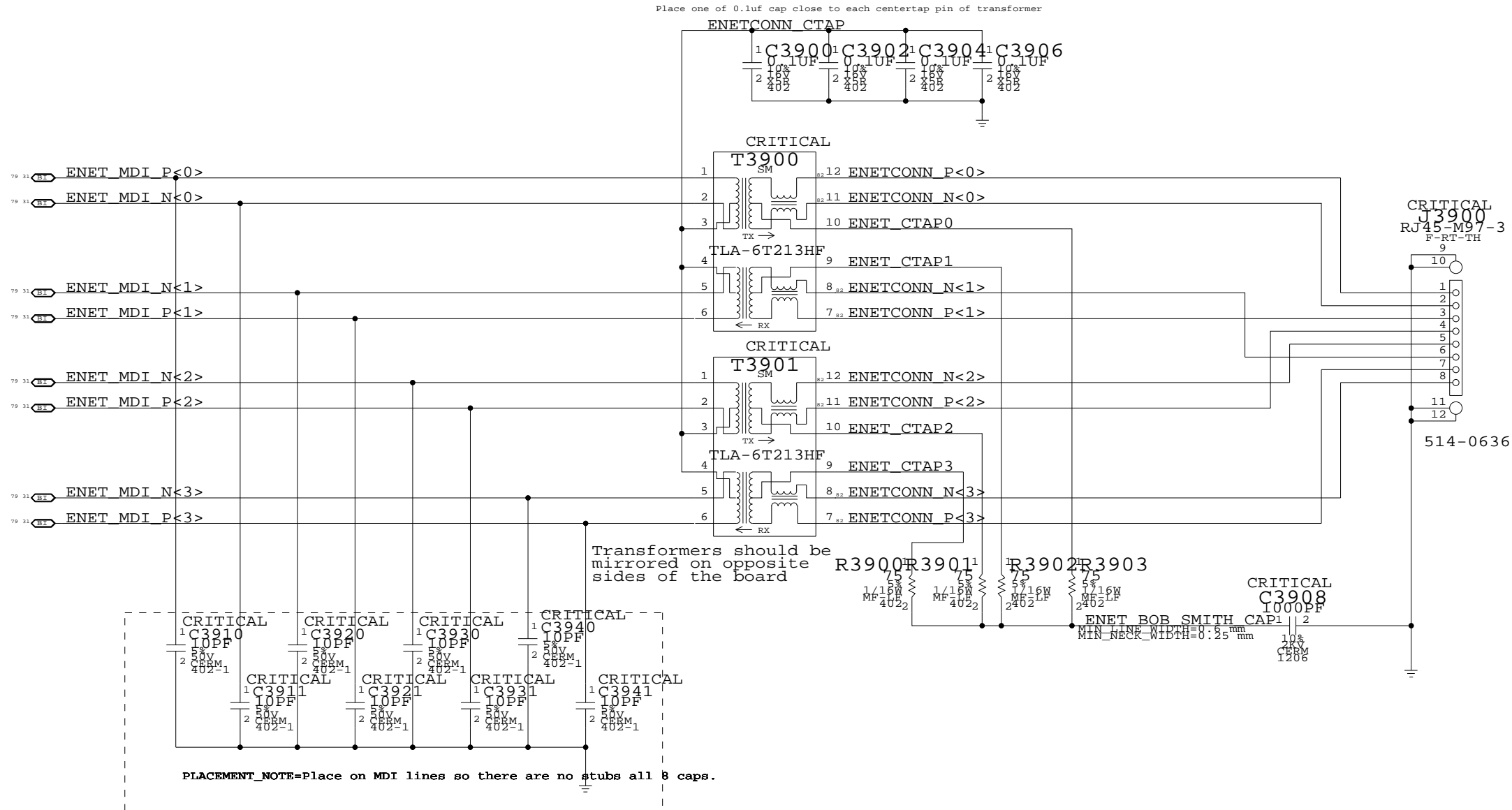


# Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



**Ethernet Connector**

SYNC\_MASTER=K19\_MLB SYNC\_DATE=03/13/2009

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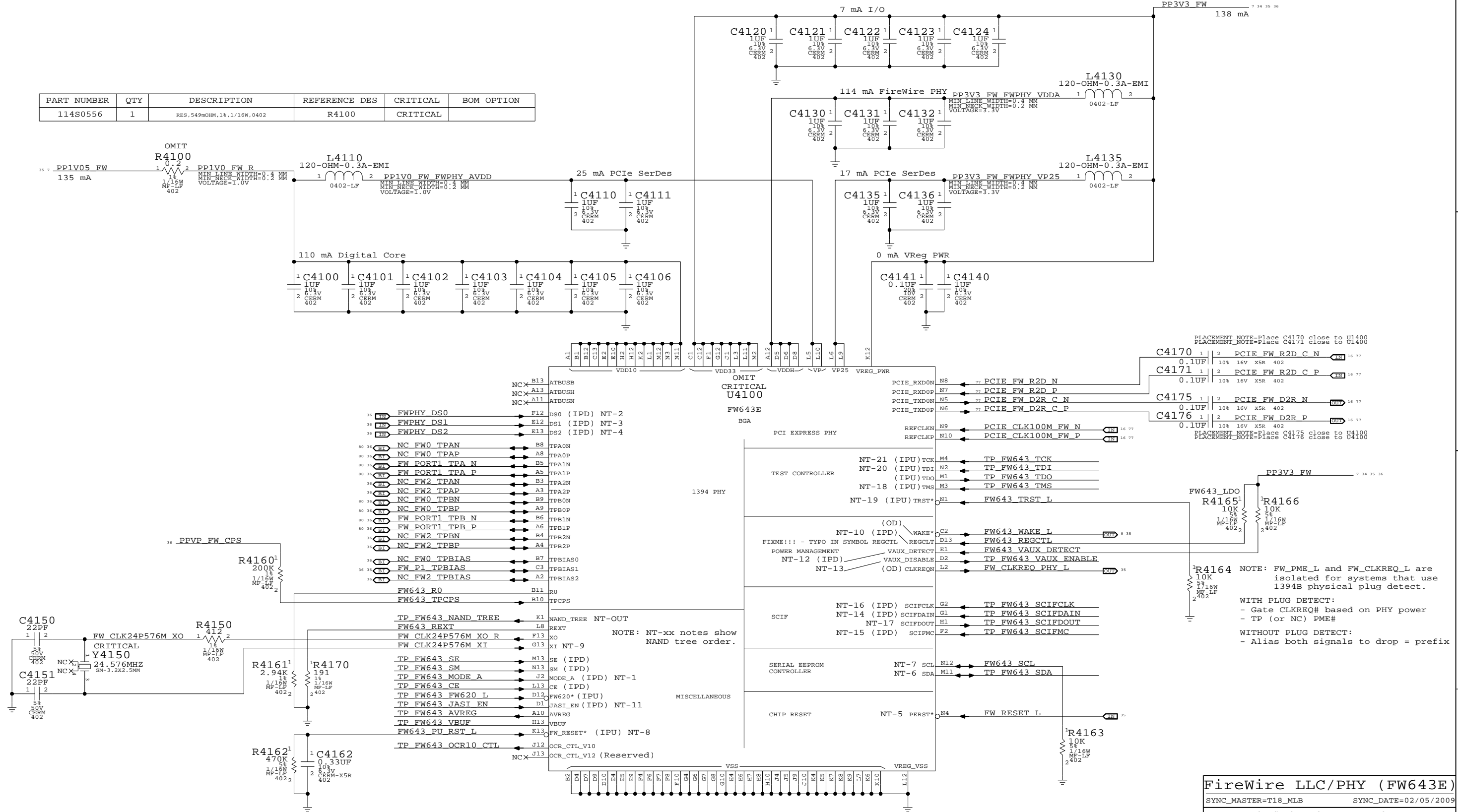
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	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	33	83	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0556	1	RES, 549mOHM, 1%, 1/16W, 0402	R4100	CRITICAL	



**FireWire LLC/PHY (FW643E)**  
 SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	NONE	SHT	OF
		34	83

D

D

C

C

B

B

A

A

Page Notes

Power aliases required by this page:  
 -PPBUS\_S5\_FWPWRSW (system supply for bus power)  
 -PP3V3\_FW\_LATEVG\_ACTIVE  
 -PPVFW\_FWSUMMODE (power passthru summation mode)

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:  
 Rds(on) = 90mOhm max  
 I(max) = 1.7A (85C)

CRITICAL  
 Q4291  
 NTR4101P  
 SOT-23-HF

1.05V FW FET

CRITICAL  
 Q4295  
 SI2312BDS  
 SOT23

FireWire Port Power Switch

Late-VG Event Detection

FWLATEVG Hysteresis:  
 3.08V when port power is on  
 2.91V when late Vg event and port power is off

FireWire Port Power

NOTICE OF PROPRIETARY PROPERTY

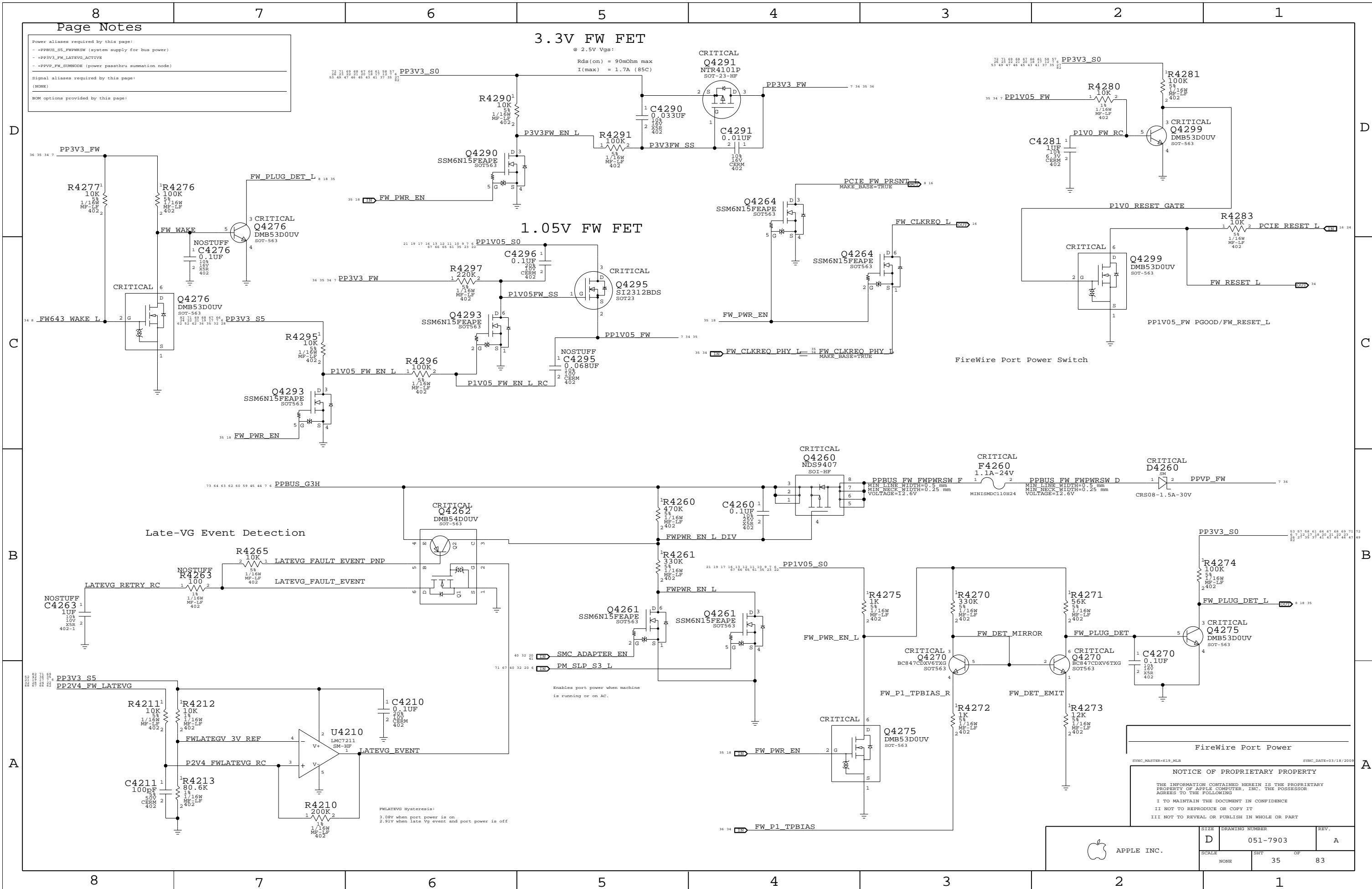
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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	35	83



Page Notes

Power aliases required by this page:  
 - =PPVP\_FW\_PORT1  
 - =PP3V3\_FW\_LATEVG

Signal aliases required by this page:  
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

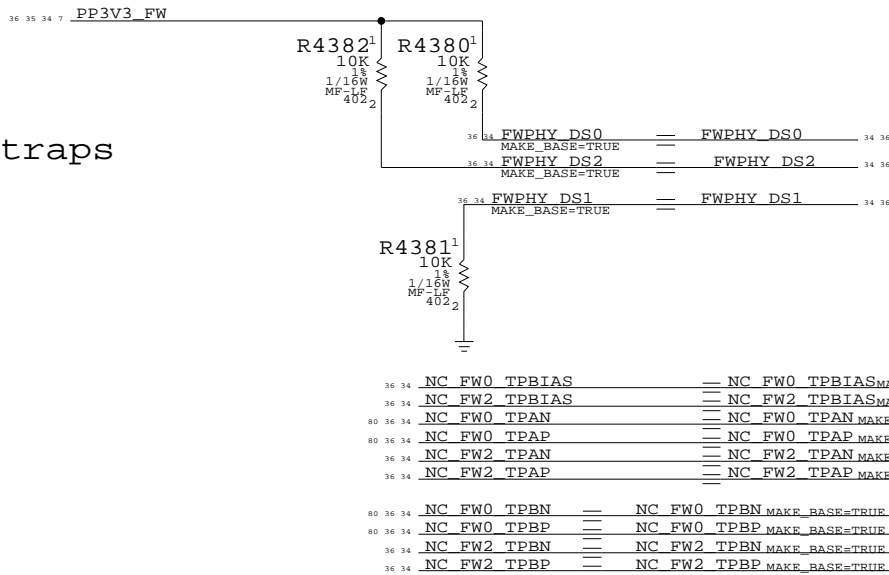
BOM options provided by this page:  
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

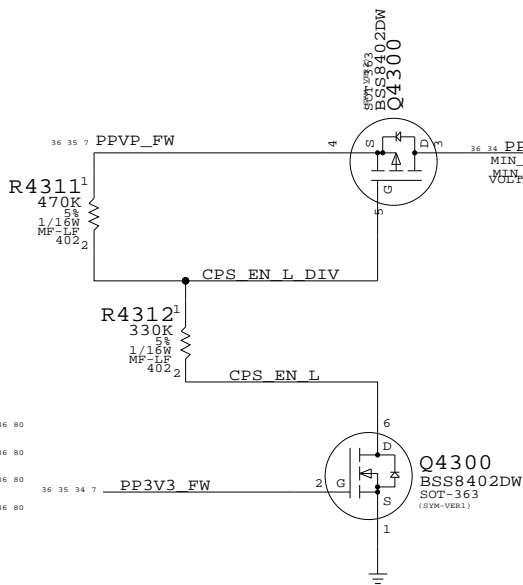
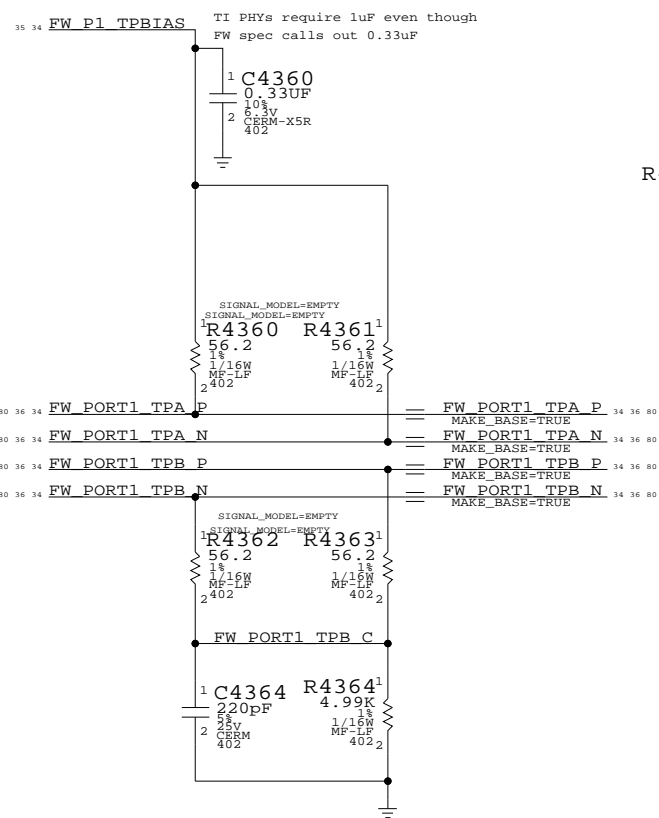
FireWire PHY Config Straps

Configures PHY for:  
 - 1-port Portable Power Class (0)  
 - Port "1" Bilingual (1394B)

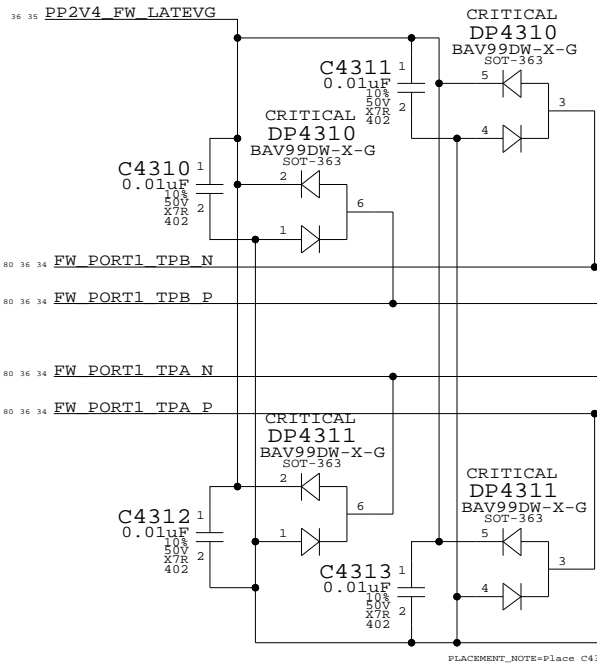


Termination

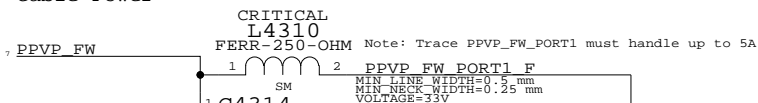
Place close to FireWire PHY



"Snapback" & "Late VG" Protection

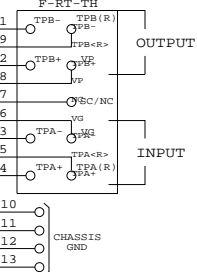


Cable Power



PORT 1 BILINGUAL

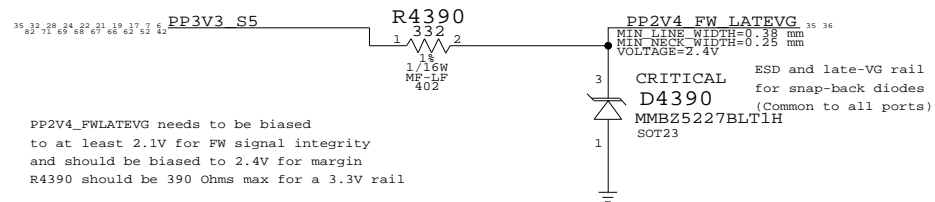
CRITICAL J4310 1394B-M97 F-RT-TH



514S0605

AREF needs to be isolated from all local grounds per 1394b spec  
 When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)  
 BREF should be hard-connected to logic ground for speed signaling and connection

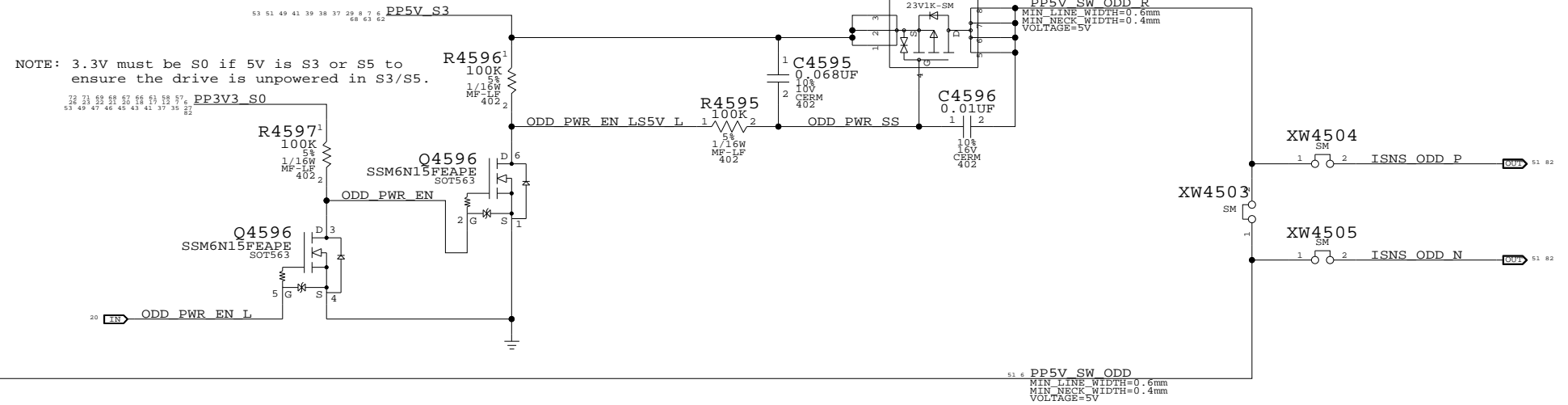
Late-VG Protection Power



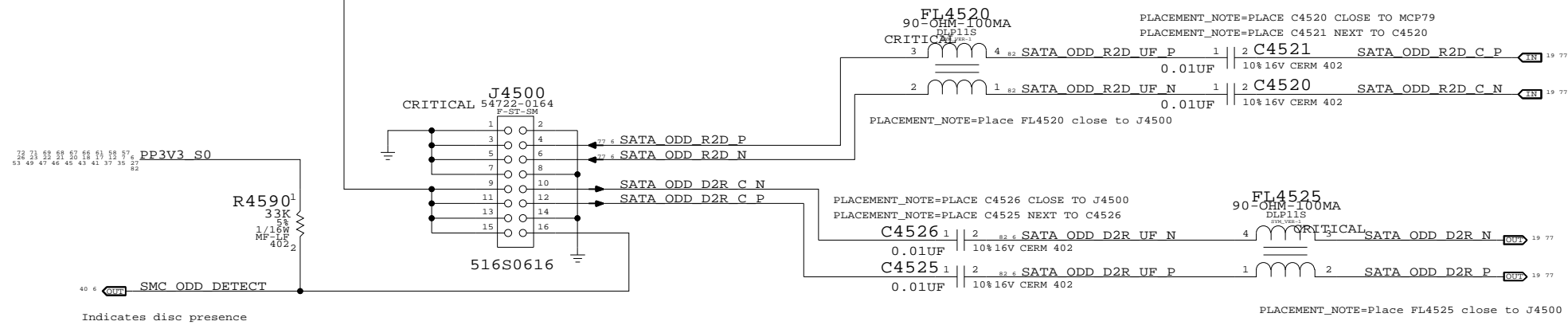
FireWire Ports		
SYNC_MASTER=K19_MLB	SYNC_DATE=02/05/2009	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	83
NONE	36		

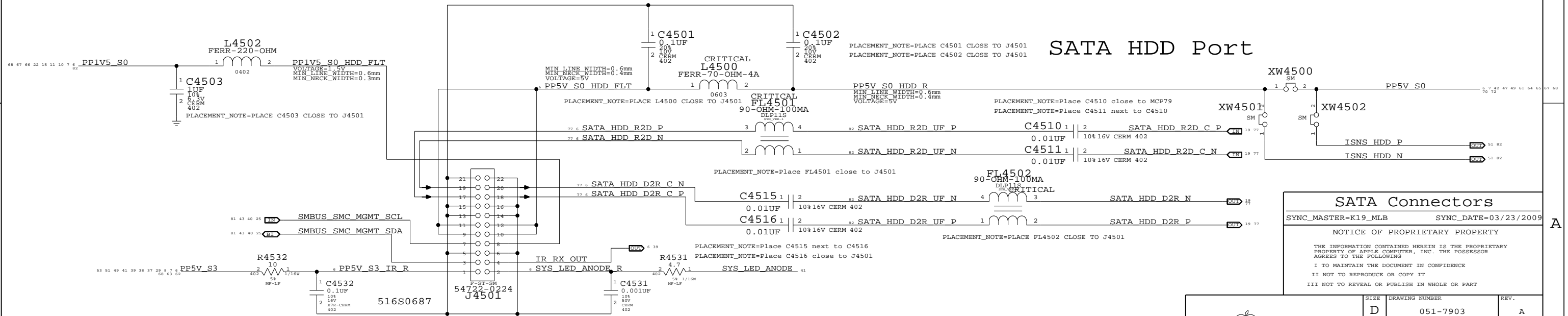
# ODD Power Control



# SATA ODD Port

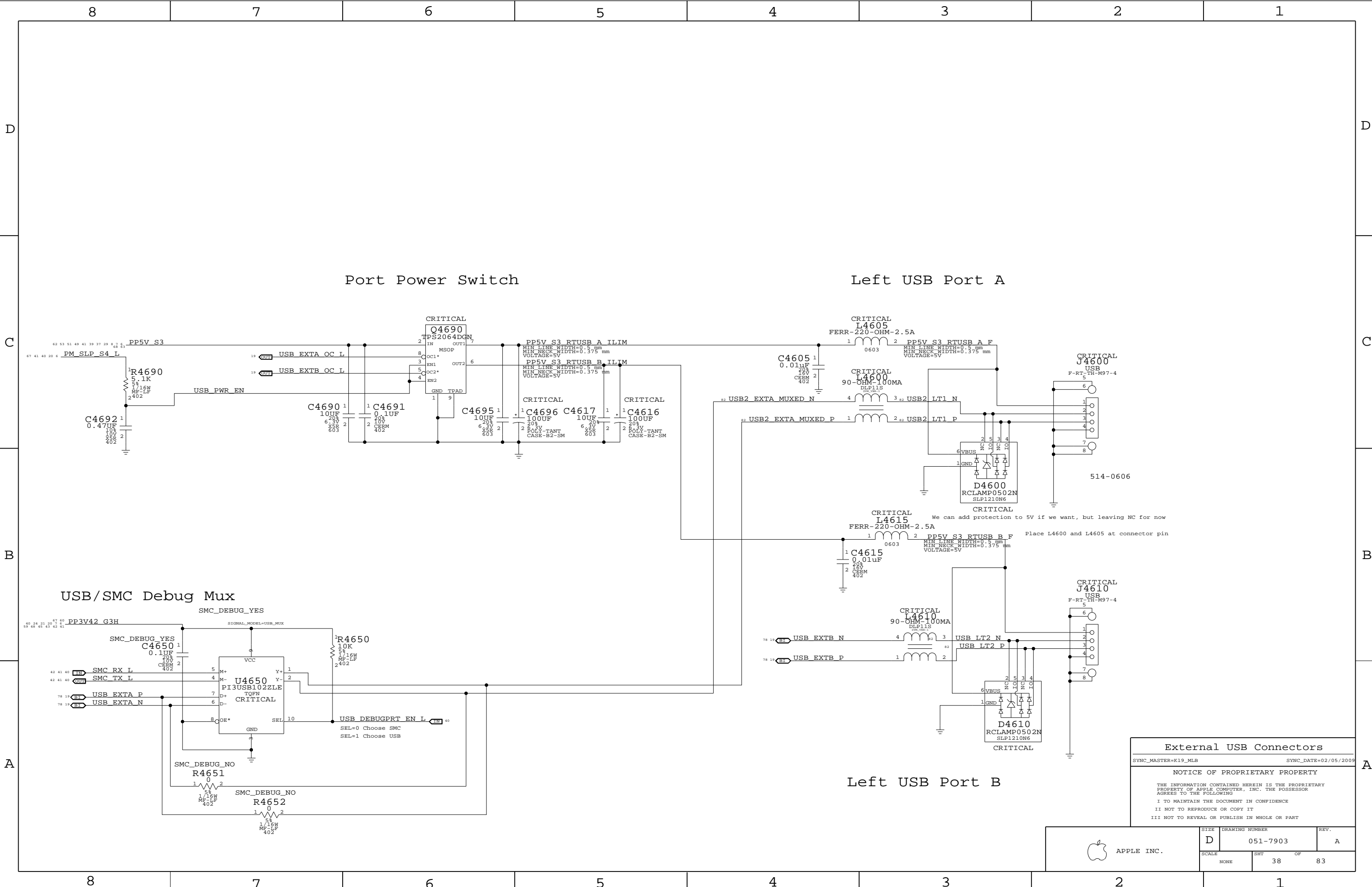


# SATA HDD Port



**SATA Connectors**  
 SYNC\_MASTER=K19\_MLB SYNC\_DATE=03/23/2009  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	REV.
NONE	37	83	



Port Power Switch

Left USB Port A

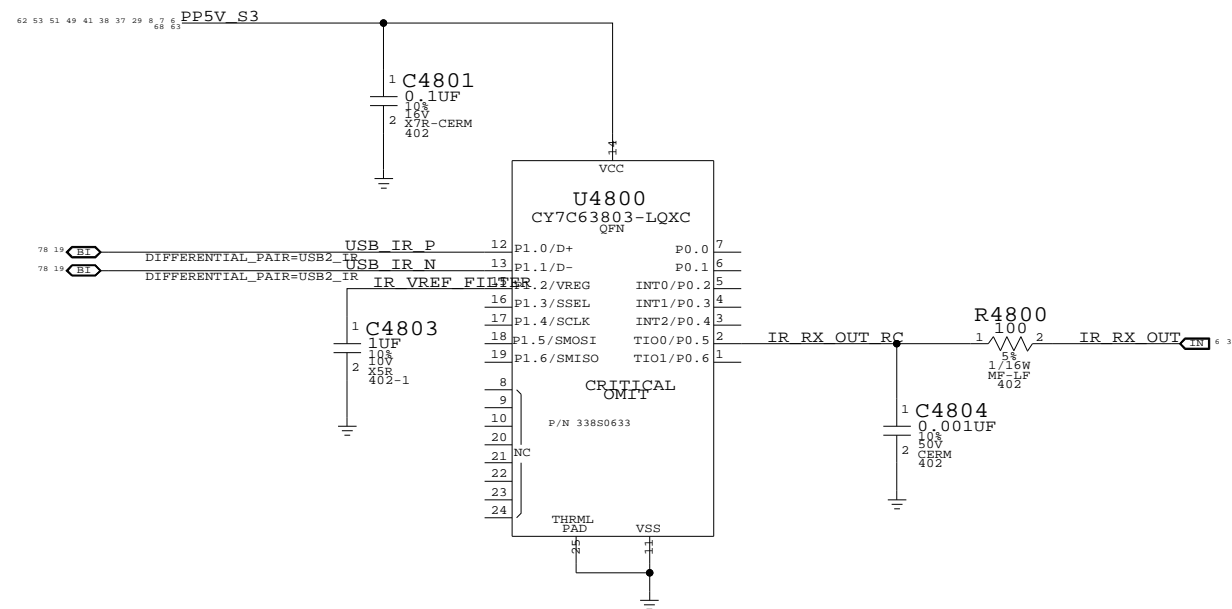
USB/SMC Debug Mux

Left USB Port B

**External USB Connectors**  
 SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	38	83	

# IR SUPPORT



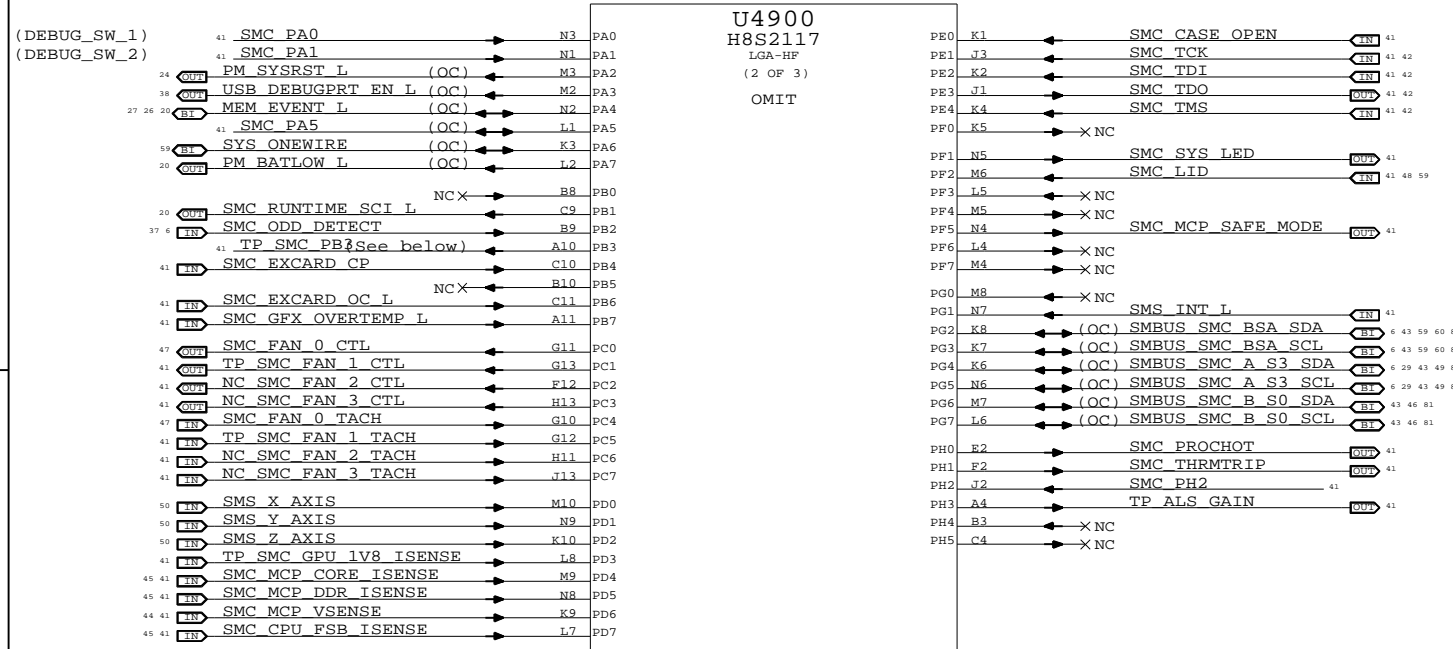
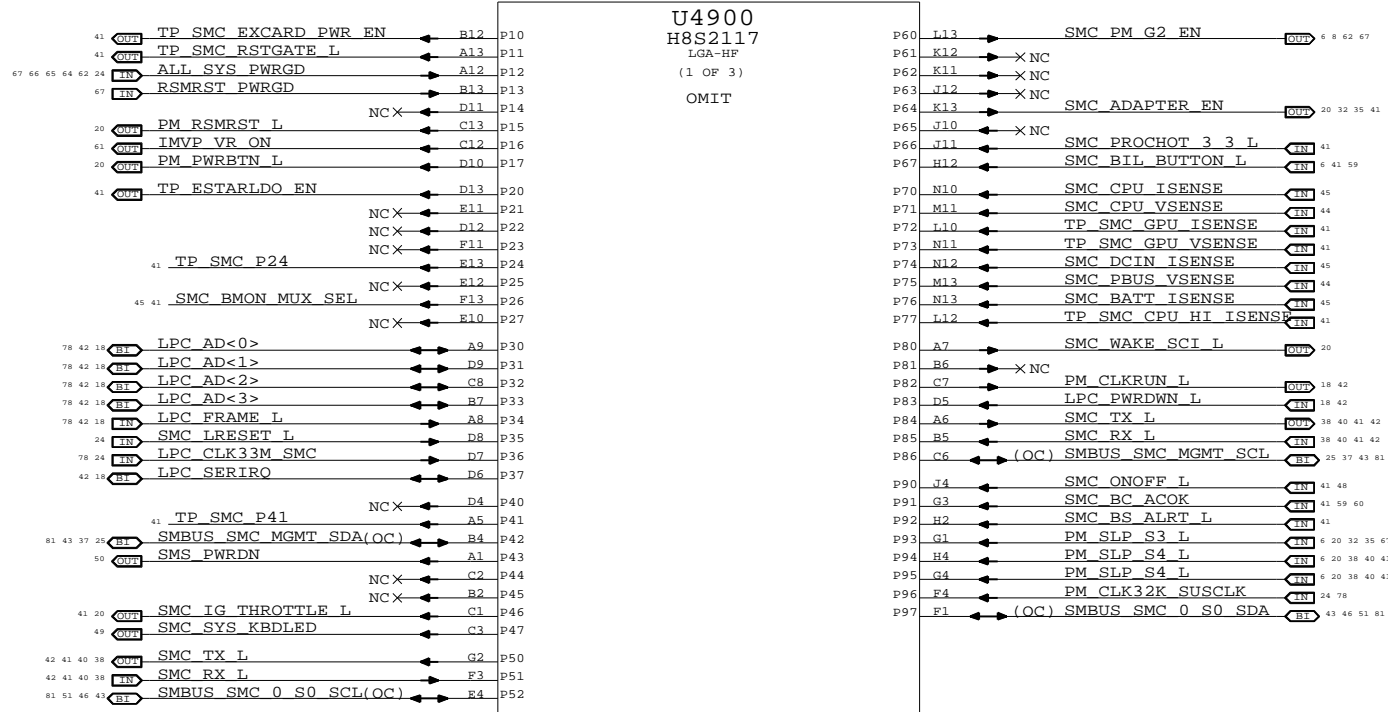
Front Flex Support

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009

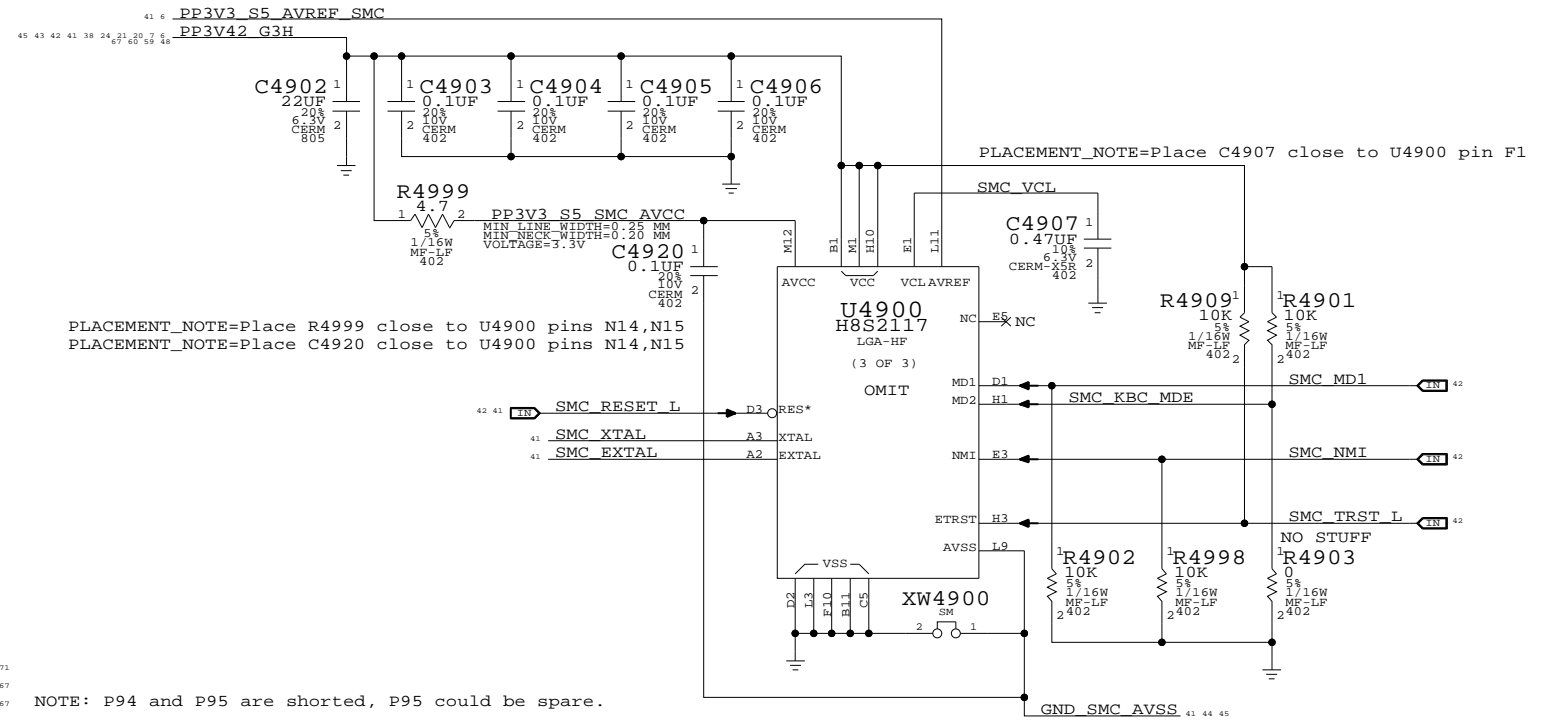
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	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT OF		
NONE	39 OF		83

NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC\_PB3:  
SMC\_IG\_THROTTLE\_L for MG systems.  
Otherwise, TP/NC okay (was ISENSE\_CAL\_EN)



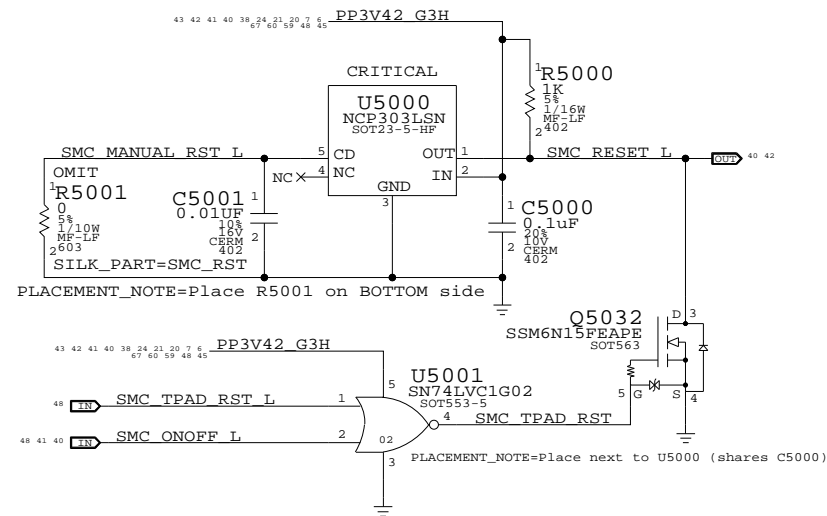
NOTE: SMS Interrupt can be active high or low, rename net accordingly.  
If SMS interrupt is not used, pull up to SMC rail.

SMC  
SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009  
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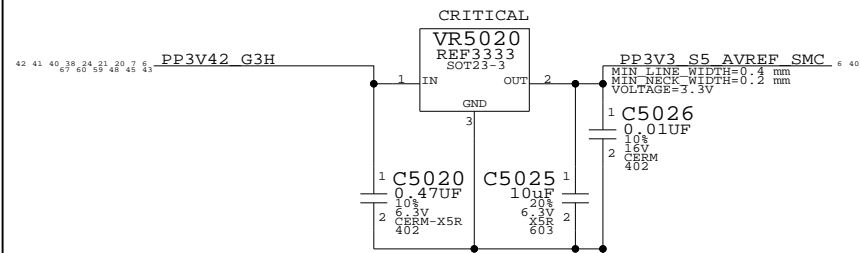
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	40		83



### SMC Reset "Button" / Brownout Detect

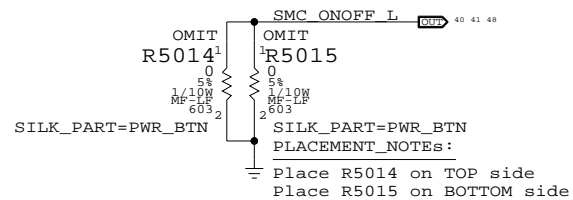


### SMC AVREF Supply

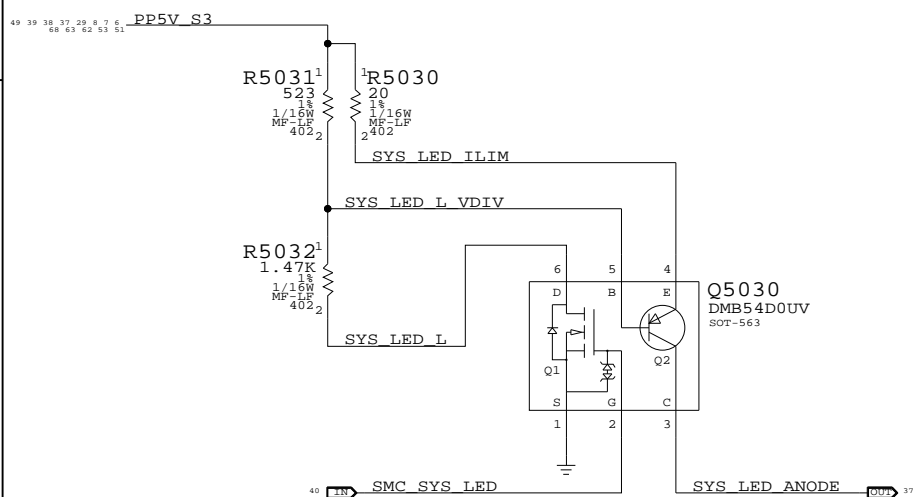


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

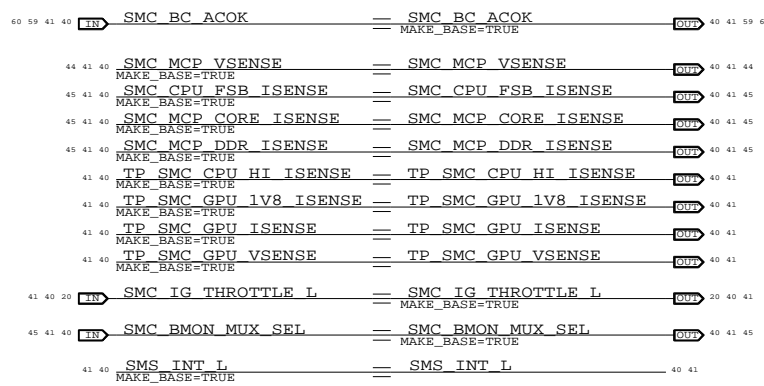
### Debug Power "Buttons"



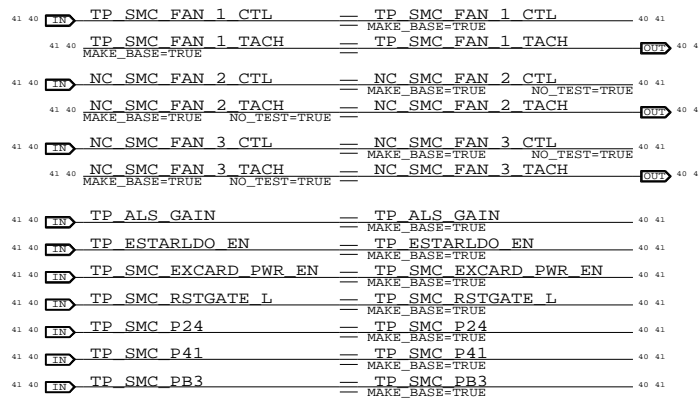
### System (Sleep) LED Circuit



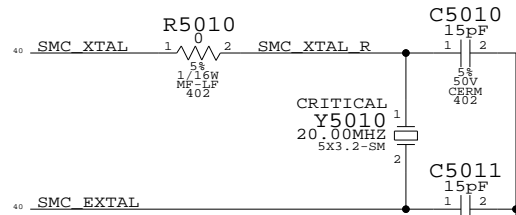
### SMC Aliases



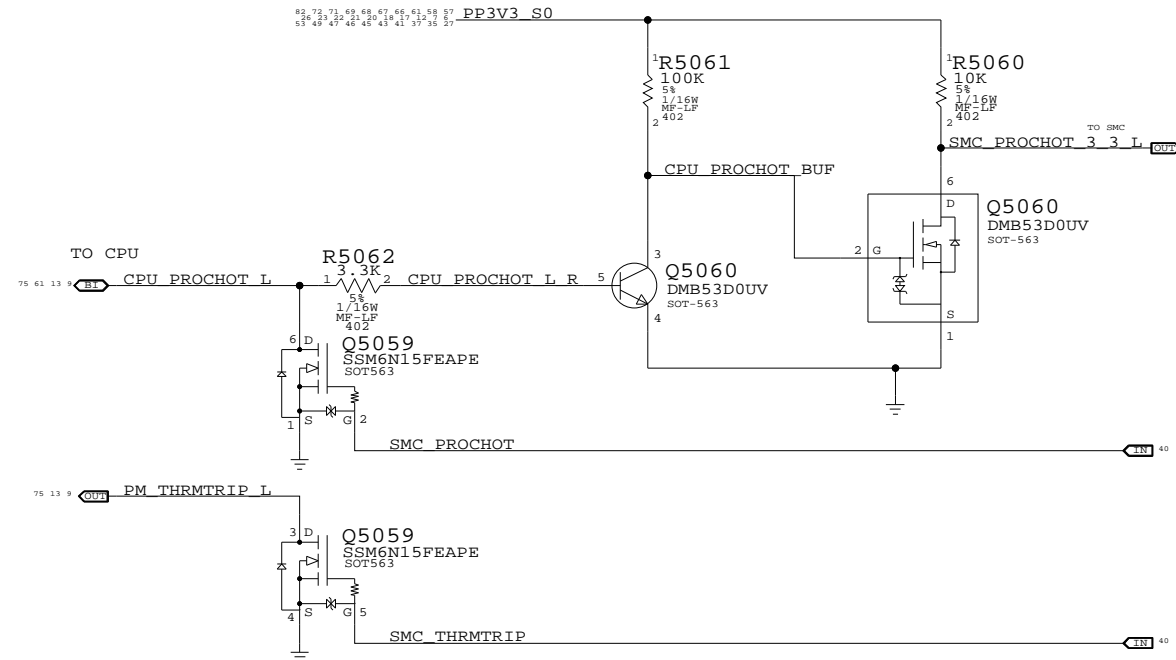
### Unused Pins



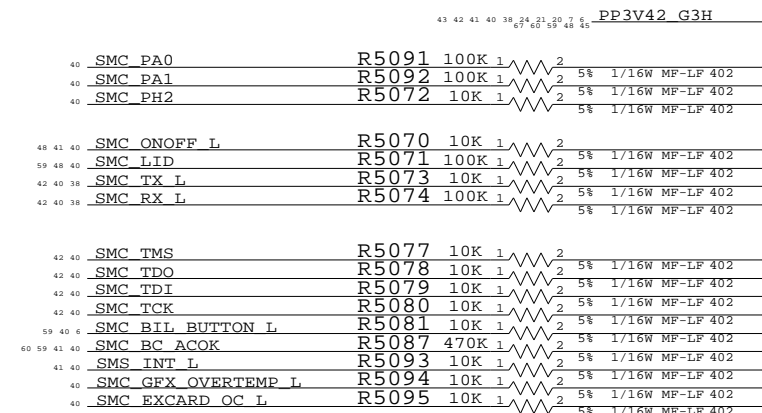
### SMC Crystal Circuit



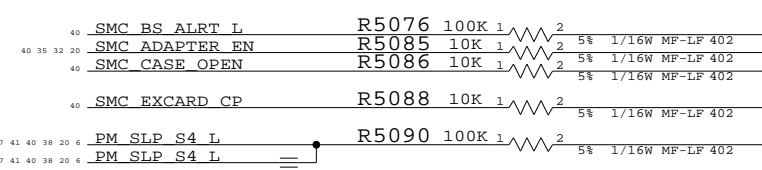
### SMC FSB to 3.3V Level Shifting



### SMC Pull-ups



### SMC Pull-downs



### SMC Support

SYNC\_MASTER=(K19\_MLB) SYNC\_DATE=(11/25/2008)

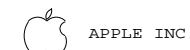
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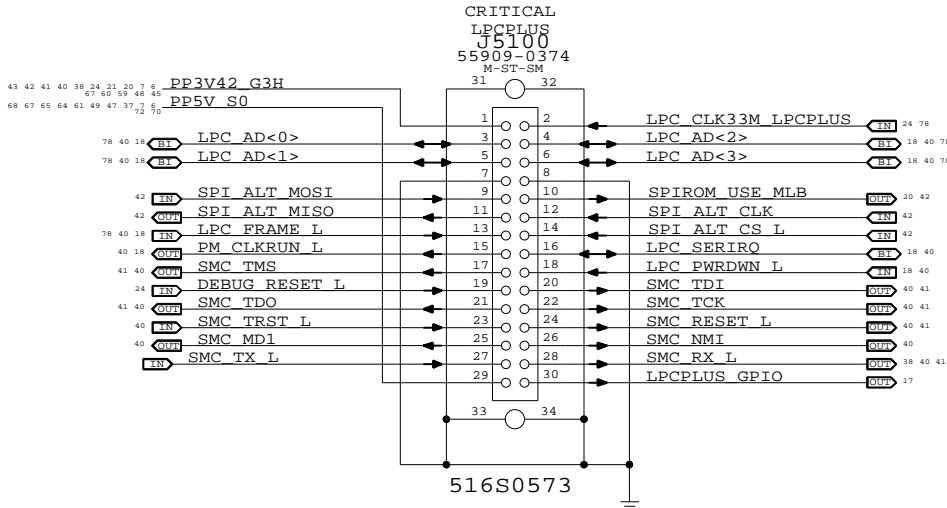
SIZE DRAWING NUMBER REV.

D 051-7903 A

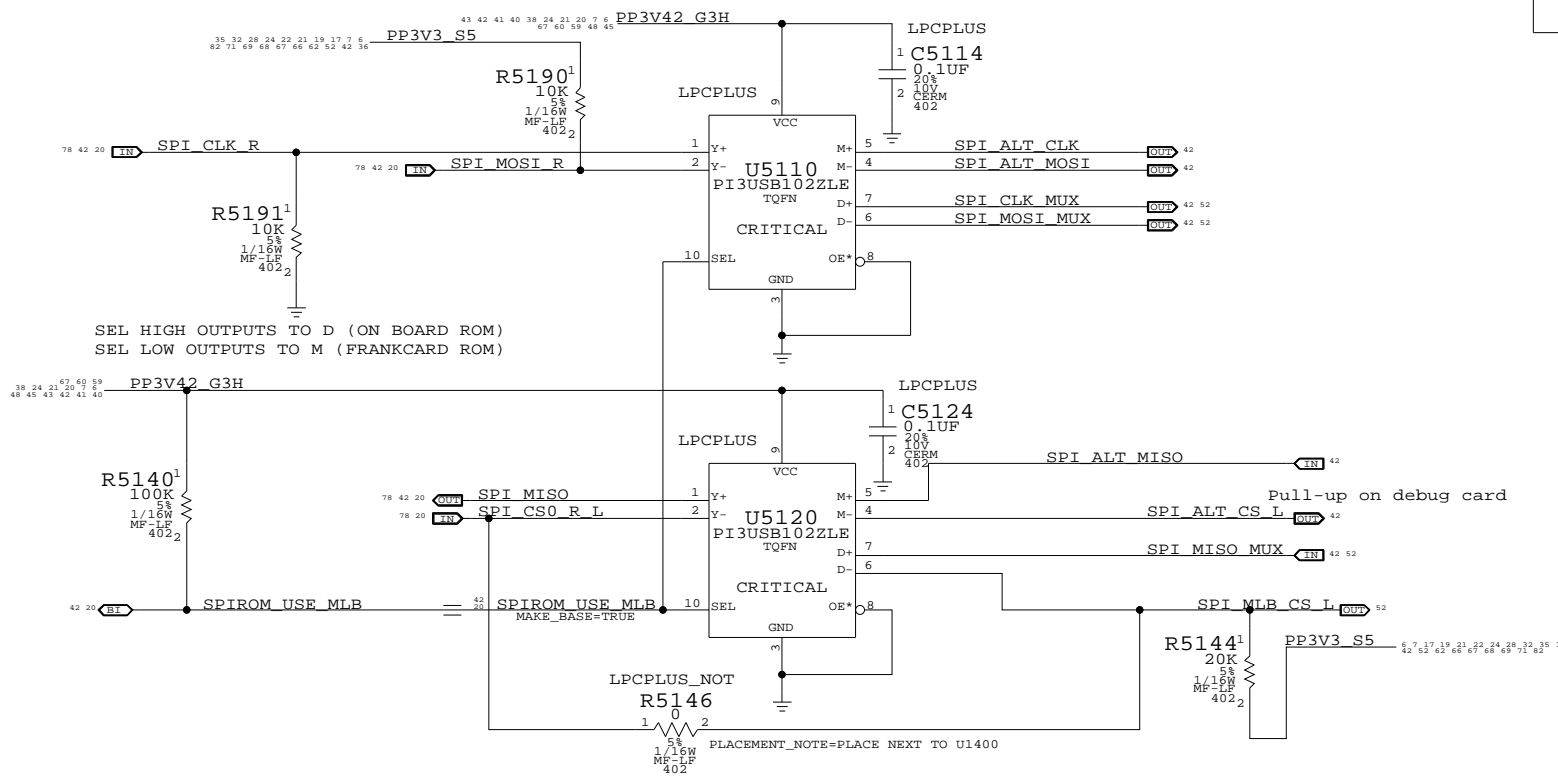
SCALE SHEET OF

NONE 41 OF 83

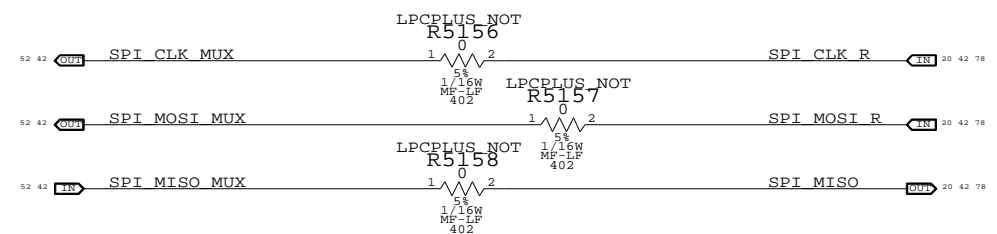
### LPC+SPI Connector



### Alternate SPI ROM Support



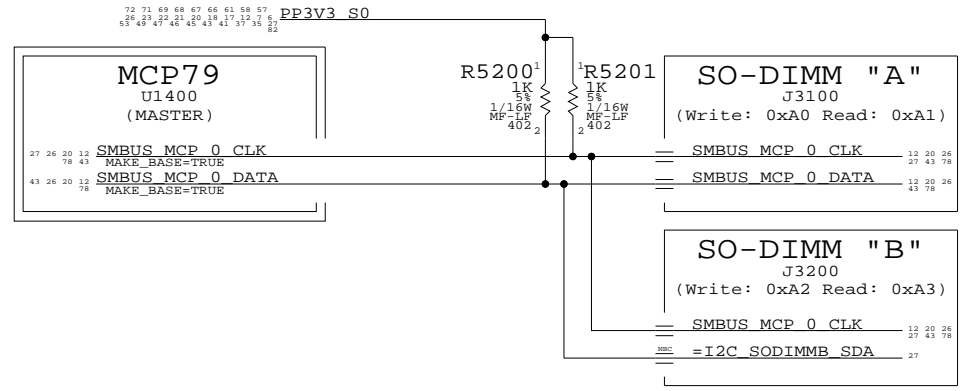
### SPI MUX BYPASS



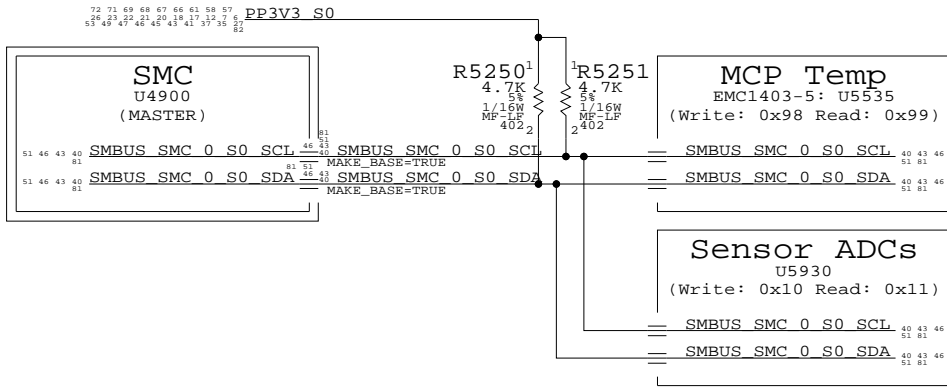
**LPC+SPI Debug Connector**  
 SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	42	83	

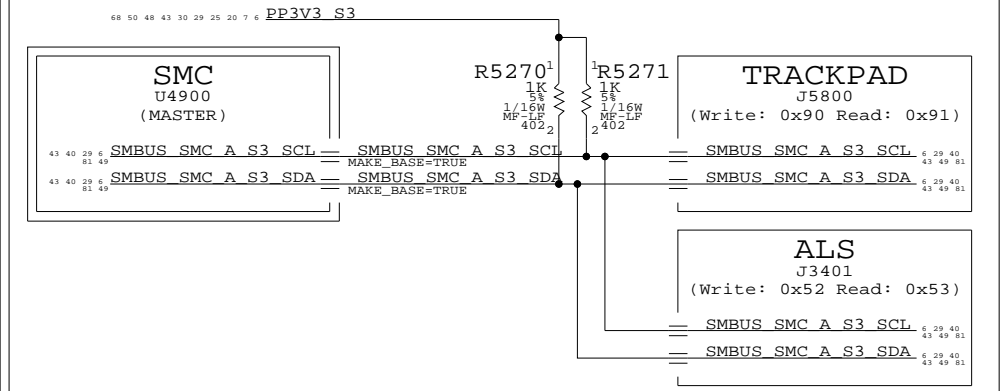
### MCP79 SMBUS "0" CONNECTIONS



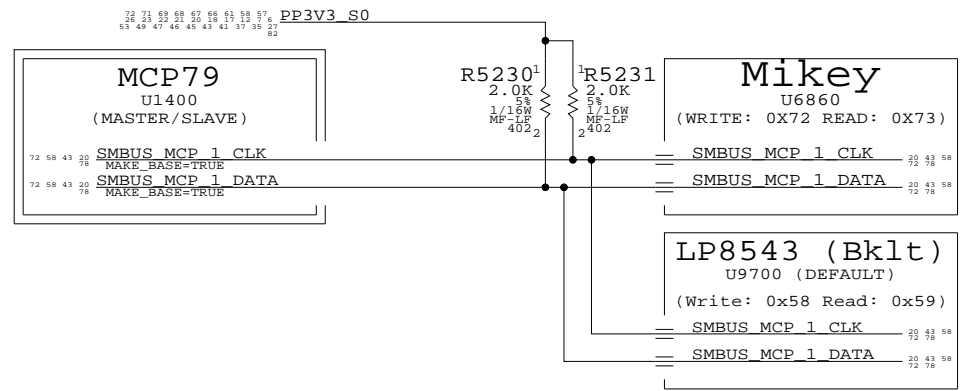
### SMC "0" SMBus Connections



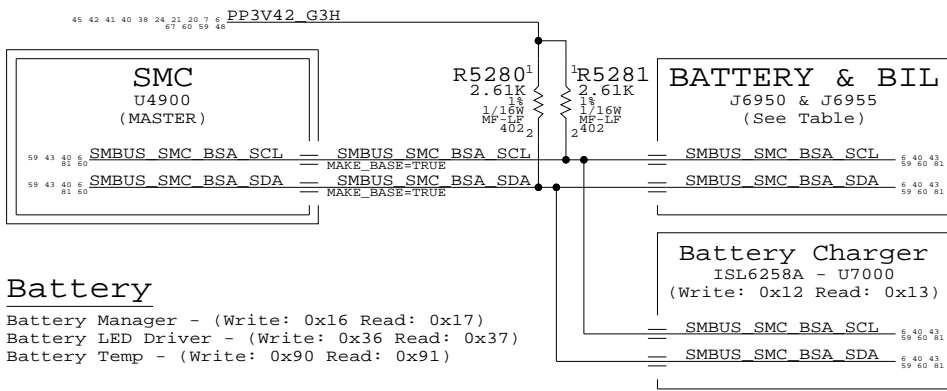
### SMC "A" SMBus Connections



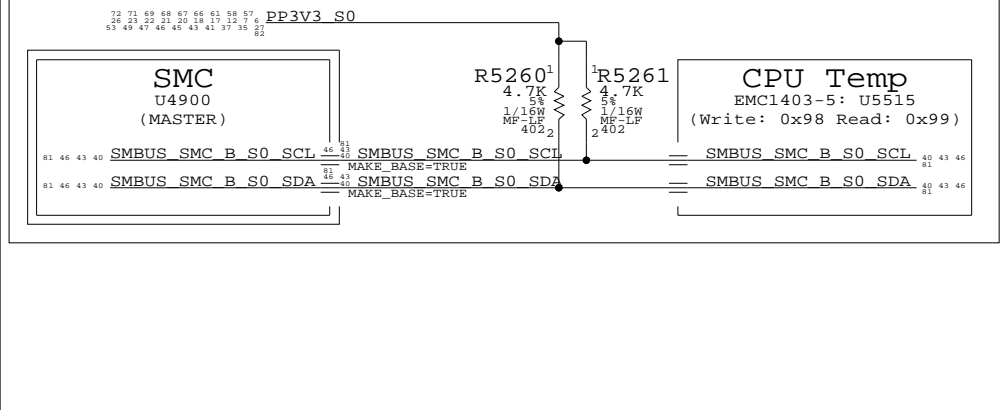
### MCP79 SMBUS "1" CONNECTIONS



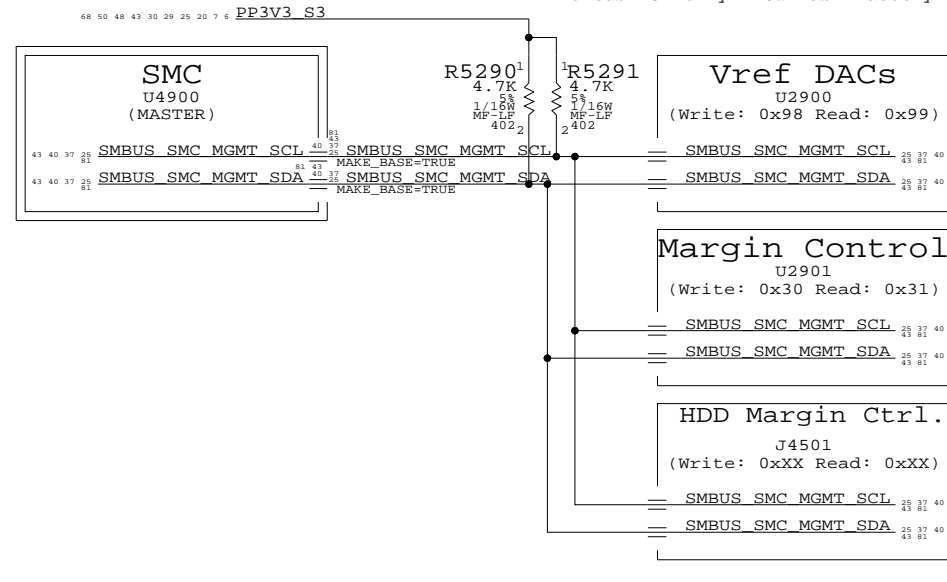
### SMC "Battery A" SMBus Connections



### SMC "B" SMBus Connections



### SMC "Management" SMBus Connections



### K19i SMBus Connections

SYNC\_MASTER=WFERRY\_K19I SYNC\_DATE=12/12/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	43	83

8

7

6

5

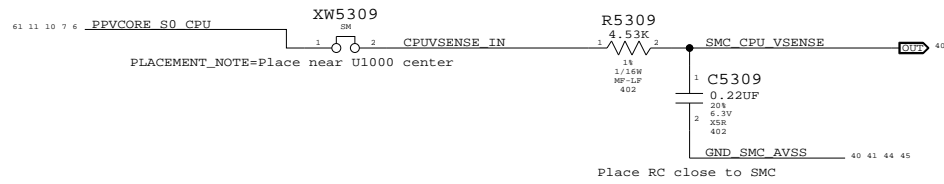
4

3

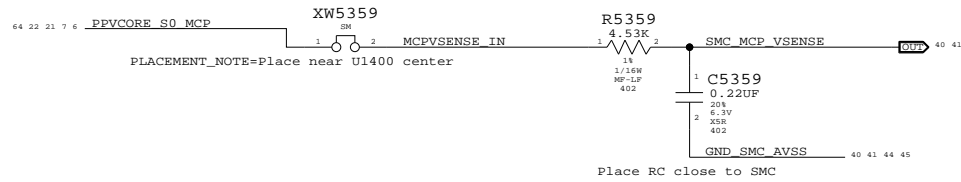
2

1

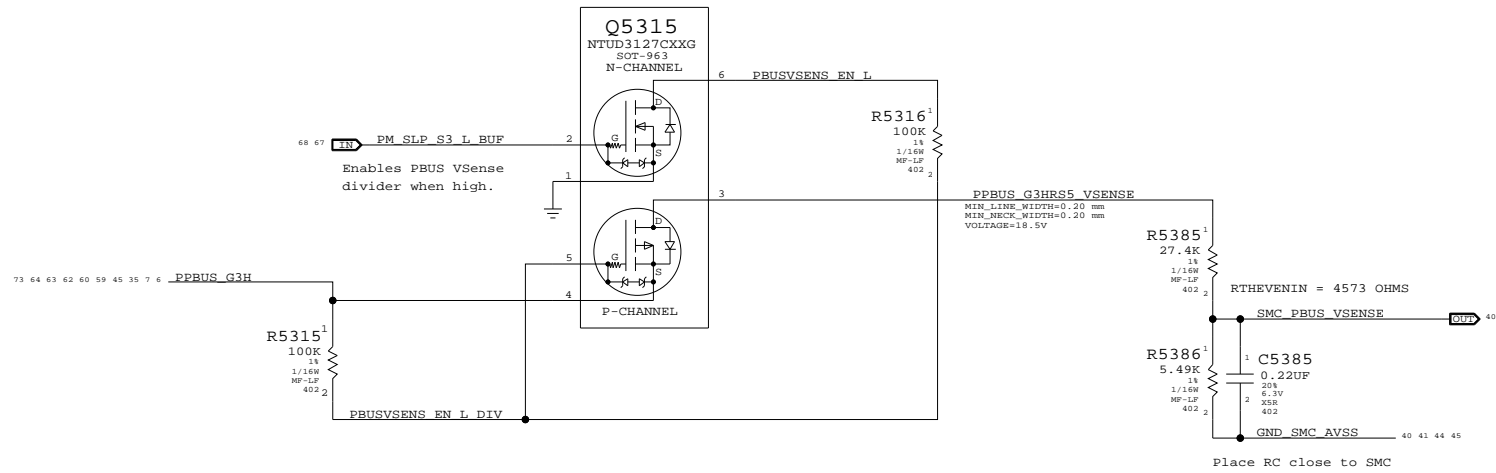
### CPU Voltage Sense / Filter



### MCP Voltage Sense / Filter



### PBUS VOLTAGE SENSE ENABLE & FILTER



### VOLTAGE SENSING

SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/05/2009

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SIZE DRAWING NUMBER REV.

D 051-7903 A

SCALE NONE SHEET 44 OF 83

8

7

6

5

4

3

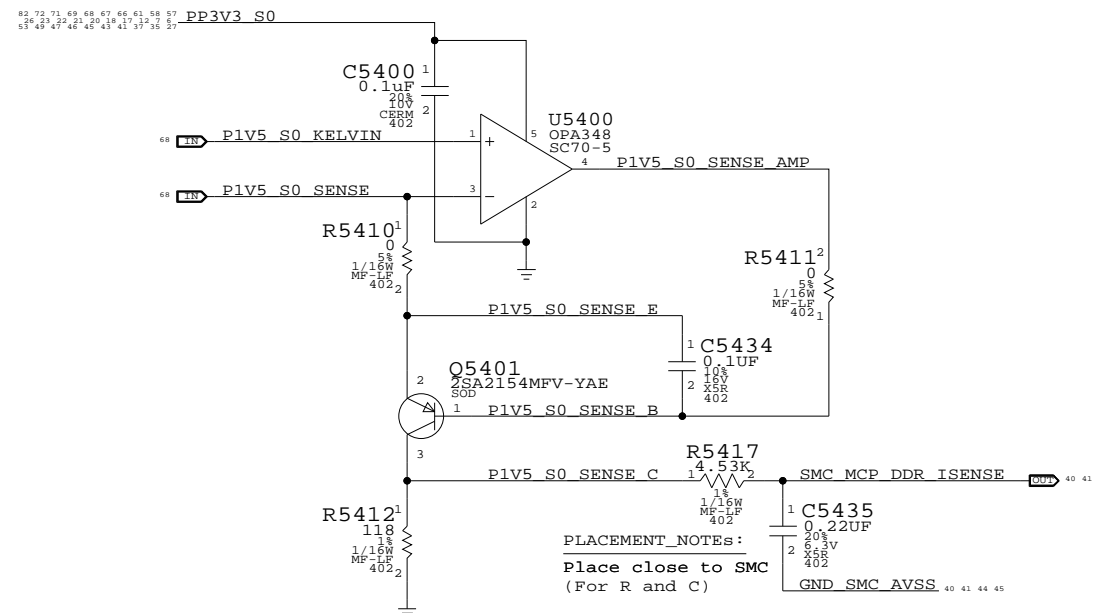
2

1

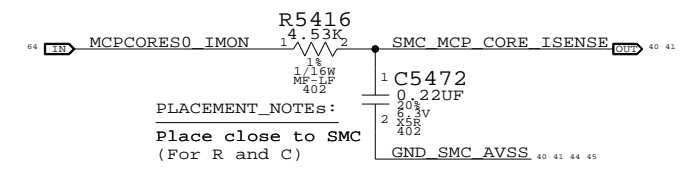
D

D

MCP MEM VDD Current Sense / Filter



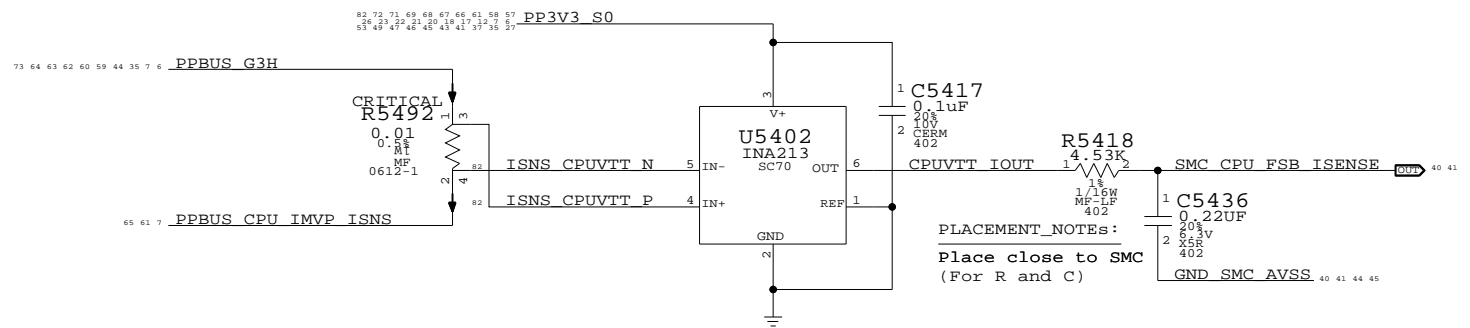
MCP VCore Current Sense Filter



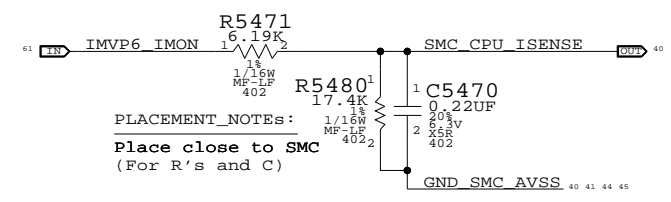
C

C

MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



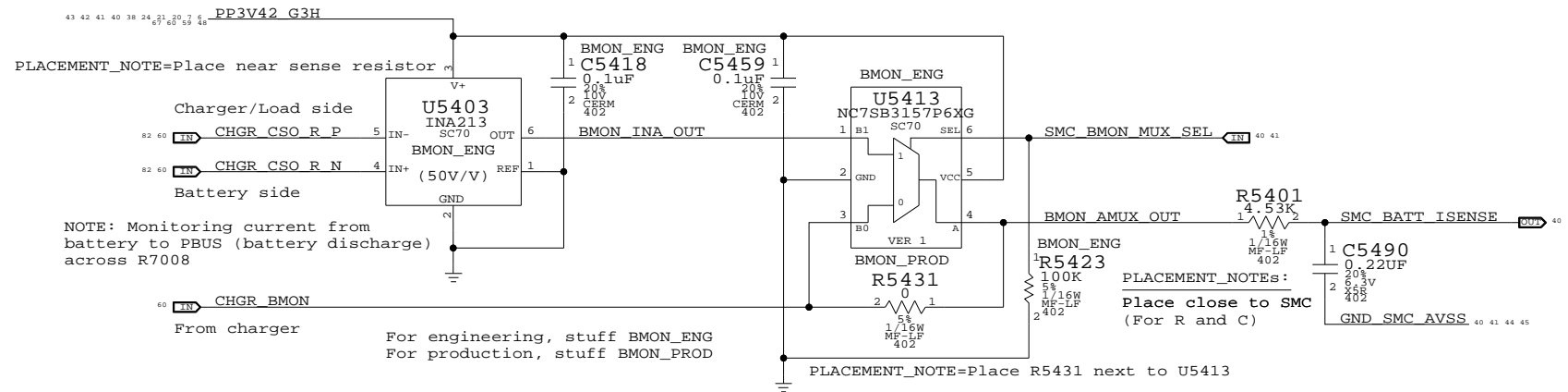
CPU VCore Load Side Current Sense / Filter



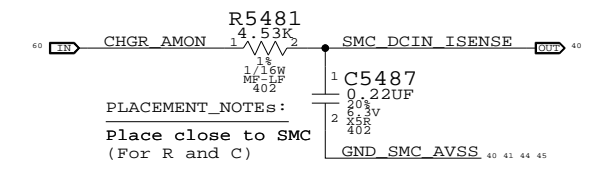
B

B

Battery (BMON) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



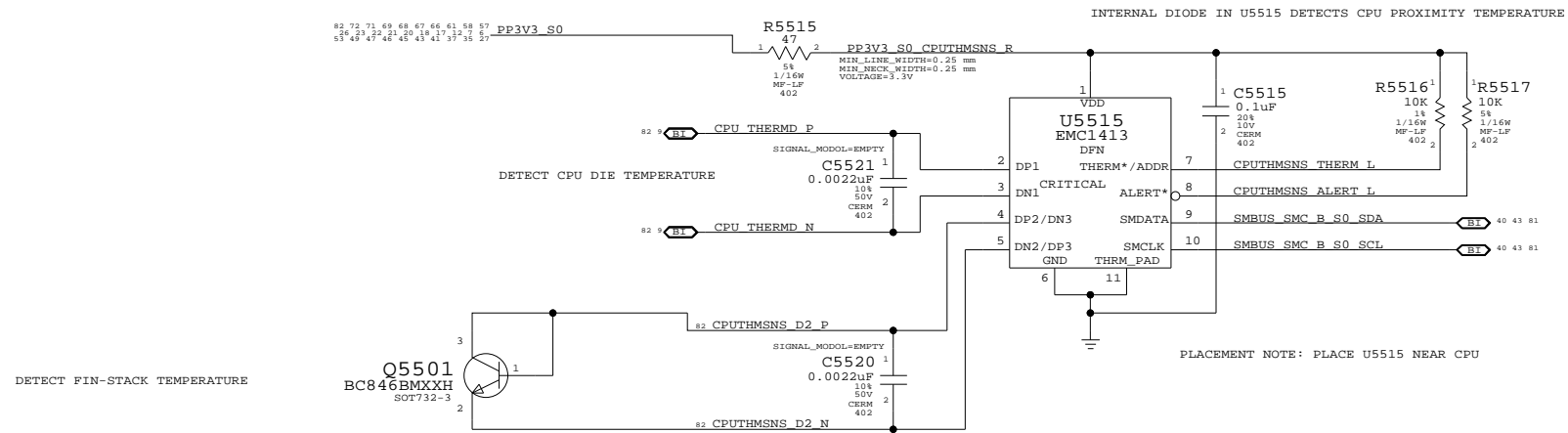
A

A

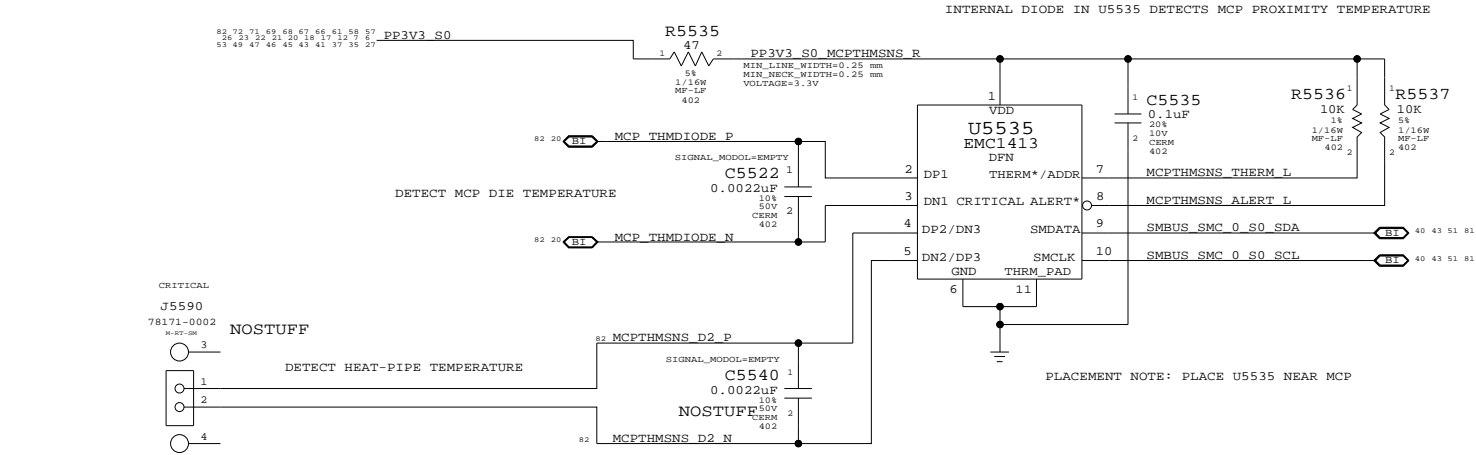
**Current Sensing**  
 SYNC\_MASTER=WFERRY\_K19I SYNC\_DATE=12/16/2008  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	45		83

### CPU T-Diode Thermal Sensor



### MCP T-Diode Thermal Sensor



**Thermal Sensors**

SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/05/2009

**NOTICE OF PROPRIETARY PROPERTY**

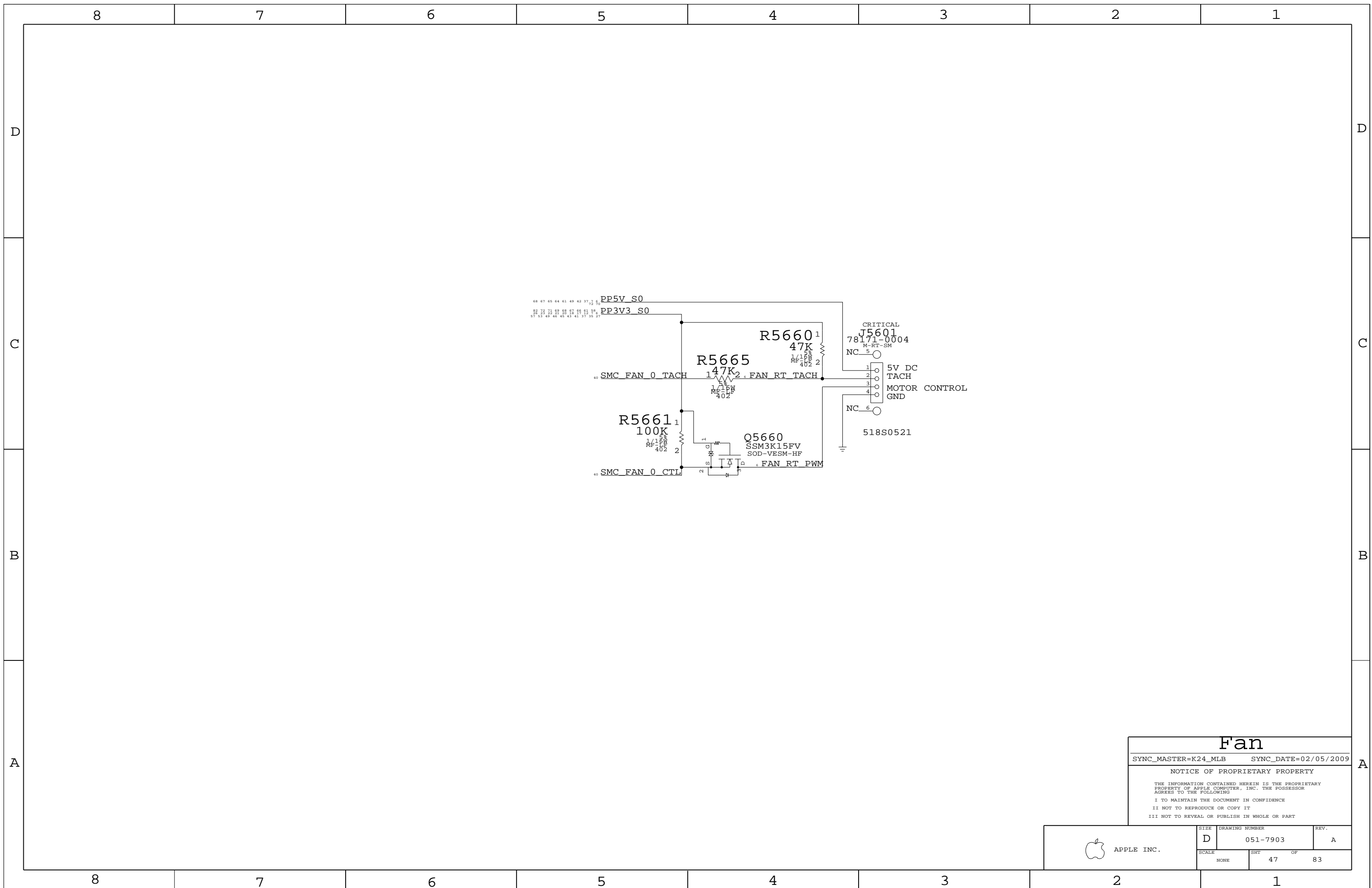
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	46	83	



**Fan**

SYNC\_MASTER=K24\_MLB      SYNC\_DATE=02/05/2009


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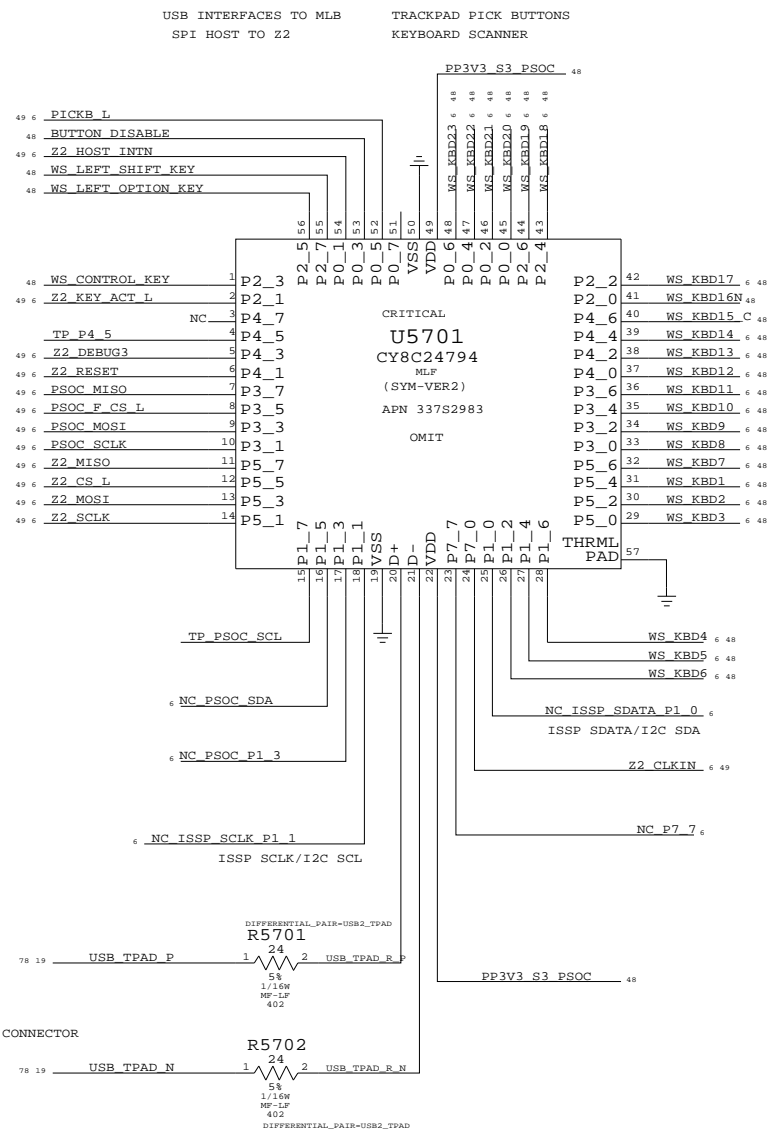
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

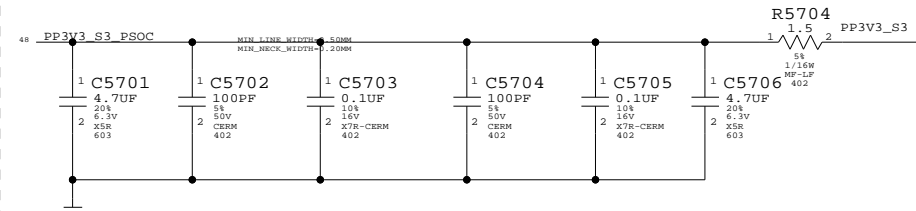
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT OF		
NONE	47	83	

### PSOC USB CONTROLLER

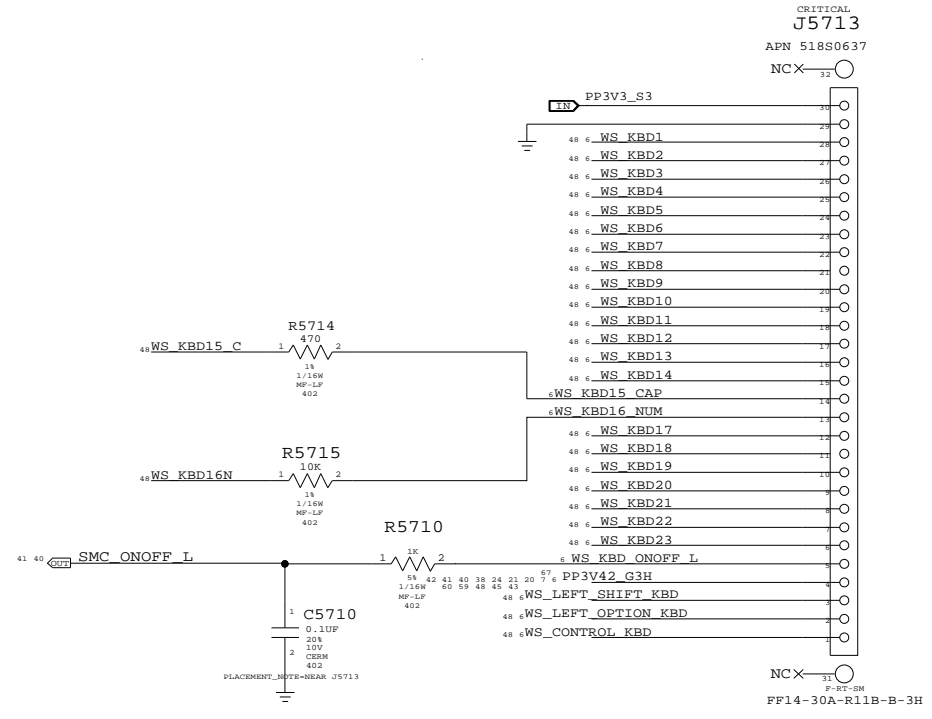


U5701 CHIP DECOUPLING  
 PLACE C5701, C5702 & C5703 CLOSE TO U5701 VDD PIN 22  
 PLACE C5704, C5705 & C5706 CLOSE TO U5701 VDD PIN 49

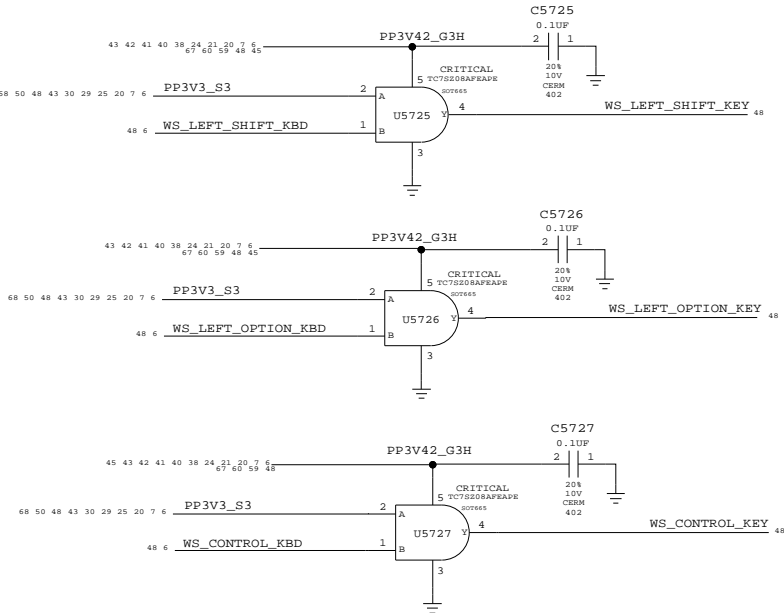


IC	PIN NAME	CURRENT	R_SMS	V_SMS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A		0.204 V	16.32E-6 W
	VOUT	60MA MAX	10 OHM	0.6 V	36E-3 W
PSOC	VDD	60MA MAX	0.2 OHM	0.012 V	0.72E-6 W
	VDD	8MA (TVP)	1.5 OHM	0.012 V	96E-6 W
1.8V BOOSTER	VDD	14MA (MAX)		0.021 V	294E-6 W
	VIN	49A (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

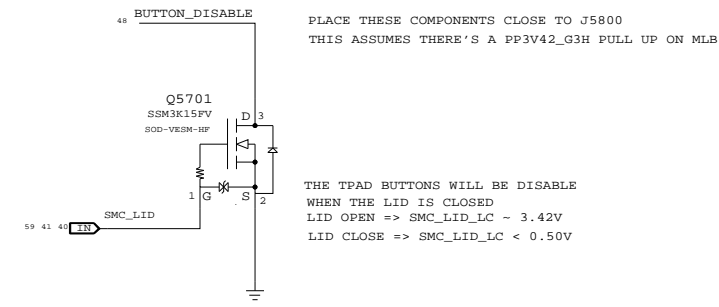
### KEYBOARD CONNECTOR



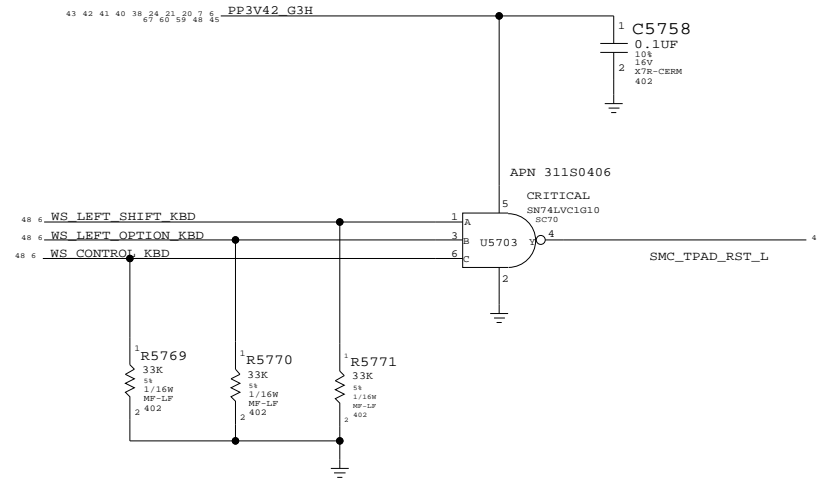
### ISOLATION CIRCUIT



### TPAD BUTTONS DISABLE



### SMC\_MANUAL\_RESET LOGIC



### Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	REF PART AS ALTERNATE

### WELLSPRING 1

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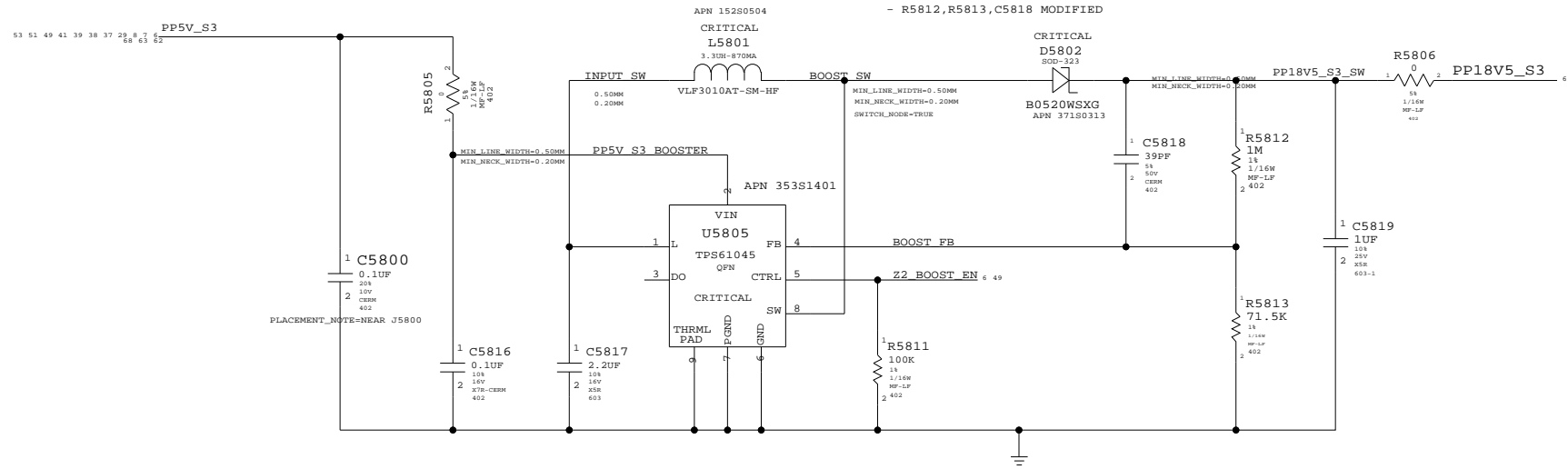


SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	48	83

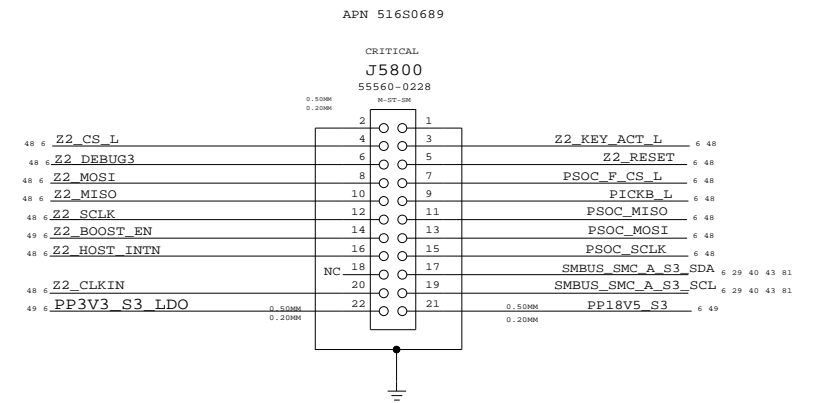


### BOOSTER +18.5VDC FOR SENSORS

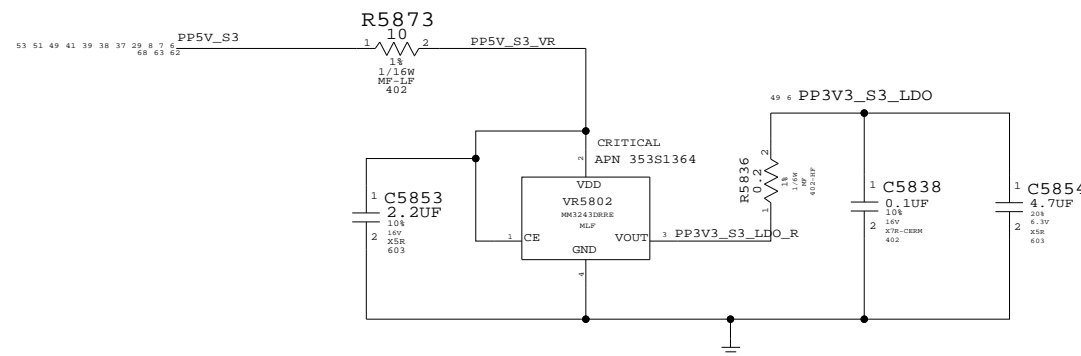
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
  - DROOP LINE REGULATION
  - RIPPLE TO MEET ERS
  - 100-300 KHZ CLEAN SPECTRUM
  - STARTUP TIME LESS THAN 2MS
  - R5812, R5813, C5818 MODIFIED



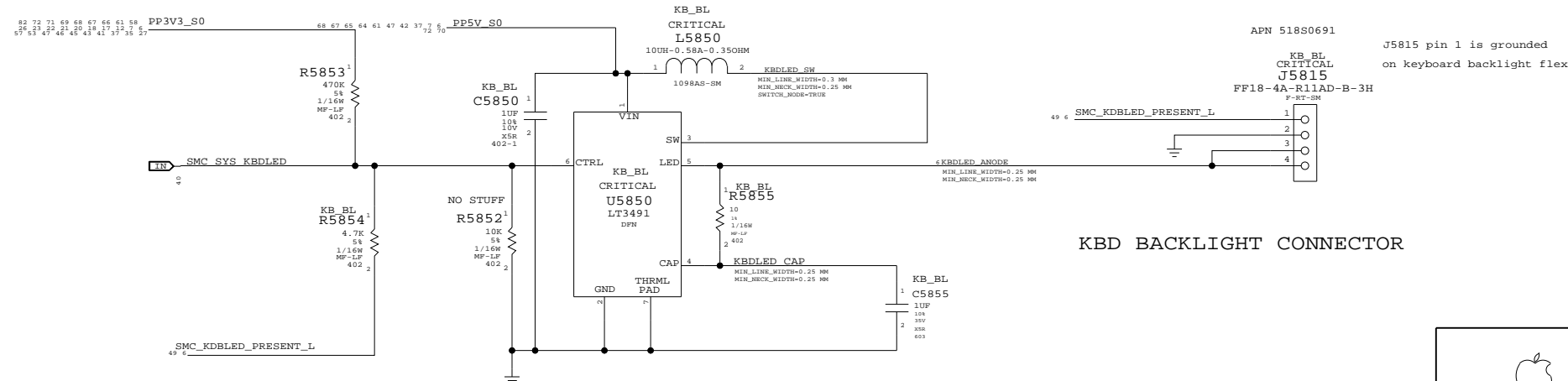
### IPD FLEX CONNECTOR



### 3V3 LDO FOR IPD



### KEYBOARD BACKLIGHT DRIVING AND DETECTION



To detect Keyboard backlight, SMC will tristate SMC\_SYS\_KBDLED:  
 LOW = keyboard backlight present  
 HIGH = keyboard backlight not present  
 BOM OPTION: KBDLED\_YES  
 TURNED ON FOR BEST MLB CONFIG  
 R5853 ALWAYS PRESENT

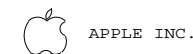
J5815 pin 1 is grounded on keyboard backlight flex

### WELLSPRING 2

SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/25/2009

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	49	83

8

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1

D

D

C

C

B

B

A

A

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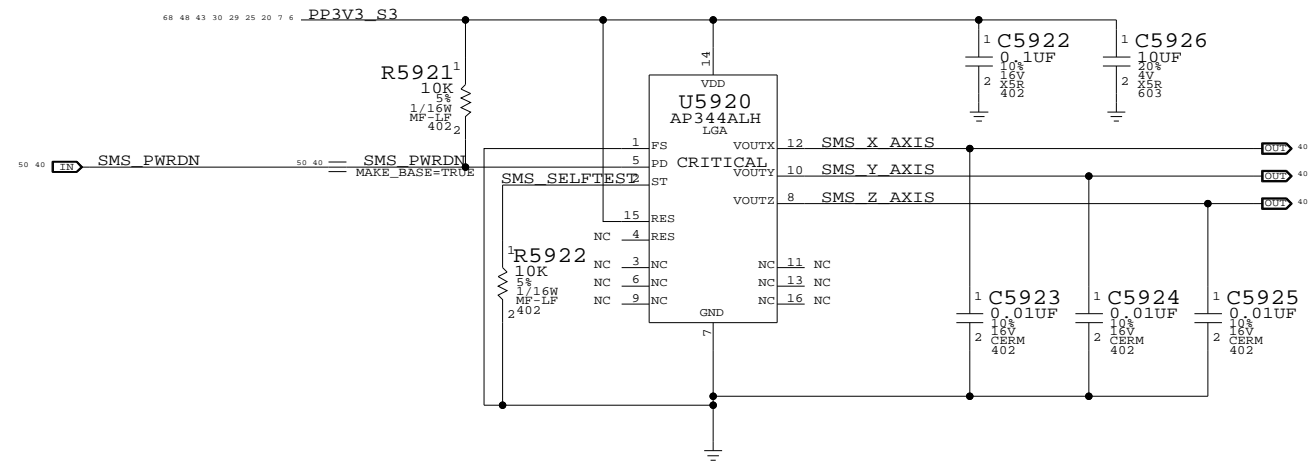
3

2

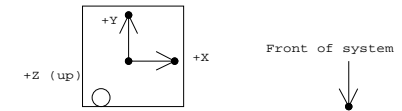
1

### Analog SMS

R5921 PULLS UP SMS\_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

#### Sudden Motion Sensor (SMS)

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009

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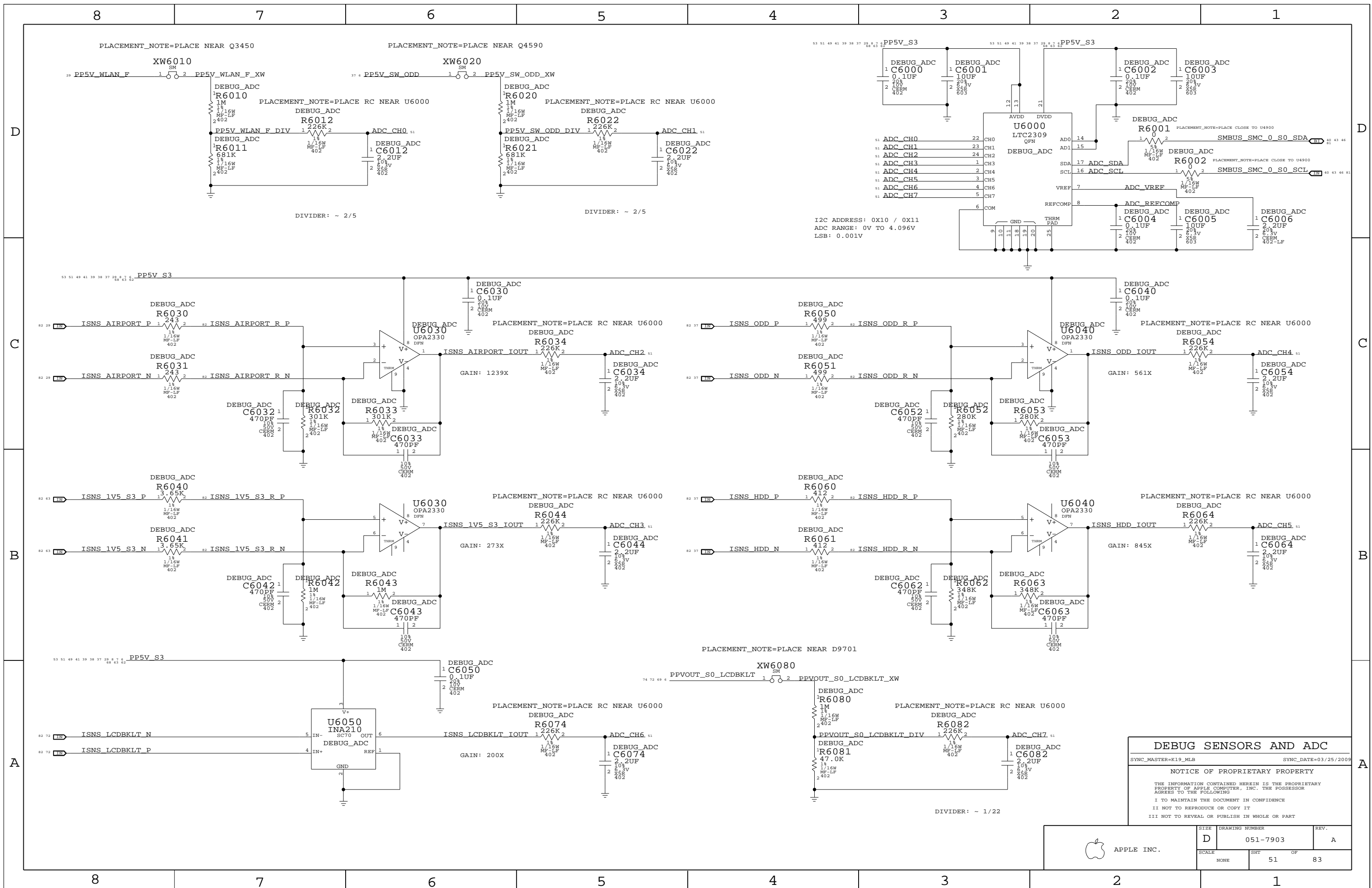
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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	50	83



**DEBUG SENSORS AND ADC**

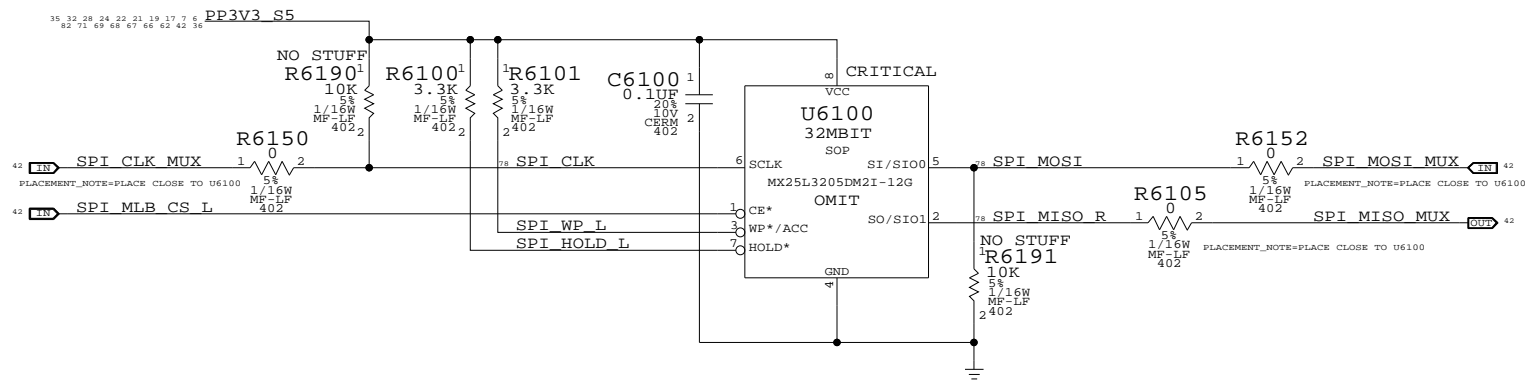
SYNC\_MASTER=K19\_MLB      SYNC\_DATE=03/25/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHEET	OF	REV.
NONE	51	83	A



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191  
 Any of the 4 frequencies can be selected  
 with R6190, R6191, R5190 and R5191

**SPI ROM**

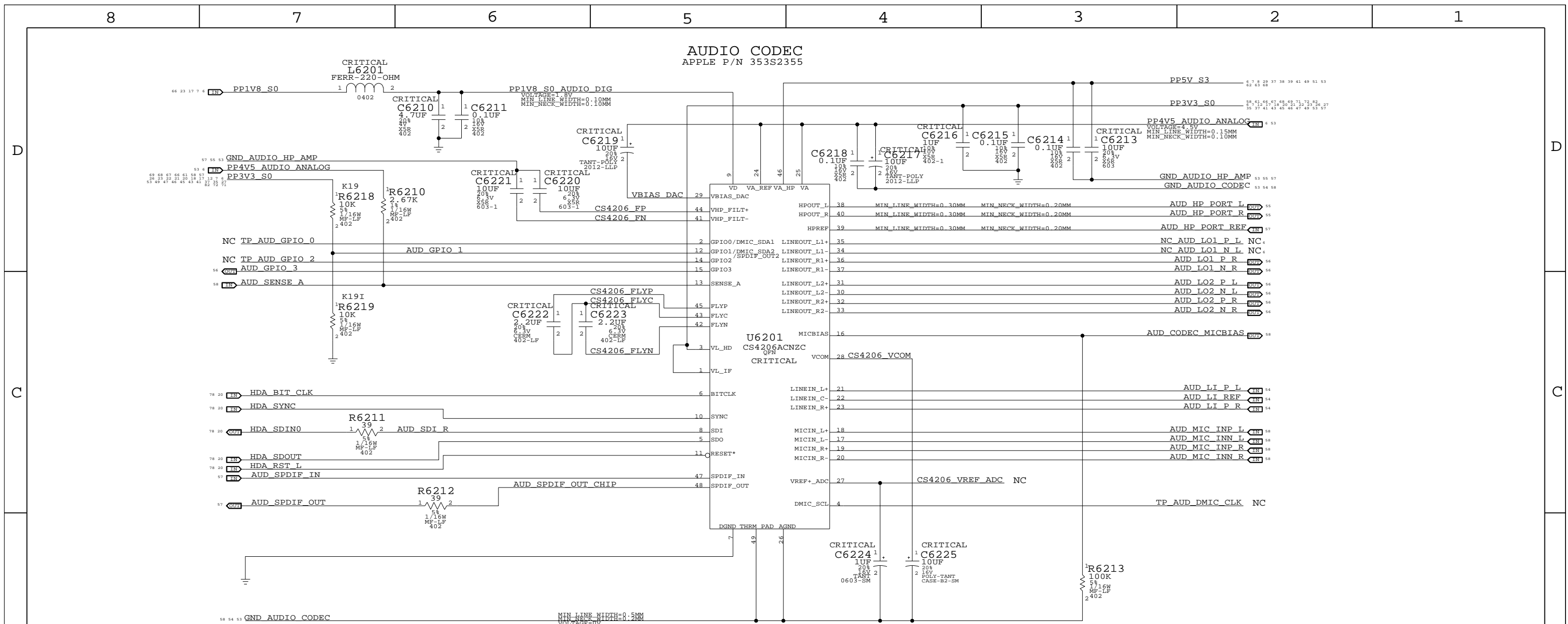
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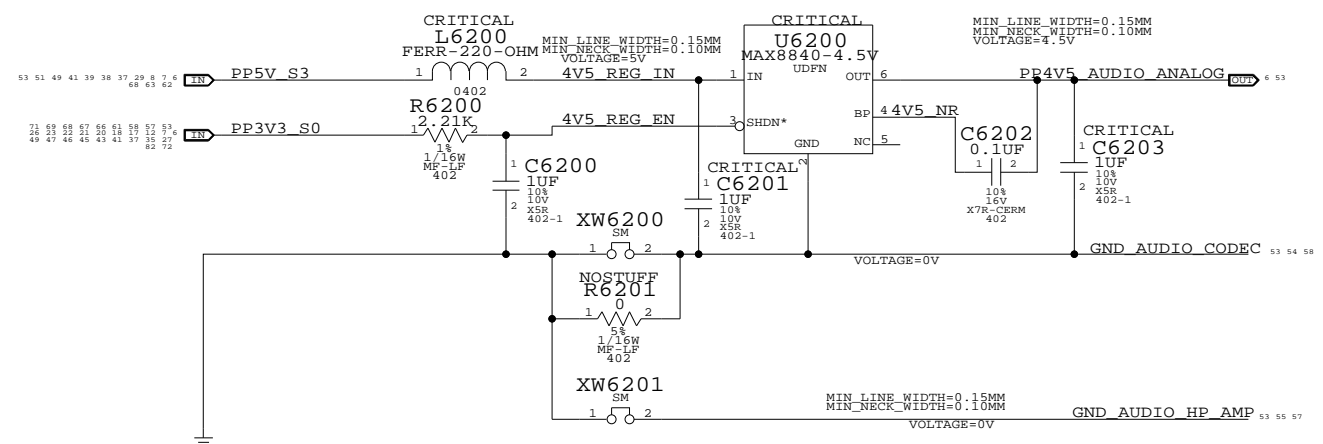
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	52	83	



4.5V POWER SUPPLY FOR CODEC  
APPLE P/N 353S2234



NOTES ON CODEC I/O

- DIFF FSINPUT= 2.45VRMS
- SE FSINPUT= 1.22VRMS
- DAC1 FSOUTPUT= 1.34VRMS
- DAC2/3 FSOUTPUTDIFF= 2.67VRMS
- DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO: CODEC/REGULATOR

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	NONE	SHT	OF
		53	83

8

7

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D

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A

A

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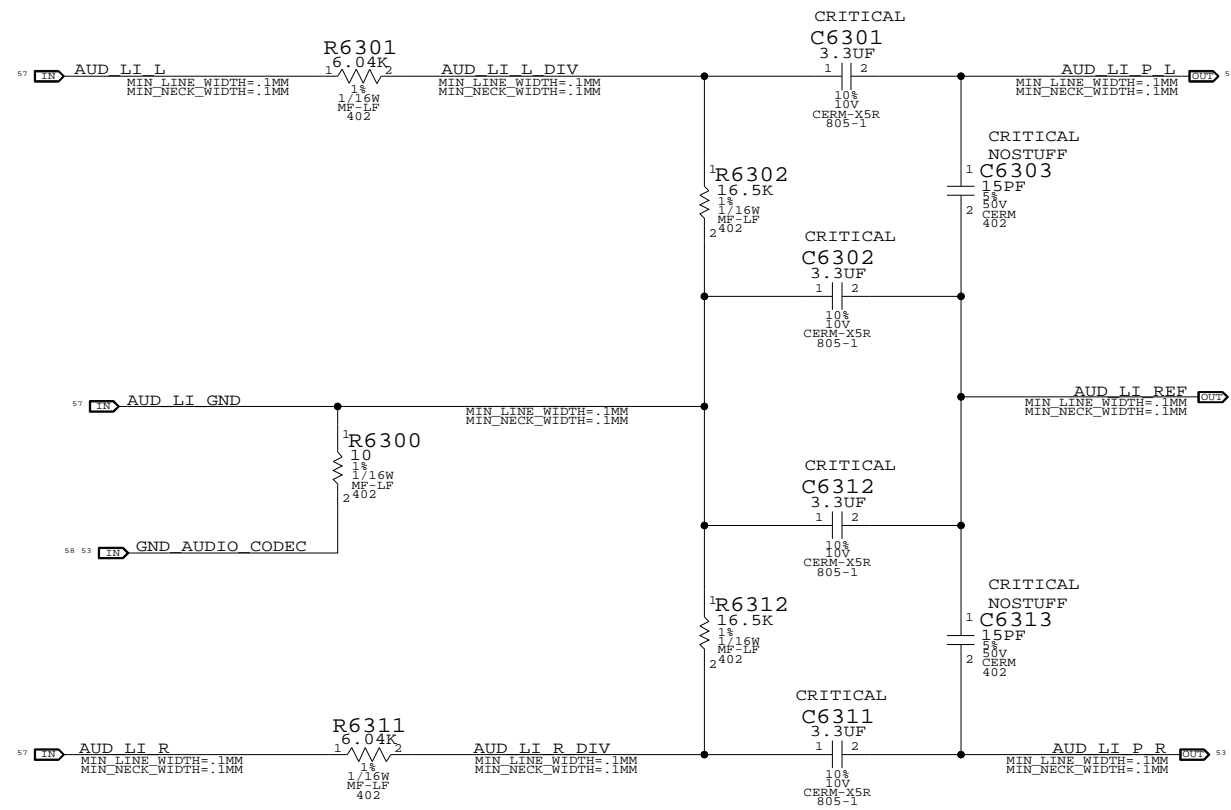
3

2

1

### LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS  
 NET RIN = 20K OHMS  
 FC = 8 HZ  
 VIN = 2VRMS, CODEC VIN = 1.21 VRMS



### AUDIO: LINE INPUT FILTER

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	54	83

8

7

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1

D

D

C

C

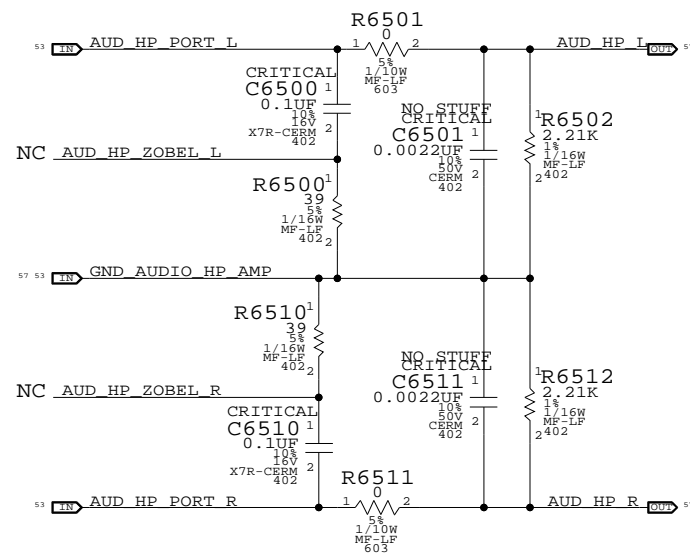
B

B

A

A

### ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



#### AUDIO: HEADPHONE FILTER

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	55	83

8

7

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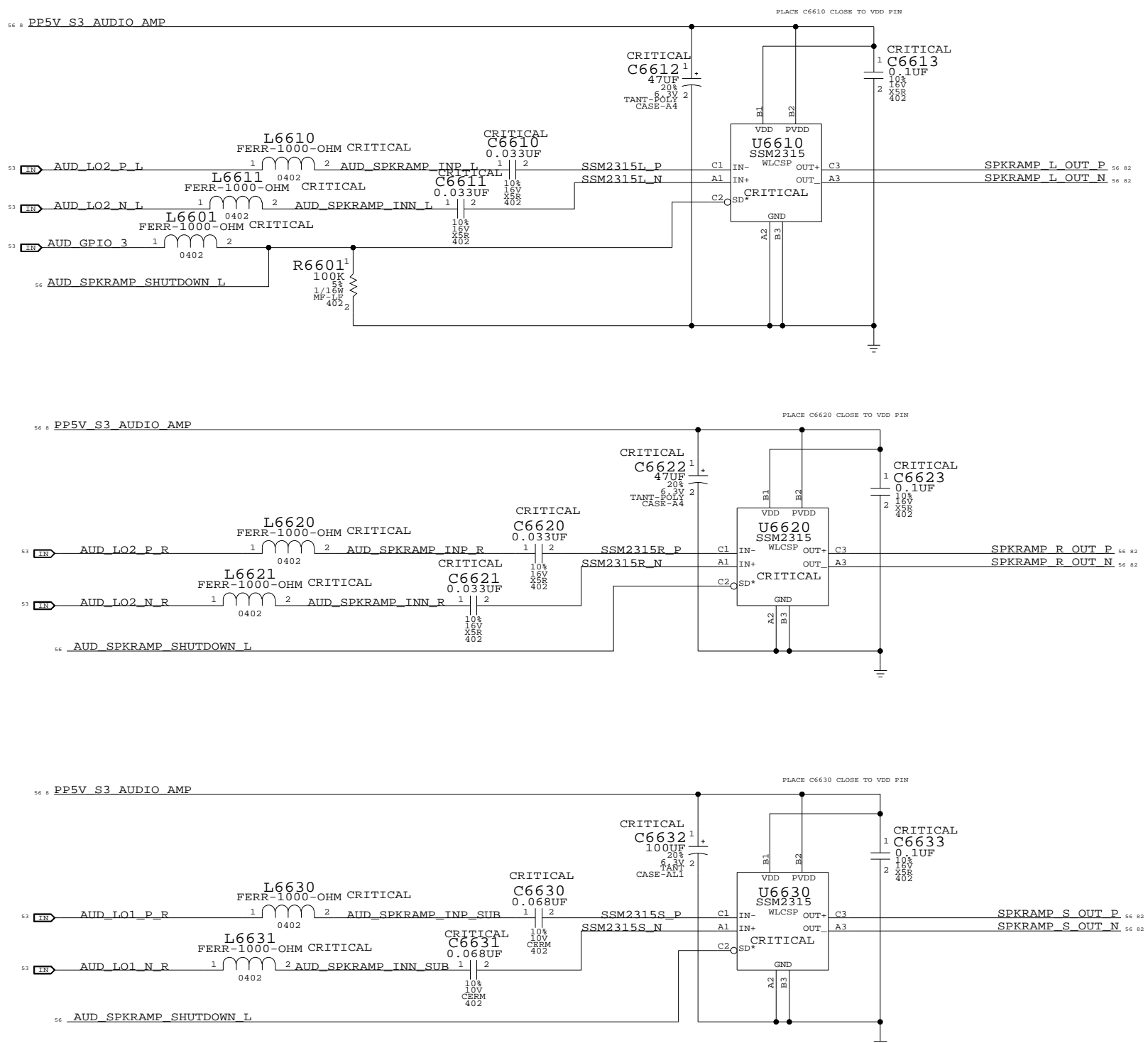
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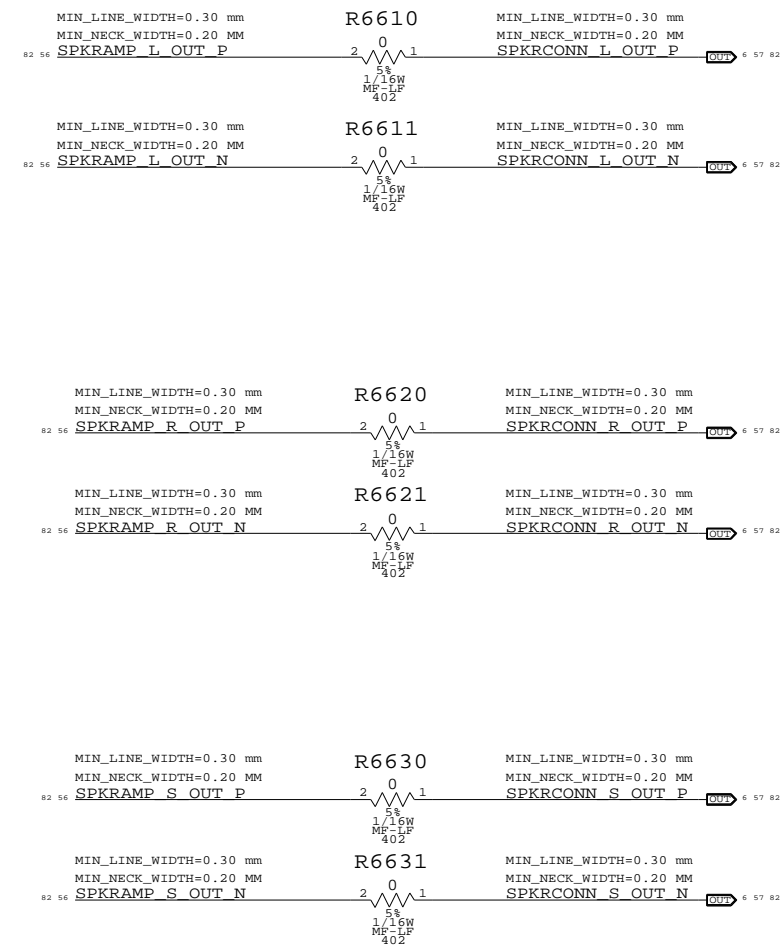
2

1

3X MONO SPEAKER AMPLIFIERS (SSM2315)  
 APN: 353S2500  
 GAIN = 6DB  
 1ST ORDER FC (L&R) = 120 HZ +/- 30%  
 1ST ORDER FC (SUB) = 58HZ +/- 30%



SPEAKER CHECKPOINTS

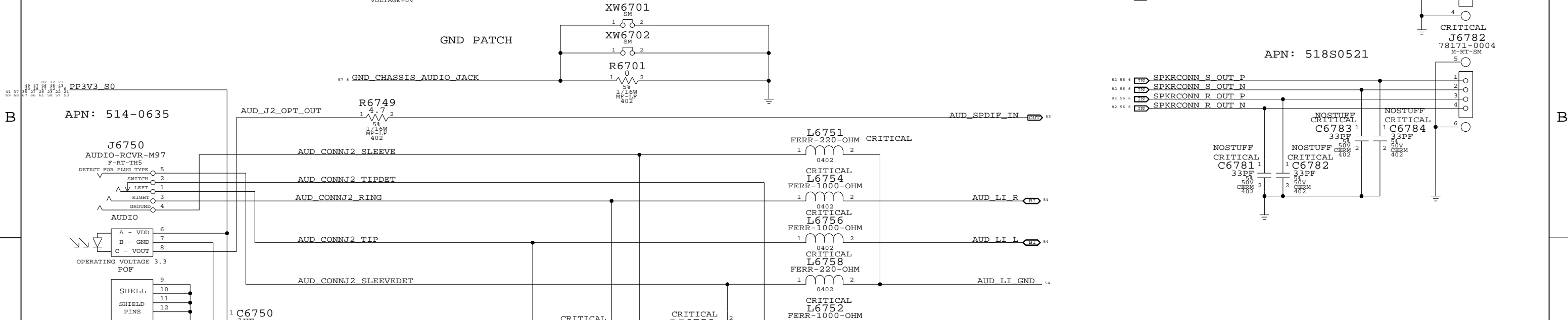
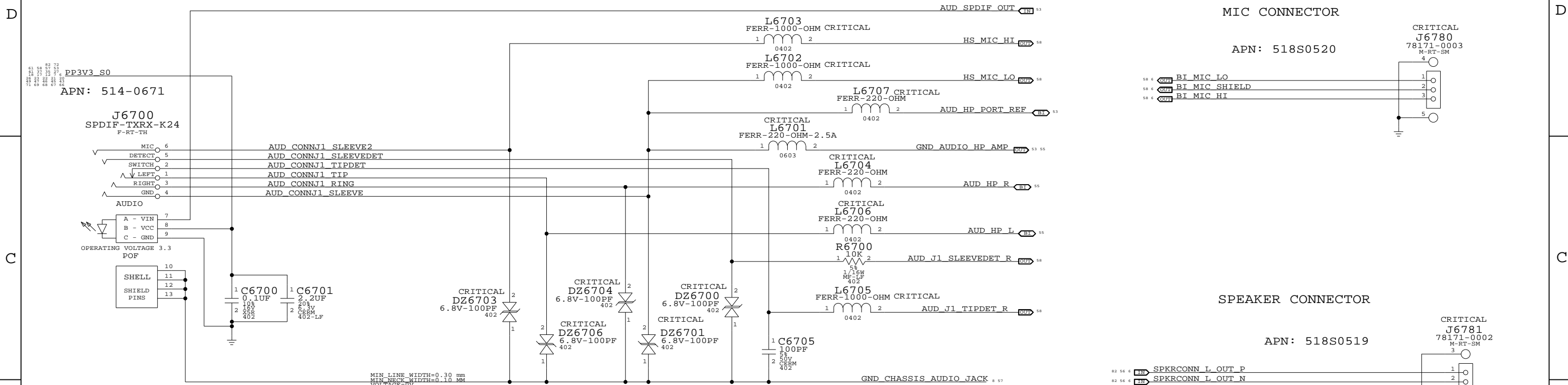


**AUDIO: SPEAKER AMP**  
 SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009  
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	D	051-7903	A
SCALE	SHT	OF	
NONE	56	83	



AUDIO JACK 1 LO/HP JACK, SPDIF TX



**AUDIO: JACKS**

SYNC\_MASTER=CASEYHARDY\_K19      SYNC\_DATE=03/20/2009

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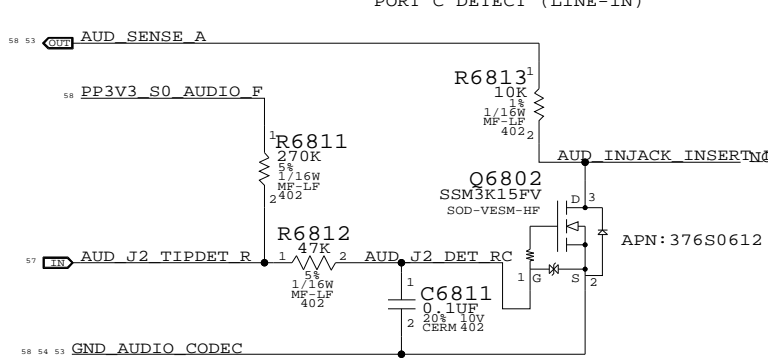
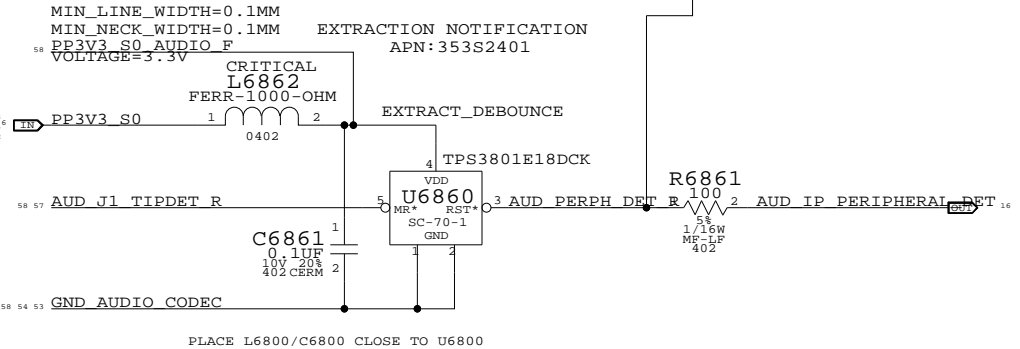
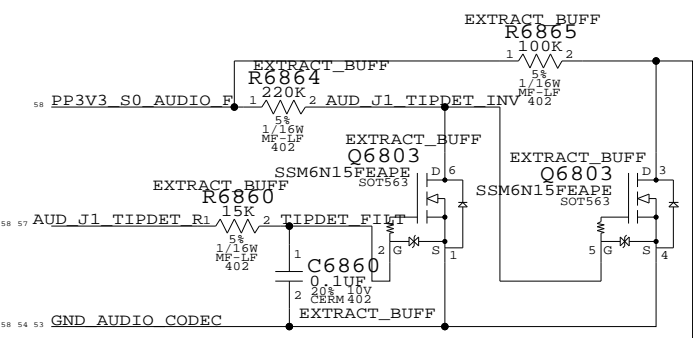
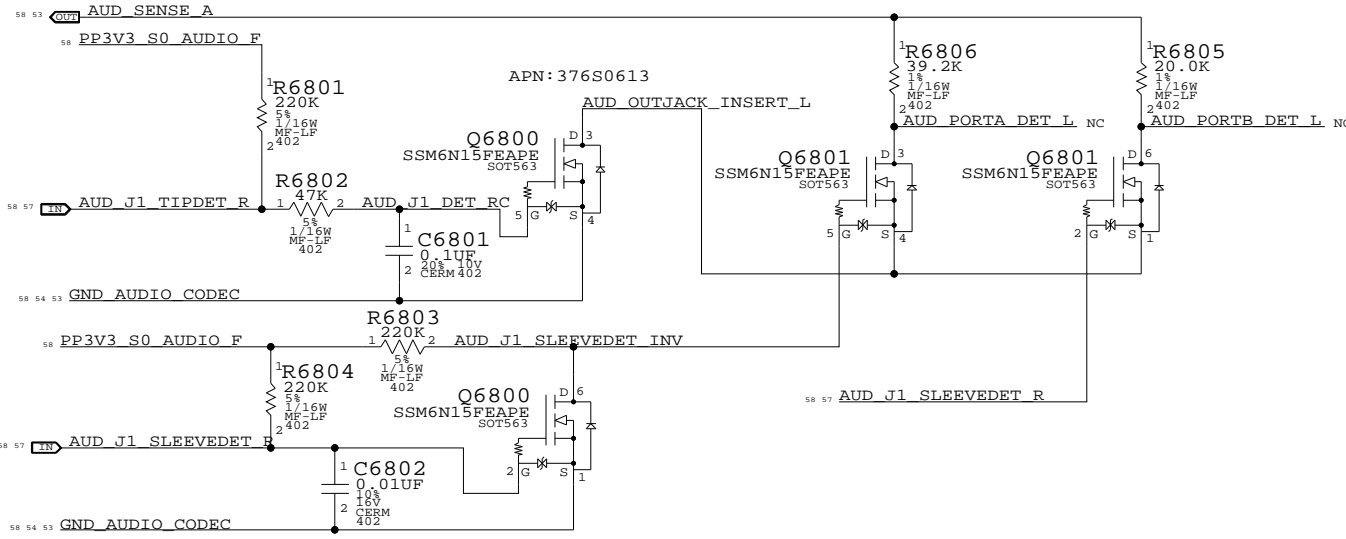
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

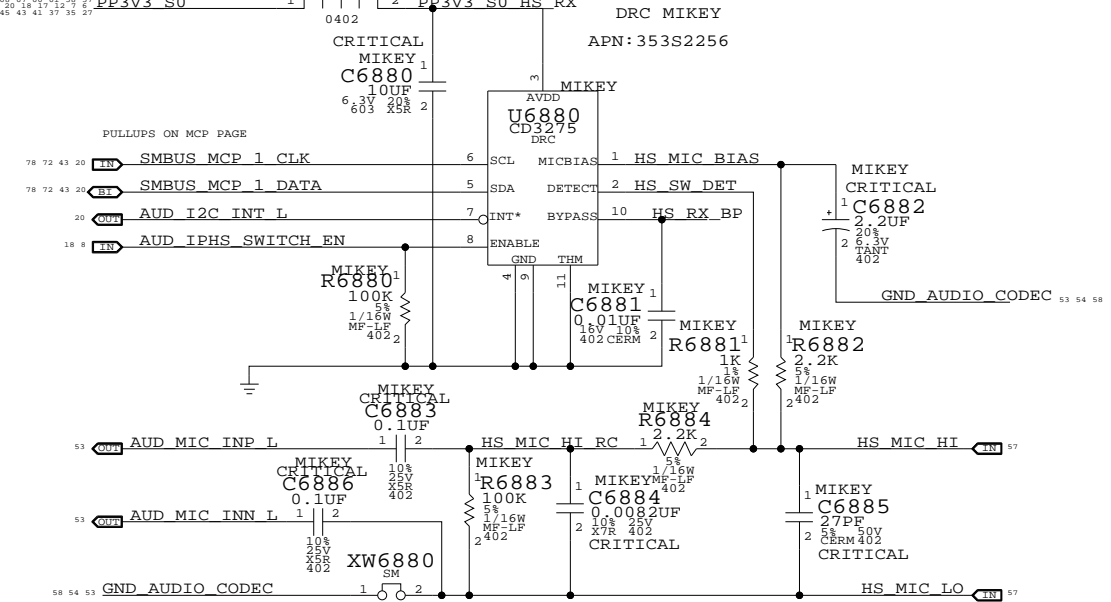
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

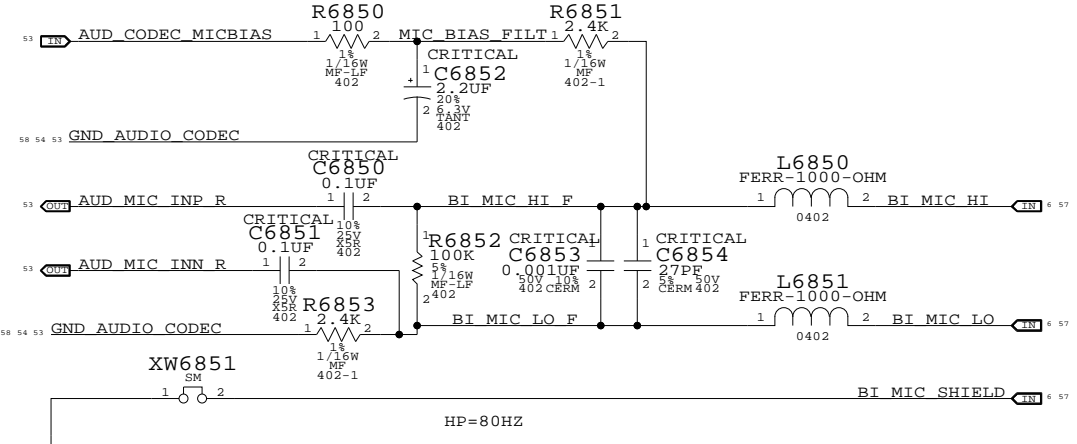
PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)



PORT B LEFT(HEADSET MIC)  
CRITICAL HP=80HZ, LP=8.82KHZ  
MIKEY MIN\_LINE\_WIDTH=0.1MM  
L6880 MIN\_NECK\_WIDTH=0.1MM  
FERR-1000-OHM VOLTAGE=3.3V



PORT B RIGHT (BUILT-IN MIC)

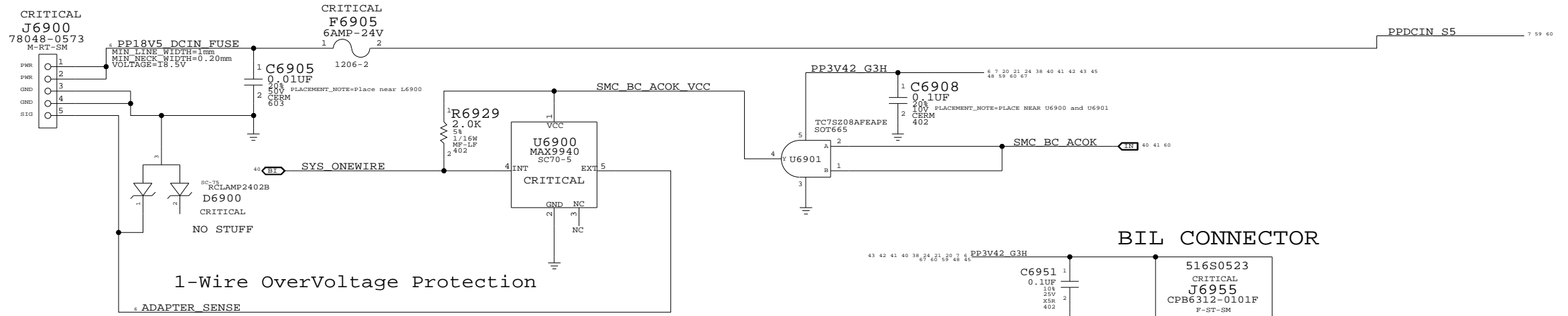


PORT C DETECT (LINE-IN)

**AUDIO: JACK TRANSLATORS**  
 SYNC\_MASTER=K19\_MLB SYNC\_DATE=03/17/2009  
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	D	051-7903	A
SCALE	SHT	OF	
NONE	58	83	

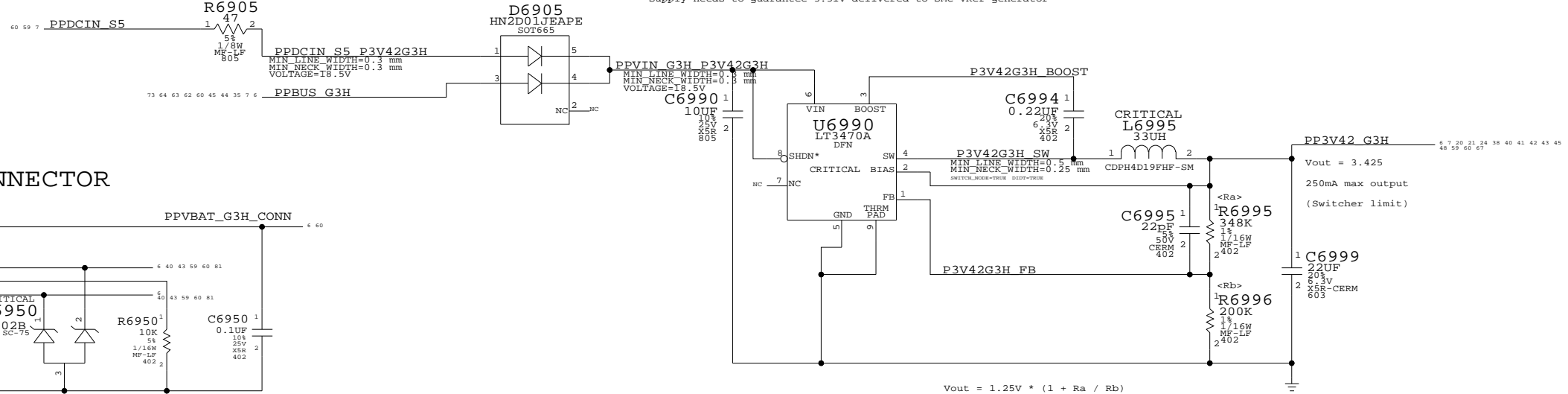
# MagSafe DC Power Jack



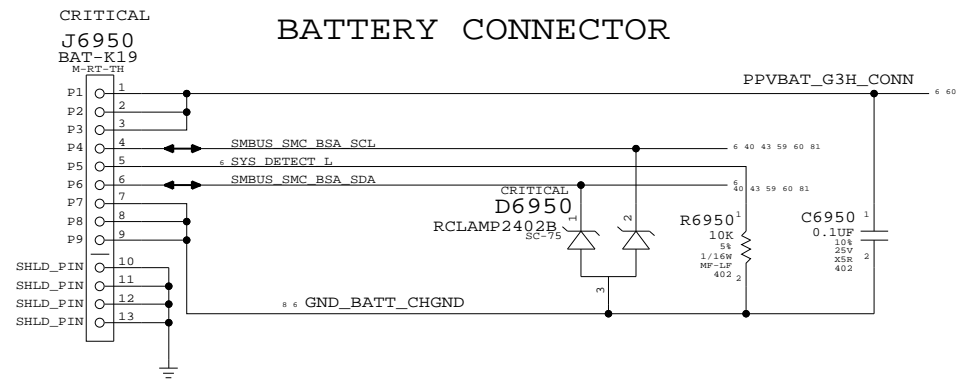
The chassis ground will otherwise float and can send transients onto ADAPTER\_SENSE when AC is connected.

# 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



# BATTERY CONNECTOR



**DC-In & Battery Connectors**

SYNC\_MASTER=K19\_MLB SYNC\_DATE=03/18/2009

**NOTICE OF PROPRIETARY PROPERTY**

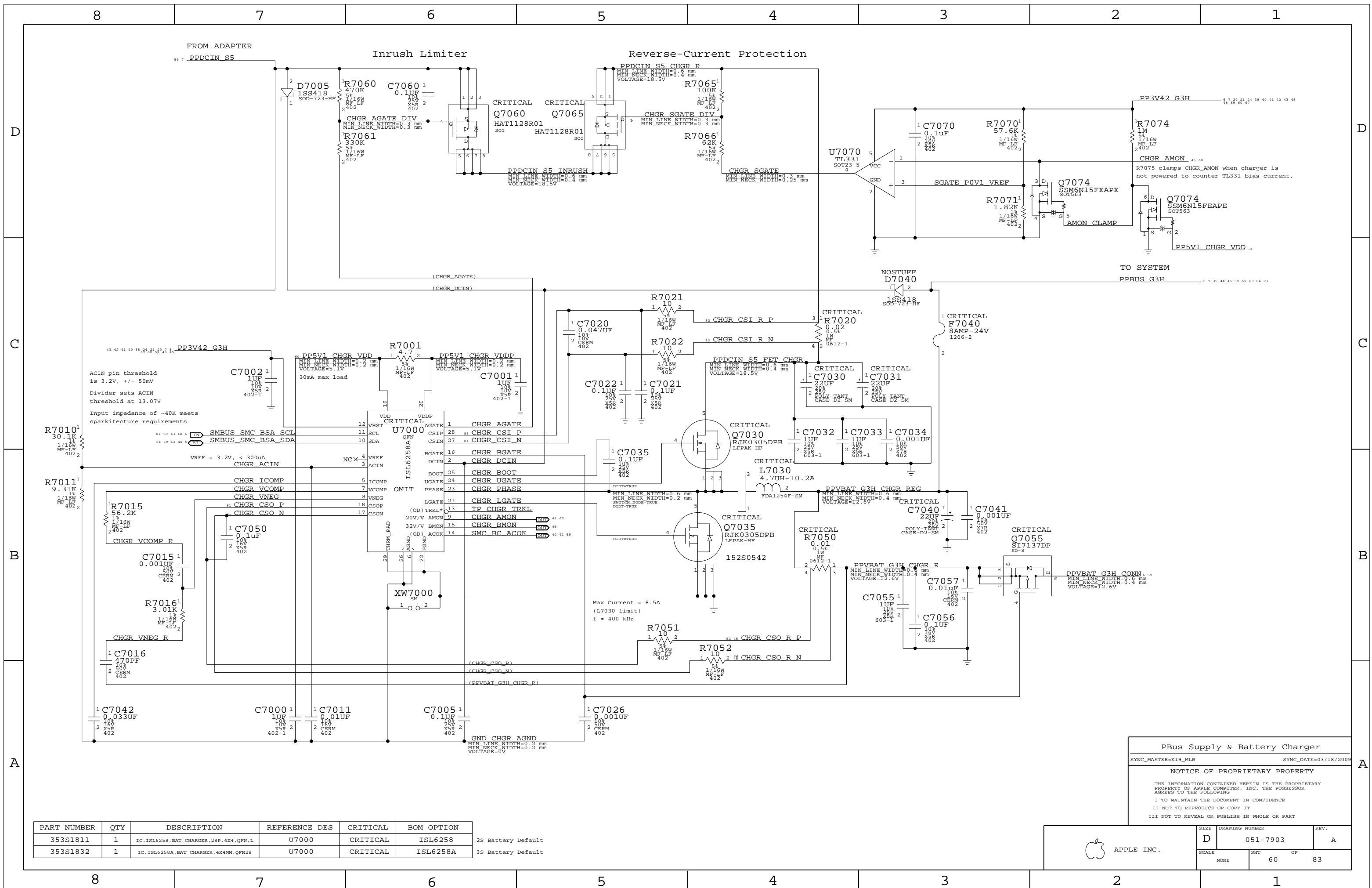
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	83
NONE	59		



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1811	1	IC, ISL6258, BAT CHARGER, 28P, 4X4, QFN, L	U7000	CRITICAL	ISL6258 2S Battery Default
353S1832	1	IC, ISL6258A, BAT CHARGER, 4X4MM, QFN28	U7000	CRITICAL	ISL6258A 3S Battery Default

**PBus Supply & Battery Charger**

SYNC\_MASTER=K19\_MLB      SYNC\_DATE=03/18/2009

**NOTICE OF PROPRIETARY PROPERTY**

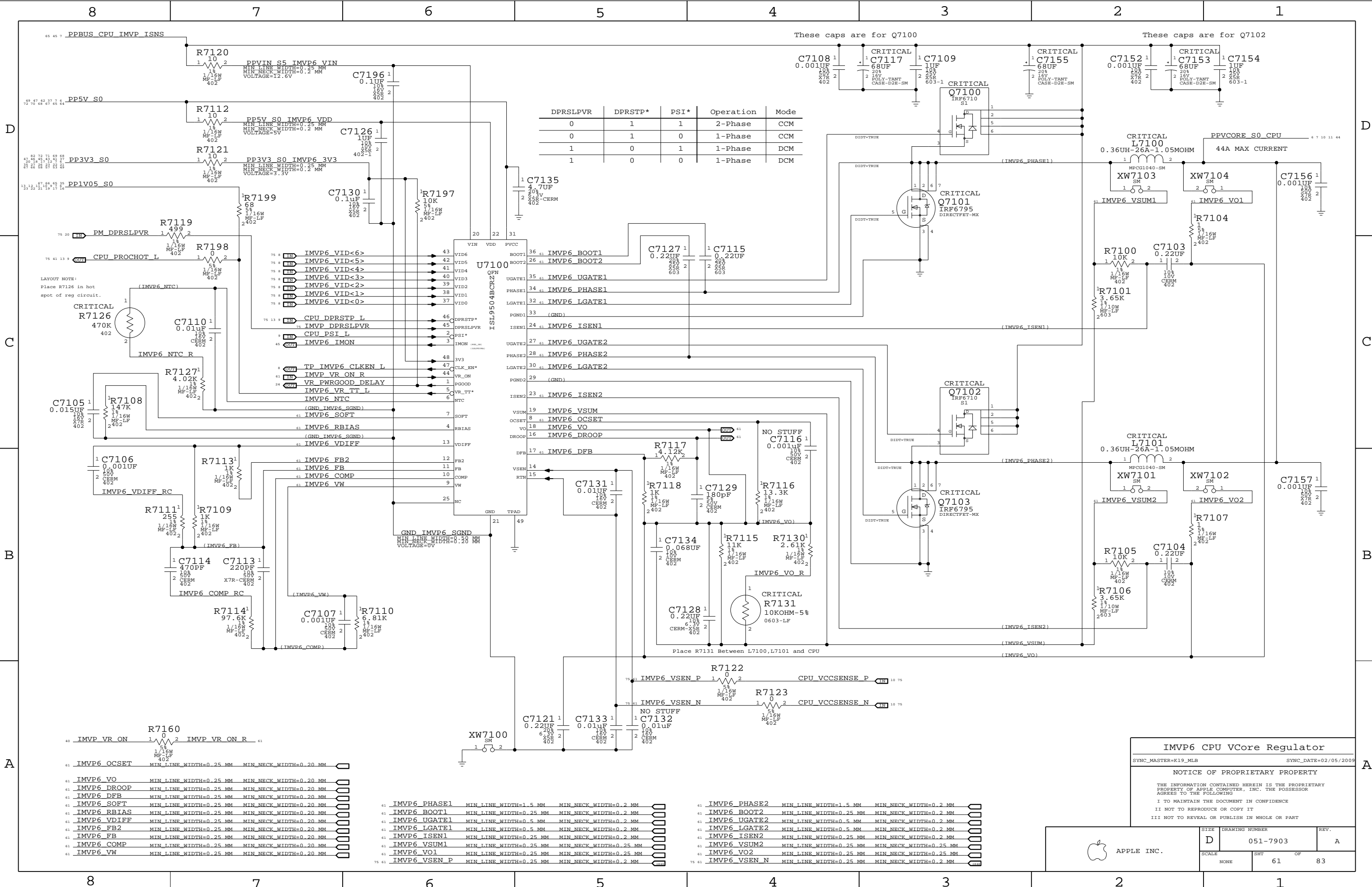
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7903	A
SHEET		OF	
60		83	



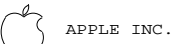
DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

**IMVP6 CPU VCore Regulator**

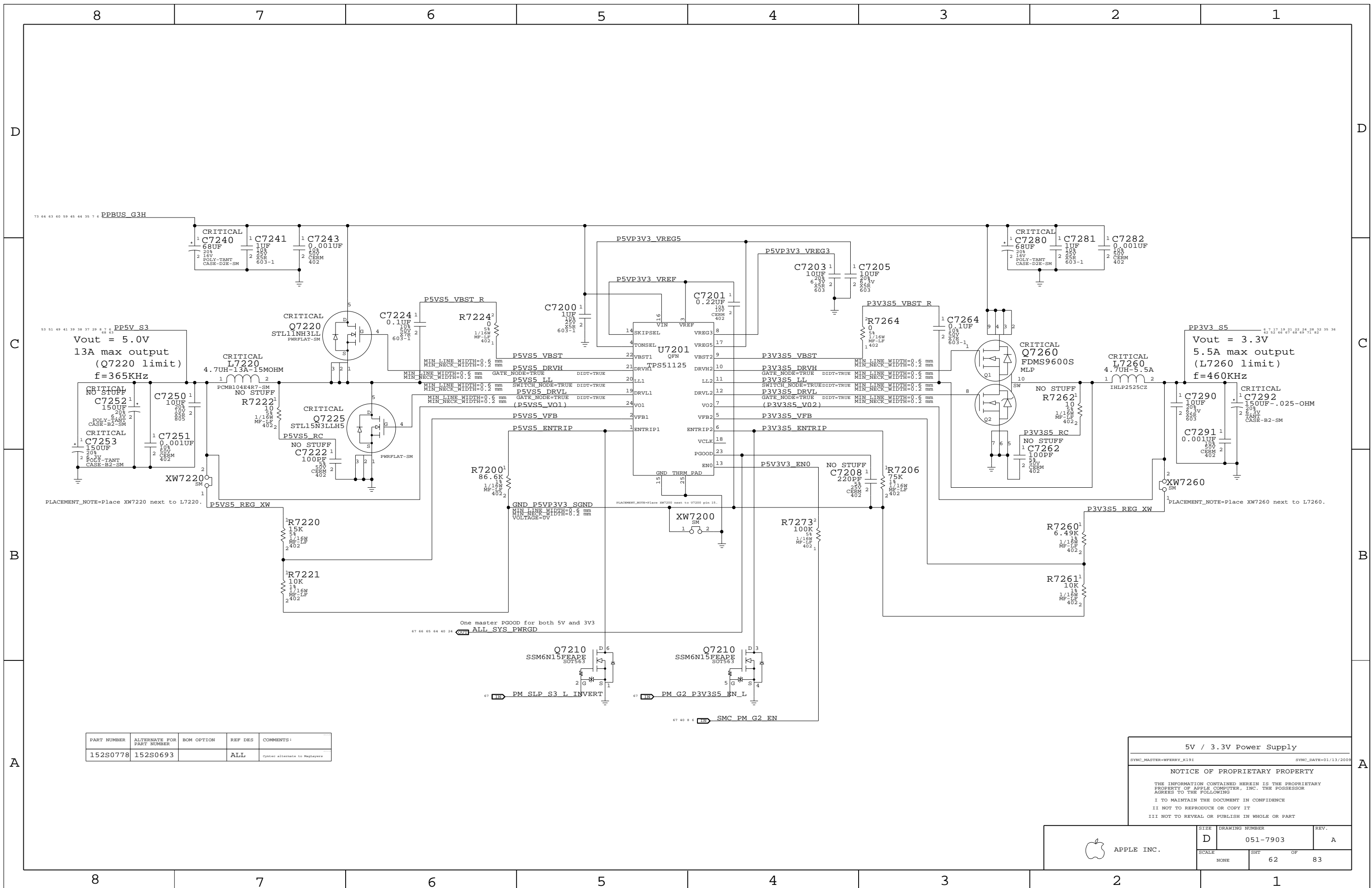
SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHEET	OF
NONE	61	83

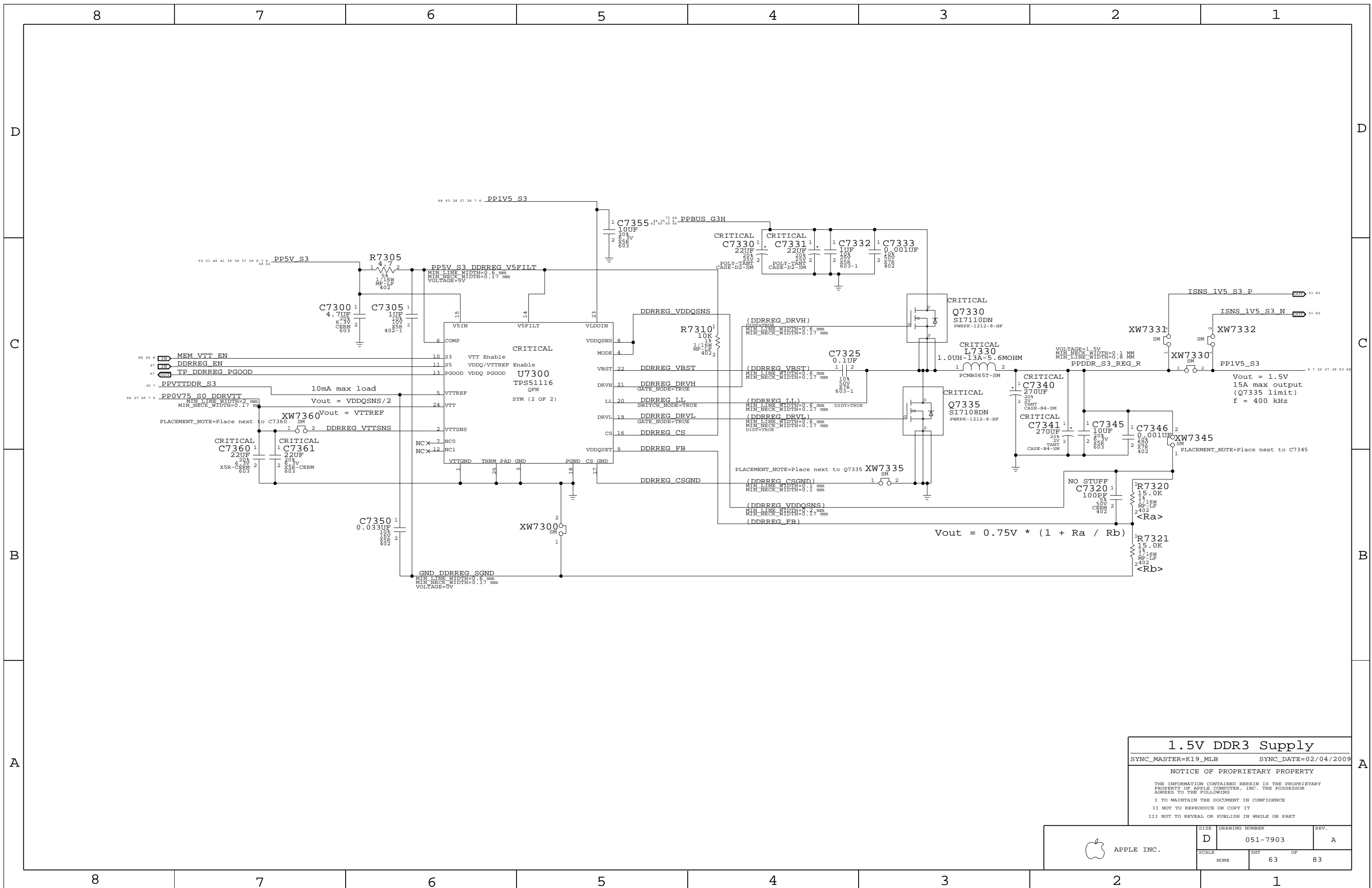


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	Cyano alternate to MagYellow

5V / 3.3V Power Supply  
 SYNC\_MASTER=WFERRY\_R191 SYNC\_DATE=01/13/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	62		83



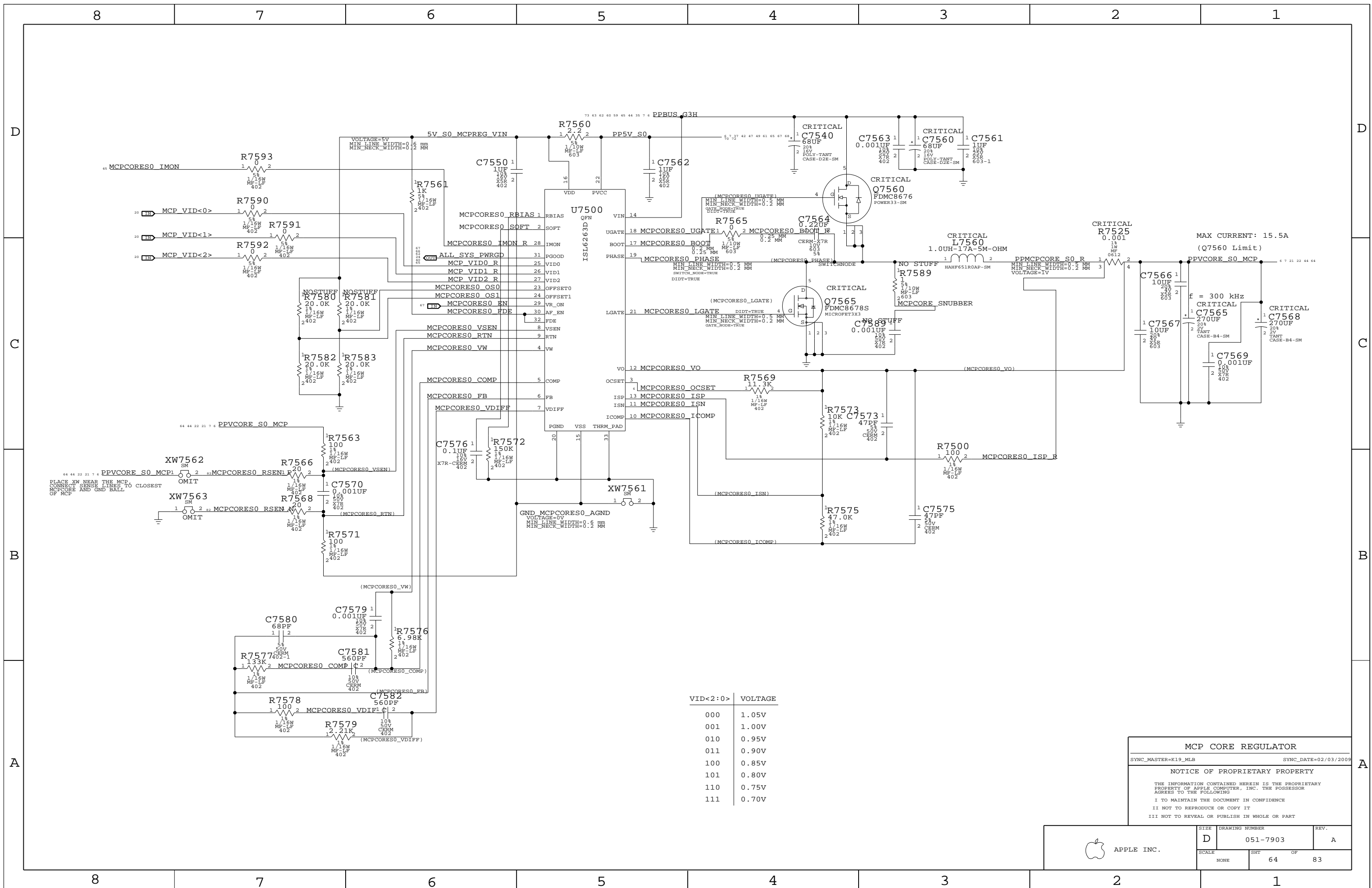
### 1.5V DDR3 Supply

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/04/2009

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	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	63	83	



VID<2:0>	VOLTAGE
000	1.05V
001	1.00V
010	0.95V
011	0.90V
100	0.85V
101	0.80V
110	0.75V
111	0.70V

**MCP CORE REGULATOR**

SYNC\_MASTER=K19\_MLB      SYNC\_DATE=02/03/2009

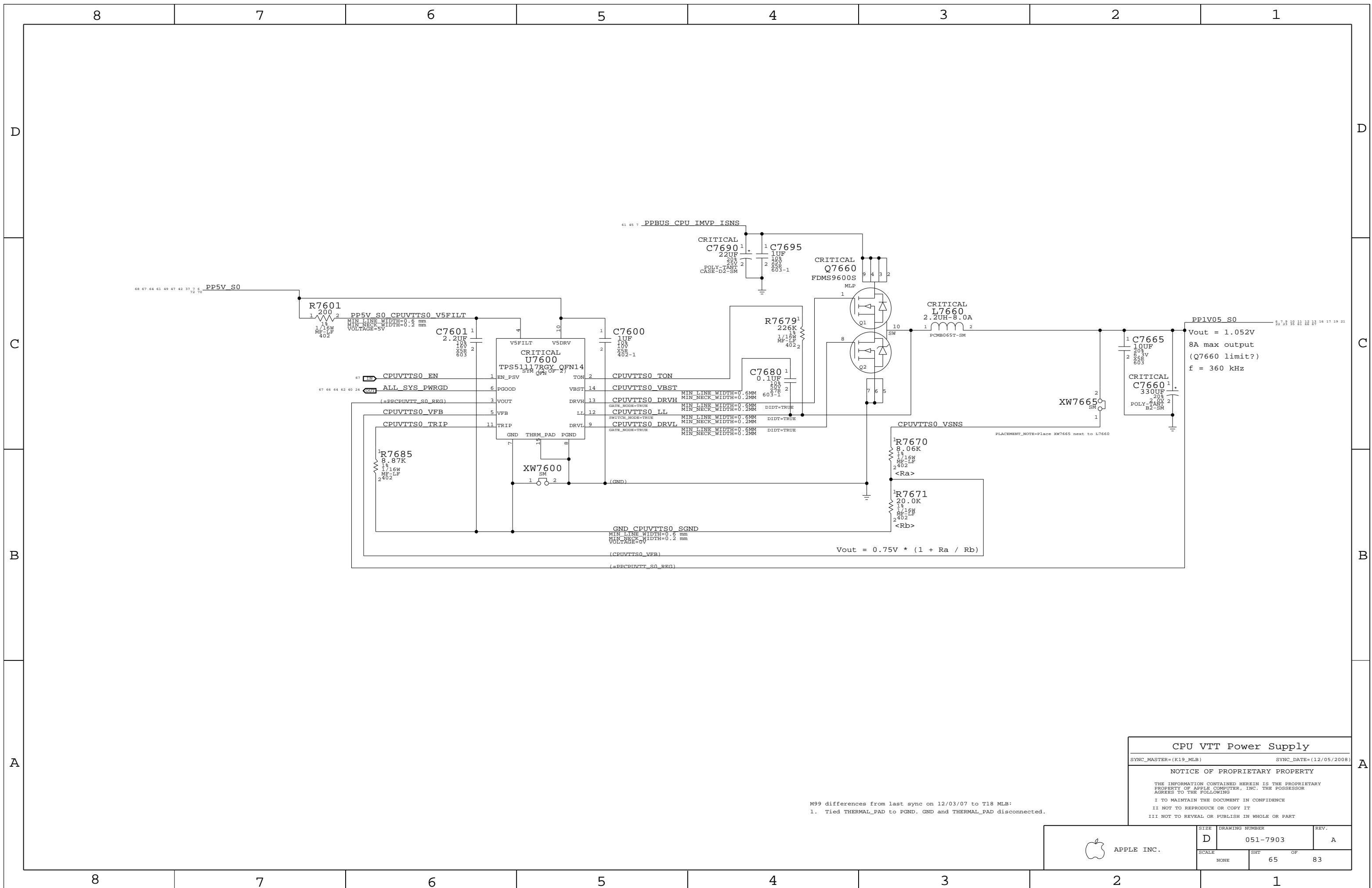
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APPLE INC.	SIZE: <b>D</b>	DRAWING NUMBER: <b>051-7903</b>	REV.: <b>A</b>
	SCALE: NONE	SHEET: 64 OF 83	





M99 differences from last sync on 12/03/07 to T18 MLB:  
 1. Tied THERMAL\_PAD to PGND. GND and THERMAL\_PAD disconnected.

**CPU VTT Power Supply**

SYNC\_MASTER=(K19\_MLB) SYNC\_DATE=(12/05/2008)

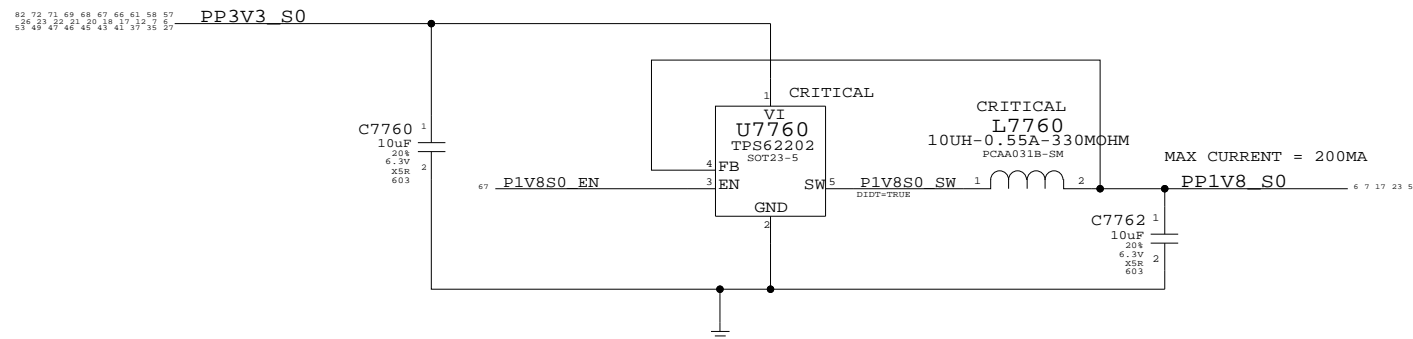
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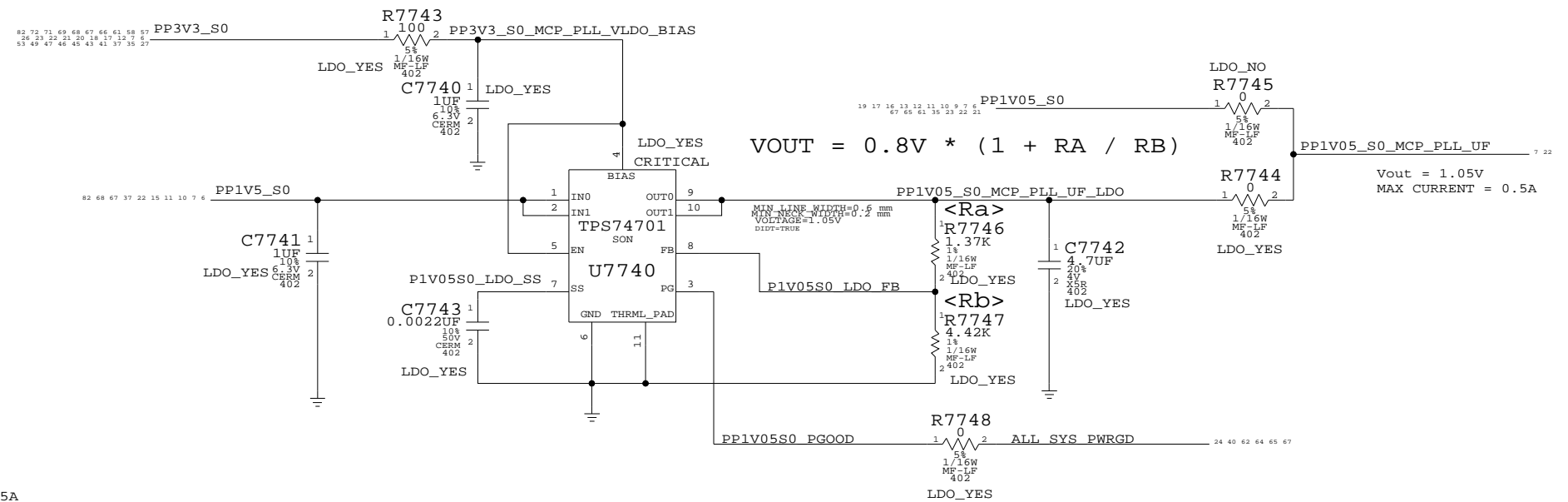
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	65	83	

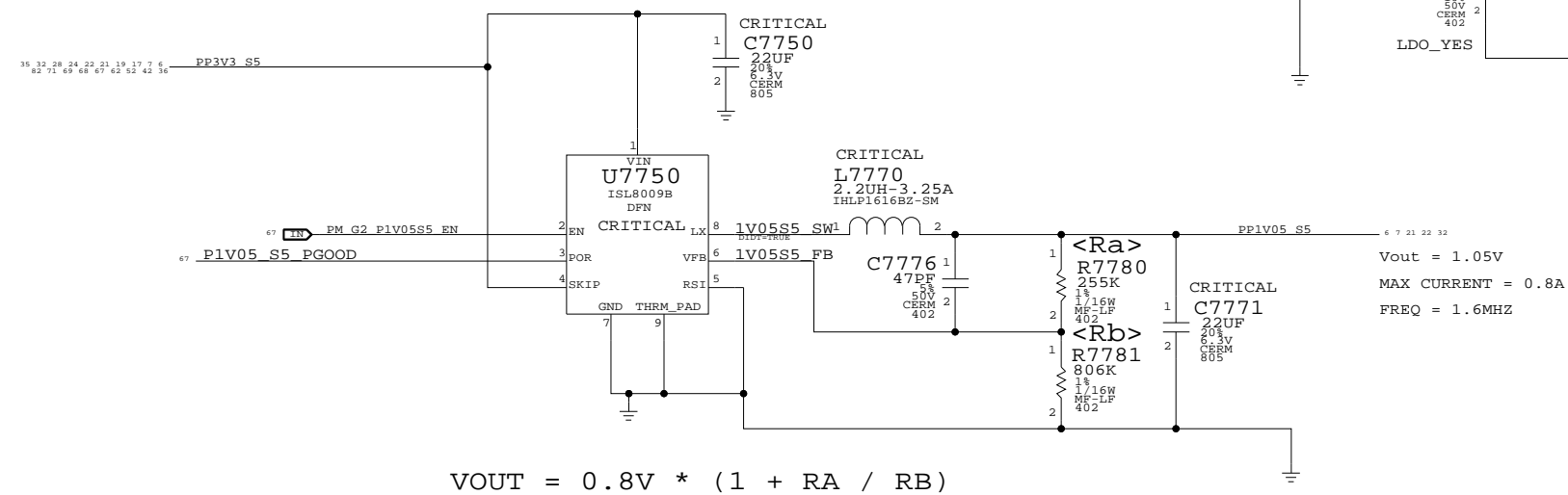
# 1.8V S0 SWITCHER



## 1.05V S0 PLL LDO



## MCP 1.05V S5 (AUXC) SUPPLY



MISC POWER SUPPLIES  
 SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/25/2009

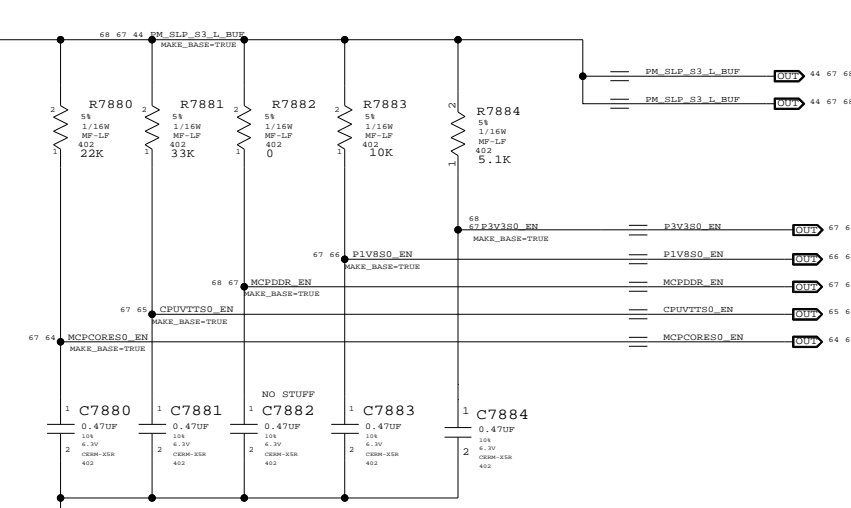
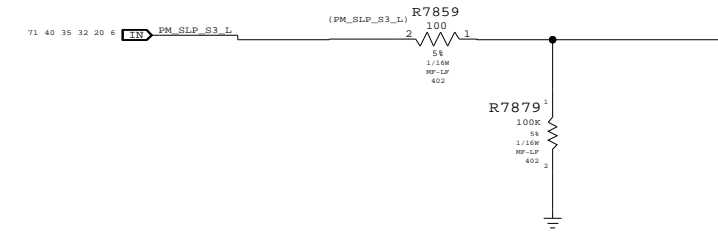
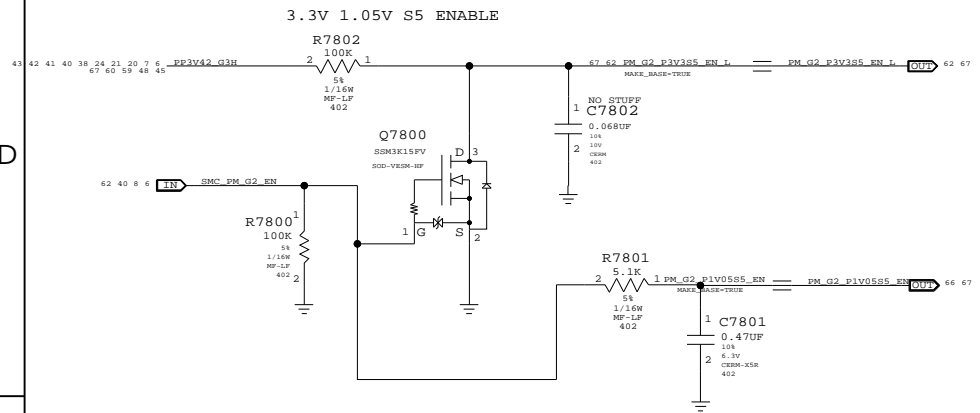
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	REV.
NONE	66	83	

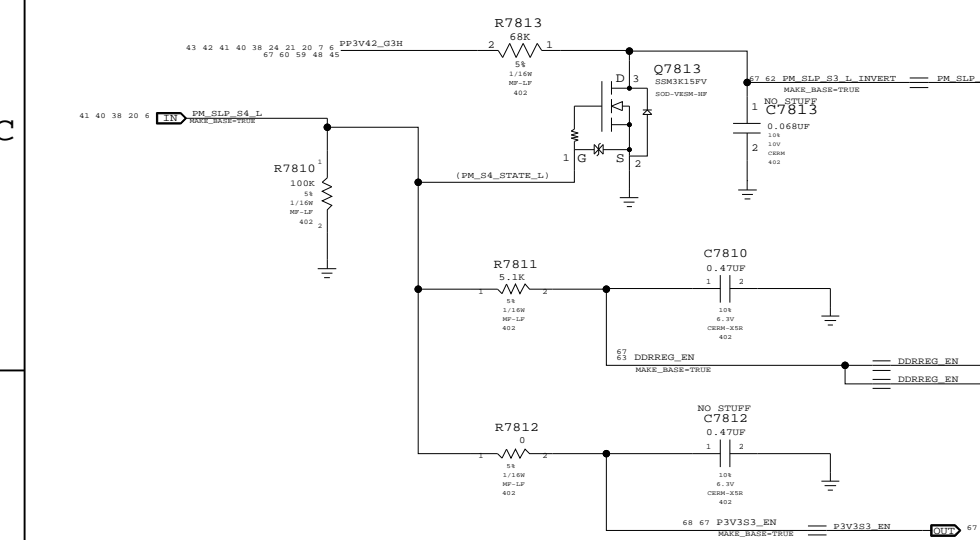
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

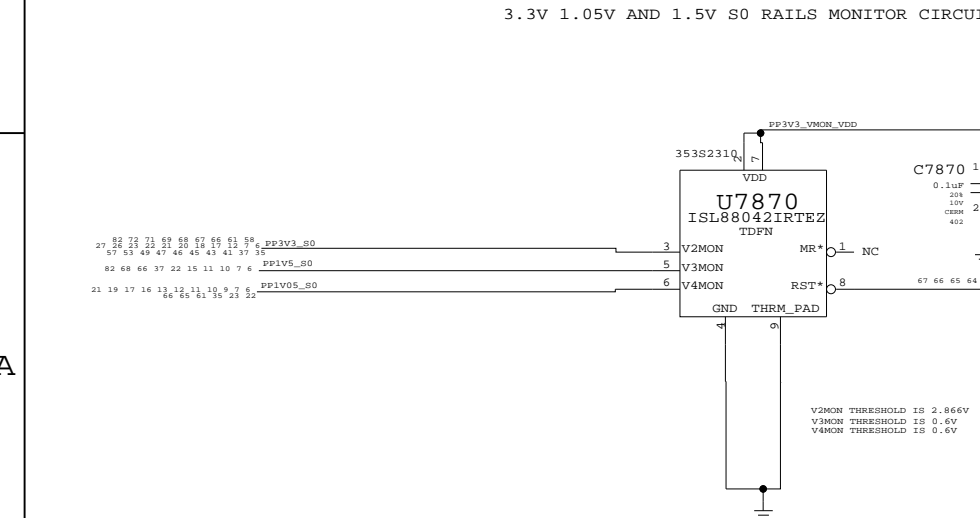
3.3V\_S0, 1.8V\_S0 ENABLE  
MCPDDR, CPUVTT, MCPCORES0 ENABLE  
1.5V S0 AND 1.05V S0 ENABLE



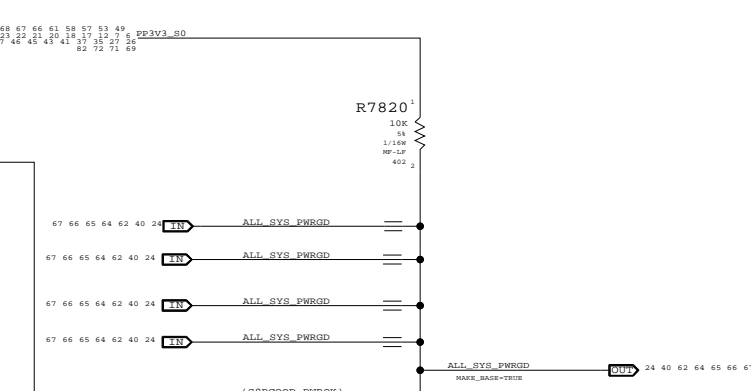
S3 ENABLE



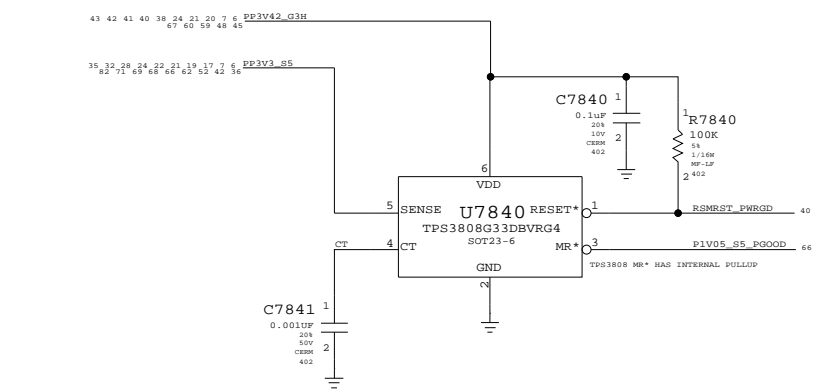
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



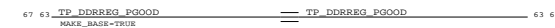
OTHER S0 RAILS PGOOD



VOLTAGE MONITOR



Unused PGOOD signal



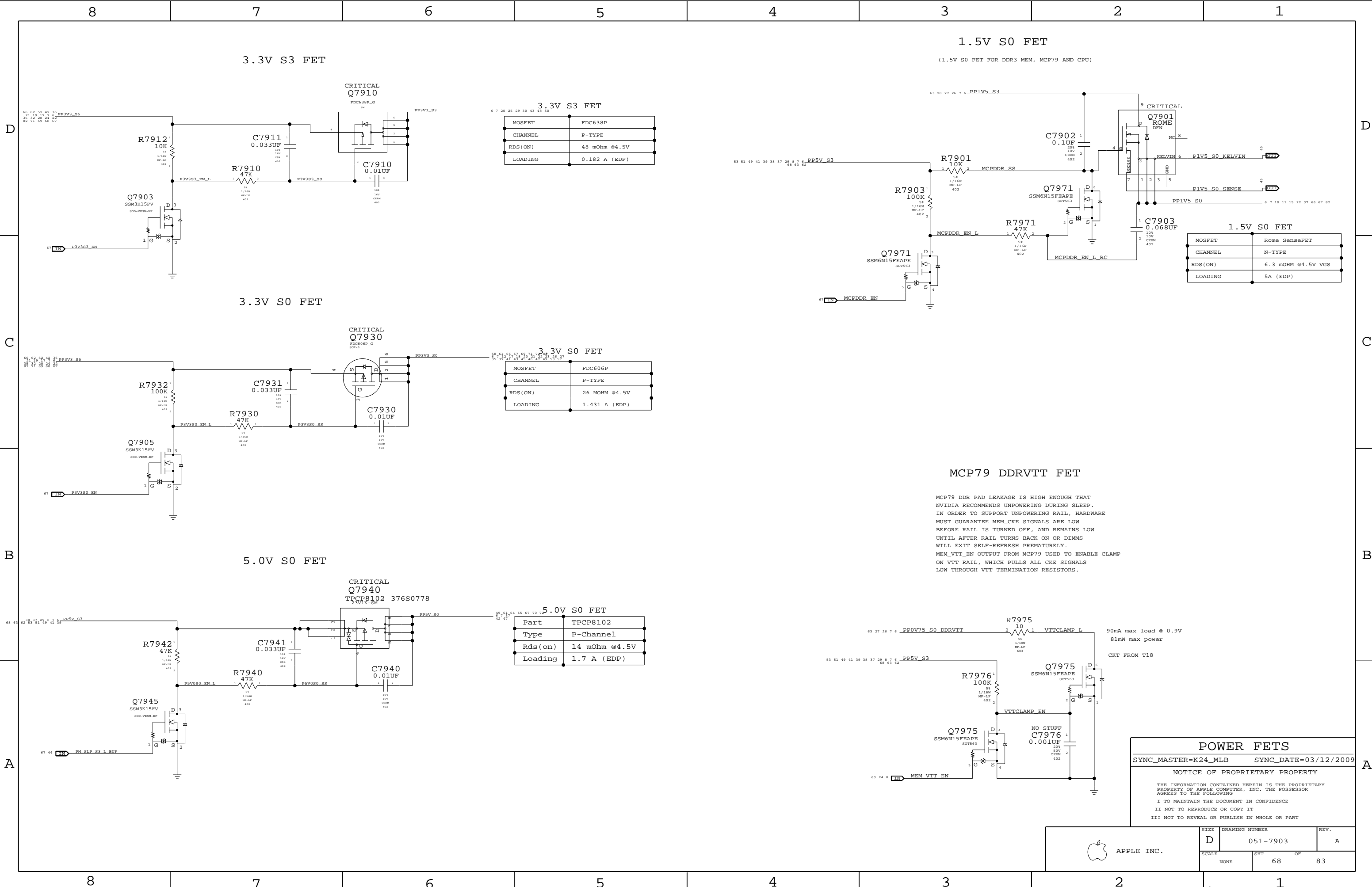
POWER SEQUENCING

SYNC\_MASTER=K24\_MLB SYNC\_DATE=02/05/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	NONE	SHT	OF
		67	83



3.3V S3 FET

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET

3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

5.0V S0 FET

5.0V S0 FET

Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
Loading	1.7 A (EDP)

1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

1.5V S0 FET

MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOhm @4.5V VGS
LOADING	5A (EDP)

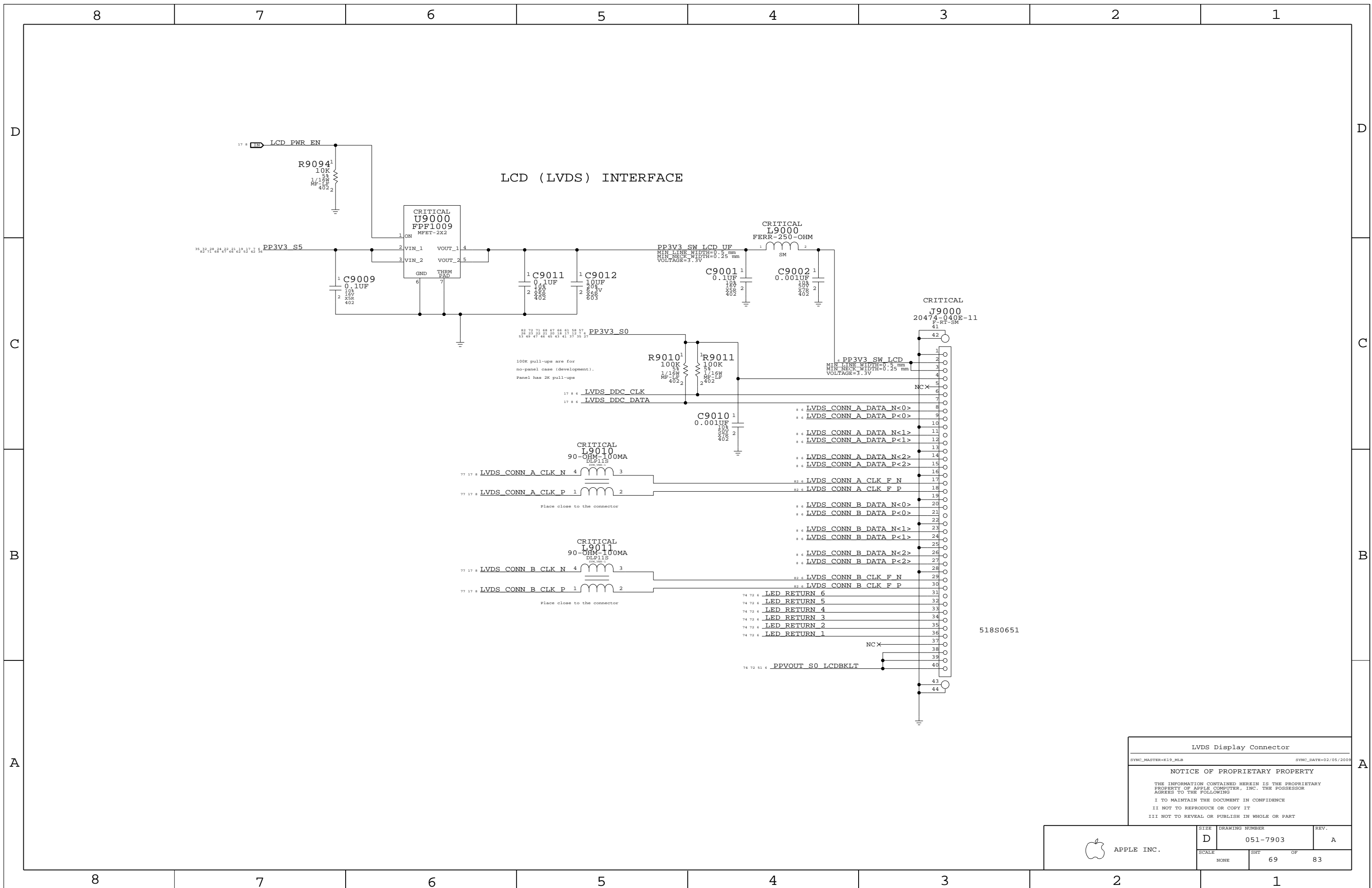
MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.

90mA max load @ 0.9V  
81mW max power  
CKT FROM T18

**POWER FETS**  
 SYNC\_MASTER=K24\_MLB SYNC\_DATE=03/12/2009  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
	SCALE	SHT	OF
	NONE	68	83



LCD (LVDS) INTERFACE

100K pull-ups are for  
no-panel case (development).  
Panel has 2K pull-ups

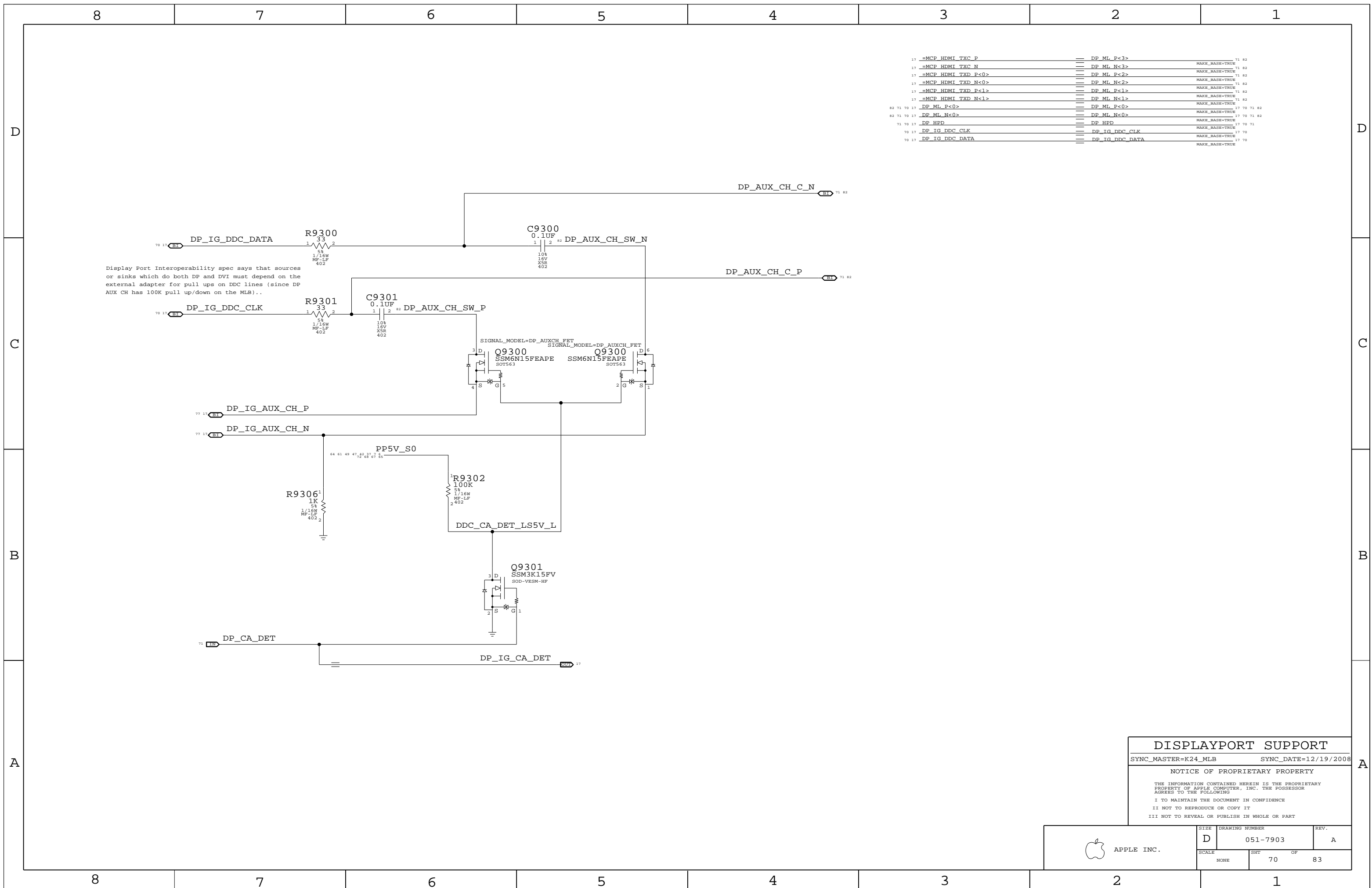
Place close to the connector

Place close to the connector

518S0651

LVDS Display Connector  
 SYNC\_MASTER=K19\_MLS SYNC\_DATE=02/05/2009  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
	SCALE	SHT	OF
	NONE	69	83



17	=MCP_HDMI_TXC_P	DP_ML_P<3>	71 82
17	=MCP_HDMI_TXC_N	DP_ML_N<3>	71 82
17	=MCP_HDMI_TXD_P<0>	DP_ML_P<2>	71 82
17	=MCP_HDMI_TXD_N<0>	DP_ML_N<2>	71 82
17	=MCP_HDMI_TXD_P<1>	DP_ML_P<1>	71 82
17	=MCP_HDMI_TXD_N<1>	DP_ML_N<1>	71 82
82 71 17	DP_ML_P<0>	DP_ML_P<0>	17 70 71 82
82 71 17	DP_ML_N<0>	DP_ML_N<0>	17 70 71 82
71 17	DP_HPD	DP_HPD	17 70 71
70 17	DP_IG_DDC_CLK	DP_IG_DDC_CLK	17 70
70 17	DP_IG_DDC_DATA	DP_IG_DDC_DATA	17 70

**DISPLAYPORT SUPPORT**

SYNC\_MASTER=K24\_MLB      SYNC\_DATE=12/19/2008

**NOTICE OF PROPRIETARY PROPERTY**

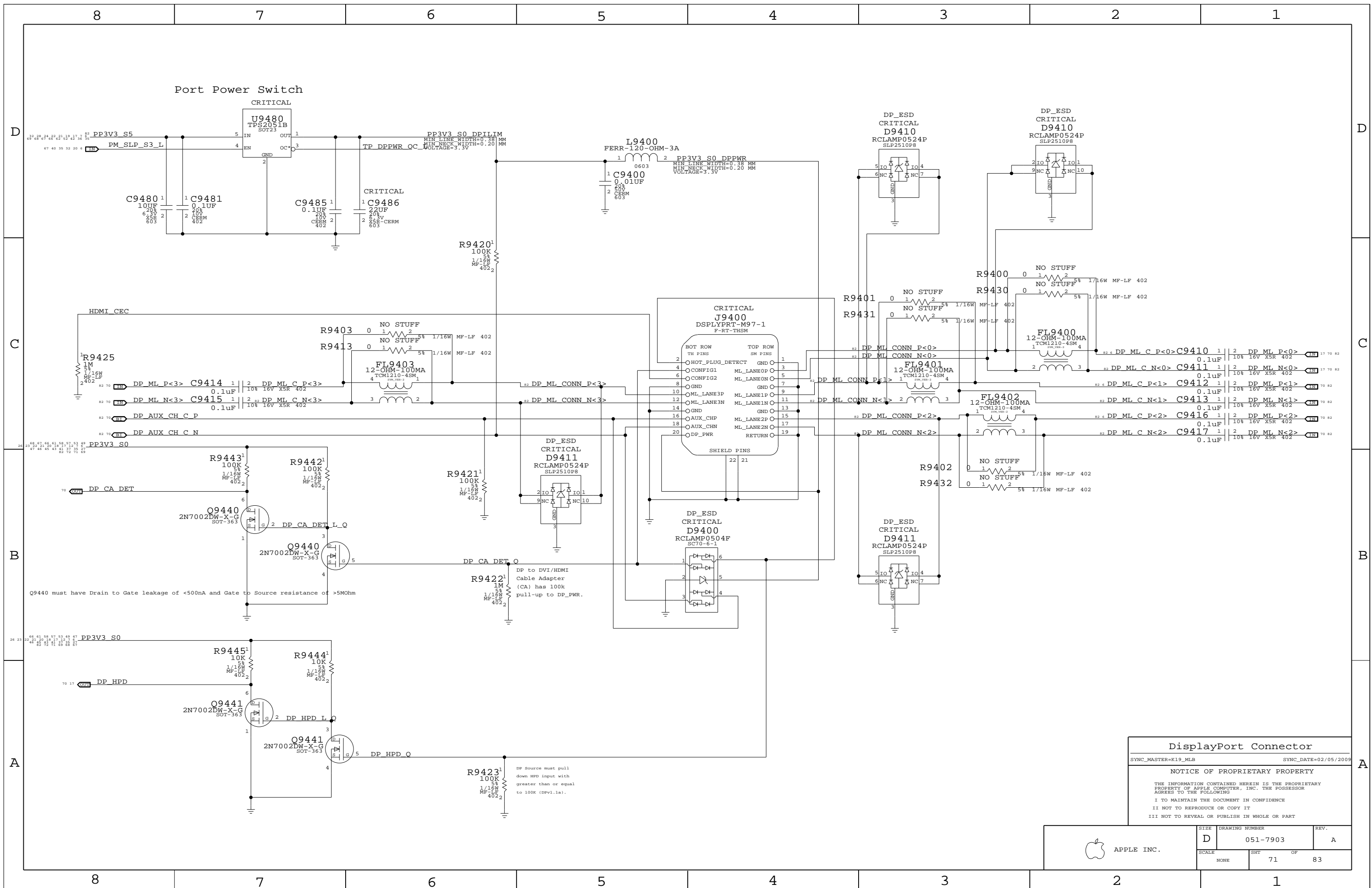
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT OF		
NONE	70 OF		83



**DisplayPort Connector**

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/05/2009

**NOTICE OF PROPRIETARY PROPERTY**

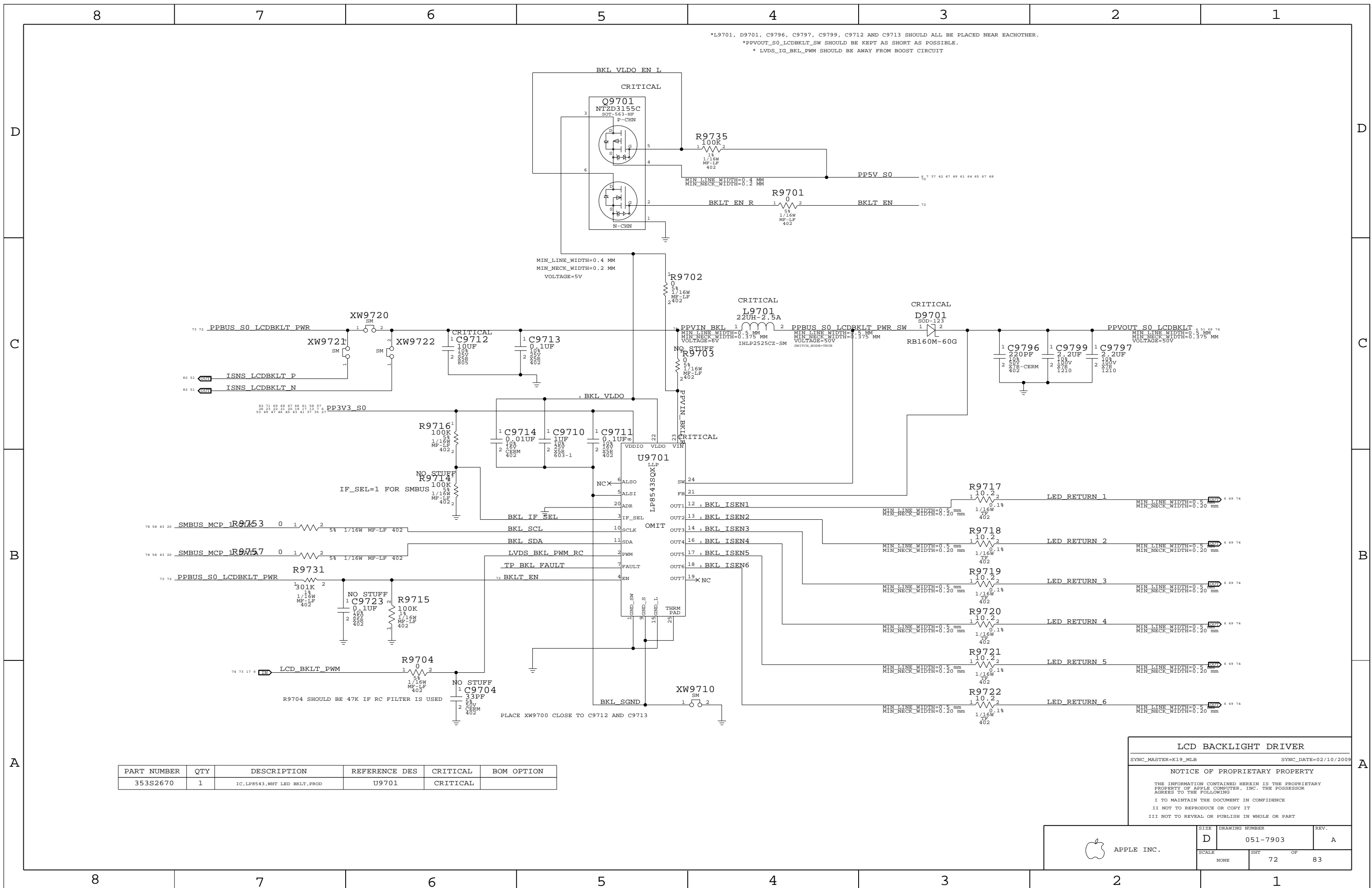
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APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7903	REV. A
	SCALE NONE	SHIT 71	OF 83



\*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.  
 \*PPVOUT\_S0\_LCDBKLT\_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.  
 \* LVDS\_IG\_BKL\_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHI LED BKLT,PROD	U9701	CRITICAL	

**LCD BACKLIGHT DRIVER**

SYNC\_MASTER=K19\_MLB SYNC\_DATE=02/10/2009

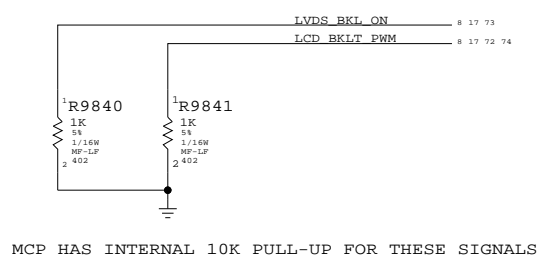
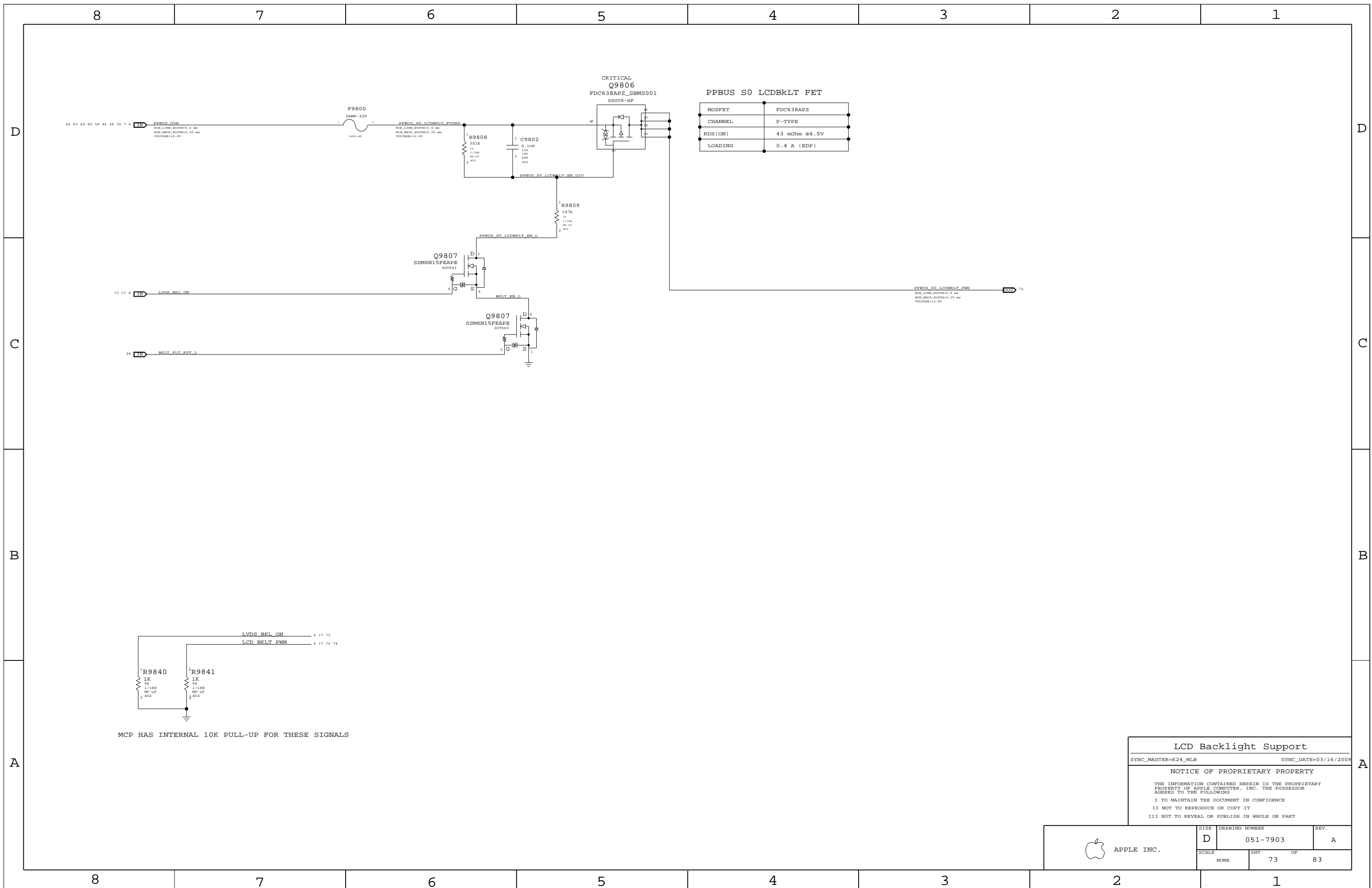
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	72		83





**LCD Backlight Support**

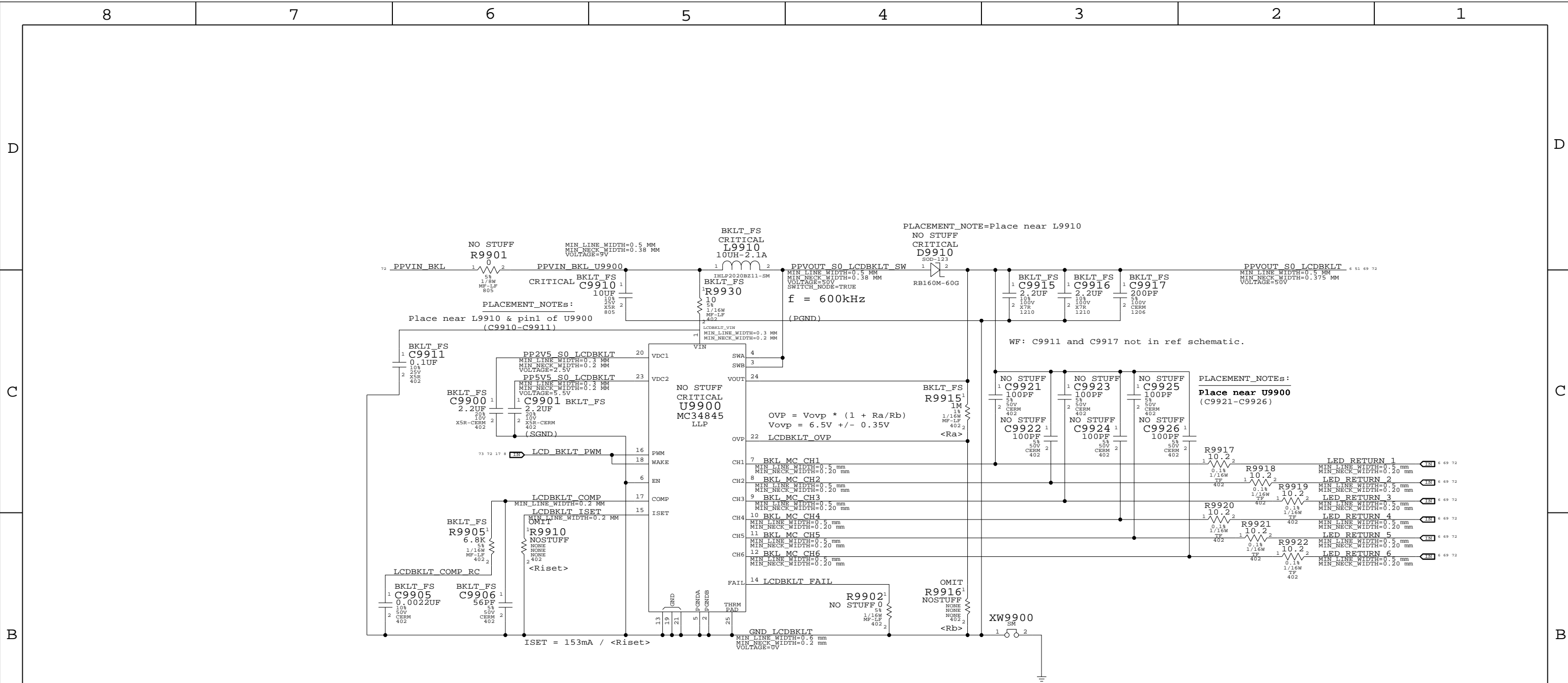
SYNC\_MASTER=K24\_MLB SYNC\_DATE=03/16/2009

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	SIZE	DRAWING NUMBER	REV.
	D	051-7903	A
SCALE	SHT	OF	
NONE	73	83	



### 13.3 Inch Panel (9 LEDs per string)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0298	1	RES.MTL FILM,1/16W,6.65K,1,0402,SMD,LF	R9910	?	LCD_13INCH
114S0445	1	RES.MTL FILM,1/16W,226K,1,0402,SMD,LF	R9916	?	LCD_13INCH

WF: Need 6.65K 0.1% resistor?

Target: ISET = 23mA, OVP = 35V  
Actual: ISET = 23mA, OVP = 35.2V

### 15.4 Inch Panel (10/11 LEDs per string)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0298	1	RES.MTL FILM,1/16W,6.65K,1,0402,SMD,LF	R9910	?	LCD_15INCH
114S0438	1	RES.MTL FILM,1/16W,191K,1,0402,SMD,LF	R9916	?	LCD_15INCH

WF: Need 6.65K 0.1% resistor?

Target: ISET = 23mA, OVP = 40V  
Actual: ISET = 23mA, OVP = 40.5V

### 17 Inch Panel (14 LEDs per string)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0299	1	RES.MTL FILM,1/16W,6.81K,1,0402,SMD,LF	R9910	?	LCD_17INCH
114S0428	1	RES.MTL FILM,1/16W,150K,1,0402,SMD,LF	R9916	?	LCD_17INCH

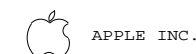
WF: Need 6.80K 0.1% resistor?

Target: ISET = 22.5mA, OVP = 50V  
Actual: ISET = 22.47mA, OVP = 49.8V

LCD Backlight Driver (MC34845)  
SYNC\_MASTER=VEMURI\_K19I SYNC\_DATE=02/09/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	74	83

## FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADSTB#s should be matched +/- 300 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

## CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

## MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

## FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

## CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	9 13
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	9 13
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	9 13
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	9 13
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	9 13
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0 L	9 13
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1 L	13
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	9 13
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	9 13
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	9 13
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9 13
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	9 13 41
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	9 13 41
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	9 13
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM THRMTRIP L	9 13 41
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	9 13
CPU_PROM_SR	CPU_50S	CPU_AGTL	CPU DPSLP L	9 13
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	9 13 41
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	9 13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	9 13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	9 13
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	12 13
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	12 13
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	13
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	13
CPU_IERR_L	CPU_50S		CPU IERR L	9
PM DPRSLVPR	CPU_50S	CPU_AGTL	PM DPRSLVPR	20 61
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLVPR	61
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	9 26
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	9
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	9
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	9 12
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	9 12
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	9 12
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	9 12
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	9 12
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	9 12
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	9 12
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	12
	CPU_50S	CPU_8MIL	CPU VID<6..0>	8 10
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>	8 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	10 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	10 61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	61

## CPU/FSB Constraints

SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	75	83

## Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

## Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM\_\*-style wildcards!

**DDR2:**  
 DQ signals should be matched within 20 ps of associated DQS pair.  
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.  
 All DQS pairs should be matched within 100 ps of clocks.  
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.  
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.  
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).  
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

**DDR3:**  
 DQ signals should be matched within 5 ps of associated DQS pair.  
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps  
 No DQS to clock matching requirement.  
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.  
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.  
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).  
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3  
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

## MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

## Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0>
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS L
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS L
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE L
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0>
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS L
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS L
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE L
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND

## Memory Constraints

SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	76	83

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedance varies by location:  
 - 37.5-ohm from MCP to first termination resistor.  
 - 50-ohm from first to second termination resistor.  
 - 75-ohm from output of three-pole filter to connector (if possible).  
 R/G/B signals should be matched as close as possible and < 10 inches.  
 SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches.  
 SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_90D	PCIE	PEG R2D P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C N<15..0>
PCIE_MINI_R2D_P	PCIE_90D	PCIE	PCIE MINI R2D P 6 29 82
PCIE_MINI_R2D_N	PCIE_90D	PCIE	PCIE MINI R2D N 6 29 82
PCIE_MINI_R2D_C_P	PCIE_90D	PCIE	PCIE MINI R2D C P 16 29
PCIE_MINI_R2D_C_N	PCIE_90D	PCIE	PCIE MINI R2D C N 16 29
PCIE_MINI_D2R_P	PCIE_90D	PCIE	PCIE MINI D2R P 6 16 29
PCIE_MINI_D2R_N	PCIE_90D	PCIE	PCIE MINI D2R N 6 16 29
PCIE_FW_R2D_P	PCIE_90D	PCIE	PCIE FW R2D P 34
PCIE_FW_R2D_N	PCIE_90D	PCIE	PCIE FW R2D N 34
PCIE_FW_R2D_C_P	PCIE_90D	PCIE	PCIE FW R2D C P 16 34
PCIE_FW_R2D_C_N	PCIE_90D	PCIE	PCIE FW R2D C N 16 34
PCIE_FW_D2R_P	PCIE_90D	PCIE	PCIE FW D2R P 16 34
PCIE_FW_D2R_N	PCIE_90D	PCIE	PCIE FW D2R N 16 34
PCIE_FW_D2R_C_P	PCIE_90D	PCIE	PCIE FW D2R C P 34
PCIE_FW_D2R_C_N	PCIE_90D	PCIE	PCIE FW D2R C N 34
PCIE_EXCARD_R2D_P	PCIE_90D	PCIE	PCIE EXCARD R2D P
PCIE_EXCARD_R2D_N	PCIE_90D	PCIE	PCIE EXCARD R2D N
NC_PCIE_EXCARD_R2DCP	PCIE_90D	PCIE	NC PCIE EXCARD R2DCP 8 16
NC_PCIE_EXCARD_R2DCN	PCIE_90D	PCIE	NC PCIE EXCARD R2DCN 8 16
NC_PCIE_EXCARD_D2RP	PCIE_90D	PCIE	NC PCIE EXCARD D2RP 8 16
NC_PCIE_EXCARD_D2RN	PCIE_90D	PCIE	NC PCIE EXCARD D2RN 8 16
NC_PCIE_CLK100MP	CLK_PCIE_100D	CLK_PCIE	NC PEG CLK100MP 8 16
NC_PCIE_CLK100MN	CLK_PCIE_100D	CLK_PCIE	NC PEG CLK100MN 8 16
PCIE_CLK100M_MINI_P	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P 16 29
PCIE_CLK100M_MINI_N	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N 16 29
PCIE_CLK100M_FW_P	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P 16 34
PCIE_CLK100M_FW_N	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N 16 34
NC_PCIE_CLK100M_EXCARDP	CLK_PCIE_100D	CLK_PCIE	NC PCIE CLK100M EXCARDP 8 16
NC_PCIE_CLK100M_EXCARDN	CLK_PCIE_100D	CLK_PCIE	NC PCIE CLK100M EXCARDN 8 16
MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP_PEX_COMP	MCP PEX CLK COMP 16
NC_CRT_IG_R_C_PR	CRT_50S	CRT	NC CRT IG R C PR 17 23
NC_CRT_IG_G_Y_Y	CRT_50S	CRT	NC CRT IG G Y Y 17 23
NC_CRT_IG_B_COMP_PB	CRT_50S	CRT	NC CRT IG B COMP PB 17 23
NC_CRT_IG_HSYNC	CRT_50S	CRT_SYNC	NC CRT IG HSYNC 17 23
NC_CRT_IG_VSYNC	CRT_50S	CRT_SYNC	NC CRT IG VSYNC 17 23
NC_MCP_TV_DAC_RSET	MCP_DAC_COMP	MCP_DAC_COMP	NC MCP TV DAC RSET 17 23
NC_MCP_TV_DAC_VREF	MCP_DAC_COMP	MCP_DAC_COMP	NC MCP TV DAC VREF 17 23
TMDS_IG_TXC_P	DP_100D	DISPLAYPORT	TMDS IG TXC P
TMDS_IG_TXC_N	DP_100D	DISPLAYPORT	TMDS IG TXC N
TMDS_IG_TXD_P<2..0>	DP_100D	DISPLAYPORT	TMDS IG TXD P<2..0>
TMDS_IG_TXD_N<2..0>	DP_100D	DISPLAYPORT	TMDS IG TXD N<2..0>
DP_IG_ML_P<3..0>	DP_100D	DISPLAYPORT	DP IG ML P<3..0>
DP_IG_ML_N<3..0>	DP_100D	DISPLAYPORT	DP IG ML N<3..0>
DP_IG_AUX_CH_P	DP_100D	DISPLAYPORT	DP IG AUX CH P 17 70
DP_IG_AUX_CH_N	DP_100D	DISPLAYPORT	DP IG AUX CH N 17 70
MCP_HDMI_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP HDMI RSET 17 23
MCP_HDMI_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP HDMI VPROBE 17 23
LVDS_CONN_A_CLK_P	LVDS_100D	LVDS	LVDS CONN A CLK P 8 17 69
LVDS_CONN_A_CLK_N	LVDS_100D	LVDS	LVDS CONN A CLK N 8 17 69
LVDS_IG_A_DATA_P<2..0>	LVDS_100D	LVDS	LVDS IG A DATA P<2..0> 8 17
LVDS_IG_A_DATA_N<2..0>	LVDS_100D	LVDS	LVDS IG A DATA N<2..0> 8 17
NC_LVDS_IG_A_DATAP<3>	LVDS_100D	LVDS	NC LVDS IG A DATAP<3> 8 17
NC_LVDS_IG_A_DATAN<3>	LVDS_100D	LVDS	NC LVDS IG A DATAN<3> 8 17
LVDS_CONN_B_CLK_P	LVDS_100D	LVDS	LVDS CONN B CLK P 8 17 69
LVDS_CONN_B_CLK_N	LVDS_100D	LVDS	LVDS CONN B CLK N 8 17 69
LVDS_IG_B_DATA_P<2..0>	LVDS_100D	LVDS	LVDS IG B DATA P<2..0> 8 17
LVDS_IG_B_DATA_N<2..0>	LVDS_100D	LVDS	LVDS IG B DATA N<2..0> 8 17
NC_LVDS_IG_B_DATAP<3>	LVDS_100D	LVDS	NC LVDS IG B DATAP<3> 8 17
NC_LVDS_IG_B_DATAN<3>	LVDS_100D	LVDS	NC LVDS IG B DATAN<3> 8 17
MCP_IFPAB_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP IFPAB RSET 17 23
MCP_IFPAB_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP IFPAB VPROBE 17 23
SATA_HDD_R2D_C_P	SATA_100D	SATA	SATA HDD R2D C P 19 37
SATA_HDD_R2D_C_N	SATA_100D	SATA	SATA HDD R2D C N 19 37
SATA_HDD_R2D_P	SATA_100D	SATA	SATA HDD R2D P 6 37
SATA_HDD_R2D_N	SATA_100D	SATA	SATA HDD R2D N 6 37
SATA_HDD_D2R_P	SATA_100D	SATA	SATA HDD D2R P 19 37
SATA_HDD_D2R_N	SATA_100D	SATA	SATA HDD D2R N 19 37
SATA_HDD_D2R_C_P	SATA_100D	SATA	SATA HDD D2R C P 6 37
SATA_HDD_D2R_C_N	SATA_100D	SATA	SATA HDD D2R C N 6 37
SATA_ODD_R2D_C_P	SATA_100D	SATA	SATA ODD R2D C P 19 37
SATA_ODD_R2D_C_N	SATA_100D	SATA	SATA ODD R2D C N 19 37
SATA_ODD_R2D_P	SATA_100D	SATA	SATA ODD R2D P 6 37
SATA_ODD_R2D_N	SATA_100D	SATA	SATA ODD R2D N 6 37
SATA_ODD_D2R_P	SATA_100D	SATA	SATA ODD D2R P 19 37
SATA_ODD_D2R_N	SATA_100D	SATA	SATA ODD D2R N 19 37
SATA_ODD_D2R_C_P	SATA_100D	SATA	SATA ODD D2R C P 6 37
SATA_ODD_D2R_C_N	SATA_100D	SATA	SATA ODD D2R C N 6 37
MCP_SATA_TERM	SATA_TERM	SATA_TERM	MCP SATA TERM 19

**MCP Constraints 1**

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## PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.8.

## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.9.1.

## USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAIS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.10.1.

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.11.1.

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.12.1.

## SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.13.

## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.14.

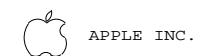
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	12 18
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	12 18
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	12 18
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	12 18
PCI_AD	PCI_55S	PCI	PCI_PAR	12 18
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_IRDY_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_DEVSEL_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_PERR_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_SERR_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_STOP_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_TRDY_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_FRAME_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_REQ0_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_REQ0_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_GNT0_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_REQ1_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_GNT1_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_INTW_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_INTX_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_INTY_L	12 18
PCI_CNTRL	PCI_55S	PCI	PCI_INTZ_L	12 18
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP_R	18
CLK_PCI_55S	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP	18
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	18 40 42
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	18 40 42
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	18 24
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R	18 24
CLK_LPC_55S	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC	24 40
CLK_LPC_55S	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS	24 42
USB_EXTA	USB_90D	USB	USB_EXTA_P	19 38
USB_90D	USB_90D	USB	USB_EXTA_N	19 38
USB_90D	USB_90D	USB	USB_EXTA_MUXED_P	19 38
USB_90D	USB_90D	USB	USB_EXTA_MUXED_N	19 38
USB_MINI	USB_90D	USB	NC_USB_MINIP	8 19
USB_90D	USB_90D	USB	NC_USB_MININ	8 19
USB_EXTD	USB_90D	USB	NC_USB_EXTDP	8 19
USB_90D	USB_90D	USB	NC_USB_EXTDN	8 19
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	6 19 29
USB_90D	USB_90D	USB	USB_CAMERA_N	6 19 29
USB_BT	USB_90D	USB	USB_BT_P	6 19 29
USB_90D	USB_90D	USB	USB_BT_N	6 19 29
USB_TPAD	USB_90D	USB	USB_TPAD_P	19 48
USB_90D	USB_90D	USB	USB_TPAD_N	19 48
USB_IR	USB_90D	USB	USB_IR_P	19 39
USB_90D	USB_90D	USB	USB_IR_N	19 39
USB_EXTB	USB_90D	USB	USB_EXTB_P	19 38
USB_90D	USB_90D	USB	USB_EXTB_N	19 38
USB_EXCARD	USB_90D	USB	NC_USB_EXCARDP	8 19
USB_90D	USB_90D	USB	NC_USB_EXCARDN	8 19
USB_EXTC	USB_90D	USB	NC_USB_EXTCP	8 19
USB_90D	USB_90D	USB	NC_USB_EXTCN	8 19
USB_CARDREADER	USB_90D	USB	USB_CARDREADER_P	19 30
USB_90D	USB_90D	USB	USB_CARDREADER_N	19 30
MCP_USB_RBIAIS	MCP_USB_RBIAIS		MCP_USB_RBIAIS_GND	19
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	12 20 26 27 43
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	12 20 26 43
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	20 43 58 72
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	20 43 58 72
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	20 53
HDA_55S	HDA_55S	HDA	HDA_BIT_CLK_R	20 53
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	20 53
HDA_55S	HDA_55S	HDA	HDA_SYNC_R	20 53
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	20 53
HDA_55S	HDA_55S	HDA	HDA_RST_L	20 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	20 53
HDA_55S	HDA_55S	HDA	HDA_SDIN_CODEC	20 53
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	20 53
HDA_55S	HDA_55S	HDA	HDA_SDOUT_R	20 53
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP_HDA_PULLDN_COMP	20
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	20 24
CLK_SLOW_55S	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	24 40
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	20 42
SPI_55S	SPI_55S	SPI	SPI_CLK	52
SPI_MOST	SPI_55S	SPI	SPI_MOST_R	20 42
SPI_55S	SPI_55S	SPI	SPI_MOST	52
SPI_MISO	SPI_55S	SPI	SPI_MISO	20 42
SPI_55S	SPI_55S	SPI	SPI_MISO_R	52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	20 42
SPI_55S	SPI_55S	SPI	SPI_CS0_L	52

## MCP Constraints 2

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SIZE	DRAWING NUMBER	REV.
D	051-7903	A
SCALE	SHT	OF
NONE	78	83

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD 17
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND 17
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R 17 32
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1 31 32
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET INTR L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO 17 31
ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC 17 31
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET PWRDWN L
	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R 31
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK 17 31
	ENET_MII_55S	ENET_MII	ENET RXD R<3..0> 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET RXD<0> 17 31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<3..1> 17 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET RX CTRL 17 31
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK 17 31
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET TXD<0> 17 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TXD<3..1> 17 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TX CTRL 17 31
	ENET_MII_55S	ENET_MII	ENET RESET L 17 31
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0> 31 33
	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0> 31 33

Ethernet Constraints

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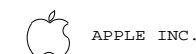
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### FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

### FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	
	PHYSICAL			
EW_P0_TPA	EW_110D	EW_TP	NC FW0 TPAP	34 36
EW_P0_TPB	EW_110D	EW_TP	NC FW0 TPAN	34 36
EW_P0_TPB	EW_110D	EW_TP	NC FW0 TPBP	34 36
EW_P0_TPB	EW_110D	EW_TP	NC FW0 TPBN	34 36
EW_P1_TPA	EW_110D	EW_TP	FW PORT1 TPA P	34 36
EW_P1_TPA	EW_110D	EW_TP	FW PORT1 TPA N	34 36
EW_P1_TPB	EW_110D	EW_TP	FW PORT1 TPB P	34 36
EW_P1_TPB	EW_110D	EW_TP	FW PORT1 TPB N	34 36
Port 2 Not Used				

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### FireWire Constraints

SYNC\_MASTER=T18\_MLB SYNC\_DATE=02/05/2009

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NONE	80	83

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IT01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

### SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SMBUS_SMC	SCL	SDA	X	Y
	PHYSICAL	SPACING					
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL			6 29 40 43 49	
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA			6 29 40 43 49	
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL			40 43 46	
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA			40 43 46	
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL			40 43 46 51	
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA			40 43 46 51	
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL			6 40 43 59 60	
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA			6 40 43 59 60	
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL			25 37 40 43	
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA			25 37 40 43	

### SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		CHGR	Type	X	Y
	PHYSICAL	SPACING				
CHGR_CSI	IT01_DIFFPAIR		CHGR_CSI_P			60
	IT01_DIFFPAIR		CHGR_CSI_N			60
CHGR_CSO	IT01_DIFFPAIR		CHGR_CSO_P			60
	IT01_DIFFPAIR		CHGR_CSO_N			60

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### SMC Constraints

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# K19i Board-Specific Physical & Spacing Constraints

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA				MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.080 MM	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.151 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_LPC	*	BGA	BGA_P2MM
CLK_PCI	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA	STANDARD
MEM_40S_VDD	BGA	STANDARD

## K19i PCB Rule Definitions

SYNC\_MASTER=WFERRY\_K19I SYNC\_DATE=12/12/2008

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