1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,CANNAREGIO,K20,DVT1

12/12/08

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
31		657084	ENGINEERING RELEASED	12/12/08	?

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7656	1	SCHEM,CANNAREGIO,K20	SCH	CRITICAL	
820-2390	1	PCBF,CANNAREGIO,K20	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Dec 12 16:50:42 2008

DIMENSIONS ARE IN MILLIMETERS

XX ±

X.XX ±

X.XXX ±

ANGLES ±

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

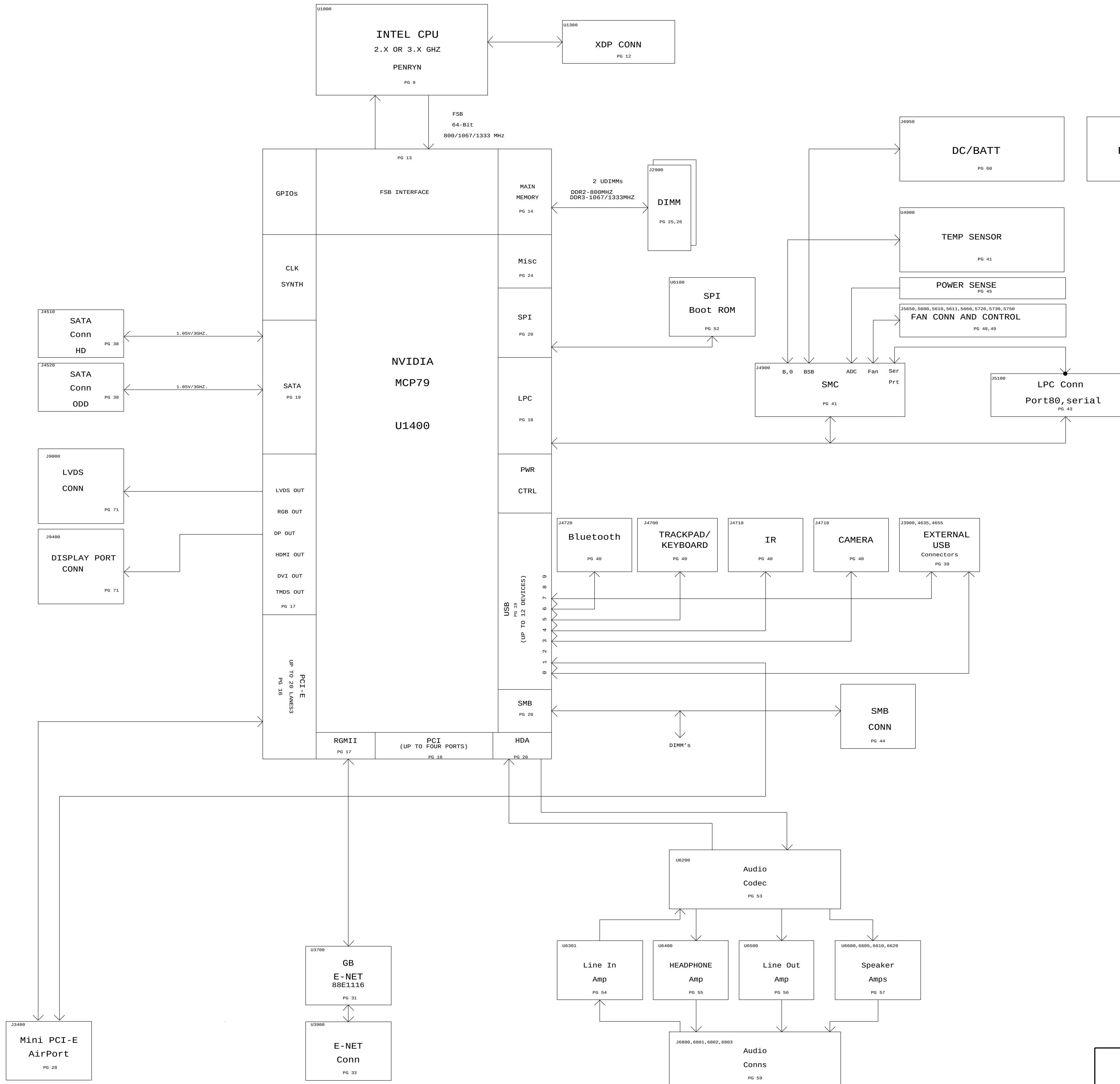
SIZE D

APPLE INC.

TITLE
SCHEM,CANNAREGIO,K20

DRAWING NUMBER 051-7656

REV. 31



System Block Diagram

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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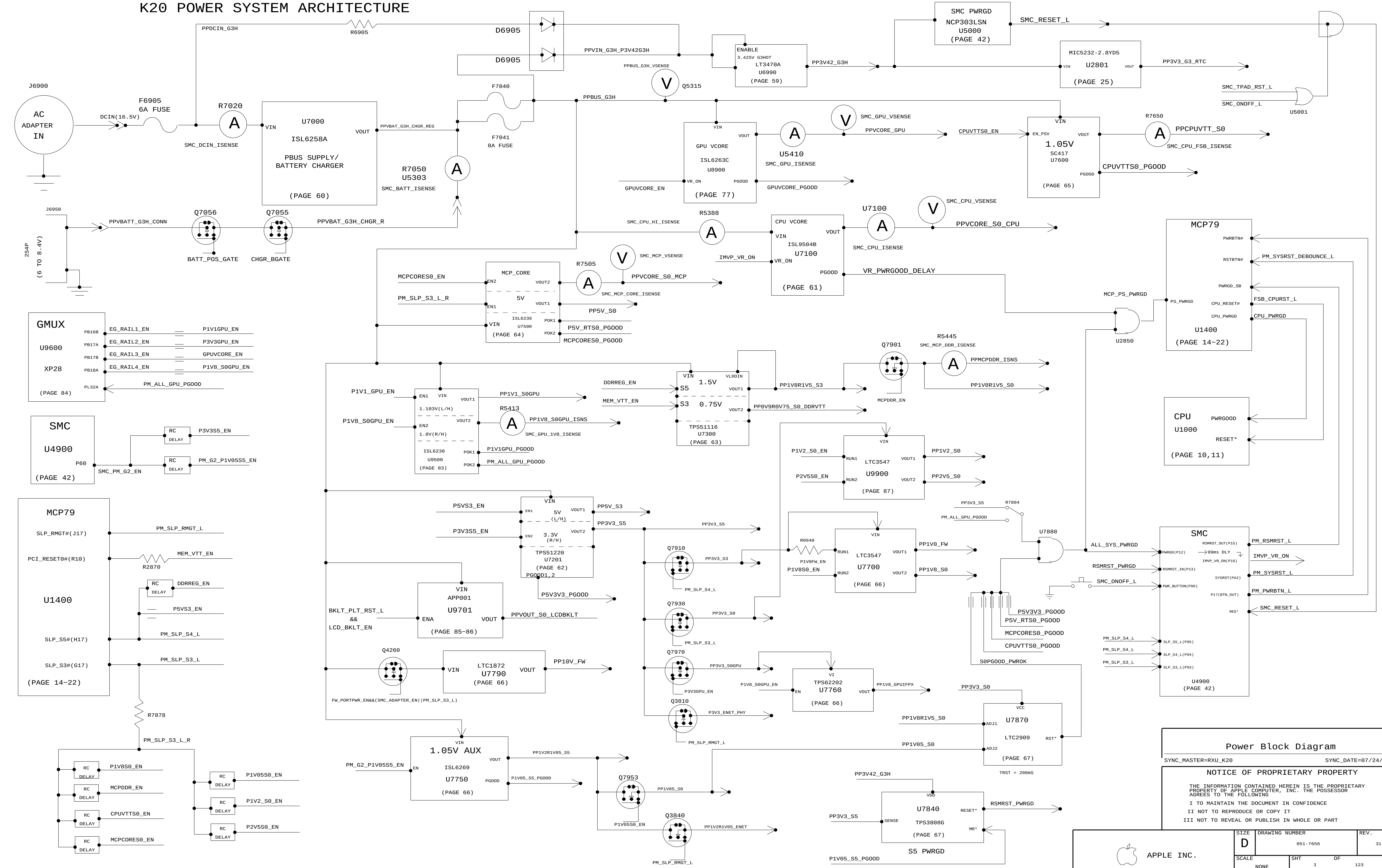
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 2	OF 123

K20 POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=RXU_K20 SYNC_DATE=07/24/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 3	OF 123

Proto:

See earlier schematics for info about proto changes

Pre-EVT:

See earlier schematics for info about Pre-EVT changes

EVT:

10/29/08
csa. 5 Added BKLT_PLL_NOT BOM option K20_COMMON2 BOM group. This stuffs R9713.
csa. 68 Changed net name on input to U6860 from PP3V3_S0_AUDIO to =PP3V3_S0_AUDIO.
See <rdar://problem/6327731> K20 PreEVT: iPhone headset detection test fail
csa. 97 Changed R9707 to 2.87K per <rdar://problem/6327135> Change R9707 to 2.87k, 1% resistor
10/29/08
csa. 9 Changed SH0924 to 870-1698 tall emi pogo pin.
11/5/08
    csa. 4 Updated Revision History.
csa. 8 Tied =PP3V3_FW_FWPHY and =PP3V3_FW_P1V0FW aliases to PP3V3_S0.
csa. 9 Removed R0942 and R0943 which were for selecting from S0 or S3 for =PP3V3_FW_FWPHY.
Removed R0940 and R0941 which were for selecting from S0 or S3 for =PP3V3_FW_P1V0FW.
Tied =PP3V3_S3_GMUX alias to PP3V3_S3.
csa. 75 Changed U7500 from 353S2312 Intersil ISL6236 to 353S2203 TI SN0802043.
Changed TONSEL from GND to PP5V_S0_MCPREG_VCC. This changes output frequencies to 200/300KHz for 5V/MCPCore.
Added C7562 330uF cap on =PPMCPCORE_S0_REG.
Changed snubber resistors R7598 and R7599 to 1/6W 0402, APN 114S0548.
csa. 87 Changed pulldown values to 10K on GPIO7_FBVDDQ_ALTVO, R8794.
Changed pulldowns R8792 and R8793 from 1K to 4.7K for power consumption.
csa. 90 Removed R9094. Replaced by R9678 on csa. 96 to tie to GMUX_S3_PD_GND.
csa. 96 Added Q9607 dual FET for disabling GMUX power sequence enable configuration pulldowns during S0.
Moved R9094 to R9678 and tied to GMUX_S3_PD_GND.
csa. 97 Changed R9707 to 2.67K 1%. This gives 22.5mA on LED current.
11/10/08
csa. 68 Changed R6885 from 0 ohms to 2.2K.
Changed C6885 from 470 pF to 0.0082 uF.
csa. 87 Changed R8792 and R8793 from 4.7K to 10K pulldowns on EG_LCD_PWR_EN and EG_BKLT_EN.
csa. 96 Changed R9678 pulldown on LCD_PWR_EN from 10K to 4.7K.
Removed BOM options on FET circuit for GMUX_S3_PD_GND.
Added R9684 NO STUFF 0 ohms to tie ALL_SYS_PWRGD to Q9607.
11/11/08
csa. 8 removed =PP3V3_S3_P1V0FW and =PP3V3_S3_BKL_VDDIO
csa. 41 changed R4160 from 274K to 200K <rdar://6292976>
csa. 68 changed R6885 from 0 ohm to 2.2K for Mic LPF
csa. 75 NO STUFF R7598, C7598, R7599, C7599 (snubbers)
csa. 87 changed R8795 from 1K to 10K pull down
csa. 96 NO STUFF R9677, C9695, STUFF R9684
11/12/08
csa. 5 removed MCP79 B01 from Module Parts table and added B03
csa. 39 added Bom table for J3900 (514-0636)
csa. 46 added Bom table for J4600, J4610 (514-0638)
csa. 94 added Bom table for J9400 (514-0637)
csa. 123 added Bom table for JC320 (514-0638)
11/13/08
csa. 1 change title to DVT
csa. 32 Added alternate table for J3200 (516S0709, Molex DIMM connector)
11/19/08
csa. 5 changed MCP79 B03 to 338S0710; change to binned G96 338S0714;
      added PROD_DIGSMS and TPDT_DEBOUNCE to BOM groups
csa. 68 added bom option TPDT_BYPASS to R6865; TPDT_DEBOUNCE to U6860,C6861,R6860,R6862
csa. 97 changed Q9701 to 376S0757 <radr://6383480>
11/25/08
csa. 5 changed BOM option MCP_B02 to MCP_B03; added BOM option GMUX_1V8
added Mag Layer alternate 155S0457 to Murata 155S0329
csa. 93 added BOM table for 16 LVDS termination resistors to select GMUX_2V5 or GMUX_1V8
added BOM option GMUX_2V5 to 8 parallel resistors so they'll be NO STUFFed for GMUX_1V8
csa. 97 reverted Q9701 to 376S0678 due to parts availability
csa. 99 added BOM table for R9900 to select either 2.5V output or 1.8V output

DVT:

12/02/08
Start of PVT.
csa. 5 removed JTAG_ALLDEV bom option to remove U0600, R0601, C0601, C0602
      added 516-0213 (Molex TH SODIMM CONN) as alternate to 516-0201 (Foxconn)
      added GMUX_JTAG_CONN bom option to the bom table
csa. 6 added GMUX_JTAG_CONN bom option to J0600
csa. 99 moved OMIT from R9900 to R9901 to select either 150K (GMUX_2V5) or 237K (GMUX_1V8)
12/03/08
csa. 32 removed redundant alternate table for J3200
csa. 97 Per radar 6383480, Change the FET Q9701 from APN: 376S0678 to 376S0757
diode D9701 from APN: 371S0551 to 371S0572
12/09/08
csa. 1 changed title to DVT(1)
csa. 26 NO STUFF C2690, R2690
csa. 32 Refreshed symbol for J3200 for update to BGA SODIMM conn.
csa. 54 changed R5498 to 4.02K for 1.4x gain and R5493 to 2.87K <rdar://6423810>
csa. 89 changed L8920 to 152S0955 (25A Isat); R8900 to 7.15K for 24.6A OCP <rdar://6423810>

12/12/08
csa. 1 changed title to DVT1
csa. 4 removed pre-EVT check in notes from Rev. History
csa. 99 changed text note to reflect 2.5V to 1.8V GMUX rail change

31

SYNC_MASTER=NA SYNC_DATE=NA

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	4	123

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9728	PCBA,BEST,2.66,512SAM_VRAM,K20	K20_COMMON,EEE_4CM,CPU_2_66GHZ,FB_512_SAMSUNG
630-9727	PCBA,BEST,2.66,512QIM_VRAM,K20	K20_COMMON,EEE_4CH,CPU_2_66GHZ,FB_512_QIMONDA
630-9730	PCBA,BEST,2.93,512SAM_VRAM,K20	K20_COMMON,EEE_4CQ,CPU_2_93GHZ,FB_512_SAMSUNG
630-9729	PCBA,BEST,2.93,512QIM_VRAM,K20	K20_COMMON,EEE_4CP,CPU_2_93GHZ,FB_512_QIMONDA

K20 BOM GROUPS

BOM GROUP	BOM OPTIONS
K20_COMMON	ALTERNATE,COMMON,K20_COMMON1,K20_COMMON2,K20_DEBUG,K20_PROGPARTS
K20_COMMON1	ONEWIRE_PU,ISL6258,MEMRESET_HW,MEMRESET_MCP,MCP_B03,MCP_PROD,MCPSEQ_SMC,BMON_ENG,MCP_CS1_NO,FW_LVG_NEW,PROD_DIGSMS,TPDT_DEBOUNCE
K20_COMMON2	BOOT_MODE_USER,GPUVID_1P00V,MUXGFX,DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_GMUX,DP_CA_DET_EG_PLD,BKLT_PLL_NOT,GMUX_1V8
K20_DEBUG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,TPAD_DEBUG,GMUX_JTAG_CONN
K20_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_1024_SAMSUNG	VRAM8,VRAM_1024_SAMSUNG
FB_1024_QIMONDA	VRAM8,VRAM_1024_QIMONDA
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_QIMONDA	VRAM4,VRAM_512_QIMONDA

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CH]	CRITICAL	EEE_4CH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CM]	CRITICAL	EEE_4CM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CP]	CRITICAL	EEE_4CP
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CQ]	CRITICAL	EEE_4CQ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0782		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
514-0612	514-0607		ALL	FOXLINK ALT TO FOXCONN XCVR
514-0613	514-0608		ALL	FOXLINK ALT TO FOXCONN RCVR
152S0684	152S0421		ALL	MAG LAYERS ALT TO VISHAY
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
516S0709	516S0706		ALL	MOLEX ALT TO FOXCONN
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
516-0213	516-0201		ALL	MOLEX ALT TO FOXCONN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3645	1	IC,PDC,QXXX,QS,2.66,25W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3644	1	IC,PDC,QXXX,QS,2.86,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_86GHZ
338S0714	1	IC,ASSP,GPU,NV G96-GS,LOWLKG,BGA969,LF	U8000	CRITICAL	
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0710	1	IC,MCP79XT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2355	1	IC,SMC,DEVELOPMENT,K20	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2356	1	IC,EFI ROM,DEVELOPMENT,K20	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
338S0603	1	IC,GMCP,MCP79-A01Q,35x35MM,BGA1437	U1400	CRITICAL	MCP_A01Q
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3643	1	IC,PDC,QXXX,QS,2.93,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_93GHZ
337S3640	1	IC,PDC,SL3BX,PRQ,2.53,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3641	1	IC,PDC,SLB43.PRQ,2.80,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
338S0635	1	IC,GMCP,MCP79-B02,35x35MM,BGA1437	U1400	CRITICAL	MCP_B02
333S0481	4	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0472	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_QIMONDA
333S0481	8	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_1024_SAMSUNG
333S0472	8	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_1024_QIMONDA

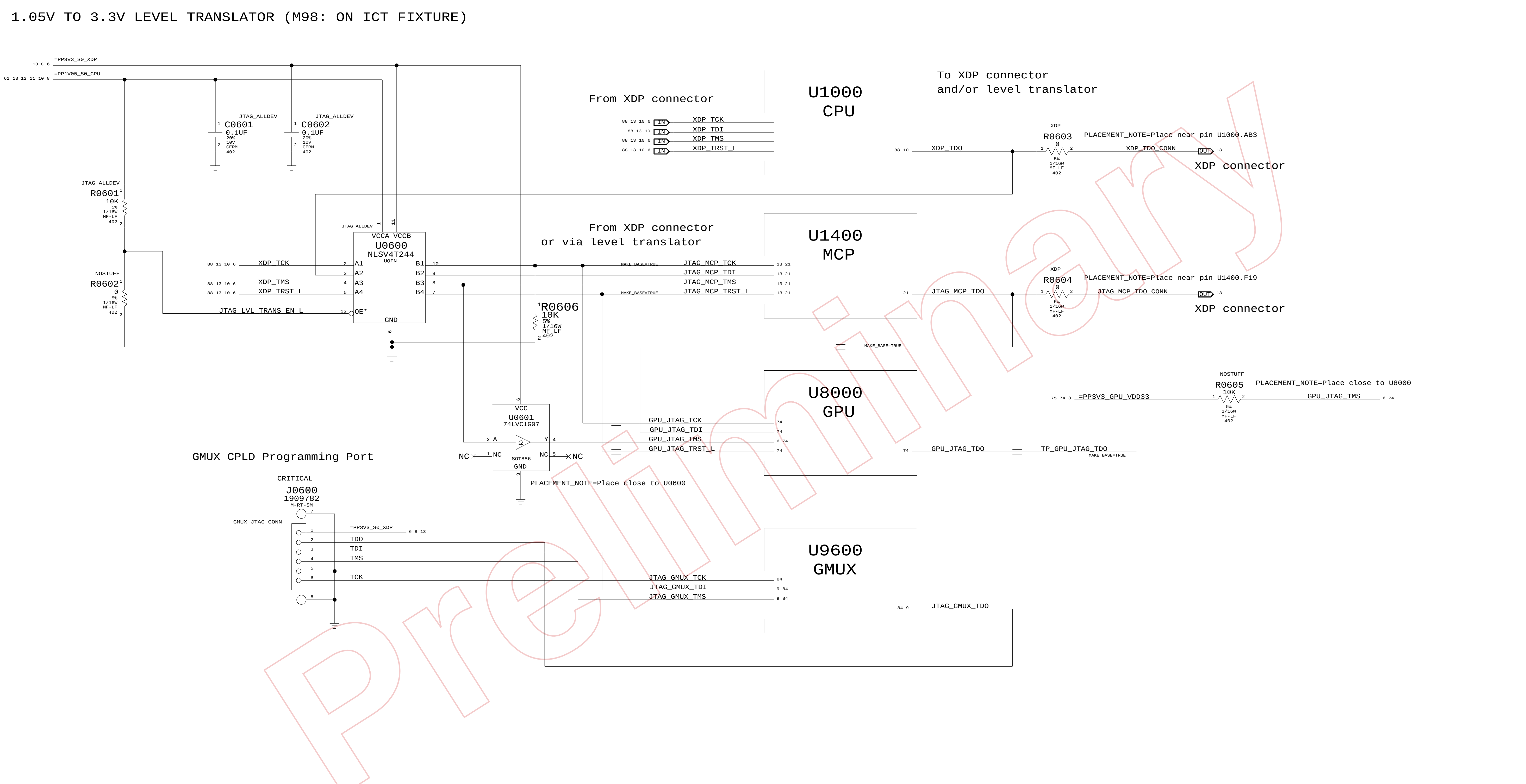
BOM Configuration

SYNC_MASTER=K20_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	5	123



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE NONE SHT 6 OF 123

Functional Test Points

J5650 (LEFT FAN CONN)
FUNC_TEST
- =PP5V_S0_FAN_LT
- FAN_LT_PWM
- FAN_LT_TACH

3 TPs per Fan

J5660 (RIGHT FAN CONN)
- FAN_RT_PWM
- FAN_RT_TACH
- GND

5 TPs per Fan

J6780 (MIC CONN)
- BI_MIC_LO
- BI_MIC_SHIELD
- BI_MIC_HI

J6781 (LEFT SPEAKER)
- SPKRAMP_L1_OUT_P
- SPKRAMP_L1_OUT_N
- SPKRAMP_L2_OUT_P
- SPKRAMP_L2_OUT_N

J6782 (RIGHT & SUB SPEAKER)
- SPKRAMP_LFE_OUT_P
- SPKRAMP_LFE_OUT_N
- SPKRAMP_R1_OUT_P
- SPKRAMP_R1_OUT_N
- SPKRAMP_R2_OUT_P
- SPKRAMP_R2_OUT_N

J9000 (LVDS CONN)
- BKL_SYNC
- PP3V3_SW_LCD
- =PP3V3_S0_DDC_LCD
- PPVOUT_S0_LCDBKLT
- LVDS_DDC_CLK
- LVDS_DDC_DATA
- LVDS_CONN_A_DATA_P<0>
- LVDS_CONN_A_DATA_N<0>
- LVDS_CONN_A_DATA_P<1>
- LVDS_CONN_A_DATA_N<1>
- LVDS_CONN_A_DATA_P<2>
- LVDS_CONN_A_DATA_N<2>
- LVDS_CONN_A_CLK_F_P
- LVDS_CONN_A_CLK_F_N
- LVDS_CONN_B_DATA_P<0>
- LVDS_CONN_B_DATA_N<0>
- LVDS_CONN_B_DATA_P<1>
- LVDS_CONN_B_DATA_N<1>
- LVDS_CONN_B_DATA_P<2>
- LVDS_CONN_B_DATA_N<2>
- LVDS_CONN_B_CLK_F_P
- LVDS_CONN_B_CLK_F_N
- LED_RETURN_1
- LED_RETURN_2
- LED_RETURN_3
- LED_RETURN_4
- LED_RETURN_5
- LED_RETURN_6
- GND

2 TP needed

4 TPs

J4500 (SATA ODD CONN)
- PP5V_SW_ODD
- SMC_ODD_DETECT
- SATA_ODD_D2R_C_P
- SATA_ODD_D2R_C_N
- SATA_ODD_R2D_P
- SATA_ODD_R2D_N
- GND

3 TPs

5 TPs

J4501 (SATA HDD CONN)
- PP5V_S0_HDD_FLT
- SATA_HDD_R2D_P
- SATA_HDD_R2D_N
- SATA_HDD_D2R_C_N
- SATA_HDD_D2R_C_P
- GND

J5815 (KBD BACKLIGHT CONN)
- KBDLED_ANODE
- SMC_KBDLED_PRESENT_L
- GND

FUNC_TEST
- GND
- GND

6 TPs

USB PORTS
- PP5V_S3_RTUSB_A_F
- USB2_LT1_N
- USB2_LT1_P
- GND
- PP5V_S3_RTUSB_B_F
- USB_LT2_N
- USB_LT2_P
- GND
- PP5V_S3_RTUSB_C_F
- USB_LT3_N
- USB_LT3_P
- GND

J3401 (AIRPORT/BT/CAMERA CONN)
- PCIE_MINI_D2R_P
- PCIE_MINI_D2R_N
- PCIE_MINI_R2D_P
- PCIE_MINI_R2D_N
- PCIE_CLK100M_MINI_CONN_P
- PCIE_CLK100M_MINI_CONN_N
- MINI_CLKREQ_Q_L
- PCIE_WAKE_L
- MINI_RESET_CONN_L
- PP5V_WLAN
- PP5V_S3_BTCAMERA_F
- SMBUS_SMC_A_S3_SDA
- SMBUS_SMC_A_S3_SCL
- USB_CAMERA_CONN_P
- USB_CAMERA_CONN_N
- CONN_USB2_BT_P
- CONN_USB2_BT_N

J3500 (EXPRESS CARD CONN)
- PP1V5_S0_EXCARD_SWITCH
- PCIE_WAKE_L
- SMBUS_MCP_0_CLK
- SMBUS_MCP_0_DATA
- PP3V3_S0_EXCARD_SWITCH
- PP3V3_S3_EXCARD_SWITCH
- USB2_EXCARD_CONN_N
- USB2_EXCARD_CONN_P
- EXCARD_CPUSB_L
- EXCARD_CLKREQ_CONN_L
- EXCARD_CPPE_L
- PLT_RESET_SWITCH_L
- PCIE_EXCARD_D2R_P
- PCIE_EXCARD_D2R_N
- PCIE_EXCARD_R2D_P
- PCIE_EXCARD_R2D_N
- PCIE_CLK100M_EXCARD_CONN_P
- PCIE_CLK100M_EXCARD_CONN_N

J5800 (IPD FLEX CONN)
- PP3V3_S3_LDO
- PP18V5_S3
- TPAD_GND_F
- Z2_CS_L
- Z2_DEBUG3
- Z2_MISO
- Z2_MOSI
- Z2_BOOST_EN
- Z2_BOOT_CFG1
- Z2_CLKIN
- Z2_KEY_ACT_L
- Z2_RESET
- PSOC_F_CS_L
- PICKB_L
- PSOC_MISO
- PSOC_MOSI
- PSOC_SCLK
- SMBUS_SMC_A_S3_SCL
- SMBUS_SMC_A_S3_SDA

J6900 (DC POWER CONN)
- ADAPTER_SENSE
- PP18V5_DCIN_FUSE
- GND

J6950 (MAIN BATT CONN)
- PPVBAT_G3H_CONN_F
- SMBUS_SMC_BSA_SCL
- SMBUS_SMC_BSA_SDA
- SMC_BS_ALRT_L
- GND

J6995 (BAT LED CONN)
- PP3V42_G3H
- SMBUS_SMC_BSA_SDA
- SMBUS_SMC_BSA_SCL
- SMC_BIL_BUTTON_DB_L
- GND

J5713 (KEY BOARD CONN)
- PP3V3_S3
- PP3V42_G3H
- WS_KBD1
- WS_KBD2
- WS_KBD3
- WS_KBD4
- WS_KBD5
- WS_KBD6
- WS_KBD7
- WS_KBD8
- WS_KBD9
- WS_KBD10
- WS_KBD11
- WS_KBD12
- WS_KBD13
- WS_KBD14
- WS_KBD15_CAP
- WS_KBD16_NUM
- WS_KBD17
- WS_KBD18
- WS_KBD19
- WS_KBD20
- WS_KBD21
- WS_KBD22
- WS_KBD23
- WS_KBD_ONOFF_L
- WS_LEFT_SHIFT_KBD
- WS_LEFT_OPTION_KBD
- WS_CONTROL_KBD

J4800 (FRONT CABLE CONN)
- PP3V42_G3H_LIDSWITCH_R
- PP5V_S3_IR_R
- SMC_LID_R
- IR_RX_OUT
- SYS_LED_ANODE
- GND

J5502 (SENSOR CONN)
- MCPTHMSNS_D_P
- MCPTHMSNS_D_N

POWER RAILS
FUNC_TEST
- PM_SLP_S3_L
- PPBUS_G3H
- PPBUS_CPU_IMVP_ISNS
- PP3V42_G3H
- PP5V_S3
- PP5V_S0
- PPVCORE_S0_CPU
- PPVCORE_S0_MCP
- PP3V3_S5
- PP3V3_S3
- PP3V3_S0
- PP2V5_S0
- PP1V2_S0
- PP1V8_S0
- PP1V8R1V5_S3
- PP1V8R1V5_S0
- PPMCPDDR_ISNS
- PP1V05_S0
- PP1V2R1V05_S5
- PPCPUVTT_S0
- PP0V9R0V75_S0_DDRVTT
- PP1V2R1V05_ENET
- PP3V3_ENET_PHY
- PPVP_FW
- PP1V0_FW
- PP3V3_S0GPU
- PP1V1_S0GPU
- PP1V8_S0GPU_ISNS
- PPVCORE_GPU
- PP1V8_S0GPU_ISNS_R
- PP3V3_S5_AVREF_SMC
- PP18V5_S3
- PPDCIN_G3H
- PPVCORE_S0_MCP
- PPMCPDDR_ISNS
- PPVTTDDR_S3
- PP1V8_GPUIFPX

FUNC_TEST
- SYS_LED_ANODE_R
- LPC_CLK33M_LPCPLUS
- LPC_AD<0..3>
- SPI_ALT_MOSI
- SPI_ALT_MISO
- LPC_FRAME_L
- PM_CLKRUN_L
- SMC_TMS
- DEBUG_RESET_L
- SMC_TDO
- SMC_TRST_L
- SMC_MD1
- SMC_TX_L
- SPIROM_USE_MLB
- SPI_ALT_CLK
- SPI_ALT_CS_L
- LPC_SERIRQ
- LPC_PWRDWN_L
- SMC_TDI
- SMC_TCK
- SMC_RESET_L
- SMC_NMI
- SMC_RX_L
- LPCPLUS_GPIO
- ISSP_SCLK_P1_1
- ISSP_SDATA_P1_0
- SMC_ONOFF_L
- PM_SYSRST_L
- BKL_FB
- BKL_GD
- BKL_SW
- BKLT_EN
- BKL_SCL
- BKL_SDA
- LCD_BKLT_PWM

ICT Test Points

CPU FSB NO_TESTS
NO_TEST
- FSB_A_L<31..3>
- FSB_ADS_L
- FSB_ADSTB_L<1..0>
- FSB_D_L<63..0>
- FSB_DBSY_L
- FSB_DINV_L<3..0>
- FSB_DRDY_L
- FSB_DSTB_L_N<3..0>
- FSB_DSTB_L_P<3..0>
- FSB_HIT_L
- FSB_HITM_L
- FSB_LOCK_L
- FSB_REQ_L<4..0>

FB NO_TESTS
NO_TEST
- FB_A_DQ<63..0>
- FB_B_DQ<63..0>
- FB_B_BA<1>
- FB_B_CAS_L
- FB_B_CS0_L
- FB_B_MA<11>

LVDS NO_TESTS
NO_TEST
- LVDS_A_DATA_N<0>
- LVDS_A_DATA_P<0>
- LVDS_B_CLK_P
- LVDS_B_DATA_N<0>
- LVDS_B_DATA_P<0>
- LVDS_EG_A_DATA_N<2>

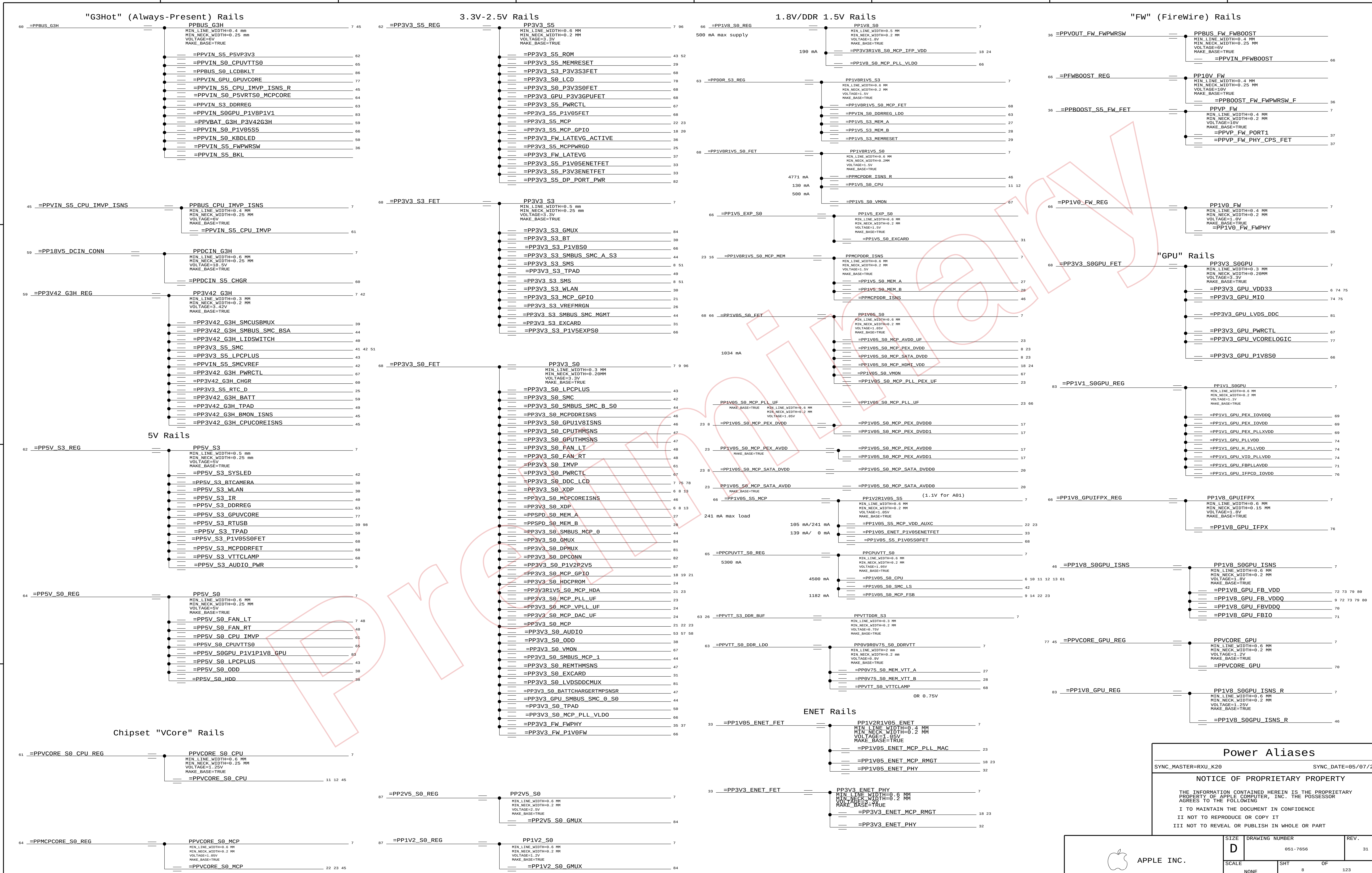
NC NO_TESTS
NO_TEST
- NC_PCI_AD<31..8>
- NC_PCI_C_BE_L<3..0>
- NC_PCI_CLK0
- NC_PCI_CLK1
- NC_PCI_DEVSEL_L
- NC_PCI_FRAME_L
- NC_PCI_GNT0_L
- NC_PCI_GNT1_L
- NC_PCI_INTW_L
- NC_PCI_INTX_L
- NC_PCI_INTY_L
- NC_PCI_INTZ_L
- NC_PCI_IRDY_L
- NC_PCI_PAR
- NC_PCI_PERR_L
- NC_PCI_RESET1_L
- NC_PCI_SERR_L
- NC_PCI_STOP_L
- NC_PCI_TRDY_L
- NC_PCIE_CLK100M_PE4P
- NC_PCIE_CLK100M_PE5N
- NC_PCIE_CLK100M_PE5P
- NC_PCIE_CLK100M_PE6N
- NC_PCIE_CLK100M_PE6P
- NC_PCIE_PE4_D2RN
- NC_PCIE_PE4_D2RP
- NC_PE4_CLKREQ_L
- NC_PEX_CLKREQ_L
- NC_PSOC_P1_3
- NC_SATA_C_D2RN
- NC_SATA_C_D2RP
- NC_SATA_C_R2D_CN
- NC_SATA_C_R2D_CP
- NC_SATA_D_D2RN
- NC_SATA_D_D2RP
- NC_SATA_D_R2D_CN
- NC_SATA_D_R2D_CP
- NC_SATA_E_D2RN
- NC_SATA_E_D2RP
- NC_SATA_E_R2D_CN
- NC_SATA_E_R2D_CP
- NC_SATA_F_D2RN
- NC_SATA_F_D2RP
- NC_SATA_F_R2D_CN
- NC_SATA_F_R2D_CP
- NC_SB_A20GATE
- NC_SMC_P41
- NC_USB_10P
- NC_USB_11N
- NC_USB_11P
- NC_USB_EXTDN
- NC_USB_EXTDP
- NC_USB_MININ
- NC_USB_MINIP
- NC_XDP_OBSDATA_B2
- NC_XDP_OBSDATA_B3

(Each connected from TP_ net of same name, e.g. TP_PCI_AD<31..8>, via MAKE_BASE=TRUE)

NC NO_TESTS
NO_TEST
- NC_SMC_FAN_3_TACH
- NC_SMC_FAN_3_CTL
- NC_SMC_FAN_2_TACH
- NC_SMC_FAN_2_CTL
- NC_FW2_TPBP
- NC_FW2_TPBN
- NC_FW2_TPBIAS
- NC_FW2_TPAP
- NC_FW2_TPAN
- NC_FW0_TPBP
- NC_FW0_TPBN
- NC_FW0_TPAP
- NC_ESTARLDO_EN
- NC_ALS_GAIN

NC NO_TESTS
NO_TEST
- NC_CPU_PECI_MCP
- NC_CPU_TEST3
- NC_ENET_INTR_L
- NC_ENET_PWRDWN_L
- NC_FW643_AVREG
- NC_FW643_TDI
- NC_MEM_A_A<15>
- NC_MEM_A_CKE<2>
- NC_MEM_A_CKE<3>
- NC_MEM_A_CLK2N
- NC_MEM_A_CLK2P
- NC_MEM_A_CLK3N
- NC_MEM_A_CLK3P
- NC_MEM_A_CLK4N
- NC_MEM_A_CLK4P
- NC_MEM_A_CLK5N
- NC_MEM_A_CLK5P
- NC_MEM_A_CS_L<2>
- NC_MEM_A_CS_L<3>
- NC_MEM_A_ODT<2>
- NC_MEM_A_ODT<3>
- NC_MEM_B_A<15>
- NC_MEM_B_CKE<2>
- NC_MEM_B_CLK2P
- NC_MEM_B_CLK3N
- NC_MEM_B_CLK3P
- NC_MEM_B_CLK4N
- NC_MEM_B_CLK4P
- NC_MEM_B_CLK5N
- NC_MEM_B_CLK5P
- NC_MEM_B_CS_L<2>
- NC_MEM_B_CS_L<3>
- NC_MEM_B_ODT<2>
- NC_MEM_B_ODT<3>
- NC_MLB_RAM_SIZE
- NC_MLB_RAM_VENDOR
- NC_GPU_BUFRST_L
- NC_GPU_GSTATE<0>
- NC_GPU_GSTATE<1>
- NC_GPU_MIOA_D<9..0>
- NC_GPU_MIOA_DE
- NC_GPU_PGOOD_OUT_L
- NC_GPU_VCORE_VID3
- NC_LPC_DRQ0_L
- NC_LVDS_EG_B_CLK_N
- NC_LVDS_EG_B_CLK_P
- NC_LVDS_EG_BKL_PWM
- NC_LVDS_IG_B_CLKN
- NC_LVDS_IG_B_CLKP
- NC_LVDS_IG_BKL_PWM
- NC_MCP_BUF_SIO_CLK
- NC_MCP_GPIO_18
- NC_MCP_KBDRSTIN_L
- NC_MCP_SATALED_L

(Each connected from TP_ net of same name, e.g. TP_CPU_PECI_MCP, via MAKE_BASE=TRUE)

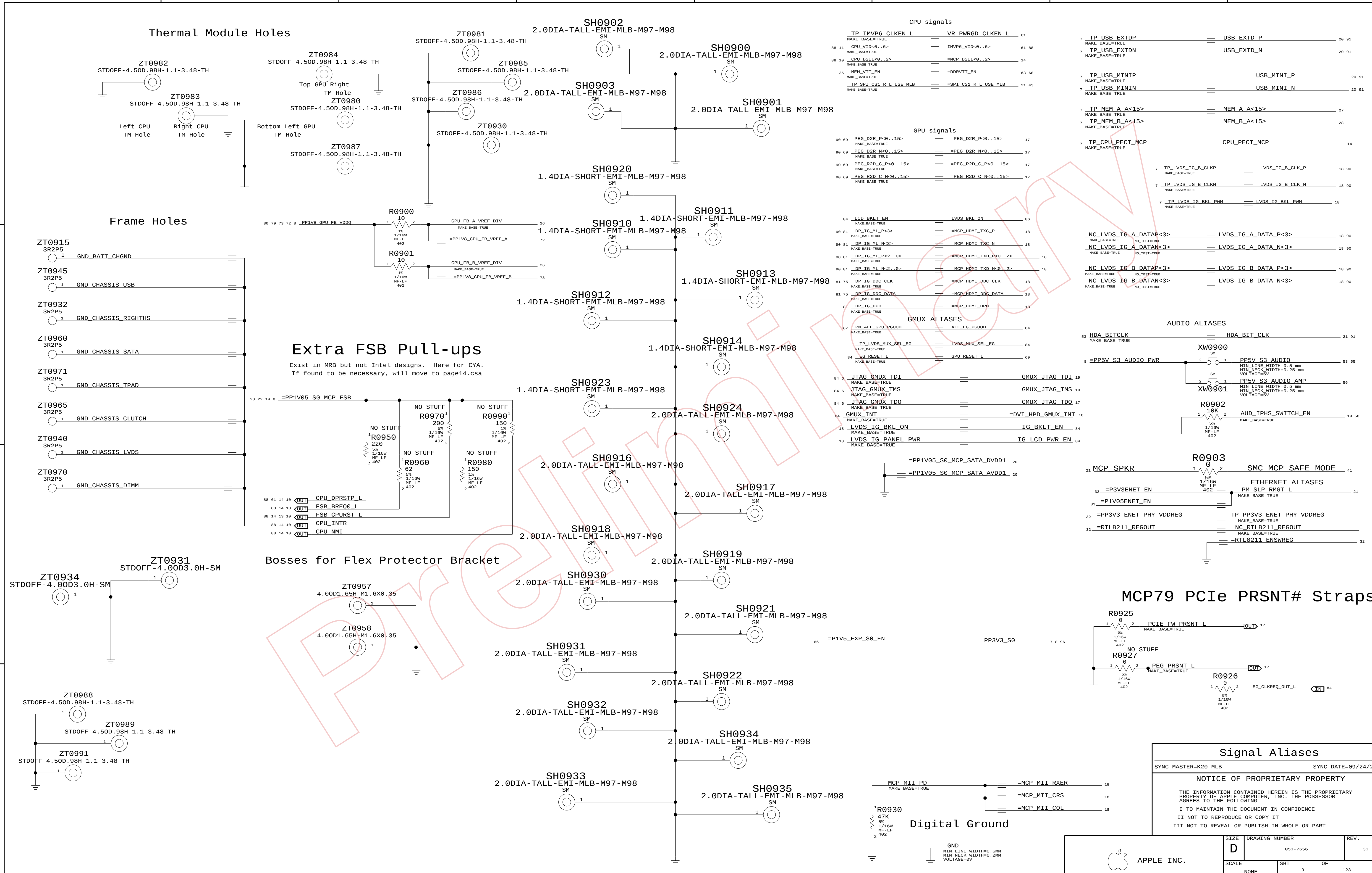


Power Aliases

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 8	OF 123



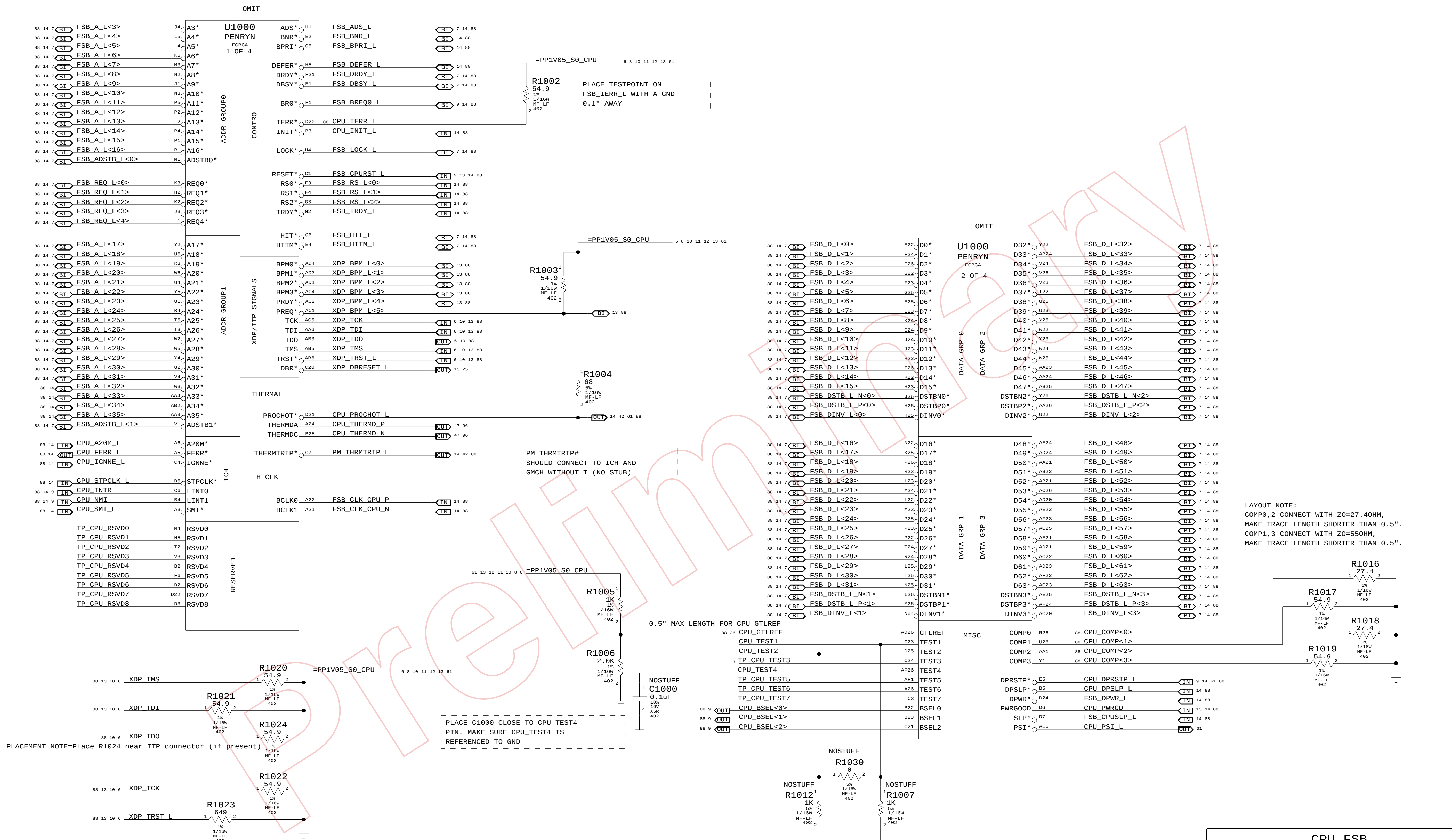
Signal Aliases

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	9	123



CPU FSB

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 10	OF 123

(CPU CORE POWER)

=PPVCORE_S0_CPU 8 11 12 45

Standard Voltage:

44.0 A (Design Target)

41.0 A (HFM)
30.4 A (LFM)
25.5 A (SuperLFM)

27.4 A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)

27.4 A (Sleep HFM)
16.8 A (Sleep SuperLFM)

25.0 A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)

11.5 A (Deeper Sleep)

9.4 A (Enhanced Deeper Sleep)

Low Voltage:

23.0 A (Design Target)

21.0 A (HFM)
18.7 A (LFM)
TBD A (SuperLFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant SuperLFM)

TBD A (Sleep HFM)
TBD A (Sleep SuperLFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep SuperLFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

17.0 A (Design Target)

TBD A (HFM)
TBD A (LFM)

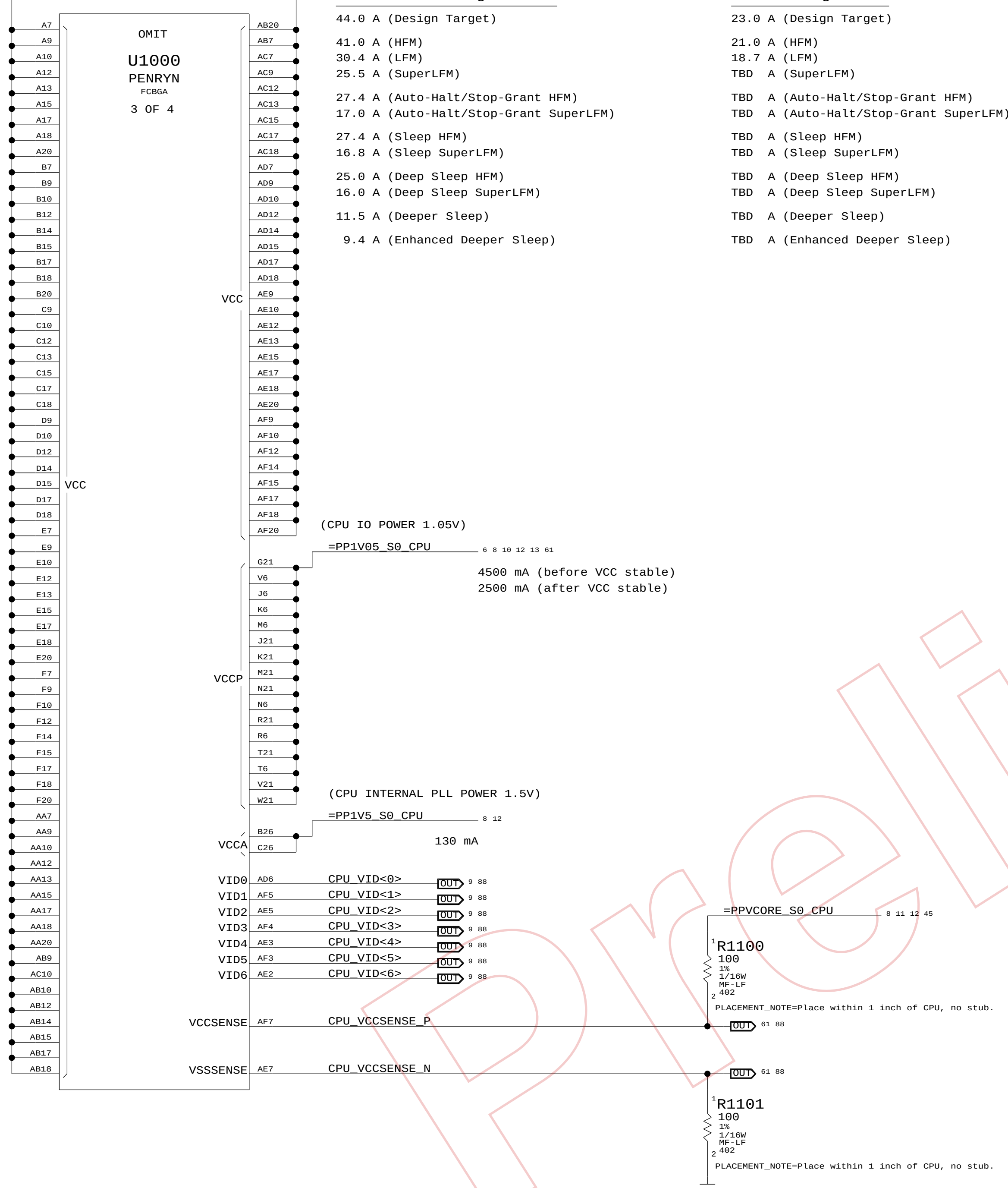
TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant LFM)

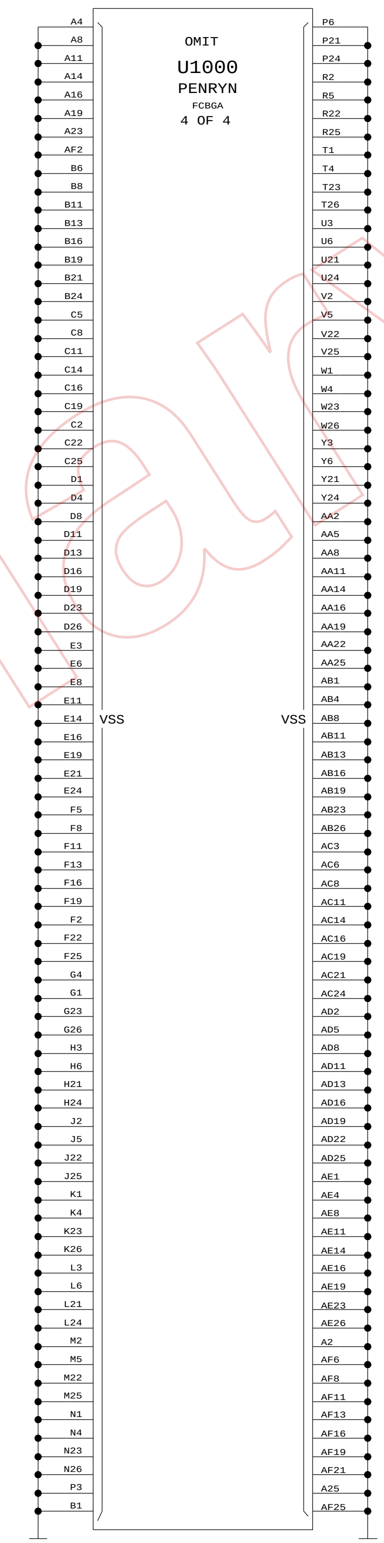
TBD A (Sleep HFM)
TBD A (Sleep LFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep LFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)





Current numbers from Merom for Santa Rosa EMTS, doc #22221.

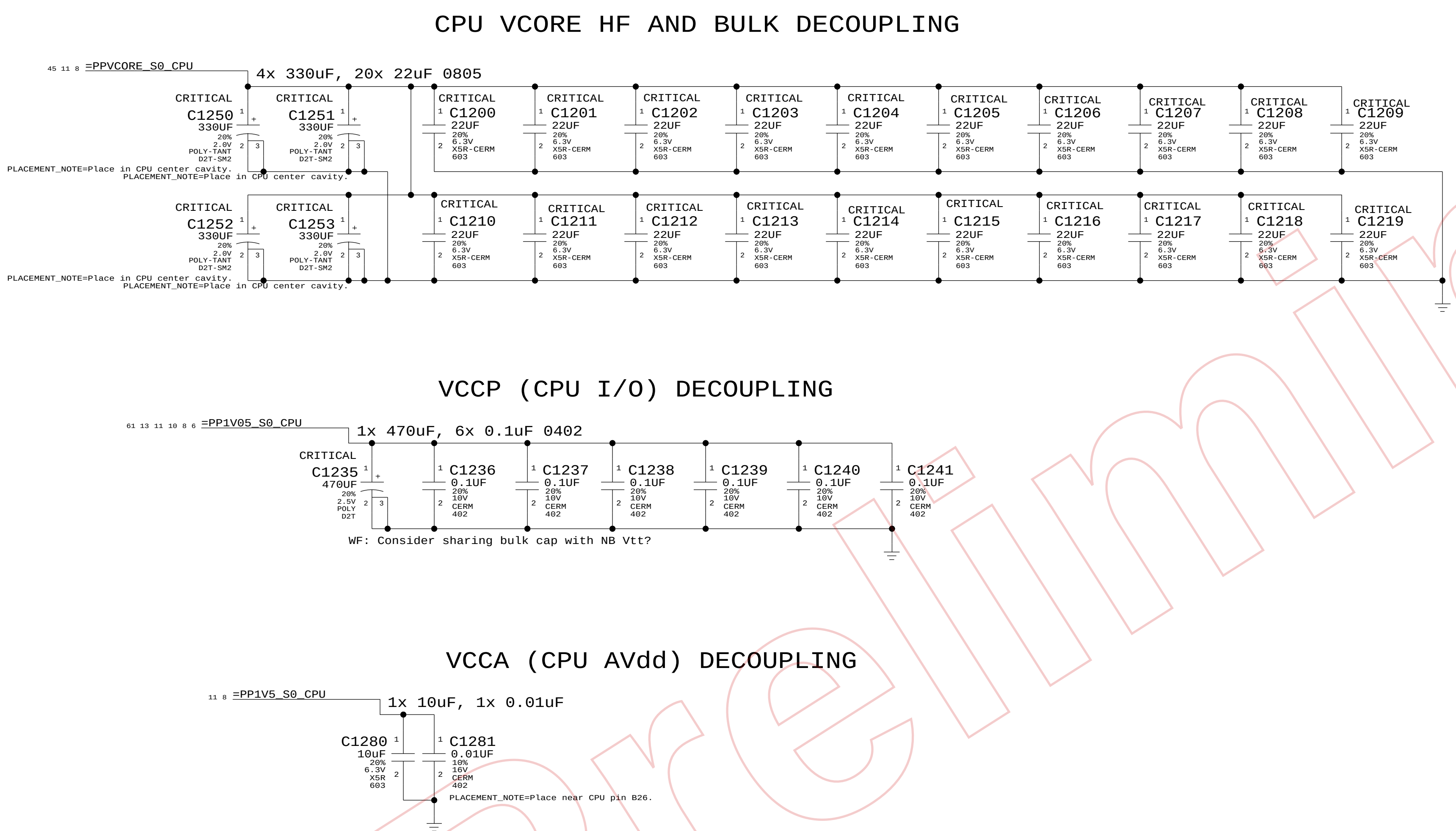
CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	11	123



CPU Decoupling & VID

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

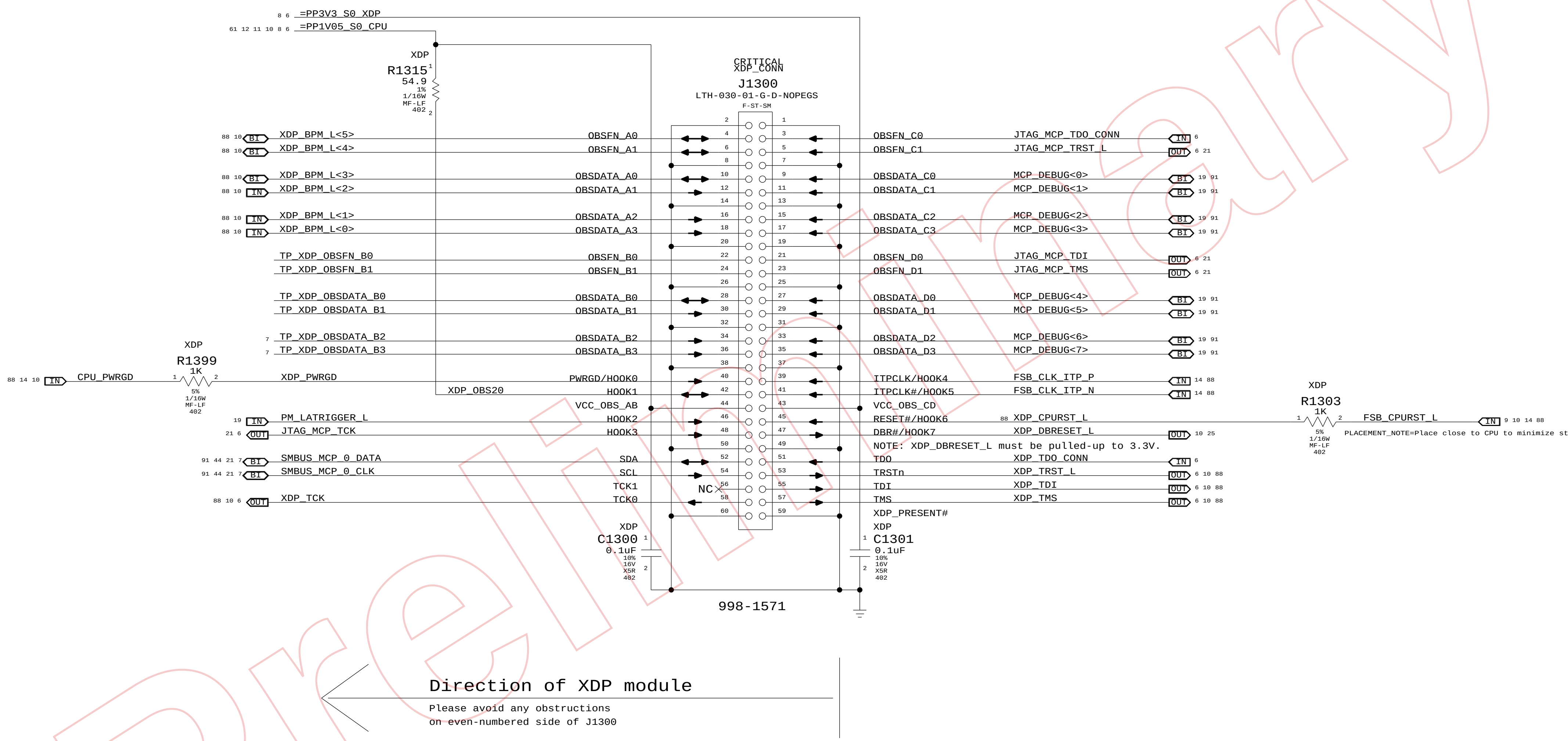
SCALE NONE — SHT 12 OF 123

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

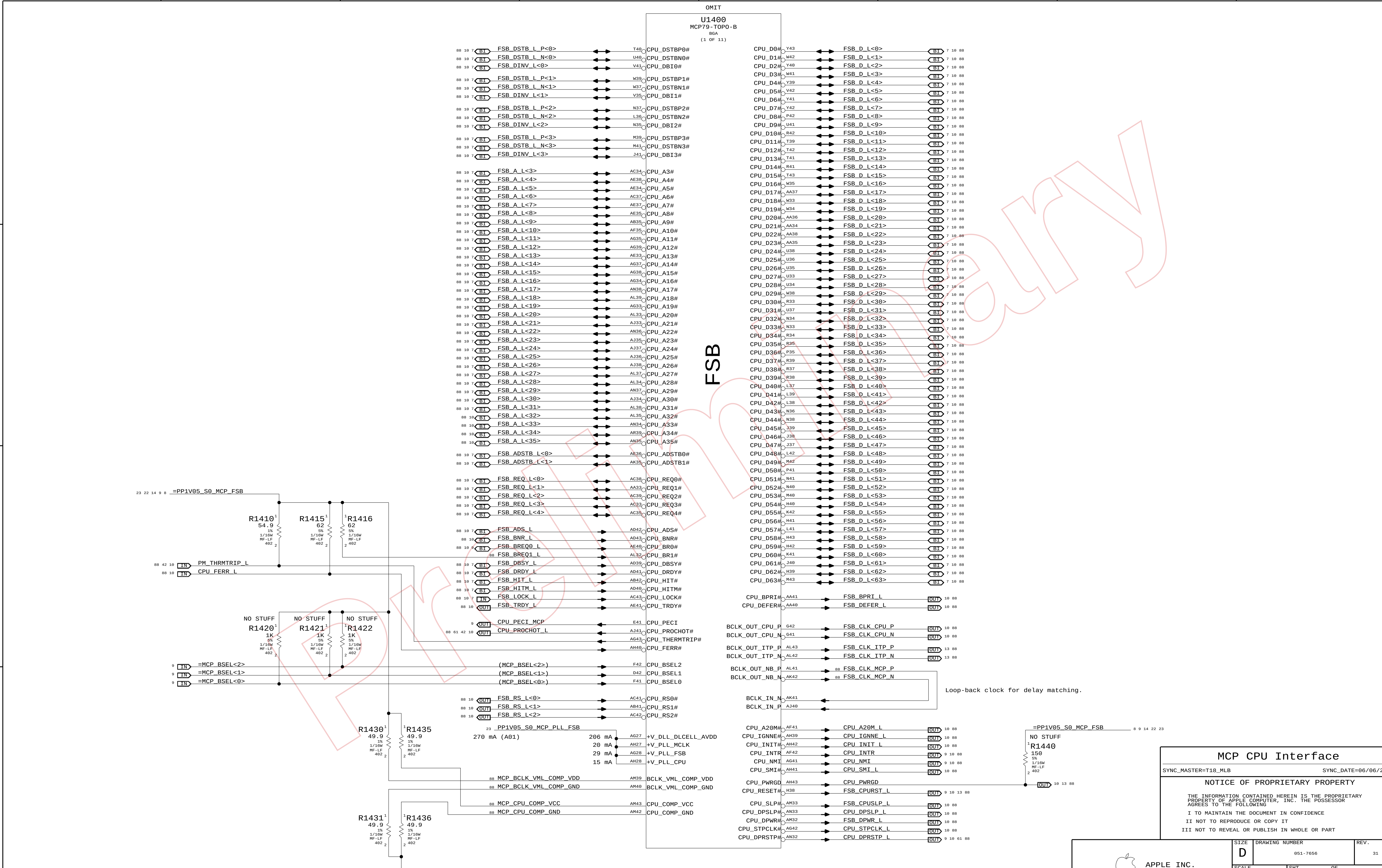


eXtended Debug Port(MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 13	OF 123



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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APPLE INC.

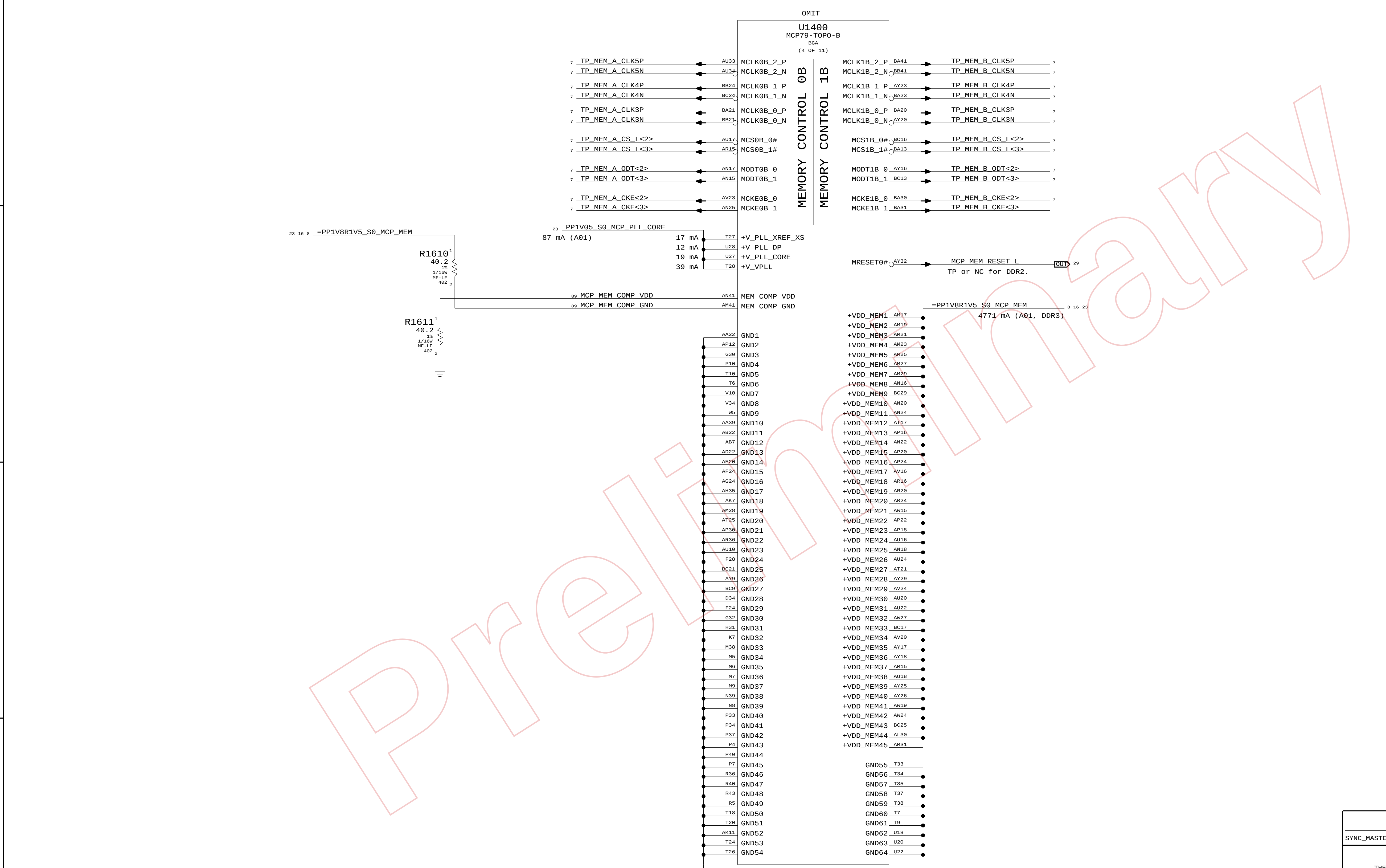
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 14	OF 123

MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 15	OF 123



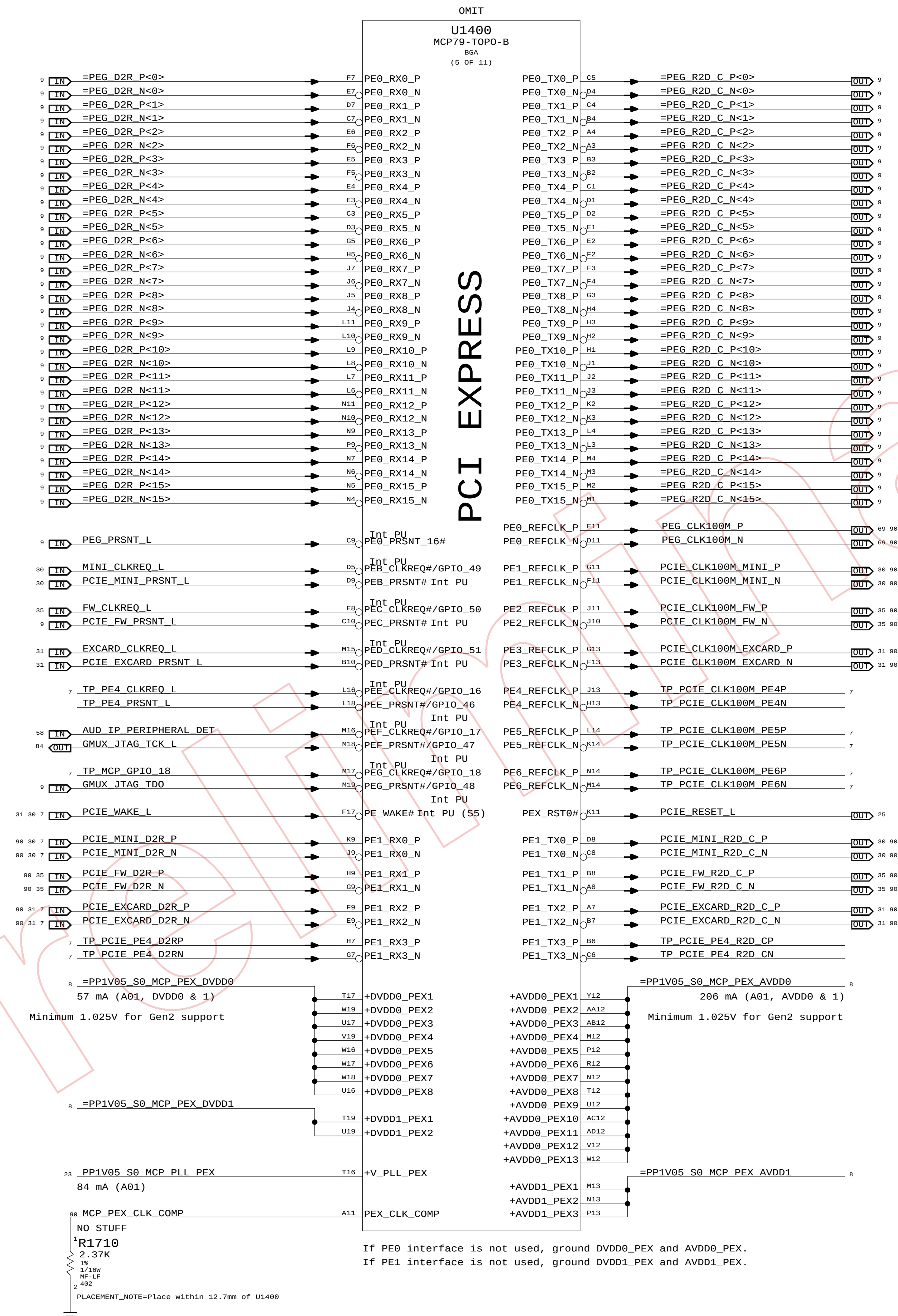
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 16	OF 123



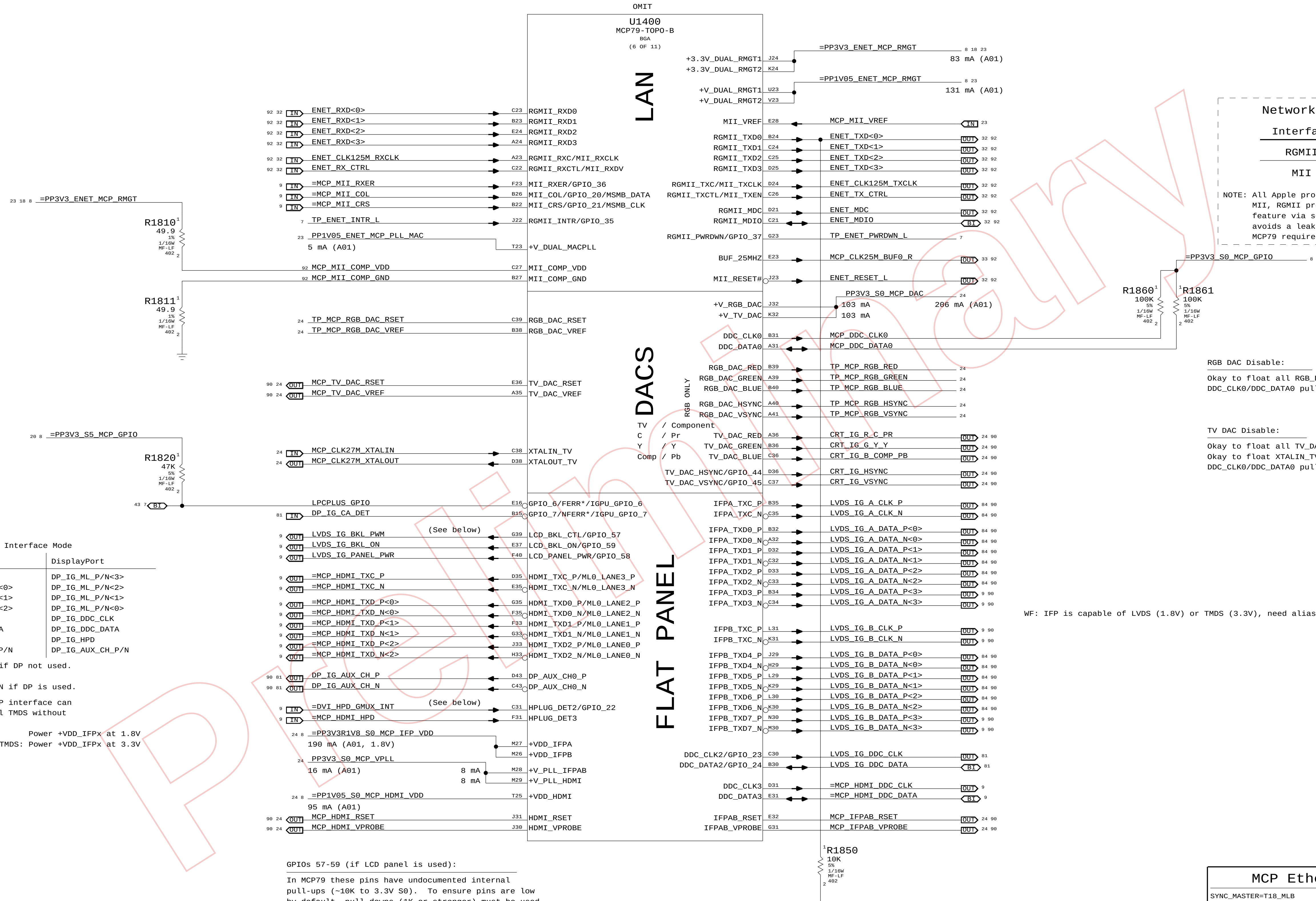
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 17	OF 123



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

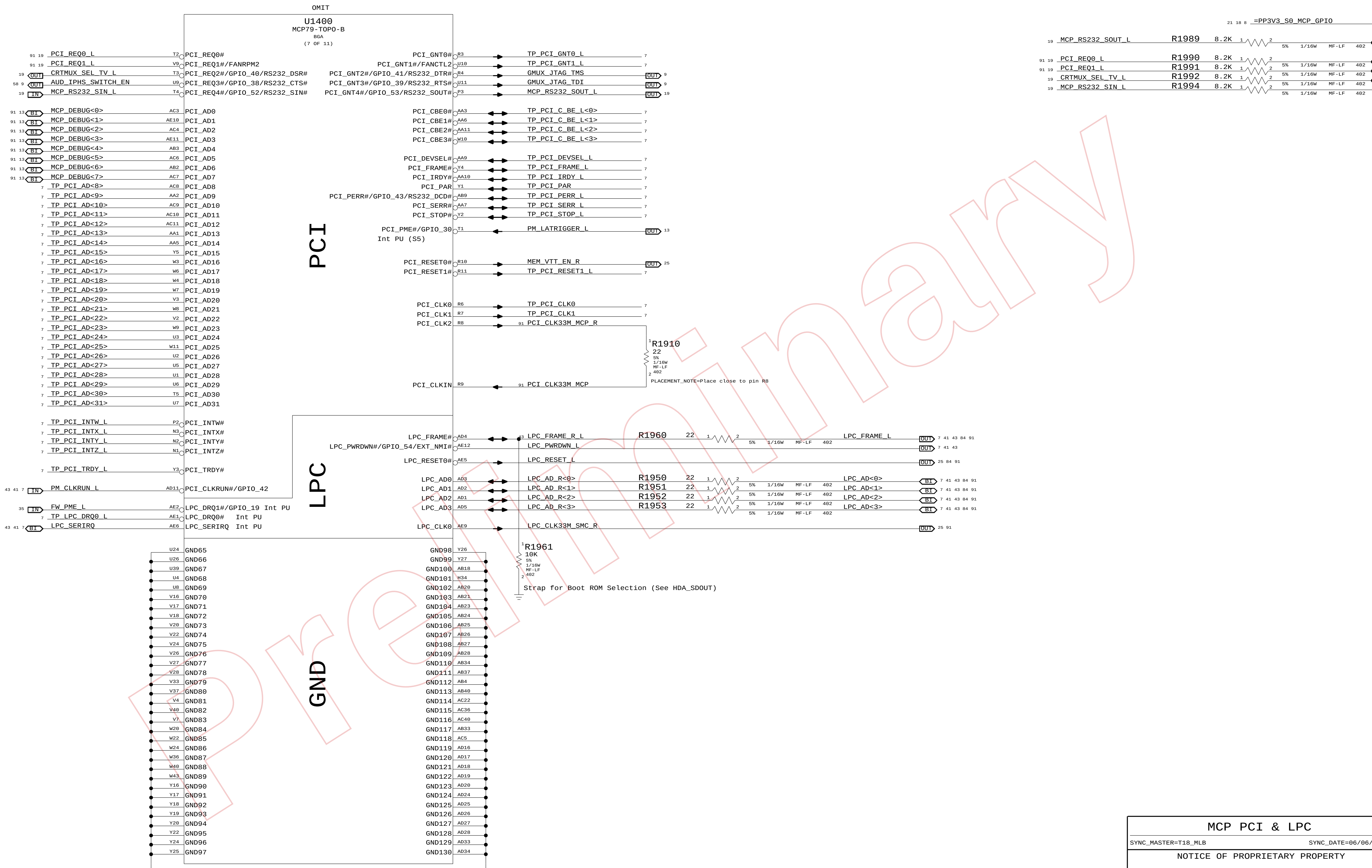
MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 18 OF 123



MCP PCI & LPC

SYNC_MASTER=T18_MLB

SYNC_DATE=06/06/2008

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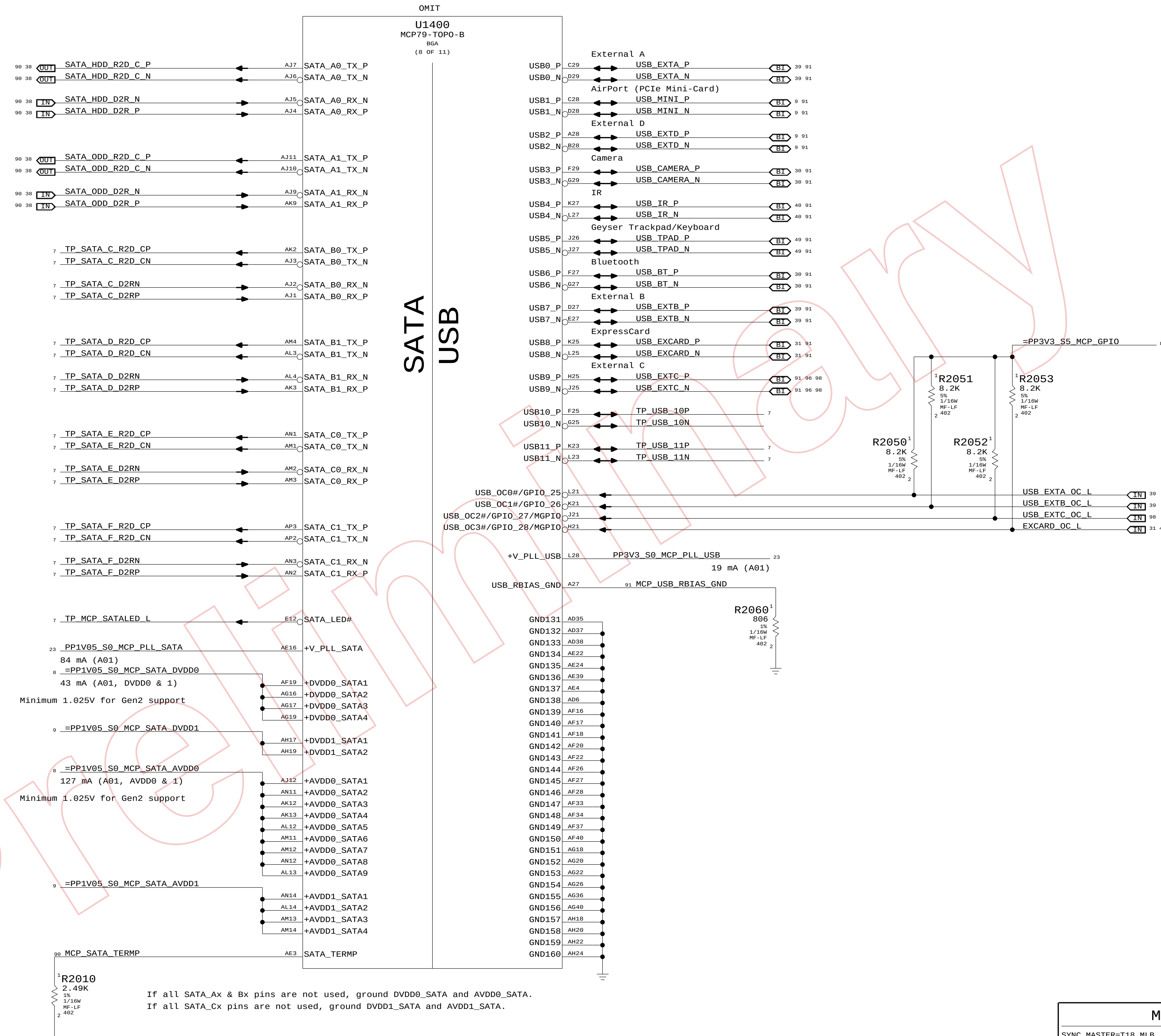
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 19	OF 123



If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

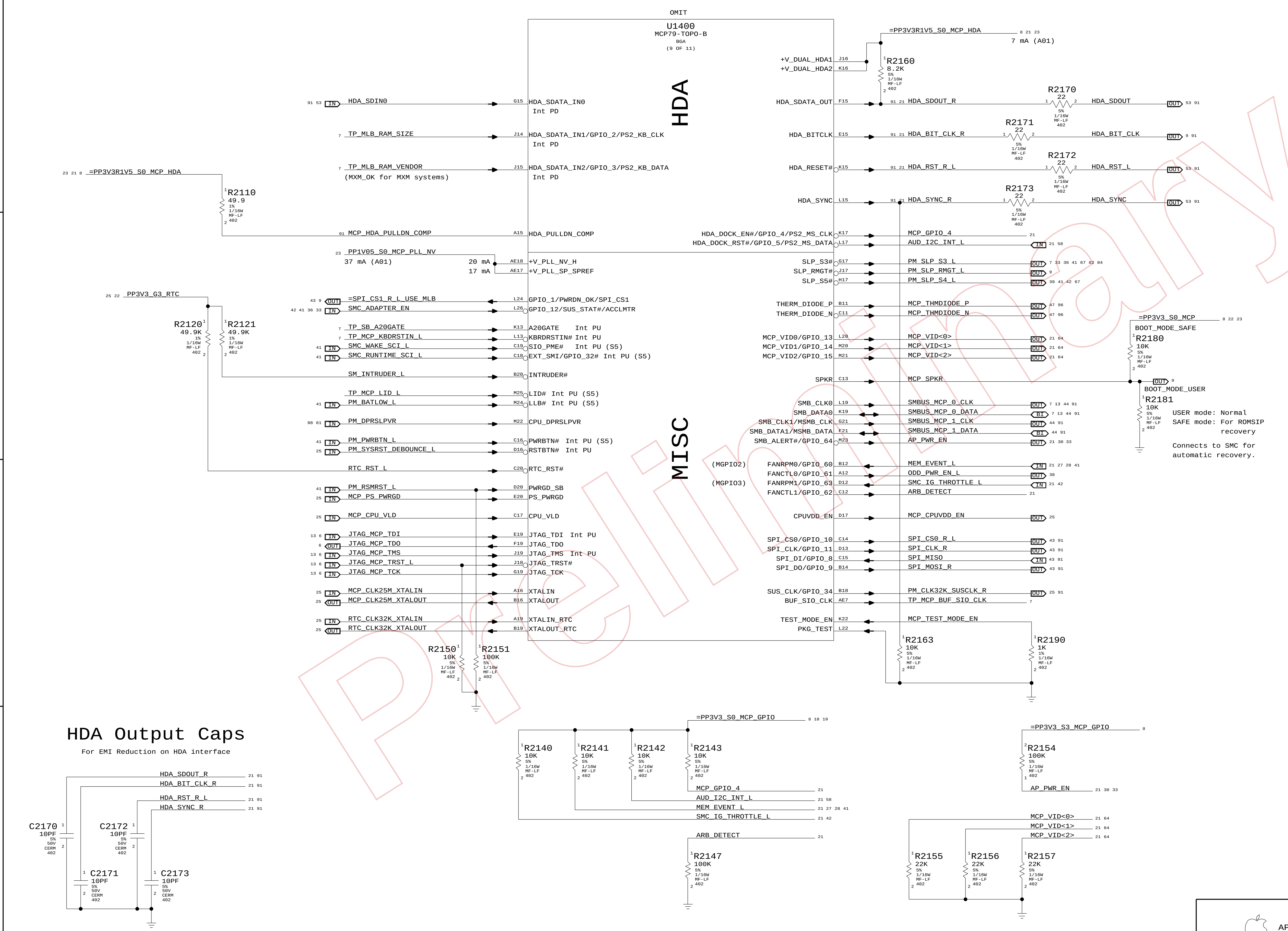
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 20	OF 123



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

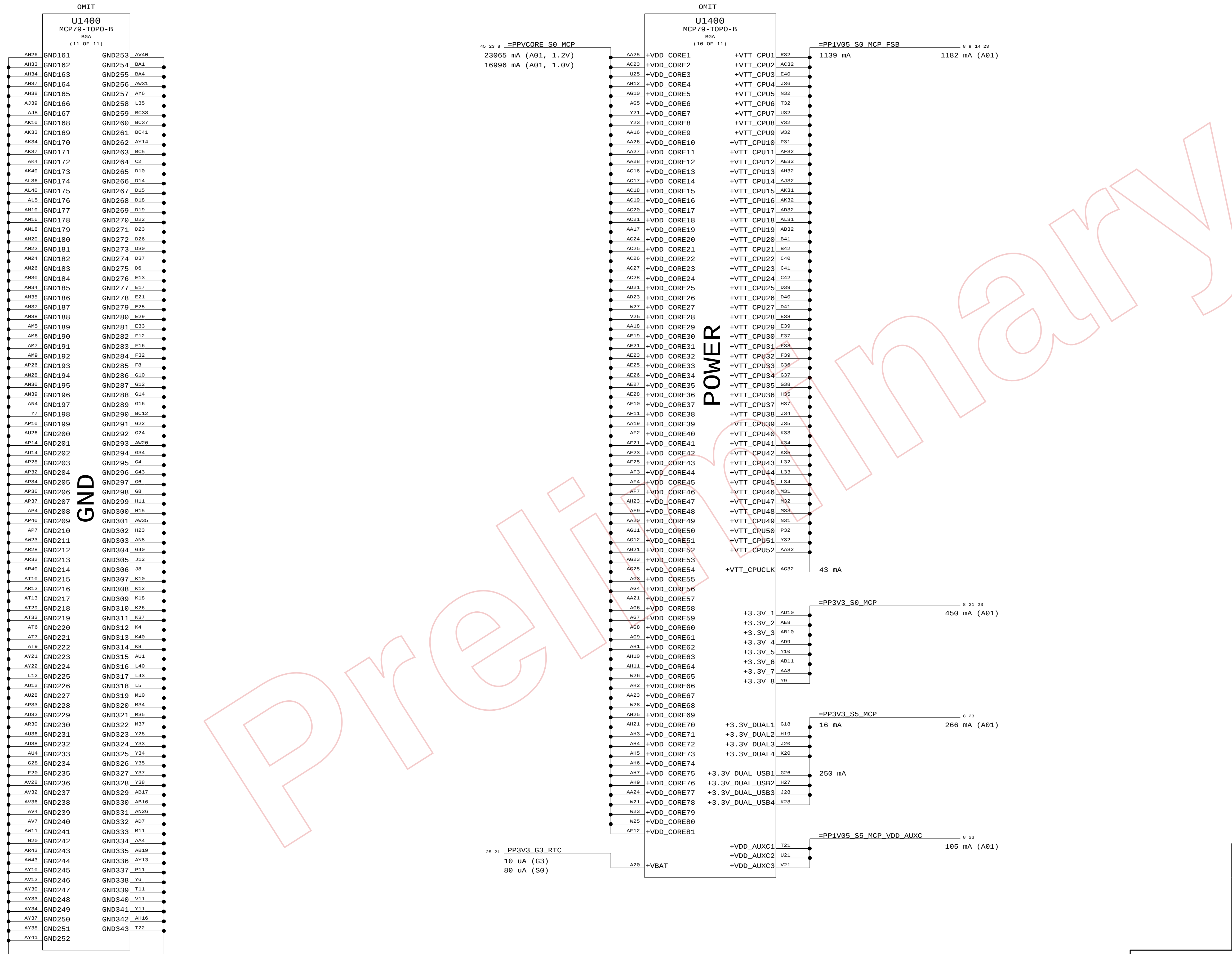
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 21	OF 123



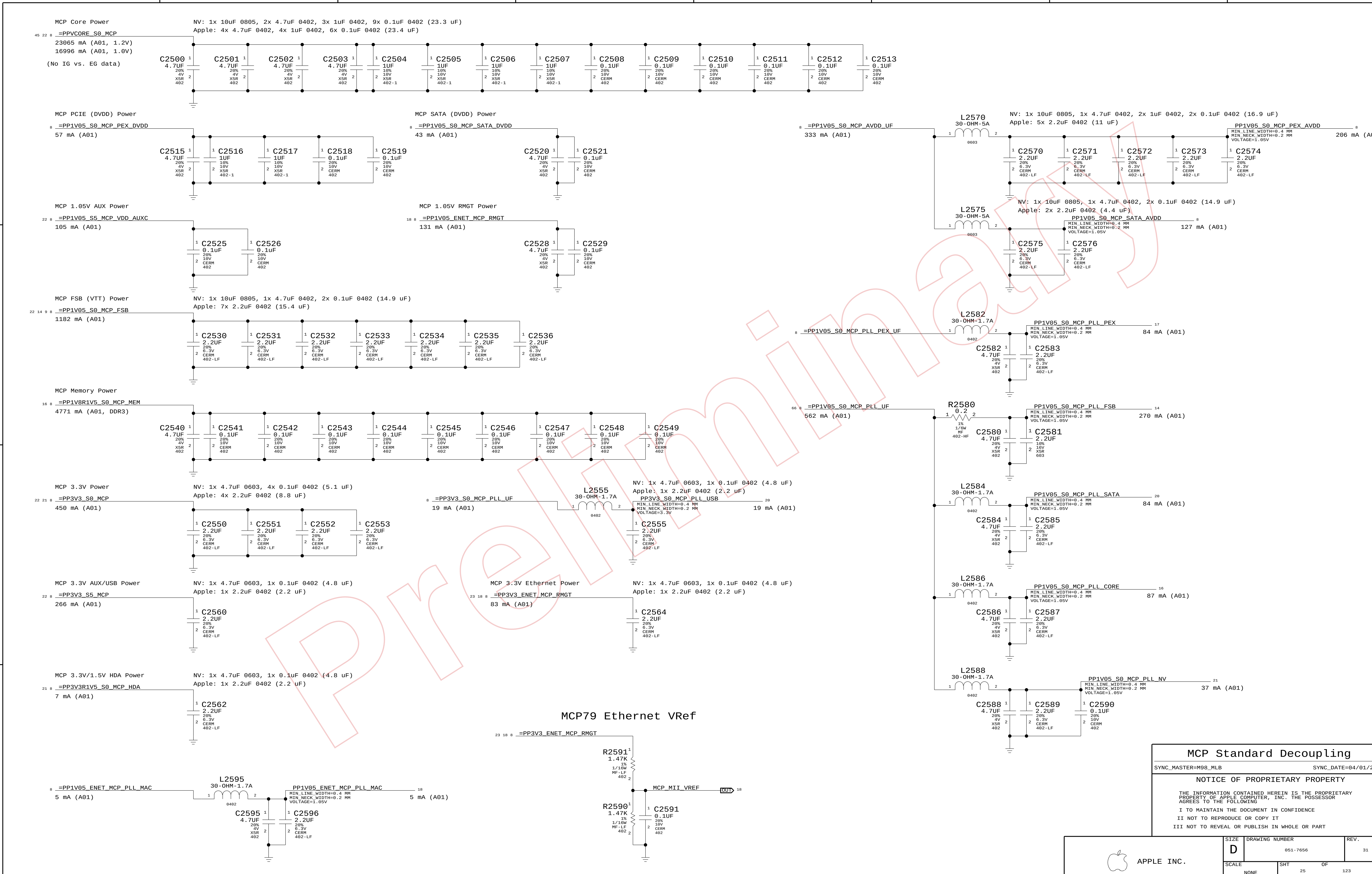
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 22	OF 123

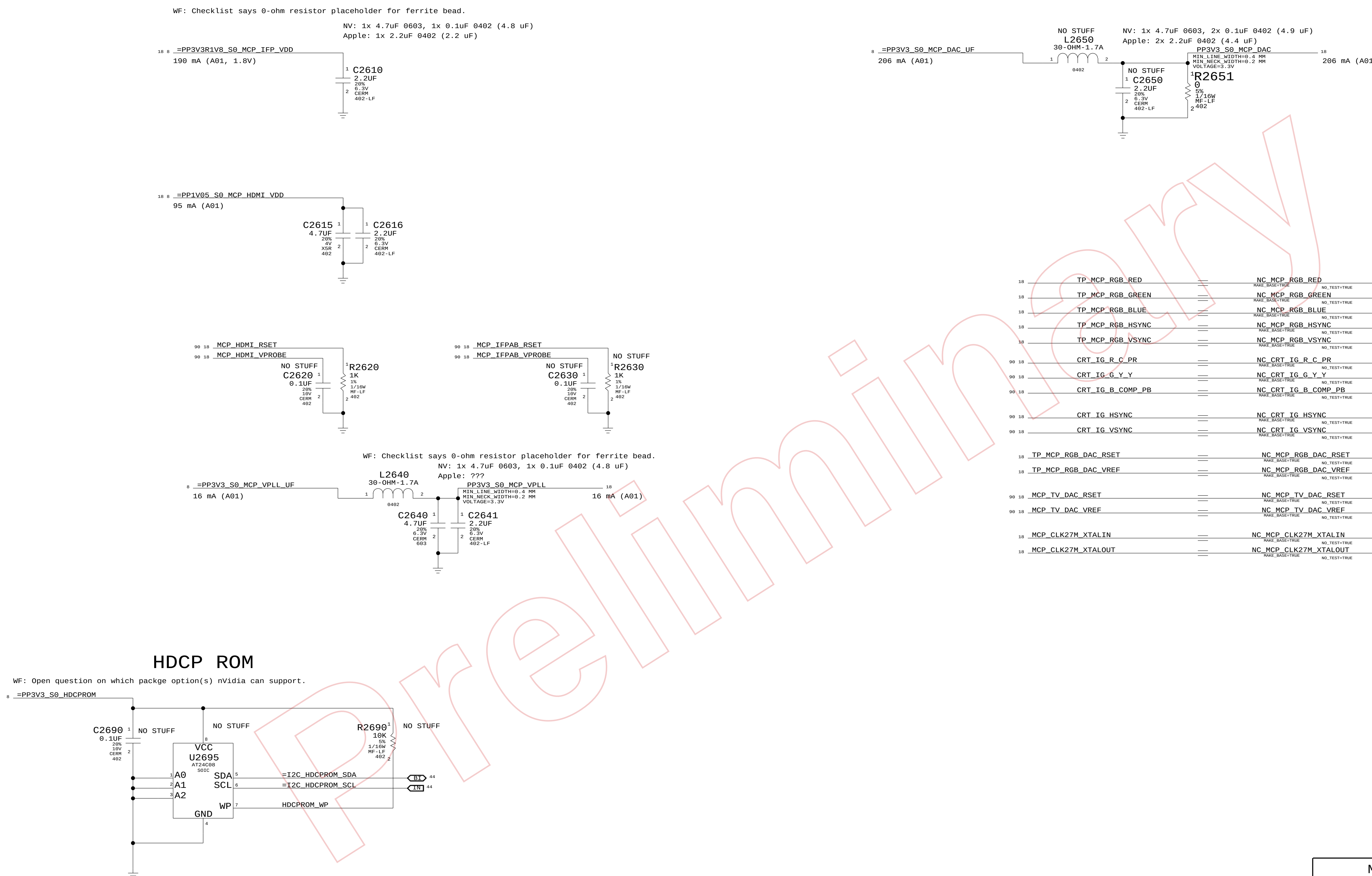


MCP Standard Decoupling

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 25	OF 123



Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

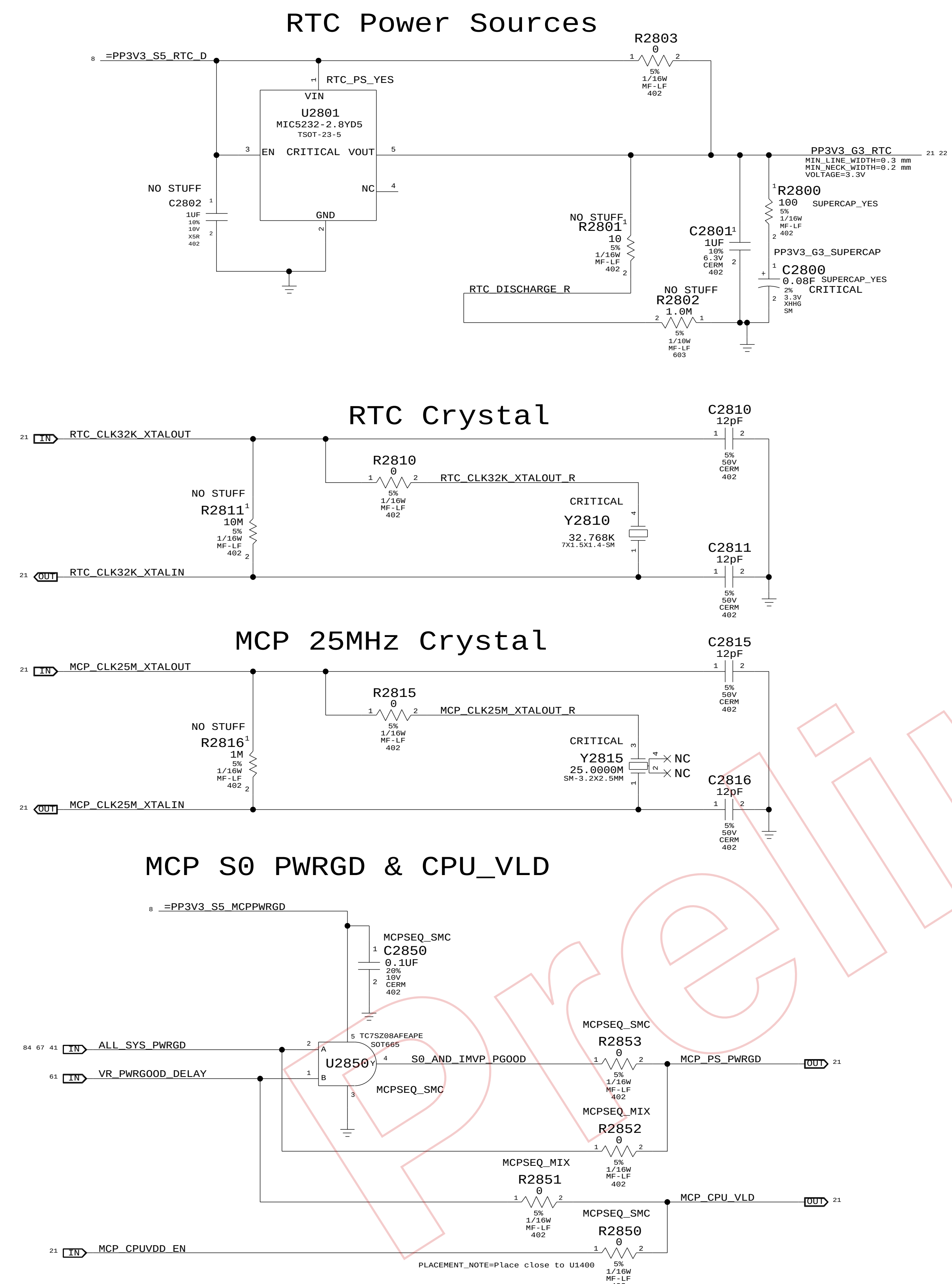
MCP Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	26	123

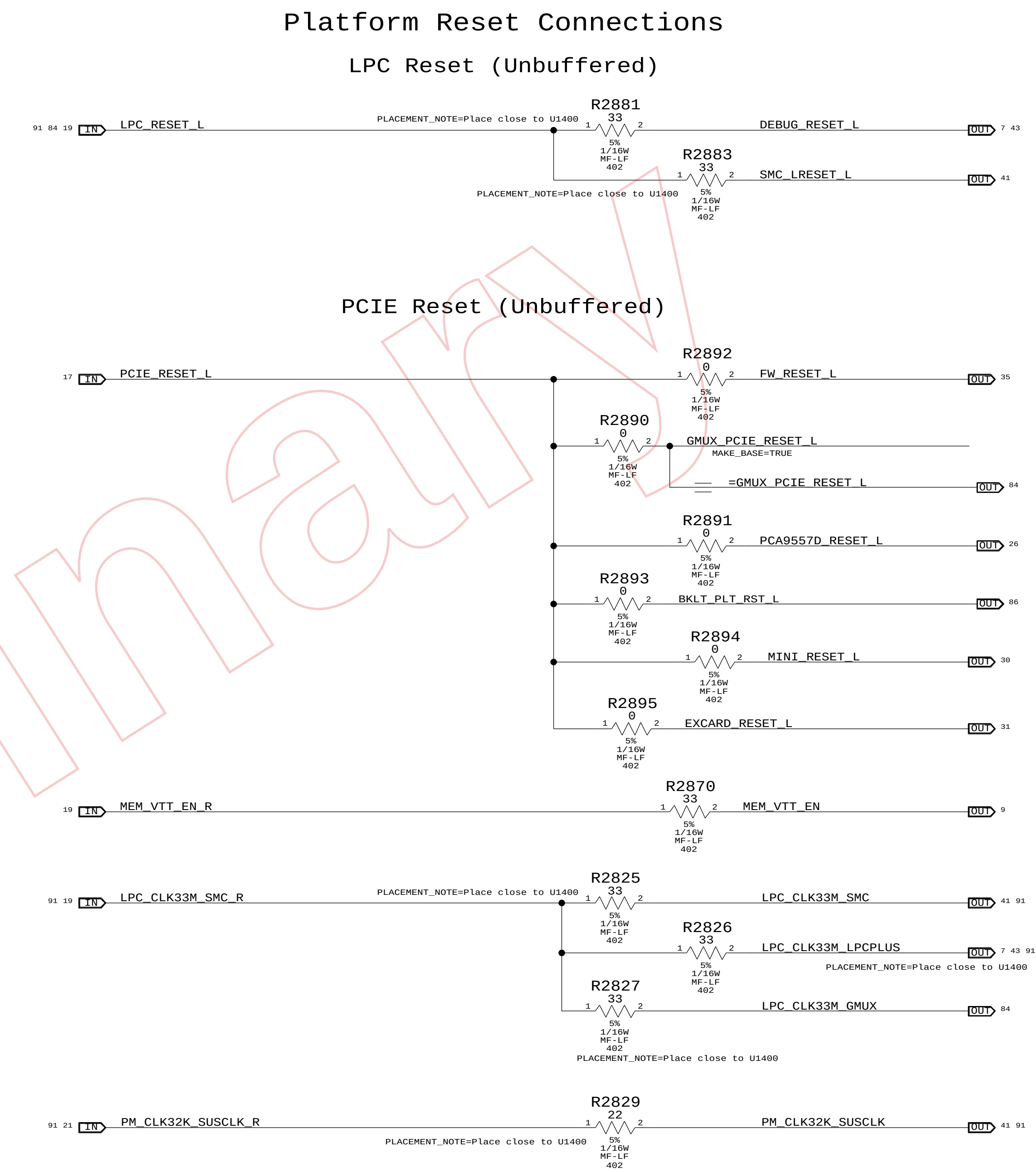


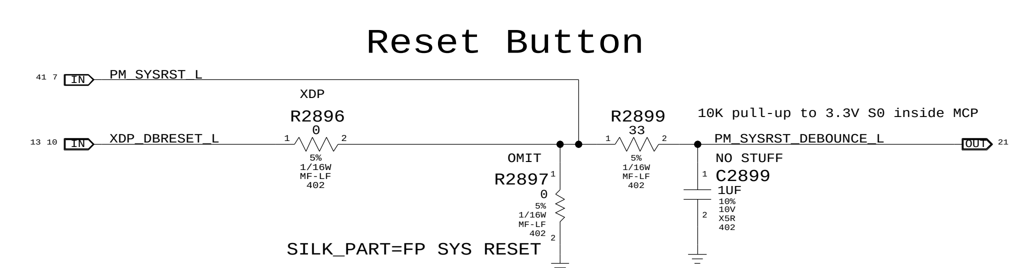
MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.





SB Misc

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 28	OF 123

Preliminary

Page Notes

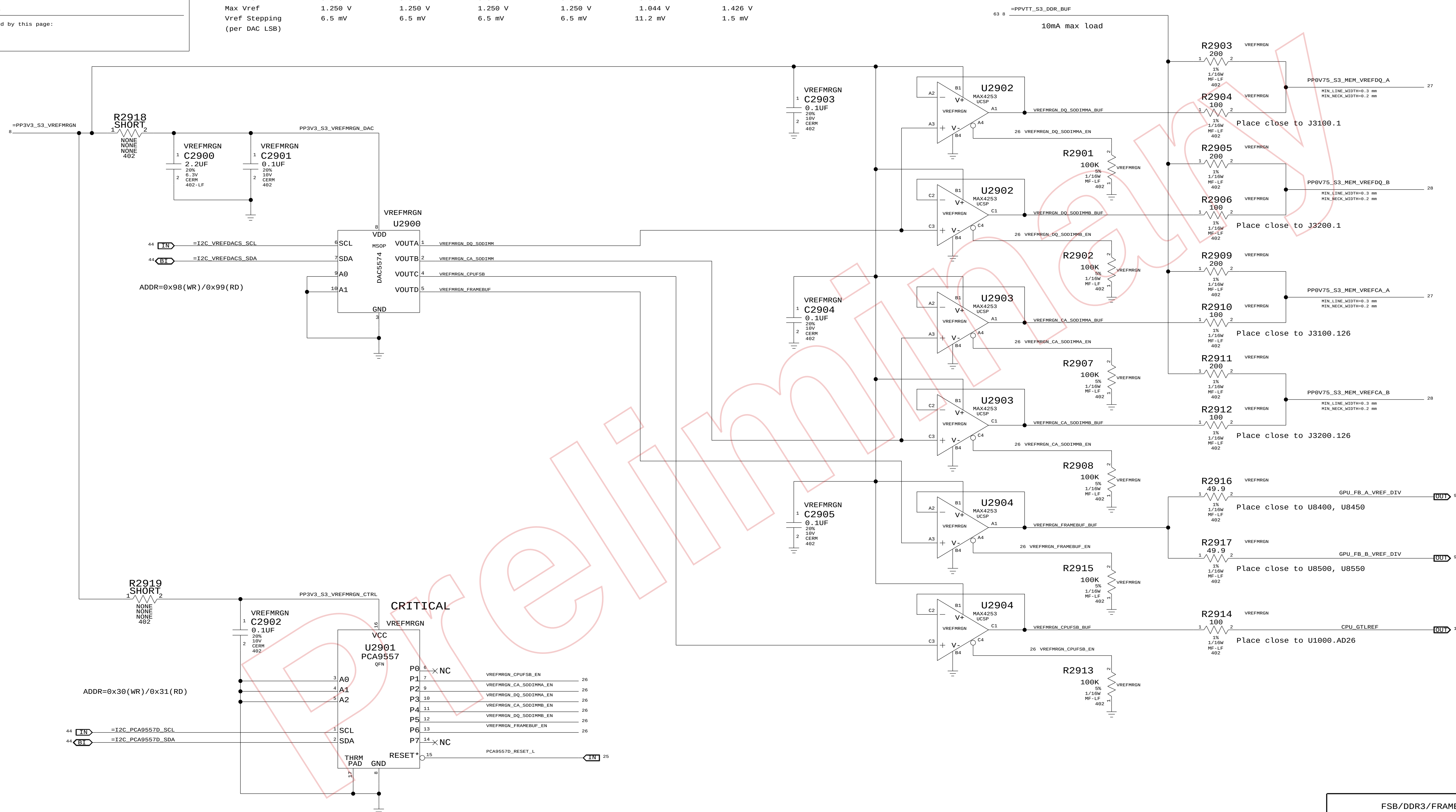
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	C	D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE | SHT 29 OF 123

Page Notes

Power aliases required by this page:

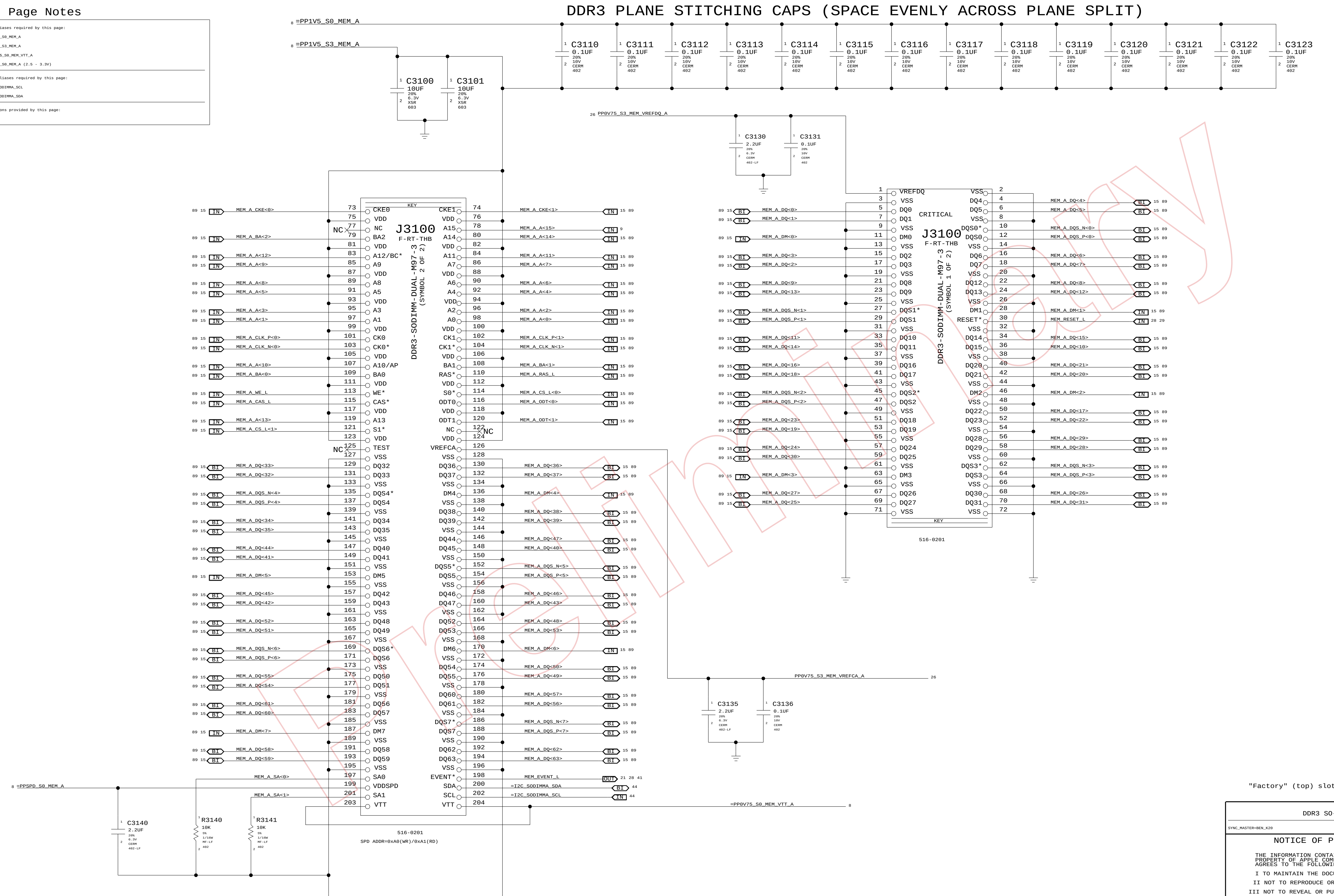
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN_K20 SYNC_DATE=06/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

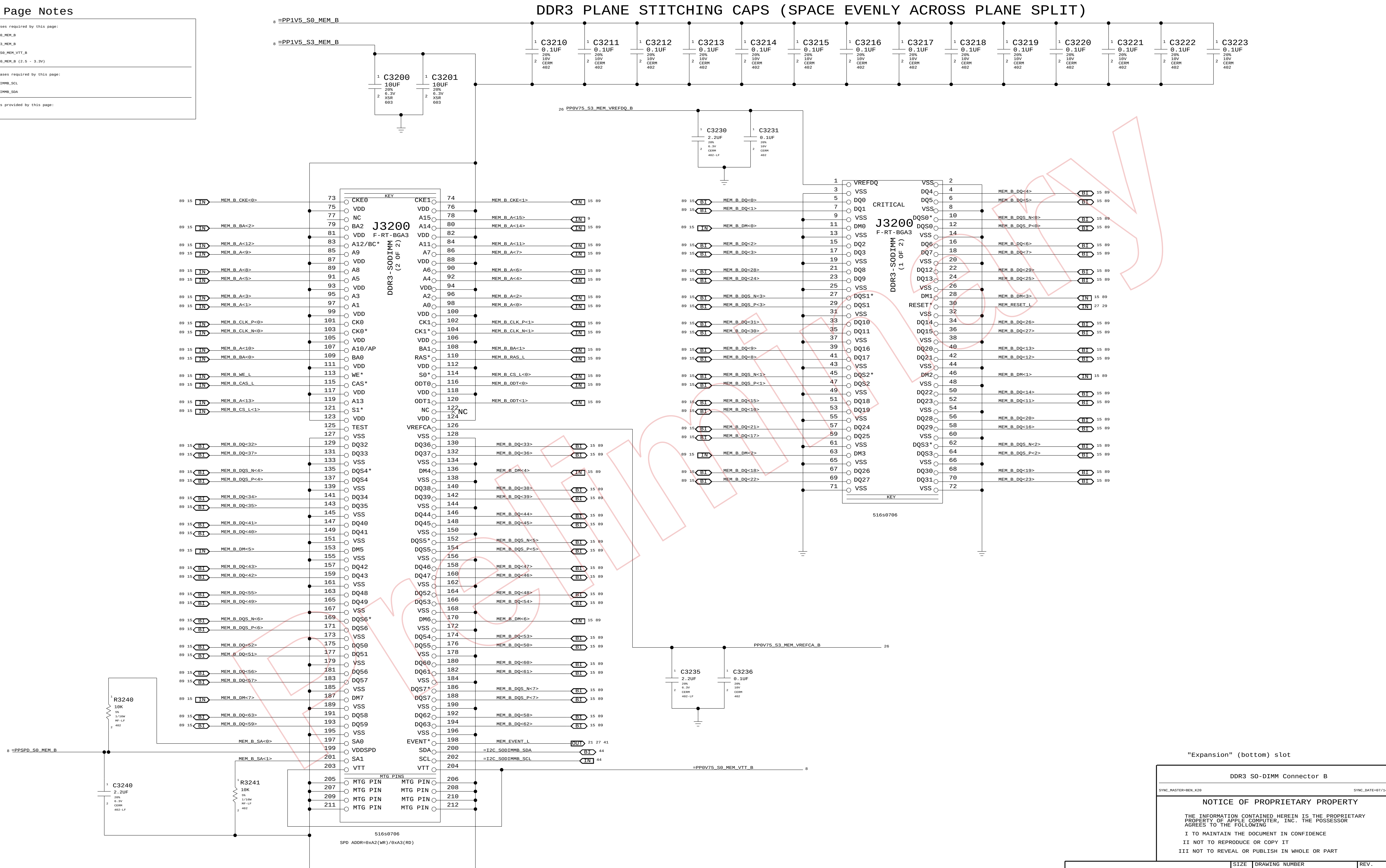
SCALE	SHT	OF
NONE	31	123

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=BEN_K20 SYNC_DATE=07/14/2009

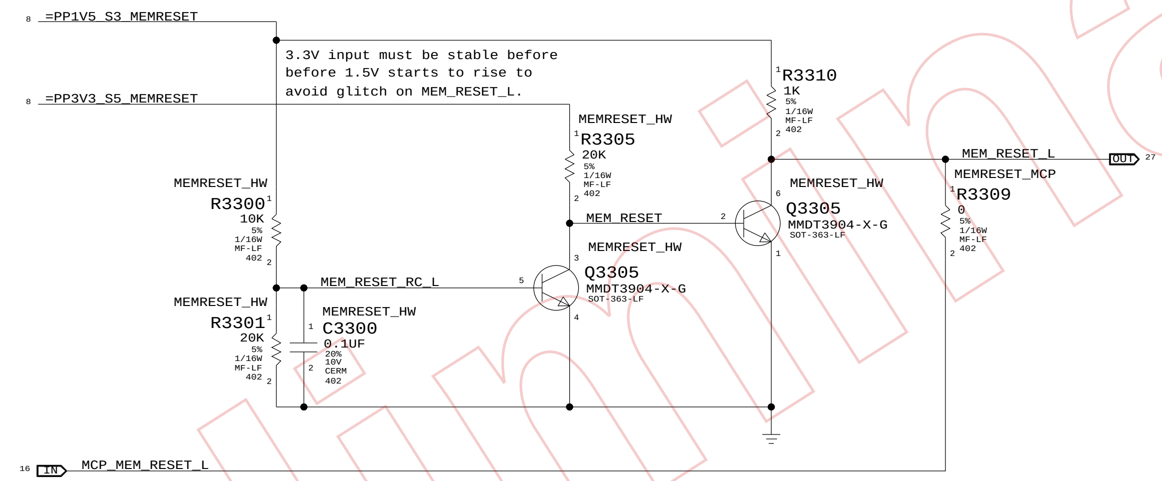
NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 32	OF 123

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

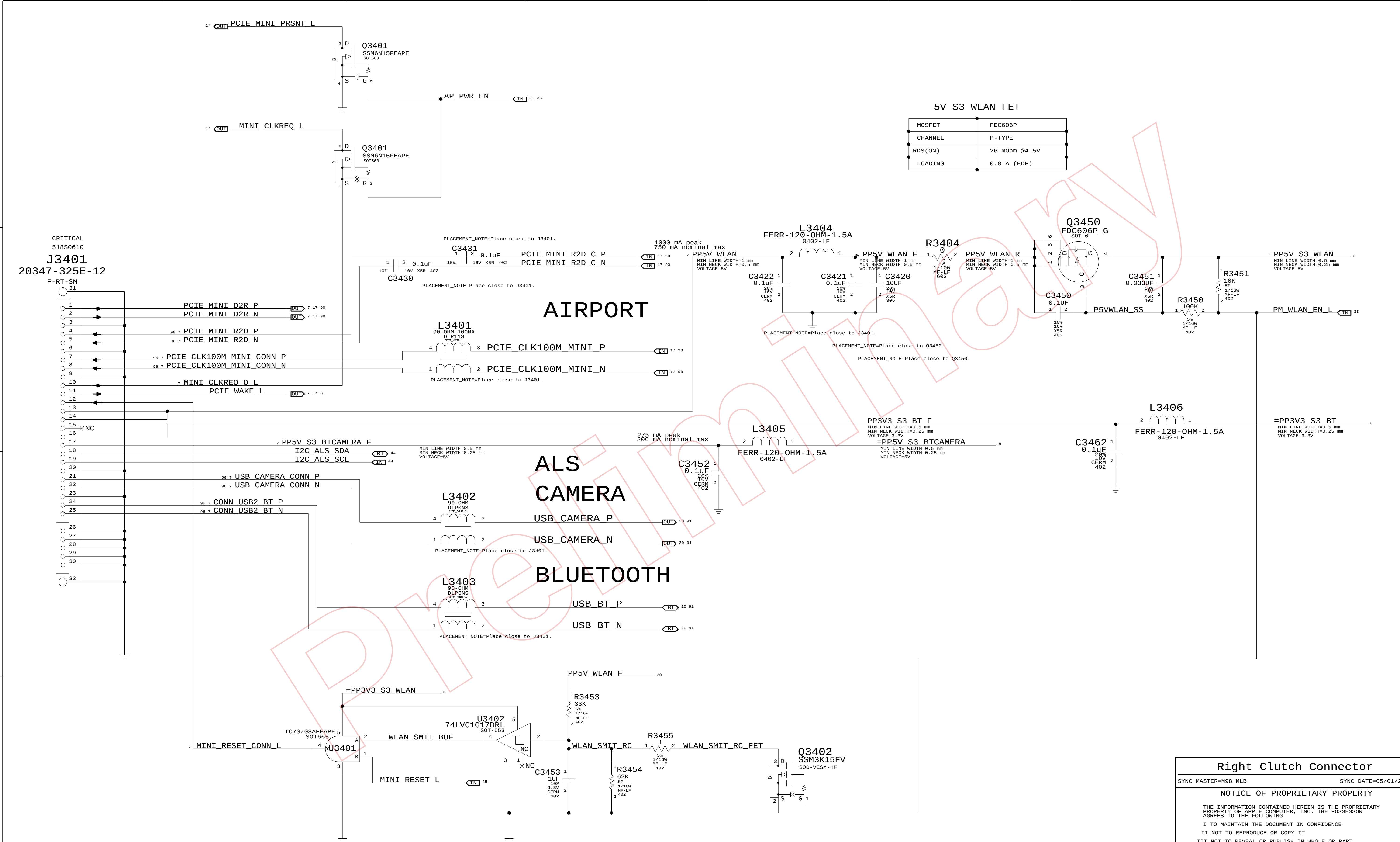


DDR3 Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 33	OF 123



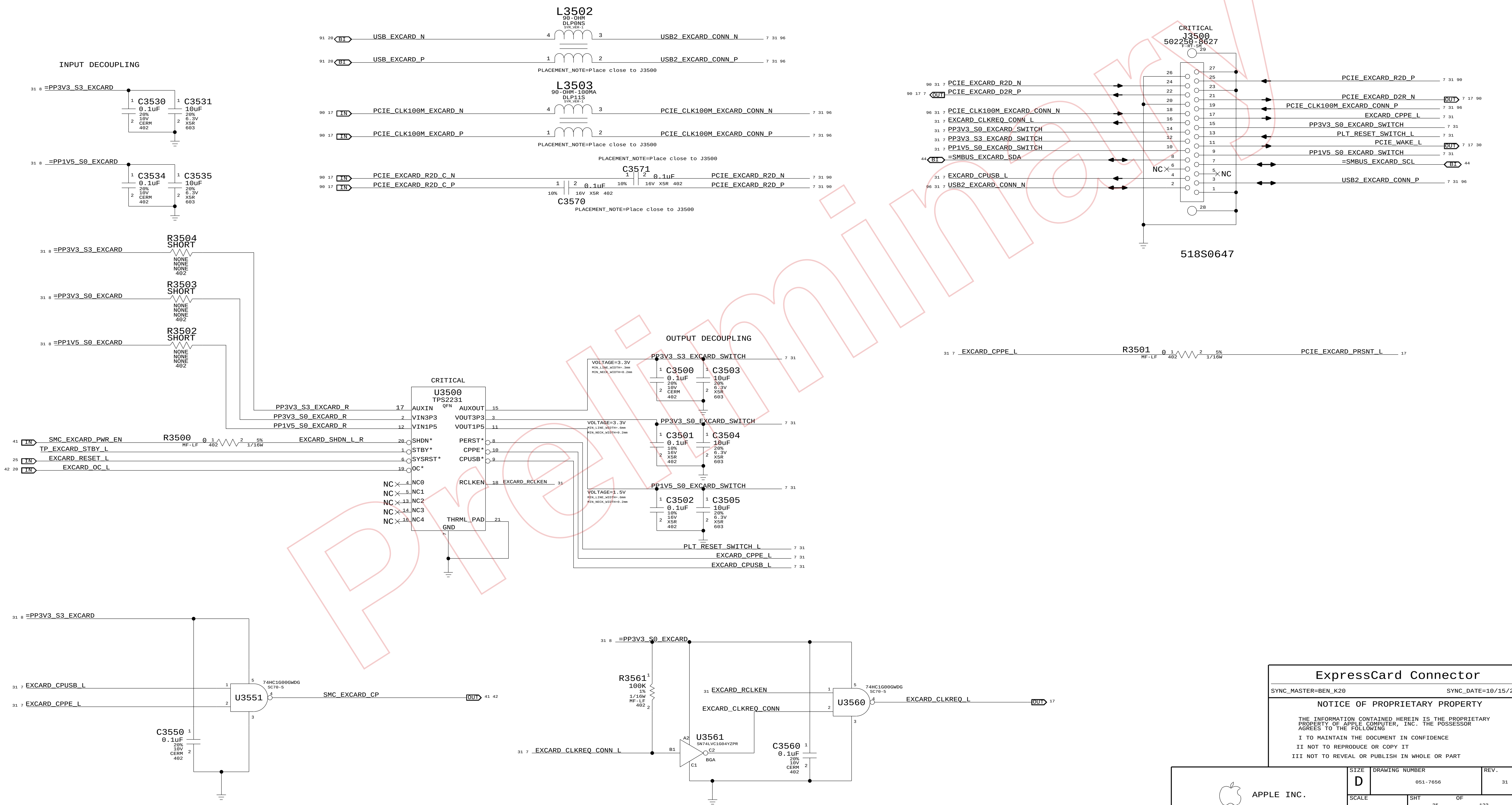
Right Clutch Connector

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 34	OF 123

EXPRESSCARD/34 FLEX CONNECTOR



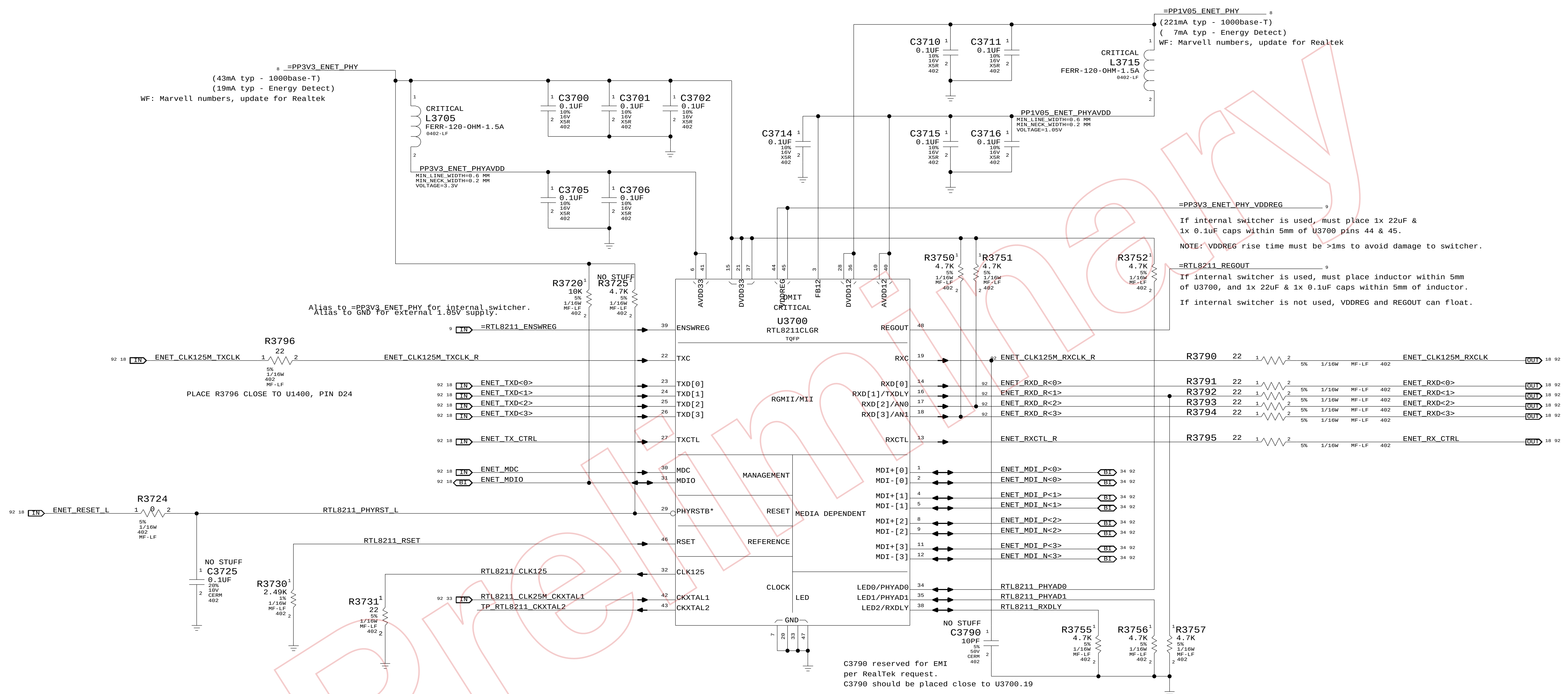
ExpressCard Connector

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 35	OF 123



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

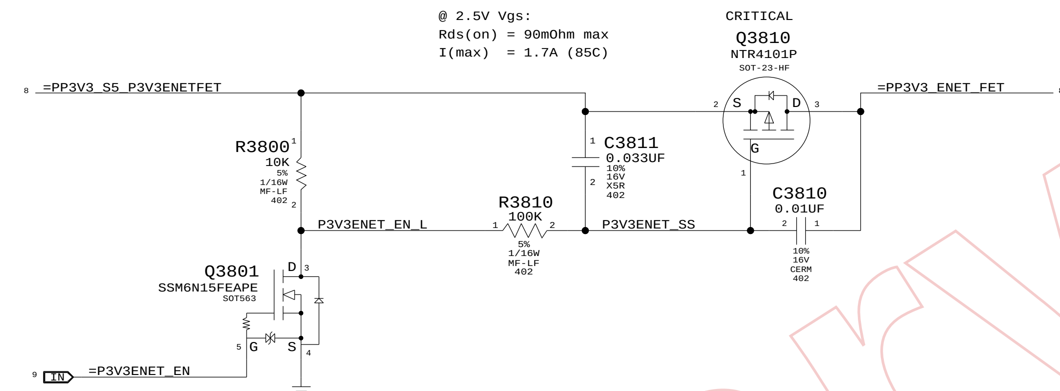
Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 37 OF 123	

3.3V ENET FET



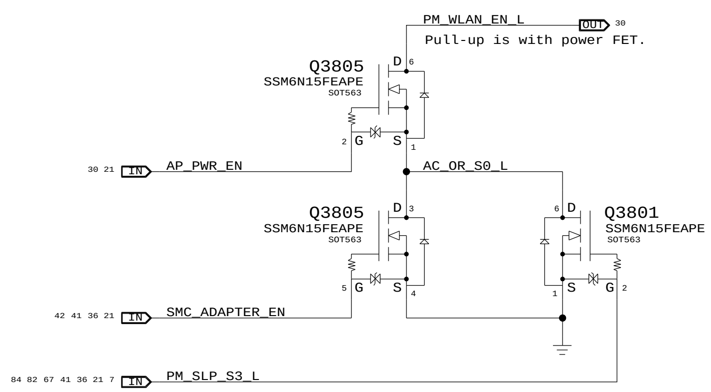
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

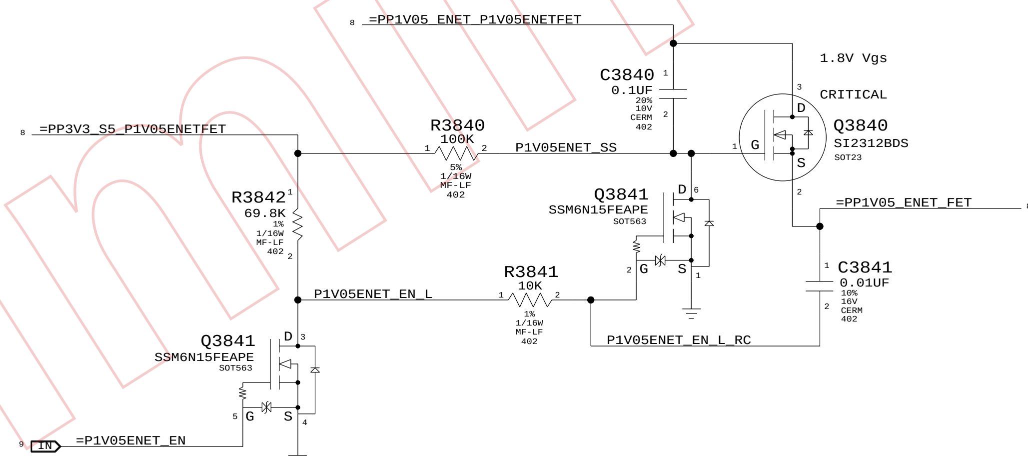
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

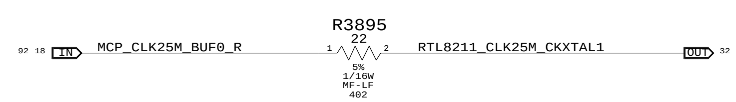


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



Ethernet & AirPort Support

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

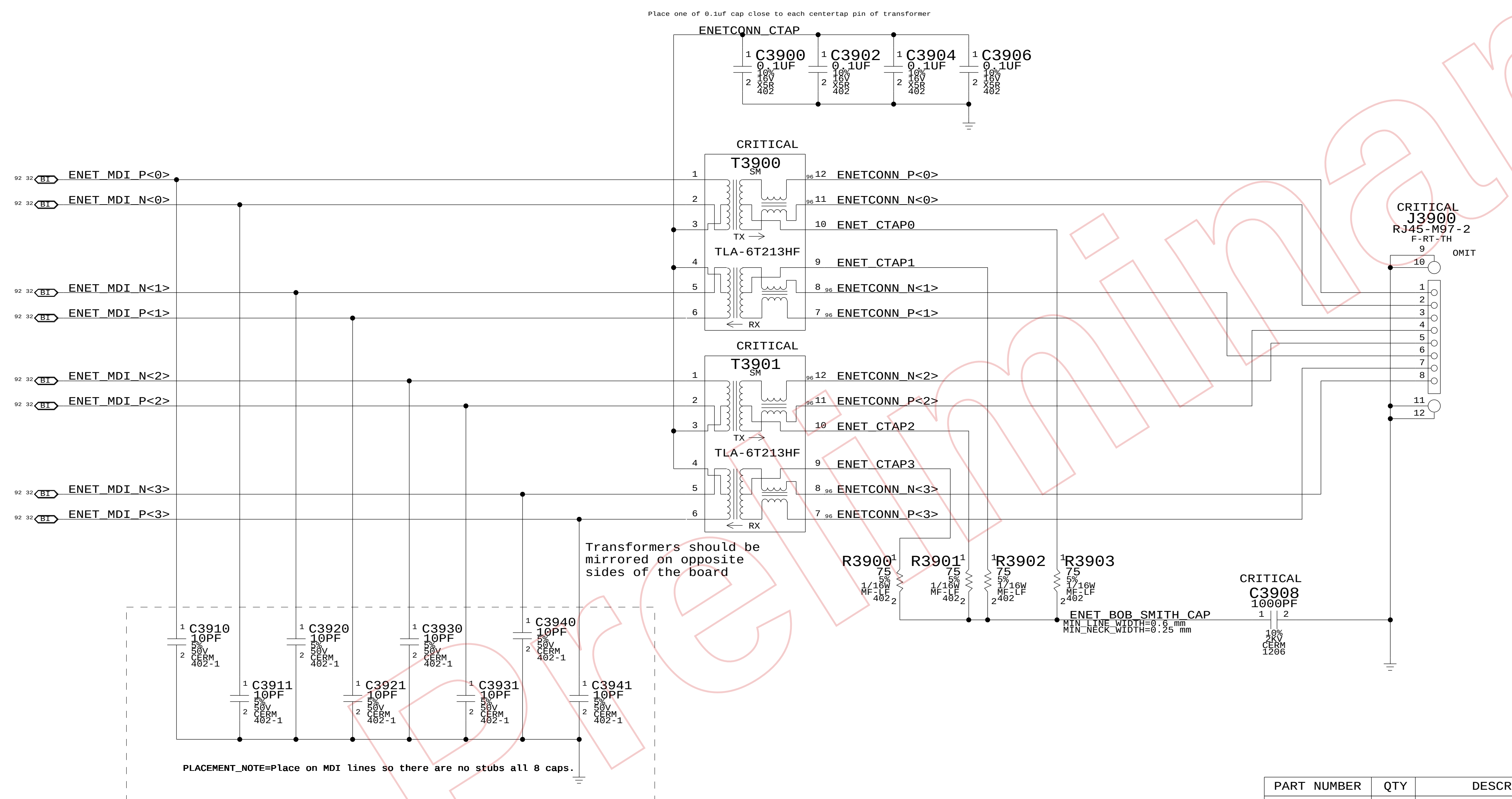
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 38	OF 123

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0636	1	CONN,RJ45,HB,10/100TX	J3900	CRITICAL	

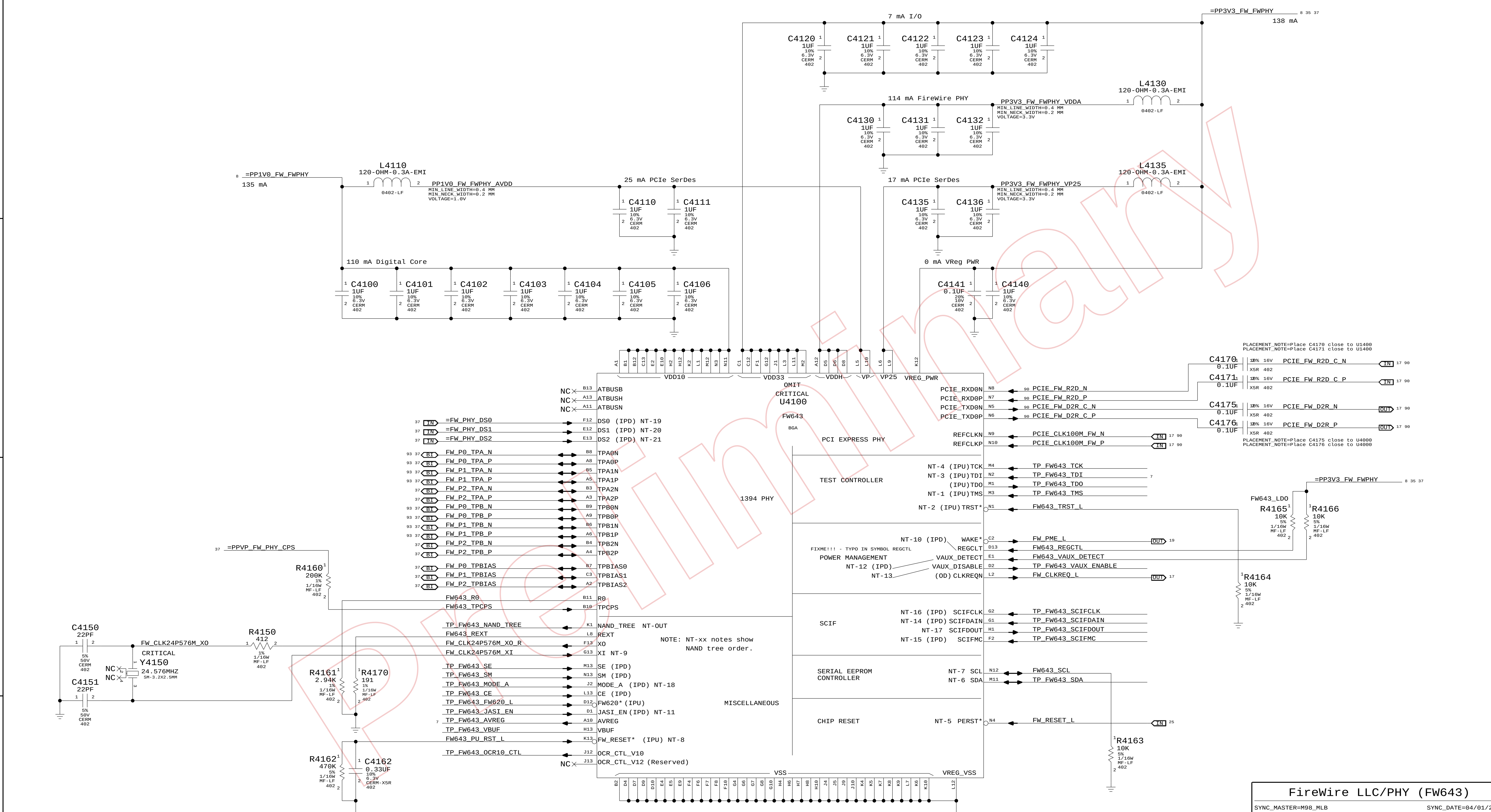
Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	39	123



FireWire LLC/PHY (FW643)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 41	OF 123

Page Notes

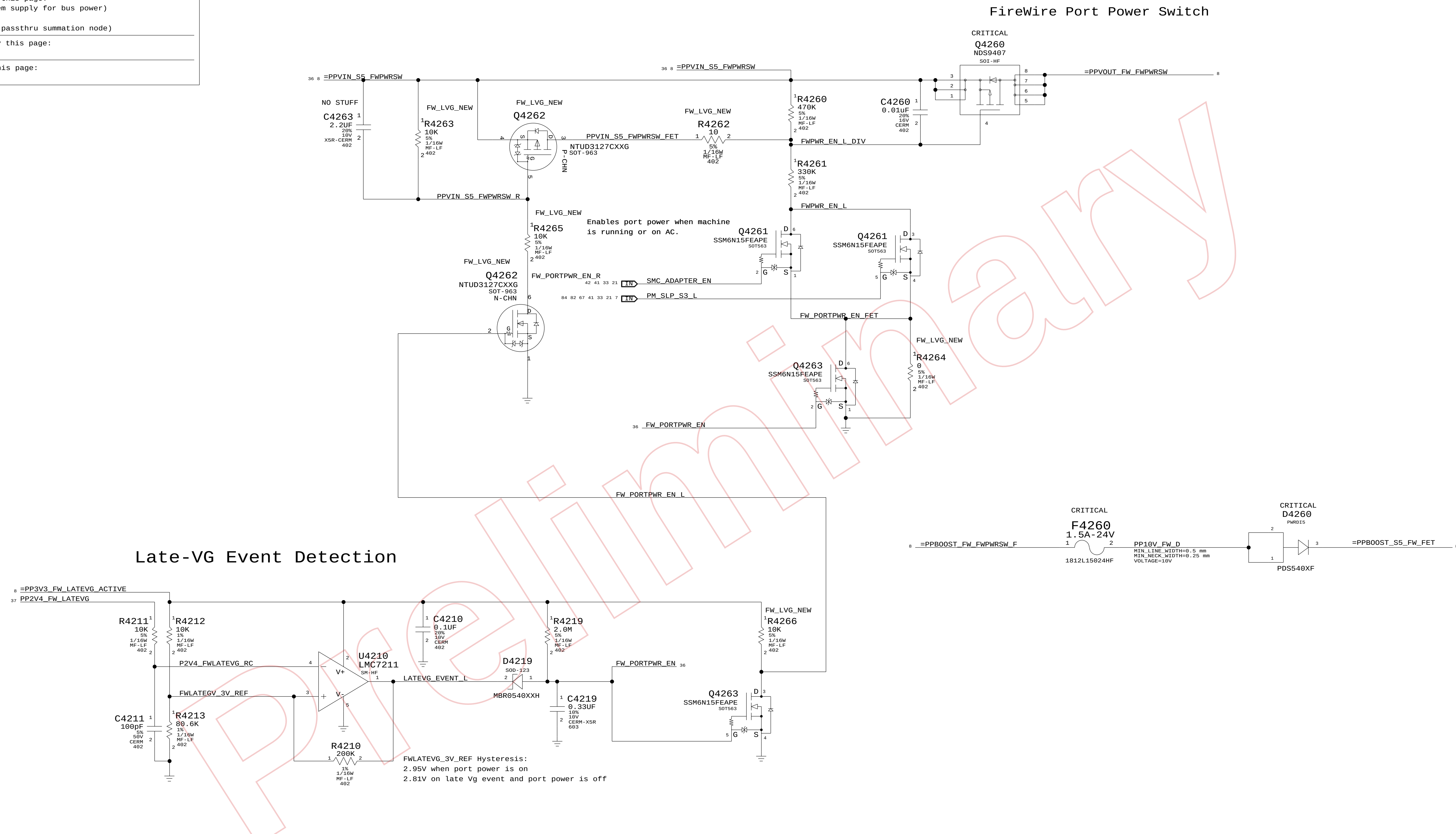
Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch

Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 42 OF 123

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

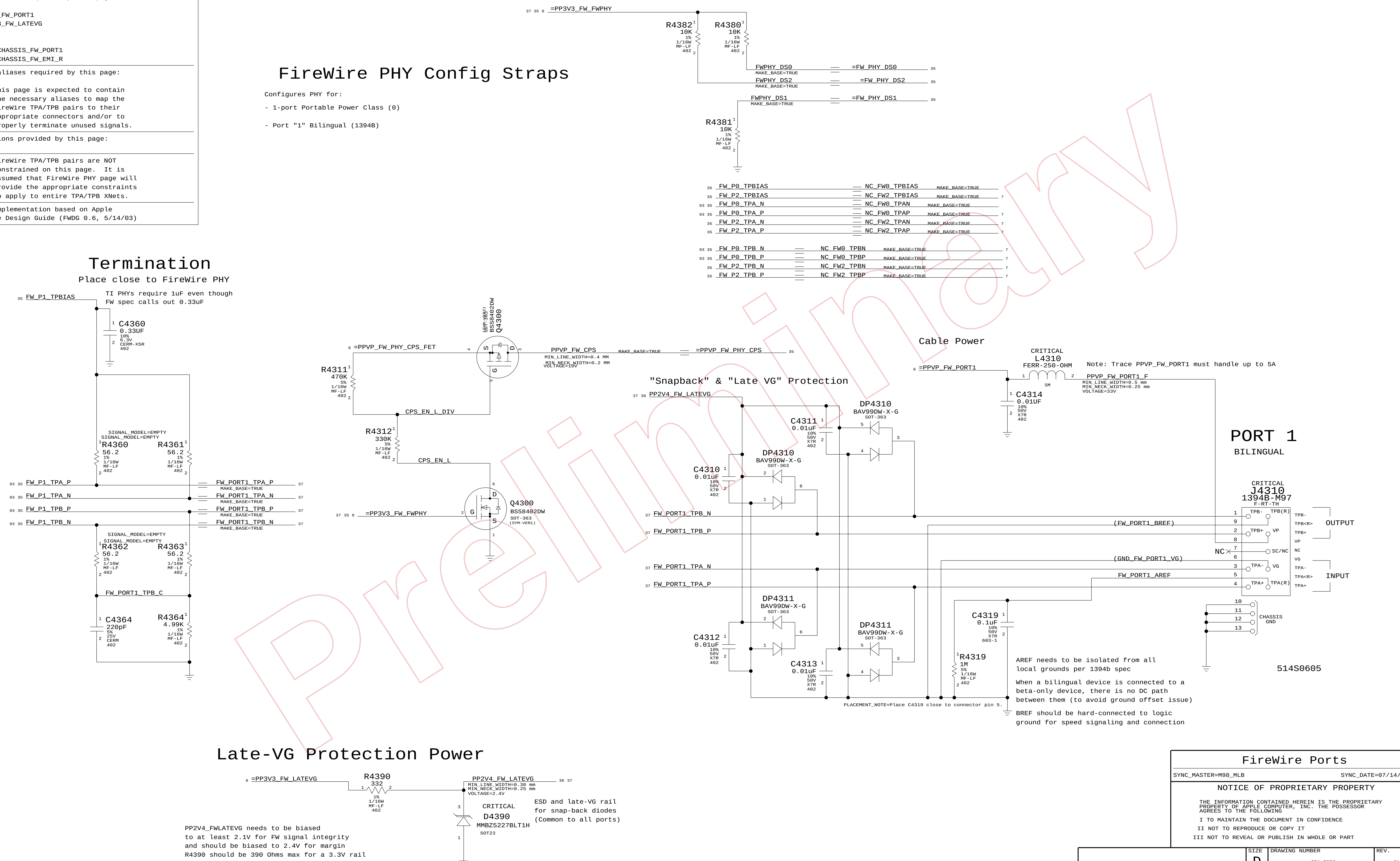
Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



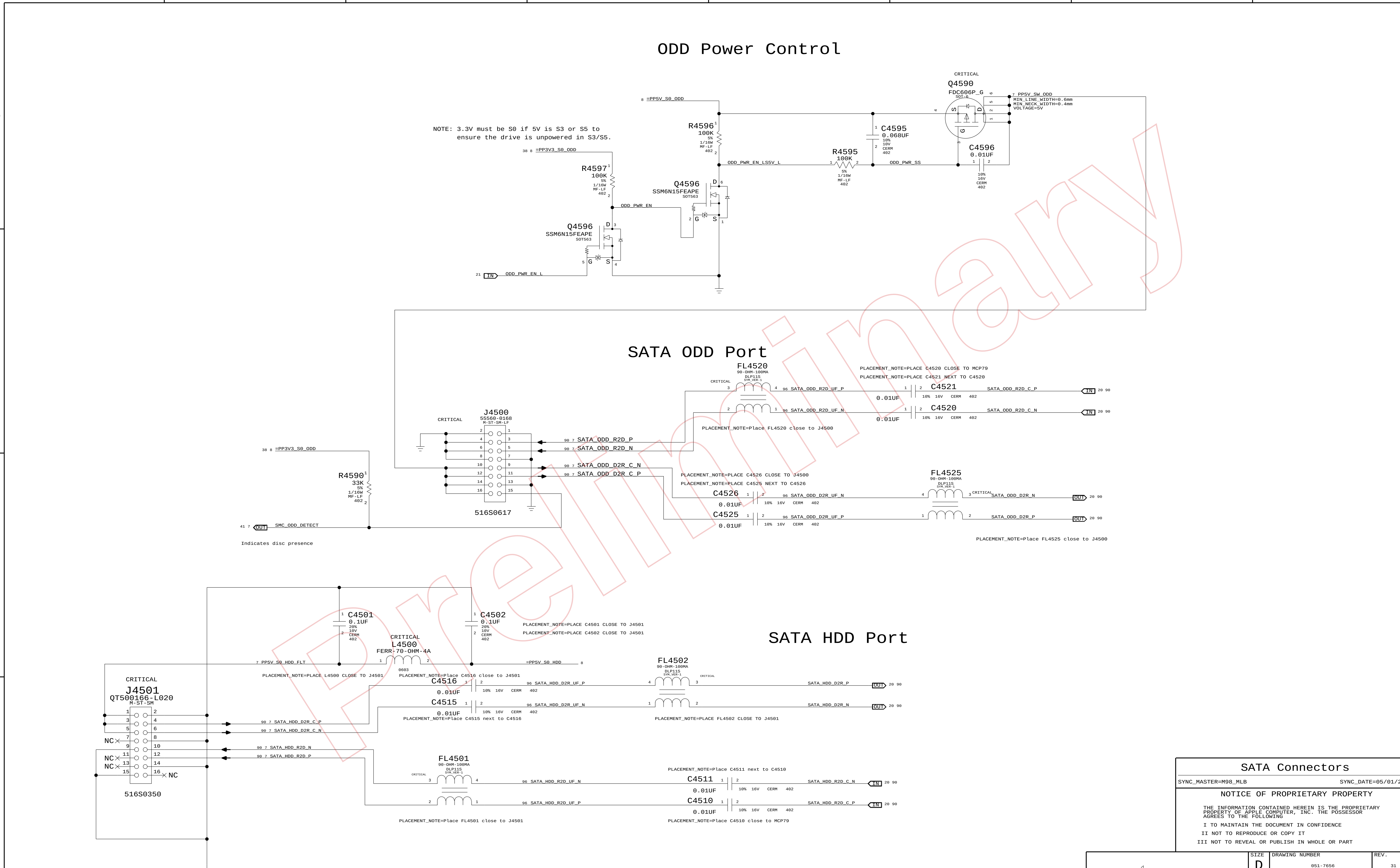
FireWire Ports

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 43	OF 123



SATA Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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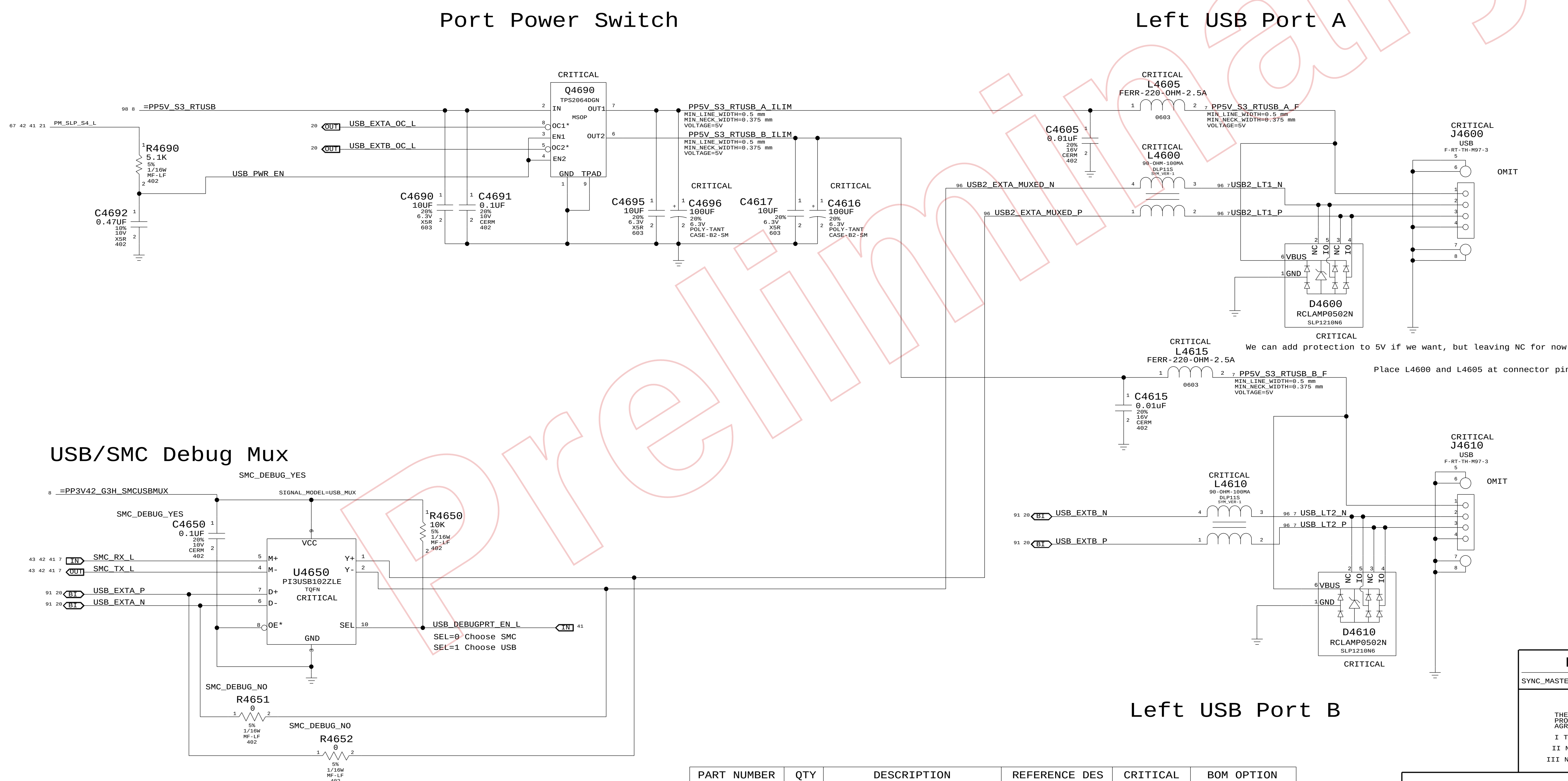
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 45	OF 123



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN,RCPT,USB,HB,4P	J4600, J4610	CRITICAL	

External USB Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

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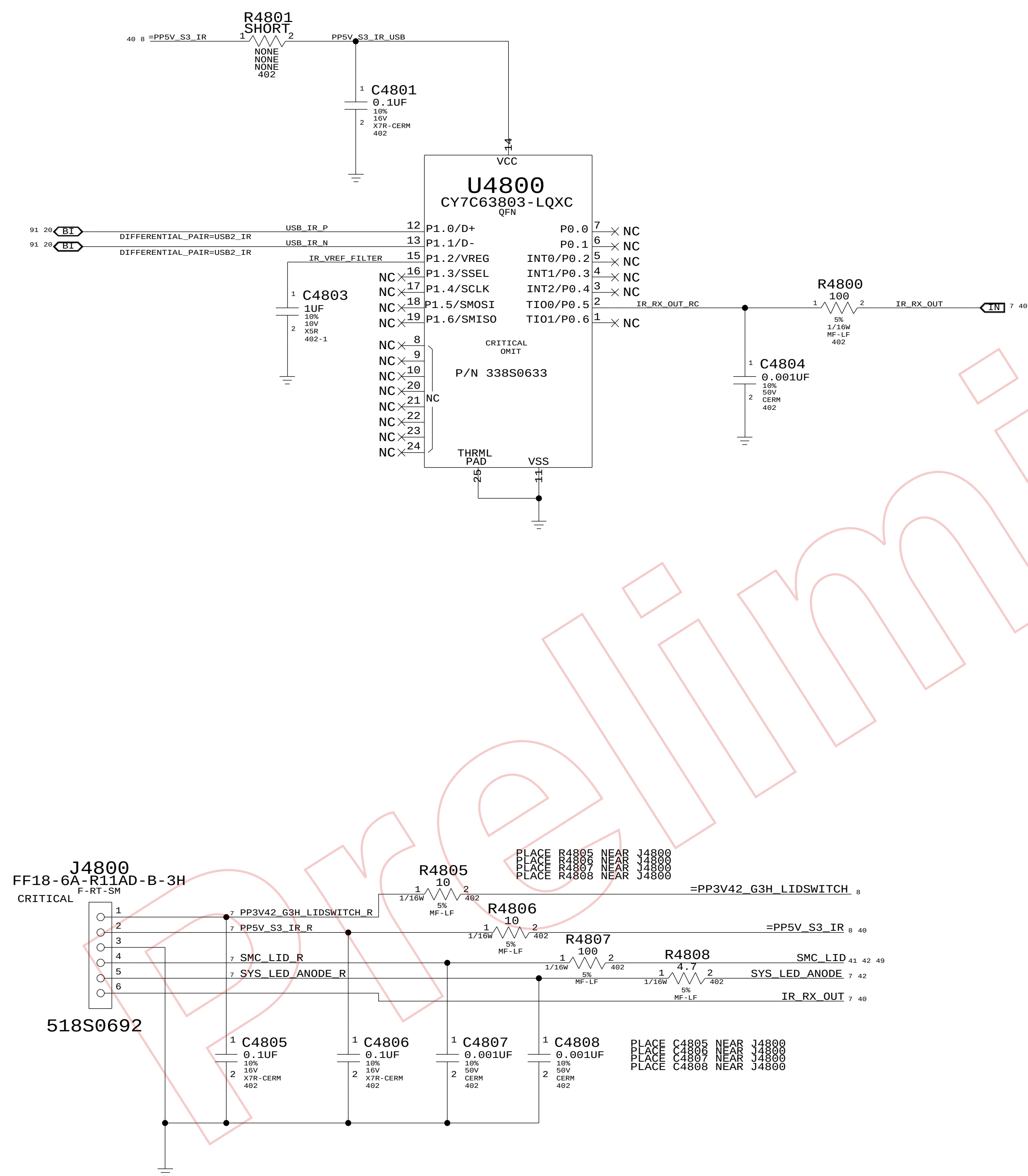
SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 46 OF 123



Front Flex Support

SYNC_MASTER=CHANG_K20 SYNC_DATE=07/18/2008

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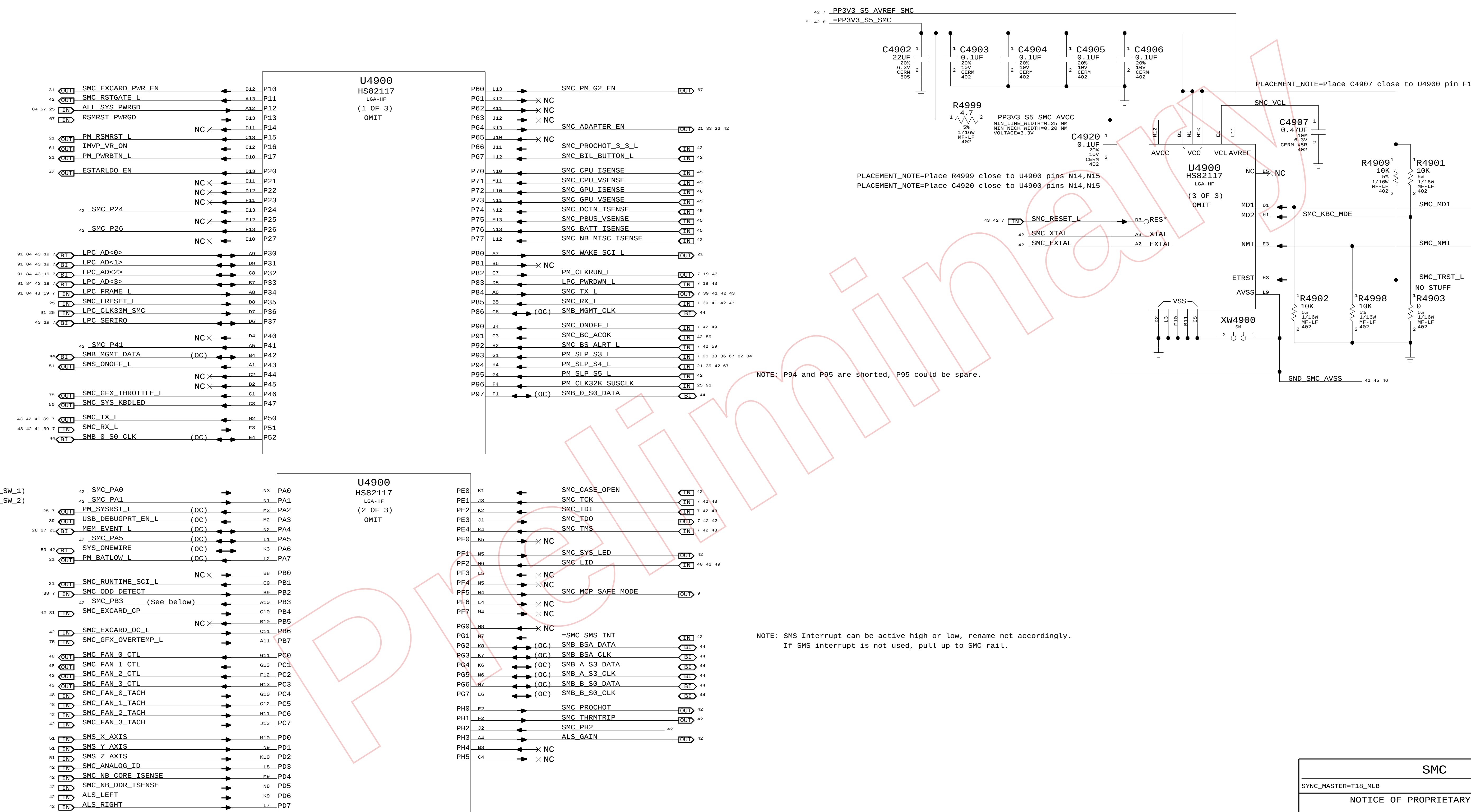
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	48	123

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

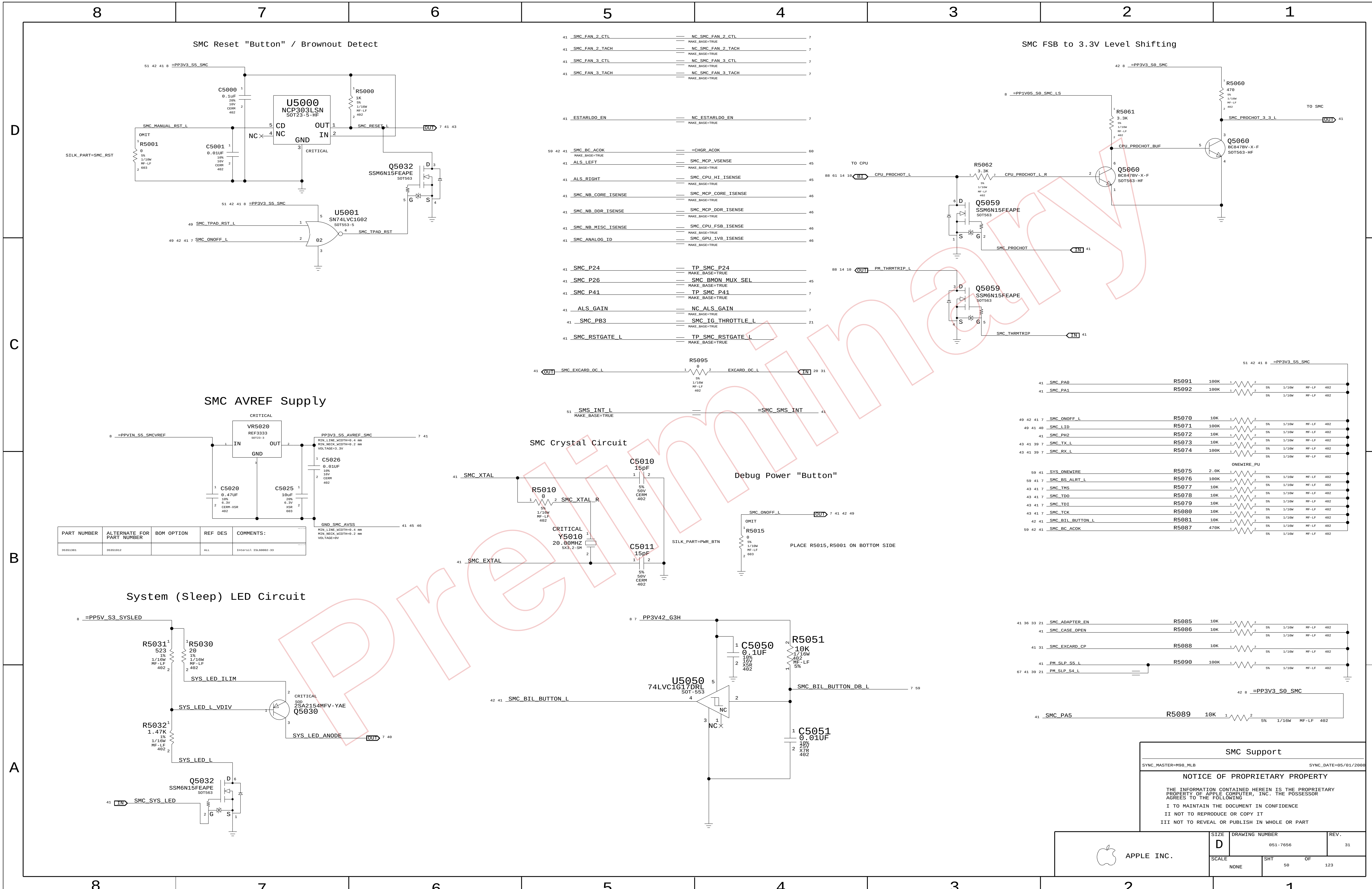
SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

NOTICE OF PROPRIETARY PROPERTY

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 49	OF 123

APPLE INC.



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

SMC Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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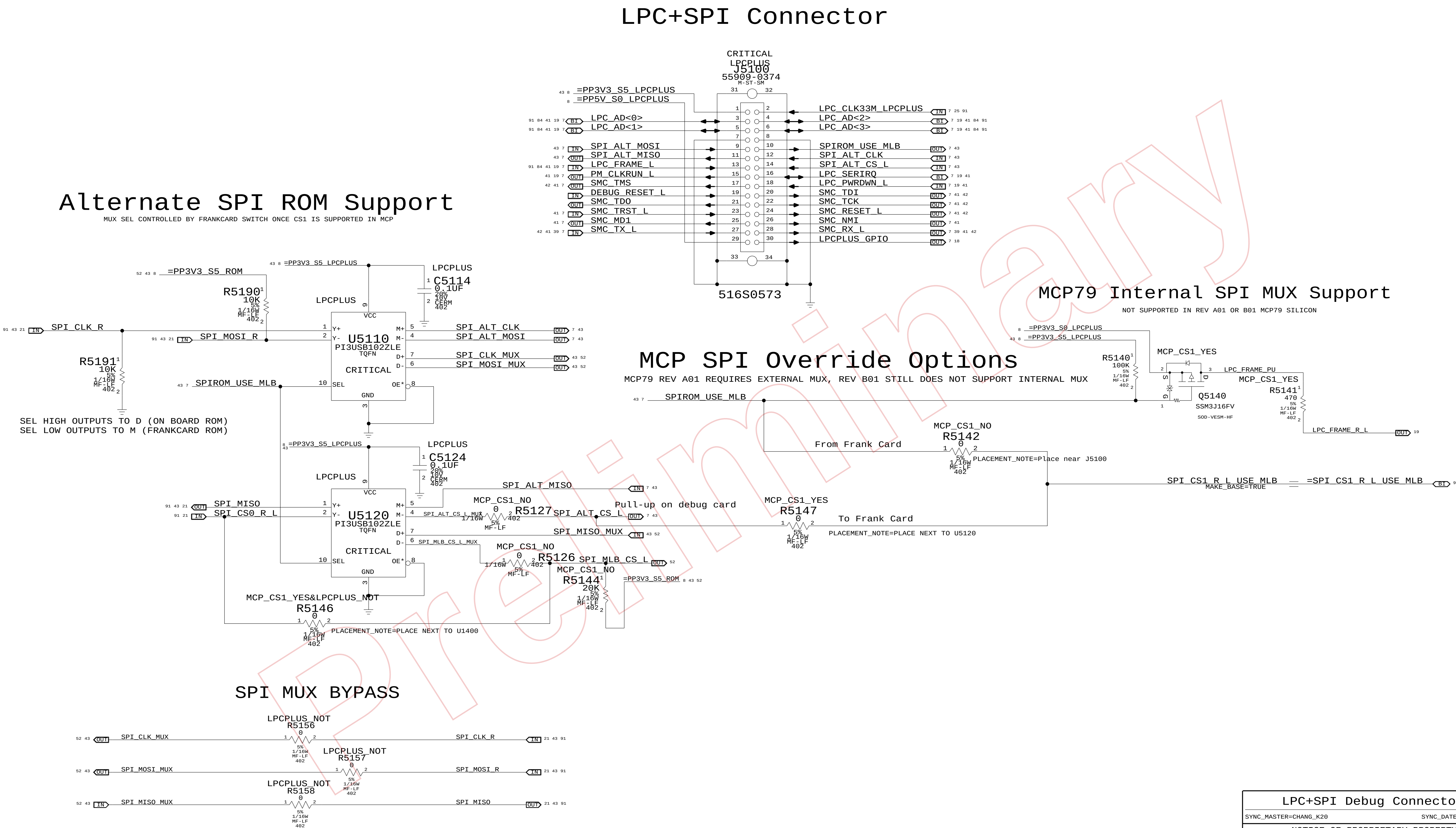
SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	50	123



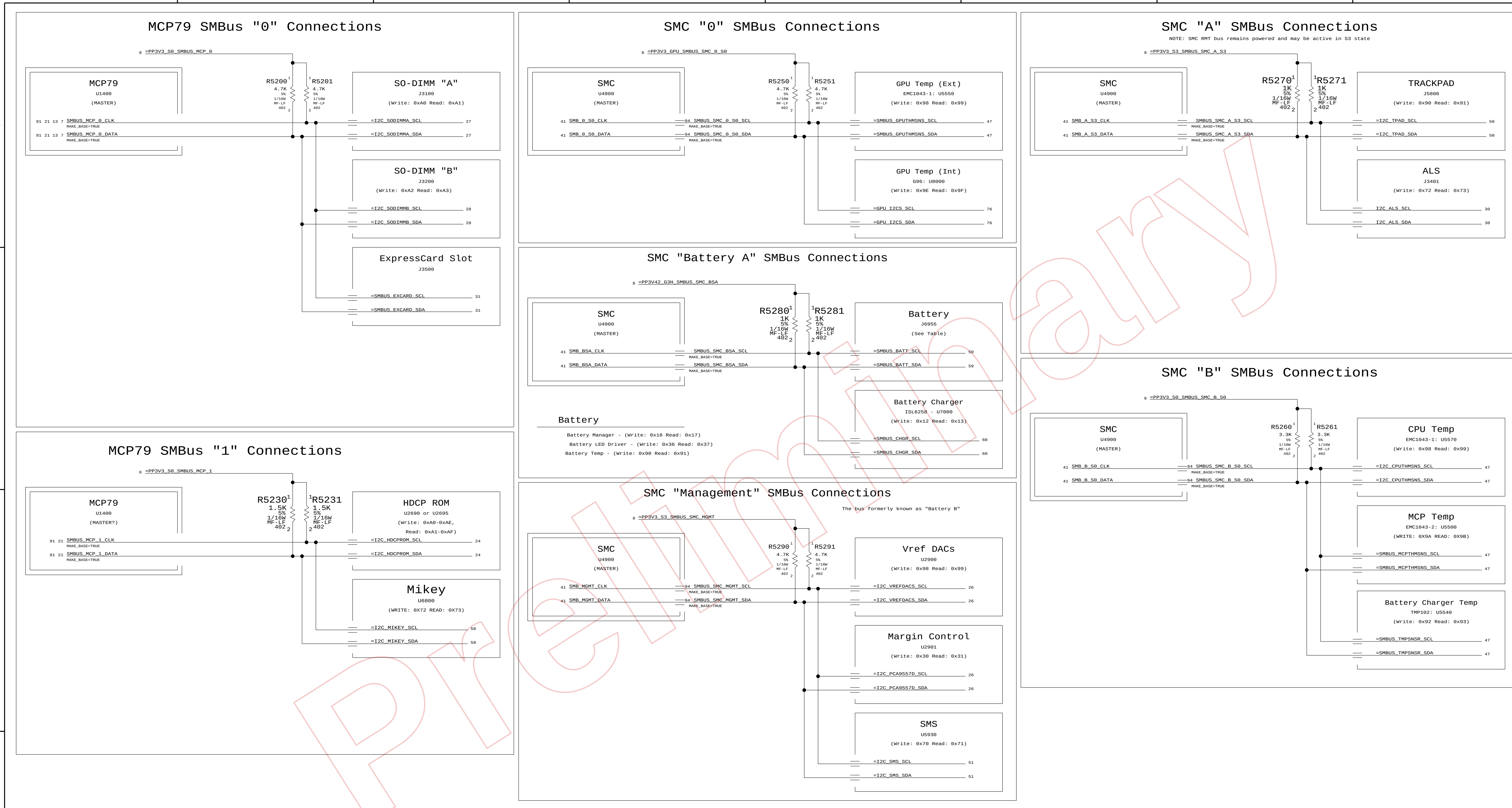
LPC+SPI Debug Connector

SYNC_MASTER=CHANG_K20 SYNC_DATE=05/28/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE NONE SHT 51 OF 123

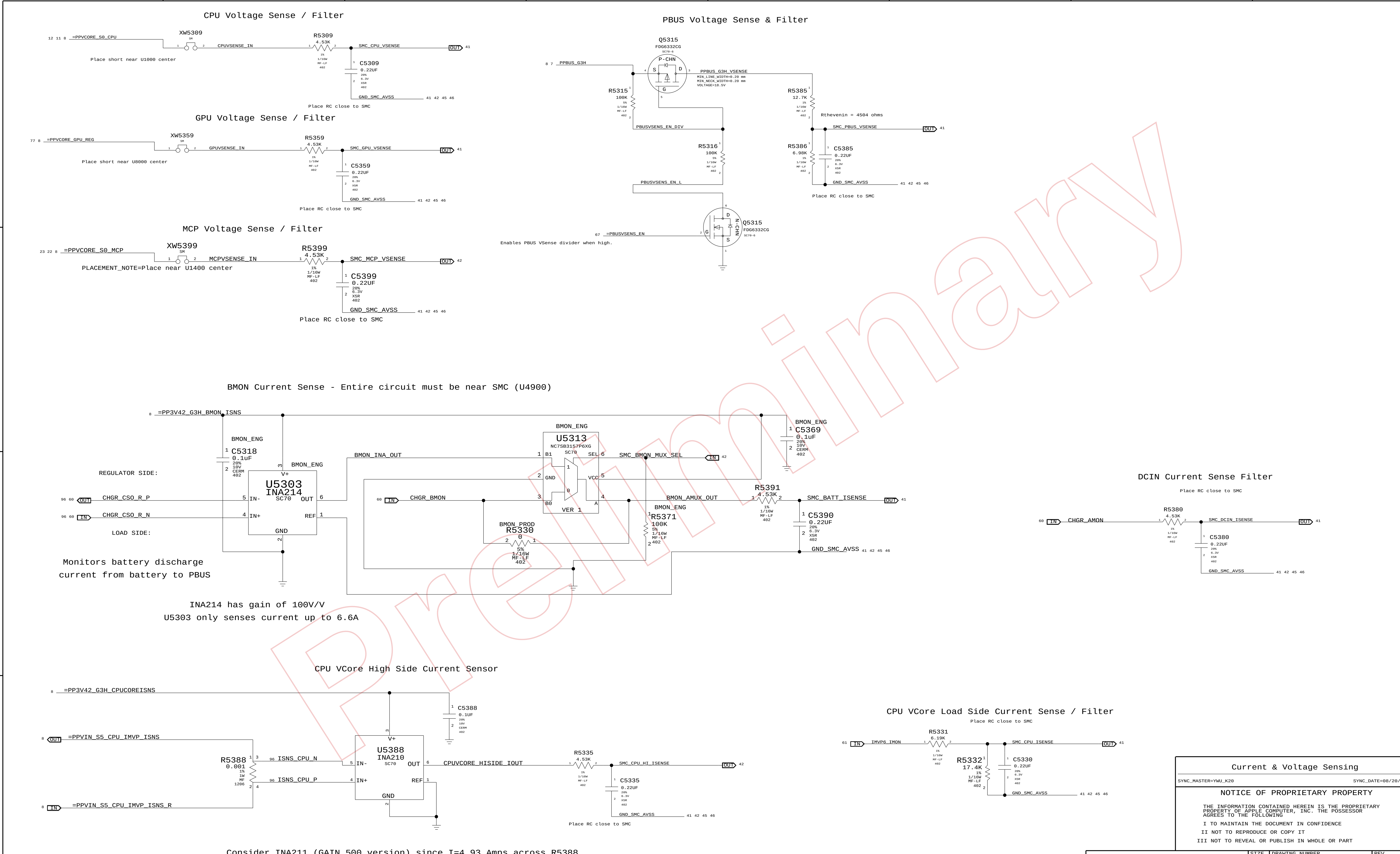


K20 SMBUS CONNECTIONS

SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 52	OF 123



Current & Voltage Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/20/2008

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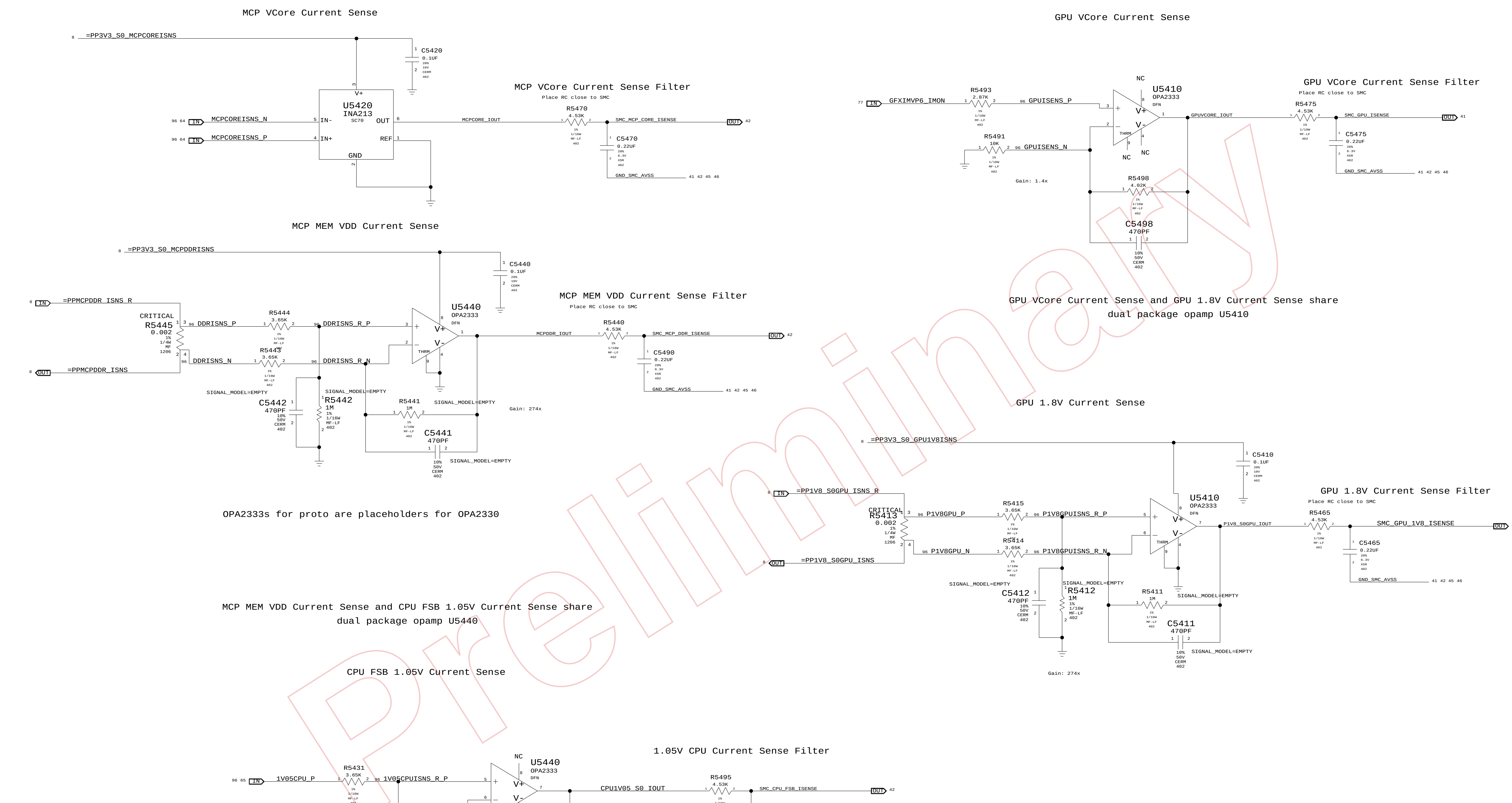
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 53	OF 123



Current Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/12/2008

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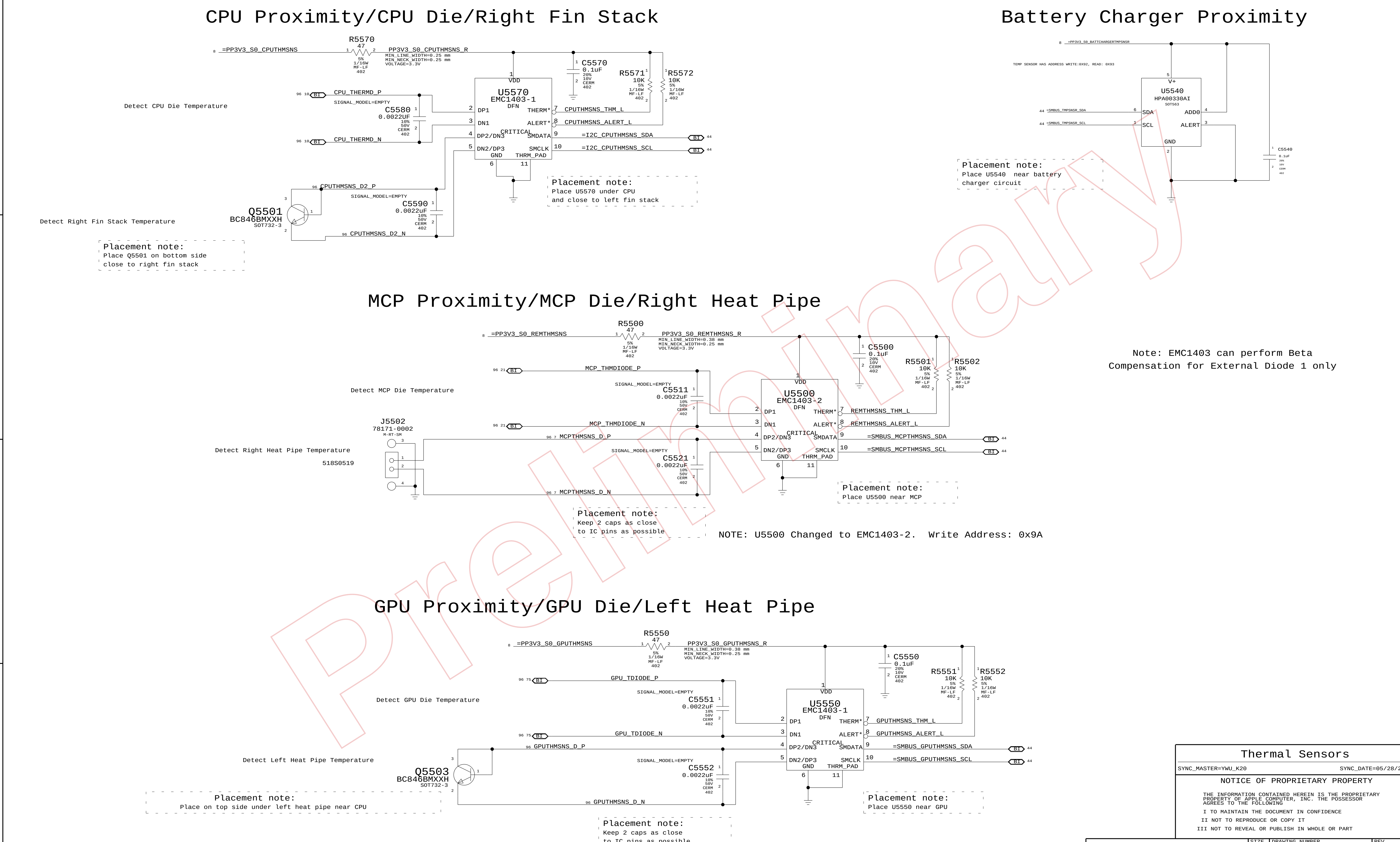
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 54	OF 123



Thermal Sensors

SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

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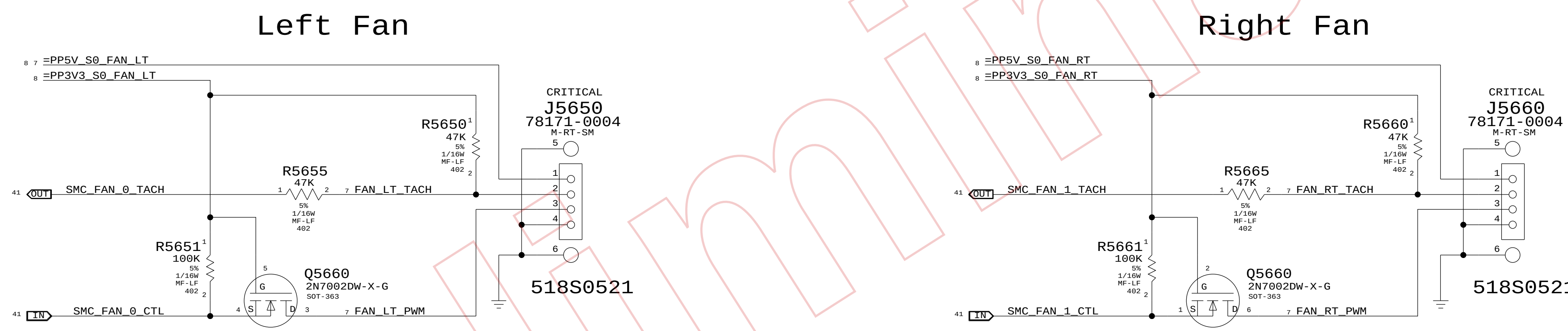
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	55	123



Fan Connectors

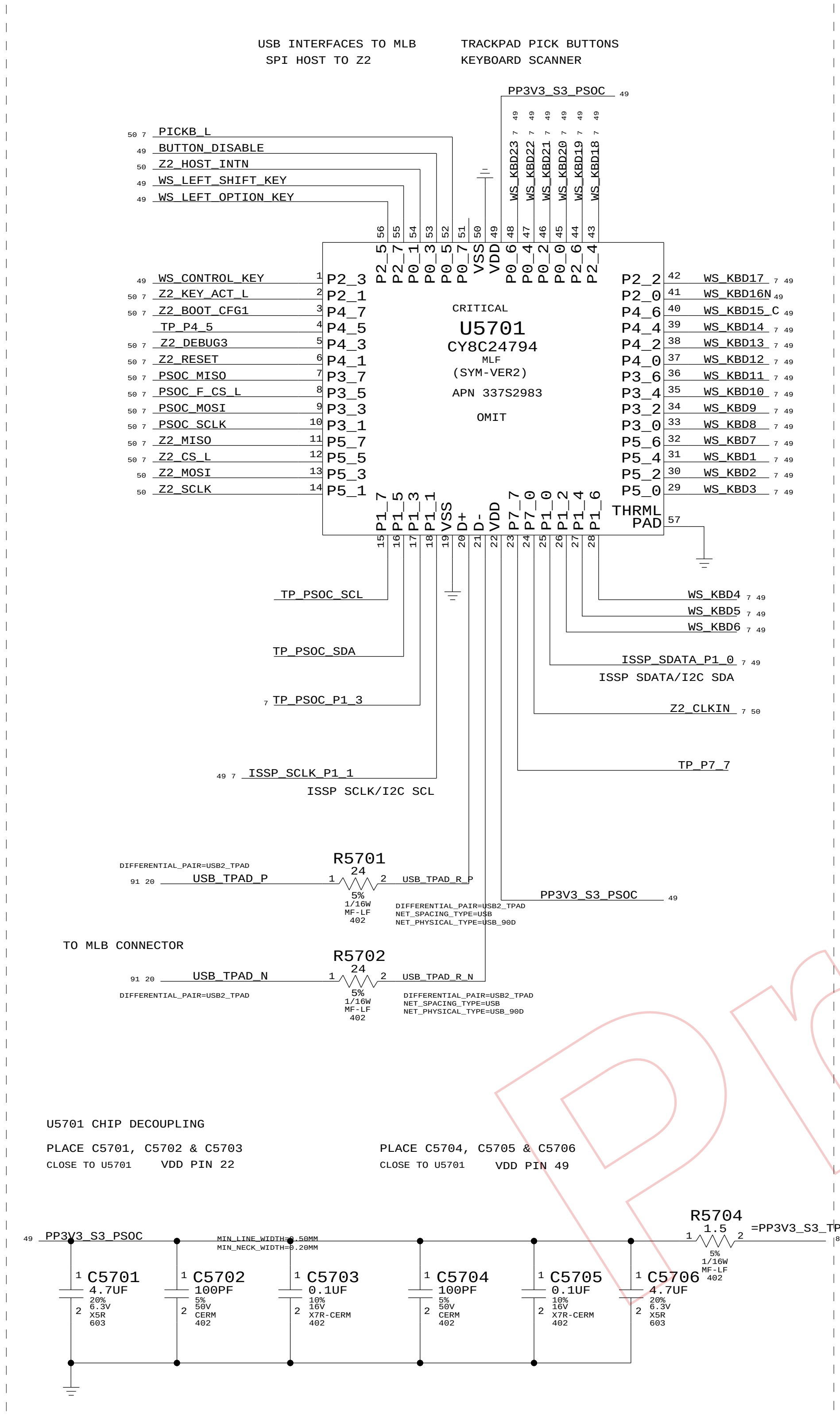
SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	56	123

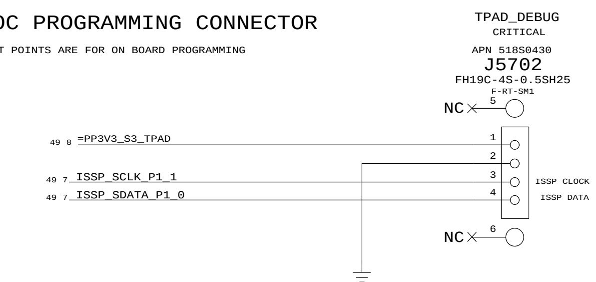
PSOC USB CONTROLLER



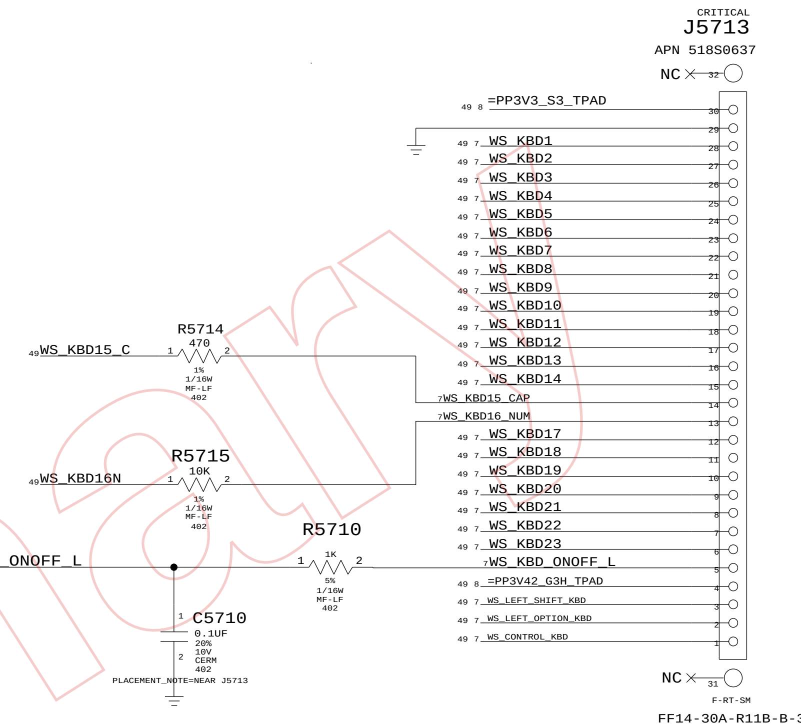
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

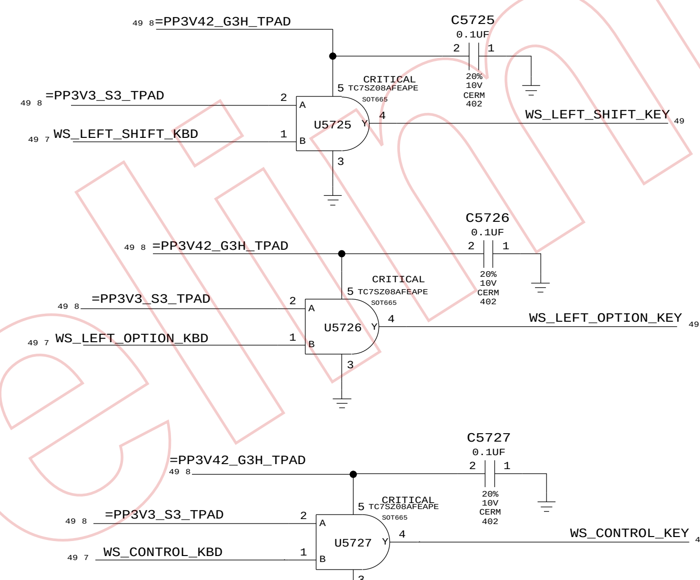
TEST POINTS ARE FOR ON BOARD PROGRAMMING



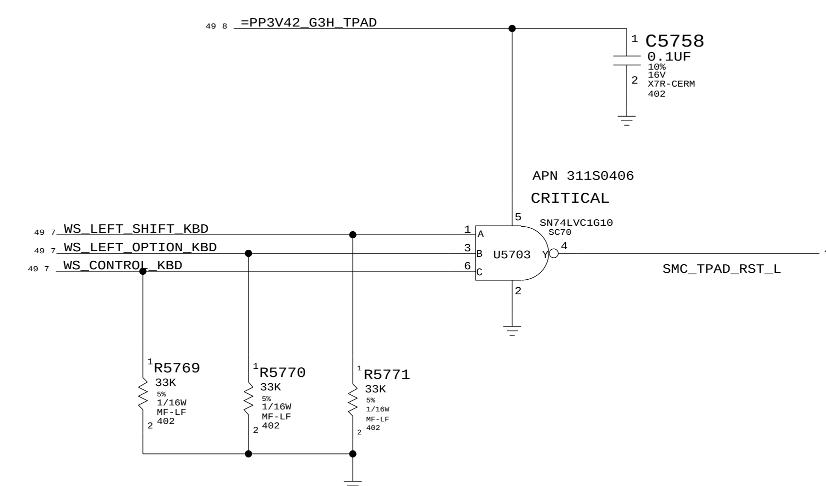
KEYBOARD CONNECTOR



ISOLATION CIRCUIT

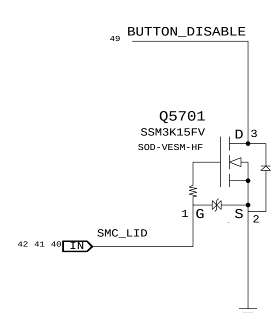


SMC_MANUAL_RESET LOGIC



TPAD BUTTONS DISABLE

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB



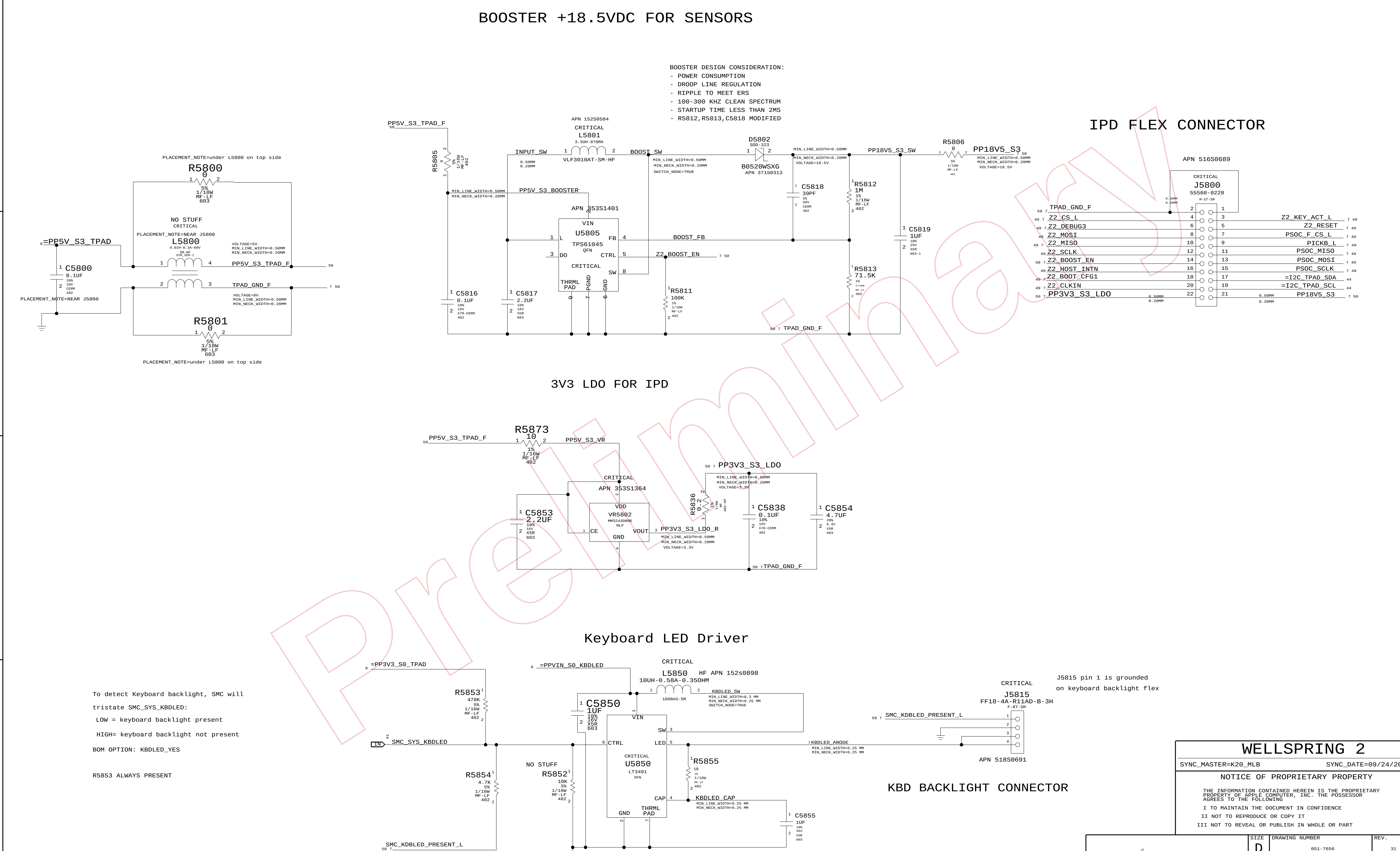
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

WELLSPRING 1

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 57	OF 123



To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT

WELLSPRING 2

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

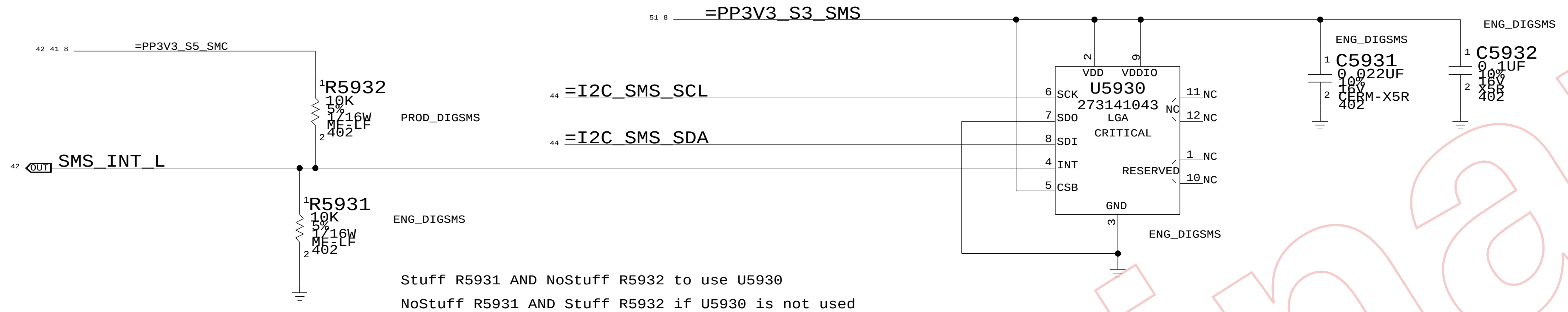
NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 58	OF 123

Digital SMS

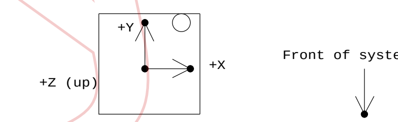
Pull-up required if SMS_INT_L not used.



Stuff R5931 AND NoStuff R5932 to use U5930

NoStuff R5931 AND Stuff R5932 if U5930 is not used

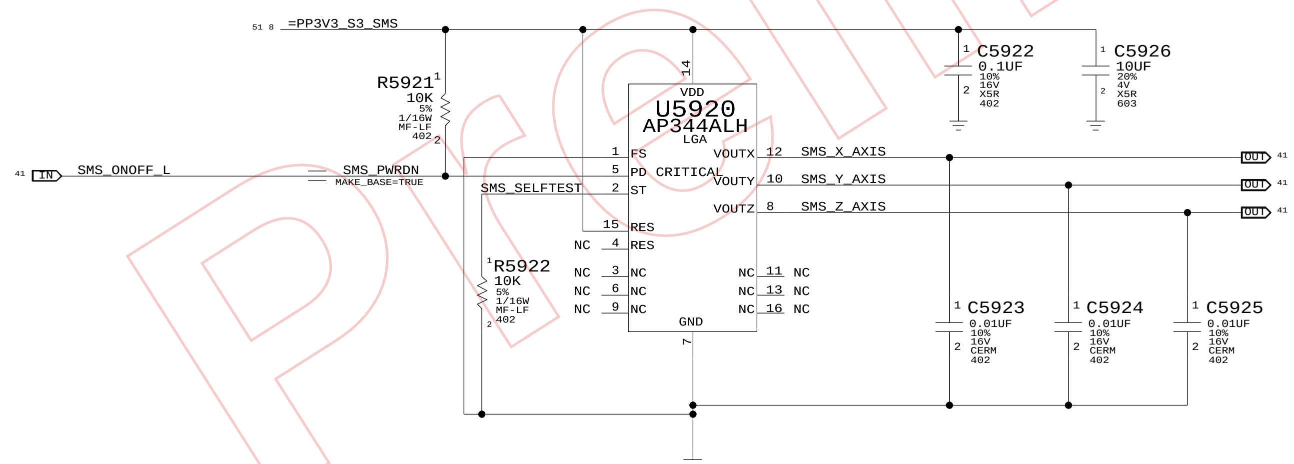
Desired orientation when
placed on board top-side:



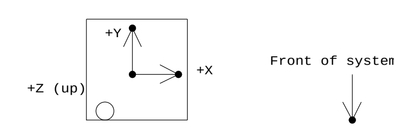
Circle indicates pin 1 location when placed
in correct orientation

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when
placed on board top-side:



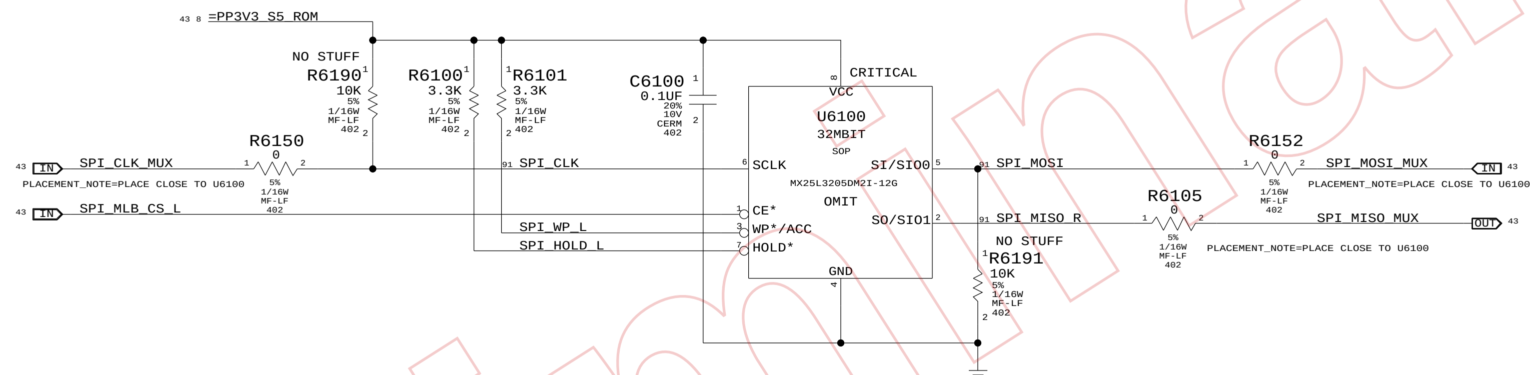
Circle indicates pin 1 location when placed
in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 59	OF 123



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

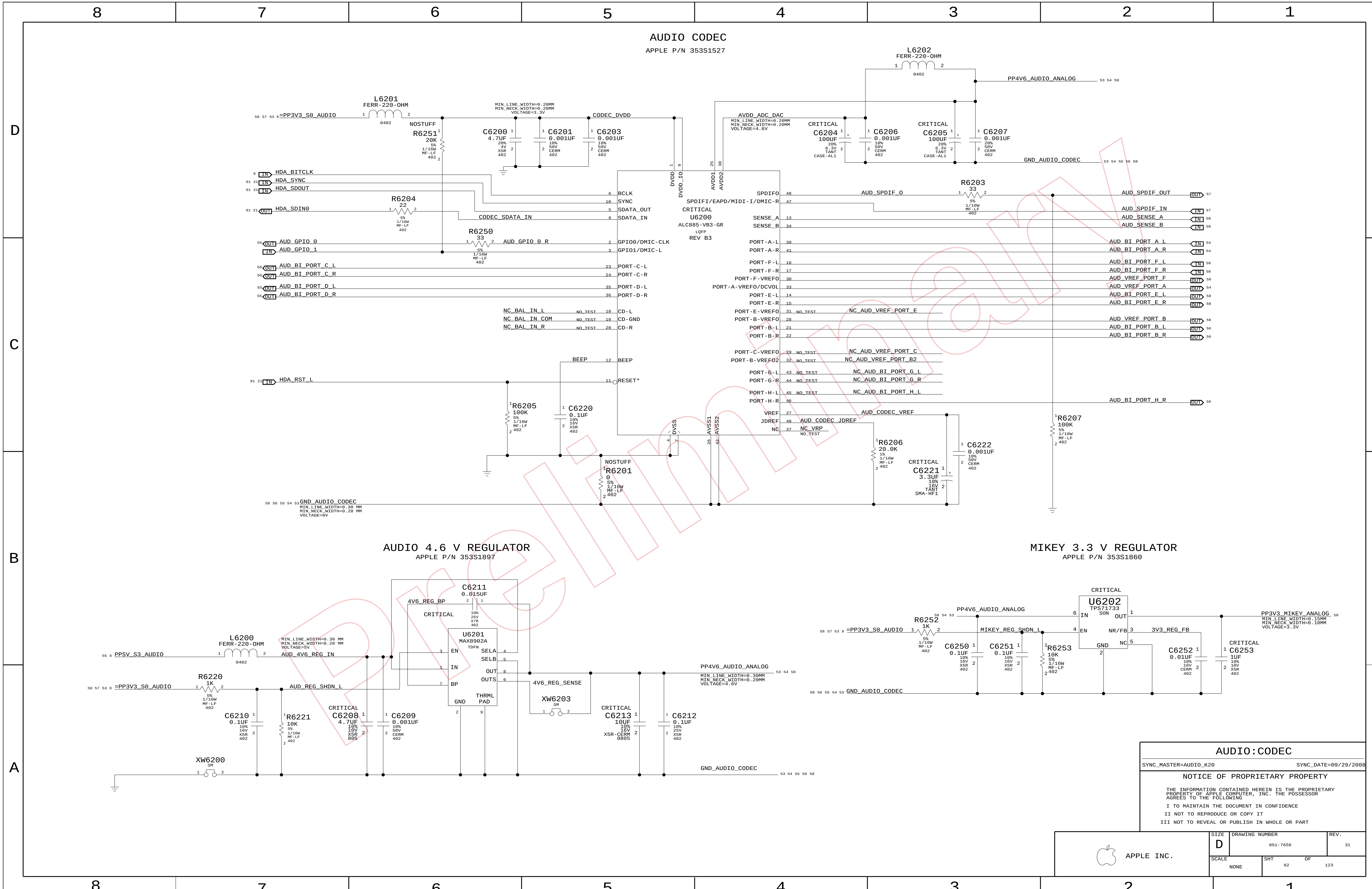
SPI ROM

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	61	123



AUDIO:CODEC

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

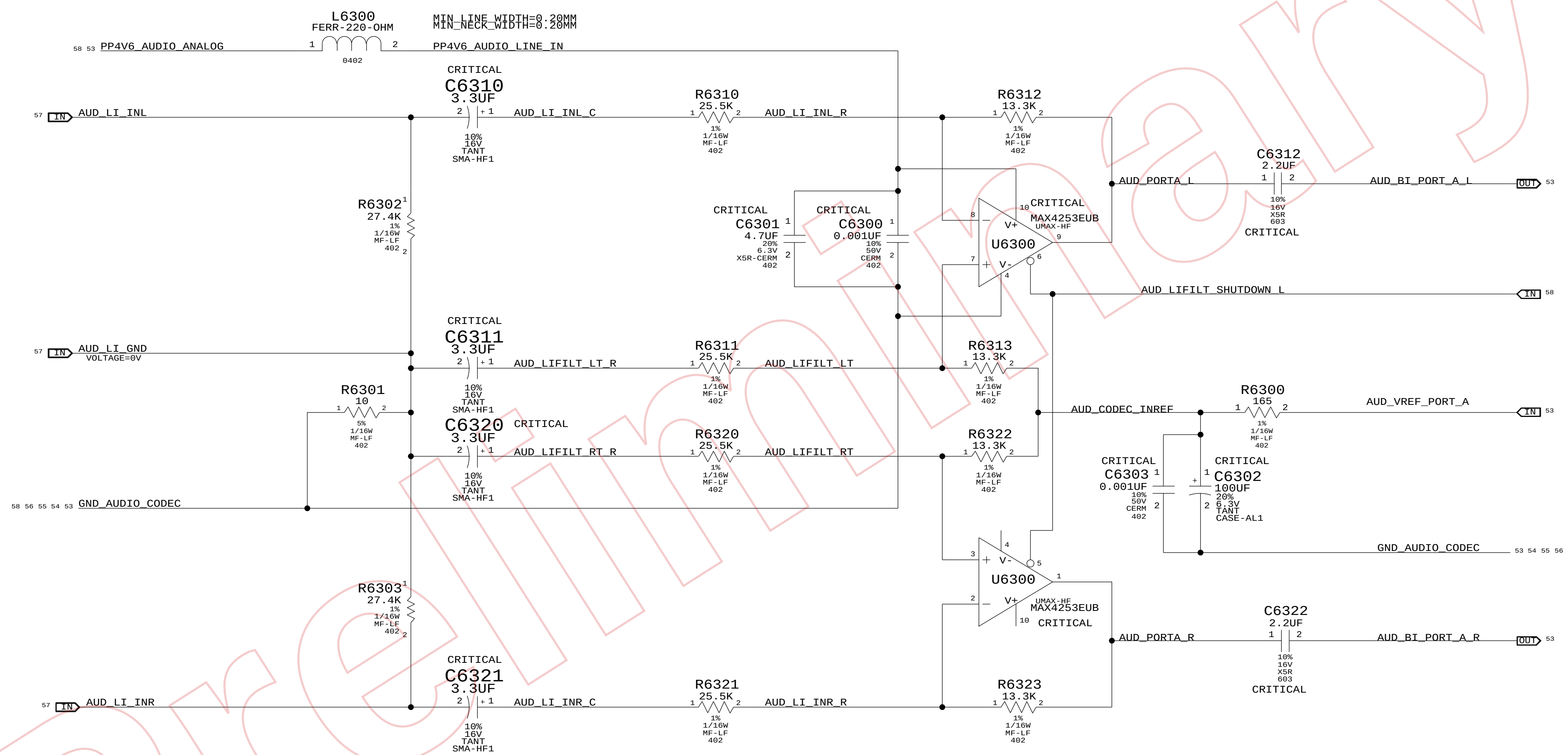
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 62	OF 123

Pseudo-Diff Line-In Filter

GAIN = -5.4 DB AV = 0.52

FC = 1.89 HZ



AUDIO: LINE IN

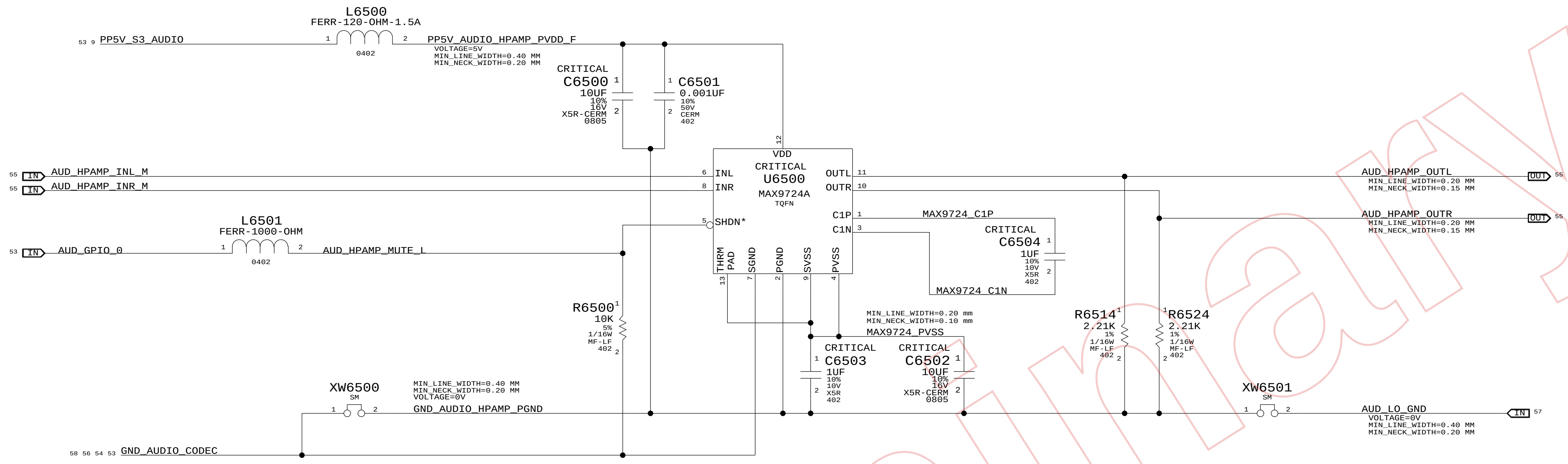
SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 63	OF 123

Headphone Amplifier (MAX9724A)

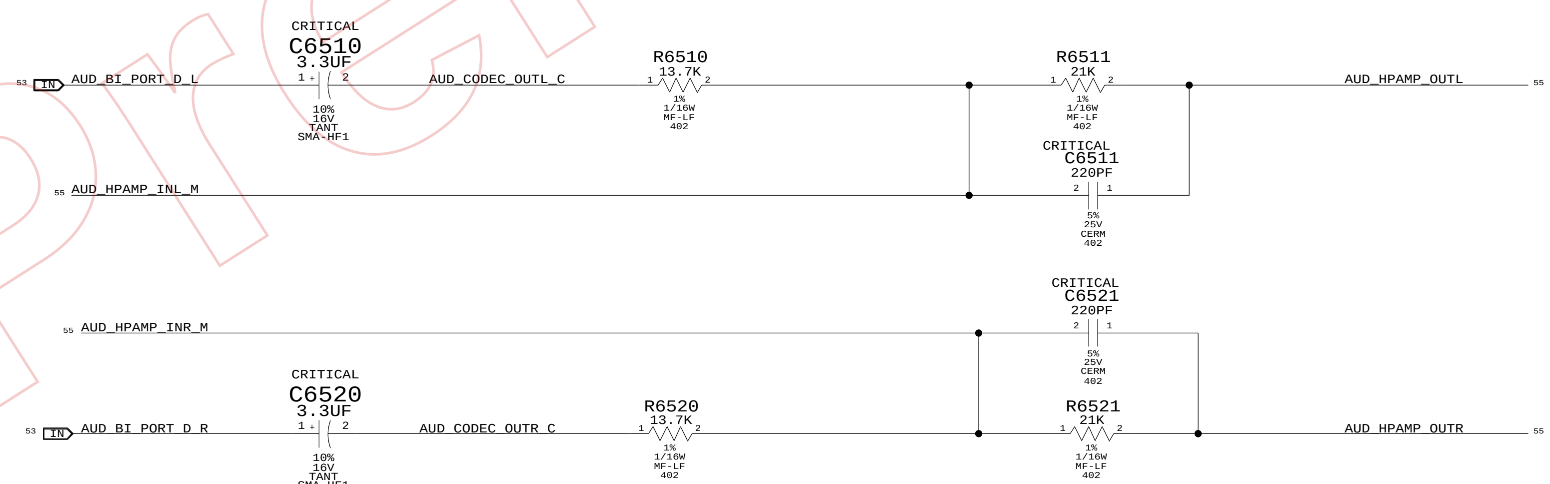
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

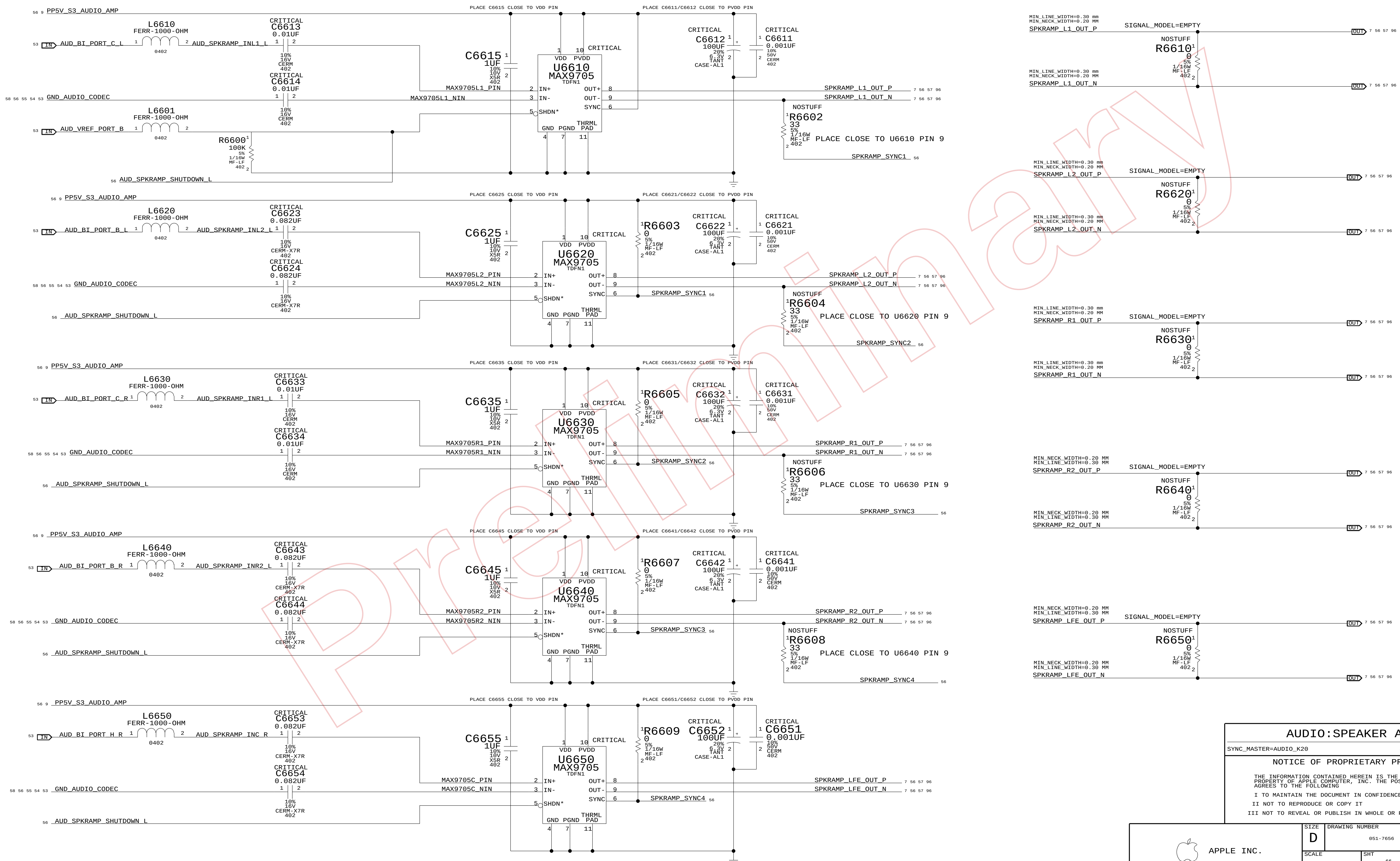
SCALE	SHT	OF
NONE	65	123

4X MONO SPEAKER AMPLIFIERS (MAX9705)

APN: 353S1595
GAIN = 12 DB

FC (SPEAKERS L1/R1) = ~796 HZ
FC (SPEAKERS L2/R2/LFE) = ~97 HZ

SPEAKER CHECKPOINTS



AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

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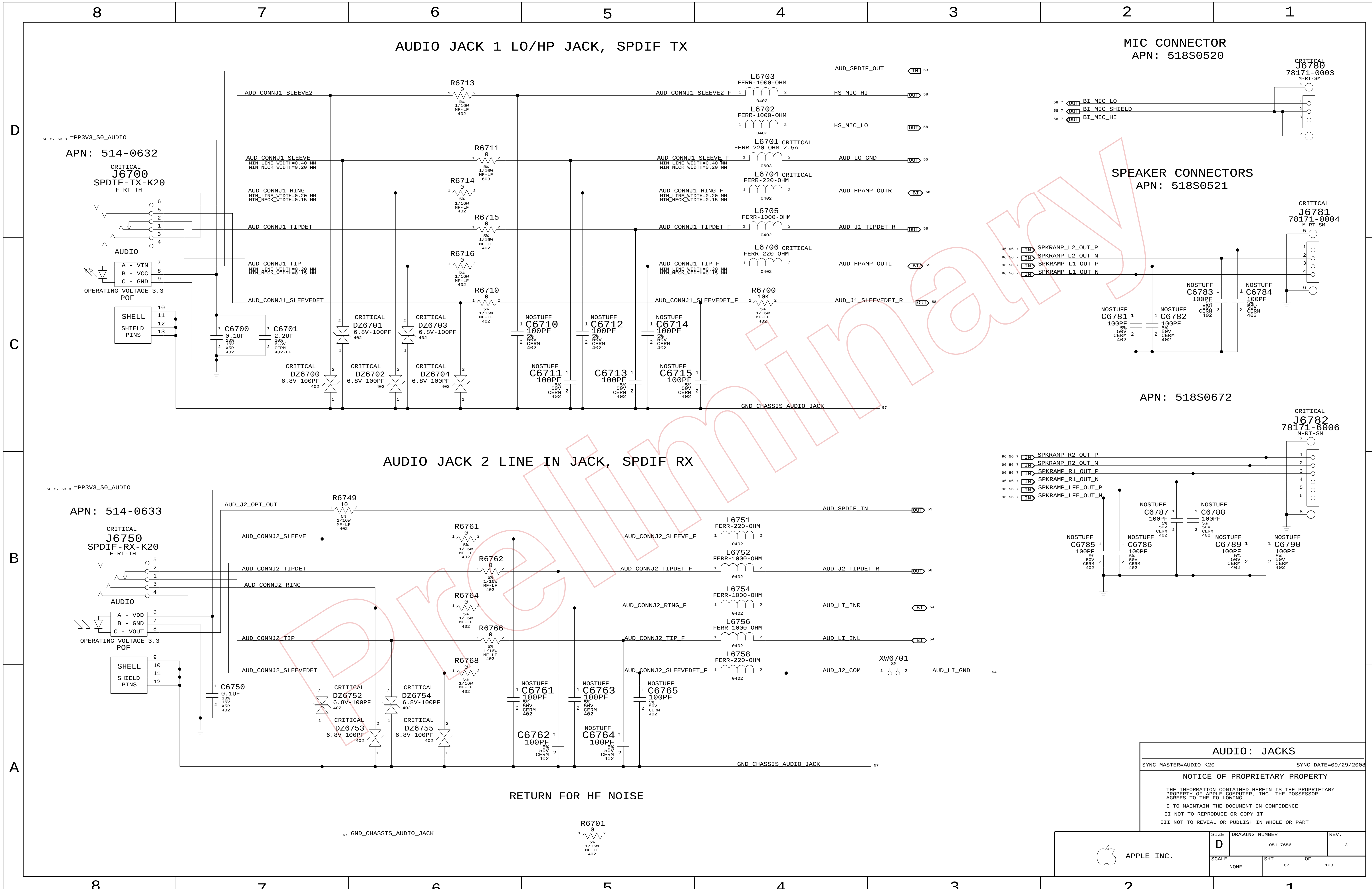
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 66	OF 123



AUDIO JACK 1 LO/HP JACK, SPDIF TX
APN: 514-0632
CRITICAL
J6700
SPDIF-TX-K20
F-RT-TH
AUDIO
A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
=PP3V3_S0_AUDIO
AUD_SPDIF_OUT
AUD_CONNJ1_SLEEVE2
AUD_CONNJ1_SLEEVE2_F
HS_MIC_HI
HS_MIC_LO
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_SLEEVE_F
AUD_LO_GND
AUD_CONNJ1_RING
AUD_CONNJ1_RING_F
AUD_HPAMP_OUTR
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIPDET_F
AUD_J1_TIPDET_R
AUD_CONNJ1_TIP
AUD_CONNJ1_TIP_F
AUD_HPAMP_OUTL
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_SLEEVEDET_F
AUD_J1_SLEEVEDET_R
GND_CHASSIS_AUDIO_JACK
MIC CONNECTOR
APN: 518S0520
CRITICAL
J6780
78171-0003
M-RT-SM
BI_MIC_LO
BI_MIC_SHIELD
BI_MIC_HI
SPEAKER CONNECTORS
APN: 518S0521
CRITICAL
J6781
78171-0004
M-RT-SM
SPKRAMP_L2_OUT_P
SPKRAMP_L2_OUT_N
SPKRAMP_L1_OUT_P
SPKRAMP_L1_OUT_N
APN: 518S0672
CRITICAL
J6782
78171-6006
M-RT-SM
SPKRAMP_R2_OUT_P
SPKRAMP_R2_OUT_N
SPKRAMP_R1_OUT_P
SPKRAMP_R1_OUT_N
SPKRAMP_LFE_OUT_P
SPKRAMP_LFE_OUT_N
AUDIO JACK 2 LINE IN JACK, SPDIF RX
APN: 514-0633
CRITICAL
J6750
SPDIF-RX-K20
F-RT-TH
AUDIO
A - VDD
B - GND
C - VOUT
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
AUD_J2_OPT_OUT
AUD_SPDIF_IN
AUD_CONNJ2_SLEEVE
AUD_CONNJ2_SLEEVE_F
AUD_CONNJ2_TIPDET
AUD_CONNJ2_TIPDET_F
AUD_J2_TIPDET_R
AUD_CONNJ2_RING
AUD_CONNJ2_RING_F
AUD_LI_INR
AUD_CONNJ2_TIP
AUD_CONNJ2_TIP_F
AUD_LI_INL
AUD_CONNJ2_SLEEVEDET
AUD_CONNJ2_SLEEVEDET_F
AUD_J2_COM
XW6701
AUD_LI_GND
RETURN FOR HF NOISE
GND_CHASSIS_AUDIO_JACK
R6701
Preliminary
AUDIO: JACKS
SYNC_MASTER=AUDIO_K20
SYNC_DATE=09/29/2008
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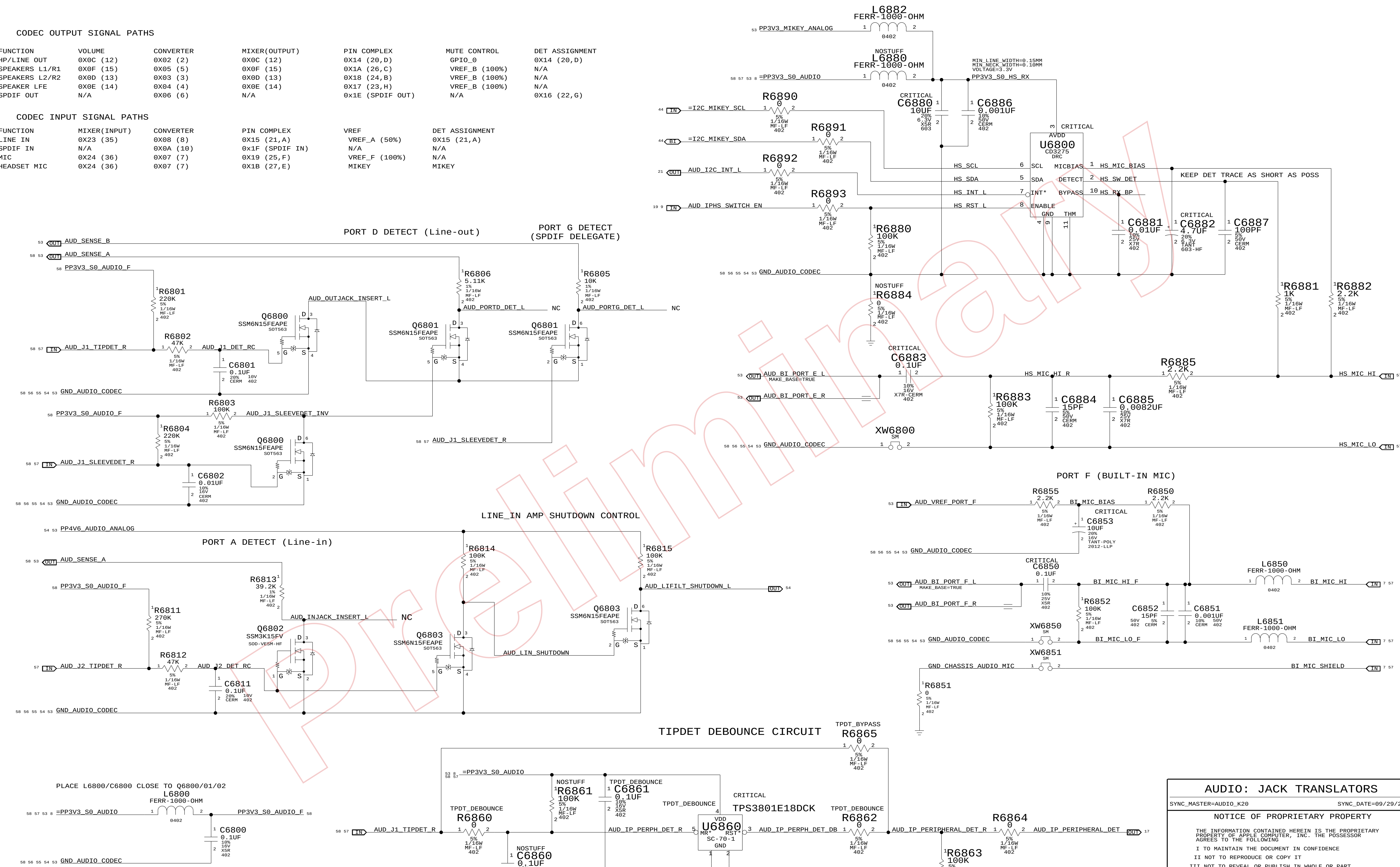
APPLE INC.
SIZE D
DRAWING NUMBER 051-7656
REV. 31
SCALE NONE
SHT 67 OF 123

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SPEAKERS L1/R1	0X0F (15)	0X05 (5)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPEAKERS L2/R2	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SPEAKER LFE	0X0E (14)	0X04 (4)	0X0E (14)	0X17 (23,H)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)	N/A	0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0X1F (SPDIF IN)	N/A	N/A
MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY



AUDIO: JACK TRANSLATORS

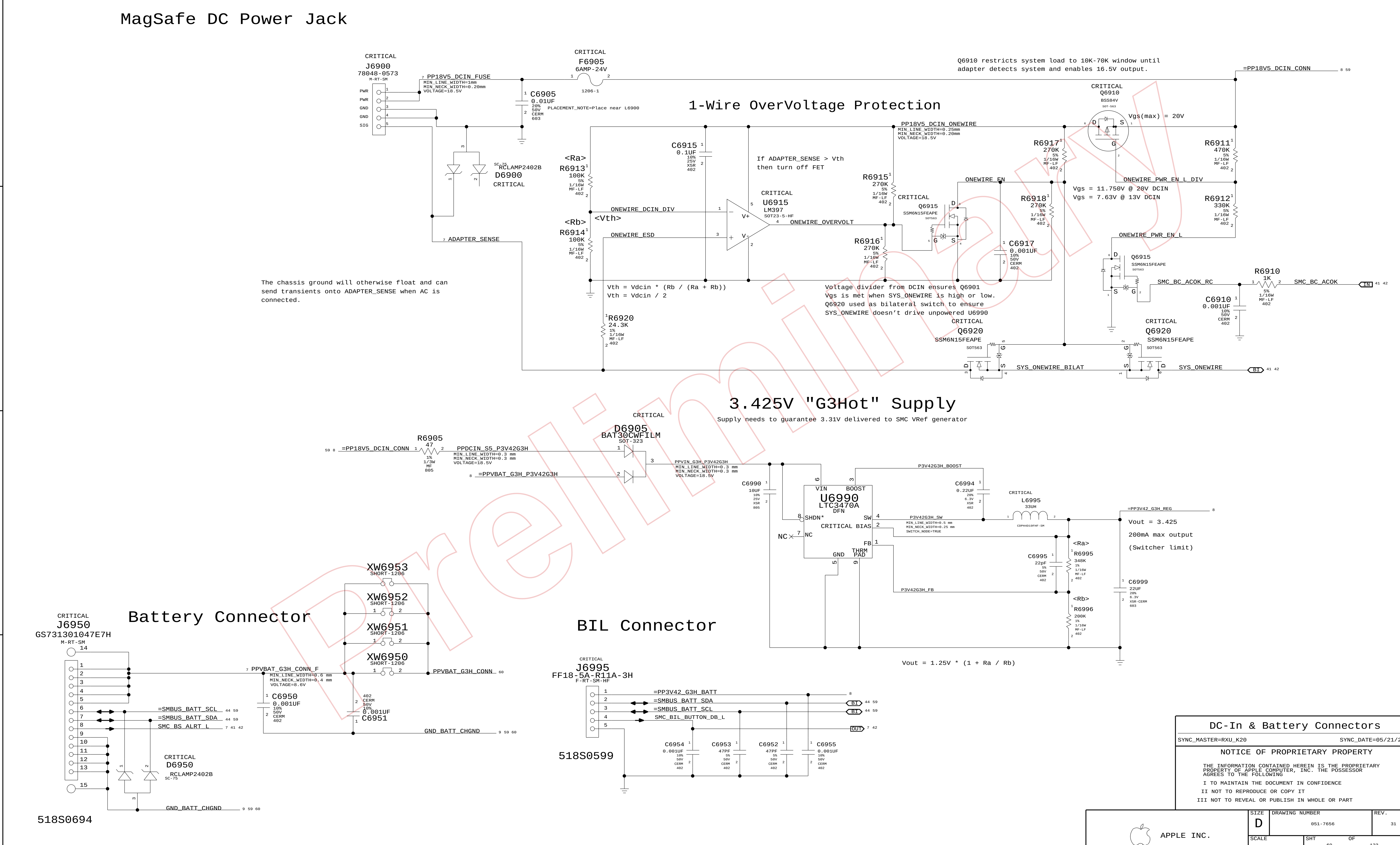
SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	68	123



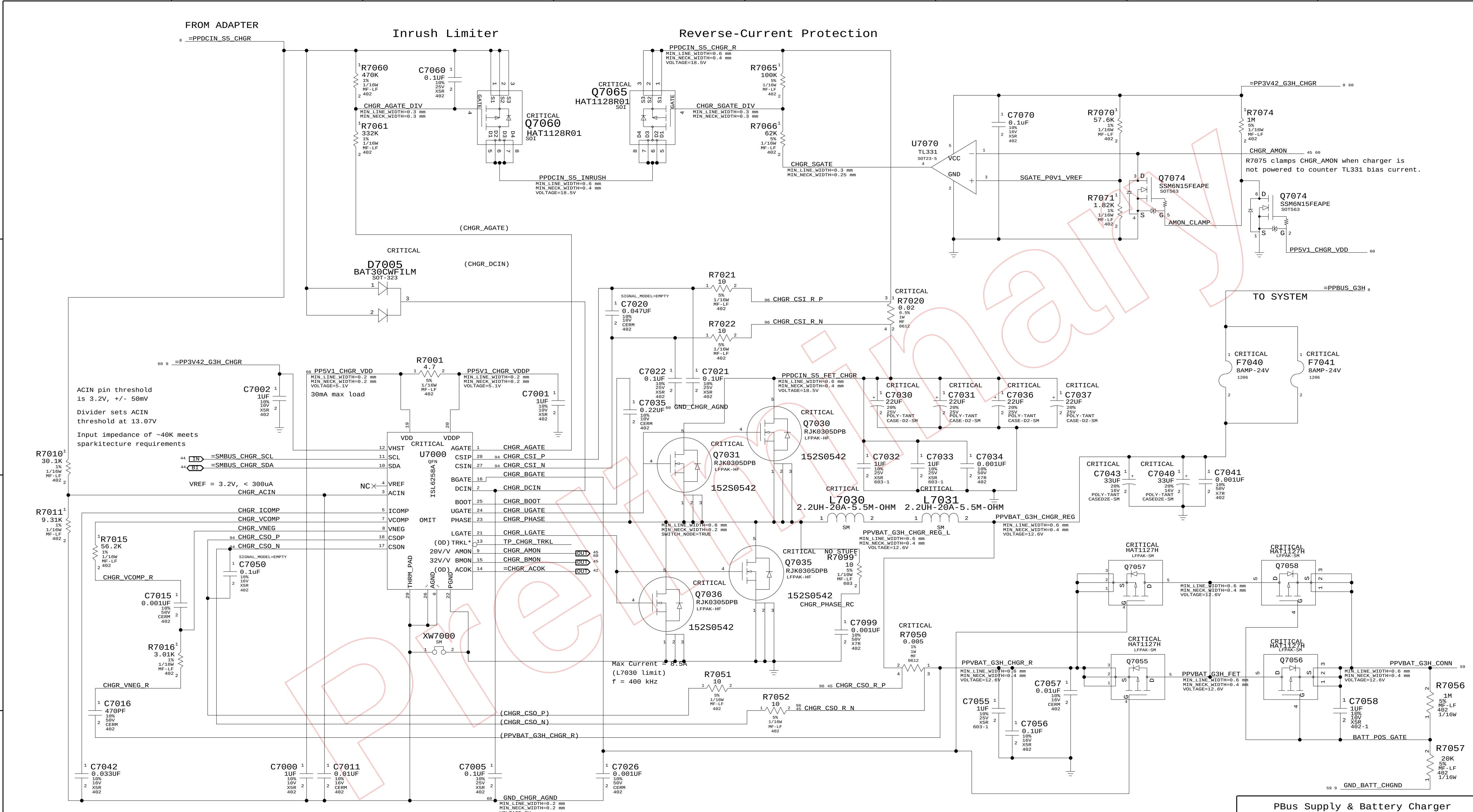
DC-In & Battery Connectors

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 69	OF 123



M99 differences from last sync on 12/02/07 to T18 MLB:
1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

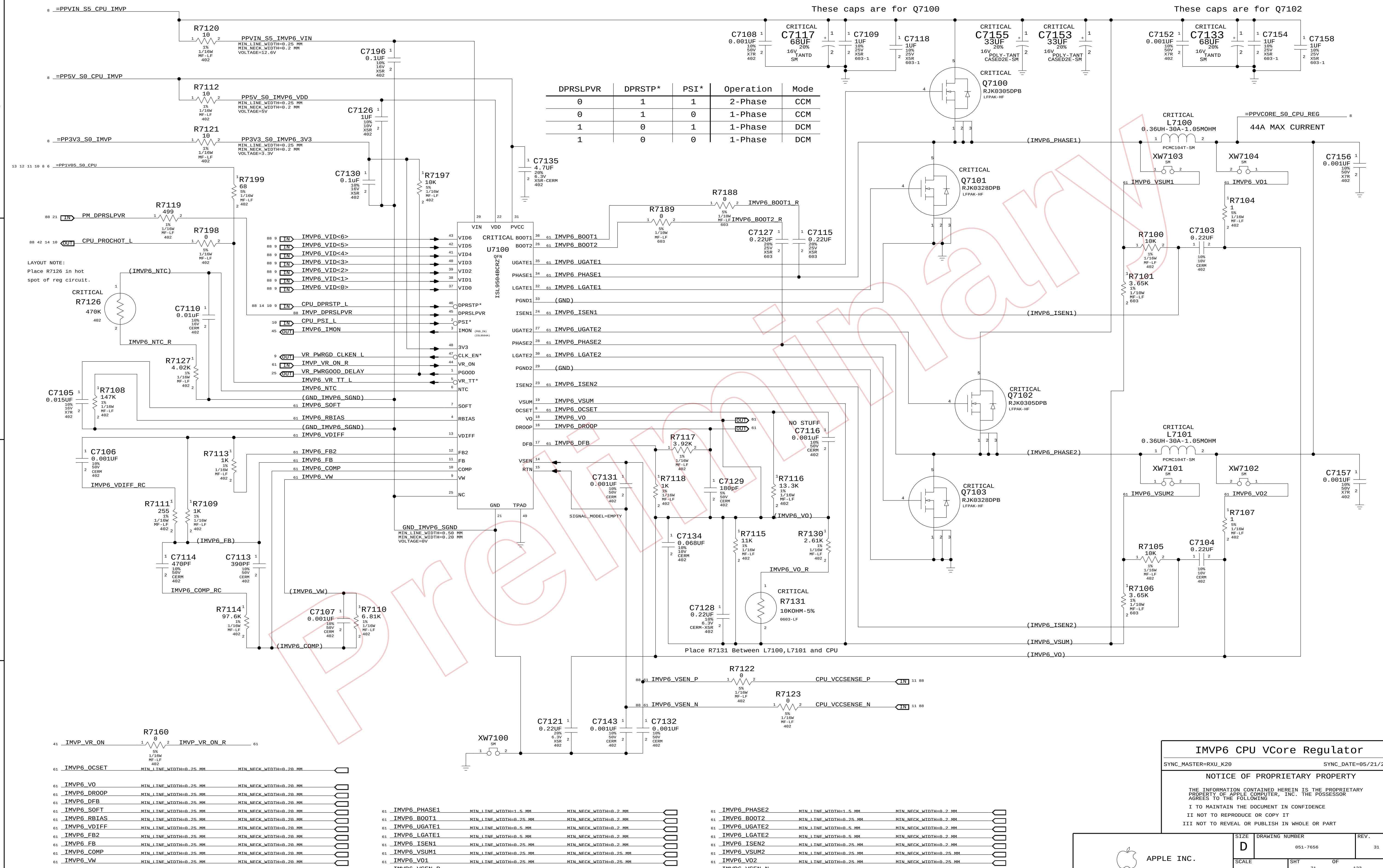
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1938	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

PBus Supply & Battery Charger

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 70	OF 123



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

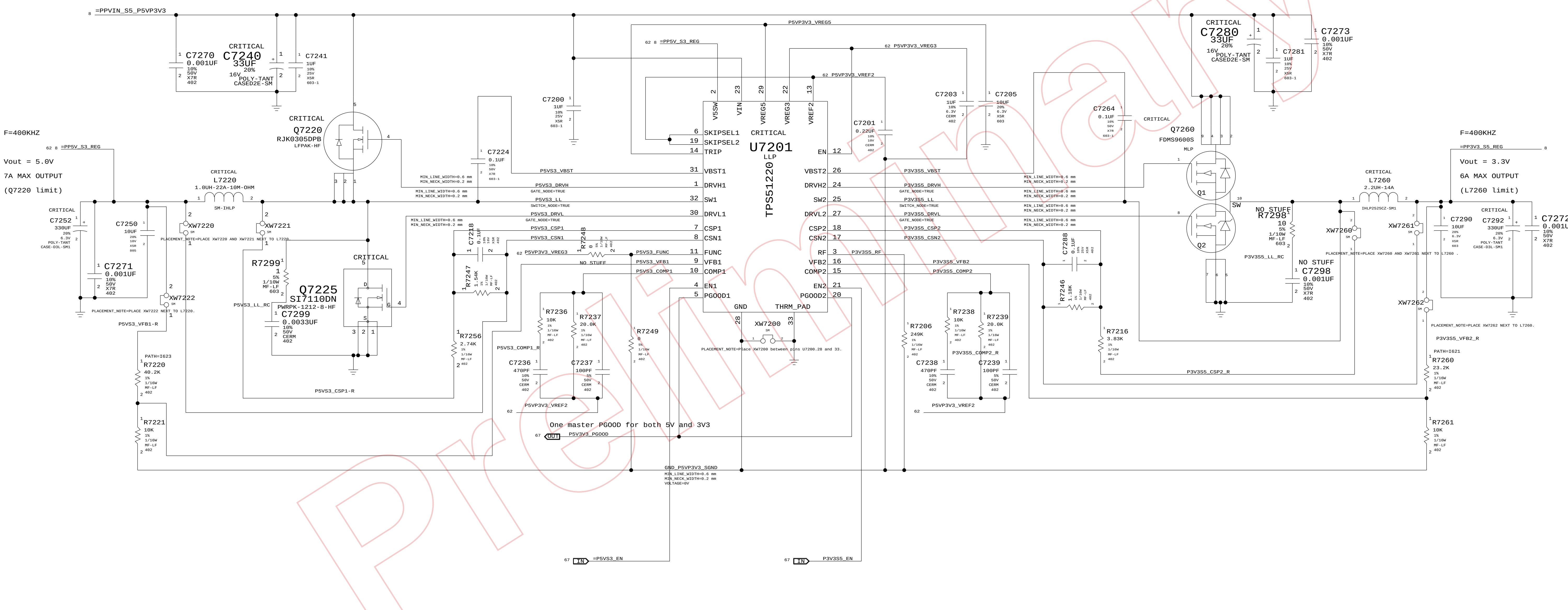
IMVP6 CPU VCore Regulator

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-7656 | REV. 31

SCALE NONE | SHT 71 OF 123



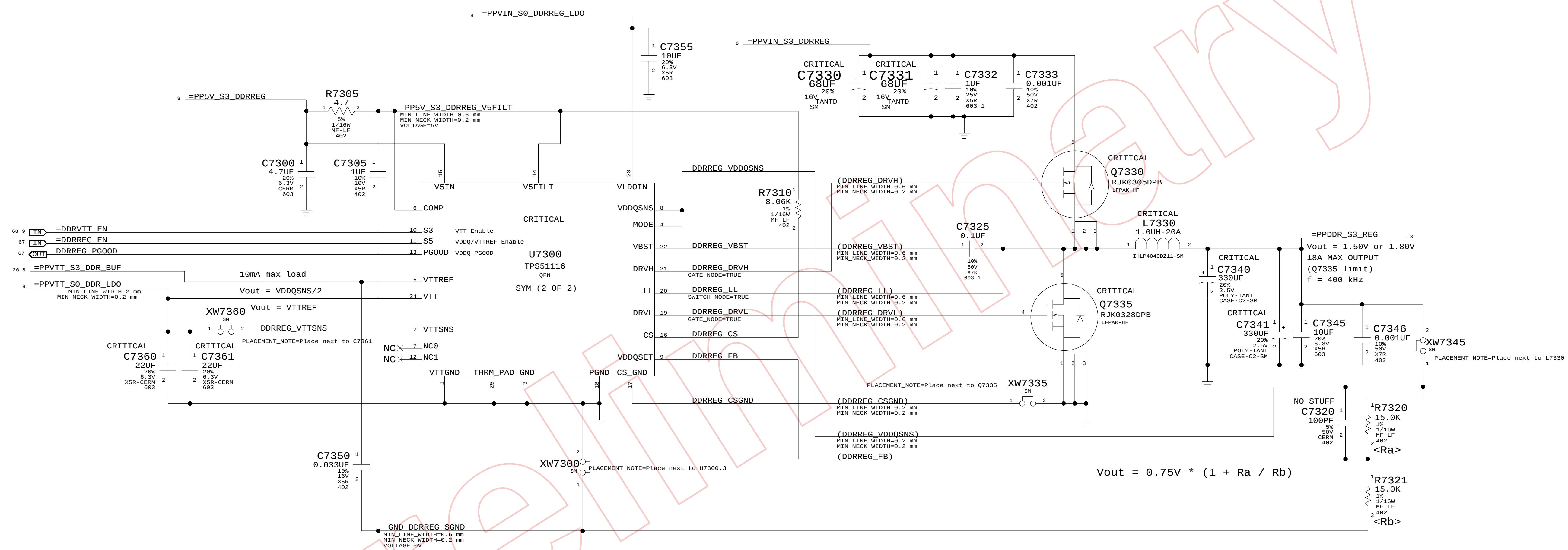
5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 72	OF 123



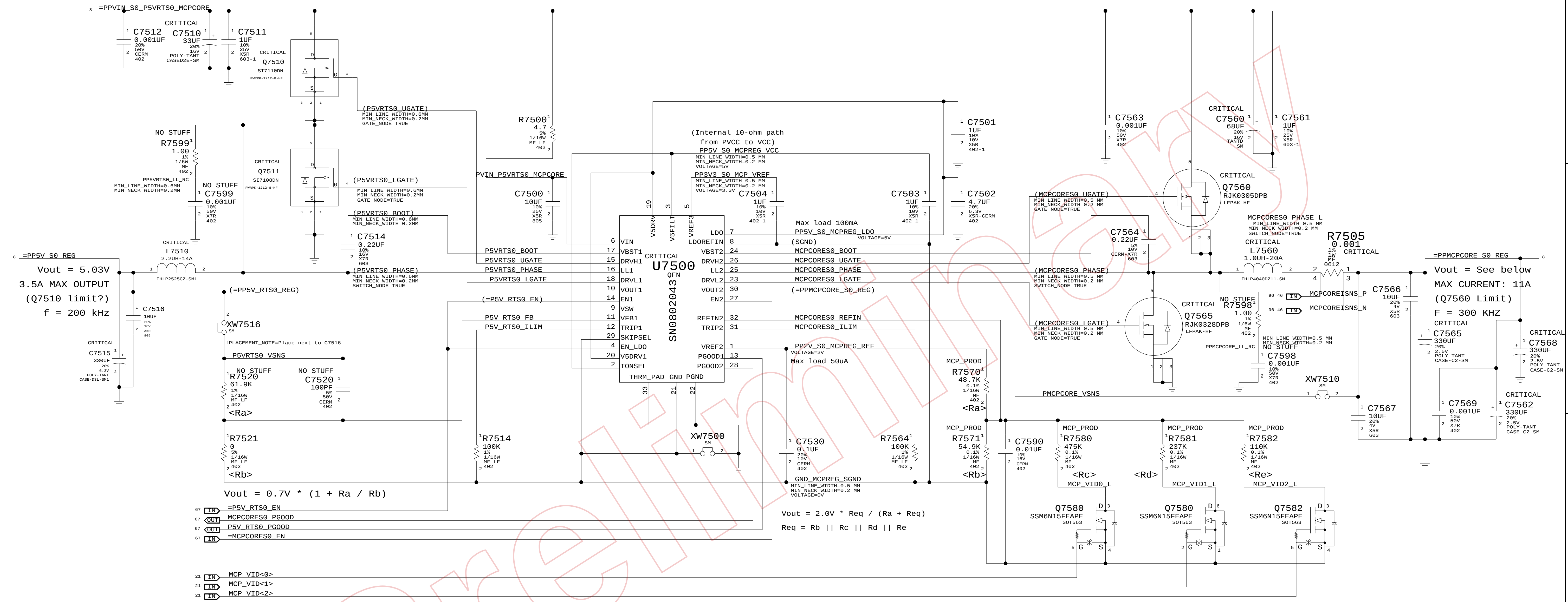
1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	73	123



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

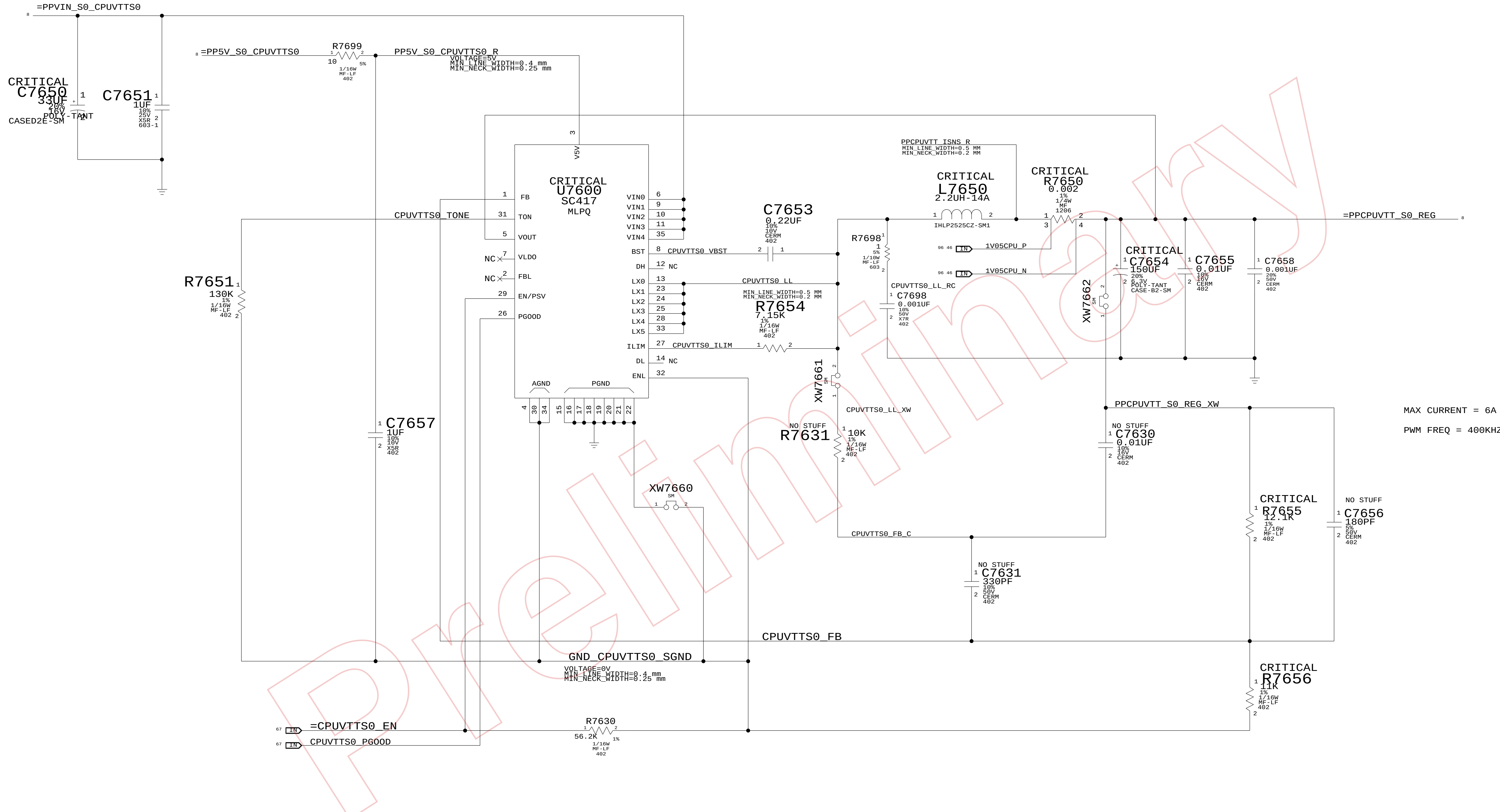
5V_S0 / MCP CORE REGULATOR

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-7656 | REV. 31

SCALE NONE | SHT 75 OF 123



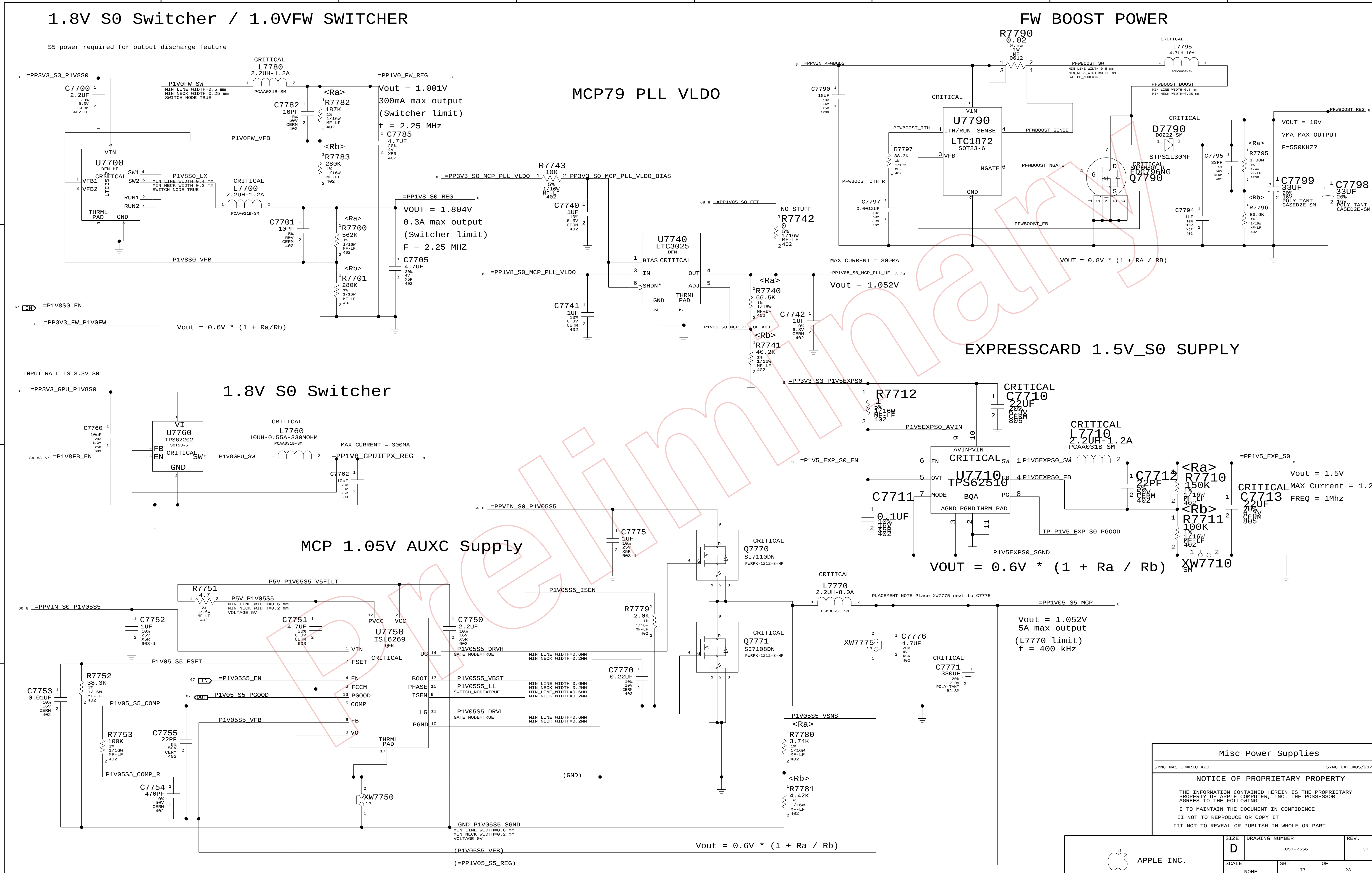
CPU VTT Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	76	123



Misc Power Supplies

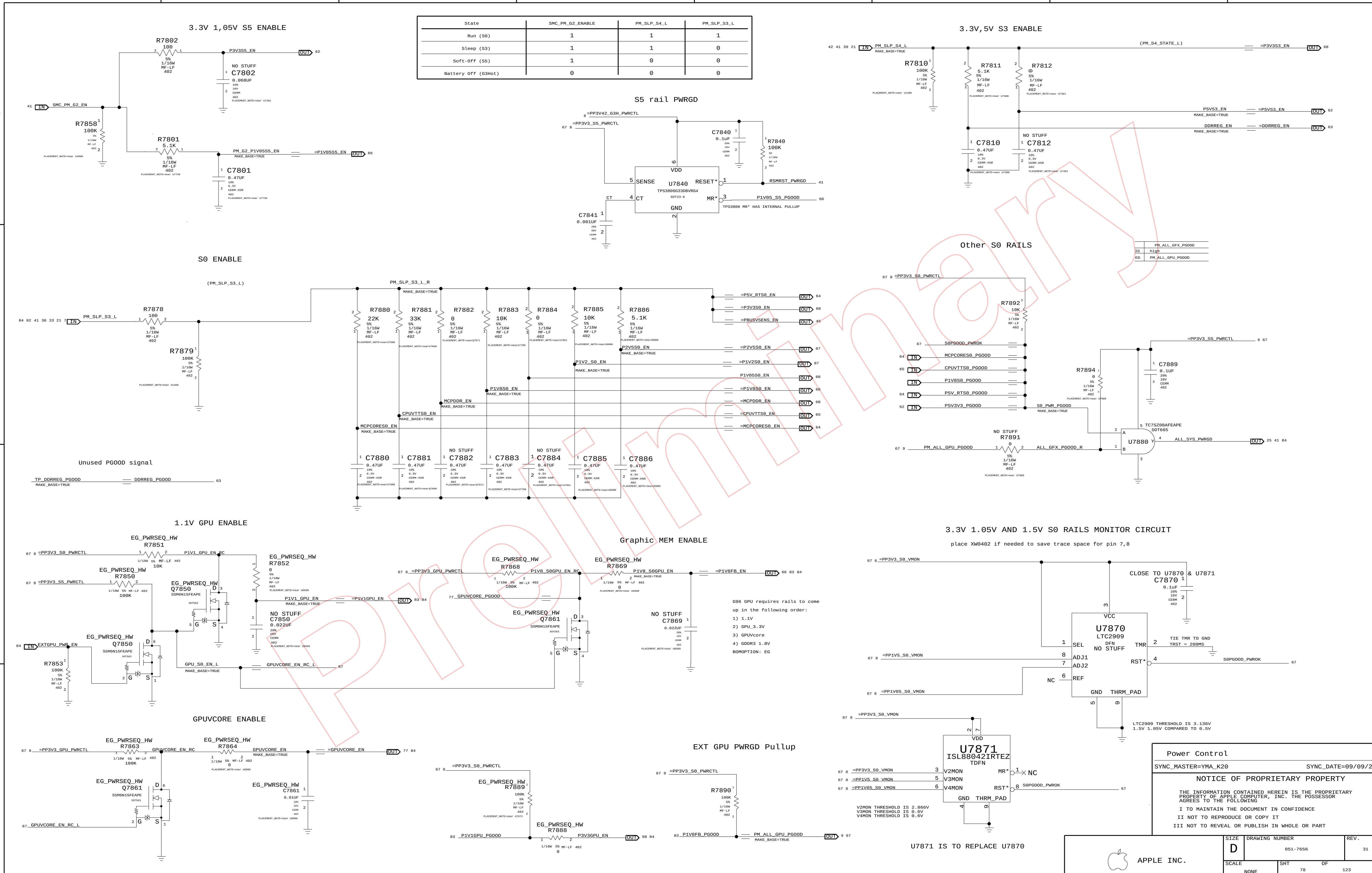
SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	77	123



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Power Control

SYNC_MASTER=YMA_K20 SYNC_DATE=09/09/2008

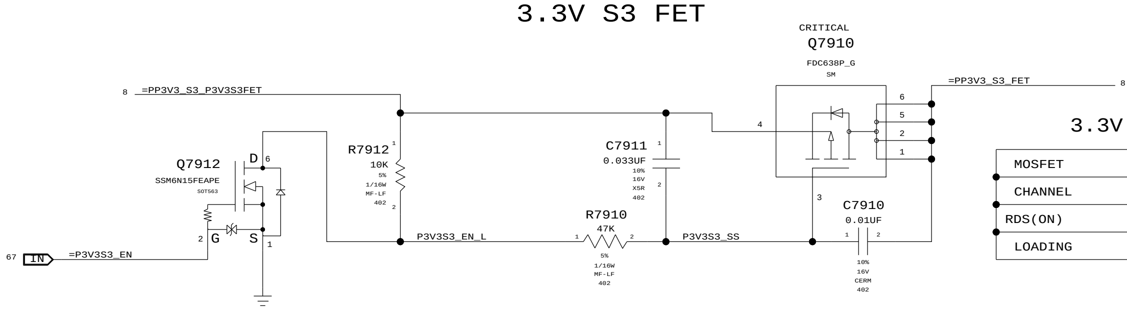
NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	78	123

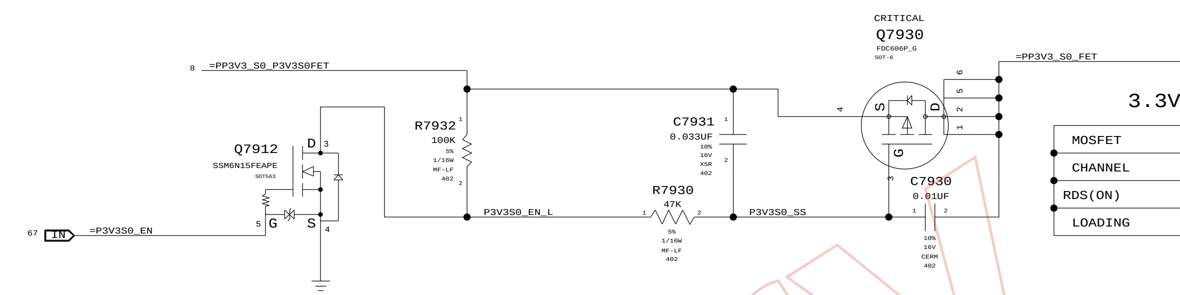
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

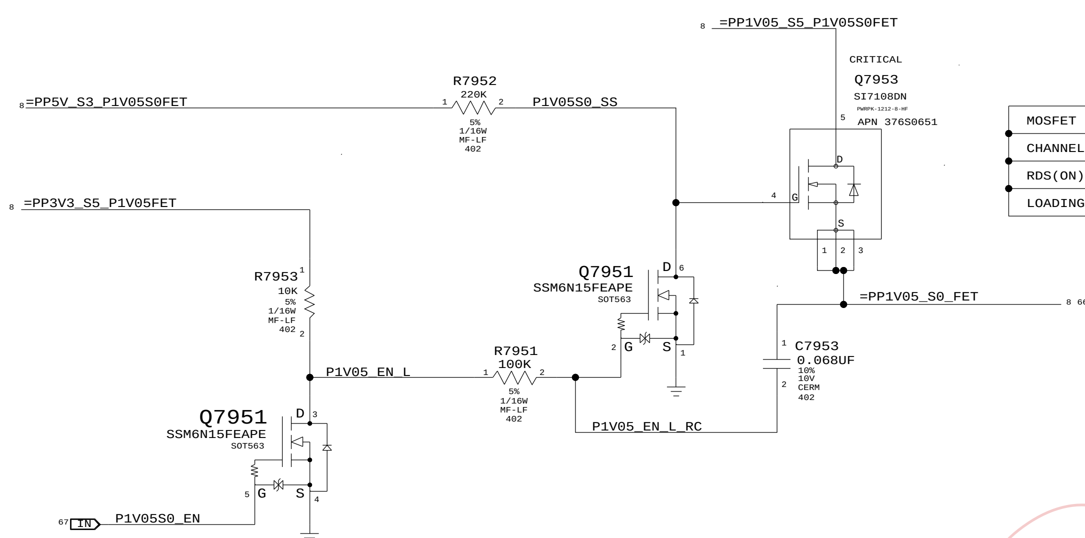
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

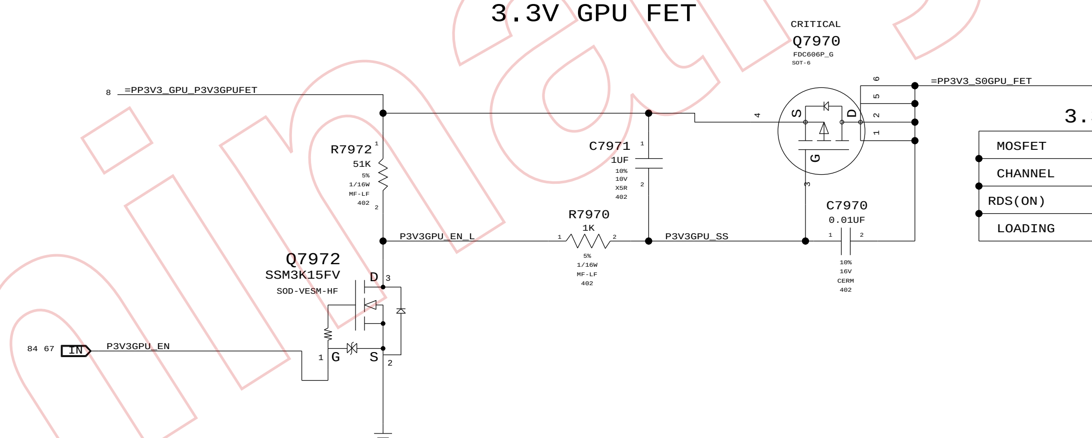
1.05V S0 FET



1.05V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.1 A (EDP)

3.3V GPU FET



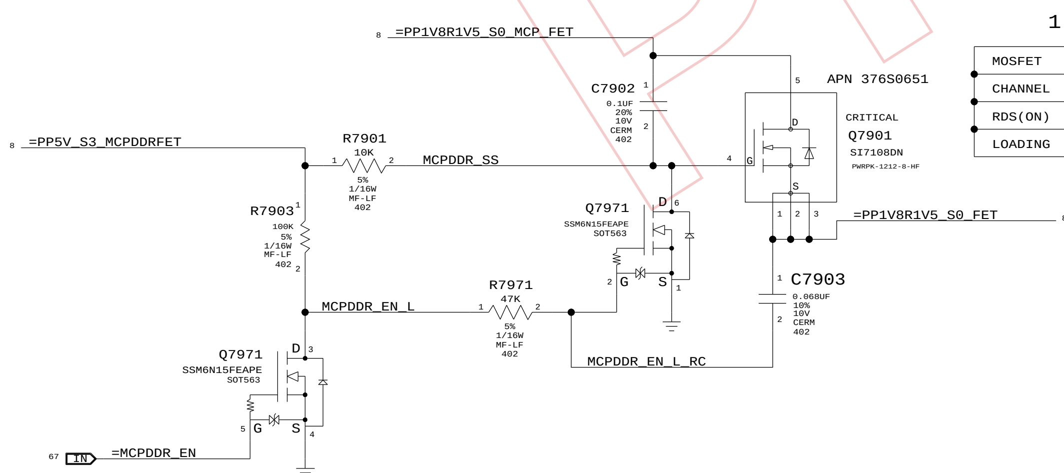
3.3V GPU FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)

MCP79 DDR FETs

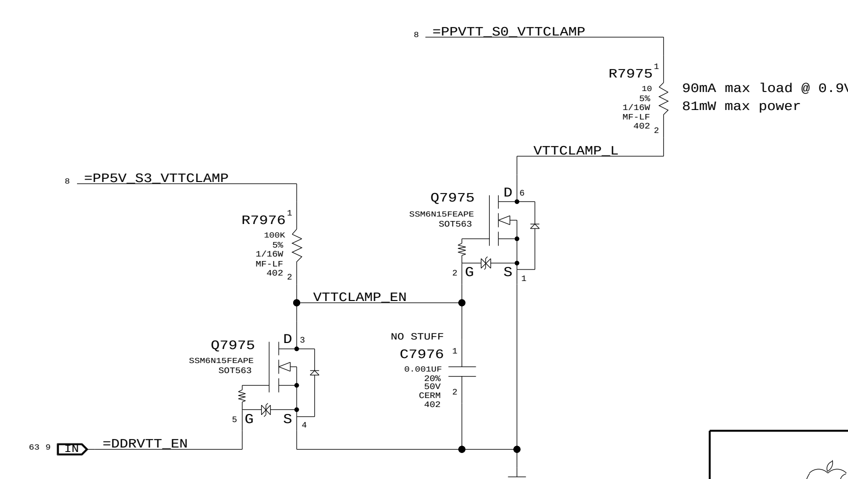
MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.

1.5V S0 FET



1.5V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)



Power FETs

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

APPLE INC.

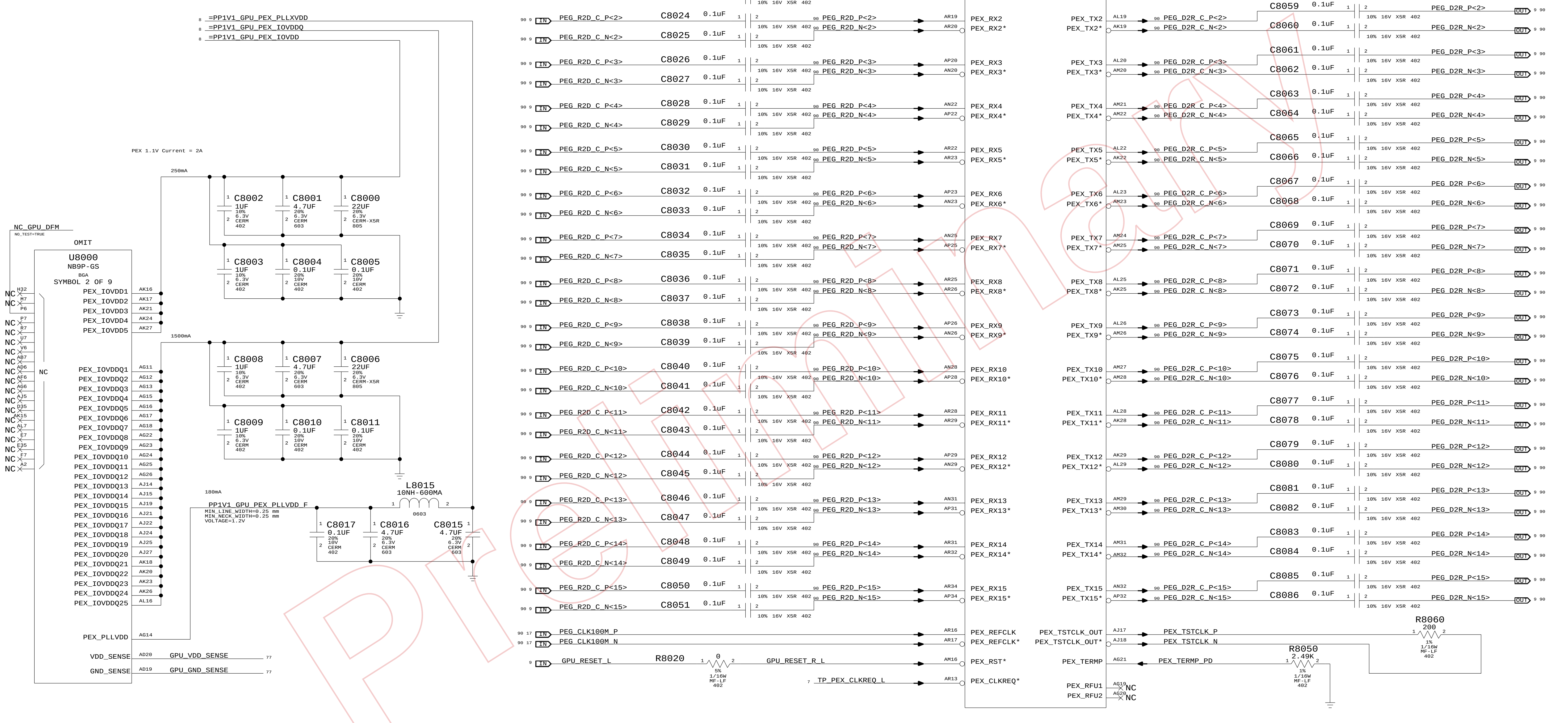
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 79	OF 123

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 PCI-E

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

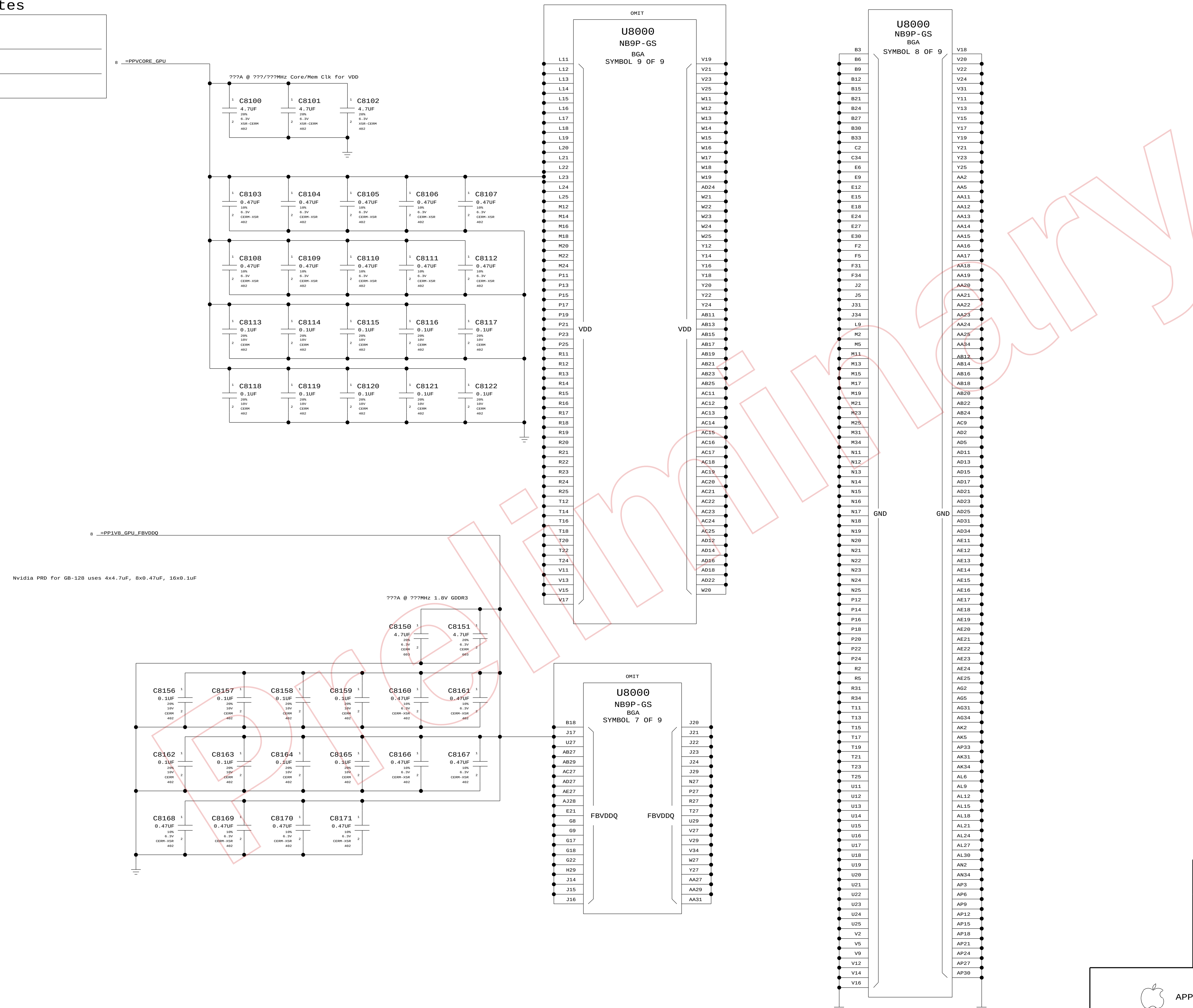
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 80	OF 123

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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APPLE INC.

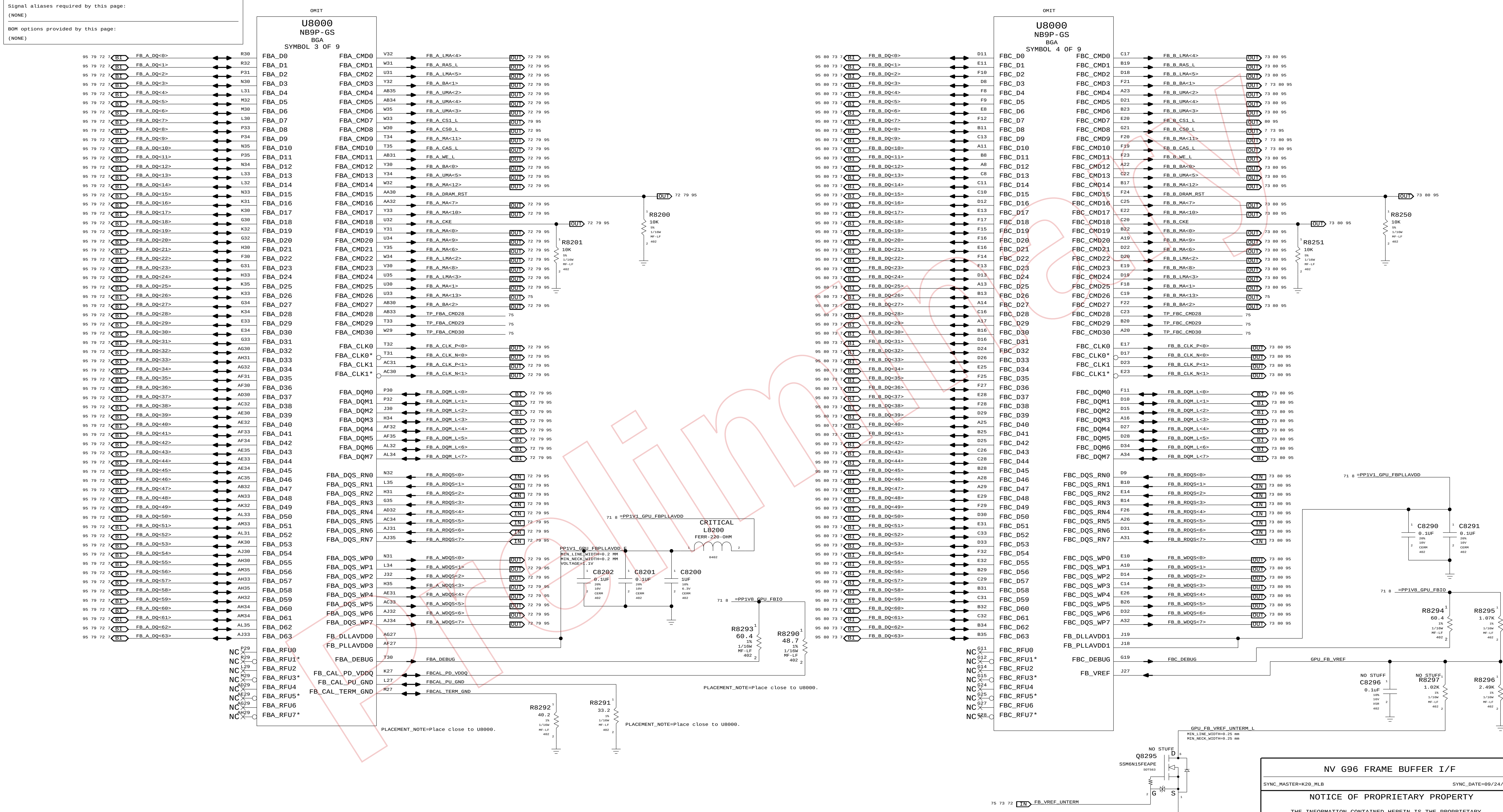
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 81	OF 123

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



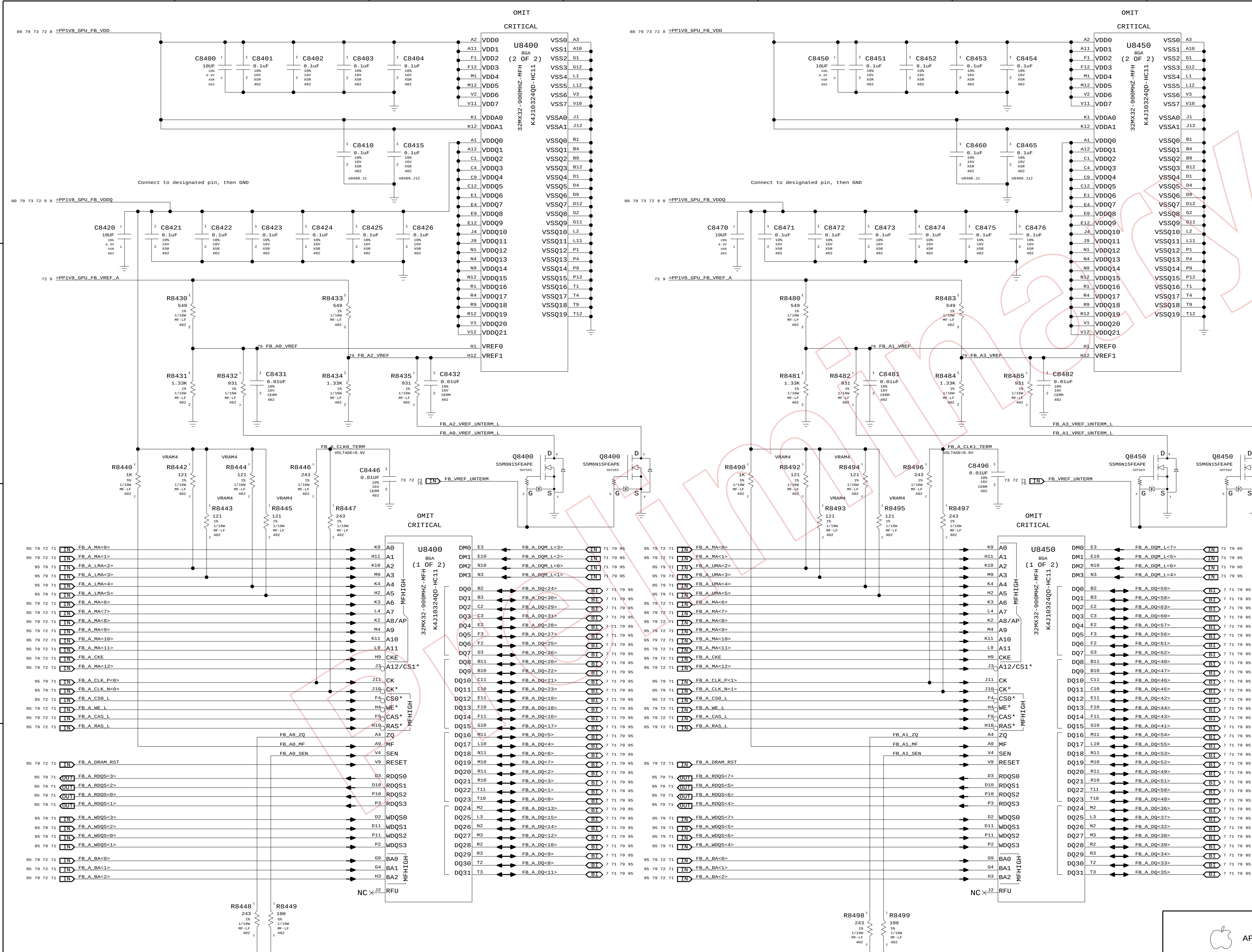
NV G96 FRAME BUFFER I/F

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 82	OF 123



Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

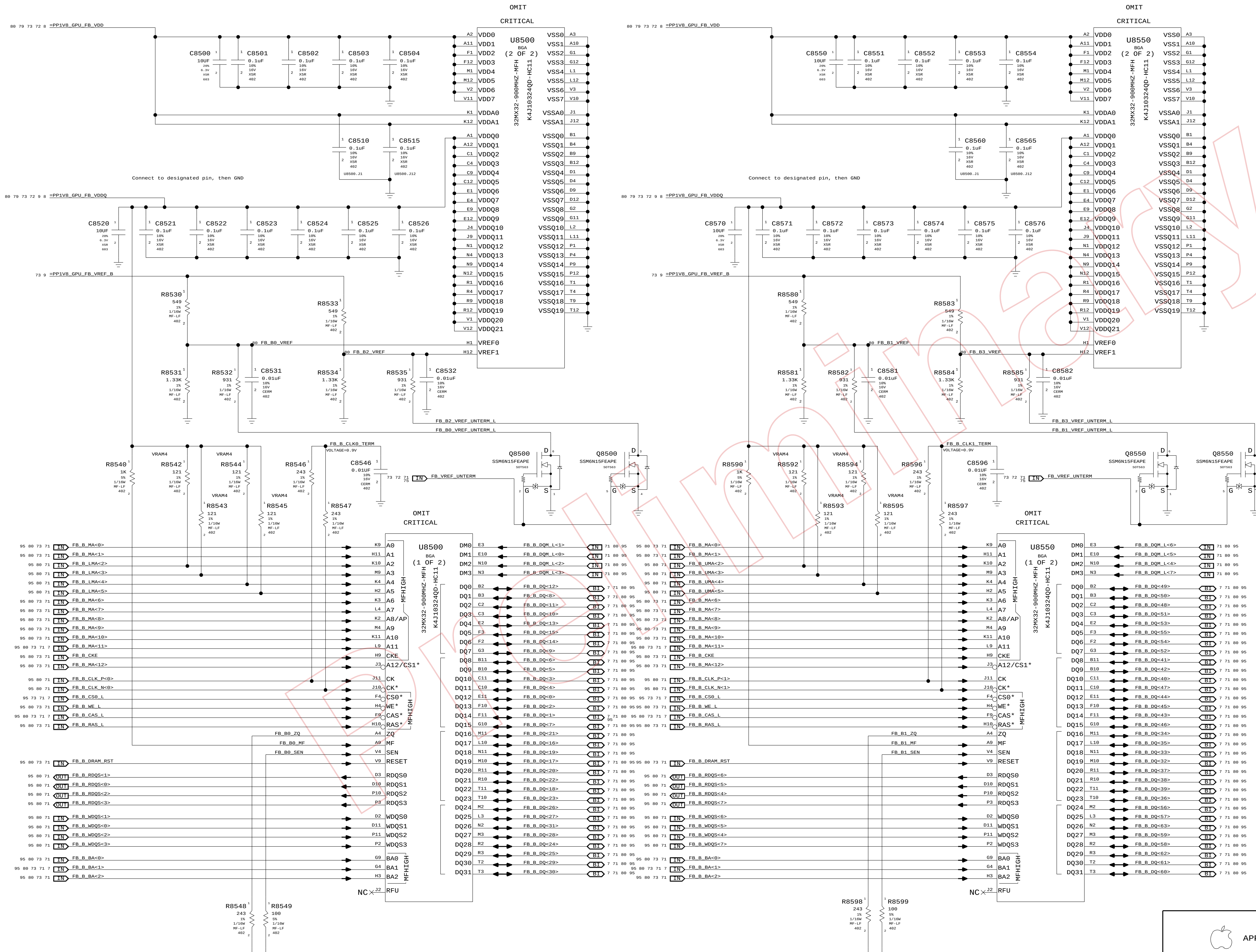
VRAM4

GDDR3 Frame Buffer A (Bottom)

SYNC_MASTER=M98_MLB

SYNC_DATE=04/01/2008

APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHT 84	OF 123



Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM4

GDDR3 Frame Buffer B (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

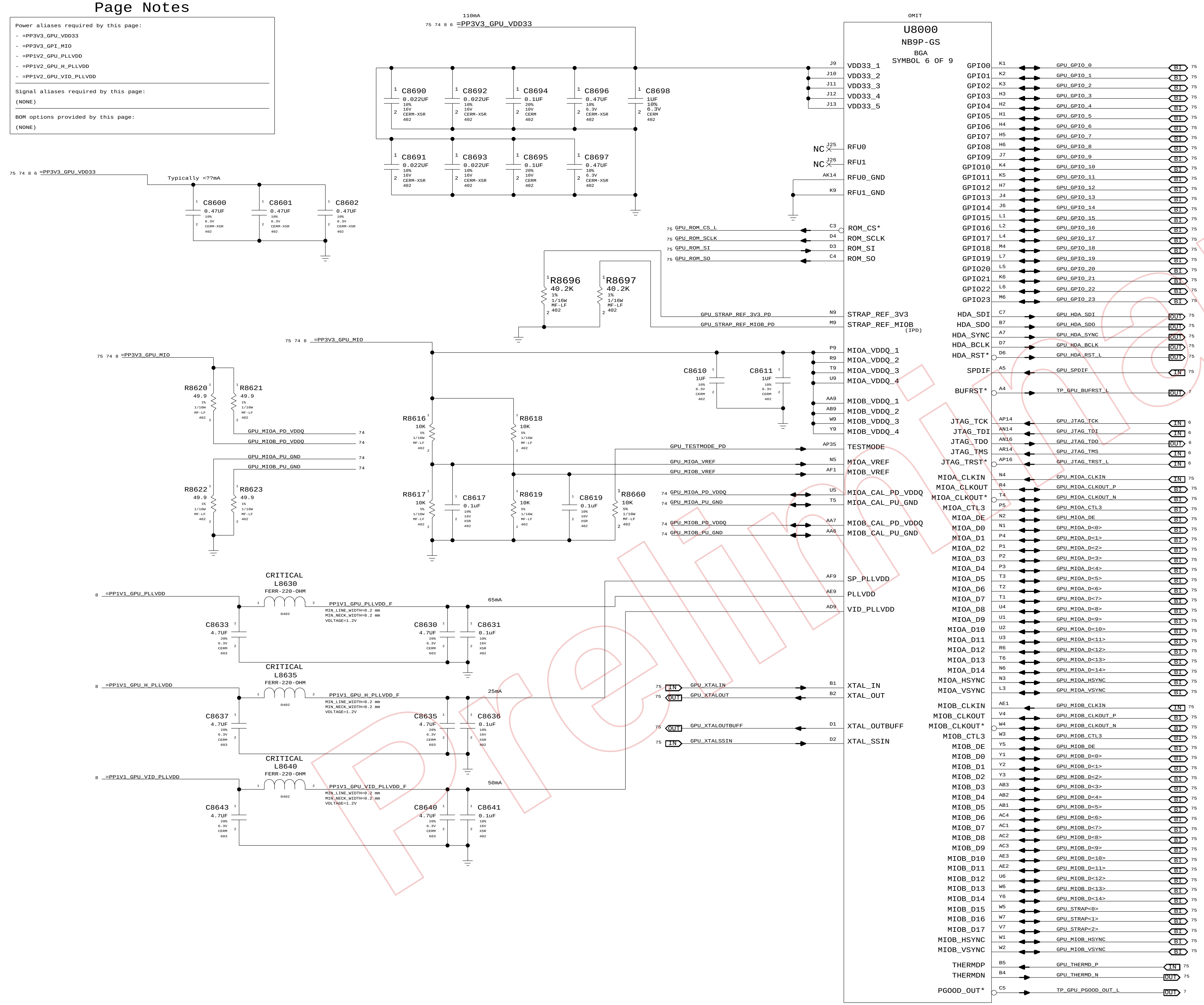
SCALE	SHT	OF
NONE	85	123

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G96 GPIO/MIO/MISC

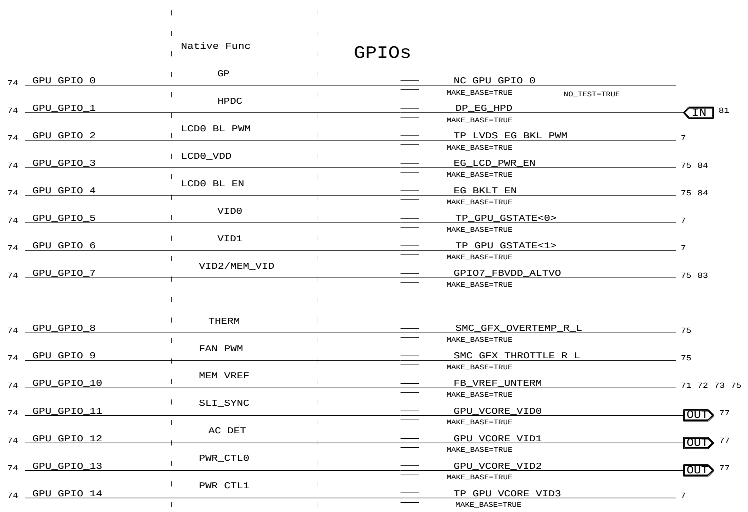
SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

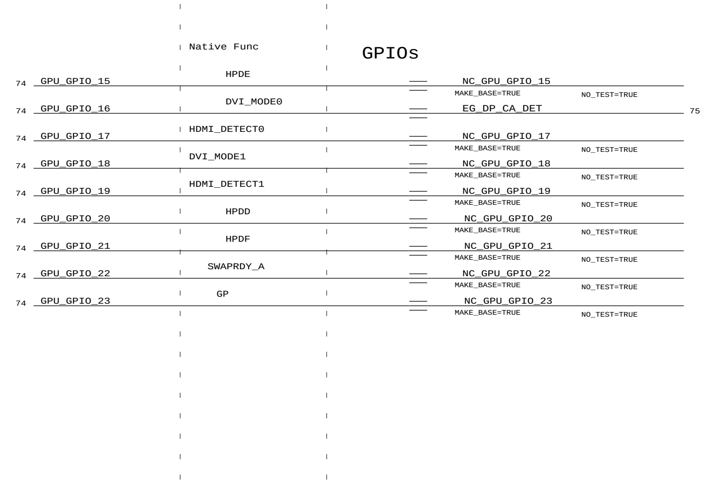
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

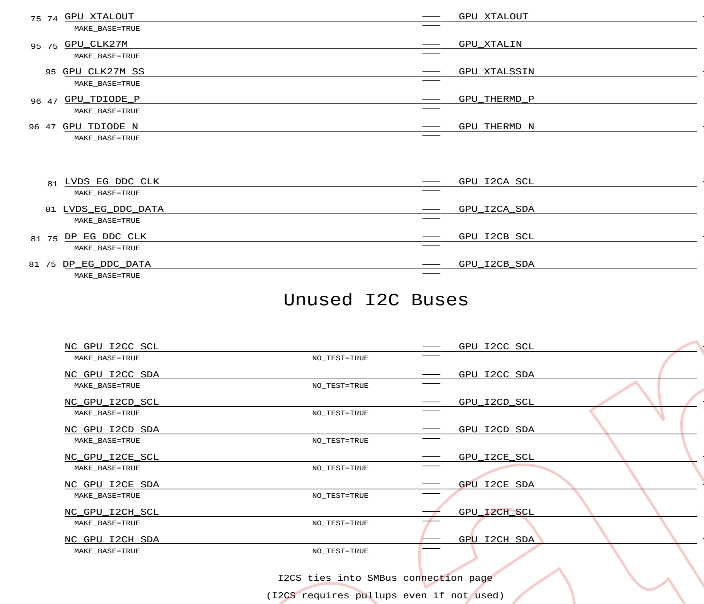
SCALE	SHT	OF
NONE	86	123

GPIOs

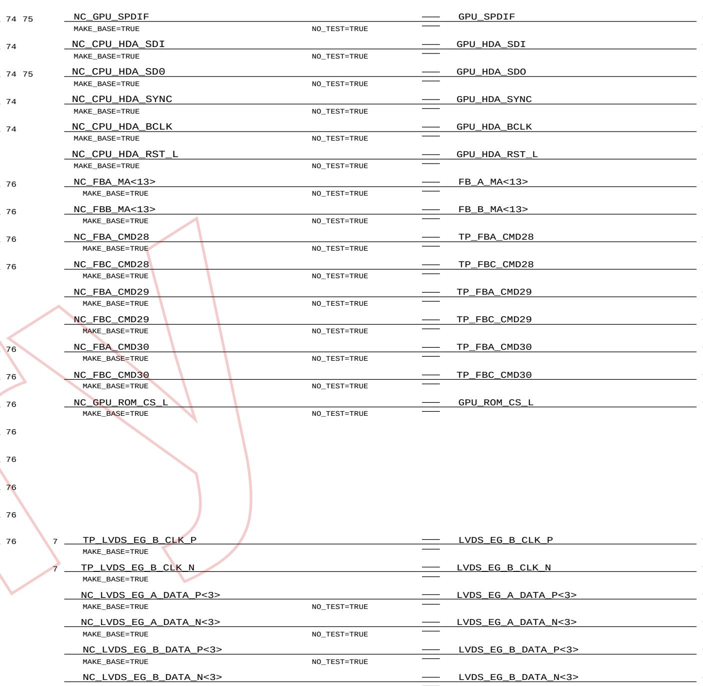




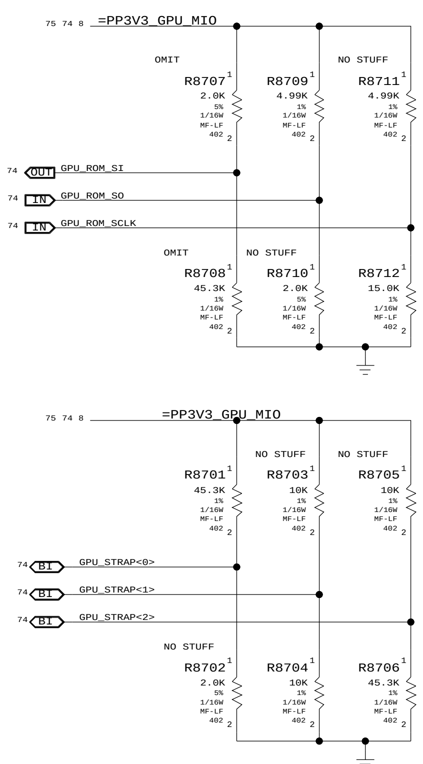
Renamed signals



Unused signals



Config Straps



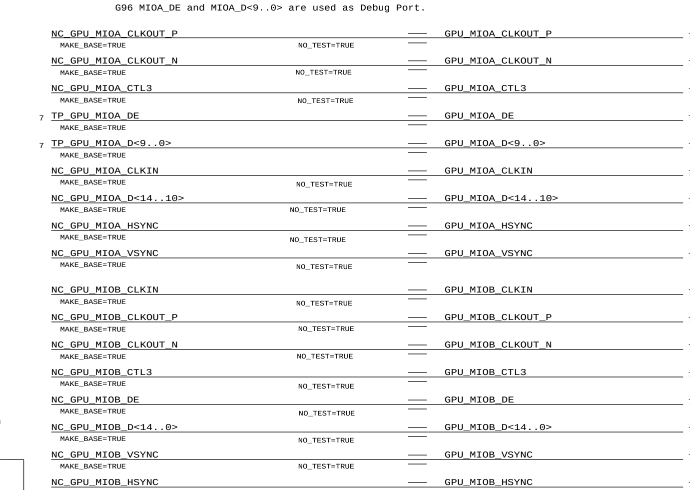
Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap	S1/S2 Bit[3:0]	PU/PD	Rval
0	0000	PD	5k
1	0001	PD	10k
2	0010	PD	15k
3	0011	PD	20k
4	0100	PD	25k
5	0101	PD	30k
6	0110	PD	35k
7	0111	PD	45k

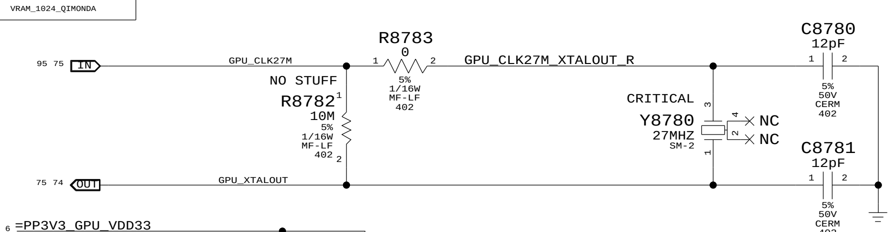
Strap	S1/S2 Bit[3:0]	PU/PD	Rval
8	1000	PU	5k
9	1001	PU	10k
A	1010	PU	15k
B	1011	PU	20k
C	1100	PU	25k
D	1101	PU	30k
E	1110	PU	35k
F	1111	PU	45k

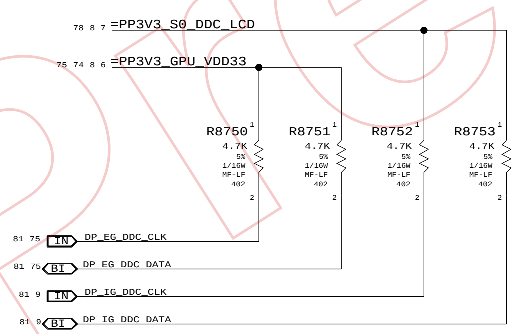
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8707		VRAM_1024_QIMONDA

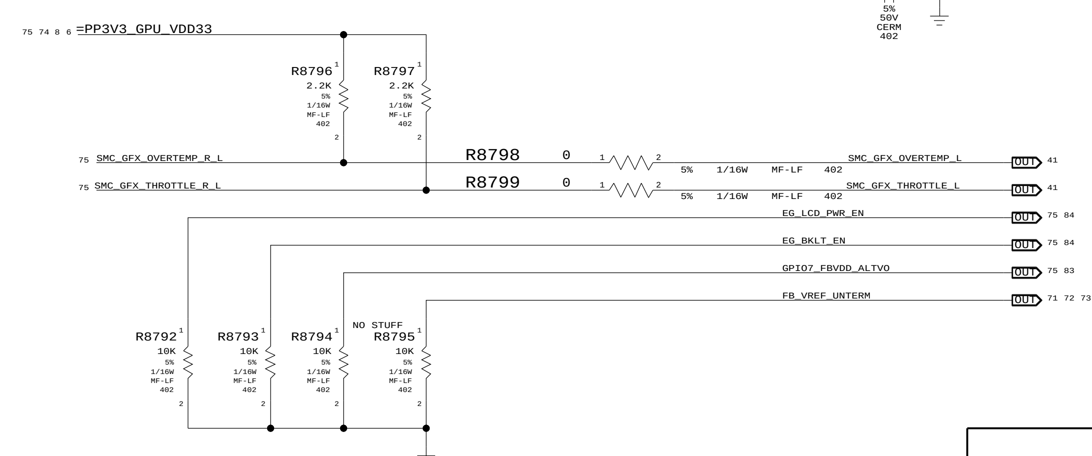
G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.



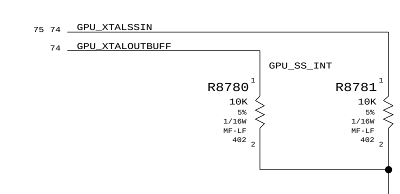
GPU 27MHz Crystal

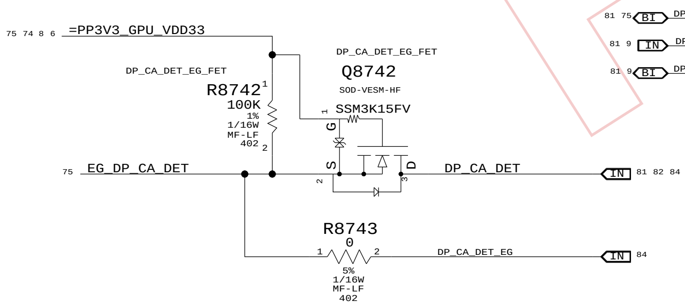






Unused Clocks





Isolation FETs for DP MUX inputs

G96 GPIOs & Straps

SYNC_MASTER=M98_MLB SYNC_DATE=05/12/2008

APPLE INC.

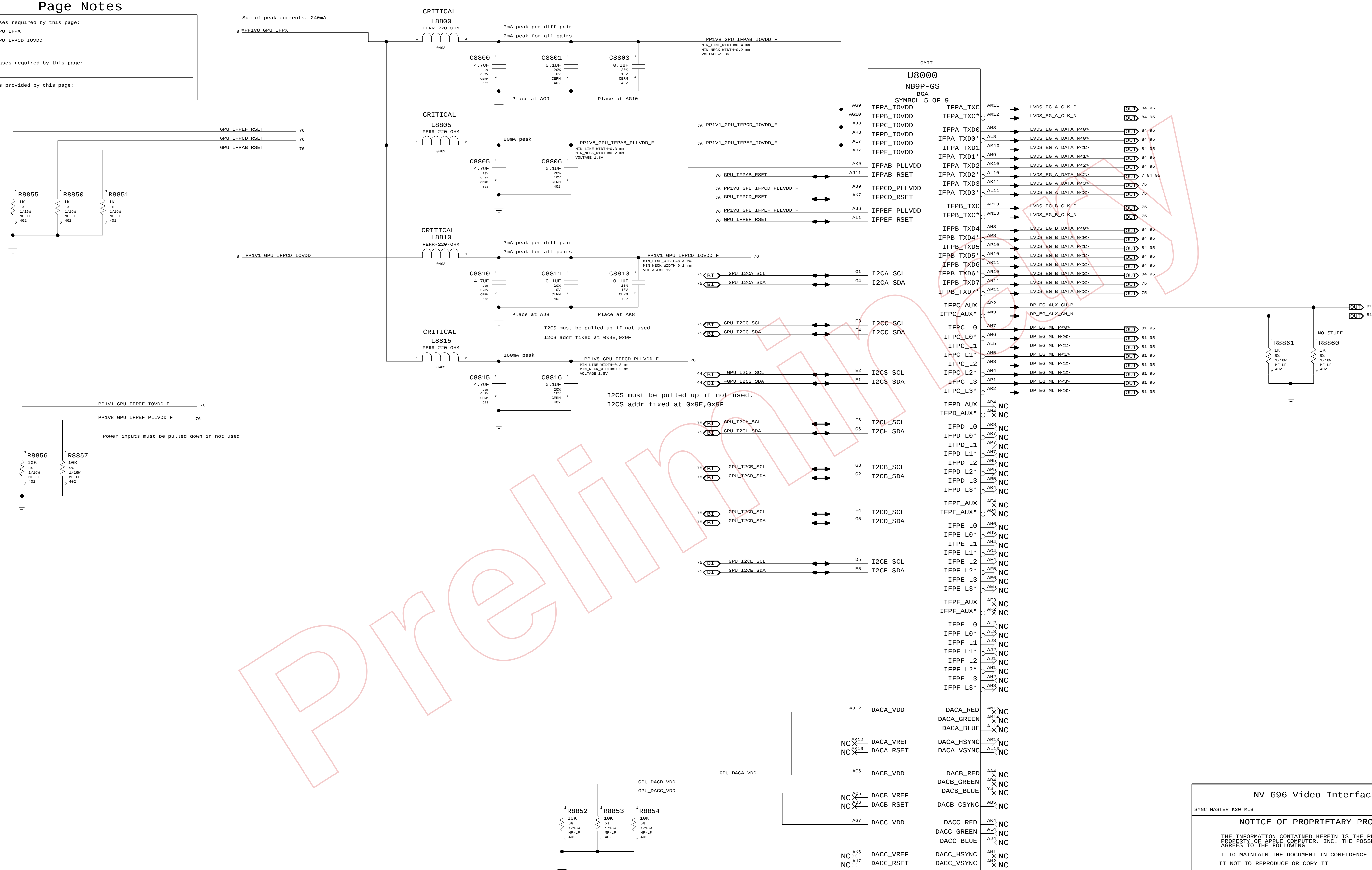
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 87	OF 123

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



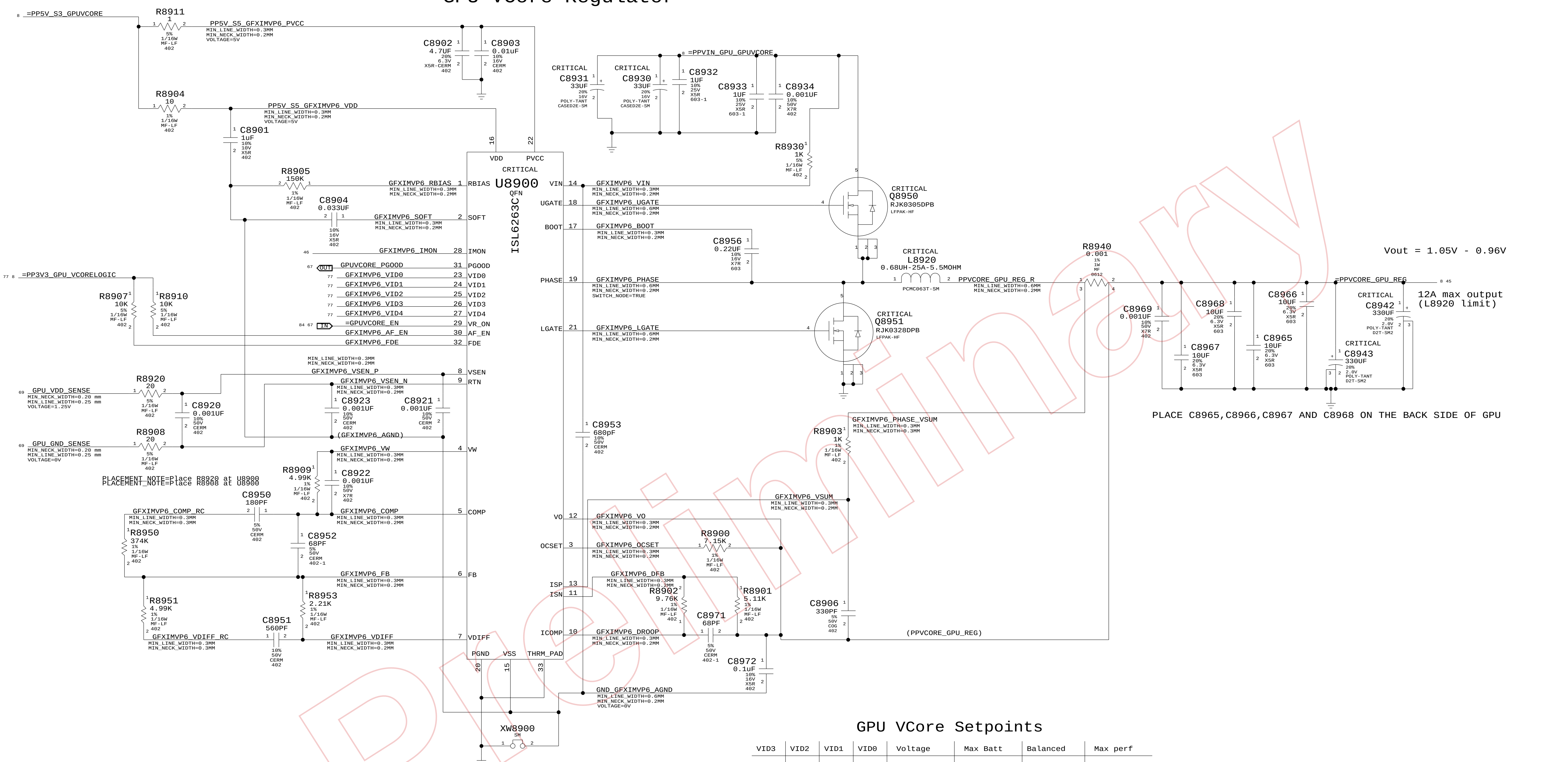
NV G96 Video Interfaces

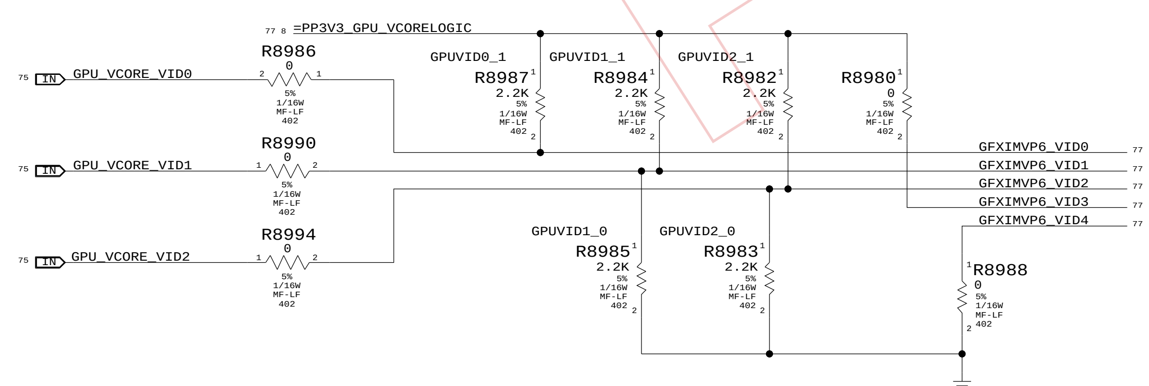
SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 88	OF 123

GPU VCore Regulator





GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	X		-
1	1	1	0	0.92700V	-	X	-
1	0	1	1	1.00425V	-	-	X

Other VID states may not be valid

Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

Preliminary

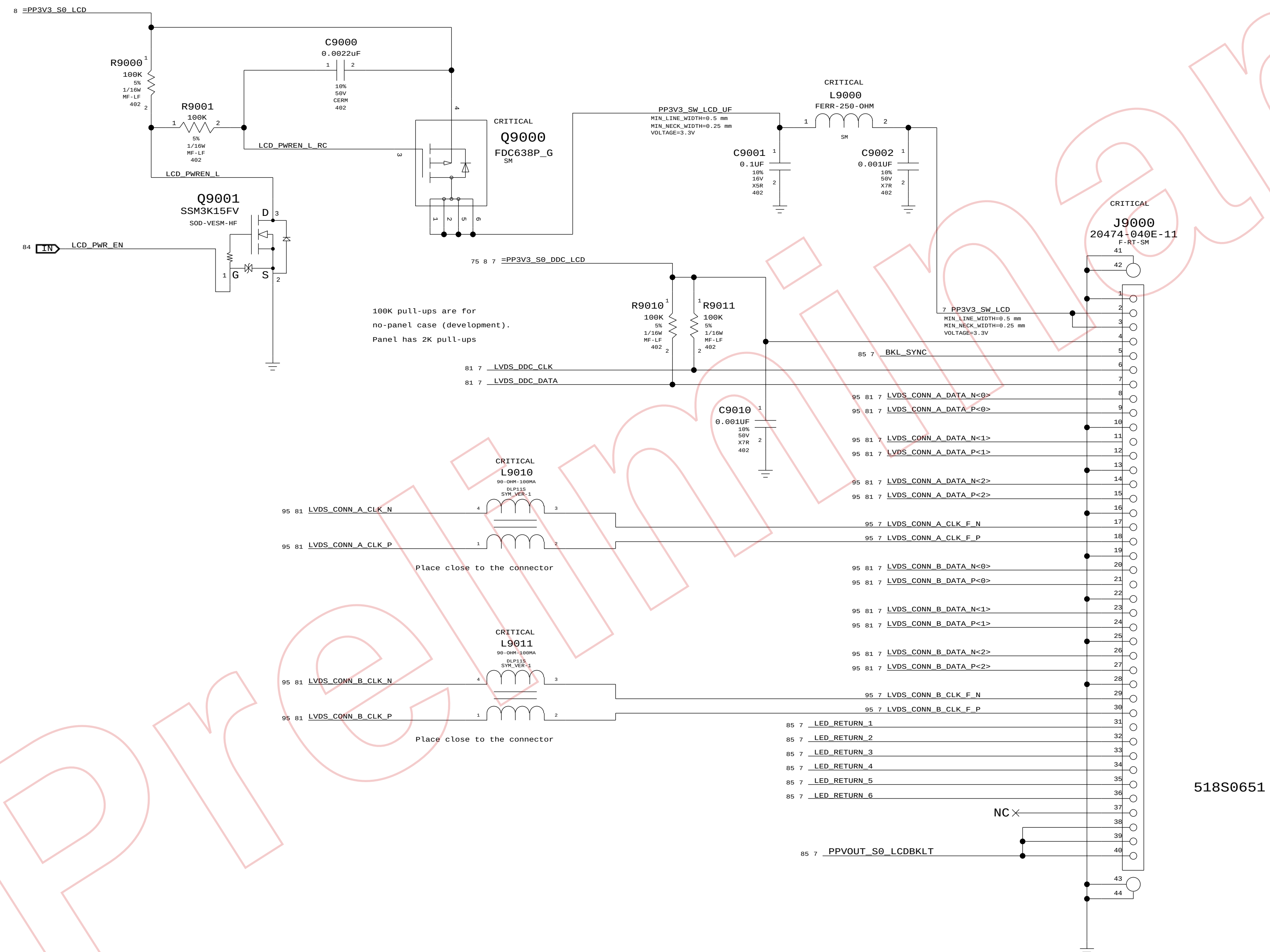
GPU (G96) CORE SUPPLY

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 89	OF 123

LCD (LVDS) INTERFACE



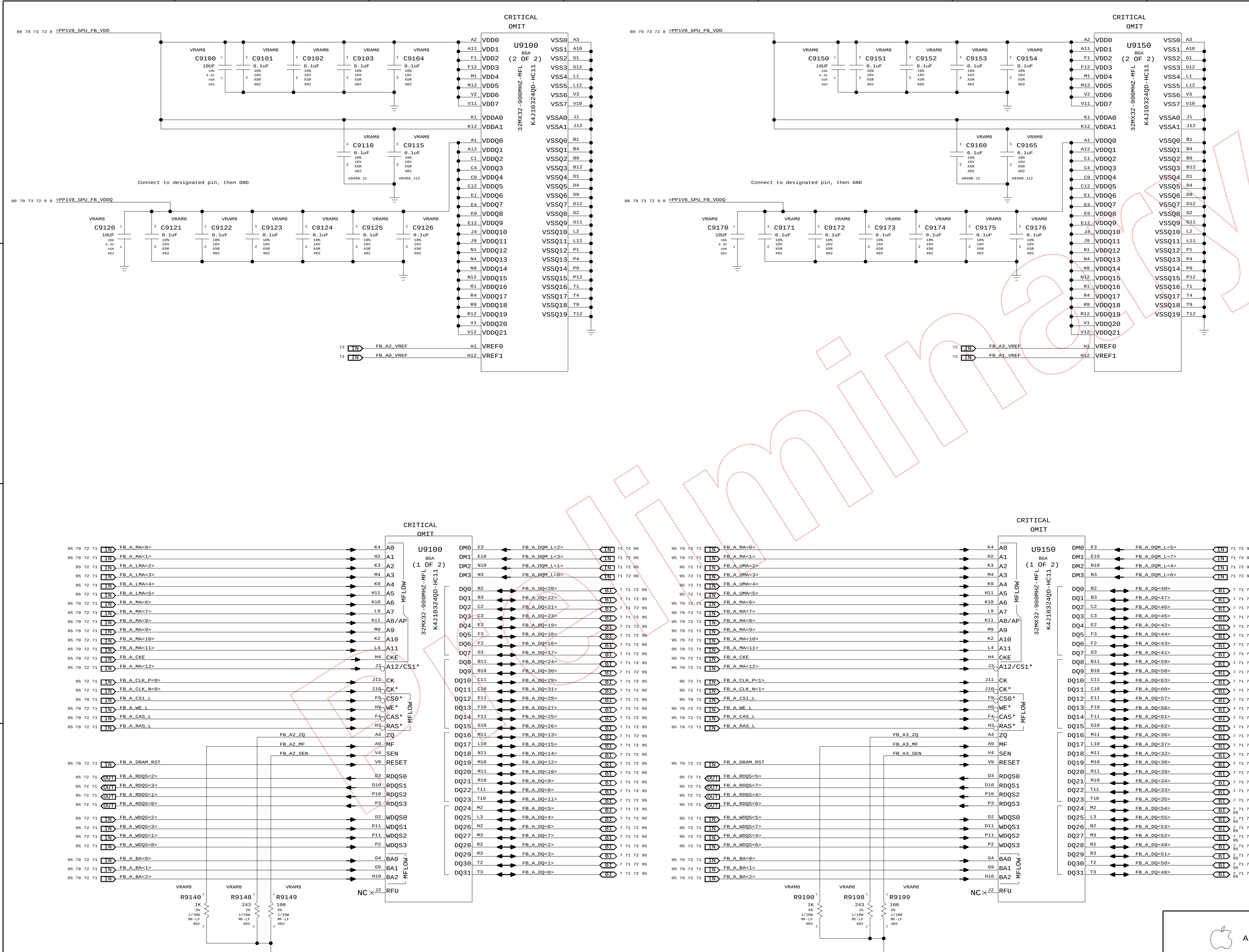
LVDS Display Connector

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 90	OF 123

8 7 6 5 4 3 2 1



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM8

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M99_MLB SYNC_DATE=04/04/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 91	OF 123

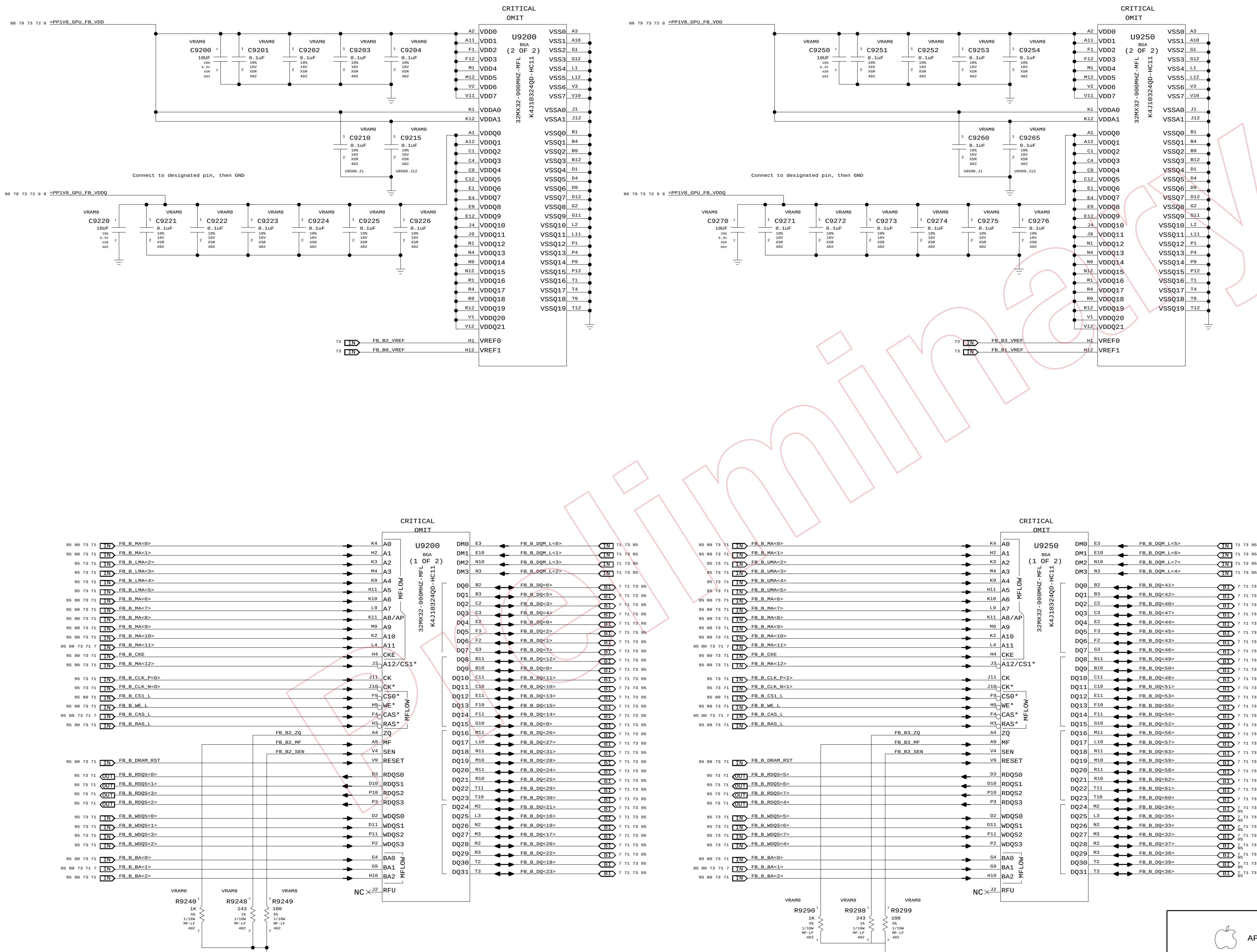
8 7 6 5 4 3 2 1

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM8



GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M88_MLB SYNC_DATE=11/01/2007

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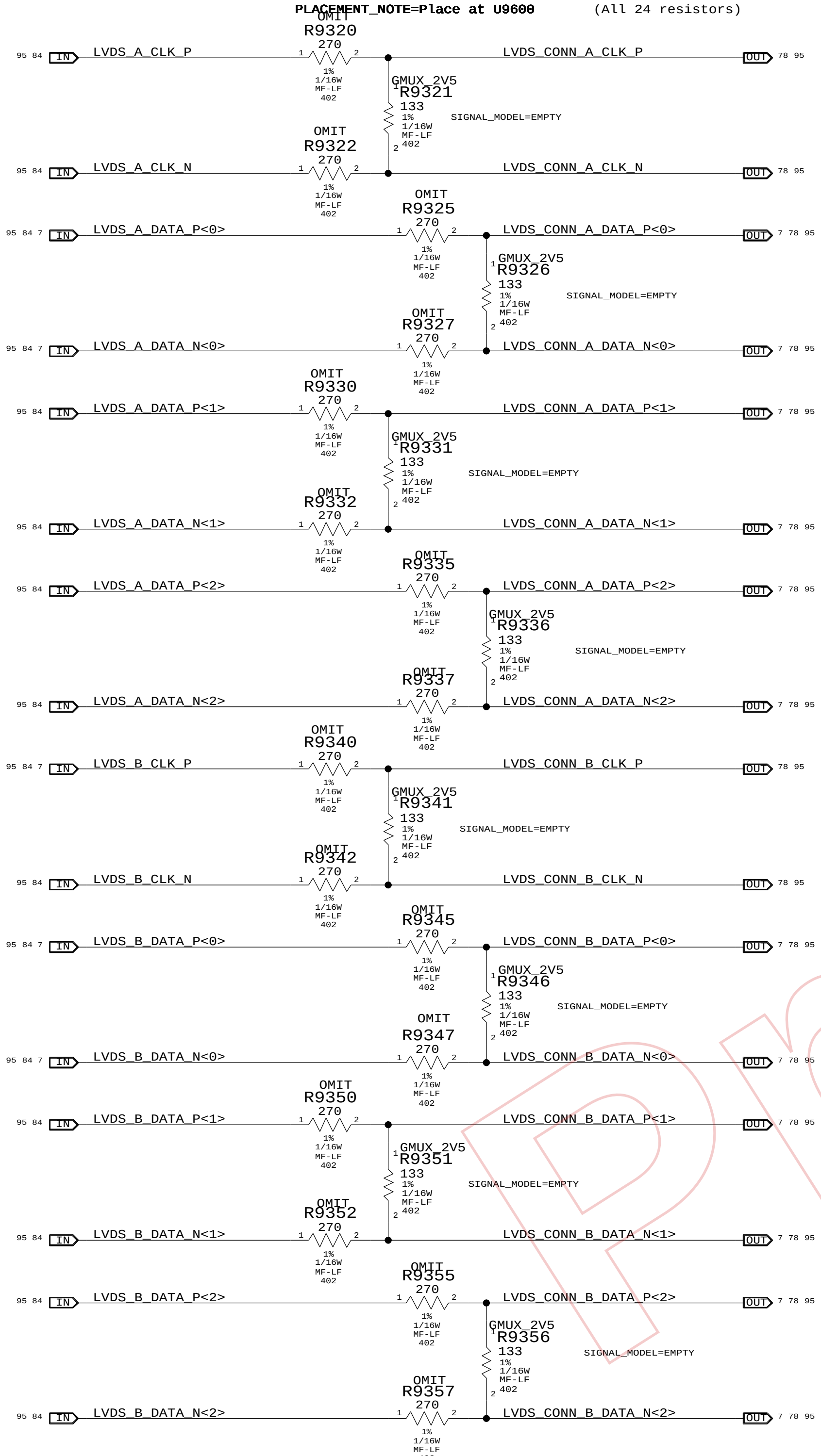
D	051-7656	31
SCALE NONE	SHT 92	OF 123

LVDS Transmitter Termination

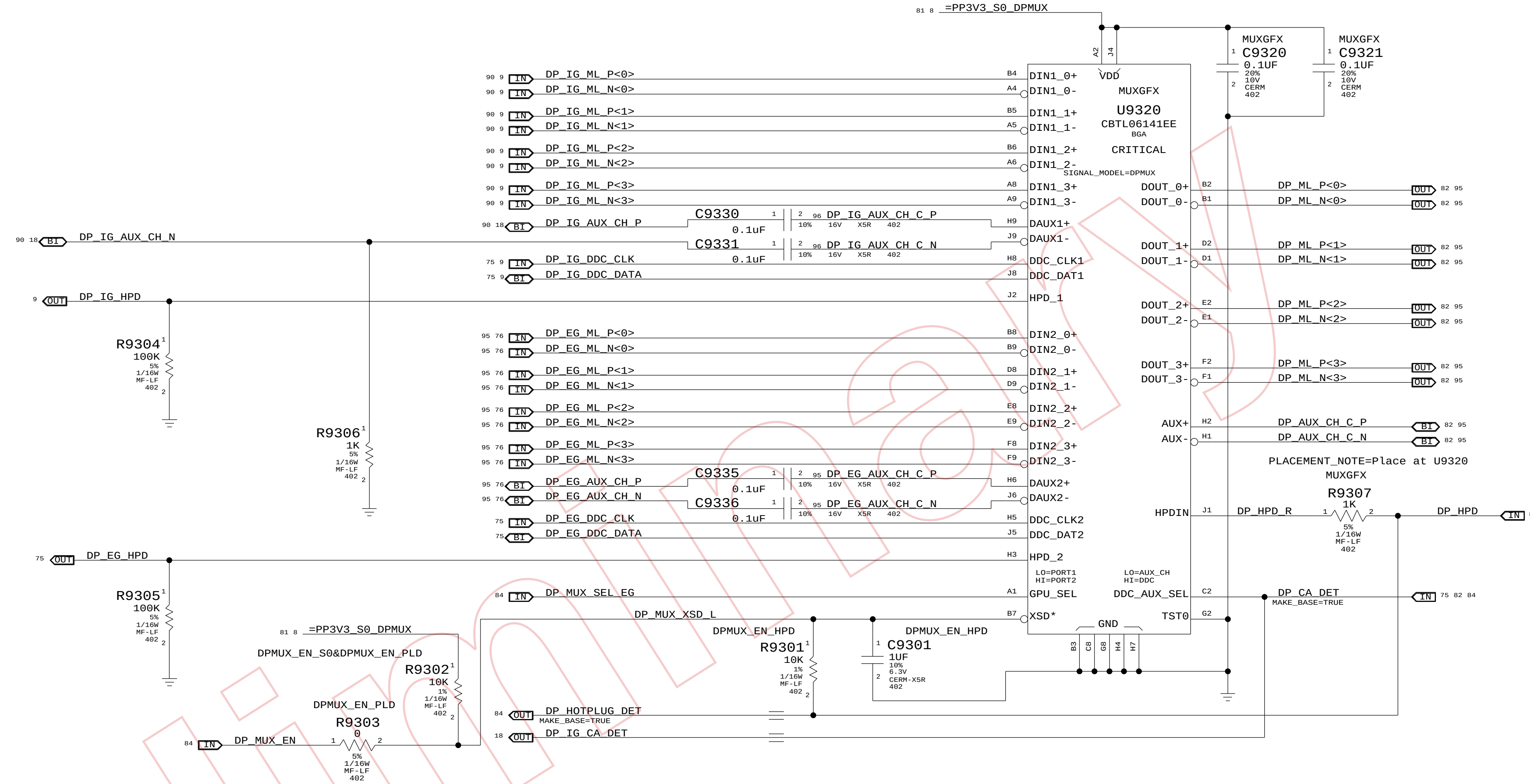
All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9600 (All 24 resistors)

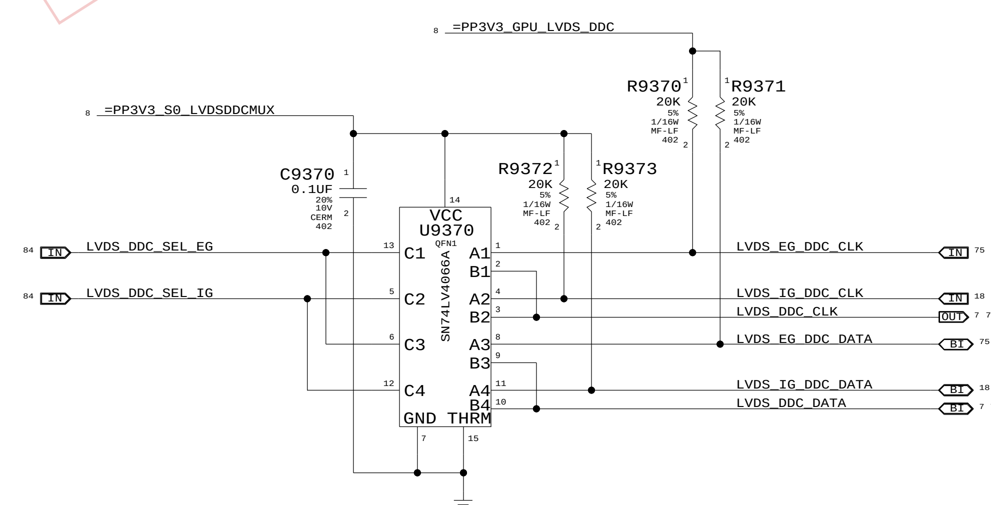


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L	R9320,R9322,R9325,R9327,R9330,R9332,R9335,R9337,R9340,R9342,R9345,R9347,R9350,R9352,R9355,R9357		GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1,0402,SMD,LF	R9320,R9322,R9325,R9327,R9330,R9332,R9335,R9337,R9340,R9342,R9345,R9347,R9350,R9352,R9355,R9357		GMUX_1V8

DisplayPort Mux



LVDS DDC MUX



Muxed Graphics Support

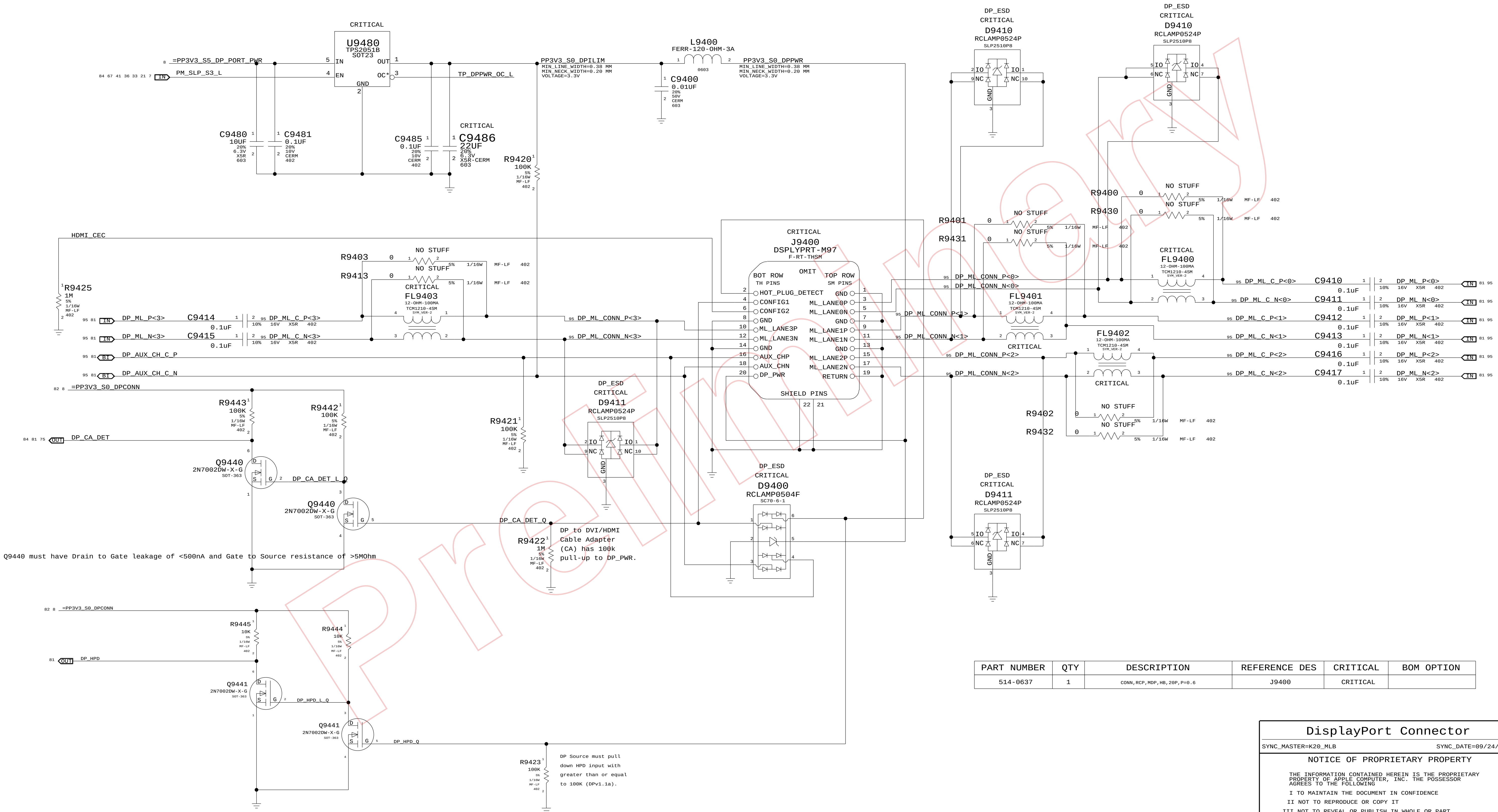
SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	93	123

Port Power Switch



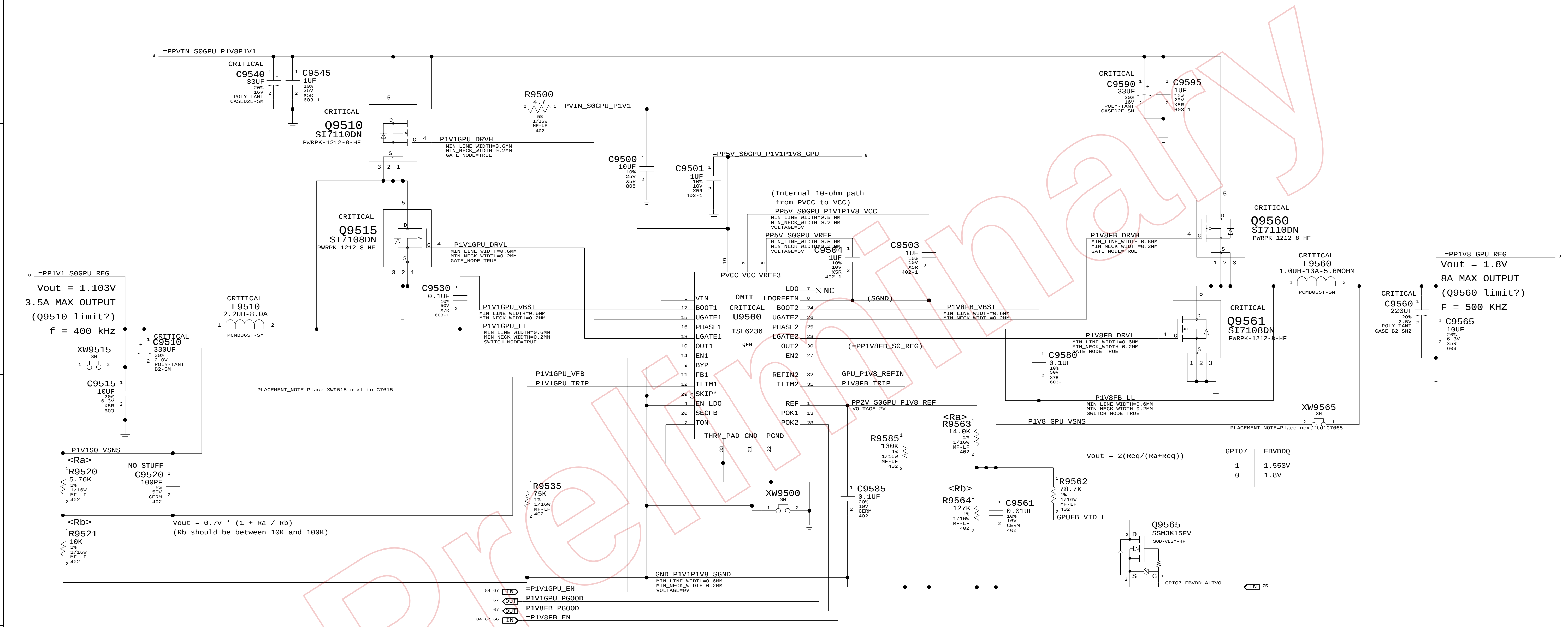
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0637	1	CONN,RCP,MDP,HB,20P,P=0.6	J9400	CRITICAL	

DisplayPort Connector

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 94 OF 123	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CNTRL,QFN32	U9500	CRITICAL	

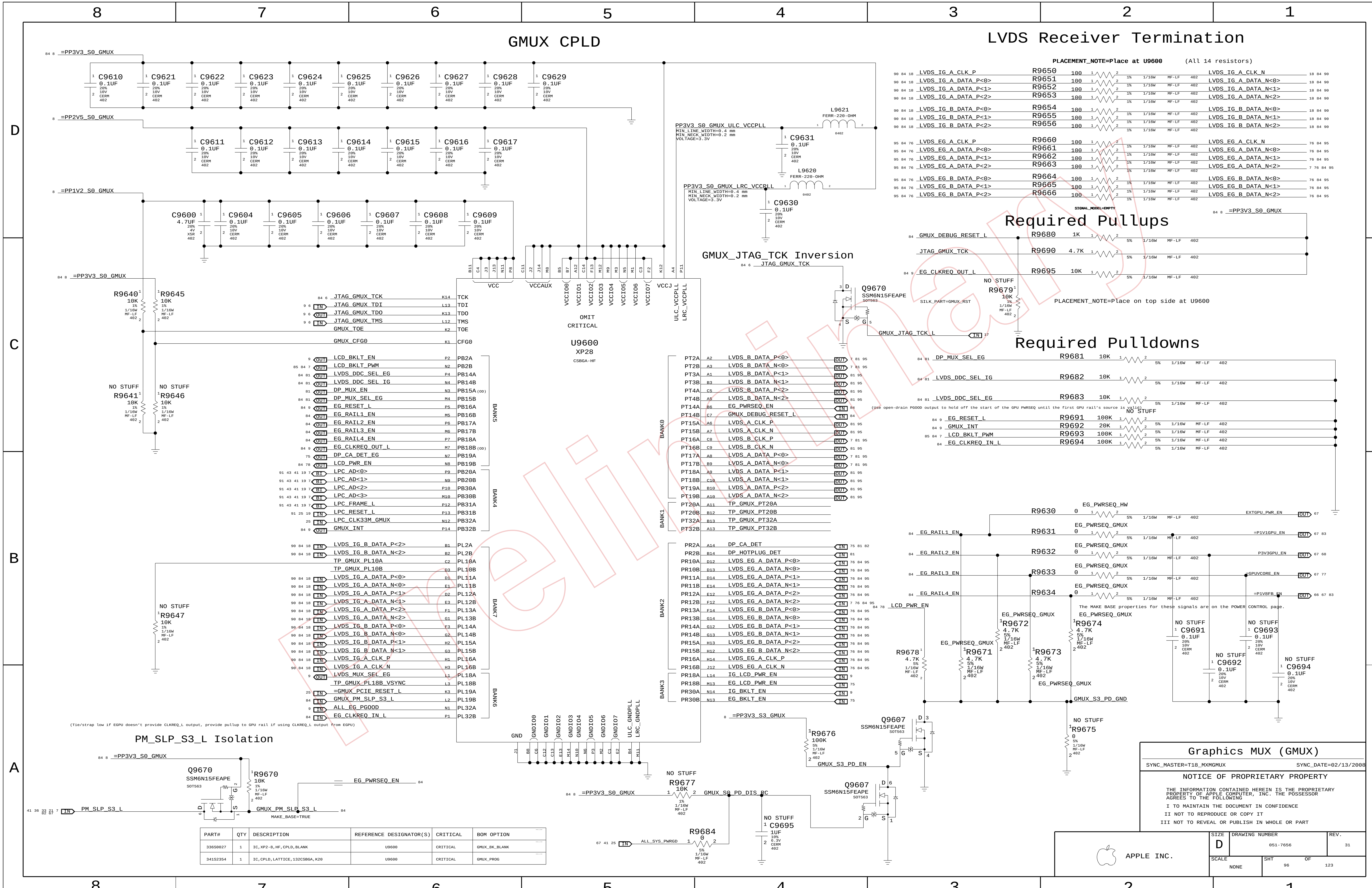
1.1V / 1V8 FB Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

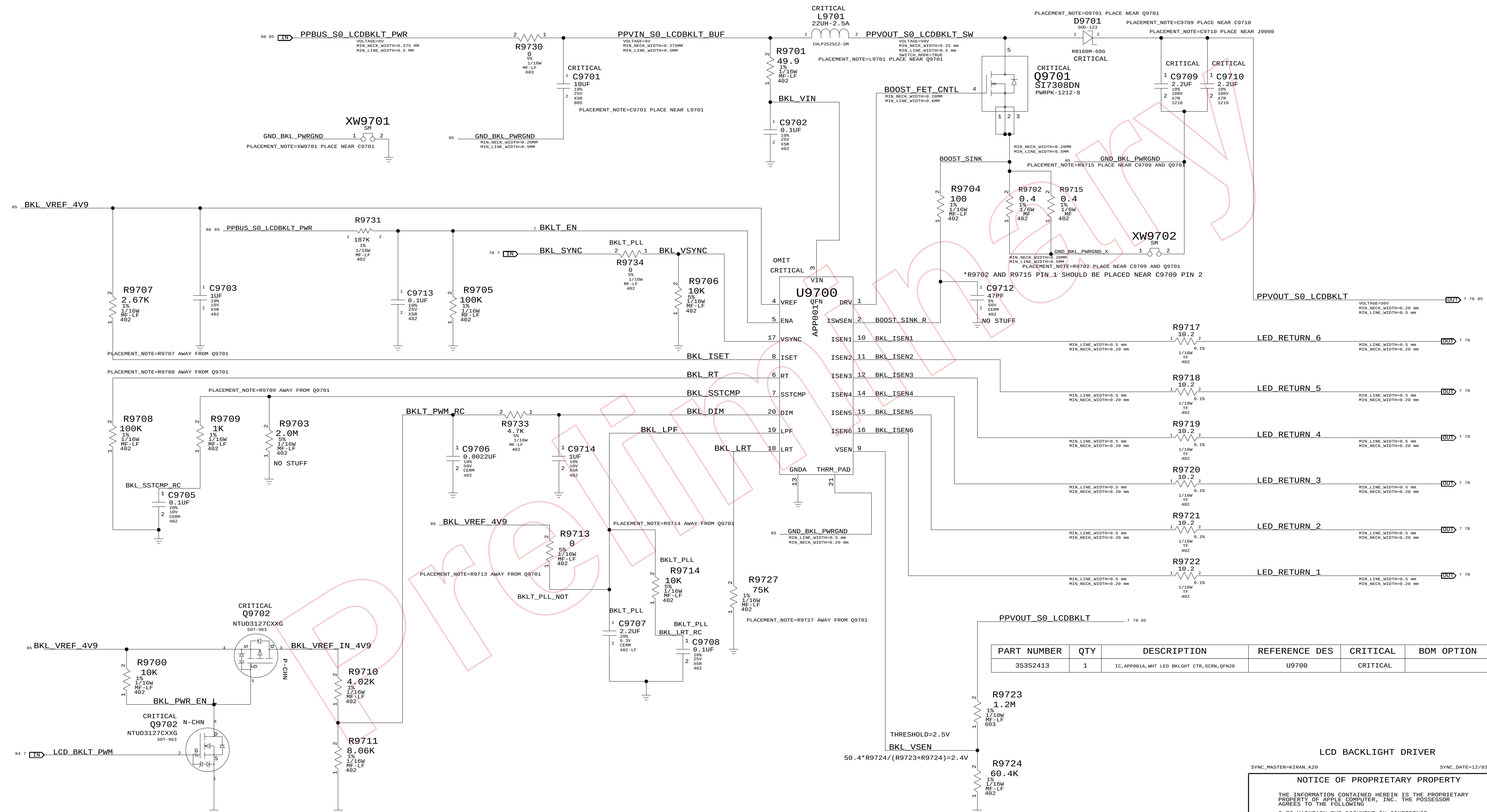
SIZE D | DRAWING NUMBER 051-7656 | REV. 31

SCALE NONE | SHT 95 OF 123



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_BK_BLANK
341S2354	1	IC,CPLD,LATTICE,132CSBGA,K20	U9600	CRITICAL	GMUX_PROG

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2413	1	IC,APP001A,WHT LED BKLGHT CTR,SCRN,QFN20	U9700	CRITICAL	

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

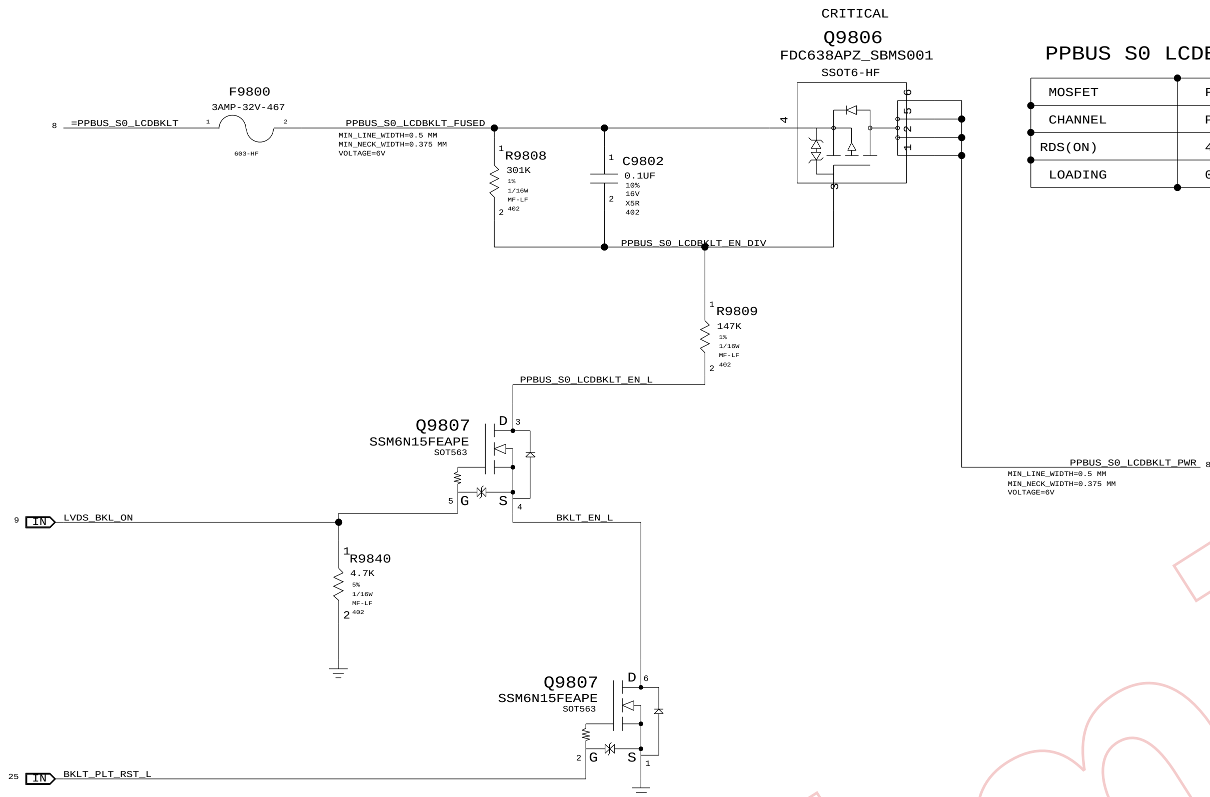
LCD BACKLIGHT DRIVER

SYNC_MASTER=KIRAN_K20 SYNC_DATE=12/03/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 97 OF 123



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

Preliminary

LCD Backlight Support

SYNC_MASTER=YLEE_K20 SYNC_DATE=07/18/2008

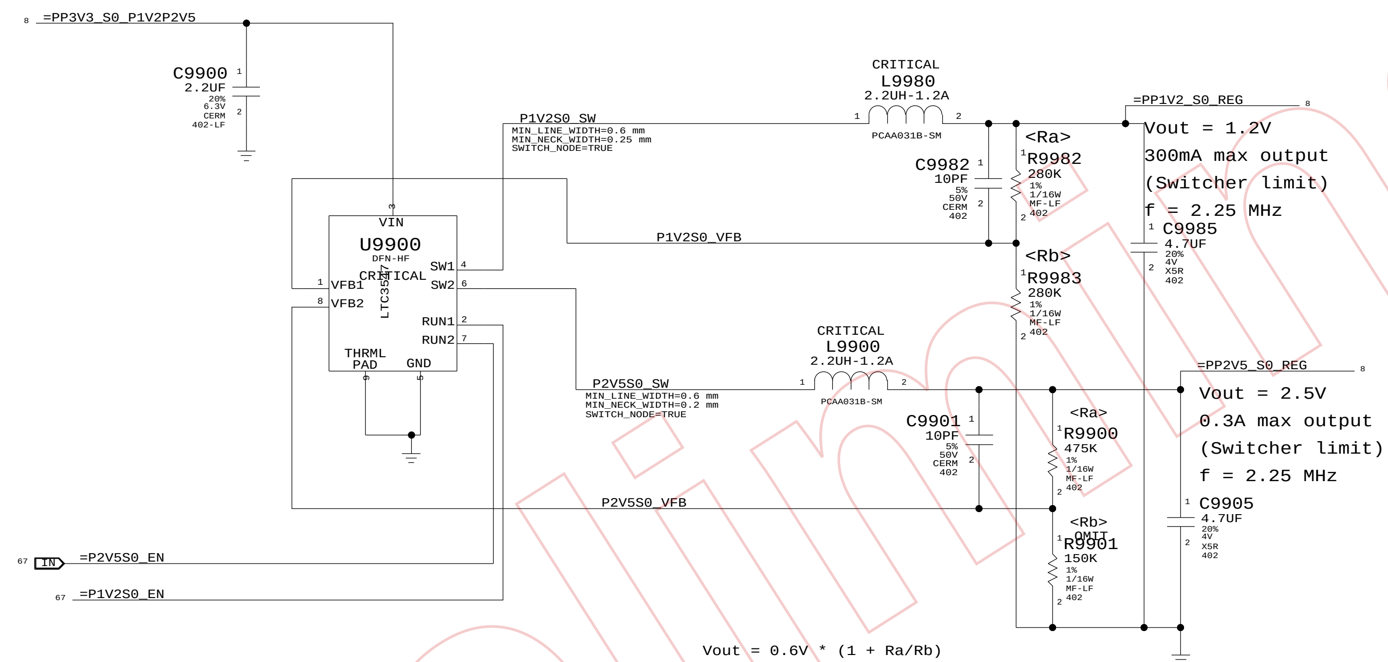
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE NONE

SHT 98 OF 123

GMUX 1.8V/1.2V S0 Switcher



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0428	1	RES,MTL FILM,1/16W,150K,1,0402,SMD,LF	R9901		GMUX_2V5
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R9901		GMUX_1V8

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 99 OF 123

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 42 61
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 42
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 61
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 61
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	61
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61

CPU/FSB Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	100	123

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 101	OF 123

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	69
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	69
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 69
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	69
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	69
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7 17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7 17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P	35
	PCIE_90D	PCIE	PCIE_FW_R2D_N	35
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 35
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 35
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	35
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 31
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	17 31
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	7 17 31
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	7 17 31
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 69
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 69
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 30
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 35
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 31
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 24
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 24
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 24
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	18 24
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	18 24
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 24
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_HDD_R2D_P	7 38
	SATA_100D	SATA	SATA_HDD_R2D_N	7 38
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 38
	SATA_100D	SATA	SATA_HDD_D2R_N	20 38
	SATA_100D	SATA	SATA_HDD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_HDD_D2R_C_N	7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_ODD_R2D_P	7 38
	SATA_100D	SATA	SATA_ODD_R2D_N	7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 38
	SATA_100D	SATA	SATA_ODD_D2R_N	20 38
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 38
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

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8	7	6	5	4	3	2	1

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	7 19 41 43 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	7 19 41 43 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 25 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 43
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 39
	USB_90D	USB	USB_EXTA_N	20 39
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20 30
	USB_90D	USB	USB_CAMERA_N	20 30
USB_BT	USB_90D	USB	USB_BT_P	20 30
	USB_90D	USB	USB_BT_N	20 30
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 49
	USB_90D	USB	USB_TPAD_N	20 49
USB_IR	USB_90D	USB	USB_IR_P	20 40
	USB_90D	USB	USB_IR_N	20 40
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 39
	USB_90D	USB	USB_EXTB_N	20 39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 31
	USB_90D	USB	USB_EXCARD_N	20 31
USB_EXTC	USB_90D	USB	USB_EXTC_P	20 96 98
	USB_90D	USB	USB_EXTC_N	20 96 98
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 53
	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
	HDA_55S	HDA	HDA_RST_L	21 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 53
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 53
	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 41
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 43
	SPI_55S	SPI	SPI_CLK	52
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 43
	SPI_55S	SPI	SPI_MOSI	52
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 43
	SPI_55S	SPI	SPI_MISO_R	52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 43
	SPI_55S	SPI	SPI_CS0_L	

MCP Constraints 2

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	32 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 32
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 32
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32 34
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32 34

Ethernet Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 104 OF 123

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	35 37
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37

Port 2 Not Used

FireWire Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHT 105	OF 123

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	7 44
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	7 44
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 44
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 44
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	60
	1TO1_DIFFPAIR		CHGR_CSI_N	60
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	60
	1TO1_DIFFPAIR		CHGR_CSO_N	60

Preliminary

SMC Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	106	123

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I148	LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
I149	LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
I199	LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	7 81 84
I198	LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	7 81 84
I152	LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	7 81 84
I153	LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
I201	LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	7 81 84
I200	LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	7 81 84
I183		LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 78
I182		LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 78
I184		LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 78
I185		LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 78
I190		LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	78 81
I191		LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	78 81
I192		LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 78 81
I193		LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 78 81
I194		LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	78 81
I195		LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	78 81
I196		LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 78 81
I197		LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 78 81
I161	DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	82
I160		DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
I155	DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	81 82
I157		DP_100D	DISPLAYPORT	DP_ML_N<3..0>	81 82
I202	DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
I203		DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
I159	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
I158	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

GDDR3 FB A/B Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	71 72 79
		GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	71 72 79
	FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	71 72 79
		GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	71 72 79
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	71 72 79
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	71 72 79
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	71 72 79
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	71 72 79
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	71 72 79
	FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	71 72 79
	FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE	71 72 79
	FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L	71 72
	FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	71 72 79
	FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	71 72 79
	FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	71 72 79
	FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	71 72 79
	FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	71 72 79
	FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	71 72 79
	FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	71 72 79
	FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	71 72 79
	FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	71 72 79
	FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	71 72 79
	FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	71 72 79
	FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	7 71 72 79
	FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	7 71 72 79
	FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	7 71 72 79
	FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	7 71 72 79
	FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	71 72 79
	FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	71 72 79
	FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	71 72 79
	FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	71 72 79
	FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	71 72 79
	FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	71 72 79
	FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	71 72 79
	FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	71 72 79
	FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	71 72 79
	FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	71 72 79
	FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	71 72 79
	FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	71 72 79
	FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	7 71 72 79
	FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	7 71 72 79
	FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	7 71 72 79
	FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	7 71 72 79
	FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	71 72 79
	FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	71 72 79
	FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	71 72 79
	FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	71 72 79
I204	FB_AB_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS1_L	71 79

GDDR3 FB C/D Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	71 73 80
		GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	71 73 80
	FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	71 73 80
		GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	71 73 80
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	71 73 80
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	7 71 73 80
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	7 71 73 80
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	71 73 80
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	7 71 73 80
	FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	71 73 80
	FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE	71 73 80
	FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L	7 71 73
	FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	71 73 80
	FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	71 73 80
	FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	71 73 80
	FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	71 73 80
	FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	71 73 80
	FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	71 73 80
	FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	71 73 80
	FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	71 73 80
	FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	71 73 80
	FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	71 73 80
	FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	71 73 80
	FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	7 71 73 80
	FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	7 71 73 80
	FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	7 71 73 80
	FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	7 71 73 80
	FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	71 73 80
	FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	71 73 80
	FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	71 73 80
	FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	71 73 80
	FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	71 73 80
	FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	71 73 80
	FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	71 73 80
	FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	71 73 80
	FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	71 73 80
	FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	71 73 80
	FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	71 73 80
	FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	71 73 80
	FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	7 71 73 80
	FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	7 71 73 80
	FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	7 71 73 80
	FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	7 71 73 80
	FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	71 73 80
	FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	71 73 80
	FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	71 73 80
	FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	71 73 80
I205	FB_CD_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS1_L	71 80

G96 Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	75
	CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	75
	LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	76 84
	LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	76 84
	LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	76 84
	LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	7 76 84
	LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	76 84
	LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	76 84
I142	DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0>	76 81
I144	DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0>	76 81
I140	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	76 81
I143	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	76 81
I139		DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	81
I138		DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GPU (G96) Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 107	OF 123

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLSH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
		ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	34
		ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	34
I146		SATA_100D	SATA	SATA_ODD_R2D_UF_P	38
I145		SATA_100D	SATA	SATA_ODD_R2D_UF_N	38
I144		SATA_100D	SATA	SATA_ODD_D2R_UF_P	38
I142		SATA_100D	SATA	SATA_ODD_D2R_UF_N	38
I143		SATA_100D	SATA	SATA_HDD_D2R_UF_P	38
I140		SATA_100D	SATA	SATA_HDD_D2R_UF_N	38
I141		SATA_100D	SATA	SATA_HDD_R2D_UF_P	38
I139		SATA_100D	SATA	SATA_HDD_R2D_UF_N	38
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P	46 64
		SENSE_1TO1_55S	SENSE	MCPCOREISNS_N	46 64
I124	CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
I125		THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
I127	CPU_THERMD_DP	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 47
I126		THERM_1TO1_55S	THERM	CPU_THERMD_N	10 47
I128	GPUTHMSNS_D_DP	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
I130		THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
I129	GPU_THERMD_DP	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 75
		THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 75
I138	MCPTHMSNS_D_DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	7 47
I137		THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	7 47
I135	MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 47
I136		THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 47
I156	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P	46
I157		SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N	46
I155	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	46
I154		SENSE_1TO1_55S	SENSE	DDRISNS_R_N	46
I153	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	46
I152		SENSE_1TO1_55S	SENSE	GPUISENS_N	46
I151	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P	46 65
I150		SENSE_1TO1_55S	SENSE	1V05CPU_N	46 65
I149	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	46
I148		SENSE_1TO1_55S	SENSE	DDRISNS_N	46
I158	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P	46
I147		SENSE_1TO1_55S	SENSE	P1V8GPU_N	46
I186	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	45
I185		SENSE_1TO1_55S	SENSE	ISNS_CPU_N	45
			GND	GND	
			SB_POWER	PP3V3_S5	7 8
			SB_POWER	PP3V3_S0	7 8 9
			SB_POWER	PP1V5_S0	
I131	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	
I132		SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	
I134	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	46
I133		SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	46
I245	ASIC_CNTRLMEM1	FLSH_55S		NF_CLE_R	96
I246	ASIC_CNTRLMEM1	FLSH_55S		NF_ALE_R	96
I244	ASIC_CNTRLMEM1	FLSH_55S		NF_CE0_L_R	96
I243	ASIC_CNTRLMEM1	FLSH_55S		NF_CE1_L_R	96
I242	ASIC_CNTRLMEM1	FLSH_55S		NF_RE0_L_R	96
I241	ASIC_CNTRLMEM1	FLSH_55S		NF_WE0_L_R	96
I239	ASIC_CNTRLMEM2	FLSH_55S		NF_CLE_R	96
I240	ASIC_CNTRLMEM2	FLSH_55S		NF_ALE_R	96
I238	ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L_R	96
I237	ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L_R	96
I236	ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L_R	96
I235	ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L_R	96
I234	ASIC_CNTRLMEM3	FLSH_55S		NF_CLE	96
I233	ASIC_CNTRLMEM3	FLSH_55S		NF_ALE	96
I232	ASIC_CNTRLMEM3	FLSH_55S		NF_CE0_L	96
I231	ASIC_CNTRLMEM3	FLSH_55S		NF_CE1_L	96
I230	ASIC_CNTRLMEM3	FLSH_55S		NF_RE0_L	96
I229	ASIC_CNTRLMEM3	FLSH_55S		NF_WE0_L	96
I228	ASIC_CNTRLMEM2	FLSH_55S		NF_CLE	96
I227	ASIC_CNTRLMEM2	FLSH_55S		NF_ALE	96
I226	ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L	96
I225	ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L	96
I224	ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L	96
I223	ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L	96

M99 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I160		CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
I159		CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
I168		1TO1_DIFFPAIR		CHGR_CSI_R_P	60
I166		1TO1_DIFFPAIR		CHGR_CSI_R_N	60
I167		1TO1_DIFFPAIR		CHGR_CSO_R_P	45 60
I165		1TO1_DIFFPAIR		CHGR_CSO_R_N	45 60
I182	(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	39
I181	(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	39
I179	(USB_EXTA)	USB_90D	USB	USB2_LT1_P	7 39
I180	(USB_EXTA)	USB_90D	USB	USB2_LT1_N	7 39
I177	(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_P	
I178	(USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_N	
I176	(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 30
I175	(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 30
I174		USB_90D	USB	CONN_USB2_BT_P	7 30
I172		USB_90D	USB	CONN_USB2_BT_N	7 30
I173		USB_90D	USB	USB_LT2_P	7 39
I171		USB_90D	USB	USB_LT2_N	7 39
I169		USB_90D	USB	USB2_EXCARD_CONN_P	7 31
I170		USB_90D	USB	USB2_EXCARD_CONN_N	7 31
I183		DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
I184		DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
I187	MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
I188		CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
I189	PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
I190		PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
I191	PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
I192		PCIE_90D	PCIE	PCIE_FC_D2R_N	
I193		PCIE_90D	PCIE	PCIE_FC_R2D_P	
I194		PCIE_90D	PCIE	PCIE_FC_R2D_N	
I195		CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	7 31
I196		CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	7 31
I198	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_P	7 56 57
I197		DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_N	7 56 57
I201	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_P	7 56 57
I200		DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_N	7 56 57
I199	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_P	7 56 57
I202		DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_N	7 56 57
I206	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_P	7 56 57
I207		DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_N	7 56 57
I247	SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	7 56 57
I248		DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	7 56 57
I210		USB_90D	USB	USB_EXTC_P	20 91 98
I209		USB_90D	USB	USB_EXTC_N	20 91 98
I212		USB_90D	USB	USB_LT3_P	7 98
I211		USB_90D	USB	USB_LT3_N	7 98

Project Specific Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	108	123

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PCB Rule Definitions

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

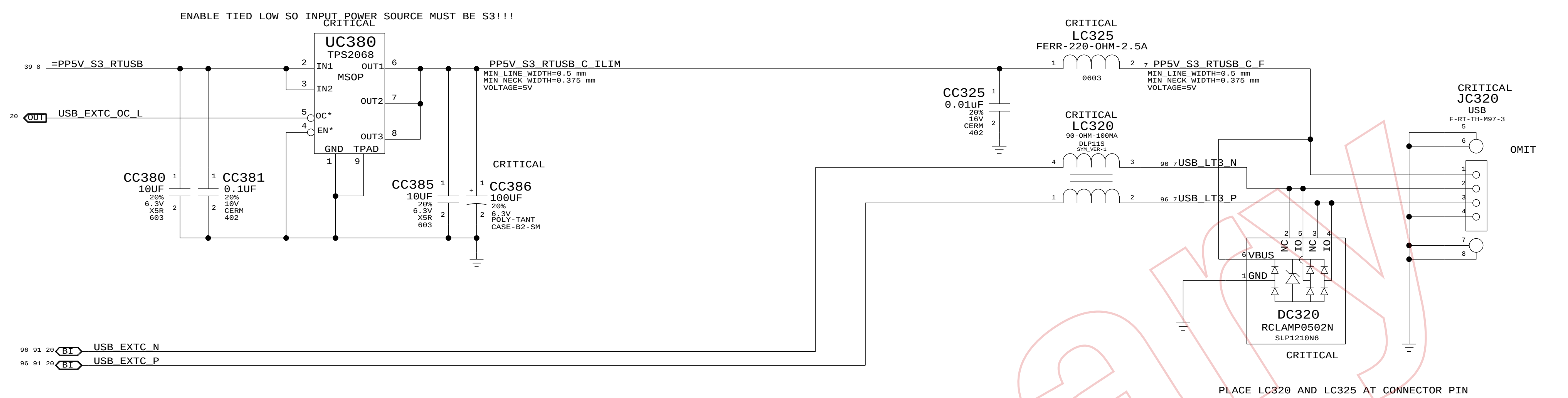
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	109	123

Port Power Switch

LEFT USB PORT C



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	1	CONN,RCPT,USB,HB,4P	JC320	CRITICAL	

PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	123	123