1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC , CANNAREGIO

12/12/08

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
31		657084	ENGINEERING RELEASED	12/12/08	?

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	K20_MLB	04/01/2008
2	2	System Block Diagram	M98_MLB	04/01/2008
3	3	Power Block Diagram	RXU_K20	07/24/2008
4	4	Revision History	NA	NA
5	5	BOM Configuration	K20_MLB	04/01/2008
6	6	JTAG Scan Chain	BEN_K20	07/11/2008
7	7	Functional / ICT Test	K20_MLB	09/24/2008
8	8	Power Aliases	RXU_K20	05/07/2008
9	9	Signal Aliases	K20_MLB	09/24/2008
10	10	CPU FSB	M98_MLB	04/01/2008
11	11	CPU Power & Ground	M98_MLB	04/01/2008
12	12	CPU Decoupling & VID	M98_MLB	04/01/2008
13	13	eXtended Debug Port(MiniXDP)	M98_MLB	04/01/2008
14	14	MCP CPU Interface	T18_MLB	06/06/2008
15	15	MCP Memory Interface	T18_MLB	06/06/2008
16	16	MCP Memory Misc	T18_MLB	06/06/2008
17	17	MCP PCIe Interfaces	T18_MLB	06/06/2008
18	18	MCP Ethernet & Graphics	T18_MLB	06/06/2008
19	19	MCP PCI & LPC	T18_MLB	06/06/2008
20	20	MCP SATA & USB	T18_MLB	06/06/2008
21	21	MCP HDA & MISC	T18_MLB	06/06/2008
22	22	MCP Power & Ground	T18_MLB	06/06/2008
23	25	MCP Standard Decoupling	M98_MLB	04/01/2008
24	26	MCP Graphics Support	M98_MLB	04/01/2008
25	28	SB Misc	M98_MLB	05/01/2008
26	29	FSB/DDR3/FRAMEBUF Vref Margining	BEN_K20	10/15/2008
27	31	DDR3 SO-DIMM Connector A	BEN_K20	06/10/2008
28	32	DDR3 SO-DIMM Connector B	BEN_K20	07/14/2008
29	33	DDR3 Support	M98_MLB	04/01/2008
30	34	Right Clutch Connector	M98_MLB	05/01/2008
31	35	ExpressCard Connector	BEN_K20	10/15/2008
32	37	Ethernet PHY (RTL8211CL)	SUMA_K20	07/22/2008
33	38	Ethernet & AirPort Support	SUMA_K20	07/15/2008
34	39	Ethernet Connector	SUMA_K20	07/15/2008
35	41	FireWire LLC/PHY (FW643)	M98_MLB	04/01/2008
36	42	FireWire Port Power	YWU_K20	05/28/2008
37	43	FireWire Ports	M98_MLB	07/14/2008
38	45	SATA Connectors	M98_MLB	05/01/2008
39	46	External USB Connectors	M98_MLB	07/14/2008
40	48	Front Flex Support	CHANG_K20	07/18/2008
41	49	SMC	T18_MLB	06/06/2008
42	50	SMC Support	M98_MLB	05/01/2008
43	51	LPC+SPI Debug Connector	CHANG_K20	05/28/2008
44	52	K20 SMBUS CONNECTIONS	BEN_K20	07/22/2008
45	53	Current & Voltage Sensing	YWU_K20	08/20/2008
46	54	Current Sensing	YWU_K20	08/12/2008
47	55	Thermal Sensors	YWU_K20	05/28/2008
48	56	Fan Connectors	M98_MLB	04/01/2008
49	57	WELLSPRING 1	YMA_K20	05/19/2008
50	58	WELLSPRING 2	K20_MLB	09/24/2008
51	59	Sudden Motion Sensor (SMS)	YWU_K20	06/17/2008
52	61	SPI ROM	M98_MLB	05/01/2008
53	62	AUDIO:CODEC	AUDIO_K20	09/29/2008
54	63	AUDIO: LINE IN	AUDIO_K20	09/29/2008
55	65	AUDIO: HEADPHONE AMP	AUDIO_K20	09/29/2008
56	66	AUDIO:SPEAKER AMP	AUDIO_K20	09/29/2008
57	67	AUDIO: JACKS	AUDIO_K20	09/29/2008
58	68	AUDIO: JACK TRANSLATORS	AUDIO_K20	09/29/2008
59	69	DC-In & Battery Connectors	RXU_K20	05/21/2008
60	70	PBus Supply & Battery Charger	RXU_K20	05/21/2008
61	71	IMVP6 CPU VCore Regulator	RXU_K20	05/21/2008
62	72	5V / 3.3V Power Supply	RXU_K20	05/21/2008
63	73	1.5V DDR3 Supply	RXU_K20	05/21/2008
64	75	5V_S0 / MCP CORE REGULATOR	RXU_K20	05/21/2008
65	76	CPU VTT Power Supply	RXU_K20	05/21/2008
66	77	Misc Power Supplies	RXU_K20	05/21/2008
67	78	Power Control	YMA_K20	09/09/2008
68	79	Power FETs	YMA_K20	05/19/2008
69	80	NV G96 PCI-E	M98_MLB	04/01/2008
70	81	NV G96 CORE/FB POWER	M98_MLB	04/01/2008
71	82	NV G96 FRAME BUFFER I/F	K20_MLB	09/24/2008
72	84	GDDR3 Frame Buffer A (Bottom)	M98_MLB	04/01/2008
73	85	GDDR3 Frame Buffer B (Bottom)	M98_MLB	04/01/2008
74	86	NV G96 GPIO/MIO/MISC	K20_MLB	09/24/2008
75	87	G96 GPIOs & Straps	M98_MLB	05/12/2008
76	88	NV G96 Video Interfaces	K20_MLB	09/24/2008
77	89	GPU (G96) CORE SUPPLY	RXU_K20	05/21/2008
78	90	LVDS Display Connector	M98_MLB	07/14/2008
79	91	GDDR3 Frame Buffer A (Top)	M99_MLB	04/04/2008
80	92	GDDR3 Frame Buffer B (Top)	M88_MLB	11/01/2007
81	93	Muxed Graphics Support	M98_MLB	05/01/2008
82	94	DisplayPort Connector	K20_MLB	09/24/2008
83	95	1.1V / 1V8 FB Power Supply	RXU_K20	05/21/2008
84	96	Graphics MUX (GMUX)	T18_MXMGMUX	02/13/2008
85	97	LCD BACKLIGHT DRIVER	KIRAN_K20	12/03/2008
86	98	LCD Backlight Support	YLEE_K20	07/18/2008
87	99	Misc Power Supplies	RXU_K20	05/07/2008
88	100	CPU/FSB Constraints	M98_MLB	04/01/2008
89	101	Memory Constraints	M98_MLB	04/01/2008
90	102	MCP Constraints 1	M98_MLB	04/01/2008
91	103	MCP Constraints 2	M98_MLB	04/01/2008
92	104	Ethernet Constraints	M98_MLB	04/01/2008
93	105	FireWire Constraints	M98_MLB	04/01/2008
94	106	SMC Constraints	M98_MLB	04/01/2008
95	107	GPU (G96) Constraints	M98_MLB	05/01/2008
96	108	Project Specific Constraints	M98_MLB	04/01/2008
97	109	PCB Rule Definitions	M98_MLB	04/01/2008
98	123	PROJECT SPECIFIC CONNS	N/A	N/A

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

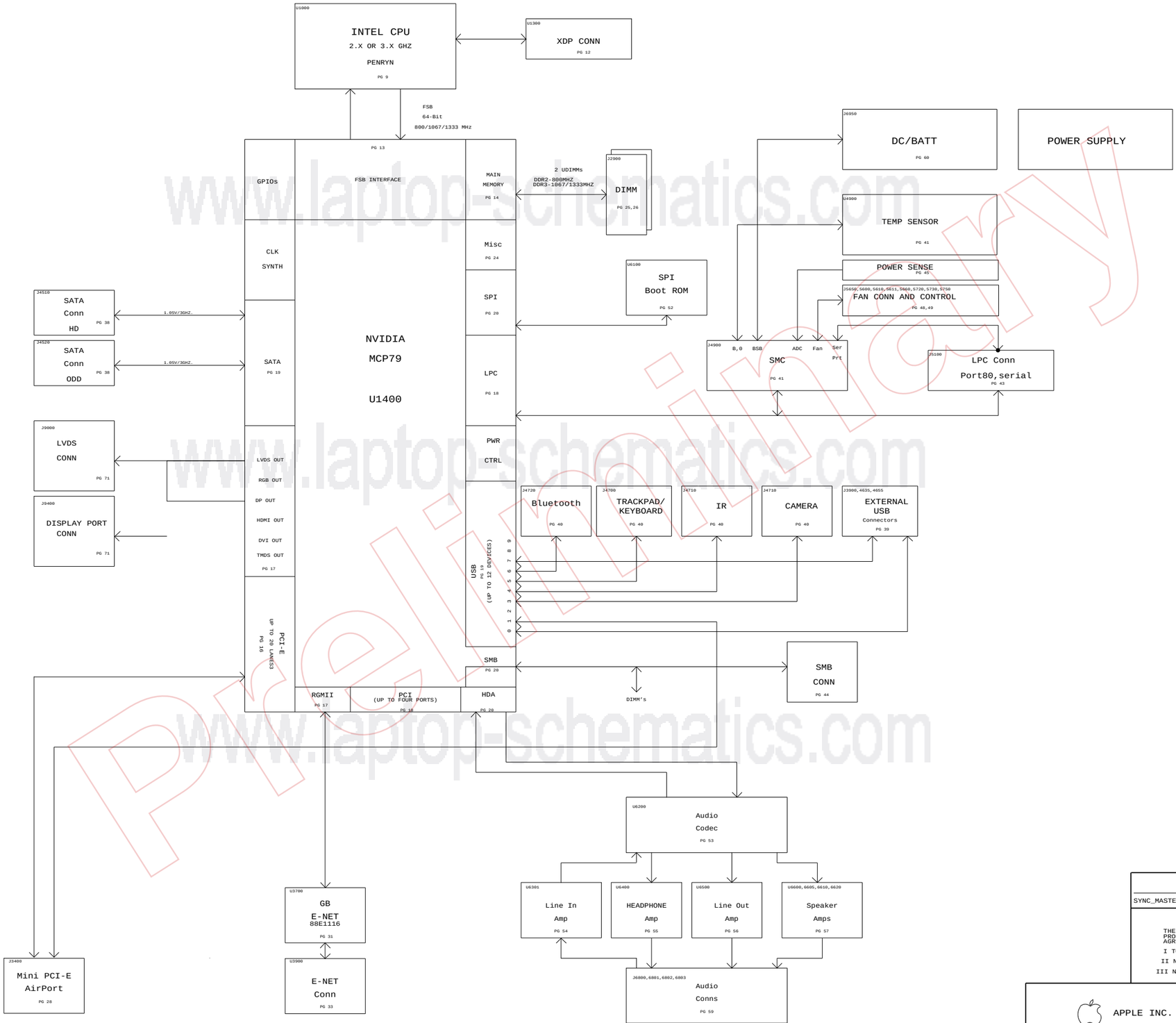
SIZE D

APPLE INC.

TITLE
SCHEM,CANNAREGIO

DRAWING NUMBER 051-7656 REV. 31

SHT 1 OF 123



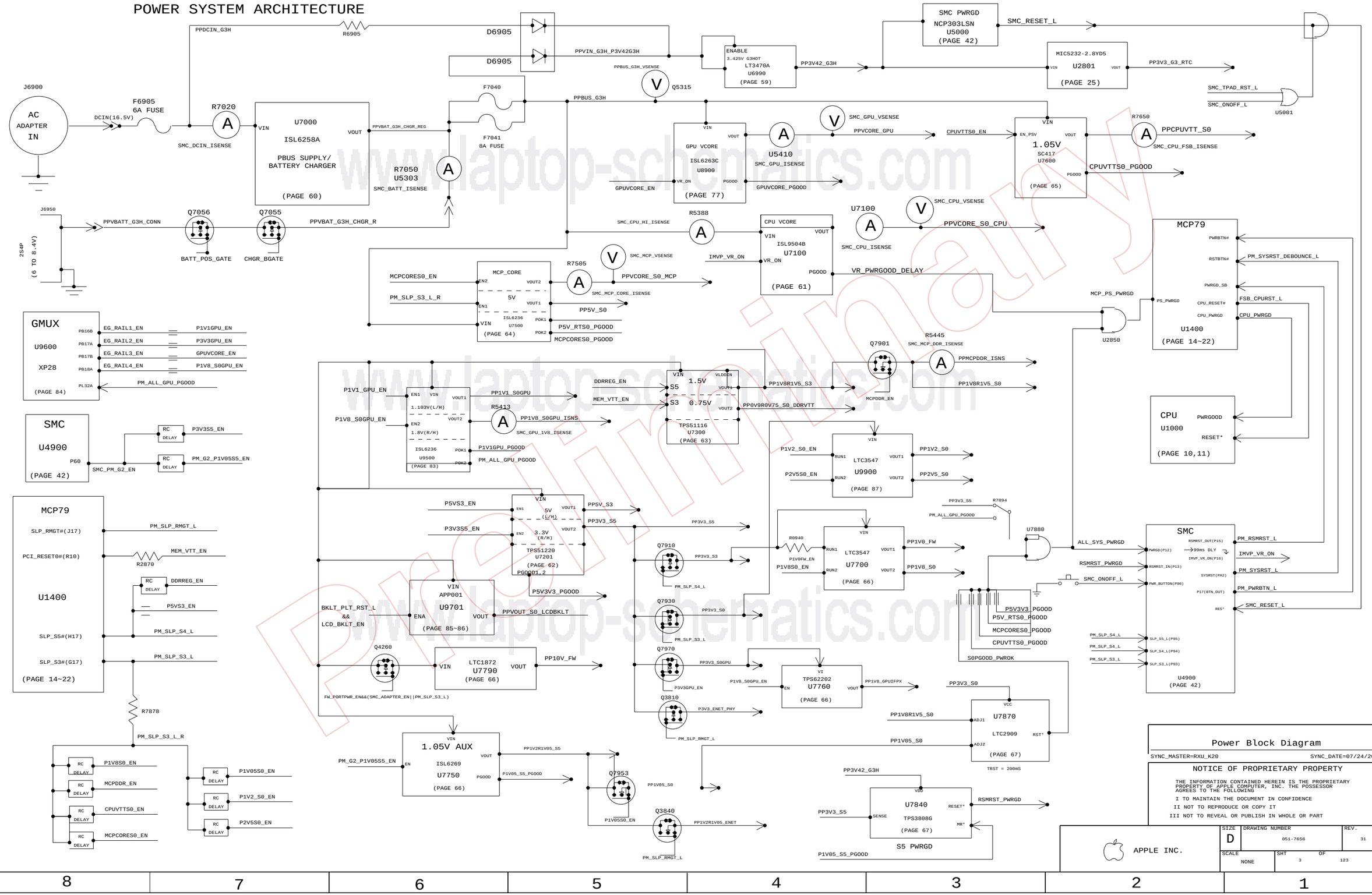
System Block Diagram

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	2	123

POWER SYSTEM ARCHITECTURE



Proto:

See earlier schematics for info about proto changes

Pre-EVT:

See earlier schematics for info about Pre-EVT changes

EVT:

10/29/08
csa. 5 Added BKLT_PLL_NOT BOM option K20_COMMON2 BOM group. This stuffs R9713.
csa. 68 Changed net name on input to U6860 from PP3V3_S0_AUDIO to =PP3V3_S0_AUDIO.
See <rdar://problem/6327731> K20 PreEVT: iPhone headset detection test fail
csa. 97 Changed R9707 to 2.87K per <rdar://problem/6327135> Change R9707 to 2.87k, 1% resistor
10/29/08
csa. 9 Changed SH0924 to 870-1698 tall emi pogo pin.
11/5/08
csa. 4 Updated Revision History.
csa. 8 Tied =PP3V3_FW_FWPHY and =PP3V3_FW_P1V0FW aliases to PP3V3_S0.
csa. 9 Removed R0942 and R0943 which were for selecting from S0 or S3 for =PP3V3_FW_FWPHY.
Removed R0940 and R0941 which were for selecting from S0 or S3 for =PP3V3_FW_P1V0FW.
Tied =PP3V3_S3_GMUX alias to PP3V3_S3.
csa. 75 Changed U7500 from 353S2312 Intersil ISL6236 to 353S2203 TI SN0802043.
Changed TONSEL from GND to PP5V_S0_MCPREG_VCC. This changes output frequencies to 200/300KHz for 5V/MCPCore.
Added C7562 330uF cap on =PPMCPCORE_S0_REG.
Changed snubber resistors R7598 and R7599 to 1/6W 0402, APN 114S0548.
csa. 87 Changed pulldown values to 10K on GPIO7_FBVDDQ_ALTVO, R8794.
Changed pulldowns R8792 and R8793 from 1K to 4.7K for power consumption.
csa. 90 Removed R9094. Replaced by R9678 on csa. 96 to tie to GMUX_S3_PD_GND.
csa. 96 Added Q9607 dual FET for disabling GMUX power sequence enable configuration pulldowns during S0.
Moved R9094 to R9678 and tied to GMUX_S3_PD_GND.
csa. 97 Changed R9707 to 2.67K 1%. This gives 22.5mA on LED current.
11/10/08
csa. 68 Changed R6885 from 0 ohms to 2.2K.
Changed C6885 from 470 pF to 0.0082 uF.
csa. 87 Changed R8792 and R8793 from 4.7K to 10K pulldowns on EG_LCD_PWR_EN and EG_BKLT_EN.
csa. 96 Changed R9678 pulldown on LCD_PWR_EN from 10K to 4.7K.
Removed BOM options on FET circuit for GMUX_S3_PD_GND.
Added R9684 NO STUFF 0 ohms to tie ALL_SYS_PWRGD to Q9607.
11/11/08
csa. 8 removed =PP3V3_S3_P1V0FW and =PP3V3_S3_BKL_VDDIO
csa. 41 changed R4160 from 274K to 200K <rdar://6292976>
csa. 68 changed R6885 from 0 ohm to 2.2K for Mic LPF
csa. 75 NO STUFF R7598, C7598, R7599, C7599 (snubbers)
csa. 87 changed R8795 from 1K to 10K pull down
csa. 96 NO STUFF R9677, C9695, STUFF R9684
11/12/08
csa. 5 removed MCP79 B01 from Module Parts table and added B03
csa. 39 added Bom table for J3900 (514-0636)
csa. 46 added Bom table for J4600, J4610 (514-0638)
csa. 94 added Bom table for J9400 (514-0637)
csa. 123 added Bom table for JC320 (514-0638)
11/13/08
csa. 1 change title to DVT
csa. 32 Added alternate table for J3200 (516S0709, Molex DIMM connector)
11/19/08
csa. 5 changed MCP79 B03 to 338S0710; change to binned G96 338S0714;
added PROD_DIGSMS and TPDT_DEBOUNCE to BOM groups
csa. 68 added bom option TPDT_BYPASS to R6865; TPDT_DEBOUNCE to U6860,C6861,R6860,R6862
csa. 97 changed Q9701 to 376S0757 <radr://6383480>
11/25/08
csa. 5 changed BOM option MCP_B02 to MCP_B03; added BOM option GMUX_1V8
added Mag Layer alternate 155S0457 to Murata 155S0329
csa. 93 added BOM table for 16 LVDS termination resistors to select GMUX_2V5 or GMUX_1V8
added BOM option GMUX_2V5 to 8 parallel resistors so they'll be NO STUFFed for GMUX_1V8
csa. 97 reverted Q9701 to 376S0678 due to parts availability
csa. 99 added BOM table for R9900 to select either 2.5V output or 1.8V output

DVT:

12/02/08
Start of PVT.
csa. 5 removed JTAG_ALLDEV bom option to remove U0600, R0601, C0601, C0602
added 516-0213 (Molex TH SODIMM CONN) as alternate to 516-0201 (Foxconn)
added GMUX_JTAG_CONN bom option to the bom table
csa. 6 added GMUX_JTAG_CONN bom option to J0600
csa. 99 moved OMIT from R9900 to R9901 to select either 150K (GMUX_2V5) or 237K (GMUX_1V8)
12/03/08
csa. 32 removed redundant alternate table for J3200
csa. 97 Per radar 6383480, Change the FET Q9701 from APN: 376S0678 to 376S0757
diode D9701 from APN: 371S0551 to 371S0572
12/09/08
csa. 1 changed title to DVT(1)
csa. 26 NO STUFF C2690, R2690
csa. 32 Refreshed symbol for J3200 for update to BGA SODIMM conn.
csa. 54 changed R5498 to 4.02K for 1.4x gain and R5493 to 2.87K <rdar://6423810>
csa. 89 changed L8920 to 152S0955 (25A Isat); R8900 to 7.15K for 24.6A OCP <rdar://6423810>

12/12/08
csa. 1 changed title to DVT1
csa. 4 removed pre-EVT check in notes from Rev. History
csa. 99 changed text note to reflect 2.5V to 1.8V GMUX rail change

31

SYNC_MASTER=NA SYNC_DATE=NA

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3645	1	IC,PDC,QXXX,Q5,2.66,25W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3644	1	IC,PDC,QXXX,Q5,2.86,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_86GHZ
338S0714	1	IC,ASSP,GPU,NV G96-GS,LOWLKG,BGA969,LF	U8000	CRITICAL	
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/DHCI LINK/PCI-E,12	U4100	CRITICAL	
338S0710	1	IC,MCP79XT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2355	1	IC,SMC,DEVELOPMENT,K20	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2356	1	IC,EFI ROM,DEVELOPMENT,K20	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
338S0603	1	IC,GMCP,MCP79-A01Q,35x35MM,BGA1437	U1400	CRITICAL	MCP_A01Q
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3643	1	IC,PDC,QXXX,Q5,2.93,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_93GHZ
337S3640	1	IC,PDC,SL3BX,PMQ,2.53,35W,1066,C0,6M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3641	1	IC,PDC,SLB43,PMQ,2.80,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
338S0635	1	IC,GMCP,MCP79-B02,35x35MM,BGA1437	U1400	CRITICAL	MCP_B02
333S0481	4	IC,SGRAM,GDDR3,32Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0472	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_QIMONDA
333S0481	8	IC,SGRAM,GDDR3,32Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_1024_SAMSUNG
333S0472	8	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550,U9100,U9150,U9200,U9250	CRITICAL	VRAM_1024_QIMONDA

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cyntec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor
341S2367	341S2366		ALL	Macronix alt to SST
152S0876	152S0782		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
514-0612	514-0607		ALL	FOXLINK ALT TO FOXCONN XCVR
514-0613	514-0608		ALL	FOXLINK ALT TO FOXCONN RCVR
152S0684	152S0421		ALL	MAG LAYERS ALT TO VISHAY
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
516S0709	516S0706		ALL	MOLEX ALT TO FOXCONN
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
516-0213	516-0201		ALL	MOLEX ALT TO FOXCONN

BOM Configuration

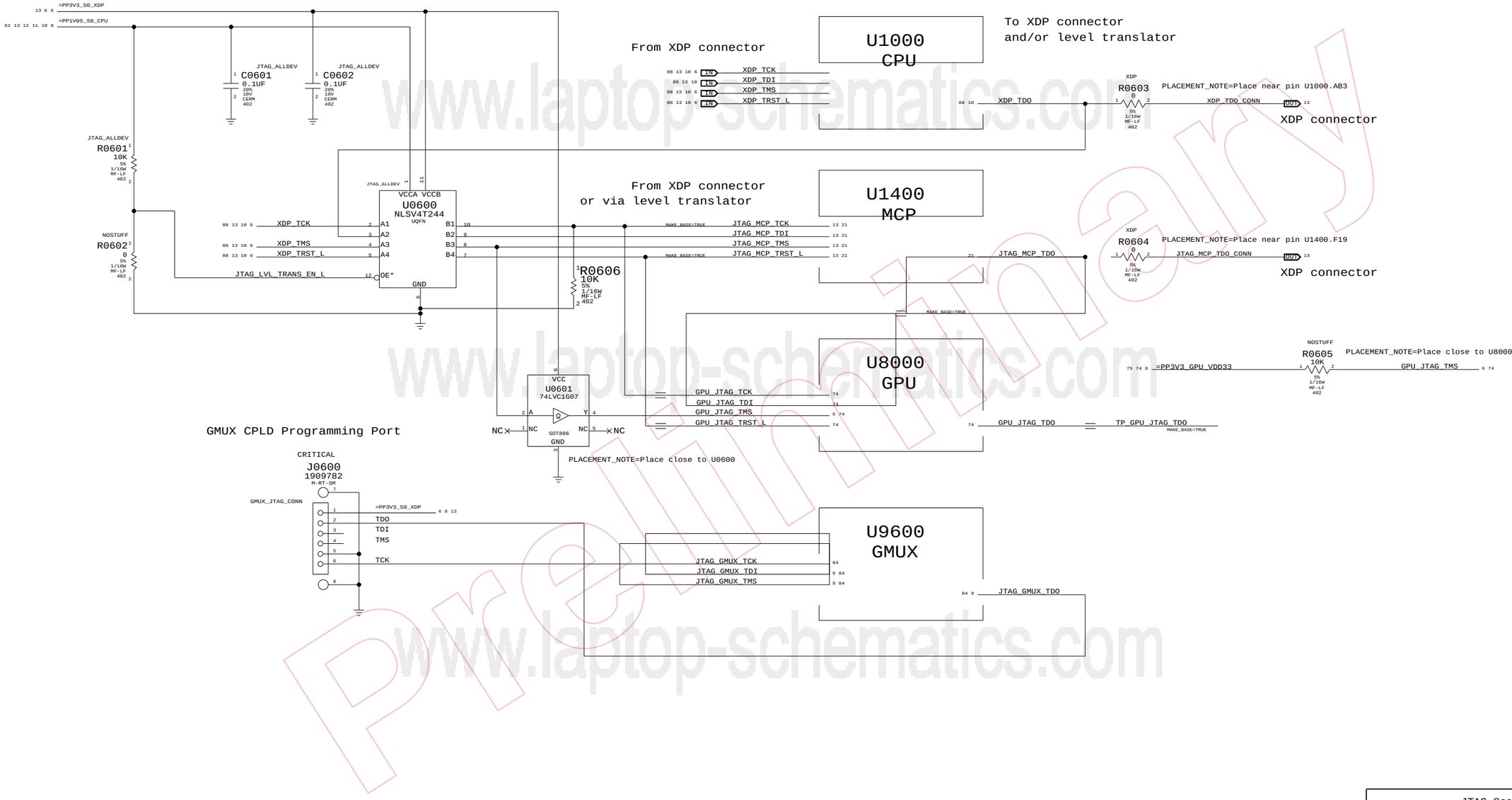
SYNC_MASTER=K20_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 5 OF 123

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 6 OF 123	

Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 48	3 TPs per Fan
TRUE	FAN_LT_PWM	48	
TRUE	FAN_LT_TACH	48	

J5660 (RIGHT FAN CONN)

TRUE	FAN_RT_PWM	48	
TRUE	FAN_RT_TACH	48	5 TPs per Fan
TRUE	GND		

J6780 (MIC CONN)

J557	TRUE	BI_MIC_LO	57 58
J558	TRUE	BI_MIC_SHIELD	57 58
J559	TRUE	BI_MIC_HI	57 58

J6781 (LEFT SPEAKER)

J985	TRUE	SPKRAMP_L1_OUT_P	56 57 96
J987	TRUE	SPKRAMP_L1_OUT_N	56 57 96
J986	TRUE	SPKRAMP_L2_OUT_P	56 57 96
J988	TRUE	SPKRAMP_L2_OUT_N	56 57 96

J6782 (RIGHT & SUB SPEAKER)

J989	TRUE	SPKRAMP_LFE_OUT_P	56 57 96
J990	TRUE	SPKRAMP_LFE_OUT_N	56 57 96
J992	TRUE	SPKRAMP_R1_OUT_P	56 57 96
J991	TRUE	SPKRAMP_R1_OUT_N	56 57 96
J994	TRUE	SPKRAMP_R2_OUT_P	56 57 96
J993	TRUE	SPKRAMP_R2_OUT_N	56 57 96

J9000 (LVDS CONN)

J125	TRUE	BKL_SYNC	78 85
J995	TRUE	PP3V3_SW_LCD	78
J996	TRUE	=PP3V3_S0_DDC_LCD	8 75 78
J997	TRUE	PPVOUT_S0_LCDBKLT	78 85
J998	TRUE	LVDS_DDC_CLK	78 81
J100	TRUE	LVDS_DDC_DATA	78 81
J100	TRUE	LVDS_CONN_A_DATA_P<0>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_N<0>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_P<1>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_N<1>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_P<2>	78 81 95
J100	TRUE	LVDS_CONN_A_DATA_N<2>	78 81 95
J100	TRUE	LVDS_CONN_A_CLK_F_P	78 95
J100	TRUE	LVDS_CONN_A_CLK_F_N	78 95
J100	TRUE	LVDS_CONN_B_DATA_P<0>	78 81 95
J100	TRUE	LVDS_CONN_B_DATA_N<0>	78 81 95
J100	TRUE	LVDS_CONN_B_DATA_P<1>	78 81 95
J100	TRUE	LVDS_CONN_B_DATA_N<1>	78 81 95
J100	TRUE	LVDS_CONN_B_DATA_P<2>	78 81 95
J100	TRUE	LVDS_CONN_B_DATA_N<2>	78 81 95
J100	TRUE	LVDS_CONN_B_CLK_F_P	78 95
J100	TRUE	LVDS_CONN_B_CLK_F_N	78 95
J101	TRUE	LED_RETURN_1	78 85
J101	TRUE	LED_RETURN_2	78 85
J101	TRUE	LED_RETURN_3	78 85
J101	TRUE	LED_RETURN_4	78 85
J101	TRUE	LED_RETURN_5	78 85
J101	TRUE	LED_RETURN_6	78 85
	TRUE	GND	

2 TP needed

4 TPs

J4500 (SATA ODD CONN)

J102	TRUE	PP5V_SW_ODD	38
J102	TRUE	SMC_ODD_DETECT	38 41
J102	TRUE	SATA_ODD_D2R_C_P	38 90
J102	TRUE	SATA_ODD_D2R_C_N	38 90
J102	TRUE	SATA_ODD_R2D_P	38 90
J102	TRUE	SATA_ODD_R2D_N	38 90
	TRUE	GND	

3 TPs

J4501 (SATA HDD CONN)

J103	TRUE	PP5V_S0_HDD_FLT	38
J103	TRUE	SATA_HDD_R2D_P	38 90
J103	TRUE	SATA_HDD_R2D_N	38 90
J103	TRUE	SATA_HDD_D2R_C_N	38 90
J103	TRUE	SATA_HDD_D2R_C_P	38 90
	TRUE	GND	

5 TPs

J5815 (KBD BACKLIGHT CONN)

J114	TRUE	KBDLED_ANODE	50
J114	TRUE	SMC_KDBLED_PRESENT_L	50
	TRUE	GND	

FUNC_TEST

TRUE	GND	
TRUE	GND	6 TPs

USB PORTS

J105	TRUE	PP5V_S3_RTUSB_A_F	39
J105	TRUE	USB2_LT1_N	39 96
J105	TRUE	USB2_LT1_P	39 96
	TRUE	GND	
J105	TRUE	PP5V_S3_RTUSB_B_F	39
J105	TRUE	USB_LT2_N	39 96
J105	TRUE	USB_LT2_P	39 96
	TRUE	GND	
J105	TRUE	PP5V_S3_RTUSB_C_F	98
J105	TRUE	USB_LT3_N	96 98
J105	TRUE	USB_LT3_P	96 98
	TRUE	GND	

J3401 (AIRPORT/BT/CAMERA CONN)

J105	TRUE	PCIE_MINI_D2R_P	17 30 90
J105	TRUE	PCIE_MINI_D2R_N	17 30 90
J105	TRUE	PCIE_MINI_R2D_P	30 90
J105	TRUE	PCIE_MINI_R2D_N	30 90
J105	TRUE	PCIE_CLK100M_MINI_CONN_P	30 96
J105	TRUE	PCIE_CLK100M_MINI_CONN_N	30 96
J105	TRUE	MINI_CLKREQ_Q_L	30
J105	TRUE	PCIE_WAKE_L	7 17 30 31
J105	TRUE	MINI_RESET_CONN_L	30
J105	TRUE	PP5V_WLAN	30
J100	TRUE	PP5V_S3_BTCAMERA_F	30
J100	TRUE	SMBUS_SMC_A_S3_SDA	7 44 94
J100	TRUE	SMBUS_SMC_A_S3_SCL	7 44 94
J100	TRUE	USB_CAMERA_CONN_P	30 96
J100	TRUE	USB_CAMERA_CONN_N	30 96
J100	TRUE	CONN_USB2_BT_P	30 96
J100	TRUE	CONN_USB2_BT_N	30 96

J3500 (EXPRESS CARD CONN)

J106	TRUE	PP1V5_S0_EXCARD_SWITCH	31
J106	TRUE	PCIE_WAKE_L	7 17 30 31
J106	TRUE	SMBUS_MCP_0_CLK	13 21 44 91
J107	TRUE	SMBUS_MCP_0_DATA	13 21 44 91
J107	TRUE	PP3V3_S0_EXCARD_SWITCH	31
J107	TRUE	PP3V3_S3_EXCARD_SWITCH	31
J107	TRUE	USB2_EXCARD_CONN_N	31 96
J107	TRUE	USB2_EXCARD_CONN_P	31 96
J107	TRUE	EXCARD_CPUSB_L	31
J107	TRUE	EXCARD_CLKREQ_CONN_L	31
J107	TRUE	EXCARD_CPPE_L	31
J107	TRUE	PLT_RESET_SWITCH_L	31
J107	TRUE	PCIE_EXCARD_D2R_P	17 31 90
J108	TRUE	PCIE_EXCARD_D2R_N	17 31 90
J108	TRUE	PCIE_EXCARD_R2D_P	31 90
J108	TRUE	PCIE_EXCARD_R2D_N	31 90
J108	TRUE	PCIE_CLK100M_EXCARD_CONN_P	31 96
J108	TRUE	PCIE_CLK100M_EXCARD_CONN_N	31 96

J5800 (IPD FLEX CONN)

J108	TRUE	PP3V3_S3_LDO	50
J108	TRUE	PP18V5_S3	7 50
J108	TRUE	TPAD_GND_F	50
J127	TRUE	Z2_CS_L	49 50
J108	TRUE	Z2_DEBUG3	49 50
J108	TRUE	Z2_MISO	49 50
J109	TRUE	Z2_BOOST_EN	50
J109	TRUE	Z2_BOOT_CFG1	49 50
J109	TRUE	Z2_CLKIN	49 50
J109	TRUE	Z2_KEY_ACT_L	49 50
J109	TRUE	Z2_RESET	49 50
J109	TRUE	PSOC_F_CS_L	49 50
J109	TRUE	PICKB_L	49 50
J109	TRUE	PSOC_MISO	49 50
J109	TRUE	PSOC_MOSI	49 50
J109	TRUE	PSOC_SCLK	49 50
J110	TRUE	SMBUS_SMC_A_S3_SCL	7 44 94
J110	TRUE	SMBUS_SMC_A_S3_SDA	7 44 94

J6900 (DC POWER CONN)

J115	TRUE	ADAPTER_SENSE	59
J115	TRUE	PP18V5_DCIN_FUSE	59
	TRUE	GND	

J6950 (MAIN BATT CONN)

J113	TRUE	PPVBAT_G3H_CONN_F	59
J113	TRUE	SMBUS_SMC_BSA_SCL	7 44 94
J113	TRUE	SMBUS_SMC_BSA_SDA	7 44 94
J113	TRUE	SMC_BS_ALRT_L	41 42 59
	TRUE	GND	

J6995 (BAT LED CONN)

J114	TRUE	PP3V42_G3H	7 8 42
J114	TRUE	SMBUS_SMC_BSA_SDA	7 44 94
J114	TRUE	SMBUS_SMC_BSA_SCL	7 44 94
J114	TRUE	SMC_BIL_BUTTON_DB_L	42 59
	TRUE	GND	

J5713 (KEY BOARD CONN)

E110	TRUE	PP3V3_S3	7 8
E110	TRUE	PP3V42_G3H	7 8 42
E110	TRUE	WS_KBD1	49
E110	TRUE	WS_KBD2	49
E110	TRUE	WS_KBD3	49
E110	TRUE	WS_KBD4	49
E110	TRUE	WS_KBD5	49
E110	TRUE	WS_KBD6	49
E111	TRUE	WS_KBD7	49
E111	TRUE	WS_KBD8	49
E111	TRUE	WS_KBD9	49
E111	TRUE	WS_KBD10	49
E111	TRUE	WS_KBD11	49
E111	TRUE	WS_KBD12	49
E111	TRUE	WS_KBD13	49
E111	TRUE	WS_KBD14	49
E111	TRUE	WS_KBD15_CAP	49
E111	TRUE	WS_KBD16_NUM	49
E111	TRUE	WS_KBD17	49
E112	TRUE	WS_KBD18	49
E112	TRUE	WS_KBD19	49
E112	TRUE	WS_KBD20	49
E112	TRUE	WS_KBD21	49
E112	TRUE	WS_KBD22	49
E112	TRUE	WS_KBD23	49
E112	TRUE	WS_KBD_ONOFF_L	49
E113	TRUE	WS_LEFT_SHIFT_KBD	49
E113	TRUE	WS_LEFT_OPTION_KBD	49
E113	TRUE	WS_CONTROL_KBD	49

J4800 (FRONT CABLE CONN)

E114	TRUE	PP3V42_G3H_LIDSWITCH_R	40
E114	TRUE	PP5V_S3_IR_R	40
E114	TRUE	SMC_LID_R	40
E114	TRUE	IR_RX_OUT	40
E114	TRUE	SYS_LED_ANODE	40 42
	TRUE	GND	

J5502 (SENSOR CONN)

E115	TRUE	MCPTHMSNS_D_P	47 96
E115	TRUE	MCPTHMSNS_D_N	47 96

POWER RAILS

FUNC_TEST

L648	TRUE	PM_SLP_S3_L	21 33 36 41 67 82 84
L802	TRUE	PPBUS_G3H	8 45
E801	TRUE	PPBUS_CPU_IMVP_ISNS	8
E804	TRUE	PP3V42_G3H	7 8 42
E605	TRUE	PP5V_S3	8
E605	TRUE	PP5V_S0	8
E607	TRUE	PPVCORE_S0_CPU	8
E605	TRUE	PPVCORE_S0_MCP	7 8
E610	TRUE	PP3V3_S5	8 96
E612	TRUE	PP3V3_S3	7 8
E611	TRUE	PP3V3_S0	8 9 95
E615	TRUE	PP2V5_S0	8
E605	TRUE	PP1V2_S0	8
E625	TRUE	PP1V8_S0	8
E624	TRUE	PP1VBR1V5_S3	8
E623	TRUE	PP1VBR1V5_S0	8
E622	TRUE	PPMCPDDR_ISNS	7 8
E620	TRUE	PP1V05_S0	8
E621	TRUE	PP1V2R1V05_S5	8
E618	TRUE	PPCPUVTT_S0	8
E617	TRUE	PP0V9R0V75_S0_DDRVTT	8
E615	TRUE	PP1V2R1V05_ENET	8
E616	TRUE	PP3V3_ENET_PHY	8
E614	TRUE	PPVP_FW	8
E627	TRUE	PP1V0_FW	8
E626	TRUE	PP3V3_S0GPU	8
E629	TRUE	PP1V1_S0GPU	8
E638	TRUE	PP1V8_S0GPU_ISNS	8
E637	TRUE	PPVCORE_GPU	8
E636	TRUE	PP1V8_S0GPU_ISNS_R	8
J789	TRUE	PP3V3_S5_AVREF_SMC	41 42
E710	TRUE	PP18V5_S3	7 50
E710	TRUE	PPDCIN_G3H	8
E110	TRUE	PPVCORE_S0_MCP	7 8
E110	TRUE	PPMCPDDR_ISNS	7 8
E110	TRUE	PPVTTDDR_S3	8
E110	TRUE	PP1V8_GPUIFPX	8

FUNC_TEST

E220	TRUE	SYS_LED_ANODE_R	40
E220	TRUE	LPC_CLK33M_LPCPLUS	25 43 91
E220	TRUE	LPC_AD<0..3>	19 41 43 84 91
E220	TRUE	SPI_ALT_MOSI	43
E220	TRUE	SPI_ALT_MISO	43
E220	TRUE	LPC_FRAME_L	19 41 43 84 91
E227	TRUE	PM_CLKRUN_L	19 41 43
E220	TRUE	SMC_TMS	41 42 43
E220	TRUE	DEBUG_RESET_L	25 43
E220	TRUE	SMC_TDO	41 42 43
E220	TRUE	SMC_TRST_L	41 43
E231	TRUE	SMC_MD1	41 43
E230	TRUE	SMC_TX_L	39 41 42 43
E230	TRUE	SPIROM_USE_MLB	43
E230	TRUE	SPI_ALT_CLK	43
E230	TRUE	SPI_ALT_CS_L	43
E737	TRUE	LPC_SERIRQ	19 41 43
E230	TRUE	LPC_PWRDWN_L	19 41 43
E739	TRUE	SMC_TDI	41 42 43
E740	TRUE	SMC_TCK	41 42 43
E741	TRUE	SMC_RESET_L	41 42 43
E742	TRUE	SMC_NMI	41 43
E743	TRUE	SMC_RX_L	39 41 42 43
E744	TRUE	LPCPLUS_GPIO	18 43
E761	TRUE	ISSP_SCLK_P1_1	49
E762	TRUE	ISSP_SDATA_P1_0	49
	TRUE	SMC_ONOFF_L	41 42 49
E745	TRUE	PM_SYSRST_L	25 41
E120	TRUE	BKL_FB	
E120	TRUE	BKL_GD	
E120	TRUE	BKL_SW	
E130	TRUE	BKLT_EN	85
E130	TRUE	BKL_SCL	
E130	TRUE	BKL_SDA	
E130	TRUE	LCD_BKLT_PWM	84 85

ICT Test Points

CPU FSB NO_TESTs

NO_TEST

	TRUE	FSB_A_L<31..3>	10 14 88
	TRUE	FSB_ADS_L	10 14 88
	TRUE	FSB_ADSTB_L<1..0>	10 14 88
	TRUE	FSB_D_L<63..0>	10 14 88
	TRUE	FSB_DBSY_L	10 14 88
	TRUE	FSB_DINV_L<3..0>	10 14 88
	TRUE	FSB_DRDY_L	10 14 88
	TRUE	FSB_DSTB_L_N<3..0>	10 14 88
	TRUE	FSB_DSTB_L_P<3..0>	10 14 88
	TRUE	FSB_HIT_L	10 14 88
	TRUE	FSB_HITM_L	10 14 88
	TRUE	FSB_LOCK_L	10 14 88
	TRUE	FSB_REQ_L<4..0>	10 14 88

FB NO_TESTs

NO_TEST

J89	TRUE	FB_A_DQ<63..0>	71 72 79 95
J89	TRUE	FB_B_DQ<63..0>	71 73 80 95
J89	TRUE	FB_B_BA<1>	71 73 80 95
J89	TRUE	FB_B_CAS_L	71 73 80 95
J89	TRUE	FB_B_CS0_L	71 73 95
J89	TRUE	FB_B_MA<11>	71 73 80 95

LVDS NO_TESTs

NO_TEST

J125	TRUE	LVDS_A_DATA_N<0>	81 84 95
J125	TRUE	LVDS_A_DATA_P<0>	81 84 95
J125	TRUE	LVDS_B_CLK_P	81 84 95
J125	TRUE	LVDS_B_DATA_N<0>	81 84 95
J125	TRUE	LVDS_B_DATA_P<0>	81 84 95
J125	TRUE	LVDS_EG_A_DATA_N<2>	76 84 95

NC NO_TESTs

NO_TEST

J126	TRUE	NC_SMC_FAN_3_TACH	42
J761	TRUE	NC_SMC_FAN_3_CTL	42
J762	TRUE	NC_SMC_FAN_2_TACH	42
J763	TRUE	NC_SMC_FAN_2_CTL	42
J764	TRUE	NC_FW2_TPBP	37
J765	TRUE	NC_FW2_TPBN	37
J767	TRUE	NC_FW2_TPBIAS	37
J766	TRUE	NC_FW2_TPAP	37
J769	TRUE	NC_FW2_TPAN	37
J768	TRUE	NC_FW0_TPBP	37
J770	TRUE	NC_FW0_TPBN	37
J772	TRUE	NC_FW0_TPAP	37
J771	TRUE	NC_ESTARLDO_EN	42
J774	TRUE	NC_ALS_GAIN	42

NC NO_TESTs

NO_TEST

9	TP_CPU_PECI_MCP		TRUE	NC_CPU_PECI_MCP	
10	TP_CPU_TEST3		TRUE	NC_CPU_TEST3	
18	TP_ENET_INTR_L		TRUE	NC_ENET_INTR_L	
18	TP_ENET_PWRDWN_L		TRUE	NC_ENET_PWRDWN_L	
35	TP_FW643_AVREG		TRUE	NC_FW643_AVREG	
35	TP_FW643_TDI		TRUE	NC_FW643_TDI	
9	TP_MEM_A_A<15>		TRUE	NC_MEM_A_A<15>	
16	TP_MEM_A_CKE<2>		TRUE	NC_MEM_A_CKE<2>	
16	TP_MEM_A_CKE<3>		TRUE	NC_MEM_A_CKE<3>	
15	TP_MEM_A_CLK2N		TRUE	NC_MEM_A_CLK2N	
15	TP_MEM_A_CLK2P		TRUE	NC_MEM_A_CLK2P	
16	TP_MEM_A_CLK3N		TRUE	NC_MEM_A_CLK3N	
16	TP_MEM_A_CLK3P		TRUE	NC_MEM_A_CLK3P	
16	TP_MEM_A_CLK4N		TRUE	NC_MEM_A_CLK4N	
16	TP_MEM_A_CLK4P		TRUE	NC_MEM_A_CLK4P	
16	TP_MEM_A_CLK5N		TRUE	NC_MEM_A_CLK5N	
16	TP_MEM_A_CLK5P		TRUE	NC_MEM_A_CLK5P	
16	TP_MEM_A_CS_L<2>		TRUE	NC_MEM_A_CS_L<2>	
16	TP_MEM_A_CS_L<3>		TRUE	NC_MEM_A_CS_L<3>	
16	TP_MEM_A_ODT<2>		TRUE	NC_MEM_A_ODT<2>	
16	TP_MEM_A_ODT<3>		TRUE	NC_MEM_A_ODT<3>	
9	TP_MEM_B_A<15>		TRUE	NC_MEM_B_A<15>	
16	TP_MEM_B_CKE<2>		TRUE	NC_MEM_B_CKE<2>	
15	TP_MEM_B_CLK2P		TRUE	NC_MEM_B_CLK2P	
16	TP_MEM_B_CLK3N		TRUE	NC_MEM_B_CLK3N	
16	TP_MEM_B_CLK3P		TRUE	NC_MEM_B_CLK3P	
16	TP_MEM_B_CLK4N		TRUE	NC_MEM_B_CLK4N	
16	TP_MEM_B_CLK4P		TRUE	NC_MEM_B_CLK4P	
16	TP_MEM_B_CLK5N		TRUE	NC_MEM_B_CLK5N	
16	TP_MEM_B_CLK5P		TRUE	NC_MEM_B_CLK5P	
16	TP_MEM_B_CS_L<2>		TRUE	NC_MEM_B_CS_L<2>	
16	TP_MEM_B_CS_L<3>		TRUE	NC_MEM_B_CS_L<3>	
16	TP_MEM_B_ODT<2>		TRUE	NC_MEM_B_ODT<2>	
16	TP_MEM_B_ODT<3>		TRUE	NC_MEM_B_ODT<3>	
21	TP_MLB_RAM_SIZE		TRUE	NC_MLB_RAM_SIZE	
21	TP_MLB_RAM_VENDOR		TRUE	NC_MLB_RAM_VENDOR	
74	TP_GPU_BUFRST_L		TRUE	NC_GPU_BUFRST_L	
75	TP_GPU_GSTATE<0>		TRUE	NC_GPU_GSTATE<0>	
75	TP_GPU_GSTATE<1>		TRUE	NC_GPU_GSTATE<1>	
75	TP_GPU_MIOA_D<9..0>		TRUE	NC_GPU_MIOA_D<9..0>	
75	TP_GPU_MIOA_DE		TRUE	NC_GPU_MIOA_DE	
74	TP_GPU_PGOOD_OUT_L		TRUE	NC_GPU_PGOOD_OUT_L	
75	TP_GPU_VCORE_VID3		TRUE	NC_GPU_VCORE_VID3	
19	TP_LPC_DRQ0_L		TRUE	NC_LPC_DRQ0_L	
75	TP_LVDS_EG_B_CLK_N		TRUE	NC_LVDS_EG_B_CLK_N	
75	TP_LVDS_EG_B_CLK_P		TRUE	NC_LVDS_EG_B_CLK_P	
75	TP_LVDS_EG_BKL_PWM		TRUE	NC_LVDS_EG_BKL_PWM	
9	TP_LVDS_IG_B_CLKN		TRUE	NC_LVDS_IG_B_CLKN	
9	TP_LVDS_IG_B_CLKP		TRUE	NC_LVDS_IG_B_CLKP	
9	TP_LVDS_IG_BKL_PWM		TRUE	NC_LVDS_IG_BKL_PWM	
21	TP_MCP_BUF_SIO_CLK		TRUE	NC_MCP_BUF_SIO_CLK	
17	TP_MCP_GPIO_18		TRUE	NC_MCP_GPIO_18	
21	TP_MCP_KBDRSTIN_L		TRUE	NC_MCP_KBDRSTIN_L	
20	TP_MCP_SATALED_L		TRUE	NC_MCP_SATALED_L	

NC NO_TESTs

NO_TEST

19	TP_PCI_AD<31..8>		TRUE	NC_PCI_AD<31..8>	
19	TP_PCI_C_BE_L<3..0>		TRUE	NC_PCI_C_BE_L<3..0>	
19	TP_PCI_CLK0		TRUE	NC_PCI_CLK0	
19	TP_PCI_CLK1		TRUE	NC_PCI_CLK1	
19	TP_PCI_DEVSEL_L		TRUE	NC_PCI_DEVSEL_L	
19	TP_PCI_FRAME_L		TRUE	NC_PCI_FRAME_L	
19	TP_PCI_GNT0_L		TRUE	NC_PCI_GNT0_L	
19	TP_PCI_GNT1_L		TRUE	NC_PCI_GNT1_L	
19	TP_PCI_INTW_L		TRUE	NC_PCI_INTW_L	
19	TP_PCI_INTX_L		TRUE	NC_PCI_INTX_L	
19	TP_PCI_INTY_L		TRUE	NC_PCI_INTY_L	
19	TP_PCI_INTZ_L		TRUE	NC_PCI_INTZ_L	
19	TP_PCI_IRDY_L		TRUE	NC_PCI_IRDY_L	
19	TP_PCI_PAR		TRUE	NC_PCI_PAR	
19	TP_PCI_PERR_L		TRUE	NC_PCI_PERR_L	
19	TP_PCI_RESET1_L		TRUE	NC_PCI_RESET1_L	
19	TP_PCI_SERR_L		TRUE	NC_PCI_SERR_L	
19	TP_PCI_STOP_L		TRUE	NC_PCI_STOP_L	
19	TP_PCI_TRDY_L		TRUE	NC_PCI_TRDY_L	
17	TP_PCIE_CLK100M_PE4P		TRUE	NC_PCIE_CLK100M_PE4P	
17	TP_PCIE_CLK100M_PE5N		TRUE	NC_PCIE_CLK100M_PE5N	
17	TP_PCIE_CLK100M_PE5P		TRUE	NC_PCIE_CLK100M_PE5P	
17	TP_PCIE_CLK100M_PE6N		TRUE	NC_PCIE_CLK100M_PE6N	
17	TP_PCIE_CLK100M_PE6P		TRUE	NC_PCIE_CLK100M_PE6P	
17	TP_PCIE_PE4_D2RN		TRUE	NC_PCIE_PE4_D2RN	
17	TP_PCIE_PE4_D2RP		TRUE	NC_PCIE_PE4_D2RP	
17	TP_PE4_CLKREQ_L		TRUE	NC_PE4_CLKREQ_L	
69	TP_PEX_CLKREQ_L		TRUE	NC_PEX_CLKREQ_L	
49	TP_PSOC_P1_3		TRUE	NC_PSOC_P1_3	
20	TP_SATA_C_D2RN		TRUE	NC_SATA_C_D2RN	
20	TP_SATA_C_D2RP		TRUE	NC_SATA_C_D2RP	
20	TP_SATA_C_R2D_CN		TRUE	NC_SATA_C_R2D_CN	
20	TP_SATA_C_R2D_CP		TRUE	NC_SATA_C_R2D_CP	
20	TP_SATA_D_D2RN		TRUE	NC_SATA_D_D2RN	
20	TP_SATA_D_D2RP		TRUE	NC_SATA_D_D2RP	
20	TP_SATA_D_R2D_CN		TRUE	NC_SATA_D_R2D_CN	
20	TP_SATA_D_R2D_CP		TRUE	NC_SATA_D_R2D_CP	
20	TP_SATA_E_D2RN		TRUE	NC_SATA_E_D2RN	
20	TP_SATA_E_D2RP		TRUE	NC_SATA_E_D2RP	
20	TP_SATA_E_R2D_CN		TRUE	NC_SATA_E_R2D_CN	
20	TP_SATA_E_R2D_CP		TRUE	NC_SATA_E_R2D_CP	
20	TP_SATA_F_D2RN		TRUE	NC_SATA_F_D2RN	
20	TP_SATA_F_D2RP		TRUE	NC_SATA_F_D2RP	
20	TP_SATA_F_R2D_CN		TRUE	NC_SATA_F_R2D_CN	
20	TP_SATA_F_R2D_CP		TRUE	NC_SATA_F_R2D_CP	
21	TP_SB_A20GATE		TRUE	NC_SB_A20GATE	
42	TP_SMC_P41		TRUE	NC_SMC_P41	
20	TP_USB_10P		TRUE	NC_USB_10P	
20	TP_USB_11N		TRUE	NC_USB_11N	
20	TP_USB_11P		TRUE	NC_USB_11P	
9	TP_USB_EXTDN		TRUE	NC_USB_EXTDN	
9	TP_USB_EXTDP		TRUE	NC_USB_EXTDP	
9	TP_USB_MININ		TRUE	NC_USB_MININ	
9	TP_USB_MINIP		TRUE	NC_USB_MINIP	
13	TP_XDP_OBSDATA_B2		TRUE	NC_XDP_OBSDATA_B2	
13	TP_XDP_OBSDATA_B3		TRUE	NC_XDP_OBSDATA_B3	

Functional / ICT Test

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 7 OF 123	

"G3Hot" (Always-Present) Rails

60 =PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=6V
MAKE_BASE=TRUE
7 45
=PPVIN_S5_P5VP3V3 62
=PPVIN_S0_CPUVTTS0 65
=PPBUS_S0_LCDBKLT 86
=PPVIN_GPU_GPUVCORE 77
=PPVIN_S5_CPU_IMVP_ISNS_R 45
=PPVIN_S0_P5VRTS0_MCPCORE 64
=PPVIN_S3_DDRREG 63
=PPVIN_S0GPU_P1V8P1V1 83
=PPVBAT_G3H_P3V42G3H 59
=PPVIN_S0_P1V05S5 66
=PPVIN_S0_KBDLED 50
=PPVIN_S5_FWPWRSW 36
=PPVIN_S5_BKL 37

45 =PPVIN_S5_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
7
=PPVIN_S5_CPU_IMVP 61

59 =PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
7
=PPDCIN_S5_CHGR 60

59 =PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
7 42
=PP3V42_G3H_SMCUSBMUX 39
=PP3V42_G3H_SMBUS_SMC_BSA 44
=PP3V42_G3H_LIDSWITCH 40
=PP3V3_S5_SMC 41 42 51
=PP3V3_S5_LPCPLUS 43
=PPVIN_S5_SMCVREF 42
=PP3V42_G3H_PWRCTL 67
=PP3V42_G3H_CHGR 60
=PP3V3_S5_RTC_D 25
=PP3V42_G3H_BATT 59
=PP3V42_G3H_TPAD 49
=PP3V42_G3H_BMON_ISNS 45
=PP3V42_G3H_CPUCOREISNS 45

5V Rails

62 =PP5V_S3_REG
PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
7
=PP5V_S3_SYSLED 42
=PP5V_S3_BTCAMERA 30
=PP5V_S3_WLAN 30
=PP5V_S3_IR 40
=PP5V_S3_DDRREG 63
=PP5V_S3_GPUVCORE 77
=PP5V_S3_RTUSB 39 98
=PP5V_S3_TPAD 50
=PP5V_S3_P1V05S0FET 68
=PP5V_S3_MCPDDRFET 68
=PP5V_S3_VTTCLAMP 68
=PP5V_S3_AUDIO_PWR 9

64 =PP5V_S0_REG
PP5V_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V
MAKE_BASE=TRUE
7
=PP5V_S0_FAN_LT 7 48
=PP5V_S0_FAN_RT 48
=PP5V_S0_CPU_IMVP 61
=PP5V_S0_CPUVTTS0 65
=PP5V_S0GPU_P1V1P1V8_GPU 83
=PP5V_S0_LPCPLUS 43
=PP5V_S0_ODD 38
=PP5V_S0_HDD 38

Chipset "VCore" Rails

61 =PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
7
=PPVCORE_S0_CPU 11 12 45

64 =PPMCPCORE_S0_REG
PPVCORE_S0_MCP
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
=PPVCORE_S0_MCP 22 23 45

3.3V-2.5V Rails

62 =PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
7 96
=PP3V3_S5_ROM 43 52
=PP3V3_S5_MEMRESET 29
=PP3V3_S3_P3V3S3FET 68
=PP3V3_S0_LCD 78
=PP3V3_S0_P3V3S0FET 68
=PP3V3_GPU_P3V3GPUFET 68
=PP3V3_S5_PWRCTL 67
=PP3V3_S5_P1V05FET 68
=PP3V3_S5_MCP 22 23
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_FW_LATEVG_ACTIVE 36
=PP3V3_S5_MCPPWRGD 25
=PP3V3_FW_LATEVG 37
=PP3V3_S5_P1V05ENETFET 33
=PP3V3_S5_P3V3ENETFET 33
=PP3V3_S5_DP_PORT_PWR 82

68 =PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
7
=PP3V3_S3_GMUX 84
=PP3V3_S3_BT 30
=PP3V3_S3_P1V8S0 66
=PP3V3_S3_SMBUS_SMC_A_S3 44
=PP3V3_S3_SMS 8 51
=PP3V3_S3_TPAD 49
=PP3V3_S3_SMS 8 51
=PP3V3_S3_WLAN 30
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_VREFMRGN 26
=PP3V3_S3_SMBUS_SMC_MGMT 44
=PP3V3_S3_EXCARD 31
=PP3V3_S3_P1V5EXPS0 66

68 =PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
7 9 96
=PP3V3_S0_LPCPLUS 43
=PP3V3_S0_SMC 42
=PP3V3_S0_SMBUS_SMC_B_S0 44
=PP3V3_S0_MCPDDRISNS 46
=PP3V3_S0_GPU1V8ISNS 46
=PP3V3_S0_CPUTHMSNS 47
=PP3V3_S0_GPUTHMSNS 47
=PP3V3_S0_FAN_LT 48
=PP3V3_S0_FAN_RT 48
=PP3V3_S0_IMVP 61
=PP3V3_S0_PWRCTL 67
=PP3V3_S0_DDC_LCD 7 75 78
=PP3V3_S0_XDP 6 8 13
=PP3V3_S0_MCPCOREISNS 46
=PP3V3_S0_XDP 6 8 13
=PPSPD_S0_MEM_A 27
=PPSPD_S0_MEM_B 28
=PP3V3_S0_SMBUS_MCP_0 44
=PP3V3_S0_GMUX 84
=PP3V3_S0_DPMUX 81
=PP3V3_S0_DPCONN 82
=PP3V3_S0_P1V2P2V5 87
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3_S0_HDCPROM 24
=PP3V3R1V5_S0_MCP_HDA 21 23
=PP3V3_S0_MCP_PLL_UF 23
=PP3V3_S0_MCP_VPLL_UF 24
=PP3V3_S0_MCP_DAC_UF 24
=PP3V3_S0_MCP 21 22 23
=PP3V3_S0_AUDIO 53 57 58
=PP3V3_S0_ODD 38
=PP3V3_S0_VMON 67
=PP3V3_S0_SMBUS_MCP_1 44
=PP3V3_S0_REMTHMSNS 47
=PP3V3_S0_EXCARD 31
=PP3V3_S0_LVDSDDCMUX 81
=PP3V3_S0_BATTCHARGERTMPSNSR 47
=PP3V3_GPU_SMBUS_SMC_0_S0 44
=PP3V3_S0_TPAD 50
=PP3V3_S0_MCP_PLL_VLDO 66
=PP3V3_FW_FWPHY 35 37
=PP3V3_FW_P1V0FW 66

87 =PP2V5_S0_REG
PP2V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=2.5V
MAKE_BASE=TRUE
7
=PP2V5_S0_GMUX 84

87 =PP1V2_S0_REG
PP1V2_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
7
=PP1V2_S0_GMUX 84

1.8V/DDR 1.5V Rails

66 =PP1V8_S0_REG
500 mA max supply
PP1V8_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
7
190 mA =PP3V3R1V8_S0_MCP_IFP_VDD 18 24
=PP1V8_S0_MCP_PLL_VLDO 66

63 =PPDDR_S3_REG
PP1V8R1V5_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
7
=PP1V8R1V5_S0_MCP_FET 68
=PPVIN_S0_DDRREG_LDO 63
=PP1V5_S3_MEM_A 27
=PP1V5_S3_MEM_B 28
=PP1V5_S3_MEMRESET 29

68 =PP1V8R1V5_S0_FET
PP1V8R1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
7
4771 mA =PPMCPDDR_ISNS_R 46
130 mA =PP1V5_S0_CPU 11 12
500 mA =PP1V5_S0_VMON 67

66 =PP1V5_EXP_S0
PP1V5_EXP_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_EXCARD 31

23 16 =PP1V8R1V5_S0_MCP_MEM
PPMCPDDR_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
7
=PP1V5_S0_MEM_A 27
=PP1V5_S0_MEM_B 28
=PPMCPDDR_ISNS 46

68 66 =PP1V05_S0_FET
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
=PP1V05_S0_MCP_AVDD_UF 23
1034 mA =PP1V05_S0_MCP_PEX_DVDD 8 23
=PP1V05_S0_MCP_SATA_DVDD 8 23
=PP1V05_S0_MCP_HDMI_VDD 18 24
=PP1V05_S0_VMON 67
=PP1V05_S0_MCP_PLL_PEX_UF 23

PP1V05_S0_MCP_PLL_UF
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_S0_MCP_PLL_UF 23 66

23 8 =PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PEX_DVDD0 17
=PP1V05_S0_MCP_PEX_DVDD1 17

23 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PEX_AVDD0 17
=PP1V05_S0_MCP_PEX_AVDD1 17

23 8 =PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_SATA_DVDD0 20

23 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_SATA_AVDD0 20

66 =PP1V05_S5_MCP
PP1V2R1V05_S5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
(1.1V for A01)
7
241 mA max load
105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC 22 23
139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET 33
=PP1V05_S5_P1V05S0FET 68

65 =PPCPUVTT_S0_REG
PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
5300 mA
4500 mA =PP1V05_S0_CPU 6 10 11 12 13 61
=PP1V05_S0_SMC_LS 42
1182 mA =PP1V05_S0_MCP_FSB 9 14 22 23

63 26 =PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE
7

63 =PPVTT_S0_DDR_LDO
PP0V9R0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
7
=PP0V75_S0_MEM_VTT_A 27
=PP0V75_S0_MEM_VTT_B 28
=PPVTT_S0_VTTCLAMP 68
OR 0.75V

ENET Rails

33 =PP1V05_ENET_FET
PP1V2R1V05_ENET
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
=PP1V05_ENET_MCP_PLL_MAC 23
=PP1V05_ENET_MCP_RMGT 18 23
=PP1V05_ENET_PHY 32

33 =PP3V3_ENET_FET
PP3V3_ENET_PHY
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
7
=PP3V3_ENET_MCP_RMGT 18 23
=PP3V3_ENET_PHY 32

"FW" (FireWire) Rails

36 =PPVOUT_FW_FWPWRSW
PPBUS_FW_FWBOOST
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=6V
MAKE_BASE=TRUE
=PPVIN_PFWBOOST 66

66 =PFWBOOST_REG
PP10V_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=10V
MAKE_BASE=TRUE
=PPBOOST_FW_FWPWRSW_F 36

36 =PPBOOST_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=10V
MAKE_BASE=TRUE
7
=PPVP_FW_PORT1 37
=PPVP_FW_PHY_CPS_FET 37

66 =PP1V0_FW_REG
PP1V0_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE
7
=PP1V0_FW_FWPHY 35

"GPU" Rails

68 =PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
7
=PP3V3_GPU_VDD33 6 74 75
=PP3V3_GPU_MIO 74 75
=PP3V3_GPU_LVDS_DDC 81
=PP3V3_GPU_PWRCTL 67
=PP3V3_GPU_VCORELOGIC 77
=PP3V3_GPU_P1V8S0 66

83 =PP1V1_S0GPU_REG
PP1V1_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.1V
MAKE_BASE=TRUE
7
=PP1V1_GPU_PEX_IOVDDQ 69
=PP1V1_GPU_PEX_IOVDD 69
=PP1V1_GPU_PEX_PLLXVDD 69
=PP1V1_GPU_PLLVDD 74
=PP1V1_GPU_H_PLLVDD 74
=PP1V1_GPU_VID_PLLVDD 74
=PP1V1_GPU_FBPLLAVDD 71
=PP1V1_GPU_IFPCD_IOVDD 76

66 =PP1V8_GPUIFPX_REG
PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
7
=PP1V8_GPU_IFPX 76

46 =PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
7
=PP1V8_GPU_FB_VDD 72 73 79 80
=PP1V8_GPU_FB_VDDQ 9 72 73 79 80
=PP1V8_GPU_FBVDDQ 70
=PP1V8_GPU_FBIO 71

77 45 =PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE
7
=PPVCORE_GPU 70

83 =PP1V8_GPU_REG
PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
7
=PP1V8_S0GPU_ISNS_R 46

Power Aliases

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 8 OF 123	

Thermal Module Holes

ZT0982 STDOFF-4.5OD.98H-1.1-3.48-TH — Left CPU TM Hole
ZT0983 STDOFF-4.5OD.98H-1.1-3.48-TH — Right CPU TM Hole
ZT0984 STDOFF-4.5OD.98H-1.1-3.48-TH — Top GPU Right TM Hole
ZT0980 STDOFF-4.5OD.98H-1.1-3.48-TH — Bottom Left GPU TM Hole
ZT0981 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0985 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0986 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0930 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0987 STDOFF-4.5OD.98H-1.1-3.48-TH

Frame Holes

ZT0915 3R2P5 — GND_BATT_CHGND
ZT0945 3R2P5 — GND_CHASSIS_USB
ZT0932 3R2P5 — GND_CHASSIS_RIGHTHS
ZT0960 3R2P5 — GND_CHASSIS_SATA
ZT0971 3R2P5 — GND_CHASSIS_TPAD
ZT0965 3R2P5 — GND_CHASSIS_CLUTCH
ZT0940 3R2P5 — GND_CHASSIS_LVDS
ZT0970 3R2P5 — GND_CHASSIS_DIMM

ZT0931 STDOFF-4.0OD3.0H-SM
ZT0934 STDOFF-4.0OD3.0H-SM

ZT0988 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0989 STDOFF-4.5OD.98H-1.1-3.48-TH
ZT0991 STDOFF-4.5OD.98H-1.1-3.48-TH

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

23 22 14 8 =PP1V05_S0_MCP_FSB

NO STUFF R0950 220 5% 1/16W MF-LF 402
NO STUFF R0970 200 5% 1/16W MF-LF 402
NO STUFF R0960 62 5% 1/16W MF-LF 402
NO STUFF R0990 150 1% 1/16W MF-LF 402
NO STUFF R0980 150 1% 1/16W MF-LF 402

88 61 14 10 OUT CPU_DPRSTP_L
88 14 10 OUT FSB_BREQ0_L
88 14 13 10 OUT FSB_CPURST_L
88 14 10 OUT CPU_INTR
88 14 10 OUT CPU_NMI

Bosses for Flex Protector Bracket

ZT0957 4.0OD1.65H-M1.6X0.35
ZT0958 4.0OD1.65H-M1.6X0.35

80 79 73 72 8 =PP1V8_GPU_FB_VDDQ
R0900 10 1% 1/16W MF-LF 402
R0901 10 1% 1/16W MF-LF 402
GPU_FB_A_VREF_DIV — 26
=PP1V8_GPU_FB_VREF_A — 72
GPU_FB_B_VREF_DIV — 26
=PP1V8_GPU_FB_VREF_B — 73

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0901 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
SH0924 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0917 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0918 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0919 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0930 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0921 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0931 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0922 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0932 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0934 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0933 2.0DIA-TALL-EMI-MLB-M97-M98 SM
SH0935 2.0DIA-TALL-EMI-MLB-M97-M98 SM

CPU signals

TP_IMVP6_CLKEN_L — VR_PWRGD_CLKEN_L (MAKE_BASE=TRUE) — 61
88 11 CPU_VID<0..6> — IMVP6_VID<0..6> — 61 88
88 10 CPU_BSEL<0..2> — =MCP_BSEL<0..2> — 14
25 MEM_VTT_EN — =DDRVTT_EN — 63 68
TP_SPI_CS1_R_L_USE_MLB — =SPI_CS1_R_L_USE_MLB — 21 43

GPU signals

90 69 PEG_D2R_P<0..15> — =PEG_D2R_P<0..15> — 17
90 69 PEG_D2R_N<0..15> — =PEG_D2R_N<0..15> — 17
90 69 PEG_R2D_C_P<0..15> — =PEG_R2D_C_P<0..15> — 17
90 69 PEG_R2D_C_N<0..15> — =PEG_R2D_C_N<0..15> — 17

84 LCD_BKLT_EN — LVDS_BKL_ON — 86
90 81 DP_IG_ML_P<3> — =MCP_HDMI_TXC_P — 18
90 81 DP_IG_ML_N<3> — =MCP_HDMI_TXC_N — 18
90 81 DP_IG_ML_P<2..0> — =MCP_HDMI_TXD_P<0..2> — 18
90 81 DP_IG_ML_N<2..0> — =MCP_HDMI_TXD_N<0..2> — 18
81 75 DP_IG_DDC_CLK — =MCP_HDMI_DDC_CLK — 18
81 75 DP_IG_DDC_DATA — =MCP_HDMI_DDC_DATA — 18
85 DP_IG_HPD — =MCP_HDMI_HPD — 18

GMUX ALIASES

67 PM_ALL_GPU_PGOOD — ALL_EG_PGOOD — 84
TP_LVDS_MUX_SEL_EG — LVDS_MUX_SEL_EG — 84
84 EG_RESET_L — GPU_RESET_L — 69

84 6 JTAG_GMUX_TDI — GMUX_JTAG_TDI — 19
84 6 JTAG_GMUX_TMS — GMUX_JTAG_TMS — 19
84 6 JTAG_GMUX_TDO — GMUX_JTAG_TDO — 17
84 GMUX_INT — =DVI_HPD_GMUX_INT — 18
18 LVDS_IG_BKL_ON — IG_BKLT_EN — 84
18 LVDS_IG_PANEL_PWR — IG_LCD_PWR_EN — 84

=PP1V05_S0_MCP_SATA_DVDD1 — 20
=PP1V05_S0_MCP_SATA_AVDD1 — 20

66 =P1V5_EXP_S0_EN — PP3V3_S0 — 7 8 96

MCP_MII_PD (MAKE_BASE=TRUE)
R0930 47K 5% 1/16W MF-LF 402
=MCP_MII_RXER — 18
=MCP_MII_CRS — 18
=MCP_MII_COL — 18

Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V)

7 TP_USB_EXTDP — USB_EXTD_P — 20 91
7 TP_USB_EXTDN — USB_EXTD_N — 20 91
7 TP_USB_MINIP — USB_MINI_P — 20 91
7 TP_USB_MININ — USB_MINI_N — 20 91
7 TP_MEM_A_A<15> — MEM_A_A<15> — 27
7 TP_MEM_B_A<15> — MEM_B_A<15> — 28
7 TP_CPU_PECI_MCP — CPU_PECI_MCP — 14

7 TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P — 18 90
7 TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N — 18 90
7 TP_LVDS_IG_BKL_PWM — LVDS_IG_BKL_PWM — 18

NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3> — 18 90
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3> — 18 90
NC_LVDS_IG_B_DATAP<3> — LVDS_IG_B_DATA_P<3> — 18 90
NC_LVDS_IG_B_DATAN<3> — LVDS_IG_B_DATA_N<3> — 18 90

AUDIO ALIASES

53 HDA_BITCLK — HDA_BIT_CLK — 21 91

8 =PP5V_S3_AUDIO_PWR
XW0900 SM — PP5V_S3_AUDIO — 53 55 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V
XW0901 SM — PP5V_S3_AUDIO_AMP — 56 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V
R0902 10K 5% 1/16W MF-LF 402
AUD_IPHS_SWITCH_EN — 19 58

R0903 0 5% 1/16W MF-LF 402
21 MCP_SPKR — SMC_MCP_SAFE_MODE — 41

ETHERNET ALIASES

33 =P3V3ENET_EN — PM_SLP_RMGT_L — 21
33 =P1V05ENET_EN
32 =PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
32 =RTL8211_REGOUT — NC_RTL8211_REGOUT
=RTL8211_ENSWREG — 32

MCP79 PCIe PRSNT# Straps

R0925 0 5% 1/16W MF-LF 402 — PCIE_FW_PRSNT_L — OUT 17
NO STUFF
R0927 0 5% 1/16W MF-LF 402 — PEG_PRSNT_L — OUT 17
R0926 0 5% 1/16W MF-LF 402 — EG_CLKREQ_OUT_L — IN 84

Signal Aliases

SYNC_MASTER=K20_MLB — SYNC_DATE=09/24/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 9 OF 123	

OMIT

U1000
PENRYN
FCBGA
1 OF 4

ADDR GROUP0
FSB_A_L<3> J4 A3*
FSB_A_L<4> L5 A4*
FSB_A_L<5> L4 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M3 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L2 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> M1 ADSTB0*

REQ
FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> M2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L1 REQ4*

ADDR GROUP1
FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U1 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W2 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> U2 A30*
FSB_A_L<31> V4 A31*
FSB_A_L<32> W3 A32*
FSB_A_L<33> AA4 A33*
FSB_A_L<34> AB2 A34*
FSB_A_L<35> AA3 A35*
FSB_ADSTB_L<1> V1 ADSTB1*

ICH
CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

RESERVED
TP_CPU_RSVD0 M4 RSVD0
TP_CPU_RSVD1 N5 RSVD1
TP_CPU_RSVD2 T2 RSVD2
TP_CPU_RSVD3 V3 RSVD3
TP_CPU_RSVD4 B2 RSVD4
TP_CPU_RSVD5 F6 RSVD5
TP_CPU_RSVD6 D2 RSVD6
TP_CPU_RSVD7 D22 RSVD7
TP_CPU_RSVD8 D3 RSVD8

CONTROL
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 CPU_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* C1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

XDP/ITP SIGNALS
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERMAL
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC B25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

H CLK
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
0.5" MAX LENGTH FOR CPU_GTLREF
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

OMIT

U1000
PENRYN
FCBGA
2 OF 4

DATA GRP 0
D0* E22 FSB_D_L<0>
D1* F24 FSB_D_L<1>
D2* E26 FSB_D_L<2>
D3* G22 FSB_D_L<3>
D4* F23 FSB_D_L<4>
D5* G25 FSB_D_L<5>
D6* E25 FSB_D_L<6>
D7* E23 FSB_D_L<7>
D8* K24 FSB_D_L<8>
D9* G24 FSB_D_L<9>
D10* J24 FSB_D_L<10>
D11* J23 FSB_D_L<11>
D12* H22 FSB_D_L<12>
D13* F26 FSB_D_L<13>
D14* K22 FSB_D_L<14>
D15* H23 FSB_D_L<15>
DSTBN0* J26 FSB_DSTB_L_N<0>
DSTBP0* H26 FSB_DSTB_L_P<0>
DINV0* H25 FSB_DINV_L<0>

DATA GRP 1
D16* N22 FSB_D_L<16>
D17* K25 FSB_D_L<17>
D18* P26 FSB_D_L<18>
D19* R23 FSB_D_L<19>
D20* L23 FSB_D_L<20>
D21* M24 FSB_D_L<21>
D22* L22 FSB_D_L<22>
D23* M23 FSB_D_L<23>
D24* P25 FSB_D_L<24>
D25* P23 FSB_D_L<25>
D26* P22 FSB_D_L<26>
D27* T24 FSB_D_L<27>
D28* R24 FSB_D_L<28>
D29* L25 FSB_D_L<29>
D30* T25 FSB_D_L<30>
D31* N25 FSB_D_L<31>
DSTBN1* L26 FSB_DSTB_L_N<1>
DSTBP1* M26 FSB_DSTB_L_P<1>
DINV1* N24 FSB_DINV_L<1>

DATA GRP 2
D32* Y22 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* V23 FSB_D_L<36>
D37* T22 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U23 FSB_D_L<39>
D40* Y25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* W24 FSB_D_L<43>
D44* W25 FSB_D_L<44>
D45* AA23 FSB_D_L<45>
D46* AA24 FSB_D_L<46>
D47* AB25 FSB_D_L<47>
DSTBN2* Y26 FSB_DSTB_L_N<2>
DSTBP2* AA26 FSB_DSTB_L_P<2>
DINV2* U22 FSB_DINV_L<2>

DATA GRP 3
D48* AE24 FSB_D_L<48>
D49* AD24 FSB_D_L<49>
D50* AA21 FSB_D_L<50>
D51* AB22 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC26 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AC25 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AC22 FSB_D_L<60>
D61* AD23 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AC23 FSB_D_L<63>
DSTBN3* AE25 FSB_DSTB_L_N<3>
DSTBP3* AF24 FSB_DSTB_L_P<3>
DINV3* AC20 FSB_DINV_L<3>

MISC
GTLREF AD26
TEST1 C23
TEST2 D25
TEST3 C24
TEST4 AF26
TEST5 AF1
TEST6 A26
TEST7 C3
BSEL0 B22
BSEL1 B23
BSEL2 C21

COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 AA1 CPU_COMP<2>
COMP3 Y1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_CPUSLP_L
PSI* AE6 CPU_PSI_L

R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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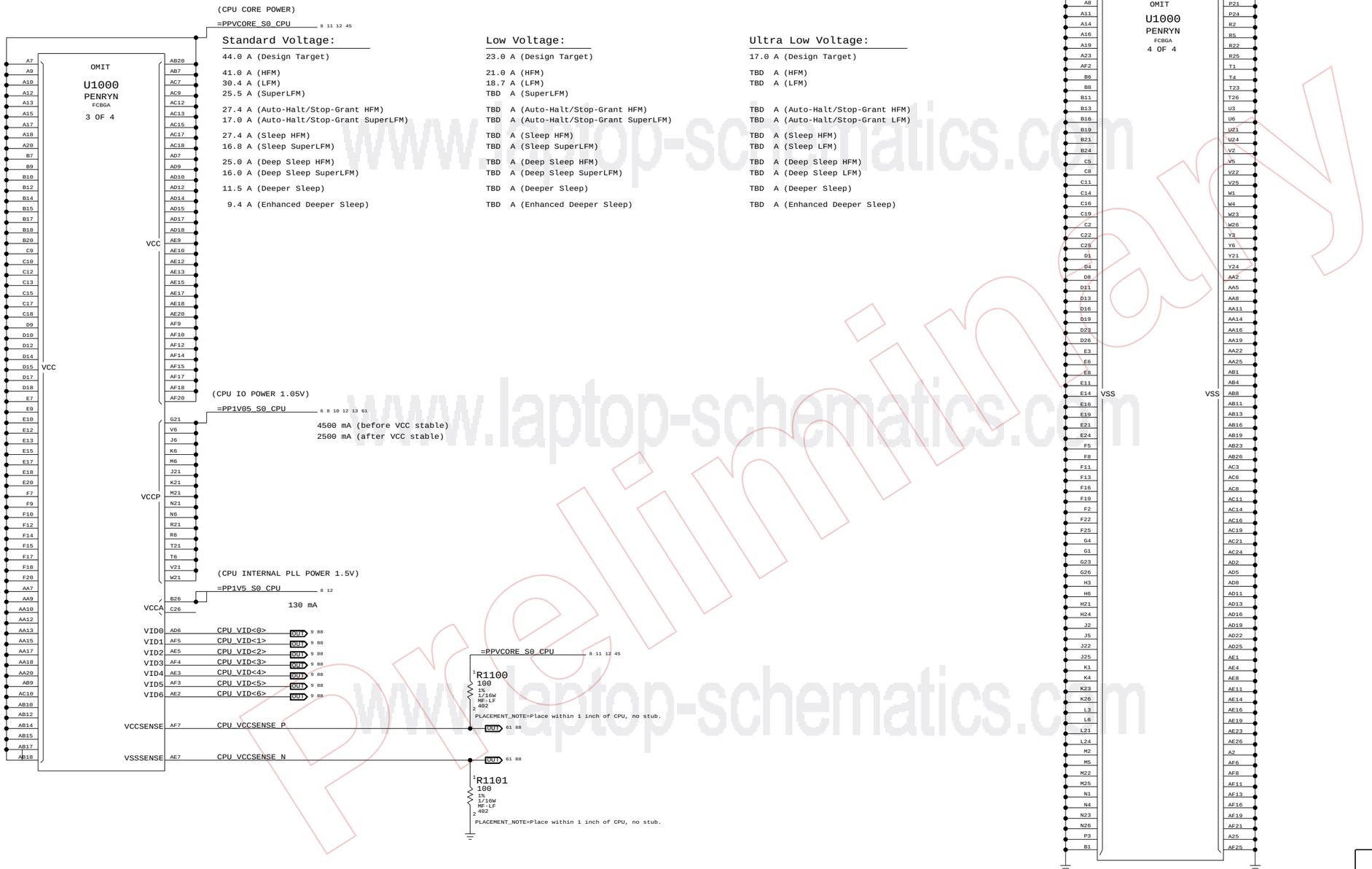
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 10 OF 123	



Current numbers from Merom for Santa Rosa EMTS, doc #22221.

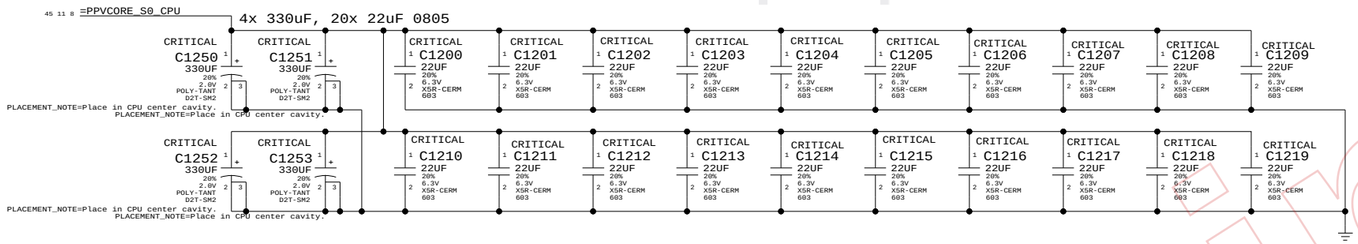
CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

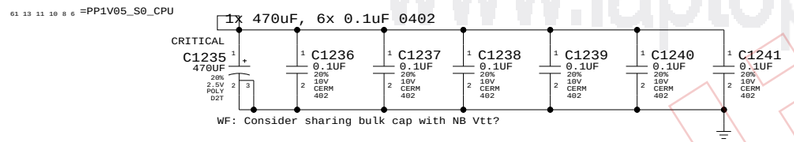
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 11 OF 123	

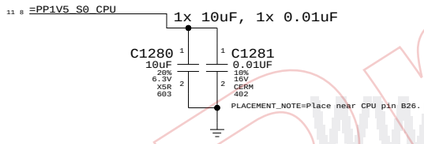
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

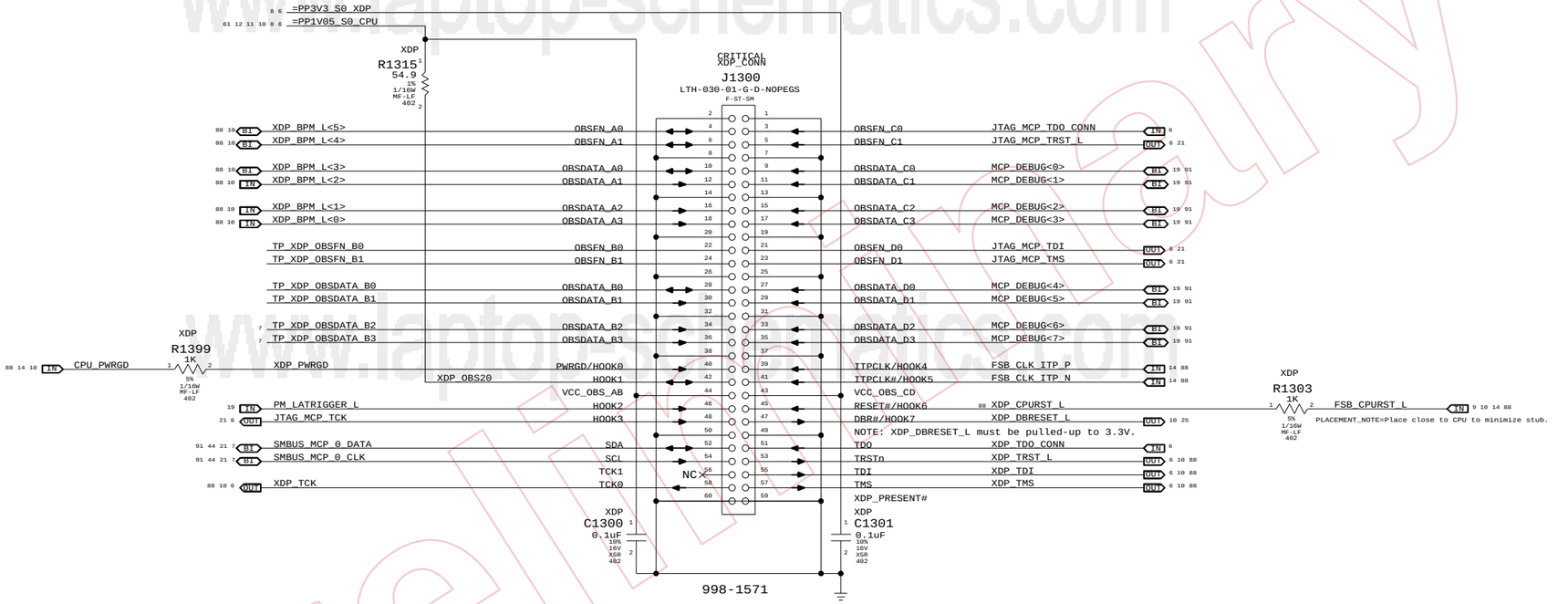
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	12	123

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 13 OF 123	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#	
FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#	
FSB_DINV_L<0>	V41	CPU_DBI0#	
FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#	
FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#	
FSB_DINV_L<1>	V35	CPU_DBI1#	
FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#	
FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#	
FSB_DINV_L<2>	N35	CPU_DBI2#	
FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#	
FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#	
FSB_DINV_L<3>	J41	CPU_DBI3#	
FSB_A_L<3>	AC34	CPU_A3#	
FSB_A_L<4>	AE38	CPU_A4#	
FSB_A_L<5>	AE34	CPU_A5#	
FSB_A_L<6>	AC37	CPU_A6#	
FSB_A_L<7>	AE37	CPU_A7#	
FSB_A_L<8>	AE35	CPU_A8#	
FSB_A_L<9>	AB35	CPU_A9#	
FSB_A_L<10>	AF35	CPU_A10#	
FSB_A_L<11>	AG35	CPU_A11#	
FSB_A_L<12>	AG39	CPU_A12#	
FSB_A_L<13>	AE33	CPU_A13#	
FSB_A_L<14>	AG37	CPU_A14#	
FSB_A_L<15>	AG38	CPU_A15#	
FSB_A_L<16>	AG34	CPU_A16#	
FSB_A_L<17>	AN38	CPU_A17#	
FSB_A_L<18>	AL39	CPU_A18#	
FSB_A_L<19>	AG33	CPU_A19#	
FSB_A_L<20>	AL33	CPU_A20#	
FSB_A_L<21>	AJ33	CPU_A21#	
FSB_A_L<22>	AN36	CPU_A22#	
FSB_A_L<23>	AJ35	CPU_A23#	
FSB_A_L<24>	AJ37	CPU_A24#	
FSB_A_L<25>	AJ36	CPU_A25#	
FSB_A_L<26>	AJ38	CPU_A26#	
FSB_A_L<27>	AL37	CPU_A27#	
FSB_A_L<28>	AL34	CPU_A28#	
FSB_A_L<29>	AN37	CPU_A29#	
FSB_A_L<30>	AJ34	CPU_A30#	
FSB_A_L<31>	AL38	CPU_A31#	
FSB_A_L<32>	AL35	CPU_A32#	
FSB_A_L<33>	AN34	CPU_A33#	
FSB_A_L<34>	AR39	CPU_A34#	
FSB_A_L<35>	AN35	CPU_A35#	
FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#	
FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#	
FSB_REQ_L<0>	AC38	CPU_REQ0#	
FSB_REQ_L<1>	AA33	CPU_REQ1#	
FSB_REQ_L<2>	AC39	CPU_REQ2#	
FSB_REQ_L<3>	AC33	CPU_REQ3#	
FSB_REQ_L<4>	AC35	CPU_REQ4#	
FSB_ADS_L	AD42	CPU_ADS#	
FSB_BNR_L	AD43	CPU_BNR#	
FSB_BREQ0_L	AE40	CPU_BR0#	
FSB_BREQ1_L	AL32	CPU_BR1#	
FSB_DBSY_L	AD39	CPU_DBSY#	
FSB_DRDY_L	AD41	CPU_DRDY#	
FSB_HIT_L	AB42	CPU_HIT#	
FSB_HITM_L	AD40	CPU_HITM#	
FSB_LOCK_L	AC43	CPU_LOCK#	
FSB_TRDY_L	AE41	CPU_TRDY#	
CPU_PECI_MCP	E41	CPU_PECI	
CPU_PROCHOT_L	AJ41	CPU_PROCHOT#	
	AG43	CPU_THERMTRIP#	
	AH40	CPU_FERR#	
(MCP_BSEL<2>)	F42	CPU_BSEL2	
(MCP_BSEL<1>)	D42	CPU_BSEL1	
(MCP_BSEL<0>)	F41	CPU_BSEL0	
FSB_RS_L<0>	AC41	CPU_RS0#	
FSB_RS_L<1>	AB41	CPU_RS1#	
FSB_RS_L<2>	AC42	CPU_RS2#	
PP1V05_S0_MCP_PLL_FSB			
270 mA (A01)	AG27	+V_DLL_DLCELL_AVDD	206 mA
	AH27	+V_PLL_MCLK	20 mA
	AG28	+V_PLL_FSB	29 mA
	AH28	+V_PLL_CPU	15 mA
MCP_BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AM43	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AM42	CPU_COMP_GND	

CPU_D0#	Y43	FSB_D_L<0>	
CPU_D1#	W42	FSB_D_L<1>	
CPU_D2#	Y40	FSB_D_L<2>	
CPU_D3#	W41	FSB_D_L<3>	
CPU_D4#	Y39	FSB_D_L<4>	
CPU_D5#	V42	FSB_D_L<5>	
CPU_D6#	Y41	FSB_D_L<6>	
CPU_D7#	Y42	FSB_D_L<7>	
CPU_D8#	P42	FSB_D_L<8>	
CPU_D9#	U41	FSB_D_L<9>	
CPU_D10#	R42	FSB_D_L<10>	
CPU_D11#	T39	FSB_D_L<11>	
CPU_D12#	T42	FSB_D_L<12>	
CPU_D13#	T41	FSB_D_L<13>	
CPU_D14#	R41	FSB_D_L<14>	
CPU_D15#	T43	FSB_D_L<15>	
CPU_D16#	W35	FSB_D_L<16>	
CPU_D17#	AA37	FSB_D_L<17>	
CPU_D18#	W33	FSB_D_L<18>	
CPU_D19#	W34	FSB_D_L<19>	
CPU_D20#	AA36	FSB_D_L<20>	
CPU_D21#	AA34	FSB_D_L<21>	
CPU_D22#	AA38	FSB_D_L<22>	
CPU_D23#	AA35	FSB_D_L<23>	
CPU_D24#	U38	FSB_D_L<24>	
CPU_D25#	U36	FSB_D_L<25>	
CPU_D26#	U35	FSB_D_L<26>	
CPU_D27#	U33	FSB_D_L<27>	
CPU_D28#	U34	FSB_D_L<28>	
CPU_D29#	W38	FSB_D_L<29>	
CPU_D30#	R33	FSB_D_L<30>	
CPU_D31#	U37	FSB_D_L<31>	
CPU_D32#	N34	FSB_D_L<32>	
CPU_D33#	N33	FSB_D_L<33>	
CPU_D34#	R34	FSB_D_L<34>	
CPU_D35#	R35	FSB_D_L<35>	
CPU_D36#	P35	FSB_D_L<36>	
CPU_D37#	R39	FSB_D_L<37>	
CPU_D38#	R37	FSB_D_L<38>	
CPU_D39#	R38	FSB_D_L<39>	
CPU_D40#	L37	FSB_D_L<40>	
CPU_D41#	L39	FSB_D_L<41>	
CPU_D42#	L38	FSB_D_L<42>	
CPU_D43#	N36	FSB_D_L<43>	
CPU_D44#	N38	FSB_D_L<44>	
CPU_D45#	J39	FSB_D_L<45>	
CPU_D46#	J38	FSB_D_L<46>	
CPU_D47#	J37	FSB_D_L<47>	
CPU_D48#	L42	FSB_D_L<48>	
CPU_D49#	M42	FSB_D_L<49>	
CPU_D50#	P41	FSB_D_L<50>	
CPU_D51#	N41	FSB_D_L<51>	
CPU_D52#	N40	FSB_D_L<52>	
CPU_D53#	M40	FSB_D_L<53>	
CPU_D54#	H40	FSB_D_L<54>	
CPU_D55#	K42	FSB_D_L<55>	
CPU_D56#	H41	FSB_D_L<56>	
CPU_D57#	L41	FSB_D_L<57>	
CPU_D58#	H43	FSB_D_L<58>	
CPU_D59#	H42	FSB_D_L<59>	
CPU_D60#	K41	FSB_D_L<60>	
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CPU_D62#	H39	FSB_D_L<62>	
CPU_D63#	M43	FSB_D_L<63>	
CPU_BPRI#	AA41	FSB_BPRI_L	
CPU_DEFER#	AA40	FSB_DEFER_L	
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AL41	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AK42	FSB_CLK_MCP_N	
BCLK_IN_N	AK41		
BCLK_IN_P	AJ40		
CPU_A20M#	AF41	CPU_A20M_L	
CPU_IGNNE#	AH39	CPU_IGNNE_L	
CPU_INIT#	AH42	CPU_INIT_L	
CPU_INTR	AF42	CPU_INTR	
CPU_NMI	AG41	CPU_NMI	
CPU_SMI#	AH41	CPU_SMI_L	
CPU_PWRGD	AH43	CPU_PWRGD	
CPU_RESET#	H38	FSB_CPURST_L	
CPU_SLP#	AM33	FSB_CPUSLP_L	
CPU_DPSLP#	AN33	CPU_DPSLP_L	
CPU_DPWR#	AM32	FSB_DPWR_L	
CPU_STPCLK#	AG42	CPU_STPCLK_L	
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

NO STUFF
R1440 150 5% 1/16W MF-LF 402

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

PM_THRMTRIP_L
CPU_FERR_L

NO STUFF R1420 1K 5% 1/16W MF-LF 402
NO STUFF R1421 1K 5% 1/16W MF-LF 402
NO STUFF R1422 1K 5% 1/16W MF-LF 402

=MCP_BSEL<2>
=MCP_BSEL<1>
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R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP CPU Interface

SYNC_MASTER=T18_MLB
SYNC_DATE=06/06/2008

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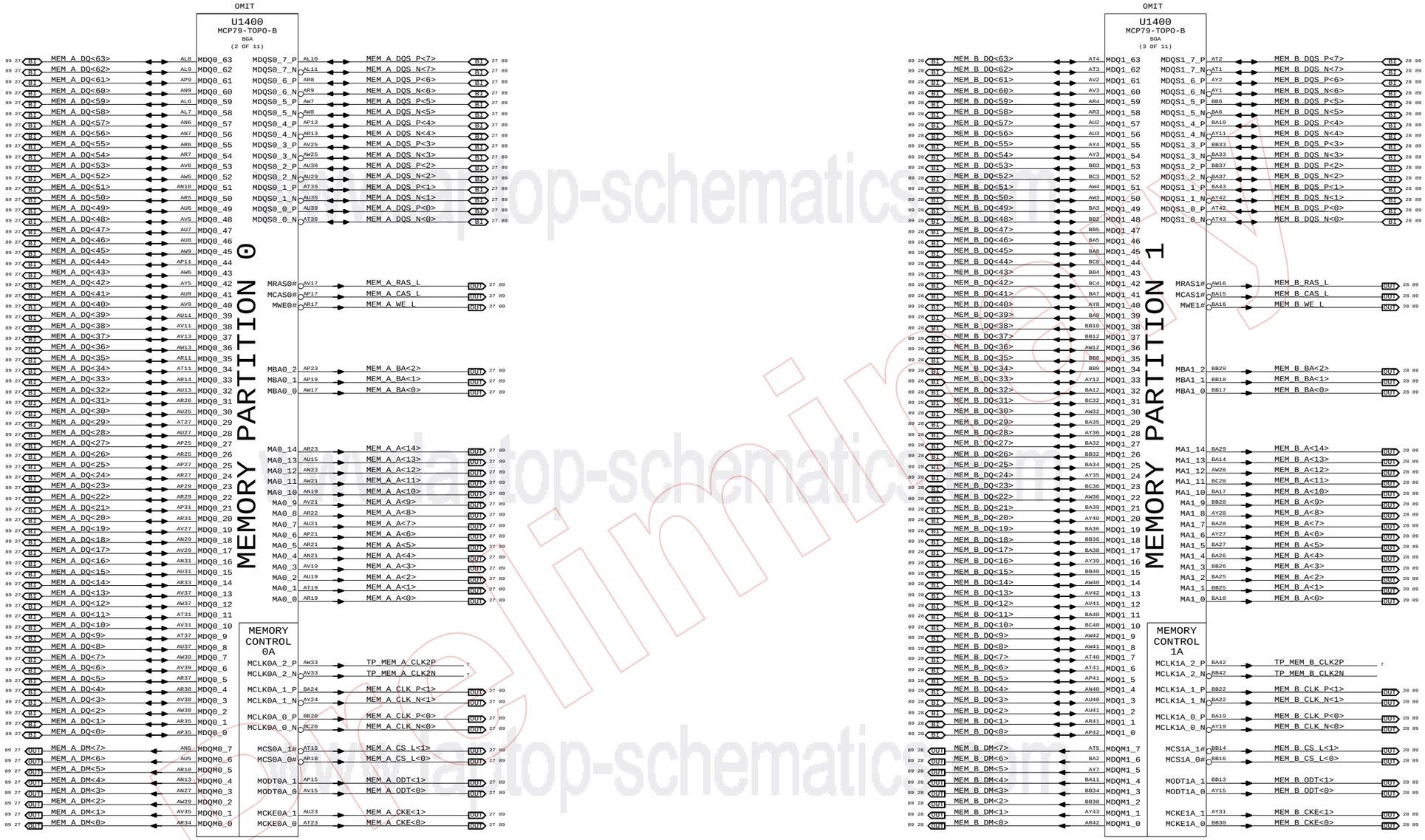
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 14 OF 123	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U1400
MCP79-TOPO-B
BGA
(2 OF 11)
MEMORY PARTITION 0
MEMORY CONTROL 0A
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MEM_A_DQ<62> AL9 MDQ0_62
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MEM_A_DQ<48> AV5 MDQ0_48
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MEM_A_DQ<43> AW6 MDQ0_43
MEM_A_DQ<42> AY5 MDQ0_42
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MEM_A_DM<4> AN13 MDQM0_4
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MEM_A_DM<2> AW29 MDQM0_2
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MDQS0_7_N AL11 MEM_A_DQS_N<7>
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MDQS0_6_N AR9 MEM_A_DQS_N<6>
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MDQS0_5_N AW8 MEM_A_DQS_N<5>
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MDQS0_4_N AR13 MEM_A_DQS_N<4>
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MDQS0_3_N AW25 MEM_A_DQS_N<3>
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MCAS0# AP17 MEM_A_CAS_L
MWE0# AR17 MEM_A_WE_L
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MA0_1 AT19 MEM_A_A<1>
MA0_0 AR19 MEM_A_A<0>
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MCLK0A_1_N AY24 MEM_A_CLK_N<1>
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MCS0A_0# AR18 MEM_A_CS_L<0>
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MODT0A_0 AV15 MEM_A_ODT<0>
MCKE0A_1 AU23 MEM_A_CKE<1>
MCKE0A_0 AT23 MEM_A_CKE<0>
OMIT
U1400
MCP79-TOPO-B
BGA
(3 OF 11)
MEMORY PARTITION 1
MEMORY CONTROL 1A
MEM_B_DQ<63> AT4 MDQ1_63
MEM_B_DQ<62> AT3 MDQ1_62
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MEM_B_DQ<35> BB8 MDQ1_35
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MEM_B_DQ<22> AW36 MDQ1_22
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MDQS1_0_N AT43 MEM_B_DQS_N<0>
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MCAS1# BA15 MEM_B_CAS_L
MWE1# BA16 MEM_B_WE_L
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MA1_7 BA28 MEM_B_A<7>
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MA1_5 BA27 MEM_B_A<5>
MA1_4 BA26 MEM_B_A<4>
MA1_3 BB26 MEM_B_A<3>
MA1_2 BA25 MEM_B_A<2>
MA1_1 BB25 MEM_B_A<1>
MA1_0 BA18 MEM_B_A<0>
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MCLK1A_2_N BB42 TP_MEM_B_CLK2N
MCLK1A_1_P BB22 MEM_B_CLK_P<1>
MCLK1A_1_N BA22 MEM_B_CLK_N<1>
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MCS1A_0# BB16 MEM_B_CS_L<0>
MODT1A_1 BB13 MEM_B_ODT<1>
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SYNC_MASTER=T18_MLB
SYNC_DATE=06/06/2008
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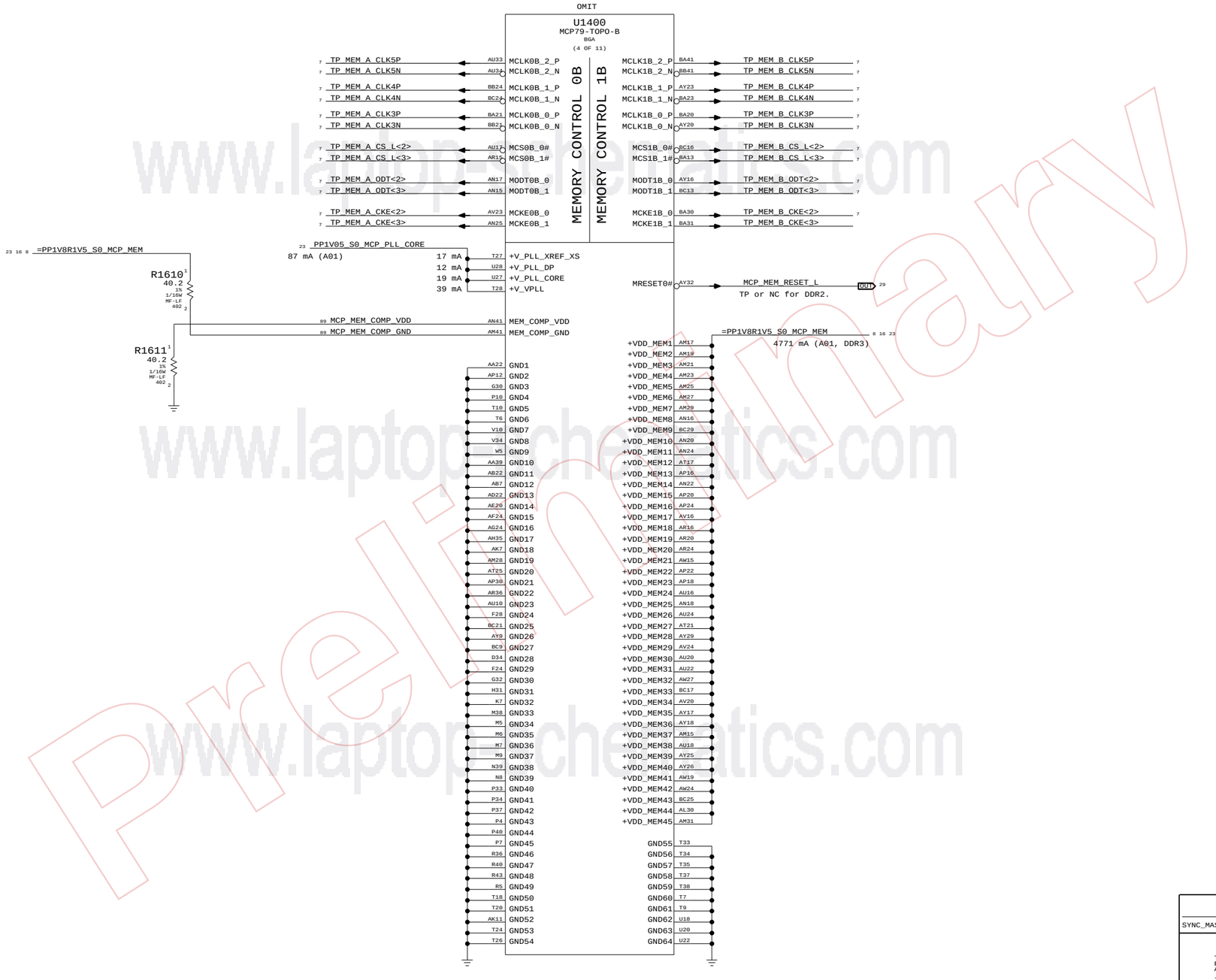
SIZE D
DRAWING NUMBER 051-7656
REV. 31
SCALE NONE
SHT 15 OF 123



MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 16 OF 123	

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OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

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				PE0_REFCLK_N	D11	PEG_CLK100M_N	69 90
MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49 Int PU		PE1_REFCLK_P	G11	PCIE_CLK100M_MINI_P	30 90
PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU		PE1_REFCLK_N	F11	PCIE_CLK100M_MINI_N	30 90
FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50 Int PU		PE2_REFCLK_P	J11	PCIE_CLK100M_FW_P	35 90
PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU		PE2_REFCLK_N	J10	PCIE_CLK100M_FW_N	35 90
EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51 Int PU		PE3_REFCLK_P	G13	PCIE_CLK100M_EXCARD_P	31 90
PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU		PE3_REFCLK_N	F13	PCIE_CLK100M_EXCARD_N	31 90
TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16 Int PU		PE4_REFCLK_P	J13	TP_PCIE_CLK100M_PE4P	
TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU		PE4_REFCLK_N	H13	TP_PCIE_CLK100M_PE4N	
AUD_IP_PERIPHERAL_DET	M16	PEF_CLKREQ#/GPIO_17 Int PU		PE5_REFCLK_P	L14	TP_PCIE_CLK100M_PE5P	
GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU		PE5_REFCLK_N	K14	TP_PCIE_CLK100M_PE5N	
TP_MCP_GPIO_18	M17	PEG_CLKREQ#/GPIO_18 Int PU		PE6_REFCLK_P	N14	TP_PCIE_CLK100M_PE6P	
GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU		PE6_REFCLK_N	M14	TP_PCIE_CLK100M_PE6N	
PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)		PEX_RST0#	K11	PCIE_RESET_L	25
PCIE_MINI_D2R_P	K9	PE1_RX0_P		PE1_TX0_P	D8	PCIE_MINI_R2D_C_P	30 90
PCIE_MINI_D2R_N	J9	PE1_RX0_N		PE1_TX0_N	C8	PCIE_MINI_R2D_C_N	30 90
PCIE_FW_D2R_P	H9	PE1_RX1_P		PE1_TX1_P	B8	PCIE_FW_R2D_C_P	35 90
PCIE_FW_D2R_N	G9	PE1_RX1_N		PE1_TX1_N	A8	PCIE_FW_R2D_C_N	35 90
PCIE_EXCARD_D2R_P	F9	PE1_RX2_P		PE1_TX2_P	A7	PCIE_EXCARD_R2D_C_P	31 90
PCIE_EXCARD_D2R_N	E9	PE1_RX2_N		PE1_TX2_N	B7	PCIE_EXCARD_R2D_C_N	31 90
TP_PCIE_PE4_D2RP	H7	PE1_RX3_P		PE1_TX3_P	B6	TP_PCIE_PE4_R2D_CP	
TP_PCIE_PE4_D2RN	G7	PE1_RX3_N		PE1_TX3_N	C6	TP_PCIE_PE4_R2D_CN	

=PP1V05_S0_MCP_PEX_DVDD0
57 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

+DVDD0_PEX1	T17
+DVDD0_PEX2	W19
+DVDD0_PEX3	U17
+DVDD0_PEX4	V19
+DVDD0_PEX5	W16
+DVDD0_PEX6	W17
+DVDD0_PEX7	W18
+DVDD0_PEX8	U16

=PP1V05_S0_MCP_PEX_AVDD0
206 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

+AVDD0_PEX1	Y12
+AVDD0_PEX2	AA12
+AVDD0_PEX3	AB12
+AVDD0_PEX4	M12
+AVDD0_PEX5	P12
+AVDD0_PEX6	R12
+AVDD0_PEX7	N12
+AVDD0_PEX8	T12
+AVDD0_PEX9	U12
+AVDD0_PEX10	AC12
+AVDD0_PEX11	AD12
+AVDD0_PEX12	V12
+AVDD0_PEX13	W12

=PP1V05_S0_MCP_PEX_DVDD1

+DVDD1_PEX1	T19
+DVDD1_PEX2	U19

PP1V05_S0_MCP_PLL_PEX
84 mA (A01)

+V_PLL_PEX	T16

=PP1V05_S0_MCP_PEX_AVDD1

+AVDD1_PEX1	M13
+AVDD1_PEX2	N13
+AVDD1_PEX3	P13

MCP_PEX_CLK_COMP — PEX_CLK_COMP A11

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

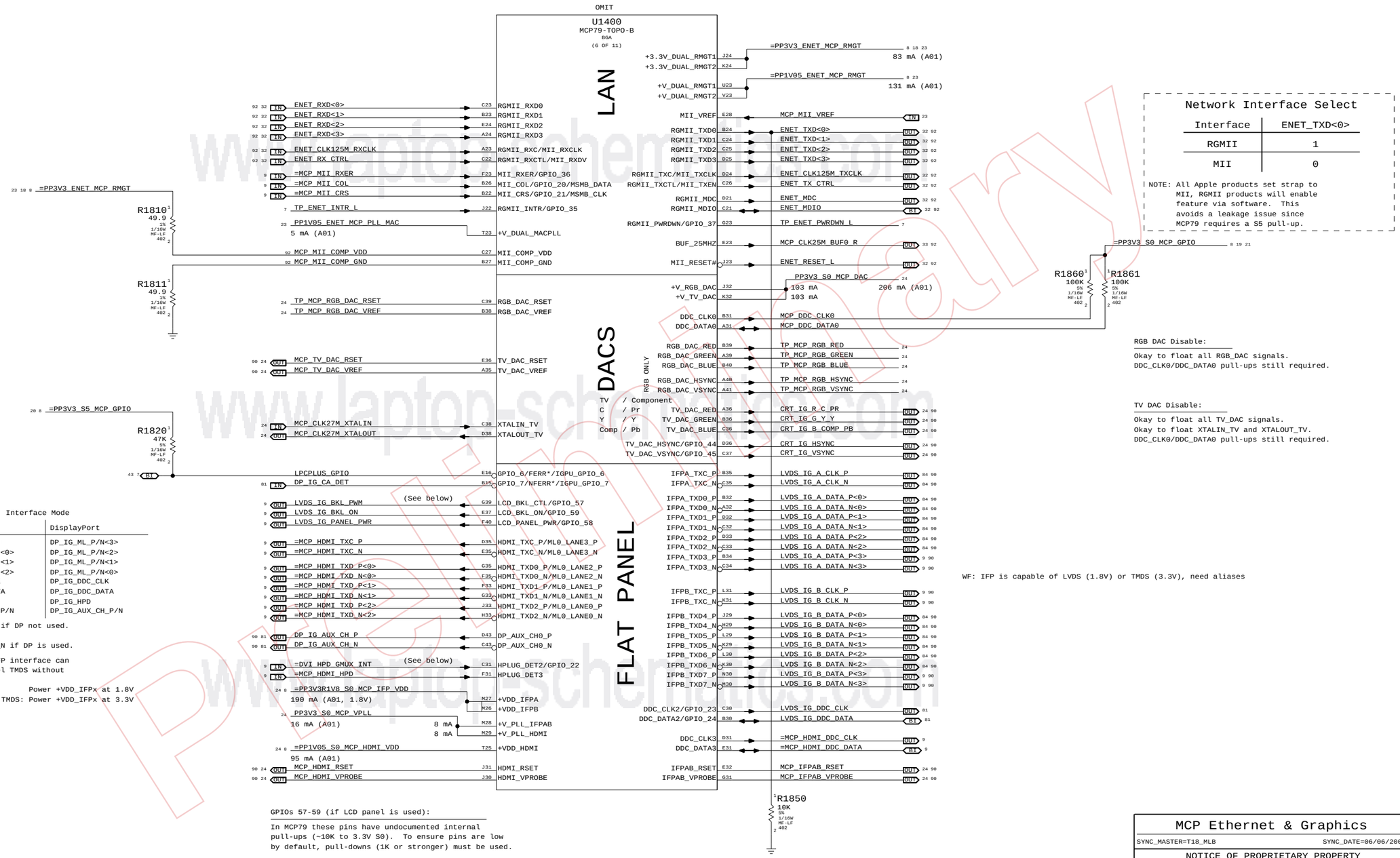
MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 17 OF 123	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).


OMIT
U1400
MCP79-TOPO-B
BGA
(6 OF 11)
LAN
DACS
RGB ONLY
FLAT PANEL
ENET_RXD<0>
ENET_RXD<1>
ENET_RXD<2>
ENET_RXD<3>
ENET_CLK125M_RXCLK
ENET_RX_CTRL
=MCP_MII_RXER
=MCP_MII_COL
=MCP_MII_CRS
TP_ENET_INTR_L
=PP3V3_ENET_MCP_RMGT
R1810 49.9 1% 1/16W MF-LF 402
R1811 49.9 1% 1/16W MF-LF 402
PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
MCP_MII_COMP_VDD
MCP_MII_COMP_GND
TP_MCP_RGB_DAC_RSET
TP_MCP_RGB_DAC_VREF
MCP_TV_DAC_RSET
MCP_TV_DAC_VREF
=PP3V3_S5_MCP_GPIO
R1820 47K 5% 1/16W MF-LF 402
MCP_CLK27M_XTALIN
MCP_CLK27M_XTALOUT
LPCPLUS_GPIO
DP_IG_CA_DET
(See below)
LVDS_IG_BKL_PWM
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
=MCP_HDMI_TXC_P
=MCP_HDMI_TXC_N
=MCP_HDMI_TXD_P<0>
=MCP_HDMI_TXD_N<0>
=MCP_HDMI_TXD_P<1>
=MCP_HDMI_TXD_N<1>
=MCP_HDMI_TXD_P<2>
=MCP_HDMI_TXD_N<2>
DP_IG_AUX_CH_P
DP_IG_AUX_CH_N
(See below)
=DVI_HPD_GMUX_INT
=MCP_HDMI_HPD
=PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)
PP3V3_S0_MCP_VPLL
16 mA (A01)
8 mA
8 mA
=PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)
MCP_HDMI_RSET
MCP_HDMI_VPROBE
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
RGMII_RXC/MII_RXCLK
RGMII_RXCTL/MII_RXDV
MII_RXER/GPIO_36
MII_COL/GPIO_20/MSMB_DATA
MII_CRS/GPIO_21/MSMB_CLK
RGMII_INTR/GPIO_35
+V_DUAL_MACPLL
MII_COMP_VDD
MII_COMP_GND
RGB_DAC_RSET
RGB_DAC_VREF
TV_DAC_RSET
TV_DAC_VREF
XTALIN_TV
XTALOUT_TV
GPIO_6/FERR*/IGPU_GPIO_6
GPIO_7/NFERR*/IGPU_GPIO_7
LCD_BKL_CTL/GPIO_57
LCD_BKL_ON/GPIO_59
LCD_PANEL_PWR/GPIO_58
HDMI_TXC_P/ML0_LANE3_P
HDMI_TXC_N/ML0_LANE3_N
HDMI_TXD0_P/ML0_LANE2_P
HDMI_TXD0_N/ML0_LANE2_N
HDMI_TXD1_P/ML0_LANE1_P
HDMI_TXD1_N/ML0_LANE1_N
HDMI_TXD2_P/ML0_LANE0_P
HDMI_TXD2_N/ML0_LANE0_N
DP_AUX_CH0_P
DP_AUX_CH0_N
HPLUG_DET2/GPIO_22
HPLUG_DET3
+VDD_IFPA
+VDD_IFPB
+V_PLL_IFPAB
+V_PLL_HDMI
+VDD_HDMI
HDMI_RSET
HDMI_VPROBE
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
+3.3V_DUAL_RMGT1
+3.3V_DUAL_RMGT2
+V_DUAL_RMGT1
+V_DUAL_RMGT2
MII_VREF
MCP_MII_VREF
RGMII_TXD0
RGMII_TXD1
RGMII_TXD2
RGMII_TXD3
RGMII_TXC/MII_TXCLK
RGMII_TXCTL/MII_TXEN
RGMII_MDC
RGMII_MDIO
RGMII_PWRDWN/GPIO_37
BUF_25MHZ
MII_RESET#
ENET_TXD<0>
ENET_TXD<1>
ENET_TXD<2>
ENET_TXD<3>
ENET_CLK125M_TXCLK
ENET_TX_CTRL
ENET_MDC
ENET_MDIO
TP_ENET_PWRDWN_L
MCP_CLK25M_BUF0_R
ENET_RESET_L
PP3V3_S0_MCP_DAC
206 mA (A01)
+V_RGB_DAC
+V_TV_DAC
103 mA
103 mA
DDC_CLK0
DDC_DATA0
MCP_DDC_CLK0
MCP_DDC_DATA0
RGB_DAC_RED
RGB_DAC_GREEN
RGB_DAC_BLUE
RGB_DAC_HSYNC
RGB_DAC_VSYNC
TP_MCP_RGB_RED
TP_MCP_RGB_GREEN
TP_MCP_RGB_BLUE
TP_MCP_RGB_HSYNC
TP_MCP_RGB_VSYNC
TV / Component
C / Pr
Y / Y
Comp / Pb
TV_DAC_RED
TV_DAC_GREEN
TV_DAC_BLUE
TV_DAC_HSYNC/GPIO_44
TV_DAC_VSYNC/GPIO_45
CRT_IG_R_C_PR
CRT_IG_G_Y_Y
CRT_IG_B_COMP_PB
CRT_IG_HSYNC
CRT_IG_VSYNC
IFPA_TXC_P
IFPA_TXC_N
IFPA_TXD0_P
IFPA_TXD0_N
IFPA_TXD1_P
IFPA_TXD1_N
IFPA_TXD2_P
IFPA_TXD2_N
IFPA_TXD3_P
IFPA_TXD3_N
LVDS_IG_A_CLK_P
LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_P<0>
LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<1>
LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<2>
LVDS_IG_A_DATA_N<2>
LVDS_IG_A_DATA_P<3>
LVDS_IG_A_DATA_N<3>
IFPB_TXC_P
IFPB_TXC_N
IFPB_TXD4_P
IFPB_TXD4_N
IFPB_TXD5_P
IFPB_TXD5_N
IFPB_TXD6_P
IFPB_TXD6_N
IFPB_TXD7_P
IFPB_TXD7_N
LVDS_IG_B_CLK_P
LVDS_IG_B_CLK_N
LVDS_IG_B_DATA_P<0>
LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_P<1>
LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_P<2>
LVDS_IG_B_DATA_N<2>
LVDS_IG_B_DATA_P<3>
LVDS_IG_B_DATA_N<3>
DDC_CLK2/GPIO_23
DDC_DATA2/GPIO_24
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
DDC_CLK3
DDC_DATA3
=MCP_HDMI_DDC_CLK
=MCP_HDMI_DDC_DATA
IFPAB_RSET
IFPAB_VPROBE
MCP_IFPAB_RSET
MCP_IFPAB_VPROBE
R1850 10K 5% 1/16W MF-LF 402
=PP3V3_S0_MCP_GPIO
R1860 100K 5% 1/16W MF-LF 402
R1861 100K 5% 1/16W MF-LF 402
Network Interface Select
Interface
ENET_TXD<0>
RGMII
1
MII
0
NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.
RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.
TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.
Interface Mode
MCP Signal
TMDS/HDMI
DisplayPort
=MCP_HDMI_TXC_P/N
=MCP_HDMI_TXD_P/N<0>
=MCP_HDMI_TXD_P/N<1>
=MCP_HDMI_TXD_P/N<2>
=MCP_HDMI_DDC_CLK
=MCP_HDMI_DDC_DATA
=MCP_HDMI_HPD
DP_IG_AUX_CH_P/N
TMDS_IG_TXC_P/N
TMDS_IG_TXD_P/N<0>
TMDS_IG_TXD_P/N<1>
TMDS_IG_TXD_P/N<2>
TMDS_IG_DDC_CLK
TMDS_IG_DDC_DATA
TMDS_IG_HPD
TP_DP_IG_AUX_CHP/N
DP_IG_ML_P/N<3>
DP_IG_ML_P/N<2>
DP_IG_ML_P/N<1>
DP_IG_ML_P/N<0>
DP_IG_DDC_CLK
DP_IG_DDC_DATA
DP_IG_HPD
DP_IG_AUX_CH_P/N
NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V
GPIOs 57-59 (if LCD panel is used):
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.
=DVI_HPD_GMUX_INT:
Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.
WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases
MCP Ethernet & Graphics
SYNC_MASTER=T18_MLB
SYNC_DATE=06/06/2008
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U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI

91 19	PCI_REQ0_L	T2	PCI_REQ0#	PCI_GNT0#	R3	TP_PCI_GNT0_L	7
91 19	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2	PCI_GNT1#/FANCTL2	U10	TP_PCI_GNT1_L	7
19 OUT	CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	PCI_GNT2#/GPIO_41/RS232_DTR#	R4	GMUX_JTAG_TMS	OUT 9
58 9 OUT	AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	PCI_GNT3#/GPIO_39/RS232_RTS#	U11	GMUX_JTAG_TDI	OUT 9
19 IN	MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	OUT 19
91 13 BI	MCP_DEBUG<0>	AC3	PCI_AD0	PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>	7
91 13 BI	MCP_DEBUG<1>	AE10	PCI_AD1	PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>	7
91 13 BI	MCP_DEBUG<2>	AC4	PCI_AD2	PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>	7
91 13 BI	MCP_DEBUG<3>	AE11	PCI_AD3	PCI_CBE3#	W10	TP_PCI_C_BE_L<3>	7
91 13 BI	MCP_DEBUG<4>	AB3	PCI_AD4				
91 13 BI	MCP_DEBUG<5>	AC6	PCI_AD5	PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L	7
91 13 BI	MCP_DEBUG<6>	AB2	PCI_AD6	PCI_FRAME#	Y4	TP_PCI_FRAME_L	7
91 13 BI	MCP_DEBUG<7>	AC7	PCI_AD7	PCI_IRDY#	AA10	TP_PCI_IRDY_L	7
7	TP_PCI_AD<8>	AC8	PCI_AD8	PCI_PAR	Y1	TP_PCI_PAR	7
7	TP_PCI_AD<9>	AA2	PCI_AD9	PCI_PERR#/GPIO_43/RS232_DCD#	AB9	TP_PCI_PERR_L	7
7	TP_PCI_AD<10>	AC9	PCI_AD10	PCI_SERR#	AA7	TP_PCI_SERR_L	7
7	TP_PCI_AD<11>	AC10	PCI_AD11	PCI_STOP#	Y2	TP_PCI_STOP_L	7
7	TP_PCI_AD<12>	AC11	PCI_AD12	PCI_PME#/GPIO_30 Int PU (S5)	T1	PM_LATRIGGER_L	OUT 13
7	TP_PCI_AD<13>	AA1	PCI_AD13				
7	TP_PCI_AD<14>	AA5	PCI_AD14	PCI_RESET0#	R10	MEM_VTT_EN_R	OUT 25
7	TP_PCI_AD<15>	Y5	PCI_AD15	PCI_RESET1#	R11	TP_PCI_RESET1_L	7
7	TP_PCI_AD<16>	W3	PCI_AD16				
7	TP_PCI_AD<17>	W6	PCI_AD17	PCI_CLK0	R6	TP_PCI_CLK0	7
7	TP_PCI_AD<18>	W4	PCI_AD18	PCI_CLK1	R7	TP_PCI_CLK1	7
7	TP_PCI_AD<19>	W7	PCI_AD19	PCI_CLK2	R8	91 PCI_CLK33M_MCP_R	
7	TP_PCI_AD<20>	V3	PCI_AD20				
7	TP_PCI_AD<21>	W8	PCI_AD21				
7	TP_PCI_AD<22>	V2	PCI_AD22				
7	TP_PCI_AD<23>	W9	PCI_AD23				
7	TP_PCI_AD<24>	U3	PCI_AD24				
7	TP_PCI_AD<25>	W11	PCI_AD25				
7	TP_PCI_AD<26>	U2	PCI_AD26				
7	TP_PCI_AD<27>	U5	PCI_AD27				
7	TP_PCI_AD<28>	U1	PCI_AD28				
7	TP_PCI_AD<29>	U6	PCI_AD29				
7	TP_PCI_AD<30>	T5	PCI_AD30				
7	TP_PCI_AD<31>	U7	PCI_AD31				
7	TP_PCI_INTW_L	P2	PCI_INTW#				
7	TP_PCI_INTX_L	N3	PCI_INTX#				
7	TP_PCI_INTY_L	N2	PCI_INTY#				
7	TP_PCI_INTZ_L	N1	PCI_INTZ#				
7	TP_PCI_TRDY_L	Y3	PCI_TRDY#				
43 41 7 IN	PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42				
35 IN	FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU				
7	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU				
43 41 7 BI	LPC_SERIRQ	AE6	LPC_SERIRQ Int PU				

R1910
22
5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	3 LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402	LPC_FRAME_L	OUT	7 41 43 84 91
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L			OUT	7 41 43
LPC_RESET0#	AE5	LPC_RESET_L			OUT	25 84 91
LPC_AD0	AD3	LPC_AD_R<0>	R1950 22 5% 1/16W MF-LF 402	LPC_AD<0>	BI	7 41 43 84 91
LPC_AD1	AD2	LPC_AD_R<1>	R1951 22 5% 1/16W MF-LF 402	LPC_AD<1>	BI	7 41 43 84 91
LPC_AD2	AD1	LPC_AD_R<2>	R1952 22 5% 1/16W MF-LF 402	LPC_AD<2>	BI	7 41 43 84 91
LPC_AD3	AD5	LPC_AD_R<3>	R1953 22 5% 1/16W MF-LF 402	LPC_AD<3>	BI	7 41 43 84 91
LPC_CLK0	AE9	LPC_CLK33M_SMC_R			OUT	25 91

R1961
10K
5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

21 18 8 =PP3V3_S0_MCP_GPIO

19 MCP_RS232_SOUT_L	R1989	8.2K	5% 1/16W MF-LF 402	
91 19 PCI_REQ0_L	R1990	8.2K	5% 1/16W MF-LF 402	
91 19 PCI_REQ1_L	R1991	8.2K	5% 1/16W MF-LF 402	
19 CRTMUX_SEL_TV_L	R1992	8.2K	5% 1/16W MF-LF 402	
19 MCP_RS232_SIN_L	R1994	8.2K	5% 1/16W MF-LF 402	

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

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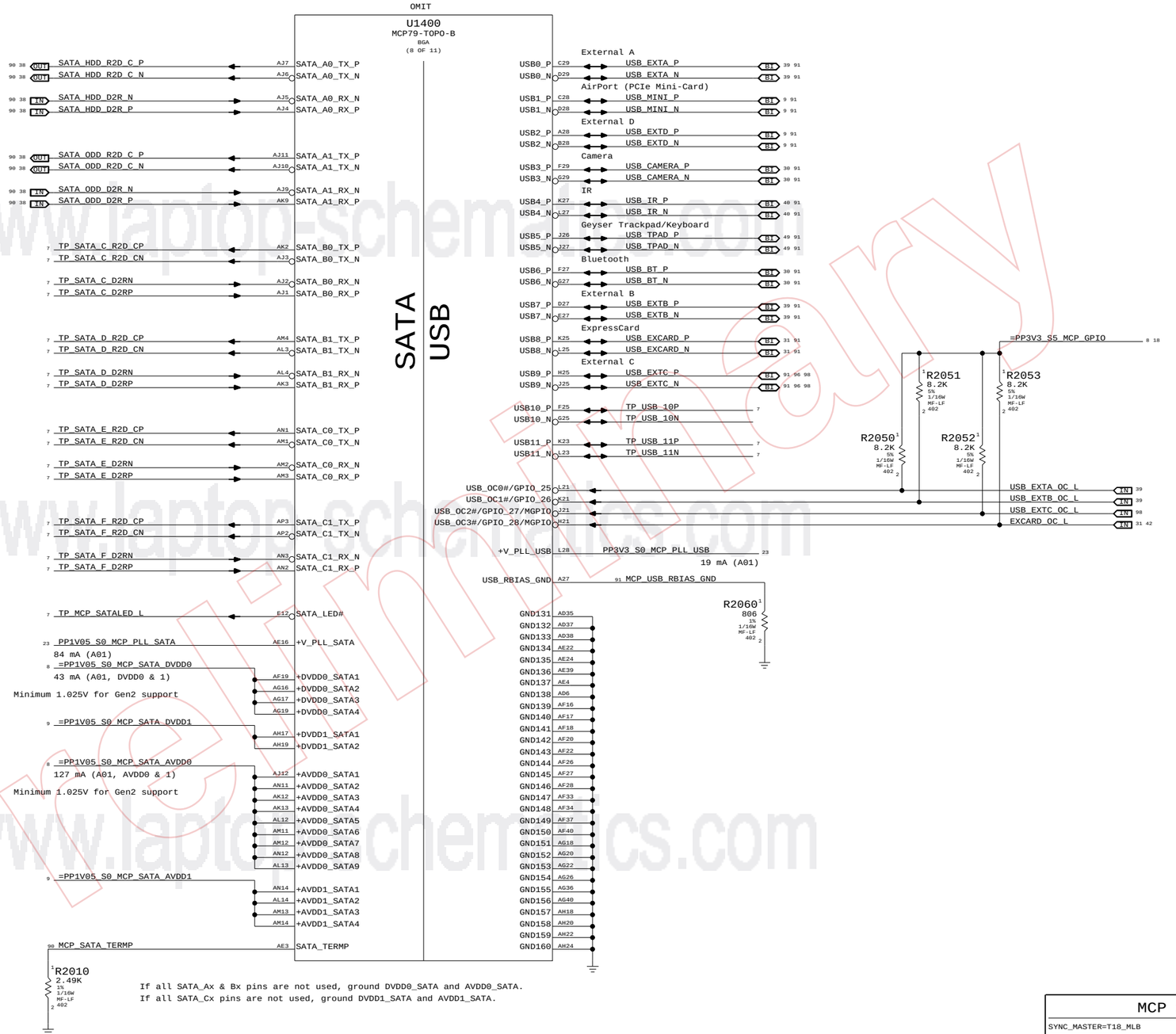
NONE	19	123



MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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D	051-7656	31
SCALE: NONE	SHT 20 OF 123	

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OMIT

U1400
MCP79-TOPO-B
BGA
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HDA

HDA_SDIN0	G15	HDA_SDATA_IN0	Int PD
TP_MLB_RAM_SIZE	J14	HDA_SDATA_IN1/GPIO_2/PS2_KB_CLK	Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems)	J15	HDA_SDATA_IN2/GPIO_3/PS2_KB_DATA	Int PD
MCP_HDA_PULLDN_COMP	A15	HDA_PULLDN_COMP	
PP1V05_S0_MCP_PLL_NV 37 mA (A01)	AE18	+V_PLL_NV_H	20 mA
	AE17	+V_PLL_SP_SPREF	17 mA

=PP3V3R1V5_S0_MCP_HDA → R2110 49.9 1% 1/16W MF-LF 402

PP3V3_G3_RTC → R2120 49.9K 1% 1/16W MF-LF 402; R2121 49.9K 1% 1/16W MF-LF 402

=SPI_CS1_R_L_USE_MLB	L24	GPIO_1/PWRDN_OK/SPI_CS1	
SMC_ADAPTER_EN	L20	GPIO_12/SUS_STAT#/ACCLMTR	
TP_SB_A20GATE	K13	A20GATE	Int PU
TP_MCP_KBDRSTIN_L	L13	KBRDRSTIN#	Int PU
SMC_WAKE_SCI_L	C19	SIO_PME#	Int PU (S5)
SMC_RUNTIME_SCI_L	C18	EXT_SMI/GPIO_32#	Int PU (S5)
SM_INTRUDER_L	B20	INTRUDER#	
TP_MCP_LID_L	M25	LID#	Int PU (S5)
PM_BATLOW_L	M24	LLB#	Int PU (S5)
PM_DPRSLPVR	M22	CPU_DPRSLPVR	
PM_PWRBTN_L	C16	PWRBTN#	Int PU (S5)
PM_SYSRST_DEBOUNCE_L	D16	RSTBTN#	Int PU
RTC_RST_L	C20	RTC_RST#	
PM_RSMRST_L	D20	PWRGD_SB	
MCP_PS_PWRGD	E20	PS_PWRGD	
MCP_CPU_VLD	C17	CPU_VLD	
JTAG_MCP_TDI	E19	JTAG_TDI	Int PU
JTAG_MCP_TDO	F19	JTAG_TDO	
JTAG_MCP_TMS	J19	JTAG_TMS	Int PU
JTAG_MCP_TRST_L	J18	JTAG_TRST#	
JTAG_MCP_TCK	G19	JTAG_TCK	
MCP_CLK25M_XTALIN	A16	XTALIN	
MCP_CLK25M_XTALOUT	B16	XTALOUT	
RTC_CLK32K_XTALIN	A19	XTALIN_RTC	
RTC_CLK32K_XTALOUT	B19	XTALOUT_RTC	

R2150 10K 5% 1/16W MF-LF 402; R2151 100K 5% 1/16W MF-LF 402

MISC

HDA_SDATA_OUT	F15	HDA_SDOUT_R	→ R2170 22 → HDA_SDOUT
HDA_BITCLK	E15	HDA_BIT_CLK_R	→ R2171 22 → HDA_BIT_CLK
HDA_RESET#	K15	HDA_RST_R_L	→ R2172 22 → HDA_RST_L
HDA_SYNC	L15	HDA_SYNC_R	→ R2173 22 → HDA_SYNC
HDA_DOCK_EN#/GPIO_4/PS2_MS_CLK	K17	MCP_GPIO_4	
HDA_DOCK_RST#/GPIO_5/PS2_MS_DATA	L17	AUD_I2C_INT_L	
SLP_S3#	G17	PM_SLP_S3_L	
SLP_RMGT#	J17	PM_SLP_RMGT_L	
SLP_S5#	M17	PM_SLP_S4_L	
THERM_DIODE_P	B11	MCP_THMDIODE_P	
THERM_DIODE_N	C11	MCP_THMDIODE_N	
MCP_VID0/GPIO_13	L20	MCP_VID<0>	
MCP_VID1/GPIO_14	M20	MCP_VID<1>	
MCP_VID2/GPIO_15	M21	MCP_VID<2>	
SPKR	C13	MCP_SPKR	
SMB_CLK0	L19	SMBUS_MCP_0_CLK	
SMB_DATA0	K19	SMBUS_MCP_0_DATA	
SMB_CLK1/MSMB_CLK	G21	SMBUS_MCP_1_CLK	
SMB_DATA1/MSMB_DATA	F21	SMBUS_MCP_1_DATA	
SMB_ALERT#/GPIO_64	M23	AP_PWR_EN	
(MGPIO2) FANRPM0/GPIO_60	B12	MEM_EVENT_L	
FANCTL0/GPIO_61	A12	ODD_PWR_EN_L	
(MGPIO3) FANRPM1/GPIO_63	D12	SMC_IG_THROTTLE_L	
FANCTL1/GPIO_62	C12	ARB_DETECT	
CPUVDD_EN	D17	MCP_CPUVDD_EN	
SPI_CS0/GPIO_10	C14	SPI_CS0_R_L	
SPI_CLK/GPIO_11	D13	SPI_CLK_R	
SPI_DI/GPIO_8	C15	SPI_MISO	
SPI_DO/GPIO_9	B14	SPI_MOSI_R	
SUS_CLK/GPIO_34	B18	PM_CLK32K_SUSCLK_R	
BUF_SIO_CLK	AE7	TP_MCP_BUF_SIO_CLK	
TEST_MODE_EN	K22	MCP_TEST_MODE_EN	
PKG_TEST	L22		

=PP3V3R1V5_S0_MCP_HDA → R2160 8.2K 5% 1/16W MF-LF 402 → +V_DUAL_HDA1, +V_DUAL_HDA2

=PP3V3_S0_MCP → R2180 10K 5% 1/16W MF-LF 402 → BOOT_MODE_SAFE

BOOT_MODE_USER → R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

R2163 10K 5% 1/16W MF-LF 402

R2190 1K 1% 1/16W MF-LF 402

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R, HDA_BIT_CLK_R, HDA_RST_R_L, HDA_SYNC_R

C2170 10PF 5% 50V CERM 402; C2172 10PF 5% 50V CERM 402; C2171 10PF 5% 50V CERM 402; C2173 10PF 5% 50V CERM 402

=PP3V3_S0_MCP_GPIO → R2140 10K; R2141 10K; R2142 10K; R2143 10K → MCP_GPIO_4, AUD_I2C_INT_L, MEM_EVENT_L, SMC_IG_THROTTLE_L

ARB_DETECT → R2147 100K

=PP3V3_S3_MCP_GPIO → R2154 100K → AP_PWR_EN

MCP_VID<0>, MCP_VID<1>, MCP_VID<2> → R2155 22K; R2156 22K; R2157 22K

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 21 OF 123	

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GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

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POWER

45 23 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32
AC23	+VDD_CORE2	+VTT_CPU2	AC32
U25	+VDD_CORE3	+VTT_CPU3	E40
AH12	+VDD_CORE4	+VTT_CPU4	J36
AG10	+VDD_CORE5	+VTT_CPU5	N32
AG5	+VDD_CORE6	+VTT_CPU6	T32
Y21	+VDD_CORE7	+VTT_CPU7	U32
Y23	+VDD_CORE8	+VTT_CPU8	V32
AA16	+VDD_CORE9	+VTT_CPU9	W32
AA26	+VDD_CORE10	+VTT_CPU10	P31
AA27	+VDD_CORE11	+VTT_CPU11	AF32
AA28	+VDD_CORE12	+VTT_CPU12	AE32
AC16	+VDD_CORE13	+VTT_CPU13	AH32
AC17	+VDD_CORE14	+VTT_CPU14	AJ32
AC18	+VDD_CORE15	+VTT_CPU15	AK31
AC19	+VDD_CORE16	+VTT_CPU16	AK32
AC20	+VDD_CORE17	+VTT_CPU17	AD32
AC21	+VDD_CORE18	+VTT_CPU18	AL31
AA17	+VDD_CORE19	+VTT_CPU19	AB32
AC24	+VDD_CORE20	+VTT_CPU20	B41
AC25	+VDD_CORE21	+VTT_CPU21	B42
AC26	+VDD_CORE22	+VTT_CPU22	C40
AC27	+VDD_CORE23	+VTT_CPU23	C41
AC28	+VDD_CORE24	+VTT_CPU24	C42
AD21	+VDD_CORE25	+VTT_CPU25	D39
AD23	+VDD_CORE26	+VTT_CPU26	D40
W27	+VDD_CORE27	+VTT_CPU27	D41
V25	+VDD_CORE28	+VTT_CPU28	E38
AA18	+VDD_CORE29	+VTT_CPU29	E39
AE19	+VDD_CORE30	+VTT_CPU30	F37
AE21	+VDD_CORE31	+VTT_CPU31	F38
AE23	+VDD_CORE32	+VTT_CPU32	F39
AE25	+VDD_CORE33	+VTT_CPU33	G36
AE26	+VDD_CORE34	+VTT_CPU34	G37
AE27	+VDD_CORE35	+VTT_CPU35	G38
AE28	+VDD_CORE36	+VTT_CPU36	H35
AF10	+VDD_CORE37	+VTT_CPU37	H37
AF11	+VDD_CORE38	+VTT_CPU38	J34
AA19	+VDD_CORE39	+VTT_CPU39	J35
AF2	+VDD_CORE40	+VTT_CPU40	K33
AF21	+VDD_CORE41	+VTT_CPU41	K34
AF23	+VDD_CORE42	+VTT_CPU42	K35
AF25	+VDD_CORE43	+VTT_CPU43	L32
AF3	+VDD_CORE44	+VTT_CPU44	L33
AF4	+VDD_CORE45	+VTT_CPU45	L34
AF7	+VDD_CORE46	+VTT_CPU46	M31
AH23	+VDD_CORE47	+VTT_CPU47	M32
AF9	+VDD_CORE48	+VTT_CPU48	M33
AA20	+VDD_CORE49	+VTT_CPU49	N31
AG11	+VDD_CORE50	+VTT_CPU50	P32
AG12	+VDD_CORE51	+VTT_CPU51	Y32
AG21	+VDD_CORE52	+VTT_CPU52	AA32
AG23	+VDD_CORE53		
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32
AG3	+VDD_CORE55		
AG4	+VDD_CORE56		
AA21	+VDD_CORE57		
AG6	+VDD_CORE58		
AG7	+VDD_CORE59		
AG8	+VDD_CORE60		
AG9	+VDD_CORE61		
AH1	+VDD_CORE62		
AH10	+VDD_CORE63		
AH11	+VDD_CORE64		
W26	+VDD_CORE65		
AH2	+VDD_CORE66		
AA23	+VDD_CORE67		
W28	+VDD_CORE68		
AH25	+VDD_CORE69		
AH21	+VDD_CORE70	+3.3V_DUAL1	G18
AH3	+VDD_CORE71	+3.3V_DUAL2	H19
AH4	+VDD_CORE72	+3.3V_DUAL3	J20
AH5	+VDD_CORE73	+3.3V_DUAL4	K20
AH6	+VDD_CORE74		
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28
W23	+VDD_CORE79		
W25	+VDD_CORE80		
AF12	+VDD_CORE81		
A20	+VBAT	+VDD_AUXC1	T21
		+VDD_AUXC2	U21
		+VDD_AUXC3	V21

=PP1V05_S0_MCP_FSB
8 9 14 23
1139 mA 1182 mA (A01)

=PP3V3_S0_MCP
8 21 23
450 mA (A01)

+3.3V_1 AD10
+3.3V_2 AE8
+3.3V_3 AB10
+3.3V_4 AD9
+3.3V_5 Y10
+3.3V_6 AB11
+3.3V_7 AA8
+3.3V_8 Y9

=PP3V3_S5_MCP
8 23
16 mA 266 mA (A01)

+3.3V_DUAL1 G18
+3.3V_DUAL2 H19
+3.3V_DUAL3 J20
+3.3V_DUAL4 K20

+3.3V_DUAL_USB1 G26 250 mA
+3.3V_DUAL_USB2 H27
+3.3V_DUAL_USB3 J28
+3.3V_DUAL_USB4 K28

43 mA

=PP1V05_S5_MCP_VDD_AUXC
8 23
105 mA (A01)

+VDD_AUXC1 T21
+VDD_AUXC2 U21
+VDD_AUXC3 V21

25 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 22 OF 123	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

45 22 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

8 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

8 =PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

22 8 =PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

18 8 =PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

22 14 9 8 =PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

16 8 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

22 21 8 =PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

8 =PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
20 19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

22 8 =PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

23 18 8 =PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

21 8 =PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

8 =PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
18 5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

23 18 8 =PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402

MCP_MII_VREF OUT 18

C2591 0.1UF 20% 10V CERM 402

8 =PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
8 206 mA (A01)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
8 127 mA (A01)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

8 =PP1V05_S0_MCP_PLL_PEX_UF

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
17 84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 2.2UF 20% 6.3V CERM 402-LF

66 8 =PP1V05_S0_MCP_PLL_UF
562 mA (A01)

R2580 0.2 1% 1/5W MF 402-HF

PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
14 270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 2.2UF 20% 16V X5R 603

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
20 84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 2.2UF 20% 6.3V CERM 402-LF

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
16 87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2587 2.2UF 20% 6.3V CERM 402-LF

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
21 37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 2.2UF 20% 6.3V CERM 402-LF
C2590 0.1UF 20% 10V CERM 402

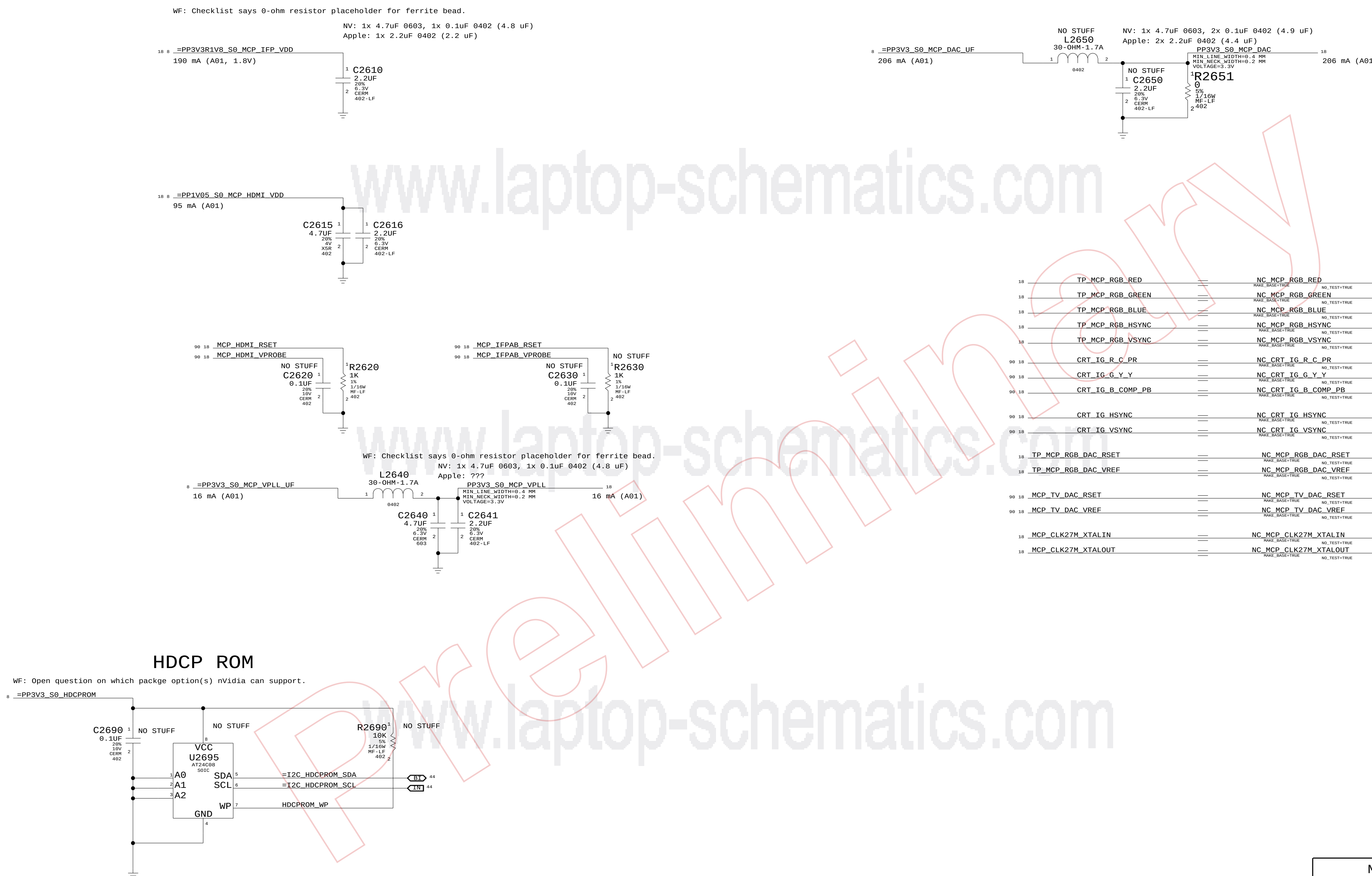
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	25	123



WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
=PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)
C2610
2.2UF
20%
6.3V
CERM
402-LF
NO STUFF
L2650
30-OHM-1.7A
0402
NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
=PP3V3_S0_MCP_DAC_UF
206 mA (A01)
PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
206 mA (A01)
NO STUFF
C2650
2.2UF
R2651
0
5%
1/16W
MF-LF
402
=PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)
C2615
4.7UF
20%
4V
X5R
402
C2616
2.2UF
20%
6.3V
CERM
402-LF
TP_MCP_RGB_RED
NC_MCP_RGB_RED
TP_MCP_RGB_GREEN
NC_MCP_RGB_GREEN
TP_MCP_RGB_BLUE
NC_MCP_RGB_BLUE
TP_MCP_RGB_HSYNC
NC_MCP_RGB_HSYNC
TP_MCP_RGB_VSYNC
NC_MCP_RGB_VSYNC
CRT_IG_R_C_PR
NC_CRT_IG_R_C_PR
CRT_IG_G_Y_Y
NC_CRT_IG_G_Y_Y
CRT_IG_B_COMP_PB
NC_CRT_IG_B_COMP_PB
CRT_IG_HSYNC
NC_CRT_IG_HSYNC
CRT_IG_VSYNC
NC_CRT_IG_VSYNC
TP_MCP_RGB_DAC_RSET
NC_MCP_RGB_DAC_RSET
TP_MCP_RGB_DAC_VREF
NC_MCP_RGB_DAC_VREF
MCP_TV_DAC_RSET
NC_MCP_TV_DAC_RSET
MCP_TV_DAC_VREF
NC_MCP_TV_DAC_VREF
MCP_CLK27M_XTALIN
NC_MCP_CLK27M_XTALIN
MCP_CLK27M_XTALOUT
NC_MCP_CLK27M_XTALOUT
MAKE_BASE=TRUE
NO_TEST=TRUE
MCP_HDMI_RSET
MCP_HDMI_VPROBE
NO STUFF
C2620
0.1UF
R2620
1K
1%
1/16W
MF-LF
402
MCP_IFPAB_RSET
MCP_IFPAB_VPROBE
NO STUFF
C2630
0.1UF
R2630
1K
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???
=PP3V3_S0_MCP_VPLL_UF
16 mA (A01)
L2640
30-OHM-1.7A
PP3V3_S0_MCP_VPLL
16 mA (A01)
C2640
4.7UF
C2641
2.2UF
HDCP ROM
WF: Open question on which packge option(s) nVidia can support.
=PP3V3_S0_HDCPROM
C2690
0.1UF
NO STUFF
VCC
U2695
AT24C08
SOIC
A0
A1
A2
SDA
SCL
WP
GND
R2690
10K
=I2C_HDCPROM_SDA
=I2C_HDCPROM_SCL
HDCPROM_WP

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

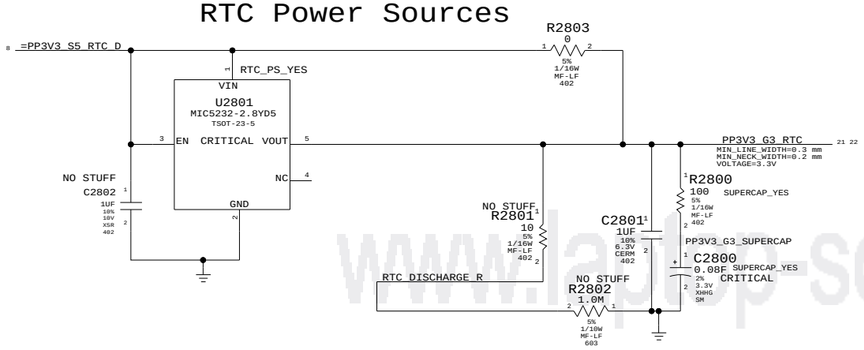
MCP Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

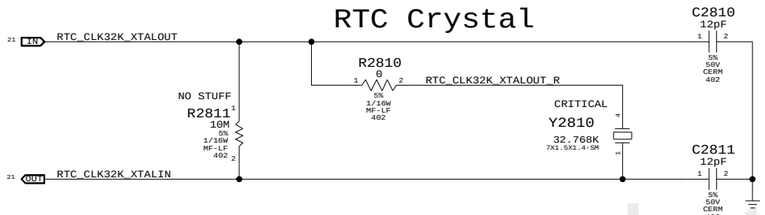
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE NONE	SHT 26	OF 123

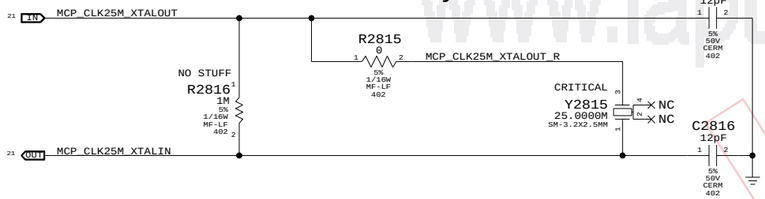
RTC Power Sources



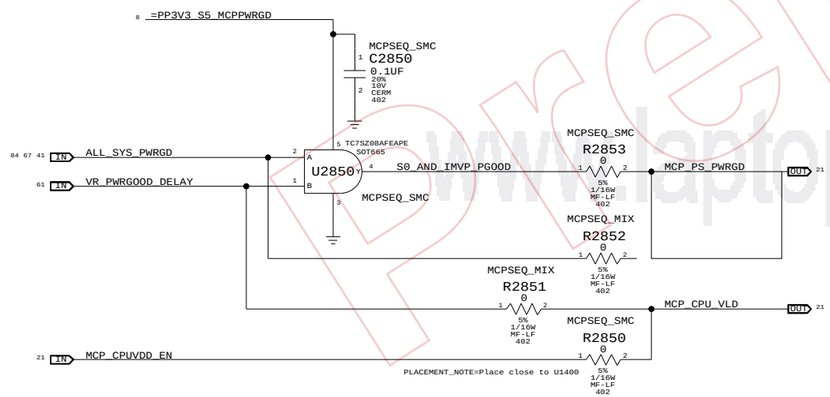
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

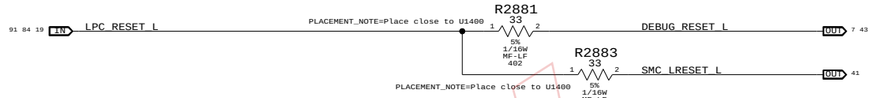
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

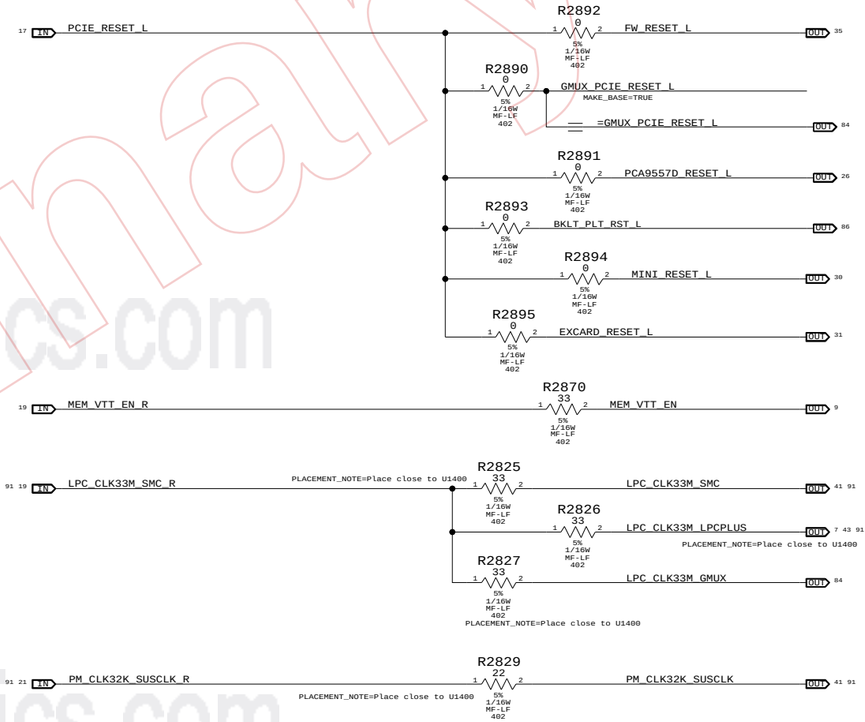
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

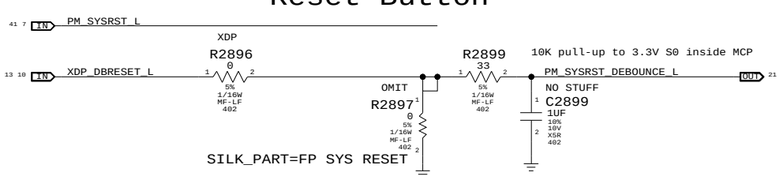
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc		
SYNC_MASTER=M98_MLB		SYNC_DATE=05/01/2008

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
	SCALE: NONE	SHT 28 OF 123	

Page Notes

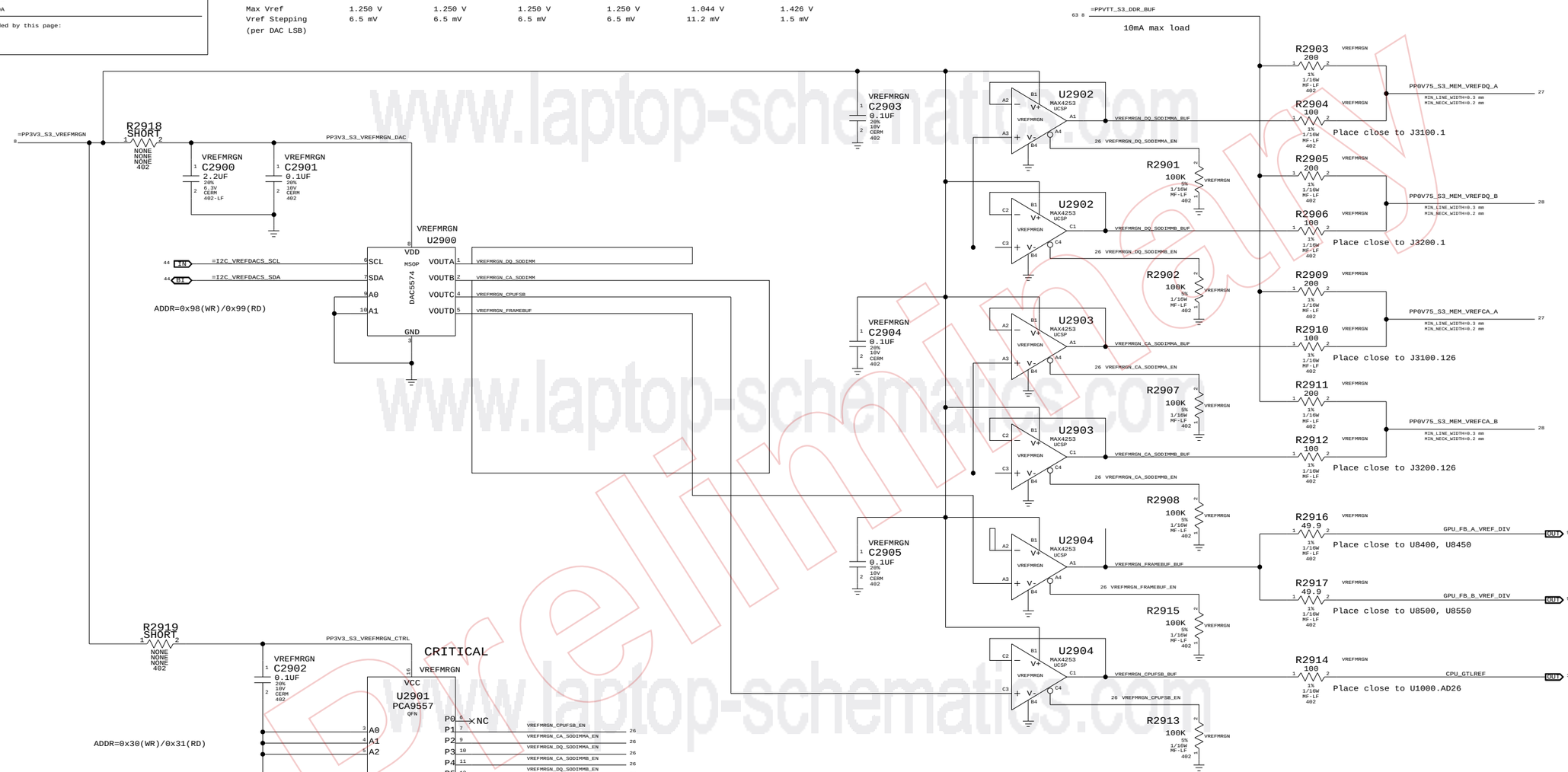
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	C	D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 29 OF 123

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_A
8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_A
C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)
KEY

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NC
NC
NC

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)
CRITICAL

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

KEY
516-0201

PP0V75_S3_MEM_VREFCA_A 26
C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

8 =PPSPD_S0_MEM_A
C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402
MEM_A_SA<0>
MEM_A_SA<1>

516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)

8 =PP0V75_S0_MEM_VTT_A

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN_K20 SYNC_DATE=06/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 31 OF 123	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_B
8 =PP1V5_S3_MEM_B

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603

26 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

89 15 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15 89
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 9
89 15 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15 89
		81	VDD	VDD	82		
89 15 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15 89
89 15 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15 89
		87	VDD	VDD	88		
89 15 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15 89
89 15 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15 89
		93	VDD	VDD	94		
89 15 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15 89
89 15 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15 89
		99	VDD	VDD	100		
89 15 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15 89
89 15 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15 89
		105	VDD	VDD	106		
89 15 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15 89
89 15 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15 89
		111	VDD	VDD	112		
89 15 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15 89
89 15 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15 89
		117	VDD	VDD	118		
89 15 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15 89
89 15 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
89 15 BI	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<33>	BI 15 89
89 15 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132	MEM_B_DQ<36>	BI 15 89
		133	VSS	VSS	134		
89 15 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 15 89
89 15 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 15 89
89 15 BI	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>	BI 15 89
89 15 BI	MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<44>	BI 15 89
89 15 BI	MEM_B_DQ<41>	147	DQ40	DQ45	148	MEM_B_DQ<45>	BI 15 89
89 15 BI	MEM_B_DQ<40>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 15 89
89 15 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 15 89
		155	VSS	VSS	156		
89 15 BI	MEM_B_DQ<43>	157	DQ42	DQ46	158	MEM_B_DQ<47>	BI 15 89
89 15 BI	MEM_B_DQ<42>	159	DQ43	DQ47	160	MEM_B_DQ<46>	BI 15 89
		161	VSS	VSS	162		
89 15 BI	MEM_B_DQ<55>	163	DQ48	DQ52	164	MEM_B_DQ<48>	BI 15 89
89 15 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<54>	BI 15 89
		167	VSS	VSS	168		
89 15 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15 89
89 15 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<53>	BI 15 89
89 15 BI	MEM_B_DQ<52>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 15 89
89 15 BI	MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<60>	BI 15 89
89 15 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61>	BI 15 89
89 15 BI	MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 15 89
89 15 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 15 89
		189	VSS	VSS	190		
89 15 BI	MEM_B_DQ<63>	191	DQ58	DQ62	192	MEM_B_DQ<58>	BI 15 89
89 15 BI	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<62>	BI 15 89
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 21 27 41
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 44
	MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 44
		203	VTT	VTT	204		
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

KEY
MTG PINS
516s0706
SPD ADDR=0xA2(WR)/0xA3(RD)

=PP0V75_S0_MEM_VTT_B 8

J3200 F-RT-BGA3 DDR3-SODIMM (1 OF 2) CRITICAL

1	VREFDQ	VSS	2		
3	VSS	DQ4	4	MEM_B_DQ<4>	BI 15 89
5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 15 89
7	DQ1	VSS	8		
9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 15 89
11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 15 89
13	VSS	VSS	14		
15	DQ2	DQ6	16	MEM_B_DQ<6>	BI 15 89
17	DQ3	DQ7	18	MEM_B_DQ<7>	BI 15 89
19	VSS	VSS	20		
21	DQ8	DQ12	22	MEM_B_DQ<29>	BI 15 89
23	DQ9	DQ13	24	MEM_B_DQ<25>	BI 15 89
25	VSS	VSS	26		
27	DQS1*	DM1	28	MEM_B_DM<3>	IN 15 89
29	DQS1	RESET*	30	MEM_RESET_L	IN 27 29
31	VSS	VSS	32		
33	DQ10	DQ14	34	MEM_B_DQ<26>	BI 15 89
35	DQ11	DQ15	36	MEM_B_DQ<27>	BI 15 89
37	VSS	VSS	38		
39	DQ16	DQ20	40	MEM_B_DQ<13>	BI 15 89
41	DQ17	DQ21	42	MEM_B_DQ<12>	BI 15 89
43	VSS	VSS	44		
45	DQS2*	DM2	46	MEM_B_DM<1>	IN 15 89
47	DQS2	VSS	48		
49	VSS	DQ22	50	MEM_B_DQ<14>	BI 15 89
51	DQ18	DQ23	52	MEM_B_DQ<11>	BI 15 89
53	DQ19	VSS	54		
55	VSS	DQ28	56	MEM_B_DQ<20>	BI 15 89
57	DQ24	DQ29	58	MEM_B_DQ<16>	BI 15 89
59	DQ25	VSS	60		
61	VSS	DQS3*	62	MEM_B_DQS_N<2>	BI 15 89
63	DM3	DQS3	64	MEM_B_DQS_P<2>	BI 15 89
65	VSS	VSS	66		
67	DQ26	DQ30	68	MEM_B_DQ<19>	BI 15 89
69	DQ27	DQ31	70	MEM_B_DQ<23>	BI 15 89
71	VSS	VSS	72		

89 15 BI MEM_B_DQ<0>
89 15 BI MEM_B_DQ<1>
89 15 IN MEM_B_DM<0>
89 15 BI MEM_B_DQ<2>
89 15 BI MEM_B_DQ<3>
89 15 BI MEM_B_DQ<28>
89 15 BI MEM_B_DQ<24>
89 15 BI MEM_B_DQS_N<3>
89 15 BI MEM_B_DQS_P<3>
89 15 BI MEM_B_DQ<31>
89 15 BI MEM_B_DQ<30>
89 15 BI MEM_B_DQ<9>
89 15 BI MEM_B_DQ<8>
89 15 BI MEM_B_DQS_N<1>
89 15 BI MEM_B_DQS_P<1>
89 15 BI MEM_B_DQ<15>
89 15 BI MEM_B_DQ<10>
89 15 BI MEM_B_DQ<21>
89 15 BI MEM_B_DQ<17>
89 15 IN MEM_B_DM<2>
89 15 BI MEM_B_DQ<18>
89 15 BI MEM_B_DQ<22>

KEY
516s0706

PP0V75_S3_MEM_VREFCA_B 26

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402

8 =PPSPD_S0_MEM_B

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

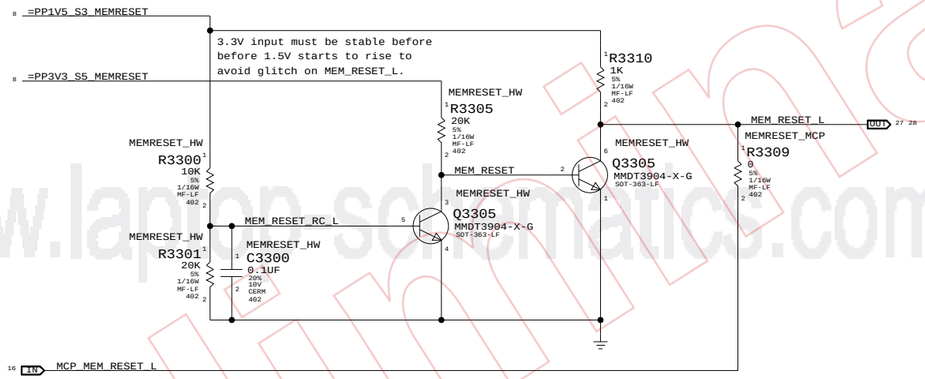
SYNC_MASTER=BEN_K20 SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT 32 OF 123	
NONE		

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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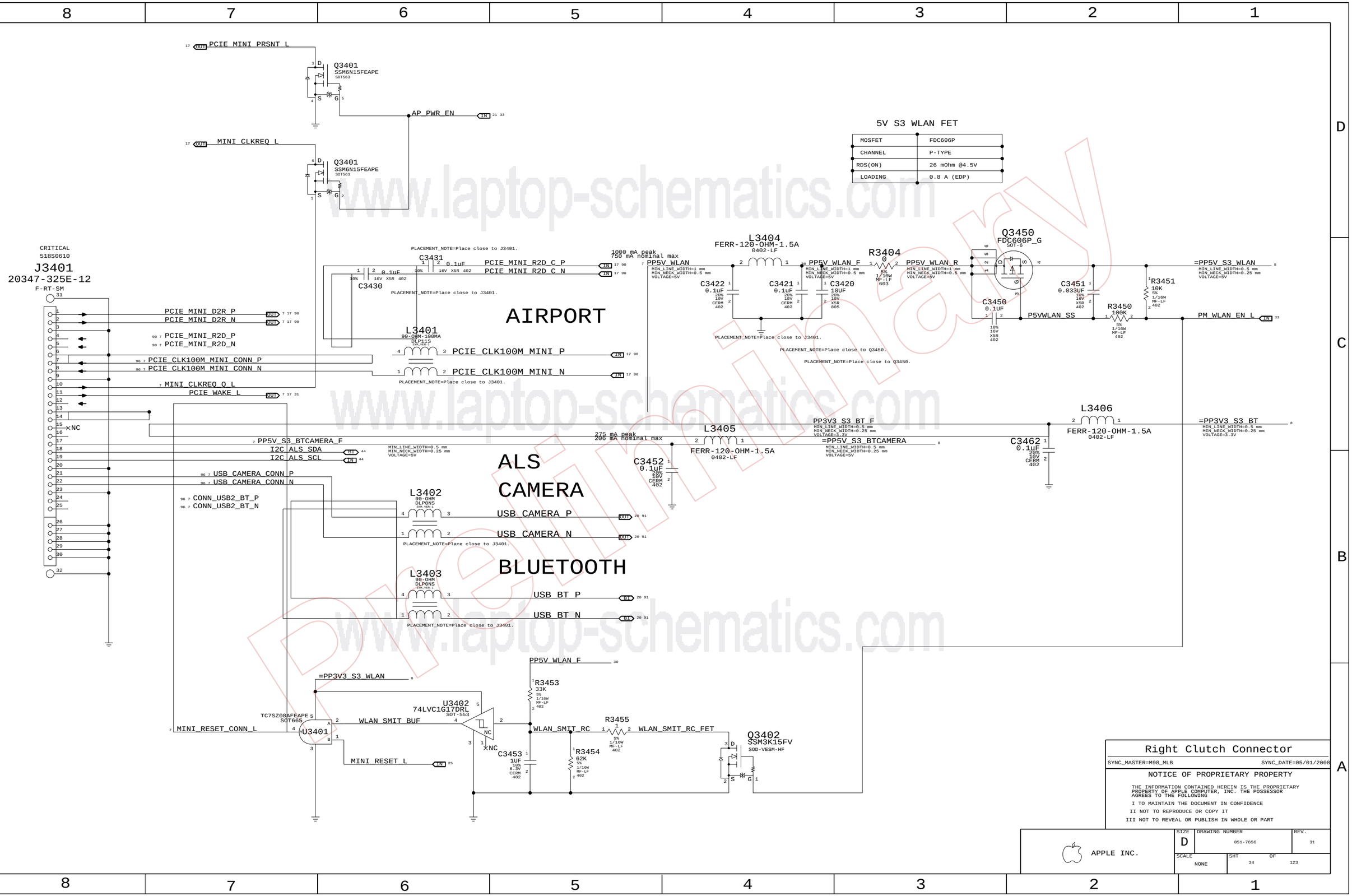
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	33	123



EXPRESSCARD/34 FLEX CONNECTOR

INPUT DECOUPLING

31 8 =PP3V3_S3_EXCARD
C3530 0.1uF 20% 10V CERM 402
C3531 10uF 20% 6.3V X5R 603

31 8 =PP1V5_S0_EXCARD
C3534 0.1uF 20% 10V CERM 402
C3535 10uF 20% 6.3V X5R 603

31 8 =PP3V3_S3_EXCARD — R3504 SHORT NONE NONE NONE NONE 402
31 8 =PP3V3_S0_EXCARD — R3503 SHORT NONE NONE NONE 402
31 8 =PP1V5_S0_EXCARD — R3502 SHORT NONE NONE NONE NONE 402

L3502 90-OHM DLP0NS SYM_VER-1
91 20 B↕ USB_EXCARD_N — 4 — 3 — USB2_EXCARD_CONN_N 7 31 96
91 20 B↕ USB_EXCARD_P — 1 — 2 — USB2_EXCARD_CONN_P 7 31 96
PLACEMENT_NOTE=Place close to J3500

L3503 90-OHM-100MA DLP11S SYM_VER-1
90 17 IN PCIE_CLK100M_EXCARD_N — 4 — 3 — PCIE_CLK100M_EXCARD_CONN_N 7 31 96
90 17 IN PCIE_CLK100M_EXCARD_P — 1 — 2 — PCIE_CLK100M_EXCARD_CONN_P 7 31 96
PLACEMENT_NOTE=Place close to J3500

PLACEMENT_NOTE=Place close to J3500
C3571 0.1uF 10% 16V X5R 402
90 17 IN PCIE_EXCARD_R2D_C_N — PCIE_EXCARD_R2D_N 7 31 90
90 17 IN PCIE_EXCARD_R2D_C_P — PCIE_EXCARD_R2D_P 7 31 90
C3570 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place close to J3500

CRITICAL
J3500 502250-5627 FCI-SMT-SR
90 31 7 PCIE_EXCARD_R2D_N
90 17 7 OUT PCIE_EXCARD_D2R_P
96 31 7 PCIE_CLK100M_EXCARD_CONN_N
31 7 EXCARD_CLKREQ_CONN_L
31 7 PP3V3_S0_EXCARD_SWITCH
31 7 PP3V3_S3_EXCARD_SWITCH
31 7 PP1V5_S0_EXCARD_SWITCH
44 B↕ =SMBUS_EXCARD_SDA
31 7 EXCARD_CPUSB_L
96 31 7 USB2_EXCARD_CONN_N
NC
NC
PCIE_EXCARD_R2D_P 7 31 90
PCIE_EXCARD_D2R_N OUT 7 17 90
PCIE_CLK100M_EXCARD_CONN_P 7 31 96
EXCARD_CPPE_L 7 31
PP3V3_S0_EXCARD_SWITCH 7 31
PLT_RESET_SWITCH_L 7 31
PCIE_WAKE_L OUT 7 17 30
PP1V5_S0_EXCARD_SWITCH 7 31
=SMBUS_EXCARD_SCL B↕ 44
USB2_EXCARD_CONN_P 7 31 96
518S0647

OUTPUT DECOUPLING

CRITICAL
U3500 TPS2231 QFN
PP3V3_S3_EXCARD_R 17 AUXIN — AUXOUT 15
PP3V3_S0_EXCARD_R 2 VIN3P3 — VOUT3P3 3
PP1V5_S0_EXCARD_R 12 VIN1P5 — VOUT1P5 11
41 IN SMC_EXCARD_PWR_EN
TP_EXCARD_STBY_L
28 IN EXCARD_RESET_L
42 20 IN EXCARD_OC_L
R3500 0 MF-LF 402 5% 1/16W EXCARD_SHDN_L_R
20 SHDN* — PERST* 8
1 STBY* — CPPE* 10
6 SYSRST* — CPUSB* 9
19 OC*
NC 4 NC0 — RCLKEN 18 EXCARD_RCLKEN 31
NC 5 NC1
NC 13 NC2
NC 14 NC3
NC 16 NC4 — THRML_PAD 21
GND

PP3V3_S3_EXCARD_SWITCH 7 31
VOLTAGE=3.3V MIN_LINE_WIDTH=.5mm MIN_NECK_WIDTH=0.2mm
C3500 0.1uF 20% 10V CERM 402
C3503 10uF 20% 6.3V X5R 603
PP3V3_S0_EXCARD_SWITCH 7 31
VOLTAGE=3.3V MIN_LINE_WIDTH=.5mm MIN_NECK_WIDTH=0.2mm
C3501 0.1uF 10% 16V X5R 402
C3504 10uF 20% 6.3V X5R 603
PP1V5_S0_EXCARD_SWITCH 7 31
VOLTAGE=1.5V MIN_LINE_WIDTH=.6mm MIN_NECK_WIDTH=0.2mm
C3502 0.1uF 10% 16V X5R 402
C3505 10uF 20% 6.3V X5R 603
PLT_RESET_SWITCH_L 7 31
EXCARD_CPPE_L 7 31
EXCARD_CPUSB_L 7 31

31 7 EXCARD_CPPE_L — R3501 0 MF-LF 402 5% 1/16W — PCIE_EXCARD_PRSNT_L 17

31 8 =PP3V3_S3_EXCARD
31 7 EXCARD_CPUSB_L
31 7 EXCARD_CPPE_L
U3551 74HC1G00GWDG SC70-5
SMC_EXCARD_CP OUT 41 42
C3550 0.1uF 20% 10V CERM 402

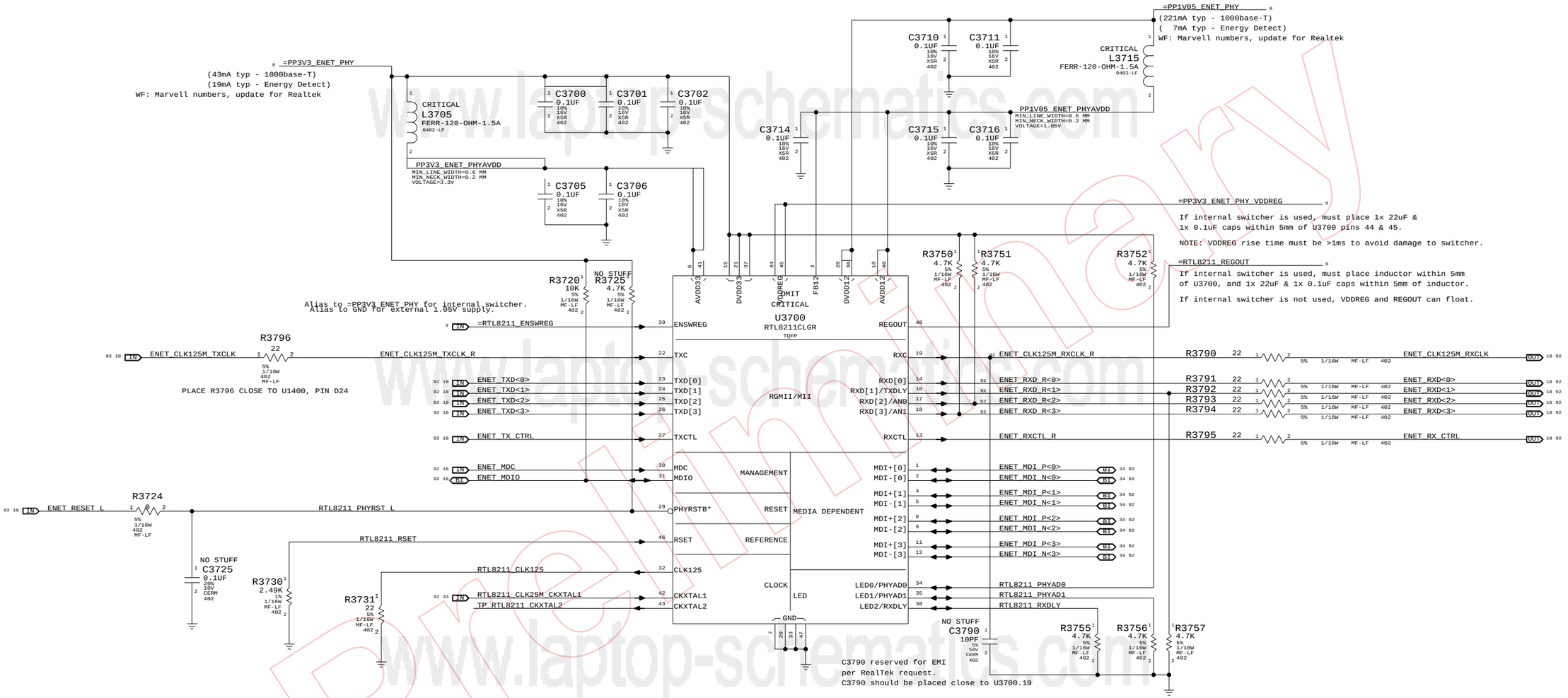
31 8 =PP3V3_S0_EXCARD
R3561 100K 1% 1/16W MF-LF 402
31 EXCARD_RCLKEN
EXCARD_CLKREQ_CONN
U3560 74HC1G00GWDG SC70-5
EXCARD_CLKREQ_L OUT 17
31 7 EXCARD_CLKREQ_CONN_L
U3561 SN74LVC1G04YZPR BGA
C3560 0.1uF 20% 10V CERM 402

ExpressCard Connector

SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 35 OF 123	



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

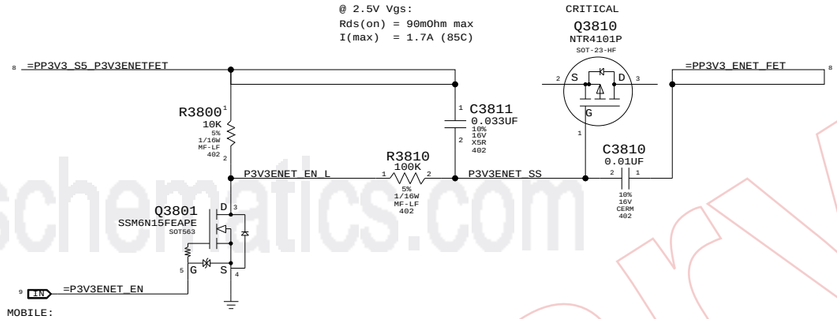
Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 37 OF 123	

3.3V ENET FET



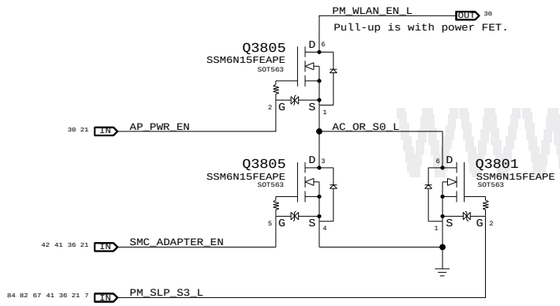
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

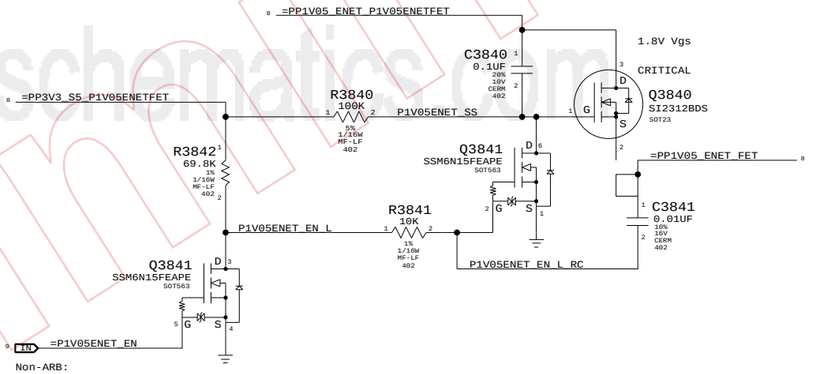
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET

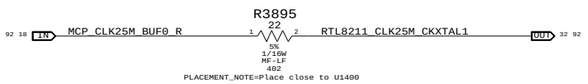


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

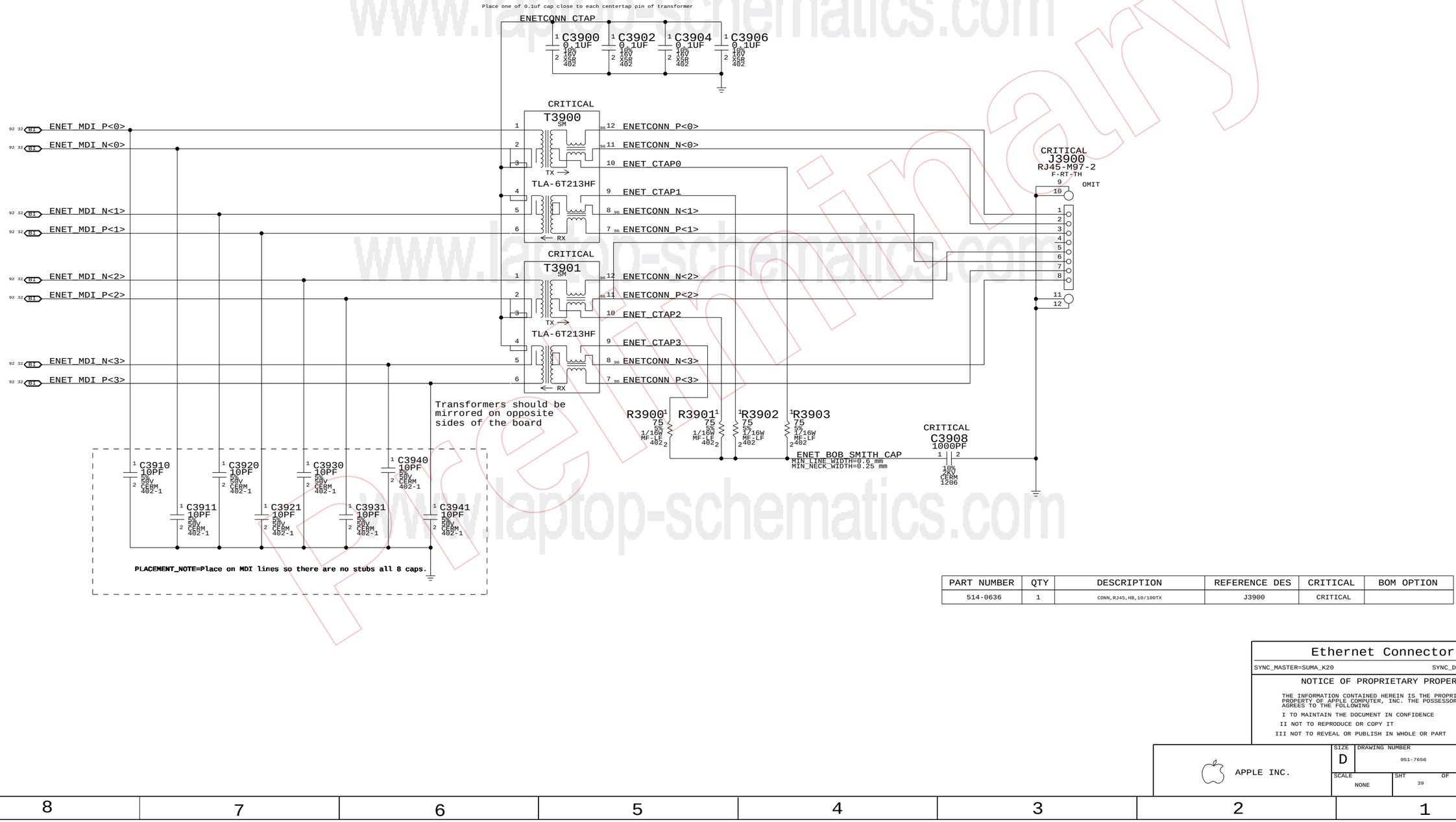
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 38 OF 123	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0636	1	CONN,RJ45,HB,10/100TX	J3900	CRITICAL	

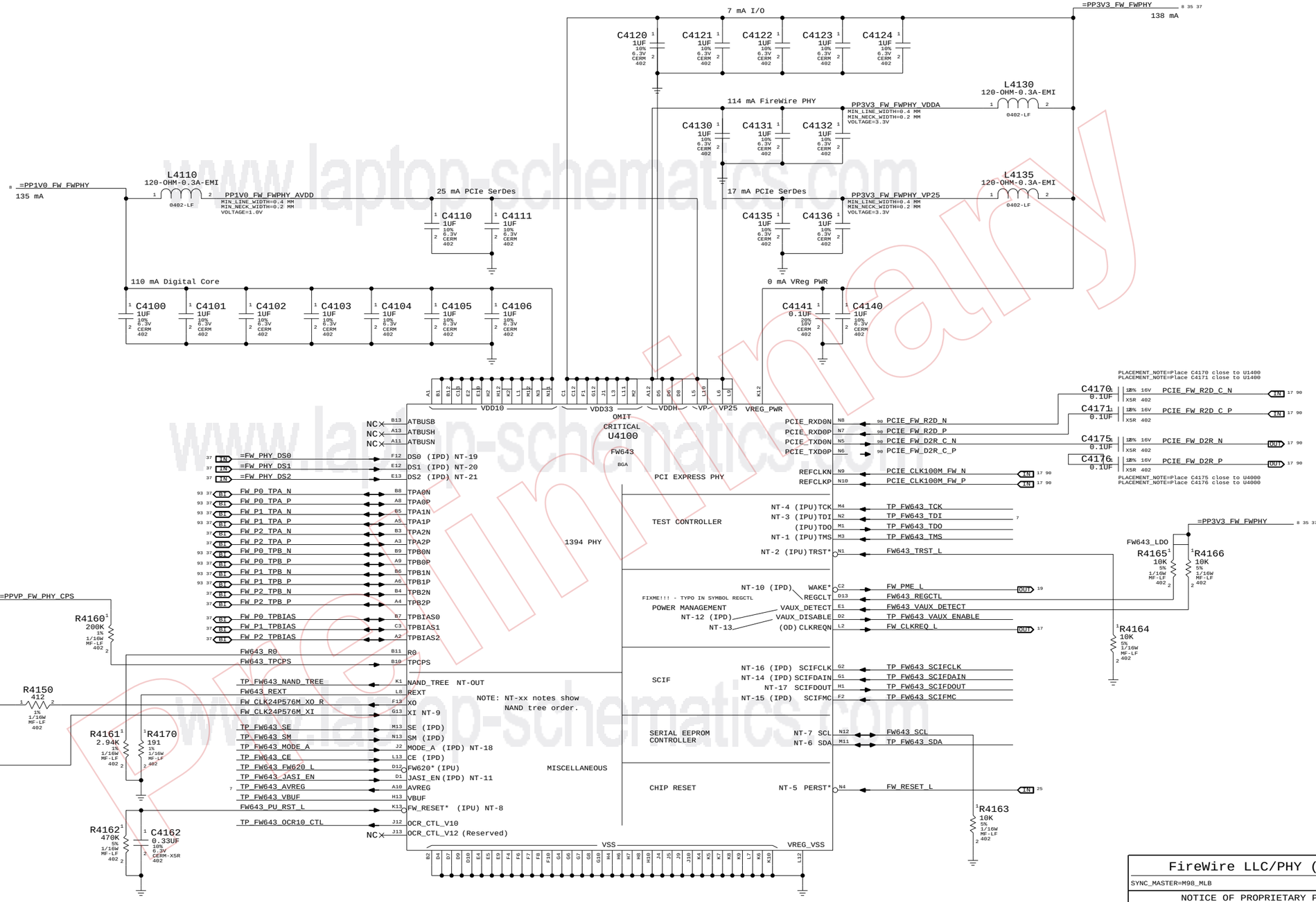
Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	39	123



FireWire LLC/PHY (FW643)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 41 OF 123	

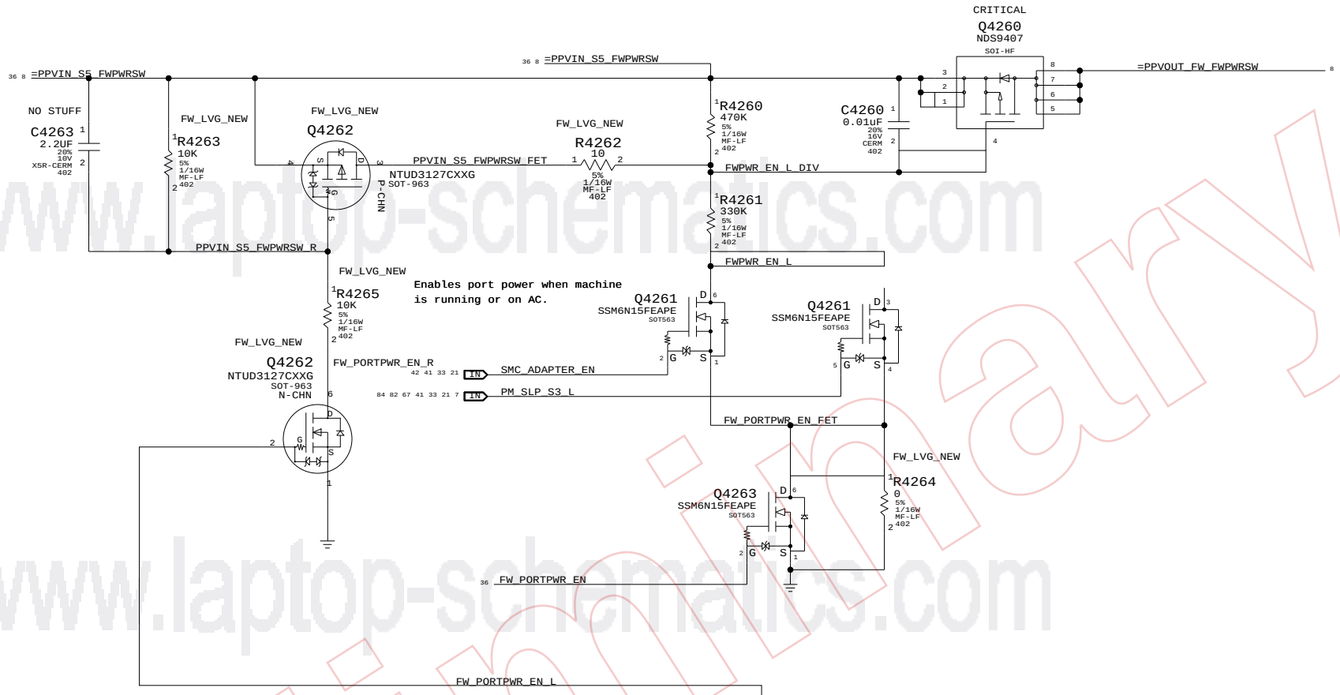
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

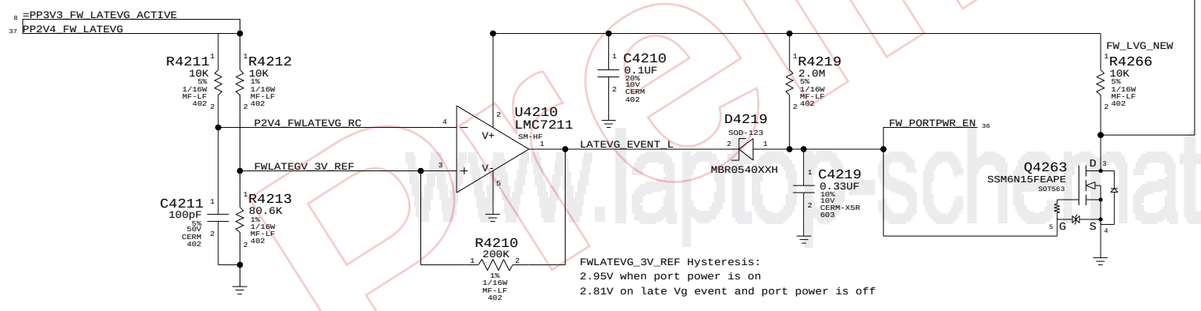
Signal aliases required by this page:
(NONE)

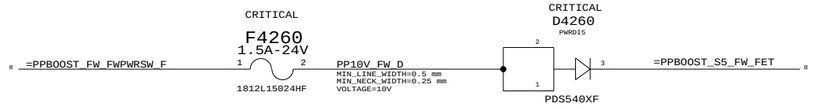
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection





FireWire Port Power		
SYNC_MASTER=YWU_K20	SYNC_DATE=05/28/2008	

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
	SCALE: NONE	SHT 42 OF 123	

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

=PP3V3_FW_FWPHY
R4382 10K 1% 1/16W MF-LF 402
R4380 10K 1% 1/16W MF-LF 402
FWPHY_DS0 MAKE_BASE=TRUE =FW_PHY_DS0
FWPHY_DS2 MAKE_BASE=TRUE =FW_PHY_DS2
FWPHY_DS1 MAKE_BASE=TRUE =FW_PHY_DS1
R4381 10K 1% 1/16W MF-LF 402

FW_P0_TPBIAS NC_FW0_TPBIAS MAKE_BASE=TRUE
FW_P2_TPBIAS NC_FW2_TPBIAS MAKE_BASE=TRUE
FW_P0_TPA_N NC_FW0_TPAN MAKE_BASE=TRUE
FW_P0_TPA_P NC_FW0_TPAP MAKE_BASE=TRUE
FW_P2_TPA_N NC_FW2_TPAN MAKE_BASE=TRUE
FW_P2_TPA_P NC_FW2_TPAP MAKE_BASE=TRUE
FW_P0_TPB_N NC_FW0_TPBN MAKE_BASE=TRUE
FW_P0_TPB_P NC_FW0_TPBP MAKE_BASE=TRUE
FW_P2_TPB_N NC_FW2_TPBN MAKE_BASE=TRUE
FW_P2_TPB_P NC_FW2_TPBP MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

FW_P1_TPBIAS
TI PHYs require 1uF even though FW spec calls out 0.33uF
C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

FW_P1_TPA_P MAKE_BASE=TRUE FW_PORT1_TPA_P
FW_P1_TPA_N MAKE_BASE=TRUE FW_PORT1_TPA_N
FW_P1_TPB_P MAKE_BASE=TRUE FW_PORT1_TPB_P
FW_P1_TPB_N MAKE_BASE=TRUE FW_PORT1_TPB_N

SIGNAL_MODEL=EMPTY
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

=PP3V3_FW_LATEVG
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V
CRITICAL
D4390 MMBZ5227BLT1H SOT23

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

ESD and late-VG rail for snap-back diodes (Common to all ports)

"Snapback" & "Late VG" Protection

=PPVP_FW_PHY_CPS_FET
R4311 470K 5% 1/16W MF-LF 402
CPS_EN_L_DIV
R4312 330K 5% 1/16W MF-LF 402
CPS_EN_L
Q4300 BSS8402DW SOT-363 (SYM-VER1)
=PP3V3_FW_FWPHY
PPVP_FW_CPS MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=10V MAKE_BASE=TRUE =PPVP_FW_PHY_CPS

PP2V4_FW_LATEVG
DP4310 BAV99DW-X-G SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402
DP4311 BAV99DW-X-G SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402

FW_PORT1_TPB_N
FW_PORT1_TPB_P
FW_PORT1_TPA_N
FW_PORT1_TPA_P

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

Cable Power

=PPVP_FW_PORT1
CRITICAL
L4310 FERR-250-OHM SM
Note: Trace PPVP_FW_PORT1 must handle up to 5A
PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4314 0.01UF 10% 50V X7R 402
C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

PORT 1

BILINGUAL

CRITICAL
J4310 1394B-M97 F-RT-TH

(FW_PORT1_BREF)
(GND_FW_PORT1_VG)
FW_PORT1_AREF
NC

OUTPUT: TPB- TPB(R) TPB<R> TPB+ VP NC SC/NC VG TPA- TPA<R> TPA+
INPUT: TPA- VG TPA+ TPA(R)
CHASSIS GND

514S0605

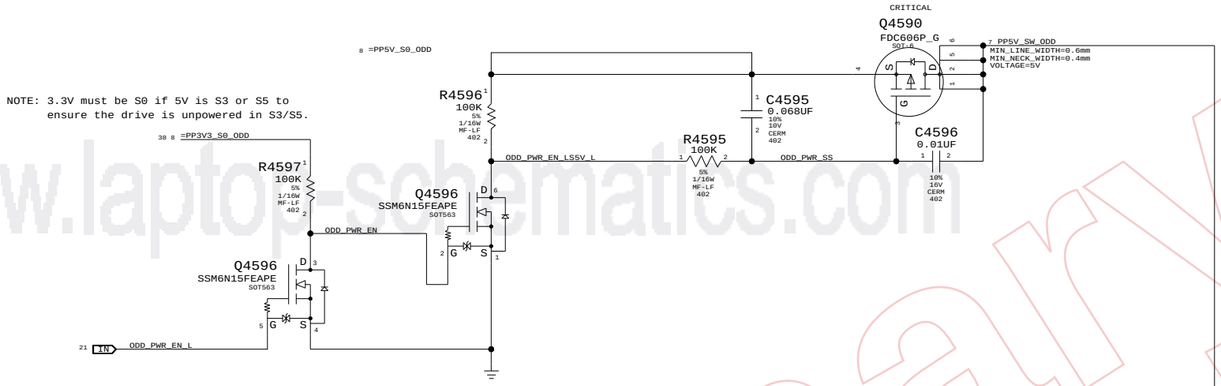
FireWire Ports

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

APPLE INC.

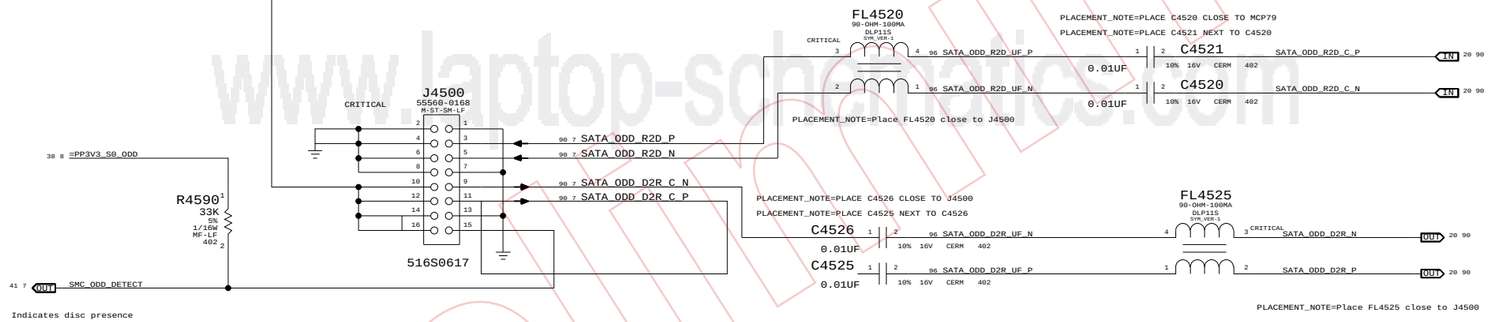
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 43 OF 123	

ODD Power Control

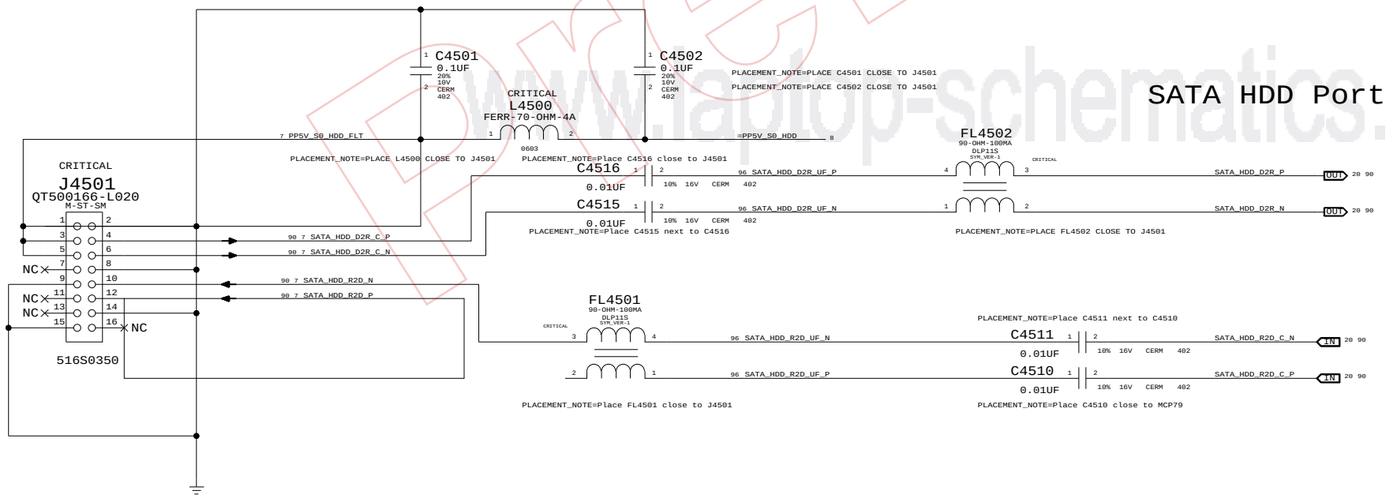


NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

SATA ODD Port



SATA HDD Port



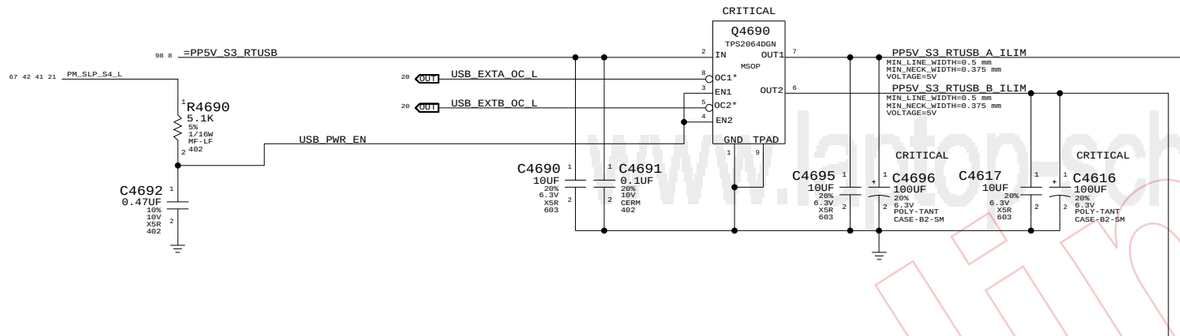
SATA Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

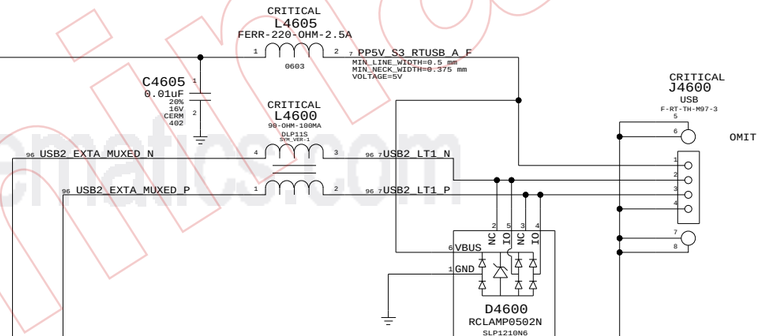
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 45 OF 123	

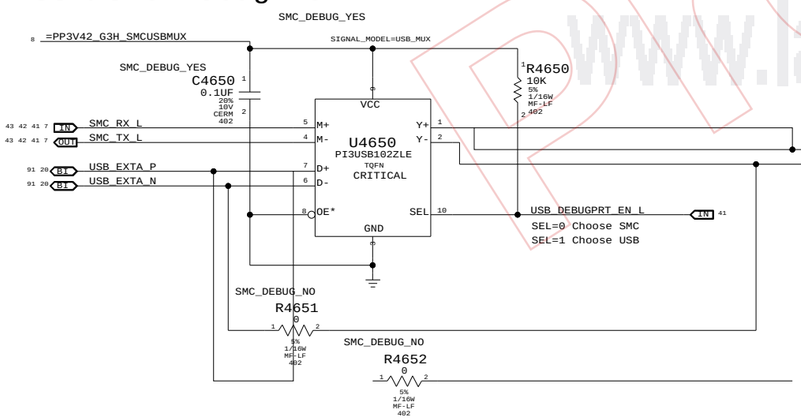
Port Power Switch



Left USB Port A



USB/SMC Debug Mux



Left USB Port B

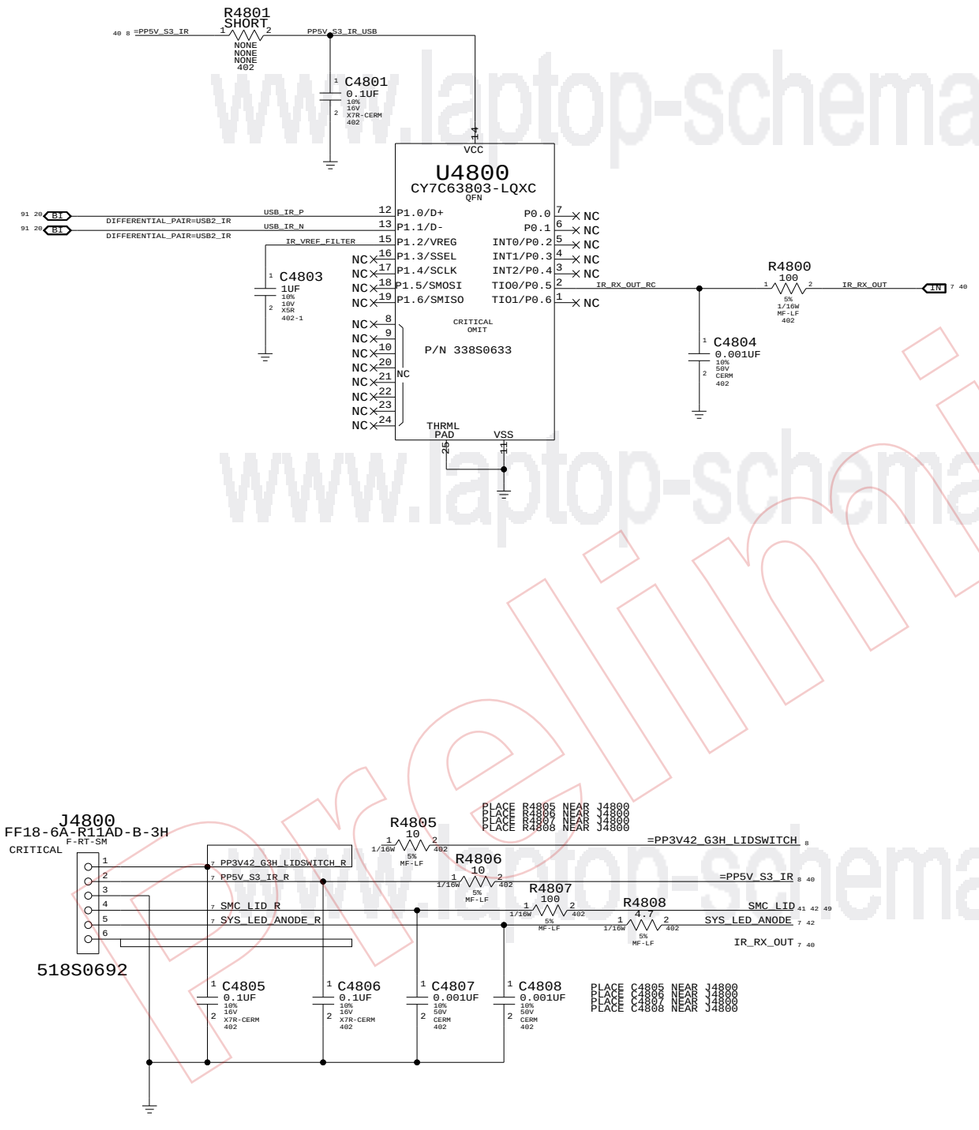
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN,RCPT,USB,HB,4P	J4600, J4610	CRITICAL	

External USB Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 46 OF 123	



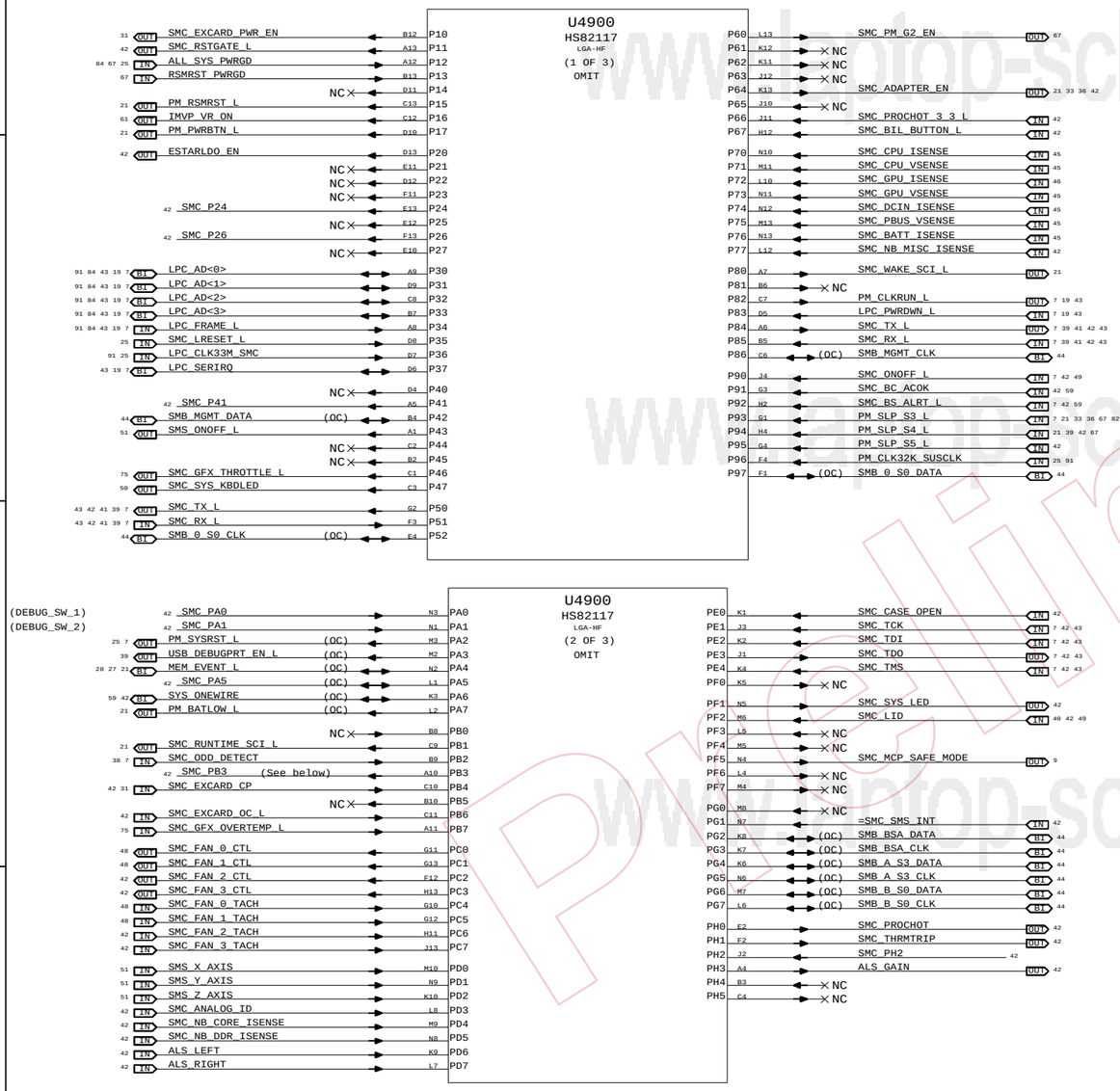
Front Flex Support

SYNC_MASTER=CHANG_K20 SYNC_DATE=07/18/2008

APPLE INC.

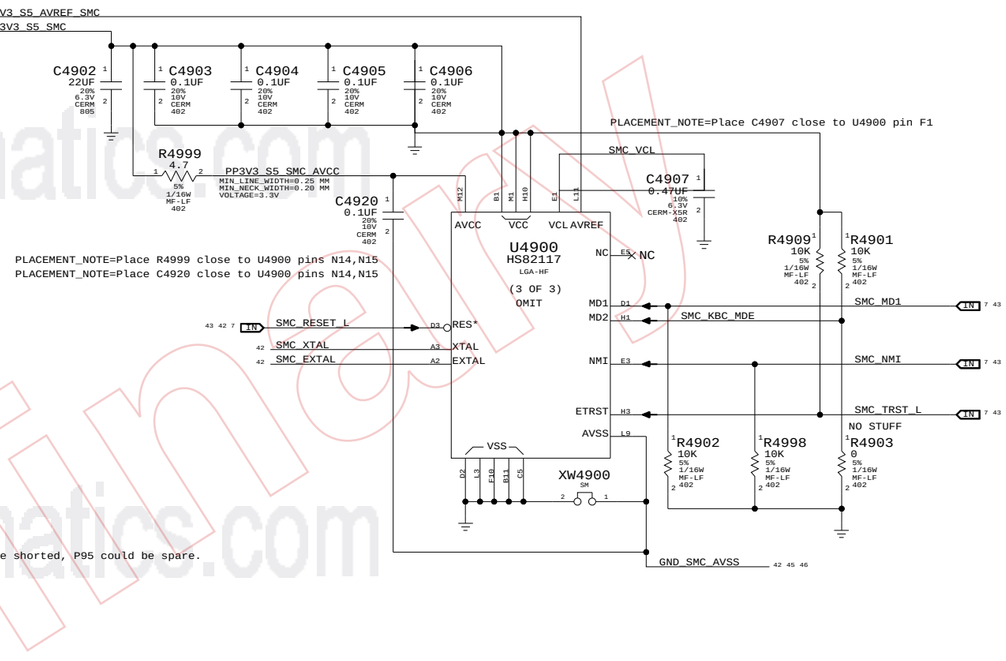
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	48	123

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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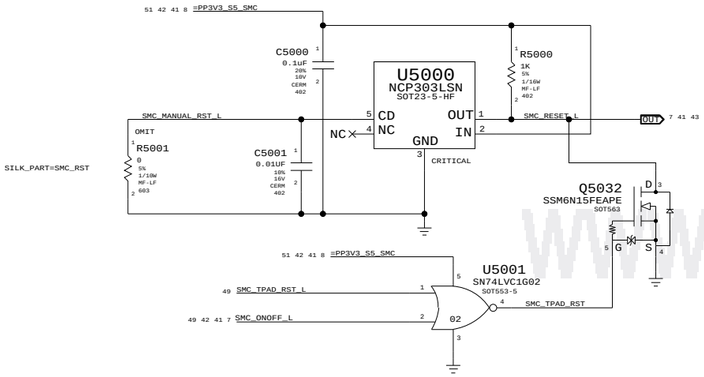
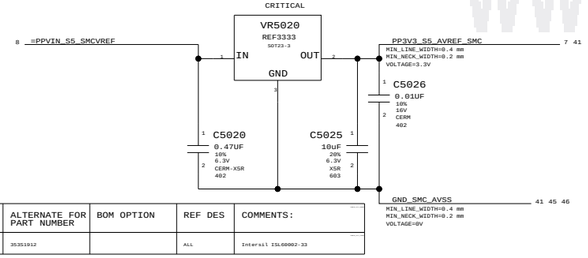
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	49	123

SMC Reset "Button" / Brownout Detect

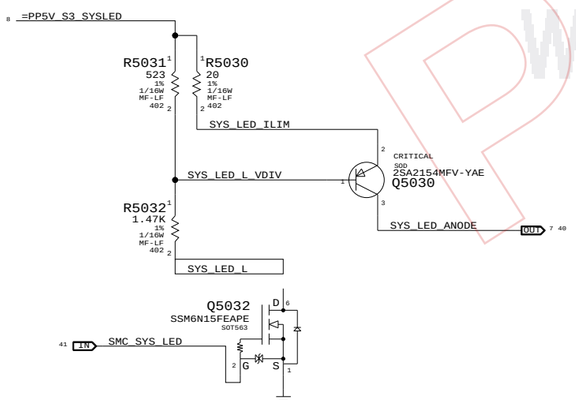


SMC AVREF Supply

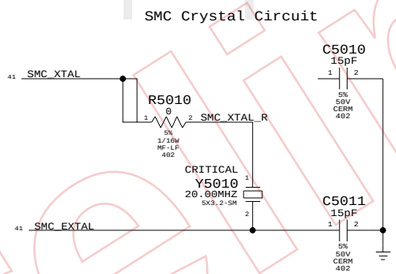


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

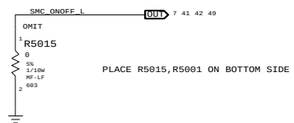
System (Sleep) LED Circuit



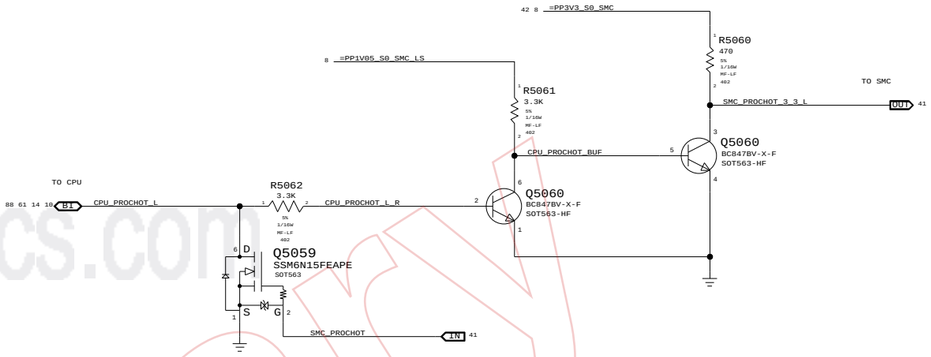
SMC Crystal Circuit



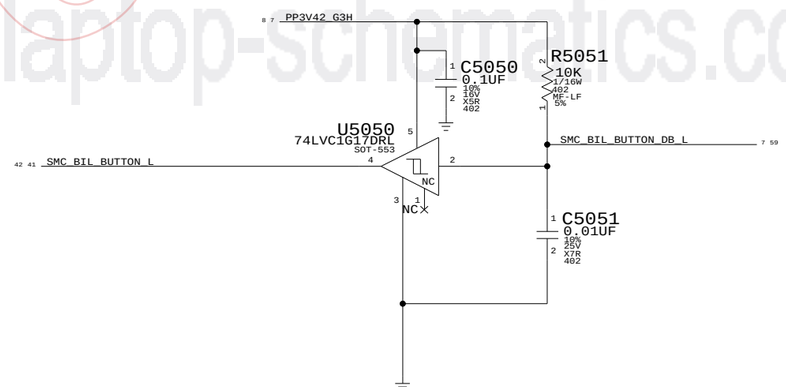
Debug Power "Button"



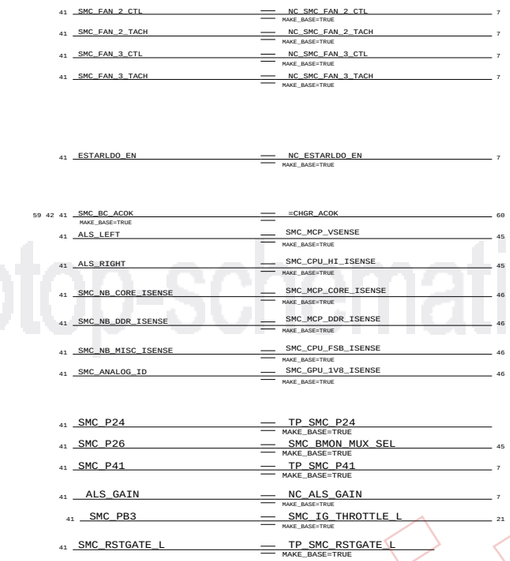
SMC FSB to 3.3V Level Shifting



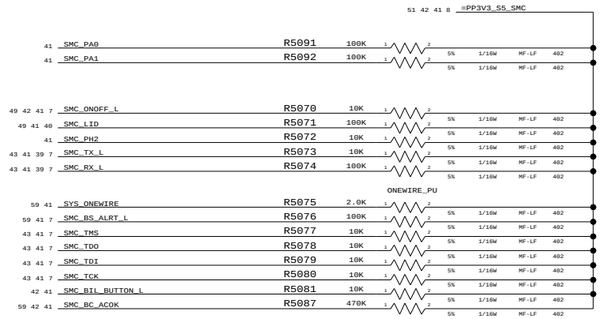
PP3V42_G3H



Signal Connections



Pull-ups



SMC Support

SYNC_MASTER=M98_MLB — SYNC_DATE=05/01/2008

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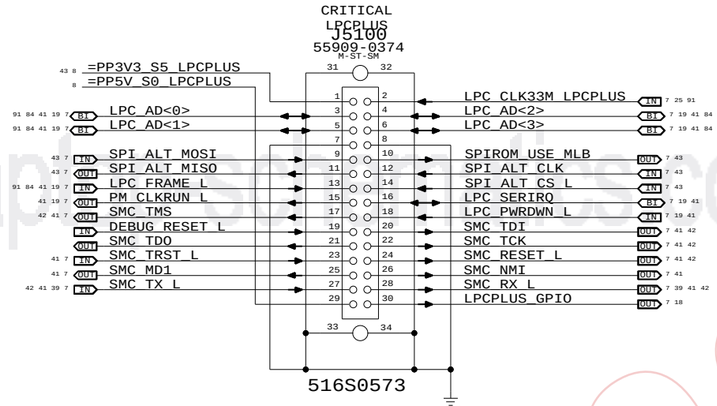
APPLE INC.

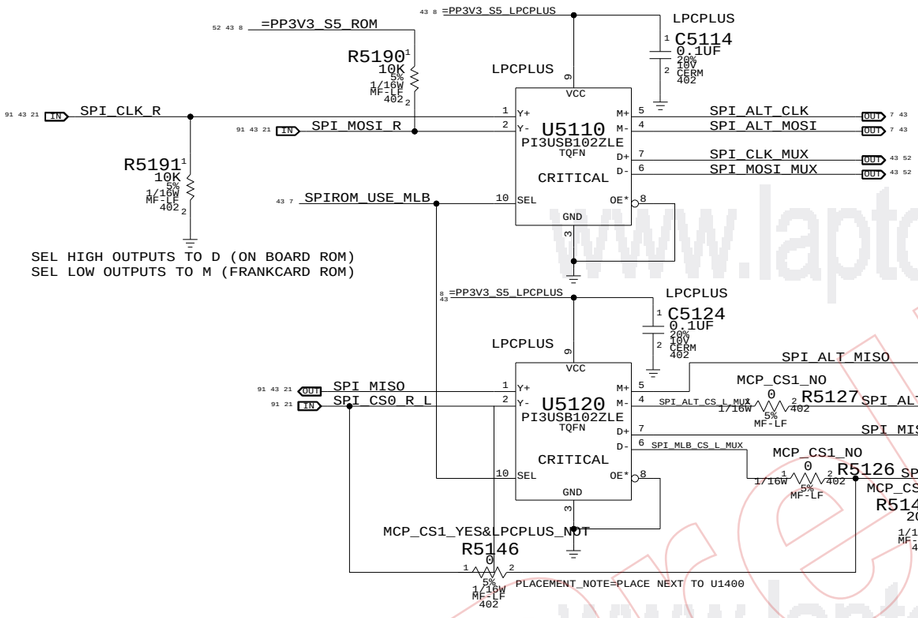
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 50 OF 123	

LPC+SPI Connector



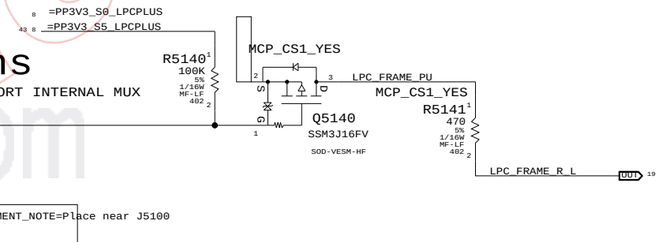
Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP



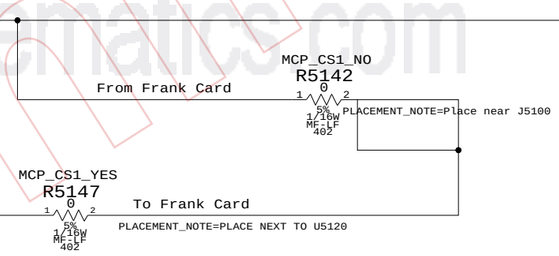
MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON



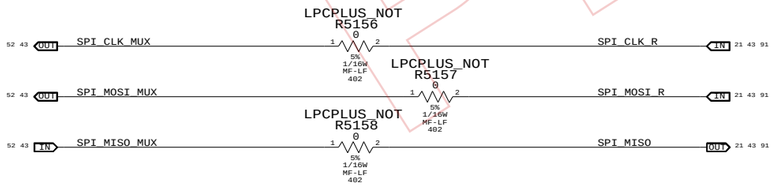
MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX



SPI_CS1_R_L_USE_MLB
MAKE_BASE=TRUE
=SPI_CS1_R_L_USE_MLB

SPI MUX BYPASS



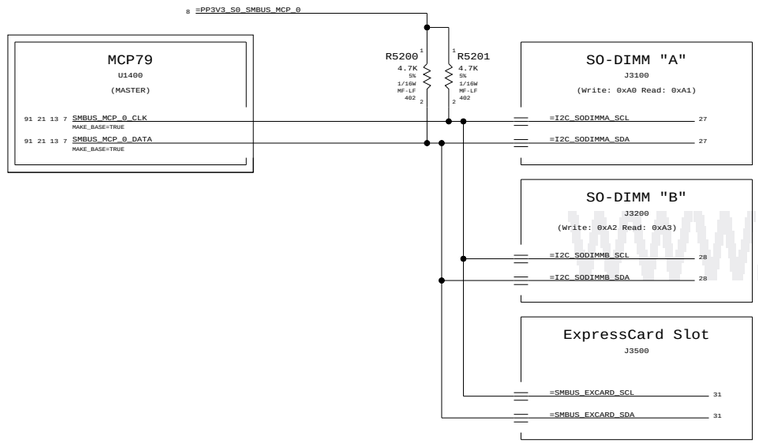
LPC+SPI Debug Connector

SYNC_MASTER=CHANG_K20 SYNC_DATE=05/28/2008

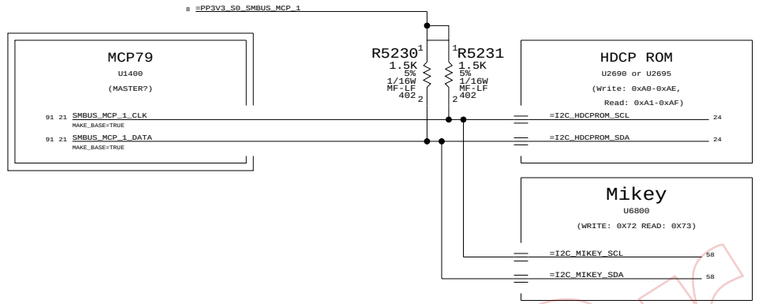
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 51 OF 123	

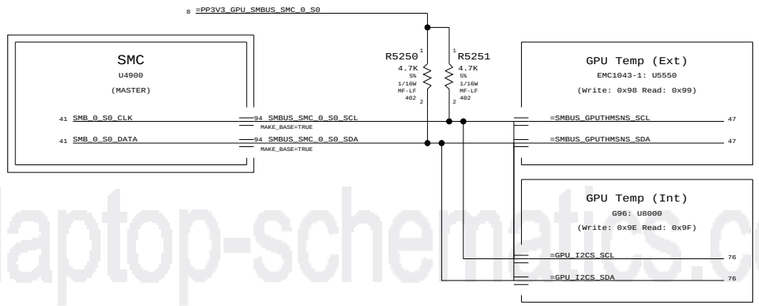
MCP79 SMBus "0" Connections



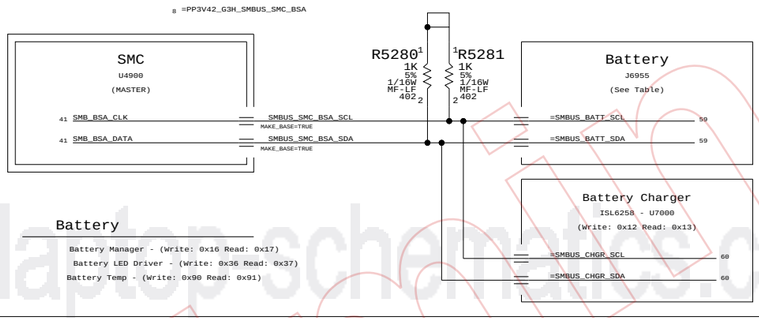
MCP79 SMBus "1" Connections



SMC "0" SMBus Connections

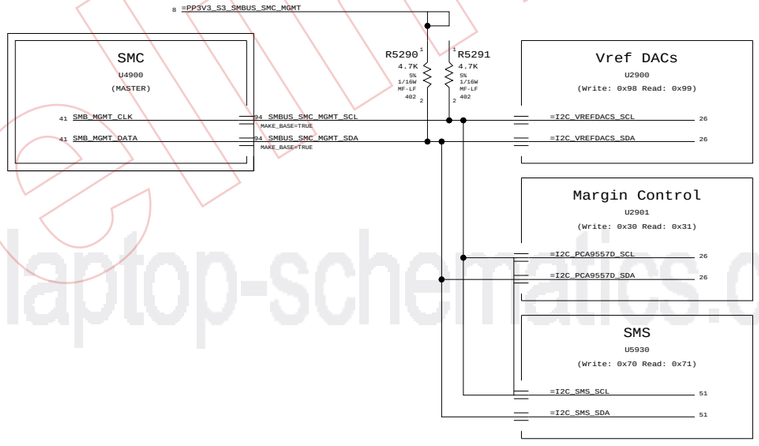


SMC "Battery A" SMBus Connections



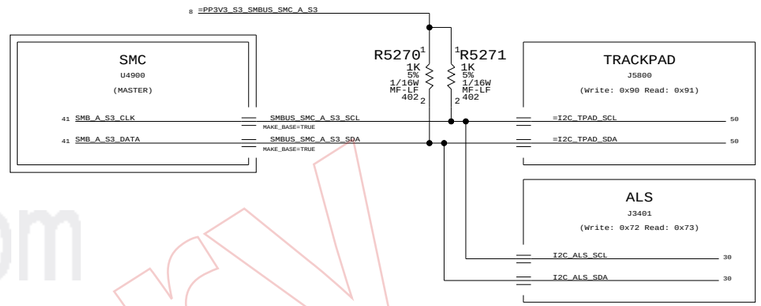
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

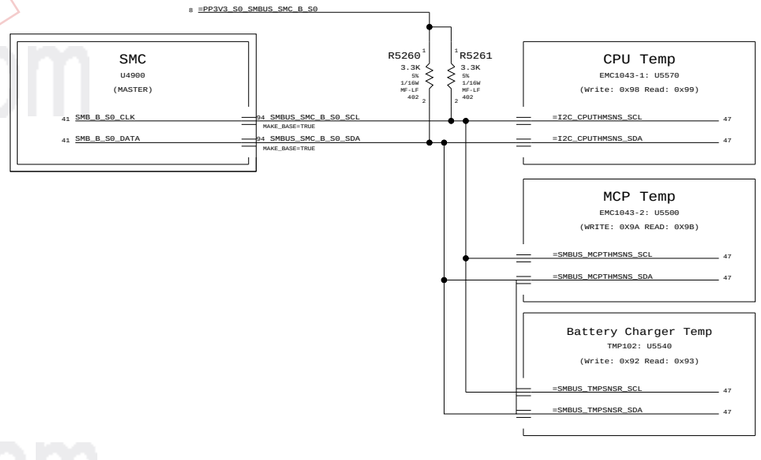


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



K20 SMBUS CONNECTIONS

SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	52	123

CPU Voltage Sense / Filter

12 11 8 =PPVCORE_S0_CPU — XW5309 (SM) — CPUVSENSE_IN — R5309 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_VSENSE OUT 41

Place short near U1000 center

C5309 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

Place RC close to SMC

GPU Voltage Sense / Filter

77 8 =PPVCORE_GPU_REG — XW5359 (SM) — GPUVSENSE_IN — R5359 4.53K 1% 1/16W MF-LF 402 — SMC_GPU_VSENSE OUT 41

Place short near U8000 center

C5359 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

Place RC close to SMC

MCP Voltage Sense / Filter

23 22 8 =PPVCORE_S0_MCP — XW5399 (SM) — MCPVSENSE_IN — R5399 4.53K 1% 1/16W MF-LF 402 — SMC_MCP_VSENSE OUT 42

PLACEMENT_NOTE=Place near U1400 center

C5399 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

Place RC close to SMC

PBUS Voltage Sense & Filter

Q5315 FDG6332CG SC70-6 P-CHN

8 7 PPBUS_G3H — R5315 100K 1% 1/16W MF-LF 402 — PPBUS_G3H_VSENSE

MIN_LINE_WIDTH=0.20 mm
MIN_NECK_WIDTH=0.20 mm
VOLTAGE=18.5V

PBUSVSENS_EN_DIV

R5316 100K 1% 1/16W MF-LF 402

PBUSVSENS_EN_L

67 =PBUSVSENS_EN

Enables PBUS VSense divider when high.

Q5315 FDG6332CG SC70-6 N-CHN

R5385 12.7K 1% 1/16W MF-LF 402 — SMC_PBUS_VSENSE OUT 41

Rthevenin = 4504 ohms

R5386 6.98K 1% 1/16W MF-LF 402

C5385 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

Place RC close to SMC

BMON Current Sense - Entire circuit must be near SMC (U4900)

8 =PP3V42_G3H_BMON_ISNS

C5318 0.1uF 20% 10V CERM 402

REGULATOR SIDE:

U5303 INA214 SC70 — V+ — IN- — IN+ — OUT — REF — GND

96 60 OUT CHGR_CSO_R_P

96 60 IN CHGR_CSO_R_N

LOAD SIDE:

Monitors battery discharge
current from battery to PBUS

BMON_INA_OUT

U5313 NC7SB3157P6XG SC70 — B1 — SEL — GND — VCC — B0 — A — VER 1

60 IN CHGR_BMON

BMON_PROD R5330 0 5% 1/16W MF-LF 402

BMON_AMUX_OUT

R5371 100K 5% 1/16W MF-LF 402

R5391 4.53K 1% 1/16W MF-LF 402 — SMC_BATT_ISENSE OUT 41

C5390 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

C5369 0.1uF 20% 10V CERM 402

SMC_BMON_MUX_SEL IN 42

INA214 has gain of 100V/V
U5303 only senses current up to 6.6A

DCIN Current Sense Filter

Place RC close to SMC

60 IN CHGR_AMON — R5380 4.53K 1% 1/16W MF-LF 402 — SMC_DCIN_ISENSE OUT 41

C5380 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

CPU VCore High Side Current Sensor

8 =PP3V42_G3H_CPUCOREISNS

C5388 0.1UF 20% 10V CERM 402

8 OUT =PPVIN_S5_CPU_IMVP_ISNS

R5388 0.001 1% 1W MF 1206

8 IN =PPVIN_S5_CPU_IMVP_ISNS_R

96 ISNS_CPU_N

96 ISNS_CPU_P

U5388 INA210 SC70 — V+ — IN- — IN+ — OUT — REF — GND

CPUVCORE_HISIDE_IOUT

R5335 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_HI_ISENSE OUT 42

C5335 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

Place RC close to SMC

Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

CPU VCore Load Side Current Sense / Filter

Place RC close to SMC

61 IN IMVP6_IMON — R5331 6.19K 1% 1/16W MF-LF 402 — SMC_CPU_ISENSE OUT 41

R5332 17.4K 1% 1/16W MF-LF 402

C5330 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 41 42 45 46

Current & Voltage Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/20/2008

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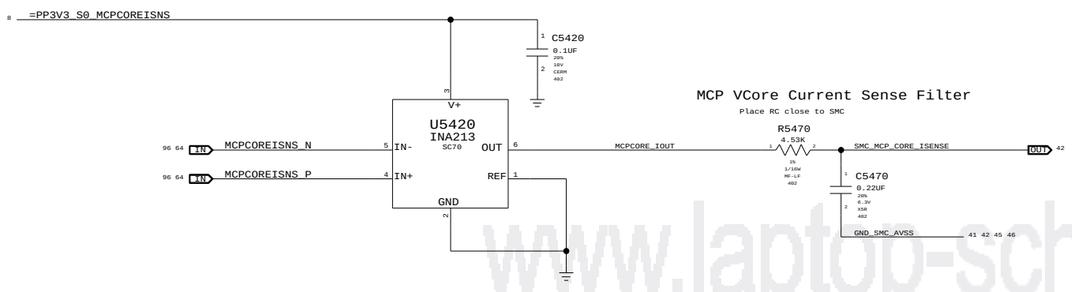
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 53 OF 123	

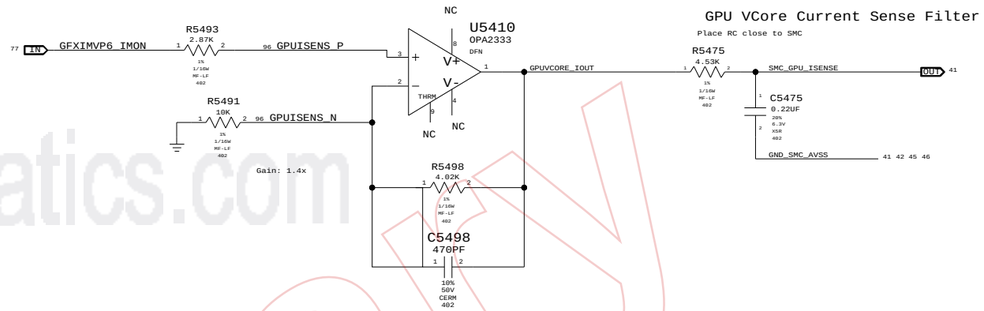
MCP VCore Current Sense



MCP VCore Current Sense Filter

Place RC close to SMC

GPU VCore Current Sense

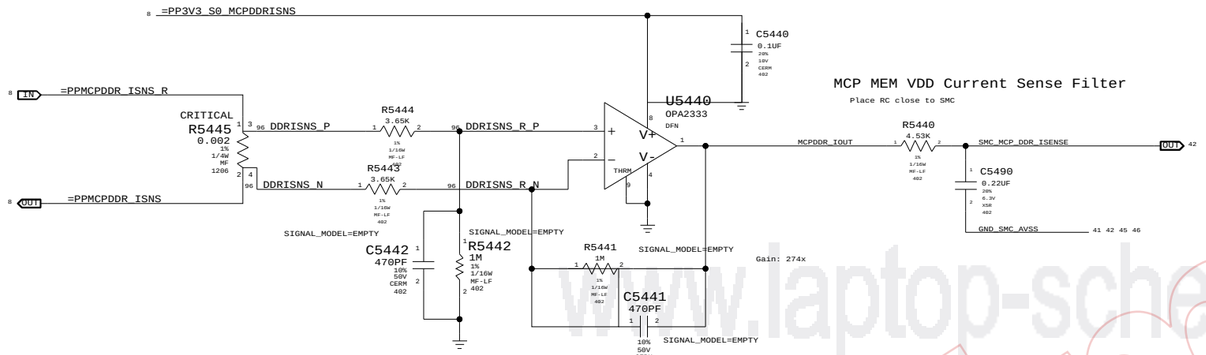


GPU VCore Current Sense Filter

Place RC close to SMC

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

MCP MEM VDD Current Sense



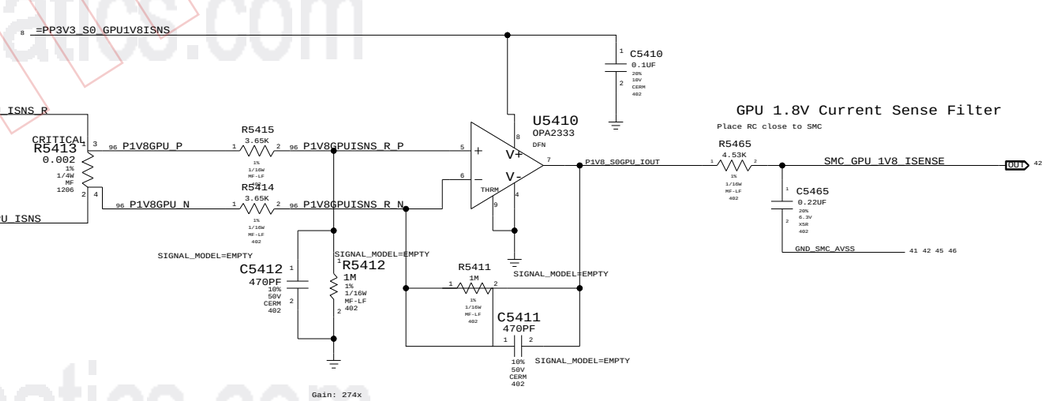
MCP MEM VDD Current Sense Filter

Place RC close to SMC

OPA2333s for proto are placeholders for OPA2330

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

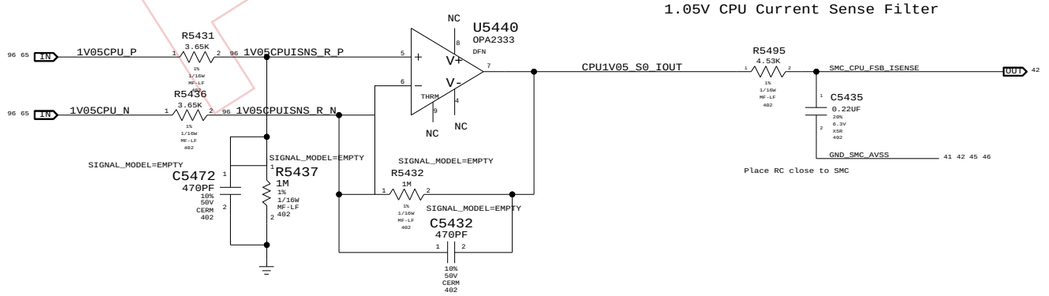
GPU 1.8V Current Sense



GPU 1.8V Current Sense Filter

Place RC close to SMC

CPU FSB 1.05V Current Sense



1.05V CPU Current Sense Filter

Place RC close to SMC

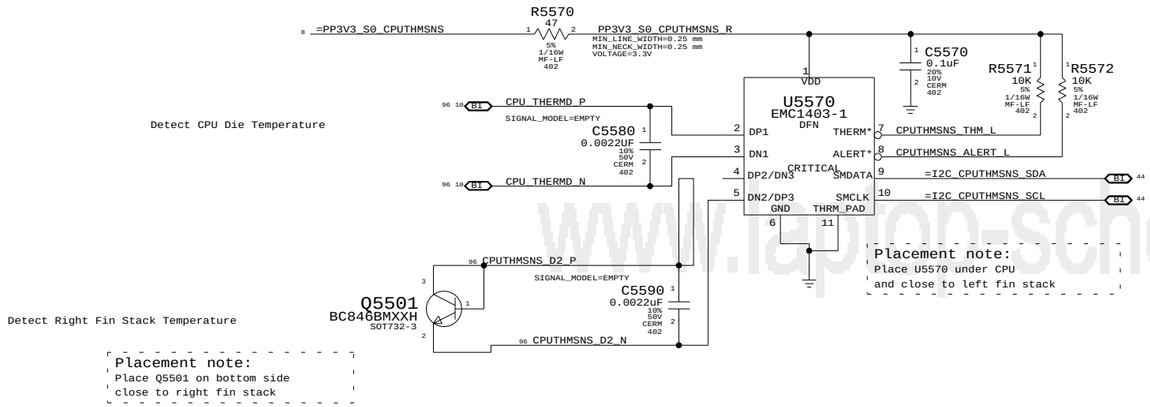
Current Sensing

SYNC_MASTER=YWU_K20 SYNC_DATE=08/12/2008

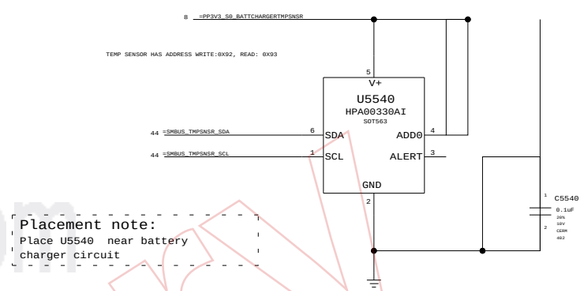
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	54	123

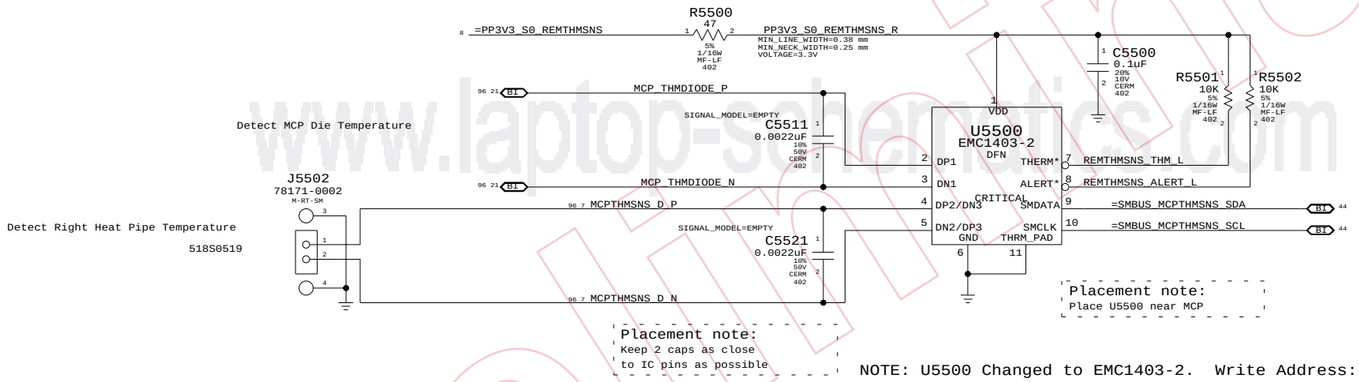
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity



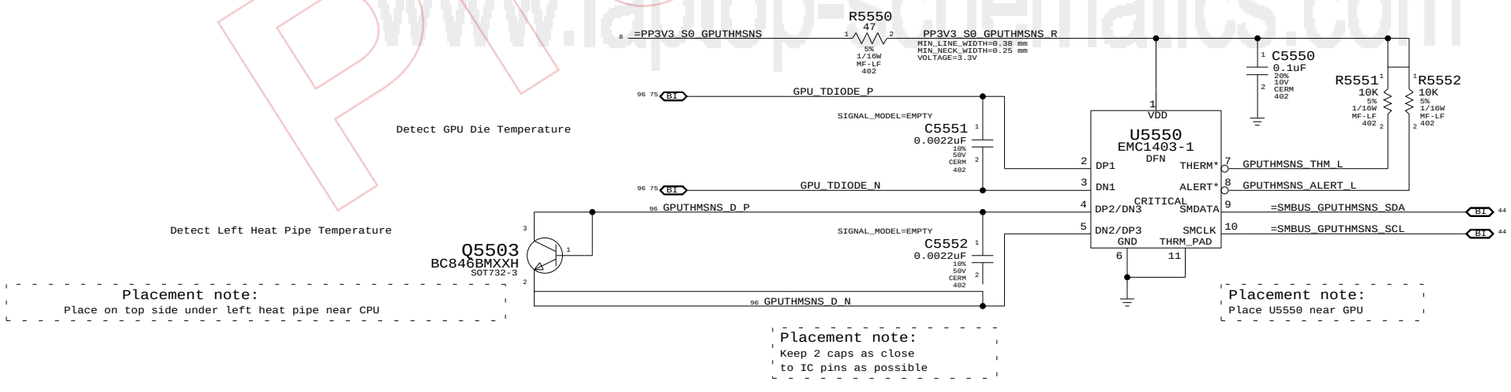
MCP Proximity/MCP Die/Right Heat Pipe



Note: EMC1403 can perform Beta
Compensation for External Diode 1 only

NOTE: U5500 Changed to EMC1403-2. Write Address: 0x9A

GPU Proximity/GPU Die/Left Heat Pipe



Thermal Sensors

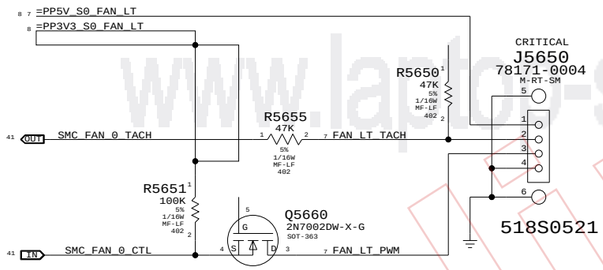
SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

APPLE INC.

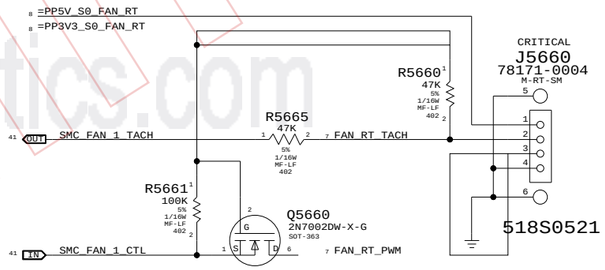
SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	55	123

Left Fan



Right Fan



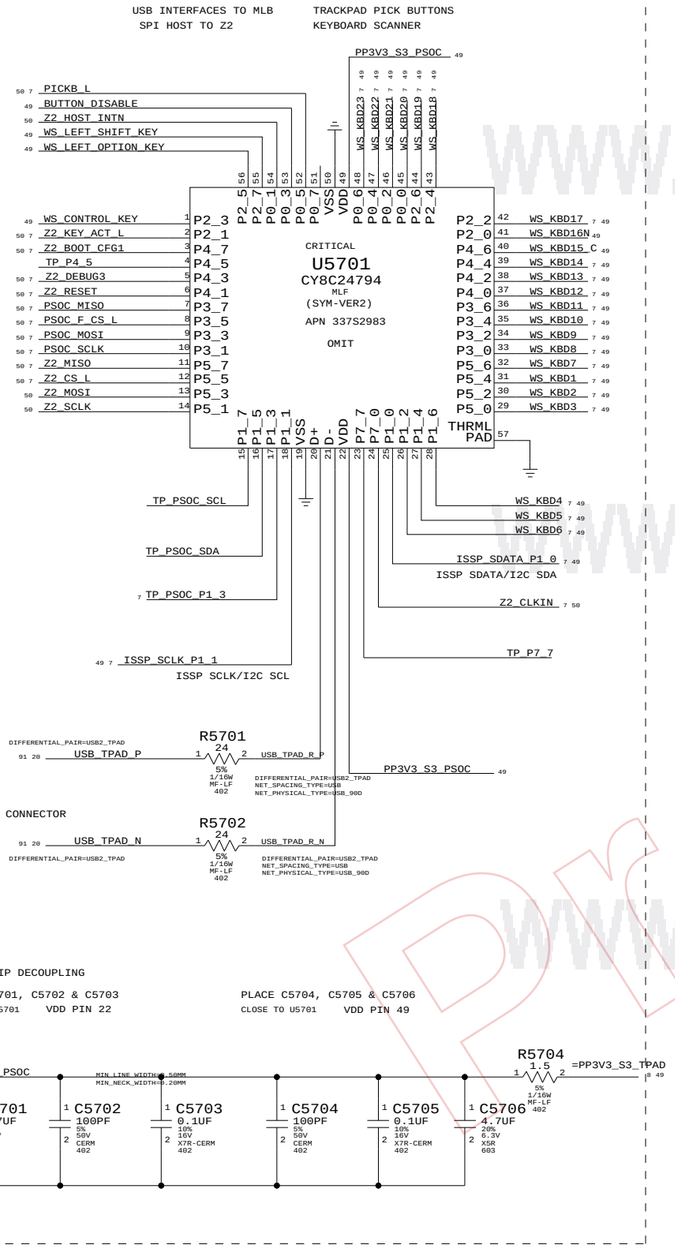
Fan Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

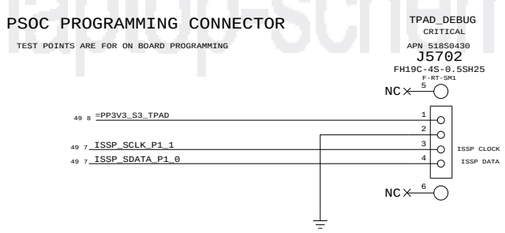
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	56	123

PSOC USB CONTROLLER

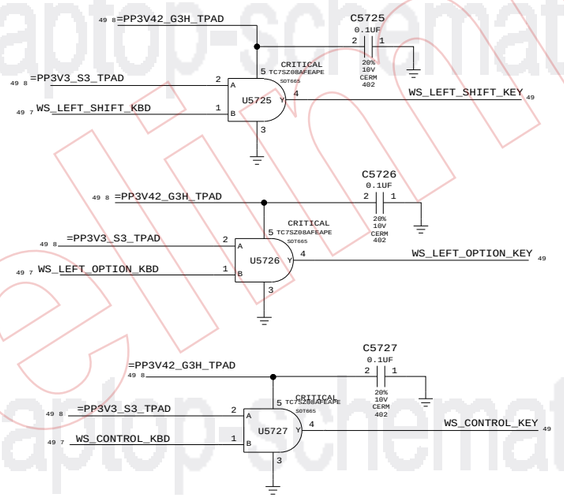


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

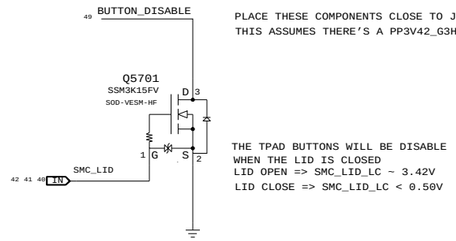
PSOC PROGRAMMING CONNECTOR



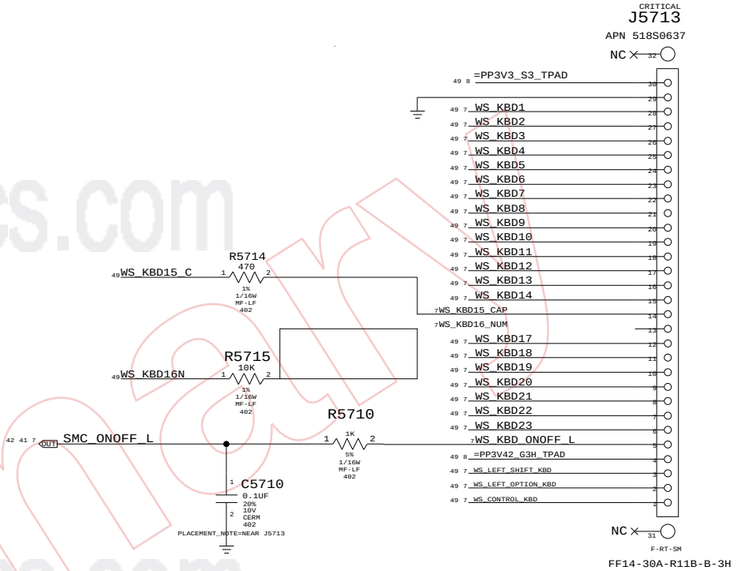
ISOLATION CIRCUIT



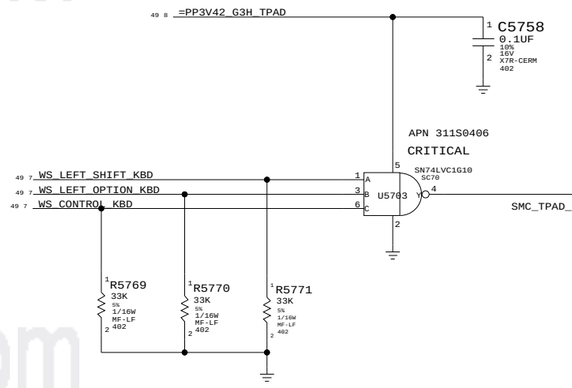
TPAD BUTTONS DISABLE



KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC

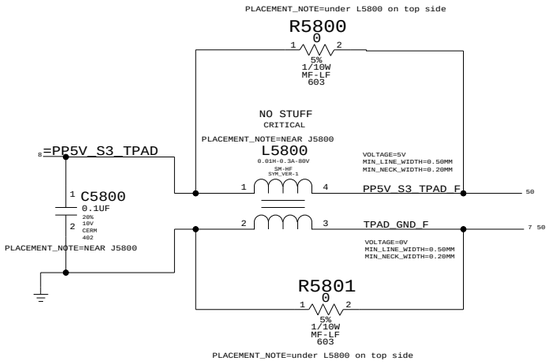


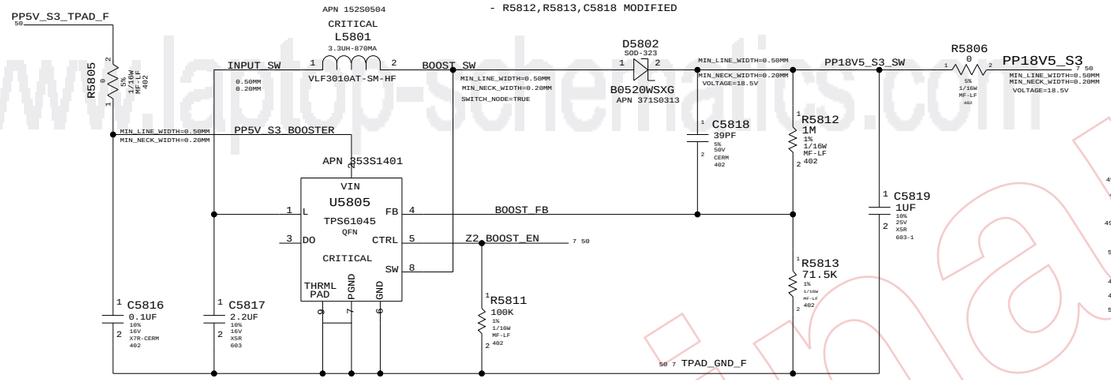
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	57	123

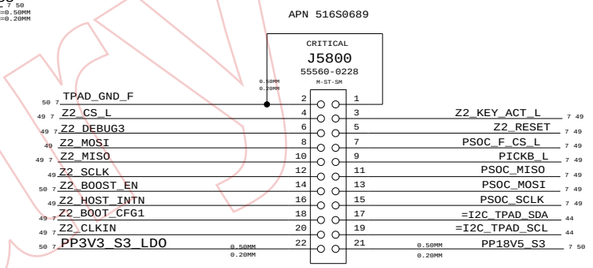
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

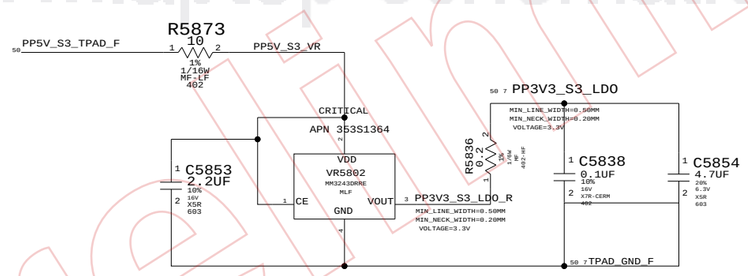




IPD FLEX CONNECTOR



3V3 LDO FOR IPD



Keyboard LED Driver

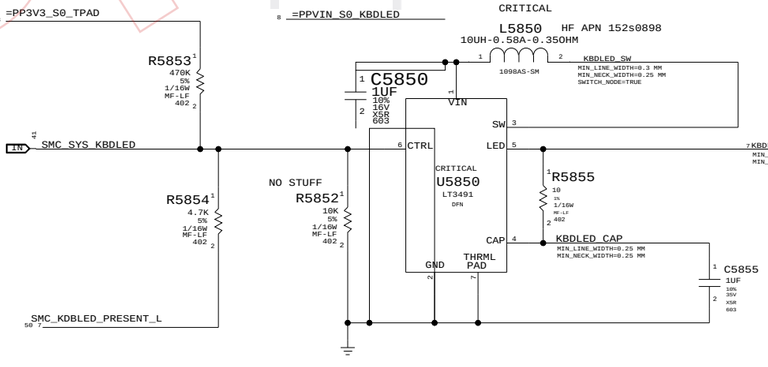
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

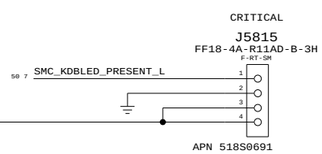
LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





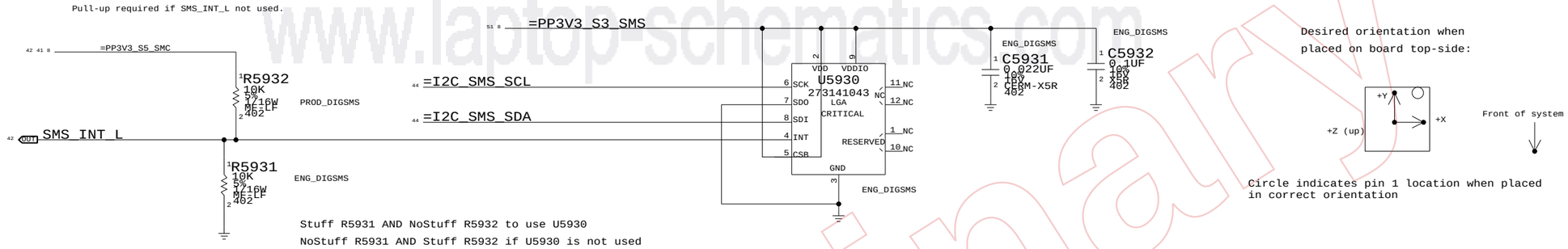
J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

APPLE INC.

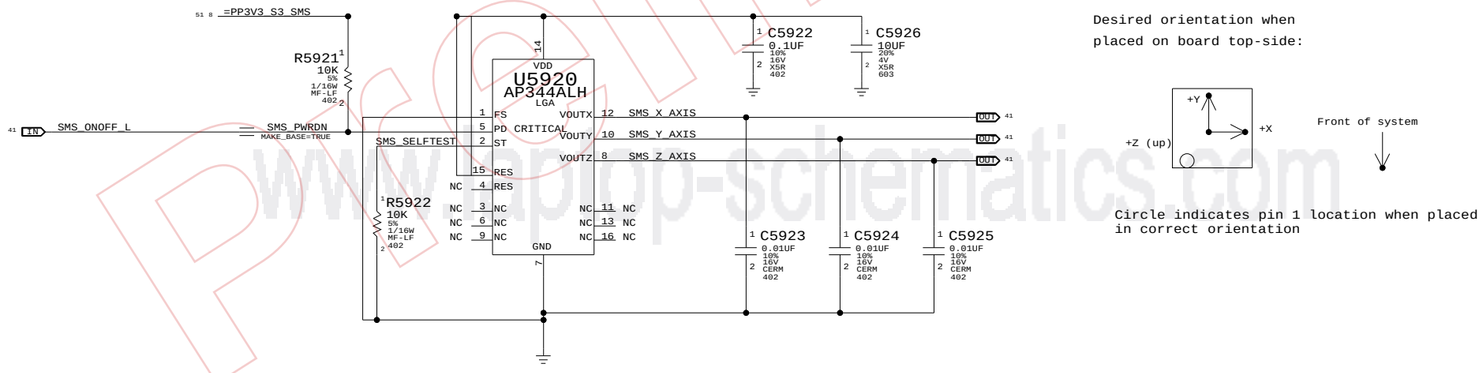
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 58 OF 123	

Digital SMS



Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

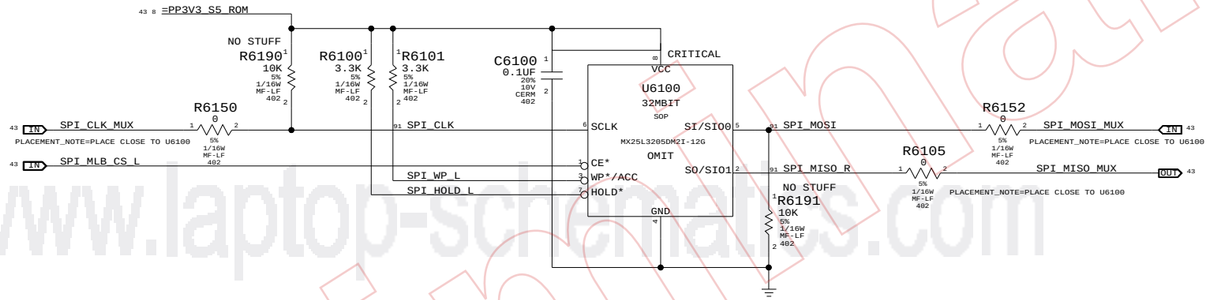


Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 59 OF 123	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

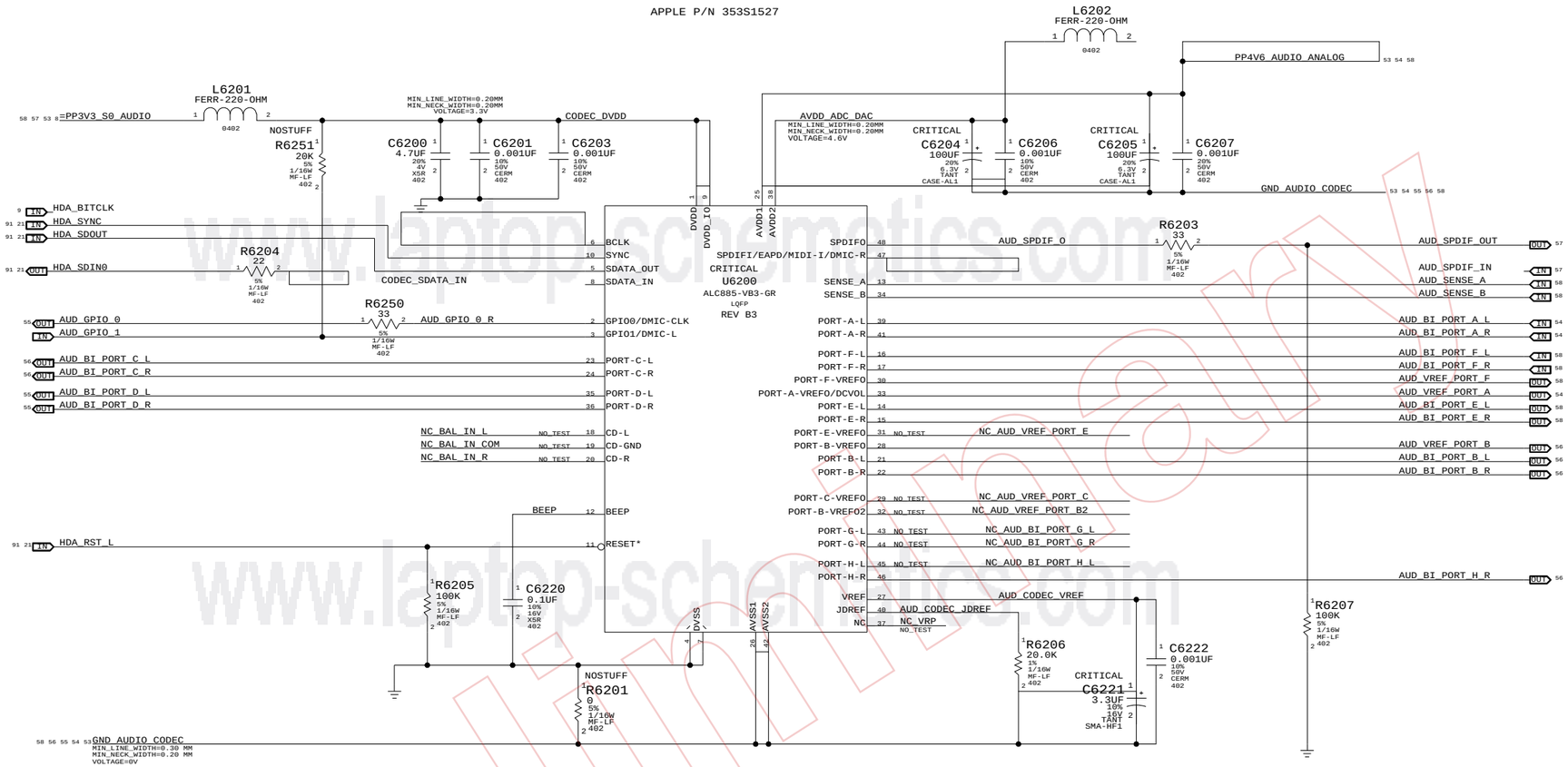
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	61	123

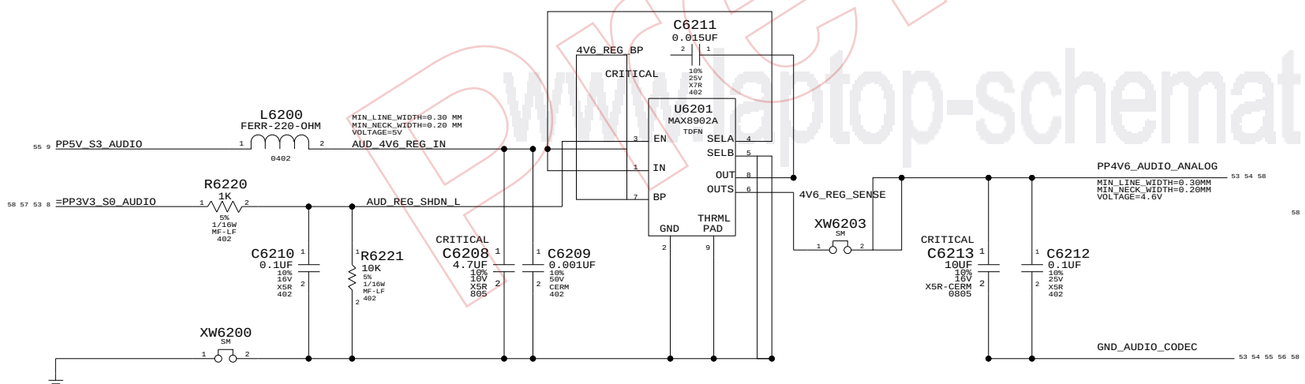
AUDIO CODEC

APPLE P/N 353S1527



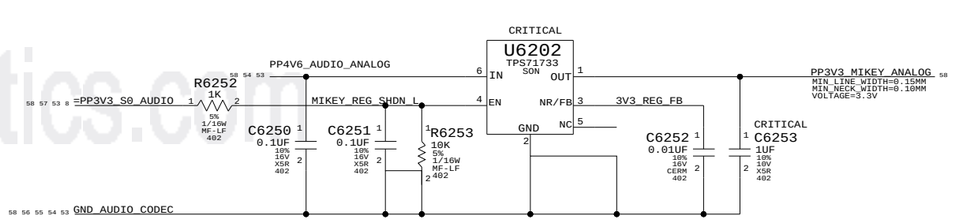
AUDIO 4.6 V REGULATOR

APPLE P/N 353S1897



MIKEY 3.3 V REGULATOR

APPLE P/N 353S1860



AUDIO:CODEC

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

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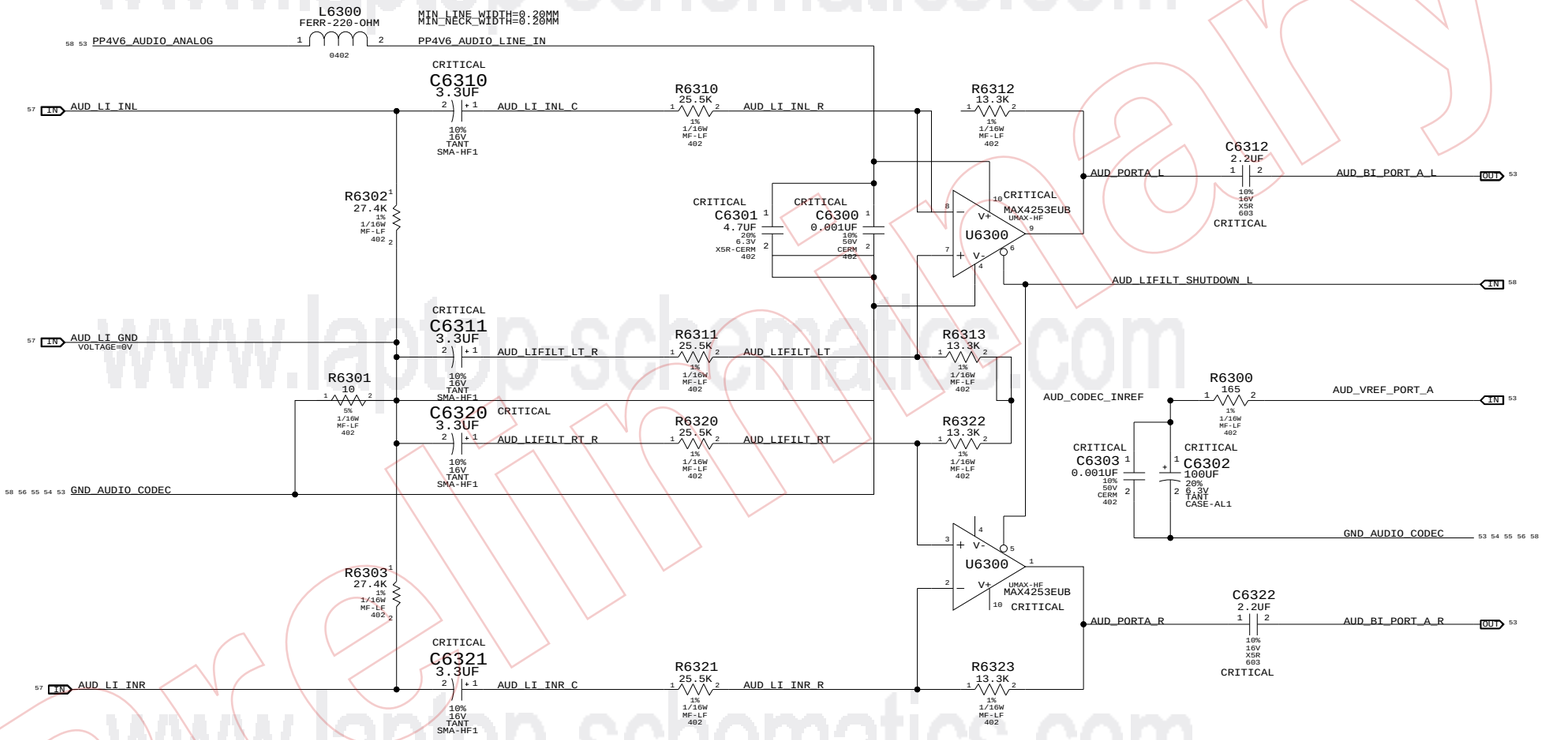
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 62 OF 123	

Pseudo-Diff Line-In Filter
GAIN = -5.4 DB AV = 0.52
FC = 1.89 HZ



AUDIO: LINE IN

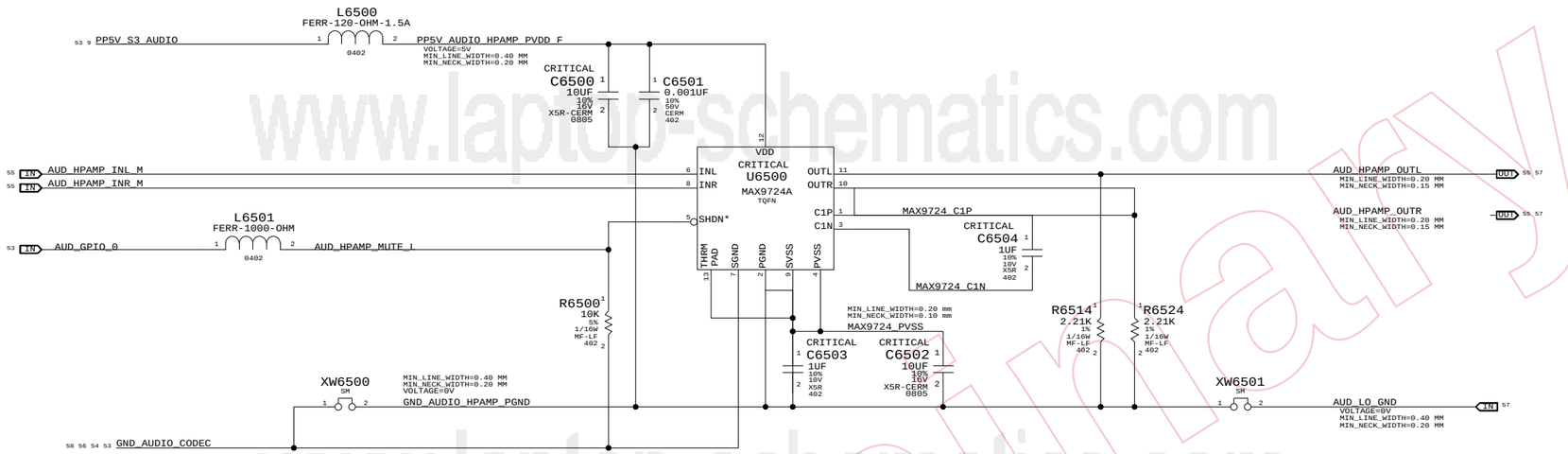
SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 63 OF 123	

Headphone Amplifier (MAX9724A)

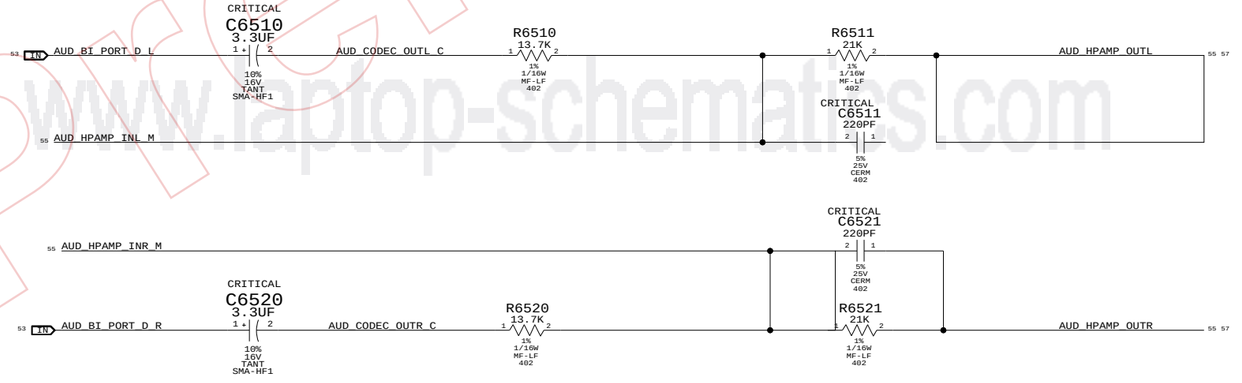
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

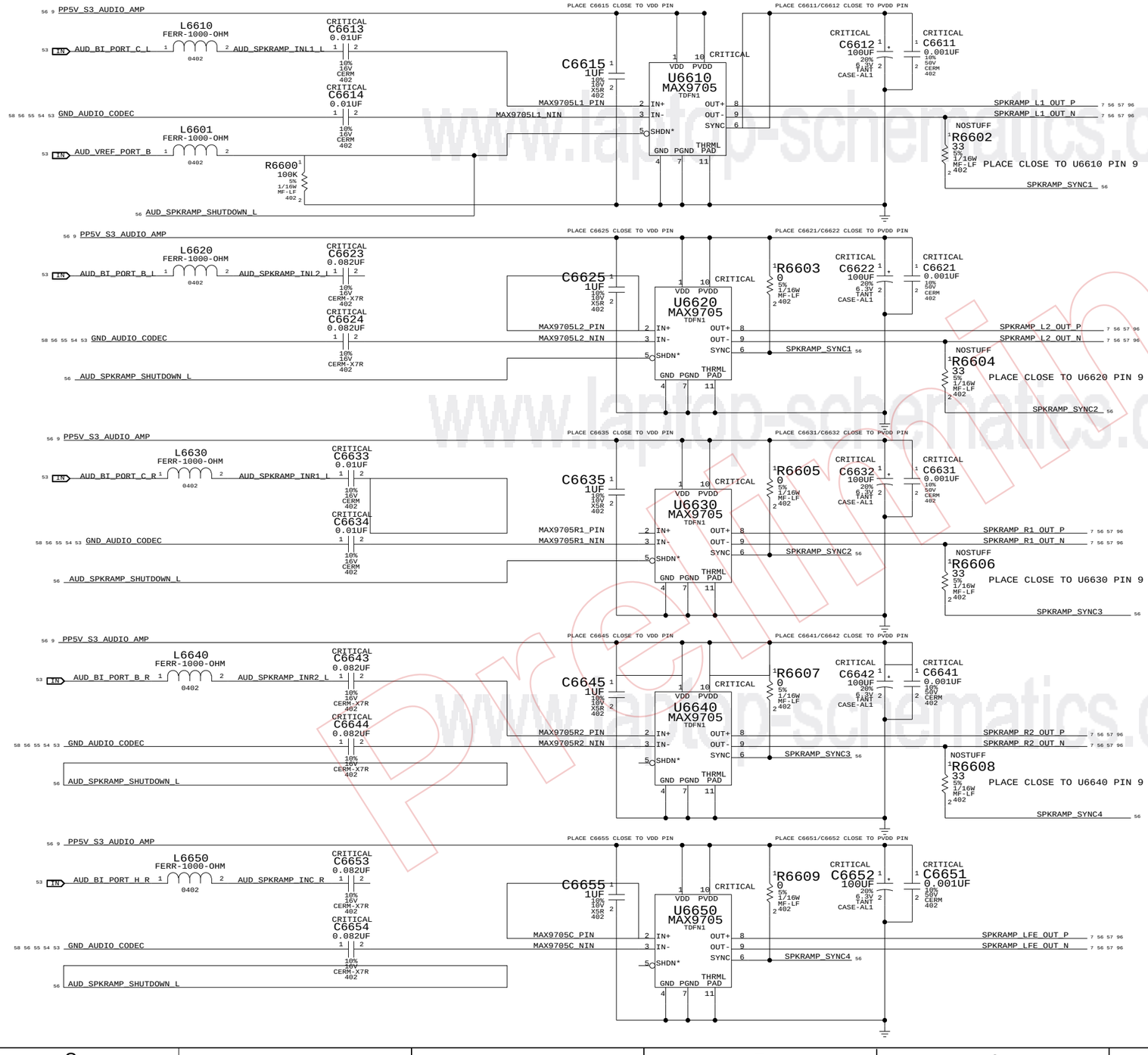
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	65	123

4X MONO SPEAKER AMPLIFIERS (MAX9705)

APN: 353S1595
GAIN = 12 DB

FC (SPEAKERS L1/R1) = ~796 HZ
FC (SPEAKERS L2/R2/LFE) = ~97 HZ

SPEAKER CHECKPOINTS



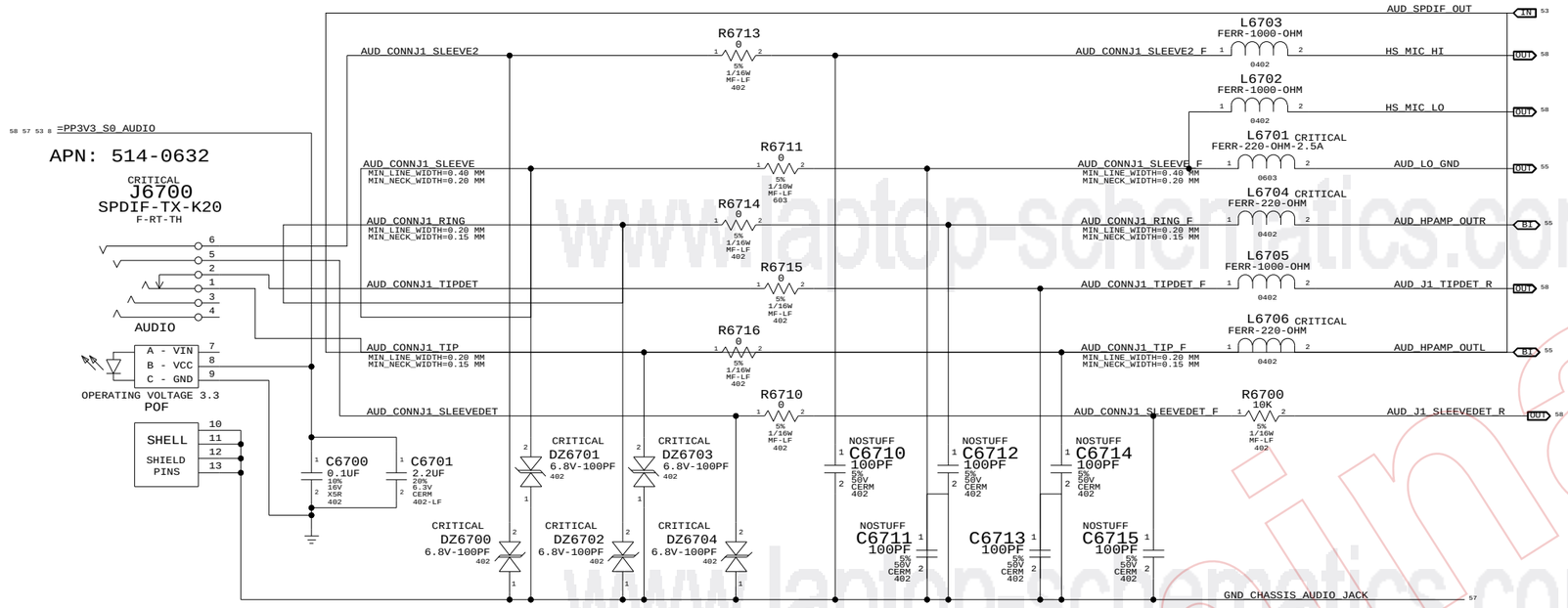
AUDIO:SPEAKER AMP

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

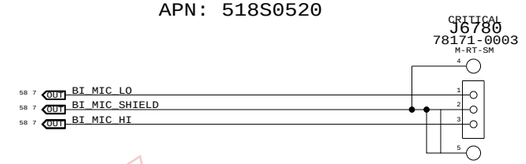
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 66 OF 123	

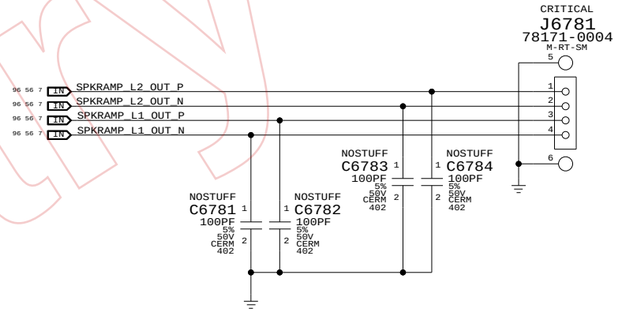
AUDIO JACK 1 LO/HP JACK, SPDIF TX



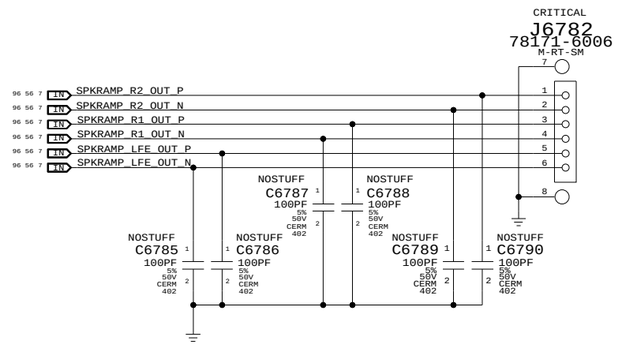
MIC CONNECTOR
APN: 518S0520



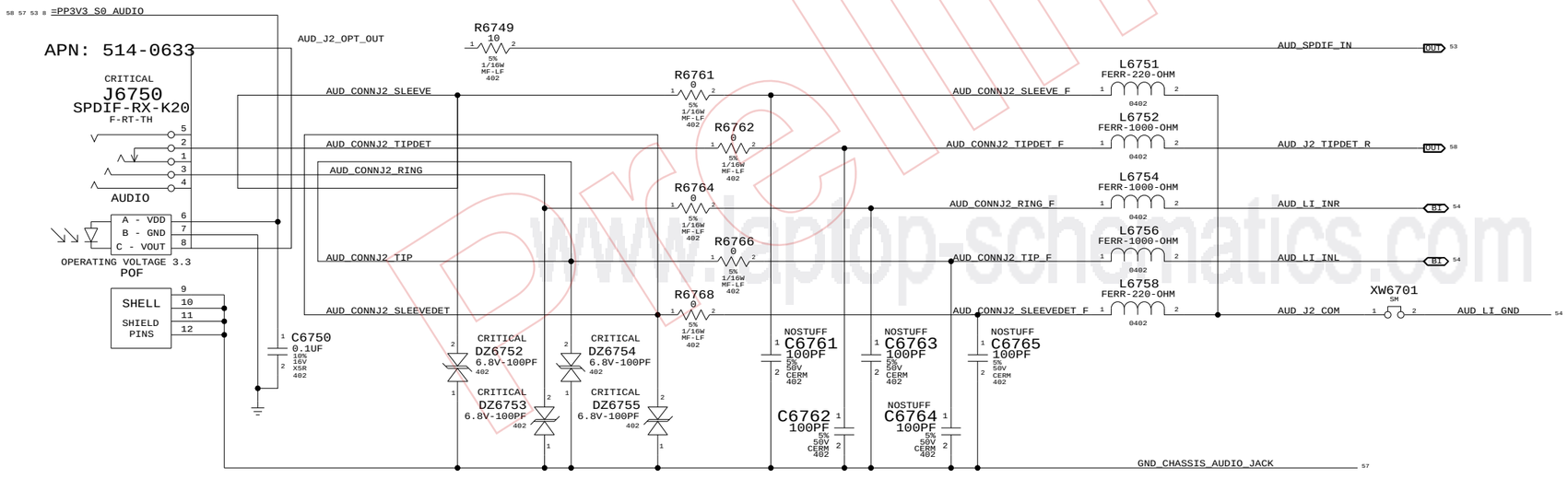
SPEAKER CONNECTORS
APN: 518S0521



APN: 518S0672



AUDIO JACK 2 LINE IN JACK, SPDIF RX



RETURN FOR HF NOISE

AUDIO: JACKS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	67	123

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SPEAKERS L1/R1	0X0F (15)	0X05 (5)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPEAKERS L2/R2	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SPEAKER LFE	0X0E (14)	0X04 (4)	0X0E (14)	0X17 (23,H)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)	N/A	0x1E (SPDIF OUT)	N/A	0X16 (22,G)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT D DETECT (Line-out)

PORT G DETECT (SPDIF DELEGATE)

PORT A DETECT (Line-in)

LINE_IN AMP SHUTDOWN CONTROL

PORT F (BUILT-IN MIC)

TIPDET DEBOUNCE CIRCUIT

PLACE L6800/C6800 CLOSE TO Q6800/01/02

AUDIO: JACK TRANSLATORS	
SYNC_MASTER=AUDIO_K20	SYNC_DATE=09/29/2008

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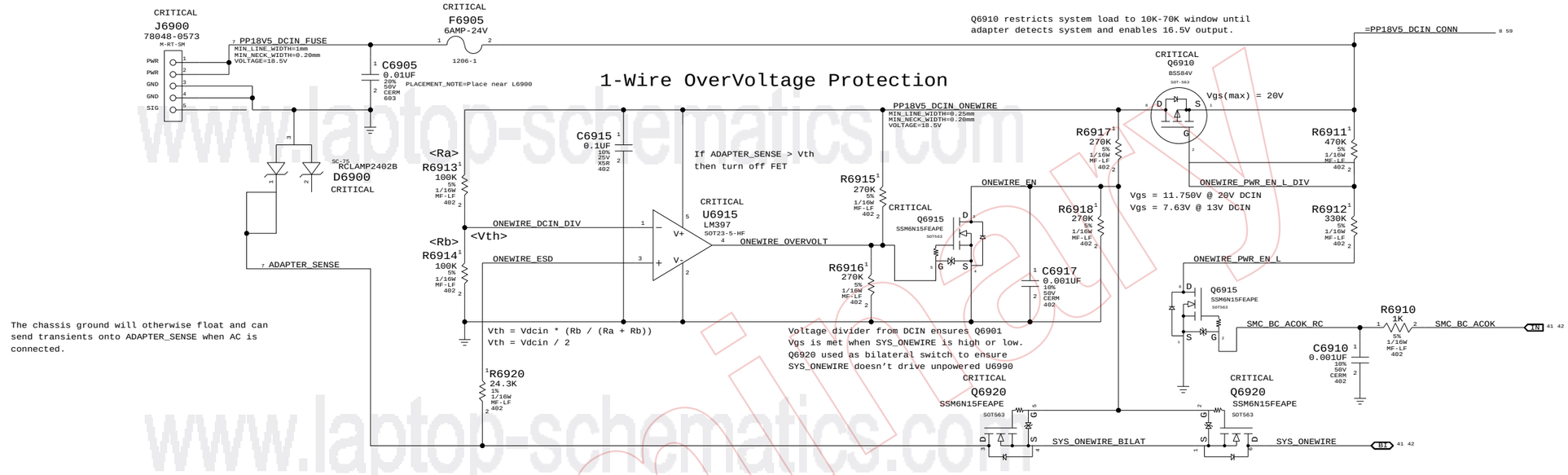
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 68 OF 123	

MagSafe DC Power Jack



DC-In & Battery Connectors

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 69 OF 123	

FROM ADAPTER

=PPDCIN_S5_CHGR

Inrush Limiter

R7060 470K 1% 1/16W MF-LF 402

C7060 0.1UF 10% 25V X5R 402

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7061 332K 1% 1/16W MF-LF 402

CRITICAL
Q7060
HAT1128R01
SO1

PPDCIN_S5_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

Reverse-Current Protection

PPDCIN_S5_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL
Q7065
HAT1128R01
SO1

R7065 100K 5% 1/16W MF-LF 402

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7066 62K 5% 1/16W MF-LF 402

CHGR_SGATE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.25 mm

U7070 TL331 SOT23-5
VCC
GND
SGATE_P0V1_VREF

C7070 0.1uF 10% 16V X5R 402

R7070 57.6K 1% 1/16W MF-LF 402

=PP3V42_G3H_CHGR

R7074 1M 5% 1/16W MF-LF 402

CHGR_AMON

R7075 clamps CHGR_AMON when charger is not powered to counter TL331 bias current.

R7071 1.82K 1% 1/16W MF-LF 402

Q7074 SSM6N15FEAPE SOT563

AMON_CLAMP

Q7074 SSM6N15FEAPE SOT563

PP5V1_CHGR_VDD

(CHGR_AGATE)

CRITICAL
D7005
BAT30CWFILM
SOT-323

(CHGR_DCIN)

=PP3V42_G3H_CHGR

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.07V

Input impedance of ~40K meets sparkitecture requirements

C7002 1UF 10% 10V X5R 402

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

30mA max load

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

R7010 30.1K 1% 1/16W MF-LF 402

R7011 9.31K 1% 1/16W MF-LF 402

R7015 56.2K 1% 1/16W MF-LF 402

CHGR_VCOMP_R

C7050 0.1uF 10% 16V X5R 402

SIGNAL_MODEL=EMPTY

C7015 0.001UF 10% 50V CERM 402

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 50V CERM 402

C7042 0.033UF 10% 16V X5R 402

C7000 1UF 10% 10V X5R 402

C7011 0.01UF 10% 16V CERM 402

C7005 0.1UF 10% 25V X5R 402

C7026 0.001UF 10% 50V CERM 402

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

CRITICAL
U7000
ISL6258A
QFN

VDD		VDDP
VHST	12	AGATE
SCL	11	CSIP
SDA	10	CSIN
VREF	4	BGATE
ACIN	3	DCIN
ICOMP	5	BOOT
VCOMP	7	UGATE
VNEG	8	PHASE
CSOP	18	LGATE
CSON	17	(OD) TRKL*
THRM_PAD	29	20V/V AMON
AGND	6	32V/V BMON
PGND	22	(OD) ACOK

=SMBUS_CHGR_SCL (IN)
=SMBUS_CHGR_SDA (BI)
VREF = 3.2V, < 300uA
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
NC
CHGR_AGATE
CHGR_CSI_P
CHGR_CSI_N
CHGR_BGATE
CHGR_DCIN
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
TP_CHGR_TRKL
CHGR_AMON
CHGR_BMON
=CHGR_ACOK

XW7000 SM

R7021 10 5% 1/16W MF-LF 402

R7022 10 5% 1/16W MF-LF 402

CHGR_CSI_R_P
CHGR_CSI_R_N

C7020 0.047UF 10% 10V CERM 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

C7035 0.22UF 10% 16V CERM 402

GND_CHGR_AGND

CRITICAL
R7020
0.02
0.5%
1W
MF
0612

PPDCIN_S5_FET_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL
Q7030
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
Q7031
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
Q7036
RJK0305DPB
LFPAK-HF

152S0542

CRITICAL
C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7036 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL
C7037 22UF 20% 25V POLY-TANT CASE-D2-SM

C7032 1UF 10% 25V X5R 603-1

C7033 1UF 10% 25V X5R 603-1

C7034 0.001UF 10% 50V X7R 402

CRITICAL
L7030
2.2UH-20A-5.5M-OHM

CRITICAL
L7031
2.2UH-20A-5.5M-OHM

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

PPVBAT_G3H_CHGR_REG_L
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

R7099 10 5% 1/10W MF-LF 603

NO STUFF

CHGR_PHASE_RC

C7099 0.001UF 10% 50V X7R 402

Max Current = 8.5A
(L7030 limit)
f = 400 kHz

R7051 10 5% 1/16W MF-LF 402

R7052 10 5% 1/16W MF-LF 402

CHGR_CSO_R_P
CHGR_CSO_R_N

(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)

CRITICAL
R7050
0.005
1%
1W
MF
0612

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7055 1UF 10% 25V X5R 603-1

C7057 0.01UF 10% 16V CERM 402

C7056 0.1UF 10% 16V X5R 402

TO SYSTEM

=PPBUS_G3H

CRITICAL
F7040
8AMP-24V
1206

CRITICAL
F7041
8AMP-24V
1206

CRITICAL
C7043 33UF 20% 16V POLY-TANT CASED2E-SM

CRITICAL
C7040 33UF 20% 16V POLY-TANT CASED2E-SM

C7041 0.001UF 10% 50V X7R 402

CRITICAL
HAT1127H
LFPAK-SM
Q7057

CRITICAL
HAT1127H
LFPAK-SM
Q7058

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

CRITICAL
HAT1127H
LFPAK-SM
Q7055

CRITICAL
HAT1127H
LFPAK-SM
Q7056

PPVBAT_G3H_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

C7058 1UF 10% 16V X5R 402-1

BATT_POS_GATE

R7056 1M 5% MF-LF 402 1/16W

R7057 20K 5% MF-LF 402 1/16W

GND_BATT_CHGND

M99 differences from last sync on 12/02/07 to T18 MLB:
1. L7030 changed from T18 MLB inductor to 152S0542.
2. Added Q7056, C7058,R7055,R7056..
3. U7000 Thermal Pad is now connected to GND, not through XW.
4. Q7060 and Q7065 changed to 376S0667.
5. Q7055 and Q7056 changed to 376S0666.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1938	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

PBus Supply & Battery Charger

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 70 OF 123	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

LAYOUT NOTE:
Place R7126 in hot
spot of reg circuit.

Place R7131 Between L7100,L7101 and CPU

IMVP6 CPU VCore Regulator

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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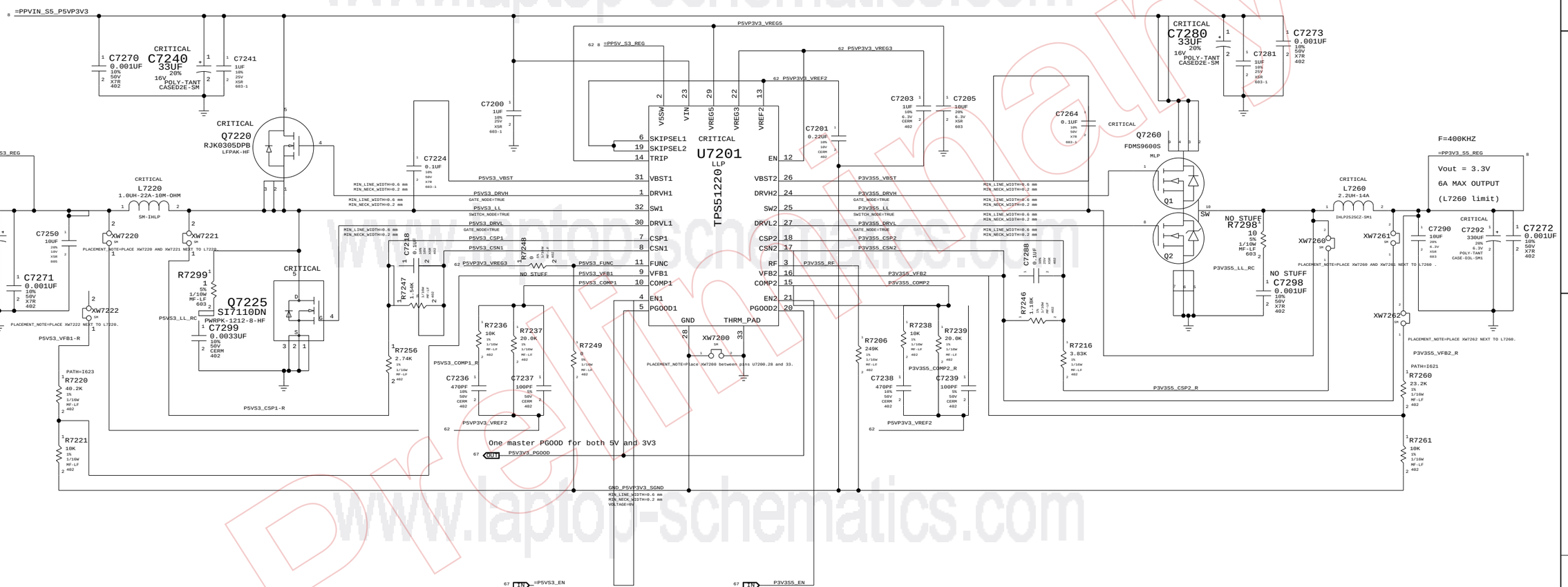
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	71	123



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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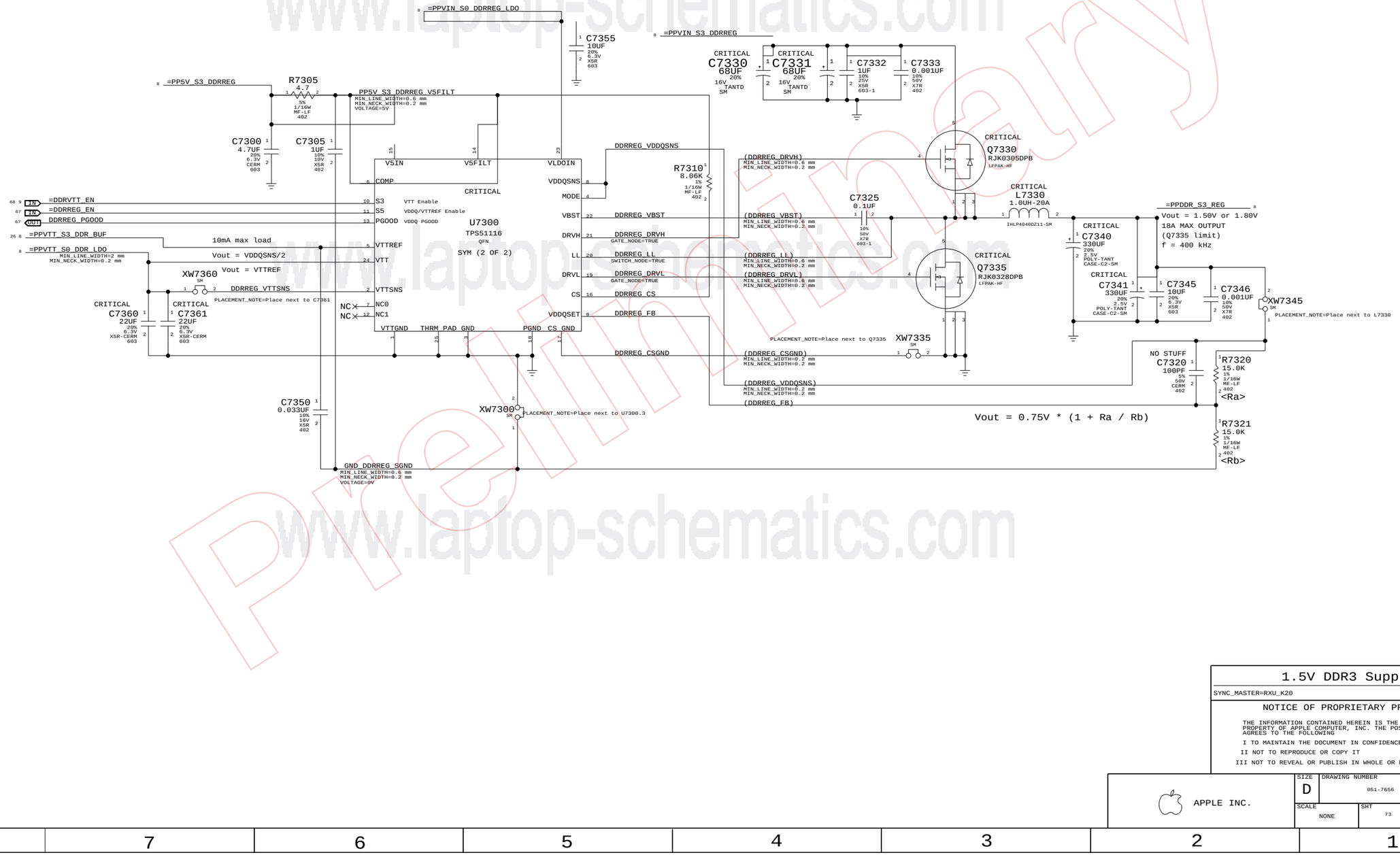
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 72 OF 123	

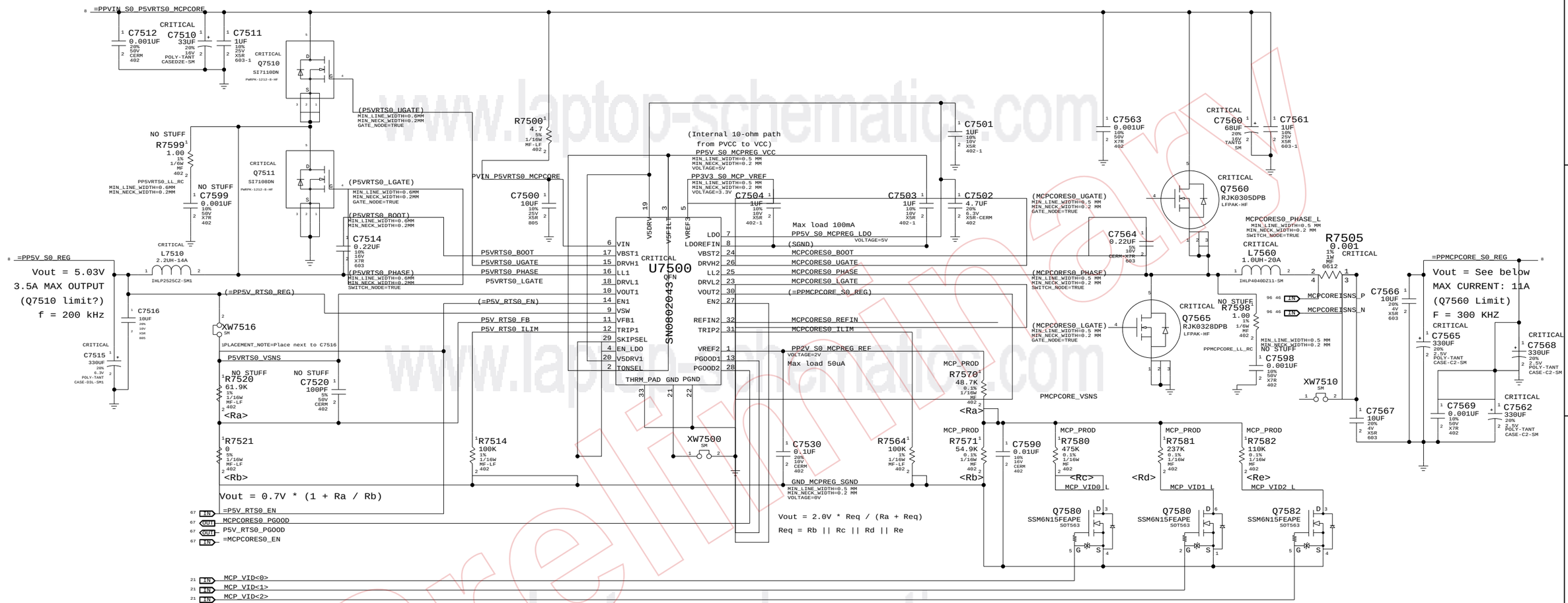


1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 73 OF 123	



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

VID<2:0>	Rev A01 Voltage	Production Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

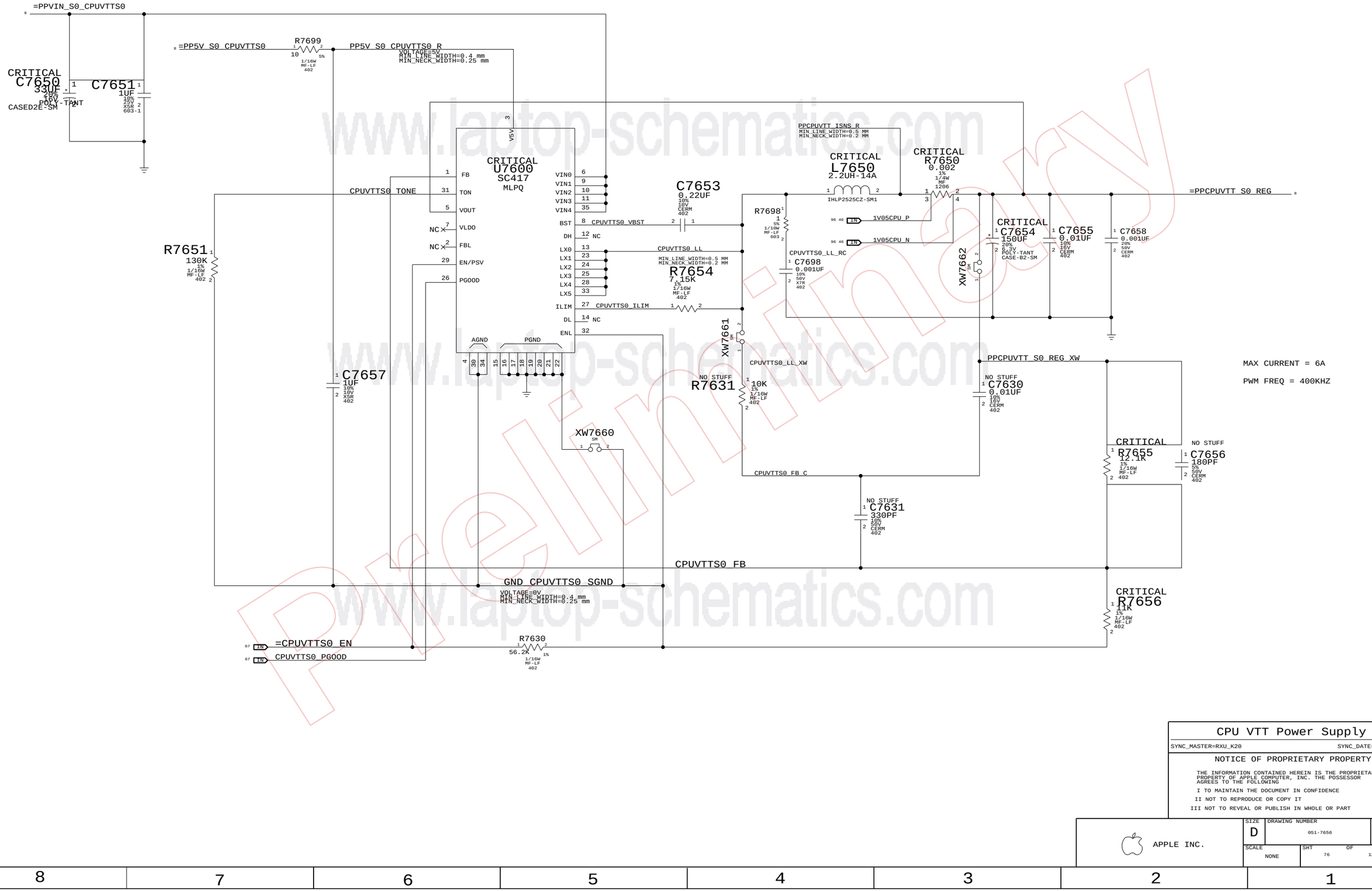
5V_S0 / MCP CORE REGULATOR

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE NONE SHT 75 OF 123

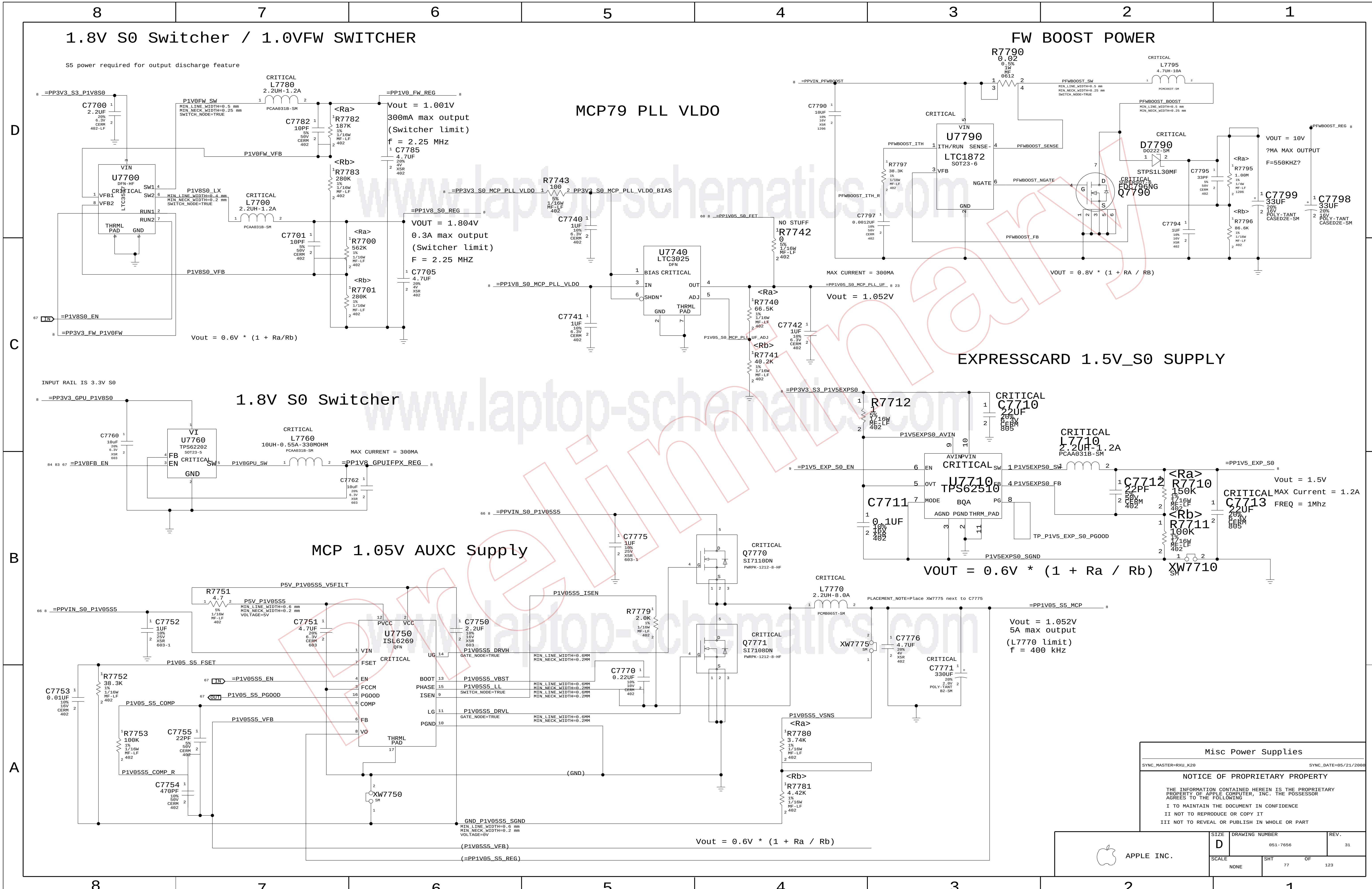


CPU VTT Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	76	123



1.8V S0 Switcher / 1.0VFW SWITCHER
S5 power required for output discharge feature
=PP3V3_S3_P1V8S0
C7700 2.2UF
U7700 LTC3547 CRITICAL
L7780 2.2UH-1.2A CRITICAL
=PP1V0_FW_REG
Vout = 1.001V
300mA max output
(Switcher limit)
f = 2.25 MHz
C7785 4.7UF
C7782 10PF
R7782 187K
R7783 280K
P1V0FW_SW
P1V0FW_VFB
P1V8S0_LX
L7700 2.2UH-1.2A CRITICAL
C7701 10PF
R7700 562K
R7701 280K
=PP1V8_S0_REG
VOUT = 1.804V
0.3A max output
(Switcher limit)
F = 2.25 MHZ
C7705 4.7UF
P1V8S0_VFB
=P1V8S0_EN
=PP3V3_FW_P1V0FW
Vout = 0.6V * (1 + Ra/Rb)
MCP79 PLL VLDO
R7743 100
=PP3V3_S0_MCP_PLL_VLDO
PP3V3_S0_MCP_PLL_VLDO_BIAS
C7740 1UF
=PP1V05_S0_FET
NO STUFF
R7742 0
U7740 LTC3025
=PP1V8_S0_MCP_PLL_VLDO
C7741 1UF
MAX CURRENT = 300MA
=PP1V05_S0_MCP_PLL_UF
Vout = 1.052V
R7740 66.5K
R7741 40.2K
C7742 1UF
P1V05_S0_MCP_PLL_UF_ADJ
INPUT RAIL IS 3.3V S0
1.8V S0 Switcher
=PP3V3_GPU_P1V8S0
C7760 10uF
U7760 TPS62202
L7760 10UH-0.55A-330MOHM CRITICAL
MAX CURRENT = 300MA
=PP1V8_GPUIFPX_REG
=P1V8FB_EN
P1V8GPU_SW
C7762 10uF
MCP 1.05V AUXC Supply
=PPVIN_S0_P1V05S5
C7775 1UF
Q7770 SI7110DN CRITICAL
Q7771 SI7108DN CRITICAL
R7751 4.7
P5V_P1V05S5_V5FILT
P5V_P1V05S5
=PPVIN_S0_P1V05S5
C7752 1UF
C7751 4.7UF
U7750 ISL6269 CRITICAL
C7750 2.2UF
P1V05S5_ISEN
R7779 2.0K
P1V05S5_DRVH
P1V05_S5_FSET
R7752 38.3K
C7753 0.01UF
=P1V05S5_EN
P1V05_S5_PGOOD
P1V05_S5_COMP
P1V05S5_VBST
P1V05S5_LL
C7770 0.22UF
P1V05S5_DRVL
P1V05S5_VFB
R7753 100K
C7755 22PF
P1V05S5_COMP_R
C7754 470PF
XW7750
(GND)
GND_P1V05S5_SGND
(P1V05S5_VFB)
(=PP1V05_S5_REG)
Vout = 0.6V * (1 + Ra / Rb)
L7770 2.2UH-8.0A CRITICAL
PLACEMENT_NOTE=Place XW7775 next to C7775
=PP1V05_S5_MCP
Vout = 1.052V
5A max output
(L7770 limit)
f = 400 kHz
XW7775
C7776 4.7UF
C7771 330UF CRITICAL
P1V05S5_VSNS
R7780 3.74K
R7781 4.42K
FW BOOST POWER
R7790 0.02
=PPVIN_PFWBOOST
L7795 4.7UH-10A CRITICAL
PFWBOOST_SW
PFWBOOST_BOOST
=PFWBOOST_REG
C7790 10UF
U7790 LTC1872 CRITICAL
PFWBOOST_ITH
PFWBOOST_SENSE
R7797 38.3K
PFWBOOST_NGATE
D7790 STPS1L30MF CRITICAL
Q7790 FDC796NG CRITICAL
C7795 33PF
R7795 1.00M
R7796 86.6K
C7799 33UF
C7798 33UF
VOUT = 10V
?MA MAX OUTPUT
F=550KHZ?
C7797 0.0012UF
C7794 1UF
PFWBOOST_FB
VOUT = 0.8V * (1 + RA / RB)
EXPRESSCARD 1.5V_S0 SUPPLY
=PP3V3_S3_P1V5EXPS0
R7712 1
C7710 22UF CRITICAL
P1V5EXPS0_AVIN
L7710 2.2UH-1.2A CRITICAL
=P1V5_EXP_S0_EN
U7710 TPS62510 CRITICAL
P1V5EXPS0_SW
P1V5EXPS0_FB
C7711 0.1UF
C7712 22PF
R7710 150K
R7711 100K
C7713 22UF CRITICAL
=PP1V5_EXP_S0
Vout = 1.5V
MAX Current = 1.2A
FREQ = 1Mhz
TP_P1V5_EXP_S0_PGOOD
P1V5EXPS0_SGND
XW7710
VOUT = 0.6V * (1 + Ra / Rb)
Misc Power Supplies
SYNC_MASTER=RXU_K20
SYNC_DATE=05/21/2008
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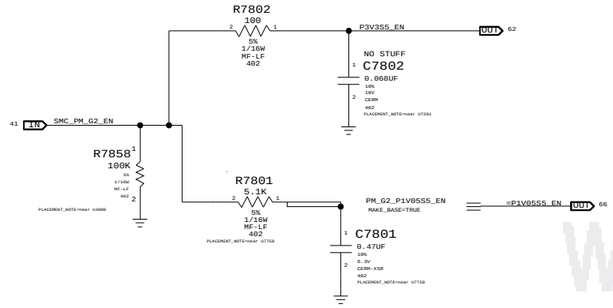
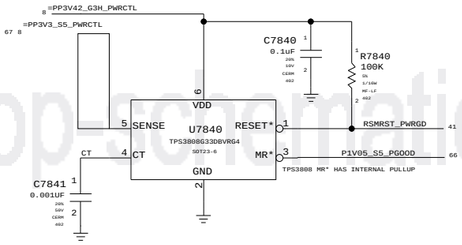
APPLE INC.
SIZE D
DRAWING NUMBER 051-7656
REV. 31
SCALE NONE
SHT 77 OF 123

3.3V 1,05V S5 ENABLE

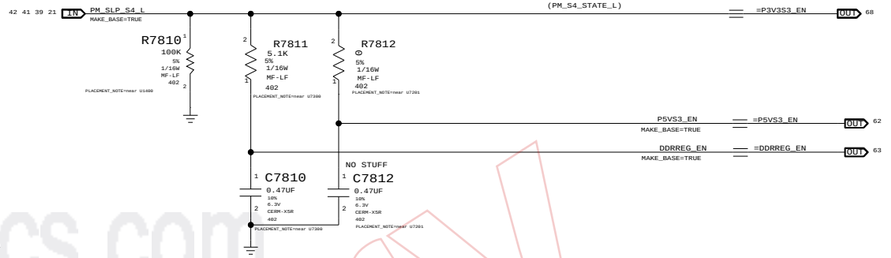


State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

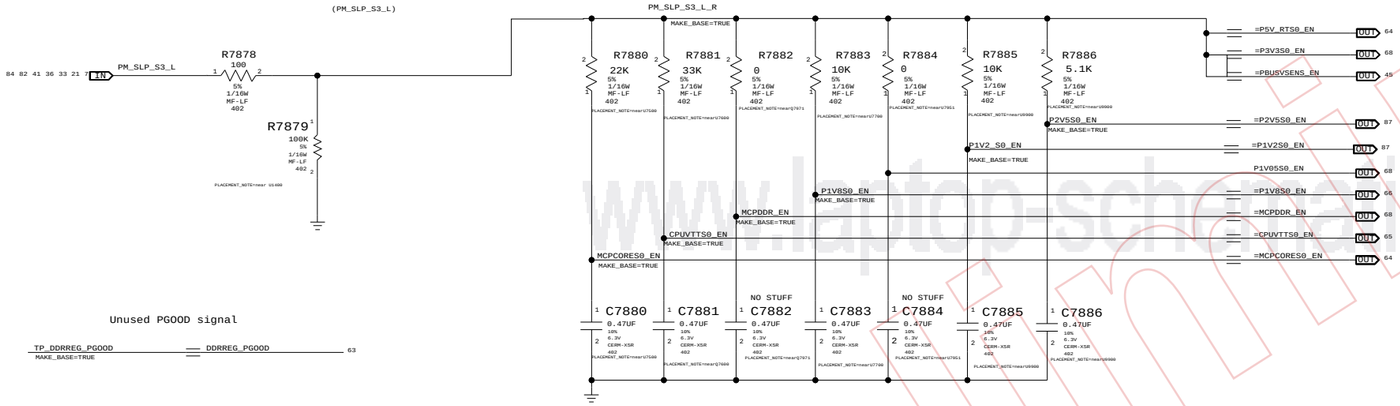
S5 rail PWRGD



3.3V,5V S3 ENABLE

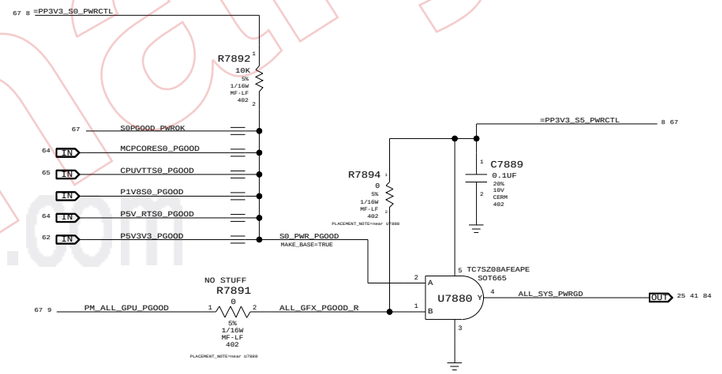


S0 ENABLE



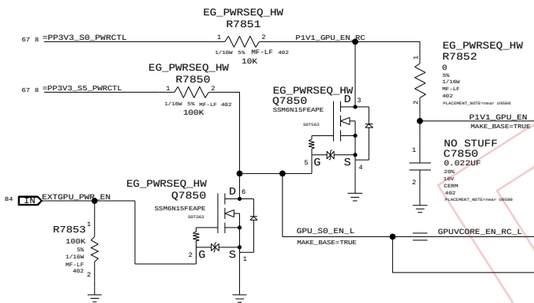
Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

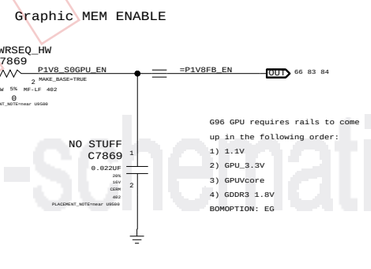


Unused PGOOD signal

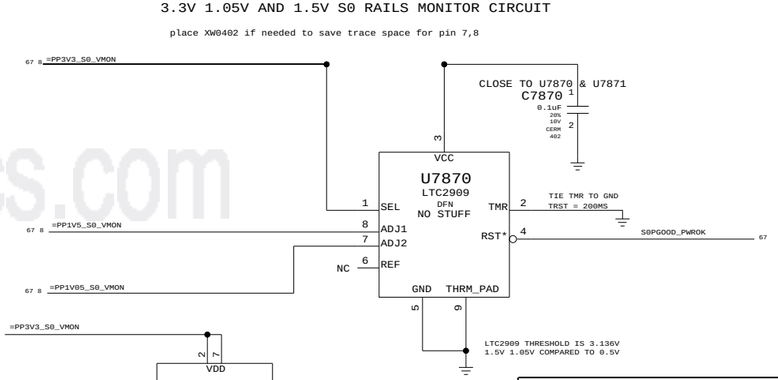
1.1V GPU ENABLE



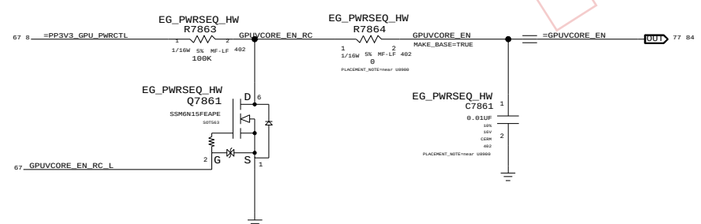
Graphic MEM ENABLE



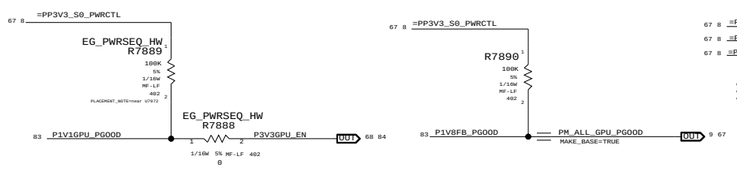
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



GPUVCORE ENABLE



EXT GPU PWRGD Pullup



Power Control		
SYNC_MASTER=YMA_K20		SYNC_DATE=09/09/2008

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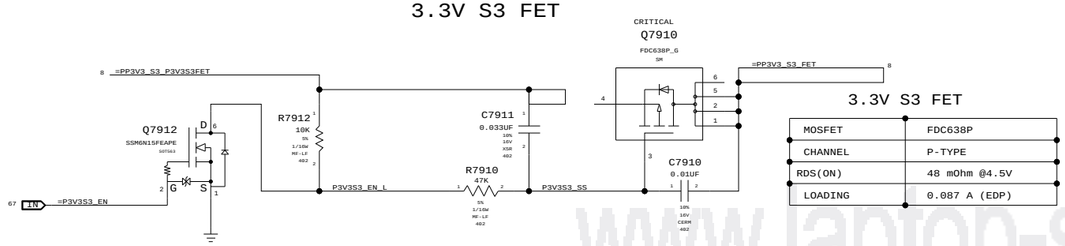
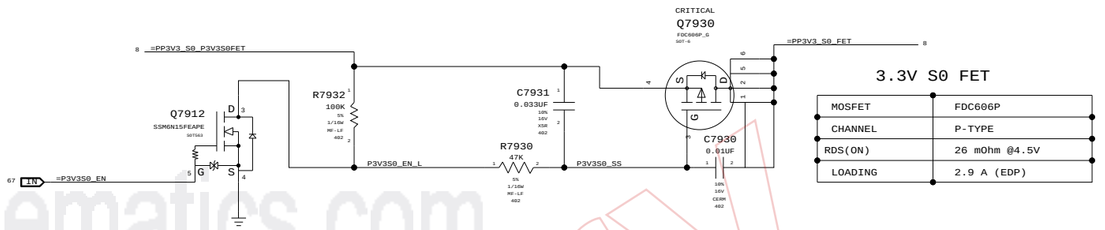
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
	SCALE	SHT	OF
	NONE	78	123

3.3V S3 FET



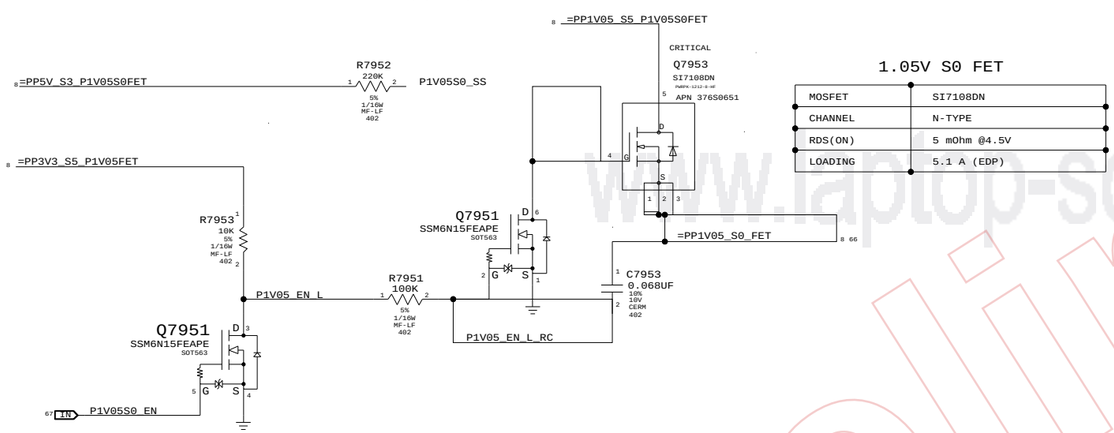
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

3.3V S0 FET



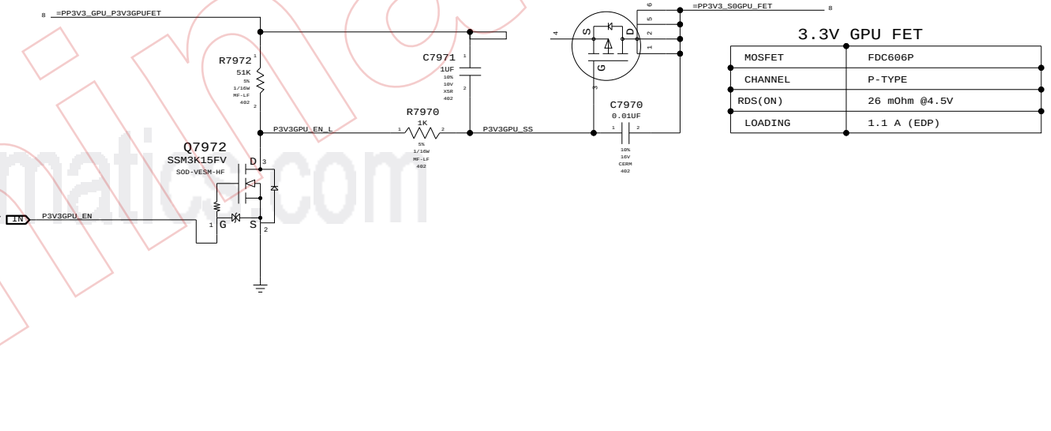
3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

1.05V S0 FET



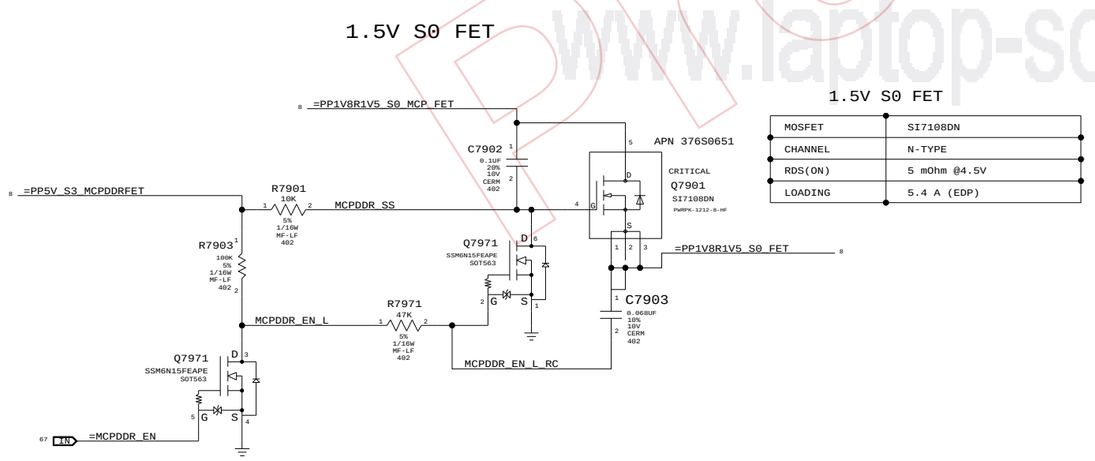
1.05V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.1 A (EDP)

3.3V GPU FET



3.3V GPU FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)

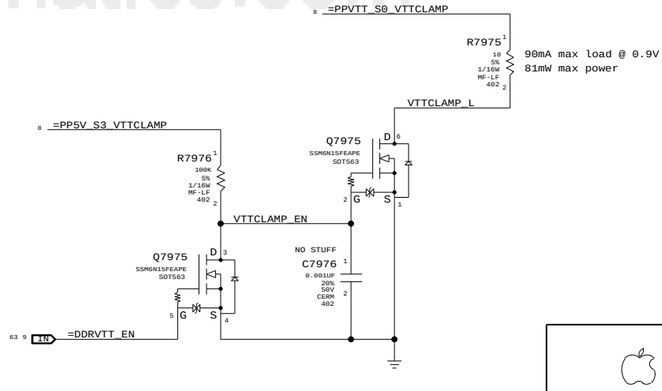
1.5V S0 FET



1.5V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)

MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.



Power FETs

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

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D	051-7656	31
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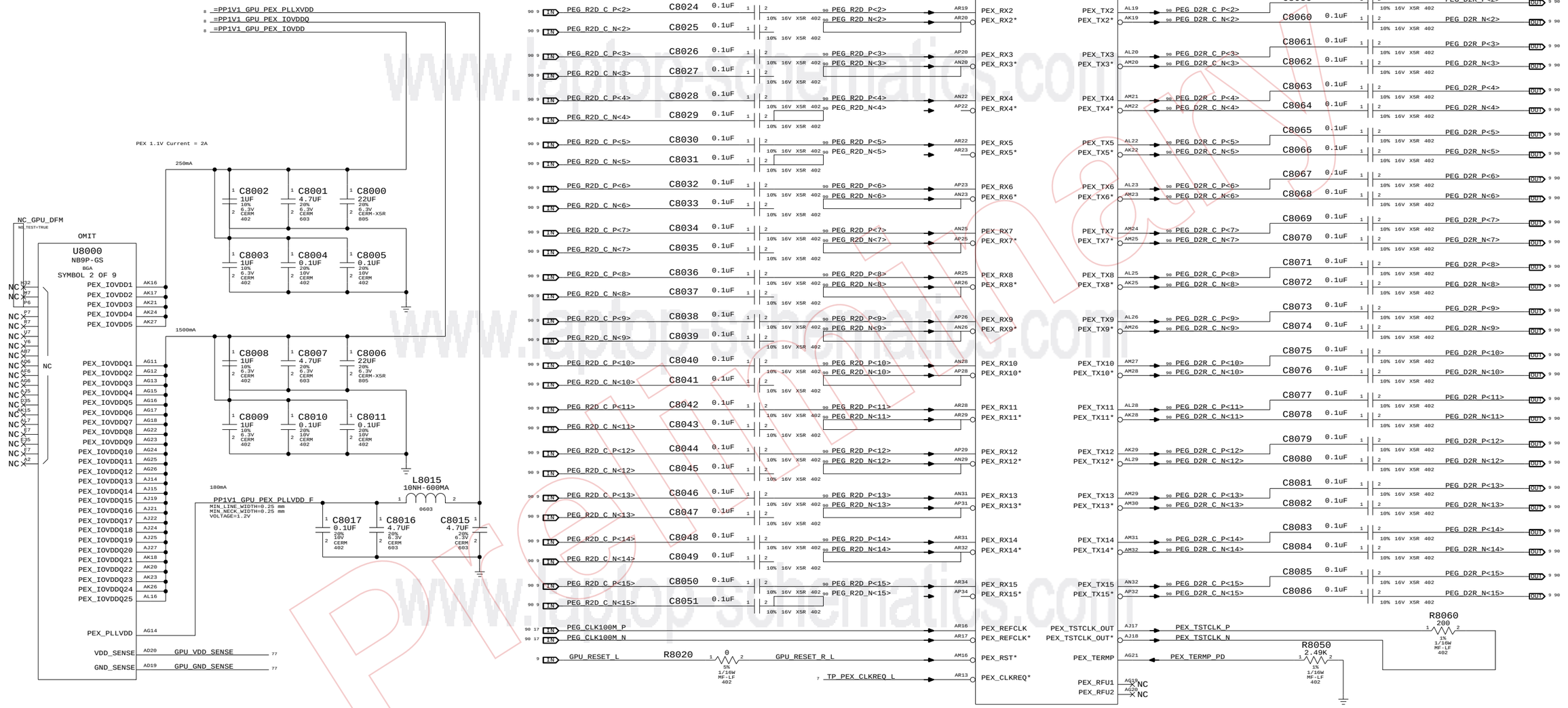
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



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PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17	PEX_RX0	PEX_TX0	AL17	PEG_D2R_C_P<0>
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PEG_CLK100M_P			AR16	PEX_REFCLK	PEX_TSTCLK_OUT	AJ17	PEX_TSTCLK_P
PEG_CLK100M_N			AR17	PEX_REFCLK*	PEX_TSTCLK_OUT*	AJ18	PEX_TSTCLK_N
GPU_RESET_L	R8020 0 5% 1/10W MF-LF 402	GPU_RESET_R_L	AM16	PEX_RST*	PEX_TERMP	AG21	PEX_TERMP_PD
		TP_PEX_CLKREQ_L	AR13	PEX_CLKREQ*	PEX_RFU1	AG19	NC
					PEX_RFU2	AG20	NC

R8060 200 1% 1/10W MF-LF 402

R8050 2.49K 1% 1/10W MF-LF 402

NV G96 PCI-E

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 80 OF 123	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

B =PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402
C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402
C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

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L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17 — VDD

V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20 — VDD

B =PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

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B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16 — FBVDDQ

J20 J21 J22 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31 — FBVDDQ

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B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16 — GND

V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30 — GND

NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	81	123

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63

FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30

FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*

FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7

FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7

FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7

FB_DLLAVDD0 FB_PLLAVDD0

FBA_DEBUG

FB_CAL_PD_VDDQ FB_CAL_PU_GND FB_CAL_TERM_GND

NC FBA_RFU0 NC FBA_RFU1* NC FBA_RFU2 NC FBA_RFU3* NC FBA_RFU4 NC FBA_RFU5* NC FBA_RFU6 NC FBA_RFU7*

R8200 10K 5% 1/16W MF-LF 402
R8201 10K 5% 1/16W MF-LF 402

71 8 =PP1V1_GPU_FBPLLAVDD
PP1V1_GPU_FBPLLAVDD_E MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.1V
CRITICAL
L8200 FERR-220-OHM 0402
C8202 0.1UF 20% 10V CERM 402
C8201 0.1UF 20% 10V CERM 402
C8200 1UF 10% 6.3V CERM 402

71 8 =PP1V8_GPU_FBIO
R8293 60.4 1% 1/16W MF-LF 402
R8290 48.7 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to U8000.

R8292 40.2 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to U8000.
R8291 33.2 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to U8000.

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FBC_D0 FBC_D1 FBC_D2 FBC_D3 FBC_D4 FBC_D5 FBC_D6 FBC_D7 FBC_D8 FBC_D9 FBC_D10 FBC_D11 FBC_D12 FBC_D13 FBC_D14 FBC_D15 FBC_D16 FBC_D17 FBC_D18 FBC_D19 FBC_D20 FBC_D21 FBC_D22 FBC_D23 FBC_D24 FBC_D25 FBC_D26 FBC_D27 FBC_D28 FBC_D29 FBC_D30 FBC_D31 FBC_D32 FBC_D33 FBC_D34 FBC_D35 FBC_D36 FBC_D37 FBC_D38 FBC_D39 FBC_D40 FBC_D41 FBC_D42 FBC_D43 FBC_D44 FBC_D45 FBC_D46 FBC_D47 FBC_D48 FBC_D49 FBC_D50 FBC_D51 FBC_D52 FBC_D53 FBC_D54 FBC_D55 FBC_D56 FBC_D57 FBC_D58 FBC_D59 FBC_D60 FBC_D61 FBC_D62 FBC_D63

FBC_CMD0 FBC_CMD1 FBC_CMD2 FBC_CMD3 FBC_CMD4 FBC_CMD5 FBC_CMD6 FBC_CMD7 FBC_CMD8 FBC_CMD9 FBC_CMD10 FBC_CMD11 FBC_CMD12 FBC_CMD13 FBC_CMD14 FBC_CMD15 FBC_CMD16 FBC_CMD17 FBC_CMD18 FBC_CMD19 FBC_CMD20 FBC_CMD21 FBC_CMD22 FBC_CMD23 FBC_CMD24 FBC_CMD25 FBC_CMD26 FBC_CMD27 FBC_CMD28 FBC_CMD29 FBC_CMD30

FBC_CLK0 FBC_CLK0* FBC_CLK1 FBC_CLK1*

FBC_DQM0 FBC_DQM1 FBC_DQM2 FBC_DQM3 FBC_DQM4 FBC_DQM5 FBC_DQM6 FBC_DQM7

FBC_DQS_RN0 FBC_DQS_RN1 FBC_DQS_RN2 FBC_DQS_RN3 FBC_DQS_RN4 FBC_DQS_RN5 FBC_DQS_RN6 FBC_DQS_RN7

FBC_DQS_WP0 FBC_DQS_WP1 FBC_DQS_WP2 FBC_DQS_WP3 FBC_DQS_WP4 FBC_DQS_WP5 FBC_DQS_WP6 FBC_DQS_WP7

FB_DLLAVDD1 FB_PLLAVDD1

FBC_DEBUG

FB_VREF

NC FBC_RFU0 NC FBC_RFU1* NC FBC_RFU2 NC FBC_RFU3* NC FBC_RFU4 NC FBC_RFU5* NC FBC_RFU6 NC FBC_RFU7*

R8250 10K 5% 1/16W MF-LF 402
R8251 10K 5% 1/16W MF-LF 402

71 8 =PP1V1_GPU_FBPLLAVDD
C8290 0.1UF 20% 10V CERM 402
C8291 0.1UF 20% 10V CERM 402

71 8 =PP1V8_GPU_FBIO
R8294 60.4 1% 1/16W MF-LF 402
R8295 1.07K 1% 1/16W MF-LF 402
R8296 2.49K 1% 1/16W MF-LF 402
GPU_FB_VREF
NO STUFF C8296 0.1uF 10% 16V X5R 402
NO STUFF R8297 1.02K 1% 1/16W MF-LF 402
GPU_FB_VREF_UNTERM_L MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

NO STUFF Q8295 SSM6N15FEAPE SOT563
75 73 72 FB_VREF_UNTERM

NV G96 FRAME BUFFER I/F

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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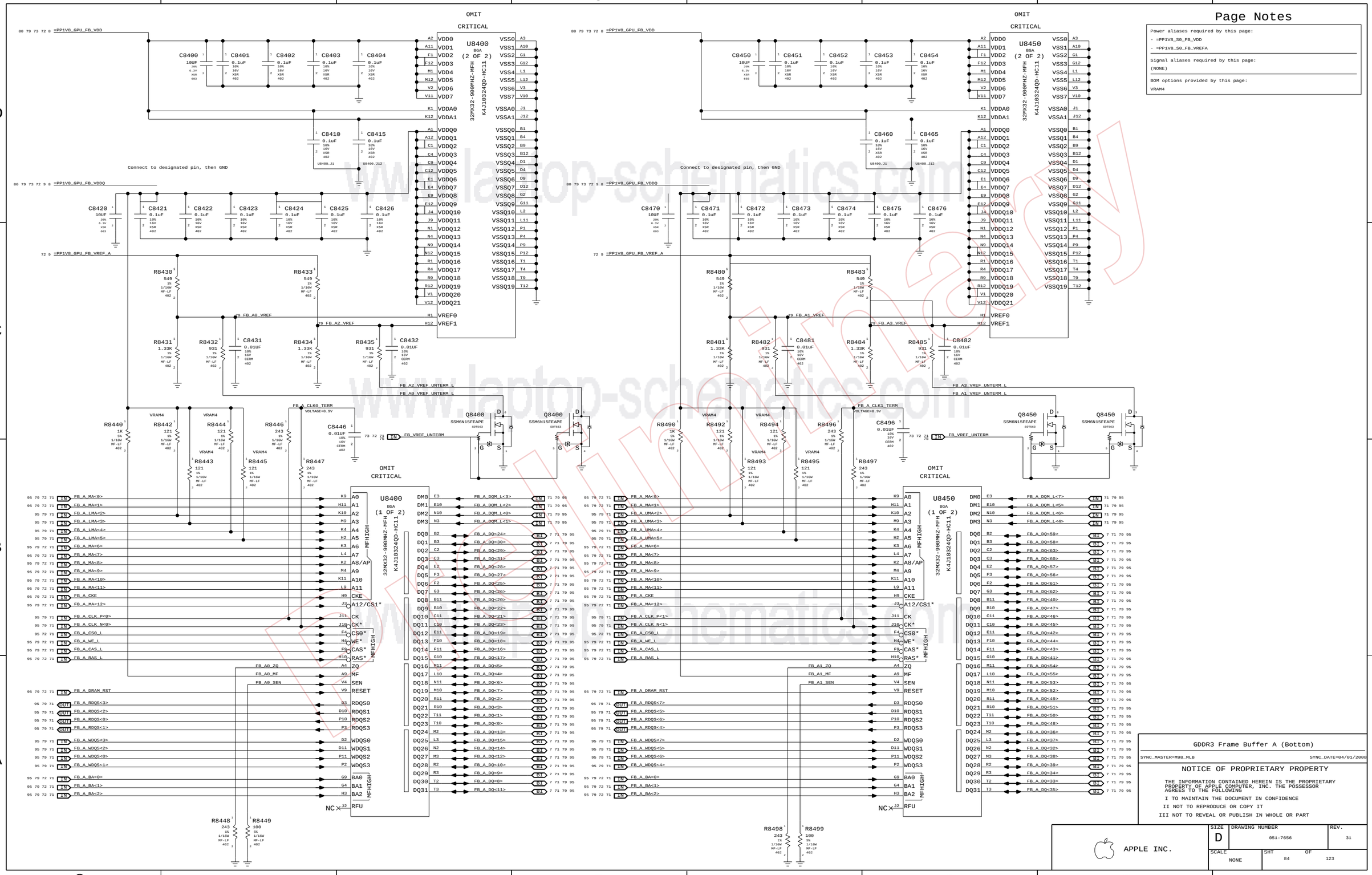
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	82	123



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

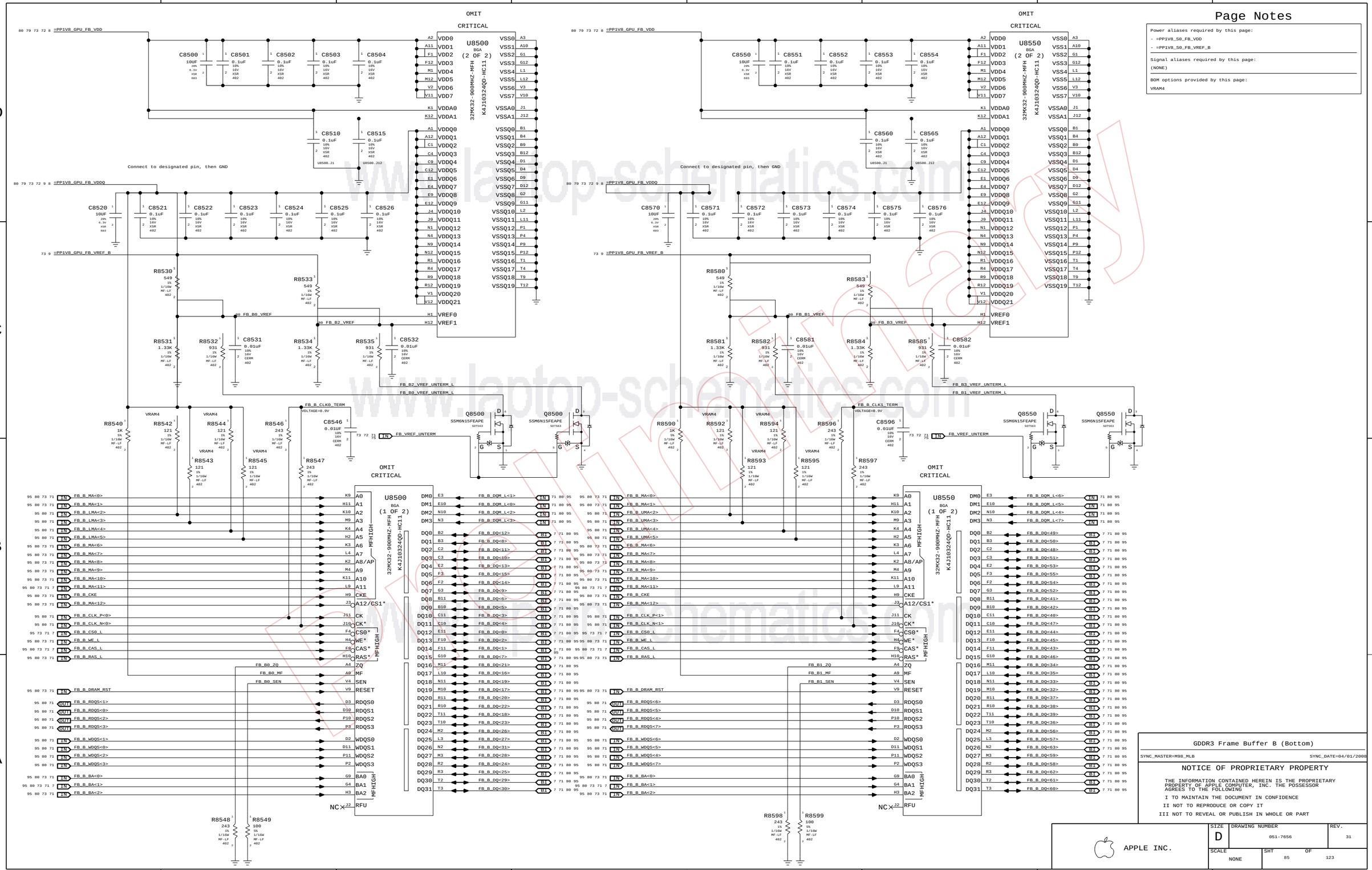
BOM options provided by this page:
VRAM4

GDDR3 Frame Buffer A (Bottom)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 84 OF 123	



Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
75 74 8 6 =PP3V3_GPU_VDD33

OMIT

U8000
NB9P-GS
BGA
SYMBOL 6 OF 9

J9	VDD33_1		K1	GPIO0	GPU_GPIO_0
J10	VDD33_2		K2	GPIO1	GPU_GPIO_1
J11	VDD33_3		K3	GPIO2	GPU_GPIO_2
J12	VDD33_4		H3	GPIO3	GPU_GPIO_3
J13	VDD33_5		H2	GPIO4	GPU_GPIO_4
			H1	GPIO5	GPU_GPIO_5
			H4	GPIO6	GPU_GPIO_6
			H5	GPIO7	GPU_GPIO_7
			H6	GPIO8	GPU_GPIO_8
			J7	GPIO9	GPU_GPIO_9
			K4	GPIO10	GPU_GPIO_10
			K5	GPIO11	GPU_GPIO_11
			H7	GPIO12	GPU_GPIO_12
			J4	GPIO13	GPU_GPIO_13
			J6	GPIO14	GPU_GPIO_14
			L1	GPIO15	GPU_GPIO_15
			L2	GPIO16	GPU_GPIO_16
			L4	GPIO17	GPU_GPIO_17
			M4	GPIO18	GPU_GPIO_18
			L7	GPIO19	GPU_GPIO_19
			L5	GPIO20	GPU_GPIO_20
			K6	GPIO21	GPU_GPIO_21
			L6	GPIO22	GPU_GPIO_22
			M6	GPIO23	GPU_GPIO_23
J25	RFU0	NC			
J26	RFU1	NC			
AK14	RFU0_GND				
K9	RFU1_GND				
C3	ROM_CS*	75 GPU_ROM_CS_L			
D4	ROM_SCLK	75 GPU_ROM_SCLK			
D3	ROM_SI	75 GPU_ROM_SI			
C4	ROM_SO	75 GPU_ROM_SO			
N9	STRAP_REF_3V3	GPU_STRAP_REF_3V3_PD	C7	HDA_SDI	GPU_HDA_SDI
M9	STRAP_REF_MIOB (IPD)	GPU_STRAP_REF_MIOB_PD	B7	HDA_SDO	GPU_HDA_SDO
			A7	HDA_SYNC	GPU_HDA_SYNC
			D7	HDA_BCLK	GPU_HDA_BCLK
			D6	HDA_RST*	GPU_HDA_RST_L
P9	MIOA_VDDQ_1		A5	SPDIF	GPU_SPDIF
R9	MIOA_VDDQ_2		A4	BUFRST*	TP_GPU_BUFRST_L
T9	MIOA_VDDQ_3		AP14	JTAG_TCK	GPU_JTAG_TCK
U9	MIOA_VDDQ_4		AN14	JTAG_TDI	GPU_JTAG_TDI
AA9	MIOB_VDDQ_1		AN16	JTAG_TDO	GPU_JTAG_TDO
AB9	MIOB_VDDQ_2		AR14	JTAG_TMS	GPU_JTAG_TMS
W9	MIOB_VDDQ_3		AP16	JTAG_TRST*	GPU_JTAG_TRST_L
Y9	MIOB_VDDQ_4		N4	MIOA_CLKIN	GPU_MIOA_CLKIN
AP35	TESTMODE	GPU_TESTMODE_PD	R4	MIOA_CLKOUT	GPU_MIOA_CLKOUT_P
N5	MIOA_VREF	GPU_MIOA_VREF	T4	MIOA_CLKOUT*	GPU_MIOA_CLKOUT_N
AF1	MIOB_VREF	GPU_MIOB_VREF	P5	MIOA_CTL3	GPU_MIOA_CTL3
U5	MIOA_CAL_PD_VDDQ	74 GPU_MIOA_PD_VDDQ	N2	MIOA_DE	GPU_MIOA_DE
T5	MIOA_CAL_PU_GND	74 GPU_MIOA_PU_GND	N1	MIOA_D0	GPU_MIOA_D<0>
AA7	MIOB_CAL_PD_VDDQ	74 GPU_MIOB_PD_VDDQ	P4	MIOA_D1	GPU_MIOA_D<1>
AA6	MIOB_CAL_PU_GND	74 GPU_MIOB_PU_GND	P1	MIOA_D2	GPU_MIOA_D<2>
AF9	SP_PLLVDD		P2	MIOA_D3	GPU_MIOA_D<3>
AE9	PLLVDD		P3	MIOA_D4	GPU_MIOA_D<4>
AD9	VID_PLLVDD		T3	MIOA_D5	GPU_MIOA_D<5>
B1	XTAL_IN	75 IN GPU_XTALIN	T2	MIOA_D6	GPU_MIOA_D<6>
B2	XTAL_OUT	75 OUT GPU_XTALOUT	T1	MIOA_D7	GPU_MIOA_D<7>
D1	XTAL_OUTBUFF	75 OUT GPU_XTALOUTBUFF	U4	MIOA_D8	GPU_MIOA_D<8>
D2	XTAL_SSIN	75 IN GPU_XTALSSIN	U1	MIOA_D9	GPU_MIOA_D<9>
			U2	MIOA_D10	GPU_MIOA_D<10>
			U3	MIOA_D11	GPU_MIOA_D<11>
			R6	MIOA_D12	GPU_MIOA_D<12>
			T6	MIOA_D13	GPU_MIOA_D<13>
			N6	MIOA_D14	GPU_MIOA_D<14>
			N3	MIOA_HSYNC	GPU_MIOA_HSYNC
			L3	MIOA_VSYNC	GPU_MIOA_VSYNC
			AE1	MIOB_CLKIN	GPU_MIOB_CLKIN
			V4	MIOB_CLKOUT	GPU_MIOB_CLKOUT_P
			W4	MIOB_CLKOUT*	GPU_MIOB_CLKOUT_N
			W3	MIOB_CTL3	GPU_MIOB_CTL3
			Y5	MIOB_DE	GPU_MIOB_DE
			Y1	MIOB_D0	GPU_MIOB_D<0>
			Y2	MIOB_D1	GPU_MIOB_D<1>
			Y3	MIOB_D2	GPU_MIOB_D<2>
			AB3	MIOB_D3	GPU_MIOB_D<3>
			AB2	MIOB_D4	GPU_MIOB_D<4>
			AB1	MIOB_D5	GPU_MIOB_D<5>
			AC4	MIOB_D6	GPU_MIOB_D<6>
			AC1	MIOB_D7	GPU_MIOB_D<7>
			AC2	MIOB_D8	GPU_MIOB_D<8>
			AC3	MIOB_D9	GPU_MIOB_D<9>
			AE3	MIOB_D10	GPU_MIOB_D<10>
			AE2	MIOB_D11	GPU_MIOB_D<11>
			U6	MIOB_D12	GPU_MIOB_D<12>
			W6	MIOB_D13	GPU_MIOB_D<13>
			Y6	MIOB_D14	GPU_MIOB_D<14>
			W5	MIOB_D15	GPU_STRAP<0>
			W7	MIOB_D16	GPU_STRAP<1>
			V7	MIOB_D17	GPU_STRAP<2>
			W1	MIOB_HSYNC	GPU_MIOB_HSYNC
			W2	MIOB_VSYNC	GPU_MIOB_VSYNC
			B5	THERMDP	GPU_THERMD_P
			B4	THERMDN	GPU_THERMD_N
			C5	PGOOD_OUT*	TP_GPU_PGOOD_OUT_L

75 74 8 6 =PP3V3_GPU_VDD33

Typically <??mA

C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

75 74 8 =PP3V3_GPU_MIO

75 74 8 =PP3V3_GPU_MIO

R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ 74
GPU_MIOB_PD_VDDQ 74
GPU_MIOA_PU_GND 74
GPU_MIOB_PU_GND 74
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1uF 10% 16V XSR 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1uF 10% 16V XSR 402
R8660 10K 5% 1/16W MF-LF 402

CRITICAL
L8630 FERR-220-OHM 0402
8 =PP1V1_GPU_PLLVDD
PP1V1_GPU_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V XSR 402

CRITICAL
L8635 FERR-220-OHM 0402
8 =PP1V1_GPU_H_PLLVDD
PP1V1_GPU_H_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V XSR 402

CRITICAL
L8640 FERR-220-OHM 0402
8 =PP1V1_GPU_VID_PLLVDD
PP1V1_GPU_VID_PLLVDD_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V XSR 402

NV G96 GPIO/MIO/MISC

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	86	123

GPIOs

		Native Func			
74	GPU_GPIO_0	GP	NC_GPU_GPIO_0	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_1	HPDC	DP_EG_HPD	MAKE_BASE=TRUE	IN 81
74	GPU_GPIO_2	LCD0_BL_PWM	TP_LVDS_EG_BKL_PWM	MAKE_BASE=TRUE	7
74	GPU_GPIO_3	LCD0_VDD	EG_LCD_PWR_EN	MAKE_BASE=TRUE	75 84
74	GPU_GPIO_4	LCD0_BL_EN	EG_BKLT_EN	MAKE_BASE=TRUE	75 84
74	GPU_GPIO_5	VID0	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE	7
74	GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE	7
74	GPU_GPIO_7	VID2/MEM_VID	GPIO7_FBVDD_ALTVO	MAKE_BASE=TRUE	75 83
74	GPU_GPIO_8	THERM	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE	75
74	GPU_GPIO_9	FAN_PWM	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE	75
74	GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	MAKE_BASE=TRUE	71 72 73 75
74	GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID0	MAKE_BASE=TRUE	OUT 77
74	GPU_GPIO_12	AC_DET	GPU_VCORE_VID1	MAKE_BASE=TRUE	OUT 77
74	GPU_GPIO_13	PWR_CTL0	GPU_VCORE_VID2	MAKE_BASE=TRUE	OUT 77
74	GPU_GPIO_14	PWR_CTL1	TP_GPU_VCORE_VID3	MAKE_BASE=TRUE	7

GPIOs

		Native Func			
74	GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET		75
74	GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE NO_TEST=TRUE	
74	GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE NO_TEST=TRUE	

Renamed signals

75 74	GPU_XTALOUT	GPU_XTALOUT	74 75
95 75	GPU_CLK27M	GPU_XTALIN	74
95	GPU_CLK27M_SS	GPU_XTALSSIN	74 75
96 47	GPU_TDIODE_P	GPU_THERMD_P	74
96 47	GPU_TDIODE_N	GPU_THERMD_N	74
81	LVDS_EG_DDC_CLK	GPU_I2CA_SCL	76
81	LVDS_EG_DDC_DATA	GPU_I2CA_SDA	76
81 75	DP_EG_DDC_CLK	GPU_I2CB_SCL	76
81 75	DP_EG_DDC_DATA	GPU_I2CB_SDA	76

Unused signals

	NC_GPU_SPDIF	GPU_SPDIF	74
	NC_CPU_HDA_SDI	GPU_HDA_SDI	74
	NC_CPU_HDA_SDO	GPU_HDA_SDO	74
	NC_CPU_HDA_SYNC	GPU_HDA_SYNC	74
	NC_CPU_HDA_BCLK	GPU_HDA_BCLK	74
	NC_CPU_HDA_RST_L	GPU_HDA_RST_L	74
	NC_FBA_MA<13>	FB_A_MA<13>	71
	NC_FBB_MA<13>	FB_B_MA<13>	71
	NC_FBA_CMD28	TP_FBA_CMD28	71
	NC_FBC_CMD28	TP_FBC_CMD28	71
	NC_FBA_CMD29	TP_FBA_CMD29	71
	NC_FBC_CMD29	TP_FBC_CMD29	71
	NC_FBA_CMD30	TP_FBA_CMD30	71
	NC_FBC_CMD30	TP_FBC_CMD30	71
	NC_GPU_ROM_CS_L	GPU_ROM_CS_L	74

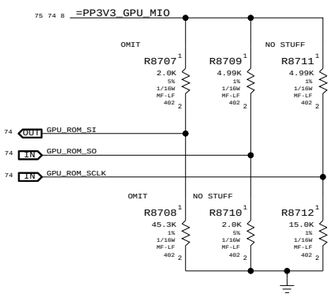
Unused I2C Buses

	NC_GPU_I2CC_SCL	GPU_I2CC_SCL	76
	NC_GPU_I2CC_SDA	GPU_I2CC_SDA	76
	NC_GPU_I2CD_SCL	GPU_I2CD_SCL	76
	NC_GPU_I2CD_SDA	GPU_I2CD_SDA	76
	NC_GPU_I2CE_SCL	GPU_I2CE_SCL	76
	NC_GPU_I2CE_SDA	GPU_I2CE_SDA	76
	NC_GPU_I2CH_SCL	GPU_I2CH_SCL	76
	NC_GPU_I2CH_SDA	GPU_I2CH_SDA	76

I2C5 ties into SMBus connection page
(I2C5 requires pullups even if not used)

7	TP_LVDS_EG_B_CLK_P	LVDS_EG_B_CLK_P	76
7	TP_LVDS_EG_B_CLK_N	LVDS_EG_B_CLK_N	76
	NC_LVDS_EG_A_DATA_P<3>	LVDS_EG_A_DATA_P<3>	76
	NC_LVDS_EG_A_DATA_N<3>	LVDS_EG_A_DATA_N<3>	76
	NC_LVDS_EG_B_DATA_P<3>	LVDS_EG_B_DATA_P<3>	76
	NC_LVDS_EG_B_DATA_N<3>	LVDS_EG_B_DATA_N<3>	76

Config Straps

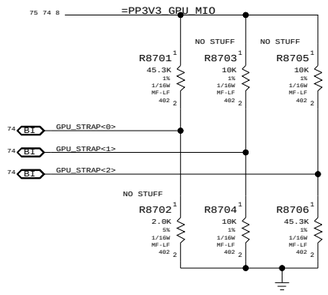


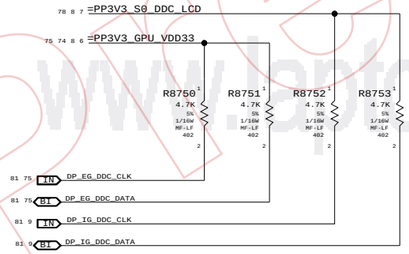
Physical Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

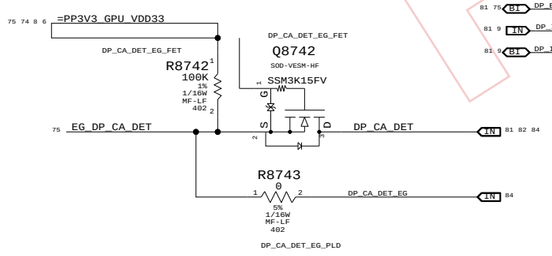
Strap S1/S2 Bit[3:0] PU/PD Rval
0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k
3 0011 PD 20k
4 0100 PD 25k
5 0101 PD 30k
6 0110 PD 35k
7 0111 PD 45k

Strap S1/S2 Bit[3:0] PU/PD Rval
8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k

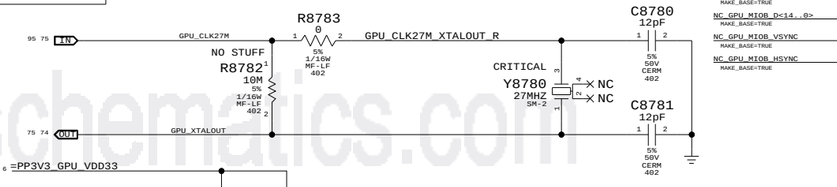
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL F1LM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0361	1	RES,MTL F1LM,1/16W,30.1K,1,0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES,MTL F1LM,1/16W,29.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL F1LM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES,MTL F1LM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES,MTL F1LM,1/16W,30.1K,1,0402,SMD,LF	R8707		VRAM_1024_QIMONDA



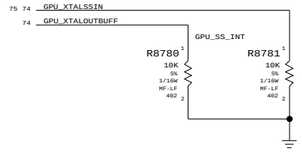




GPU 27MHz Crystal



Unused Clocks



G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

	NC_GPU_MIOA_CLKOUT_P	GPU_MIOA_CLKOUT_P	74
	NC_GPU_MIOA_CLKOUT_N	GPU_MIOA_CLKOUT_N	74
	NC_GPU_MIOA_CTL3	GPU_MIOA_CTL3	74
7	TP_GPU_MIOA_DE	GPU_MIOA_DE	74
7	TP_GPU_MIOA_D<9..0>	GPU_MIOA_D<9..0>	74
	NC_GPU_MIOA_CLKIN	GPU_MIOA_CLKIN	74
	NC_GPU_MIOA_D<14..10>	GPU_MIOA_D<14..10>	74
	NC_GPU_MIOA_HSYNC	GPU_MIOA_HSYNC	74
	NC_GPU_MIOA_VSYNC	GPU_MIOA_VSYNC	74
	NC_GPU_MIOB_CLKIN	GPU_MIOB_CLKIN	74
	NC_GPU_MIOB_CLKOUT_P	GPU_MIOB_CLKOUT_P	74
	NC_GPU_MIOB_CLKOUT_N	GPU_MIOB_CLKOUT_N	74
	NC_GPU_MIOB_CTL3	GPU_MIOB_CTL3	74
	NC_GPU_MIOB_DE	GPU_MIOB_DE	74
	NC_GPU_MIOB_D<14..0>	GPU_MIOB_D<14..0>	74
	NC_GPU_MIOB_VSYNC	GPU_MIOB_VSYNC	74
	NC_GPU_MIOB_HSYNC	GPU_MIOB_HSYNC	74

G96 GPIOs & Straps

SYNC_MASTER=M98_MLB SYNC_DATE=05/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 87 OF 123	

Isolation FETs for DP MUX inputs

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

8 =PP1V8_GPU_IFPX

CRITICAL
L8800
FERR-220-OHM
0402

?mA peak per diff pair
?mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402

Place at AG9
Place at AG10

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

CRITICAL
L8805
FERR-220-OHM
0402

80mA peak

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPEF_RSET 76
GPU_IFPCD_RSET 76
GPU_IFPAB_RSET 76

R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

CRITICAL
L8810
FERR-220-OHM
0402

8 =PP1V1_GPU_IFPCD_IOVDD

?mA peak per diff pair
?mA peak for all pairs

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402

Place at AJ8
Place at AK8

PP1V1_GPU_IFPCD_IOVDD_F 76
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.1V

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

CRITICAL
L8815
FERR-220-OHM
0402

160mA peak

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

PP1V8_GPU_IFPCD_PLLVDD_F 76
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFEEF_IOVDD_F 76
PP1V8_GPU_IFPEF_PLLVDD_F 76

Power inputs must be pulled down if not used

R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD	IFPA_TXC	AM11
AG10	IFPB_IOVDD	IFPA_TXC*	AM12
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8
AE7	IFPE_IOVDD	IFPA_TXD1	AM10
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10
AJ9	IFPCD_PLLVDD	IFPA_TXD3	AK11
AK7	IFPCD_RSET	IFPA_TXD3*	AL11
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13
AL1	IFPEF_RSET	IFPB_TXC*	AN13
		IFPB_TXD4	AN8
		IFPB_TXD4*	AP8
		IFPB_TXD5	AP10
		IFPB_TXD5*	AN10
		IFPB_TXD6	AR11
		IFPB_TXD6*	AR10
		IFPB_TXD7	AN11
		IFPB_TXD7*	AP11
		IFPC_AUX	AP2
		IFPC_AUX*	AN3
		IFPC_L0	AM7
		IFPC_L0*	AM6
		IFPC_L1	AL5
		IFPC_L1*	AM5
		IFPC_L2	AM3
		IFPC_L2*	AM4
		IFPC_L3	AP1
		IFPC_L3*	AR2
		IFPD_AUX	AP4
		IFPD_AUX*	AN4
		IFPD_L0	AR8
		IFPD_L0*	AR7
		IFPD_L1	AK7
		IFPD_L1*	AK8
		IFPD_L2	AN6
		IFPD_L2*	AP6
		IFPD_L3	AR5
		IFPD_L3*	AR4
		IFPE_AUX	AE4
		IFPE_AUX*	AD4
		IFPE_L0	AH6
		IFPE_L0*	AH5
		IFPE_L1	AH4
		IFPE_L1*	AG4
		IFPE_L2	AF4
		IFPE_L2*	AF5
		IFPE_L3	AE6
		IFPE_L3*	AE5
		IFPF_AUX	AF3
		IFPF_AUX*	AF2
		IFPF_L0	AL2
		IFPF_L0*	AL1
		IFPF_L1	AJ3
		IFPF_L1*	AJ2
		IFPF_L2	AJ1
		IFPF_L2*	AH2
		IFPF_L3	AH3
		IFPF_L3*	AH1
AJ12	DACA_VDD	DACA_RED	AM15
AK12	DACA_VREF	DACA_GREEN	AM14
AK13	DACA_RSET	DACA_BLUE	AL13
AC6	DACB_VDD	DACA_HSYNC	AM13
AC5	DACB_VREF	DACA_VSYNC	AL12
AD6	DACB_RSET	DACB_RED	AA4
AG7	DACC_VDD	DACB_GREEN	AB2
AK6	DACC_VREF	DACB_BLUE	Y4
AK7	DACC_RSET	DACB_CSYNC	AB5
		DACC_RED	AK4
		DACC_GREEN	AL4
		DACC_BLUE	AJ4
		DACC_HSYNC	AM1
		DACC_VSYNC	AK2

75 B1	GPU_I2CA_SCL	G1	I2CA_SCL
75 B1	GPU_I2CA_SDA	G4	I2CA_SDA
75 B1	GPU_I2CC_SCL	E3	I2CC_SCL
75 B1	GPU_I2CC_SDA	E4	I2CC_SDA
44 B1	=GPU_I2CS_SCL	E2	I2CS_SCL
44 B1	=GPU_I2CS_SDA	E1	I2CS_SDA
75 B1	GPU_I2CH_SCL	F6	I2CH_SCL
75 B1	GPU_I2CH_SDA	G6	I2CH_SDA
75 B1	GPU_I2CB_SCL	G3	I2CB_SCL
75 B1	GPU_I2CB_SDA	G2	I2CB_SDA
75 B1	GPU_I2CD_SCL	F4	I2CD_SCL
75 B1	GPU_I2CD_SDA	G5	I2CD_SDA
75 B1	GPU_I2CE_SCL	D5	I2CE_SCL
75 B1	GPU_I2CE_SDA	E5	I2CE_SDA

76	PP1V1_GPU_IFPCD_IOVDD_F	AJ8	IFPC_IOVDD
76	PP1V1_GPU_IFPEF_IOVDD_F	AD7	IFPF_IOVDD
76	PP1V8_GPU_IFPCD_PLLVDD_F	AK9	IFPAB_PLLVDD
76	GPU_IFPAB_RSET	AJ11	IFPAB_RSET
76	PP1V8_GPU_IFPCD_PLLVDD_F	AJ9	IFPCD_PLLVDD
76	GPU_IFPCD_RSET	AK7	IFPCD_RSET
76	PP1V8_GPU_IFPEF_PLLVDD_F	AJ6	IFPEF_PLLVDD
76	GPU_IFPEF_RSET	AL1	IFPEF_RSET

IFPA_TXC	AM11	LVDS_EG_A_CLK_P	OUT 84 95
IFPA_TXC*	AM12	LVDS_EG_A_CLK_N	OUT 84 95
IFPA_TXD0	AM8	LVDS_EG_A_DATA_P<0>	OUT 84 95
IFPA_TXD0*	AL8	LVDS_EG_A_DATA_N<0>	OUT 84 95
IFPA_TXD1	AM10	LVDS_EG_A_DATA_P<1>	OUT 84 95
IFPA_TXD1*	AM9	LVDS_EG_A_DATA_N<1>	OUT 84 95
IFPA_TXD2	AK10	LVDS_EG_A_DATA_P<2>	OUT 84 95
IFPA_TXD2*	AL10	LVDS_EG_A_DATA_N<2>	OUT 7 84 95
IFPA_TXD3	AK11	LVDS_EG_A_DATA_P<3>	OUT 75
IFPA_TXD3*	AL11	LVDS_EG_A_DATA_N<3>	OUT 75
IFPB_TXC	AP13	LVDS_EG_B_CLK_P	OUT 75
IFPB_TXC*	AN13	LVDS_EG_B_CLK_N	OUT 75
IFPB_TXD4	AN8	LVDS_EG_B_DATA_P<0>	OUT 84 95
IFPB_TXD4*	AP8	LVDS_EG_B_DATA_N<0>	OUT 84 95
IFPB_TXD5	AP10	LVDS_EG_B_DATA_P<1>	OUT 84 95
IFPB_TXD5*	AN10	LVDS_EG_B_DATA_N<1>	OUT 84 95
IFPB_TXD6	AR11	LVDS_EG_B_DATA_P<2>	OUT 84 95
IFPB_TXD6*	AR10	LVDS_EG_B_DATA_N<2>	OUT 84 95
IFPB_TXD7	AN11	LVDS_EG_B_DATA_P<3>	OUT 75
IFPB_TXD7*	AP11	LVDS_EG_B_DATA_N<3>	OUT 75
IFPC_AUX	AP2	DP_EG_AUX_CH_P	OUT 81 95
IFPC_AUX*	AN3	DP_EG_AUX_CH_N	OUT 81 95
IFPC_L0	AM7	DP_EG_ML_P<0>	OUT 81 95
IFPC_L0*	AM6	DP_EG_ML_N<0>	OUT 81 95
IFPC_L1	AL5	DP_EG_ML_P<1>	OUT 81 95
IFPC_L1*	AM5	DP_EG_ML_N<1>	OUT 81 95
IFPC_L2	AM3	DP_EG_ML_P<2>	OUT 81 95
IFPC_L2*	AM4	DP_EG_ML_N<2>	OUT 81 95
IFPC_L3	AP1	DP_EG_ML_P<3>	OUT 81 95
IFPC_L3*	AR2	DP_EG_ML_N<3>	OUT 81 95

R8861 1K 5% 1/16W MF-LF 402 — NO STUFF
R8860 1K 5% 1/16W MF-LF 402

GPU_DACA_VDD
GPU_DACB_VDD
GPU_DACC_VDD

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

NV G96 Video Interfaces

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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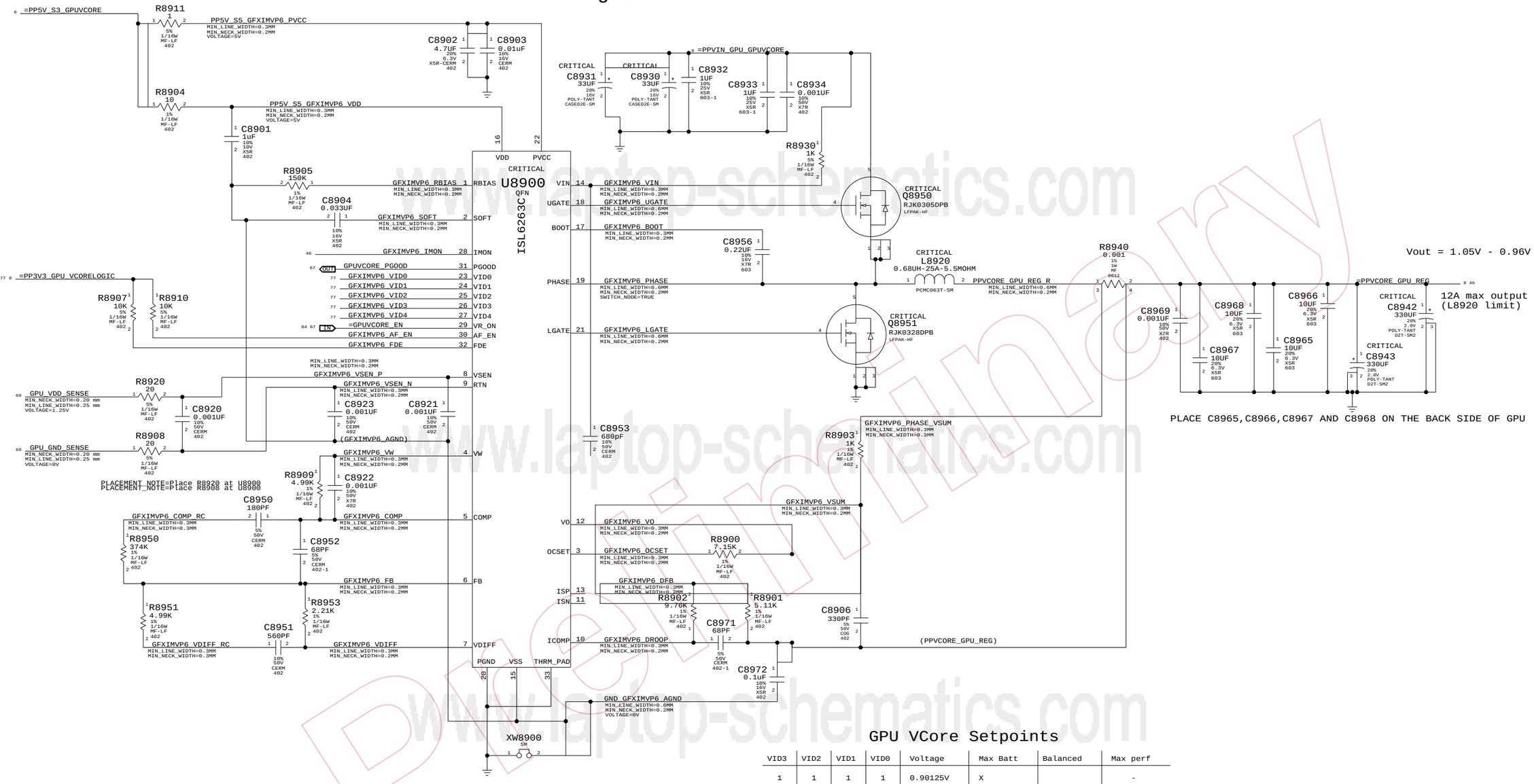
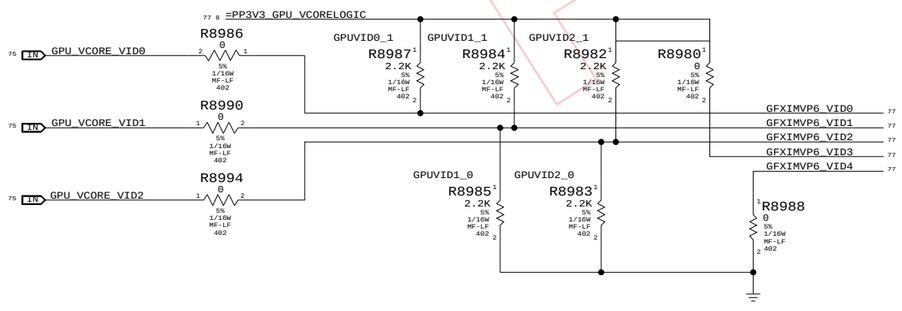
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 88 OF 123	

GPU VCore Regulator





GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	X		-
1	1	1	0	0.92700V	-	X	-
1	0	1	1	1.00425V	-	-	X

Other VID states may not be valid

Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

GPU (G96) CORE SUPPLY

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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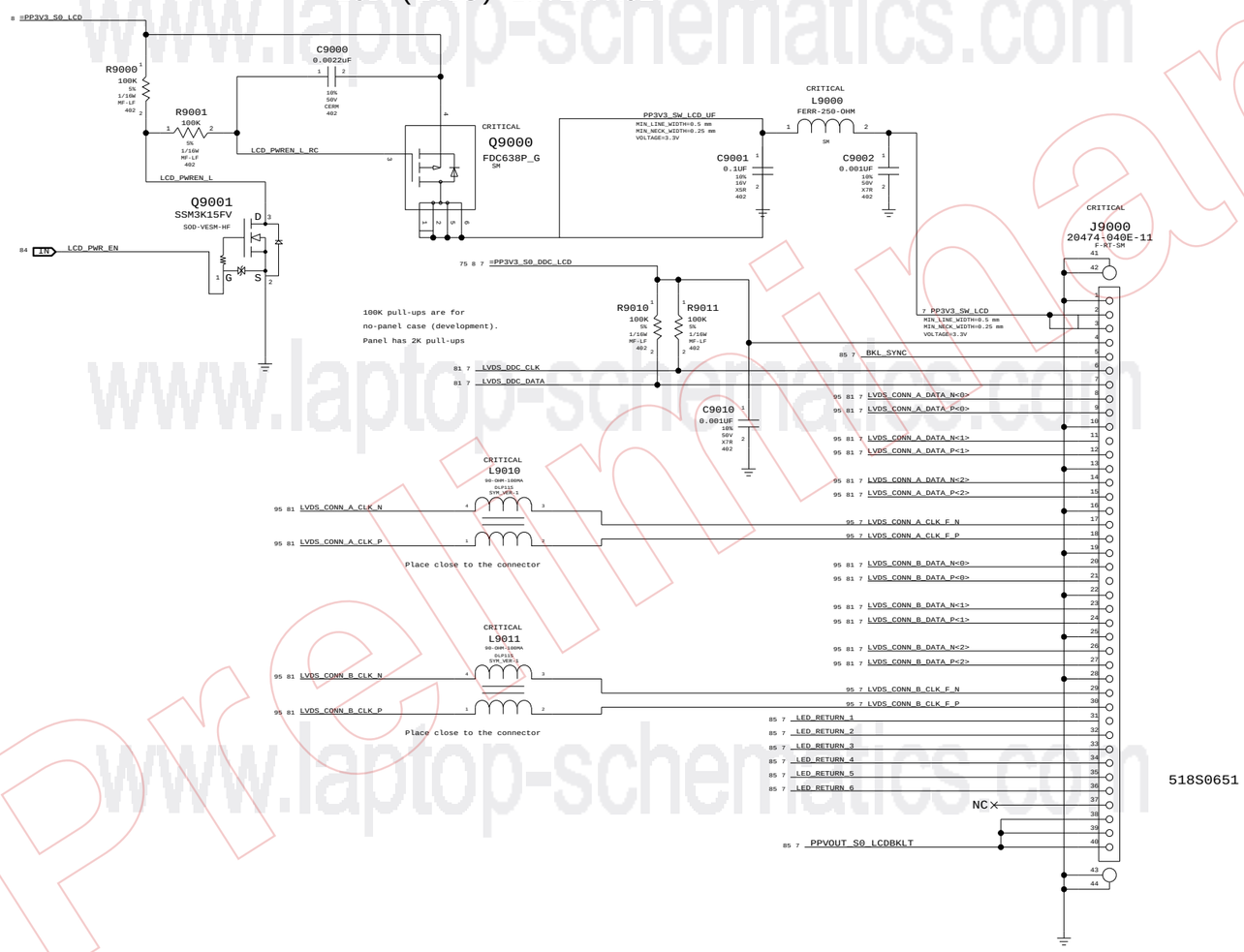
SCALE: NONE	SHT 89 OF 123	

LCD (LVDS) INTERFACE



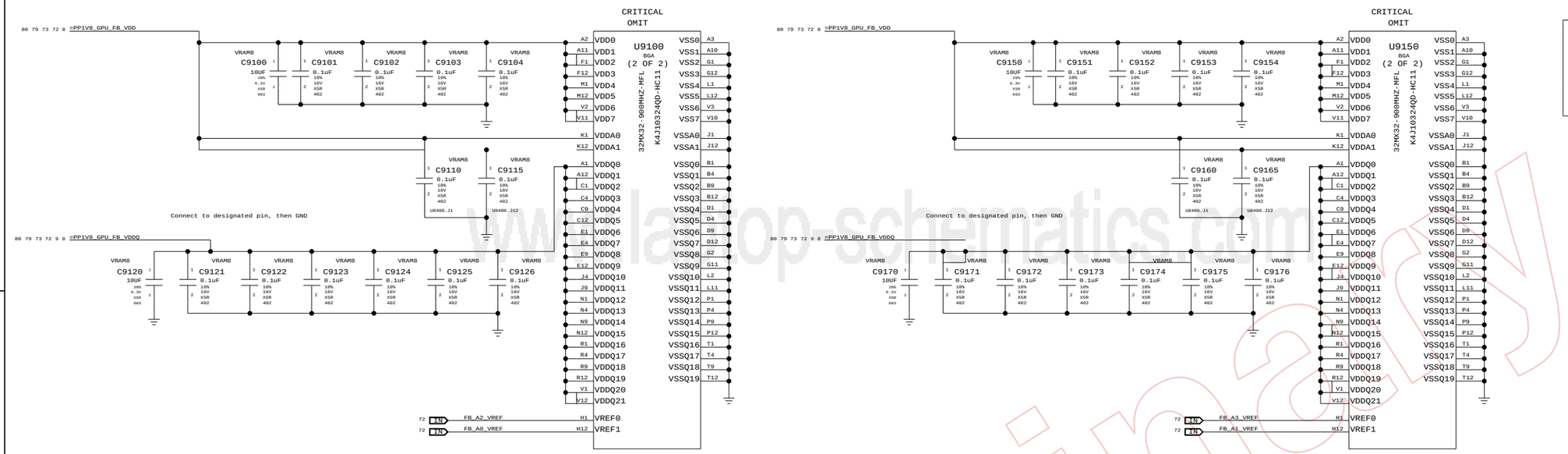
518S0651

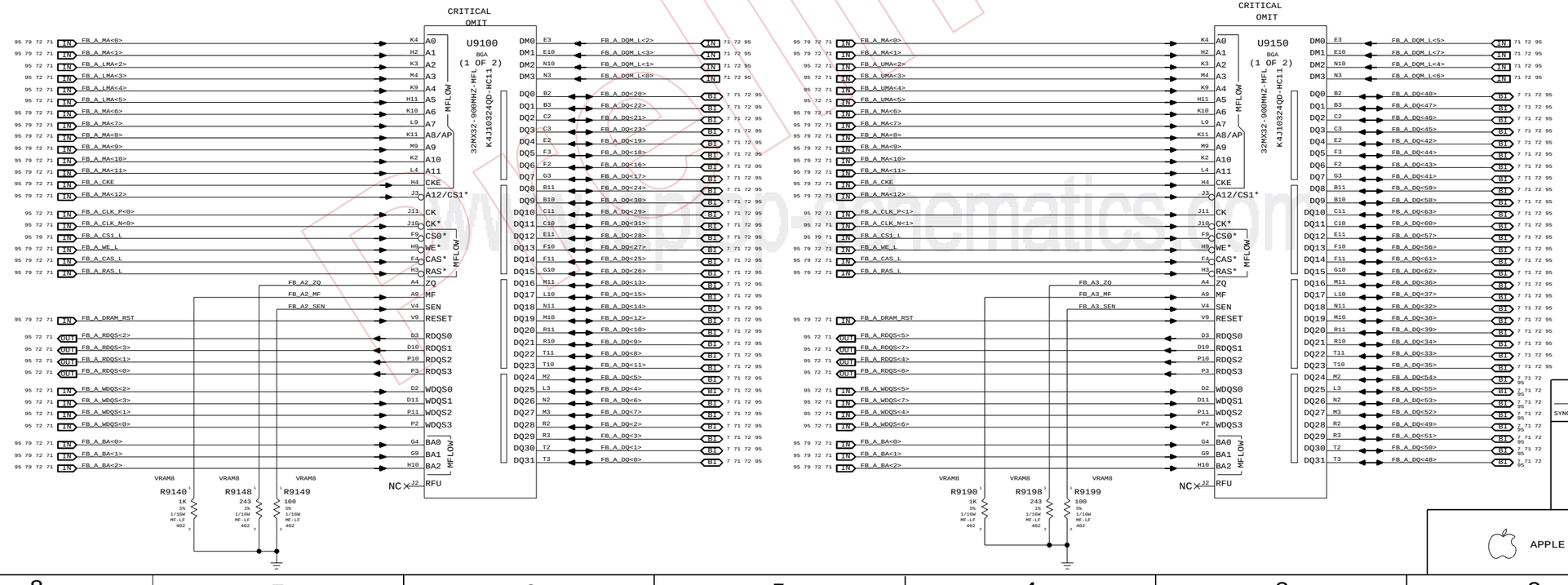
LVDS Display Connector

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	90	123





Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

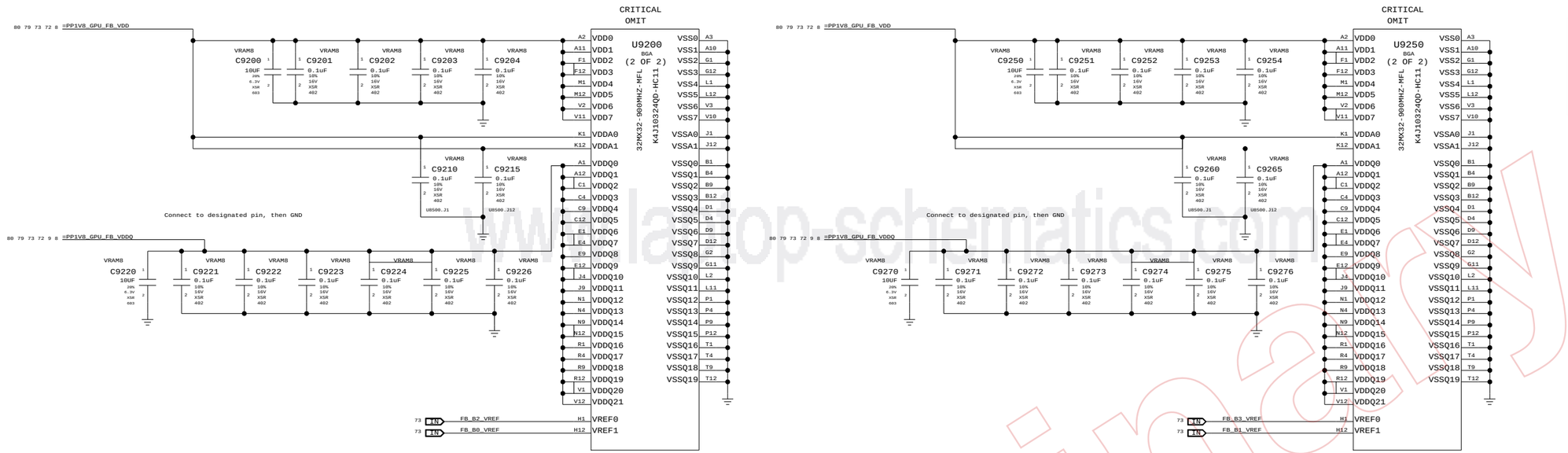
VRAM8

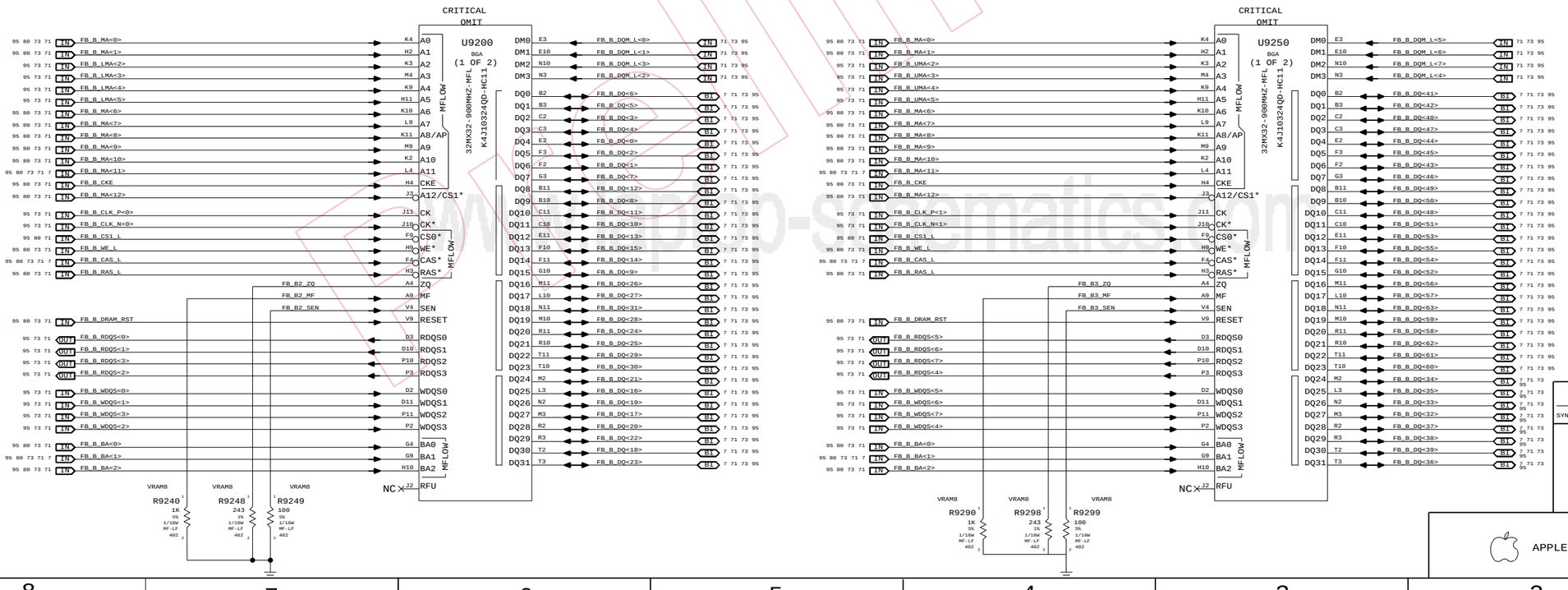
GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M99_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 91 OF 123	





Page Notes

Power aliases required by this page:

- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

VRAM8

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M88_MLB SYNC_DATE=11/01/2007

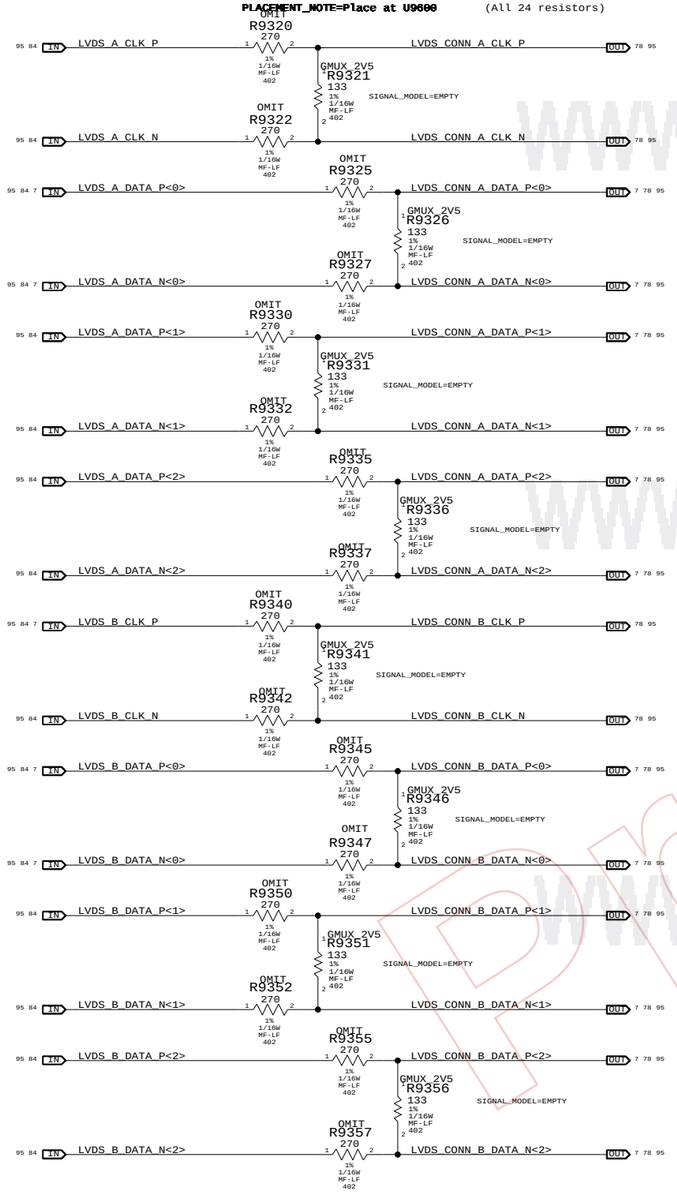
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 92 OF 123	

LVDS Transmitter Termination

All emulated LVDS outputs require this termination

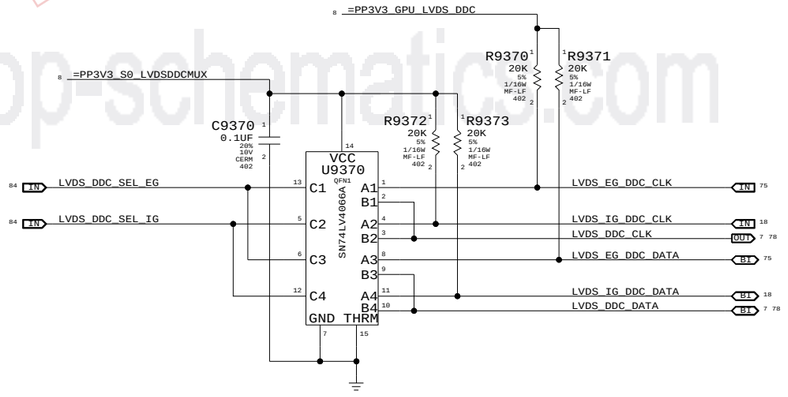
PLACEMENT_NOTE=Place at U9600 (All 24 resistors)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L			GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1,0402,SMD,LF			GMUX_1V8

DisplayPort Mux

LVDS DDC MUX



Muxed Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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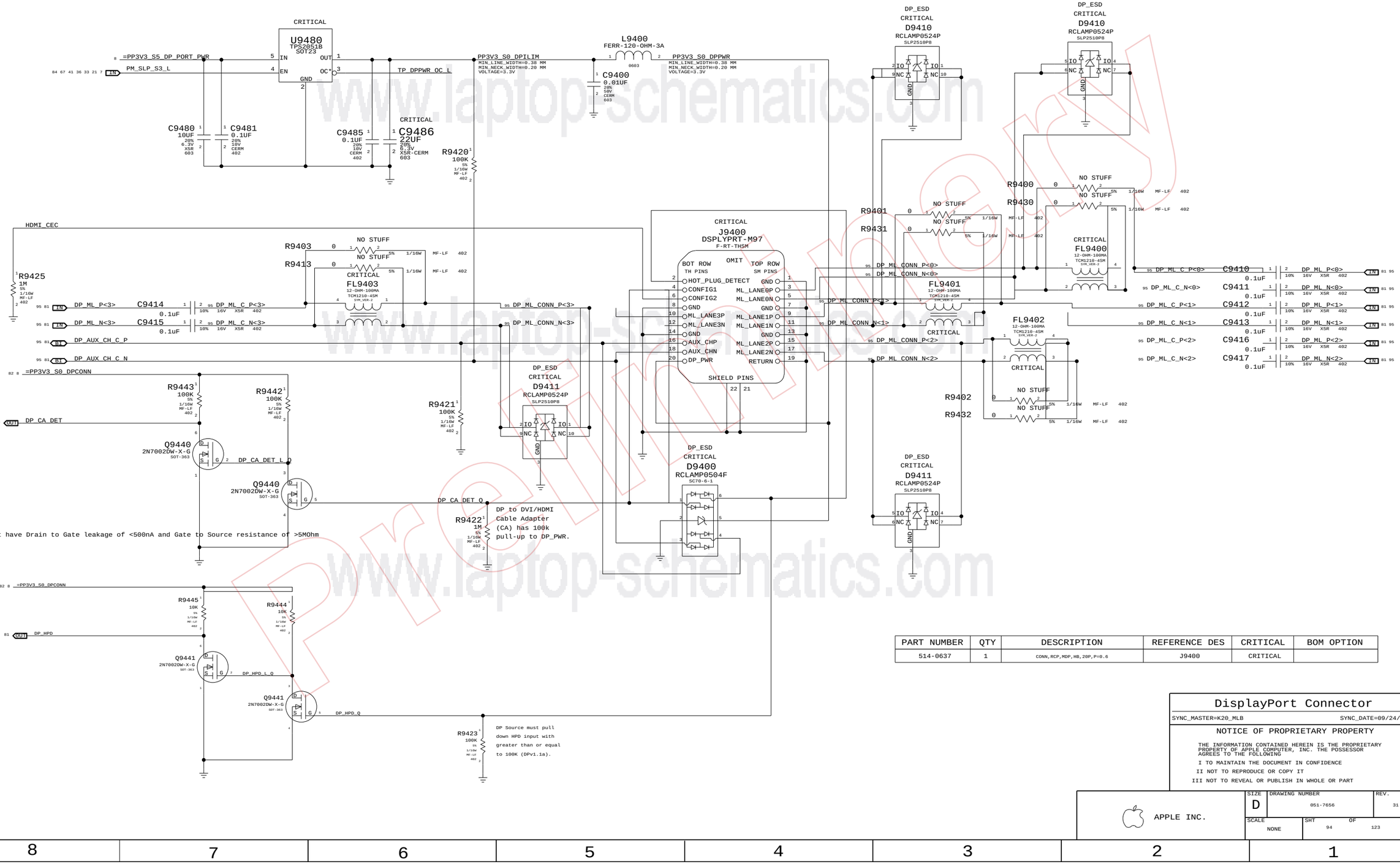
D	051-7656	31
SCALE: NONE	SHT 93 OF 123	

Port Power Switch



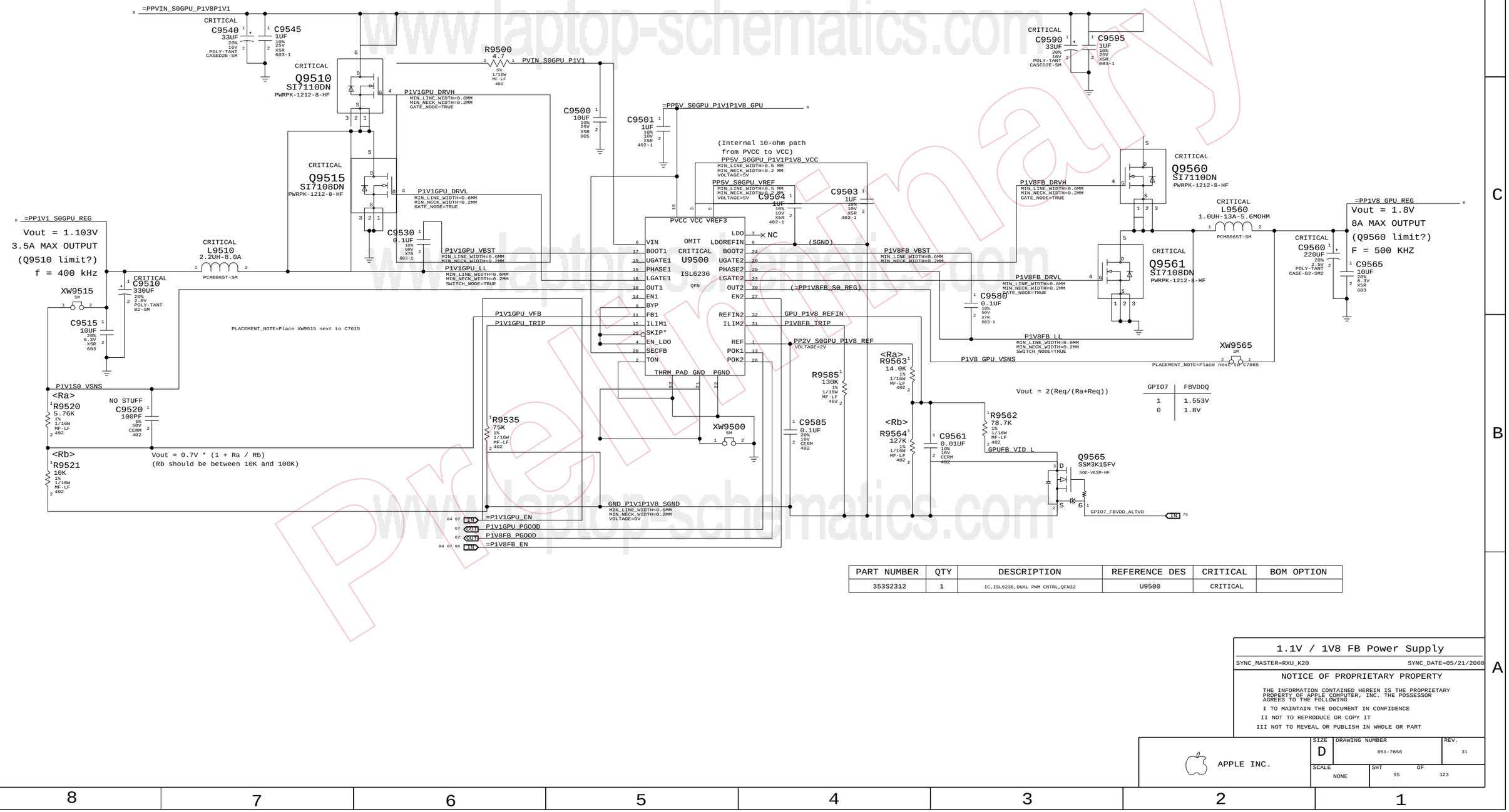
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0637	1	CONN,RCP,MDP,HB,20P,P=0.6	J9400	CRITICAL	

DisplayPort Connector

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 94 OF 123	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CNTRL,QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 95 OF 123	

GMUX CPLD

=PP3V3_S0_GMUX
C9610 0.1UF 20% 10V CERM 402
C9621 0.1UF 20% 10V CERM 402
C9622 0.1UF 20% 10V CERM 402
C9623 0.1UF 20% 10V CERM 402
C9624 0.1UF 20% 10V CERM 402
C9625 0.1UF 20% 10V CERM 402
C9626 0.1UF 20% 10V CERM 402
C9627 0.1UF 20% 10V CERM 402
C9628 0.1UF 20% 10V CERM 402
C9629 0.1UF 20% 10V CERM 402

=PP2V5_S0_GMUX
C9611 0.1UF 20% 10V CERM 402
C9612 0.1UF 20% 10V CERM 402
C9613 0.1UF 20% 10V CERM 402
C9614 0.1UF 20% 10V CERM 402
C9615 0.1UF 20% 10V CERM 402
C9616 0.1UF 20% 10V CERM 402
C9617 0.1UF 20% 10V CERM 402

=PP1V2_S0_GMUX
C9600 4.7UF 20% 4V X5R 402
C9604 0.1UF 20% 10V CERM 402
C9605 0.1UF 20% 10V CERM 402
C9606 0.1UF 20% 10V CERM 402
C9607 0.1UF 20% 10V CERM 402
C9608 0.1UF 20% 10V CERM 402
C9609 0.1UF 20% 10V CERM 402

=PP3V3_S0_GMUX
R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402

NO STUFF
R9641 10K 1% 1/16W MF-LF 402
NO STUFF
R9646 10K 1% 1/16W MF-LF 402

NO STUFF
R9647 10K 1% 1/16W MF-LF 402

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

PP3V3_S0_GMUX_ULC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
L9621 FERR-220-OHM 0402
C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
L9620 FERR-220-OHM 0402
C9630 0.1UF 20% 10V CERM 402

VCC: C4, J3, J13, N11, P8
VCCAUX: C11, J2, J14, M8
VCCIO00: B11
VCCIO01: B5
VCCIO02: B7
VCCIO03: A12
VCCIO04: C14
VCCIO05: F13
VCCIO06: M12
VCCIO07: M9, M3, N5, M1, C3, F2
VCCJ: K12
ULC_VCCPLL: A4
LRC_VCCPLL: P11

OMIT
CRITICAL

U9600
XP28
CSBGA-HF

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	IN
JTAG_GMUX_TDO	K13	TDO	OUT
JTAG_GMUX_TMS	L12	TMS	IN
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB2A	OUT
LCD_BKLT_PWM	N2	PB2B	OUT
LVDS_DDC_SEL_EG	P4	PB14A	OUT
LVDS_DDC_SEL_IG	N4	PB14B	OUT
DP_MUX_EN	N3	PB15A (do)	OUT
DP_MUX_SEL_EG	M4	PB15B	OUT
EG_RESET_L	P5	PB16A	OUT
EG_RAIL1_EN	M5	PB16B	OUT
EG_RAIL2_EN	P6	PB17A	OUT
EG_RAIL3_EN	M6	PB17B	OUT
EG_RAIL4_EN	P7	PB18A	OUT
EG_CLKREQ_OUT_L	M7	PB18B (do)	OUT
DP_CA_DET_EG	N7	PB19A	OUT
LCD_PWR_EN	N8	PB19B	OUT
LPC_AD<0>	P9	PB20A	BI
LPC_AD<1>	N9	PB20B	BI
LPC_AD<2>	P10	PB30A	BI
LPC_AD<3>	M10	PB30B	BI
LPC_FRAME_L	P12	PB31A	BI
LPC_RESET_L	P13	PB31B	IN
LPC_CLK33M_GMUX	N12	PB32A	IN
GMUX_INT	P14	PB32B	OUT
LVDS_IG_B_DATA_P<2>	B1	PL2A	IN
LVDS_IG_B_DATA_N<2>	B2	PL2B	IN
TP_GMUX_PL10A	C2	PL10A	
TP_GMUX_PL10B	D3	PL10B	
LVDS_IG_A_DATA_P<0>	D1	PL11A	IN
LVDS_IG_A_DATA_N<0>	E1	PL11B	IN
LVDS_IG_A_DATA_P<1>	D2	PL12A	IN
LVDS_IG_A_DATA_N<1>	E3	PL12B	IN
LVDS_IG_A_DATA_P<2>	F1	PL13A	IN
LVDS_IG_A_DATA_N<2>	G1	PL13B	IN
LVDS_IG_B_DATA_P<0>	F3	PL14A	IN
LVDS_IG_B_DATA_N<0>	G2	PL14B	IN
LVDS_IG_B_DATA_P<1>	H2	PL15A	IN
LVDS_IG_B_DATA_N<1>	G3	PL15B	IN
LVDS_IG_A_CLK_P	H1	PL16A	IN
LVDS_IG_A_CLK_N	H3	PL16B	IN
LVDS_MUX_SEL_EG	L1	PL18A	OUT
TP_GMUX_PL18B_VSYNC	L3	PL18B	
=GMUX_PCIE_RESET_L	K3	PL19A	IN
GMUX_PM_SLP_S3_L	L2	PL19B	IN
ALL_EG_PGOOD	N1	PL32A	IN
EG_CLKREQ_IN_L	P1	PL32B	IN

BANK5, BANK4, BANK7, BANK6

GND: J1, B8, C6, F12, G13, J14, N10, P3, M2, C1, E2, B4, M11
GNDIO00, GNDIO01, GNDIO02, GNDIO03, GNDIO04, GNDIO05, GNDIO06, GNDIO07, ULC_GNDPLL, LRC_GNDPLL

LVDS_B_DATA_P<0>	A2	PT2A	OUT
LVDS_B_DATA_N<0>	A3	PT2B	OUT
LVDS_B_DATA_P<1>	A1	PT3A	OUT
LVDS_B_DATA_N<1>	B3	PT3B	OUT
LVDS_B_DATA_P<2>	C5	PT4A	OUT
LVDS_B_DATA_N<2>	A5	PT4B	OUT
EG_PWRSEQ_EN	B6	PT14A	IN
GMUX_DEBUG_RESET_L	C7	PT14B	IN
LVDS_A_CLK_P	A6	PT15A	OUT
LVDS_A_CLK_N	A7	PT15B	OUT
LVDS_B_CLK_P	C8	PT16A	OUT
LVDS_B_CLK_N	C9	PT16B	OUT
LVDS_A_DATA_P<0>	A8	PT17A	OUT
LVDS_A_DATA_N<0>	B9	PT17B	OUT
LVDS_A_DATA_P<1>	A9	PT18A	OUT
LVDS_A_DATA_N<1>	C10	PT18B	OUT
LVDS_A_DATA_P<2>	B10	PT19A	OUT
LVDS_A_DATA_N<2>	A10	PT19B	OUT
TP_GMUX_PT20A	A11	PT20A	
TP_GMUX_PT20B	B12	PT20B	
TP_GMUX_PT32A	B13	PT32A	
TP_GMUX_PT32B	A13	PT32B	

BANK0, BANK1

DP_CA_DET	A14	PR2A	IN
DP_HOTPLUG_DET	B14	PR2B	IN
LVDS_EG_A_DATA_P<0>	D12	PR10A	IN
LVDS_EG_A_DATA_N<0>	D13	PR10B	IN
LVDS_EG_A_DATA_P<1>	D14	PR11A	IN
LVDS_EG_A_DATA_N<1>	E14	PR11B	IN
LVDS_EG_A_DATA_P<2>	E12	PR12A	IN
LVDS_EG_A_DATA_N<2>	F12	PR12B	IN
LVDS_EG_B_DATA_P<0>	G12	PR13A	IN
LVDS_EG_B_DATA_N<0>	G14	PR13B	IN
LVDS_EG_B_DATA_P<1>	G12	PR14A	IN
LVDS_EG_B_DATA_N<1>	G13	PR14B	IN
LVDS_EG_B_DATA_P<2>	H13	PR15A	IN
LVDS_EG_B_DATA_N<2>	H12	PR15B	IN
LVDS_EG_A_CLK_P	H14	PR16A	IN
LVDS_EG_A_CLK_N	J12	PR16B	IN
IG_LCD_PWR_EN	L14	PR18A	IN
EG_LCD_PWR_EN	M13	PR18B	IN
IG_BKLT_EN	N14	PR30A	IN
EG_BKLT_EN	N13	PR30B	IN

BANK2, BANK3

GMUX_JTAG_TCK Inversion

JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
SILK_PART=GMUX_RST
GMUX_JTAG_TCK_L

PM_SLP_S3_L Isolation

=PP3V3_S0_GMUX
Q9670 SSM6N15FEAPE SOT563
R9670 10K 1% 1/16W MF-LF 402
PM_SLP_S3_L
GMUX_PM_SLP_S3_L
EG_PWRSEQ_EN
MAKE_BASE=TRUE

=PP3V3_S3_GMUX
R9676 100K 5% 1/16W MF-LF 402
Q9607 SSM6N15FEAPE SOT563
GMUX_S3_PD_EN

=PP3V3_S0_GMUX
NO STUFF
R9677 10K 1% 1/16W MF-LF 402
GMUX_S0_PD_DIS_RC
Q9607 SSM6N15FEAPE SOT563
NO STUFF
C9695 1UF 10% 6.3V CERM 402
ALL_SYS_PWRGD
R9684 0 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_BK_BLANK
341S2354	1	IC,CPLD,LATTICE,132CSBGA,K20	U9600	CRITICAL	GMUX_PROG

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9600 (All 14 resistors)

LVDS_IG_A_CLK_P	R9650	100	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA_P<0>	R9651	100	LVDS_IG_A_DATA_N<0>	
LVDS_IG_A_DATA_P<1>	R9652	100	LVDS_IG_A_DATA_N<1>	
LVDS_IG_A_DATA_P<2>	R9653	100	LVDS_IG_A_DATA_N<2>	
LVDS_IG_B_DATA_P<0>	R9654	100	LVDS_IG_B_DATA_N<0>	
LVDS_IG_B_DATA_P<1>	R9655	100	LVDS_IG_B_DATA_N<1>	
LVDS_IG_B_DATA_P<2>	R9656	100	LVDS_IG_B_DATA_N<2>	
LVDS_EG_A_CLK_P	R9660	100	LVDS_EG_A_CLK_N	
LVDS_EG_A_DATA_P<0>	R9661	100	LVDS_EG_A_DATA_N<0>	
LVDS_EG_A_DATA_P<1>	R9662	100	LVDS_EG_A_DATA_N<1>	
LVDS_EG_A_DATA_P<2>	R9663	100	LVDS_EG_A_DATA_N<2>	
LVDS_EG_B_DATA_P<0>	R9664	100	LVDS_EG_B_DATA_N<0>	
LVDS_EG_B_DATA_P<1>	R9665	100	LVDS_EG_B_DATA_N<1>	
LVDS_EG_B_DATA_P<2>	R9666	100	LVDS_EG_B_DATA_N<2>	

All: 1% 1/16W MF-LF 402
SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX
GMUX_DEBUG_RESET_L R9680 1K 5% 1/16W MF-LF 402
JTAG_GMUX_TCK R9690 4.7K 5% 1/16W MF-LF 402
EG_CLKREQ_OUT_L R9695 10K 5% 1/16W MF-LF 402

NO STUFF
R9679 10K 1% 1/16W MF-LF 402

PLACEMENT_NOTE=Place on top side at U9600

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K
LVDS_DDC_SEL_IG	R9682	10K
LVDS_DDC_SEL_EG	R9683	10K

5% 1/16W MF-LF 402

NO STUFF

EG_RESET_L	R9691	100K
GMUX_INT	R9692	20K
LCD_BKLT_PWM	R9693	100K
EG_CLKREQ_IN_L	R9694	100K

5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

EG_PWRSEQ_HW
R9630 0 5% 1/16W MF-LF 402 EXTGPU_PWR_EN OUT 67

EG_PWRSEQ_GMUX
R9631 0 5% 1/16W MF-LF 402 =P1V1GPU_EN OUT 67 83
R9632 0 5% 1/16W MF-LF 402 P3V3GPU_EN OUT 67 68
R9633 0 5% 1/16W MF-LF 402 GPUVCORE_EN OUT 67 77
R9634 0 5% 1/16W MF-LF 402 =P1V8FB_EN OUT 66 67 83

The MAKE BASE properties for these signals are on the POWER CONTROL page.

LCD_PWR_EN
R9678 4.7K 5% 1/16W MF-LF 402
EG_PWRSEQ_GMUX
R9671 4.7K 5% 1/16W MF-LF 402
R9672 4.7K 5% 1/16W MF-LF 402
R9673 4.7K 5% 1/16W MF-LF 402
R9674 4.7K 5% 1/16W MF-LF 402
GMUX_S3_PD_GND
NO STUFF R9675 0 5% 1/16W MF-LF 402
NO STUFF C9691 0.1UF 20% 10V CERM 402
NO STUFF C9692 0.1UF 20% 10V CERM 402
NO STUFF C9693 0.1UF 20% 10V CERM 402
NO STUFF C9694 0.1UF 20% 10V CERM 402

Graphics MUX (GMUX)

SYNC_MASTER=T18_MXMGMUX SYNC_DATE=02/13/2008

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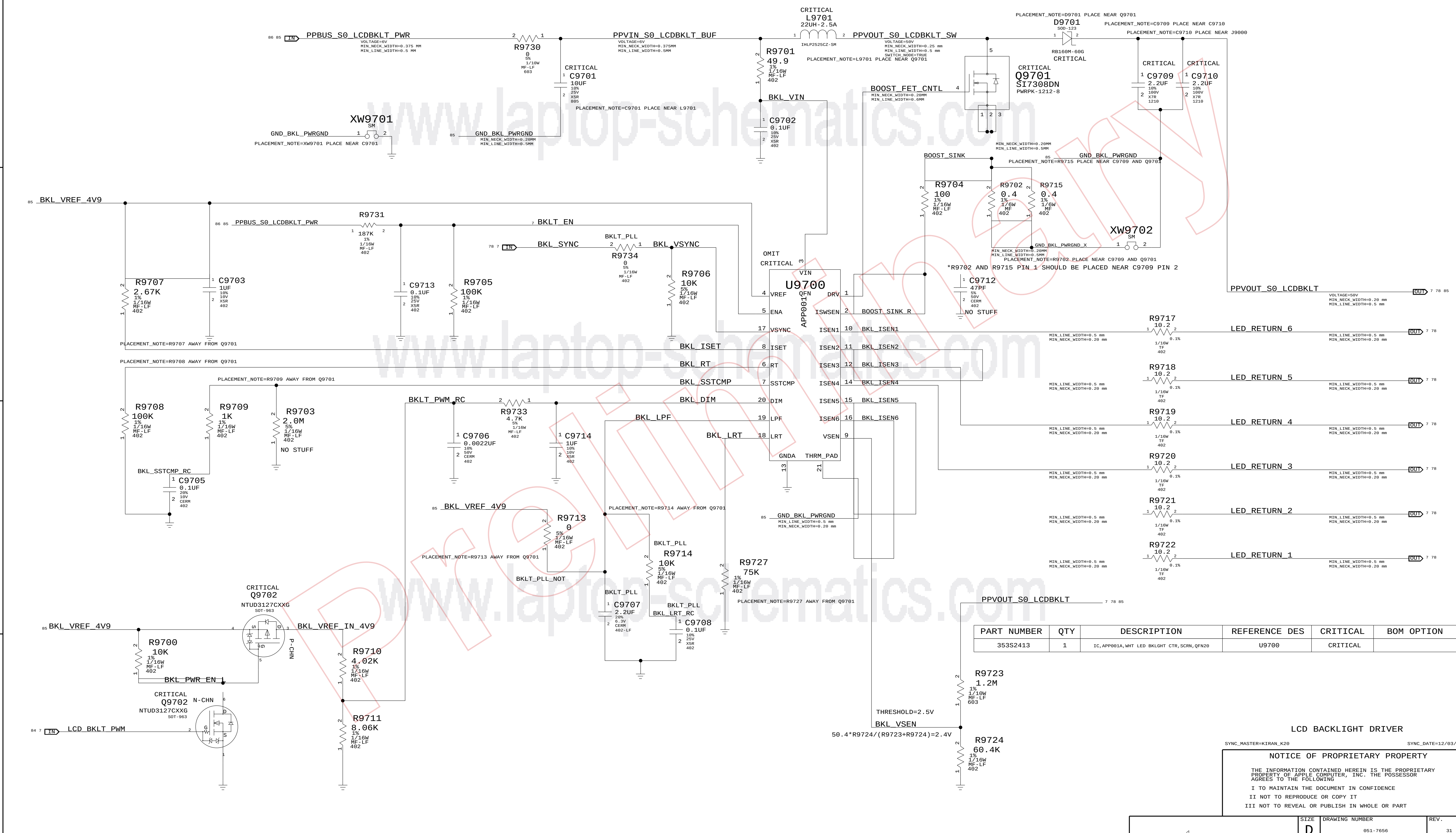
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 96 OF 123	

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2413	1	IC,APP001A,WHT LED BKLGHT CTR,SCRN,QFN20	U9700	CRITICAL	

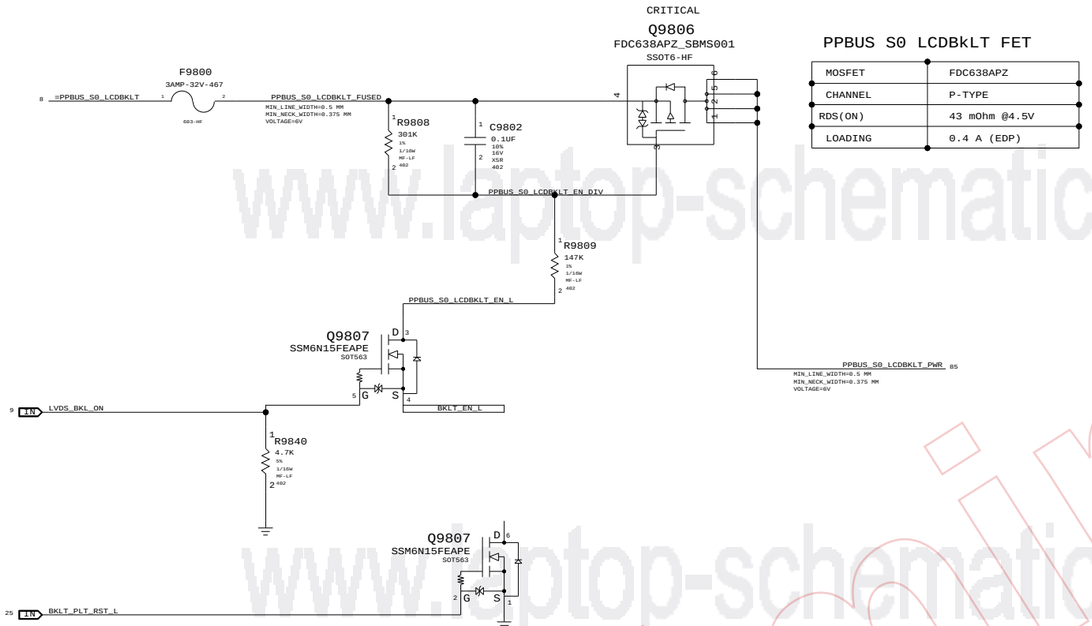
*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

LCD BACKLIGHT DRIVER

SYNC_MASTER=KIRAN_K20 SYNC_DATE=12/03/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-7656 | REV. 31
SCALE NONE | SHT 97 OF 123



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

LCD Backlight Support

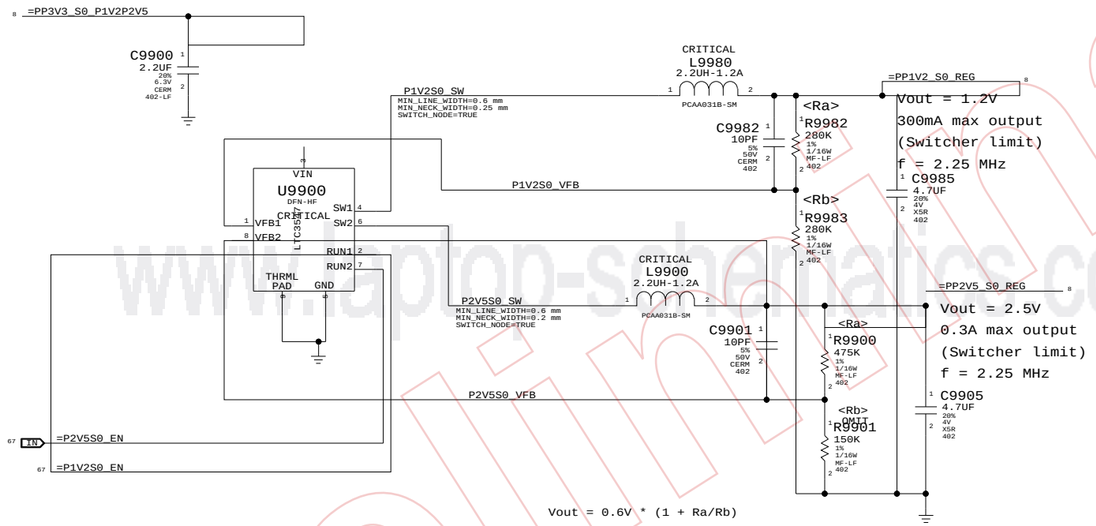
SYNC_MASTER=YLEE_K20 SYNC_DATE=07/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	98	123

GMUX 1.8V/1.2V S0 Switcher



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0428	1	RES,MTL FILM,1/16W,150K,1,0402,SMD,LF	R9901		GMUX_2V5
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R9901		GMUX_1V8

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	99	123

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 42 61
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 42
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 61
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 61
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	61
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 61
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61

CPU/FSB Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 100 OF 123	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

Memory Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE: NONE SHT 101 OF 123

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	69
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	69
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 69
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 69
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	69
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	69
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7 17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7 17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P	35
	PCIE_90D	PCIE	PCIE_FW_R2D_N	35
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 35
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 35
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	35
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	35
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	7 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	7 31
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	17 31
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	7 17 31
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	7 17 31
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 69
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 69
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 30
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 35
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 35
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 31
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 24
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 24
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 24
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 24
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	18 24
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	18 24
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 24
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_HDD_R2D_P	7 38
	SATA_100D	SATA	SATA_HDD_R2D_N	7 38
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 38
	SATA_100D	SATA	SATA_HDD_D2R_N	20 38
	SATA_100D	SATA	SATA_HDD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_HDD_D2R_C_N	7 38
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 38
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 38
	SATA_100D	SATA	SATA_ODD_R2D_P	7 38
	SATA_100D	SATA	SATA_ODD_R2D_N	7 38
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 38
	SATA_100D	SATA	SATA_ODD_D2R_N	20 38
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 38
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 38
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

MCP Constraints 1

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 7 19 41 43 84
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 7 19 41 43 84
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 19 25 84
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 25 41
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 7 25 43
USB_EXTA	USB_90D	USB	USB_EXTA_P 20 39
	USB_90D	USB	USB_EXTA_N 20 39
	USB_90D	USB	USB_EXTA_MUXED_P
	USB_90D	USB	USB_EXTA_MUXED_N
USB_MINI	USB_90D	USB	USB_MINI_P 9 20
	USB_90D	USB	USB_MINI_N 9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P 9 20
	USB_90D	USB	USB_EXTD_N 9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 20 30
	USB_90D	USB	USB_CAMERA_N 20 30
USB_BT	USB_90D	USB	USB_BT_P 20 30
	USB_90D	USB	USB_BT_N 20 30
USB_TPAD	USB_90D	USB	USB_TPAD_P 20 49
	USB_90D	USB	USB_TPAD_N 20 49
USB_IR	USB_90D	USB	USB_IR_P 20 40
	USB_90D	USB	USB_IR_N 20 40
USB_EXTB	USB_90D	USB	USB_EXTB_P 20 39
	USB_90D	USB	USB_EXTB_N 20 39
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 20 31
	USB_90D	USB	USB_EXCARD_N 20 31
USB_EXTC	USB_90D	USB	USB_EXTC_P 20 96 98
	USB_90D	USB	USB_EXTC_N 20 96 98
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 7 13 21 44
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 7 13 21 44
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 21 44
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 21 44
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 9 21
	HDA_55S	HDA	HDA_BIT_CLK_R 21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 21 53
	HDA_55S	HDA	HDA_SYNC_R 21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 21
	HDA_55S	HDA	HDA_RST_L 21 53
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 21 53
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 21 53
	HDA_55S	HDA	HDA_SDOUT_R 21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 21 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 25 41
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 21 43
	SPI_55S	SPI	SPI_CLK 52
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 21 43
	SPI_55S	SPI	SPI_MOSI 52
SPI_MISO	SPI_55S	SPI	SPI_MISO 21 43
	SPI_55S	SPI	SPI_MISO_R 52
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 21 43
	SPI_55S	SPI	SPI_CS0_L

MCP Constraints 2

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 33
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	32 33
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 32
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 32
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 32
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 32
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 32
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 32
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32 34
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32 34

Ethernet Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPA	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P0_TPB	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPA	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP
FW_P1_TPB	FW_110D	FW_TP

Port 2 Not Used

FW_P0_TPA_P 35 37
FW_P0_TPA_N 35 37
FW_P0_TPB_P 35 37
FW_P0_TPB_N 35 37
FW_P1_TPA_P 35 37
FW_P1_TPA_N 35 37
FW_P1_TPB_P 35 37
FW_P1_TPB_N 35 37

FireWire Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	7 44
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	7 44
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	44
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	7 44
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	7 44
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	60
	1TO1_DIFFPAIR		CHGR_CSI_N	60
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	60
	1TO1_DIFFPAIR		CHGR_CSO_N	60

SMC Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
J145 LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
J146 LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
J190 LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	7 81 84
J189 LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	7 81 84
J153 LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	7 81 84
J152 LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
J200 LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	7 81 84
J201 LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	7 81 84
J157	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 78
J158	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 78
J154	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 78
J155	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 78
J135	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	78 81
J137	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	78 81
J132	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 78 81
J133	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 78 81
J134	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	78 81
J135	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	78 81
J136	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 78 81
J137	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 78 81
J151 DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	82
J150	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
J152 DP_ML	DP_100D	DISPLAYPORT	**DP_ML_P<3..0>**	81 82
J153	DP_100D	DISPLAYPORT	**DP_ML_N<3..0>**	81 82
J202 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
J203	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
J150 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
J149 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	71 72 79
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	71 72 79
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	7 71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	7 71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	71 72 79
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	71 72 79
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE	71 72 79
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L	71 72
FB_AB_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	71 72 79
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	71 72 79
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	71 72 79
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	71 72 79
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	71 72 79
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	71 72 79
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	71 72 79
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	71 72 79
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	71 72 79
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	71 72 79
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	71 72 79
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	7 71 72 79
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	7 71 72 79
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	7 71 72 79
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	7 71 72 79
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	71 72 79
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	71 72 79
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	71 72 79
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	71 72 79
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	71 72 79
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	71 72 79
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	71 72 79
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	71 72 79
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	71 72 79
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	71 72 79
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	71 72 79
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	71 72 79
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	7 71 72 79
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	7 71 72 79
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	7 71 72 79
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	7 71 72 79
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	71 72 79
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	71 72 79
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	71 72 79
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	71 72 79
U200 FB_AB_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS1_L	71 79

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOT96)	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M	75
CK505_CLK27MSS	CLK_SLOW_555	CLK_SLOW	GPU_CLK27M_SS	75
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	76 84
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	76 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	7 76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	76 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	76 84
J142 DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_P<3..0>**	76 81
J144 DP_ML	DP_100D	DISPLAYPORT	**DP_EG_ML_N<3..0>**	76 81
J145 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	76 81
J143 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	76 81
J139	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	81
J138	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	71 73 80
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	71 73 80
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	7 71 73 80
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	71 73 80
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE	71 73 80
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L	7 71 73
FB_CD_CMD_EO	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	71 73 80
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	71 73 80
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	71 73 80
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	71 73 80
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	71 73 80
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	71 73 80
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	71 73 80
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	71 73 80
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	71 73 80
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	71 73 80
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	71 73 80
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	7 71 73 80
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	7 71 73 80
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	7 71 73 80
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	7 71 73 80
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	71 73 80
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	71 73 80
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	71 73 80
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	71 73 80
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	71 73 80
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	71 73 80
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	71 73 80
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	71 73 80
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	71 73 80
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	71 73 80
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	71 73 80
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	71 73 80
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	7 71 73 80
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	7 71 73 80
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	7 71 73 80
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	7 71 73 80
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	71 73 80
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	71 73 80
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	71 73 80
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	71 73 80
U200 FB_CD_CS1	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS1_L	71 80

GPU (G96) Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE: NONE	SHT 107 OF 123	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLSH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	34
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	34
U145	SATA_100D	SATA	SATA_ODD_R2D_UF_P	38
U145	SATA_100D	SATA	SATA_ODD_R2D_UF_N	38
U144	SATA_100D	SATA	SATA_ODD_D2R_UF_P	38
U142	SATA_100D	SATA	SATA_ODD_D2R_UF_N	38
U143	SATA_100D	SATA	SATA_HDD_D2R_UF_P	38
U140	SATA_100D	SATA	SATA_HDD_D2R_UF_N	38
U141	SATA_100D	SATA	SATA_HDD_R2D_UF_P	38
U139	SATA_100D	SATA	SATA_HDD_R2D_UF_N	38
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_P	46 64
	SENSE_1TO1_55S	SENSE	MCPCOREISNS_N	46 64
U134 CPUTHMSNS_D2_DP	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
U131	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
U127 CPU_THERMD_DP	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 47
U124	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 47
U129 GPUTHMSNS_D_DP	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
U128	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
U126 GPU_THERMD_DP	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 75
U125	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 75
U138 MCPTHMSNS_D_DP	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	7 47
U137	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	7 47
U135 MCP_THERMD_DP	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 47
U136	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 47
U158 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_P	46
U157	SENSE_1TO1_55S	SENSE	1V05CPUISNS_R_N	46
U155 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_R_P	46
U154	SENSE_1TO1_55S	SENSE	DDRISNS_R_N	46
U153 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_P	46
U152	SENSE_1TO1_55S	SENSE	GPUISENS_N	46
U151 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	1V05CPU_P	46 65
U150	SENSE_1TO1_55S	SENSE	1V05CPU_N	46 65
U149 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	DDRISNS_P	46
U148	SENSE_1TO1_55S	SENSE	DDRISNS_N	46
U168 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPU_P	46
U147	SENSE_1TO1_55S	SENSE	P1V8GPU_N	46
U186 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	45
U185	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	45
		GND	GND	
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8 9
		SB_POWER	PP1V5_S0	
U167 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	
U167	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	
U167 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	46
U167	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	46
T24 ASIC_CNTRLMEM1	FLSH_55S		NF_CLE_R	96
T24 ASIC_CNTRLMEM1	FLSH_55S		NF_ALE_R	96
T24 ASIC_CNTRLMEM1	FLSH_55S		NF_CE0_L_R	96
T24 ASIC_CNTRLMEM1	FLSH_55S		NF_CE1_L_R	96
T24 ASIC_CNTRLMEM1	FLSH_55S		NF_RE0_L_R	96
T24 ASIC_CNTRLMEM1	FLSH_55S		NF_WE0_L_R	96
T23 ASIC_CNTRLMEM2	FLSH_55S		NF_CLE_R	96
T24 ASIC_CNTRLMEM2	FLSH_55S		NF_ALE_R	96
T23 ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L_R	96
T23 ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L_R	96
T23 ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L_R	96
T23 ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L_R	96
T23 ASIC_CNTRLMEM3	FLSH_55S		NF_CLE	96
T23 ASIC_CNTRLMEM3	FLSH_55S		NF_ALE	96
T23 ASIC_CNTRLMEM3	FLSH_55S		NF_CE0_L	96
T23 ASIC_CNTRLMEM3	FLSH_55S		NF_CE1_L	96
T23 ASIC_CNTRLMEM3	FLSH_55S		NF_RE0_L	96
T22 ASIC_CNTRLMEM3	FLSH_55S		NF_WE0_L	96
T22 ASIC_CNTRLMEM2	FLSH_55S		NF_CLE	96
T22 ASIC_CNTRLMEM2	FLSH_55S		NF_ALE	96
T22 ASIC_CNTRLMEM2	FLSH_55S		NF_CE0_L	96
T22 ASIC_CNTRLMEM2	FLSH_55S		NF_CE1_L	96
T22 ASIC_CNTRLMEM2	FLSH_55S		NF_RE0_L	96
T22 ASIC_CNTRLMEM2	FLSH_55S		NF_WE0_L	96

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
J180	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
J180	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
J185	1TO1_DIFFPAIR		CHGR_CSI_R_P	60
J185	1TO1_DIFFPAIR		CHGR_CSI_R_N	60
J187	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 60
J185	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 60
J182 (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	39
J181 (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	39
J172 (USB_EXTA)	USB_90D	USB	USB2_LT1_P	7 39
J180 (USB_EXTA)	USB_90D	USB	USB2_LT1_N	7 39
J172 (USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_P	
J176 (USB_EXTD)	USB_90D	USB	CONN_TPAD_USB_N	
J176 (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 30
J176 (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 30
J174	USB_90D	USB	CONN_USB2_BT_P	7 30
J172	USB_90D	USB	CONN_USB2_BT_N	7 30
J173	USB_90D	USB	USB_LT2_P	7 39
J173	USB_90D	USB	USB_LT2_N	7 39
J180	USB_90D	USB	USB2_EXCARD_CONN_P	7 31
J176	USB_90D	USB	USB2_EXCARD_CONN_N	7 31
J185	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
J184	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
J187 MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
J188	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
J190 PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
J190	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
J192 PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
J192	PCIE_90D	PCIE	PCIE_FC_D2R_N	
J193	PCIE_90D	PCIE	PCIE_FC_R2D_P	
J193	PCIE_90D	PCIE	PCIE_FC_R2D_N	
J181	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	7 31
J180	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	7 31
J188 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_P	7 56 57
J187	DIFFPAIR	AUDIO	SPKRAMP_L1_OUT_N	7 56 57
J201 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_P	7 56 57
J200	DIFFPAIR	AUDIO	SPKRAMP_L2_OUT_N	7 56 57
J199 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_P	7 56 57
J202	DIFFPAIR	AUDIO	SPKRAMP_R1_OUT_N	7 56 57
J206 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_P	7 56 57
J207	DIFFPAIR	AUDIO	SPKRAMP_R2_OUT_N	7 56 57
J247 SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_P	7 56 57
J248	DIFFPAIR	AUDIO	SPKRAMP_LFE_OUT_N	7 56 57
J210	USB_90D	USB	USB_EXTC_P	20 91 98
J209	USB_90D	USB	USB_EXTC_N	20 91 98
J212	USB_90D	USB	USB_LT3_P	7 98
J213	USB_90D	USB	USB_LT3_N	7 98

Project Specific Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

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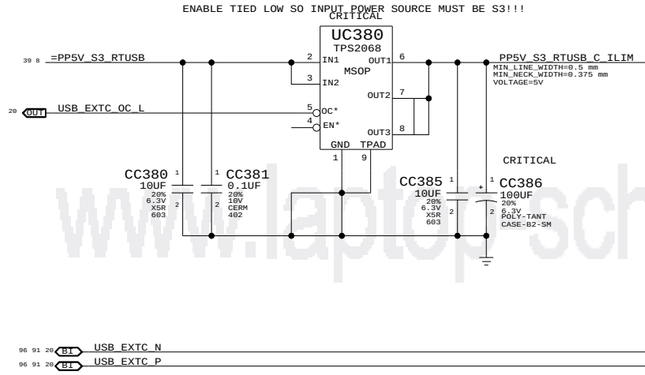
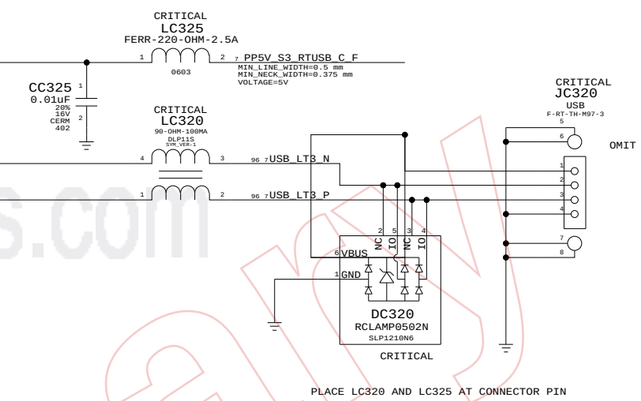
Port Power Switch



LEFT USB PORT C



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	1	CONN,RCPT,USB,HB,4P	JC320	CRITICAL	

PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31

SCALE	SHT	OF
NONE	123	123