1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE

SCHEM,MLB,M96
PVT
09/26/2008

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7631	1	SCHEM,MLB,M96	SCH	CRITICAL	
820-2375	1	PCBF,MLB,M96	PCB	CRITICAL	

DRAWING
TITLE=M96_MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Sep 26 10:40:55 2008

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

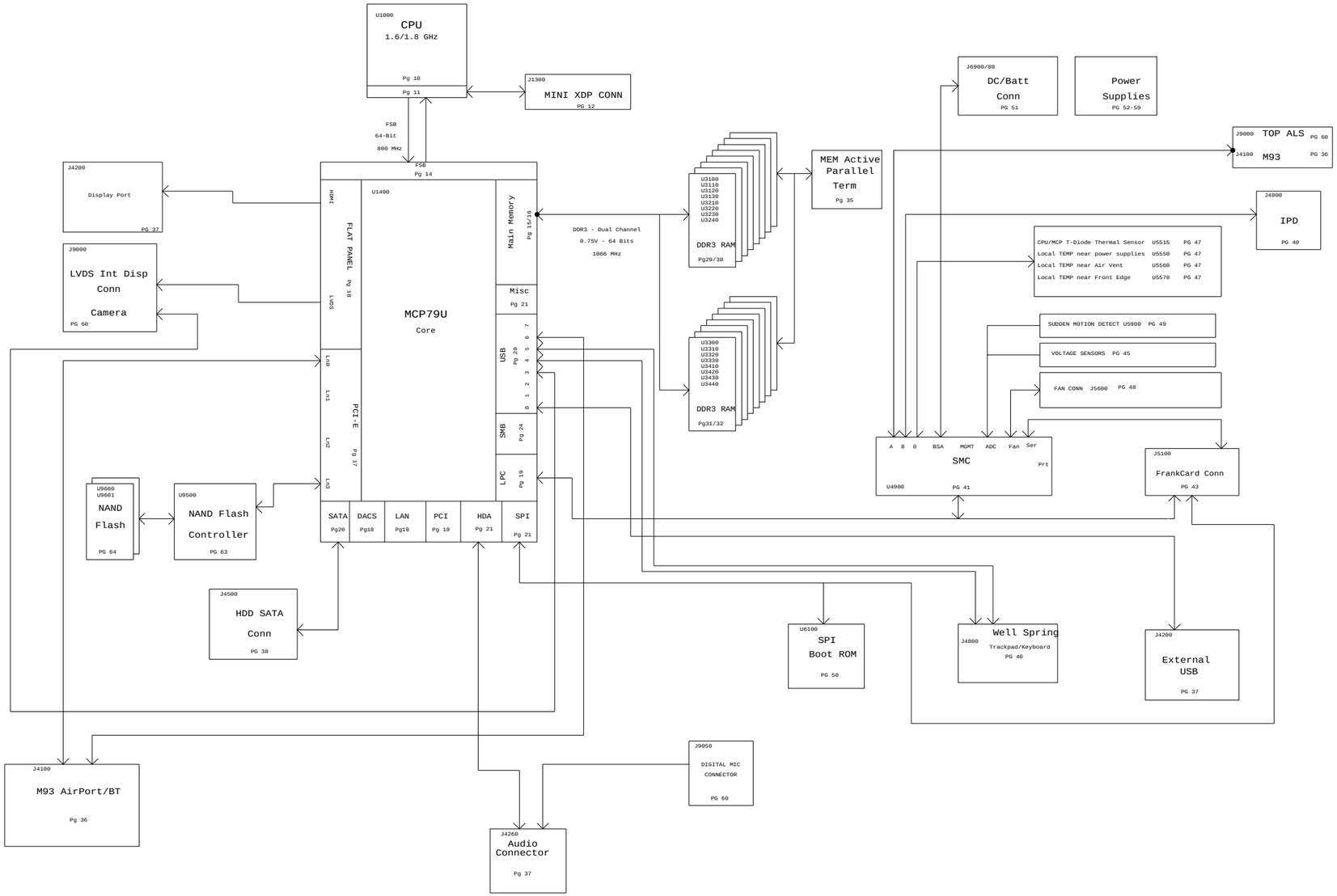
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,M96

DRAWING NUMBER 051-7631
REV. A.0.0

SHT 1 OF 71



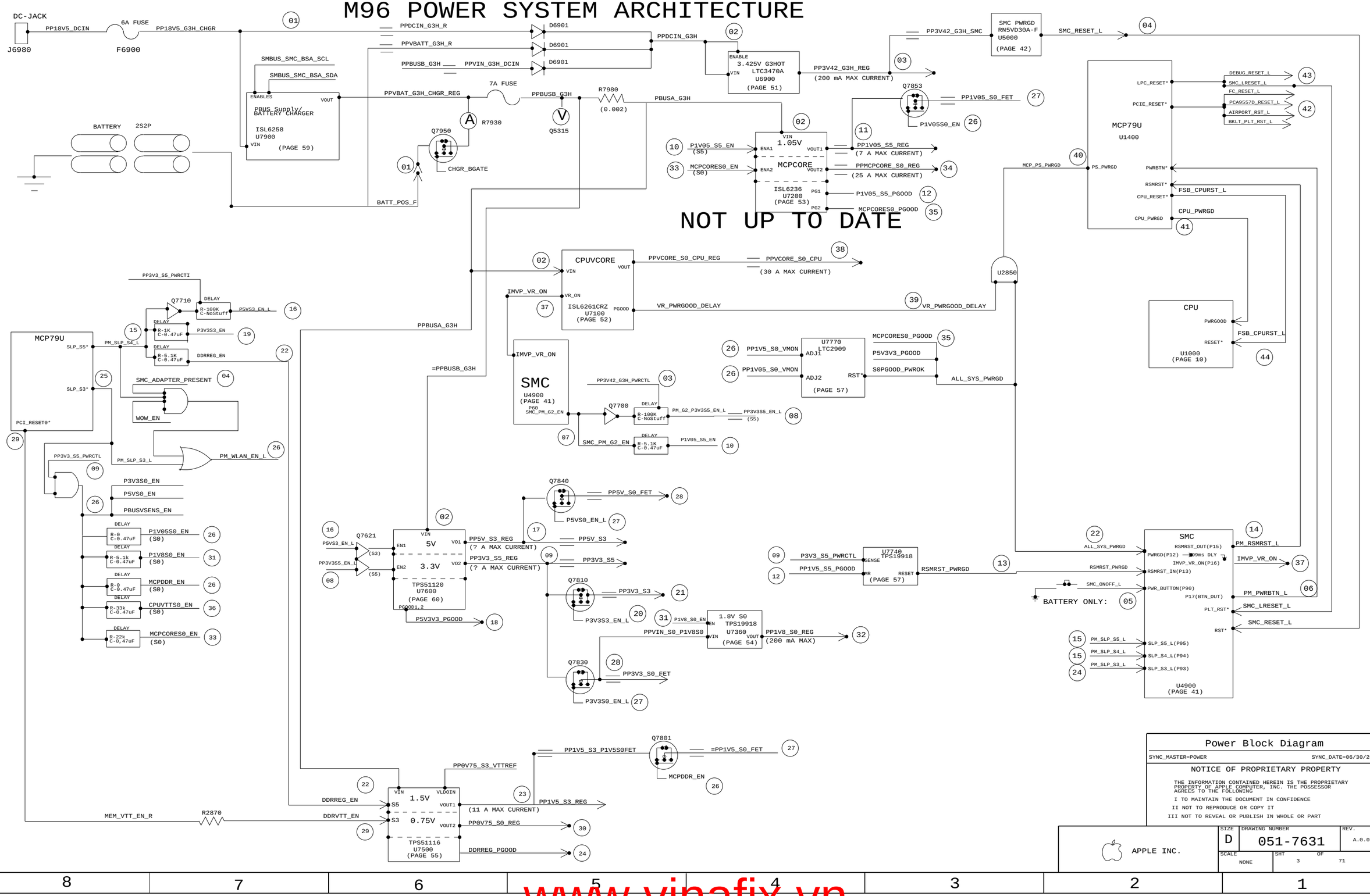
System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 2 OF 71	

M96 POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=POWER

SYNC_DATE=06/30/2005

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 3 OF 71	

BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9734	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M96	EEE_4DA,M96_COMMON,M96_HYNIX,M96_SS_CAP,CPU_1_6GHZ
630-9735	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M96	EEE_4DB,M96_COMMON,M96_HYNIX,M96_MU_CAP,CPU_1_6GHZ
630-9514	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M96	EEE_2AL,M96_COMMON,M96_HYNIX,M96_TY_CAP,CPU_1_6GHZ
630-9738	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M96	EEE_4DC,M96_COMMON,M96_HYNIX,M96_SS_CAP,CPU_1_8GHZ
630-9516	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M96	EEE_2AN,M96_COMMON,M96_HYNIX,M96_MU_CAP,CPU_1_8GHZ
630-9517	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M96	EEE_2AP,M96_COMMON,M96_HYNIX,M96_TY_CAP,CPU_1_8GHZ
630-9512	PCBA,MLB,1.6GHZ,MI 2GB,SS CAP,M96	EEE_2AJ,M96_COMMON,M96_MICRON,M96_SS_CAP,CPU_1_6GHZ
630-9513	PCBA,MLB,1.6GHZ,MI 2GB,MU CAP,M96	EEE_2AK,M96_COMMON,M96_MICRON,M96_MU_CAP,CPU_1_6GHZ
630-9828	PCBA,MLB,1.6GHZ,MI 2GB,TY CAP,M96	EEE_5P6,M96_COMMON,M96_MICRON,M96_TY_CAP,CPU_1_6GHZ
630-9515	PCBA,MLB,1.8GHZ,MI 2GB,SS CAP,M96	EEE_2AM,M96_COMMON,M96_MICRON,M96_SS_CAP,CPU_1_8GHZ
630-9829	PCBA,MLB,1.8GHZ,MI 2GB,MU CAP,M96	EEE_5P7,M96_COMMON,M96_MICRON,M96_MU_CAP,CPU_1_8GHZ
630-9830	PCBA,MLB,1.8GHZ,MI 2GB,TY CAP,M96	EEE_5P8,M96_COMMON,M96_MICRON,M96_TY_CAP,CPU_1_8GHZ

Bar Code Label / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4DA]	CRITICAL	EEE_4DA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4DB]	CRITICAL	EEE_4DB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AL]	CRITICAL	EEE_2AL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4DC]	CRITICAL	EEE_4DC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AN]	CRITICAL	EEE_2AN
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AP]	CRITICAL	EEE_2AP
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AJ]	CRITICAL	EEE_2AJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AK]	CRITICAL	EEE_2AK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:5P6]	CRITICAL	EEE_5P6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AM]	CRITICAL	EEE_2AM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:5P7]	CRITICAL	EEE_5P7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:5P8]	CRITICAL	EEE_5P8

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M96_COMMON	ALTERNATE,COMMON,M96_COMMON1,M96_COMMON2,M96_COMMON3
M96_COMMON1	MCP_B02,BOOTROM_DEVEL,SMC_PRGRM,BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP,NO_VREFMRGN
M96_COMMON2	LPCPLUS_NOT,LPCPLUS_CONN,XDP
M96_COMMON3	MCP_CS1_NO
M96_HYNIX	DRAM_HYNIX
M96_MICRON	DRAM_MICRON,DRAM_SPD_2
M96_SS_CAP	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF
M96_MU_CAP	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF
M96_TY_CAP	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3658	1	IC,PDC,QS,1.60GHZ,17W,1066,6M	U1000	CRITICAL	CPU_1_6GHZ
337S3659	1	IC,PDC,QS,1.80GHZ,17W,1066,6M	U1000	CRITICAL	CPU_1_8GHZ
338S0604	1	IC,GMCP,MCP79U-A01Q,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_A01Q
338S0601	1	IC,GMCP,MCP79U-B01,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_B01
338S0637	1	IC,GMCP,MCP79U-B02,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_B02
335S0615	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2382	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M96	U6100	CRITICAL	BOOTROM_DEVEL
341S2326	1	IC,EFI,BOOTROM FINAL (LOCKED),M96	U6100	CRITICAL	BOOTROM_FINAL
338S0563	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2327	1	IC,PRGRM,SMC (NEW),M96	U4900	CRITICAL	SMC_PRGRM
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_HYNIX
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_MICRON
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0067	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	
152S0684	152S0421	ALL	1.0UH,22A,10MOHM	
376S0627	376S0723	ALL	POWER NFET, 30V, 18A	
152S0905	152S0861	ALL	IND,IHLP4040CZ,0.68uH,18A	
128S0262	128S0220	ALL	100UF 20% 6.3V BCASE	

CONFIGURATION OPTIONS

SYNC_MASTER=(N/A) SYNC_DATE=(N/A)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

SCALE: NONE SHT 4 OF 71

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	4	CAP, 1UF, 6.3V, 10%, 0402	C7547, C7308, C2564, C2565	CRITICAL	SS_CAP_1UF
138S0629	7	CAP, 1UF, 6.3V, 10%, 0402	C2566, C2567, C2616, C2617, C7298, C7245, C7283	CRITICAL	SS_CAP_1UF
138S0629	9	CAP, 1UF, 6.3V, 10%, 0402	C3000, C2296, C7297, C7493, C7508, C7568, C7631, C8798, C7551	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	4	CAP, 1UF, 6.3V, 10%, 0402	C7547, C7308, C2564, C2565	CRITICAL	MU_CAP_1UF
138S0628	7	CAP, 1UF, 6.3V, 10%, 0402	C2566, C2567, C2616, C2617, C7298, C7245, C7283	CRITICAL	MU_CAP_1UF
138S0628	9	CAP, 1UF, 6.3V, 10%, 0402	C3000, C2296, C7297, C7493, C7508, C7568, C7631, C8798, C7551	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	4	CAP, 1UF, 6.3V, 10%, 0402	C7547, C7308, C2564, C2565	CRITICAL	TY_CAP_1UF
138S0630	7	CAP, 1UF, 6.3V, 10%, 0402	C2566, C2567, C2616, C2617, C7298, C7245, C7283	CRITICAL	TY_CAP_1UF
138S0630	9	CAP, 1UF, 6.3V, 10%, 0402	C3000, C2296, C7297, C7493, C7508, C7568, C7631, C8798, C7551	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240, C1241, C1242, C1243, C1244, C1245, C1246, C1247, C1248, C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250, C1251, C1252, C1253, C1254, C1255, C1256, C1257, C1258, C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260, C1261, C1262, C1263, C1264, C1265, C1266, C1267	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8660, C8661, C8662, C8663, C8664, C8665, C8666, C8667, C8668, C8669	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8610, C8611, C8612, C8613, C8614, C8615, C8616, C8617, C8618, C8619	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8622, C8623, C8624, C8625, C8626, C8627, C8628, C8629	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8630, C8631, C8632, C8633, C8634, C8635, C8636, C8637, C8638, C8639	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209, C1210, C1211	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8640, C8641, C8642, C8643, C8644, C8645, C8646, C8647, C8648, C8649	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8622, C8623, C8624, C8625, C8626, C8627, C8628, C8629	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8642, C8643, C8645, C8646, C8660, C8661, C8662, C8665	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8660, C8661, C8662, C8665, C8610, C8611, C8612, C8613, C8615, C8616	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8624, C8625, C8630, C8631, C8634, C8635, C8640, C8641	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8642, C8643, C8645, C8646, C8660, C8661, C8662, C8665	CRITICAL	SS_CAP_2_2UF
138S0632	7	CAP, 2.2UF, 6.3V, 20%, 0402	C2530, C2531, C2532, C2533, C2534, C2535, C2536	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2568, C2569, C2592, C2593, C2595, C2598, C2662, C2642	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2570, C2571, C2572, C2573, C2574, C2575, C2576, C2610	CRITICAL	SS_CAP_2_2UF
138S0632	3	CAP, 2.2UF, 6.3V, 20%, 0402	C4000, C7302, C7511	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240, C1241, C1242, C1243, C1244, C1245, C1246, C1247, C1248, C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250, C1251, C1252, C1253, C1254, C1255, C1256, C1257, C1258, C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260, C1261, C1262, C1263, C1264, C1265, C1266, C1267	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8660, C8661, C8662, C8663, C8664, C8665, C8666, C8667, C8668, C8669	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8610, C8611, C8612, C8613, C8614, C8615, C8616, C8617, C8618, C8619	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8622, C8623, C8624, C8625, C8626, C8627, C8628, C8629	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8630, C8631, C8632, C8633, C8634, C8635, C8636, C8637, C8638, C8639	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209, C1210, C1211	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8640, C8641, C8642, C8643, C8644, C8645, C8646, C8647, C8648, C8649	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8624, C8625, C8630, C8631, C8634, C8635, C8640, C8641	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8642, C8643, C8645, C8646, C8660, C8661, C8662, C8665	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8660, C8661, C8662, C8665, C8610, C8611, C8612, C8613, C8615, C8616	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8624, C8625, C8630, C8631, C8634, C8635, C8640, C8641	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8642, C8643, C8645, C8646, C8660, C8661, C8662, C8665	CRITICAL	MU_CAP_2_2UF
138S0633	7	CAP, 2.2UF, 6.3V, 20%, 0402	C2530, C2531, C2532, C2533, C2534, C2535, C2536	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2568, C2569, C2592, C2593, C2595, C2598, C2662, C2642	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2570, C2571, C2572, C2573, C2574, C2575, C2576, C2610	CRITICAL	MU_CAP_2_2UF
138S0633	3	CAP, 2.2UF, 6.3V, 20%, 0402	C4000, C7302, C7511	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240, C1241, C1242, C1243, C1244, C1245, C1246, C1247, C1248, C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250, C1251, C1252, C1253, C1254, C1255, C1256, C1257, C1258, C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260, C1261, C1262, C1263, C1264, C1265, C1266, C1267	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8660, C8661, C8662, C8663, C8664, C8665, C8666, C8667, C8668, C8669	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8610, C8611, C8612, C8613, C8614, C8615, C8616, C8617, C8618, C8619	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8622, C8623, C8624, C8625, C8626, C8627, C8628, C8629	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8630, C8631, C8632, C8633, C8634, C8635, C8636, C8637, C8638, C8639	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209, C1210, C1211	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8640, C8641, C8642, C8643, C8644, C8645, C8646, C8647, C8648, C8649	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8624, C8625, C8630, C8631, C8634, C8635, C8640, C8641	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8642, C8643, C8645, C8646, C8660, C8661, C8662, C8665	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8660, C8661, C8662, C8665, C8610, C8611, C8612, C8613, C8615, C8616	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620, C8621, C8624, C8625, C8630, C8631, C8634, C8635, C8640, C8641	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8642, C8643, C8645, C8646, C8660, C8661, C8662, C8665	CRITICAL	TY_CAP_2_2UF
138S0634	7	CAP, 2.2UF, 6.3V, 20%, 0402	C2530, C2531, C2532, C2533, C2534, C2535, C2536	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2568, C2569, C2592, C2593, C2595, C2598, C2662, C2642	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2570, C2571, C2572, C2573, C2574, C2575, C2576, C2610	CRITICAL	TY_CAP_2_2UF
138S0634	3	CAP, 2.2UF, 6.3V, 20%, 0402	C4000, C7302, C7511	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1210, C1211, C1212, C1213, C1214, C1215, C1216, C1217, C1218, C1219	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1220, C1221, C1222, C1223, C1224, C1225, C1226, C1227, C1228, C1230	CRITICAL	SS_CAP_10UF
138S0626	3	CAP, 10UF, 6.3V, 20%, 0603	C1230, C1231, C1300	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4100, C4613, C8660, C7502, C7521, C7650, C7690, C8012	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C7304, C7297, C7509, C7491, C7695	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1210, C1211, C1212, C1213, C1214, C1215, C1216, C1217, C1218, C1219	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1220, C1221, C1222, C1223, C1224, C1225, C1226, C1227, C1228, C1230	CRITICAL	MU_CAP_10UF
138S0625	3	CAP, 10UF, 6.3V, 20%, 0603	C1230, C1231, C1300	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4100, C4613, C8660, C7502, C7521, C7650, C7690, C8012	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C7304, C7297, C7509, C7491, C7695	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1200, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1210, C1211, C1212, C1213, C1214, C1215, C1216, C1217, C1218, C1219	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1220, C1221, C1222, C1223, C1224, C1225, C1226, C1227, C1228, C1230	CRITICAL	TY_CAP_10UF
138S0627	3	CAP, 10UF, 6.3V, 20%, 0603	C1230, C1231, C1300	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4100, C4613, C8660, C7502, C7521, C7650, C7690, C8012	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C7304, C7297, C7509, C7491, C7695	CRITICAL	TY_CAP_10UF

Acoustic Cap BOM Config Tables

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

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SCALE: NONE	SHT 5 OF 71	

Functional Test Points

NB NO_TESTS

These are normally testpoints but become NC

NO_TEST

Power Supply NO_TESTs

NO_TEST

CLOCK NO_TESTS

NO_TEST

LVDS NO_TESTS

NO_TEST

REQUIRED NETS

FUNC TEST - BATTERY CONNECTOR

x2	I647	TRUE	BATT_POS	49
x2	I649	TRUE	GND	
	I638	TRUE	SMC_BS_ALRT_L	39 40 49
	I644	TRUE	SMBUS_SMC_BSA_SCL	39 42 49 58 69
	I639	TRUE	SMBUS_SMC_BSA_SDA	39 42 49 58 69

FUNC TEST - DC-IN CONNECTOR

x6	I648	TRUE	PP18V5_DCIN	49 70
	I655	TRUE	ADAPTER_SENSE	49
x6	I706	TRUE	GND	

FUNC TEST - FAN CONNECTOR

	I668	TRUE	PP5V_S0	6 7 38 41 46 50 57 60 70
	I667	TRUE	FAN_RT_PWM	46
	I669	TRUE	FAN_RT_TACH	46
	I714	TRUE	GND	

FUNC TEST - AIRPORT

I741	TRUE	CK505_SRC_CLKREQ6_L	6
I742	TRUE	PCIE_WAKE_L	6 16 34
I743	TRUE	AIRPORT_RST_L	6 24 34
I744	TRUE	SMBUS_SMC_A_S3_SCL	6 34 38 39 42 69
I745	TRUE	SMBUS_SMC_A_S3_SDA	6 34 38 39 42 69
I746	TRUE	GND	

FUNC TEST - MIC

I747	TRUE	PP3V3_S0_MIC_F	59 70
I748	TRUE	AUD_MIC_DATA_F	59
I749	TRUE	AUD_MIC_CLK_F	59
I750	TRUE	GND_MIC_F	59

FUNC TEST - AUDIO CONNECTOR

I645	TRUE	HDA_SYNC	20 35 68
I646	TRUE	HDA_BIT_CLK	20 35 68
I735	TRUE	AUD_MIC_DATA	35 59
I736	TRUE	HDA_SDOUT	20 35 68
I737	TRUE	PPBUS_G3H	6 7 35 43 44 49 55 58 63 70
I738	TRUE	HDA_SDIN0	20 35 68
I740	TRUE	AUD_MIC_CLK	35 59
I739	TRUE	PM_SLP_S3_L	20 34 35 39 56

FUNC TEST - IPD CONNECTOR

I507	TRUE	SMC_LID	38 39 40
I508	TRUE	PP3V42_G3H_IPD_F	38 70
I509	TRUE	SMC_SYS_KBDLED	38 39
I509	TRUE	SMC_SYS_LED	38 39
I510	TRUE	USB_TPAD_N	8 19 38 68
I512	TRUE	USB_TPAD_P	8 19 38 68
I511	TRUE	SMC_ONOFF_L	6 38 39 40
I513	TRUE	USB_IR_N	6 8 19 38 68
I514	TRUE	USB_IR_P	6 8 19 38 68
I515	TRUE	PP5V_S0_KBDLED_F	6 38 70
I516	TRUE	PP5V_S3_TOPCASE_F	38 70
I517	TRUE	SMBUS_SMC_A_S3_SCL	6 34 38 39 42 69
I518	TRUE	SMBUS_SMC_A_S3_SDA	6 34 38 39 42 69
I524	TRUE	SMC_ONOFF_L	6 38 39 40
I519	TRUE	USB_IR_N	6 8 19 38 68
I527	TRUE	USB_IR_P	6 8 19 38 68
I674	TRUE	PP5V_S0_KBDLED_F	6 38 70
I735	TRUE	LSOC_PRESS_H_R	38

FUNC TEST - M93 WIRELESS CONNECTOR

I478	TRUE	AIRPORT_RST_L	6 24 34
I475	TRUE	PCIE_WAKE_L	6 16 34
I476	TRUE	CK505_SRC_CLKREQ6_L	6
I479	TRUE	PCIE_CLK100M_MINI_N_F	34
I477	TRUE	PCIE_CLK100M_MINI_P_F	34
I478	TRUE	PCIE_E_D2R_N_F	34
I477	TRUE	PCIE_E_D2R_P_F	34
I488	TRUE	PCIE_E_R2D_C_N_F	6 34
I483	TRUE	PCIE_E_R2D_C_P_F	6 34
I484	TRUE	AIRPORT_RST_L	6 24 34
I482	TRUE	SMBUS_SMC_A_S3_SDA	6 34 38 39 42 69
I499	TRUE	SMBUS_SMC_A_S3_SCL	6 34 38 39 42 69
I500	TRUE	PCIE_E_R2D_C_N_F	6 34
I501	TRUE	PCIE_E_R2D_C_P_F	6 34
I502	TRUE	PP3V3_S3_AP_AUX	34 70

NICE2HAVE NETS

FUNC TEST - Power Supplies

	I92	PPVCORE_S0_CPU	7 10 11 50 64 70
	I454	PP0V75_S0	7 33 54 57 70
	I455	PP1V05_S0	23 40 50 57 70
	I457	PP1V5_S0	7 10 11 15 22 56 57 66 70
	I460	PP1V5_S3	7 26 27 28 29 30 31 32 34 54 57 70
	I459	PP1V05_S5	7 21 22 53 57 70
	I458	PPMCPCORE_S0	7 21 22 43 51 70
	I461	PP5V_S0	6 7 38 41 46 50 57 60 70
	I466	PP3V3_S0	6 7 12 22 25 26 36 38 39 40 41 42 53 56 57 59 60 61 62 70
	I463	PP3V3_S3	7 26 27 28 29 30 31 32 34 54 57 70
	I462	PP5V_S3	7 37 38 51 54 55 57
	I467	PP3V3_S5	4 7 37 39 51 53 57
	I468	PP3V42_G3H	4 24 37 39 40 41 49 58 70
	I474	PP18V5_G3H	7 49 70
	I472	PPDCIN_G3H	7 49 70
	I472	PPBUS_G3H	6 7 35 43 44 49 58 63 70
	I474	PPBUS_R_G3H	7 44 50 51 53 54 58 70
	I457	PP1V8_S0	7 17 23 52 70

FUNC TEST - SATA HDD

	I751	TRUE	PP3V3_S0_HDD_F
	I752	TRUE	SATA_HDD_R2D_N
	I753	TRUE	SATA_HDD_R2D_P
	I754	TRUE	SATA_HDD_D2R_C_N
	I755	TRUE	SATA_HDD_D2R_C_P
	I756	TRUE	GND

FUNC TEST - RIO HATCH CONNECTOR

	I716	TRUE	DP_ML_C_N<3..0>
	I717	TRUE	DP_ML_C_P<3..0>
	I718	TRUE	DP_AUX_CH_C_N
	I719	TRUE	DP_AUX_CH_C_P
	I720	TRUE	DP_CA_DET_Q
	I721	TRUE	HDMI_CEC
	I722	TRUE	DP_HPD_Q
	I723	TRUE	PP3V3_S0_DPPWR
	I725	TRUE	USB2_EXTA_F_P
	I726	TRUE	USB2_EXTA_F_N
	I727	TRUE	PP5V_S3_USB2_EXTA_F
	I728	TRUE	GND

FUNC TEST - XDP/ITP CONNECTOR

	I693	TRUE	XDP_BPM_L<0..5>
	I690	TRUE	TP_XDP_OBSFN_B0
	I680	TRUE	TP_XDP_OBSFN_B1
	I681	TRUE	TP_XDP_OBSDATA_B0
	I683	TRUE	TP_XDP_OBSDATA_B1
	I682	TRUE	TP_XDP_OBSDATA_B2
	I684	TRUE	TP_XDP_OBSDATA_B3
	I685	TRUE	XDP_PWRGD
	I687	TRUE	XDP_OBS20
	I686	TRUE	SMBUS_MCP_0_DATA
	I688	TRUE	SMBUS_MCP_0_CLK
	I689	TRUE	XDP_TCK
	I691	TRUE	JTAG_MCP_TDO_CONN
	I692	TRUE	JTAG_MCP_TRST_L
	I702	TRUE	MCP_DEBUG<7..0>
	I694	TRUE	JTAG_MCP_TDI
	I695	TRUE	JTAG_MCP_TMS
	I696	TRUE	FSB_CLK_ITP_P
	I697	TRUE	FSB_CLK_ITP_N
	I698	TRUE	XDP_CPURST_L
	I699	TRUE	XDP_DBRESET_L
	I701	TRUE	XDP_TDO_CONN
	I700	TRUE	XDP_TRST_L
	I702	TRUE	XDP_TDI
	I703	TRUE	XDP_TMS
	I704	TRUE	PP3V3_S0
	I705	TRUE	PP1V05_S0

FUNC TEST - CAMERA USB, LVDS, ALS

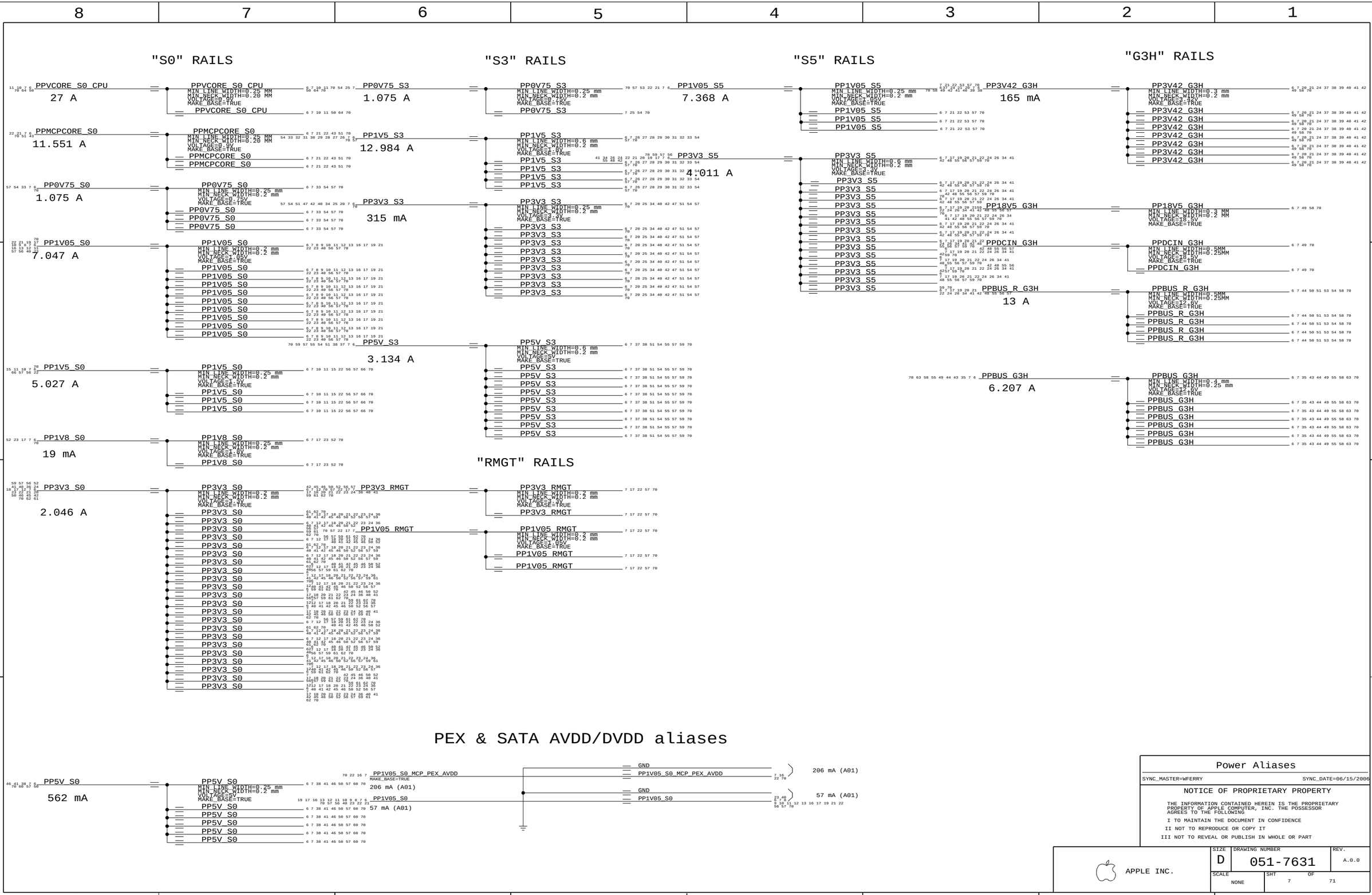
x2	I654	TRUE	PP5V_S3_CAMERA_F
	I655	TRUE	USB2_CAMERA_F_P
	I656	TRUE	USB2_CAMERA_F_N
	I657	TRUE	LCDBKLT_RTN<1..6>
	I658	TRUE	LVDS_IG_A_DATA_N<0..2>
	I659	TRUE	LVDS_IG_A_DATA_P<0..2>
	I660	TRUE	PPVOUT_S0_LCDBKLT
	I661	TRUE	LVDS_IG_A_CLK_F_N
	I662	TRUE	LVDS_IG_A_CLK_F_P
	I663	TRUE	LVDS_IG_DDC_CLK
	I664	TRUE	LVDS_IG_DDC_DATA
	I665	TRUE	PP3V3_S0_LCD_F
x2	I666	TRUE	PP3V3_LCDVDD_SW_F
	I711	TRUE	SMBUS_SMC_MGMT_SDA
	I712	TRUE	SMBUS_SMC_MGMT_SCL
x10	I713	TRUE	GND

x13 I822 TRUE GND

Functional Test and No-Tests

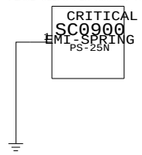
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 6 OF 71	



EMI SPRING CLIPS

PLACE CLIPS PER MCO ON TOPSIDE NEAR BATTERY CONNECTOR J6900



BOSSES

Z0900 4.5OD2.0H-M1.6X0.35
Z0901 4.5OD2.0H-M1.6X0.35
Z0902 4.5OD2.0H-M1.6X0.35
Z0903 4.5OD2.0H-M1.6X0.35
Z0904 4.5OD2.0H-M1.6X0.35

STANDOFFS

Z0910 STDOFF-4.0OD2.4H-0.5-THNP
Z0911 STDOFF-4.0OD2.4H-0.5-THNP
Z0912 STDOFF-4.0OD2.4H-0.5-THNP

SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

		NO_TEST	
NC_SMC_PA0	NC_SMC_PA0	TRUE	MAKE_BASE=TRUE
NC_SMC_PA1	NC_SMC_PA1	TRUE	MAKE_BASE=TRUE
NC_ESTARLDO_EN	NC_ESTARLDO_EN	TRUE	MAKE_BASE=TRUE
NC_SMC_P26	NC_SMC_P26	TRUE	MAKE_BASE=TRUE
NC_SMC_P41	NC_SMC_P41	TRUE	MAKE_BASE=TRUE
NC_SMC_P67	NC_SMC_P67	TRUE	MAKE_BASE=TRUE
NC_SMC_GFX_OVERTEMP_L	NC_SMC_GFX_OVERTEMP_L	TRUE	MAKE_BASE=TRUE
NC_EXCARD_OC_L	NC_EXCARD_OC_L	TRUE	MAKE_BASE=TRUE
NC_SMC_P24	NC_SMC_P24	TRUE	MAKE_BASE=TRUE
NC_SMC_EXCARD_CP	NC_SMC_EXCARD_CP	TRUE	MAKE_BASE=TRUE
NC_ALS_RIGHT	NC_ALS_RIGHT	TRUE	MAKE_BASE=TRUE
NC_ALS_GAIN	NC_ALS_GAIN	TRUE	MAKE_BASE=TRUE
NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	TRUE	MAKE_BASE=TRUE
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	TRUE	MAKE_BASE=TRUE
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	TRUE	MAKE_BASE=TRUE
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	TRUE	MAKE_BASE=TRUE
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	TRUE	MAKE_BASE=TRUE
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	TRUE	MAKE_BASE=TRUE
NC_SMC_RSTGATE_L	NC_SMC_RSTGATE_L	TRUE	MAKE_BASE=TRUE
NC_ISENSE_CAL_EN	NC_ISENSE_CAL_EN	TRUE	MAKE_BASE=TRUE
NC_SMC_FWE	NC_SMC_FWE	TRUE	MAKE_BASE=TRUE
NC_SMC_ANALOG_ID	NC_SMC_ANALOG_ID	TRUE	MAKE_BASE=TRUE
NC_ALS_LEFT	NC_ALS_LEFT	TRUE	MAKE_BASE=TRUE
NC_SMC_NB_DDR_ISENSE	NC_SMC_NB_DDR_ISENSE	TRUE	MAKE_BASE=TRUE
NC_SMC_P10	NC_SMC_P10	TRUE	MAKE_BASE=TRUE
NC_SMC_PA5	NC_SMC_PA5	TRUE	MAKE_BASE=TRUE
NC_SMC_GPU_ISENSE	NC_SMC_GPU_ISENSE	TRUE	MAKE_BASE=TRUE

SMC_IG_THROTTLE_L — SMC_IG_THROTTLE_L
SMC_SMS_INT_L — SMC_SMS_INT_L
SMC_ADAPTER_EN — SMC_ADAPTER_EN

PCI-E ALIASES

UNUSED GPU LANES

NC_PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
NC_PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
NC_PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
NC_PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE MAKE_BASE=TRUE
TP_PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
TP_PEG_CLKREQ_L	TP_PEG_CLKREQ_L	MAKE_BASE=TRUE
TP_PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
TP_PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE
TP_EXTGPU_PWR_EN	TP_EXTGPU_PWR_EN	MAKE_BASE=TRUE
TP_EXTGPU_RESET_L	TP_EXTGPU_RESET_L	MAKE_BASE=TRUE

AIRPORT CARD AND TURBOMEM PRESENT SIGNAL

GND — GND — MAKE_BASE=TRUE

HDA PULL-DOWN

UNUSED IPHS SIGNAL(FOR IPHONE JACK)

AUD_IPHS_SWITCH_EN

AUD_I2C_INT_L IS PU ON MCP PAGE

R0920 100K 5% 1/20W MF 201

DP HOTPLUG PULL-DOWN

HPLUG_DET2 — HPLUG_DET2 MAKE_BASE=TRUE

R0940 20K 5% 1/20W MF 201

LAN ALIASES

UNUSED ETHERNET RG/MII INTERFACE

ENET_RXD<0>
ENET_RXD<1>
ENET_RXD<2>
ENET_RXD<3>
ENET_MDIO
ENET_RX_CTRL
ENET_CLK125M_TXCLK
MCP_MII_VREF
ENET_CLK125M_RXCLK
ENET_INTR_L

RP0930 10K 5% 1/32W 4X0201-HF
RP0931 10K 5% 1/32W 4X0201-HF
RP0932 10K 5% 1/32W 4X0201-HF

NC_ENET_RESET_L	NC_ENET_RESET_L	MAKE_BASE=TRUE
NC_MCP_CLK25M_BUF0_R	NC_MCP_CLK25M_BUF0_R	MAKE_BASE=TRUE
NC_ENET_PWRDWN_L	NC_ENET_PWRDWN_L	MAKE_BASE=TRUE
NC_ENET_MDC	NC_ENET_MDC	MAKE_BASE=TRUE
NC_ENEX_TX_CTRL	NC_ENEX_TX_CTRL	MAKE_BASE=TRUE
ENET_TXD<3..0>	NC_ENET_TXD<3..0>	MAKE_BASE=TRUE

GND — VOLTAGE=0V MIN_NECK_WIDTH=0.20 MM MIN_LINE_WIDTH=0.38 MM

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

NC_MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE MAKE_BASE=TRUE
NC_MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE MAKE_BASE=TRUE
NC_MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE MAKE_BASE=TRUE
NC_MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE MAKE_BASE=TRUE
NC_CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE MAKE_BASE=TRUE
NC_CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE MAKE_BASE=TRUE
NC_CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE MAKE_BASE=TRUE
NC_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE MAKE_BASE=TRUE
NC_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

NC_LVDS_IG_A_DATA_P3	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE MAKE_BASE=TRUE
NC_LVDS_IG_A_DATA_N3	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE MAKE_BASE=TRUE
NC_LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE MAKE_BASE=TRUE
NC_LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE MAKE_BASE=TRUE
NC_LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE MAKE_BASE=TRUE
NC_LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE MAKE_BASE=TRUE

MISC NC MCP79 ALIASES

TP_CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
TP_FW_PME_L	TP_FW_PME_L	MAKE_BASE=TRUE
TP_ODD_PWR_EN_L	TP_ODD_PWR_EN_L	MAKE_BASE=TRUE

SATA ALIASES

UNUSED SATA ODD SIGNALS

TP_SATA_ODD_R2D_C_P	TP_SATA_ODD_R2D_C_P	MAKE_BASE=TRUE
TP_SATA_ODD_R2D_C_N	TP_SATA_ODD_R2D_C_N	MAKE_BASE=TRUE
TP_SATA_ODD_D2R_P	TP_SATA_ODD_D2R_P	MAKE_BASE=TRUE
TP_SATA_ODD_D2R_N	TP_SATA_ODD_D2R_N	MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

TP_USB_EXTB_P	TP_USB_EXTB_P	MAKE_BASE=TRUE
TP_USB_EXTB_N	TP_USB_EXTB_N	MAKE_BASE=TRUE
TP_USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
TP_USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
TP_USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
TP_USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
TP_USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
TP_USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE

EXTERNAL PORT A

USB_EXTA_P	USB_EXTA_P	MAKE_BASE=TRUE
USB_EXTA_N	USB_EXTA_N	MAKE_BASE=TRUE
USB_EXTA_OC_L	USB_EXTA_OC_L	MAKE_BASE=TRUE

CAMERA

USB_CAMERA_P	USB_CAMERA_P	MAKE_BASE=TRUE
USB_CAMERA_N	USB_CAMERA_N	MAKE_BASE=TRUE

TRACKPAD(WELLSPRING)

USB_TPAD_P	USB_TPAD_P	MAKE_BASE=TRUE
USB_TPAD_N	USB_TPAD_N	MAKE_BASE=TRUE

IR

USB_IR_P	USB_IR_P	MAKE_BASE=TRUE
USB_IR_N	USB_IR_N	MAKE_BASE=TRUE

BT (M93)

USB_BT_P	USB_BT_P	MAKE_BASE=TRUE
USB_BT_N	USB_BT_N	MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

CPU_BSEL<0:2> — CPU_BSEL<0:2> MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

PP1V05_S0

R0995 220 5% 1/20W MF 201 — NO STUFF
R0997 200 5% 1/20W MF 201 — NO STUFF
R0999 150 5% 1/20W MF 201 — NO STUFF
R0996 62 5% 1/20W MF 201 — NO STUFF
R0998 150 5% 1/20W MF 201 — NO STUFF

CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI

MEM ALIASES

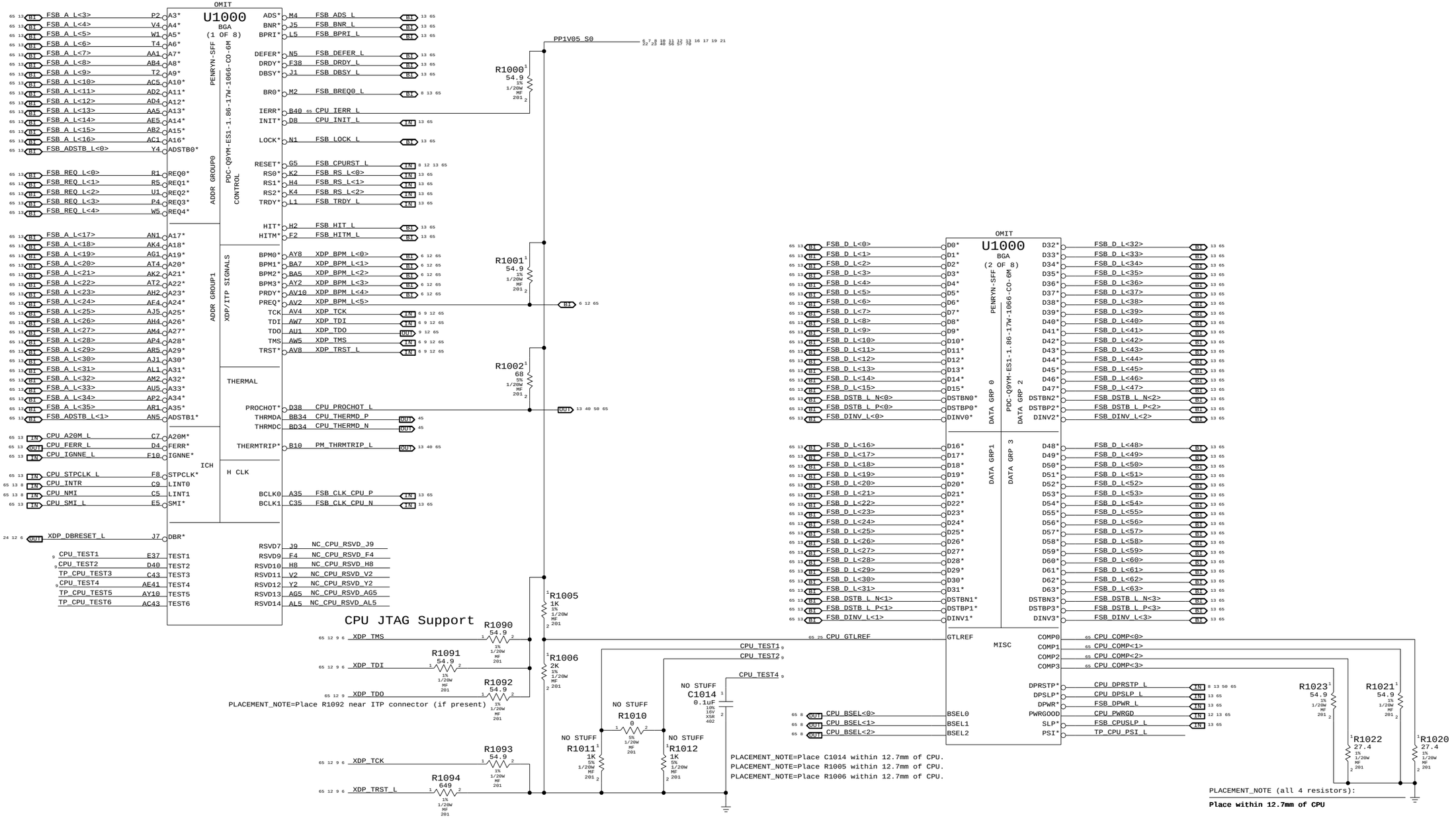
		NO_TEST	
NC_MEM_A_CLK4P	NC_MEM_A_CLK4P	TRUE	MAKE_BASE=TRUE
NC_MEM_A_CLK4N	NC_MEM_A_CLK4N	TRUE	MAKE_BASE=TRUE
NC_MEM_A_CLK3P	NC_MEM_A_CLK3P	TRUE	MAKE_BASE=TRUE
NC_MEM_A_CLK3N	NC_MEM_A_CLK3N	TRUE	MAKE_BASE=TRUE
NC_MEM_A_CS_L<2>	NC_MEM_A_CS_L<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CS_L<3>	NC_MEM_A_CS_L<3>	TRUE	MAKE_BASE=TRUE
NC_MEM_A_CKE<2>	NC_MEM_A_CKE<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CKE<3>	NC_MEM_A_CKE<3>	TRUE	MAKE_BASE=TRUE
NC_MEM_B_CLK4P	NC_MEM_B_CLK4P	TRUE	MAKE_BASE=TRUE
NC_MEM_B_CLK4N	NC_MEM_B_CLK4N	TRUE	MAKE_BASE=TRUE
NC_MEM_B_CLK3P	NC_MEM_B_CLK3P	TRUE	MAKE_BASE=TRUE
NC_MEM_B_CLK3N	NC_MEM_B_CLK3N	TRUE	MAKE_BASE=TRUE
NC_MEM_B_CS_L<2>	NC_MEM_B_CS_L<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CS_L<3>	NC_MEM_B_CS_L<3>	TRUE	MAKE_BASE=TRUE
NC_MEM_B_ODT<2>	NC_MEM_B_ODT<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_ODT<3>	NC_MEM_B_ODT<3>	TRUE	MAKE_BASE=TRUE
NC_MEM_B_CKE<2>	NC_MEM_B_CKE<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CKE<3>	NC_MEM_B_CKE<3>	TRUE	MAKE_BASE=TRUE

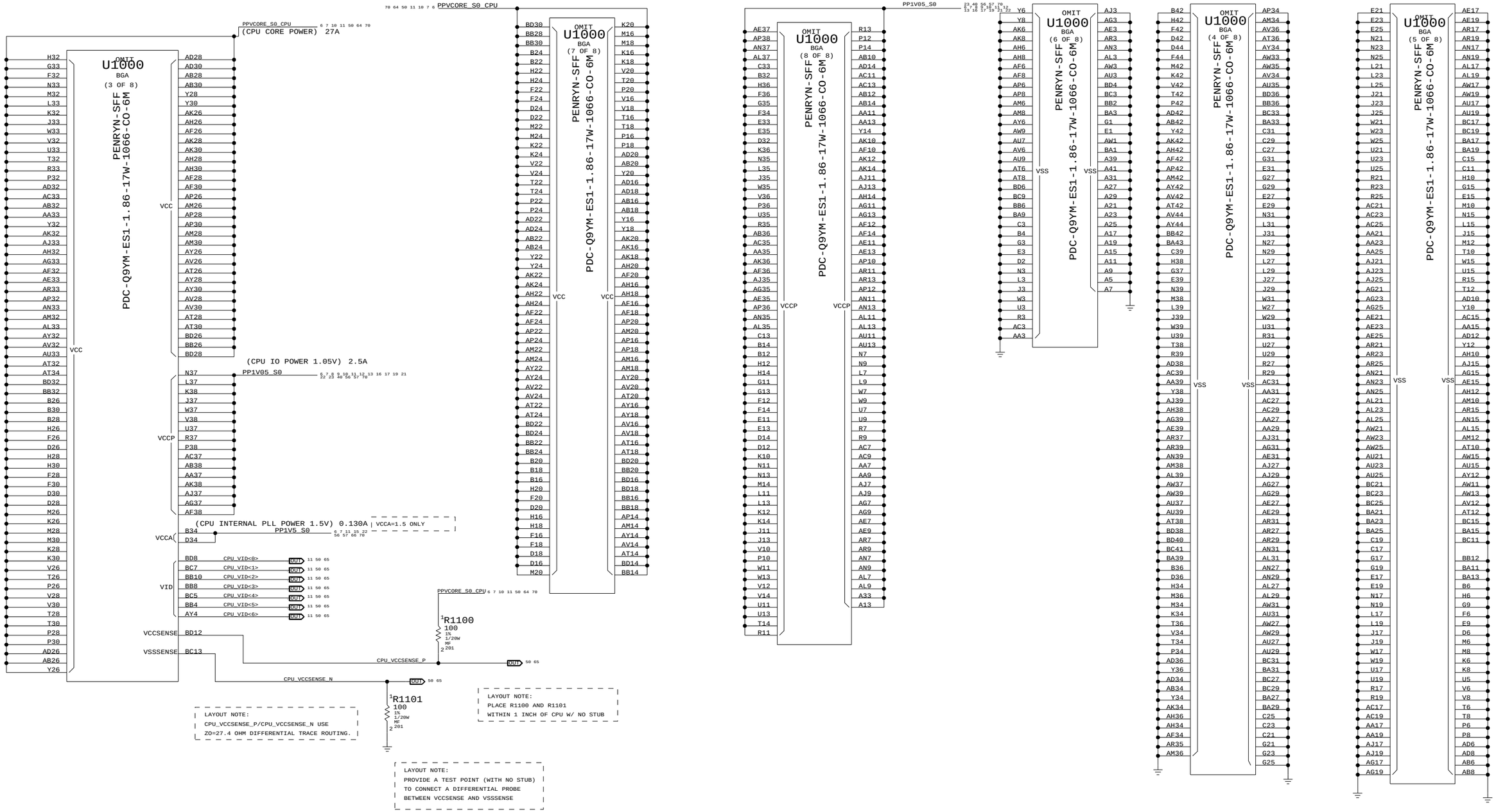
SIGNAL ALIAS /RESET

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT: 8 OF 71	





CPU Power & Ground

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE: NONE	SHT 10 OF 71	

CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

70 64 50 10 7 6 PPVCORE_S0_CPU

10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1200 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1201 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1202 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1203 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1204 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1205 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1206 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1207 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1208 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1209 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1210 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1211 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1212 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1213 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1214 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1215 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1216 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1217 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1218 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1219 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1220 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1221 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1222 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1223 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1224 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1225 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1226 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1227 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1228 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1229 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1230 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1231 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1240 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1241 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1242 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1243 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1244 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1245 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1246 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1247 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1248 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1249 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1250 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1251 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1252 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1253 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1254 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1255 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1256 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1257 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1258 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1259 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1260 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1261 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1262 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1263 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1264 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1265 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1266 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1267 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 330UF 20% 2.0V POLY-TANT D2T-SM1
CRITICAL C1271 330UF 20% 2.0V POLY-TANT D2T-SM1

CRITICAL C1272 330UF 20% 2.0V POLY-TANT D2T-SM1

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

Intel recommends 3x220UF @ 9mOHM

CPU VCORE VID CONNECTIONS

65 50 10 CPU_VID<0..6> → IMVP6_VID<0..6> 65
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

70 66 57 56 22 15 10 7 6 PP1V5_S0

1x 10uF, 1x 0.01uF

C1280 10UF 20% 6.3V X5R 603
C1281 0.01UF 10% 10V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

21 19 17 16 13 12 10 9 8 7 6 PP1V05_S0
70 67 66 40 23 22

1X 330UF, 12X 2.2UF

C1283 C1284 C1285 C1286 C1287 C1288 2.2UF 20% 6.3V CERM OMIT 402-LF

CRITICAL C1290 330UF 20% 2.5V POLY-TANT CASE-C2-SM

C1291 C1292 C1293 C1294 C1295 C1296 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

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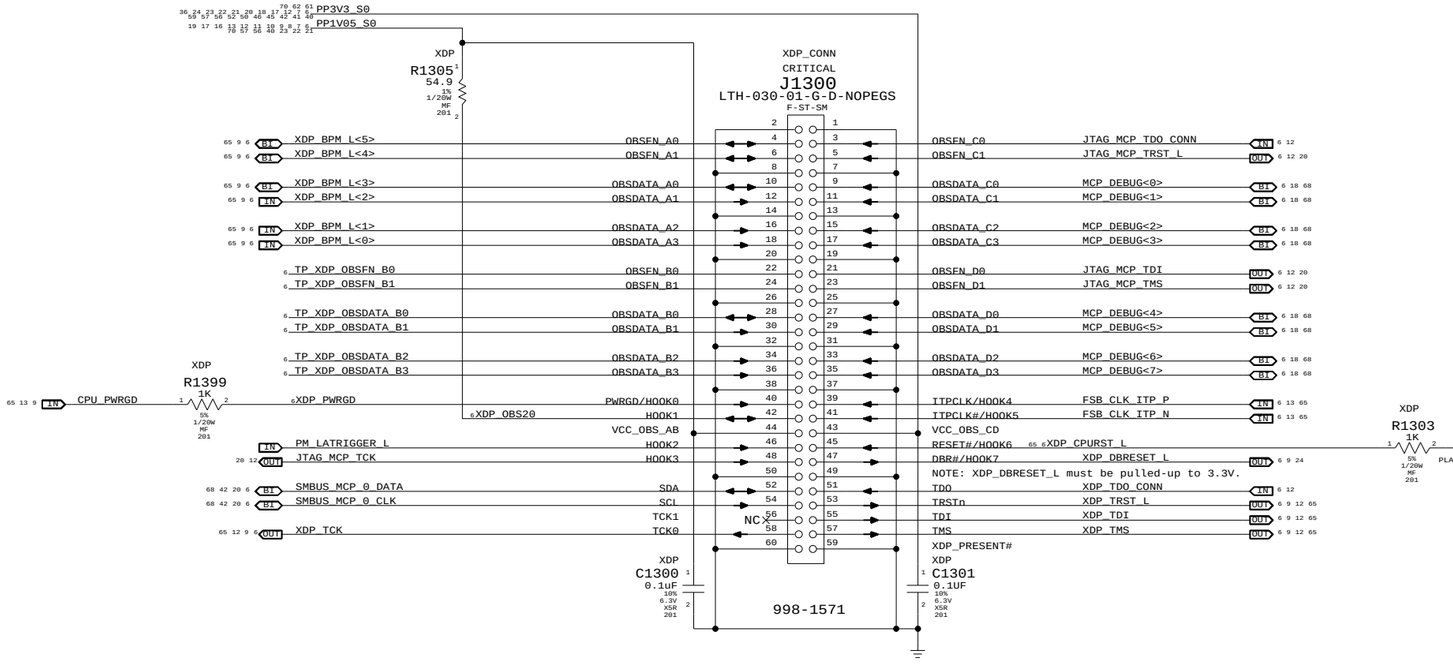
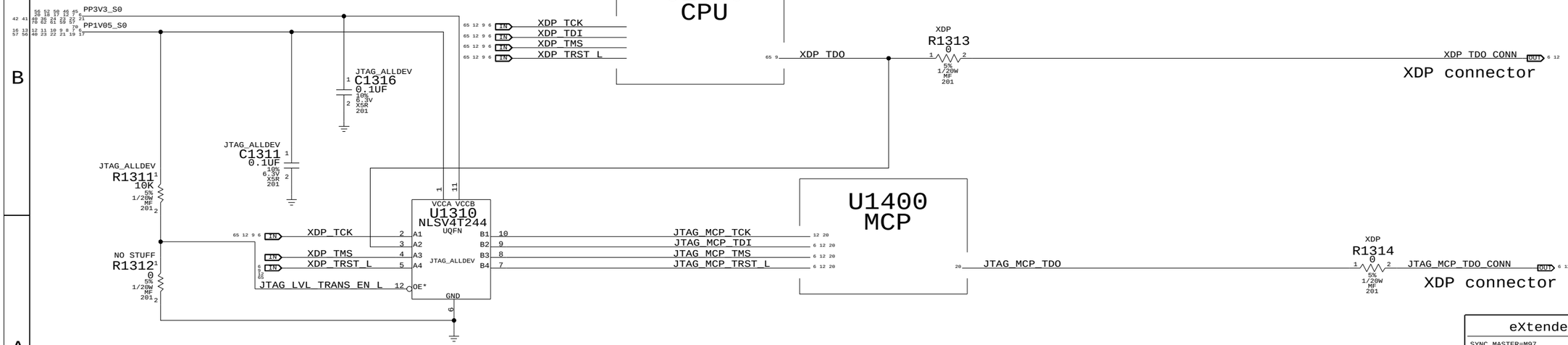
SCALE: NONE SHT 11 OF 71

MCP79-specific pinout



From XDP connector



eXtended Debug Port (XDP)

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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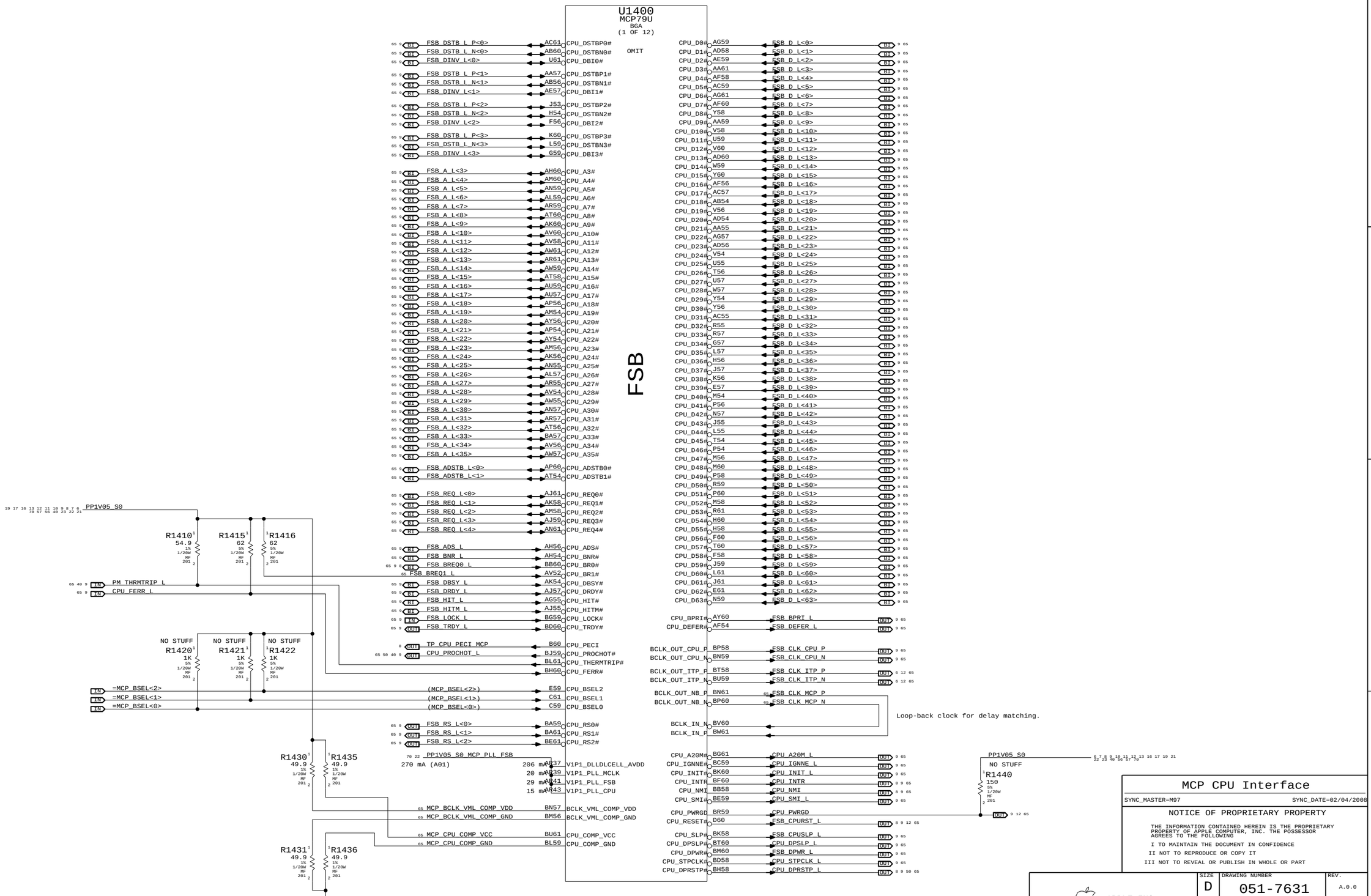

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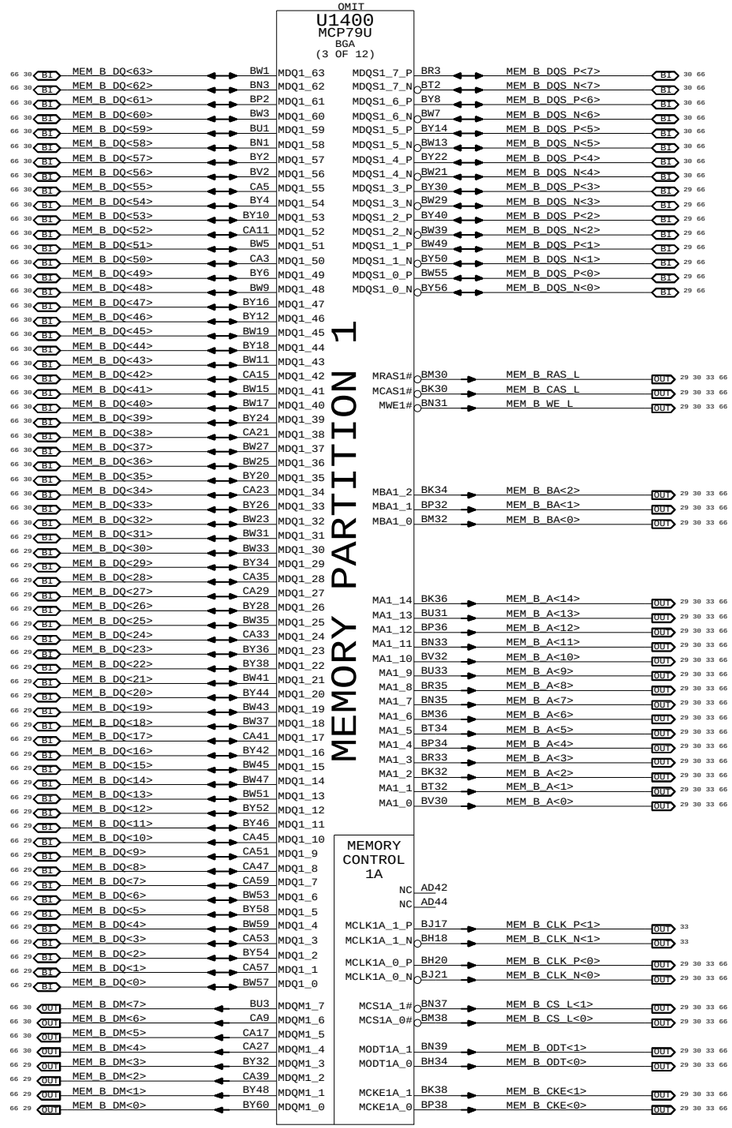

MCP Memory Interface

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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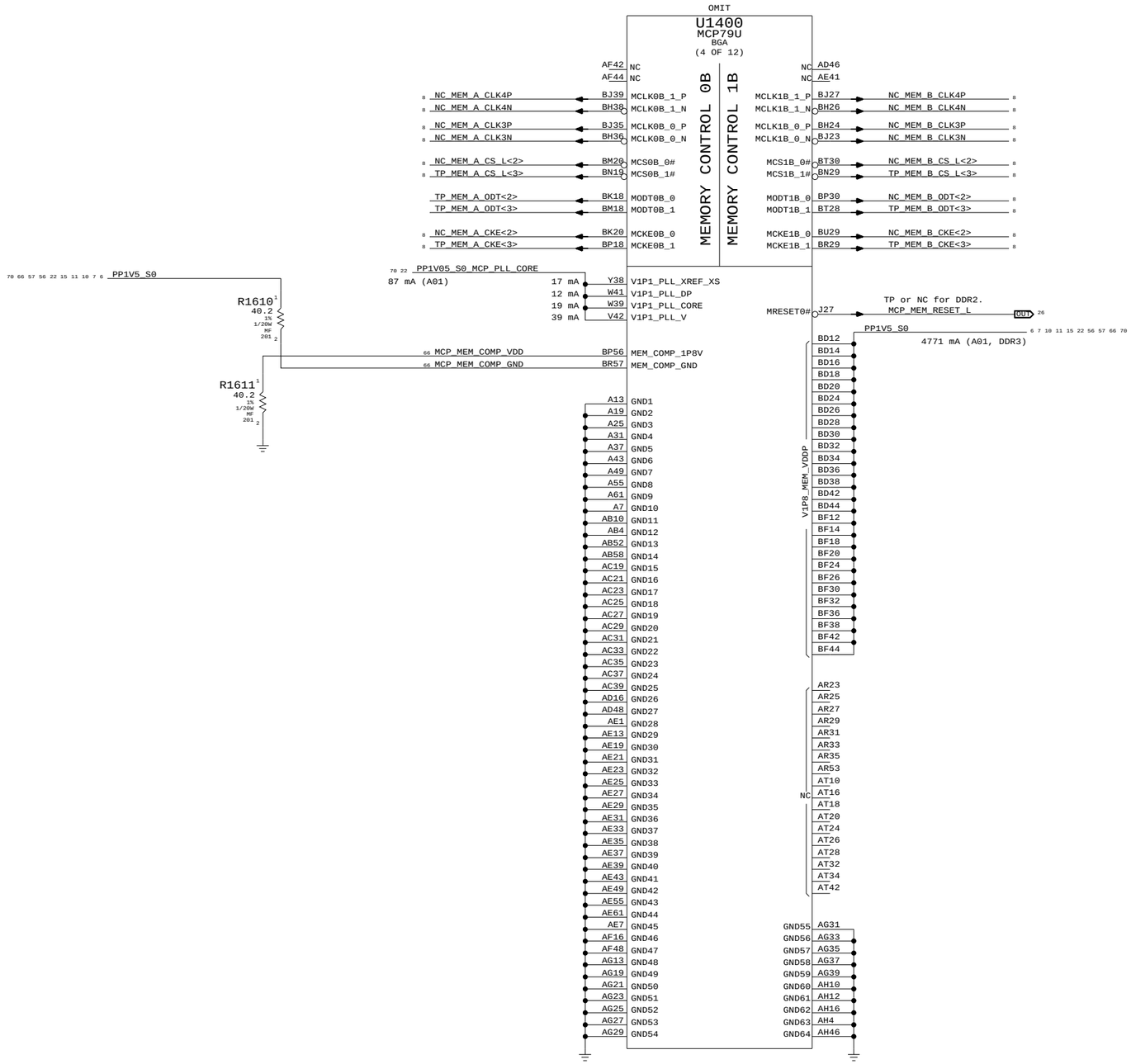

MCP Memory Misc

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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D	051-7631	A.0.0

SCALE	SHT	OF
NONE	15	71

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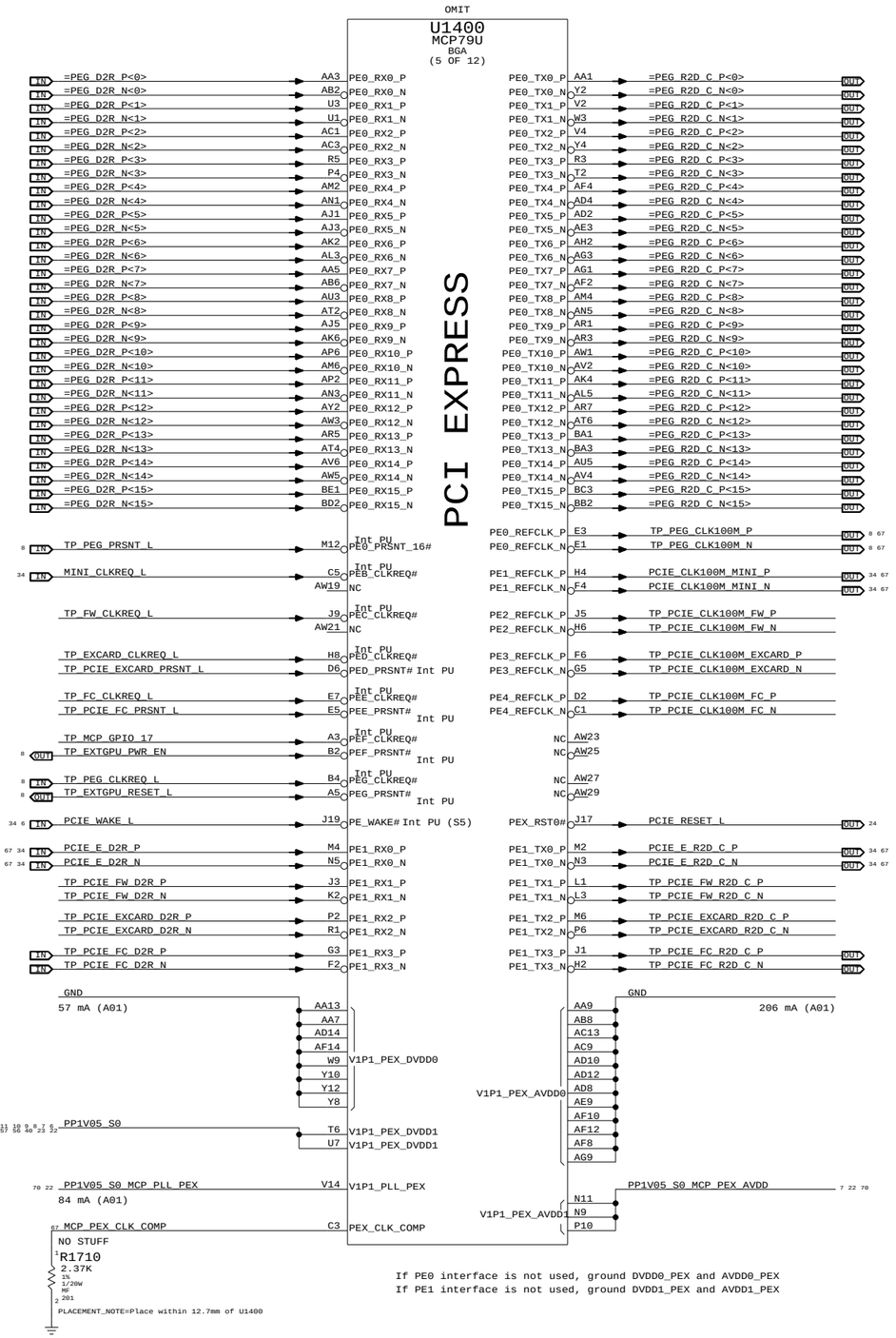

MCP PCIe Interfaces

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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D	051-7631	A.0.0
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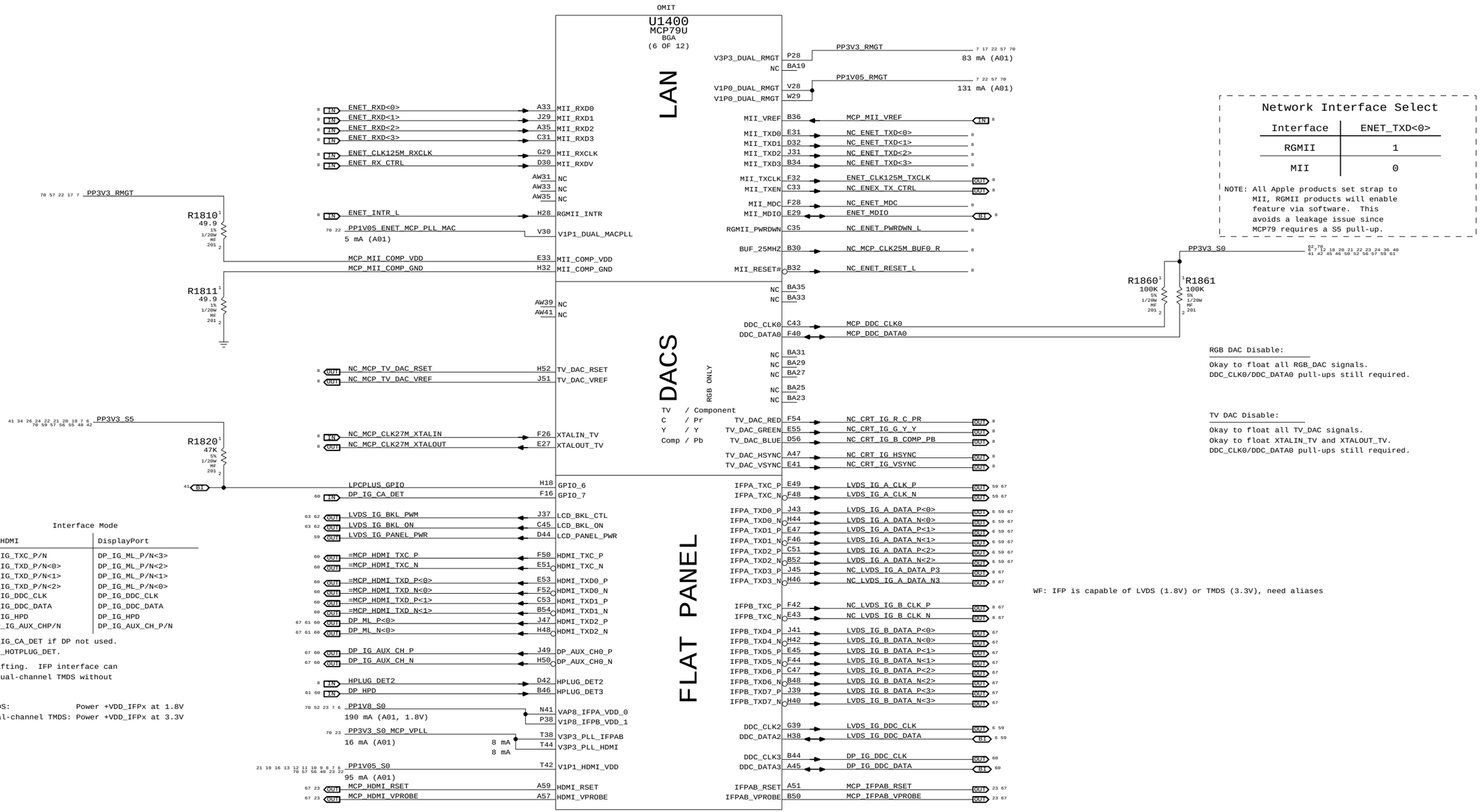

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MCP Ethernet & Graphics

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 17 OF 71	

OMIT

U1400
MCP79U
BGA
(7 OF 12)

PCI

68 18	PCI_REQ0_L	AJ9	PCI_REQ0#		
68 18	PCI_REQ1_L	AD6	PCI_REQ1#		
18 OUT	CRTMUX_SEL_TV_L	AH6	PCI_REQ2#		
8 OUT	AUD_IPHS_SWITCH_EN	AP8	PCI_REQ3#		
18 IN	MCP_RS232_SIN_L	AC5	PCI_REQ4#		
68 12 6 BI	MCP_DEBUG<0>	BC5	PCI_AD0	NC	BE57
68 12 6 BI	MCP_DEBUG<1>	BK4	PCI_AD1	NC	BE9
68 12 6 BI	MCP_DEBUG<2>	BE5	PCI_AD2	PCI_GNT2#	AE5 → TP_LVDSMUX_SEL_IG_L OUT
68 12 6 BI	MCP_DEBUG<3>	BH4	PCI_AD3	PCI_GNT3#	AC7 → TP_DPMUX_SEL_IG_L OUT
68 12 6 BI	MCP_DEBUG<4>	BE3	PCI_AD4	PCI_GNT4#	AF6 → MCP_RS232_SOUT_L OUT 18
68 12 6 BI	MCP_DEBUG<5>	BA5	PCI_AD5		BE53
68 12 6 BI	MCP_DEBUG<6>	BJ3	PCI_AD6		BD8
68 12 6 BI	MCP_DEBUG<7>	BJ5	PCI_AD7		BD56
		BC53			BD52
		BB8			BD48
		BB6			BC57
		BB56		NC	BC9
		BB54			BD50
		BB52			BD54
		BB50			BD6
		BB48			BE49
		BB46			BE55
		BB44			BA53
		BB42			
		BB38			
		BB36			
		BB34			
		BB32	NC		
		BB30			
		BB28			
		BB26			
		BB24			
		BB20			
		BB10			
		BA9			
		BA7			
		BA55			
		BA49			
		BA43			
		BA41			
		BA39			

FIXME: USED TO BE PM_LATRIGGER_L

Int PU (S5)

PCI_RESET0#	G17	MEM_VTT_EN_R OUT 24			
PCI_RESET1#	G21	TP_PCI_RESET1_L			
PCI_CLK0	AM10	TP_PCI_CLK0			
NC	BE7				
PCI_CLK2	AG5	68 PCI_CLK33M_MCP_R			
PCI_CLKIN	AG7	68 PCI_CLK33M_MCP			

R1910 22 5% 1/20W MF 201
PLACEMENT_NOTE=Place close to pin R8

LPC

41 39 IN	PM_CLKRUN_L	AH8	PCI_CLKRUN#		
8	TP_FW_PME_L	AN9	LPC_DRQ1# Int PU		
	TP_LPC_DRQ0_L	AN7	LPC_DRQ0# Int PU		
41 39 BI	LPC_SERIRQ	AT8	LPC_SERIRQ Int PU		
LPC_FRAME#	AJ7	41 LPC_FRAME_R_L	R1960 22 5% 1/20W MF 201	LPC_FRAME_L	OUT 39 41 68
LPC_PWRDWN#	AL9	LPC_PWRDWN_L			OUT 39 41
LPC_RESET0#	E17	LPC_RESET_L			OUT 24 68
LPC_AD0	AM8	LPC_AD_R<0>	R1961 22 5% 1/20W MF 201	LPC_AD<0>	BI 39 41 68
LPC_AD1	AK8	LPC_AD_R<1>	R1962 22 5% 1/20W MF 201	LPC_AD<1>	BI 39 41 68
LPC_AD2	AK10	LPC_AD_R<2>	R1963 22 5% 1/20W MF 201	LPC_AD<2>	BI 39 41 68
LPC_AD3	AR9	LPC_AD_R<3>	R1964 22 5% 1/20W MF 201	LPC_AD<3>	BI 39 41 68
LPC_CLK0	BB4	LPC_CLK33M_SMC_R			OUT 24 68

R1965 10K 5% 1/20W MF 201

Strap for Boot ROM Selection (See HDA_SDOUT)

GND

AH48	GND65	GND98	AL7
AH52	GND66	GND99	AM16
AH58	GND67	GND100	AM48
AJ19	GND68	GND101	AN13
AJ21	GND69	GND102	AN19
AJ23	GND70	GND103	AN21
AJ25	GND71	GND104	AN23
AJ27	GND72	GND105	AN25
AJ29	GND73	GND106	AN27
AJ31	GND74	GND107	AN29
AJ33	GND75	GND108	AN31
AJ35	GND76	GND109	AN33
AJ37	GND77	GND110	AN35
AJ39	GND78	GND111	AN37
AK16	GND79	GND112	AN39
AK48	GND80	GND113	AN53
AL1	GND81	GND114	AP10
AL13	GND82	GND115	AP12
AL19	GND83	GND116	AP16
AL21	GND84	GND117	AP4
AL23	GND85	GND118	AP42
AL25	GND86	GND119	AP44
AL27	GND87	GND120	AP46
AL29	GND88	GND121	AP48
AL31	GND89	GND122	AP52
AL33	GND90	GND123	AP58
AL35	GND91	GND124	AT14
AL37	GND92	GND125	AT30
AL39	GND93	GND126	AT36
AL43	GND94	GND127	AT38
AL49	GND95	GND128	AT48
AL55	GND96	GND129	AU1
AL61	GND97	GND130	AU13

PP3V3_S0

18	MCP_RS232_SOUT_L	RP1900	8.2K	3	6
68 18	PCI_REQ0_L	RP1900	8.2K	4	5
68 18	PCI_REQ1_L	RP1901	8.2K	1	8
18	CRTMUX_SEL_TV_L	RP1901	8.2K	2	7
18	MCP_RS232_SIN_L	RP1901	8.2K	4	5

5% 1/32W 4X0201-HF

FIXME: ADJUST PINOUT PER LAYOUT

MCP PCI & LPC

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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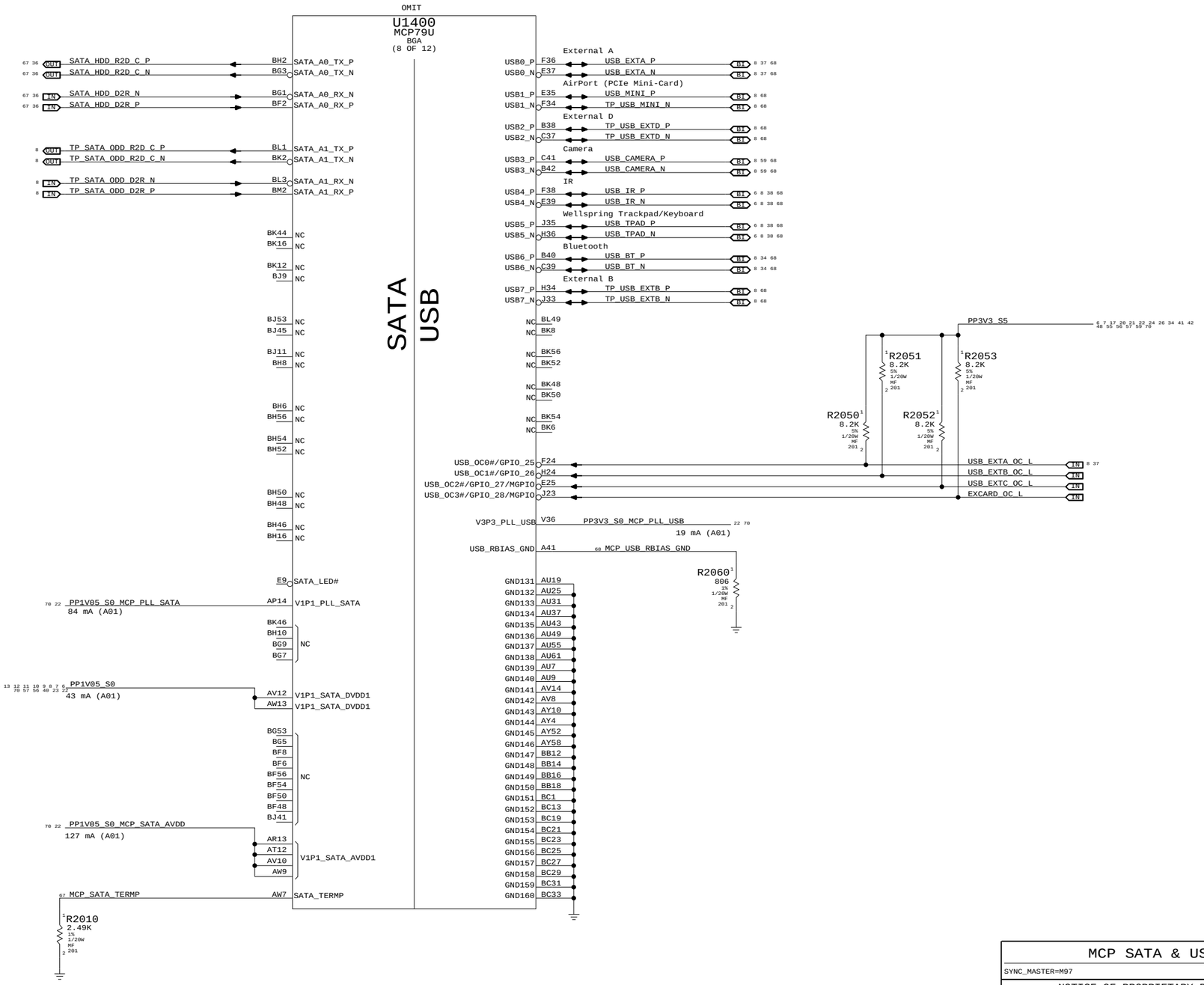

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MCP SATA & USB

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	19	71

OMIT

U1400
MCP79U
BGA
(9 OF 12)

HDA

HDA_SDIN0 — F14 HDA_SDATA_IN0 (Int PD)
MLB_RAM_SIZE_0 — J15 GPIO_2 (Int PD)
MLB_RAM_VENDOR_0 — B14 GPIO_3 (Int PD)
PP3V3_S0 — R2110 49.9 1% 1/20W MF 201 — MCP_HDA_PULLDN_COMP — B12 HDA_PULLDN_COMP
PP1V05_S0_MCP_PLL_NV — 37 mA (A01) — AP20 V1P1_PLL_NV_H (20 mA) — AP18 V1P1_PLL_SP_SPREF (17 mA)

V3P3_DUAL_HDA P20
V3P3_DUAL_HDA T20
PP3V3_S0 — R2160 8.2K 5% 1/20W MF 201 — 7 mA (A01)

HDA_SDATA_OUT H14 — HDA_SDOUT_R — R2170 22 — HDA_SDOUT
HDA_BITCLK C13 — HDA_BIT_CLK_R — R2171 22 — HDA_BIT_CLK
HDA_RESET# A11 — HDA_RST_R_L — R2172 22 — HDA_RST_L
HDA_SYNC E13 — HDA_SYNC_R — R2173 22 — HDA_SYNC

MISC

PP3V42_G3H — R2120 49.9K 1% 1/20W MF 201 — R2121 49.9K 1% 1/20W MF 201

SPI_CS1_R_L_USE_MLB — C21 GPIO_1
SMC_ADAPTER_EN — J25 GPIO_12
TP_SB_A20GATE — B6 A20GATE (Int PU)
TP_MCP_KBDRSTIN_L — C7 KBRDRSTIN# (Int PU)
SMC_WAKE_SCI_L — C23 SIO_PME# (Int PU (S5))
SMC_RUNTIME_SCI_L — F20 EXT_SMI/GPIO_32# (Int PU (S5))
SM_INTRUDER_L — C29 INTRUDER#
TP_MCP_LID_L — A27 LID# (Int PU (S5))
PM_BATLOW_L — B20 LLB# (Int PU (S5))
PM_DPRSLPVR — D12 CPU_DPRSLPVR
PM_PWRBTN_L — F18 PWRBTN# (Int PU (S5))
PM_SYSRST_DEBOUNCE_L — D18 RSTBTN# (Int PU)
RTC_RST_L — A29 RTC_RST#
PM_RSMRST_L — G27 PWRGD_SB
MCP_PS_PWRGD — A23 PS_PWRGD
MCP_CPU_VLD — D20 CPU_VLD
JTAG_MCP_TDI — J21 JTAG_TDI (Int PU)
JTAG_MCP_TDO — B22 JTAG_TDO
JTAG_MCP_TMS — F22 JTAG_TMS (Int PU)
JTAG_MCP_TRST_L — E21 JTAG_TRST#
JTAG_MCP_TCK — H22 JTAG_TCK
MCP_CLK25M_XTALIN — B26 XTALIN
MCP_CLK25M_XTALOUT — C25 XTALOUT
RTC_CLK32K_XTALIN — B28 XTALIN_RTC
RTC_CLK32K_XTALOUT — C27 XTALOUT_RTC

R2151 100K 5% 1/20W MF 201
R2150 10K 5% 1/20W MF 201

GPIO_4 B16 — MCP_GPIO_4 — OUT 20
GPIO_5 D14 — AUD_I2C_INT_L — IN 20
SLP_S3# C19 — PM_SLP_S3_L — OUT 6 34 35 39 56
SLP_RMGT# H16 — PM_SLP_RMGT_L — OUT 57
SLP_S5# C17 — PM_SLP_S4_L — OUT 34 39 40 56
THERM_DIODE_P E11 — MCP_THMDIODE_P — OUT 45
THERM_DIODE_N G11 — MCP_THMDIODE_N — OUT 45
GPIO_13 B8 — MCP_VID<0> — OUT 20 51
GPIO_14 F12 — MCP_VID<1> — OUT 20 51
GPIO_15 C11 — MCP_VID<2> — OUT 20 51
SPKR H12 — MCP_SPKR
SMB_CLK0 A17 — SMBUS_MCP_0_CLK — OUT 6 12 42 68
SMB_DATA0 B18 — SMBUS_MCP_0_DATA — BI 6 12 42 68
SMB_CLK1/MSMB_CLK E23 — SMBUS_MCP_1_CLK — OUT 42 68
SMB_DATA1/MSMB_DATA G23 — SMBUS_MCP_1_DATA — BI 42 68
SMB_ALERT#/GPIO_64 B24 — AP_PWR_EN — OUT 20 34
FANRPM0/GPIO_60 A9 — MEM_EVENT_L — IN 20 39
FANCTL0/GPIO_61 B10 — TP_ODD_PWR_EN_L — 8
FANRPM1/GPIO_63 D8 — SMC_IG_THROTTLE_L — 8 20 39
FANCTL1/GPIO_62 C9 — ARB_DETECT — 20
CPUVDD_EN E19 — MCP_CPUVDD_EN — OUT 24
GPIO_10 E15 — SPI_CS0_R_L — OUT 41 68
GPIO_11 G15 — SPI_CLK_R — OUT 41 68
GPIO_8 A15 — SPI_MISO — IN 41 68
GPIO_9 C15 — SPI_MOSI_R — OUT 41 68
SUS_CLK/GPIO_34 H20 — PM_CLK32K_SUSCLK_R — OUT 24 68
BUF_SIO_CLK BD4 — TP_MCP_BUF_SIO_CLK
TEST_MODE_EN A21 — MCP_TEST_MODE_EN
PKG_TEST H26

R2163 10K 5% 1/20W MF 201
R2190 1K 1% 1/20W MF 201

PP3V3_S0 — R2180 10K 5% 1/20W MF 201 — BOOT_MODE_SAFE
BOOT_MODE_USER — R2181 10K 5% 1/20W MF 201
R2182 0 5% 1/20W MF 201 — MCP_SAFE_MODE — IN 39
MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

PP3V3_S5 — DRAM_4GB — R2195 1K 5% 1/20W MF 201 — DRAM_SPD_2 — R2197 1K 5% 1/20W MF 201
MLB_RAM_SIZE_0
MLB_RAM_VENDOR_0

PP3V3_S0 — R2140 10K — R2143 10K — R2141 10K — R2142 10K
AUD_I2C_INT_L
MEM_EVENT_L
MCP_GPIO_4
SMC_IG_THROTTLE_L

PP3V3_S3 — R2158 100K
AP_PWR_EN

ARB_DETECT — R2147 100K

MCP_VID<0>
MCP_VID<1>
MCP_VID<2>
R2155 22K
R2156 22K
R2157 22K

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R — C2170 33PF 5% 25V NP0-C0G 201
HDA_BIT_CLK_R — C2171 33PF 5% 25V NP0-C0G 201
HDA_RST_R_L — C2172 10PF 5% 25V NPO 201
HDA_SYNC_R — C2173 10PF 5% 25V NPO 201

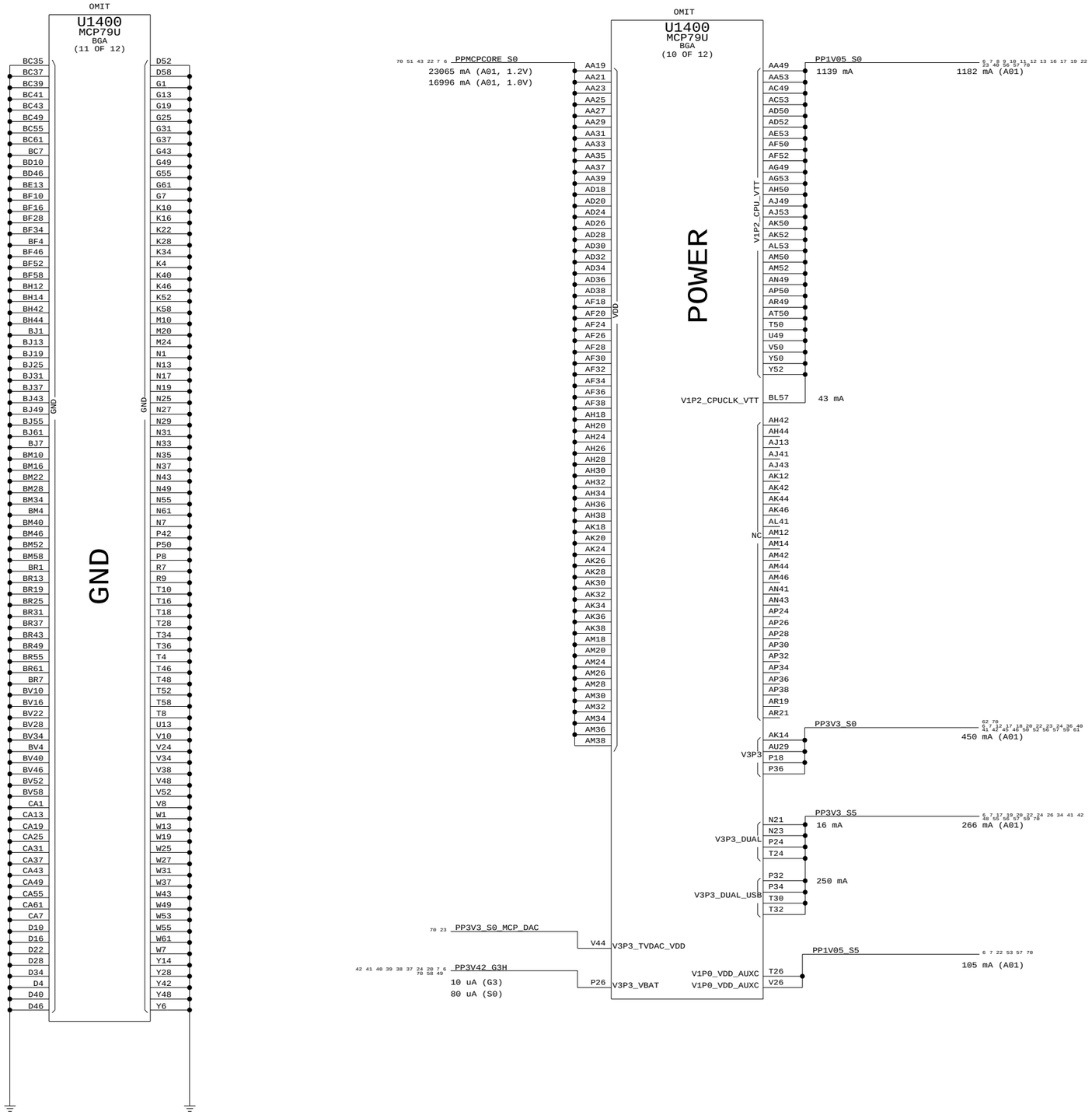
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP HDA & MISC

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 20 OF 71	



MCP Power & Ground

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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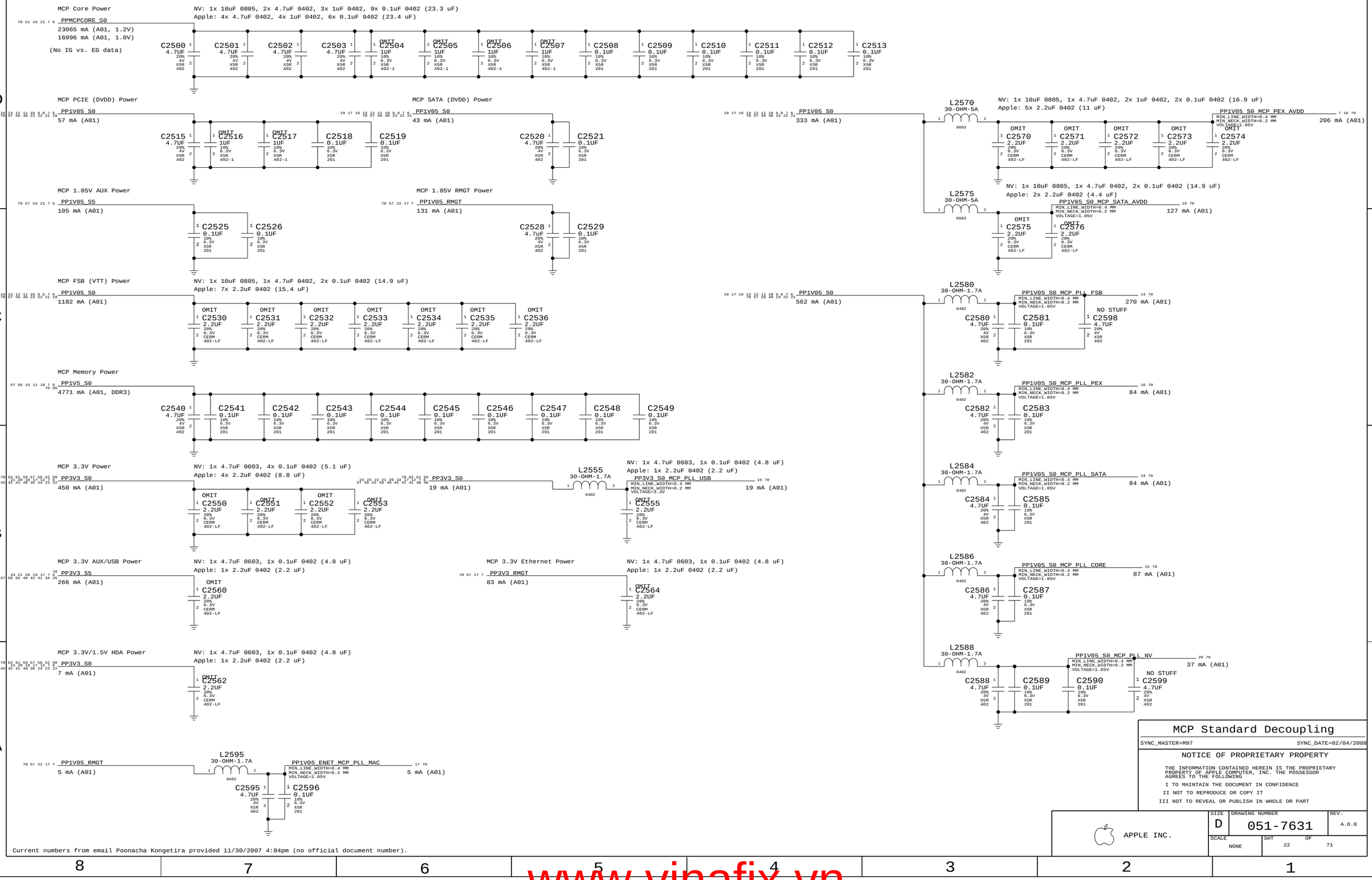
APPLE INC.

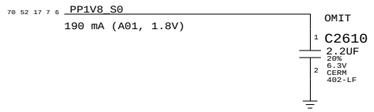
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 21 OF 71	

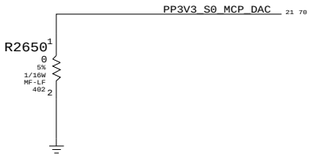
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

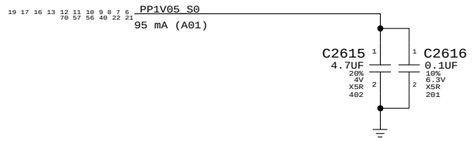


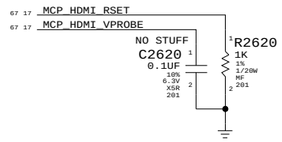
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

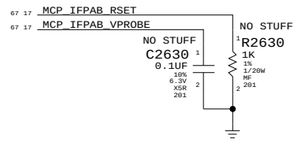
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



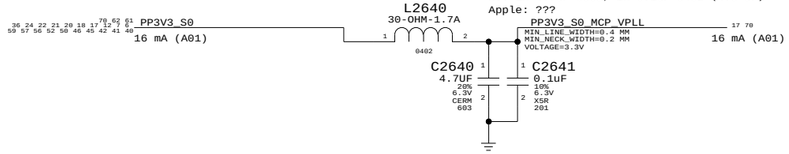








WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



SYNC FROM M97

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Graphics Support

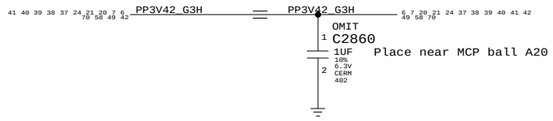
SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

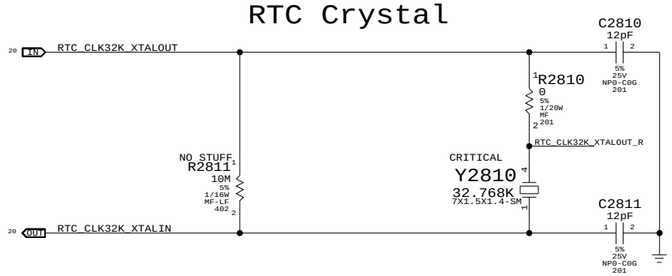
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

SCALE	SHT	OF
NONE	23	71

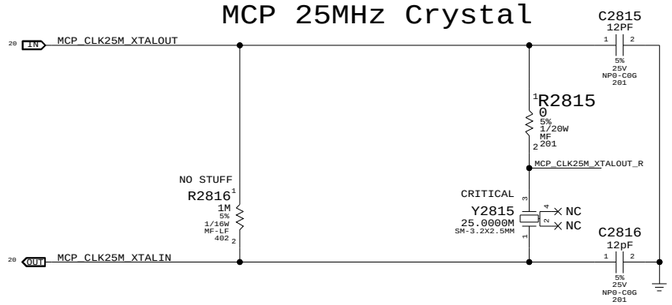
RTC Power Sources



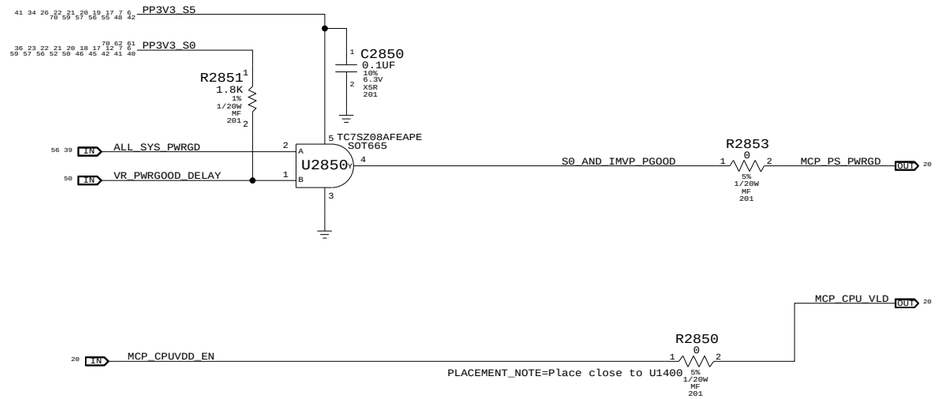
RTC Crystal



MCP 25MHz Crystal



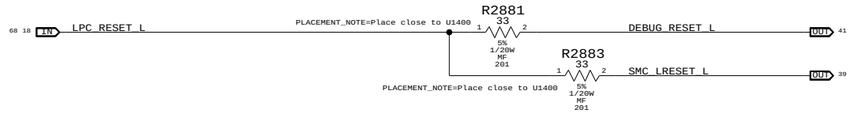
MCP S0 PWRGD & CPU_VLD



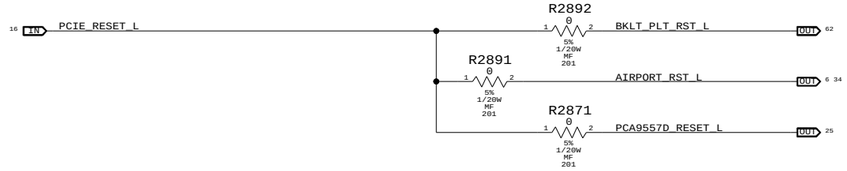
SYNC FROM M97
CHANGED RTC POWER SOURCE TO DIRECT CONNECTION
ADDED MCPSEQ_SMC LOGIC

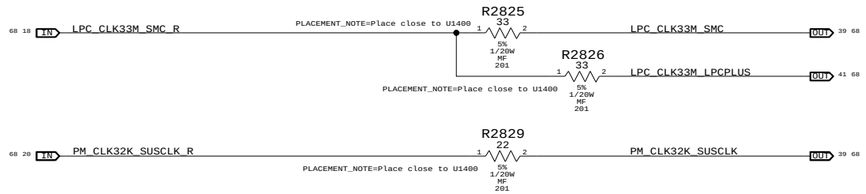
Platform Reset Connections

LPC Reset (Unbuffered)

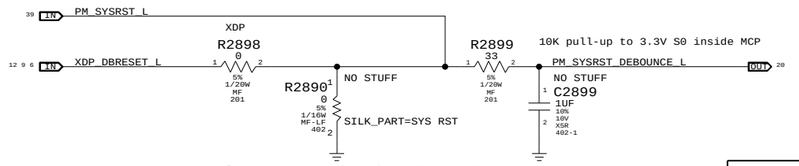


PCIE Reset (Unbuffered)





Reset Button



SB Misc	
SYNC_MASTER=M97	SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 24 OF 71	

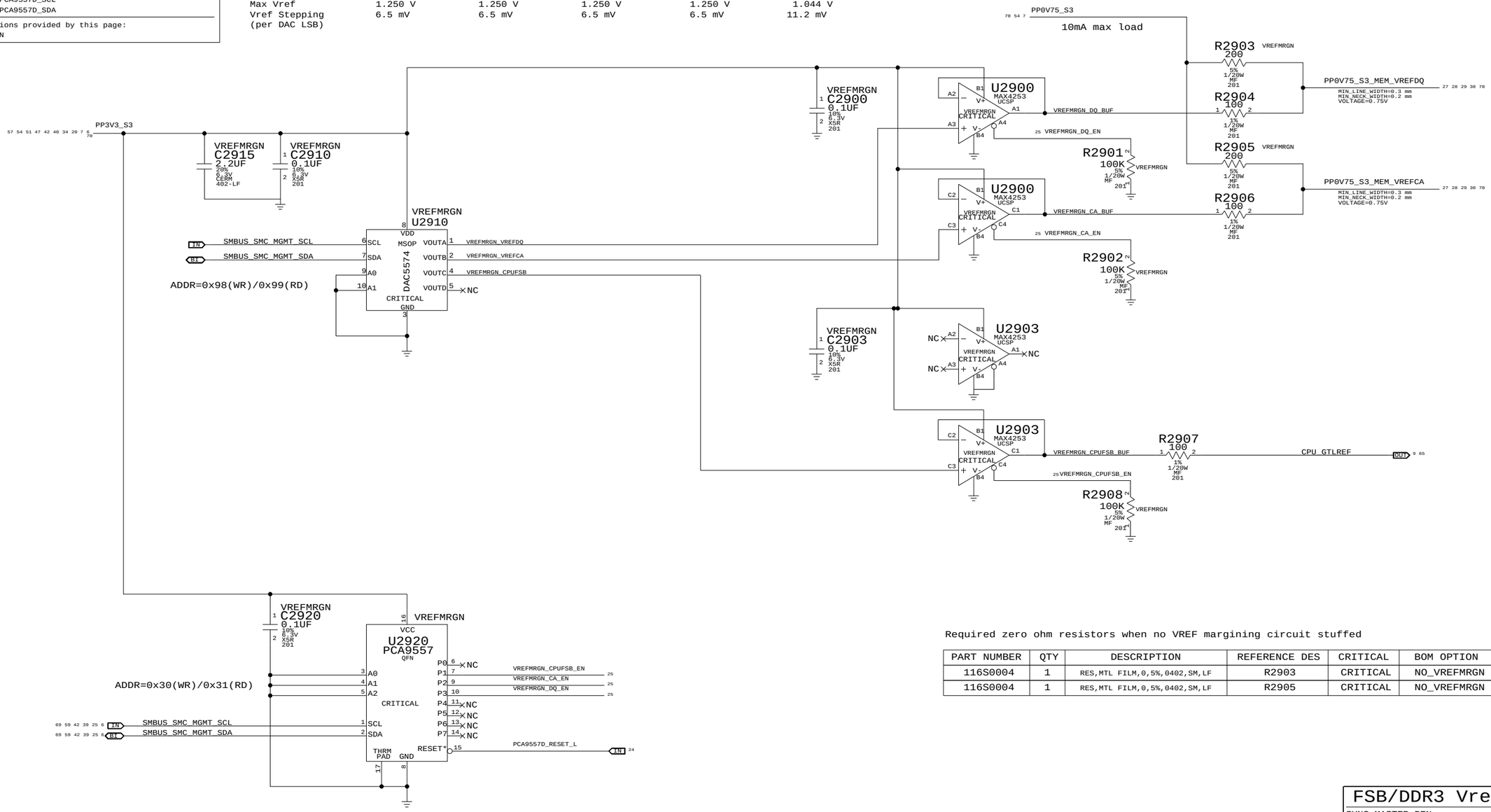
Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

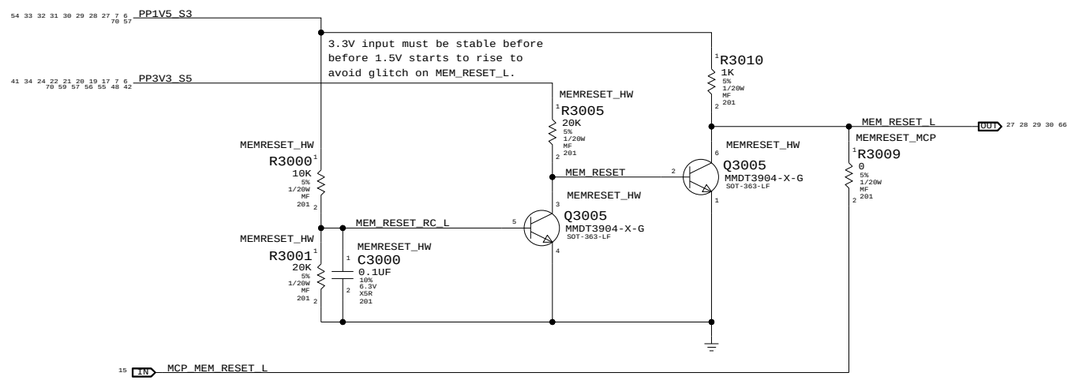
SYNC_MASTER=BEN SYNC_DATE=01/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 25 OF 71	

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

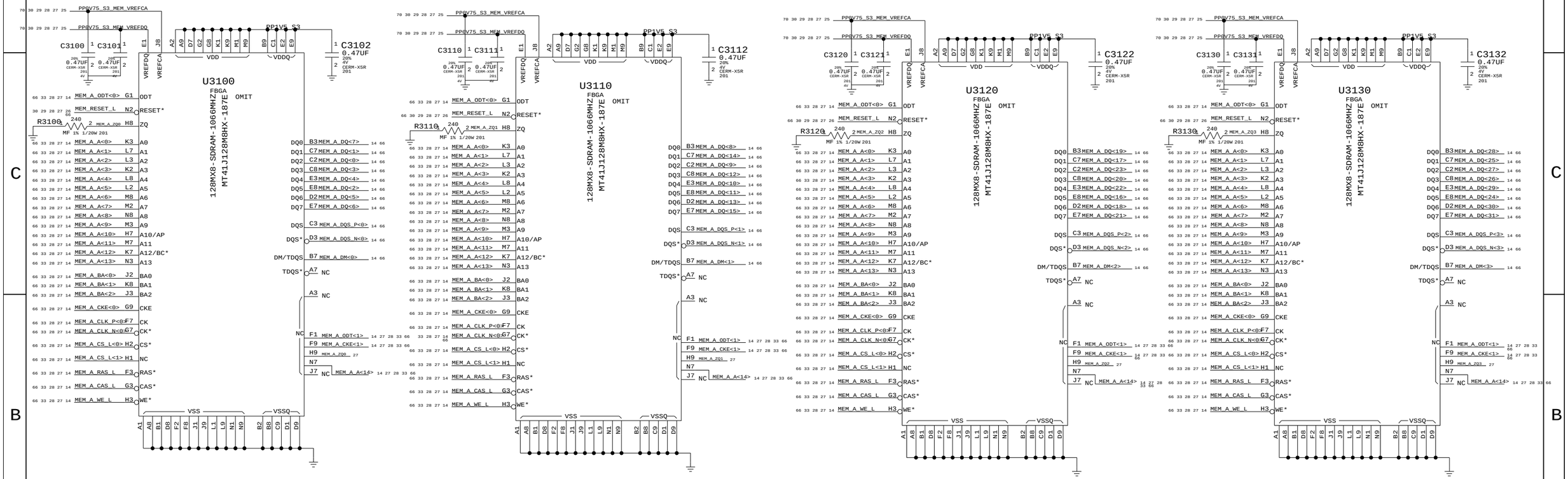


DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=01/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 26 OF 71	



DDR3 DRAM Channel A (0-31)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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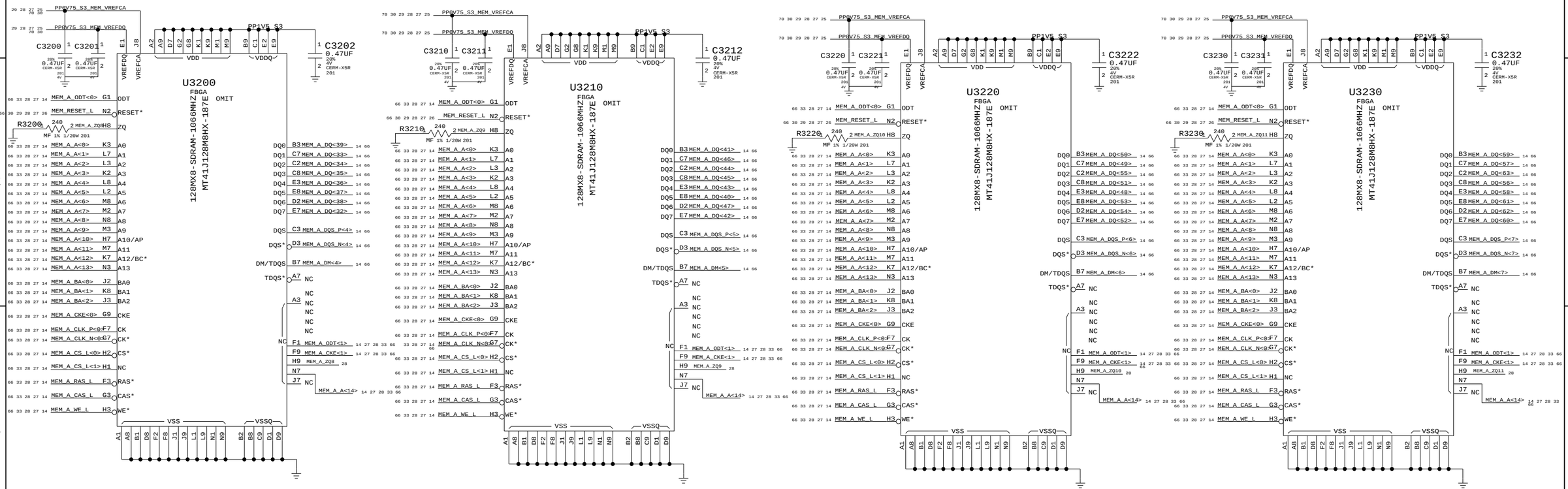
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 27 OF 71	

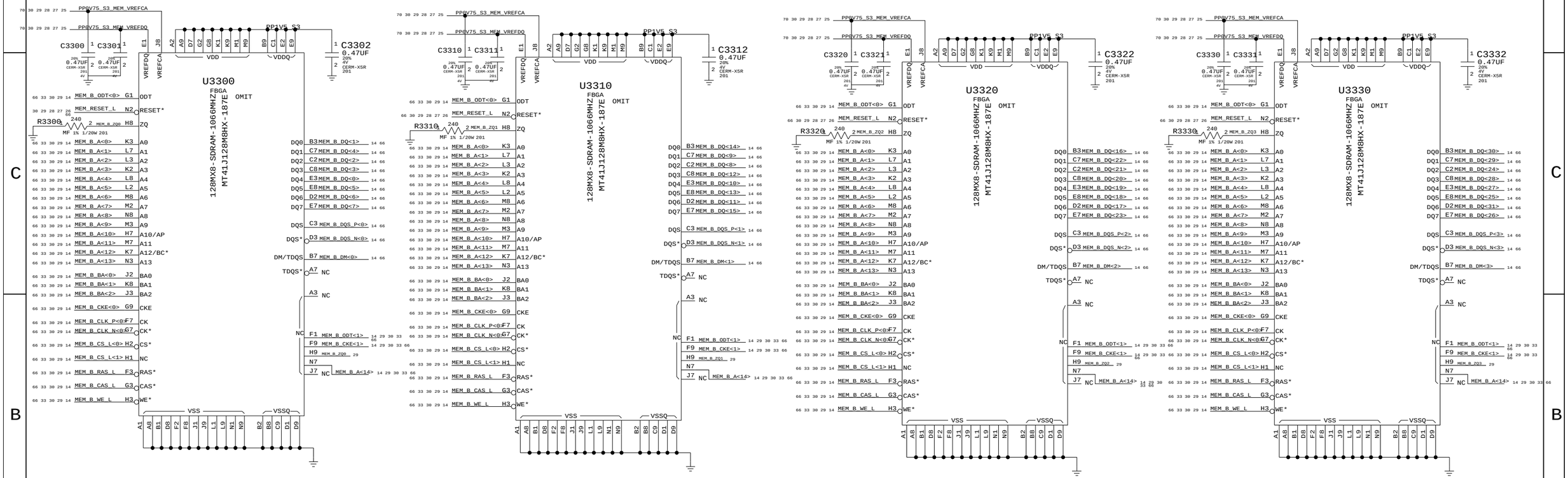


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel A (32-63)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 28 OF 71	



DDR3 DRAM Channel B (0-31)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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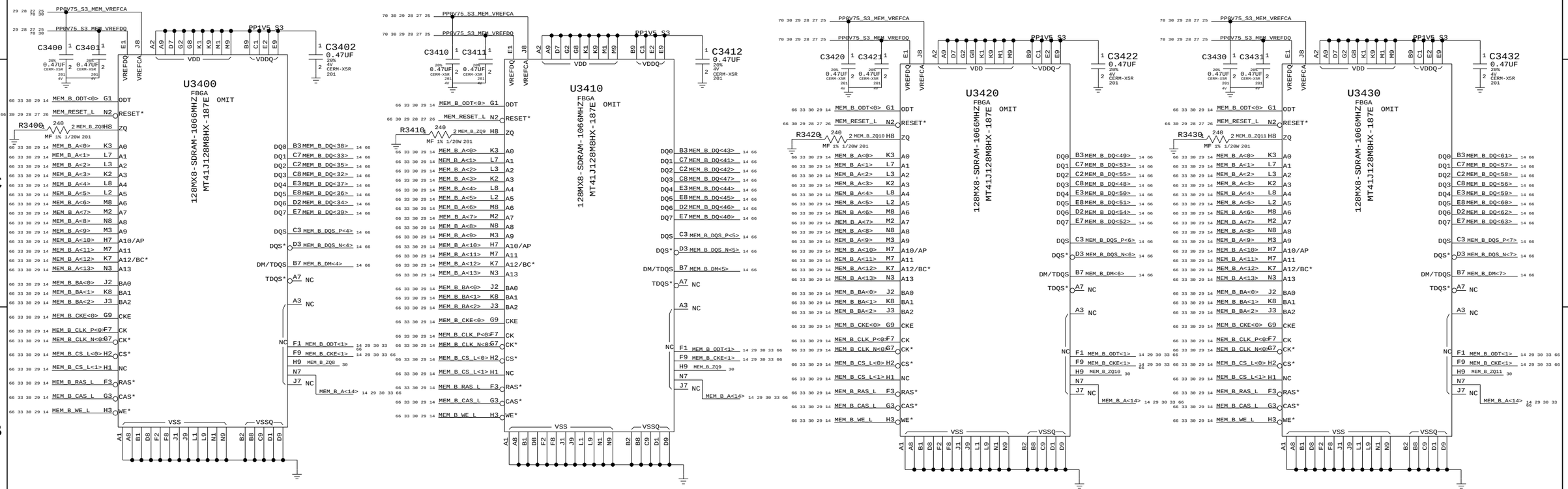
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

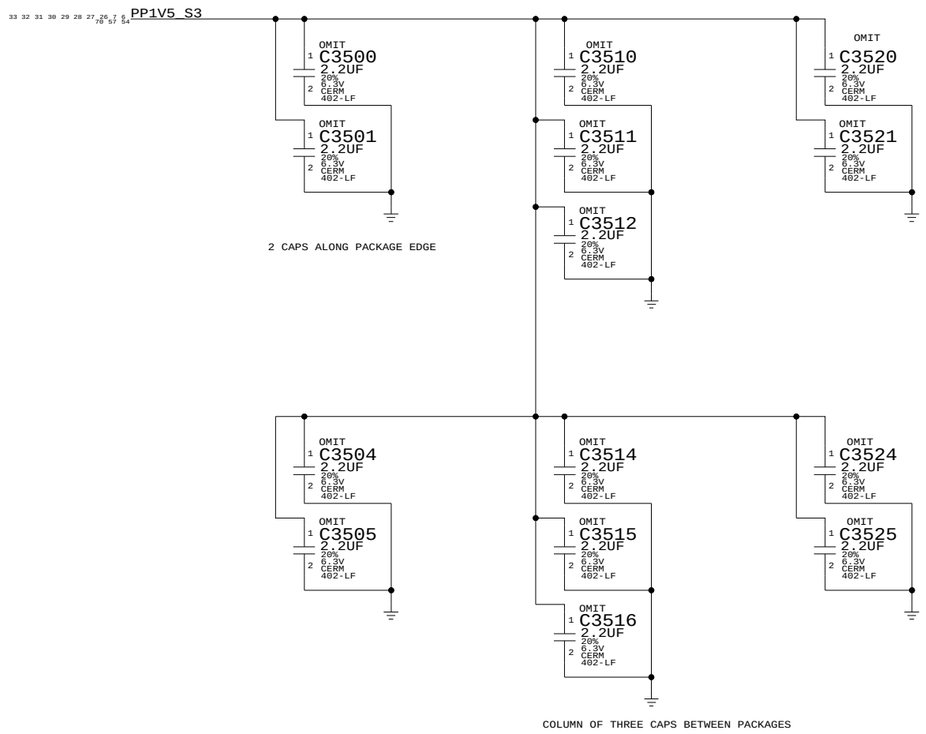
SCALE: NONE SHT 29 OF 71

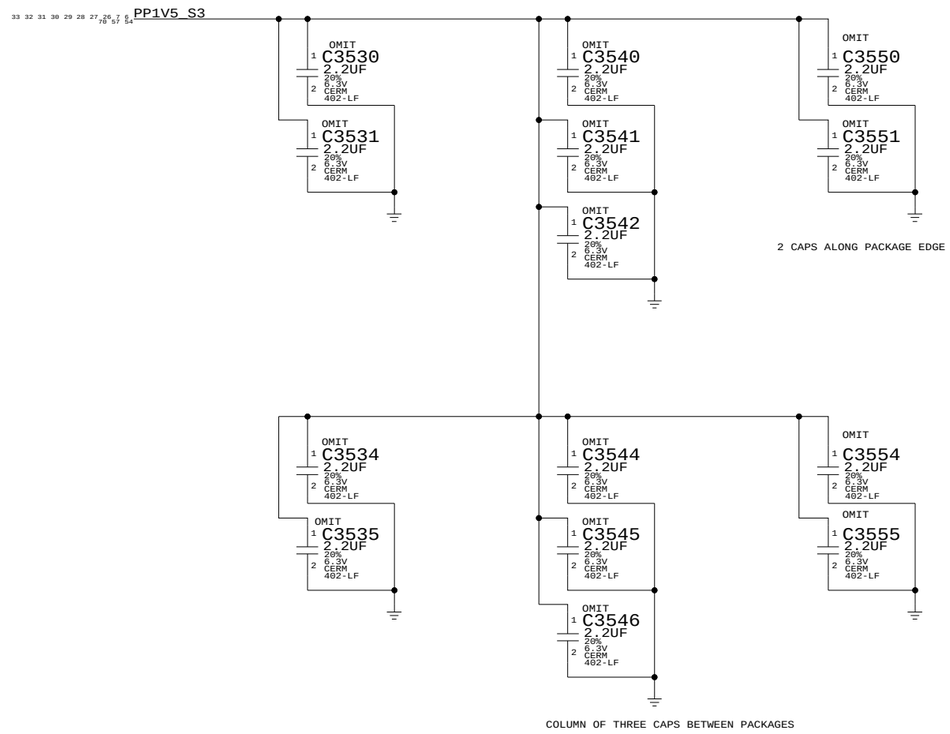


DDR3 DRAM Channel B (32-63)

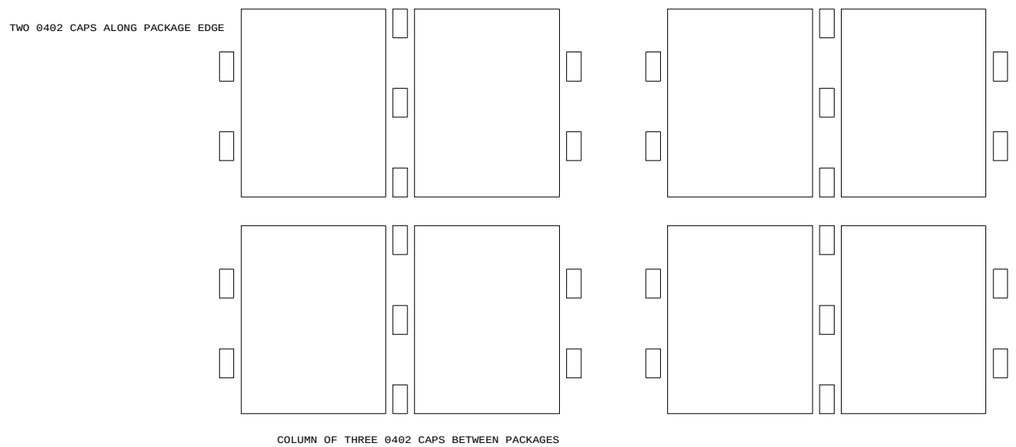
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 30 OF 71	





APPROXIMATE CAP ARRANGEMENT



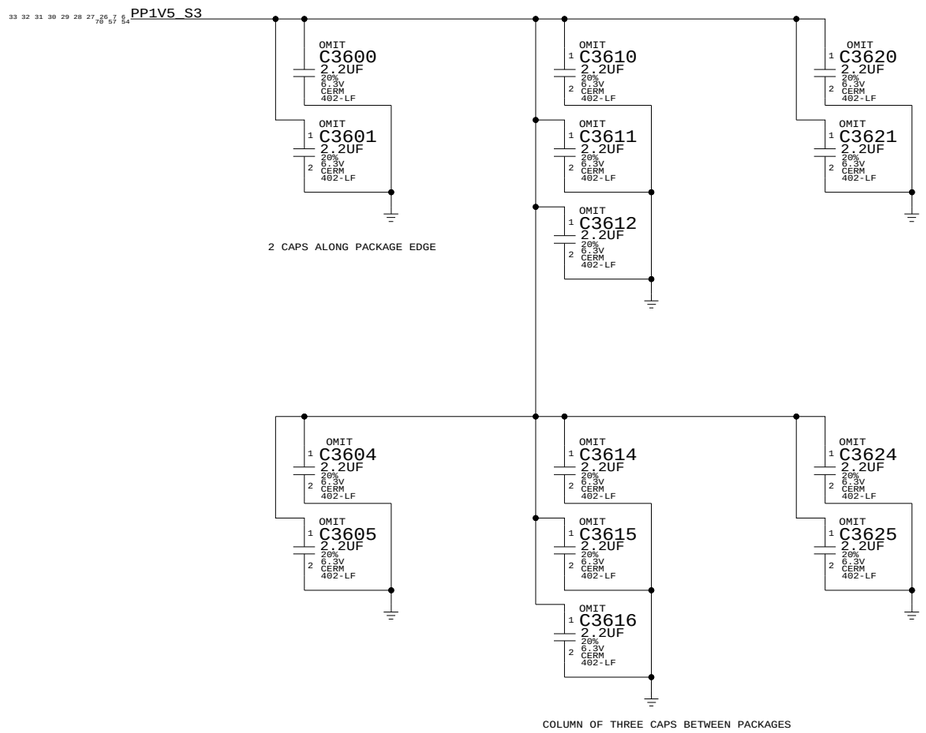
DDR BYPASSING 1

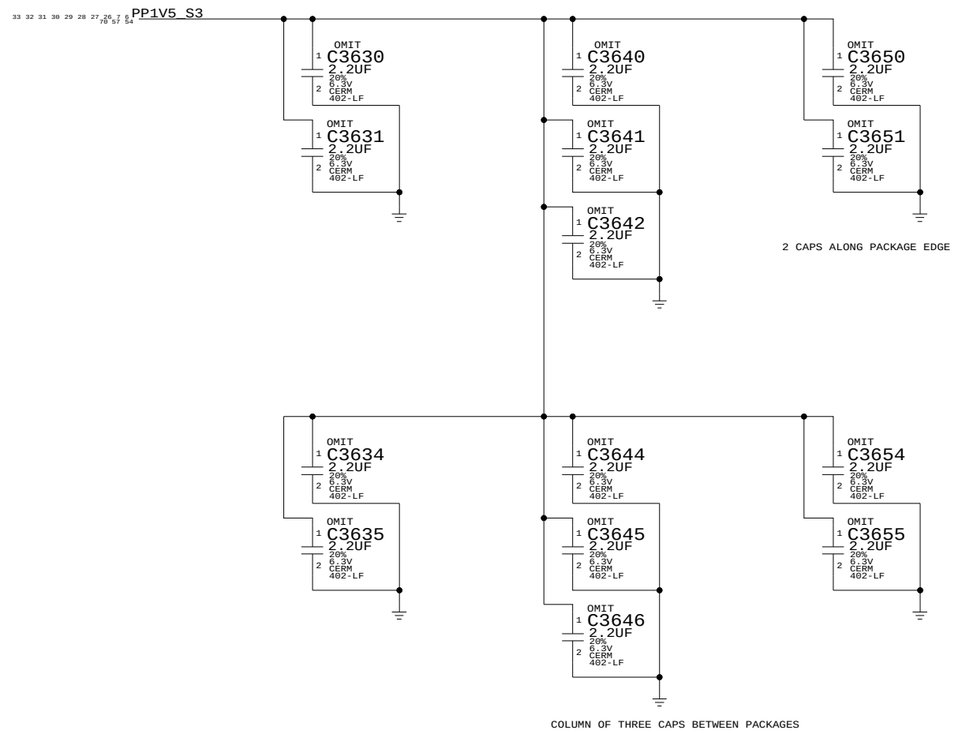
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

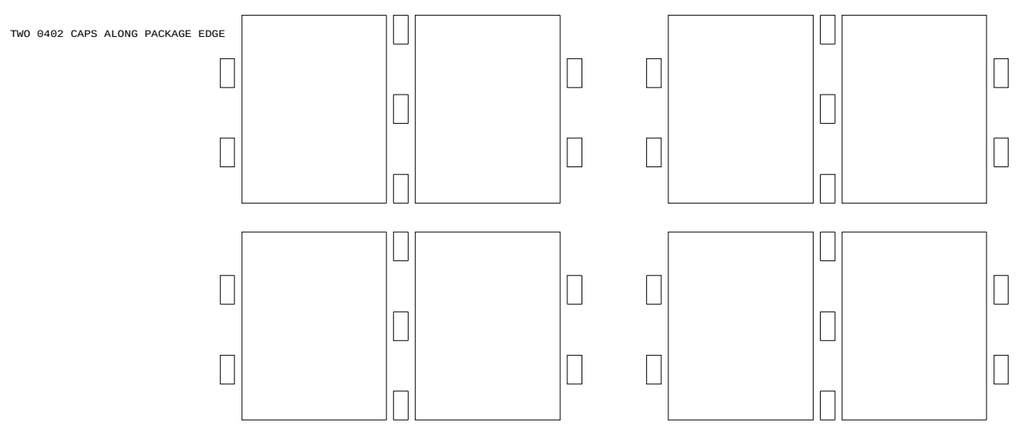
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

SCALE	SHT	OF
NONE	31	71





APPROXIMATE CAP ARRANGEMENT



DDR BYPASSING 2

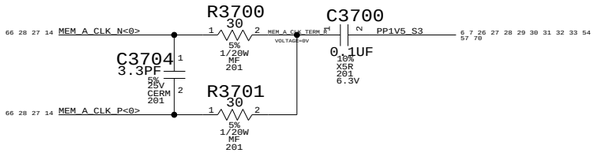
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

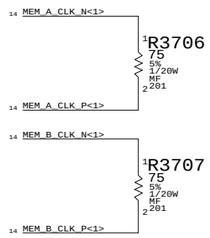
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 32 OF 71	

MEM CLOCK TERMINATION

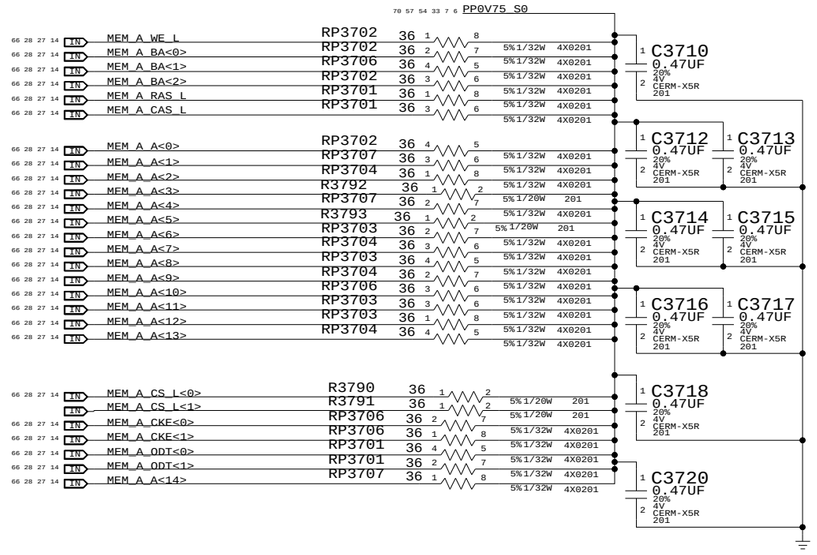
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

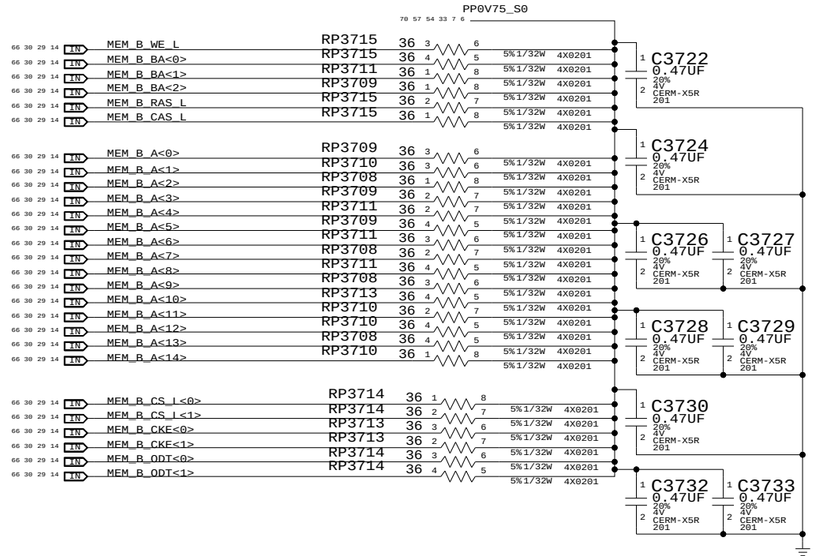


Unused Clock Termination



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



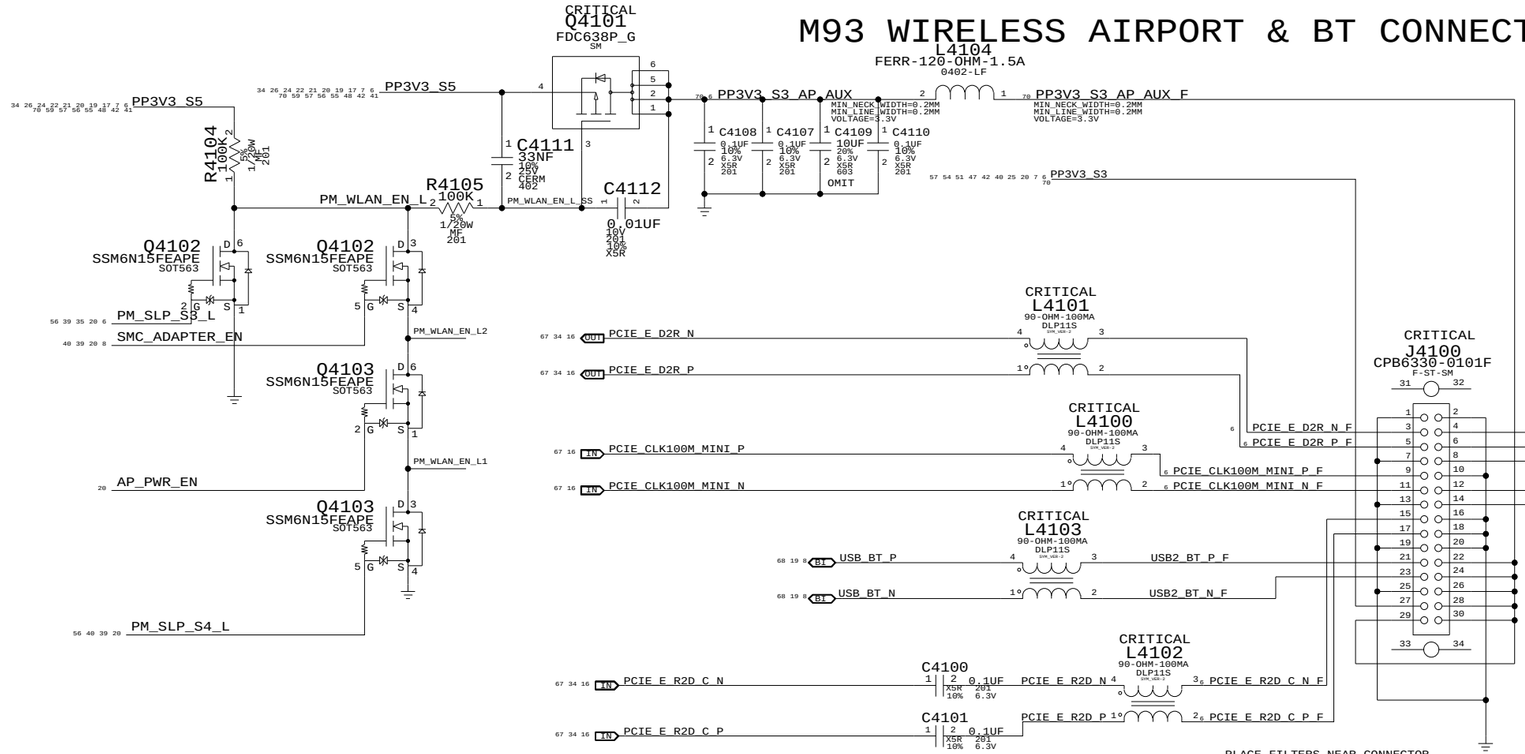


Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 33 OF 71	

M93 WIRELESS AIRPORT & BT CONNECTOR



PCIE_E_D2R_N — PCIE_E_D2R_N MAKE_BASE=TRUE

PCIE_E_D2R_P — PCIE_E_D2R_P MAKE_BASE=TRUE

PCIE_E_R2D_C_N — PCIE_E_R2D_C_N MAKE_BASE=TRUE

PCIE_E_R2D_C_P — PCIE_E_R2D_C_P MAKE_BASE=TRUE

PLACE C4100,C4101 < 250 MILS FROM MCP

PLACE FILTERS NEAR CONNECTOR

APN:516S0580

Wireless M93 Connector

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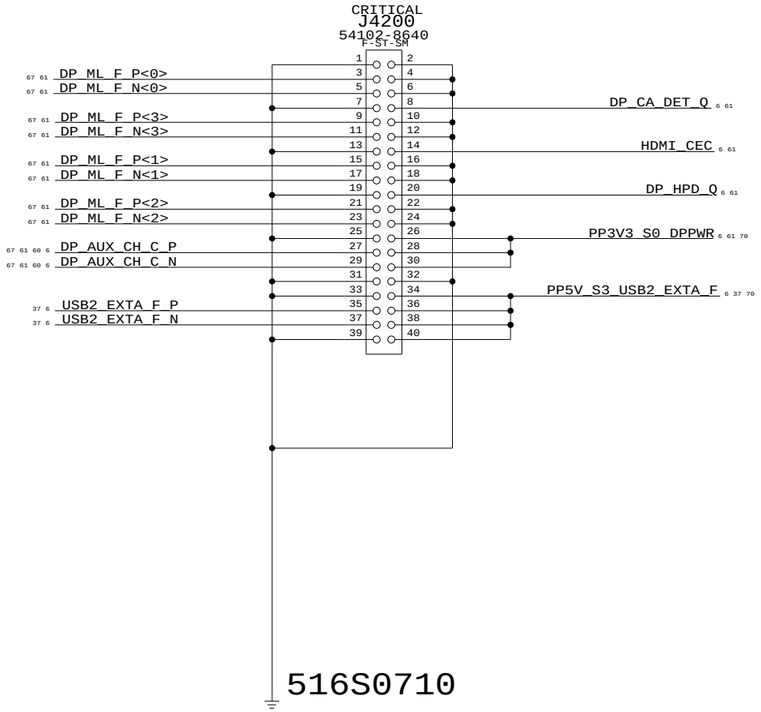
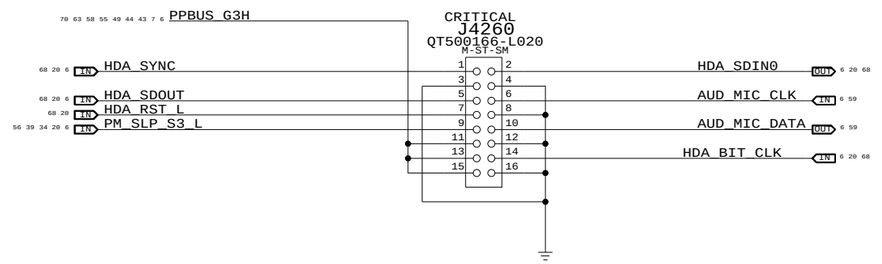
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 34 OF 71	

Micro-DisplayPort / USB to RIO Hatch Assembly



Audio Connector



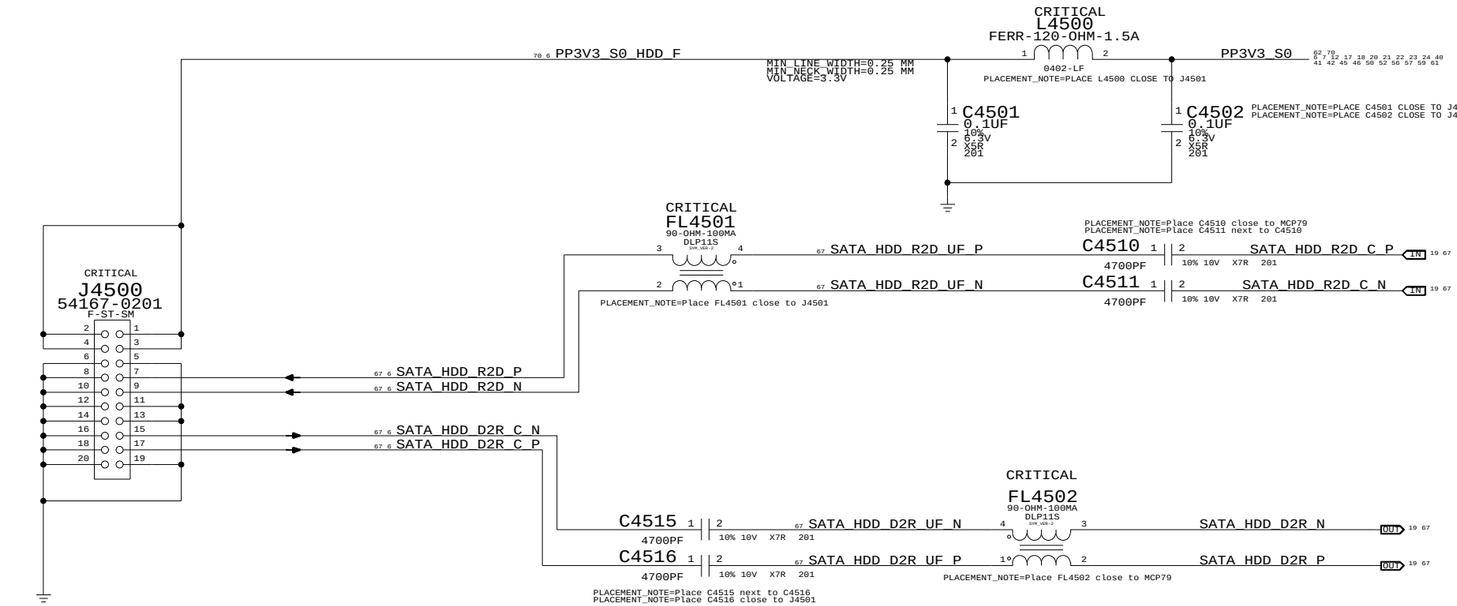
Hatch and Audio Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 35 OF 71	

SATA HDD PORT



SATA Connectors

SYNC_MASTER=CHANGZHANG SYNC_DATE=02/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 36 OF 71	

USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT

CRITICAL
C4610 100UF 20% 6.3V POLY-TANT CASE-B2-SM

CRITICAL
L4602 FERR-120-OHM-3A 0603
PP5V_S3_USB2_EXTA_F
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

ROUTE USB DATA LINES AS DIFFERENTIAL PAIRS

CRITICAL
L4600 90-OHM-100MA DLP11S

PP5V_S3_USB2_EXTA_F
USB2_EXTA_F_N
USB2_EXTA_F_P
CONNECT TO RIO CONNECTOR J4200

70 59 57 55 54 51 38 7 6 PP5V_S3

OMIT
C4613 10uF 20% 6.3V X5R 603

C4612 0.1UF 10% 6.3V X5R 201

CRITICAL
U4600 TPS2052B MSOP

2	IN	OUT1	7
8	OC1*		
3	EN1	OUT2	6
5	OC2*		
4	EN2		
	GND	TPAD	
1			9

70 PP5V_S3_USB2_EXTA
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

68 37 USB_EXTA_MUXED_N
68 37 USB_EXTA_MUXED_P

CRITICAL
D4600 SC-75 RCLAMP0502B

C4602 0.01UF 10% 10V X5R 201

LAYOUT NOTE:C4602 IS AN EMC BY-PASS CAP FOR J4200

DUAL SWITCH HAS GANGED OUTPUT
BOTH SWITCHES WILL TRIP TOGETHER AT 1.5A-2.2A

56 USBPWR_EN

EXTAUSB_OC_F_L

R4650 1K 5% 1/16W MF-LF 402

8 19 USB_EXTA_OC_L

C4650 0.47UF 10% 6.3V CERM-X5R 402

USB/SMC MUX

42 41 40 39 38 24 21 20 7 6 70 58 49 PP3V42_G3H

R4675 100 5% 1/20W MF 201

70 PP3V42_G3H_SMCUSBMUX_R

C4675 0.1UF 10% 6.3V X5R 201

PLACE C4675 NEAR U4675

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V

R4677 10K 5% 1/20W MF 201

USB_EXTA_MUXED_P 37 68
USB_EXTA_MUXED_N 37 68

VCC

41 40 39 SMC_RX_L
41 40 39 SMC_TX_L
68 19 8 USB_EXTA_P
68 19 8 USB_EXTA_N

CRITICAL
U4675 PI3USB102ZLE TQFN

5	M+	Y+	1
4	M-	Y-	2
7	D+		
6	D-		
8	OE*	SEL	10

USB_DEBUGPRT_EN_L 39

SEL=0 CHOOSE SMC
SEL=1 CHOOSE USB

GND

NOSTUFF
R4678 0 5% 1/20W MF 201

PLACE NEAR U4675

NOSTUFF
R4679 0 5% 1/20W MF 201

USB EXTERNAL CONNECTORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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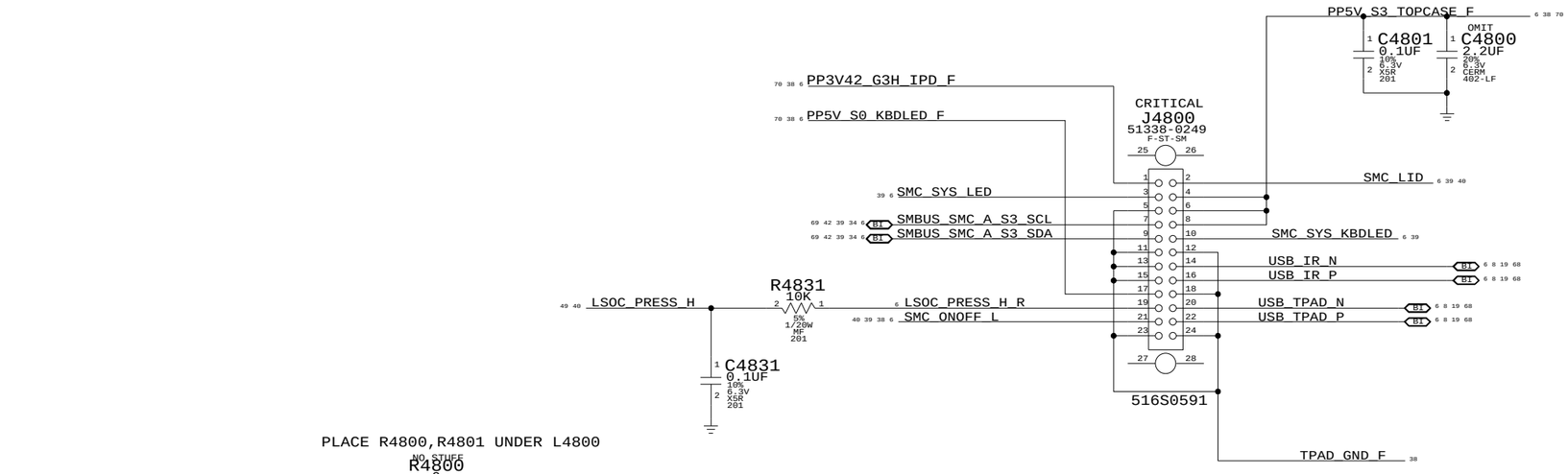
APPLE INC.

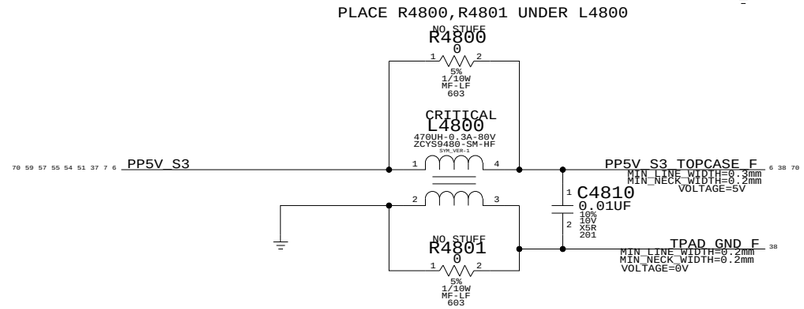
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

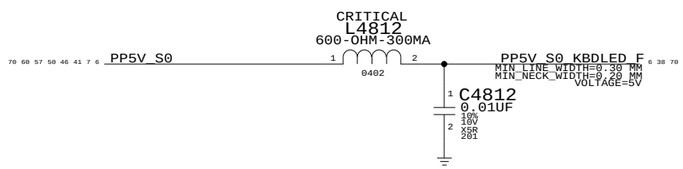
SCALE: NONE SHT 37 OF 71

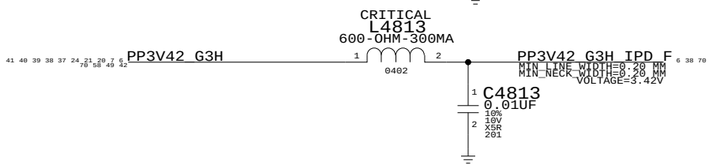
IPD Connector



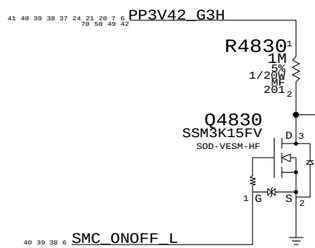
PLACE R4800,R4801 UNDER L4800







Power Button Inverter



Inverted to drive SMC_RESET logic

IPD Connector

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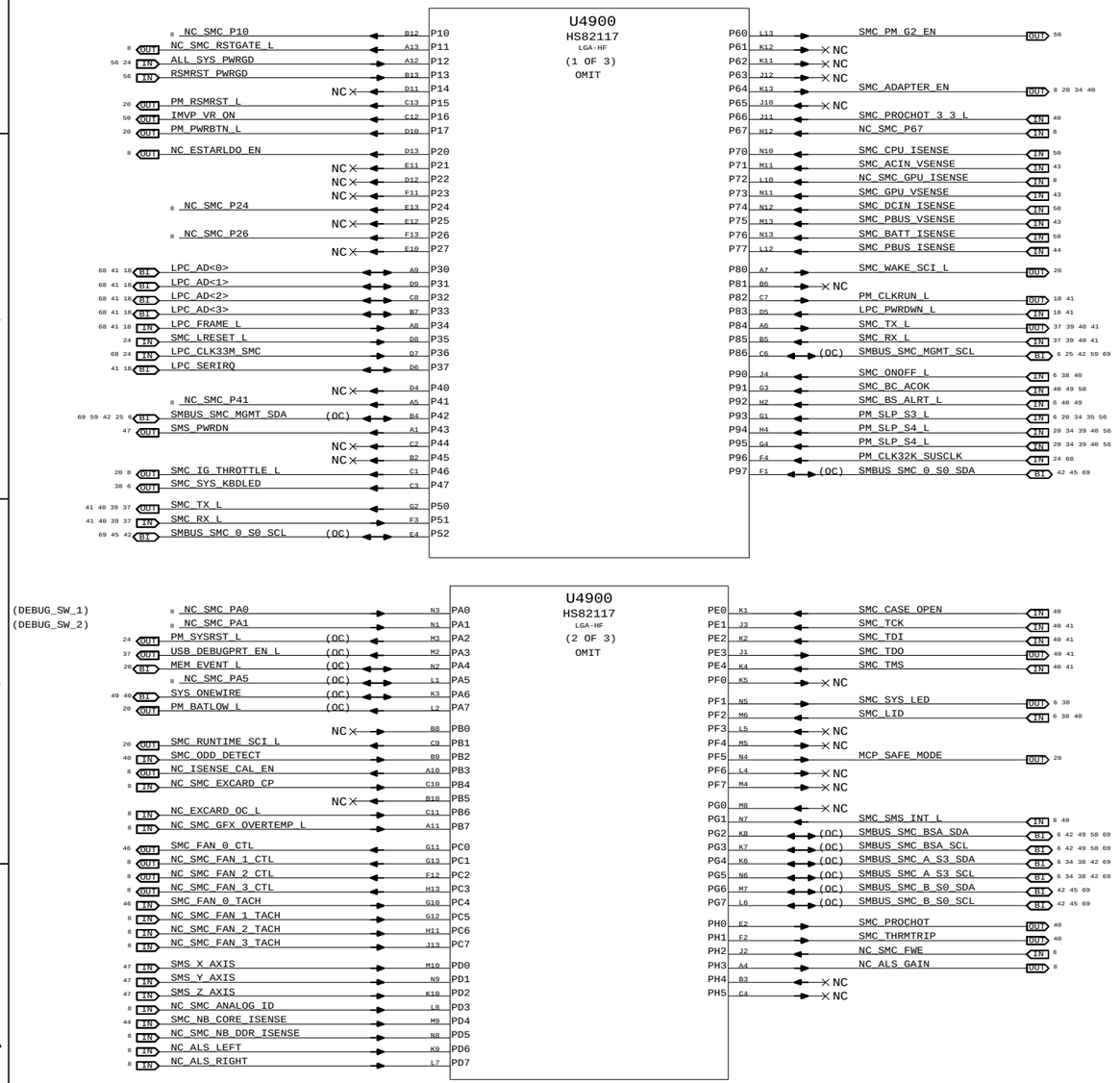
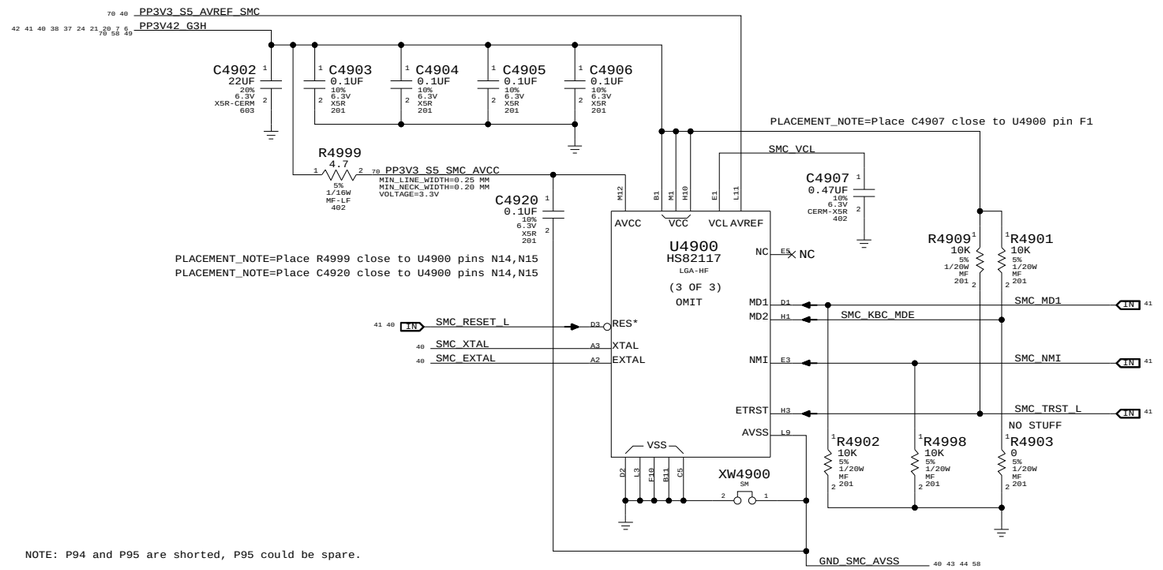
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 38 OF 71	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.



NOTE: P94 and P95 are shorted, P95 could be spare.

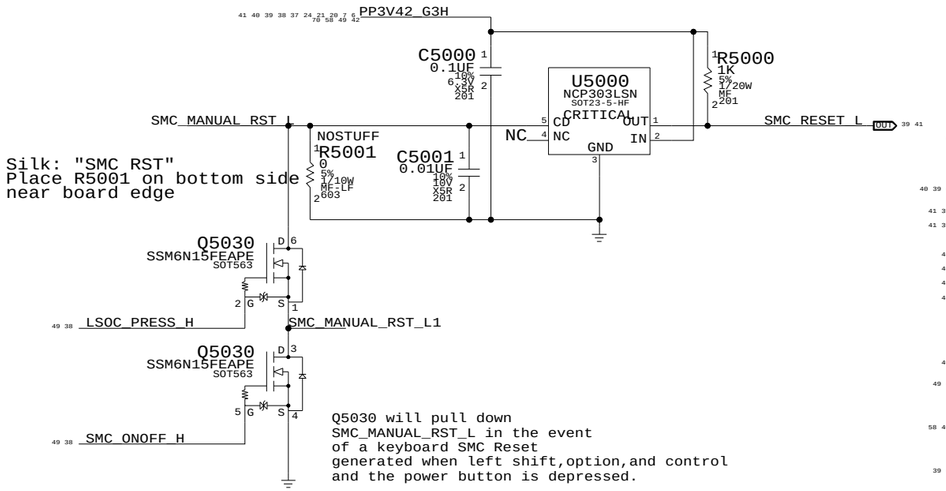
SMC

SYNC_MASTER=M97 SYNC_DATE=02/21/2008

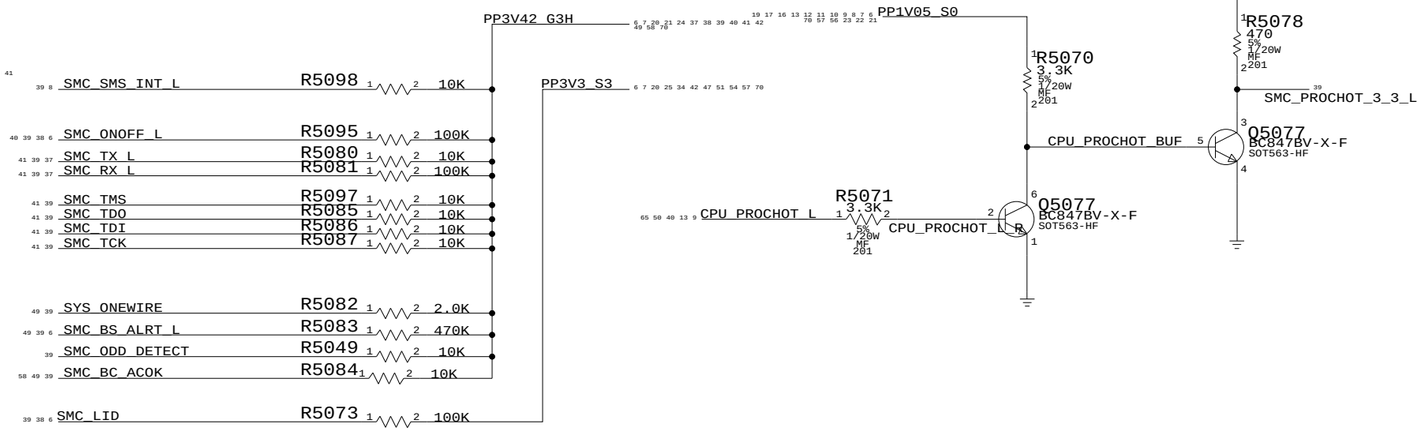
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 39 OF 71	

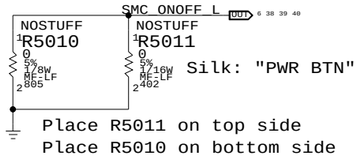
SMC Reset Button / Brownout Detect



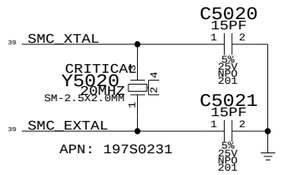
SMC 1.05V to 3.3V Level Shifting

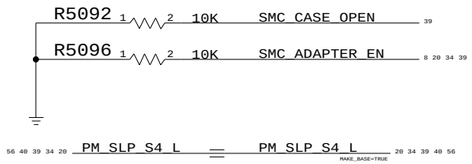


Debug Power Button

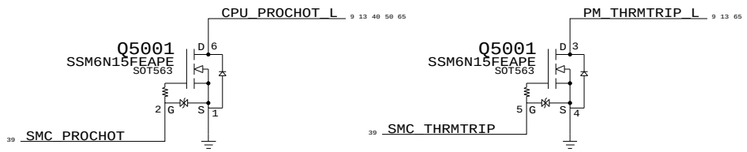


SMC Crystal Circuit

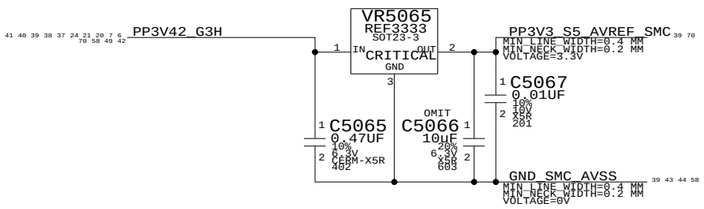




SMC 3.3V to 1.05V Level Shifting



SMC AVREF Supply



SMC SUPPORT

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

SCALE	SHT	OF
NONE	40	71

LPC+SPI Connector

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be
selected w/ R5190,R5191,R5192,R5193

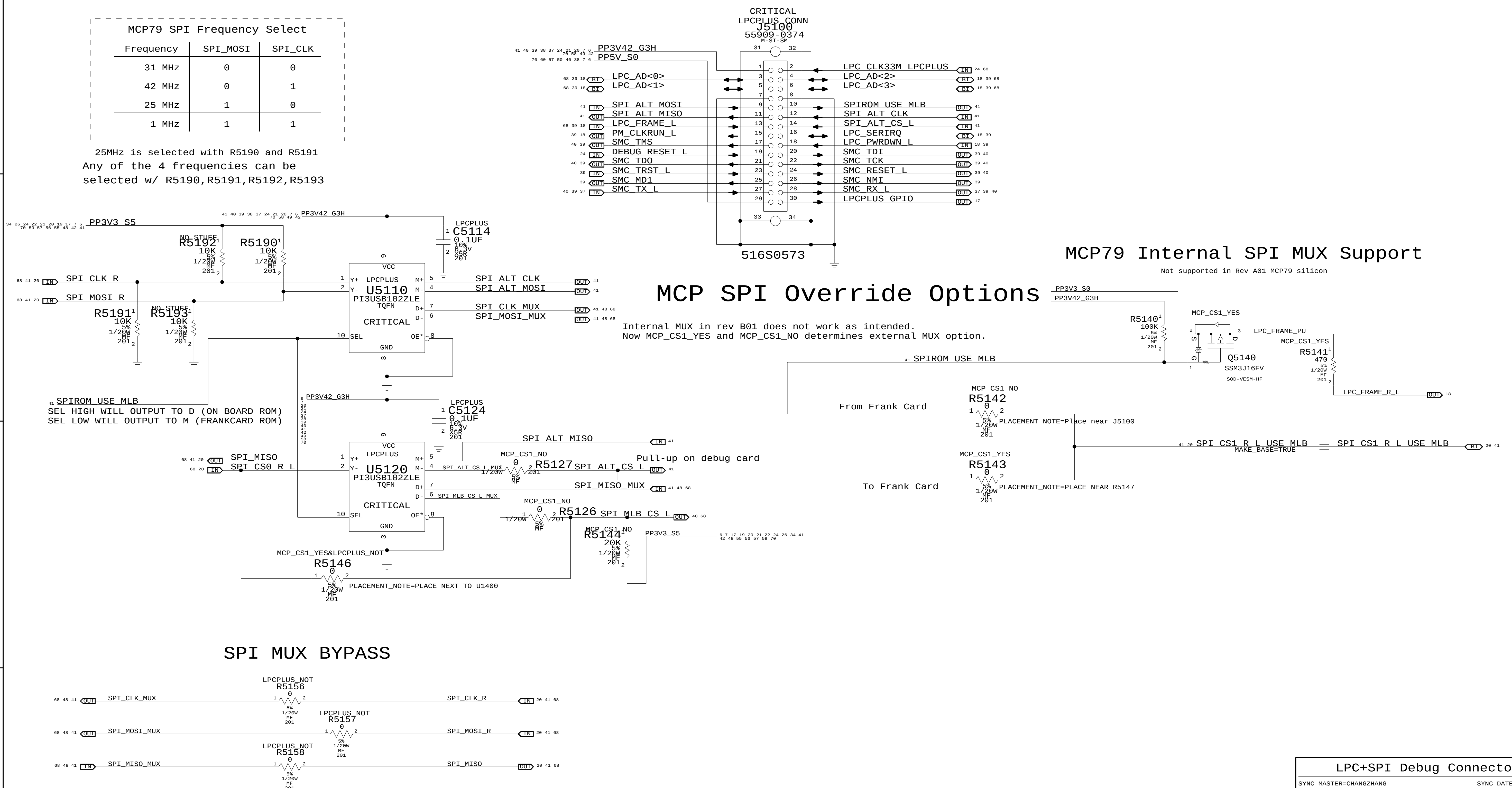
MCP SPI Override Options

Internal MUX in rev B01 does not work as intended.
Now MCP_CS1_YES and MCP_CS1_NO determines external MUX option.

MCP79 Internal SPI MUX Support

Not supported in Rev A01 MCP79 silicon

SEL HIGH WILL OUTPUT TO D (ON BOARD ROM)
SEL LOW WILL OUTPUT TO M (FRANKCARD ROM)



CRITICAL
LPCPLUS_CONN
J5100
55909-0374
516S0573
PP3V42_G3H
PP5V_S0
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_CLK33M_LPCPLUS
SPI_ALT_MOSI
SPI_ALT_MISO
LPC_FRAME_L
PM_CLKRUN_L
SMC_TMS
DEBUG_RESET_L
SMC_TDO
SMC_TRST_L
SMC_MD1
SMC_TX_L
SPIROM_USE_MLB
SPI_ALT_CLK
SPI_ALT_CS_L
LPC_SERIRQ
LPC_PWRDWN_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_NMI
SMC_RX_L
LPCPLUS_GPIO
PP3V3_S5
SPI_CLK_R
SPI_MOSI_R
NO STUFF
R5192
R5190
R5191
R5193
10K
LPCPLUS
C5114
0.1UF
U5110
PI3USB102ZLE
TQFN
CRITICAL
SPI_CLK_MUX
SPI_MOSI_MUX
C5124
U5120
SPI_MISO
SPI_CS0_R_L
SPI_ALT_MISO
MCP_CS1_NO
R5127
SPI_ALT_CS_L
Pull-up on debug card
SPI_MISO_MUX
R5126
SPI_MLB_CS_L
R5144
20K
MCP_CS1_YES&LPCPLUS_NOT
R5146
PLACEMENT_NOTE=PLACE NEXT TO U1400
PP3V3_S0
R5140
100K
MCP_CS1_YES
Q5140
SSM3J16FV
SOD-VESM-HF
LPC_FRAME_PU
R5141
470
LPC_FRAME_R_L
From Frank Card
R5142
PLACEMENT_NOTE=Place near J5100
SPI_CS1_R_L_USE_MLB
MAKE_BASE=TRUE
R5143
To Frank Card
PLACEMENT_NOTE=PLACE NEAR R5147
SPI MUX BYPASS
LPCPLUS_NOT
R5156
R5157
R5158

LPC+SPI Debug Connector	
SYNC_MASTER=CHANGZHANG	SYNC_DATE=01/24/2008

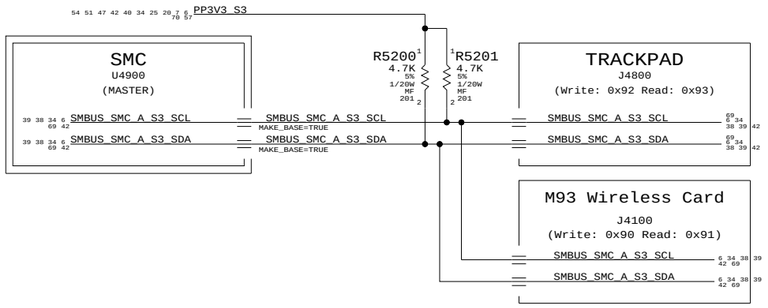
NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

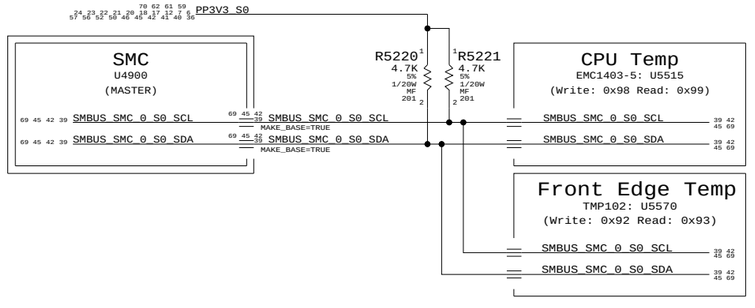
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 41	OF 71

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

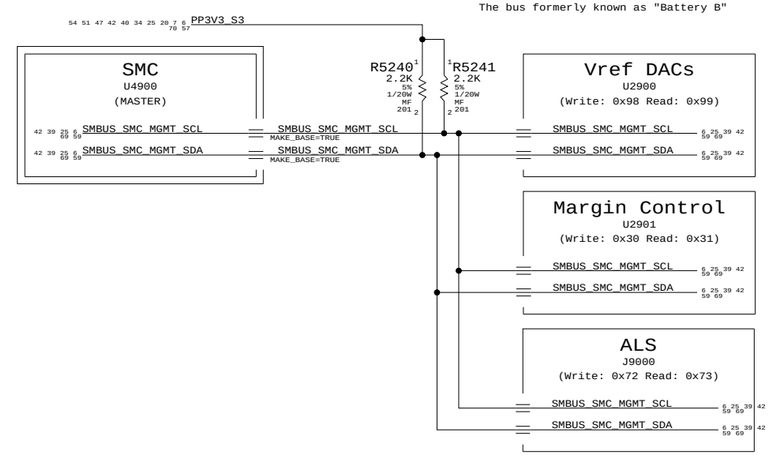


SMC "0" SMBus Connections

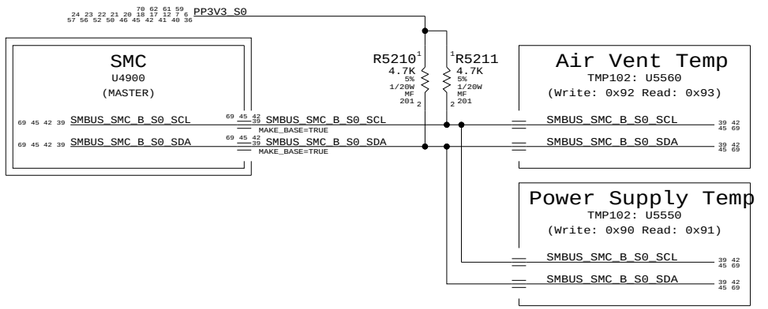


SMC "Management" SMBus Connections

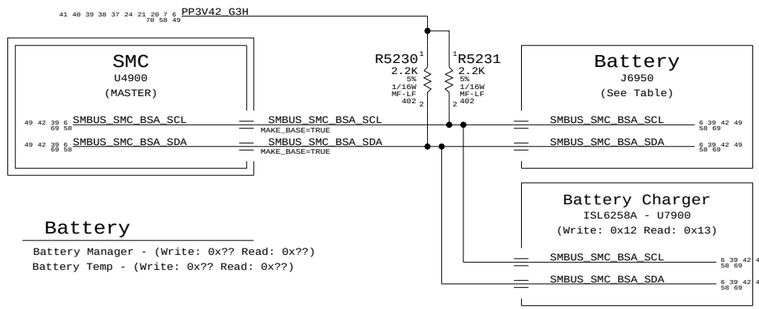
The bus formerly known as "Battery B"



SMC "B" SMBus Connections



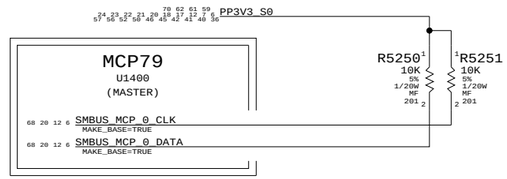
SMC "Battery A" SMBus Connections



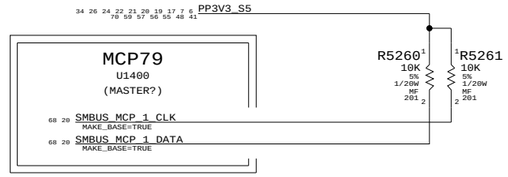
Battery

Battery Manager - (Write: 0x?? Read: 0x??)
Battery Temp - (Write: 0x?? Read: 0x??)

MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS



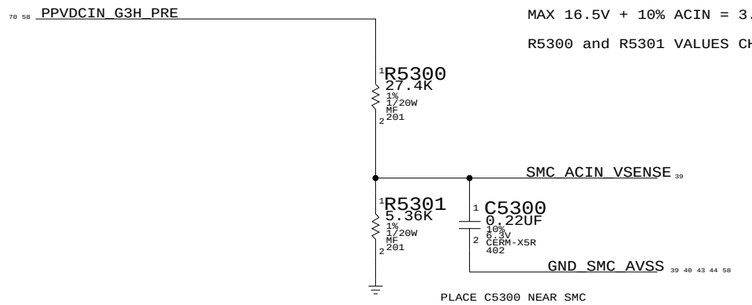
M97 SMBUS CONNECTIONS

SYNC_MASTER=BEN SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 42 OF 71	

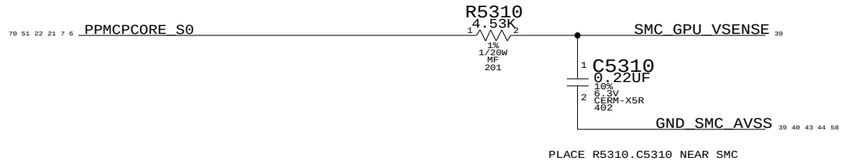
ACIN VOLTAGE SENSE



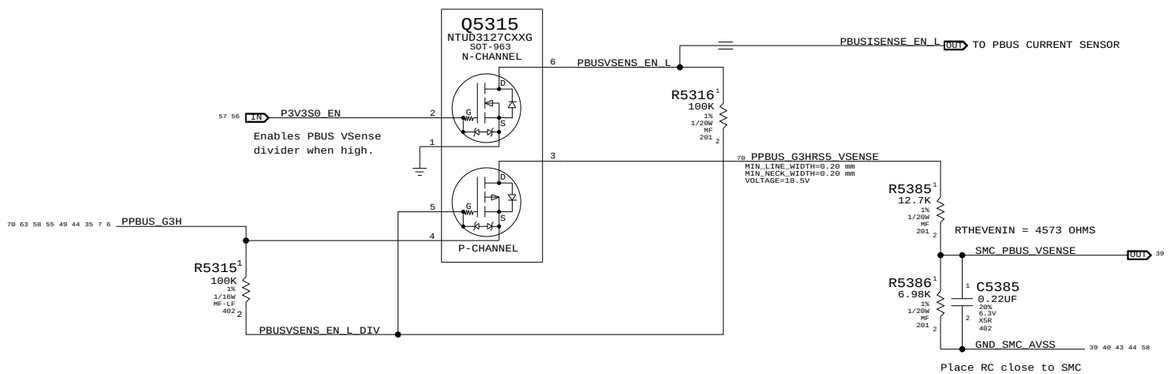
MAX 16.5V + 10% ACIN = 3.0V SMC_ACIN_VSENSE

R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

MCP VOLTAGE SENSE



PBUS VOLTAGE SENSE



Voltage Sensors

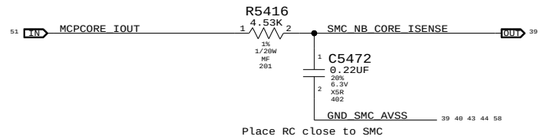
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 43 OF 71	

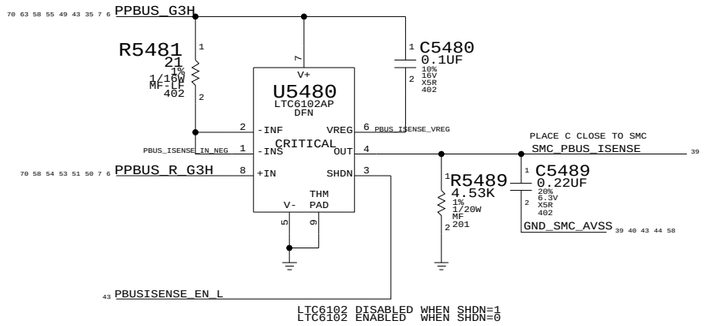
MCP VCore Current Sense

MCP VCore Current Sense Filter



Place RC close to SMC

PBUS Current Sense



LTC6102 DISABLED WHEN SHDN=1
LTC6102 ENABLED WHEN SHDN=0

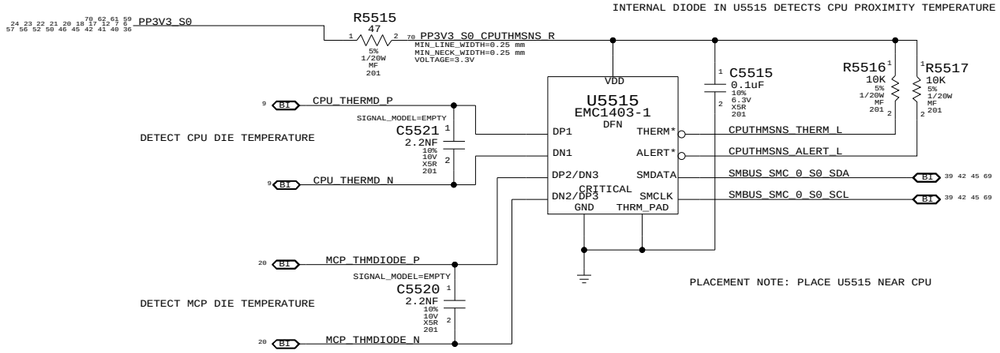
Current Sensing

SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008

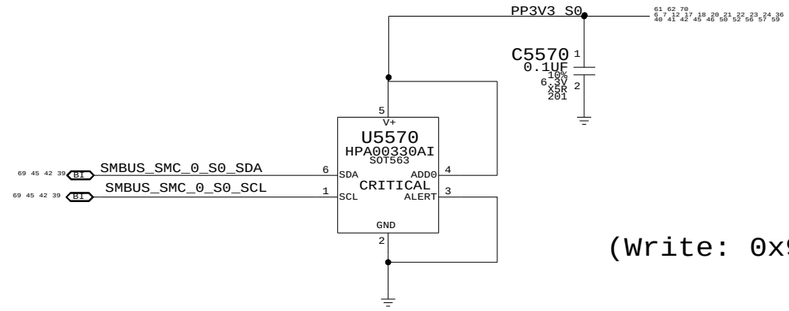
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 44 OF 71	

CPU/MCP T-Diode Thermal Sensor

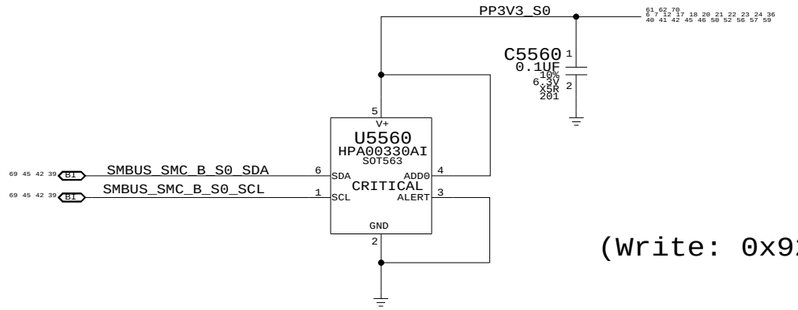


LOCAL TEMP NEAR FRONT EDGE



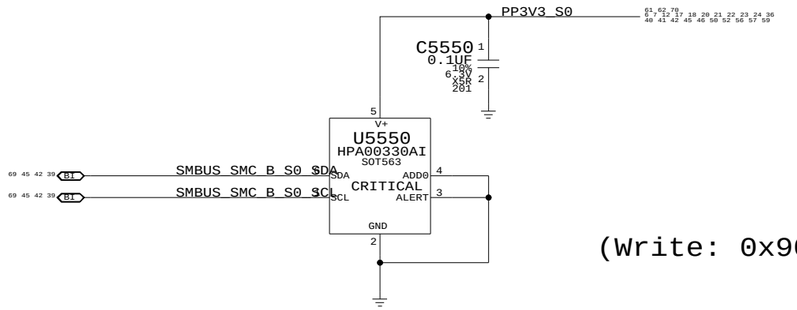
(Write: 0x92 Read: 0x93)

LOCAL TEMP NEAR AIR VENT



(Write: 0x92 Read: 0x93)

LOCAL TEMP NEAR POWER SUPPLIES



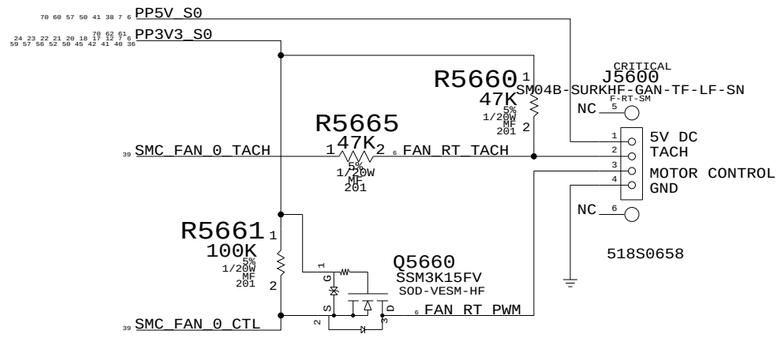
(Write: 0x90 Read: 0x91)

TEMPERATURE SENSORS	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 45 OF 71	

FAN CONNECTOR

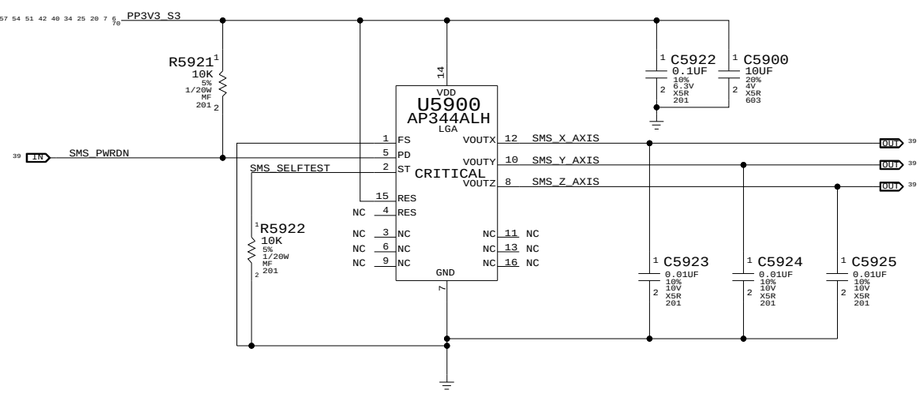


Fan	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

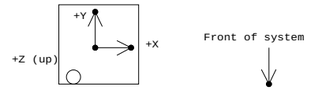
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 46 OF 71	

SUDDEN MOTION SENSOR



Desired orientation when placed on board top-side:



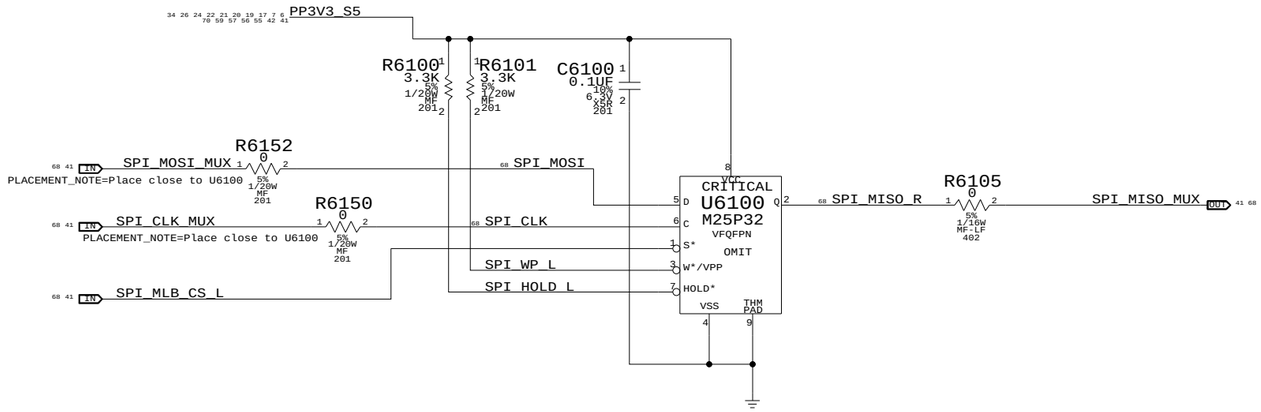
Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 47 OF 71	



SPI ROM

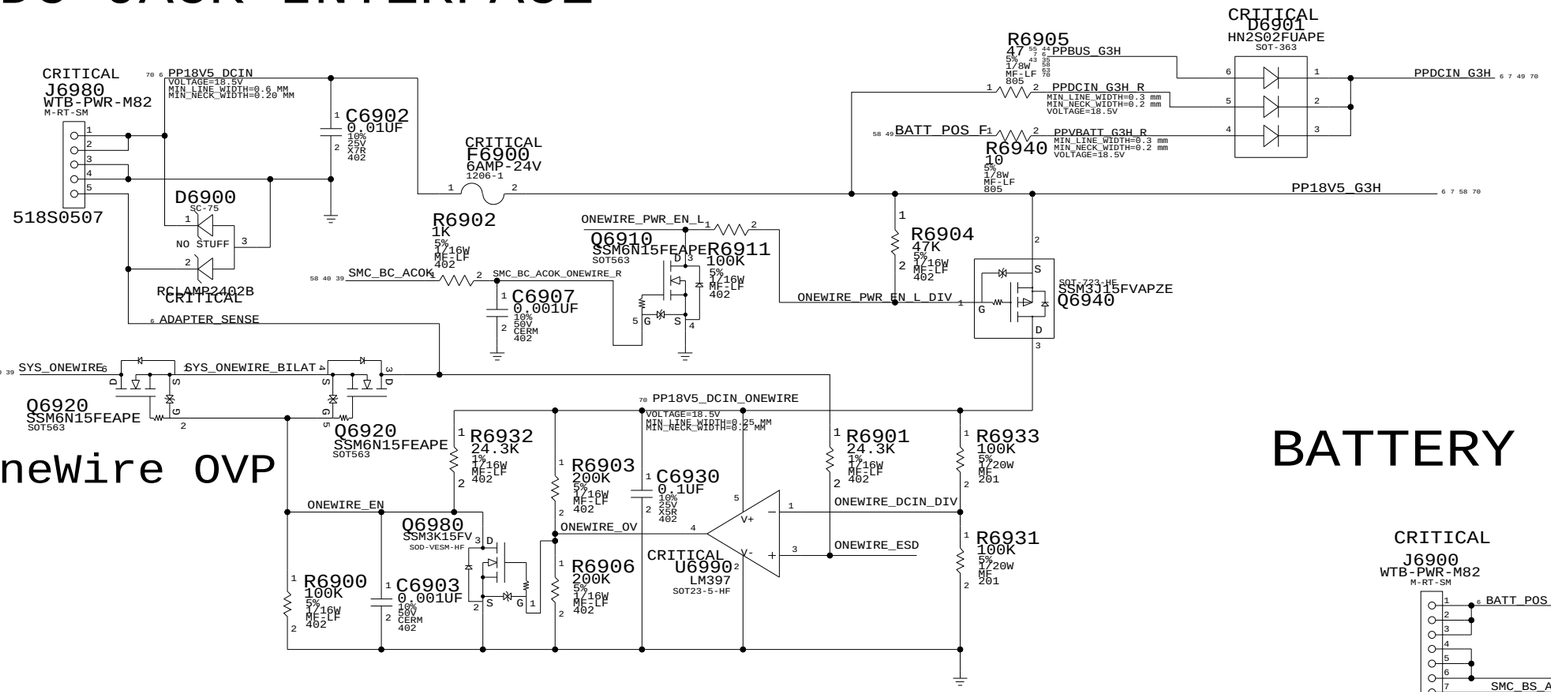
SYNC_MASTER=CHANGZHANG SYNC_DATE=02/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

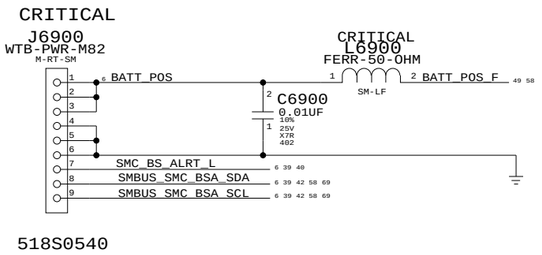
SCALE	SHT	OF
NONE	48	71

DC-JACK INTERFACE



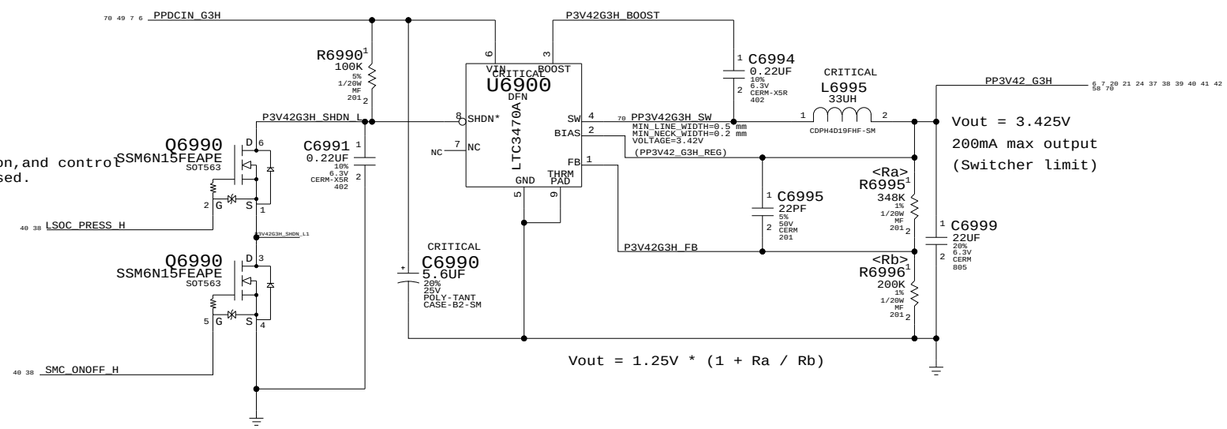
OneWire OVP

BATTERY INTERFACE



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Q6990 will pull down P3V42G3H_SHDN_L in the event of a keyboard SMC Reset generated when left shift,option,and control and the power button is depressed.

Vout = 3.425V
200mA max output
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

DC-In & Battery Connectors		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	
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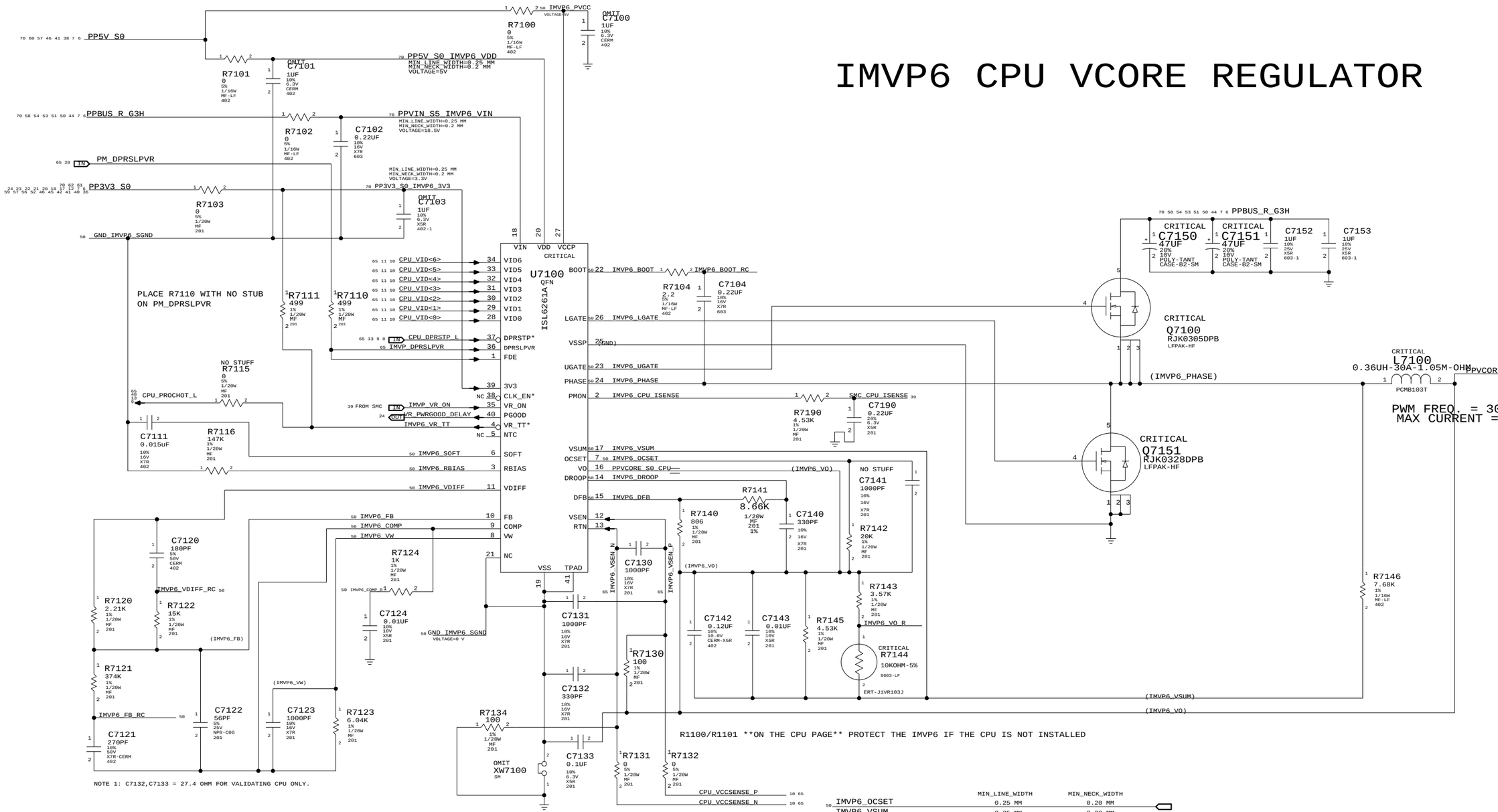
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7631
	REV: A.0.0	
	SCALE: NONE	SHT 49 OF 71

IMVP6 CPU VCORE REGULATOR



NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE	1.5 MM	0.20 MM
IMVP6_BOOT	0.25 MM	0.20 MM
IMVP6_UGATE	1.5 MM	0.20 MM
IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
PPVCORE_S0_CPU	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_PVCC	0.25 MM	0.20 MM
IMVP6_COMP_R	0.25 MM	0.20 MM
IMVP6_FB_RC	0.25 MM	0.20 MM
IMVP6_VDIFF_RC	0.25 MM	0.20 MM

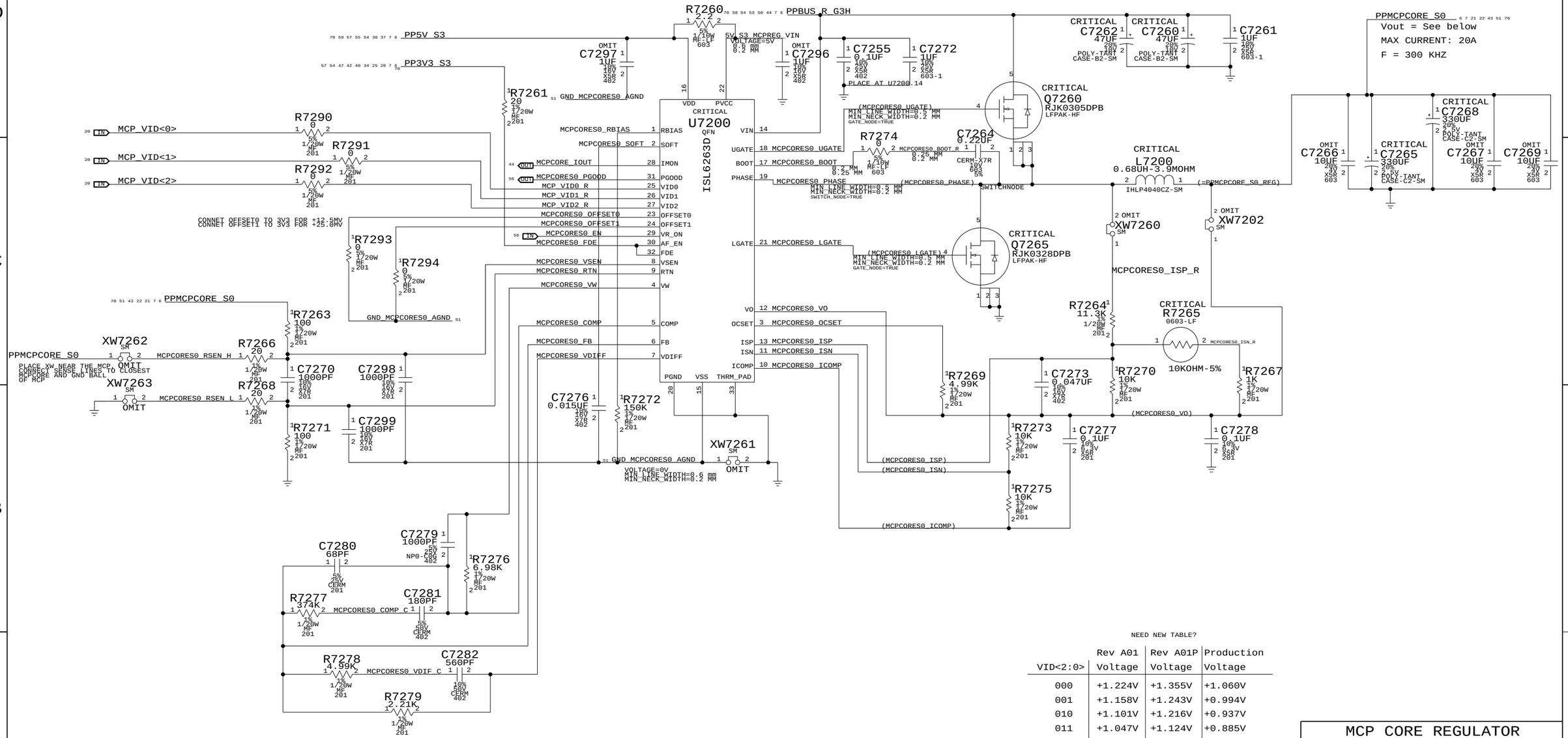
IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 50 OF 71	

MCP CORE POWER SUPPLY



NEED NEW TABLE?

VID<2:0>	Rev A01 Voltage	Rev A01P Voltage	Production Voltage
000	+1.224V	+1.355V	+1.060V
001	+1.158V	+1.243V	+0.994V
010	+1.101V	+1.216V	+0.937V
011	+1.047V	+1.124V	+0.885V
100	+0.996V	+1.065V	+0.830V
101	+0.952V	+0.994V	+0.789V
110	+0.913V	+0.977V	+0.752V
111	+0.876V	+0.917V	+0.719V

(Also A01Q)

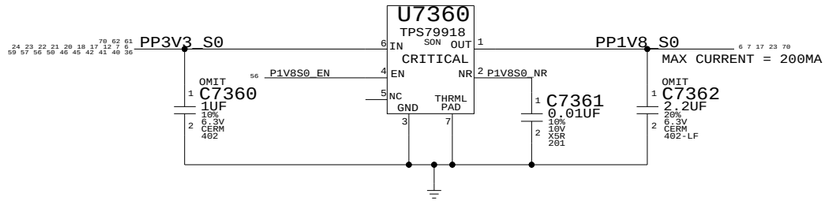
MCP CORE REGULATOR

SYNC_MASTER=MINGJING SYNC_DATE=06/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 51 OF 71	

1.8V S0 LDO



1.8V LDO Supply

SYNC_MASTER= SYNC_DATE=

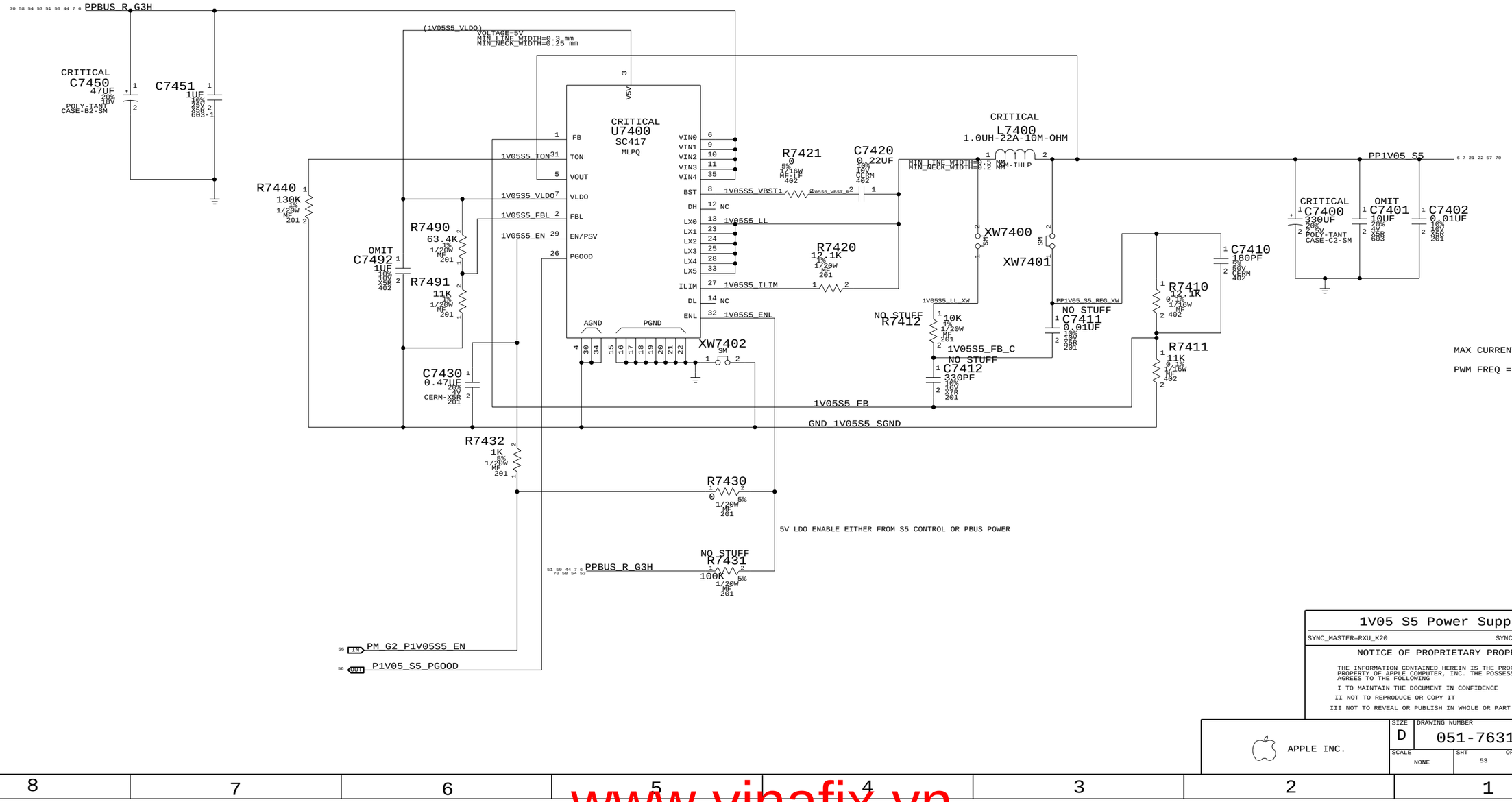
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

SCALE	SHT	OF
NONE	52	71

1V05 S5 POWER SUPPLY

supply for MCP1V05 AUX, FSB (CPU & MCP) VTT, 1V05 S0



1V05 S5 Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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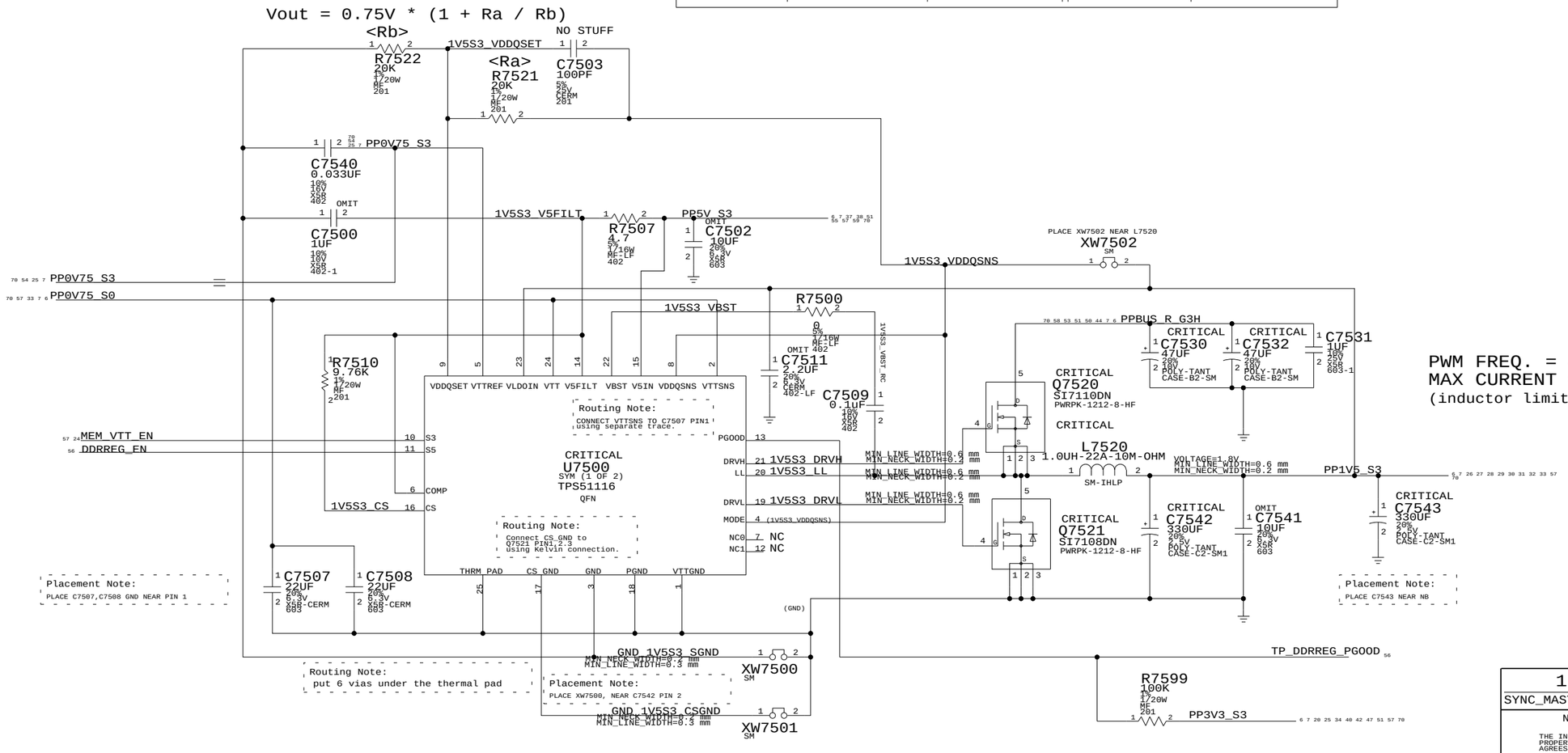
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 53 OF 71	

1.5V/0.75V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



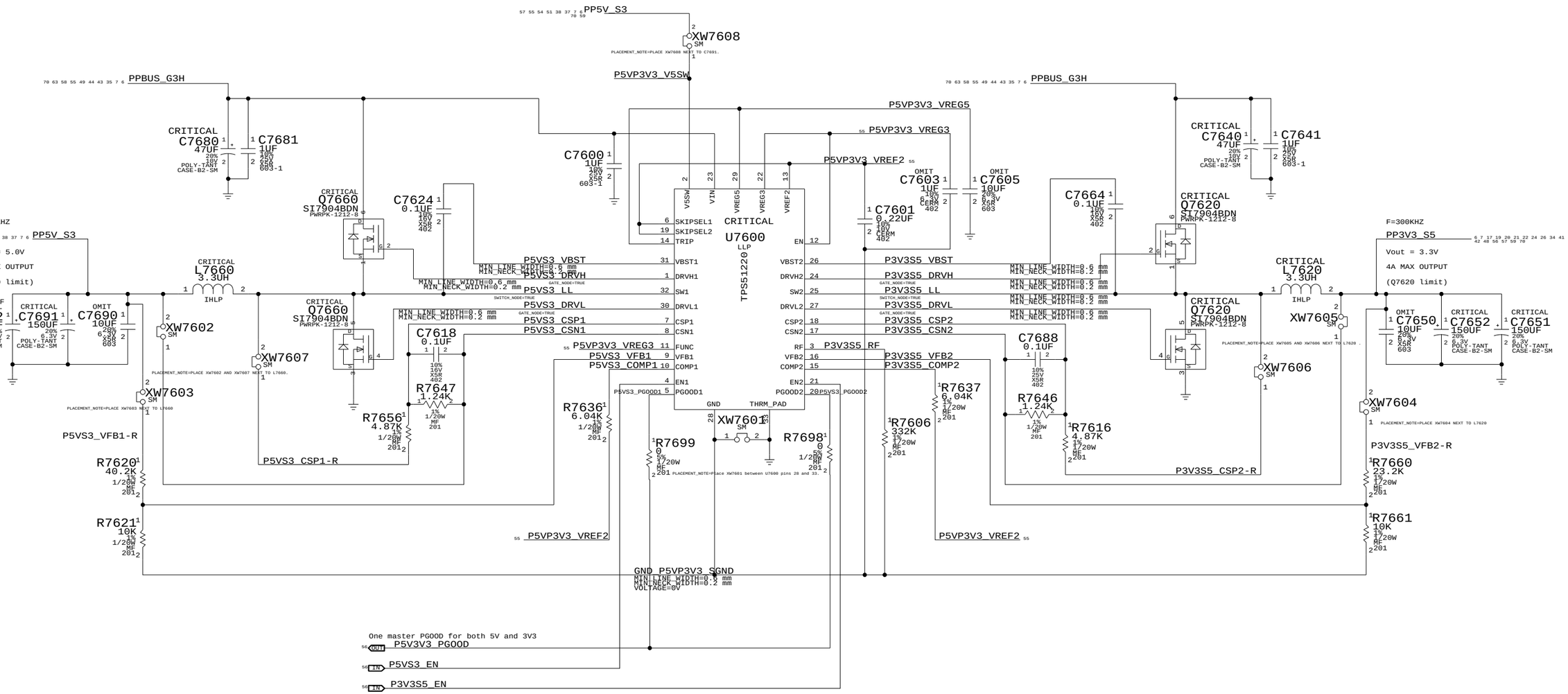
1.5V/0.75V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 54 OF 71	

5V_S3 / 3V3_S5 POWER SUPPLY



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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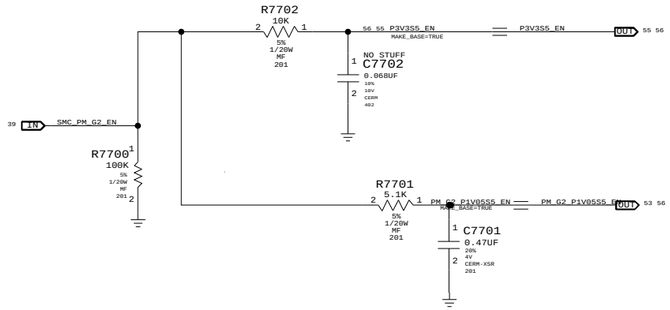
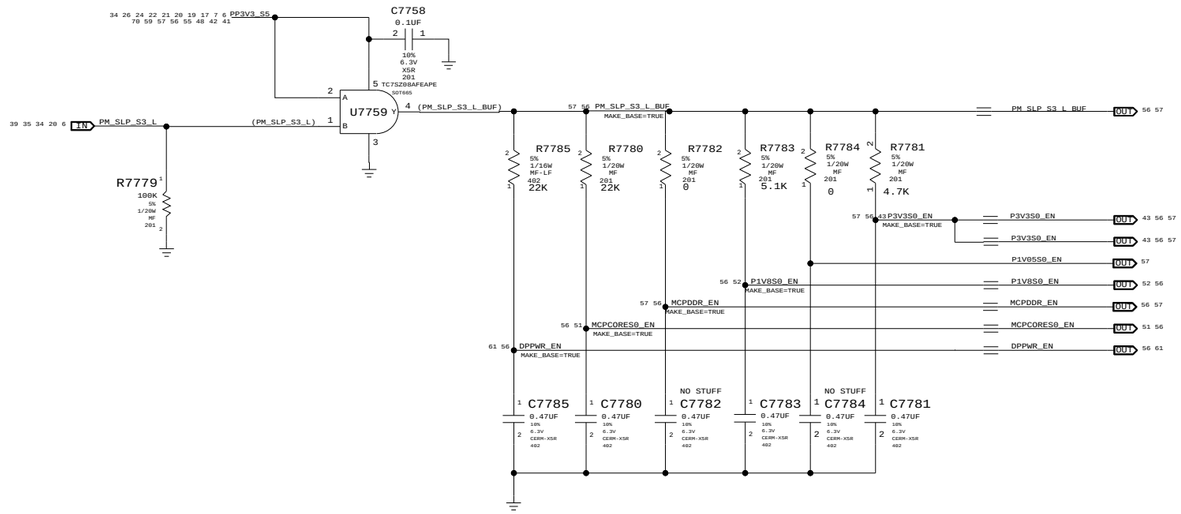
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 55 OF 71	

Power Control Signals

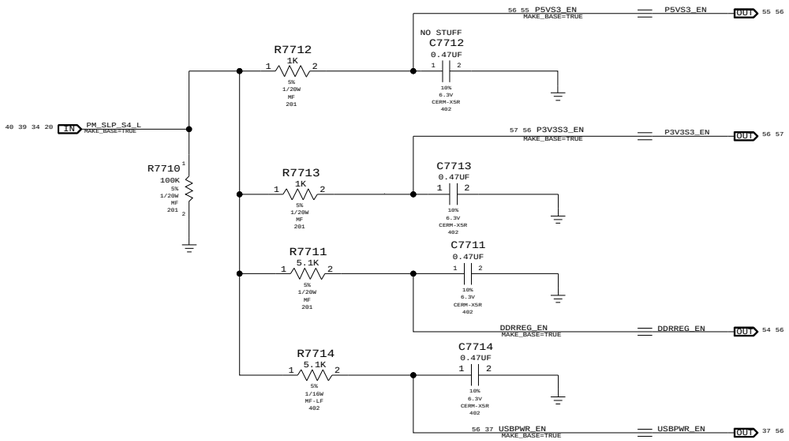
S5 ENABLE



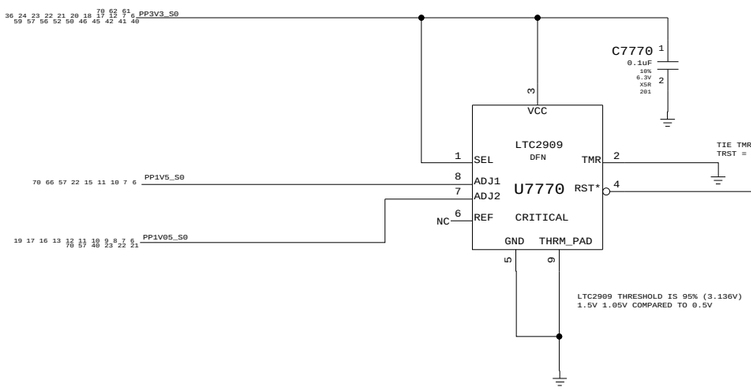
S0 ENABLE



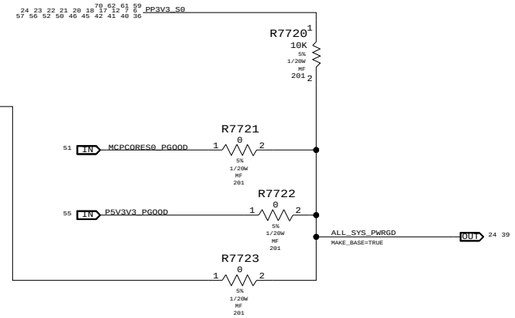
S3 ENABLE



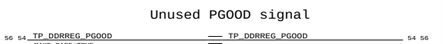
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

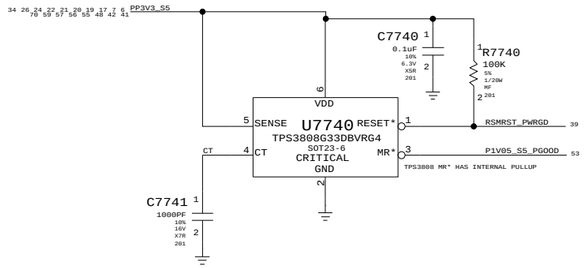


OTHER S0 RAILS PGOOD



Unused PGOOD signal





POWER SEQUENCING

SYNC_MASTER=YUAN.MA SYNC_DATE=02/04/2008

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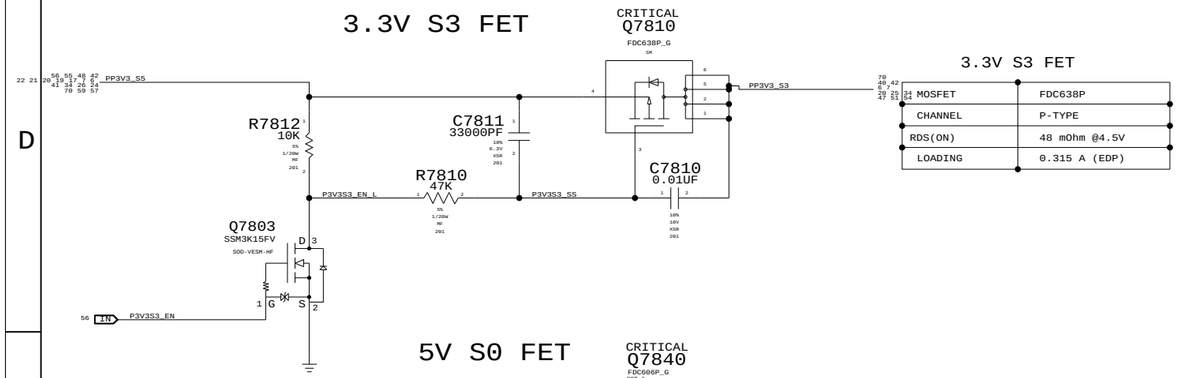
APPLE INC.

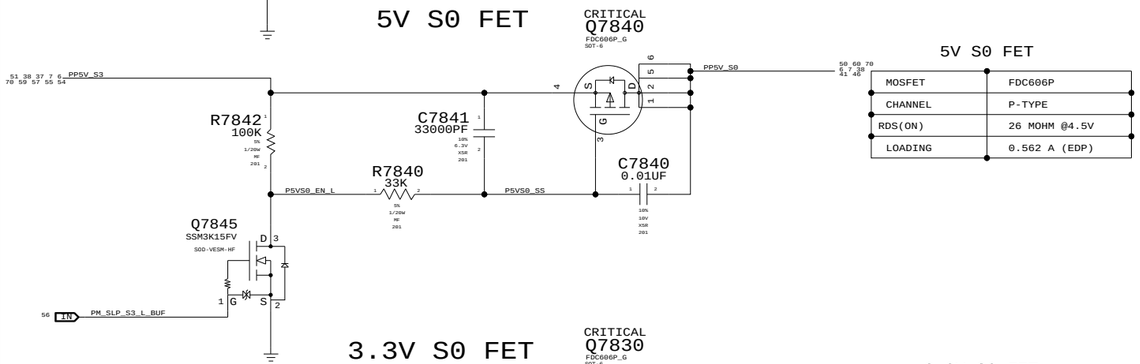
SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 56 OF 71	

3.3V S3 FET



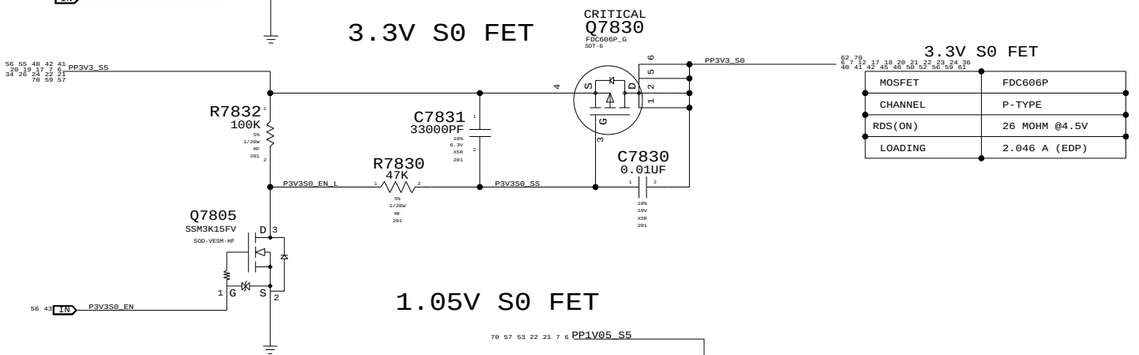
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.315 A (EDP)

5V S0 FET



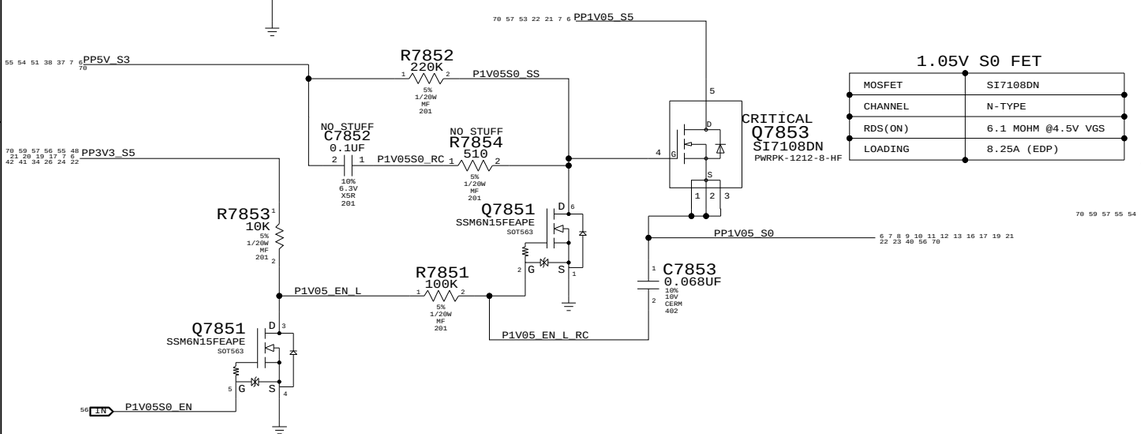
5V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	0.562 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	2.046 A (EDP)

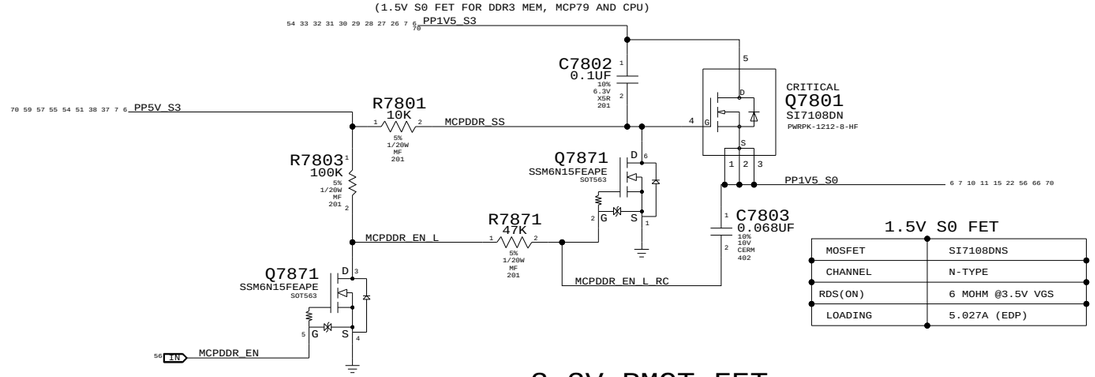
1.05V S0 FET



1.05V S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6.1 MOHM @4.5V VGS
LOADING	8.25A (EDP)

1.5V S0 FET

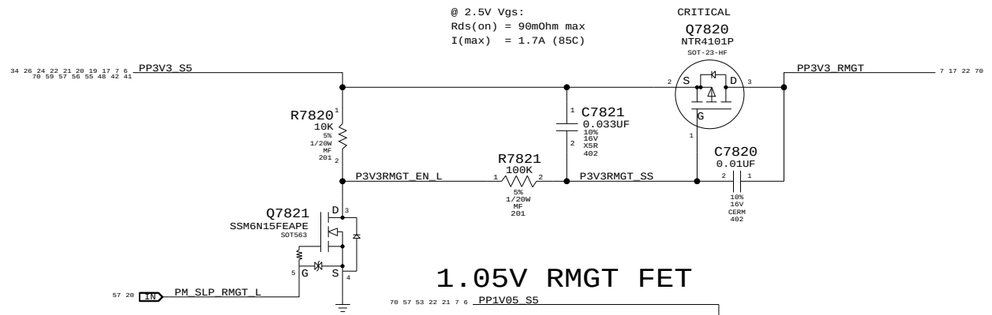
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



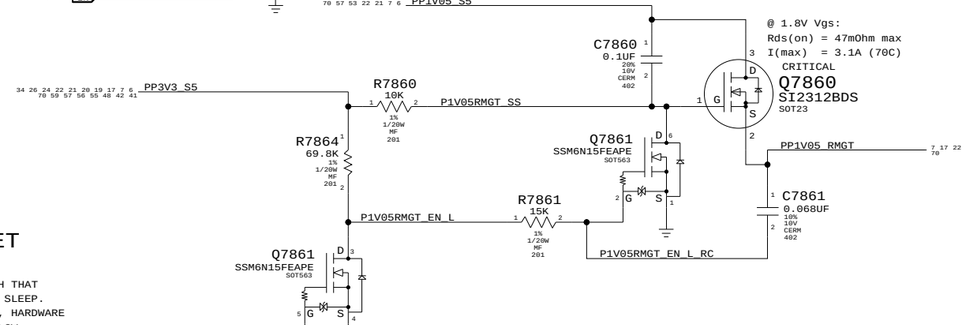
1.5V S0 FET	
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5.027A (EDP)

3.3V RMGT FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

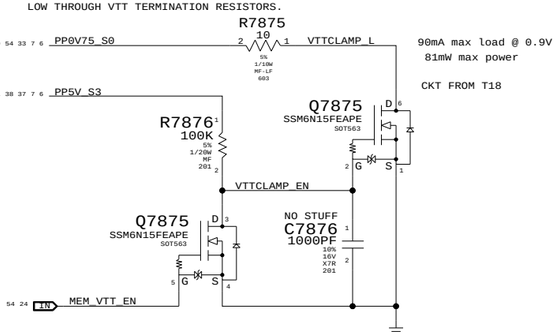


1.05V RMGT FET



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



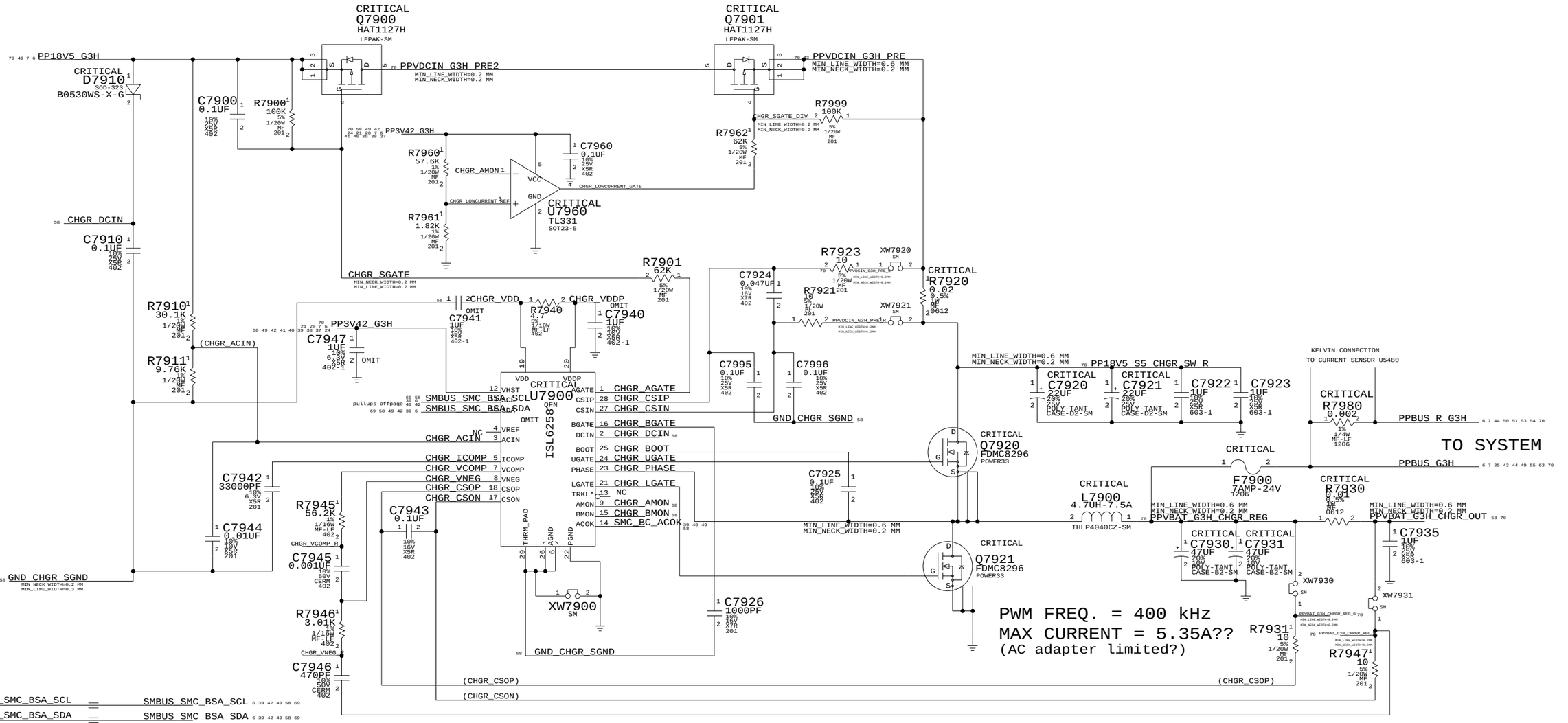
POWER FETS

SYNC_MASTER=YUAN.MA SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 57 OF 71	

PBUS SUPPLY / BATTERY CHARGER



PBUS Supply/Battery Charger			
SYNC_MASTER=M70	SYNC_DATE=01/09/2007		
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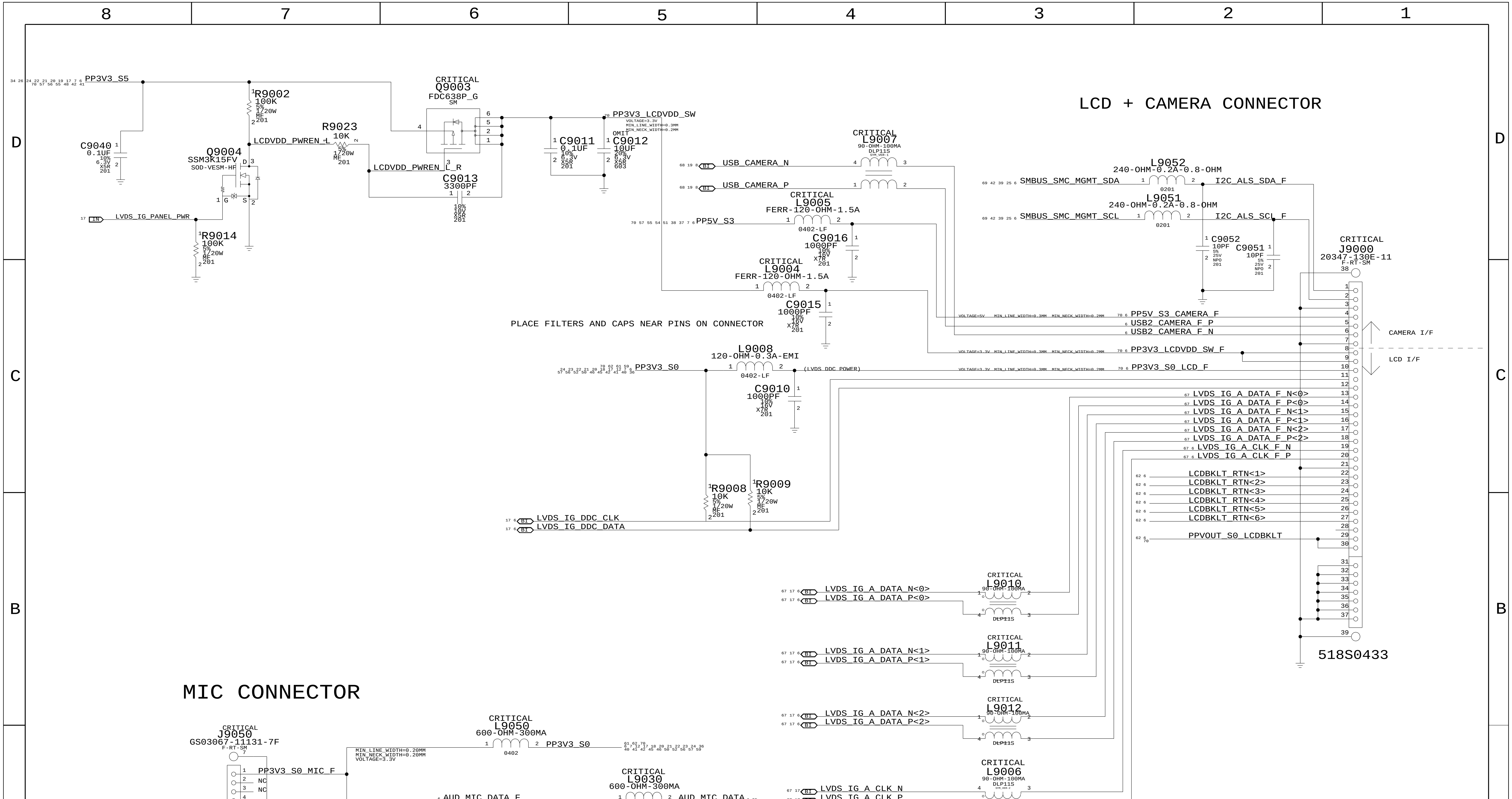
APPLE INC.	SIZE D	DRAWING NUMBER 051-7631	REV. A.0.0
	SCALE NONE	SHT 58 OF 71	


LCD + CAMERA CONNECTOR
MIC CONNECTOR
PLACE FILTERS AND CAPS NEAR PINS ON CONNECTOR
APN:518S0536
518S0433
PP3V3_S5
R9002 100K
Q9003 FDC638P_G
Q9004 SSM3K15FV
R9023 10K
LCDVDD_PWREN_L
LCDVDD_PWREN_L_R
C9013 3300PF
C9040 0.1UF
R9014 100K
LVDS_IG_PANEL_PWR
PP3V3_LCDVDD_SW
C9011 0.1UF
C9012 10UF
USB_CAMERA_N
USB_CAMERA_P
L9007 90-OHM-100MA
L9005 FERR-120-OHM-1.5A
PP5V_S3
C9016 1000PF
L9004 FERR-120-OHM-1.5A
C9015 1000PF
L9052 240-OHM-0.2A-0.8-OHM
L9051 240-OHM-0.2A-0.8-OHM
SMBUS_SMC_MGMT_SDA
SMBUS_SMC_MGMT_SCL
I2C_ALS_SDA_F
I2C_ALS_SCL_F
C9052 10PF
C9051 10PF
J9000 20347-130E-11
PP5V_S3_CAMERA_F
USB2_CAMERA_F_P
USB2_CAMERA_F_N
PP3V3_LCDVDD_SW_F
PP3V3_S0_LCD_F
CAMERA I/F
LCD I/F
L9008 120-OHM-0.3A-EMI
PP3V3_S0
(LVDS DDC POWER)
C9010 1000PF
LVDS_IG_A_DATA_F_N<0>
LVDS_IG_A_DATA_F_P<0>
LVDS_IG_A_DATA_F_N<1>
LVDS_IG_A_DATA_F_P<1>
LVDS_IG_A_DATA_F_N<2>
LVDS_IG_A_DATA_F_P<2>
LVDS_IG_A_CLK_F_N
LVDS_IG_A_CLK_F_P
LCDBKLT_RTN<1>
LCDBKLT_RTN<2>
LCDBKLT_RTN<3>
LCDBKLT_RTN<4>
LCDBKLT_RTN<5>
LCDBKLT_RTN<6>
PPVOUT_S0_LCDBKLT
R9008 10K
R9009 10K
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
L9010 90-OHM-100MA
LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<0>
L9011 90-OHM-100MA
LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<1>
L9012 90-OHM-100MA
LVDS_IG_A_DATA_N<2>
LVDS_IG_A_DATA_P<2>
L9006 90-OHM-100MA
LVDS_IG_A_CLK_N
LVDS_IG_A_CLK_P
J9050 GS03067-11131-7F
L9050 600-OHM-300MA
PP3V3_S0_MIC_F
AUD_MIC_DATA_F
AUD_MIC_CLK_F
GND_MIC_F
L9030 600-OHM-300MA
AUD_MIC_DATA
L9031 600-OHM-300MA
AUD_MIC_CLK
L9053 600-OHM-300MA
C9050 0.01UF
C9053 0.01UF
C9030 10PF
C9031 10PF
NO STUFF

LVDS,Camera Conn. and ALS Conn.

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
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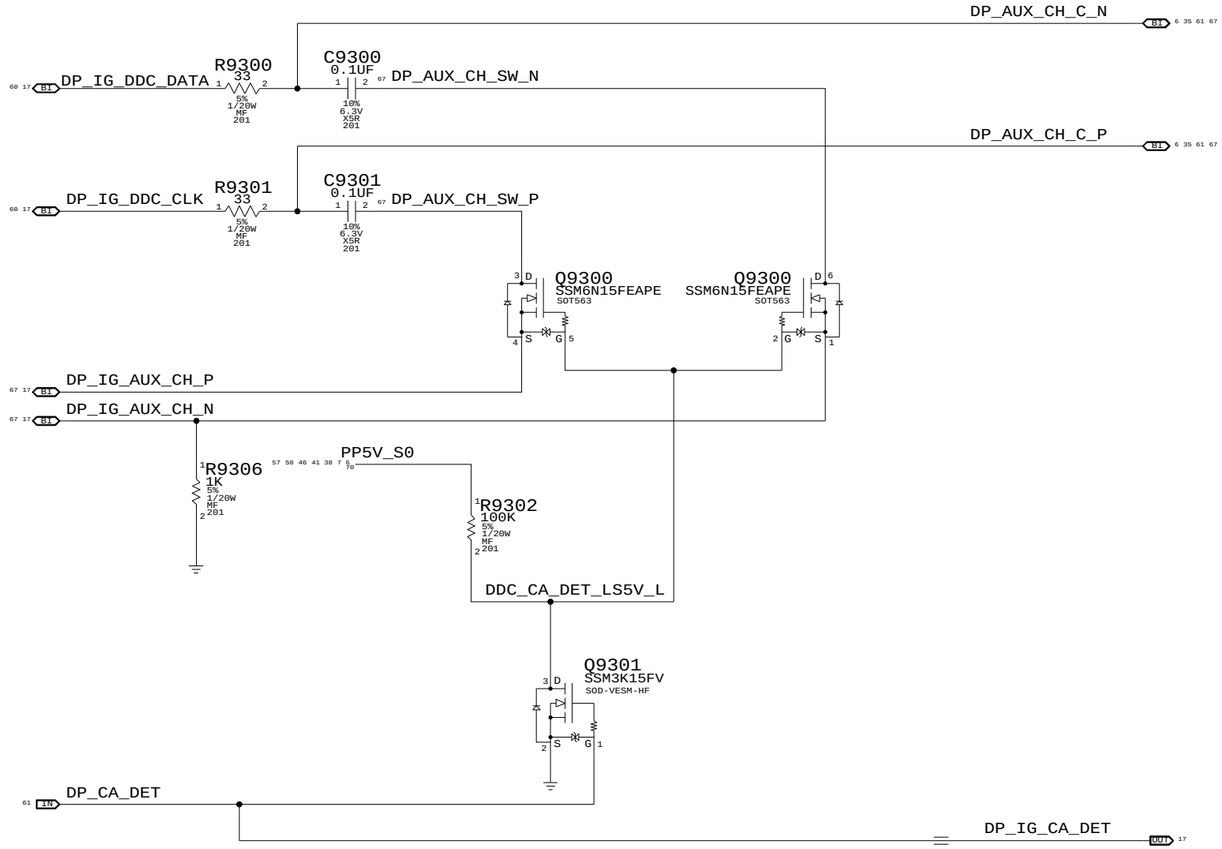



```
17 =MCP_HDMI_TXC_P          DP_ML_P<3>          61 67  MAKE_BASE=TRUE
17 =MCP_HDMI_TXC_N          DP_ML_N<3>          61 67  MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_P<0>       DP_ML_P<2>          61 67  MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_N<0>       DP_ML_N<2>          61 67  MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_P<1>       DP_ML_P<1>          61 67  MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_N<1>       DP_ML_N<1>          61 67  MAKE_BASE=TRUE
67 61 60 17 DP_ML_P<0>      DP_ML_P<0>          17 60 61 67  MAKE_BASE=TRUE
67 61 60 17 DP_ML_N<0>      DP_ML_N<0>          17 60 61 67  MAKE_BASE=TRUE
61 60 17 DP_HPD             DP_HPD              17 60 61  MAKE_BASE=TRUE
60 17 DP_IG_DDC_CLK         DP_IG_DDC_CLK       17 60  MAKE_BASE=TRUE
60 17 DP_IG_DDC_DATA        DP_IG_DDC_DATA      17 60  MAKE_BASE=TRUE
```

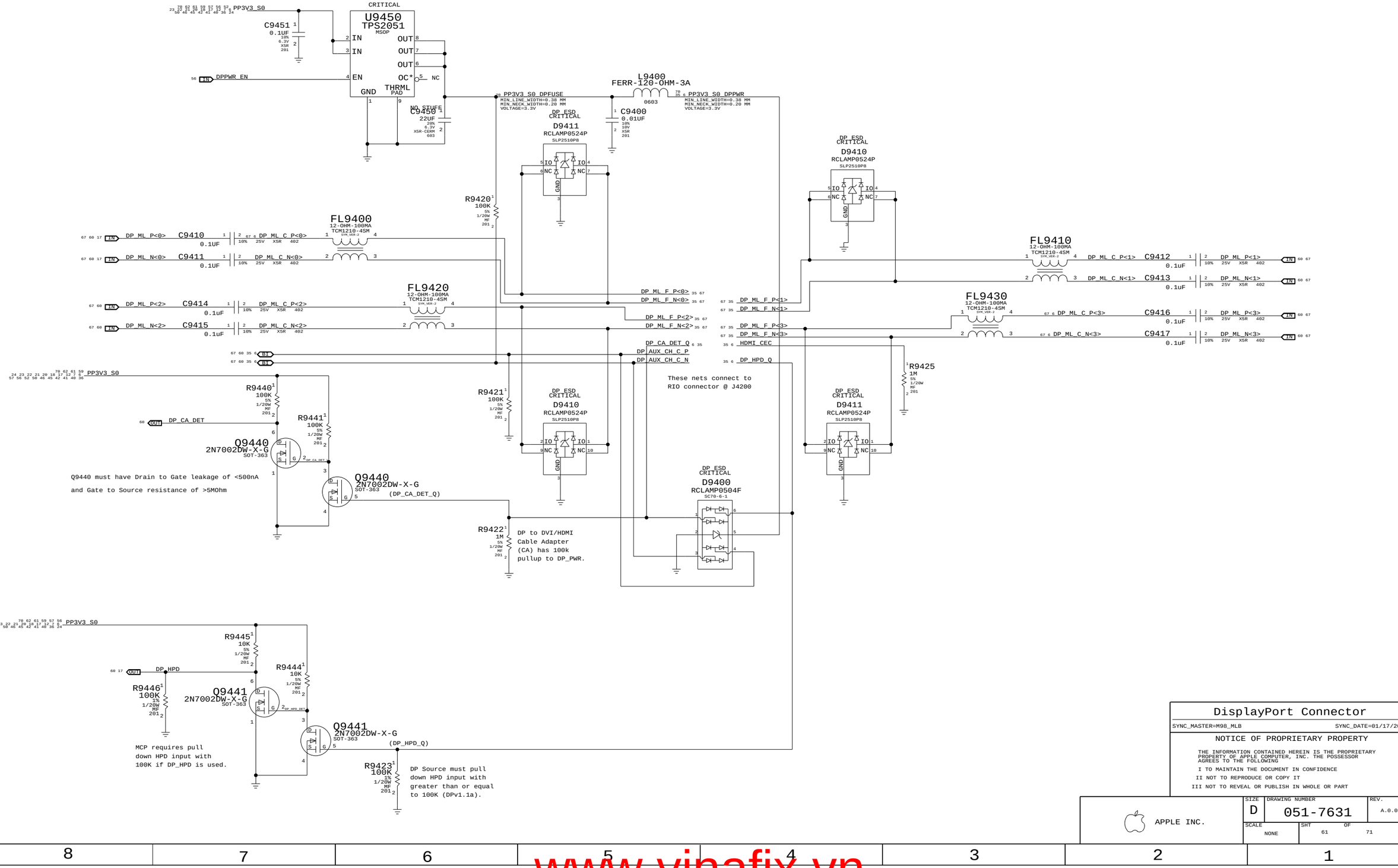
DISPLAYPORT SUPPORT

SYNC_MASTER=NMARTIN SYNC_DATE=12/18/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 60 OF 71	



DisplayPort Connector

SYNC_MASTER=M98_MLB SYNC_DATE=01/17/2008

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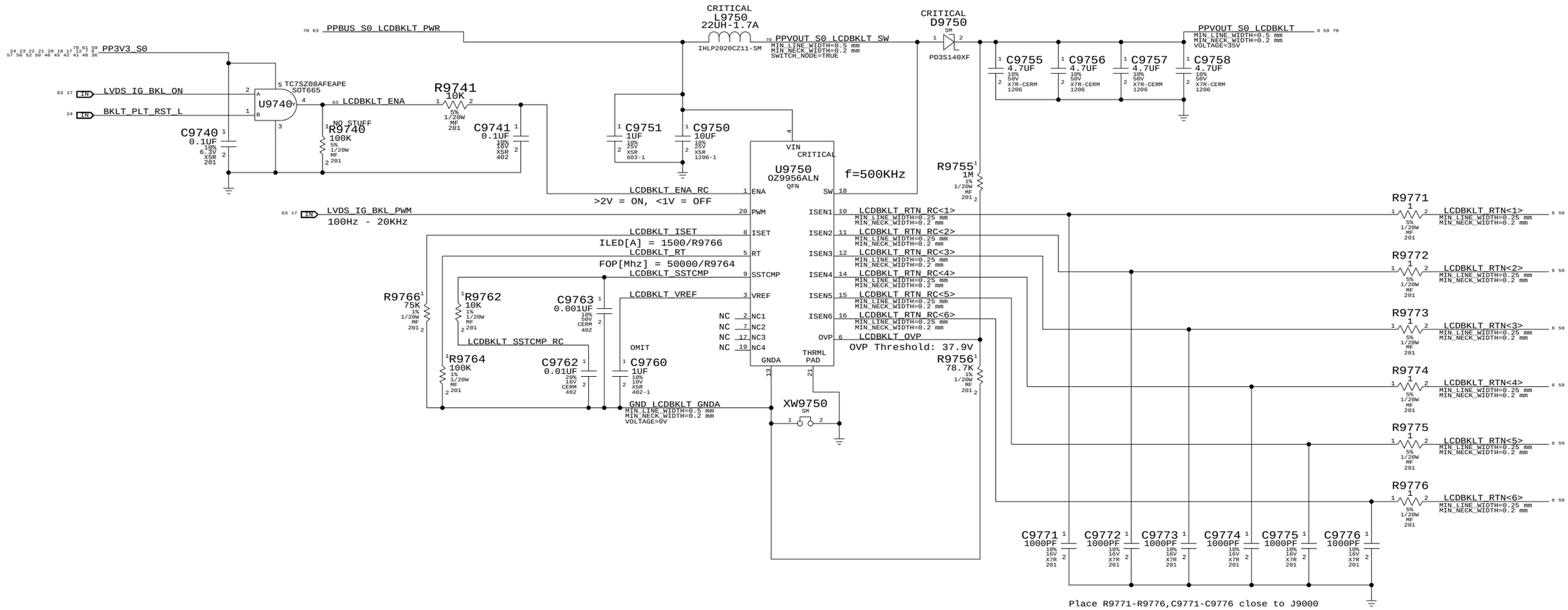
SCALE: NONE	SHT 61 OF 71	

LED Backlight Driver



LED Backlight Driver

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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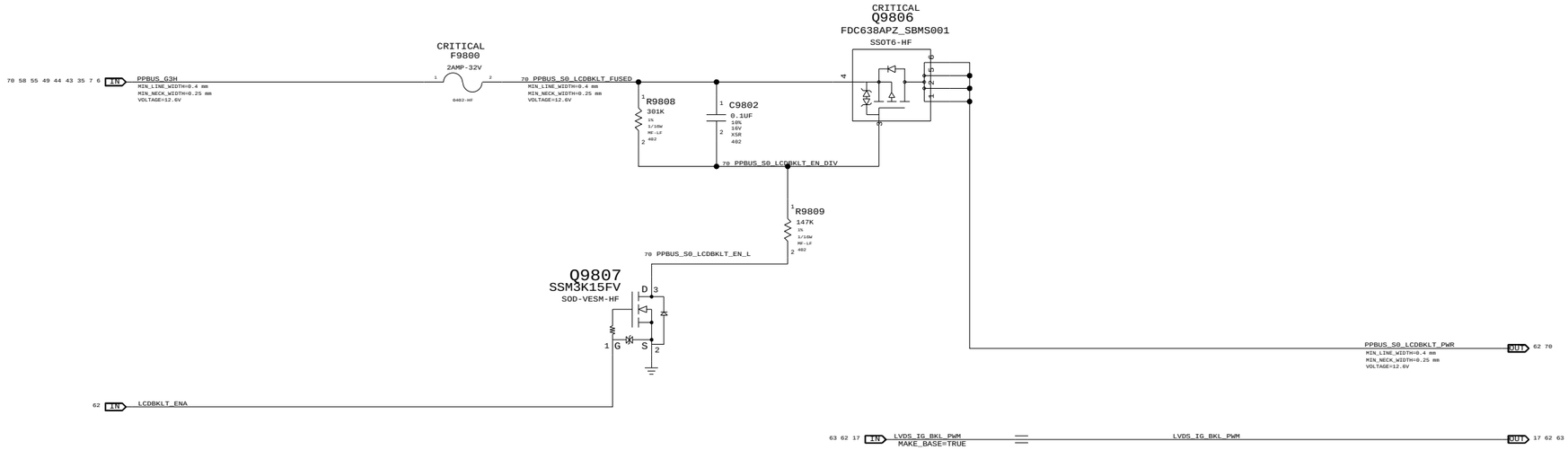
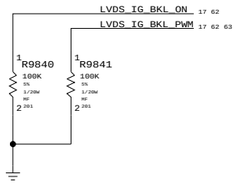
SCALE: NONE	SHT 62 OF 71	





LCD Backlight Support

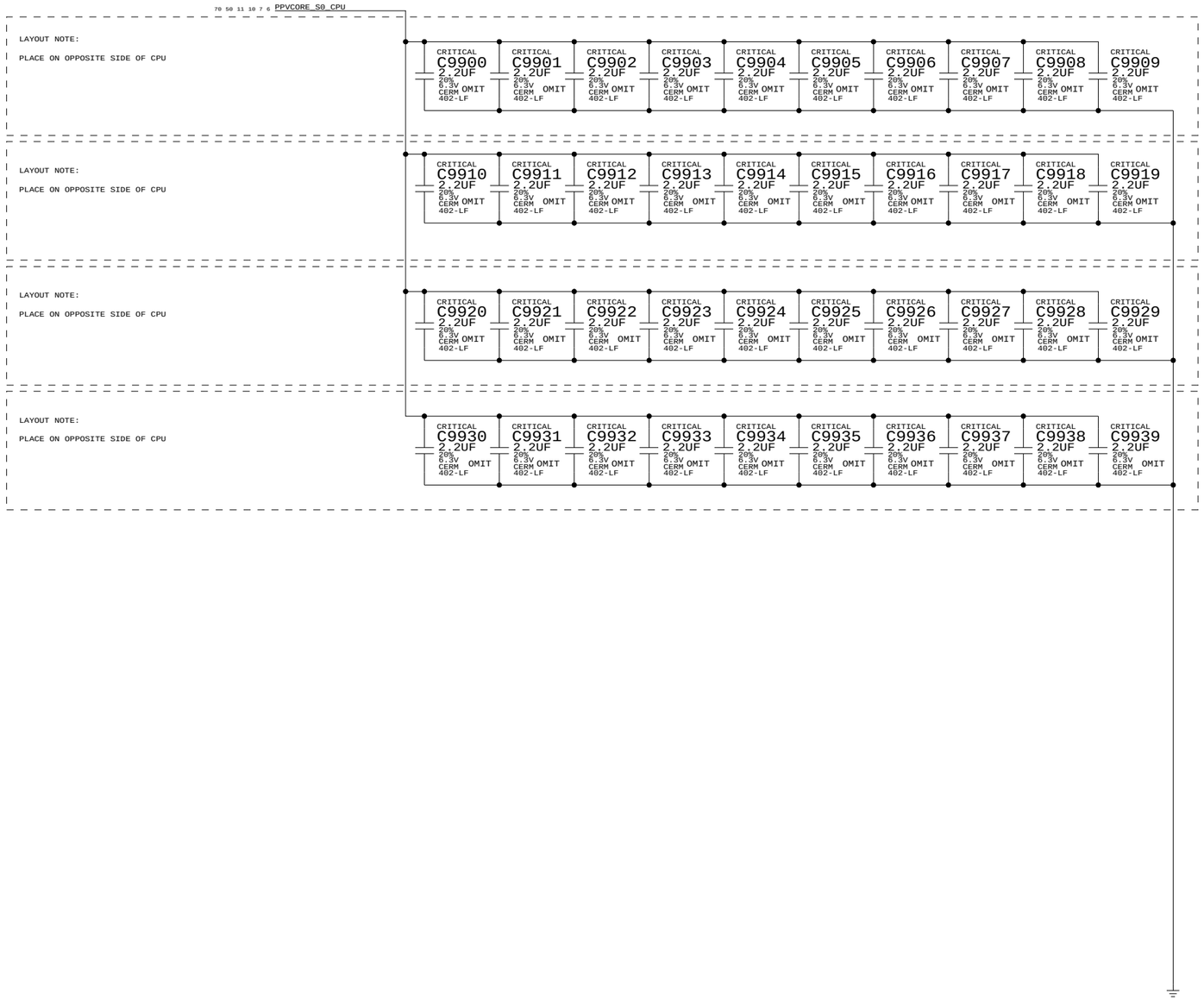
SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 63 OF 71	

ADDITIONAL CPU VCORE HF DECOUPLING

40x 2.2uF 0402



Additional CPU/GPU Decoupling

SYNC_MASTER= SYNC_DATE=

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 64 OF 71	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	9 13
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	9 13
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	9 13
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	9 13
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	9 13
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	9 13
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	9 13
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	9 13
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	8 9 13
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	13
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	9 13
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	8 9 12 13
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9 13
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8 9
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9 13
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	8 9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	8 9 13
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9 13 40 50
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9 12 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9 13
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9 13 40
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9 13
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9 13
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	8 9 13 50
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9 13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9 13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	6 12 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	6 12 13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13
	CPU_IERR_L	CPU_50S		CPU_IERR_L	9
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	20 50
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	50
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9 25
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 9 12
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	9 12
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 9 12
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 9 12
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 9 12
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	6 9 12
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	6 9 12
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	6 12
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	10 11 50
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	11
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10 50
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10 50
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	50
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	50

CPU/FSB Constraints

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 65 OF 71	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	0.110 MM	=50_OHM_SE	=STANDARD	=STANDARD
MEM_50S_VDD	*	=50_OHM_SE	=50_OHM_SE	0.110 MM	=50_OHM_SE	=STANDARD	=STANDARD
MEM_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
MEM_90D_VDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=2.28:1_SPACING	?
MEM_CTRL2CTRL	*	=1.1:1_SPACING	?
MEM_CTRL2MEM	*	=2.28:1_SPACING	?
MEM_CMD2CMD	*	=1.1:1_SPACING	?
MEM_CMD2MEM	*	=2.28:1_SPACING	?
MEM_DATA2DATA	*	=1.1:1_SPACING	?
MEM_DATA2MEM	*	=2.28:1_SPACING	?
MEM_DQS2MEM	*	=2.28:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V5_MEM	*	PWR_P2MM
MEM_CTRL	PP1V5_MEM	*	PWR_P2MM
MEM_DATA	PP1V5_MEM	*	PWR_P2MM
MEM_DQS	PP1V5_MEM	*	PWR_P2MM
MEM_CMD	PP1V5_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	PWR	*	BUS2PWR_GND
MEM_CLK	GND	*	BUS2PWR_GND
MEM_CTRL	PWR	*	BUS2PWR_GND
MEM_CTRL	GND	*	BUS2PWR_GND
MEM_CMD	PWR	*	BUS2PWR_GND
MEM_CMD	GND	*	BUS2PWR_GND
MEM_DATA	PWR	*	BUS2PWR_GND
MEM_DATA	GND	*	BUS2PWR_GND
MEM_DQS	PWR	*	BUS2PWR_GND
MEM_DQS	GND	*	BUS2PWR_GND

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_90D	MEM_CLK	MEM_A_CLK_P<0>	14 27 28 33
MEM_A_CLK	MEM_90D	MEM_CLK	MEM_A_CLK_N<0>	14 27 28 33
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CKE<1..0>	14 27 28 33
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CS_L<1..0>	14 27 28 33
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_ODT<1..0>	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_A<14..0>	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_BA<2..0>	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_RAS_L	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_CAS_L	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_WE_L	14 27 28 33
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	14 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	14 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	14 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	14 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	14 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	14 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	14 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	14 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0>	14 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1>	14 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2>	14 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3>	14 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4>	14 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5>	14 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6>	14 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7>	14 28
MEM_A_DQS0	MEM_90D	MEM_DQS	MEM_A_DQS_P<0>	14 27
MEM_A_DQS0	MEM_90D	MEM_DQS	MEM_A_DQS_N<0>	14 27
MEM_A_DQS1	MEM_90D	MEM_DQS	MEM_A_DQS_P<1>	14 27
MEM_A_DQS1	MEM_90D	MEM_DQS	MEM_A_DQS_N<1>	14 27
MEM_A_DQS2	MEM_90D	MEM_DQS	MEM_A_DQS_P<2>	14 27
MEM_A_DQS2	MEM_90D	MEM_DQS	MEM_A_DQS_N<2>	14 27
MEM_A_DQS3	MEM_90D	MEM_DQS	MEM_A_DQS_P<3>	14 27
MEM_A_DQS3	MEM_90D	MEM_DQS	MEM_A_DQS_N<3>	14 27
MEM_A_DQS4	MEM_90D	MEM_DQS	MEM_A_DQS_P<4>	14 28
MEM_A_DQS4	MEM_90D	MEM_DQS	MEM_A_DQS_N<4>	14 28
MEM_A_DQS5	MEM_90D	MEM_DQS	MEM_A_DQS_P<5>	14 28
MEM_A_DQS5	MEM_90D	MEM_DQS	MEM_A_DQS_N<5>	14 28
MEM_A_DQS6	MEM_90D	MEM_DQS	MEM_A_DQS_P<6>	14 28
MEM_A_DQS6	MEM_90D	MEM_DQS	MEM_A_DQS_N<6>	14 28
MEM_A_DQS7	MEM_90D	MEM_DQS	MEM_A_DQS_P<7>	14 28
MEM_A_DQS7	MEM_90D	MEM_DQS	MEM_A_DQS_N<7>	14 28
MEM_B_CLK	MEM_90D	MEM_CLK	MEM_B_CLK_P<0>	14 29 30 33
MEM_B_CLK	MEM_90D	MEM_CLK	MEM_B_CLK_N<0>	14 29 30 33
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CKE<1..0>	14 29 30 33
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CS_L<1..0>	14 29 30 33
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_ODT<1..0>	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_A<14..0>	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_BA<2..0>	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_RAS_L	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_CAS_L	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_WE_L	14 29 30 33
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	14 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	14 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	14 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	14 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	14 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	14 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	14 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	14 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0>	14 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1>	14 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2>	14 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3>	14 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4>	14 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5>	14 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6>	14 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7>	14 30
MEM_B_DQS0	MEM_90D	MEM_DQS	MEM_B_DQS_P<0>	14 29
MEM_B_DQS0	MEM_90D	MEM_DQS	MEM_B_DQS_N<0>	14 29
MEM_B_DQS1	MEM_90D	MEM_DQS	MEM_B_DQS_P<1>	14 29
MEM_B_DQS1	MEM_90D	MEM_DQS	MEM_B_DQS_N<1>	14 29
MEM_B_DQS2	MEM_90D	MEM_DQS	MEM_B_DQS_P<2>	14 29
MEM_B_DQS2	MEM_90D	MEM_DQS	MEM_B_DQS_N<2>	14 29
MEM_B_DQS3	MEM_90D	MEM_DQS	MEM_B_DQS_P<3>	14 29
MEM_B_DQS3	MEM_90D	MEM_DQS	MEM_B_DQS_N<3>	14 29
MEM_B_DQS4	MEM_90D	MEM_DQS	MEM_B_DQS_P<4>	14 30
MEM_B_DQS4	MEM_90D	MEM_DQS	MEM_B_DQS_N<4>	14 30
MEM_B_DQS5	MEM_90D	MEM_DQS	MEM_B_DQS_P<5>	14 30
MEM_B_DQS5	MEM_90D	MEM_DQS	MEM_B_DQS_N<5>	14 30
MEM_B_DQS6	MEM_90D	MEM_DQS	MEM_B_DQS_P<6>	14 30
MEM_B_DQS6	MEM_90D	MEM_DQS	MEM_B_DQS_N<6>	14 30
MEM_B_DQS7	MEM_90D	MEM_DQS	MEM_B_DQS_P<7>	14 30
MEM_B_DQS7	MEM_90D	MEM_DQS	MEM_B_DQS_N<7>	14 30
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD VOLTAGE=0V	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND VOLTAGE=1.5V	15
		MEM_CLK	MEM_RESET_L	30 26 27 28 29

PP1V5_S0 NET_SPACING_TYPE=PP1V5_MEM
GND NET_SPACING_TYPE=GND

SYNC_MASTER=M97	SYNC_DATE=02/04/2008

Memory Constraints

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0
SCALE: NONE	SHT 66 OF 71	

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_E_R2D_C_P	16 34
	PCIE_90D	PCIE	PCIE_E_R2D_C_N	16 34
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_E_D2R_P	16 34
	PCIE_90D	PCIE	PCIE_E_D2R_N	16 34
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_N	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	
	PCIE_90D	PCIE	PCIE_FC_R2D_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_N	
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
	PCIE_90D	PCIE	PCIE_FC_D2R_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	TP_PEG_CLK100M_P	8 16
	CLK_PCIE_100D	CLK_PCIE	TP_PEG_CLK100M_N	8 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16 34
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	6 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	6 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_F_P<3..0>	35 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_F_N<3..0>	35 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	17 60 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	17 60 61
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17 60
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17 60
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	6 35 60 61
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	6 35 60 61
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	60
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	60
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17 23
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17 23
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6 59
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6 59
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17 59
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17 59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_F_P<2..0>	59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_F_N<2..0>	59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6 17 59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6 17 59
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_A_DATA_P3	8 17
LVDS_IG_A_DATA3	LVDS_100D	LVDS	NC_LVDS_IG_A_DATA_N3	8 17
LVDS_IG_B_CLK	LVDS_100D	LVDS	NC_LVDS_IG_B_CLK_P	8 17
LVDS_IG_B_CLK	LVDS_100D	LVDS	NC_LVDS_IG_B_CLK_N	8 17
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	17
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	17
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	17
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	17
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 23
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 23
SATA_HDD_R2D	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P	19 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N	19 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_P	6 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_N	6 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P	36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N	36
SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA_HDD_D2R_P	19 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_N	19 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P	6 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N	6 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_P	36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_N	36
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19

MCP Constraints 1

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 6 12 18
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 18
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 18
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 18
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 18
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 18 39 41
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 18 39 41
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 18 24
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 18 24
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 24 39
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 24 41
USB_EXTA	USB_90D	USB	USB_EXTA_P 8 19 37
	USB_90D	USB	USB_EXTA_N 8 19 37
	USB_90D	USB	USB_EXTA_MUXED_P 37
	USB_90D	USB	USB_EXTA_MUXED_N 37
	USB_90D	USB	CONN_USB_EXTA_P
	USB_90D	USB	CONN_USB_EXTA_N
USB_MINI	USB_90D	USB	USB_MINI_P 8 19
	USB_90D	USB	TP_USB_MINI_N 8 19
USB_EXTD	USB_90D	USB	TP_USB_EXTD_P 8 19
	USB_90D	USB	TP_USB_EXTD_N 8 19
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 8 19 59
	USB_90D	USB	USB_CAMERA_N 8 19 59
	USB_90D	USB	USB_CAMERA_CONN_P
	USB_90D	USB	USB_CAMERA_CONN_N
USB_BT	USB_90D	USB	USB_BT_P 8 19 34
	USB_90D	USB	USB_BT_N 8 19 34
	USB_90D	USB	CONN_USB2_BT_P
	USB_90D	USB	CONN_USB2_BT_N
USB_TPAD	USB_90D	USB	USB_TPAD_P 6 8 19 38
	USB_90D	USB	USB_TPAD_N 6 8 19 38
	USB_90D	USB	CONN_TPAD_USB_P
	USB_90D	USB	CONN_TPAD_USB_N
USB_IR	USB_90D	USB	USB_IR_P 6 8 19 38
	USB_90D	USB	USB_IR_N 6 8 19 38
USB_EXTB	USB_90D	USB	TP_USB_EXTB_P 8 19
	USB_90D	USB	TP_USB_EXTB_N 8 19
	USB_90D	USB	CONN_USB_EXTB_P
	USB_90D	USB	CONN_USB_EXTB_N
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 8
	USB_90D	USB	TP_USB_EXCARD_N 8
USB_EXTC	USB_90D	USB	TP_USB_EXTC_P 8
	USB_90D	USB	TP_USB_EXTC_N 8
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 19
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 6 12 20 42
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 6 12 20 42
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 20 42
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 20 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 6 20 35
	HDA_55S	HDA	HDA_BIT_CLK_R 20
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 6 20 35
	HDA_55S	HDA	HDA_SYNC_R 20
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 20
	HDA_55S	HDA	HDA_RST_L 20 35
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 6 20 35
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 6 20 35
	HDA_55S	HDA	HDA_SDOUT_R 20
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 20
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 20 24
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 24 39
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 20 41
	SPI_55S	SPI	SPI_CLK 48
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 20 41
	SPI_55S	SPI	SPI_MOSI 48
SPI_MISO	SPI_55S	SPI	SPI_MISO 20 41
	SPI_55S	SPI	SPI_MISO_R 48
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 20 41
	SPI_55S	SPI	SPI_CS0_L
SPI_CLK	SPI_55S	SPI	SPI_CLK_MUX 41 48
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_MUX 41 48
SPI_MISO	SPI_55S	SPI	SPI_MISO_MUX 41 48
SPI_CS0	SPI_55S	SPI	SPI_MLB_CS_L 41 48

MCP Constraints 2

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	6 34 38 39 42
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	6 34 38 39 42
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	39 42 45
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	39 42 45
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	39 42 45
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	39 42 45
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	6 39 42 49 58
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	6 39 42 49 58
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	6 25 39 42 59
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	6 25 39 42 59

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SMC Constraints

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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1	PP0V75_S0	NET_SPACING_TYPE=PWR	6 7 33 54 57
2	PP0V75_S3	NET_SPACING_TYPE=PWR	7 25 54
3	PP0V75_S3_MEM_VREFCA	NET_SPACING_TYPE=PWR	25 27 28 29 30
4	PP0V75_S3_MEM_VREFDQ	NET_SPACING_TYPE=PWR	25 27 28 29 30
5	PP18V5_DCIN	NET_SPACING_TYPE=PWR	6 49
6	PP18V5_DCIN_ONEWIRE	NET_SPACING_TYPE=PWR	49
7	PP18V5_G3H	NET_SPACING_TYPE=PWR	6 7 49 58
8	PP18V5_S5_CHGR_SW_R	NET_SPACING_TYPE=PWR	58
10	PP1V05_ENET_MCP_PLL_MAC	NET_SPACING_TYPE=PWR	17 22
9	PP1V05_RMGT	NET_SPACING_TYPE=PWR	7 17 22 57
12	PP1V05_S0	NET_SPACING_TYPE=PWR	6 7 8 9 10 11 12 13 16 17 19 21 22 23 49 56 57
11	PP1V05_S0_MCP_PEX_AVDD	NET_SPACING_TYPE=PWR	7 16 22
13	PP1V05_S0_MCP_PEX_AVDD_R	NET_SPACING_TYPE=PWR	
14	PP1V05_S0_MCP_PEX_DVDD_R	NET_SPACING_TYPE=PWR	
16	PP1V05_S0_MCP_PLL_CORE	NET_SPACING_TYPE=PWR	15 22
15	PP1V05_S0_MCP_PLL_FSB	NET_SPACING_TYPE=PWR	13 22
18	PP1V05_S0_MCP_PLL_NV	NET_SPACING_TYPE=PWR	20 22
17	PP1V05_S0_MCP_PLL_PEX	NET_SPACING_TYPE=PWR	16 22
19	PP1V05_S0_MCP_PLL_SATA	NET_SPACING_TYPE=PWR	19 22
21	PP1V05_S0_MCP_SATA_AVDD	NET_SPACING_TYPE=PWR	19 22
20	PP1V05_S5	NET_SPACING_TYPE=PWR	6 7 21 22 53 57
23	PP1V2_S0_FC_VDD	NET_SPACING_TYPE=PWR	
6160	PP1V5_S0	NET_SPACING_TYPE=PP1V5_MEM	6 7 10 11 15 22 56 57 66
6161	PP1V5_S0_FC_AVDDL_F	NET_SPACING_TYPE=PWR	
22	PP1V5_S0_FC_AVDDT_F	NET_SPACING_TYPE=PWR	
24	PP1V5_S3	NET_SPACING_TYPE=PP1V5_MEM	6 7 26 27 28 29 30 31 32 33 54 57
25	PP1V8_S0	NET_SPACING_TYPE=PWR	6 7 17 23 52
26	PP2V_S0_MCPREG_REF	NET_SPACING_TYPE=PWR	
28	PP3V3_LCDVDD_SW	NET_SPACING_TYPE=PWR	59
27	PP3V3_LCDVDD_SW_F	NET_SPACING_TYPE=PWR	6 59
30	PP3V3_RMGT	NET_SPACING_TYPE=PWR	7 17 22 57
29	PP3V3_S0	NET_SPACING_TYPE=PWR	6 7 12 17 18 20 21 22 23 24 36 61 62
31	PP3V3_S0_CPUTHMSNS_R	NET_SPACING_TYPE=PWR	40 41 42 45 46 50 52 56 57 59 45
33	PP3V3_S0_DPFUSE	NET_SPACING_TYPE=PWR	61
32	PP3V3_S0_DPPWR	NET_SPACING_TYPE=PWR	6 35 61
35	PP3V3_S0_FC_AVDD_F	NET_SPACING_TYPE=PWR	
34	PP3V3_S0_HDD_F	NET_SPACING_TYPE=PWR	6 36
36	PP3V3_S0_IMVP6_3V3	NET_SPACING_TYPE=PWR	50
38	PP3V3_S0_LCD_F	NET_SPACING_TYPE=PWR	6 59
37	PP3V3_S0_MCPREG_VREF3	NET_SPACING_TYPE=PWR	
39	PP3V3_S0_MCP_DAC	NET_SPACING_TYPE=GND	21 23
41	PP3V3_S0_MCP_PLL_USB	NET_SPACING_TYPE=PWR	19 22
40	PP3V3_S0_MCP_VPLL	NET_SPACING_TYPE=PWR	17 23
43	PP3V3_S3	NET_SPACING_TYPE=PWR	6 7 20 25 34 40 42 47 51 54 57
42	PP3V3_S3_AP_AUX	NET_SPACING_TYPE=PWR	6 34
44	PP3V3_S3_AP_AUX_F	NET_SPACING_TYPE=PWR	34
46	PP3V3_S0_MIC_F	NET_SPACING_TYPE=PWR	6 59
45	PP3V3_S5	NET_SPACING_TYPE=PWR	6 7 17 19 20 21 22 24 26 34 41 42 48 55 56 57 59
48	PP3V3_S5_AVREF_SMC	NET_SPACING_TYPE=PWR	39 40
47	PP3V3_S5_MCP	NET_SPACING_TYPE=PWR	
49	PP3V3_S5_SMC_AVCC	NET_SPACING_TYPE=PWR	39
50	PP3V42G3H_SW	NET_SPACING_TYPE=PWR	49
52	PP3V42_G3H	NET_SPACING_TYPE=PWR	6 7 20 21 24 37 38 39 40 41 42 49 58
51	PP3V42_G3H_IPD_F	NET_SPACING_TYPE=PWR	6 38
54	PP3V42_G3H_SMCUSBMUX_R	NET_SPACING_TYPE=PWR	37
53	PP5V_S0	NET_SPACING_TYPE=PWR	6 7 38 41 46 50 57 60
55	PP5V_S0_IMVP6_VDD	NET_SPACING_TYPE=PWR	50
57	PP5V_S0_KBDLED_F	NET_SPACING_TYPE=PWR	6 38
56	PP5V_S0_MCPREG_VCC	NET_SPACING_TYPE=PWR	
59	PP5V_S3	NET_SPACING_TYPE=PWR	6 7 37 38 51 54 55 57 59
58	PP5V_S3_CAMERA_F	NET_SPACING_TYPE=PWR	6 59
72	PP5V_S3_MCPREG_LDO	NET_SPACING_TYPE=PWR	
71	PP5V_S3_TOPCASE_F	NET_SPACING_TYPE=PWR	6 38
73	PP5V_S3_USB2_EXTA	NET_SPACING_TYPE=PWR	37
74	PP5V_S3_USB2_EXTA_F	NET_SPACING_TYPE=PWR	6 35 37
76	PPBUS_G3H	NET_SPACING_TYPE=PWR	6 7 35 43 44 49 55 58 63
75	PPBUS_G3HRS5_VSENSE	NET_SPACING_TYPE=PWR	43
78	PPBUS_R_G3H	NET_SPACING_TYPE=PWR	6 7 44 50 51 53 54 58
77	PPBUS_S0_LCDBKLT_EN_DIV	NET_SPACING_TYPE=PWR	63
79	PPBUS_S0_LCDBKLT_EN_L	NET_SPACING_TYPE=PWR	63
81	PPBUS_S0_LCDBKLT_FUSED	NET_SPACING_TYPE=PWR	63
80	PPBUS_S0_LCDBKLT_PWR	NET_SPACING_TYPE=PWR	62 63
83	PPDCIN_G3H	NET_SPACING_TYPE=PWR	6 7 49
82	PPDCIN_G3H_R	NET_SPACING_TYPE=PWR	49
84	PPMCPCORE_S0	NET_SPACING_TYPE=PWR	6 7 21 22 43 51
86	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR	49 70
85	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR	58 70
6102	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR	49 70
6103	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR	58 70
6104	PPVBAT_G3H_CHGR_REG	NET_SPACING_TYPE=PWR	58
6105	PPVBAT_G3H_CHRGR_REG_0	NET_SPACING_TYPE=PWR	58
6106	PPVBAT_G3H_CHRGR_REG_R	NET_SPACING_TYPE=PWR	58
6108	PPVCORE_S0_CPU	NET_SPACING_TYPE=PWR	6 7 10 11 50 64
6109	PPVDCIN_G3H_PRE	NET_SPACING_TYPE=PWR	43 58
6107	PPVDCIN_G3H_PRE2	NET_SPACING_TYPE=PWR	58
6110	PPVDCIN_G3H_PRE_0	NET_SPACING_TYPE=PWR	58
6112	PPVDCIN_G3H_PRE_R	NET_SPACING_TYPE=PWR	58
6113	PPVIN_S5_IMVP6_VIN	NET_SPACING_TYPE=PWR	50
6111	PPVOUT_S0_LCDBKLT	NET_SPACING_TYPE=PWR	6 59 62
6114	PPVOUT_S0_LCDBKLT_SW	NET_SPACING_TYPE=PWR	62

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M96 Power and Ground Nets

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M96 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.200 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.210 MM	0.200 MM			
55_OHM_SE	ISL2,ISL13	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.250 MM	0.200 MM			
50_OHM_SE	ISL2,ISL13	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.350 MM	0.200 MM			
40_OHM_SE	ISL2,ISL13	Y	0.122 MM	0.122 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	0.110 MM	0.110 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.200 MM			
27P4_OHM_SE	*	Y	0.215 MM	0.215 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.180 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.205 MM	0.200 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.179 MM	0.179 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.179 MM	0.179 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE_MEM	TOP,BOTTOM	Y	0.170 MM	0.110 MM	10 MM		
40_OHM_SE_MEM	ISL2,ISL13	Y	0.122 MM	0.066 MM	170 MM	=STANDARD	=STANDARD
40_OHM_SE_MEM	*	Y	0.110 MM	0.066 MM	170 MM	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
4:1_SPACING	*	0.4 MM	?
2.28:1_SPACING	*	0.228 MM	?
1.1:1_SPACING	*	0.110 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.230 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.345 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.460 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.575 MM	?
2X_DIELECTRIC	ISL2,ISL13	0.110 MM	?
3X_DIELECTRIC	ISL2,ISL13	0.165 MM	?
4X_DIELECTRIC	ISL2,ISL13	0.220 MM	?
5X_DIELECTRIC	ISL2,ISL13	0.275 MM	?
2X_DIELECTRIC	*	0.120 MM	?
3X_DIELECTRIC	*	0.180 MM	?
4X_DIELECTRIC	*	0.240 MM	?
5X_DIELECTRIC	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_STATIC		=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_50S	BGA_P1MM	STANDARD

M96 RULE DEFINITIONS

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	A.0.0

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