1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M97 MLB SCHEMATIC

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
A		625211	PRODUCTION RELEASED	08/29/08	?

08/27/2008

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7537	1	SCHEM,MLB,M97	SCH	CRITICAL	
820-2327	1	PCBF,MLB,M97	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

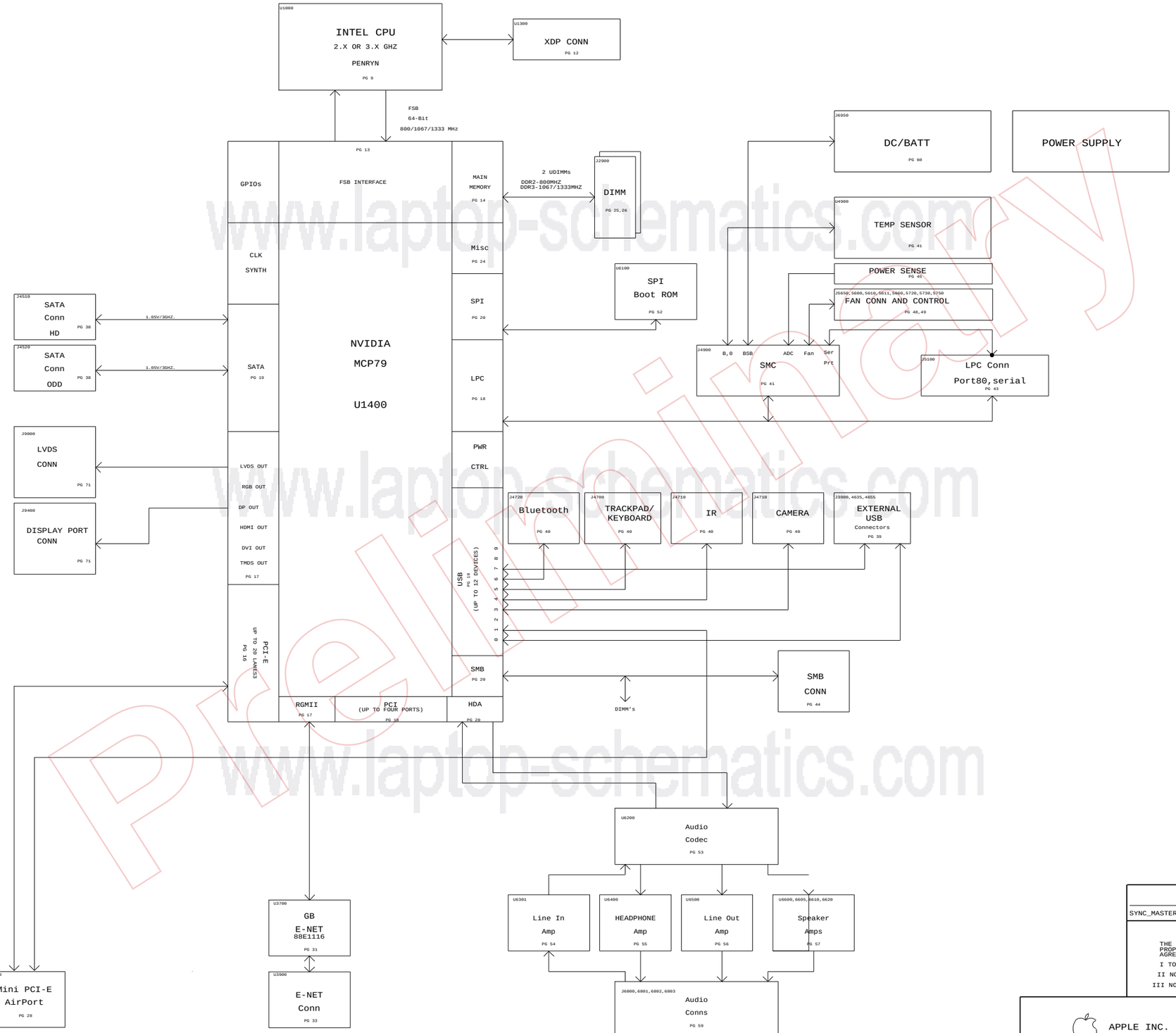
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,M97

DRAWING NUMBER 051-7537 REV. A

SHT 1 OF 109



System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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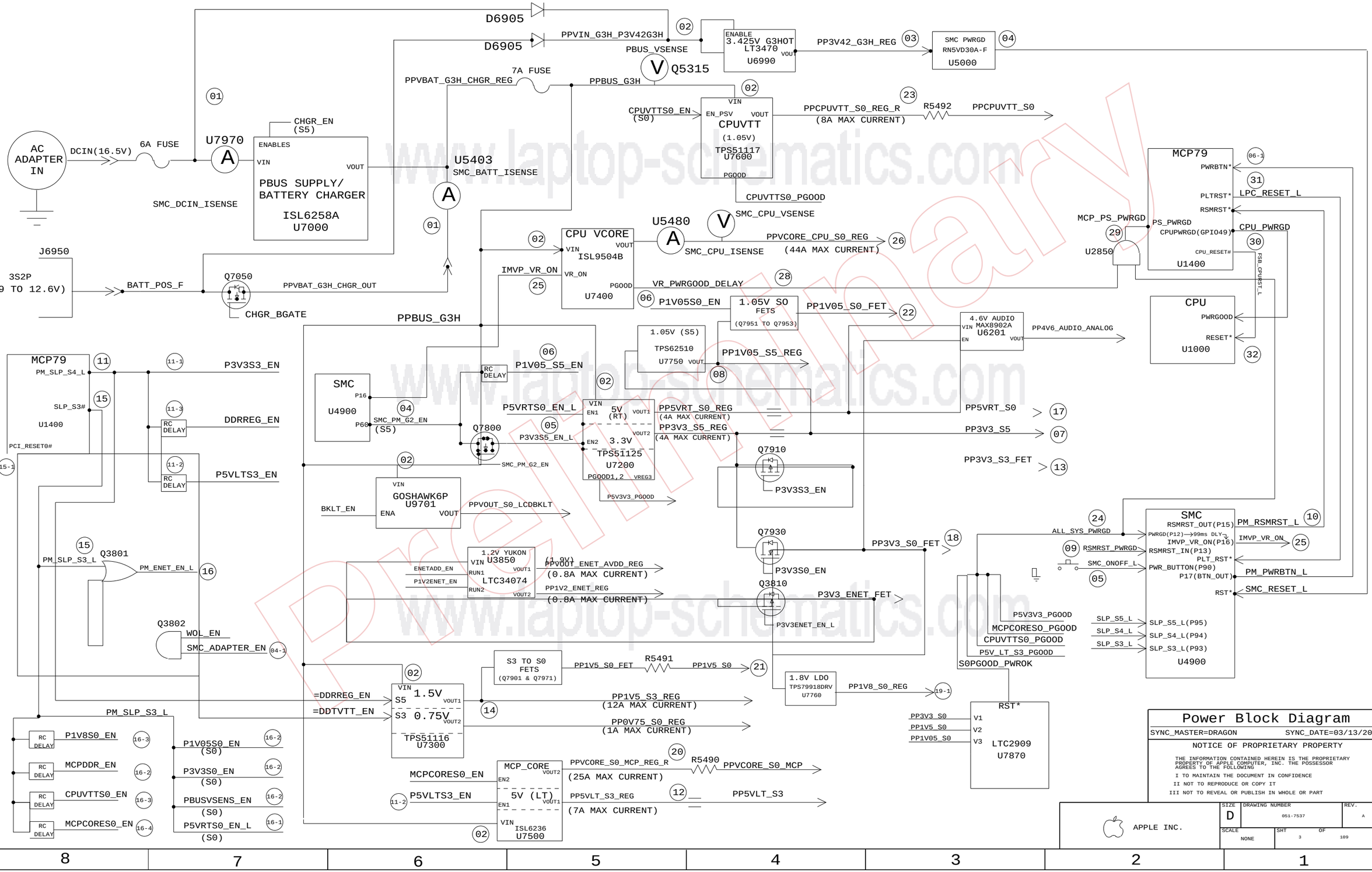
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 2 OF 109	

M97 POWER SYSTEM ARCHITECTURE



BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9554	PCBA,MLB,BETTER,M97	M97_COMMON,CPU_2_0GHZ,EEE_2KA
630-9314	PCBA,MLB,BEST,M97	M97_COMMON,CPU_2_4GHZ,EEE_1DJ

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2K9]	CRITICAL	EEE_2K9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2KA]	CRITICAL	EEE_2KA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:1DJ]	CRITICAL	EEE_1DJ

BOM Groups

BOM GROUP	BOM OPTIONS
M97_COMMON	COMMON,ALTERNATE,M97_MCP,M97_MISC,M97_DEBUG_PVT,M97_PROGPARTS
M97_MCP	MCP_B02,MCP_PROD,MEMRESET_HW,MEMRESET_MCP,BOOT_MODE_USER,MCPSEQ_SMC,MCP_CS1_NO
M97_MISC	ONEWIRE_PU,BKLT_PLL_NOT,DP_ESD,ENG_BMON,MIKEY
M97_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
M97_DEBUG_ENG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,TPAD_DEBUG
M97_DEBUG_PVT	SMC_DEBUG_YES,XDP,LPCPLUS,NO_VREFMRGN
M97_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3622	1	PDC,QJGL,QS,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ_QS
337S3624	1	PDC,QDYD,QS,2.26,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ_QS
337S3625	1	PDC,QDYJ,QS,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ_QS
337S3646	1	PDC,SLG8E,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3653	1	PDC,SL3BU,PRQ,2.26,25W,1066,C0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0540	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01	U1400	CRITICAL	MCP_A01
338S0591	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01P	U1400	CRITICAL	MCP_A01P
338S0603	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01Q	U1400	CRITICAL	MCP_A01Q
338S0600	1	IC,GMCP,MCP79,35X35MM,BGA1437,B01	U1400	CRITICAL	MCP_B01
338S0635	1	IC,GMCP,MCP79,35X35MM,BGA1437,B02	U1400	CRITICAL	MCP_B02
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER,48P,TQFP	U3700	CRITICAL	

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2287	1	IC,SMC,M97	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2285	1	IC,PRGRM,EFI BOOTROM,UNLOCK,M97	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2348	1	IC,WELLSPRING CONTROLLER,M97	U5701	CRITICAL	WELLSPRING_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
514-0612	514-0607		ALL	FOXLINK AS ALTERNATE
514-0613	514-0608		ALL	FOXLINK AS ALTERNATE

M97 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

BOM Configuration

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE	SHT	OF
NONE	4	109

Revision History

A

SYNC_MASTER=M97_MLB

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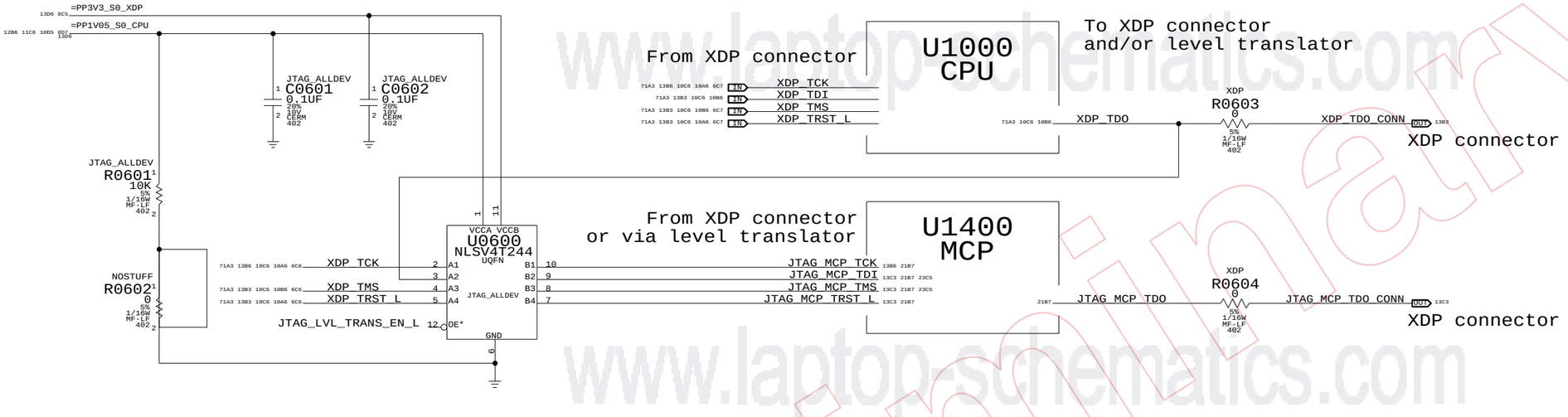
SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	5	109

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

1.05V TO 3.3V LEVEL TRANSLATOR (M97: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 6 OF 109	

Functional Test Points

Fan Connectors

J14	TRUE	PP5VRT_S0	(NEED 3 TP) 7D3 8D5
J15	TRUE	FAN_RT_PWM	46B4
J16	TRUE	FAN_RT_TACH	46C4

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

P23D	TRUE	MIC_HI_CONN	54B1 54D2
P23C	TRUE	MIC_LO_CONN	54B1 54D2
P23B	TRUE	MIC_SHLD_CONN	54D2 55A6

SPEAKER FUNC_TEST

J22	TRUE	SPKRAMP_L_N_OUT	53A2 54C2
J22	TRUE	SPKRAMP_L_P_OUT	53B2 54C2
J22	TRUE	SPKRAMP_R_N_OUT	53C3 54C2
J22	TRUE	SPKRAMP_R_P_OUT	53C3 54C2
J22	TRUE	SPKRAMP_SUB_N_OUT	53B2 54C2
J22	TRUE	SPKRAMP_SUB_P_OUT	53B2 54C2

THERMAL FUNC_TEST

J24B	TRUE	MCPTHMSNS_D2_P	45B5 77D3
J24B	TRUE	MCPTHMSNS_D2_N	45B5 77D3

LVDS FUNC_TEST

P25D	TRUE	PP3V3_LCDVDD_SW_F	7C3 66C2
P25B	TRUE	PP3V3_S0_LCD_F	66C3
P25C	TRUE	PPVOUT_S0_LCDBKLT	7C3 66B2 69B3 69C1
J24B	TRUE	LVDS_IG_DDC_CLK	18A3 66C5
P25G	TRUE	LVDS_IG_DDC_DATA	18A3 66B5
P25H	TRUE	LVDS_IG_A_DATA_N<0>	18B3 66C2 73B3
P25J	TRUE	LVDS_IG_A_DATA_P<0>	18B3 66C2 73B3
P25K	TRUE	LVDS_IG_A_DATA_N<1>	18B3 66C2 73B3
P25L	TRUE	LVDS_IG_A_DATA_P<1>	18B3 66C2 73B3
P25M	TRUE	LVDS_IG_A_DATA_N<2>	18B3 66C2 73B3
P25N	TRUE	LVDS_IG_A_DATA_P<2>	18B3 66C2 73B3
P25P	TRUE	LVDS_IG_A_CLK_F_N	66B2 73B3
P25R	TRUE	LVDS_IG_A_CLK_F_P	66B2 73B3
P25S	TRUE	LED_RETURN_1	66B3 69C1
P23E	TRUE	LED_RETURN_2	66B3 69B1
P24F	TRUE	LED_RETURN_3	66B3 69B1
P24A	TRUE	LED_RETURN_4	66B3 69B1
P24E	TRUE	LED_RETURN_5	66B3 69B1
P24G	TRUE	LED_RETURN_6	66B3 69B1

(NEED TO ADD 5 GND TP)

SATA ODD CONN

P26A	TRUE	PP5V_SW_ODD	(NEED 4 TP) 7C3 36D3
P26B	TRUE	SMC_ODD_DETECT	36B7 39B8
P26D	TRUE	SATA_ODD_D2R_C_P	36B5 73A3
P26F	TRUE	SATA_ODD_D2R_C_N	36B5 73A3
P26H	TRUE	SATA_ODD_R2D_P	36B5 73A3
P26K	TRUE	SATA_ODD_R2D_N	7C5 36B5 73A3

(NEED TO ADD 4 GND TP)

DC POWER CONN

J31A	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP) 56D6
J30C	TRUE	ADAPTER_SENSE	56D7

(NEED TO ADD 4 GND TP)

BATT POWER CONN

J28D	TRUE	PPVBAT_G3H_CONN_F	(NEED 3 TP) 56A8
J28C	TRUE	GND_BATT_CONN	(NEED 3 TP) 56A8
J32B	TRUE	SMBUS_SMC_BSA_SCL	7A7 42C5 76D3
J32A	TRUE	SMBUS_SMC_BSA_SCL	7A7 42C5 76D3
J32D	TRUE	SMC_BS_ALRT_L	39C5 40B2 56A8

BATT SIGNAL CONN

J32C	TRUE	PP3V42_G3H	(NEED 3 TP) 7B5 7C3 8D1
J32B	TRUE	SMBUS_SMC_BSA_SCL	7A7 42C5 76D3
J32A	TRUE	SMBUS_SMC_BSA_SCL	7A7 42C5 76D3
J32E	TRUE	SMC_BIL_BUTTON_DB_L	56A5

(NEED TO ADD 3 GND TP)

FRONT FLEX CONN

J31C	TRUE	PP3V42_G3H_LIDSWITCH_R	38B6
J31E	TRUE	PP5V_S3_IR_R	38B6
J30B	TRUE	IR_RX_OUT	38A4 38C4
J30E	TRUE	SMC_LID_R	38B6
J30F	TRUE	SYS_LED_ANODE_R	38B6

(NEED TO ADD 2 GND TP)

RIGHT CLUTCH CONN

P30A	TRUE	PP5V_S3_BTCAMERA_F	31B7
P30C	TRUE	PCIE_MINI_D2R_P	17B6 31C7 73D3
P30E	TRUE	PCIE_MINI_D2R_N	17B6 31C7 73D3
P30G	TRUE	PCIE_MINI_R2D_P	31C7 73D3
P30J	TRUE	PCIE_MINI_R2D_N	31C7 73D3
P30K	TRUE	PCIE_CLK100M_MINI_CONN_P	31C8 73D3
P30M	TRUE	PCIE_CLK100M_MINI_CONN_N	31C8 73D3
P30N	TRUE	USB_CAMERA_CONN_P	31B7 74C3
P30P	TRUE	USB_CAMERA_CONN_N	31B7 74C3
P30R	TRUE	PP5V_WLAN	7C3 31C5
P30S	TRUE	PCIE_WAKE_L	17B6 23C5 31C7
P29C	TRUE	SMBUS_SMC_A_S3_SCL	7B5 42D2 76D3
P29B	TRUE	SMBUS_SMC_A_S3_SDA	7B5 42D2 76D3
P29A	TRUE	CONN_USB2_BT_P	31B7 74B3
P29N	TRUE	CONN_USB2_BT_N	31B7 74B3
P27A	TRUE	MINI_CLKREQ_O_L	31C7
P28N	TRUE	MINI_RESET_CONN_L	31A7

(NEED TO ADD 3 GND TP)

SATA HDD CONN

J31D	TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP) 7C3 36A7
J31A	TRUE	SATA_HDD_R2D_P	36A7 73A3
J31C	TRUE	SATA_HDD_R2D_N	36A7 73A3
J31B	TRUE	SATA_HDD_D2R_C_P	36A7 73A3
J31F	TRUE	SATA_HDD_D2R_C_N	36A7 73A3
J31G	TRUE	SATA_ODD_R2D_N	7B7 36B5 73A3

(NEED TO ADD 4 GND TP)

IPD_FLEX_CONN

J37C	TRUE	PP3V3_S3_LDO	7C3 48B4 48C3
J37E	TRUE	PP18V5_S3	7C3 48C1 48D3
J37G	TRUE	TPAD_GND_F	48B4 48C3 48C4 48C7
J37J	TRUE	Z2_CS_L	47C8 48C3
J37D	TRUE	Z2_DEBUG3	47C8 48C3
J37A	TRUE	Z2_MOSI	47C8 48C3
J37F	TRUE	Z2_MISO	47C8 48C3
J36C	TRUE	Z2_SCLK	47C8 48C3
J36D	TRUE	Z2_BOOST_EN	48C3 48C5
J36F	TRUE	Z2_HOST_INTN	47D8 48C3
J36A	TRUE	Z2_BOOT_CFG1	47C8 48C3
J36J	TRUE	Z2_CLKIN	47B6 48C3
J36G	TRUE	Z2_KEY_ACT_L	47C8 48C1
J36E	TRUE	Z2_RESET	47C8 48C1
J36B	TRUE	PSOC_MISO	47C8 48C1
J36P	TRUE	PSOC_MOSI	47C8 48C1
J36H	TRUE	PSOC_SCLK	47C8 48C1
J35C	TRUE	SMBUS_SMC_A_S3_SDA	7C5 42D2 76D3
J35F	TRUE	SMBUS_SMC_A_S3_SCL	7D5 42D2 76D3
J35G	TRUE	PSOC_F_CS_L	47C8 48C1
J37J	TRUE	PICKB_L	47D8 48C1

KEYBOARD CONN

P35A	TRUE	PP3V3_S3	7D3 8D3
P35C	TRUE	PP3V42_G3H	7A7 7C3 8D1
P34A	TRUE	WS_KBD1	47C6 47D2
P34B	TRUE	WS_KBD2	47C6 47D2
P34C	TRUE	WS_KBD3	47C6 47D2
P34D	TRUE	WS_KBD4	47C6 47D2
P34F	TRUE	WS_KBD5	47C6 47D2
P34G	TRUE	WS_KBD6	47C6 47D2
P34H	TRUE	WS_KBD7	47C6 47D2
P35D	TRUE	WS_KBD8	47C6 47D2
P35E	TRUE	WS_KBD9	47C6 47D2
P35H	TRUE	WS_KBD10	47C6 47D2
P35K	TRUE	WS_KBD11	47C2 47C6
P32F	TRUE	WS_KBD12	47C2 47C6
P32G	TRUE	WS_KBD13	47C2 47C6
P32D	TRUE	WS_KBD14	47C2 47C6
P32E	TRUE	WS_KBD15_CAP	47C2
P32C	TRUE	WS_KBD16_NUM	47C2
P32A	TRUE	WS_KBD17	47C2 47C6
P33D	TRUE	WS_KBD18	47C2 47D7
P33E	TRUE	WS_KBD19	47C2 47D7
P33B	TRUE	WS_KBD20	47C2 47D7
P33C	TRUE	WS_KBD21	47C2 47D7
P33F	TRUE	WS_KBD22	47C2 47D7
P33G	TRUE	WS_KBD23	47C2 47D7
P33H	TRUE	WS_KBD_ONOFF_L	47C2
P33K	TRUE	WS_LEFT_SHIFT_KBD	47B3 47B5 47C2
P33J	TRUE	WS_LEFT_OPTION_KBD	47B3 47B5 47C2
P33A	TRUE	WS_CONTROL_KBD	47B3 47B5 47C2

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

P35B	TRUE	KBDLED_ANODE	48A4

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

P23F	TRUE	PPVCORE_S0_CPU	8D7
P23H	TRUE	PPCPUVTT_S0	8D7
P23G	TRUE	PPVCORE_S0_MCP	8C7
P23K	TRUE	PP0V75_S0	8C7
P23M	TRUE	PP1V05_S0	8C7
P23J	TRUE	PP1V5_S0	8B7
P23L	TRUE	PP1V8_S0	8B7
P23N	TRUE	PP5VRT_S0	7D7 8D5
P27B	TRUE	PP3V3_S0	8C5
P27D	TRUE	PP1V5_S3	8D3
P27C	TRUE	PP3V3_S3	7B5 8D3
P27E	TRUE	PP5VLT_S3	8C3
P27G	TRUE	PP1V1R1V05_S5	8B3
P27F	TRUE	PP3V3_S5	8B3
P27J	TRUE	PP3V42_G3H	7A7 7B5 8D1
P27K	TRUE	PPBUS_G3H	8C1
P27H	TRUE	PP3V3_ENET_PHY	8B1
P27N	TRUE	PP1V2R1V05_ENET	8B1
P27M	TRUE	PP3V3_G3_RTC	21C8 22A5 26D4
P30D	TRUE	PP5V_WLAN	7D5 31C5
P30F	TRUE	PP5V_SW_ODD	7B7 36D3
P30H	TRUE	PP5V_S0_HDD_FLT	7C5 36A7
P30K	TRUE	PP3V3_S5_AVREF_SMC	39D4 40B6
P30L	TRUE	PP18V5_S3	7C5 48C1 48D3
P30M	TRUE	PP3V3_S3_LDO	7C5 48B4 48C3
P30N	TRUE	PP3V3_LCDVDD_SW_F	7C7 66C2
P30R	TRUE	PPVOUT_S0_LCDBKLT	7C7 66B2 69B3 69C1
P30S	TRUE	BKL_VREF_4V9	69A8 69B6 69C4 69C8
P31B	TRUE	PP4V6_AUDIO_ANALOG	51A3 51D3 52D6
P31C	TRUE	SMC_PM_G2_EN	39D5 64D8
P31A	TRUE	PM_SLP_S4_L	21C3 39C5 48A2 64C8
P31D	TRUE	PM_SLP_S3_L	21C3 34B7 39C5 41A5 64D5 68D8

(NEED TO ADD 4 GND TP)

FUNC TEST

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 7 OF 109	

"S0,S0M" RAILS

60D1 =PPVCORE_S0_CPU_REG (CPU VCORE PWR)
- PPVCORE_S0_CPU — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=1.25V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_CPU — 11B5 11D6 12D6
  - =PPVCORE_S0_CPU_VSENSE — 43D8

65A6 62C7 =PPCPUVTT_S0_REG
- PPCPUVTT_S0 — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S0_CPU — 6D8 10D5 11C6 12B6 13D6
  - =PP1V05_S0_MCP_FSB — 9C2 14A2 14B7 22D3 24C8
  - =PP1V05_S0_SMC_LS — 40D3

61C1 =PPMCPCORE_S0_REG
44D8 =PPVCORE_S0_MCP_REG_R (MCP VCORE REG. OUTPUT)
- PPVCORE_S0_MCP_R
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_MCP_VSENSE — 43D8

44D7 =PPVCORE_S0_MCP
24D8 61B1 (MCP VCORE AFTER SENSE RES)
- PPVCORE_S0_MCP — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE

59C8 =PP0V75_S0_REG
- PP0V75_S0 — 7D3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=0.75V
  MAKE_BASE=TRUE
  - =PPVTT_S0_VTTCLAMP — 65B3
  - =PP0V75_S0_MEM_VTT_A — 28A4
  - =PP0V75_S0_MEM_VTT_B — 29A4

65A5 =PP1V05_S0_FET
- PP1V05_S0 — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.4V
  MAKE_BASE=TRUE
  - =PP1V05_S0_MCP_PEX_DVDD — 8A8 24D8
  - =PP1V05_S0_MCP_AVDD_UF — 24D4
  - =PP1V05_S0_MCP_PLL_UF — 24C4
  - =PP1V05_S0_MCP_SATA_DVDD — 8A8 24D6
  - =PP1V05_S0_MCP_HDMI_VDD — 18A6 25D7
  - =PP1V05_S0_VMON — 64A8

65D1 =PP1V5_S0_FET
44C8 =PP1V5_S0_FET_R (DDR PWR REG. OUTPUT)
- PP1V5_S0_R
  MIN_LINE_WIDTH=0.5 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S0_CPU — 11B6 12B6
  - =PP1V5_S0_VMON — 64A8
  - =PP1V5_FC_CON — 32C3

44C7 =PP1V5_S0 (DDR PWR AFTER SENSE RES.)
- PP1V5_S0 — 7D3
  MIN_LINE_WIDTH=0.5 MM
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V8R1V5_S0_MCP_MEM — 16C3 16C7 24C8
  - =PP1V5_S0_MEM_MCP — 29B3

63C2 =PP1V8_S0_REG
- PP1V8_S0 — 7D3
  MIN_LINE_WIDTH=0.5 MM
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.8V
  MAKE_BASE=TRUE
  - =PP3V3R1V8_S0_MCP_IFP_VDD — 18B6 25D7

58B8 =PP5VRT_S0_REG
- PP5VRT_S0 — 7D3 7D7
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S0_HDD — 36A5
  - =PP5V_S0_LPCPLUS — 41D5
  - =PP5V_S0_FAN_RT — 46C5
  - =PP5V_S0_CPU_IMVP — 60D8
  - =PP5V_S0_ODD — 36D5
  - =PP5V_S0_KBDLED — 48A5
  - =PP5V_S0_DP_AUX_MUX — 67B6
  - =PP5V_S0_CPUVTTS0 — 62C8

65C6 =PP3V3_S0_FET
- PP3V3_S0 — 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S0_XDP — 6D8 13D6
  - =PP3V3_S0_MCP — 21C2 22B3 24B8
  - =PP3V3_S0_MCP_DAC_UF — 25D4
  - =PP3V3_S0_MCP_VPLL_UF — 25B7
  - =PP3V3_S0_ODD — 36B7 36D5
  - =PP3V3_S0_LPCPLUS — 41C3
  - =PP3V3_S0_SMBUS_SMC_0_S0 — 42D5
  - =PP3V3_S0_SMBUS_SMC_B_S0 — 42C3
  - =PP3V3_S0_SMBUS_MCP_0 — 42D8
  - =PP3V3_S0_FAN_RT — 46C5
  - =PP3V3_S0_AUDIO — 51A7 51D8 52D6 54D8 55B5
  - =PP3V3_S0_IMVP — 60D8
  - =PP3V3_S0_LCD — 66C5
  - =PP3V3_S0_MCP_GPIO — 18C1 19D1 21A4
  - =PP3V3_S0_HDCPROM — 25B8
  - =PP3V3_S0_MCP_PLL_UF — 24B6
  - =PP3V3R1V5_S0_MCP_HDA — 21D3 21D8 24A8
  - =PP3V3_S0_SMC — 40A1 40D2
  - =PP3V3_S0_MCPTHMSNS — 45C6
  - =PP3V3_S0_CPUTHMSNS — 45D6
  - =PP5VR3V3_S0_MCPCOREISNS — 44D7
  - =PP3V3_S0_DPCONN — 68A8 68B8
  - =PPSPD_S0_MEM_A — 28A8
  - =PPSPD_S0_MEM_B — 29A8
  - =PP3V3_S0_PWRCTL — 64A5
  - =PP3V3_S0_VMON — 64B8
  - =PP3V3_S0_MCPDDRISNS — 44C7
  - =PP3V3_S0_CPUVTTISNS — 44B7
  - =PPVIN_S0_P1V8S0 — 63C5
  - =PP3V3_FC_CON — 32C3
  - =PP3V3_S0_TPAD — 48A6
  - =PP3V3_S0_SMBUS_MCP_1 — 42C8

"S3" RAILS

59B1 =PP1V5_S3_REG
- PP1V5_S3 — 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S3_P1V5S0FET — 65D3
  - =PP1V5_S3_MEM_A — 28D7
  - =PP1V5_S3_MEM_B — 29D7
  - =PP1V5_S3_MEMRESET — 30C6

65D6 =PP3V3_S3_FET
- PP3V3_S3 — 7B5 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S3_SMBUS_SMC_A_S3 — 42D3
  - =PP3V3_S3_PDCISENS — 59B3
  - =PP3V3_S3_SMBUS_SMC_MGMT — 42B5
  - =PP3V3_S3_VREFMRGN — 27D8
  - =PP3V3_S3_WLAN — 31A6
  - =PP3V3_S3_MCP_GPIO — 21A3
  - =PP3V3_S3_TPAD — 47A6 47B5 47C5 47D2
  - =PP3V3_S3_SMS — 49B7 49D6

61C8 =PP5VLT_S3_REG
- PP5VLT_S3 — 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S3_EXTUSB — 37C7
  - =PP5V_S3_IR — 38B4 38D7
  - =PP5V_S3_BTCAMERA — 31B3
  - =PP5V_S3_VTTCLAMP — 65A3
  - =PP5V_S3_MCPDDRFET — 65D4
  - =PP5V_S3_SYSLED — 40B8
  - =PP5V_S3_TPAD — 48C8
  - =PP5V_S3_WLAN — 31C1
  - =PP5V_S3_1V5S30V75S0 — 59C5
  - =PP5V_S3_AUDIO — 51A7 55D4
  - =PP5V_S3_AUDIO_AMP — 53B8 53C8 53D8
  - =PP5V_S3_P1V05S0FET — 65B8

59D7 27D3 =PPVTT_S3_DDR_BUF
- PPVTT_S3_DDR_BUF
  MIN_LINE_WIDTH=0.3 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=0.75V
  MAKE_BASE=TRUE

"S5" RAILS

63B4 =PP1V05_S5_REG
- PP1V1R1V05_S5 — 7C3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S5_MCP_VDD_AUXC — 22A3 24C8
  - =PP1V05_ENET_P1V05ENETFET — 34C4
  - =PP1V05_S5_P1V05S0FET — 65B6

58B1 =PP3V3_S5_REG
- PP3V3_S5 — 7C3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S5_MCP_GPIO — 18C7 20C1
  - =PP3V3_S5_ROM — 41B5 41C7 50C6
  - =PP3V3_S5_LCD — 66C8
  - =PP3V3_S5_MCP — 22B3 24B8
  - =PP3V3_S5_MCPPWRGD — 26B8
  - =PP3V3_S5_SMBUS_MCP_1 — 42C7
  - =PP3V3_S5_MCP_A01 — 23C4 41B4
  - =PP3V3_S5_PWRCTL — 64B3 64C4
  - =PP3V3_S5_P1V05ENETFET — 34C5
  - =PP3V3_S5_P3V3S3FET — 65D8
  - =PP3V3_S5_P3V3S0FET — 65C8
  - =PP3V3_S5_P1V05S5 — 63B7
  - =PP3V3_S5_P1V05FET — 65A8
  - =PP3V3_S5_MEMRESET — 30C6
  - =PP3V3_S5_P3V3ENETFET — 34D5
  - =PP3V3_S5_DP_PORT_PWR — 68D8

"G3H" RAILS

56B4 =PP3V42_G3H_REG
- PP3V42_G3H — 7A7 7B5 7C3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.42V
  MAKE_BASE=TRUE
  - =PPVIN_S5_SMCVREF — 40B8
  - =PP3V42_G3H_SMBUS_SMC_BSA — 42C5
  - =PP3V42_G3H_PWRCTL — 64B3 64D3 64D8
  - =PP3V42_G3H_CHGR — 57A8 57C6 57D5
  - =PP3V42_G3H_SMCUSBMUX — 37B8
  - =PP3V42_G3H_LIDSWITCH — 38B4
  - =PP3V42_G3H_TPAD — 47B3 47B5 47C2 47C5
  - =PP3V42_G3H_BATT — 56A3 56B3
  - =PP3V3_S5_SMC — 39D4 40C1 40C7 40D8 49D7
  - =PP3V3_S5_LPCPLUS — 41B7 41C3 41C7 41D5
  - =PP3V42_G3H_RTC_D — 26D8
  - =PP3V42_G3H_BMON_ISNS — 44A8

56D1 56B8 =PP18V5_DCIN_CONN
- PP18V5_G3H
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=18.5V
  MAKE_BASE=TRUE
  - =PP18V5_G3H_CHGR — 57D8

57C1 =PPBUS_G3H
- PPBUS_G3H — 7C3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPBUS_S0_LCDBKLT — 70D8
  - =PPVIN_S0_MCPCORES0 — 61C3
  - =PPVIN_S0_MCPREG_VIN — 61C6
  - =PPVIN_S5_1V5S30V75S0 — 59C2
  - =PPVIN_S5_3V3S5 — 58B3
  - =PPVIN_S0_5VRTS0 — 58B6 58C6
  - =PPVIN_S3_5VLTS3 — 61D8
  - =PPBUS_G3HRS5 — 43B8
  - =PPPCPUVCORE_VTT_ISNS_R — 44B8 (BEFORE HIGH SIDE SENSING RES.)

44B7 =PPCPUVCORE_VTT_ISNS (AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
- PPBUS_G3H_CPU_ISNS
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPVIN_S0_CPUVTTS0 — 62C6
  - =PPVIN_S5_CPU_IMVP — 60C2 60D4 68D8

"ENET" RAILS

34D2 =PP3V3_ENET_FET
- PP3V3_ENET_PHY — 7C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_ENET_MCP_RMGT — 18C7 18D3 24A6 24B6
  - =PP3V3_ENET_PHY — 33D7

34B2 =PP1V05_ENET_FET
- PP1V2R1V05_ENET — 7C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_ENET_MCP_PLL_MAC — 24A8
  - =PP1V05_ENET_MCP_RMGT — 18D3 24C6
  - =PP1V05_ENET_PHY — 33D2

PEX & SATA AVDD/DVDD aliases

24D1 PP1V05_S0_MCP_PEX_AVDD (MAKE_BASE=TRUE)
206 mA (A01)
- =PP1V05_S0_MCP_PEX_AVDD0 — 17B3
- =PP1V05_S0_MCP_PEX_AVDD1 — 17A3

206 mA (A01)

24D8 8B7 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
- =PP1V05_S0_MCP_PEX_DVDD0 — 17B6
- =PP1V05_S0_MCP_PEX_DVDD1 — 17A6

57 mA (A01)

24C2 PP1V05_S0_MCP_SATA_AVDD (MAKE_BASE=TRUE)
127 mA (A01)
- =PP1V05_S0_MCP_SATA_AVDD0 — 20B6
- =PP1V05_S0_MCP_SATA_AVDD1 — 20A6

127 mA (A01)

24D6 8B7 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)
- =PP1V05_S0_MCP_SATA_DVDD0 — 20B6
- =PP1V05_S0_MCP_SATA_DVDD1 — 20B6

43 mA (A01)

Power Aliases

SYNC_MASTER=BEN

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SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE	SHT	OF
NONE	8	109

HEATSINK STANDOFFS

Z0902 STDOFF-4.50D.98H-1.1-3.48-TH — LEFT OF CPU

Z0901 STDOFF-4.50D.98H-1.1-3.48-TH — ABOVE CPU

Z0903 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW MCP

Z0904 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW CPU

FAN STANDOFF

Z0905 STDOFF-4.50D.98H-1.1-3.48-TH

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

AUDIO CHASSIS GND

GND_CHASSIS_AUDIO MAKE_BASE=TRUE

OMIT Z0906 TH SL-3.10X2.70

548B 54A8 =GND_CHASSIS_AUDIO_JACK
55A4 54A3 =GND_CHASSIS_AUDIO_MIC

MLB MOUNTING SCREW HOLES

OMIT Z0908 3R2P5
OMIT Z0909 3R2P5
OMIT Z0910 3R2P5
OMIT Z0911 3R2P5
OMIT Z0912 3R2P5
OMIT Z0913 3R2P5

VENICE BOARD STANDOFFS

VENICE Z0914 STDOFF-4.0OD3.0H-TH
VENICE Z0915 STDOFF-4.0OD3.0H-TH
VENICE Z0916 STDOFF-4.0OD3.0H-TH

EMI IO POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
ZS0901 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
ZS0902 1.4DIA-SHORT-EMI-MLB-M97-M98 SM
ZS0903 1.4DIA-SHORT-EMI-MLB-M97-M98 SM

EMI POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98 SM

PCI-E ALIASES

UNUSED GPU LANES

17D6 17C6 =PEG_D2R_N<15:0> — NC_PEG_D2R_N<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17D6 17C6 =PEG_D2R_P<15:0> — NC_PEG_D2R_P<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17D3 17C3 =PEG_R2D_C_N<15:0> — NC_PEG_R2D_C_N<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17D3 17C3 =PEG_R2D_C_P<15:0> — NC_PEG_R2D_C_P<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17C6 PEG_PRSNT_L — TP_PEG_PRSNT_L MAKE_BASE=TRUE
17C3 PEG_CLK100M_P — TP_PEG_CLK100M_P MAKE_BASE=TRUE
17C3 PEG_CLK100M_N — TP_PEG_CLK100M_N MAKE_BASE=TRUE

UNUSED FW LANE

17B6 PCIE_FW_D2R_P — TP_PCIE_FW_D2R_P MAKE_BASE=TRUE
17B6 PCIE_FW_D2R_N — TP_PCIE_FW_D2R_N MAKE_BASE=TRUE
17B3 PCIE_FW_R2D_C_P — TP_PCIE_FW_R2D_C_P MAKE_BASE=TRUE
17B3 PCIE_FW_R2D_C_N — TP_PCIE_FW_R2D_C_N MAKE_BASE=TRUE
17C6 PCIE_FW_PRSNT_L — TP_PCIE_FW_PRSNT_L MAKE_BASE=TRUE
17C6 FW_CLKREQ_L — TP_FW_CLKREQ_L MAKE_BASE=TRUE
17C3 PCIE_CLK100M_FW_P — TP_PCIE_CLK100M_FW_P MAKE_BASE=TRUE
17C3 PCIE_CLK100M_FW_N — TP_PCIE_CLK100M_FW_N MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

17B6 PCIE_EXCARD_D2R_P — TP_PCIE_EXCARD_D2R_P MAKE_BASE=TRUE
17B6 PCIE_EXCARD_D2R_N — TP_PCIE_EXCARD_D2R_N MAKE_BASE=TRUE
17B3 PCIE_EXCARD_R2D_C_P — TP_PCIE_EXCARD_R2D_C_P MAKE_BASE=TRUE
17B3 PCIE_EXCARD_R2D_C_N — TP_PCIE_EXCARD_R2D_C_N MAKE_BASE=TRUE
17C6 PCIE_EXCARD_PRSNT_L — TP_PCIE_EXCARD_PRSNT_L MAKE_BASE=TRUE
17C6 EXCARD_CLKREQ_L — TP_EXCARD_CLKREQ_L MAKE_BASE=TRUE
17C3 PCIE_CLK100M_EXCARD_P — TP_PCIE_CLK100M_EXCARD_P MAKE_BASE=TRUE
17C3 PCIE_CLK100M_EXCARD_N — TP_PCIE_CLK100M_EXCARD_N MAKE_BASE=TRUE

AIRPORT CARD PRESENT SIGNAL

31D7 17C6 PCIE_MINI_PRSNT_L — MAKE_BASE=TRUE

FOR VENICE CARD

17B6 TP_PE4_CLKREQ_L — FC_CLKREQ_L 32C5 MAKE_BASE=TRUE
17B6 TP_PE4_PRSNT_L — FC_PRSNT_L 32B3 MAKE_BASE=TRUE
17B3 TP_PCIE_CLK100M_PE4P — PCIE_CLK100M_FC_P 32C5 73D3 MAKE_BASE=TRUE
17B3 TP_PCIE_CLK100M_PE4N — PCIE_CLK100M_FC_N 32C5 73C3 MAKE_BASE=TRUE
17B6 TP_PCIE_PE4_D2RP — PCIE_FC_D2R_P 32B5 73D3 MAKE_BASE=TRUE
17B6 TP_PCIE_PE4_D2RN — PCIE_FC_D2R_N 32B5 73D3 MAKE_BASE=TRUE
17B3 TP_PCIE_PE4_R2D_CP — PCIE_FC_R2D_C_P 32C6 73D3 MAKE_BASE=TRUE
17B3 TP_PCIE_PE4_R2D_CN — PCIE_FC_R2D_C_N 32C6 73D3 MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

20C3 USB_EXTC_P — TP_USB_EXTC_P MAKE_BASE=TRUE
20C3 USB_EXTC_N — TP_USB_EXTC_N MAKE_BASE=TRUE
20D3 USB_EXTD_P — TP_USB_EXTD_P MAKE_BASE=TRUE
20D3 USB_EXTD_N — TP_USB_EXTD_N MAKE_BASE=TRUE
20C3 USB_EXCARD_P — TP_USB_EXCARD_P MAKE_BASE=TRUE
20C3 USB_EXCARD_N — TP_USB_EXCARD_N MAKE_BASE=TRUE
20D3 USB_MINI_P — TP_USB_MINI_P MAKE_BASE=TRUE
20D3 USB_MINI_N — TP_USB_MINI_N MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

18C6 MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET NO_TEST=TRUE MAKE_BASE=TRUE
18C6 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF NO_TEST=TRUE MAKE_BASE=TRUE
18C6 MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN NO_TEST=TRUE MAKE_BASE=TRUE
18C6 MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB NO_TEST=TRUE MAKE_BASE=TRUE
18B3 CRT_IG_HSYNC — NC_CRT_IG_HSYNC NO_TEST=TRUE MAKE_BASE=TRUE
18B3 CRT_IG_VSYNC — NC_CRT_IG_VSYNC NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

18B3 LVDS_IG_A_DATA_P<3> — NC_LVDS_IG_A_DATA_P3 NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_A_DATA_N<3> — NC_LVDS_IG_A_DATA_N3 NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_CLK_P — NC_LVDS_IG_B_CLK_P NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_CLK_N — NC_LVDS_IG_B_CLK_N NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_DATA_P<3:0> — NC_LVDS_IG_B_DATA_P<3:0> NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_DATA_N<3:0> — NC_LVDS_IG_B_DATA_N<3:0> NO_TEST=TRUE MAKE_BASE=TRUE

MISC MCP79 ALIASES

14B6 CPU_PECI_MCP — TP_CPU_PECI_MCP
19B7 FW_PME_L — TP_FW_PME_L MAKE_BASE=TRUE
17B6 GMUX_JTAG_TCK_L — TP_GMUX_JTAG_TCK_L MAKE_BASE=TRUE
17B6 GMUX_JTAG_TDO — TP_GMUX_JTAG_TDO MAKE_BASE=TRUE
19D4 GMUX_JTAG_TDI — TP_GMUX_JTAG_TDI MAKE_BASE=TRUE
19D4 GMUX_JTAG_TMS — TP_GMUX_JTAG_TMS MAKE_BASE=TRUE

LAN ALIASES

18D6 =MCP_MII_RXER — MCP_MII_PD MAKE_BASE=TRUE
18C6 =MCP_MII_COL
18C6 =MCP_MII_CRS

R0930 4.7K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

1886 =DVI_HPD_GMUX_INT — HPLUG_DET2 MAKE_BASE=TRUE

R0940 20K 5% 1/16W MF-LF 402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

28C5 MEM_A_A<15> — TP_MEM_A_A15 MAKE_BASE=TRUE
29C5 MEM_B_A<15> — TP_MEM_B_A15 MAKE_BASE=TRUE

ETHERNET ALIASES

34C5 =P3V3ENET_EN — PM_SLP_RMGT_L 21C3 MAKE_BASE=TRUE
34B5 =P1V05ENET_EN
33C2 =PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
33C2 =RTL8211_REGOUT — NC_RTL8211_REGOUT MAKE_BASE=TRUE
33C6 =RTL8211_ENSWREG MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

71C3 10B4 10A4 IN CPU_BSEL<0:2> — =MCP_BSEL<0:2> OUT 14A7 MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

24C8 22D3 14B7 14A2 8D7 =PP1V05_S0_MCP_FSB

MCP_A01&MCP_A01P&MCP_A01Q

R0950 220 5% 1/16W MF-LF 402
NO STUFF R0970 200 5% 1/16W MF-LF 402
NO STUFF R0990 150 5% 1/16W MF-LF 402
NO STUFF R0960 62 5% 1/16W MF-LF 402
NO STUFF R0980 150 5% 1/16W MF-LF 402

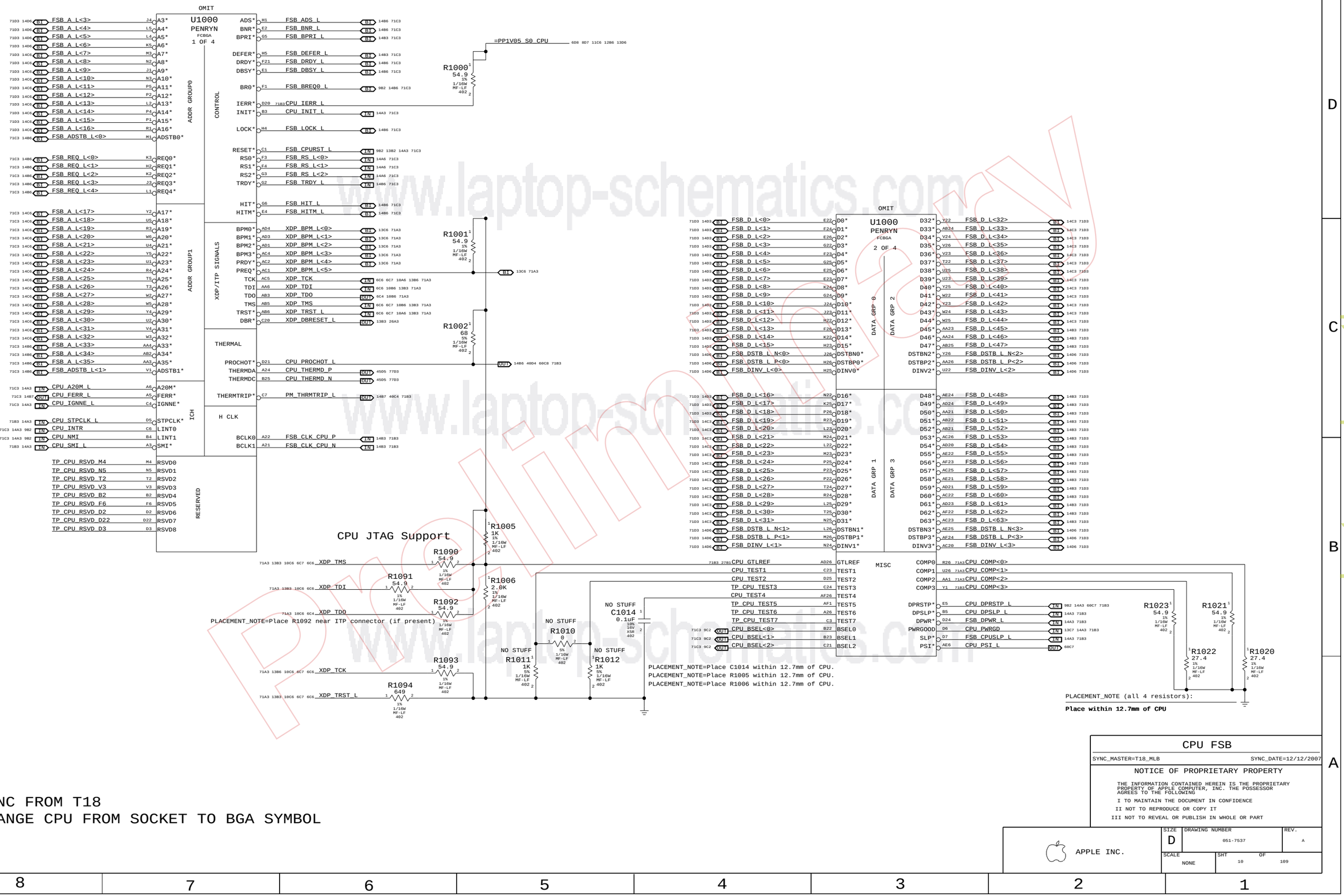
71B3 60C7 14A3 10B2 OUT CPU_DPRSTP_L
71C3 14B6 10C6 OUT FSB_BREQ0_L
71C3 14A3 13B2 10C6 OUT FSB_CPURST_L
71C3 14A3 10B6 OUT CPU_INTR
71C3 14A3 10B6 OUT CPU_NMI

SIGNAL ALIAS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 9 OF 109	


OMIT
U1000
PENRYN
FCBGA
1 OF 4
ADDR GROUP0
ADDR GROUP1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
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FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
FSB_A_L<19>
FSB_A_L<20>
FSB_A_L<21>
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FSB_A_L<32>
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FSB_A_L<34>
FSB_A_L<35>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_RSVD_M4
TP_CPU_RSVD_N5
TP_CPU_RSVD_T2
TP_CPU_RSVD_V3
TP_CPU_RSVD_B2
TP_CPU_RSVD_F6
TP_CPU_RSVD_D2
TP_CPU_RSVD_D22
TP_CPU_RSVD_D3
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
CPU_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
=PP1V05_S0_CPU
R1000 54.9 1% 1/16W MF-LF 402
R1001 54.9 1% 1/16W MF-LF 402
R1002 68 5% 1/16W MF-LF 402
CPU JTAG Support
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
R1090 54.9 1% 1/16W MF-LF 402
R1091 54.9 1% 1/16W MF-LF 402
R1092 54.9 1% 1/16W MF-LF 402
R1093 54.9 1% 1/16W MF-LF 402
R1094 649 1% 1/16W MF-LF 402
R1010 0 5% 1/16W MF-LF 402
R1011 1K 5% 1/16W MF-LF 402
R1012 1K 5% 1/16W MF-LF 402
C1014 0.1uF 10% 16V X5R 402
NO STUFF
PLACEMENT_NOTE=Place R1092 near ITP connector (if present)
PLACEMENT_NOTE=Place C1014 within 12.7mm of CPU.
PLACEMENT_NOTE=Place R1005 within 12.7mm of CPU.
PLACEMENT_NOTE=Place R1006 within 12.7mm of CPU.
OMIT
U1000
PENRYN
FCBGA
2 OF 4
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
FSB_D_L<6>
FSB_D_L<7>
FSB_D_L<8>
FSB_D_L<9>
FSB_D_L<10>
FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTB_L_N<0>
FSB_DSTB_L_P<0>
FSB_DINV_L<0>
FSB_D_L<16>
FSB_D_L<17>
FSB_D_L<18>
FSB_D_L<19>
FSB_D_L<20>
FSB_D_L<21>
FSB_D_L<22>
FSB_D_L<23>
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FSB_D_L<27>
FSB_D_L<28>
FSB_D_L<29>
FSB_D_L<30>
FSB_D_L<31>
FSB_DSTB_L_N<1>
FSB_DSTB_L_P<1>
FSB_DINV_L<1>
FSB_D_L<32>
FSB_D_L<33>
FSB_D_L<34>
FSB_D_L<35>
FSB_D_L<36>
FSB_D_L<37>
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FSB_D_L<39>
FSB_D_L<40>
FSB_D_L<41>
FSB_D_L<42>
FSB_D_L<43>
FSB_D_L<44>
FSB_D_L<45>
FSB_D_L<46>
FSB_D_L<47>
FSB_DSTB_L_N<2>
FSB_DSTB_L_P<2>
FSB_DINV_L<2>
FSB_D_L<48>
FSB_D_L<49>
FSB_D_L<50>
FSB_D_L<51>
FSB_D_L<52>
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FSB_D_L<54>
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FSB_D_L<58>
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FSB_D_L<60>
FSB_D_L<61>
FSB_D_L<62>
FSB_D_L<63>
FSB_DSTB_L_N<3>
FSB_DSTB_L_P<3>
FSB_DINV_L<3>
CPU_GTLREF
CPU_TEST1
CPU_TEST2
TP_CPU_TEST3
CPU_TEST4
TP_CPU_TEST5
TP_CPU_TEST6
TP_CPU_TEST7
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGD
FSB_CPUSLP_L
CPU_PSI_L
R1023 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1022 27.4 1% 1/16W MF-LF 402
R1020 27.4 1% 1/16W MF-LF 402
PLACEMENT_NOTE (all 4 resistors):
Place within 12.7mm of CPU
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CPU FSB
SYNC_MASTER=T18_MLB
SYNC_DATE=12/12/2007
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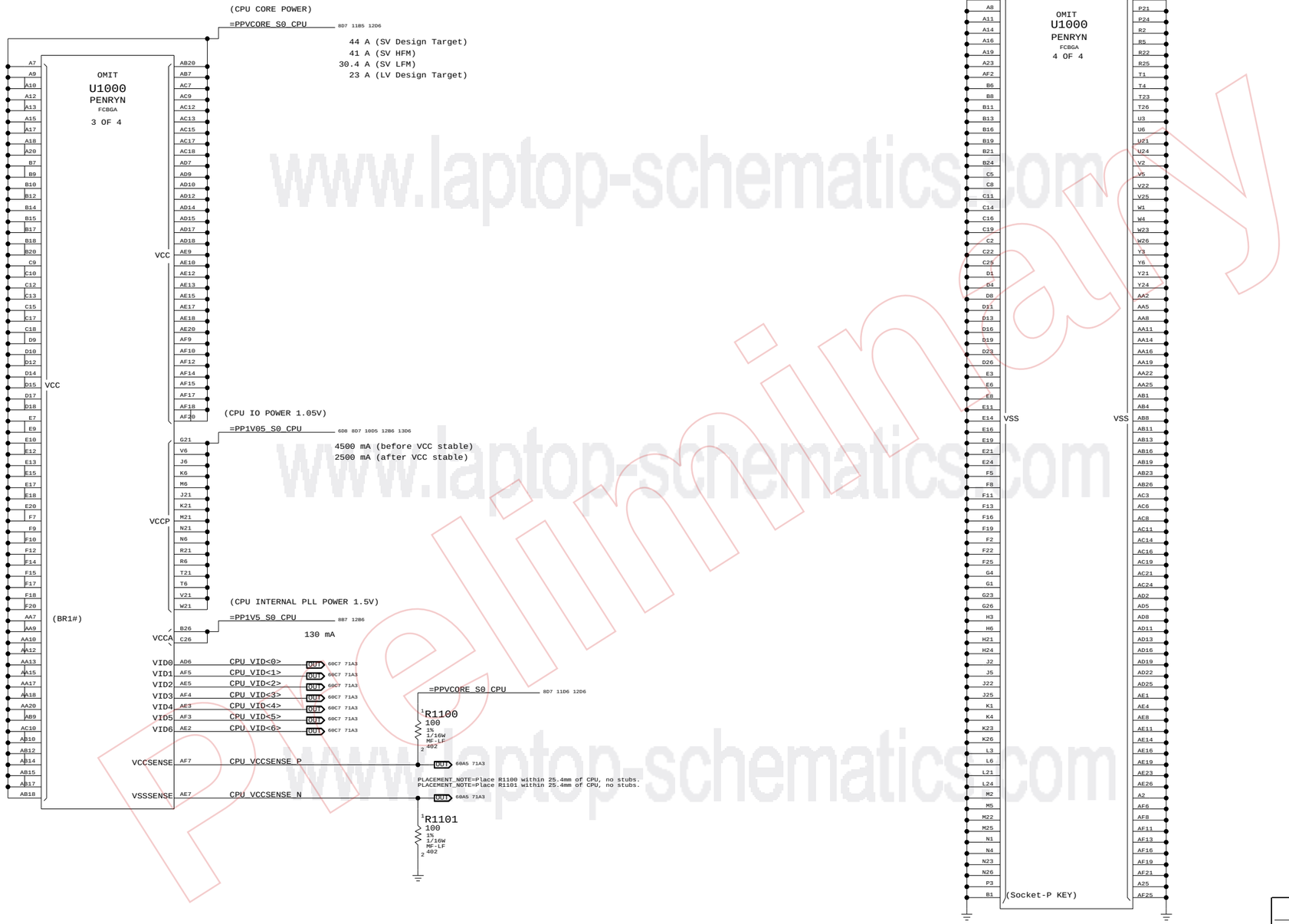
APPLE INC.
SIZE D
DRAWING NUMBER 051-7537
REV. A
SCALE NONE
SHT 10 OF 109



SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

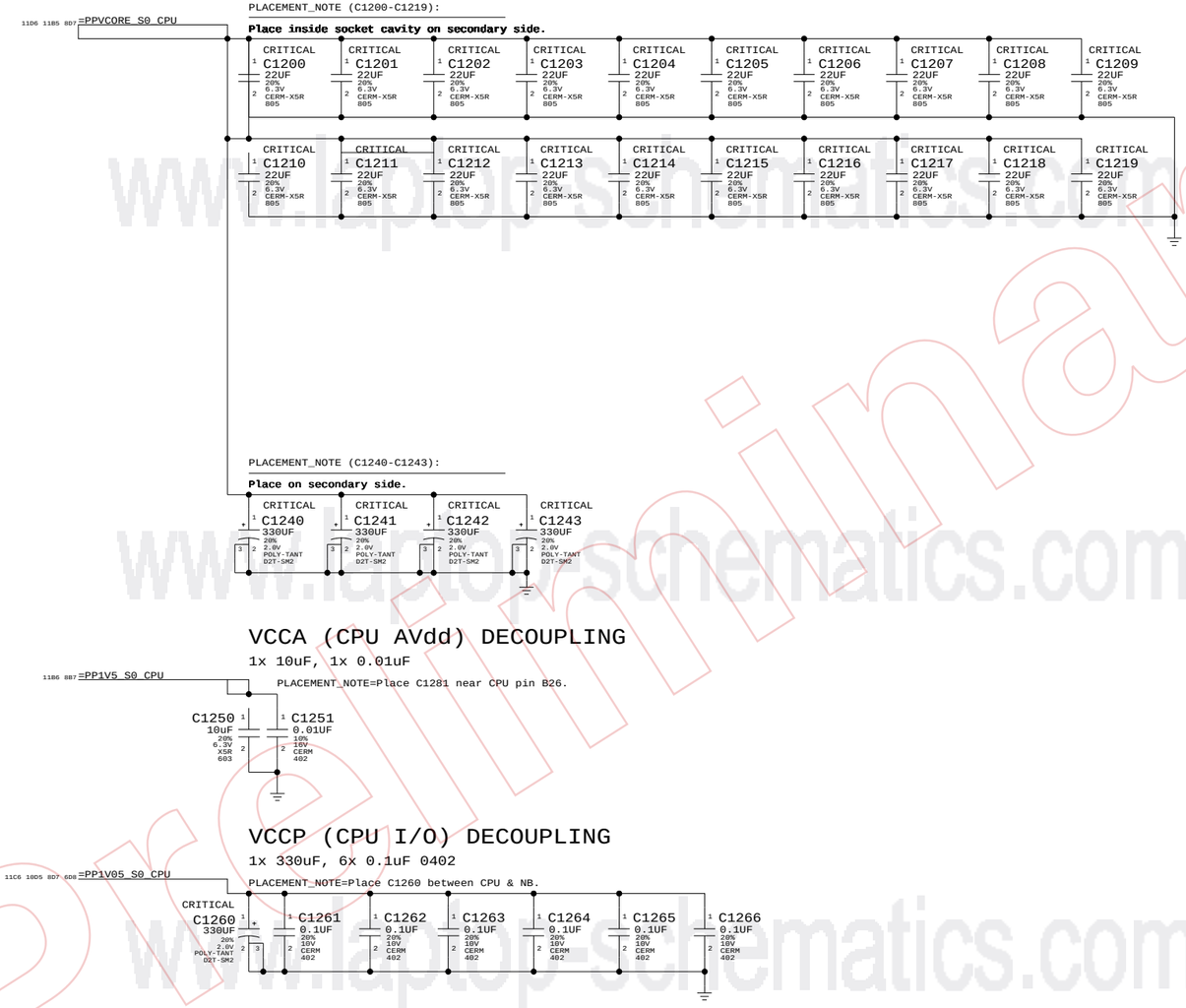
SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 11 OF 109	

CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF

VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

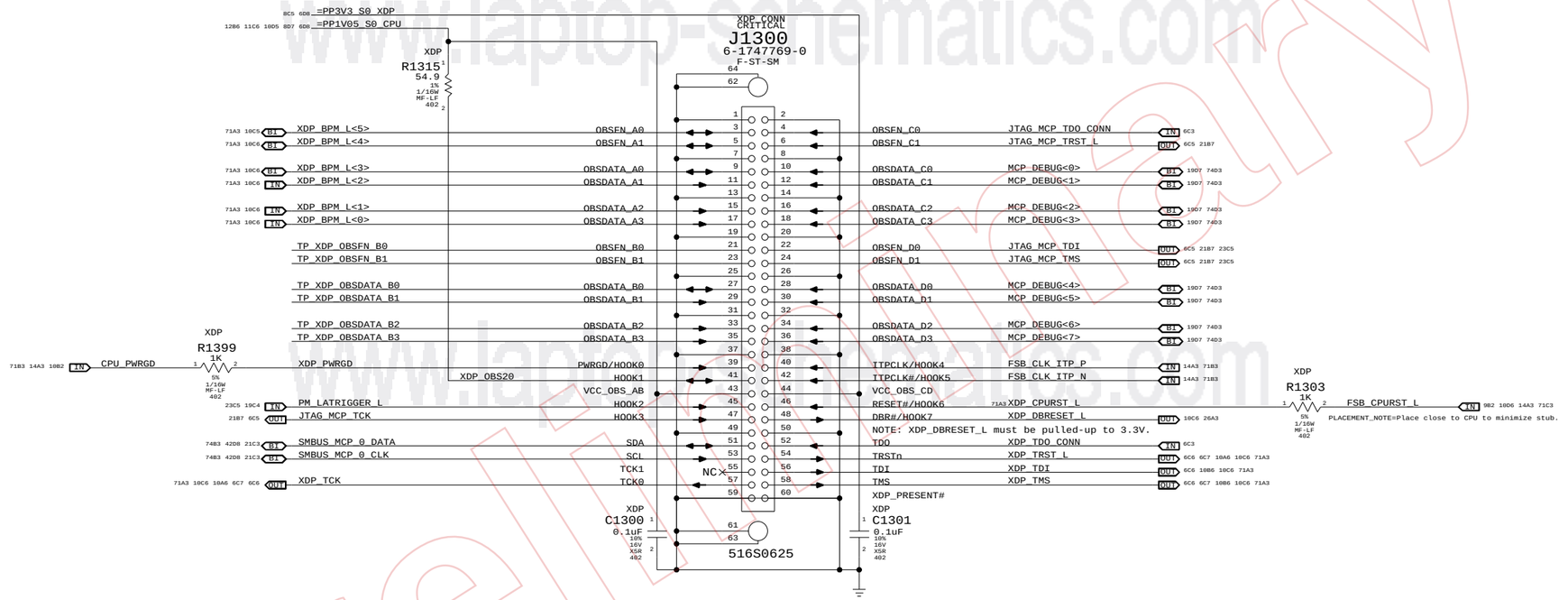
CPU Decoupling

SYNC_MASTER=RAYMOND SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 12 OF 109	

MCP79-specific pinout



SYNC FROM T18
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
RENAME XDP_TDO TO XDP_TDO_CONN

eXtended Debug Port (XDP)

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 13 OF 109	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

71D3 10C4	BI	FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#			
71D3 10C4	BI	FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#			
71D3 10C4	BI	FSB_DINV_L<0>	V41	CPU_DBI0#			
71D3 10B4	BI	FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#			
71D3 10B4	BI	FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#			
71D3 10B4	BI	FSB_DINV_L<1>	V35	CPU_DBI1#			
71D3 10C2	BI	FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#			
71D3 10C2	BI	FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#			
71D3 10C2	BI	FSB_DINV_L<2>	N35	CPU_DBI2#			
71D3 10B2	BI	FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#			
71D3 10B2	BI	FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#			
71D3 10B2	BI	FSB_DINV_L<3>	J41	CPU_DBI3#			
71D3 10D8	BI	FSB_A_L<3>	AC34	CPU_A3#			
71D3 10D8	BI	FSB_A_L<4>	AE38	CPU_A4#			
71D3 10D8	BI	FSB_A_L<5>	AE34	CPU_A5#			
71D3 10D8	BI	FSB_A_L<6>	AC37	CPU_A6#			
71D3 10D8	BI	FSB_A_L<7>	AE37	CPU_A7#			
71D3 10D8	BI	FSB_A_L<8>	AE35	CPU_A8#			
71D3 10D8	BI	FSB_A_L<9>	AB35	CPU_A9#			
71D3 10D8	BI	FSB_A_L<10>	AF35	CPU_A10#			
71D3 10D8	BI	FSB_A_L<11>	AG35	CPU_A11#			
71D3 10D8	BI	FSB_A_L<12>	AG39	CPU_A12#			
71D3 10D8	BI	FSB_A_L<13>	AE33	CPU_A13#			
71D3 10D8	BI	FSB_A_L<14>	AG37	CPU_A14#			
71D3 10D8	BI	FSB_A_L<15>	AG38	CPU_A15#			
71D3 10D8	BI	FSB_A_L<16>	AG34	CPU_A16#			
71C3 10C8	BI	FSB_A_L<17>	AN38	CPU_A17#			
71C3 10C8	BI	FSB_A_L<18>	AL39	CPU_A18#			
71C3 10C8	BI	FSB_A_L<19>	AG33	CPU_A19#			
71C3 10C8	BI	FSB_A_L<20>	AL33	CPU_A20#			
71C3 10C8	BI	FSB_A_L<21>	AJ33	CPU_A21#			
71C3 10C8	BI	FSB_A_L<22>	AN36	CPU_A22#			
71C3 10C8	BI	FSB_A_L<23>	AJ35	CPU_A23#			
71C3 10C8	BI	FSB_A_L<24>	AJ37	CPU_A24#			
71C3 10C8	BI	FSB_A_L<25>	AJ36	CPU_A25#			
71C3 10C8	BI	FSB_A_L<26>	AJ38	CPU_A26#			
71C3 10C8	BI	FSB_A_L<27>	AL37	CPU_A27#			
71C3 10C8	BI	FSB_A_L<28>	AL34	CPU_A28#			
71C3 10C8	BI	FSB_A_L<29>	AN37	CPU_A29#			
71C3 10C8	BI	FSB_A_L<30>	AJ34	CPU_A30#			
71C3 10C8	BI	FSB_A_L<31>	AL38	CPU_A31#			
71C3 10C8	BI	FSB_A_L<32>	AL35	CPU_A32#			
71C3 10C8	BI	FSB_A_L<33>	AN34	CPU_A33#			
71C3 10C8	BI	FSB_A_L<34>	AR39	CPU_A34#			
71C3 10C8	BI	FSB_A_L<35>	AN35	CPU_A35#			
71C3 10D8	BI	FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#			
71C3 10C8	BI	FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#			
71C3 10D8	BI	FSB_REQ_L<0>	AC38	CPU_REQ0#			
71C3 10D8	BI	FSB_REQ_L<1>	AA33	CPU_REQ1#			
71C3 10D8	BI	FSB_REQ_L<2>	AC39	CPU_REQ2#			
71C3 10D8	BI	FSB_REQ_L<3>	AC33	CPU_REQ3#			
71C3 10D8	BI	FSB_REQ_L<4>	AC35	CPU_REQ4#			
71C3 10D6	BI	FSB_ADS_L	AD42	CPU_ADS#			
71C3 10D6	BI	FSB_BNR_L	AD43	CPU_BNR#			
71C3 10D6 98C2	BI	FSB_BREQ0_L	AE40	CPU_BR0#			
71C3		FSB_BREQ1_L	AL32	CPU_BR1#			
71C3 10D6	BI	FSB_DBSY_L	AD39	CPU_DBSY#			
71C3 10D6	BI	FSB_DRDY_L	AD41	CPU_DRDY#			
71C3 10C6	BI	FSB_HIT_L	AB42	CPU_HIT#			
71C3 10C6	BI	FSB_HITM_L	AD40	CPU_HITM#			
71C3 10D6	IN	FSB_LOCK_L	AC43	CPU_LOCK#			
71C3 10D6	OUT	FSB_TRDY_L	AE41	CPU_TRDY#			
9C4	OUT	CPU_PECI_MCP	E41	CPU_PECI			
71B3 60C8 40D4 10C5	OUT	CPU_PROCHOT_L	AJ41	CPU_PROCHOT#			
			AG43	CPU_THERMTRIP#			
			AH40	CPU_FERR#			
9C1	IN	=MCP_BSEL<2>	(MCP_BSEL<2>)	F42	CPU_BSEL2		
9C1	IN	=MCP_BSEL<1>	(MCP_BSEL<1>)	D42	CPU_BSEL1		
9C1	IN	=MCP_BSEL<0>	(MCP_BSEL<0>)	F41	CPU_BSEL0		
71C3 10D6	OUT	FSB_RS_L<0>	AC41	CPU_RS0#			
71C3 10D6	OUT	FSB_RS_L<1>	AB41	CPU_RS1#			
71C3 10D6	OUT	FSB_RS_L<2>	AC42	CPU_RS2#			

CPU_D0#	Y43	FSB_D_L<0>	BI	10C4 71D3			
CPU_D1#	W42	FSB_D_L<1>	BI	10C4 71D3			
CPU_D2#	Y40	FSB_D_L<2>	BI	10C4 71D3			
CPU_D3#	W41	FSB_D_L<3>	BI	10C4 71D3			
CPU_D4#	Y39	FSB_D_L<4>	BI	10C4 71D3			
CPU_D5#	V42	FSB_D_L<5>	BI	10C4 71D3			
CPU_D6#	Y41	FSB_D_L<6>	BI	10C4 71D3			
CPU_D7#	Y42	FSB_D_L<7>	BI	10C4 71D3			
CPU_D8#	P42	FSB_D_L<8>	BI	10C4 71D3			
CPU_D9#	U41	FSB_D_L<9>	BI	10C4 71D3			
CPU_D10#	R42	FSB_D_L<10>	BI	10C4 71D3			
CPU_D11#	T39	FSB_D_L<11>	BI	10C4 71D3			
CPU_D12#	T42	FSB_D_L<12>	BI	10C4 71D3			
CPU_D13#	T41	FSB_D_L<13>	BI	10C4 71D3			
CPU_D14#	R41	FSB_D_L<14>	BI	10C4 71D3			
CPU_D15#	T43	FSB_D_L<15>	BI	10C4 71D3			
CPU_D16#	W35	FSB_D_L<16>	BI	10C4 71D3			
CPU_D17#	AA37	FSB_D_L<17>	BI	10C4 71D3			
CPU_D18#	W33	FSB_D_L<18>	BI	10C4 71D3			
CPU_D19#	W34	FSB_D_L<19>	BI	10B4 71D3			
CPU_D20#	AA36	FSB_D_L<20>	BI	10B4 71D3			
CPU_D21#	AA34	FSB_D_L<21>	BI	10B4 71D3			
CPU_D22#	AA38	FSB_D_L<22>	BI	10B4 71D3			
CPU_D23#	AA35	FSB_D_L<23>	BI	10B4 71D3			
CPU_D24#	U38	FSB_D_L<24>	BI	10B4 71D3			
CPU_D25#	U36	FSB_D_L<25>	BI	10B4 71D3			
CPU_D26#	U35	FSB_D_L<26>	BI	10B4 71D3			
CPU_D27#	U33	FSB_D_L<27>	BI	10B4 71D3			
CPU_D28#	U34	FSB_D_L<28>	BI	10B4 71D3			
CPU_D29#	W38	FSB_D_L<29>	BI	10B4 71D3			
CPU_D30#	R33	FSB_D_L<30>	BI	10B4 71D3			
CPU_D31#	U37	FSB_D_L<31>	BI	10B4 71D3			
CPU_D32#	N34	FSB_D_L<32>	BI	10C2 71D3			
CPU_D33#	N33	FSB_D_L<33>	BI	10C2 71D3			
CPU_D34#	R34	FSB_D_L<34>	BI	10C2 71D3			
CPU_D35#	R35	FSB_D_L<35>	BI	10C2 71D3			
CPU_D36#	P35	FSB_D_L<36>	BI	10C2 71D3			
CPU_D37#	R39	FSB_D_L<37>	BI	10C2 71D3			
CPU_D38#	R37	FSB_D_L<38>	BI	10C2 71D3			
CPU_D39#	R38	FSB_D_L<39>	BI	10C2 71D3			
CPU_D40#	L37	FSB_D_L<40>	BI	10C2 71D3			
CPU_D41#	L39	FSB_D_L<41>	BI	10C2 71D3			
CPU_D42#	L38	FSB_D_L<42>	BI	10C2 71D3			
CPU_D43#	N36	FSB_D_L<43>	BI	10C2 71D3			
CPU_D44#	N38	FSB_D_L<44>	BI	10C2 71D3			
CPU_D45#	J39	FSB_D_L<45>	BI	10C2 71D3			
CPU_D46#	J38	FSB_D_L<46>	BI	10C2 71D3			
CPU_D47#	J37	FSB_D_L<47>	BI	10C2 71D3			
CPU_D48#	L42	FSB_D_L<48>	BI	10C2 71D3			
CPU_D49#	M42	FSB_D_L<49>	BI	10C2 71D3			
CPU_D50#	P41	FSB_D_L<50>	BI	10C2 71D3			
CPU_D51#	N41	FSB_D_L<51>	BI	10B2 71D3			
CPU_D52#	N40	FSB_D_L<52>	BI	10B2 71D3			
CPU_D53#	M40	FSB_D_L<53>	BI	10B2 71D3			
CPU_D54#	H40	FSB_D_L<54>	BI	10B2 71D3			
CPU_D55#	K42	FSB_D_L<55>	BI	10B2 71D3			
CPU_D56#	H41	FSB_D_L<56>	BI	10B2 71D3			
CPU_D57#	L41	FSB_D_L<57>	BI	10B2 71D3			
CPU_D58#	H43	FSB_D_L<58>	BI	10B2 71D3			
CPU_D59#	H42	FSB_D_L<59>	BI	10B2 71D3			
CPU_D60#	K41	FSB_D_L<60>	BI	10B2 71D3			
CPU_D61#	J40	FSB_D_L<61>	BI	10B2 71D3			
CPU_D62#	H39	FSB_D_L<62>	BI	10B2 71D3			
CPU_D63#	M43	FSB_D_L<63>	BI	10B2 71D3			
CPU_BPRI#	AA41	FSB_BPRI_L	OUT	10D6 71C3			
CPU_DEFER#	AA40	FSB_DEFER_L	OUT	10D6 71C3			
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	OUT	10B6 71B3			
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	OUT	10B6 71B3			
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	OUT	13C3 71B3			
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	OUT	13B3 71B3			
BCLK_OUT_NB_P	AL41	71B3 FSB_CLK_MCP_P					
BCLK_OUT_NB_N	AK42	71B3 FSB_CLK_MCP_N					
BCLK_IN_N	AK41						
BCLK_IN_P	AJ40						
CPU_A20M#	AF41	CPU_A20M_L	OUT	10C8 71C3			
CPU_IGNNE#	AH39	CPU_IGNNE_L	OUT	10C8 71C3			
CPU_INIT#	AH42	CPU_INIT_L	OUT	10D6 71C3			
CPU_INTR	AF42	CPU_INTR	OUT	98J 10B8 71C3			
CPU_NMI	AG41	CPU_NMI	OUT	98J 10B8 71C3			
CPU_SMI#	AH41	CPU_SMI_L	OUT	10B8 71B3			
CPU_PWRGD	AH43	CPU_PWRGD	OUT	10B2 13C7 71B3			
CPU_RESET#	H38	FSB_CPURST_L	OUT	98J 10D6 13B2 71C3			
CPU_SLP#	AM33	FSB_CPUSLP_L	OUT	10A2 71B3			
CPU_DPSLP#	AN33	CPU_DPSLP_L	OUT	10B2 71B3			
CPU_DPWR#	AM32	FSB_DPWR_L	OUT	10B2 71B3			
CPU_STPCLK#	AG42	CPU_STPCLK_L	OUT	10B8 71B3			
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	OUT	98J 10B2 60C7 71B3			

Loop-back clock for delay matching.

24C8 22D3 14A2 9C2 8D7 =PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

71B3 40C4 10C6 IN PM_THRMTRIP_L
71C3 10C8 IN CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
NO STUFF
R1421 1K 5% 1/16W MF-LF 402
NO STUFF
R1422 1K 5% 1/16W MF-LF 402

9C1 IN =MCP_BSEL<2>
9C1 IN =MCP_BSEL<1>
9C1 IN =MCP_BSEL<0>

24C2 PP1V05_S0_MCP_PLL_FSB
270 mA (A01)

206 mA	AG27	+V_DLL_DLCELL_AVDD
20 mA	AH27	+V_PLL_MCLK
29 mA	AG28	+V_PLL_FSB
15 mA	AH28	+V_PLL_CPU

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402

71B3 MCP_BCLK_VML_COMP_VDD AM39 BCLK_VML_COMP_VDD
71B3 MCP_BCLK_VML_COMP_GND AM40 BCLK_VML_COMP_GND

71B3 MCP_CPU_COMP_VCC AM43 CPU_COMP_VCC
71B3 MCP_CPU_COMP_GND AM42 CPU_COMP_GND

R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

=PP1V05_S0_MCP_FSB 8D7 9C2 14B7 22D3 24C8
NO STUFF
R1440 150 5% 1/16W MF-LF 402
OUT 10B2 13C7 71B3

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP CPU Interface

SYNC_MASTER=T18_MLB
SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 14 OF 109	

OMIT

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MCP79-TOPO-B
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MEMORY PARTITION 0

MEM_A_DQ<63>	AL8	MDQ0_63	MDQS0_7_P	AL10	MEM_A_DQS_P<7>	28A5	72C3
MEM_A_DQ<62>	AL9	MDQ0_62	MDQS0_7_N	AL11	MEM_A_DQS_N<7>	28A5	72C3
MEM_A_DQ<61>	AP9	MDQ0_61	MDQS0_6_P	AR8	MEM_A_DQS_P<6>	28B7	72C3
MEM_A_DQ<60>	AN9	MDQ0_60	MDQS0_6_N	AR9	MEM_A_DQS_N<6>	28B7	72C3
MEM_A_DQ<59>	AL6	MDQ0_59	MDQS0_5_P	AW7	MEM_A_DQS_P<5>	28B5	72C3
MEM_A_DQ<58>	AL7	MDQ0_58	MDQS0_5_N	AW8	MEM_A_DQS_N<5>	28B5	72C3
MEM_A_DQ<57>	AN6	MDQ0_57	MDQS0_4_P	AP13	MEM_A_DQS_P<4>	28B7	72C3
MEM_A_DQ<56>	AN7	MDQ0_56	MDQS0_4_N	AR13	MEM_A_DQS_N<4>	28B7	72C3
MEM_A_DQ<55>	AR6	MDQ0_55	MDQS0_3_P	AV25	MEM_A_DQS_P<3>	28C4	72C3
MEM_A_DQ<54>	AR7	MDQ0_54	MDQS0_3_N	AW25	MEM_A_DQS_N<3>	28C4	72C3
MEM_A_DQ<53>	AV6	MDQ0_53	MDQS0_2_P	AU30	MEM_A_DQS_P<2>	28B2	72C3
MEM_A_DQ<52>	AW5	MDQ0_52	MDQS0_2_N	AU29	MEM_A_DQS_N<2>	28B2	72C3
MEM_A_DQ<51>	AN10	MDQ0_51	MDQS0_1_P	AT35	MEM_A_DQS_P<1>	28C4	72C3
MEM_A_DQ<50>	AR5	MDQ0_50	MDQS0_1_N	AU35	MEM_A_DQS_N<1>	28C4	72C3
MEM_A_DQ<49>	AU6	MDQ0_49	MDQS0_0_P	AU39	MEM_A_DQS_P<0>	28C2	72C3
MEM_A_DQ<48>	AV5	MDQ0_48	MDQS0_0_N	AT39	MEM_A_DQS_N<0>	28C2	72C3
MEM_A_DQ<47>	AU7	MDQ0_47					
MEM_A_DQ<46>	AU8	MDQ0_46					
MEM_A_DQ<45>	AW9	MDQ0_45					
MEM_A_DQ<44>	AP11	MDQ0_44					
MEM_A_DQ<43>	AW6	MDQ0_43					
MEM_A_DQ<42>	AY5	MDQ0_42	MRAS0#	AV17	MEM_A_RAS_L	28C5	72D3
MEM_A_DQ<41>	AU9	MDQ0_41	MCAS0#	AP17	MEM_A_CAS_L	28C7	72D3
MEM_A_DQ<40>	AV9	MDQ0_40	MWE0#	AR17	MEM_A_WE_L	28C7	72D3
MEM_A_DQ<39>	AU11	MDQ0_39					
MEM_A_DQ<38>	AV11	MDQ0_38					
MEM_A_DQ<37>	AV13	MDQ0_37					
MEM_A_DQ<36>	AW13	MDQ0_36					
MEM_A_DQ<35>	AR11	MDQ0_35					
MEM_A_DQ<34>	AT11	MDQ0_34	MBA0_2	AP23	MEM_A_BA<2>	28C7	72D3
MEM_A_DQ<33>	AR14	MDQ0_33	MBA0_1	AP19	MEM_A_BA<1>	28C5	72D3
MEM_A_DQ<32>	AU13	MDQ0_32	MBA0_0	AW17	MEM_A_BA<0>	28C7	72D3
MEM_A_DQ<31>	AR26	MDQ0_31					
MEM_A_DQ<30>	AU25	MDQ0_30					
MEM_A_DQ<29>	AT27	MDQ0_29					
MEM_A_DQ<28>	AU27	MDQ0_28					
MEM_A_DQ<27>	AP25	MDQ0_27	MA0_14	AR23	MEM_A_A<14>	28C5	72D3
MEM_A_DQ<26>	AR25	MDQ0_26	MA0_13	AU15	MEM_A_A<13>	28C7	72D3
MEM_A_DQ<25>	AP27	MDQ0_25	MA0_12	AN23	MEM_A_A<12>	28C7	72D3
MEM_A_DQ<24>	AR27	MDQ0_24	MA0_11	AW21	MEM_A_A<11>	28C5	72D3
MEM_A_DQ<23>	AP29	MDQ0_23	MA0_10	AN19	MEM_A_A<10>	28C7	72D3
MEM_A_DQ<22>	AR29	MDQ0_22	MA0_9	AV21	MEM_A_A<9>	28C7	72D3
MEM_A_DQ<21>	AP31	MDQ0_21	MA0_8	AR22	MEM_A_A<8>	28C7	72D3
MEM_A_DQ<20>	AR31	MDQ0_20	MA0_7	AU21	MEM_A_A<7>	28C5	72D3
MEM_A_DQ<19>	AV27	MDQ0_19	MA0_6	AP21	MEM_A_A<6>	28C5	72D3
MEM_A_DQ<18>	AN29	MDQ0_18	MA0_5	AR21	MEM_A_A<5>	28C7	72D3
MEM_A_DQ<17>	AV29	MDQ0_17	MA0_4	AN21	MEM_A_A<4>	28C5	72D3
MEM_A_DQ<16>	AN31	MDQ0_16	MA0_3	AV19	MEM_A_A<3>	28C7	72D3
MEM_A_DQ<15>	AU31	MDQ0_15	MA0_2	AU19	MEM_A_A<2>	28C5	72D3
MEM_A_DQ<14>	AR33	MDQ0_14	MA0_1	AT19	MEM_A_A<1>	28C7	72D3
MEM_A_DQ<13>	AV37	MDQ0_13	MA0_0	AR19	MEM_A_A<0>	28C5	72D3
MEM_A_DQ<12>	AW37	MDQ0_12					
MEM_A_DQ<11>	AT31	MDQ0_11					
MEM_A_DQ<10>	AV31	MDQ0_10					
MEM_A_DQ<9>	AT37	MDQ0_9					
MEM_A_DQ<8>	AU37	MDQ0_8					
MEM_A_DQ<7>	AW39	MDQ0_7					
MEM_A_DQ<6>	AV39	MDQ0_6					
MEM_A_DQ<5>	AR37	MDQ0_5					
MEM_A_DQ<4>	AR38	MDQ0_4					
MEM_A_DQ<3>	AV38	MDQ0_3					
MEM_A_DQ<2>	AW38	MDQ0_2					
MEM_A_DQ<1>	AR35	MDQ0_1					
MEM_A_DQ<0>	AP35	MDQ0_0					
MEM_A_DM<7>	AN5	MDQM0_7					
MEM_A_DM<6>	AU5	MDQM0_6					
MEM_A_DM<5>	AR10	MDQM0_5					
MEM_A_DM<4>	AN13	MDQM0_4	MODT0A_1	AP15	MEM_A_ODT<1>	28C5	72D3
MEM_A_DM<3>	AN27	MDQM0_3	MODT0A_0	AV15	MEM_A_ODT<0>	28C5	72D3
MEM_A_DM<2>	AW29	MDQM0_2					
MEM_A_DM<1>	AV35	MDQM0_1	MCKE0A_1	AU23	MEM_A_CKE<1>	28D5	72D3
MEM_A_DM<0>	AR34	MDQM0_0	MCKE0A_0	AT23	MEM_A_CKE<0>	28D7	72D3

MEMORY CONTROL 0A

MCLK0A_2_P	AW33	TP_MEM_A_CLK2P	
MCLK0A_2_N	AV33	TP_MEM_A_CLK2N	
MCLK0A_1_P	BA24	MEM_A_CLK_P<1>	28C5 72D3
MCLK0A_1_N	AY24	MEM_A_CLK_N<1>	28C5 72D3
MCLK0A_0_P	BB20	MEM_A_CLK_P<0>	28C7 72D3
MCLK0A_0_N	BC20	MEM_A_CLK_N<0>	28C7 72D3
MCS0A_1#	AT15	MEM_A_CS_L<1>	28C7 72D3
MCS0A_0#	AR18	MEM_A_CS_L<0>	28C5 72D3

OMIT

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BGA
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MEMORY PARTITION 1

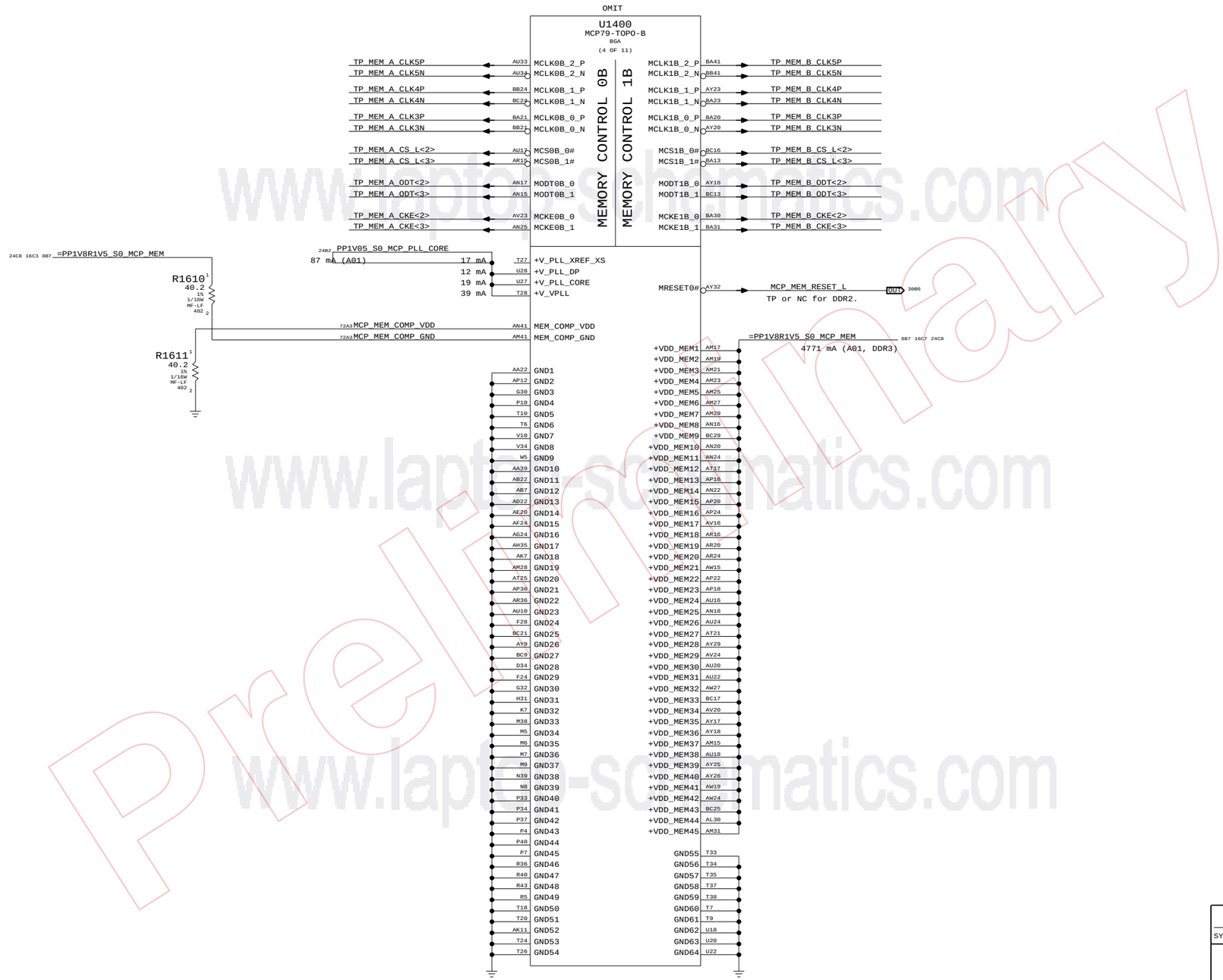
MEM_B_DQ<63>	AT4	MDQ1_63	MDQS1_7_P	AT2	MEM_B_DQS_P<7>	29A5	72A3
MEM_B_DQ<62>	AT3	MDQ1_62	MDQS1_7_N	AT1	MEM_B_DQS_N<7>	29A5	72A3
MEM_B_DQ<61>	AV2	MDQ1_61	MDQS1_6_P	AY2	MEM_B_DQS_P<6>	29B7	72A3
MEM_B_DQ<60>	AV3	MDQ1_60	MDQS1_6_N	AY1	MEM_B_DQS_N<6>	29B7	72A3
MEM_B_DQ<59>	AR4	MDQ1_59	MDQS1_5_P	BB6	MEM_B_DQS_P<5>	29B5	72A3
MEM_B_DQ<58>	AR3	MDQ1_58	MDQS1_5_N	BA6	MEM_B_DQS_N<5>	29B5	72A3
MEM_B_DQ<57>	AU2	MDQ1_57	MDQS1_4_P	BA10	MEM_B_DQS_P<4>	29B7	72A3
MEM_B_DQ<56>	AU3	MDQ1_56	MDQS1_4_N	AY11	MEM_B_DQS_N<4>	29B7	72A3
MEM_B_DQ<55>	AY4	MDQ1_55	MDQS1_3_P	BB33	MEM_B_DQS_P<3>	29B2	72A3
MEM_B_DQ<54>	AY3	MDQ1_54	MDQS1_3_N	BA33	MEM_B_DQS_N<3>	29B2	72A3
MEM_B_DQ<53>	BB3	MDQ1_53	MDQS1_2_P	BB37	MEM_B_DQS_P<2>	29C4	72A3
MEM_B_DQ<52>	BC3	MDQ1_52	MDQS1_2_N	BA37	MEM_B_DQS_N<2>	29C4	72A3
MEM_B_DQ<51>	AW4	MDQ1_51	MDQS1_1_P	BA43	MEM_B_DQS_P<1>	29C4	72A3
MEM_B_DQ<50>	AW3	MDQ1_50	MDQS1_1_N	AY42	MEM_B_DQS_N<1>	29C4	72A3
MEM_B_DQ<49>	BA3	MDQ1_49	MDQS1_0_P	AT42	MEM_B_DQS_P<0>	29C2	72A3
MEM_B_DQ<48>	BB2	MDQ1_48	MDQS1_0_N	AT43	MEM_B_DQS_N<0>	29C2	72A3
MEM_B_DQ<47>	BB5	MDQ1_47					
MEM_B_DQ<46>	BA5	MDQ1_46					
MEM_B_DQ<45>	BA8	MDQ1_45					
MEM_B_DQ<44>	BC8	MDQ1_44					
MEM_B_DQ<43>	BB4	MDQ1_43					
MEM_B_DQ<42>	BC4	MDQ1_42	MRAS1#	AW16	MEM_B_RAS_L	29C5	72B3
MEM_B_DQ<41>	BA7	MDQ1_41	MCAS1#	BA15	MEM_B_CAS_L	29C7	72B3
MEM_B_DQ<40>	AY8	MDQ1_40	MWE1#	BA16	MEM_B_WE_L	29C7	72B3
MEM_B_DQ<39>	BA9	MDQ1_39					
MEM_B_DQ<38>	BB10	MDQ1_38					
MEM_B_DQ<37>	BB12	MDQ1_37					
MEM_B_DQ<36>	AW12	MDQ1_36					
MEM_B_DQ<35>	BB8	MDQ1_35					
MEM_B_DQ<34>	BB9	MDQ1_34	MBA1_2	BB29	MEM_B_BA<2>	29C7	72B3
MEM_B_DQ<33>	AY12	MDQ1_33	MBA1_1	BB18	MEM_B_BA<1>	29C5	72B3
MEM_B_DQ<32>	BA12	MDQ1_32	MBA1_0	BB17	MEM_B_BA<0>	29C7	72B3
MEM_B_DQ<31>	BC32	MDQ1_31					
MEM_B_DQ<30>	AW32	MDQ1_30					
MEM_B_DQ<29>	BA35	MDQ1_29					
MEM_B_DQ<28>	AY36	MDQ1_28					
MEM_B_DQ<27>	BA32	MDQ1_27	MA1_14	BA29	MEM_B_A<14>	29C5	72B3
MEM_B_DQ<26>	BB32	MDQ1_26	MA1_13	BA14	MEM_B_A<13>	29C7	72B3
MEM_B_DQ<25>	BA34	MDQ1_25	MA1_12	AW28	MEM_B_A<12>	29C7	72B3
MEM_B_DQ<24>	AY35	MDQ1_24	MA1_11	BC28	MEM_B_A<11>	29C5	72B3
MEM_B_DQ<23>	BC36	MDQ1_23	MA1_10	BA17	MEM_B_A<10>	29C7	72B3
MEM_B_DQ<22>	AW36	MDQ1_22	MA1_9	BB28	MEM_B_A<9>	29C7	72B3
MEM_B_DQ<21>	BA39	MDQ1_21	MA1_8	AY28	MEM_B_A<8>	29C7	72B3
MEM_B_DQ<20>	AY40	MDQ1_20	MA1_7	BA28	MEM_B_A<7>	29C5	72B3
MEM_B_DQ<19>	BA36	MDQ1_19	MA1_6	AY27	MEM_B_A<6>	29C5	72B3
MEM_B_DQ<18>	BB36	MDQ1_18	MA1_5	BA27	MEM_B_A<5>	29C7	72B3
MEM_B_DQ<17>	BA38	MDQ1_17	MA1_4	BA26	MEM_B_A<4>	29C5	72B3
MEM_B_DQ<16>	AY39	MDQ1_16	MA1_3	BB26	MEM_B_A<3>	29C7	72B3
MEM_B_DQ<15>	BB40	MDQ1_15	MA1_2	BA25	MEM_B_A<2>	29C5	72B3
MEM_B_DQ<14>	AW40	MDQ1_14	MA1_1	BB25	MEM_B_A<1>	29C7	72B3
MEM_B_DQ<13>	AV42	MDQ1_13	MA1_0	BA18	MEM_B_A<0>	29C5	72B3
MEM_B_DQ<12>	AV41	MDQ1_12					
MEM_B_DQ<11>	BA40	MDQ1_11					
MEM_B_DQ<10>	BC40	MDQ1_10					
MEM_B_DQ<9>	AW42	MDQ1_9					
MEM_B_DQ<8>	AW41	MDQ1_8					
MEM_B_DQ<7>	AT40	MDQ1_7					
MEM_B_DQ<6>	AT41	MDQ1_6					
MEM_B_DQ<5>	AP41	MDQ1_5					
MEM_B_DQ<4>	AN40	MDQ1_4					
MEM_B_DQ<3>	AU40	MDQ1_3					
MEM_B_DQ<2>	AU41	MDQ1_2					
MEM_B_DQ<1>	AR41	MDQ1_1					
MEM_B_DQ<0>	AP42	MDQ1_0					
MEM_B_DM<7>	AT5	MDQM1_7					
MEM_B_DM<6>	BA2	MDQM1_6					
MEM_B_DM<5>	AY7	MDQM1_5					
MEM_B_DM<4>	BA11	MDQM1_4	MODT1A_1	BB13	MEM_B_ODT<1>	29C5	72B3
MEM_B_DM<3>	BB34	MDQM1_3	MODT1A_0	AY15	MEM_B_ODT<0>	29C5	72B3
MEM_B_DM<2>	BB38	MDQM1_2					
MEM_B_DM<1>	AY43	MDQM1_1	MCKE1A_1	AY31	MEM_B_CKE<1>	29D5	72B3
MEM_B_DM<0>	AR42	MDQM1_0	MCKE1A_0	BB30	MEM_B_CKE<0>	29D7	72B3

MEMORY CONTROL 1A

MCLK1A_2_P	BA42	TP_MEM_B_CLK2P	
MCLK1A_2_N	BB42	TP_MEM_B_CLK2N	
MCLK1A_1_P	BB22	MEM_B_CLK_P<1>	29C5 72B3
MCLK1A_1_N	BA22	MEM_B_CLK_N<1>	29C5 72B3
MCLK1A_0_P	BA19	MEM_B_CLK_P<0>	29C7 72B3
MCLK1A_0_N	AY19	MEM_B_CLK_N<0>	29C7 72B3
MCS1A_1#	BB14	MEM_B_CS_L<1>	29C7 72B3
MCS1A_0#	BB16	MEM_B_CS_L<0>	29C5 72B3

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 15 OF 109	



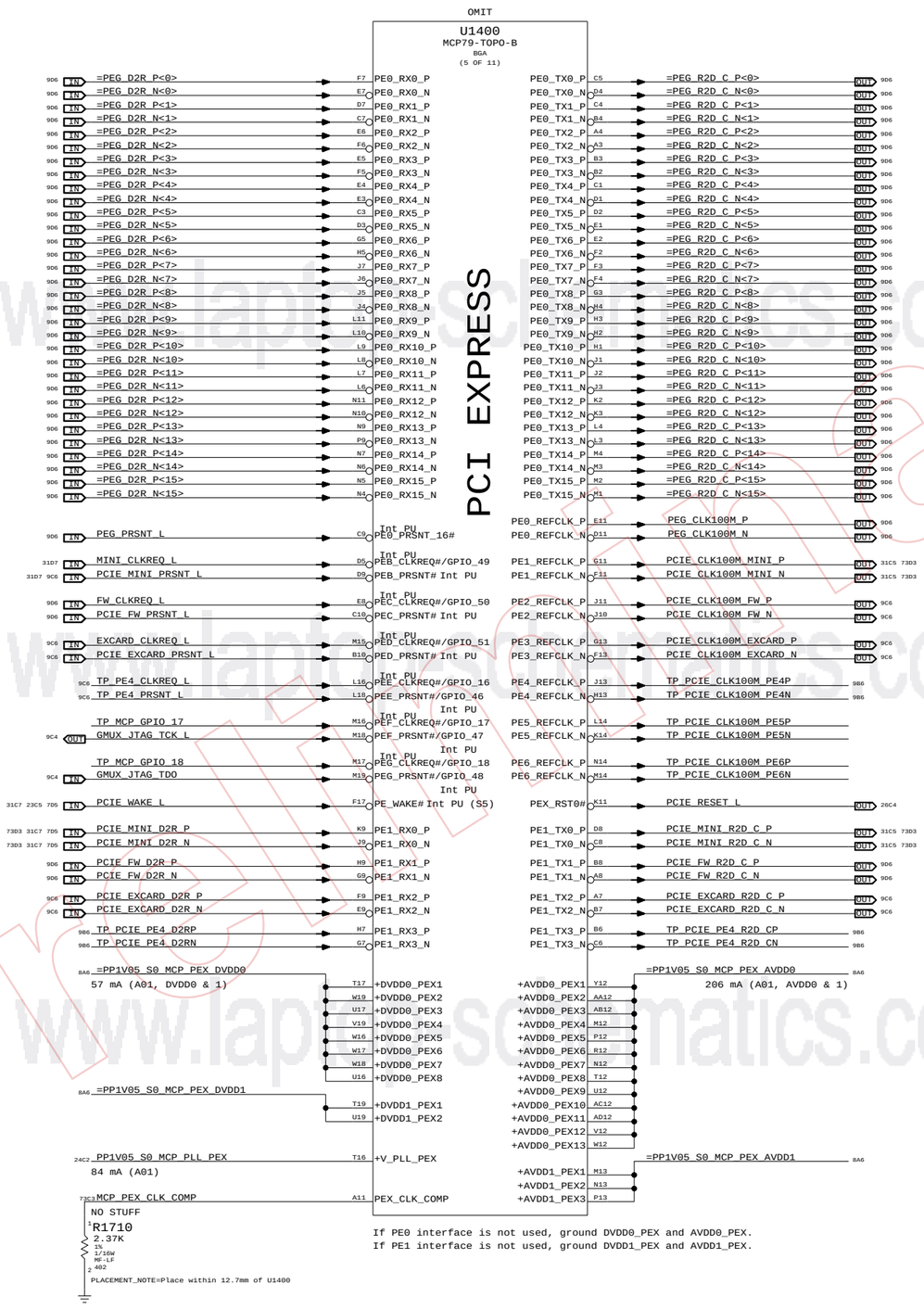
MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 16 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 17 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
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LAN

75D3 33C1	IN	ENET_RXD<0>	RGMII_RXD0 C23
75D3 33C1	IN	ENET_RXD<1>	RGMII_RXD1 B23
75D3 33C1	IN	ENET_RXD<2>	RGMII_RXD2 E24
75D3 33B1	IN	ENET_RXD<3>	RGMII_RXD3 A24
75D3 33C1	IN	ENET_CLK125M_RXCLK	RGMII_RXC/MII_RXCLK A23
75D3 33B1	IN	ENET_RX_CTRL	RGMII_RXCTL/MII_RXDV C22
9C4	IN	=MCP_MII_RXER	MII_RXER/GPIO_36 F23
9C4	IN	=MCP_MII_COL	MII_COL/GPIO_20/MSMB_DATA B26
9C4	IN	=MCP_MII_CRS	MII_CRS/GPIO_21/MSMB_CLK B22
		TP_ENET_INTR_L	RGMII_INTR/GPIO_35 J22
24A6		PP1V05_ENET_MCP_PLL_MAC	+V_DUAL_MACPLL T23
		5 mA (A01)	
75D3		MCP_MII_COMP_VDD	MII_COMP_VDD C27
75D3		MCP_MII_COMP_GND	MII_COMP_GND B27
		TP_MCP_RGB_DAC_RSET	RGB_DAC_RSET C39
		TP_MCP_RGB_DAC_VREF	RGB_DAC_VREF B38
9D4	OUT	MCP_TV_DAC_RSET	TV_DAC_RSET E36
9D4	OUT	MCP_TV_DAC_VREF	TV_DAC_VREF A35
9D4	IN	MCP_CLK27M_XTALIN	XTALIN_TV C38
9D4	OUT	MCP_CLK27M_XTALOUT	XTALOUT_TV D38
41C3	BI	LPCPLUS_GPIO	GPIO_6/FERR*/IGPU_GPIO_6 E16
67A5	IN	DP_IG_CA_DET	GPIO_7/NFERR*/IGPU_GPIO_7 B15
78A7 69A8	OUT	LVDS_IG_BKL_PWM	LCD_BKL_CTL/GPIO_57 G39
78C8 78B7	OUT	LVDS_IG_BKL_ON	LCD_BKL_ON/GPIO_59 E37
66B8	OUT	LVDS_IG_PANEL_PWR	LCD_PANEL_PWR/GPIO_58 F40
67D3	OUT	=MCP_HDMI_TXC_P	HDMI_TXC_P/ML0_LANE3_P D35
67D3	OUT	=MCP_HDMI_TXC_N	HDMI_TXC_N/ML0_LANE3_N E35
67D3	OUT	=MCP_HDMI_TXD_P<0>	HDMI_TXD0_P/ML0_LANE2_P G35
67D3	OUT	=MCP_HDMI_TXD_N<0>	HDMI_TXD0_N/ML0_LANE2_N F35
67D3	OUT	=MCP_HDMI_TXD_P<1>	HDMI_TXD1_P/ML0_LANE1_P F33
67D3	OUT	=MCP_HDMI_TXD_N<1>	HDMI_TXD1_N/ML0_LANE1_N G33
67D3	OUT	=MCP_HDMI_TXD_P<2>	HDMI_TXD2_P/ML0_LANE0_P J33
67D3	OUT	=MCP_HDMI_TXD_N<2>	HDMI_TXD2_N/ML0_LANE0_N H33
73B3 67C7	OUT	DP_IG_AUX_CH_P	DP_AUX_CH0_P D43
73B3 67B7	OUT	DP_IG_AUX_CH_N	DP_AUX_CH0_N C43
9B4	IN	=DVI_HPD_GMUX_INT	HPLUG_DET2/GPIO_22 C31
67D3	IN	=MCP_HDMI_HPD	HPLUG_DET3 F31
25D7 8A7		=PP3V3R1V8_S0_MCP_IFP_VDD	+VDD_IFPA M27
		190 mA (A01, 1.8V)	+VDD_IFPB M26
25B5		PP3V3_S0_MCP_VPLL	+V_PLL_IFPAB M28
		16 mA (A01)	8 mA
			8 mA +V_PLL_HDMI M29
25D7 8B7		=PP1V05_S0_MCP_HDMI_VDD	+VDD_HDMI T25
		95 mA (A01)	
73B3 25C7	OUT	MCP_HDMI_RSET	HDMI_RSET J31
73B3 25C7	OUT	MCP_HDMI_VPROBE	HDMI_VPROBE J30

(See below)

(See below)

DACS

RGB ONLY

TV / Component
C / Pr
Y / Y
Comp / Pb

		=PP3V3_ENET_MCP_RMGT	8B1 18C7 24A6 24B6
			83 mA (A01)
		+3.3V_DUAL_RMGT1	J24
		+3.3V_DUAL_RMGT2	K24
		=PP1V05_ENET_MCP_RMGT	8B1 24C6
			131 mA (A01)
		+V_DUAL_RMGT1	U23
		+V_DUAL_RMGT2	V23
		MII_VREF	E28 MCP_MII_VREF IN 24A4
		RGMII_TXD0	B24 ENET_TXD<0> OUT 33C6 75C3
		RGMII_TXD1	C24 ENET_TXD<1> OUT 33C6 75C3
		RGMII_TXD2	C25 ENET_TXD<2> OUT 33C6 75C3
		RGMII_TXD3	D25 ENET_TXD<3> OUT 33B6 75C3
		RGMII_TXC/MII_TXCLK	D24 ENET_CLK125M_TXCLK OUT 33C8 75D3
		RGMII_TXCTL/MII_TXEN	C26 ENET_TX_CTRL OUT 33B6 75C3
		RGMII_MDC	D21 ENET_MDC OUT 33B6 75D3
		RGMII_MDIO	C21 ENET_MDIO BI 33B6 75D3
		RGMII_PWRDWN/GPIO_37	G23 TP_ENET_PWRDWN_L
		BUF_25MHZ	E23 MCP_CLK25M_BUF0_R OUT 34A5 75D3
		MII_RESET#	J23 ENET_RESET_L OUT 33B7 75C3
		PP3V3_S0_MCP_DAC	25D2
		+V_RGB_DAC	J32 103 mA
		+V_TV_DAC	K32 103 mA
			206 mA (A01)
		DDC_CLK0	B31 MCP_DDC_CLK0
		DDC_DATA0	A31 MCP_DDC_DATA0
		RGB_DAC_RED	B39 TP_MCP_RGB_RED
		RGB_DAC_GREEN	A39 TP_MCP_RGB_GREEN
		RGB_DAC_BLUE	B40 TP_MCP_RGB_BLUE
		RGB_DAC_HSYNC	A40 TP_MCP_RGB_HSYNC
		RGB_DAC_VSYNC	A41 TP_MCP_RGB_VSYNC
		TV_DAC_RED	A36 CRT_IG_R_C_PR OUT 9D4
		TV_DAC_GREEN	B36 CRT_IG_G_Y_Y OUT 9D4
		TV_DAC_BLUE	C36 CRT_IG_B_COMP_PB OUT 9D4
		TV_DAC_HSYNC/GPIO_44	D36 CRT_IG_HSYNC OUT 9D4
		TV_DAC_VSYNC/GPIO_45	C37 CRT_IG_VSYNC OUT 9D4

FLAT PANEL

		IFPA_TXC_P	B35 LVDS_IG_A_CLK_P OUT 66B3 73B3
		IFPA_TXC_N	C35 LVDS_IG_A_CLK_N OUT 66B3 73B3
		IFPA_TXD0_P	B32 LVDS_IG_A_DATA_P<0> OUT 7C7 66C2 73B3
		IFPA_TXD0_N	A32 LVDS_IG_A_DATA_N<0> OUT 7C7 66C2 73B3
		IFPA_TXD1_P	D32 LVDS_IG_A_DATA_P<1> OUT 7C7 66C2 73B3
		IFPA_TXD1_N	C32 LVDS_IG_A_DATA_N<1> OUT 7C7 66C2 73B3
		IFPA_TXD2_P	D33 LVDS_IG_A_DATA_P<2> OUT 7C7 66C2 73B3
		IFPA_TXD2_N	C33 LVDS_IG_A_DATA_N<2> OUT 7C7 66C2 73B3
		IFPA_TXD3_P	B34 LVDS_IG_A_DATA_P<3> OUT 9D4
		IFPA_TXD3_N	C34 LVDS_IG_A_DATA_N<3> OUT 9D4
		IFPB_TXC_P	L31 LVDS_IG_B_CLK_P OUT 9C4
		IFPB_TXC_N	K31 LVDS_IG_B_CLK_N OUT 9C4
		IFPB_TXD4_P	J29 LVDS_IG_B_DATA_P<0> OUT 9C4
		IFPB_TXD4_N	H29 LVDS_IG_B_DATA_N<0> OUT 9C4
		IFPB_TXD5_P	L29 LVDS_IG_B_DATA_P<1> OUT 9C4
		IFPB_TXD5_N	K29 LVDS_IG_B_DATA_N<1> OUT 9C4
		IFPB_TXD6_P	L30 LVDS_IG_B_DATA_P<2> OUT 9C4
		IFPB_TXD6_N	K30 LVDS_IG_B_DATA_N<2> OUT 9C4
		IFPB_TXD7_P	N30 LVDS_IG_B_DATA_P<3> OUT 9C4
		IFPB_TXD7_N	M30 LVDS_IG_B_DATA_N<3> OUT 9C4
		DDC_CLK2/GPIO_23	C30 LVDS_IG_DDC_CLK OUT 7C7 66C5
		DDC_DATA2/GPIO_24	B30 LVDS_IG_DDC_DATA BI 7C7 66B5
		DDC_CLK3	D31 =MCP_HDMI_DDC_CLK OUT 67D3
		DDC_DATA3	E31 =MCP_HDMI_DDC_DATA BI 67D3
		IFPAB_RSET	E32 MCP_IFPAB_RSET OUT 25C6 73A3
		IFPAB_VPROBE	G31 MCP_IFPAB_VPROBE OUT 25C6 73A3

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

24B6 24A6 18D3 8B1 =PP3V3_ENET_MCP_RMGT

R1810 49.9 1% 1/16W MF-LF 402

R1811 49.9 1% 1/16W MF-LF 402

20C1 8A3 =PP3V3_S5_MCP_GPIO

R1820 47K 5% 1/16W MF-LF 402

R1850 10K 5% 1/16W MF-LF 402

=PP3V3_S0_MCP_GPIO 8C5 19D1 21A4

R1860 100K 5% 1/16W MF-LF 402

R1861 100K 5% 1/16W MF-LF 402

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 18 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
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PCI

74D3 19D2	PCI_REQ0_L	T2	PCI_REQ0#
74D3 19D2	PCI_REQ1_L	V9	PCI_REQ1#/FANRPM2
19D2 OUT	CRTMUX_SEL_TV_L	T3	PCI_REQ2#/GPIO_40/RS232_DSR#
52C7 OUT	AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#
19D2 IN	MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#
74D3 13C3 BI	MCP_DEBUG<0>	AC3	PCI_AD0
74D3 13C3 BI	MCP_DEBUG<1>	AE10	PCI_AD1
74D3 13C3 BI	MCP_DEBUG<2>	AC4	PCI_AD2
74D3 13C3 BI	MCP_DEBUG<3>	AE11	PCI_AD3
74D3 13C3 BI	MCP_DEBUG<4>	AB3	PCI_AD4
74D3 13C3 BI	MCP_DEBUG<5>	AC6	PCI_AD5
74D3 13C3 BI	MCP_DEBUG<6>	AB2	PCI_AD6
74D3 13C3 BI	MCP_DEBUG<7>	AC7	PCI_AD7
	TP_PCI_AD<8>	AC8	PCI_AD8
	TP_PCI_AD<9>	AA2	PCI_AD9
	TP_PCI_AD<10>	AC9	PCI_AD10
	TP_PCI_AD<11>	AC10	PCI_AD11
	TP_PCI_AD<12>	AC11	PCI_AD12
	TP_PCI_AD<13>	AA1	PCI_AD13
	TP_PCI_AD<14>	AA5	PCI_AD14
	TP_PCI_AD<15>	Y5	PCI_AD15
	TP_PCI_AD<16>	W3	PCI_AD16
	TP_PCI_AD<17>	W6	PCI_AD17
	TP_PCI_AD<18>	W4	PCI_AD18
	TP_PCI_AD<19>	W7	PCI_AD19
	TP_PCI_AD<20>	V3	PCI_AD20
	TP_PCI_AD<21>	W8	PCI_AD21
	TP_PCI_AD<22>	V2	PCI_AD22
	TP_PCI_AD<23>	W9	PCI_AD23
	TP_PCI_AD<24>	U3	PCI_AD24
	TP_PCI_AD<25>	W11	PCI_AD25
	TP_PCI_AD<26>	U2	PCI_AD26
	TP_PCI_AD<27>	U5	PCI_AD27
	TP_PCI_AD<28>	U1	PCI_AD28
	TP_PCI_AD<29>	U6	PCI_AD29
	TP_PCI_AD<30>	T5	PCI_AD30
	TP_PCI_AD<31>	U7	PCI_AD31
	TP_PCI_INTW_L	P2	PCI_INTW#
	TP_PCI_INTX_L	N3	PCI_INTX#
	TP_PCI_INTY_L	N2	PCI_INTY#
	TP_PCI_INTZ_L	N1	PCI_INTZ#
	TP_PCI_TRDY_L	Y3	PCI_TRDY#
41D5 39C5 IN	PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42
9C4 IN	FW_PME_L	AE2	LPC_DRQ1#/GPIO_19 Int PU
	TP_LPC_DRQ0_L	AE1	LPC_DRQ0# Int PU
41D3 39C8 BI	LPC_SERIRQ	AE6	LPC_SERIRQ Int PU

PCI_GNT0#	R3	TP_PCI_GNT0_L	
PCI_GNT1#/FANCTL2	U10	TP_PCI_GNT1_L	
PCI_GNT2#/GPIO_41/RS232_DTR#	R4	GMUX_JTAG_TMS	OUT 9C4
PCI_GNT3#/GPIO_39/RS232_RTS#	U11	GMUX_JTAG_TDI	OUT 9C4
PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	OUT 19D2
PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>	
PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>	
PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>	
PCI_CBE3#	W10	TP_PCI_C_BE_L<3>	
PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L	
PCI_FRAME#	Y4	TP_PCI_FRAME_L	
PCI_IRDY#	AA10	TP_PCI_IRDY_L	
PCI_PAR	Y1	TP_PCI_PAR	
PCI_PERR#/GPIO_43/RS232_DCD#	AB9	TP_PCI_PERR_L	
PCI_SERR#	AA7	TP_PCI_SERR_L	
PCI_STOP#	Y2	TP_PCI_STOP_L	
PCI_PME#/GPIO_30 Int PU (S5)	T1	PM_LATRIGGER_L	OUT 13B6 23C5
PCI_RESET0#	R10	MEM_VTT_EN_R	OUT 26C4
PCI_RESET1#	R11	TP_PCI_RESET1_L	
PCI_CLK0	R6	TP_PCI_CLK0	
PCI_CLK1	R7	TP_PCI_CLK1	
PCI_CLK2	R8	74C3 PCI_CLK33M_MCP_R	
PCI_CLKIN	R9	74C3 PCI_CLK33M_MCP	

R1910 22 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	39C1 LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402 LPC_FRAME_L OUT 39C8 41D5 74C3
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L	OUT 39C5 41D3
LPC_RESET0#	AE5	LPC_RESET_L	OUT 26D4 74C3
LPC_AD0	AD3	LPC_AD_R<0>	R1950 22 5% 1/16W MF-LF 402 LPC_AD<0> BI 39C8 41D5 74C3
LPC_AD1	AD2	LPC_AD_R<1>	R1951 22 5% 1/16W MF-LF 402 LPC_AD<1> BI 39C8 41D5 74C3
LPC_AD2	AD1	LPC_AD_R<2>	R1952 22 5% 1/16W MF-LF 402 LPC_AD<2> BI 39C8 41D3 74C3
LPC_AD3	AD5	LPC_AD_R<3>	R1953 22 5% 1/16W MF-LF 402 LPC_AD<3> BI 39C8 41D3 74C3
LPC_CLK0	AE9	LPC_CLK33M_SMC_R	OUT 26C4 74C3

R1961 10K 5% 1/16W MF-LF 402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

21A4 18C1 8C5 =PP3V3_S0_MCP_GPIO

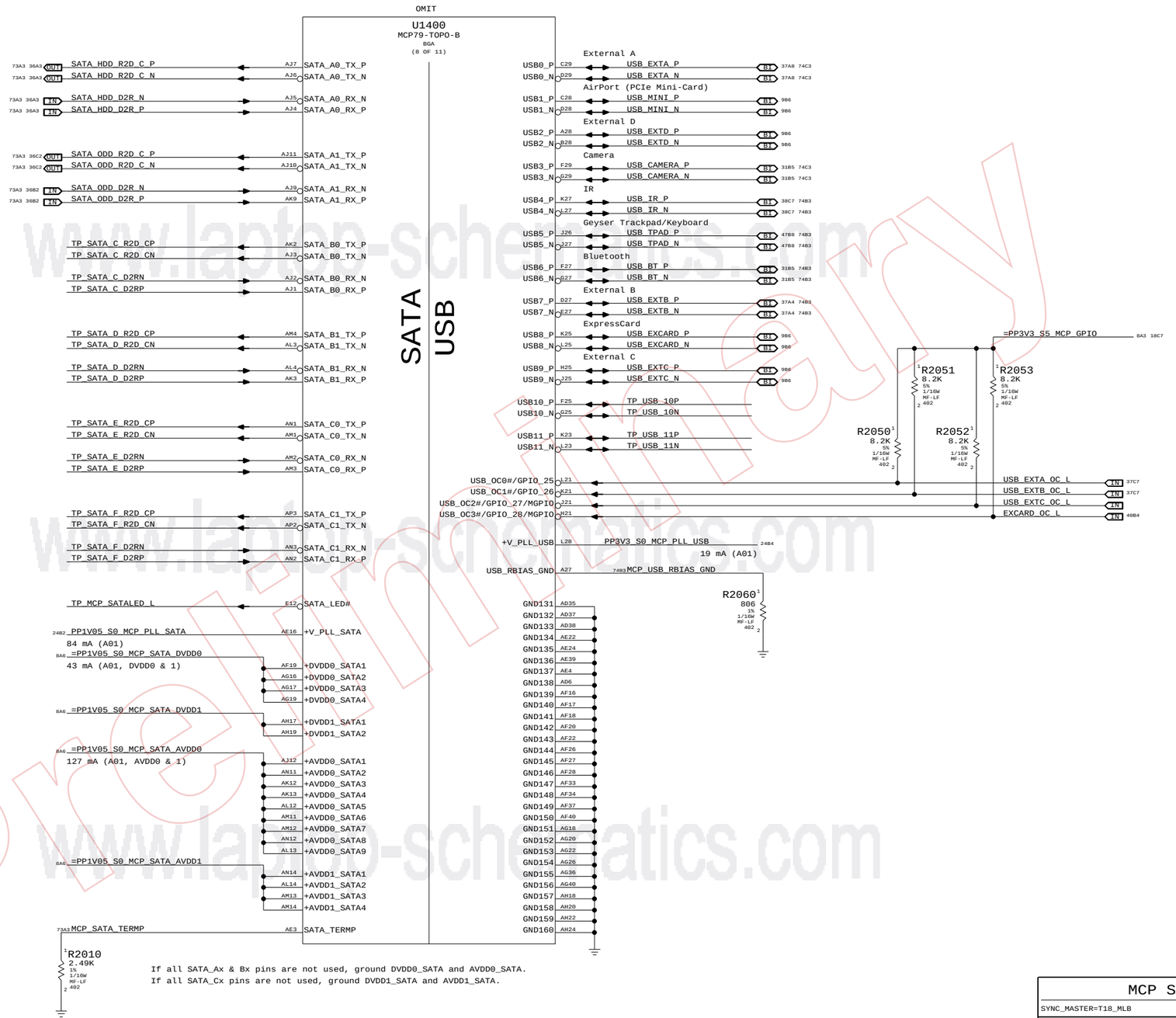
19D4	MCP_RS232_SOUT_L	R1989	8.2K 5% 1/16W MF-LF 402
74D3 19D7	PCI_REQ0_L	R1990	8.2K 5% 1/16W MF-LF 402
74D3 19D7	PCI_REQ1_L	R1991	8.2K 5% 1/16W MF-LF 402
19D7	CRTMUX_SEL_TV_L	R1992	8.2K 5% 1/16W MF-LF 402
19D7	MCP_RS232_SIN_L	R1994	8.2K 5% 1/16W MF-LF 402

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 19 OF 109	



If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB

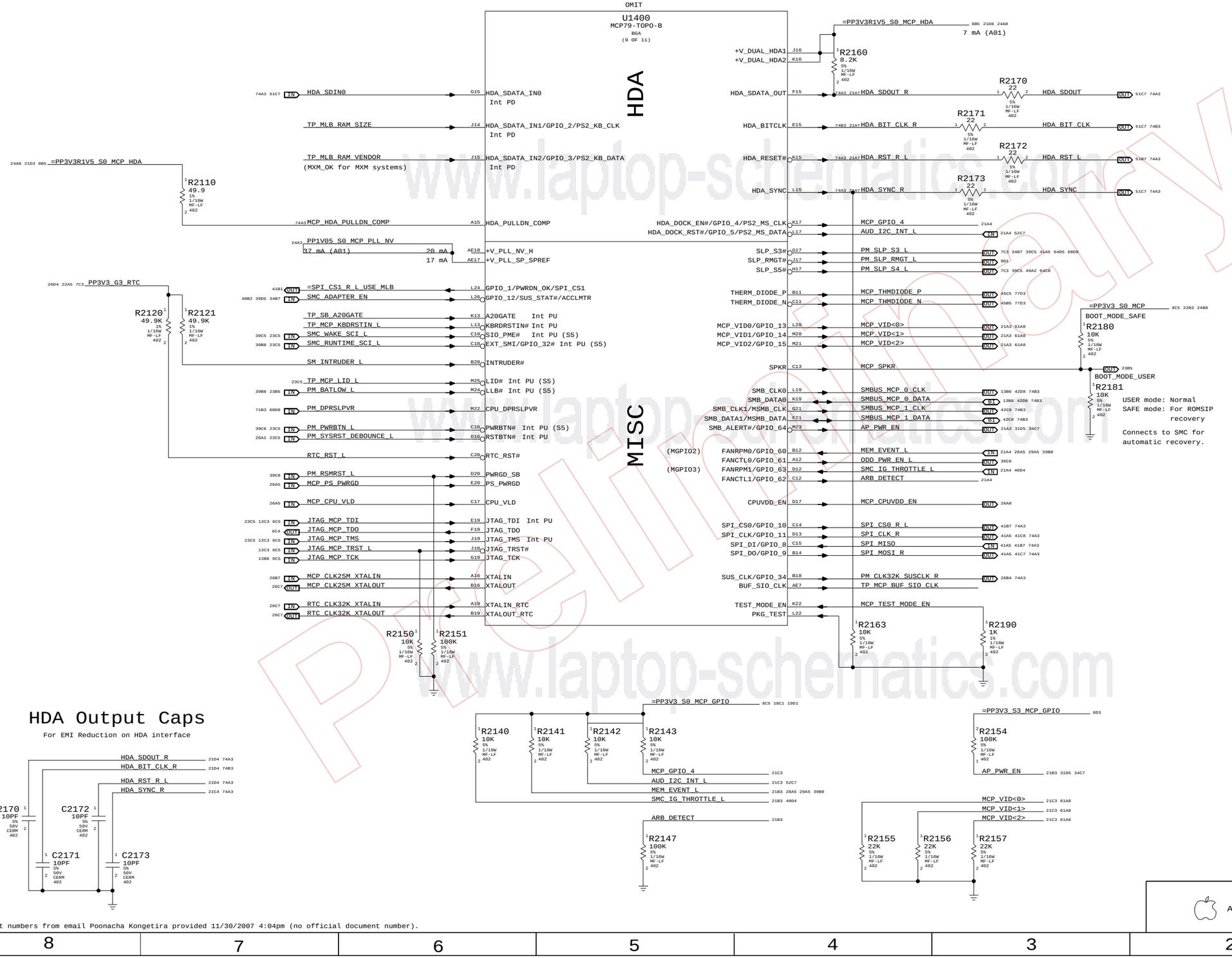
SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE	SHT	OF
NONE	20	109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE: NONE SHT 21 OF 109

OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

61B1 44D7 24D8 8C8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

AA25	+VDD_CORE1	+VTT_CPU1	R32	
AC23	+VDD_CORE2	+VTT_CPU2	AC32	
U25	+VDD_CORE3	+VTT_CPU3	E40	
AH12	+VDD_CORE4	+VTT_CPU4	J36	
AG10	+VDD_CORE5	+VTT_CPU5	N32	
AG5	+VDD_CORE6	+VTT_CPU6	T32	
Y21	+VDD_CORE7	+VTT_CPU7	U32	
Y23	+VDD_CORE8	+VTT_CPU8	V32	
AA16	+VDD_CORE9	+VTT_CPU9	W32	
AA26	+VDD_CORE10	+VTT_CPU10	P31	
AA27	+VDD_CORE11	+VTT_CPU11	AF32	
AA28	+VDD_CORE12	+VTT_CPU12	AE32	
AC16	+VDD_CORE13	+VTT_CPU13	AH32	
AC17	+VDD_CORE14	+VTT_CPU14	AJ32	
AC18	+VDD_CORE15	+VTT_CPU15	AK31	
AC19	+VDD_CORE16	+VTT_CPU16	AK32	
AC20	+VDD_CORE17	+VTT_CPU17	AD32	
AC21	+VDD_CORE18	+VTT_CPU18	AL31	
AA17	+VDD_CORE19	+VTT_CPU19	AB32	
AC24	+VDD_CORE20	+VTT_CPU20	B41	
AC25	+VDD_CORE21	+VTT_CPU21	B42	
AC26	+VDD_CORE22	+VTT_CPU22	C40	
AC27	+VDD_CORE23	+VTT_CPU23	C41	
AC28	+VDD_CORE24	+VTT_CPU24	C42	
AD21	+VDD_CORE25	+VTT_CPU25	D39	
AD23	+VDD_CORE26	+VTT_CPU26	D40	
W27	+VDD_CORE27	+VTT_CPU27	D41	
V25	+VDD_CORE28	+VTT_CPU28	E38	
AA18	+VDD_CORE29	+VTT_CPU29	E39	
AE19	+VDD_CORE30	+VTT_CPU30	F37	
AE21	+VDD_CORE31	+VTT_CPU31	F38	
AE23	+VDD_CORE32	+VTT_CPU32	F39	
AE25	+VDD_CORE33	+VTT_CPU33	G36	
AE26	+VDD_CORE34	+VTT_CPU34	G37	
AE27	+VDD_CORE35	+VTT_CPU35	G38	
AE28	+VDD_CORE36	+VTT_CPU36	H35	
AF10	+VDD_CORE37	+VTT_CPU37	H37	
AF11	+VDD_CORE38	+VTT_CPU38	J34	
AA19	+VDD_CORE39	+VTT_CPU39	J35	
AF2	+VDD_CORE40	+VTT_CPU40	K33	
AF21	+VDD_CORE41	+VTT_CPU41	K34	
AF23	+VDD_CORE42	+VTT_CPU42	K35	
AF25	+VDD_CORE43	+VTT_CPU43	L32	
AF3	+VDD_CORE44	+VTT_CPU44	L33	
AF4	+VDD_CORE45	+VTT_CPU45	L34	
AF7	+VDD_CORE46	+VTT_CPU46	M31	
AH23	+VDD_CORE47	+VTT_CPU47	M32	
AF9	+VDD_CORE48	+VTT_CPU48	M33	
AA20	+VDD_CORE49	+VTT_CPU49	N31	
AG11	+VDD_CORE50	+VTT_CPU50	P32	
AG12	+VDD_CORE51	+VTT_CPU51	Y32	
AG21	+VDD_CORE52	+VTT_CPU52	AA32	
AG23	+VDD_CORE53			
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA
AG3	+VDD_CORE55			
AG4	+VDD_CORE56			
AA21	+VDD_CORE57			
AG6	+VDD_CORE58			
AG7	+VDD_CORE59	+3.3V_1	AD10	=PP3V3_S0_MCP (8C5 21C2 24B8) 450 mA (A01)
AG8	+VDD_CORE60	+3.3V_2	AE8	
AG9	+VDD_CORE61	+3.3V_3	AB10	
AH1	+VDD_CORE62	+3.3V_4	AD9	
AH10	+VDD_CORE63	+3.3V_5	Y10	
AH11	+VDD_CORE64	+3.3V_6	AB11	
W26	+VDD_CORE65	+3.3V_7	AA8	
AH2	+VDD_CORE66	+3.3V_8	Y9	
AA23	+VDD_CORE67			
W28	+VDD_CORE68			
AH25	+VDD_CORE69			=PP3V3_S5_MCP (8A3 24B8)
AH21	+VDD_CORE70	+3.3V_DUAL1	G18	16 mA 266 mA (A01)
AH3	+VDD_CORE71	+3.3V_DUAL2	H19	
AH4	+VDD_CORE72	+3.3V_DUAL3	J20	
AH5	+VDD_CORE73	+3.3V_DUAL4	K20	
AH6	+VDD_CORE74			
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26	250 mA
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27	
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28	
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28	
W23	+VDD_CORE79			
W25	+VDD_CORE80			
AF12	+VDD_CORE81			
		+VDD_AUXC1	T21	=PP1V05_S5_MCP_VDD_AUXC (8B3 24C8) 105 mA (A01)
		+VDD_AUXC2	U21	
A20	+VBAT	+VDD_AUXC3	V21	

=PP1V05_S0_MCP_FSB (8D7 9C2 14A2 14B7 24C8)
1139 mA 1182 mA (A01)

26D4 21C8 7C3 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

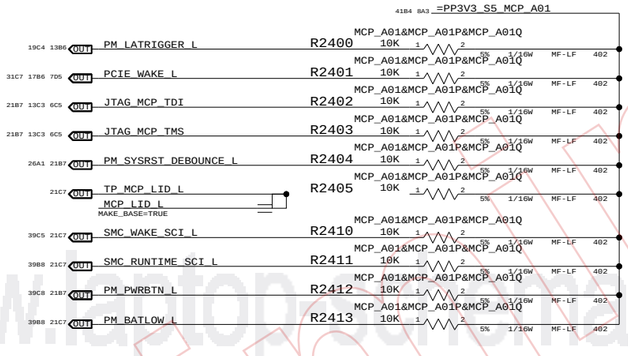
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 22 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

RADAR 5925345

MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/08/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 24 OF 109	

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

61B1 44D7 22D5 8C8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

8B7 8A9 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

8B7 8A9 =PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

22A3 8B3 =PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

18D3 8B1 =PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

14B7 14A2 9C2 8B7 22G3 =PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

16C7 16C3 8B7 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

22B3 21C2 8C9 =PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

8B5 =PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

PP3V3_S0_MCP_PLL_USB 20C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

22B3 8A9 =PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

24A6 18D3 18C7 8B1 =PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

21D8 21D3 8B5 =PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

8B1 =PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC 18C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

MCP79 Ethernet VRef

24B6 18D3 18C7 8B1 =PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402

MCP_MII_VREF OUT 18D3

C2591 0.1UF 20% 10V CERM 402

8B7 =PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

PP1V05_S0_MCP_PEX_AVDD 8A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP1V05_S0_MCP_SATA_AVDD 8A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

8B7 =PP1V05_S0_MCP_PLL_UF
562 mA (A01)

L2580 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_FSB 14A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX 17A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA 20B6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE 16C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV 21C7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 25 OF 109	

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

18B6 8A7 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610 2.2UF 20% 6.3V CERM 402-LF

18A6 8B7 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615 4.7UF 20% 4V X5R 402
C2616 0.1UF 20% 10V CERM 402

73B3 18A6 MCP_HDMI_RSET
73B3 18A6 MCP_HDMI_VPROBE

NO STUFF
C2620 0.1UF 20% 10V CERM 402
R2620 1K 1% 1/16W MF-LF 402

73A3 18A3 MCP_IFPAB_RSET
73A3 18A3 MCP_IFPAB_VPROBE

NO STUFF
C2630 0.1UF 20% 10V CERM 402
NO STUFF
R2630 1K 1% 1/16W MF-LF 402

NO STUFF
L2650 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

8C5 =PP3V3_S0_MCP_DAC_UF
206 mA (A01)

PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18C3
206 mA (A01)

NO STUFF
C2650 2.2UF 20% 6.3V CERM 402-LF
R2651 0 5% 1/16W MF-LF 402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

8C5 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640 30-OHM-1.7A 0402

PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18A6
16 mA (A01)

C2640 4.7UF 20% 6.3V CERM 603
C2641 0.1UF 20% 10V CERM 402

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.

88S =PP3V3_S0_HDCPROM

C2690 0.1UF 20% 10V CERM 402

NOSTUFF
U2695 AT24C08 SOIC
A0 A1 A2 GND
SDA =I2C_HDCPROM_SDA
SCL =I2C_HDCPROM_SCL
WP HDCPROM_WP

R2690 10K 5% 1/16W MF-LF 402

42C6 SDA
42C6 SCL

NOSTUFF
U2690 AT24C01B SOT23
25A7 HDCPROM_WP
WP SDA SCL GND

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

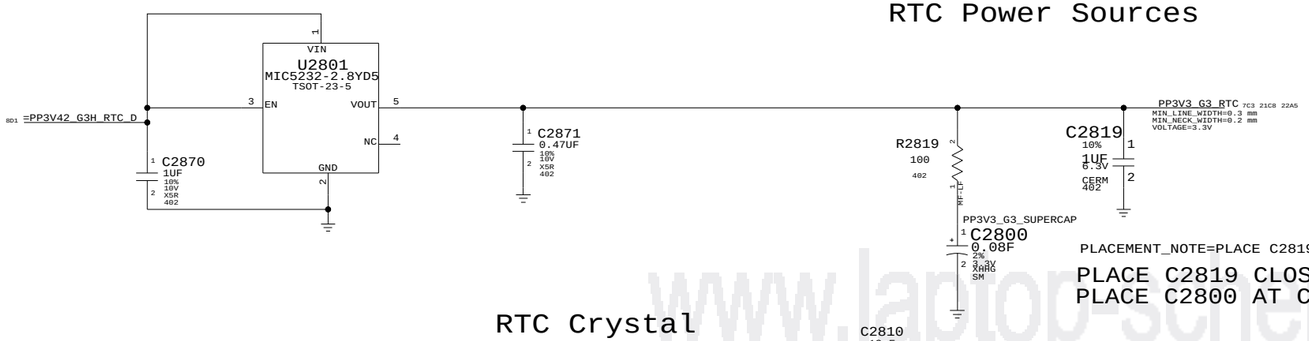
MCP Graphics Support

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 26 OF 109	

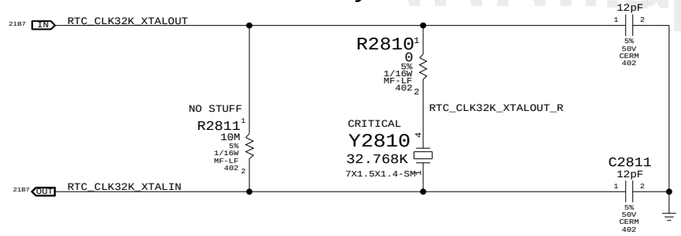
RTC Power Sources



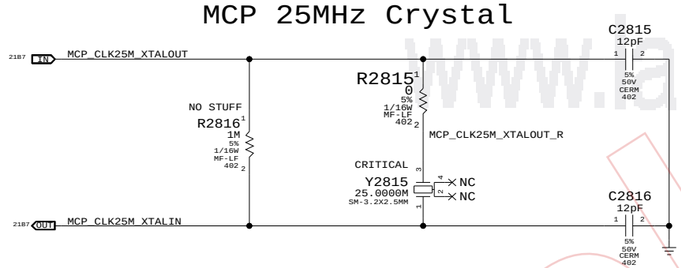
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79

PLACE C2819 CLOSE TO MCP79
PLACE C2800 AT COOLEST SPOT ON MLB

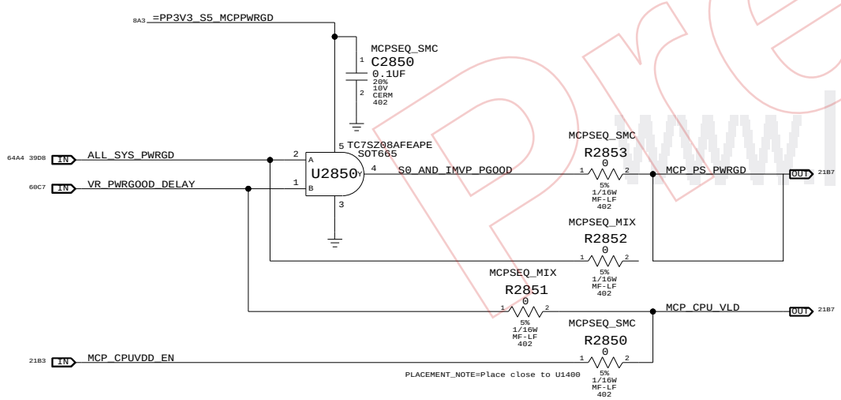
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

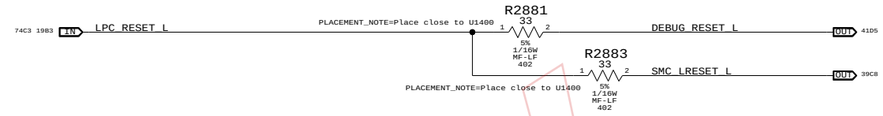
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

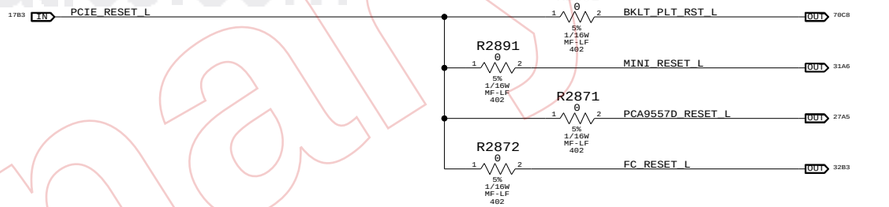
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

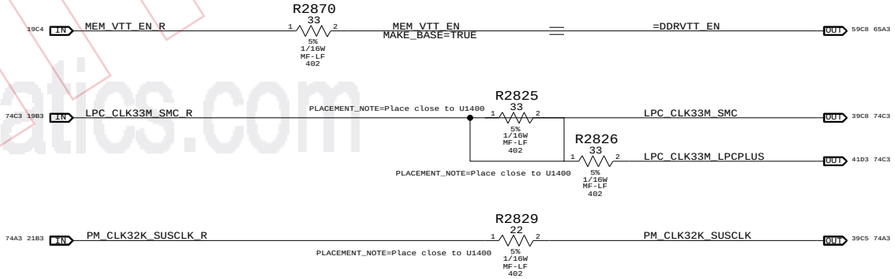
Platform Reset Connections

LPC Reset (Unbuffered)

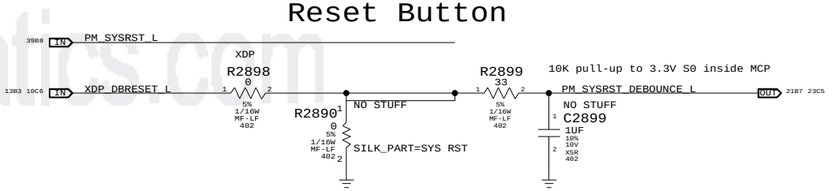


PCIE Reset (Unbuffered)





Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SB Misc

SYNC_MASTER=RAYMOND SYNC_DATE=04/05/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 28 OF 109	

Page Notes

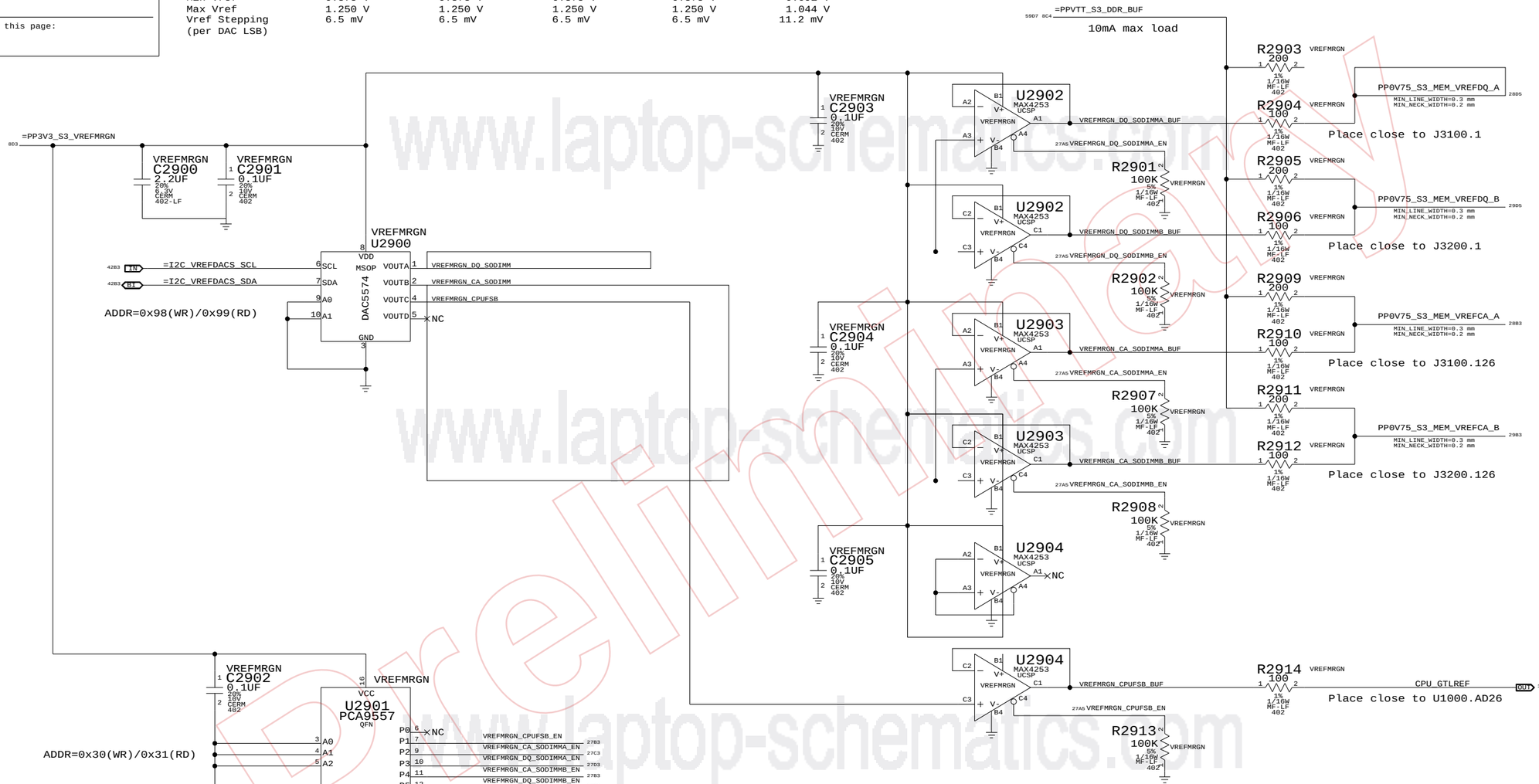
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 29 OF 109	

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

8D3 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 6.3V X5S-CERM 0204-1
C3111 0.1UF 20% 6.3V X5S-CERM 0204-1
C3112 0.1UF 20% 6.3V X5S-CERM 0204-1
C3113 0.1UF 20% 6.3V X5S-CERM 0204-1
C3114 0.1UF 20% 6.3V X5S-CERM 0204-1
C3115 0.1UF 20% 6.3V X5S-CERM 0204-1
C3116 0.1UF 20% 6.3V X5S-CERM 0204-1
C3117 0.1UF 20% 6.3V X5S-CERM 0204-1

27D1 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)
KEY

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NC
NC
NC

72D3 15A5 IN	MEM_A_CKE<0>	MEM_A_CKE<1>	IN 15A5 72D3
72D3 15C5 IN	MEM_A_BA<2>	MEM_A_A<15>	IN 9D2
72D3 15C5 IN	MEM_A_A<12>	MEM_A_A<14>	IN 15C5 72D3
72D3 15B5 IN	MEM_A_A<9>	MEM_A_A<11>	IN 15C5 72D3
72D3 15B5 IN	MEM_A_A<8>	MEM_A_A<7>	IN 15B5 72D3
72D3 15B5 IN	MEM_A_A<5>	MEM_A_A<6>	IN 15B5 72D3
72D3 15B5 IN	MEM_A_A<3>	MEM_A_A<4>	IN 15B5 72D3
72D3 15B5 IN	MEM_A_A<1>	MEM_A_A<2>	IN 15B5 72D3
72D3 15B5 IN	MEM_A_CLK_P<0>	MEM_A_A<0>	IN 15B5 72D3
72D3 15B5 IN	MEM_A_CLK_N<0>	MEM_A_CLK_P<1>	IN 15B5 72D3
72D3 15C5 IN	MEM_A_A<10>	MEM_A_CLK_N<1>	IN 15B5 72D3
72D3 15C5 IN	MEM_A_BA<0>	MEM_A_BA<1>	IN 15C5 72D3
72D3 15C5 IN	MEM_A_WE_L	MEM_A_RAS_L	IN 15C5 72D3
72D3 15C5 IN	MEM_A_CAS_L	MEM_A_CS_L<0>	IN 15B5 72D3
72D3 15C5 IN	MEM_A_A<13>	MEM_A_ODT<0>	IN 15A5 72D3
72D3 15B5 IN	MEM_A_CS_L<1>	MEM_A_ODT<1>	IN 15A5 72D3
72D3 15C7 BI	MEM_A_DQ<32>	MEM_A_DQ<37>	BI 15C7 72D3
72D3 15C7 BI	MEM_A_DQ<33>	MEM_A_DQ<36>	BI 15C7 72D3
72C3 15D5 BI	MEM_A_DQS_N<4>	MEM_A_DM<4>	IN 15A7 72C3
72C3 15D5 BI	MEM_A_DQS_P<4>	MEM_A_DQ<35>	BI 15C7 72D3
72D3 15C7 BI	MEM_A_DQ<34>	MEM_A_DQ<39>	BI 15C7 72D3
72D3 15C7 BI	MEM_A_DQ<38>	MEM_A_DQ<40>	BI 15C7 72D3
72D3 15C7 BI	MEM_A_DQ<44>	MEM_A_DQ<41>	BI 15C7 72D3
72D3 15C7 BI	MEM_A_DQ<45>	MEM_A_DQS_N<5>	BI 15D5 72C3
72C3 15B7 IN	MEM_A_DM<5>	MEM_A_DQS_P<5>	BI 15D5 72C3
72D3 15C7 BI	MEM_A_DQ<47>	MEM_A_DQ<43>	BI 15C7 72D3
72D3 15C7 BI	MEM_A_DQ<46>	MEM_A_DQ<42>	BI 15C7 72D3
72D3 15D7 BI	MEM_A_DQ<49>	MEM_A_DQ<53>	BI 15D7 72D3
72D3 15D7 BI	MEM_A_DQ<52>	MEM_A_DQ<48>	BI 15D7 72D3
72C3 15D5 BI	MEM_A_DQS_N<6>	MEM_A_DM<6>	IN 15B7 72C3
72C3 15D5 BI	MEM_A_DQS_P<6>	MEM_A_DQ<55>	BI 15D7 72D3
72D3 15D7 BI	MEM_A_DQ<54>	MEM_A_DQ<50>	BI 15D7 72D3
72D3 15D7 BI	MEM_A_DQ<51>	MEM_A_DQ<57>	BI 15D7 72D3
72D3 15D7 BI	MEM_A_DQ<61>	MEM_A_DQ<56>	BI 15D7 72D3
72D3 15D7 BI	MEM_A_DQ<60>	MEM_A_DQS_N<7>	BI 15D5 72C3
72C3 15B7 IN	MEM_A_DM<7>	MEM_A_DQS_P<7>	BI 15D5 72C3
72D3 15D7 BI	MEM_A_DQ<58>	MEM_A_DQ<62>	BI 15D7 72D3
72D3 15D7 BI	MEM_A_DQ<59>	MEM_A_DQ<63>	BI 15D7 72D3
	MEM_A_SA<0>	MEM_EVENT_L	OUT 21A4 21B3 29A5 39B8
	MEM_A_SA<1>	=I2C_SODIMMA_SDA	BI 42D6
		=I2C_SODIMMA_SCL	IN 42D6
		=PP0V75_S0_MEM_VTT_A	8C7

8B5 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)
CRITICAL
KEY

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

72D3 15B7 BI	MEM_A_DQ<0>	MEM_A_DQ<4>	BI 15B7 72D3
72D3 15B7 BI	MEM_A_DQ<1>	MEM_A_DQ<5>	BI 15B7 72D3
72C3 15A7 IN	MEM_A_DM<0>	MEM_A_DQS_N<0>	BI 15D5 72C3
72D3 15B7 BI	MEM_A_DQ<6>	MEM_A_DQS_P<0>	BI 15D5 72C3
72D3 15B7 BI	MEM_A_DQ<7>	MEM_A_DQ<3>	BI 15B7 72D3
72D3 15B7 BI	MEM_A_DQ<8>	MEM_A_DQ<2>	BI 15B7 72D3
72D3 15B7 BI	MEM_A_DQ<12>	MEM_A_DQ<9>	BI 15B7 72D3
72C3 15D5 BI	MEM_A_DQS_N<1>	MEM_A_DQ<13>	BI 15B7 72D3
72C3 15D5 BI	MEM_A_DQS_P<1>	MEM_A_DM<1>	IN 15A7 72C3
72D3 15B7 BI	MEM_A_DQ<10>	MEM_RESET_L	IN 29C2 30C3
72D3 15B7 BI	MEM_A_DQ<15>	MEM_A_DQ<11>	BI 15B7 72D3
72D3 15C7 BI	MEM_A_DQ<25>	MEM_A_DQ<14>	BI 15B7 72D3
72D3 15C7 BI	MEM_A_DQ<24>	MEM_A_DQ<29>	BI 15C7 72D3
72C3 15D5 BI	MEM_A_DQS_N<3>	MEM_A_DQ<28>	BI 15C7 72D3
72C3 15D5 BI	MEM_A_DQS_P<3>	MEM_A_DM<3>	IN 15A7 72C3
72D3 15C7 BI	MEM_A_DQ<26>	MEM_A_DQ<27>	BI 15C7 72D3
72D3 15C7 BI	MEM_A_DQ<30>	MEM_A_DQ<31>	BI 15C7 72D3
72D3 15B7 BI	MEM_A_DQ<20>	MEM_A_DQ<18>	BI 15B7 72D3
72D3 15B7 BI	MEM_A_DQ<21>	MEM_A_DQ<17>	BI 15B7 72D3
72C3 15A7 IN	MEM_A_DM<2>	MEM_A_DQS_N<2>	BI 15D5 72C3
72D3 15C7 BI	MEM_A_DQ<23>	MEM_A_DQS_P<2>	BI 15D5 72C3
72D3 15B7 BI	MEM_A_DQ<16>	MEM_A_DQ<19>	BI 15B7 72D3
		MEM_A_DQ<22>	BI 15C7 72D3

516-0201

PP0V75_S3_MEM_VREFCA_A 27C1

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN SYNC_DATE=06/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	31	109

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

8D3 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 6.3V X6S-CERM 0204-1
C3211 0.1UF 20% 6.3V X6S-CERM 0204-1
C3212 0.1UF 20% 6.3V X6S-CERM 0204-1
C3213 0.1UF 20% 6.3V X6S-CERM 0204-1
C3214 0.1UF 20% 6.3V X6S-CERM 0204-1
C3215 0.1UF 20% 6.3V X6S-CERM 0204-1
C3216 0.1UF 20% 6.3V X6S-CERM 0204-1
C3217 0.1UF 20% 6.3V X6S-CERM 0204-1

27C1 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

72B3 15A1 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15A1 72B3
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 9D2
72B3 15C1 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15C1 72B3
		81	VDD	VDD	82		
72B3 15C1 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15C1 72B3
72B3 15B1 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15B1 72B3
		87	VDD	VDD	88		
72B3 15B1 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15B1 72B3
72B3 15B1 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15B1 72B3
		93	VDD	VDD	94		
72B3 15B1 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15B1 72B3
72B3 15B1 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15B1 72B3
		99	VDD	VDD	100		
72B3 15B1 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15B1 72B3
72B3 15B1 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15B1 72B3
		105	VDD	VDD	106		
72B3 15C1 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15C1 72B3
72B3 15C1 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15C1 72B3
		111	VDD	VDD	112		
72B3 15C1 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15B1 72B3
72B3 15C1 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15A1 72B3
		117	VDD	VDD	118		
72B3 15C1 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15A1 72B3
72B3 15B1 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
72B3 15C3 BI	MEM_B_DQ<37>	129	DQ32	DQ36	130	MEM_B_DQ<36>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<32>	131	DQ33	DQ37	132	MEM_B_DQ<33>	BI 15C3 72B3
		133	VSS	VSS	134		
72A3 15D1 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 15A3 72B3
72A3 15D1 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<35>	141	DQ34	DQ39	142	MEM_B_DQ<34>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<39>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<40>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<45>	147	DQ40	DQ45	148	MEM_B_DQ<44>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 15D1 72A3
72B3 15B3 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 15D1 72A3
		155	VSS	VSS	156		
72B3 15C3 BI	MEM_B_DQ<46>	157	DQ42	DQ46	158	MEM_B_DQ<42>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<47>	159	DQ43	DQ47	160	MEM_B_DQ<43>	BI 15C3 72B3
		161	VSS	VSS	162		
72B3 15D3 BI	MEM_B_DQ<53>	163	DQ48	DQ52	164	MEM_B_DQ<52>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<48>	BI 15D3 72B3
		167	VSS	VSS	168		
72A3 15D1 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15B3 72A3
72A3 15D1 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<51>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<55>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<54>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<63>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<59>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<58>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 15D1 72A3
72A3 15B3 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 15D1 72A3
		189	VSS	VSS	190		
72B3 15D3 BI	MEM_B_DQ<61>	191	DQ58	DQ62	192	MEM_B_DQ<62>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<60>	193	DQ59	DQ63	194	MEM_B_DQ<57>	BI 15D3 72B3
		195	VSS	VSS	196		
MEM_B_SA<0>		197	SA0	EVENT*	198	MEM_EVENT_L	OUT 21A4 21B3 28A5 39B8
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 42D6
MEM_B_SA<1>		201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 42D6
		203	VTT	VTT	204		=PP0V75_S0_MEM_VTT_B 8C7
		MTG PINS					
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

J3200 F-RT-BGA3 DDR3-SODIMM (1 OF 2) CRITICAL

		1	VREFDQ	VSS	2		
72B3 15B3 BI	MEM_B_DQ<1>	3	VSS	DQ4	4	MEM_B_DQ<4>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<0>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 15B3 72B3
		7	DQ1	VSS	8		
72B3 15A3 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 15D1 72A3
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 15D1 72A3
		13	VSS	VSS	14		
72B3 15B3 BI	MEM_B_DQ<3>	15	DQ2	DQ6	16	MEM_B_DQ<7>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<6>	17	DQ3	DQ7	18	MEM_B_DQ<2>	BI 15B3 72B3
		19	VSS	VSS	20		
72B3 15B3 BI	MEM_B_DQ<13>	21	DQ8	DQ12	22	MEM_B_DQ<12>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<14>	23	DQ9	DQ13	24	MEM_B_DQ<9>	BI 15B3 72B3
		25	VSS	VSS	26		
72A3 15D1 BI	MEM_B_DQS_N<1>	27	DQS1*	DM1	28	MEM_B_DM<1>	IN 15A3 72B3
72A3 15D1 BI	MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28C2 30C3
		31	VSS	VSS	32		
72B3 15B3 BI	MEM_B_DQ<15>	33	DQ10	DQ14	34	MEM_B_DQ<8>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<10>	35	DQ11	DQ15	36	MEM_B_DQ<11>	BI 15B3 72B3
		37	VSS	VSS	38		
72B3 15B3 BI	MEM_B_DQ<20>	39	DQ16	DQ20	40	MEM_B_DQ<16>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<17>	41	DQ17	DQ21	42	MEM_B_DQ<21>	BI 15B3 72B3
		43	VSS	VSS	44		
72A3 15D1 BI	MEM_B_DQS_N<2>	45	DQS2*	DM2	46	MEM_B_DM<2>	IN 15A3 72B3
72A3 15D1 BI	MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<18>	BI 15B3 72B3
72B3 15C3 BI	MEM_B_DQ<22>	51	DQ18	DQ23	52	MEM_B_DQ<23>	BI 15C3 72B3
72B3 15B3 BI	MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<29>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<24>	57	DQ24	DQ29	58	MEM_B_DQ<25>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<28>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<3>	BI 15D1 72A3
72B3 15A3 IN	MEM_B_DM<3>	63	DM3	DQS3	64	MEM_B_DQS_P<3>	BI 15D1 72A3
		65	VSS	VSS	66		
72B3 15C3 BI	MEM_B_DQ<26>	67	DQ26	DQ30	68	MEM_B_DQ<30>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<31>	69	DQ27	DQ31	70	MEM_B_DQ<27>	BI 15C3 72B3
		71	VSS	VSS	72		

KEY

516S0706

PP0V75_S3_MEM_VREFCA_B 27C1

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402

8B5 =PPSPD_S0_MEM_B

C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

DDR3 GROUND RETURN CAPS (MCP SIDE)

8B7 =PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 6.3V X6S-CERM 0204-1
C3223 0.1UF 20% 6.3V X6S-CERM 0204-1
C3224 0.1UF 20% 6.3V X6S-CERM 0204-1
C3225 0.1UF 20% 6.3V X6S-CERM 0204-1
C3226 0.1UF 20% 6.3V X6S-CERM 0204-1
C3227 0.1UF 20% 6.3V X6S-CERM 0204-1
C3228 0.1UF 20% 6.3V X6S-CERM 0204-1
C3229 0.1UF 20% 6.3V X6S-CERM 0204-1

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

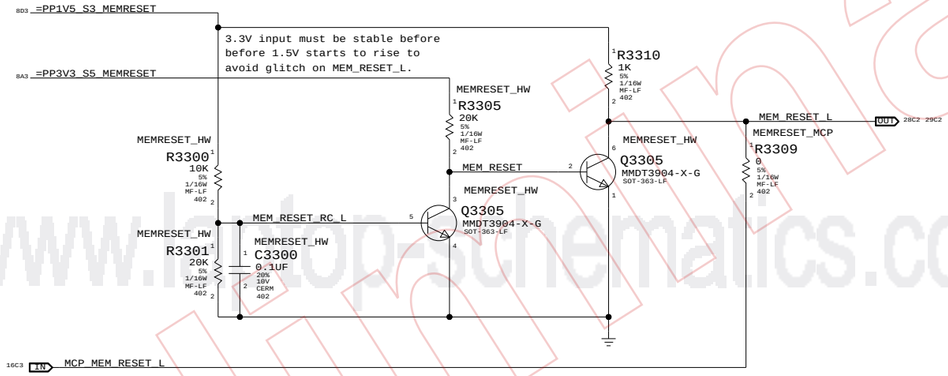
SYNC_MASTER=BEN SYNC_DATE=05/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 32 OF 109	

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 33 OF 109	

PCIE_MINI_PRSNT_L
Q3401
SSM6N15FEAPE
SOT563
AP_PWR_EN
MINI_CLKREQ_L
Q3401
SSM6N15FEAPE
SOT563

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_Q_L
PCIE_WAKE_L
NC
NC
PP5V_S3_BTCAMERA_F
I2C_ALS_SDA
I2C_ALS_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
CONN_USB2_BT_P
CONN_USB2_BT_N

PLACEMENT_NOTE=Place close to J3401.
C3431 0.1uF 10% 16V X5R 402
PCIE_MINI_R2D_C_P
C3430 0.1uF 10% 16V X5R 402
PCIE_MINI_R2D_C_N
1000 mA peak
750 mA nominal max
PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

AIRPORT

CRITICAL
L3401
90-OHM-100MA
DLP11S
PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N
PLACEMENT_NOTE=Place close to J3401.

ALS
CAMERA
CRITICAL
L3402
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3401.

BLUETOOTH
CRITICAL
L3403
90-OHM
DLP0NS
USB_BT_P
USB_BT_N
PLACEMENT_NOTE=Place close to J3401.

5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

L3404
FERR-120-OHM-1.5A
0402-LF
C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 20% 10V CERM 402
C3420 10UF 20% 10V X5R 805
PP5V_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
PLACEMENT_NOTE=Place close to J3401.
PLACEMENT_NOTE=Place close to Q3450.
PLACEMENT_NOTE=Place close to Q3450.
Q3450
FDC606P_G
SOT-6
C3450 0.1UF 10% 16V X5R 402
P5VWLAN_SS
C3451 0.033UF 10% 16V X5R 402
R3451 10K 5% 1/16W MF-LF 402
R3450 100K 5% 1/16W MF-LF 402
=PP5V_S3_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
PM_WLAN_EN_L

L3405
FERR-120-OHM-1.5A
0402-LF
275 mA peak
200 mA nominal max
C3452 0.1uF 20% 10V CERM 402
=PP5V_S3_BTCAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

=PP3V3_S3_WLAN
PP5V_WLAN_F
R3453 33K 5% 1/16W MF-LF 402
U3402
74LVC1G17DRL
SOT-553
TC7SZ08AFEAPE
SOT665
U3401
MINI_RESET_CONN_L
WLAN_SMIT_BUF
WLAN_SMIT_RC
NC
C3453 1UF 10% 6.3V CERM 402
R3454 62K 5% 1/16W MF-LF 402
MINI_RESET_L

Right Clutch Connector
SYNC_MASTER=YITE
SYNC_DATE=04/22/2008

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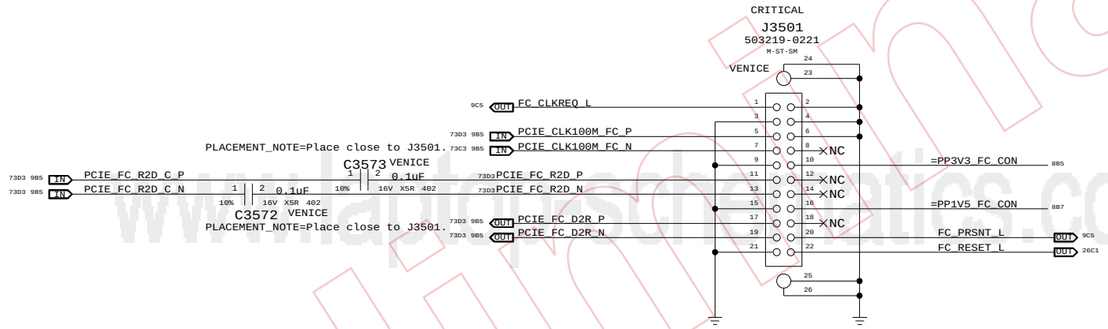
APPLE INC.
SIZE D
DRAWING NUMBER 051-7537
REV. A
SCALE NONE
SHT 34 OF 109



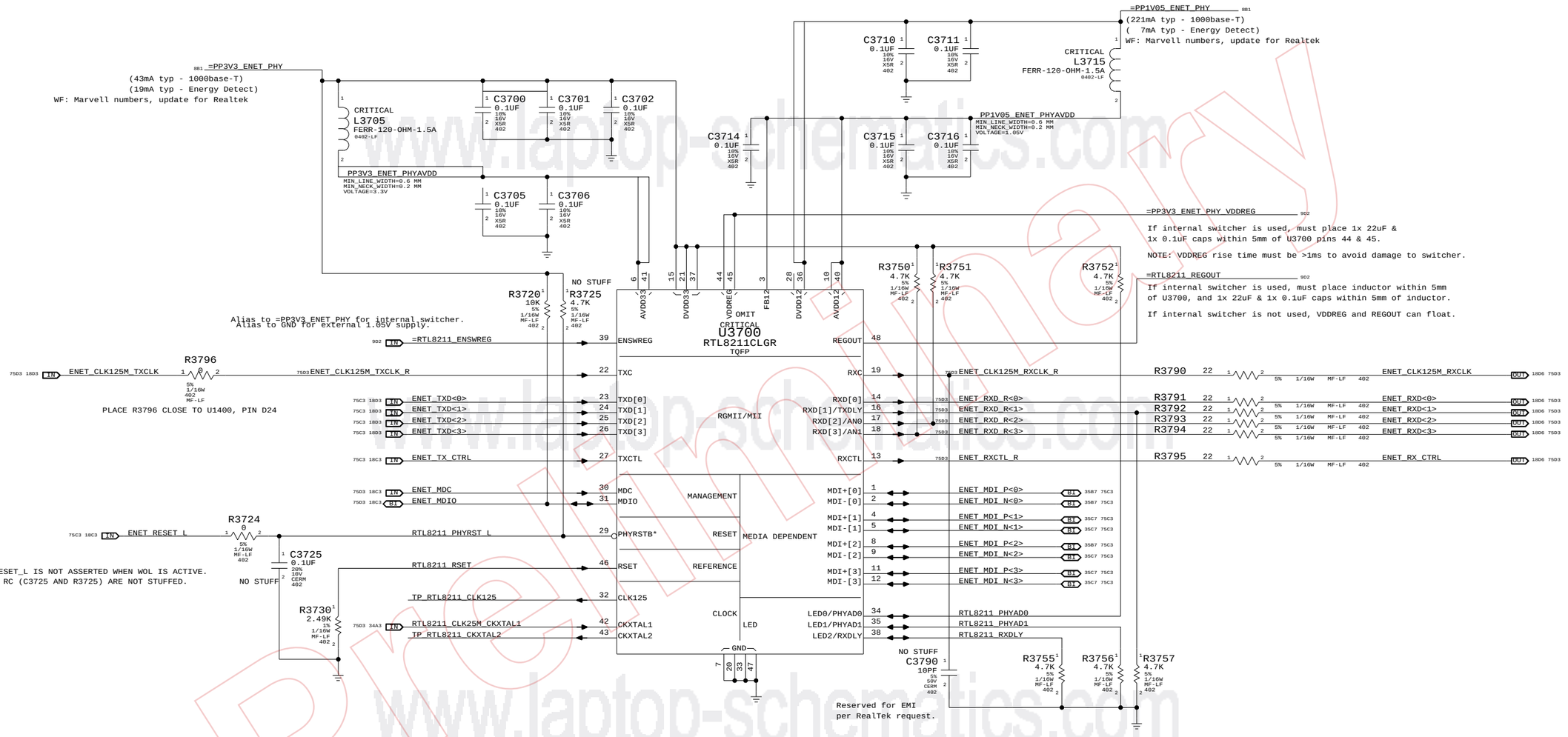
Venice Connector

VENICE CONNECTOR

SYNC_MASTER=YITE SYNC_DATE=03/13/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	35	109



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA SYNC_DATE=05/23/2008

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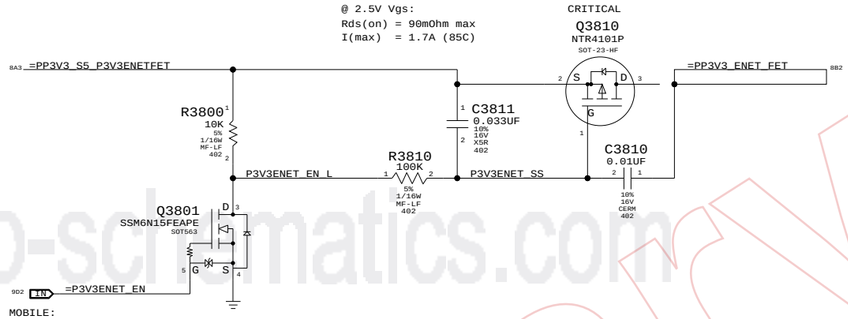
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 37 OF 109	

3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL



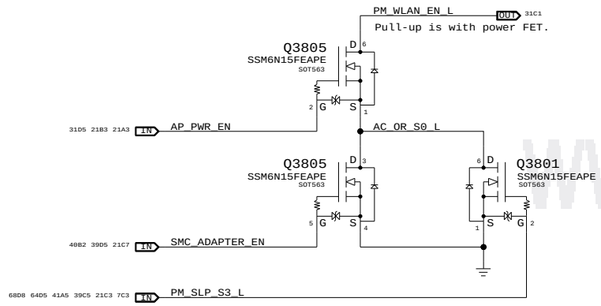
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and
=P3V3ENET_EN. Nets separated on
ARB for alternate power options.

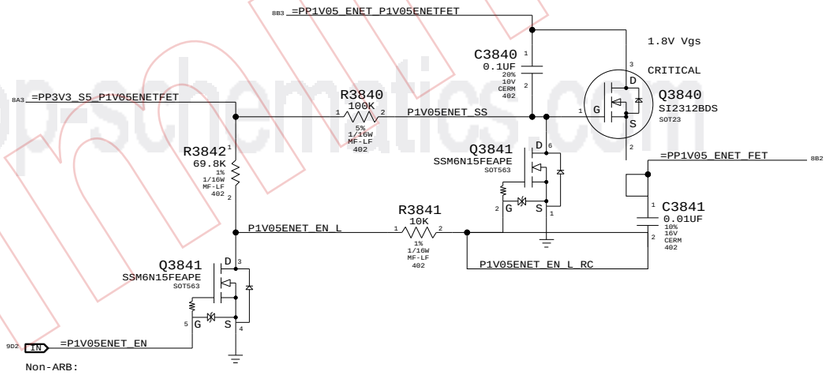
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET



Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and
=P1V05ENET_EN. Nets separated on
ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

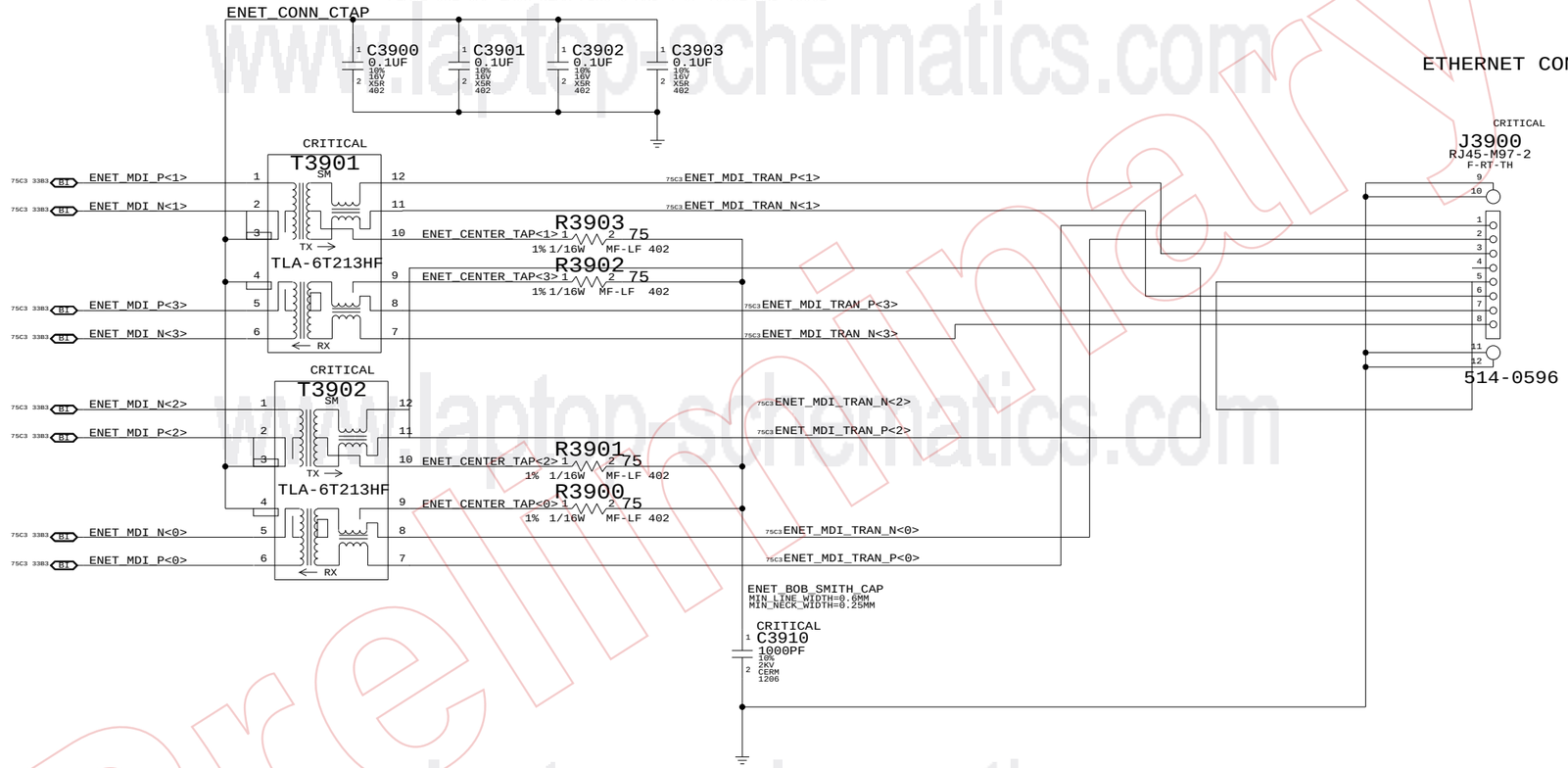
SYNC_MASTER=SUMA SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 38 OF 109	

- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902



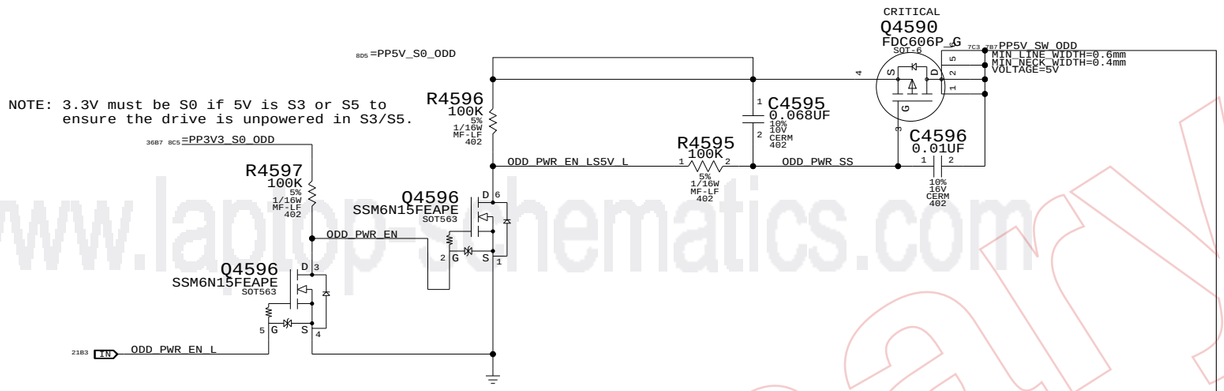
ETHERNET CONNECTOR

SYNC_MASTER=SUMA SYNC_DATE=04/04/2008

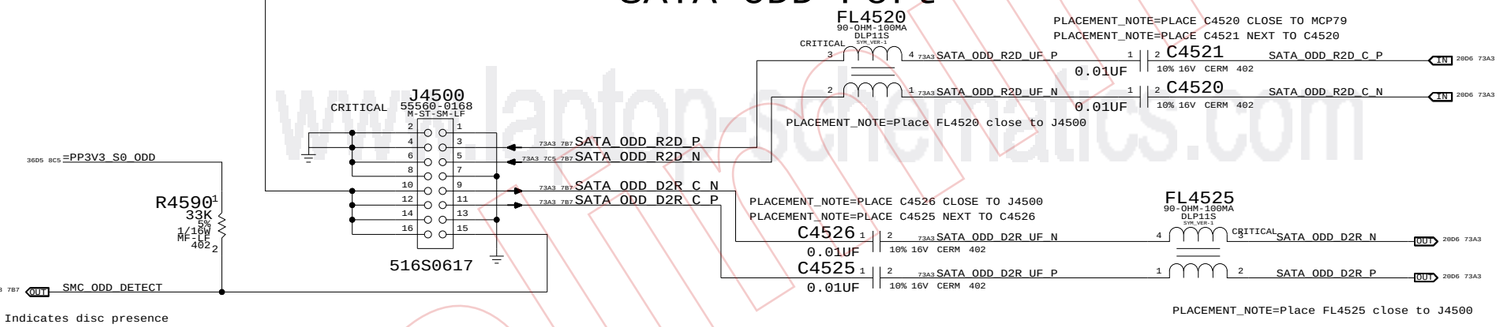
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 39 OF 109	

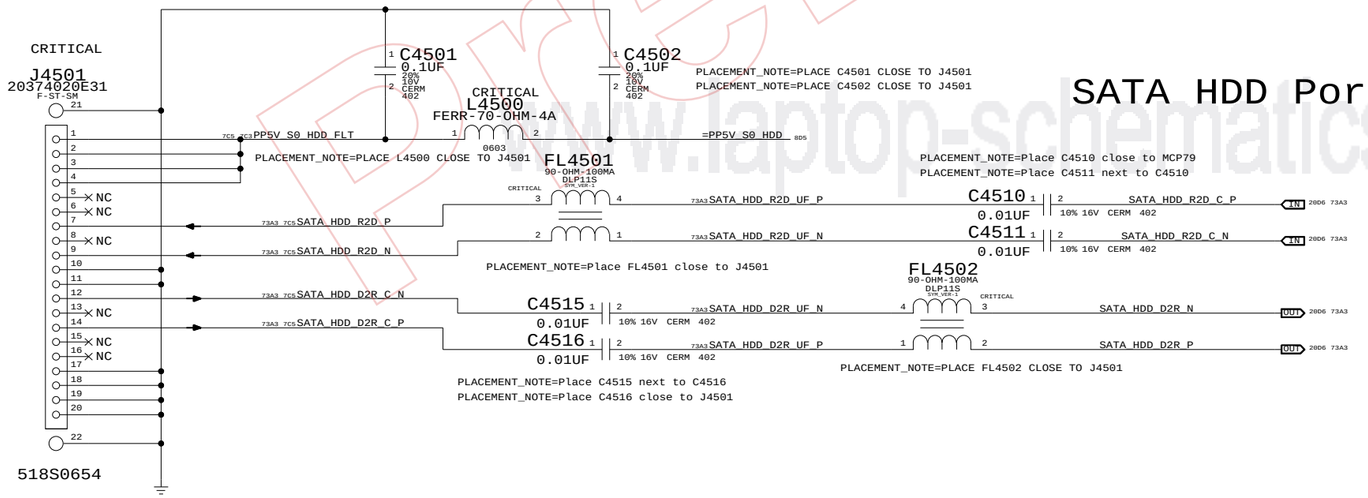
ODD Power Control



SATA ODD Port



SATA HDD Port



SATA Connectors

SYNC_MASTER=CHANGZHANG SYNC_DATE=04/14/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 45 OF 109	

Port Power Switch

We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

CRITICAL
U4690
TPS2064DGN
MSOP

8C3 =PP5V_S3_EXTUSB
20C2 OUT USB_EXTA_OC_L
20C2 OUT USB_EXTB_OC_L
IN OUT1 OUT2 OC1* OC2* EN1 EN2 GND TPAD
PP5V_S3_RTUSB_A_ILIM
PP5V_S3_RTUSB_B_ILIM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

NOSTUFF C4690 10UF 20% 6.3V X5R 603
C4691 0.1UF 20% 10V CERM 402
C4695 10UF 20% 6.3V X5R 603
CRITICAL C4696 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C4617 10UF 20% 6.3V X5R 603
CRITICAL C4616 100UF 20% 6.3V POLY-TANT CASE-B2-SM
USB_PWR_EN_R

CAN NOSTUFF C4696 AND C4616 AFTER CHARACTERIZATION

64C6 IN =USB_PWR_EN
R4690 0 5% 1/16W MF-LF 402
NOSTUFF R4691 0 5% 1/16W MF-LF 402

STUFF R4691 IF USING TPS2060(ACTIVE LOW ENABLE)
STUFF R4690 IF USING TPS2064(ACTIVE HIGH ENABLE)

USB/SMC Debug Mux

8D1 =PP3V42_G3H_SMCUSBMUX
SMC_DEBUG_YES
C4650 0.1UF 20% 10V CERM 402
R4650 10K 5% 1/16W MF-LF 402
VCC
U4650
PI3USB102ZLE
TQFN
CRITICAL
GND

41C3 40B2 39C5 39B8 IN SMC_RX_L
41C5 40B2 39C5 39B8 OUT SMC_TX_L
74C3 20D3 BI USB_EXTA_P
74C3 20D3 BI USB_EXTA_N
M+ M- D+ D- OE* SEL Y+ Y-
USB_DEBUGPRT_EN_L
IN 39B8
SEL=0 Choose SMC
SEL=1 Choose USB

SMC_DEBUG_NO
R4651 0 5% 1/16W MF-LF 402
SMC_DEBUG_NO
R4652 0 5% 1/16W MF-LF 402

USB PORT A (FRONT PORT)

PLACEMENT_NOTE=NEAR J4600
CRITICAL L4605 FERR-220-OHM-2.5A 0603
PP5V_S3_RTUSB_A_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
C4605 0.01uF 20% 16V CERM 402
PLACEMENT_NOTE=NEAR J4600
CRITICAL L4600 90-OHM DLP0NS
74C3 USB_EXTA_MUXED_N
74C3 USB_EXTA_MUXED_P
74C3 CONN_USB_EXTA_N
74C3 CONN_USB_EXTA_P
CRITICAL J4600 USB F-RT-TH-M97-3
514-0606
VBUS GND NC IO NC IO
CRITICAL D4600 RCLAMP0502N SLP1210N6

PLACEMENT_NOTE=NEAR J4610
CRITICAL L4615 FERR-220-OHM-2.5A 0603
We can add protection to 5V if we want, but leaving NC for now
Place L4600 and L4605 at connector pin
PP5V_S3_RTUSB_B_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
C4615 0.01uF 20% 16V CERM 402

PLACEMENT_NOTE=NEAR J4610
CRITICAL L4610 90-OHM DLP0NS
74B3 20C8 BI USB_EXTB_N
74B3 20C9 BI USB_EXTB_P
74B3 CONN_USB_EXTB_N
74B3 CONN_USB_EXTB_P
CRITICAL J4610 USB F-RT-TH-M97-3
514-0606
VBUS GND NC IO NC IO
CRITICAL D4610 RCLAMP0502N SLP1210N6

USB PORT B (BACK PORT)

External USB Connectors		
SYNC_MASTER=YUAN.MA	SYNC_DATE=01/18/2008	
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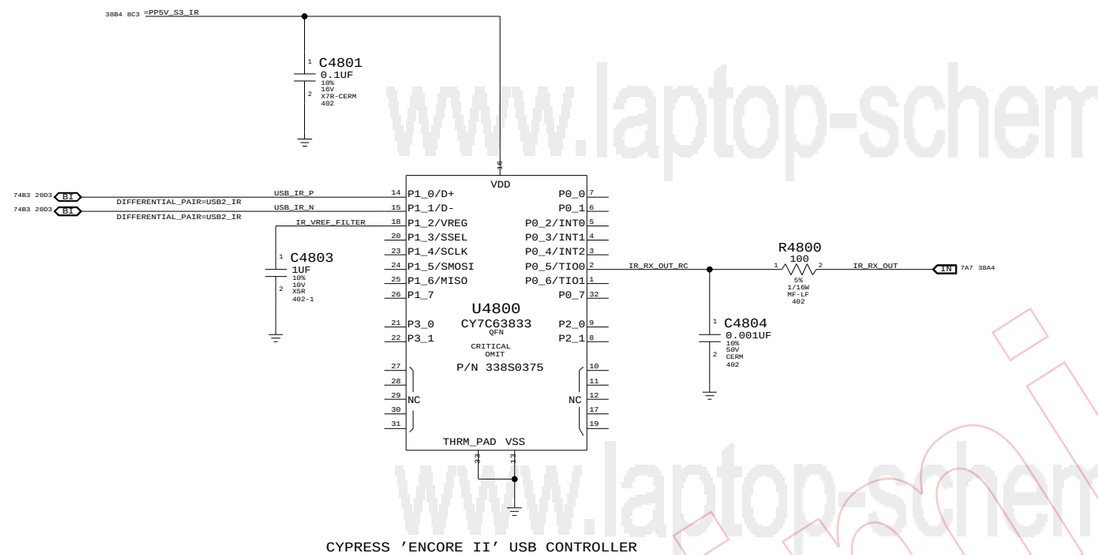
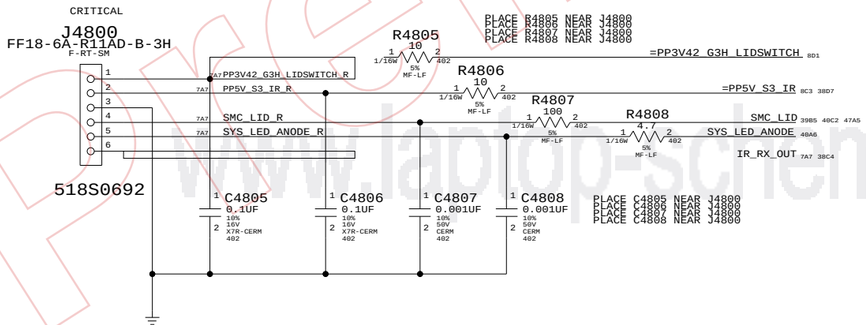
APPLE INC.	SIZE D	DRAWING NUMBER 051-7537 REV. A
	SCALE NONE	SHT 46 OF 109



CYPRESS 'ENCORE II' USB CONTROLLER



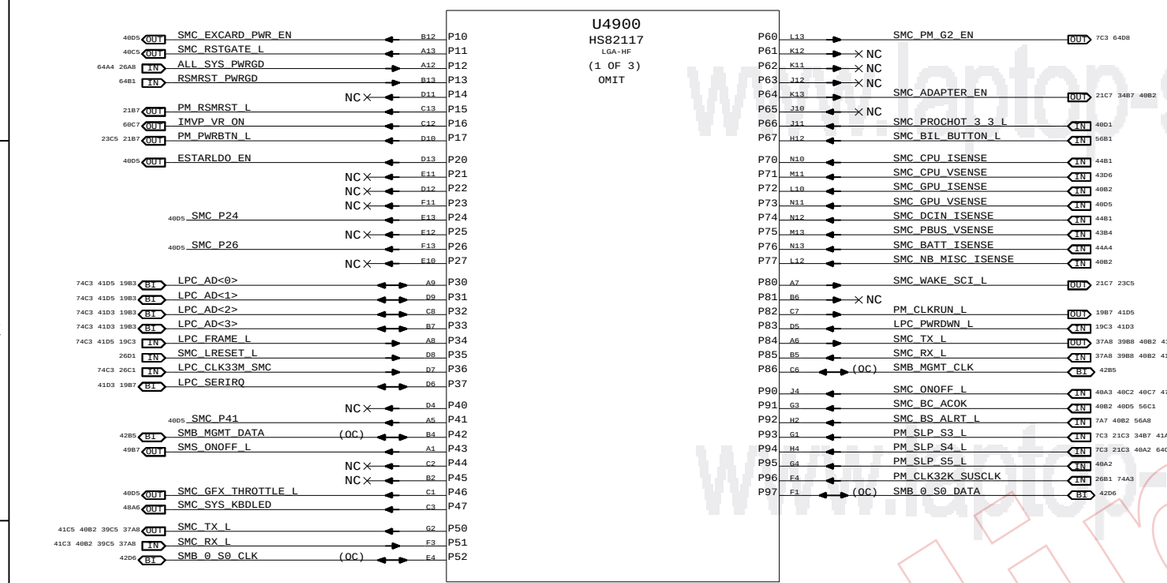
Front Flex Support

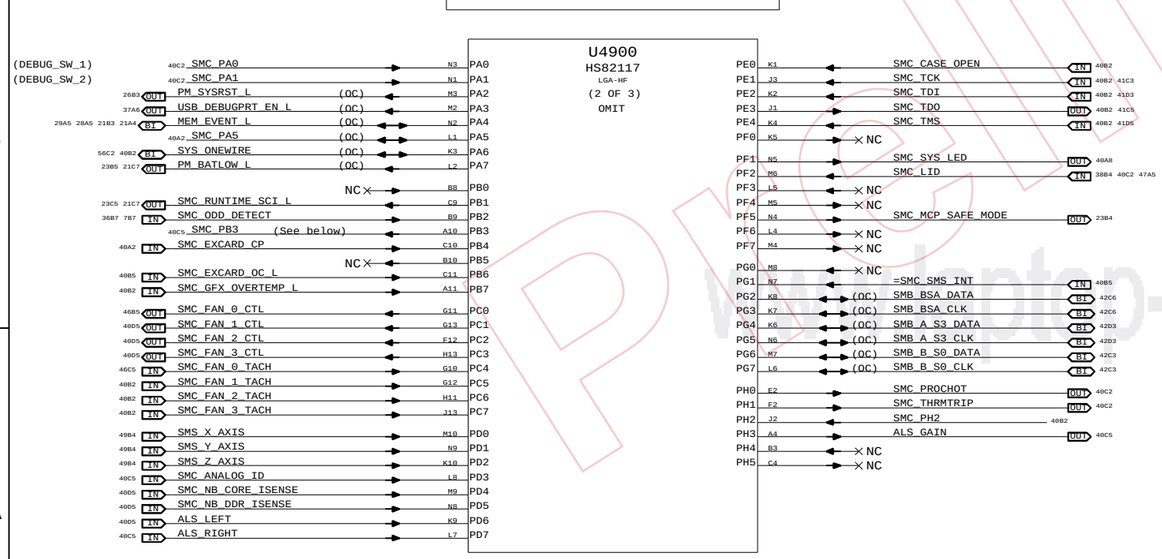
SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 48 OF 109	

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

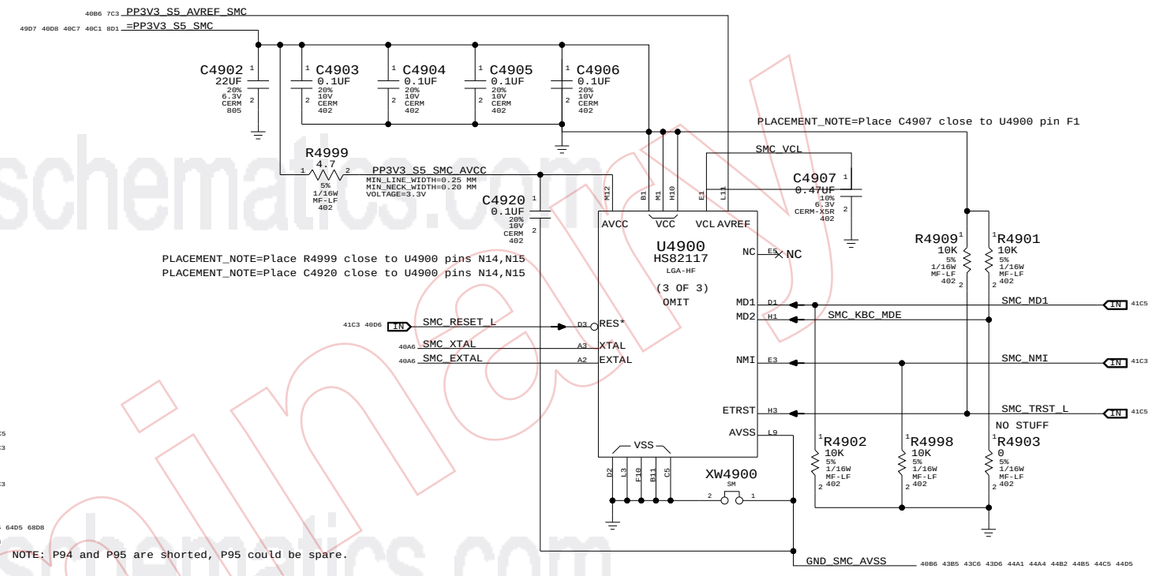




(DEBUG_SW_1)
(DEBUG_SW_2)

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

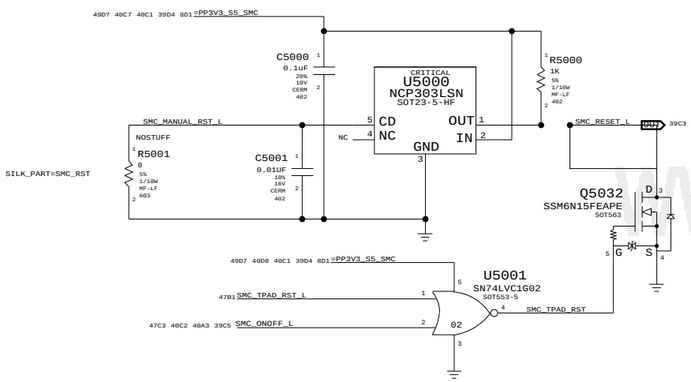
SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

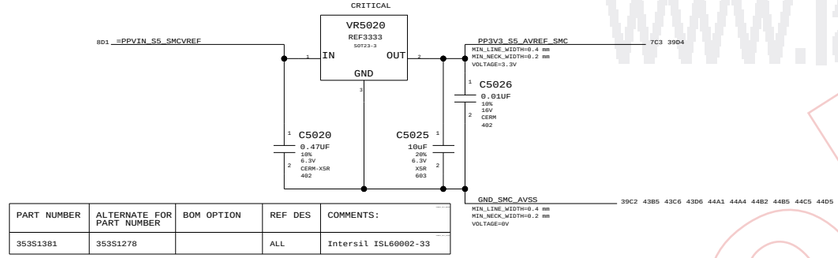
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 49 OF 109	

SMC Reset "Button" / Brownout Detect

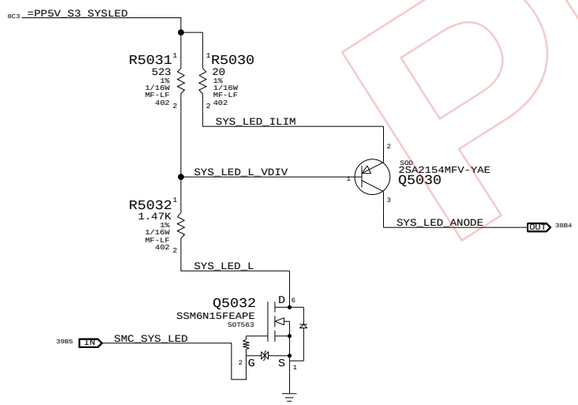


SMC AVREF Supply

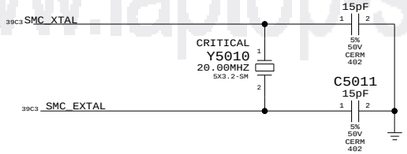


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

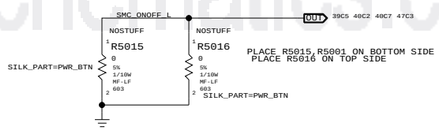
System (Sleep) LED Circuit



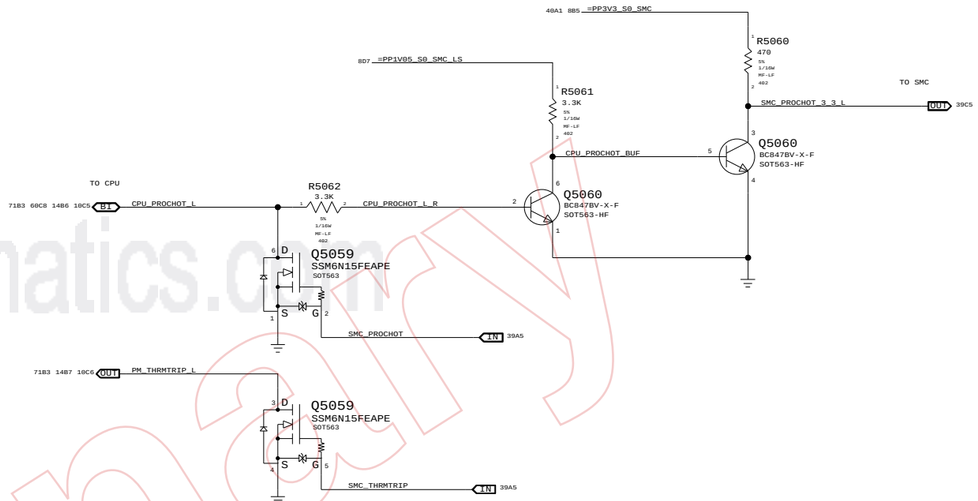
SMC Crystal Circuit

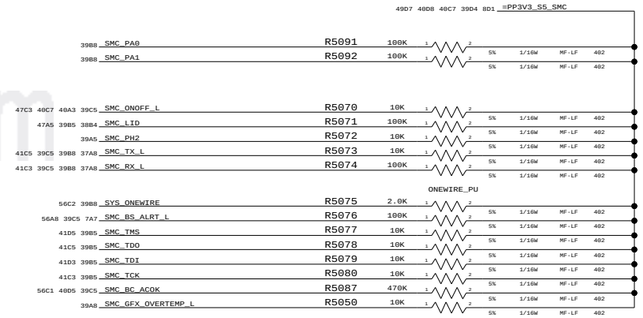


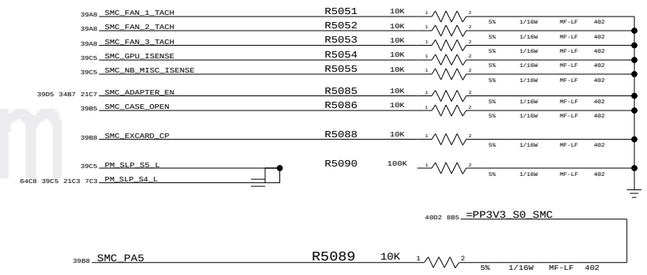
Debug Power "Button"

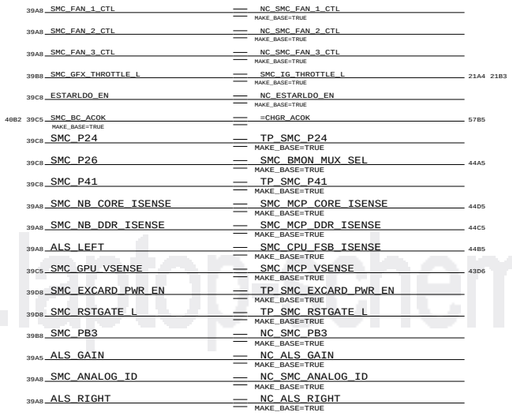


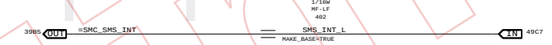
SMC FSB to 3.3V Level Shifting











SMC Support

SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

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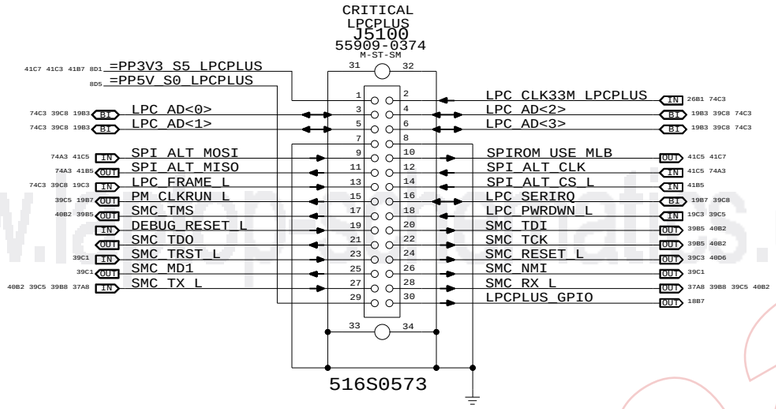
APPLE INC.

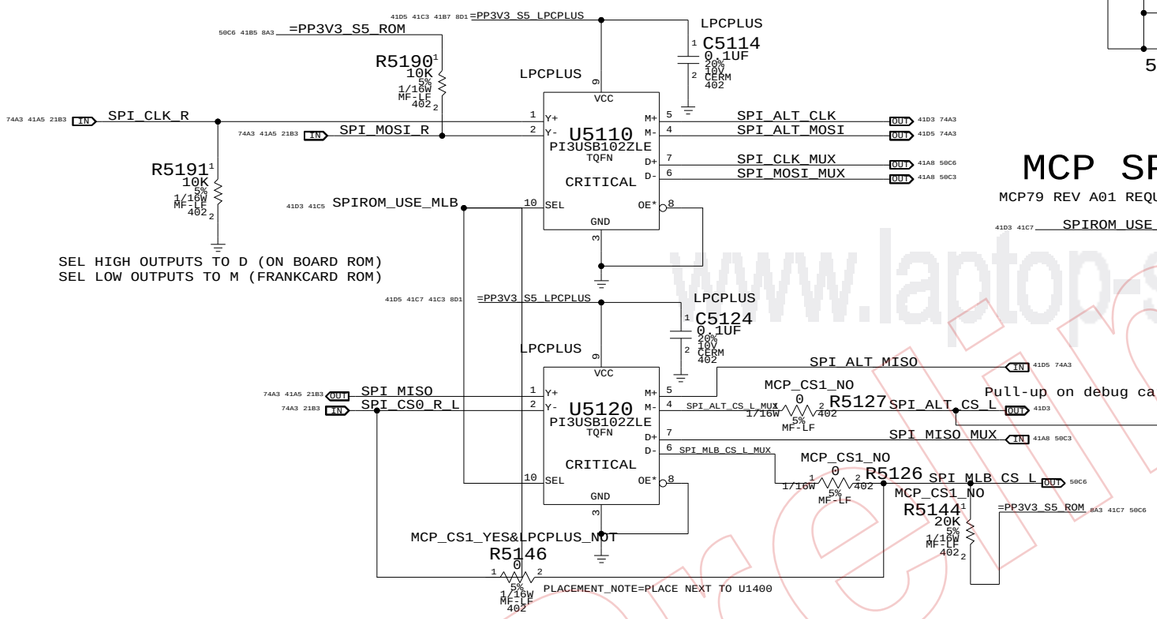
SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 50 OF 109	

LPC+SPI Connector



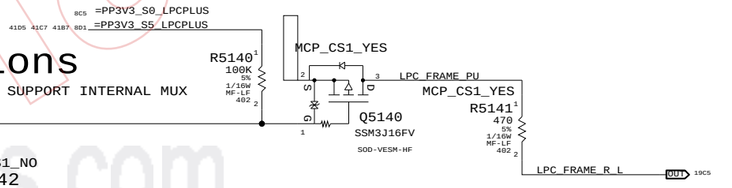
Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP



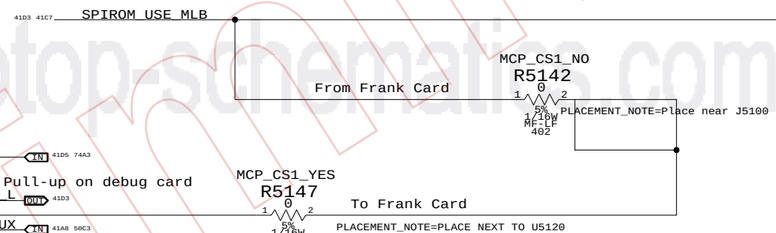
MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON



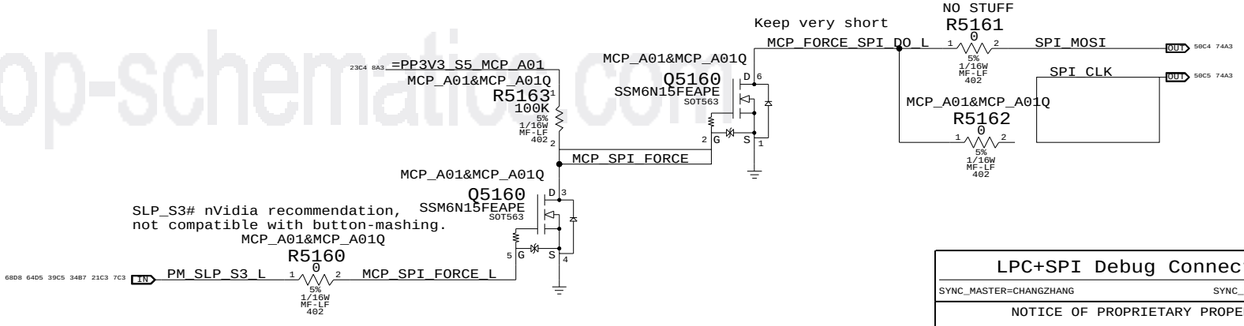
MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

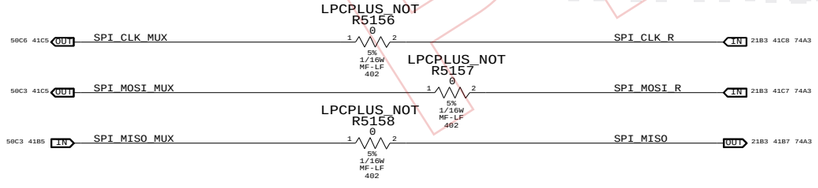


SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED.NOT NEEDED FOR B01 OR LATER.



SPI MUX BYPASS



LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

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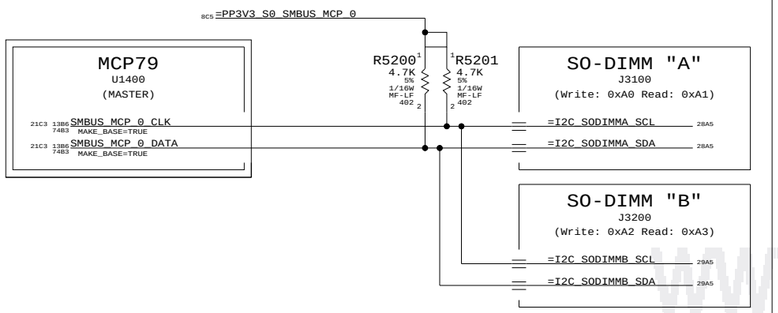
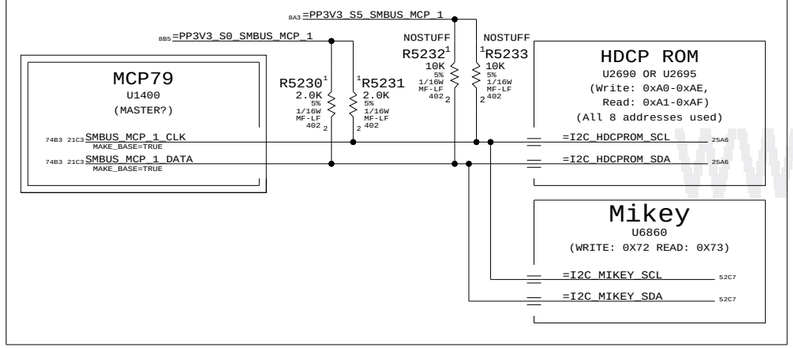
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 51 OF 109	

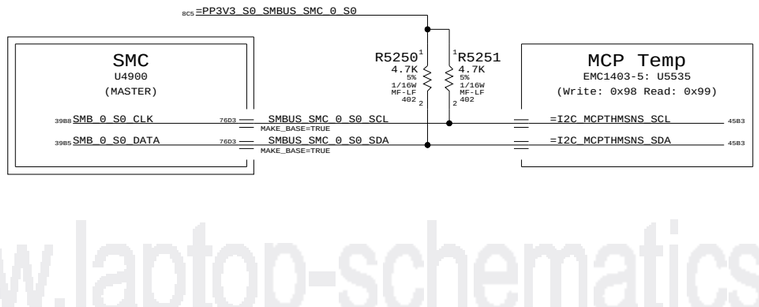
MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS

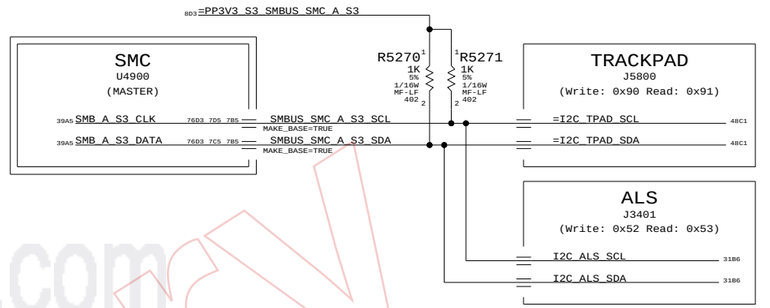


SMC "0" SMBus Connections

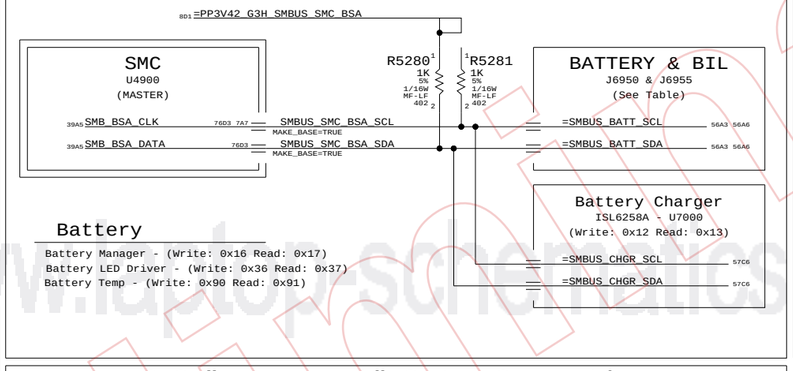


SMC "A" SMBus Connections

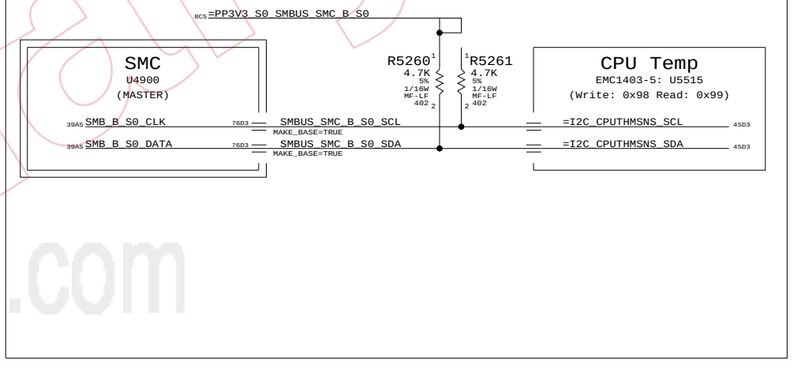
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections

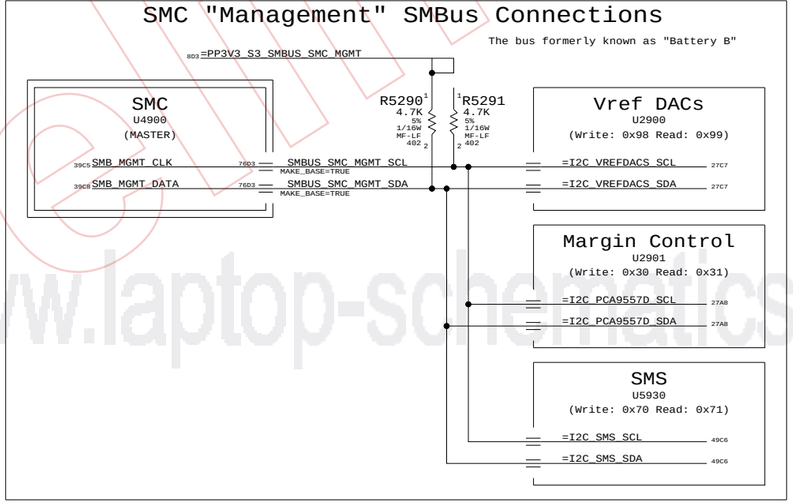


SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



M97 SMBUS CONNECTIONS

SYNC_MASTER=BEN SYNC_DATE=04/21/2008

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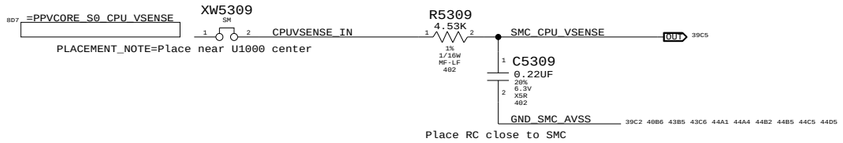
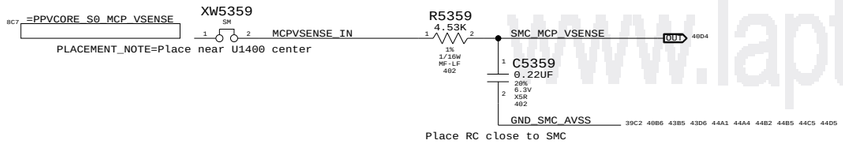
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 52 OF 109	

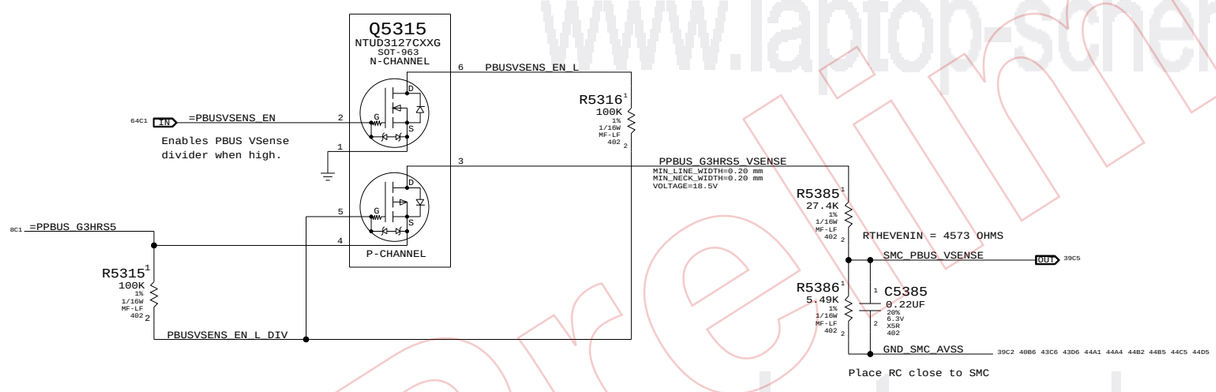
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



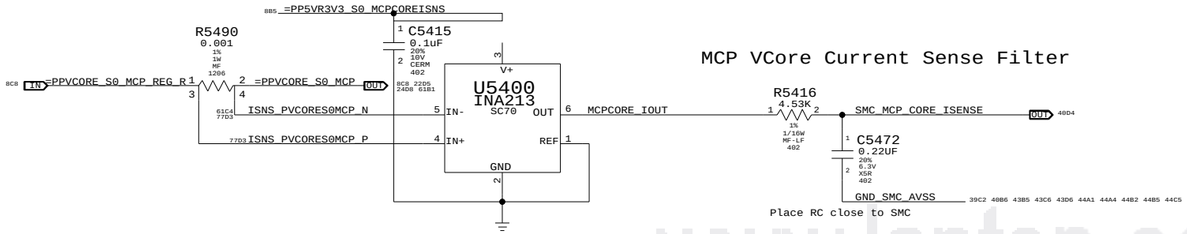
VOLTAGE SENSING

SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 53 OF 109	

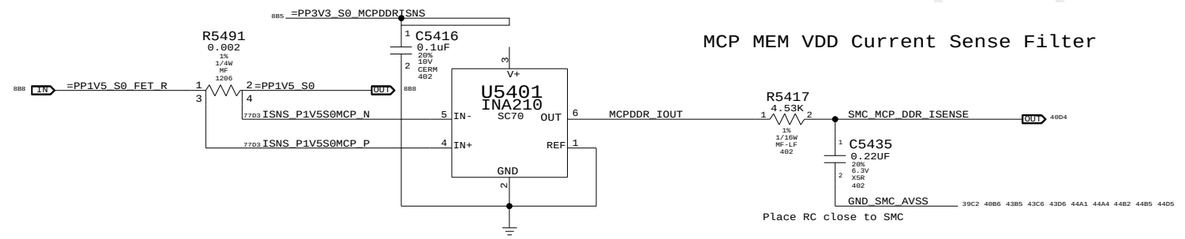
MCP VCore Current Sense



MCP VCore Current Sense Filter

Place RC close to SMC

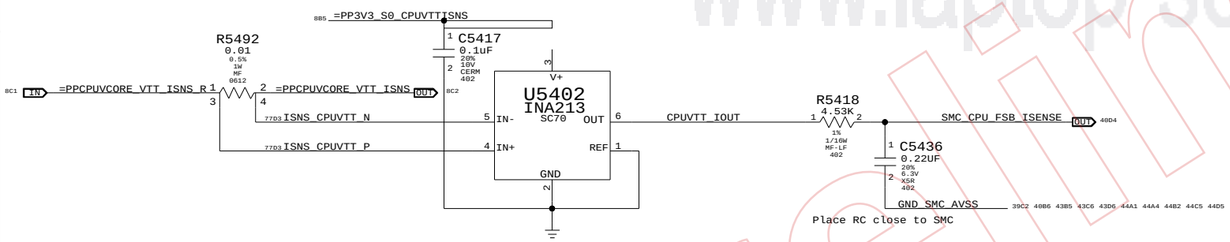
MCP MEM VDD Current Sense



MCP MEM VDD Current Sense Filter

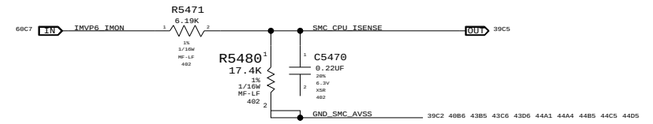
Place RC close to SMC

CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE

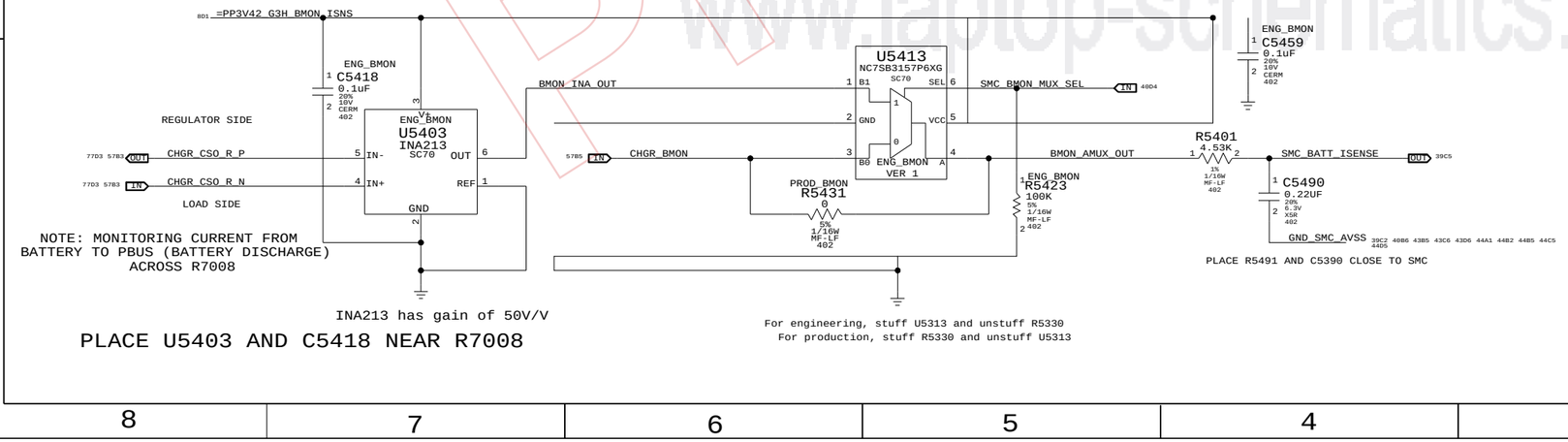


CPU VCore Load Side Current Sense / Filter

Place RC close to SMC

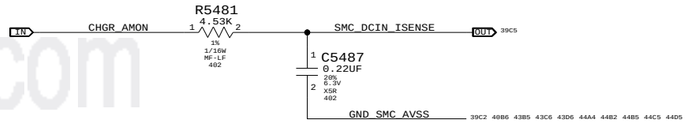


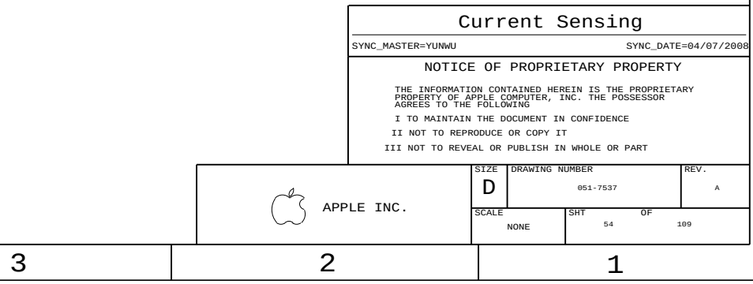
BMON CURRENT SENSE



PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)

DC-IN (AMON) CURRENT SENSE





PLACE R5491 AND C5390 CLOSE TO SMC

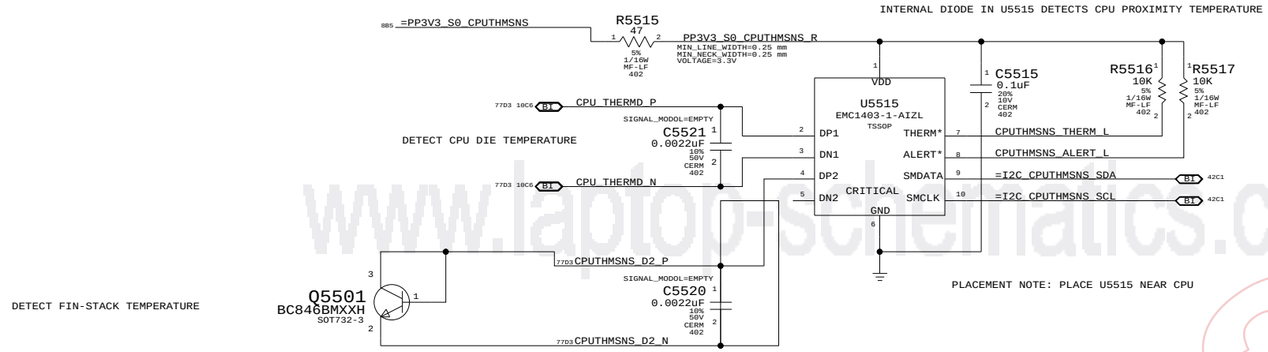
Current Sensing

SYNC_MASTER=YUNWU SYNC_DATE=04/07/2008

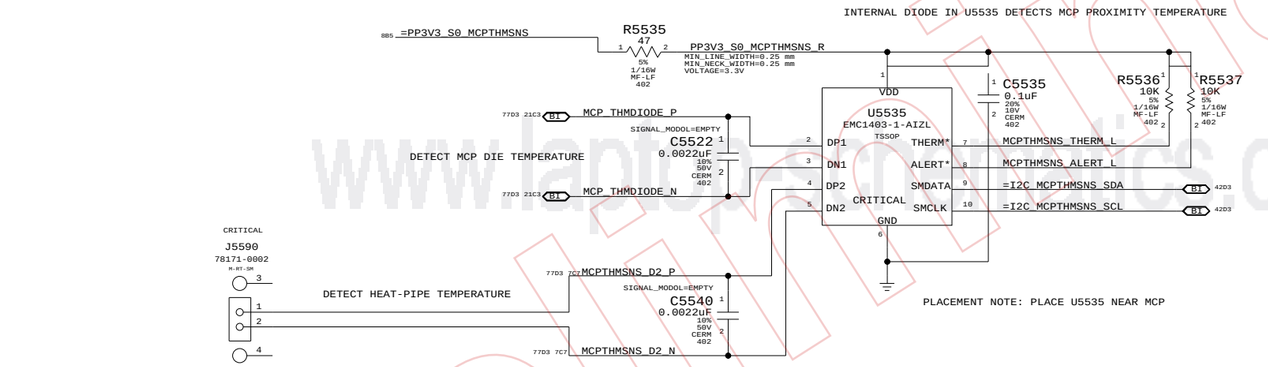
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 54 OF 109	

CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



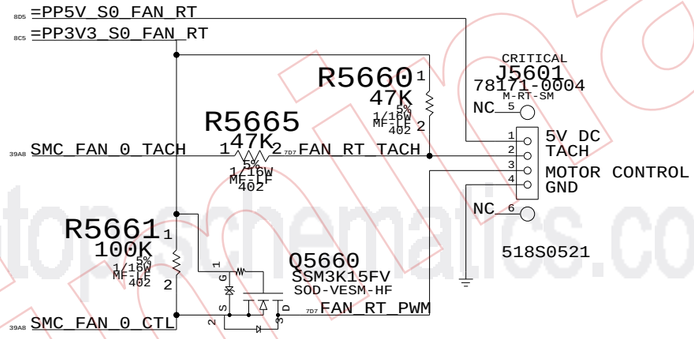
REPLACED 518S0521 WITH 518S0519

Thermal Sensors

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 55 OF 109	



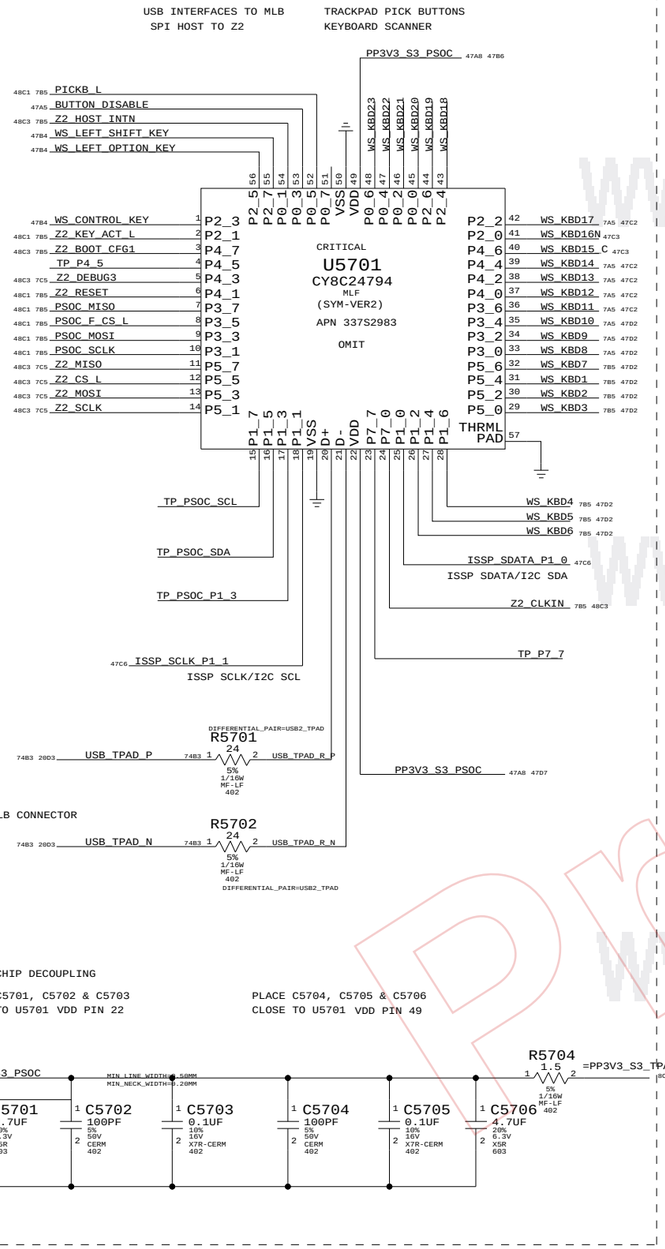
Fan

SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	56	109

PSOC USB CONTROLLER



U5701 CHIP DECOUPLING

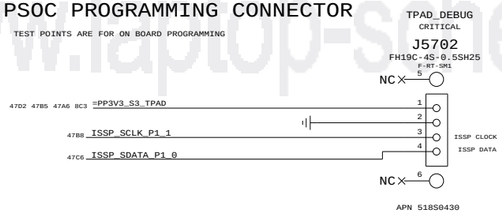
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

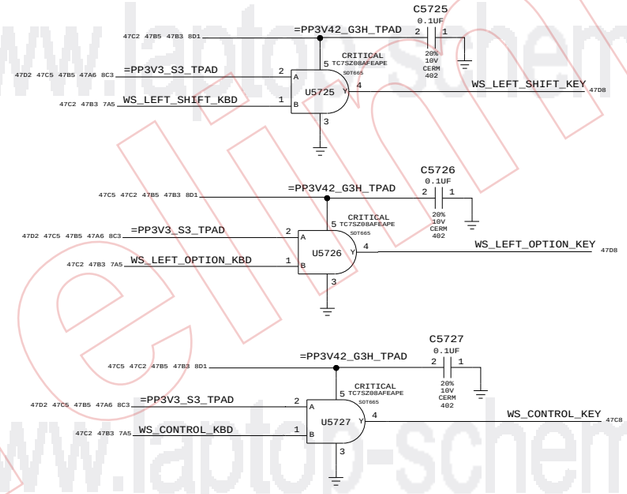
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

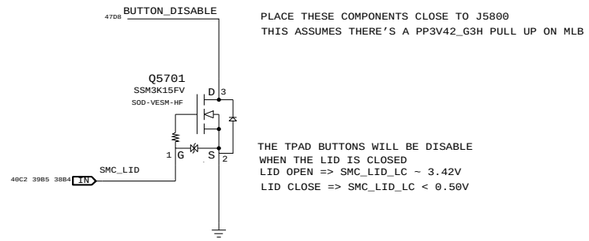
TEST POINTS ARE FOR ON BOARD PROGRAMMING



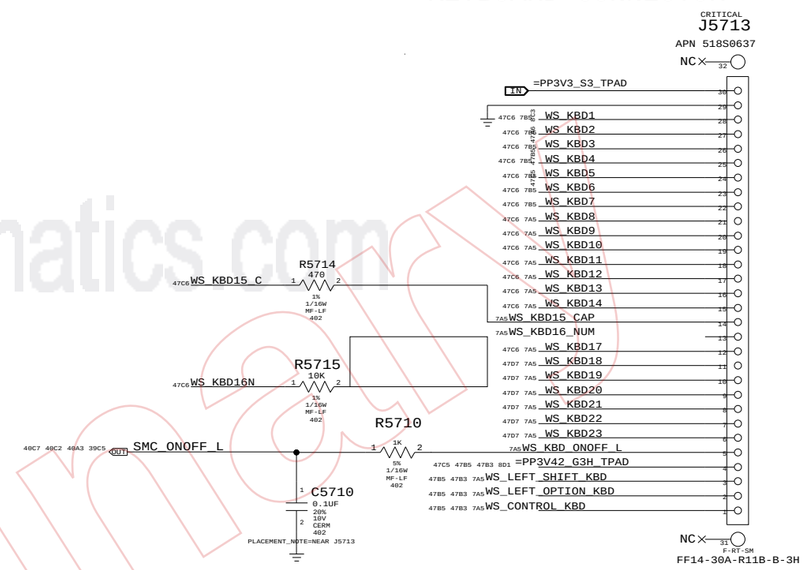
ISOLATION CIRCUIT



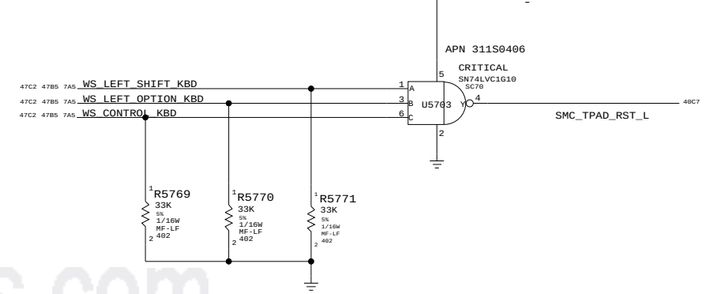
TPAD BUTTONS DISABLE



KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC

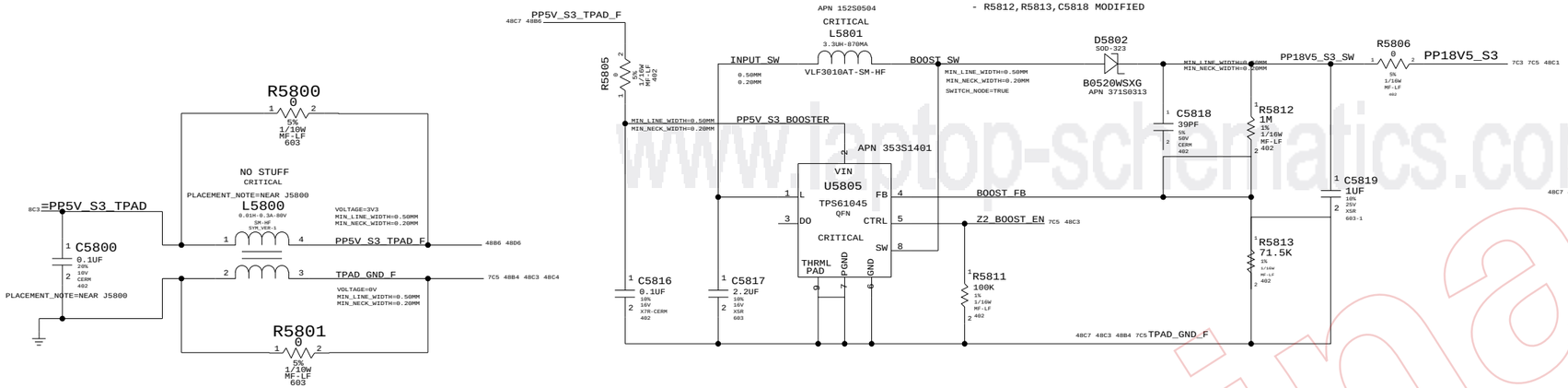


WELLSPRING 1	
SYNC_MASTER=YUAN.MA	SYNC_DATE=04/22/2008

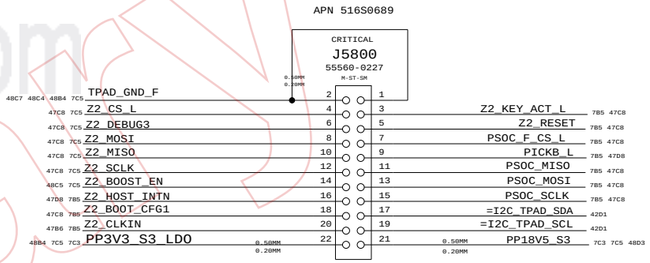
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
	SCALE: NONE	SHT 57 OF 109	

BOOSTER +18.5VDC FOR SENSORS

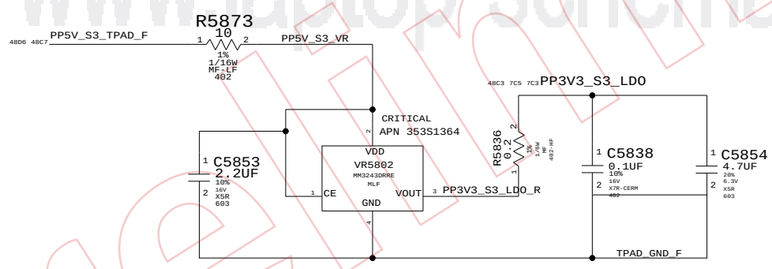
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



KEYBOARD BACKLIGHT DRIVNG AND DETECTION

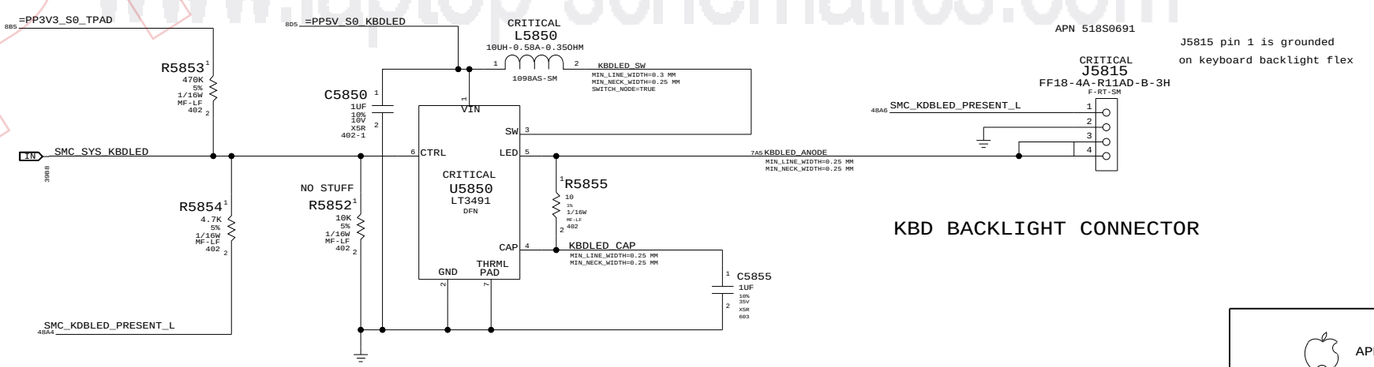
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT



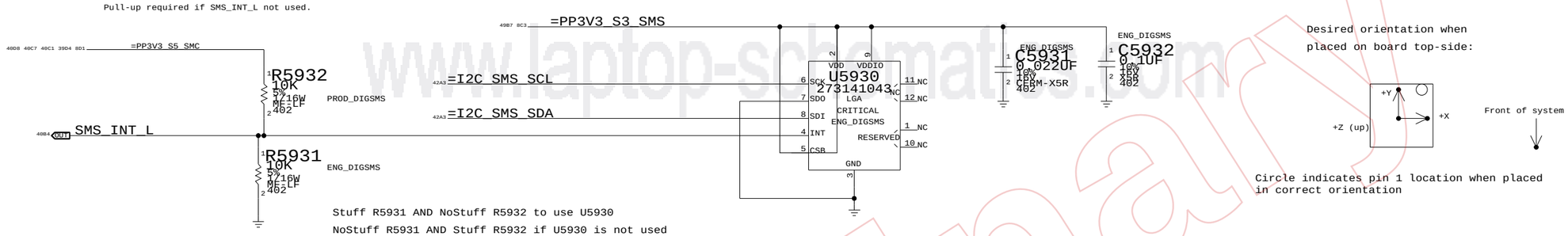
KBD BACKLIGHT CONNECTOR

WELLSPRING 2	
SYNC_MASTER=YUAN.MA	SYNC_DATE=05/09/2008

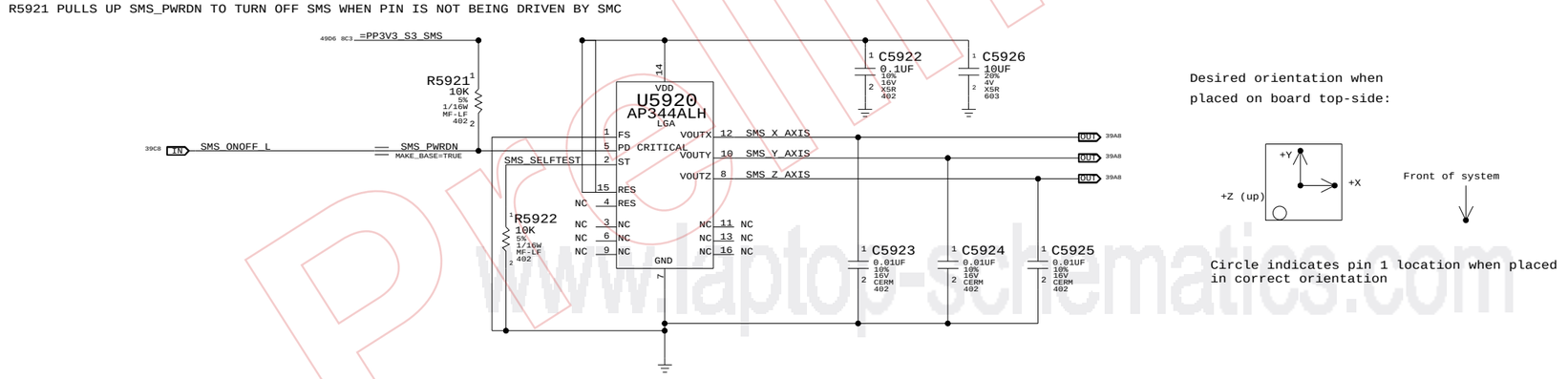
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 58 OF 109	

Digital SMS



Analog SMS

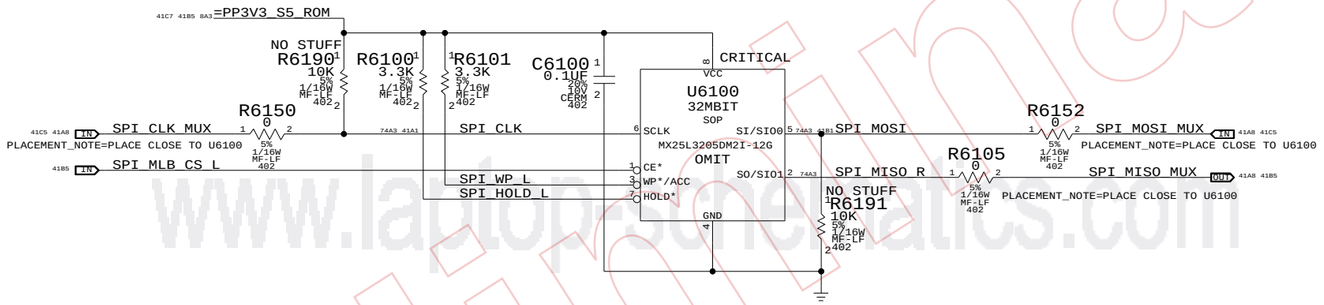


SMS

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 59 OF 109	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE	SHT	OF
NONE	61	109

AUDIO CODEC

APPLE P/N 353S1538

ALIAS OF PP3V3_SO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

VOLTAGE=3.3V
=PP3V3_S0_AUDIO

CRITICAL
L6201
FERR-220-OHM
0402

MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.28MM
VOLTAGE=3.3V
CODEC_DVDD

CRITICAL
C6200 1UF 10% 6.3V CERM 402
C6201 0.01UF 10% 25V X7R 402
C6203 0.01UF 10% 25V X7R 402

R6270 100K 5% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.28MM
AVDD_ADC_DAC

CRITICAL
C6204 100UF 20% 6.3V TANT CASE-AL1
C6206 0.01UF 10% 25V X7R 402
CRITICAL
C6205 100UF 20% 6.3V TANT CASE-AL1
C6207 0.01UF 10% 25V X7R 402

CRITICAL
L6202
FERR-220-OHM
0402

MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=4.6V
PP4V6_AUDIO_ANALOG 7C3 51A3 52D6

GND_AUDIO_CODEC 51A7 51B7 52B6 52C3 52C6 53A8 53B8 53C8 54B3 55A2 55A4 55A8 55B4 55B5 55B8 55C4

HDA_BIT_CLK 74B3 21D2 IN
HDA_SYNC 74A3 21C2 IN
HDA_SDOUT 74A3 21D2 IN
HDA_SDIN0 74A3 21D7 OUT

R6204 22 5% 1/16W MF-LF 402

HP AMP. SHDN CONTROL
AUD_GPIO_0 55D3 OUT

PORT C RT=SUB. SPKR SIGNAL SOURCE
AUD_BI_PORT_C_R 53B8 OUT
AUD_BI_PORT_D_L 55C4 OUT
AUD_BI_PORT_D_R 55B4 OUT
PORT D=HP SIGNAL SOURCE

HDA_RST_L 74A3 21D2 IN

R6203 100K 5% 1/16W MF-LF 402
CRITICAL
C6208 0.1UF 10% 10V X5R 402

NO STUFF
R6201 0 5% 1/16W MF-LF 402

CRITICAL
U6200
ALC885Q-VB3-GR
QFN
REV B3

DVDD	1		
DVDD_IO	9		
AVDD1	25		
AVDD2	38		
	6	BCLK	
	10	SYNC	
	5	SDATA_OUT	
CODEC_SDATA_IN	8	SDATA_IN	
AUD_GPIO_1	3	GPIO1/DMIC-L	
	2	GPIO0/DMIC-CLK	
NC_AUD_BI_PORT_C_L NO_TEST	23	PORT-C-L	
	24	PORT-C-R	
	35	PORT-D-L	
	36	PORT-D-R	
NC_BAL_IN_L NO_TEST	18	CD-L	
NC_BAL_IN_COM NO_TEST	19	CD-GND	
NC_BAL_IN_R NO_TEST	20	CD-R	
BEEP	12	BEEP	
	11	RESET*	
THRM_PAD	49		
DVSS	4		
	7		
AVSS1	26		
AVSS2	42		
SPDIFO	48	SPDIFI/EAPD/MIDI-I/DMIC-R	47
SENSE_A	13		
SENSE_B	34		
PORT-A-L	39		
PORT-A-R	41		
PORT-F-L	16		
PORT-F-R	17		
PORT-F-VREFO	30		
PORT-A-VREFO/DCVOL	33 NO_TEST	NC_AUD_VREF_PORT_A	
PORT-E-L	14		
PORT-E-R	15		
PORT-E-VREFO	31 NO_TEST	NC_AUD_VREF_PORT_E	
PORT-B-VREFO	28		
PORT-B-L	21		
PORT-B-R	22		
PORT-C-VREFO	29 NO_TEST	NC_AUD_VREF_PORT_C	
PORT-B-VREFO2	32 NO_TEST	NC_AUD_VREF_PORT_D	
PORT-G-L	43 NO_TEST	NC_AUD_BI_PORT_G_L	
PORT-G-R	44 NO_TEST	NC_AUD_BI_PORT_G_R	
PORT-H-L	45 NO_TEST	NC_AUD_BI_PORT_H_L	
PORT-H-R	46 NO_TEST	NC_AUD_BI_PORT_H_R	
VREF	27	AUD_CODEC_VREF	
JDREF	40	AUD_CODEC_JDREF	
NC	37 NC_VRP NO_TEST		

AUD_SPDIF_O

R6206 22 5% 1/16W MF-LF 402

AUD_SPDIF_OUT 54D3 OUT
AUD_SPDIF_I 54B3 IN
AUD_SENSE_A 55C8 55A8 IN
AUD_SENSE_B 55C8 IN

PORT A = LINE INPUT
AUD_BI_PORT_A_L 55B1 IN
AUD_BI_PORT_A_R 55A1 IN
AUD_BI_PORT_F_L 55A4 IN
AUD_BI_PORT_F_R 55A4 IN — PORT F= MIC INPUT
AUD_VREF_PORT_F 55B4 OUT — PORT F VREF=MIC BIAS
AUD_BI_PORT_E_L 52B4 IN — PORT E = MIKEY MIC INPUT

SPKR. AMP. SHDN CONTROL
AUD_VREF_PORT_B 53C8 53B8 53A8 OUT
AUD_BI_PORT_B_L 53A8 OUT
AUD_BI_PORT_B_R 53C8 OUT
PORT B=L AND R SPKR AMP. SIGNAL SOURCE

R6209 100K 5% 1/16W MF-LF 402

R6205 20.0K 1% 1/16W MF-LF 402

CRITICAL
C6210 3.3UF 10% 16V TANT SMA-HF

C6212 0.001UF 10% 50V CERM 402

GND_AUDIO_CODEC 55A2 54B3 53C8 53B8 53A8 52C6 52C3 52B6 51D3 51A7 55C4 55B8 55B5 55B4 55A8 55A4
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

AUDIO 4.6V REGULATOR

APPLE P/N 353S1897

ALIAS OF PP5VLT_S3, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

VOLTAGE=5V
=PP5V_S3_AUDIO

CRITICAL
L6200
FERR-220-OHM
0402

MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.30MM
PP5V_S3_AUDIO_F

CRITICAL
U6201
MAX8902A
TDFN

=PP3V3_S0_AUDIO

R6202 1K 5% 1/16W MF-LF 402

PP4V6_ENABLE

EN	3	
IN	1	
BP	7	
GND	2	
	9	THRML PAD
SELA	4	
SELB	5	
OUT	8	
OUTS	6	

MAX8902_BP

C6220 0.1UF 10% 16V X5R 402
R6210 10K 5% 1/16W MF-LF 402
C6223 0.01UF 10% 25V X7R 402
CRITICAL
C6221 10UF 20% 6.3V X5R 603
C6224 0.01UF 10% 50V X7R 603-1
CRITICAL
C6222 10UF 20% 6.3V X5R 603
C6225 0.01UF 10% 25V X7R 402

PP4V6_AUDIO_ANALOG 7C3 51D3 52D6

GND_AUDIO_CODEC 55A2 54B3 53C8 53B8 53A8 52C6 52C3 52B6 51D3 51B7 55C4 55B8 55B5 55B4 55A8 55A4

XW6200 SM
PLACE XW6200 AND XW6201 NEAR U6201
XW6201 SM
STAR GND PT. FOR AUDIO SYSTEM
GND_SPKR_AMP 53C4 53B3 53A4

AUDIO: CODEC

SYNC_MASTER=AUDIO
SYNC_DATE=07/01/2008

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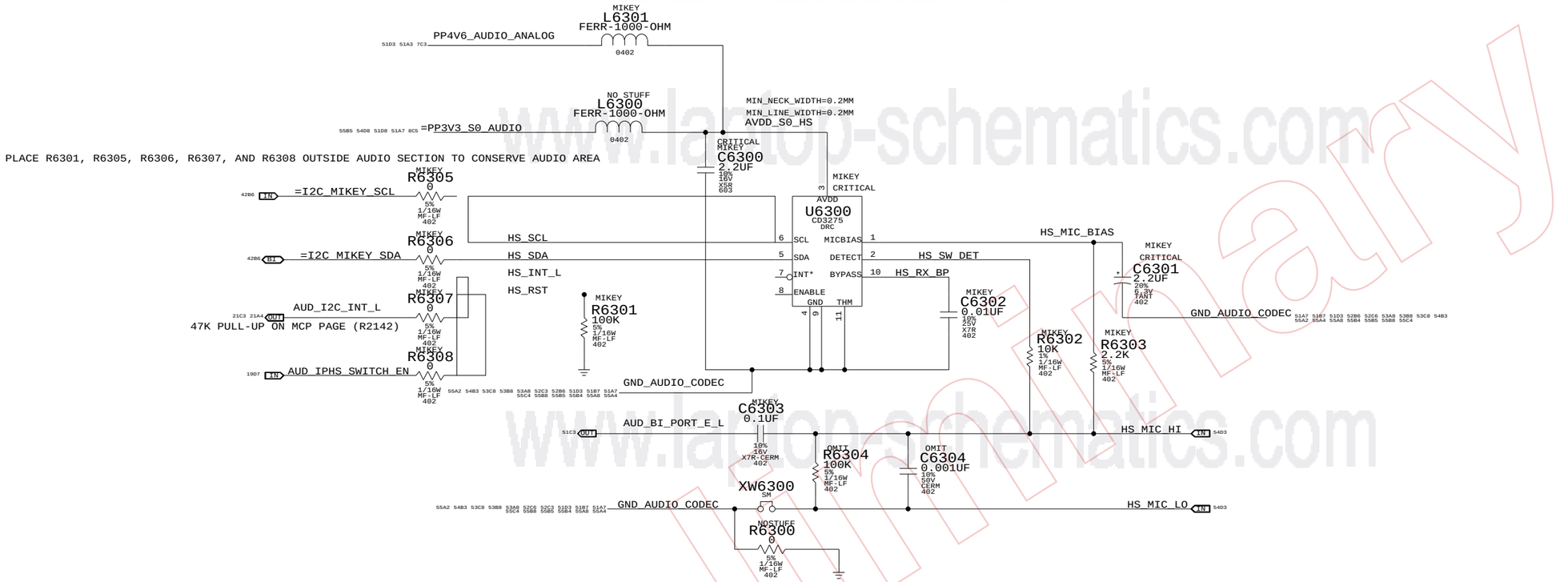
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 62 OF 109	

MIKEY RECEIVER CKT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6304	?	NOMIKEY
132S0045	1	100PF 50V 10% 0402 CAPACITOR	C6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6304	?	NOMIKEY

AUDIO: MIKEY

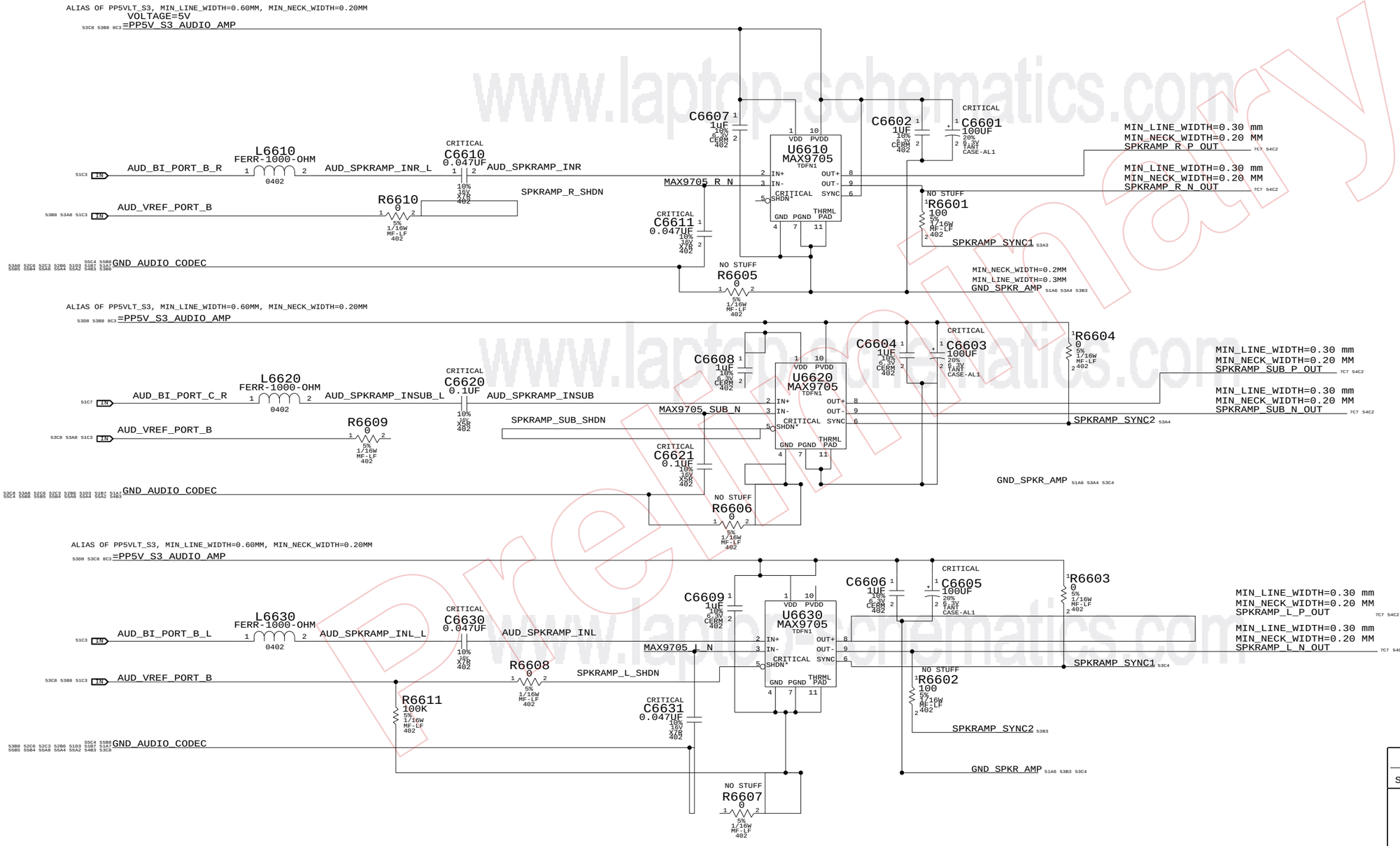
SYNC_MASTER=AUDIO SYNC_DATE=07/03/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 63 OF 109	

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	12DB



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 66 OF 109	

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

=PP3V3_S0_AUDIO
R6790 0 5% 1/16W MF-LF 402
PP3V3_S0_AUDIO_SPDIF
AUD_CONNJ1_MIC
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_CONNJ1_SLEEVEDET
R6702 0 5% 1/16W MF-LF 402
R6703 0 5% 1/16W MF-LF 402
R6704 0 5% 1/16W MF-LF 402
R6705 0 5% 1/16W MF-LF 402
R6706 0 5% 1/16W MF-LF 402
R6707 0 5% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.15MM
MIN_LINE_WIDTH=0.2MM
CRITICAL
J6700
AUDIO-JACK-TRANS-M97
F-RT-TH3
AUDIO
A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
APN:514-0607
C6700 1UF 10% 6.3V CERM 402
CRITICAL DZ6706 6.8V-100PF 402
CRITICAL DZ6702 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402
C6705 100PF 5% 50V C0BM 402
=GND_CHASSIS_AUDIO_JACK
NOSTUFF R6760 0 5% 1/16W MF-LF 402 CHASSIS GND BAND AID
AUD_CONNJ1_MIC_F
AUD_CONNJ1_SLEEVE_F
AUD_CONNJ1_TIPDET_F
AUD_CONNJ1_RING_F
AUD_CONNJ1_TIP_F
AUD_CONNJ1_SLEEVEDET_F
L6709 FERR-1000-OHM 0402
L6710 FERR-1000-OHM 0402
CRITICAL L6701 FERR-120-OHM-1.5A 0402-LF
L6704 FERR-1000-OHM 0402
L6706 FERR-1000-OHM 0402
R6700 10K 5% 1/16W MF-LF 402
R6701 4.7 5% 1/16W MF-LF 402
AUD_SPDIF_OUT
HS_MIC_HI
HS_MIC_LO
AUD_LO_AMP_OUTR
AUD_LO_AMP_OUTL
AUD_J1_SLEEVEDET_R
AUD_J1_TIPDET_R
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.4MM
AUD_J1_COM
XW6700 SM
AUD_LO_GND

MIC CONNECTOR

APN:518S0520

CRITICAL J6701 78171-0003 M-RT-SM
MIC_LO_CONN
MIC_HI_CONN
MIC_SHLD_CONN

SPEAKER CONNECTOR

APN:518S0519

CRITICAL J6702 78171-0002 M-RT-SM
SPKRAMP_L_P_OUT
SPKRAMP_L_N_OUT
SPKRAMP_SUB_P_OUT
C6760 100PF 5% 50V CERM 402
C6761 100PF 5% 50V CERM 402
C6762 100PF 5% 50V CERM 402
C6763 100PF 5% 50V CERM 402
CRITICAL J6703 78171-0004 M-RT-SM
SPKRAMP_SUB_N_OUT
SPKRAMP_R_P_OUT
SPKRAMP_R_N_OUT
APN:518S0521
C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

=PP3V3_S0_AUDIO_SPDIF
AUD_J2_OPT_OUT
R6749 22 5% 1/16W MF-LF 402
AUD_CONNJ2_SLEEVE
AUD_CONNJ2_TIPDET
AUD_CONNJ2_TIP
AUD_CONNJ2_RING
AUD_CONNJ2_SLEEVEDET
R6752 0 5% 1/16W MF-LF 402
R6753 0 5% 1/16W MF-LF 402
R6754 0 5% 1/16W MF-LF 402
R6755 0 5% 1/16W MF-LF 402
R6756 0 5% 1/16W MF-LF 402
CRITICAL
J6750
AUDIO-RCVR-M97
F-RT-TH3
AUDIO
A - VDD
B - GND
C - VOUT
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
APN:514-0608
C6750 1UF 10% 6.3V CERM 402
CRITICAL DZ6752 6.8V-100PF 402
CRITICAL DZ6753 6.8V-100PF 402
CRITICAL DZ6754 6.8V-100PF 402
CRITICAL DZ6755 6.8V-100PF 402
C6756 100PF 5% 50V C0BM 402
=GND_CHASSIS_AUDIO_JACK
AUD_CONNJ2_SLEEVE_F
AUD_CONNJ2_TIPDET_F
AUD_CONNJ2_RING_F
AUD_CONNJ2_TIP_F
AUD_CONNJ2_SLEEVEDET_F
CRITICAL L6751 FERR-120-OHM-1.5A 0402-LF
L6754 FERR-1000-OHM 0402
L6756 FERR-1000-OHM 0402
R6750 10K 5% 1/16W MF-LF 402
R6751 4.7 5% 1/16W MF-LF 402
AUD_SPDIF_I
AUD_PORTA_R
AUD_PORTA_L
AUD_J2_TIPDET_R
XW6701 SM
AUD_J2_COM
GND_AUDIO_CODEC

MIC EMI FILTER

MIC_LO
MIC_HI
L6770 FERR-1000-OHM 0402
L6771 FERR-1000-OHM 0402
L6772 FERR-1000-OHM 0402
L6773 FERR-1000-OHM 0402
MIC_LO_CONN_F
MIC_HI_CONN_F
MIC_LO_CONN
MIC_HI_CONN
CRITICAL DZ6770 6.8V-100PF 402
CRITICAL DZ6771 6.8V-100PF 402
=GND_CHASSIS_AUDIO_MIC

AUDIO: JACK

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

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APPLE INC.

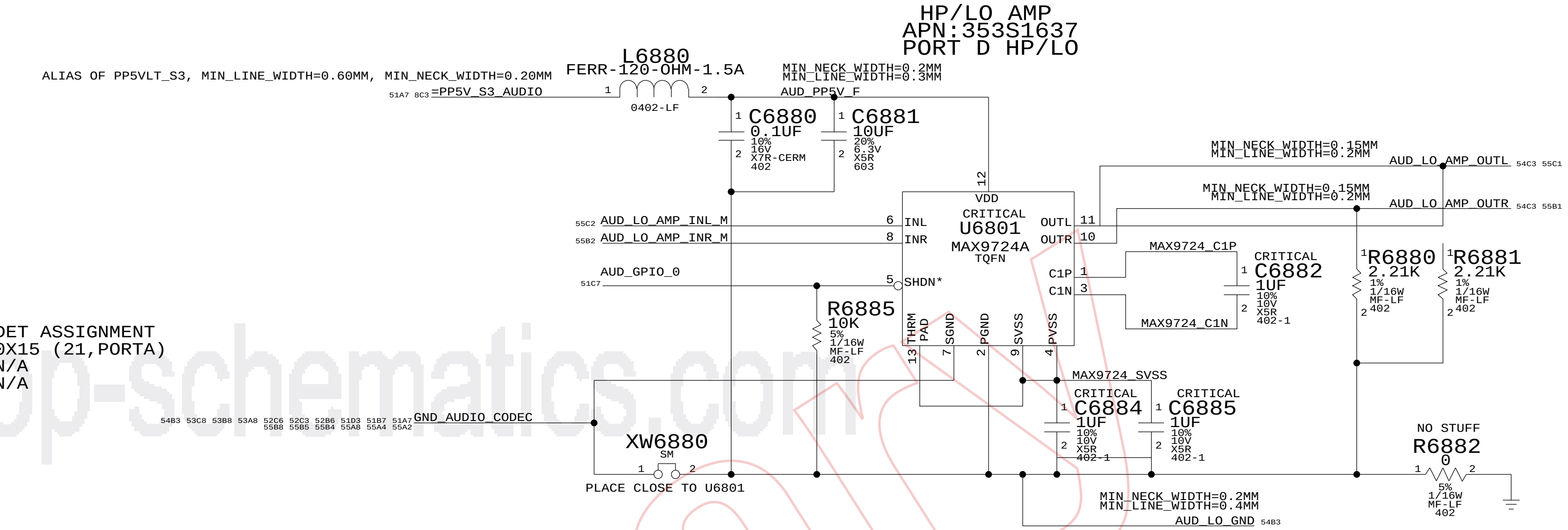
SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	67	109

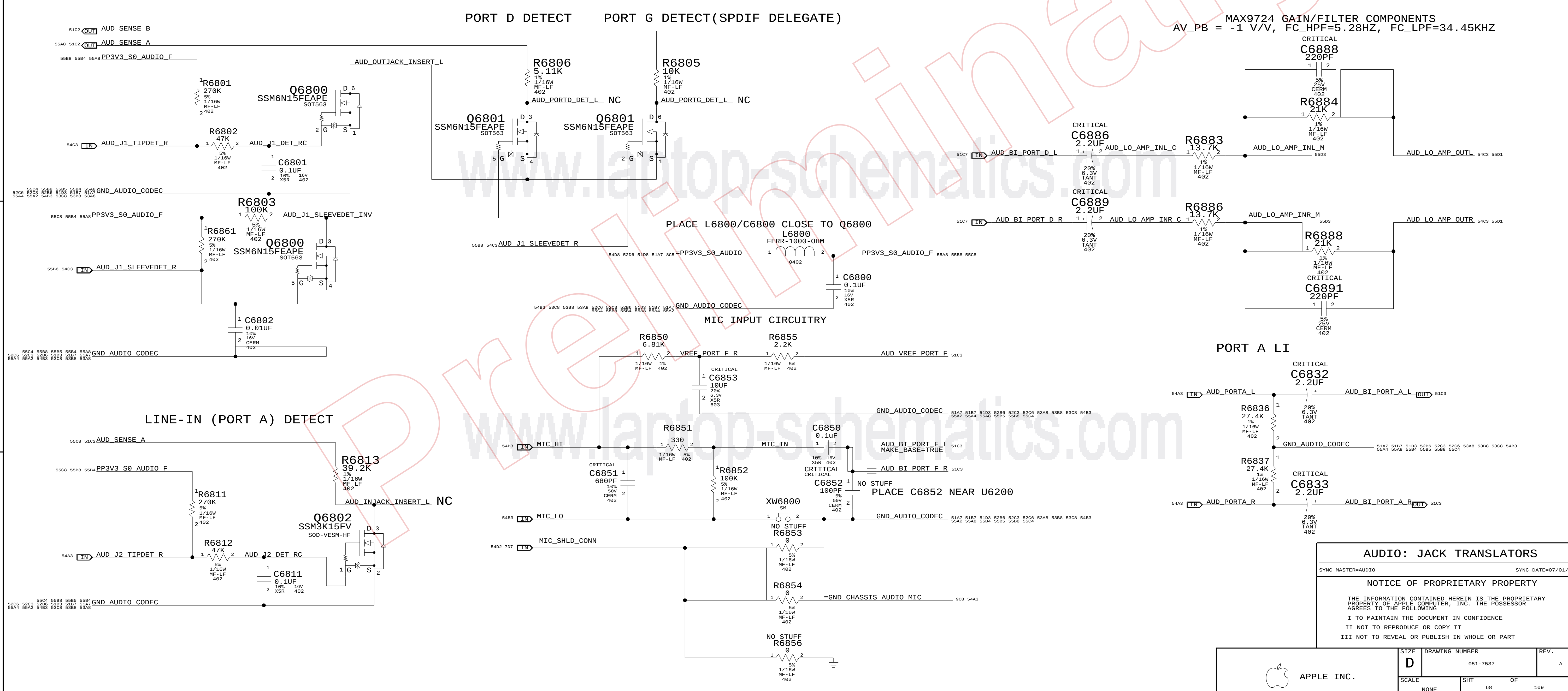
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0C (12)	0X02 (2)	0X14 (20,PORTD)	GPIO 0	0X14 (20,PORTD)
SAT SPKRS	0X0D (13)	0X03 (3)	0X18 (24,PORTB)	VREF_B(100%)	N/A
SUB SPKR	0X0F (15)	0X05 (5)	0X1A (26,PORTC)	VREF_B(100%)	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X16 (22, PORTG)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X15 (21,PORTA)	N/A	0X15 (21,PORTA)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X19 (25,PORTF)	VREF_F (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A





AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE NONE SHT 68 OF 109

MagSafe DC Power Jack

CRITICAL
J6900
78048-0573
M-RT-SM
518S0656

787 PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

CRITICAL
F6905
6AMP-24V
1206-1

C6905 0.01UF 20% 50V CERM 603

R6928 0 5% 1/16W MF-LF 402

787 ADAPTER_SENSE

ADAPTER_SENSE_R

Q6910 restricts system load to 10K-70K window until adapter detects system and enables 16.5V output.

=PP18V5_DCIN_CONN 8C2 56B8

1-Wire OverVoltage Protection

CRITICAL
Q6910
NTUD3127CXXG
SOT-963
Vgs(max) = 8V

PP18V5_DCIN_ONEWIRE
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

R6917 270K 5% 1/16W MF-LF 402
P-CHN
R6911 180K 5% 1/16W MF-LF 402

C6915 0.1UF 10% 25V X5R 402

<Ra>
R6913 100K 5% 1/16W MF-LF 402

If ADAPTER_SENSE > Vth
then turn off FET

ONEWIRE_PWR_EN_L_DIV
Vgs = 7.30V @ 20V DCIN
Vgs = 4.74V @ 13V DCIN

R6915 270K 5% 1/16W MF-LF 402
ONEWIRE_EN
R6918 270K 5% 1/16W MF-LF 402
R6912 470K 5% 1/16W MF-LF 402

ONEWIRE_DCIN_DIV
<Vth>

CRITICAL
U6915
LM397
SOT23-5-HF

CRITICAL
Q6915
SSM3K15FV
SOD-VESM-HF

<Rb>
R6914 100K 5% 1/16W MF-LF 402

ONEWIRE_ESD
ONEWIRE_OVERVOLT

R6916 270K 5% 1/16W MF-LF 402

C6917 0.001UF 10% 50V CERM 402

ONEWIRE_PWR_EN_L

CRITICAL
Q6910
N-CHN
NTUD3127CXXG
SOT-963

R6910 1K 5% 1/16W MF-LF 402
SMC_BC_ACOK_RC
SMC_BC_ACOK 4N 39C5 40B2 40D5

C6910 0.001UF 10% 50V CERM 402

Vth = Vdcin * (Rb / (Ra + Rb))
Vth = Vdcin / 2

R6920 24.3K 1% 1/16W MF-LF 402

VOLTAGE DIVIDER FROM DCIN ENSURES Q6910
Vgs is met when SYS_ONEWIRE is high or low.
Q6920 used as bilateral switch to ensure
SYS_ONEWIRE doesn't drive unpowered U6990

CRITICAL
Q6920
SSM6N15FEAPE
SOT563

SYS_ONEWIRE_BILAT
SYS_ONEWIRE 8I 39B8 40B2

R6905 47 5% 1/8W MF-LF 805
56D1 8C2 =PP18V5_DCIN_CONN
PPDCIN_S5_P3V42G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=18.5V

D6905
HN2D01JEAPE
SOT665

57A2 56A7 BATT_POS_F
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=12.6V

NC NC

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

C6990 10UF 10% 25V X5R 805

U6990
LT3470ETS8
TSOT23-8
VIN BOOST SHDN* NC NC SW BIAS FB GND

P3V42G3H_BOOST
C6994 0.22uF 20% 6.3V X5R 402

CRITICAL
L6995
33UH
CDPH4D19FHF-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

=PP3V42_G3H_REG 8D2

Vout = 3.425V
200mA max output
(Switcher limit)

C6995 22pF 5% 50V CERM 402

<Ra>
R6995 348K 1% 1/16W MF-LF 402

CRITICAL
C6999 22UF 20% 6.3V CERM 805

P3V42G3H_FB

<Rb>
R6996 200K 1% 1/16W MF-LF 402

Vout = 1.25V * (1 + Ra / Rb)

BIL BUTTON DEBOUNCE CIRCUIT

56A3 8D1 =PP3V42_G3H_BATT

C6960 0.1UF 10% 16V X5R 402

R6960 10K 1/16W 402 MF-LF 5%

U6960
74LVC1G17DRL
SOT-553

(SMC_BIL_BUTTON_L)
SMC_BIL_BUTTON_L OUT 39C5
TO SMC

C6961 0.01UF 10% 25V X7R 402

BATTERY POWER CONNECTOR

CRITICAL
J6950
BAT-M98
F-RT-SM
516S0698

7B7 PPVBAT_G3H_CONN_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

L6950
FERR-50-OHM
SM-LF

57A2 56B8 BATT_POS_F

=SMBUS_BATT_SCL 42C3 56A3
=SMBUS_BATT_SDA 42C3 56A3
SMC_BS_ALRT_L

CRITICAL
D6950
RCLAMP2402B
SC-75

C6956 47PF 5% 50V CERM 402

C6950 0.1UF 10% 25V X5R 402

L6951
FERR-50-OHM
SM-LF

7A7 GND_BATT_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=0V

BATTERY SIGNAL CONNECTOR

CRITICAL
J6955
78171-0005
M-RT-SM
518S0588

=PP3V42_G3H_BATT OUT 8D1 56B3
=SMBUS_BATT_SDA BI 42C3 56A6
=SMBUS_BATT_SCL BI 42C3 56A6
7A7 SMC_BIL_BUTTON_DB_L

C6954 0.001UF 10% 50V CERM 402
C6952 47PF 5% 50V CERM 402
C6951 0.1UF 10% 25V X5R 402
C6953 47PF 5% 50V CERM 402

DC-In & Battery Connectors

SYNC_MASTER=JACK SYNC_DATE=03/13/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 69 OF 109	

PBUS SUPPLY / BATTERY CHARGER

=PP18V5_G3H_CHGR
D7010 1SS418 SOD-723-HF
CHGR_DCIN
C7063 0.1UF 10% 25V X5R 402
R7098 100K 5% 1/16W MF-LF 402
Q7000 HAT1127H LFPAK-SM CRITICAL
PPVDCIN_G3H_PRE2
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.3 MM
Q7001 HAT1127H LFPAK-SM CRITICAL
PPVDCIN_G3H_PRE
CHGR_SGATE
R7001 62K 5% 1/16W MF-LF 402
=PP3V42_G3H_CHGR
R7060 57.6K 1% 1/16W MF-LF 402
C7060 0.1UF 10% 25V X5R 402
CHGR_AMON
R7061 1.82K 1% 1/16W MF-LF 402
CHGR_LOWCURRENT_REF
U7060 TL331 SOT23-5 CRITICAL
CHGR_LOWCURRENT_GATE
R7062 62K 5% 1/16W MF-LF 402
CHGR_LOWCURRENT_GATE_R
R7099 100K 5% 1/16W MF-LF 402
R7023 10 5% 1/16W MF-LF 402
XW7020 SM
CHGR_CSIP_XW7020
C7024 0.047UF 10% 16V CERM 402
R7021 10 5% 1/16W MF-LF 402
R7020 0.02 0.5% 1W MF 0612 CRITICAL
XW7021 SM
CHGR_CSIN_XW7021
MIN_NECK_WIDTH=0.3 MM MIN_LINE_WIDTH=0.6 MM PP18V5_S5_CHGR_SW_R
C7020 22UF 20% 25V POLY-TANT CASE-D2-SM CRITICAL
C7021 22UF 20% 25V POLY-TANT CASE-D2-SM CRITICAL
C7022 1UF 10% 25V X5R 603-1
C7023 1UF 10% 25V X5R 603-1
C7027 0.001UF 10% 50V CERM 402
C7010 0.1UF 10% 25V X5R 402
(CHGR_ACIN)
R7010 30.1K 1% 1/16W MF-LF 402
R7011 9.31K 1% 1/16W MF-LF 402
CHGR_VDD
R7040 4.7 5% 1/16W MF-LF 402
CHGR_VDDP
C7041 1UF 10% 16V X5R 402-1
C7040 1UF 10% 16V X5R 402-1
=PP3V42_G3H_CHGR
C7047 1UF 10% 16V X5R 402-1
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
U7000 ISL6258A QFN CRITICAL
VHST SCL SDA VREF ACIN ICOMP VCOMP VNEG CSOP CSON
AGATE CSIP CSIN BGATE DCIN BOOT UGATE PHASE LGATE TRKL* AMON BMON ACOK
THRM_PAD AGND PGND
CHGR_AGATE CHGR_CSIP CHGR_CSIN CHGR_BGATE CHGR_DCIN CHGR_BOOT CHGR_UGATE CHGR_PHASE CHGR_LGATE CHGR_AMON CHGR_BMON =CHGR_ACOK
GND_CHGR_SGND
C7061 0.1UF 10% 25V X5R 402
C7062 0.1UF 10% 25V X5R 402
CHGR_ACIN
C7042 0.033UF 10% 16V X5R 402
C7044 0.01UF 10% 16V CERM 402
R7045 56.2K 1% 1/16W MF-LF 402
CHGR_VCOMP_R
C7043 0.1UF 10% 16V X5R 402
C7045 0.001UF 10% 50V CERM 402
R7046 3.01K 1% 1/16W MF-LF 402
CHGR_VNEG_R
C7046 470PF 10% 16V CERM 402
XW7000 SM
C7026 0.001UF 10% 50V X7R 402
GND_CHGR_SGND
(CHGR_CSOP)
(CHGR_CSON)
(CHGR_CSO_R_N)
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM
C7025 0.1UF 10% 25V X5R 402
Q7020 RJK0305DPB LFPAK-HF CRITICAL
Q7021 RJK0305DPB LFPAK-HF CRITICAL
L7000 4.7UH-9.5A IHLP4040DZ-SM CRITICAL
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.25 MM
PPVBAT_G3H_CHGR_REG
C7008 33UF 20% 16V POLY-TANT CASED2E-SM CRITICAL
R7008 0.01 0.5% 1W MF 0612 CRITICAL
=PPBUS_G3H
F7000 7AMP 1206 CRITICAL
TO SYSTEM
PPVBAT_G3H_CHGR_OUT
C7011 1UF 10% 25V X5R 603-1
C7028 0.001UF 10% 50V CERM 402
R7031 10 5% 1/16W MF-LF 402
CHGR_CSO_R_P
R7047 10 5% 1/16W MF-LF 402
CHGR_CSO_R_N

PWM FREQ. = 400 kHz
MAX CURRENT = 7A
(??? limited)

AMON PULLDOWN LOGIC

CHGR_AMON
=PP3V42_G3H_CHGR
R7074 1M 5% 1/16W MF-LF 402
Q7070 SSM6N15FEAPE SOT563
NOSTUFF R7075 1M 5% 1/16W MF-LF 402
CHGR_VDD_L
Q7070 SSM6N15FEAPE SOT563
CHGR_VDD
R7073 1K 5% 1/16W MF-LF 402
CHGR_VDD_R

BATTERY INRUSH FETS

PPVBAT_G3H_CHGR_OUT
C7050 0.01uF 10% 16V CERM 402
C7051 0.1UF 10% 16V X5R 402
Q7050 FDS6681Z SO-8 CRITICAL
BATT_POS_INRUSH
Q7052 FDS6681Z SO-8 CRITICAL
C7052 0.1UF 10% 16V X5R 402
R7052 1M 5% MF-LF 402 1/16W
R7053 330K 5% MF-LF 402 1/16W
CHGR_BGATE
BATT_POS_GATE
BATT_POS_F

TO BATTERY

PBUS Supply/Battery Charger		
SYNC_MASTER=RAYMOND	SYNC_DATE=01/31/2008	

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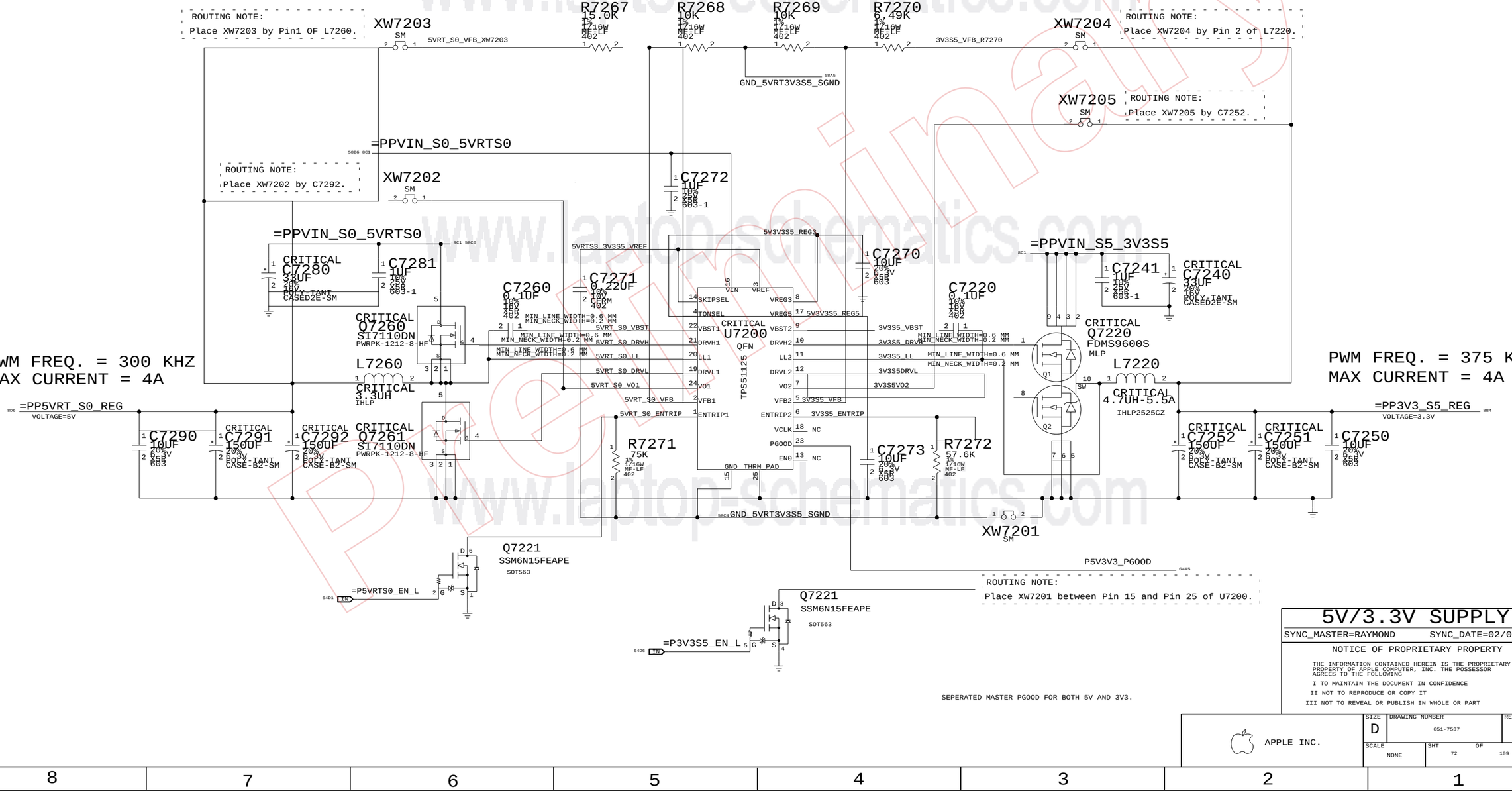
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 70 OF 109	

5V_RT/3.3V POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



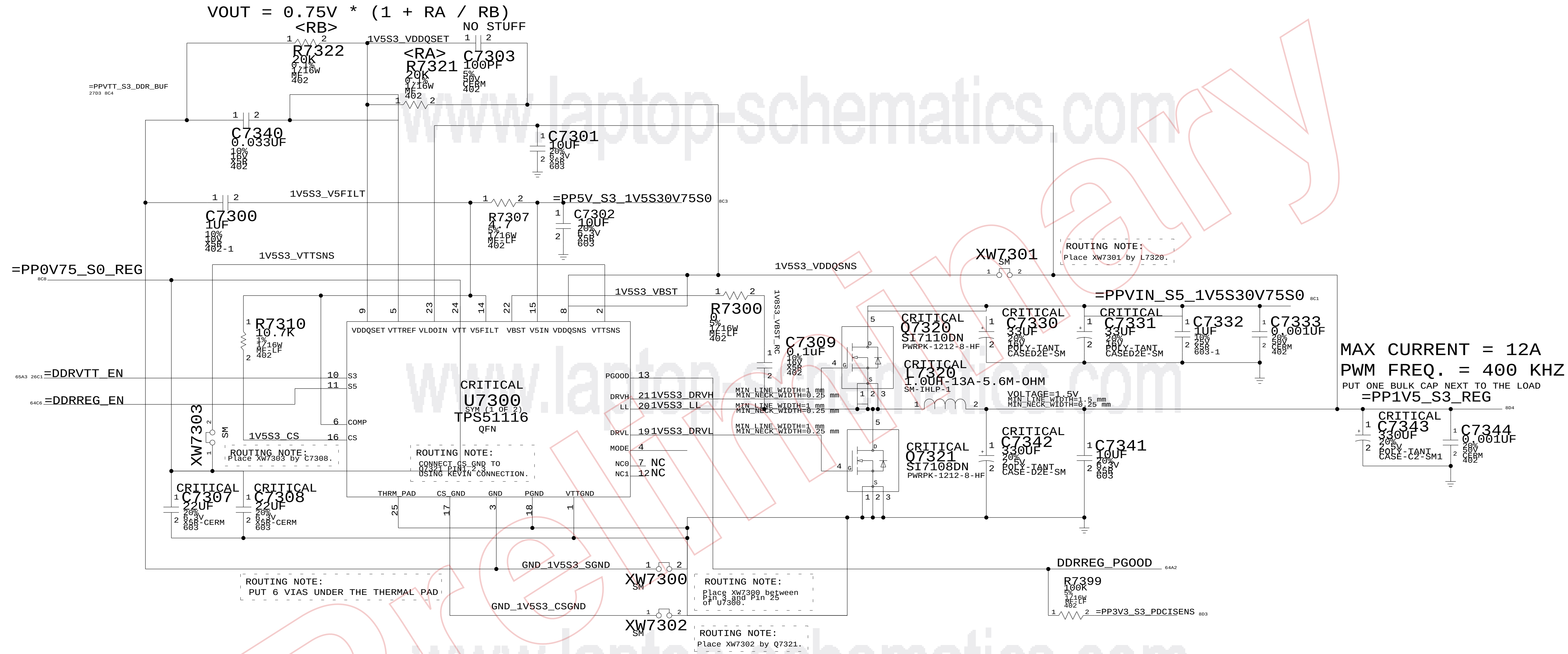
5V/3.3V SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 72 OF 109	

1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

1.5V/0.75V DDR3 SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE D DRAWING NUMBER 051-7537 REV. A

SCALE NONE SHT 73 OF 109

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

PWM FREQ. = 300 KHZ
MAX CURRENT = 44A
LOAD LINE SLOPE = -2.1 MV/A

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

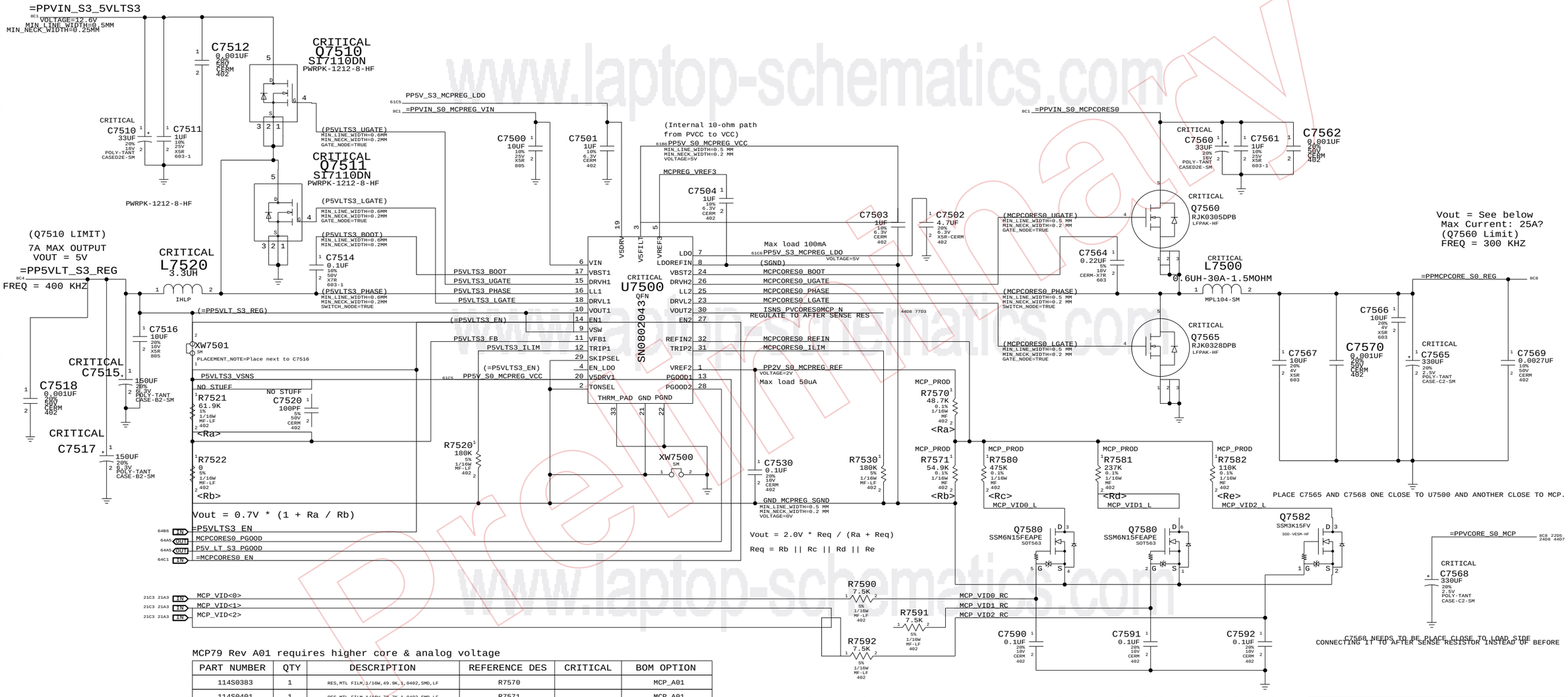
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE D | DRAWING NUMBER 051-7537 | REV. A
SCALE NONE | SHT 74 OF 109

MCP VCORE/5V_S3 LEFT REGULATOR



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0383	1	RES,MTL FILM,1/16W,49.9K,1,0402,SMD,LF	R7570		MCP_A01
114S0401	1	RES,MTL FILM,1/16W,78.7K,1,0402,SMD,LF	R7571		MCP_A01
114S0484	1	RES,MTL FILM,1/16W,549K,1,0402,SMD,LF	R7580		MCP_A01
114S0454	1	RES,MTL FILM,1/16W,274K,1,0402,SMD,LF	R7581		MCP_A01
114S0423	1	RES,MTL FILM,1/16W,133K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01P&MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01P&MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01P&MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01P&MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01P&MCP_A01Q

Rev A01 Production

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:
Added C7568 bulk cap on output.
Tied TON to REF.
Changed Q7510 to 376S0674.
C7500 changed to 138S0638.
L7560 changed from T18 MLB inductor to 152S0782.
Changed Q7565 to 376S0637.
Changed R7514 to 280K, R7564 to 180K.

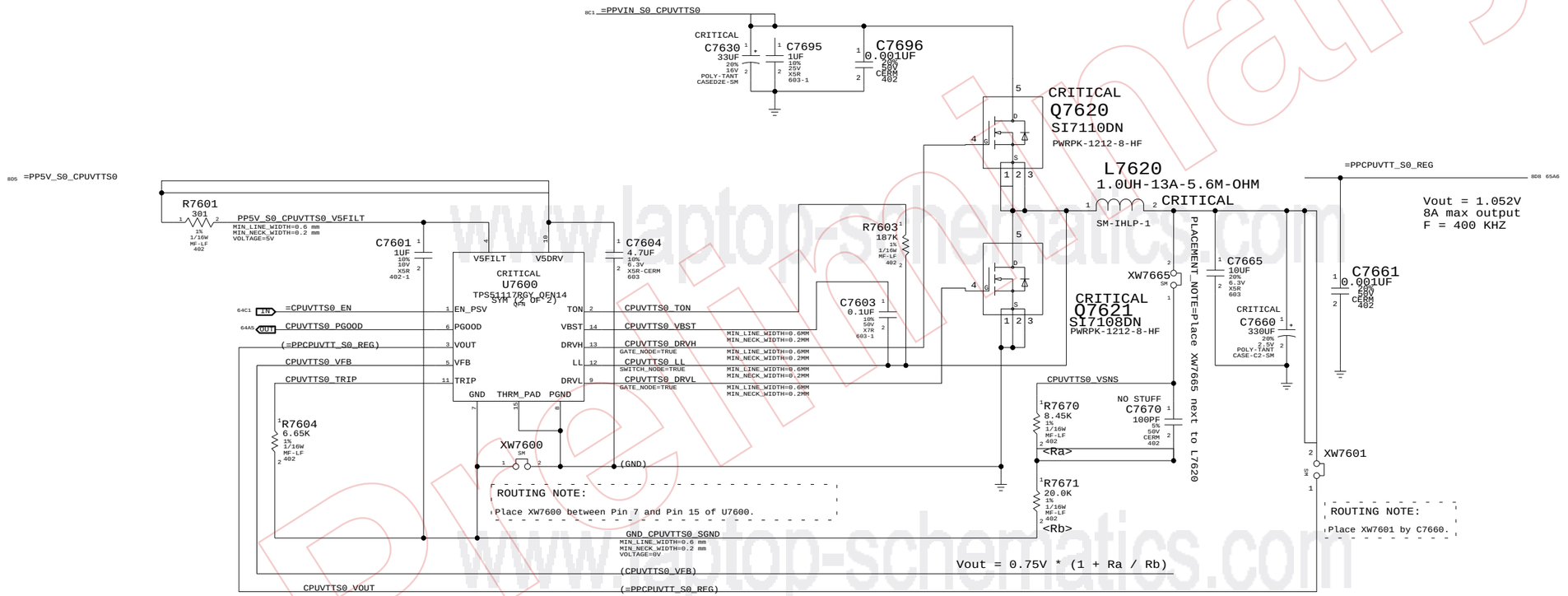
MCP VCORE REGULATOR

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 75 OF 109	

CPUVTT POWER SUPPLY



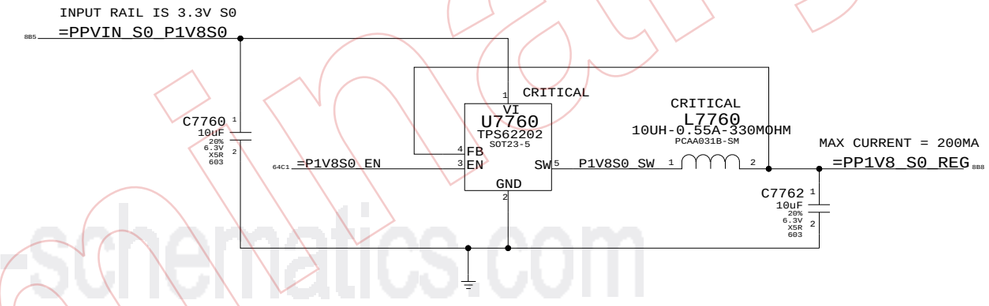
CPU VTT(1.05V) SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

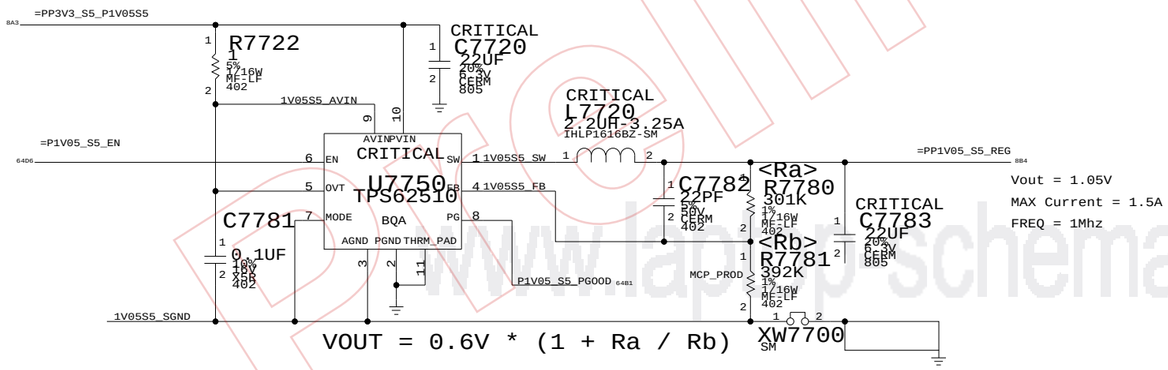
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 76 OF 109	

1.8V S0 SWITCHER



MCP 1.05V_S5 AUXC SUPPLY



MCP79 Rev A01 requires higher voltage

	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
VOUT = 1.102V	114S0464	1	RES,MTL FILM,1/16W,348K,1%,0402,SMD,LF	R7781		MCP_A01&MCP_A01P&MCP_A01Q

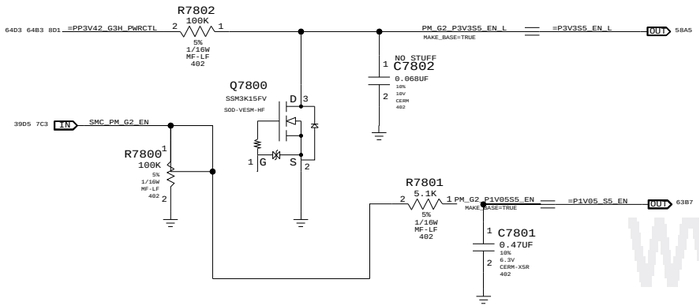
MISC POWER SUPPLIES

SYNC_MASTER=RAYMOND SYNC_DATE=01/23/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 77 OF 109	

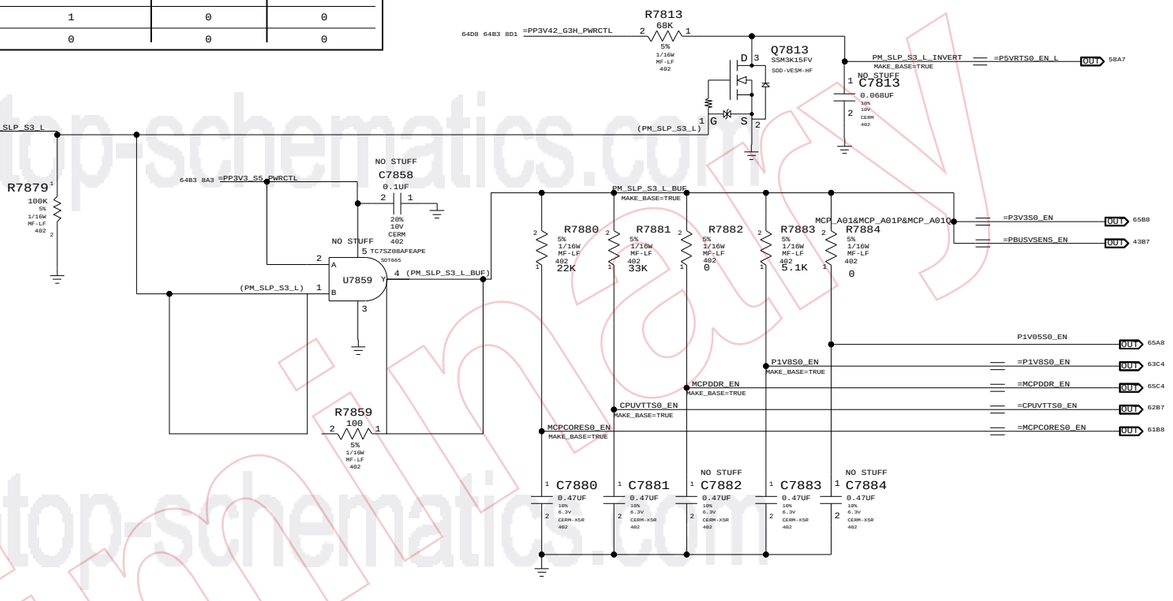
3.3V 1.05V S5 ENABLE



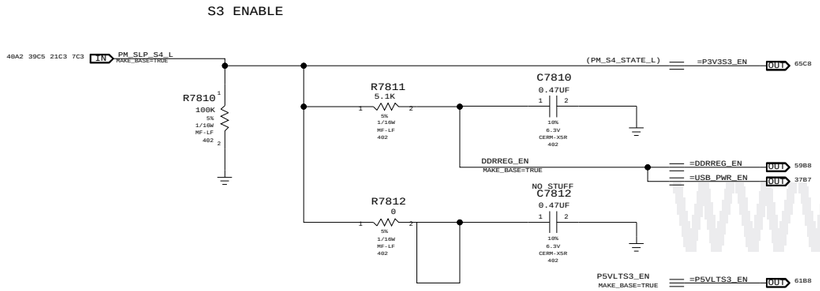
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

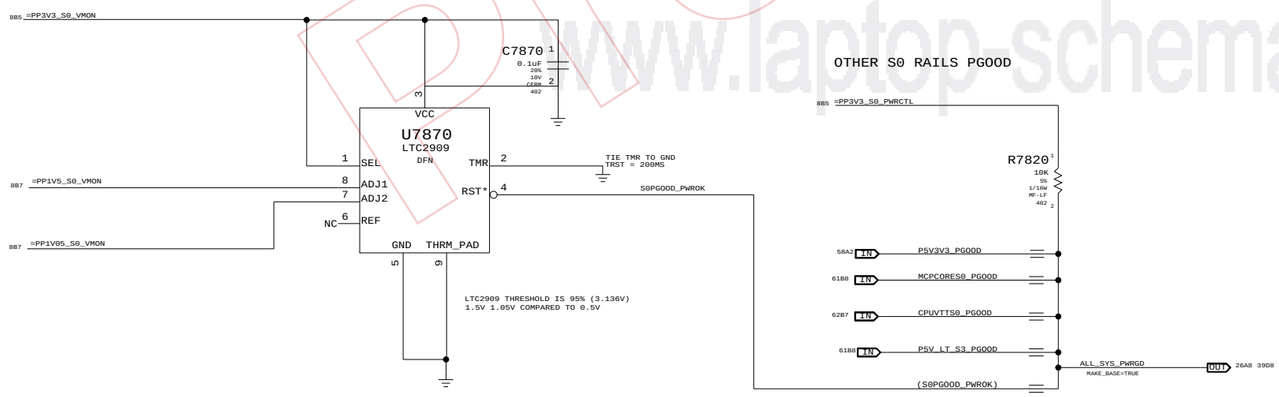
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



S3 ENABLE

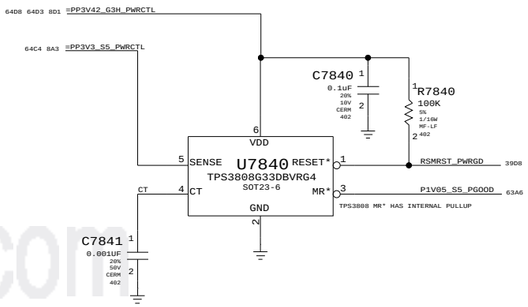


3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

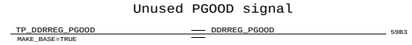


OTHER S0 RAILS PGOOD

VOLTAGE MONITOR



Unused PGOOD signal



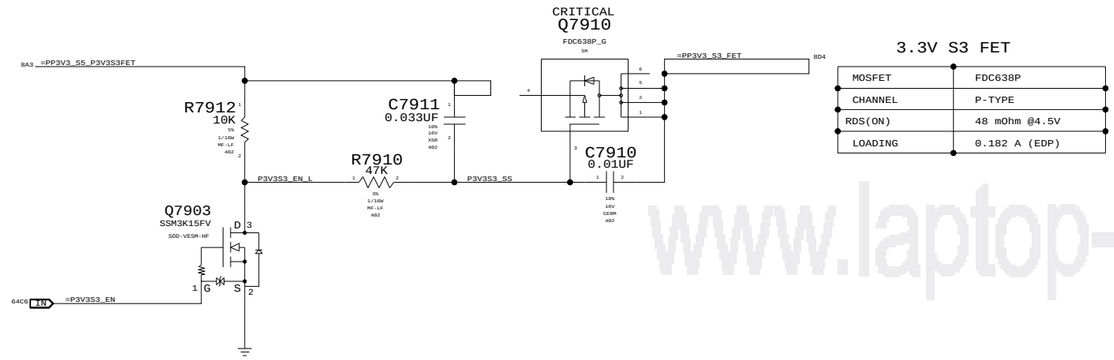
POWER SEQUENCING

SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

APPLE INC.

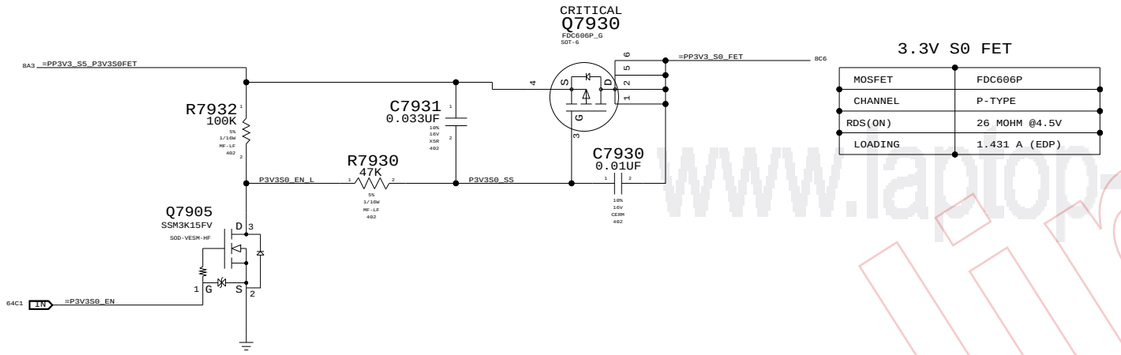
SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 78 OF 109	

3.3V S3 FET



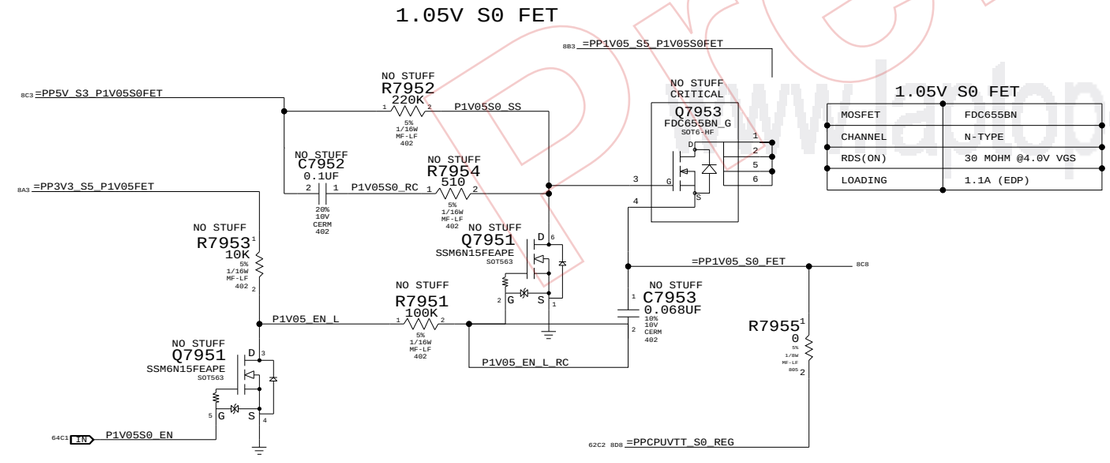
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

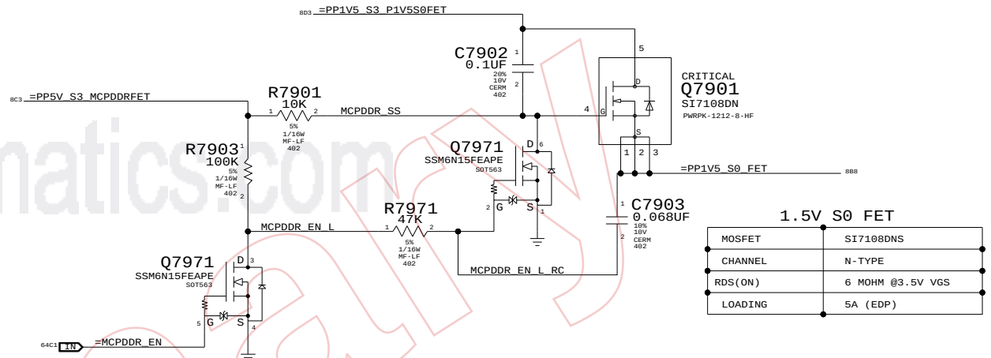
1.05V S0 FET



1.05V S0 FET	
MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	30 MOHM @4.0V VGS
LOADING	1.1A (EDP)

1.5V S0 FET

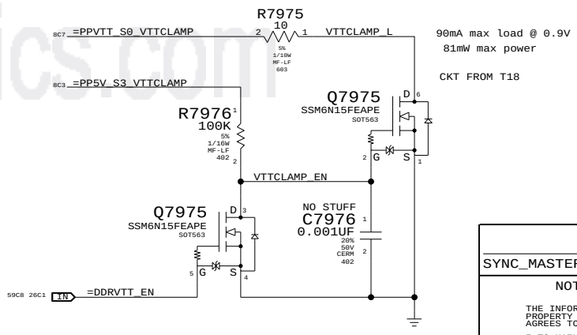
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.

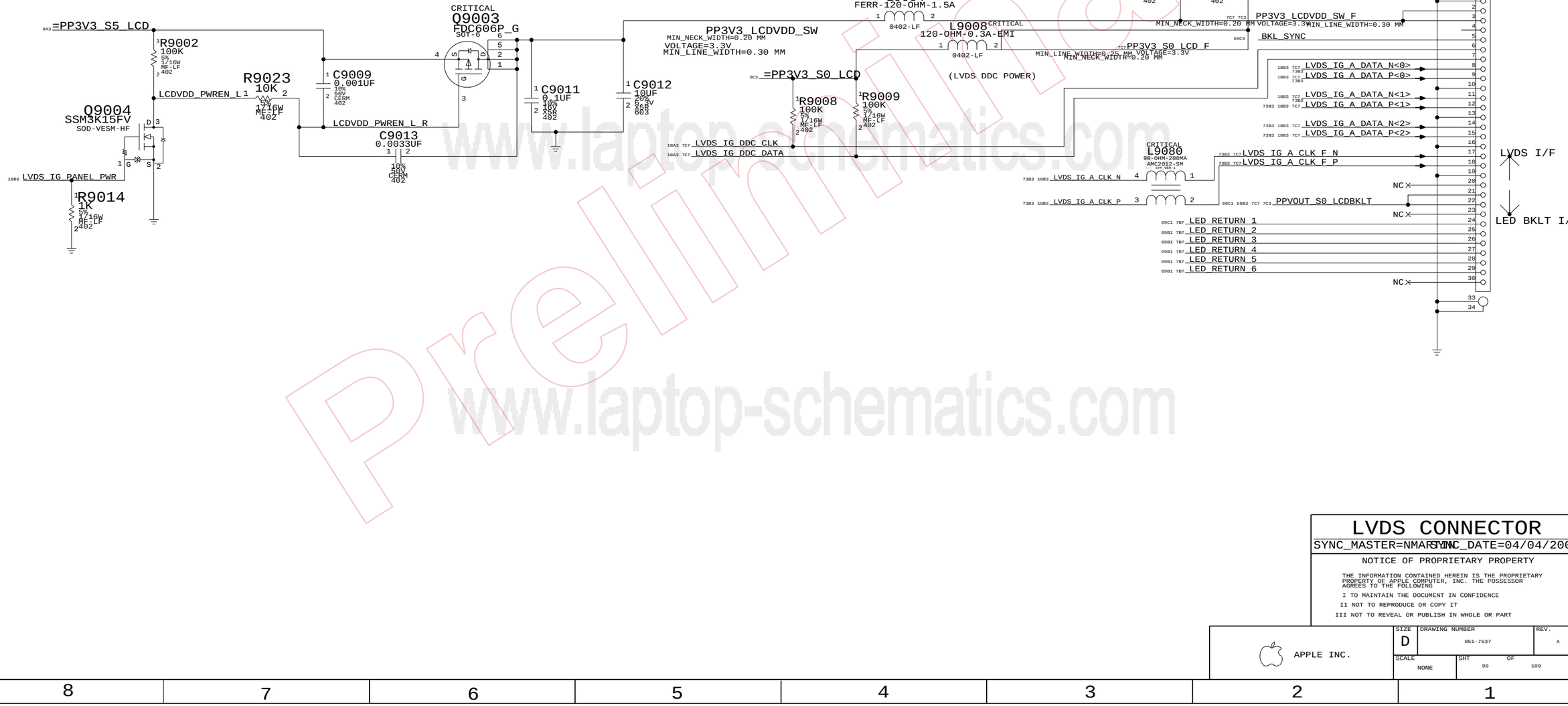


POWER FETS

SYNC_MASTER=YUAN.MA SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	79	109



LVDS CONNECTOR

SYNC_MASTER=NMARSYNC SYNC_DATE=04/04/2008

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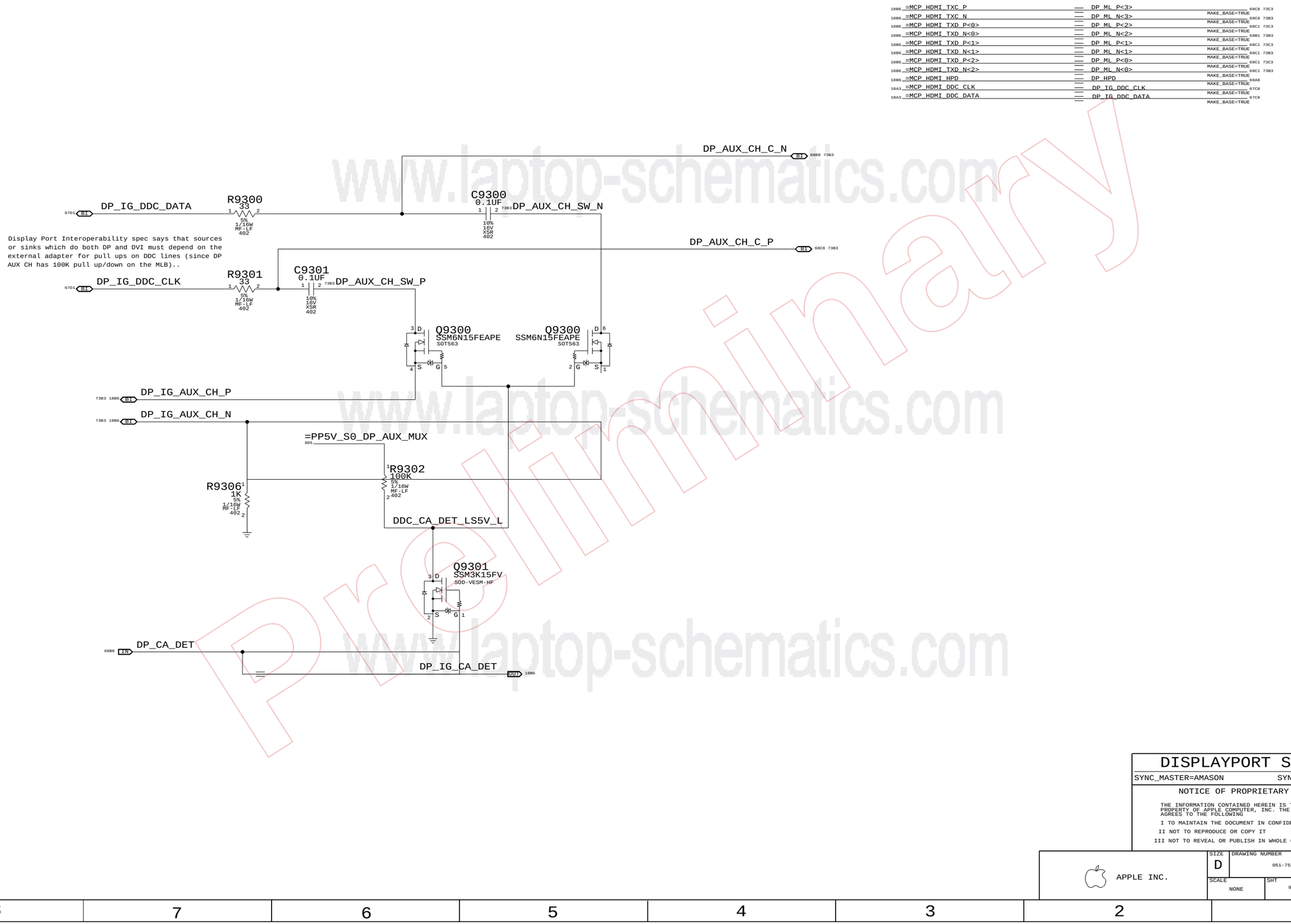
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 90 OF 109	



DISPLAYPORT SUPPORT

SYNC_MASTER=AMASON SYNC_DATE=04/18/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE NONE SHT 93 OF 109

Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
IN
OUT
EN
OC*
GND
TP_DPPWR_OC_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
C9480 10UF 20% 6.3V X5R 603
C9481 0.1UF 20% 16V CERM 402
NO STUFF
C9485 10UF 20% 6.3V X5R 603
CRITICAL
C9486 22UF 20% 6.3V X5R-CERM 603
L9400
FERR-120-OHM-3A
0603
C9400 0.01UF 10% 16V CERM 402
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
R9420 100K 5% 1/10W MF-LF 402

DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8
IO
NC
GND

R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402
R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402

FL9400
12-OHM-100MA
TCM1210-4SM
FL9401
12-OHM-100MA
TCM1210-4SM
FL9402
12-OHM-100MA
TCM1210-4SM

DP_ML_C_P<0> C9410 0.1uF DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1uF DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1uF DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1uF DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1uF DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1uF DP_ML_N<2>

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402

HDMI_CEC
R9425 1M 5% 1/10W MF-LF 402

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402
FL9403
12-OHM-100MA
TCM1210-4SM

DP_ML_P<3> C9414 0.1uF DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N

CRITICAL
J9400
DSPLYPRT-M97-2
F-RT-THSM
BOT ROW TH PINS
TOP ROW SM PINS
DP_HPD
DP_C_A_DET
HDMI_CEC
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
514-0610

DP_ML_CONN_P<3>
DP_ML_CONN_N<3>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

R9421 100K 5% 1/16W MF-LF 402
DP_ESD
CRITICAL
D9411
RCLAMP0524P
SLP2510P8

DP_ESD
CRITICAL
D9400
RCLAMP0504F
SC70-6-1

DP_ESD
CRITICAL
D9411
RCLAMP0524P
SLP2510P8

R9422 1M 5% 1/10W MF-LF 402
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD
R9446 100K 5% 1/16W MF-LF 402
MCP79 requires pull down HPD input with 100K if DP_HPD is used.
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/16W MF-LF 402
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

DisplayPort Connector

SYNC_MASTER=AMASON
SYNC_DATE=06/30/2008

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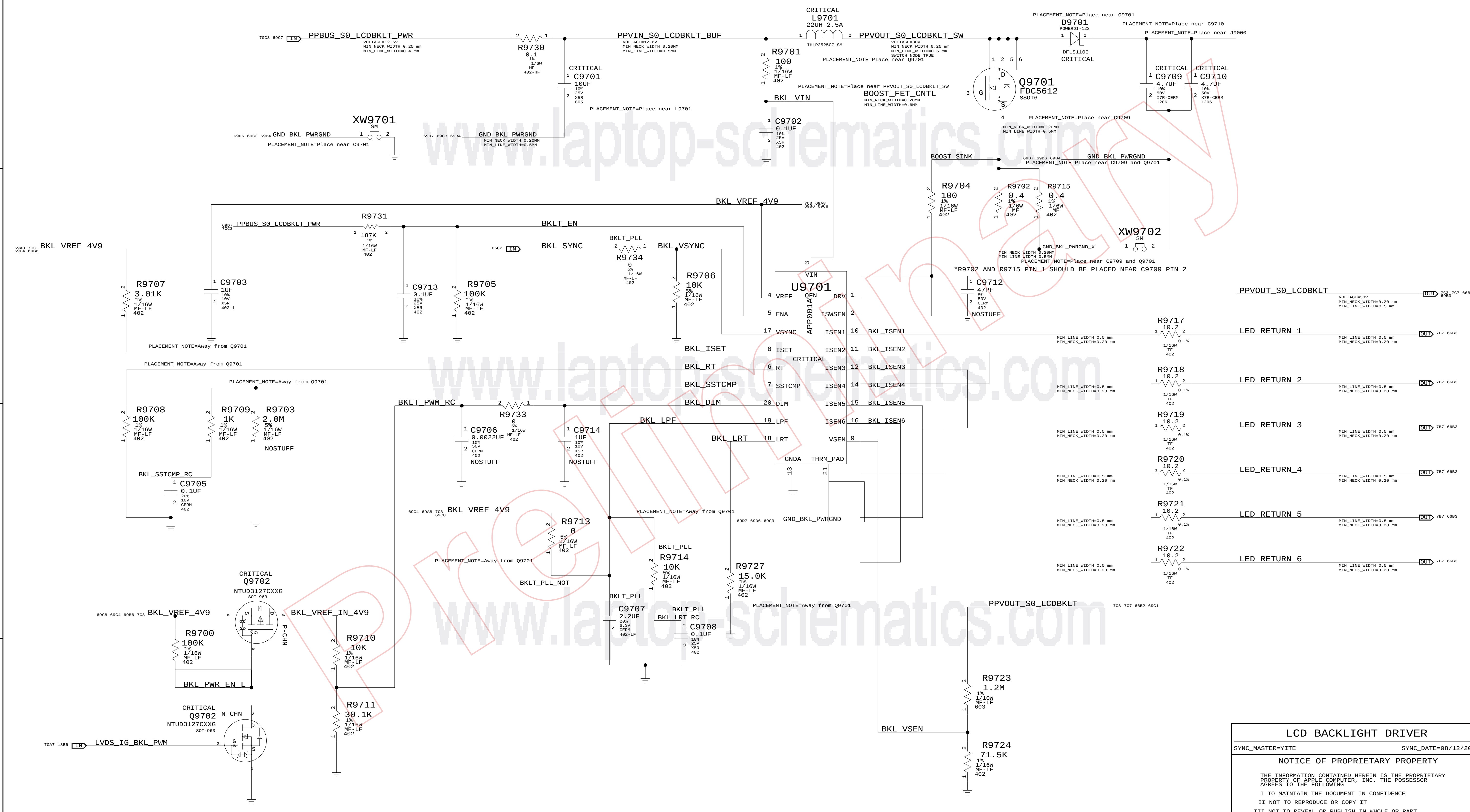
APPLE INC.
SIZE D
DRAWING NUMBER 051-7537
REV. A
SCALE NONE
SHT 94 OF 109

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.



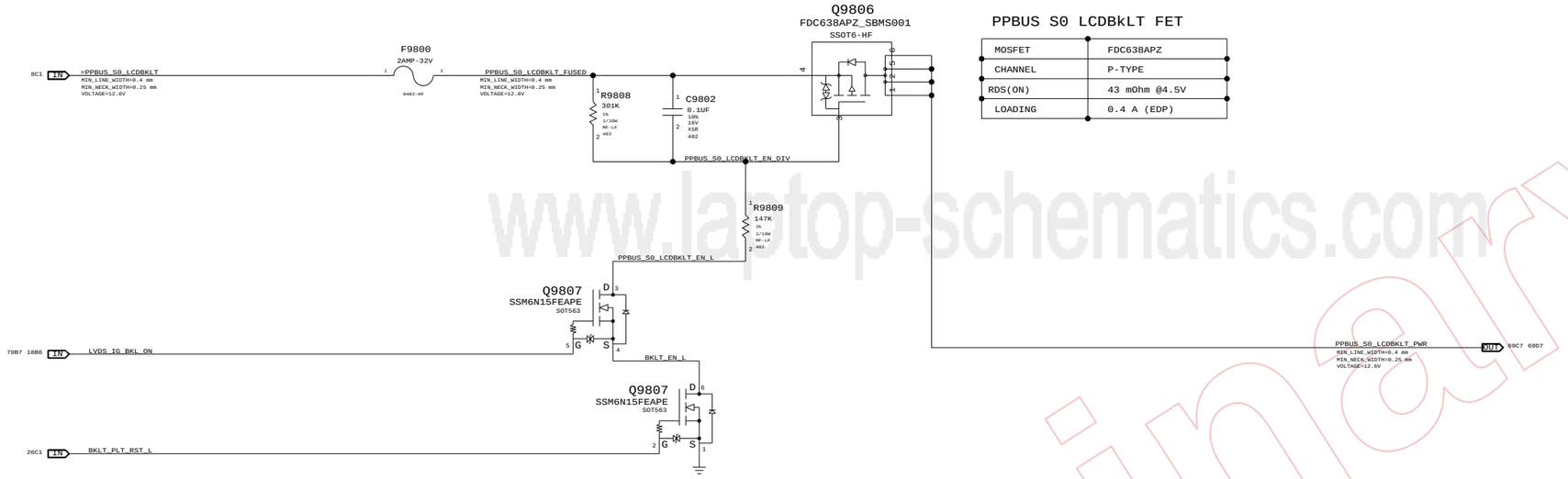
*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

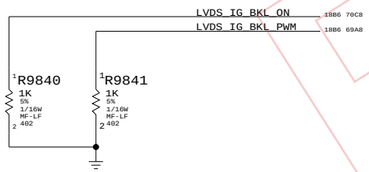
LCD BACKLIGHT DRIVER

SYNC_MASTER=YITE SYNC_DATE=08/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE NONE	SHT 97	OF 109





LCD Backlight Support

SYNC_MASTER=YITE SYNC_DATE=06/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 98 OF 109	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20557), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	10C4 14D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	10C4 14D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	10C4 14D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	10C4 14D6
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	10B4 10C4 14C3 14D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	10B4 14D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	10B4 14D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	10B4 14D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	10C2 14B3 14C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	10C2 14D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	10C2 14D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	10C2 14D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	10B2 10C2 14B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	10B2 14D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	10B2 14D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	10B2 14D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10D8 14C6 14D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10D8 14B6
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10D8 14B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10C8 14B6 14C6
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10C8 14B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	10D6 14B6
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9B2 10D6 14B6
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10D6 14B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10D6 14B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	10C6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	10C6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	10D6 14B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9B2 10D6 13B2 14A3
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10D6 14A6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10D6 14B6
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10C8 14A3
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9C2 10A4 10B4
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10C8 14B7
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10C8 14A3
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10D6 14A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9B2 10B8 14A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9B2 10B8 14A3
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10C5 14B6 40D4 60C8
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10B2 13C7 14A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10B8 14A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10B8 14A3
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10C6 14B7 40C4
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10A2 14A3
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10B2 14A3
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9B2 10B2 14A3 60C7
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10B2 14A3
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14A6
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10B6 14B3
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10B6 14B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13C3 14A3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13B3 14A3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14A4
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14A4
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21C7 60D8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	60C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10B4 27B1
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10B3
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6C6 10B6 10C6 13B3
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6C4 10B6 10C6
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6C6 6C7 10B6 10C6 13B3
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6C6 6C7 10A6 10C6 13B6
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6C6 6C7 10A6 10C6 13B3
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10C6 13C6
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10C5 13C6
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13B4
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	11B6 60C7
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11A5 60A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11A5 60A5
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

CPU/FSB Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 100 OF 109	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15B5 28C5 28C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15B5 28C5 28C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15A5 28D5 28D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15B5 28C5 28C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15A5 28C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15B5 15C5 28C5 28C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15C5 28C5 28C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15C5 28C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15C5 28C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15C5 28C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15B7 28C2 28C4 28D2 28D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15B7 28C2 28C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15B7 15C7 28B2 28B4 28C2 28C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15C7 28C2 28C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15C7 28B5 28B7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15C7 28B5 28B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15D7 28B5 28B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15D7 28A5 28A7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15A7 28C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15A7 28C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15A7 28B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15A7 28C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15A7 28B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15B7 28B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15B7 28B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15B7 28A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15D5 28C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15D5 28C2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15D5 28C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15D5 28C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15D5 28B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15D5 28B2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15D5 28C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15D5 28C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15D5 28B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15D5 28B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15D5 28B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15D5 28B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15D5 28B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15D5 28B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15D5 28A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15D5 28A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15B1 29C5 29C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15B1 29C5 29C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15A1 29D5 29D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15B1 29C5 29C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15A1 29C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15B1 15C1 29C5 29C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15C1 29C5 29C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15C1 29C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15C1 29C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15C1 29C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15B3 29C2 29C4 29D2 29D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15B3 29C2 29C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15B3 15C3 29C2 29C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15C3 29B2 29B4 29C2 29C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15C3 29B5 29B7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15C3 29B5 29B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15D3 29B5 29B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15D3 29A5 29A7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15A3 29C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15A3 29C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15A3 29C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15A3 29B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15A3 29B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15B3 29B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15B3 29B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15B3 29A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15D1 29C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15D1 29C2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15D1 29C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15D1 29C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15D1 29C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15D1 29C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15D1 29B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15D1 29B2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15D1 29B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15D1 29B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15D1 29B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15D1 29B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15D1 29B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15D1 29B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15D1 29A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15D1 29A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16C6

Memory Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE: NONE SHT: 101 OF 109

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7D5 31C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7D5 31C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17B3 31C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17B3 31C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7D5 17B6 31C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7D5 17B6 31C7
	PCIE_90D	PCIE	PCIE_FC_R2D_P	32C5
	PCIE_90D	PCIE	PCIE_FC_R2D_N	32C5
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	9B5 32C6
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	9B5 32C6
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	9B5 32B5
	PCIE_90D	PCIE	PCIE_FC_D2R_N	9B5 32B5
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17C3 31C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17C3 31C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7D5 31C8
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7D5 31C8
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	9B5 32C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	9B5 32C5
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	67D1 68C1 68C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	68C2 68C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	67D1 68B1 68C1 68C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	68B2 68C2 68C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18B6 67C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18B6 67B7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	67C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	67C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	67C4 68C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	67D4 68B8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18A6 25C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18A6 25C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18B3 66B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	7C7 66B2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18B3 66B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	7C7 66B2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	7C7 18B3 66C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	7C7 18B3 66C2
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	68C3 68C4 68C5
DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	68B3 68C3 68C4 68C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18A3 25C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18A3 25C6
SATA_HDD_R2D	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_R2D_P	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_R2D_N	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P	36A5
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N	36A5
SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA_HDD_D2R_P	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_D2R_N	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_P	36A5
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_N	36A5
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20D6 36C2
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20D6 36C2
	SATA_100D	SATA	SATA_ODD_R2D_P	7B7 36B5
	SATA_100D	SATA	SATA_ODD_R2D_N	7B7 7C5 36B5
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	36C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	36C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20D6 36B2
	SATA_100D	SATA	SATA_ODD_D2R_N	20D6 36B2
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7B7 36B5
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7B7 36B5
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	36B4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	36B4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20A6

MCP Constraints 1

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 102 OF 109	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13C3 19D7
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	19D2 19D7
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	19D2 19D7
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19C5
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19B3 39C8 41D3 41D5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19C3 39C8 41D5
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19B3 26D4
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19B3 26C4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	26C1 39C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	26B1 41D3
USB_EXTA	USB_90D	USB	USB_EXTA_P	20D3 37A8
	USB_90D	USB	USB_EXTA_N	20D3 37A8
	USB_90D	USB	USB_EXTA_MUXED_P	37C4
	USB_90D	USB	USB_EXTA_MUXED_N	37C4
	USB_90D	USB	CONN_USB_EXTA_P	37C3
	USB_90D	USB	CONN_USB_EXTA_N	37C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	20D3 31B5
	USB_90D	USB	USB_CAMERA_N	20D3 31B5
	USB_90D	USB	USB_CAMERA_CONN_P	7D5 31B7
	USB_90D	USB	USB_CAMERA_CONN_N	7D5 31B7
USB_BT	USB_90D	USB	USB_BT_P	20C3 31B5
	USB_90D	USB	USB_BT_N	20C3 31B5
	USB_90D	USB	CONN_USB2_BT_P	7C5 31B7
	USB_90D	USB	CONN_USB2_BT_N	7C5 31B7
USB_TPAD	USB_90D	USB	USB_TPAD_P	20D3 47B8
	USB_90D	USB	USB_TPAD_N	20D3 47B8
	USB_90D	USB	USB_TPAD_R_P	47B7
	USB_90D	USB	USB_TPAD_R_N	47B7
USB_IR	USB_90D	USB	USB_IR_P	20D3 38C7
	USB_90D	USB	USB_IR_N	20D3 38C7
USB_EXTB	USB_90D	USB	USB_EXTB_P	20C3 37A4
	USB_90D	USB	USB_EXTB_N	20C3 37A4
	USB_90D	USB	CONN_USB_EXTB_P	37A3
	USB_90D	USB	CONN_USB_EXTB_N	37A3
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20B4
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	13B6 21C3 42D8
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	13B6 21C3 42D8
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21C3 42C8
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21C3 42C8
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	21D2 51C7
	HDA_55S	HDA	HDA_BIT_CLK_R	21A7 21D4
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21C2 51C7
	HDA_55S	HDA	HDA_SYNC_R	21A7 21C4
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21A7 21D4
	HDA_55S	HDA	HDA_RST_L	21D2 51B7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21D7 51C7
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21D2 51C7
	HDA_55S	HDA	HDA_SDOUT_R	21A7 21D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21C7
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21B3 26B4
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26B1 39C5
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21B3 41A5 41C8
	SPI_55S	SPI	SPI_CLK	41A1 50C5
	SPI_55S	SPI	SPI_ALT_CLK	41C5 41D3
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21B3 41A5 41C7
	SPI_55S	SPI	SPI_MOSI	41B1 50C4
	SPI_55S	SPI	SPI_ALT_MOSI	41C5 41D5
SPI_MISO	SPI_55S	SPI	SPI_MISO	21B3 41A5 41B7
	SPI_55S	SPI	SPI_MISO_R	50C4
	SPI_55S	SPI	SPI_ALT_MISO	41B5 41D5
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21B3 41B7
	SPI_55S	SPI	SPI_CS0_L	
	SPI_55S	SPI	SPI_CS1_R_L	
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB	41B2

MCP Constraints 2

SYNC_MASTER=T18_MLB SYNC_DATE=12/14/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE: NONE SHT 103 OF 109

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18C3 34A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	33B6 34A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18C3 33B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18C3 33B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	33C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18D6 33C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	33B4 33C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18D6 33C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18D6 33B1 33C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18D6 33B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	33B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	33C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18D3 33C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18D3 33C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18D3 33B6 33C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18C3 33B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18C3 33B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	33B3 35B7 35C7
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	33B3 35B7 35C7
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	35B4 35C4 35C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	35B4 35C4 35C5

Ethernet Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=03/19/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE NONE SHT 104 OF 109

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S5	SMB	SMBUS_SMC_A_S3_SCL	7B5 7D5 42D2
SMBUS_SMC_A_S3_SDA	SMB_5S5	SMB	SMBUS_SMC_A_S3_SDA	7B5 7C5 42D2
SMBUS_SMC_B_S0_SCL	SMB_5S5	SMB	SMBUS_SMC_B_S0_SCL	42C2
SMBUS_SMC_B_S0_SDA	SMB_5S5	SMB	SMBUS_SMC_B_S0_SDA	42C2
SMBUS_SMC_0_S0_SCL	SMB_5S5	SMB	SMBUS_SMC_0_S0_SCL	42D5
SMBUS_SMC_0_S0_SDA	SMB_5S5	SMB	SMBUS_SMC_0_S0_SDA	42D5
SMBUS_SMC_BSA_SCL	SMB_5S5	SMB	SMBUS_SMC_BSA_SCL	7A7 42C5
SMBUS_SMC_BSA_SDA	SMB_5S5	SMB	SMBUS_SMC_BSA_SDA	42C5
SMBUS_SMC_MGMT_SCL	SMB_5S5	SMB	SMBUS_SMC_MGMT_SCL	42B5
SMBUS_SMC_MGMT_SDA	SMB_5S5	SMB	SMBUS_SMC_MGMT_SDA	42B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SMC Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 106 OF 109	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

M97 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR		CHGR_CSO_R_P	44A8 57B3
	DIFFPAIR		CHGR_CSO_R_N	44A8 57B3
	DIFFPAIR		CPUTHMSNS_D2_P	45C5
	DIFFPAIR		CPUTHMSNS_D2_N	45C5
	DIFFPAIR		CPU_THERMD_P	10C6 45D5
	DIFFPAIR		CPU_THERMD_N	10C6 45D5
	DIFFPAIR		ISNS_CPUVTT_P	44B7
	DIFFPAIR		ISNS_CPUVTT_N	44B7
	DIFFPAIR		ISNS_P1V5S0MCP_P	44C7
	DIFFPAIR		ISNS_P1V5S0MCP_N	44C7
	DIFFPAIR		ISNS_PVCORES0MCP_P	44D8
	DIFFPAIR		ISNS_PVCORES0MCP_N	44D8 61C4
	DIFFPAIR		MCPTHMSNS_D2_P	7C7 45B5
	DIFFPAIR		MCPTHMSNS_D2_N	7C7 45B5
	DIFFPAIR		MCP_THMDIODE_P	21C3 45C5
	DIFFPAIR		MCP_THMDIODE_N	21C3 45B5

M97 SPECIAL CONSTRAINTS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE: NONE	SHT 107 OF 109	

M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3,ISL4,ISL9,ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

M97 RULE DEFINITIONS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A

SCALE	SHT	OF
NONE	109	109