

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, MBP17

PVT 12/18/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
0.1		521911	Proto Release	?	?
				DATE	DATE

Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	(MASTER)	(MASTER)
3	Power Block Diagram	(MASTER)	(MASTER)
4	Power Block Diagram	N/A	N/A
5	BOM Configuration	N/A	N/A
6	Revision History	N/A	N/A
7	Functional / ICT Test	MASTER	MASTER
8	Power Aliases	(MASTER)	(MASTER)
9	Signal Aliases	MASTER	MASTER
10	CPU FSB	M87_MLB	08/28/2007
11	CPU Power & Ground	M87_MLB	08/28/2007
12	CPU Decoupling & VID	M87_MLB	08/28/2007
13	eXtended Debug Port (XDP)	T9_NOME	01/22/2007
14	NB CPU Interface	T9_NOME	01/25/2007
15	NB PEG / Video Interfaces	T9_NOME	03/19/2007
16	NB Misc Interfaces	T9_NOME	01/25/2007
17	NB DDR2 Interfaces	T9_NOME	01/25/2007
18	NB Power 1	T9_NOME	01/25/2007
19	NB Power 2	T9_NOME	01/25/2007
20	NB Grounds	T9_NOME	01/25/2007
21	NB Standard Decoupling	MASTER	MASTER
22	NB Graphics Decoupling	M87_MLB	08/28/2007
23	SB Enet, Disk, FSB, LPC	T9_NOME	01/25/2007
24	SB PCI, PCIE, DMI, USB	M87_MLB	08/28/2007
25	SB Pwr Mgt, GPIO, Clink	M87_MLB	08/28/2007
26	SB Power & Ground	T9_NOME	01/25/2007
27	SB Decoupling	MASTER	MASTER
28	SB Misc	M87_MLB	08/28/2007
29	Clock (CK505)	T9_NOME	01/25/2007
30	Clock Termination	M87_MLB	08/28/2007
31	DDR2 SO-DIMM Connector A	M87_MLB	08/28/2007
32	DDR2 SO-DIMM Connector B	M87_MLB	08/28/2007
33	Memory Active Termination	(MASTER)	(MASTER)
34	Left I/O Board Connector	(MASTER)	(MASTER)
35	Ethernet (Yukon)	T9_NOME	01/25/2007
36	Yukon Power Control	T9_NOME	03/19/2007
37	Ethernet Connector	M87_MLB	08/28/2007
38	FireWire Link (TSB83AA22)	M87_MLB	08/28/2007
39	FireWire PHY (TSB83AA22)	M87_MLB	08/28/2007
40	FireWire Port Power	M87_MLB	08/28/2007
41	FireWire Ports	M87_MLB	08/28/2007
42	PATA Connector	MASTER	MASTER
43	External USB Connector	MASTER	MASTER
44	Left Clutch Barrel Interconnect	M87_MLB	08/28/2007
45	SMC	M87_MLB	08/28/2007

Page	Contents	Sync	Date
46	SMC Support	M87_MLB	10/15/2007
47	LPC+ Debug Connector	M87_MLB	08/28/2007
48	SMBus Connections	(MASTER)	(MASTER)
49	Current & Voltage Sensing	M87_MLB	08/28/2007
50	Current Sensing	MASTER	MASTER
51	Thermal Sensors	M87_MLB	08/28/2007
52	Fan Connectors	M87_MLB	08/28/2007
53	Current & Thermal Sensors	M87_LIO	11/06/2007
54	ALS Support	M87_MLB	08/28/2007
55	Sudden Motion Sensor (SMS)	M87_MLB	08/28/2007
56	SPI BootROM	T9_NOME	01/25/2007
57	DC-In & Battery Connectors	(MASTER)	(MASTER)
58	Power FETs	M87_MLB	08/28/2007
59	IMVP6 CPU VCore Regulator	MASTER	MASTER
60	5V / 3.3V Power Supply	MASTER	MASTER
61	1.25V / 1.05V Power Supply	M87_MLB	08/28/2007
62	1.8V DDR2 Supply	M87_MLB	08/28/2007
63	1.5V Power Supply	MASTER	MASTER
64	FW PHY Power Supplies	M87_MLB	08/28/2007
65	3.425V G3Hot Supply & Power Control	M87_MLB	09/26/2007
66	PBus Supply & Batt. Charger	MASTER	MASTER
67	NV G84M PCI-E	M87_MLB	08/28/2007
68	NV G84M Core/FB Power	M87_MLB	08/28/2007
69	NV G84M Frame Buffer I/F	M87_MLB	08/28/2007
70	GDDR3 Frame Buffer A (Top)	M87_MLB	08/28/2007
71	GDDR3 Frame Buffer B (Top)	M87_MLB	08/28/2007
72	NV G84M GPIO/MIO/Misc	M87_MLB	08/28/2007
73	GPU Straps	M87_MLB	08/28/2007
74	NV G84M Video Interfaces	M87_MLB	08/28/2007
75	GPU (G84M) Core Supply	M87_MLB	09/26/2007
76	LVDS Display Connector	MASTER	MASTER
77	GDDR3 Frame Buffer A (Bot)	M87_MLB	08/28/2007
78	GDDR3 Frame Buffer B (Bot)	M87_MLB	08/28/2007
79	1.8V FB Power Supply	MASTER	MASTER
80	DVI Display Connector	MASTER	MASTER
81	Project Specific Connectors	(MASTER)	(MASTER)
82	LCD Backlight Support	M87_LIO	12/06/2007
83	CPU/FSB Constraints	T9_NOME	01/25/2007
84	NB Constraints	T9_NOME	01/25/2007
85	Memory Constraints	T9_NOME	01/25/2007
86	SB Constraints (1 of 2)	T9_NOME	01/25/2007
87	SB Constraints (2 of 2)	T9_NOME	01/25/2007
88	Clock & SMC Constraints	M87_MLB	08/28/2007
89	FireWire Constraints	T9_NOME	01/25/2007

Page	Contents	Sync	Date
90	GPU (G84M) Constraints	M87_MLB	10/02/2007
91	Project Specific Constraints	M87_MLB	08/28/2007
92	PCB Rule Definitions	M87_MLB	10/03/2007

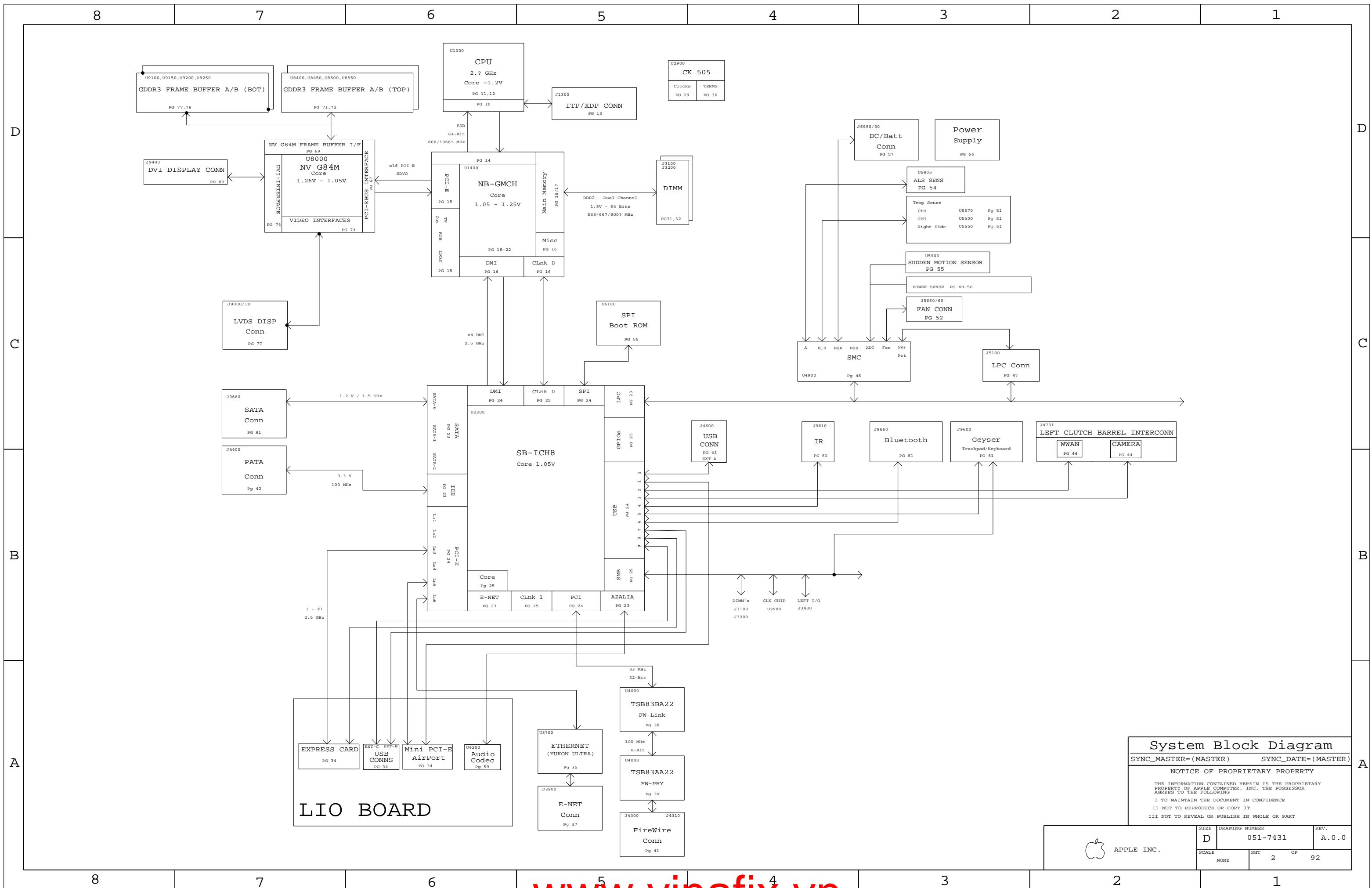
ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7431	1	SCHEM, MLB, MBP17	SCH	CRITICAL	
820-2262	1	PCBFB, MLB, MBP17	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST MODIFIED=Tue Dec 18 15:43:01 2007

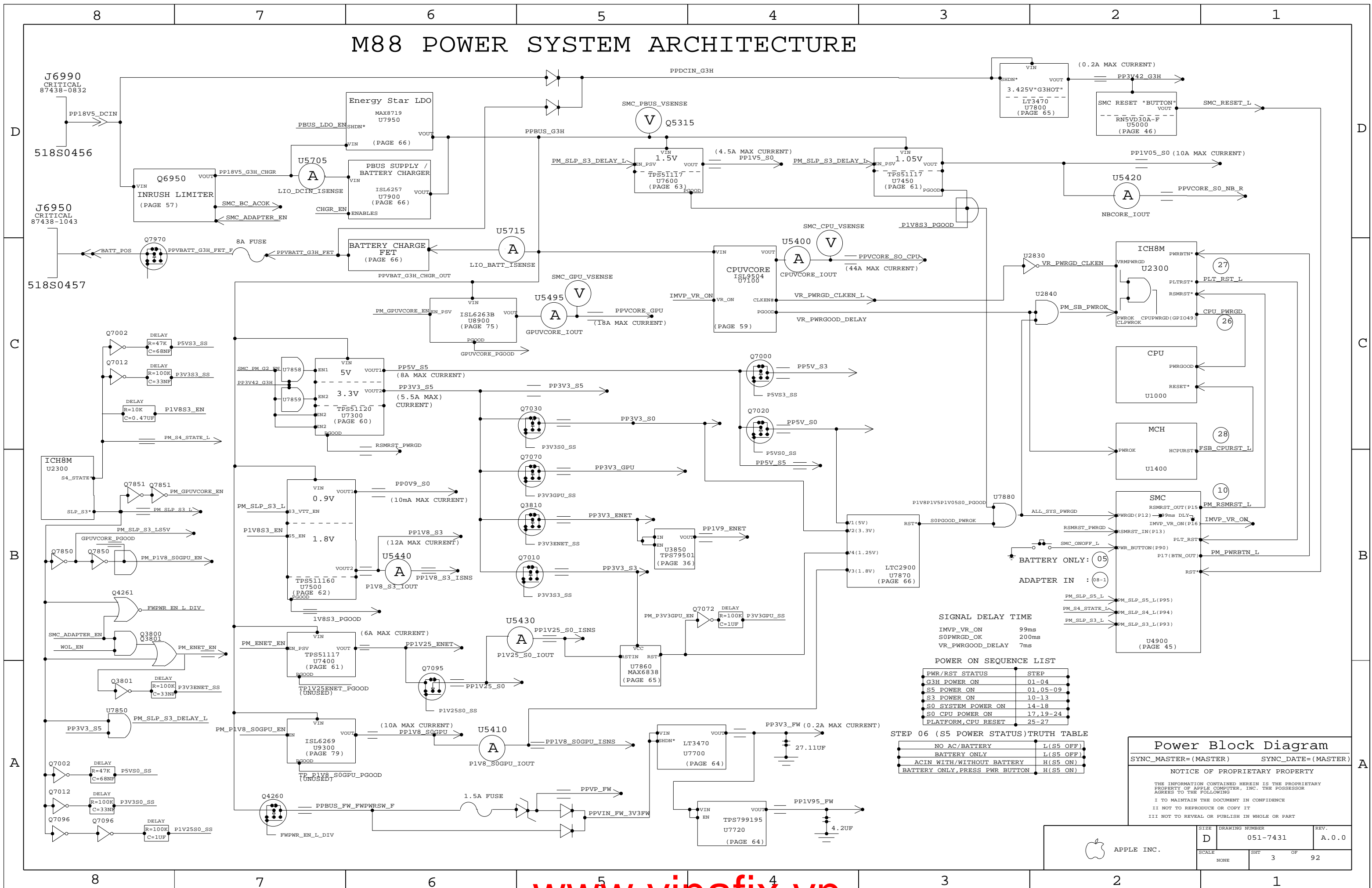
DIMENSIONS ARE IN MILLIMETERS		METRIC		APPLE INC.	
XX :	_____	DRAPFER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	
		DRAWING NUMBER		REV. A.0.0	
				SHT 1 OF 92	



System Block Diagram
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	2	92	

M88 POWER SYSTEM ARCHITECTURE

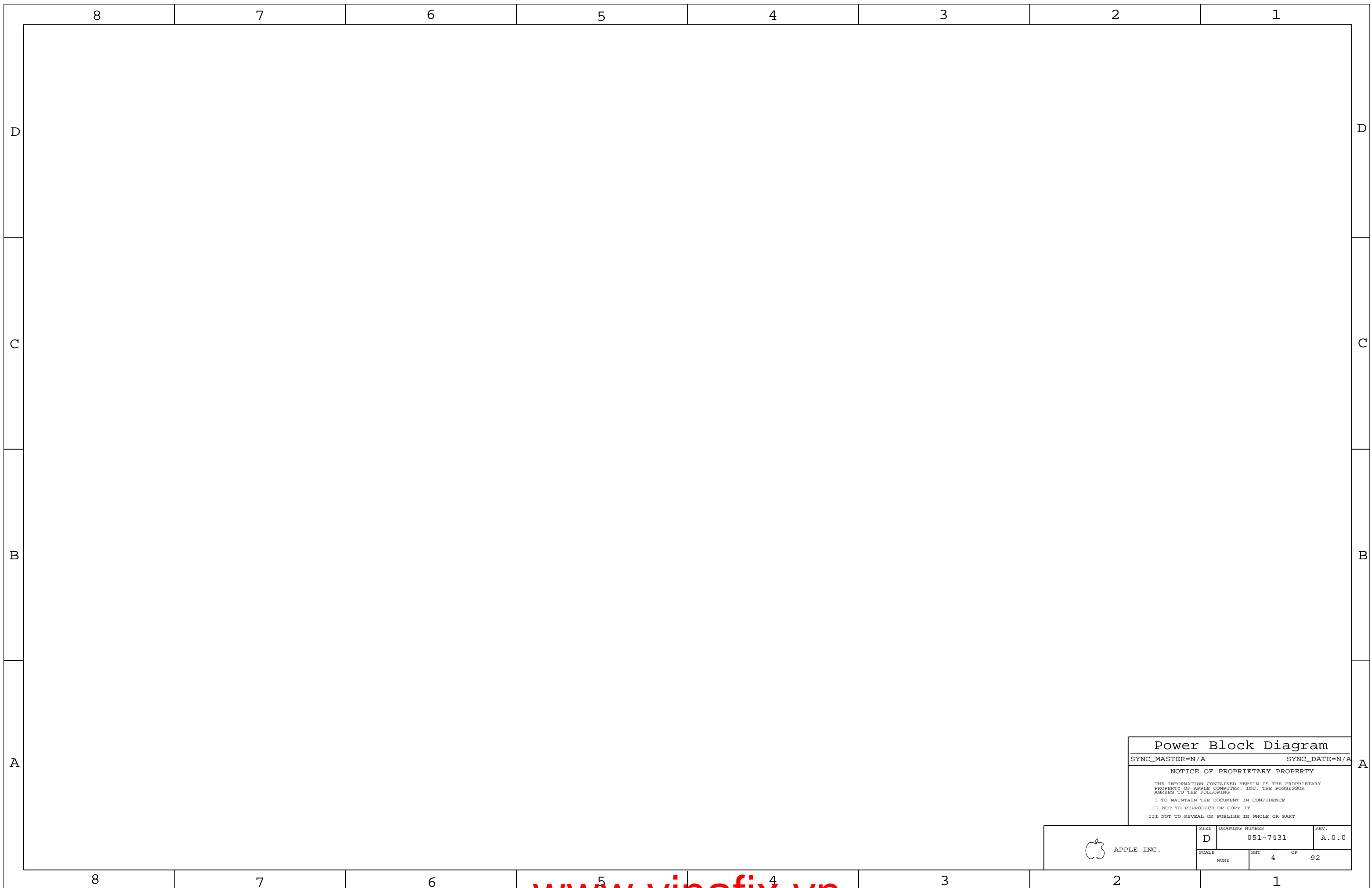


Power Block Diagram
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D	051-7431	A.0.0
SCALE	SHT	OF
NONE	3	92



Power Block Diagram

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	D	051-7431	A.0.0
SCALE		SHT	OF
NONE		4	92

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9092	PCBA, 2.6GHZ, 512VRAM-HY, M88	M88_COMMON, CPU_2_6GHZ, FB_512_HYNIX, EEE_Z3K
630-9093	PCBA, 2.6GHZ, 512VRAM-SAM, M88	M88_COMMON, CPU_2_6GHZ, FB_512_SAMSUNG, EEE_Z3L
630-9225	PCBA, 2.5GHZ, 512VRAM-HY, M88	M88_COMMON, CPU_2_5GHZ, FB_512_HYNIX, EEE_ZVW
630-9228	PCBA, 2.5GHZ, 512VRAM-SAM, M88	M88_COMMON, CPU_2_5GHZ, FB_512_SAMSUNG, EEE_ZVX

BOM Groups

BOM GROUP	BOM OPTIONS
M88_COMMON	COMMON, ALTERNATE, M88_COMMON1, M88_COMMON2, M88_DEBUG, M88_PROGPARTS
M88_COMMON1	BKLT_5V_PWR, ISL9504B, ONEWIRE_PU, GPUVID_1P23V
M88_COMMON2	PLV8S3_1V8, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN
M88_DEBUG	SMC_DEBUG_NO, XDP, LPCPLUS
M88_PROGPARTS	BOOTROM_PROG, SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4, VRAM_16M, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4, VRAM_16M, VRAM_HYNIX, VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM8, VRAM_16M, VRAM_SAMSUNG, VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM8, VRAM_16M, VRAM_HYNIX, VRAM_512_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3K]	CRITICAL	EEE_Z3K
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3L]	CRITICAL	EEE_Z3L
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:ZVW]	CRITICAL	EEE_ZVW
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:ZVX]	CRITICAL	EEE_ZVX

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3559	1	IC, PDC, SR, PRQ, 2.6G, 35W, 800FSB, 6M, BGA	U1000	CRITICAL	CPU_2_6GHZ
337S3560	1	IC, PDC, SR, PRQ, 2.5G, 35W, 800FSB, 6M, BGA	U1000	CRITICAL	CPU_2_5GHZ
338S0509	1	IC, GPU, NV, G84M, BGA	U8000	CRITICAL	
338S0432	1	IC, NB, CRESTLINE, GM, CO, PRQ, ROHS-SPECIAL, 965PM	U1400	CRITICAL	
338S0434	1	IC, SB, ICH8M, BL, PRQ, BGA	U2300	CRITICAL	
353S1651	1	IC, ISL9504B, 2PH IMVP6 REG, PMON, QFN48	U7100	CRITICAL	ISL9504B
359S0130	1	IC, SLG2AP101, LW PWR CLK GEN, CK505, QFN68	U2900	CRITICAL	
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	

338S0274	1	IC, SMC, HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2194	1	IC, SMC, DEVELOPMENT, M88	U4900	CRITICAL	SMC_PROG
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2192	1	IC, EFI ROM, DEVELOPMENT, M87	U6100	CRITICAL	BOOTROM_PROG

333S0423	4	IC, SGRAM, GDDR3, 16MX32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0423	8	IC, SGRAM, GDDR3, 16MX32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_SAMSUNG
333S0424	4	IC, SGRAM, GDDR3, 16MX32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX
333S0424	8	IC, SGRAM, GDDR3, 16MX32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_HYNIX

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	See alt to TCM/BTech magazine
138S0603	138S0602		ALL	Match alt to memory 256M module spec
353S1681	353S1294		ALL	SI alternate to BCL1041
376S0543	376S0466		ALL	See alternate to BCL1041 B1462
152S0683	152S0276		ALL	See legacy alternate to BCL1041
104S0024	104S0017		ALL	Alternate alternate to Option
128S0083	128S0165		ALL	alternate to legacy from Range 104P 12.1mm
128S0113	128S0160		ALL	alternate to legacy from Range 104P 12.1mm
128S0115	128S0150		ALL	alternate to legacy from Range 104P 12.1mm
128S0122	128S0157		ALL	alternate to legacy from Range 104P 12.1mm
128S0057	128S0147		ALL	alternate to legacy from Range 104P 12.1mm
128S0056	128S0175		ALL	alternate to legacy from Range 104P 12.1mm
376S0448	376S0445		ALL	DIFFERENTIAL FOR PWB200

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	5	92

Proto:

See earlier schematics for info about releases 0.0.1 - 4.0.0

EVT:

5.0.0:
08/03/07 -- Page 5: Removed Q4690 BOM table entry. BOM table is on CSA pg. 46
6.0.0 & 5.1.0:
08/10/07 -- Synced to M87 MLB label 4.3.0
08/10/07 -- Page 3: Revised power block diagram.
08/10/07 -- Page 10-12: Updated U1000 CPU part number to reflect latest Penryn pin-out.
08/10/07 -- Page 37: T3900,T3901 magnetics changed to 157S0053.
08/10/07 -- Page 65: Changed L7810 3.425V G3 Hot inductor to 152S0301. R7070 changed from 100K to 10K.
6.1.0:
08/14/07 -- Synced to M87 MLB label 5.1.0
08/14/07 -- Page 49: Changed Q5322 to SOT23 part same as M87.
08/14/07 -- Page 75: Changed GPU VID pull up/downs to 2.2K ohms.
6.2.0:
08/16/07 -- Removed Rev B Silego clock chip as alternate.
08/16/07 -- Page 51: Temp Sensors: Changed U5500 and U5570 to EMC1043-1 APN 353S1947.
7.0.0:
08/17/07 -- Page 48: Changed SMBus SMC "A" pull ups R5270 and R5271 to 3.3K to improve rise time on SCL..
7.1.0:
08/22/07 -- Page. 9,34: Added GPIOs to support iPhone headset. ICH8 GPIO 22 IPHS_SW_BIAS_EN_L routes to JJ3400.63
08/22/07 -- Page. 9,34: Removed R3410 and R3411. ICH8 GPIO 2 IPHS_SW_INT routes to JJ3400.65
08/22/07 -- Synced M87 MLB label 6.2.0
08/22/07 -- Page 51: Temp sensors: Added R5501,R5502,R5571,R5572 pull ups on U5500 and U5570.
08/22/07 -- Page 61: R7455 changed to 7.5K to change max load current margin on PPIV05.
08/22/07 -- Page 90: Changed frame buffer net physical type to GDDR3_50SE.
08/22/07 -- Synced M87 LIO label 1.5.0
08/22/07 -- Page 66: U7901 voltage follower changed from OPA333 to OPA705.
08/22/07 -- Page 82: Changed L9891,L9893,L9894 to 155S0220
7.2.0:
08/23/07 -- Page 5: Changed CPU parts to ES2, B1 for EVT
08/23/07 -- Page 9: IPHS_SW_BIAS_EN_L now connected to SB_SLOAD (GPIO 38).
08/23/07 -- Synced M87 MLB label 6.5.0
08/23/07 -- Page 50: Current Sensors: Changed U5410 and U5440 to MAX4245 Changed R5413 and R5443 to 0.005 ohm resistors.
08/23/07 -- Page 91: Added diff pair properties to new current sensor pairs.
08/23/07 -- Synced M87 LIO label 1.7.0
08/23/07 -- Page 66: Changed U7901 to MAX4245. Changed F7902 to 740S0055.
08/23/07 -- Page 82: Add BOMOPTION OMIT to RX9892.
8.0.0:
08/24/07 -- Page 25: Added NO STUFF to R2552 (was pull up on SB GPIO38 which is now used on IPHS).
08/24/07 -- Page 59: CPU Vcore supply changes per characterization Changed L7100 and L7101 to 152S0624. Changed C7134 to 0.01uF 132S0042.
8.1.0:
08/24/07 -- Synced M87 MLB label 8.2.0
Page 5,75: Changed BOM option to GPUVID_LP23V
Page 73: Changed R5491 and R5493 to 6.81K to allow full resolution of GPUVCORE current sense
Page 50: Adding C5411,C5412,C5441,C5442 feedback caps for current sense op amps
Page 66: Changed R7920 to halogen free 107S0110.
8.2.0:
08/29/07 -- Synced m87_mlb CSA pgs. Major release label name : m87_mlb_051-7413_8.2.0
08/29/07 -- Changed net physical and net spacing to CRT_50S on these signals NB_CLK100M_DPLSS_P/N NB_CLK96M_DOT_P/N
8.3.0:
08/29/07 -- Changed the following filters to 155S0371 for supply issues: pg. 43 L4600 pg. 44 FL4735 pg. 76 L9010,L9011
08/29/07 -- pg. 80 L9460,L9464,L9468,L9476,L9480,L9484
8.4.0:
08/30/07 -- Changed the orientation on these filters to match layout: pg. 43 L4600 pg. 76 L9010,L9011
9.0.0:
08/30/07 -- RFA 529050 EVT Release of Schematic BOM and PCBF
9.1.0:
BOM Changes only
09/04/07 -- Page 5: Added alternate sources for these parts:
09/04/07 -- 152S0683 is the Mag layers alternate for Dale/Vishay inductors.
09/04/07 -- 128S0164 is the Kemet alternate to Sanyo caps
09/04/07 -- 104S0023 is the Panasonic alternate to Cynotec resistors
09/04/07 -- Page 50: Changed R5425 and R5435 to 104S0023.
10.0.0:
09/06/07 -- HF capacitor substitution, with halogen parts as alternates. pg. 5 Alternates BOM table updates.
11.0.0:
09/11/07 -- Page 57: Removed NO STUFF from DZ6960 (377S0044), ESD diode on BATT_POS per Chris.
09/11/07 -- Page 5: Removed alternate to 128S0164 Kemet 220uF tantalum cap at C7540 and C7541.
09/11/07 -- Added BOM variants and EEE codes for 2.5GHz:
09/11/07 -- 630-9225: ZVW PCBA,2.5GHZ,512VRAM-HY,M88
09/11/07 -- 630-9228: ZVX PCBA,2.5GHZ,512VRAM-SAM,M88
09/11/07 -- Page 62: Removed OMIT property and BOM option table to make C7540 and C7541 only 128S0073.
09/11/07 -- Page 82: LCD Backlight Added OMIT properties and BOM option table to change these beads to 155S0220: L9891,L9893,L9894

DVT:

11.1.0:
09/12/07 --Page 66: Swapped U7901 pins 1 and 3 signals (positive and negative inputs).
11.2.0:
09/26/07 -- Synced M* & MLB label 10.2.0
09/26/07 -- Page 50 & 75: GPUVCORE: Current sense to use IMVP6 IMON + Non-inverting Opamp removed R8992,C8992
09/26/07 -- Page 65: Changed C7860 to 0.0047uF (radar://5468257
12.0.0:
09/28/07 -- Removed BOM tables and OMIT BOM options from HF capacitor substitution, with halogen parts as alternates.
09/28/07 -- Synced M87 MLB label 10.3.0
09/28/07 -- Page 50: updating GPUVcore current sense resistor values for gain of 4.83
12.0.0:
10/01/07 -- Synced M87 LIO label 9.0.0 Added R9810
10/01/07 -- Synced M87 LIO label 7.0.0
10/01/07 -- <rdar://problem/5493576> M87/M88 MLB/LED: LED driver current mirror can not be disabled + power sequencing issue
<rdar://problem/5510696> TASK: M87 LIO changes to support LED board
10/01/07 -- Page 5: Added 376S0448 as alternate for 376S0445.
13.0.0:
10/05/07 -- Page 5: Removed HDCP ROM. Removed U8770, R8770,R871, C8770.
10/05/07 -- Page 75: GPU Vcore supply: Changed L8920 from 152S0525 to 152S0697.Dale 0.9uH 27A inductor has smaller pad size than Vishay IHLP4040.
13.1.0:
10/09/07 -- Synced m87_mlb label Change 72968 Page 5: Changed Module parts for new Penryn APNs.
10/09/07 -- Page 93: <rdar://problem/5525486> M87/88 1V8 FB DC converter transient response improve/BOM change
10/09/07 -- R9308 change to 40.2k, 0402, 1%; C9308 change to 680pF, 0402, 10V, 10% C9307 change to 68pF, 0402, 10V, 10%

DVT (cont):

14.0.0:
10/12/07 -- Page 81: Added FL9600 155S0372 to multi-touch trackpad power and GND.
10/12/07 -- Synced M87_MLB label: 12.1.0
10/12/07 -- Page 46: Changed to new Sleep LED circuit Deleted, Q5032,R5032,R5030 Added, C5030 Changed Q5030 to new LED Driver IC
10/12/07 -- Synced M* & LIO label: 10.0.0
10/12/07 -- Changed R9807 to 5.1k Changed C9807 to 0.1uF Changed R9809 to 200k
14.1.0:
10/19/07 -- Synced M87_MLB label: 12.2.0 Page 50: Named unnamed net on Q5030.
10/19/07 -- Page 69: NO STUFF battery positive terminal varistor DZ6960
14.5.0:
10/24/07 -- Page 43: Changed L4605 ferrite bead to 155S0329 for lower DCR.
10/24/07 -- Page 57: Changed DZ6960-DZ6963 to 377S0068. These are NO STUFFs.
10/24/07 -- Page 90: Graphics constraint changed all GDDR3_46SE constraints back to GDDR3_50SE.
16.0.0:
11/01/07 -- Page 53: Changed U5750 TMP102 to RevE part 353S2039 with old part 353S1807 as alternate.
11/01/07 -- Page 59: CPU Vcore power supplychange C7134 to 0.022uF 132S0102 per Dayu
17.0.0:
11/06/07 -- Page 25: Removed NO STUFF BOM option from R2552, pull up on SB GPIO38.
11/06/07 -- Synced M87_LIO label 14.0.0 pg. 82 Changed C9805 to 2.2uF for LED power sequencing.
PVT:
18.0.0:
12/10/07 -- Page 98: Changed R9808 to 200K, R9809 to 100K, C9802 to 0.033uF, C9807 to 0.33uF to improve Q9806 Vgs and sequencing
18.1.0:
12/12/07 -- Page 5: Updated CPUs to PRQ parts, removed XDP_CONN and GPU_TMP401 bom options and changed to SMC_DEBUG_NO for PVT
12/12/07 -- Page 50: Removed ST SIL driver and returned to EVT's BJT-driven current source
12/12/07 -- Page 98: Changed C9805 to actual 2.2uF part (removed table entry)
18.2.0:
12/13/07 -- Page 13: NO STUFFed R1330/R1331 since the LVDS_CTRL_DATA/CLK lines are grounded
18.3.0:
12/16/07 -- Page 54: Added C8992/R8992 to provide differential sense option
A.0.0:
12/18/07 -- Release as Rev A

D

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Revision History	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
	SCALE	SHT	OF
	NONE	6	92

Functional Test Points

Fan Connectors

FUNC_TEST		
TRUE	PP5V_S0	7 8 27 42 47 48 52 54 58 59 65 80 81 89
TRUE	FAN_LT_PWM	52
TRUE	FAN_LT_TACH	52
TRUE	FAN_RT_PWM	52
TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST		
TRUE	PP3V42_G3H	8 28 43 45 46 47 48 57 75 76 81 82 83 84
TRUE	PP5V_S0	7 8 27 42 47 48 52 54 58 59 65 80 81 89
TRUE	LPC_AD<0>	23 45 47
TRUE	LPC_AD<1>	23 45 47
TRUE	LPC_FRAME_L	23 45 47
TRUE	PM_CLKRUN_L	25 45 47
TRUE	PCI_FW_GNT_L	24 38 47 87
TRUE	SMC_TMS	45 46 47
TRUE	DEBUG_RESET_L	28 47
TRUE	SMC_TRST_L	45 47
TRUE	SMC_TDO	45 46 47
TRUE	SMC_MD1	45 47
TRUE	SMC_TX_L	43 45 46 47
TRUE	FWH_INIT_L	47
TRUE	PCI_CLK33M_LPCPLUS	30 47 88
TRUE	LPC_AD<2>	23 45 47
TRUE	LPC_AD<3>	23 45 47
TRUE	INT_SERIRQ	25 45 47
TRUE	PM_SUS_STAT_L	25 45 46 47
TRUE	SMC_TDI	45 46 47
TRUE	SMC_TCK	45 46 47
TRUE	SMC_RESET_L	45 46 47
TRUE	SMC_NMI	45 47
TRUE	SMC_RX_L	43 45 46 47
TRUE	LINDACARD_GPIO	25 47

Left ALS

FUNC_TEST		
TRUE	ALS_GAIN	34 45 54
TRUE	LTALS_OUT	34 54
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST		
TRUE	HSTHMSNS_D_P	51 91
TRUE	HSTHMSNS_D_N	51 91
TRUE	RSFSTHMSNS_D_P	51 91
TRUE	RSFSTHMSNS_D_N	51 91
TRUE	CEUTHMSNS_D2_P	51 91
TRUE	CEUTHMSNS_D2_N	51 91

System Validation TPs

FUNC_TEST		
TRUE	CPU_PWRGD	10 13 23 83
TRUE	CPU_DPSLP_L	7 10 23 83
TRUE	PM DPRSLPVR	16 25 59 83
TRUE	CPU_DPSLP_L	7 10 23 83
TRUE	PM_LAN_ENABLE	25 45
TRUE	PCI_RST_L	24 28
TRUE	PM_RSMRST_L	25 45
TRUE	PM_SB_PWR0K	9 25 28
TRUE	SB_RTC_RST_L	23 28
TRUE	PM_STPCPU_L	25 29 30
TRUE	PM_STPPCI_L	25 29 30
TRUE	VR_PWRGD_CLKEN	25 28
TRUE	VR_PWRGD_DELAY	9 16 28 59
TRUE	FSB_CPURST_L	10 13 14 83
TRUE	FSB_CPUSLP_L	10 14 83
TRUE	FSB_DPWR_L	10 14 83
TRUE	NB_SB_SYNC_L	16 25
TRUE	PM_BMBUSY_L	16 25

Battery Digital Connector

FUNC_TEST		
TRUE	SMC_BS_ALERT_L	45 46 57
TRUE	SMBUS_SMC_BSA_SCL	45 48 57 88
TRUE	SMBUS_SMC_BSA_SDA	45 48 57 88
TRUE	BATT_POS	57 66
TRUE	GND	
TRUE	GND (HOST_DETECT_L)	

Left I/O Power Connector

FUNC_TEST		
TRUE	PP18V5_DCIN	87 Request for 2 test points
TRUE	PPBUS_G3H	82 83 84 85 86 87 88 89 Request for 3 test points
TRUE	GND	

Request for at least 10 GND test points
NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST		
TRUE	PPVBATT_G3_RTC	28
TRUE	GND	

Current Sense Calibration

FUNC_TEST		
TRUE	ISENSE_CAL_EN	45 49
TRUE	PP5V_S0	7 8 27 42 47 48 52 54 58 59 65 80 81 89
TRUE	PPVCORE_S0_CPU	8 9 11 12 } 2 TPs per
TRUE	PPVCORE_GPU	8 49 68 75 } per
TRUE	GND	

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST		
TRUE	PP5V_S3_CAMERA_F	44
TRUE	USB_CAMERA_F_N	44 91
TRUE	USB_CAMERA_F_P	44 91

Other Func Test Points

FUNC_TEST		
TRUE	PM_SYSRST_L	25 28 45
TRUE	SMC_ONOFF_L	45 46 81

ICT Test Points

CPU FSB NO_TESTS

MAKE BASE	NO_TEST	
TRUE	FSB_A_L<31..3>	10 14 83
TRUE	FSB_ADS_L	10 14 83
TRUE	FSB_ADSTB_L<1..0>	10 14 83
TRUE	FSB_BNR_L	10 14 83
TRUE	FSB_BREQ0_L	10 14 83
TRUE	FSB_D_L<63..0>	10 14 83
TRUE	FSB_DBSY_L	10 14 83
TRUE	FSB_DINV_L<3..0>	10 14 83
TRUE	FSB_DRY_L	10 14 83
TRUE	FSB_DSTB_L_N<3..0>	10 14 83
TRUE	FSB_DSTB_L_P<3..0>	10 14 83
TRUE	FSB_HIT_L	10 14 83
TRUE	FSB_HITM_L	10 14 83
TRUE	FSB_LOCK_L	10 14 83
TRUE	FSB_REQ_L<4..0>	10 14 83
TRUE	NC_CPU_RSVD5	NC_CPU_RSVD5 7 10

NB NO_TESTS

MAKE BASE	NO_TEST	
TRUE	NC_NB_NC<1..16>	TP_NB_NC<1..16> 16
TRUE	NC_NB_RSVD<26..27>	TP_NB_RSVD<26..27> 16
TRUE	NC_NB_RSVD<24>	TP_NB_RSVD<24> 16

Backlight Connector

FUNC_TEST		
TRUE	BKLT_PWR	81 82
TRUE	BKLT_GND	81 82
TRUE	BKLT_P5V_EN	81 82
TRUE	BKLT_PWM	81 82
TRUE	GND	

IR & Sleep LED Connector

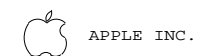
FUNC_TEST		
TRUE	PP5V_S3	8 44 46 58 81
TRUE	USB_IR_N	24 81 86
TRUE	USB_IR_P	24 81 86
TRUE	SYS_LED_ANODE	46 81
TRUE	GND	

Functional / ICT Test

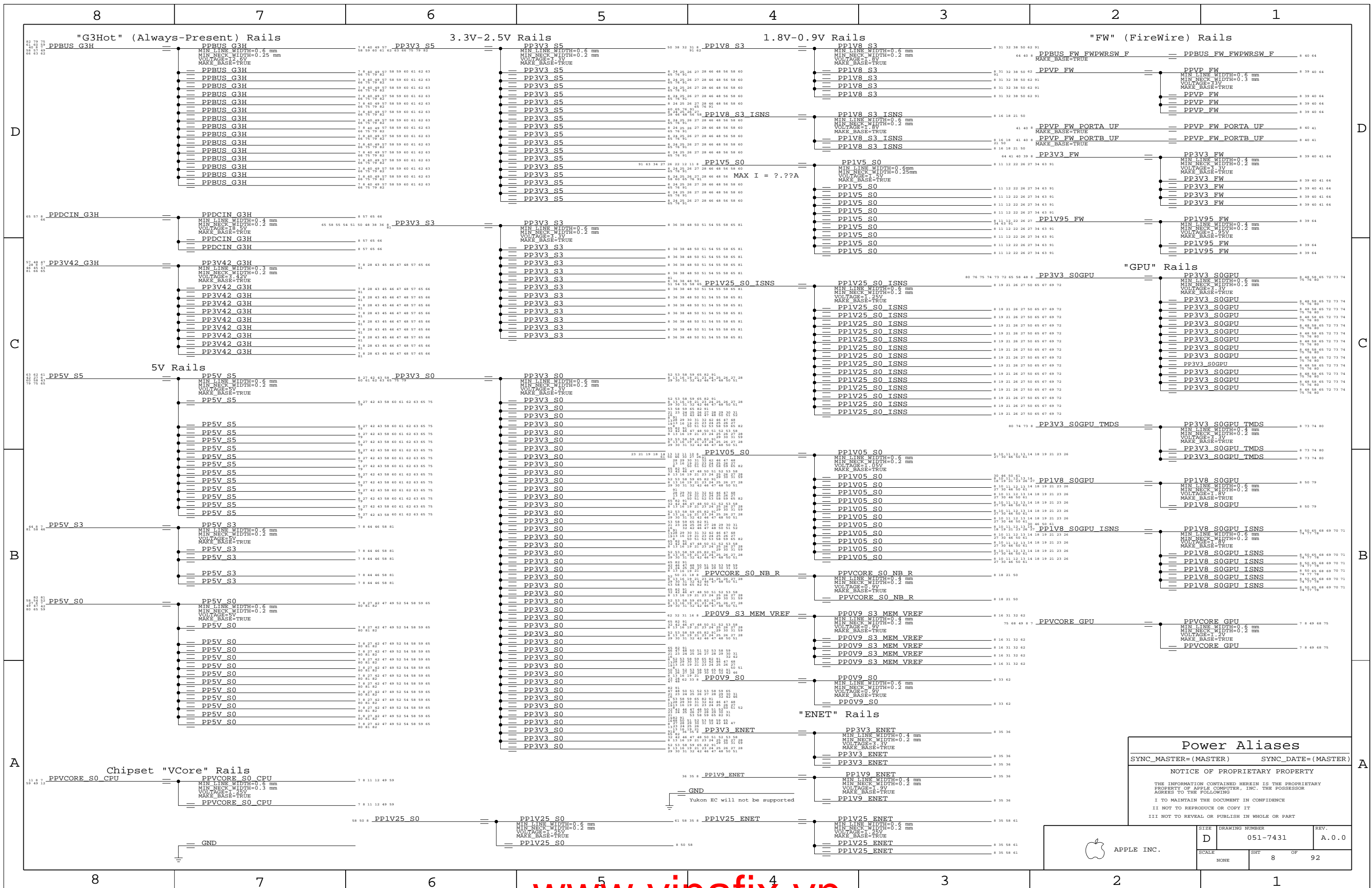
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SCALE	SHT	OF
NONE	7	92



Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
NONE	8	92	

8

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1

86 24 9	TP_USB_EXTDN MAKE_BASE=TRUE	==	TP_USB_EXTDN	9 24 86
86 24 9	TP_USB_EXTDP MAKE_BASE=TRUE	==	TP_USB_EXTDP	9 24 86
28 25 9 7	PM_SB_PWROK MAKE_BASE=TRUE	==	PM_SB_PWROK	7 9 25 28
59 28 16 9 7	VR_PWRGOOD_DELAY MAKE_BASE=TRUE	==	VR_PWRGOOD_DELAY	7 9 16 28 59
88 67 30 29 9	PEG_CLK100M_GPU_P MAKE_BASE=TRUE	==	PEG_CLK100M_GPU_P	9 29 30 67 88
88 67 30 29 9	PEG_CLK100M_GPU_N MAKE_BASE=TRUE	==	PEG_CLK100M_GPU_N	9 29 30 67 88
55 45 9	SMC_SMS_INT MAKE_BASE=TRUE	==	SMC_SMS_INT	9 45 55
23 9	TP_EXTGPU_PWR_EN MAKE_BASE=TRUE	==	TP_EXTGPU_PWR_EN	9 23
34 25 9	IPHS_SW_BIAS_EN_L MAKE_BASE=TRUE	==	IPHS_SW_BIAS_EN_L	9 25 34
34 24 9	IPHS_SW_INT MAKE_BASE=TRUE	==	IPHS_SW_INT	9 24 34
66 46 45 9	SMC_ENRGYSTR_LDO_EN MAKE_BASE=TRUE	==	SMC_ENRGYSTR_LDO_EN	9 45 46 66
31 9	TP_MEM_A_A<15> MAKE_BASE=TRUE	==	TP_MEM_A_A<15>	9 31
32 9	TP_MEM_B_A<15> MAKE_BASE=TRUE	==	TP_MEM_B_A<15>	9 32
82 28 24 9 7	PLT_RST_L	==	PLT_RST_L	7 9 24 28 82
82 73 72 9	GPU_BL_PWM	==	GPU_BL_PWM	9 72 73 82
82 73 72 9	GPU_BKLT_EN	==	GPU_BKLT_EN	9 72 73 82

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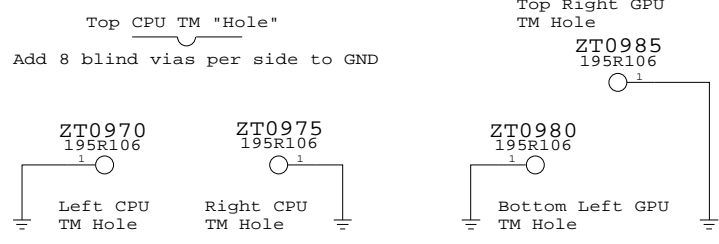
B

A

A

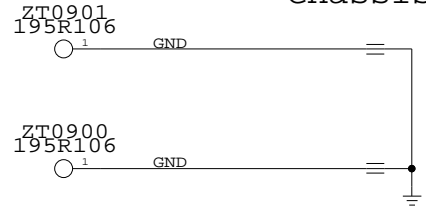
Thermal Module Holes

All holes are plated through holes with two exceptions:

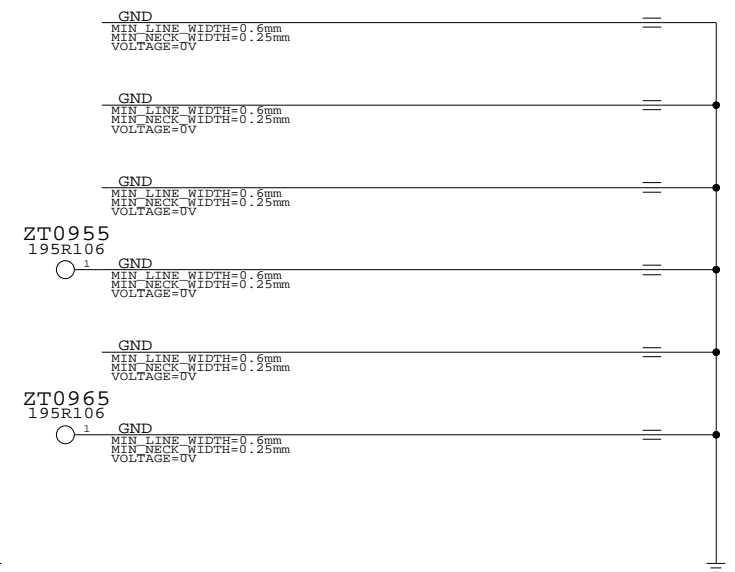


- GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)
- GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

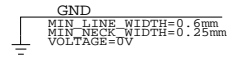
Chassis GNDS



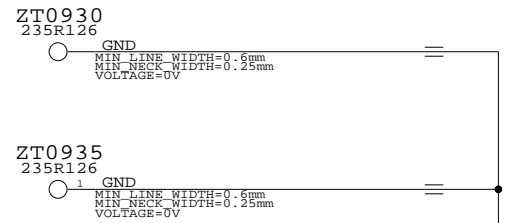
Frame holes



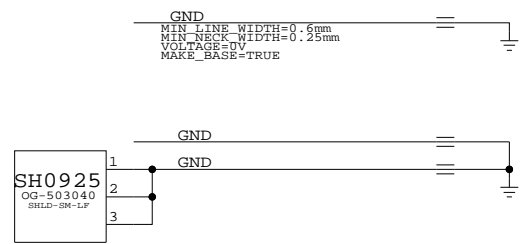
Digital Ground



RAM door (Torx) holes

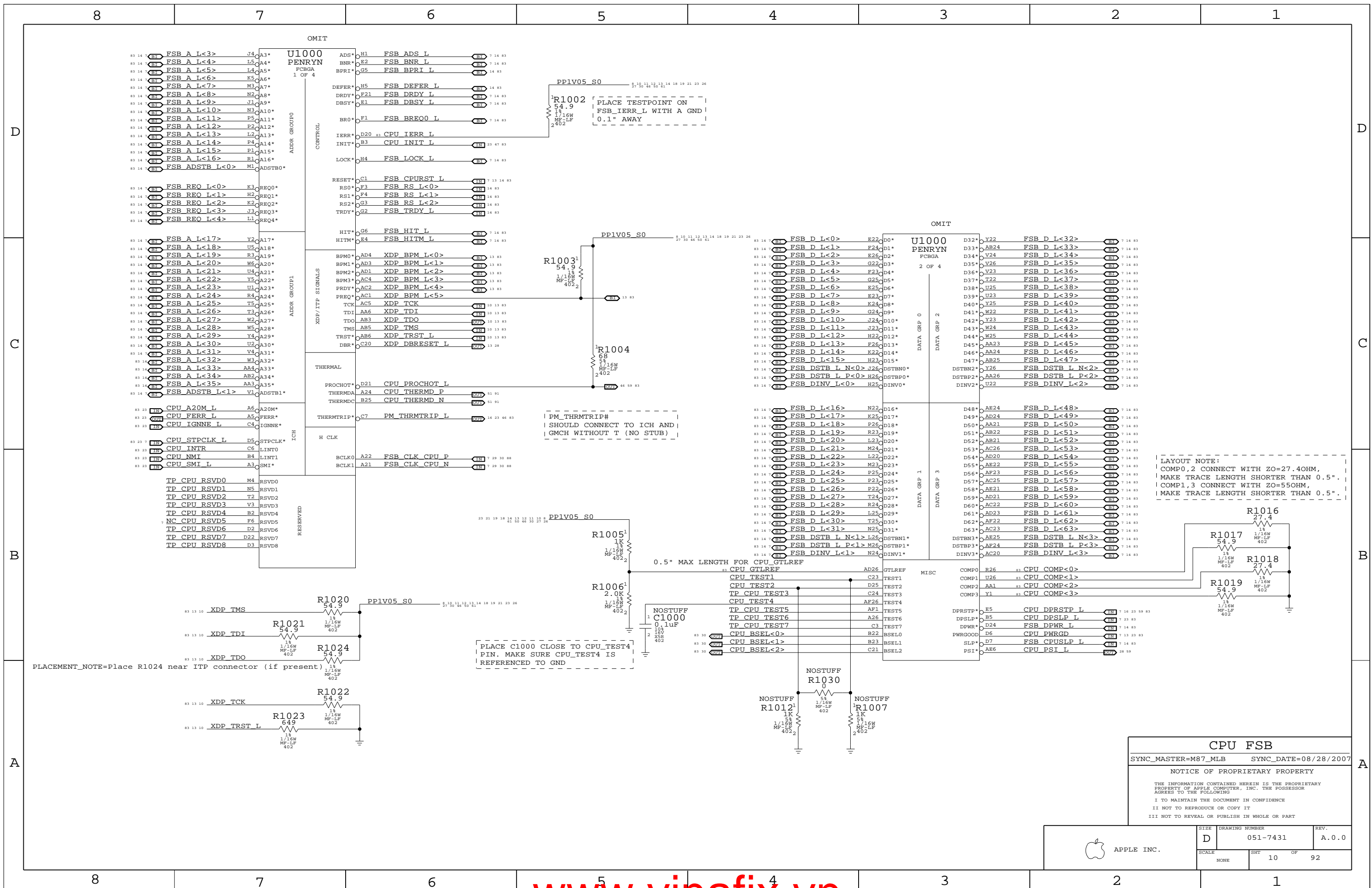


Chassis connection to be made at the mounting hole east of the LVDS connector



Signal Aliases		
SYNC_MASTER=MASTER	SYNC_DATE=MASTER	
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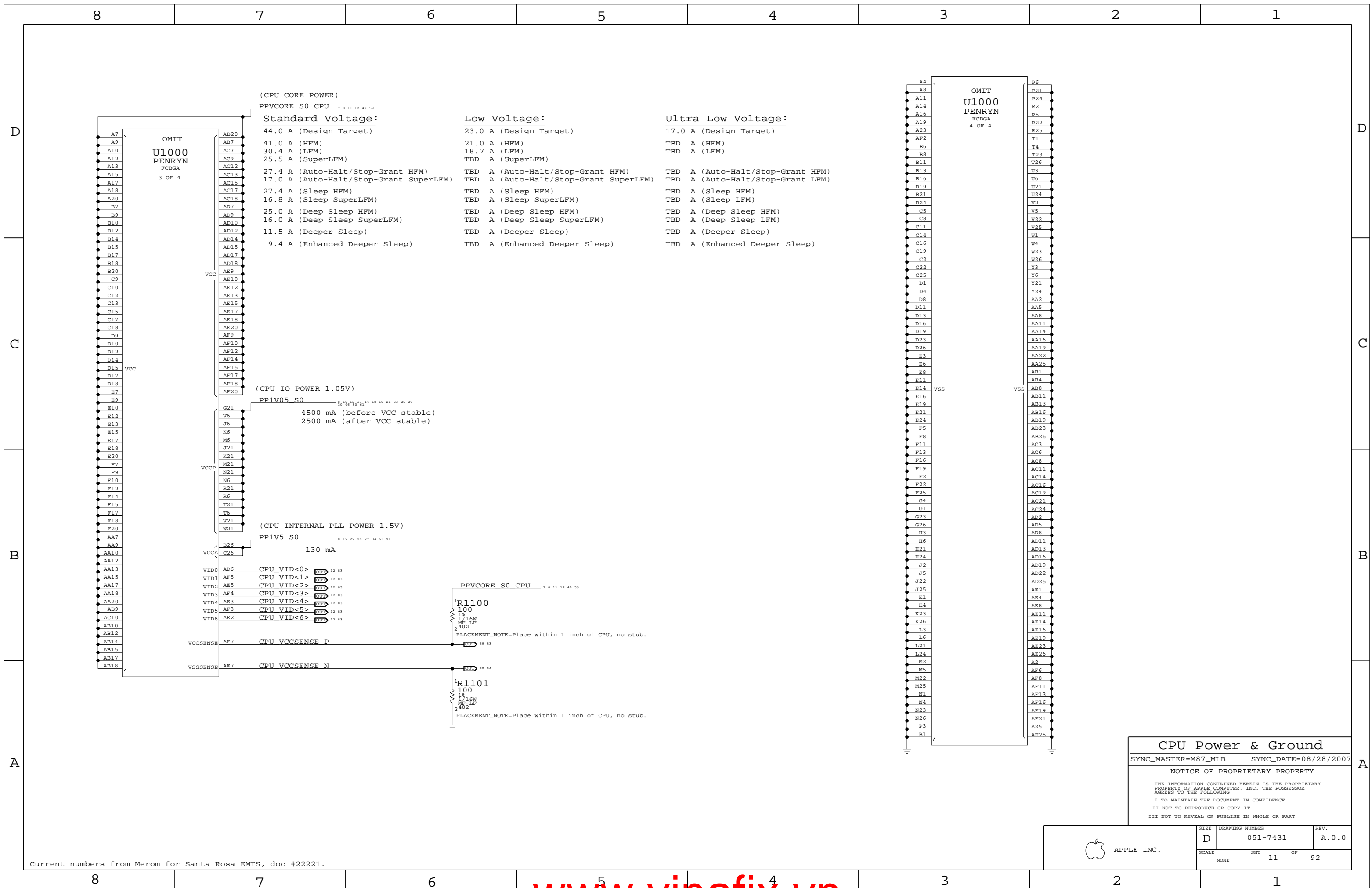
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	9	92	



LAYOUT NOTE:
 COMPO,2 CONNECT WITH ZO=27.4OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".
 COMPL,3 CONNECT WITH ZO=55OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007
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	D	051-7431	A.0.0
SCALE	SHT	OF	92
NONE	10		



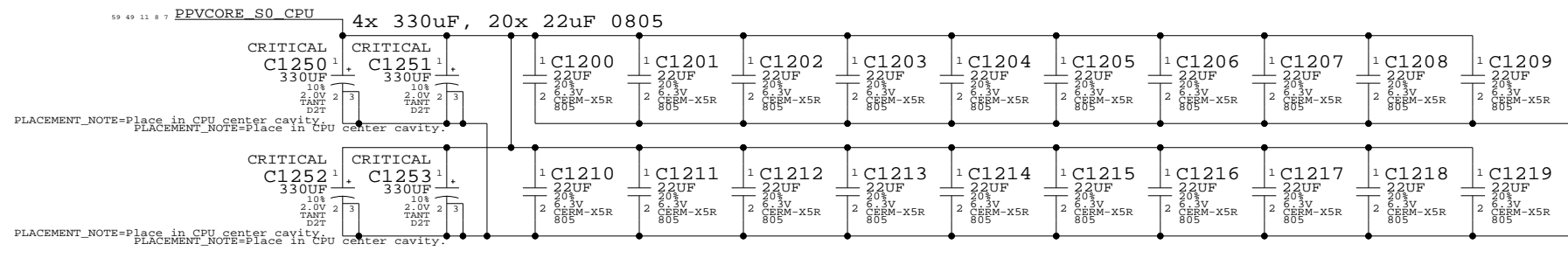
CPU Power & Ground
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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	D	051-7431	A.0.0
SCALE	SHT 11 OF 92		
NONE			

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

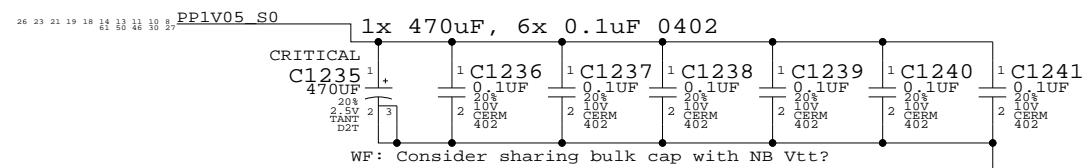
CPU VCORE HF AND BULK DECOUPLING



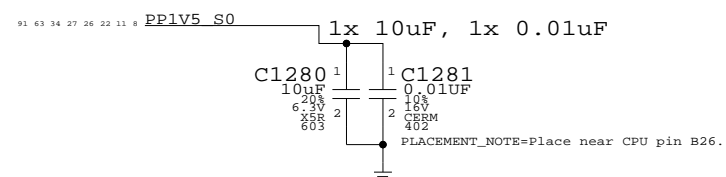
CPU VCORE VID CONNECTIONS

83 11 CPU VID<0..6> == IMVP6 VID<0..6> 7 59 83
MAKE_BASE=TRUE

VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

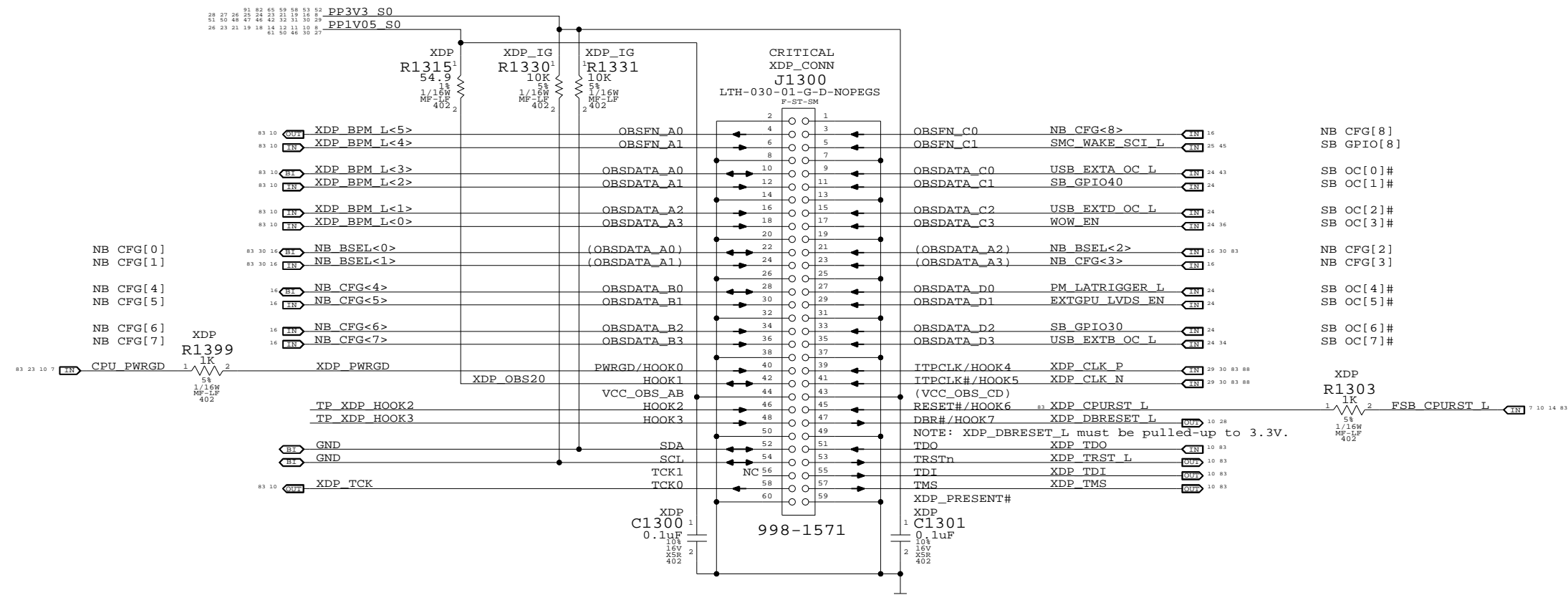
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SCALE	SHT 12 OF 92		
NONE			

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

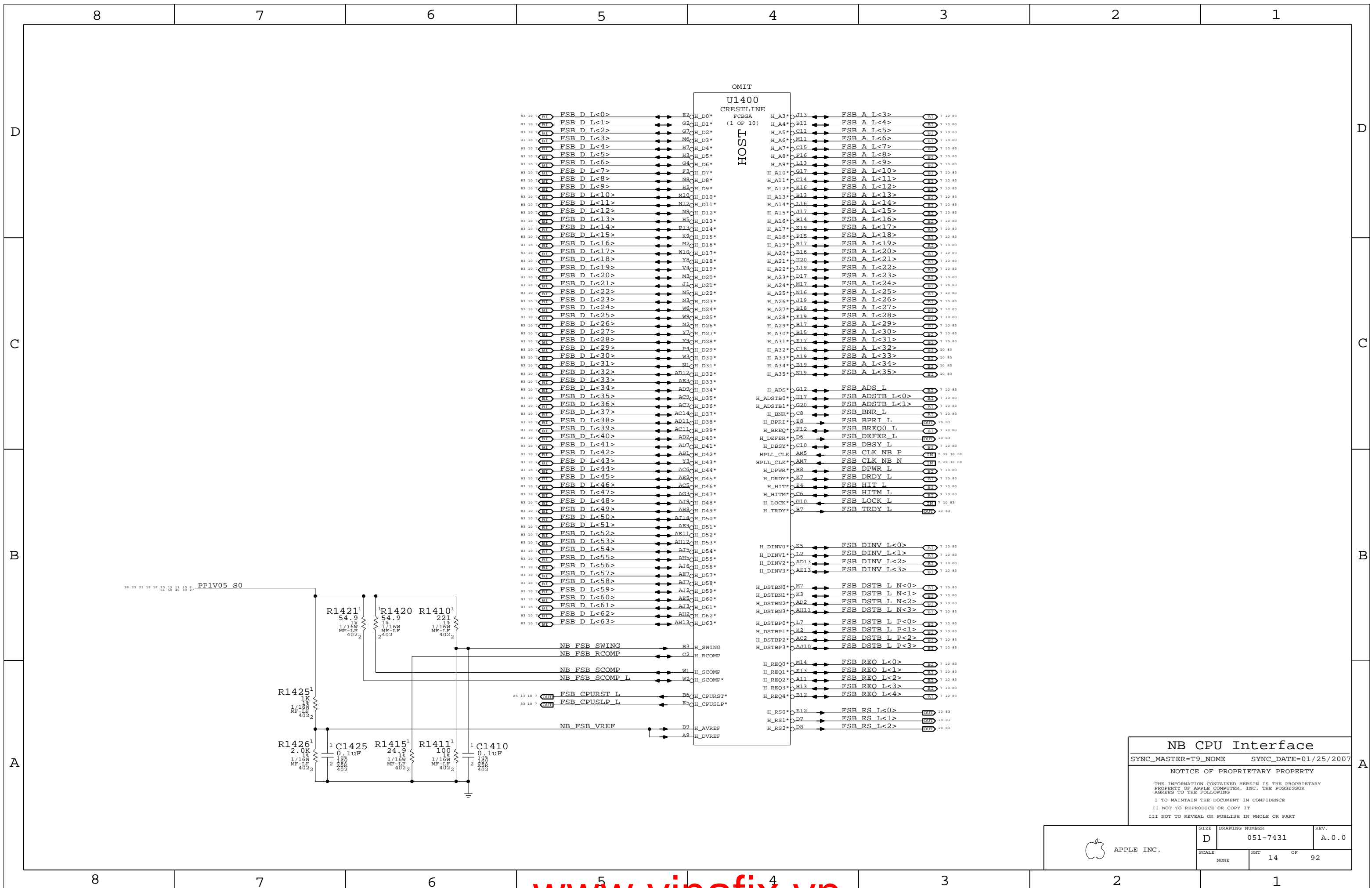


← Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)
SYNC_MASTER=T9_NOME SYNC_DATE=01/22/2007

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NONE			



U1400
CRESTLINE

(1 OF 10)

HOST

NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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NONE	14	92	

LVDS Disable

Can leave all signals NC if LVDS is not implemented. Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

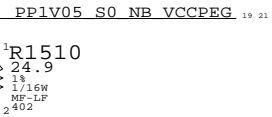
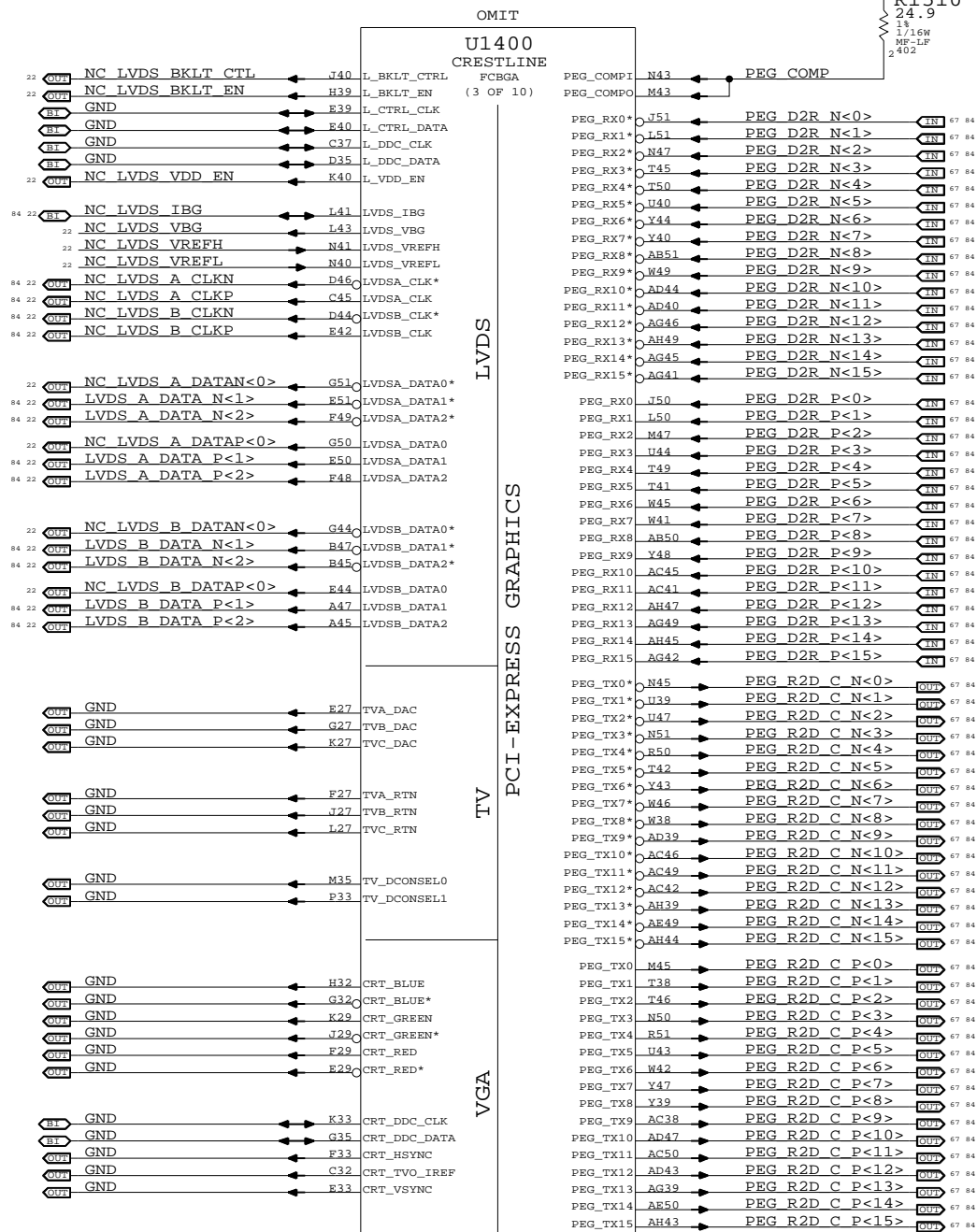
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND. Can tie the following rails to GND: VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND. Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore). Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore). Tie VCC_AXG and VCC_AXG_NCTF to GND. Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

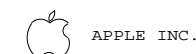
SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces
SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

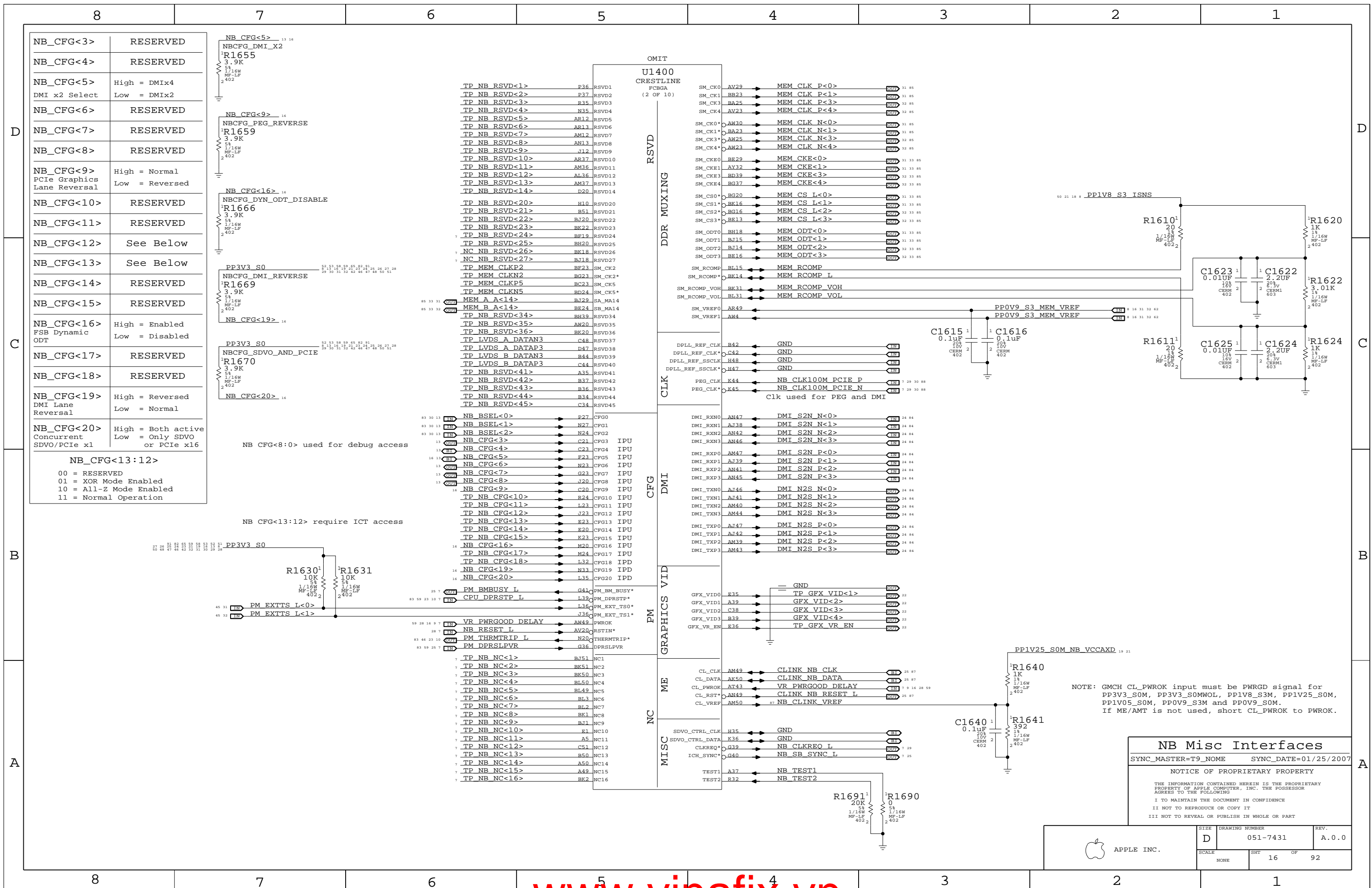
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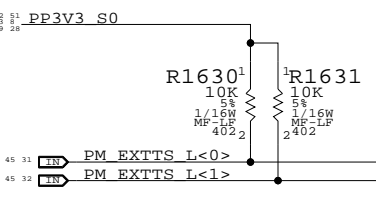


NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIx4 DMI x2 Select Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
NB_CFG<20>	High = Both active Concurrent Low = Only SDVO SDVO/PCIe x1 or PCIe x16

NB_CFG<13:12>
00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<8:0> used for debug access

NB_CFG<13:12> require ICT access



NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_SOM, PP3V3_SOMWOL, PP1V8_S3M, PP1V25_SOM, PP1V05_SOM, PP0V9_S3M and PP0V9_SOM. If ME/AMT is not used, short CL_PWROK to PWROK.

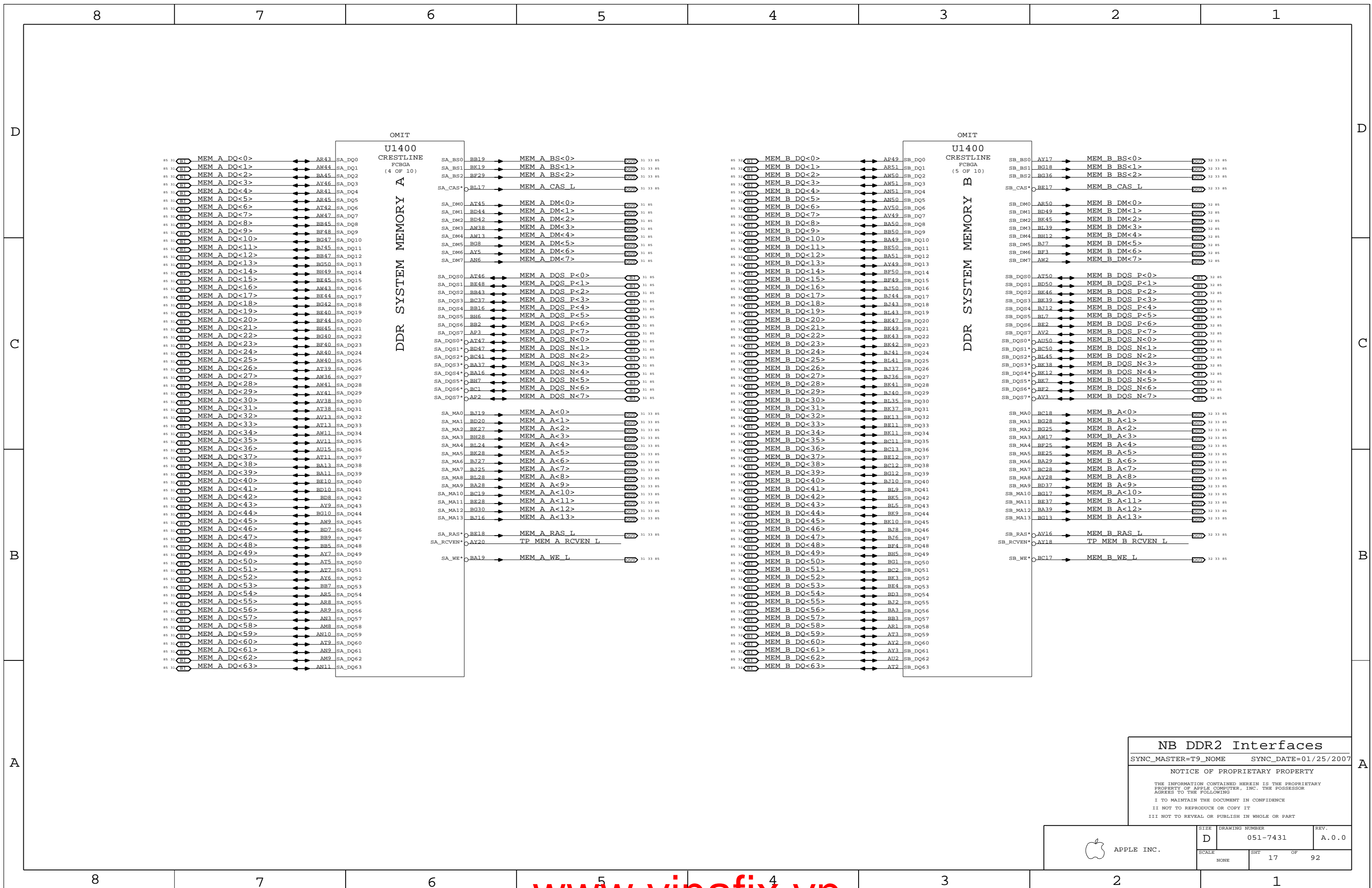
NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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SCALE	SHT	OF
NONE	16	92

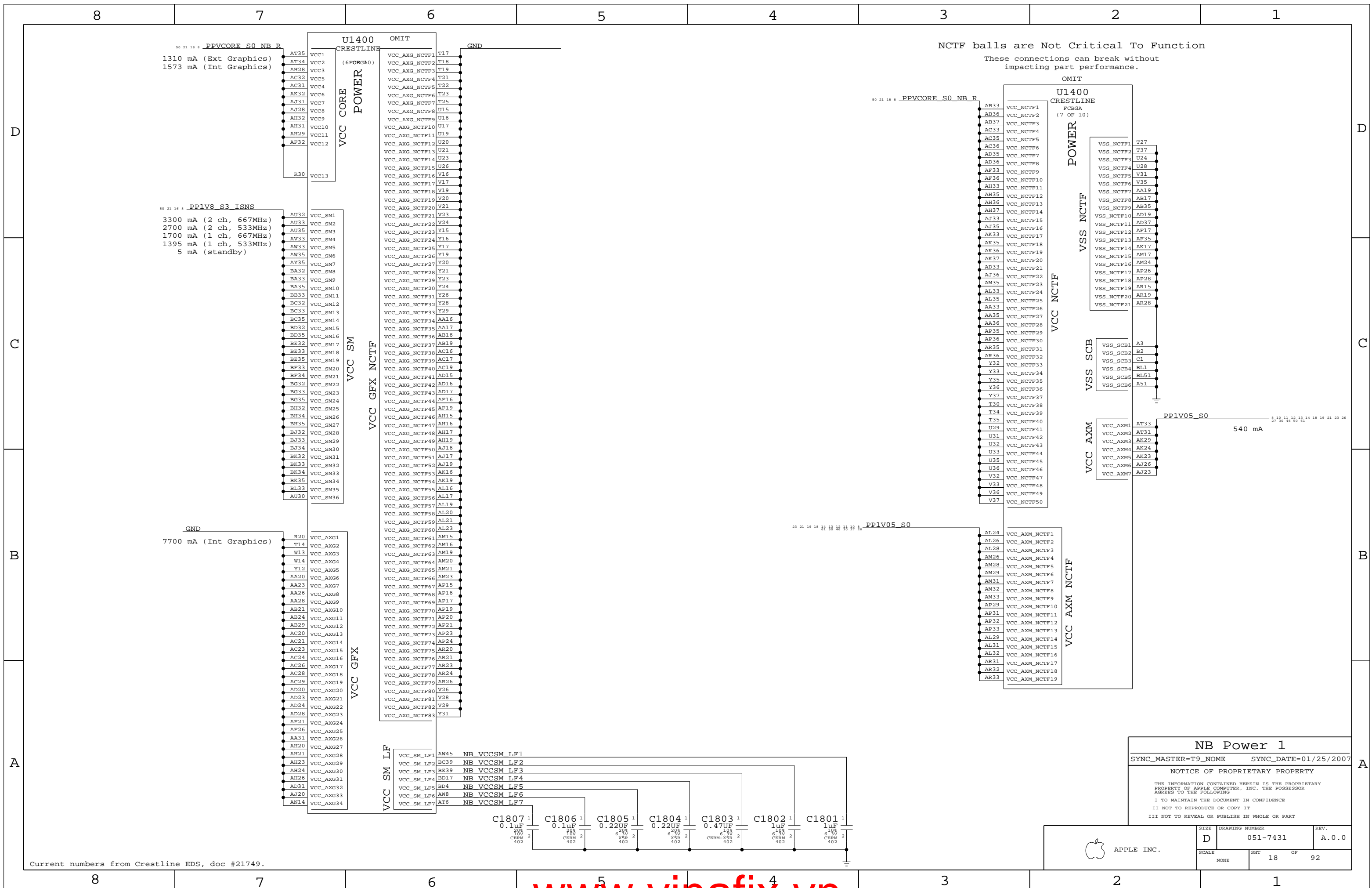




NB DDR2 Interfaces
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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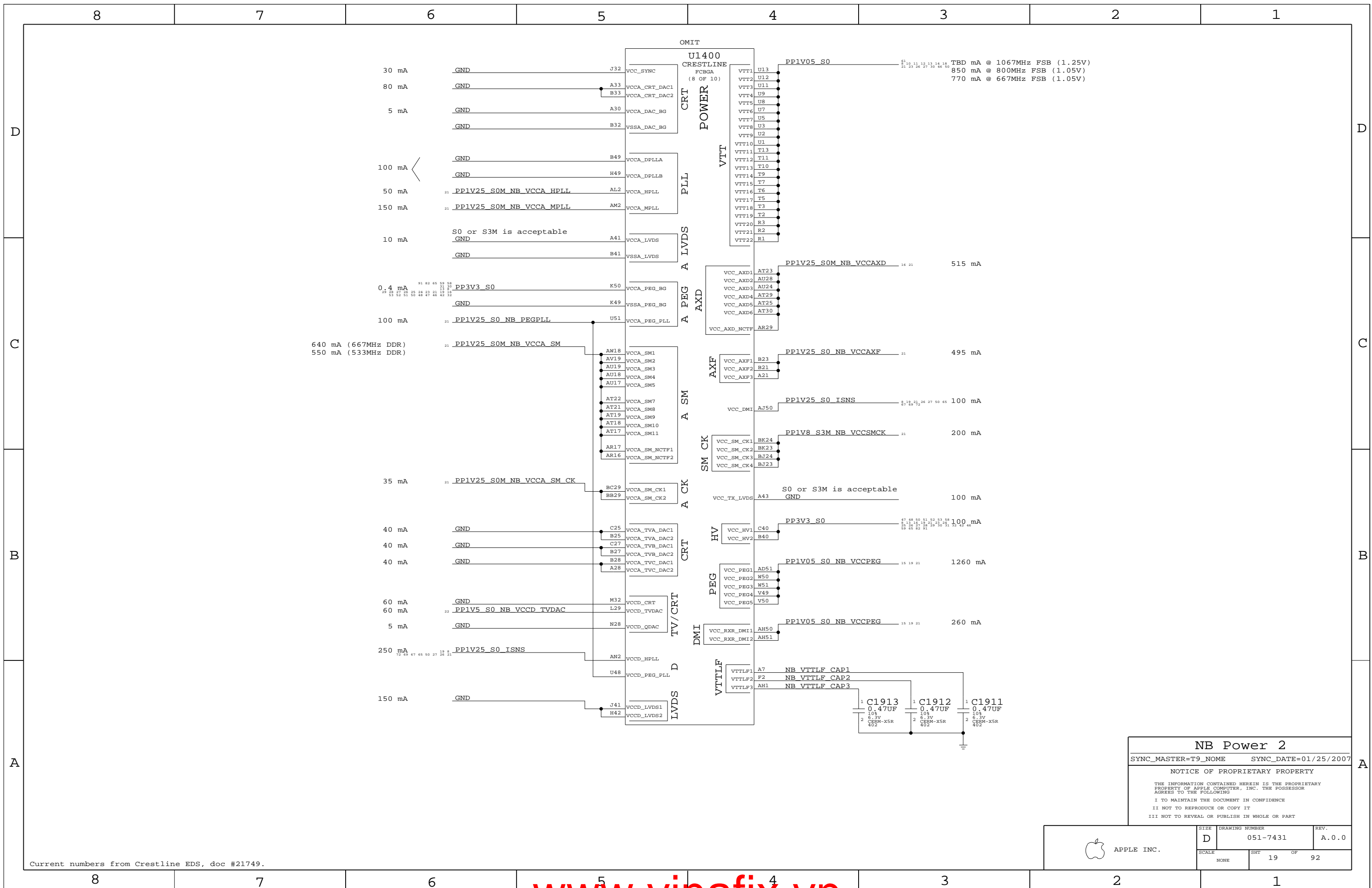
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	92
NONE	17		



NCTF balls are Not Critical To Function
These connections can break without impacting part performance.

NB Power 1
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007
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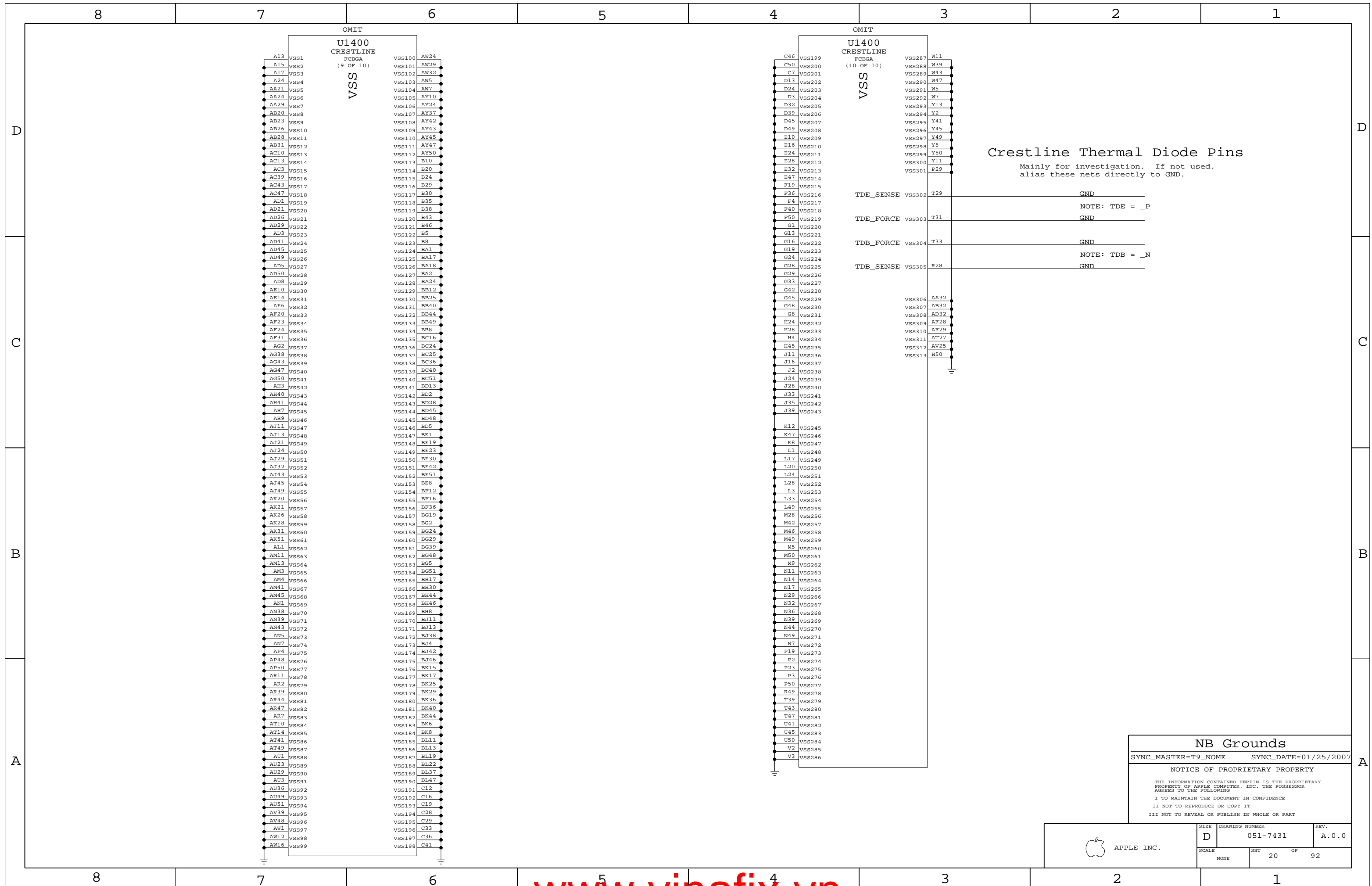
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT 18 OF 92		
NONE			



Current numbers from Crestline EDS, doc #21749.

NB Power 2
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007
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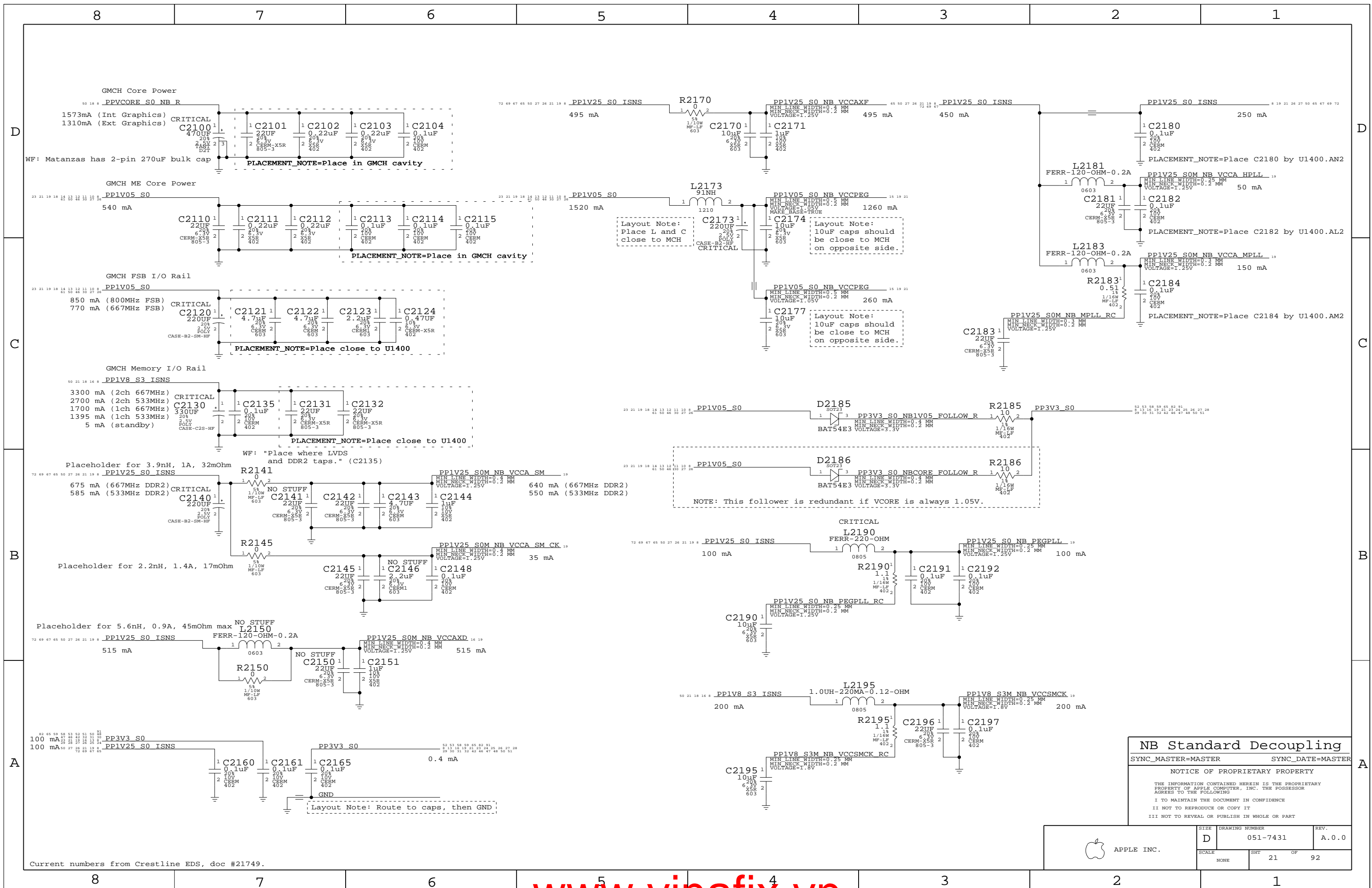
APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHEET 19	OF 92



Crestline Thermal Diode Pins
 Mainly for investigation. If not used,
 alias these nets directly to GND.

NB Grounds
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT 20 OF 92		
NONE			



GMCH Core Power

1573mA (Int Graphics)
1310mA (Ext Graphics)

GMCH ME Core Power

540 mA

GMCH FSB I/O Rail

850 mA (800MHz FSB)
770 mA (667MHz FSB)

GMCH Memory I/O Rail

3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)

Placeholder for 3.9nH, 1A, 32mOhm

Placeholder for 2.2nH, 1.4A, 17mOhm

Placeholder for 5.6nH, 0.9A, 45mOhm max

100 mA PP3V3 S0
100 mA PP1V25 S0 ISNS

0.4 mA

Current numbers from Crestline EDS, doc #21749.

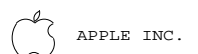
NB Standard Decoupling

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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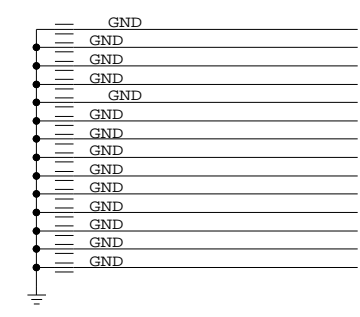
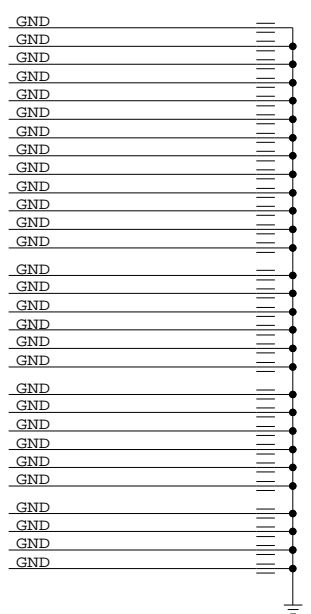
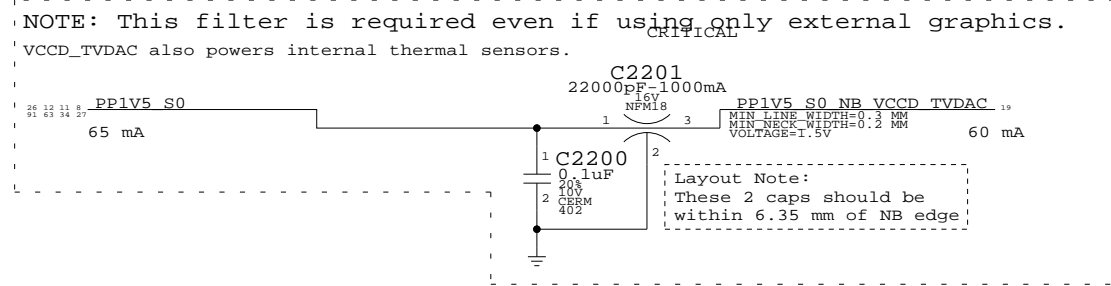
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	21	92

Crestline LVDS Strapping



22 15	NC LVDS BKLT CTL	==	NC LVDS BKLT CTL	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS BKLT EN	==	NC LVDS BKLT EN	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS VDD EN	==	NC LVDS VDD EN	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 22 15	NC LVDS IBG	==	NC LVDS IBG	15 22 84
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS VBG	==	NC LVDS VBG	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 22 15	NC LVDS A CLKN	==	NC LVDS A CLKN	15 22 84
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 22 15	NC LVDS A CLKP	==	NC LVDS A CLKP	15 22 84
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 22 15	NC LVDS B CLKN	==	NC LVDS B CLKN	15 22 84
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 22 15	NC LVDS B CLKP	==	NC LVDS B CLKP	15 22 84
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS A DATAN<0>	==	NC LVDS A DATAN<0>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS A DATA N<1>	==	NC LVDS A DATAN<1>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS A DATA N<2>	==	NC LVDS A DATAN<2>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS A DATAP<0>	==	NC LVDS A DATAP<0>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS A DATA P<1>	==	NC LVDS A DATAP<1>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS A DATA P<2>	==	NC LVDS A DATAP<2>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS B DATAN<0>	==	NC LVDS B DATAN<0>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS B DATA N<1>	==	NC LVDS B DATAN<1>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS B DATA N<2>	==	NC LVDS B DATAN<2>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS B DATAP<0>	==	NC LVDS B DATAP<0>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS B DATA P<1>	==	NC LVDS B DATAP<1>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
84 15	LVDS B DATA P<2>	==	NC LVDS B DATAP<2>	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS VREFH	==	NC LVDS VREFH	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 15	NC LVDS VREFL	==	NC LVDS VREFL	15 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 16	TP GFX VID<1>	==	TP GFX VID<1>	16 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	
16	GFX VID<2>	==	TP GFX VID<2>	
	MAKE_BASE=TRUE		NO_TEST=TRUE	
16	GFX VID<3>	==	TP GFX VID<3>	
	MAKE_BASE=TRUE		NO_TEST=TRUE	
16	GFX VID<4>	==	TP GFX VID<4>	
	MAKE_BASE=TRUE		NO_TEST=TRUE	
22 16	TP GFX VR EN	==	TP GFX VR EN	16 22
	MAKE_BASE=TRUE		NO_TEST=TRUE	

NB Graphics Decoupling
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

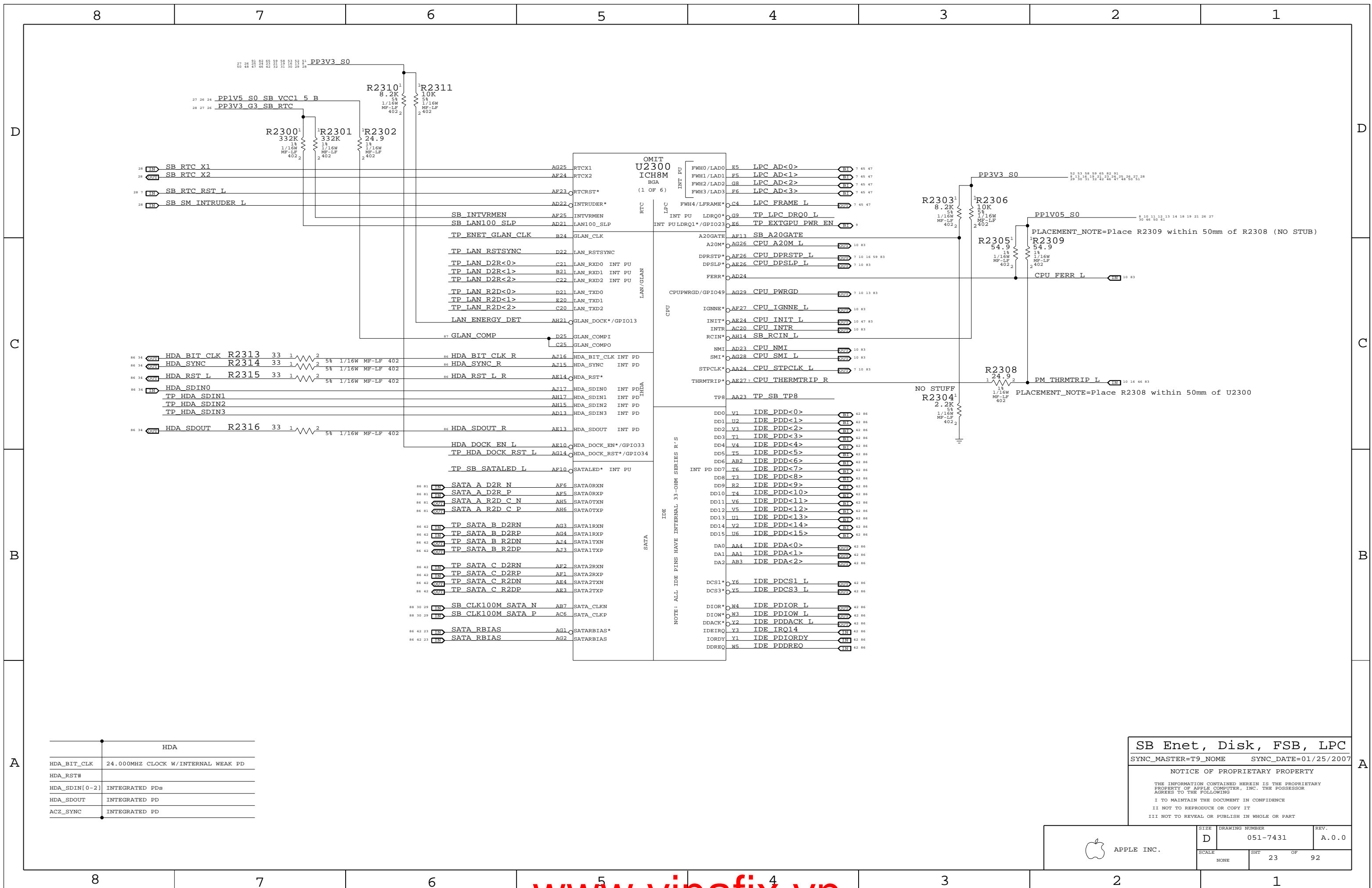
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	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	22	92	

Current numbers from Crestline EDS Addendum, doc #20127.

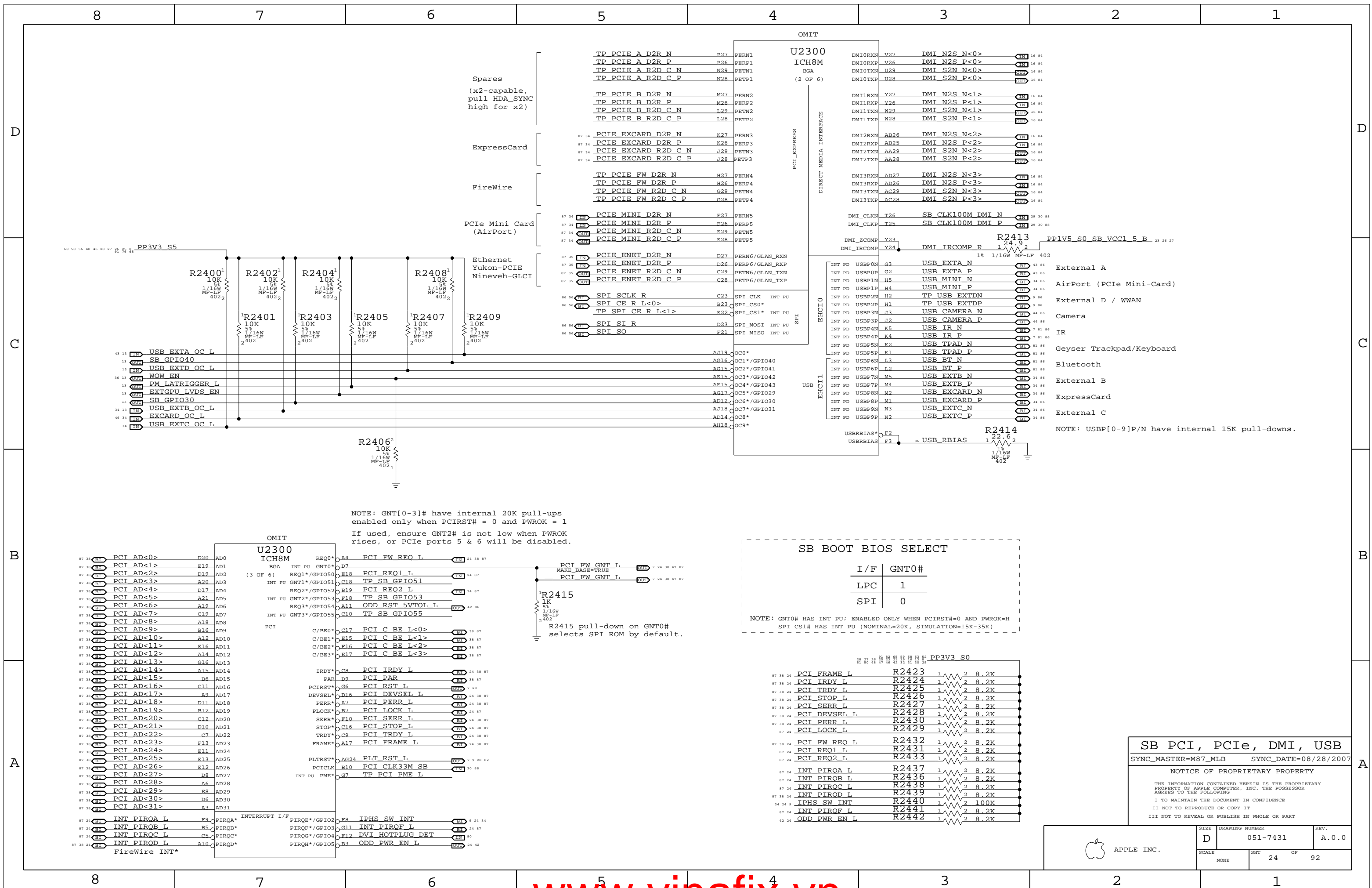


HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	23	92	



NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

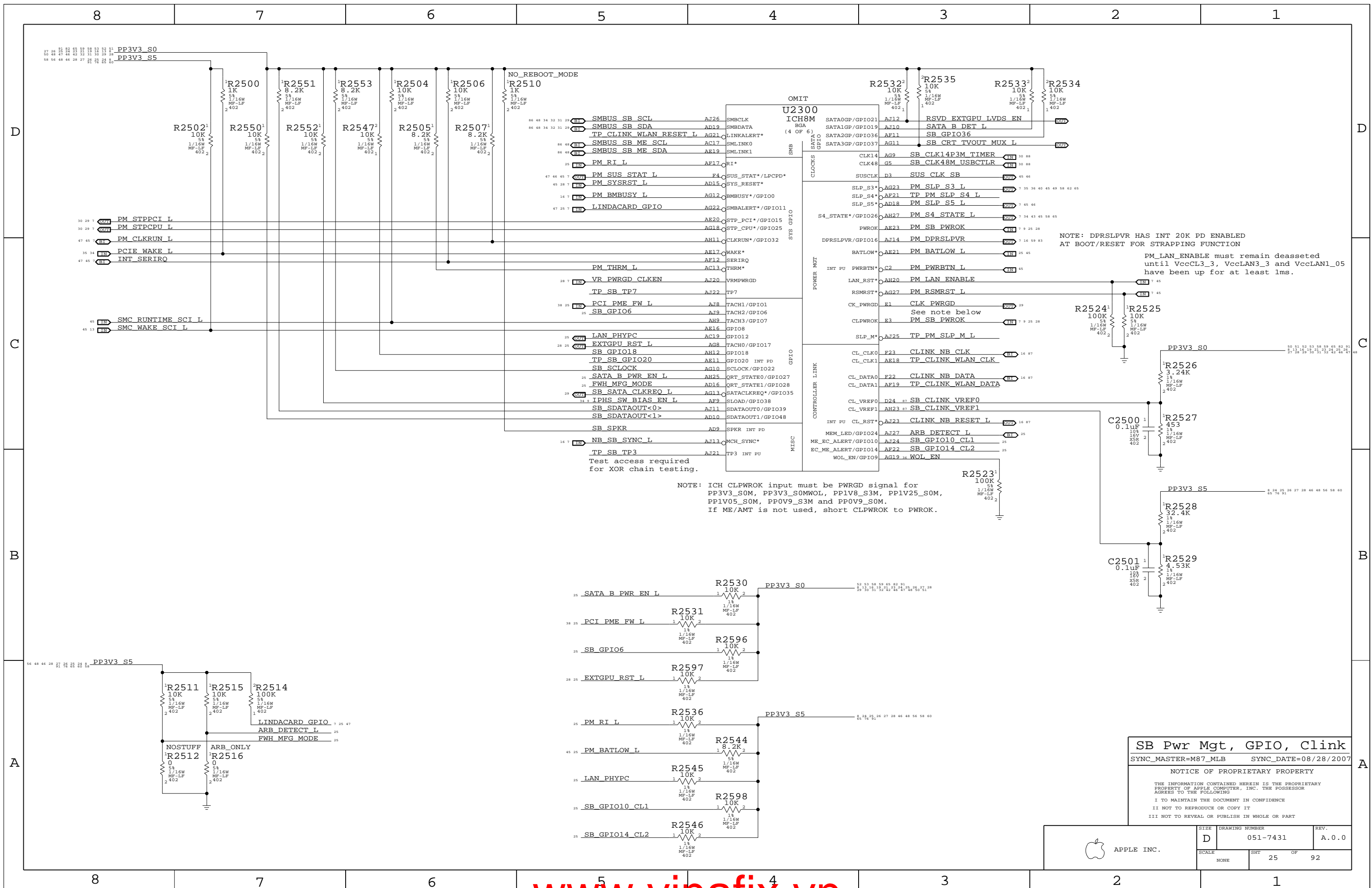
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

PP3V3 S0

87 38 24	PCI FRAME L	R2423	1	2	8.2K
87 38 24	PCI IRDY L	R2424	1	2	8.2K
87 38 24	PCI TRDY L	R2425	1	2	8.2K
87 38 24	PCI STOP L	R2426	1	2	8.2K
87 38 24	PCI SERR L	R2427	1	2	8.2K
87 38 24	PCI DEVSEL L	R2428	1	2	8.2K
87 38 24	PCI PERR L	R2430	1	2	8.2K
87 24	PCI LOCK L	R2429	1	2	8.2K
87 38 24	PCI FW REO L	R2432	1	2	8.2K
87 24	PCI REQ1 L	R2431	1	2	8.2K
87 24	PCI REQ2 L	R2433	1	2	8.2K
87 24	INT PIRQA L	R2437	1	2	8.2K
87 24	INT PIROB L	R2436	1	2	8.2K
87 24	INT PIROC L	R2438	1	2	8.2K
87 24	INT PIROD L	R2439	1	2	8.2K
87 34 9	IPHS SW INT	R2440	1	2	100K
87 24	INT PIROF L	R2441	1	2	8.2K
42 24	ODD PWR EN L	R2442	1	2	8.2K

SB PCI, PCIe, DMI, USB
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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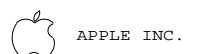


SB Pwr Mgt, GPIO, Clink

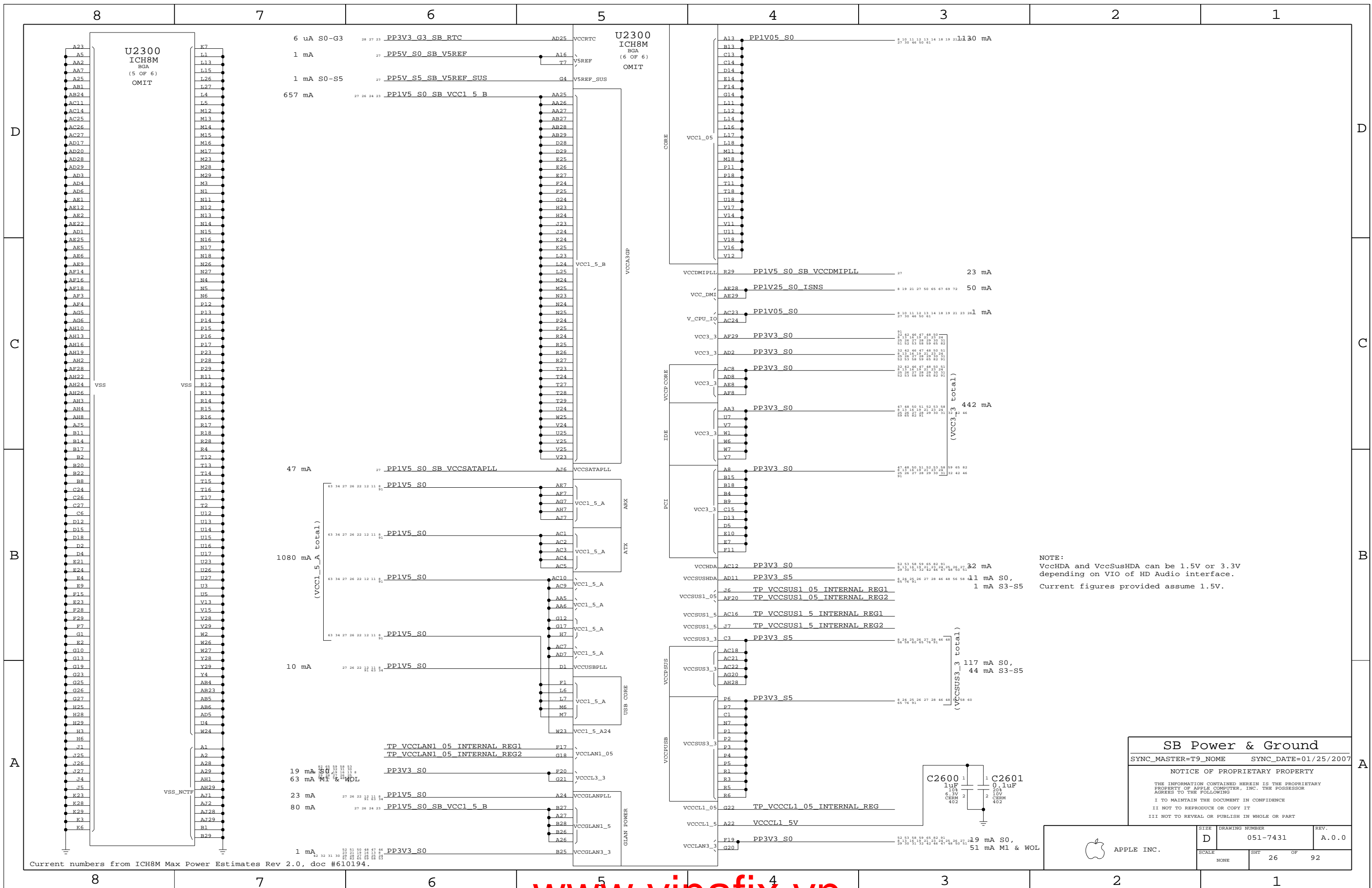
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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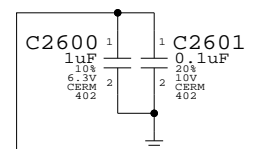


SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	25	92



Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.



SB Power & Ground

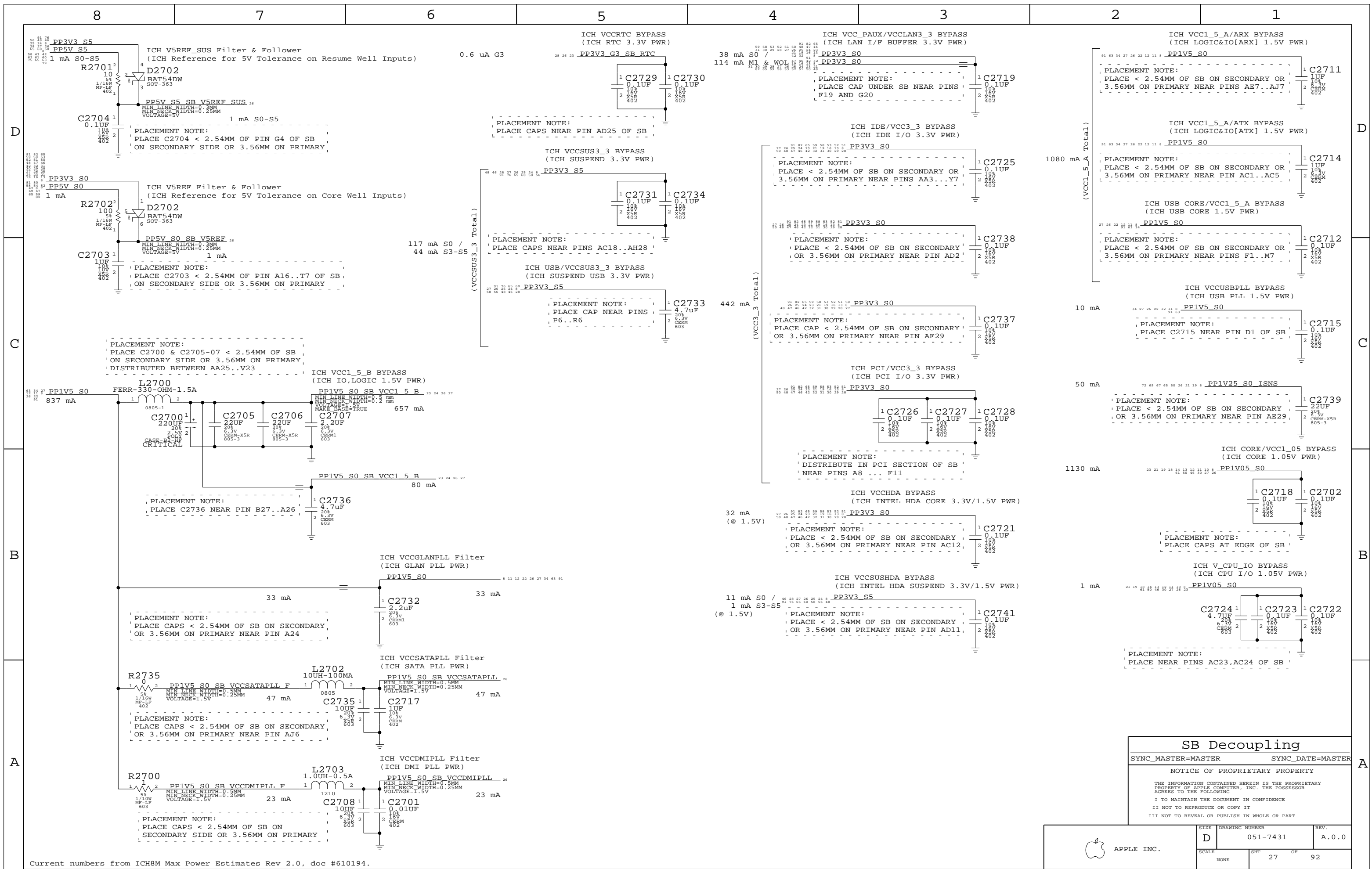
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	26	92



SB Decoupling

SYNC_MASTER=MASTER SYNC_DATE=MASTER

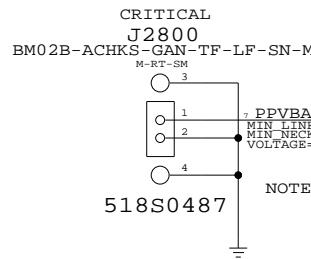
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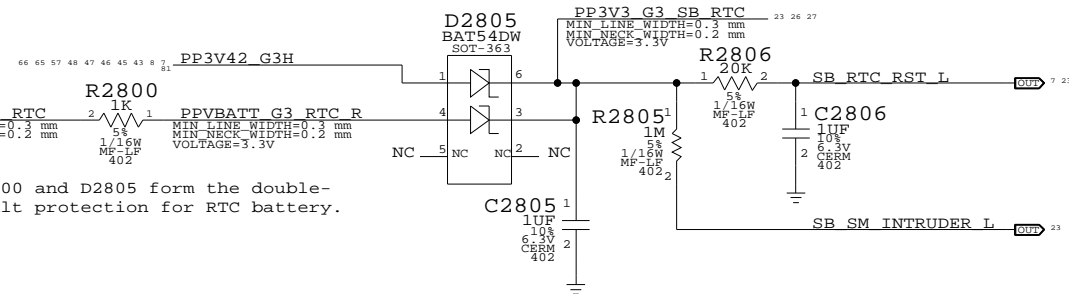
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	27	92	

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

Coin-Cell Connector

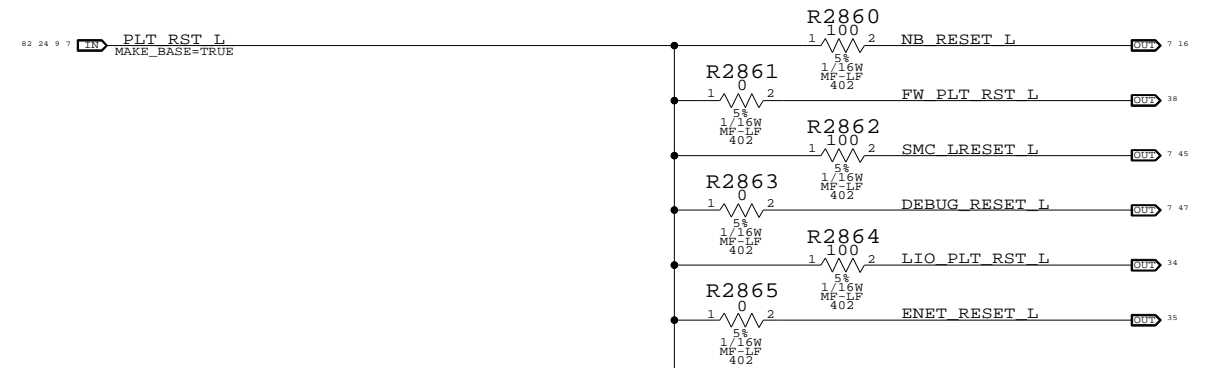


RTC Power Sources

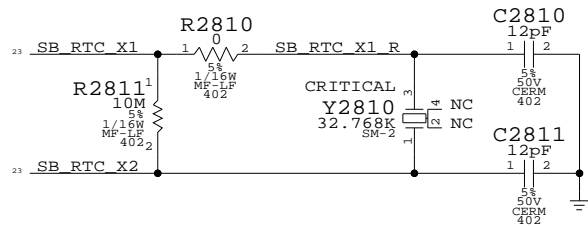


Platform Reset Connections

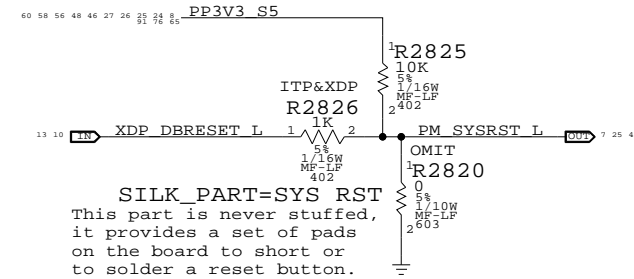
Unbuffered



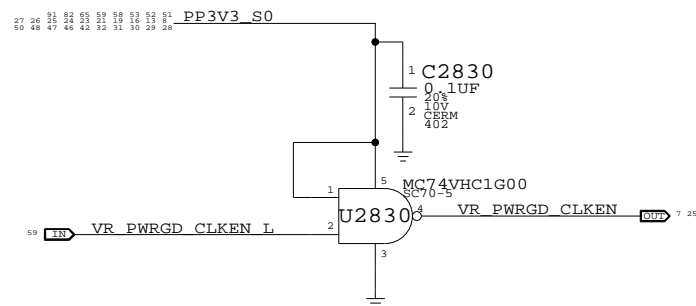
SB RTC Crystal



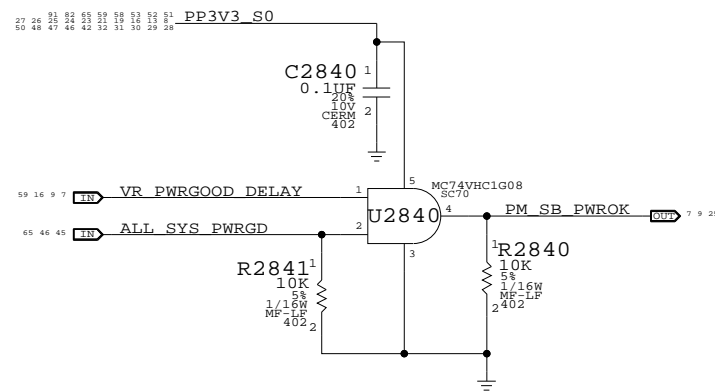
System Reset "Button"



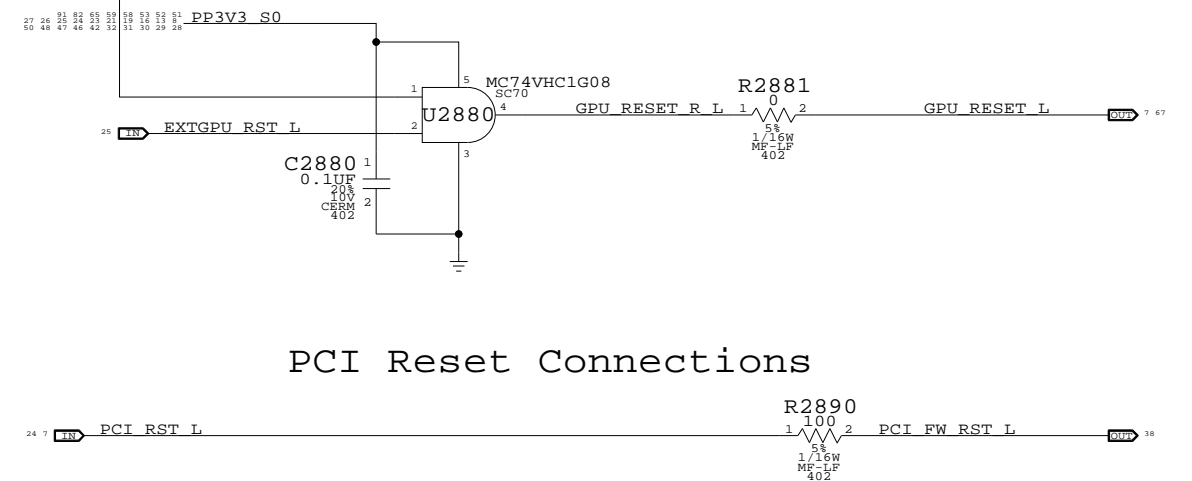
VRMPWRGD Inverter



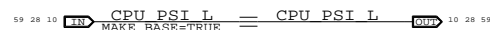
PWROK Circuit



PCI Reset Connections



CPU VCore ForcePSI



SB Misc

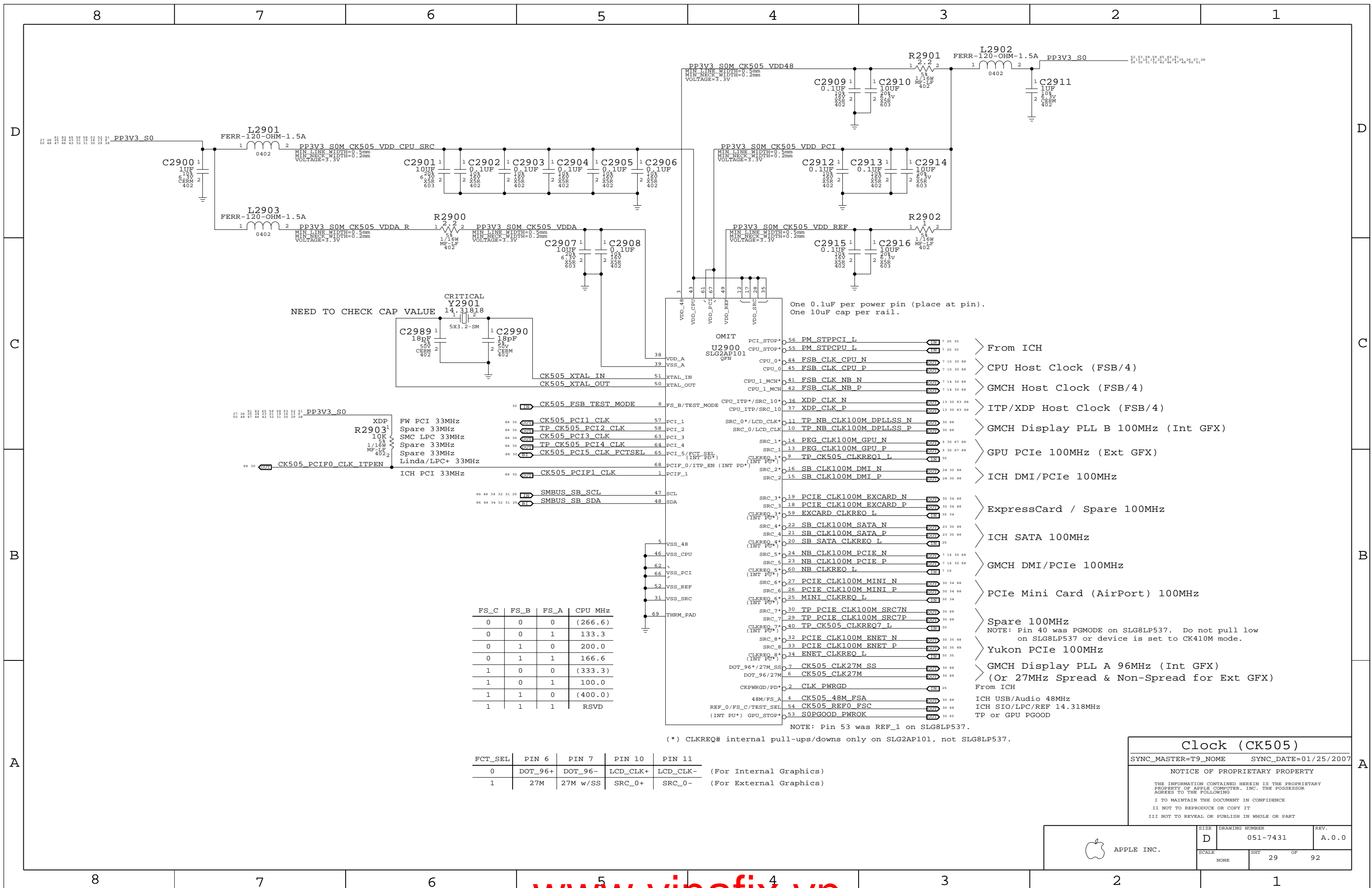
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	28	92



NEED TO CHECK CAP VALUE

One 0.1uF per power pin (place at pin).
One 10uF cap per rail.

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

NOTE: Pin 53 was REF_1 on SLG8LP537.

(*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

Clock (CK505)

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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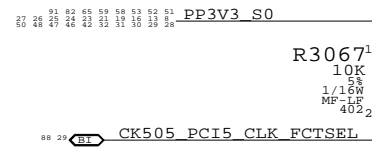
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	29	92	

CLK Termination

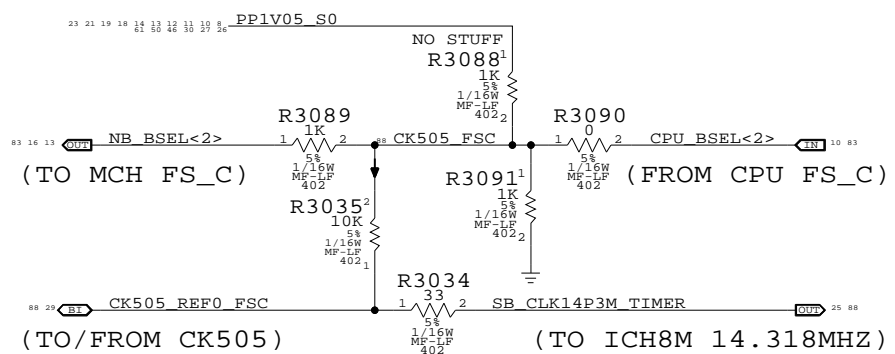
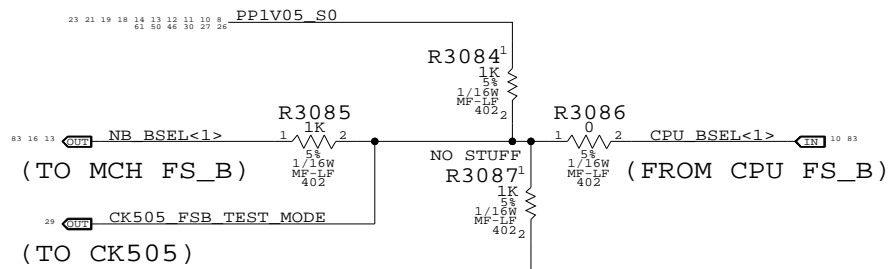
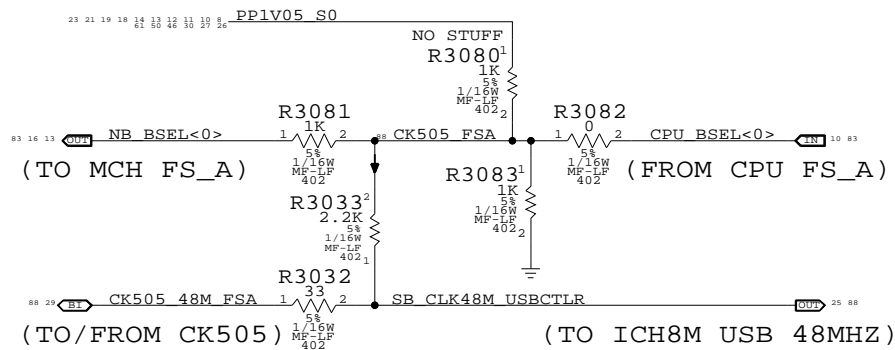
(Note: HOST/SRC/GFX clock termination removed. Silago SL8GLP536 or equiv. support only)

CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)

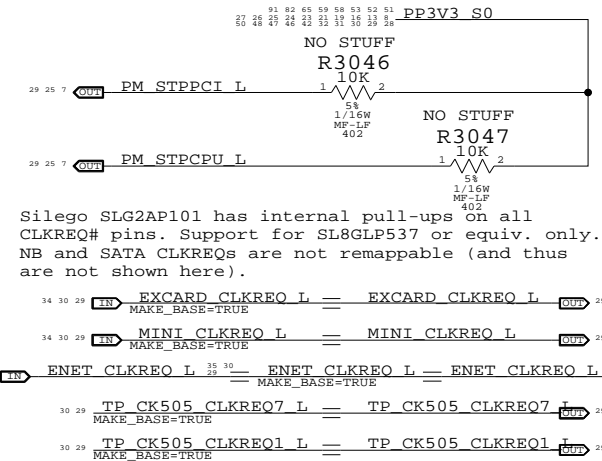


FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

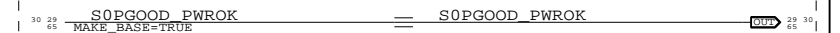
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLKREQ Controls

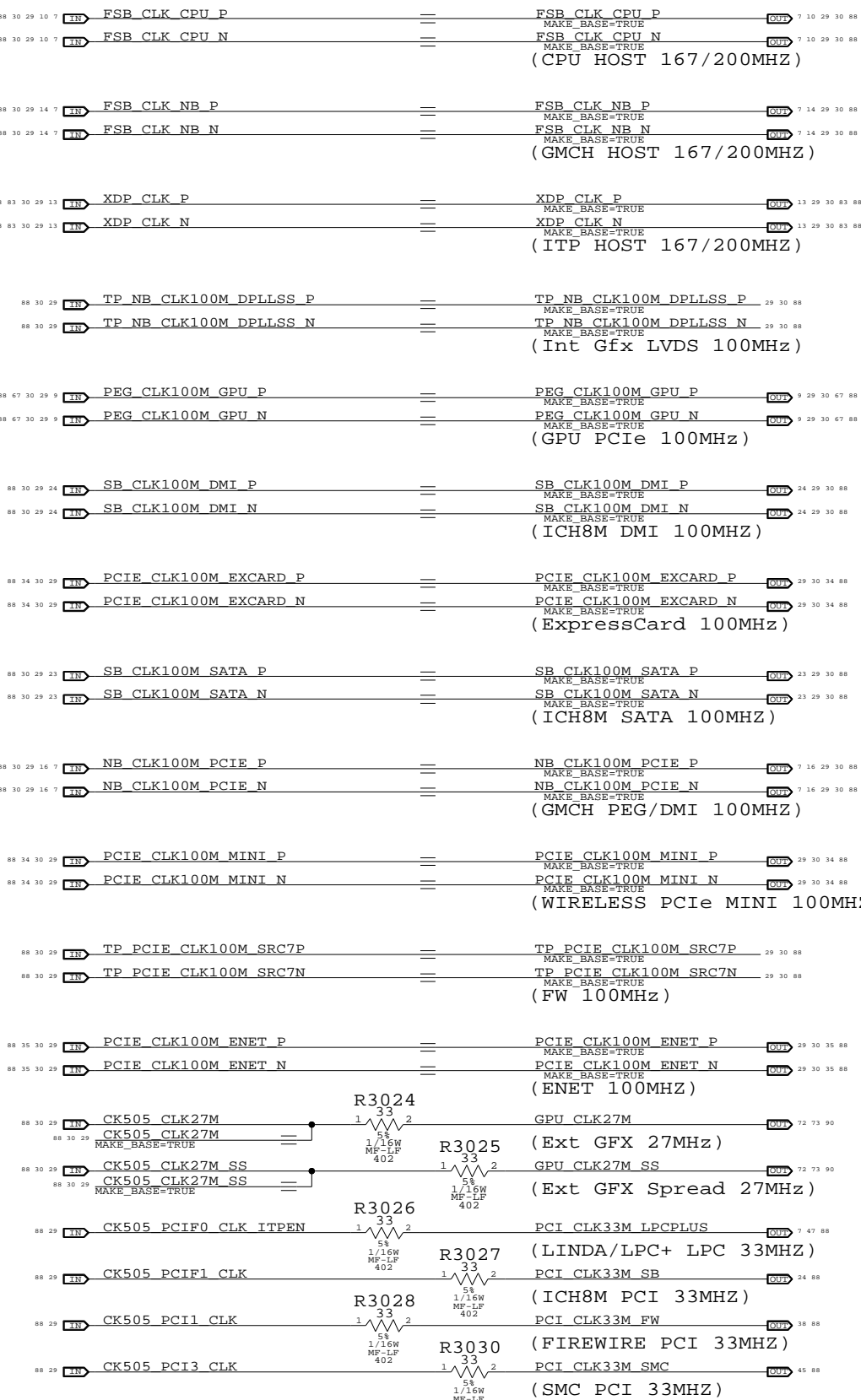
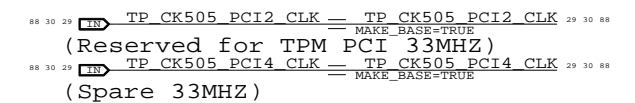


Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	30	92

Page Notes

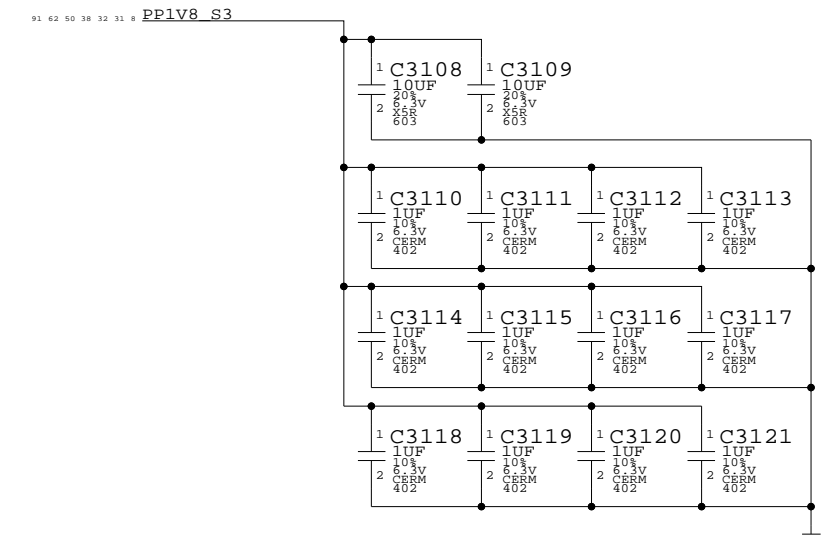
Power aliases required by this page:
 - =PP1V8_S3M_MEM_A
 - =PP0V9_S3M_MEM_DIMMVREFA
 - =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

BOM options provided by this page:
 (NONE)

"Factory" (thru-hole) slot

DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector A
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	31	92	

Page Notes

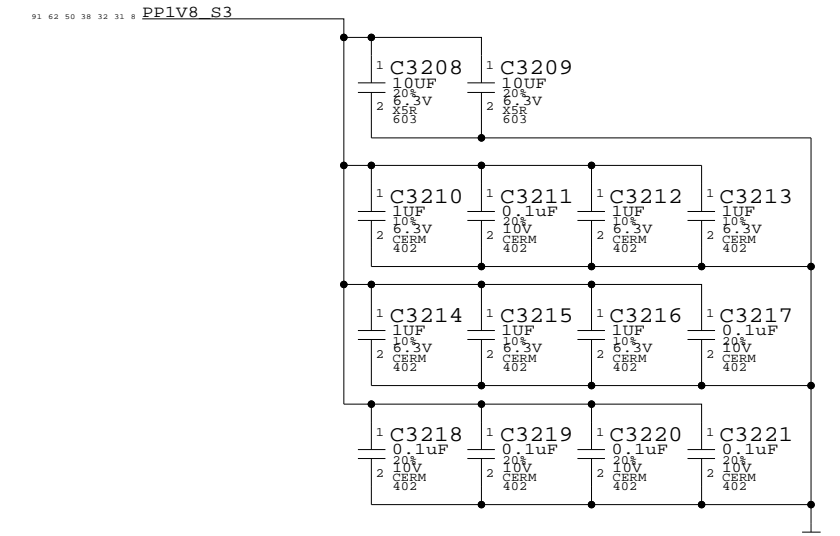
Power aliases required by this page:
 - =PP1V8_S3M_MEM_B
 - =PP0V9_S3M_MEM_DIMMVREFB
 - =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

BOM options provided by this page:
 (NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	32	92

8

7

6

5

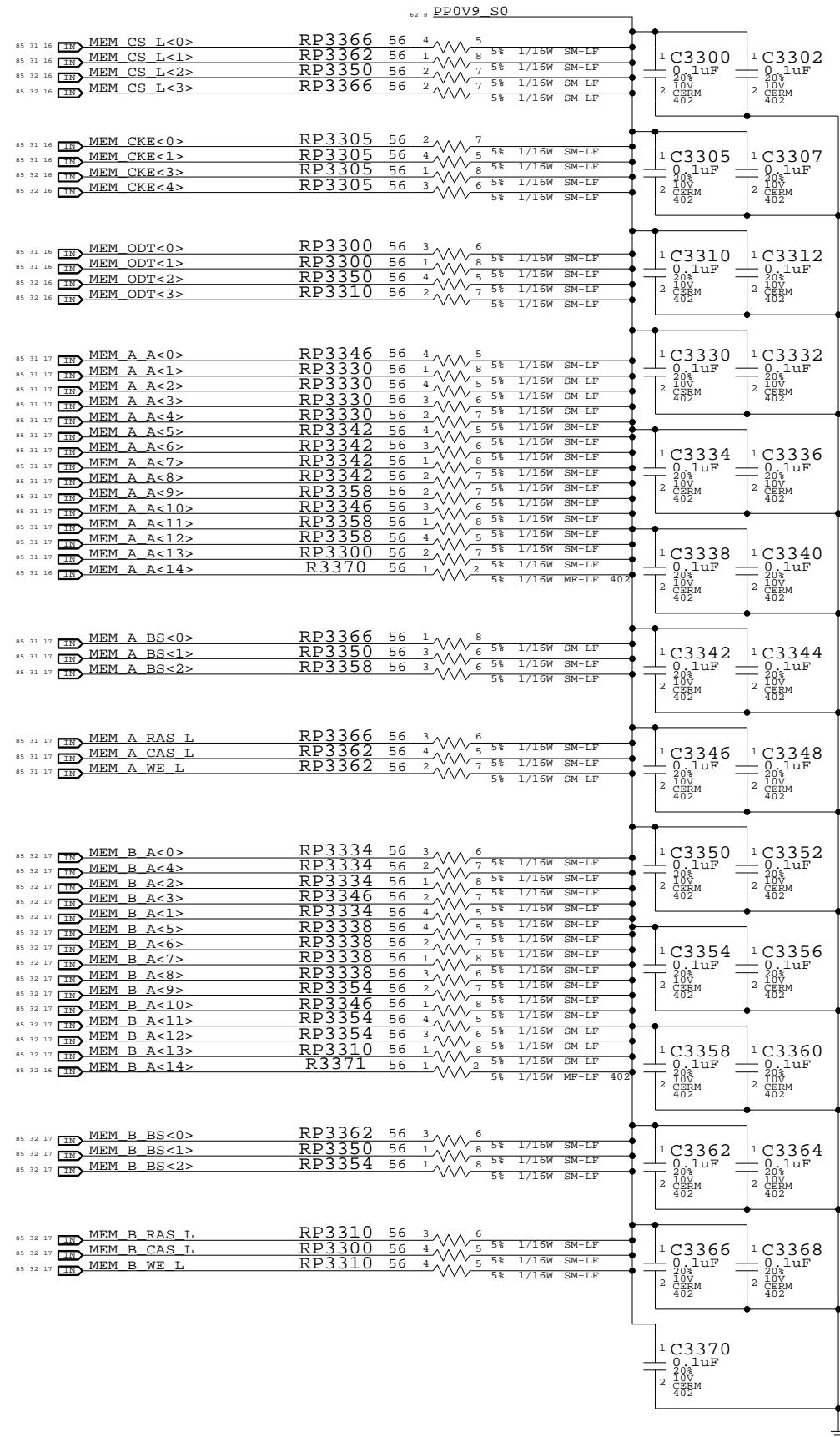
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector

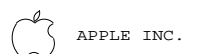


Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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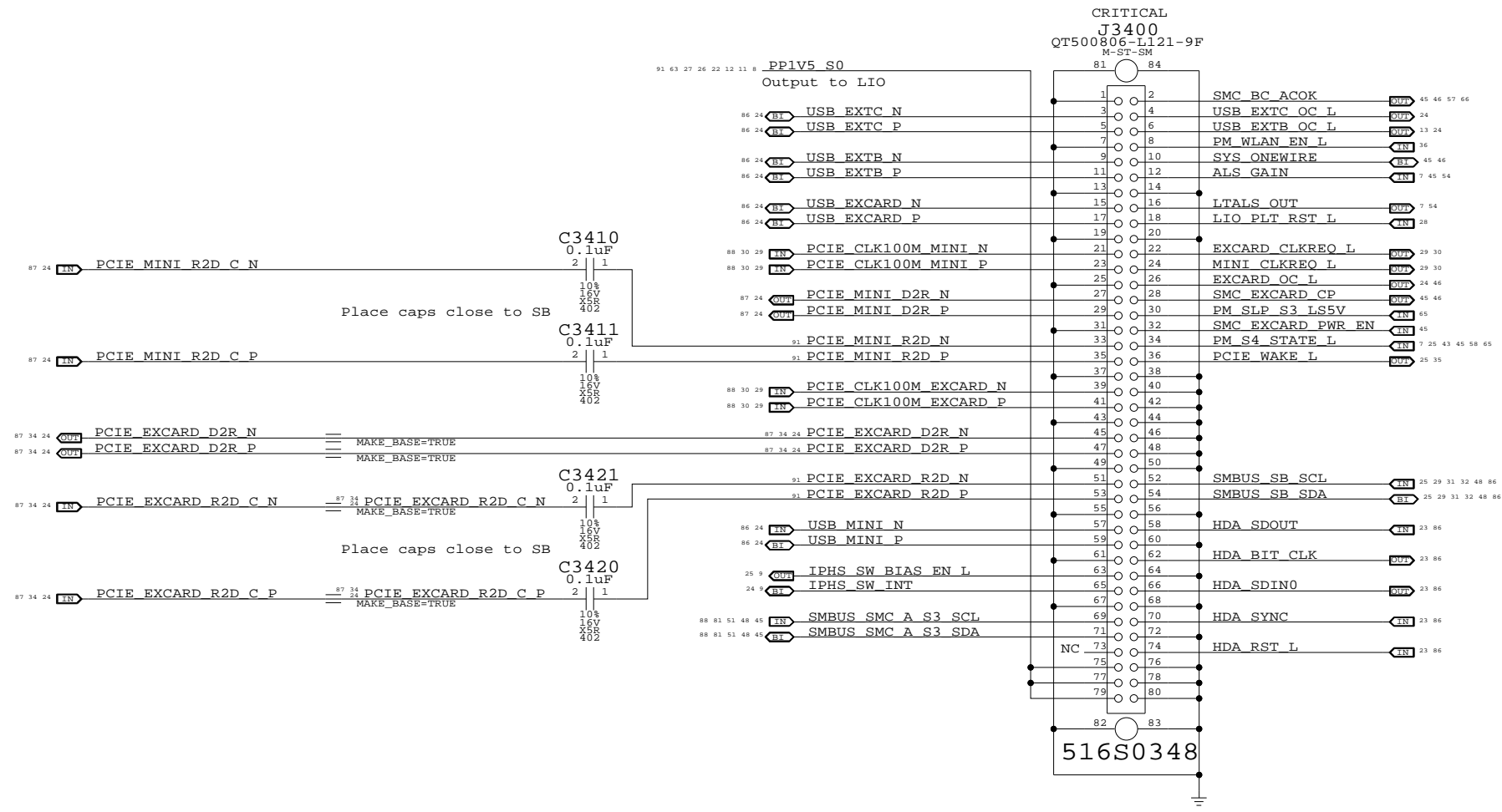
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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	33	92

Left I/O Board Connector



Left I/O Board Connector
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT 34 OF 92		
NONE			

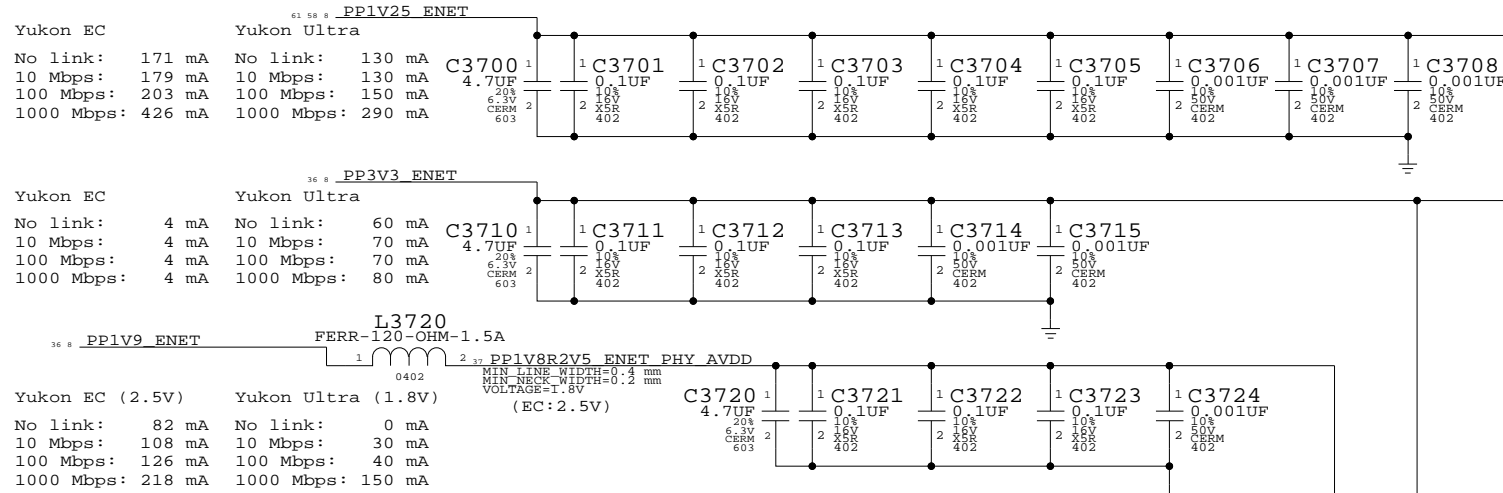
Page Notes

Power aliases required by this page:
 - =PP3V3_ENET_PHY (EC / Ultra)
 - =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
 - =YUKON_EC_PP2V5_ENET (2.5V / GND)
 - =PP1V2_ENET_PHY

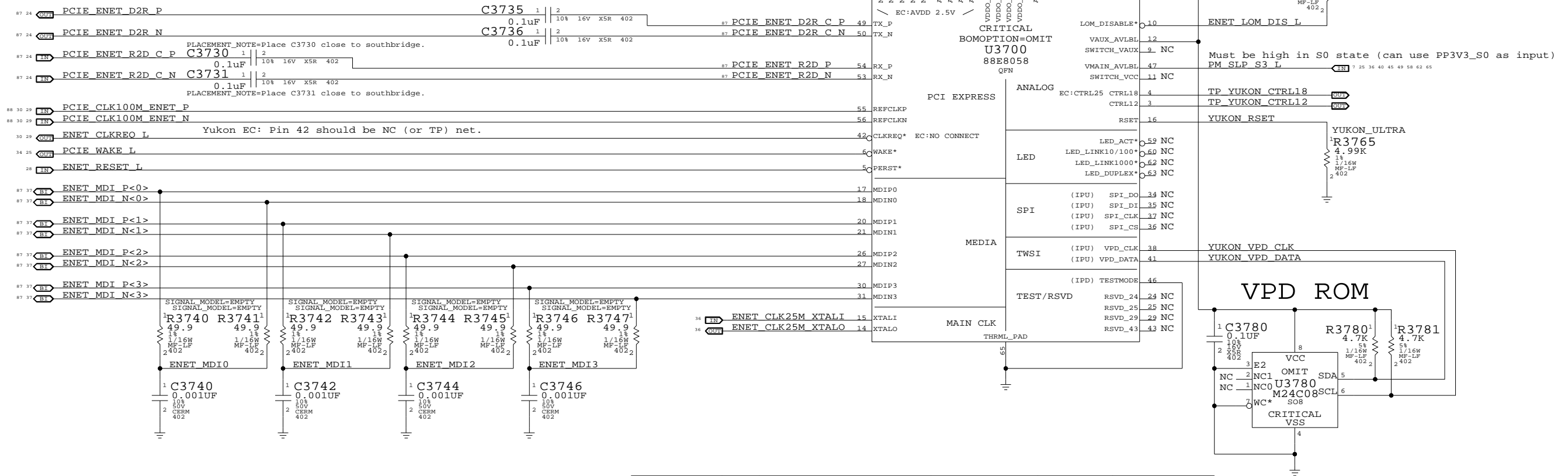
Signal aliases required by this page:
 - =ENET_CLKREQ_L (NC/TP for Yukon EC)
 - =ENET_VMAIN_AVLBLE (See note by pin)

BOM options provided by this page:
 YUKON_EC - Selects Yukon EC RSET value.
 YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



GND
 Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
 Yukon Ultra: Alias to GND



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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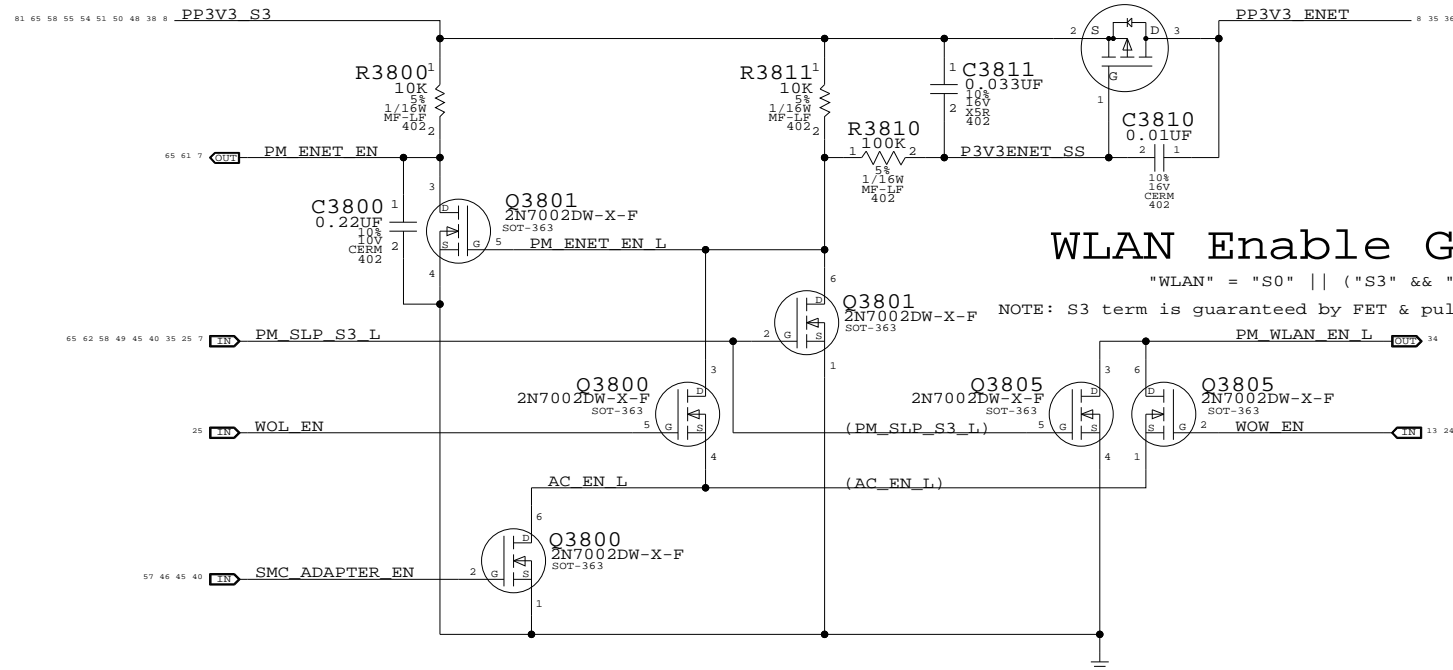
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	35	92

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
 NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

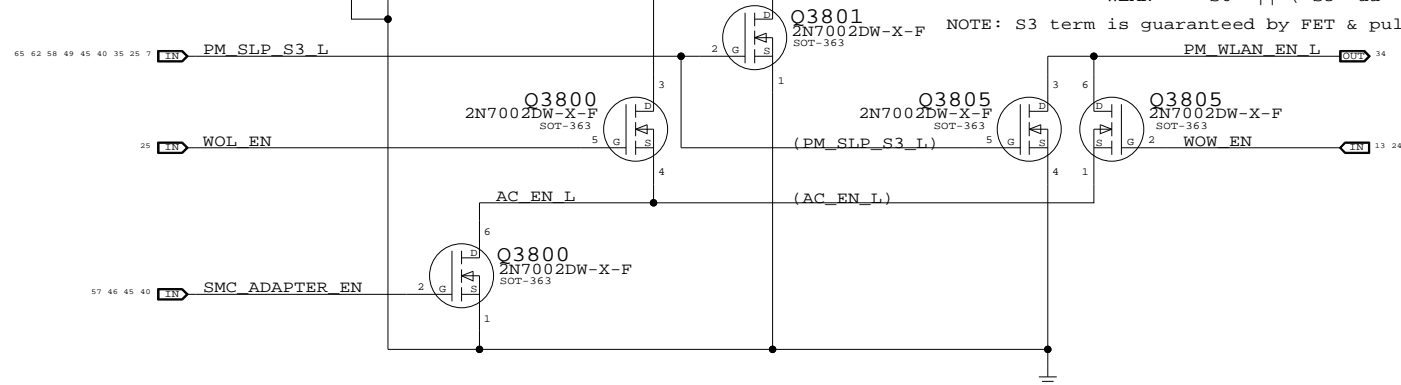


3.3V ENET FET

CRITICAL
 Q3810
 NTR4101P
 SOT-23

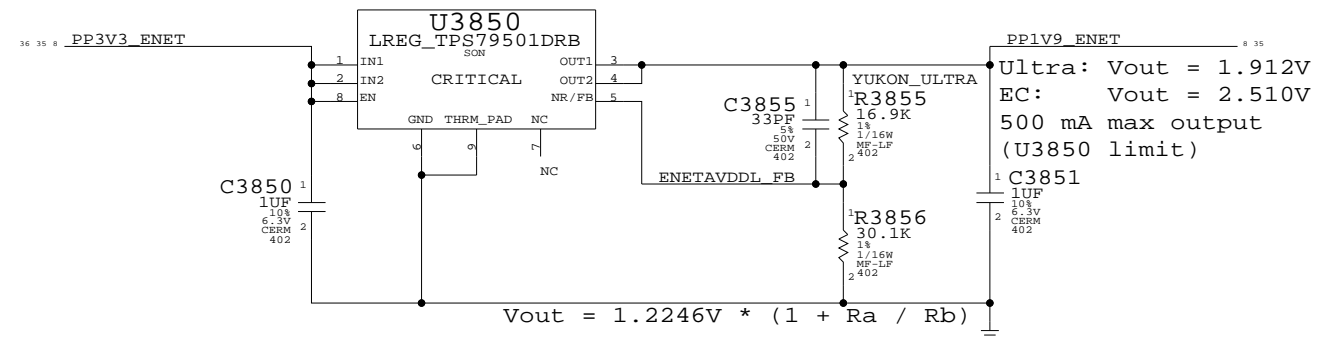
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")
 NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



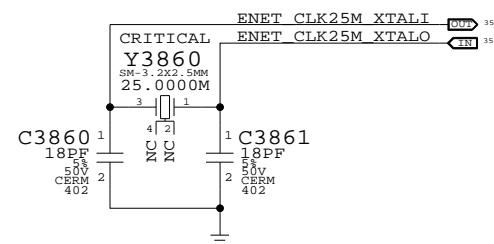
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
 Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

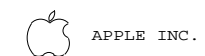
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D	051-7431	A.0.0
SCALE	SHT	OF
NONE	36	92

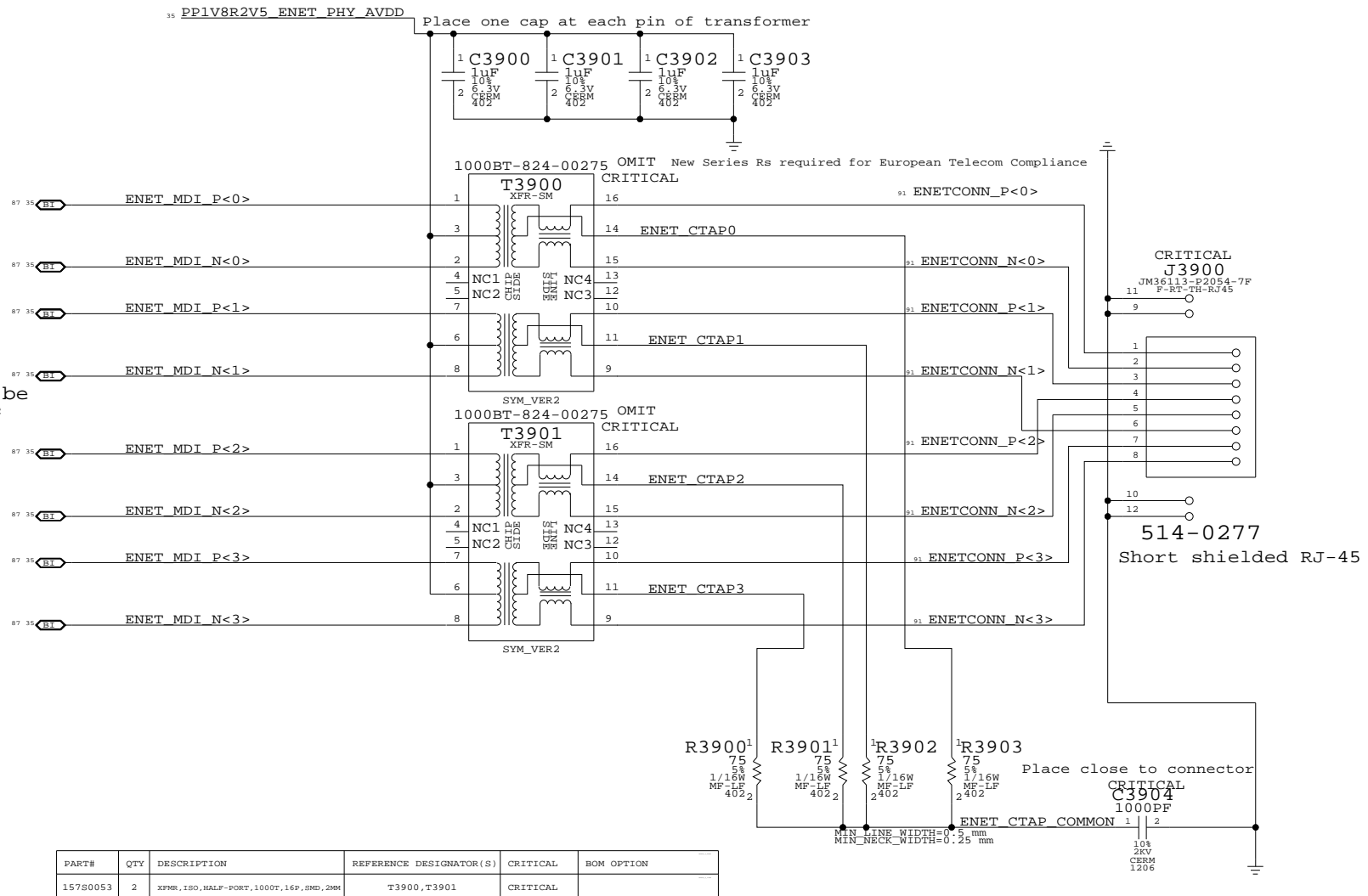
Page Notes

Power aliases required by this page:
 - =GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Transformers should be mirrored on opposite sides of the board



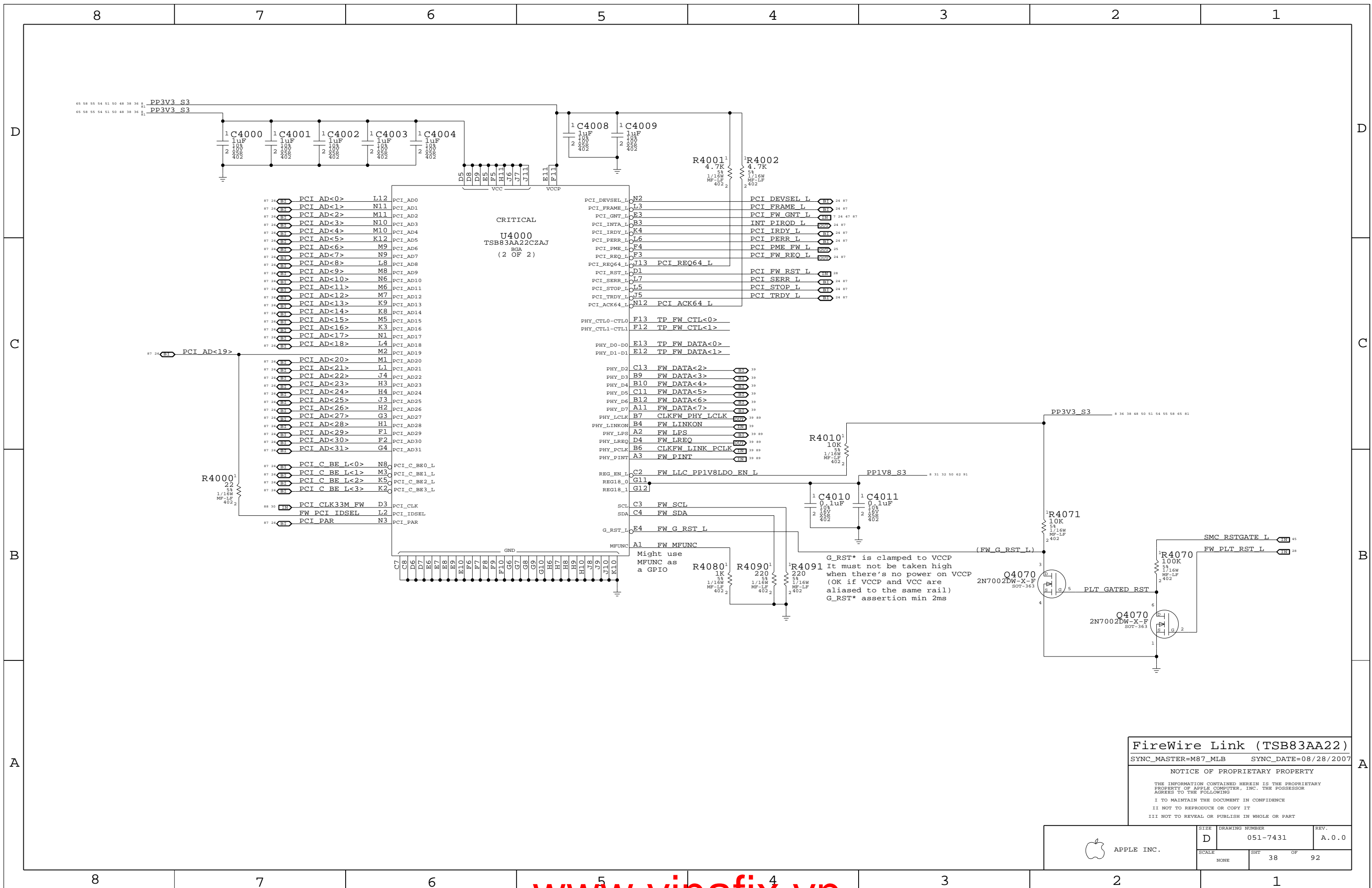
Ethernet Connector
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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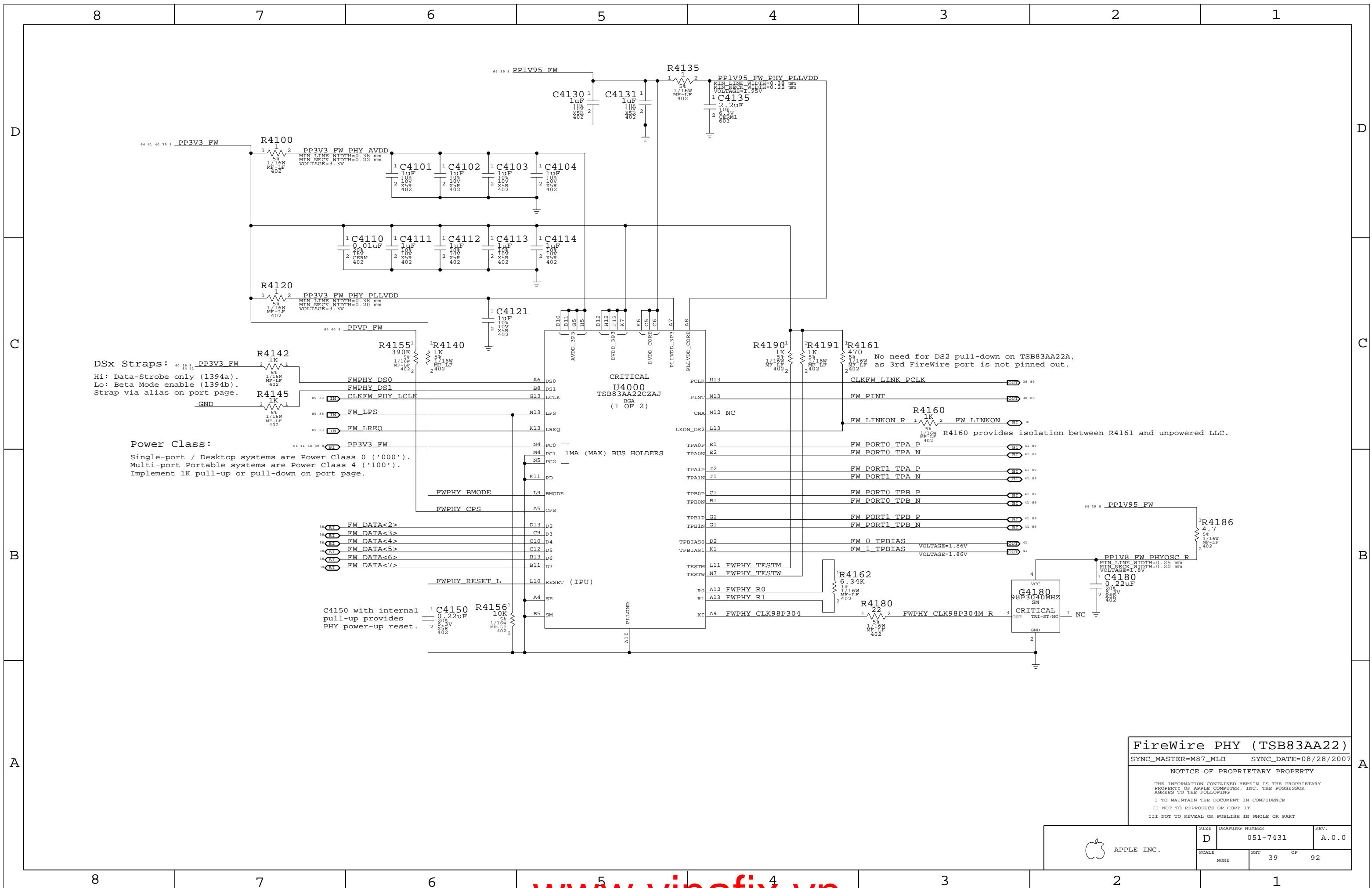
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	37	92	



FireWire Link (TSB83AA22)
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE		SHT	OF
NONE		38	92



PP3V3 FW

DSx Straps:
 Hi: Data-Strobe only (1394a).
 Lo: Beta Mode enable (1394b).
 Strap via alias on port page.

Power Class:

Single-port / Desktop systems are Power Class 0 ('000').
 Multi-port Portable systems are Power Class 4 ('100').
 Implement 1K pull-up or pull-down on port page.

C4150 with internal pull-up provides PHY power-up reset.

No need for DS2 pull-down on TSB83AA22A, as 3rd FireWire port is not pinned out.

R4160 provides isolation between R4161 and unpowered LLC.

FireWire PHY (TSB83AA22)
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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	D	051-7431	A.0.0
SCALE	SHT 39 OF 92		
NONE			

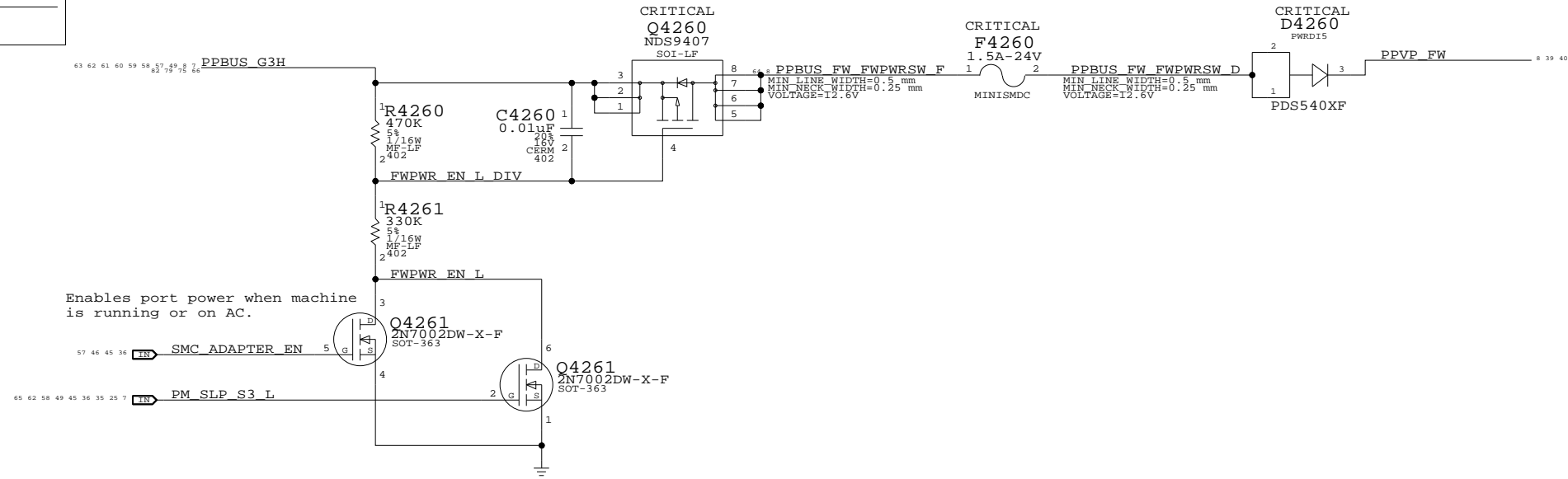
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - FW_PORT_FAULT_PU

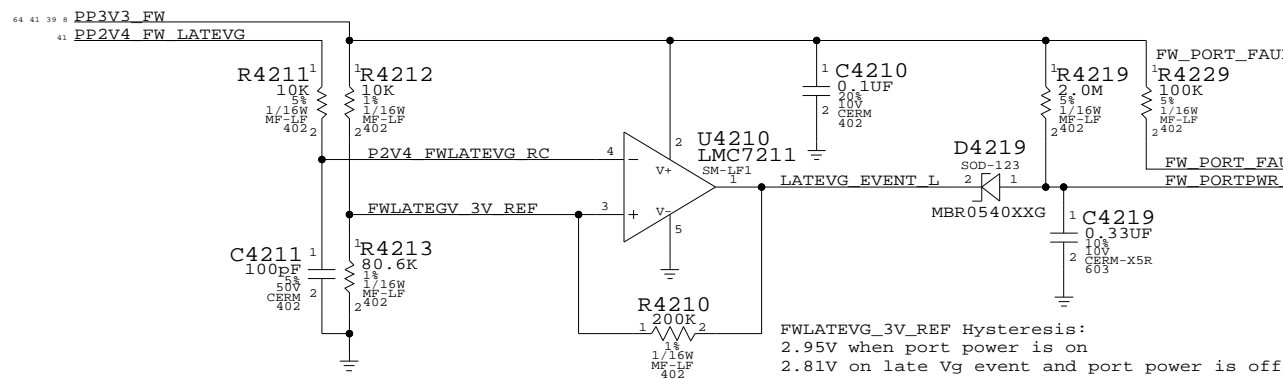
FireWire Port Power Switch



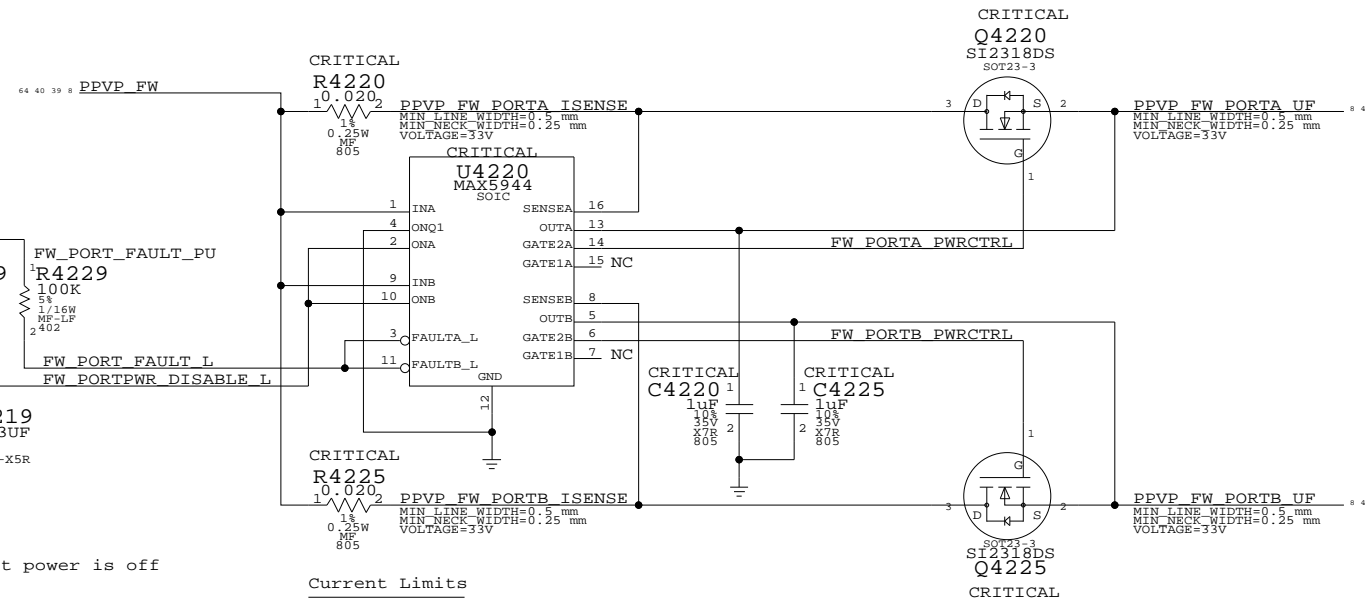
Enables port power when machine is running or on AC.

Current Limit/Active Late-VG Protection

Late-VG Event Detection



FWLATEVG_3V_REF Hysteresis:
 2.95V when port power is on
 2.81V on late Vg event and port power is off



Current Limits
 0.020 ohm => 2.4A
 0.025 ohm => 2A
 0.030 ohm => 1.66A (Ideal)
 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	40	92

Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT0
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG
 - =GND_CHASSIS_FW_PORT0L
 - =GND_CHASSIS_FW_PORT0U
 - =GND_CHASSIS_FW_PORT1
 - =GND_CHASSIS_FW_PORT1U
 - =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
 (NONE)
 NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

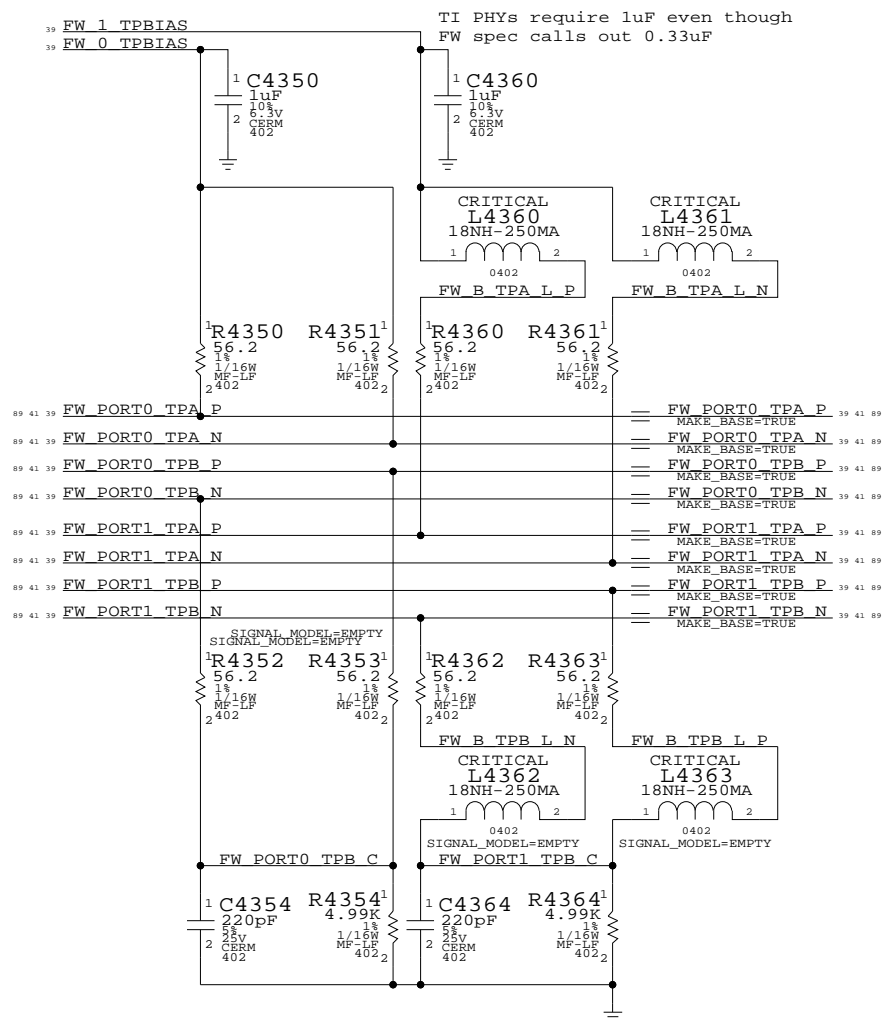
FireWire PHY Config Straps

Configures PHY for:

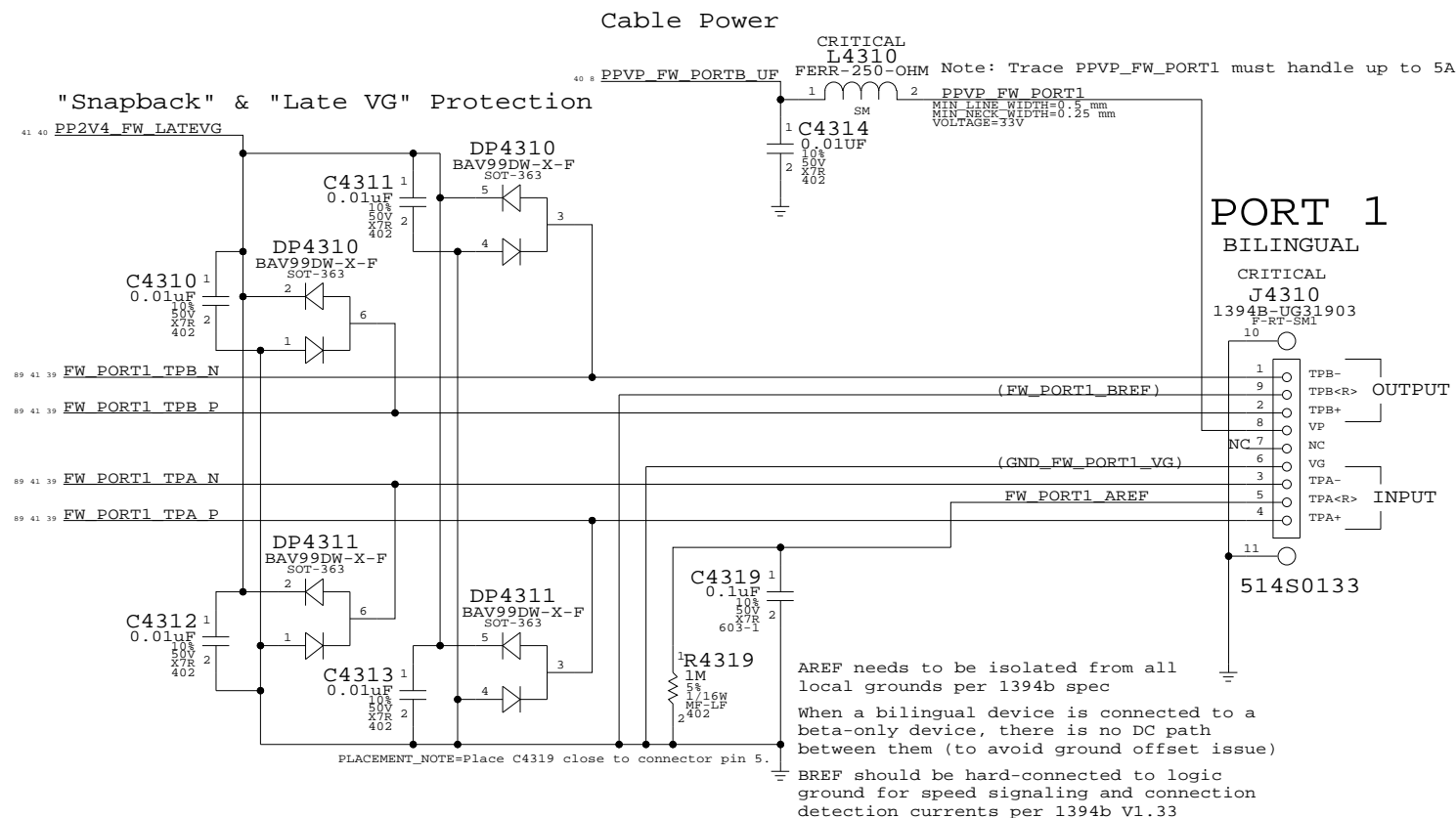
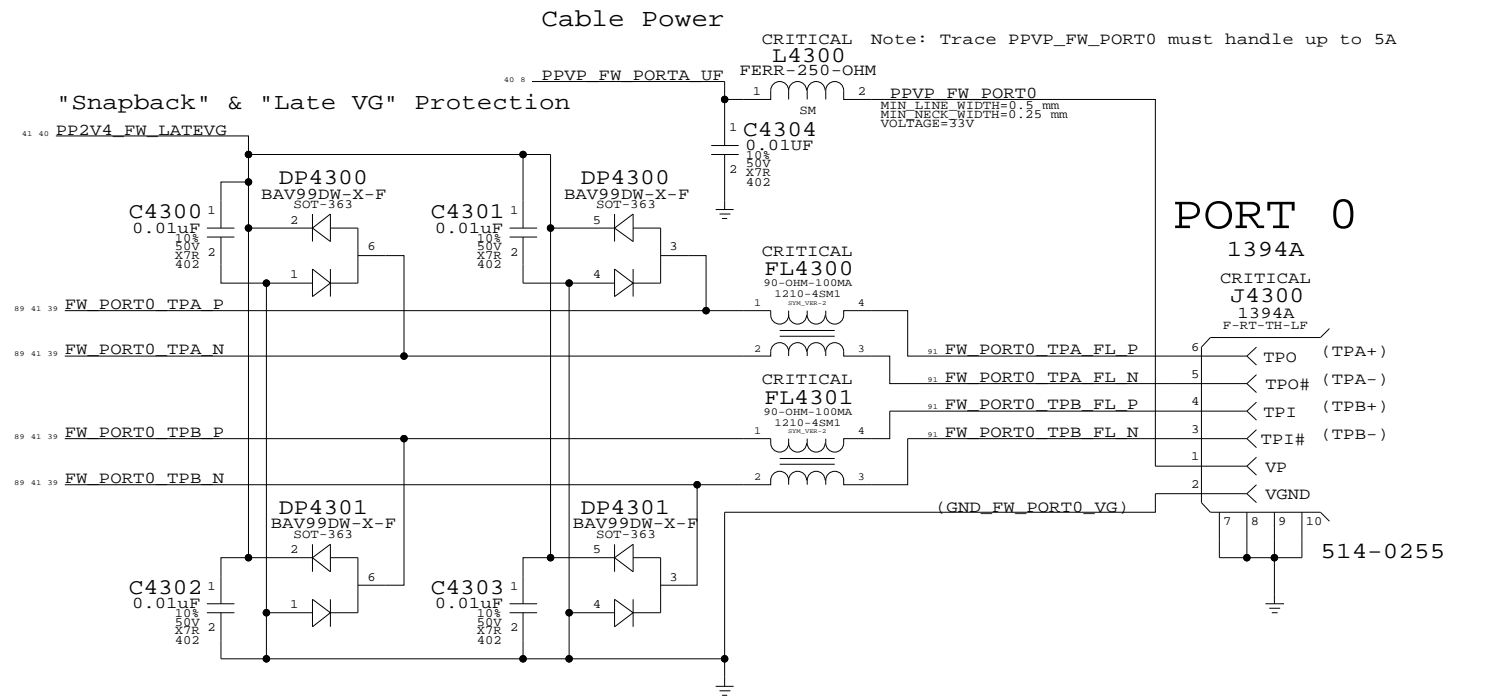
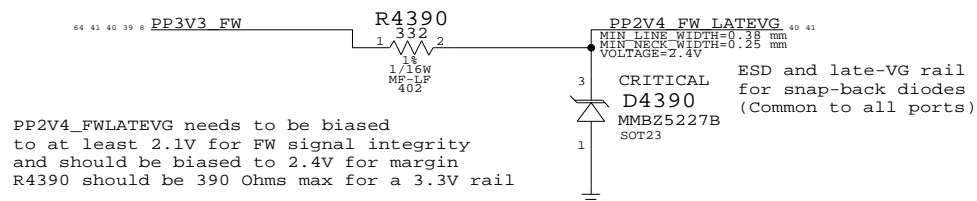
- 2-port Portable Power Class (4) PP3V3 FW
- Port "0" Data-Strobe only (1394A) PP3V3 FW
- Port "1" Bilingual (1394B) GND

Termination

Place close to FireWire PHY



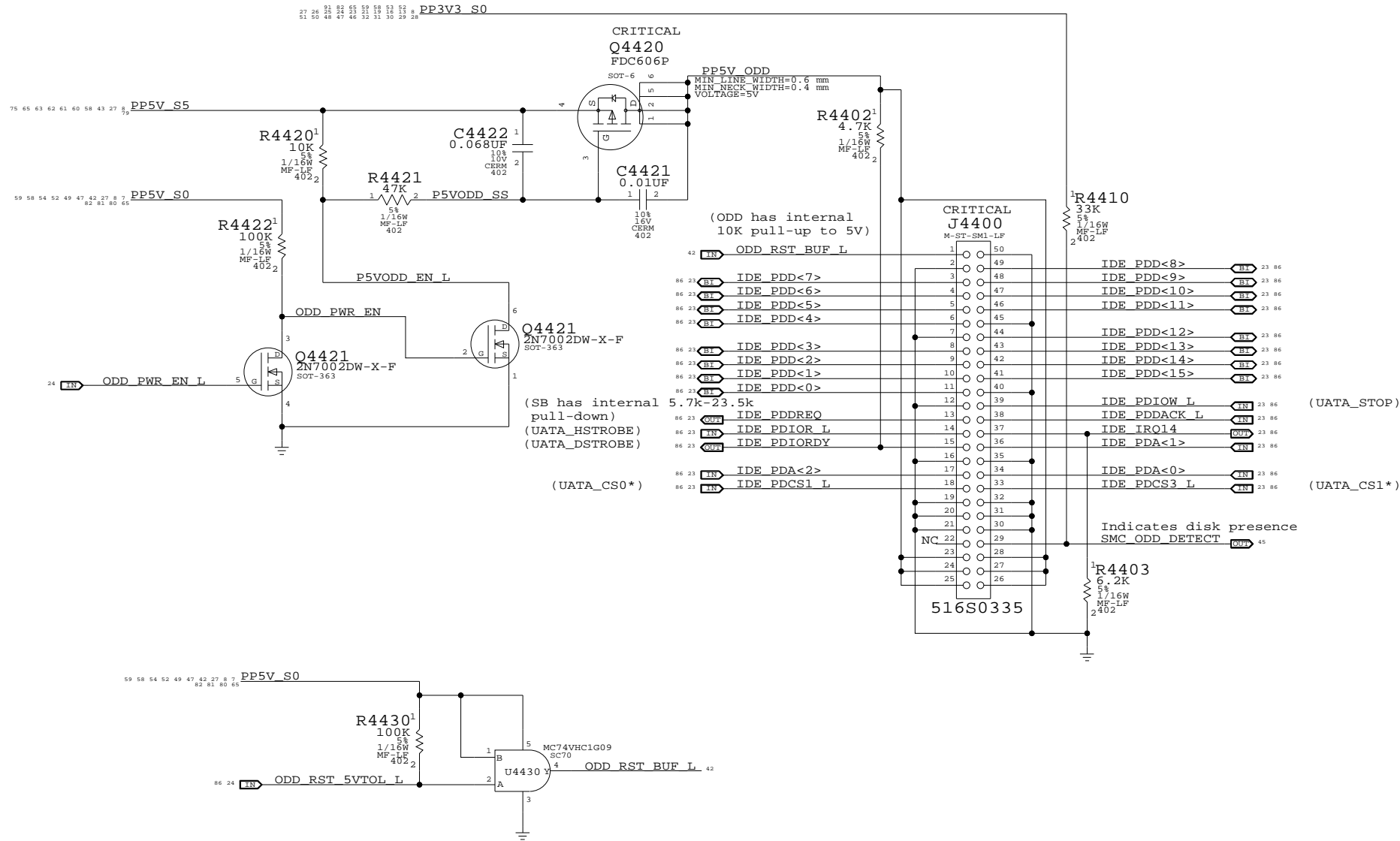
Late-VG Protection Power



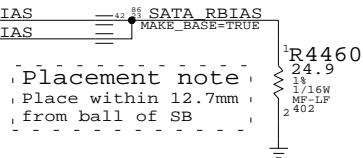
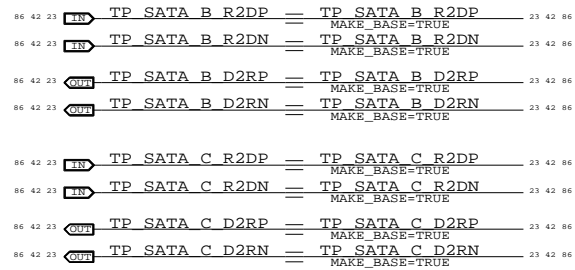
FireWire Ports		
SYNC_MASTER=M87_MLB	SYNC_DATE=08/28/2007	
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	D	051-7431	A.0.0
SCALE	SHT	OF	92
NONE	41		

IDE (ODD) Connector



Unused SATA Ports



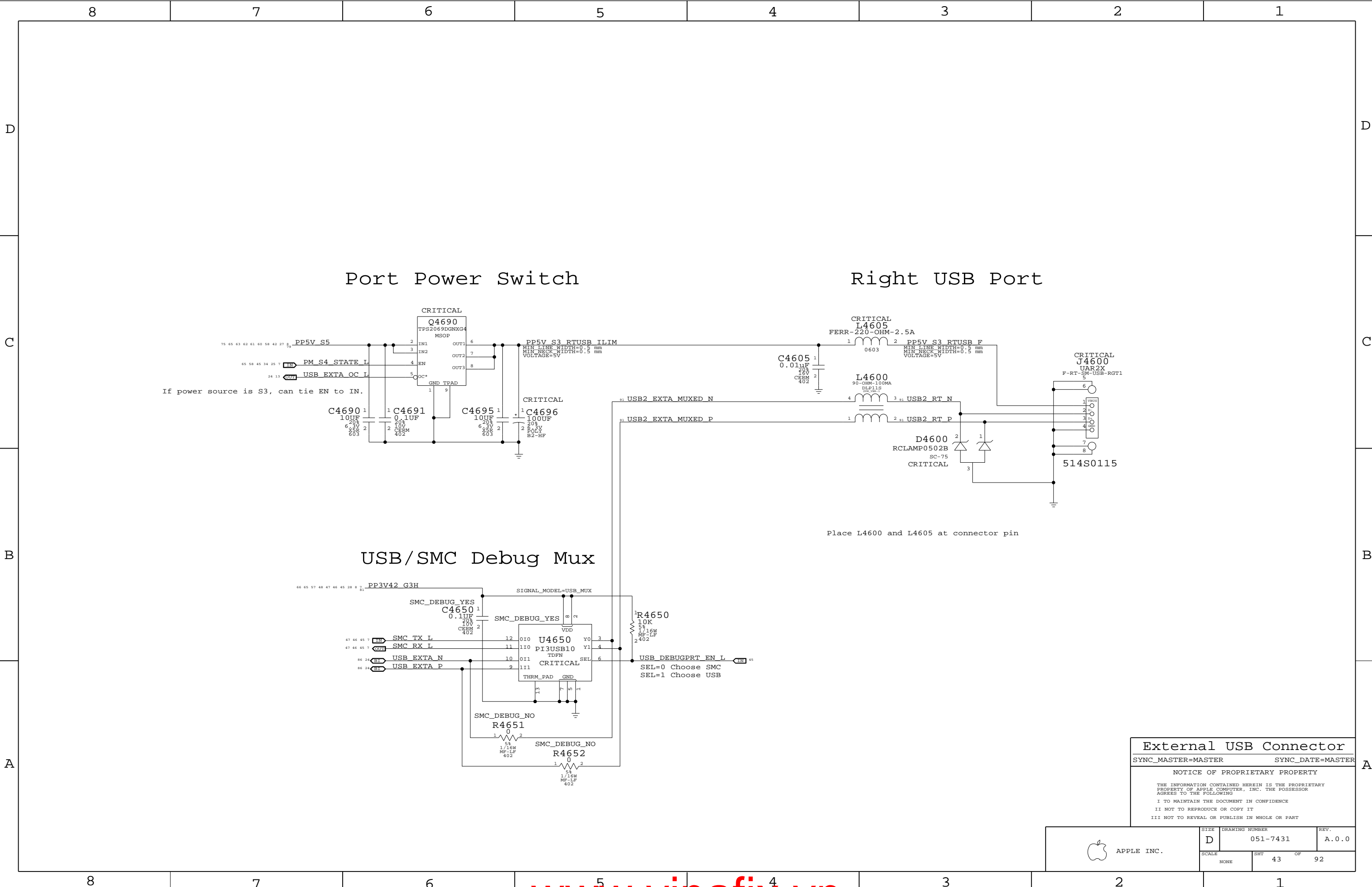
PATA Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT 42 OF 92		
NONE			



Port Power Switch

Right USB Port

USB/SMC Debug Mux

Place L4600 and L4605 at connector pin

External USB Connector

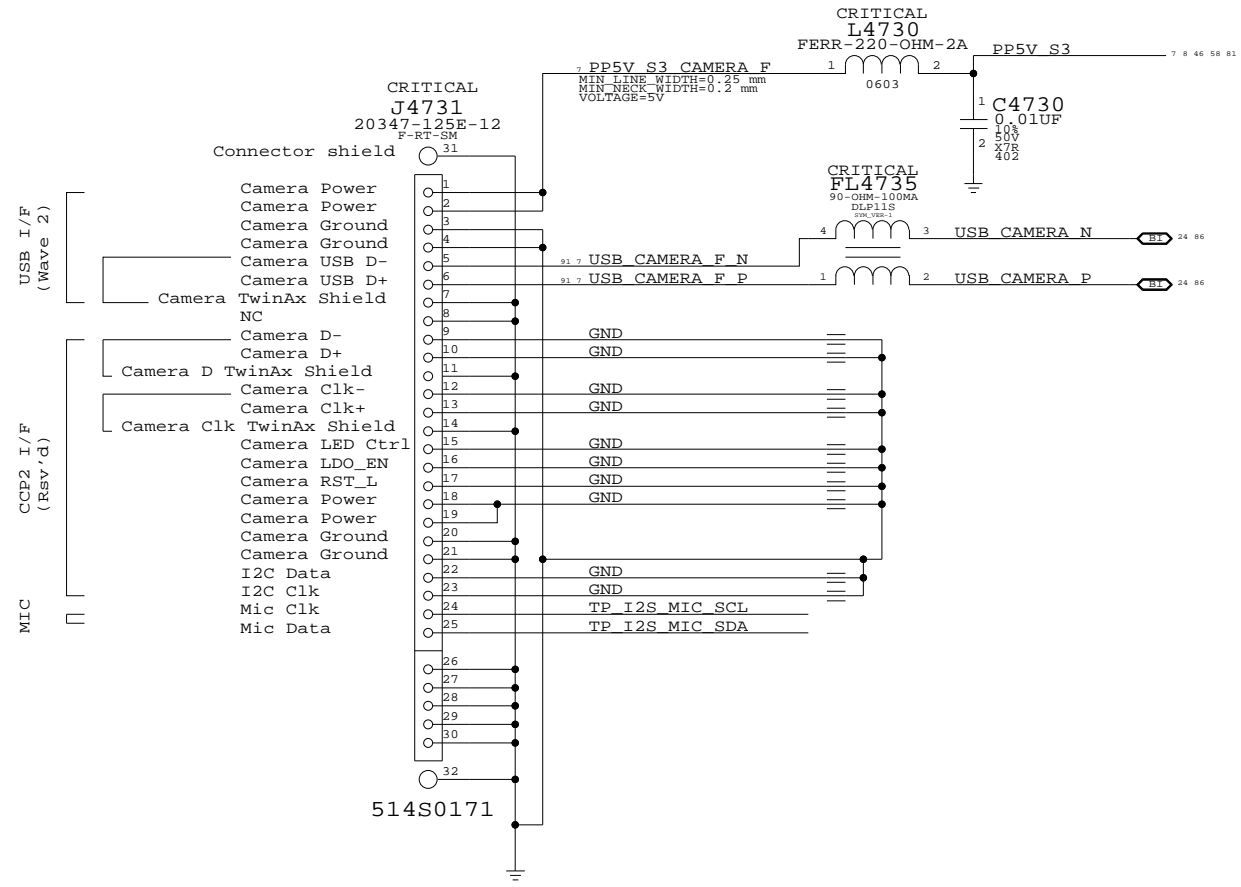
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT 43	OF 92

Left Clutch Barrel Interconnect



Left Clutch Barrel Interconnect
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT		OF
NONE	44		92

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

C

B

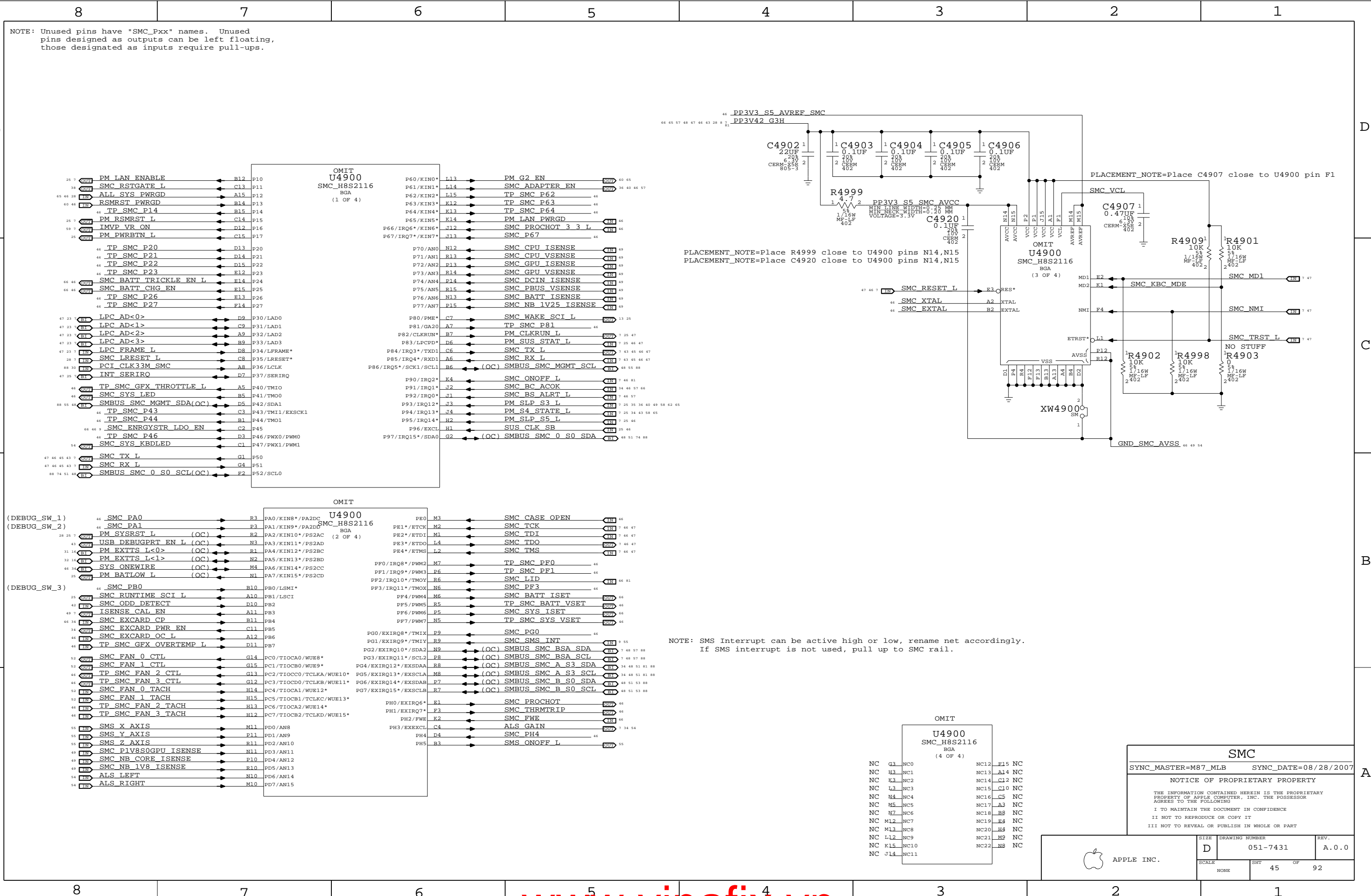
A

D

C

B

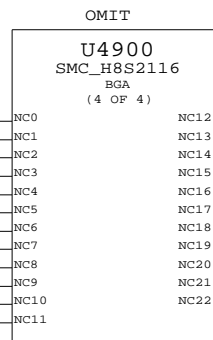
A



PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
 PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

PLACEMENT_NOTE=Place C4907 close to U4900 pin F1

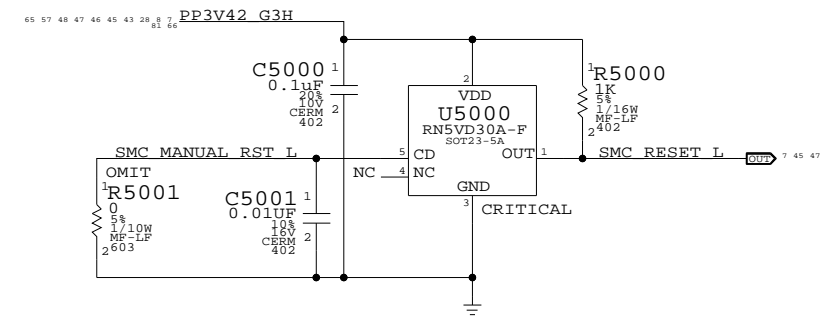
NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.



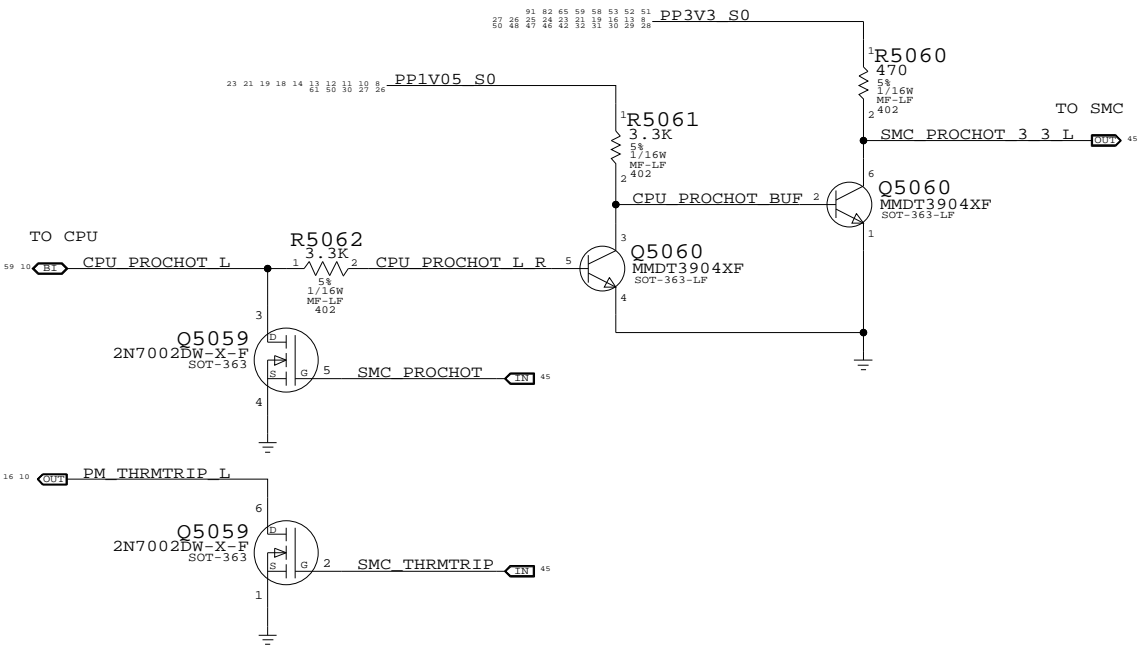
SMC
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	92
NONE	45		

SMC Reset "Button" / Brownout Detect

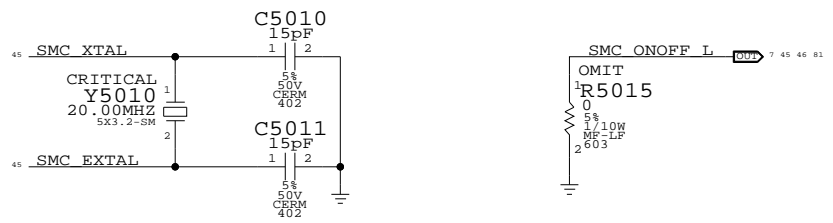


SMC FSB to 3.3V Level Shifting

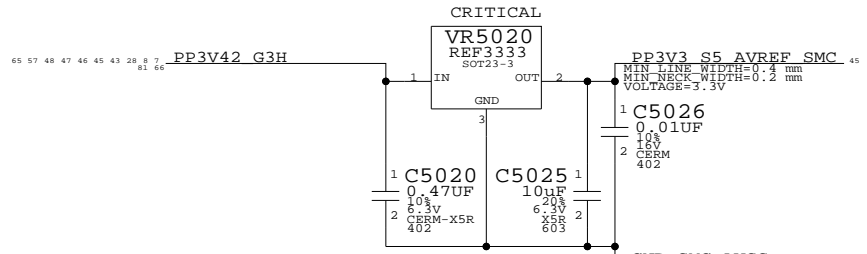


TP_SMC_FAN_2_CTL	==	TP_SMC_FAN_2_CTL	45 46
TP_SMC_FAN_2_TACH	==	TP_SMC_FAN_2_TACH	45 46
TP_SMC_FAN_3_CTL	==	TP_SMC_FAN_3_CTL	45 46
TP_SMC_FAN_3_TACH	==	TP_SMC_FAN_3_TACH	45 46
TP_SMC_GFX_OVERTEMP_L	==	TP_SMC_GFX_OVERTEMP_L	45 46
TP_SMC_GFX_THROTTLE_L	==	TP_SMC_GFX_THROTTLE_L	45 46
TP_SMC_BATT_VSET	==	TP_SMC_BATT_VSET	45 46
TP_SMC_SYS_VSET	==	TP_SMC_SYS_VSET	45 46
TP_SMC_P14	==	TP_SMC_P14	45 46
TP_SMC_P20	==	TP_SMC_P20	45 46
TP_SMC_P21	==	TP_SMC_P21	45 46
TP_SMC_P22	==	TP_SMC_P22	45 46
TP_SMC_P23	==	TP_SMC_P23	45 46
TP_SMC_P26	==	TP_SMC_P26	45 46
TP_SMC_P27	==	TP_SMC_P27	45 46
TP_SMC_P43	==	TP_SMC_P43	45 46
TP_SMC_P44	==	TP_SMC_P44	45 46
TP_SMC_P46	==	TP_SMC_P46	45 46
TP_SMC_P62	==	TP_SMC_P62	45 46
TP_SMC_P63	==	TP_SMC_P63	45 46
TP_SMC_P64	==	TP_SMC_P64	45 46
TP_SMC_P81	==	TP_SMC_P81	45 46
TP_SMC_PFO	==	TP_SMC_PFO	45 46
TP_SMC_PF1	==	TP_SMC_PF1	45 46

SMC Crystal Circuit Debug Power "Button"

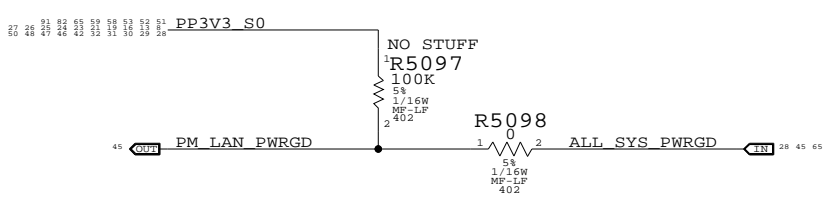


SMC AVREF Supply



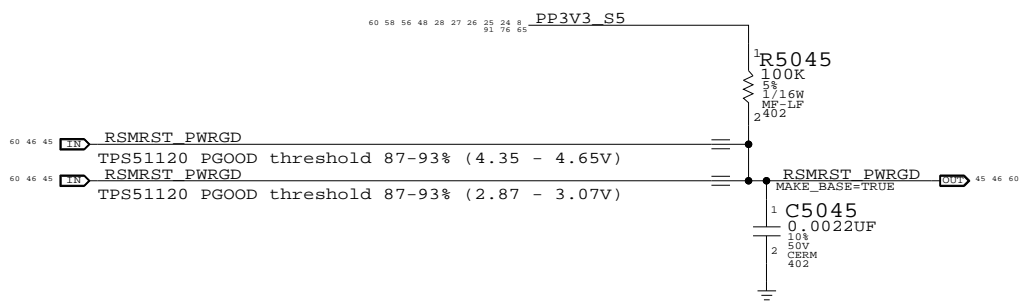
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Interail ISL60002-33

LAN PWRGD Circuit

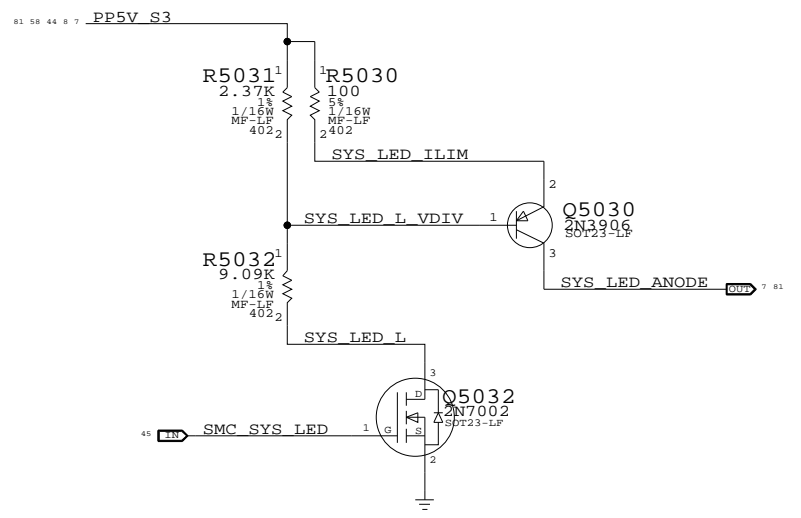


S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



System (Sleep) LED Circuit

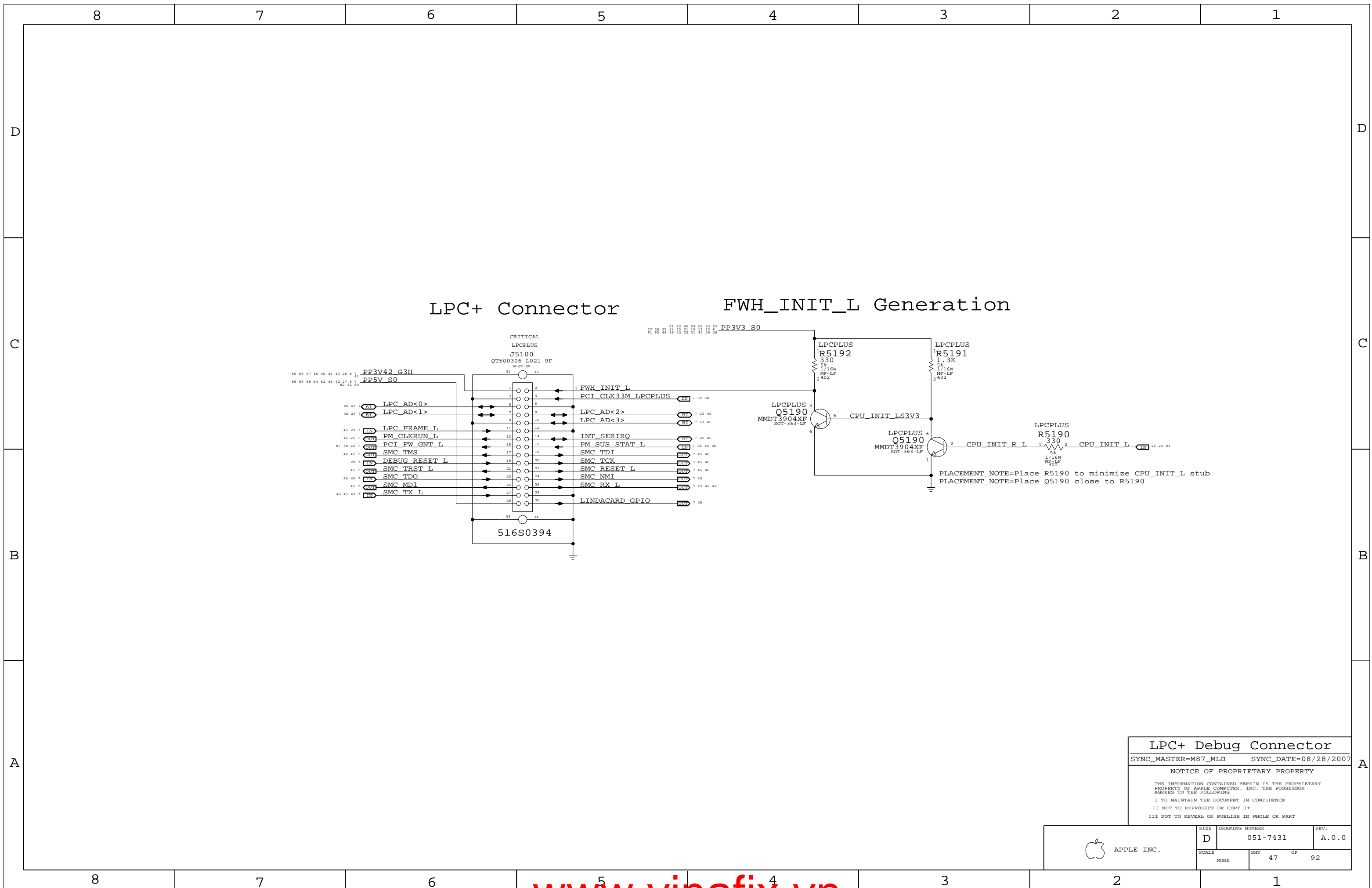


SMC_PA0	R5091	100K	1	5%	1/16W MF-LF 402
SMC_PA1	R5092	100K	1	5%	1/16W MF-LF 402
SMC_PB0	R5093	100K	1	5%	1/16W MF-LF 402
SMC_ONOFF_L	R5070	10K	1	5%	1/16W MF-LF 402
SMC_LID	R5071	100K	1	5%	1/16W MF-LF 402
SMC_FWE	R5072	10K	1	5%	1/16W MF-LF 402
SMC_TX_L	R5073	10K	1	5%	1/16W MF-LF 402
SMC_RX_L	R5074	100K	1	5%	1/16W MF-LF 402
ONEWIRE_PU					
SYS_ONEWIRE	R5075	2.0K	1	5%	1/16W MF-LF 402
SMC_BS_ALRT_L	R5076	100K	1	5%	1/16W MF-LF 402
SMC_TMS	R5077	10K	1	5%	1/16W MF-LF 402
SMC_TDO	R5078	10K	1	5%	1/16W MF-LF 402
SMC_TDI	R5079	10K	1	5%	1/16W MF-LF 402
SMC_TCK	R5080	10K	1	5%	1/16W MF-LF 402
SMC_P67	R5094	10K	1	5%	1/16W MF-LF 402
SMC_P63	R5081	10K	1	5%	1/16W MF-LF 402
SMC_P60	R5096	10K	1	5%	1/16W MF-LF 402
SMC_PH4	R5082	10K	1	5%	1/16W MF-LF 402
SMC_BATT_TRICKLE_EN_L	R5083	10K	1	5%	1/16W MF-LF 402
SMC_BATT_CHG_EN	R5084	10K	1	5%	1/16W MF-LF 402
SMC_ADAPTER_EN	R5085	10K	1	5%	1/16W MF-LF 402
SMC_CASE_OPEN	R5086	10K	1	5%	1/16W MF-LF 402
SMC_BC_ACOK	R5087	470K	1	5%	1/16W MF-LF 402
SMC_EXCARD_CP	R5088	10K	1	5%	1/16W MF-LF 402
PM_SUS_STAT_L	R5089	100K	1	5%	1/16W MF-LF 402
PM_SLP_S5_L	R5090	100K	1	5%	1/16W MF-LF 402

SMC Support
 SYNC_MASTER=M87_MLB SYNC_DATE=10/15/2007

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	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	46	92	



LPC+ Connector

FWH_INIT_L Generation

LPC+ Debug Connector

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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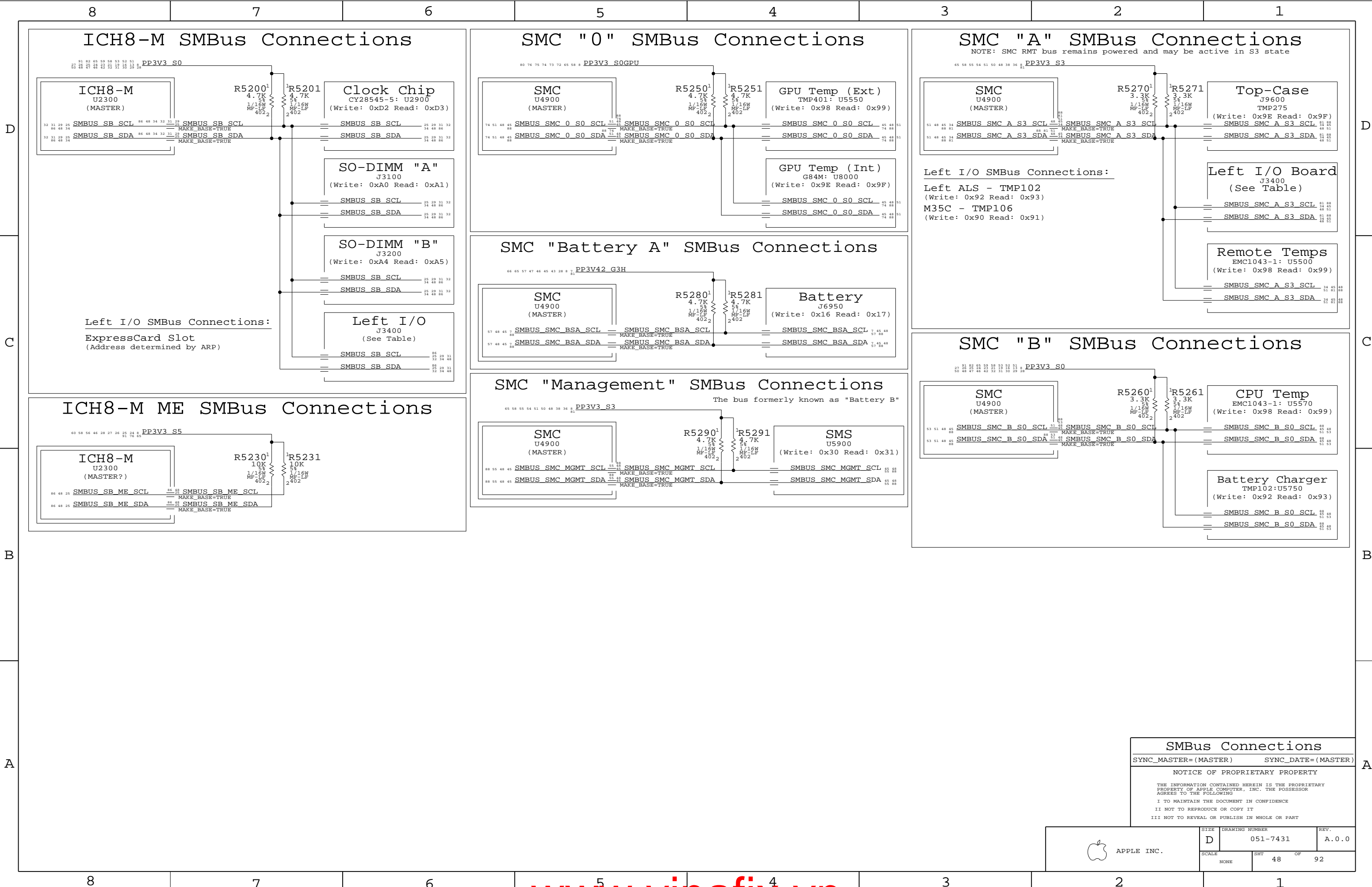
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APPLE INC.

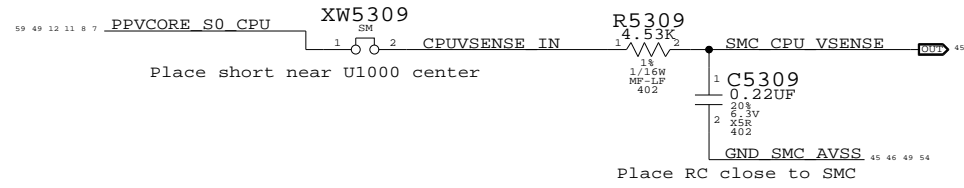
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	47	92



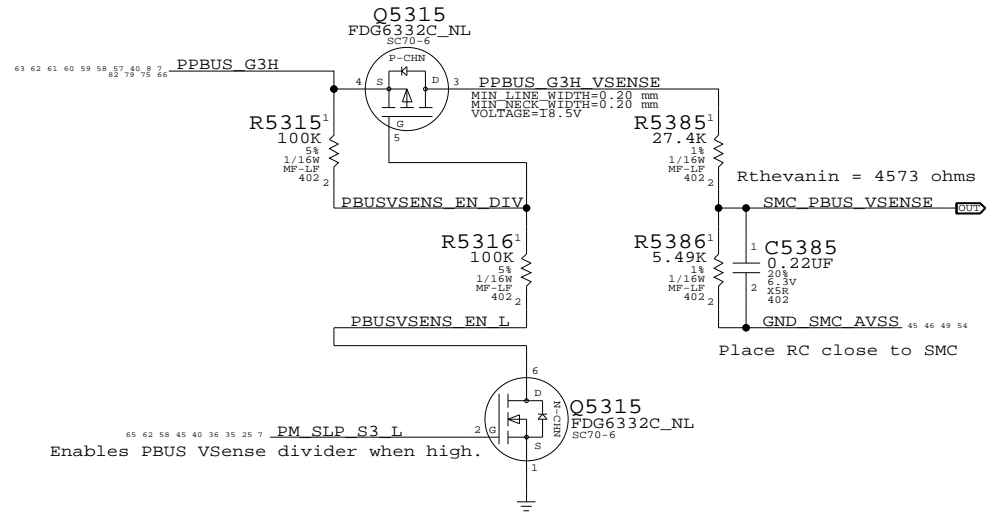
SMBus Connections
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT		OF
NONE	48		92

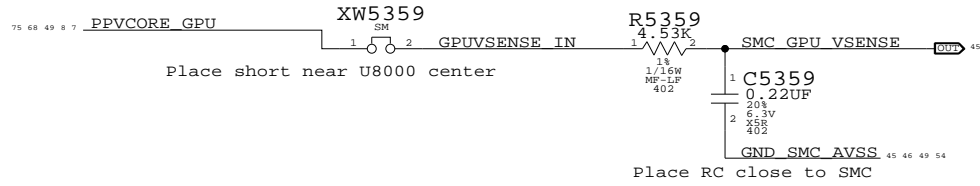
CPU Voltage Sense / Filter



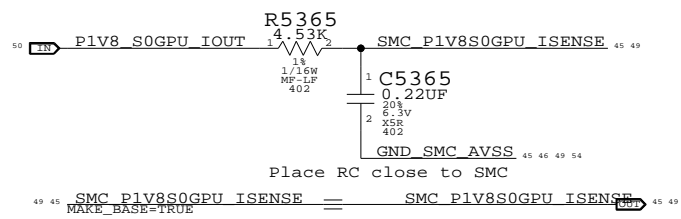
PBUS Voltage Sense & Filter



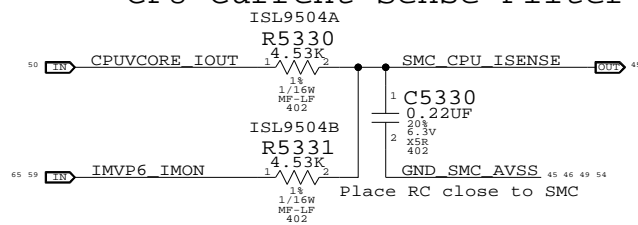
GPU Voltage Sense / Filter



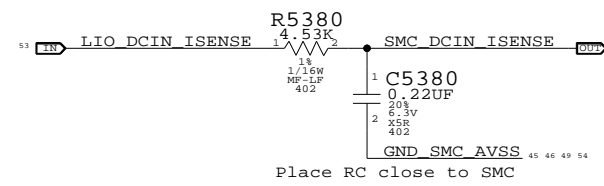
1.8V FB Current Sense Filter



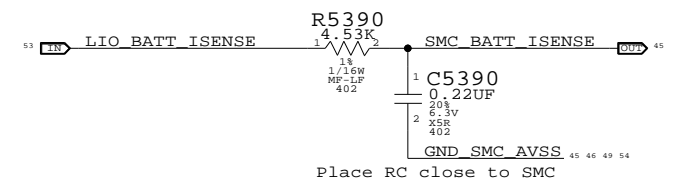
CPU Current Sense Filter



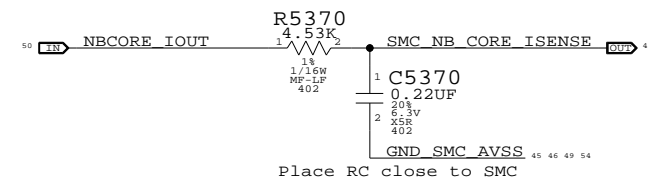
DCIN Current Sense Filter



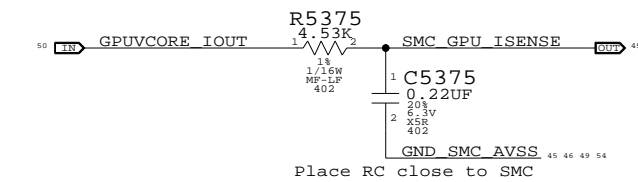
Battery (PBUS) Current Sense Filter



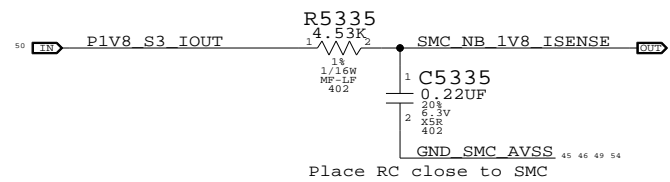
NB Core Current Sense Filter



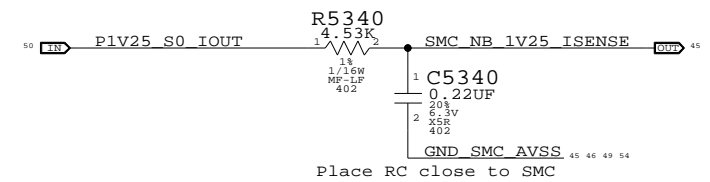
GPU Current Sense Filter



NB 1.8V Current Sense Filter

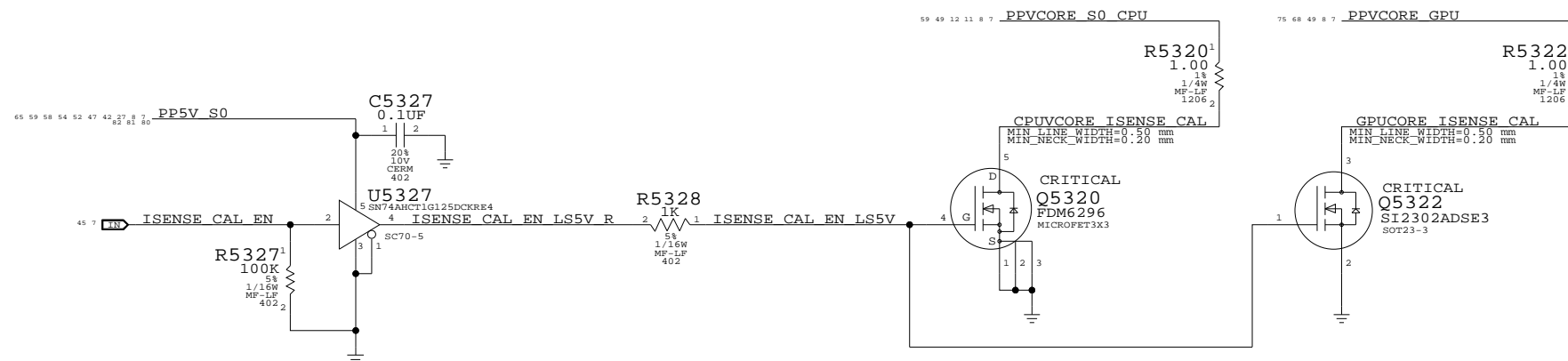


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

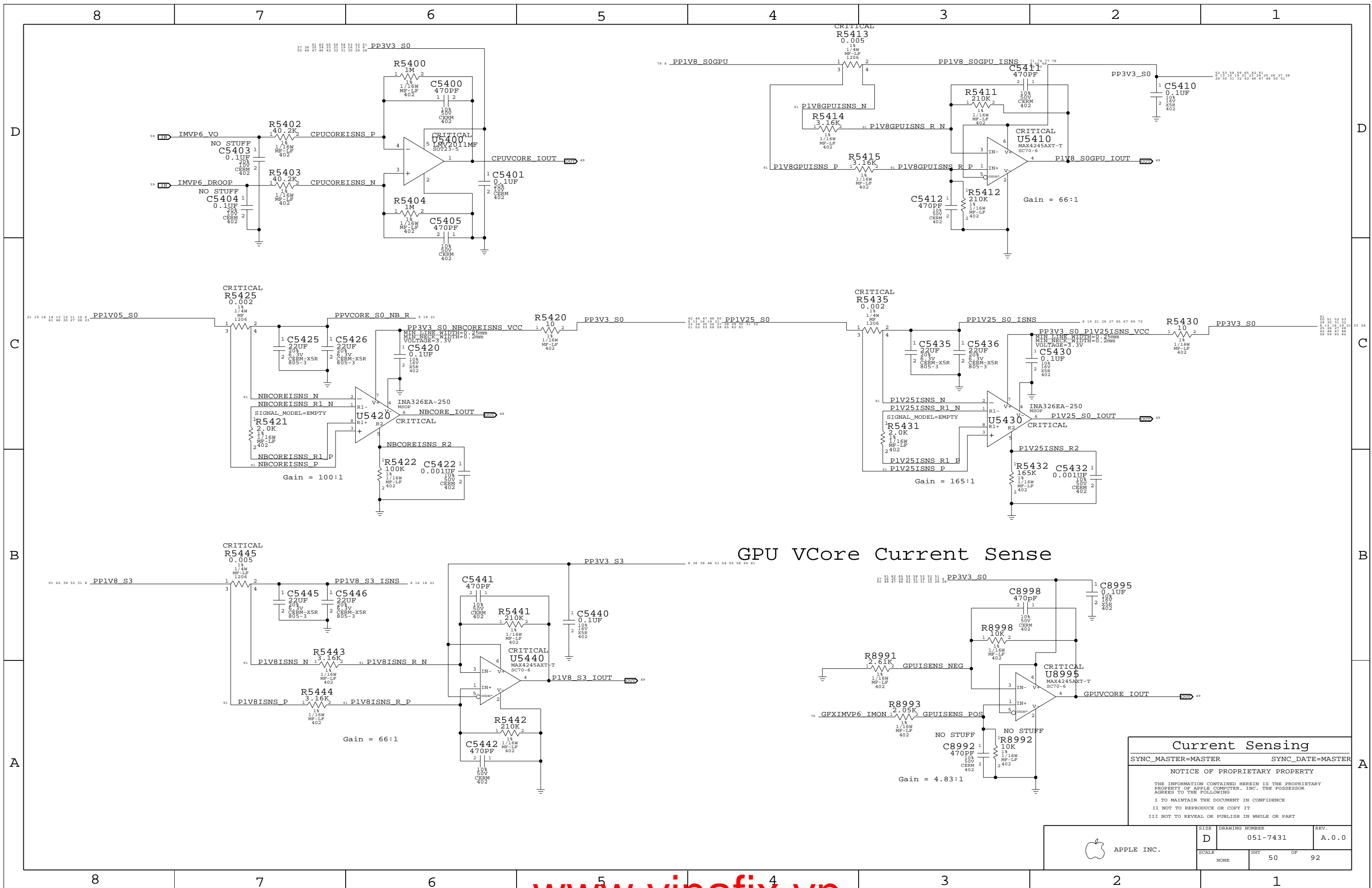
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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D	051-7431	A.0.0
SCALE	SHT	OF
NONE	49	92



GPU VCore Current Sense

Current Sensing
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

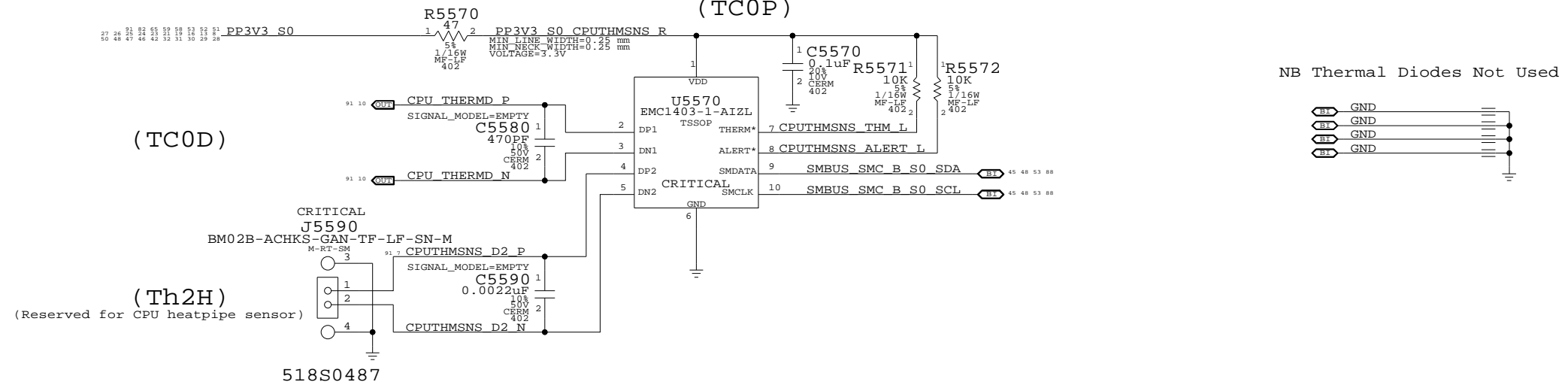
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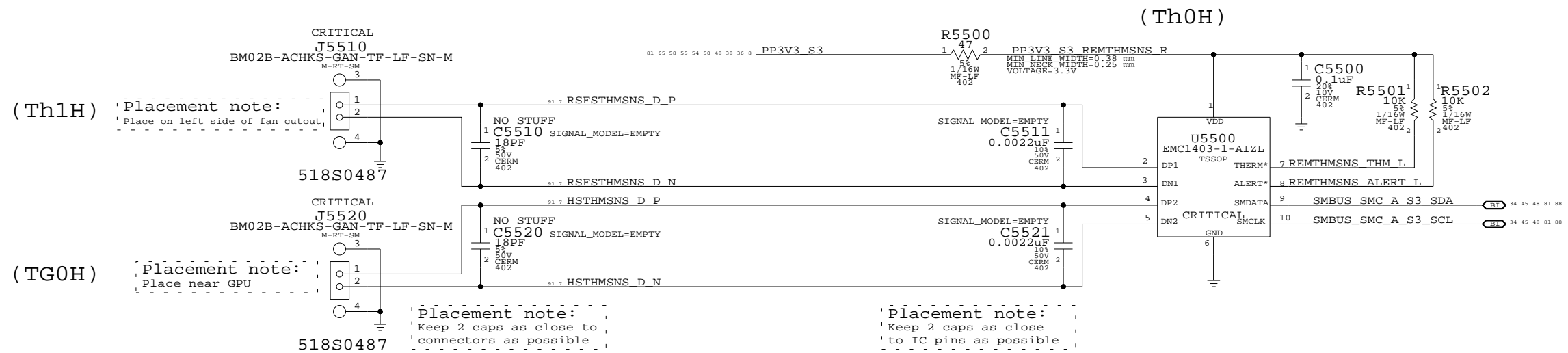
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	92
NONE	50		

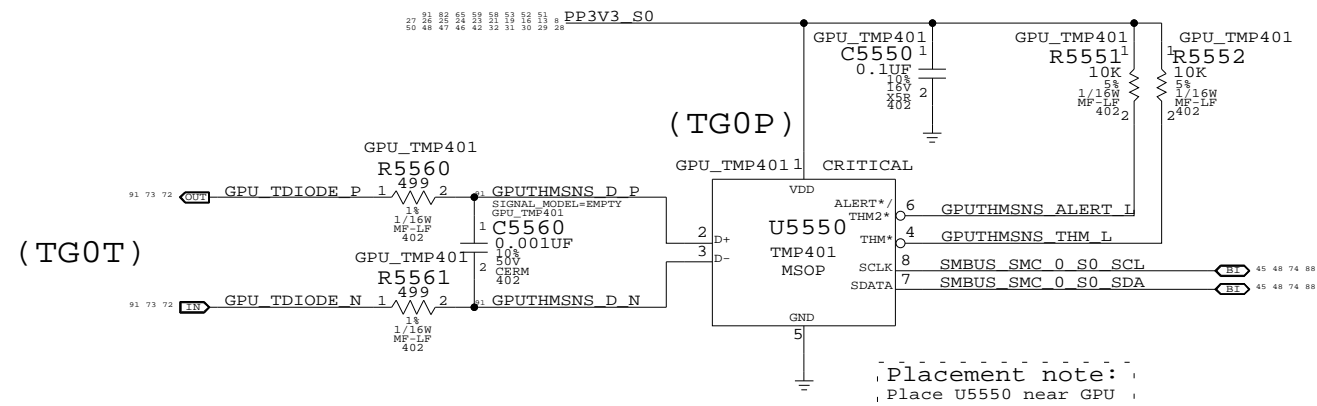
CPU T-Diode Thermal Sensor (TC0P)



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor (Th0H)

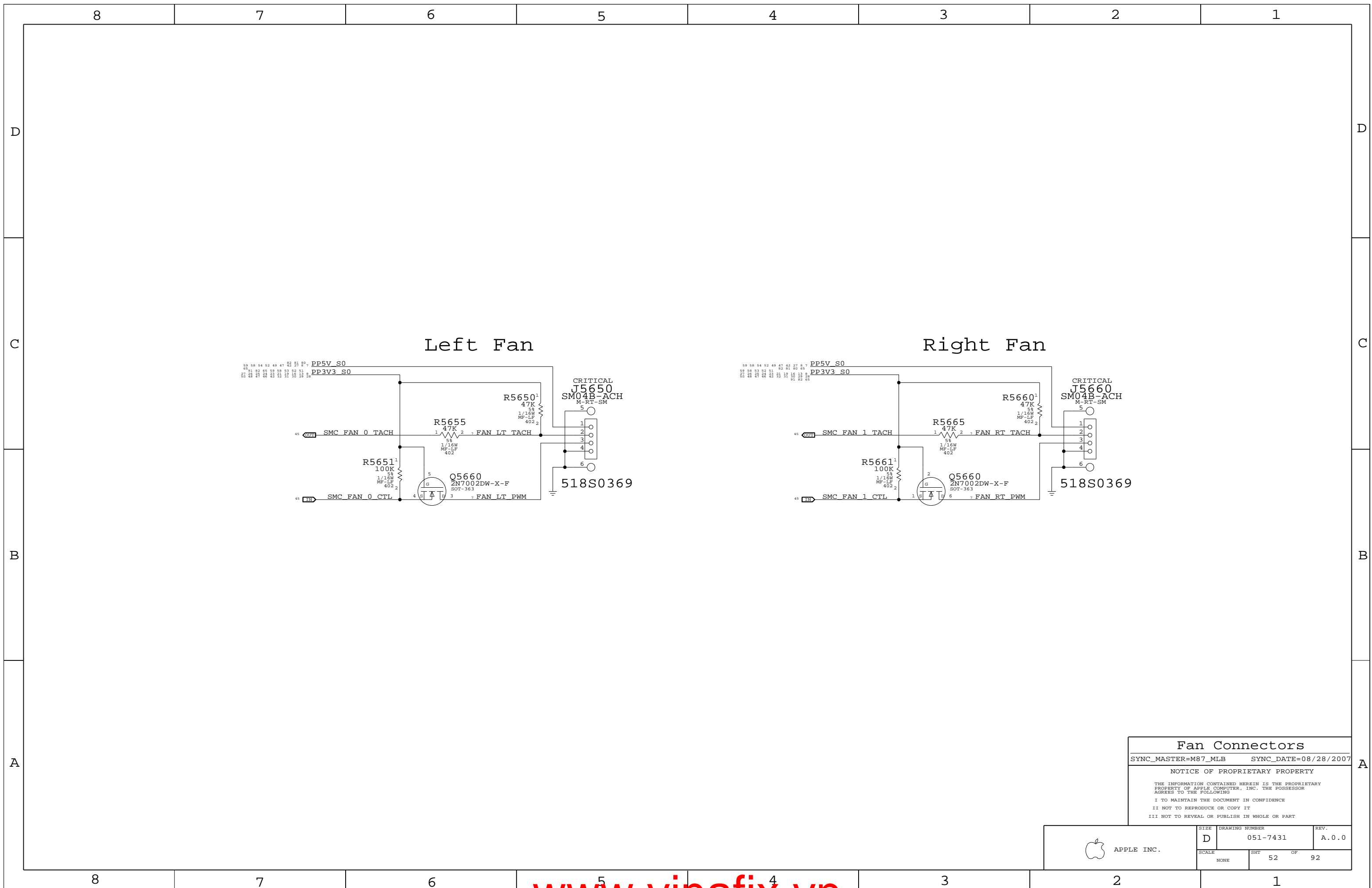


GPU Die Thermal Sensor (TG0P)



Thermal Sensors		
SYNC_MASTER=M87_MLB	SYNC_DATE=08/28/2007	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT		OF
NONE	51		92



Fan Connectors

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

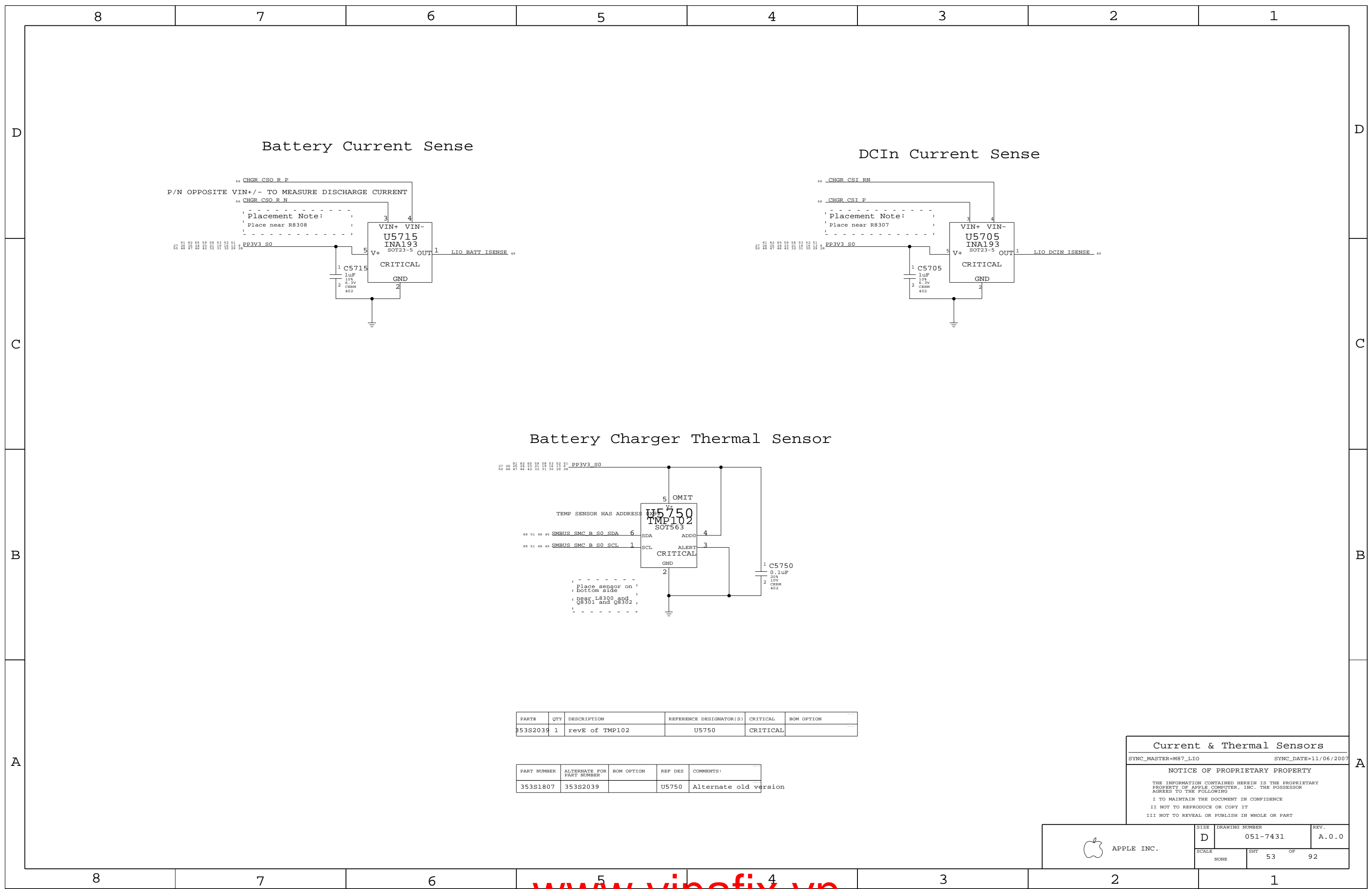
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	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHT 52	OF 92



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2039	1	revE of TMP102	U5750	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1807	353S2039		U5750	Alternate old version

Current & Thermal Sensors

SYNC_MASTER=M87_LIO SYNC_DATE=11/06/2007

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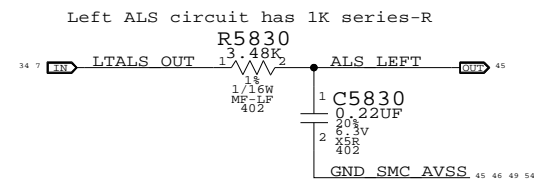
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

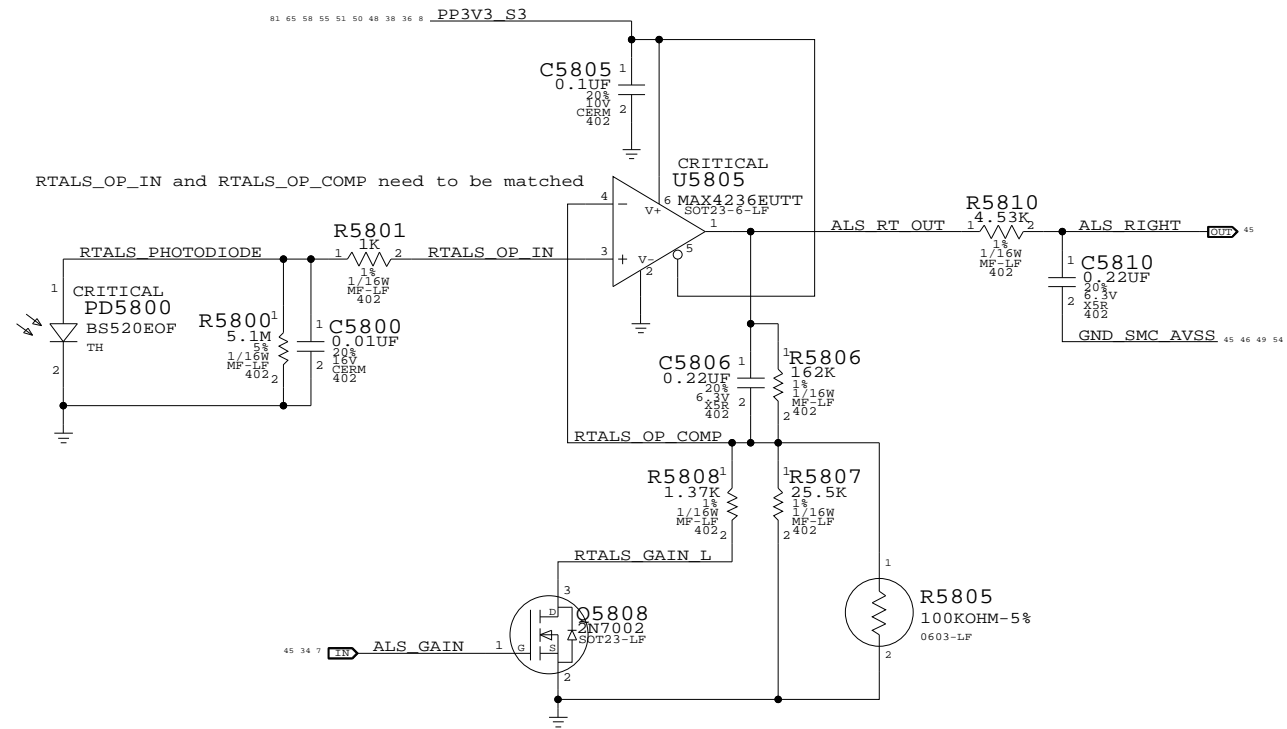
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT 53 OF 92		
NONE			

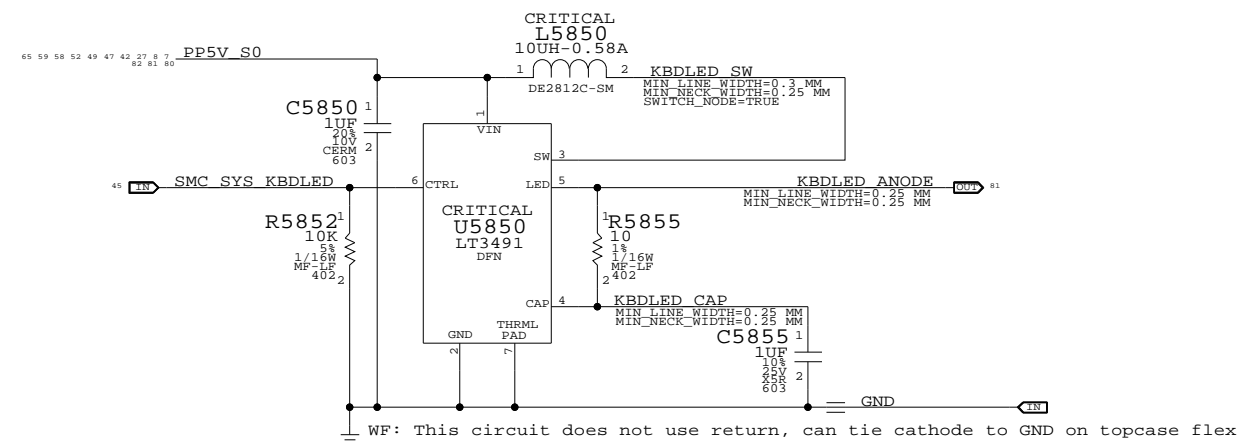
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

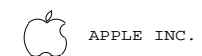
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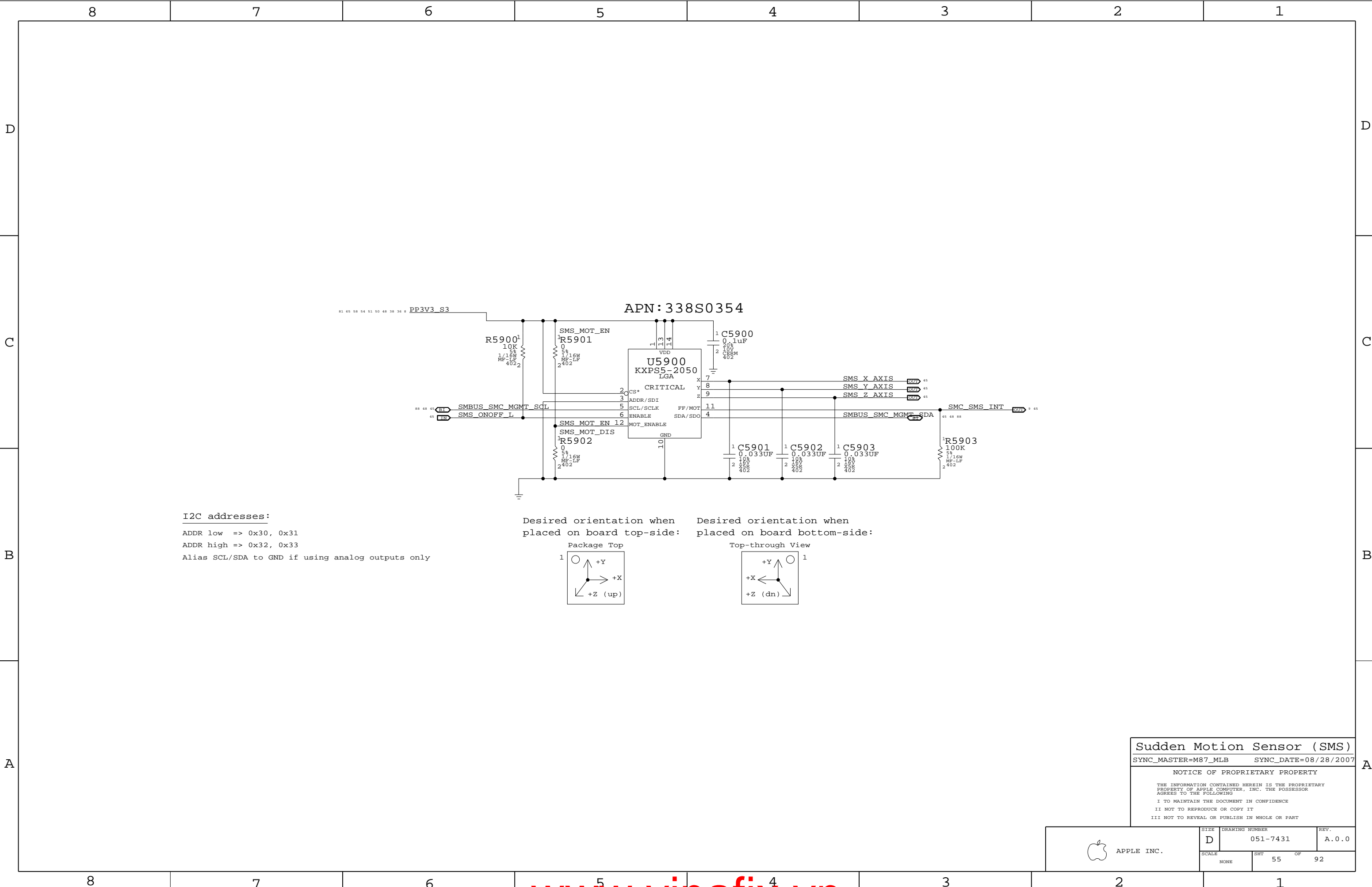
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

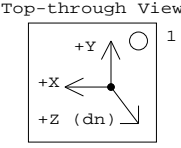
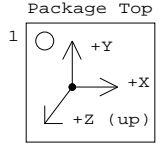
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	54	92



APN: 338S0354

I2C addresses:
 ADDR low => 0x30, 0x31
 ADDR high => 0x32, 0x33
 Alias SCL/SDA to GND if using analog outputs only

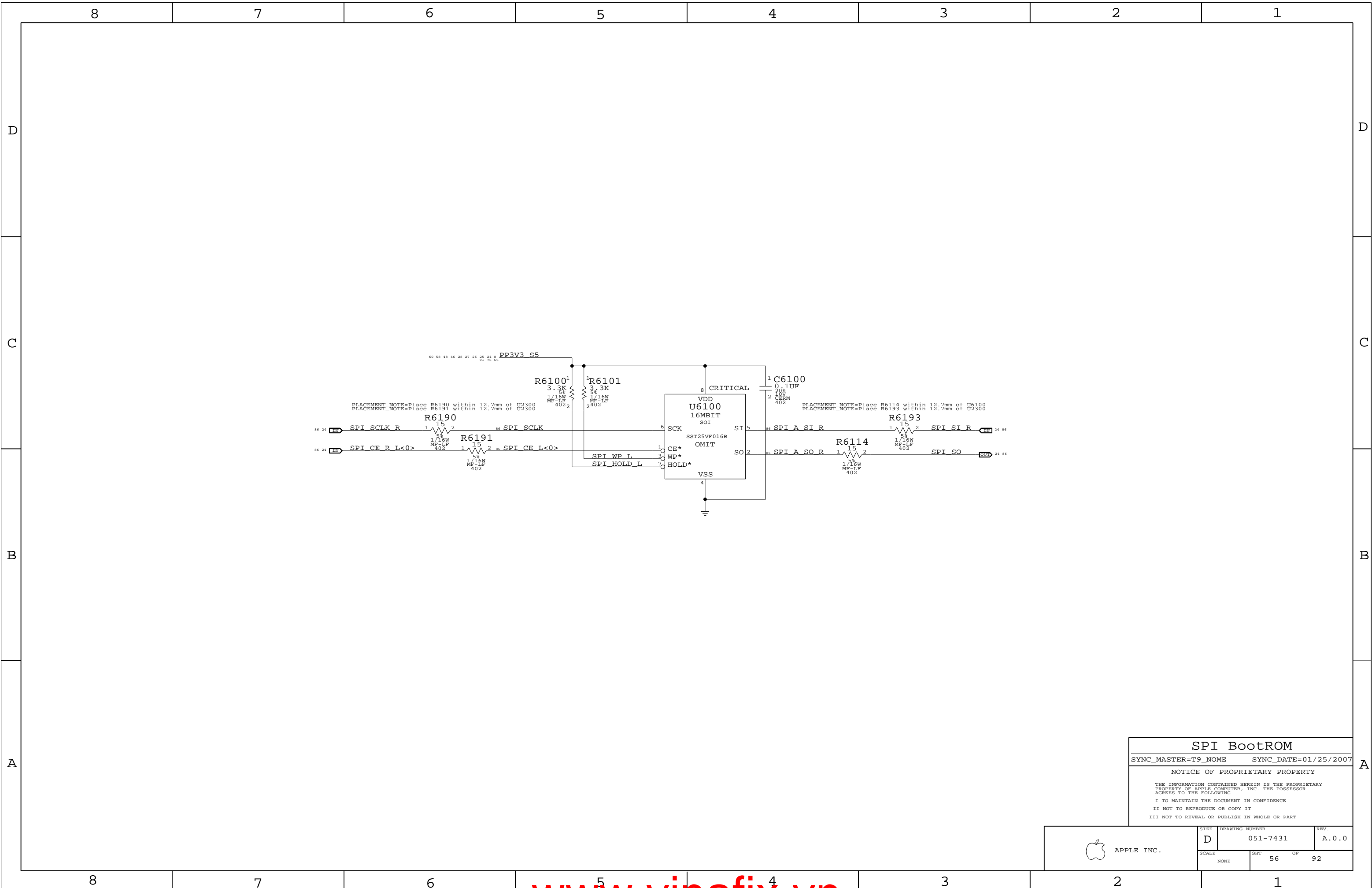
Desired orientation when placed on board top-side: Desired orientation when placed on board bottom-side:



Sudden Motion Sensor (SMS)
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT 55 OF 92		
NONE			



SPI BootROM

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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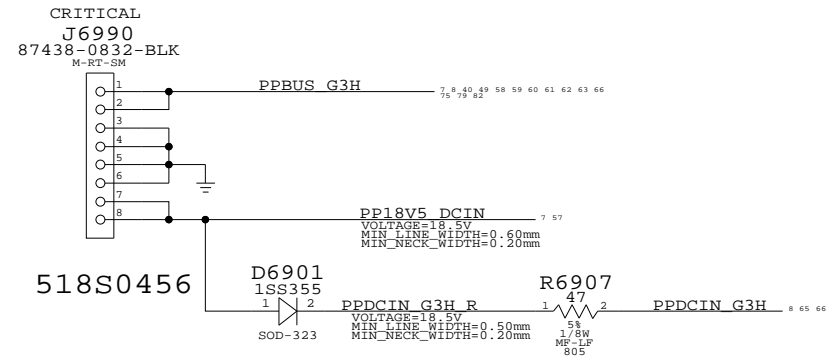
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

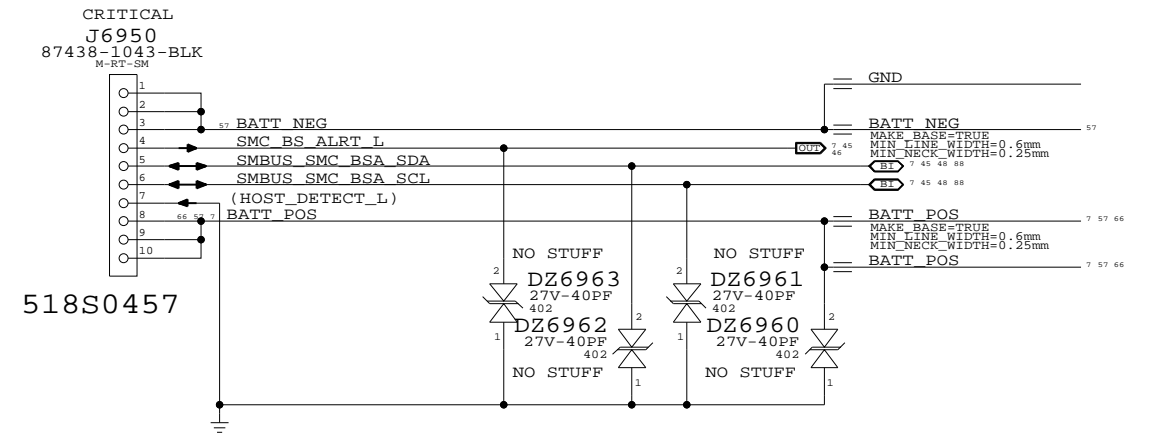
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	<small>SIZE</small> D	<small>DRAWING NUMBER</small> 051-7431	<small>REV.</small> A.0.0
	<small>SCALE</small> NONE	<small>SHT</small> 56	<small>OF</small> 92

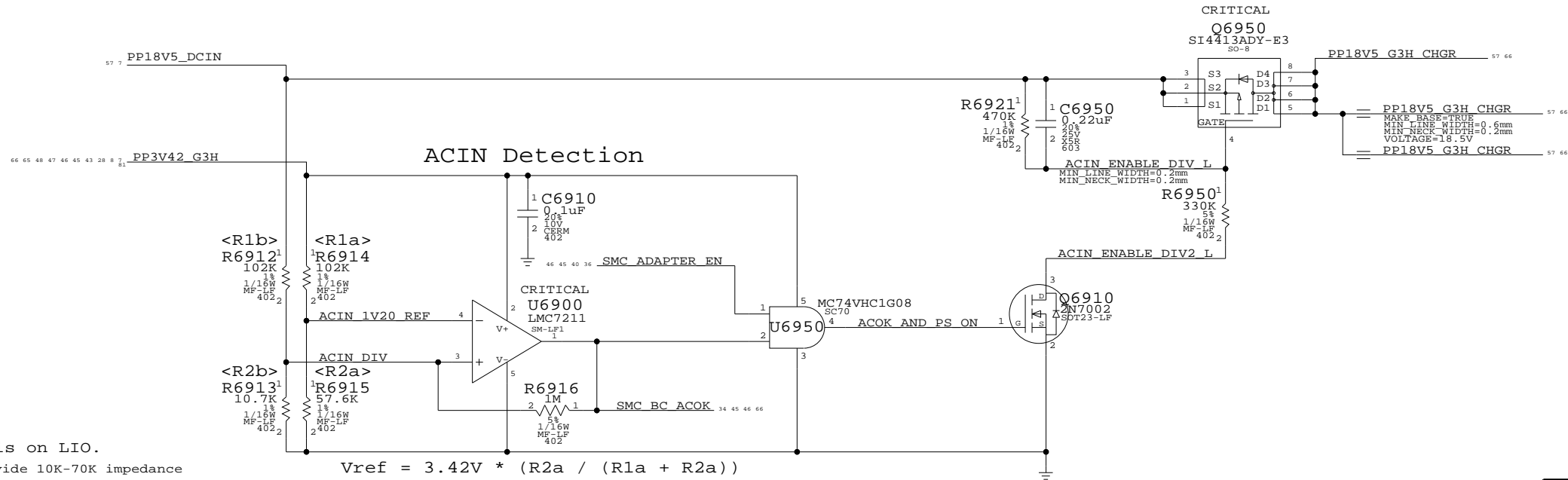
DC-In Connector



Battery Connector



Inrush Limiter



NOTE: R6910 is on LIO.
System must provide 10K-70K impedance to A52 adapter for system load detection.
REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

$$V_{ref} = 3.42V * (R2a / (R1a + R2a))$$

$$V_{th} = (V_{ref} / (R2b / (R1b + R2b)))$$

$$V_{ref} = 1.23V$$

$$V_{th} = 13.0V$$

Assuming 1% variance for R6910-R6915 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

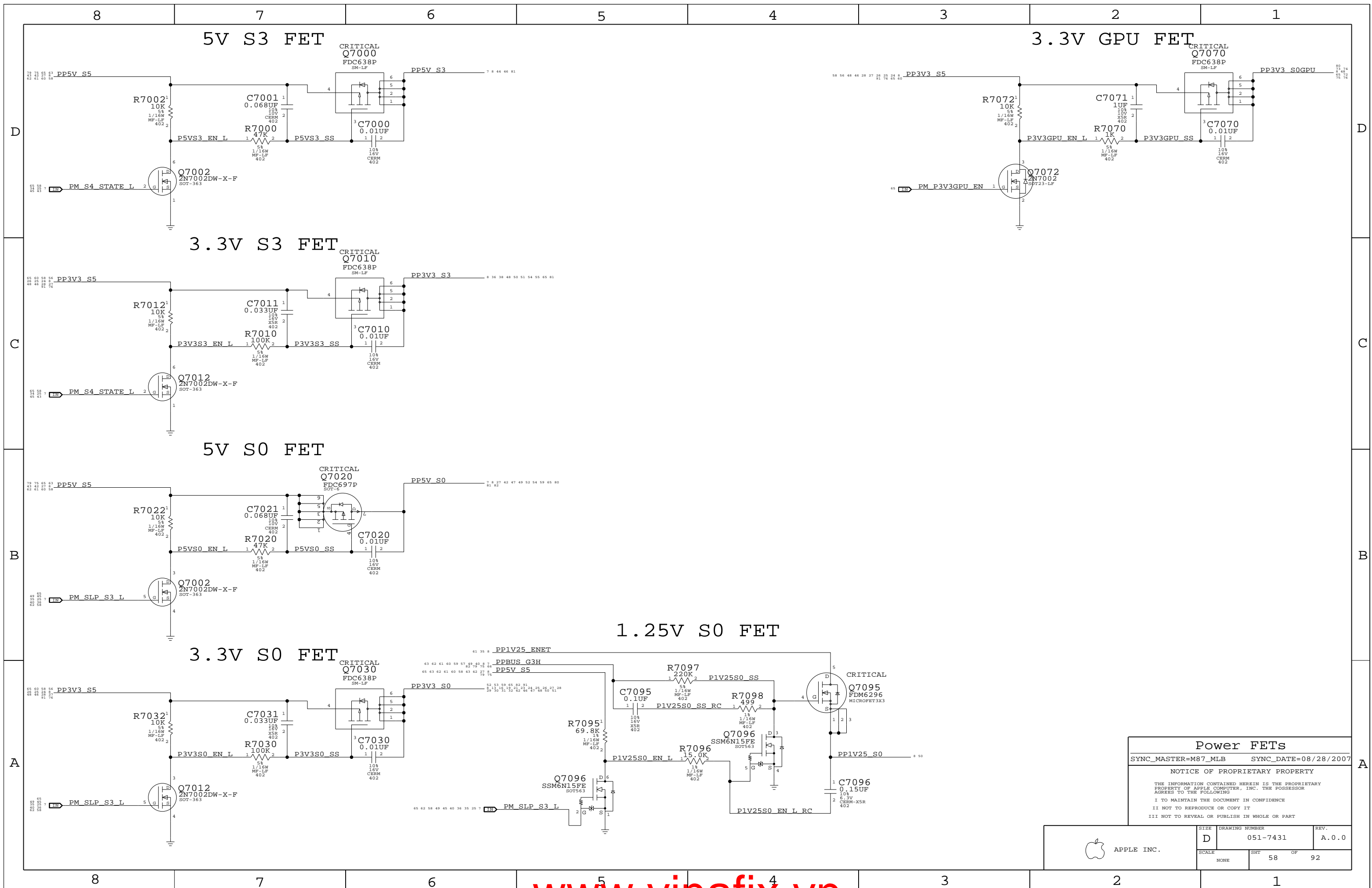
DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	57	92	



Power FETs

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

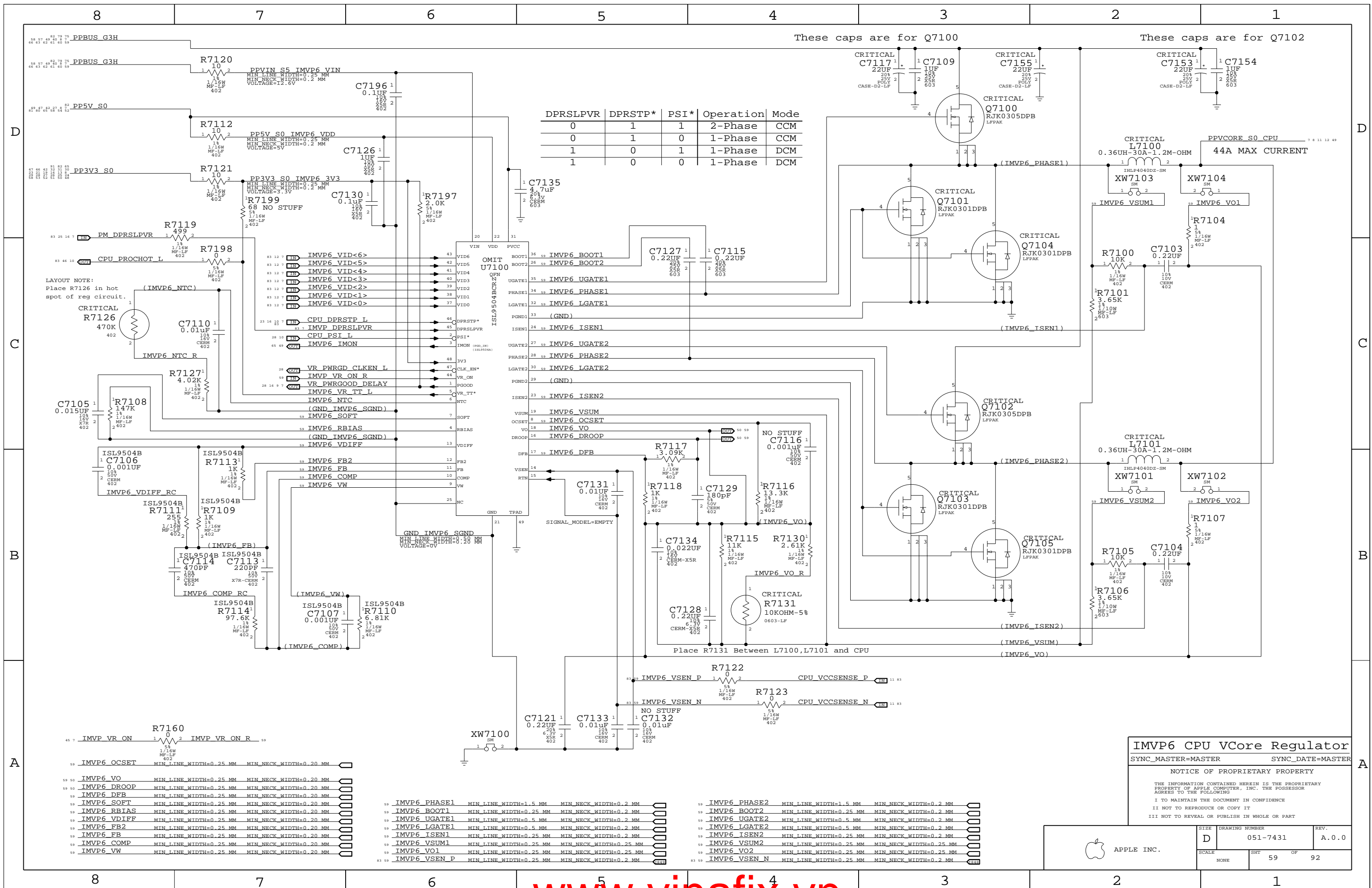
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	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	58	92	



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

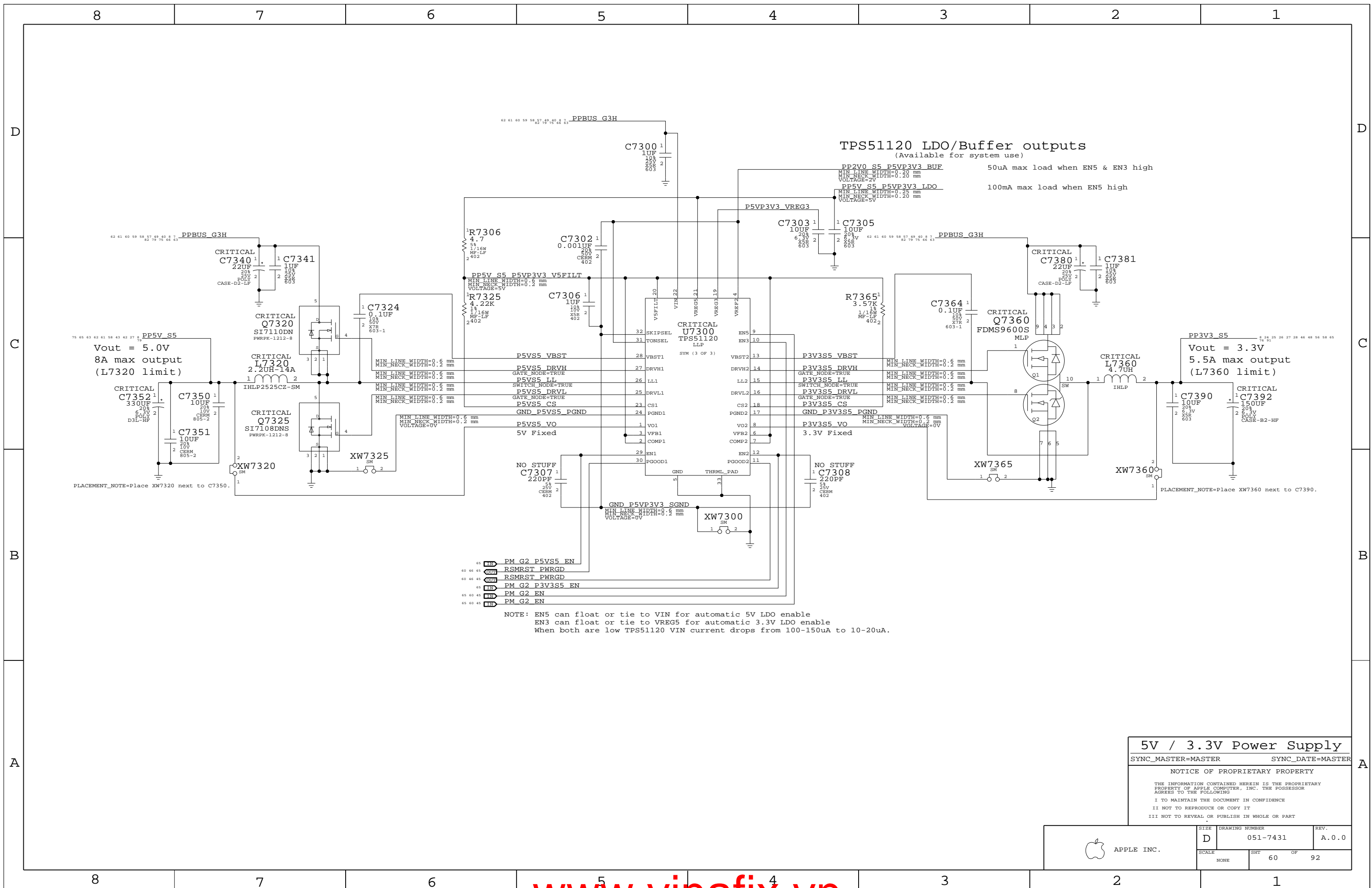
Place R7131 Between L7100, L7101 and CPU

IMVP6 CPU VCore Regulator
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHEET	OF	
NONE	59	92	



TPS51120 LDO/Buffer outputs
(Available for system use)

50uA max load when EN5 & EN3 high

100mA max load when EN5 high

Vout = 5.0V
8A max output
(L7320 limit)

Vout = 3.3V
5.5A max output
(L7360 limit)

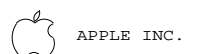
NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

5V / 3.3V Power Supply

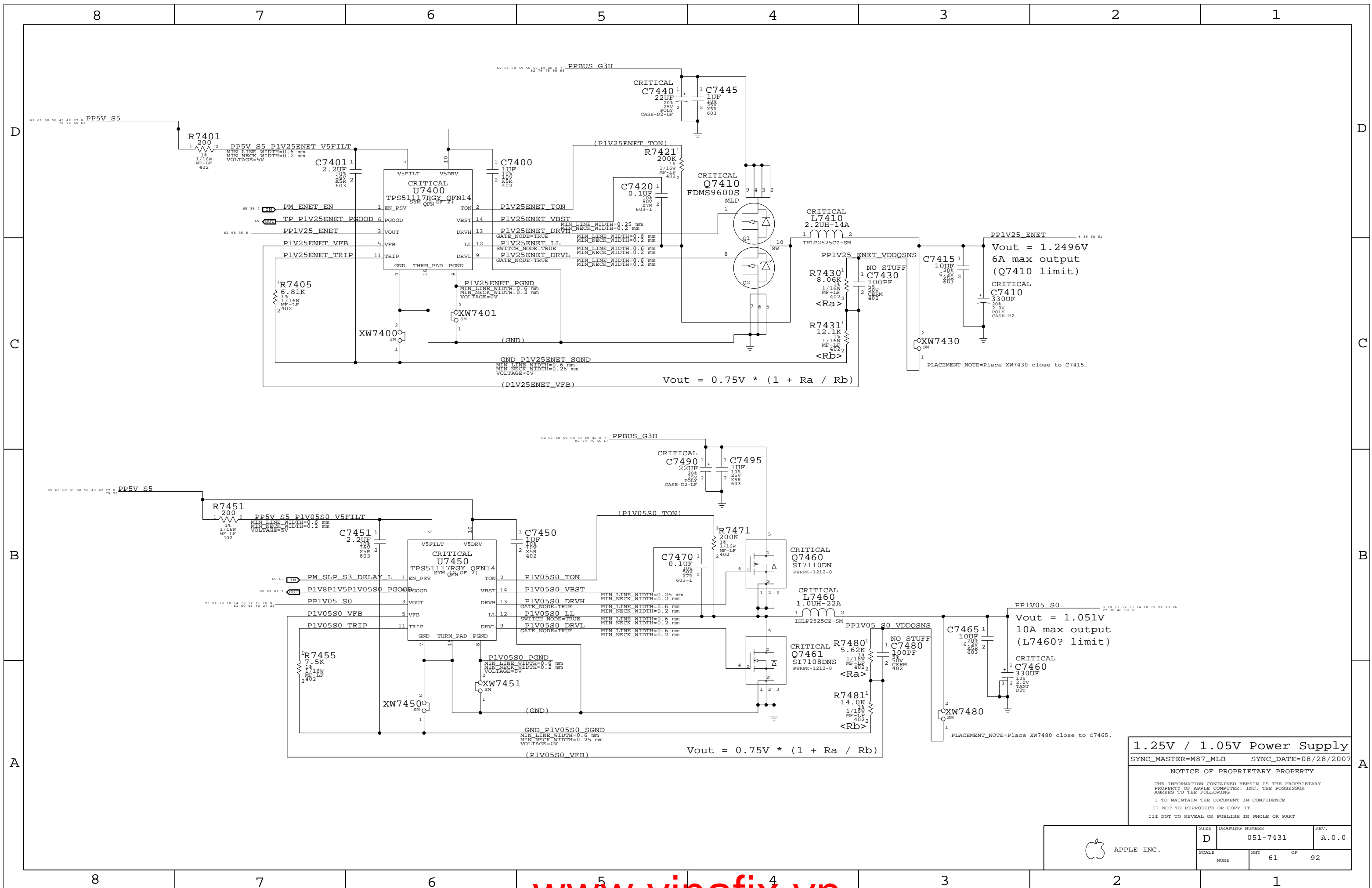
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	60	92



$V_{out} = 0.75V * (1 + R_a / R_b)$

Vout = 1.2496V
6A max output
(Q7410 limit)

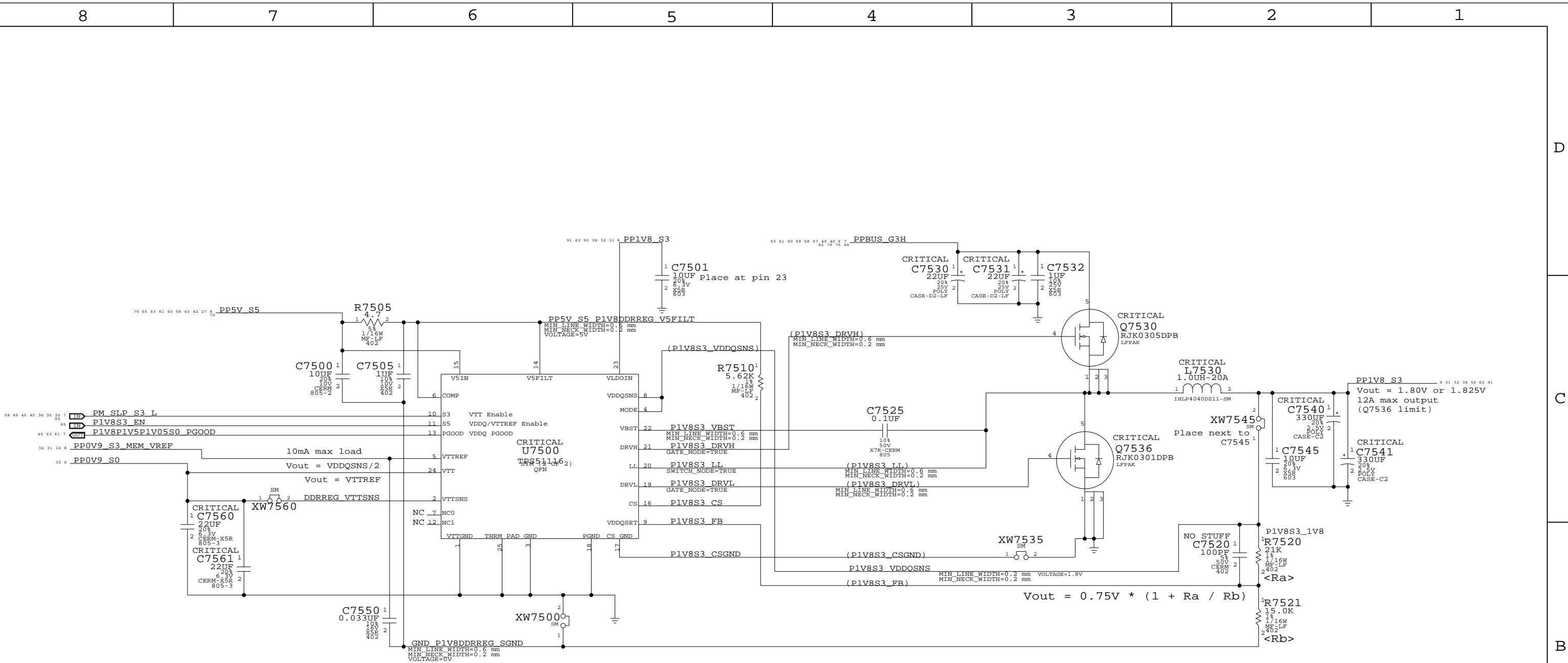
Vout = 1.051V
10A max output
(L7460? limit)

$V_{out} = 0.75V * (1 + R_a / R_b)$

1.25V / 1.05V Power Supply
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	61	92	



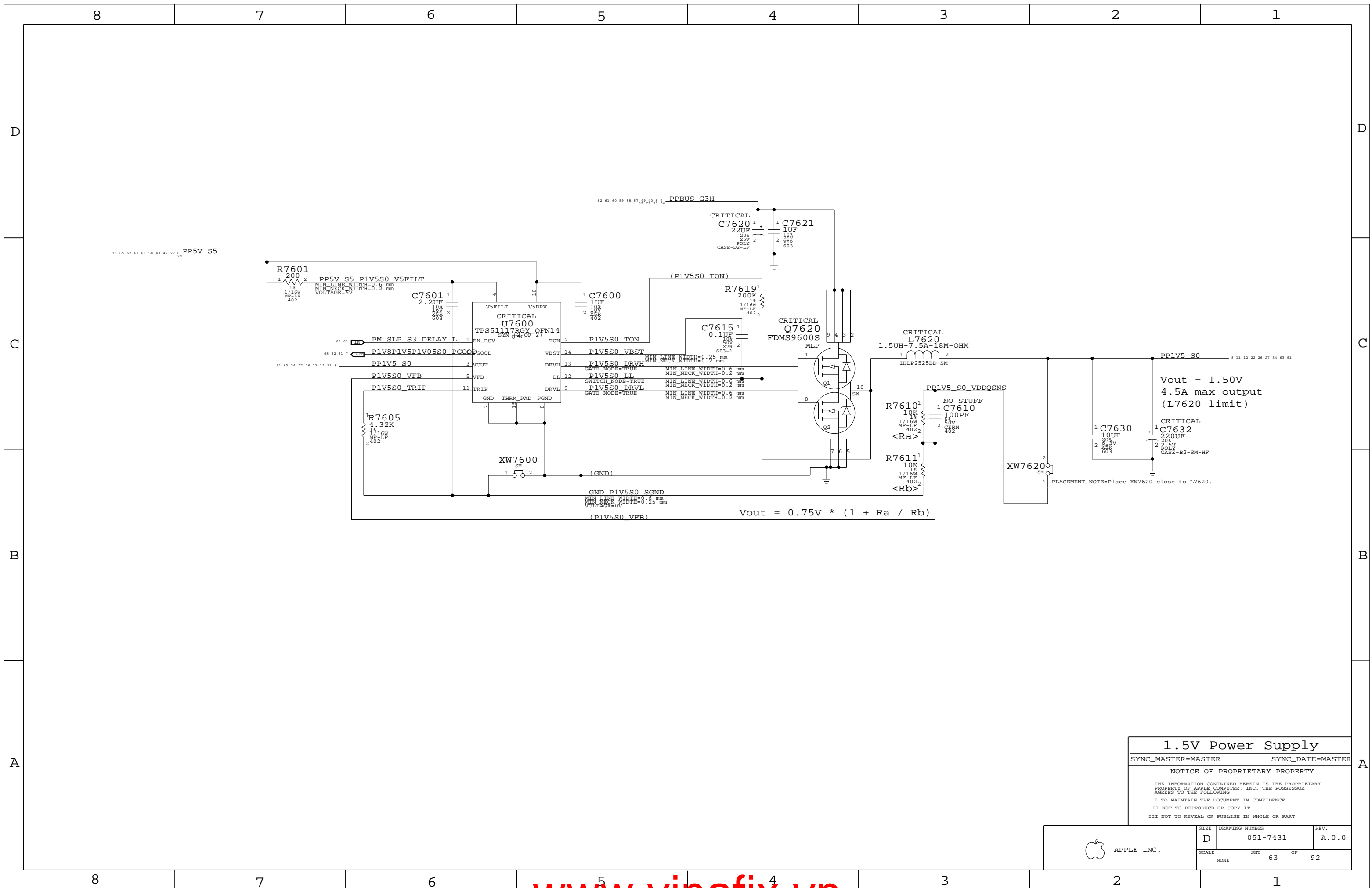
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	62	92	



1.5V Power Supply

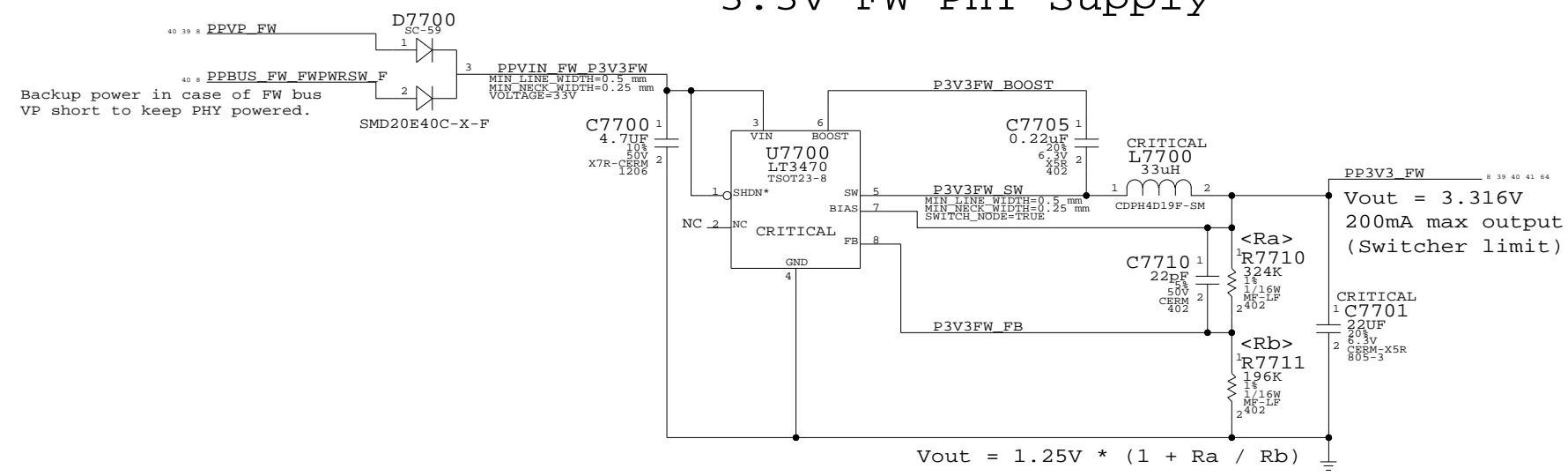
SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

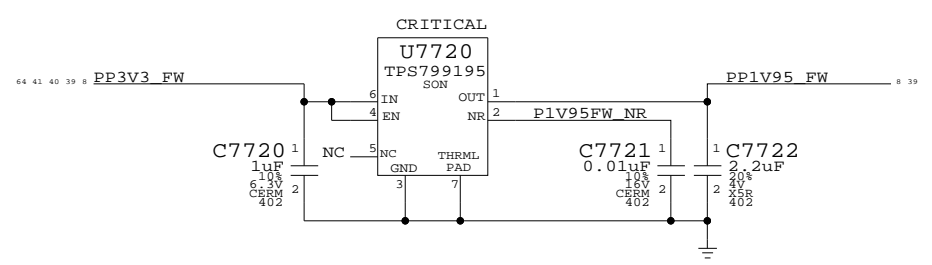
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	63	92	

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

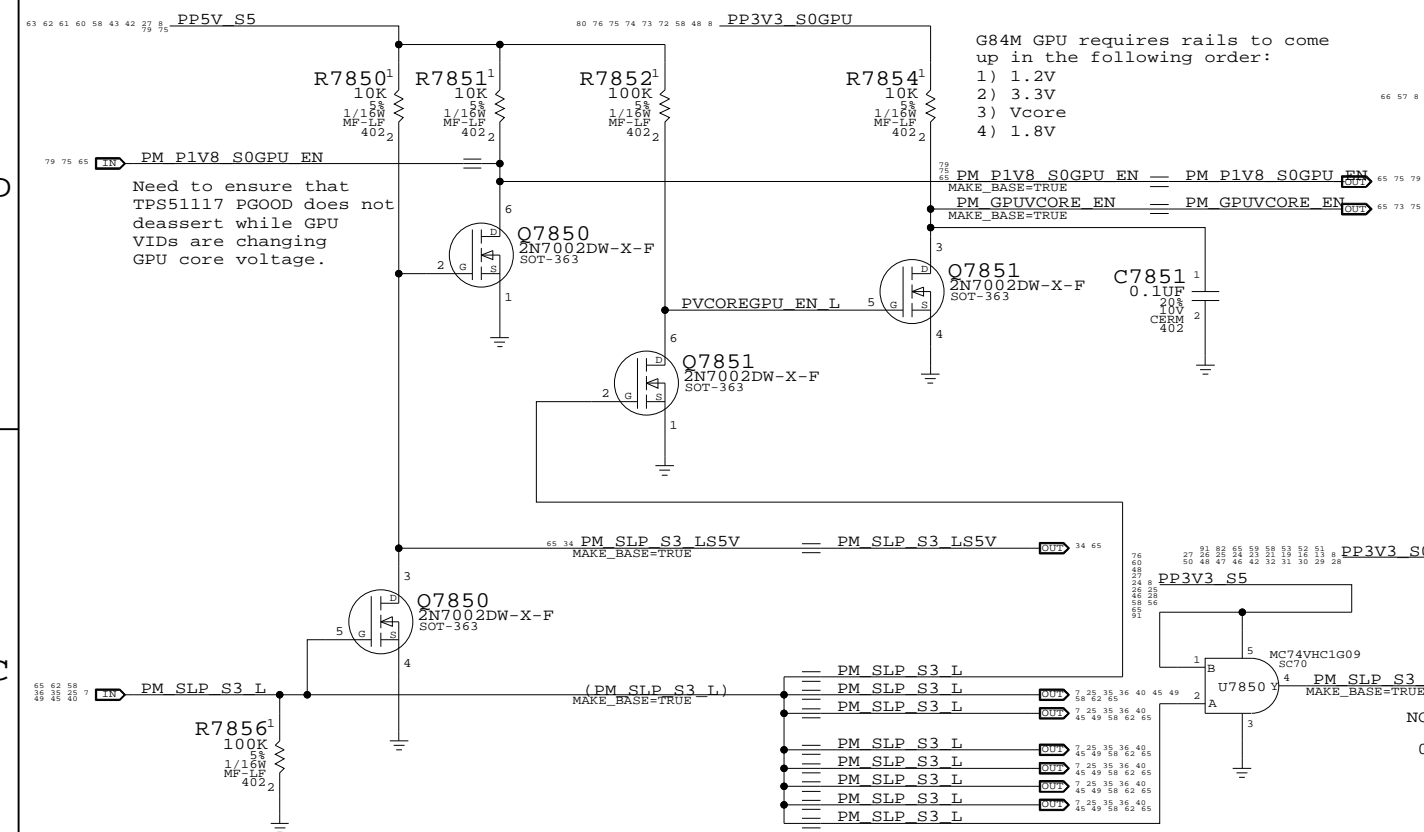
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	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	64	92	

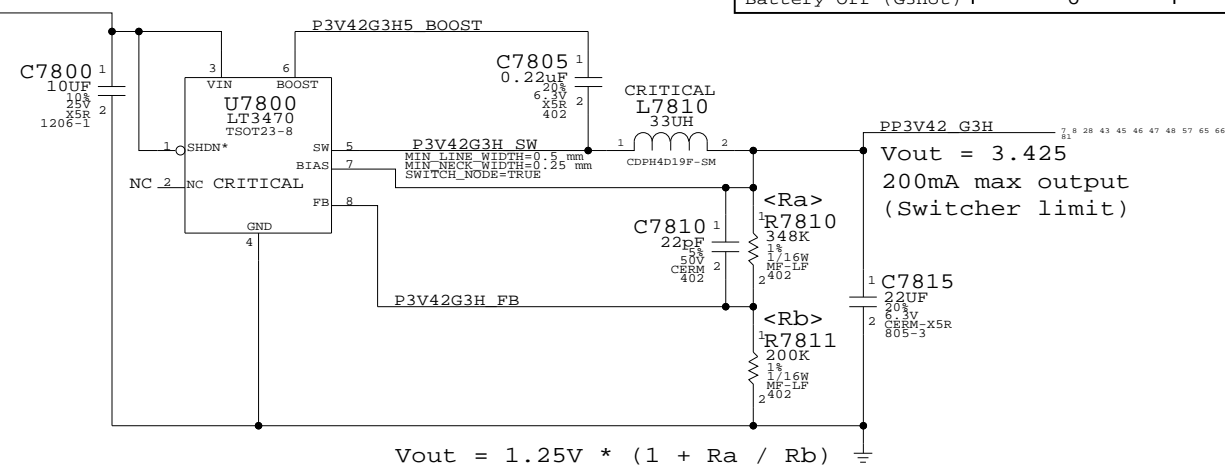
Power Control Signals



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



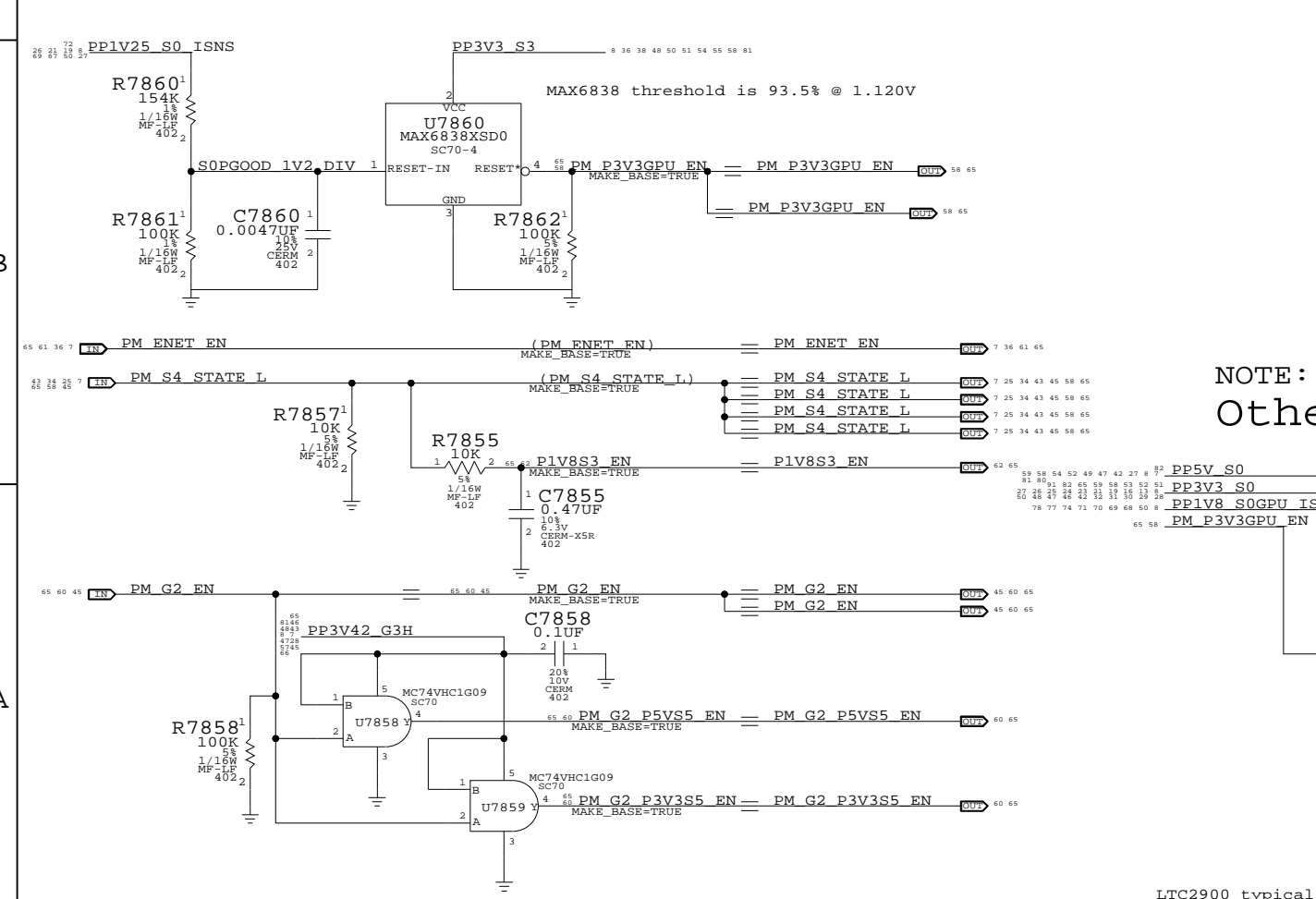
Vout = 3.425
200mA max output
(Switcher limit)

Unused PGOOD Signals

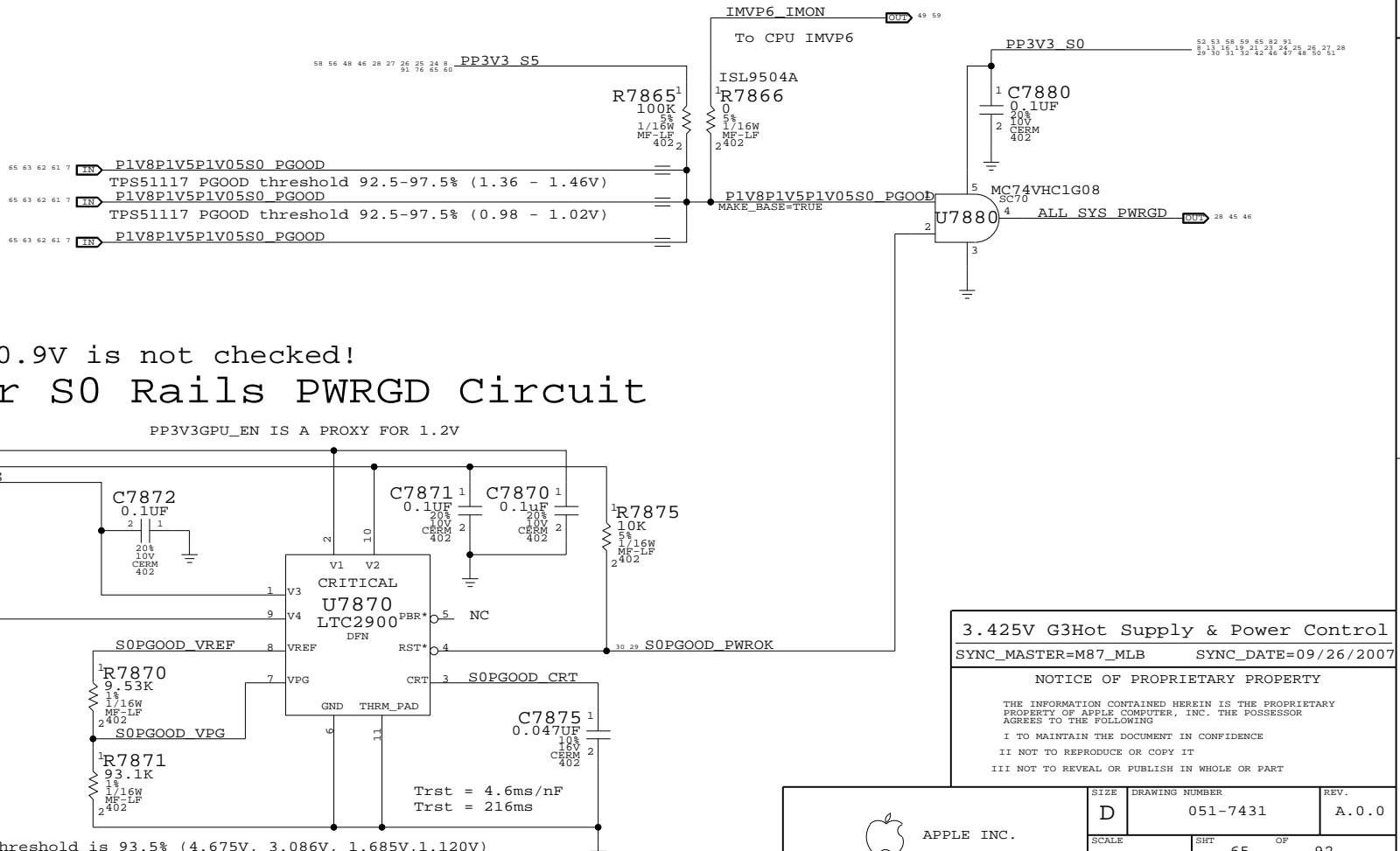
- TP_P1V25ENET_PGOOD = TP_P1V25ENET_PGOOD
- TP_P1V8_S0GPU_PGOOD = TP_P1V8_S0GPU_PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



NOTE: 0.9V is not checked!
Other S0 Rails PWRGD Circuit

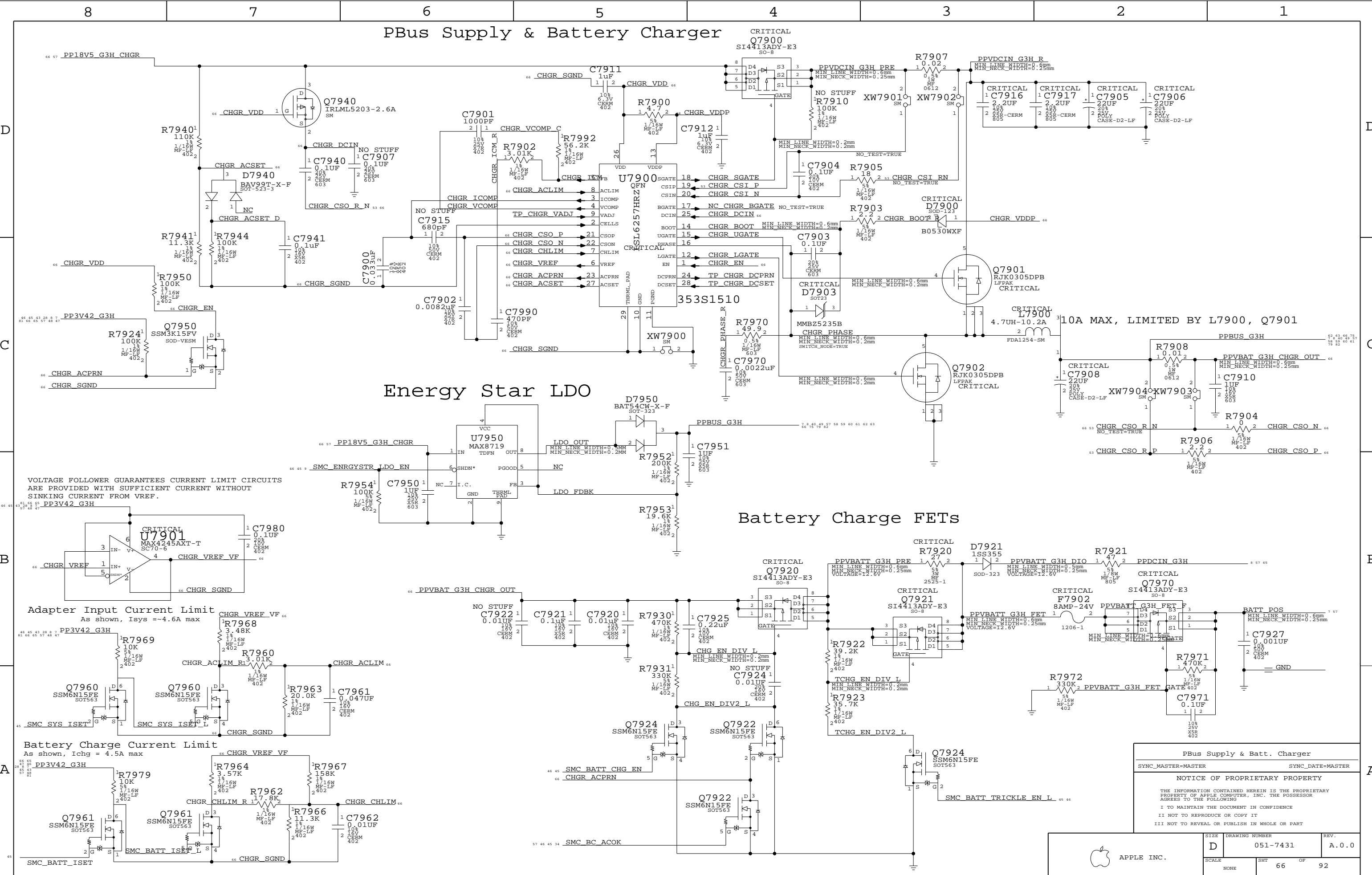


3.425V G3Hot Supply & Power Control
SYNC_MASTER=M87_MLB SYNC_DATE=09/26/2007

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	D	051-7431	A.0.0
SCALE	SHT	OF	92
NONE	65		

PBus Supply & Battery Charger



Energy Star LDO

Battery Charge FETs

Adapter Input Current Limit
As shown, Isys = -4.6A max

Battery Charge Current Limit
As shown, Ichg = 4.5A max

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APPLE INC.		SIZE	DRAWING NUMBER	REV.
		D	051-7431	A.0.0
SCALE	SHEET	OF		
NONE	66	92		

Page Notes

Power aliases required by this page:

- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

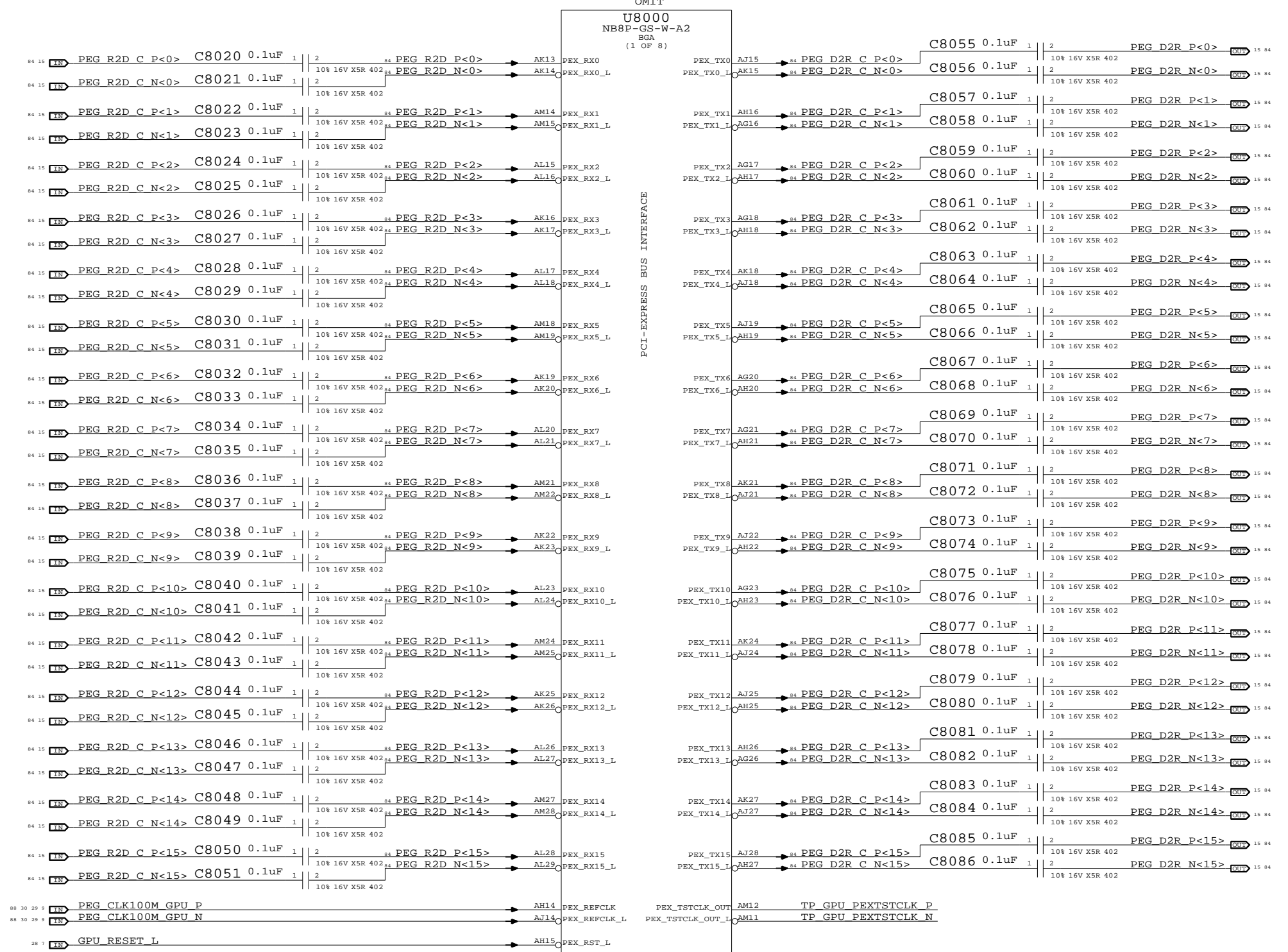
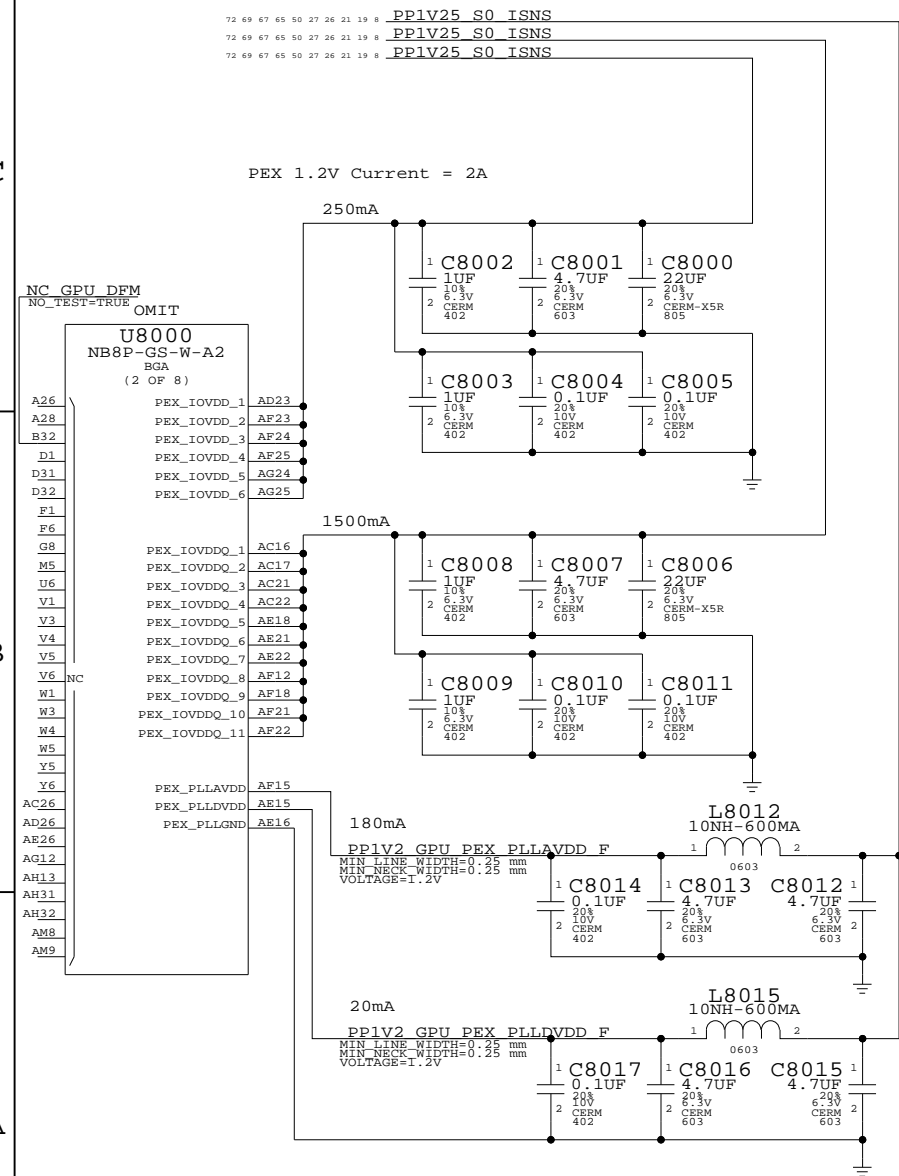
(NONE)

D

C

B

A



D

C

B

A

NV G84M PCI-E

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	NONE	SHT	67 OF 92

Page Notes

Power aliases required by this page:

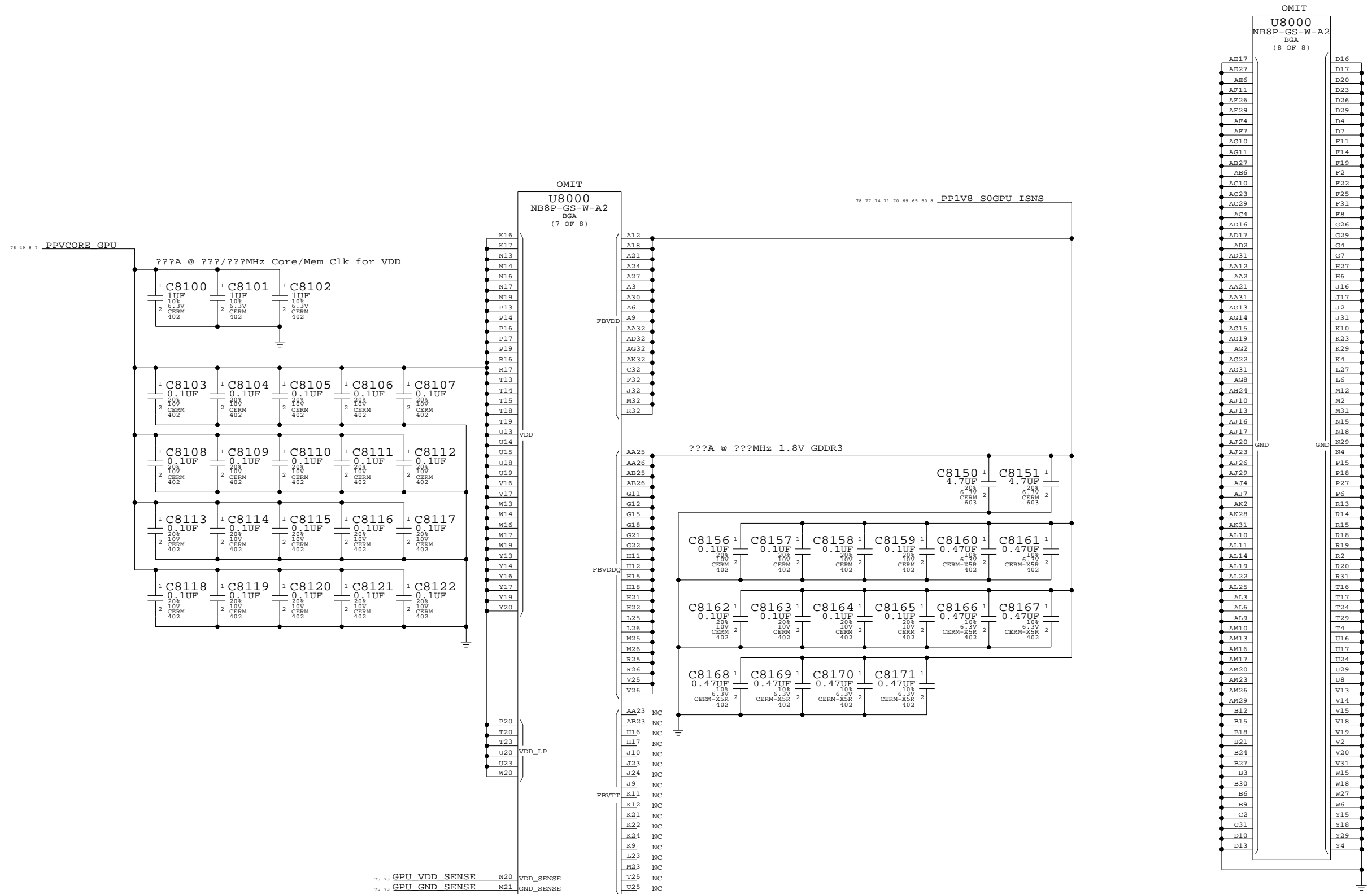
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



NV G84M Core/FB Power

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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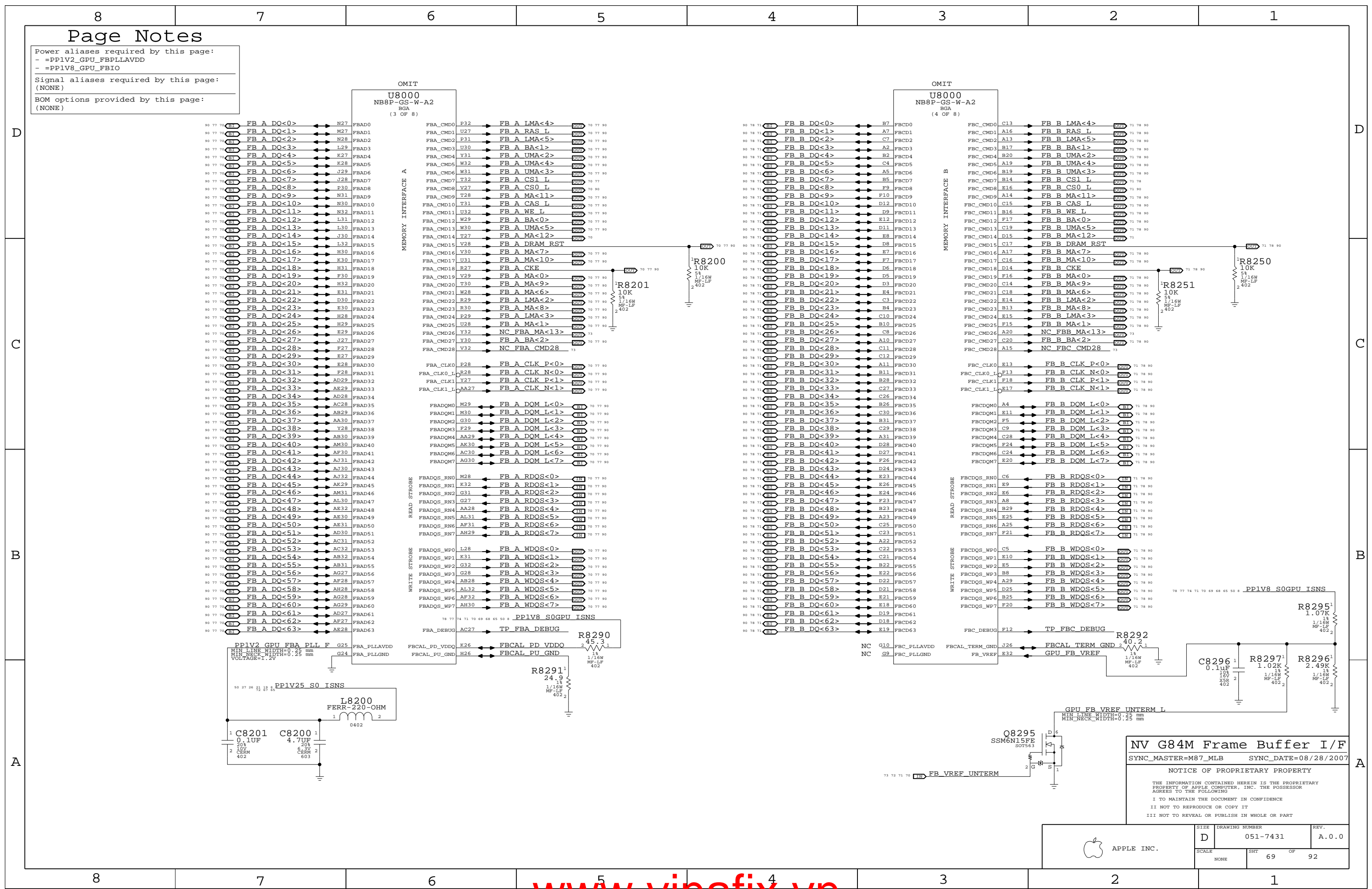
	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	68	92	

Page Notes

Power aliases required by this page:
 - =PPIV2_GPU_FBLLAVDD
 - =PPIV8_GPU_FBIO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

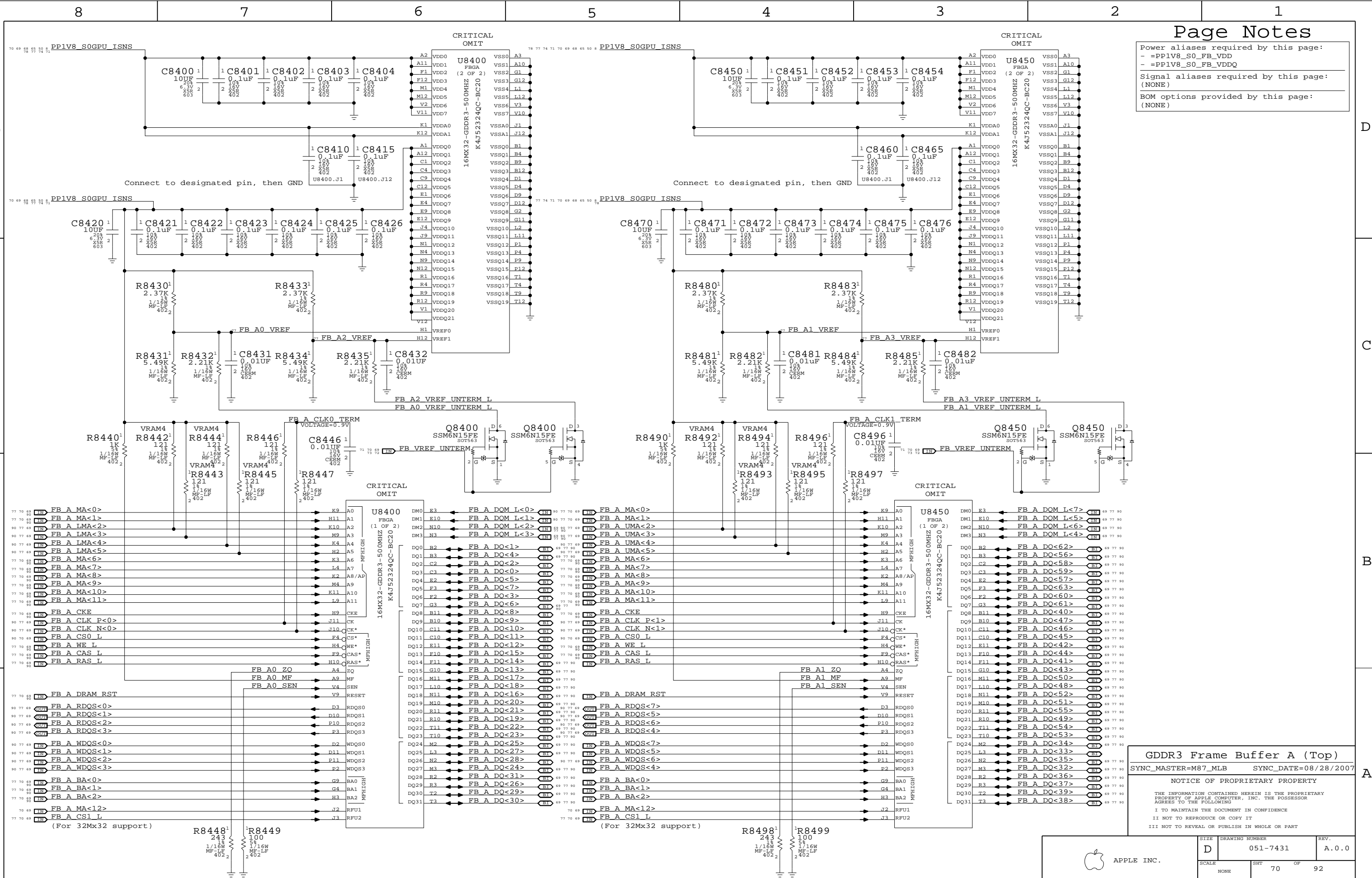


NV G84M Frame Buffer I/F
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	69	92	

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

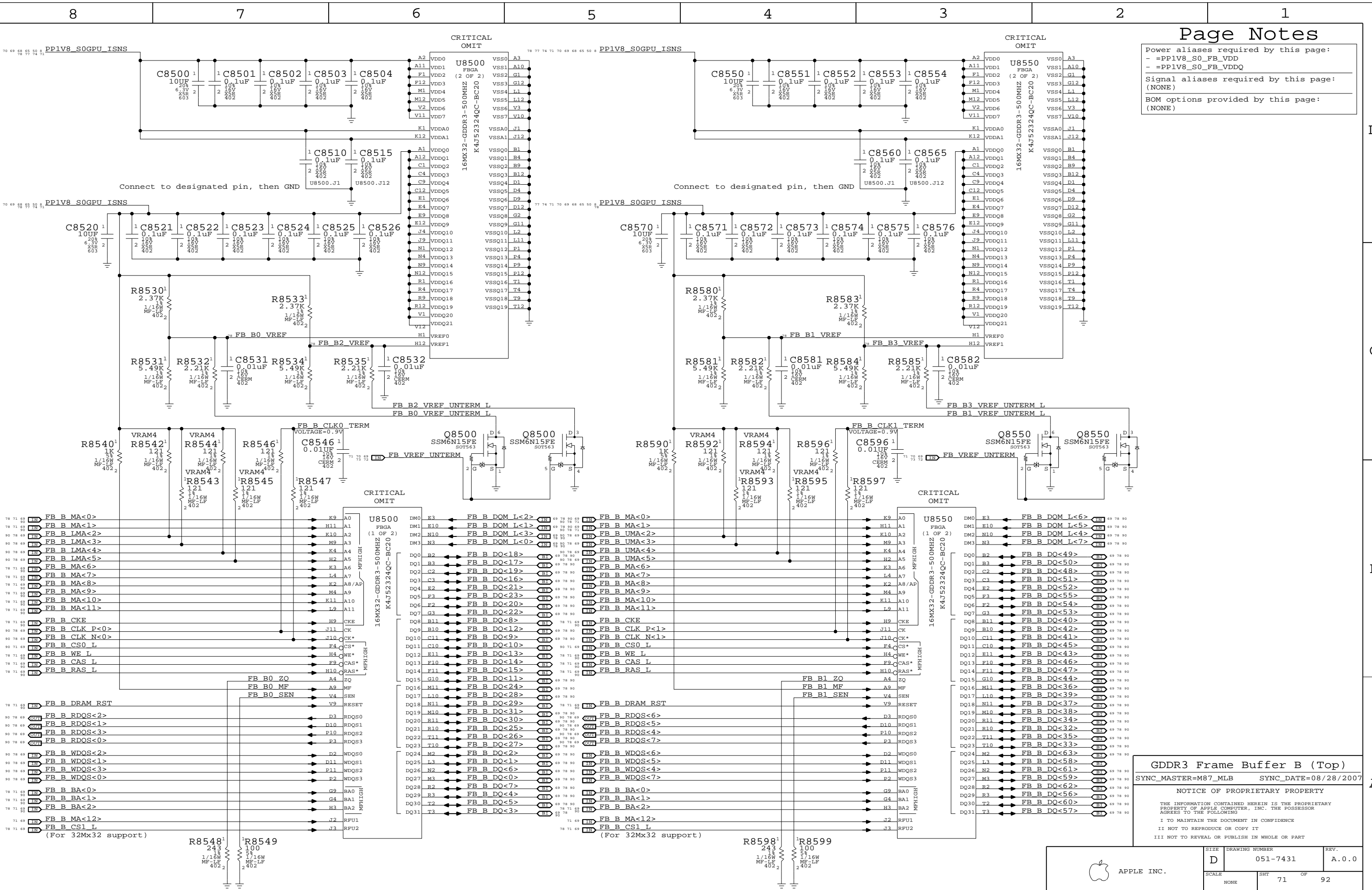
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	70	OF 92
NONE			

Power aliases required by this page:
 - =PP1V8_S0_FB_VDD
 - =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B (Top)
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	71	92

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_VDD33
 - =PP3V3_GPU_MIO
 - =PP1V2_GPU_PLLVDD
 - =PP1V2_GPU_H_PLLVDD
 - =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

D

D

C

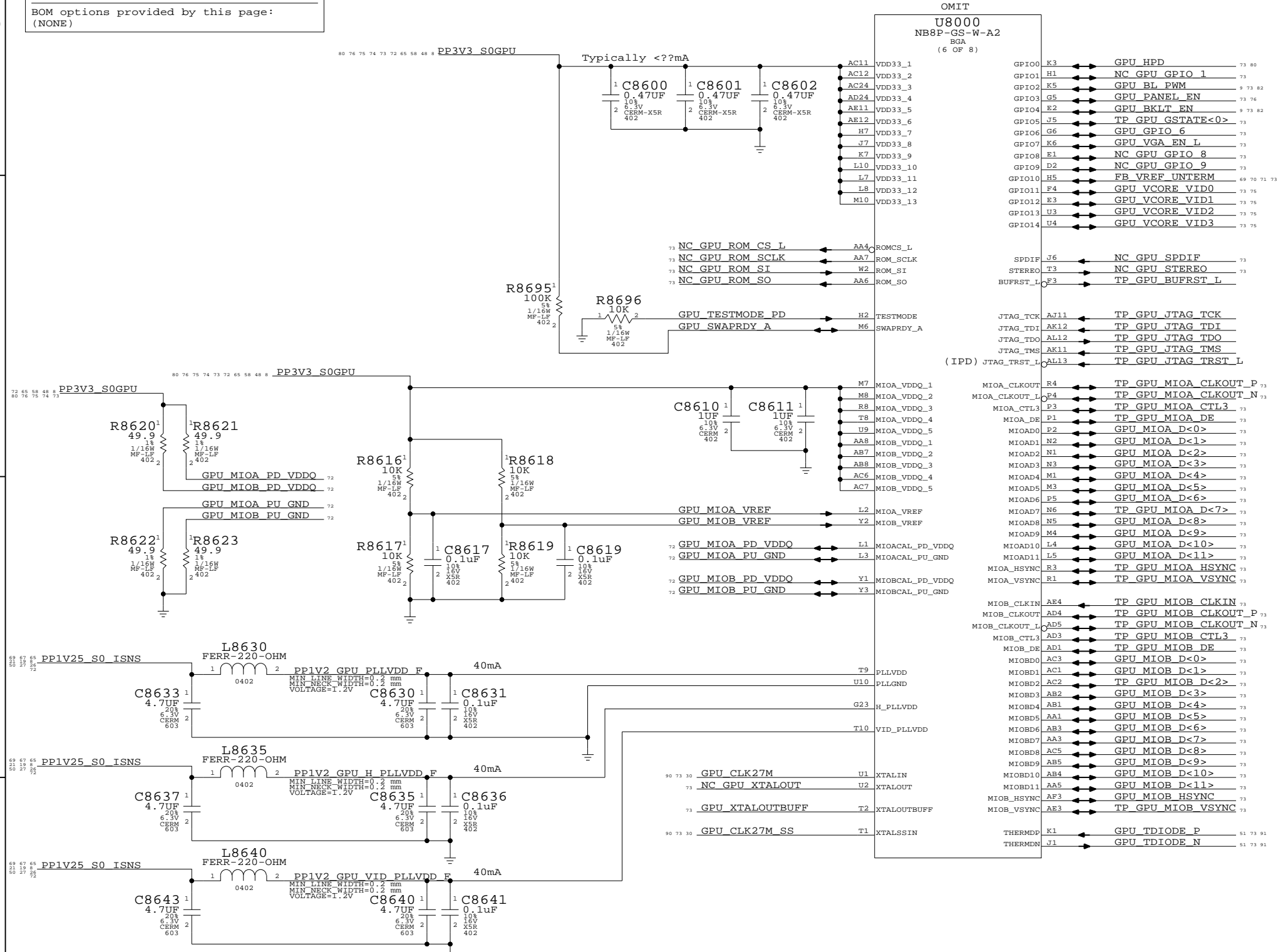
C

B

B

A

A



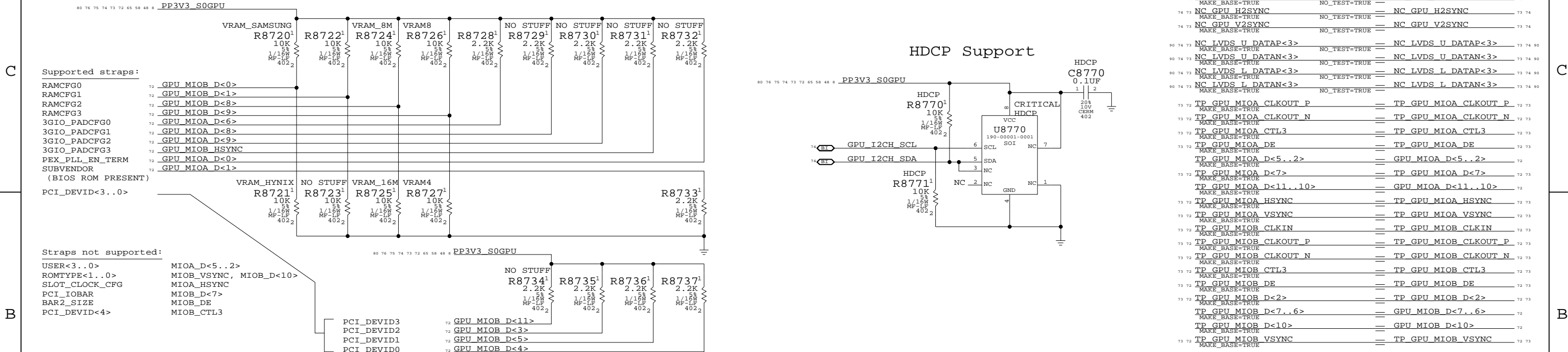
NV G84M GPIO/MIO/Misc
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	72	92	

GPIOs		Renamed signals		Unused signals	
Native Func	HPD0	GPU HPD	GPU CLK27M	GPU CLK27M	NC GPU XTALOUT
GPU HPD	HPD1	GPU HPD	GPU CLK27M SS	GPU CLK27M SS	NC GPU SPDIF
NC GPU GPIO 1	LCD0_BL_PWM	GPU BL_PWM	GPU TDIODE P	GPU TDIODE P	NC GPU STEREO
GPU BL_PWM	LCD0_VDD	GPU PANEL EN	GPU TDIODE N	GPU TDIODE N	NC GPU STEREO
GPU PANEL EN	LCD0_BL_EN	GPU BKLT EN	GPU DVI DDC CLK	GPU DVI DDC CLK	
GPU BKLT EN	VID0	TP GPU GSTATE<0>	GPU DVI DDC DATA	GPU DVI DDC DATA	
TP GPU GSTATE<0>	VID1	TP GPU GSTATE<1>	GPU PANEL DDC CLK	GPU PANEL DDC CLK	
GPU GPIO 6	MEM_VID	GPU VGA EN L	GPU PANEL DDC DATA	GPU PANEL DDC DATA	
GPU VGA EN L	THERM	NC GPU GPIO 8	GPU VDD SENSE	GPU VDD SENSE	
NC GPU GPIO 8	FAN_PWM	NC GPU GPIO 9	GPU GND SENSE	GPU GND SENSE	
NC GPU GPIO 9	MEM_VREF	FB VREF UNTERM			
FB VREF UNTERM	SLI_SYNC	GPU VCORE VID0			
GPU VCORE VID0	AC_DET	GPU VCORE VID1			
GPU VCORE VID1	PWR_CTL0	GPU VCORE VID2			
GPU VCORE VID2	PWR_CTL1	GPU VCORE VID3			
GPU VCORE VID3					

I2CS ties into SMBus connection page (I2CS requires pullups even if not used)



HDCP Support



TMDs Backdrive Protection



Unused Clocks

GPU CLK27M_SS	GPU SS_INT
GPU XTALOUTBUFF	R8780
	R8781

GPU Straps

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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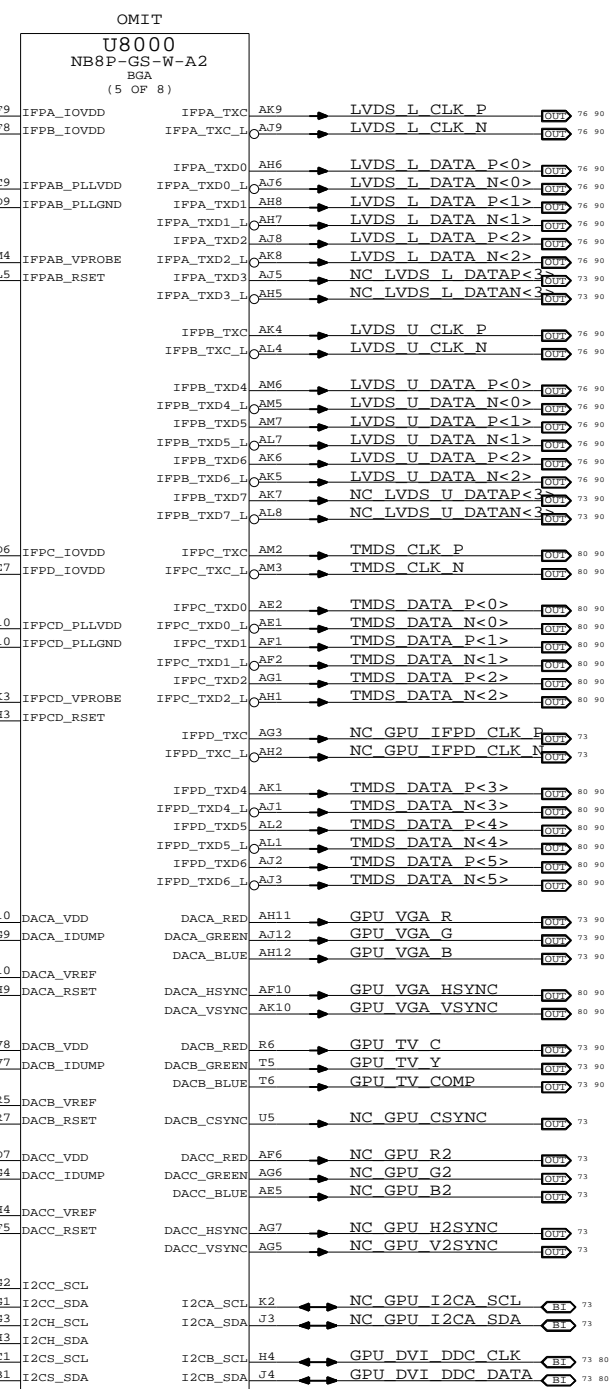
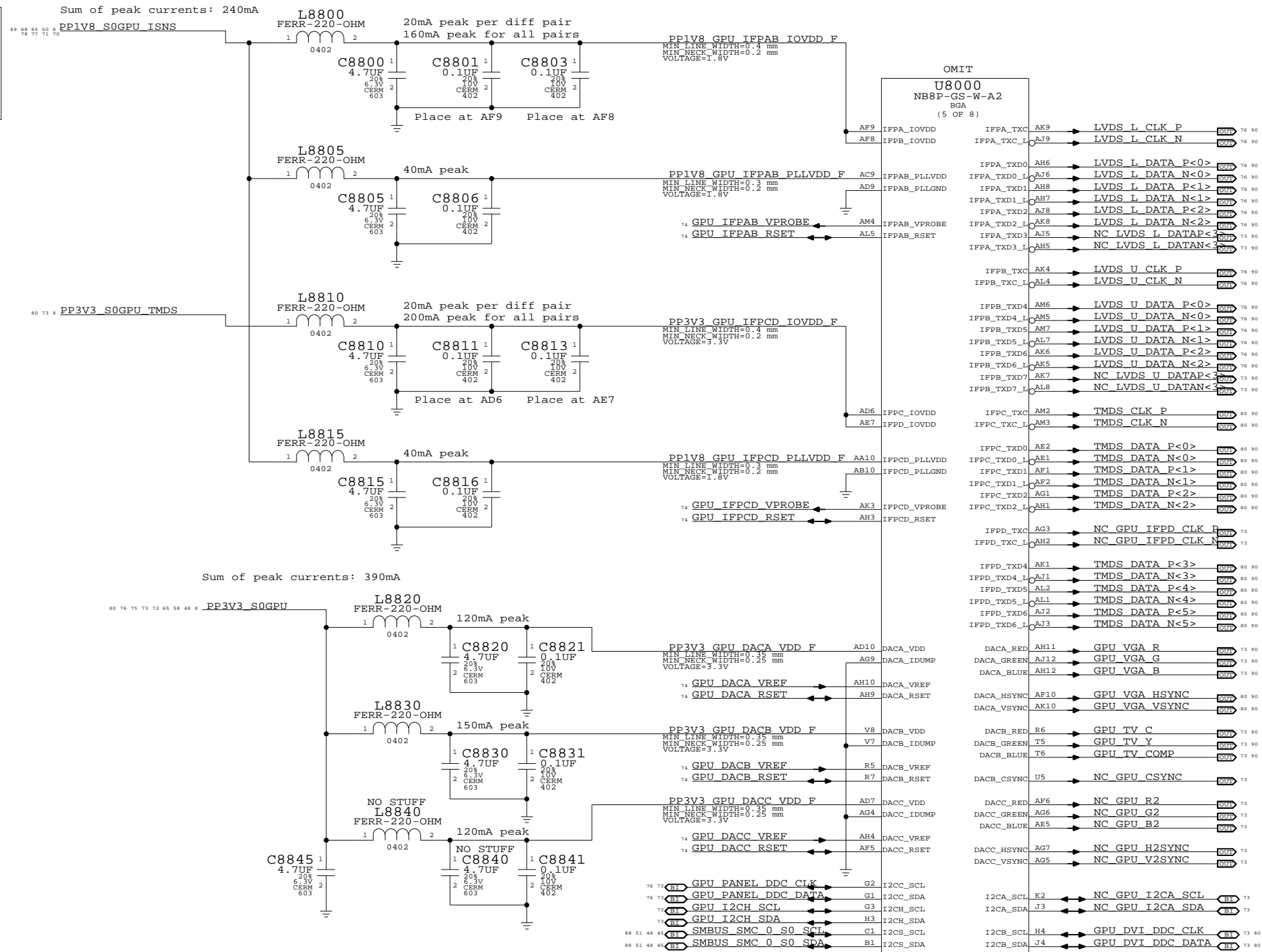
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	92
NONE	73	92	

Page Notes

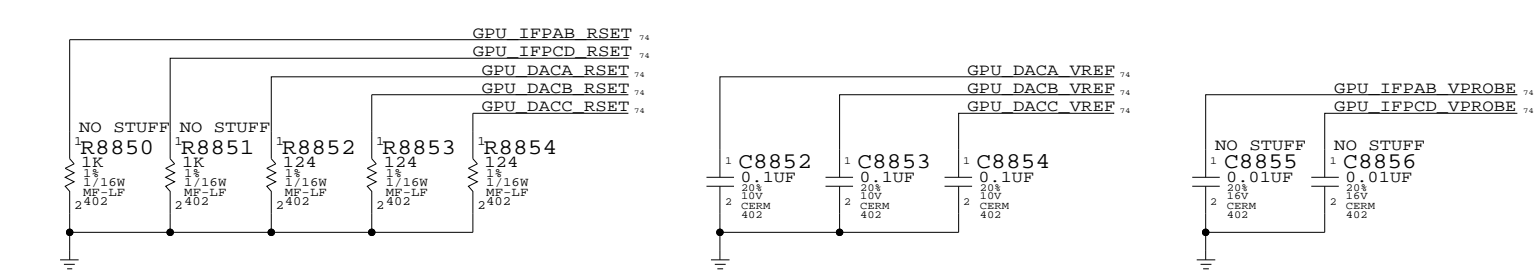
Power aliases required by this page:
 - =PP1V8_GPU_IFPX
 - =PP3V3_GPU_IFPCD_IOVDD
 - =PP3V3_GPU_DAC

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb



NV G84M Video Interfaces
 SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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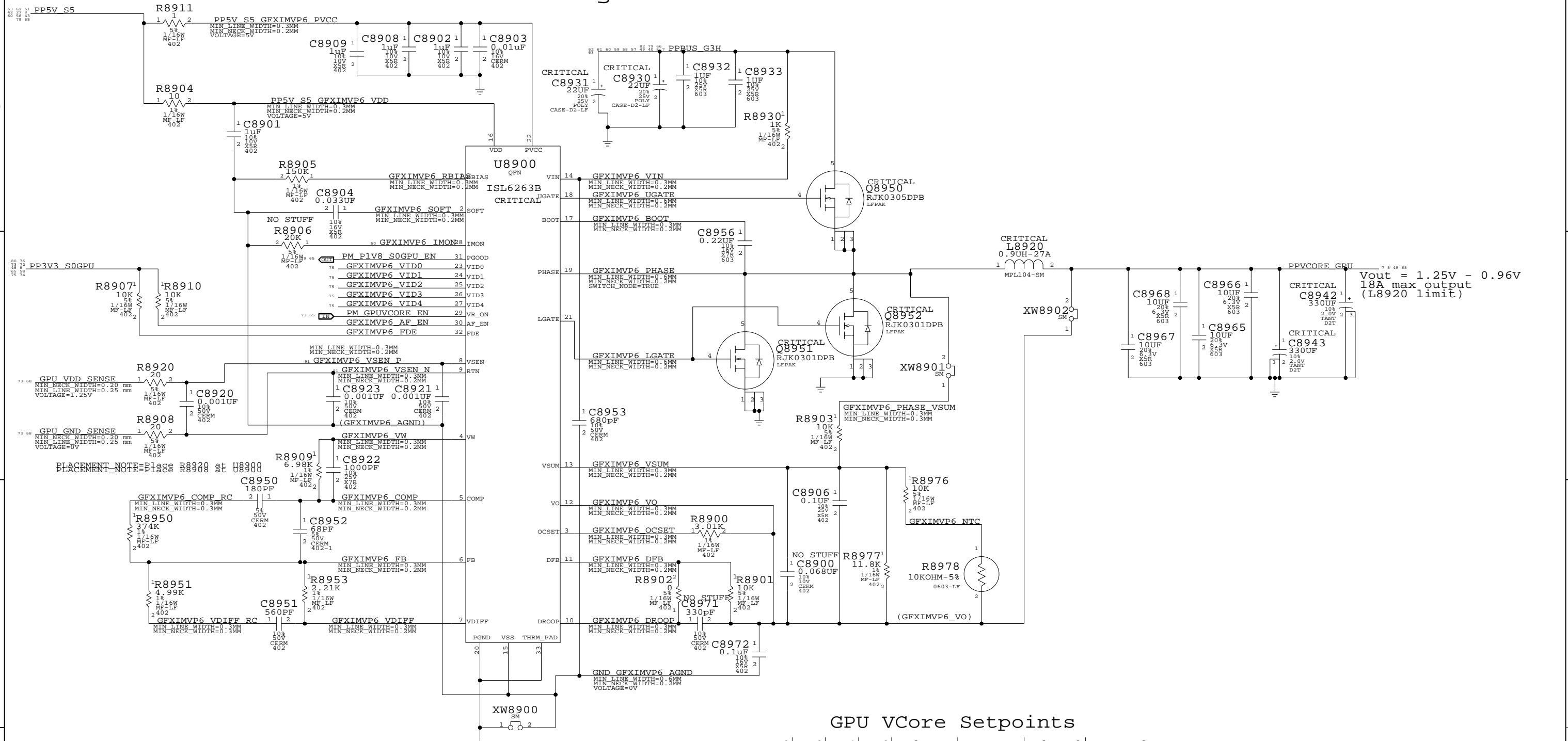
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	NONE	SHT	74 OF 92

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	0	1	1.05575V	M87, M88	M87	-
0	1	1	0	1.13300V	-	M88	M87
0	0	1	0	1.23600V	-	-	M88

Other VID states may not be valid

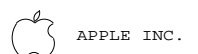
M87/M88 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P23V	GPUVID3_0, GPUVID2_0, GPUVID1_1, GPUVID0_0
GPUVID_1P13V	GPUVID3_0, GPUVID2_1, GPUVID1_1, GPUVID0_0
GPUVID_1P05V	GPUVID3_1, GPUVID2_0, GPUVID1_0, GPUVID0_1

GPU (G84M) Core Supply

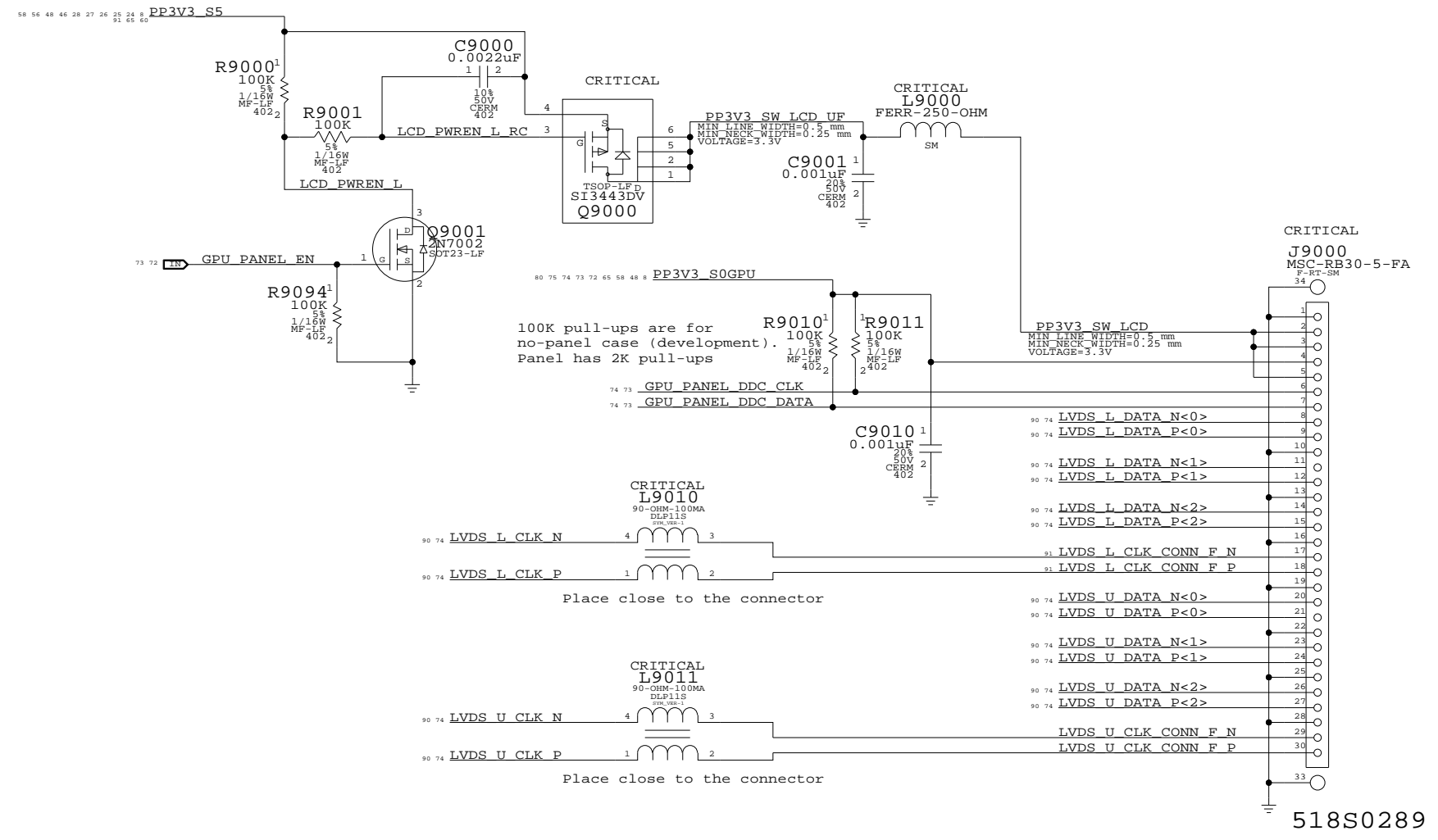
SYNC_MASTER=M87_MLB SYNC_DATE=09/26/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	75	92

LCD (LVDS) INTERFACE



LVDS Display Connector
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE		SHT	OF
NONE		76	92

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer A (Bot)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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Power aliases required by this page:
 - =PP1V8_S0_FB_VDD
 - =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B (Bot)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

NOTICE OF PROPRIETARY PROPERTY

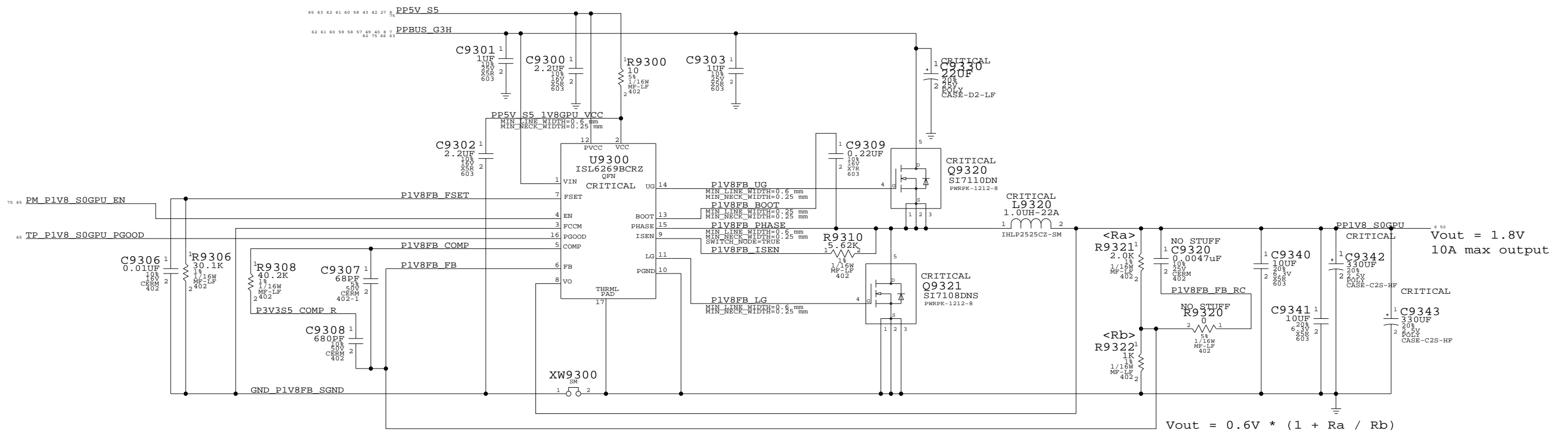
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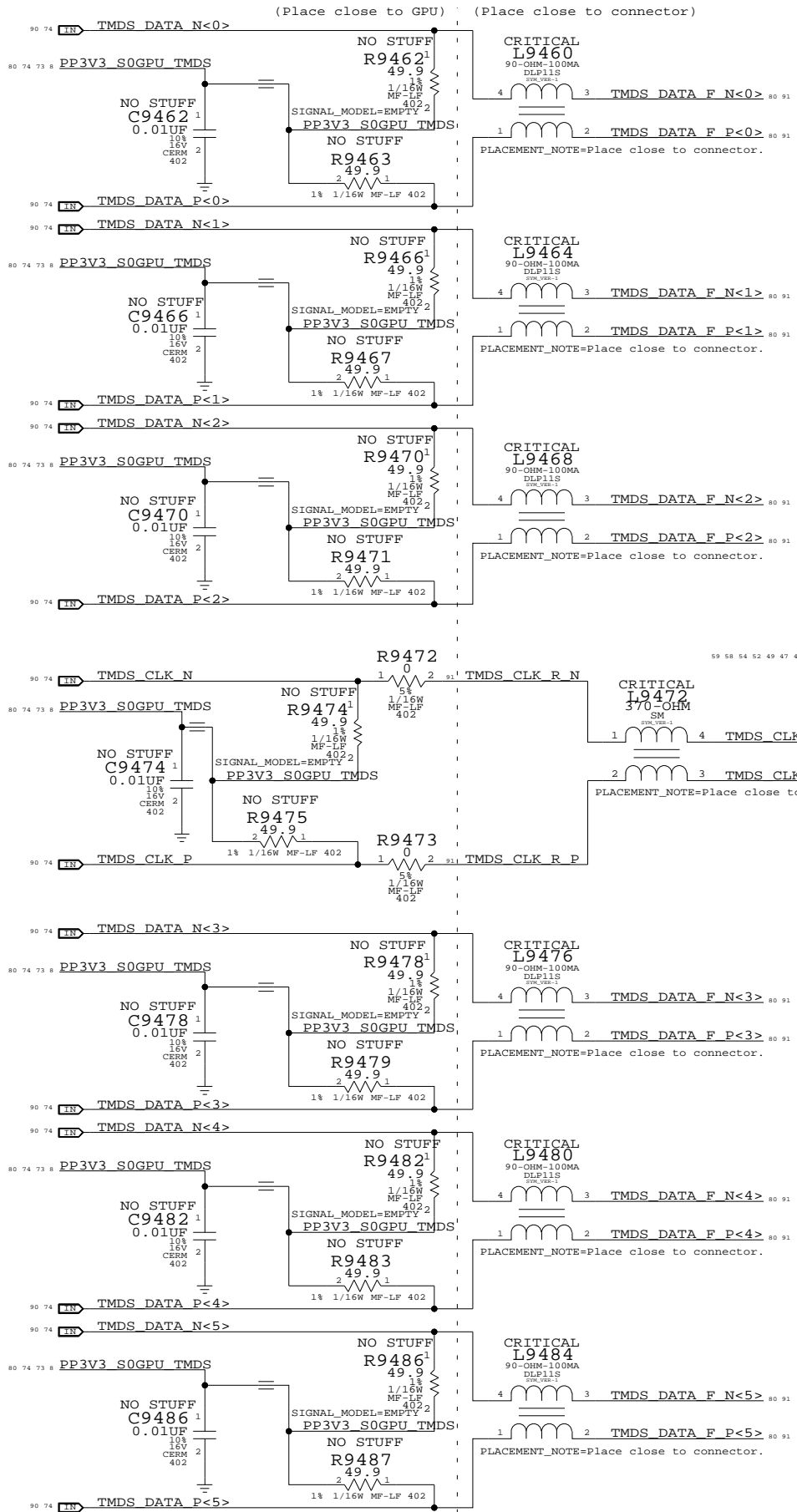
1.8V Frame Buffer Regulator



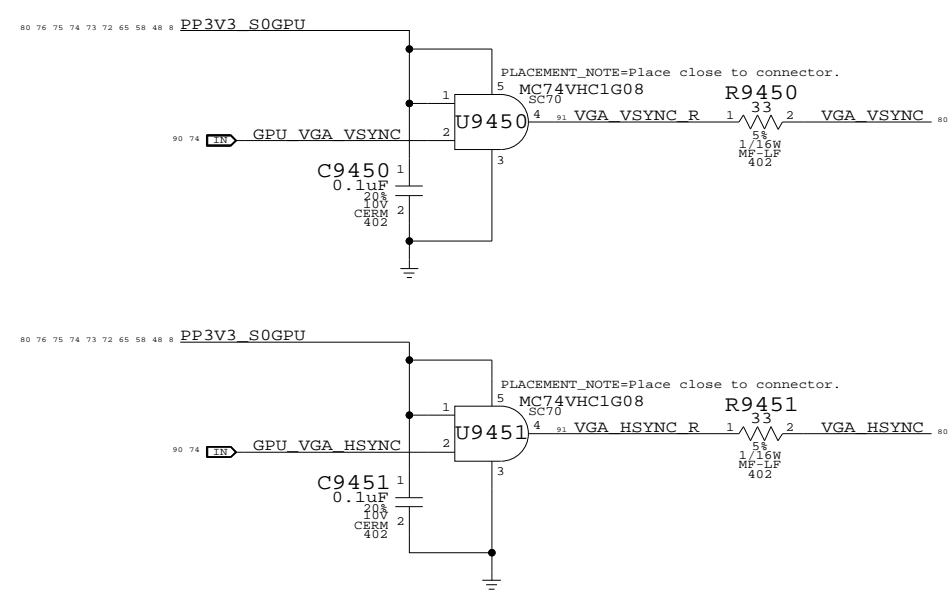
1.8V FB Power Supply
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	SIZE D	DRAWING NUMBER 051-7431	REV. A.0.0
	SCALE NONE	SHEET 79	OF 92

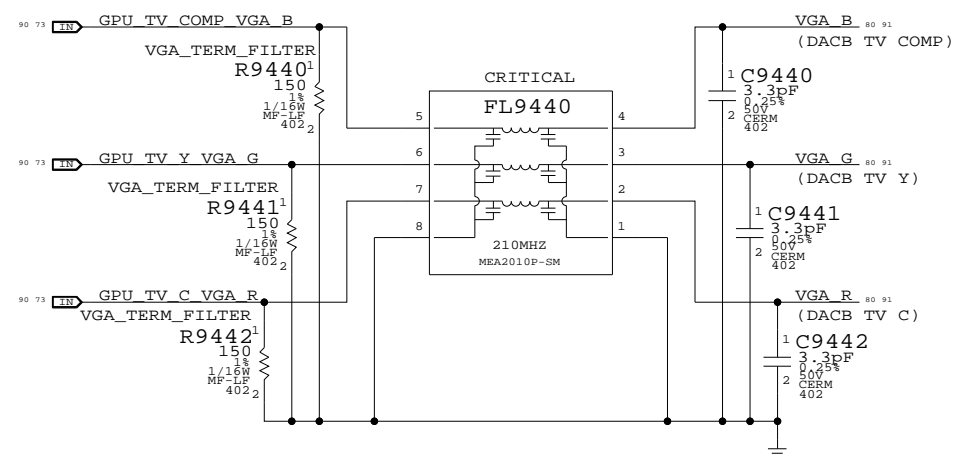
TMDS Filtering



VGA SYNC Buffers

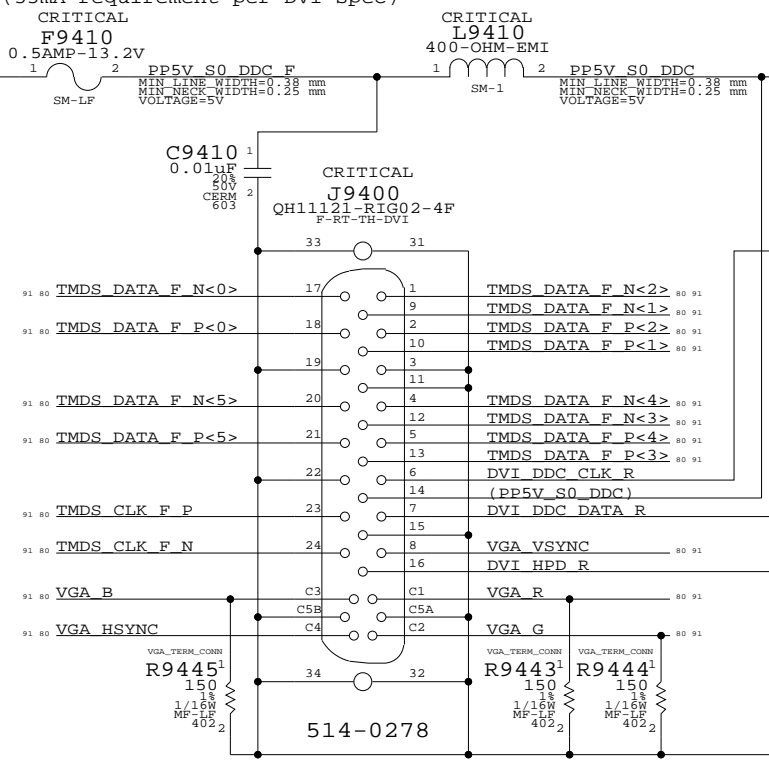


ANALOG FILTERING PLACE CLOSE TO CONNECTOR

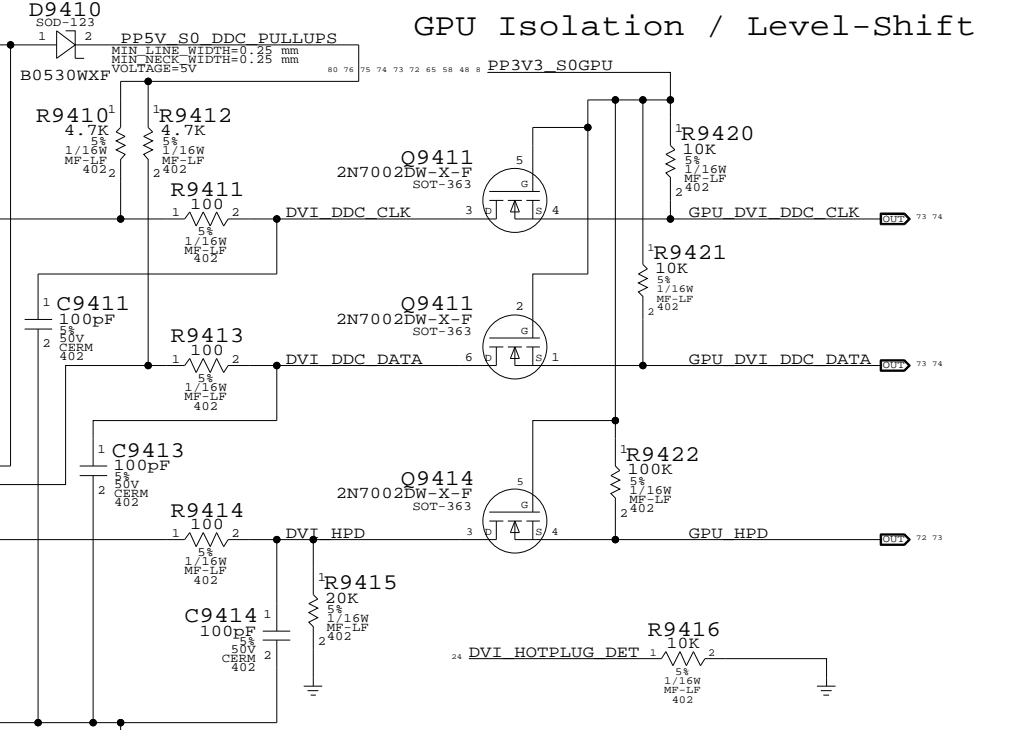


DVI INTERFACE

DVI DDC Current Limit (55mA requirement per DVI spec)



Isolation required for DVI->ADC Adapter



DVI Display Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

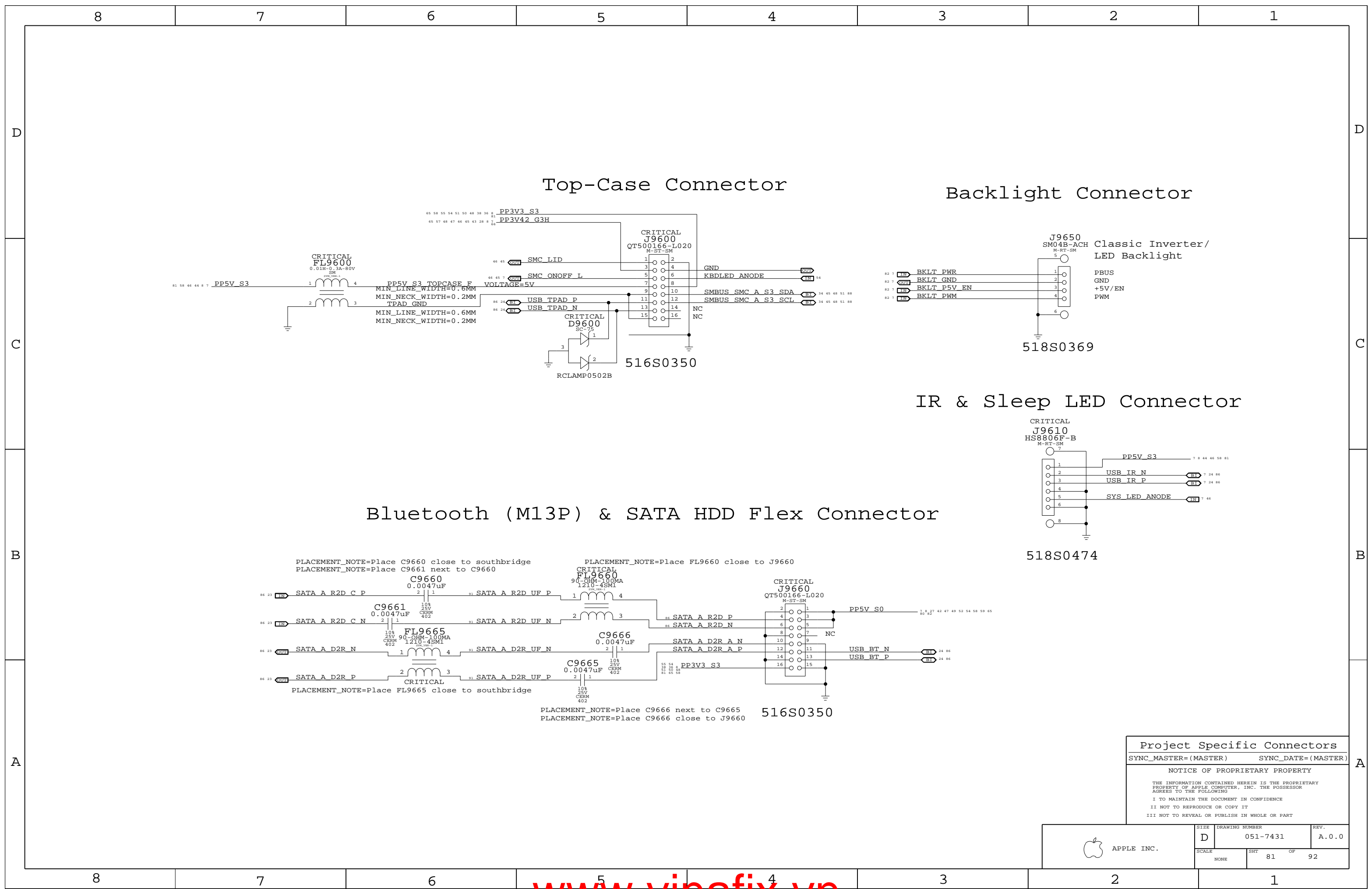
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	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	80	92	



Top-Case Connector

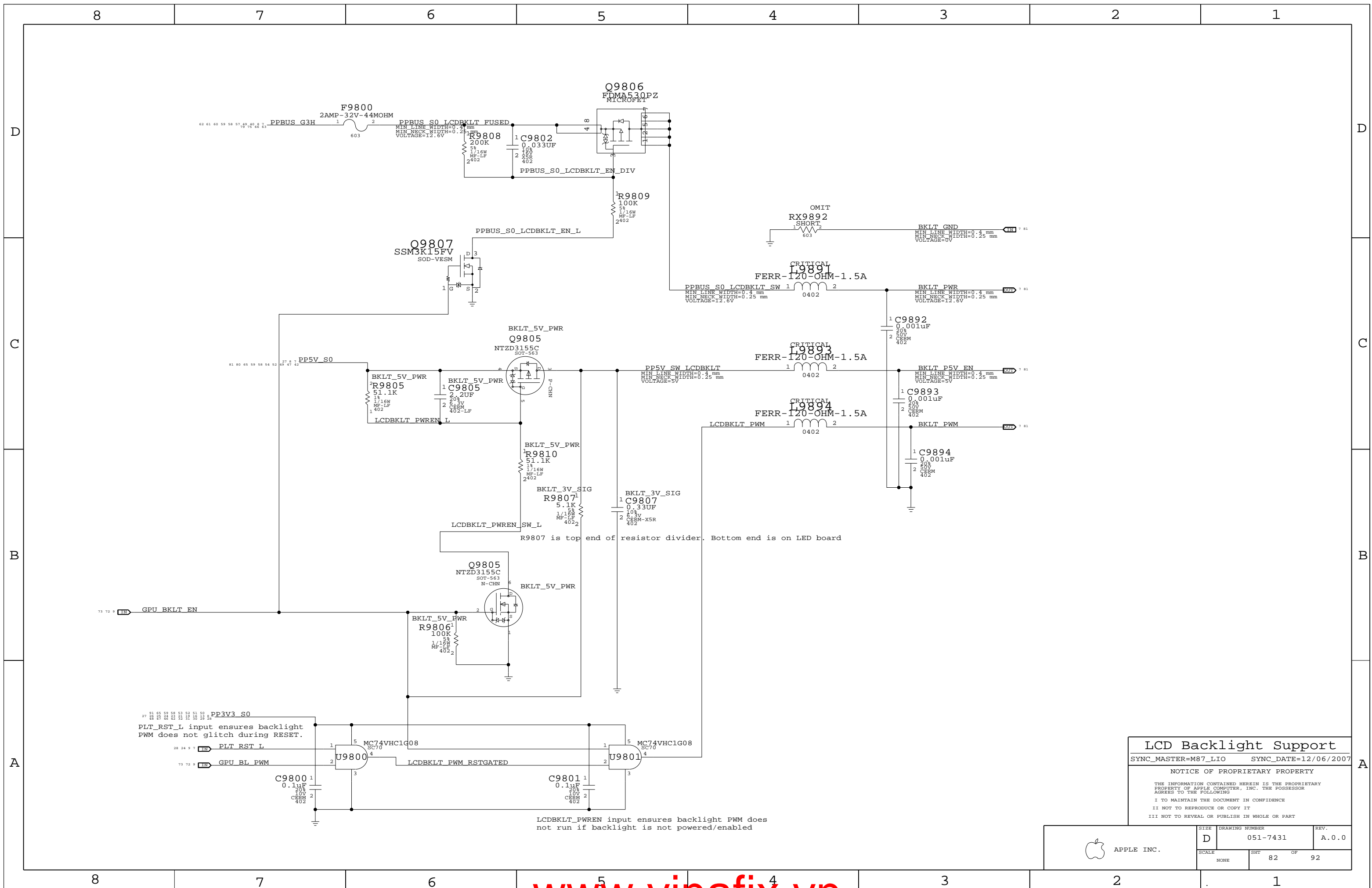
Backlight Connector

IR & Sleep LED Connector

Bluetooth (M13P) & SATA HDD Flex Connector

Project Specific Connectors
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE		SHT	OF
NONE		81	92



LCD Backlight Support

SYNC_MASTER=M87_LIO SYNC_DATE=12/06/2007

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	D	051-7431	A.0.0
SCALE	SHT	OF	REV.
NONE	82	92	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

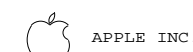
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BRQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	10 46 59
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FRGM_SB	CPU_55S		CPU INTR	10 23
CPU_FRGM_SB	CPU_55S		CPU NMI	10 23
CPU_FRGM_SB	CPU_55S		CPU A20M L	10 23
CPU_FRGM_SB	CPU_55S		CPU DPSTP L	7 10 23
CPU_FRGM_SB	CPU_55S		CPU IGNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FRGM_SB	CPU_55S		CPU SMI L	10 23
CPU_FRGM_SB	CPU_55S		CPU STPCLK L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2T01	PM DPRSLPVR	7 16 25 59
(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	7 59
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	7 10 16 23 59
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TEST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_1000	CLK_FSB	CLK_FSB	XDP CLK P	13 29 30 88
CLK_FSB_1000	CLK_FSB	CLK_FSB	XDP CLK N	13 29 30 88
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
CPU_VID<6..0>	CPU_55S	CPU_2T01	CPU VID<6..0>	11 12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 59
CPU_27P4S	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	59
CPU_27P4S	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	59

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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SCALE	SHT	OF
NONE	83	92

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
 CRT & TVDAC signal single-ended impedance varies by location:
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.
 - 50-ohm +/- 15% from first to second termination resistor.
 - 55-ohm +/- 15% from second termination resistor to connector.
 CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0> 67
	PCIE_100D	PCIE	PEG R2D N<15..0> 67
	PCIE_100D	PCIE	PEG R2D C P<15..0> 15 67
	PCIE_100D	PCIE	PEG R2D C N<15..0> 15 67
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0> 15 67
	PCIE_100D	PCIE	PEG D2R N<15..0> 15 67
	PCIE_100D	PCIE	PEG D2R C P<15..0> 67
	PCIE_100D	PCIE	PEG D2R C N<15..0> 67
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0> 16 24
	DMI_100D	DMI	DMI N2S N<3..0> 16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0> 16 24
	DMI_100D	DMI	DMI S2N N<3..0> 16 24
LVDS_A_CLK	LVDS_100D	LVDS	NC LVDS A CLKP 15 22
LVDS_A_CLK	LVDS_100D	LVDS	NC LVDS A CLKN 15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0> 15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0> 15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3> 15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3> 15 22
LVDS_B_CLK	LVDS_100D	LVDS	NC LVDS B CLKP 15 22
LVDS_B_CLK	LVDS_100D	LVDS	NC LVDS B CLKN 15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0> 15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0> 15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3> 15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3> 15 22
LVDS_IBG		LVDS	NC LVDS IBG 15 22
CRT_TVO_IREF		CRT	CRT TVO IREF
CRT_RED	CRT_50S	CRT	CRT RED
CRT_GREEN	CRT_50S	CRT	CRT GREEN
CRT_BLUE	CRT_50S	CRT	CRT BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R
TV_A_DAC	CRT_50S	TVDAC	TV A DAC
TV_B_DAC	CRT_50S	TVDAC	TV B DAC
TV_C_DAC	CRT_50S	TVDAC	TV C DAC


NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	84	92	

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Need to support MEM_*-style wildcards!

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MEM_A_CLK	MEM_70D	MEM_CLK	MEM CLK P<2..0> 16 31
	MEM_70D	MEM_CLK	MEM CLK N<2..0> 16 31
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<1..0> 16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<1..0> 16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<1..0> 16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<14..0> 16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BS<2..0> 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L 17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0> 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8> 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16> 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24> 17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32> 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40> 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48> 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56> 17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0> 17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1> 17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2> 17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3> 17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4> 17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5> 17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6> 17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7> 17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<0> 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<1> 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<2> 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<3> 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<4> 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<5> 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<6> 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7> 17 31
	MEM_85D	MEM_DQS	MEM A DQS N<7> 17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM CLK P<5..3> 16 32
	MEM_70D	MEM_CLK	MEM CLK N<5..3> 16 32
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<4..3> 16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<3..2> 16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<3..2> 16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0> 16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0> 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L 17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0> 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8> 17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16> 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24> 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32> 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40> 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48> 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56> 17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0> 17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1> 17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2> 17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3> 17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4> 17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5> 17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6> 17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7> 17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<0> 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<1> 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<2> 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<3> 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<4> 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<5> 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<6> 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7> 17 32
	MEM_85D	MEM_DQS	MEM B DQS N<7> 17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	85	92	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE PDD<15..0> 23 42
IDE_PDA	IDE_55S	IDE	IDE PDA<2..0> 23 42
IDE_PDCS	IDE_55S	IDE	IDE PDCS1 L 23 42
IDE_PDCCS	IDE_55S	IDE	IDE PDCCS3 L 23 42
IDE_CNVL	IDE_55S	IDE	IDE PDIOW L 23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE PDIOR L 23 42
IDE_CNVL	IDE_55S	IDE	IDE PDDACK L 23 42
IDE_CNVL	IDE_55S	IDE	IDE PDDREO 23 42
IDE_PDIORDY	IDE_55S	IDE	IDE PDIORDY 23 42
IDE_IRQ14	IDE_55S	IDE	IDE IRQ14 23 42
IDE_RST_L	IDE_55S	IDE	ODD RST 5VTOL L 24 42
SATA_A_R2D	SATA_100D	SATA	SATA A R2D C P 23 81
SATA_100D	SATA	SATA	SATA A R2D C N 23 81
SATA_100D	SATA	SATA	SATA A R2D P 81
SATA_100D	SATA	SATA	SATA A R2D N 81
SATA_A_D2R	SATA_100D	SATA	SATA A D2R P 23 81
SATA_100D	SATA	SATA	SATA A D2R N 23 81
SATA_100D	SATA	SATA	SATA A D2R C P 81
SATA_100D	SATA	SATA	SATA A D2R C N 81
SATA_B_R2D	SATA_100D	SATA	TP SATA B R2DP 23 42
SATA_100D	SATA	SATA	TP SATA B R2DN 23 42
SATA_100D	SATA	SATA	SATA B R2D P 23 42
SATA_100D	SATA	SATA	SATA B R2D N 23 42
SATA_B_D2R	SATA_100D	SATA	TP SATA B D2RP 23 42
SATA_100D	SATA	SATA	TP SATA B D2RN 23 42
SATA_100D	SATA	SATA	SATA B D2R C P 23 42
SATA_100D	SATA	SATA	SATA B D2R C N 23 42
SATA_C_R2D	SATA_100D	SATA	TP SATA C R2DP 23 42
SATA_100D	SATA	SATA	TP SATA C R2DN 23 42
SATA_100D	SATA	SATA	SATA C R2D P 23 42
SATA_100D	SATA	SATA	SATA C R2D N 23 42
SATA_C_D2R	SATA_100D	SATA	TP SATA C D2RP 23 42
SATA_100D	SATA	SATA	TP SATA C D2RN 23 42
SATA_100D	SATA	SATA	SATA C D2R C P 23 42
SATA_100D	SATA	SATA	SATA C D2R C N 23 42
SATA_RBIAS	SATA_55S	SATA	SATA RBIAS 23 42
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK 23 34
HDA_55S	HDA	HDA	HDA BIT CLK R 23 34
HDA_SYNC	HDA_55S	HDA	HDA SYNC 23 34
HDA_55S	HDA	HDA	HDA SYNC R 23 34
HDA_RST_L	HDA_55S	HDA	HDA RST L 23 34
HDA_55S	HDA	HDA	HDA RST L R 23 34
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0 23 34
HDA_55S	HDA	HDA	HDA SDIN CODEC 23 34
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT 23 34
HDA_55S	HDA	HDA	HDA SDOUT R 23 34
USB_EXT_A	USB_90D	USB	USB EXT_A P 24 43
USB_90D	USB	USB	USB EXT_A N 24 43
USB_90D	USB	USB	USB EXT_A MUXED P 24 43
USB_90D	USB	USB	USB EXT_A MUXED N 24 43
USB_MINI	USB_90D	USB	USB MINI P 24 34
USB_90D	USB	USB	USB MINI N 24 34
USB_EXTD	USB_90D	USB	TP USB EXTDP 9 24
USB_90D	USB	USB	TP USB EXTDN 9 24
USB_CAMERA	USB_90D	USB	USB CAMERA P 24 44
USB_90D	USB	USB	USB CAMERA N 24 44
USB_BT	USB_90D	USB	USB BT P 24 81
USB_90D	USB	USB	USB BT N 24 81
USB_TPAD	USB_90D	USB	USB TPAD P 24 81
USB_90D	USB	USB	USB TPAD N 24 81
USB_IR	USB_90D	USB	USB IR P 7 24 81
USB_90D	USB	USB	USB IR N 7 24 81
USB_EXTB	USB_90D	USB	USB EXTB P 24 34
USB_90D	USB	USB	USB EXTB N 24 34
USB_EXCARD	USB_90D	USB	USB EXCARD P 24 34
USB_90D	USB	USB	USB EXCARD N 24 34
USB_EXTC	USB_90D	USB	USB EXTC P 24 34
USB_90D	USB	USB	USB EXTC N 24 34
USB_RBIAS	USB_60S	USB	USB RBIAS 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS SB_SCL 25 29 31 32 34 48
SMB_SB_SDA	SMB_55S	SMB	SMBUS SB_SDA 25 29 31 32 34 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS SB ME_SCL 25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS SB ME_SDA 25 48
SPI_SCLK	SPI_55S	SPI	SPI SCLK R 24 56
SPI_55S	SPI	SPI	SPI SCLK 56
SPI_55S	SPI	SPI	SPI A SCLK R 56
SPI_55S	SPI	SPI	SPI B SCLK R 56
SPI_SI	SPI_55S	SPI	SPI SI R 24 56
SPI_55S	SPI	SPI	SPI SI 56
SPI_55S	SPI	SPI	SPI A SI R 56
SPI_55S	SPI	SPI	SPI B SI R 56
SPI_SO	SPI_55S	SPI	SPI SO 24 56
SPI_55S	SPI	SPI	SPI A SO R 56
SPI_55S	SPI	SPI	SPI B SO R 56
SPI_55S	SPI	SPI	SPI B SO R 56
SPI_CE_L0	SPI_55S	SPI	SPI CE R L<0> 24 56
SPI_55S	SPI	SPI	SPI CE L<0> 56
SPI_CE_L1	SPI_55S	SPI	SPI CE R L<1> 56
SPI_55S	SPI	SPI	SPI CE L<1> 56

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

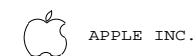
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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	86	92

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	24
PCI_CNTRL	PCI_55S	PCI	PCI SERR_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT_L	7 24 38 47
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	24
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	24
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT PIROC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT PIROD_L	24 38
INT_PIRQF_L	PCI_55S	PCI	INT PIROF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C P	
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R P	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C P	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R P	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C P	24 34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C N	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R P	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R N	24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C P	
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R P	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P	24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R P	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R N	24 34
GLAN_COMP			GLAN COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C N	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D P	35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R P	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R N	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C P	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
SCALE	SHT	OF	
NONE	87	92	

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
CK505_CPUH	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 29 30 88
CK505_CPUN	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 29 30 88
CK505_NBH	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 88
CK505_NBN	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 88
CK505_IPTH	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 83 88
CK505_IPTN	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 83 88
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PC11	CLK_MED_55S	CLK_MED	CK505_PC11_CLK	29 30
CK505_PC12	CLK_MED_55S	CLK_MED	TP CK505_PC12_CLK	29 30
CK505_PC13	CLK_MED_55S	CLK_MED	CK505_PC13_CLK	29 30
CK505_PC14	CLK_MED_55S	CLK_MED	TP CK505_PC14_CLK	29 30
CK505_PC15	CLK_MED_55S	CLK_MED	CK505_PC15_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M_SS	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	TP_NB_CLK100M_DPLLSS_P	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	TP_NB_CLK100M_DPLLSS_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 67 88
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 67 88
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 88
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 88
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 88
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 88
CK505_SRC9	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 88
CK505_SRC10	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 88
CK505_SRC11	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 88
CK505_SRC12	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 88
CK505_SRC13	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 88
CK505_SRC14	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 88
CK505_SRC15	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7P	29 30
CK505_SRC16	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7N	29 30
CK505_SRC17	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 88
CK505_SRC18	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 88
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 29 30 88
(CK505_CPUN)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 29 30 88
(CK505_NBH)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 88
(CK505_NBN)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 88
(CK505_IPTH)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 83 88
(CK505_IPTN)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 83 88
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PC11)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PC12)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	30 45
(CK505_PC13)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_PCI4 is project-specific	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTRL	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_P	
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_N	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_P	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_N	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 67 88
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 67 88
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 88
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 88
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 88
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 88
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 88
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 88
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 88
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 88
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 88
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 88
(CK505_SRC7)	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 88
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 88

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	34 45 48 51 81
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	34 45 48 51 81
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	41 45
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	41 45
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	45 48 51 74
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	45 48 51 74
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 45 48 57
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 45 48 57
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	45 48 55
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	45 48 55

Clock & SMC Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	88	92

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
EW_D_CTL	EW_55S	FW	FW LINK<7..0>
EW_D_CTL	EW_55S	FW	FW CTL<1..0>
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW LINK LCLK
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW PHY LCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW LINK PCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW PHY PCLK 38 39
EW_LKON	EW_55S	FW	FW LKON
EW_LKON	EW_55S	FW	FW LKON R
EW_LPS	EW_55S	FW	FW LPS 38 39
EW_LREQ	EW_55S	FW	FW LREQ 38 39
EW_PINT	EW_55S	FW	FW PINT 38 39
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI R
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI
EW_0_TPA	EW_110D	EW_TP	FW PORT0 TPA P 39 41
EW_0_TPA	EW_110D	EW_TP	FW PORT0 TPA N 39 41
EW_0_TPB	EW_110D	EW_TP	FW PORT0 TPB P 39 41
EW_0_TPB	EW_110D	EW_TP	FW PORT0 TPB N 39 41
EW_1_TPA	EW_110D	EW_TP	FW PORT1 TPA P 39 41
EW_1_TPA	EW_110D	EW_TP	FW PORT1 TPA N 39 41
EW_1_TPB	EW_110D	EW_TP	FW PORT1 TPB P 39 41
EW_1_TPB	EW_110D	EW_TP	FW PORT1 TPB N 39 41
Port 2 Not Used			

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	89	92

GDDR3 Frame Buffer Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	=55_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>	69 70 77
FB_A_CLK_N	GDDR3_80D	GDDR3_CLK	FB A CLK N<0>	69 70 77
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>	69 70 77
FB_B_CLK_N	GDDR3_80D	GDDR3_CLK	FB B CLK N<1>	69 70 77
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<1..0>	69 70 77
FB_B_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<11..6>	69 70 77
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A BA<2..0>	69 70 77
FB_B_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B RAS L	69 70 77
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A CAS L	69 70 77
FB_B_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B WE L	69 70 77
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A CE	69 70 77
FB_B_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B CS0 L	69 70 77
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A DRAM RST	69 70 77
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB B LMA<5..2>	69 70 77
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB C UMA<5..2>	69 70 77
FB_A_DQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<0>	69 70 77
FB_B_DQS1	GDDR3_50SE	GDDR3_DQS	FB B WDQS<1>	69 70 77
FB_C_DQS2	GDDR3_50SE	GDDR3_DQS	FB C WDQS<2>	69 70 77
FB_D_DQS3	GDDR3_50SE	GDDR3_DQS	FB D WDQS<3>	69 70 77
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<0>	69 70 77
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB B RDQS<1>	69 70 77
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB C RDQS<2>	69 70 77
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB D RDQS<3>	69 70 77
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<7..0>	69 70 77
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<15..8>	69 70 77
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB C DQ<23..16>	69 70 77
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB D DQ<31..24>	69 70 77
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM L<0>	69 70 77
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM L<1>	69 70 77
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB C DQM L<2>	69 70 77
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB D DQM L<3>	69 70 77
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<4>	69 70 77
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB B WDQS<5>	69 70 77
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB C WDQS<6>	69 70 77
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB D WDQS<7>	69 70 77
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<4>	69 70 77
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB B RDQS<5>	69 70 77
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB C RDQS<6>	69 70 77
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB D RDQS<7>	69 70 77
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<39..32>	69 70 77
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<47..40>	69 70 77
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB C DQ<55..48>	69 70 77
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB D DQ<63..56>	69 70 77
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM L<4>	69 70 77
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM L<5>	69 70 77
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB C DQM L<6>	69 70 77
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB D DQM L<7>	69 70 77

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB C CLK P<0>	69 71 78
FB_C_CLK_N	GDDR3_80D	GDDR3_CLK	FB C CLK N<0>	69 71 78
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB D CLK P<1>	69 71 78
FB_D_CLK_N	GDDR3_80D	GDDR3_CLK	FB D CLK N<1>	69 71 78
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C MA<1..0>	69 71 78
FB_D_CMD	GDDR3_40R55SE	GDDR3_CMD	FB D MA<11..6>	69 71 78
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C BA<2..0>	69 71 78
FB_D_CMD	GDDR3_40R55SE	GDDR3_CMD	FB D RAS L	69 71 78
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C CAS L	69 71 78
FB_D_CMD	GDDR3_40R55SE	GDDR3_CMD	FB D WE L	69 71 78
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C CE	69 71 78
FB_D_CMD	GDDR3_40R55SE	GDDR3_CMD	FB D CS0 L	69 71 78
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C DRAM RST	69 71 78
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB D LMA<5..2>	69 71 78
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB C UMA<5..2>	69 71 78
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB C WDQS<0>	69 71 78
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB D WDQS<1>	69 71 78
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB C WDQS<2>	69 71 78
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB D WDQS<3>	69 71 78
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB C RDQS<0>	69 71 78
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB D RDQS<1>	69 71 78
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB C RDQS<2>	69 71 78
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB D RDQS<3>	69 71 78
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB C DQ<7..0>	69 71 78
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB D DQ<15..8>	69 71 78
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB C DQ<23..16>	69 71 78
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB D DQ<31..24>	69 71 78
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB C DQM L<0>	69 71 78
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB D DQM L<1>	69 71 78
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB C DQM L<2>	69 71 78
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB D DQM L<3>	69 71 78
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB C WDQS<4>	69 71 78
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB D WDQS<5>	69 71 78
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB C WDQS<6>	69 71 78
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB D WDQS<7>	69 71 78
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB C RDQS<4>	69 71 78
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB D RDQS<5>	69 71 78
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB C RDQS<6>	69 71 78
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB D RDQS<7>	69 71 78
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB C DQ<39..32>	69 71 78
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB D DQ<47..40>	69 71 78
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB C DQ<55..48>	69 71 78
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB D DQ<63..56>	69 71 78
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB C DQM L<4>	69 71 78
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB D DQM L<5>	69 71 78
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB C DQM L<6>	69 71 78
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB D DQM L<7>	69 71 78

G84M Net Properties

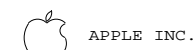
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M	30 72 73
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M SS	30 72 73
LVDS_L_CLK	LVDS_100D	LVDS	LVDS L CLK P	74 76
LVDS_L_CLK	LVDS_100D	LVDS	LVDS L CLK N	74 76
LVDS_L_DATA	LVDS_100D	LVDS	LVDS L DATA P<2..0>	74 76
LVDS_L_DATA	LVDS_100D	LVDS	LVDS L DATA N<2..0>	74 76
LVDS_L_DATA	LVDS_100D	LVDS	NC LVDS L DATAP<3>	73 74
LVDS_L_DATA	LVDS_100D	LVDS	NC LVDS L DATAN<3>	73 74
LVDS_U_CLK	LVDS_100D	LVDS	LVDS U CLK P	74 76
LVDS_U_CLK	LVDS_100D	LVDS	LVDS U CLK N	74 76
LVDS_U_DATA	LVDS_100D	LVDS	LVDS U DATA P<2..0>	74 76
LVDS_U_DATA	LVDS_100D	LVDS	LVDS U DATA N<2..0>	74 76
LVDS_U_DATA	LVDS_100D	LVDS	NC LVDS U DATAP<3>	73 74
LVDS_U_DATA	LVDS_100D	LVDS	NC LVDS U DATAN<3>	73 74
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK P	74 80
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK N	74 80
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA P<5..0>	74 80
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA N<5..0>	74 80
VGA_B_TV_C	VGA_50S	VGA	GPU TV C VGA R	73 80
VGA_G_TV_Y	VGA_50S	VGA	GPU TV Y VGA G	73 80
VGA_B_TV_COMP	VGA_50S	VGA	GPU TV COMP VGA B	73 80
VGA_50S	VGA_50S	VGA	GPU VGA R	73 74
VGA_50S	VGA_50S	VGA	GPU VGA G	73 74
VGA_50S	VGA_50S	VGA	GPU VGA B	73 74
VGA_50S	VGA_50S	VGA	GPU TV C	73 74
VGA_50S	VGA_50S	VGA	GPU TV Y	73 74
VGA_50S	VGA_50S	VGA	GPU TV COMP	73 74
VGA_SYNC	VGA_55S	VGA_SYNC	GPU VGA HSYNC	74 80
VGA_SYNC	VGA_55S	VGA_SYNC	GPU VGA VSYNC	74 80

GPU (G84M) Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=10/02/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	90	92

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	OVERRIDE	OVERRIDE	0.100 MM	2.54 MM	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4, ISL10			0.100 MM	2.54 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M87 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P 34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N 34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0> 37
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0> 37
	ENET_100D	ENETCONN	ENETCONN_P<3..0> 37
	ENET_100D	ENETCONN	ENETCONN_N<3..0> 37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N 41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P 81
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N 81
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P 81
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N 81
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_P 43
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_N 43
(USB_EXT_A)	USB_90D	USB	USB2_RT_P 43
(USB_EXT_A)	USB_90D	USB	USB2_RT_N 43
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_P 43
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_N 43
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P 7 44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N 7 44
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_VSEN_P 75
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_VSEN_N 75
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	NBCOREISNS_P 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	NBCOREISNS_N 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_P 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_N 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V25ISNS_P 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V25ISNS_N 50
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPUTHMSNS_D2_P 7 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPUTHMSNS_D2_N 7 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THERMD_P 10 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THERMD_N 10 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPUTHMSNS_D_P 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPUTHMSNS_D_N 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_P 51 72 73
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_N 51 72 73
THERM_DIFFPAIR	THERM_1T01_55S	THERM	HSTHMSNS_D_P 7 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	HSTHMSNS_D_N 7 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	RSFSTHMSNS_D_P 7 51
THERM_DIFFPAIR	THERM_1T01_55S	THERM	RSFSTHMSNS_D_N 7 51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P 76
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N 76
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_R_P 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_R_N 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GPIUSNS_R_P 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GPIUSNS_R_N 50
	TMDS_100D	TMDS	TMDS_CLK_R_P 80
	TMDS_100D	TMDS	TMDS_CLK_R_N 80
	TMDS_100D	TMDS	TMDS_CLK_F_P 80
	TMDS_100D	TMDS	TMDS_CLK_F_N 80
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0> 80
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0> 80
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R 80
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G 80
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B 80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R 80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R 80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC 80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC 80
	PP1V8_MEM		PP1V8_S3 8 31 32 38 50 62 91
	PP1V8_MEM		PP1V8_S3 8 31 32 38 50 62 91
	GND		GND
	ENET_POWER		ENET_POWER
	SB_POWER		PP3V3_S5 8 24 25 26 27 28 46 48 56 58 60
	SB_POWER		PP3V3_S0 8 24 25 26 27 28 46 48 56 58 60
	SB_POWER		PP1V5_S0 8 11 12 22 26 27 34 63
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GPIUSNS_P 50
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GPIUSNS_N 50
	FW_POWER		FW_POWER

Project Specific Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

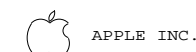
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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	91	92

M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2, ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
46_OHM_SE	TOP, BOTTOM	Y	0.126 MM	0.126 MM			
46_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	N	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

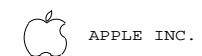
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M87_MLB SYNC_DATE=10/03/2007

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