

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# SCHEM, MLB, M82

## PVT

11/14/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
		546198			

Page	(-,CS#)	Contents	Sync	Date
1	1	Table of Contents	N/A	N/A
2	2	System Block Diagram	WFERRY-WF	05/11/2006
3	3	Power Block Diagram	POWER	06/30/2005
4	4	CONFIGURATION OPTIONS	(N/A)	(N/A)
5	5	Acoustic Cap BOM Config Tables	N/A	N/A
6	6	ICT Test Points	(MASTER)	(MASTER)
7	7	Functional Test and No-Tests	(MASTER)	(MASTER)
8	8	Power Aliases	WFERRY	06/15/2006
9	9	SIGNAL ALIAS /RESET	(MASTER)	(MASTER)
10	10	CPU FSB	(MASTER)	(MASTER)
11	11	CPU Power & Ground	(MASTER)	(MASTER)
12	12	CPU Decoupling & VID	MSARWAR	04/26/2006
13	13	extended Debug Port (XDP)	M75	01/24/2007
14	14	NB CPU Interface	(MASTER)	(MASTER)
15	15	NB PEG / Video Interfaces	M70	01/09/2007
16	16	NB Misc Interfaces	M70	01/09/2007
17	17	NB DDR2 Interfaces	M70	01/09/2007
18	18	NB Power 1	M70	01/09/2007
19	19	NB Power 2	M70	01/09/2007
20	20	NB Grounds	M70	01/09/2007
21	21	NB Standard Decoupling	M70	01/09/2007
22	22	NB Graphics Decoupling	M70	01/09/2007
23	23	SB Enet, Disk, FSB, LPC	M70	01/09/2007
24	24	SB PCI, PCIE, DMI, USB	M70	01/09/2007
25	25	SB Pwr Mgt, GPIO, Clink	M70	01/09/2007
26	26	SB Power & Ground	M70	01/09/2007
27	27	SB Decoupling	M70	02/01/2007
28	28	SB Misc	M70	01/09/2007
29	29	Clock (CK505)	M70	02/01/2007
30	30	Clock Termination	M70	01/09/2007
31	31	DDR2 DRAM Channel A	(MASTER)	(MASTER)
32	32	DDR2 DRAM Channel B	(MASTER)	(MASTER)
33	33	Memory Active Termination	M70	01/09/2007
34	34	DDR2 BYPASSING 1	MEMORY	06/20/2005
35	35	DDR2 BYPASSING 2	MEMORY	06/20/2005
36	36	Wireless M93 Connector	M70	01/09/2007
37	37	Hatch and Audio Connectors	(MASTER)	(MASTER)
38	38	PATA HDD CONNECTOR	(MASTER)	(MASTER)
39	39	USB EXTERNAL CONNECTORS	M70	01/09/2007
40	40	IPD Connector	M70	01/09/2007
41	41	SMC	M70	01/09/2007

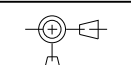

Page	(-,CS#)	Contents	Sync	Date
42	50	SMC SUPPORT	M70	01/09/2007
43	51	LPC+SPI Debug Connector	M70	01/09/2007
44	52	SMBUS CONNECTIONS	M70	01/09/2007
45	53	Voltage Sensors	M70	01/09/2007
46	55	TEMPERATURE SENSORS	M70	01/09/2007
47	56	Fan	M70	01/09/2007
48	59	Sudden Motion Sensor (SMS)	M76_MLB	01/12/2007
49	61	SPI ROMs	WFERRY	04/26/2006
50	69	DC-In & Battery Connectors	M70	01/09/2007
51	70	S0 FETS & Power Sequencing	M70	01/09/2007
52	71	IMVP6 CPU VCore Regulator	POWER	07/13/2005
53	72	Render VCore Supplies	(MASTER)	(MASTER)
54	73	1.5V/1.05V Supplies	M70	01/09/2007
55	75	1.8V/0.9V Supplies	M70	01/09/2007
56	76	5V/3.3V Supplies	M70	02/01/2007
57	77	3.42V/1.25V Switcher	M70	01/09/2007
58	78	S3 FET & S3/S5 Control	M70	02/01/2007
59	79	PBUS Supply/Battery Charger	M70	01/09/2007
60	90	LVDS,Camera Conn. and ALS Conn.	GPU	06/23/2006
61	92	SDVO/TMDS Tx	GRAPHIC	06/06/2005
62	93	HDCP uController		
63	94	DVI CONNECTIONS	M70	01/09/2007
64	97	LED Backlight Driver	(MASTER)	(MASTER)
65	99	Additional CPU/GPU Decoupling		
66	100	CPU/FSB Constraints	T9	01/30/2007
67	101	NB Constraints	T9	01/30/2007
68	102	Memory Constraints	T9	01/30/2007
69	103	SB Constraints (1 of 2)	T9	01/30/2007
70	104	SB Constraints (2 of 2)	T9	01/30/2007
71	105	Clock & SMC Constraints	T9	01/30/2007
72	108	M82 Power and Ground Nets	(MASTER)	(MASTER)
73	109	M82 Rule Definitions	(MASTER)	(MASTER)

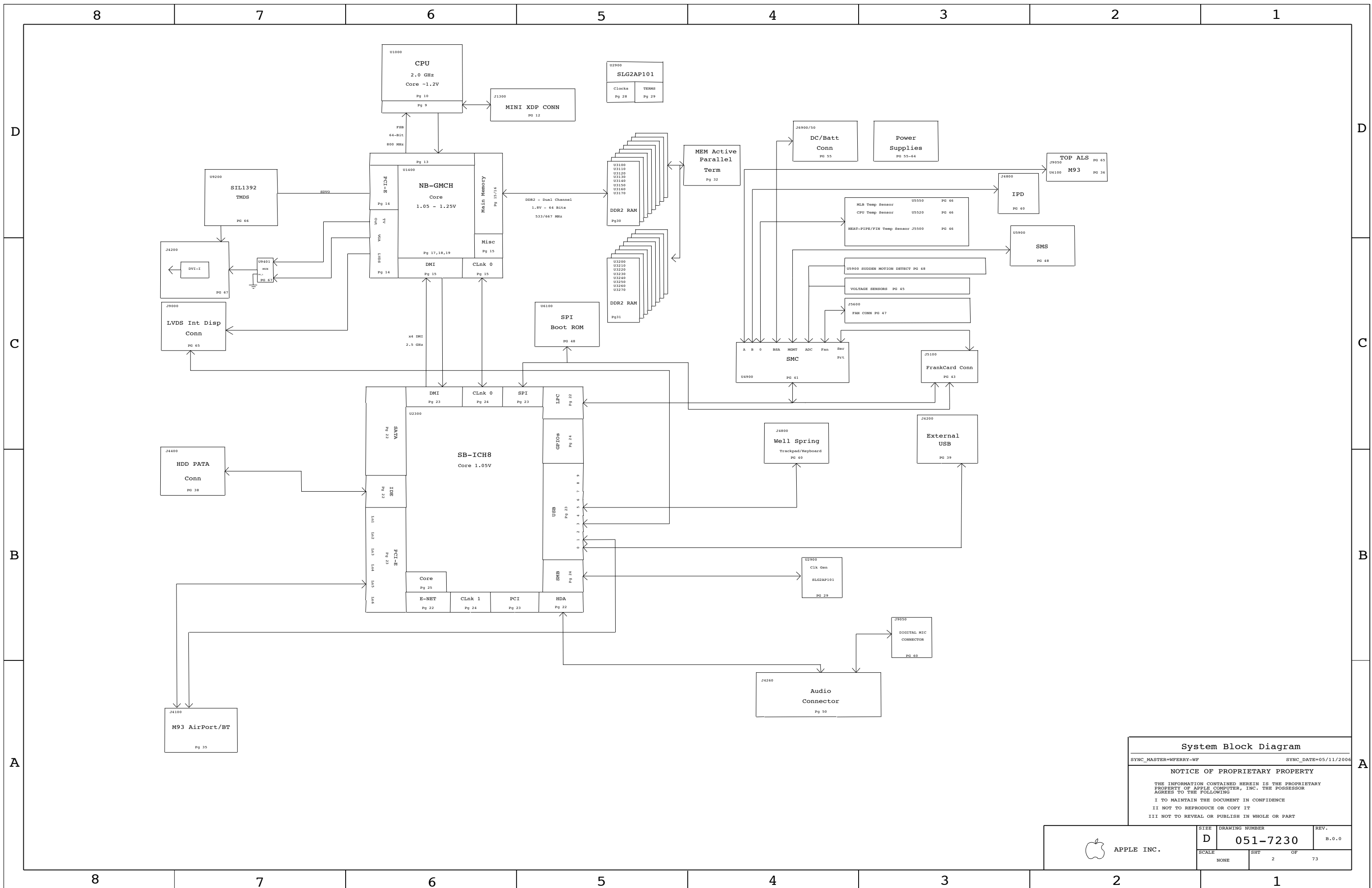
# ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7230	1	SCHEM, MLB, M82	SCH	CRITICAL	
820-2179	1	PCBF, MLB, M82	PCB	CRITICAL	

DRAWING  
TITLE=M82\_MLB  
ABBREV=DRAWING  
LAST\_MODIFIED=Nov 14 17:25:50 2007

<p style="text-align: center;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <p style="text-align: center;">           THIRD ANGLE PROJECTION       </p>	<p><b>METRIC</b></p>	 <b>APPLE INC.</b>																
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAFTER</td> <td style="width: 25%; text-align: center;">/</td> <td style="width: 25%;">DESIGN CK</td> <td style="width: 25%; text-align: center;">/</td> </tr> <tr> <td>ENG APPD</td> <td style="text-align: center;">/</td> <td>MFG APPD</td> <td style="text-align: center;">/</td> </tr> <tr> <td>QA APPD</td> <td style="text-align: center;">/</td> <td>DESIGNER</td> <td style="text-align: center;">/</td> </tr> <tr> <td>RELEASE</td> <td style="text-align: center;">/</td> <td>SCALE</td> <td style="text-align: center;">NONE</td> </tr> </table>		DRAFTER	/	DESIGN CK	/	ENG APPD	/	MFG APPD	/	QA APPD	/	DESIGNER	/	RELEASE	/	SCALE	NONE	<p style="text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: 8px;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: 8px;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p>
DRAFTER	/	DESIGN CK	/															
ENG APPD	/	MFG APPD	/															
QA APPD	/	DESIGNER	/															
RELEASE	/	SCALE	NONE															
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">MATERIAL/FINISH NOTED AS APPLICABLE</td> <td style="width: 10%;">SIZE <b>D</b></td> <td style="width: 30%;">DRAWING NUMBER <b>051-7230</b></td> </tr> </table>		MATERIAL/FINISH NOTED AS APPLICABLE	SIZE <b>D</b>	DRAWING NUMBER <b>051-7230</b>	<p style="text-align: center; font-size: 14px;"><b>SCHEM, MLB, M82</b></p> <p style="text-align: right;">REV. <b>B.0.0</b></p> <p style="text-align: right; font-size: 8px;">SHT 1 OF 73</p>													
MATERIAL/FINISH NOTED AS APPLICABLE	SIZE <b>D</b>	DRAWING NUMBER <b>051-7230</b>																



**System Block Diagram**

SYNC\_MASTER=WFERRY-WF      SYNC\_DATE=05/11/2006

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

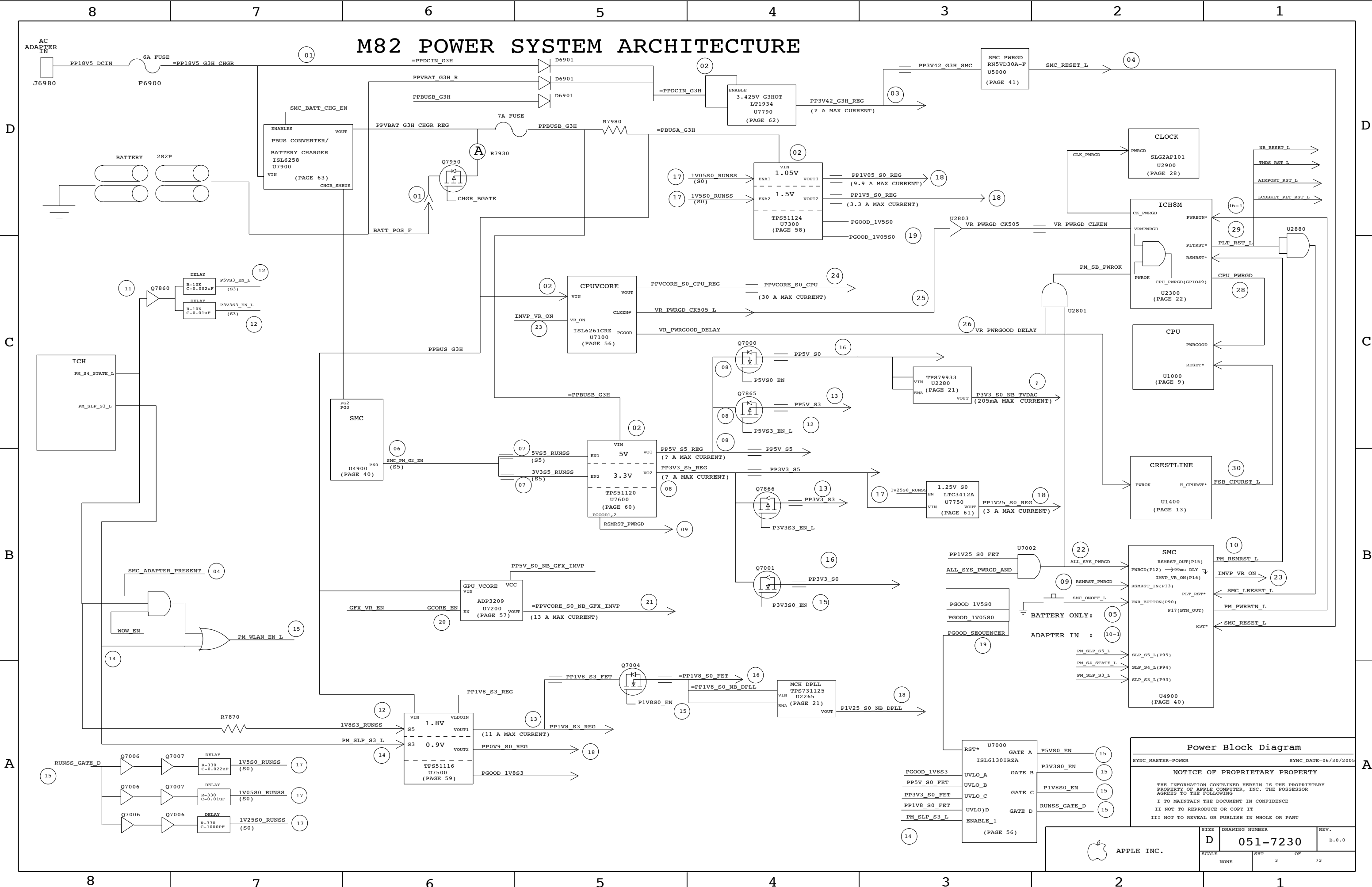
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7230</b>	REV. B.0.0
	SCALE NONE	SHEET 2	OF 73

# M82 POWER SYSTEM ARCHITECTURE



**Power Block Diagram**  
 SYNC\_MASTER=POWER SYNC\_DATE=06/30/2005

**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	3	73



PGOOD_1V8S3	UVLO_A	GATE A	P5VS0_EN	15
PP5V_S0_FET	UVLO_B	GATE B	P3V3S0_EN	15
PP3V3_S0_FET	UVLO_C	GATE C	P1V8S0_EN	15
PP1V8_S0_FET	UVLO_D	GATE D	RUNSS_GATE_D	15
PM_SLP_S3_L	ENABLE_1			

RUNSS_GATE_D	Q7006	Q7007	DELAY	1V5S0_RUNSS	17
			R-330 C-0.022uF (S0)		
	Q7006	Q7007	DELAY	1V05S0_RUNSS	17
			R-330 C-0.01uF (S0)		
	Q7006	Q7006	DELAY	1V25S0_RUNSS	17
			R-330 C-1000PF (S0)		

8

7

6

5

4

3

2

1

BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7886	PCBA,MLB,1.6GHZ,MI 2GB,SS CAP,M82	EEE_XSC,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9024	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M82	EEE_YMS,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9133	PCBA,MLB,1.8GHZ,MI 2GB,SS CAP,M82	EEE_Z80,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9134	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M82	EEE_Z81,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9204	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M82	EEE_ZU5,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9205	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M82	EEE_ZU6,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9206	PCBA,MLB,1.6GHZ,MI 2GB,MU CAP,M82	EEE_ZU7,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9207	PCBA,MLB,1.6GHZ,MI 2GB,TY CAP,M82	EEE_ZU8,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9208	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M82	EEE_ZU9,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9209	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M82	EEE_ZUA,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_TY_CAP
630-9210	PCBA,MLB,1.8GHZ,MI 2GB,MU CAP,M82	EEE_ZUB,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9211	PCBA,MLB,1.8GHZ,MI 2GB,TY CAP,M82	EEE_ZUC,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_TY_CAP

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:XSC]	CRITICAL	EEE_XSC
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:YMS]	CRITICAL	EEE_YMS
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:Z80]	CRITICAL	EEE_Z80
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:Z81]	CRITICAL	EEE_Z81
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZU5]	CRITICAL	EEE_ZU5
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZU6]	CRITICAL	EEE_ZU6
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZU7]	CRITICAL	EEE_ZU7
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZU8]	CRITICAL	EEE_ZU8
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZU9]	CRITICAL	EEE_ZU9
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZUA]	CRITICAL	EEE_ZUA
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZUB]	CRITICAL	EEE_ZUB
826-4393	1	LBL,F/N LABEL,PCB,28MM X 6 MM	[EEE:ZUC]	CRITICAL	EEE_ZUC

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M82_COMMON	ALTERNATE,COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3
M82_COMMON1	ISL6258,BOOTROM_DEVEL,SMC_PRGRM
M82_COMMON2	SMS_MOT_DIS,LPCLPLUS,XDP,DRAM_2GB
M82_COMMON3	
M82_MICRON	DRAM_MICRON,DRAM_SPD_1
M82_HYNIX	DRAM_HYNIX,DRAM_SPD_2
M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2
M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF
M82_MU_CAP	MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF
M82_TY_CAP	TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ
337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ
338S0420	1	IC,965GM,CRESTLINE,USFF BGA	U1400	CRITICAL	
338S0421	1	IC,ICH8M,USFF BGA	U2300	CRITICAL	
359S0130	1	LOW POWER CLOCK SYNTHESIZER,8LQ2AP101,6SPIN	U2900	CRITICAL	
335S0510	1	IC,16MBIT 8-PIN SERIAL FLASH,WQFN	U6100	CRITICAL	BOOTROM_BLANK_2MB
335S0509	1	IC,32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL
341S2112	1	IC,EFI,BOOTROM FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL
337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK
341S2173	1	IC,PRGM,SST SST89V54RD,UCNTRLR,M82	U9300	CRITICAL	SST8051_PRGRM
338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON
333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258
197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ
197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ
197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ
337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ
337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ
338S0514	1	IC,965GM,CRESTLINE,PRQ,USFF BGA	U1400	CRITICAL	NB_PRQ
338S0515	1	IC,ICH8M,PRQ,USFF BGA	U2300	CRITICAL	SB_PRQ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0044	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	

CONFIGURATION OPTIONS

SYNC\_MASTER=(N/A) SYNC\_DATE=(N/A)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

APPLE INC.

SIZE DRAWING NUMBER REV.

D 051-7230 B.0.0

SCALE NONE SHT 4 OF 73

8

7

6

5

4

3

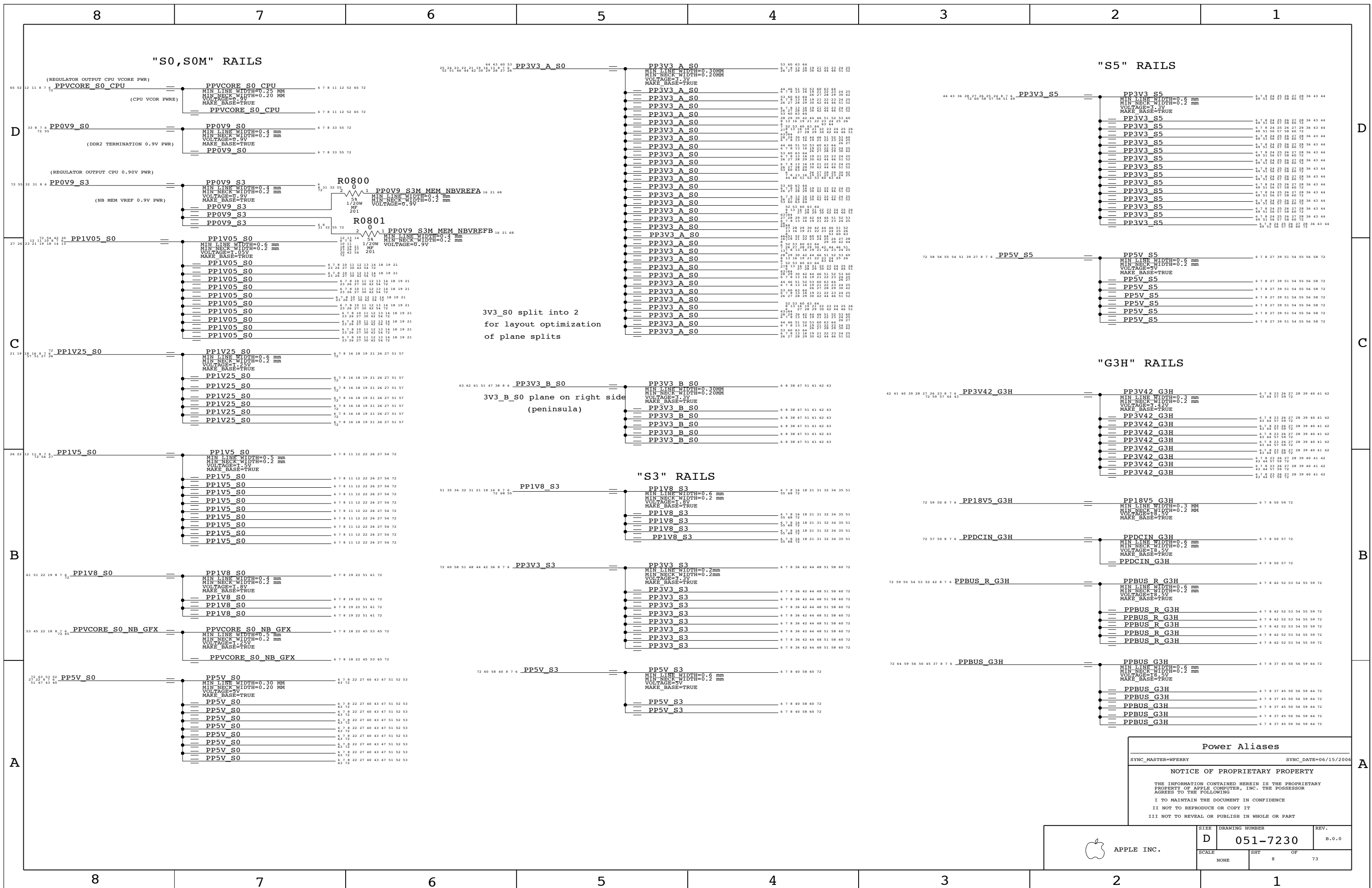
2

1









"S0,S0M" RAILS

"S5" RAILS

"G3H" RAILS

"S3" RAILS

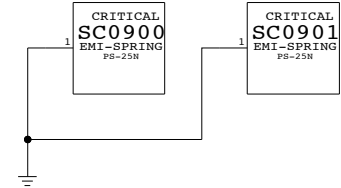
Power Aliases		
SYNC_MASTER=WFEERY	SYNC_DATE=06/15/2006	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

 APPLE INC.	SIZE D	DRAWING NUMBER 051-7230	REV. B.0.0
	SCALE NONE	SHEET 8	OF 73

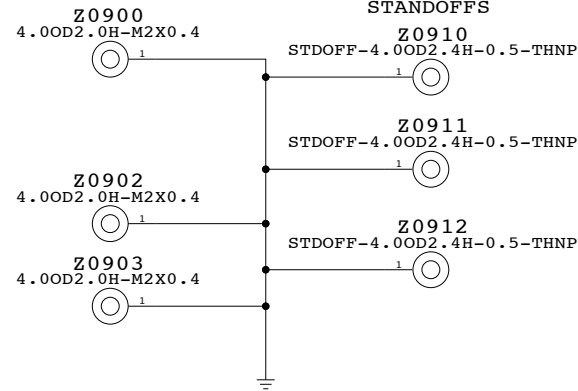


EMI SPRING CLIPS

PLACE CLIPS PER MCO ON TOPSIDE NEAR BATTERY CONNECTOR J6900



BOSSES TO CONNECT TO HEATSINK



SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

Table listing SMC aliases such as NC\_SMC\_PA0, NC\_SMC\_PA1, NC\_SMC\_PA2, etc., with their corresponding NC\_SMC aliases and TRUE/FALSE status.

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

Table listing LVDS aliases such as NC\_LVDS\_B\_CLK\_N, NC\_LVDS\_B\_CLK\_P, NC\_LVDS\_B\_DATA\_N0, etc., with their corresponding NC\_LVDS aliases and TRUE/FALSE status.

PCI\_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

Table listing PCI Express Graphics aliases such as NC\_PEG\_D2R\_N0, NC\_PEG\_D2R\_N1, NC\_PEG\_D2R\_N2, etc., with their corresponding NC\_PEG aliases and TRUE/FALSE status.

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

Table listing SATA aliases such as NC\_SATA\_A\_D2R\_N, NC\_SATA\_A\_D2R\_P, NC\_SATA\_A\_R2D\_C\_N, etc., with their corresponding NC\_SATA aliases and TRUE/FALSE status.

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

Table listing Clock aliases such as NC\_CK505\_SRC1\_N, NC\_CK505\_SRC1\_P, NC\_CK505\_SRC1\_L, etc., with their corresponding NC\_CK505 aliases and TRUE/FALSE status.

SB ALIASES

NO-CONNECT UNUSED INTERFACE PORTS

Table listing SB aliases such as VR\_PWRGD\_CK505, PM\_SB\_PWROK, PCI\_AD<0..31>, etc., with their corresponding aliases and TRUE/FALSE status.

NB ALIASES

Table listing NB aliases such as GFX\_VR\_EN, VR\_PWRGOOD\_DELAY, NB\_CLK96M\_DOT\_P, etc., with their corresponding aliases and TRUE/FALSE status.

AUDIO ALIASES

Table listing Audio aliases such as HDA\_BIT\_CLK, HDA\_SYNC, HDA\_RST\_L, etc., with their corresponding aliases and TRUE/FALSE status.

USB ALIASES

USB PORT [0] = External USB2.0 Port A

Table listing USB aliases for Port 0, Port 1, Port 2, and Port 3, such as USB2\_EXTA\_P, USB2\_EXTA\_N, USB2\_MIXED\_EXTA\_P, etc.

USB PORT [3] = CAMERA

Table listing USB aliases for Port 3, such as USB2\_CAMERA\_P, USB2\_CAMERA\_N, etc.

USB PORT [4] = IR CONTROLLER

Table listing USB aliases for Port 4, such as USB\_IR\_P, USB\_IR\_N, etc.

USB PORT [5] = Trackpad(Wellspring)

Table listing USB aliases for Port 5, such as USB2\_WSPRING\_P, USB2\_WSPRING\_N, etc.

USB PORT [6] = BLUETOOTH

Table listing USB aliases for Port 6, such as NC\_USB\_BT\_P, NC\_USB\_BT\_N, etc.

USB PORT [7] = Unused

Table listing USB aliases for Port 7, such as NC\_USB2\_EXTB\_P, NC\_USB2\_EXTB\_N, etc.

USB PORT [8] = Unused

Table listing USB aliases for Port 8, such as TP\_USB\_EXCARD\_P, TP\_USB\_EXCARD\_N, etc.

USB PORT [9] = Unused

Table listing USB aliases for Port 9, such as TP\_USB\_EXTC\_P, TP\_USB\_EXTC\_N, etc.

SIGNAL ALIAS /RESET

SYNC\_MASTER=(MASTER) SYNC\_DATA=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

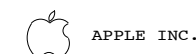
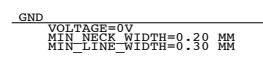
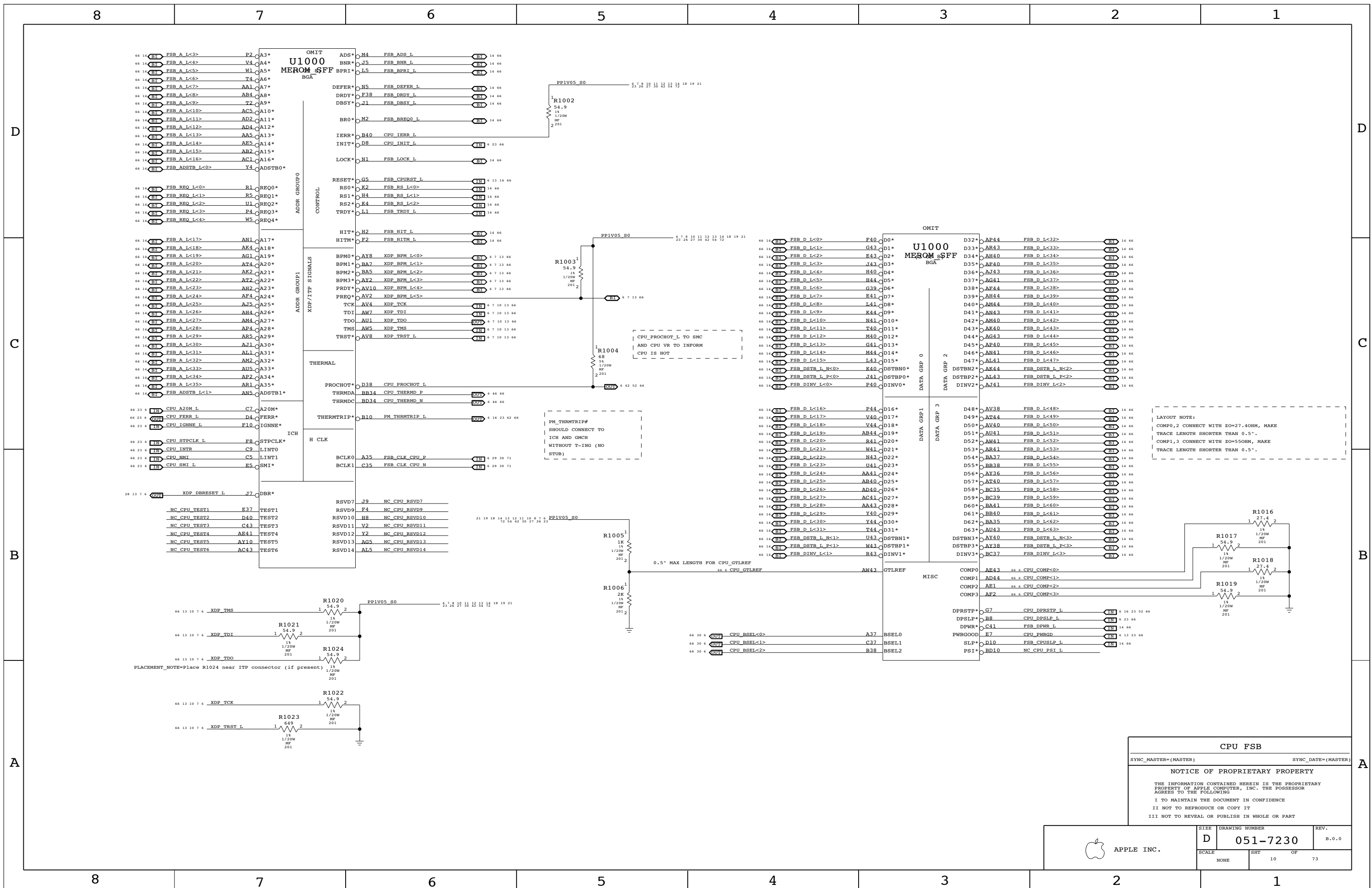


Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, OF, and a grid with values D, 051-7230, B.0.0, NONE, 9, 73.

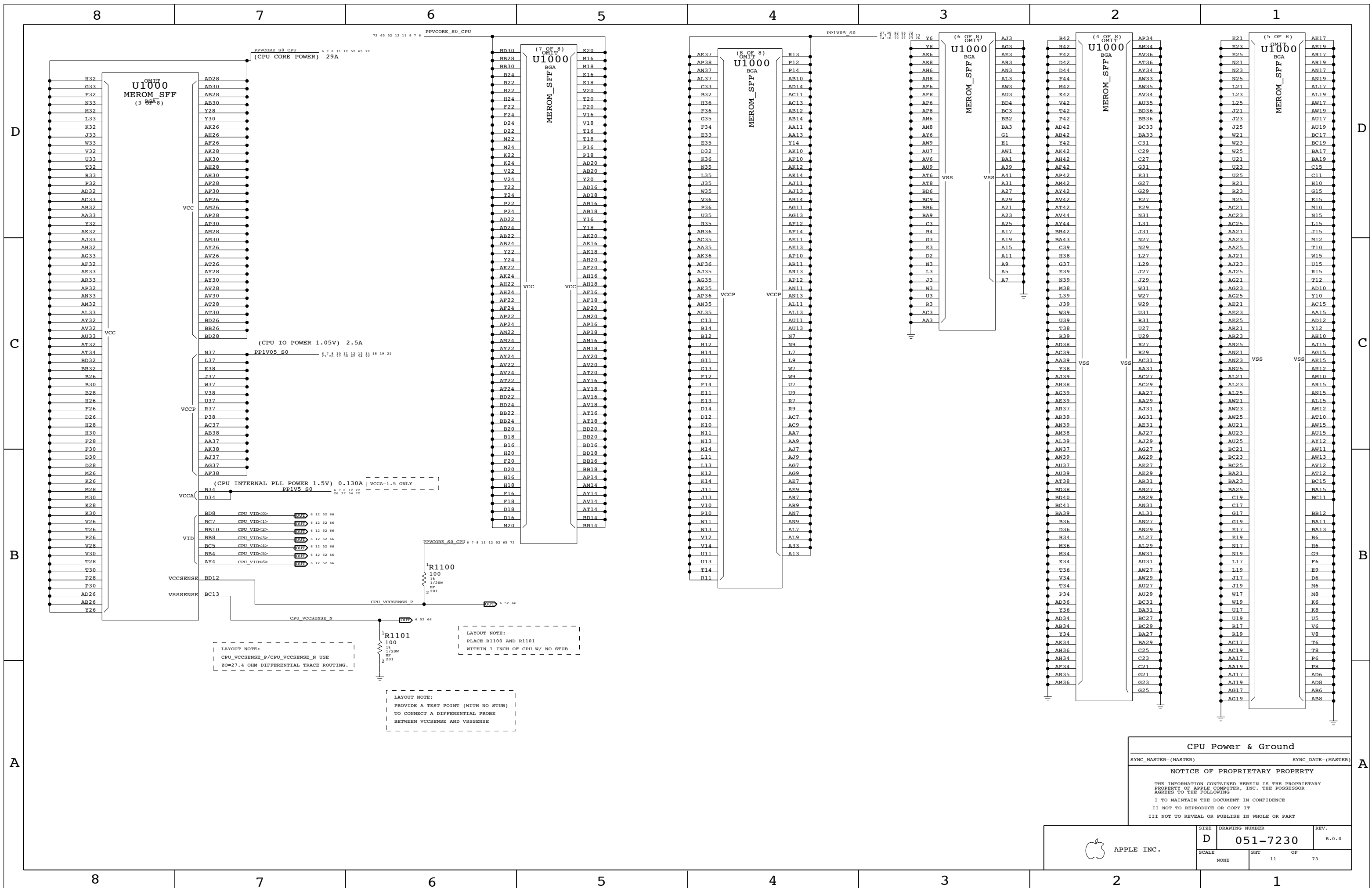




LAYOUT NOTE:  
 COMP0,2 CONNECT WITH Z0=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".  
 COMP1,3 CONNECT WITH Z0=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

**CPU FSB**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		10	73



LAYOUT NOTE:  
CPU\_VCCSENSE\_P/CPU\_VCCSENSE\_N USE  
20=27.4 OHM DIFFERENTIAL TRACE ROUTING.

LAYOUT NOTE:  
PLACE R1100 AND R1101  
WITHIN 1 INCH OF CPU W/ NO STUB

LAYOUT NOTE:  
PROVIDE A TEST POINT (WITH NO STUB)  
TO CONNECT A DIFFERENTIAL PROBE  
BETWEEN VCCSENSE AND VSSSENSE

**CPU Power & Ground**

SYNC\_MASTER={MASTER} SYNC\_DATE={MASTER}

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		11	73

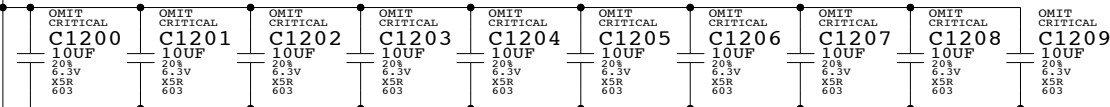
# CPU VCORE HF AND BULK DECOUPLING

3x 330uF, 32x 10uF 0603, 28x 1uF 0402  
Intel recommends 32+28 but is evaluating 24+24

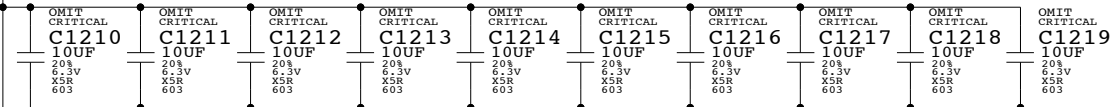
72 45 52 11 8 7 6 PPVCORE\_S0\_CPU

10UF 0603 = APN:138S0568 = MURATA, TAIYO, TDK, SAMSUNG

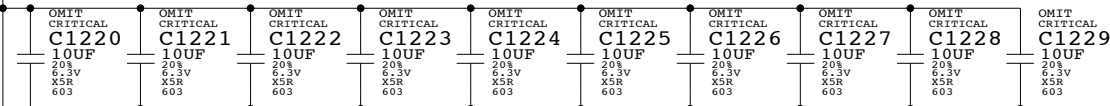
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



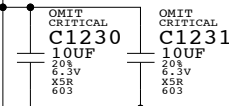
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



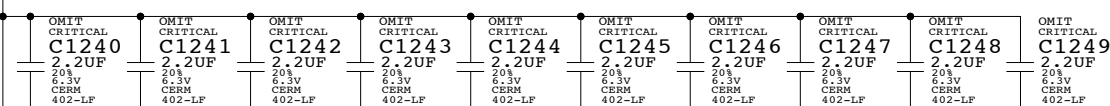
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



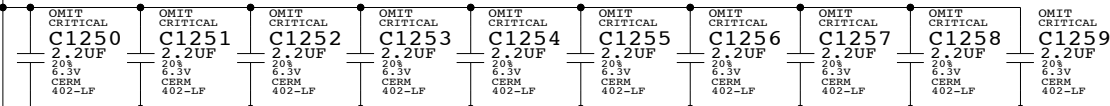
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



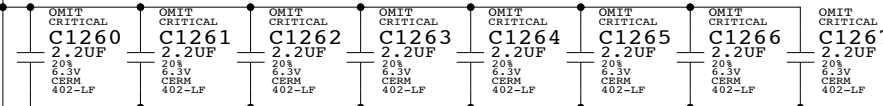
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



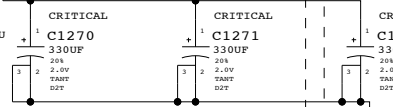
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:  
PLACE ON SAME SIDE AS CPU



LAYOUT NOTE:  
PLACE ON SAME SIDE AS CPU

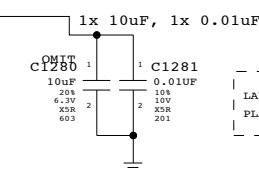
Intel recommends 3x220UF @ 9mOHM

## CPU VCORE VID CONNECTIONS

66 52 11 6 CPU\_VID<0..6> MAKE\_BASE=TRUE IMVP6\_VID<0..6> 66

## VCCA (CPU AVdd) DECOUPLING

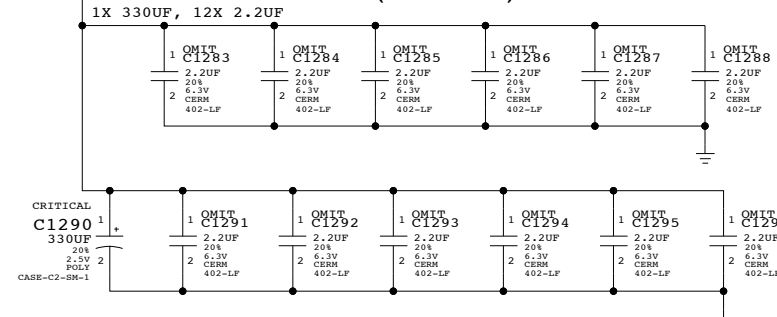
72 54 27 26 22 11 8 7 6 PPV5\_S0



LAYOUT NOTE:  
PLACE C1281 NEAR PIN B34 OF U1000

## VCCP (CPU I/O) DECOUPLING

23 21 19 18 17 16 15 14 13 12 11 10 9 8 7 6 PPV05\_S0



LAYOUT NOTE:  
PLACE C1290 CLOSE TO CPU  
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS  
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

## CPU Decoupling & VID

SYNC\_MASTER=MSASHAR SYNC\_DATE=04/26/2004

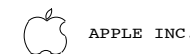
### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE DRAWING NUMBER REV.

D 051-7230 B.0.0

SCALE SHEET OF 73

8

7

6

5

4

3

2

1

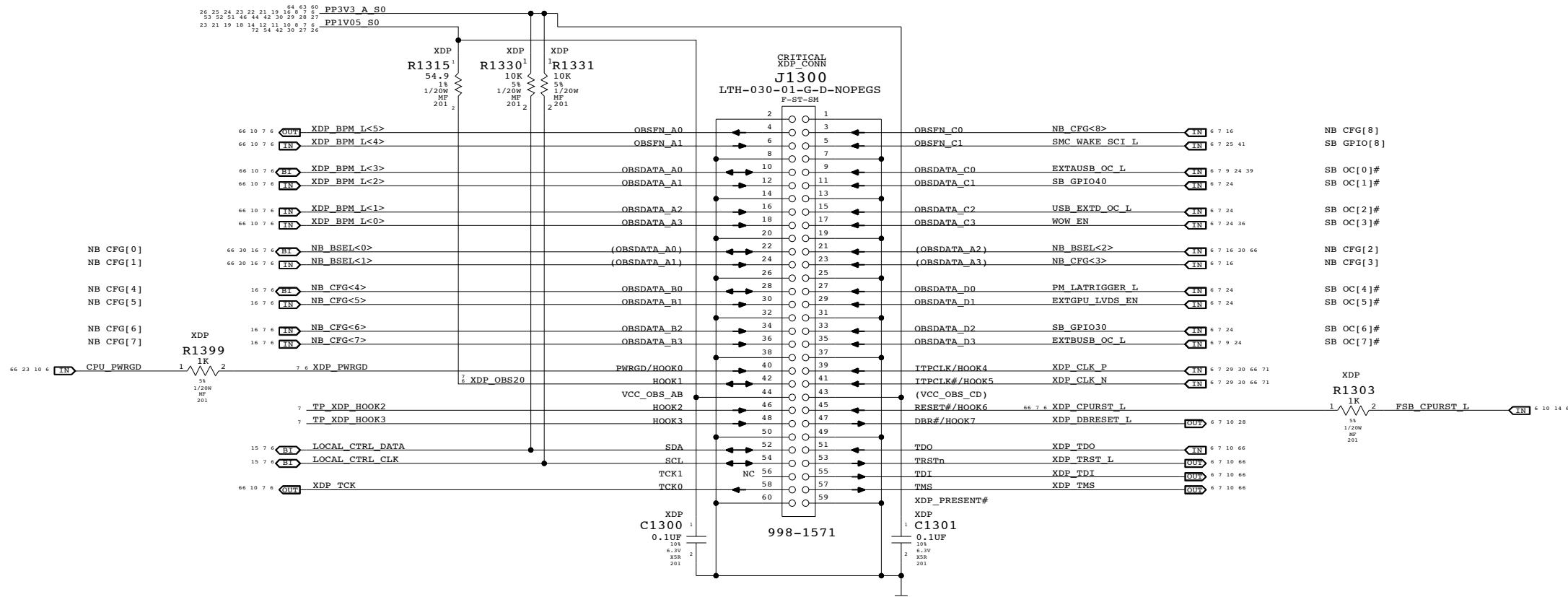
D

D

# Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



← Direction of XDP module to edge of board  
Please avoid any obstructions

C

C

B

B

A

A

**eXtended Debug Port (XDP)**  
 SYNC\_MASTER=M75 SYNC\_DATE=01/24/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT		OF
NONE	13		73

8

7

6

5

4

3

2

1



**NB CPU Interface**

SYNC\_MASTER={MASTER} SYNC\_DATE={MASTER}

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT		OF
NONE	14		73

LVDS Disable

Can leave all signals NC if LVDS is not implemented. Tie VCC\_TX\_LVDS and VCCA\_LVDS to GND.

If SDVO is used, VCCD\_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD\_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx\_DAC and TVx\_RTN to GND. Must power all TVDAC rails. VCCA\_TVx\_DAC and VCCA\_DAC\_BG can share filtering with VCCA\_CRT\_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA\_CRT.

CRT & TV-Out Disable

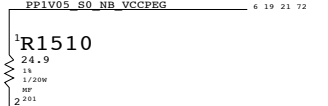
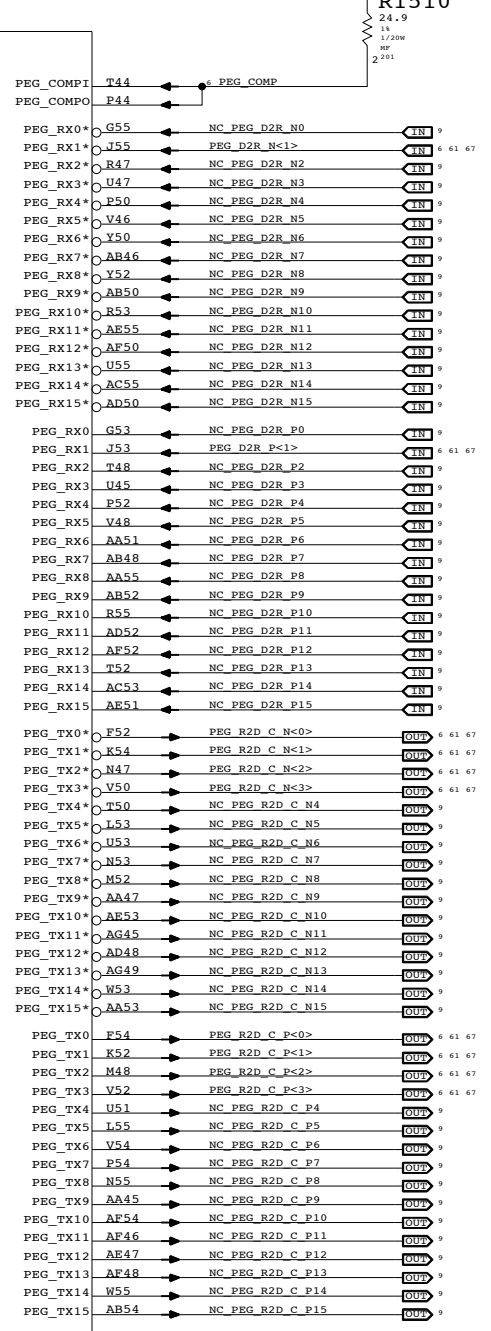
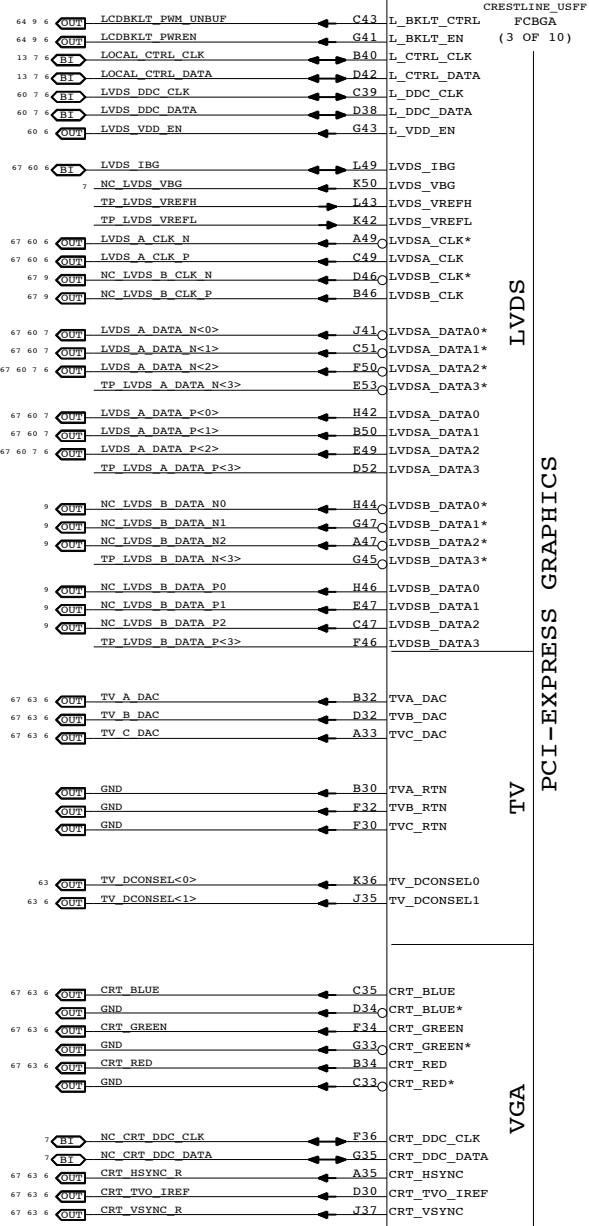
Tie TVx\_DAC, TVx\_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT\_TVO\_IREF to GND. Can tie the following rails to GND: VCCA\_CRT\_DAC, VCCA\_DAC\_BG, VCCA\_TVx\_DAC, VCCD\_CRT, VCCD\_QDAC and VCC\_SYNC.

NOTE: Must keep VDDC\_TVDAC powered and filtered at all times!

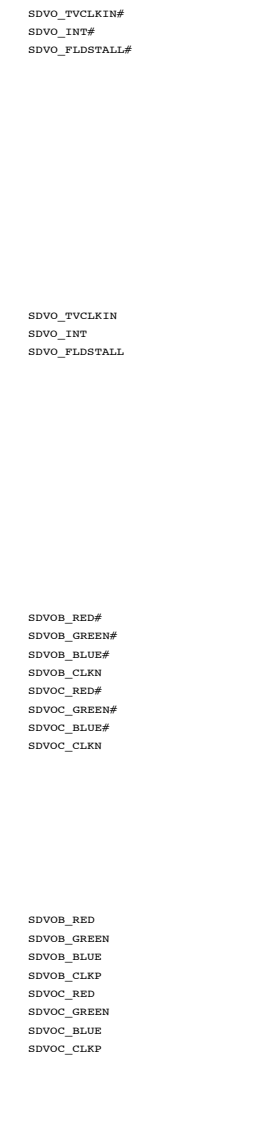
Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT\_DDC\_\*, L\_CTRL\_\*, L\_DDC\_\*, SDVO\_CTRL\_\* and TV\_DCONSELx to GND.

Tie DPLL\_REF\_CLK and DPLL\_REF\_SSCLK to GND. Tie DPLL\_REF\_CLK\* and DPLL\_REF\_SSCLK\* to VCC (VCore). Tie VCCA\_DPLLA and VCCA\_DPLLB to VCC (VCore). Tie VCC\_AXG and VCC\_AXG\_NCTF to GND. Leave GFX\_VID<3..0> and GFX\_VR\_EN as NC.

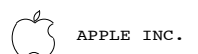


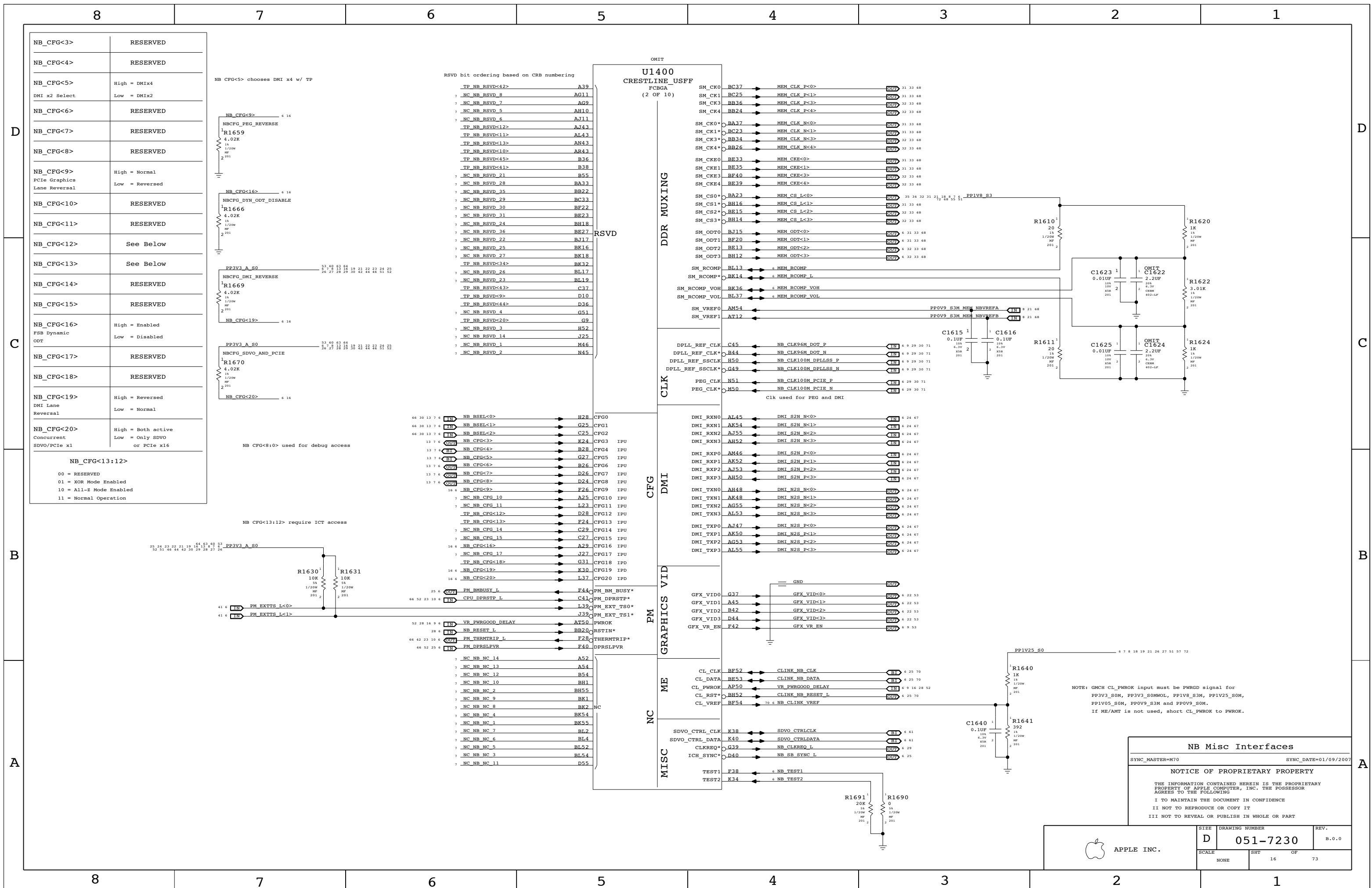
SDVO Alternate Function



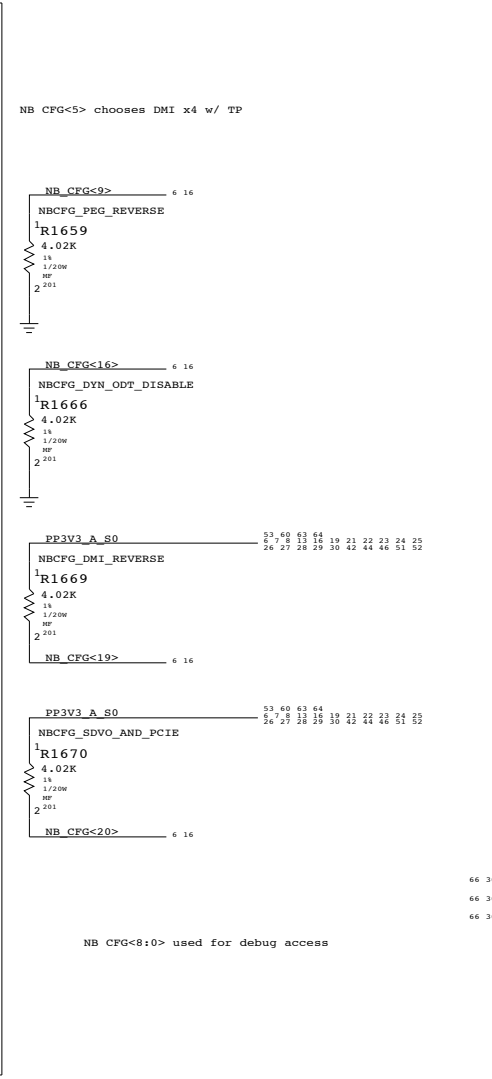
NB PEG / Video Interfaces
SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

Table with columns: SIZE (D), DRAWING NUMBER (051-7230), REV. (B.0.0), SCALE (NONE), SHEET (15 OF 73)





NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIx4 DMI x2 Select Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
NB_CFG<20>	High = Both active Concurrent SDVO/PCIe x1 Low = Only SDVO or PCIe x16

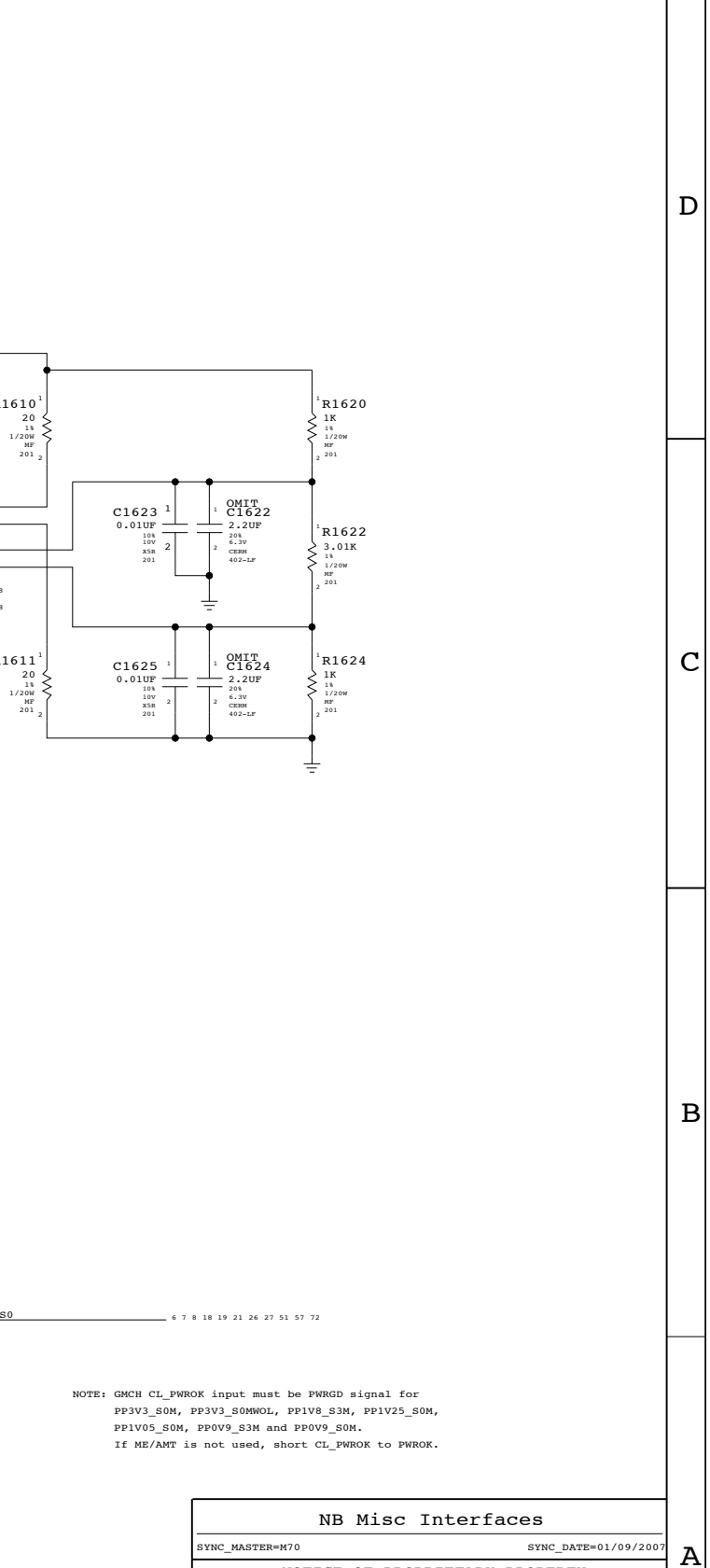


RSVD bit ordering based on CRB numbering

TP NB_RSVD<42>	A39
NC NB_RSVD_8	AG11
NC NB_RSVD_7	AG9
NC NB_RSVD_5	AH10
NC NB_RSVD_6	AJ11
TP NB_RSVD<12>	AL43
TP NB_RSVD<11>	AL43
TP NB_RSVD<13>	AM43
TP NB_RSVD<10>	AR43
TP NB_RSVD<45>	B36
TP NB_RSVD<41>	B38
NC NB_RSVD_21	B55
NC NB_RSVD_28	BA33
NC NB_RSVD_35	BB22
NC NB_RSVD_29	BC33
NC NB_RSVD_30	BE22
NC NB_RSVD_31	BE23
NC NB_RSVD_24	BH18
NC NB_RSVD_36	BE27
NC NB_RSVD_22	BJ17
NC NB_RSVD_25	BK16
NC NB_RSVD_27	BK18
TP NB_RSVD<34>	BK32
NC NB_RSVD_26	BL17
NC NB_RSVD_23	BL19
TP NB_RSVD<43>	C37
TP NB_RSVD<9>	D10
TP NB_RSVD<44>	D36
NC NB_RSVD_4	G51
TP NB_RSVD<20>	G9
NC NB_RSVD_3	H52
NC NB_RSVD_14	J25
NC NB_RSVD_1	M46
NC NB_RSVD_2	N45

U1400 CRESTLINE USFF PCBGA (2 OF 10)

SM_CK0	BC37	MEM_CLK_P<0>	31 33 68
SM_CK1	BC25	MEM_CLK_P<1>	31 33 68
SM_CK3	BB36	MEM_CLK_P<3>	32 33 68
SM_CK4	BB24	MEM_CLK_P<4>	32 33 68
SM_CK0*	BA37	MEM_CLK_N<0>	31 33 68
SM_CK1*	BC23	MEM_CLK_N<1>	31 33 68
SM_CK3*	BB34	MEM_CLK_N<3>	32 33 68
SM_CK4*	BB26	MEM_CLK_N<4>	32 33 68
SM_CKE0	BE33	MEM_CKE<0>	31 33 68
SM_CKE1	BE35	MEM_CKE<1>	31 33 68
SM_CKE3	BF40	MEM_CKE<3>	32 33 68
SM_CKE4	BE39	MEM_CKE<4>	32 33 68
SM_CS0*	BA23	MEM_CS_L<0>	35 34 32 31 23 18 # 2 6 1 PP1V8_S3
SM_CS1*	BH16	MEM_CS_L<1>	31 33 68
SM_CS2*	BE15	MEM_CS_L<2>	31 33 68
SM_CS3*	BH14	MEM_CS_L<3>	32 33 68
SM_ODT0	BJ15	MEM_ODT<0>	6 31 33 68
SM_ODT1	BE20	MEM_ODT<1>	6 31 33 68
SM_ODT2	BE13	MEM_ODT<2>	6 32 33 68
SM_ODT3	BH12	MEM_ODT<3>	6 32 33 68
SM_RCOMP	BL13	MEM_RCOMP	
SM_RCOMP*	BK14	MEM_RCOMP_L	
SM_RCOMP_VOH	BK36	MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL37	MEM_RCOMP_VOL	
SM_VREF0	AM54	MEM_VREF0	
SM_VREF1	AT12	MEM_VREF1	
DPLL_REF_CLK	C45	NB_CLK96M_DOT_P	6 9 29 30 71
DPLL_REF_CLK*	B44	NB_CLK96M_DOT_N	6 9 29 30 71
DPLL_REF_SSCLK	H50	NB_CLK100M_DPLLSS_P	6 9 29 30 71
DPLL_REF_SSCLK*	G49	NB_CLK100M_DPLLSS_N	6 9 29 30 71
PEG_CLK	N51	NB_CLK100M_PCIE_P	6 29 30 71
PEG_CLK*	M50	NB_CLK100M_PCIE_N	6 29 30 71
		Clk used for PEG and DMI	
DMI_RXN0	AL45	DMI_S2N_N<0>	6 24 67
DMI_RXN1	AK54	DMI_S2N_N<1>	6 24 67
DMI_RXN2	AJ55	DMI_S2N_N<2>	6 24 67
DMI_RXN3	AH52	DMI_S2N_N<3>	6 24 67
DMI_RXP0	AM46	DMI_S2N_P<0>	6 24 67
DMI_RXP1	AK52	DMI_S2N_P<1>	6 24 67
DMI_RXP2	AJ53	DMI_S2N_P<2>	6 24 67
DMI_RXP3	AH50	DMI_S2N_P<3>	6 24 67
DMI_TXN0	AH48	DMI_N2S_N<0>	6 24 67
DMI_TXN1	AK48	DMI_N2S_N<1>	6 24 67
DMI_TXN2	AG55	DMI_N2S_N<2>	6 24 67
DMI_TXN3	AL53	DMI_N2S_N<3>	6 24 67
DMI_TXP0	AJ47	DMI_N2S_P<0>	6 24 67
DMI_TXP1	AK50	DMI_N2S_P<1>	6 24 67
DMI_TXP2	AG53	DMI_N2S_P<2>	6 24 67
DMI_TXP3	AL55	DMI_N2S_P<3>	6 24 67
GFX_VID0	G37	GFX_VID<0>	6 22 53
GFX_VID1	A45	GFX_VID<1>	6 22 53
GFX_VID2	B42	GFX_VID<2>	6 22 53
GFX_VID3	D44	GFX_VID<3>	6 22 53
GFX_VR_EN	F42	GFX_VR_EN	6 9 53
CL_CLK	BF52	CLINK_NB_CLK	6 25 70
CL_DATA	BE53	CLINK_NB_DATA	6 25 70
CL_PWROK	AP50	VR_PWRGOOD_DELAY	6 9 14 28 52
CL_RST*	BH52	CLINK_NB_RESET_L	6 25 70
CL_VREF	BF54	70 6 NB CLINK VREF	6 25 70
SDVO_CTRL_CLK	K38	SDVO_CTRLCLK	6 61
SDVO_CTRL_DATA	K40	SDVO_CTRLDATA	6 61
CLKREQ*	G39	NB_CLKREQ_L	6 29
ICH_SYNC*	D40	NB_SB_SYNC_L	6 25
TEST1	F38	6 NB_TEST1	
TEST2	K34	6 NB_TEST2	



**NB Misc Interfaces**

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

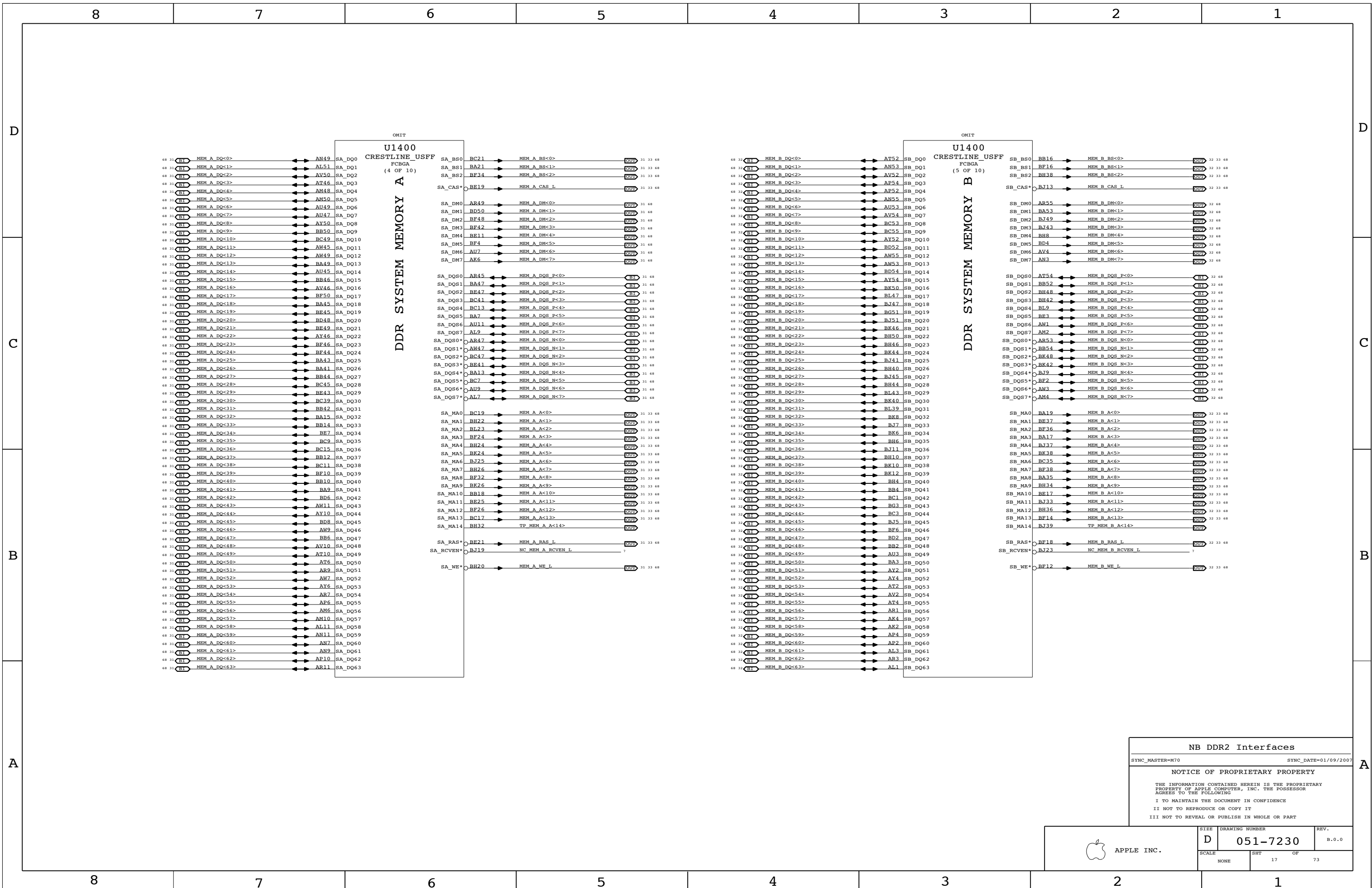
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	16	73

APPLE INC.





**NB DDR2 Interfaces**

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**

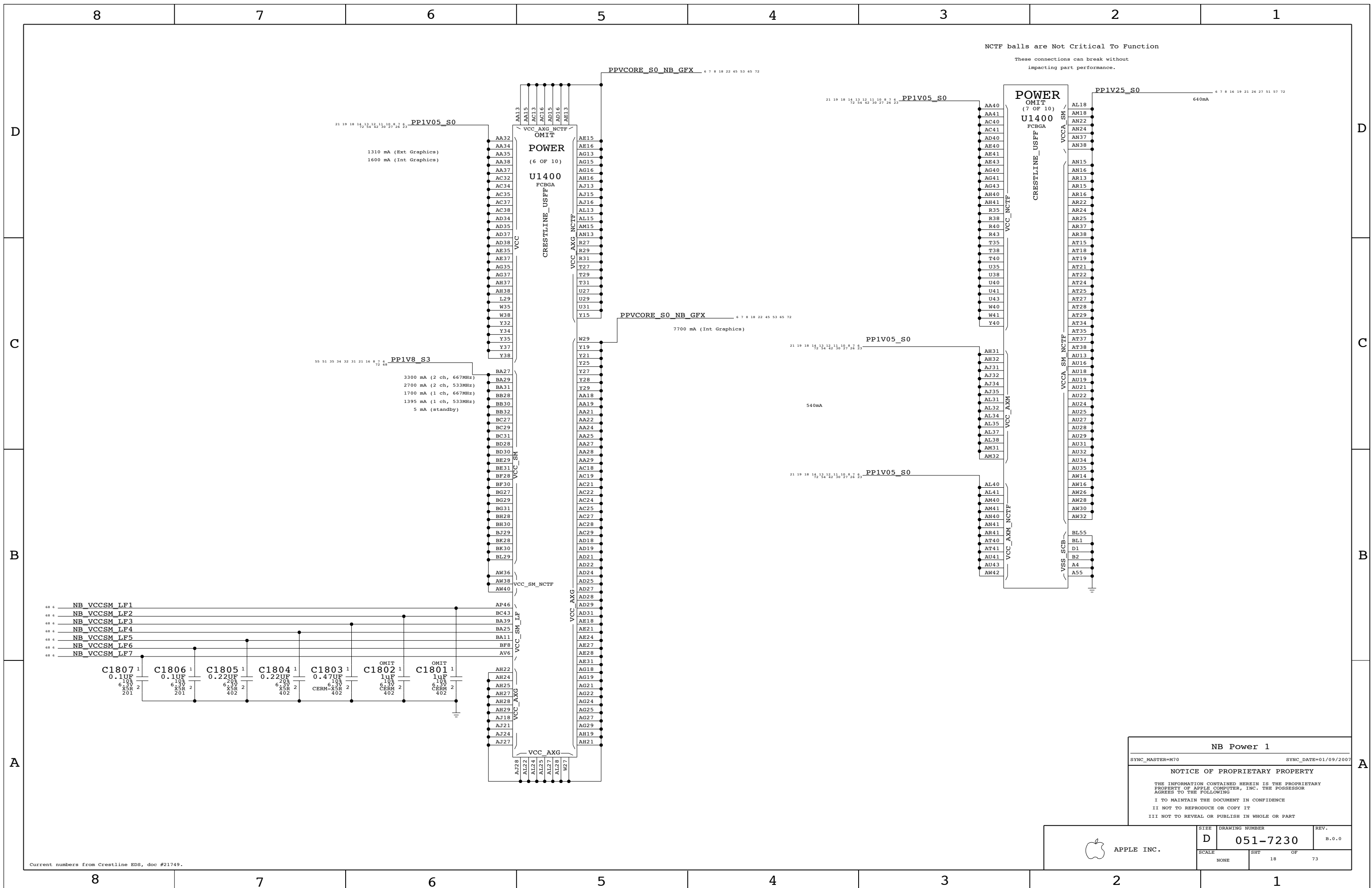
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

<b>APPLE INC.</b>	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	17	17	73



NCTF balls are Not Critical To Function  
 These connections can break without impacting part performance.

PP1V05\_S0  
 1310 mA (Ext Graphics)  
 1600 mA (Int Graphics)

PP1V8\_S3  
 3300 mA (2 ch, 667MHz)  
 2700 mA (2 ch, 533MHz)  
 1700 mA (1 ch, 667MHz)  
 1395 mA (1 ch, 533MHz)  
 5 mA (standby)

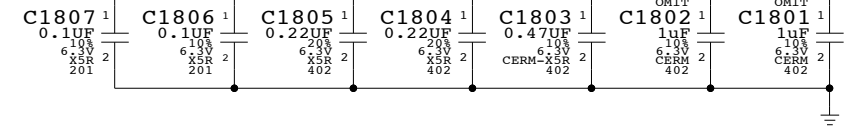
PPV CORE S0 NB GFX  
 7700 mA (Int Graphics)

PP1V05\_S0  
 540mA

PP1V25\_S0  
 640mA

POWER OMIT (7 OF 10)  
 U1400 FCBGA  
 CRESTLINE\_USFF

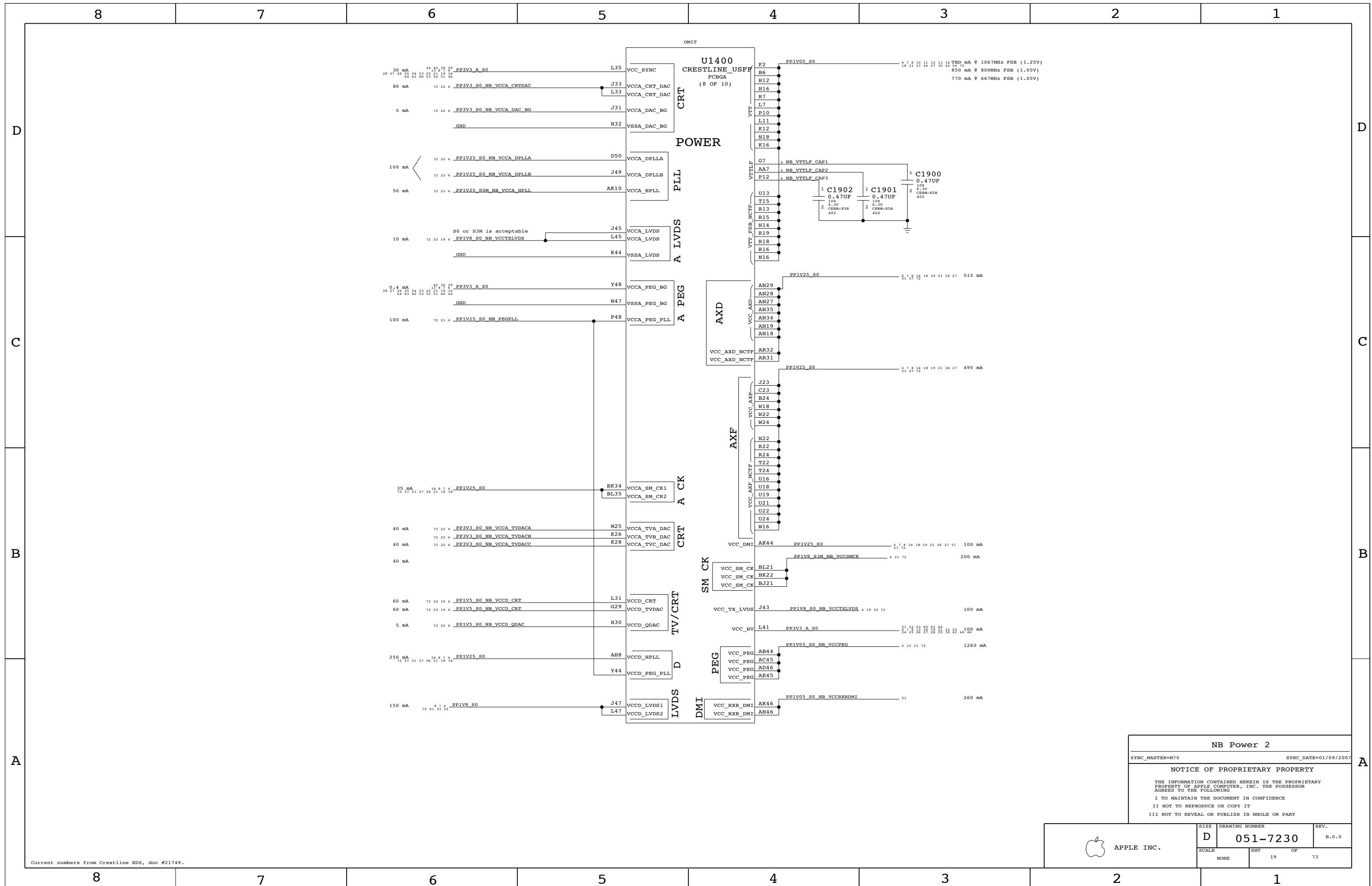
NB\_VCCSM\_LF1  
 NB\_VCCSM\_LF2  
 NB\_VCCSM\_LF3  
 NB\_VCCSM\_LF4  
 NB\_VCCSM\_LF5  
 NB\_VCCSM\_LF6  
 NB\_VCCSM\_LF7



NB Power 1  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		REV.
NONE	18 OF 73		

Current numbers from Crestline EDS, doc #21749.



**NB Power 2**

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

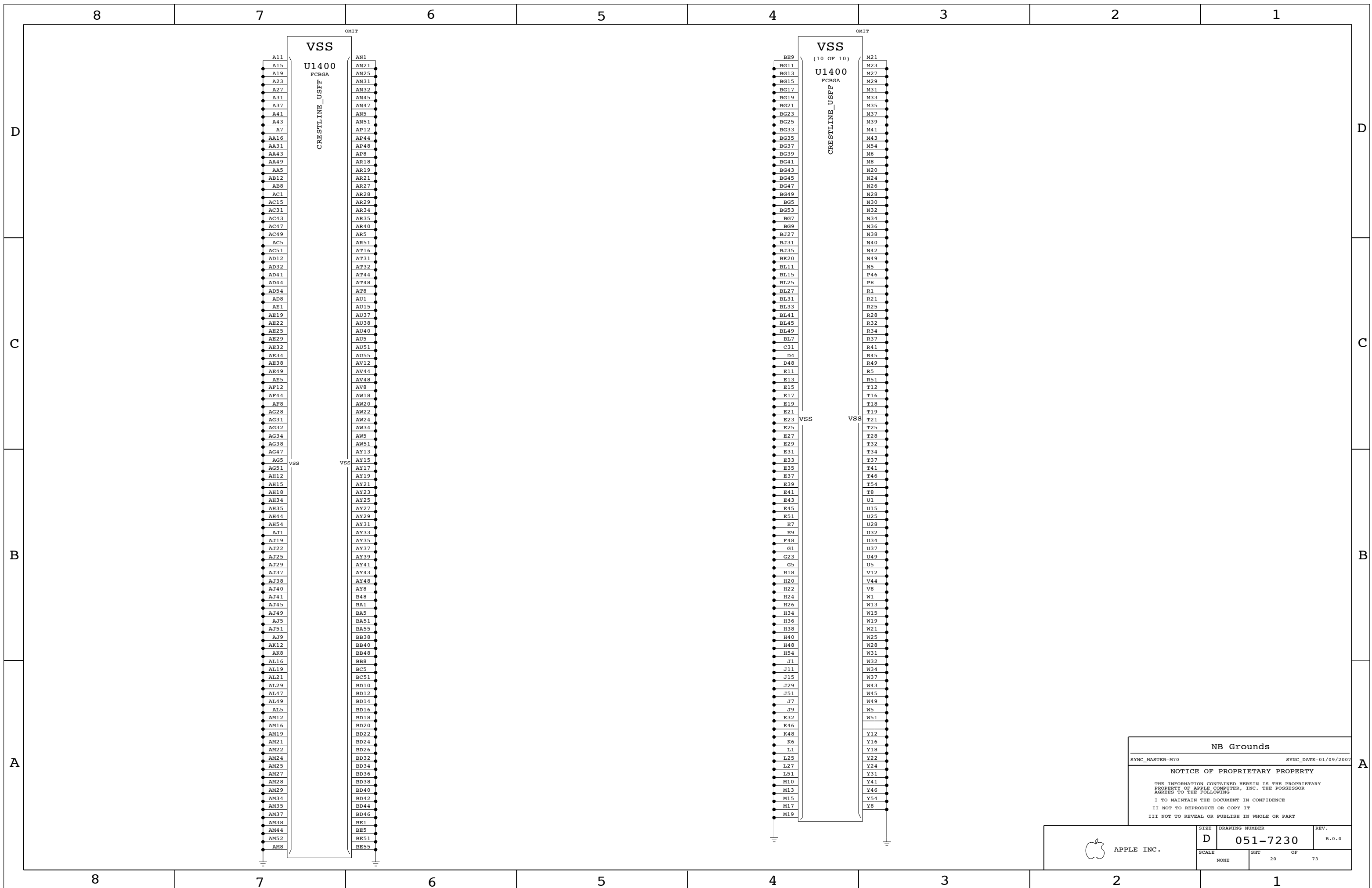
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7230</b>	REV. B.0.0
	SCALE NONE	SHEET 19	OF 73

Current numbers from Crestline EDS, doc #21749.



**NB Grounds**

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**

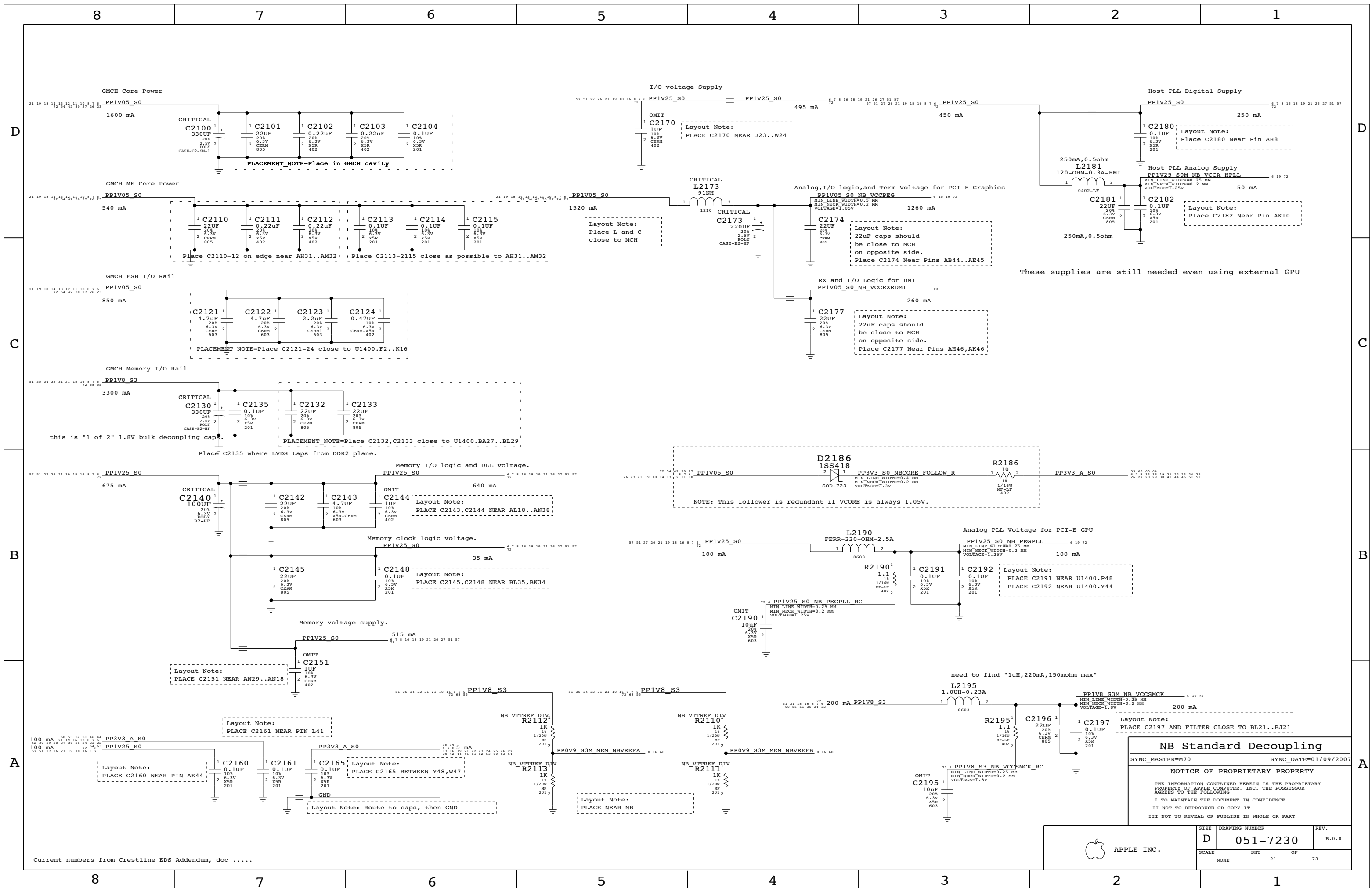
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

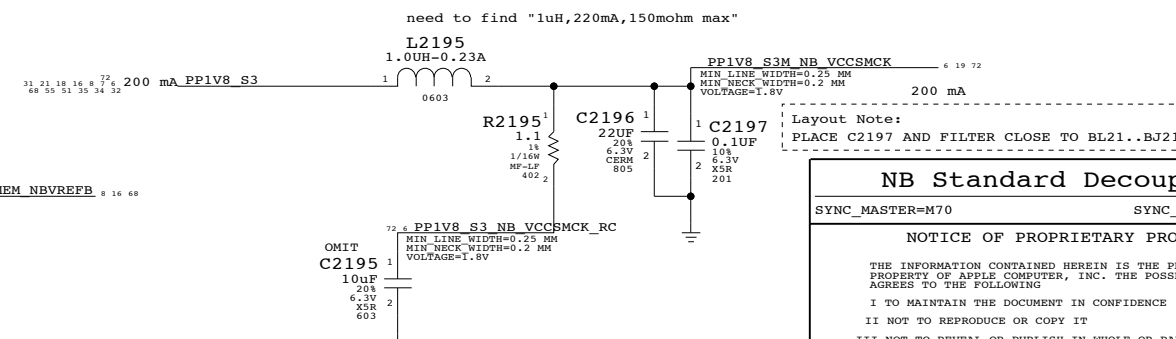
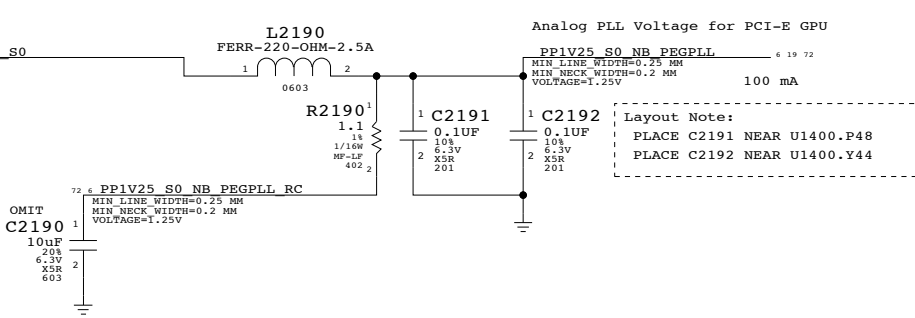
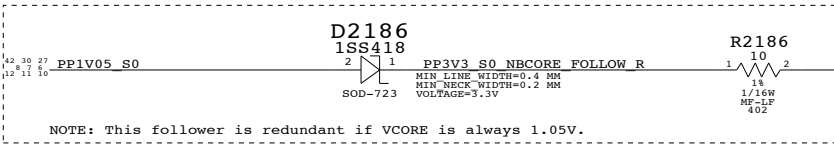
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	D	DRAWING NUMBER	051-7230	REV.	B.0.0
	SCALE	NONE	SHT	20	OF	73



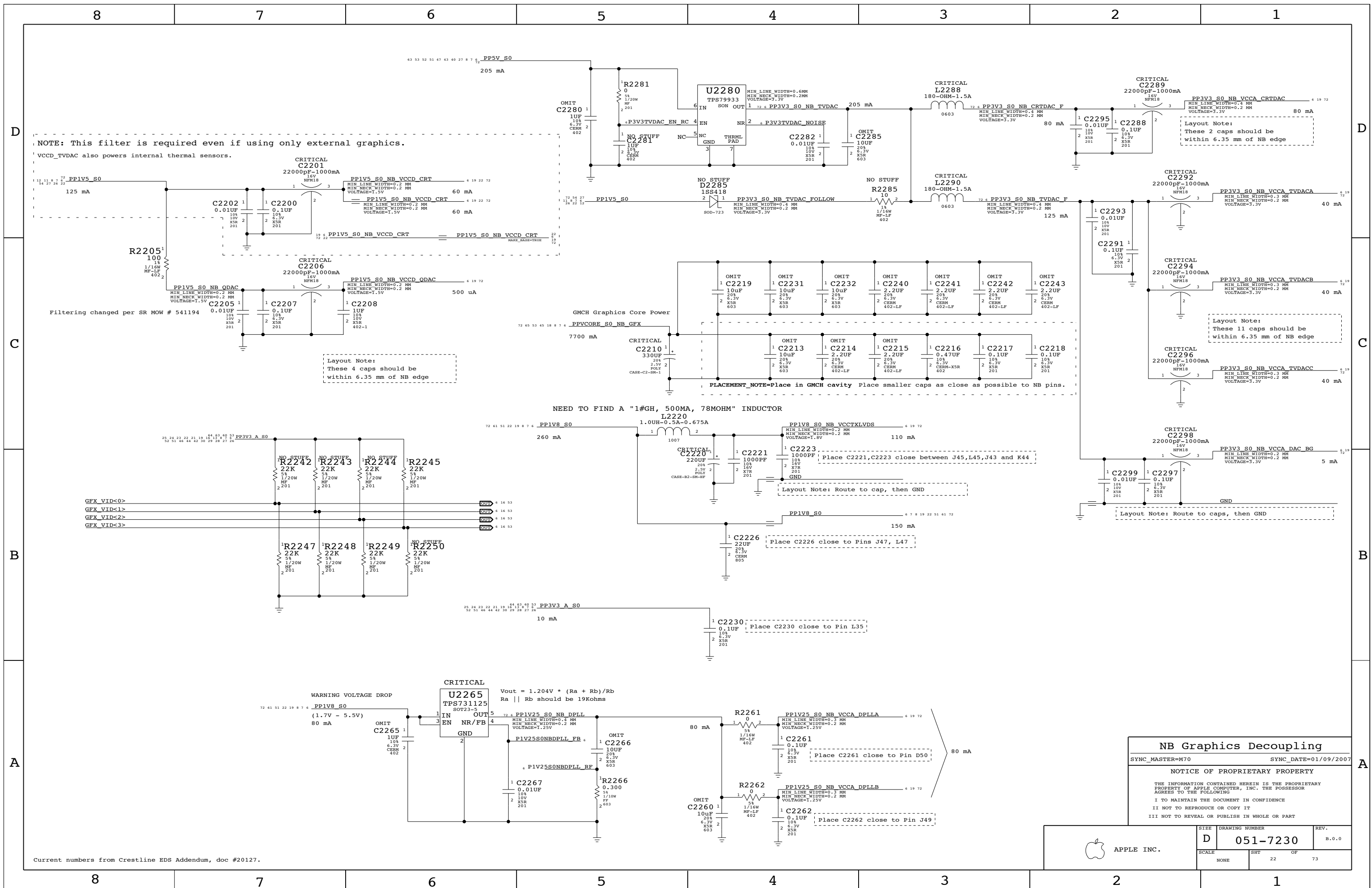
These supplies are still needed even using external GPU



**NB Standard Decoupling**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		21	73

Current numbers from Crestline EDS Addendum, doc .....



NOTE: This filter is required even if using only external graphics.  
 VCCD\_TV DAC also powers internal thermal sensors.

Layout Note:  
 These 2 caps should be  
 within 6.35 mm of NB edge

Layout Note:  
 These 4 caps should be  
 within 6.35 mm of NB edge

Layout Note:  
 These 11 caps should be  
 within 6.35 mm of NB edge

NEED TO FIND A "1#GH, 500MA, 78MOHM" INDUCTOR

Layout Note: Route to cap, then GND

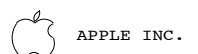
Layout Note: Place C2226 close to Pins J47, L47

Layout Note: Place C2230 close to Pin L35

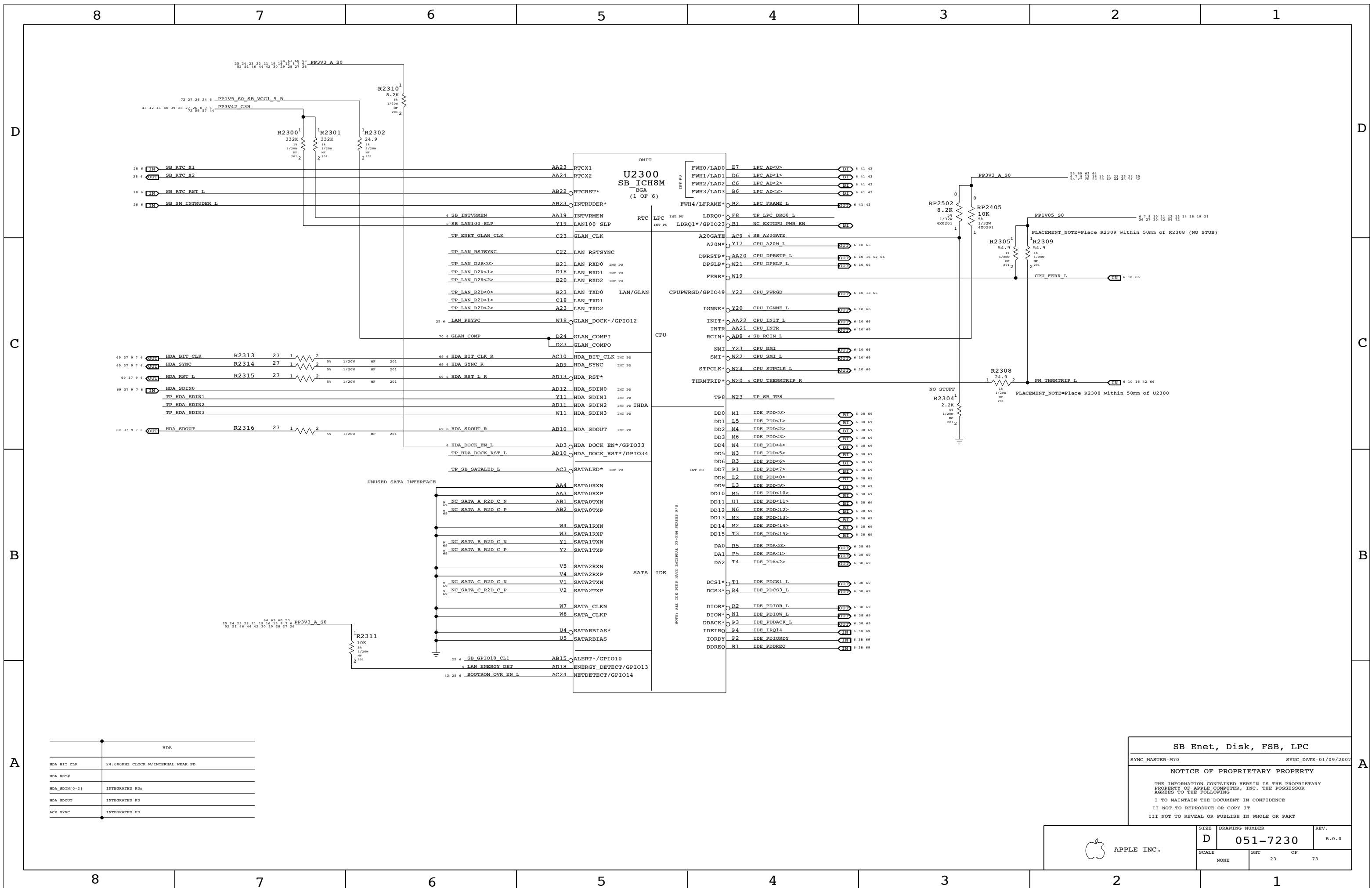
Layout Note: Place C2261 close to Pin D50

Layout Note: Place C2262 close to Pin J49

**NB Graphics Decoupling**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY  
 PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR  
 AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



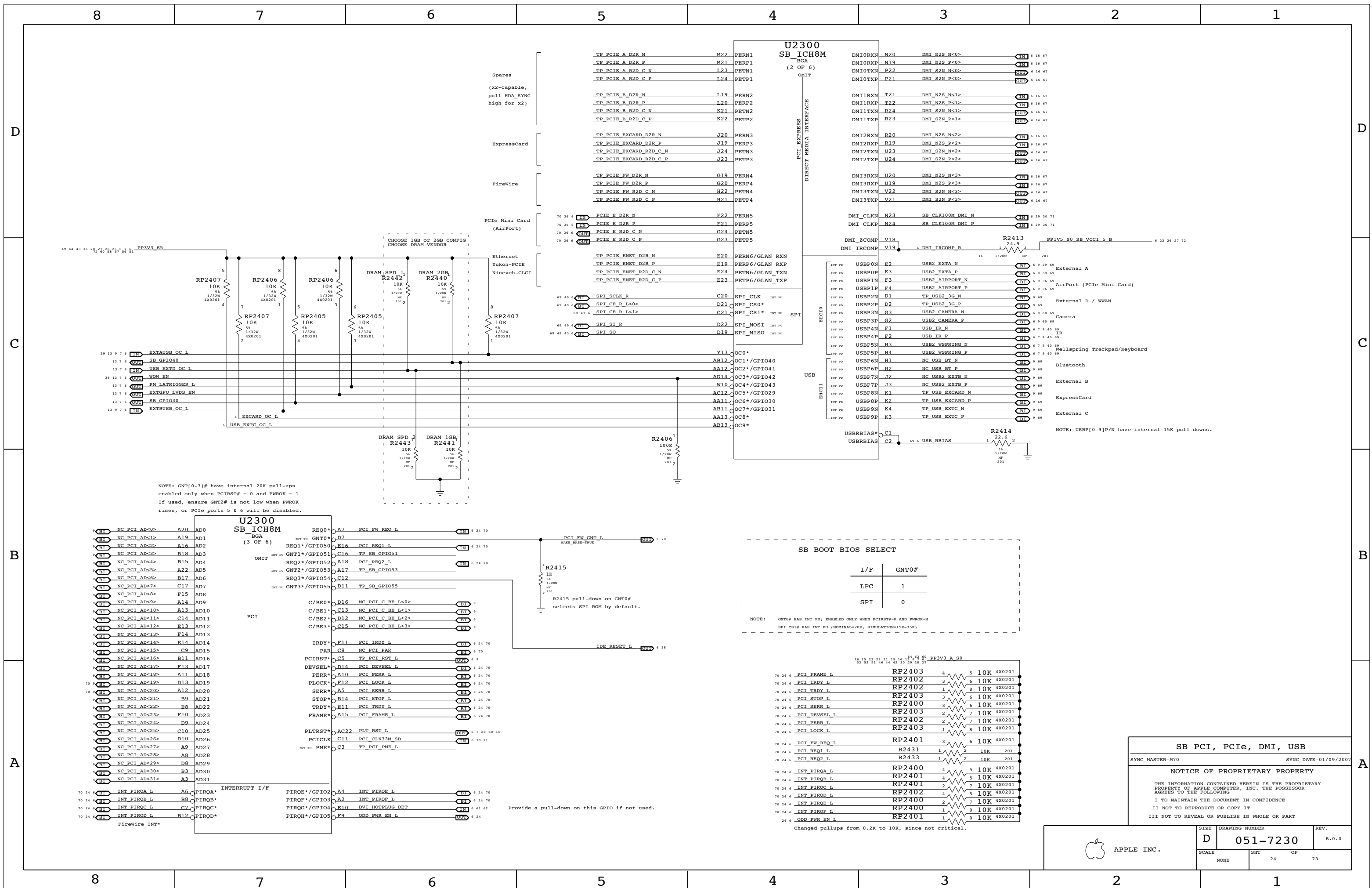
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	22	73



HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDS
HDA_SDOUT	INTEGRATED PD
ACI_SYNC	INTEGRATED PD

<b>SB Enet, Disk, FSB, LPC</b>	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007
<b>NOTICE OF PROPRIETARY PROPERTY</b>	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

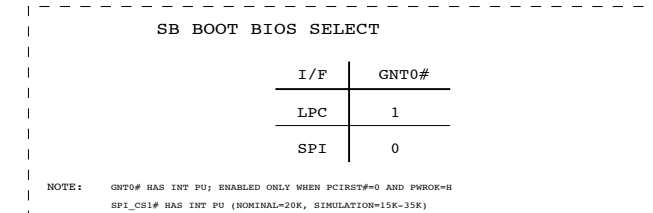
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	23		



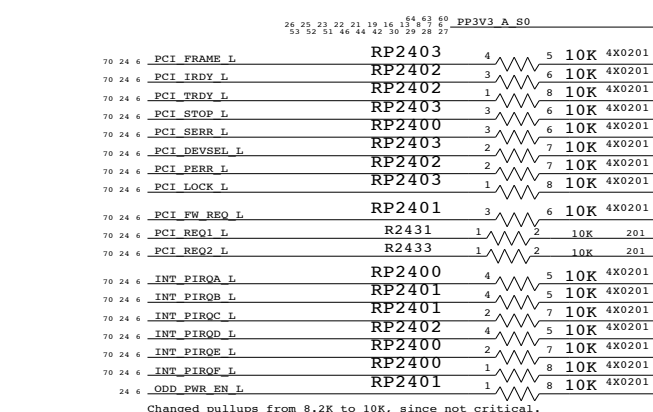
49 44 43 36 28 27 26 25 8 7 6  
PP3V3\_S5

CHOOSE 1GB or 2GB CONFIG  
CHOOSE DRAM VENDOR

NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.



NOTE: GNT0# HAS INT FU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H  
SPI\_CS1# HAS INT FU (NOMINAL=20K, SIMULATION=15K-35K)

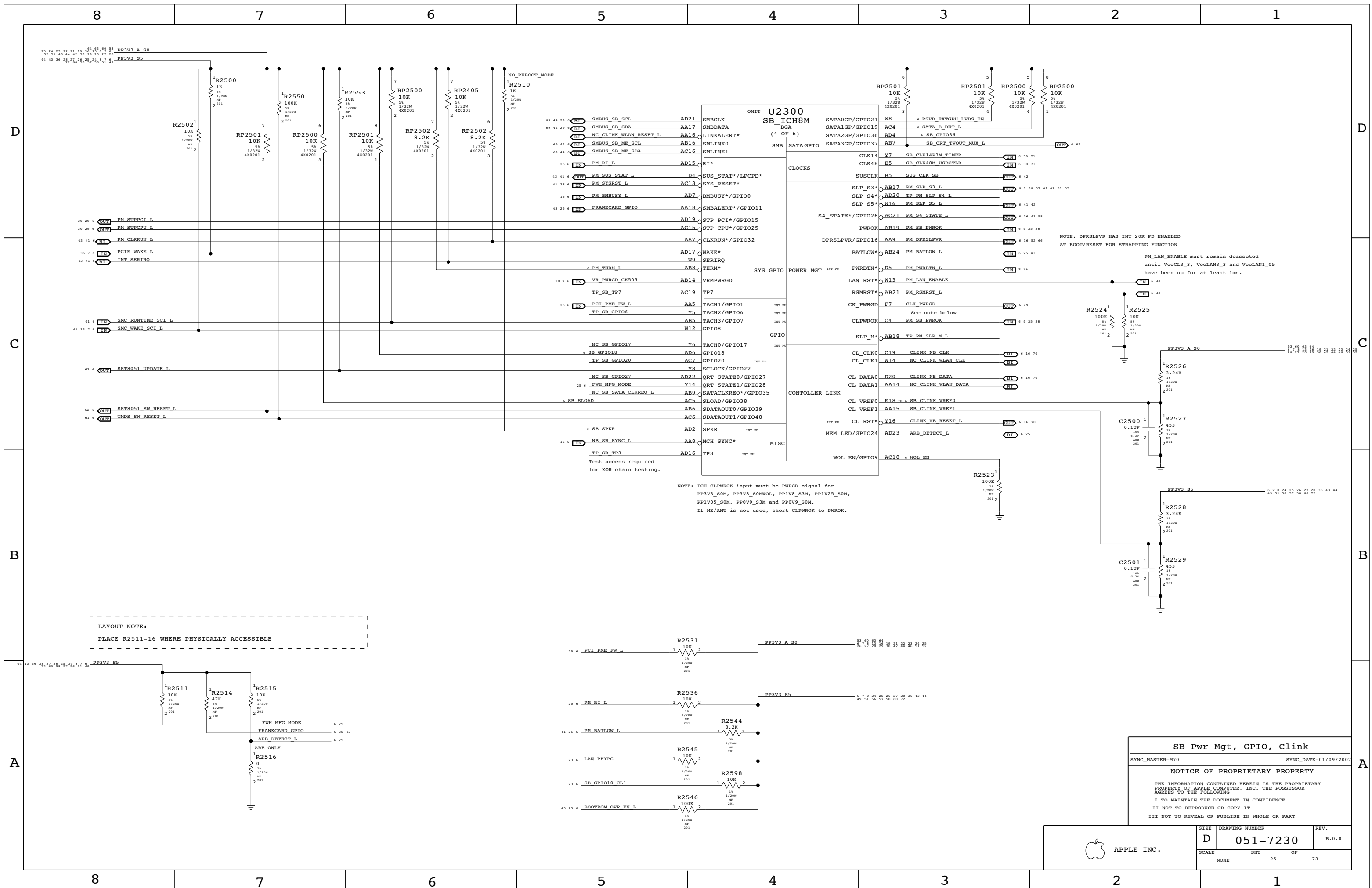


Changed pullups from 8.2K to 10K, since not critical.

SB PCI, PCIe, DMI, USB  
SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART





NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3\_S0M, PP3V3\_S0MMWOL, PP1V8\_S3M, PP1V25\_S0M, PP1V05\_S0M, PP0V9\_S3M and PP0V9\_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

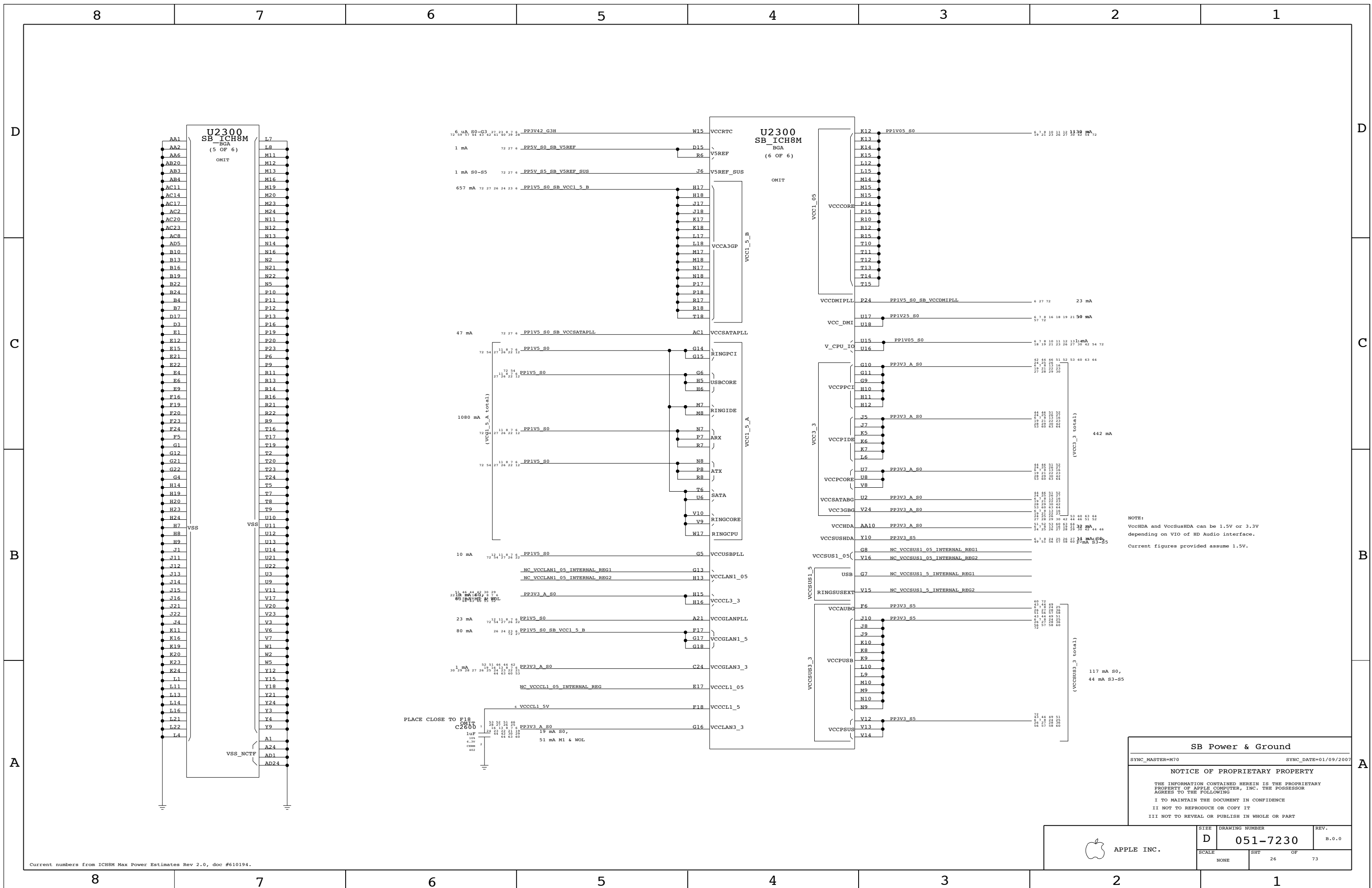
NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION

PM\_LAN\_ENABLE must remain deasserted until VccCL3\_3, VccLAN3\_3 and VccLAN1\_05 have been up for at least 1ms.

LAYOUT NOTE:  
PLACE R2511-16 WHERE PHYSICALLY ACCESSIBLE

**SB Pwr Mgt, GPIO, Clink**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		25	73

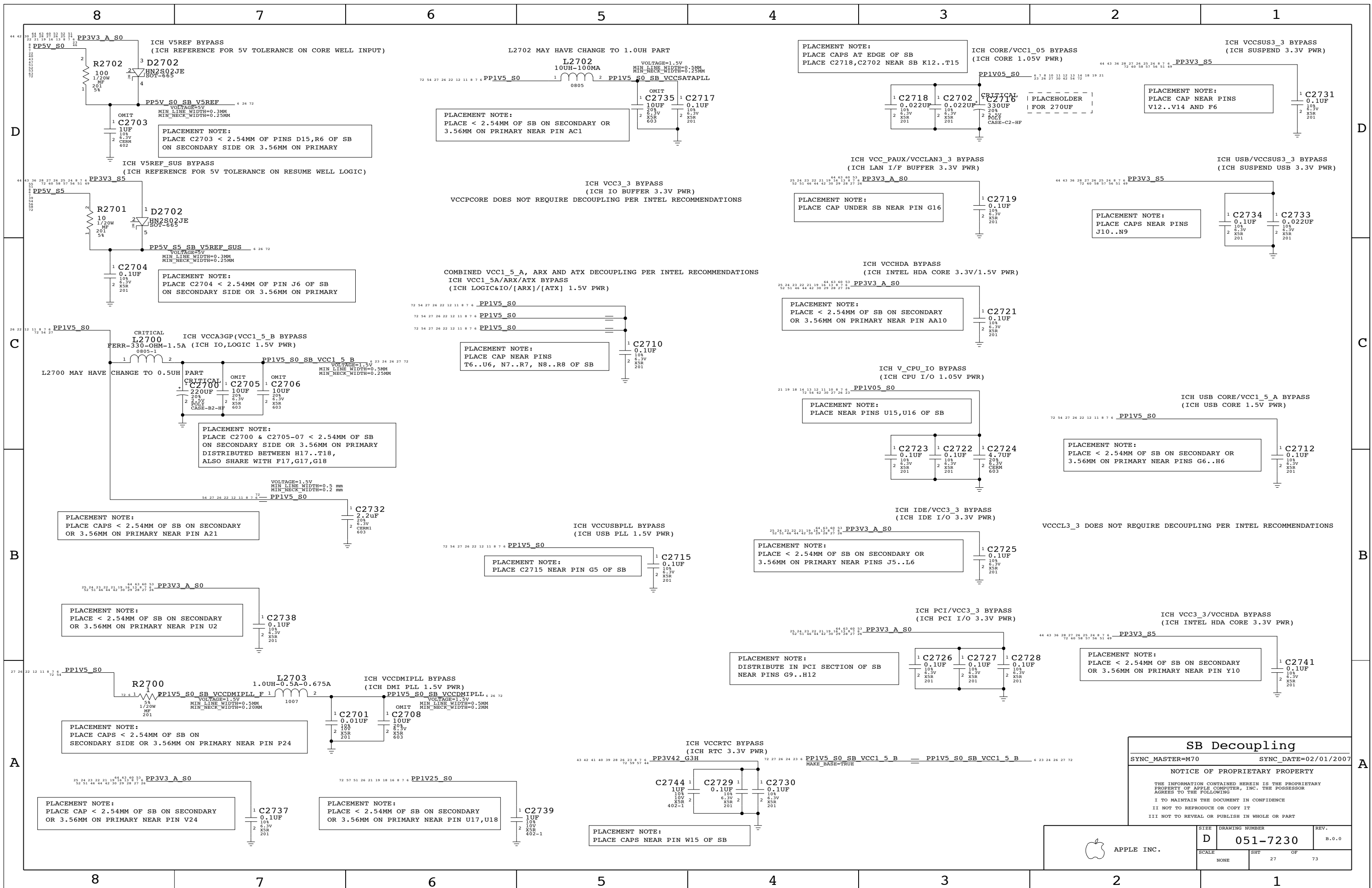


Power Plane	Component	Current (mA)
VCC1_5_B	VCCRTC	6.7
	V5REF	1
	V5REF_SUS	1
	VCC3AGP	657
	VCCDMIPLL	4.27
	VCCDMI	6.7
	V_CPU_IO	6.7
	VCCPPCI	42
	VCCFIDE	44
	VCCPCORE	44
VCC1_5_A	VCCSATABLL	47
	RINGPCI	72
	USBCORE	27
	RINGIDE	11
	ARX	27
	ATX	11
	SATA	27
	RINGCORE	11
	RINGCPU	27
	VCCSUSBP	10
VCC3_3	VCCGLANPLL	23
	VCCGLAN1_5	80
	VCCGLAN3_3	1
	VCCCL1_05	1
	VCCCL1_5	1
	VCCCLAN3_3	1
	VCCSUS1_5	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
VCC3_5	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
	VCCSUS1_05	1
VCCSUS3_3	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1
	VCCSUS3_3	1

NOTE:  
VccHDA and VccSUSHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.  
Current figures provided assume 1.5V.

<b>SB Power &amp; Ground</b>			
SYNC_MASTER=M70		SYNC_DATE=01/09/2007	
<b>NOTICE OF PROPRIETARY PROPERTY</b>			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING			
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	26 OF 73

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.



**SB Decoupling**

SYNC\_MASTER=M70      SYNC\_DATE=02/01/2007

**NOTICE OF PROPRIETARY PROPERTY**

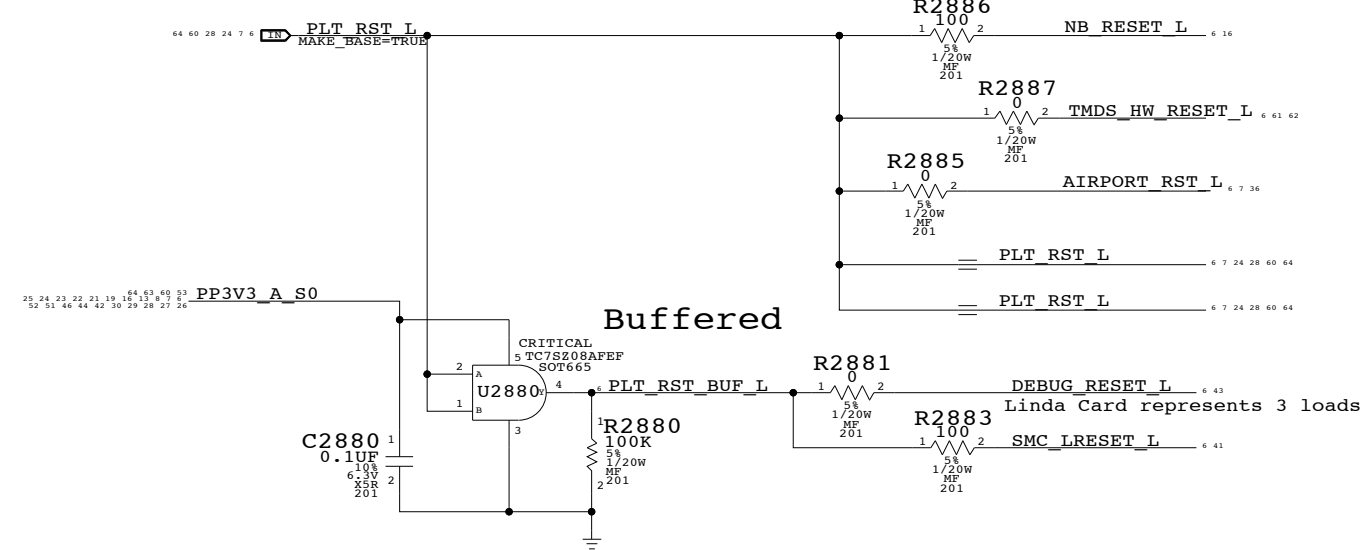
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

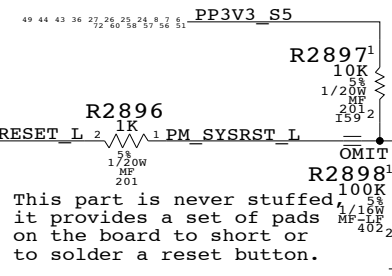
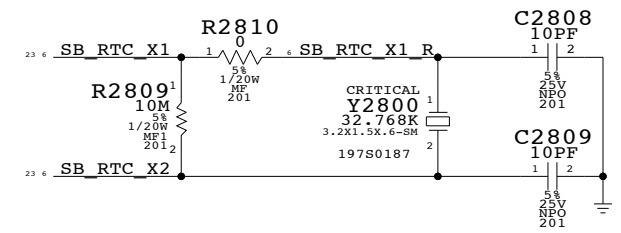
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	SCALE	SHT	OF
	NONE	27	73

# Platform Reset Connections

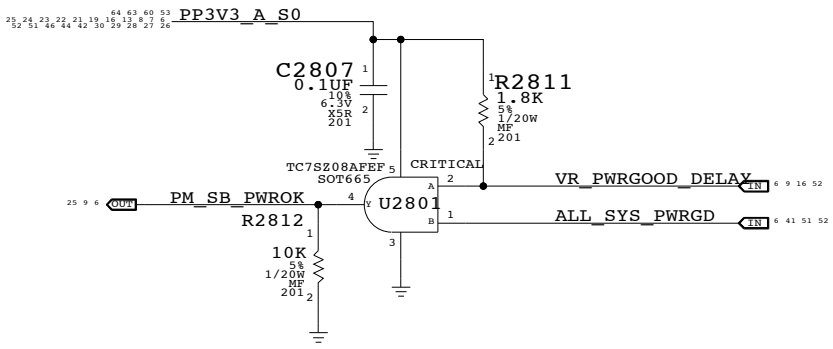
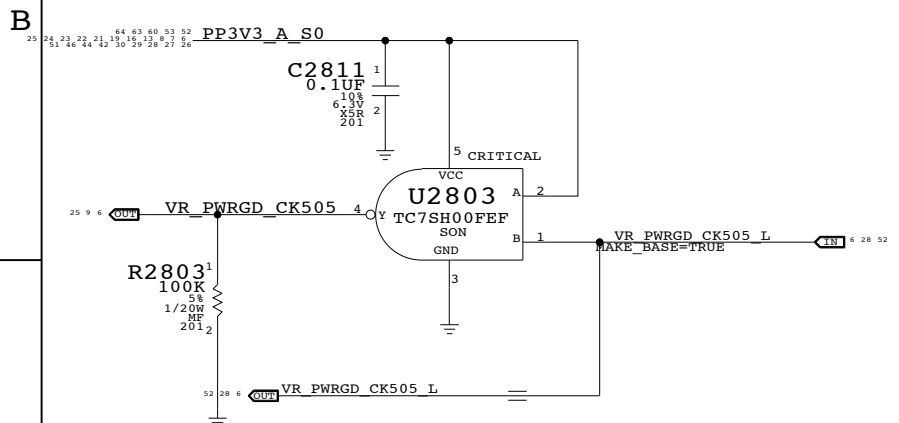
Unbuffered



## SB RTC Crystal Circuit



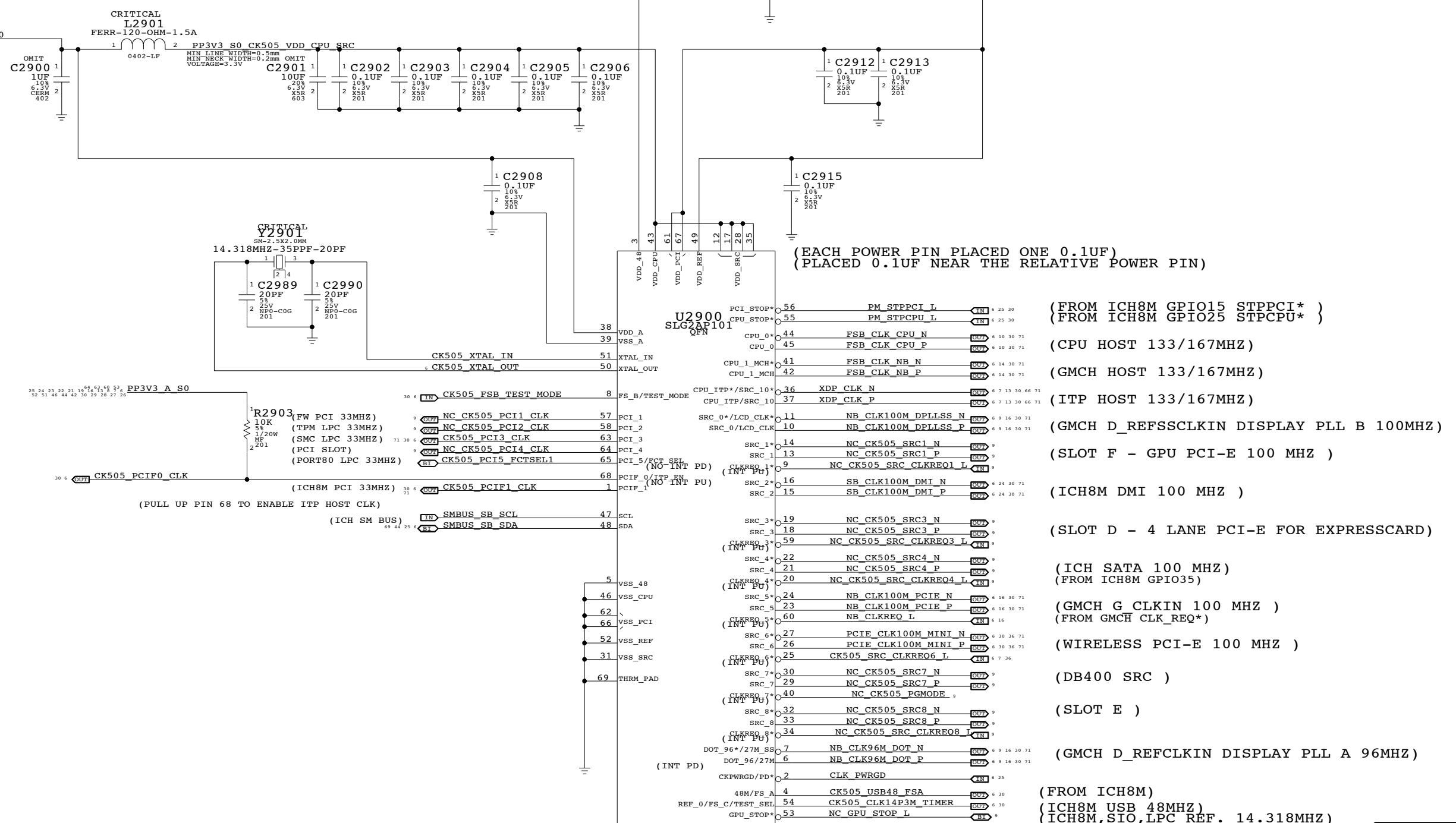
**Silk: "SYS RST"**  
Place R2898 pads on bottom side near board edge



**SB Misc**  
 SYNC\_MASTER=M70      SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		28	73

Silego recommend to remove L2903,R2900,C2907,C2910  
R2901,L2902,C2916,C2911,C2914 and R2902



(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- (FROM ICH8M GPIO15 STPPCI\* )
- (FROM ICH8M GPIO25 STPCPU\* )
- (CPU HOST 133/167MHZ)
- (GMCH HOST 133/167MHZ)
- (ITP HOST 133/167MHZ)
- (GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)
- (SLOT F - GPU PCI-E 100 MHZ )
- (ICH8M DMI 100 MHZ )
- (SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
- (ICH SATA 100 MHZ)
- (FROM ICH8M GPIO35)
- (GMCH G CLKIN 100 MHZ )
- (FROM GMCH CLK\_REQ\*)
- (WIRELESS PCI-E 100 MHZ )
- (DB400 SRC )
- (SLOT E )
- (GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)
- (FROM ICH8M)
- (ICH8M USB 48MHZ)
- (ICH8M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT96T	DOT96C	100MT_SST	100MC_SST
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM  
\* FOR EXT. GRAPHIC SYSTEM

**Clock (CK505)**

SYNC\_MASTER=M70      SYNC\_DATE=02/01/2007

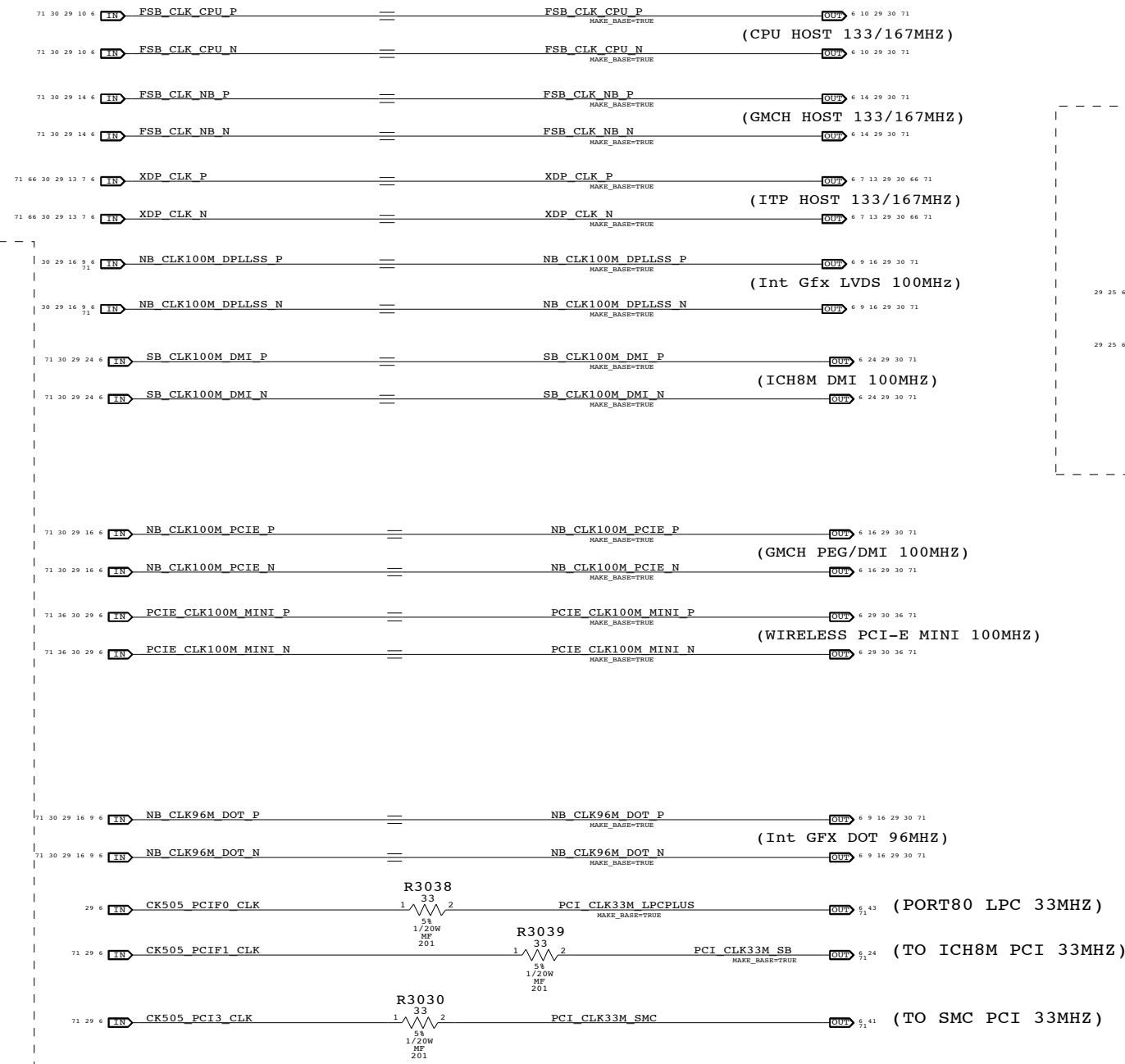
**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

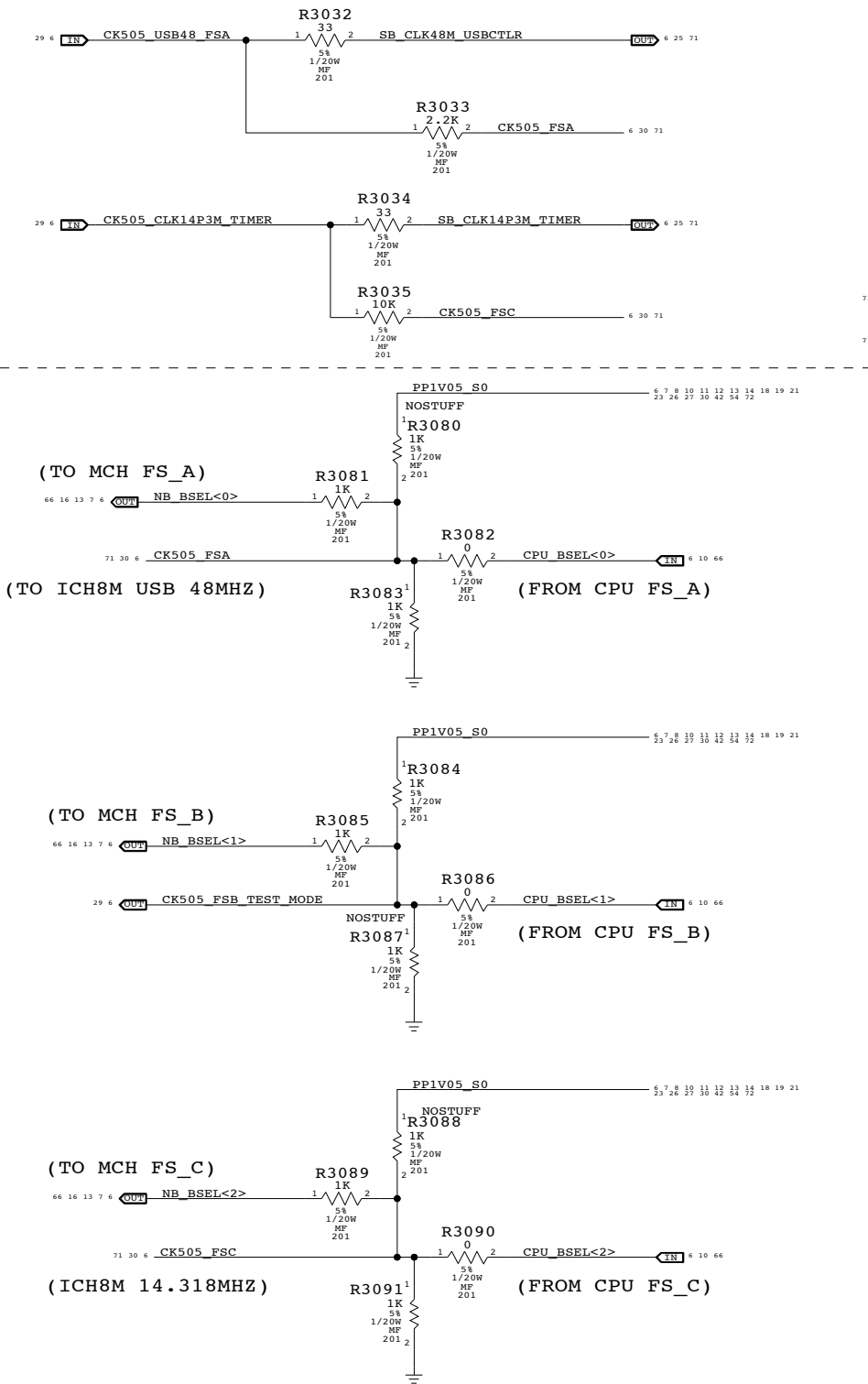
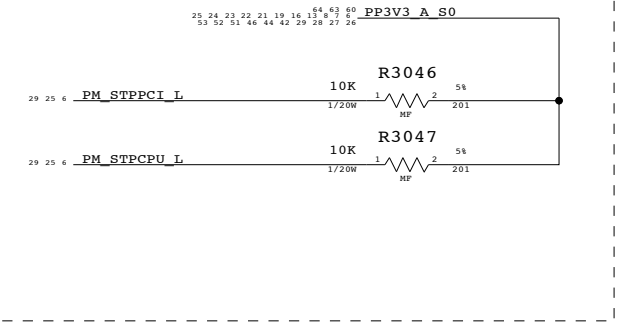
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	29		

# CLK Termination



## CLKREQ Controls

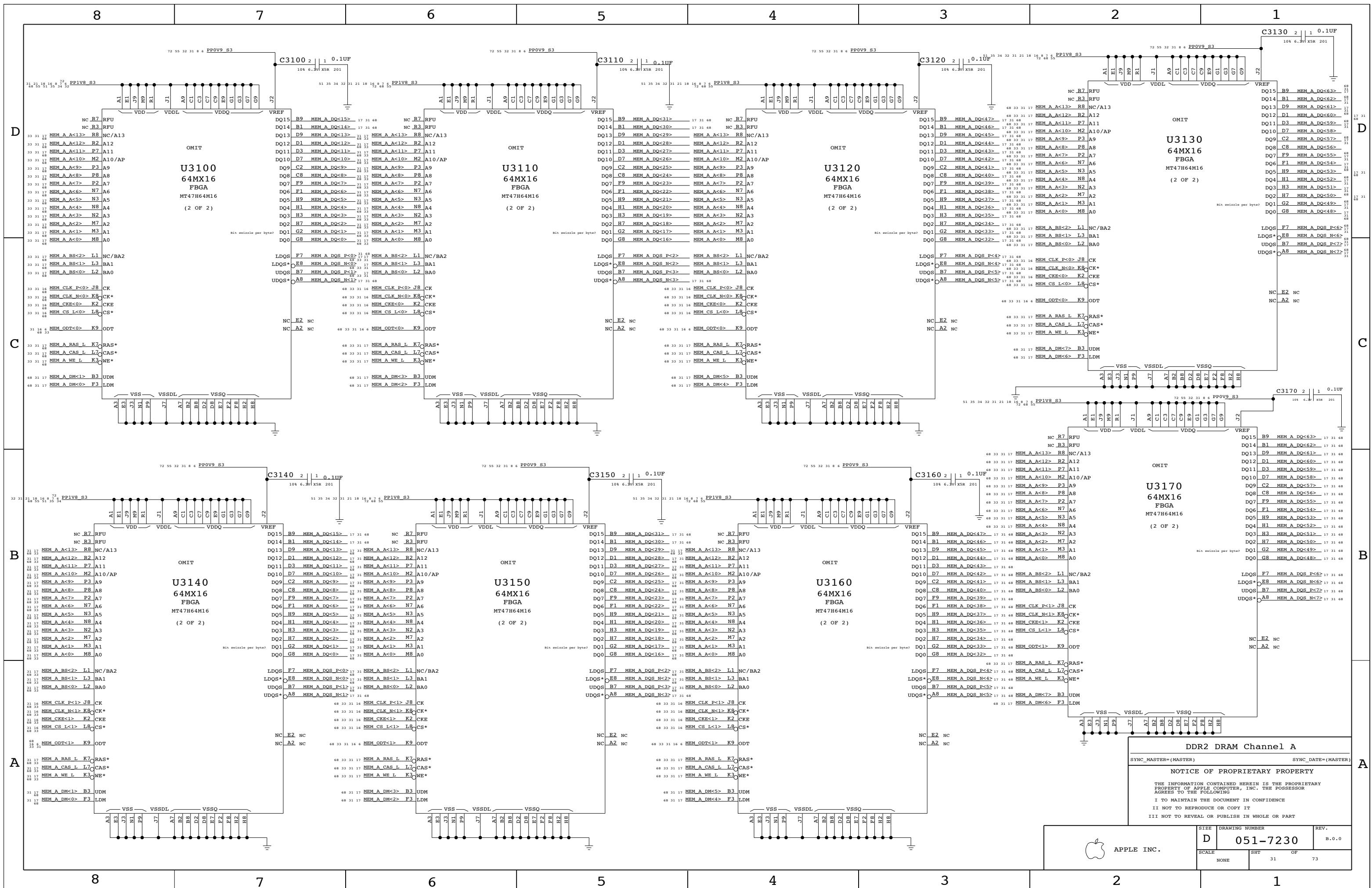


FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	1	166M
* 0	1	0	200M
1	1	0	400M
1	1	1	Resrvd
1	0	1	100M
1	0	0	333M

NOSTUFF R3082, R3086, R3090  
FOR MANUAL CPU FREQUENCY  
CPU speed is currently set to 200MHz

**Clock Termination**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC. DRAWING NUMBER: D 051-7230 REV. B.0.0  
 SCALE: NONE SHT: 30 OF 73

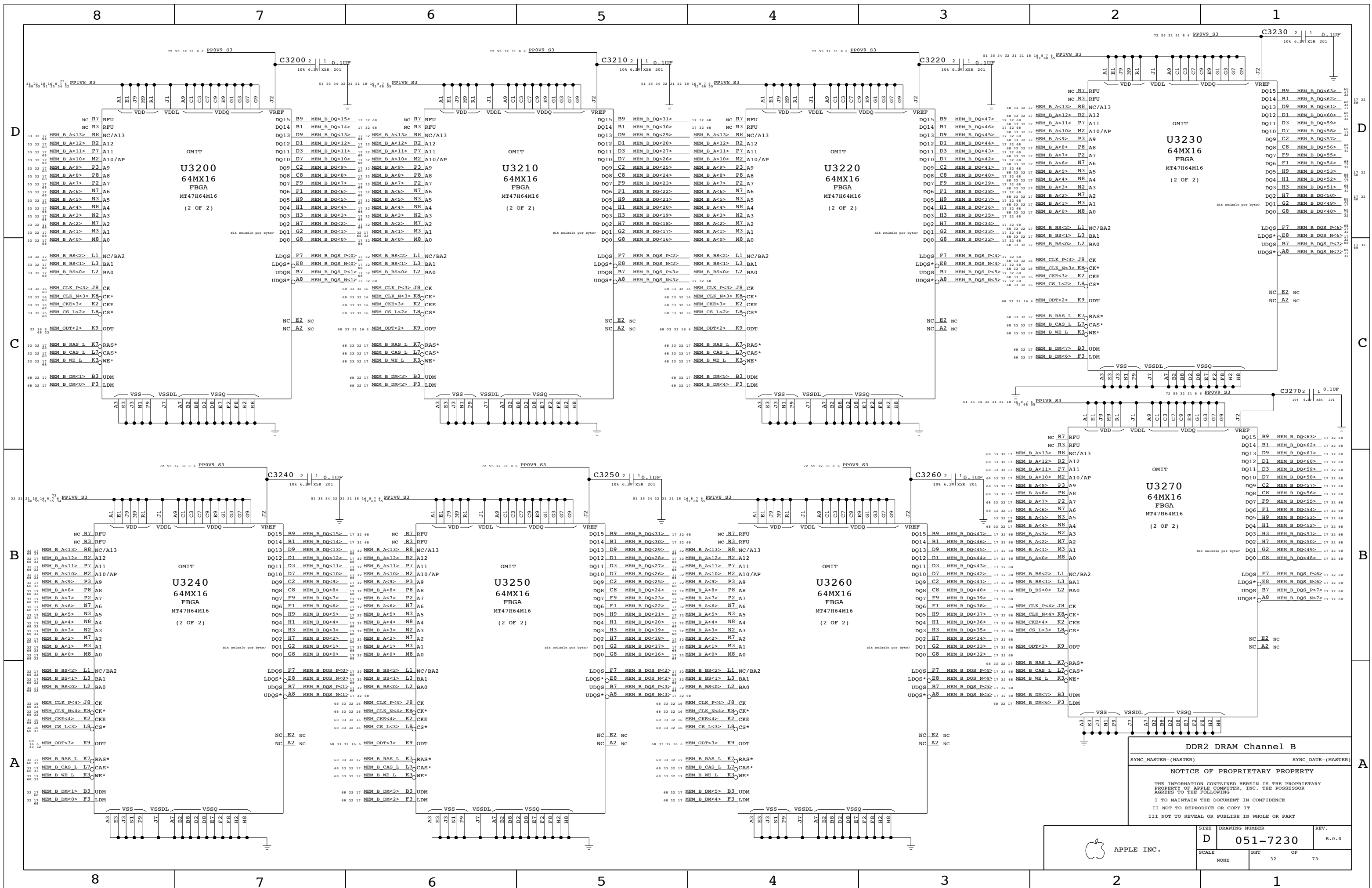


U3130  
64MX16  
FBGA  
MT47H64M16  
(2 OF 2)

U3170  
64MX16  
FBGA  
MT47H64M16  
(2 OF 2)

DDR2 DRAM Channel A  
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



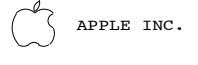
U3230  
64MX16  
FBGA  
MT47H64M16  
(2 OF 2)

U3270  
64MX16  
FBGA  
MT47H64M16  
(2 OF 2)

DDR2 DRAM Channel B  
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

**NOTICE OF PROPRIETARY PROPERTY**  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	32	73





8

7

6

5

4

3

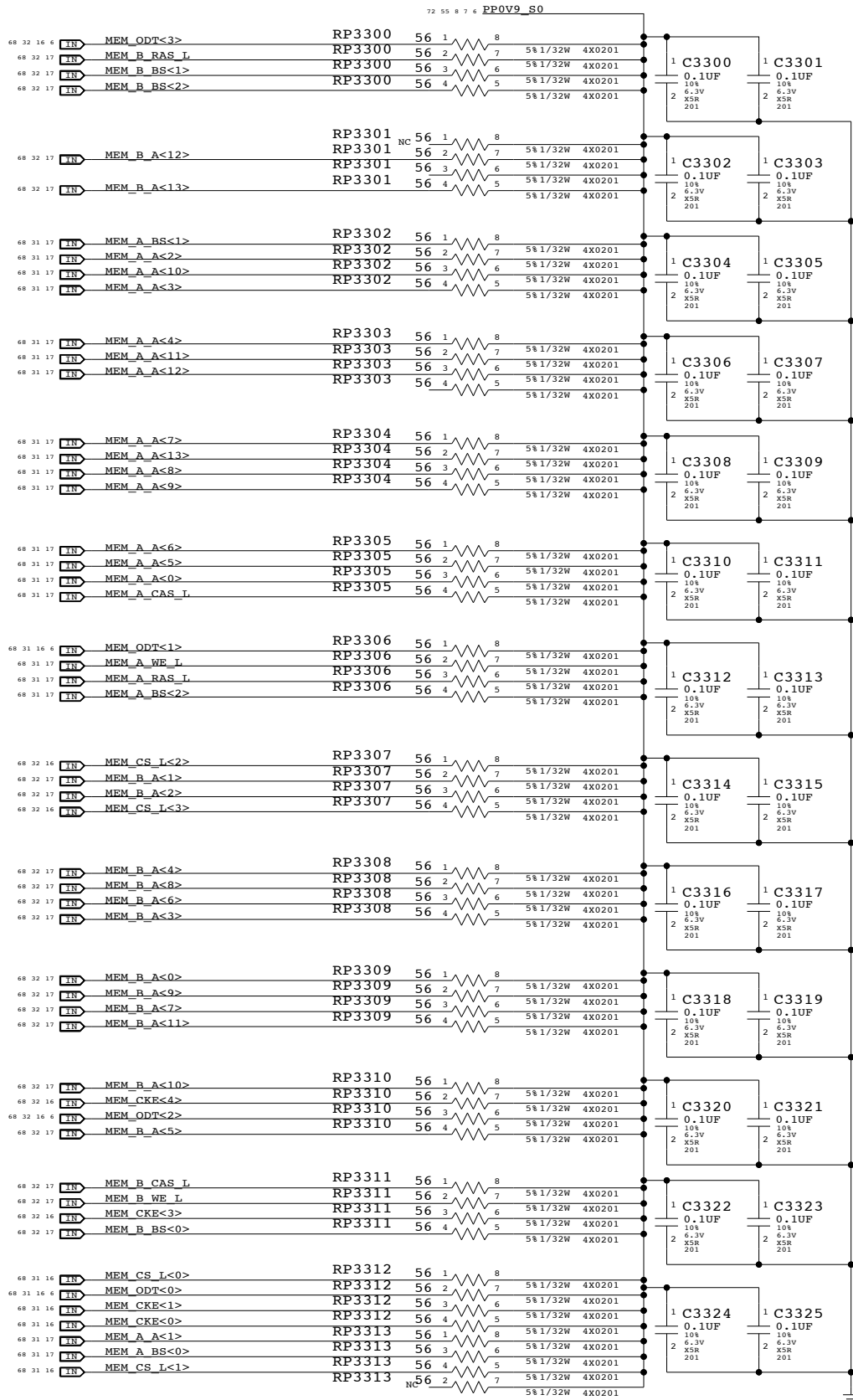
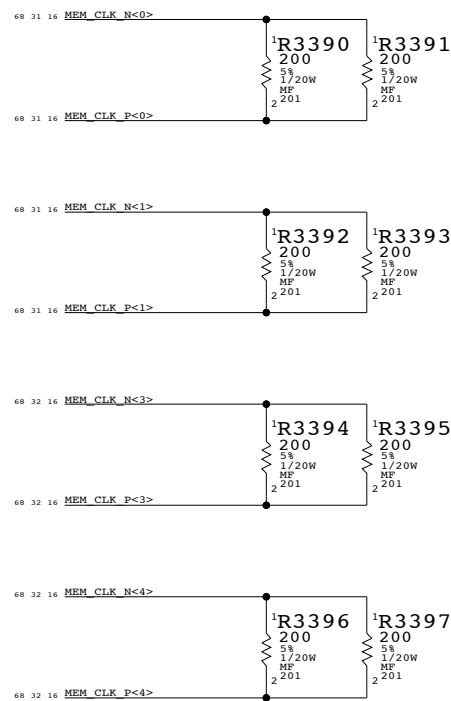
2

1

One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it

MEM CLOCK TERMINATION

Place one resistor at each end of Y split



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9\_S0\_MEM\_TERM

Memory Active Termination

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	33	73

8

7

6

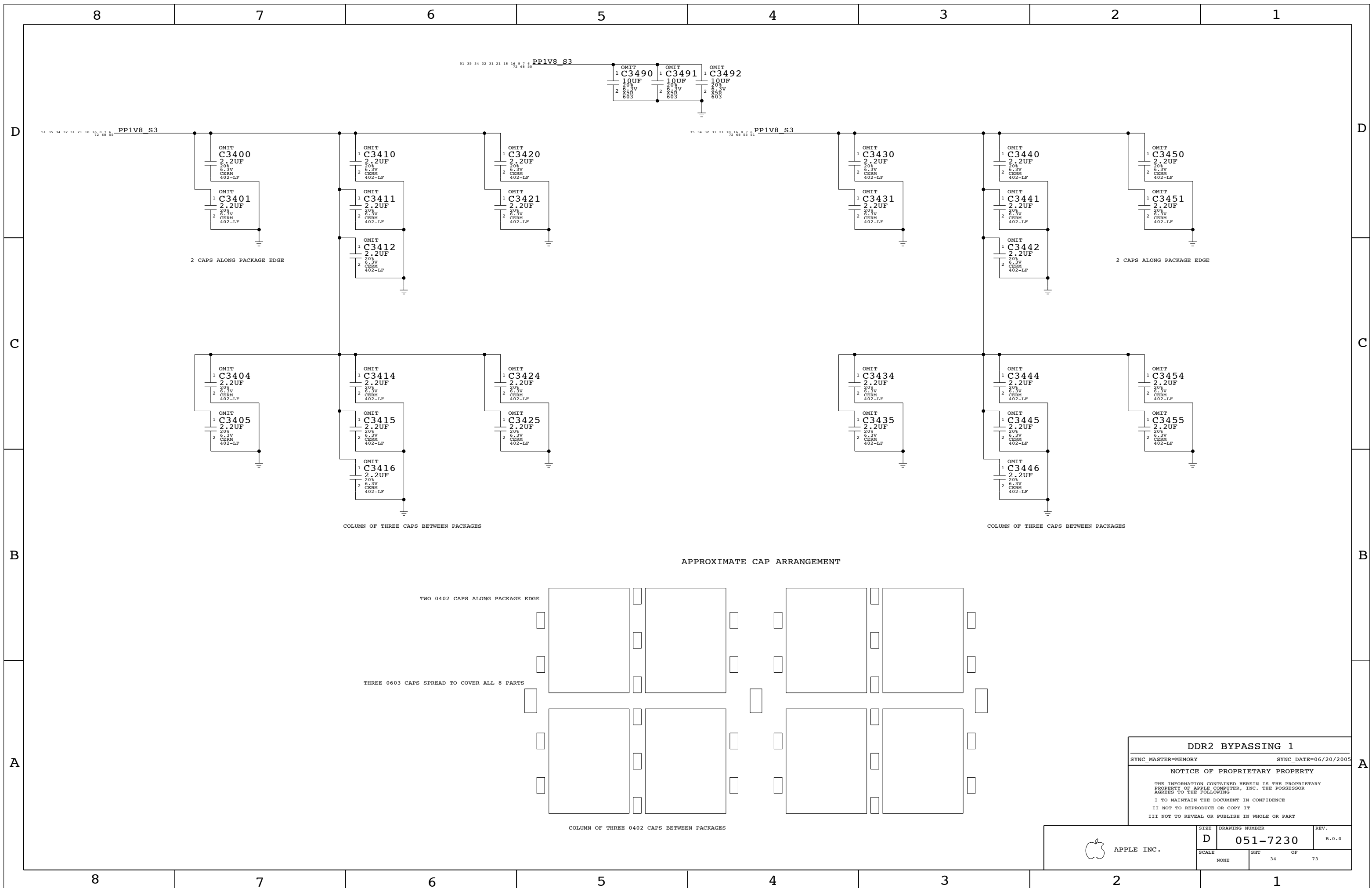
5

4

3

2

1



**DDR2 BYPASSING 1**

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

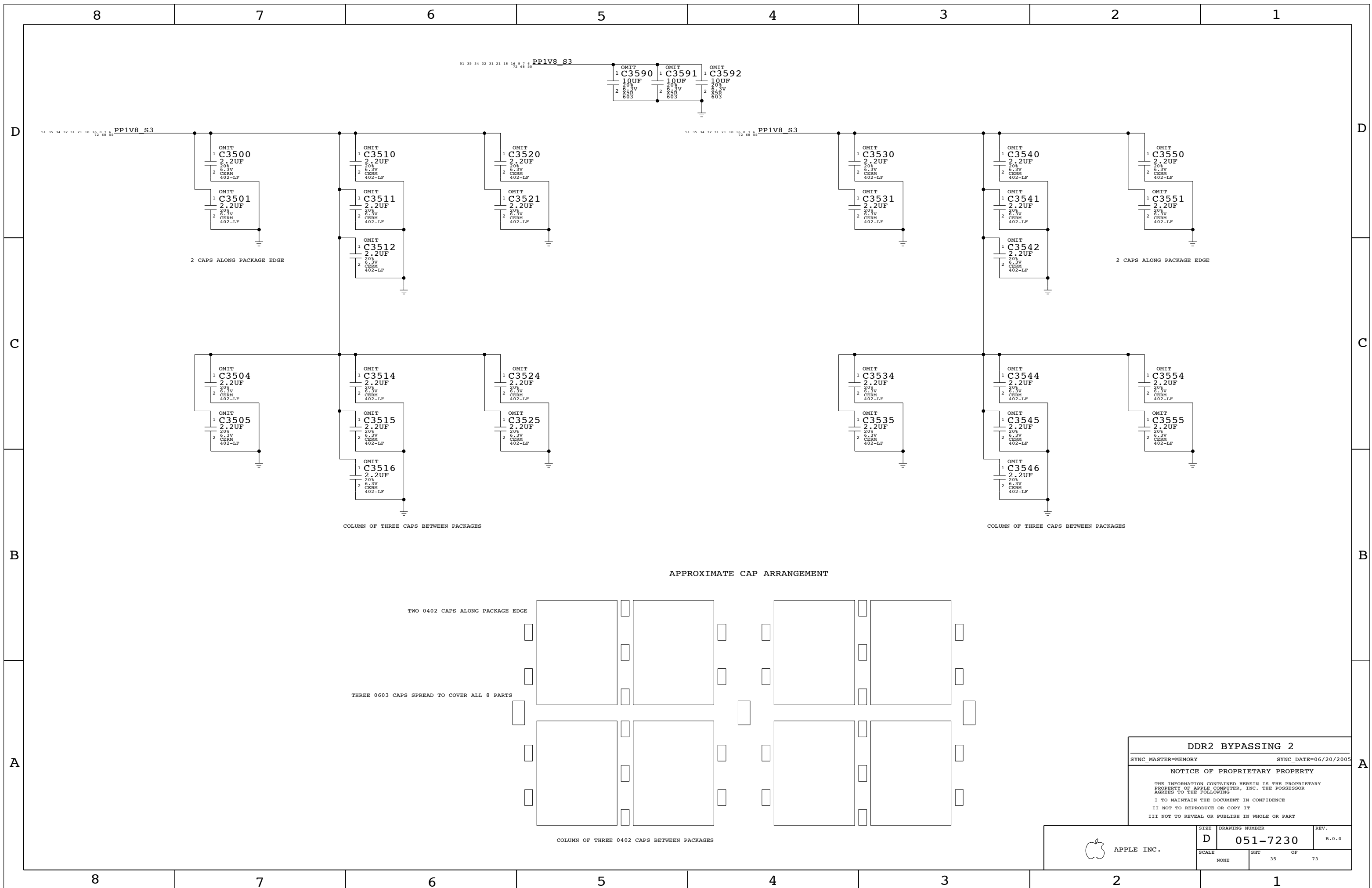
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

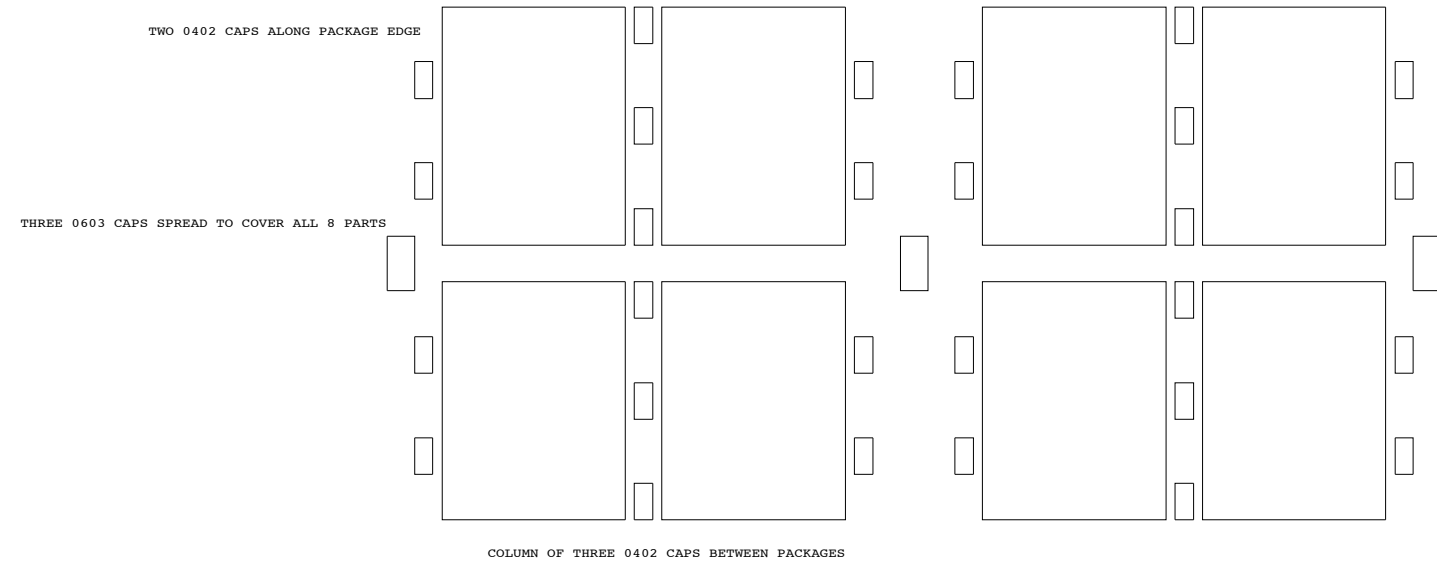
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SCALE	SHEET	OF	REV.
	NONE	34	73	B.0.0

SIZE	DRAWING NUMBER
D	051-7230



APPROXIMATE CAP ARRANGEMENT



**DDR2 BYPASSING 2**

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SCALE	SHEET	OF	REV.
	NONE	35	73	B.0.0

SIZE	DRAWING NUMBER
D	051-7230

8

7

6

5

4

3

2

1

D

D

C

C

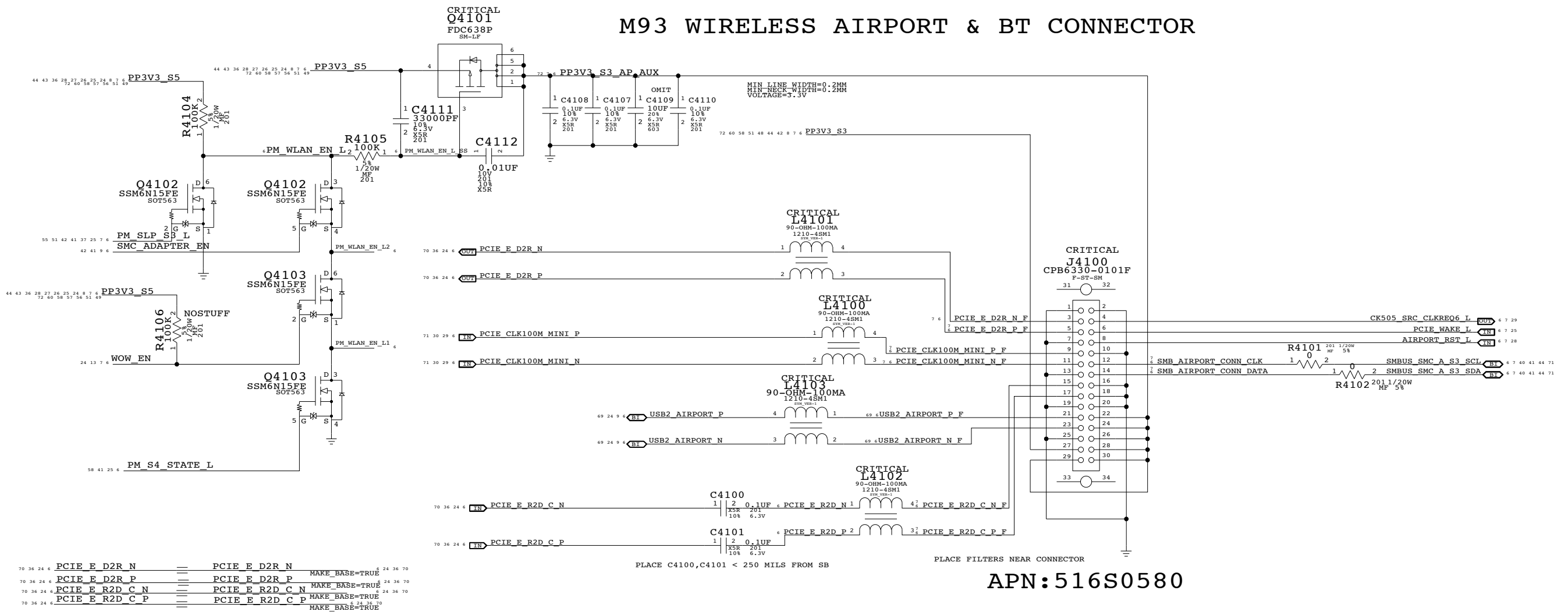
B

B

A

A

# M93 WIRELESS AIRPORT & BT CONNECTOR



70 36 24 6	PCIE_E D2R_N	PCIE_E D2R_N	MAKE_BASE=TRUE	24 36 70
70 36 24 6	PCIE_E D2R_P	PCIE_E D2R_P	MAKE_BASE=TRUE	24 36 70
70 36 24 6	PCIE_E R2D_C_N	PCIE_E R2D_C_N	MAKE_BASE=TRUE	24 36 70
70 36 24 6	PCIE_E R2D_C_P	PCIE_E R2D_C_P	MAKE_BASE=TRUE	24 36 70

## APN: 516S0580

Wireless M93 Connector

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	36	73

8

7

6

5

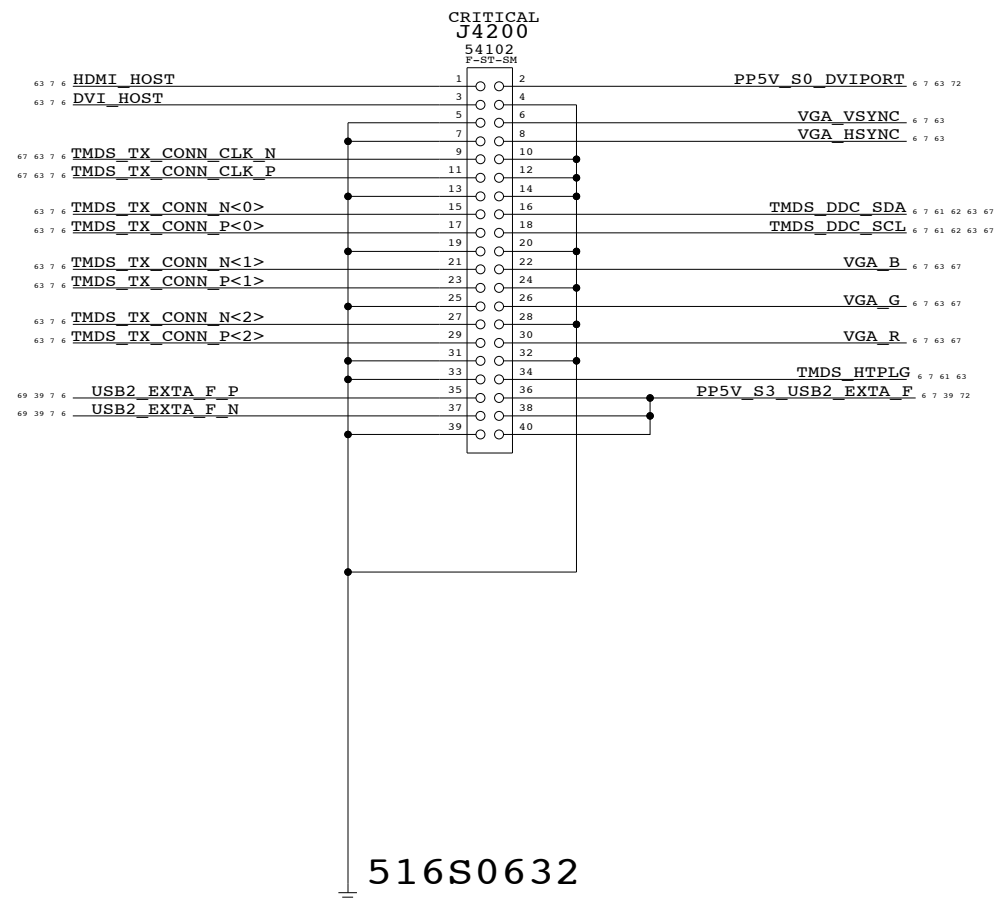
4

3

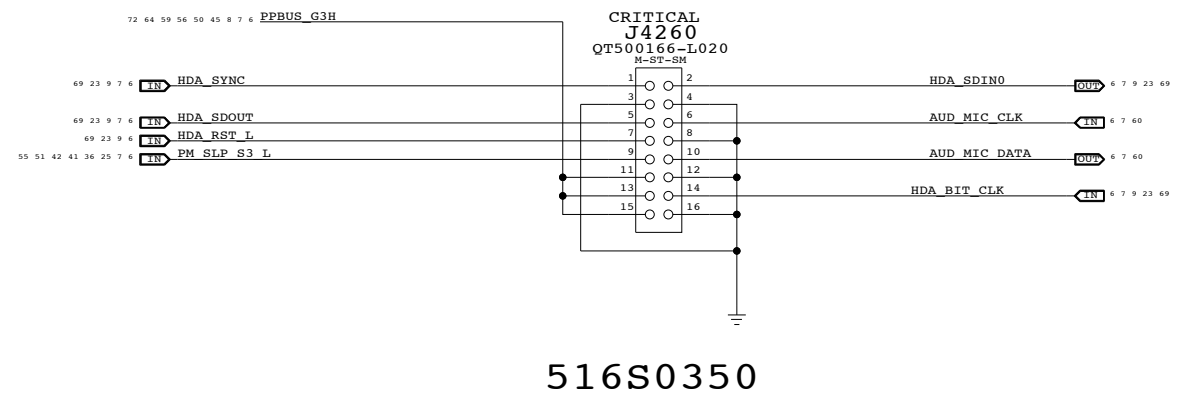
2

1

# Micro DVI, USB, to RIO Hatch Assembly

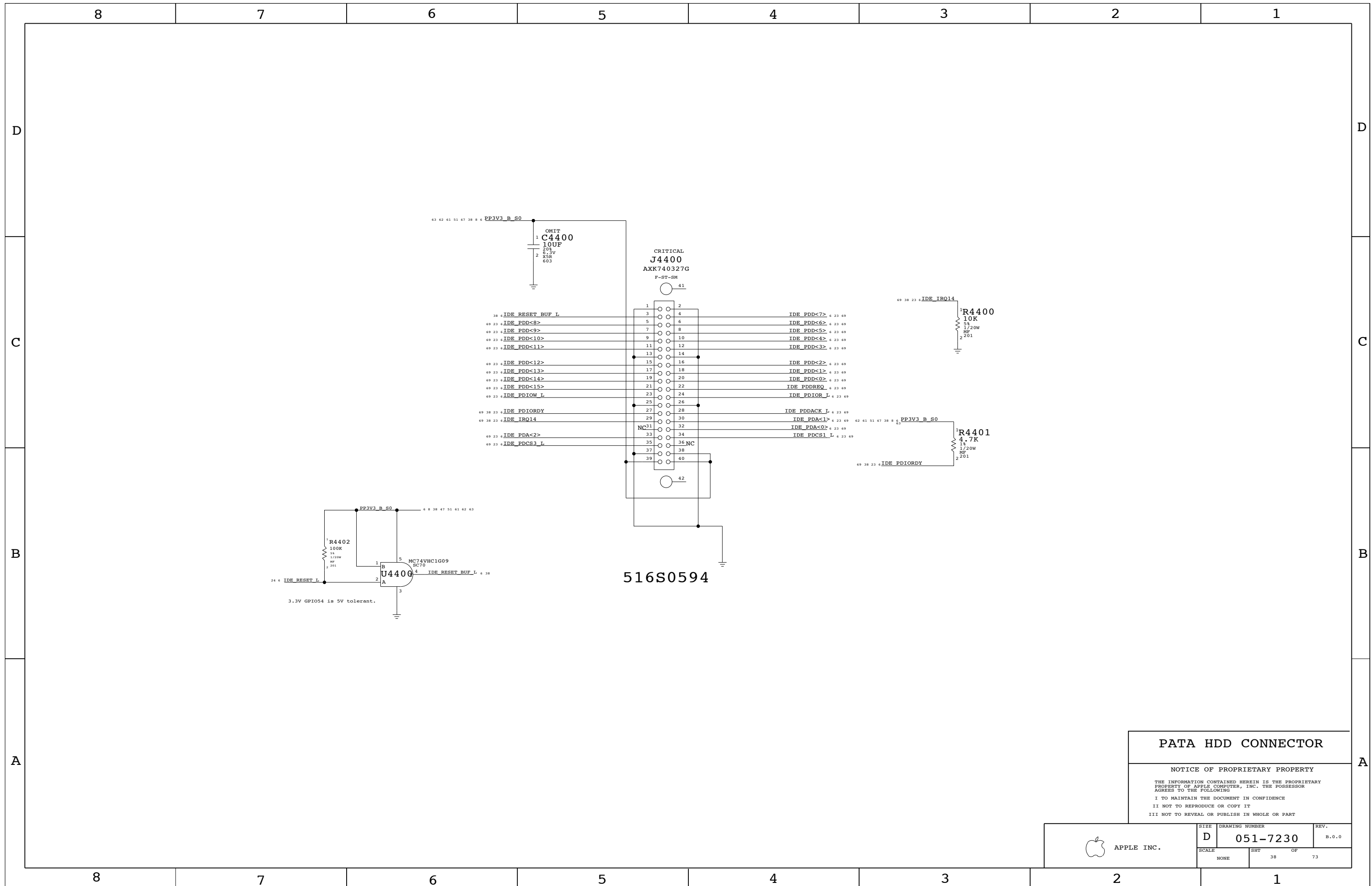


# Audio Connector



Hatch and Audio Connectors  
 SYNC\_MASTER={MASTER} SYNC\_DATE={MASTER}  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	
NONE	37	73	



**PATA HDD CONNECTOR**

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		
NONE	38 OF 73		

8

7

6

5

4

3

2

1

D

D

C

C

B

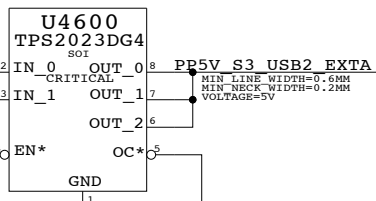
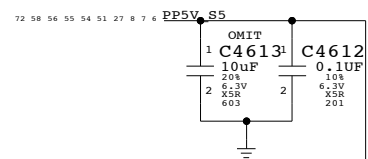
B

A

A

### USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT



PM\_SLP\_S4\_LS5V

R4650



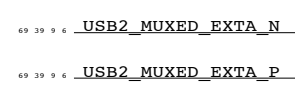
CURRENT LIMIT TO 1.5A CONTINUOUS

CRITICAL L4602 FERR-120-OHM-3A

PP5V S3 USB2 EXTA\_F  
MIN LINE WIDTH=0.6MM  
MIN TRACE WIDTH=0.2MM  
VOLTAGE=5V

ROUTE USB DATA LINES AS DIFFERENTIAL PAIRS

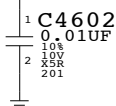
CRITICAL L4600 90-OHM-100MA 1210-45M1



PP5V S3 USB2 EXTA\_F  
USB2\_EXTA\_F\_N  
USB2\_EXTA\_F\_P

CONNECT TO RIO CONNECTOR J4200

CRITICAL D4600 RCLAMP0502B



C4602 0.01uF

LAYOUT NOTE: C4602 IS AN EMC BY-PASS CAP FOR J4200

### USB/SMC MUX

PP3V42\_G3H

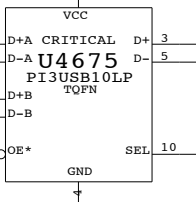
R4675 100



C4675 0.1uF

PLACE C4675 NEAR U4675

R4677 10K



SMC\_RX\_L  
SMC\_TX\_L

USB2\_EXTA\_P  
USB2\_EXTA\_N

USB2\_MUXED\_EXTA\_P  
USB2\_MUXED\_EXTA\_N

USB\_DEBUGPRT\_EN\_L

SEL=0 CHOOSE SMC  
SEL=1 CHOOSE USB

**USB EXTERNAL CONNECTORS**

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		73
NONE	39		

8

7

6

5

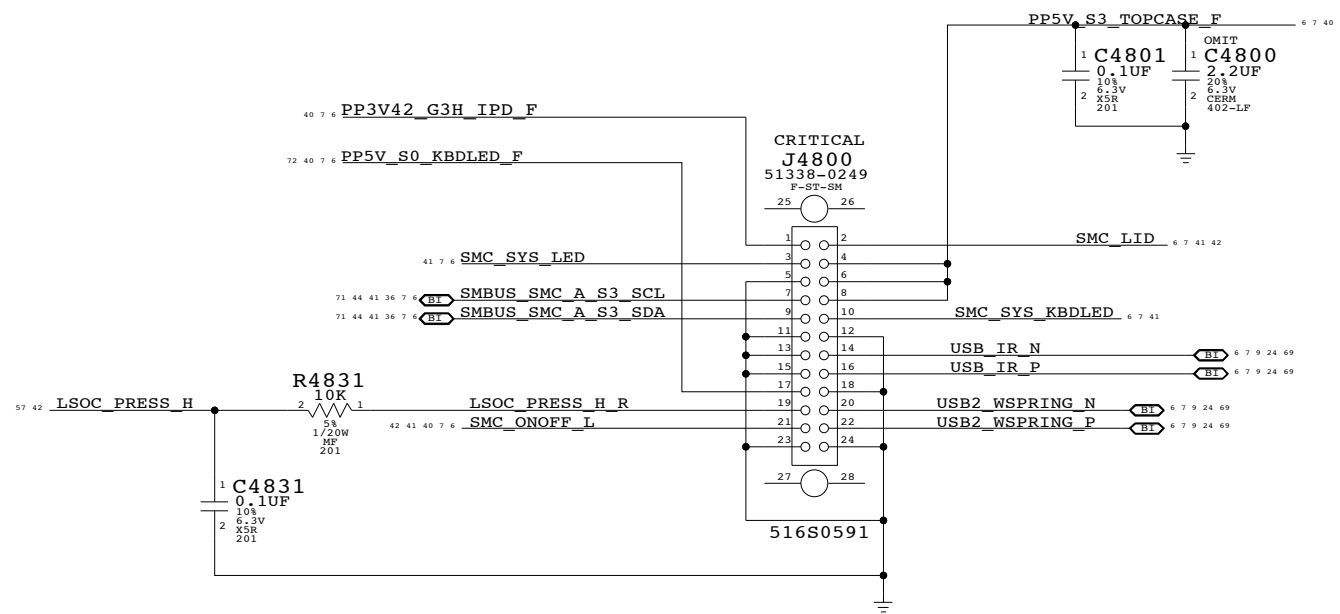
4

3

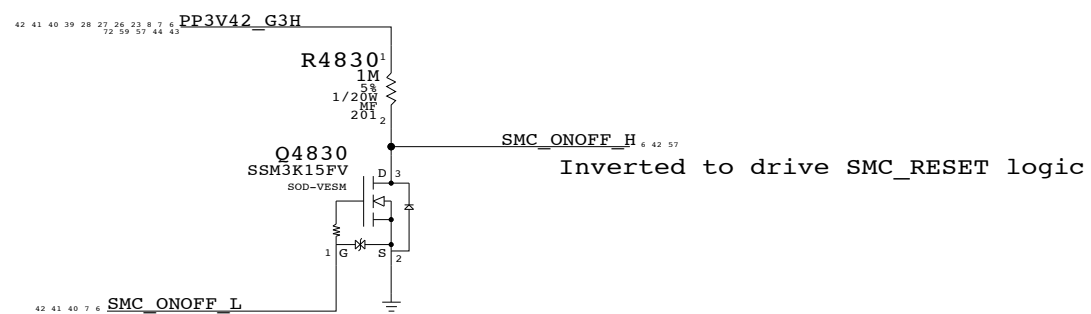
2

1

# IPD Connector



## Power Button Inverter



8 7 6 5 4 3 2 1

D

D

C

C

B

B

A

A

8 7 6 5 4 3 2 1

**IPD Connector**

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7230</b>	REV. B.0.0
	SCALE NONE	SHEET 40	OF 73



8

7

6

5

4

3

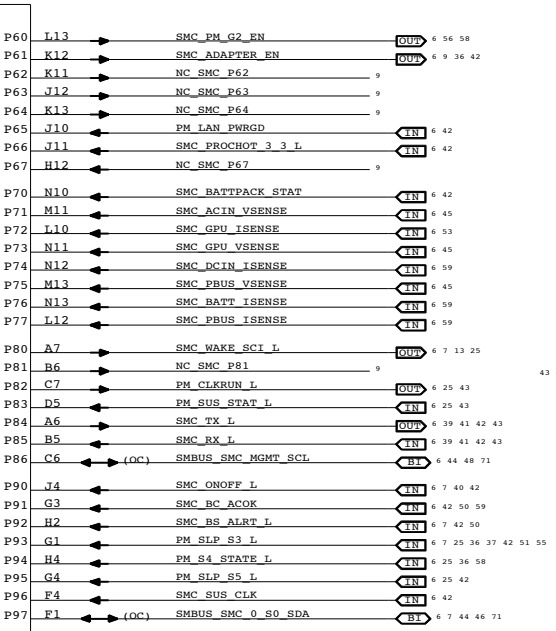
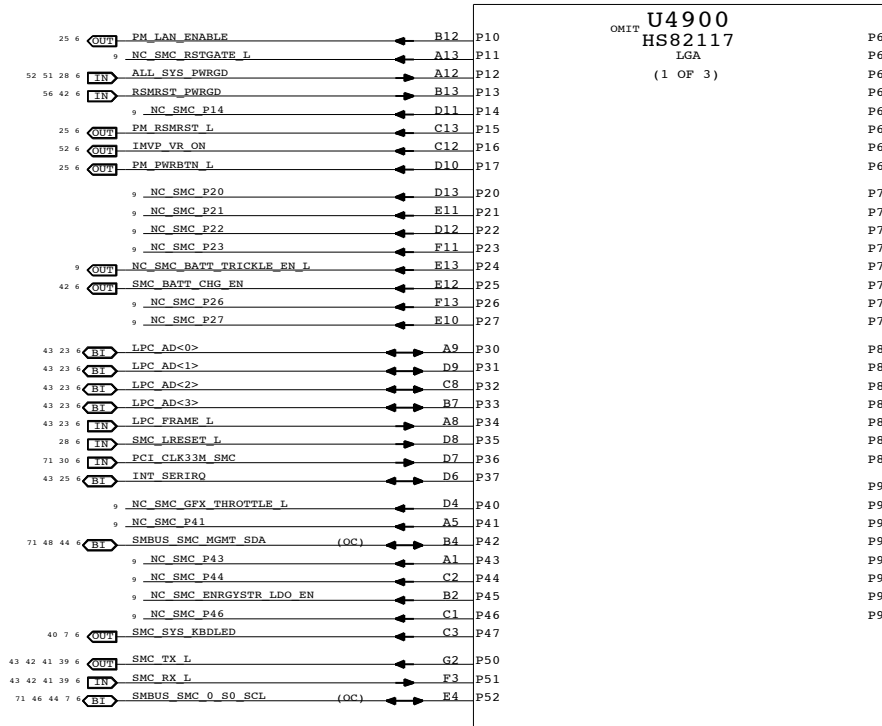
2

1

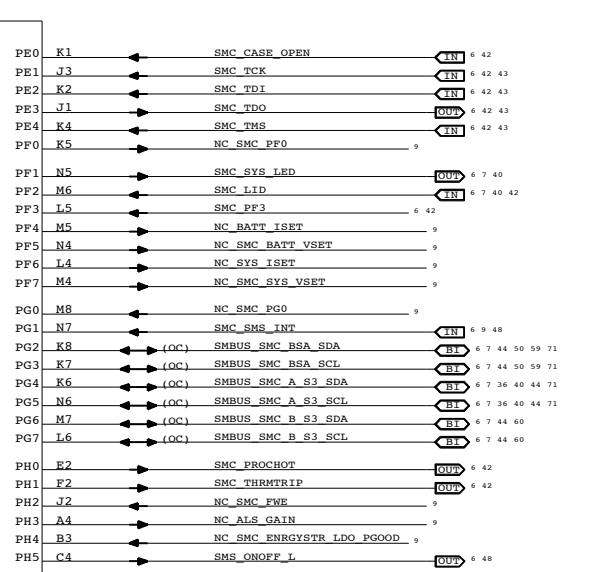
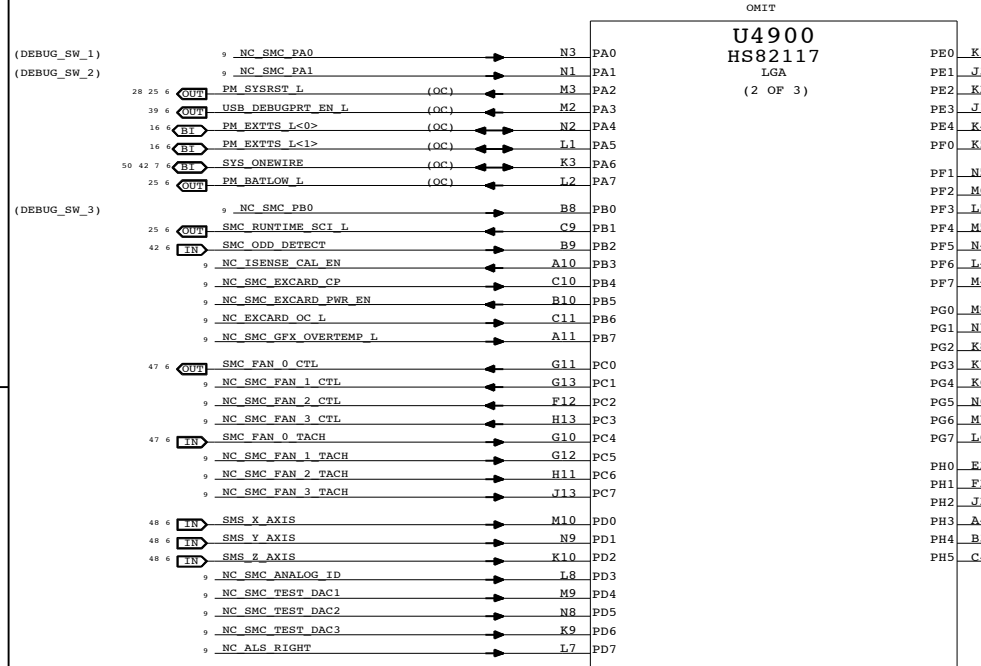
NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

# SMC

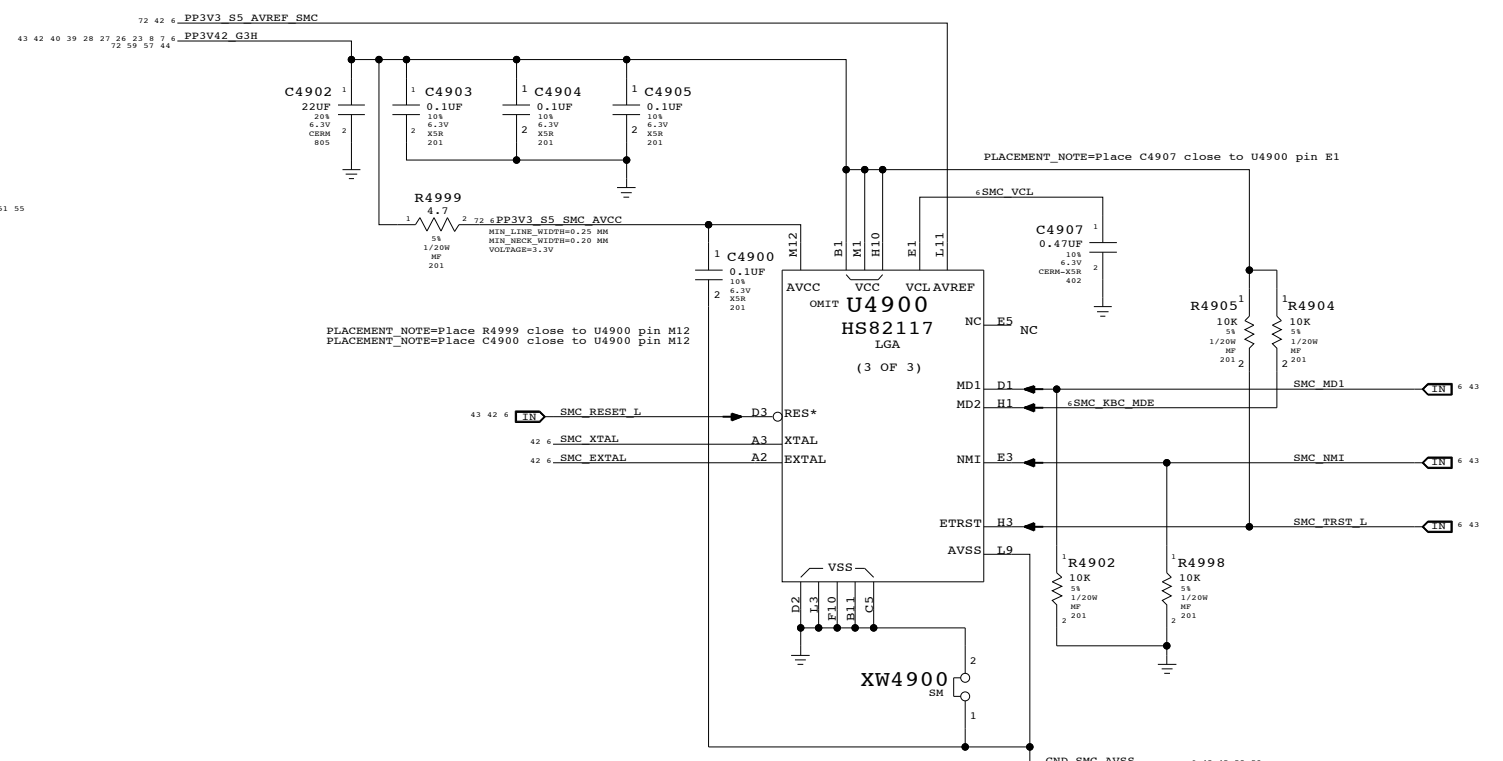
U4900  
HS82117  
LGA  
(1 OF 3)



U4900  
HS82117  
LGA  
(2 OF 3)



NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.



SMC

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		41	73

8

7

6

5

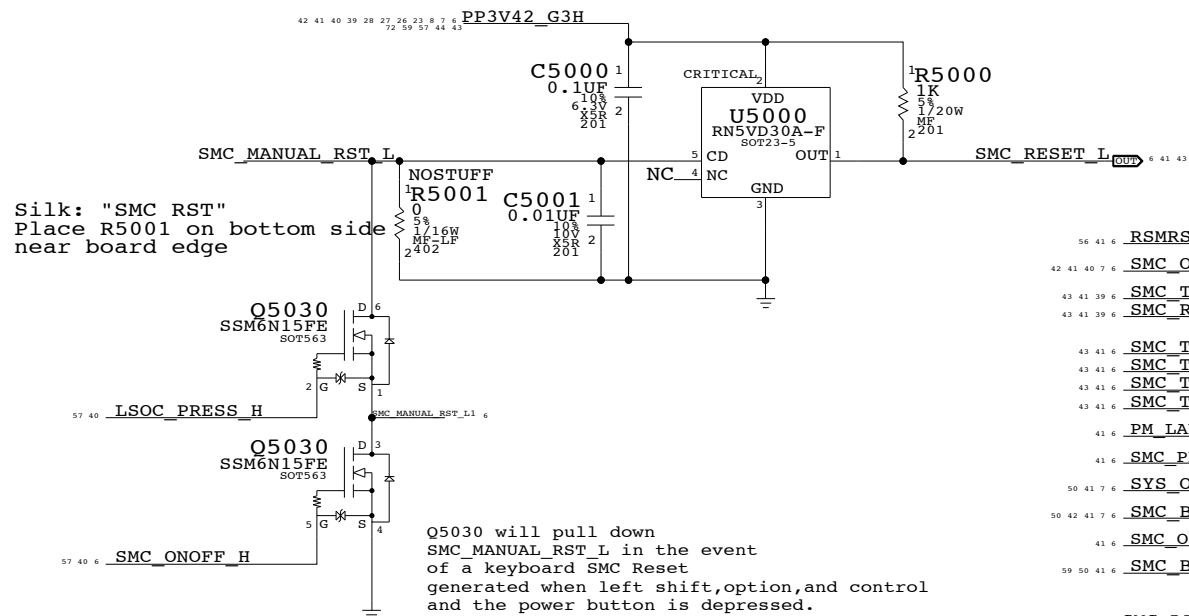
4

3

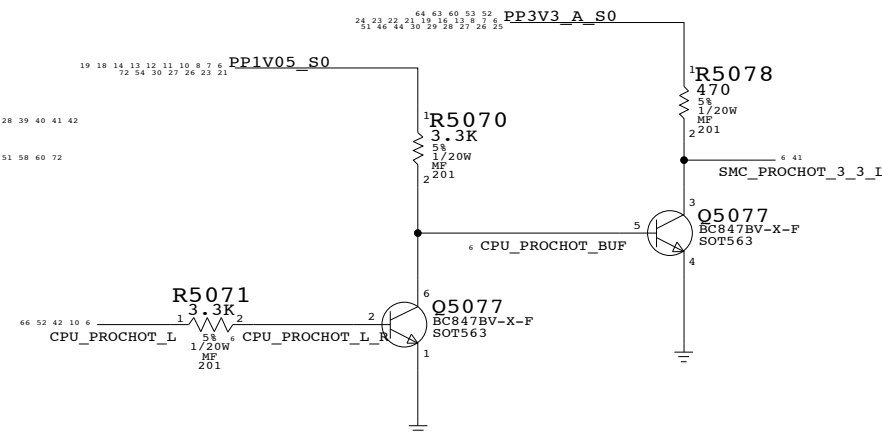
2

1

### SMC Reset Button / Brownout Detect



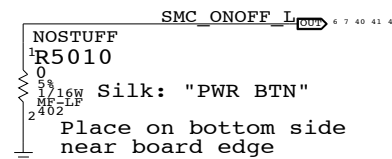
### SMC 1.05V to 3.3V Level Shifting



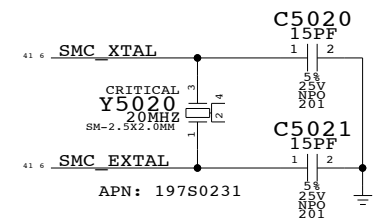
- 56 41 6 RSMRST\_PWRGD R5094 1 2 100K
- 42 41 40 7 6 SMC\_ONOFF\_L R5095 1 2 100K
- 43 41 39 6 SMC\_TX\_L R5080 1 2 10K
- 43 41 39 6 SMC\_RX\_L R5081 1 2 100K
- 43 41 6 SMC\_TMS R5097 1 2 10K
- 43 41 6 SMC\_TDO R5085 1 2 10K
- 43 41 6 SMC\_TDI R5086 1 2 10K
- 43 41 6 SMC\_TCK R5087 1 2 10K
- 43 41 6 PM\_LAN\_PWRGD R5090 1 2 10K
- 41 6 SMC\_PF3 R5091 1 2 10K
- 50 41 7 6 SYS\_ONEWIRE R5082 1 2 2.0K
- 50 42 41 7 6 SMC\_BS\_ALRT\_L R5083 1 2 470K
- 41 6 SMC\_ODD\_DETECT R5049 1 2 10K
- 59 50 41 6 SMC\_BC\_ACOK R5084 1 2 10K
- 41 40 7 6 SMC\_LID R5073 1 2 100K

- R5006 1 2 100K PM\_SLP\_S5\_L 6 25 41
- R5092 1 2 10K SMC\_CASE\_OPEN 6 41
- R5096 1 2 10K SMC\_ADAPTER\_EN 6 9 36 41
- R5093 1 2 10K SMC\_BATT\_CHG\_EN 6 41

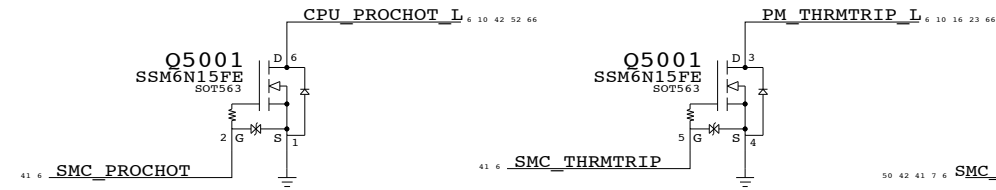
### Debug Power Button



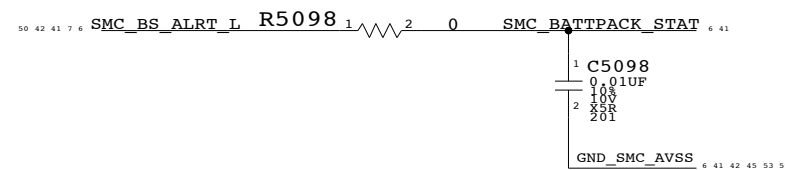
### SMC Crystal Circuit



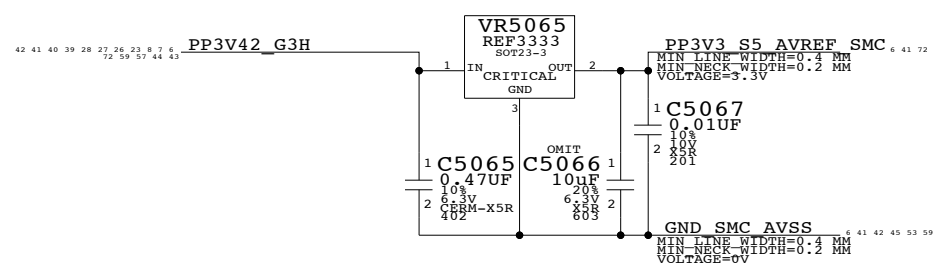
### SMC 3.3V to 1.05V Level Shifting



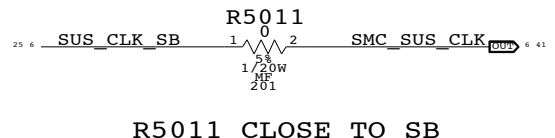
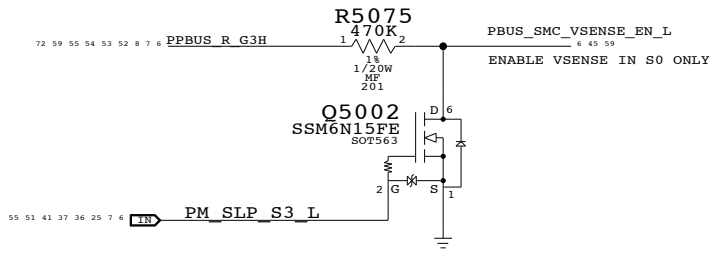
### Battery Pack Status



### SMC AVREF Supply



### 3.3V TO PBUS LEVEL SHIFTING



**SMC SUPPORT**

SYNC\_MASTER=M70      SYNC\_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		42	73

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

5

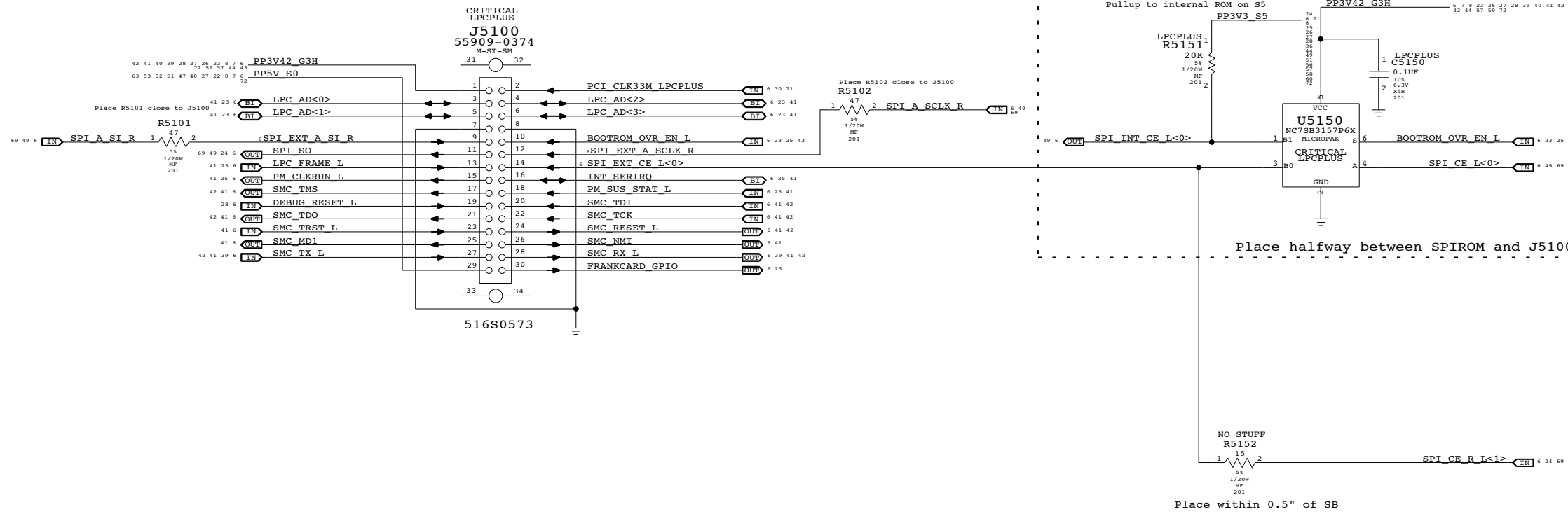
4

3

2

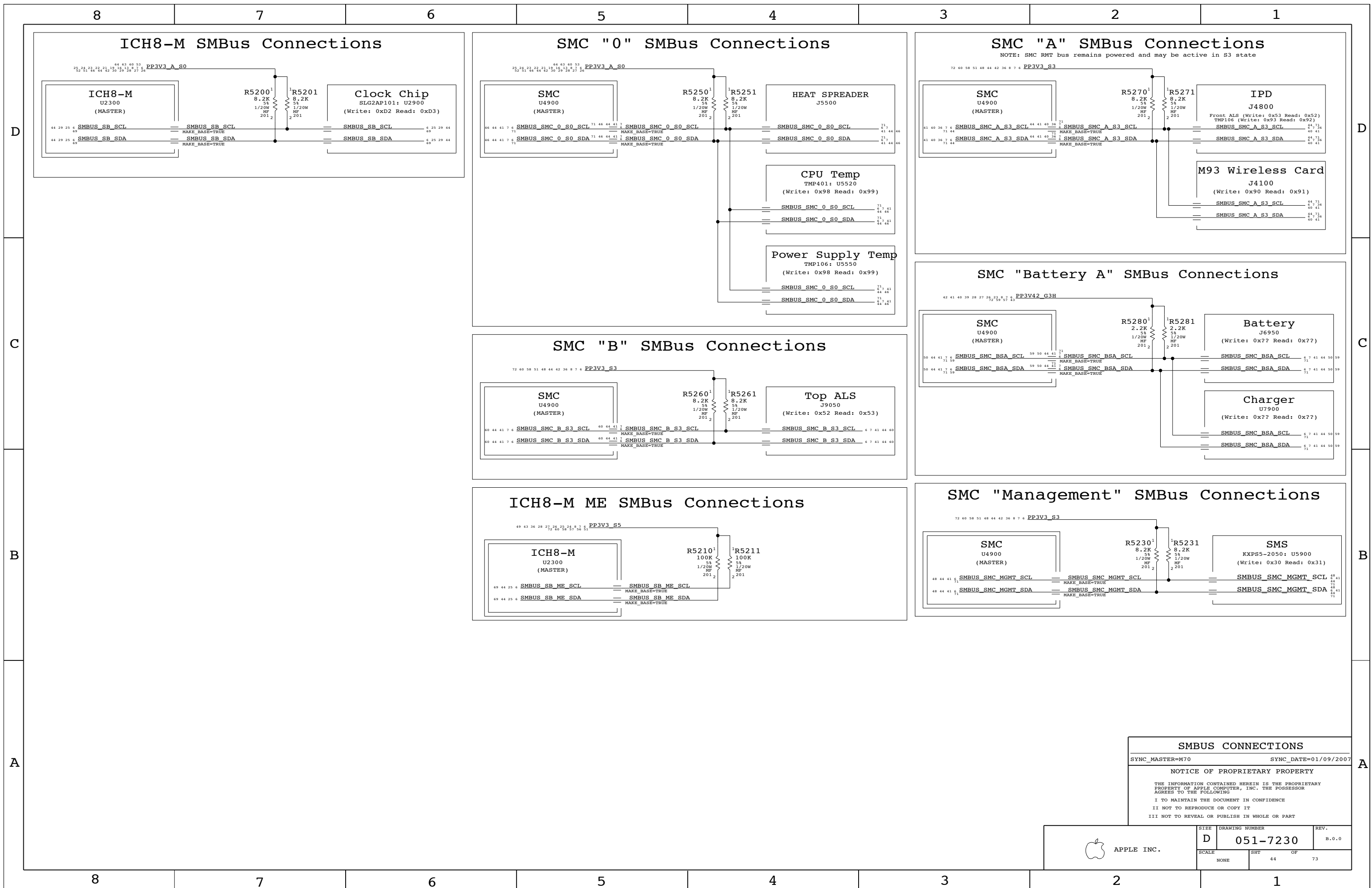
1

# LPC+SPI Connector



**LPC+SPI Debug Connector**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		43	73



**SMBUS CONNECTIONS**

SYNC\_MASTER=M70      SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		
NONE	44 OF 73		

8

7

6

5

4

3

2

1

D

D

C

C

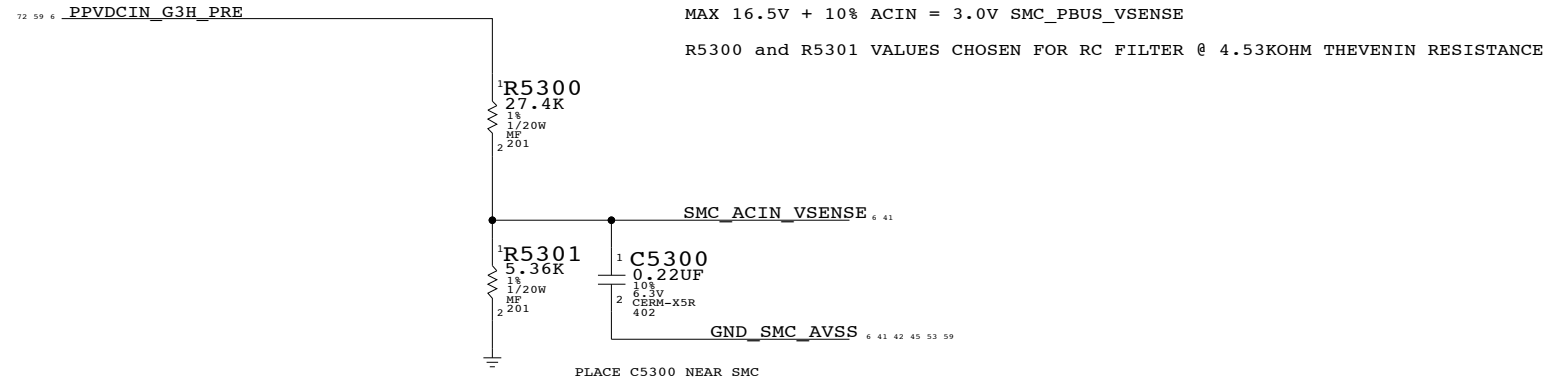
B

B

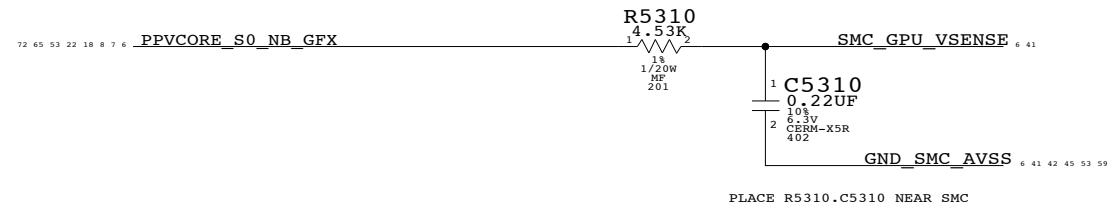
A

A

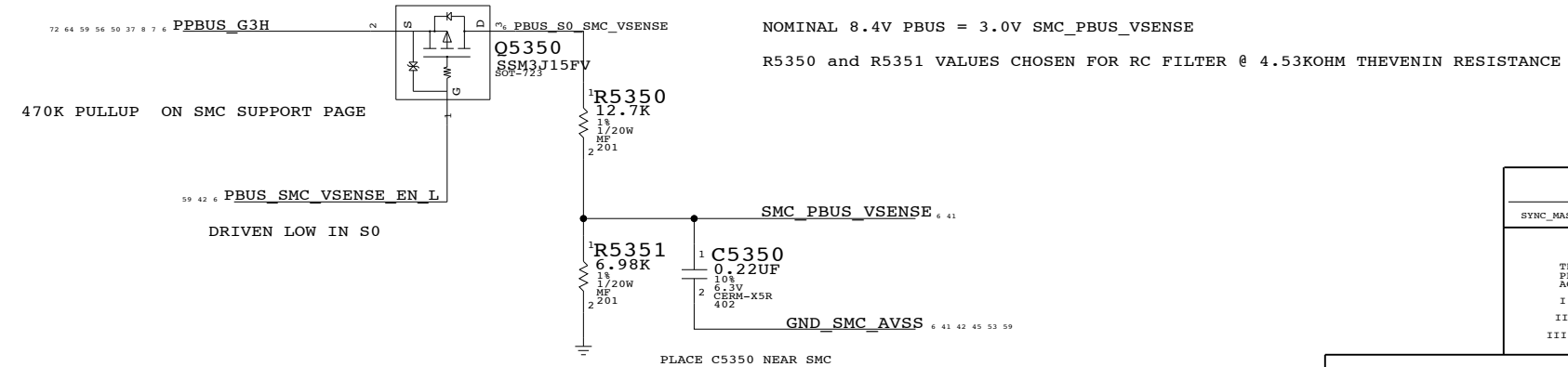
### ACIN VOLTAGE SENSE



### GPU VOLTAGE SENSE



### PBUS VOLTAGE SENSE



#### Voltage Sensors

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

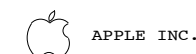
#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF	73
NONE	45		

8

7

6

5

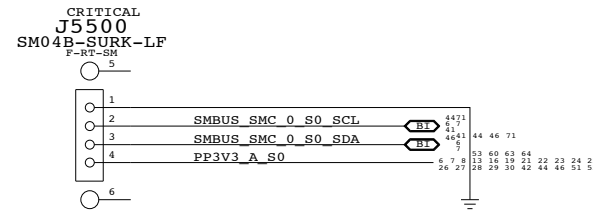
4

3

2

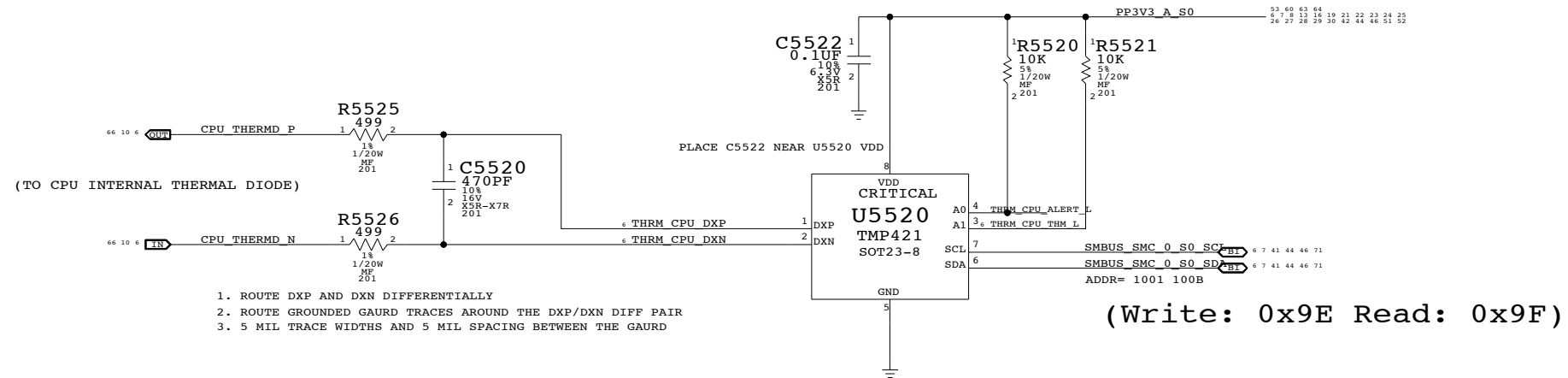
1

### REMOTE TEMP AT HEAT SPREADER

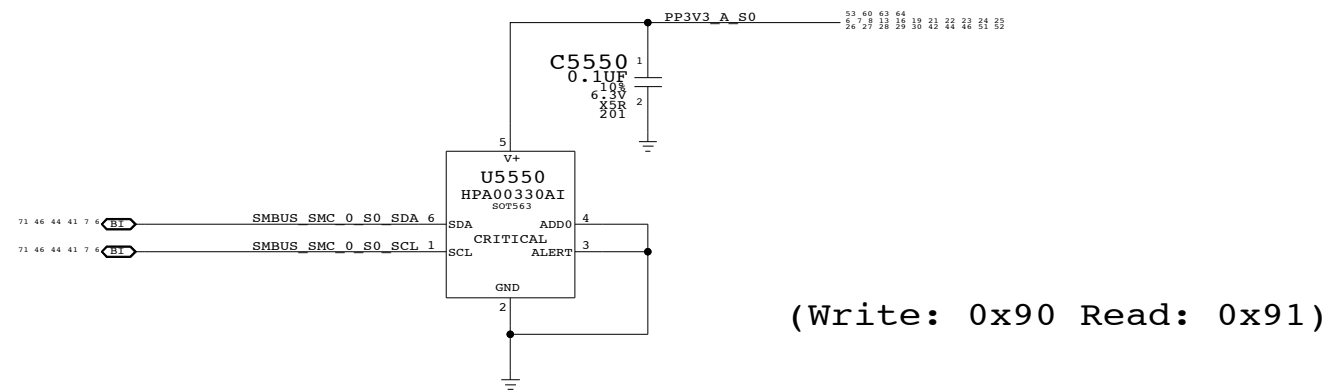


APN: 518S0354

### CPU THERMAL DIODE



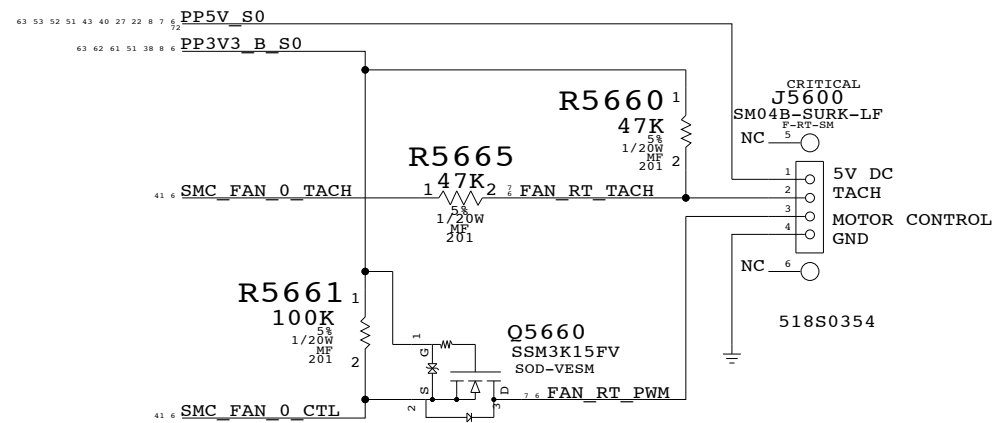
### LOCAL TEMP NEAR POWER SUPPLIES



**TEMPERATURE SENSORS**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		
NONE	46 OF 73		

# FAN CONNECTOR

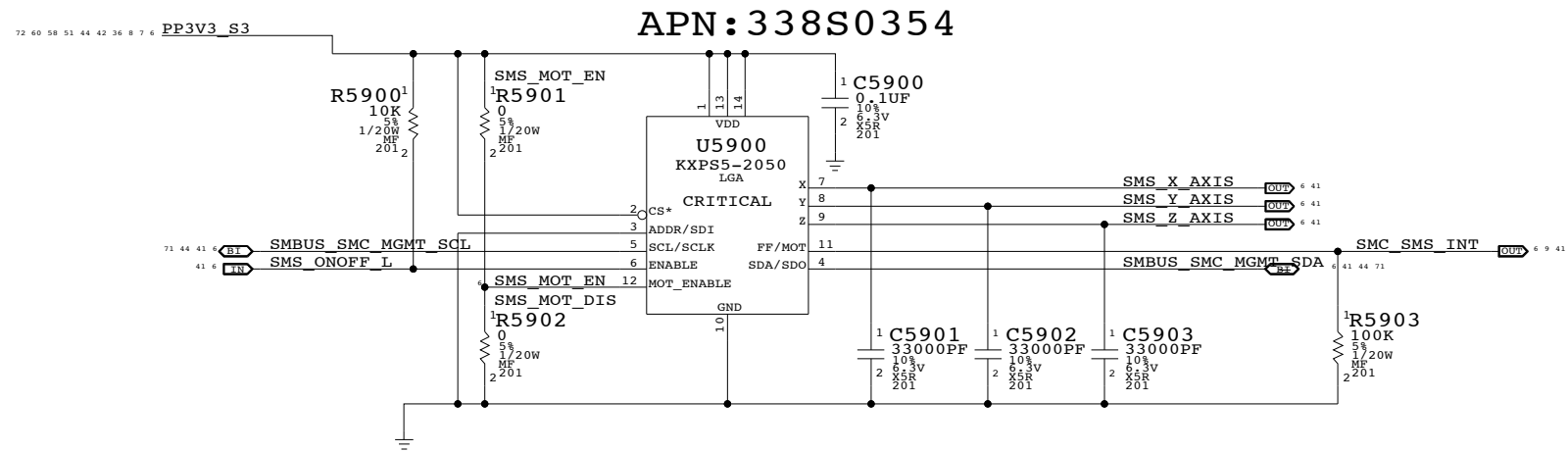


**Fan**

SYNC\_MASTER=M70      SYNC\_DATE=01/09/2007  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		
NONE	47	73	

# SUDDEN MOTION SENSOR



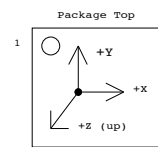
## I2C addresses:

ADDR low => 0x30, 0x31

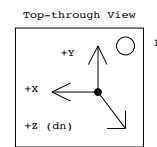
ADDR high => 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



## Sudden Motion Sensor (SMS)

SYNC\_MASTER=076\_MLS SYNC\_DATE=01/12/2007

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

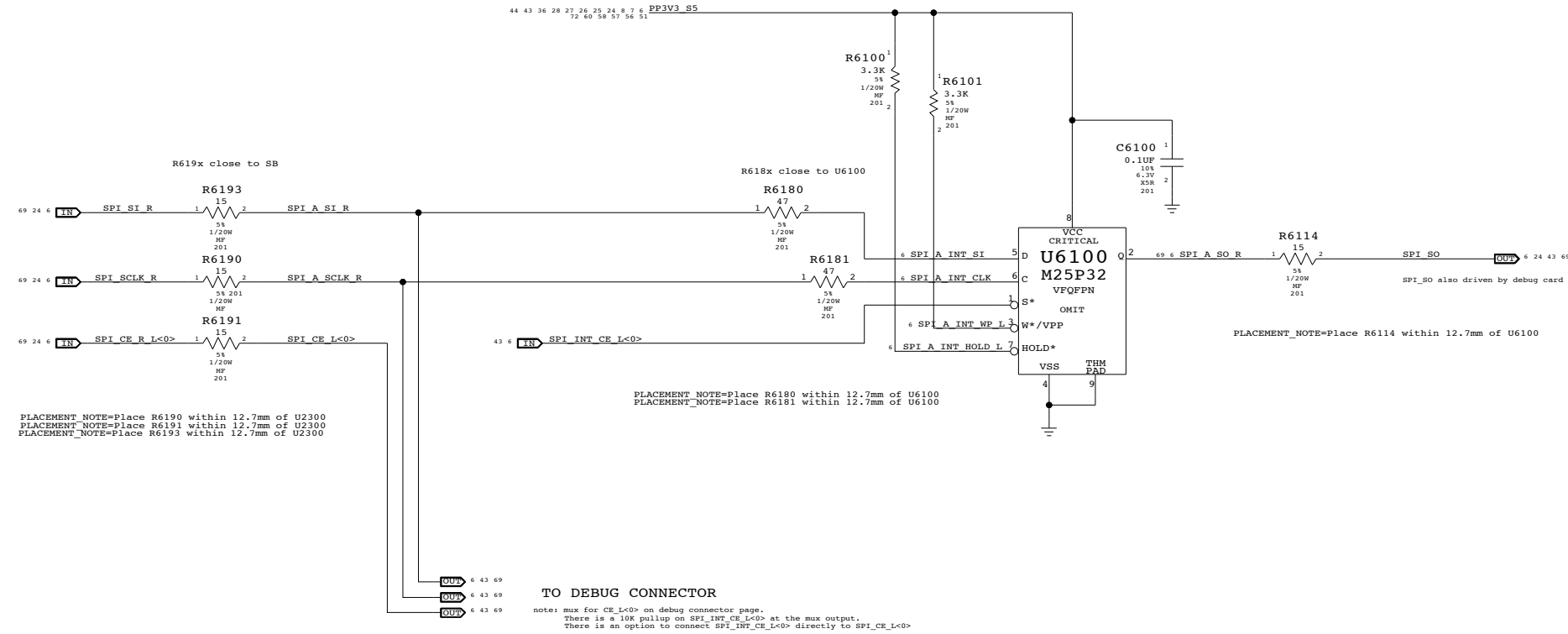
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	48	73



# SPI ROM



**SPI ROMs**

SYNC\_MASTER=WFERRY SYNC\_DATE=04/26/2006

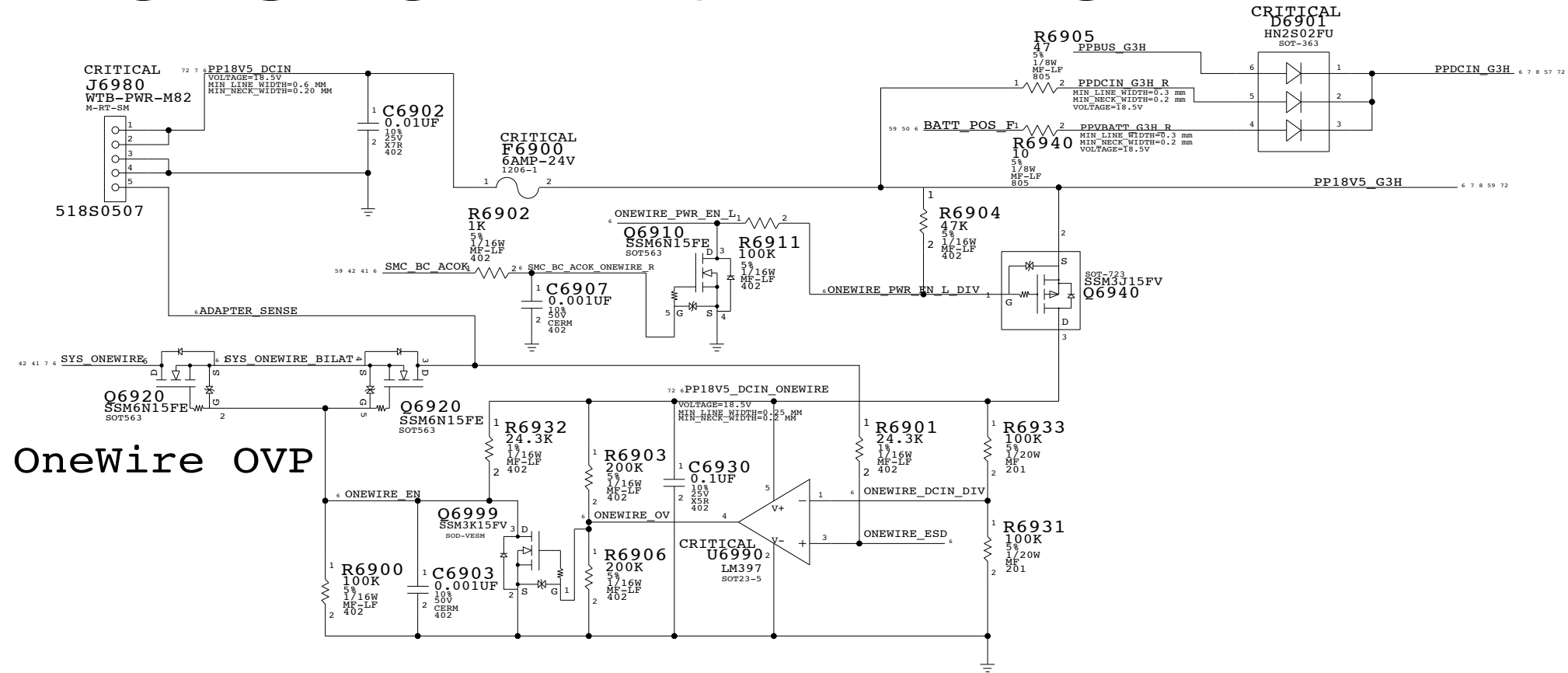
**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

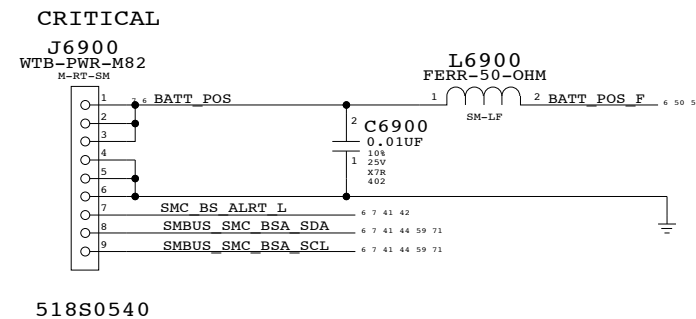
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		
NONE	49 OF 73		

# DC-JACK INTERFACE



# BATTERY INTERFACE



DC-In & Battery Connectors  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

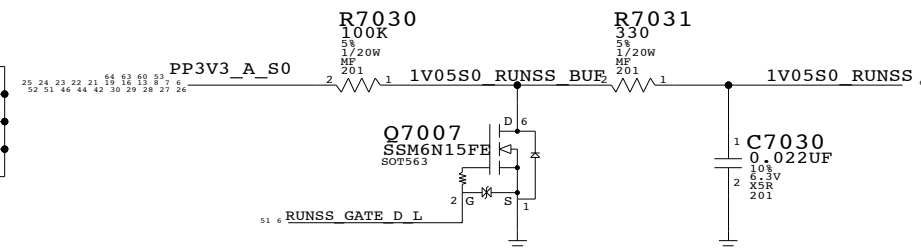
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

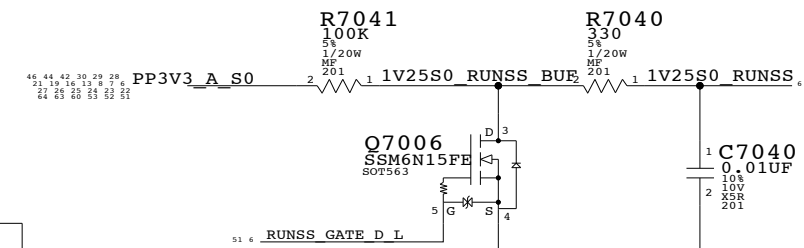
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		
NONE	50 OF		73

# S0 FETS & POWER SEQUENCING & PGOOD

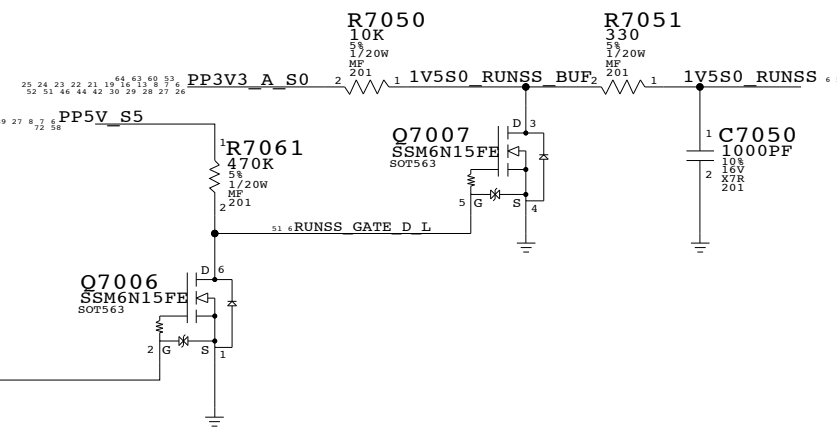
## 1.05V S0 RUN/SS CONTROL



## 1.25V S0 RUN/SS CONTROL



## 1.5V S0 RUN/SS CONTROL



## 3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.063 A

## 3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	.776 A

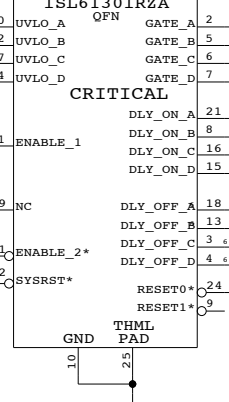
## 1.8V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.120 A

## 5V S0 FET

MOSFET	FDM6296
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @4.5V
LOADING	4.061 A

## PGOOD SEQUENCER



DEASSERTED 160MS  
AFTER UVLO\_D VALID

PGOOD SEQUENCER

PGOOD 1V05S0

PGOOD 1V5S0

NO STUFF  
R7013

NO STUFF  
R7014

PGOOD 1V25S0

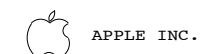
STUFF R7013, R7014 and UNSTUFF U7002, C7001, C7002  
TO USE WIRE-AND OF ALL PGOODs INSTEAD OF TPS3808

## S0 FETS & Power Sequencing

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

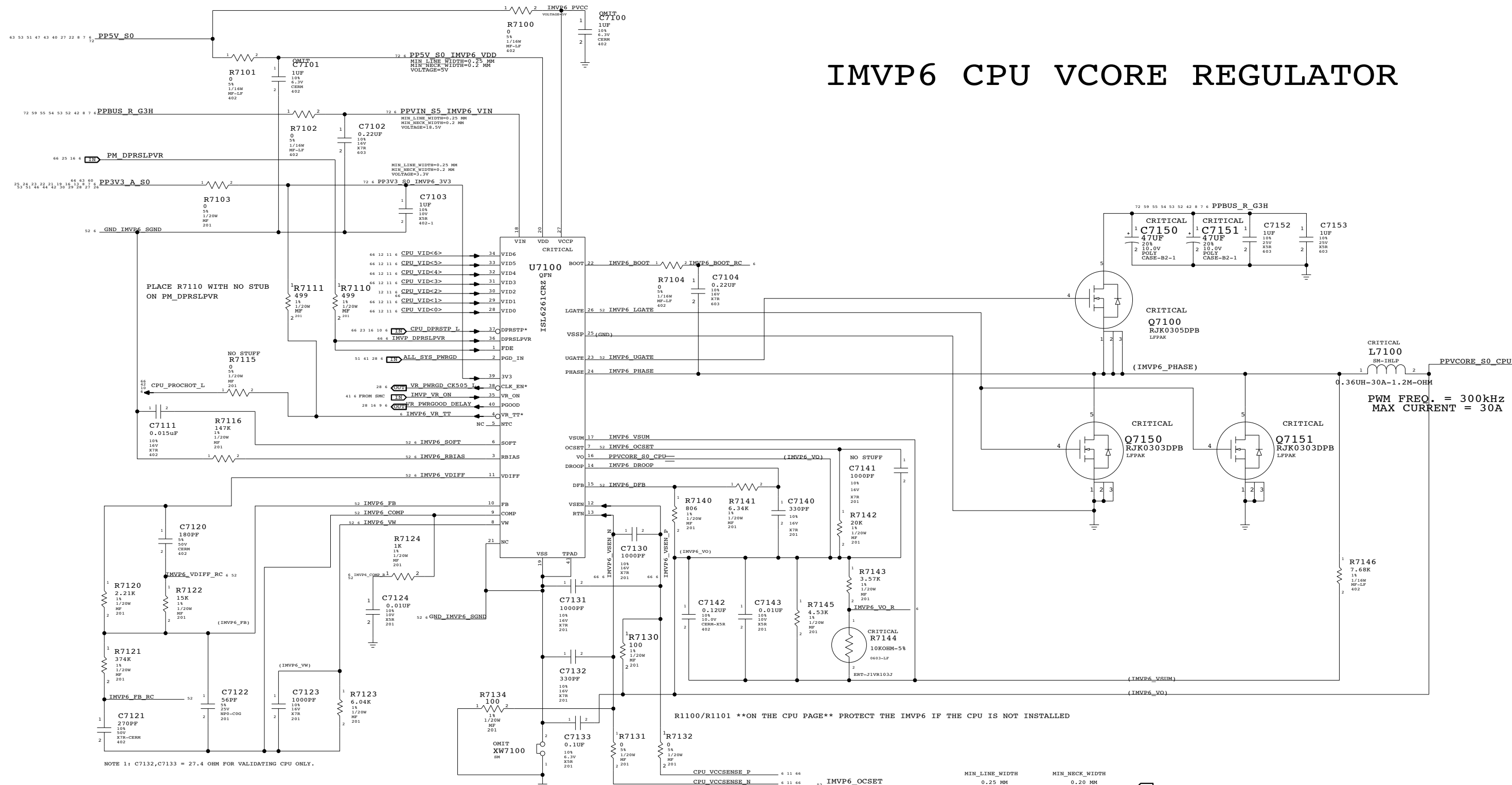
### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	D	DRAWING NUMBER	051-7230	REV.	B.0.0
SCALE	NONE	SHT	51	OF	73

# IMVP6 CPU VCore Regulator



NOTE 1: C7132, C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 \*\*ON THE CPU PAGE\*\* PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
52 4 IMVP6 PHASE	1.5 MM	0.20 MM
52 4 IMVP6 BOOT	0.25 MM	0.20 MM
52 4 IMVP6 UGATE	1.5 MM	0.20 MM
52 4 IMVP6 LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
52 IMVP6_OCSET	0.25 MM	0.20 MM
52 IMVP6_VSUM	0.25 MM	0.20 MM
52 GND_IMVP6_SGND	0.50 MM	0.20 MM
52 PPVCORE_S0_CPU	0.25 MM	0.20 MM
52 IMVP6_DROOP	0.25 MM	0.20 MM
52 IMVP6_DFB	0.25 MM	0.20 MM
52 IMVP6_SOFT	0.25 MM	0.20 MM
52 IMVP6_RBIAS	0.25 MM	0.20 MM
52 IMVP6_VDIFF	0.25 MM	0.20 MM
52 IMVP6_FB	0.25 MM	0.20 MM
52 IMVP6_COMP	0.25 MM	0.20 MM
52 IMVP6_VW	0.25 MM	0.20 MM
52 IMVP6_PVCC	0.25 MM	0.20 MM
52 IMVP6_COMP_R	0.25 MM	0.20 MM
52 IMVP6_COMP_RC	0.25 MM	0.20 MM
52 IMVP6_FB_RC	0.25 MM	0.20 MM
52 IMVP6_VDIFF_RC	0.25 MM	0.20 MM

## IMVP6 CPU VCore Regulator

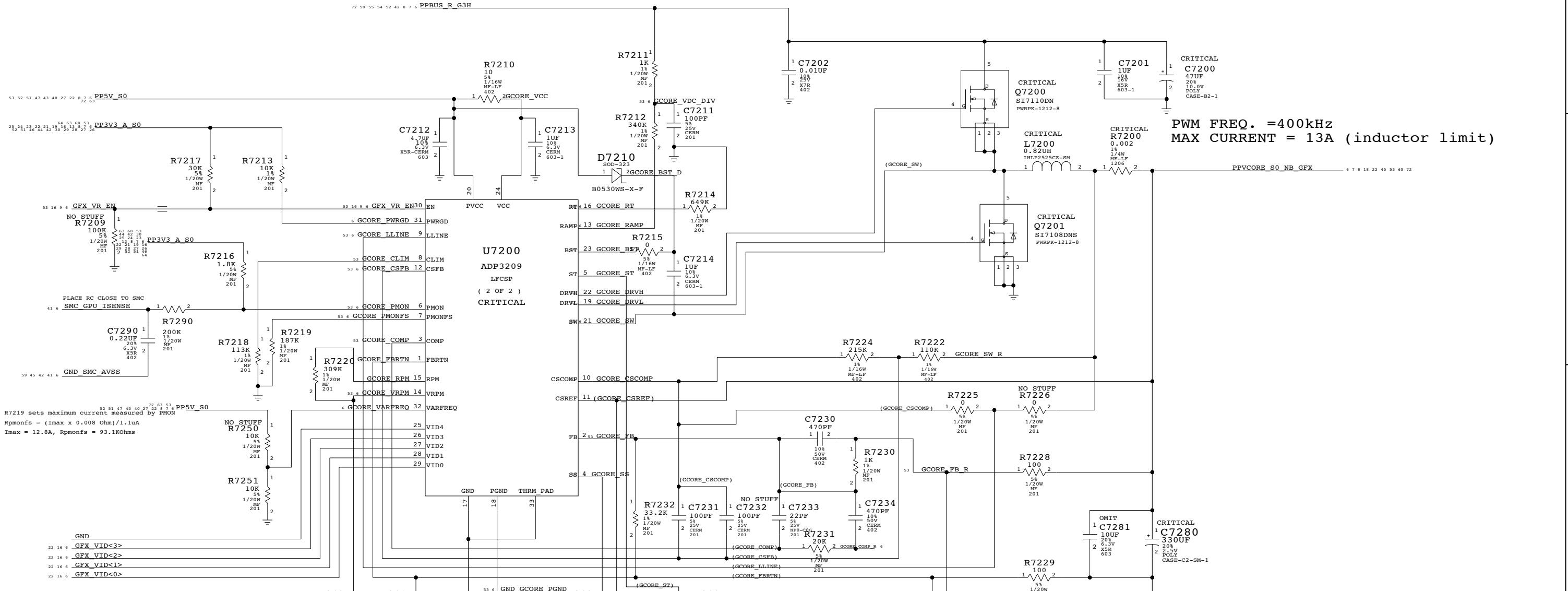
SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		52	73

# RENDER VCORE POWER SUPPLY



PWM FREQ. = 400kHz  
MAX CURRENT = 13A (inductor limit)

ROUTE AS DIFF PAIR TO NB GFX VCC AND GND FOR REMOTE SENSING

NOTE: VID<4> is tied to GND

VID	4	3	2	1	0	VOLTAGE
VID	0	0	0	0	0	1.250V
VID	0	0	0	0	1	1.225V
VID	0	0	0	1	0	1.200V
VID	0	0	0	1	1	1.175V
VID	0	0	1	0	0	1.150V
VID	0	0	1	0	1	1.125V
VID	0	1	0	0	0	1.100V
VID	0	1	0	1	1	1.075V
VID	0	1	0	0	0	1.050V
VID	0	1	0	1	1	1.025V
VID	0	1	1	0	0	1.000V
VID	0	1	1	0	1	0.975V
VID	0	1	1	1	0	0.950V
VID	0	1	1	1	1	0.925V
VID	1	1	1	0	0	0.900V
VID	1	1	1	1	1	0.875V

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GCORE SW	0.6 MM	0.20 MM
GCORE BST	0.3 MM	0.20 MM
GCORE DRVH	0.6 MM	0.20 MM
GCORE DRVL	0.6 MM	0.20 MM
GCORE BST D	0.3 MM	0.20 MM
GND GCORE PGND	0.6 MM	0.20 MM
GCORE VDC DIV	0.3 MM	0.20 MM
GCORE RAMP	0.3 MM	0.20 MM
GCORE CLIM	0.3 MM	0.20 MM
GCORE SS	0.3 MM	0.20 MM
GCORE ST	0.3 MM	0.20 MM
GCORE SW R	0.6 MM	0.20 MM

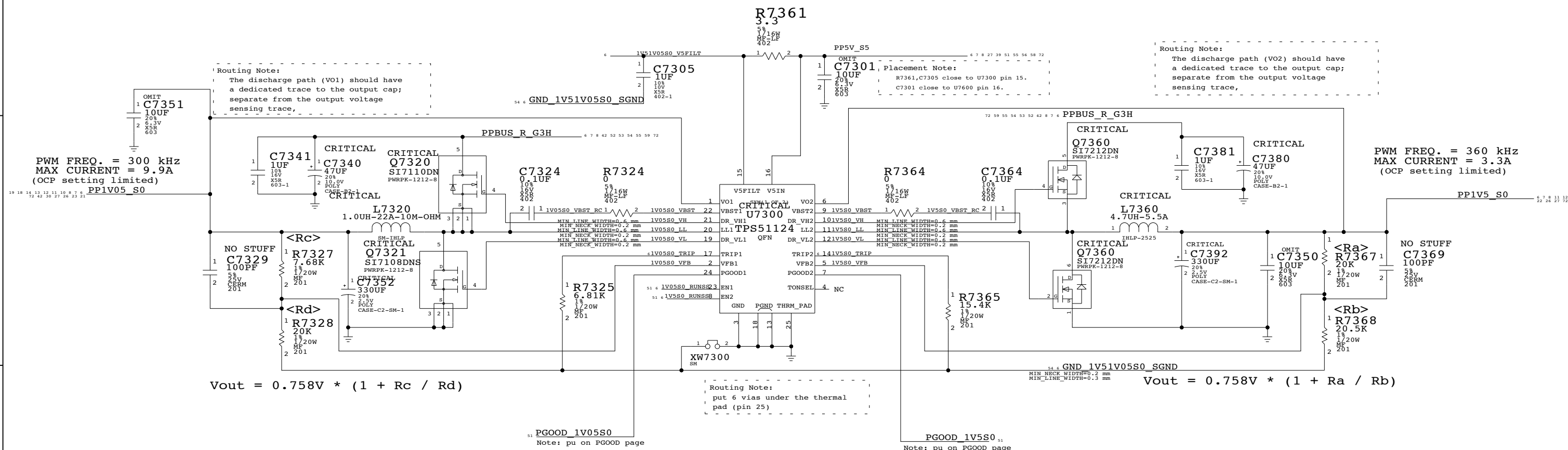
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GCORE CSCOMP	0.3 MM	0.20 MM
GCORE CSFB	0.3 MM	0.20 MM
GCORE LLINE	0.3 MM	0.20 MM
GCORE RT	0.3 MM	0.20 MM
GFX VR EN	0.3 MM	0.20 MM
GCORE COMP	0.3 MM	0.20 MM
GCORE FB	0.3 MM	0.20 MM
GCORE FBRTN	0.3 MM	0.20 MM
GCORE PMON	0.3 MM	0.20 MM
GCORE PMONFS	0.3 MM	0.20 MM
GCORE RPM	0.3 MM	0.20 MM
GCORE VRPM	0.3 MM	0.20 MM
GCORE FB R	0.3 MM	0.20 MM

**Render VCore Supplies**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE		53	

# 1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



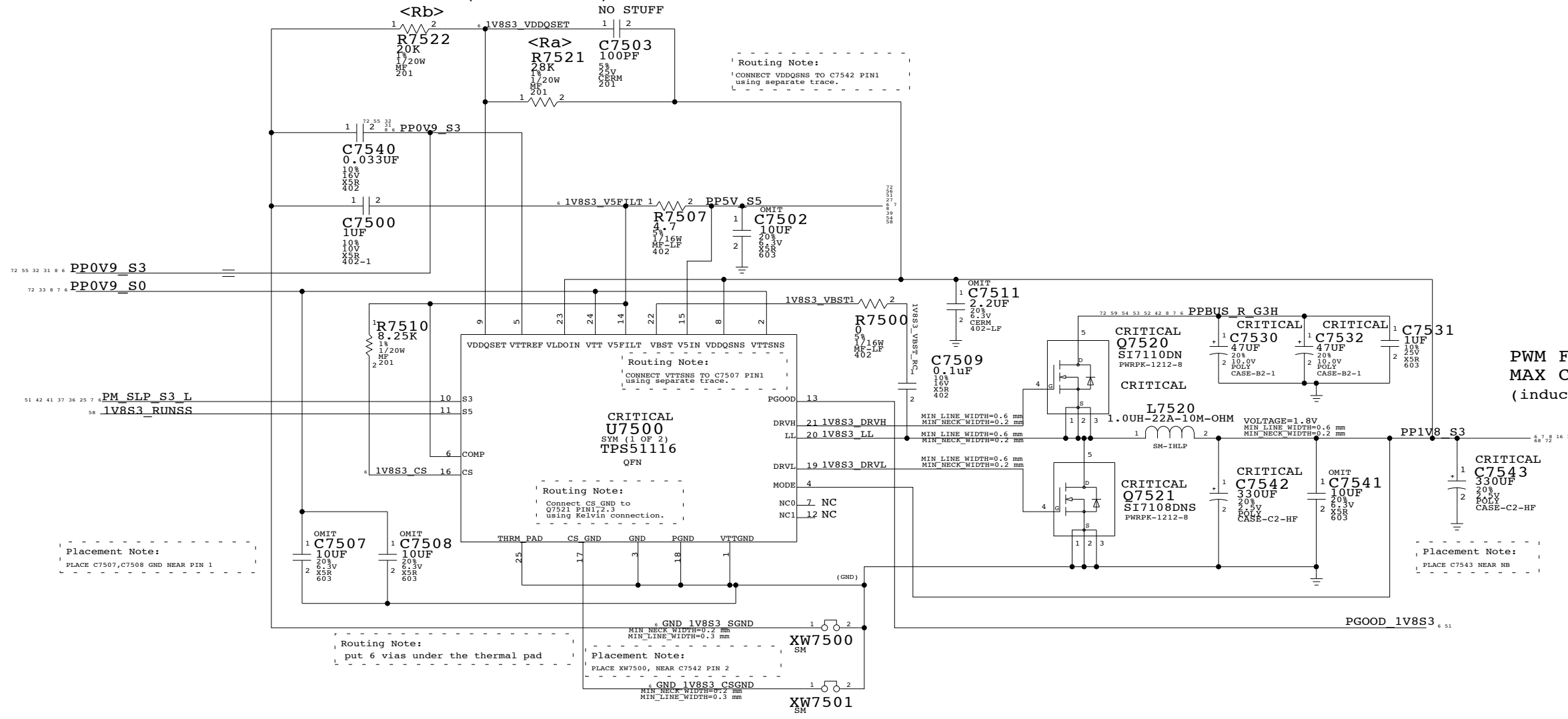
**1.5V/1.05V Supplies**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		54	73

# 1.8V/0.9V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V

$$V_{out} = 0.75V * (1 + R_a / R_b)$$



PWM FREQ. = 400 kHz  
MAX CURRENT = 11A  
(inductor limited)

**1.8V/0.9V Supplies**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	55		

# 5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

$$V_{out} = 1V * (1 + R_a / R_b)$$

$$5.106V = 1V * (1 + 20K / 4.87K)$$

<Ra>      <Rb>

R7667      R7668

20K      4.87K

NO STUFF      1/20W

C7667      MF

100PF      201

Routing Note:  
The discharge path (VO1) should have a dedicated trace to the output cap;

Routing Note:  
The discharge path (VO2) should have a dedicated trace to the output cap; separate from the output voltage sensing trace,

Routing Note:  
put 6 vias under the thermal pad (pin 33)

PWM FREQ. = 280 kHz  
MAX CURRENT = 6.0A  
(inductor limited)

PWM FREQ. = 430 kHz  
MAX CURRENT = 7.8A  
(OCP setting limited)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682, C7680	KEMET T520V336M016AT045760
128S0093	128S0092	?	C7640	KEMET T520V336M016AT045760

Placement Note:  
R7601, C7605 close to U7600 pin 20.  
C7602 close to U7600 pin 22.  
C7604 close to U7600 pin 21.  
C7603 close to U7600 pin 19.  
R7605, R7603 close to U7600.

**5V/3.3V Supplies**  
 SYNC\_MASTER=M70      SYNC\_DATE=02/01/2007

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

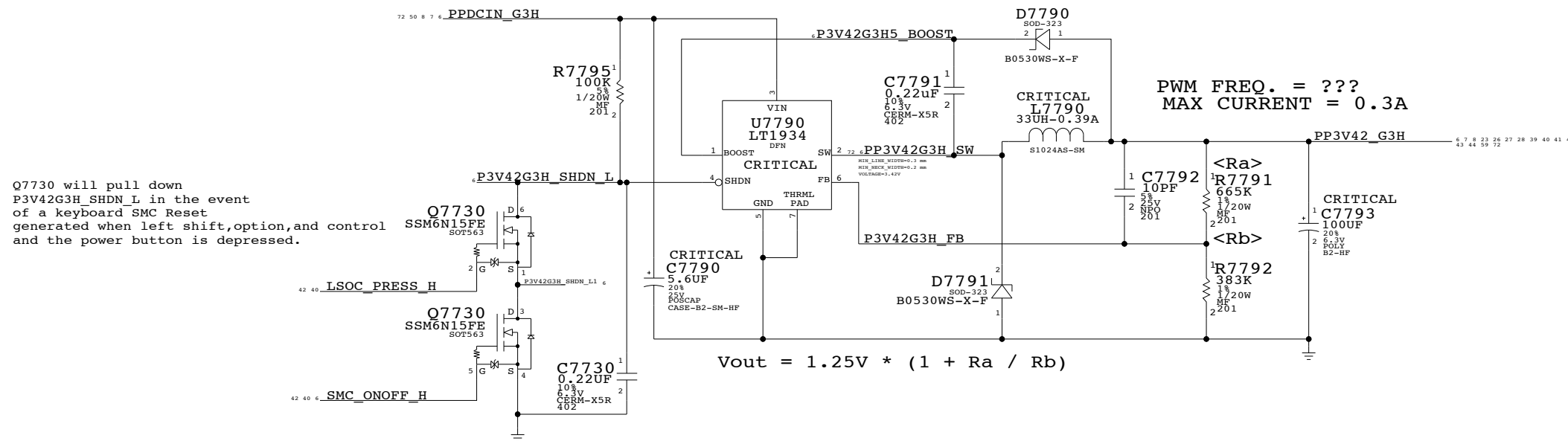
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	56	73



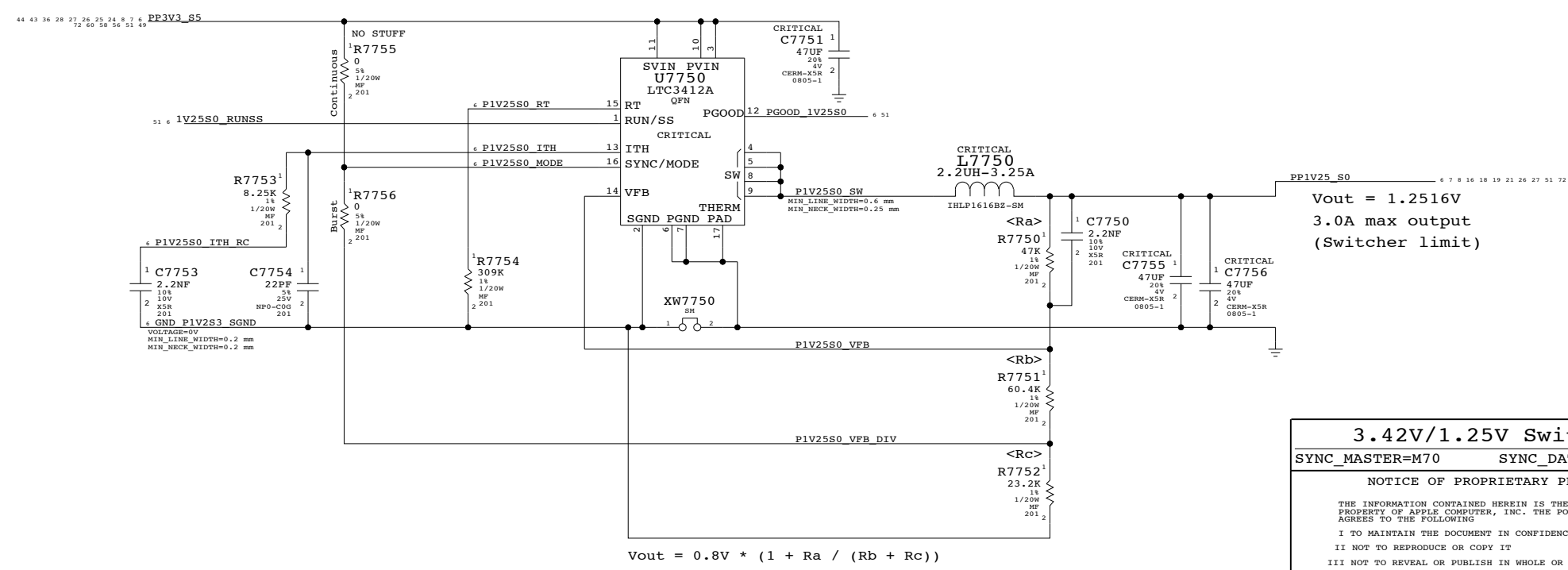
# 3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Q7730 will pull down P3V42G3H\_SHDN\_L in the event of a keyboard SMC Reset generated when left shift, option, and control and the power button is depressed.

# 1.25V S0 REGULATOR



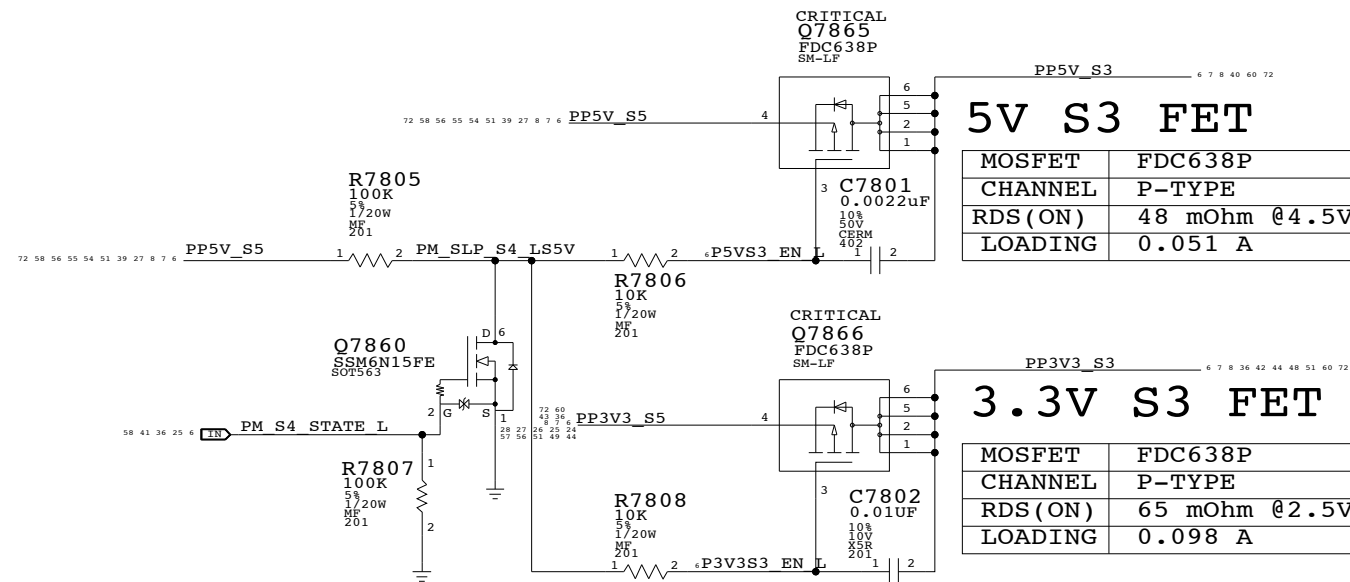
**3.42V/1.25V Switcher**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT OF		73
NONE	57		

# S3 FETS & S3/S5 CONTROL

## 5V/3.3V S5 RUN/SS CONTROL

## 1.8V S3 RUN/SS CONTROL



**5V S3 FET**

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

**3.3V S3 FET**

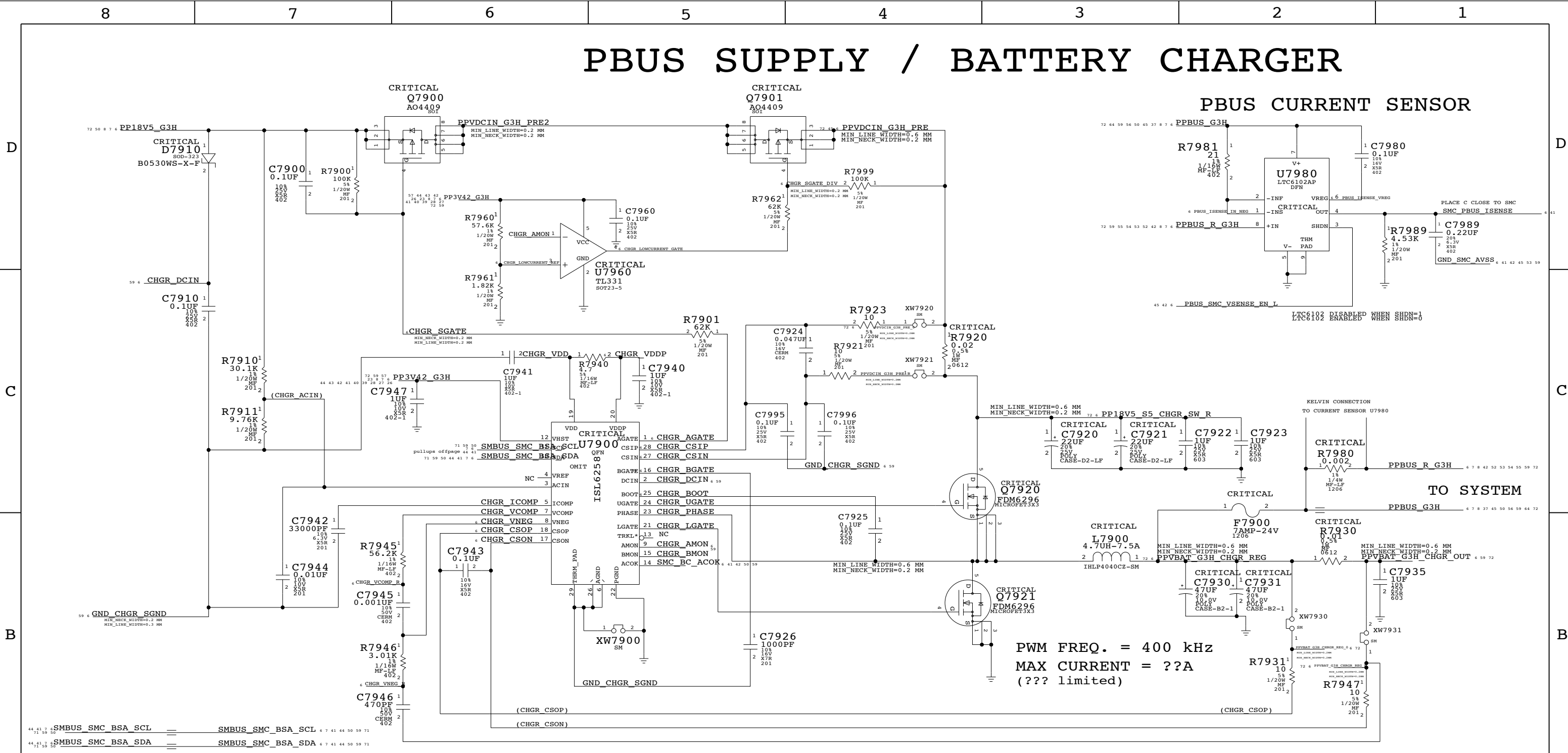
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

**S3 FET & S3/S5 Control**  
 SYNC\_MASTER=M70 SYNC\_DATE=02/01/2007

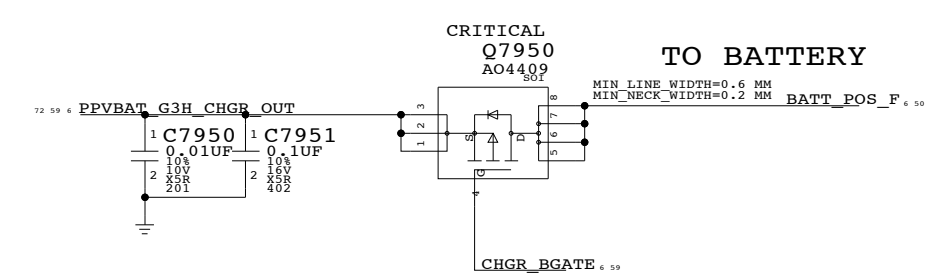
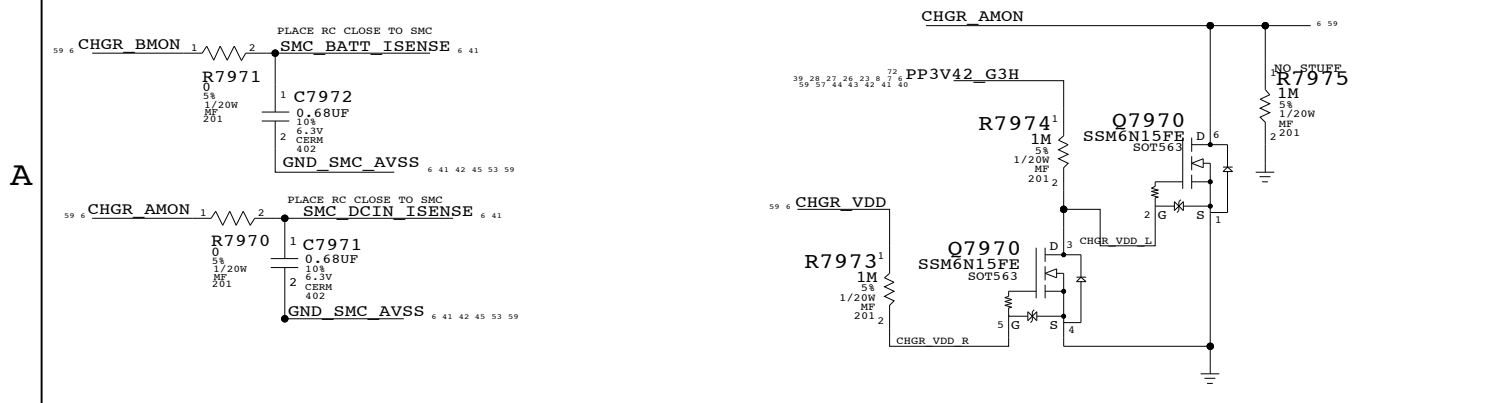
NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	NONE	SHT	OF
		58	73

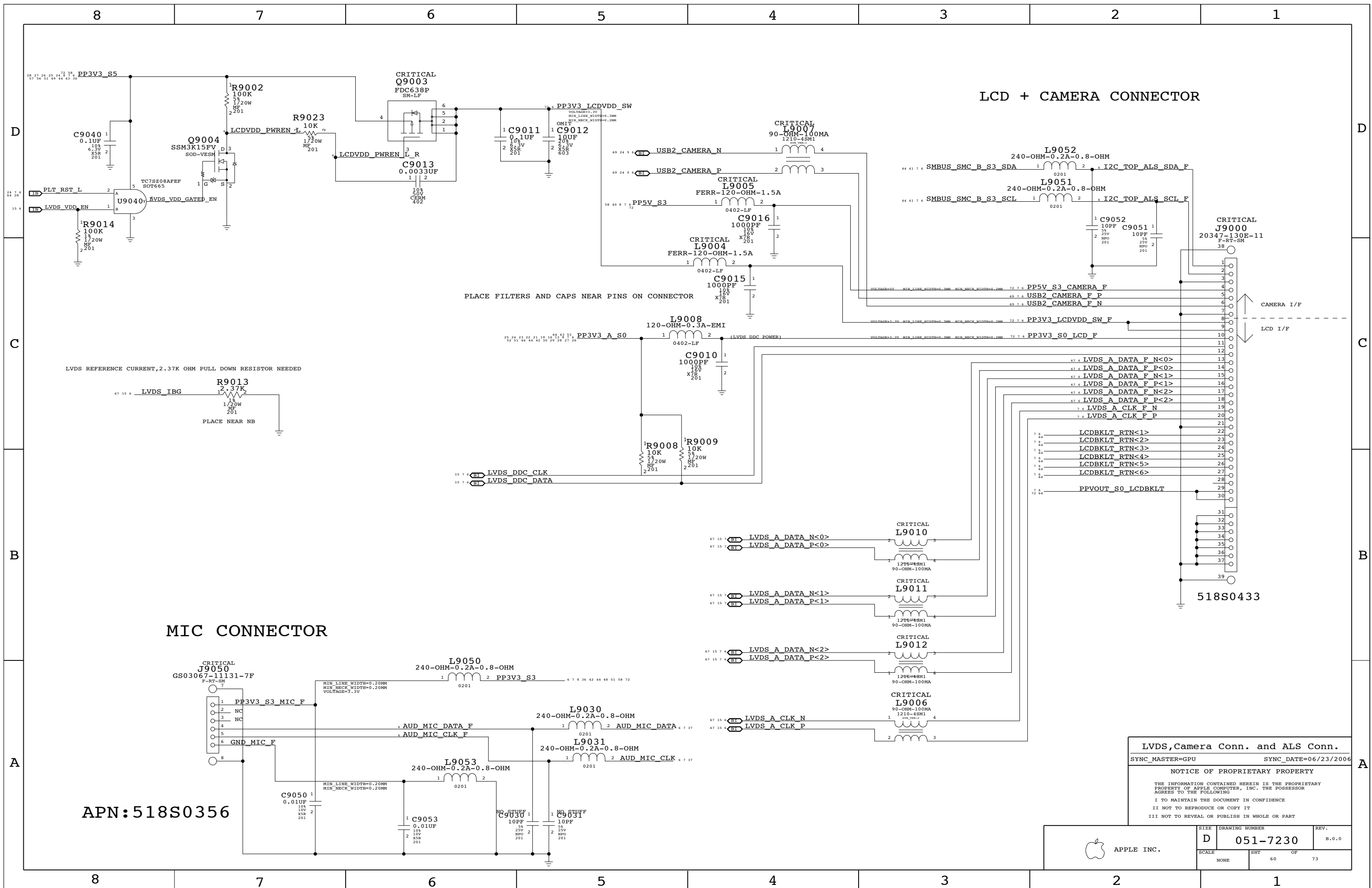
# PBUS SUPPLY / BATTERY CHARGER



## AMON PULLDOWN LOGIC



APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	59		



LCD + CAMERA CONNECTOR

PLACE FILTERS AND CAPS NEAR PINS ON CONNECTOR

LVDS REFERENCE CURRENT, 2.37K OHM PULL DOWN RESISTOR NEEDED

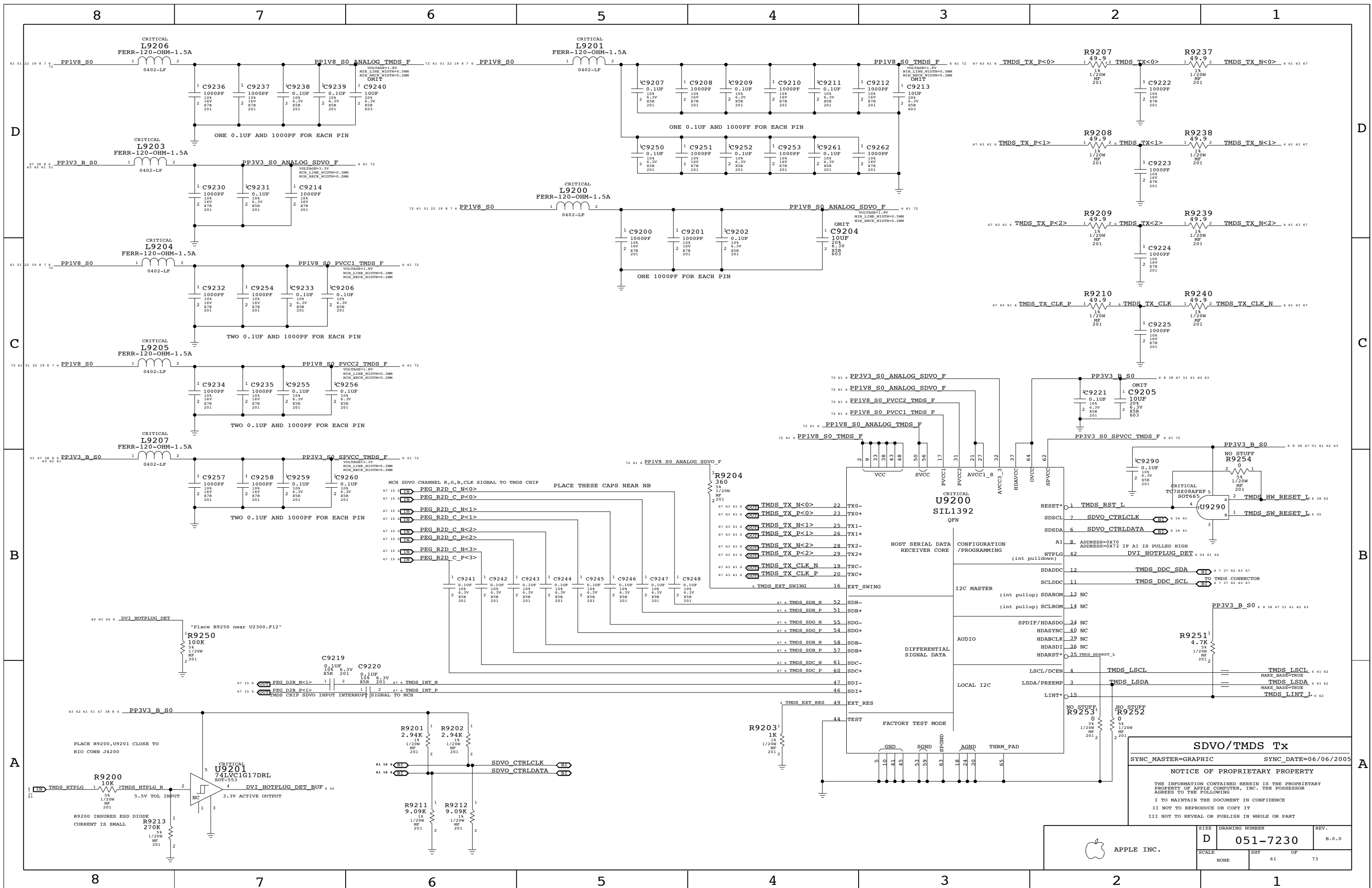
PLACE NEAR NB

MIC CONNECTOR

APN: 518S0356

LVDS, Camera Conn. and ALS Conn.  
 SYNC\_MASTER=GPU SYNC\_DATE=06/23/2006  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT		OF
NONE	60		73

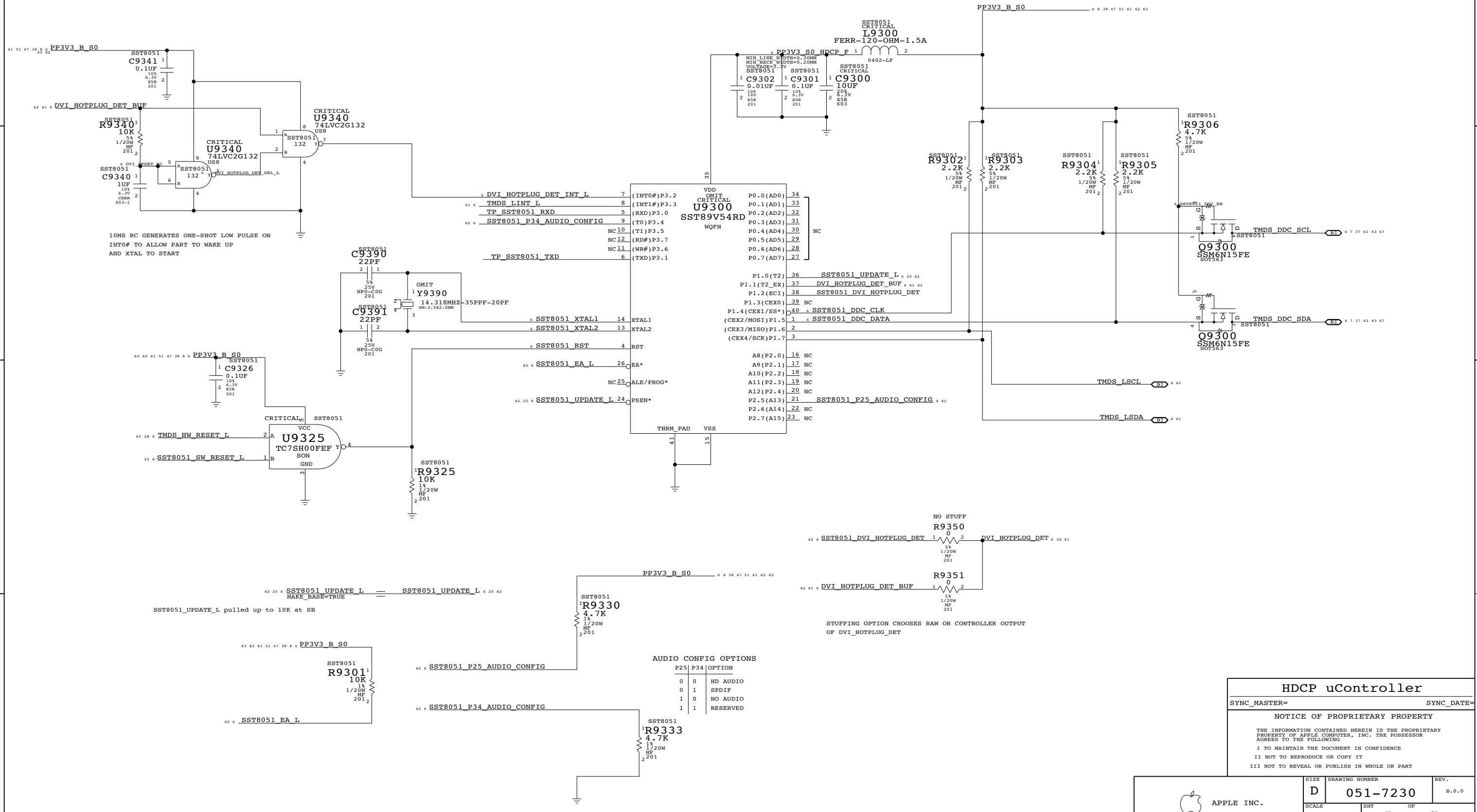


**SDVO/TMSD Tx**  
 SYNC\_MASTER=GRAPHIC SYNC\_DATE=06/06/2005

**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	61		

# SST8051 microcontroller for HDCP support



AUDIO CONFIG OPTIONS

P25	P34	OPTION
0	0	HD AUDIO
0	1	SPDIF
1	0	NO AUDIO
1	1	RESERVED

**HDCP uController**

SYNC\_MASTER= \_\_\_\_\_ SYNC\_DATE= \_\_\_\_\_

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

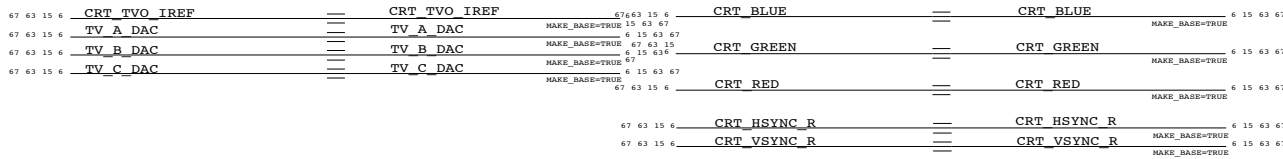
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7230	B.0.0
SHEET		OF	
62		73	

NB VIDEO ALIASES

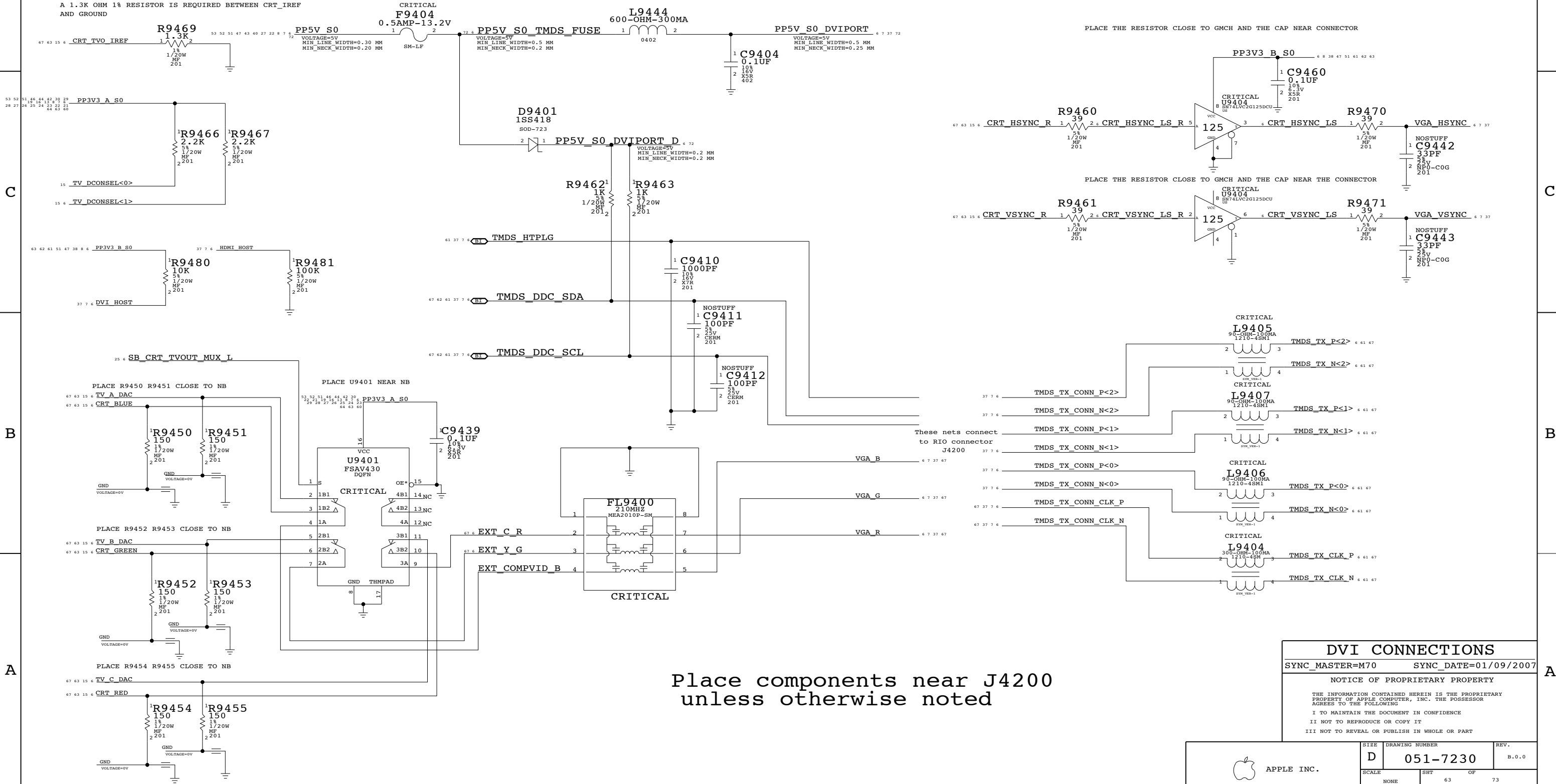


Video Connectors

TMD5(MICRO DVI) INTERFACE  
EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT\_IREF AND GROUND



PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

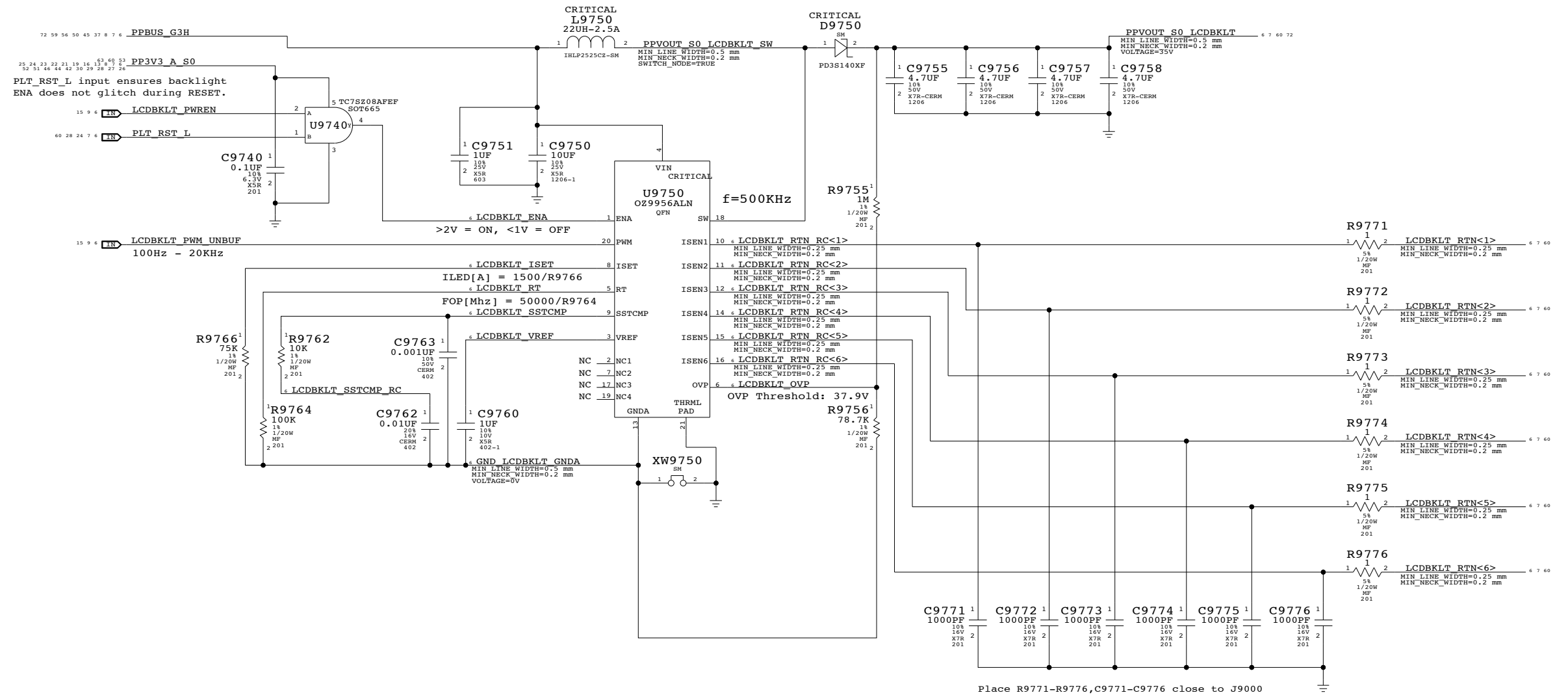
These nets connect to RIO connector J4200

Place components near J4200 unless otherwise noted

**DVI CONNECTIONS**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	63		

# LED Backlight Driver



## LED Backlight Driver

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE DRAWING NUMBER REV.

D 051-7230 B.0.0

SCALE NONE SHIT OF 73



8

7

6

5

4

3

2

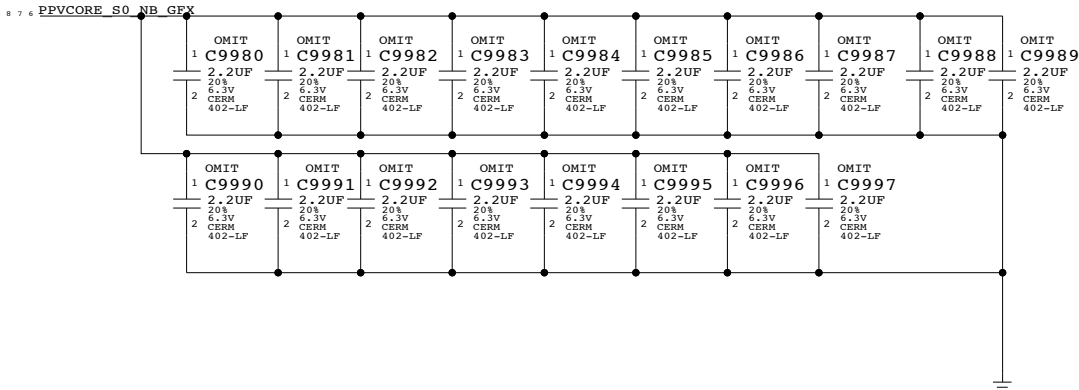
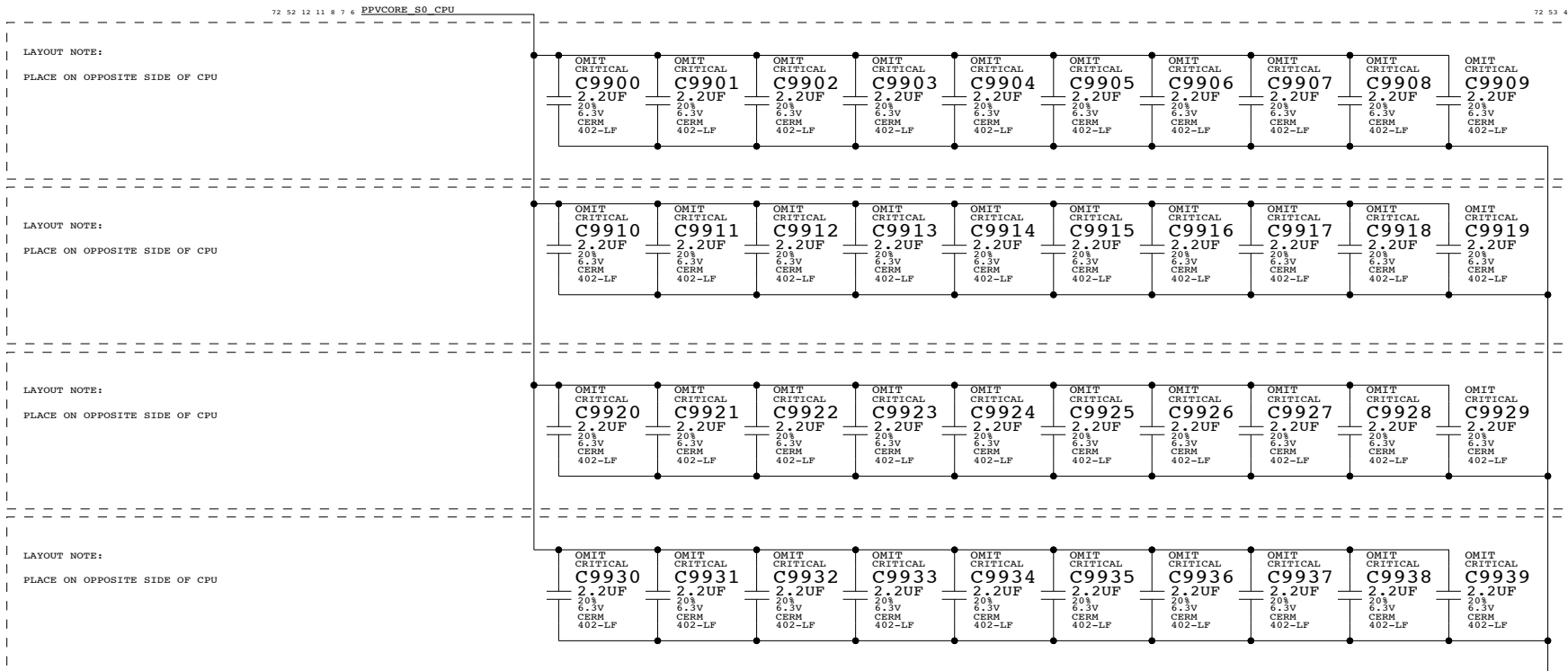
1

### ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

### ADDITIONAL GPU VCORE HF DECOUPLING

18x 1uF 0402



#### Additional CPU/GPU Decoupling

SYNC\_MASTER= SYNC\_DATE=

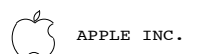
**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	65	73

8

7

6

5

4

3

2

1

**FSB (Front-Side Bus) Constraints**

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	ISL3, ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_4MIL	*	0.100 MM	?
FSB_9MIL	*	0.228 MM	?
FSB_DATA	*	=FSB_4MIL	?
FSB_DATA2DATA	*	=FSB_4MIL	?
FSB_DSTB	*	=FSB_9MIL	?
FSB_DATA2DSTB	*	=FSB_9MIL	?
FSB_ADDR	*	=FSB_4MIL	?
FSB_ADDR2ADDR	*	=FSB_4MIL	?
FSB_ADSTB	*	=FSB_9MIL	?
FSB_ADDR2ADSTB	*	=FSB_9MIL	?
FSB_COMMON	*	=FSB_4MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

**CPU Signal Constraints**

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?
CPU_THERMD	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

**CPU / FSB Net Properties**

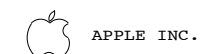
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0 L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK L
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS L<2..0>
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY L
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST L
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV L<0>
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV L<1>
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV L<2>
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV L<3>
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ L<4..0>
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>
CPU_IERR_L	CPU_55S		CPU_IERR L
CPU_FERR_L	CPU_55S		CPU_FERR L
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU_PROCHOT L
CPU_PWRGD	CPU_55S		CPU_PWRGD
CPU_INTR	CPU_55S		CPU_INTR
CPU_NMI	CPU_55S		CPU_NMI
CPU_A20M_L	CPU_55S		CPU_A20M L
CPU_DPSLP_L	CPU_55S		CPU_DPSLP L
CPU_IGNNE_L	CPU_55S		CPU_IGNNE L
CPU_INIT_L	CPU_55S		CPU_INIT L
CPU_SMI_L	CPU_55S		CPU_SMI L
CPU_STPCLK_L	CPU_55S		CPU_STPCLK L
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM_THRMTRIP L
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP L
PM_DPRSLEVR	CPU_55S	CPU_2T01	PM_DPRSLEVR
IMVP_DPRSLEVR	CPU_55S	CPU_2T01	IMVP_DPRSLEVR
CPU_BSEL0	CPU_55S	CPU_2T01	CPU_BSEL<0>
CPU_BSEL0	CPU_55S	CPU_2T01	NB_BSEL<0>
CPU_BSEL1	CPU_55S	CPU_2T01	CPU_BSEL<1>
CPU_BSEL1	CPU_55S	CPU_2T01	NB_BSEL<1>
CPU_BSEL2	CPU_55S	CPU_2T01	CPU_BSEL<2>
CPU_BSEL2	CPU_55S	CPU_2T01	NB_BSEL<2>
CPU_DPRSTP_L	CPU_55S	CPU_2T01	CPU_DPRSTP L
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST L
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>
CLK_FSB_100n	CLK_FSB_100n	CLK_FSB	XDP_CLK_P
CLK_FSB_100p	CLK_FSB_100p	CLK_FSB	XDP_CLK_N
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST L
CPU_VID<6..0>	CPU_55S	CPU_2T01	CPU_VID<6..0>
IMVP6_VID<6..0>	CPU_55S	CPU_2T01	IMVP6_VID<6..0>
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N
IMVP6_VSEN_P	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P
IMVP6_VSEN_N	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N
CPU_THERMD_P	CPU_70D	CPU_THERMD	CPU_THERMD_P
CPU_THERMD_N	CPU_70D	CPU_THERMD	CPU_THERMD_N

**CPU/FSB Constraints**

SYNC\_MASTER=T9 SYNC\_DATE=01/30/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	66	73

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
PCIE_R2D_2_Pcie_R2D	*	0.228 MM	?
PCIE_D2R_2_Pcie_D2R	*	0.228 MM	?
PCIE_R2D_2_Pcie_D2R	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_N2S_2_DMI_N2S	*	0.228 MM	?
DMI_S2N_2_DMI_S2N	*	0.228 MM	?
DMI_N2S_2_DMI_S2N	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_R2D_2_Pcie_R2D
PCIE_D2R	PCIE_D2R	*	PCIE_D2R_2_Pcie_D2R
PCIE_R2D	PCIE_D2R	*	PCIE_R2D_2_Pcie_D2R

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PWR	*	BUS2PWR_GND
PCIE_R2D	GND	*	BUS2PWR_GND
PCIE_D2R	PWR	*	BUS2PWR_GND
PCIE_D2R	GND	*	BUS2PWR_GND
DMI_N2S	PWR	*	BUS2PWR_GND
DMI_N2S	GND	*	BUS2PWR_GND
DMI_S2N	PWR	*	BUS2PWR_GND
DMI_S2N	GND	*	BUS2PWR_GND
LVDS	PWR	*	BUS2PWR_GND
LVDS	GND	*	BUS2PWR_GND
TMDS	PWR	*	BUS2PWR_GND
TMDS	GND	*	BUS2PWR_GND

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PWR	*	BUS2PWR_GND
PCIE_R2D	GND	*	BUS2PWR_GND
PCIE_D2R	PWR	*	BUS2PWR_GND
PCIE_D2R	GND	*	BUS2PWR_GND
DMI_N2S	PWR	*	BUS2PWR_GND
DMI_N2S	GND	*	BUS2PWR_GND
DMI_S2N	PWR	*	BUS2PWR_GND
DMI_S2N	GND	*	BUS2PWR_GND
LVDS	PWR	*	BUS2PWR_GND
LVDS	GND	*	BUS2PWR_GND
TMDS	PWR	*	BUS2PWR_GND
TMDS	GND	*	BUS2PWR_GND

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?
LVDS2LVDS	*	0.300 MM	?
TMDS	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC
LVDS	LVDS	*	LVDS2LVDS

LVDS signals are 100-ohm +/- 20% differential impedance.  
 CRT & TVDAC signal single-ended impedance varies by location:  
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.  
 - 50-ohm +/- 15% from first to second termination resistor.  
 - 55-ohm +/- 15% from second termination resistor to connector.  
 CRT\_HSYNC/CRT\_VSYNC signals are 55-ohm +/- 15% single-ended impedance.  
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
PEG_R2D	PCIE_100D	PCIE_R2D	PEG_R2D_P<15..0>
	PCIE_100D	PCIE_R2D	PEG_R2D_N<15..0>
	PCIE_100D	PCIE_R2D	PEG_R2D_C_P<15..0>
	PCIE_100D	PCIE_R2D	PEG_R2D_C_N<15..0>
PEG_D2R	PCIE_100D	PCIE_D2R	PEG_D2R_P<15..0>
	PCIE_100D	PCIE_D2R	PEG_D2R_N<15..0>
	PCIE_100D	PCIE_D2R	PEG_D2R_C_P<15..0>
	PCIE_100D	PCIE_D2R	PEG_D2R_C_N<15..0>
DMI_N2S	DMI_100D	DMI_N2S	DMI_N2S_P<3..0>
	DMI_100D	DMI_N2S	DMI_N2S_N<3..0>
	DMI_100D	DMI_S2N	DMI_S2N_P<3..0>
	DMI_100D	DMI_S2N	DMI_S2N_N<3..0>
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_P<2..0>
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_N<2..0>
LVDS_A_DATA1	LVDS_100D	LVDS	NC_LVDS_A_DATA_P3
LVDS_A_DATA1	LVDS_100D	LVDS	NC_LVDS_A_DATA_N3
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_P
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_N
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>
LVDS_B_DATA1	LVDS_100D	LVDS	NC_LVDS_B_DATA_P3
LVDS_B_DATA1	LVDS_100D	LVDS	NC_LVDS_B_DATA_N3
LVDS_IBG	LVDS	LVDS	LVDS_IBG
CRT_TV0_IREF	CRT	CRT	CRT_TV0_IREF
CRT_RED	CRT_50S	CRT	CRT_RED
CRT_GREEN	CRT_50S	CRT	CRT_GREEN
CRT_BLUE	CRT_50S	CRT	CRT_BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC
EXT_COMEVID_B	CRT_50S	CRT	EXT_COMEVID_B
EXT_Y_G	CRT_50S	CRT	EXT_Y_G
EXT_C_R	CRT_50S	CRT	EXT_C_R
VGA_R	CRT_50S	CRT	VGA_R
VGA_G	CRT_50S	CRT	VGA_G
VGA_B	CRT_50S	CRT	VGA_B
	PCIE_100D	PCIE_R2D	TMDS_SDB_P
	PCIE_100D	PCIE_R2D	TMDS_SDB_N
	PCIE_100D	PCIE_R2D	TMDS_SDC_P
	PCIE_100D	PCIE_R2D	TMDS_SDC_N
	PCIE_100D	PCIE_R2D	TMDS_SDG_P
	PCIE_100D	PCIE_R2D	TMDS_SDG_N
	PCIE_100D	PCIE_R2D	TMDS_SDR_P
	PCIE_100D	PCIE_R2D	TMDS_SDR_N
	TMDS_100D	TMDS	TMDS_TX_CLK_P
	TMDS_100D	TMDS	TMDS_TX_CLK_N
	PCIE_100D	PCIE_D2R	TMDS_INT_P
	PCIE_100D	PCIE_D2R	TMDS_INT_N
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_P
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_N
	TMDS_100D	TMDS	TMDS_CONN_P<3..0>
	TMDS_100D	TMDS	TMDS_CONN_N<3..0>
	TMDS_100D	TMDS	TMDS_TX_P<3..0>
	TMDS_100D	TMDS	TMDS_TX_N<3..0>
	SNB_55S	SNB	TMDS_DDC_SCL
	SNB_55S	SNB	TMDS_DDC_SDA

NB Constraints

SYNC\_MASTER=T9 SYNC\_DATE=01/30/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	67	73

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	ISL3, ISL10	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_87D	*	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK2MEM	*	=2.28:1_SPACING	?	MEM_CLK	GND	*	GND_P2MM
MEM_CTRL2CTRL	*	=1:1_SPACING	?	MEM_CMD	GND	*	GND_P2MM
MEM_CTRL2MEM	*	=2.28:1_SPACING	?	MEM_CTRL	GND	*	GND_P2MM
MEM_CMD2CMD	*	=1:1_SPACING	?	MEM_DATA	GND	*	GND_P2MM
MEM_CMD2MEM	*	=2.28:1_SPACING	?	MEM_DQS	GND	*	GND_P2MM
MEM_DATA2DATA	*	=1:1_SPACING	?	MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_DATA2MEM	*	=2.28:1_SPACING	?	MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DQS2MEM	*	=2.28:1_SPACING	?	MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_2OTHER	*	25 MIL	?	MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

PP0V9_S3M_MEM_NBVREFB	NET_SPACING_TYPE=NB_STATIC	8 16 21
PP0V9_S3M_MEM_NBVREFA	NET_SPACING_TYPE=NB_STATIC	8 16 21
NB_VCCSM_LF1	NET_SPACING_TYPE=NB_STATIC	4 10
NB_VCCSM_LF2	NET_SPACING_TYPE=NB_STATIC	4 10
NB_VCCSM_LF3	NET_SPACING_TYPE=NB_STATIC	4 10
NB_VCCSM_LF4	NET_SPACING_TYPE=NB_STATIC	4 10
NB_VCCSM_LF5	NET_SPACING_TYPE=NB_STATIC	4 10
NB_VCCSM_LF6	NET_SPACING_TYPE=NB_STATIC	4 10
NB_VCCSM_LF7	NET_SPACING_TYPE=NB_STATIC	4 10
PP1V8_S3	NET_SPACING_TYPE=PP1V8_MEM	5, 7, 16 18 21 31 32 34 35 51
GND	NET_SPACING_TYPE=GND	

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	MEM_87D	MEM_CLK	MEM_CLK P<2..0>	16 31 33
	MEM_87D	MEM_CLK	MEM_CLK N<2..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_CS L<1..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	4 16 31 33
	MEM_55S	MEM_CMD	MEM_A A<13..0>	17 31 33
	MEM_55S	MEM_CMD	MEM_A BS<2..0>	17 31 33
	MEM_55S	MEM_CMD	MEM_A RAS L	17 31 33
	MEM_55S	MEM_CMD	MEM_A CAS L	17 31 33
	MEM_55S	MEM_CMD	MEM_A WE L	17 31 33
	MEM_55S	MEM_DATA	MEM A DQ<7..0>	17 31
	MEM_55S	MEM_DATA	MEM A DQ<15..8>	17 31
	MEM_55S	MEM_DATA	MEM A DQ<23..16>	17 31
	MEM_55S	MEM_DATA	MEM A DQ<31..24>	17 31
	MEM_55S	MEM_DATA	MEM A DQ<39..32>	17 31
	MEM_55S	MEM_DATA	MEM A DQ<47..40>	17 31
	MEM_55S	MEM_DATA	MEM A DQ<55..48>	17 31
	MEM_55S	MEM_DATA	MEM A DQ<63..56>	17 31
	MEM_55S	MEM_DATA	MEM A DM<0>	17 31
	MEM_55S	MEM_DATA	MEM A DM<1>	17 31
	MEM_55S	MEM_DATA	MEM A DM<2>	17 31
	MEM_55S	MEM_DATA	MEM A DM<3>	17 31
	MEM_55S	MEM_DATA	MEM A DM<4>	17 31
	MEM_55S	MEM_DATA	MEM A DM<5>	17 31
	MEM_55S	MEM_DATA	MEM A DM<6>	17 31
	MEM_55S	MEM_DATA	MEM A DM<7>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<0>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<0>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<1>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<1>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<2>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<2>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<3>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<3>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<4>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<4>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<5>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<5>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<6>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<6>	17 31
	MEM_85D	MEM_DQS	MEM A DQS P<7>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<7>	17 31
	MEM_87D	MEM_CLK	MEM_CLK P<5..3>	16 32 33
	MEM_87D	MEM_CLK	MEM_CLK N<5..3>	16 32 33
	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
	MEM_45S	MEM_CTRL	MEM_CS L<3..2>	16 32 33
	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	4 16 32 33
	MEM_55S	MEM_CMD	MEM B A<13..0>	17 32 33
	MEM_55S	MEM_CMD	MEM B BS<2..0>	17 32 33
	MEM_55S	MEM_CMD	MEM B RAS L	17 32 33
	MEM_55S	MEM_CMD	MEM B CAS L	17 32 33
	MEM_55S	MEM_CMD	MEM B WE L	17 32 33
	MEM_55S	MEM_DATA	MEM B DQ<7..0>	17 32
	MEM_55S	MEM_DATA	MEM B DQ<15..8>	17 32
	MEM_55S	MEM_DATA	MEM B DQ<23..16>	17 32
	MEM_55S	MEM_DATA	MEM B DQ<31..24>	17 32
	MEM_55S	MEM_DATA	MEM B DQ<39..32>	17 32
	MEM_55S	MEM_DATA	MEM B DQ<47..40>	17 32
	MEM_55S	MEM_DATA	MEM B DQ<55..48>	17 32
	MEM_55S	MEM_DATA	MEM B DQ<63..56>	17 32
	MEM_55S	MEM_DATA	MEM B DM<0>	17 32
	MEM_55S	MEM_DATA	MEM B DM<1>	17 32
	MEM_55S	MEM_DATA	MEM B DM<2>	17 32
	MEM_55S	MEM_DATA	MEM B DM<3>	17 32
	MEM_55S	MEM_DATA	MEM B DM<4>	17 32
	MEM_55S	MEM_DATA	MEM B DM<5>	17 32
	MEM_55S	MEM_DATA	MEM B DM<6>	17 32
	MEM_55S	MEM_DATA	MEM B DM<7>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<0>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<0>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<1>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<1>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<2>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<2>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<3>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<3>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<4>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<4>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<5>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<5>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<6>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<6>	17 32
	MEM_85D	MEM_DQS	MEM B DQS P<7>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<7>	17 32

**Memory Constraints**

SYNC\_MASTER=T9 SYNC\_DATE=01/30/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	
NONE	68	73	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	PWR	*	BUS2PWR_GND
USB	GND	*	BUS2PWR_GND

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
IDE_BDD	IDE_55S	IDE	IDE_PDD<15..0>	6 23 38
IDE_BDA	IDE_55S	IDE	IDE_PDA<2..0>	6 23 38
IDE_EDCS1	IDE_55S	IDE	IDE_PDCS1 L	6 23 38
IDE_EDCS	IDE_55S	IDE	IDE_PDCS3 L	6 23 38
IDE_CNTR1	IDE_55S	IDE	IDE_PDIOV L	6 23 38
IDE_BDIOR_1	IDE_55S	IDE	IDE_PDIOV R	6 23 38
IDE_CNTR2	IDE_55S	IDE	IDE_PDDACK L	6 23 38
IDE_CNTR3	IDE_55S	IDE	IDE_PDDREQ	6 23 38
IDE_BDIORDY	IDE_55S	IDE	IDE_PDIOV L	6 23 38
IDE_IRO14	IDE_55S	IDE	IDE_IRO14	6 23 38
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L	6 23 38
SATA_A_R2D	SATA_100D	SATA	NC_SATA_A_R2D_C_P	9 23
SATA_100D	SATA_100D	SATA	NC_SATA_A_R2D_C_N	9 23
SATA_100D	SATA_100D	SATA	SATA_A_R2D_P	9 23
SATA_100D	SATA_100D	SATA	SATA_A_R2D_N	9 23
SATA_A_D2R	SATA_100D	GND	NC_SATA_A_D2R_P	9
SATA_100D	SATA_100D	GND	NC_SATA_A_D2R_N	9
SATA_100D	SATA_100D	SATA	SATA_A_D2R_C_P	9
SATA_100D	SATA_100D	SATA	SATA_A_D2R_C_N	9
SATA_B_R2D	SATA_100D	SATA	NC_SATA_B_R2D_C_P	9 23
SATA_100D	SATA_100D	SATA	NC_SATA_B_R2D_C_N	9 23
SATA_100D	SATA_100D	SATA	SATA_B_R2D_P	9 23
SATA_100D	SATA_100D	SATA	SATA_B_R2D_N	9 23
SATA_A_D2R	SATA_100D	GND	NC_SATA_B_D2R_P	9
SATA_100D	SATA_100D	GND	NC_SATA_B_D2R_N	9
SATA_100D	SATA_100D	SATA	SATA_B_D2R_C_P	9
SATA_100D	SATA_100D	SATA	SATA_B_D2R_C_N	9
SATA_C_R2D	SATA_100D	SATA	NC_SATA_C_R2D_C_P	9 23
SATA_100D	SATA_100D	SATA	NC_SATA_C_R2D_C_N	9 23
SATA_100D	SATA_100D	SATA	SATA_C_R2D_P	9 23
SATA_100D	SATA_100D	SATA	SATA_C_R2D_N	9 23
SATA_A_D2R	SATA_100D	GND	NC_SATA_C_D2R_P	9
SATA_100D	SATA_100D	GND	NC_SATA_C_D2R_N	9
SATA_100D	SATA_100D	SATA	SATA_C_D2R_C_P	9
SATA_100D	SATA_100D	SATA	SATA_C_D2R_C_N	9
SATA_RB1AR	SATA_55S	SATA	SATA_RB1AR	9
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	6 7 9 23 37
HDA_55S	HDA_55S	HDA	HDA_BIT_CLK_R	6 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	6 7 9 23 37
HDA_55S	HDA_55S	HDA	HDA_SYNC_R	6 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	6 9 23 37
HDA_55S	HDA_55S	HDA	HDA_RST_L_R	6 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	6 7 9 23 37
HDA_55S	HDA_55S	HDA	HDA_SDIN_CODEC	6 7 9 23 37
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	6 7 9 23 37
HDA_55S	HDA_55S	HDA	HDA_SDOUT_R	6 23
USB_EXTA	USB_90D	USB	USB2_EXTA_P	6 9 24 39
USB_90D	USB_90D	USB	USB2_EXTA_N	6 9 24 39
USB_90D	USB_90D	USB	USB2_MUXED_EXTA_N	6 9 39
USB_90D	USB_90D	USB	USB2_MUXED_EXTA_P	6 9 39
USB_MINI	USB_90D	USB	USB2_AIRPORT_P	6 9 24 36
USB_90D	USB_90D	USB	USB2_AIRPORT_N	6 9 24 36
USB_EXTD	USB_90D	USB	TP_USB2_3G_P	9 24
USB_90D	USB_90D	USB	TP_USB2_3G_N	9 24
USB_CAMERA	USB_90D	USB	USB2_CAMERA_P	6 9 24 60
USB_90D	USB_90D	USB	USB2_CAMERA_N	6 9 24 60
USB_BT	USB_90D	USB	NC_USB_BT_P	9 24
USB_90D	USB_90D	USB	NC_USB_BT_N	9 24
USB_TPAD	USB_90D	USB	USB2_WSPRING_P	6 7 9 24 40
USB_90D	USB_90D	USB	USB2_WSPRING_N	6 7 9 24 40
USB_IR	USB_90D	USB	USB_IR_P	6 7 9 24 40
USB_90D	USB_90D	USB	USB_IR_N	6 7 9 24 40
USB_EXTR	USB_90D	USB	NC_USB2_EXTB_P	9 24
USB_90D	USB_90D	USB	NC_USB2_EXTB_N	9 24
USB_EXCARD	USB_90D	USB	TP_USB_EXCARD_P	9 24
USB_90D	USB_90D	USB	TP_USB_EXCARD_N	9 24
USB_EXTC	USB_90D	USB	TP_USB_EXTC_P	9 24
USB_90D	USB_90D	USB	TP_USB_EXTC_N	9 24
USB_90D	USB_90D	USB	USB2_AIRPORT_P_F	6 36
USB_90D	USB_90D	USB	USB2_AIRPORT_N_F	6 36
USB_90D	USB_90D	USB	USB2_CAMERA_F_P	6 7 60
USB_90D	USB_90D	USB	USB2_CAMERA_F_N	6 7 60
USB_90D	USB_90D	USB	USB2_EXTA_F_P	6 7 37 39
USB_90D	USB_90D	USB	USB2_EXTA_F_N	6 7 37 39
USB_90D	USB_90D	USB	USB2_3G_F_P	9 24
USB_90D	USB_90D	USB	USB2_3G_F_N	9 24
USB_RB1AR	USB_60S	USB	USB_RB1AR	6 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL	6 25 29 44
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA	6 25 29 44
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL	6 25 44
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA	6 25 44
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	6 24 49
SPI_55S	SPI_55S	SPI	SPI_SCLK	6 24 49
SPI_55S	SPI_55S	SPI	SPI_A_SCLK_R	6 43 49
SPI_55S	SPI_55S	SPI	SPI_B_SCLK_R	6 43 49
SPI_SI	SPI_55S	SPI	SPI_SI_R	6 24 49
SPI_55S	SPI_55S	SPI	SPI_SI	6 24 49
SPI_55S	SPI_55S	SPI	SPI_A_SI_R	6 43 49
SPI_55S	SPI_55S	SPI	SPI_B_SI_R	6 43 49
SPI_SO	SPI_55S	SPI	SPI_SO	6 24 43 49
SPI_55S	SPI_55S	SPI	SPI_A_SO_R	6 49
SPI_55S	SPI_55S	SPI	SPI_B_SO	6 49
SPI_55S	SPI_55S	SPI	SPI_B_SO_R	6 49
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	6 24 49
SPI_55S	SPI_55S	SPI	SPI_CE_L<0>	6 43 49
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	6 24 43
SPI_55S	SPI_55S	SPI	SPI_CE_L<1>	6 24 43

**SB Constraints (1 of 2)**  
 SYNC\_MASTER=T9 SYNC\_DATE=01/30/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?
PCIE_R2D	*	=PCIE	?
PCIE_D2R	*	=PCIE	?
PCIE_9MIL	*	0.228 MM	?
PCIE_12MIL	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_9MIL
PCIE_D2R	PCIE_D2R	*	PCIE_9MIL
PCIE_D2R	PCIE_R2D	*	PCIE_12MIL

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	9
PCI_AD19	PCI_55S	PCI	NC_PCI_AD<19>	9 24
PCI_AD20	PCI_55S	PCI	NC_PCI_AD<20>	9 24
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	9
PCI_AD	PCI_55S	PCI	NC_PCI_PAR	9 24
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	9
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	6 24
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	6 24
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	6 24
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	6 24
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	6 24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	6 24
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	6 24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	6 24
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	6 24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	6 24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	6 24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	6 24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	6 24
PCI_A_R2D	PCI_100D	PCI_R2D	PCIE A R2D C P	
PCI_A_R2D	PCI_100D	PCI_R2D	PCIE A R2D C N	
PCI_A_D2R	PCI_100D	PCI_D2R	PCIE A D2R P	
PCI_A_D2R	PCI_100D	PCI_D2R	PCIE A D2R N	
PCI_B_R2D	PCI_100D	PCI_R2D	PCIE B R2D C P	
PCI_B_R2D	PCI_100D	PCI_R2D	PCIE B R2D C N	
PCI_B_D2R	PCI_100D	PCI_D2R	PCIE B D2R P	
PCI_B_D2R	PCI_100D	PCI_D2R	PCIE B D2R N	
			PCIE EXCARD R2D C P	
			PCIE EXCARD R2D C N	
			PCIE EXCARD D2R P	
			PCIE EXCARD D2R N	
			PCIE FW R2D C P	
			PCIE FW R2D C N	
			PCIE FW D2R P	
			PCIE FW D2R N	
PCI_E_R2D	PCI_100D	PCI_R2D	PCIE E R2D C P	6 24 36
PCI_E_R2D	PCI_100D	PCI_R2D	PCIE E R2D C N	6 24 36
PCI_E_D2R	PCI_100D	PCI_D2R	PCIE E D2R P	6 24 36
PCI_E_D2R	PCI_100D	PCI_D2R	PCIE E D2R N	6 24 36
			PCIE ENET R2D C P	
			PCIE ENET R2D C N	
			PCIE ENET D2R P	
			PCIE ENET D2R N	
GLAN_COMP			GLAN COMP	6 23
ENET_KBIAS			NINEVEH_KBIAS_P	
ENET_RBIAS			NINEVEH_RBIAS	
(PCIE_ENET_R2D)	GLAN_100D	ENET_GLAN	ENET GLAN R2D P	
GLAN_100D	ENET_GLAN		ENET GLAN R2D N	
(PCIE_ENET_D2R)	GLAN_100D	ENET_GLAN	ENET GLAN D2R C P	
GLAN_100D	ENET_GLAN		ENET GLAN D2R C N	
ENET_LAN	LAN_55S	ENET_LAN	LAN_RSTSYNC	
ENET_LAN	LAN_55S	ENET_LAN	LAN_R2D<2..0>	
ENET_LAN	LAN_55S	ENET_LAN	LAN_D2R<2..0>	
ENET_GLAN_CLK	LAN_55S	ENET_CLK	ENET_GLAN_CLK_R	
LAN_55S	ENET_CLK		ENET_GLAN_CLK	
ENET_MDI0	ENET_100D	ENET_MDI	ENET MDI P<0>	
ENET_100D	ENET_MDI		ENET MDI N<0>	
ENET_MDI1	ENET_100D	ENET_MDI	ENET MDI P<1>	
ENET_100D	ENET_MDI		ENET MDI N<1>	
ENET_MDI2	ENET_100D	ENET_MDI	ENET MDI P<2>	
ENET_100D	ENET_MDI		ENET MDI N<2>	
ENET_MDI3	ENET_100D	ENET_MDI	ENET MDI P<3>	
ENET_100D	ENET_MDI		ENET MDI N<3>	
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	6 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	6 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	6 16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	6 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	6 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	6 25

SB Constraints (2 of 2)  
 SYNC\_MASTER=T9 SYNC\_DATE=01/30/2007  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	73
NONE	70		

### Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	PWR	*	BUS2PWR_GND
CLK_FSB	GND	*	BUS2PWR_GND
CLK_PCIE	PWR	*	BUS2PWR_GND
CLK_PCIE	GND	*	BUS2PWR_GND
CLK_MED	PWR	*	BUS2PWR_GND
CLK_MED	GND	*	BUS2PWR_GND

### Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
CK505_PCIE0	CLK_MED_55S	CLK_MED	CK505_PCIE0_CLK_ITPEN	
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK	6 29 30
CK505_PCIE2	CLK_MED_55S	CLK_MED	CK505_PCIE2_CLK	
CK505_PCIE3	CLK_MED_55S	CLK_MED	CK505_PCIE3_CLK	6 29 30
CK505_PCIE4	CLK_MED_55S	CLK_MED	CK505_PCIE4_CLK	
CK505_PCIE5	CLK_MED_55S	CLK_MED	CK505_PCIE5_CLK_FCTSEL	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
(CK505_PCIE0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6 30 43
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	6 24 30
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	
(CK505_PCIE2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCIE3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	6 30 41
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTRL	6 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	6 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	6 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	6 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
CK505_SRC4	SATA_100D	GND	SB_CLK100M_SATA_P	
CK505_SRC4	SATA_100D	GND	SB_CLK100M_SATA_N	
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
(CK505_SRC7)			CK505_SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	

### SMC SMBus Net Properties

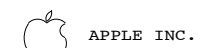
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	6 7 36 40 41 44
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	6 7 36 40 41 44
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	
SMBUS_SMC_O_S0_SCL	SMB_55S	SMB	SMBUS_SMC_O_S0_SCL	6 7 41 44 46
SMBUS_SMC_O_S0_SDA	SMB_55S	SMB	SMBUS_SMC_O_S0_SDA	6 7 41 44 46
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	6 7 41 44 50 59
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	6 7 41 44 50 59
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	6 41 44 48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	6 41 44 48

### Clock & SMC Constraints

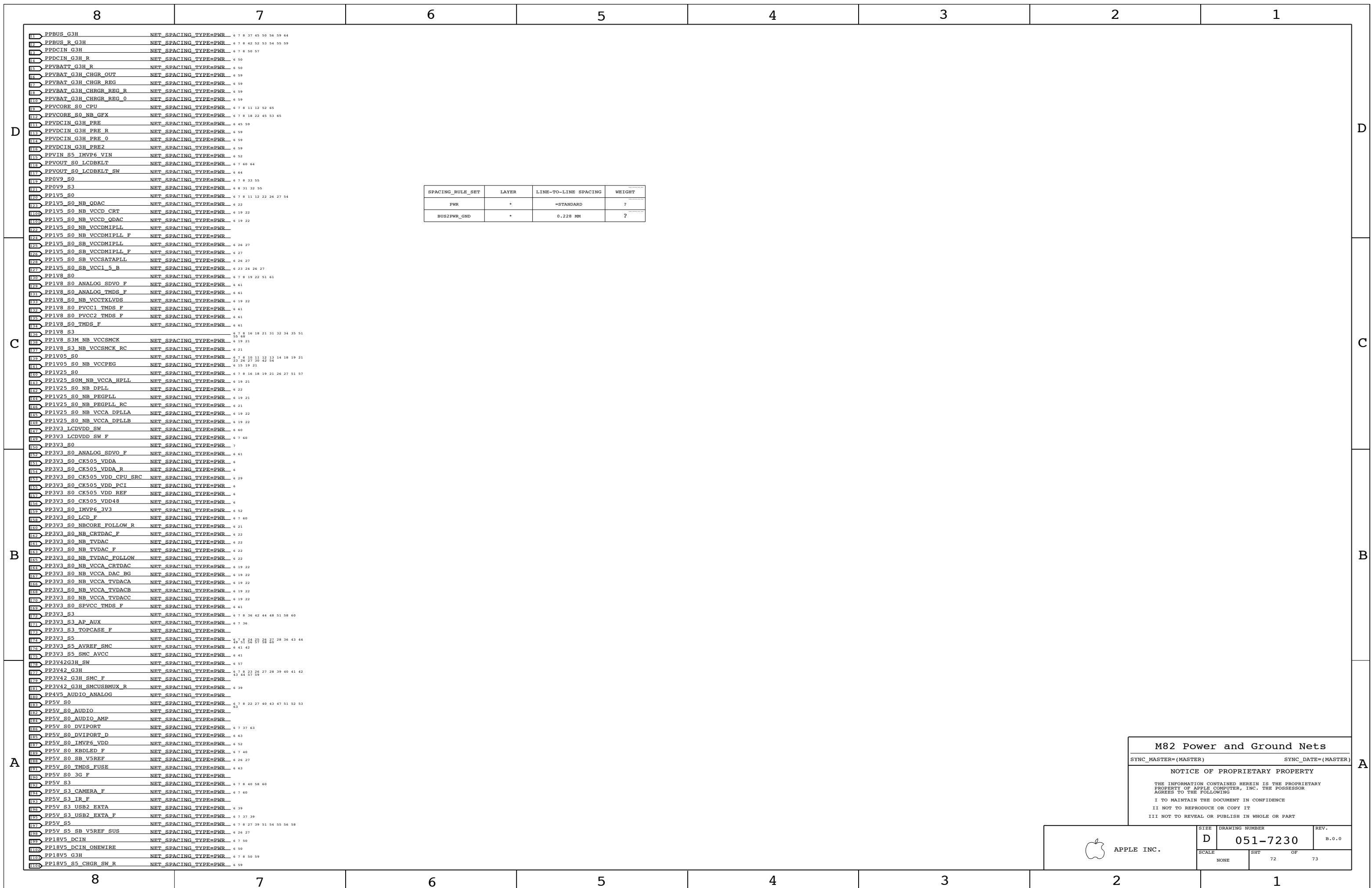
SYNC\_MASTER=T9 SYNC\_DATE=01/30/2007

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	71	73



SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

**M82 Power and Ground Nets**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
SCALE	SHT	OF	
NONE	72	73	



8

7

6

5

4

3

2

1

### M82 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, ISL12, ISL13, BOTTOM				NO_TYPE, BGA			MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL2, ISL4, ISL5	Y	0.215 MM	0.215 MM			
27P4_OHM_SE	ISL10, ISL11, ISL13	Y	0.215 MM	0.215 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP, BOTTOM	Y	0.290 MM	0.290 MM			
45_OHM_SE	ISL2, ISL4, ISL5	Y	0.091 MM	0.091 MM			
45_OHM_SE	ISL10, ISL11, ISL13	Y	0.091 MM	0.091 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP, BOTTOM	Y	0.235 MM	0.235 MM			
50_OHM_SE	ISL2, ISL4, ISL5	Y	0.070 MM	0.070 MM			
50_OHM_SE	ISL10, ISL11, ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP, BOTTOM	Y	0.190 MM	0.190 MM			
55_OHM_SE	ISL2, ISL4, ISL5	Y	0.070 MM	0.070 MM	55OHM SE ON INTERNAL LAYERS NOT ACHIEVABLE IN M82 STACKUP USING 50OHM SE		
55_OHM_SE	ISL10, ISL11, ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP, BOTTOM	Y	0.310 MM	0.310 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP, BOTTOM	Y	0.230 MM	0.230 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
85_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
87_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
87_OHM_DIFF	TOP, BOTTOM	Y	0.220 MM	0.220 MM		0.180 MM	0.180 MM
87_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
87_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP, BOTTOM	Y	0.190 MM	0.190 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP, BOTTOM	Y	0.170 MM	0.170 MM		0.205 MM	0.205 MM
100_OHM_DIFF	ISL2, ISL4, ISL5	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	ISL10, ISL11, ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
111_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

### M82 Rule Definitions

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

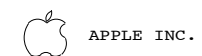
#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE	SHT	OF
NONE	73	73

8

7

6

5

4

3

2

1