

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# OROYA

03/20/2007 - DVT

| REV | ZONE | ECN | DESCRIPTION OF CHANGE | CK APPD<br>DATE | ENG APPD<br>DATE |
|-----|------|-----|-----------------------|-----------------|------------------|
| ?   |      | ?   | ?                     | ?               | ?                |

| Page | (.csa) | Contents                        | Sync       | Date       |
|------|--------|---------------------------------|------------|------------|
| 1    | 1      | Table of Contents               | N/A        | N/A        |
| 2    | 2      | System Block Diagram            | (T9_MLB)   | 08/23/2006 |
| 3    | 3      | Power Block Diagram             | (T9_MLB)   | 08/23/2006 |
| 4    | 4      | Power Block Diagram             | N/A        | N/A        |
| 5    | 5      | BOM Configuration               | N/A        | N/A        |
| 6    | 6      | Revision History                | N/A        | N/A        |
| 7    | 7      | Functional / ICT Test           | (MASTER)   | (MASTER)   |
| 8    | 8      | Power Aliases                   | (MASTER)   | (MASTER)   |
| 9    | 9      | Signal Aliases                  | (T9_MLB)   | 08/23/2006 |
| 10   | 10     | CPU FSB                         | T9_NOME    | 03/16/2007 |
| 11   | 11     | CPU Power & Ground              | T9_NOME    | 03/16/2007 |
| 12   | 12     | CPU Decoupling & VID            | M76_MLB    | 03/19/2007 |
| 13   | 13     | eXtended Debug Port (XDP)       | T9_NOME    | 12/12/2006 |
| 14   | 14     | NB CPU Interface                | T9_NOME    | 03/16/2007 |
| 15   | 15     | NB PEG / Video Interfaces       | T9_NOME    | 03/16/2007 |
| 16   | 16     | NB Misc Interfaces              | T9_NOME    | 03/16/2007 |
| 17   | 17     | NB DDR2 Interfaces              | T9_NOME    | 03/16/2007 |
| 18   | 18     | NB Power 1                      | T9_NOME    | 03/16/2007 |
| 19   | 19     | NB Power 2                      | T9_NOME    | 03/16/2007 |
| 20   | 20     | NB Grounds                      | T9_NOME    | 03/16/2007 |
| 21   | 21     | NB Standard Decoupling          | T9_NOME    | 01/17/2007 |
| 22   | 22     | NB Graphics Decoupling          | M76_MLB    | 03/12/2007 |
| 23   | 23     | SB Enet, Disk, FSB, LPC         | T9_NOME    | 03/16/2007 |
| 24   | 24     | SB PCI, PCIE, DMI, USB          | T9_NOME    | 03/16/2007 |
| 25   | 25     | SB Pwr Mgt, GPIO, Clink         | T9_NOME    | 03/16/2007 |
| 26   | 26     | SB Power & Ground               | T9_NOME    | 03/16/2007 |
| 27   | 27     | SB Decoupling                   | T9_NOME    | 01/17/2007 |
| 28   | 28     | SB Misc                         | (T9_MLB)   | 08/24/2006 |
| 29   | 29     | Clock (CK505)                   | T9_NOME    | 03/16/2007 |
| 30   | 30     | Clock Termination               | (MASTER)   | 08/23/2006 |
| 31   | 31     | DDR2 SO-DIMM Connector A        | (M59_SYNC) | 08/24/2006 |
| 32   | 32     | DDR2 SO-DIMM Connector B        | (M59_SYNC) | 08/24/2006 |
| 33   | 33     | Memory Active Termination       | (T9_NOME)  | 11/14/2006 |
| 34   | 34     | Left I/O Board Connector        | (M59_SYNC) | 08/24/2006 |
| 35   | 35     | Ethernet (Yukon)                | T9_NOME    | 03/16/2007 |
| 36   | 36     | Yukon Power Control             | T9_NOME    | 03/16/2007 |
| 37   | 37     | Ethernet Connector              | M76_MLB    | 03/19/2007 |
| 38   | 38     | FireWire Link (TSB83AA22)       | M76_MLB    | 03/19/2007 |
| 39   | 39     | FireWire PHY (TSB83AA22)        | M76_MLB    | 03/19/2007 |
| 40   | 40     | FireWire Port Power             | M76_MLB    | 03/19/2007 |
| 41   | 41     | FireWire Ports                  | M76_MLB    | 03/19/2007 |
| 42   | 42     | PATA Connector                  | (MASTER)   | (MASTER)   |
| 43   | 43     | External USB Connector          | M76_MLB    | 03/19/2007 |
| 44   | 44     | Left Clutch Barrel Interconnect | M76_MLB    | 03/19/2007 |

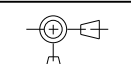
| Page | (.csa) | Contents                            | Sync       | Date       |
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| 45   | 45     | SMC                                 | T9_NOME    | 01/17/2007 |
| 46   | 46     | SMC Support                         | (MASTER)   | (MASTER)   |
| 47   | 47     | LPC+ Debug Connector                | M76_MLB    | 03/19/2007 |
| 48   | 48     | SMBus Connections                   | (MASTER)   | (MASTER)   |
| 49   | 49     | Current & Voltage Sensing           | (MASTER)   | (MASTER)   |
| 50   | 50     | Current Sensing                     | (MASTER)   | (MASTER)   |
| 51   | 51     | Thermal Sensors                     | (MASTER)   | (MASTER)   |
| 52   | 52     | Fan Connectors                      | M76_MLB    | 03/19/2007 |
| 53   | 53     | ALS Support                         | M76_MLB    | 03/19/2007 |
| 54   | 54     | Sudden Motion Sensor (SMS)          | M76_MLB    | 03/19/2007 |
| 55   | 55     | SPI BootROM                         | T9_NOME    | 03/16/2007 |
| 56   | 56     | PBus-In & Battery Connectors        | (M59_SYNC) | 09/09/2006 |
| 57   | 57     | Power FETs                          | M76_MLB    | 03/19/2007 |
| 58   | 58     | IMVP6 CPU VCore Regulator           | M76_MLB    | 01/23/2007 |
| 59   | 59     | IMVP6 NB Gfx Core Regulator         | M76_MLB    | 03/19/2007 |
| 60   | 60     | 5V / 3.3V Power Supply              | M76_MLB    | 03/19/2007 |
| 61   | 61     | 1.25V / 1.05V Power Supply          | M76_MLB    | 03/12/2007 |
| 62   | 62     | 1.8V DDR2 Supply                    | M76_MLB    | 03/19/2007 |
| 63   | 63     | 1.5V Power Supply                   | M76_MLB    | 03/12/2007 |
| 64   | 64     | FW PHY Power Supplies               | M76_MLB    | 03/19/2007 |
| 65   | 65     | 3.425V G3Hot Supply & Power Control | (MASTER)   | (MASTER)   |
| 66   | 66     | NV G84M PCI-E                       | (MASTER)   | (MASTER)   |
| 67   | 67     | NV G84M Core/FB Power               | (MASTER)   | (MASTER)   |
| 68   | 68     | NV G84M Frame Buffer I/F            | (MASTER)   | (MASTER)   |
| 69   | 69     | GDDR3 Frame Buffer A                | (MASTER)   | (MASTER)   |
| 70   | 70     | GDDR3 Frame Buffer B                | (MASTER)   | (MASTER)   |
| 71   | 71     | NV G84M GPIO/MIO/Misc               | (MASTER)   | (MASTER)   |
| 72   | 72     | GPU Straps                          | (MASTER)   | (MASTER)   |
| 73   | 73     | NV G84M Video Interfaces            | (MASTER)   | (MASTER)   |
| 74   | 74     | GPU (G84M) Core Supply              | (MASTER)   | (MASTER)   |
| 75   | 75     | LVDS Display Connector              | (MASTER)   | (MASTER)   |
| 76   | 76     | DVI Display Connector               | (MASTER)   | (MASTER)   |
| 77   | 77     | LVDS Interface Mux                  | (MASTER)   | (MASTER)   |
| 78   | 78     | M75 Specific Connectors             | (M59_SYNC) | 08/24/2006 |
| 79   | 79     | CPU/FSB Constraints                 | T9_NOME    | 01/17/2007 |
| 80   | 80     | NB Constraints                      | T9_NOME    | 01/17/2007 |
| 81   | 81     | Memory Constraints                  | T9_NOME    | 01/17/2007 |
| 82   | 82     | SB Constraints (1 of 2)             | T9_NOME    | 01/17/2007 |
| 83   | 83     | SB Constraints (2 of 2)             | T9_NOME    | 01/17/2007 |
| 84   | 84     | Clock & SMC Constraints             | T9_NOME    | 01/17/2007 |
| 85   | 85     | FireWire Constraints                | T9_NOME    | 01/17/2007 |
| 86   | 86     | GPU (G84M) Constraints              | (MASTER)   | (MASTER)   |
| 87   | 87     | M75 Specific Constraints            | (MASTER)   | (MASTER)   |
| 88   | 88     | M75 Rule Definitions                | (MASTER)   | (MASTER)   |

# ALIASES RESOLVED

## Schematic / PCB #'s

| PART NUMBER | QTY | DESCRIPTION     | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-----------------|---------------|----------|------------|
| 051-7225    | 1   | SCHEM, MLB, M75 | SCH           | CRITICAL |            |
| 820-2101    | 1   | PCBF, MLB, M75  | PCB           | CRITICAL |            |

DRAWING TITLE=MLB ABBREV=DRAWING LAST\_MODIFIED=Tue Mar 20 20:28:27 2007

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| MATERIAL/FINISH NOTED AS APPLICABLE   |  | SIZE    | D     | DRAWING NUMBER   | REV.   |
|   |  |         |       | 051-7225   | 14.0.0 |
|   |  |         |       | SHT 1  | OF 88  |



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Power Block Diagram

SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/23/2006


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Power Block Diagram

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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## BOM Variants

| BOM NUMBER | BOM NAME                | BOM OPTIONS                                  |
|------------|-------------------------|--|
| 630-7931   | PCBA,OROYA1,M75         | M75_COMMON,EEE_X5D,CPU_2_2GHZ,FB_128_SAMSUNG |
| 630-7932   | PCBA,OROYA2,M75         | M75_COMMON,EEE_X5E,CPU_2_4GHZ,FB_256_SAMSUNG |
| 630-8659   | PCBA,OROYA1,VRAM-HY,M75 | M75_COMMON,EEE_XXS,CPU_2_2GHZ,FB_128_HYNIX   |
| 630-8662   | PCBA,OROYA2,VRAM-HY,M75 | M75_COMMON,EEE_XXT,CPU_2_4GHZ,FB_256_HYNIX   |

## M75 BOM Groups

| BOM GROUP     | BOM OPTIONS  |
|---------------|--|
| M75_COMMON    | ALTERNATE,COMMON,M75_COMMON1,M75_COMMON2,M75_DEBUG,M75_PROGPARTS |
| M75_COMMON1   | EXTGPU_RST_HW,GPU_TMP401,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU     |
| M75_COMMON2   | P1V8S3_1V825,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN     |
| M75_DEBUG     | SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS                               |
| M75_PROGPARTS | BOOTROM_PROG,SMC_PROG  |

| BOM GROUP      | BOM OPTIONS                            |
|----------------|--|
| FB_128_SAMSUNG | VRAM_128,VRAM_SAMSUNG,VRAM_128_SAMSUNG |
| FB_128_HYNIX   | VRAM_128,VRAM_HYNIX,VRAM_128_HYNIX     |
| FB_256_SAMSUNG | VRAM_256,VRAM_SAMSUNG,VRAM_256_SAMSUNG |
| FB_256_HYNIX   | VRAM_256,VRAM_HYNIX,VRAM_256_HYNIX     |

## Bar Code Labels / EEE #'s

| PART NUMBER | QTY | DESCRIPTION                   | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-------------------------------|---------------|----------|------------|
| 826-4393    | 1   | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:X5D]     | CRITICAL | EEE_X5D    |
| 826-4393    | 1   | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:X5E]     | CRITICAL | EEE_X5E    |
| 826-4393    | 1   | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:XXS]     | CRITICAL | EEE_XXS    |
| 826-4393    | 1   | LBL,P/N LABEL,PCB,28MM X 6 MM | [EEE:XXT]     | CRITICAL | EEE_XXT    |

## Module Parts

| PART NUMBER | QTY | DESCRIPTION                                | REFERENCE DES | CRITICAL | BOM OPTION    |
|-------------|-----|--|---------------|----------|---------------|
| 337S3457    | 1   | IC,MEC,SR,E1,QS,2.2G,35W,800FSB,4M,BGA     | U1000         | CRITICAL | CPU_2_2GHZ    |
| 337S3458    | 1   | IC,MEC,SR,E1,QS,2.4G,35W,800FSB,4M,BGA     | U1000         | CRITICAL | CPU_2_4GHZ    |
| 338S0388    | 1   | IC,GPU,NV G84M,BGA                         | U8000         | CRITICAL |               |
| 338S0426    | 1   | IC,NB,CRESTLINE,GM,C0,QS,965PM             | U1400         | CRITICAL |               |
| 338S0427    | 1   | IC,SB,ICH8M,B1,QS,BGA                      | U2300         | CRITICAL |               |
| 353S1461    | 1   | IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,LF    | U7100         | CRITICAL | ISL9504A      |
| 353S1651    | 1   | IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48       | U7100         | CRITICAL | ISL9504B      |
| 359S0127    | 1   | IC,68 PIN,CK505,LOW POWER CLOCK GENER      | U2900         | CRITICAL | SLG8LP537     |
| 359S0130    | 1   | IC,SLG2AP101,1.5W PWR CLCK GEN,CK505,QFN68 | U2900         | CRITICAL | SLG2AP101     |
| 338S0386    | 1   | IC,88E8058,GIGABIT ENET XCVR,64P QFN       | U3700         | CRITICAL |               |
| 338S0274    | 1   | IC,SMC,HS8/2116                            | U4900         | CRITICAL | SMC_BLANK     |
| 341S2004    | 1   | IC,SMC,DEVELOPMENT,M75                     | U4900         | CRITICAL | SMC_PROG      |
| 335S0384    | 1   | IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8     | U6100         | CRITICAL | BOOTROM_BLANK |
| 341S2002    | 1   | IC,EFI ROM,DEVELOPMENT,M75                 | U6100         | CRITICAL | BOOTROM_PROG  |

|          |   |                                       |                         |          |                  |
|----------|---|---------------------------------------|-------------------------|----------|------------------|
| 333S0404 | 4 | IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA  | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_128_SAMSUNG |
| 333S0409 | 4 | IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA  | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_128_HYNIX   |
| 333S0382 | 4 | IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_256_SAMSUNG |
| 333S0401 | 4 | IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA | U8400,U8450,U8500,U8550 | CRITICAL | VRAM_256_HYNIX   |

| PART NUMBER | IS ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:                        |
|-------------|------------------------------|------------|---------|----------------------------------|
| 157S0011    | 157S0030                     |            | ALL     | See alt to TOK/BI-Tech magnetica |
| 152S0476    | 152S0276                     |            | ALL     | Inductor alternate               |
| 353S1681    | 353S1294                     |            | ALL     | TI alt to National               |
| 138S0603    | 138S0602                     |            | ALL     | Murata alt to Samsung            |

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## BOM Configuration

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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| NONE  | 5              | 88     |

PROTO

See Perforce change notes for updates before Proto Release
12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)

EVT

8.1.0:
01/05/07 -- Clock Termination: Removed NO STUFF property from R3067
01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ)
8.2.0:
01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs)
9.0.0:
01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap)
01/12/07 -- Power Aliases: Moved Ethernet to PP3V3\_S3 from S5 (layout improvements)
01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76
9.1.0:
01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3\_S5 from S0
01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K
01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL\_EN and Wake-on-Wireless support
01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs
01/17/07 -- Power Sequencing: Added RC delay on PP1V8\_S3 switcher enable
01/17/07 -- Testpoints: Removed FUNC\_TEST from NB\_RESET\_L and FSB\_DPWR\_L per PCB request
01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131
01/17/07 -- BOM: Added Hynix BOM configurations
9.2.0:
01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5\_S0\_SB\_VCC1\_5\_B
01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms
01/18/07 -- IMVP: Updated BOMPTIONS and values for ISL9504B
01/18/07 -- Testpoints: Added NO\_TEST property to LVDS\_L\_DATA\_N<1>, \_N<2>, \_P<2> due to lack of layout space for TP
01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)
9.3.0:
01/19/07 -- SB Decoupling: Removed filtering for PP1V5\_S0\_SB\_VCCGLANPLL to enable PP1V5\_S0 corrections at SB
01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x
01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101
01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails
01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3\_S5 to eliminate a leakage path
9.4.0:
01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible
01/19/07 -- SB GPIOs: Changed SB\_GPIO42 to WOW\_EN and changed pullup to pulldown (T9\_noME change 40787)
9.5.0:
01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9\_noME change 40998)
01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9\_noME change 40975)
01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility
01/22/07 -- BOM: Added BOMPTIONS for SLG2AP101 (primary) and SLG8LP537 (backup)
01/22/07 -- BOM: Selected P1V8S3\_1V825 BOMPTION to lift voltage at FB memories
10.0.0:
01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9\_noME change 41248)
01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMPTIONS to GPU straps)
01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)

EVT\_SE

10.1.0:
01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0
01/24/07 -- PATA Conn: Changed =PP5V\_S0\_ODDPWREN to =PP3V3\_S0\_ODDPWREN for minor power savings
01/24/07 -- Power Aliases: Updated PP3V3\_S0 aliases to support above changes
10.2.0:
01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST
01/25/07 -- Power Aliases: Updated PP5V\_S0 aliases to support above changes
11.0.0:
01/25/07 -- BOM: Updated gain of PP1V25\_ENET current sense amplifier to 165 (R5432 to 165K)
01/25/07 -- BOM: Updated all Intel APNs to use QS parts
01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03)
12.0.0:
02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup
02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup
02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain
02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain
02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)

DVT

12.1.0:
02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)
02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K)
02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)
02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX\_PGOOD out of PWR\_OK chain (rdar://4974927)
02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)
02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453)
02/26/07 -- SB GPIOs: Sync'd page25.csa to T9\_MLB to get pullup updates
02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773)
12.2.0:
02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378)
02/28/07 -- Power Aliases: Moving P1V8\_GPU FET source to P1V8\_S3 rather than P1V8\_S3\_ISNS to improve power delivery to GPU (rdar://5021462)
12.3.0:
02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)
02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)
02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)
03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)
03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD\_CRT of NB to GND per CRT disable guidelines
12.4.0:
03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3\_SW\_LCD (in case we add extra cable for power - rdar://5024882)
03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)
12.5.0:
03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V\_S5 to enable layout improvements
12.6.0:
03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on)
03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height
12.7.0:
03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity
03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request
03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)
03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage

DVT (cont'd)

12.8.0:
03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0:
03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0:
03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN\_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0:
03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS\_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0:
03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0:
03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM\_G2\_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0:
03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM\_G2\_EN
14.0.0:
03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)



Revision History

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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Table with columns: DRAWING NUMBER (D 051-7225), REV. (14.0.0), SCALE (NONE), SHT (6 OF 88)

## Functional Test Points

## ICT Test Points

### Fan Connectors

| FUNC_TEST        | Pin                |
|------------------|--------------------|
| TRUE PP5V_S0     | 7 8 27 42 47 52 57 |
| TRUE FAN_LT_PWM  | 52                 |
| TRUE FAN_LT_TACH | 52                 |
| TRUE FAN_RT_PWM  | 52                 |
| TRUE FAN_RT_TACH | 52                 |

### Battery Digital Connector

| FUNC_TEST              | Pin         |
|------------------------|-------------|
| TRUE SMC_BS_ALERT_L    | 45 46 56    |
| TRUE SMBUS_SMC_BSA_SCL | 45 48 56 84 |
| TRUE SMBUS_SMC_BSA_SDA | 45 48 56 84 |
| TRUE GND_BATT          | 56          |

### CPU FSB NO\_TESTS

| NO_TEST                 | Pin      |
|-------------------------|----------|
| TRUE FSB_A_L<31..3>     | 10 14 79 |
| TRUE FSB_ADS_L          | 10 14 79 |
| TRUE FSB_ADSTB_L<1..0>  | 10 14 79 |
| TRUE FSB_BNR_L          | 10 14 79 |
| TRUE FSB_BREQ0_L        | 10 14 79 |
| TRUE FSB_D_L<63..0>     | 10 14 79 |
| TRUE FSB_DBSY_L         | 10 14 79 |
| TRUE FSB_DINV_L<3..0>   | 10 14 79 |
| TRUE FSB_DRDY_L         | 10 14 79 |
| TRUE FSB_DSTB_L_N<3..0> | 10 14 79 |
| TRUE FSB_DSTB_L_P<3..0> | 10 14 79 |
| TRUE FSB_HIT_L          | 10 14 79 |
| TRUE FSB_HITM_L         | 10 14 79 |
| TRUE FSB_LOCK_L         | 10 14 79 |
| TRUE FSB_REQ_L<4..0>    | 10 14 79 |

### NB NO\_TESTS

| NO_TEST              | Pin                   |
|----------------------|-----------------------|
| TRUE NC_NB_NC<1..16> | == TP_NB_NC<1..16>_16 |

### LPC+ Debug Connector

| FUNC_TEST               | Pin                   |
|-------------------------|-----------------------|
| TRUE PP3V42_G3H         | 8 28 35 43 45 46 47   |
| TRUE PP5V_S0            | 7 8 27 42 47 52 57 58 |
| TRUE LPC_AD<0>          | 23 45 47              |
| TRUE LPC_AD<1>          | 23 45 47              |
| TRUE LPC_FRAME_L        | 23 45 47              |
| TRUE PM_CLKRUN_L        | 25 45 47              |
| TRUE PCI_FW_GNT_L       | 24 38 47 83           |
| TRUE SMC_TMS            | 45 46 47              |
| TRUE DEBUG_RESET_L      | 28 47                 |
| TRUE SMC_TRST_L         | 45 47                 |
| TRUE SMC_TDO            | 45 46 47              |
| TRUE SMC_MD1            | 45 47                 |
| TRUE SMC_TX_L           | 43 45 46 47           |
| TRUE FWH_INIT_L         | 47                    |
| TRUE PCI_CLK33M_LPCPLUS | 30 47 84              |
| TRUE LPC_AD<2>          | 23 45 47              |
| TRUE LPC_AD<3>          | 23 45 47              |
| TRUE INT_SERRIO         | 25 45 47              |
| TRUE PM_SUS_STAT_L      | 25 45 46 47           |
| TRUE SMC_TDI            | 45 46 47              |
| TRUE SMC_TCK            | 45 46 47              |
| TRUE SMC_RESET_L        | 45 46 47              |
| TRUE SMC_NMI            | 45 47                 |
| TRUE SMC_RX_L           | 43 45 46 47           |
| TRUE LINDACARD_GPIO     | 25 47                 |

### Left I/O Power Connector

| FUNC_TEST      | Pin                             |
|----------------|---------------------------------|
| TRUE PPBUS_G3H | 8 40 49 56 57 58 59 60 61 62 63 |
| TRUE GND       |                                 |

Request for at least 10 GND test points  
NOTE: 10 additional GND test points are called out separately in these notes.

### RTC Battery Connector

| FUNC_TEST           | Pin |
|---------------------|-----|
| TRUE PPVBATT_G3_RTC | 28  |
| TRUE GND            |     |

### Current Sense Calibration

| FUNC_TEST              | Pin                   |
|------------------------|-----------------------|
| TRUE ISENSE_CAL_EN     | 45 49                 |
| TRUE PP5V_S3           | 7 8 44 46 49 53 57 78 |
| TRUE PPVCORE_S0_NB_GFX | 8 18 32 69            |
| TRUE PPVCORE_S0_CPU    | 8 11 12 49            |
| TRUE PPVCORE_GPU       | 8 49 67 74            |
| TRUE GND               |                       |

2 TPs per

6 TPs, 2 with each of above TP pairs

### Left Clutch Barrel Connector

| FUNC_TEST         | Pin                   |
|-------------------|-----------------------|
| TRUE PP5V_S3      | 7 8 44 46 49 53 57 78 |
| TRUE USB_CAMERA_N | 24 44 82              |
| TRUE USB_CAMERA_P | 24 44 82              |
| TRUE PP5V_S3      | 7 8 44 46 49 53 57 78 |
| TRUE USB_WWAN_N   | 24 44 82              |
| TRUE USB_WWAN_P   | 24 44 82              |

### Left ALS Connector

| FUNC_TEST      | Pin                 |
|----------------|---------------------|
| TRUE PP3V3_S3  | 8 36 38 48 50 51 53 |
| TRUE ALS_GAIN  | 45 53 78            |
| TRUE LTALS_OUT | 53 78               |
| TRUE GND       |                     |

### Thermal Diode Connectors

| FUNC_TEST           | Pin   |
|---------------------|-------|
| TRUE HSTHMSNS_D_P   | 51 87 |
| TRUE HSTHMSNS_D_N   | 51    |
| TRUE RSFTHMSNS_D_P  | 51 87 |
| TRUE RSFTHMSNS_D_N  | 51    |
| TRUE CPUTHMSNS_D2_P | 51 87 |
| TRUE CPUTHMSNS_D2_N | 51    |

CPUTHMSNS can not be supported due to layout constraints

### Other Func Test Points

| FUNC_TEST        | Pin      |
|------------------|----------|
| TRUE PM_SYSRST_L | 25 28 45 |
| TRUE SMC_ONOFF_L | 45 46 78 |

## System Validation TPs

| FUNC_TEST             | Pin         |
|-----------------------|-------------|
| TRUE CPU_PWRGD        | 10 13 23 79 |
| TRUE CPU_DPSLP_L      | 7 10 23 79  |
| TRUE PM DPRSLPVR      | 16 25 58 79 |
| TRUE CPU_DPSLP_L      | 7 10 23 79  |
| TRUE PM_LAN_ENABLE    | 25 45       |
| TRUE PCI_RST_L        | 24 28       |
| TRUE PM_RSMRST_L      | 25 45       |
| TRUE PM_SB_PWROK      | 9 25 28     |
| TRUE SB_RTC_RST_L     | 23 28       |
| TRUE PM_STPCPU_L      | 25 29 30    |
| TRUE PM_STPPCI_L      | 25 29 30    |
| TRUE VR_PWRGD_CLKEN   | 25 28       |
| TRUE VR_PWRGOOD_DELAY | 9 16 28 58  |
| TRUE FSB_CPURST_L     | 10 13 14 79 |
| TRUE FSB_CPUSLP_L     | 10 14 79    |
| TRUE FSB_DPWR_L       | 10 14 79    |
| TRUE NB_SB_SYNC_L     | 16 25       |

| FUNC_TEST                | Pin                        |
|--------------------------|----------------------------|
| TRUE IMVP_VR_ON          | 45 58                      |
| TRUE IMVP DPRSLPVR       | 58 79                      |
| TRUE PM_SLP_S3_L         | 25 35 36 40 45 49 57 62 65 |
| TRUE PM_S4_STATE_L       | 25 34 43 45 57 65          |
| TRUE PM_SLP_S5_L         | 25 45 46                   |
| TRUE PM_ENET_EN          | 36 61 65                   |
| TRUE P1V5P1V05S0_PGOOD   | 61 63 65                   |
| TRUE CPU DPRSTP_L        | 10 16 23 58 79             |
| TRUE IMVP6_VID<6..0>     | 12 58 79                   |
| TRUE PLT_RST_L           | 24 28 77                   |
| TRUE NB_RESET_L          | 16 28                      |
| TRUE GPU_RESET_L         | 28 66                      |
| TRUE SMC_LRESET_L        | 28 45                      |
| TRUE CPU_STPCLK_L        | 10 23 79                   |
| TRUE FSB_CLK_NB_P        | 14 29 30 84                |
| TRUE FSB_CLK_NB_N        | 14 29 30 84                |
| TRUE NB_CLKREQ0_L        | 16 29                      |
| TRUE NB_CLK100M_PCIE_P   | 16 29 30 84                |
| TRUE NB_CLK100M_PCIE_N   | 16 29 30 84                |
| TRUE NB_CLK96M_DOT_P     | 84                         |
| TRUE NB_CLK96M_DOT_N     | 84                         |
| TRUE NB_CLK100M_DPLLSS_P | 16 22 29 30 84             |
| TRUE NB_CLK100M_DPLLSS_N | 16 22 29 30 84             |
| TRUE CPU_THERMTRIP_R     | 33                         |

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## Functional / ICT Test

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

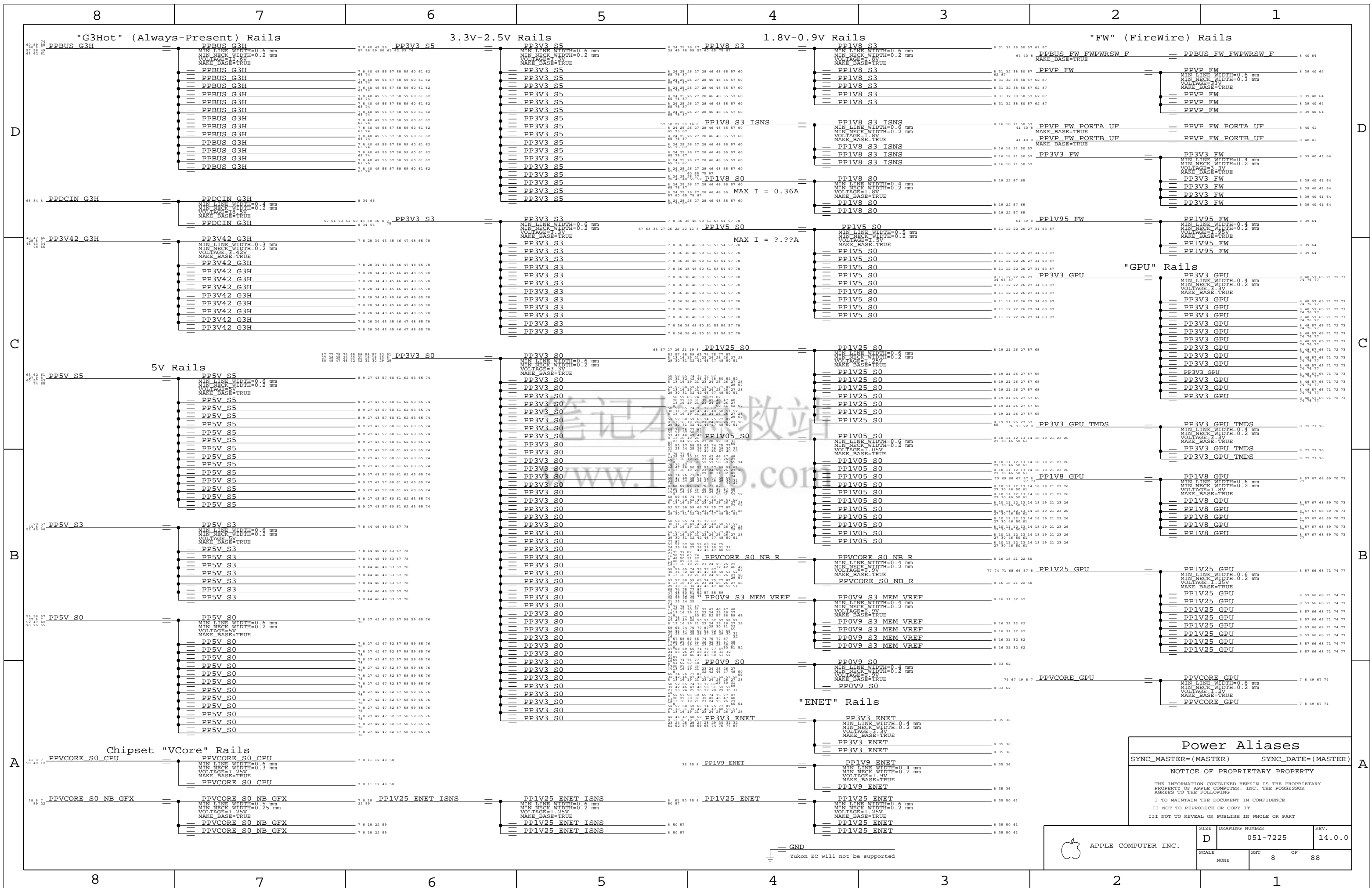
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| SCALE | SHT | OF | REV.   |
|-------|-----|----|--------|
| NONE  | 7   | 88 | 14.0.0 |



**Power Aliases**

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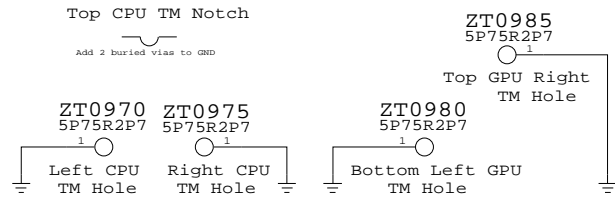
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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 8    | 88             |        |

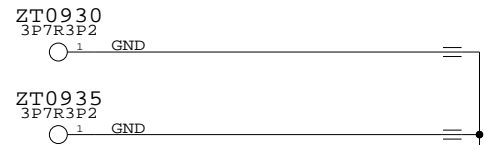
GND  
 Yukon EC will not be supported



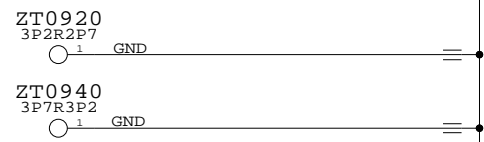
### Thermal Module Holes



### RAM Door (Torx) Holes

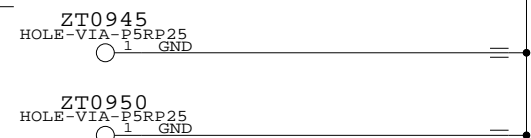


### Frame Holes



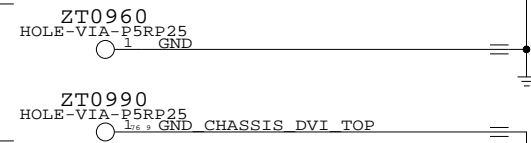
### Board Edge Notches

(Can't be PTH)

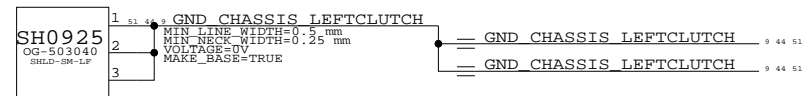
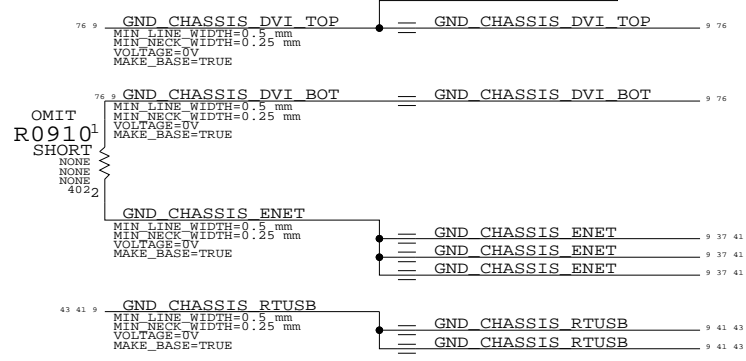


### Tooling Holes

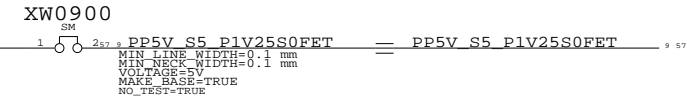
(Can't be PTH)



### Chassis GNDs

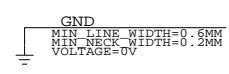


|               |                                      |    |                    |               |
|---------------|--------------------------------------|----|--------------------|---------------|
| 28 25 9 7     | PM_SB_PWROK<br>MAKE_BASE=TRUE        | == | PM_SB_PWROK        | 7 9 25 28     |
| 58 28 16 9 7  | VR_PWRGOOD_DELAY<br>MAKE_BASE=TRUE   | == | VR_PWRGOOD_DELAY   | 7 9 16 28 58  |
| 54 45 9       | SMC_SMS_INT<br>MAKE_BASE=TRUE        | == | SMC_SMS_INT        | 9 45 54       |
| 84 66 30 29 9 | PEG_CLK100M_GPU_P<br>MAKE_BASE=TRUE  | == | PEG_CLK100M_GPU_P  | 9 29 30 66 84 |
| 84 66 30 29 9 | PEG_CLK100M_GPU_N<br>MAKE_BASE=TRUE  | == | PEG_CLK100M_GPU_N  | 9 29 30 66 84 |
| 77 59 9       | PM_ALL_NBGFX_PGOOD<br>MAKE_BASE=TRUE | == | PM_ALL_NBGFX_PGOOD | 9 59 77       |
| 59 16 9       | GFX_VR_EN<br>MAKE_BASE=TRUE          | == | GFX_VR_EN          | 9 16 59       |
| 59            | GFXIMVP6_VID<4..0><br>MAKE_BASE=TRUE | == | GFX_VID<4..0>      | 16            |
| 31 9          | TP_MEM_A_A<15><br>MAKE_BASE=TRUE     | == | TP_MEM_A_A<15>     | 9 31          |
| 32 9          | TP_MEM_B_A<15><br>MAKE_BASE=TRUE     | == | TP_MEM_B_A<15>     | 9 32          |
| 82 24 9       | TP_USB_EXTCP<br>MAKE_BASE=TRUE       | == | TP_USB_EXTCP       | 9 24 82       |
| 82 24 9       | TP_USB_EXTCN<br>MAKE_BASE=TRUE       | == | TP_USB_EXTCN       | 9 24 82       |



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### Digital Ground



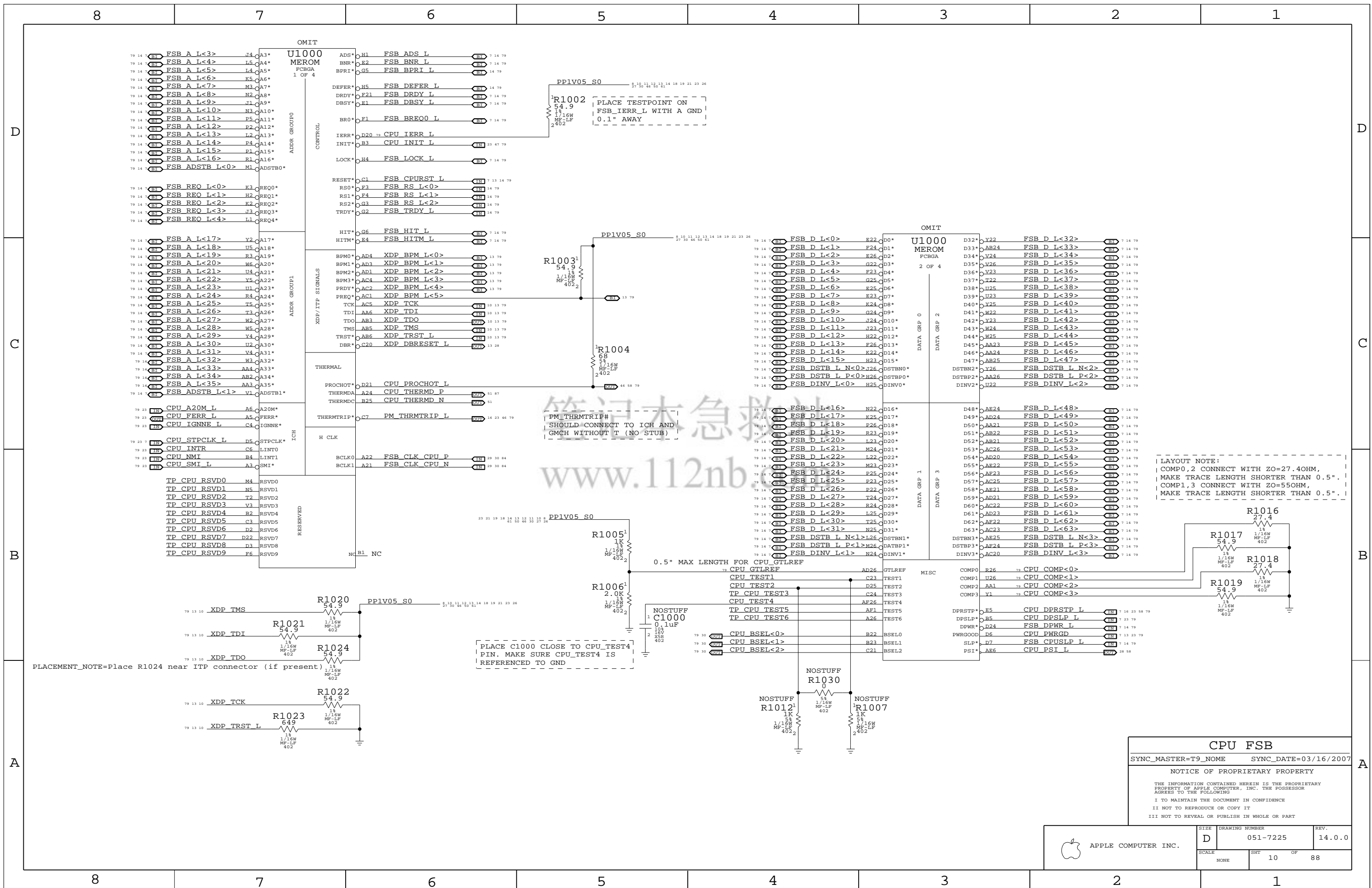
### Signal Aliases

SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/23/2006

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| SCALE               | SHT  | OF             |        |
| NONE                | 9    | 88             |        |



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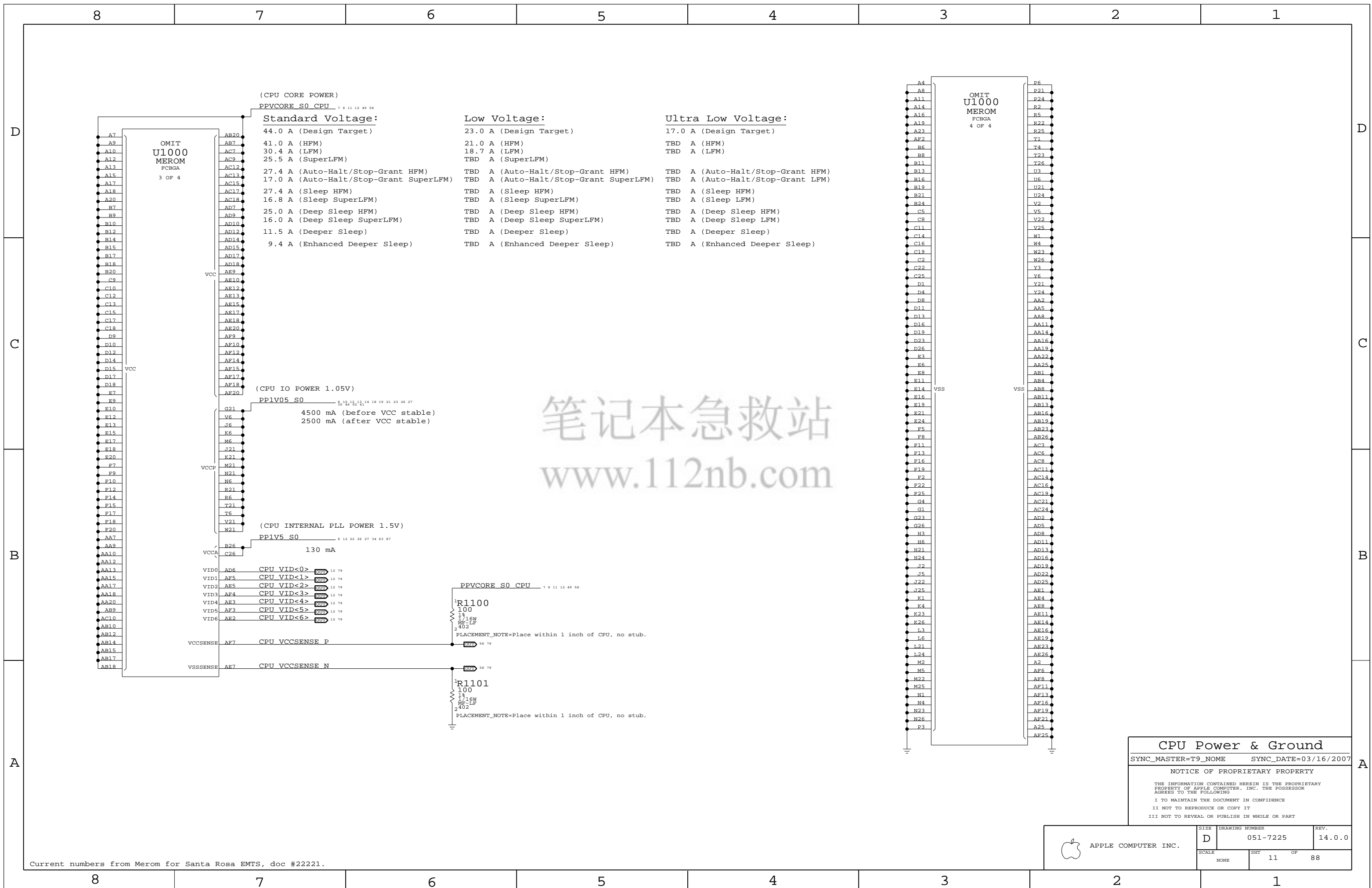
LAYOUT NOTE:  
COMPO,2 CONNECT WITH ZO=27.4OHM,  
MAKE TRACE LENGTH SHORTER THAN 0.5".  
COMPL,3 CONNECT WITH ZO=55OHM,  
MAKE TRACE LENGTH SHORTER THAN 0.5".

PLACE C1000 CLOSE TO CPU TEST4  
PIN. MAKE SURE CPU TEST4 IS  
REFERENCED TO GND

PLACEMENT\_NOTE=Place R1024 near ITP connector (if present)

**CPU FSB**  
SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007  
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| SCALE               | SHT  | OF             |        |
| NONE                | 10   | 88             |        |



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**CPU Power & Ground**  
SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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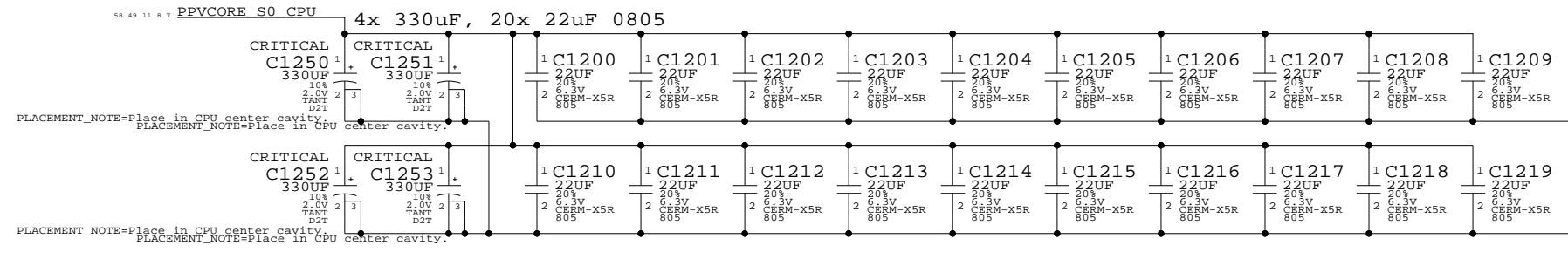
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|                     | D            | 051-7225       | 14.0.0 |
| SCALE               | SHT 11 OF 88 |                |        |
| NONE                |              |                |        |

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

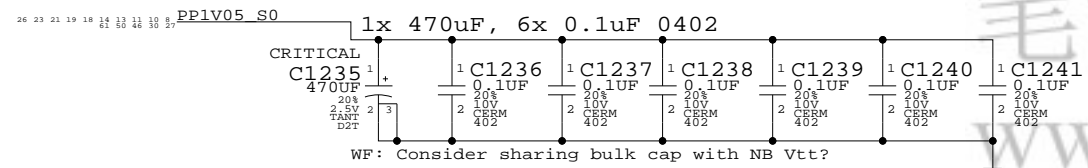
### CPU VCORE HF AND BULK DECOUPLING



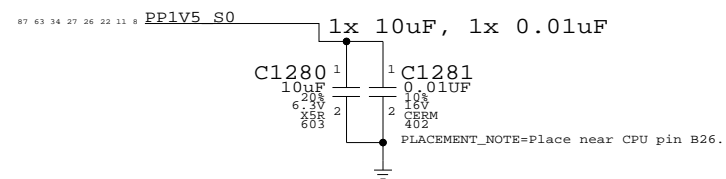
### CPU VCORE VID CONNECTIONS

79 11 CPU VID<0..6> == IMVP6 VID<0..6> 7 58 79  
MAKE\_BASE=TRUE

### VCCP (CPU I/O) DECOUPLING



### VCCA (CPU AVdd) DECOUPLING



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### CPU Decoupling & VID

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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| SCALE               | SHT  | OF             |        |
| NONE                | 12   | 88             |        |

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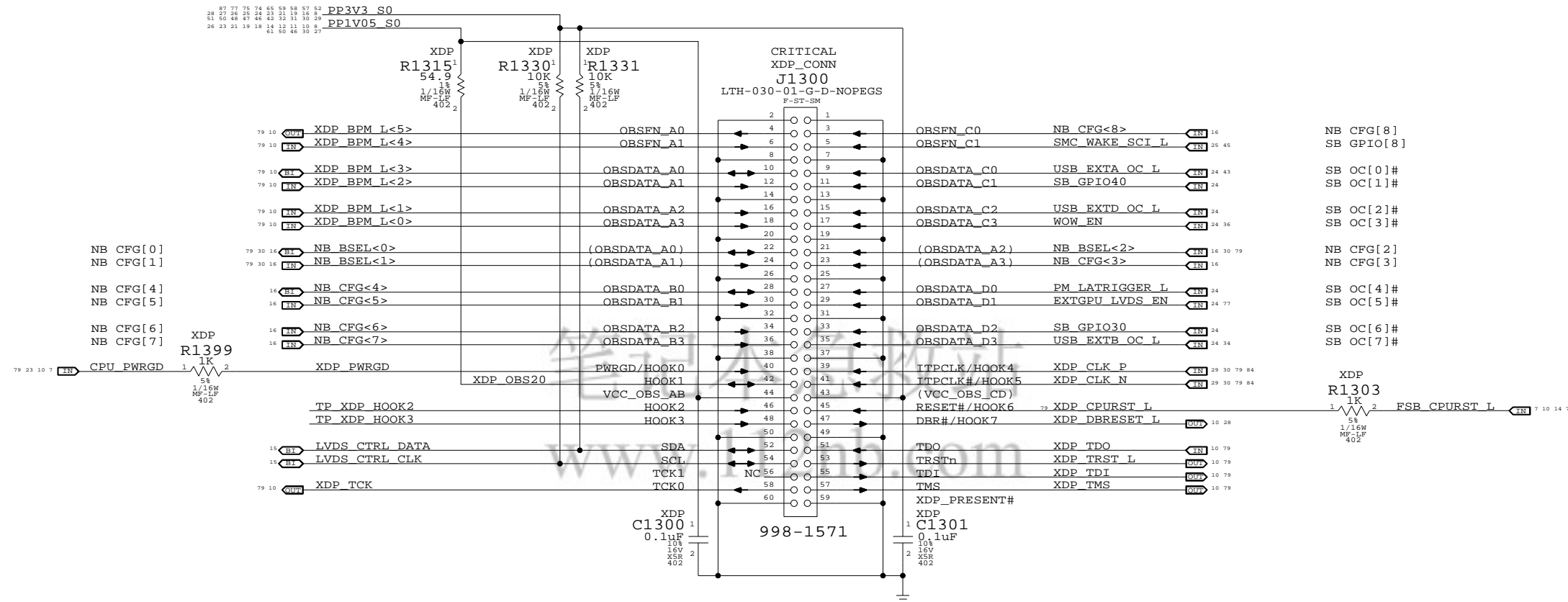
3

2

1

# Mini-XDP Connector

NOTE: This is not the standard XDP pinout.  
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



← Direction of XDP module  
Please avoid any obstructions  
on even-numbered side of J1300

eXtended Debug Port (XDP)  
 SYNC\_MASTER=T9\_NOME    SYNC\_DATE=12/12/2006  
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| SCALE               |      | SHT            | OF     |
| NONE                |      | 13             | 88     |

8

7

6

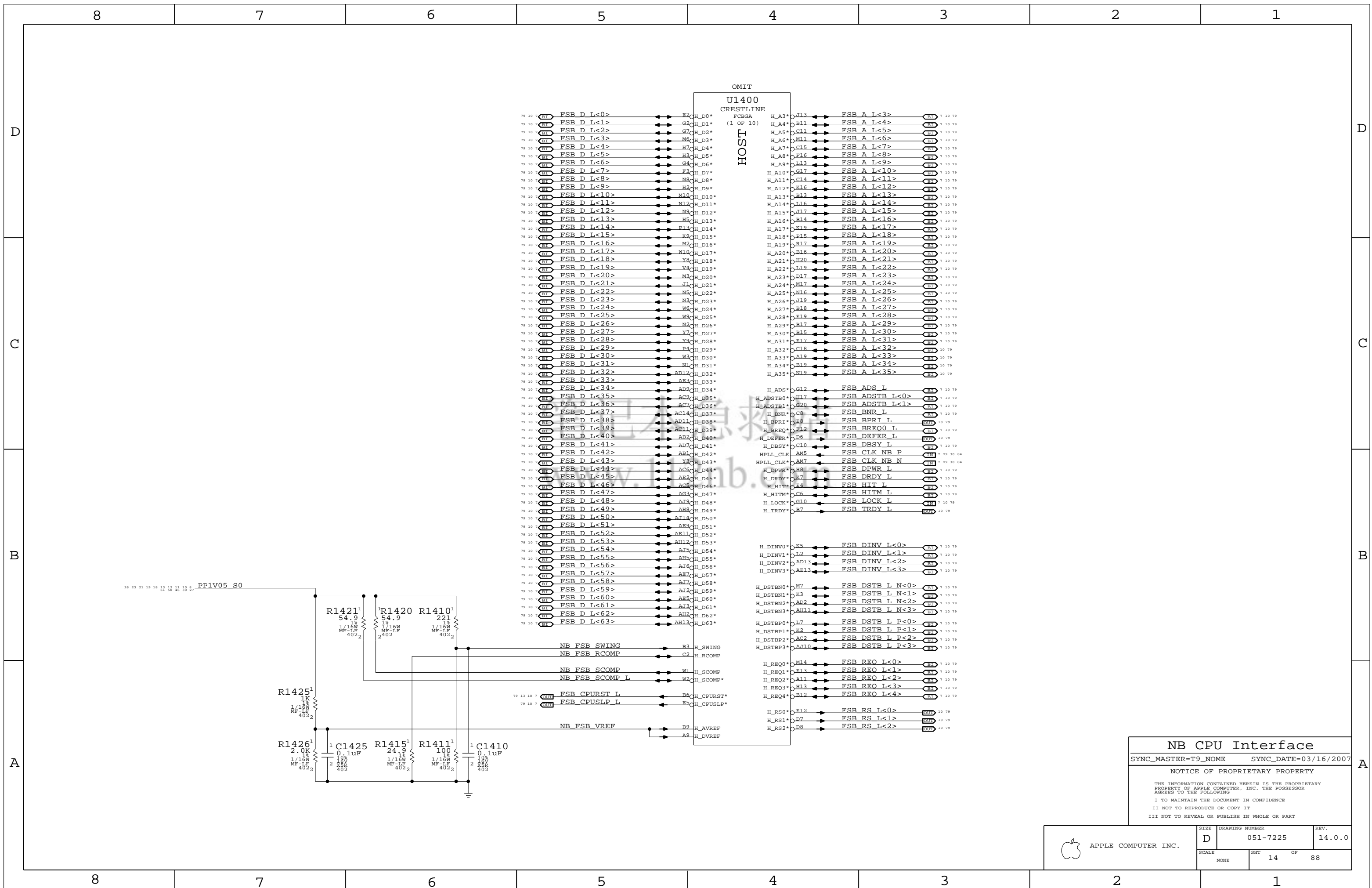
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1



NB CPU Interface  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 14   | 88             |        |

LVDS Disable

Can leave all signals NC if LVDS is not implemented. Tie VCC\_TX\_LVDS and VCCA\_LVDS to GND.

If SDVO is used, VCCD\_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD\_LVDS to GND also.

Note: SR DG says to tie LVDS\_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx\_DAC and TVx\_RTN to GND. Must power all TVDAC rails. VCCA\_TVx\_DAC and VCCA\_DAC\_BG can share filtering with VCCA\_CRT\_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA\_CRT.

CRT & TV-Out Disable

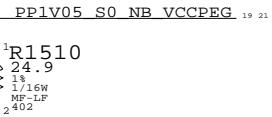
Tie TVx\_DAC, TVx\_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT\_TVO\_IREF to GND. Can tie the following rails to GND: VCCA\_CRT\_DAC, VCCA\_DAC\_BG, VCCA\_TVx\_DAC, VCCD\_CRT, VCCD\_QDAC and VCC\_SYNC.

NOTE: Must keep VDDC\_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT\_DDC\*, L\_CTRL\*, L\_DDC\*, SDVO\_CTRL\* and TV\_DCONSELx to GND.

Tie DPLL\_REF\_CLK and DPLL\_REF\_SSCLK to GND. Tie DPLL\_REF\_CLK\* and DPLL\_REF\_SSCLK\* to VCC (VCore). Tie VCCA\_DPLLA and VCCA\_DPLLB to VCC (VCore). Tie VCC\_AXG and VCC\_AXG\_NCTF to GND. Leave GFX\_VID<3..0> and GFX\_VR\_EN as NC.



SDVO Alternate Function

SDVO\_TVCLKIN#
SDVO\_INT#
SDVO\_FLDSTALL#

SDVO\_TVCLKIN
SDVO\_INT
SDVO\_FLDSTALL

SDVOB\_RED#
SDVOB\_GREEN#
SDVOB\_BLUE#
SDVOB\_CLKN
SDVOC\_RED#
SDVOC\_GREEN#
SDVOC\_BLUE#
SDVOC\_CLKN

SDVOB\_RED
SDVOB\_GREEN
SDVOB\_BLUE
SDVOB\_CLKP
SDVOC\_RED
SDVOC\_GREEN
SDVOC\_BLUE
SDVOC\_CLKP

NB PEG / Video Interfaces
SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

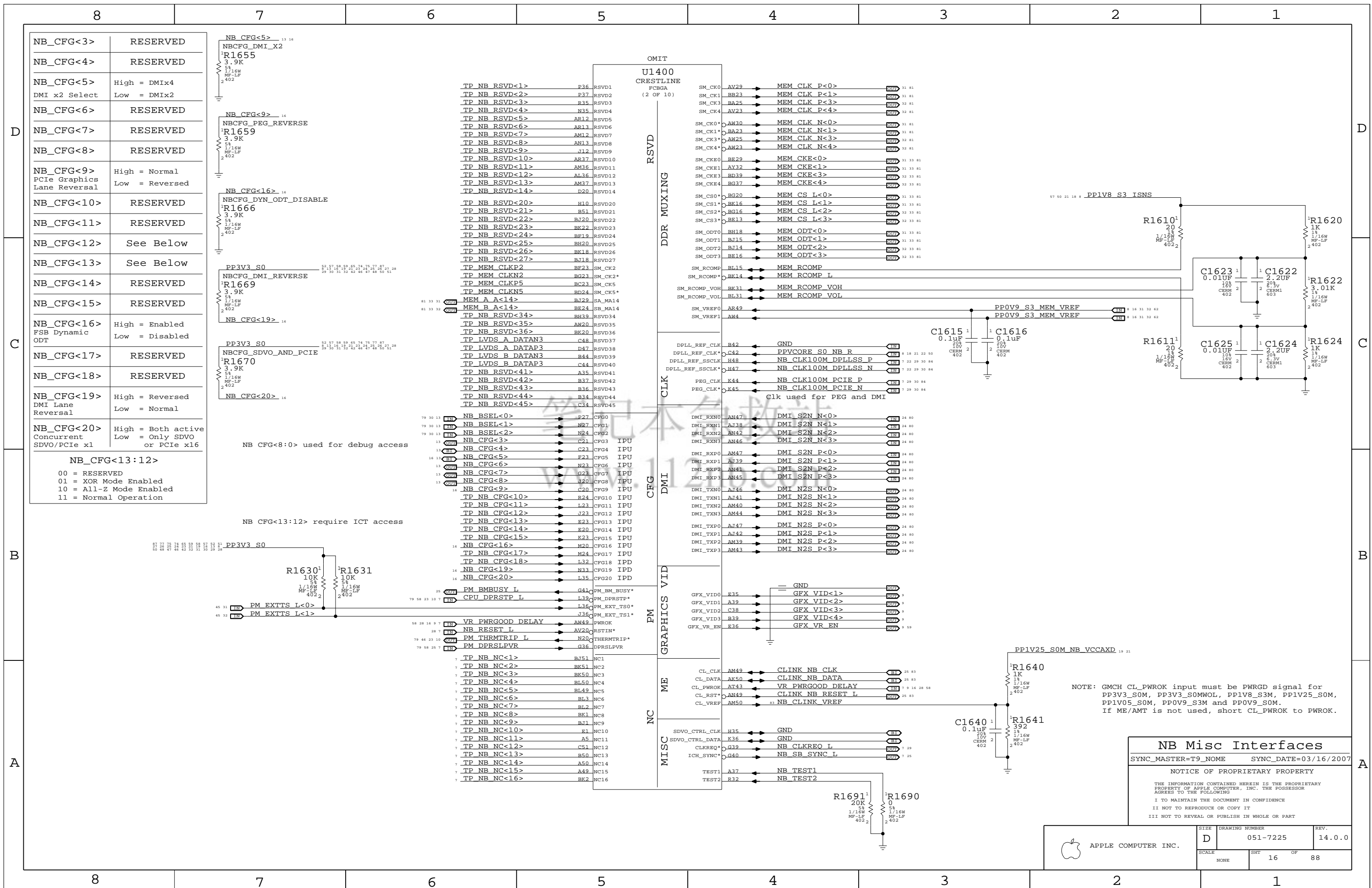
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Table with columns: SCALE, DRAWING NUMBER, SHEET, OF, REV. Values: NONE, 051-7225, 15, 88, 14.0.0

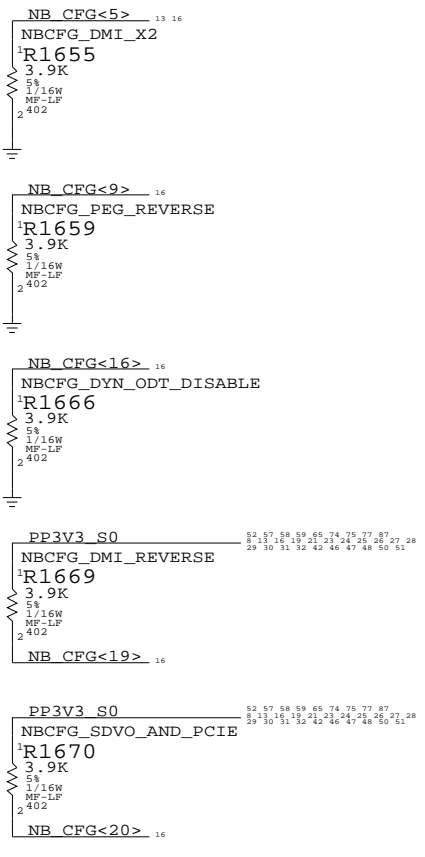


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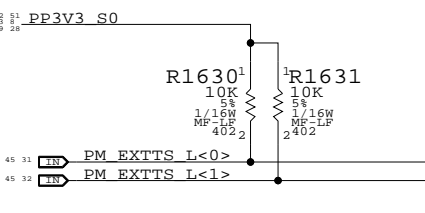
|            |   |
|------------|---|
| NB_CFG<3>  | RESERVED  |
| NB_CFG<4>  | RESERVED  |
| NB_CFG<5>  | High = DMIx4<br>Low = DMIx2   |
| NB_CFG<6>  | RESERVED  |
| NB_CFG<7>  | RESERVED  |
| NB_CFG<8>  | RESERVED  |
| NB_CFG<9>  | High = Normal<br>PCIe Graphics Lane Reversal<br>Low = Reversed                  |
| NB_CFG<10> | RESERVED  |
| NB_CFG<11> | RESERVED  |
| NB_CFG<12> | See Below   |
| NB_CFG<13> | See Below   |
| NB_CFG<14> | RESERVED  |
| NB_CFG<15> | RESERVED  |
| NB_CFG<16> | High = Enabled<br>FSB Dynamic ODT<br>Low = Disabled                             |
| NB_CFG<17> | RESERVED  |
| NB_CFG<18> | RESERVED  |
| NB_CFG<19> | High = Reversed<br>DMI Lane Reversal<br>Low = Normal                            |
| NB_CFG<20> | High = Both active<br>Concurrent<br>Low = Only SDVO<br>SDVO/PCIe x1 or PCIe x16 |

NB\_CFG<13:12>  
 00 = RESERVED  
 01 = XOR Mode Enabled  
 10 = All-Z Mode Enabled  
 11 = Normal Operation



NB\_CFG<8:0> used for debug access

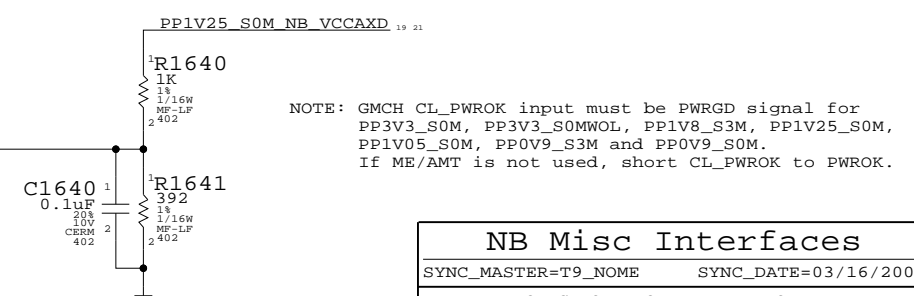
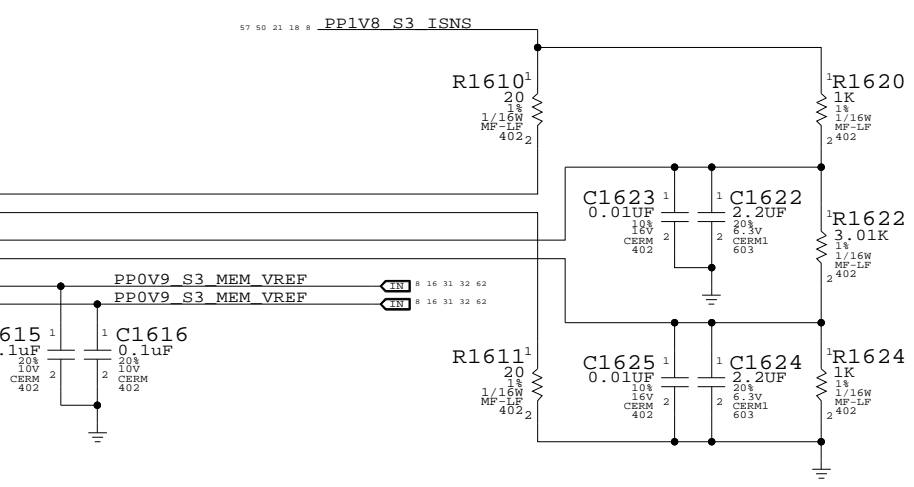
NB\_CFG<13:12> require ICT access



U1400 CRESTLINE (2 OF 10)

|                  |      |             |
|------------------|------|-------------|
| TP NB_RSVD<1>    | P36  | RSVD1       |
| TP NB_RSVD<2>    | P37  | RSVD2       |
| TP NB_RSVD<3>    | R35  | RSVD3       |
| TP NB_RSVD<4>    | N35  | RSVD4       |
| TP NB_RSVD<5>    | AR12 | RSVD5       |
| TP NB_RSVD<6>    | AR13 | RSVD6       |
| TP NB_RSVD<7>    | AM12 | RSVD7       |
| TP NB_RSVD<8>    | AM13 | RSVD8       |
| TP NB_RSVD<9>    | J12  | RSVD9       |
| TP NB_RSVD<10>   | AR37 | RSVD10      |
| TP NB_RSVD<11>   | AM36 | RSVD11      |
| TP NB_RSVD<12>   | AL36 | RSVD12      |
| TP NB_RSVD<13>   | AM37 | RSVD13      |
| TP NB_RSVD<14>   | D20  | RSVD14      |
| TP NB_RSVD<20>   | H10  | RSVD20      |
| TP NB_RSVD<21>   | B51  | RSVD21      |
| TP NB_RSVD<22>   | BJ20 | RSVD22      |
| TP NB_RSVD<23>   | BK22 | RSVD23      |
| TP NB_RSVD<24>   | BF19 | RSVD24      |
| TP NB_RSVD<25>   | BH20 | RSVD25      |
| TP NB_RSVD<26>   | BK18 | RSVD26      |
| TP NB_RSVD<27>   | BJ18 | RSVD27      |
| TP MEM_CLKP2     | BE23 | SM_CK2*     |
| TP MEM_CLKN2     | EG23 | SM_CK2*     |
| TP MEM_CLKP5     | BC23 | SM_CK5*     |
| TP MEM_CLKN5     | BD24 | SM_CK5*     |
| MEM A A<14>      | BJ29 | SM_MA14     |
| MEM B A<14>      | BE24 | SB_MA14     |
| TP NB_RSVD<34>   | BH39 | RSVD34      |
| TP NB_RSVD<35>   | AW20 | RSVD35      |
| TP NB_RSVD<36>   | BK20 | RSVD36      |
| TP LVDS A DATAP3 | C48  | RSVD37      |
| TP LVDS A DATAP3 | D47  | RSVD38      |
| TP LVDS B DATAP3 | B44  | RSVD39      |
| TP LVDS B DATAP3 | C44  | RSVD40      |
| TP NB_RSVD<41>   | A35  | RSVD41      |
| TP NB_RSVD<42>   | B37  | RSVD42      |
| TP NB_RSVD<43>   | B36  | RSVD43      |
| TP NB_RSVD<44>   | B34  | RSVD44      |
| TP NB_RSVD<45>   | C34  | RSVD45      |
| NB_BSEL<0>       | P27  | CFG0        |
| NB_BSEL<1>       | N27  | CFG1        |
| NB_BSEL<2>       | N24  | CFG2        |
| NB_CFG<3>        | C21  | CFG3 IPU    |
| NB_CFG<4>        | C23  | CFG4 IPU    |
| NB_CFG<5>        | F23  | CFG5 IPU    |
| NB_CFG<6>        | N23  | CFG6 IPU    |
| NB_CFG<7>        | G23  | CFG7 IPU    |
| NB_CFG<8>        | J20  | CFG8 IPU    |
| NB_CFG<9>        | C20  | CFG9 IPU    |
| TP NB_CFG<10>    | R24  | CFG10 IPU   |
| TP NB_CFG<11>    | L23  | CFG11 IPU   |
| TP NB_CFG<12>    | J23  | CFG12 IPU   |
| TP NB_CFG<13>    | E23  | CFG13 IPU   |
| TP NB_CFG<14>    | E20  | CFG14 IPU   |
| TP NB_CFG<15>    | K23  | CFG15 IPU   |
| NB_CFG<16>       | M20  | CFG16 IPU   |
| TP NB_CFG<17>    | M24  | CFG17 IPU   |
| TP NB_CFG<18>    | L32  | CFG18 IPD   |
| NB_CFG<19>       | N33  | CFG19 IPD   |
| NB_CFG<20>       | L35  | CFG20 IPD   |
| PM_BMBUSY L      | G41  | PM_BMBUSY*  |
| CPU DPRSTP L     | L39  | PM_DPRSTP*  |
|                  | L36  | PM_EXT_TSO* |
|                  | J36  | PM_EXT_TS1* |
| VR_PWRGOOD DELAY | AW49 | PWROK       |
| NB_RESET L       | AV20 | RSTIN*      |
| PM_THRMTRIP L    | N20  | THERMTRIP*  |
| PM DPRSLPVR      | G36  | DPRSLPVR    |
| TP NB_NC<1>      | BJ51 | NC1         |
| TP NB_NC<2>      | BK51 | NC2         |
| TP NB_NC<3>      | BK50 | NC3         |
| TP NB_NC<4>      | BL50 | NC4         |
| TP NB_NC<5>      | BL49 | NC5         |
| TP NB_NC<6>      | BL3  | NC6         |
| TP NB_NC<7>      | BL2  | NC7         |
| TP NB_NC<8>      | BK1  | NC8         |
| TP NB_NC<9>      | BJ1  | NC9         |
| TP NB_NC<10>     | E1   | NC10        |
| TP NB_NC<11>     | A5   | NC11        |
| TP NB_NC<12>     | B50  | NC12        |
| TP NB_NC<13>     | C51  | NC13        |
| TP NB_NC<14>     | A50  | NC14        |
| TP NB_NC<15>     | A49  | NC15        |
| TP NB_NC<16>     | BK2  | NC16        |

|                 |      |                          |      |               |
|-----------------|------|--------------------------|------|---------------|
| SM_CK0          | AV29 | MEM_CLK P<0>             | 9090 | 31 81         |
| SM_CK1          | BB23 | MEM_CLK P<1>             | 9090 | 31 81         |
| SM_CK3          | BA25 | MEM_CLK P<3>             | 9090 | 32 81         |
| SM_CK4          | AV23 | MEM_CLK P<4>             | 9090 | 32 81         |
| SM_CK0*         | AW30 | MEM_CLK N<0>             | 9090 | 31 81         |
| SM_CK1*         | BA23 | MEM_CLK N<1>             | 9090 | 31 81         |
| SM_CK3*         | AW25 | MEM_CLK N<3>             | 9090 | 32 81         |
| SM_CK4*         | AW23 | MEM_CLK N<4>             | 9090 | 32 81         |
| SM_CKE0         | BE29 | MEM_CKE<0>               | 9090 | 31 33 81      |
| SM_CKE1         | AY32 | MEM_CKE<1>               | 9090 | 31 33 81      |
| SM_CKE3         | BD39 | MEM_CKE<3>               | 9090 | 32 33 81      |
| SM_CKE4         | BG37 | MEM_CKE<4>               | 9090 | 32 33 81      |
| SM_CSO*         | BG20 | MEM_CS L<0>              | 9090 | 31 33 81      |
| SM_CS1*         | BK16 | MEM_CS L<1>              | 9090 | 31 33 81      |
| SM_CS2*         | BG16 | MEM_CS L<2>              | 9090 | 32 33 81      |
| SM_CS3*         | BE13 | MEM_CS L<3>              | 9090 | 32 33 81      |
| SM_ODT0         | BH18 | MEM_ODT<0>               | 9090 | 31 33 81      |
| SM_ODT1         | BJ15 | MEM_ODT<1>               | 9090 | 31 33 81      |
| SM_ODT2         | BJ14 | MEM_ODT<2>               | 9090 | 32 33 81      |
| SM_ODT3         | BE16 | MEM_ODT<3>               | 9090 | 32 33 81      |
| SM_RCOMP        | BL15 | MEM_RCOMP                | 9090 |               |
| SM_RCOMP*       | BK14 | MEM_RCOMP L              | 9090 |               |
| SM_RCOMP_VOH    | BK11 | MEM_RCOMP_VOH            | 9090 |               |
| SM_RCOMP_VOL    | BL31 | MEM_RCOMP_VOL            | 9090 |               |
| SM_VREF0        | AR49 |                          | 9090 |               |
| SM_VREF1        | AW4  |                          | 9090 |               |
| DPLL_REF_CLK    | B42  | GND                      | 9090 |               |
| DPLL_REF_CLK*   | C42  | PPVCORE S0 NB R          | 9090 | 8 18 21 22 50 |
| DPLL_REF_SSCLK  | H48  | NB_CLK100M DPLLSS P      | 9090 | 7 22 29 30 84 |
| DPLL_REF_SSCLK* | H47  | NB_CLK100M DPLLSS N      | 9090 | 7 22 29 30 84 |
| PEG_CLK         | K44  | NB_CLK100M PCIE P        | 9090 | 7 29 30 84    |
| PEG_CLK*        | K45  | NB_CLK100M PCIE N        | 9090 | 7 29 30 84    |
|                 |      | Clk used for PEG and DMI |      |               |
| DMI_RXN0        | AN47 | DMI S2N N<0>             | 9090 | 24 80         |
| DMI_RXN1        | AT38 | DMI S2N N<1>             | 9090 | 24 80         |
| DMI_RXN2        | AN42 | DMI S2N N<2>             | 9090 | 24 80         |
| DMI_RXN3        | AN46 | DMI S2N N<3>             | 9090 | 24 80         |
| DMI_RXP0        | AM47 | DMI S2N P<0>             | 9090 | 24 80         |
| DMI_RXP1        | AT39 | DMI S2N P<1>             | 9090 | 24 80         |
| DMI_RXP2        | AN41 | DMI S2N P<2>             | 9090 | 24 80         |
| DMI_RXP3        | AN45 | DMI S2N P<3>             | 9090 | 24 80         |
| DMI_TXN0        | AT46 | DMI N2S N<0>             | 9090 | 24 80         |
| DMI_TXN1        | AT41 | DMI N2S N<1>             | 9090 | 24 80         |
| DMI_TXN2        | AM40 | DMI N2S N<2>             | 9090 | 24 80         |
| DMI_TXN3        | AM44 | DMI N2S N<3>             | 9090 | 24 80         |
| DMI_TXP0        | AT47 | DMI N2S P<0>             | 9090 | 24 80         |
| DMI_TXP1        | AT42 | DMI N2S P<1>             | 9090 | 24 80         |
| DMI_TXP2        | AM39 | DMI N2S P<2>             | 9090 | 24 80         |
| DMI_TXP3        | AM43 | DMI N2S P<3>             | 9090 | 24 80         |
| GFX_VID0        | E35  | GFX VID<1>               | 9090 | 9             |
| GFX_VID1        | A39  | GFX VID<2>               | 9090 | 9             |
| GFX_VID2        | C38  | GFX VID<3>               | 9090 | 9             |
| GFX_VID3        | B39  | GFX VID<4>               | 9090 | 9             |
| GFX_VR_EN       | E36  | GFX VR_EN                | 9090 | 9 9           |
| CL_CLK          | AM49 | CLINK NB_CLK             | 9090 | 25 83         |
| CL_DATA         | AK50 | CLINK NB_DATA            | 9090 | 25 83         |
| CL_PWROK        | AT43 | VR_PWRGOOD DELAY         | 9090 | 9 16 28 58    |
| CL_RST*         | AN49 | CLINK NB RESET L         | 9090 | 25 83         |
| CL_VREF         | AM50 | NB CLINK VREF            | 9090 | 25 83         |
| SDVO_CTRL_CLK   | H35  | GND                      | 9090 |               |
| SDVO_CTRL_DATA  | K36  | GND                      | 9090 |               |
| CLKREQ*         | G39  | NB_CLKREQ L              | 9090 | 7 29          |
| ICH_SYNC*       | G40  | NB_SB_SYNC L             | 9090 | 7 25          |
| TEST1           | A37  | NB TEST1                 | 9090 |               |
| TEST2           | R32  | NB TEST2                 | 9090 |               |



**NB Misc Interfaces**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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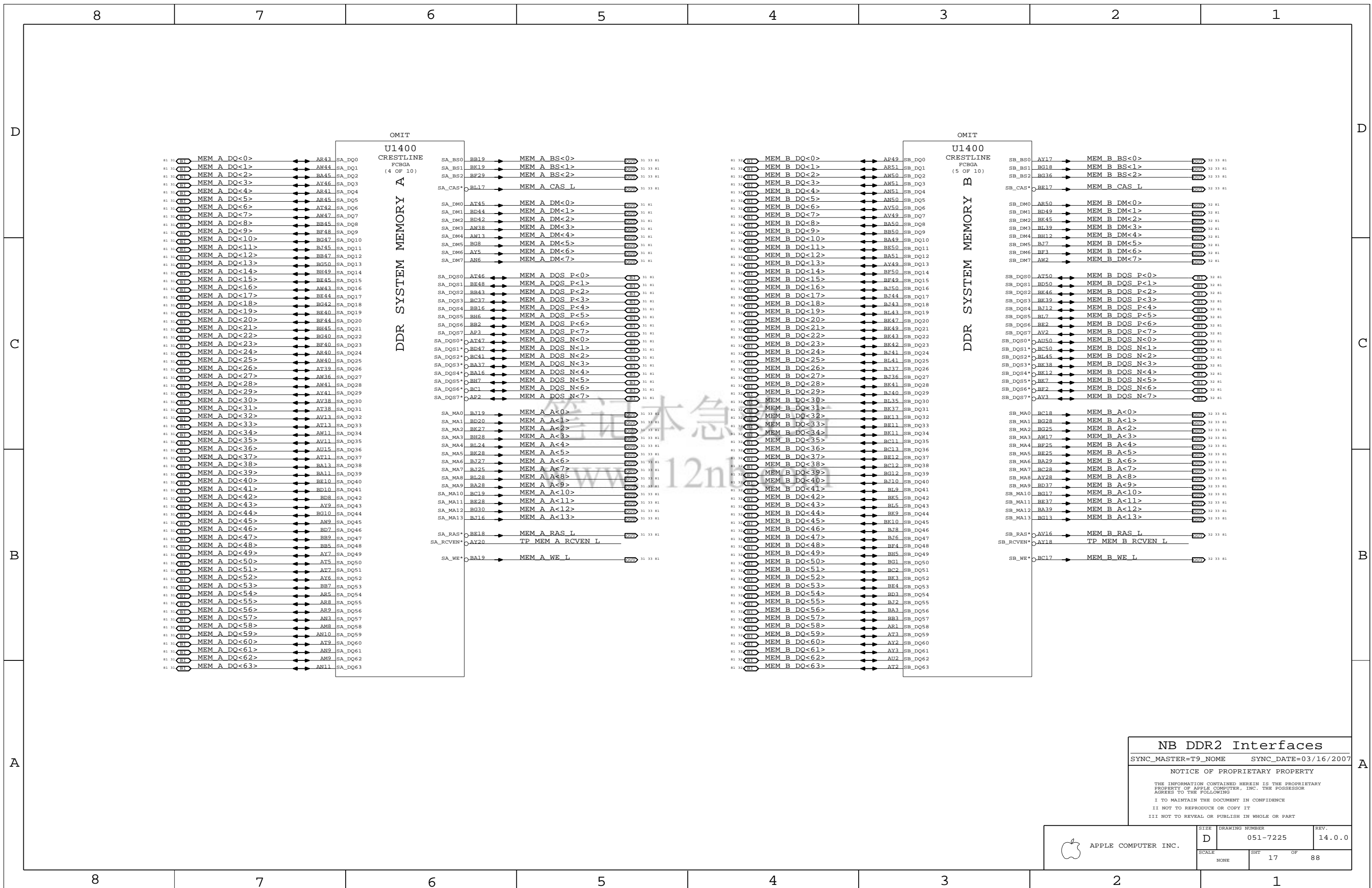
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| SCALE | NONE | SHT            | 16       | OF   | 88     |

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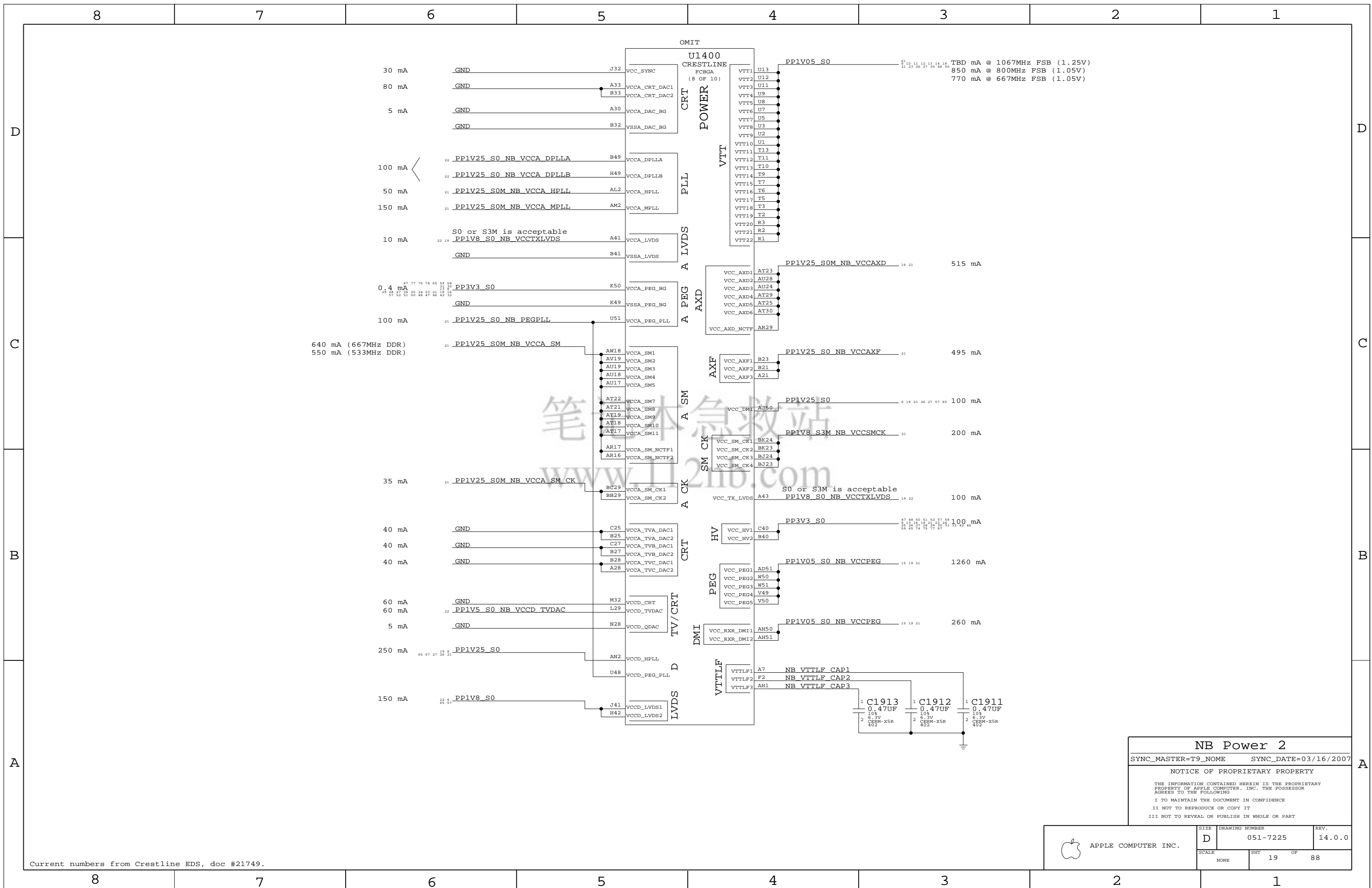


**NB DDR2 Interfaces**  
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Current numbers from Crestline EDS, doc #21749.

**NB Power 2**

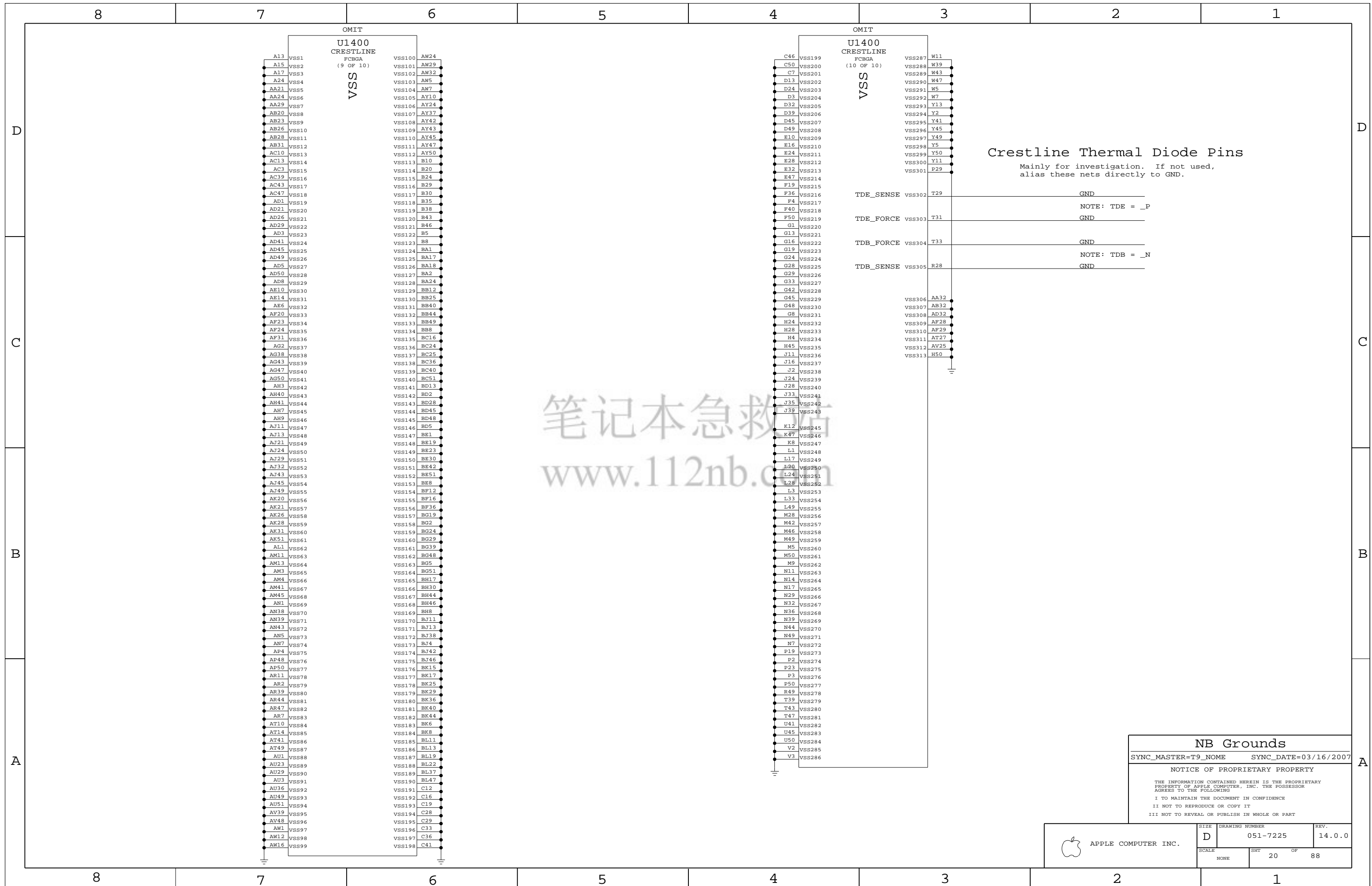
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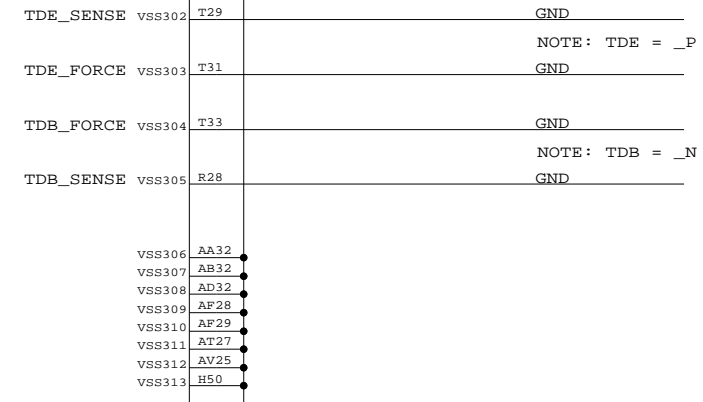
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|                     | SCALE<br>NONE    | SHEET<br>19                | OF<br>88       |



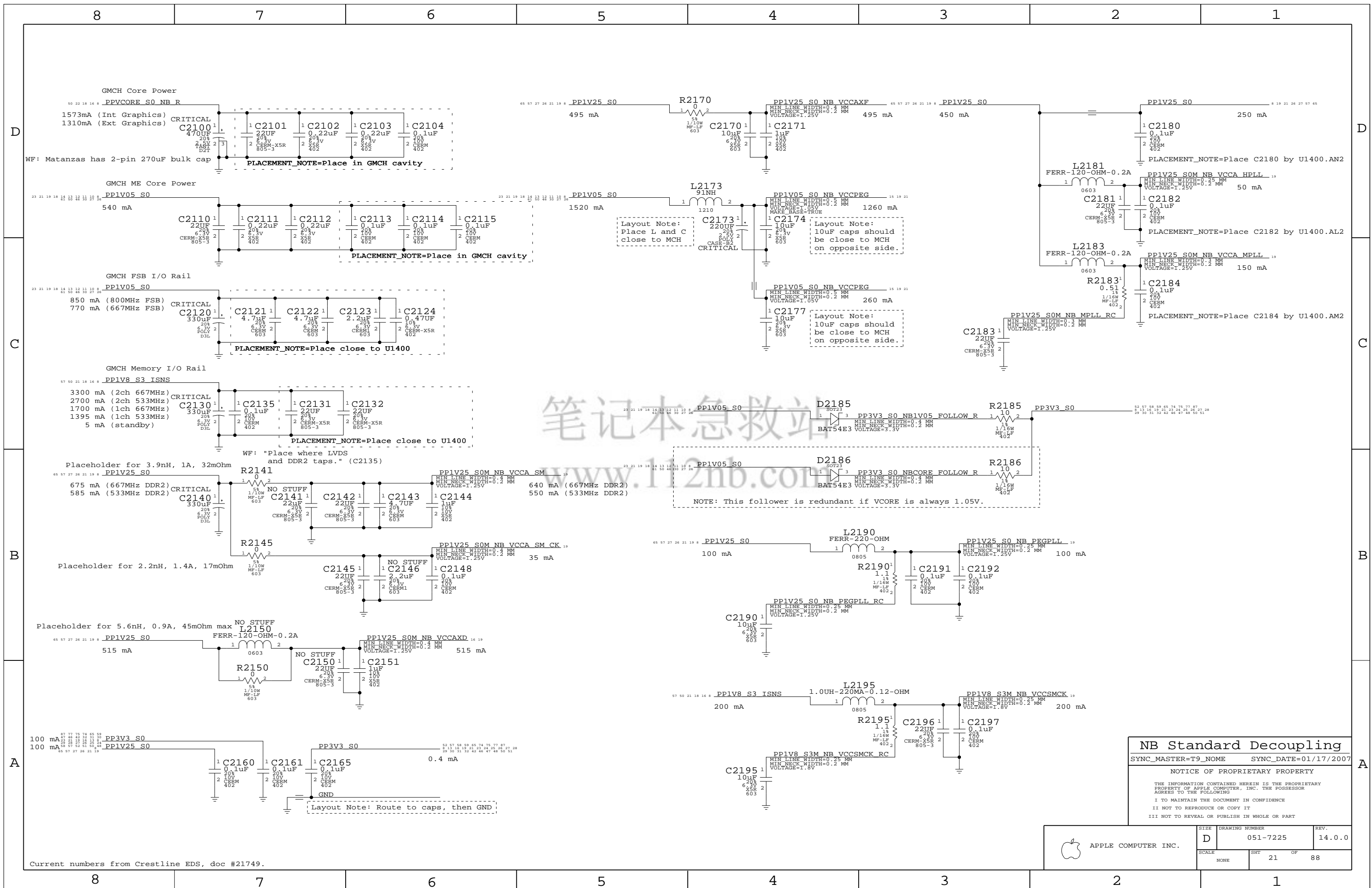
**Crestline Thermal Diode Pins**  
 Mainly for investigation. If not used,  
 alias these nets directly to GND.



**NB Grounds**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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| NONE                | 20   |                | 88     |



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**NB Standard Decoupling**

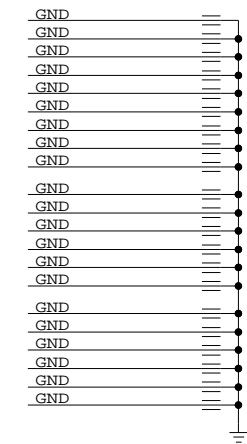
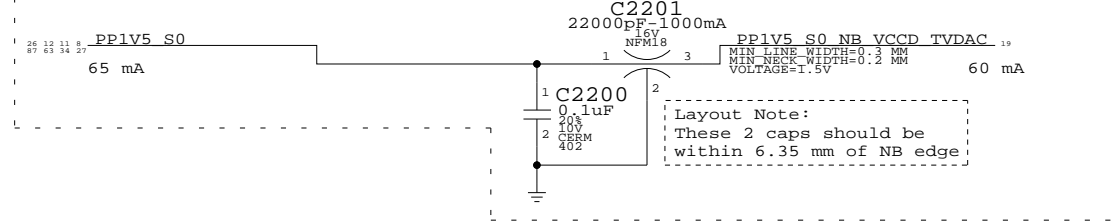
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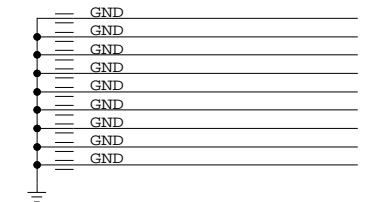
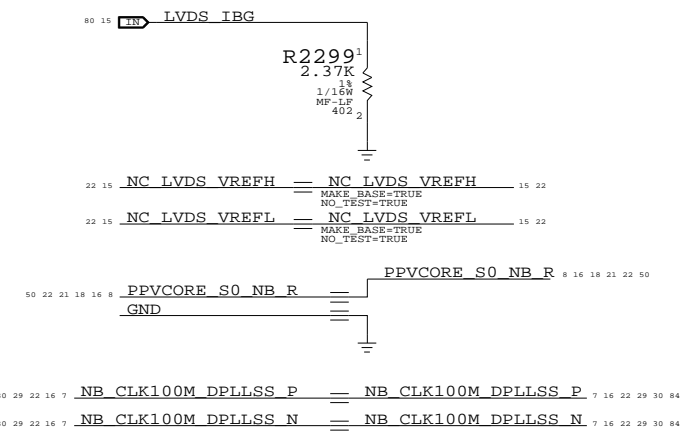
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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 21   | 88             |        |

NOTE: This filter is required even if using only external graphics.  
 VCCD\_TVDAC also powers internal thermal sensors.

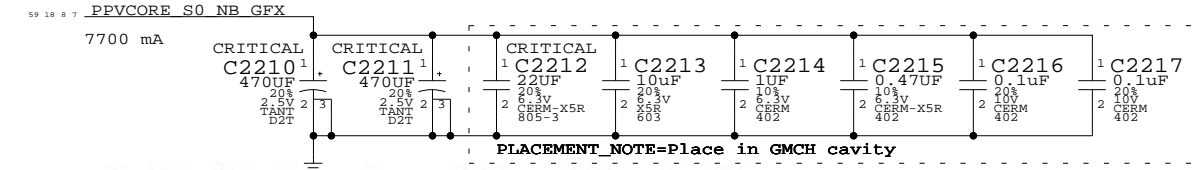


Crestline LVDS Support

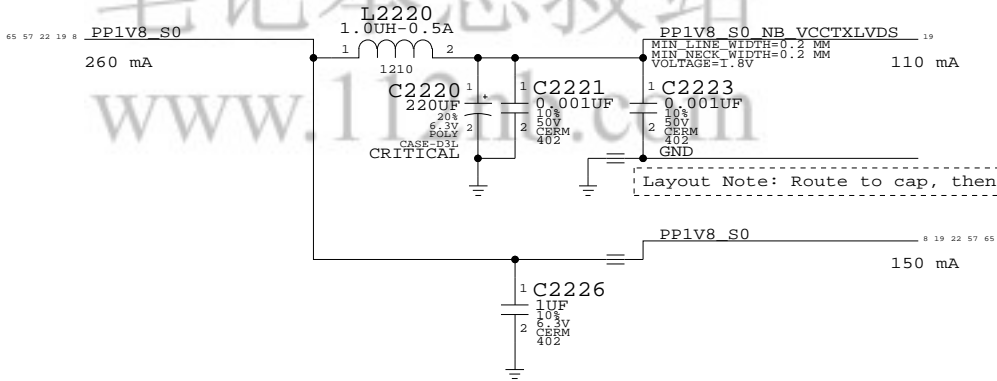


C

GMCH Graphics Core Power

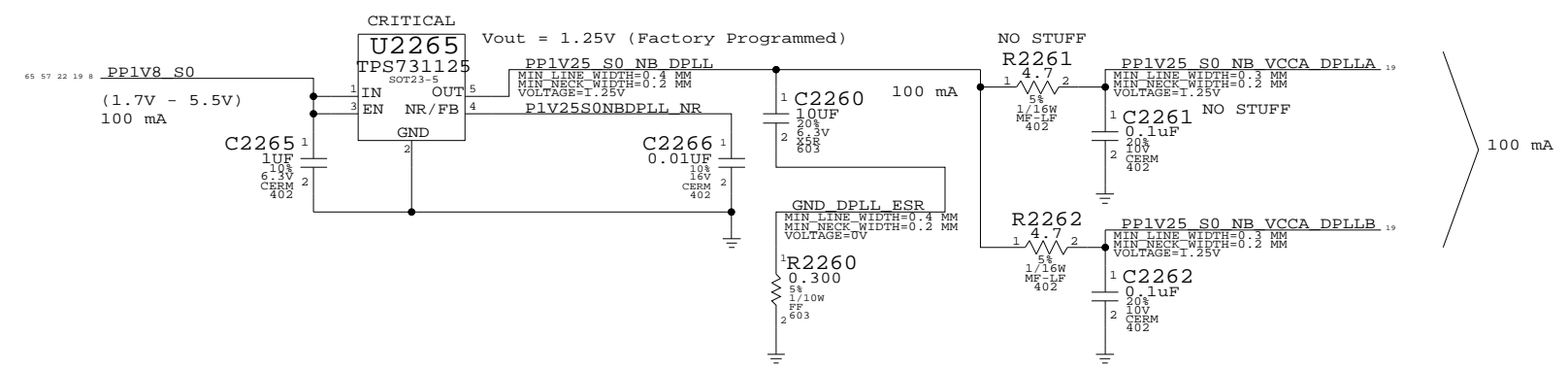


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B

A



NB Graphics Decoupling

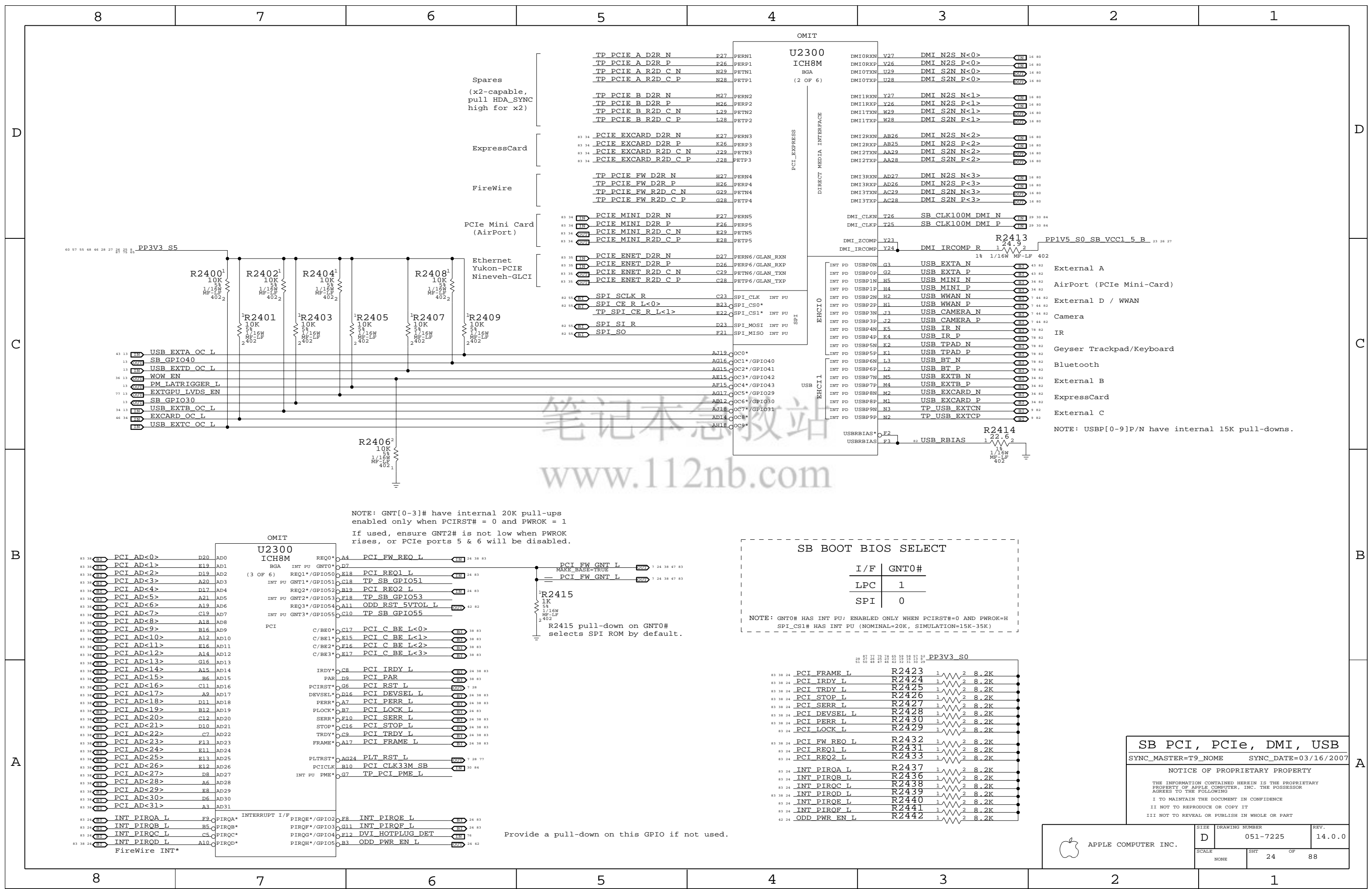
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             | REV.   |
| NONE                | 22   | 88             |        |





NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

| I/F | GNT0# |
|-----|-------|
| LPC | 1     |
| SPI | 0     |

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H  
SPI\_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

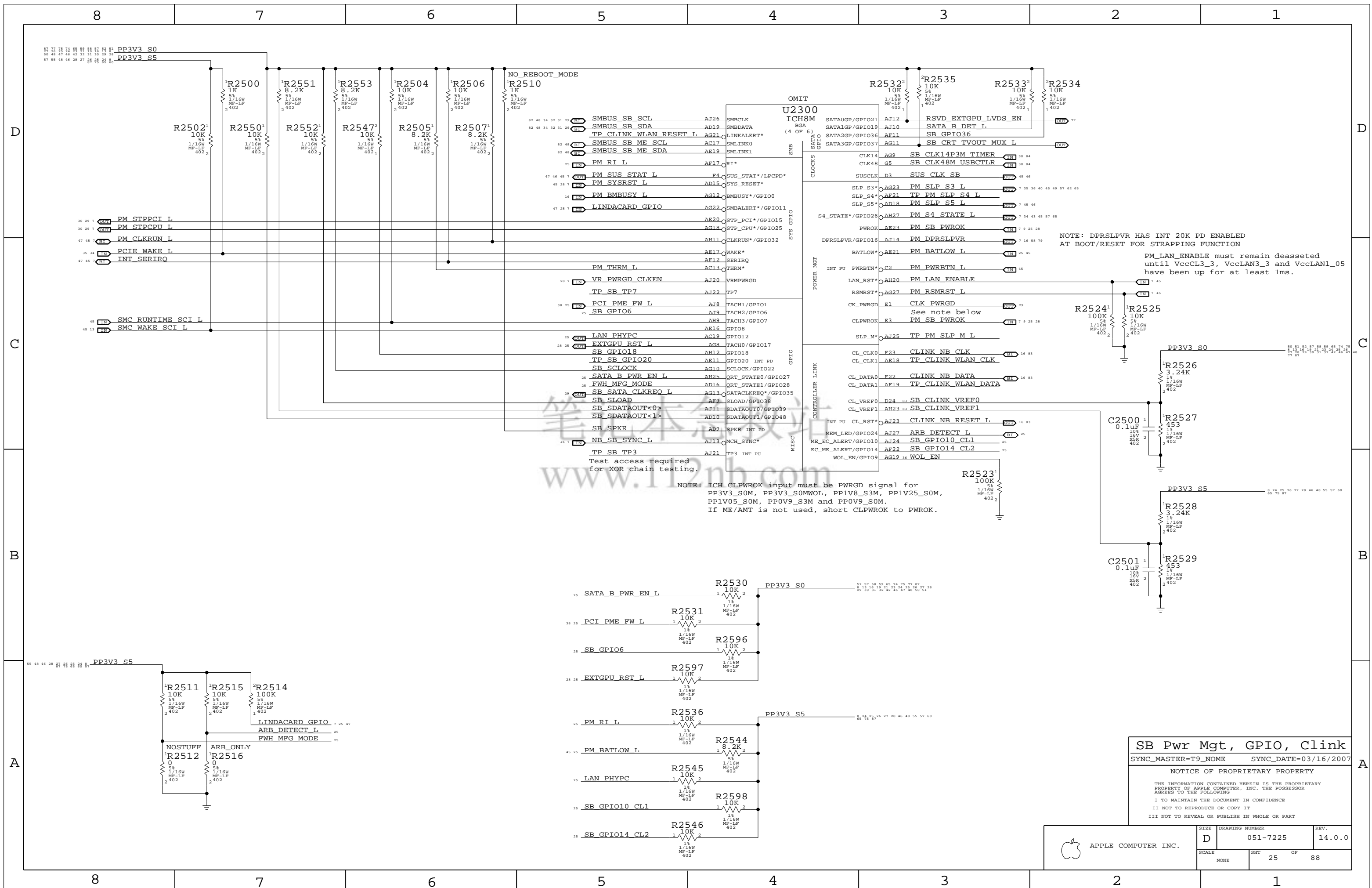
| Component    | Value        |
|--------------|--------------|
| PCI FRAME L  | R2423 1 8.2K |
| PCI IRDY L   | R2424 1 8.2K |
| PCI TRDY L   | R2425 1 8.2K |
| PCI STOP L   | R2426 1 8.2K |
| PCI SERR L   | R2427 1 8.2K |
| PCI DEVSEL L | R2428 1 8.2K |
| PCI PERR L   | R2430 1 8.2K |
| PCI LOCK L   | R2429 1 8.2K |
| PCI FW REO L | R2432 1 8.2K |
| PCI REQ1 L   | R2431 1 8.2K |
| PCI REQ2 L   | R2433 1 8.2K |
| INT PIRQA L  | R2437 1 8.2K |
| INT PIROB L  | R2436 1 8.2K |
| INT PIROC L  | R2438 1 8.2K |
| INT PIROD L  | R2439 1 8.2K |
| INT PIROE L  | R2440 1 8.2K |
| INT PIROF L  | R2441 1 8.2K |
| ODD PWR EN L | R2442 1 8.2K |

**SB PCI, PCIe, DMI, USB**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION  
 PM\_LAN\_ENABLE must remain deasserted until VccCL3\_3, VccLAN3\_3 and VccLAN1\_05 have been up for at least 1ms.

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3\_S0M, PP3V3\_S0MMWOL, PP1V8\_S3M, PP1V25\_S0M, PP1V05\_S0M, PP0V9\_S3M and PPOV9\_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

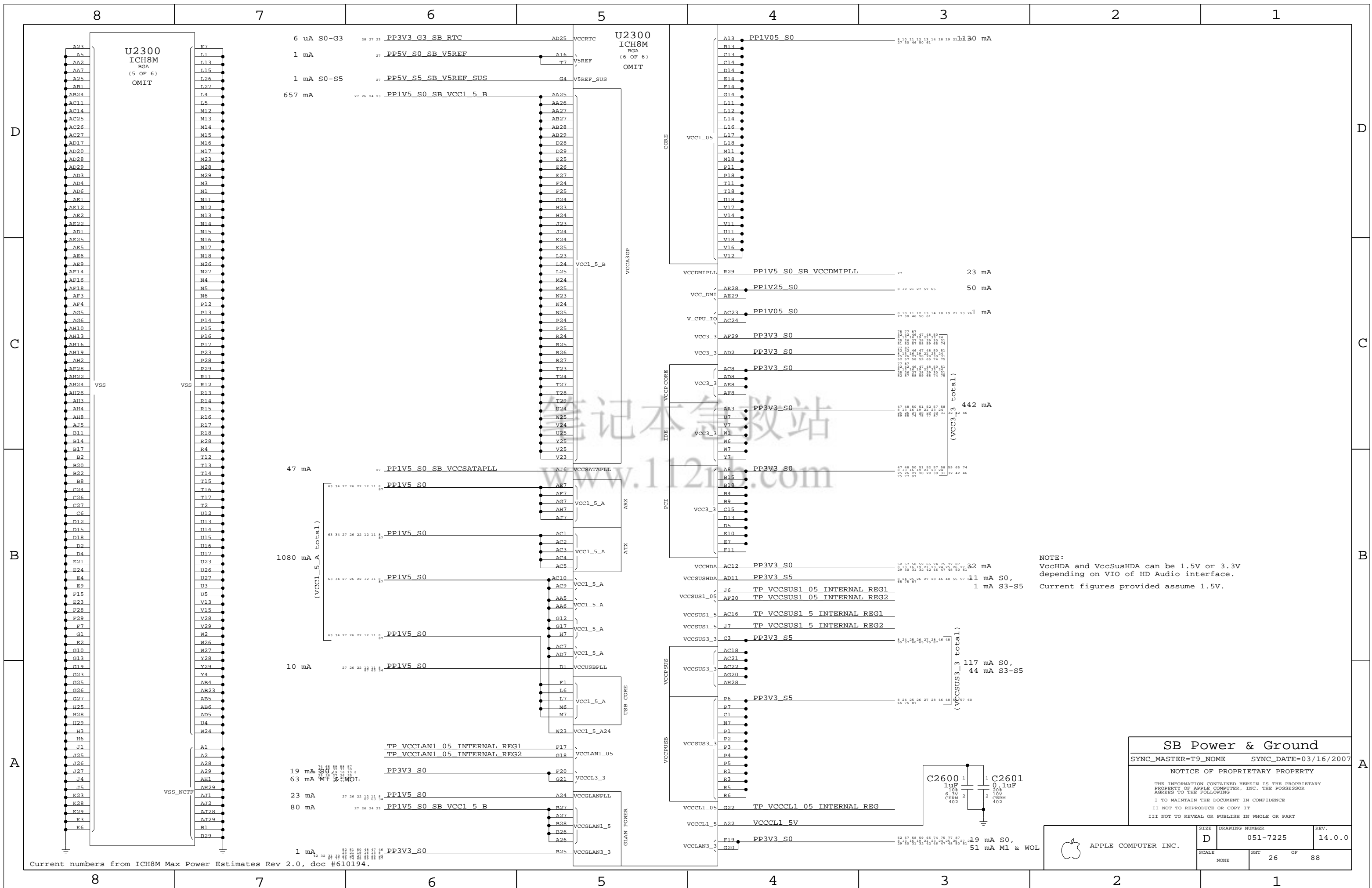
**SB Pwr Mgt, GPIO, Clink**

SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

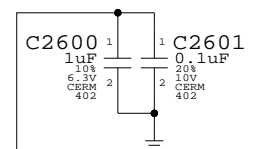
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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 25   | 88             |        |



Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

NOTE:  
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.  
Current figures provided assume 1.5V.



| SB Power & Ground   |                      |  |
|---|----------------------|--|
| SYNC_MASTER=T9_NOME   | SYNC_DATE=03/16/2007 |  |
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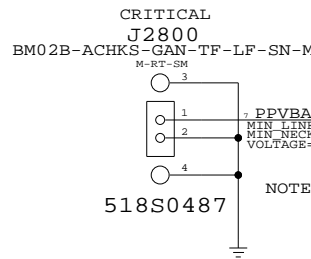
|               |           |                            |                |
|---------------|-----------|----------------------------|----------------|
| SCALE<br>NONE | SIZE<br>D | DRAWING NUMBER<br>051-7225 | REV.<br>14.0.0 |
|               | SHT<br>26 | OF<br>88                   |                |



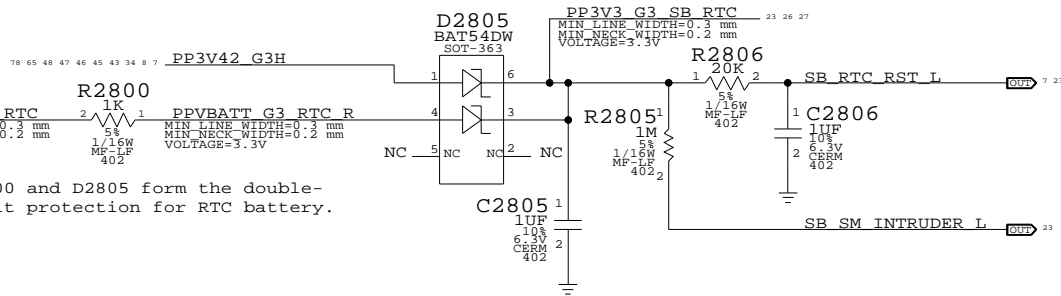
APPLE COMPUTER INC.



Coin-Cell Connector

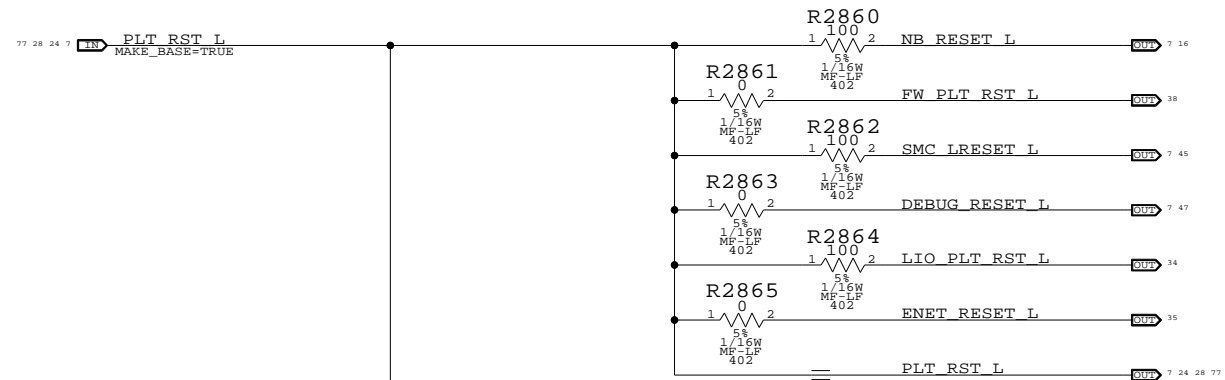


RTC Power Sources

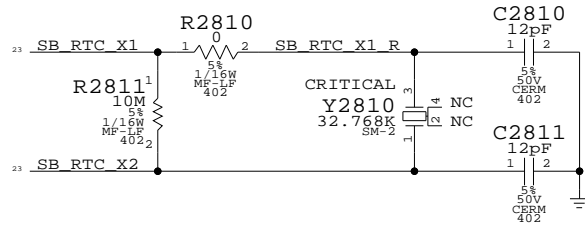


Platform Reset Connections

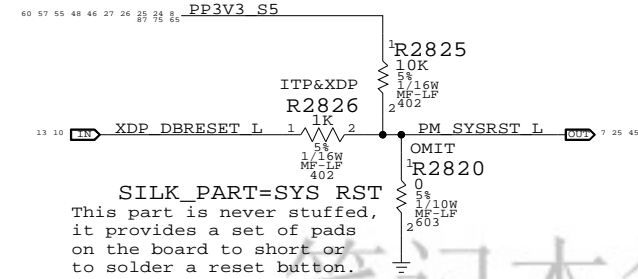
Unbuffered



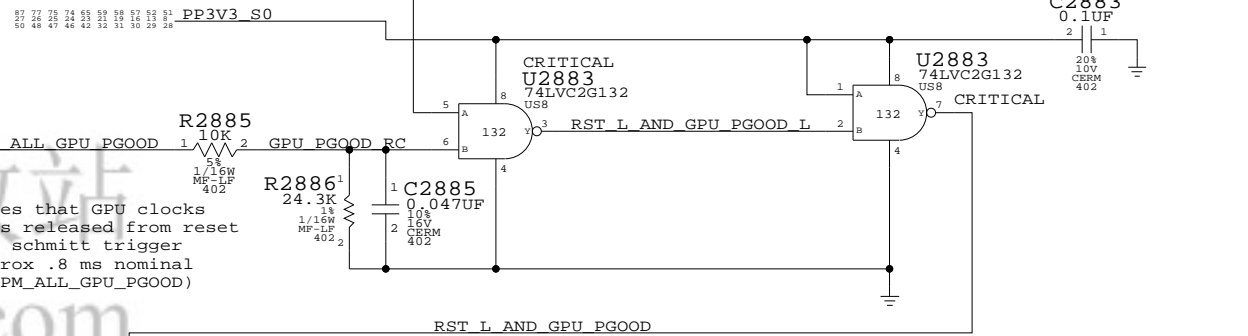
SB RTC Crystal



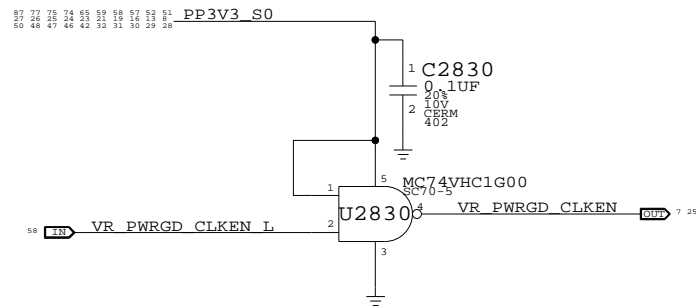
System Reset "Button"



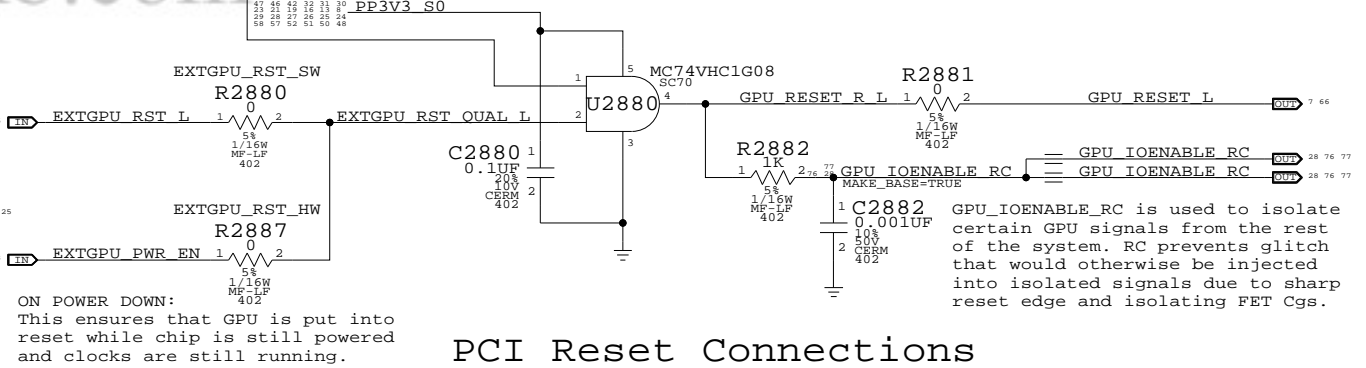
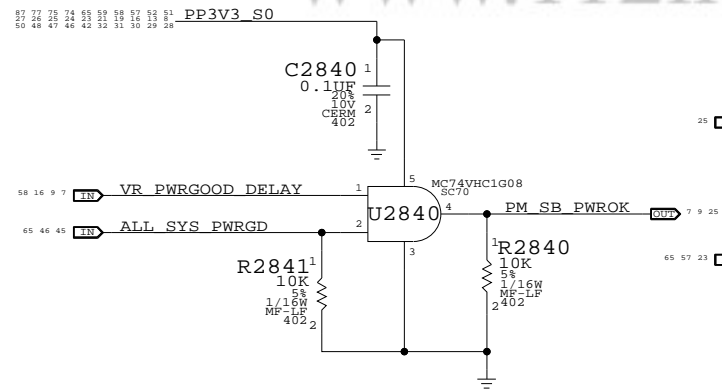
Muxed GFX GPU Reset Support



VRMPWRGD Inverter



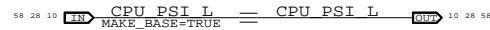
PWROK Circuit



PCI Reset Connections



CPU VCore ForcePSI



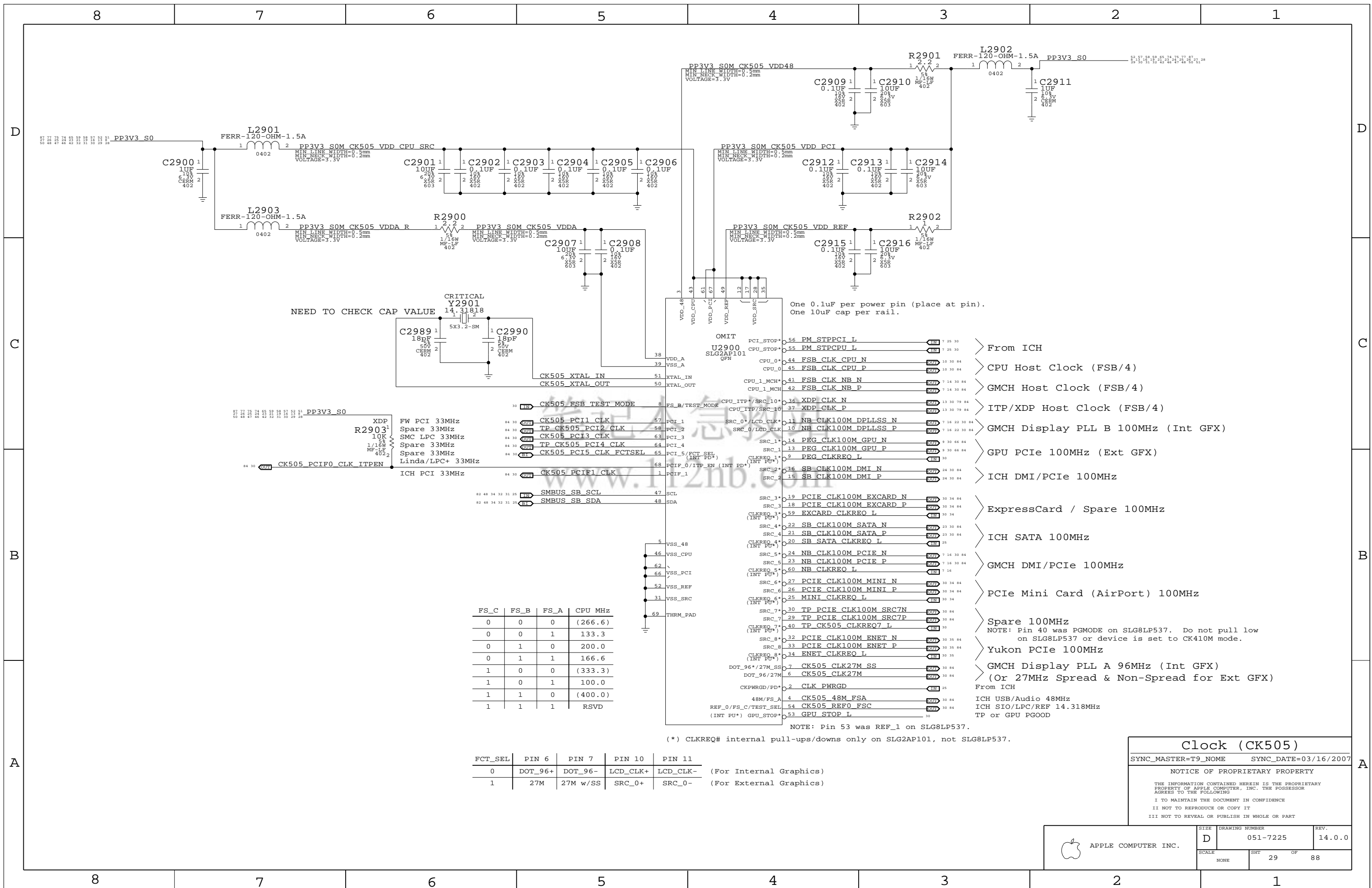
SB Misc

SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/24/2006

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| SCALE               | SHT  | OF             |        |
| NONE                | 28   | 88             |        |



NEED TO CHECK CAP VALUE

CRITICAL  
Y2901  
14.31818

C2989 18pF 50V CERM 402  
C2990 18pF 50V CERM 402

One 0.1uF per power pin (place at pin).  
One 10uF cap per rail.

| FS_C | FS_B | FS_A | CPU MHz |
|------|------|------|---------|
| 0    | 0    | 0    | (266.6) |
| 0    | 0    | 1    | 133.3   |
| 0    | 1    | 0    | 200.0   |
| 0    | 1    | 1    | 166.6   |
| 1    | 0    | 0    | (333.3) |
| 1    | 0    | 1    | 100.0   |
| 1    | 1    | 0    | (400.0) |
| 1    | 1    | 1    | RSVD    |

| FCT_SEL | PIN 6   | PIN 7    | PIN 10   | PIN 11   |
|---------|---------|----------|----------|----------|
| 0       | DOT_96+ | DOT_96-  | LCD_CLK+ | LCD_CLK- |
| 1       | 27M     | 27M w/SS | SRC_0+   | SRC_0-   |

(For Internal Graphics)  
(For External Graphics)

- > From ICH
- > CPU Host Clock (FSB/4)
- > GMCH Host Clock (FSB/4)
- > ITP/XDP Host Clock (FSB/4)
- > GMCH Display PLL B 100MHz (Int GFX)
- > GPU PCIe 100MHz (Ext GFX)
- > ICH DMI/PCIe 100MHz
- > ExpressCard / Spare 100MHz
- > ICH SATA 100MHz
- > GMCH DMI/PCIe 100MHz
- > PCIe Mini Card (AirPort) 100MHz
- > Spare 100MHz  
NOTE: Pin 40 was PGMODE on SLG8LP537. Do not pull low on SLG8LP537 or device is set to CK410M mode.
- > Yukon PCIe 100MHz
- > GMCH Display PLL A 96MHz (Int GFX)  
(Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- ICH USB/Audio 48MHz
- ICH SIO/LPC/REF 14.318MHz
- TP or GPU PGOOD

NOTE: Pin 53 was REF\_1 on SLG8LP537.

(\*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

**Clock (CK505)**

SYNC\_MASTER=T9\_NAME    SYNC\_DATE=03/16/2007

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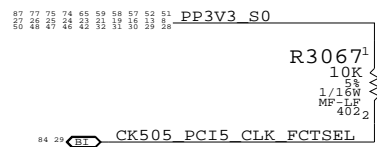
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 29   | 88             |        |

# CLK Termination

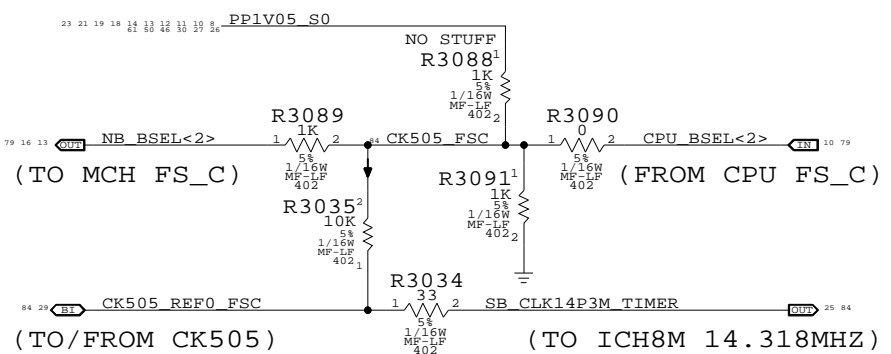
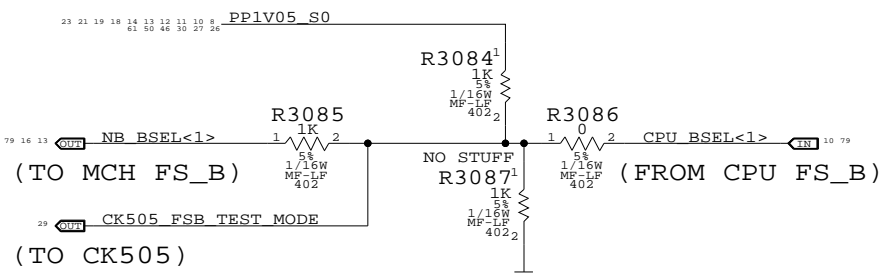
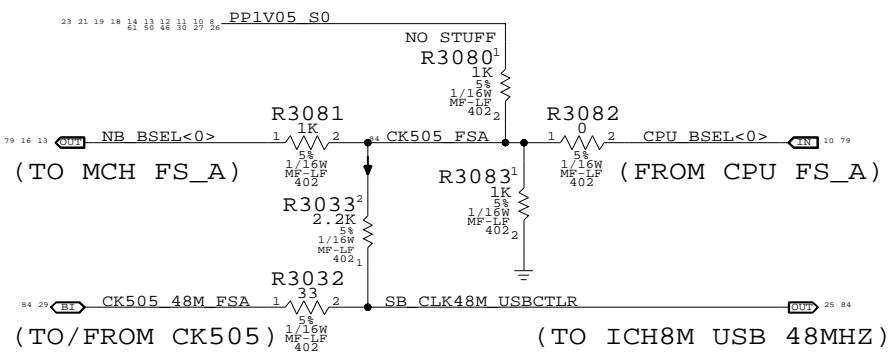
(Note: HOST/SRC/GFX clock termination removed. Silago SL8GLP536 or equiv. support only)

## CK505 Configuration Straps

FCT\_SEL (GFX clock select)



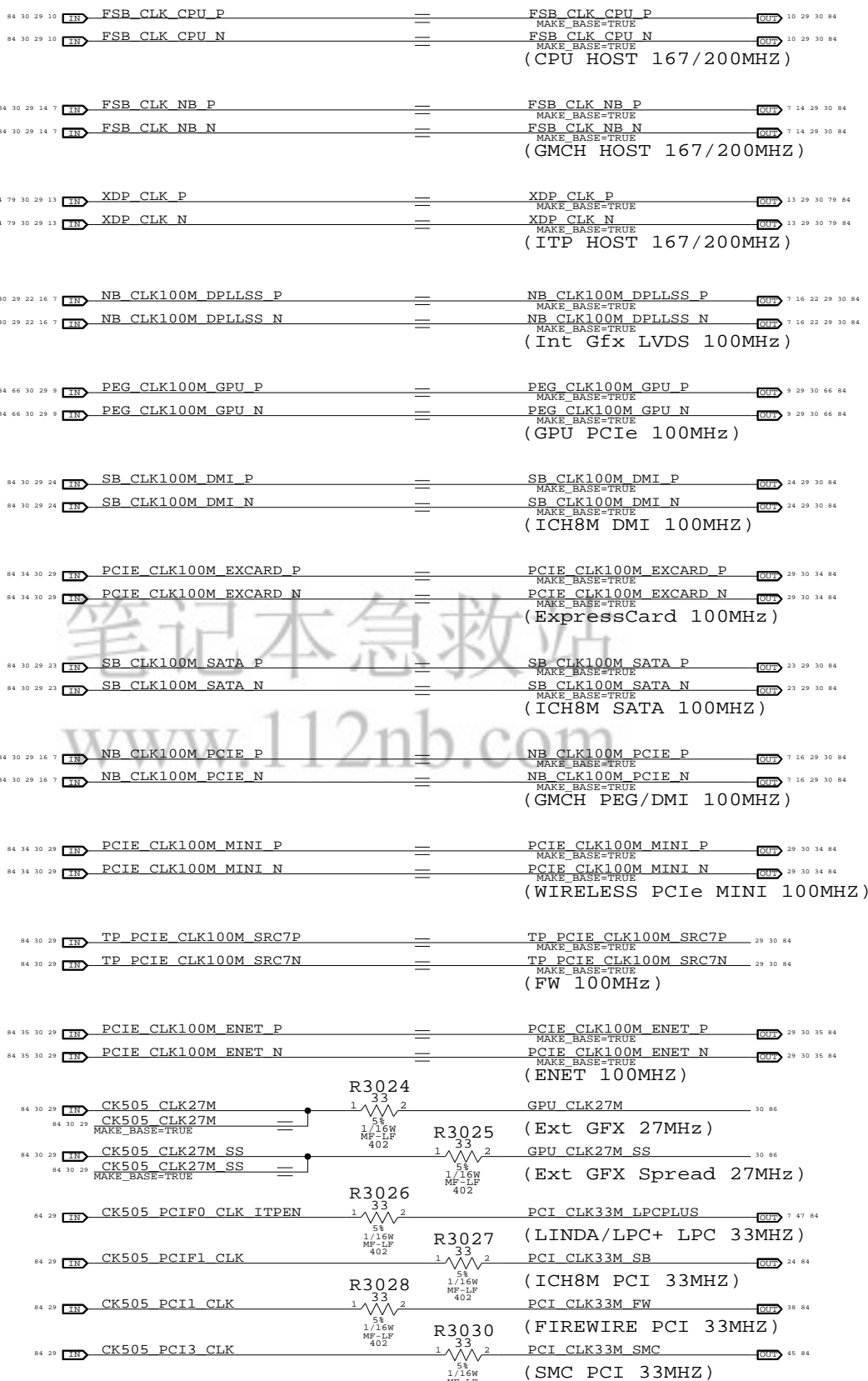
FS\_A, FS\_B, FS\_C (Host clock freq select)



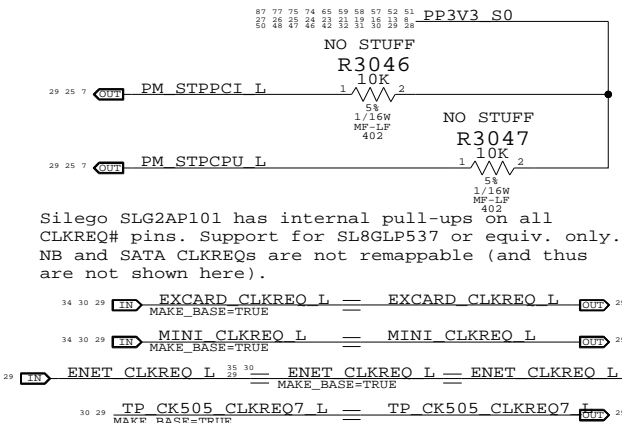
| FS_C | FS_B | FS_A | CPU MHz |
|------|------|------|---------|
| 0    | 0    | 0    | (266.6) |
| 0    | 0    | 1    | 133.3   |
| 0    | 1    | 0    | 200.0   |
| 0    | 1    | 1    | 166.6   |
| 1    | 0    | 0    | (333.3) |
| 1    | 0    | 1    | 100.0   |
| 1    | 1    | 0    | (400.0) |
| 1    | 1    | 1    | RSVD    |

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

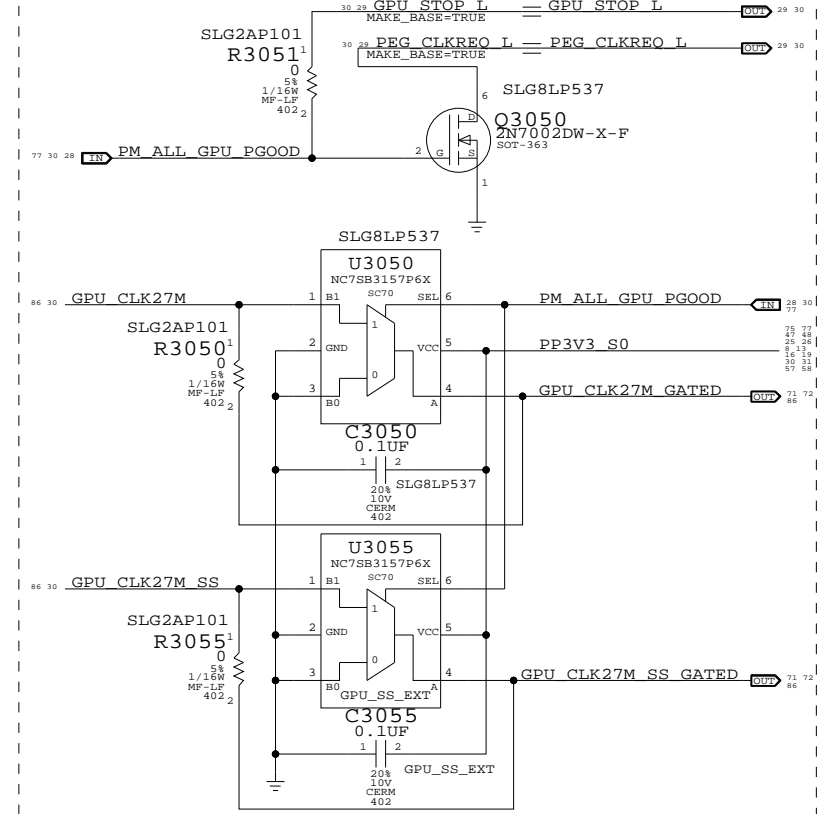
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)



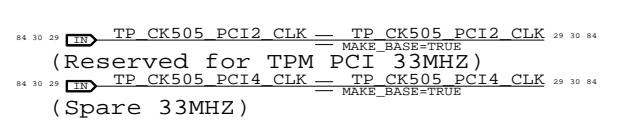
## CLKREQ Controls



## GPU Clock Gating



## Unused Clocks



### Clock Termination

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| SCALE | SHT            | OF     |
| NONE  | 30             | 88     |







8

7

6

5

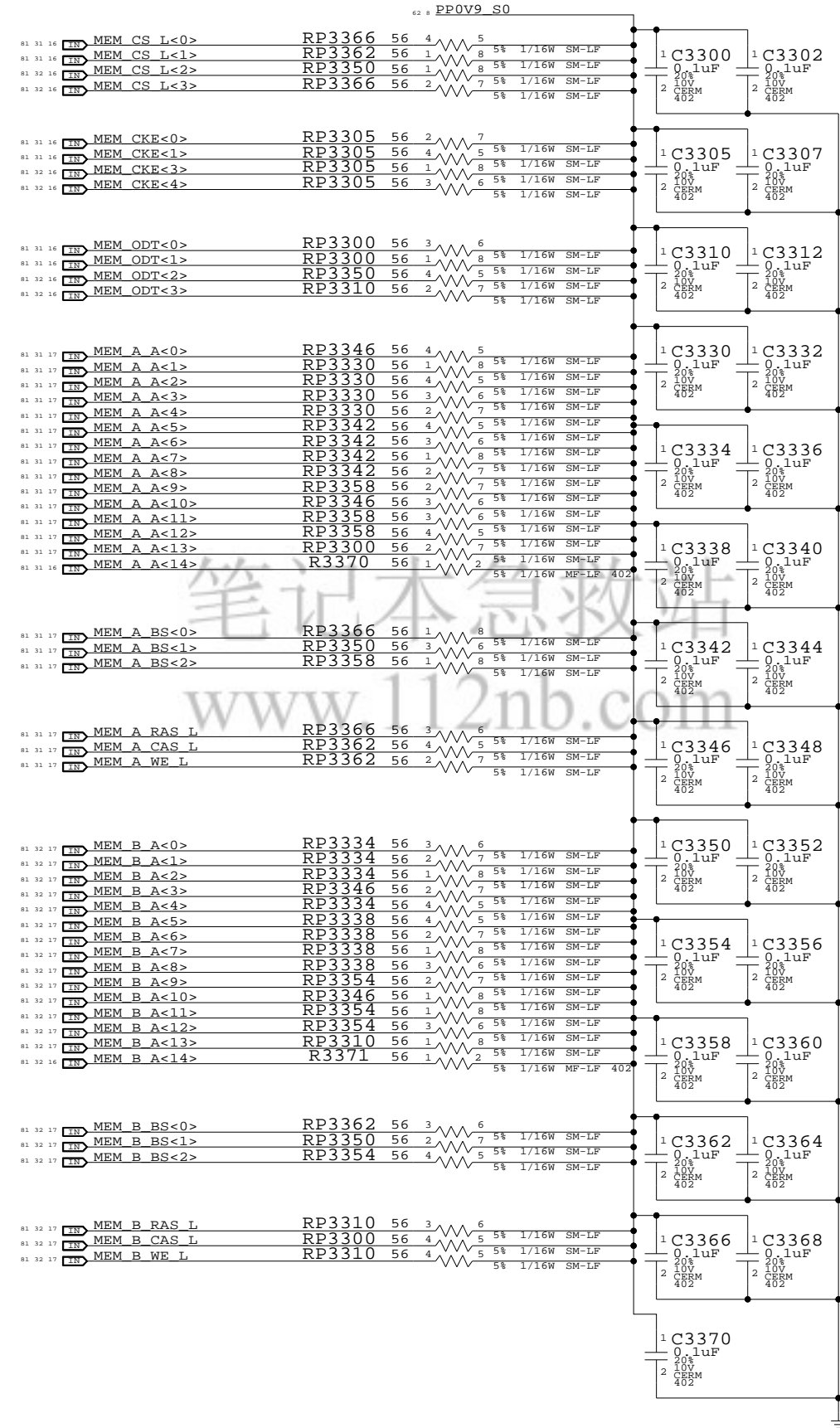
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors  
 Ensure CS\_L and ODT resistors are close to SO-DIMM connector



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Memory Active Termination  
 SYNC\_MASTER=(T9\_NOME) SYNC\_DATE=11/14/2006

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 33   | 88             |        |

8

7

6

5

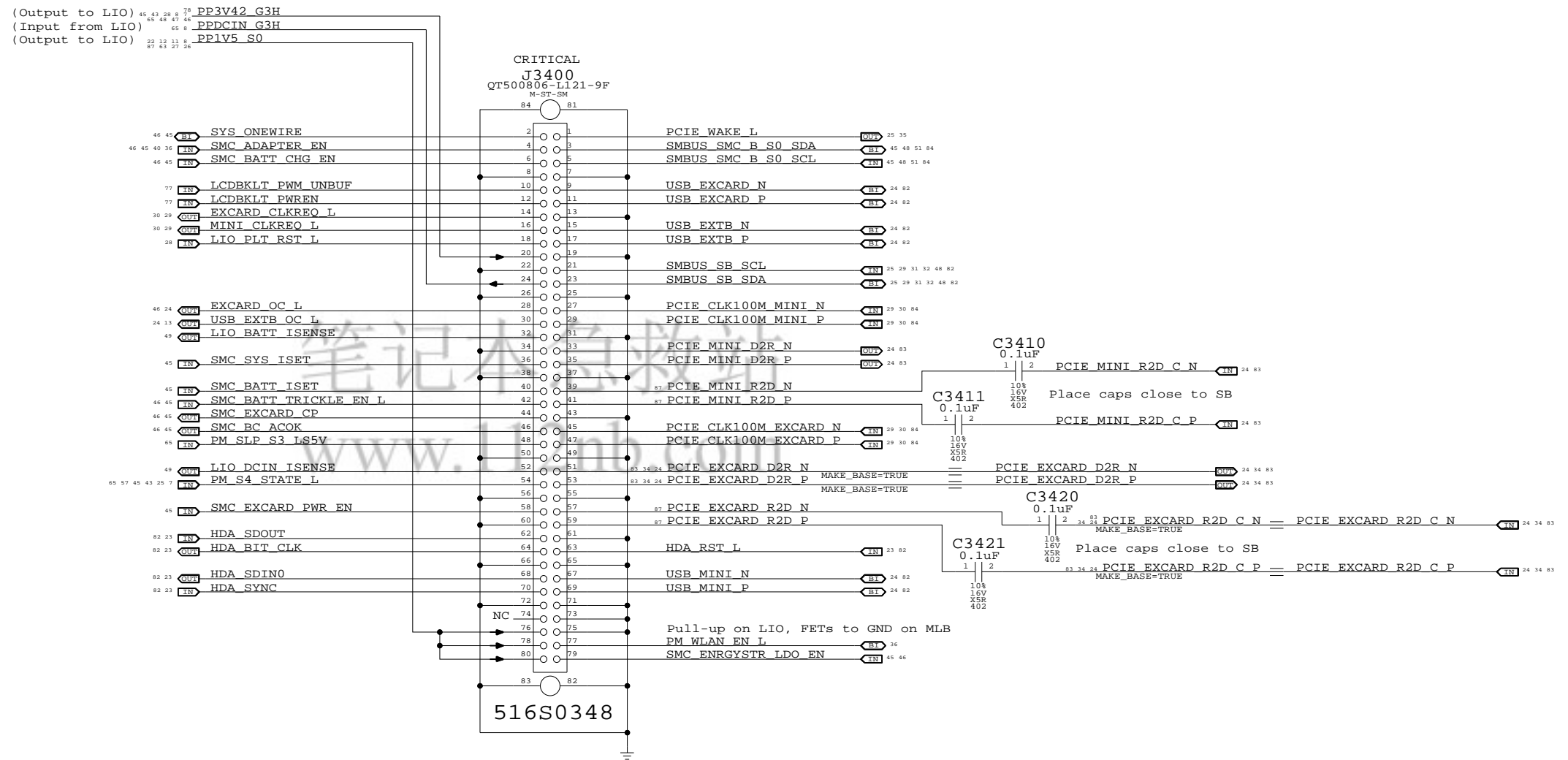
4

3

2

1

# Left I/O Board Connector



Left I/O Board Connector  
 SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=08/24/2006

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  |                | OF     |
| NONE                | 34   |                | 88     |

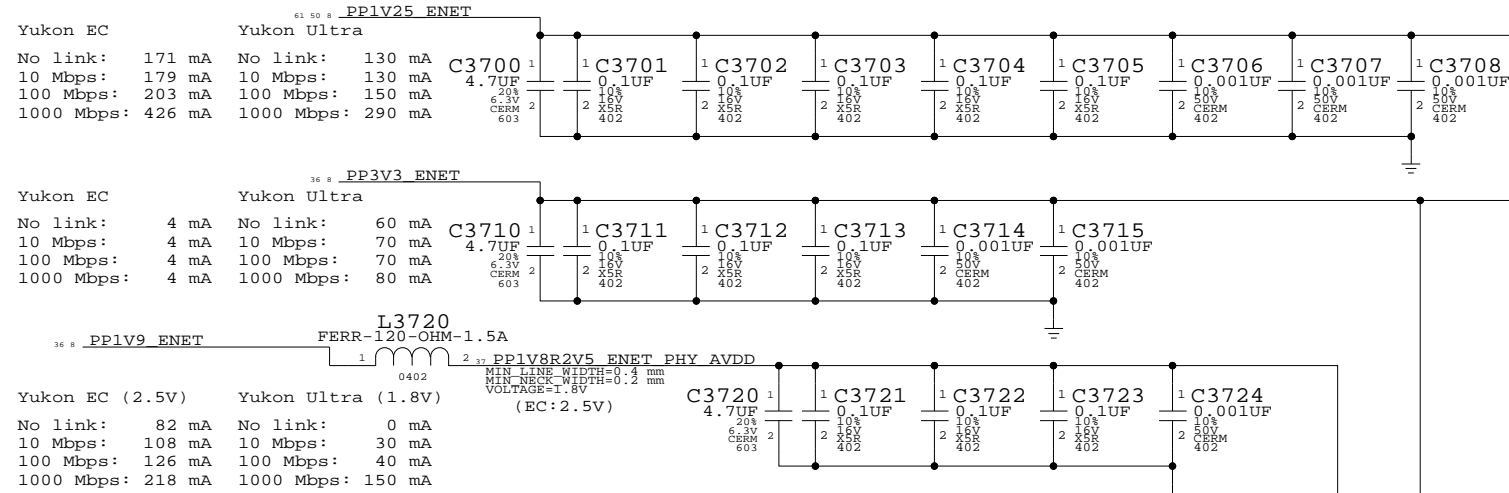
# Page Notes

Power aliases required by this page:  
 - =PP3V3\_ENET\_PHY (EC / Ultra)  
 - =PP1V8R2V5\_ENET\_PHY (2.5V / 1.8V)  
 - =YUKON\_EC\_PP2V5\_ENET (2.5V / GND)  
 - =PP1V2\_ENET\_PHY

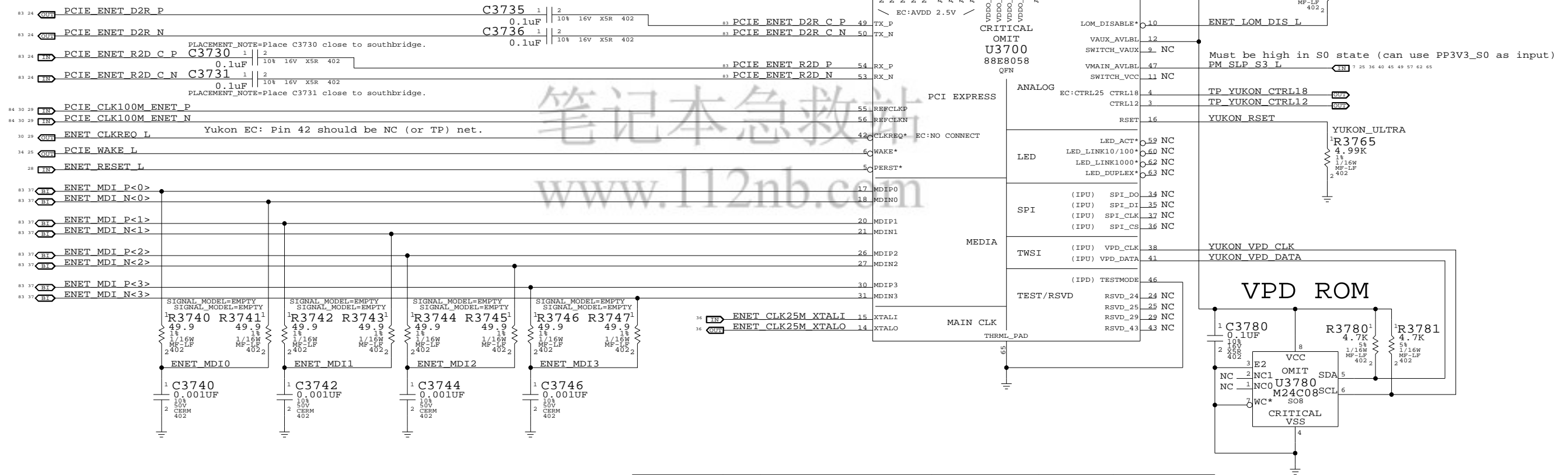
Signal aliases required by this page:  
 - =ENET\_CLKREQ\_L (NC/TP for Yukon EC)  
 - =ENET\_VMAIN\_AVLBLE (See note by pin)

BOM options provided by this page:  
 YUKON\_EC - Selects Yukon EC RSET value.  
 YUKON\_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



GND  
 Yukon EC: Alias to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF & 1x 0.001uF caps  
 Yukon Ultra: Alias to GND



| PART NUMBER | QTY | DESCRIPTION                               | REFERENCE DES | CRITICAL | BOM OPTION  |
|-------------|-----|---|---------------|----------|-------------|
| 338S0386    | 1   | IC, 88E8058, GIGABIT ENET XCVR, 64P QFN   | U3700         | CRITICAL | YUKON_ULTRA |
| 341S2060    | 1   | IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08 | U3780         | CRITICAL | YUKON_ULTRA |
| 338S0270    | 1   | IC, 88E8053, GIGABIT ENET XCVR, 64P QFN   | U3700         | CRITICAL | YUKON_EC    |
| 341S1797    | 1   | IC, EEPROM, SERIAL IIC, 8KBIT, S08        | U3780         | CRITICAL | YUKON_EC    |
| 114S0285    | 1   | RES, 4.87K, 1%, 1/16W, 0402, LF           | R3760         |          | YUKON_EC    |

To support Yukon EC and Ultra on the same board:

- Alias =YUKON\_EC\_PP2V5\_ENET to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5\_ENET\_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET\_CLKREQ\_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON\_ULTRA)
- Use YUKON\_EC and YUKON\_ULTRA BOMOPTIONS to select stuffed part

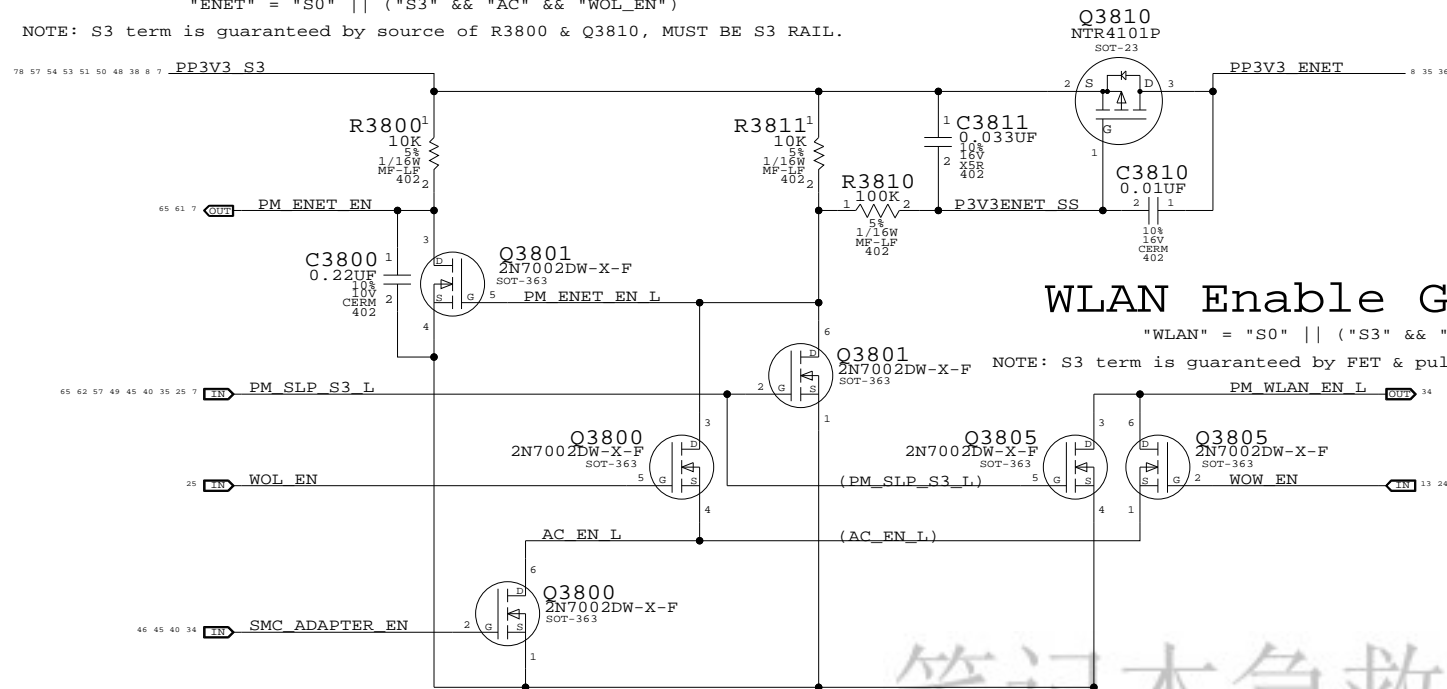
**Ethernet (Yukon)**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007  
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|-------|----------------|--------|
| SIZE  | DRAWING NUMBER | REV.   |
| D     | 051-7225       | 14.0.0 |
| SCALE | SHT            | OF     |
| NONE  | 35             | 88     |

## ENET Enable Generation

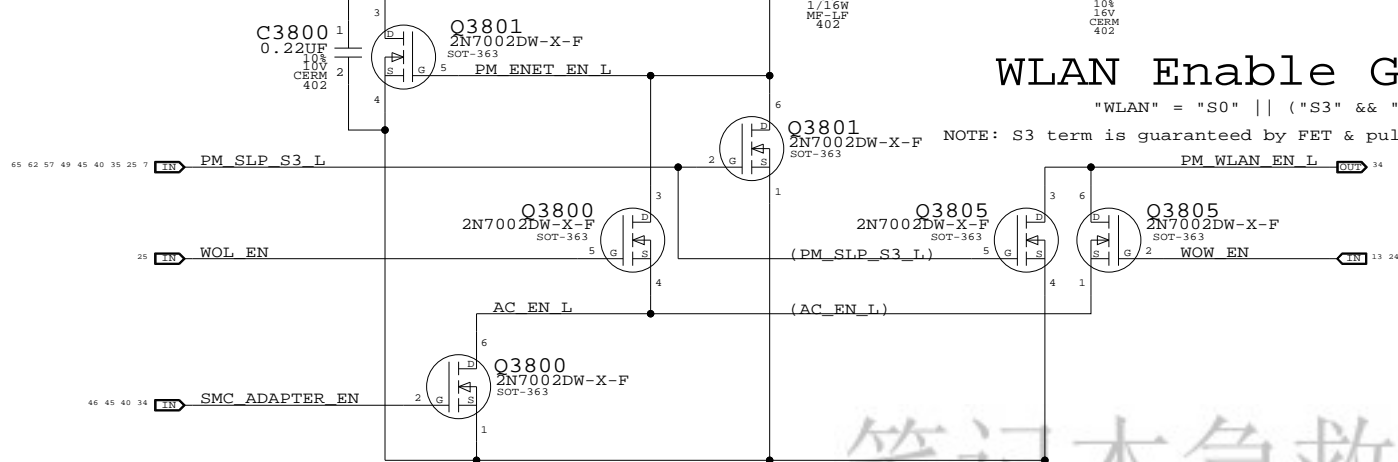
"ENET" = "S0" || ("S3" && "AC" && "WOL\_EN")  
 NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



## 3.3V ENET FET

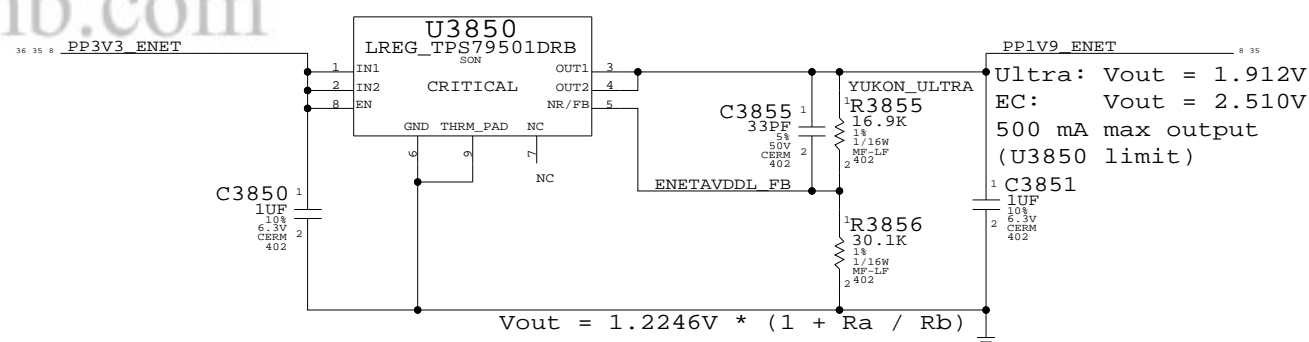
## WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOL\_EN")  
 NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



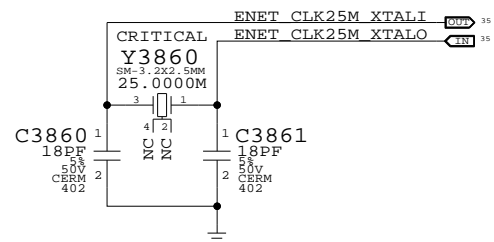
## Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC  
 Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



| PART NUMBER | QTY | DESCRIPTION               | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------------|---------------|----------|------------|
| 114S0363    | 1   | RES,31.6K,1%,1/16W,402,LF | R3855         |          | YUKON_EC   |

## Yukon Crystal



## Yukon Power Control

SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 36   | 88             |        |

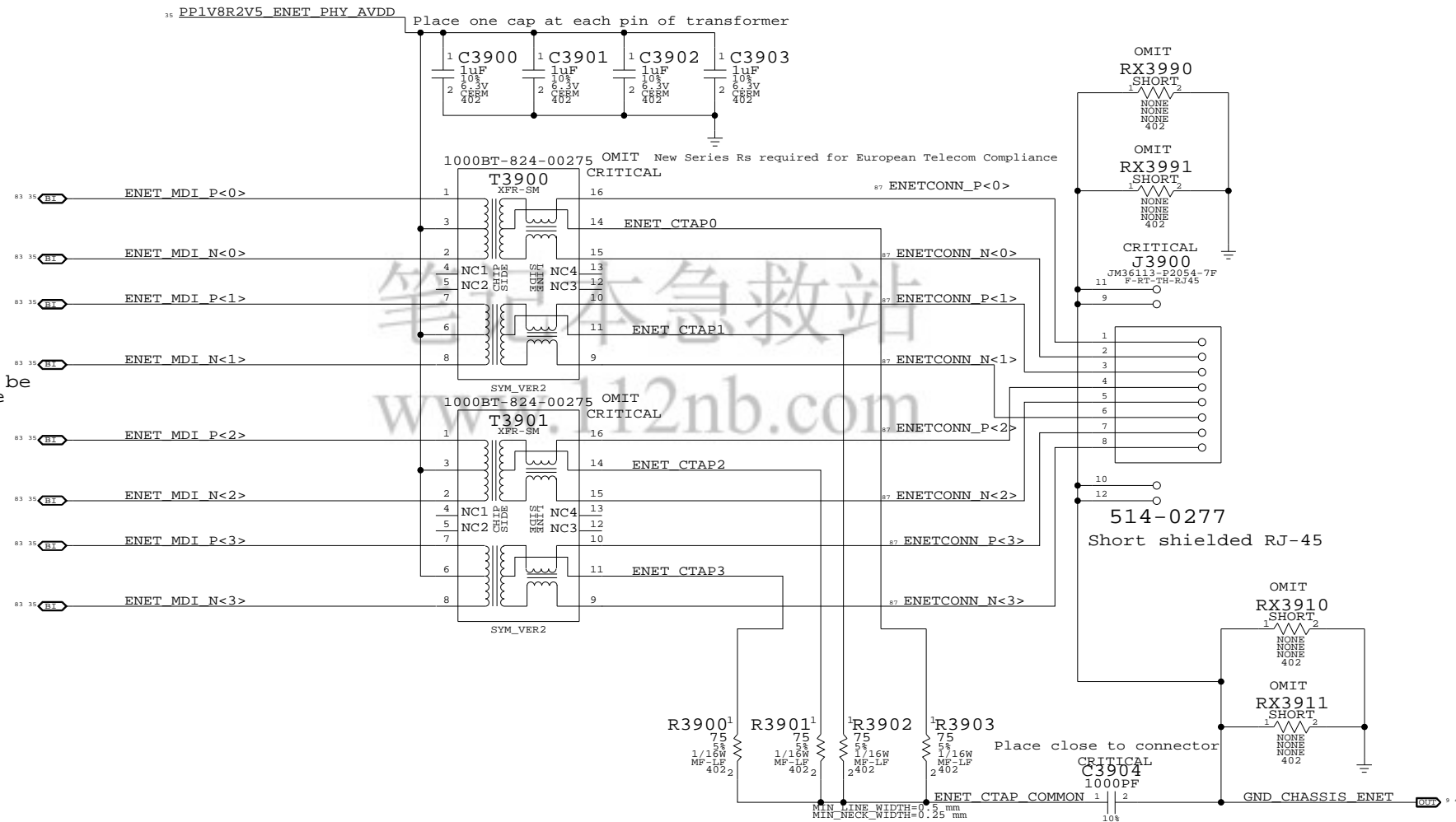
# Page Notes

Power aliases required by this page:  
 - =GND\_CHASSIS\_ENET

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

Transformers should be mirrored on opposite sides of the board



| PART#    | QTY | DESCRIPTION                               | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---|-------------------------|----------|------------|
| 15780030 | 2   | XPR, ISO, HALP-PORT, 1000T, 16P, SMD, 2MM | T3900, T3901            | CRITICAL |            |

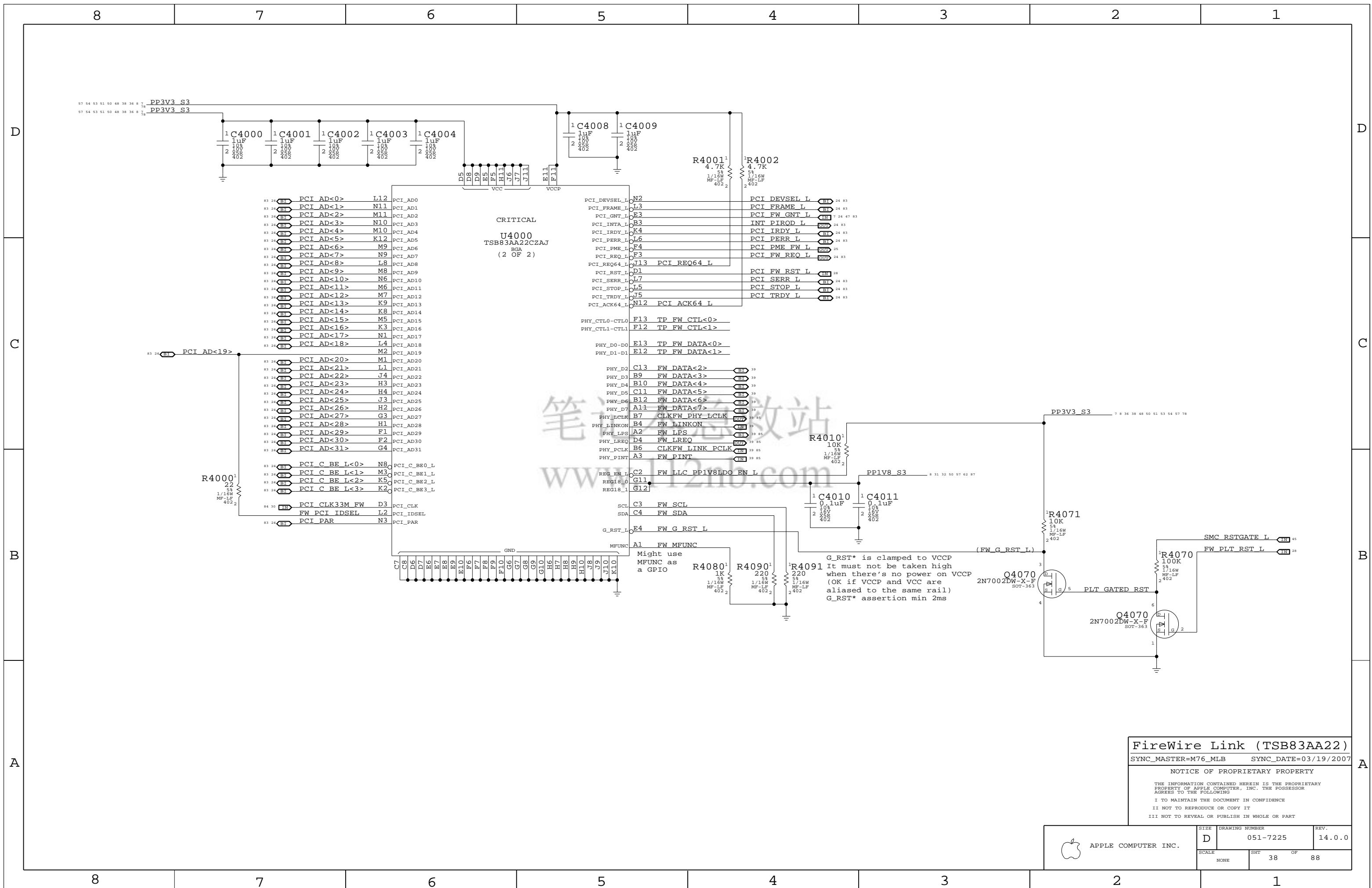
**Ethernet Connector**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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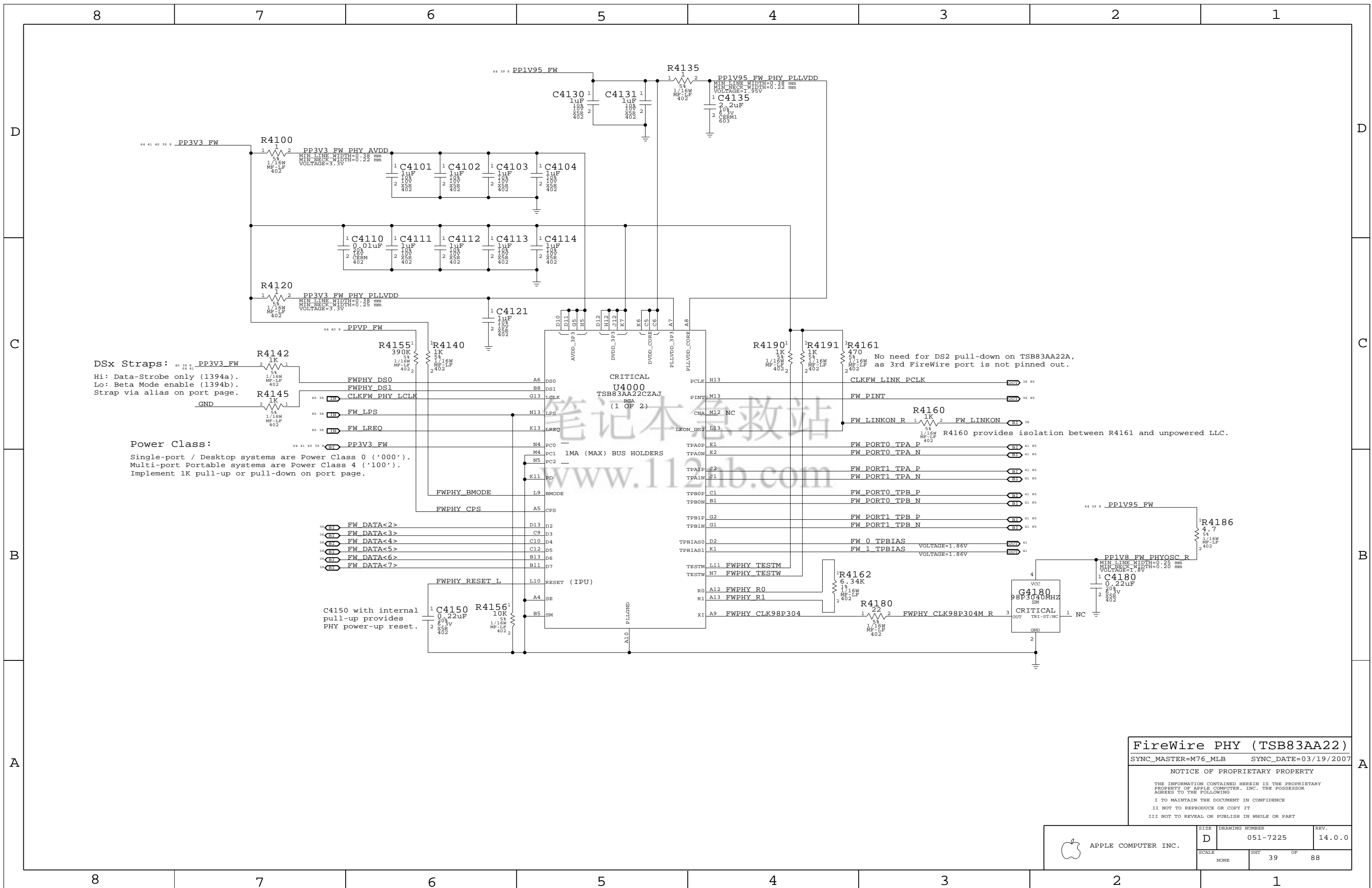
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|---------------------|------|----------------|--------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             | REV.   |
| NONE                | 37   | 88             |        |



**FireWire Link (TSB83AA22)**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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| SCALE               | SHT  | OF             |        |
| NONE                | 38   | 88             |        |



DSx Straps:

Hi: Data-Strobe only (1394a).  
Lo: Beta Mode enable (1394b).  
Strap via alias on port page.

**Power Class:**

Single-port / Desktop systems are Power Class 0 ('000').  
Multi-port Portable systems are Power Class 4 ('100').  
Implement 1K pull-up or pull-down on port page.

C4150 with internal pull-up provides PHY power-up reset.

No need for DS2 pull-down on TSB83AA22A, as 3rd FireWire port is not pinned out.

R4160 provides isolation between R4161 and unpowered LLC.

**FireWire PHY (TSB83AA22)**  
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 39   | 88             |        |

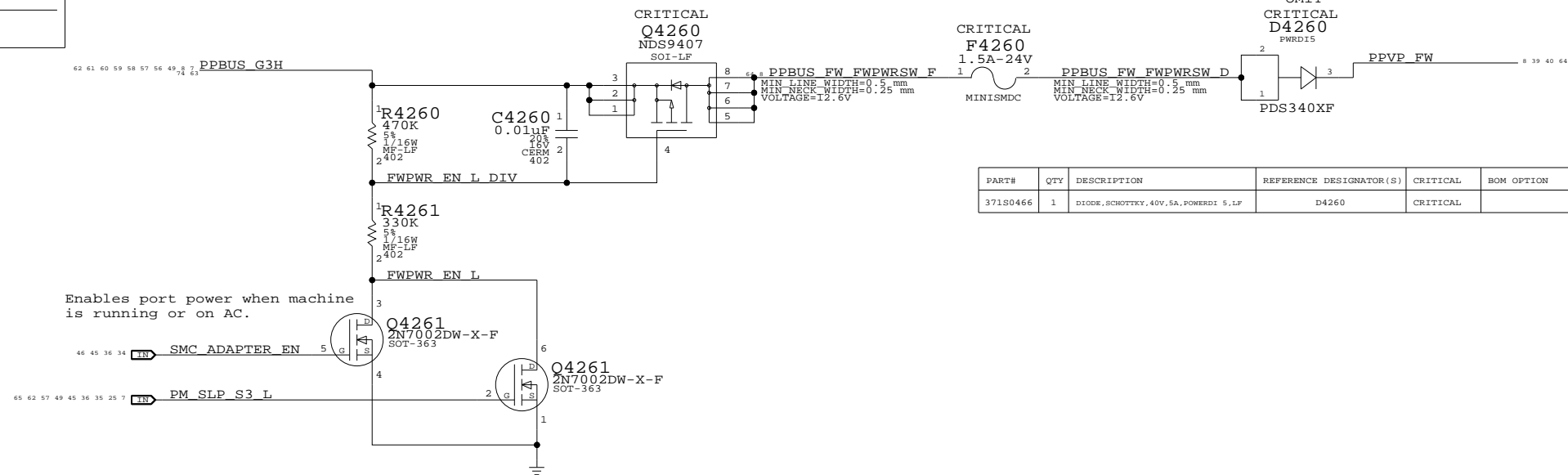
# Page Notes

Power aliases required by this page:  
 - =PPBUS\_S5\_FWPWSW (system supply for bus power)  
 - =PP3V3\_FW\_LATEVG\_ACTIVE  
 - =PPVP\_FW\_SUMNODE (power passthru summation node)

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - FW\_PORT\_FAULT\_PU

## FireWire Port Power Switch

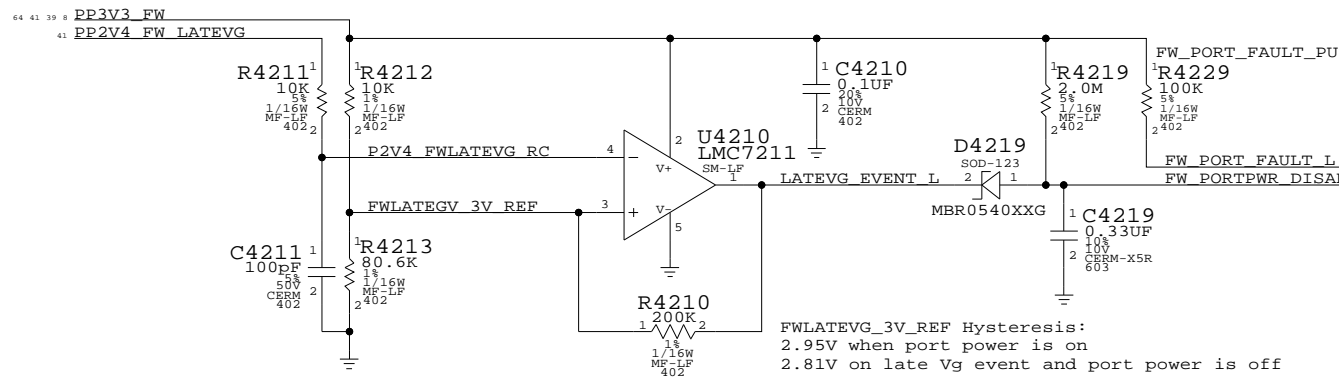


Enables port power when machine is running or on AC.

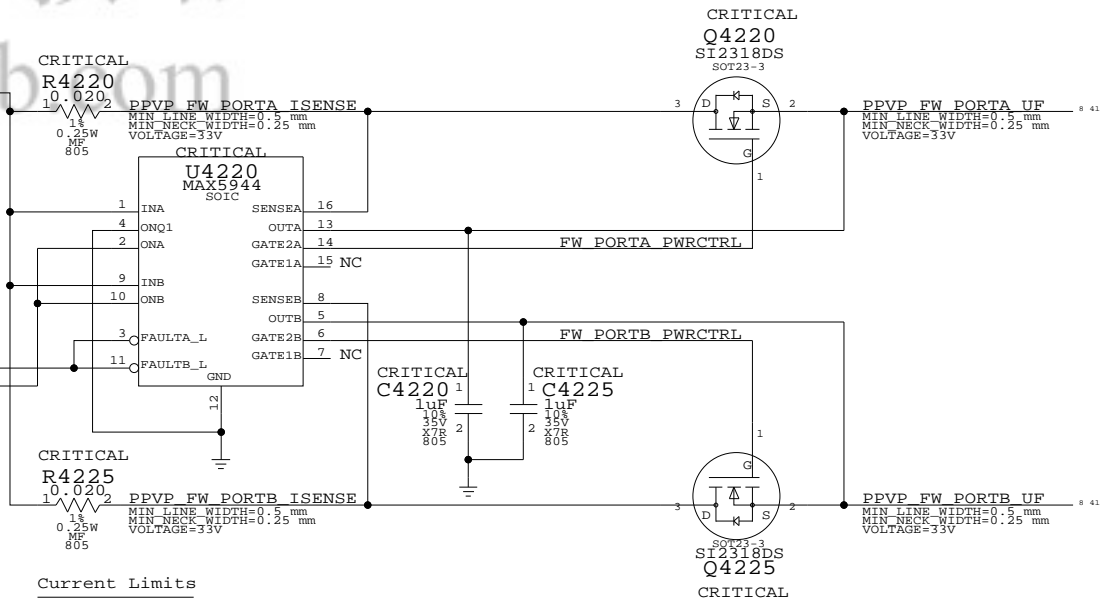
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## Current Limit/Active Late-VG Protection

## Late-VG Event Detection



FWLATEVG\_3V\_REF Hysteresis:  
 2.95V when port power is on  
 2.81V on late Vg event and port power is off



Current Limits  
 0.020 ohm => 2.4A  
 0.025 ohm => 2A  
 0.030 ohm => 1.66A (Ideal)  
 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

## FireWire Port Power

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 40   | 88             |        |



# Page Notes

Power aliases required by this page:  
 - =PPVP\_FW\_PORT0  
 - =PPVP\_FW\_PORT1  
 - =PP3V3\_FW\_LATEVG  
 - =GND\_CHASSIS\_FW\_PORT0L  
 - =GND\_CHASSIS\_FW\_PORT0U  
 - =GND\_CHASSIS\_FW\_PORT1  
 - =GND\_CHASSIS\_FW\_EMI\_R

Signal aliases required by this page:  
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:  
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

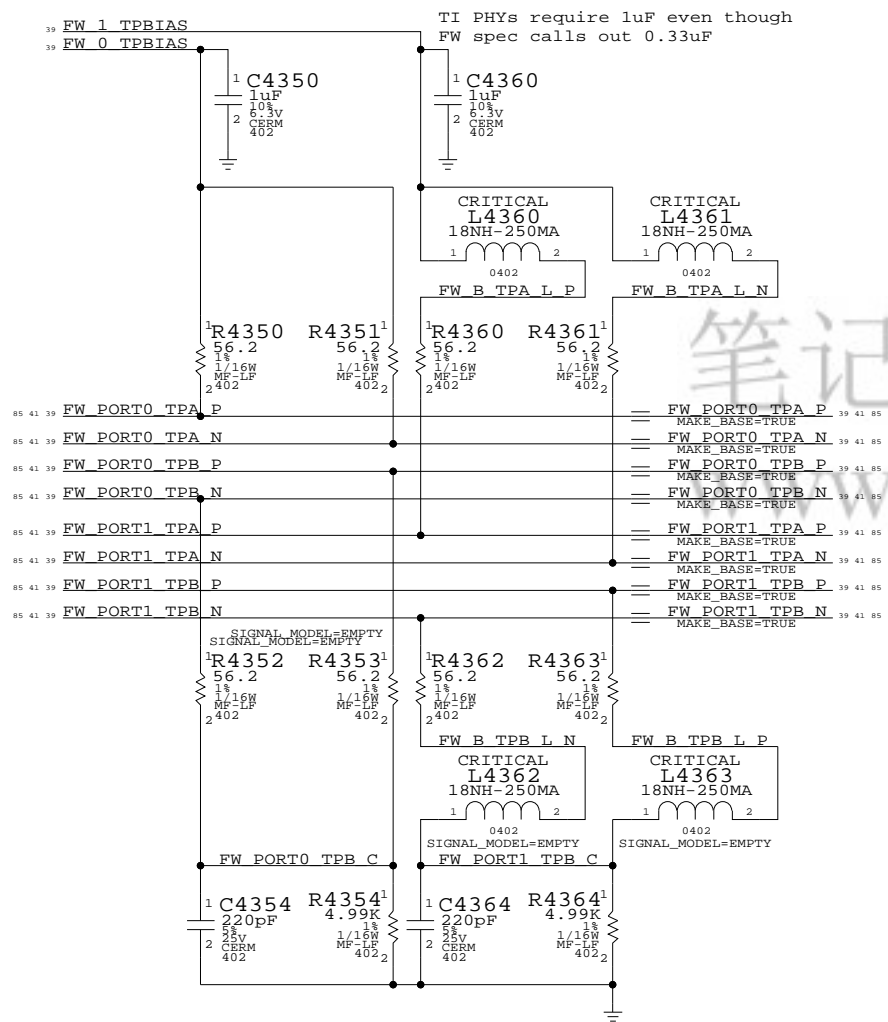
## FireWire PHY Config Straps

Configures PHY for:

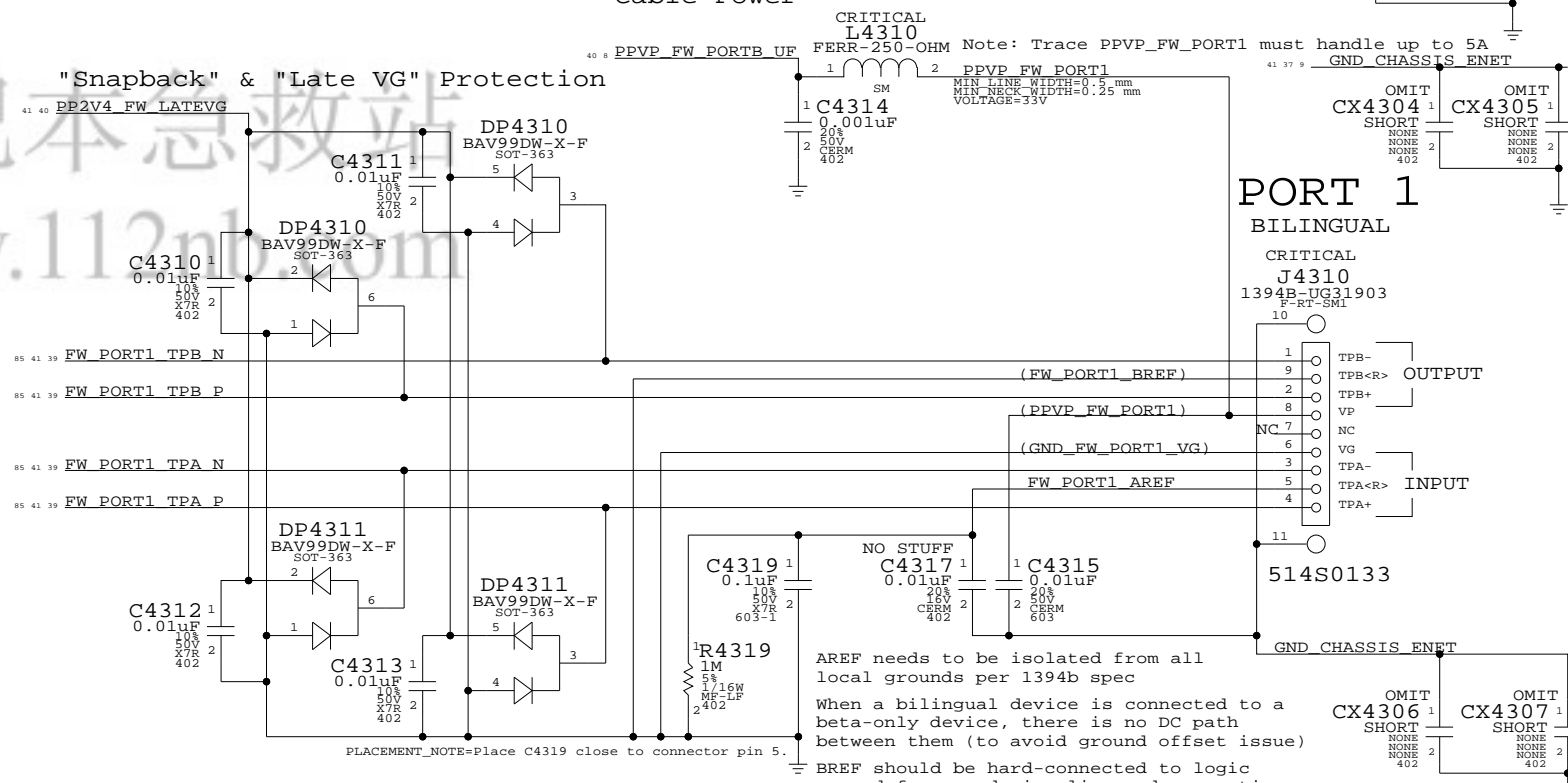
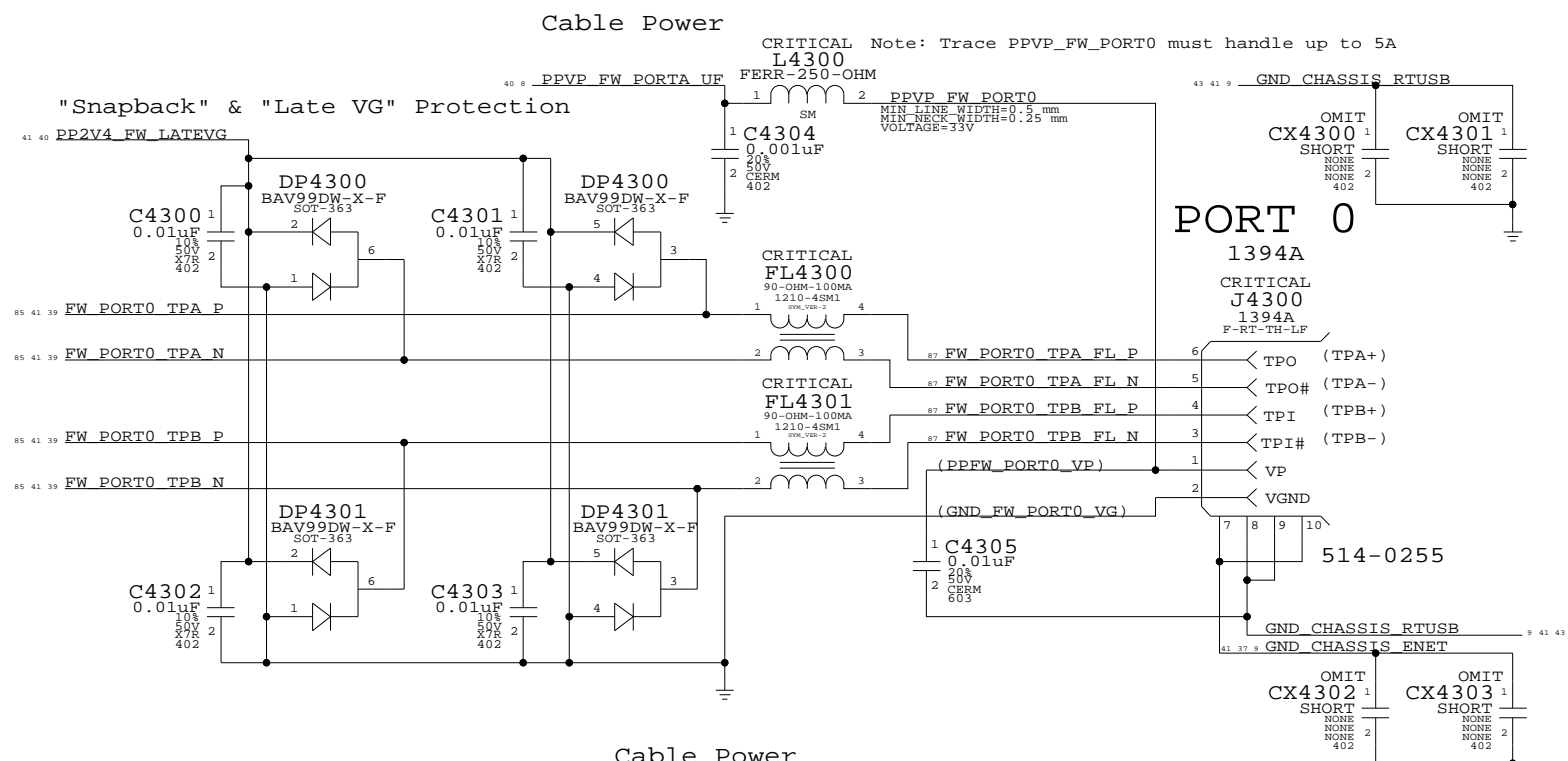
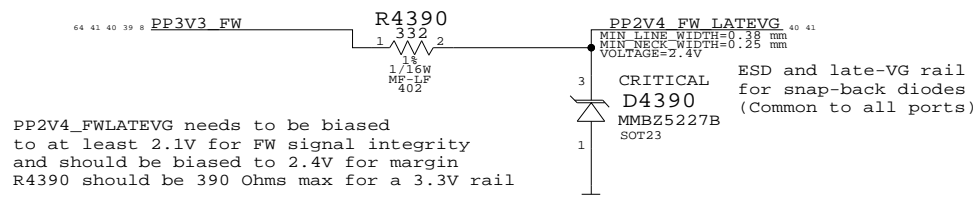
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

## Termination

Place close to FireWire PHY



## Late-VG Protection Power



**FireWire Ports**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

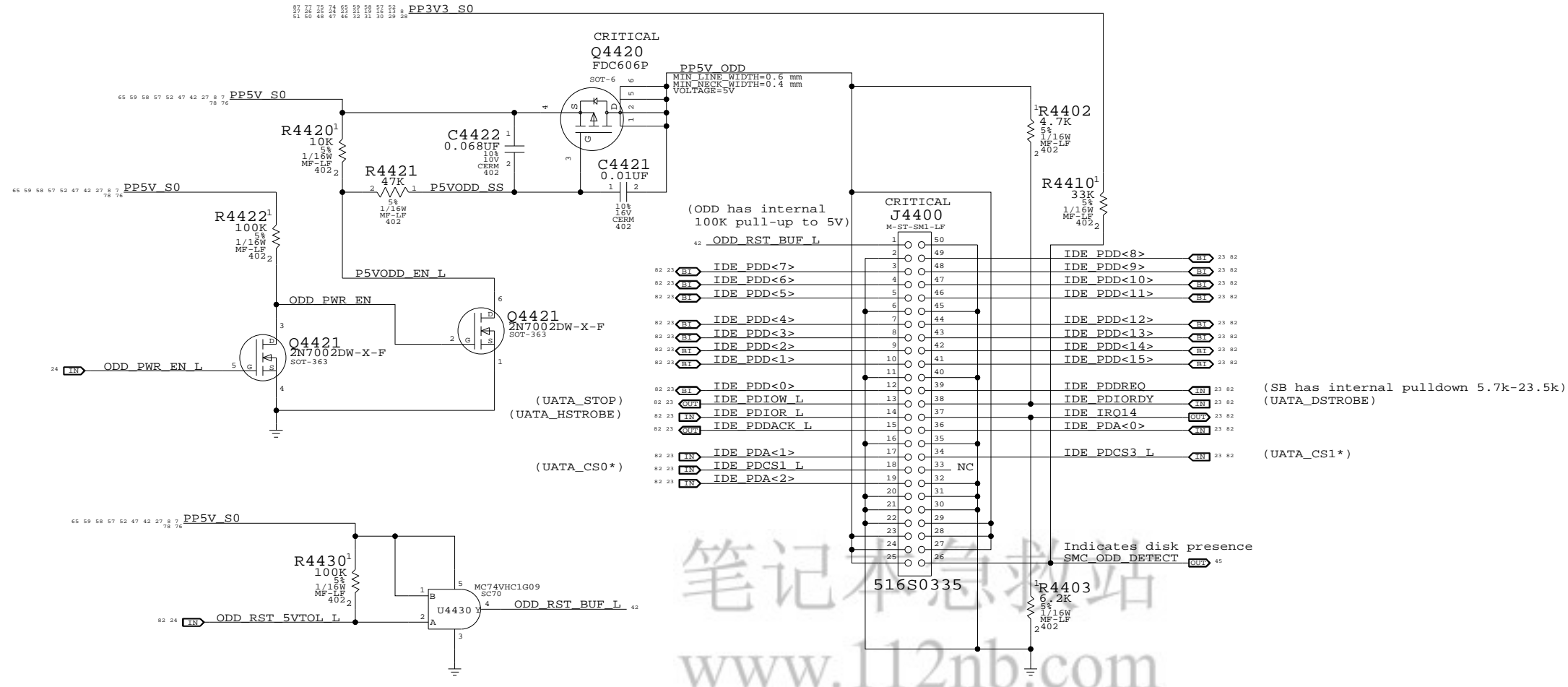
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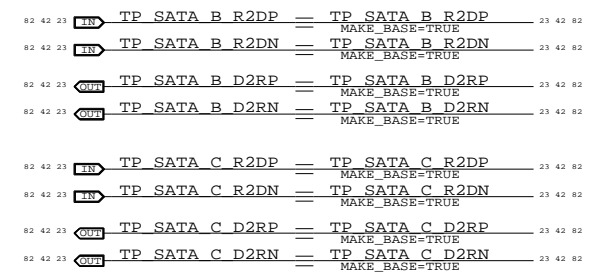
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| SCALE               | SHT  | OF             |        |
| NONE                | 41   | 88             |        |

# IDE (ODD) Connector



## Unused SATA Ports

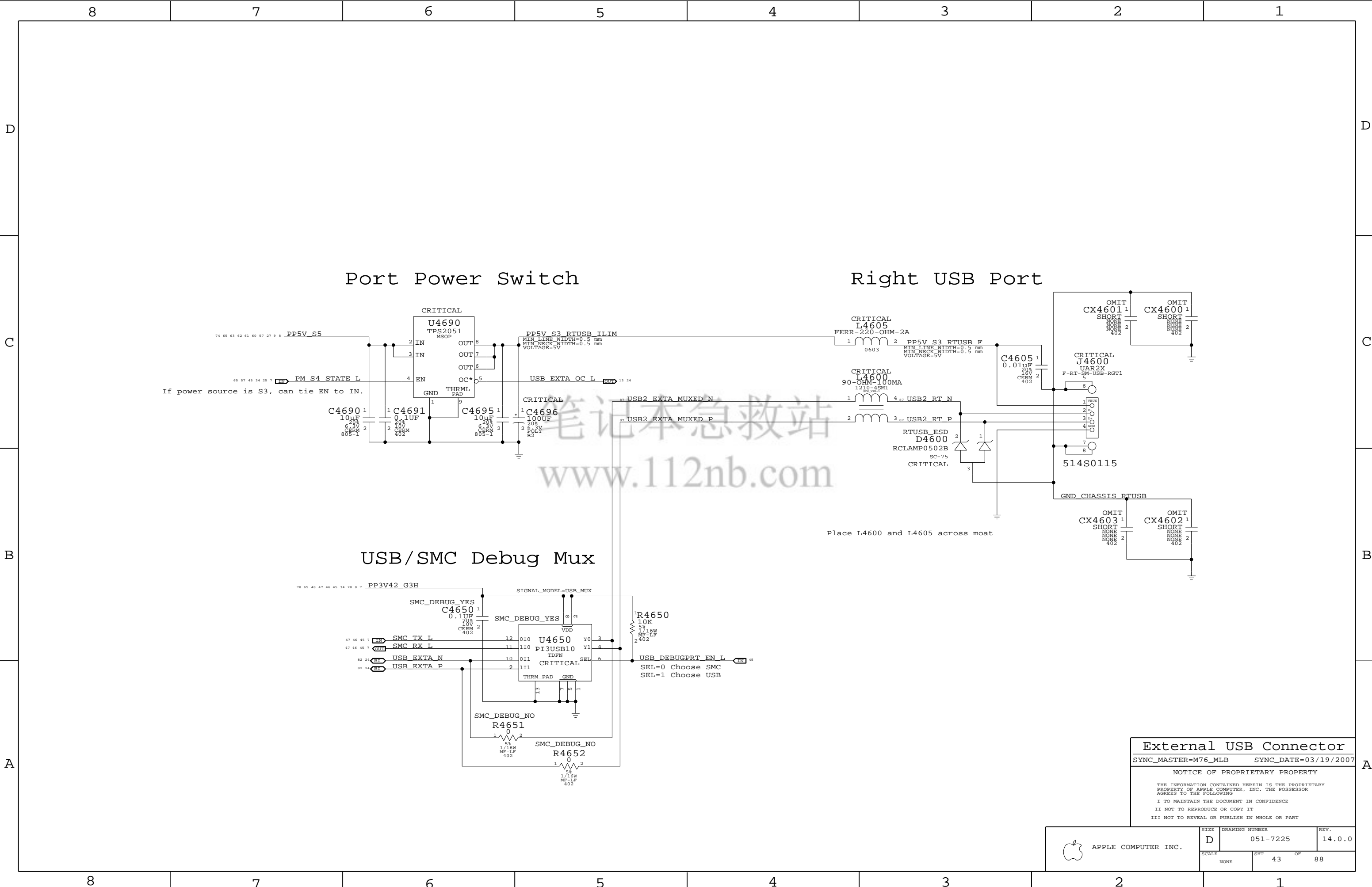


Placement note  
Place within 12.7mm  
from ball of SB

**PATA Connector**  
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| SCALE               | SHT  | OF             |        |
| NONE                | 42   | 88             |        |

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Place L4600 and L4605 across moat

**External USB Connector**

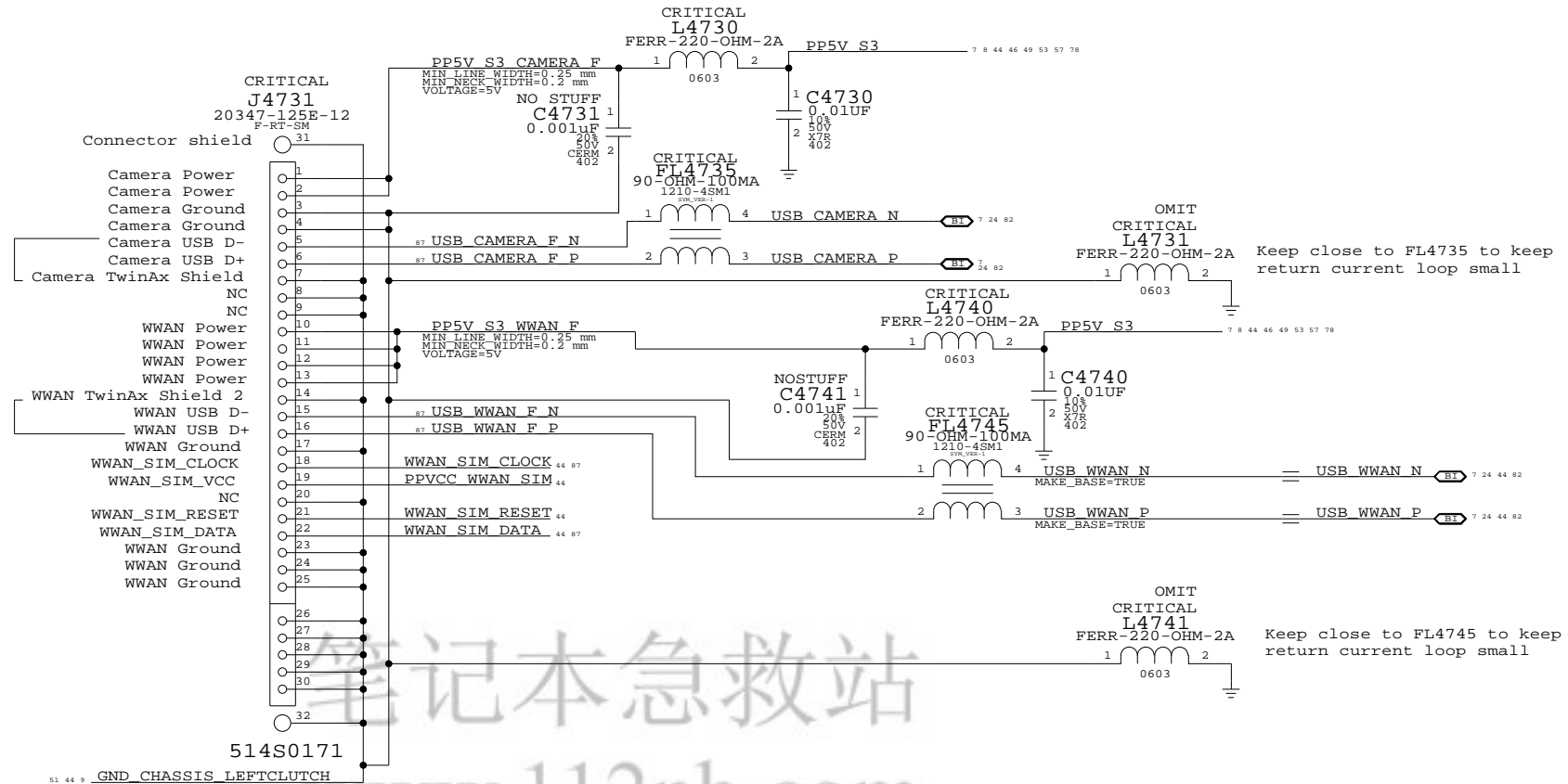
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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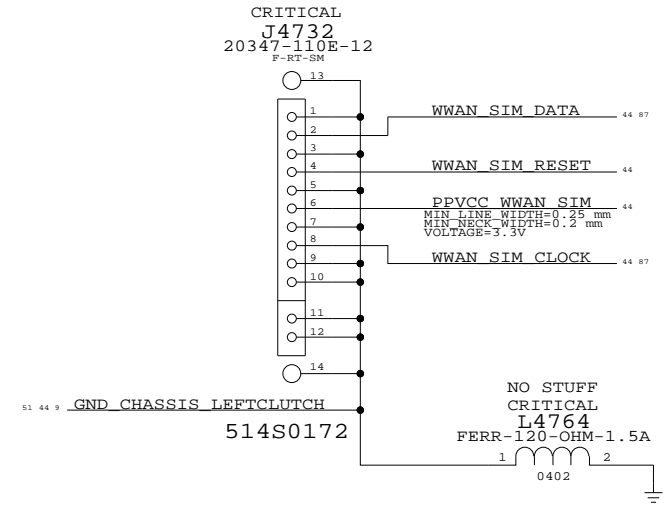
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|---------------------|------|----------------|--------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 43   | 88             |        |

# Left Clutch Barrel Interconnect



| PART#    | QTY | DESCRIPTION                    | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------------|-------------------------|----------|------------|
| 113S0022 | 2   | RES_MF,1/10W,00HM,5,0603,SM,LF | L4731,L4741             | CRITICAL |            |

# SIM Interconnect

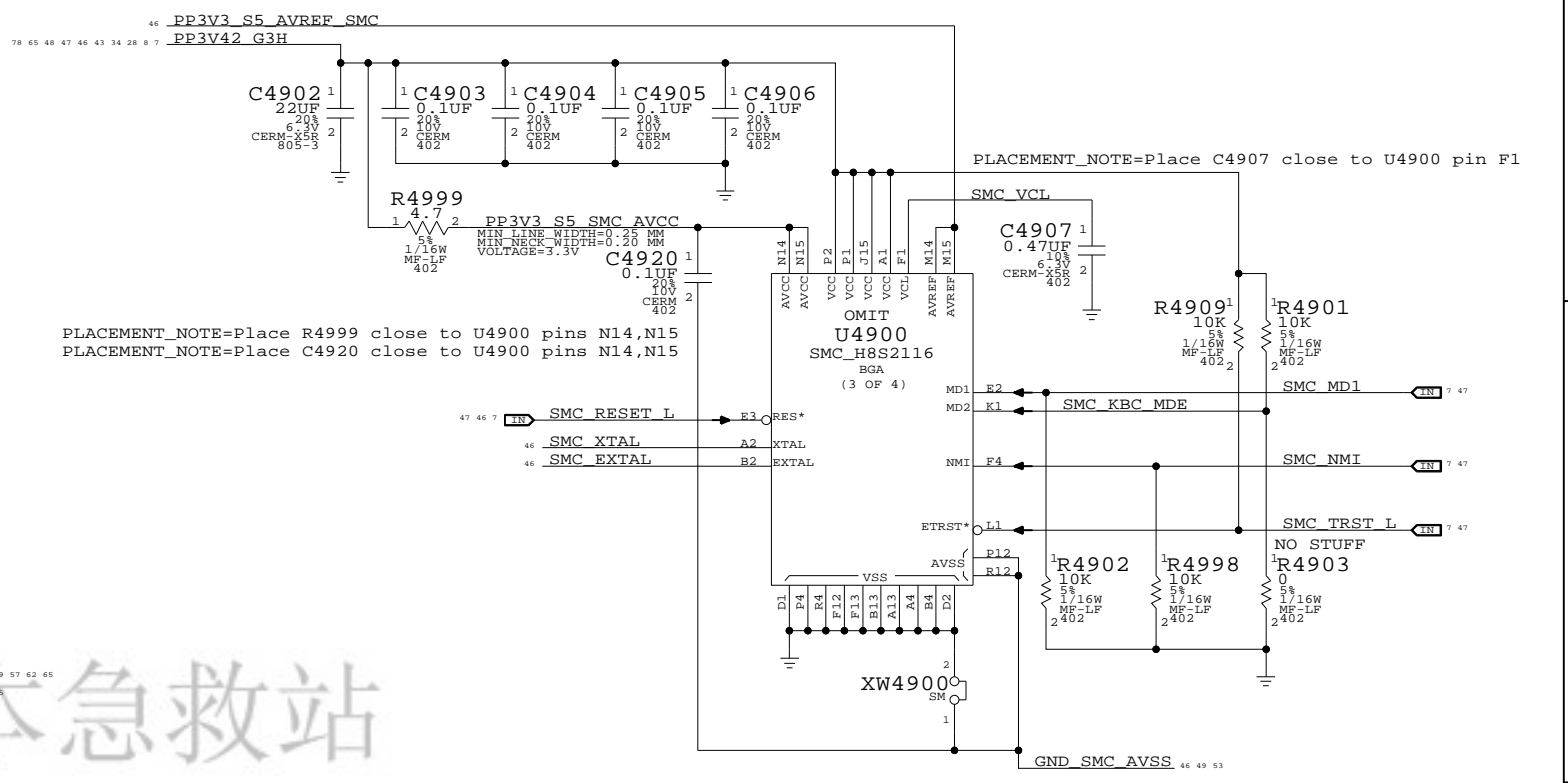
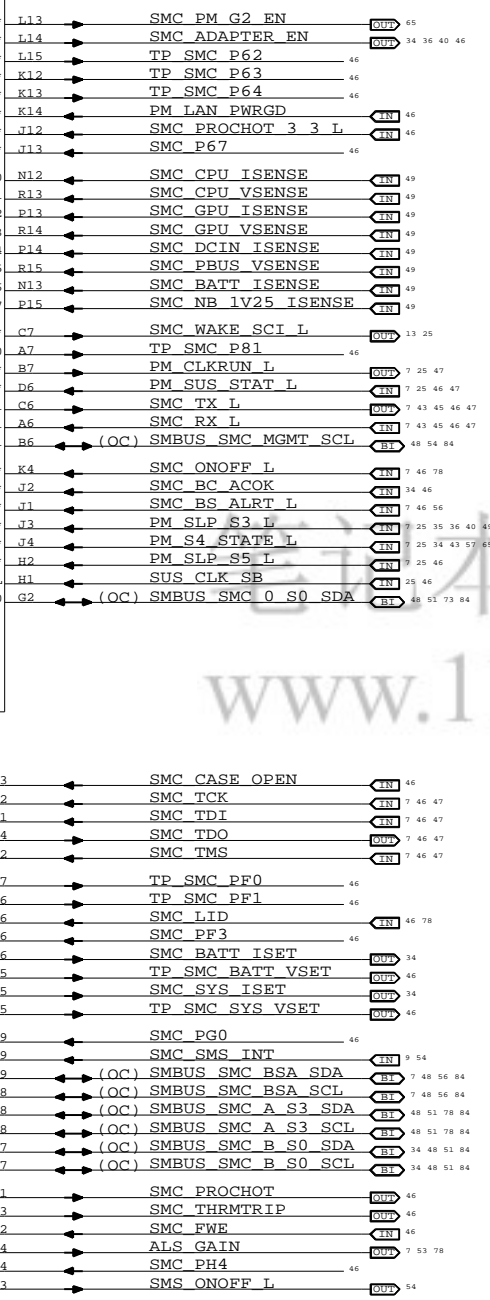
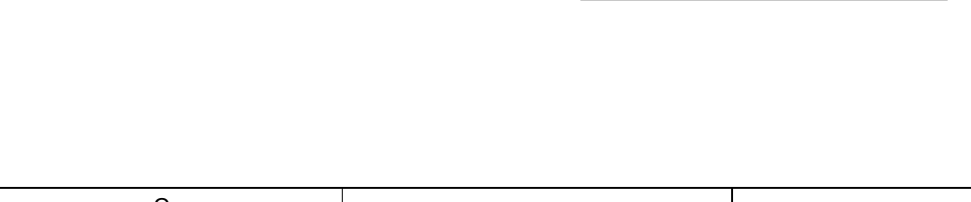
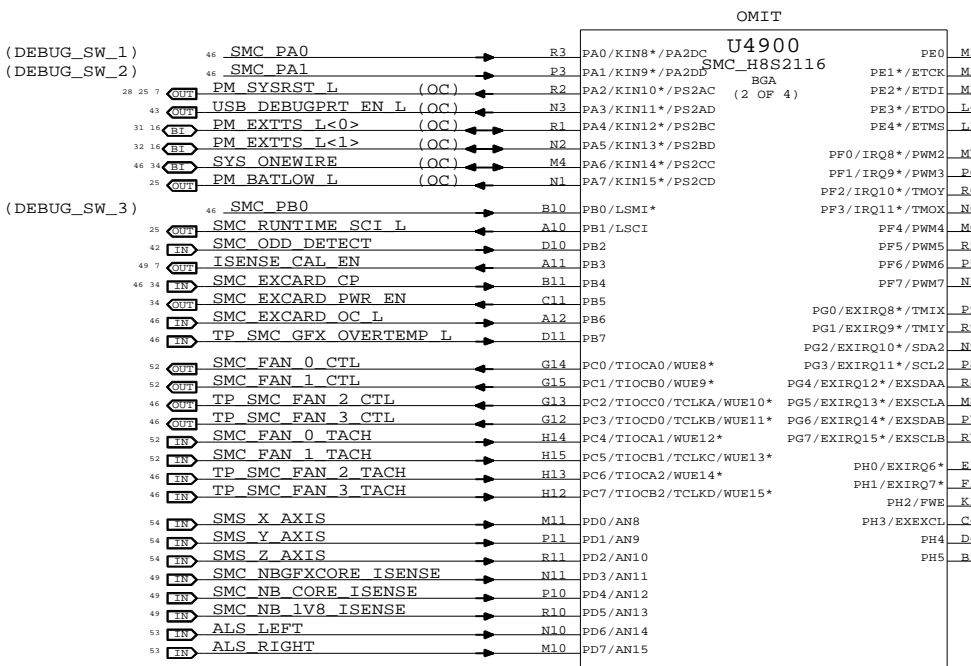
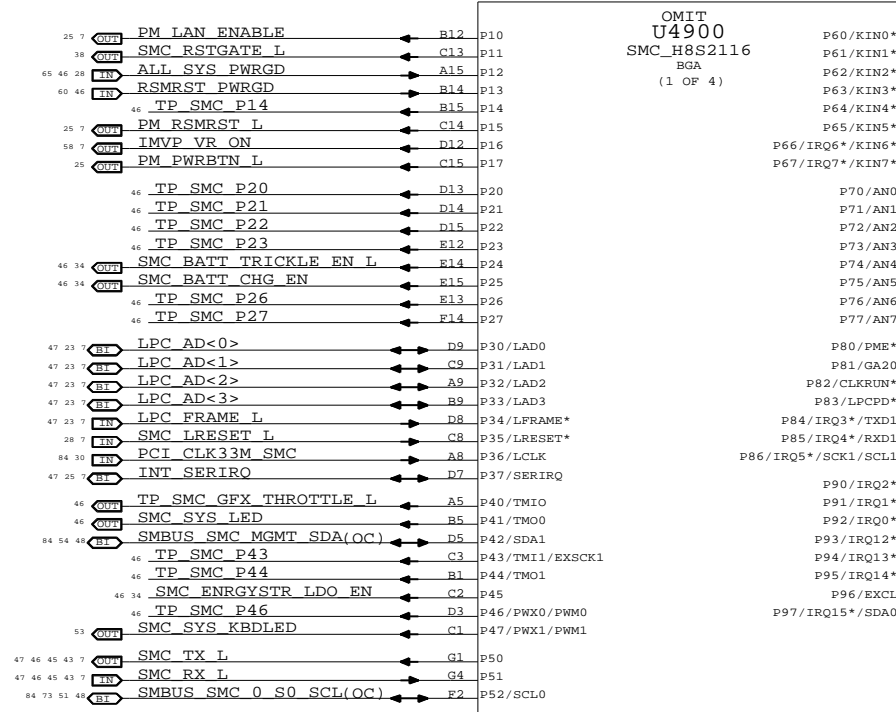


Left Clutch Barrel Interconnect  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

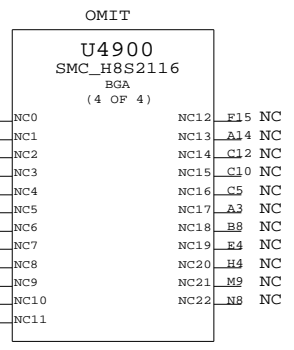
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| SCALE               | SHT  | OF             |        |
| NONE                | 44   | 88             |        |

NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

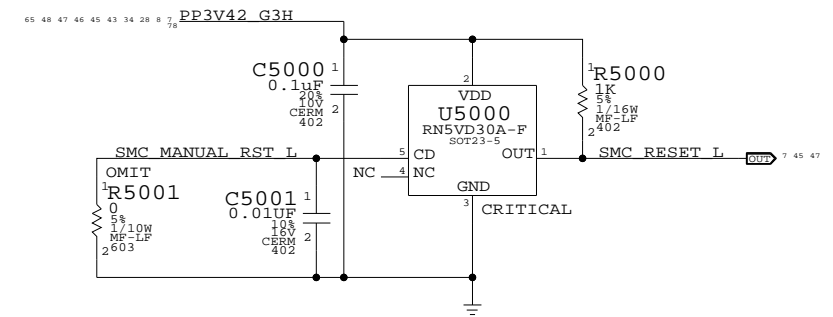


NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

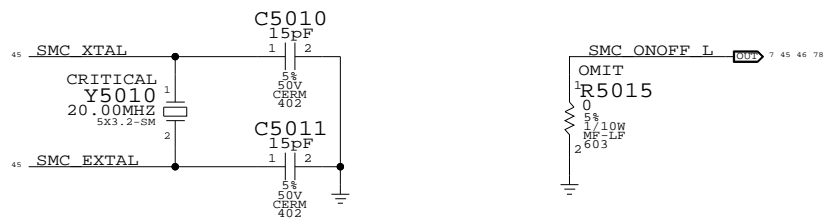


SMC  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007  
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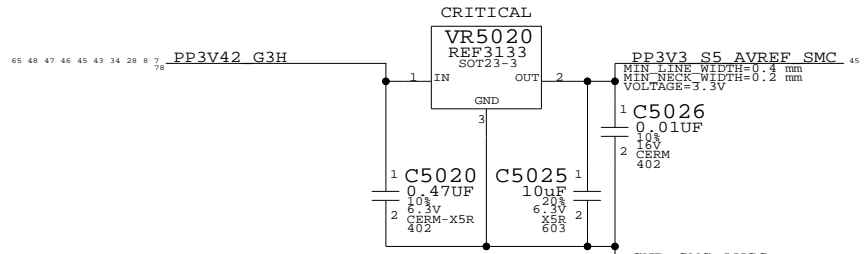
### SMC Reset "Button" / Brownout Detect



### SMC Crystal Circuit Debug Power "Button"

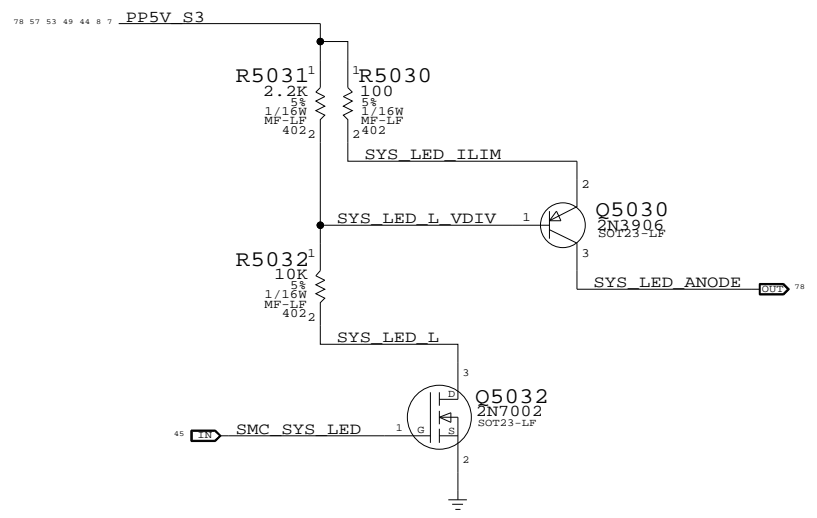


### SMC AVREF Supply



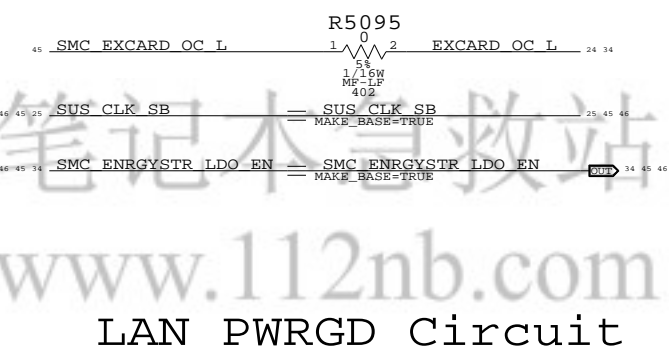
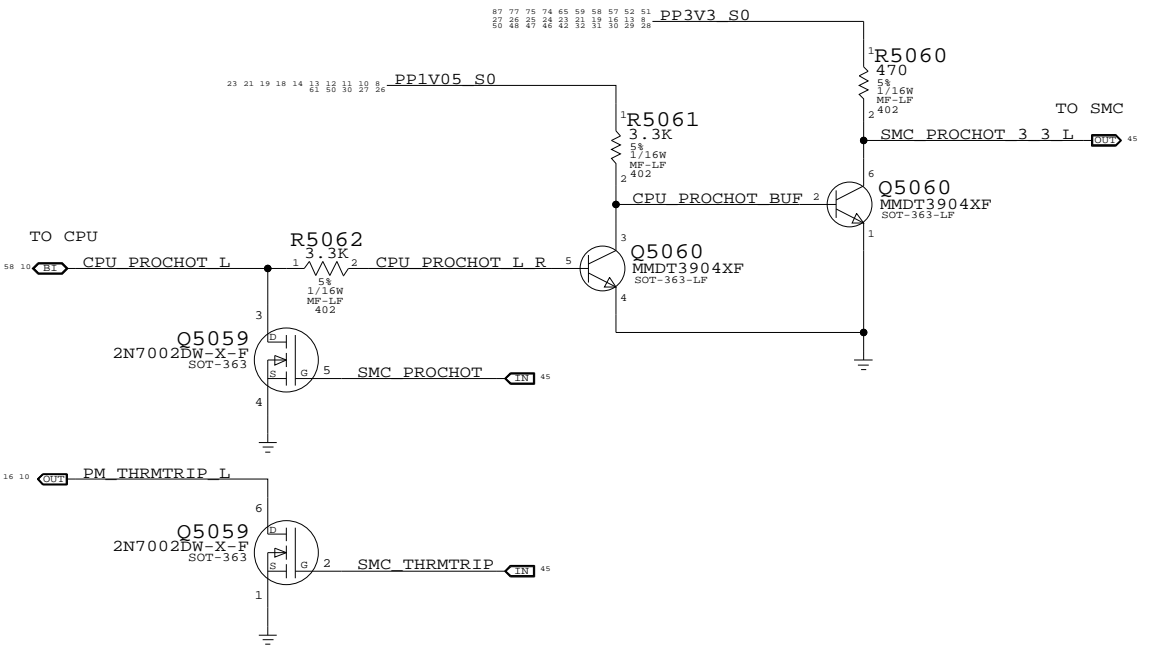
| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:            |
|-------------|---------------------------|------------|---------|----------------------|
| 35381381    | 35381278                  |            | ALL     | Interail ISL60002-33 |

### System (Sleep) LED Circuit



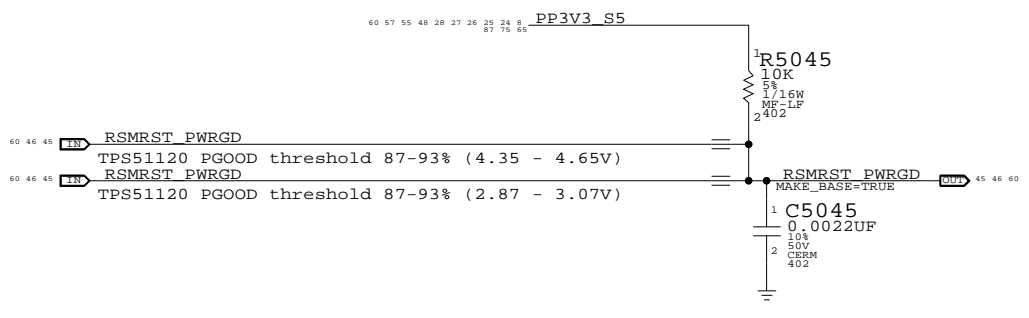
- TP\_SMC\_FAN\_2\_CTL == TP\_SMC\_FAN\_2\_CTL
- TP\_SMC\_FAN\_2\_TACH == TP\_SMC\_FAN\_2\_TACH
- TP\_SMC\_FAN\_3\_CTL == TP\_SMC\_FAN\_3\_CTL
- TP\_SMC\_FAN\_3\_TACH == TP\_SMC\_FAN\_3\_TACH
- TP\_SMC\_GFX\_OVERTEMP\_L == TP\_SMC\_GFX\_OVERTEMP\_L
- TP\_SMC\_GFX\_THROTTLE\_L == TP\_SMC\_GFX\_THROTTLE\_L
- TP\_SMC\_BATT\_VSET == TP\_SMC\_BATT\_VSET
- TP\_SMC\_SYS\_VSET == TP\_SMC\_SYS\_VSET
- TP\_SMC\_P14 == TP\_SMC\_P14
- TP\_SMC\_P20 == TP\_SMC\_P20
- TP\_SMC\_P21 == TP\_SMC\_P21
- TP\_SMC\_P22 == TP\_SMC\_P22
- TP\_SMC\_P23 == TP\_SMC\_P23
- TP\_SMC\_P26 == TP\_SMC\_P26
- TP\_SMC\_P27 == TP\_SMC\_P27
- TP\_SMC\_P43 == TP\_SMC\_P43
- TP\_SMC\_P44 == TP\_SMC\_P44
- TP\_SMC\_P46 == TP\_SMC\_P46
- TP\_SMC\_P62 == TP\_SMC\_P62
- TP\_SMC\_P63 == TP\_SMC\_P63
- TP\_SMC\_P64 == TP\_SMC\_P64
- TP\_SMC\_P81 == TP\_SMC\_P81
- TP\_SMC\_PF0 == TP\_SMC\_PF0
- TP\_SMC\_PF1 == TP\_SMC\_PF1

### SMC FSB to 3.3V Level Shifting



### S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation

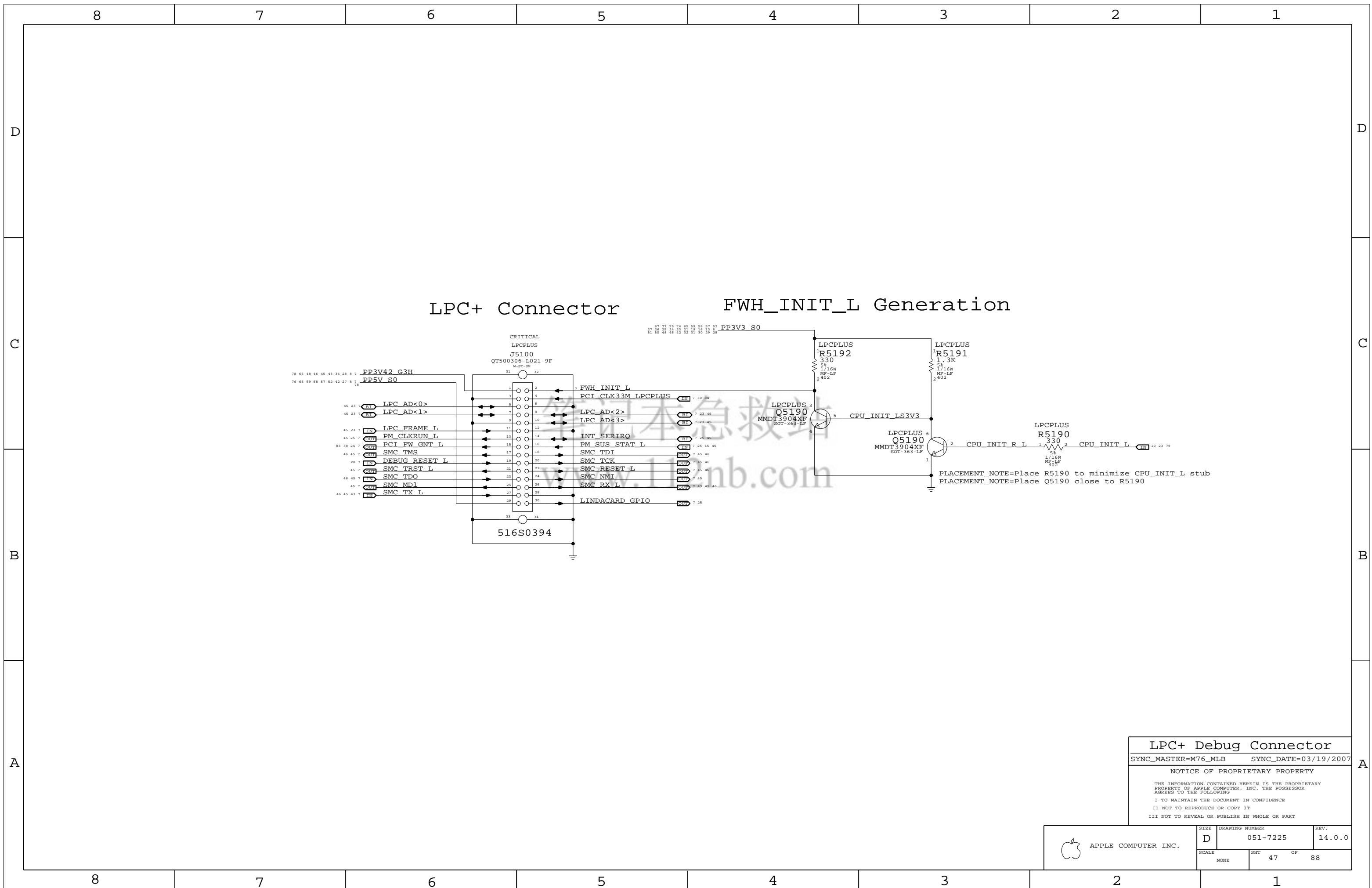


- SMC\_PA0 R5091 100K
- SMC\_PA1 R5092 100K
- SMC\_PB0 R5093 100K
- SMC\_ONOFF\_L R5070 10K
- SMC\_LID R5071 100K
- SMC\_FWE R5072 10K
- SMC\_TX\_L R5073 10K
- SMC\_RX\_L R5074 100K
- SMC\_BS\_ALRT\_L R5076 100K
- SMC\_TMS R5077 10K
- SMC\_TDO R5078 10K
- SMC\_TDI R5079 10K
- SMC\_TCK R5080 10K
- SMC\_P67 R5094 10K
- SMC\_P63 R5081 10K
- SMC\_P60 R5096 10K
- SMC\_PH4 R5082 10K
- SMC\_BATT\_TRICKLE\_EN\_L R5083 10K
- SMC\_BATT\_CHG\_EN R5084 10K
- SMC\_ADAPTER\_EN R5085 10K
- SMC\_CASE\_OPEN R5086 10K
- SMC\_BC\_ACOK R5087 470K
- SMC\_EXCARD\_CP R5088 10K
- PM\_SUS\_STAT\_L R5089 100K
- PM\_SLP\_S5\_L R5090 100K

**SMC Support**  
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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 46   | 88             |        |



LPC+ Connector

FWH\_INIT\_L Generation

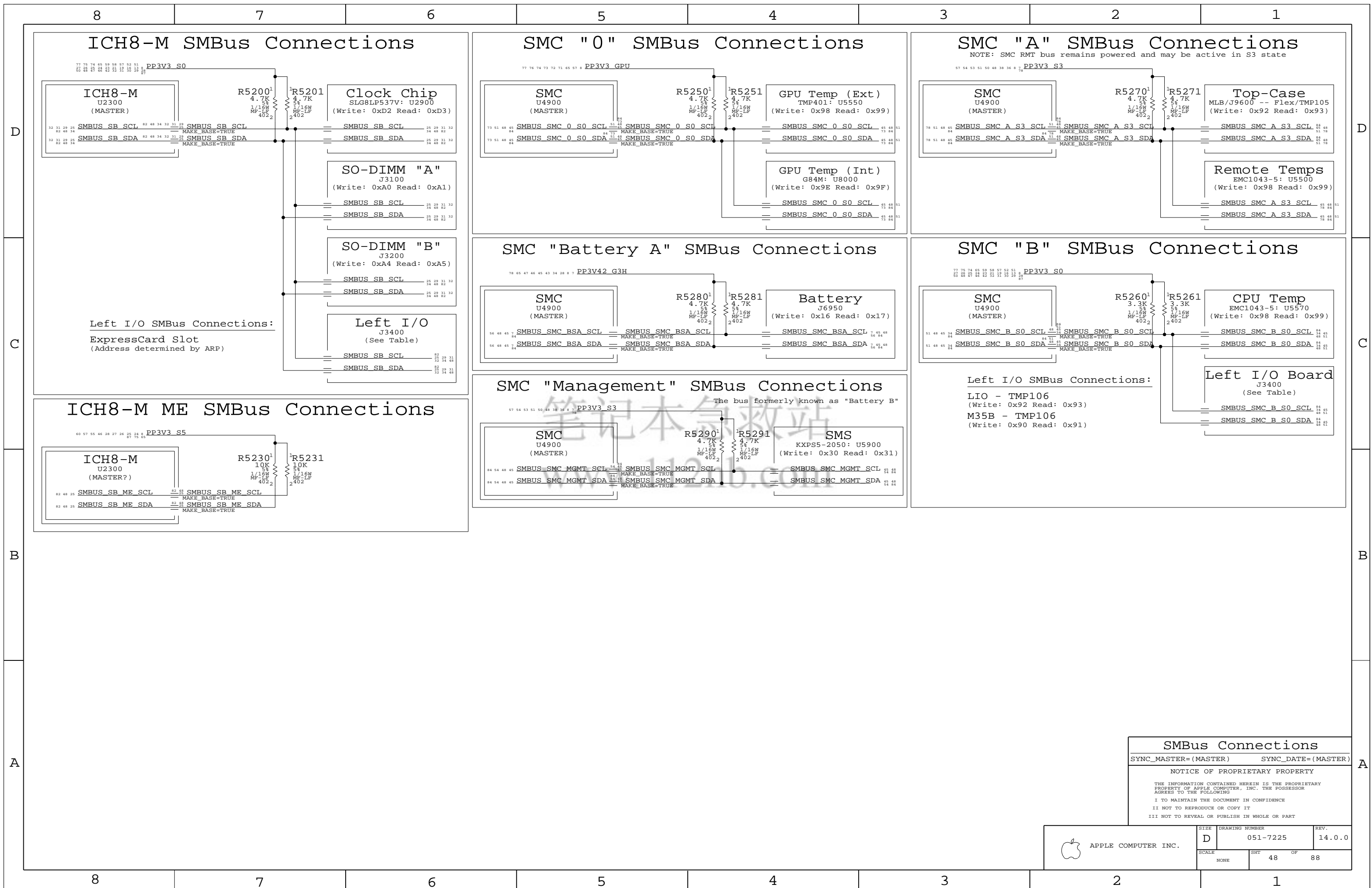
LPC+ Debug Connector

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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|                     | SCALE<br>NONE    | SHEET<br>47                | OF<br>88       |



**SMBus Connections**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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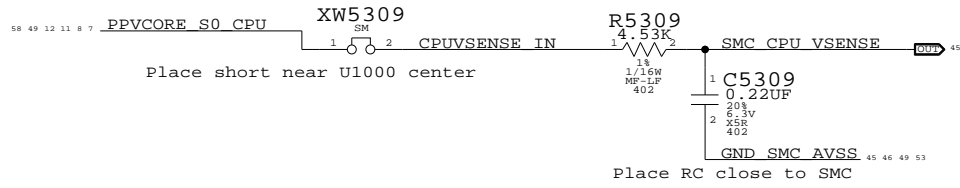
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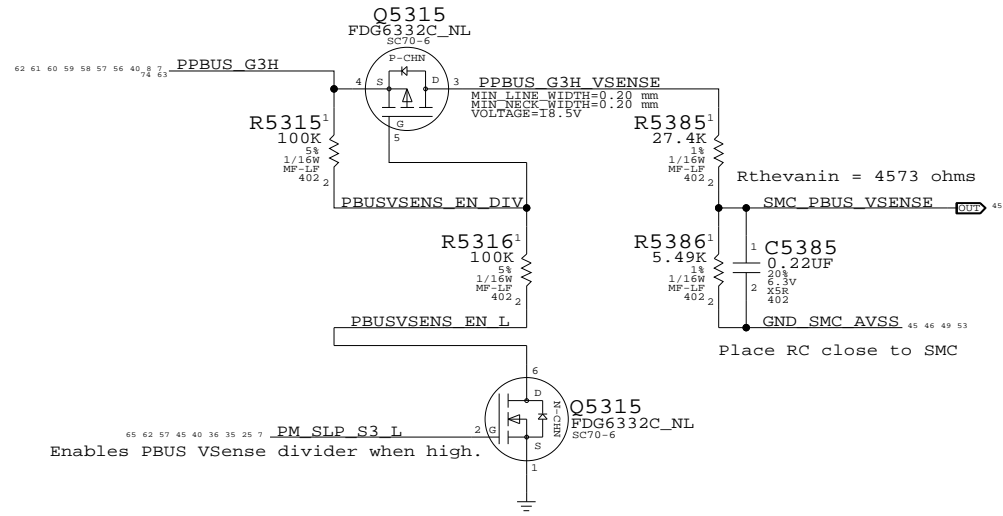
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|---------------------|------|----------------|--------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 48   | 88             |        |



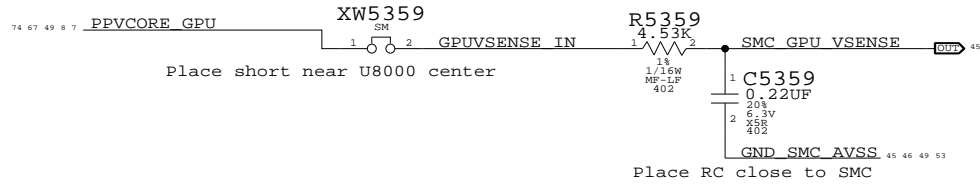
### CPU Voltage Sense / Filter



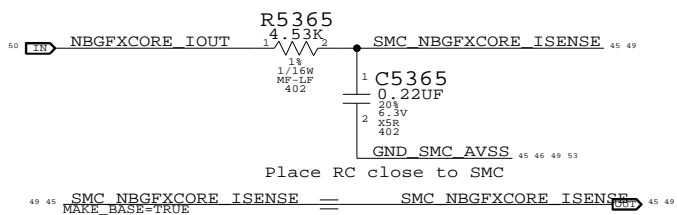
### PBUS Voltage Sense & Filter



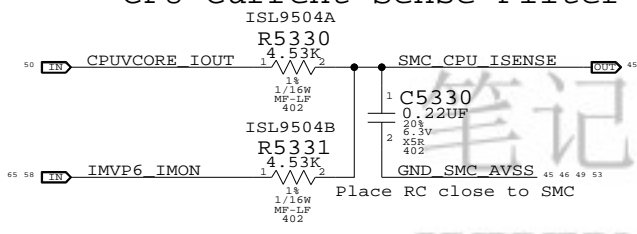
### GPU Voltage Sense / Filter



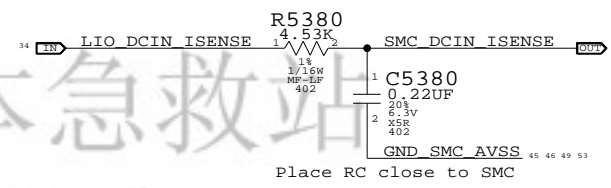
### NB GFX Current Sense Filter



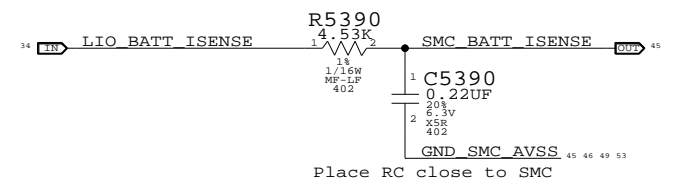
### CPU Current Sense Filter



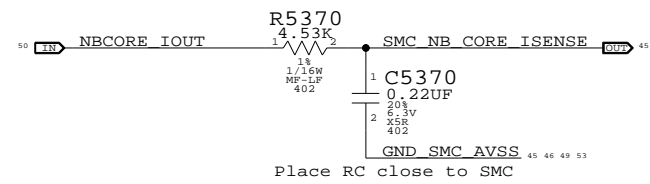
### DCIN Current Sense Filter



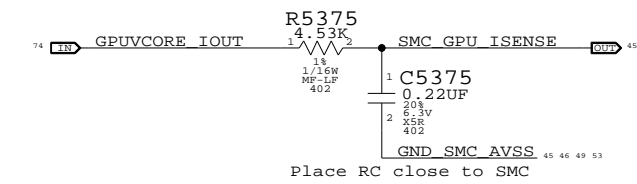
### Battery (PBUS) Current Sense Filter



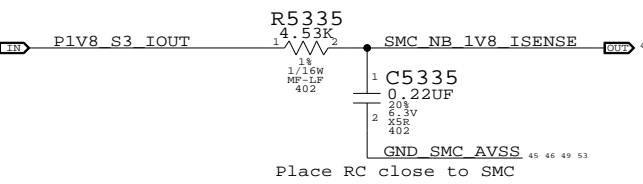
### NB Core Current Sense Filter



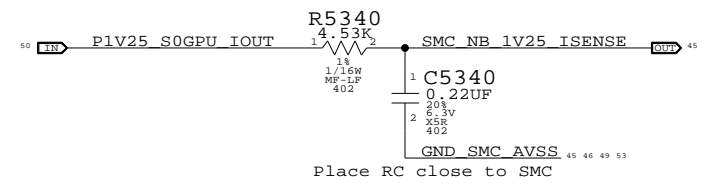
### GPU Current Sense Filter



### NB 1.8V Current Sense Filter

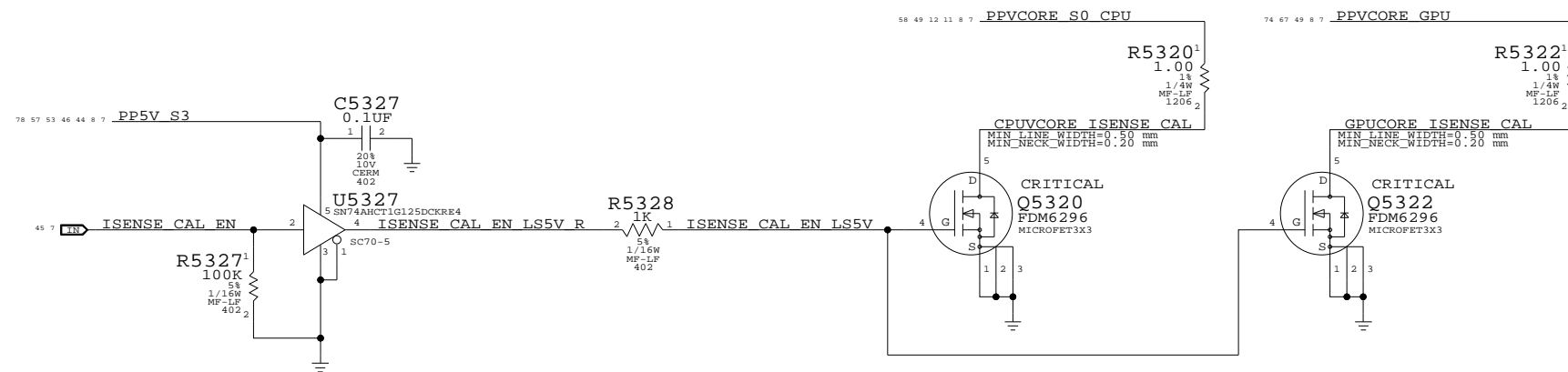


### S0/GPU 1.25V Current Sense Filter



## Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



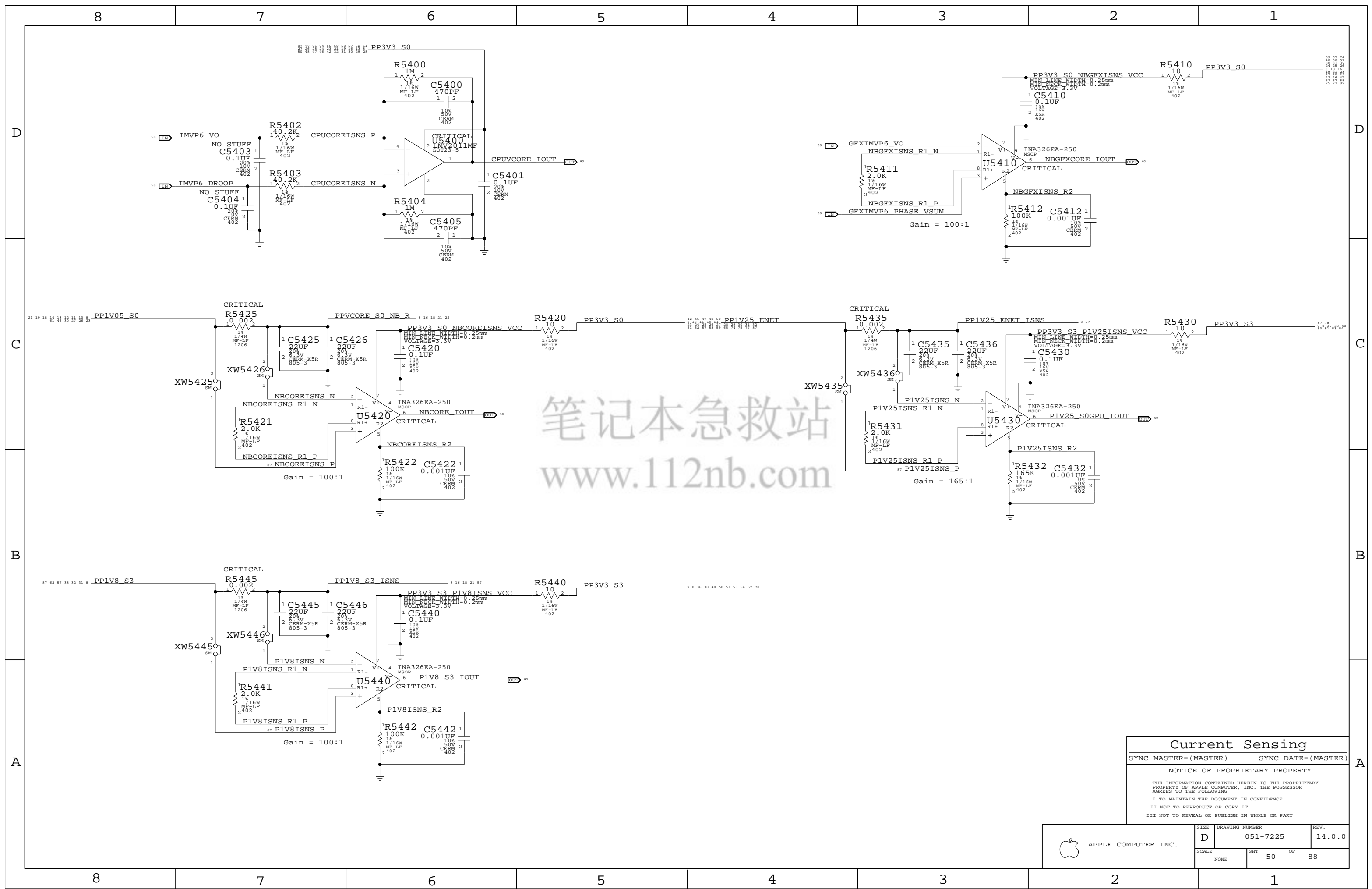
### Current & Voltage Sensing

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             | REV.   |
| NONE                | 49   | 88             |        |

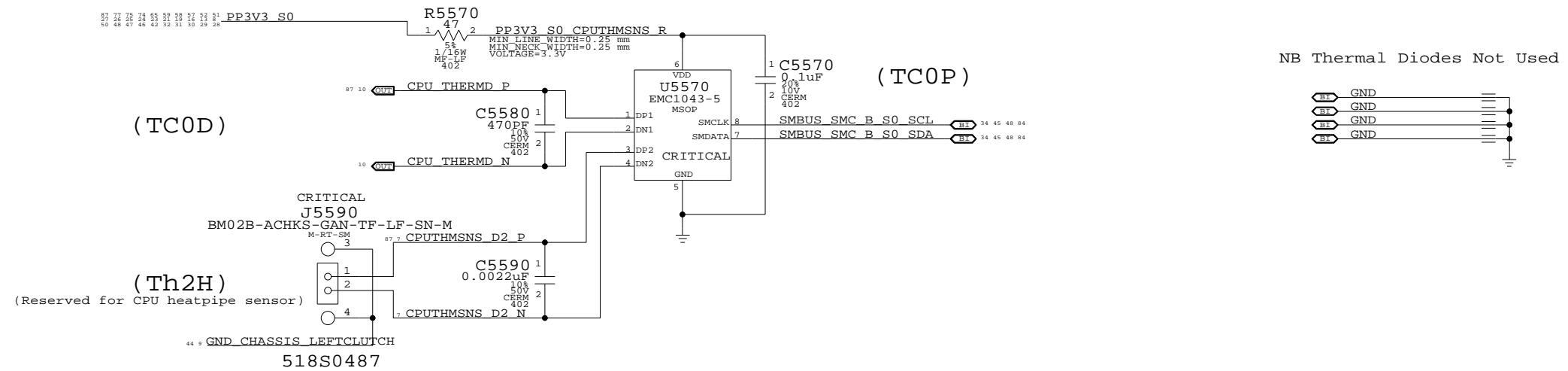


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| SCALE               | SHT  | OF             |        |
| NONE                | 50   | 88             |        |

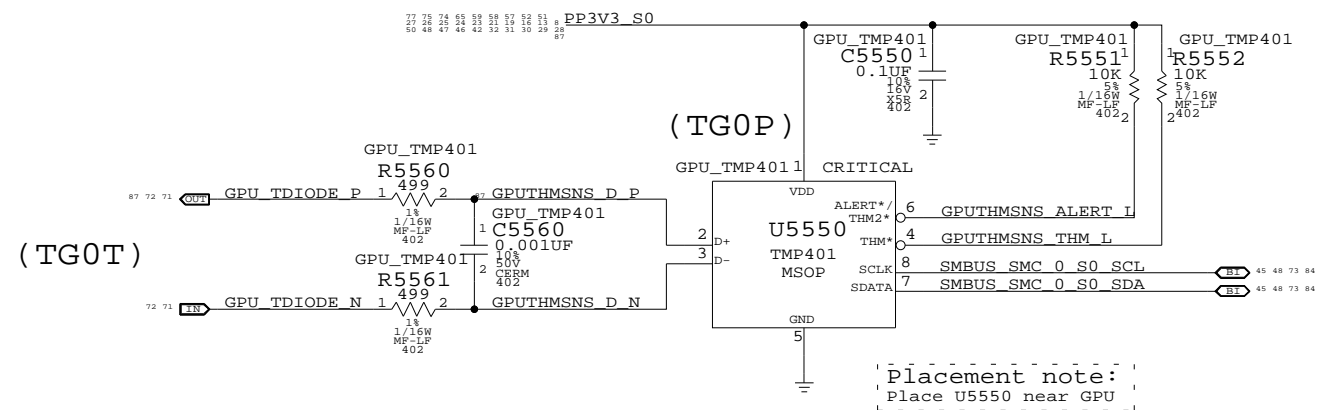
# CPU T-Diode Thermal Sensor



# GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



# GPU Die Thermal Sensor



**Thermal Sensors**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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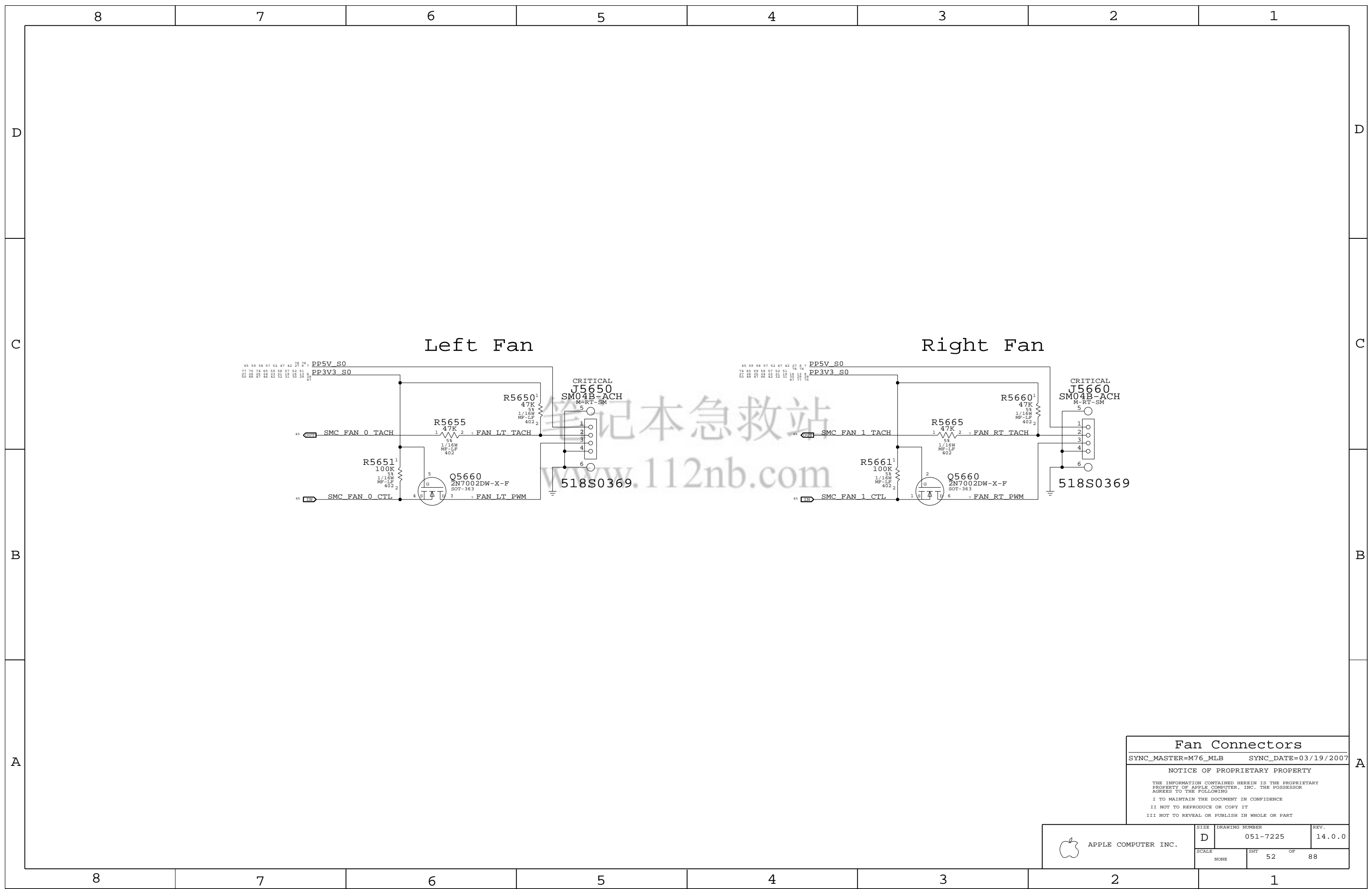
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             | 88     |
| NONE                | 51   | 88             |        |



**Fan Connectors**

SYNC\_MASTER=M76\_MLB      SYNC\_DATE=03/19/2007

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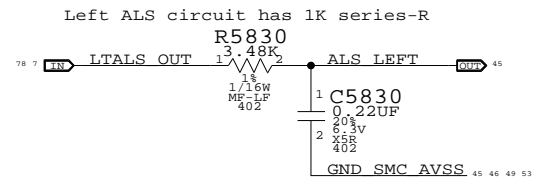
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

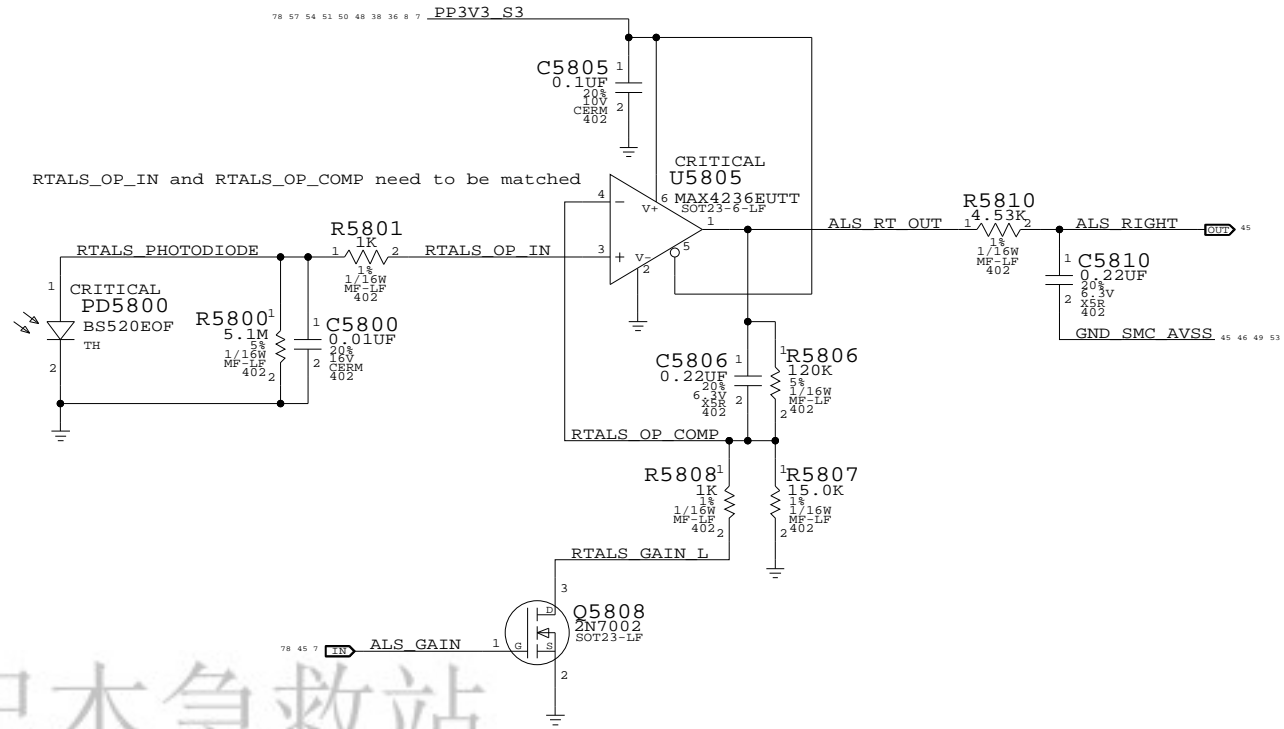
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

|                     |                  |                            |                |
|---------------------|------------------|----------------------------|----------------|
| APPLE COMPUTER INC. | SIZE<br><b>D</b> | DRAWING NUMBER<br>051-7225 | REV.<br>14.0.0 |
|                     | SCALE<br>NONE    | SHT<br>52                  | OF<br>88       |

### Left ALS Filter

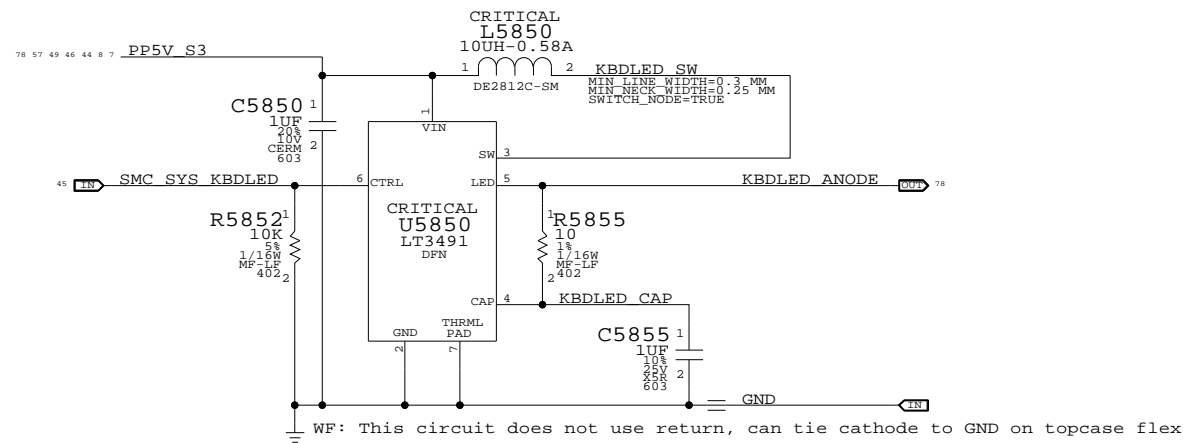


### Right ALS Circuit



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### Keyboard LED Driver



### ALS Support

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

#### NOTICE OF PROPRIETARY PROPERTY

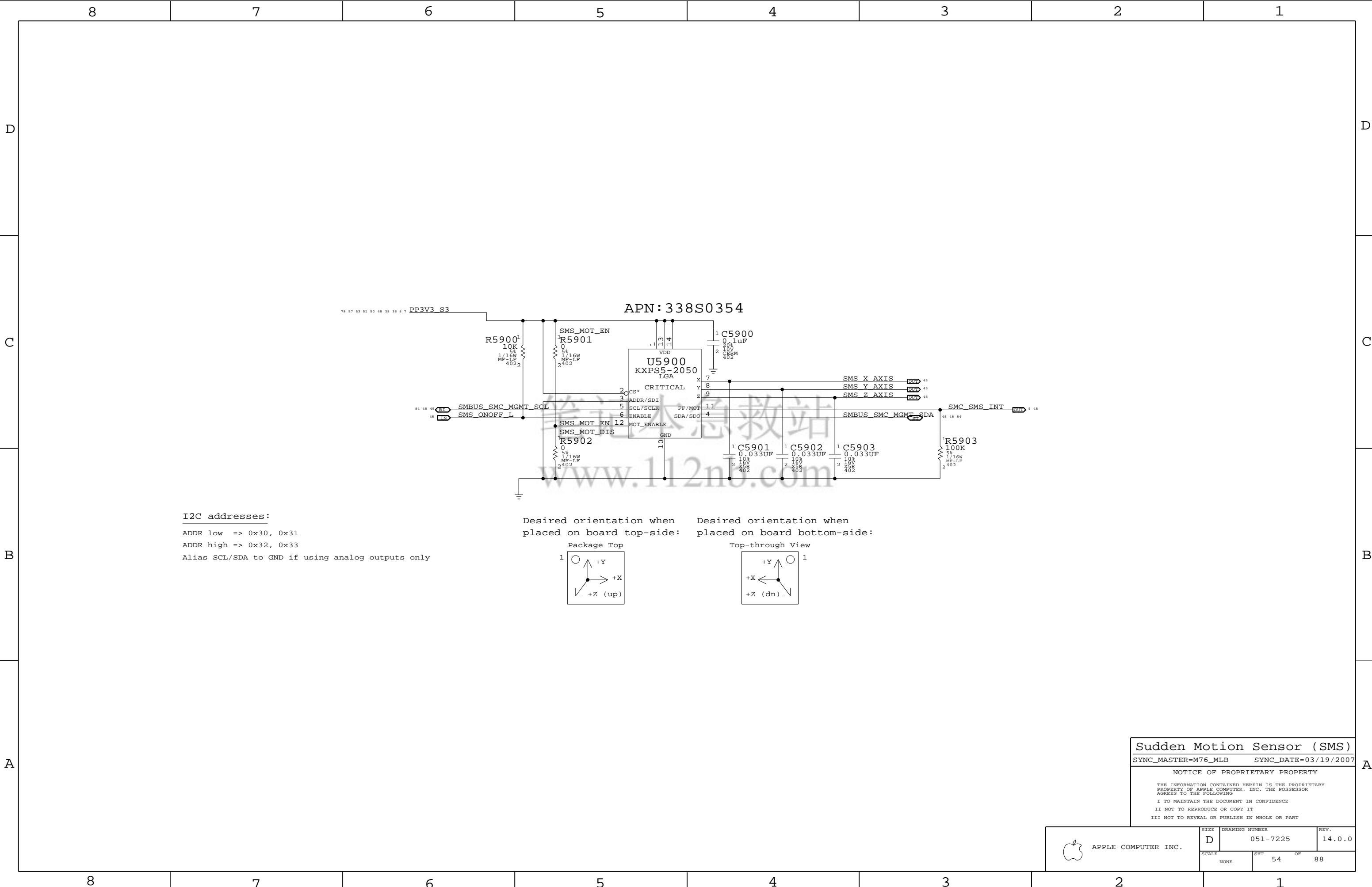
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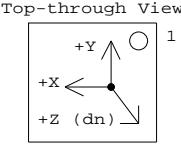
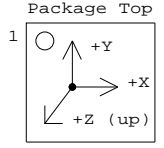
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|---------------------|------|----------------|--------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 53   | 88             |        |



APN: 338S0354

I2C addresses:  
 ADDR low => 0x30, 0x31  
 ADDR high => 0x32, 0x33  
 Alias SCL/SDA to GND if using analog outputs only

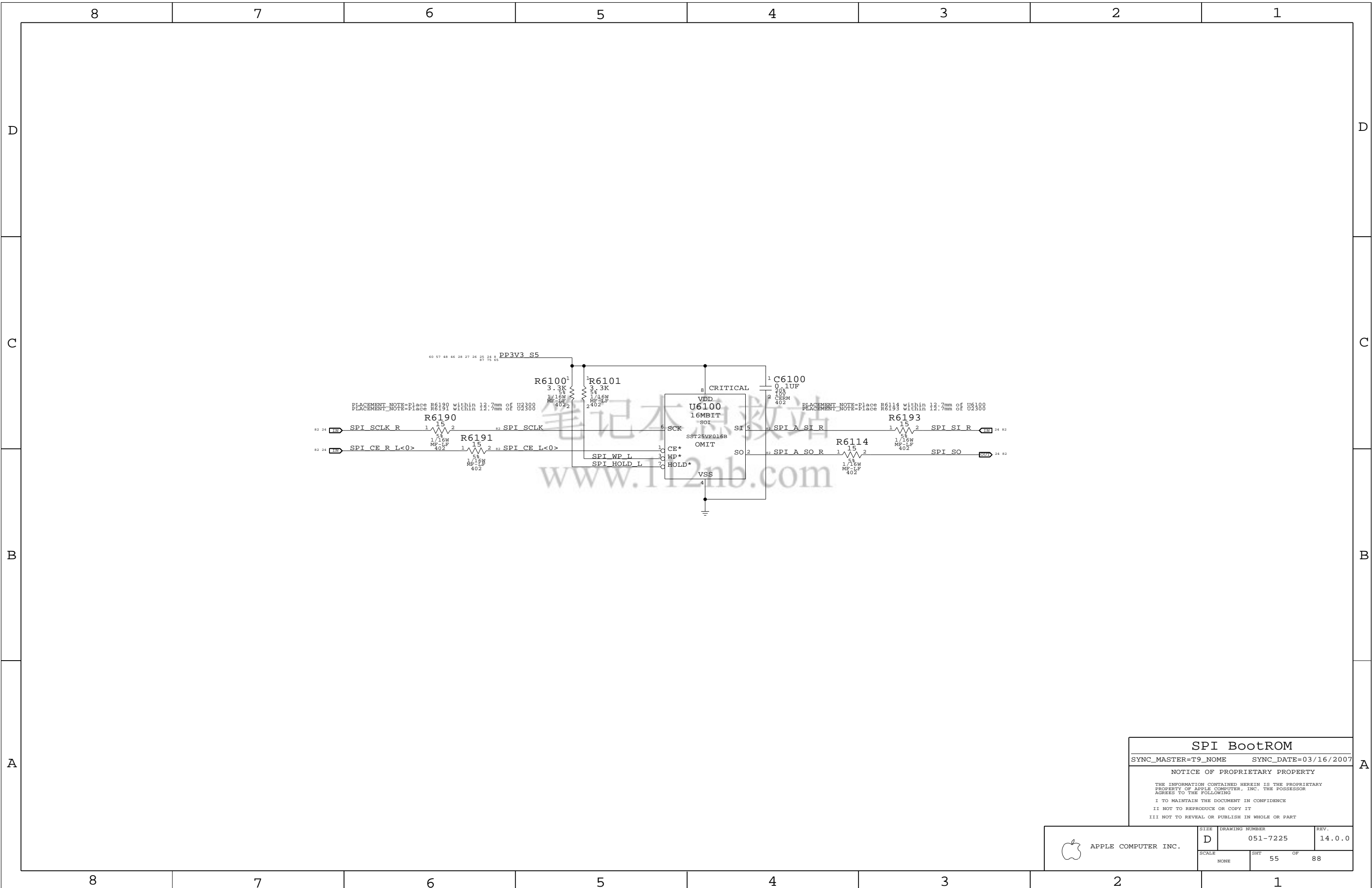
Desired orientation when placed on board top-side:      Desired orientation when placed on board bottom-side:



Sudden Motion Sensor (SMS)  
 SYNC\_MASTER=M76\_MLB      SYNC\_DATE=03/19/2007

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| SCALE               | SHT  |                | OF     |
| NONE                | 54   |                | 88     |



**SPI BootROM**

SYNC\_MASTER=T9\_NOME      SYNC\_DATE=03/16/2007

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| APPLE COMPUTER INC. | SIZE<br><b>D</b> | DRAWING NUMBER<br>051-7225 | REV.<br>14.0.0 |
|                     | SCALE<br>NONE    | SHEET<br>55                | OF<br>88       |

8

7

6

5

4

3

2

1

D

D

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C

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B

A

A

8

7

6

5

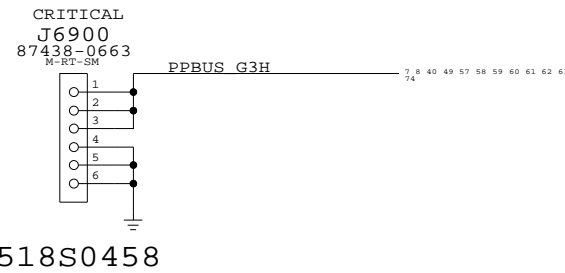
4

3

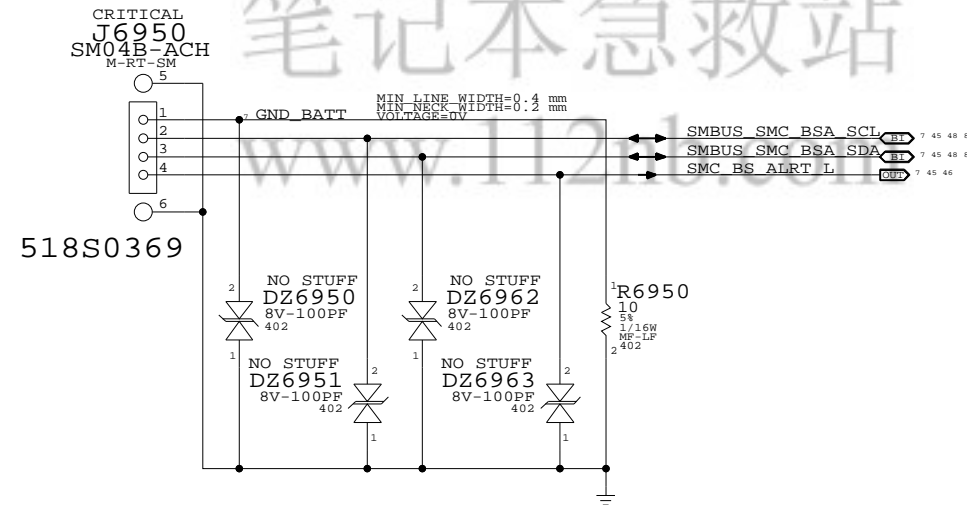
2

1

### Left I/O Power Connector



### Battery Connector (Digital Signals)



#### PBus-In & Battery Connectors

SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=09/09/2006

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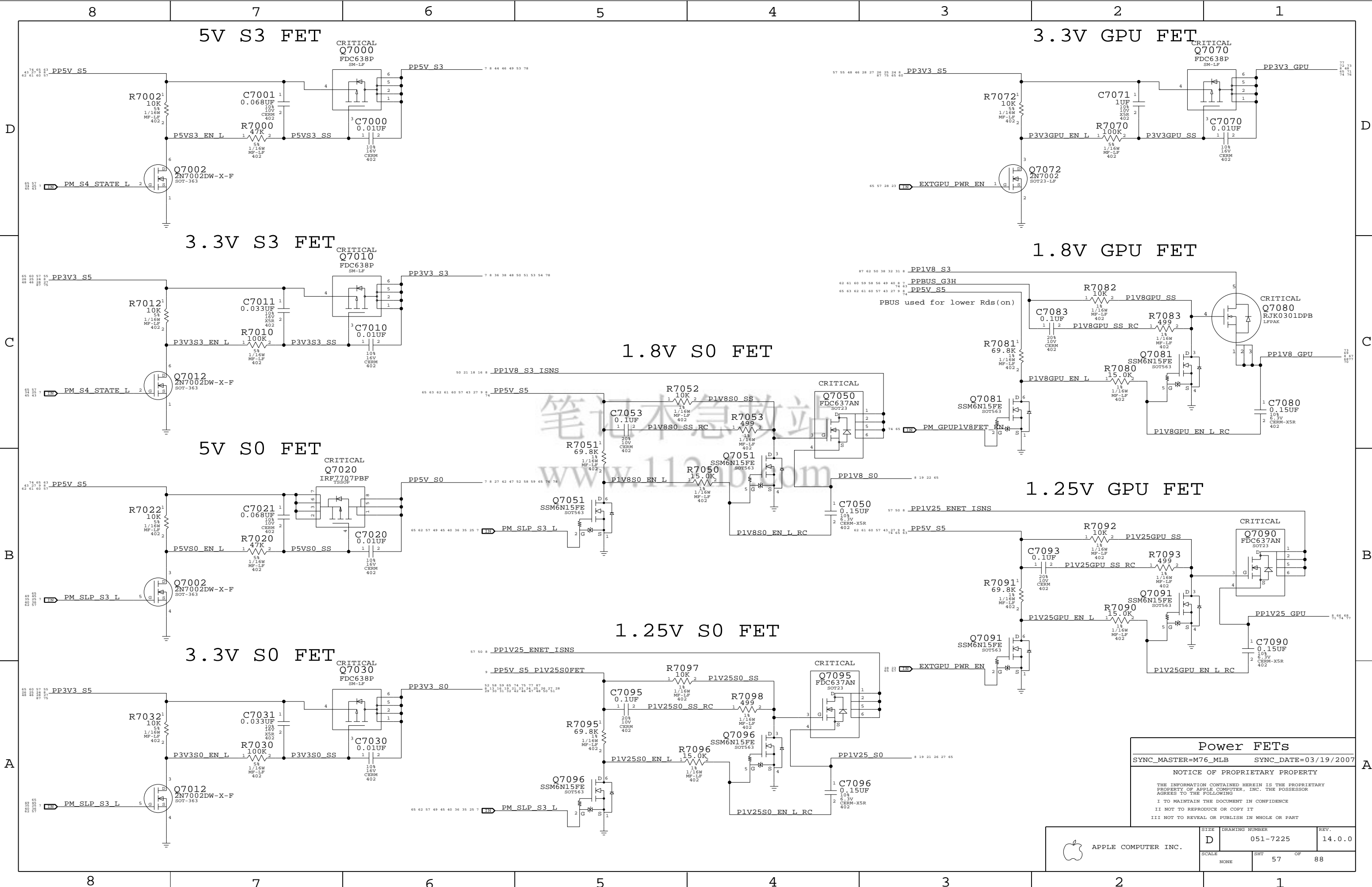
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
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| NONE                | 56   | 88             |        |

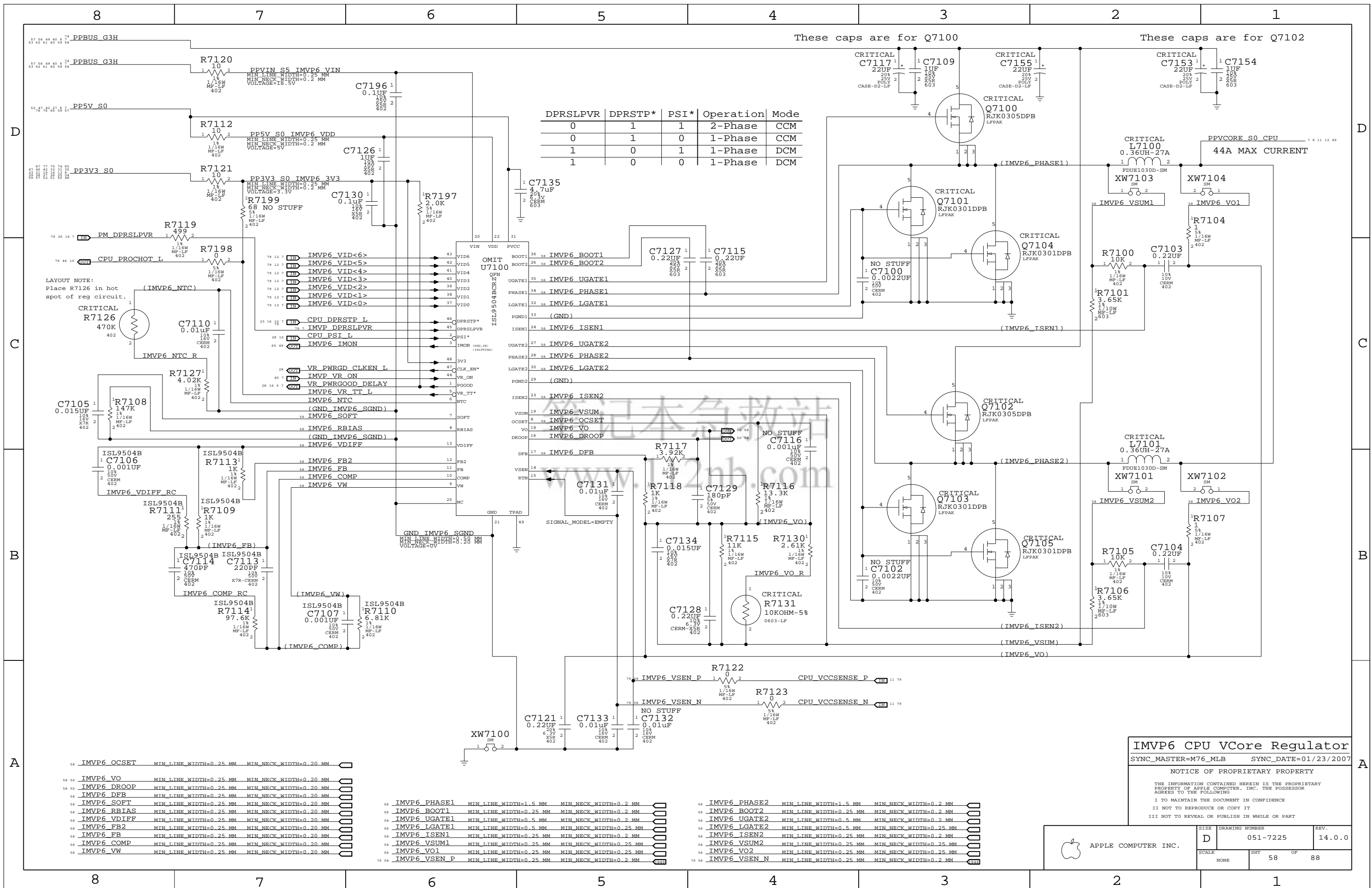




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**Power FETs**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007  
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| SCALE               | SHT  | OF             |        |
| NONE                | 57   | 88             |        |



| DPRSLPVR | DPRSTP* | PSI* | Operation | Mode |
|----------|---------|------|-----------|------|
| 0        | 1       | 1    | 2-Phase   | CCM  |
| 0        | 1       | 0    | 1-Phase   | CCM  |
| 1        | 0       | 1    | 1-Phase   | DCM  |
| 1        | 0       | 0    | 1-Phase   | DCM  |

These caps are for Q7100

These caps are for Q7102

www.123hb.com

**IMVP6 CPU VCore Regulator**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=01/23/2007

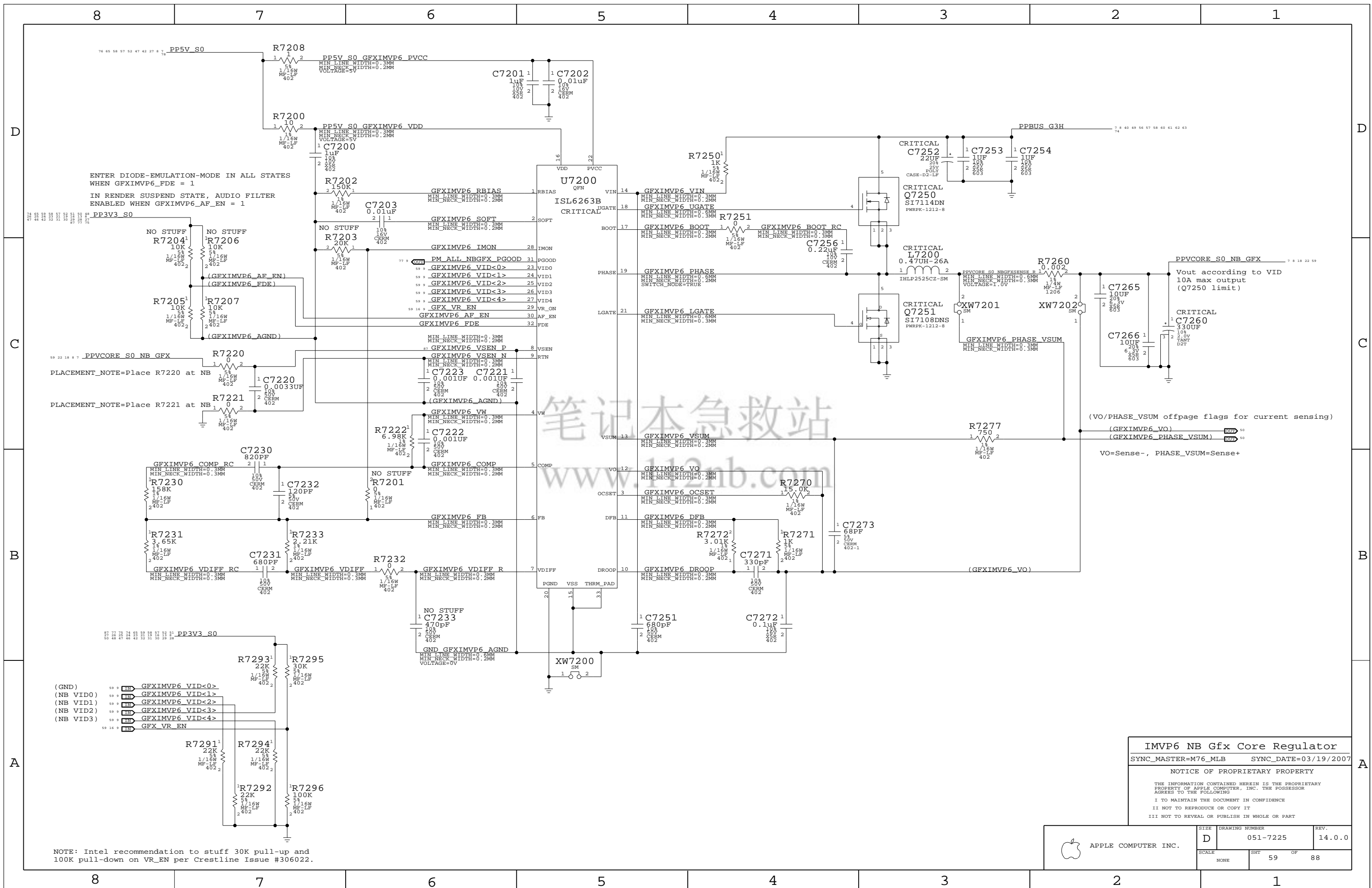
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|                     | D     | 051-7225       | 14.0.0 |
| SCALE               | SHEET | OF             |        |
| NONE                | 58    | OF             | 88     |

- 58 IMVP6\_OCSET MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_VO MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_DROOP MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_DFB MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_SOFT MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_RBIAS MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_VDIFF MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_FB2 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_FB MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_COMP MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM
- 58 IMVP6\_VW MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.20 MM

- 58 IMVP6\_PHASE1 MIN\_LINE\_WIDTH=1.5 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_BOOT1 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_UGATE1 MIN\_LINE\_WIDTH=0.5 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_LGATE1 MIN\_LINE\_WIDTH=0.5 MM MIN\_NECK\_WIDTH=0.25 MM
- 58 IMVP6\_ISEN1 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_VSUM1 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.25 MM
- 58 IMVP6\_VO1 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.25 MM
- 58 IMVP6\_VSEN\_P MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_PHASE2 MIN\_LINE\_WIDTH=1.5 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_BOOT2 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_UGATE2 MIN\_LINE\_WIDTH=0.5 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_LGATE2 MIN\_LINE\_WIDTH=0.5 MM MIN\_NECK\_WIDTH=0.25 MM
- 58 IMVP6\_ISEN2 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.2 MM
- 58 IMVP6\_VSUM2 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.25 MM
- 58 IMVP6\_VO2 MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.25 MM
- 58 IMVP6\_VSEN\_N MIN\_LINE\_WIDTH=0.25 MM MIN\_NECK\_WIDTH=0.2 MM



ENTER DIODE-EMULATION-MODE IN ALL STATES  
WHEN GFXIMVP6\_FDE = 1  
IN RENDER SUSPEND STATE, AUDIO FILTER  
ENABLED WHEN GFXIMVP6\_AF\_EN = 1

PLACEMENT\_NOTE=Place R7220 at NB  
PLACEMENT\_NOTE=Place R7221 at NB

(GND)  
GFXIMVP6 VID<0>  
GFXIMVP6 VID<1>  
GFXIMVP6 VID<2>  
GFXIMVP6 VID<3>  
GFXIMVP6 VID<4>  
GFX VR\_EN

NOTE: Intel recommendation to stuff 30K pull-up and 100K pull-down on VR\_EN per Crestline Issue #306022.

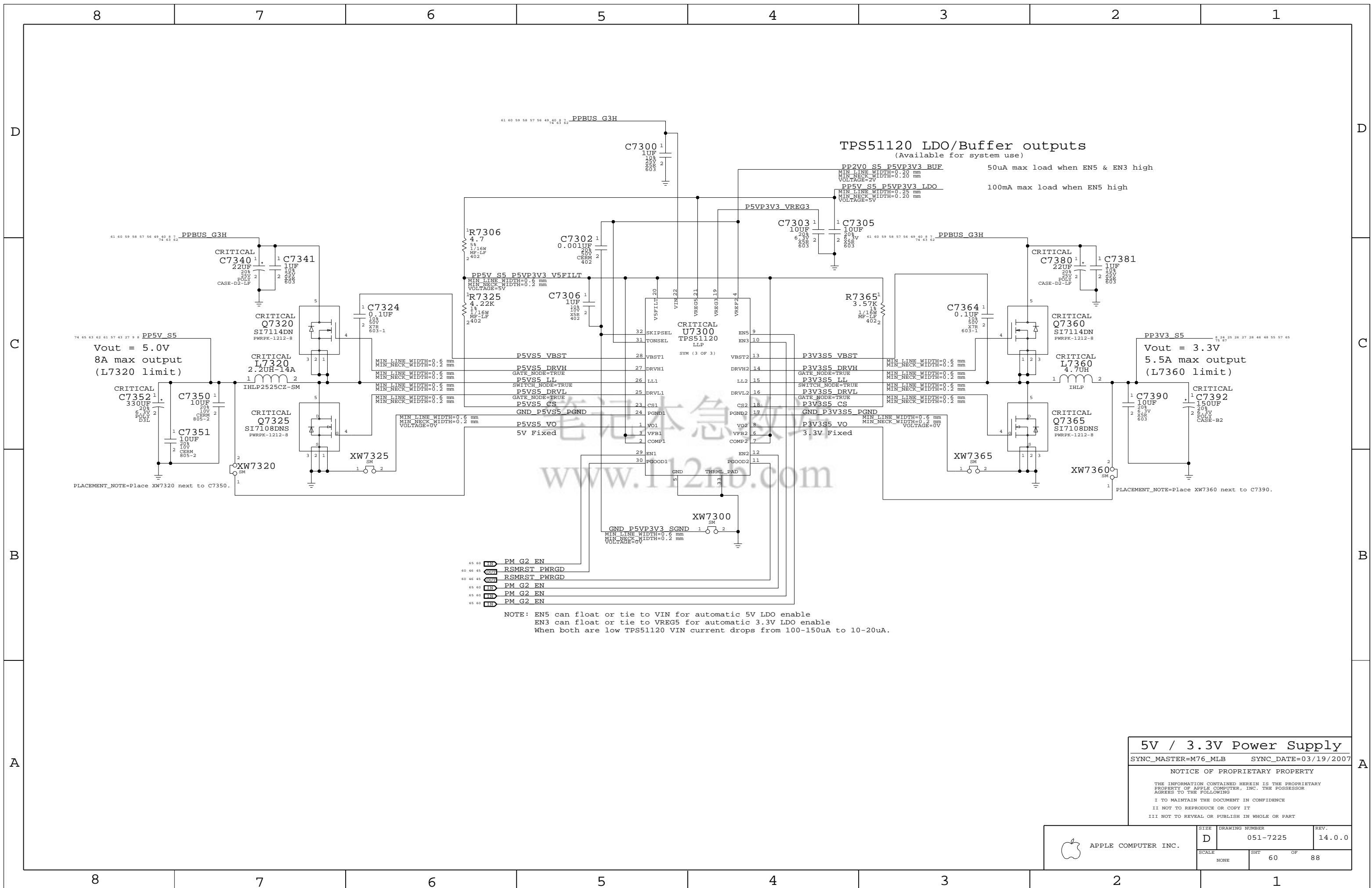
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|---------------|-----------|----------|------|----------------|--------|
| SCALE<br>NONE | SHT<br>59 | OF<br>88 | SIZE | DRAWING NUMBER | REV.   |
|               |           |          | D    | 051-7225       | 14.0.0 |

**IMVP6 NB Gfx Core Regulator**  
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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APPLE COMPUTER INC.



**TPS51120 LDO/Buffer outputs**  
 (Available for system use)

PP2V0\_S5\_P5VP3V3\_BUF 50uA max load when EN5 & EN3 high  
 MIN\_LINE\_WIDTH=0.20 mm  
 MIN\_NECK\_WIDTH=0.20 mm  
 VOLTAGE=2V

PP5V\_S5\_P5VP3V3\_LDO 100mA max load when EN5 high  
 MIN\_LINE\_WIDTH=0.25 mm  
 MIN\_NECK\_WIDTH=0.20 mm  
 VOLTAGE=5V

Vout = 5.0V  
 8A max output  
 (L7320 limit)

Vout = 3.3V  
 5.5A max output  
 (L7360 limit)

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable  
 EN3 can float or tie to VREG5 for automatic 3.3V LDO enable  
 When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

**5V / 3.3V Power Supply**

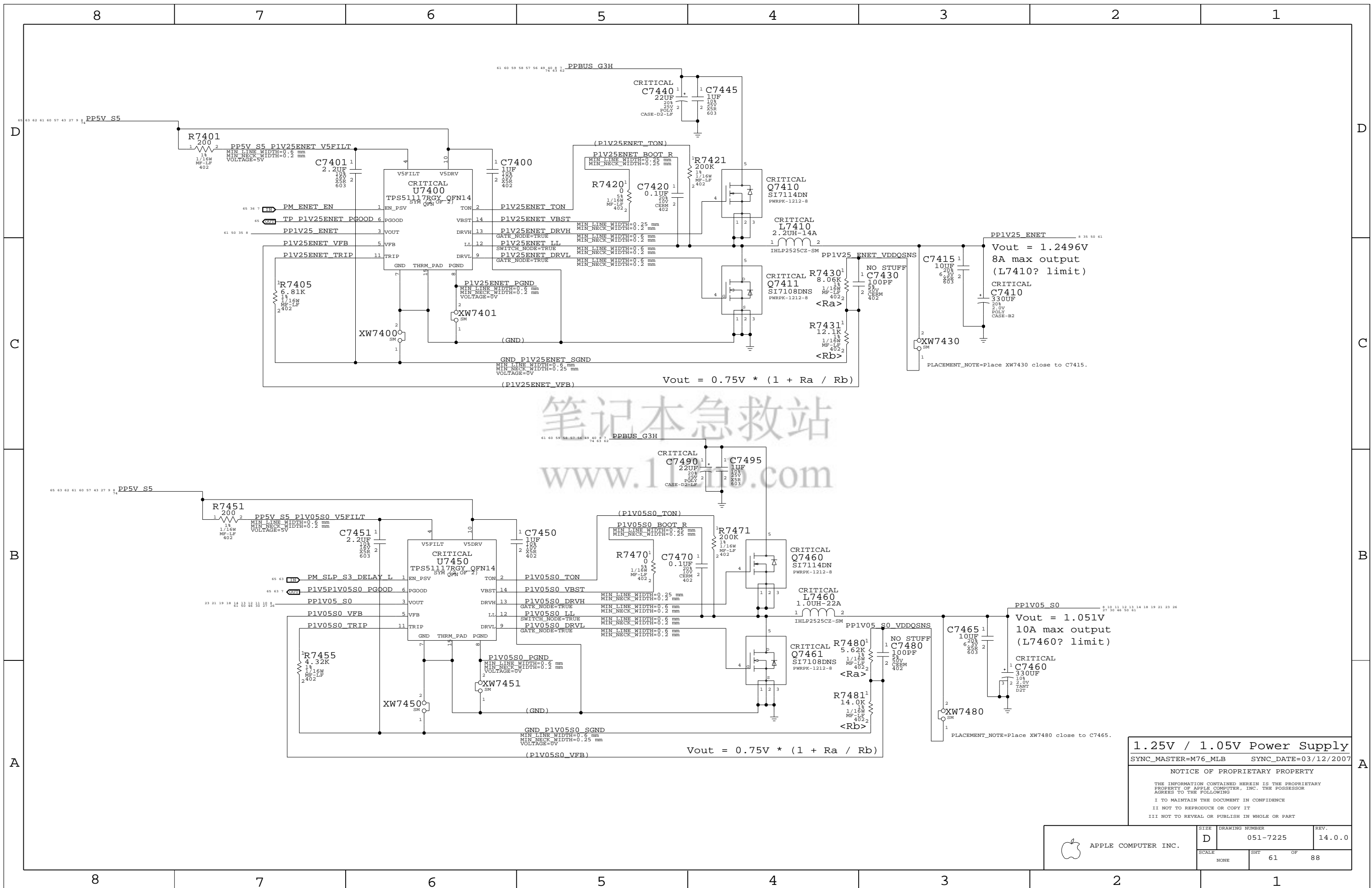
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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 60   | 88             |        |

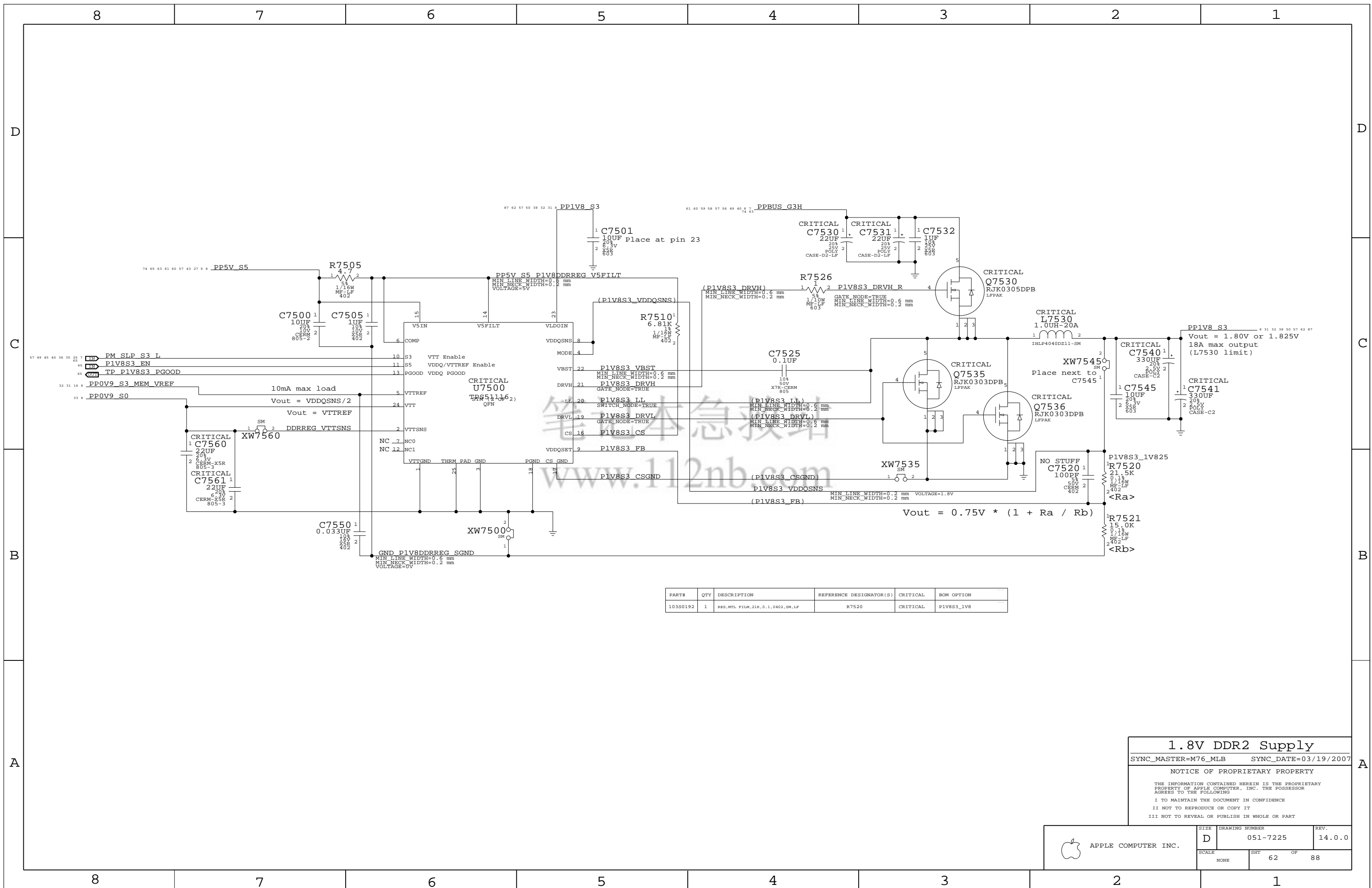


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www.111111.com

1.25V / 1.05V Power Supply  
SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 61   | 88             |        |



| PART#    | QTY | DESCRIPTION                     | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---------------------------------|-------------------------|----------|------------|
| 10380192 | 1   | RES,MTL FILM,21K,0.1,0402,SM,LF | R7520                   | CRITICAL | P1V8S3_1V8 |

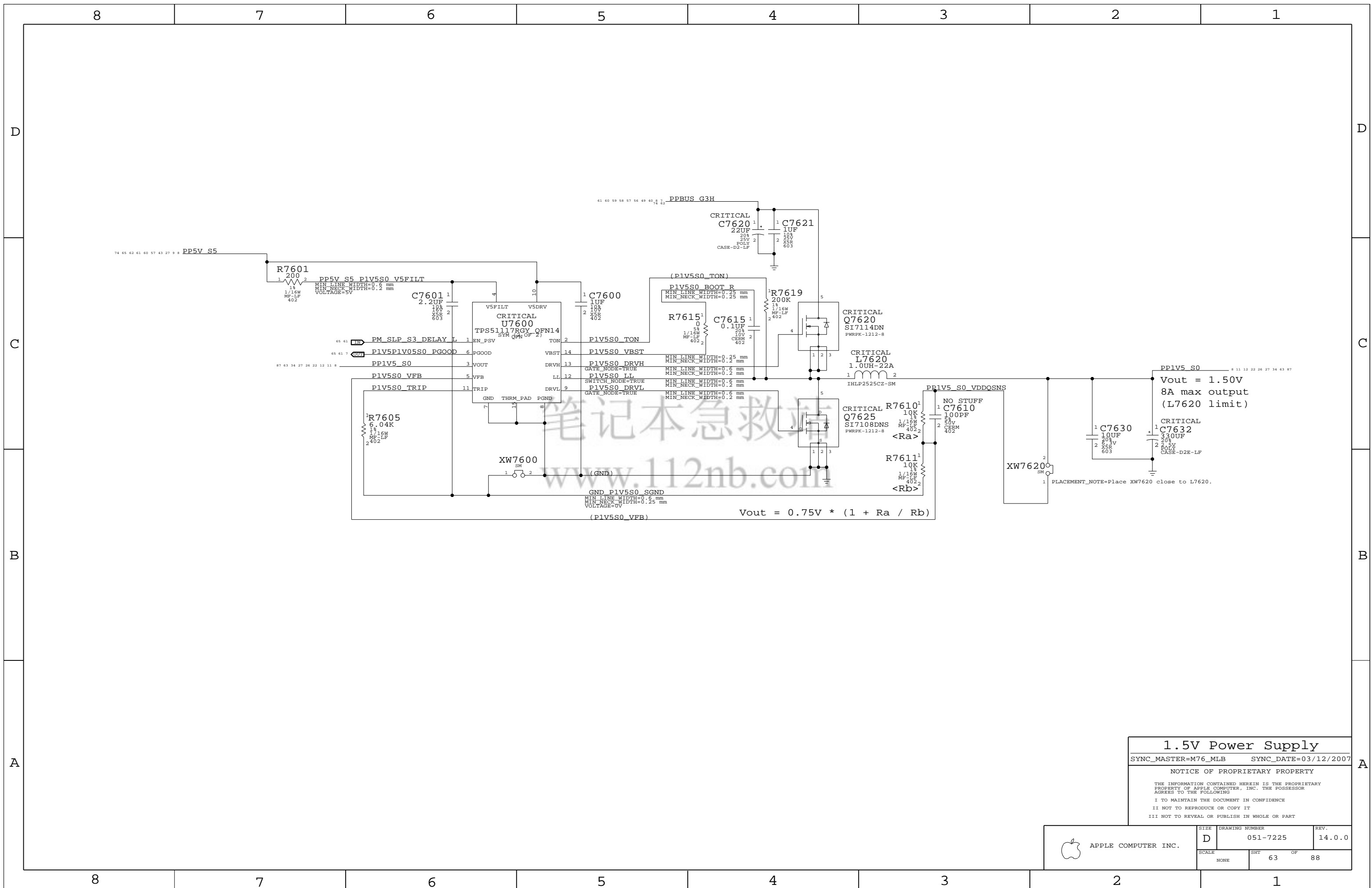
**1.8V DDR2 Supply**  
 SYNC\_MASTER=M76\_MLB    SYNC\_DATE=03/19/2007

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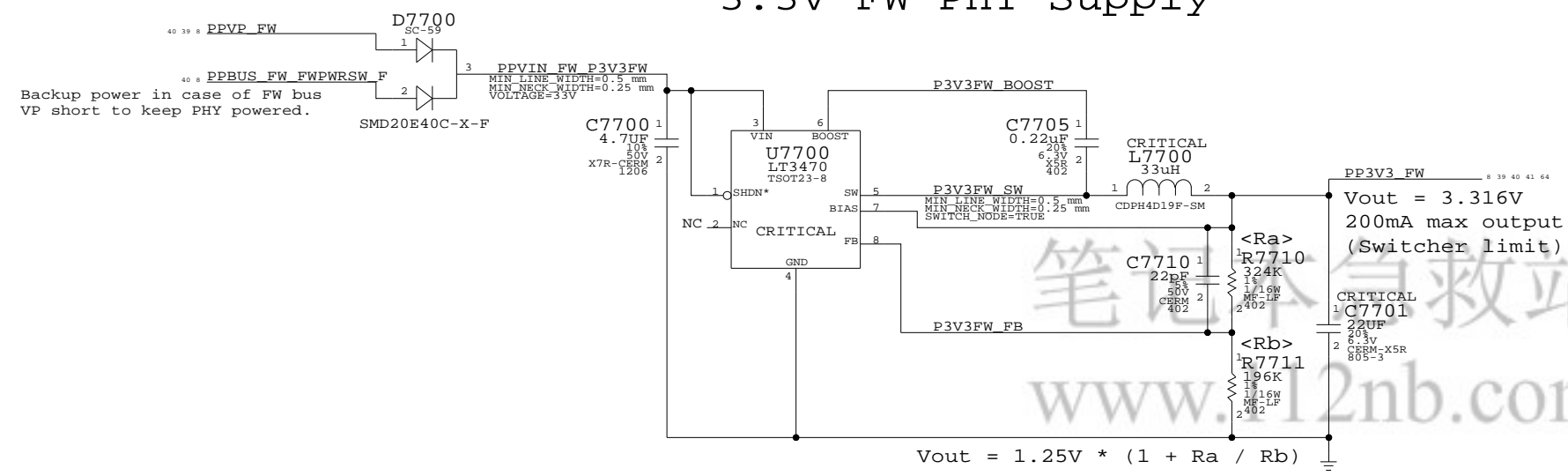
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| <br>APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                         | D    | 051-7225       | 14.0.0 |
| SCALE                   | SHT  | OF             | REV.   |
| NONE                    | 62   | 88             |        |



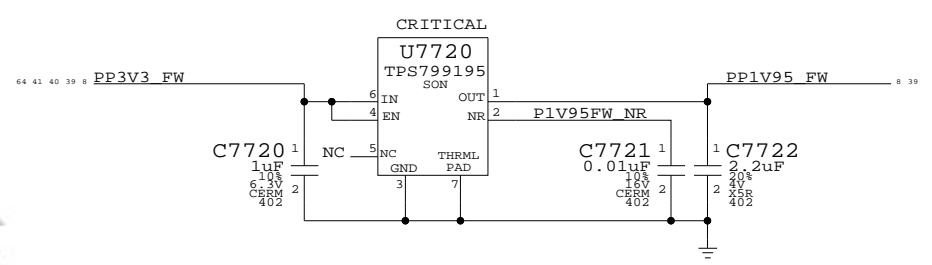
**1.5V Power Supply**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007  
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  |                | OF     |
| NONE                | 63   |                | 88     |

### 3.3V FW PHY Supply



### 1.95V FW PHY Supply



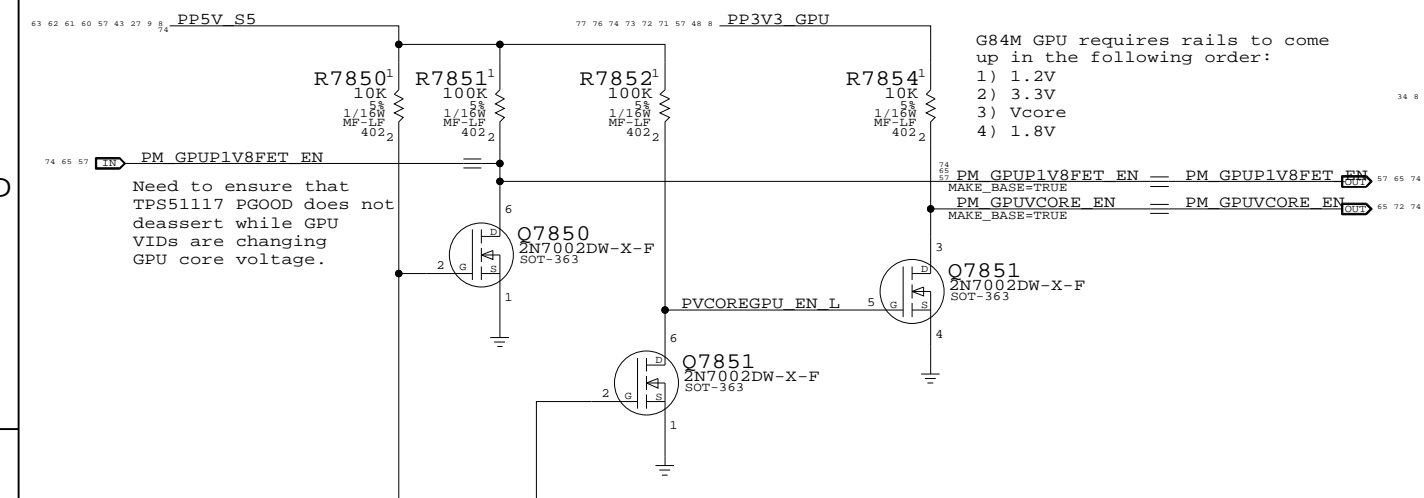
**FW PHY Power Supplies**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             | REV.   |
| NONE                | 64   | 88             |        |



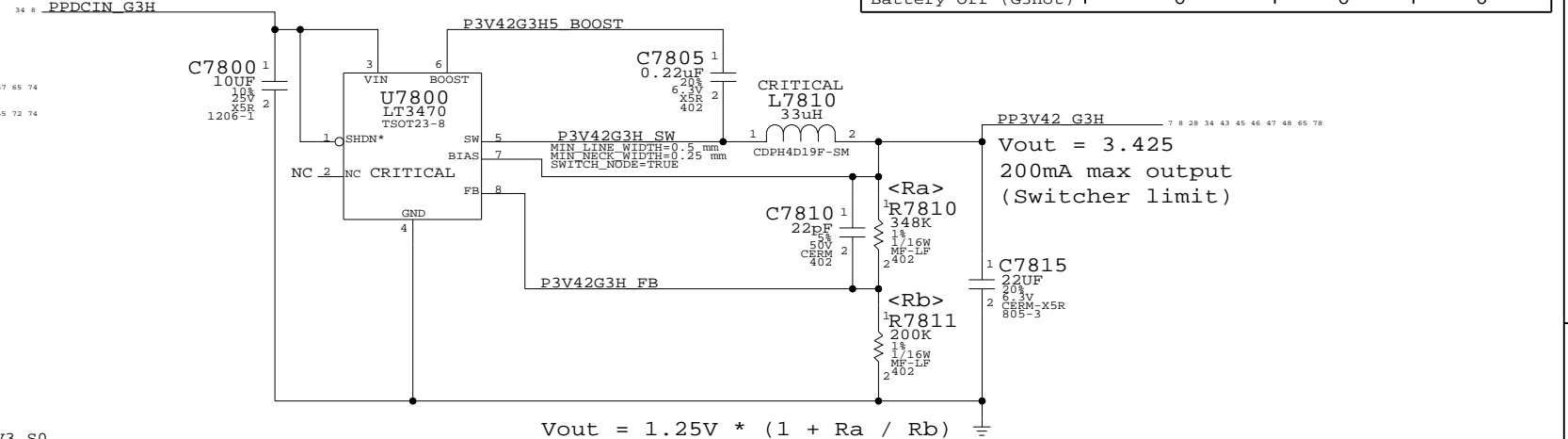
# Power Control Signals



# 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

| State               | SMC_PM_G2_ENABLE | PM_SLP_S4_L | PM_SLP_S3_L |
|---------------------|------------------|-------------|-------------|
| Run (S0)            | 1                | 1           | 1           |
| Sleep (S3)          | 1                | 1           | 0           |
| Soft-Off (S5)       | 1                | 0           | 0           |
| Battery Off (G3Hot) | 0                | 0           | 0           |

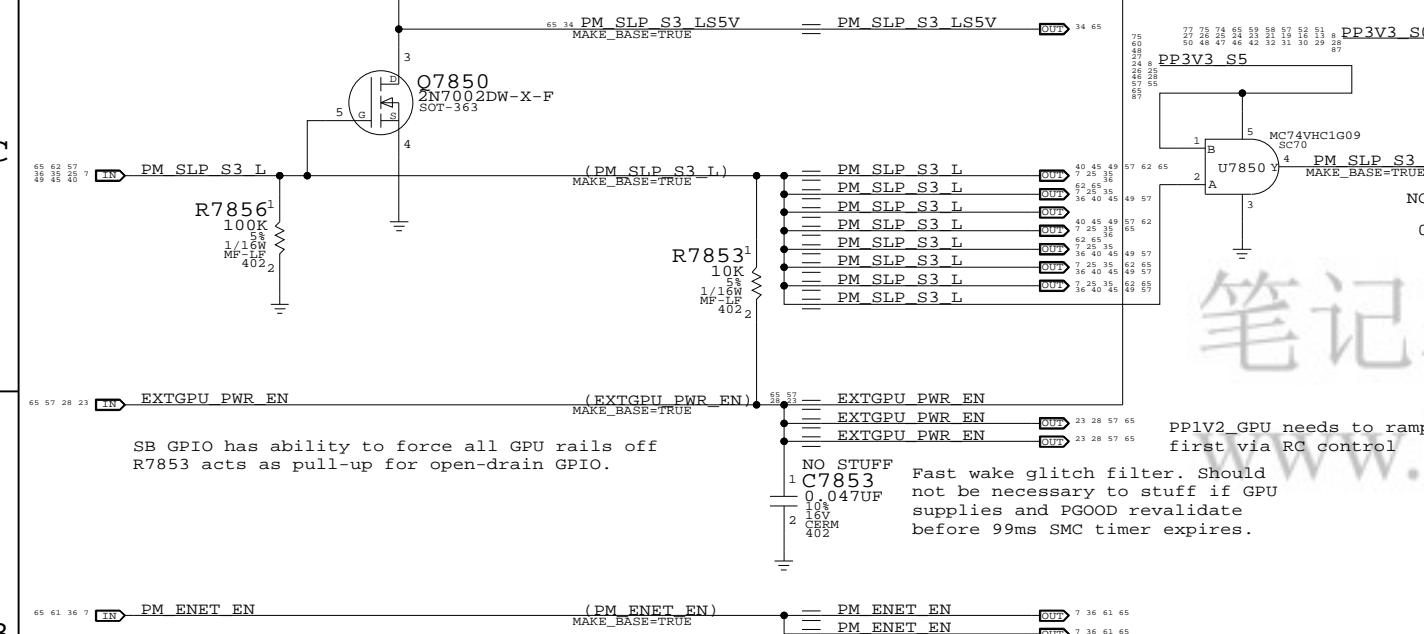


# Unused PGOOD Signals

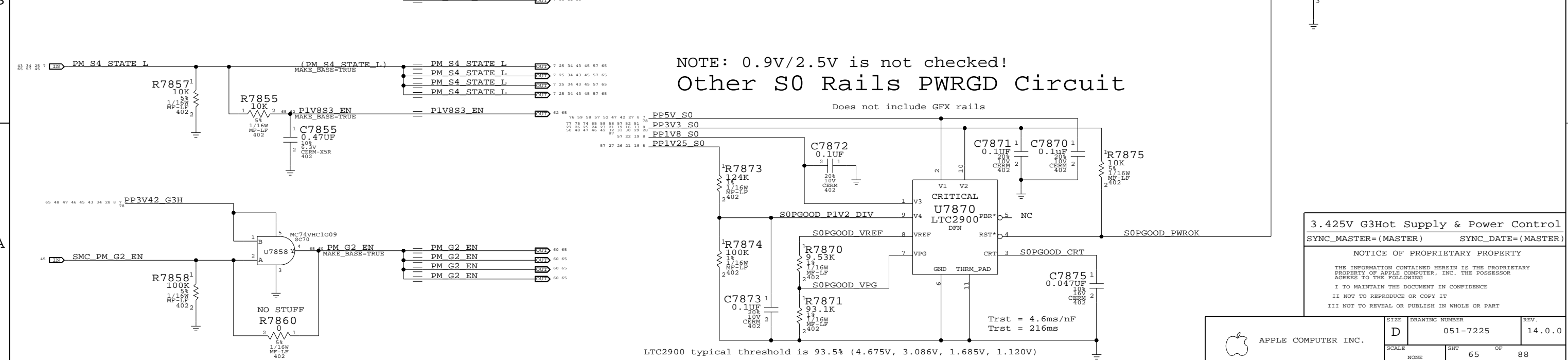
|                    |   |                    |
|--------------------|---|--------------------|
| TP P1V25ENET PGOOD | = | TP P1V25ENET PGOOD |
| TP P1V8S3 PGOOD    | = | TP P1V8S3 PGOOD    |

# 1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



# NOTE: 0.9V/2.5V is not checked! Other S0 Rails PWRGD Circuit



# 3.425V G3Hot Supply & Power Control

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|-------|----------------|--------|
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| SCALE | SHT            | OF     |
| NONE  | 65             | 88     |



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# Page Notes

Power aliases required by this page:

- =PP1V2\_GPU\_PEX\_PLLXVDD
- =PP1V2\_GPU\_PEX\_IOVDDQ
- =PP1V2\_GPU\_PEX\_IOVDD

Signal aliases required by this page:  
(NONE)

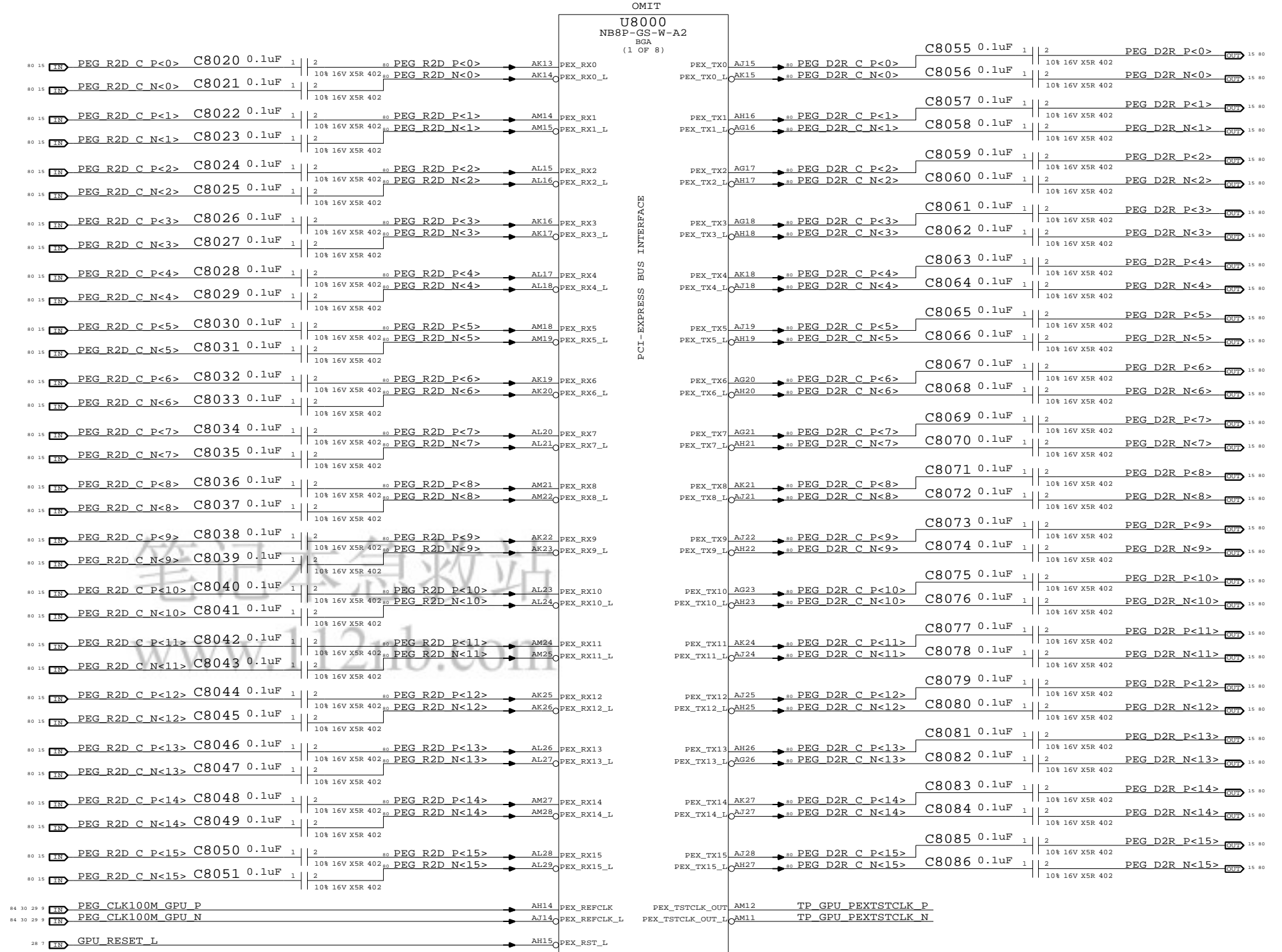
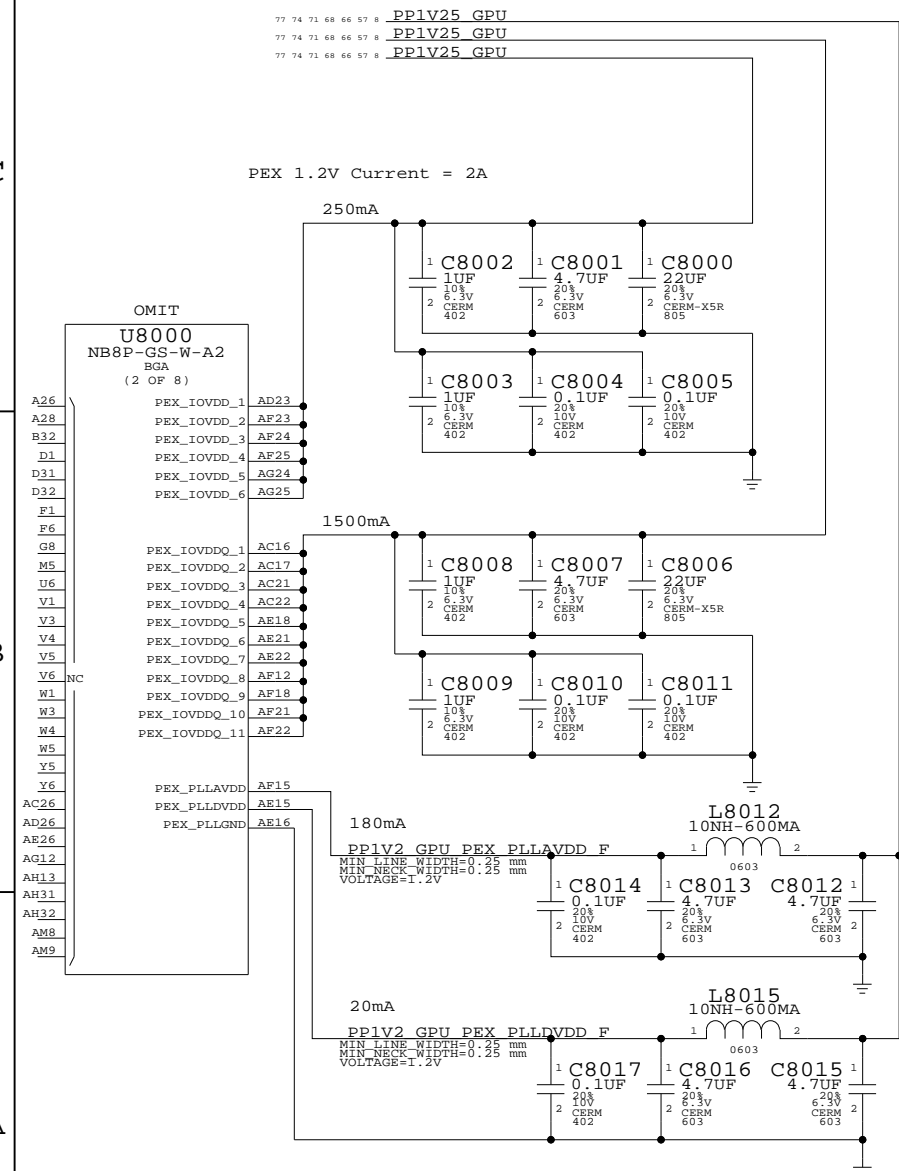
BOM options provided by this page:  
(NONE)

D

C

B

A



PCI EXPRESS BUS INTERFACE

NV G84M PCI-E  
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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| SCALE               | SHT  | OF             |        |
| NONE                | 66   | 88             |        |

# Page Notes

Power aliases required by this page:

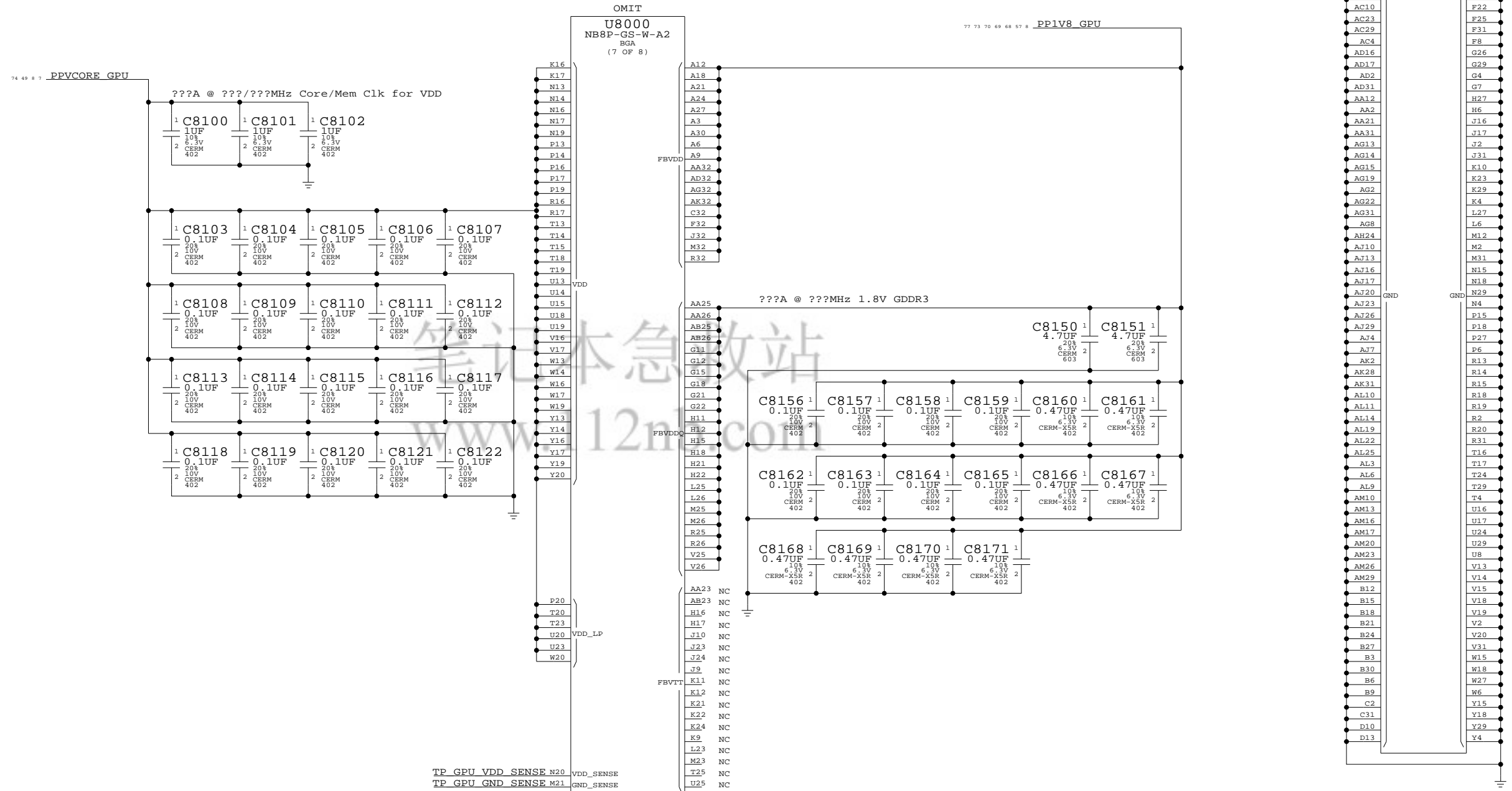
- =PPVCORE\_GPU
- =PP1V8\_GPU\_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



## NV G84M Core/FB Power

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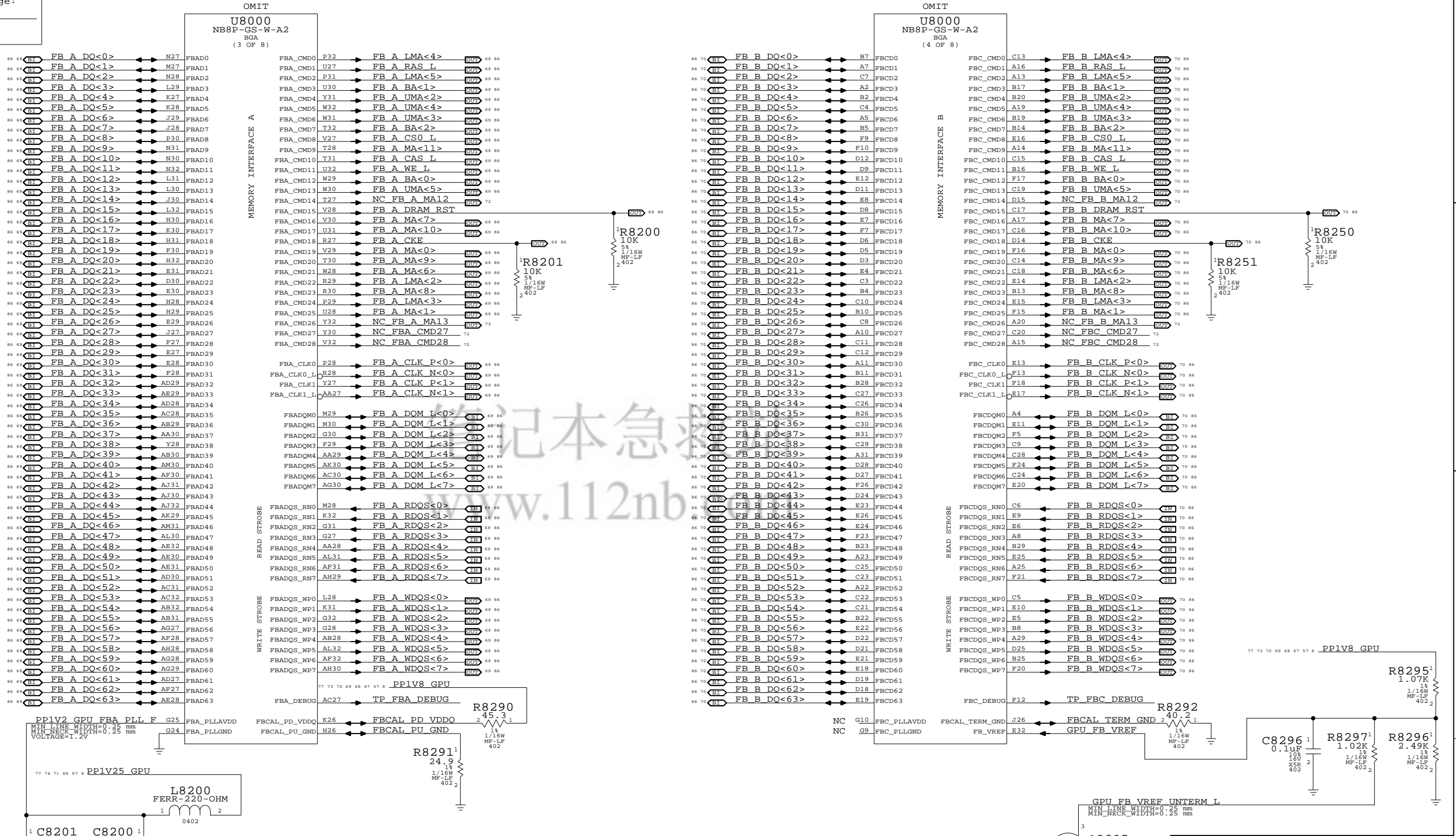
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|---------------------|------|----------------|--------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 67   | 88             |        |

# Page Notes

Power aliases required by this page:  
- =PPIV2\_GPU\_FBPLLAVDD  
- =PPIV8\_GPU\_FBIO

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



NV G84M Frame Buffer I/F  
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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| NONE  | 68             | 88     |



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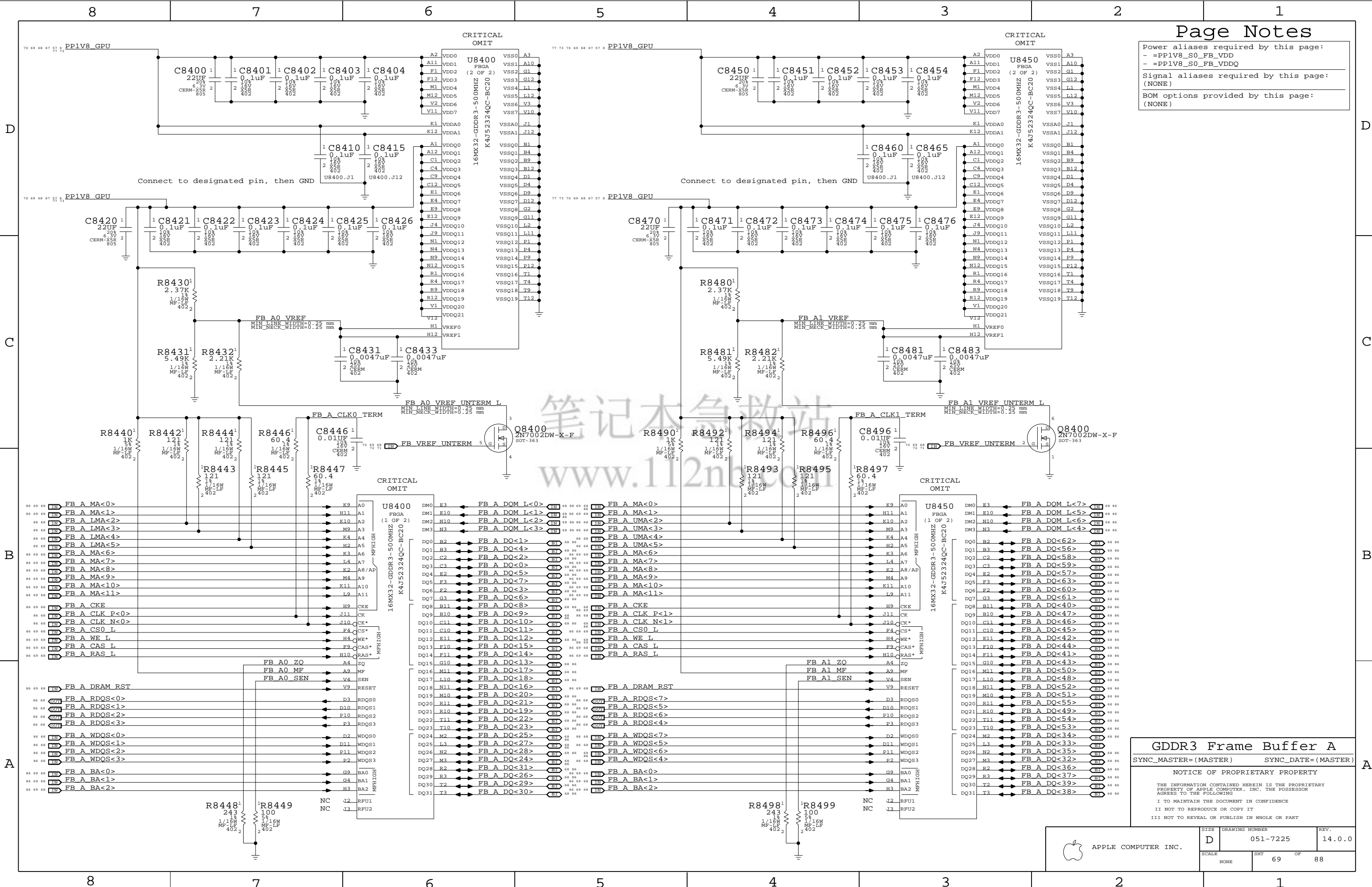
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- =PP1V8\_S0\_FB\_VDD  
- =PP1V8\_S0\_FB\_VDDQ  
Signal aliases required by this page:  
(NONE)  
BOM options provided by this page:  
(NONE)

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GDDR3 Frame Buffer A  
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|-------|----------------|--------|
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| D     | 051-7225       | 14.0.0 |
| SCALE | SHT            | OF     |
| NONE  | 69             | 88     |



8 7 6 5 4 3 2 1

D

D

C

C

B

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8 7 6 5 4 3 2 1

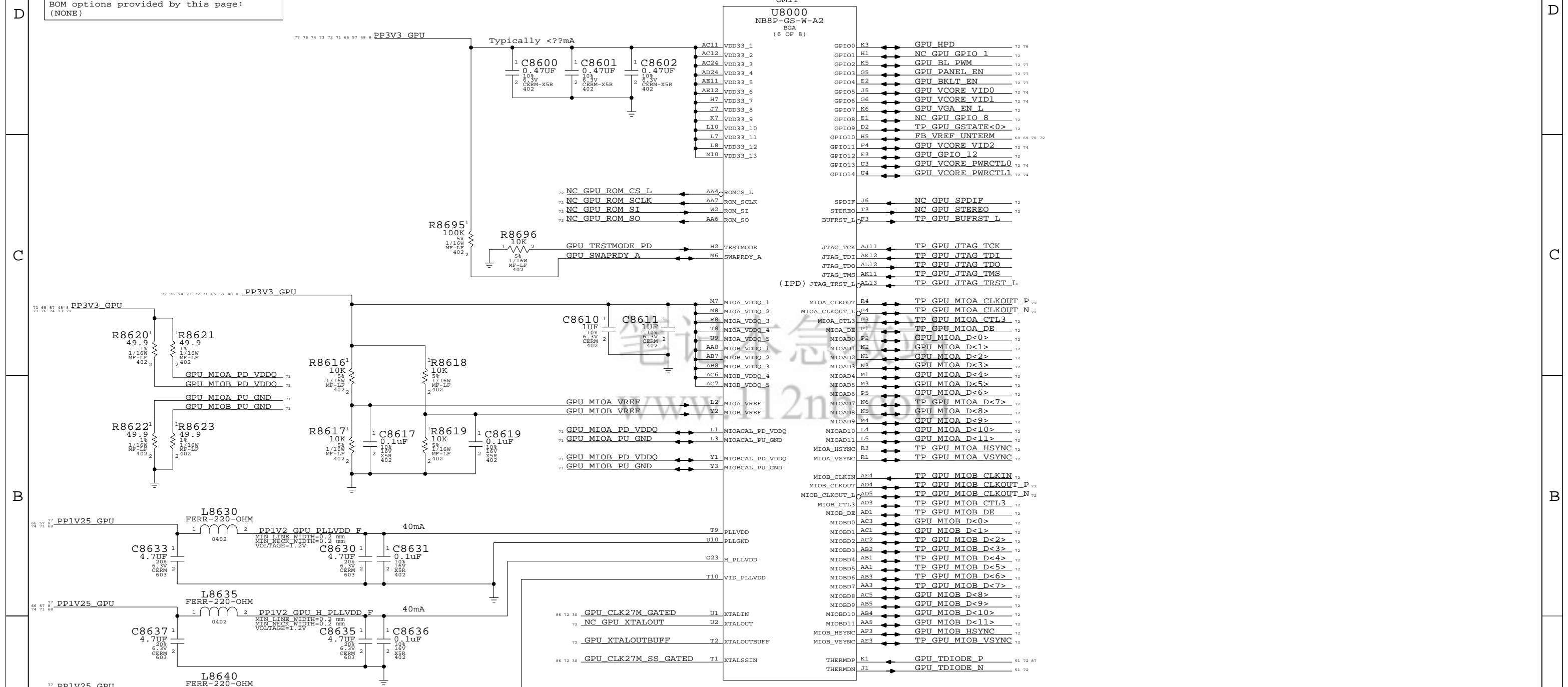


# Page Notes

Power aliases required by this page:  
 - =PP3V3\_GPU\_VDD33  
 - =PP3V3\_GPU\_MIO  
 - =PP1V2\_GPU\_PLLVDD  
 - =PP1V2\_GPU\_H\_PLLVDD  
 - =PP1V2\_GPU\_VID\_PLLVDD

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



OMIT

U8000  
NB8P-GS-W-A2  
BGA  
(6 OF 8)

|                   |      |                      |    |    |    |
|-------------------|------|----------------------|----|----|----|
| GPIO0             | K3   | GPU HPD              | 72 | 76 |    |
| GPIO1             | H1   | NC GPU GPIO 1        | 72 | 77 |    |
| GPIO2             | K5   | GPU BL PWM           | 72 | 77 |    |
| GPIO3             | G5   | GPU PANEL EN         | 72 | 77 |    |
| GPIO4             | E2   | GPU BKLT EN          | 72 | 77 |    |
| GPIO5             | J5   | GPU VCORE VID0       | 72 | 74 |    |
| GPIO6             | G6   | GPU VCORE VID1       | 72 | 74 |    |
| GPIO7             | K6   | GPU VGA EN L         | 72 | 74 |    |
| GPIO8             | E1   | NC GPU GPIO 8        | 72 | 74 |    |
| GPIO9             | D2   | TP GPU GSTATE<0>     | 72 | 74 |    |
| GPIO10            | H5   | FB VREF UNTERM       | 68 | 69 | 72 |
| GPIO11            | F4   | GPU VCORE VID2       | 72 | 74 |    |
| GPIO12            | E3   | GPU GPIO 12          | 72 | 74 |    |
| GPIO13            | U3   | GPU VCORE PWRCTL0    | 72 | 74 |    |
| GPIO14            | U4   | GPU VCORE PWRCTL1    | 72 | 74 |    |
| SPDIP             | J6   | NC GPU SPDIF         | 72 | 74 |    |
| STEREO            | T3   | NC GPU STEREO        | 72 | 74 |    |
| BUFRST_L          | F3   | TP GPU BUFRST L      | 72 | 74 |    |
| JTAG_TCK          | AJ11 | TP GPU JTAG TCK      | 72 | 74 |    |
| JTAG_TDI          | AK12 | TP GPU JTAG TDI      | 72 | 74 |    |
| JTAG_TDO          | AL12 | TP GPU JTAG TDO      | 72 | 74 |    |
| JTAG_TMS          | AK11 | TP GPU JTAG TMS      | 72 | 74 |    |
| (IPD) JTAG_TRST_L | AL13 | TP GPU JTAG TRST L   | 72 | 74 |    |
| MIOA_CLKOUT       | R4   | TP GPU MIOA_CLKOUT_P | 72 | 74 |    |
| MIOA_CLKOUT_L     | P4   | TP GPU MIOA_CLKOUT_N | 72 | 74 |    |
| MIOA_CTL3         | P3   | TP GPU MIOA_CTL3     | 72 | 74 |    |
| MIOA_DE           | P1   | TP GPU MIOA DE       | 72 | 74 |    |
| MIOA_D0           | P2   | GPU MIOA D<0>        | 72 | 74 |    |
| MIOA_D1           | N2   | GPU MIOA D<1>        | 72 | 74 |    |
| MIOA_D2           | N1   | GPU MIOA D<2>        | 72 | 74 |    |
| MIOA_D3           | N3   | GPU MIOA D<3>        | 72 | 74 |    |
| MIOA_D4           | M1   | GPU MIOA D<4>        | 72 | 74 |    |
| MIOA_D5           | M3   | GPU MIOA D<5>        | 72 | 74 |    |
| MIOA_D6           | P5   | GPU MIOA D<6>        | 72 | 74 |    |
| MIOA_D7           | N6   | TP GPU MIOA D<7>     | 72 | 74 |    |
| MIOA_D8           | N5   | GPU MIOA D<8>        | 72 | 74 |    |
| MIOA_D9           | M4   | GPU MIOA D<9>        | 72 | 74 |    |
| MIOA_D10          | L4   | GPU MIOA D<10>       | 72 | 74 |    |
| MIOA_D11          | L5   | GPU MIOA D<11>       | 72 | 74 |    |
| MIOA_HSYNC        | R3   | TP GPU MIOA HSYNC    | 72 | 74 |    |
| MIOA_VSYNC        | R1   | TP GPU MIOA VSYNC    | 72 | 74 |    |
| MIOB_CLKIN        | AE4  | TP GPU MIOB_CLKIN    | 72 | 74 |    |
| MIOB_CLKOUT       | AD4  | TP GPU MIOB_CLKOUT_P | 72 | 74 |    |
| MIOB_CLKOUT_L     | AD5  | TP GPU MIOB_CLKOUT_N | 72 | 74 |    |
| MIOB_CTL3         | AD3  | TP GPU MIOB_CTL3     | 72 | 74 |    |
| MIOB_DE           | AD1  | TP GPU MIOB DE       | 72 | 74 |    |
| MIOB_D0           | AC3  | GPU MIOB D<0>        | 72 | 74 |    |
| MIOB_D1           | AC1  | GPU MIOB D<1>        | 72 | 74 |    |
| MIOB_D2           | AC2  | TP GPU MIOB D<2>     | 72 | 74 |    |
| MIOB_D3           | AB2  | TP GPU MIOB D<3>     | 72 | 74 |    |
| MIOB_D4           | AB1  | TP GPU MIOB D<4>     | 72 | 74 |    |
| MIOB_D5           | AA1  | TP GPU MIOB D<5>     | 72 | 74 |    |
| MIOB_D6           | AB3  | TP GPU MIOB D<6>     | 72 | 74 |    |
| MIOB_D7           | AA3  | TP GPU MIOB D<7>     | 72 | 74 |    |
| MIOB_D8           | AC5  | GPU MIOB D<8>        | 72 | 74 |    |
| MIOB_D9           | AB5  | GPU MIOB D<9>        | 72 | 74 |    |
| MIOB_D10          | AB4  | GPU MIOB D<10>       | 72 | 74 |    |
| MIOB_D11          | AA5  | GPU MIOB D<11>       | 72 | 74 |    |
| MIOB_HSYNC        | AF3  | GPU MIOB HSYNC       | 72 | 74 |    |
| MIOB_VSYNC        | AE3  | TP GPU MIOB VSYNC    | 72 | 74 |    |
| THERMDP           | K1   | GPU TDIODE P         | 51 | 72 | 87 |
| THERMDN           | J1   | GPU TDIODE N         | 51 | 72 | 87 |

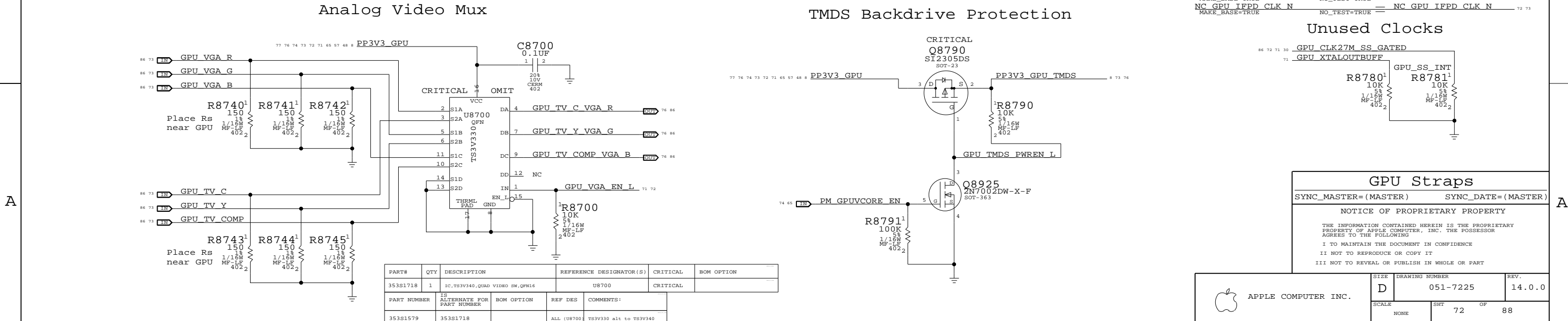
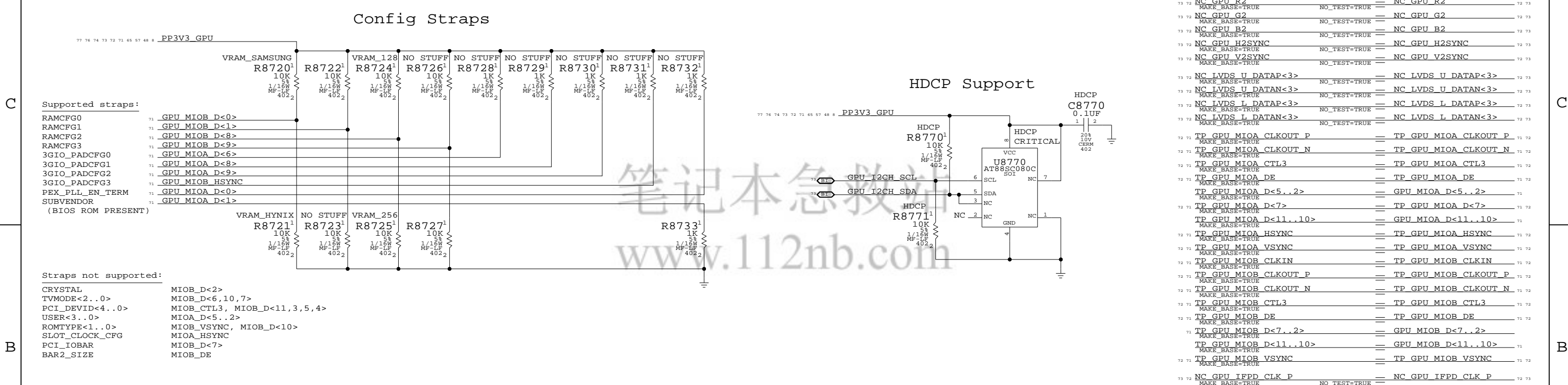
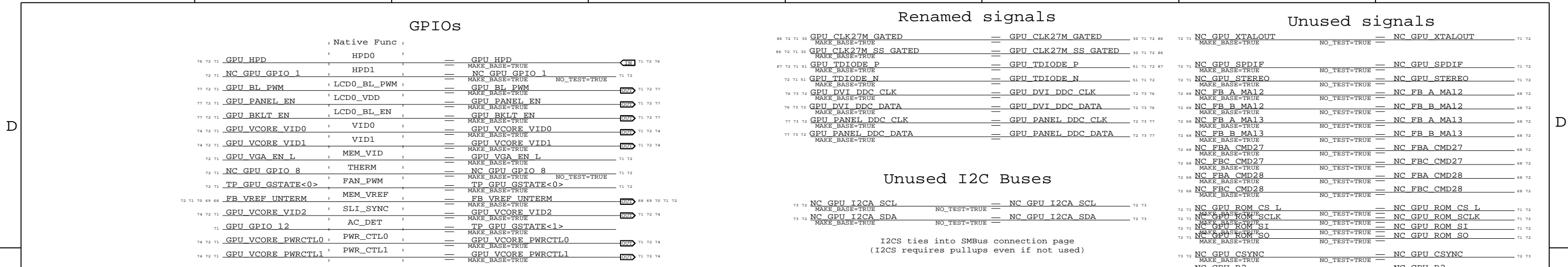
## NV G84M GPIO/MIO/Misc

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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| SCALE               | SHT  | OF             |        |
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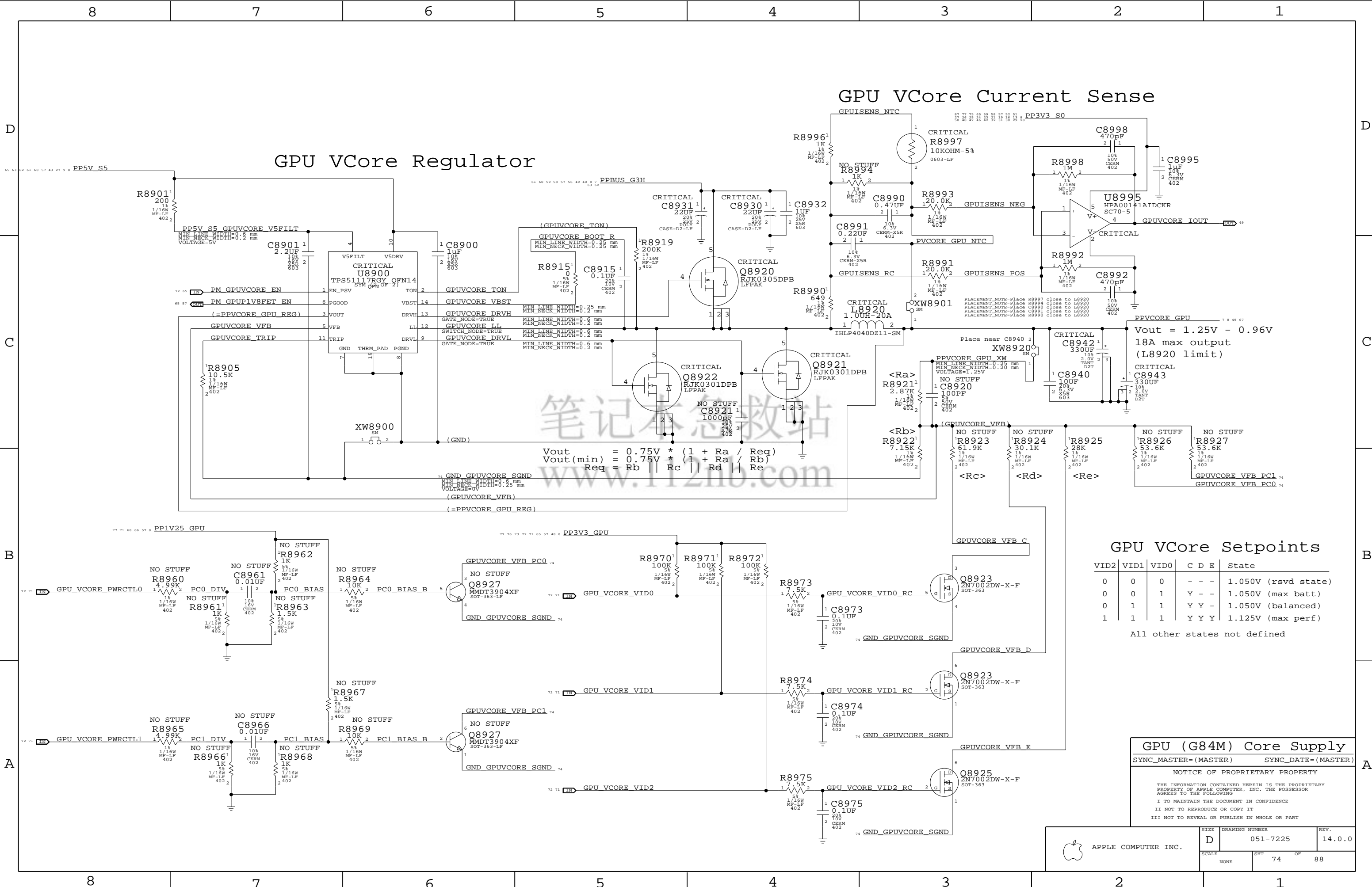






# GPU VCore Regulator

# GPU VCore Current Sense



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$$V_{out} = 0.75V * (1 + R_a / R_{eq})$$

$$V_{out}(\min) = 0.75V * (1 + R_a / R_b)$$

$$R_{eq} = R_b || R_c || R_d || R_e$$

## GPU VCore Setpoints

| VID2 | VID1 | VID0 | C | D | E | State               |
|------|------|------|---|---|---|---------------------|
| 0    | 0    | 0    | - | - | - | 1.050V (rsvd state) |
| 0    | 0    | 1    | Y | - | - | 1.050V (max batt)   |
| 0    | 1    | 1    | Y | Y | - | 1.050V (balanced)   |
| 1    | 1    | 1    | Y | Y | Y | 1.125V (max perf)   |

All other states not defined

## GPU (G84M) Core Supply

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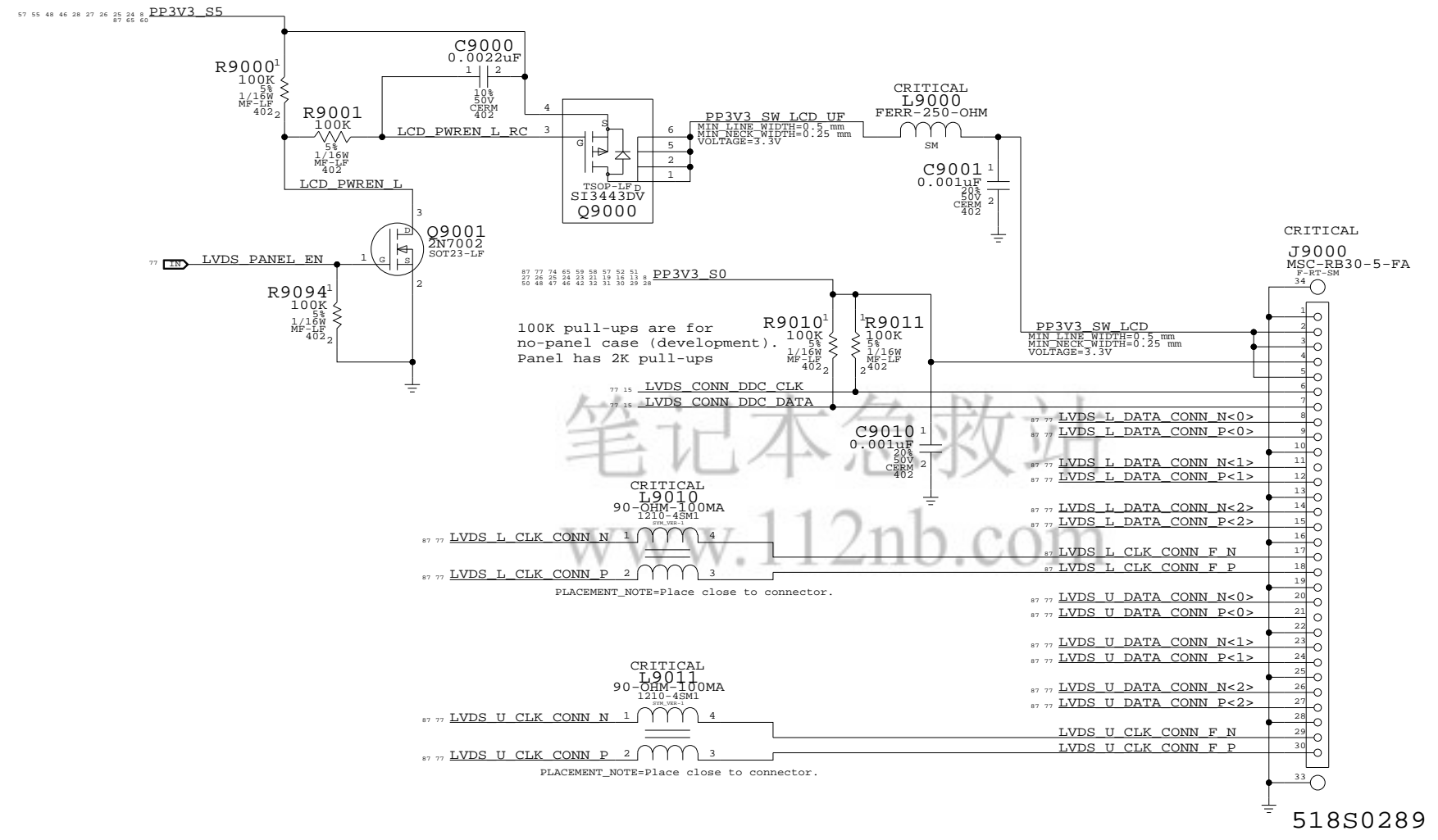
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| SCALE               | SHT  | OF             |        |
| NONE                | 74   | 88             |        |

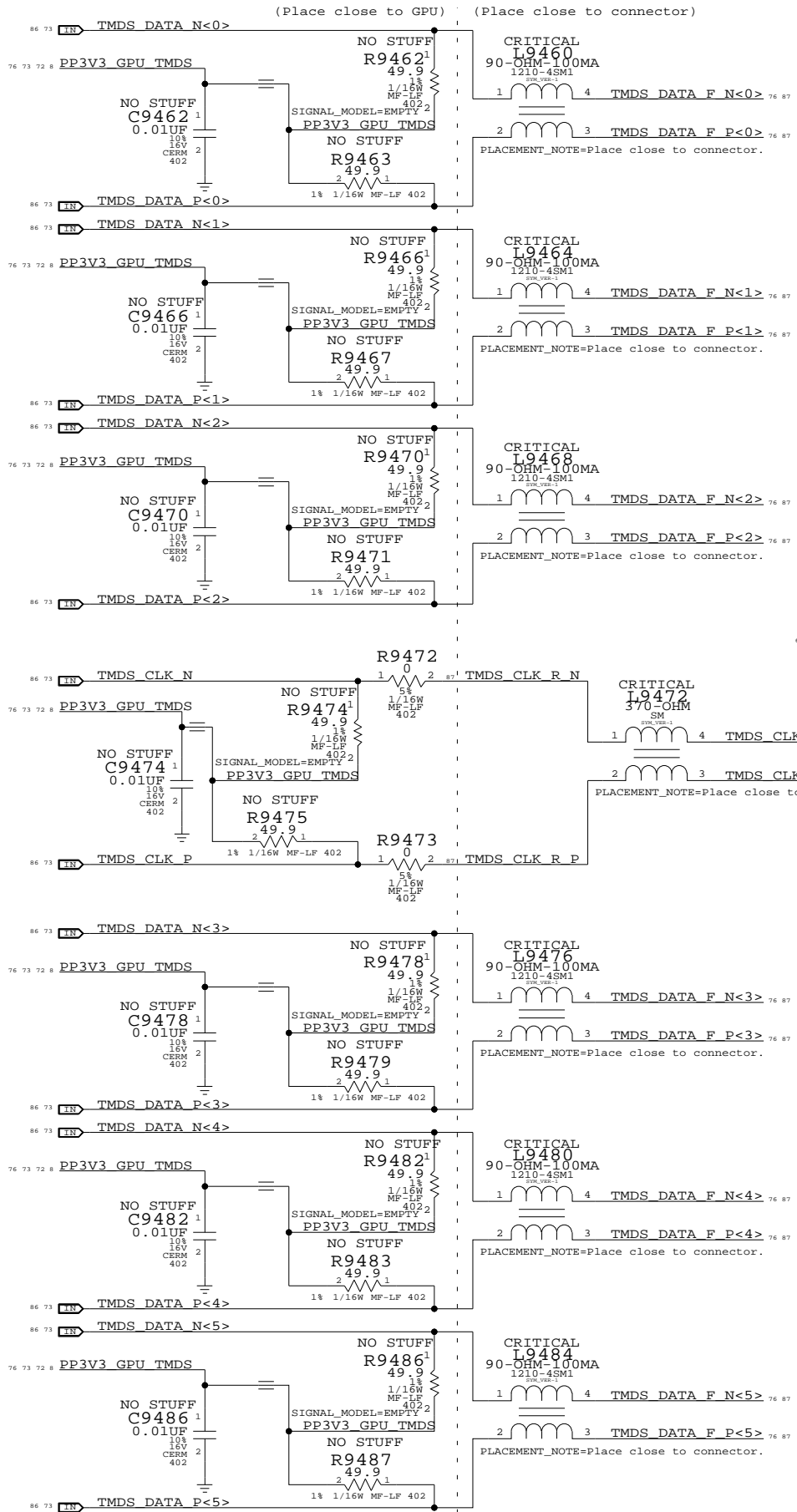
# LCD (LVDS) INTERFACE



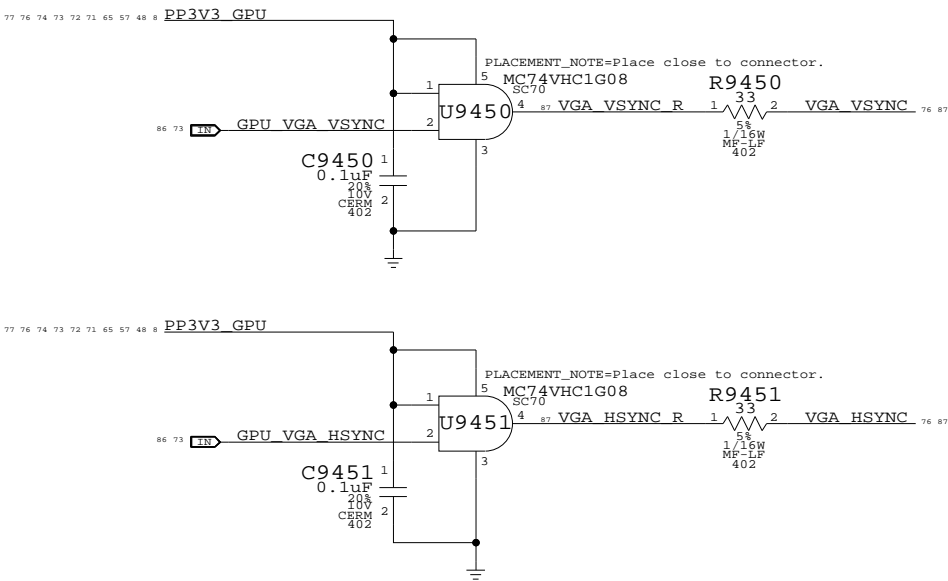
**LVDS Display Connector**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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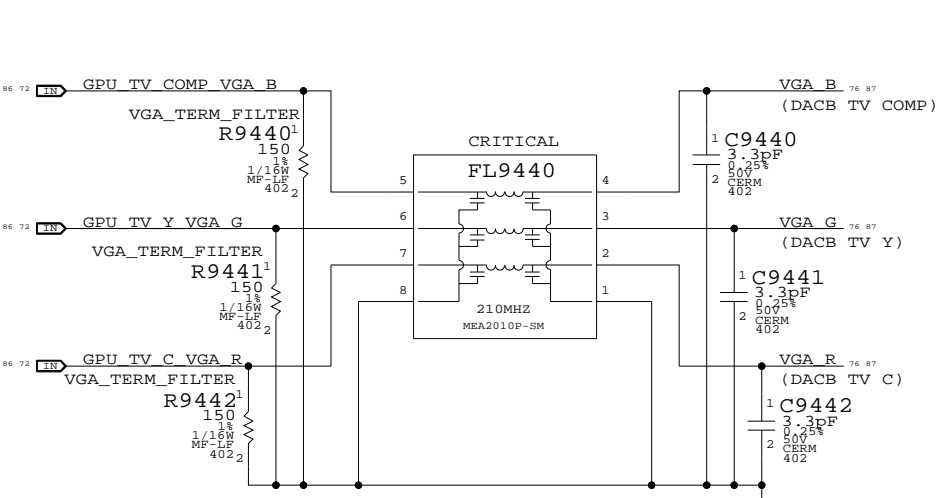
# TMDS Filtering



# VGA SYNC Buffers



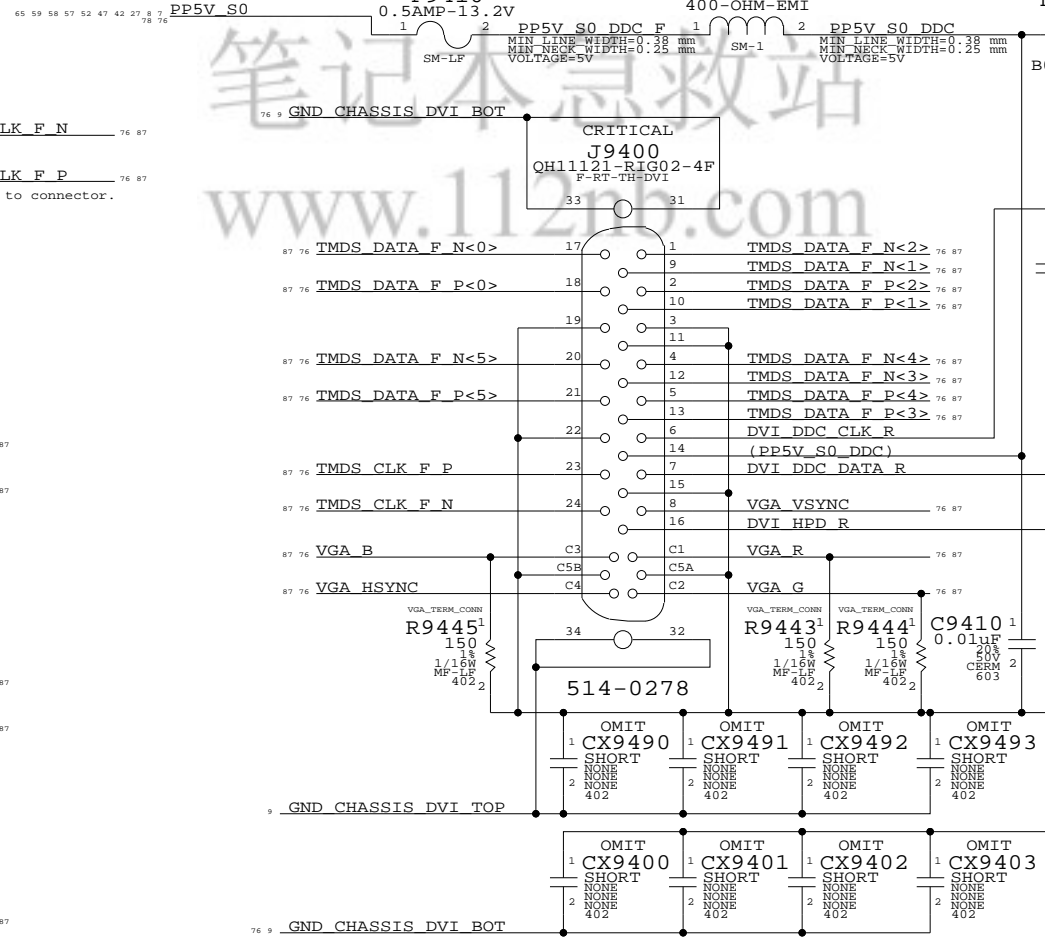
# ANALOG FILTERING



# DVI INTERFACE

## DVI DDC Current Limit

(55mA requirement per DVI spec)



## DVI Display Connector

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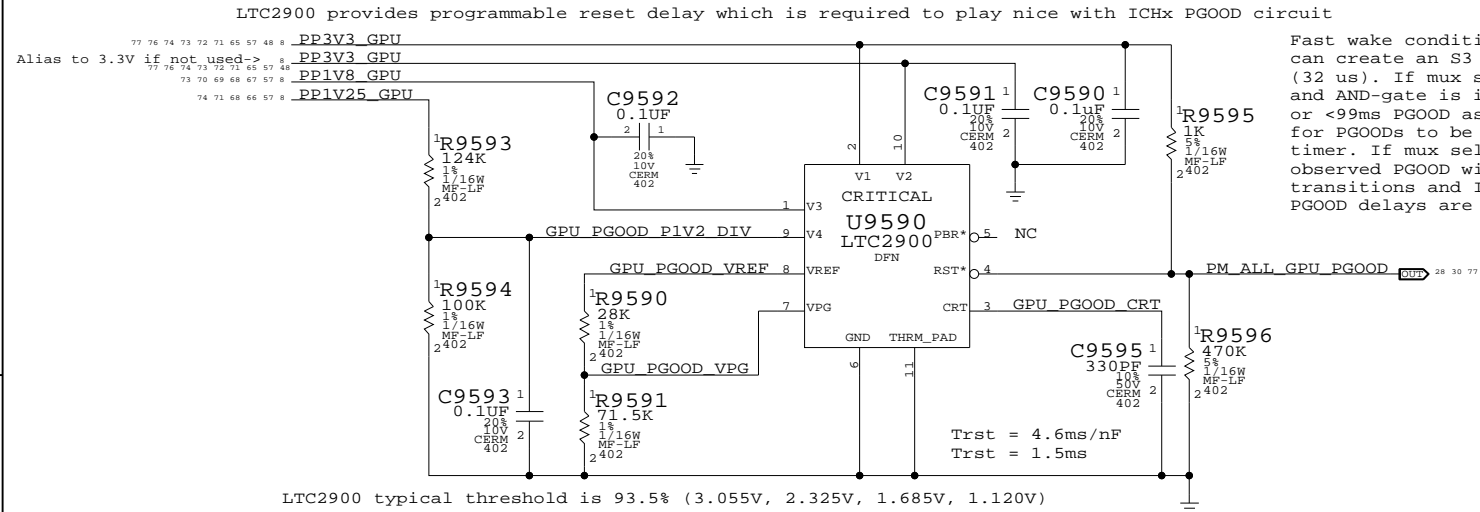
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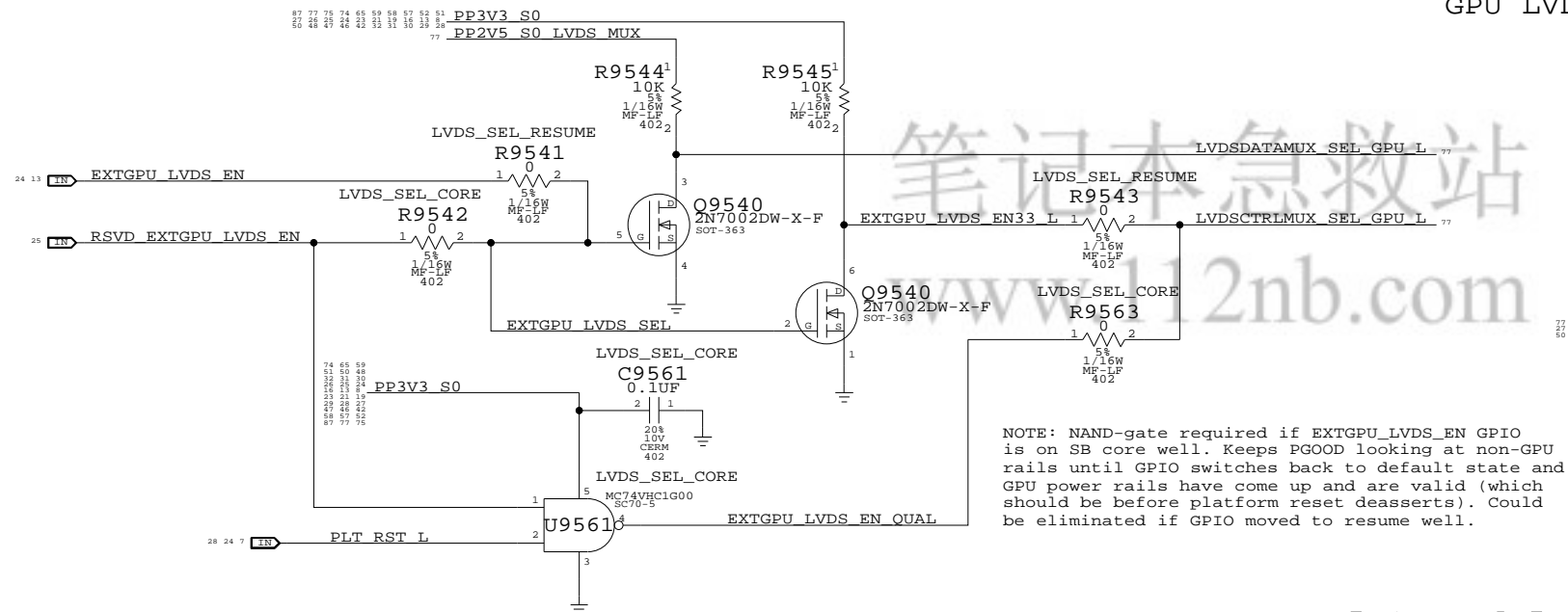
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|---------------------|------|----------------|--------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
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| SCALE               | SHT  | OF             |        |
| NONE                | 76   | 88             |        |

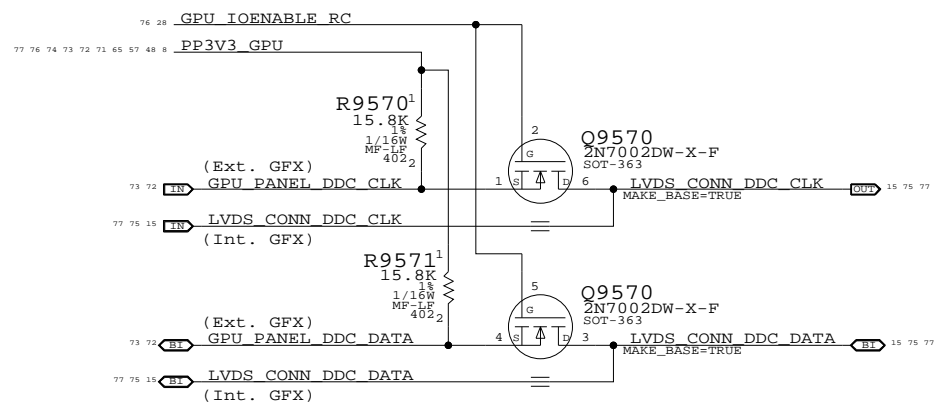
# PGOOD Monitor for GPU Rails



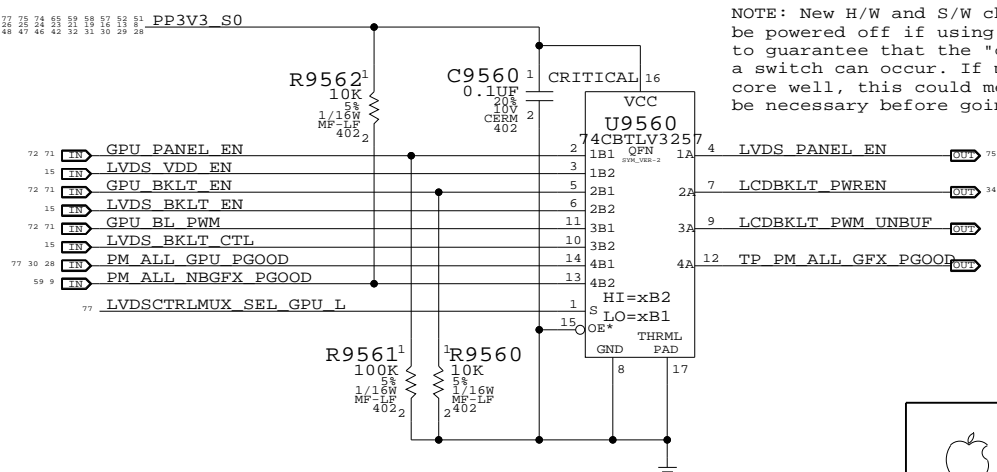
# Mux Select Conditioning



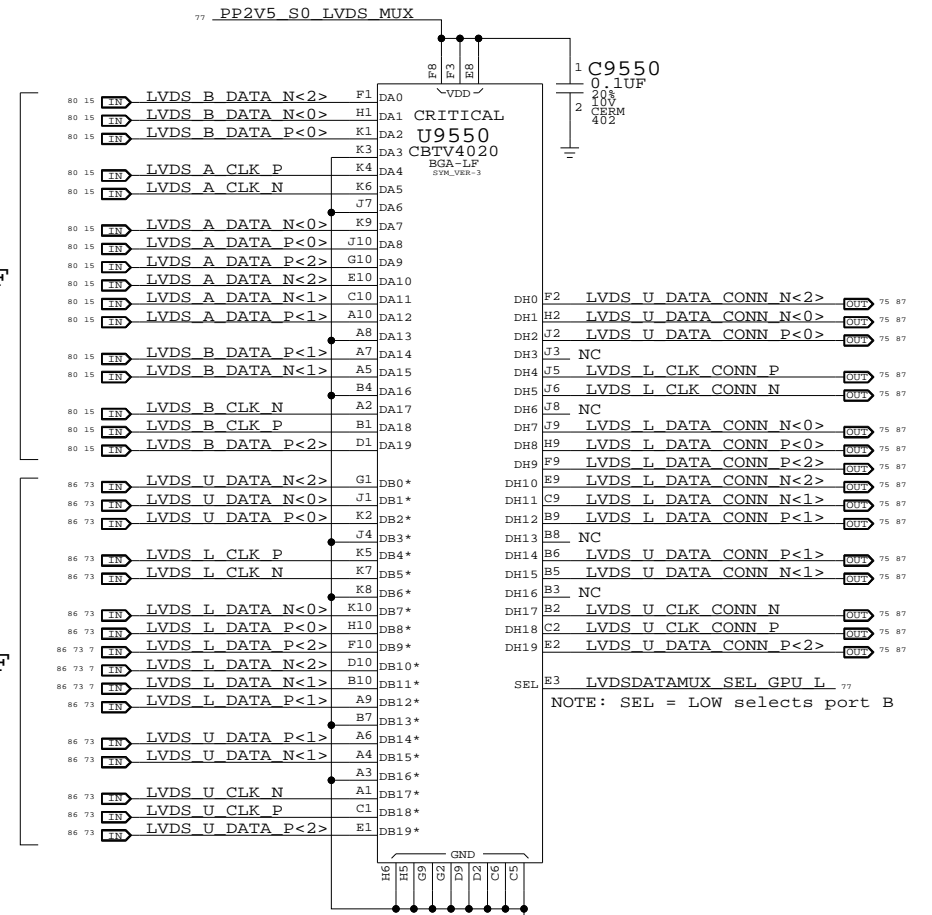
# GPU DDC Pass FETs



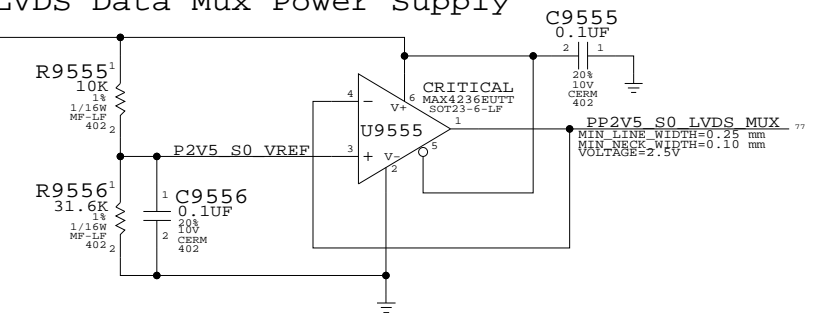
# Panel/Backlight Control Mux



# LVDS I/F Mux

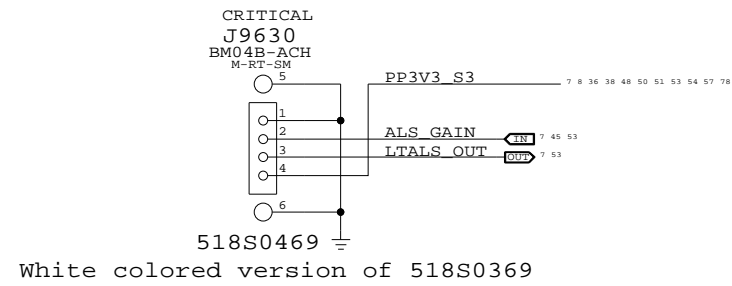


# LVDS Data Mux Power Supply

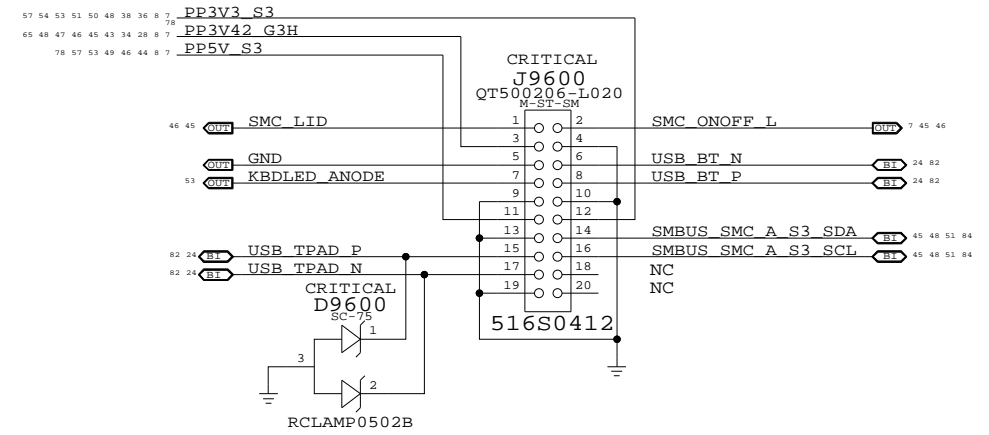


**LVDS Interface Mux**  
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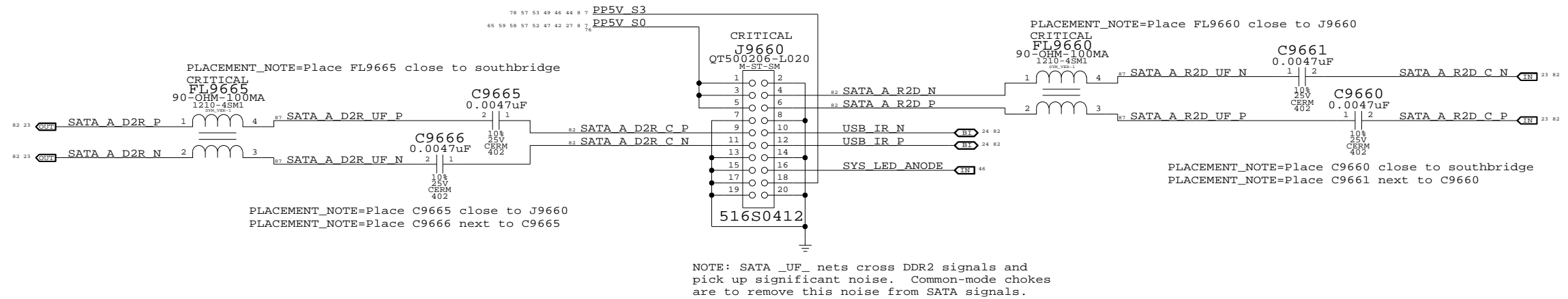
### Left ALS Connector



### Top-Case Connector



### SATA HDD & IR & SIL Flex Connector



### M75 Specific Connectors

SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=08/24/2006

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|                     | D    | 051-7225       | 14.0.0   |
| SCALE               | NONE | SHT            | 78 OF 88 |

### FSB (Front-Side Bus) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| FSB_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| FSB_DSTB_55S      | *     | =1:1_DIFFPAIR         | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =1:1_DIFFPAIR        | =1:1_DIFFPAIR     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FSB_ADDR         | *     | =3:1_SPACING         | ?      |
| FSB_ADDR2ADDR    | *     | =2:1_SPACING         | ?      |
| FSB_ADSTB        | *     | =3:1_SPACING         | ?      |
| FSB_ADDR2ADSTB   | *     | =3:1_SPACING         | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FSB_DATA         | *     | =3:1_SPACING         | ?      |
| FSB_DATA2DATA    | *     | =2:1_SPACING         | ?      |
| FSB_DSTB         | *     | =3:1_SPACING         | ?      |
| FSB_DATA2DSTB    | *     | =3:1_SPACING         | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FSB_COMMON       | *     | =2:1_SPACING         | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| FSB_ADDR          | FSB_ADDR          | *         | FSB_ADDR2ADDR    |
| FSB_ADDR          | FSB_ADSTB         | *         | FSB_ADDR2ADSTB   |
| FSB_DATA          | FSB_DATA          | *         | FSB_DATA2DATA    |
| FSB_DATA          | FSB_DSTB          | *         | FSB_DATA2DSTB    |

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

### CPU Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CPU_27P4S         | *     | Y                     | =27P4_OHM_SE       | =27P4_OHM_SE       | =27P4_OHM_SE        | 7 MIL                | 7 MIL             |
| CPU_55S           | *     | Y                     | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CPU_2T01         | *     | =2:1_SPACING         | ?      |
| CPU_COMP         | *     | 25 MIL               | ?      |
| CPU_GTLREF       | *     | 25 MIL               | ?      |
| CPU_ITP          | *     | =2:1_SPACING         | ?      |
| CPU_VCCSENSE     | *     | 25 MIL               | ?      |

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

### CPU / FSB Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE     |              |                 |               |
|---------------------------|--------------|--------------|-----------------|---------------|
|                           | PHYSICAL     | SPACING      |                 |               |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB ADS L       | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB BNR L       | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB BPRI L      | 10 14         |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB BRQ0 L      | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB DBSY L      | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB DEFER L     | 10 14         |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB DPWR L      | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB DRDY L      | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB HIT L       | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB HITM L      | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB LOCK L      | 7 10 14       |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB RS L<2..0>  | 10 14         |
| FSB_COMMON                | FSB_55S      | FSB_COMMON   | FSB TRDY L      | 10 14         |
| FSB_CPURST_L              | FSB_55S      | FSB_COMMON   | FSB CPURST L    | 7 10 13 14    |
| FSB_DATA_GROUP0           | FSB_55S      | FSB_DATA     | FSB D L<15..0>  | 7 10 14       |
| FSB_DATA_GROUP0           | FSB_55S      | FSB_DATA     | FSB DINV L<0>   | 7 10 14       |
| FSB_DSTB0                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L P<0> | 7 10 14       |
| FSB_DSTB0                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L N<0> | 7 10 14       |
| FSB_DATA_GROUP1           | FSB_55S      | FSB_DATA     | FSB D L<31..16> | 7 10 14       |
| FSB_DATA_GROUP1           | FSB_55S      | FSB_DATA     | FSB DINV L<1>   | 7 10 14       |
| FSB_DSTB1                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L P<1> | 7 10 14       |
| FSB_DSTB1                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L N<1> | 7 10 14       |
| FSB_DATA_GROUP2           | FSB_55S      | FSB_DATA     | FSB D L<47..32> | 7 10 14       |
| FSB_DATA_GROUP2           | FSB_55S      | FSB_DATA     | FSB DINV L<2>   | 7 10 14       |
| FSB_DSTB2                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L P<2> | 7 10 14       |
| FSB_DSTB2                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L N<2> | 7 10 14       |
| FSB_DATA_GROUP3           | FSB_55S      | FSB_DATA     | FSB D L<63..48> | 7 10 14       |
| FSB_DATA_GROUP3           | FSB_55S      | FSB_DATA     | FSB DINV L<3>   | 7 10 14       |
| FSB_DSTB3                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L P<3> | 7 10 14       |
| FSB_DSTB3                 | FSB_DSTB_55S | FSB_DSTB     | FSB DSTB L N<3> | 7 10 14       |
| FSB_ADDR_GROUP0           | FSB_55S      | FSB_ADDR     | FSB A L<16..3>  | 7 10 14       |
| FSB_ADDR_GROUP0           | FSB_55S      | FSB_ADDR     | FSB REQ L<4..0> | 7 10 14       |
| FSB_ADSTB0                | FSB_55S      | FSB_ADSTB    | FSB ADSTB L<0>  | 7 10 14       |
| FSB_ADDR_GROUP1           | FSB_55S      | FSB_ADDR     | FSB A L<35..17> | 7 10 14       |
| FSB_ADSTB1                | FSB_55S      | FSB_ADSTB    | FSB ADSTB L<1>  | 7 10 14       |
| CPU_IERR_L                | CPU_55S      |              | CPU IERR L      | 10            |
| CPU_FERR_L                | CPU_55S      |              | CPU FERR L      | 10 23         |
| CPU_PROCHOT_L             | CPU_55S      | CPU_2T01     | CPU PROCHOT L   | 10 46 58      |
| CPU_PWRGD                 | CPU_55S      |              | CPU PWRGD       | 7 10 13 23    |
| CPU_FROM_SB               | CPU_55S      |              | CPU INTR        | 10 23         |
| CPU_FROM_SB               | CPU_55S      |              | CPU NMI         | 10 23         |
| CPU_FROM_SB               | CPU_55S      |              | CPU A20M L      | 10 23         |
| CPU_FROM_SB               | CPU_55S      |              | CPU DPUSLP L    | 7 10 23       |
| CPU_FROM_SB               | CPU_55S      |              | CPU IGNE L      | 10 23         |
| CPU_INIT_L                | CPU_55S      |              | CPU INIT L      | 10 23 47      |
| CPU_FROM_SB               | CPU_55S      |              | CPU SMI L       | 10 23         |
| CPU_FROM_SB               | CPU_55S      |              | CPU STPCLK L    | 7 10 23       |
| PM_THRMTRIP_L             | CPU_55S      | CPU_2T01     | PM THRMTRIP L   | 10 16 23 46   |
| FSB_CPUSLP_L              | CPU_55S      |              | FSB CPUSLP L    | 7 10 14       |
| PM_DPRSLEVR               | CPU_55S      | CPU_2T01     | PM DPRSLPVR     | 7 16 25 58    |
| (See above)               | CPU_55S      | CPU_2T01     | IMVP DPRSLPVR   | 7 8           |
| CPU_BSEL0                 | CPU_55S      | CPU_2T01     | CPU BSEL<0>     | 10 30         |
| (See above)               | CPU_55S      | CPU_2T01     | NB BSEL<0>      | 13 16 30      |
| CPU_BSEL1                 | CPU_55S      | CPU_2T01     | CPU BSEL<1>     | 10 30         |
| (See above)               | CPU_55S      | CPU_2T01     | NB BSEL<1>      | 13 16 30      |
| CPU_BSEL2                 | CPU_55S      | CPU_2T01     | CPU BSEL<2>     | 10 30         |
| (See above)               | CPU_55S      | CPU_2T01     | NB BSEL<2>      | 13 16 30      |
| CPU_DPRSTP_L              | CPU_55S      | CPU_2T01     | CPU DPRSTP L    | 7 10 16 23 58 |
| CPU_GTLREF                | CPU_55S      | CPU_GTLREF   | CPU GTLREF      | 10            |
| CPU_COMP                  | CPU_55S      | CPU_COMP     | CPU COMP<3>     | 10            |
| CPU_COMP                  | CPU_27P4S    | CPU_COMP     | CPU COMP<2>     | 10            |
| CPU_COMP                  | CPU_55S      | CPU_COMP     | CPU COMP<1>     | 10            |
| CPU_COMP                  | CPU_27P4S    | CPU_COMP     | CPU COMP<0>     | 10            |
| XDP_TDI                   | CPU_55S      | CPU_ITP      | XDP TDI         | 10 13         |
| XDP_TDO                   | CPU_55S      | CPU_ITP      | XDP TDO         | 10 13         |
| XDP_TMS                   | CPU_55S      | CPU_ITP      | XDP TMS         | 10 13         |
| XDP_TCK                   | CPU_55S      | CPU_ITP      | XDP TCK         | 10 13         |
| XDP_TEST_L                | CPU_55S      | CPU_ITP      | XDP TRST L      | 10 13         |
| XDP_BPM_L                 | CPU_55S      | CPU_ITP      | XDP BPM L<4..0> | 10 13         |
| XDP_BPM_L5                | CPU_55S      | CPU_ITP      | XDP BPM L<5>    | 10 13         |
| CLK_FSB_1000              | CLK_FSB      | CLK_FSB      | XDP CLK P       | 13 29 30 84   |
| CLK_FSB_1000              | CLK_FSB      | CLK_FSB      | XDP CLK N       | 13 29 30 84   |
| (FSB_CPURST_L)            | CPU_55S      | CPU_ITP      | XDP CPURST L    | 13            |
| CPU_VID<6..0>             | CPU_55S      | CPU_2T01     | CPU VID<6..0>   | 11 12         |
| CPU_VCCSENSE              | CPU_27P4S    | CPU_VCCSENSE | CPU VCCSENSE P  | 7 12 58       |
| CPU_VCCSENSE              | CPU_27P4S    | CPU_VCCSENSE | CPU VCCSENSE N  | 11 58         |
| CPU_27P4S                 | CPU_VCCSENSE |              | IMVP6 VSEN P    | 58            |
| CPU_27P4S                 | CPU_VCCSENSE |              | IMVP6 VSEN N    | 58            |

### CPU/FSB Constraints

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|       | SHT 79 OF 88   |        |

PCI-Express / DMI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCIE_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| DMI_100D          | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCIE             | *     | 20 MIL               | ?      |
| DMI              | *     | 20 MIL               | ?      |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| LVDS_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| CRT_50S           | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =STANDARD            | =STANDARD         |
| CRT_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| LVDS             | *     | 20 MIL               | ?      |
| CRT              | *     | 25 MIL               | ?      |
| CRT_2CRT         | *     | 20 MIL               | ?      |
| CRT_SYNC         | *     | 25 MIL               | ?      |
| CRT_SYNC2SYNC    | *     | 20 MIL               | ?      |
| TVDAC            | *     | 25 MIL               | ?      |
| TVDAC_2TVDAC     | *     | 20 MIL               | ?      |

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CRT               | CRT               | *         | CRT_2CRT         |
| CRT_SYNC          | CRT_SYNC          | *         | CRT_SYNC2SYNC    |
| TVDAC             | TVDAC             | *         | TVDAC_2TVDAC     |

LVDS signals are 100-ohm +/- 20% differential impedance.  
 CRT & TVDAC signal single-ended impedance varies by location:  
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.  
 - 50-ohm +/- 15% from first to second termination resistor.  
 - 55-ohm +/- 15% from second termination resistor to connector.  
 CRT\_HSYNC/CRT\_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE  |          |                     |
|---------------------------|-----------|----------|---------------------|
|                           | PHYSICAL  | SPACING  |                     |
| PEG_R2D                   | PCIE_100D | PCIE     | PEG R2D P<15..0>    |
|                           | PCIE_100D | PCIE     | PEG R2D N<15..0>    |
|                           | PCIE_100D | PCIE     | PEG R2D C P<15..0>  |
|                           | PCIE_100D | PCIE     | PEG R2D C N<15..0>  |
| PEG_D2R                   | PCIE_100D | PCIE     | PEG D2R P<15..0>    |
|                           | PCIE_100D | PCIE     | PEG D2R N<15..0>    |
|                           | PCIE_100D | PCIE     | PEG D2R C P<15..0>  |
|                           | PCIE_100D | PCIE     | PEG D2R C N<15..0>  |
| DMI_N2S                   | DMI_100D  | DMI      | DMI N2S P<3..0>     |
|                           | DMI_100D  | DMI      | DMI N2S N<3..0>     |
| DMI_S2N                   | DMI_100D  | DMI      | DMI S2N P<3..0>     |
|                           | DMI_100D  | DMI      | DMI S2N N<3..0>     |
| LVDS_A_CLK                | LVDS_100D | LVDS     | LVDS A CLK P        |
| LVDS_A_CLK                | LVDS_100D | LVDS     | LVDS A CLK N        |
| LVDS_A_DATA               | LVDS_100D | LVDS     | LVDS A DATA P<2..0> |
| LVDS_A_DATA               | LVDS_100D | LVDS     | LVDS A DATA N<2..0> |
| LVDS_A_DATA3              | LVDS_100D | LVDS     | LVDS A DATA P<3>    |
| LVDS_A_DATA3              | LVDS_100D | LVDS     | LVDS A DATA N<3>    |
| LVDS_B_CLK                | LVDS_100D | LVDS     | LVDS B CLK P        |
| LVDS_B_CLK                | LVDS_100D | LVDS     | LVDS B CLK N        |
| LVDS_B_DATA               | LVDS_100D | LVDS     | LVDS B DATA P<2..0> |
| LVDS_B_DATA               | LVDS_100D | LVDS     | LVDS B DATA N<2..0> |
| LVDS_B_DATA3              | LVDS_100D | LVDS     | LVDS B DATA P<3>    |
| LVDS_B_DATA3              | LVDS_100D | LVDS     | LVDS B DATA N<3>    |
| LVDS_IBG                  |           | LVDS     | LVDS IBG            |
| CRT_TVO_IREF              |           | CRT      | CRT TVO IREF        |
| CRT_RED                   | CRT_50S   | CRT      | CRT RED             |
| CRT_GREEN                 | CRT_50S   | CRT      | CRT GREEN           |
| CRT_BLUE                  | CRT_50S   | CRT      | CRT BLUE            |
| CRT_SYNC                  | CRT_55S   | CRT_SYNC | CRT HSYNC R         |
| CRT_SYNC                  | CRT_55S   | CRT_SYNC | CRT VSYNC R         |
| TV_A_DAC                  | CRT_50S   | TVDAC    | TV A DAC            |
| TV_B_DAC                  | CRT_50S   | TVDAC    | TV B DAC            |
| TV_C_DAC                  | CRT_50S   | TVDAC    | TV C DAC            |

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NB Constraints

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### DDR2 Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_45S           | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |
| MEM_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| MEM_70D           | *     | =70_OHM_DIFF          | =70_OHM_DIFF       | =70_OHM_DIFF       | =70_OHM_DIFF        | =70_OHM_DIFF         | =70_OHM_DIFF      |
| MEM_85D           | *     | =85_OHM_DIFF          | =85_OHM_DIFF       | =85_OHM_DIFF       | =85_OHM_DIFF        | =85_OHM_DIFF         | =85_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MEM_CLK2MEM      | *     | =4:1_SPACING         | ?      |
| MEM_CTRL2CTRL    | *     | =2:1_SPACING         | ?      |
| MEM_CTRL2MEM     | *     | =3:1_SPACING         | ?      |
| MEM_CMD2CMD      | *     | =1.5:1_SPACING       | ?      |
| MEM_CMD2MEM      | *     | =3:1_SPACING         | ?      |
| MEM_DATA2DATA    | *     | =1.5:1_SPACING       | ?      |
| MEM_DATA2MEM     | *     | =3:1_SPACING         | ?      |
| MEM_DQS2MEM      | *     | =3:1_SPACING         | ?      |
| MEM_2OTHER       | *     | 25 MIL               | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK           | MEM_CLK           | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_CTRL          | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_CMD           | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_DATA          | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_DQS           | *         | MEM_CLK2MEM      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CMD           | MEM_CLK           | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_CTRL          | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_CMD           | *         | MEM_CMD2CMD      |
| MEM_CMD           | MEM_DATA          | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_DQS           | *         | MEM_CMD2MEM      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CTRL          | MEM_CLK           | *         | MEM_CTRL2MEM     |
| MEM_CTRL          | MEM_CTRL          | *         | MEM_CTRL2CTRL    |
| MEM_CTRL          | MEM_CMD           | *         | MEM_CTRL2MEM     |
| MEM_CTRL          | MEM_DATA          | *         | MEM_CTRL2MEM     |
| MEM_CTRL          | MEM_DQS           | *         | MEM_CTRL2MEM     |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DATA          | MEM_CLK           | *         | MEM_DATA2MEM     |
| MEM_DATA          | MEM_CTRL          | *         | MEM_DATA2MEM     |
| MEM_DATA          | MEM_CMD           | *         | MEM_DATA2MEM     |
| MEM_DATA          | MEM_DATA          | *         | MEM_DATA2DATA    |
| MEM_DATA          | MEM_DQS           | *         | MEM_DATA2MEM     |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK           | *                 | *         | MEM_2OTHER       |
| MEM_CTRL          | *                 | *         | MEM_2OTHER       |
| MEM_CMD           | *                 | *         | MEM_2OTHER       |
| MEM_DATA          | *                 | *         | MEM_2OTHER       |
| MEM_DQS           | *                 | *         | MEM_2OTHER       |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQS           | MEM_CLK           | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_CTRL          | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_CMD           | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_DATA          | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_DQS           | *         | MEM_DQS2MEM      |

Need to support MEM\_\*-style wildcards!  
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

### Memory Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | NET_TYPE | SPACING          |
|---------------------------|----------|----------|------------------|
| MEM_A_CLK                 | MEM_70D  | MEM_CLK  | MEM_CLK P<2..0>  |
| MEM_A_CLK                 | MEM_70D  | MEM_CLK  | MEM_CLK N<2..0>  |
| MEM_A_CNTRL               | MEM_45S  | MEM_CTRL | MEM_CKE<1..0>    |
| MEM_A_CNTRL               | MEM_45S  | MEM_CTRL | MEM_CS L<1..0>   |
| MEM_A_CNTRL               | MEM_45S  | MEM_CTRL | MEM_ODT<1..0>    |
| MEM_A_CMD                 | MEM_55S  | MEM_CMD  | MEM_A A<14..0>   |
| MEM_A_CMD                 | MEM_55S  | MEM_CMD  | MEM_A BS<2..0>   |
| MEM_A_CMD                 | MEM_55S  | MEM_CMD  | MEM_A RAS L      |
| MEM_A_CMD                 | MEM_55S  | MEM_CMD  | MEM_A CAS L      |
| MEM_A_CMD                 | MEM_55S  | MEM_CMD  | MEM_A WE L       |
| MEM_A_DQ_BYTE0            | MEM_55S  | MEM_DATA | MEM A DQ<7..0>   |
| MEM_A_DQ_BYTE1            | MEM_55S  | MEM_DATA | MEM A DQ<15..8>  |
| MEM_A_DQ_BYTE2            | MEM_55S  | MEM_DATA | MEM A DQ<23..16> |
| MEM_A_DQ_BYTE3            | MEM_55S  | MEM_DATA | MEM A DQ<31..24> |
| MEM_A_DQ_BYTE4            | MEM_55S  | MEM_DATA | MEM A DQ<39..32> |
| MEM_A_DQ_BYTE5            | MEM_55S  | MEM_DATA | MEM A DQ<47..40> |
| MEM_A_DQ_BYTE6            | MEM_55S  | MEM_DATA | MEM A DQ<55..48> |
| MEM_A_DQ_BYTE7            | MEM_55S  | MEM_DATA | MEM A DQ<63..56> |
| MEM_A_DM0                 | MEM_55S  | MEM_DATA | MEM A DM<0>      |
| MEM_A_DM1                 | MEM_55S  | MEM_DATA | MEM A DM<1>      |
| MEM_A_DM2                 | MEM_55S  | MEM_DATA | MEM A DM<2>      |
| MEM_A_DM3                 | MEM_55S  | MEM_DATA | MEM A DM<3>      |
| MEM_A_DM4                 | MEM_55S  | MEM_DATA | MEM A DM<4>      |
| MEM_A_DM5                 | MEM_55S  | MEM_DATA | MEM A DM<5>      |
| MEM_A_DM6                 | MEM_55S  | MEM_DATA | MEM A DM<6>      |
| MEM_A_DM7                 | MEM_55S  | MEM_DATA | MEM A DM<7>      |
| MEM_A_DQS0                | MEM_85D  | MEM_DQS  | MEM A DQS P<0>   |
| MEM_A_DQS0                | MEM_85D  | MEM_DQS  | MEM A DQS N<0>   |
| MEM_A_DQS1                | MEM_85D  | MEM_DQS  | MEM A DQS P<1>   |
| MEM_A_DQS1                | MEM_85D  | MEM_DQS  | MEM A DQS N<1>   |
| MEM_A_DQS2                | MEM_85D  | MEM_DQS  | MEM A DQS P<2>   |
| MEM_A_DQS2                | MEM_85D  | MEM_DQS  | MEM A DQS N<2>   |
| MEM_A_DQS3                | MEM_85D  | MEM_DQS  | MEM A DQS P<3>   |
| MEM_A_DQS3                | MEM_85D  | MEM_DQS  | MEM A DQS N<3>   |
| MEM_A_DQS4                | MEM_85D  | MEM_DQS  | MEM A DQS P<4>   |
| MEM_A_DQS4                | MEM_85D  | MEM_DQS  | MEM A DQS N<4>   |
| MEM_A_DQS5                | MEM_85D  | MEM_DQS  | MEM A DQS P<5>   |
| MEM_A_DQS5                | MEM_85D  | MEM_DQS  | MEM A DQS N<5>   |
| MEM_A_DQS6                | MEM_85D  | MEM_DQS  | MEM A DQS P<6>   |
| MEM_A_DQS6                | MEM_85D  | MEM_DQS  | MEM A DQS N<6>   |
| MEM_A_DQS7                | MEM_85D  | MEM_DQS  | MEM A DQS P<7>   |
| MEM_A_DQS7                | MEM_85D  | MEM_DQS  | MEM A DQS N<7>   |
| MEM_B_CLK                 | MEM_70D  | MEM_CLK  | MEM_CLK P<5..3>  |
| MEM_B_CLK                 | MEM_70D  | MEM_CLK  | MEM_CLK N<5..3>  |
| MEM_B_CNTRL               | MEM_45S  | MEM_CTRL | MEM_CKE<4..3>    |
| MEM_B_CNTRL               | MEM_45S  | MEM_CTRL | MEM_CS L<3..2>   |
| MEM_B_CNTRL               | MEM_45S  | MEM_CTRL | MEM_ODT<3..2>    |
| MEM_B_CMD                 | MEM_55S  | MEM_CMD  | MEM B A<14..0>   |
| MEM_B_CMD                 | MEM_55S  | MEM_CMD  | MEM B BS<2..0>   |
| MEM_B_CMD                 | MEM_55S  | MEM_CMD  | MEM B RAS L      |
| MEM_B_CMD                 | MEM_55S  | MEM_CMD  | MEM B CAS L      |
| MEM_B_CMD                 | MEM_55S  | MEM_CMD  | MEM B WE L       |
| MEM_B_DQ_BYTE0            | MEM_55S  | MEM_DATA | MEM B DQ<7..0>   |
| MEM_B_DQ_BYTE1            | MEM_55S  | MEM_DATA | MEM B DQ<15..8>  |
| MEM_B_DQ_BYTE2            | MEM_55S  | MEM_DATA | MEM B DQ<23..16> |
| MEM_B_DQ_BYTE3            | MEM_55S  | MEM_DATA | MEM B DQ<31..24> |
| MEM_B_DQ_BYTE4            | MEM_55S  | MEM_DATA | MEM B DQ<39..32> |
| MEM_B_DQ_BYTE5            | MEM_55S  | MEM_DATA | MEM B DQ<47..40> |
| MEM_B_DQ_BYTE6            | MEM_55S  | MEM_DATA | MEM B DQ<55..48> |
| MEM_B_DQ_BYTE7            | MEM_55S  | MEM_DATA | MEM B DQ<63..56> |
| MEM_B_DM0                 | MEM_55S  | MEM_DATA | MEM B DM<0>      |
| MEM_B_DM1                 | MEM_55S  | MEM_DATA | MEM B DM<1>      |
| MEM_B_DM2                 | MEM_55S  | MEM_DATA | MEM B DM<2>      |
| MEM_B_DM3                 | MEM_55S  | MEM_DATA | MEM B DM<3>      |
| MEM_B_DM4                 | MEM_55S  | MEM_DATA | MEM B DM<4>      |
| MEM_B_DM5                 | MEM_55S  | MEM_DATA | MEM B DM<5>      |
| MEM_B_DM6                 | MEM_55S  | MEM_DATA | MEM B DM<6>      |
| MEM_B_DM7                 | MEM_55S  | MEM_DATA | MEM B DM<7>      |
| MEM_B_DQS0                | MEM_85D  | MEM_DQS  | MEM B DQS P<0>   |
| MEM_B_DQS0                | MEM_85D  | MEM_DQS  | MEM B DQS N<0>   |
| MEM_B_DQS1                | MEM_85D  | MEM_DQS  | MEM B DQS P<1>   |
| MEM_B_DQS1                | MEM_85D  | MEM_DQS  | MEM B DQS N<1>   |
| MEM_B_DQS2                | MEM_85D  | MEM_DQS  | MEM B DQS P<2>   |
| MEM_B_DQS2                | MEM_85D  | MEM_DQS  | MEM B DQS N<2>   |
| MEM_B_DQS3                | MEM_85D  | MEM_DQS  | MEM B DQS P<3>   |
| MEM_B_DQS3                | MEM_85D  | MEM_DQS  | MEM B DQS N<3>   |
| MEM_B_DQS4                | MEM_85D  | MEM_DQS  | MEM B DQS P<4>   |
| MEM_B_DQS4                | MEM_85D  | MEM_DQS  | MEM B DQS N<4>   |
| MEM_B_DQS5                | MEM_85D  | MEM_DQS  | MEM B DQS P<5>   |
| MEM_B_DQS5                | MEM_85D  | MEM_DQS  | MEM B DQS N<5>   |
| MEM_B_DQS6                | MEM_85D  | MEM_DQS  | MEM B DQS P<6>   |
| MEM_B_DQS6                | MEM_85D  | MEM_DQS  | MEM B DQS N<6>   |
| MEM_B_DQS7                | MEM_85D  | MEM_DQS  | MEM B DQS P<7>   |
| MEM_B_DQS7                | MEM_85D  | MEM_DQS  | MEM B DQS N<7>   |

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 REV: 14.0.0  
 SCALE: NONE SHEET: 81 OF 88

### Disk Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| IDE_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| SATA_55S          | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| SATA_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| IDE              | *     | =1.8:1_SPACING       | ?      |
| SATA             | *     | 20 MIL               | ?      |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

### HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| HDA_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| HDA              | *     | =1.8:1_SPACING       | ?      |

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

### USB 2.0 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| USB_60S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| USB_90D           | *     | =90_OHM_DIFF          | =90_OHM_DIFF       | =90_OHM_DIFF       | =90_OHM_DIFF        | =90_OHM_DIFF         | =90_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| USB              | *     | 20 MIL               | ?      |
| USB_2CLK         | *     | 25 MIL               | ?      |

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

### Internal Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SMB_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| SPI_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SMB              | *     | =3:1_SPACING         | ?      |
| SPI              | *     | =1.8:1_SPACING       | ?      |

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE  |         |                  |                   |
|---------------------------|-----------|---------|------------------|-------------------|
|                           | PHYSICAL  | SPACING |                  |                   |
| IDE_PDD                   | IDE_55S   | IDE     | IDE_PDD<15..0>   | 23 42             |
| IDE_PDA                   | IDE_55S   | IDE     | IDE_PDA<2..0>    | 23 42             |
| IDE_PDCS                  | IDE_55S   | IDE     | IDE_PDCS1 L      | 23 42             |
| IDE_PDCCS                 | IDE_55S   | IDE     | IDE_PDCCS3 L     | 23 42             |
| IDE_CNVL                  | IDE_55S   | IDE     | IDE_PDIOW L      | 23 42             |
| IDE_PDIOR_L               | IDE_55S   | IDE     | IDE_PDIOR L      | 23 42             |
| IDE_CNVL                  | IDE_55S   | IDE     | IDE_PDDACK L     | 23 42             |
| IDE_CNVL                  | IDE_55S   | IDE     | IDE_PDDREO       | 23 42             |
| IDE_PDIORDY               | IDE_55S   | IDE     | IDE_PDIORDY      | 23 42             |
| IDE_IRQ14                 | IDE_55S   | IDE     | IDE_IRQ14        | 23 42             |
| IDE_RST_L                 | IDE_55S   | IDE     | ODD_RST_5VTOL L  | 24 42             |
| SATA_A_R2D                | SATA_100D | SATA    | SATA A R2D C P   | 23 78             |
| SATA_100D                 | SATA      | SATA    | SATA A R2D C N   | 23 78             |
| SATA_100D                 | SATA      | SATA    | SATA A R2D P     | 78                |
| SATA_100D                 | SATA      | SATA    | SATA A R2D N     | 78                |
| SATA_A_D2R                | SATA_100D | SATA    | SATA A D2R P     | 23 78             |
| SATA_100D                 | SATA      | SATA    | SATA A D2R N     | 23 78             |
| SATA_100D                 | SATA      | SATA    | SATA A D2R C P   | 78                |
| SATA_100D                 | SATA      | SATA    | SATA A D2R C N   | 78                |
| SATA_B_R2D                | SATA_100D | SATA    | TP SATA B R2DP   | 23 42             |
| SATA_100D                 | SATA      | SATA    | TP SATA B R2DN   | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA B R2D P     | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA B R2D N     | 23 42             |
| SATA_B_D2R                | SATA_100D | SATA    | TP SATA B D2RP   | 23 42             |
| SATA_100D                 | SATA      | SATA    | TP SATA B D2RN   | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA B D2R C P   | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA B D2R C N   | 23 42             |
| SATA_C_R2D                | SATA_100D | SATA    | TP SATA C R2DP   | 23 42             |
| SATA_100D                 | SATA      | SATA    | TP SATA C R2DN   | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA C R2D P     | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA C R2D N     | 23 42             |
| SATA_C_D2R                | SATA_100D | SATA    | TP SATA C D2RP   | 23 42             |
| SATA_100D                 | SATA      | SATA    | TP SATA C D2RN   | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA C D2R C P   | 23 42             |
| SATA_100D                 | SATA      | SATA    | SATA C D2R C N   | 23 42             |
| SATA_RBIAS                | SATA_55S  |         | SATA RBIAS       | 23 42             |
| HDA_BIT_CLK               | HDA_55S   | HDA     | HDA BIT CLK      | 23 34             |
| HDA_55S                   | HDA       | HDA     | HDA BIT CLK R    | 23                |
| HDA_SYNC                  | HDA_55S   | HDA     | HDA SYNC         | 23 34             |
| HDA_55S                   | HDA       | HDA     | HDA SYNC R       | 23                |
| HDA_RST_L                 | HDA_55S   | HDA     | HDA RST L        | 23 34             |
| HDA_55S                   | HDA       | HDA     | HDA RST L R      | 23                |
| HDA_SDIN0                 | HDA_55S   | HDA     | HDA SDIN0        | 23 34             |
| HDA_55S                   | HDA       | HDA     | HDA SDIN CODEC   | 23                |
| HDA_SDOUT                 | HDA_55S   | HDA     | HDA SDOUT        | 23 34             |
| HDA_55S                   | HDA       | HDA     | HDA SDOUT R      | 23                |
| USB_EXTA                  | USB_90D   | USB     | USB EXTA P       | 24 43             |
| USB_90D                   | USB       | USB     | USB EXTA N       | 24 43             |
| USB_90D                   | USB       | USB     | USB EXTA MUXED P | 24 43             |
| USB_90D                   | USB       | USB     | USB EXTA MUXED N | 24 43             |
| USB_MINI                  | USB_90D   | USB     | USB MINI P       | 24 34             |
| USB_90D                   | USB       | USB     | USB MINI N       | 24 34             |
| USB_EXTD                  | USB_90D   | USB     | USB WWAN P       | 7 24 44           |
| USB_90D                   | USB       | USB     | USB WWAN N       | 7 24 44           |
| USB_CAMERA                | USB_90D   | USB     | USB CAMERA P     | 7 24 44           |
| USB_90D                   | USB       | USB     | USB CAMERA N     | 7 24 44           |
| USB_BT                    | USB_90D   | USB     | USB BT P         | 24 78             |
| USB_90D                   | USB       | USB     | USB BT N         | 24 78             |
| USB_TPAD                  | USB_90D   | USB     | USB TPAD P       | 24 78             |
| USB_90D                   | USB       | USB     | USB TPAD N       | 24 78             |
| USB_IR                    | USB_90D   | USB     | USB IR P         | 24 78             |
| USB_90D                   | USB       | USB     | USB IR N         | 24 78             |
| USB_EXTB                  | USB_90D   | USB     | USB EXTB P       | 24 34             |
| USB_90D                   | USB       | USB     | USB EXTB N       | 24 34             |
| USB_EXCARD                | USB_90D   | USB     | USB EXCARD P     | 24 34             |
| USB_90D                   | USB       | USB     | USB EXCARD N     | 24 34             |
| USB_EXTC                  | USB_90D   | USB     | TP USB EXTCP     | 9 24              |
| USB_90D                   | USB       | USB     | TP USB EXTCN     | 9 24              |
| USB_RBIAS                 | USB_60S   |         | USB RBIAS        | 24                |
| SMB_SB_SCL                | SMB_55S   | SMB     | SMBUS SB SCL     | 25 29 31 32 34 48 |
| SMB_SB_SDA                | SMB_55S   | SMB     | SMBUS SB SDA     | 25 29 31 32 34 48 |
| SMB_SB_ME_SCL             | SMB_55S   | SMB     | SMBUS SB ME SCL  | 25 48             |
| SMB_SB_ME_SDA             | SMB_55S   | SMB     | SMBUS SB ME SDA  | 25 48             |
| SPI_SCLK                  | SPI_55S   | SPI     | SPI SCLK R       | 24 55             |
| SPI_55S                   | SPI       | SPI     | SPI SCLK         | 55                |
| SPI_55S                   | SPI       | SPI     | SPI A SCLK R     | 55                |
| SPI_55S                   | SPI       | SPI     | SPI B SCLK R     | 55                |
| SPI_SI                    | SPI_55S   | SPI     | SPI SI R         | 24 55             |
| SPI_55S                   | SPI       | SPI     | SPI SI           | 55                |
| SPI_55S                   | SPI       | SPI     | SPI A SI R       | 55                |
| SPI_55S                   | SPI       | SPI     | SPI B SI R       | 55                |
| SPI_SO                    | SPI_55S   | SPI     | SPI SO           | 24 55             |
| SPI_55S                   | SPI       | SPI     | SPI A SO R       | 55                |
| SPI_55S                   | SPI       | SPI     | SPI B SO         | 55                |
| SPI_55S                   | SPI       | SPI     | SPI B SO R       | 55                |
| SPI_CE_L0                 | SPI_55S   | SPI     | SPI CE R L<0>    | 24 55             |
| SPI_55S                   | SPI       | SPI     | SPI CE L<0>      | 55                |
| SPI_55S                   | SPI       | SPI     | SPI CE R L<1>    | 55                |
| SPI_55S                   | SPI       | SPI     | SPI CE L<1>      | 55                |

### SB Constraints (1 of 2)

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|                     | SHT   | OF             |        |
|                     | 82    | 88             |        |

### PCI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCI_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCI              | *     | =2:1_SPACING         | ?      |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

### Controller Link (AMT) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLINK_55S         | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| CLINK_12MIL       | *     | =STANDARD             | 12 MILS            | 5 MILS             | 300 MILS            | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLINK            | *     | =1.8:1_SPACING       | ?      |
| CLINK_VREF       | *     | 12 MILS              | ?      |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

### Ethernet (Yukon) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| ENET_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| ENET_MDI         | *     | 25 MILS              | ?      |

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE    |            |                     |            |
|---------------------------|-------------|------------|---------------------|------------|
|                           | PHYSICAL    | SPACING    |                     |            |
| PCI_AD                    | PCI_55S     | PCI        | PCI AD<18..0>       | 24 38      |
| PCI_AD19                  | PCI_55S     | PCI        | PCI AD<19>          | 24 38      |
| PCI_AD20                  | PCI_55S     | PCI        | PCI AD<20>          | 24 38      |
| PCI_AD                    | PCI_55S     | PCI        | PCI AD<31..21>      | 24 38      |
| PCI_AD                    | PCI_55S     | PCI        | PCI PAR             | 24 38      |
| PCI_C_BE_L                | PCI_55S     | PCI        | PCI C BE L<3..0>    | 24 38      |
| PCI_CNTRL                 | PCI_55S     | PCI        | PCI IRDY_L          | 24 38      |
| PCI_CNTRL                 | PCI_55S     | PCI        | PCI DEVSEL_L        | 24 38      |
| PCI_CNTRL                 | PCI_55S     | PCI        | PCI PERR_L          | 24 38      |
| PCI_LOCK_L                | PCI_55S     | PCI        | PCI LOCK_L          | 24         |
| PCI_CNTRL                 | PCI_55S     | PCI        | PCI SERR_L          | 24 38      |
| PCI_CNTRL                 | PCI_55S     | PCI        | PCI STOP_L          | 24 38      |
| PCI_CNTRL                 | PCI_55S     | PCI        | PCI TRDY_L          | 24 38      |
| PCI_CNTRL                 | PCI_55S     | PCI        | PCI FRAME_L         | 24 38      |
| PCI_FW_REQ_L              | PCI_55S     | PCI        | PCI FW REQ_L        | 24 38      |
| PCI_FW_GNT_L              | PCI_55S     | PCI        | PCI FW GNT_L        | 7 24 38 47 |
| PCI_REQ1_L                | PCI_55S     | PCI        | PCI REQ1_L          | 24         |
| PCI_GNT1_L                | PCI_55S     | PCI        | PCI GNT1_L          | 24         |
| PCI_REQ2_L                | PCI_55S     | PCI        | PCI REQ2_L          | 24         |
| PCI_GNT2_L                | PCI_55S     | PCI        | PCI GNT2_L          | 24         |
| INT_PIRQA_L               | PCI_55S     | PCI        | INT PIRQA_L         | 24         |
| INT_PIRQB_L               | PCI_55S     | PCI        | INT PIROB_L         | 24         |
| INT_PIRQC_L               | PCI_55S     | PCI        | INT PIROC_L         | 24         |
| INT_PIRQD_L               | PCI_55S     | PCI        | INT PIROD_L         | 24 38      |
| INT_PIRQE_L               | PCI_55S     | PCI        | INT PIROE_L         | 24         |
| INT_PIRQF_L               | PCI_55S     | PCI        | INT PIROF_L         | 24         |
| PCIE_A_R2D                | PCIE_100D   | PCIE       | PCIE A R2D C P      |            |
| PCIE_A_R2D                | PCIE_100D   | PCIE       | PCIE A R2D C N      |            |
| PCIE_A_D2R                | PCIE_100D   | PCIE       | PCIE A D2R P        |            |
| PCIE_A_D2R                | PCIE_100D   | PCIE       | PCIE A D2R N        |            |
| PCIE_B_R2D                | PCIE_100D   | PCIE       | PCIE B R2D C P      |            |
| PCIE_B_R2D                | PCIE_100D   | PCIE       | PCIE B R2D C N      |            |
| PCIE_B_D2R                | PCIE_100D   | PCIE       | PCIE B D2R P        |            |
| PCIE_B_D2R                | PCIE_100D   | PCIE       | PCIE B D2R N        |            |
| PCIE_EXCARD_R2D           | PCIE_100D   | PCIE       | PCIE EXCARD R2D C P | 24 34      |
| PCIE_EXCARD_R2D           | PCIE_100D   | PCIE       | PCIE EXCARD R2D C N | 24 34      |
| PCIE_EXCARD_D2R           | PCIE_100D   | PCIE       | PCIE EXCARD D2R P   | 24 34      |
| PCIE_EXCARD_D2R           | PCIE_100D   | PCIE       | PCIE EXCARD D2R N   | 24 34      |
| PCIE_FW_R2D               | PCIE_100D   | PCIE       | PCIE FW R2D C P     |            |
| PCIE_FW_R2D               | PCIE_100D   | PCIE       | PCIE FW R2D C N     |            |
| PCIE_FW_D2R               | PCIE_100D   | PCIE       | PCIE FW D2R P       |            |
| PCIE_FW_D2R               | PCIE_100D   | PCIE       | PCIE FW D2R N       |            |
| PCIE_MINI_R2D             | PCIE_100D   | PCIE       | PCIE MINI R2D C P   | 24 34      |
| PCIE_MINI_R2D             | PCIE_100D   | PCIE       | PCIE MINI R2D C N   | 24 34      |
| PCIE_MINI_D2R             | PCIE_100D   | PCIE       | PCIE MINI D2R P     | 24 34      |
| PCIE_MINI_D2R             | PCIE_100D   | PCIE       | PCIE MINI D2R N     | 24 34      |
| GLAN_COMP                 |             |            | GLAN COMP           | 23         |
| CLINK_NB                  | CLINK_55S   | CLINK      | CLINK NB CLK        | 16 25      |
| CLINK_NB                  | CLINK_55S   | CLINK      | CLINK NB DATA       | 16 25      |
| CLINK_NB_RESET_L          | CLINK_55S   | CLINK      | CLINK NB RESET_L    | 16 25      |
| CLINK_WLAN                | CLINK_55S   | CLINK      | CLINK WLAN CLK      |            |
| CLINK_WLAN                | CLINK_55S   | CLINK      | CLINK WLAN DATA     |            |
| CLINK_WLAN_RESET_L        | CLINK_55S   | CLINK      | CLINK WLAN RESET_L  |            |
| NB_CLINK_VREF             | CLINK_12MIL | CLINK_VREF | NB CLINK VREF       | 16         |
| SB_CLINK_VREF0            | CLINK_12MIL | CLINK_VREF | SB CLINK VREF0      | 25         |
| SB_CLINK_VREF1            | CLINK_12MIL | CLINK_VREF | SB CLINK VREF1      | 25         |
| PCIE_ENET_R2D             | PCIE_100D   | PCIE       | PCIE ENET R2D C P   | 24 35      |
| PCIE_ENET_R2D             | PCIE_100D   | PCIE       | PCIE ENET R2D C N   | 24 35      |
| PCIE_ENET_R2D             | PCIE_100D   | PCIE       | PCIE ENET R2D P     | 35         |
| PCIE_ENET_R2D             | PCIE_100D   | PCIE       | PCIE ENET R2D N     | 35         |
| PCIE_ENET_D2R             | PCIE_100D   | PCIE       | PCIE ENET D2R P     | 24 35      |
| PCIE_ENET_D2R             | PCIE_100D   | PCIE       | PCIE ENET D2R N     | 24 35      |
| PCIE_ENET_D2R             | PCIE_100D   | PCIE       | PCIE ENET D2R C P   | 35         |
| PCIE_ENET_D2R             | PCIE_100D   | PCIE       | PCIE ENET D2R C N   | 35         |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI P<0>       | 35 37      |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI N<0>       | 35 37      |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI P<1>       | 35 37      |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI N<1>       | 35 37      |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI P<2>       | 35 37      |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI N<2>       | 35 37      |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI P<3>       | 35 37      |
| ENET_MDI                  | ENET_100D   | ENET_MDI   | ENET MDI N<3>       | 35 37      |

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### SB Constraints (2 of 2)

SYNC\_MASTER=T9\_NAME SYNC\_DATE=01/17/2007

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| SIZE  | DRAWING NUMBER | REV.   |
|-------|----------------|--------|
| D     | 051-7225       | 14.0.0 |
| SCALE | SHT            | OF     |
| NONE  | 83             | 88     |

### Clock Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_FSB_100D      | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| CLK_PCIE_100D     | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| CLK_MED_55S       | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| CLK_SLOW_55S      | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_FSB          | *     | 25 MIL               | ?      |
| CLK_PCIE         | *     | 20 MIL               | ?      |
| CLK_MED          | *     | 20 MIL               | ?      |
| CLK_SLOW         | *     | 10 MIL               | ?      |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

### Clock Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE      |          |                                |                  |
|---------------------------|---------------|----------|--------------------------------|------------------|
|                           | PHYSICAL      | SPACING  |                                |                  |
| CK505_CPU                 | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_CPU_P                  | 10 29 30 84      |
| CK505_CPU                 | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_CPU_N                  | 10 29 30 84      |
| CK505_NB                  | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_NB_P                   | 7 14 29 30 84    |
| CK505_NB                  | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_NB_N                   | 7 14 29 30 84    |
| CK505_ITP                 | CLK_FSB_100D  | CLK_FSB  | XDP_CLK_P                      | 13 29 30 79 84   |
| CK505_ITP                 | CLK_FSB_100D  | CLK_FSB  | XDP_CLK_N                      | 13 29 30 79 84   |
| CK505_PCIE0               | CLK_MED_55S   | CLK_MED  | CK505_PCIE0_CLK_ITPEN          | 29 30            |
| CK505_PCIE1               | CLK_MED_55S   | CLK_MED  | CK505_PCIE1_CLK                | 29 30            |
| CK505_PCI1                | CLK_MED_55S   | CLK_MED  | CK505_PCI1_CLK                 | 29 30            |
| CK505_PCI2                | CLK_MED_55S   | CLK_MED  | TP CK505_PCI2_CLK              | 29 30            |
| CK505_PCI3                | CLK_MED_55S   | CLK_MED  | CK505_PCI3_CLK                 | 29 30            |
| CK505_PCI4                | CLK_MED_55S   | CLK_MED  | TP CK505_PCI4_CLK              | 29 30            |
| CK505_PCI5                | CLK_MED_55S   | CLK_MED  | CK505_PCI5_CLK_PCTSEL          | 29 30            |
| (CPU_BSEL0)               | CLK_MED_55S   | CLK_MED  | CK505_48M_FSA                  | 29 30            |
| (CPU_BSEL2)               | CLK_MED_55S   | CLK_MED  | CK505_REF0_FSC                 | 29 30            |
| CK505_DOT96               | CLK_PCIE_100D | CLK_PCIE | CK505_CLK27M                   | 29 30            |
|                           | CLK_PCIE_100D | CLK_PCIE | CK505_CLK27M_SS                | 29 30            |
| CK505_LVDS                | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_DPLLSS_P            | 7 16 22 29 30 84 |
|                           | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_DPLLSS_N            | 7 16 22 29 30 84 |
| CK505_SRC1                | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M_GPU_P              | 9 29 30 66 84    |
|                           | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M_GPU_N              | 9 29 30 66 84    |
| CK505_SRC2                | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_DMI_P               | 24 29 30 84      |
|                           | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_DMI_N               | 24 29 30 84      |
| CK505_SRC3                | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_P          | 29 30 34 84      |
|                           | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_N          | 29 30 34 84      |
| CK505_SRC4                | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_SATA_P              | 23 29 30 84      |
|                           | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_SATA_N              | 23 29 30 84      |
| CK505_SRC5                | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_PCIE_P              | 7 16 29 30 84    |
|                           | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_PCIE_N              | 7 16 29 30 84    |
| CK505_SRC6                | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_P            | 29 30 34 84      |
|                           | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_N            | 29 30 34 84      |
| CK505_SRC7                | CLK_PCIE_100D | CLK_PCIE | TP_PCIE_CLK100M_SRC7P          | 29 30            |
|                           | CLK_PCIE_100D | CLK_PCIE | TP_PCIE_CLK100M_SRC7N          | 29 30            |
| CK505_SRC8                | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_ENET_P            | 29 30 35 84      |
|                           | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_ENET_N            | 29 30 35 84      |
| (CK505_CPU)               | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_CPU_P                  | 10 29 30 84      |
| (CK505_CPU)               | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_CPU_N                  | 10 29 30 84      |
| (CK505_NB)                | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_NB_P                   | 7 14 29 30 84    |
| (CK505_NB)                | CLK_FSB_100D  | CLK_FSB  | FSB_CLK_NB_N                   | 7 14 29 30 84    |
| (CK505_ITP)               | CLK_FSB_100D  | CLK_FSB  | XDP_CLK_P                      | 13 29 30 79 84   |
| (CK505_ITP)               | CLK_FSB_100D  | CLK_FSB  | XDP_CLK_N                      | 13 29 30 79 84   |
| (CK505_PCIE0)             | CLK_MED_55S   | CLK_MED  | PCI_CLK33M_LPCPLUS             | 7 30 47          |
| (CK505_PCIE1)             | CLK_MED_55S   | CLK_MED  | PCI_CLK33M_SB                  | 24 30            |
| (CK505_PCI1)              | CLK_MED_55S   | CLK_MED  | PCI_CLK33M_FW                  | 30 38            |
| (CK505_PCI2)              | CLK_MED_55S   | CLK_MED  | PCI_CLK33M_TPM                 | 30 45            |
| (CK505_PCI3)              | CLK_MED_55S   | CLK_MED  | PCI_CLK33M_SMC                 | 30 45            |
| (CPU_BSEL0)               | CLK_MED_55S   | CLK_MED  | SB_CLK48M_USBCTRL              | 25 30            |
| (CPU_BSEL2)               | CLK_MED_55S   | CLK_MED  | SB_CLK14P3M_TIMER              | 25 30            |
| (CPU_BSEL0)               | CLK_MED_55S   | CLK_MED  | CK505_FSA                      | 30               |
| (CPU_BSEL2)               | CLK_MED_55S   | CLK_MED  | CK505_FSC                      | 30               |
| (CK505_DOT96)             | CLK_PCIE_100D | CLK_PCIE | NB_CLK96M_DOT_P                | 7                |
| (CK505_DOT96)             | CLK_PCIE_100D | CLK_PCIE | NB_CLK96M_DOT_N                | 7                |
| CK505_LVDS                | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_DPLLSS_P            | 7 16 22 29 30 84 |
| CK505_LVDS                | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_DPLLSS_N            | 7 16 22 29 30 84 |
| CK505_SRC1                | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M_GPU_P              | 9 29 30 66 84    |
| CK505_SRC1                | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M_GPU_N              | 9 29 30 66 84    |
| CK505_SRC2                | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_DMI_P               | 24 29 30 84      |
| CK505_SRC2                | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_DMI_N               | 24 29 30 84      |
| CK505_SRC3                | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_P          | 29 30 34 84      |
| CK505_SRC3                | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_EXCARD_N          | 29 30 34 84      |
| CK505_SRC4                | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_SATA_P              | 23 29 30 84      |
| CK505_SRC4                | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_SATA_N              | 23 29 30 84      |
| CK505_SRC5                | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_PCIE_P              | 7 16 29 30 84    |
| CK505_SRC5                | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_PCIE_N              | 7 16 29 30 84    |
| CK505_SRC6                | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_P            | 29 30 34 84      |
| CK505_SRC6                | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_MINI_N            | 29 30 34 84      |
| (CK505_SRC7)              | CLK_PCIE_100D | CLK_PCIE | CK505_SRC7 is project-specific |                  |
| (CK505_SRC8)              | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_ENET_P            | 29 30 35 84      |
| (CK505_SRC8)              | CLK_PCIE_100D | CLK_PCIE | PCIE_CLK100M_ENET_N            | 29 30 35 84      |

### SMC SMBus Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE |         |                    |             |
|---------------------------|----------|---------|--------------------|-------------|
|                           | PHYSICAL | SPACING |                    |             |
| SMBUS_SMC_A_S3_SCL        | SMB_55S  | SMB     | SMBUS_SMC_A_S3_SCL | 45 48 51 78 |
| SMBUS_SMC_A_S3_SDA        | SMB_55S  | SMB     | SMBUS_SMC_A_S3_SDA | 45 48 51 78 |
| SMBUS_SMC_B_S0_SCL        | SMB_55S  | SMB     | SMBUS_SMC_B_S0_SCL | 34 45       |
| SMBUS_SMC_B_S0_SDA        | SMB_55S  | SMB     | SMBUS_SMC_B_S0_SDA | 34 45       |
| SMBUS_SMC_0_S0_SCL        | SMB_55S  | SMB     | SMBUS_SMC_0_S0_SCL | 45 48 51 73 |
| SMBUS_SMC_0_S0_SDA        | SMB_55S  | SMB     | SMBUS_SMC_0_S0_SDA | 45 48 51 73 |
| SMBUS_SMC_BSA_SCL         | SMB_55S  | SMB     | SMBUS_SMC_BSA_SCL  | 7 45 48 56  |
| SMBUS_SMC_BSA_SDA         | SMB_55S  | SMB     | SMBUS_SMC_BSA_SDA  | 7 45 48 56  |
| SMBUS_SMC_MGMT_SCL        | SMB_55S  | SMB     | SMBUS_SMC_MGMT_SCL | 45 48 54    |
| SMBUS_SMC_MGMT_SDA        | SMB_55S  | SMB     | SMBUS_SMC_MGMT_SDA | 45 48 54    |

### Clock & SMC Constraints

SYNC\_MASTER=T9\_NAME SYNC\_DATE=01/17/2007

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|       |                |        |
|-------|----------------|--------|
| SIZE  | DRAWING NUMBER | REV.   |
| D     | 051-7225       | 14.0.0 |
| SCALE | SHT            | OF     |
| NONE  | 84             | 88     |

### FireWire Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| FW_55S            | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| FW_110D           | *     | =110_OHM_DIFF         | =110_OHM_DIFF      | =110_OHM_DIFF      | =110_OHM_DIFF       | =110_OHM_DIFF        | =110_OHM_DIFF     |


| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FW               | *     | =2:1_SPACING         | ?      |
| FW_TP            | *     | =3:1_SPACING         | ?      |

### FireWire Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE    |         | SPACING |                       |
|---------------------------|-------------|---------|---------|-----------------------|
|                           | PHYSICAL    |         |         |                       |
| EW_D_CTL                  | EW_55S      | FW      |         | FW LINK<7..0>         |
| EW_D_CTL                  | EW_55S      | FW      |         | FW CTL<1..0>          |
| EW_LCLK                   | CLK_MED_55S | CLK_MED |         | CLKFW LINK LCLK       |
| EW_LCLK                   | CLK_MED_55S | CLK_MED |         | CLKFW PHY LCLK 38 39  |
| EW_PCLK                   | CLK_MED_55S | CLK_MED |         | CLKFW LINK PCLK 38 39 |
| EW_PCLK                   | CLK_MED_55S | CLK_MED |         | CLKFW PHY PCLK 38 39  |
| EW_LKON                   | EW_55S      | FW      |         | FW LKON               |
| EW_LKON                   | EW_55S      | FW      |         | FW LKON R             |
| EW_LPS                    | EW_55S      | FW      |         | FW LPS 38 39          |
| EW_LREQ                   | EW_55S      | FW      |         | FW LREQ 38 39         |
| EW_PINT                   | EW_55S      | FW      |         | FW PINT 38 39         |
| EWPHY_CLK98P304M_XI       | CLK_MED_55S | CLK_MED |         | CLK98P304M FW XI R    |
| EWPHY_CLK98P304M_XI       | CLK_MED_55S | CLK_MED |         | CLK98P304M FW XI      |
| EW_0_TPA                  | EW_110D     | EW_TP   |         | FW PORT0 TPA P 39 41  |
| EW_0_TPA                  | EW_110D     | EW_TP   |         | FW PORT0 TPA N 39 41  |
| EW_0_TPB                  | EW_110D     | EW_TP   |         | FW PORT0 TPB P 39 41  |
| EW_0_TPB                  | EW_110D     | EW_TP   |         | FW PORT0 TPB N 39 41  |
| EW_1_TPA                  | EW_110D     | EW_TP   |         | FW PORT1 TPA P 39 41  |
| EW_1_TPA                  | EW_110D     | EW_TP   |         | FW PORT1 TPA N 39 41  |
| EW_1_TPB                  | EW_110D     | EW_TP   |         | FW PORT1 TPB P 39 41  |
| EW_1_TPB                  | EW_110D     | EW_TP   |         | FW PORT1 TPB N 39 41  |
| Port 2 Not Used           |             |         |         |                       |

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|  |  |                      |
|--|--|----------------------|
| <b>FireWire Constraints</b>  |  |                      |
| SYNC_MASTER=T9_NOME  |  | SYNC_DATE=01/17/2007 |
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|  APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.   |
|   | D    | 051-7225       | 14.0.0 |
| SCALE   | SHT  | OF             |        |
| NONE  | 85   | 88             |        |

### GDDR3 Frame Buffer Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| GDDR3_40R50SE     | *     | =50_OHM_SE            | =40_OHM_SE         | =50_OHM_SE         | 12.7 MM             | =STANDARD            | =STANDARD         |
| GDDR3_50SE        | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =STANDARD            | =STANDARD         |
| GDDR3_80D         | *     | =80_OHM_DIFF          | =80_OHM_DIFF       | =80_OHM_DIFF       | =80_OHM_DIFF        | =80_OHM_DIFF         | =80_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GDDR3_CLK        | *     | =2.5:1_SPACING       | ?      |
| GDDR3_CMD        | *     | =2.5:1_SPACING       | ?      |
| GDDR3_DATA       | *     | =2.5:1_SPACING       | ?      |
| GDDR3_DQS        | *     | =2.5:1_SPACING       | ?      |

### Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| TMDS_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| VGA_50S           | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =STANDARD            | =STANDARD         |
| VGA_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| TMDS             | *     | 20 MIL               | ?      |
| VGA              | *     | 20 MIL               | ?      |
| VGA_SYNC         | *     | 20 MIL               | ?      |

### GDDR3 FB A/B Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE      |            |                 |       |
|---------------------------|---------------|------------|-----------------|-------|
|                           | PHYSICAL      | SPACING    |                 |       |
| FB_A_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB A CLK P<0>   | 68 69 |
| FB_A_CLK_N                | GDDR3_80D     | GDDR3_CLK  | FB A CLK N<0>   | 68 69 |
| FB_B_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB A CLK P<1>   | 68 69 |
| FB_B_CLK_N                | GDDR3_80D     | GDDR3_CLK  | FB A CLK N<1>   | 68 69 |
| FB_AB_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB A MA<1..0>   | 68 69 |
| FB_AB_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB A MA<11..6>  | 68 69 |
| FB_AB_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB A BA<2..0>   | 68 69 |
| FB_AB_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB A RAS L      | 68 69 |
| FB_AB_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB A CAS L      | 68 69 |
| FB_AB_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB A WE L       | 68 69 |
| FB_AB_CMD_PD              | GDDR3_40R50SE | GDDR3_CMD  | FB A CKE        | 68 69 |
| FB_AB_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB A CS0 L      | 68 69 |
| FB_AB_CMD_PD              | GDDR3_40R50SE | GDDR3_CMD  | FB A DRAM RST   | 68 69 |
| FB_A_CMD                  | GDDR3_50SE    | GDDR3_CMD  | FB A LMA<5..2>  | 68 69 |
| FB_B_CMD                  | GDDR3_50SE    | GDDR3_CMD  | FB A UMA<5..2>  | 68 69 |
| FB_A_WDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<0>    | 68 69 |
| FB_A_WDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<1>    | 68 69 |
| FB_A_WDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<2>    | 68 69 |
| FB_A_WDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<3>    | 68 69 |
| FB_A_RDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<0>    | 68 69 |
| FB_A_RDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<1>    | 68 69 |
| FB_A_RDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<2>    | 68 69 |
| FB_A_RDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<3>    | 68 69 |
| FB_A_DQ_BYTE0             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<7..0>   | 68 69 |
| FB_A_DQ_BYTE1             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<15..8>  | 68 69 |
| FB_A_DQ_BYTE2             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<23..16> | 68 69 |
| FB_A_DQ_BYTE3             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<31..24> | 68 69 |
| FB_A_DQM0                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<0>   | 68 69 |
| FB_A_DQM1                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<1>   | 68 69 |
| FB_A_DQM2                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<2>   | 68 69 |
| FB_A_DQM3                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<3>   | 68 69 |
| FB_B_WDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<4>    | 68 69 |
| FB_B_WDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<5>    | 68 69 |
| FB_B_WDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<6>    | 68 69 |
| FB_B_WDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB A WDQS<7>    | 68 69 |
| FB_B_RDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<4>    | 68 69 |
| FB_B_RDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<5>    | 68 69 |
| FB_B_RDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<6>    | 68 69 |
| FB_B_RDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB A RDQS<7>    | 68 69 |
| FB_B_DQ_BYTE0             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<39..32> | 68 69 |
| FB_B_DQ_BYTE1             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<47..40> | 68 69 |
| FB_B_DQ_BYTE2             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<55..48> | 68 69 |
| FB_B_DQ_BYTE3             | GDDR3_50SE    | GDDR3_DATA | FB A DQ<63..56> | 68 69 |
| FB_B_DQM0                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<4>   | 68 69 |
| FB_B_DQM1                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<5>   | 68 69 |
| FB_B_DQM2                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<6>   | 68 69 |
| FB_B_DQM3                 | GDDR3_50SE    | GDDR3_DATA | FB A DQM L<7>   | 68 69 |

### GDDR3 FB C/D Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE      |            |                 |       |
|---------------------------|---------------|------------|-----------------|-------|
|                           | PHYSICAL      | SPACING    |                 |       |
| FB_C_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB B CLK P<0>   | 68 70 |
| FB_C_CLK_N                | GDDR3_80D     | GDDR3_CLK  | FB B CLK N<0>   | 68 70 |
| FB_D_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB B CLK P<1>   | 68 70 |
| FB_D_CLK_N                | GDDR3_80D     | GDDR3_CLK  | FB B CLK N<1>   | 68 70 |
| FB_CD_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB B MA<1..0>   | 68 70 |
| FB_CD_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB B MA<11..6>  | 68 70 |
| FB_CD_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB B BA<2..0>   | 68 70 |
| FB_CD_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB B RAS L      | 68 70 |
| FB_CD_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB B CAS L      | 68 70 |
| FB_CD_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB B WE L       | 68 70 |
| FB_CD_CMD_PD              | GDDR3_40R50SE | GDDR3_CMD  | FB B CKE        | 68 70 |
| FB_CD_CMD                 | GDDR3_40R50SE | GDDR3_CMD  | FB B CS0 L      | 68 70 |
| FB_CD_CMD_PD              | GDDR3_40R50SE | GDDR3_CMD  | FB B DRAM RST   | 68 70 |
| FB_C_CMD                  | GDDR3_50SE    | GDDR3_CMD  | FB B LMA<5..2>  | 68 70 |
| FB_D_CMD                  | GDDR3_50SE    | GDDR3_CMD  | FB B UMA<5..2>  | 68 70 |
| FB_C_WDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<0>    | 68 70 |
| FB_C_WDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<1>    | 68 70 |
| FB_C_WDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<2>    | 68 70 |
| FB_C_WDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<3>    | 68 70 |
| FB_C_RDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<0>    | 68 70 |
| FB_C_RDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<1>    | 68 70 |
| FB_C_RDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<2>    | 68 70 |
| FB_C_RDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<3>    | 68 70 |
| FB_C_DQ_BYTE0             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<7..0>   | 68 70 |
| FB_C_DQ_BYTE1             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<15..8>  | 68 70 |
| FB_C_DQ_BYTE2             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<23..16> | 68 70 |
| FB_C_DQ_BYTE3             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<31..24> | 68 70 |
| FB_C_DQM0                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<0>   | 68 70 |
| FB_C_DQM1                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<1>   | 68 70 |
| FB_C_DQM2                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<2>   | 68 70 |
| FB_C_DQM3                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<3>   | 68 70 |
| FB_D_WDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<4>    | 68 70 |
| FB_D_WDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<5>    | 68 70 |
| FB_D_WDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<6>    | 68 70 |
| FB_D_WDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB B WDQS<7>    | 68 70 |
| FB_D_RDQS0                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<4>    | 68 70 |
| FB_D_RDQS1                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<5>    | 68 70 |
| FB_D_RDQS2                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<6>    | 68 70 |
| FB_D_RDQS3                | GDDR3_50SE    | GDDR3_DQS  | FB B RDQS<7>    | 68 70 |
| FB_D_DQ_BYTE0             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<39..32> | 68 70 |
| FB_D_DQ_BYTE1             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<47..40> | 68 70 |
| FB_D_DQ_BYTE2             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<55..48> | 68 70 |
| FB_D_DQ_BYTE3             | GDDR3_50SE    | GDDR3_DATA | FB B DQ<63..56> | 68 70 |
| FB_D_DQM0                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<4>   | 68 70 |
| FB_D_DQM1                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<5>   | 68 70 |
| FB_D_DQM2                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<6>   | 68 70 |
| FB_D_DQM3                 | GDDR3_50SE    | GDDR3_DATA | FB B DQM L<7>   | 68 70 |

### G84M Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE     |          |                     |          |
|---------------------------|--------------|----------|---------------------|----------|
|                           | PHYSICAL     | SPACING  |                     |          |
| (CK505_DOT96)             | CLK_SLOW_55S | CLK_SLOW | GPU_CLK27M          | 30       |
|                           | CLK_SLOW_55S | CLK_SLOW | GPU_CLK27M_GATED    | 30 71 72 |
| CK505_CLK27MSS            | CLK_SLOW_55S | CLK_SLOW | GPU_CLK27M_SS       | 30       |
|                           | CLK_SLOW_55S | CLK_SLOW | GPU_CLK27M_SS_GATED | 30 71 72 |
|                           | LVDS_100D    | LVDS     | LVDS L CLK P        | 73 77    |
|                           | LVDS_100D    | LVDS     | LVDS L CLK N        | 73 77    |
|                           | LVDS_100D    | LVDS     | LVDS L DATA P<3..0> | 73 77    |
|                           | LVDS_100D    | LVDS     | LVDS L DATA N<3..0> | 73 77    |
|                           | LVDS_100D    | LVDS     | LVDS U CLK P        | 73 77    |
|                           | LVDS_100D    | LVDS     | LVDS U CLK N        | 73 77    |
|                           | LVDS_100D    | LVDS     | LVDS U DATA P<3..0> | 73 77    |
|                           | LVDS_100D    | LVDS     | LVDS U DATA N<3..0> | 73 77    |
| TMDS_CLK                  | TMDS_100D    | TMDS     | TMDS CLK P          | 73 76    |
| TMDS_CLK                  | TMDS_100D    | TMDS     | TMDS CLK N          | 73 76    |
| TMDS_DATA                 | TMDS_100D    | TMDS     | TMDS DATA P<5..0>   | 73 76    |
| TMDS_DATA                 | TMDS_100D    | TMDS     | TMDS DATA N<5..0>   | 73 76    |
| VGA_B_TV_C                | VGA_50S      | VGA      | GPU_TV_C_VGA_R      | 72 76    |
| VGA_G_TV_Y                | VGA_50S      | VGA      | GPU_TV_Y_VGA_G      | 72 76    |
| VGA_B_TV_COMP             | VGA_50S      | VGA      | GPU_TV_COMP_VGA_B   | 72 76    |
|                           | VGA_50S      | VGA      | GPU_VGA_R           | 72 73    |
|                           | VGA_50S      | VGA      | GPU_VGA_G           | 72 73    |
|                           | VGA_50S      | VGA      | GPU_VGA_B           | 72 73    |
|                           | VGA_50S      | VGA      | GPU_TV_C            | 72 73    |
|                           | VGA_50S      | VGA      | GPU_TV_Y            | 72 73    |
|                           | VGA_50S      | VGA      | GPU_TV_COMP         | 72 73    |
| VGA_SYNC                  | VGA_55S      | VGA_SYNC | GPU_VGA_HSYNC       | 73 76    |
| VGA_SYNC                  | VGA_55S      | VGA_SYNC | GPU_VGA_VSYNC       | 73 76    |

### GPU (G84M) Constraints

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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|                     | D    | 051-7225       | 14.0.0 |
| SCALE               | SHT  | OF             |        |
| NONE                | 86   | 88             |        |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SENSE_1T01_55S    | *     | =1:1_DIFFPAIR         | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =1:1_DIFFPAIR        | =1:1_DIFFPAIR     |
| THERM_1T01_55S    | *     | =1:1_DIFFPAIR         | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =1:1_DIFFPAIR        | =1:1_DIFFPAIR     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SENSE            | *     | =2:1_SPACING         | ?      |
| THERM            | *     | =2:1_SPACING         | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| ENETCONN         | *     | 25 MILS              | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND              | *     | =STANDARD            | ?      |
| PP1V8_MEM        | *     | =STANDARD            | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND_P2MM         | *     | 0.20 MM              | 1000   |
| PWR_P2MM         | *     | 0.20 MM              | 1000   |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK           | GND               | *         | GND_P2MM         |
| MEM_CMD           | GND               | *         | GND_P2MM         |
| MEM_CTRL          | GND               | *         | GND_P2MM         |
| MEM_DATA          | GND               | *         | GND_P2MM         |
| MEM_DQS           | GND               | *         | GND_P2MM         |
| MEM_CLK           | PP1V8_MEM         | *         | PWR_P2MM         |
| MEM_CMD           | PP1V8_MEM         | *         | PWR_P2MM         |
| MEM_CTRL          | PP1V8_MEM         | *         | PWR_P2MM         |
| MEM_DATA          | PP1V8_MEM         | *         | PWR_P2MM         |
| MEM_DQS           | PP1V8_MEM         | *         | PWR_P2MM         |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CLK_VREF          | GND               | *         | GND_P2MM         |
| CLK_MED           | GND               | *         | GND_P2MM         |
| CLK_PCIE          | GND               | *         | GND_P2MM         |
| DMI               | GND               | *         | GND_P2MM         |
| PCIE              | GND               | *         | GND_P2MM         |
| SATA              | GND               | *         | GND_P2MM         |
| USB               | GND               | *         | GND_P2MM         |
| CLK_PCIE          | SB_POWER          | *         | PWR_P2MM         |
| DMI               | SB_POWER          | *         | PWR_P2MM         |
| SATA              | SB_POWER          | *         | PWR_P2MM         |
| USB               | SB_POWER          | *         | PWR_P2MM         |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| LVDS              | GND               | *         | GND_P2MM         |

## Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

| PHYSICAL_RULE_SET | LAYER  | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|--------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_70D           | BOTTOM |                       |                    | 0.127 MM           | 6.35 MM             |                      |                   |

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_45S           | OVERRIDE    | OVERRIDE              | OVERRIDE           | 0.100 MM           | 2.54 MM             | OVERRIDE             | OVERRIDE          |
| MEM_70D           | ISL10       |                       |                    | 0.100 MM           | 2.54 MM             |                      |                   |
| MEM_85D           | ISL4, ISL10 |                       |                    | 0.100 MM           | 2.54 MM             |                      |                   |

## Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| LVDS_100D         | BGA       | 100_DIFF_BGA      |
| TMDS_100D         | BGA       | 100_DIFF_BGA      |

## SIM Card Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| WWAN_SIM          | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =50_OHM_SE           | =50_OHM_SE        |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| WWAN_SIM         | *     | =2:1_SPACING         | ?      |

## M75 Specific Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE       |          |                          |
|---------------------------|----------------|----------|--------------------------|
|                           | PHYSICAL       | SPACING  |                          |
| (PCIE_EXCARD)             | PCIE_100D      | PCIE     | PCIE_EXCARD_R2D_P        |
| (PCIE_EXCARD)             | PCIE_100D      | PCIE     | PCIE_EXCARD_R2D_N        |
| (PCIE_MINI)               | PCIE_100D      | PCIE     | PCIE_MINI_R2D_P          |
| (PCIE_MINI)               | PCIE_100D      | PCIE     | PCIE_MINI_R2D_N          |
|                           | ENET_100D      | ENET_MDI | ENET_MDI_R_P<3..0>       |
|                           | ENET_100D      | ENET_MDI | ENET_MDI_R_N<3..0>       |
|                           | ENET_100D      | ENETCONN | ENETCONN_P<3..0>         |
|                           | ENET_100D      | ENETCONN | ENETCONN_N<3..0>         |
|                           | FW_110D        | FW_TP    | FW_PORT0_TPA_FL_P        |
|                           | FW_110D        | FW_TP    | FW_PORT0_TPA_FL_N        |
|                           | FW_110D        | FW_TP    | FW_PORT0_TPB_FL_P        |
|                           | FW_110D        | FW_TP    | FW_PORT0_TPB_FL_N        |
| (SATA_A_R2D)              | SATA_100D      | SATA     | SATA_A_R2D_UF_P          |
| (SATA_A_R2D)              | SATA_100D      | SATA     | SATA_A_R2D_UF_N          |
| (SATA_A_D2R)              | SATA_100D      | SATA     | SATA_A_D2R_UF_P          |
| (SATA_A_D2R)              | SATA_100D      | SATA     | SATA_A_D2R_UF_N          |
| (USB_EXT_A)               | USB_90D        | USB      | USB2_EXT_A_MUXED_P       |
| (USB_EXT_A)               | USB_90D        | USB      | USB2_EXT_A_MUXED_N       |
| (USB_EXT_A)               | USB_90D        | USB      | USB2_RT_P                |
| (USB_EXT_A)               | USB_90D        | USB      | USB2_RT_N                |
| (USB_EXT_D)               | USB_90D        | USB      | USB_WWAN_F_P             |
| (USB_EXT_D)               | USB_90D        | USB      | USB_WWAN_F_N             |
| (USB_CAMERA)              | USB_90D        | USB      | USB_CAMERA_F_P           |
| (USB_CAMERA)              | USB_90D        | USB      | USB_CAMERA_F_N           |
| SENSE_DIFFPAIR            | SENSE_1T01_55S | SENSE    | GFXIMVP6_VSEN_P          |
| SENSE_DIFFPAIR            | SENSE_1T01_55S | SENSE    | NBCOREISNS_P             |
| SENSE_DIFFPAIR            | SENSE_1T01_55S | SENSE    | P1V8ISNS_P               |
| SENSE_DIFFPAIR            | SENSE_1T01_55S | SENSE    | P1V25ISNS_P              |
| THERM_DIFFPAIR            | THERM_1T01_55S | THERM    | CPU_THERMSNS_D2_P        |
| THERM_DIFFPAIR            | THERM_1T01_55S | THERM    | CPU_THERMD_P             |
| THERM_DIFFPAIR            | THERM_1T01_55S | THERM    | GPU_THERMSNS_D_P         |
| THERM_DIFFPAIR            | THERM_1T01_55S | THERM    | GPU_TDIODE_P             |
| THERM_DIFFPAIR            | THERM_1T01_55S | THERM    | HSTHERMSNS_D_P           |
| THERM_DIFFPAIR            | THERM_1T01_55S | THERM    | REMTHERMSNS_DX_P         |
| THERM_DIFFPAIR            | THERM_1T01_55S | THERM    | RSFSTHERMSNS_D_P         |
|                           | LVDS_100D      | LVDS     | LVDS_L_CLK_CONN_F_P      |
|                           | LVDS_100D      | LVDS     | LVDS_L_CLK_CONN_F_N      |
|                           | LVDS_100D      | LVDS     | LVDS_L_CLK_CONN_P        |
|                           | LVDS_100D      | LVDS     | LVDS_L_CLK_CONN_N        |
|                           | LVDS_100D      | LVDS     | LVDS_L_DATA_CONN_P<3..0> |
|                           | LVDS_100D      | LVDS     | LVDS_L_DATA_CONN_N<3..0> |
|                           | LVDS_100D      | LVDS     | LVDS_U_CLK_CONN_P        |
|                           | LVDS_100D      | LVDS     | LVDS_U_CLK_CONN_N        |
|                           | LVDS_100D      | LVDS     | LVDS_U_DATA_CONN_P<3..0> |
|                           | LVDS_100D      | LVDS     | LVDS_U_DATA_CONN_N<3..0> |
|                           | TMDS_100D      | TMDS     | TMDS_CLK_R_P             |
|                           | TMDS_100D      | TMDS     | TMDS_CLK_R_N             |
|                           | TMDS_100D      | TMDS     | TMDS_CLK_F_P             |
|                           | TMDS_100D      | TMDS     | TMDS_CLK_F_N             |
|                           | TMDS_100D      | TMDS     | TMDS_DATA_F_P<5..0>      |
|                           | TMDS_100D      | TMDS     | TMDS_DATA_F_N<5..0>      |
| (VGA_R_TV_Y)              | VGA_50S        | VGA      | VGA_R                    |
| (VGA_G_TV_C)              | VGA_50S        | VGA      | VGA_G                    |
| (VGA_B_TV_COMP)           | VGA_50S        | VGA      | VGA_B                    |
| (VGA_SYNC)                | VGA_55S        | VGA_SYNC | VGA_HSYNC_R              |
| (VGA_SYNC)                | VGA_55S        | VGA_SYNC | VGA_VSYNC_R              |
| (VGA_SYNC)                | VGA_55S        | VGA_SYNC | VGA_HSYNC                |
| (VGA_SYNC)                | VGA_55S        | VGA_SYNC | VGA_VSYNC                |
|                           | PP1V8_MEM      |          | PP1V8_S3                 |
|                           | PP1V8_MEM      |          | PP1V8_S3                 |
|                           | GND            |          | GND                      |
|                           | SB_POWER       |          | PP3V3_S5                 |
|                           | SB_POWER       |          | PP3V3_S0                 |
|                           | SB_POWER       |          | PP1V5_S0                 |
|                           | WWAN_SIM       | WWAN_SIM | WWAN_SIM_CLOCK           |
|                           | WWAN_SIM       | WWAN_SIM | WWAN_SIM_DATA            |

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## M75 Specific Constraints

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|                     | 87    | 88             |        |

# M75 Board-Specific Spacing & Physical Constraints

| BOARD LAYERS  |  |  |  | BOARD AREAS  |  |  |  | BOARD UNITS (MIL OR MM) | ALLEGRO VERSION |
|---|--|--|--|--------------|--|--|--|-------------------------|-----------------|
| TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM |  |  |  | NO_TYPE, BGA |  |  |  | MM                      | 15.5.1          |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DEFAULT           | *     | Y                     | =55_OHM_SE         | =55_OHM_SE         | 30 MM               | 0 MM                 | 0 MM              |
| STANDARD          | *     | Y                     | =DEFAULT           | =DEFAULT           | 12.7 MM             | =DEFAULT             | =DEFAULT          |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 55_OHM_SE         | TOP, BOTTOM | Y                     | 0.100 MM           | 0.100 MM           |                     |                      |                   |
| 55_OHM_SE         | ISL2, ISL11 | Y                     | 0.250 MM           | 0.076 MM           |                     |                      |                   |
| 55_OHM_SE         | *           | Y                     | 0.076 MM           | 0.076 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 50_OHM_SE         | TOP, BOTTOM | Y                     | 0.125 MM           | 0.125 MM           |                     |                      |                   |
| 50_OHM_SE         | *           | Y                     | 0.090 MM           | 0.090 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 45_OHM_SE         | TOP, BOTTOM | Y                     | 0.150 MM           | 0.150 MM           |                     |                      |                   |
| 45_OHM_SE         | *           | Y                     | 0.105 MM           | 0.105 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 40_OHM_SE         | TOP, BOTTOM | Y                     | 0.185 MM           | 0.185 MM           |                     |                      |                   |
| 40_OHM_SE         | *           | Y                     | 0.131 MM           | 0.131 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 27P4_OHM_SE       | TOP, BOTTOM | Y                     | 0.335 MM           | 0.335 MM           |                     |                      |                   |
| 27P4_OHM_SE       | *           | Y                     | 0.240 MM           | 0.240 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 70_OHM_DIFF       | *           | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 70_OHM_DIFF       | ISL3, ISL4  | Y                     | 0.149 MM           | 0.149 MM           |                     | 0.125 MM             | 0.125 MM          |
| 70_OHM_DIFF       | ISL9, ISL10 | Y                     | 0.149 MM           | 0.149 MM           |                     | 0.125 MM             | 0.125 MM          |
| 70_OHM_DIFF       | ISL2, ISL11 | Y                     | 0.185 MM           | 0.185 MM           |                     | 0.125 MM             | 0.125 MM          |
| 70_OHM_DIFF       | TOP, BOTTOM | Y                     | 0.185 MM           | 0.185 MM           |                     | 0.125 MM             | 0.125 MM          |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 80_OHM_DIFF       | *           | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 80_OHM_DIFF       | ISL3, ISL4  | Y                     | 0.115 MM           | 0.115 MM           |                     | 0.125 MM             | 0.125 MM          |
| 80_OHM_DIFF       | ISL9, ISL10 | Y                     | 0.115 MM           | 0.115 MM           |                     | 0.125 MM             | 0.125 MM          |
| 80_OHM_DIFF       | ISL2, ISL11 | Y                     | 0.140 MM           | 0.140 MM           |                     | 0.125 MM             | 0.125 MM          |
| 80_OHM_DIFF       | TOP, BOTTOM | Y                     | 0.140 MM           | 0.140 MM           |                     | 0.125 MM             | 0.125 MM          |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 85_OHM_DIFF       | *           | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 85_OHM_DIFF       | ISL3, ISL4  | Y                     | 0.101 MM           | 0.101 MM           |                     | 0.125 MM             | 0.125 MM          |
| 85_OHM_DIFF       | ISL9, ISL10 | Y                     | 0.101 MM           | 0.101 MM           |                     | 0.125 MM             | 0.125 MM          |
| 85_OHM_DIFF       | ISL2, ISL11 | Y                     | 0.125 MM           | 0.125 MM           |                     | 0.125 MM             | 0.125 MM          |
| 85_OHM_DIFF       | TOP, BOTTOM | Y                     | 0.125 MM           | 0.125 MM           |                     | 0.125 MM             | 0.125 MM          |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 90_OHM_DIFF       | *           | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 90_OHM_DIFF       | ISL3, ISL4  | Y                     | 0.102 MM           | 0.102 MM           |                     | 0.220 MM             | 0.220 MM          |
| 90_OHM_DIFF       | ISL9, ISL10 | Y                     | 0.102 MM           | 0.102 MM           |                     | 0.220 MM             | 0.220 MM          |
| 90_OHM_DIFF       | ISL2, ISL11 | Y                     | 0.130 MM           | 0.130 MM           |                     | 0.220 MM             | 0.220 MM          |
| 90_OHM_DIFF       | TOP, BOTTOM | Y                     | 0.130 MM           | 0.130 MM           |                     | 0.220 MM             | 0.220 MM          |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 100_OHM_DIFF      | *           | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 100_OHM_DIFF      | ISL3, ISL4  | Y                     | 0.080 MM           | 0.080 MM           |                     | 0.200 MM             | 0.200 MM          |
| 100_OHM_DIFF      | ISL9, ISL10 | Y                     | 0.080 MM           | 0.080 MM           |                     | 0.200 MM             | 0.200 MM          |
| 100_OHM_DIFF      | ISL2, ISL11 | Y                     | 0.099 MM           | 0.099 MM           |                     | 0.200 MM             | 0.200 MM          |
| 100_OHM_DIFF      | TOP, BOTTOM | Y                     | 0.099 MM           | 0.099 MM           |                     | 0.200 MM             | 0.200 MM          |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 110_OHM_DIFF      | *           | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 110_OHM_DIFF      | ISL3, ISL4  | Y                     | 0.077 MM           | 0.077 MM           |                     | 0.330 MM             | 0.330 MM          |
| 110_OHM_DIFF      | ISL9, ISL10 | Y                     | 0.077 MM           | 0.077 MM           |                     | 0.330 MM             | 0.330 MM          |
| 110_OHM_DIFF      | ISL2, ISL11 | Y                     | 0.089 MM           | 0.089 MM           |                     | 0.330 MM             | 0.330 MM          |
| 110_OHM_DIFF      | TOP, BOTTOM | Y                     | 0.089 MM           | 0.089 MM           |                     | 0.330 MM             | 0.330 MM          |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| DEFAULT          | *     | 0.1 MM               | ?      |
| STANDARD         | *     | =DEFAULT             | ?      |
| BGA_P1MM         | *     | =DEFAULT             | ?      |
| BGA_P2MM         | *     | =DEFAULT             | ?      |
| BGA_P3MM         | *     | =DEFAULT             | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| 1.5:1_SPACING    | *     | 0.15 MM              | ?      |
| 1.8:1_SPACING    | *     | 0.18 MM              | ?      |
| 2:1_SPACING      | *     | 0.2 MM               | ?      |
| 2.5:1_SPACING    | *     | 0.25 MM              | ?      |
| 3:1_SPACING      | *     | 0.3 MM               | ?      |
| 4:1_SPACING      | *     | 0.4 MM               | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| *                 | *                 | BGA       | BGA_P1MM         |
| MEM_CLK           | *                 | BGA       | BGA_P2MM         |
| CLK_FSB           | *                 | BGA       | BGA_P2MM         |
| CLK_PCIE          | *                 | BGA       | BGA_P2MM         |
| CLK_MED           | *                 | BGA       | BGA_P2MM         |
| CLK_SLOW          | *                 | BGA       | BGA_P2MM         |
| FSB_DSTB          | FSB_DSTB          | BGA       | BGA_P3MM         |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 1:1_DIFFPAIR      | *     | Y                     | =STANDARD          | =STANDARD          | =STANDARD           | 0.1 MM               | 0.1 MM            |

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| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 100_DIFF_BGA      | *           | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| 100_DIFF_BGA      | ISL3, ISL4  | Y                     | 0.075 MM           | 0.075 MM           |                     | 0.125 MM             | 0.125 MM          |
| 100_DIFF_BGA      | ISL9, ISL10 | Y                     | 0.075 MM           | 0.075 MM           |                     | 0.125 MM             | 0.125 MM          |

NOTE: 100\_DIFF\_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

**M75 Rule Definitions**  
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