1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC,MACBOOK PRO 17"

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

9/26/2006

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7164	1	SCHEM,TRUCKEE,M57	SCH	CRITICAL	
820-2059	1	PCBF,TRUCKEE,M57	PCB	CRITICAL	

DRAWING
TITLE=TRUCKEE
ABBREV=DRAWING
LAST_MODIFIED=Tue Sep 26 13:17:56 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

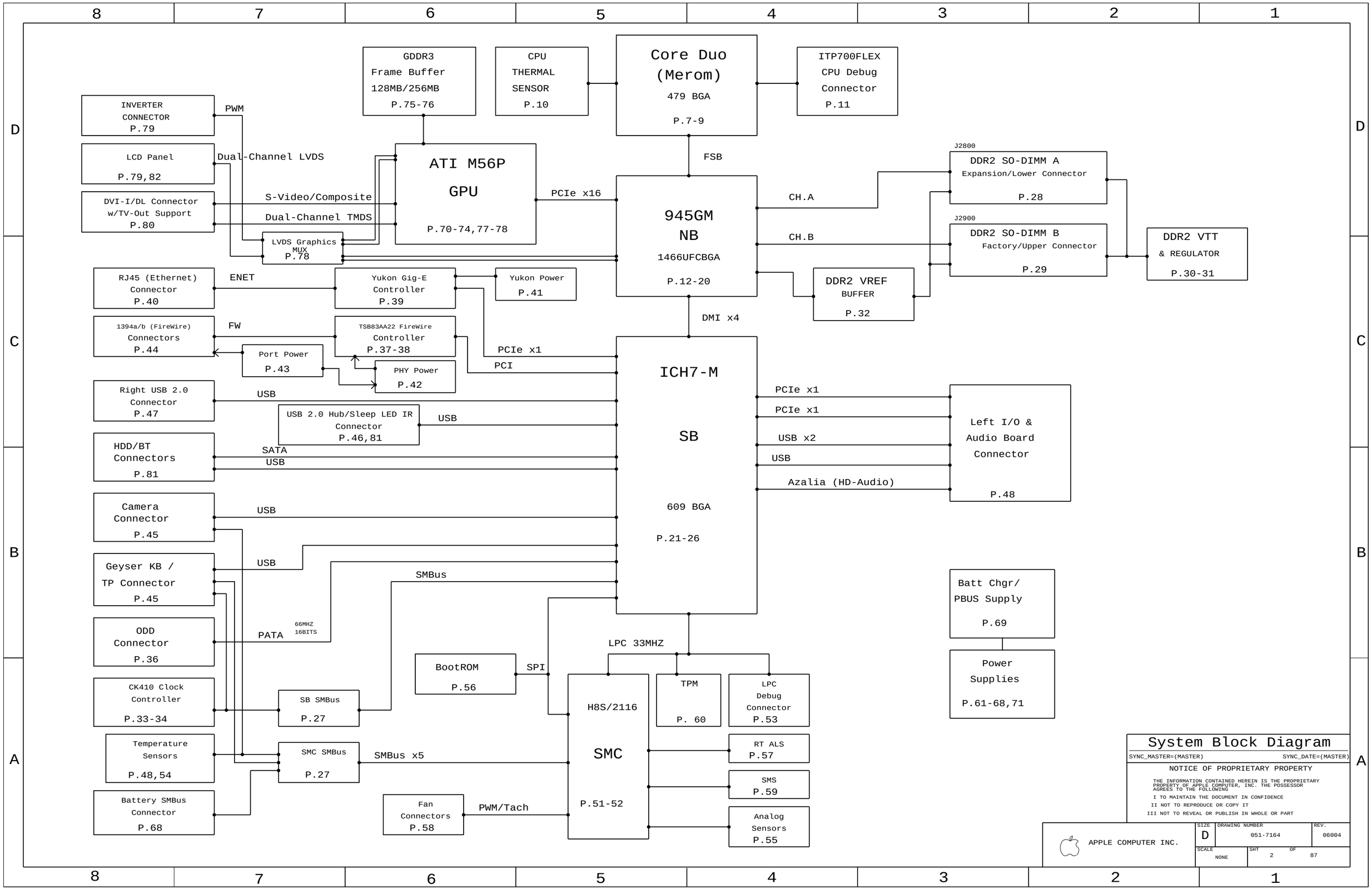
SIZE D

Apple Computer Inc.

TITLE
SCHEMATIC,MACBOOK PRO 17

DRAWING NUMBER 051-7164
REV. 06004

SHT 1 OF 87


GDDR3
Frame Buffer
128MB/256MB
P.75-76
CPU
THERMAL
SENSOR
P.10
Core Duo
(Merom)
479 BGA
P.7-9
ITP700FLEX
CPU Debug
Connector
P.11
INVERTER
CONNECTOR
P.79
PWM
LCD Panel
P.79,82
Dual-Channel LVDS
DVI-I/DL Connector
w/TV-Out Support
P.80
S-Video/Composite
Dual-Channel TMDS
LVDS Graphics
MUX
P.78
ATI M56P
GPU
P.70-74,77-78
PCIe x16
FSB
945GM
NB
1466UFCBGA
P.12-20
J2800
DDR2 SO-DIMM A
Expansion/Lower Connector
P.28
CH.A
J2900
DDR2 SO-DIMM B
Factory/Upper Connector
P.29
CH.B
DDR2 VTT
& REGULATOR
P.30-31
DDR2 VREF
BUFFER
P.32
RJ45 (Ethernet)
Connector
P.40
ENET
Yukon Gig-E
Controller
P.39
Yukon Power
P.41
1394a/b (FireWire)
Connectors
P.44
FW
TSB83AA22 FireWire
Controller
P.37-38
Port Power
P.43
PHY Power
P.42
PCIe x1
PCI
DMI x4
ICH7-M
SB
609 BGA
P.21-26
Right USB 2.0
Connector
P.47
USB
USB 2.0 Hub/Sleep LED IR
Connector
P.46,81
USB
HDD/BT
Connectors
P.81
SATA
USB
Camera
Connector
P.45
USB
Geyser KB /
TP Connector
P.45
USB
ODD
Connector
P.36
PATA
66MHZ
16BITS
SMBus
CK410 Clock
Controller
P.33-34
SB SMBus
P.27
Temperature
Sensors
P.48,54
SMC SMBus
P.27
SMBus x5
Battery SMBus
Connector
P.68
Fan
Connectors
P.58
PWM/Tach
BootROM
P.56
SPI
LPC 33MHZ
H8S/2116
SMC
P.51-52
TPM
P. 60
LPC
Debug
Connector
P.53
RT ALS
P.57
SMS
P.59
Analog
Sensors
P.55
PCIe x1
PCIe x1
USB x2
USB
Azalia (HD-Audio)
Left I/O &
Audio Board
Connector
P.48
Batt Chgr/
PBUS Supply
P.69
Power
Supplies
P.61-68,71
System Block Diagram
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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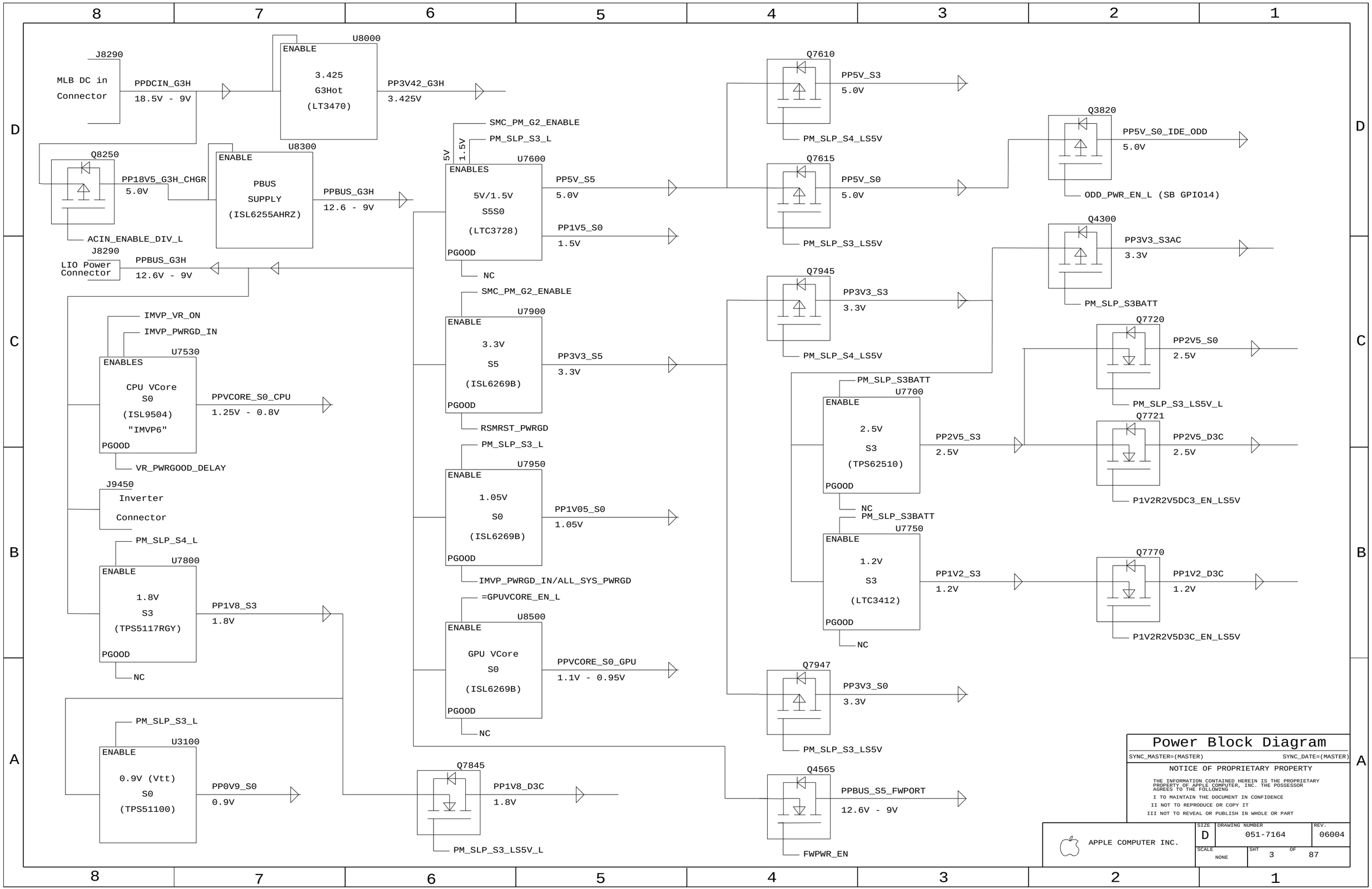
APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-7164
REV.
06004
SCALE
NONE
SHT
2
OF
87



Power Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	3	87

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7814	TRUCKEE,2.33GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJK

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG

BOM GROUP	BOM OPTIONS
M57_COMMON	ALTERNATE,COMMON,M57_COMMON1,M57_COMMON2,M57_COMMON3,M57_COMMON4,M57_DEBUG
M57_COMMON1	ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL,D3CPGOOD_3V3,ISL6255A,NO_3G
M57_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M57_COMMON3	LVDS_PD,FW_PORT_FAULT_PU
M57_COMMON4	BOOTROM_DEVEL,SMC_PRGRM
M57_DEBUG	ITP,LPCPLUS
M57_TPM	TPM

BAR CODE LABELS / EEE #'S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WJK]	CRITICAL	EEE_WJK

MODULE PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0368	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON

ALTERNATE PARTS

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445		ALL	S17806ADN for FDM6296
128S0083	128S0073		C2516	1.86 MAX ALT TO 1.9 MAX
128S0093	128S0092		ALL	KEMET IS ALT TO SANYO
353S1465	353S1461		ALL	Screened ISL6262 for ISL9504
152S0287	152S0435		ALL	Alternates for Coilcraft MSS5131

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1931	1	IC,PRGRM,SMC(NEW),M57	U5800	CRITICAL	SMC_PRGRM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1924	1	IC, BOOTROM, DEVELOPMENT, UNLOCKED ,M57	U6301	CRITICAL	BOOTROM_DEVEL
341S1925	1	IC, BOOTROM, FINAL, LOCKED, M57	U6301	CRITICAL	BOOTROM_FINAL
353S1461	1	IC,ISL9504,SYNC REG CTL,QFN 48	U7530	CRITICAL	
359S0109	1	IC,LOW POWER CLOCK SYNTHESIZER,68PIN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3393	1	IC,MDC,B2,PRQ,2.33GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_33GHZ_B2
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	

Extra TPM options:
SMC_TPM_GPIO2
SMC_TPM_GPIO1
SMC_TPM_PP

BOM CONFIGURATION

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	4	87

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	61C7
TRUE		P5VS5_RUNSS	62C5 66A6
TRUE		P1V5S0_RUNSS	62C4 66C6
TRUE		P2V5S3_MODE	
TRUE		P2V5S3_SHDNRT	
TRUE		P1V2S3_RT	63B6
TRUE		P1V2S3_RUNSS	41C4 63B7
TRUE		P1V8S3_COMP	
TRUE		P1V8S3_FSET	
TRUE		P3V3S5_COMP	65C6
TRUE		P3V3S5_FSET	65D6
TRUE		P1V05S0_COMP	65A7
TRUE		P1V05S0_FSET	65B7
TRUE		P3V42G3H_FB	66C3
TRUE		GPUVCORE_COMP	71C7
TRUE		GPUVCORE_FSET	71C7
TRUE		GPUBBP_ADJ	71B7

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 87D6
TRUE		FSB_ADS_L	7D6 12C4 87D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 87C6
TRUE		FSB_BNR_L	7D6 12C4 87D6
TRUE		FSB_BREQ0_L	7D6 12C4 87D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 87D6
TRUE		FSB_DBSY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_DRDY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_HIT_L	7D6 12B4 87D6
TRUE		FSB_HITM_L	7D6 12B4 87D6
TRUE		FSB_LOCK_L	7D6 12B4 87D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 87D6

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14B4 22D2
TRUE	DMI_N2S_N<1..0>	14B4 22D2
TRUE	SB_CLK100M_SATA_P	21B6 33B4 34C3 34C5
TRUE	SB_CLK100M_SATA_N	21B6 33B4 34C3 34C5
TRUE	USB_BT_P	6C1 6C2 6C3 22C2 81A4
TRUE	USB_BT_N	6C1 6C2 6C3 22C2 81A4

Misc NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		USB2_CAMERA_P_F	45B5
TRUE		USB2_CAMERA_N_F	45B5
TRUE		TP_FW_CTL<0>	37C3

Functional Test Points

Power Nets

FUNC_TEST		
TRUE	PP0V9_S0	19D3 34B8 34C8 34C8 35B4 65A2 67D6 67D8
TRUE	PP1V05_S0	19D3 34C8 34D3 34D3 37D3 37D4
TRUE	PP1V2_D3C	68E 78C 78E 79C 8C7 8D7
TRUE	PP1V2_S3	11B3 11C5 12A7 12B7 12C2 19C8 19D1 19D2 19D5 19D6
TRUE	PP1V5_S0	5A4 39A8 39D7 63B3 67D6 67D8
TRUE	PP1V5_S0_NB	19C5 19D3 19D2 19D5 19D6 19D7 19D1 19D2 19D4 37C4
TRUE	PP1V8_S3	31C5 32C6 37B2 64A6 64C1
TRUE	PP1V8_D3C	38D3 38D4 39B2 39D3 39D6 67B6 67B8
TRUE	PP2V5_S0	64A4 67B6 67B8 72B8 73A5 73A8 73B5 73B8 75D5 75D6 76D5 76D8 82D7
TRUE	PP2V5_D3C	37C6 37D6 39A4 39A6 39A8 19C5 19D7 63D1 66B6 67A6
TRUE	PP3V3_S0	63C1 67A6 67A8 77A8 77C6 78C8 82D7
TRUE	PP3V3_S3	
TRUE	PP3V3_S5	65D8 66C5 67C3 67D3 67D5 79D5 24C3 25B6 25C8 25D2 25C7 11B6 22C6 23D8 23A7 23B7
TRUE	PP5V_S0	62D1 63B8 63C6 65A1 65B2
TRUE	PP5V_S3	5B2 45C3 52B8 62A2 67B1 67B3 81C4 81C6
TRUE	PP5V_S5	60B8 66D6 67B1 67C1 67C3 69C8 67C7 62B5 62A1 62B2
TRUE	PPBUS_G3H	62B6 62C8 64C8 65B7 65D6 71D7
TRUE	GND	6A1 41C6 42B8 43D8 45D3 61D4 61D7 62D7 64A6 67D7 68E7 68D4 69C1 71D7 79B7

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST		
TRUE	IMVP_VR_ON	51D7 61C7
TRUE	IMVP_DPRSLPVR	61C7 87C6
TRUE	PM_SLP_S3_L	66C8
TRUE	PM_SLP_S3BATT	27C3 32B3 39C8 42A8 42C8 51C5 55D3 65B8 66B6 66C7 41B5
TRUE	PM_SLP_S4_L	66B8
TRUE	PM_SLP_S5_L	6C1 6A1 6A2 23C3 41B6 47C7 48C3 51C5 52A2
TRUE	P1V5P1V05S0_PGOOD	23C3 51C5 52A2
TRUE	CPU_DPRSTP_L	61C7 65B8 66B2 66B3 66B5
TRUE	IMVP6_VID<6..0>	7B3 21C4 61C7
TRUE	FSB_CLK_CPU_N	9C1 61C7
TRUE	FSB_CLK_CPU_P	7C6 33C4 34D3 34D5
TRUE	PLT_RST_L	7C6 33C4 34D3 34D5
TRUE	PLT_RST_L	82A4 82A 6C6 6C7 14B7 22A6 26A4 26B1 26C3 26C3 79A8
TRUE	PEG_RESET_L	5C4 6C6 6C7 14B7 22A6 26A4 26B1 26C1 26C3 79A8 82A4 26B1 70A5 82A4
TRUE	SMC_LRESET_L	26B1 51C7
TRUE	TPM_LRESET_L	26B1 60B7
TRUE	CPU_STPCLK_L	7C8 21C4 87C6
TRUE	FSB_CLK_NB_P	12A6 33C4 34D3 34D5
TRUE	FSB_CLK_NB_N	12A6 33C4 34D3 34D5
TRUE	CLK_NB_OE_L	14B6 33B4
TRUE	NB_CLK100M_GCLKIN_P	14C4 33B4 34C4 34C5
TRUE	NB_CLK100M_GCLKIN_N	14C4 33B4 34C4 34C5
TRUE	NB_CLK_DREFCLKIN_P	14C4 34B2 34B4
TRUE	NB_CLK_DREFCLKIN_N	14C4 34B2 34B4
TRUE	NB_CLK_DREFSSCLKIN_P	14B4 33B4 34B4 34B5
TRUE	NB_CLK_DREFSSCLKIN_N	14C4 33B4 34B4 34B5
TRUE	CPU_THERMTRIP_R	21C2
TRUE	TP_SB_SUS_CLK	6C6 6C7 23C3

MAC-1 TPs

FUNC_TEST		
TRUE	CPU_PWRGD	7B3 21C4 87C6
TRUE	TP_CPU_CPUSLP_L	21C4
TRUE	PM_DPRSLPVR	14B7 23C3 61C8 87C6
TRUE	CPU_DPSLP_L	7B3 21C4 87C6
TRUE	PM_LAN_ENABLE	23C3 51D7
TRUE	PCI_RST_L	22A6 37C2
TRUE	PM_RSMRST_L	23C1 51D7
TRUE	PM_SB_PWROK	23C3 26A6
TRUE	SB_RTC_RST_L	21D6 26D4
TRUE	PM_STPCPU_L	23C8 33C4
TRUE	PM_STPPCI_L	23C8 33C4
TRUE	VR_PWRGD_CK410	23C5 26B8
TRUE	VR_PWRGOOD_DELAY	14B6 26B5 61C7
TRUE	FSB_CPURST_L	7D6 11B5 12C4 87D6
TRUE	FSB_SLPCPU_L	7A3 12A4
TRUE	FSB_DPWR_L	7B3 12B4 87D6
TRUE	NB_SB_SYNC_L	14B6 22A6
TRUE	PP2V5_S0_GPU_TPVDD	78C7
TRUE	PP2V5_S0_GPU_TXVDDR	78C7
TRUE	PP2V5_S0_GPU_AVDD	78C7
TRUE	PP2V5_S0_GPU_A2VDD	78B7
TRUE	PP2V5_S0_GPU_LPVDD	78B7 66B6 67A2 67B3 67C3 67C5 71D2 79A8 79D3
TRUE	PP2V5_S0_GPU_LVDDR	78B7 26B4 26B6 26B8 26D1 27C3 27D3 33C7 33D3 33D6 34A8 36D6 40B4 26B4 26B6 26B8 26D1 27C3 27D3 33C7 33D3 33D6 34A8 36D6 40B4
TRUE	PP3V3_S0	29A4 29B4 (=PP3V3_S0_CK410)
TRUE	PP3V3_S0_CK410_VDD48	19C7 19D6 19C6 19C7 19C7 21C3 21D3 22B5 23B3 23D5
TRUE	PP3V3_S0_CK410_VDD_PCI	27B8 27C6 65C2 65C3 65D2 49B5 49C4 49C7 52D3 54B5
TRUE	PP3V3_S0_CK410_VDD_REF	49B6 49C4 49C7 52D3 54B5 62A6 65B1 65D6 66B1 66B5 82A4 82B3 82C6 82D5
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC	33C5
TRUE	PP3V3_S0_CK410_VDDA	
TRUE	PP3V3_FWPHY	6C3 6C5 6C6 38B5 38D7 42C4 43B8 44A8 44B8
TRUE	PP3V3_FWPHY_AVDD	38D5
TRUE	PP3V3_FWPHY_PLLVDD	38C6
TRUE	PP1V95_FWPHY	6C3 6C5 6C6 38B2 38D5 42C1
TRUE	PP1V95_FWPHY_PLLVDD	38D3
TRUE	PP1V2_S3	5D4 39A8 (=PP1V2_S3_ENET) 39D7 63B3 67D6 67D8
TRUE	PP3V3_S3AC	39A5 39B4 (=PP3V3_S3_ENET) 39B5 39B8 39D6 39D8 42C4 67D1 67D3
TRUE	PP2V5_S3	39D3 63C3 (=PP2V5_S3_ENET) 63D3 63D4 67B6 67B8
TRUE	PP2V5_S3_ENET_AVDD	39D5 40D5

Fan Connectors

FUNC_TEST		
TRUE	PP5V_S0	71A4 78B8 80A1 80B5 81B7 5D3 5D4 25D8 31D1 62B1 5D4 25D8 31C5 36D6 53C4 55A8 57B5 60B5 67A1 67B1 67B3
TRUE	FAN_LT_PWM	19D7 21C1 24C3 24D3 25C4 58B6
TRUE	FAN_LT_TACH	58B6
TRUE	FAN_RT_PWM	19D7 62A7 67B6 67C6 67C8 58B3
TRUE	FAN_RT_TACH	58B3

LPC+ Debug Connector

FUNC_TEST		
TRUE	PP3V42_G3H	66D2 67D3 67D5 68B8 69A8 69B8 69C8 81D4 26D6 27C3 35B7 47B5 51C2 51D3 51D4 53B1 52B5 52B7
TRUE	PP5V_S0	67B3 71A6 79B8 80A1 80B5 81B3 52D7 53C4 66A8 66C8 62B1 66B5 67A1 67B1
TRUE	LPC_AD<0>	21D4 51D7 53C4 60C6
TRUE	LPC_AD<1>	21D4 51D7 53C4 60C6
TRUE	LPC_FRAME_L	21C5 51C7 53C4 60C6
TRUE	PM_CLKRUN_L	23C8 51C5 53C4 60C6
TRUE	BOOT_LPC_SPI_L	22B3 51C7 53B4
TRUE	SMC_TMS	51B5 52B2 53B4
TRUE	DEBUG_RST_L	26B1 53B4
TRUE	SMC_TRST_L	51C1 53B4
TRUE	SMC_TDO	51B5 52B2 53B4
TRUE	SMC_MD1	51C1 53B4
TRUE	SMC_TX_L	47B5 51C7 52B2 52B3 53B4
TRUE	FWH_INIT_L	21C4 51D5 52D3 52D5
TRUE	PCI_CLK_PORT80_LPC	34D6 53C5
TRUE	LPC_AD<2>	21D4 51C7 53C5 60C6
TRUE	LPC_AD<3>	21D4 51C7 53C5 60C6
TRUE	INT_SERIRQ	23C8 51C7 53C5 60C6
TRUE	PM_SUS_STAT_L	23C5 51C5 52A2 53B5 60C6
TRUE	SMC_TDI	51B5 52B2 53B5
TRUE	SMC_TCK	51C5 52B2 53B5
TRUE	SMC_RST_L	51C3 52D6 53B5
TRUE	SMC_NMI	51C1 53B5
TRUE	SMC_RX_L	47B5 51C7 52B2 52B3 53B5
TRUE	SV_SET_UP	23B6 23C3 53B5

Resistor Calibration

FUNC_TEST		
TRUE	PP5V_S0_ISENSECAL	67D8 67D8 5A4 65A2 67D6 25C4 25D3 34B8 34C6 19D7 21C1 24C3 24D3 25C4 19D1 19D2 19D5 19D6 19D7 62A7 67B6 67C6 67C8 5D4 78C 78E 7C8 8C7
TRUE	PP1V8_S3	
TRUE	PP1V05_S0	
TRUE	PPVCORE_S0_CPU	88B5 8D7 9D7 55A6 55D7 61D1 67D1 67D3
TRUE	PPVCORE_D3C_GPU	55A5 55C7 67A6 67A8 71B7 71C1 72D8 77A7
TRUE	ISENSE_CAL_EN	51B7 55A8
TRUE	GND	

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST		
TRUE	PP5V_S3	5D4 45C8 52B8 62A2 67B1 67B3 81C4 81C6
TRUE	USB2_CAMERA_N	6D1 6D2 6D3 22C2 45D3
TRUE	USB2_CAMERA_P	6D1 6D2 6D3 22C2 45B3
TR2G0	PP5V_S3_CAMERA_F	45C5

Inverter Connector

TR27A	GND_CHASSIS_INVERTER	5B2 6A6 6A8 45B5 45C5 79A5 79A6
TR27B	PPBUS_S0_INVERTER	79B5
TR27C	PP5V_INVERTER_SW	79B5
TR27D	INVERTER_PWM	79A5
TR27E	GND_CHASSIS_INVERTER	5B2 6A6 6A8 45B5 45C5 79A5 79A6

Thermal Sensors

FUNC_TEST		
TH173	HSTHMSNS_DX_P	
TH174	HSTHMSNS_DX_N	54C5
TH172	RSFSTHMSNS_D_P	54D5
TH175	RSFSTHMSNS_D_N	54C5

SMC TPs

FUNC_TEST		
TR27	PM_SYSRST_L	23C5 26C5 51B7
TR76	SMC_ONOFF_L	51C5 52B2 52C6 81C4

Battery Connector

FUNC_TEST		
TR19	BATT_POS	68A1 68A2 69B1
TR18	BATT_NEG	68B1 68B2

LPC+ Debug Connector

FUNC_TEST		
TR19	SMC_BS_ALRT_L	51C5 52B2 68B2
TR20	SMBUS_SMC_BSA_SCL	27C1 27C2 27C3 51B5 68B2
TR21	SMBUS_SMC_BSA_SDA	27C1 27C2 27C3 51B5 68B2

Left I/O Data Connector

FUNC_TEST		
TR23	PP1V5_S0	62A8 62C1 66C5 66D6 66C3 25C6 5D4 8B7 9B7 24A3 24A5 24B5 25A6 25B2 67C5 67C6 67C8
TR24	ALS_GAIN	6D5 48C4 51B5
TR25	LTALS_OUT	48C3 57C7
TR26	ACZ_SDATAIN<0>	21C7 48B3 87B4
TR27	ACZ_SDATAOUT	21C7 48B3 87B4
TR28	ACZ_BITCLK	21C7 48B3 87B4
TR29	ACZ_RST_L	21C7 48B3 87B4
TR30	EXCARD_OC_L	6C1 6C3 22C4 22D8 48C3 52B3
TR31	LTUSB_OC_L	6D1 6D3 22C4 22D8 48C3
TR32	LT2USB_OC_L	6C1 6C3 22C4 22D8 48C3
TR33	PM_SLP_S3_LS5V	6A1 6A2 48C3 62B3 66C6 66C7 5C4 6A1 6A2 22C3 41B6 47C7 48C3 51C5 66A6 66B8 48C3 51B7
TR34	PM_SLP_S4_L	64C8
TR35	SYS_ONEWIRE	
TR36	MINI_CLKREQ_L	33B4 34A3 52B2 34A4 48C3
TR37	SMC_EXCARD_CP	48C3 51B7 52A2
TR38	EXCARD_CLKREQ_L	33B4 34A3 34A4 48C3
TR39	SMC_EXCARD_PWR_EN	48C3 51B7
TR40	LIO_PLT_RESET_L	26C1 48C3
TR41	ACZ_SYNC	21C7 48B3 87B4
TR42	USB2_LT_N	6D1 6D2 6D3 22C2 48C6
TR43	USB2_LT_P	6D1 6D2 6D3 22C2 48C6
TR44	USB2_EXCARD_N	6C1 6C2 6C3 22C2 48C6
TR45	USB2_EXCARD_P	6C1 6C2 6C3 22C2 48C6
TR46	PCIE_EXCARD_R2D_C_N	48B6 50C5 50C6
TR47	PCIE_EXCARD_R2D_C_P	48B6 50C5 50C6
TR48	PCIE_EXCARD_D2R_N	22D4 48B6 50B3 50B5 50B6
TR49	PCIE_EXCARD_D2R_P	22D4 48B6 50C3 50C5 50C6
TR50	PCIE_CLK100M_EXCARD_P	33B4 34C3 34C5 48B6
TR51	PCIE_CLK100M_EXCARD_N	33B4 34B3 34B5 48B6
TR52	USB2_LT2_N	6C1 6C2 6C3 22C2 48C6
TR53	USB2_LT2_P	6C1 6C2 6C3 22C2 48C6
TR54	PCIE_MINI_R2D_C_N	48C6 50C5 50C6
TR55	PCIE_MINI_R2D_C_P	48C6 50C5 50C6
TR56	PCIE_MINI_D2R_N	22D4 48C6 50C3 50C5 50C6
TR57	PCIE_MINI_D2R_P	22D4 48C6 50C3 50C5 50C6
TR58	PCIE_CLK100M_MINI_P	33B4 34D4 34D5 48C6
TR59	PCIE_CLK100M_MINI_N	33B4 34D4 34D5 48C6
TR60	SMBUS_SB_SCL	46B6 48B3 81C3
TR61	SMBUS_SB_SDA	28A6 29A6 33B6 67D2 67D5 67D6
TR62	PCIE_WAKE_L	23C8 39C6 48C3
TR63	SMC_BC_ACOK	48C3 51C3 52A2
TR64	SMBUS_SMC_A_S3_SCL	27C3 27C5 27D2 27D6 48B6 51B5
TR65	SMBUS_SMC_A_S3_SDA	27B3 27C3 27C5 27C6 48B6 51B5

Left I/O Power Connector

FUNC_TEST		
TR66	PP18V5_DCIN	68B8 68C5
TR67	PPBUS_G3H	61D7 62D7 64A6 65A4 65C4 65D4 65D6 67C1 67C3 68D5 69C1 71D7 79B7
TR68	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT 5 OF 87

NC_CPU_A32_L
NC_CPU_A33_L
NC_CPU_A34_L
NC_CPU_A35_L
NC_CPU_A36_L
NC_CPU_A37_L
NC_CPU_A38_L
NC_CPU_A39_L
NC_CPU_APM0_L
NC_CPU_APM1_L
NC_CPU_EXTBREF
NC_CPU_HFPLL
NC_CPU_SPARE0
NC_CPU_SPARE1
NC_CPU_SPARE2
NC_CPU_SPARE4

NC_MEM_A_A<15..14>
NC_MEM_B_A<15..14>
TP_NB_CFG<4..3>
TP_NB_CFG<6>
TP_NB_CFG<8>
TP_NB_CFG<11..10>
TP_NB_CFG<15..14>
TP_NB_CFG<17>

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12>
TP_SB_SUS_CLK

MEM_A_A<15..14>
MEM_B_A<15..14>
NB_CFG<4..3>
NB_CFG<6>
NB_CFG<8>
NB_CFG<11..10>
NB_CFG<15..14>
NB_CFG<17>
NB_CFG<13..12>
TP_SB_SUS_CLK

Inverter PWM Reset Alias

PLT_RST_L

R0600

ALS_GAIN — 0 — RTALS_GAIN — RTALS_GAIN
MAKE_BASE=TRUE
5% 1/16W MF-LF 402

NC_ENET_CTRL12
NC_ENET_CTRL25
MAKE_BASE=TRUE
NO_TEST=TRUE

Ethernet Powr Management Support

ENET_LOWPWR_EN

R0690

SB_GPIO30 — 0 — ENET_LOWPWR_EN
5% 1/16W MF-LF 402

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

FireWire Aliases

PPFW_PORTA_VP_UF
PPFW_PORTB_VP_UF
MAKE_BASE=TRUE

PP3V3_FWPHY
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.20 mm
MAKE_BASE=TRUE

PP1V95_FWPHY
VOLTAGE=1.95V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
MAKE_BASE=TRUE

SMC_RSTGATE_L
=FW_PCI_IDSEL
PCI_GNT3_L
PCI_REQ3_L
MAKE_BASE=TRUE

USB Port "A" (Debug Port) = Right USB 2.0 Port

USB2_RT_P
USB2_RT_N
RTUSB_OC_L
MAKE_BASE=TRUE

USB Port "B" = Trackpad (Geyser)

USB_TRACKPAD_P
USB_TRACKPAD_N
UNUSED_USB_B_OC_L
MAKE_BASE=TRUE

USB Port "C" = Left USB 2.0 Port

USB2_LT_P
USB2_LT_N
LTUSB_OC_L
MAKE_BASE=TRUE

USB Port "D" = Camera

USB2_CAMERA_P
USB2_CAMERA_N
UNUSED_USB_D_OC_L
MAKE_BASE=TRUE

USB Port "E" = ExpressCard

USB2_EXCARD_P
USB2_EXCARD_N
EXCARD_OC_L
MAKE_BASE=TRUE

USB Port "F" = USB 1.1 Hub

USB_HUB_P
USB_HUB_N
MAKE_BASE=TRUE

USB Port "G" = Bluetooth (M13P)

USB_BT_P
USB_BT_N
MAKE_BASE=TRUE

USB Port "H" = 2nd Left USB 2.0 Port

USB2_LT2_P
USB2_LT2_N
LT2USB_OC_L
MAKE_BASE=TRUE

TP_USB2_3G_P
TP_USB2_3G_N
MAKE_BASE=TRUE

LVDS Pull Down Aliases

=LVDS_PD_L_CLK_N
=LVDS_PD_L_CLK_P
LVDS_L_DATA_P<1>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
LVDS_L_DATA_N<2>
LVDS_L_DATA_P<2>
MAKE_BASE=TRUE

=LVDS_PD_U_CLK_N
=LVDS_PD_U_CLK_P
LVDS_U_DATA_N<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_P<2>
LVDS_U_DATA_N<2>
LVDS_U_CLK_N
LVDS_U_CLK_P
MAKE_BASE=TRUE

Base net is PM_SLP_S3_LS5V

PM_SLP_S4_L
MAKE_BASE=TRUE

Base net is PM_SLP_S4_L

PM_SLP_S3_LS5V
MAKE_BASE=TRUE

Thermal Module Holes

Add one through via per hole to GND or 2 blind vias per side per hole to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Lower Left GPU TM Hole

Frame holes

Chassis connection to be made at the fan cutout near the right ALS. Not stuffed at Proto.

NO STUFF
SH0601 EMI-SPRING 0G-502620M
GND_CHASSIS_FANFRAME
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
NO STUFF R0601 0 5% 1/10W MF-LF 402

Chassis connection to be made at the mounting hole northwest of the DVI connector. Plated hole.

ZT0600 195R106
GND_CHASSIS_DVI_TOP
C0600 0.01UF 10% 50V X7R 402
GND_CHASSIS_DVI_TOP
GND

Chassis connection to be made on FW shell

ZT0603 HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT
NO STUFF R0602 0 5% 1/10W MF-LF 402
GND_CHASSIS_DVI_BOT

ZT0604 HOLE-VIA-P5RP25
GND_CHASSIS_ENET
GND_CHASSIS_ENET
GND_CHASSIS_ENET

Chassis connection to be made at the mounting hole southwest of the USB connector. Plated hole.

ZT0601 195R106
GND_CHASSIS_USB
GND_CHASSIS_USB
GND_CHASSIS_USB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602 HOLE-VIA-P5RP25
GND_CHASSIS_LVDS
C0602 0.01UF 10% 50V X7R 402
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS

SH0600 OG-503040 SHLD-SM-LF
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
LEFT CLUTCH BARREL CABLING

ZT0612 HOLE-VIA-P5RP25 GND_CHASSIS_LIOFLEX_HOLE
C0612 0.01UF 10% 50V X7R 402
C0613 0.01UF 10% 50V X7R 402

ZT0611 HOLE-VIA-P5RP25 GND_CHASSIS_BATTCONN_HOLE
C0619 0.01UF 10% 50V X7R 402
C0614 0.01UF 10% 50V X7R 402
GND_CHASSIS_BATTCONN_HOLE

ZT0610 HOLE-VIA-P5RP25 GND_CHASSIS_LNDACARD_HOLE
C0615 0.01UF 10% 50V X7R 402
C0616 0.01UF 10% 50V X7R 402

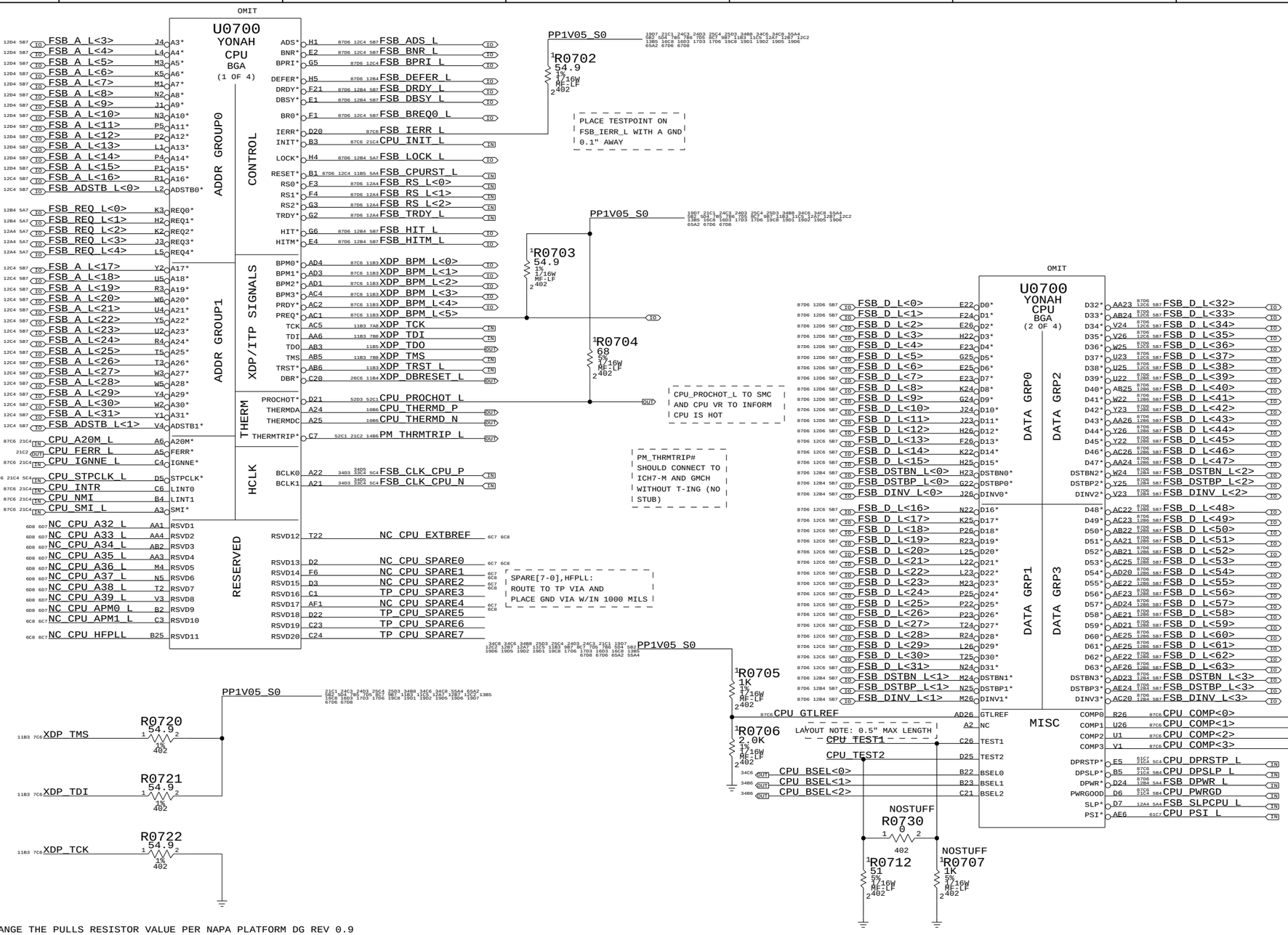
ZT0613 HOLE-VIA-P5RP25 GND_CHASSIS_ODD_HOLE
C0610 0.01UF 10% 50V X7R 402
C0611 0.01UF 10% 50V X7R 402

ZT0614 HOLE-VIA-P5RP25 GND_CHASSIS_LEFT_DIMM_HOLE
C0617 0.01UF 10% 50V X7R 402
C0618 0.01UF 10% 50V X7R 402

Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7164
REV. 06004
SCALE NONE
SHT 6 OF 87



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

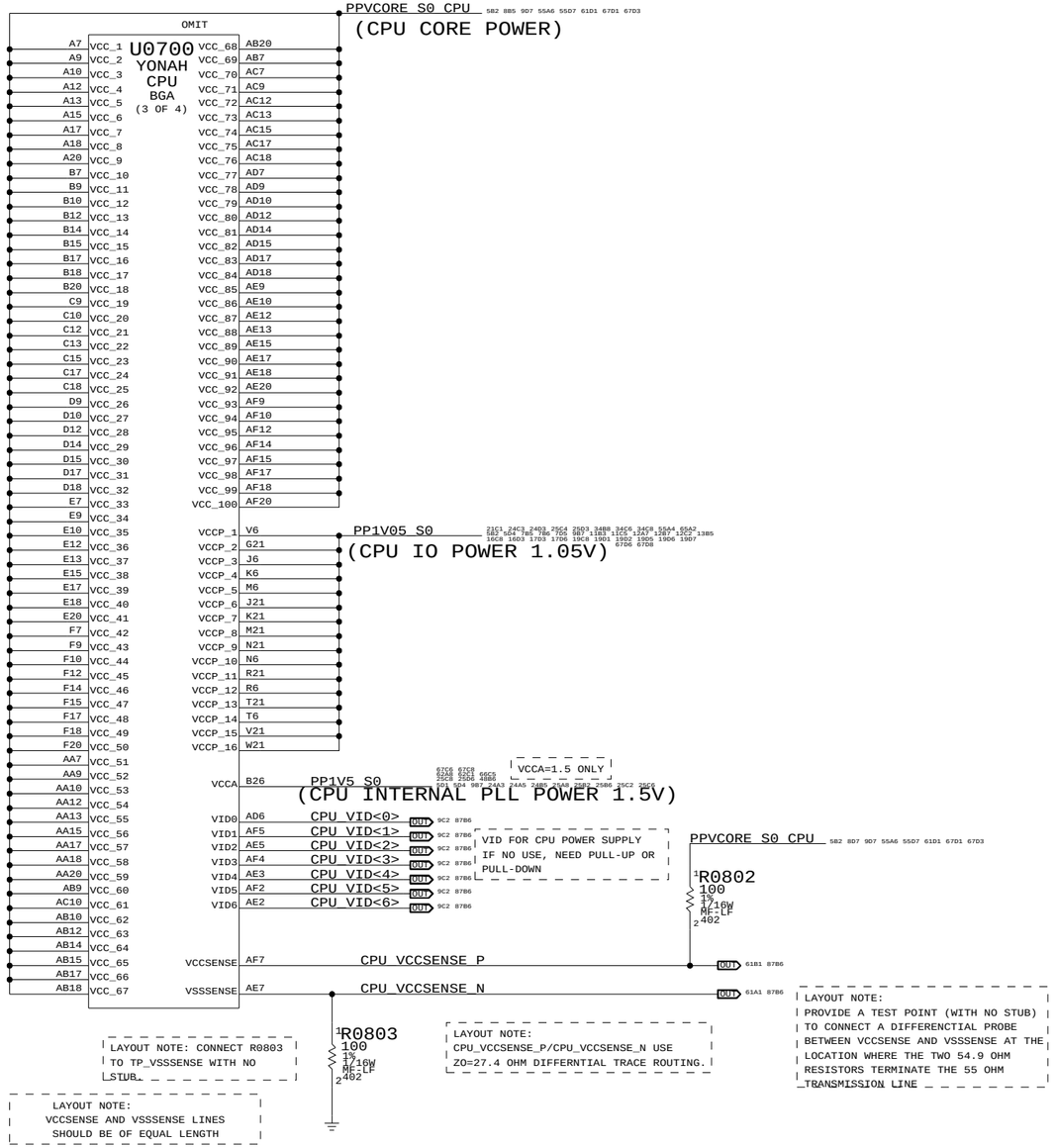
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

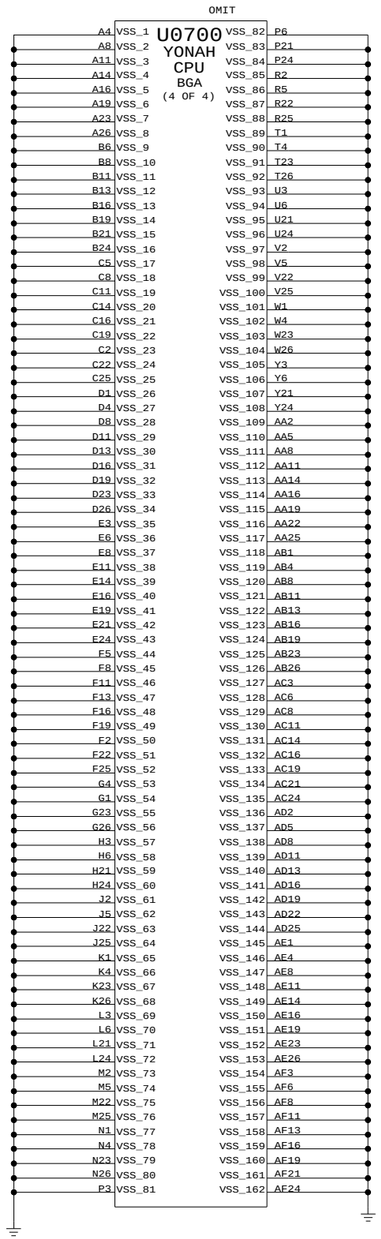
CPU 1 OF 2-FSB

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 7 OF 87	





CPU 2 OF 2-PWR/GND

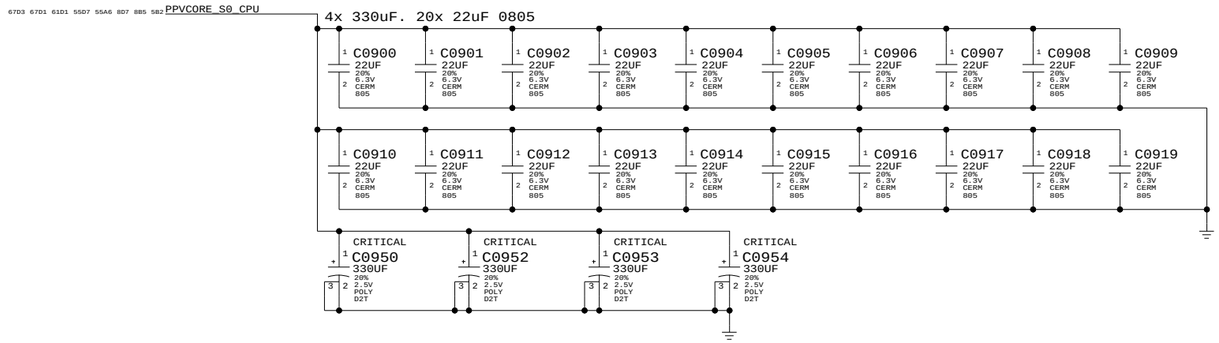
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

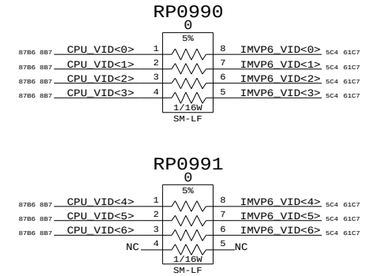
SCALE	SHT	OF
NONE	8	87

CPU VCORE HF AND BULK DECOUPLING

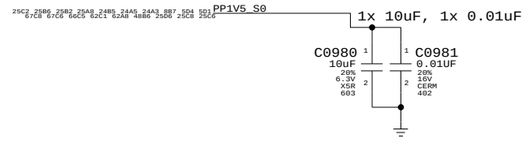


CPU VCORE VID Connections

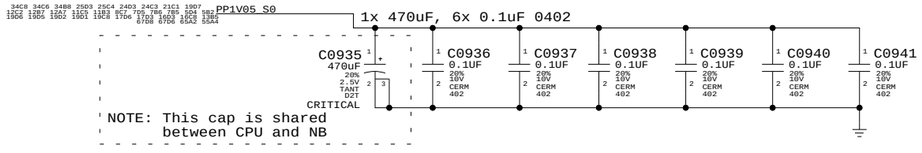
Resistors to allow for override of CPU VID
Will probably be removed before production



VCCA (CPU AVdd) Decoupling



VCCP (CPU I/O) Decoupling



CPU Decoupling & VID

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	9	87

CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

67C3 67B3 67A3 66B6 66B5 66B1 65D6 65B3
54B5 26B8 26B6 26B4 25D8 25D5 25C6 25C4 25B8
26D1 26B2 26B0 26A4 25D6 25D3 25C5 25C3 25B6
21C3 20B4 20A4 19C7 19C6 17C6 14D6 14C7 5D4 5A4
25B4 25B3 25B2 24C3 24B5 24B3 23D5 23B3 23B1 21D3
23A6 23A4 23A2 22C3 22B5 22B3 21D5 21B3 21B1 20D3
22A6 61D8 61A5 60D4 60C7 58C7 58C4 57B6 54D4
82D5 82C6 82B3 82A4 79D3 79A8 71D2 67C5

PP3V3_S0

C1002 1 0.1UF 10% 16V X5R 402 2

R1006 1 10K 5% 1/16W MF-LF 402 2

R1005 1 10K 5% 1/16W MF-LF 402 2

U1001
TMP401
MSOP
CRITICAL

1 VDD
2 D+
3 D-
4 GND
5
6 ALERT*/THM2*
7 THM*
8 SCLK
9 SDATA

THERM_ALERT_L
THERM_ALERT

SMBUS_SMC_B_S0_SCL
SMBUS_SMC_B_S0_SDA
51B5 49B5 27D3 27D2 27D1
TO

OUT 7C6 CPU_THERMD_P

R1001 499 1% 1/16W MF-LF 402

THRM_CPU_DX_P
THRM_CPU_DX_N

(TO CPU INTERNAL THERMAL DIODE)
(TC0D)

C1001 1 0.001UF 10% 50V CERM 402 2

R1002 499 1% 1/16W MF-LF 402

IN 7C6 CPU_THERMD_N

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

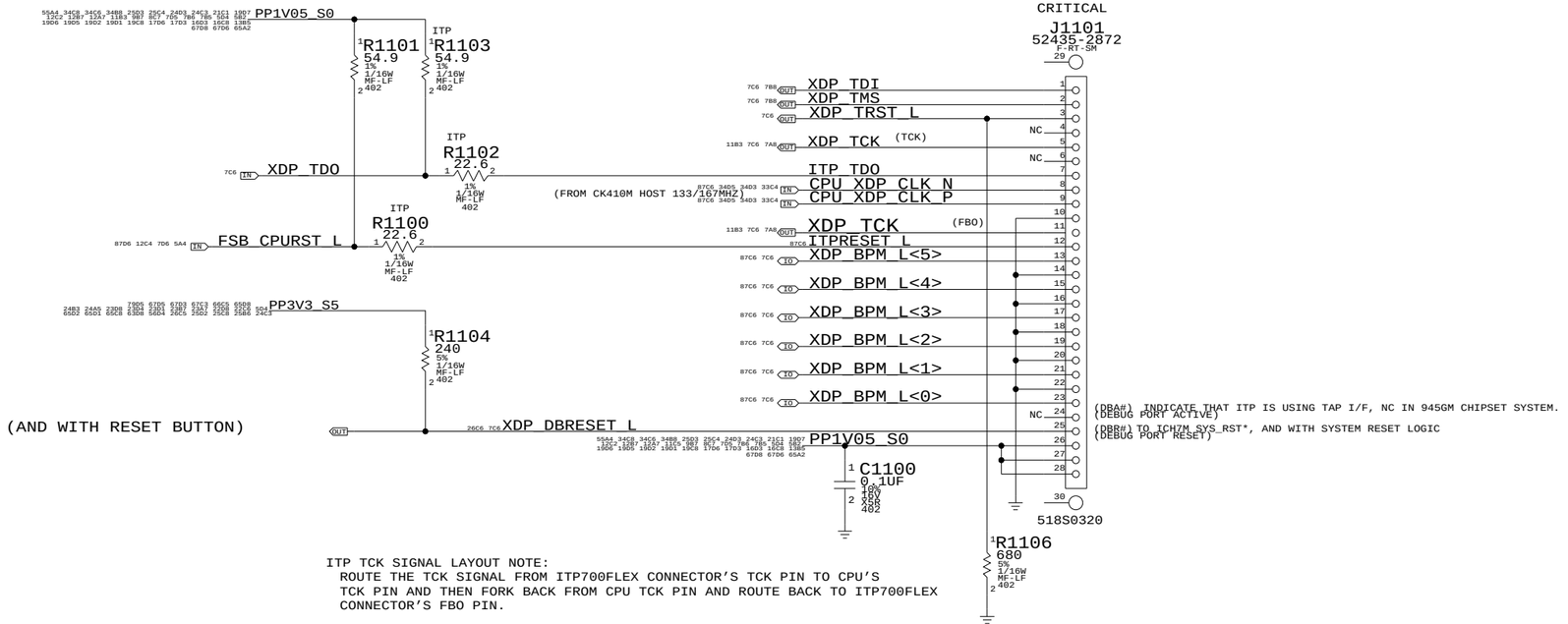
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	10	87

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

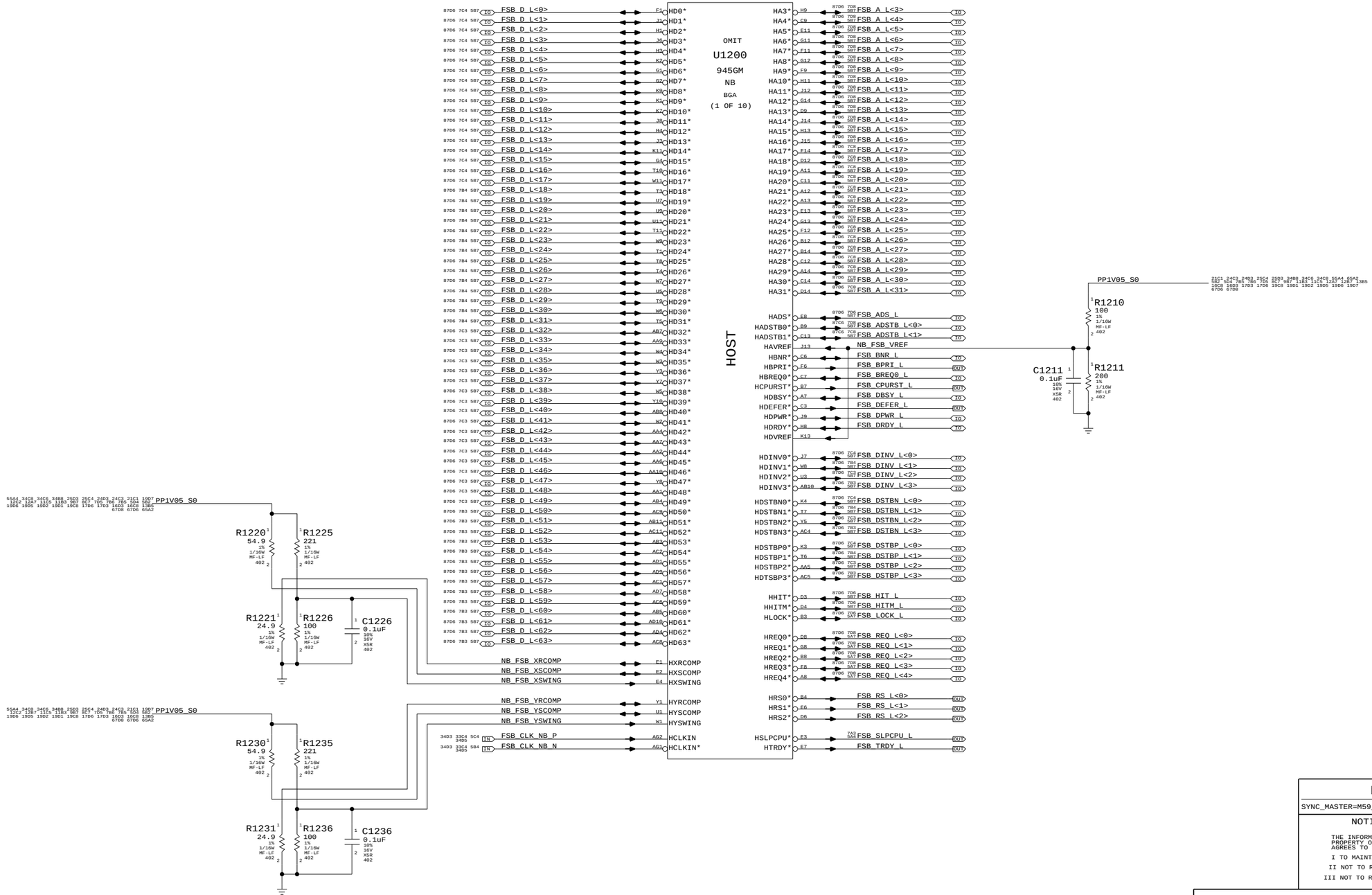
CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	11	87



NB CPU Interface

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	12	87

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

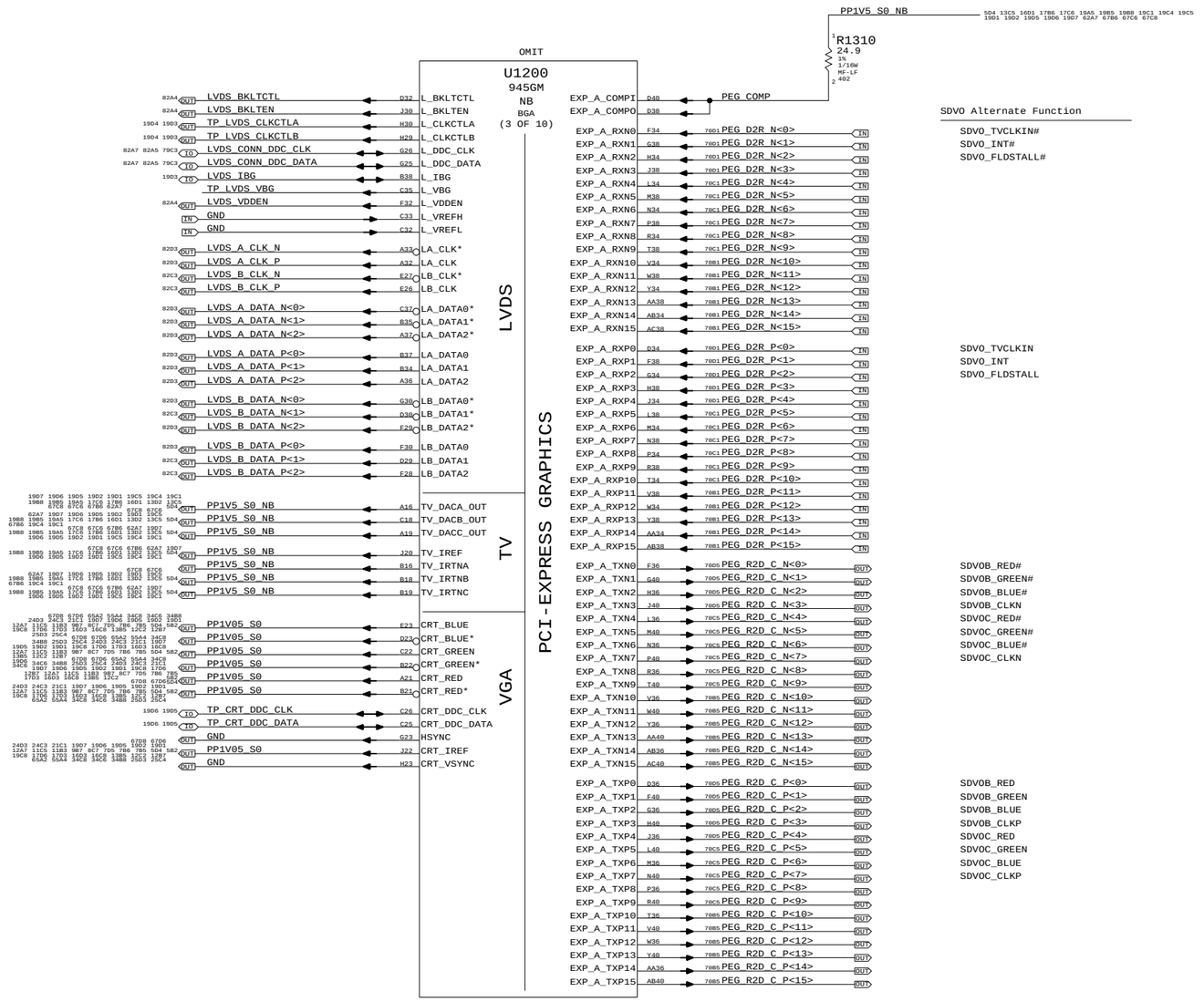
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



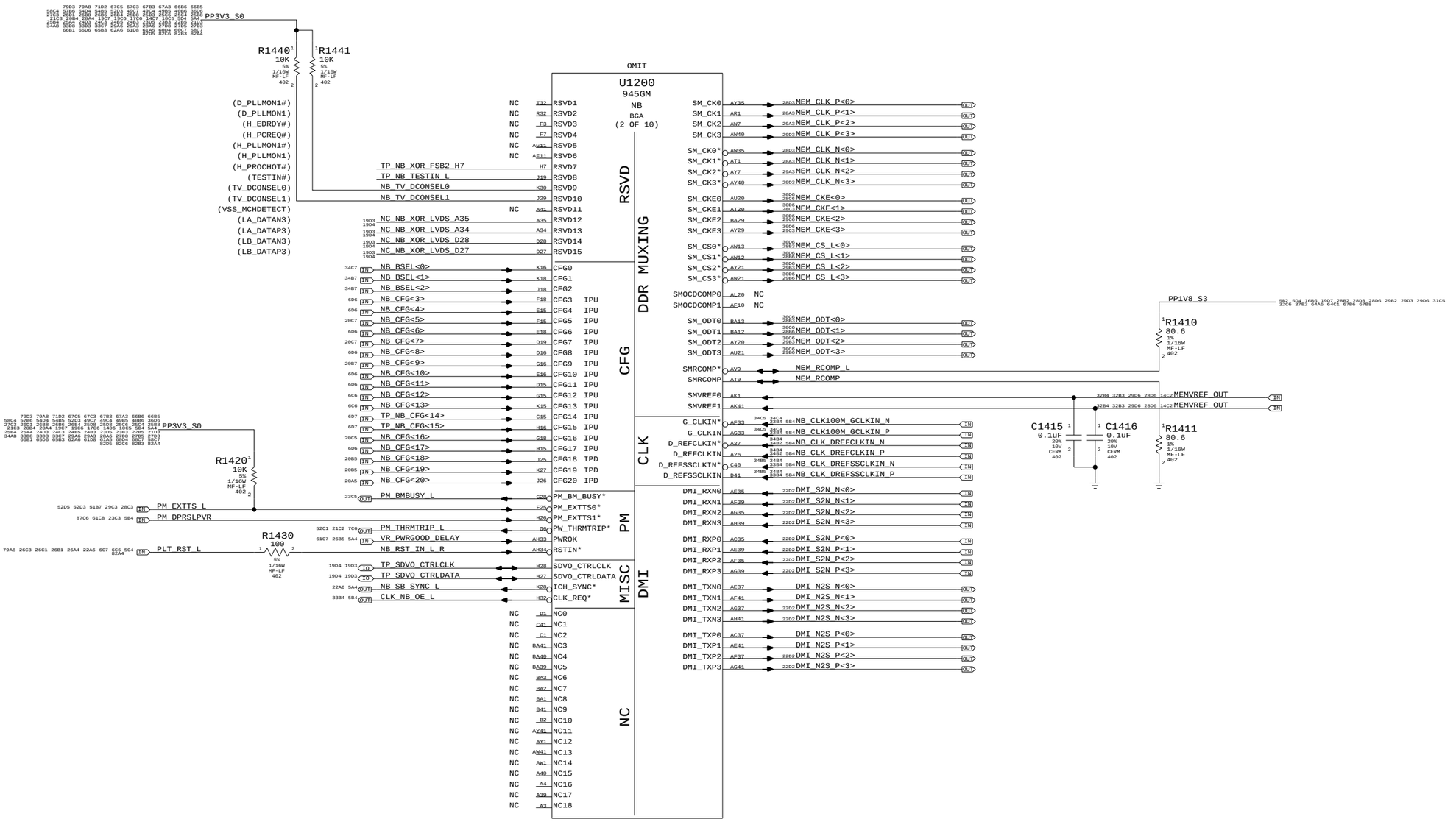
NB PEG / Video Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	13	87



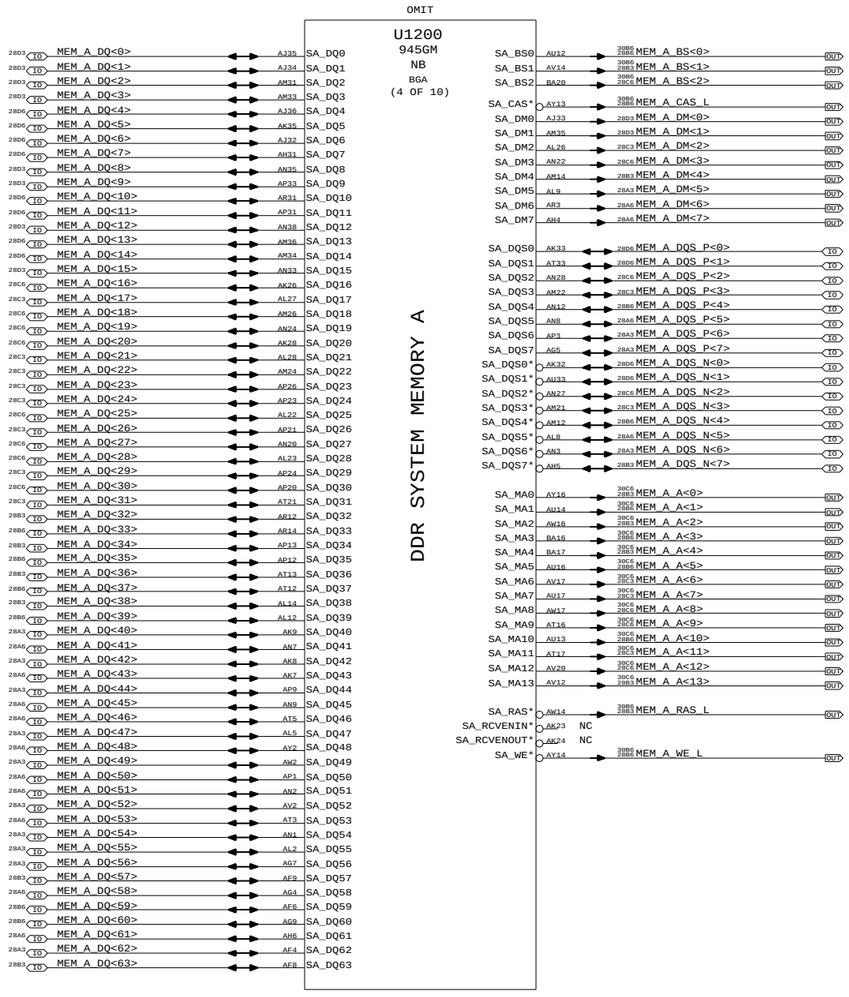
NB Misc Interfaces

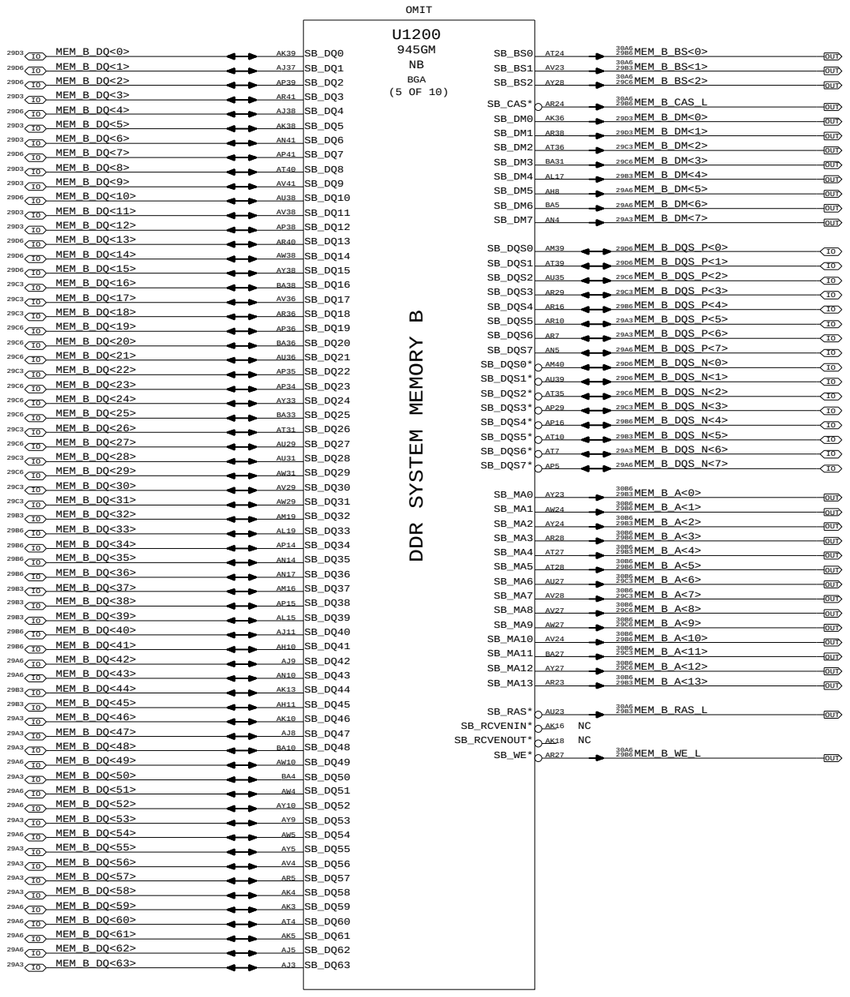
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT 14 OF 87





NB DDR2 Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	15	87

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

PP1V05_S0

OMIT

U1200
945GM
NB
BGA
(7 OF 10)
NCTF

VCC_NCTF0 AD27
VCC_NCTF1 AC27
VCC_NCTF2 AB27
VCC_NCTF3 AA27
VCC_NCTF4 Y27
VCC_NCTF5 W27
VCC_NCTF6 V27
VCC_NCTF7 U27
VCC_NCTF8 T27
VCC_NCTF9 R27
VCC_NCTF10 AD26
VCC_NCTF11 AC26
VCC_NCTF12 AB26
VCC_NCTF13 AA26
VCC_NCTF14 Y26
VCC_NCTF15 W26
VCC_NCTF16 V26
VCC_NCTF17 U26
VCC_NCTF18 T26
VCC_NCTF19 R26
VCC_NCTF20 AD25
VCC_NCTF21 AC25
VCC_NCTF22 AB25
VCC_NCTF23 AA25
VCC_NCTF24 Y25
VCC_NCTF25 W25
VCC_NCTF26 V25
VCC_NCTF27 U25
VCC_NCTF28 T25
VCC_NCTF29 R25
VCC_NCTF30 AD24
VCC_NCTF31 AC24
VCC_NCTF32 AB24
VCC_NCTF33 AA24
VCC_NCTF34 Y24
VCC_NCTF35 W24
VCC_NCTF36 V24
VCC_NCTF37 U24
VCC_NCTF38 T24
VCC_NCTF39 R24
VCC_NCTF40 AD23
VCC_NCTF41 U23
VCC_NCTF42 T23
VCC_NCTF43 R23
VCC_NCTF44 AD22
VCC_NCTF45 V22
VCC_NCTF46 U22
VCC_NCTF47 T22
VCC_NCTF48 R22
VCC_NCTF49 AD21
VCC_NCTF50 V21
VCC_NCTF51 U21
VCC_NCTF52 T21
VCC_NCTF53 R21
VCC_NCTF54 AD20
VCC_NCTF55 V20
VCC_NCTF56 U20
VCC_NCTF57 T20
VCC_NCTF58 R20
VCC_NCTF59 AD19
VCC_NCTF60 V19
VCC_NCTF61 U19
VCC_NCTF62 T19
VCC_NCTF63 AD18
VCC_NCTF64 AC18
VCC_NCTF65 AB18
VCC_NCTF66 AA18
VCC_NCTF67 Y18
VCC_NCTF68 W18
VCC_NCTF69 V18
VCC_NCTF70 U18
VCC_NCTF71 T18
VCC_NCTF72

VSS_NCTF0 AE27
VSS_NCTF1 AE26
VSS_NCTF2 AE25
VSS_NCTF3 AE24
VSS_NCTF4 AE23
VSS_NCTF5 AE22
VSS_NCTF6 AE21
VSS_NCTF7 AE20
VSS_NCTF8 AE19
VSS_NCTF9 AE18
VSS_NCTF10 AC17
VSS_NCTF11 Y17
VSS_NCTF12 U17

PP1V5_S0_NB

VCCAUX_NCTF0 AG27
VCCAUX_NCTF1 AF27
VCCAUX_NCTF2 AG26
VCCAUX_NCTF3 AF26
VCCAUX_NCTF4 AG25
VCCAUX_NCTF5 AF25
VCCAUX_NCTF6 AG24
VCCAUX_NCTF7 AF24
VCCAUX_NCTF8 AG23
VCCAUX_NCTF9 AF23
VCCAUX_NCTF10 AG22
VCCAUX_NCTF11 AF22
VCCAUX_NCTF12 AG21
VCCAUX_NCTF13 AF21
VCCAUX_NCTF14 AG20
VCCAUX_NCTF15 AF20
VCCAUX_NCTF16 AG19
VCCAUX_NCTF17 AF19
VCCAUX_NCTF18 R19
VCCAUX_NCTF19 AG18
VCCAUX_NCTF20 AF18
VCCAUX_NCTF21 R18
VCCAUX_NCTF22 AG17
VCCAUX_NCTF23 AF17
VCCAUX_NCTF24 AE17
VCCAUX_NCTF25 AD17
VCCAUX_NCTF26 AB17
VCCAUX_NCTF27 AA17
VCCAUX_NCTF28 W17
VCCAUX_NCTF29 V17
VCCAUX_NCTF30 T17
VCCAUX_NCTF31 R17
VCCAUX_NCTF32 AG16
VCCAUX_NCTF33 AF16
VCCAUX_NCTF34 AE16
VCCAUX_NCTF35 AD16
VCCAUX_NCTF36 AC16
VCCAUX_NCTF37 AB16
VCCAUX_NCTF38 AA16
VCCAUX_NCTF39 Y16
VCCAUX_NCTF40 W16
VCCAUX_NCTF41 V16
VCCAUX_NCTF42 U16
VCCAUX_NCTF43 T16
VCCAUX_NCTF44 R16
VCCAUX_NCTF45 AG15
VCCAUX_NCTF46 AF15
VCCAUX_NCTF47 AE15
VCCAUX_NCTF48 AD15
VCCAUX_NCTF49 AC15
VCCAUX_NCTF50 AB15
VCCAUX_NCTF51 AA15
VCCAUX_NCTF52 Y15
VCCAUX_NCTF53 W15
VCCAUX_NCTF54 V15
VCCAUX_NCTF55 U15
VCCAUX_NCTF56 T15
VCCAUX_NCTF57 R15

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.05V, Internal Graphics: 5500mA Max

PP1V05_S0
1.05V or 1.5V

U1200
945GM
NB
BGA
(6 OF 10)
VCC

OMIT

VCC_0 AA33
VCC_1 AK3
VCC_2 P33
VCC_3 K33
VCC_4 L33
VCC_5 J33
VCC_6 AA32
VCC_7 Y32
VCC_8 W32
VCC_9 V32
VCC_10 P32
VCC_11 N32
VCC_12 M32
VCC_13 L32
VCC_14 J32
VCC_15 AA31
VCC_16 W31
VCC_17 V31
VCC_18 T31
VCC_19 R31
VCC_20 P31
VCC_21 N31
VCC_22 M31
VCC_23 AA30
VCC_24 V30
VCC_25 W30
VCC_26 V30
VCC_27 U30
VCC_28 T30
VCC_29 R30
VCC_30 P30
VCC_31 N30
VCC_32 L30
VCC_33 AA29
VCC_34 V29
VCC_35 W29
VCC_36 V29
VCC_37 U29
VCC_38 T29
VCC_39 P29
VCC_40 M29
VCC_41 L29
VCC_42 AB28
VCC_43 AA28
VCC_44 V28
VCC_45 U28
VCC_46 T28
VCC_47 R28
VCC_48 P28
VCC_49 N28
VCC_50 M28
VCC_51 L28
VCC_52 P27
VCC_53 L27
VCC_54 M27
VCC_55 N27
VCC_56 P26
VCC_57 L27
VCC_58 N26
VCC_59 M26
VCC_60 L26
VCC_61 M25
VCC_62 L25
VCC_63 P24
VCC_64 N24
VCC_65 M24
VCC_66 AB23
VCC_67 AA23
VCC_68 Y23
VCC_69 P23
VCC_70 N23
VCC_71 M23
VCC_72 L23
VCC_73 AC22
VCC_74 AB22
VCC_75 AA22
VCC_76 Y22
VCC_77 W22
VCC_78 P22
VCC_79 N22
VCC_80 M22
VCC_81 L22
VCC_82 AC21
VCC_83 AA21
VCC_84 W21
VCC_85 N21
VCC_86 M21
VCC_87 L21
VCC_88 AC20
VCC_89 AB20
VCC_90 W20
VCC_91 P20
VCC_92 N20
VCC_93 M20
VCC_94 L20
VCC_95 AB19
VCC_96 AA19
VCC_97 Y19
VCC_98 N19
VCC_99 M19
VCC_100 L19
VCC_101 R18
VCC_102 N18
VCC_103 L18
VCC_104 P17
VCC_105 N17
VCC_106 M17
VCC_107 N16
VCC_108 M16
VCC_109 L16
VCC_110

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

SM_CK_0 AU41
SM_CK_1 AT41
SM_CK_2 AM41
SM_CK_3 AU40
SM_CK_4 BA34
SM_CK_5 AT34
SM_CK_6 AW34
SM_CK_7 AV34
SM_CK_8 AU34
SM_CK_9 AT34
SM_CK_10 AR34
SM_CK_11 BA30
SM_CK_12 AY30
SM_CK_13 AW30
SM_CK_14 AV30
SM_CK_15 AU30
SM_CK_16 AT30
SM_CK_17 AR30
SM_CK_18 AP30
SM_CK_19 AN30
SM_CK_20 AM30
SM_CK_21 AM29
SM_CK_22 AL29
SM_CK_23 AK29
SM_CK_24 AJ29
SM_CK_25 AH29
SM_CK_26 AJ28
SM_CK_27 AH28
SM_CK_28 AJ27
SM_CK_29 AH27
SM_CK_30 BA26
SM_CK_31 AY26
SM_CK_32 AW26
SM_CK_33 AV26
SM_CK_34 AU26
SM_CK_35 AT26
SM_CK_36 AR26
SM_CK_37 AJ26
SM_CK_38 AH26
SM_CK_39 AJ25
SM_CK_40 AH25
SM_CK_41 AJ24
SM_CK_42 AH24
SM_CK_43 BA23
SM_CK_44 AJ23
SM_CK_45 BA22
SM_CK_46 AY22
SM_CK_47 AM22
SM_CK_48 AV22
SM_CK_49 AU22
SM_CK_50 AT22
SM_CK_51 AR22
SM_CK_52 AP22
SM_CK_53 AK22
SM_CK_54 AJ22
SM_CK_55 AK21
SM_CK_56 AK20
SM_CK_57 BA19
SM_CK_58 AY19
SM_CK_59 AW19
SM_CK_60 AV19
SM_CK_61 AU19
SM_CK_62 AT19
SM_CK_63 AR19
SM_CK_64 AP19
SM_CK_65 AK19
SM_CK_66 AJ19
SM_CK_67 AH17
SM_CK_68 AJ16
SM_CK_69 AH16
SM_CK_70 BA15
SM_CK_71 AY15
SM_CK_72 AM15
SM_CK_73 AV15
SM_CK_74 AU15
SM_CK_75 AT15
SM_CK_76 AR15
SM_CK_77 AJ15
SM_CK_78 AK15
SM_CK_79 AJ14
SM_CK_80 AJ13
SM_CK_81 AH13
SM_CK_82 AK12
SM_CK_83 AJ12
SM_CK_84 AH12
SM_CK_85 AG12
SM_CK_86 AK11
SM_CK_87 AJ11
SM_CK_88 BA9
SM_CK_89 AY9
SM_CK_90 AW9
SM_CK_91 AV9
SM_CK_92 AT9
SM_CK_93 AR9
SM_CK_94 AP9
SM_CK_95 BA6
SM_CK_96 AY6
SM_CK_97 AV6
SM_CK_98 AU6
SM_CK_99 AT6
SM_CK_100 AR6
SM_CK_101 AJ6
SM_CK_102 AH6
SM_CK_103 AG6
SM_CK_104 AJ5
SM_CK_105 AV1
SM_CK_106 AU1
SM_CK_107 A31

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47UF 10% 6.3V CERM-X5R 402
C1613 0.47UF 10% 6.3V CERM-X5R 402

C1615 0.47UF 10% 6.3V CERM-X5R 402
Layout Note: Place near pin BA23

PP1V8_S3

C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
Layout Note: Place in cavity

C1610 0.47UF 10% 6.3V CERM-X5R 402
Layout Note: Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 0.47UF 10% 6.3V CERM-X5R 402
C1611 0.47UF 10% 6.3V CERM-X5R 402

NB Power 1

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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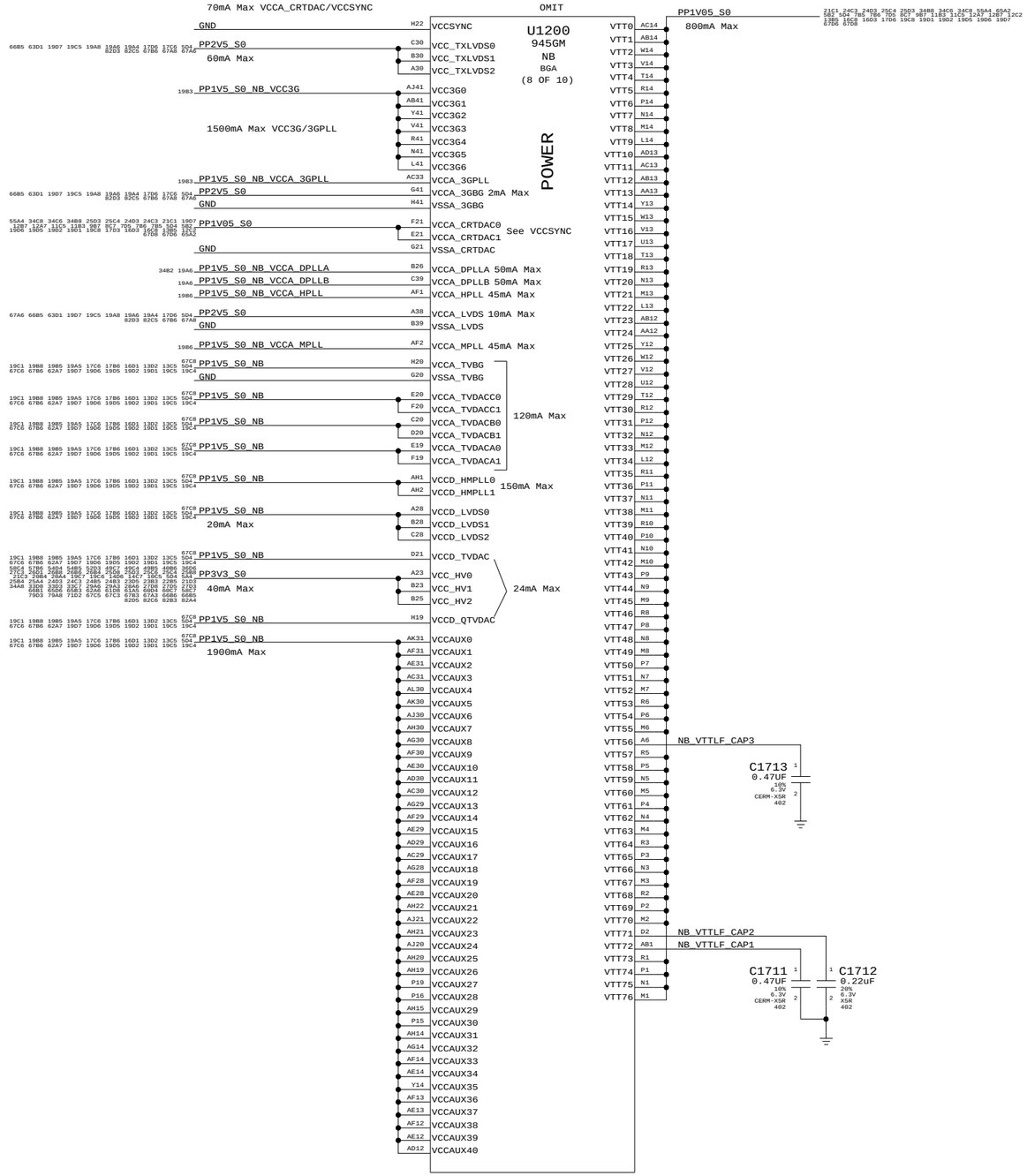
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT 16 OF 87



NB Power 2

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	17	87

OMIT

U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	18	87

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?
3674mA Max
3200mA Max
132mA Max
40mA Max?

PP1V05_S0 IN — 1500mA Max
PP1V05_S0 IN — 10mA Max?
PP1V05_S0 IN — 800mA Max
PP1V05_S0 IN — 7mA Max
PP1V5_S0_NB IN — 7mA Max
PP1V5_S0_NB IN — 1500mA Max
PP1V5_S0_NB IN — 7mA Max
PP1V5_S0_NB IN — 100mA Max
PP1V5_S0_NB IN — 24mA Max
PP1V5_S0_NB IN — 150mA Max
PP1V5_S0_NB IN — 190mA Max
PP1V8_S3 IN — 3200mA Max
GND IN — 70mA Max
PP2V5_S0 IN — 60mA Max
PP2V5_S0 IN — 2mA Max
PP3V3_S0 IN — 7mA Max
PP3V3_S0 IN — 40mA Max

PP1V05_S0 → PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, GND, GND

PP1V5_S0_NB → PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB, PP1V5_S0_NB

TP_CRT_DDC_CLK — MAKE_BASE=TRUE → TP_CRT_DDC_CLK
TP_CRT_DDC_DATA — MAKE_BASE=TRUE → TP_CRT_DDC_DATA

TP_LVDS_CLKCTLA — MAKE_BASE=TRUE → TP_LVDS_CLKCTLA
TP_LVDS_CLKCTLB — MAKE_BASE=TRUE → TP_LVDS_CLKCTLB
NC_NB_XOR_LVDS_A34 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_A34
NC_NB_XOR_LVDS_A35 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_A35
NC_NB_XOR_LVDS_D27 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_D27
NC_NB_XOR_LVDS_D28 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_D28
TP_SDVO_CTRLCLK — MAKE_BASE=TRUE → TP_SDVO_CTRLCLK
TP_SDVO_CTRLDATA — MAKE_BASE=TRUE → TP_SDVO_CTRLDATA

LVDS IBG
R1990 1.5K 1% 1/16W MF-LF 402 — GND, GND

PP1V05_S0 → (MCH CRTDAC ANALOG 2.5V PWR) PP1V05_S0; GND
(MCH H/V SYNC 2.5V PWR) GND

PP1V5_S0_NB →
(MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB
(MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB
(MCH TV OUT CHANNEL A 3.3V PWR) PP1V5_S0_NB
(MCH TV OUT CHANNEL B 3.3V PWR) PP1V5_S0_NB
(MCH TV OUT CHANNEL C 3.3V PWR) PP1V5_S0_NB
(MCH TV DAC BAND GAP 3.3V PWR) PP1V5_S0_NB
GND

GMCH CORE PWR 1.05V BYPASS

PP1V05_S0 — 1500mA Max
CRITICAL: C1900 470uF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

MCH VTT BYPASS (MCH FSB 1.05V PWR)

PP1V05_S0 — 800mA Max
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity

MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

PP3V3_S0 — 40mA Max
(SHARE C0940 470UF)
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

PP2V5_S0 — 2mA Max
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402
C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

PP1V5_S0_NB — 1900mA Max
C1918 0.1uF 20% 10V CERM 402

GMCH VCC_HPLL FILTER (HOST PLL 1.5V PWR)

PP1V5_S0_NB — 100mA Max
L1934 FERR-120-OHM-0.2A 0603
C1934 22UF 20% 6.3V CERM 805
C1935 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_HPLL — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 45mA Max

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)

L1936 FERR-120-OHM-0.2A 0603
C1936 22UF 20% 6.3V CERM 805
C1937 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_MPLL — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 45mA Max

GMCH VCCA_DPLLA FILTER (CRT/TVOUT PLL 1.5V PWR)

NO STUFF R1953 0 5% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_DPLLA — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 50MA MAX

GMCH VCCA_DPLLB FILTER (LVDS PLL 1.5V PWR)

CRITICAL: U1900 TPS73115 SOT23-5 (IN, EN, GND, OUT, NR/FB)
PP1V5_S0_NB_DPLL — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V
TPS73115_NR
C1950 1uF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603
C1953 0.1uF 20% 10V CERM 402
C1954 0.1uF 20% 10V CERM 402
NO STUFF R1954 0 5% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_DPLLB — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 50MA MAX

MCH VCC_TXLVDS BYPASS (MCH LVDS TRANSMITTER 2.5V PWR)

PP2V5_S0 — 60MA MAX
C1990 4.7UF 20% 6.3V CERM 603
C1991 0.1uF 20% 10V CERM 402

MCH VCCD_LVDS BYPASS (MCH LVDS DIGITAL 1.5V PWR)

PP1V5_S0_NB — 20MA MAX
C1992 10uF 20% 6.3V X5R 603
C1993 0.1uF 20% 10V CERM 402

MCH VCCA_LVDS BYPASS (MCH LVDS ANALOG 2.5V PWR)

PP2V5_S0 — 10MA MAX
C1994 0.01UF 20% 16V CERM 402
C1995 0.1uF 20% 10V CERM 402
Layout Note: Route to caps, then GND

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)

PP1V5_S0_NB → L1970 91nH 1210 → PP1V5_S0_NB_VCC3G — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V
C1970 220UF 20% 2.5V POLY CASE-B2
Layout Note: Place L and C close to MCH
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)

PP1V5_S0_NB → L1975 1.0UH-220MA-0.12-OHM 0805 → PP1V5_S0_NB_3GPLL_F — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V
R1975 0.51 1% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_3GPLL — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
GND
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

1500mA Max

NB (GM) Decoupling

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 19 OF 87	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

PP3V3_S0
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

PP3V3_S0
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

PP3V3_S0
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

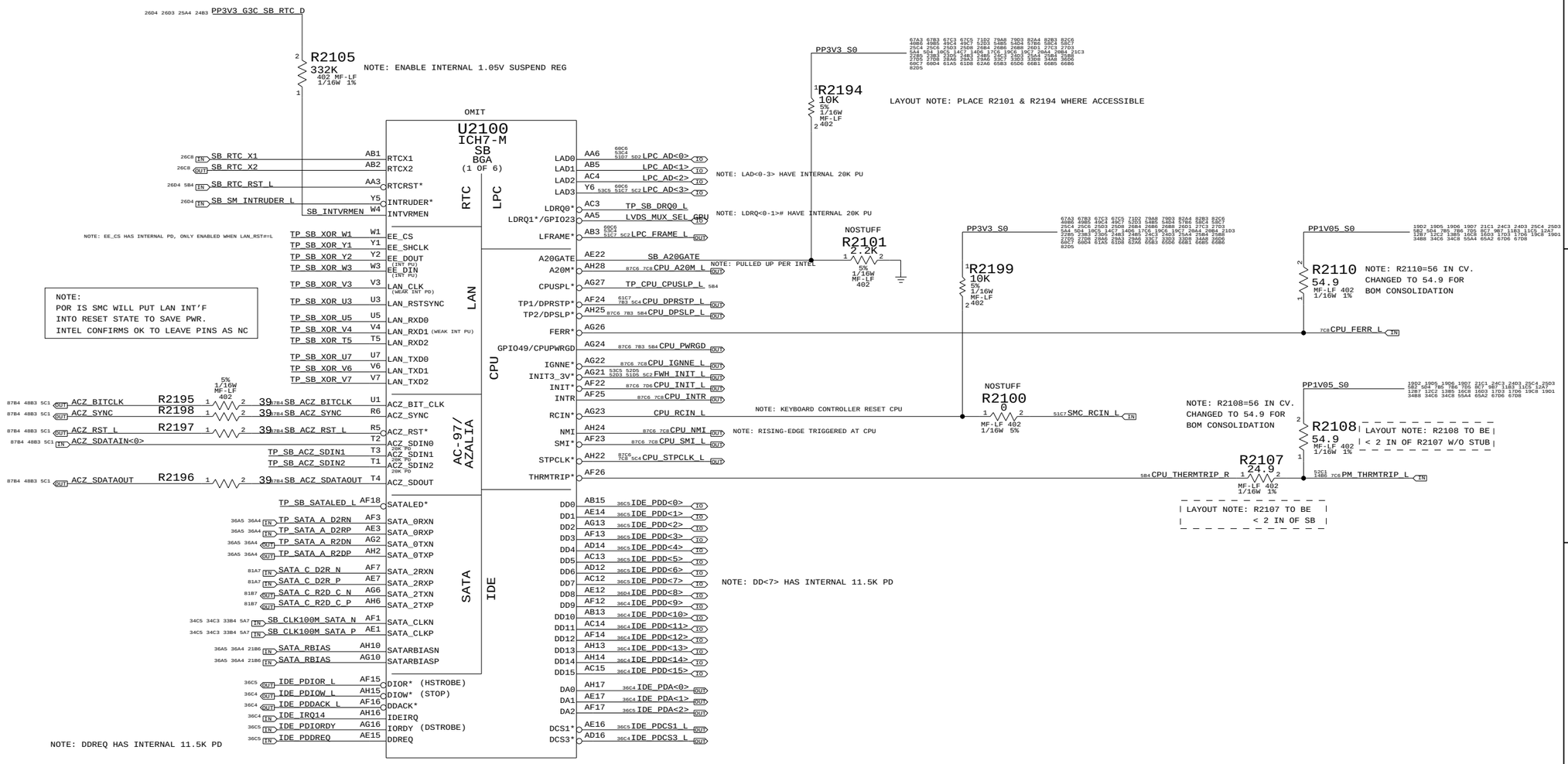
NB Config Straps

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	20	87



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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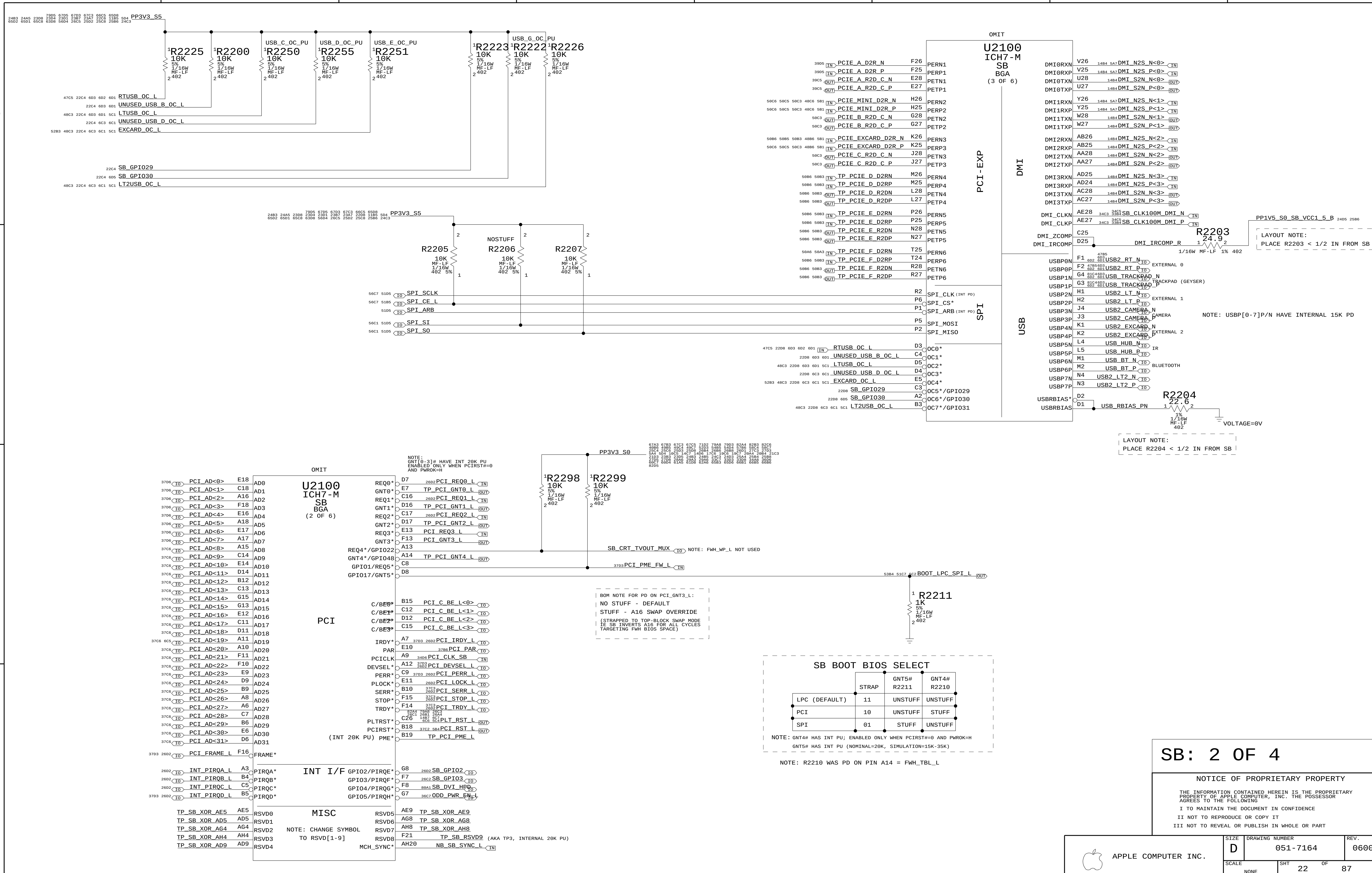
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	21	87



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE — SHT 22 OF 87

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

PP3V3_S0

PP3V3_S5

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMBUS_SB_SCL → SMBCLK C22
SMBUS_SB_SDA → SMBDATA B22
SMB_LINK_ALERT_L → LINKALERT* A26
SMLINK<0> → SMLINK0 B25
SMLINK<1> → SMLINK1 A25
NOT USED
PM_RI_L → RI* A28
SB_SPKR → SPKR (INT WEAK PD) A19
PM_SUS_STAT_L → SUS_STAT* A27
PM_SYSRST_L → SYS_RST* A22
PM_BMBUSY_L → GPIO0/BM_BUSY* AB18
SMB_ALERT_L → GPIO11/SMBALERT* B23
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L → GPIO18/STPPCI* AC20
PM_STPCPU_L → GPIO20/STPCPU* AF21
SB_GPIO26 → GPIO26 A21
BIOS_REC → GPIO27 B21
FWH_MFG_MODE → GPIO28 E23
PM_CLKRUN_L → GPIO32/CLKRUN* AG18
GPU_D3COLD_RESET_L → GPIO33/AZ_DOCK_EN* AC19
TP_AZ_DOCK_RST_L → GPIO34/AZ_DOCK_RST* U2
PCIE_WAKE_L → WAKE* F20
INT_SERIRQ → SERIRQ AH21
PM_THRM_L → THRM* AF20
VR_PWRGD_CK410 → VRMPWRGD AD22
TP_SB_GPIO6 → GPIO6 AC21
GPIO7 AC18
GPIO8 E21

SMBUS
SYS PWR MNGT
GPIO

SATA GPIO
GPIO21/SATA0GP AF19 SB_GPIO21 100 R2302
GPIO19/SATA1GP AH18 SB_GPIO19 100 R2303
GPIO36/SATA2GP AH19
GPIO37/SATA3GP AE19 SB_GPIO37 100 R2305
SATA_C_DET_L

CLKS
CLK14 AC1 SB_CLK14P3M_TIMER
CLK48 B2 SB_CLK48M_USBCTLR
SUSCLK C20 TP_SB_SUS_CLK

SLP_S3* B24 PM_SLP_S3_L
SLP_S4* D23 PM_SLP_S4_L
SLP_S5* F22 PM_SLP_S5_L
PWROK AA4 PM_SB_PWROK
GPIO16/DPRSLPVR AC22 PM_DPRSLPVR
TP0/BATLOW* C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
PWRBTN* (INT 20K PU) C23 PM_PWRBTN_L
LAN_RST* C19 PM_LAN_ENABLE
NOTE:
SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F
IN RESET STATE TO SAVE PWR
RSMRST* Y4

GPIO9 E20 SMS_INT_L
GPIO10 A20 SMC_SB_NMI
DEF=GPI GPIO12 F19 LAN_ENERGY_DET
GPIO13 E19
DEF=GPI GPIO14 R4 IDE_RESET_L
GPIO15 E22 SV_SET_UP
GPIO24 R3 CRB_SV_DET
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 AD21 SB_CLK100M_SATA_OE_L
GPIO36 AD20 SB_GPUVCORE_DISABLE_L
DEF=GPI GPIO39 AE20 SATA_C_PWR_EN_L

GPIO

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

PP3V3_S5
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 1/16W 402 MF-LF 5%
PM_BATLOW_L
PM_RSMRST_L
R2399 100K 5% 1/16W 402 MF-LF
SMC_WAKE_SCI_L

PP3V3_S5
R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%
SV_SET_UP
CRB_SV_DET

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

PP3V3_S0
R2388 10K 5% 1/16W MF-LF 402
SATA_C_PWR_EN_L

PP3V3_S5
R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%
FWH_MFG_MODE
BIOS_REC

SMC_RUNTIME_SCI_L
SMC_EXTSMI_L

SB: 3 OF 4
SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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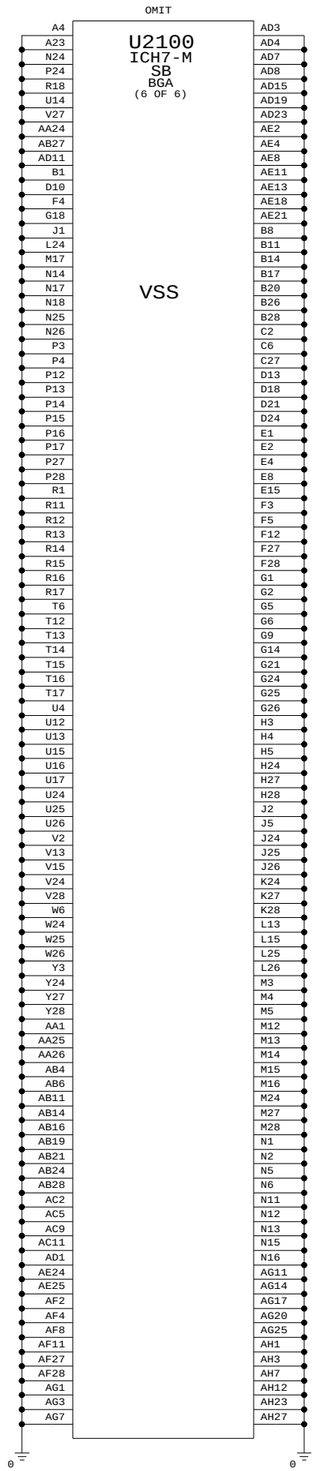
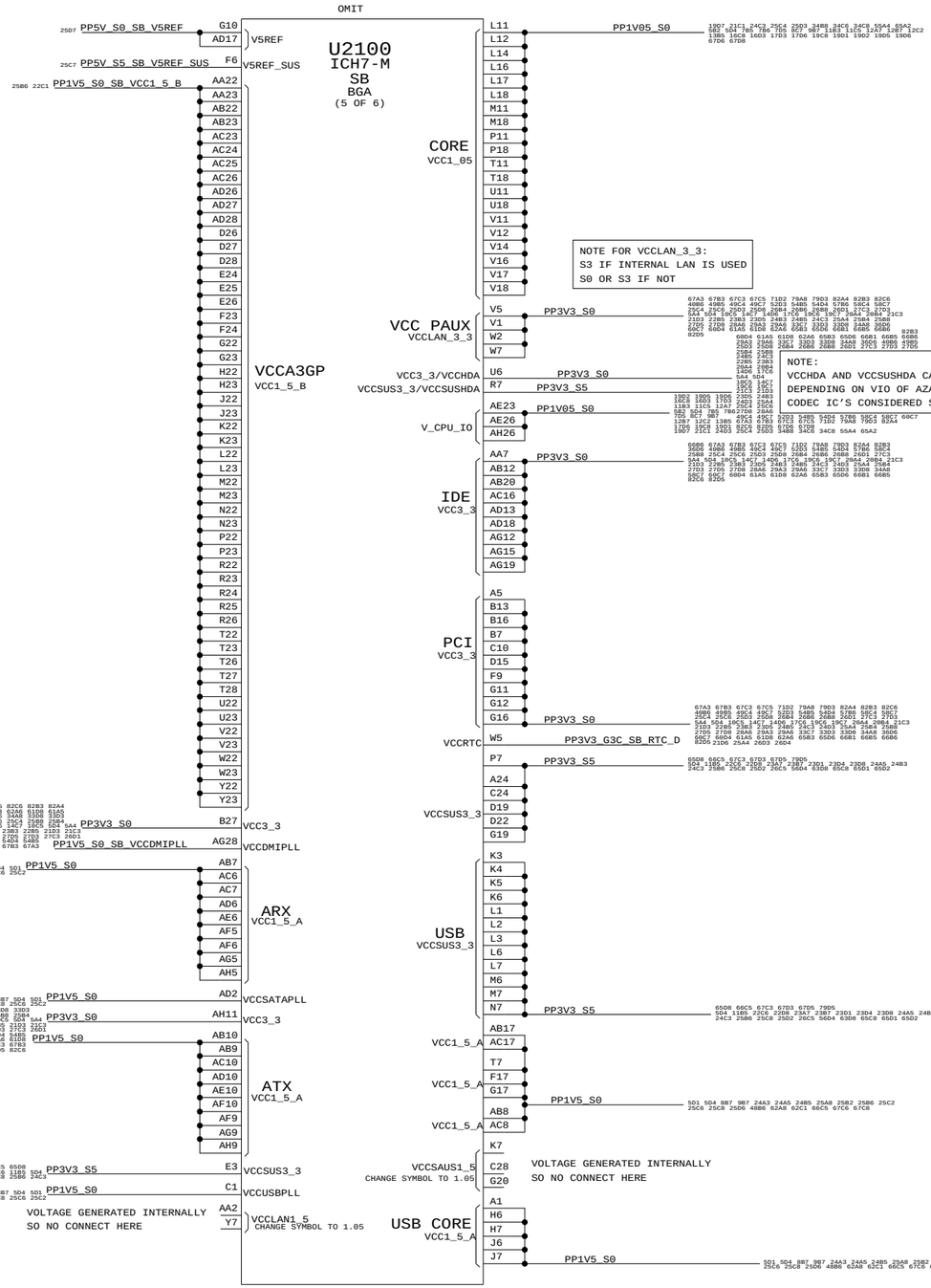
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 23 OF 87	





SB: 4 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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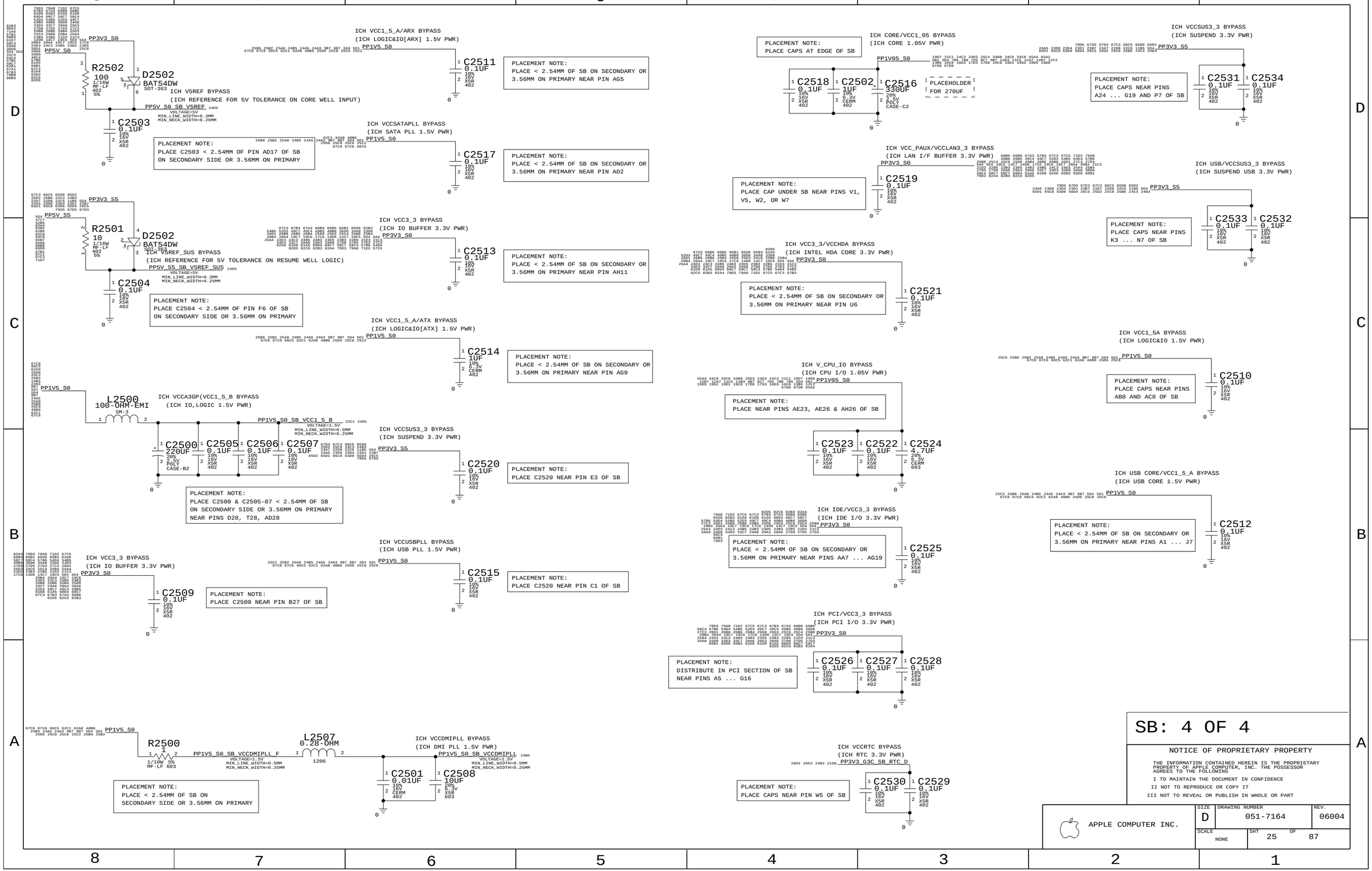
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 24 OF 87	


ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PP1V5_S0
C2511 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG5
PP3V3_S0
R2502 100 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
PP5V_S0
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE C2503 < 2.54MM OF PIN AD17 OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
PP1V5_S0
C2517 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AD2
PP3V3_S5
R2501 10 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE C2504 < 2.54MM OF PIN F6 OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2513 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PP1V5_S0
C2514 1UF 10% 6.3V CERM 402
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG9
PP1V5_S0
L2500 100-OHM-EMI SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500 220UF 20% 2.5V POLY CASE-B2
C2505 0.1UF 10% 16V X5R 402
C2506 0.1UF 10% 16V X5R 402
C2507 0.1UF 10% 16V X5R 402
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
C2520 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE C2520 NEAR PIN E3 OF SB
PLACEMENT NOTE: PLACE C2500 & C2505-07 < 2.54MM OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY NEAR PINS D28, T28, AD28
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
PP1V5_S0
C2515 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE C2520 NEAR PIN C1 OF SB
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2509 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE C2509 NEAR PIN B27 OF SB
PP1V5_S0
R2500 1 1/10W 5% MF-LF 603
L2507 0.28-OHM 1206
PP1V5_S0_SB_VCCDMIPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
C2501 0.01UF 10% 16V CERM 402
C2508 10UF 20% 6.3V X5R 603
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE: PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PP1V05_S0
C2518 0.1UF 10% 16V X5R 402
C2502 1UF 10% 6.3V CERM 402
C2516 330UF 20% 2.5V POLY CASE-C2
PLACEHOLDER FOR 270UF
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
C2531 0.1UF 10% 16V X5R 402
C2534 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE CAPS NEAR PINS A24 ... G19 AND P7 OF SB
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
PP3V3_S0
C2519 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE CAP UNDER SB NEAR PINS V1, V5, W2, OR W7
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PP3V3_S5
C2533 0.1UF 10% 16V X5R 402
C2532 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE CAPS NEAR PINS K3 ... N7 OF SB
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
PP3V3_S0
C2521 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN U6
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
PP1V05_S0
C2523 0.1UF 10% 16V X5R 402
C2522 0.1UF 10% 16V X5R 402
C2524 4.7UF 20% 6.3V CERM 603
PLACEMENT NOTE: PLACE NEAR PINS AE23, AE26 & AH26 OF SB
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
PP1V5_S0
C2510 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE CAPS NEAR PINS AB8 AND AC8 OF SB
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PP1V5_S0
C2512 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS A1 ... J7
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
PP3V3_S0
C2525 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS AA7 ... AG19
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PP3V3_S0
C2526 0.1UF 10% 16V X5R 402
C2527 0.1UF 10% 16V X5R 402
C2528 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: DISTRIBUTE IN PCI SECTION OF SB NEAR PINS A5 ... G16
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PP3V3_G3C_SB_RTC_D
C2530 0.1UF 10% 16V X5R 402
C2529 0.1UF 10% 16V X5R 402
PLACEMENT NOTE: PLACE CAPS NEAR PIN W5 OF SB
SB: 4 OF 4
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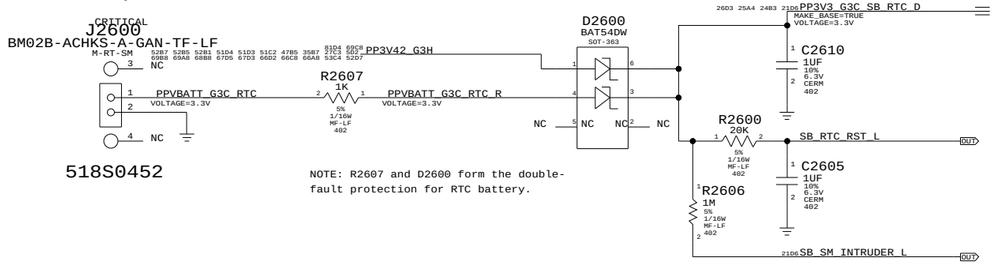
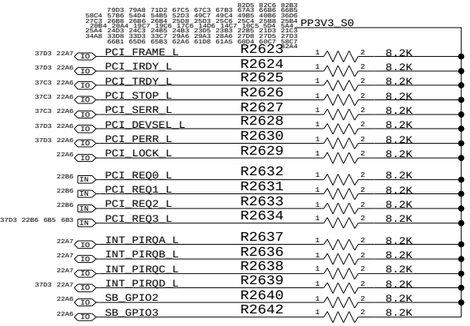
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7164
REV. 06004
SCALE NONE
SHT 25 OF 87

RTC Battery Connector



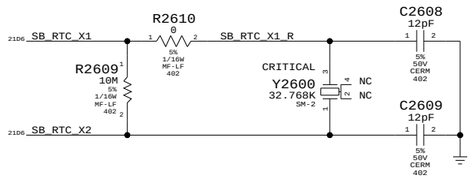
518S0452

NOTE: R2607 and D2600 form the double-fault protection for RTC battery.

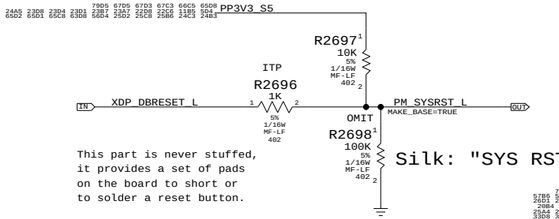


Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit



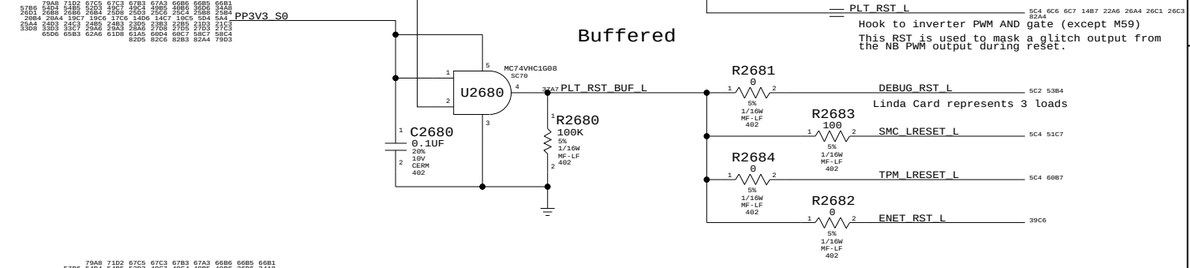
Platform Reset Connections



This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

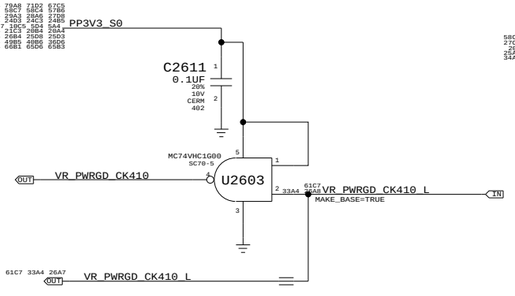
Unbuffered

Buffered



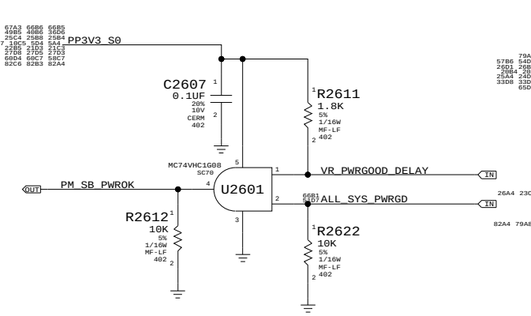
Initial resistor values are based on CRB, but may change after characterization.

VR_PWRGD_CK410_L Inverter

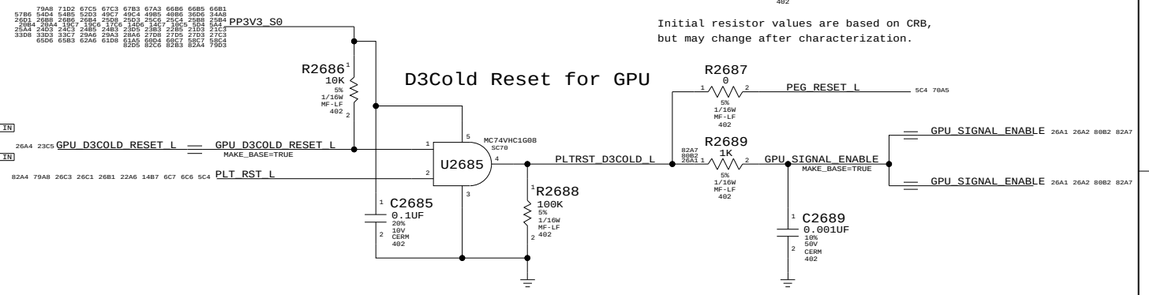


1G00 used as small & cheap inverter

VR_PWRGOOD_DELAY Generation



D3Cold Reset for GPU



SB Misc

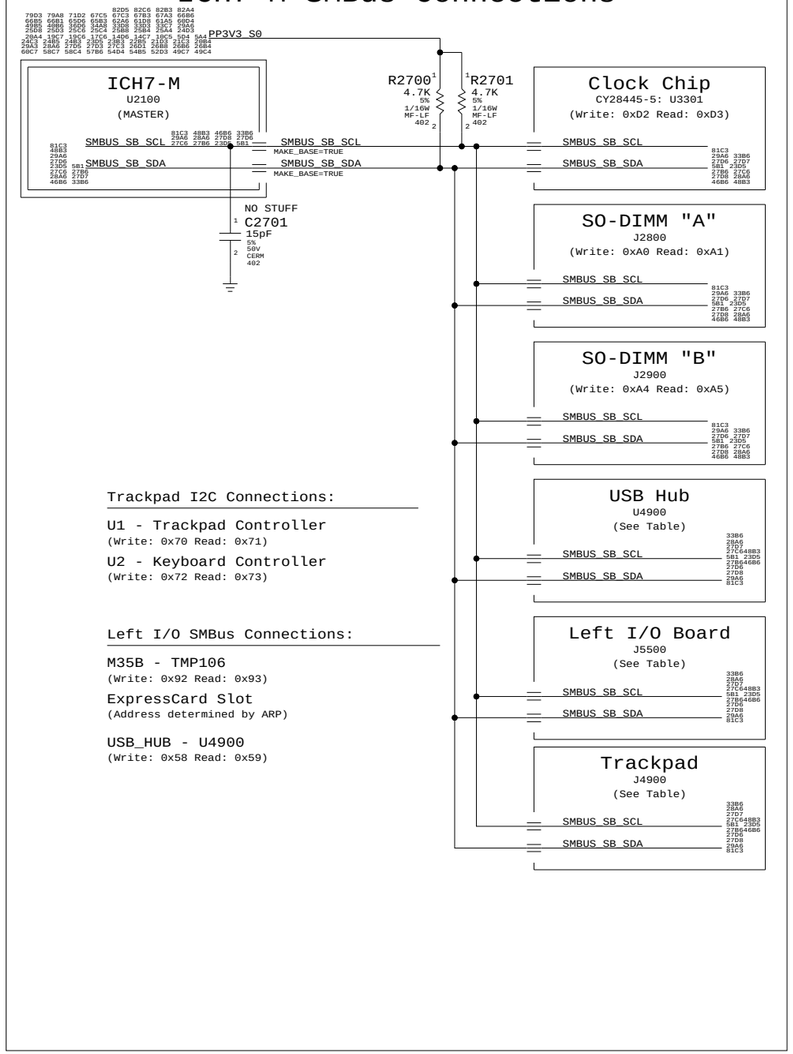
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	26	87

ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

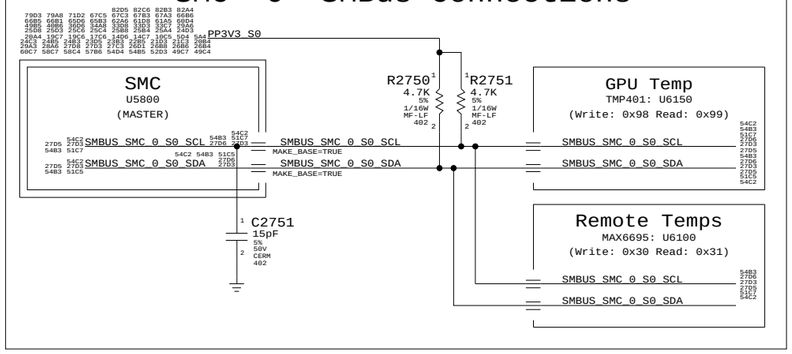
Left I/O SMBus Connections:

M35B - TMP106
(Write: 0x92 Read: 0x93)

ExpressCard Slot
(Address determined by ARP)

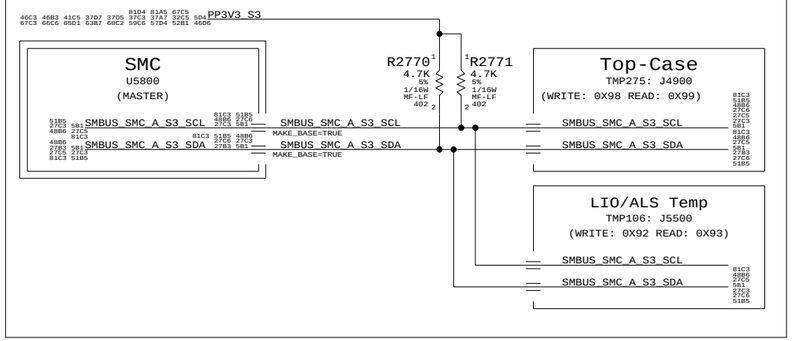
USB_HUB - U4900
(Write: 0x58 Read: 0x59)

SMC "0" SMBus Connections

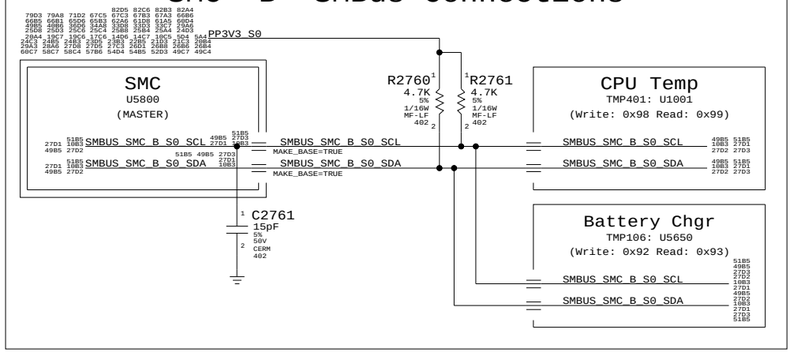


SMC "A" SMBus Connections

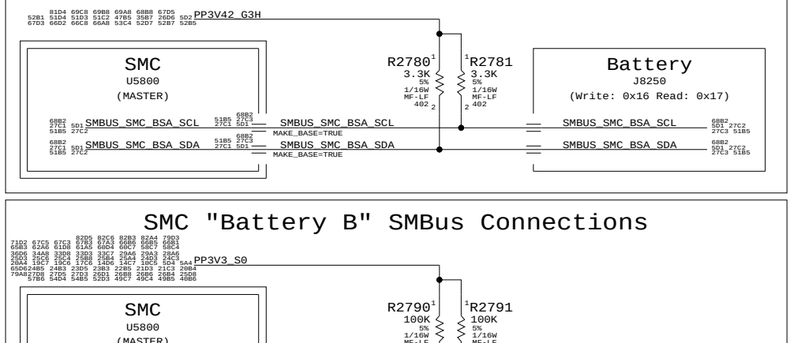
NOTE: SMC RMT bus remains powered and may be active in S3 state



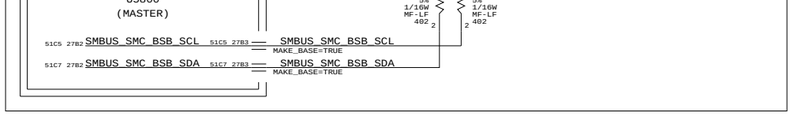
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M57 SMBUS CONNECTIONS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	27	87

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Expansion" (surface-mount) slot

PP1V8_S3

MEMVREF_OUT

C2801 2.2uF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

CRITICAL
J2800
F-RT-SM-M9
DDR2-SODIMM-DUAL

NC

KEY

PP3V3_S0

SMBUS_SB_SDA

SMBUS_SB_SCL

ADDR=0xA0(WR)/0xA1(RD)

516S0471

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C2808 10UF 20% 6.3V XSR 603

C2809 10UF 20% 6.3V XSR 603

C2810 1UF 10% 6.3V CERM 402

C2811 1UF 10% 6.3V CERM 402

C2812 1UF 10% 6.3V CERM 402

C2813 1UF 10% 6.3V CERM 402

C2814 1UF 10% 6.3V CERM 402

C2815 1UF 10% 6.3V CERM 402

C2816 1UF 10% 6.3V CERM 402

C2817 1UF 10% 6.3V CERM 402

C2818 1UF 10% 6.3V CERM 402

C2819 1UF 10% 6.3V CERM 402

C2820 1UF 10% 6.3V CERM 402

C2821 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	28	87

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Factory" (thru-hole) slot

C2901 2.2uF 20% 6.3V CERM1 603

C2900 0.1uF 20% 10V CERM 402

DDR2-SODIMM-DUAL

CRITICAL
J2900
F-RT-TH1

516-0140

SODIMM_A_SA1
ADDR=0xA4(WR)/0xA5(RD)

Resistor prevents pwr-gnd short

DDR2 Bypass Caps
(For return current)

C2908 10UF 20% 5.3V XSR 603
C2909 10UF 20% 5.3V XSR 603
C2910 1UF 10% 6.3V CERM 402
C2911 0.1uF 20% 10V CERM 402
C2912 1UF 10% 6.3V CERM 402
C2913 1UF 10% 6.3V CERM 402
C2914 1UF 10% 6.3V CERM 402
C2915 1UF 10% 6.3V CERM 402
C2916 1UF 10% 6.3V CERM 402
C2917 0.1uF 20% 10V CERM 402
C2918 0.1uF 20% 10V CERM 402
C2919 0.1uF 20% 10V CERM 402
C2920 0.1uF 20% 10V CERM 402
C2921 0.1uF 20% 10V CERM 402

R2900 10K 5% 1/16W MF-LF 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

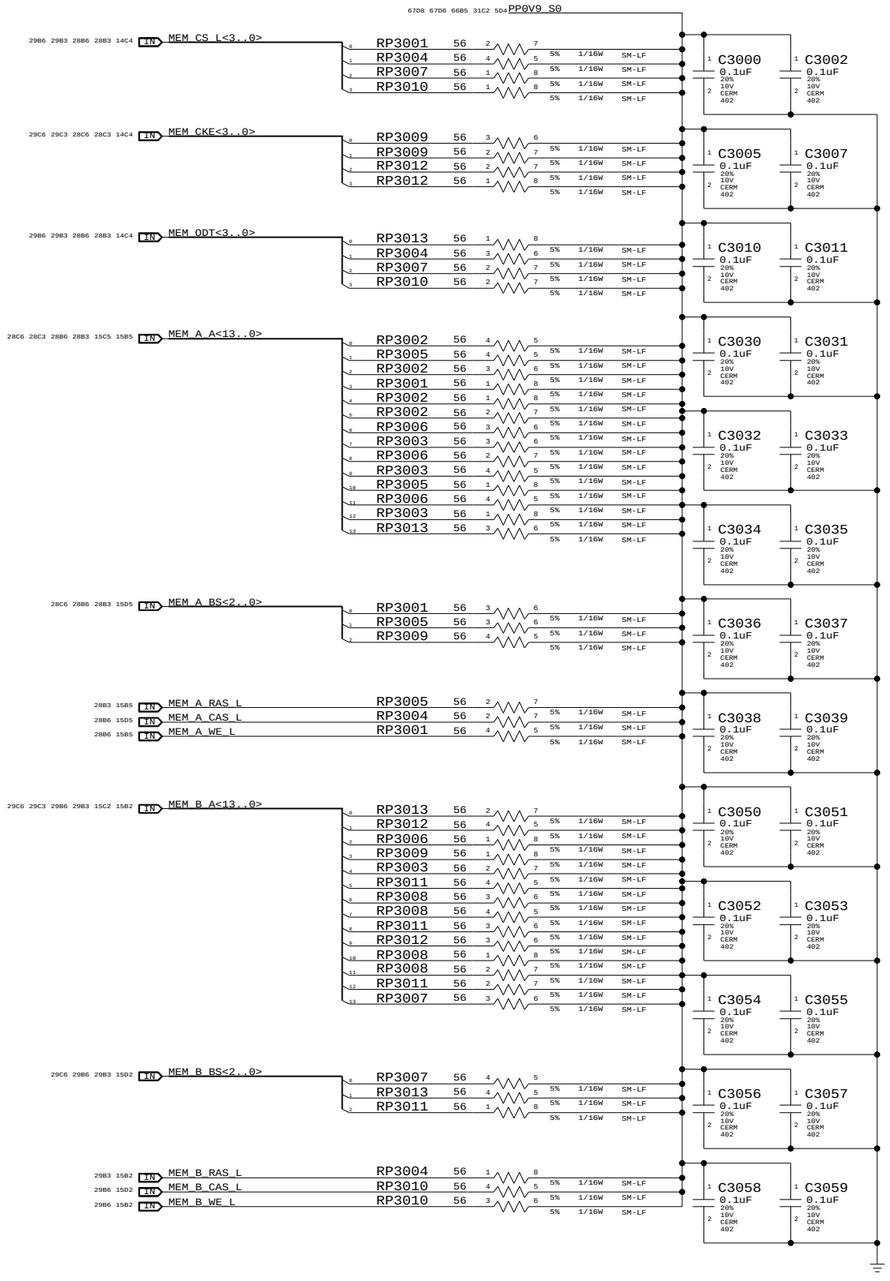
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	29	87

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

SHT 30 OF 87

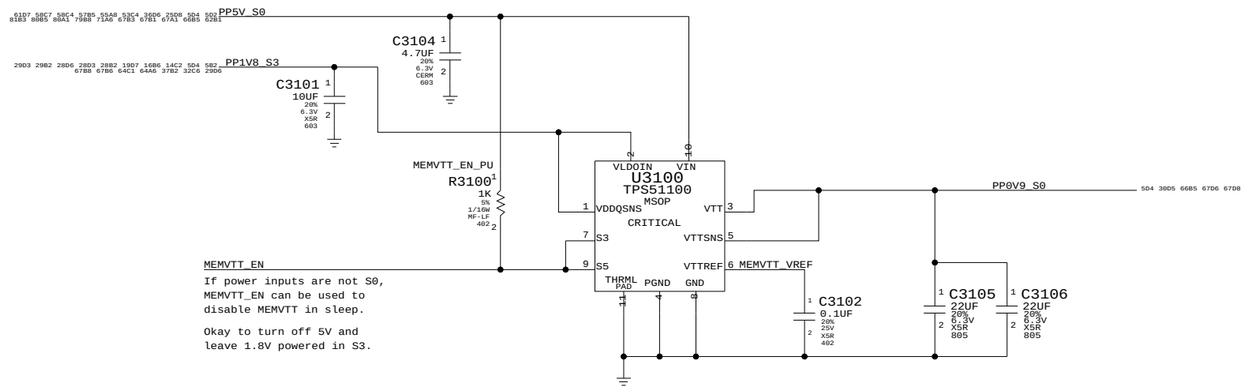
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



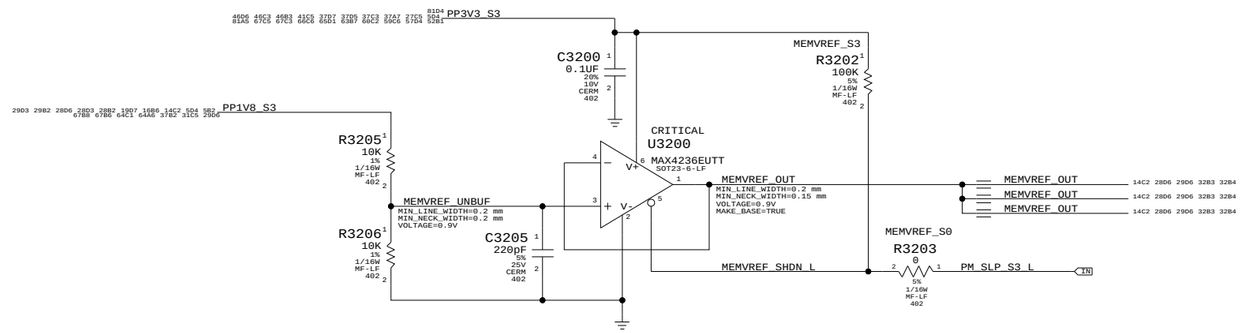
Memory Vtt Supply

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT 31 OF 87



DDR2 VRef

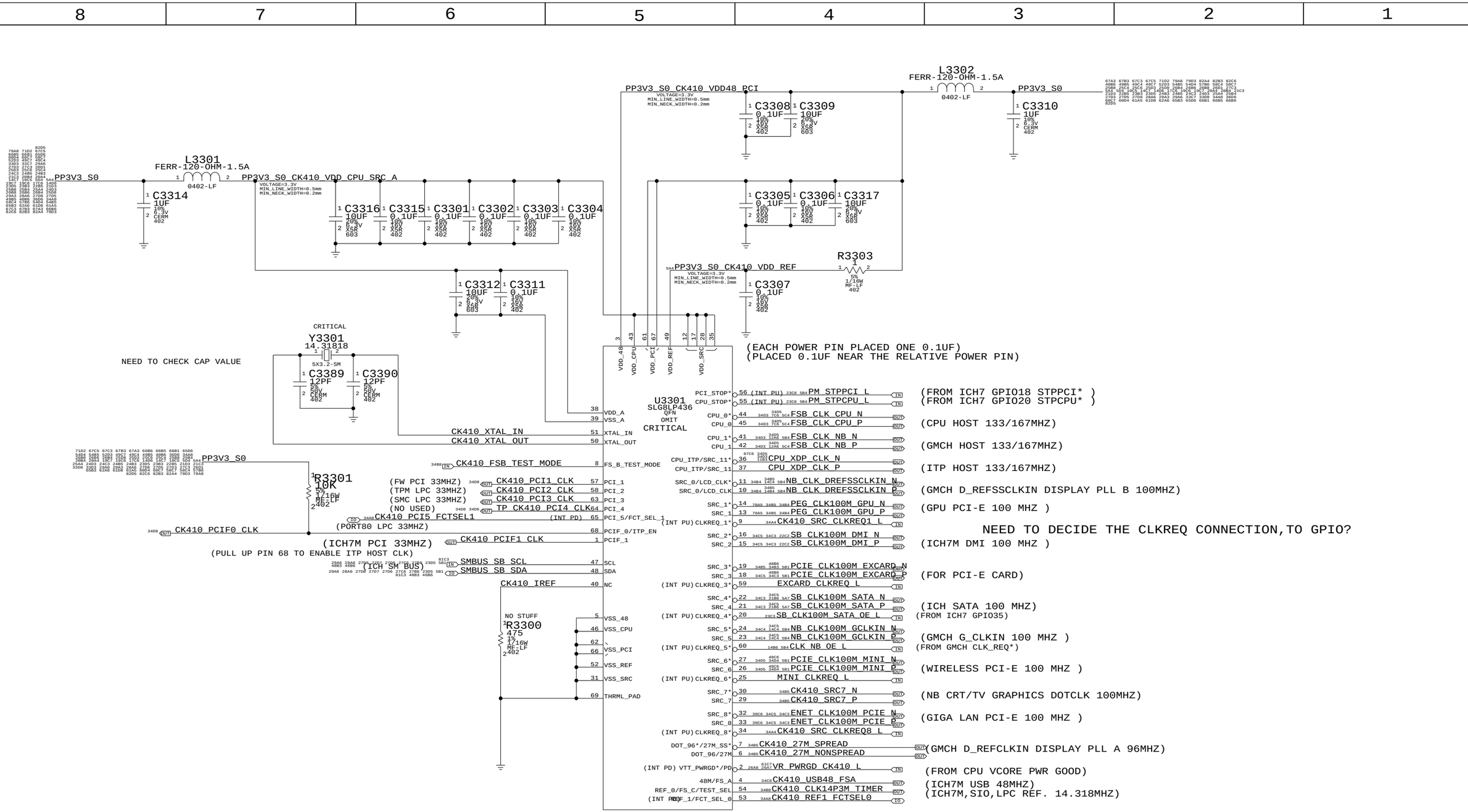
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

SHT 32 OF 87



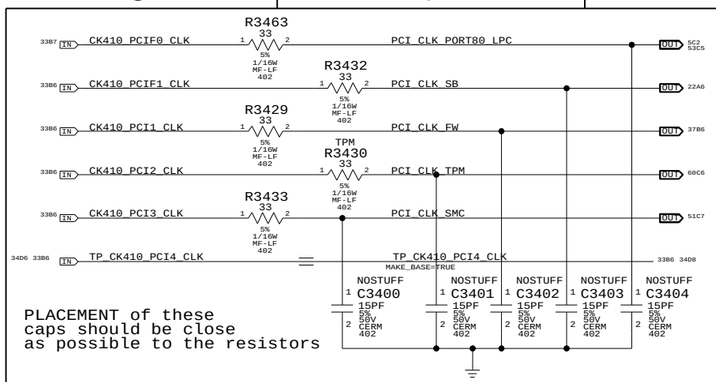
FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

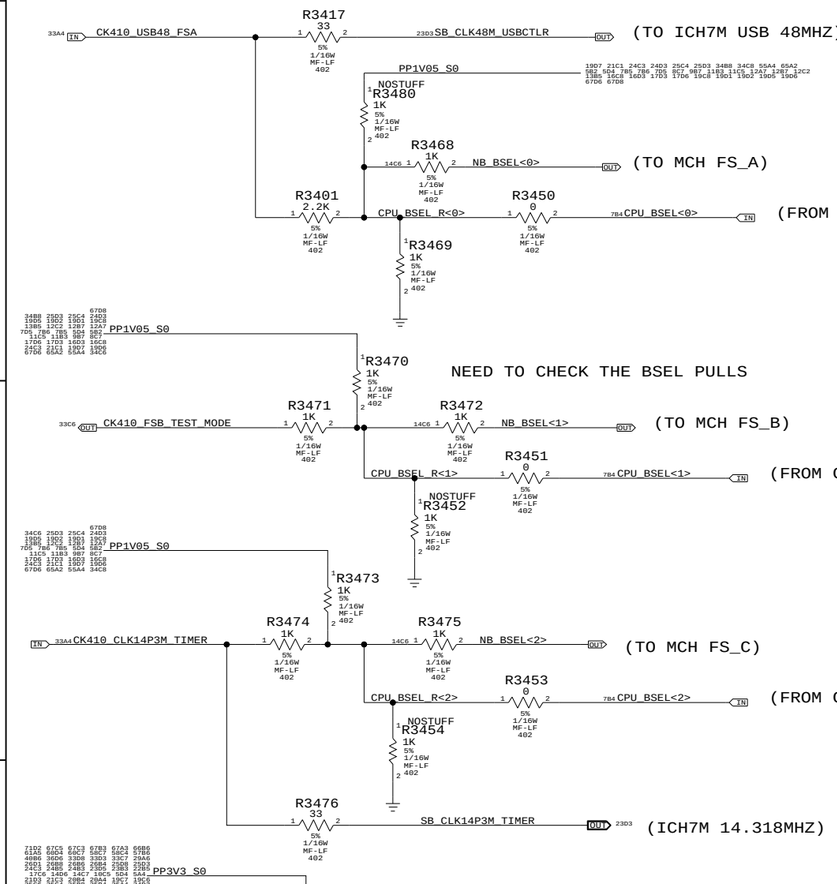
CLOCKS

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 33 OF 87	

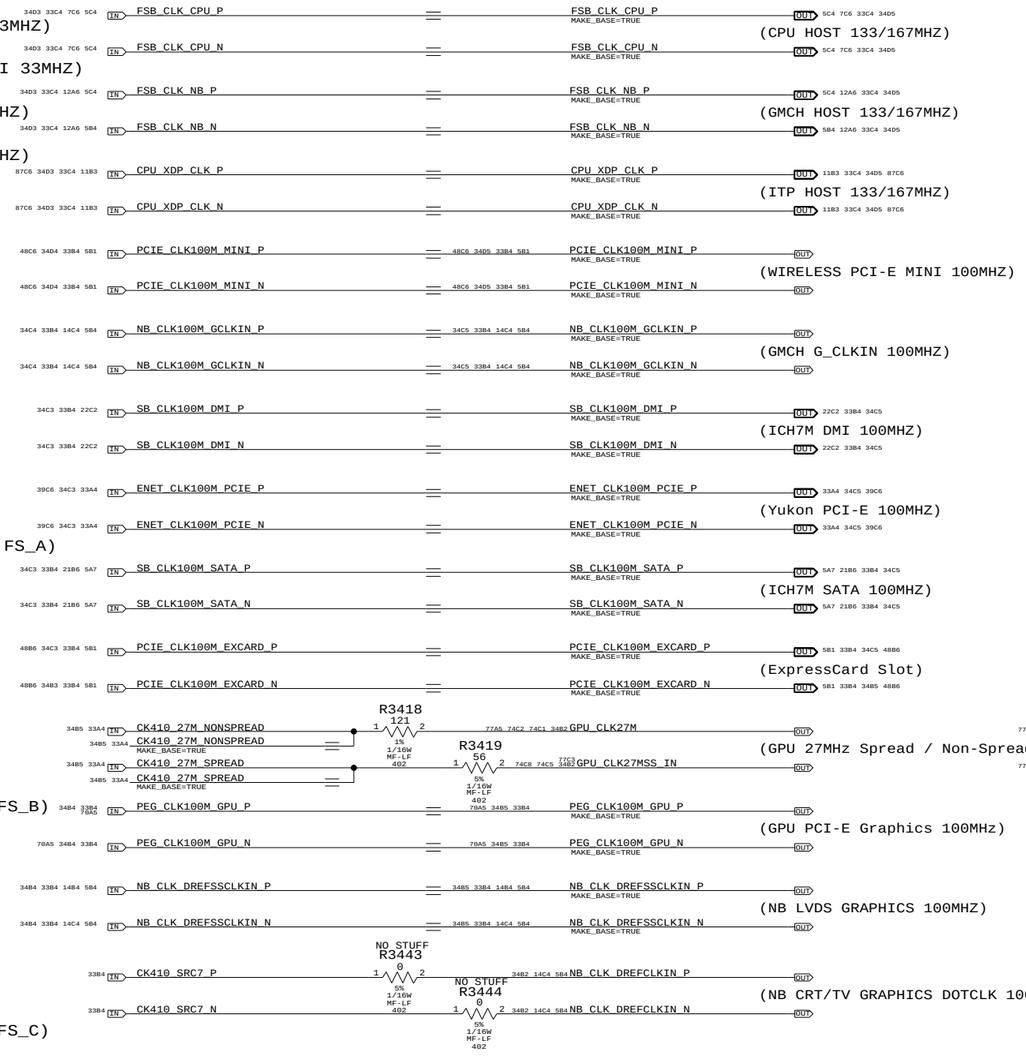


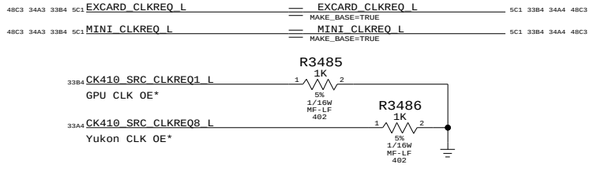


NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED





Clock Termination

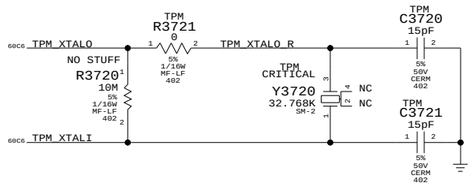
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

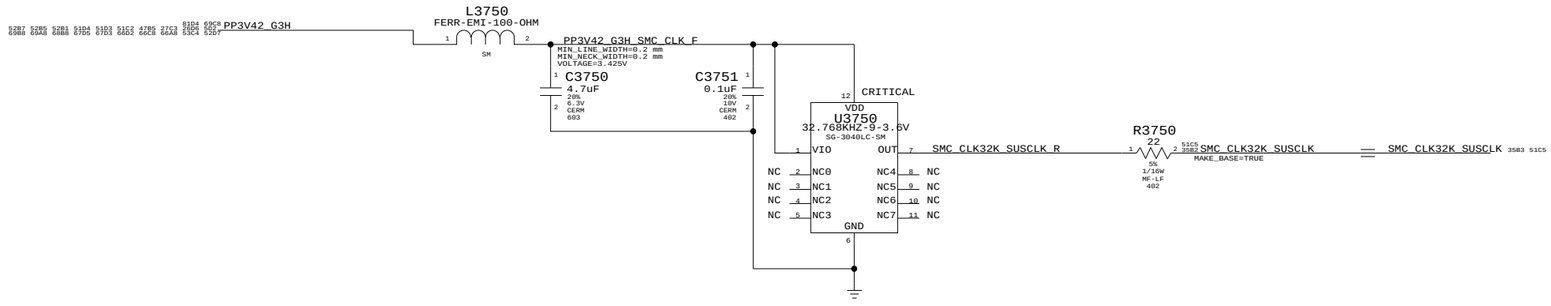
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT 34 OF 87

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

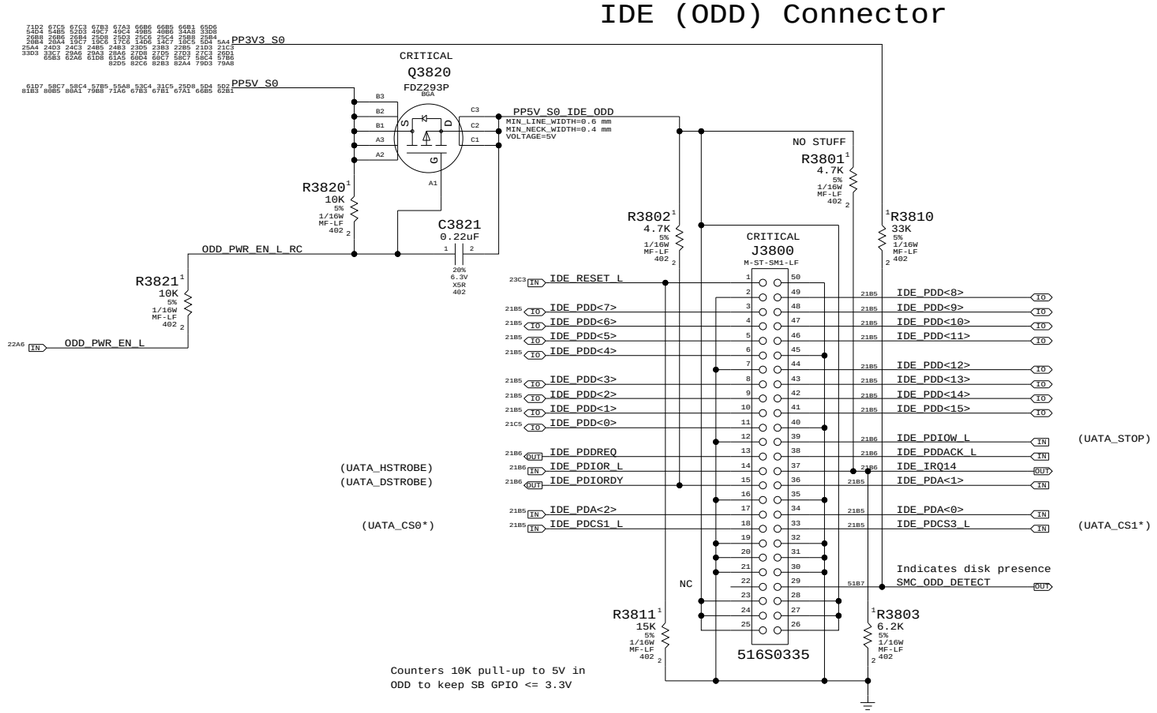
APPLE COMPUTER INC.

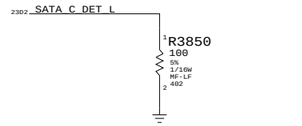
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

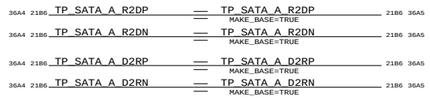
SCALE NONE

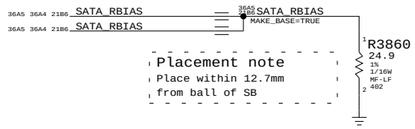
SHT 35 OF 87

IDE (ODD) Connector









PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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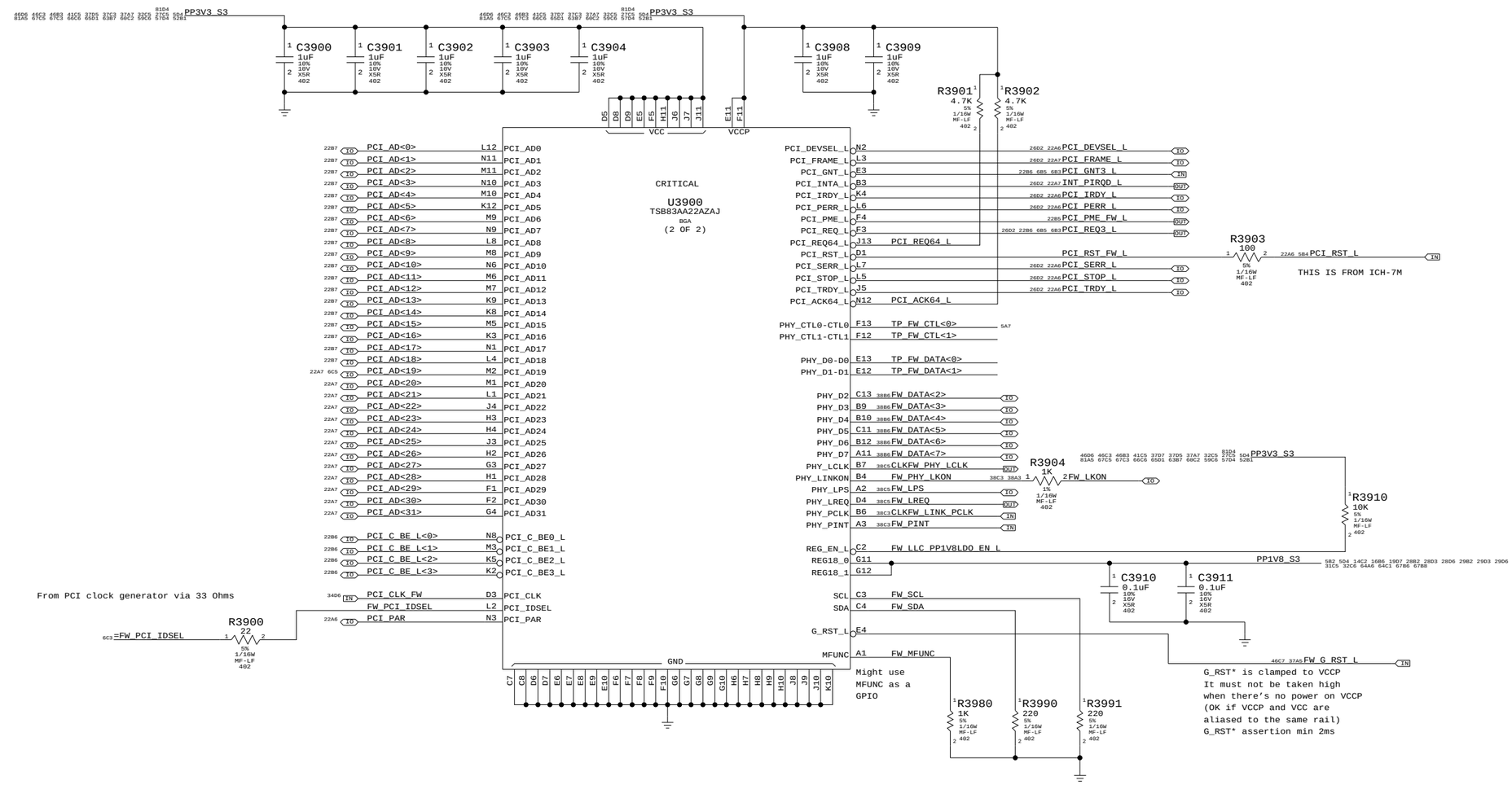
SCALE	SHT	OF
NONE	36	87



FireWire Link (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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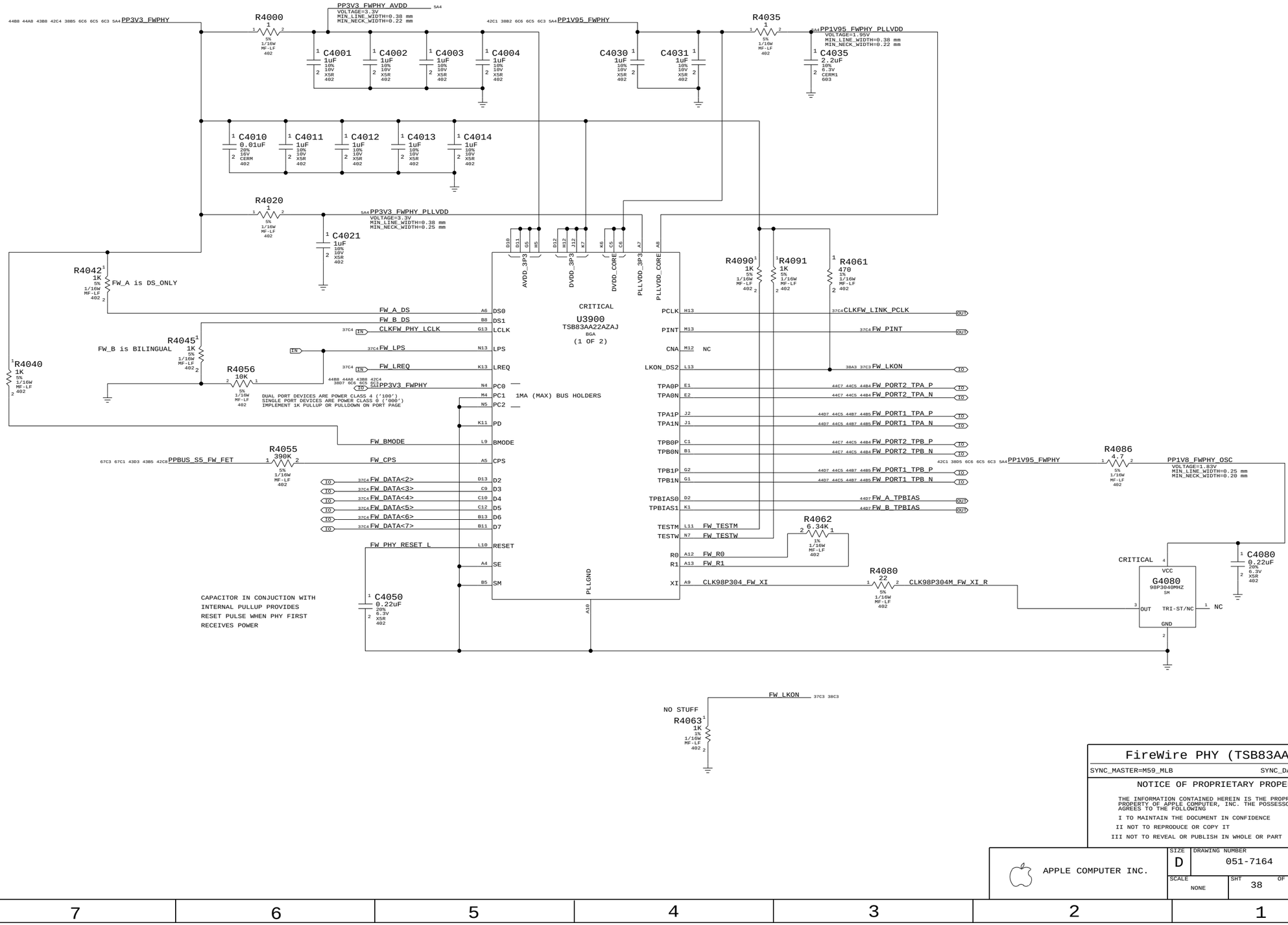
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	37	87



FireWire PHY (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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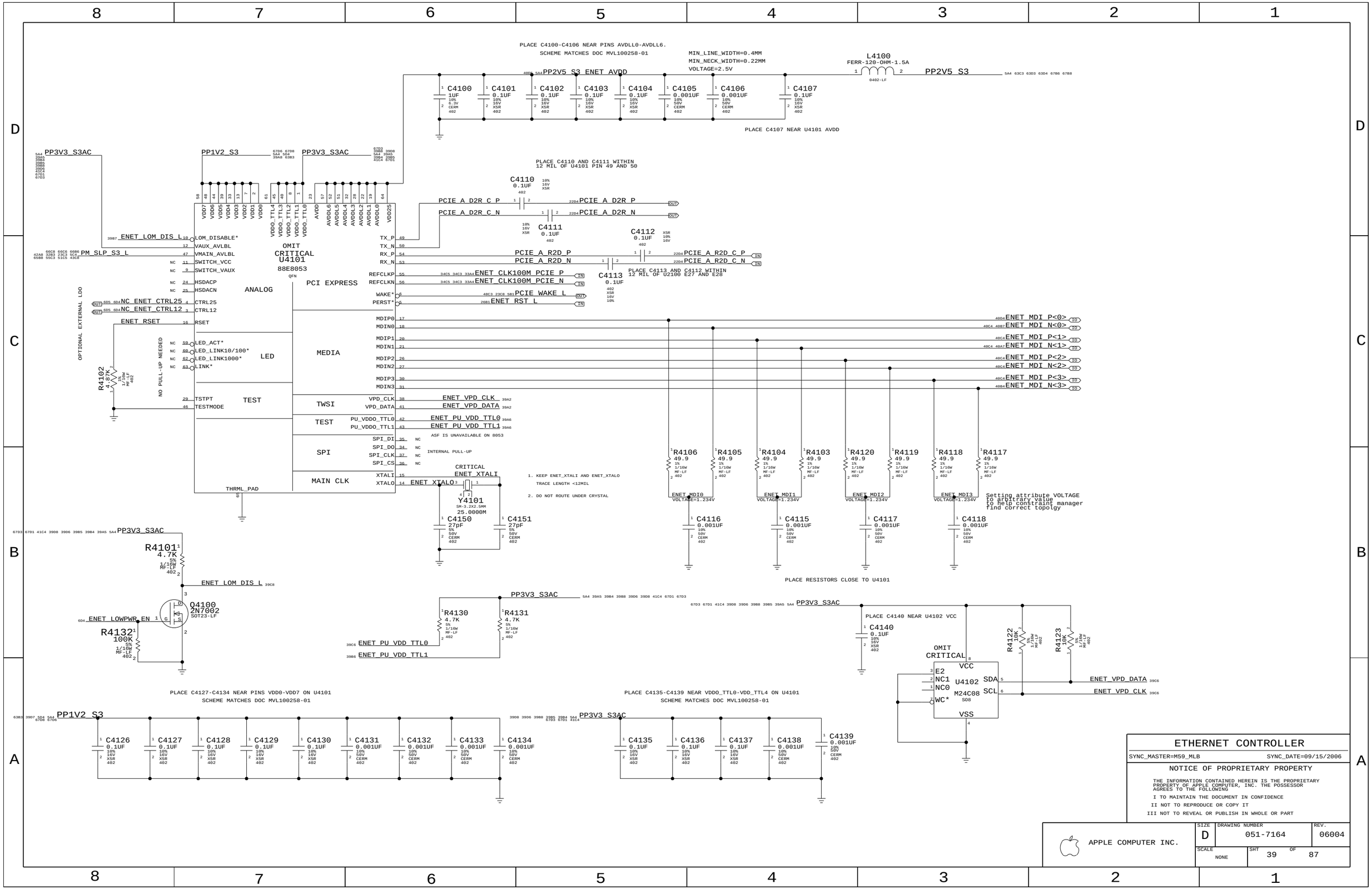
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

SHT 38 OF 87


PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V
PP2V5_S3_ENET_AVDD
L4100
FERR-120-OHM-1.5A
PP2V5_S3
C4100 1UF
C4101 0.1UF
C4102 0.1UF
C4103 0.1UF
C4104 0.1UF
C4105 0.001UF
C4106 0.001UF
C4107 0.1UF
PLACE C4107 NEAR U4101 AVDD
PP3V3_S3AC
PP1V2_S3
PP3V3_S3AC
PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50
C4110 0.1UF
PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
C4111 0.1UF
C4112 0.1UF
PCIE_A_D2R_P
PCIE_A_D2R_N
PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28
C4113 0.1UF
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N
ENET_LOM_DIS_L
PM_SLP_S3_L
OMIT
CRITICAL
U4101
88E8053
QFN
ANALOG
PCI EXPRESS
LED
TEST
TWSI
SPI
MAIN CLK
MEDIA
OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED
NC_ENET_CTRL25
NC_ENET_CTRL12
ENET_RSET
R4102 4.87K
ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
R4106 49.9
R4105 49.9
R4104 49.9
R4103 49.9
R4120 49.9
R4119 49.9
R4118 49.9
R4117 49.9
ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1
ASF IS UNAVAILABLE ON 8053
INTERNAL PULL-UP
CRITICAL
ENET_XTALI
ENET_XTALO
Y4101 25.0000M
C4150 27pF
C4151 27pF
1. KEEP ENET_XTALI AND ENET_XTALO
TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL
THRML_PAD
ENET_MDI0 VOLTAGE=1.234V
ENET_MDI1 VOLTAGE=1.234V
ENET_MDI2 VOLTAGE=1.234V
ENET_MDI3 VOLTAGE=1.234V
C4116 0.001UF
C4115 0.001UF
C4117 0.001UF
C4118 0.001UF
Setting attribute VOLTAGE
to arbitrary value
to help constraint manager
find correct topolgy
PLACE RESISTORS CLOSE TO U4101
Q4100 2N7002 SOT23-LF
R4101 4.7K
R4132 100K
R4130 4.7K
R4131 4.7K
PLACE C4140 NEAR U4102 VCC
C4140 0.1UF
OMIT
CRITICAL
U4102
M24C08
SO8
R4122 10K
R4123 10K
PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01
C4126 0.1UF
C4127 0.1UF
C4128 0.1UF
C4129 0.1UF
C4130 0.1UF
C4131 0.001UF
C4132 0.001UF
C4133 0.001UF
C4134 0.001UF
PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01
C4135 0.1UF
C4136 0.1UF
C4137 0.1UF
C4138 0.001UF
C4139 0.001UF
ETHERNET CONTROLLER
SYNC_MASTER=M59_MLB
SYNC_DATE=09/15/2006
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7164
REV. 06004
SCALE NONE
SHT 39 OF 87

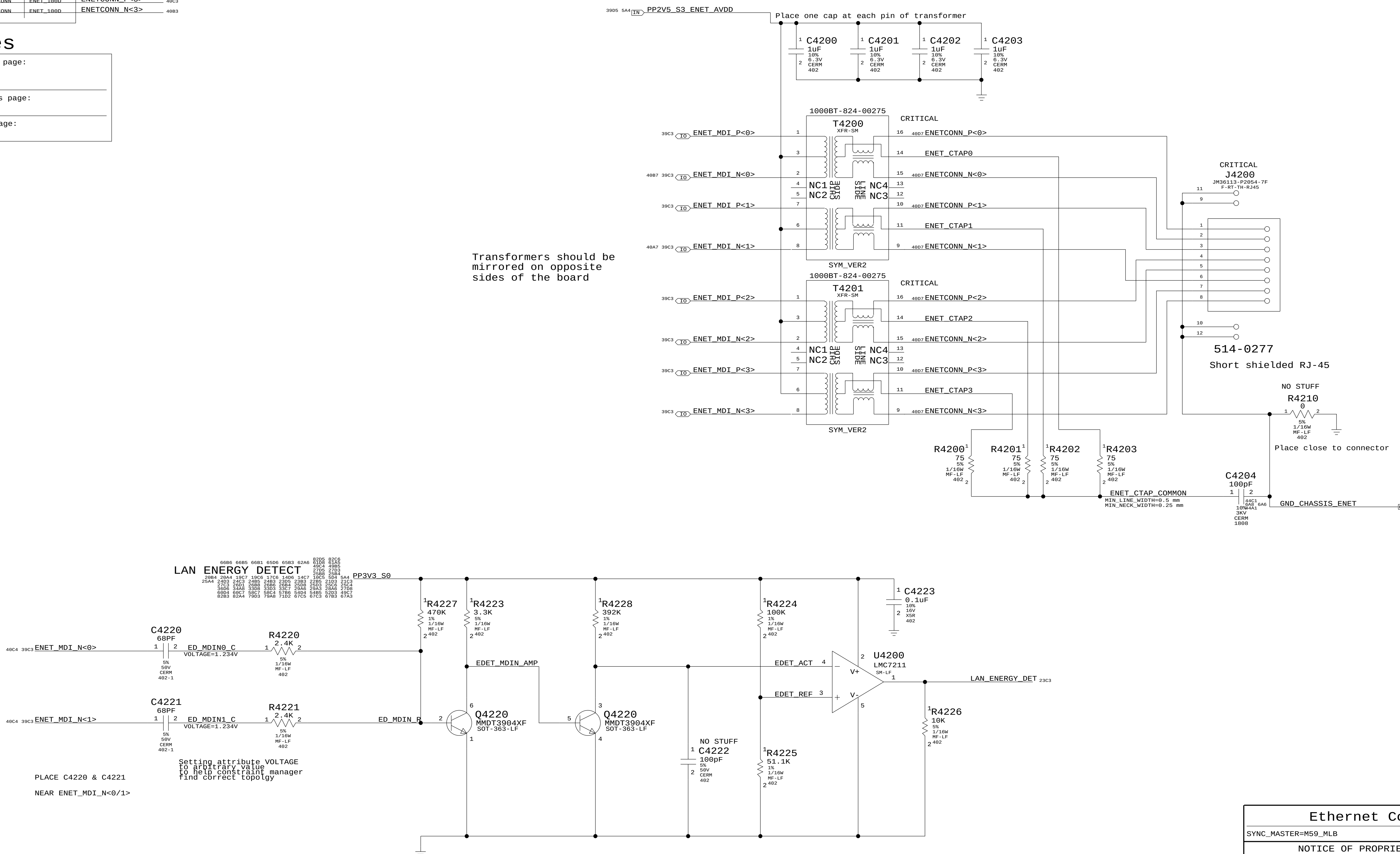
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
	ENETCONN	ENET_100D	ENETCONN_N<0>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<3>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<3>	40B3

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PP2V5_S3_ENET_AVDD
Place one cap at each pin of transformer
C4200 1uF 10% 6.3V CERM 402
C4201 1uF 10% 6.3V CERM 402
C4202 1uF 10% 6.3V CERM 402
C4203 1uF 10% 6.3V CERM 402
1000BT-824-00275
T4200
XFR-SM
CRITICAL
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENETCONN_P<0>
ENET_CTAP0
ENETCONN_N<0>
ENETCONN_P<1>
ENET_CTAP1
ENETCONN_N<1>
SYM_VER2
Transformers should be mirrored on opposite sides of the board
T4201
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
ENETCONN_P<2>
ENET_CTAP2
ENETCONN_N<2>
ENETCONN_P<3>
ENET_CTAP3
ENETCONN_N<3>
CRITICAL
J4200
JM36113-P2054-7F
F-RT-TH-RJ45
514-0277
Short shielded RJ-45
NO STUFF
R4210
0
Place close to connector
R4200 75
R4201 75
R4202 75
R4203 75
ENET_CTAP_COMMON
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
C4204
100pF
GND_CHASSIS_ENET
LAN ENERGY DETECT
PP3V3_S0
C4220 68PF
C4221 68PF
ENET_MDI_N<0>
ENET_MDI_N<1>
ED_MDIN0_C
ED_MDIN1_C
VOLTAGE=1.234V
R4220 2.4K
R4221 2.4K
ED_MDIN_R
R4227 470K
R4223 3.3K
R4228 392K
R4224 100K
R4225 51.1K
R4226 10K
EDET_MDIN_AMP
Q4220
MMDT3904XF
SOT-363-LF
NO STUFF
C4222 100pF
C4223 0.1uF
EDET_ACT
EDET_REF
U4200
LMC7211
SM-LF
LAN_ENERGY_DET
PLACE C4220 & C4221
NEAR ENET_MDI_N<0/1>
Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

Ethernet Connector	
SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006

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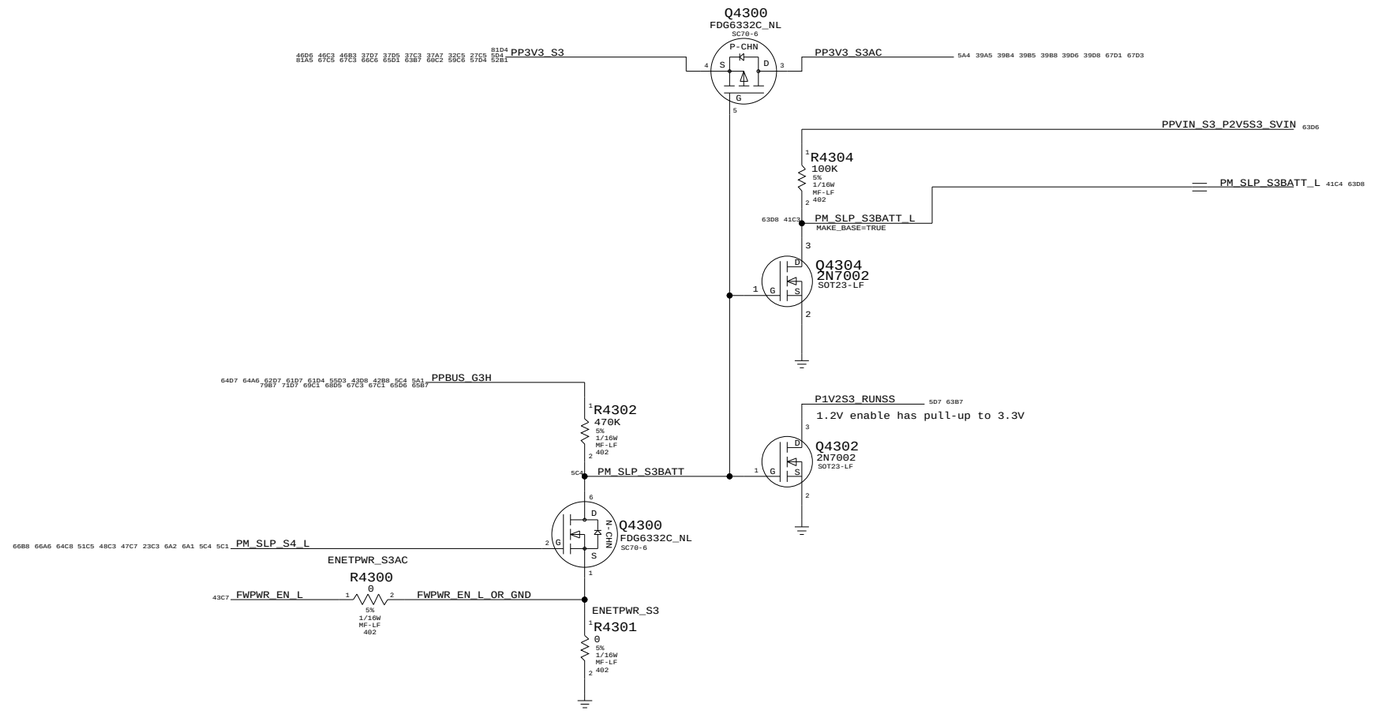
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE NONE	SHT 40	OF 87

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

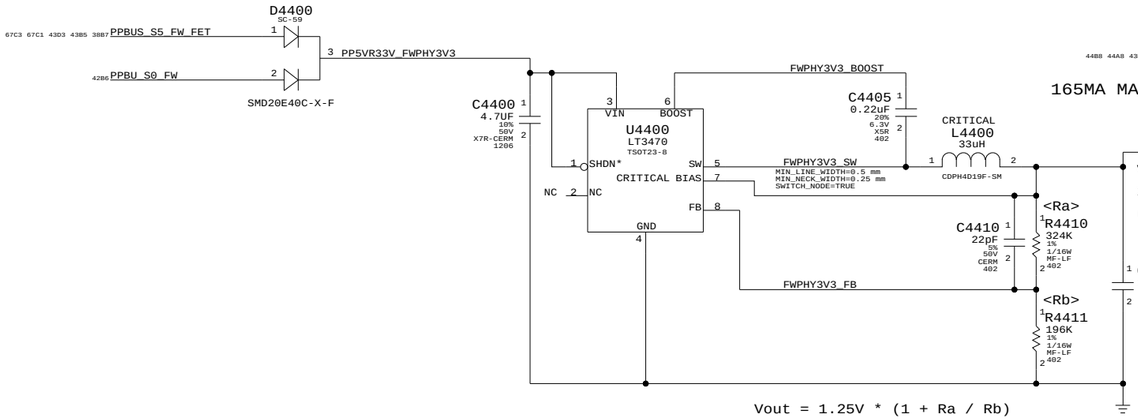
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

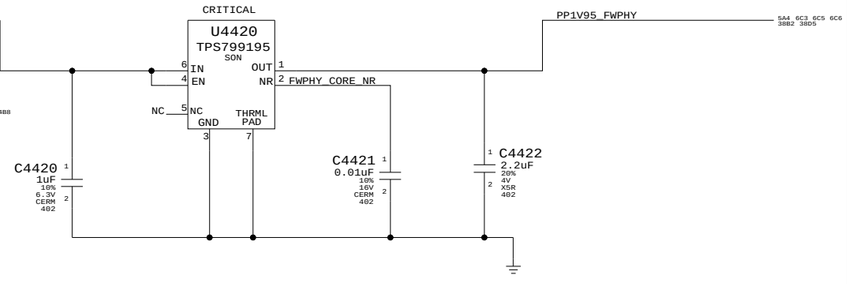
SCALE	SHT	OF
NONE	41	87

3.3V Supply for FWPHY

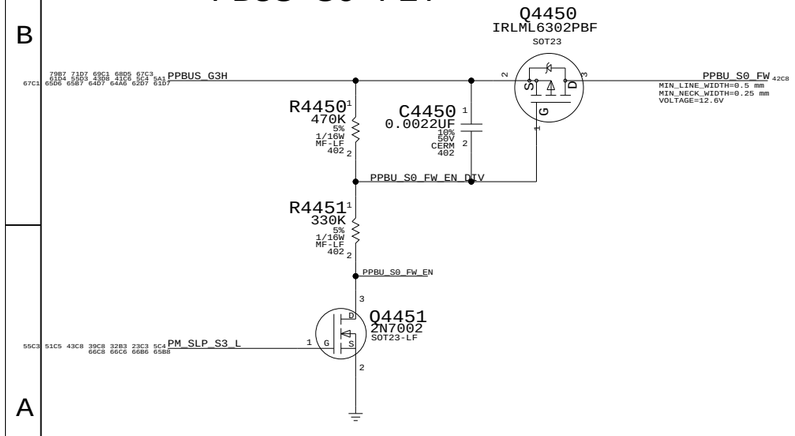


Vout = 1.25V * (1 + Ra / Rb)

1.95V Supply for FW PHY



PBUS S0 FET



FW PHY Power Supply

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	42	87

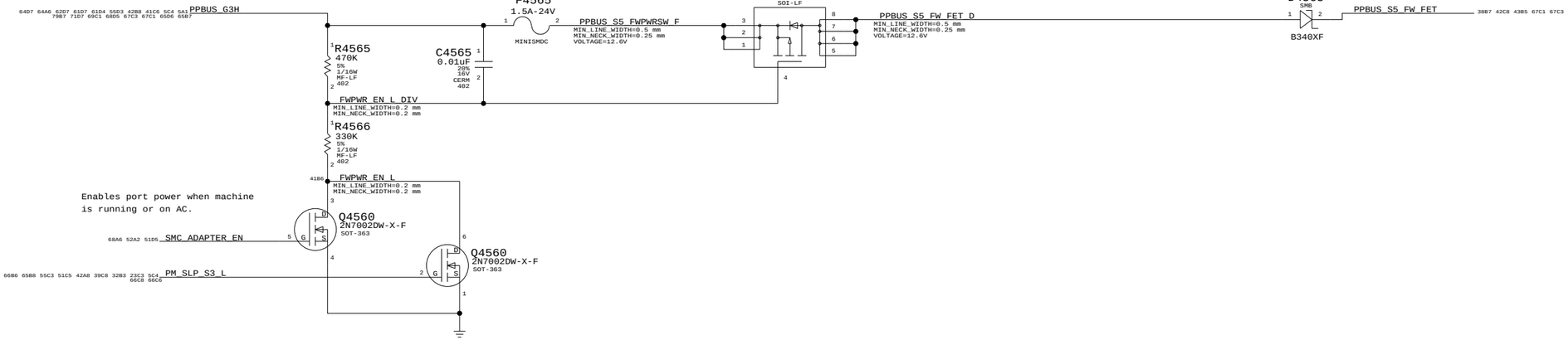
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

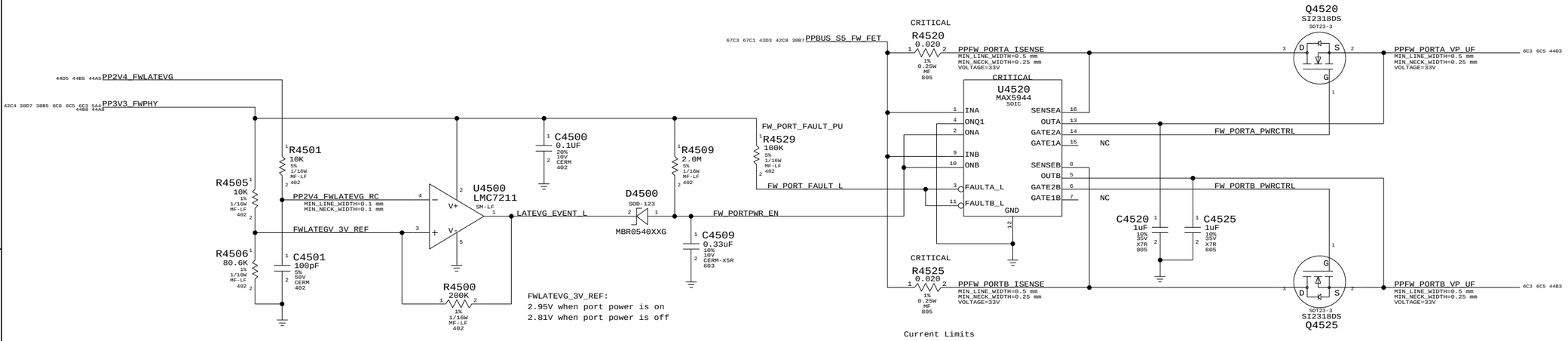
BOM options provided by this page:
(NONE)

Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 43 OF 87	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED	FW	FW_110D	FW_PORT1_TPA_P	38B3 44B5 44B7 44C5
	FW	FW_110D	FW_PORT1_TPA_N	38B3 44B5 44B7 44C5
BY	FW	FW_110D	FW_PORT1_TPB_P	38B3 44B5 44B7 44C5
	FW	FW_110D	FW_PORT1_TPB_N	38B3 44B5 44B7 44C5
PHY	FW	FW_110D	FW_PORT2_TPA_FL_P	44B2
	FW	FW_110D	FW_PORT2_TPA_FL_N	44B2
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_P	44B2
	FW	FW_110D	FW_PORT2_TPB_FL_N	44B2

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

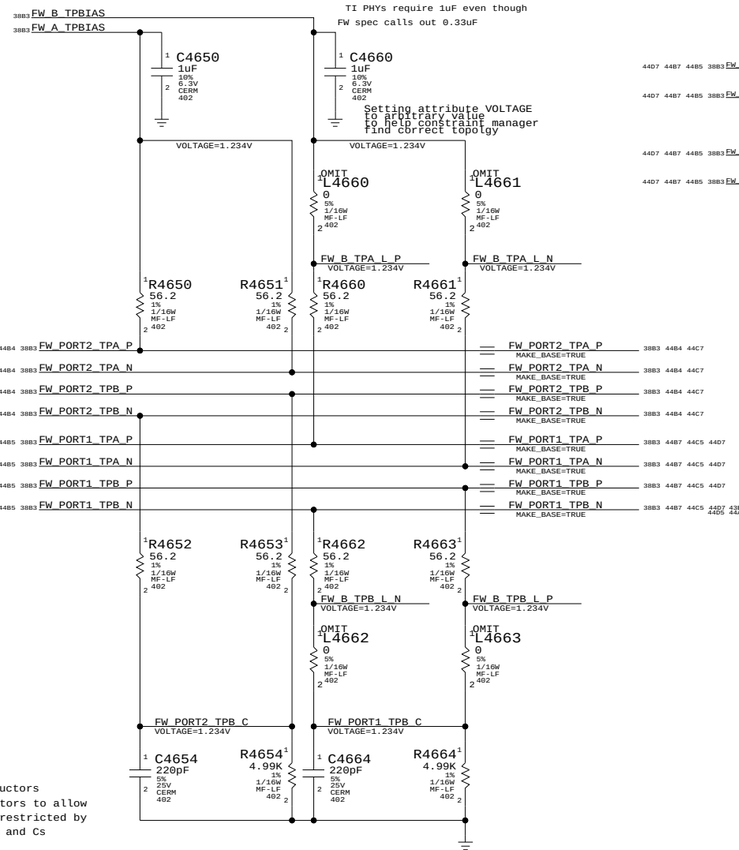
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

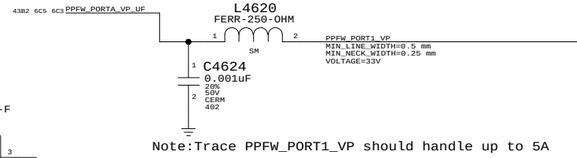
Place close to FireWire PHY



Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

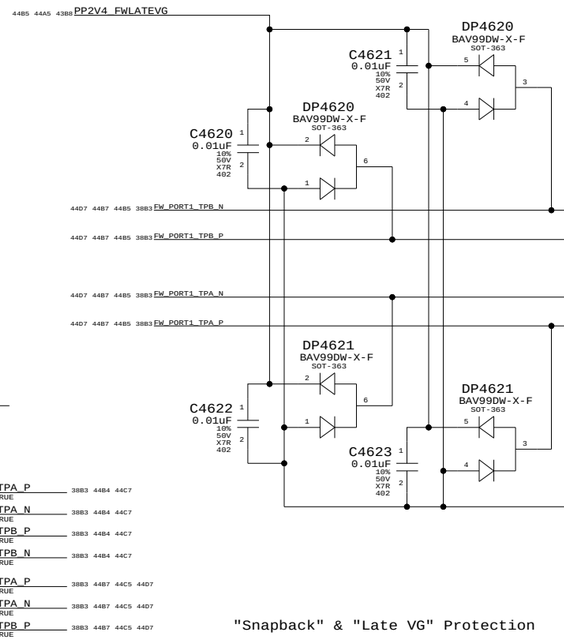
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

Cable Power

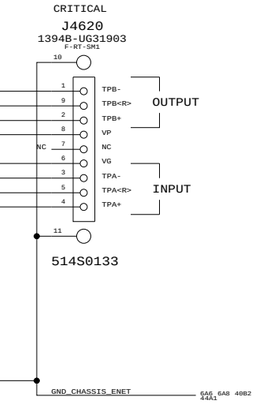


Note:Trace PPFW_PORT1_VP should handle up to 5A

"Snapback" & "Late VG" Protection



PORT 1 BILINGUAL



C4629 0.1uF 10% 50V X7R 603-1 — Place C4629 close to pin 5 of connector

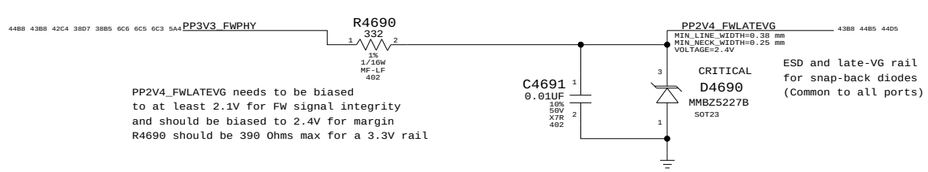
R4629 1M 5% 1/16W MF-LF 402

C4625 0.01uF 20% 50V CERM 603

NO STUFF C4627 0.01uF 20% 16V CERM 402

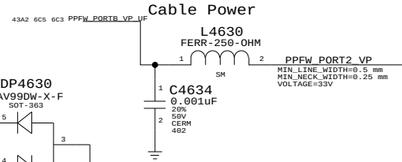
C4626 0.01uF 20% 16V CERM 402

Late-VG Protection Power

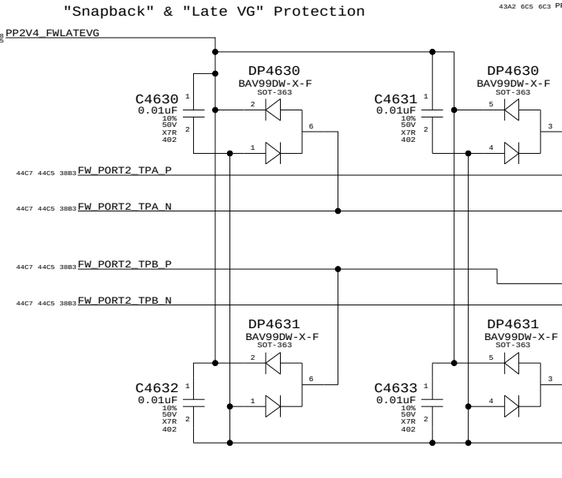


PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail

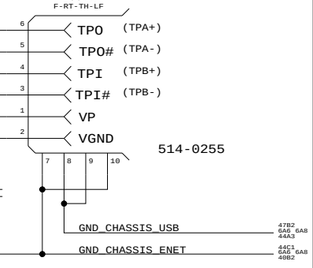
Cable Power



"Snapback" & "Late VG" Protection



PORT 2 1394A



C4635 0.01uF 20% 50V CERM 603

C4636 0.01uF 20% 16V CERM 402

R4699 0 5% 1/16W MF-LF 402 — GND_CHASSIS_USB

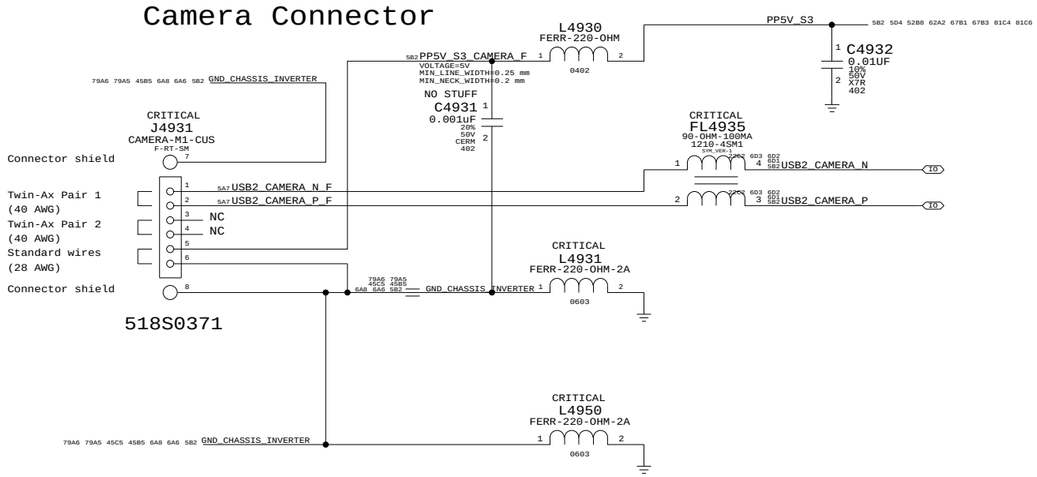
FireWire Ports

SYNC_MASTER=M59_MLB SYNC_DATE=06/27/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 44 OF 87	

Camera Connector



Camera Connector

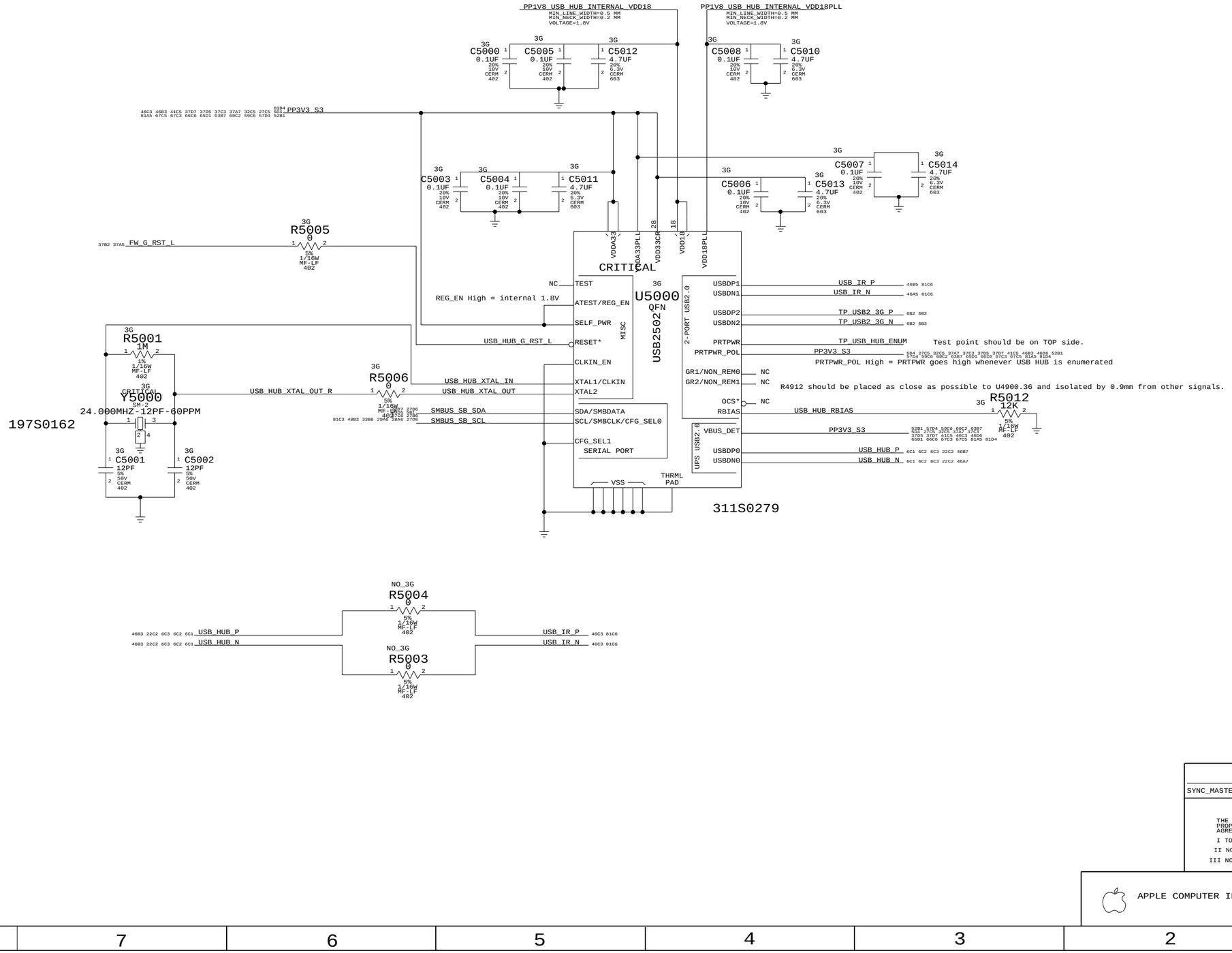
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

SHT 45 OF 87



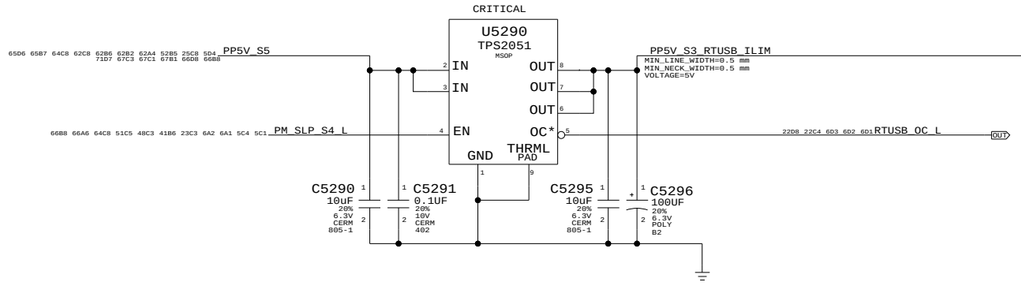
Internal USB Hub

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

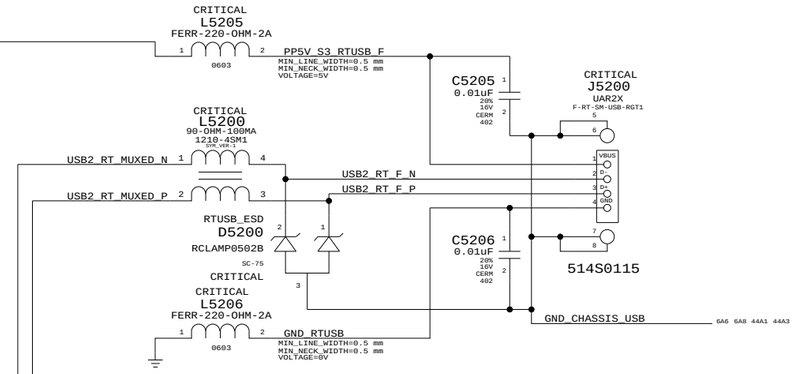
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 46 OF 87	

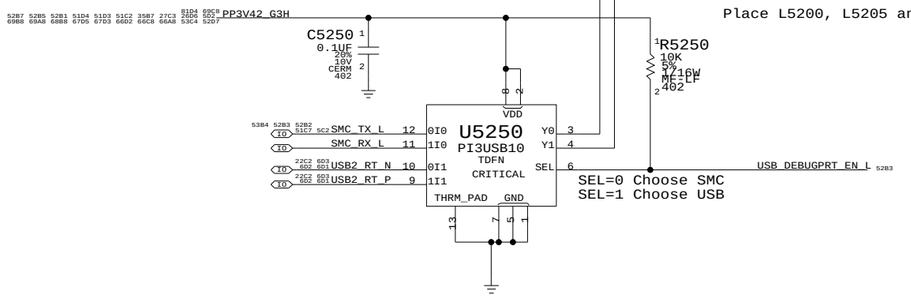
Port Power Switch



Right USB Port



USB/SMC Debug Mux



Place L5200, L5205 and L5206 across moat

External USB Connector

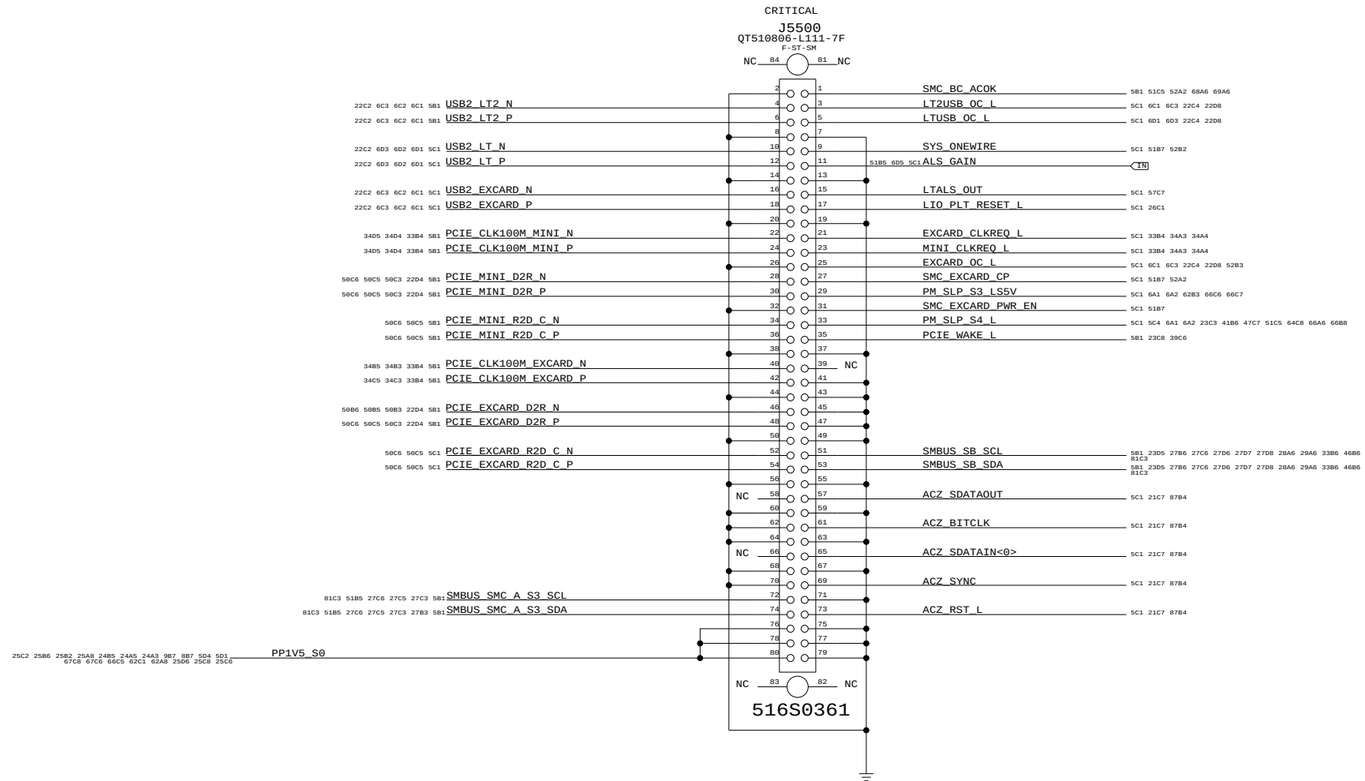
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	47	87

Left I/O Board Connector



Left I/O Board Connector

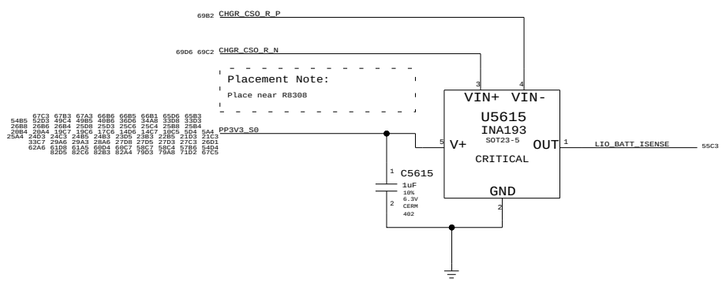
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

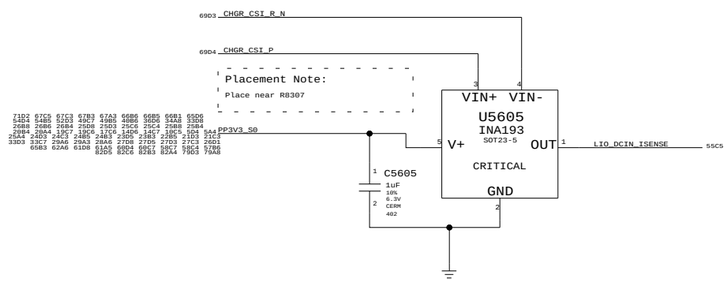
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	48	87

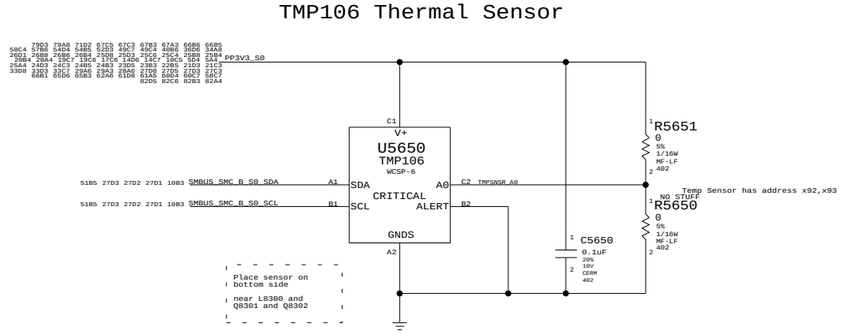
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

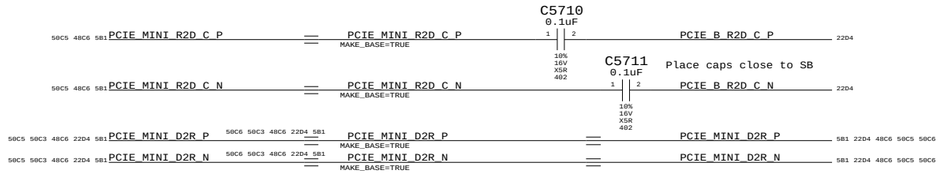
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

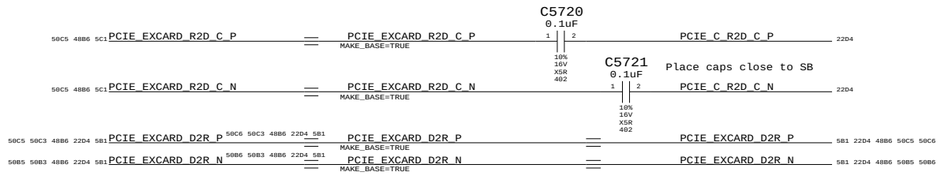
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 49 OF 87	

PCI-E x1 Port "A" = Ethernet (Yukon)

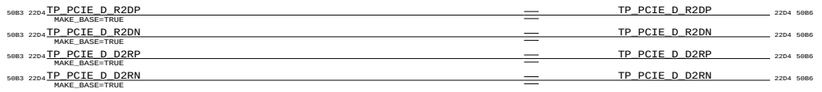
PCI-E x1 Port "B" = PCI-E Mini Card



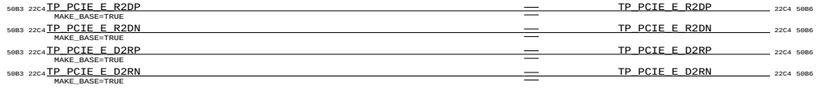
PCI-E x1 Port "C" = ExpressCard



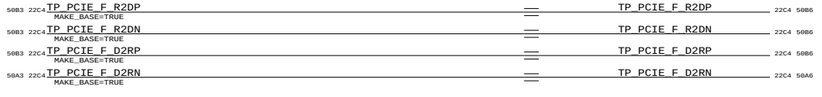
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	50	87

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	SPI_ARB
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	SPI_SCLK
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	SPI_SI
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	SPI_SO
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	FWH_INIT_L
TP_SMC_P20	D13	P20	P70/AN0	N12	SMC_CPU_ISENSE
TP_SMC_P21	D14	P21	P71/AN1	R13	SMC_CPU_VSENSE
TP_SMC_P22	D15	P22	P72/AN2	P13	SMC_GPU_ISENSE
TP_SMC_P23	E12	P23	P73/AN3	R14	SMC_GPU_VSENSE
SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE
TP_SMC_P26	E13	P26	P76/AN6	N13	SMC_BATT_ISENSE
TP_SMC_P27	F14	P27	P77/AN7	P15	SMC_P1V5S0_NB_ISENSE
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	SMC_TPM_GPIO
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SC_TX_L
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SC_RX_L
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	SMBUS_SMC_BSB_SCL
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	SMC_ONOFF_L
TP_SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2	SMC_BC_ACOK
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	SMC_BS_ALRT_L
SMBUS_SMC_BSB_SDA	D5	P42/SDA1	P93/IRQ12*	J3	PM_SLP_S3_L
SMC_TPM_PP	C3	P43/TMI1/EXSCKX1	P94/IRQ13*	J4	PM_SLP_S4_L
TP_SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	PM_SLP_S5_L
TP_SMC_XDP_TCK	C2	P45	P96/EXCL	H1	SMC_CLK32K_SUSCLK
TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	SMBUS_SMC_0_S0_SDA
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1			
SMC_TX_L	G1	P50			
SMC_RX_L	G4	P51			
SMBUS_SMC_0_S0_SCL	F2	P52/SCL0			

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	SMC_CASE_OPEN
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	SMC_TCK
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI
SMC_USB_DEBUG_MUX	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	TP_SMC_PF0
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	TP_SMC_PF1
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	TP_SMC_BATT_VSET
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	TP_SMC_SYS_VSET
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	SPI_CE_L
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	SMBUS_SMC_BSA_SDA
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	SMBUS_SMC_BSA_SCL
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	SMBUS_SMC_A_S3_SDA
TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	SMBUS_SMC_A_S3_SCL
TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	SMBUS_SMC_B_S0_SDA
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	SMBUS_SMC_B_S0_SCL
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	SMC_PROCHOT
TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	SMC_THRMTRIP
TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	SMC_FWE
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	ALS_GAIN
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	SMS_INT_L
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	SMS_ONOFF_L
TP_SMC_ANALOG_ID	N11	PD3/AN11			
SMC_P1V05S0_ISENSE	P10	PD4/AN12			
SMC_MEM_ISENSE	R10	PD5/AN13			
ALS_LEFT	N10	PD6/AN14			
ALS_RIGHT	M10	PD7/AN15			

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

PP3V42_G3H

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

PP3V42_G3H
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
PP3V42_G3H

OMIT
U5800
SMC_H8S2116
BGA
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SMC_RST_L
SMC_XTAL
SMC_EXTAL

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
KBC_MDE
SMC_MD1
SMC_NMI
SMC_TRST_L
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800
SM
GND_SMC_AVSS

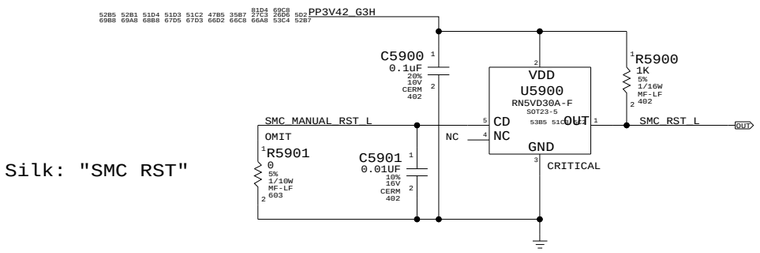
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

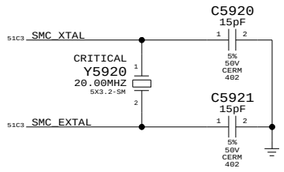
SHT 51 OF 87

SMC Reset Button / Brownout Detect

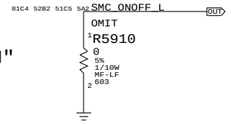


Silk: "SMC RST"

SMC Crystal Circuit

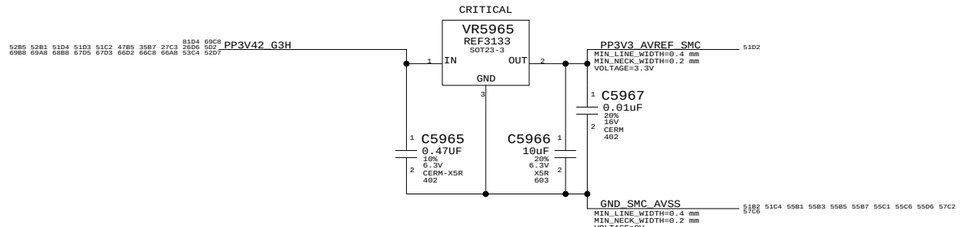


Debug Power Button

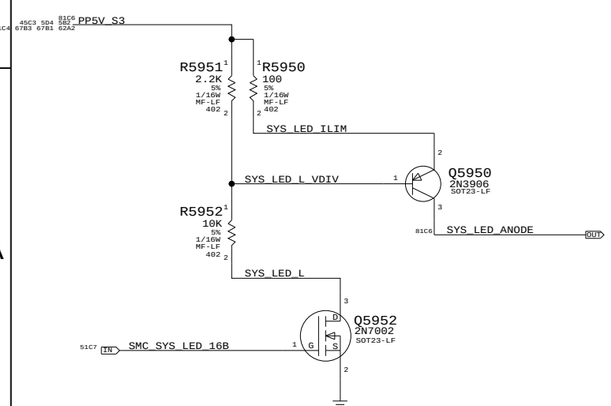


Silk: "PWR BTN"

SMC AVREF Supply

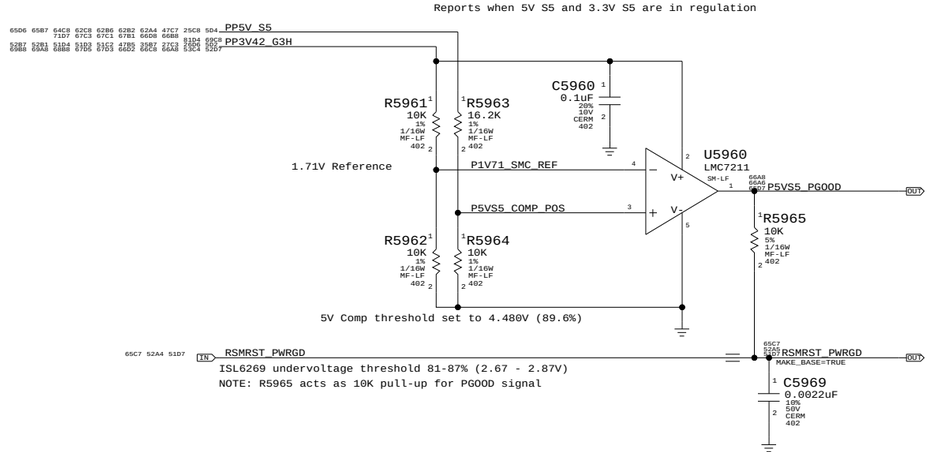


System (Sleep) LED Circuit

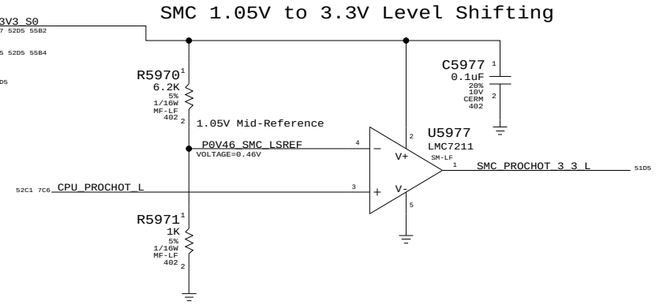


SMC PWRGD Circuit

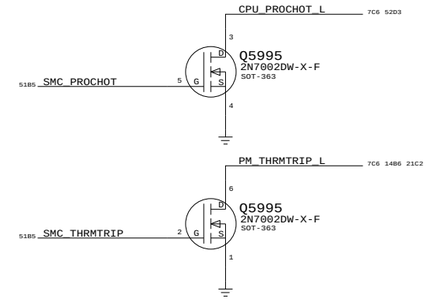
Reports when 5V S5 and 3.3V S5 are in regulation



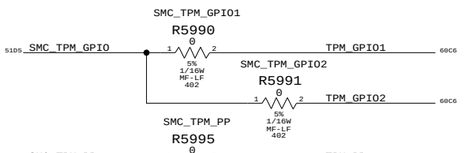
SMC 1.05V to 3.3V Level Shifting



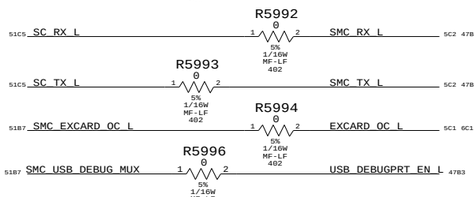
SMC 3.3V to 1.05V Level Shifting



SMC_TPM_GPIO1 / SMC_TPM_GPIO2 / SMC_TPM_PP



SC_RX_L / SC_TX_L / SMC_USB_DEBUG_MUX



Signal Table

FWH_INIT_L	FWH_INIT_L	MAKE_BASE=TRUE	
SMC_P1V05S0_ISENSE	SMC_P1V05S0_ISENSE	MAKE_BASE=TRUE	
SMC_P1V5S0_NB_ISENSE	SMC_P1V5S0_NB_ISENSE	MAKE_BASE=TRUE	
PM_EXTTS_L	PM_EXTTS_L	MAKE_BASE=TRUE	
TP_SMC_SYS_LED	TP_SMC_SYS_LED	MAKE_BASE=TRUE	
TP_SMC_ANALOG_ID	TP_SMC_ANALOG_ID	MAKE_BASE=TRUE	
TP_SMC_BATT_VSET	TP_SMC_BATT_VSET	MAKE_BASE=TRUE	
TP_SMC_SYS_VSET	TP_SMC_SYS_VSET	MAKE_BASE=TRUE	
TP_SMC_FAN_2_CTL	TP_SMC_FAN_2_CTL	MAKE_BASE=TRUE	
TP_SMC_FAN_2_TACH	TP_SMC_FAN_2_TACH	MAKE_BASE=TRUE	
TP_SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
TP_SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE	
TP_SMC_XDP_TCK	TP_SMC_XDP_TCK	MAKE_BASE=TRUE	
TP_SMC_XDP_TMS	TP_SMC_XDP_TMS	MAKE_BASE=TRUE	
TP_SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L	MAKE_BASE=TRUE	
TP_SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE	
TP_SMC_P21	TP_SMC_P21	MAKE_BASE=TRUE	
TP_SMC_P22	TP_SMC_P22	MAKE_BASE=TRUE	
TP_SMC_P23	TP_SMC_P23	MAKE_BASE=TRUE	
TP_SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE	
TP_SMC_P27	TP_SMC_P27	MAKE_BASE=TRUE	
TP_SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE	
TP_SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE	

SMC Support

SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006

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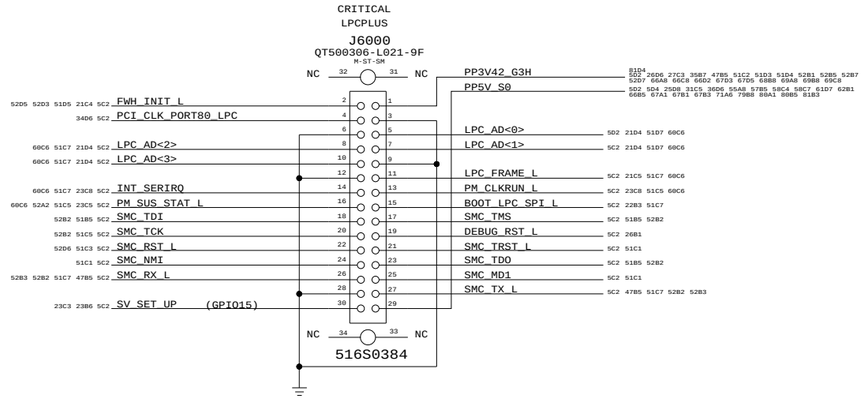
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7164	REV: 06004
	SCALE: NONE	SHT: 52	OF: 87



LPC+ Debug Connector

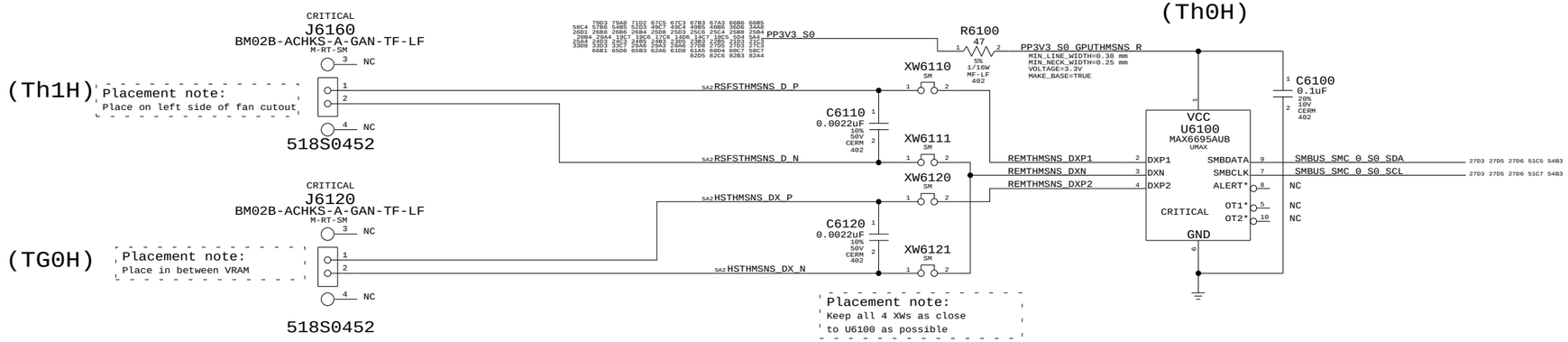
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

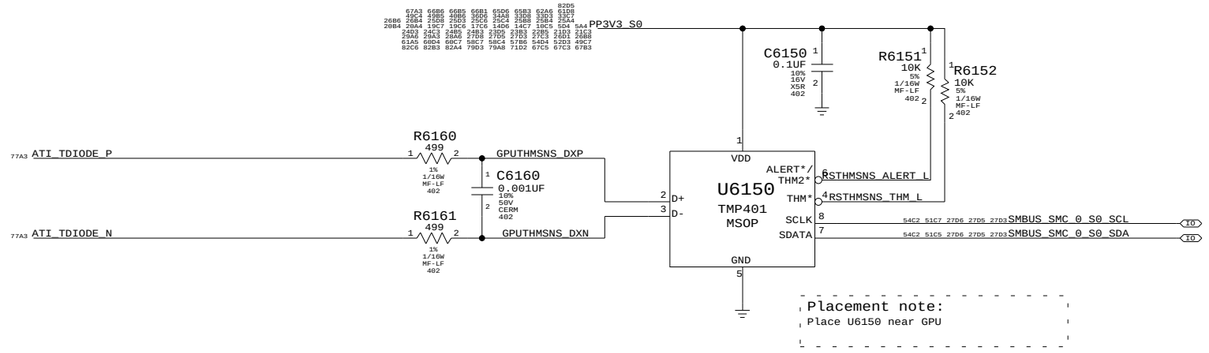
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	53	87

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

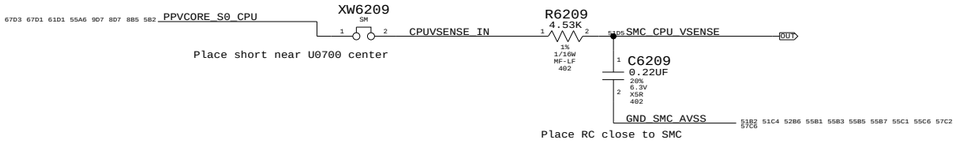
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

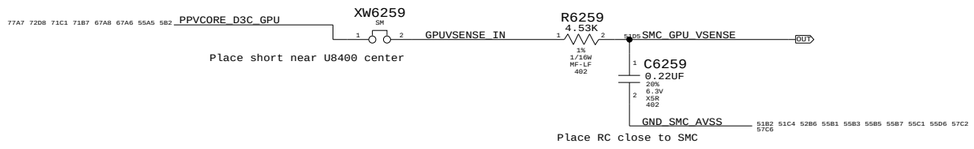
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	54	87

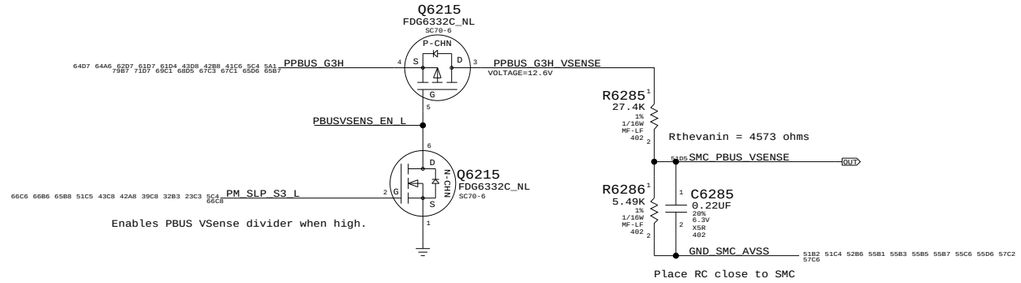
CPU Voltage Sense / Filter



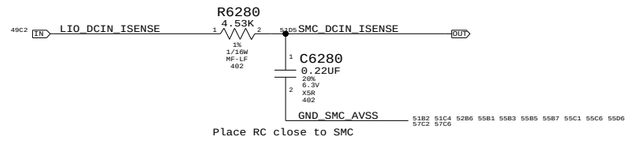
GPU Voltage Sense / Filter



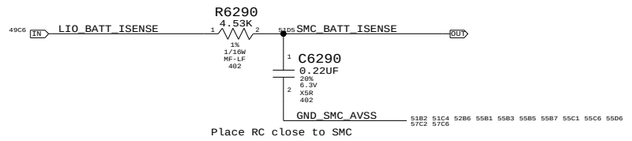
PBUS Voltage Sense Enable & Filter



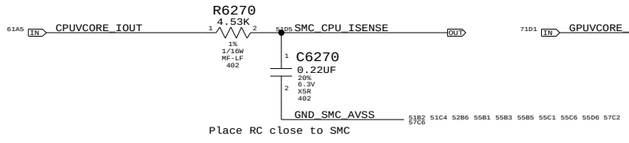
DCIN Current Sense Filter



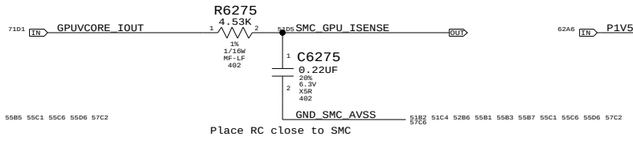
Battery Current Sense Filter



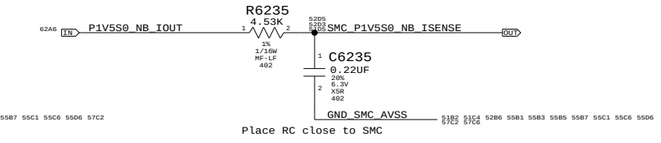
CPU Current Sense Filter



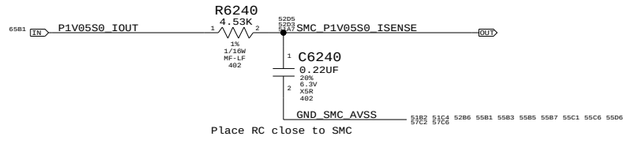
GPU Current Sense Filter



1.5V S0 (NB) Current Sense Filter

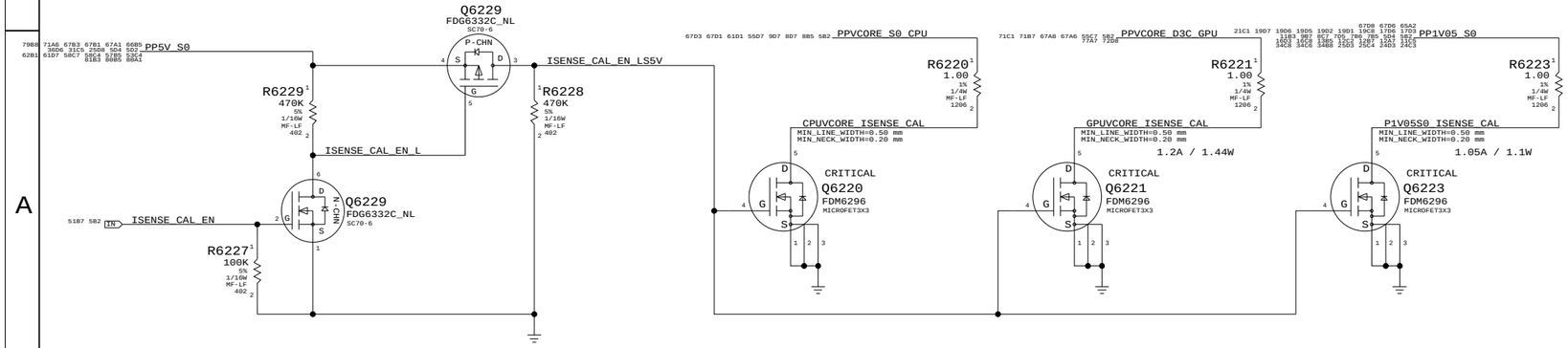


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing			
SYNC_MASTER=M59_MLB		SYNC_DATE=09/15/2006	
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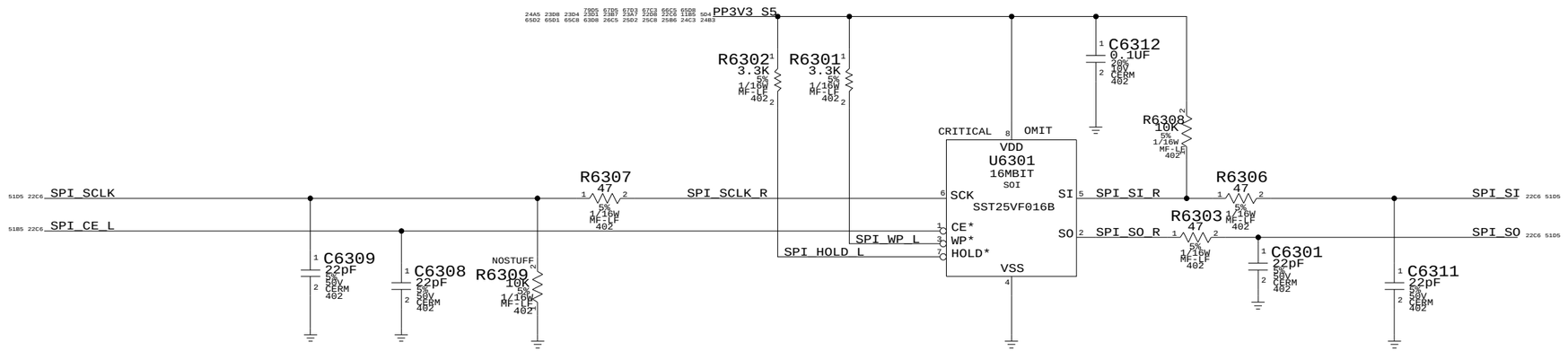
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7164	REV: 06004
	SCALE: NONE	SHT: 55 OF 87	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

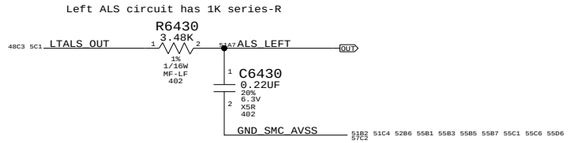
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

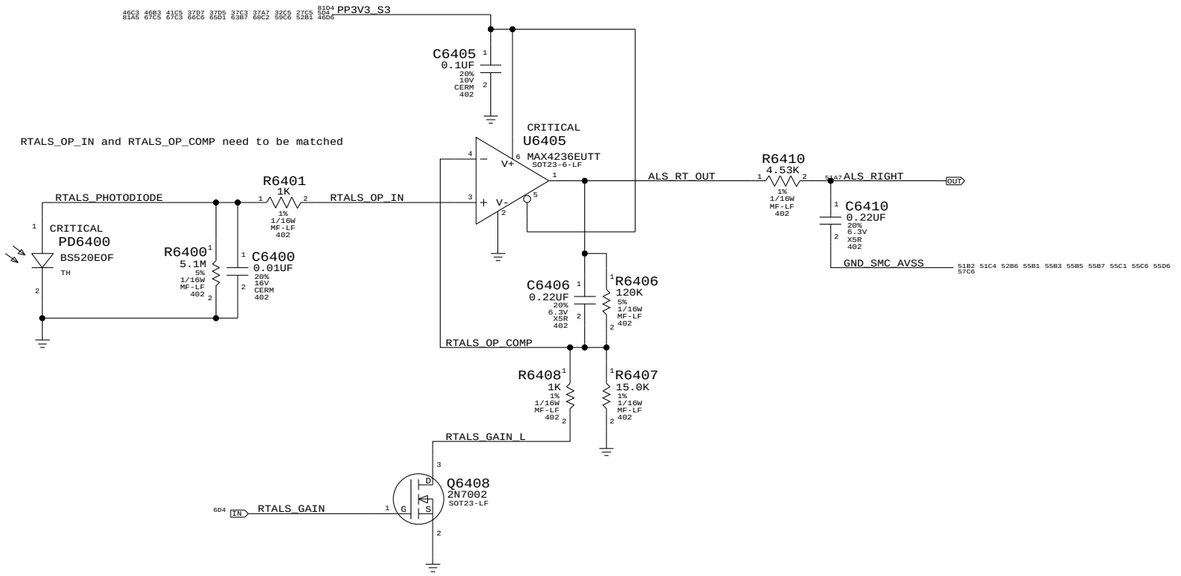
SCALE	SHT	OF
NONE	56	87

Left ALS Filter

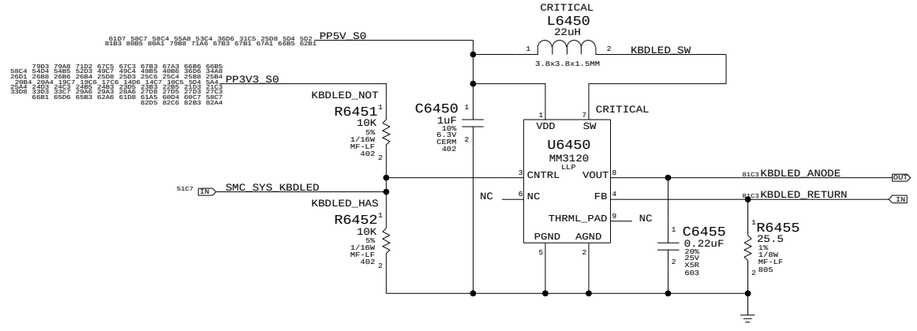
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver



ALS Support

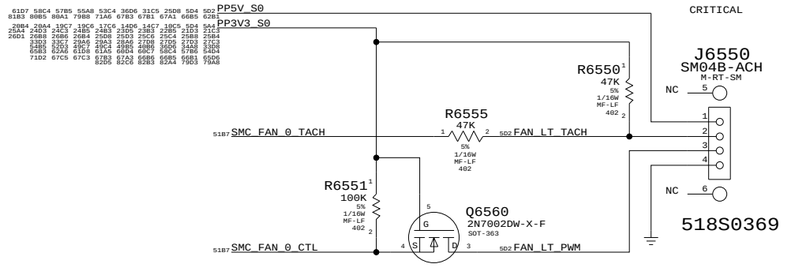
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

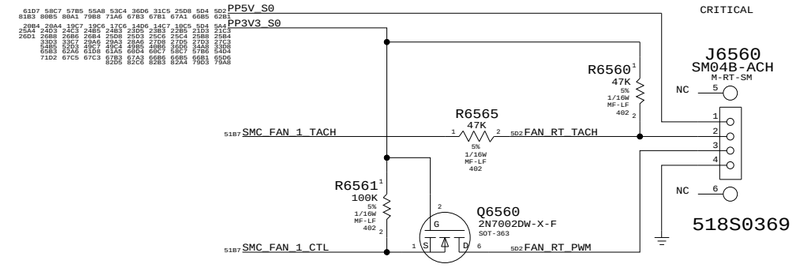
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	57	87

Left Fan



Right Fan



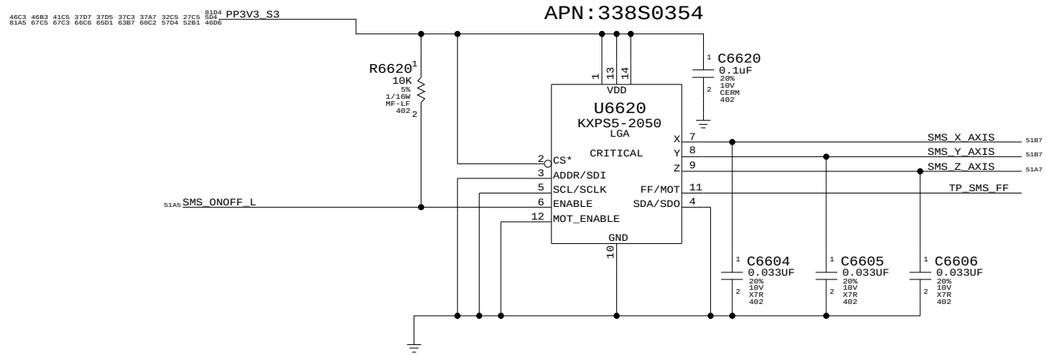
Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

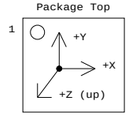
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	58	87



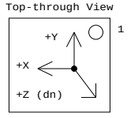
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M59 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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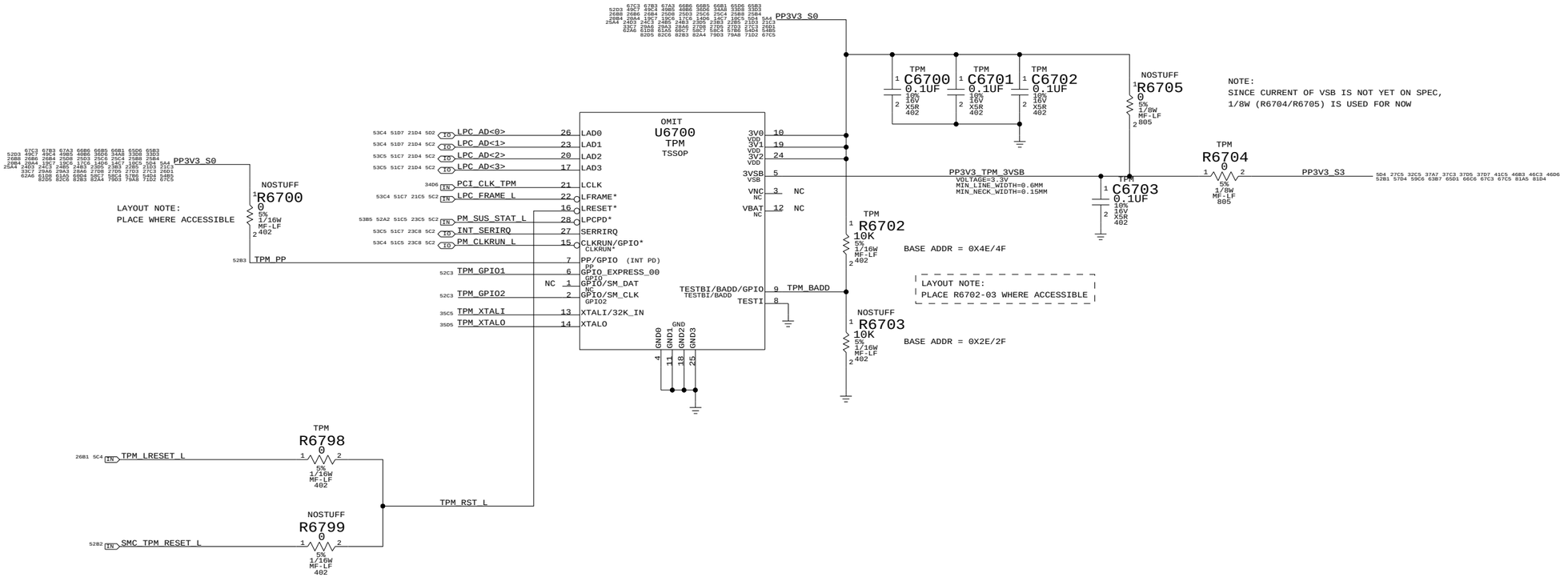
SCALE: NONE SHT 59 OF 87



TPM

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	60	87

DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

U7530 ISL9504CRZ QFN — OMIT

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)

Voffset = (Vdrp_offset * Kdroop) + Vamp_offset

Gain = Rc / (Ra + Rb)

Voffset worst-case ~2.3mV (+/- ~1A offset)

Vout @ 36A = 2.44V-2.60V

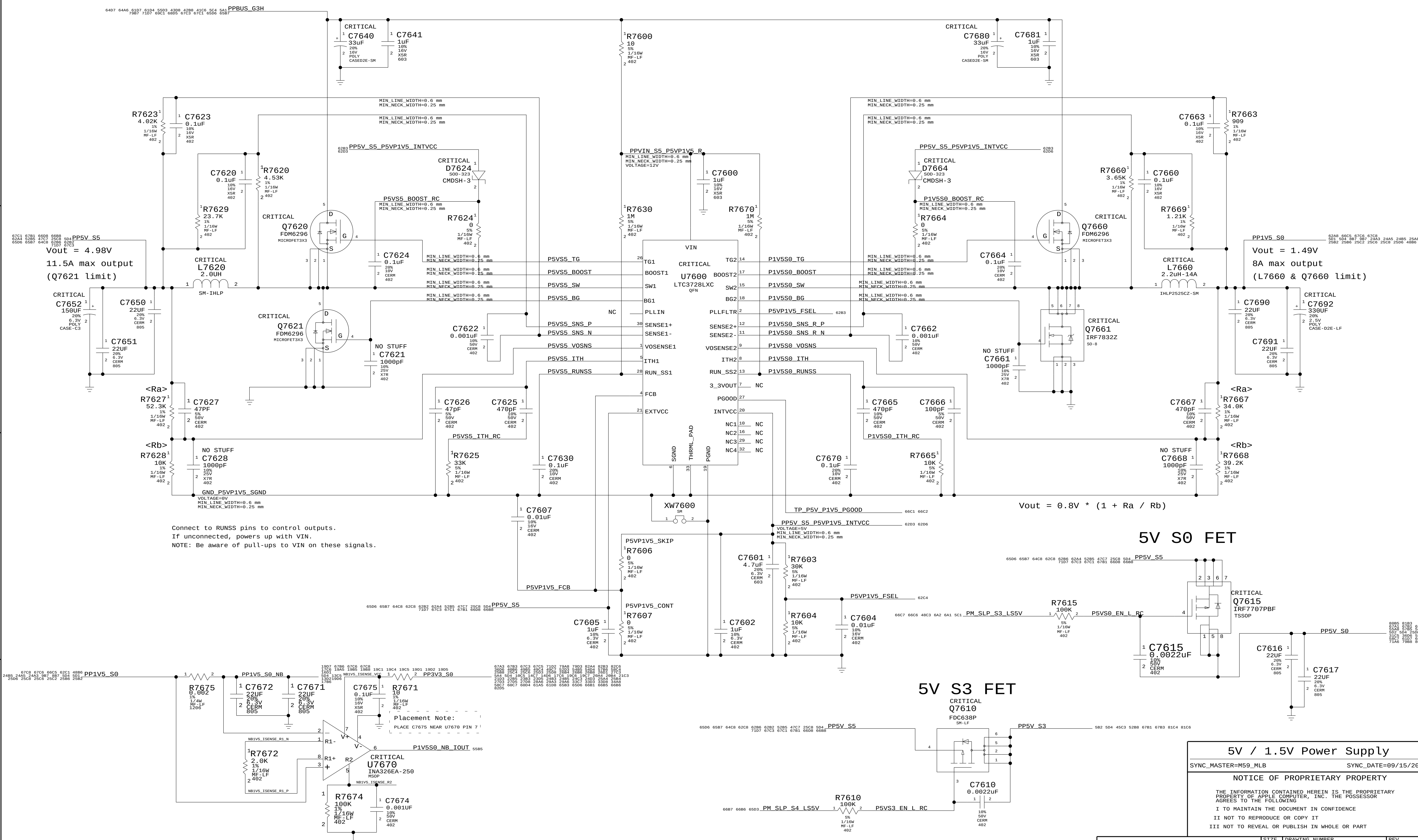
CPU VCore Current Sense

IMVP6 CPU VCore Regulator

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 61 OF 87	


PPBUS_G3H
CRITICAL
C7640
33uF
C7641
1uF
R7600
10
C7680
33uF
C7681
1uF
R7623
4.02K
C7623
0.1uF
C7663
0.1uF
R7663
909
PP5V_S5_P5VP1V5_INTVCC
PPVIN_S5_P5VP1V5_R
VOLTAGE=12V
C7620
0.1uF
R7620
4.53K
D7624
CMDSH-3
C7600
1uF
D7664
CMDSH-3
R7660
3.65K
C7660
0.1uF
R7629
23.7K
P5VS5_BOOST_RC
R7624
0
Q7620
FDM6296
R7630
1M
R7670
1M
P1V5S0_BOOST_RC
R7664
0
R7669
1.21K
Q7660
FDM6296
PP5V_S5
Vout = 4.98V
11.5A max output
(Q7621 limit)
C7624
0.1uF
C7664
0.1uF
PP1V5_S0
Vout = 1.49V
8A max output
(L7660 & Q7660 limit)
L7620
2.0UH
SM-IHLP
L7660
2.2uH-14A
IHLP2525CZ-SM
VIN
U7600
LTC3728LXC
QFN
P5VS5_TG
P5VS5_BOOST
P5VS5_SW
P5VS5_BG
P5VS5_SNS_P
P5VS5_SNS_N
P5VS5_VOSNS
P5VS5_ITH
P5VS5_RUNSS
TG1
BOOST1
SW1
BG1
PLLIN
SENSE1+
SENSE1-
VOSENSE1
ITH1
RUN_SS1
FCB
EXTVCC
TG2
BOOST2
SW2
BG2
PLLFLTR
SENSE2+
SENSE2-
VOSENSE2
ITH2
RUN_SS2
3_3VOUT
PGOOD
INTVCC
NC1
NC2
NC3
NC4
SGND
THRML_PAD
PGND
P1V5S0_TG
P1V5S0_BOOST
P1V5S0_SW
P1V5S0_BG
P5VP1V5_FSEL
P1V5S0_SNS_R_P
P1V5S0_SNS_R_N
P1V5S0_VOSNS
P1V5S0_ITH
P1V5S0_RUNSS
C7652
150UF
C7650
22UF
C7651
22UF
Q7621
FDM6296
C7621
1000pF
NO STUFF
C7622
0.001uF
C7662
0.001uF
Q7661
IRF7832Z
C7661
1000pF
C7690
22UF
C7692
330UF
C7691
22UF
<Ra>
R7627
52.3K
C7627
47PF
C7626
47pF
C7625
470pF
C7665
470pF
C7666
100pF
C7667
470pF
R7667
34.0K
P5VS5_ITH_RC
P1V5S0_ITH_RC
<Rb>
R7628
10K
C7628
1000pF
R7625
33K
C7630
0.1uF
C7670
0.1uF
R7665
10K
C7668
1000pF
R7668
39.2K
GND_P5VP1V5_SGND
VOLTAGE=0V
XW7600
TP_P5V_P1V5_PGOOD
Vout = 0.8V * (1 + Ra / Rb)
C7607
0.01uF
Connect to RUNSS pins to control outputs.
If unconnected, powers up with VIN.
NOTE: Be aware of pull-ups to VIN on these signals.
PP5V_S5_P5VP1V5_INTVCC
VOLTAGE=5V
P5VP1V5_SKIP
R7606
0
C7601
4.7uF
R7603
30K
5V S0 FET
P5VP1V5_FCB
P5VP1V5_FSEL
PP5V_S5
R7607
0
R7615
100K
PM_SLP_S3_LS5V
P5VS0_EN_L_RC
Q7615
IRF7707PBF
TSSOP
C7605
1uF
C7602
1uF
R7604
10K
C7604
0.01uF
C7615
0.0022uF
PP5V_S0
C7616
22UF
C7617
22UF
PP1V5_S0
R7675
0.002
PP1V5_S0_NB
C7672
22UF
C7671
22UF
C7675
0.1uF
R7671
10
PP3V3_S0
Placement Note:
PLACE C7675 NEAR U7670 PIN 7
5V S3 FET
Q7610
FDC638P
PP5V_S3
NB1V5_ISENSE_R1_N
R7672
2.0K
U7670
INA326EA-250
MSOP
P1V5S0_NB_IOUT
NB1V5_ISENSE_R1_P
NB1V5_ISENSE_R2
R7674
100K
C7674
0.001uF
C7610
0.0022uF
R7610
100K
PM_SLP_S4_LS5V
P5VS3_EN_L_RC

5V / 1.5V Power Supply

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

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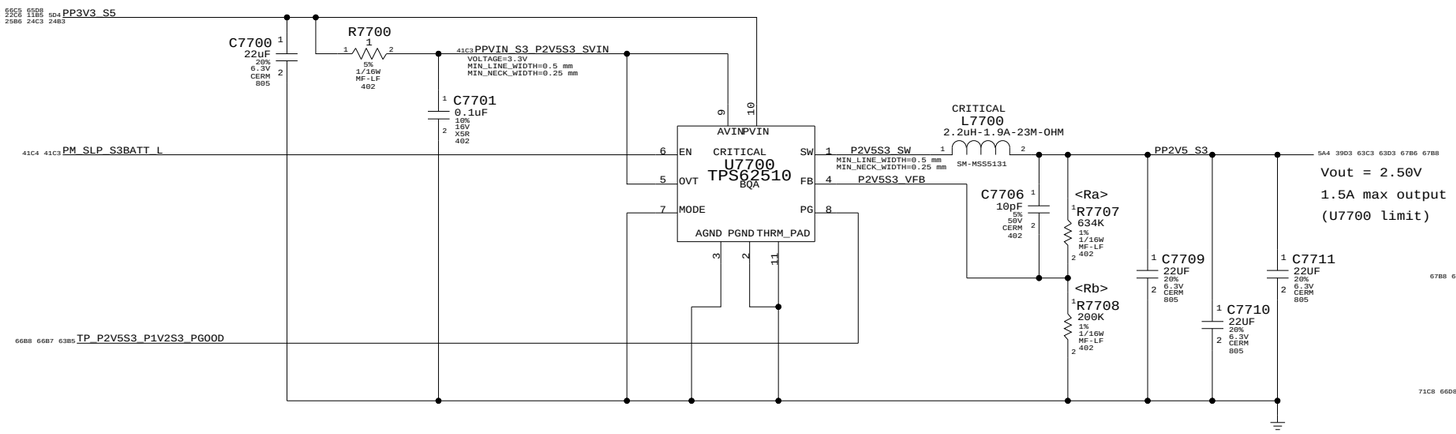
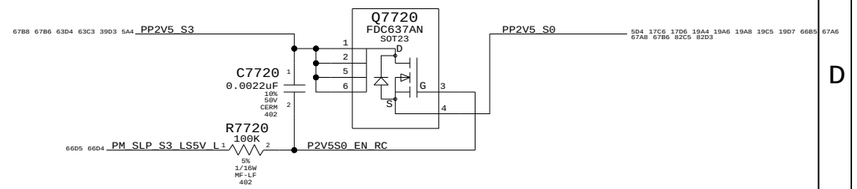
SCALE NONE	SHT 62	OF 87

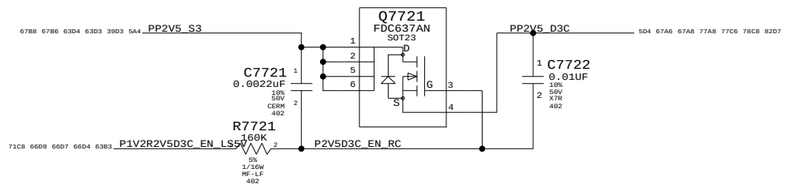
2.5V S3 Regulator



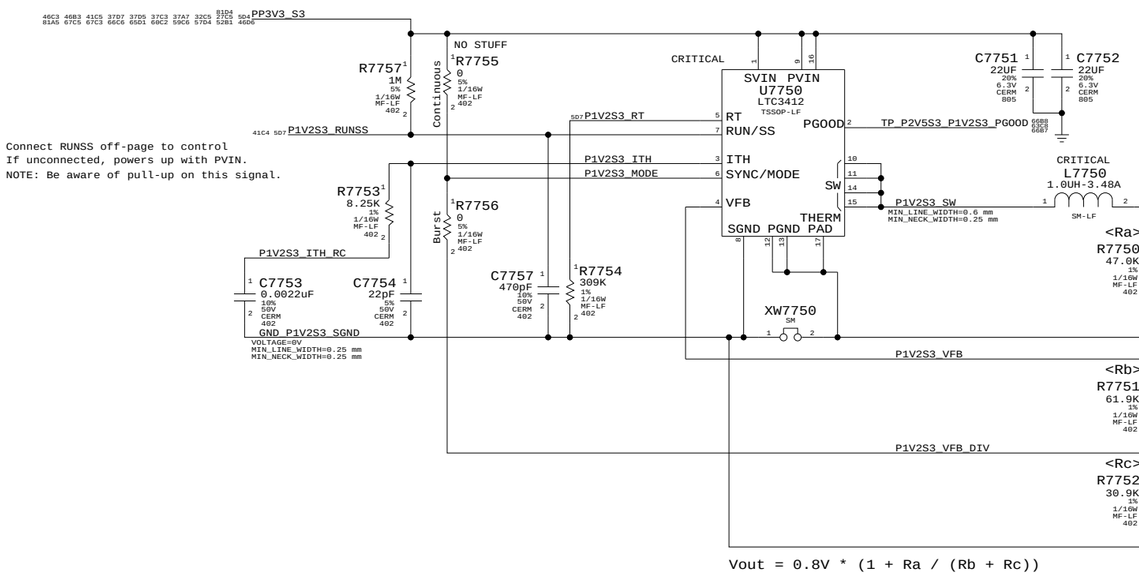
2.5V S0 FET



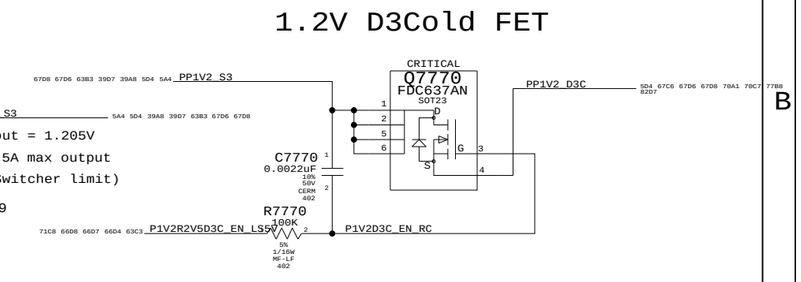
2.5V D3Cold FET



1.2V S3 Regulator



1.2V D3Cold FET

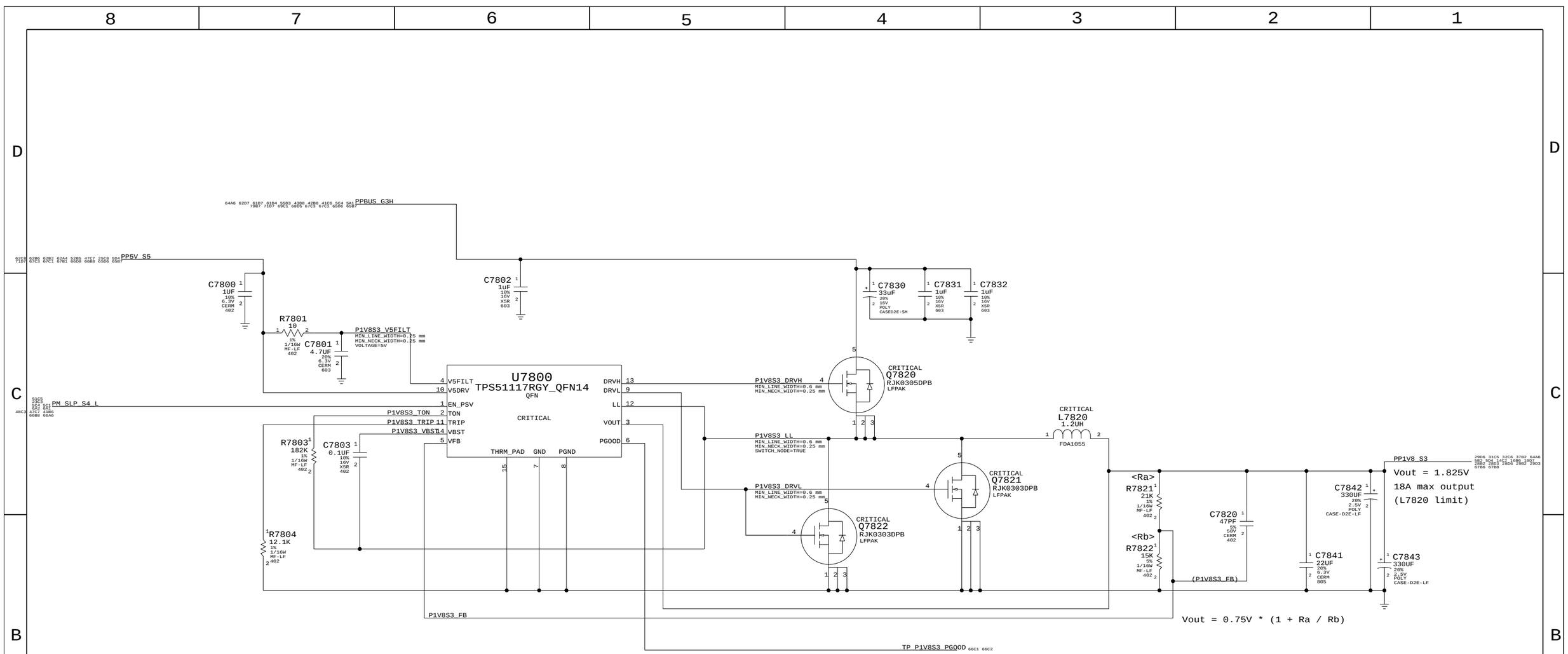


2.5V & 1.2V Regulators

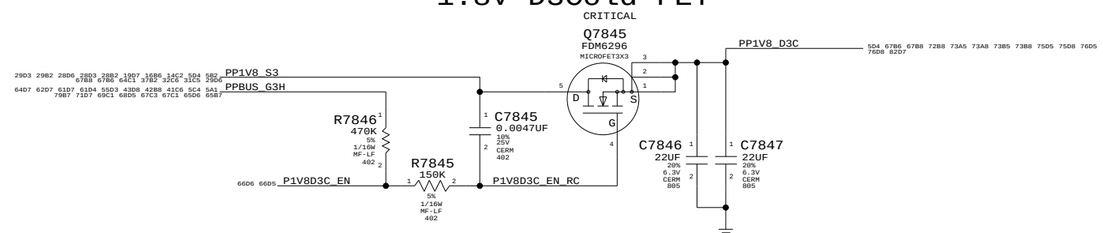
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 63 OF 87	



1.8V D3Cold FET



1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

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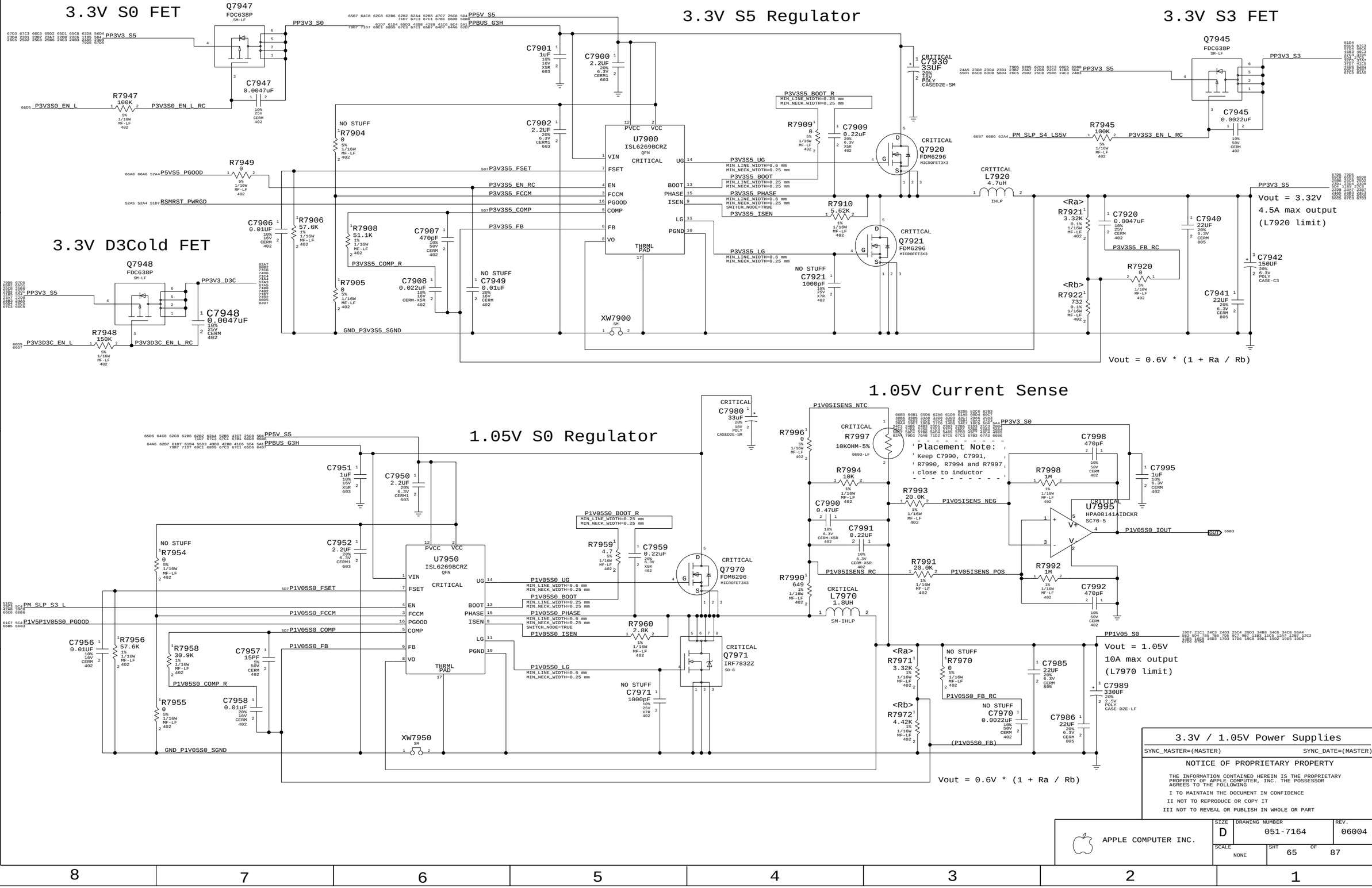
D	051-7164	06004

SCALE	SHT	OF
NONE	64	87


3.3V S0 FET
Q7947
FDC638P
SM-LF
PP3V3_S0
PP3V3_S5
P3V3S0_EN_L
R7947
100K
5%
1/16W
MF-LF
402
P3V3S0_EN_L_RC
C7947
0.0047uF
10%
25V
CERM
402
3.3V S5 Regulator
PP5V_S5
PPBUS_G3H
C7901
1uF
10%
16V
X5R
603
C7900
2.2UF
20%
6.3V
CERM1
603
C7902
2.2UF
20%
6.3V
CERM1
603
NO STUFF
R7904
0
5%
1/16W
MF-LF
402
U7900
ISL6269BCRZ
QFN
CRITICAL
PVCC
VCC
VIN
FSET
EN
FCCM
PGOOD
COMP
FB
VO
THRML
PAD
UG
BOOT
PHASE
ISEN
LG
PGND
P3V3S5_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R7909
0
C7909
0.22uF
20%
6.3V
X5R
402
CRITICAL
C7930
33UF
20%
16V
POLY
CASED2E-SM
CRITICAL
Q7920
FDM6296
MICROFET3X3
P3V3S5_UG
P3V3S5_BOOT
P3V3S5_PHASE
P3V3S5_ISEN
P3V3S5_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
R7910
5.62K
1%
1/16W
MF-LF
402
CRITICAL
Q7921
FDM6296
MICROFET3X3
NO STUFF
C7921
1000pF
10%
25V
X7R
402
CRITICAL
L7920
4.7uH
IHLP
3.3V S3 FET
Q7945
FDC638P
SM-LF
PP3V3_S3
PP3V3_S5
R7945
100K
5%
1/16W
MF-LF
402
PM_SLP_S4_LS5V
P3V3S3_EN_L_RC
C7945
0.0022uF
10%
50V
CERM
402
3.3V D3Cold FET
Q7948
FDC638P
SM-LF
PP3V3_D3C
PP3V3_S5
C7948
0.0047uF
10%
25V
CERM
402
R7948
150K
5%
1/16W
MF-LF
402
P3V3D3C_EN_L
P3V3D3C_EN_L_RC
R7906
57.6K
1%
1/16W
MF-LF
402
C7906
0.01UF
10%
16V
CERM
402
R7908
51.1K
1%
1/16W
MF-LF
402
C7907
470pF
10%
50V
CERM
402
P3V3S5_COMP_R
R7905
0
5%
1/16W
MF-LF
402
C7908
0.022uF
10%
16V
CERM-X5R
402
NO STUFF
C7949
0.01uF
20%
16V
CERM
402
XW7900
SM
GND_P3V3S5_SGND
R7949
0
5%
1/16W
MF-LF
402
P5VS5_PGOOD
RSMRST_PWRGD
P3V3S5_FSET
P3V3S5_EN_RC
P3V3S5_FCCM
P3V3S5_COMP
P3V3S5_FB
<Ra>
R7921
3.32K
0.1%
1/16W
MF-LF
402
<Rb>
R7922
732
0.1%
1/16W
MF-LF
402
C7920
0.0047uF
10%
25V
CERM
402
P3V3S5_FB_RC
R7920
0
5%
1/16W
MF-LF
402
C7940
22UF
20%
6.3V
CERM
805
C7942
150UF
20%
6.3V
POLY
CASE-C3
C7941
22UF
20%
6.3V
CERM
805
Vout = 3.32V
4.5A max output
(L7920 limit)
Vout = 0.6V * (1 + Ra / Rb)
1.05V Current Sense
1.05V S0 Regulator
CRITICAL
C7980
33uF
20%
16V
POLY
CASED2E-SM
PP5V_S5
PPBUS_G3H
C7951
1uF
10%
16V
X5R
603
C7950
2.2UF
20%
6.3V
CERM1
603
C7952
2.2UF
20%
6.3V
CERM1
603
NO STUFF
R7954
0
5%
1/16W
MF-LF
402
U7950
ISL6269BCRZ
QFN
CRITICAL
PVCC
VCC
VIN
FSET
EN
FCCM
PGOOD
COMP
FB
VO
THRML
PAD
UG
BOOT
PHASE
ISEN
LG
PGND
P1V05S0_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R7959
4.7
5%
1/16W
MF-LF
402
C7959
0.22uF
20%
6.3V
X5R
402
CRITICAL
Q7970
FDM6296
MICROFET3X3
P1V05S0_UG
P1V05S0_BOOT
P1V05S0_PHASE
P1V05S0_ISEN
P1V05S0_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
R7960
2.8K
1%
1/16W
MF-LF
402
CRITICAL
Q7971
IRF7832Z
SO-8
NO STUFF
C7971
1000pF
10%
25V
X7R
402
XW7950
SM
GND_P1V05S0_SGND
P1V5P1V05S0_PGOOD
P1V05S0_FSET
P1V05S0_FCCM
P1V05S0_COMP
P1V05S0_FB
C7956
0.01UF
10%
16V
CERM
402
R7956
57.6K
1%
1/16W
MF-LF
402
R7958
30.9K
1%
1/16W
MF-LF
402
P1V05S0_COMP_R
C7957
15PF
5%
50V
CERM
402
R7955
0
5%
1/16W
MF-LF
402
C7958
0.01uF
20%
16V
CERM
402
P1V05ISENS_NTC
R7996
0
5%
1/16W
MF-LF
402
CRITICAL
R7997
10KOHM-5%
0603-LF
R7994
10K
1%
1/16W
MF-LF
402
C7990
0.47UF
10%
6.3V
CERM-X5R
402
C7991
0.22UF
10%
6.3V
CERM-X5R
402
R7990
649
1%
1/16W
MF-LF
402
CRITICAL
L7970
1.8UH
SM-IHLP
Placement Note:
Keep C7990, C7991,
R7990, R7994 and R7997
close to inductor
R7993
20.0K
1%
1/16W
MF-LF
402
R7991
20.0K
1%
1/16W
MF-LF
402
P1V05ISENS_NEG
P1V05ISENS_RC
P1V05ISENS_POS
PP3V3_S0
C7998
470pF
10%
50V
CERM
402
R7998
1M
1%
1/16W
MF-LF
402
C7995
1uF
10%
6.3V
CERM
402
CRITICAL
U7995
HPA00141AIDCKR
SC70-5
P1V05S0_IOUT
OUT
R7992
1M
1%
1/16W
MF-LF
402
C7992
470pF
10%
50V
CERM
402
<Ra>
R7971
3.32K
1%
1/16W
MF-LF
402
<Rb>
R7972
4.42K
1%
1/16W
MF-LF
402
NO STUFF
R7970
0
5%
1/16W
MF-LF
402
P1V05S0_FB_RC
(P1V05S0_FB)
NO STUFF
C7970
0.0022uF
10%
50V
CERM
402
C7985
22UF
20%
6.3V
CERM
805
C7986
22UF
20%
6.3V
CERM
805
C7989
330UF
20%
2.5V
POLY
CASE-D2E-LF
PP1V05_S0
Vout = 1.05V
10A max output
(L7970 limit)
Vout = 0.6V * (1 + Ra / Rb)
3.3V / 1.05V Power Supplies
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-7164
REV.
06004
SCALE
NONE
SHT
65
OF
87

Power Control Signals

PP5V_S5

R8050 10K 5% 1/16W MF-LF 402

R8051 10K 5% 1/16W MF-LF 402

R8052 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

R8068 10K 5% 1/16W MF-LF 402

R8069 10K 5% 1/16W MF-LF 402

P1V2R2V5D3C_EN_LS5V

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V (MAKE_BASE=TRUE)

P1V2R2V5D3C_EN_LS5V

P1V2R2V5D3C_EN_LS5V

P3V3D3C_EN_L (MAKE_BASE=TRUE)

P3V3D3C_EN_L

P1V8D3C_EN (MAKE_BASE=TRUE)

P1V8D3C_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363

Q8056 2N7002DW-X-F SOT-363

Q8050 2N7002DW-X-F SOT-363

PM_SLP_S3_L_LS5V (MAKE_BASE=TRUE)

PM_SLP_S3_L_LS5V

P3V3S0_EN_L (MAKE_BASE=TRUE)

P3V3S0_EN_L

Q8058 2N7002DW-X-F SOT-363

Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE)

PM_SLP_S3_LS5V

PM_SLP_S3_LS5V

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363

R8054 100K 5% 1/16W MF-LF 402

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

PM_SLP_S3_L

R8056 100K 5% 1/16W MF-LF 402

Q8057 2N7002DW-X-F SOT-363

PP3V3_S3

(PM_SLP_S3_L) MAKE_BASE=TRUE

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PP3V3_S0

R8053 10K 5% 1/16W MF-LF 402

R8081 10K 5% 1/16W MF-LF 402

C8081 0.1uF 20% 10V CERM 402

PM_SLP_S3_L_GPUVCORE_EN

C8053 0.047UF 10% 10V CERM 402

SB_GPUVCORE_DISABLE_L (MAKE_BASE=TRUE)

U8081 MC74VHC1G08 SC70

GPUVCORE_EN (MAKE_BASE=TRUE)

GPUVCORE_EN

TP_P2V5S3_P1V2S3_PGOOD

TP_P2V5S3_P1V2S3_PGOOD (MAKE_BASE=TRUE)

This signal was used as an option previously to test for 2v5 and 1v2 S3 valid for GPUVCORE_EN. But was disconnected for C8053 placement.

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

PP5V_S5

R8055 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE)

PM_SLP_S4_LS5V

PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L

R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) MAKE_BASE=TRUE

PM_SLP_S4_L

PM_SLP_S4_L

PM_SLP_S4_L

PP3V42_G3H

P5VS5_PGOOD

(P5VS5_PGOOD) MAKE_BASE=TRUE

P5VS5_PGOOD

P5VS5_RUNSS

5V Enable has pull-up to PBUS

R8059 470K 5% 1/16W MF-LF 402

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN

R8058 100K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PPDCIN_G3H

C8000 10UF 10% 25V X5R 1206-1

P3V42G3H5_BOOST

U8000 LT3470 TSOT23-8

VIN BOOST SW BIAS FB GND SHDN* NC NC CRITICAL

P3V42G3H_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE

C8005 0.22uF 20% 6.3V X5R 402

CRITICAL L8010 33uH CDPH4D19F-SM

PP3V42_G3H

Vout = 3.425

200mA max output (Switcher limit)

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402

<Rb> R8011 200K 1% 1/16W MF-LF 402

C8015 22UF 20% 6.3V CERM 805

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5

PP1V5_S0

R8061 27.4K 1% 1/16W MF-LF 402

R8063 4.99K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 10V CERM 402

0.89V Reference

P1V0_P1V5PG_REF

U8060 LMC7211 SM-LF

P1V5S0_COMP_POS

P1V5S0_PGOOD

R8062 10K 1% 1/16W MF-LF 402

R8064 10K 1% 1/16W MF-LF 402

R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

P1V5P1V05S0_PGOOD

P1V5P1V05S0_PGOOD

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)

NOTE: R8065 acts as 10K pull-up for PGOOD signal

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

PP3V3_S0

PP5V_S0

PP2V5_S0

PP0V9_S0

R8074 68.1K 1% 1/16W MF-LF 402

R8072 365K 1% 1/16W MF-LF 402

R8070 845K 1% 1/16W MF-LF 402

C8070 0.1uF 20% 10V CERM 402

U8070 LTC2903 TSOT-23

CRITICAL V1

S0PGOOD_5V_DIV

S0PGOOD_2V5_DIV

S0PGOOD_0V9_DIV

RST*

GND

R8076 10K 5% 1/16W MF-LF 402

S0PGOOD_PWROK

R8075 100K 1% 1/16W MF-LF 402

C8075 0.1UF 20% 10V CERM 402

R8073 100K 1% 1/16W MF-LF 402

C8073 0.1UF 20% 10V CERM 402

R8071 100K 1% 1/16W MF-LF 402

C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)

TP_P5V_P1V5_PGOOD

TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

TP_P1V8S3_PGOOD

PP3V3_S0

MC74VHC1G08 SC70 U8080

ALL_SYS_PWRGD

PGOOD_MUXED_S0_OR_S0D3C

C8080 0.1UF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

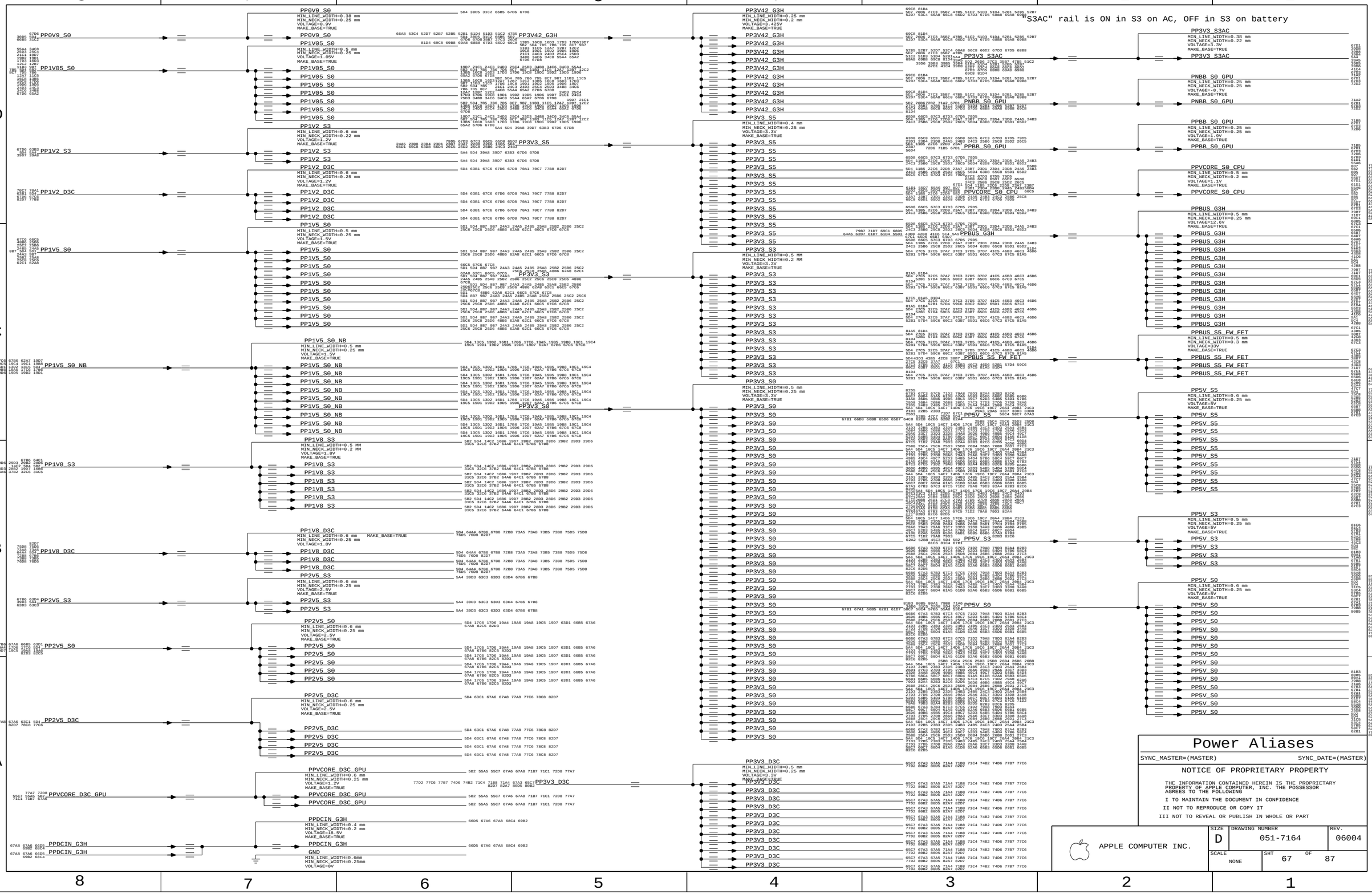
SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

SHT 66 OF 87


"S3AC" rail is ON in S3 on AC, OFF in S3 on battery
PP0V9_S0
PP1V05_S0
PP1V2_S3
PP1V2_D3C
PP1V5_S0
PP1V5_S0_NB
PP1V8_S3
PP1V8_D3C
PP2V5_S3
PP2V5_S0
PP2V5_D3C
PPVCORE_D3C_GPU
PPDCIN_G3H
GND
PP3V2_G3H
PP3V3_S5
PP3V3_S3
PP3V3_S0
PP3V3_D3C
PP3V3_S3AC
PNBB_S0_GPU
PPBB_S0_GPU
PPVCORE_S0_CPU
PPBUS_G3H
PPBUS_S5_FW_FET
PP5V_S5
PP5V_S3
PP5V_S0
Power Aliases
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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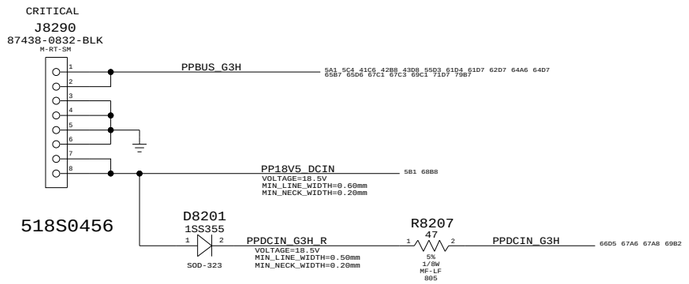
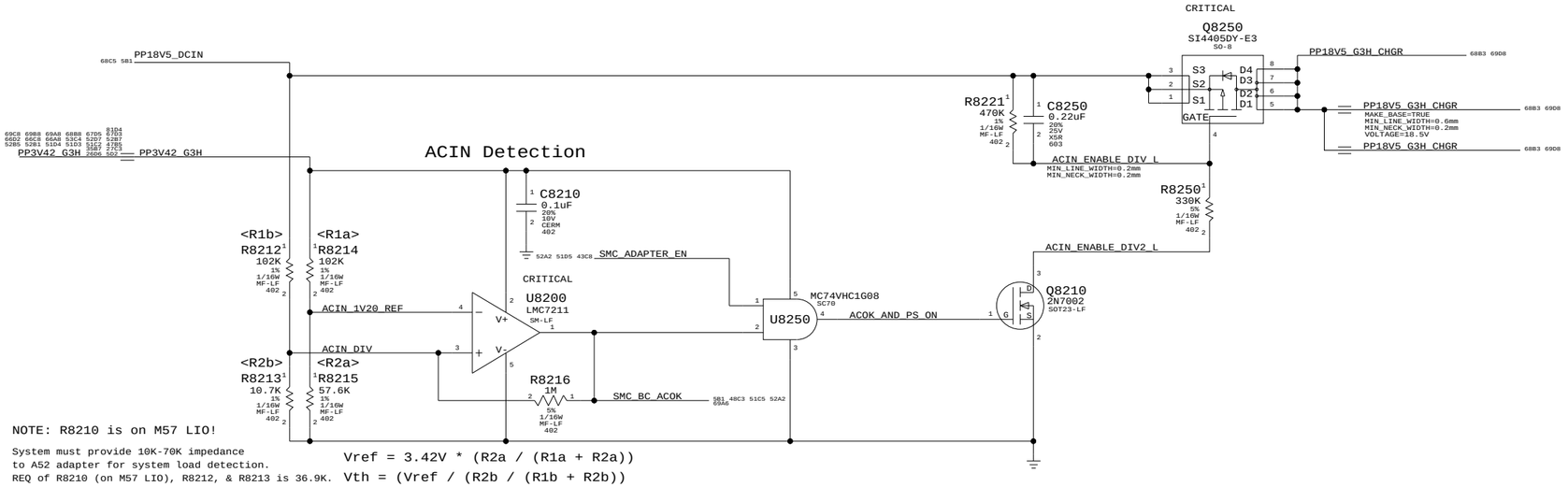
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7164
REV. 06004
SCALE NONE
SHT 67 OF 87

DC-In Connector



Inrush Limiter



NOTE: R8210 is on M57 LIO!

System must provide 10K-70K impedance
to A52 adapter for system load detection.
REQ of R8210 (on M57 LIO), R8212, & R8213 is 36.9K.

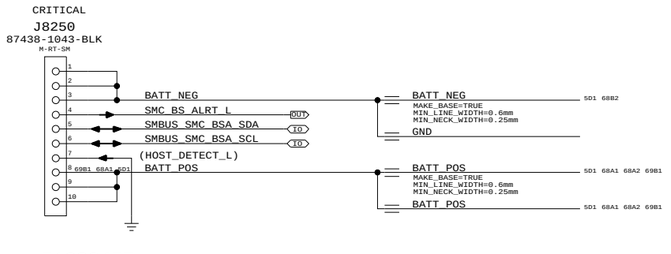
Vref = 3.42V * (R2a / (R1a + R2a))
Vth = (Vref / (R2b / (R1b + R2b))

Vref = 1.23V

Vth = 13.0V

Assuming 1% variance for R8210-R8215 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

Battery Connector



DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	68	87

PBus Supply & Battery Charger

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H,BATT CHGR,28P,QFN,LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM,5%,1/16W,0402,SMD,LF	R8304		ISL6257H

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

Battery Charge FET

Adapter Input Current Limit

As shown, Isys =~4.6A max

Battery Charge Current Limit

As shown, Icng = 3.3A max

10A MAX, LIMITED BY L8300, Q8301

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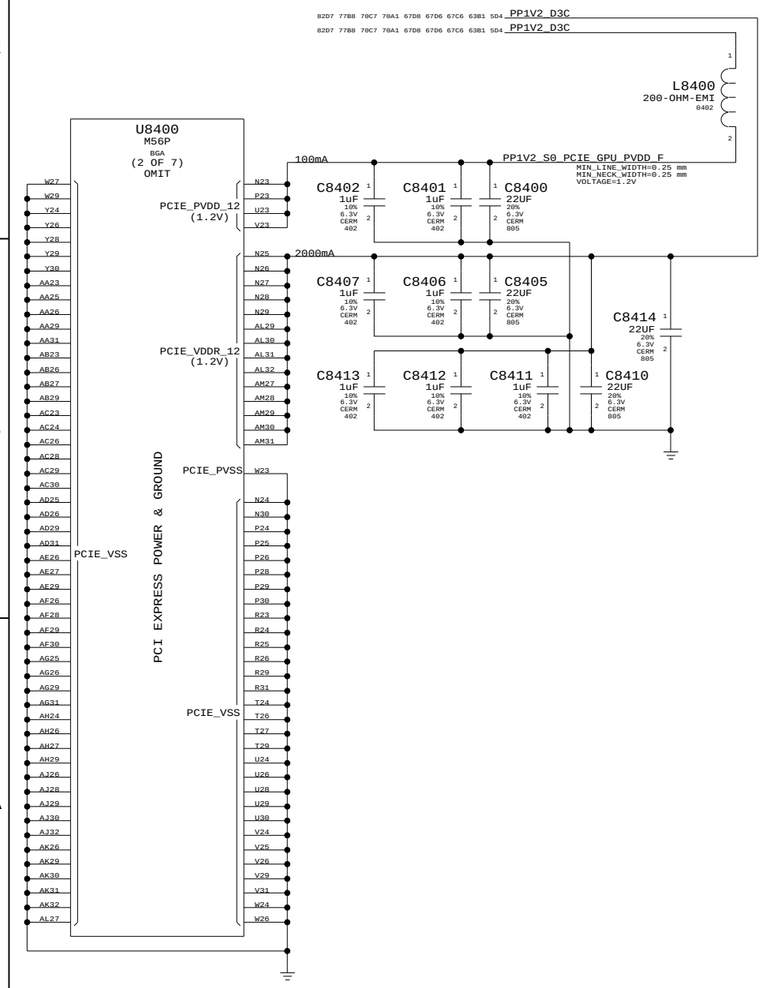
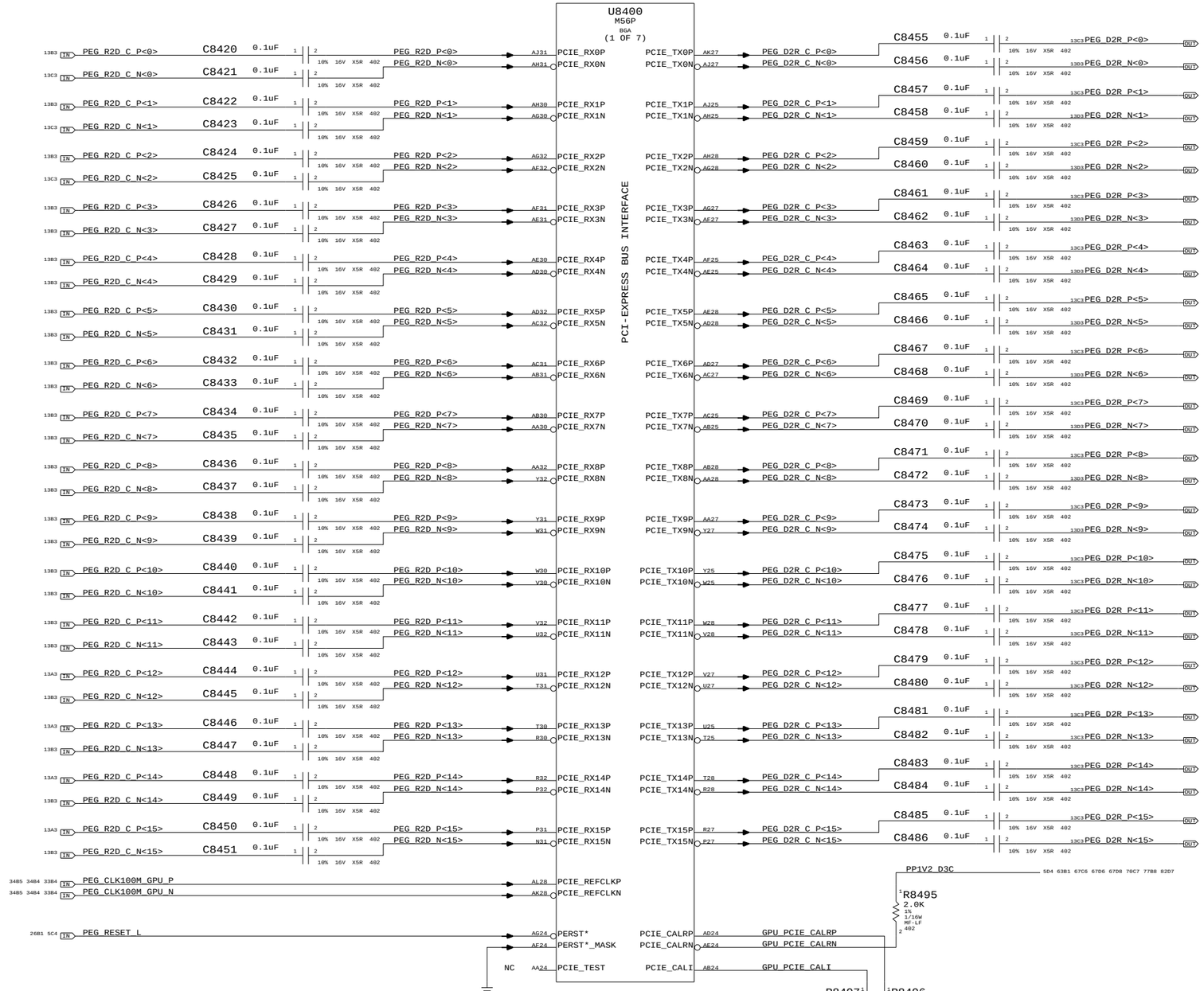
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 69 OF 87	





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

SHT 70 OF 87

GPU VCore Supply

PP5V_S5
PPBUS_G3H

C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM1 603
C8502 2.2UF 20% 6.3V CERM1 603

R8504 0 5% 1/16W MF-LF 402

U8500 ISL62698CRZ QFN
CRITICAL
PAD THRML 17

1	VIN	UG	14
7	FSET	BOOT	13
4	EN	PHASE	15
3	FCCM	ISEN	9
16	PGOOD	LG	11
5	COMP	PGND	10
6	FB		
8	VO		
12	PVCC		
2	VCC		

GPUVCORE_EN
P1V2R2V5D3C_EN_LS5V
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB

R8508 150K 1% 1/16W MF-LF 402
C8507 15pF 5% 50V CERM 402
GPUVCORE_COMP_R
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
NO STUFF R8505 0 5% 1/16W MF-LF 402
C8508 470pF 10% 50V CERM 402
GND_GPUVCORE_SGND

XW8500 SM
XW8501 SM
XW8502 SM

GPUVCORE_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R8509 4.7 5% 1/16W MF-LF 402
C8509 0.22UF 20% 6.3V XSR 402
Stuff 4.7ohm for decreased Slew rate

GPUVCORE_UG
GPUVCORE_BOOT
GPUVCORE_PHASE
GPUVCORE_ISEN
GPUVCORE_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

R8510 5.11K 1% 1/16W MF-LF 402

CRITICAL Q8520 RJK0305DPB LFPAK
CRITICAL Q8521 RJK0301DPB LFPAK
CRITICAL Q8522 RJK0301DPB LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
NO STUFF C8521 1000pF 10% 25V X7R 402

CRITICAL C8530 33uF 20% 16V POLY CASED2E-SM

GND_GPUVCORE_PGND

GPU VCore Current Sense

GPUISENS_NTC
PP3V3_S0

CRITICAL R8597 10KOHM-5% 0603-LF
NO STUFF R8594 1K 1% 1/16W MF-LF 402
R8596 1K 1% 1/16W MF-LF 402

Placement Note:
Keep C8590, C8591
R8590, R8594 and R8597
close to inductor

C8598 470pF 10% 50V CERM 402
C8595 1uF 10% 6.3V CERM 402
R8598 1M 1% 1/16W MF-LF 402

R8593 20.0K 1% 1/16W MF-LF 402
GPUISENS_NEG
C8590 0.47UF 10% 6.3V CERM-XSR 402
C8591 0.22UF 10% 6.3V CERM-XSR 402

CRITICAL U8595 HPA00141AIDCKR SC70-5
GPUVCORE_IOUT

R8591 20.0K 1% 1/16W MF-LF 402
GPUISENS_RC
GPUISENS_POS
R8590 649 1% 1/16W MF-LF 402
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402

CRITICAL L8520 1.2UH FDA1055

PPVCORE_D3C_GPU
Vout = 1.10V / 0.95V
18A max output
(L8520 limit)

<Ra> R8521 3.01K 1% 1/16W MF-LF 402
NO STUFF R8520 0 5% 1/16W MF-LF 402
GPUVCORE_FB_RC
<Rb> R8522 5.11K 1% 1/16W MF-LF 402
(GPUVCORE_FB)
NO STUFF C8520 0.0022uF 10% 50V CERM 402
C8540 22UF 20% 6.3V CERM 805
C8542 330UF 20% 2.5V POLY CASE-D2E-LF
C8541 22UF 20% 6.3V CERM 805
C8543 330UF 20% 2.5V POLY CASE-D2E-LF

<Rc> R8523 7.32K 1% 1/16W MF-LF 402
GPUVCORE_FB_LOW

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

PP3V3_D3C
R8526 10K 5% 1/16W MF-LF 402
R8525 10K 5% 1/16W MF-LF 402
GPU_VCORE_HIGH
GPU_VCORE_HIGH_RC
Q8523 2N7002DW-X-F SOT-363
C8523 0.022uF 10% 16V CERM-XSR 402
GPU_VCORE_LOW
R8524 10K 5% 1/16W MF-LF 402

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

Q8575 SI3446DV TSOP-LF
PPVCORE_D3C_GPU
GPUBB_EN_L

CRITICAL U8550 FAN2558 SOT23-6-LF

1	VIN	VOUT	6
4	PG		
3	EN	ADJ	5
2	GND		

PP3V3_D3C
GPUBB_EN
C8551 2.2uF 20% 6.3V CERM1 603
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22UF 20% 6.3V CERM 805
PPBB_S0_GPU
GPUBBP_ADJ
NO STUFF R8554 174K 1% 1/16W MF-LF 402
<Rb> R8556 16.2K 1% 1/16W MF-LF 402
<Rc>
C8557 22UF 20% 6.3V CERM 805

Vout = (1.58V /) 1.50V
180mA max output
(LDO limit)

GPUBBP_ADJ_LOW
NO STUFF Q8554 2N7002 SOT23-LF
GPU_VCORE_HIGH

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

PP5V_S0
R8570 4.7K 1% 1/16W MF-LF 402
GPUBB_EN_L
GPU_BB_CTL
R8561 0 5% 1/16W MF-LF 402
GPU_GENERICD
GPUBB_EN
Q8570 2N7002 SOT23-LF
NO STUFF C8570 0.0022uF 10% 50V CERM 402
R8560 10K 5% 1/16W MF-LF 402

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

For proper M56 power sequence, this pull-up must be powered before VCore

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.

PP3V3_D3C
C8580 10uF 20% 6.3V X5R 603
GPUBB_EN

U8580 MAX1673 SOI
CRITICAL

4	SHDN_L	IN	8
	GPUBBN_CAPP	CAP+	2
	GPUBBN_CAPN	CAP-	3
1	LIN/SKIP_L	GND	7
	FB		6
	OUT		5

MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
C8581 2.2uF 20% 6.3V CERM1 603

<Ra> R8587 68.1K 1% 1/16W MF-LF 402
GPUBBN_FB
<Rb> R8588 11.3K 1% 1/16W MF-LF 402
C8589 22UF 20% 6.3V CERM 805
PNBB_S0_GPU

Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA

Vout = -0.55V
125mA max output
(Regulator limit)

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

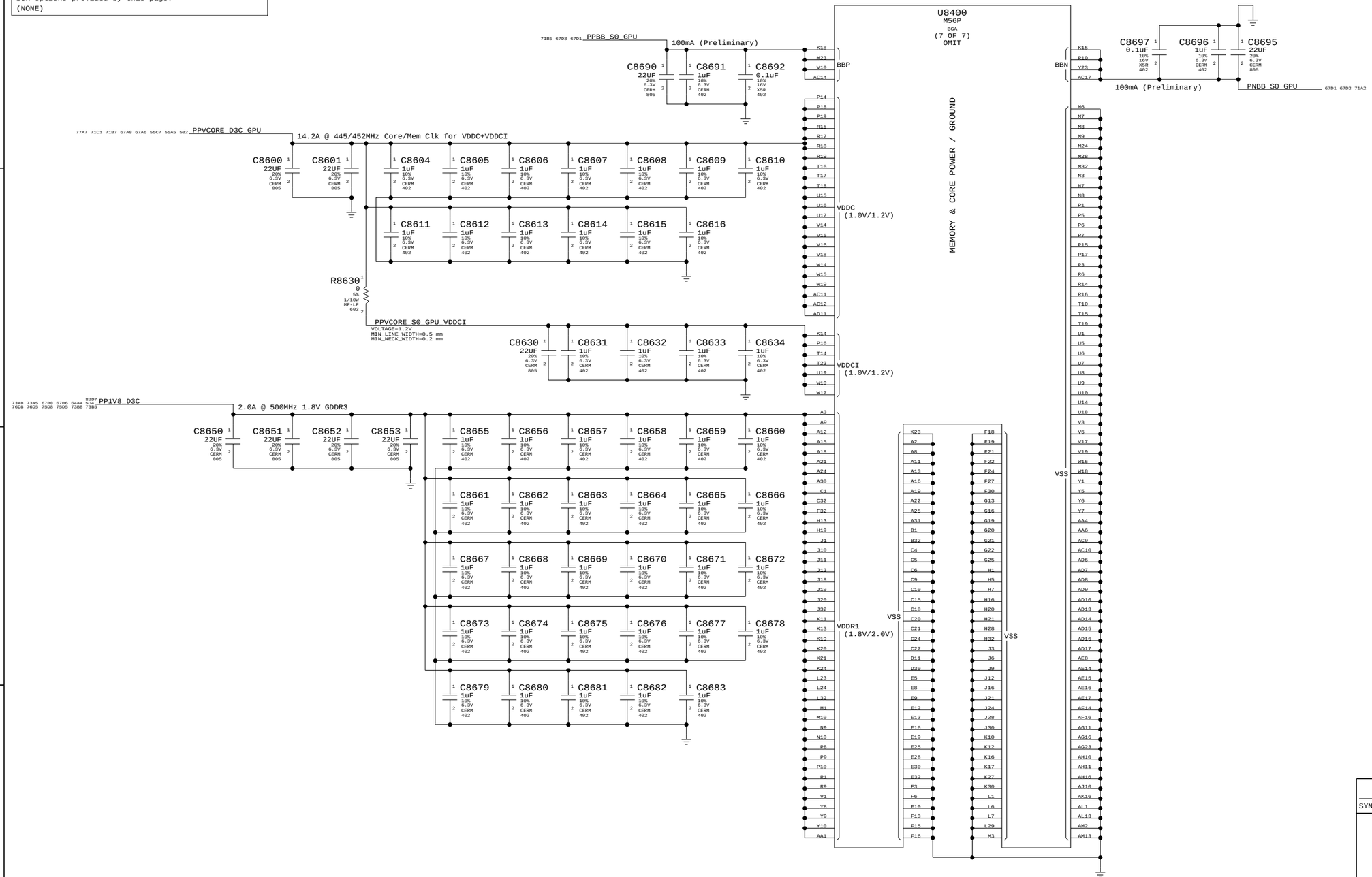
SCALE: NONE SHT 71 OF 87

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

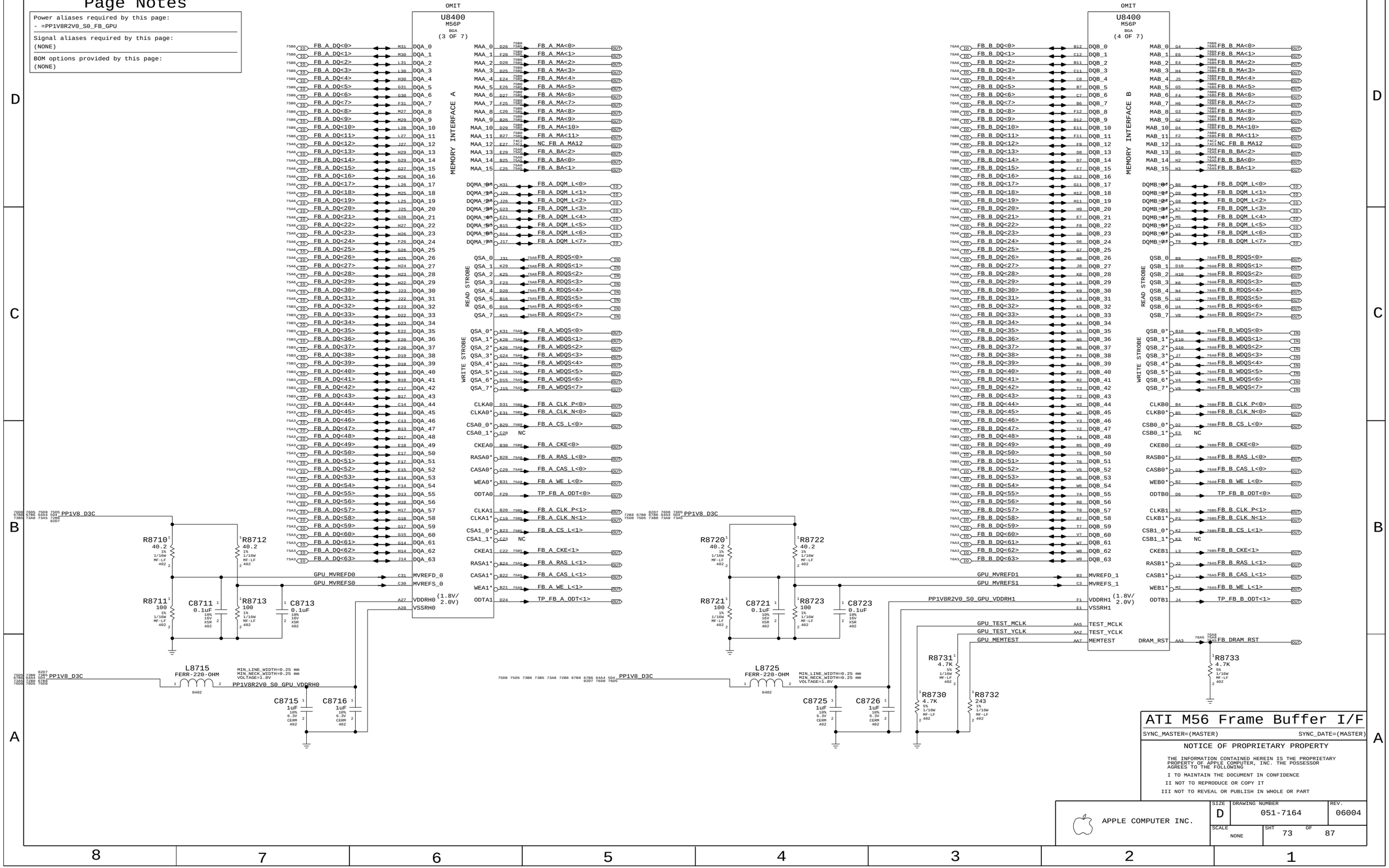
SCALE	SHT	OF
NONE	72	87

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	73	87

ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

77D2 77C6 77B7 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8800 10K 5% 1/16W MF-LF 402
NO STUFF R8802 10K 5% 1/16W MF-LF 402
NO STUFF R8804 10K 5% 1/16W MF-LF 402
NO STUFF R8806 10K 5% 1/16W MF-LF 402
NO STUFF R8809 10K 5% 1/16W MF-LF 402
GPU_MEM_256M R8812 10K 5% 1/16W MF-LF 402
GPU_MEM_256M R8824 10K 5% 1/16W MF-LF 402

GPU_DEEPMH_EN R8801 10K 5% 1/16W MF-LF 402
NO STUFF R8803 10K 5% 1/16W MF-LF 402
R8805 10K 5% 1/16W MF-LF 402
NO STUFF R8808 10K 5% 1/16W MF-LF 402
GPU_MEM_64M R8813 10K 5% 1/16W MF-LF 402
NO STUFF R8811 10K 5% 1/16W MF-LF 402
GPU_MEM_NOT_SAM R8827 10K 5% 1/16W MF-LF 402

		Serial ROM	TestBus	Misc	Straps
77D3	GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb
77D3	GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN
77D3	GPU_GPIO_2		TESTIN[2]		Reserved
77D3	GPU_GPIO_3		TESTIN[3]		Reserved
77D3	GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS
77D3	GPU_GPIO_5		TESTIN[5]		Reserved
77D3	GPU_GPIO_6		TESTIN[6]		Reserved
82A4 77D3 74C5	GPU_BLON	ENA_BL	TESTIN[7]		
77D3	GPU_GPIO_8	ROMSO	TESTWR		Reserved
77C3	GPU_GPIO_9	IPD	ROMSI		ROMIDCFG[3]
77C3 74C5	TP_GPU_GPIO_10		ROMSCK	TESTOUT[8]	
77C3	GPU_GPIO_11	IPD		TESTOUT[9]	ROMIDCFG[0]
77C3	GPU_GPIO_12	IPD		TESTOUT[10]	ROMIDCFG[1]
77C3	GPU_GPIO_13	IPD		TESTOUT[11]	ROMIDCFG[2]
77C3 74C5	NC_GPU_GPIO_14			TESTIN[8]	
77C3 74C5 71B4	GPU_VCORE_LOW			TESTIN[9]	PWRCNTL
77C3 74C5 34B4 34B2	GPU_CLK27MSS_IN			SS_IN	
77C3 74C5	NC_GPU_GPIO_17			Thm Mon Int	

GPU_BLON — MAKE_BASE=TRUE — 74C8 77D3 82A4
TP_GPU_GPIO_10 — MAKE_BASE=TRUE — 74C8 77C3
NC_GPU_GPIO_14 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3
GPU_VCORE_LOW — MAKE_BASE=TRUE — 71B4 74C8 77C3
GPU_CLK27MSS_IN — MAKE_BASE=TRUE — 34B2 34B4 74C8 77C3
NC_GPU_GPIO_17 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3

Required for debug access
Required for debug access
Required for debug access
Required for debug access

77D5 74B7 NC_GPU_GPIO_18 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_18 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_19 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_19 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_20 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_20 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_21 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_21 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_22 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_22 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_23 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_23 — 74B8 77D5
77D5 74B6 GPU_MEM_256M — 77D5 74B8 GPU_MEM_256M MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_25 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_25 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_26 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_26 — 74B8 77D5
77D5 74B6 GPU_MEMID — 77D5 74B8 GPU_MEMID MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_28 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_28 — 74B8 77D5
77C5 74B7 NC_GPU_GPIO_29 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_29 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_30 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_30 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_31 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_31 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_32 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_32 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_33 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_33 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_34 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_34 — 74B8 77C5

Renamed signals

77A5 74C1 34B4 34B2 GPU_CLK27M — MAKE_BASE=TRUE — GPU_CLK27M — 34B2 34B4 74C2 77A5

Unused signals

77A5 74C1 NC_GPU_XTALOUT — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_XTALOUT — 74C2 77A5
77A3 74C1 NC_ATI_ROMCS_L — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_ATI_ROMCS_L — 74C2 77A3
74C1 73D5 NC_FB_A_MA12 — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_FB_A_MA12 — 73D5 74C2
74C1 73D1 NC_FB_B_MA12 — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_FB_B_MA12 — 73D1 74C2
77C3 74C1 NC_GPU_GENERICA — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICA — 74C2 77C3
77C3 74C1 NC_GPU_GENERICB — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICB — 74C2 77C3
77C3 74C1 NC_GPU_GENERICC — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_GENERICC — 74C2 77C3
78C3 74C1 NC_GPU_VGA_R — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_R — 74C2 78C3
78C3 74C1 NC_GPU_VGA_G — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_G — 74C2 78C3
78C3 74C1 NC_GPU_VGA_B — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_VGA_B — 74C2 78C3
78B3 74C1 TP_GPU_VGA_HSYNC — MAKE_BASE=TRUE — TP_GPU_VGA_HSYNC — 74C2 78B3
78B3 74C1 TP_GPU_VGA_VSYNC — MAKE_BASE=TRUE — TP_GPU_VGA_VSYNC — 74C2 78B3
78B3 74C1 NC_GPU_TV_Y — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_Y — 74C2 78B3
78B3 74B1 NC_GPU_TV_C — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_C — 74B2 78B3
78B3 74B1 NC_GPU_TV_COMP — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_GPU_TV_COMP — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAP<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_U_DATAP<3> — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAN<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_U_DATAN<3> — 74B2 78B3
78A3 74B1 NC_LVDS_L_DATAP<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_L_DATAP<3> — 74B2 78A3
78A3 74B1 NC_LVDS_L_DATAN<3> — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_LVDS_L_DATAN<3> — 74B2 78A3
77C3 74B1 NC_ATI_DVPCLK — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_ATI_DVPCLK — 74B2 77C3
77C3 77B3 NC_ATI_DVPCNTL<2..0> — MAKE_BASE=TRUE — NO_TEST=TRUE — ATI_DVPCNTL<2..0>
77B3 NC_ATI_DVPDATA<15..0> — MAKE_BASE=TRUE — NO_TEST=TRUE — ATI_DVPDATA<15..0>

Required for debug access

77B3 77A3 TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

77D2 77C6 77B7 74D6 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8890 4.7K 5% 1/16W MF-LF 402
R8891 4.7K 5% 1/16W MF-LF 402

78A3 GPU_DDC_B_CLK
78A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 74 OF 87	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CRITICAL
OMIT

U8900
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8950
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

PP1V8_D3C

C8900 22UF 20% 6.3V CERM 805
C8901 C8902 C8903 C8904 C8905 C8906 C8907 0.1uF 10% 16V X5R 402
C8910 C8915 0.1uF 10% 16V X5R 402 U8900.J1 U8900.J12
C8920 22UF 20% 6.3V CERM 805
C8921 C8922 C8923 C8924 C8925 C8926 0.1uF 10% 16V X5R 402
C8931 C8933 0.1uF 10% 16V X5R 402
C8950 22UF 20% 6.3V CERM 805
C8951 C8952 C8953 C8954 C8955 C8956 C8957 0.1uF 10% 16V X5R 402
C8960 C8965 0.1uF 10% 16V X5R 402 U8900.J1 U8900.J12
C8970 22UF 20% 6.3V CERM 805
C8971 C8972 C8973 C8974 C8975 C8976 C8977 0.1uF 10% 16V X5R 402
C8981 C8983 0.1uF 10% 16V X5R 402

L8910 FERR-220-OHM 0402
PP1V8_S0_FB_A0_VDDA0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
L8915 FERR-220-OHM 0402
PP1V8_S0_FB_A0_VDDA1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
Connect to designated pin, then GND

L8960 FERR-220-OHM 0402
PP1V8_S0_FB_A1_VDDA0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
L8965 FERR-220-OHM 0402
PP1V8_S0_FB_A1_VDDA1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
Connect to designated pin, then GND

R8930 R8932 2.37K 1% 1/16W MF-LF 402
FB_A0_VREF0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
FB_A0_VREF1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R8931 R8933 5.49K 1% 1/16W MF-LF 402

R8980 R8982 2.37K 1% 1/16W MF-LF 402
FB_A1_VREF0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
FB_A1_VREF1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R8981 R8983 5.49K 1% 1/16W MF-LF 402

R8940 R8942 R8944 121 1% 1/16W MF-LF 402
R8946 60.4 1% 1/16W MF-LF 402
R8941 1K 5% 1/16W MF-LF 402
R8943 121 1% 1/16W MF-LF 402
R8945 60.4 1% 1/16W MF-LF 402
R8947 121 1% 1/16W MF-LF 402

R8990 R8992 R8994 121 1% 1/16W MF-LF 402
R8996 60.4 1% 1/16W MF-LF 402
R8991 1K 5% 1/16W MF-LF 402
R8993 121 1% 1/16W MF-LF 402
R8995 60.4 1% 1/16W MF-LF 402
R8997 121 1% 1/16W MF-LF 402

NOTE: U8900 DQ0-7 MUST connect to GPU
DQA0-7 or DQA8-15. Bits can be swapped
within byte-lane, but software must know
how these bits are mapped for GPU to support
GDDR3 vendor/device identification scheme.

FB_A_MA<0>
FB_A_MA<1>
FB_A_MA<2>
FB_A_MA<3>
FB_A_MA<4>
FB_A_MA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE<0>
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS_L<0>
FB_A_WE_L<0>
FB_A_CAS_L<0>
FB_A_RAS_L<0>
FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_DRAM_RST
FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>
FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A_DQM_L<0>
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>
FB_A_DQ<0>
FB_A_DQ<1>
FB_A_DQ<2>
FB_A_DQ<3>
FB_A_DQ<4>
FB_A_DQ<5>
FB_A_DQ<6>
FB_A_DQ<7>
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FB_A_DQM_L<5>
FB_A_DQM_L<6>
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FB_A_DQ<61>
FB_A_DQ<57>
FB_A_DQ<62>
FB_A_DQ<56>
FB_A_DQ<63>
FB_A_DQ<58>

R8948 243 1% 1/16W MF-LF 402
R8949 100 5% 1/16W MF-LF 402
R8998 243 1% 1/16W MF-LF 402
R8999 100 5% 1/16W MF-LF 402

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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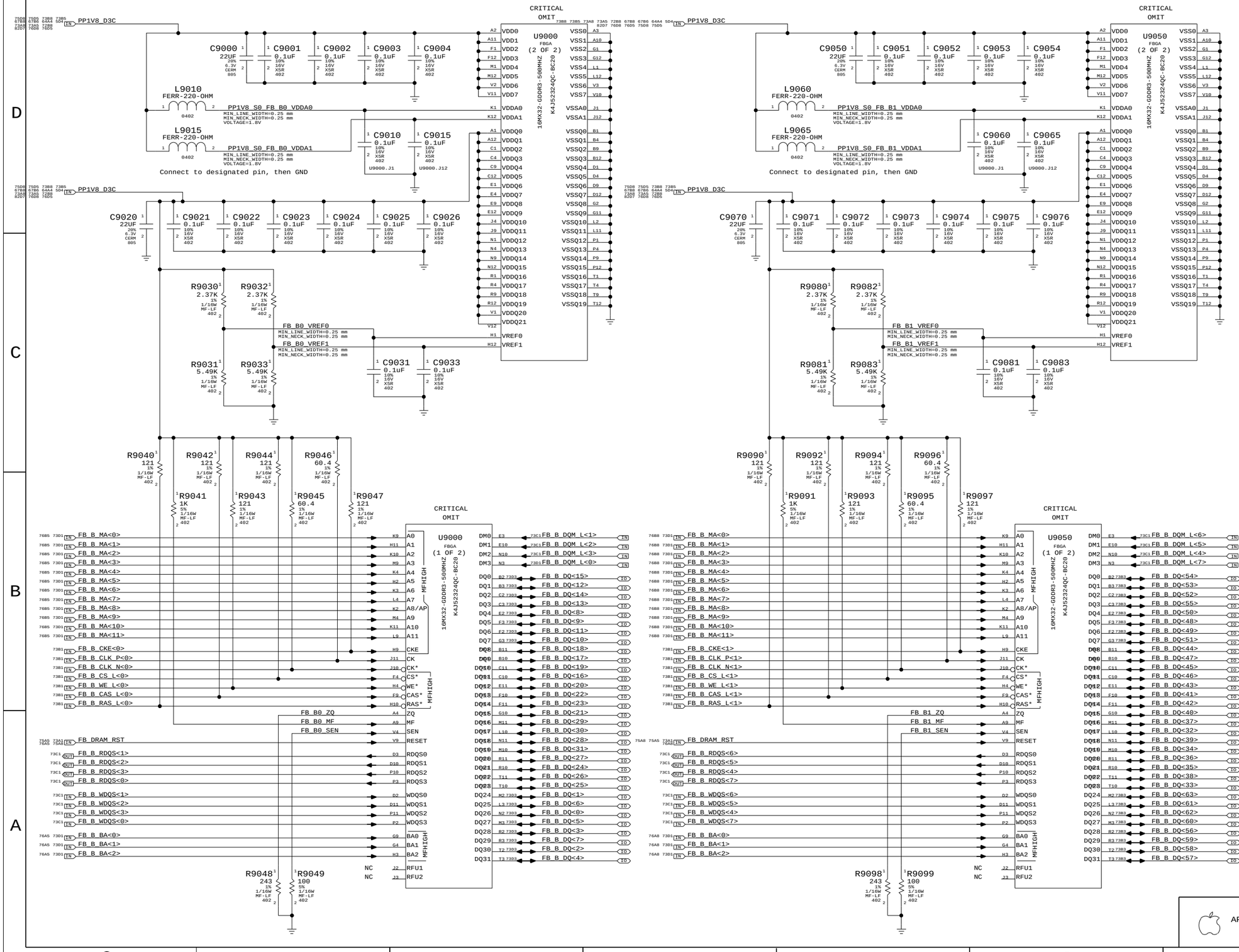
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	75	87



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

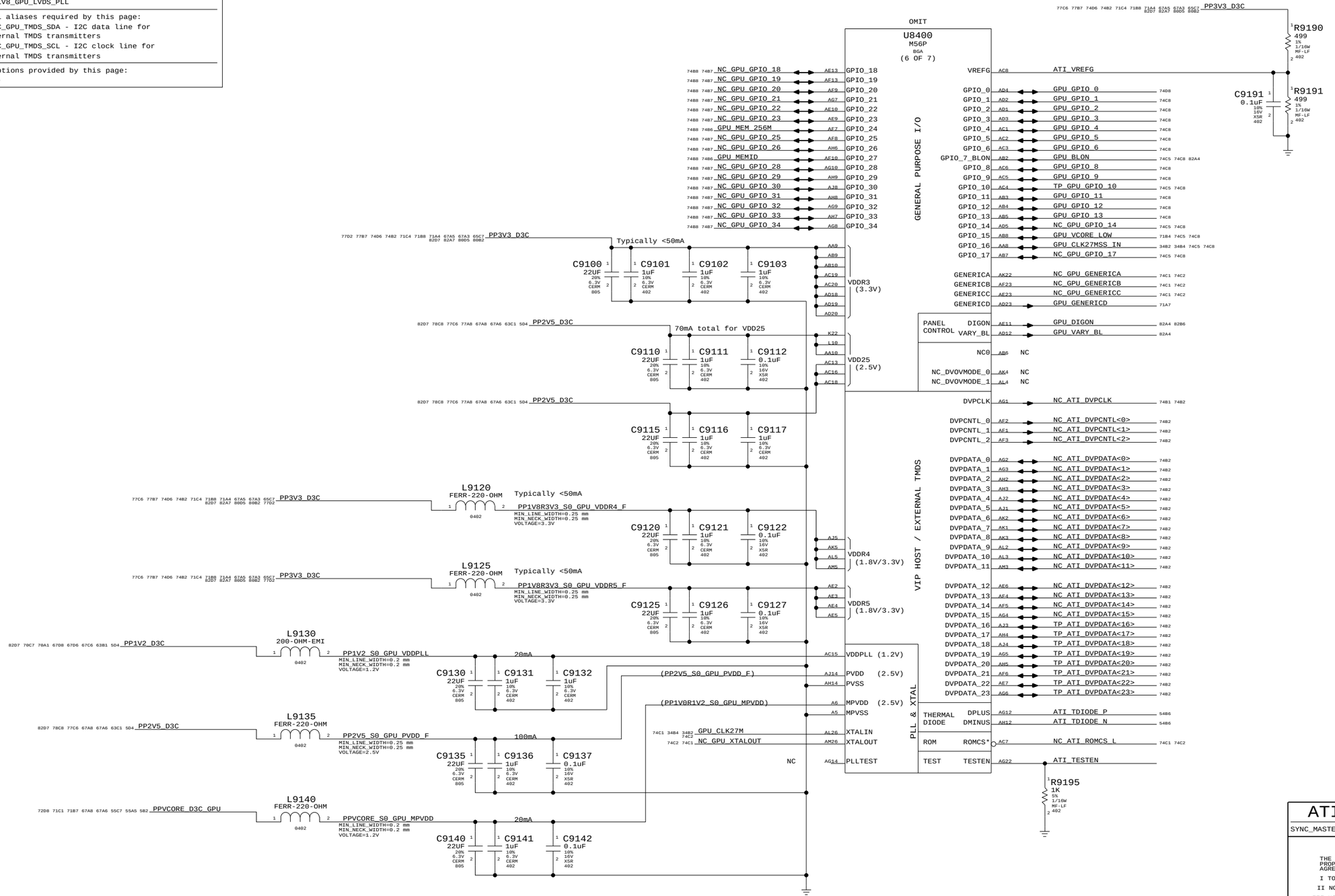
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 76 OF 87	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE

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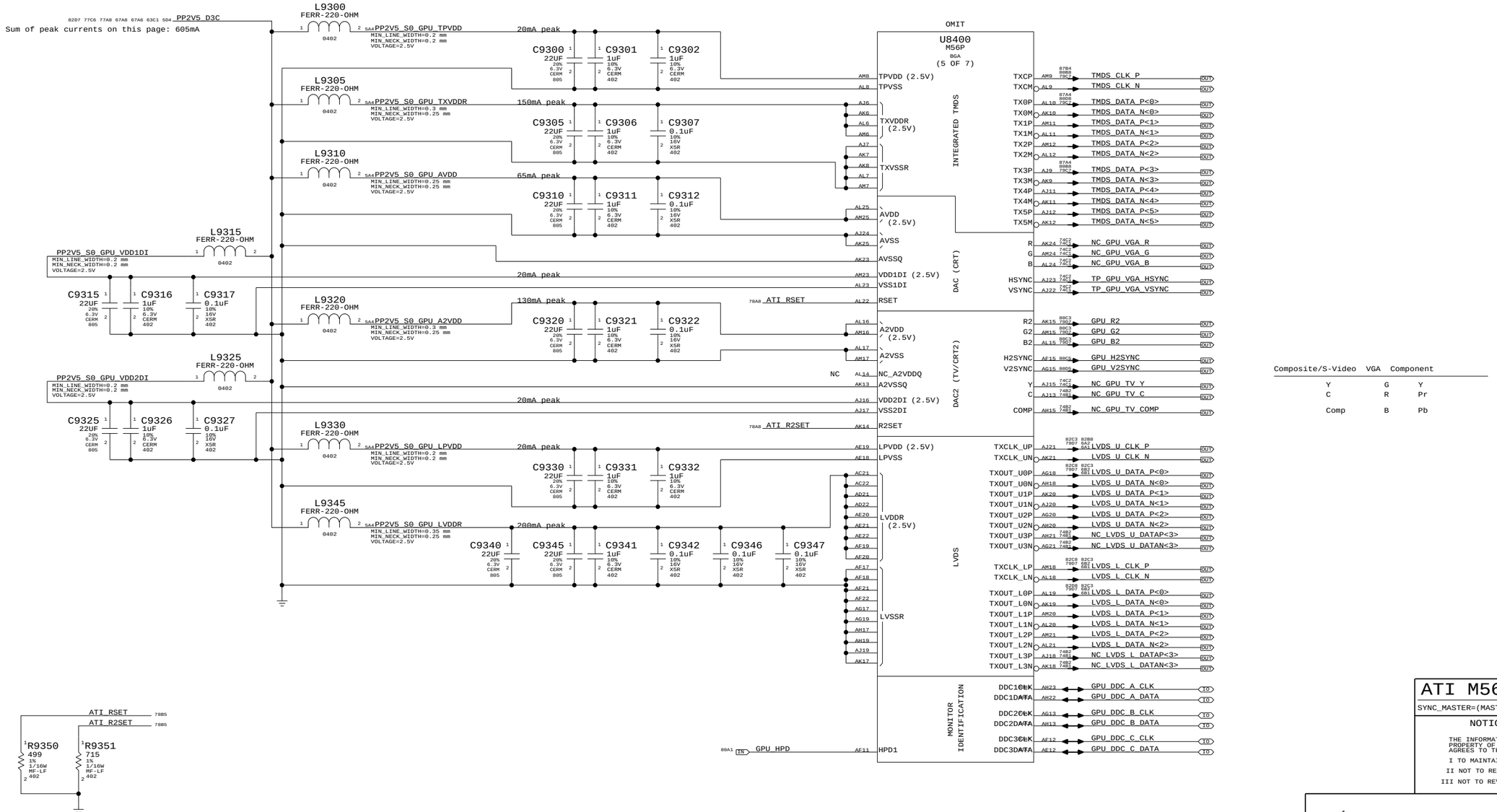
Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 78 OF 87	

LCD (LVDS) INTERFACE

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	VGA	VGA	GPU_R2 — 78B3 80C3
	VGA	VGA	GPU_G2 — 78B3 80C3
	VGA	VGA	GPU_B2 — 78B3 80C3
	LVDS	LVDS	LVDS_U_CLK_P — 6A1 6A2 78B3 82B8 82C3
	LVDS	LVDS	LVDS_U_CLK_N — 6A1 6A2 78B3 82B8 82C3
	LVDS	LVDS	LVDS_U_DATA_P<2..0> — 6A1 6B1 6B2 78B3 82B3 82C3 82C8
	LVDS	LVDS	LVDS_U_DATA_N<2..0> — 6A1 6B1 6B2 78B3 82C3 82C8
	LVDS	LVDS	LVDS_L_CLK_P — 6B1 6B2 78A3 82C3 82C8
	LVDS	LVDS	LVDS_L_CLK_N — 6B1 6B2 78A3 82C3 82D8
	LVDS	LVDS	LVDS_L_DATA_P<2..0> — 6B1 6B2 78A3 82C3 82D8
	LVDS	LVDS	LVDS_L_DATA_N<2..0> — 6B1 6B2 78A3 82C3 82D8
	LVDS	LVDS	LVDS_U_CLK_CONN_P — 79B2 82C1
	LVDS	LVDS	LVDS_U_CLK_CONN_N — 79B2 82C1
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0> — 79B2 79C2 82C1 82D1
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0> — 79C2 82C1 82D1
	LVDS	LVDS	LVDS_L_CLK_CONN_P — 79C2 82C1
	LVDS	LVDS	LVDS_L_CLK_CONN_N — 79C2 82C1
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0> — 79C2 82C1
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0> — 79C2 82C1
	TMDS	TMDS	TMDS_CLK_P — 78C3 80B8 87B4
	TMDS	TMDS	TMDS_CLK_N — 78C3 80C8 87B4
	TMDS	TMDS	TMDS_DATA_P<5..3> — 78C3 80A8 80B8 87A4
	TMDS	TMDS	TMDS_DATA_N<5..3> — 78C3 80A8 80B8 87A4
	TMDS	TMDS	TMDS_DATA_P<2..0> — 78C3 80C8 80D8 87A4
	TMDS	TMDS	TMDS_DATA_N<2..0> — 78C3 80C8 80D8 87A4

PP3V3_S5

C9400 0.0022uF 10% 50V CERM 402

R9400 100K 5% 1/10W MF-LF 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

Q9400 SI3443DV (TSOP-LF)

PP3V3_LCD_SW — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V

L9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

LCD_PWREN_L

Q9401 2N7002 SOT23-LF

LVDS_PANEL_EN

R9494 100K 5% 1/16W MF-LF 402

PP3V3_S0

100K pull-ups are for no-panel case (development). Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

LVDS_CONN_DDC_CLK

LVDS_CONN_DDC_DATA

C9410 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

CRITICAL J9400 MSC-RB30-5-FA F-RT-SM

C9420 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

PP3V3_LCD_CONN — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V

NC

LVDS_L_DATA_CONN_N<0>
LVDS_L_DATA_CONN_P<0>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_CLK_CONN_N
LVDS_L_CLK_CONN_P
LVDS_U_DATA_CONN_N<0>
LVDS_U_DATA_CONN_P<0>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_P<2>
LVDS_U_CLK_CONN_N
LVDS_U_CLK_CONN_P

C9421 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

518S0289

INVERTER INTERFACE

CRITICAL L9450 FERR-220-OHM-2A 0603

PPBUS_G3H

PPBUS_S0_INVERTER — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V

C9450 0.001uF 20% 50V CERM 402

PP5V_S0

Q9450 FDG6332C_NL SC70-6 P-CHN

R9450 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW_F — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V

L9452 400-OHM-EMI SM-1

C9451 10UF 20% 6.3V X5R 603

FP_PWR_EN_L

Q9450 FDG6332C_NL SC70-6 N-CHN

INVERTER_BKLTON

R9489 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V

C9452 0.001uF 20% 50V CERM 402

CRITICAL J9450 SM04B-ACH M-RT-SM

NC

NC

518S0369

L9454 400-OHM-EMI SM-1

INVERTER_PWM

GND_CHASSIS_INVERTER

C9454 0.001uF 20% 50V CERM 402

CRITICAL L9455 FERR-220-OHM-2A 0603

GND_CHASSIS_INVERTER

PP3V3_S0

PLT_RST_L

U9453 MC74VHC1G08 SC70

INVERTER_PWM_UNBUF

INVERTER_PWM_F

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

C9453 0.1uF 20% 10V CERM 402

Internal Display Connectors

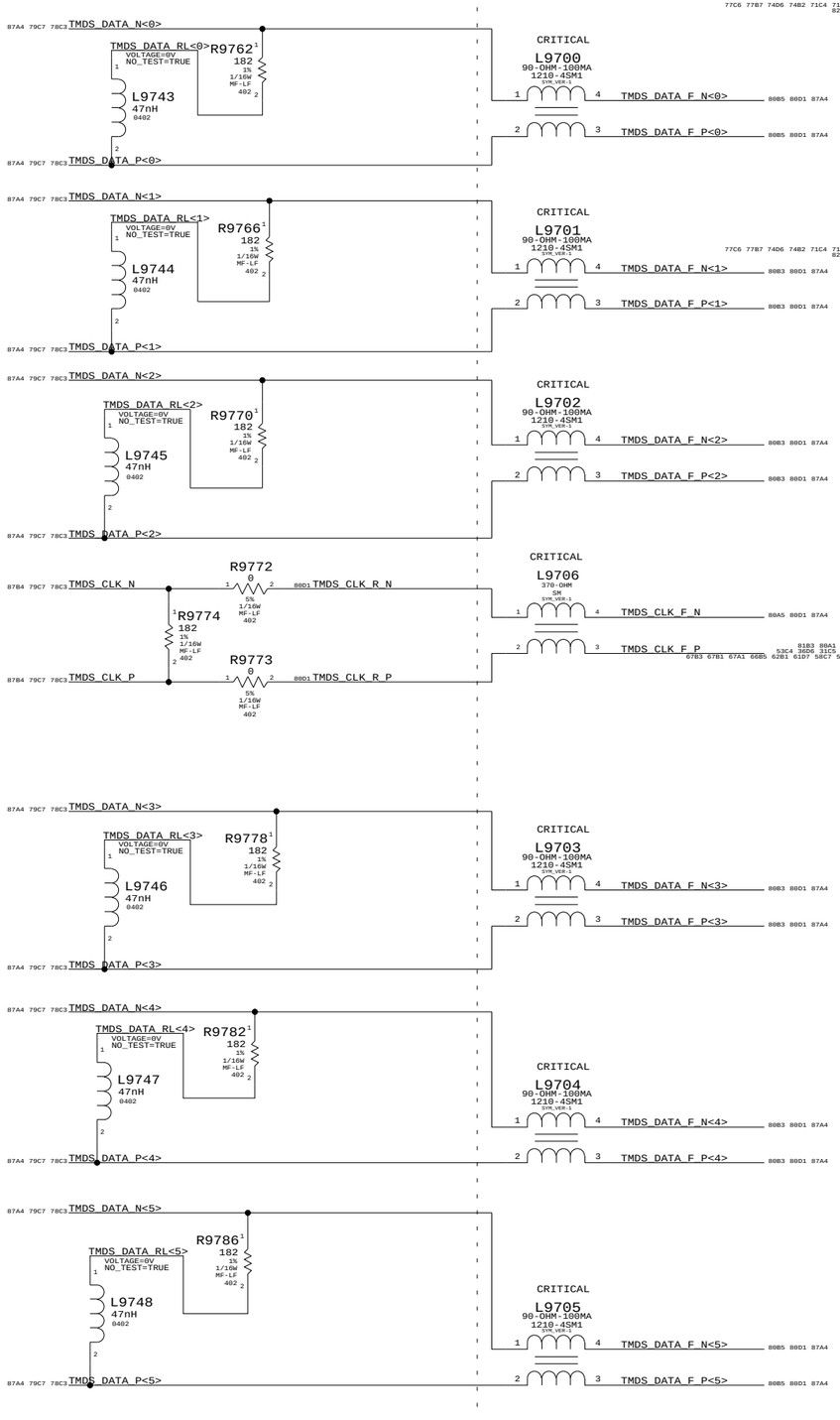
SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

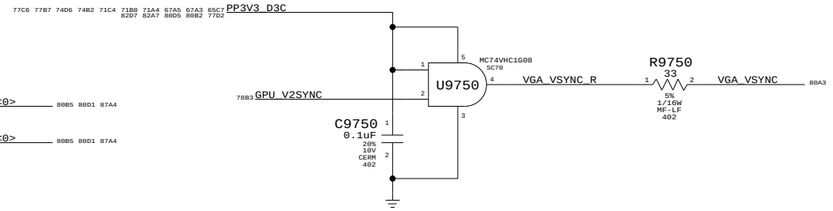
SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 79 OF 87	

TMDS Filtering

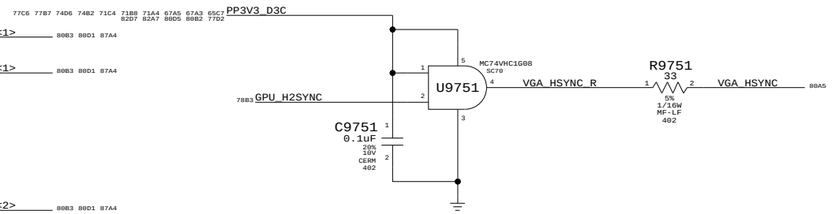
Place termination components close to GPU, common mode chokes near connector.



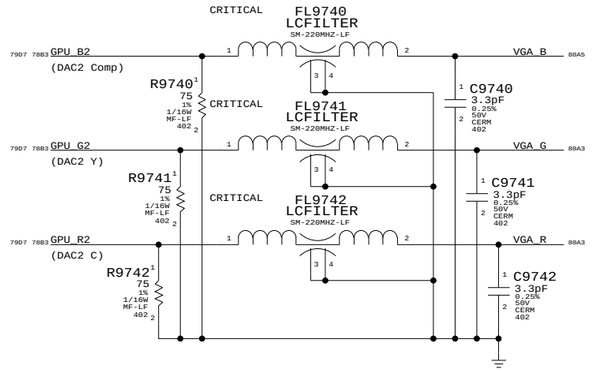
VGA SYNC BUFFERS



PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

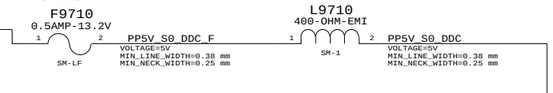


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

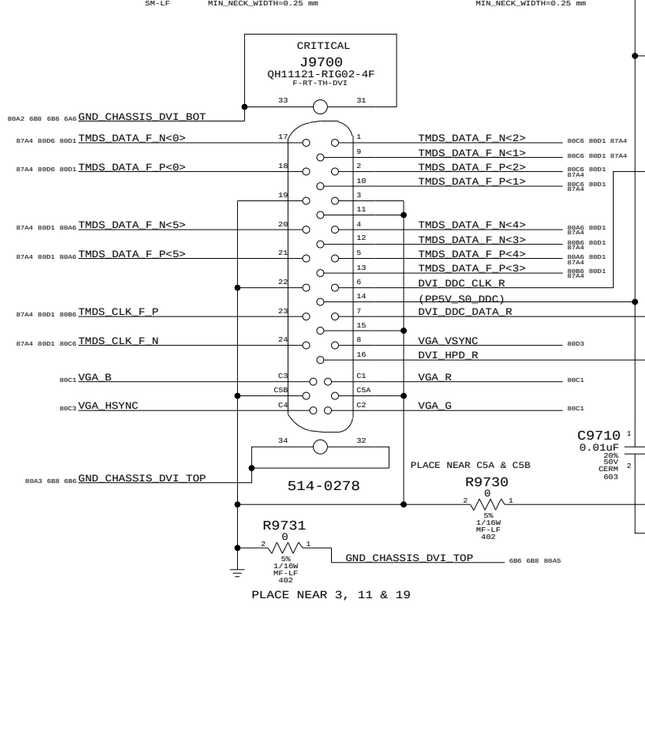


DVI INTERFACE

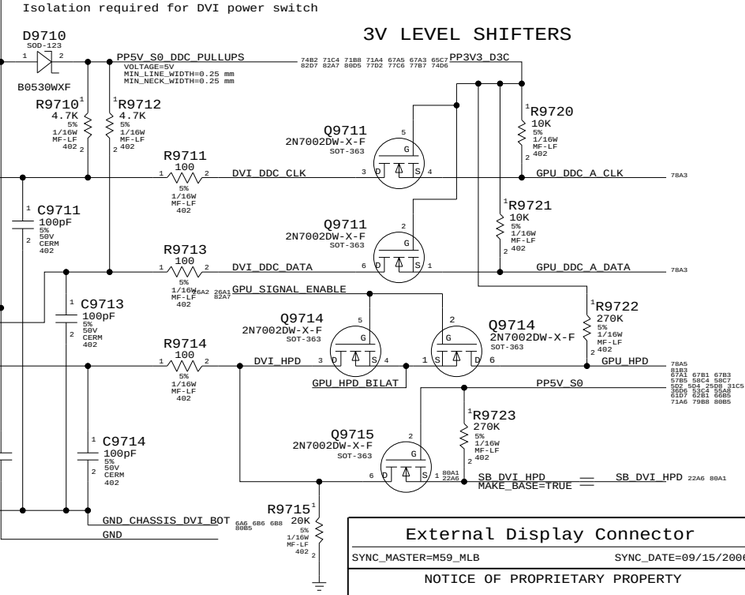
DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

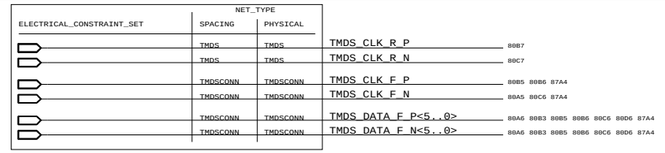


Isolation required for DVI power switch



3V LEVEL SHIFTERS



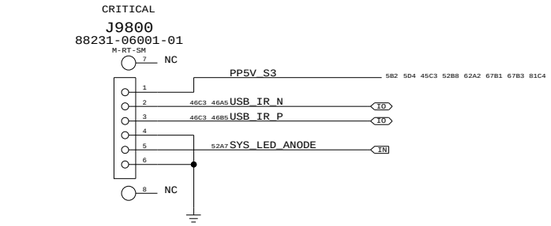


External Display Connector

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

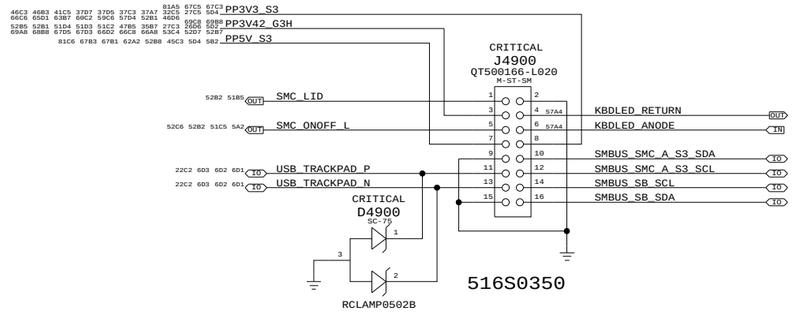
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	06004
	SCALE: NONE	SHT 80 OF 87	

IR & Sleep LED Connector



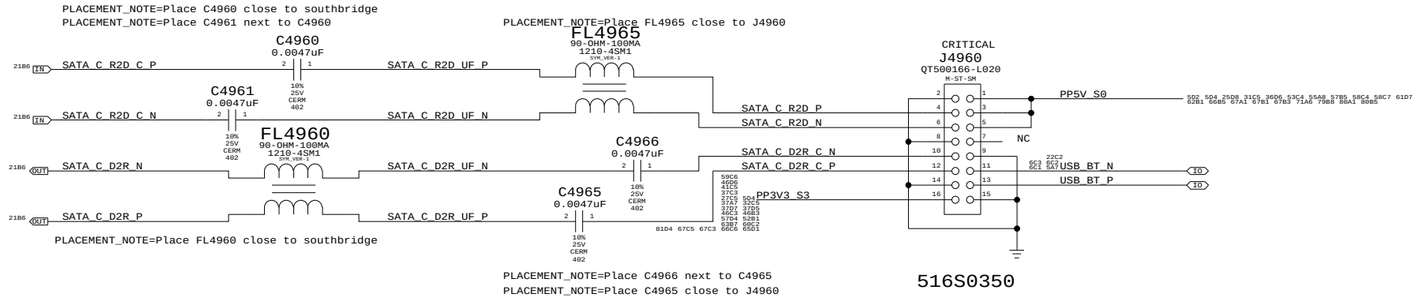
518S0474

Top-Case Connector



516S0350

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M57 SPECIFIC CONNECTORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 81 OF 87	

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_L_CLK_P
=LVDS_PD_L_CLK_N
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
=LVDS_PD_U_CLK_P
=LVDS_PD_U_CLK_N

LVDS_PD RP9900 8.2K 5% 1/16W SM-LF
LVDS_PD RP9900 8.2K 5% 1/16W SM-LF
LVDS_PD RP9900 8.2K 5% 1/16W SM-LF
LVDS_PD RP9900 8.2K 5% 1/16W SM-LF
LVDS_PD RP9901 8.2K 5% 1/16W SM-LF
LVDS_PD RP9901 8.2K 5% 1/16W SM-LF
LVDS_PD RP9901 8.2K 5% 1/16W SM-LF
LVDS_PD RP9901 8.2K 5% 1/16W SM-LF
LVDS_PD RP9902 8.2K 5% 1/16W SM-LF
LVDS_PD RP9902 8.2K 5% 1/16W SM-LF
LVDS_PD RP9902 8.2K 5% 1/16W SM-LF
LVDS_PD RP9902 8.2K 5% 1/16W SM-LF
LVDS_PD RP9903 8.2K 5% 1/16W SM-LF
LVDS_PD RP9903 8.2K 5% 1/16W SM-LF
LVDS_PD RP9903 8.2K 5% 1/16W SM-LF
LVDS_PD RP9903 8.2K 5% 1/16W SM-LF

PGOOD Monitor for GPU Rails

D3CPGOOD_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.
D3CPGOOD_3V3 BOM option uses only PP3V3_D3C to qualify D3CPGOOD.

PP3V3_D3C
PP2V5_D3C
PP1V8_D3C
PP1V2_D3C
PP3V3_S0
R9994 124K 1% 1/16W MF-LF 402
R9992 237K 1% 1/16W MF-LF 402
R9990 365K 1% 1/16W MF-LF 402
C9990 0.1UF 20% 10V CERM 402
R9997 10K 5% 1/16W MF-LF 402
C9991 0.1UF 20% 10V CERM 402
U9990 LTC2903 TSOT-23
V1 CRITICAL
V2 D3CPGOOD_2V5_DIV
V3 D3CPGOOD_1V8_DIV
V4 D3CPGOOD_1V2_DIV
RST* D3CPGOOD_PWROK
GND
R9995 100K 1% 1/16W MF-LF 402
R9993 100K 1% 1/16W MF-LF 402
R9991 100K 1% 1/16W MF-LF 402
C9995 0.1UF 20% 10V CERM 402
C9993 0.1UF 20% 10V CERM 402
C9992 0.1UF 20% 10V CERM 402
R9996 470K 5% 1/16W MF-LF 402
C9996 1UF 10% 6.3V CERM 402
U9991 MC74VHC1G08 SC70
S0PGOOD_PWROK
S0D3CPGOOD_PWROK

LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

PP3V3_S0
PP2V5_S0
C9985 0.1UF 20% 10V CERM 402
C9980 0.1UF 20% 10V CERM 402
GPU_DIGON
LVDS_MUX_SEL_GPU
U9985 MC74VHC1G08 SC70
GPU_DIGON_AND_SELECTED
CRITICAL
U9980 SN74LVC1G132 SC70-5
PP3V3_LCD_SW
R9980 10K 5% 1/16W MF-LF 402
PANEL_PWR_ON
R9981 13.3K 1% 1/16W MF-LF 402

Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

GPU DDC Pass FETs

GPU_SIGNAL_ENABLE
PP3V3_D3C
R9970 15.8K 1% 1/16W MF-LF 402
R9971 15.8K 1% 1/16W MF-LF 402
Q9970 2N7002DW-X-F SOT-363
GPU_DDC_C_CLK
GPU_DDC_C_DATA
LVDS_CONN_DDC_CLK MAKE_BASE=TRUE
LVDS_CONN_DDC_DATA MAKE_BASE=TRUE

LVDS I/F Mux

PP2V5_S0
C9950 0.1UF 20% 10V CERM 402
VDD
U9950 CBTV4020 BGA-LF SYM_VER-3 CRITICAL

NB LVDS I/F

LVDS_B_DATA_N<2>
LVDS_B_DATA_N<0>
LVDS_B_DATA_P<0>
LVDS_A_CLK_P
LVDS_A_CLK_N
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
LVDS_A_DATA_P<2>
LVDS_A_DATA_N<2>
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
LVDS_B_DATA_P<1>
LVDS_B_DATA_N<1>
LVDS_B_CLK_N
LVDS_B_CLK_P
LVDS_B_DATA_P<2>

GPU LVDS I/F

LVDS_U_DATA_N<2>
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_L_CLK_P
LVDS_L_CLK_N
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_P<2>
LVDS_L_DATA_N<2>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
LVDS_U_DATA_P<2>

DH0 LVDS_U_DATA_CONN_N<2>
DH1 LVDS_U_DATA_CONN_N<0>
DH2 LVDS_U_DATA_CONN_P<0>
DH3 NC
DH4 LVDS_L_CLK_CONN_P
DH5 LVDS_L_CLK_CONN_N
DH6 NC
DH7 LVDS_L_DATA_CONN_N<0>
DH8 LVDS_L_DATA_CONN_P<0>
DH9 LVDS_L_DATA_CONN_P<2>
DH10 LVDS_L_DATA_CONN_N<2>
DH11 LVDS_L_DATA_CONN_N<1>
DH12 LVDS_L_DATA_CONN_P<1>
DH13 NC
DH14 LVDS_U_DATA_CONN_P<1>
DH15 LVDS_U_DATA_CONN_N<1>
DH16 NC
DH17 LVDS_U_CLK_CONN_N
DH18 LVDS_U_CLK_CONN_P
DH19 LVDS_U_DATA_CONN_P<2>
SEL LVDS_MUX_SEL_GPU_L

NOTE: SEL = LOW selects port B

Panel/Backlight Control Mux

PP3V3_S0
C9960 0.1UF 20% 10V CERM 402
CRITICAL
U9960 74CBTLV3257 QFN SYM_VER-2
VCC GND THRML PAD

LVDS_VDDEN
GPU_DIGON
LVDS_BKLTEN
GPU_BLON
LVDS_BKLTCTL
GPU_VARY_BL
S0PGOOD_PWROK
S0D3CPGOOD_PWROK
LVDS_MUX_SEL_GPU_MUXED

NOTE: S = HIGH selects xB2

LVDS_PANEL_EN
INVERTER_BKLTON
INVERTER_PWM_UNBUF
PGOOD_MUXED_S0_OR_S0D3C

PP3V3_S0
C9961 0.1UF 20% 10V CERM 402
PLT_RST_L
LVDS_MUX_SEL_GPU
U9961 MC74VHC1G08 SC70
NO STUFF R9962 0 5% 1/16W MF-LF 402
R9961 100K 5% 1/16W MF-LF 402
R9960 10K 5% 1/16W MF-LF 402

LVDS_MUX_SEL_GPU
LVDS_MUX_SEL_GPU MAKE_BASE=TRUE
LVDS_MUX_SEL_GPU

NOTE: SB_GPIO23 has internal 20K PU to default selection to GPU

LVDS Interface Pull-downs

SYNC_MASTER=M59_MLB SYNC_DATE=09/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004
SCALE: NONE	SHT 82 OF 87	

Revision History

Revision History

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE	SHT	OF
NONE	83	87

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE: NONE SHT: 84 OF: 87

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_3SS_TO_5SS	*	Y	=3S_OHM_SE	=5S_OHM_SE	=3S_5S_OHM_SE	=STANDARD	=STANDARD
FB_4QS	*	Y	=4Q_OHM_SE	=4Q_OHM_SE	=4Q_OHM_SE	=STANDARD	=STANDARD
FB_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	06004

SCALE NONE SHT 85 OF 87

M9 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5A4 7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5A7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5A4 7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5B7 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5B7 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5A7 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5B7 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5B4 7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	5B4 7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	5C4 7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	5B4 14B7 23C3 61C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	5C4 61C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 33C4 34D3 34D5
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 33C4 34D3 34D5
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 61B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 61A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61A3

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 48B3
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 48B3

TMDS	TMDS	TMDS_CLK_P	78C3 79C7 80B8
TMDS	TMDS	TMDS_CLK_N	78C3 79C7 80C8
TMDS	TMDS	TMDS_DATA_P<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_N<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_P<2..0>	78C3 79C7 80C8 80D8
TMDS	TMDS	TMDS_DATA_N<2..0>	78C3 79C7 80C8 80D8
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	80A5 80C6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	80B3 80B5 80C6 80D1 80D6
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	80B3 80B5 80C6 80D1 80D6

M57 NET PROPERTIES

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