1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
				?	?

SCHEM,LIO/AUDIO ,MacBook Pro 15"
9/22/06

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7146	1	SCHEM,LIO/AUDIO,MacBook Pro 15	SCH1	CRITICAL	
820-2055	1	PCBF,LIO/AUDIO,MacBook Pro 15	PCB1	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,LIO/AUDIO,MacBook Pro 15

DRAWING NUMBER 051-7146 REV. A

SHT 1 OF 18

J8200
DC-In Jack

18V5_DCIN

U8200
AC Adapter Detect

U8290
OneWire
OverVoltage Protection

3V42_G3H

U7800
PBus Supply/Batt. Charger

PBUS_A
PBUS_B
BATTERY
DCIN_G3H

J8215
PBus/Battery Power Connector

3V3_S0

U8415
Batt.Current Sensor

U8405
DC-In.Current Sensor

U8450
Temp. Sensor

U7800
3.3V S3/S0 Supply

3V3_S0
3V3_S3

J5500
LIO-MLB Flex Connector

J5100
Left USB Port

U5100
USB Pwr Controller

DCIN_G3H
3V42_G3H
5V_S3

U5300
ExCard Pwr Switcher

3V3_S0
3V3_S3

J5300
PCI-ExpressCard 34 Connector

VR6800
Audio 4.5V Supply

5V_S0_AUDIO

3V3_S0

1V5_S0

J7350
Audio In/SPDIF Rx Jack

U6800
Audio Codec

J7380
Speaker/Mic Connector

J5400
PCI-E miniCard (Airport) Connector

3V3_S0
3V3_S3

5V_S0_AUDIO_PWR

J7300
Audio Out/SPDIF Tx Jack

U7210/U7220
SPEAKER AMPS

U7400
HP/LO MUTE SWITCH

Block Diagram

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE	SHT	OF
NONE	2	18

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7709	PCBA,LIO/AUDIO,MacBook Pro 15	ALTERNATE,COMMON,M59_COMMON

BOM GROUP	BOM OPTIONS
M59_COMMON	ISL6255A

Bar Code Label / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
000-0041	1	PLACEHOLDER FOR EEE/CCC INFO	[EEE:W39]	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445		ALL	SI7806ADN for FSM6296
128S0081	128S0061		ALL	150uF,6.3V,25MOHM,C2
128S0093	128S0092		ALL	33UF,16V,45MOHM,D2E

BOM Configuration

SYNC_MASTER=(Master) SYNC_DATE=(Master)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE	SHT	OF
NONE	3	18

POWER & GROUNDS

14D3 =PPDCIN_G3H_LIO_CONN
15B2 =PPVBATT_G3H_LIO_CONN
→ PPDCIN_G3H
MAKE_BASE=TRUE
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.20mm
→ =PPDCIN_G3H 8C6

14B3 =PP18V5_G3H_INRUSH
→ PP18V5_G3H_CHGR
MAKE_BASE=TRUE
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.60mm
MIN_NECK_WIDTH=0.20mm
→ =PP18V5_G3H_CHGR 15D8

15C1 =PPVBAT_G3H_CHGR_REG
→ PPVBAT_G3H_CHGR_REG
MAKE_BASE=TRUE
VOLTAGE=18.5V
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.25mm
→ =PPBUS_G3H_LIO_CONN 14A3
→ =PPVIN_S3_3V3S3 13D8

8C6 =PP3V42_G3H
→ PP3V42_G3H
MAKE_BASE=TRUE
VOLTAGE=3.42V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.20mm
→ =PP3V42_G3H_ACIN 14B8 15A8 15B8 15C8

8C6 =PP1V5_S0
→ PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.20mm
→ =PP1V5_S0_MINI 7C2
→ =PP1V5_S0_EXCARD 6C7 6C8

13B1 =PP3V3_S3_REG
→ PP3V3_S3_LIO
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
→ =PP3V3_S3_MINI 7C2
→ =PP3V3_S3_EXCARD 6B8 6C7 6C8

13C1 =PP3V3_S0_FET
→ PP3V3_S0_LIO
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
→ =PP3V3_S0_MINI 7D2
→ =PP3V3_S0_AUDIO 9A6 9D7 11B8 11D8 12B5
→ =PP3V3_S0_PBATTISENS 16C7
→ =PP3V3_S0_PDCISENS 16C4
→ =PP3V3_S0_TMPSNSR 16B5
→ =PP3V3_S0_EXCARD 6B4 6C7

8C6 =PP5V_S5
→ PP5V_S5
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
→ =PP5V_S5_LTUSB 5C7
→ =PP5V_S5_3V3S3 13C8

9A6 8C6 =PP5V_S0_AUDIO
→ PP5V_S0_AUDIO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM

10B8 10D8 8C6 =PP5V_S0_AUDIO_AMP
→ PP5V_S0_AUDIO_AMP
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.60 MM
MIN_NECK_WIDTH=0.10 MM

10C8 10A8 10B5 11C3 8B6 =GND_AUDIO_AMP
→ GND_AUDIO_AMP
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm

8B3 =GND_AUDIO
→ GND_AUDIO
MAKE_BASE=TRUE
VOLTAGE=0V
→ =GND_AUDIO_CODEC 9A6 9B6 9D2 10A8 10C8 11B2 11B5 12A3 12A5 12A6 12B3 12B5 12B8 12C3 12C5 12C8 12D8

CHASSIS_GND1
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
→ =GND_CHASSIS_AUDIO_JACK 11A8 11B1 11B7 11C8
→ =GND_CHASSIS_PCIE_EXCARD_LEFT 6B1 6D3

CHASSIS_GND2
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
→ =GND_CHASSIS_PCIE_EXCARD_RIGHT 6B2
→ =GND_CHASSIS_AUDIO_SPKRCONN 11B1
→ =GND_CHASSIS_AUDIO_MIC 12A6

CHASSIS_GND3
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
→ =GND_CHASSIS_DCIN_JACK 14C8
→ =GND_CHASSIS_LTUSB 5B2

GND
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm

BATTERY

GND_BATT_CHGND CONNECTS TO BATT CHASSIS GND IN LAYOUT(NC IN NETLIST)

NC GND_BATT_CHGND
MAKE_BASE=TRUE
→ =GND_BATT_CHGND 15A1

14A3 =PPBATTPOS_G3H_LIO_CONN
→ BATT_POS
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
→ =BATT_POS 15B1

14A3 =PPBATTNEG_G3H_LIO_CONN
=BATT_NEG IS ALIASED TO GND ON PAGE 15
THEREFORE CONSTRAINTS HAVE BEEN REMOVED.
→ =BATT_NEG 15A1

PCI-E EXPRESS CARD 34

8C3 6C3 USB2_EXCARD_P
NET_PHYSICAL_TYPE=USB
NET_SPACING_TYPE=USB
MAX_EXPOSED_LENGTH=12.5MM
→ I2C4

8C3 6C3 USB2_EXCARD_N
NET_PHYSICAL_TYPE=USB
NET_SPACING_TYPE=USB
MAX_EXPOSED_LENGTH=12.5MM
→ I2C6

8B2 6C3 PCIE_CLK100M_EXCARD_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C7

8B2 6C3 PCIE_CLK100M_EXCARD_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C9

8B4 PCIE_CLK100M_EXCARD_UF_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C8

8B4 PCIE_CLK100M_EXCARD_UF_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C9

8B3 6C3 PCIE_EXCARD_D2R_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C6

8B3 6C3 PCIE_EXCARD_D2R_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C4

8B3 6C3 PCIE_EXCARD_R2D_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C4

8B3 6C3 PCIE_EXCARD_R2D_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C7

8C6 6B2 EXCARD_CLKREQ_L
→ I2C5

8C6 6C7 EXCARD_OC_L
→ I2C6

8C3 PCIE_WAKE_L
MAKE_BASE=TRUE
→ PCIE_WAKE_EXCARD_L 6C3
→ PCIE_WAKE_MINI_L 7C6

8C6 LIO_PLT_RESET_L
MAKE_BASE=TRUE
→ PLT_RESET_L 6C7 7C3

PCI-E MINICARD

8B3 7B6 PCIE_MINI_R2D_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C4

8C3 7B6 PCIE_MINI_R2D_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C6

8C3 7C6 PCIE_MINI_D2R_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C5

8C3 7C6 PCIE_MINI_D2R_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C3

8C2 7C6 PCIE_CLK100M_MINI_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C8

8C2 7C6 PCIE_CLK100M_MINI_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C9

8C4 PCIE_CLK100M_MINI_UF_P
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C7

8C4 PCIE_CLK100M_MINI_UF_N
NET_PHYSICAL_TYPE=PCIE
NET_SPACING_TYPE=PCIE
MAX_EXPOSED_LENGTH=12.5MM
→ I2C6

7B3 USB2_MINI_P
NET_PHYSICAL_TYPE=USB
NET_SPACING_TYPE=USB
→ TP_USB2_MINIP

7B3 USB2_MINI_N
NET_PHYSICAL_TYPE=USB
NET_SPACING_TYPE=USB
→ TP_USB2_MININ

8C6 7C6 MINI_CLKREQ_L
→ I2C5

USB

8C3 USB2_LT_P
MAKE_BASE=TRUE
NET_PHYSICAL_TYPE=USB
NET_SPACING_TYPE=USB
→ LEFT_USB_P 5C4
MAX_EXPOSED_LENGTH=12.5MM

8C3 USB2_LT_N
MAKE_BASE=TRUE
NET_PHYSICAL_TYPE=USB
NET_SPACING_TYPE=USB
→ LEFT_USB_N 5C4
MAX_EXPOSED_LENGTH=12.5MM

8C6 LTUSB_OC_L
MAKE_BASE=TRUE
→ LEFT_USB_OC_L 5C5

SMBUS

8C3 SMBUS_SMC_SCL
MAKE_BASE=TRUE
→ =SMBUS_TMPSNSR_SCL 16B5
MAKE_BASE=TRUE
→ =SMBUS_MINI_SCL 7B3

8C3 SMBUS_SMC_SDA
MAKE_BASE=TRUE
→ =SMBUS_TMPSNSR_SDA 16B5
MAKE_BASE=TRUE
→ =SMBUS_MINI_SDA 7B3

8C3 SMBUS_SB_SCL
MAKE_BASE=TRUE
→ =SMBUS_EXCARD_SCL 6C3

8C3 SMBUS_SB_SDA
MAKE_BASE=TRUE
→ =SMBUS_EXCARD_SDA 6C3

POWER MANAGEMENT

8B6 LIO_S3_EN
MAKE_BASE=TRUE
→ =LEFT_USB_PWRON 5C7
→ =LIO_P3V3S3_EN 13B8

Aliases

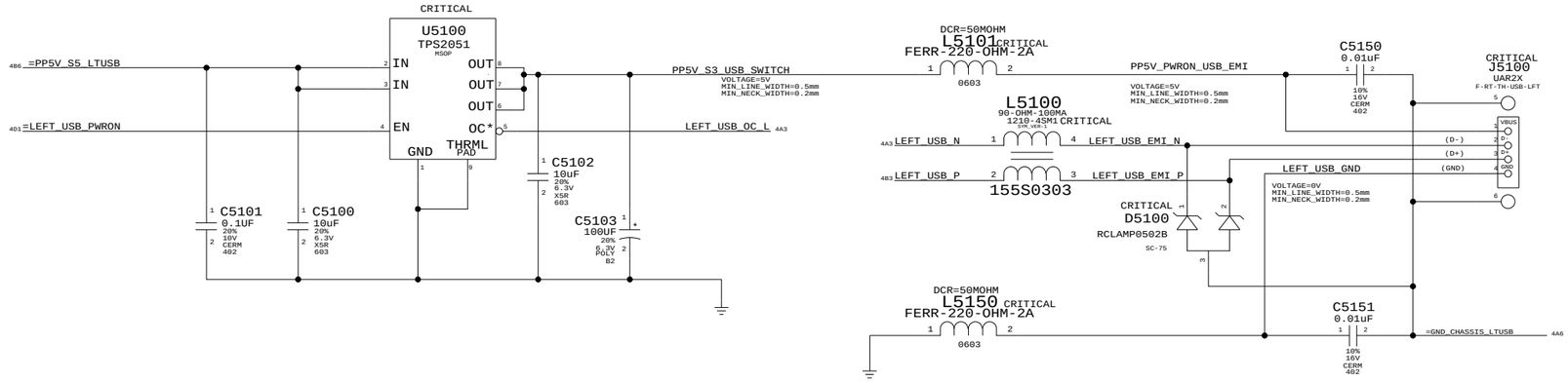
SYNC_MASTER=(Master) SYNC_DATE=(Master)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE NONE SHT 4 OF 18

LEFT USB PORT



PUT L5100, L5101, AND L5150 ACROSS THE MOAT

Left USB Port

SYNC_MASTER=(Master) SYNC_DATE=(Master)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE	SHT	OF
NONE	5	18

EXPRESSCARD/34 TOP MOUNT CONNECTOR

INPUT DECOUPLING

6C7 6B8 4C6 =PP3V3_S3_EXCARD
- C5330 0.1uF 20% 10V CERM 402
- C5331 10uF 20% 6.3V X5R 603

6C7 4C6 =PP1V5_S0_EXCARD
- C5334 0.1uF 20% 10V CERM 402
- C5335 10uF 20% 6.3V X5R 603

CRITICAL

U5300 TPS2231 QFN

6C8 6B8 4C6 =PP3V3_S3_EXCARD	17 AUXIN	AUXOUT 15	OUTPUT DECOUPLING
6B4 4C6 =PP3V3_S0_EXCARD	2 VIN3P3	VOUT3P3 3	
6C8 4C6 =PP1V5_S0_EXCARD	12 VIN1P5	VOUT1P5 11	
8B6 SMC_EXCARD_PWR_EN	20 SHDN*	PERST* 8	
TP_EXCARD_STBY_L	1 STBY*	CPPE* 10	
7C3 4C3 PLT_RESET_L	6 SYSRST*	CPUSB* 9	
8C6 4C6 EXCARD_OC_L	19 OC*		
NC 4	NC0	RCLKEN 18	EXCARD_RCLKEN 6B3
NC 5	NC1		
NC 13	NC2		
NC 14	NC3		
NC 16	NC4	THRML_PAD 21	
		GND	

R5300 0 MF-LF 402 5% 1/16W — SMC_EXCARD_PWR_EN → EXCARD_SHDN_L_R

OUTPUT DECOUPLING

PP3V3_S3_EXCARD_SWITCH 6C3 — VOLTAGE=3.3V, MIN_LINE_WIDTH=.3mm, MIN_NECK_WIDTH=0.2mm
- C5300 0.1uF 20% 10V CERM 402
- C5303 10uF 20% 6.3V X5R 603

PP3V3_S0_EXCARD_SWITCH 6C3 — VOLTAGE=3.3V, MIN_LINE_WIDTH=.6mm, MIN_NECK_WIDTH=0.2mm
- C5301 0.1uF 10% 16V X5R 402
- C5304 10uF 20% 6.3V X5R 603

PP1V5_S0_EXCARD_SWITCH 6C3 — VOLTAGE=1.5V, MIN_LINE_WIDTH=.6mm, MIN_NECK_WIDTH=0.2mm
- C5302 0.1uF 10% 16V X5R 402
- C5305 10uF 20% 6.3V X5R 603

PLT_RESET_SWITCH_L 6C3
EXCARD_CPPE_L 6A8 6C3
EXCARD_CPUSB_L 6A8 6C3

CARD CAGE CONNECTOR
CRITICAL
J5300 237-5300703903-2 F-RT-SM

6B1 4B6 =GND_CHASSIS_PCIE_EXCARD_LEFT — R5371 0 5% 1/16W MF-LF 402 — EC_HOLE1

32		
NC 28		
1		
2	8C3 4D6 USB2_EXCARD_N	
3	8C3 4D6 USB2_EXCARD_P	
4	6C3 6A8 EXCARD_CPUSB_L	
5	NC RESERVED	
6	NC RESERVED	
7	4A3 =SMBUS_EXCARD_SCL	
8	4A3 =SMBUS_EXCARD_SDA	
9	6C3 PP1V5_S0_EXCARD_SWITCH	
10		
11	4C3 PCIE_WAKE_EXCARD_L	
12	6C3 PP3V3_S3_EXCARD_SWITCH	
13	6C3 PLT_RESET_SWITCH_L	
14	6C3 PP3V3_S0_EXCARD_SWITCH	
15		
16	6A4 EXCARD_CLKREQ_CONN_L	
17	6C3 6A8 EXCARD_CPPE_L	
18	8B2 4D6 PCIE_CLK100M_EXCARD_N	
19	8B2 4D6 PCIE_CLK100M_EXCARD_P	
20		
21	8B3 4D6 PCIE_EXCARD_D2R_N	
22	8B3 4D6 PCIE_EXCARD_D2R_P	
23		
24	6C3 8B3 4C6 PCIE_EXCARD_R2D_N	
25	6C3 8B3 4D6 PCIE_EXCARD_R2D_P	
26		
27		
33		

R5370 0 5% 1/16W MF-LF 402 — EC_HOLE2 → =GND_CHASSIS_PCIE_EXCARD_LEFT 4B6 6D3

=GND_CHASSIS_PCIE_EXCARD_RIGHT 4A6

6C8 6C7 4C6 =PP3V3_S3_EXCARD
- C5350 0.1uF 20% 10V CERM 402

6C3 EXCARD_CPUSB_L
6C3 EXCARD_CPPE_L
- U5351 MC74VHC1G00 SC70-5 — SMC_EXCARD_CP 8B6

6C7 4C6 =PP3V3_S0_EXCARD
- R5361 100K 1% 1/16W MF-LF 402
- R5360 100K 1% 1/16W MF-LF 402 6C5 EXCARD_RCLKEN
- Q5360 2N7002 SOT23-LF — 6C3 EXCARD_CLKREQ_CONN_L
- C5360 0.1uF 20% 10V CERM 402

EXCARD_CLKREQ_CONN
- U5360 MC74VHC1G00 SC70-5 — EXCARD_CLKREQ_L 4C6 8C6

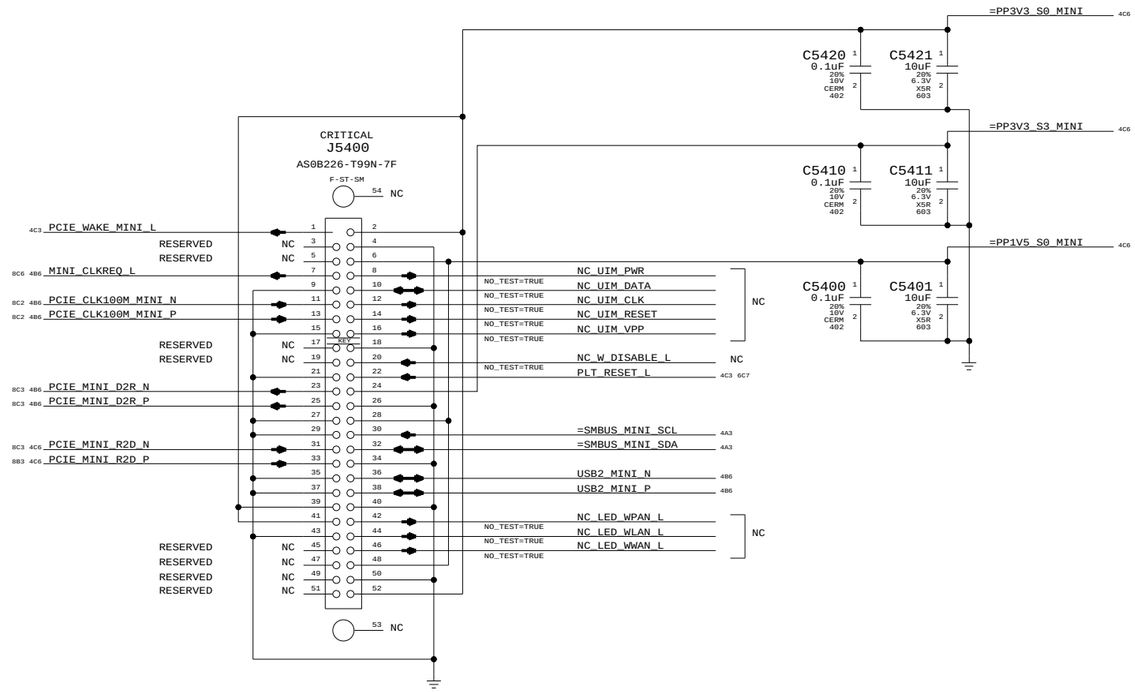
ExpressCard Connector

SYNC_MASTER=(Master) SYNC_DATE=(Master)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A
SCALE: NONE	SHT 6 OF 18	

PCI-EXPRESS MINI CARD CONNECTOR



PCI-E MiniCard Connector

SYNC_MASTER=(Master) SYNC_DATE=(Master)

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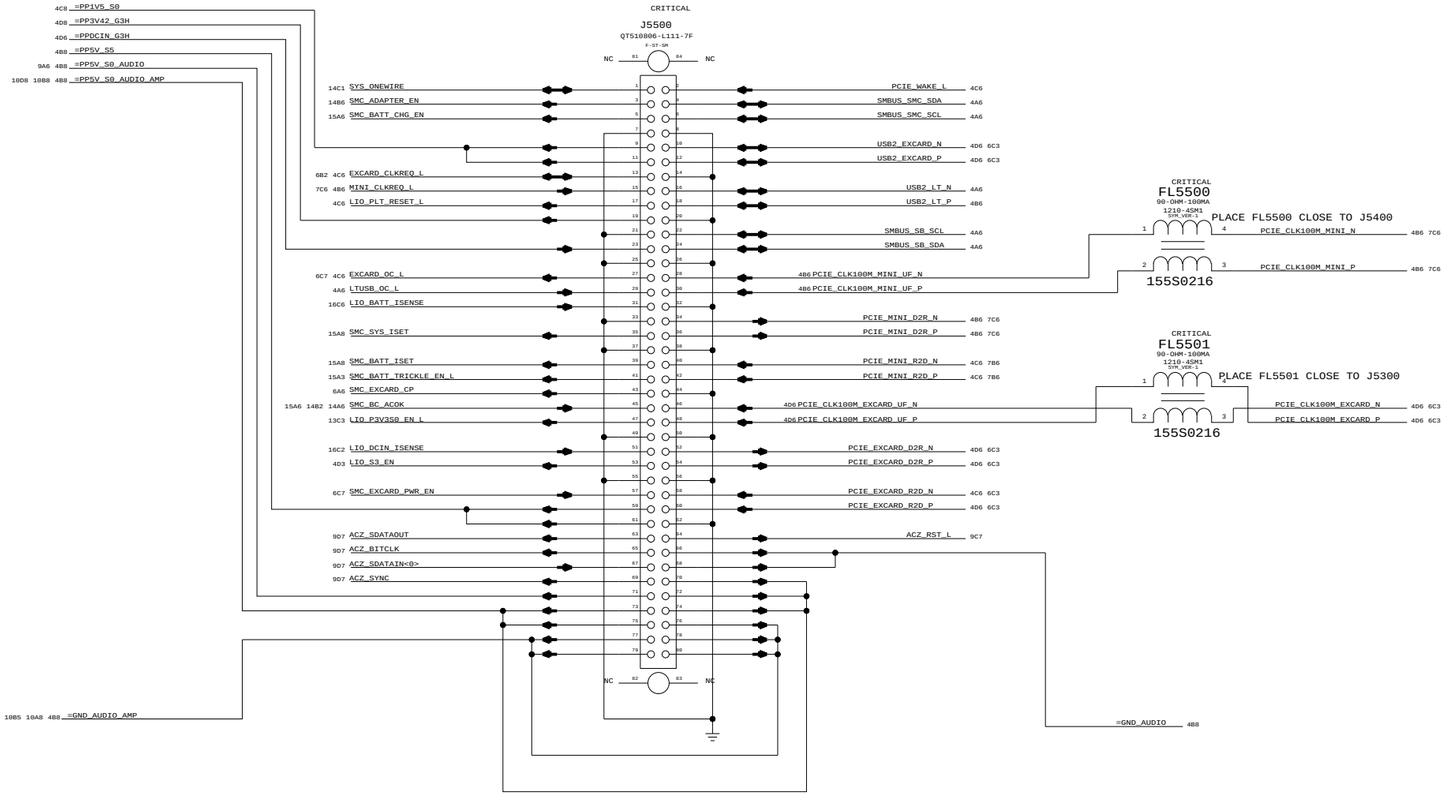
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE	SHT	OF
NONE	7	18

Left I/O Board Connector



MLB I/O Board Connector

SYNC_MASTER=(Master) SYNC_DATE=(Master)

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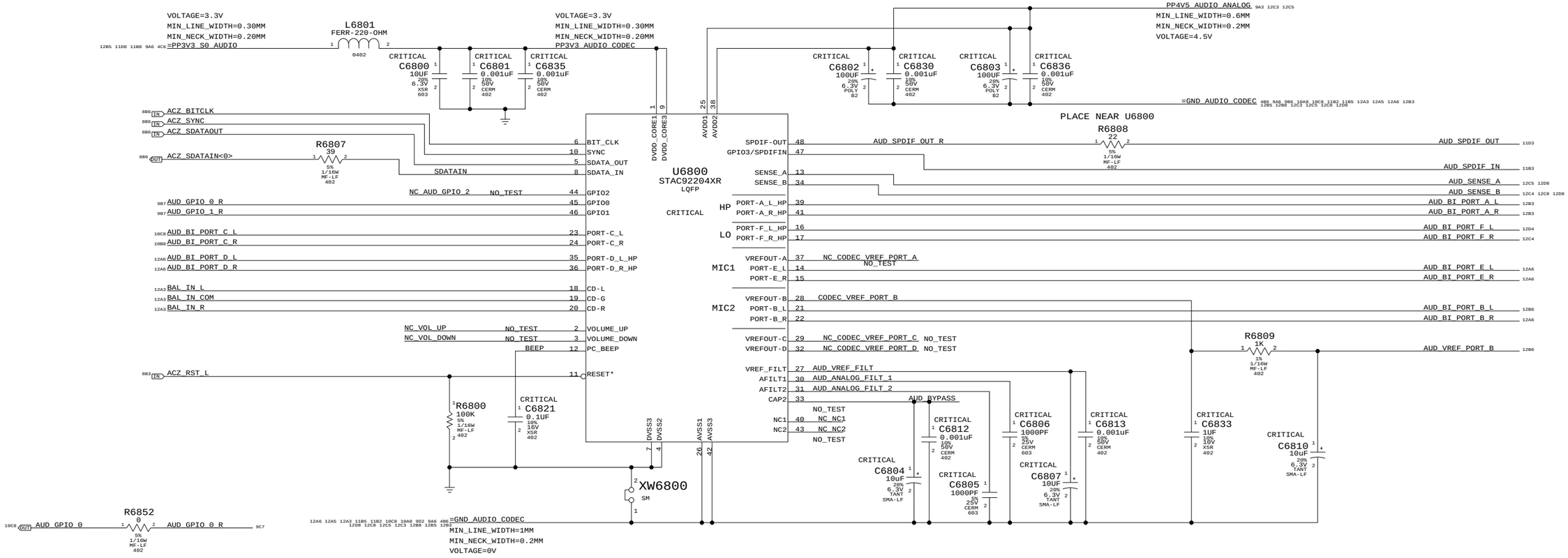
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE	SHT	OF
NONE	8	18

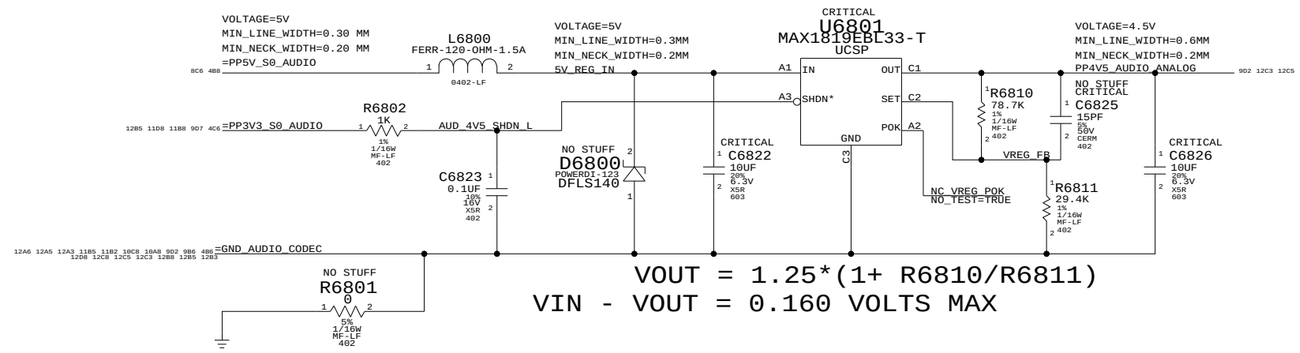
AUDIO CODEC

APPLE P/N 353S1458



4.5V POWER SUPPLY FOR CODEC

APN: 353S1455



AUDIO: CODEC

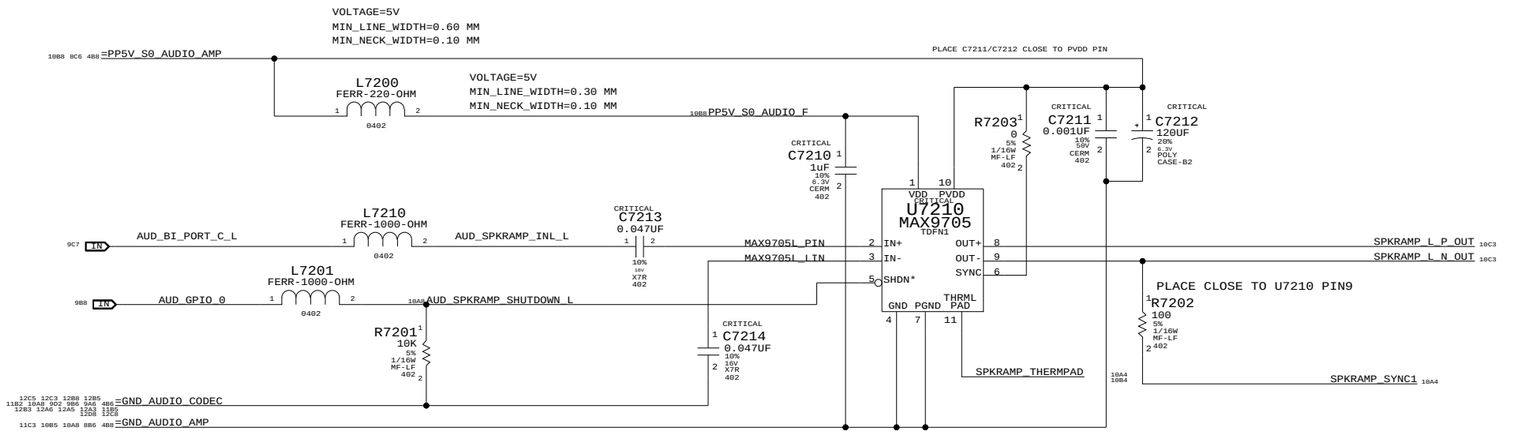
SYNC_MASTER=LENGO_M59_LIO SYNC_DATE=08/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A
SCALE: NONE	SHT 9 OF 18	

2X MONO SPEAKER AMPLIFIERS (MAX9705B) APN: 353S1595

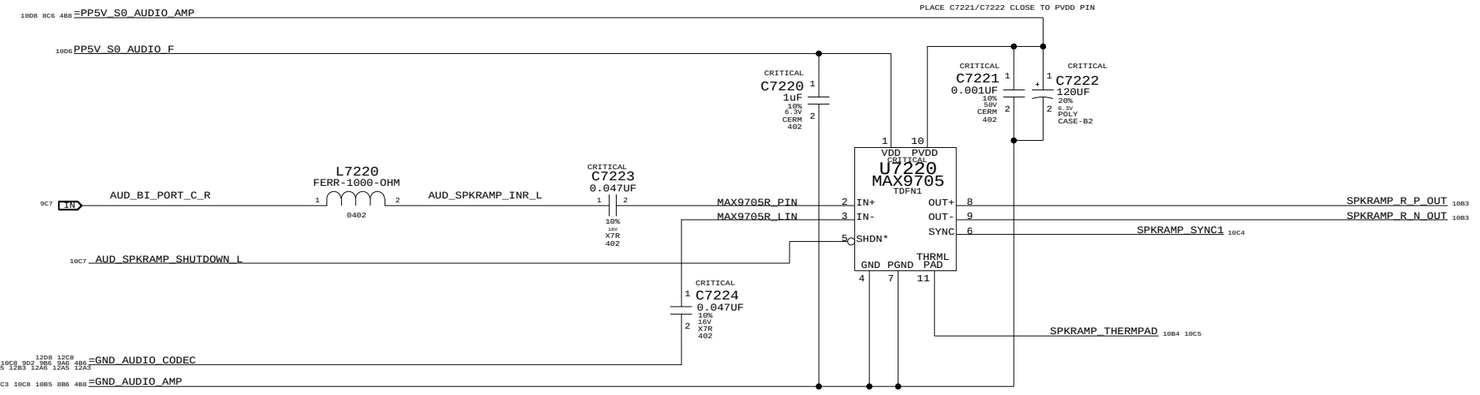
GAIN = 12DB 169 < FC < 282HZ



XW7200
SM
11C3 10C8 10A8 8B6 4B8 =GND_AUDIO_AMP
SPKRAMP_THERMPAD 10A4 10C5

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
10C4 SPKRAMP_L_P_OUT
R7210
0
5%
1/16W
MF-LF
402
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRCONN_L_P_OUT
OUT 11C3

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
10C4 SPKRAMP_L_N_OUT
R7211
0
5%
1/16W
MF-LF
402
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRCONN_L_N_OUT
OUT 11C3



MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
10B3 SPKRAMP_R_P_OUT
R7220
0
5%
1/16W
MF-LF
402
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRCONN_R_P_OUT
OUT 11C3

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
10A3 SPKRAMP_R_N_OUT
R7221
0
5%
1/16W
MF-LF
402
MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRCONN_R_N_OUT
OUT 11C3

AUDIO:SPEAKER AMP

SYNC_MASTER=LENGO_M59_LIO SYNC_DATE=08/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A
SCALE: NONE	SHT 10 OF 18	

AUDIO JACK 1 LO/HP CONNECTOR, SPDIF TX

=PP3V3_S0_AUDIO
APN: 514-0272

CRITICAL
J7300
TRANS
F-RT-TH

AUD_SPDIF_OUT

AUD_CONNJ1_SLEEVE
AUD_CONNJ1_RING
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_SLEEVEDET

L7300 FERR-120-OHM-1.5A 0402-LF
L7301 FERR-120-OHM-1.5A 0402-LF
L7302 FERR-1000-OHM 0402
L7303 FERR-1000-OHM 0402
L7304 FERR-1000-OHM 0402
L7305 FERR-1000-OHM 0402
L7306 FERR-1000-OHM 0402
L7307 FERR-1000-OHM 0402

AUD_CONNJ1_SLEEVE_F
AUD_CONNJ1_TIPDET_F
AUD_CONNJ1_RING_F
AUD_CONNJ1_TIP_F
AUD_CONNJ1_SLEEVEDET_F

AUD_PORTA_R
AUD_PORTA_L
AUD_J1_SLEEVEDET_R
AUD_J1_TIPDET_R

C7308 0.047UF 10% 10V X7R 402
C7307 0.047UF 10% 10V X7R 402
R7392 100K 5% 1/16W MF-LF 402
C7300 1UF 10% 6.3V CERM 402
C7305 100PF 5% 50V CERM 402
C7350 1UF 10% 6.3V CERM 402
C7351 10UF 20% 6.3V X5R 603
C7356 100PF 5% 50V CERM 402

NO STUFF CRITICAL DZ7300 5.6V-15A 0405
NO STUFF CRITICAL DZ7301 5.6V-15A 0405
CRITICAL DZ7302 8V-100PF 402
CRITICAL DZ7303 8V-100PF 402
CRITICAL DZ7304 8V-100PF 402
CRITICAL DZ7306 8V-100PF 402
NO STUFF CRITICAL DZ7351 5.6V-15A 0405
CRITICAL DZ7352 8V-100PF 402
CRITICAL DZ7353 8V-100PF 402
CRITICAL DZ7354 8V-100PF 402
CRITICAL DZ7355 8V-100PF 402

R7300 10K 5% 1/16W MF-LF 402
R7301 4.7 5% 1/16W MF-LF 402
R7351 4.7 5% 1/16W MF-LF 402

=GND_CHASSIS_AUDIO_JACK

PLACE AT GROUND MOAT

NO STUFF
R7391 0 5% 1/16W MF-LF 402
=GND_CHASSIS_AUDIO_JACK — =GND_AUDIO_CODEC

XW7300 SM AUD_J1_COM
XW7301 SM AUD_J2_COM
=GND_AUDIO_CODEC

R7349 0 5% 1/16W MF-LF 402
AUD_J2_OPT_OUT
AUD_SPDIF_IN

=PP3V3_S0_AUDIO
APN: 514-0273

CRITICAL
J7350
RCVR
F-RT-TH

AUD_CONNJ2_SLEEVE
AUD_CONNJ2_RING
AUD_CONNJ2_TIPDET
AUD_CONNJ2_TIP
AUD_CONNJ2_SLEEVEDET

L7350 FERR-220-OHM 0402
L7351 FERR-220-OHM 0402
L7352 FERR-1000-OHM 0402
L7353 FERR-1000-OHM 0402
L7354 FERR-1000-OHM 0402
L7355 FERR-1000-OHM 0402
L7356 FERR-1000-OHM 0402
L7357 FERR-220-OHM 0402
L7358 FERR-220-OHM 0402

AUD_CONNJ2_SLEEVE_F
AUD_CONNJ2_TIPDET_F
AUD_CONNJ2_RING_F
AUD_CONNJ2_TIP_F
AUD_CONNJ2_SLEEVEDET_F

AUD_PORTF_R
AUD_PORTF_L
AUD_J2_TIPDET_R

=GND_CHASSIS_AUDIO_JACK

AUDIO JACK 2 LINE IN CONNECTOR, SPDIF RX

SPEAKER/MIC CONNECTOR
APN: 518-0262

CRITICAL
J7380
88462-0811-01
M-ST-TH

MIC_LO
MIC_HI
MIC_SHIELD
SPKRCONN_R_P_OUT
SPKRCONN_R_N_OUT
SPKRCONN_L_P_OUT
SPKRCONN_L_N_OUT

R7380 0 5% 1/16W MF-LF 402
=GND_AUDIO_AMP
SPKR_SHIELD

XW7310 SM =GND_CHASSIS_AUDIO_SPKRCONN
XW7311 SM =GND_CHASSIS_AUDIO_JACK
XW7312 SM =GND_CHASSIS_AUDIO_JACK

AUDIO_SHIELD_PLANE
NO STUFF
R7390 0 5% 1/16W MF-LF 402

AUDIO SHIELD (FILLED SHAPE)

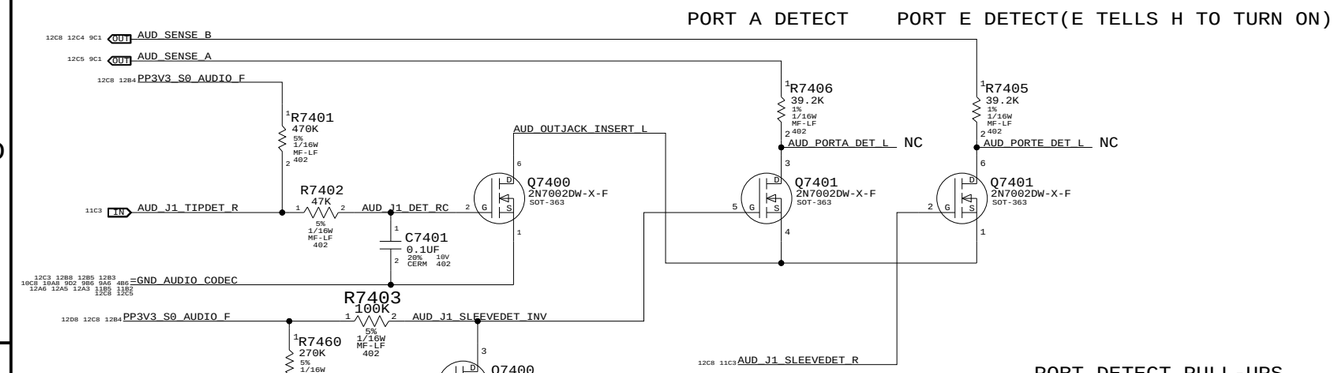
AUDIO: JACKS

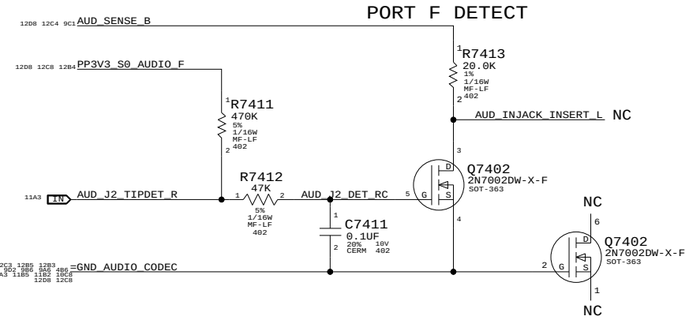
SYNC_MASTER=LENGO_M59_LIO SYNC_DATE=08/15/2006

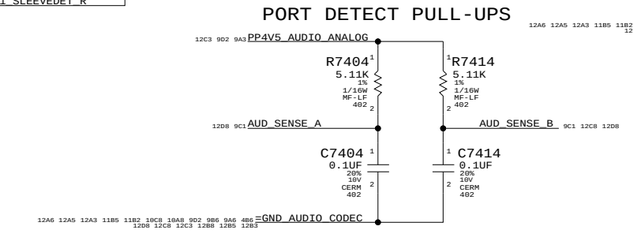
APPLE COMPUTER INC.

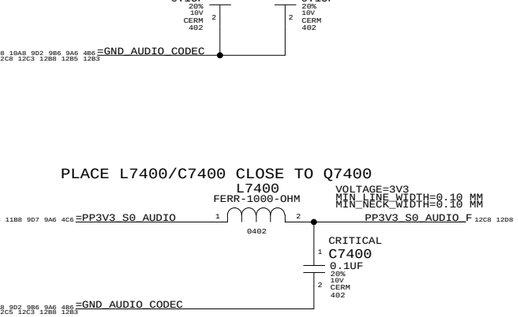
SIZE	DRAWING NUMBER	REV.
D	051-7146	A

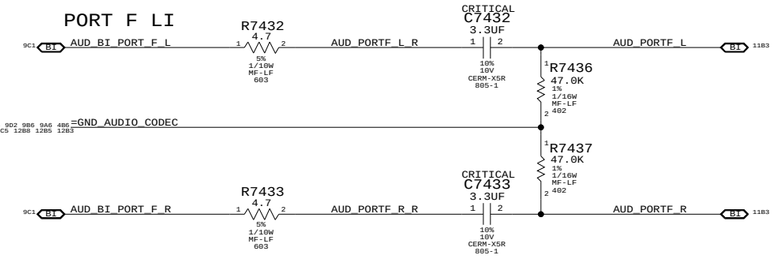
SCALE: NONE SHT 11 OF 18





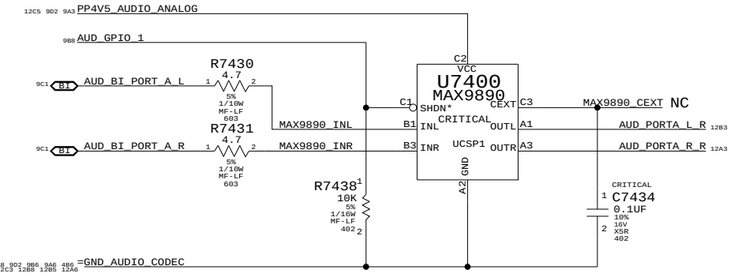


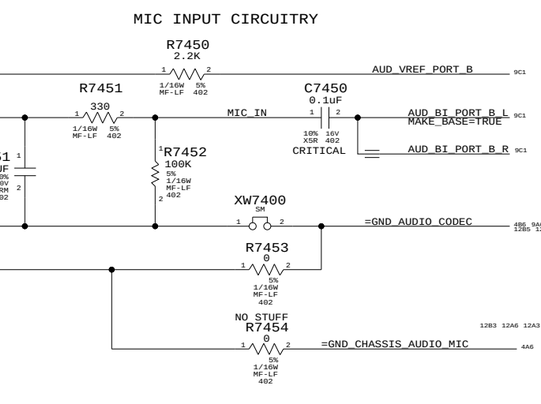


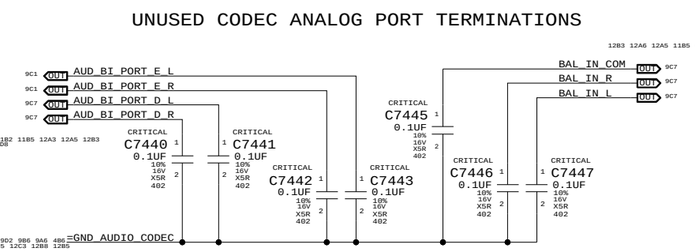


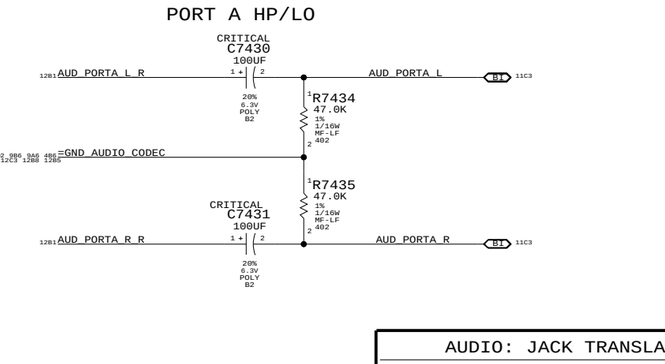
CODEC PORT ASSIGNMENTS

PORT A :HEADPHONE/LINE OUT
PORT B :MICROPHONE ON BOTH CH
PORT C :SPEAKER AMP
PORT D :UNUSED
PORT E :SPDIF OUTPUT DETECT DELEGATE
PORT F :LINE IN
CD INPUT :UNUSED









AUDIO: JACK TRANSLATORS

SYNC_MASTER=LENGO_M59_LIO SYNC_DATE=08/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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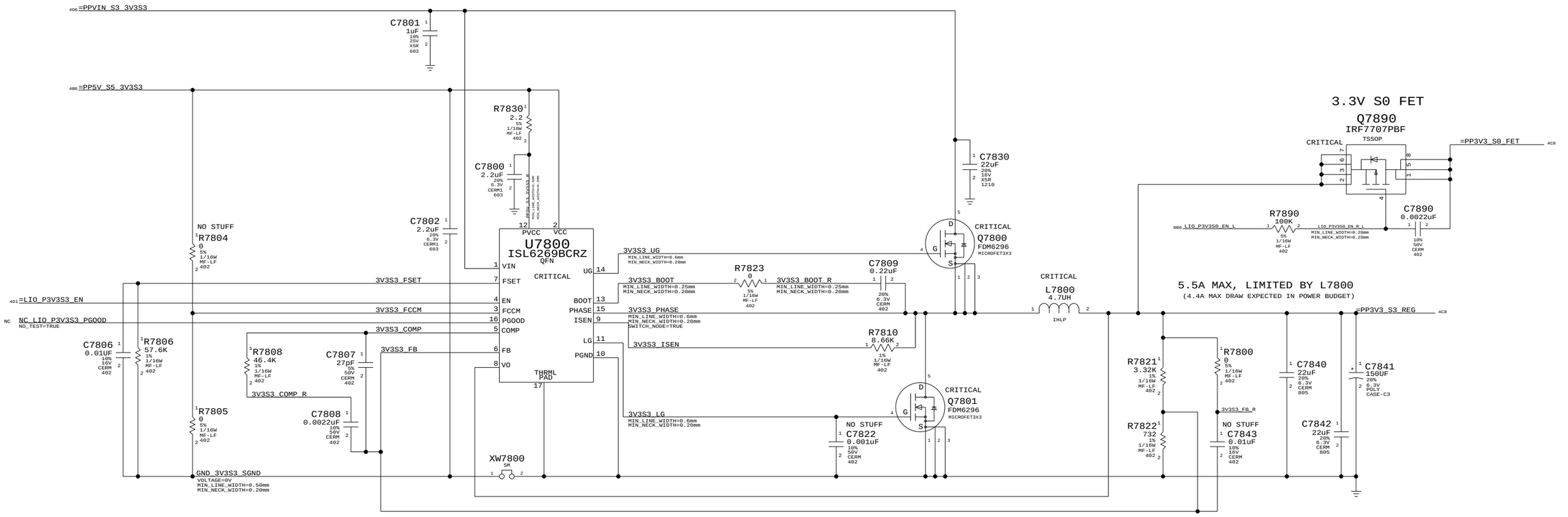
3.3V S3/S0 Power Supply



3.3V Supply

SYNC_MASTER=(Master) SYNC_DATE=(Master)

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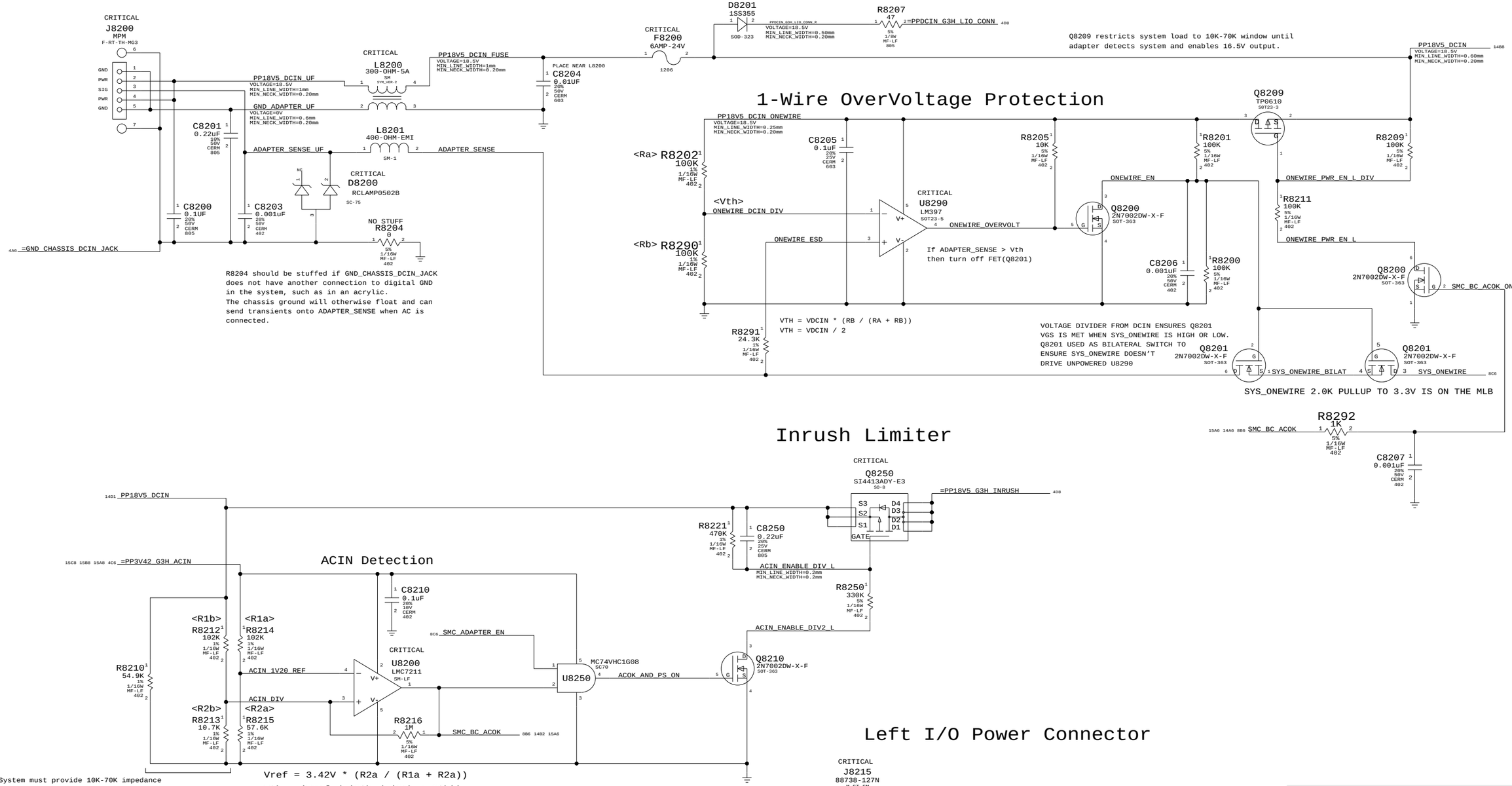
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE	SHT	OF
NONE	13	18

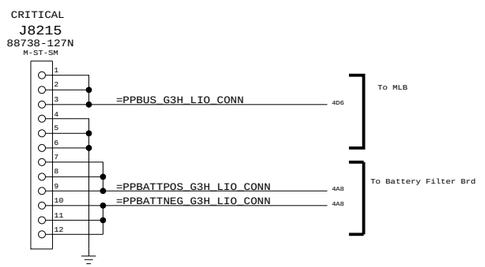
DC Power Jack



1-Wire OverVoltage Protection

Inrush Limiter

Left I/O Power Connector



Q8209 restricts system load to 10K-70K window until adapter detects system and enables 16.5V output.

DC-In & Battery Connectors

SYNC_MASTER=(Master) SYNC_DATE=(Master)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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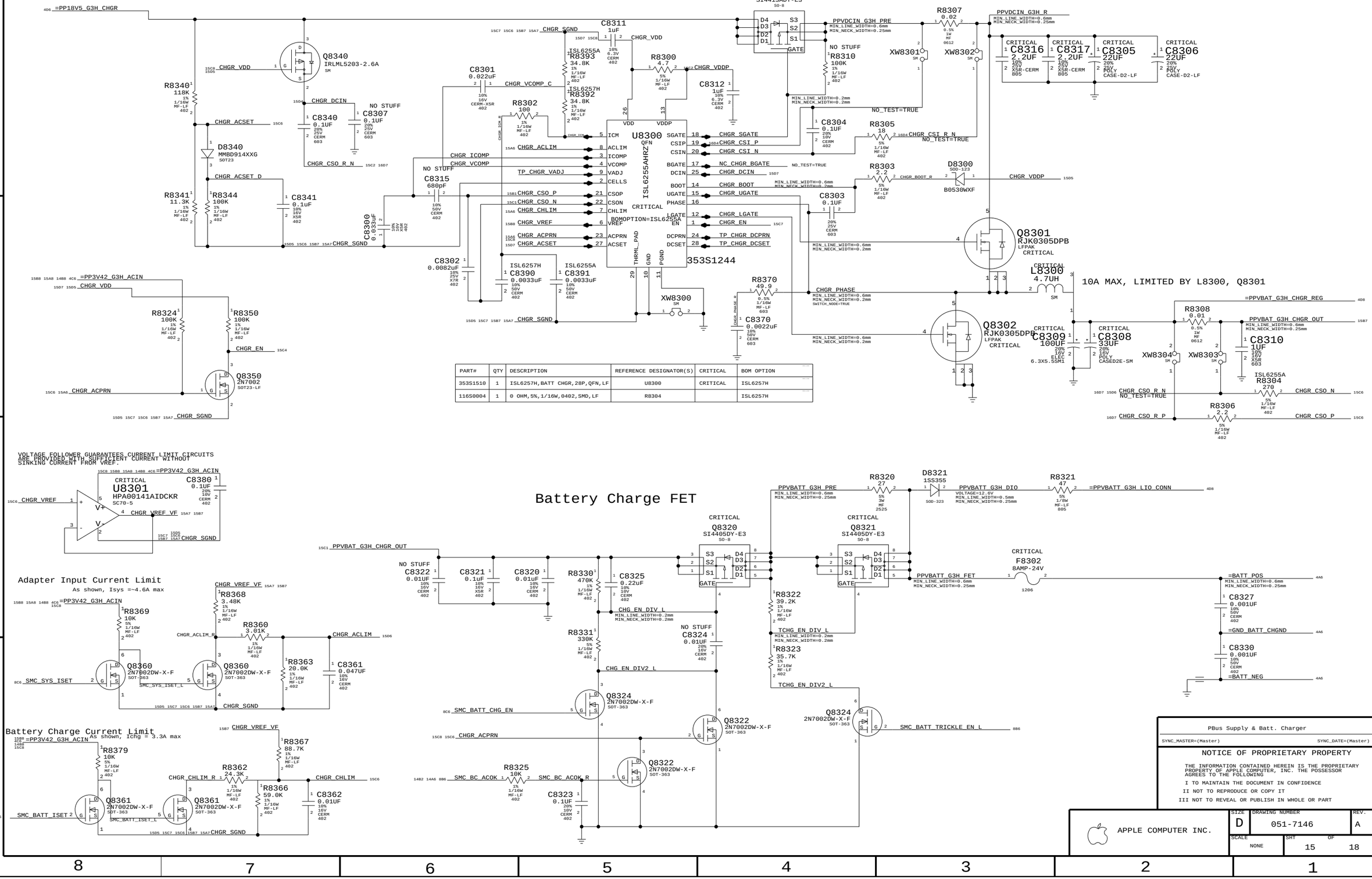
SCALE: NONE	SHT 14 OF 18	

PBus Supply & Battery Charger



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H,BATT CHGR,28P,QFN,LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM,5%,1/16W,0402,SMD,LF	R8304		ISL6257H

PBus Supply & Batt. Charger

SYNC_MASTER=(Master) SYNC_DATE=(Master)

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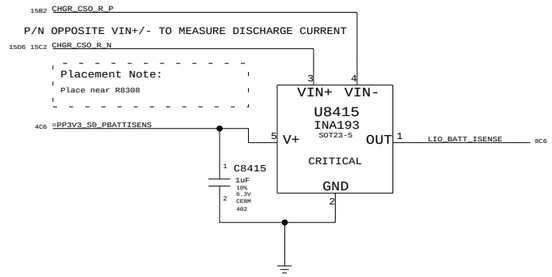
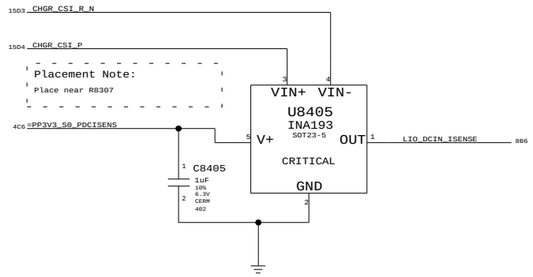
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A
SCALE: NONE	SHT 15 OF 18	

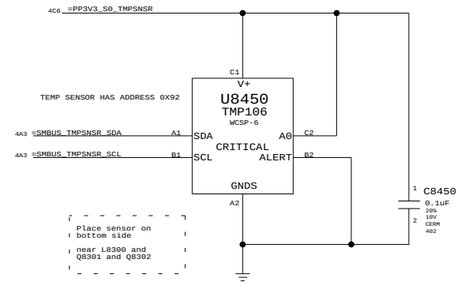
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER=(Master) SYNC_DATE=(Master)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7146	A

SCALE	SHT	OF
NONE	16	18

```
Title:       Basenet Report
Design:      lio
Date:        Sep 22 14:52:31 2006

Base nets and synonyms for lio_lib.LIO(@lio_lib.lio(sch_1))
Base Signal              Synonyms                                  Location([Zone][dir])

3V3S3_BOOT               3V3S3_BOOT - @lio_lib.LIO                 13C5
3V3S3_BOOT_R             3V3S3_BOOT_R - @lio_lib.LIO               13C5
3V3S3_COMP               3V3S3_COMP - @lio_lib.LIO                 13B6
3V3S3_COMP_R             3V3S3_COMP_R - @lio_lib.LIO               13B7
3V3S3_FB                 3V3S3_FB - @lio_lib.LIO                   13B6
3V3S3_FB_R               3V3S3_FB_R - @lio_lib.LIO                 13B2
3V3S3_FCCM               3V3S3_FCCM - @lio_lib.LIO                 13B6
3V3S3_FSET               3V3S3_FSET - @lio_lib.LIO                 13C6
3V3S3_ISEN               3V3S3_ISEN - @lio_lib.LIO                 13B5
3V3S3_LG                 3V3S3_LG - @lio_lib.LIO                   13B5
3V3S3_PHASE              3V3S3_PHASE - @lio_lib.LIO                13B5
3V3S3_UG                 3V3S3_UG - @lio_lib.LIO                   13C5
5V_REG_IN                5V_REG_IN - @lio_lib.LIO                  9A5
=BATT_POS                =BATT_POS - @lio_lib.LIO                  4A6 15B1
                         =PPBATTPOS_G3H_LIO_CONN -                 4A8 14A3
                         @lio_lib.LIO
                         BATT_POS - @lio_lib.LIO                   4A6
                         =PPBATTPOS_G3H_LIO_CONN -                 4A8 14A3
                         @lio_lib.LIO
=GND_AUDIO               =GND_AUDIO - @lio_lib.LIO                 4B8 8B3
                         =GND_AUDIO_CODEC - @lio_lib.LIO           4B6 9A6 9B6 9D2 10A8 10C8
                                                                   11B2 11B5 12A3 12A5 12A6
                                                                   12B3 12B5 12B8 12C3 12C5
                                                                   12C8 12D8
                         GND_AUDIO - @lio_lib.LIO                  4B6
                         =GND_AUDIO_CODEC - @lio_lib.LIO           4B6 9A6 9B6 9D2 10A8 10C8
                                                                   11B2 11B5 12A3 12A5 12A6
                                                                   12B3 12B5 12B8 12C3 12C5
                                                                   12C8 12D8
=GND_AUDIO_AMP           =GND_AUDIO_AMP - @lio_lib.LIO             4B8 8B6 10A8 10B5 10C8
                                                                   11C3
                         GND_AUDIO_AMP - @lio_lib.LIO              4B6
=GND_BATT_CHGND          =GND_BATT_CHGND - @lio_lib.LIO            4A6 15A1
                         GND_BATT_CHGND - @lio_lib.LIO             4A8
=GND_CHASSIS_AUDIO_J     =GND_CHASSIS_AUDIO_JACK -                 4B6 11A8 11B1 11B1 11B7
ACK                      @lio_lib.LIO                              11C8
                         =GND_CHASSIS_PCIE_EXCARD_LEFT -           4B6 6B1 6D3
                         @lio_lib.LIO
                         CHASSIS_GND1 - @lio_lib.LIO               4B8
                         =GND_CHASSIS_PCIE_EXCARD_LEFT -           4B6 6B1 6D3
                         @lio_lib.LIO
=GND_CHASSIS_AUDIO_M     =GND_CHASSIS_AUDIO_MIC -                  4A6 12A6
IC                       @lio_lib.LIO
                         =GND_CHASSIS_AUDIO_SPKRCONN -             4A6 11B1
                         @lio_lib.LIO
                         =GND_CHASSIS_PCIE_EXCARD_RIGHT -          4A6 6B2
                         @lio_lib.LIO
                         CHASSIS_GND2 - @lio_lib.LIO               4A8
                         =GND_CHASSIS_PCIE_EXCARD_RIGHT -          4A6 6B2
                         @lio_lib.LIO
                         =GND_CHASSIS_AUDIO_SPKRCONN -             4A6 11B1
                         @lio_lib.LIO
=GND_CHASSIS_DCIN_JA     =GND_CHASSIS_DCIN_JACK -                  4A6 14C8
CK                       @lio_lib.LIO
                         =GND_CHASSIS_LTUSB - @lio_lib.LIO         4A6 5B2
                         CHASSIS_GND3 - @lio_lib.LIO               4A8
                         =GND_CHASSIS_LTUSB - @lio_lib.LIO         4A6 5B2
=LEFT_USB_PWRON          =LEFT_USB_PWRON - @lio_lib.LIO            4D1 5C7
                         =LIO_P3V3S3_EN - @lio_lib.LIO             4D1 13B8
                         LIO_S3_EN - @lio_lib.LIO                  4D3 8B6
                         =LIO_P3V3S3_EN - @lio_lib.LIO             4D1 13B8
=PP1V5_S0                =PP1V5_S0 - @lio_lib.LIO                  4C8 8C6
                         =PP1V5_S0_EXCARD - @lio_lib.LIO           4C6 6C7 6C8
                         =PP1V5_S0_MINI - @lio_lib.LIO             4C6 7C2
                         PP1V5_S0 - @lio_lib.LIO                   4C6
                         =PP1V5_S0_MINI - @lio_lib.LIO             4C6 7C2
                         =PP1V5_S0_EXCARD - @lio_lib.LIO           4C6 6C7 6C8
=PP3V3_S0_AUDIO          =PP3V3_S0_AUDIO - @lio_lib.LIO            4C6 9A6 9D7 11B8 11D8
                                                                   12B5
                         =PP3V3_S0_EXCARD - @lio_lib.LIO           4C6 6B4 6C7
                         =PP3V3_S0_FET - @lio_lib.LIO              4C8 13C1
                         =PP3V3_S0_PDCISENS - @lio_lib.LIO         4C6 16C4
                         =PP3V3_S0_TMPSNSR - @lio_lib.LIO          4C6 16B5
                         =PP3V3_S0_PBATTISENS - @lio_lib.LIO       4C6 16C7
                         =PP3V3_S0_MINI - @lio_lib.LIO             4C6 7D2
                         PP3V3_S0_LIO - @lio_lib.LIO               4C6
                         =PP3V3_S0_TMPSNSR - @lio_lib.LIO          4C6 16B5
                         =PP3V3_S0_PDCISENS - @lio_lib.LIO         4C6 16C4
                         =PP3V3_S0_PBATTISENS - @lio_lib.LIO       4C6 16C7
                         =PP3V3_S0_MINI - @lio_lib.LIO             4C6 7D2
                         =PP3V3_S0_FET - @lio_lib.LIO              4C8 13C1
                         =PP3V3_S0_EXCARD - @lio_lib.LIO           4C6 6B4 6C7
=PP3V3_S3_EXCARD         =PP3V3_S3_EXCARD - @lio_lib.LIO           4C6 6B8 6C7 6C8
                         =PP3V3_S3_REG - @lio_lib.LIO              4C8 13B1
                         =PP3V3_S3_MINI - @lio_lib.LIO             4C6 7C2
                         PP3V3_S3_LIO - @lio_lib.LIO               4C6
                         =PP3V3_S3_REG - @lio_lib.LIO              4C8 13B1
                         =PP3V3_S3_MINI - @lio_lib.LIO             4C6 7C2
=PP3V42_G3H              =PP3V42_G3H - @lio_lib.LIO                4D8 8C6
                         =PP3V42_G3H_ACIN - @lio_lib.LIO           4C6 14B8 15A8 15B8 15B8
                                                                   15C8
                         PP3V42_G3H - @lio_lib.LIO                 4D6
                         =PP3V42_G3H_ACIN - @lio_lib.LIO           4C6 14B8 15A8 15B8 15B8
                                                                   15C8
=PP5V_S0_AUDIO           =PP5V_S0_AUDIO - @lio_lib.LIO             4B8 8C6 9A6
                         PP5V_S0_AUDIO - @lio_lib.LIO              4B6
=PP5V_S0_AUDIO_AMP       =PP5V_S0_AUDIO_AMP - @lio_lib.LIO         4B8 8C6 10B8 10D8
                         PP5V_S0_AUDIO_AMP - @lio_lib.LIO          4B6
=PP5V_S5                 =PP5V_S5 - @lio_lib.LIO                   4B8 9C6
                         =PP5V_S5_3V3S3 - @lio_lib.LIO             4B6 13C8
                         =PP5V_S5_LTUSB - @lio_lib.LIO             4B6 5C7
                         PP5V_S5 - @lio_lib.LIO                    4B6
                         =PP5V_S5_LTUSB - @lio_lib.LIO             4B6 5C7
                         =PP5V_S5_3V3S3 - @lio_lib.LIO             4B6 13C8
=PP18V5_G3H_CHGR         =PP18V5_G3H_CHGR - @lio_lib.LIO           4D6 15D8
                         =PP18V5_G3H_INRUSH - @lio_lib.LIO         4D8 14B3
                         PP18V5_G3H_CHGR - @lio_lib.LIO            4D6
                         =PP18V5_G3H_INRUSH - @lio_lib.LIO         4D8 14B3
=PPBUS_G3H_LIO_CONN      =PPBUS_G3H_LIO_CONN - @lio_lib.LIO        4D6 14A3
                         =PPVBAT_G3H_CHGR_REG - @lio_lib.LIO       4D8 15C1
                         =PPVIN_S3_3V3S3 - @lio_lib.LIO            4D6 13D8
                         PPVBAT_G3H_CHGR_REG - @lio_lib.LIO        4D6
                         =PPVIN_S3_3V3S3 - @lio_lib.LIO            4D6 13D8
                         =PPVBAT_G3H_CHGR_REG - @lio_lib.LIO       4D8 15C1
=PPDCIN_G3H              =PPDCIN_G3H - @lio_lib.LIO                4D6 8C6
                         =PPVBATT_G3H_LIO_CONN -                   4D8 15B2
                         @lio_lib.LIO
                         =PPDCIN_G3H_LIO_CONN - @lio_lib.LIO       4D8 14D3
                         PPDCIN_G3H - @lio_lib.LIO                 4D6
                         =PPVBATT_G3H_LIO_CONN -                   4D8 15B2
                         @lio_lib.LIO
                         =PPDCIN_G3H_LIO_CONN - @lio_lib.LIO       4D8 14D3
=SMBUS_EXCARD_SCL        =SMBUS_EXCARD_SCL - @lio_lib.LIO          4A3 6C3
                         SMBUS_SB_SCL - @lio_lib.LIO               4A6 8C3
=SMBUS_EXCARD_SDA        =SMBUS_EXCARD_SDA - @lio_lib.LIO          4A3 6C3
                         SMBUS_SB_SDA - @lio_lib.LIO               4A6 8C3
=SMBUS_MINI_SCL          =SMBUS_MINI_SCL - @lio_lib.LIO            4A3 7B3
                         SMBUS_SMC_SCL - @lio_lib.LIO              4A6 8C3
                         =SMBUS_TMPSNSR_SCL - @lio_lib.LIO         4A3 16B5
                         SMBUS_SMC_SCL - @lio_lib.LIO              4A6 8C3
                         =SMBUS_TMPSNSR_SCL - @lio_lib.LIO         4A3 16B5
=SMBUS_MINI_SDA          =SMBUS_MINI_SDA - @lio_lib.LIO            4A3 7B3
                         SMBUS_SMC_SDA - @lio_lib.LIO              4A6 8C3
                         =SMBUS_TMPSNSR_SDA - @lio_lib.LIO         4A3 16B5
                         SMBUS_SMC_SDA - @lio_lib.LIO              4A6 8C3
                         =SMBUS_TMPSNSR_SDA - @lio_lib.LIO         4A3 16B5
ACIN_1V20_REF            ACIN_1V20_REF - @lio_lib.LIO              14A7
ACIN_DIV                 ACIN_DIV - @lio_lib.LIO                   14A7
ACIN_ENABLE_DIV2_L       ACIN_ENABLE_DIV2_L - @lio_lib.LIO         14B5
ACIN_ENABLE_DIV_L        ACIN_ENABLE_DIV_L - @lio_lib.LIO          14B5
ACOK_AND_PS_ON           ACOK_AND_PS_ON - @lio_lib.LIO             14A5
ACZ_BITCLK               ACZ_BITCLK - @lio_lib.LIO                 8B6 9D7
ACZ_RST_L                ACZ_RST_L - @lio_lib.LIO                  8B3 9C7
ACZ_SDATAIN<0>           ACZ_SDATAIN<0> - @lio_lib.LIO             8B6 9D7
ACZ_SDATAOUT             ACZ_SDATAOUT - @lio_lib.LIO               8B6 9D7
ACZ_SYNC                 ACZ_SYNC - @lio_lib.LIO                   8B6 9D7
ADAPTER_SENSE            ADAPTER_SENSE - @lio_lib.LIO              14D6
ADAPTER_SENSE_UF         ADAPTER_SENSE_UF - @lio_lib.LIO           14D7
AUDIO_SHIELD_PLANE       AUDIO_SHIELD_PLANE - @lio_lib.LIO         11B3
AUD_4V5_SHDN_L           AUD_4V5_SHDN_L - @lio_lib.LIO             9A6
AUD_ANALOG_FILT_1        AUD_ANALOG_FILT_1 - @lio_lib.LIO          9C4
AUD_ANALOG_FILT_2        AUD_ANALOG_FILT_2 - @lio_lib.LIO          9C4
AUD_BI_PORT_A_L          AUD_BI_PORT_A_L - @lio_lib.LIO            9C1 12B3
AUD_BI_PORT_A_R          AUD_BI_PORT_A_R - @lio_lib.LIO            9C1 12B3
AUD_BI_PORT_B_L          AUD_BI_PORT_B_L - @lio_lib.LIO            9C1 12B6
                         AUD_BI_PORT_B_R - @lio_lib.LIO            9C1 12A6
AUD_BI_PORT_C_L          AUD_BI_PORT_C_L - @lio_lib.LIO            9C7 10C8
AUD_BI_PORT_C_R          AUD_BI_PORT_C_R - @lio_lib.LIO            9C7 10B8
AUD_BI_PORT_D_L          AUD_BI_PORT_D_L - @lio_lib.LIO            9C7 12A6
AUD_BI_PORT_D_R          AUD_BI_PORT_D_R - @lio_lib.LIO            9C7 12A6
AUD_BI_PORT_E_L          AUD_BI_PORT_E_L - @lio_lib.LIO            9C1 12A6
AUD_BI_PORT_E_R          AUD_BI_PORT_E_R - @lio_lib.LIO            9C1 12A6
AUD_BI_PORT_F_L          AUD_BI_PORT_F_L - @lio_lib.LIO            9C1 12D4
AUD_BI_PORT_F_R          AUD_BI_PORT_F_R - @lio_lib.LIO            9C1 12C4
AUD_BYPASS               AUD_BYPASS - @lio_lib.LIO                 9C4
AUD_CONNJ1_RING          AUD_CONNJ1_RING - @lio_lib.LIO            11C7
AUD_CONNJ1_RING_F        AUD_CONNJ1_RING_F - @lio_lib.LIO          11C6
AUD_CONNJ1_SLEEVE        AUD_CONNJ1_SLEEVE - @lio_lib.LIO          11D7
AUD_CONNJ1_SLEEVEDET     AUD_CONNJ1_SLEEVEDET - @lio_lib.LIO       11C7
AUD_CONNJ1_SLEEVEDET     AUD_CONNJ1_SLEEVEDET_F -                  11C6
_F                       @lio_lib.LIO
AUD_CONNJ1_SLEEVE_F      AUD_CONNJ1_SLEEVE_F - @lio_lib.LIO        11D6
AUD_CONNJ1_TIP           AUD_CONNJ1_TIP - @lio_lib.LIO             11C7
AUD_CONNJ1_TIPDET        AUD_CONNJ1_TIPDET - @lio_lib.LIO          11C7
AUD_CONNJ1_TIPDET_F      AUD_CONNJ1_TIPDET_F - @lio_lib.LIO        11D6
AUD_CONNJ1_TIP_F         AUD_CONNJ1_TIP_F - @lio_lib.LIO           11C6
AUD_CONNJ2_RING          AUD_CONNJ2_RING - @lio_lib.LIO            11B7
AUD_CONNJ2_RING_F        AUD_CONNJ2_RING_F - @lio_lib.LIO          11B5
AUD_CONNJ2_SLEEVE        AUD_CONNJ2_SLEEVE - @lio_lib.LIO          11B7
AUD_CONNJ2_SLEEVEDET     AUD_CONNJ2_SLEEVEDET - @lio_lib.LIO       11A7
AUD_CONNJ2_SLEEVEDET     AUD_CONNJ2_SLEEVEDET_F -                  11A5
_F                       @lio_lib.LIO
AUD_CONNJ2_SLEEVE_F      AUD_CONNJ2_SLEEVE_F - @lio_lib.LIO        11B5
AUD_CONNJ2_TIP           AUD_CONNJ2_TIP - @lio_lib.LIO             11B7
AUD_CONNJ2_TIPDET        AUD_CONNJ2_TIPDET - @lio_lib.LIO          11B7
AUD_CONNJ2_TIPDET_F      AUD_CONNJ2_TIPDET_F - @lio_lib.LIO        11B5
AUD_CONNJ2_TIP_F         AUD_CONNJ2_TIP_F - @lio_lib.LIO           11B5
AUD_GPIO_0               AUD_GPIO_0 - @lio_lib.LIO                 9B8 10C8
AUD_GPIO_0_R             AUD_GPIO_0_R - @lio_lib.LIO               9B7 9C7
AUD_GPIO_1               AUD_GPIO_1 - @lio_lib.LIO                 9B8 12C3
AUD_GPIO_1_R             AUD_GPIO_1_R - @lio_lib.LIO               9B7 9C7
AUD_INJACK_INSERT_L      AUD_INJACK_INSERT_L - @lio_lib.LIO        12C6
AUD_J1_COM               AUD_J1_COM - @lio_lib.LIO                 11C4
AUD_J1_DET_RC            AUD_J1_DET_RC - @lio_lib.LIO              12D7
AUD_J1_SLEEVEDET_INV     AUD_J1_SLEEVEDET_INV - @lio_lib.LIO       12C7
AUD_J1_SLEEVEDET_R       AUD_J1_SLEEVEDET_R - @lio_lib.LIO         11C3 12C6 12C8
AUD_J1_TIPDET_R          AUD_J1_TIPDET_R - @lio_lib.LIO            11C3 12D8
AUD_J2_COM               AUD_J2_COM - @lio_lib.LIO                 11B4
AUD_J2_DET_RC            AUD_J2_DET_RC - @lio_lib.LIO              12B7
AUD_J2_OPT_OUT           AUD_J2_OPT_OUT - @lio_lib.LIO             11B7
AUD_J2_TIPDET_R          AUD_J2_TIPDET_R - @lio_lib.LIO            11A3 12B8
AUD_OUTJACK_INSERT_L     AUD_OUTJACK_INSERT_L - @lio_lib.LIO       12D7
AUD_PORTA_DET_L          AUD_PORTA_DET_L - @lio_lib.LIO            12D5
AUD_PORTA_L              AUD_PORTA_L - @lio_lib.LIO                11C3 12B1
AUD_PORTA_L_R            AUD_PORTA_L_R - @lio_lib.LIO              12B1 12B3
AUD_PORTA_R              AUD_PORTA_R - @lio_lib.LIO                11C3 12A1
AUD_PORTA_R_R            AUD_PORTA_R_R - @lio_lib.LIO              12A3 12B1
AUD_PORTE_DET_L          AUD_PORTE_DET_L - @lio_lib.LIO            12D5
AUD_PORTF_L              AUD_PORTF_L - @lio_lib.LIO                11B3 12D1
AUD_PORTF_L_R            AUD_PORTF_L_R - @lio_lib.LIO              12D3
AUD_PORTF_R              AUD_PORTF_R - @lio_lib.LIO                11B3 12C1
AUD_PORTF_R_R            AUD_PORTF_R_R - @lio_lib.LIO              12C3
AUD_SENSE_A              AUD_SENSE_A - @lio_lib.LIO                9C1 12C5 12D8
AUD_SENSE_B              AUD_SENSE_B - @lio_lib.LIO                9C1 12C4 12C8 12D8
AUD_SPDIF_IN             AUD_SPDIF_IN - @lio_lib.LIO               9C1 11B3
AUD_SPDIF_OUT            AUD_SPDIF_OUT - @lio_lib.LIO              9D1 11D3
AUD_SPDIF_OUT_R          AUD_SPDIF_OUT_R - @lio_lib.LIO            9D4
AUD_SPKRAMP_INL_L        AUD_SPKRAMP_INL_L - @lio_lib.LIO          10C7
AUD_SPKRAMP_INR_L        AUD_SPKRAMP_INR_L - @lio_lib.LIO          10B7
AUD_SPKRAMP_SHUTDOWN     AUD_SPKRAMP_SHUTDOWN_L -                  10A8 10C7
_L                       @lio_lib.LIO
AUD_VREF_FILT            AUD_VREF_FILT - @lio_lib.LIO              9C4
AUD_VREF_PORT_B          AUD_VREF_PORT_B - @lio_lib.LIO            9C1 12B6
BAL_IN_COM               BAL_IN_COM - @lio_lib.LIO                 9C7 12A3
BAL_IN_L                 BAL_IN_L - @lio_lib.LIO                   9C7 12A3
BAL_IN_R                 BAL_IN_R - @lio_lib.LIO                   9C7 12A3
BEEP                     BEEP - @lio_lib.LIO                       9C6
CHGR_ACLIM               CHGR_ACLIM - @lio_lib.LIO                 15A6 15D6
CHGR_ACLIM_R             CHGR_ACLIM_R - @lio_lib.LIO               15A7
CHGR_ACPRN               CHGR_ACPRN - @lio_lib.LIO                 15A6 15C6 15C8
CHGR_ACSET               CHGR_ACSET - @lio_lib.LIO                 15C6 15D7
CHGR_ACSET_D             CHGR_ACSET_D - @lio_lib.LIO               15C7
CHGR_BOOT                CHGR_BOOT - @lio_lib.LIO                  15C4
CHGR_BOOT_R              CHGR_BOOT_R - @lio_lib.LIO                15C3
CHGR_CHLIM               CHGR_CHLIM - @lio_lib.LIO                 15A6 15C6
CHGR_CHLIM_R             CHGR_CHLIM_R - @lio_lib.LIO               15A7
CHGR_CSI_N               CHGR_CSI_N - @lio_lib.LIO                 15D4
CHGR_CSI_P               CHGR_CSI_P - @lio_lib.LIO                 15D4 16D4
CHGR_CSI_R_N             CHGR_CSI_R_N - @lio_lib.LIO               15D3 16D4
CHGR_CSO_N               CHGR_CSO_N - @lio_lib.LIO                 15C1 15C6
CHGR_CSO_P               CHGR_CSO_P - @lio_lib.LIO                 15B1 15C6
CHGR_CSO_R_N             CHGR_CSO_R_N - @lio_lib.LIO               15C2 15D6 16D7
CHGR_CSO_R_P             CHGR_CSO_R_P - @lio_lib.LIO               15B2 16D7
CHGR_DCIN                CHGR_DCIN - @lio_lib.LIO                  15D4 15D7
CHGR_EN                  CHGR_EN - @lio_lib.LIO                    15C4 15C7
CHGR_ICM                 CHGR_ICM - @lio_lib.LIO                   15D5
CHGR_ICM_R               CHGR_ICM_R - @lio_lib.LIO                 15D6
CHGR_ICOMP               CHGR_ICOMP - @lio_lib.LIO                 15D6
CHGR_LGATE               CHGR_LGATE - @lio_lib.LIO                 15C4
CHGR_PHASE               CHGR_PHASE - @lio_lib.LIO                 15C4
CHGR_PHASE_R             CHGR_PHASE_R - @lio_lib.LIO               15C4
CHGR_SGATE               CHGR_SGATE - @lio_lib.LIO                 15D4
CHGR_SGND                CHGR_SGND - @lio_lib.LIO                  15A7 15A7 15B7 15B7 15C6
                                                                   15C7 15D5
CHGR_UGATE               CHGR_UGATE - @lio_lib.LIO                 15C4
CHGR_VCOMP               CHGR_VCOMP - @lio_lib.LIO                 15D6
CHGR_VCOMP_C             CHGR_VCOMP_C - @lio_lib.LIO               15D6
CHGR_VDD                 CHGR_VDD - @lio_lib.LIO                   15C8 15D5 15D7
CHGR_VDDP                CHGR_VDDP - @lio_lib.LIO                  15C2 15D5
CHGR_VREF                CHGR_VREF - @lio_lib.LIO                  15B8 15C6
CHGR_VREF_VF             CHGR_VREF_VF - @lio_lib.LIO               15A7 15B7 15B7
CHG_EN_DIV2_L            CHG_EN_DIV2_L - @lio_lib.LIO              15A5
CHG_EN_DIV_L             CHG_EN_DIV_L - @lio_lib.LIO               15B5
CODEC_VREF_PORT_B        CODEC_VREF_PORT_B - @lio_lib.LIO          9C4
EC_HOLE1                 EC_HOLE1 - @lio_lib.LIO                   6D3
EC_HOLE2                 EC_HOLE2 - @lio_lib.LIO                   6B2
EXCARD_CLKREQ_CONN       EXCARD_CLKREQ_CONN - @lio_lib.LIO         6B3
EXCARD_CLKREQ_CONN_L     EXCARD_CLKREQ_CONN_L - @lio_lib.LIO       6A4 6C3
EXCARD_CLKREQ_L          EXCARD_CLKREQ_L - @lio_lib.LIO            4C6 6B2 8C6
EXCARD_CPPE_L            EXCARD_CPPE_L - @lio_lib.LIO              6A8 6C3 6C3
EXCARD_CPUSB_L           EXCARD_CPUSB_L - @lio_lib.LIO             6A8 6C3 6C3
EXCARD_OC_L              EXCARD_OC_L - @lio_lib.LIO                4C6 6C7 8C6
EXCARD_RCLKEN            EXCARD_RCLKEN - @lio_lib.LIO              6B3 6C5
EXCARD_SHDN_L_R          EXCARD_SHDN_L_R - @lio_lib.LIO            6C6
GND_3V3S3_SGND           GND_3V3S3_SGND - @lio_lib.LIO             13B7
GND_ADAPTER_UF           GND_ADAPTER_UF - @lio_lib.LIO             14D7
LEFT_USB_EMI_N           LEFT_USB_EMI_N - @lio_lib.LIO             5C4
LEFT_USB_EMI_P           LEFT_USB_EMI_P - @lio_lib.LIO             5C4
LEFT_USB_GND             LEFT_USB_GND - @lio_lib.LIO               5C3
LEFT_USB_N               LEFT_USB_N - @lio_lib.LIO                 4A3 5C4
                         USB2_LT_N - @lio_lib.LIO                  4A6 8C3
LEFT_USB_OC_L            LEFT_USB_OC_L - @lio_lib.LIO              4A3 5C5
                         LTUSB_OC_L - @lio_lib.LIO                 4A6 8C6
LEFT_USB_P               LEFT_USB_P - @lio_lib.LIO                 4B3 5C4
                         USB2_LT_P - @lio_lib.LIO                  4B6 8C3
LIO_BATT_ISENSE          LIO_BATT_ISENSE - @lio_lib.LIO            8C6 16C6
LIO_DCIN_ISENSE          LIO_DCIN_ISENSE - @lio_lib.LIO            8B6 16C2
LIO_P3V3S0_EN_L          LIO_P3V3S0_EN_L - @lio_lib.LIO            8B6 13C3
LIO_P3V3S0_EN_R_L        LIO_P3V3S0_EN_R_L - @lio_lib.LIO          13C2
LIO_PLT_RESET_L          LIO_PLT_RESET_L - @lio_lib.LIO            4C6 8C6
                         PLT_RESET_L - @lio_lib.LIO                4C3 6C7 7C3
MAX9705L_LIN             MAX9705L_LIN - @lio_lib.LIO               10C6
MAX9705L_PIN             MAX9705L_PIN - @lio_lib.LIO               10C6
MAX9705R_LIN             MAX9705R_LIN - @lio_lib.LIO               10A6
MAX9705R_PIN             MAX9705R_PIN - @lio_lib.LIO               10B6
MAX9890_CEXT             MAX9890_CEXT - @lio_lib.LIO               12B1
MAX9890_INL              MAX9890_INL - @lio_lib.LIO                12B3
MAX9890_INR              MAX9890_INR - @lio_lib.LIO                12B3
MIC_HI                   MIC_HI - @lio_lib.LIO                     11C3 12B8
MIC_IN                   MIC_IN - @lio_lib.LIO                     12B7
MIC_LO                   MIC_LO - @lio_lib.LIO                     11C3 12A8
MIC_SHIELD               MIC_SHIELD - @lio_lib.LIO                 11C3 12A8
MINI_CLKREQ_L            MINI_CLKREQ_L - @lio_lib.LIO              4B6 7C6 8C6
NC_AUD_GPIO_2            NC_AUD_GPIO_2 - @lio_lib.LIO              9C6
NC_CHGR_BGATE            NC_CHGR_BGATE - @lio_lib.LIO              15D4
NC_CODEC_VREF_PORT_A     NC_CODEC_VREF_PORT_A - @lio_lib.LIO       9C4
NC_CODEC_VREF_PORT_C     NC_CODEC_VREF_PORT_C - @lio_lib.LIO       9C4
NC_CODEC_VREF_PORT_D     NC_CODEC_VREF_PORT_D - @lio_lib.LIO       9C4
NC_LED_WLAN_L            NC_LED_WLAN_L - @lio_lib.LIO              7B3
NC_LED_WPAN_L            NC_LED_WPAN_L - @lio_lib.LIO              7B3
NC_LED_WWAN_L            NC_LED_WWAN_L - @lio_lib.LIO              7B3
NC_LIO_P3V3S3_PGOOD      NC_LIO_P3V3S3_PGOOD - @lio_lib.LIO        13B8
NC_NC1                   NC_NC1 - @lio_lib.LIO                     9C4
NC_NC2                   NC_NC2 - @lio_lib.LIO                     9B4
NC_UIM_CLK               NC_UIM_CLK - @lio_lib.LIO                 7C3
NC_UIM_DATA              NC_UIM_DATA - @lio_lib.LIO                7C3
NC_UIM_PWR               NC_UIM_PWR - @lio_lib.LIO                 7C3
NC_UIM_RESET             NC_UIM_RESET - @lio_lib.LIO               7C3
NC_UIM_VPP               NC_UIM_VPP - @lio_lib.LIO                 7C3
NC_VOL_DOWN              NC_VOL_DOWN - @lio_lib.LIO                9C6
NC_VOL_UP                NC_VOL_UP - @lio_lib.LIO                  9C6
NC_VREG_POK              NC_VREG_POK - @lio_lib.LIO                9A4
NC_W_DISABLE_L           NC_W_DISABLE_L - @lio_lib.LIO             7C3
ONEWIRE_DCIN_DIV         ONEWIRE_DCIN_DIV - @lio_lib.LIO           14C5
ONEWIRE_EN               ONEWIRE_EN - @lio_lib.LIO                 14C3
ONEWIRE_ESD              ONEWIRE_ESD - @lio_lib.LIO                14C4
ONEWIRE_OVERVOLT         ONEWIRE_OVERVOLT - @lio_lib.LIO           14C4
ONEWIRE_PWR_EN_L         ONEWIRE_PWR_EN_L - @lio_lib.LIO           14C2
ONEWIRE_PWR_EN_L_DIV     ONEWIRE_PWR_EN_L_DIV - @lio_lib.LIO       14C2
PCIE_CLK100M_EXCARD_     PCIE_CLK100M_EXCARD_N -                   4D6 6C3 8B2
N                        @lio_lib.LIO
PCIE_CLK100M_EXCARD_     PCIE_CLK100M_EXCARD_P -                   4D6 6C3 8B2
P                        @lio_lib.LIO
PCIE_CLK100M_EXCARD_     PCIE_CLK100M_EXCARD_UF_N -                4D6 8B4
UF_N                     @lio_lib.LIO
PCIE_CLK100M_EXCARD_     PCIE_CLK100M_EXCARD_UF_P -                4D6 8B4
UF_P                     @lio_lib.LIO
PCIE_CLK100M_MINI_N      PCIE_CLK100M_MINI_N - @lio_lib.LIO        4B6 7C6 8C2
PCIE_CLK100M_MINI_P      PCIE_CLK100M_MINI_P - @lio_lib.LIO        4B6 7C6 8C2
PCIE_CLK100M_MINI_UF     PCIE_CLK100M_MINI_UF_N -                  4B6 8C4
_N                       @lio_lib.LIO
PCIE_CLK100M_MINI_UF     PCIE_CLK100M_MINI_UF_P -                  4B6 8C4
_P                       @lio_lib.LIO
PCIE_EXCARD_D2R_N        PCIE_EXCARD_D2R_N - @lio_lib.LIO          4D6 6C3 8B3
PCIE_EXCARD_D2R_P        PCIE_EXCARD_D2R_P - @lio_lib.LIO          4D6 6C3 8B3
PCIE_EXCARD_R2D_N        PCIE_EXCARD_R2D_N - @lio_lib.LIO          4C6 6C3 8B3
PCIE_EXCARD_R2D_P        PCIE_EXCARD_R2D_P - @lio_lib.LIO          4D6 6C3 8B3
PCIE_MINI_D2R_N          PCIE_MINI_D2R_N - @lio_lib.LIO            4B6 7C6 8C3
PCIE_MINI_D2R_P          PCIE_MINI_D2R_P - @lio_lib.LIO            4B6 7C6 8C3
PCIE_MINI_R2D_N          PCIE_MINI_R2D_N - @lio_lib.LIO            4C6 7B6 8C3
PCIE_MINI_R2D_P          PCIE_MINI_R2D_P - @lio_lib.LIO            4C6 7B6 8B3
PCIE_WAKE_EXCARD_L       PCIE_WAKE_EXCARD_L - @lio_lib.LIO         4C3 6C3
                         PCIE_WAKE_L - @lio_lib.LIO                4C6 8C3
                         PCIE_WAKE_MINI_L - @lio_lib.LIO           4C3 7C6
                         PCIE_WAKE_L - @lio_lib.LIO                4C6 8C3
PLT_RESET_SWITCH_L       PLT_RESET_SWITCH_L - @lio_lib.LIO         6C3 6C3
PP1V5_S0_EXCARD_SWIT     PP1V5_S0_EXCARD_SWITCH -                  6C3 6C3
CH                       @lio_lib.LIO
PP3V3_AUDIO_CODEC        PP3V3_AUDIO_CODEC - @lio_lib.LIO          9D6
PP3V3_S0_AUDIO_F         PP3V3_S0_AUDIO_F - @lio_lib.LIO           12B4 12C8 12C8 12D8
PP3V3_S0_EXCARD_SWIT     PP3V3_S0_EXCARD_SWITCH -                  6C3 6C3
CH                       @lio_lib.LIO
PP3V3_S3_EXCARD_SWIT     PP3V3_S3_EXCARD_SWITCH -                  6C3 6C3
CH                       @lio_lib.LIO
PP4V5_AUDIO_ANALOG       PP4V5_AUDIO_ANALOG - @lio_lib.LIO         9A3 9D2 12C3 12C5
PP5V_PWRON_USB_EMI       PP5V_PWRON_USB_EMI - @lio_lib.LIO         5C3
PP5V_S0_AUDIO_F          PP5V_S0_AUDIO_F - @lio_lib.LIO            10B8 10D6
PP5V_S3_3V3S3_R          PP5V_S3_3V3S3_R - @lio_lib.LIO            13C6
PP5V_S3_USB_SWITCH       PP5V_S3_USB_SWITCH - @lio_lib.LIO         5C5
PP18V5_DCIN              PP18V5_DCIN - @lio_lib.LIO                14B8 14D1
PP18V5_DCIN_FUSE         PP18V5_DCIN_FUSE - @lio_lib.LIO           14D6
PP18V5_DCIN_ONEWIRE      PP18V5_DCIN_ONEWIRE - @lio_lib.LIO        14D5
PP18V5_DCIN_UF           PP18V5_DCIN_UF - @lio_lib.LIO             14D7
PPDCIN_G3H_LIO_CONN_R    PPDCIN_G3H_LIO_CONN_R -                   14D4
                         @lio_lib.LIO
PPVBATT_G3H_DIO          PPVBATT_G3H_DIO - @lio_lib.LIO            15B3
PPVBATT_G3H_FET          PPVBATT_G3H_FET - @lio_lib.LIO            15B3
PPVBATT_G3H_PRE          PPVBATT_G3H_PRE - @lio_lib.LIO            15B4
PPVBAT_G3H_CHGR_OUT      PPVBAT_G3H_CHGR_OUT - @lio_lib.LIO        15B7 15C1
PPVDCIN_G3H_PRE          PPVDCIN_G3H_PRE - @lio_lib.LIO            15D4
PPVDCIN_G3H_R            PPVDCIN_G3H_R - @lio_lib.LIO              15D2
SDATAIN                  SDATAIN - @lio_lib.LIO                    9C6
SMC_ADAPTER_EN           SMC_ADAPTER_EN - @lio_lib.LIO             8C6 14B6
SMC_BATT_CHG_EN          SMC_BATT_CHG_EN - @lio_lib.LIO            8C6 15A6
SMC_BATT_ISET            SMC_BATT_ISET - @lio_lib.LIO              8C6 15A8
SMC_BATT_ISET_L          SMC_BATT_ISET_L - @lio_lib.LIO            15A8
SMC_BATT_TRICKLE_EN_     SMC_BATT_TRICKLE_EN_L -                   8B6 15A3
L                        @lio_lib.LIO
SMC_BC_ACOK              SMC_BC_ACOK - @lio_lib.LIO                8B6 14A6 14B2 15A6
SMC_BC_ACOK_ONEWIRE_     SMC_BC_ACOK_ONEWIRE_R -                   14C1
R                        @lio_lib.LIO
SMC_BC_ACOK_R            SMC_BC_ACOK_R - @lio_lib.LIO              15A5
SMC_EXCARD_CP            SMC_EXCARD_CP - @lio_lib.LIO              6A6 8B6
SMC_EXCARD_PWR_EN        SMC_EXCARD_PWR_EN - @lio_lib.LIO          6C7 8B6
SMC_SYS_ISET             SMC_SYS_ISET - @lio_lib.LIO               8C6 15A8
SMC_SYS_ISET_L           SMC_SYS_ISET_L - @lio_lib.LIO             15A8
SPKRAMP_L_N_OUT          SPKRAM
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C8415	CAP_402	lio[16C7]
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D5100	DIODE_SCHOT_3P_A_SC-75	lio[5B3]
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D8200	DIODE_SCHOT_3P_A_SC-75	lio[14C7]
D8201	DIODE_SOD-323	lio[14D5]
D8300	DIODE_SCHOT_SOD-123	lio[15C3]
D8321	DIODE_SOD-323	lio[15B3]
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DZ7300	SUPPR_TRANSIENT_4P1_0405	lio[11C6]
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DZ7303	SUPPR_TRANSIENT1_402	lio[11C5]
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DZ7306	SUPPR_TRANSIENT1_402	lio[11C5]
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DZ7351	SUPPR_TRANSIENT_4P1_0405	lio[11A6]
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DZ7354	SUPPR_TRANSIENT1_402	lio[11A5]
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F8302	FUSE_1206	lio[15B3]
FL5500	FILTER_4P_1210-4SM1	lio[8C3]
FL5501	FILTER_4P_1210-4SM1	lio[8B3]
J5100	CON_F4RT_USB_S2MT_TH_F-RT-TH-USB-LFT	lio[5C2]
J5300	CON_F26RT_S2MT_SM_M59_F-RT-SM	lio[6D2]
J5400	CON_F52RT_D2MT_SM_F-ST-SM	lio[7C5]
J5500	CON_F80ST_D4MT_SM_F-ST-SM	lio[8C4]
J7300	CON_F8RT_SPDIFTRAN_TH2_F-RT-TH	lio[11D8]
J7350	CON_F8RT_SPDIFRCVR_TH2_F-RT-TH	lio[11B8]
J7380	CON_M8ST_S_TH_M-ST-TH	lio[11C1]
J8200	CON_F5RT_S2MT_TH3_F-RT-TH-MG3	lio[14D8]
J8215	CON_M12ST_S_SM_M-SSM	lio[14A4]
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L7358	IND_0402	lio[11A4]
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L7800	IND_IHLP	lio[13B3]
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L8201	IND_SM-1	lio[14D6]
L8300	IND_3P_SM	lio[15C2]
Q5360	TRA_2N7002_SOT23-LF	lio[6B3]
Q7400	TRA_2N7002DW_SOT-363	lio[12C7 12D7]
Q7401	TRA_2N7002DW_SOT-363	lio[12D5 12D6]
Q7402	TRA_2N7002DW_SOT-363	lio[12B7 12B6]
Q7800	TRA_FDM6296_MICROFET 3X3	lio[13C4]
Q7801	TRA_FDM6296_MICROFET 3X3	lio[13B4]
Q7890	TRA_IRF7707_TSSOP	lio[13C2]
Q8200	TRA_2N7002DW_SOT-363	lio[14C1 14C3]
Q8201	TRA_2N7002DW_SOT-363	lio[14C1 14C2]
Q8209	TRA_TP0610_S0T23-3	lio[14D2]
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Q8300	TRA_SI4413ADY_SO-8	lio[15D4]
Q8301	TRA_RJK_LFPAK	lio[15C3]
Q8302	TRA_RJK_LFPAK	lio[15C3]
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Q8361	TRA_2N7002DW_SOT-363	lio[15A8 15A7]
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U5360	MC74VHC1G00_SC70-5	lio[6B2]
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U7220	MAX9705_TDFN1	lio[10B5]
U7400	MAX9890_UCSP1	lio[12C2]
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U8250	MC74VHC1G08_SC70	lio[14A5]
U8290	COMPARATOR_LM397_SOT 23-5	lio[14C4]
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U8405	INA193_SOT23-5	lio[16C3]
U8415	INA193_SOT23-5	lio[16C6]
U8450	TMP106_WCSP-6	lio[16B5]
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XW8302	SHORT_SM	lio[15D3]
XW8303	SHORT_SM	lio[15C2]
XW8304	SHORT_SM	lio[15C2]