1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,M59

09/19/2006

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
A		463525	PRODUCTION RELEASE	9/19/2006	9/19/2006

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7150	1	SCHEM,MLB,M59	SCH	CRITICAL	
820-2054	1	PCBF,MLB,M59	PCB	CRITICAL	

DRAWING
TITLE=M59_MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Sep 25 10:45:58 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

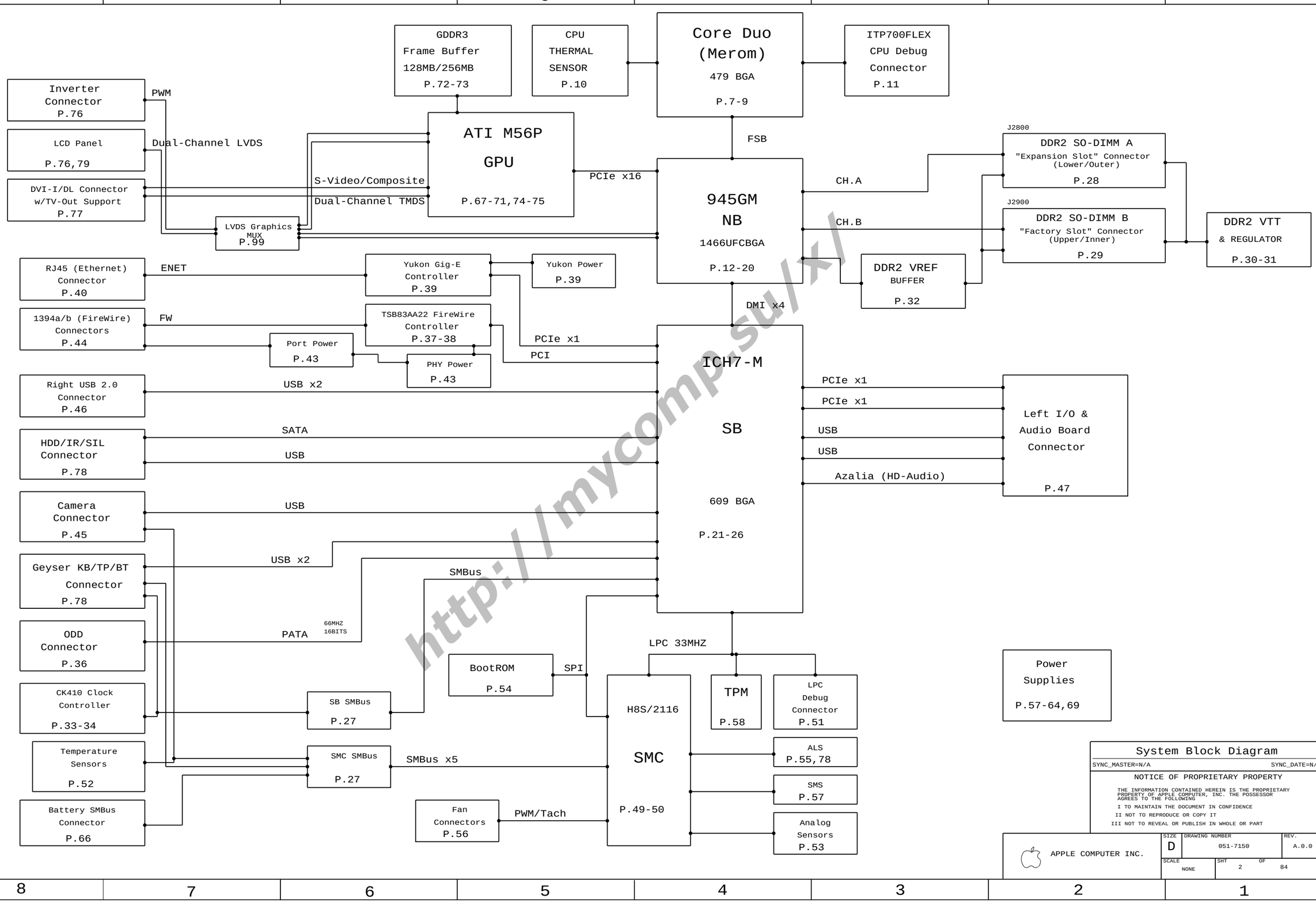
SIZE D

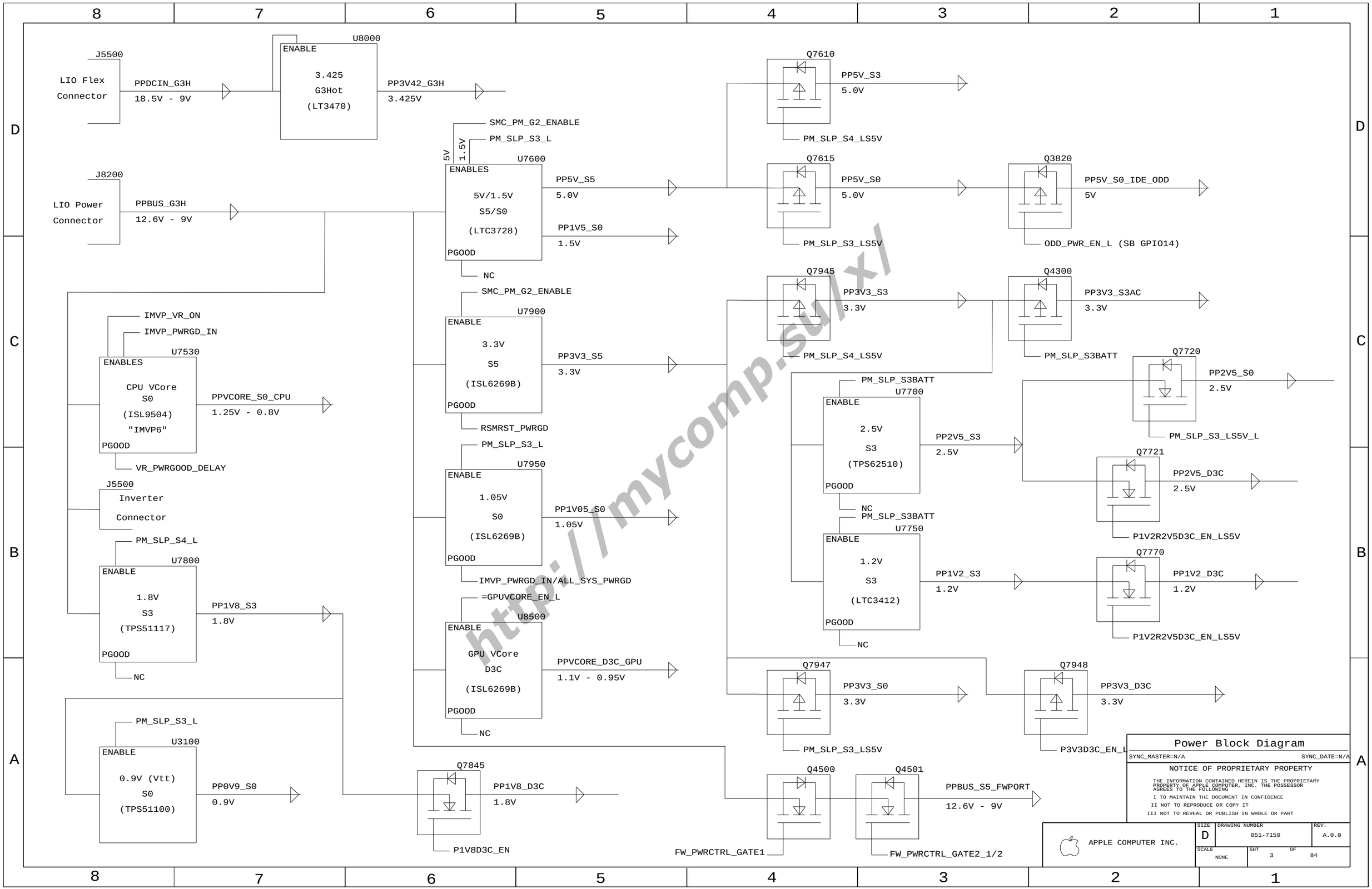
Apple Computer Inc.

TITLE
SCHEM,MLB,M59

DRAWING NUMBER 051-7150
REV. A.0.0

SHT 1 OF 84





2.16Ghz BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7849	PCBA,2.16GHZ,128VRAM,M59,MBP15	EEE_WTE,M59_COMMON,CPU_2_16GHZ,VRAM_SAM128

2.33Ghz BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7851	PCBA,2.33GHZ,256VRAM,M59,MBP15	EEE_WTG,M59_COMMON,CPU_2_33GHZ,VRAM_SAM256

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WTE]	CRITICAL	EEE_WTE
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WTG]	CRITICAL	EEE_WTG

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M59_COMMON	ALTERNATE,COMMON,M59_COMMON1,M59_COMMON2,M59_COMMON3
M59_COMMON1	BOOTROM_FINAL,ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL,D3CPGOOD_3V3
M59_COMMON2	ITP,KBDLED_HAS,LPCPLUS,LVDS_PD,MEMVREF_S3
M59_COMMON3	MEMVTT_EN_PU,RTUSB_ESD,SMC_PRGRM,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
VRAM_INF128	GPU_MEM_NOT_SAM,VRAM_128_INFINEON
VRAM_SAM128	VRAM_128_SAMSUNG
VRAM_INF256	GPU_MEM_256M,GPU_MEM_NOT_SAM,VRAM_256_INFINEON
VRAM_SAM256	GPU_MEM_256M,VRAM_256_SAMSUNG
M59_TPM	TPM

extra TPM options:
SMC_TPM_GPIO2
SMC_TPM_GPIO1
SMC_TPM_PP

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON
337S3391	1	IC,MDC,B2,PRQ,2.16G,34W,667M,4M,479BGA	U0700	CRITICAL	CPU_2_16GHZ
337S3393	1	IC,MDC,B2,PRQ,2.33G,34W,667M,4M,479BGA	U0700	CRITICAL	CPU_2_33GHZ
341S1922	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M59	U6301	CRITICAL	BOOTROM_DEVEL
341S1923	1	IC,EFI,BOOTROM FINAL (LOCKED),M59	U6301	CRITICAL	BOOTROM_FINAL
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1929	1	IC,PRGRM,SMC (NEW),M59	U5800	CRITICAL	SMC_PRGRM
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0368	1	IC,ATI,M56L-LLP,GRPHXCRTL,LF 880BGA	U8400	CRITICAL	
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,QFN48	U7530	CRITICAL	
359S0109	1	LOW POWER CLOCK SYNTHESIZER, 68PIN	U3301	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060		ALL	330uF,2V,9MOHM,D2
128S0095	128S0060		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	150uF,6.3V,25MOHM,C2
376S0448	376S0445		ALL	Si7806ADN for FDM6296
353S1465	353S1461		ALL	Screened ISL6262 for ISL9504
152S0287	152S0435		ALL	Alternates for Coilcraft MSS1132
128S0093	128S0092		ALL	33uF,16V,D2

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	4	84

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	59C7
TRUE		IMVP6_COMP	59B7
TRUE		P5VS5_RUNSS	60C5 64A6
TRUE		P1V5S0_RUNSS	5B7 60C4 64C6
TRUE		P1V2S3_RT	61B6
TRUE		P1V2S3_RUNSS	41C4 61B7
TRUE		P3V3S5_COMP	5B7 63C6
TRUE		P3V3S5_FSET	5B7 63D6
TRUE		P1V05S0_COMP	5C7 63A7
TRUE		P1V05S0_FSET	5B7 63B7
TRUE		P3V42G3H_FB	64C3
TRUE		GPUVCORE_COMP	68C7
TRUE		GPUVCORE_FSET	68C7
TRUE		GPUBBP_ADJ	68B7
TRUE		GPUBBN_FB	68A3
TRUE		GPUVCORE_FB	68C7
TRUE		GPUVCORE_FB_RC	68C3
TRUE		GPUVCORE_ISEN	68C5
TRUE		GPUVCORE_LG	68C5
TRUE		GPUVCORE_PHASE	68C5
TRUE		GPUVCORE_UG	68D5
TRUE		IMVP6_COMP_RC	59B8
TRUE		IMVP6_DFB	59B6
TRUE		IMVP6_FB	59B7
TRUE		IMVP6_OCSET	59C6
TRUE		IMVP6_VDIFF	59C7
TRUE		IMVP6_VDIFF_RC	59B8
TRUE		P1V05S0_BOOT	63B5
TRUE		P1V05S0_BOOT_R	63B5
TRUE		P1V05S0_COMP	5D7 63A7
TRUE		P1V05S0_COMP_R	63A7
TRUE		P1V05S0_FB	63A7
TRUE		P1V05S0_FB_RC	63A3
TRUE		P1V05S0_FSET	5D7 63B7
TRUE		P1V05S0_ISEN	63A5
TRUE		P1V05S0_LG	63A5
TRUE		P1V05S0_PHASE	63B5
TRUE		P1V05S0_UG	63B5
TRUE		P1V5S0_RUNSS	5D7 60C4 64C6
TRUE		P3V3S5_BOOT	63D4
TRUE		P3V3S5_BOOT_R	63D4
TRUE		P3V3S5_COMP	5D7 63C6
TRUE		P3V3S5_COMP_R	63C6
TRUE		P3V3S5_FB	63C6
TRUE		P3V3S5_FB_RC	63C2
TRUE		P3V3S5_FSET	5D7 63D6
TRUE		P3V3S5_ISEN	63C4
TRUE		P3V3S5_LG	63C4
TRUE		P3V3S5_UG	63D4
TRUE		CK410_XTAL_IN	33C6

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 84D6
TRUE		FSB_ADS_L	7D6 12C4 84D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 84C6
TRUE		FSB_BNR_L	7D6 12C4 84D6
TRUE		FSB_BREQ0_L	7D6 12C4 84D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 84D6
TRUE		FSB_DBSY_L	7D6 12B4 84D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE		FSB_DRDY_L	7D6 12B4 84D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE		FSB_HIT_L	7D6 12B4 84D6
TRUE		FSB_HITM_L	7D6 12B4 84D6
TRUE		FSB_LOCK_L	7D6 12B4 84D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 84D6

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	56C7 65A1
TRUE	FAN_LT_PWM	56B6
TRUE	FAN_LT_TACH	56B6
TRUE	FAN_RT_PWM	56B3
TRUE	FAN_RT_TACH	56B3

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	51C4 65D3
TRUE	=PP5V_S0_LPCPLUS	51C4 65A1
TRUE	LPC_AD<0>	21D4 49D7 51C4 58C6
TRUE	LPC_AD<1>	21D4 49D7 51C4 58C6
TRUE	LPC_FRAME_L	21C5 49C7 51C4 58C6
TRUE	PM_CLKRUN_L	23C8 49C5 51C4 58C6
TRUE	BOOT_LPC_SPI_L	22B3 49C7 51B4
TRUE	SMC_TMS	49B5 50B2 51B4
TRUE	DEBUG_RST_L	26B1 51B4
TRUE	SMC_TRST_L	49C1 51B4
TRUE	SMC_TDO	49B5 50B2 51B4
TRUE	SMC_MD1	49C1 51B4
TRUE	SMC_TX_L	46B5 49C7 50B2 50B3 51B4
TRUE	FWH_INIT_L	21C4 50D3 51C5
TRUE	PCI_CLK_PORT80_LPC	34D6 51C5
TRUE	LPC_AD<2>	21D4 49C7 51C5 58C6
TRUE	LPC_AD<3>	21D4 49C7 51C5 58C6
TRUE	INT_SERIRQ	23C8 49C7 51C5 58C6
TRUE	PM_SUS_STAT_L	23C5 49C5 50A2 51B5 58C6
TRUE	SMC_TDI	49B5 50B2 51B5
TRUE	SMC_TCK	49C5 50B2 51B5
TRUE	SMC_RST_L	49C3 50D6 51B5
TRUE	SMC_NMI	49C1 51B5
TRUE	SMC_RX_L	46B5 49C7 50B2 50B3 51B5
TRUE	SV_SET_UP	23B6 23C3 51B5

Left ALS Connector

FUNC_TEST

TRUE	=PP3V3_S3_LTALS	65C3 78C5
TRUE	ALS_GAIN	6D5 49B5 78C6
TRUE	LTALS_OUT	55C7 78C6
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

TRUE	HSTHMSNS_DX_P	52C5
TRUE	HSTHMSNS_DX_N	52C5
TRUE	RSFSTHMSNS_D_P	52D5
TRUE	RSFSTHMSNS_D_N	52C5

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	53A4 63A2 65D8
TRUE	PM_SYSRST_L	23C5 26C5 49B7
TRUE	SMC_ONOFF_L	49C5 50B2 50C6 78C2

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	49B7 53A8
TRUE	=PP5V_S0_ISENSECAL	53A8 65A1
TRUE	=PP1V8_S3_REG	62C1 65B8
TRUE	=PP1V5_S0_REG	60C1 65C8
TRUE	PPVCORE_S0_GPU	
TRUE	PPVCORE_S0_CPU	65D1
TRUE	GND	

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	49C5 50B2 66B5
TRUE	=SMBUS_BATT_SCL	27C1 66B5
TRUE	=SMBUS_BATT_SDA	27C1 66B5
TRUE	GND_BATT	66B5

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	47D6 65C6
TRUE	=PPDCIN_G3H_LIO	47C6 65A8
TRUE	=PP5V_S5_LIO	47C6 65B1
TRUE	=PP3V42_G3H_LIO	47D6 65D3
TRUE	PP5V_S0_AUDIO_PWR	47D4
TRUE	PP5V_S0_AUDIO	47C4
TRUE	GND_AUDIO_PWR	47A4
TRUE	GND_AUDIO	47A4
TRUE	ACZ_SDATAIN<0>	21C7 47B6 84B4
TRUE	ACZ_SDATAOUT	21C7 47B6 84B4
TRUE	ACZ_BITCLK	21C7 47B6 84B4
TRUE	ACZ_RST_L	21C7 47B3 84B4
TRUE	EXCARD_OC_L	6C3 47C6 50B3
TRUE	LTUSB_OC_L	6D3 47C6
TRUE	LIO_BATT_ISENSE	47C6 53C3
TRUE	SMC_SYS_ISET	47C6 49B5
TRUE	SMC_BATT_ISET	47B6 49B5
TRUE	SMC_BATT_CHG_EN	47C6 49D7 50A2
TRUE	SMC_BC_ACOK	47B6 49C5 50A2
TRUE	SMC_ADAPTER_EN	43B7 47C6 49D5 50A2
TRUE	LIO_P3V3S0_EN_L	47B6 64C6
TRUE	LIO_DCIN_ISENSE	47B6 53C5
TRUE	LIO_P3V3S3_EN	47B6 64A6
TRUE	SMC_BATT_TRICKLE_EN_L	47B6 49D7 50A2
TRUE	SYS_ONEWIRE	47C6 49B7 50B2
TRUE	MINI_CLKREQ_L	34A3 47C6
TRUE	SMC_EXCARD_CP	47B6 49B7 50A2
TRUE	EXCARD_CLKREQ_L	34A3 47C6
TRUE	SMC_EXCARD_PWR_EN	47B6 49B7
TRUE	LIO_PLT_RESET_L	26C1 47C6
TRUE	ACZ_SYNC	21C7 47B6 84B4
TRUE	=USB2_LT_N	6D3 47C3
TRUE	=USB2_LT_P	6D3 47C3
TRUE	=USB2_EXCARD_N	6C3 47C3
TRUE	=USB2_EXCARD_P	6C3 47C3
TRUE	=PCIE_EXCARD_R2D_N	47B3 48C6
TRUE	=PCIE_EXCARD_R2D_P	47B3 48C6
TRUE	=PCIE_EXCARD_D2R_N	47B3 48B6
TRUE	=PCIE_EXCARD_D2R_P	47B3 48C6
TRUE	PCIE_CLK100M_EXCARD_P	34C3 47B3
TRUE	PCIE_CLK100M_EXCARD_N	34B3 47B3
TRUE	=PCIE_MINI_R2D_N	47B3 48C6
TRUE	=PCIE_MINI_R2D_P	47B3 48C6
TRUE	=PCIE_MINI_D2R_N	47C3 48C6
TRUE	=PCIE_MINI_D2R_P	47C3 48C6
TRUE	PCIE_CLK100M_MINI_P	34D4 47C3
TRUE	PCIE_CLK100M_MINI_N	34D4 47C3
TRUE	=SMBUS_LIO_SMC_SCL	27D1 47C3
TRUE	=SMBUS_LIO_SMC_SDA	27D1 47C3
TRUE	=SMBUS_LIO_SB_SCL	27B6 47C3
TRUE	=SMBUS_LIO_SB_SDA	27B6 47C3
TRUE	PCIE_WAKE_L	23C8 39C6 47C3

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	65C3 66C4
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14B4 22D2
TRUE	DMI_N2S_N<1..0>	14B4 22D2
TRUE	SB_CLK100M_SATA_P	21B6 34C3
TRUE	SB_CLK100M_SATA_N	21B6 34C3

Camera Connector

FUNC_TEST

TRUE	=PP5V_S3_CAMERA	45C3 65B1
	=USB2_CAMERA_N	6C3 45C3
	=USB2_CAMERA_P	6D3 45B3

Inverter Connector

FUNC_TEST

TRUE	GND_CHASSIS_INVERTER	6A8
TRUE	PPBUS_S0_INVERTER	76B5
TRUE	GND_INVERTER	76A5
TRUE	INVERTER_PWM	76A5
TRUE	PP5V_INVERTER_SW	76B5

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3C_RTC	26D6
TRUE	GND	

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 5 OF 84	

NC_CPU_A32_L — TP_CPU_A32_L (7C8)
NC_CPU_A33_L — TP_CPU_A33_L (7B8)
NC_CPU_A34_L — TP_CPU_A34_L (7B8)
NC_CPU_A35_L — TP_CPU_A35_L (7B8)
NC_CPU_A36_L — TP_CPU_A36_L (7B8)
NC_CPU_A37_L — TP_CPU_A37_L (7B8)
NC_CPU_A38_L — TP_CPU_A38_L (7B8)
NC_CPU_A39_L — TP_CPU_A39_L (7B8)
NC_CPU_APM0_L — TP_CPU_APM0_L (7B8)
NC_CPU_APM1_L — TP_CPU_APM1_L (7B8)
NC_CPU_EXTBREF — TP_CPU_EXTBREF (7B6)
NC_CPU_HFPLL — TP_CPU_HFPLL (7B8)
NC_CPU_SPARE0 — TP_CPU_SPARE0 (7B6)
NC_CPU_SPARE1 — TP_CPU_SPARE1 (7B6)
NC_CPU_SPARE2 — TP_CPU_SPARE2 (7B6)
NC_CPU_SPARE4 — TP_CPU_SPARE4 (7B6)

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28C3)
NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29C3)
TP_NB_CFG<4..3> — NB_CFG<4..3> (14C6)
TP_NB_CFG<6> — NB_CFG<6> (14C6)
TP_NB_CFG<8> — NB_CFG<8> (14C6)
TP_NB_CFG<11..10> — NB_CFG<11..10> (14C6)
TP_NB_CFG<15..14> — NB_CFG<15..14> (14C6)
TP_NB_CFG<17> — NB_CFG<17> (14C6)

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14C6)

TP_SB_SUS_CLK — SUS_CLK_SB (23C3)

NC_SB_XOR_T5 — TP_SB_XOR_T5 (21C6)
NC_SB_XOR_U5 — TP_SB_XOR_U5 (21C6)
NC_SB_XOR_V3 — TP_SB_XOR_V3 (21C6)
NC_SB_XOR_V4 — TP_SB_XOR_V4 (21C6)
NC_SB_XOR_W3 — TP_SB_XOR_W3 (21C6)

FireWire Aliases

42C4 =PP3V3_FWPHY_REG — PP3V3_FWPHY (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE)
- =PP3V3_FWPHY (38D7 44B8)
- =PP3V3_FWPHY_CORE (42C4)
- =PP3V3_FWLATEVG (44A8)
- =PP3V3_FWLATEVG_ACTIVE (43A7)

42C1 =PP1V95_FWPHY_CORE_LDO — PP1V95_FWPHY (VOLTAGE=1.95V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE)
- =PP1V95_FWPHY (38D5)
- =PP1V8_FWPHY_OSC (38B2)

49D7 6D4 SMC_RSTGATE_L (MAKE_BASE=TRUE) — =SMC_FWRSTGATE_L (37A8)
37C6 22A7 PCI_AD<19> (MAKE_BASE=TRUE) — =FW_PCI_IDSEL (37B7)
22B6 PCI_GNT3_L (MAKE_BASE=TRUE) — =FW_PCI_GNT_L (37D3)
26D2 22B6 PCI_REQ3_L (MAKE_BASE=TRUE) — =FW_PCI_REQ_L (37D3)

Chassis GNDs

GND_CHASSIS_RTUSB (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
- =GND_CHASSIS_RTUSB (46B2)
- =GND_CHASSIS_FW_PORT2L (44A1)
- =GND_CHASSIS_FW_EMI_R (44A3)

GND_CHASSIS_DVI_TOP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
- C0600 0.01UF 10% 50V X7R 402 (1, 2)
- =GND_CHASSIS_DVI2 (77A5)
- =GND_CHASSIS_DVI4 (77A3)

GND_CHASSIS_DVI_BOT (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
- R0601 0 5% 1/16W MF-LF 402 (1, 2)
- =GND_CHASSIS_DVI1 (77B5)
- =GND_CHASSIS_DVI3 (77A2)
- =GND_CHASSIS_DVI5 (77A2)

GND_CHASSIS_ENET (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
- =GND_CHASSIS_ENET (40B2)
- =GND_CHASSIS_FW_PORT1 (44C1)
- =GND_CHASSIS_FW_PORT2U (44A1)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602 HOLE-VIA-P5RP25 (1)
C0602 0.01UF 10% 50V X7R 402 (1, 2)
GND_CHASSIS_LVDS (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
- =GND_CHASSIS_LCD1 (76D2)
- =GND_CHASSIS_LCD2 (76D3)
- =GND_CHASSIS_LCD3 (76C3)
- =GND_CHASSIS_LCD4 (76B2)

SH0600 OG-503040 SHLD-SM-LF (1, 2, 3)
5A4 GND_CHASSIS_INVERTER (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
- =GND_CHASSIS_INVERTER (76A6)
- =GND_CHASSIS_CAMERA (45B5 45C5)

TP_SMC_RSTGATE_L (MAKE_BASE=TRUE) — SMC_RSTGATE_L (6B7 49D7)
78C6 49B5 5B2 ALS_GAIN (MAKE_BASE=TRUE) — =RTALS_GAIN (55C4)

NC_ENET_CTRL12 (MAKE_BASE=TRUE, NO_TEST=TRUE) — ENET_CTRL12 (39C8)
NC_ENET_CTRL25 (MAKE_BASE=TRUE, NO_TEST=TRUE) — ENET_CTRL25 (39C8)

Ethernet Power Management Support

ENET_LOWPWR_EN
R0600 0 5% 1/16W MF-LF 402 (1, 2)
22D8 22C4 SB_GPIO30 (IN) — ENET_LOWPWR_EN (39B8) (OUT)

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

Inverter PWM Reset Alias

26C1 MS9_INVERTER_PLT_RST_L — =INVERTER_PWM_PLT_RST_L (76A8)

Thermal Module Holes

Add 2 blind vias per hole per side to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Bottom Left GPU TM Hole

RAM door (Torx) holes

ZT0630 HOLE-VIA-P5RP25 (0)
GND_CHASSIS_RAMDOOR_HOLE_0 (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
C0630 0.01UF 10% 50V X7R 402 (1, 2)

ZT0631 HOLE-VIA-P5RP25 (1)
GND_CHASSIS_RAMDOOR_HOLE_1 (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
C0631 0.01UF 10% 50V X7R 402 (1, 2)

Frame holes

ZT0615 HOLE-VIA-P5RP25 (1) GND_CHASSIS_RIGHT_FAN_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0614 HOLE-VIA-P5RP25 (1) GND_CHASSIS_RIGHT_FAN_NOTCH (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0613 HOLE-VIA-P5RP25 (1) GND_CHASSIS_DIMM_NOTCH (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0612 HOLE-VIA-P5RP25 (1) GND_CHASSIS_LIOFLEX_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0611 HOLE-VIA-P5RP25 (1) GND_CHASSIS_BATTCONN_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0610 HOLE-VIA-P5RP25 (1) GND_CHASSIS_LNDACARD_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)

C0610 0.01UF 10% 50V X7R 402 (1, 2)
C0611 0.01UF 10% 50V X7R 402 (1, 2)
C0612 0.01UF 10% 50V X7R 402 (1, 2)
C0613 0.01UF 10% 50V X7R 402 (1, 2)
C0614 0.01UF 10% 50V X7R 402 (1, 2)
C0615 0.01UF 10% 50V X7R 402 (1, 2)

USB Port "A" (Debug Port) = Right USB 2.0 Port

46B5 =USB2_RT_P — USB2_RT_P (MAKE_BASE=TRUE) — USB_A_P (22C2)
46B5 =USB2_RT_N — USB2_RT_N (MAKE_BASE=TRUE) — USB_A_N (22C2)
46C5 =RTUSB_OC_L — RTUSB_OC_L (MAKE_BASE=TRUE) — USB_A_OC_L (22C4 22D8)

USB Port "B" = Trackpad (Geyser)

78C3 =USB_TRACKPAD_P — USB_TRACKPAD_P (MAKE_BASE=TRUE) — USB_B_P (22C2)
78C3 =USB_TRACKPAD_N — USB_TRACKPAD_N (MAKE_BASE=TRUE) — USB_B_N (22C2)
UNUSED_USB_B_OC_L (MAKE_BASE=TRUE) — USB_B_OC_L (22C4 22D8)

USB Port "C" = Left USB 2.0 Port

47C3 5B1 =USB2_LT_P — USB2_LT_P (MAKE_BASE=TRUE) — USB_C_P (22C2)
47C3 5B1 =USB2_LT_N — USB2_LT_N (MAKE_BASE=TRUE) — USB_C_N (22C2)
47C6 5C1 LTUSB_OC_L (MAKE_BASE=TRUE) — USB_C_OC_L (22C4 22D8)

USB Port "D" = Camera

45B3 5A4 =USB2_CAMERA_P — USB2_CAMERA_P (MAKE_BASE=TRUE) — USB_D_P (22C2)
45C3 5A4 =USB2_CAMERA_N — USB2_CAMERA_N (MAKE_BASE=TRUE) — USB_D_N (22C2)
UNUSED_USB_D_OC_L (MAKE_BASE=TRUE) — USB_D_OC_L (22C4 22D8)

USB Port "E" = ExpressCard

47C3 5B1 =USB2_EXCARD_P — USB2_EXCARD_P (MAKE_BASE=TRUE) — USB_E_P (22C2)
47C3 5B1 =USB2_EXCARD_N — USB2_EXCARD_N (MAKE_BASE=TRUE) — USB_E_N (22C2)
50B3 47C6 5C1 EXCARD_OC_L (MAKE_BASE=TRUE) — USB_E_OC_L (22C4 22D8)

USB Port "F" = IR Receiver

78B4 =USB_IR_P — USB_IR_P (MAKE_BASE=TRUE) — USB_F_P (22C2)
78B4 =USB_IR_N — USB_IR_N (MAKE_BASE=TRUE) — USB_F_N (22C2)

USB Port "G" = Bluetooth (M13L)

78C2 =USB_BT_P — USB_BT_P (MAKE_BASE=TRUE) — USB_G_P (22C2)
78C2 =USB_BT_N — USB_BT_N (MAKE_BASE=TRUE) — USB_G_N (22C2)

USB Port "H" = Reserved

22C2 6C1 TP_USB_H_P (MAKE_BASE=TRUE) — TP_USB_H_P (6C2 22C2)
22C2 6C1 TP_USB_H_N (MAKE_BASE=TRUE) — TP_USB_H_N (6C2 22C2)

LVDS pulldown aliases

79B8 =LVDS_PD_U_CLK_N — LVDS_U_CLK_CONN_N (MAKE_BASE=TRUE) (76B2 76D7 79C1)
79B8 =LVDS_PD_U_CLK_P — LVDS_U_CLK_CONN_P (MAKE_BASE=TRUE) (76B2 76D7 79C1)
79C8 =LVDS_PD_U_DATA_P<0> — LVDS_U_DATA_CONN_P<0> (MAKE_BASE=TRUE) (76C2 76D7 79D1)
79C8 =LVDS_PD_U_DATA_N<0> — LVDS_U_DATA_CONN_N<0> (MAKE_BASE=TRUE) (76C2 76D7 79D1)
79B8 =LVDS_PD_U_DATA_P<1> — LVDS_U_DATA_CONN_P<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79B8 =LVDS_PD_U_DATA_N<1> — LVDS_U_DATA_CONN_N<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79B8 =LVDS_PD_U_DATA_P<2> — LVDS_U_DATA_CONN_P<2> (MAKE_BASE=TRUE) (76B2 76D7 79C1)
79B8 =LVDS_PD_U_DATA_N<2> — LVDS_U_DATA_CONN_N<2> (MAKE_BASE=TRUE) (76C2 76D7 79D1)
79C8 =LVDS_PD_L_CLK_N — LVDS_L_CLK_CONN_N (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79C8 =LVDS_PD_L_CLK_P — LVDS_L_CLK_CONN_P (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79D8 =LVDS_PD_L_DATA_P<0> — LVDS_L_DATA_CONN_P<0> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79D8 =LVDS_PD_L_DATA_N<0> — LVDS_L_DATA_CONN_N<0> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79D8 =LVDS_PD_L_DATA_P<1> — LVDS_L_DATA_CONN_P<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79C8 =LVDS_PD_L_DATA_N<1> — LVDS_L_DATA_CONN_N<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79C8 =LVDS_PD_L_DATA_P<2> — LVDS_L_DATA_CONN_P<2> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
79C8 =LVDS_PD_L_DATA_N<2> — LVDS_L_DATA_CONN_N<2> (MAKE_BASE=TRUE) (76C2 76D7 79C1)

Signal Aliases/Misc Comps

SYNC_MASTER=N/A — SYNC_DATE=N/A

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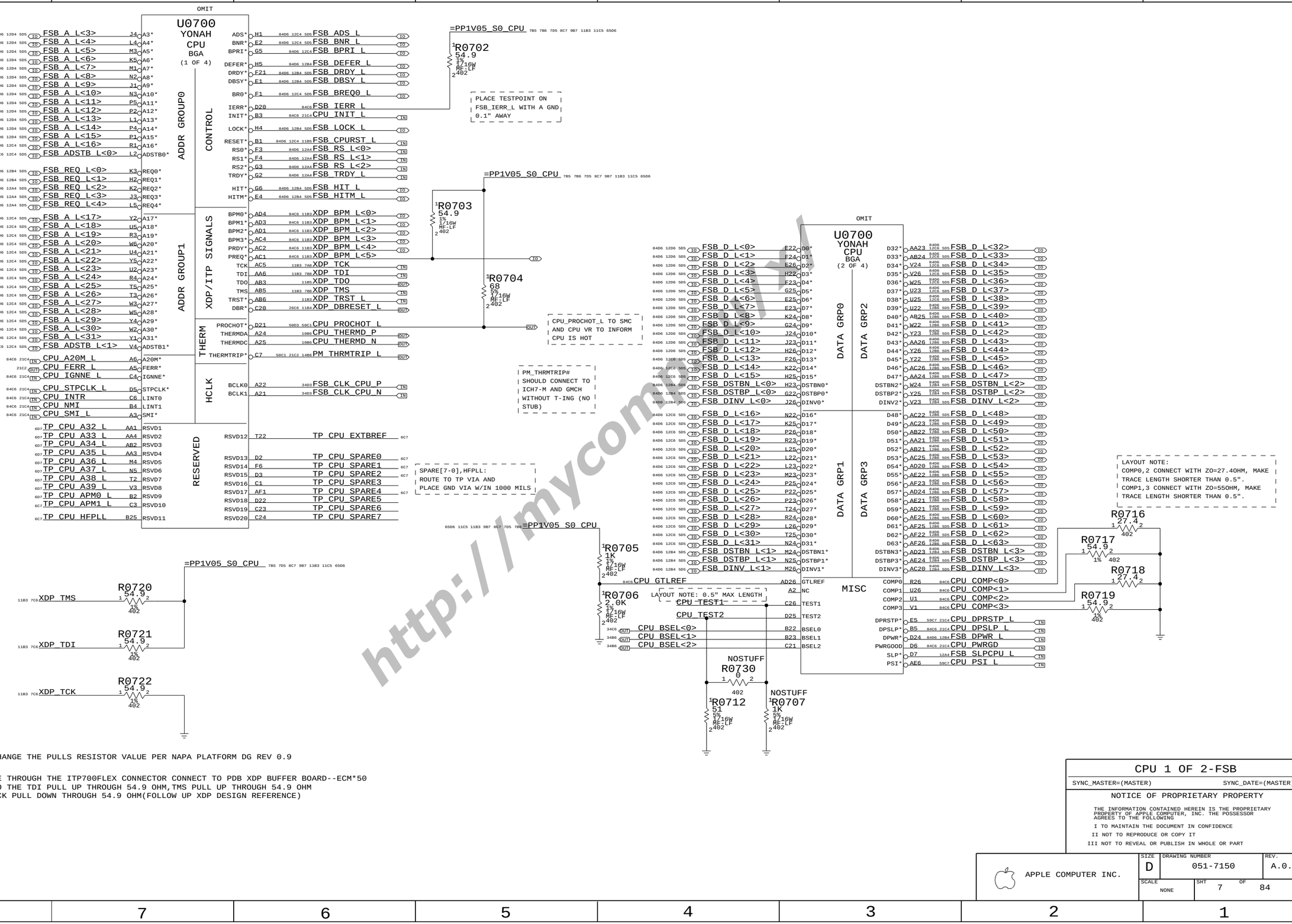
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 6 OF 84	


U0700
YONAH
CPU
BGA
(1 OF 4)
OMIT
ADDR GROUP0
CONTROL
XDP/ITP SIGNALS
ADDR GROUP1
THERM
HCLK
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
FSB_A_L<10>
FSB_A_L<11>
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FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
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FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_A32_L
TP_CPU_A33_L
TP_CPU_A34_L
TP_CPU_A35_L
TP_CPU_A36_L
TP_CPU_A37_L
TP_CPU_A38_L
TP_CPU_A39_L
TP_CPU_APM0_L
TP_CPU_APM1_L
TP_CPU_HFPLL
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
TP_CPU_EXTBREF
TP_CPU_SPARE0
TP_CPU_SPARE1
TP_CPU_SPARE2
TP_CPU_SPARE3
TP_CPU_SPARE4
TP_CPU_SPARE5
TP_CPU_SPARE6
TP_CPU_SPARE7
=PP1V05_S0_CPU
R0702 54.9 1% 1/16W MF-LF 402
R0703 54.9 1% 1/16W MF-LF 402
R0704 68 5% 1/16W MF-LF 402
R0705 1K 1% 1/16W MF-LF 402
R0706 2.0K 1% 1/16W MF-LF 402
R0707 1K 5% 1/16W MF-LF 402
R0712 51 5% 1/16W MF-LF 402
R0720 54.9 1% 402
R0721 54.9 1% 402
R0722 54.9 1% 402
R0730 0 402
R0716 27.4 1% 402
R0717 54.9 1% 402
R0718 27.4 1% 402
R0719 54.9 1% 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY
CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT
PM_THRMTRIP# SHOULD CONNECT TO ICH7-M AND GMCH WITHOUT T-ING (NO STUB)
SPARE[7-0],HFPLL: ROUTE TO TP VIA AND PLACE GND VIA W/IN 1000 MILS
LAYOUT NOTE: 0.5" MAX LENGTH
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>
NOSTUFF
CPU_GTLREF
U0700
YONAH
CPU
BGA
(2 OF 4)
OMIT
DATA GRP0
DATA GRP2
DATA GRP1
DATA GRP3
MISC
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
FSB_D_L<6>
FSB_D_L<7>
FSB_D_L<8>
FSB_D_L<9>
FSB_D_L<10>
FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTBN_L<0>
FSB_DSTBP_L<0>
FSB_DINV_L<0>
FSB_D_L<16>
FSB_D_L<17>
FSB_D_L<18>
FSB_D_L<19>
FSB_D_L<20>
FSB_D_L<21>
FSB_D_L<22>
FSB_D_L<23>
FSB_D_L<24>
FSB_D_L<25>
FSB_D_L<26>
FSB_D_L<27>
FSB_D_L<28>
FSB_D_L<29>
FSB_D_L<30>
FSB_D_L<31>
FSB_DSTBN_L<1>
FSB_DSTBP_L<1>
FSB_DINV_L<1>
FSB_D_L<32>
FSB_D_L<33>
FSB_D_L<34>
FSB_D_L<35>
FSB_D_L<36>
FSB_D_L<37>
FSB_D_L<38>
FSB_D_L<39>
FSB_D_L<40>
FSB_D_L<41>
FSB_D_L<42>
FSB_D_L<43>
FSB_D_L<44>
FSB_D_L<45>
FSB_D_L<46>
FSB_D_L<47>
FSB_DSTBN_L<2>
FSB_DSTBP_L<2>
FSB_DINV_L<2>
FSB_D_L<48>
FSB_D_L<49>
FSB_D_L<50>
FSB_D_L<51>
FSB_D_L<52>
FSB_D_L<53>
FSB_D_L<54>
FSB_D_L<55>
FSB_D_L<56>
FSB_D_L<57>
FSB_D_L<58>
FSB_D_L<59>
FSB_D_L<60>
FSB_D_L<61>
FSB_D_L<62>
FSB_D_L<63>
FSB_DSTBN_L<3>
FSB_DSTBP_L<3>
FSB_DINV_L<3>
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGD
FSB_SLPCPU_L
CPU_PSI_L
LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)
CPU 1 OF 2-FSB
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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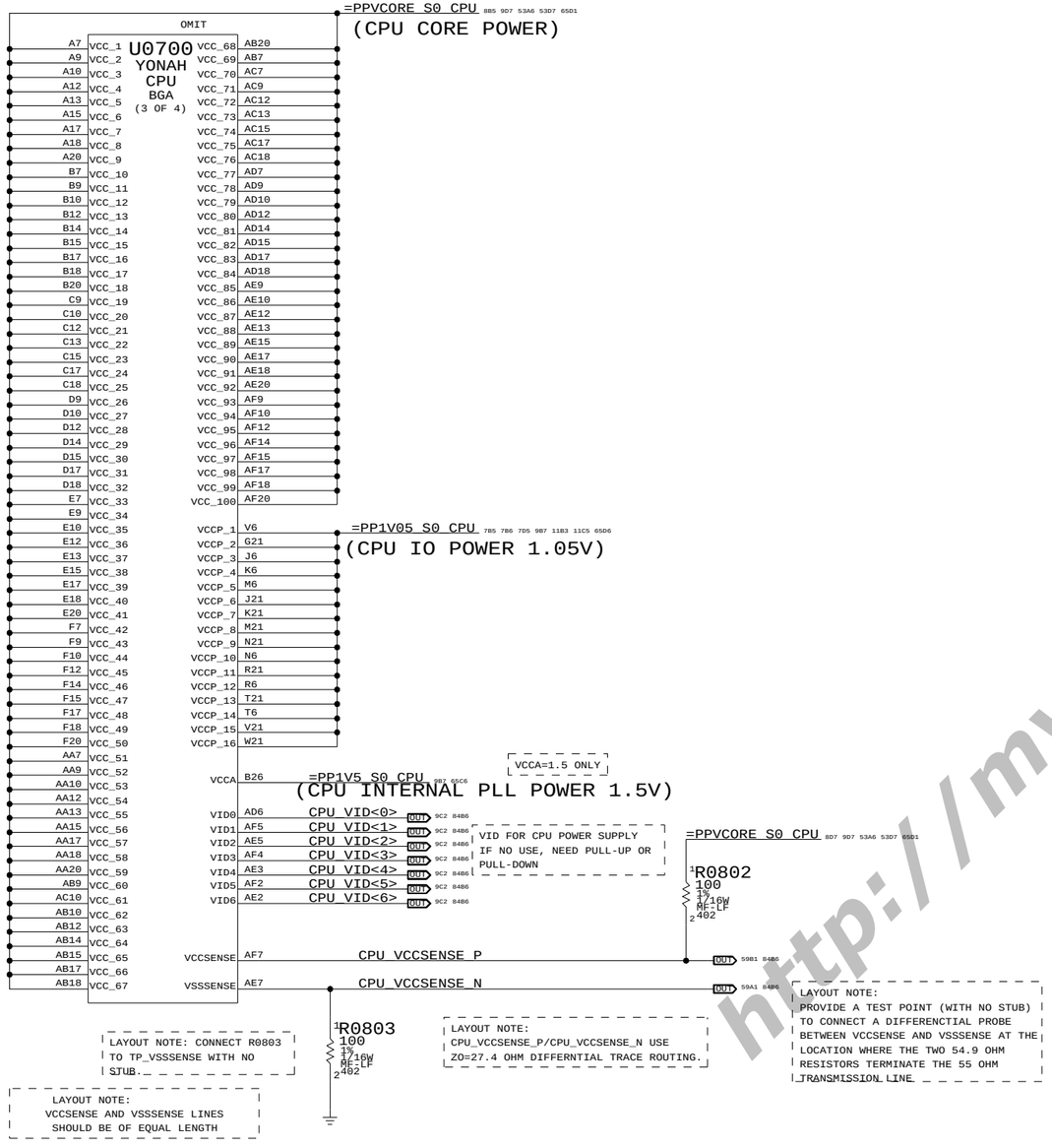
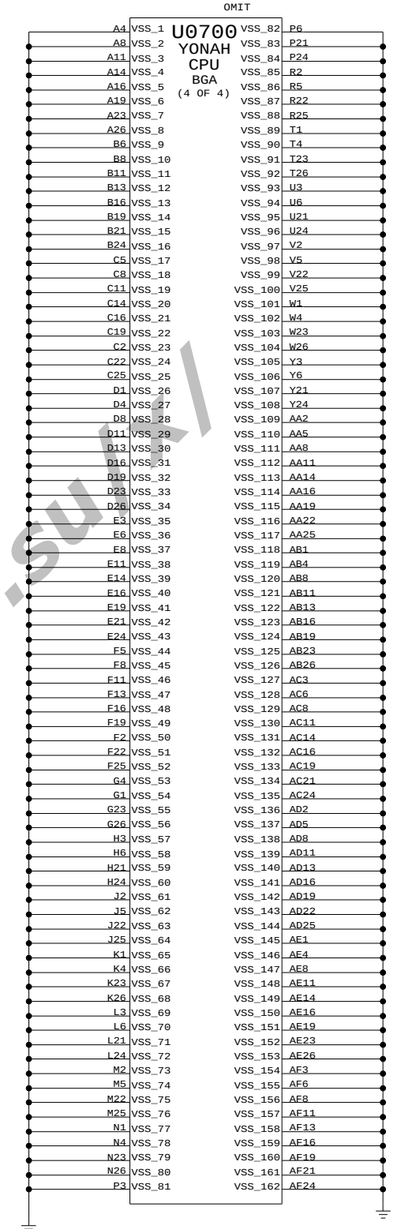
SIZE D
DRAWING NUMBER 051-7150
REV. A.0.0
SCALE NONE
SHT 7 OF 84





CPU 2 OF 2-PWR/GND

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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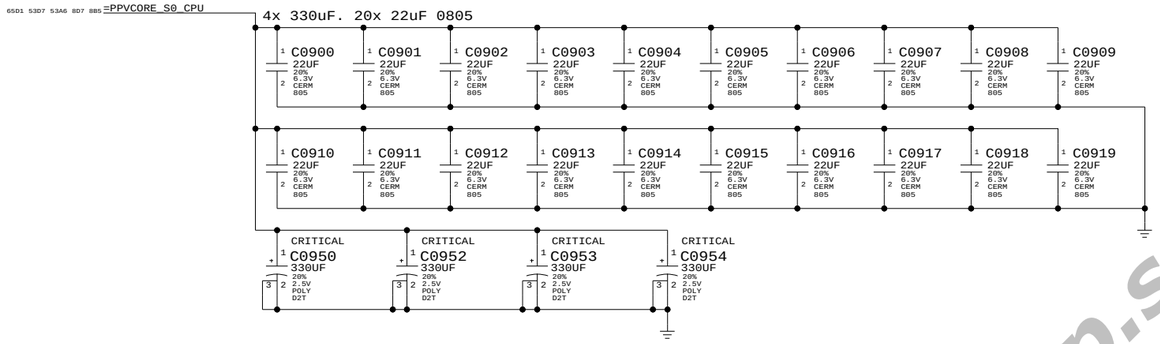
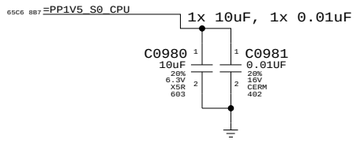
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 8 OF 84	

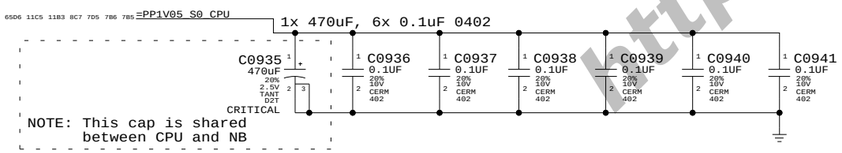
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

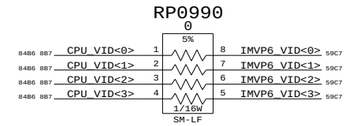


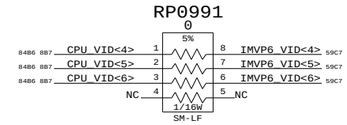
VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production





CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 9 OF 84	

CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

65B3 =PP3V3_S0_THRM_SNR

C1002 0.1UF 10% 16V X5R 402

R1006 10K 5% 1/16W MF-LF 402

R1005 10K 5% 1/16W MF-LF 402

R1001 499 1% 1/16W MF-LF 402

R1002 499 1% 1/16W MF-LF 402

C1001 0.001UF 10% 50V CERM 402

OUT 7C6 CPU_THERMD_P

IN 7C6 CPU_THERMD_N

(TO CPU INTERNAL THERMAL DIODE)
(TC0D)

THRM_CPU_DX_P

THRM_CPU_DX_N

U1001
TMP401
MSOP
CRITICAL

VDD
D+
D-
GND
ALERT*/THM2*
THM*
SCLK
SDATA

THRM_ALERT_L

THRM_ALERT

27D1 SMB_THRM_CLK TO

27D1 SMB_THRM_DATA TO

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

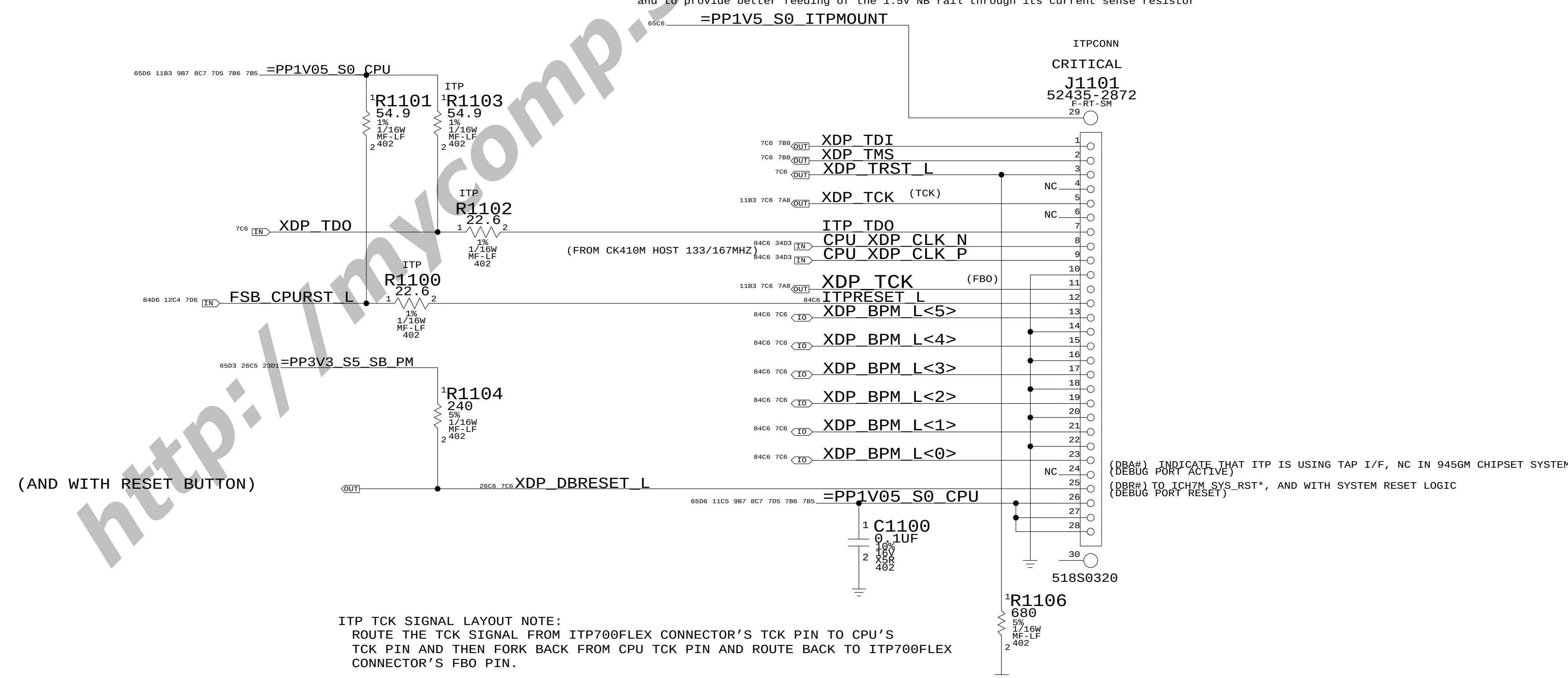
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	10	84

CPU ITP700FLEX DEBUG SUPPORT

Note: This connection to 1V5_S0 is to steal this mounting pad to add to the 1.5V S0 shape and to provide better feeding of the 1.5V NB rail through its current sense resistor

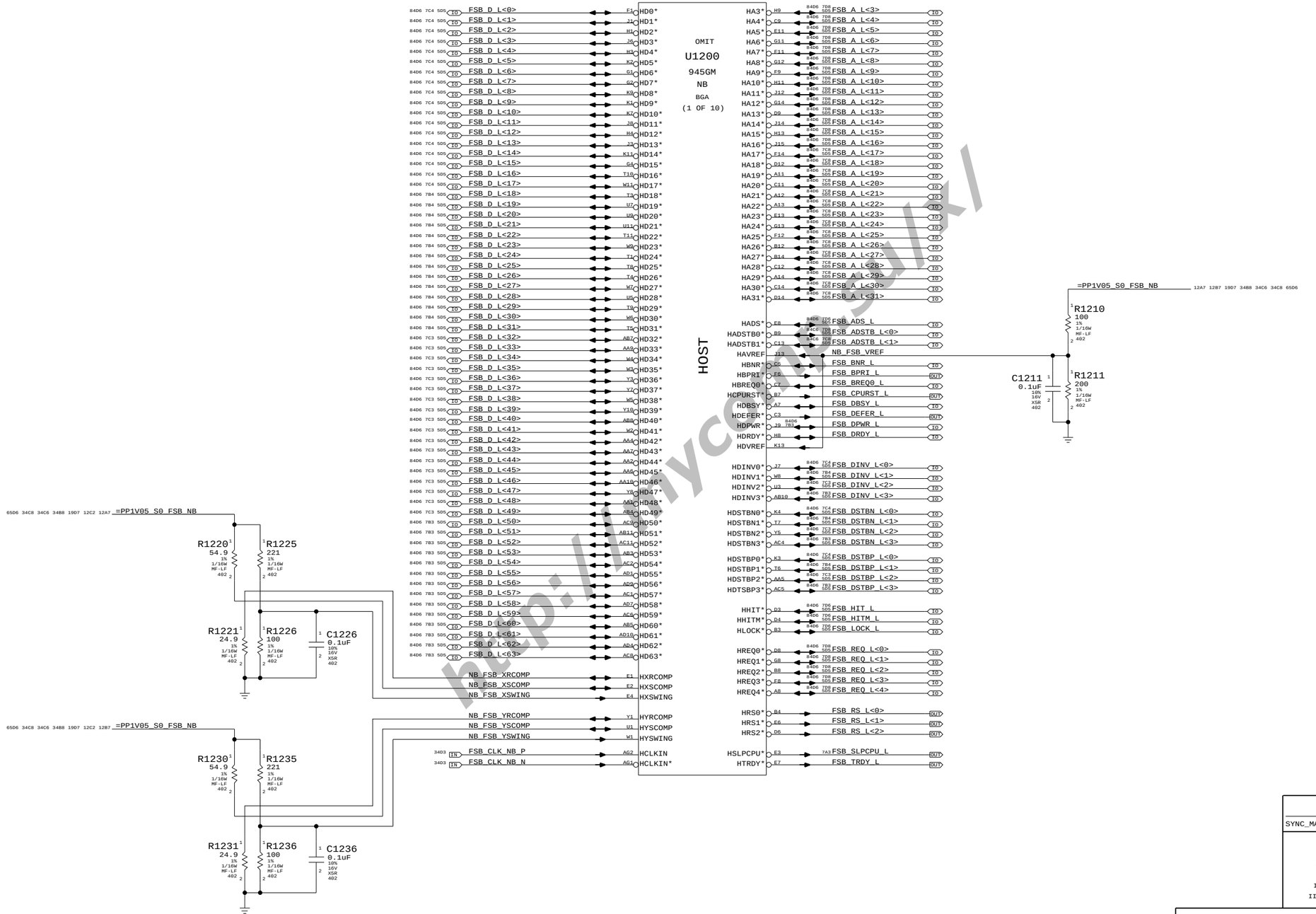


ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150	REV. A.0.0
	SCALE NONE	SHT 11	OF 84



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 12 OF 84	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

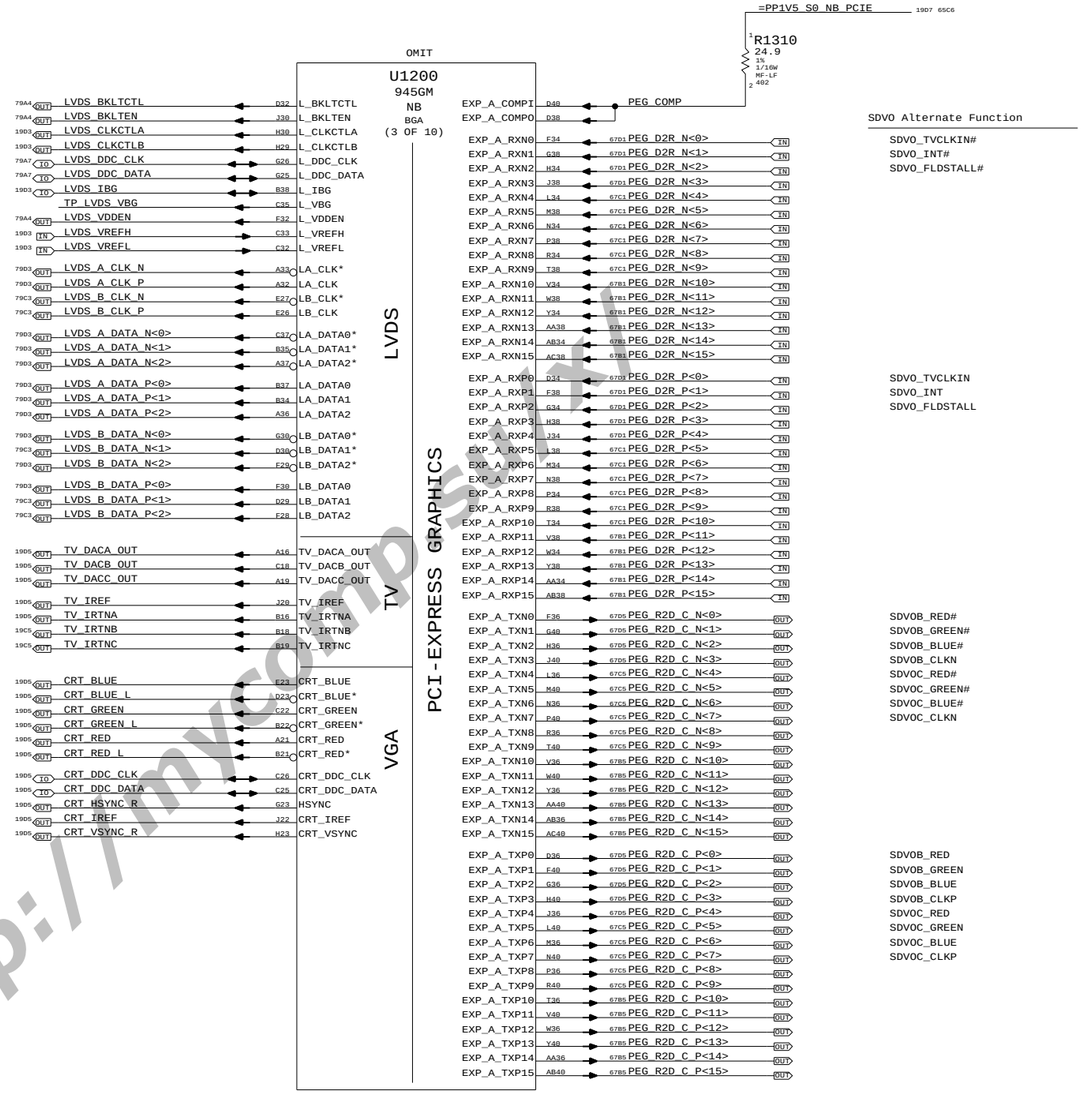
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

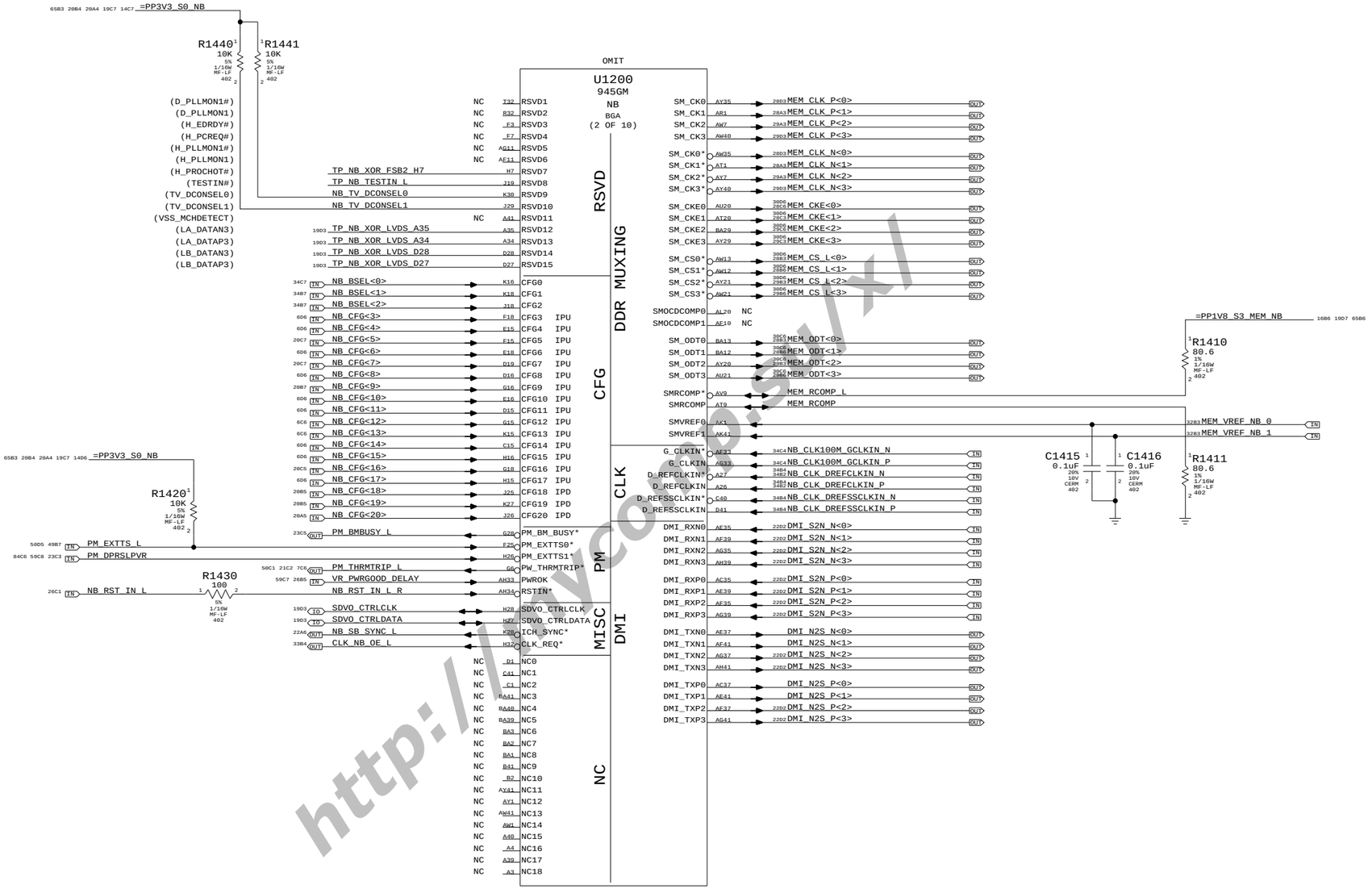


NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 13 OF 84	



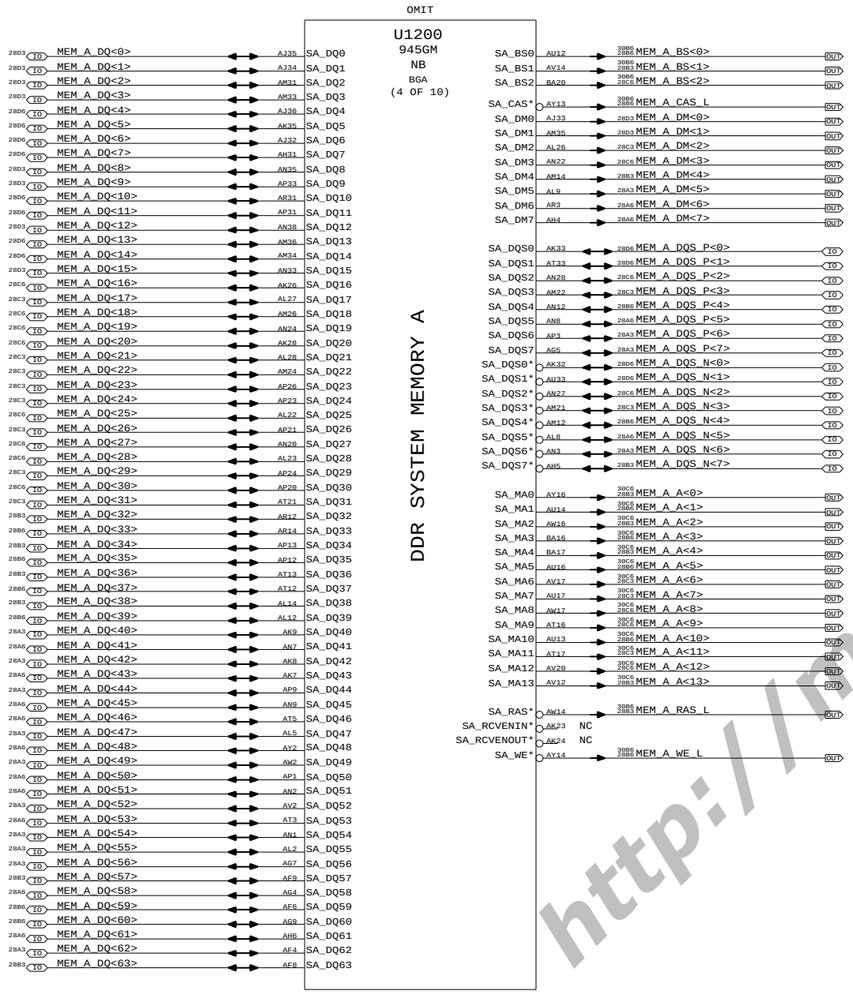
NB Misc Interfaces

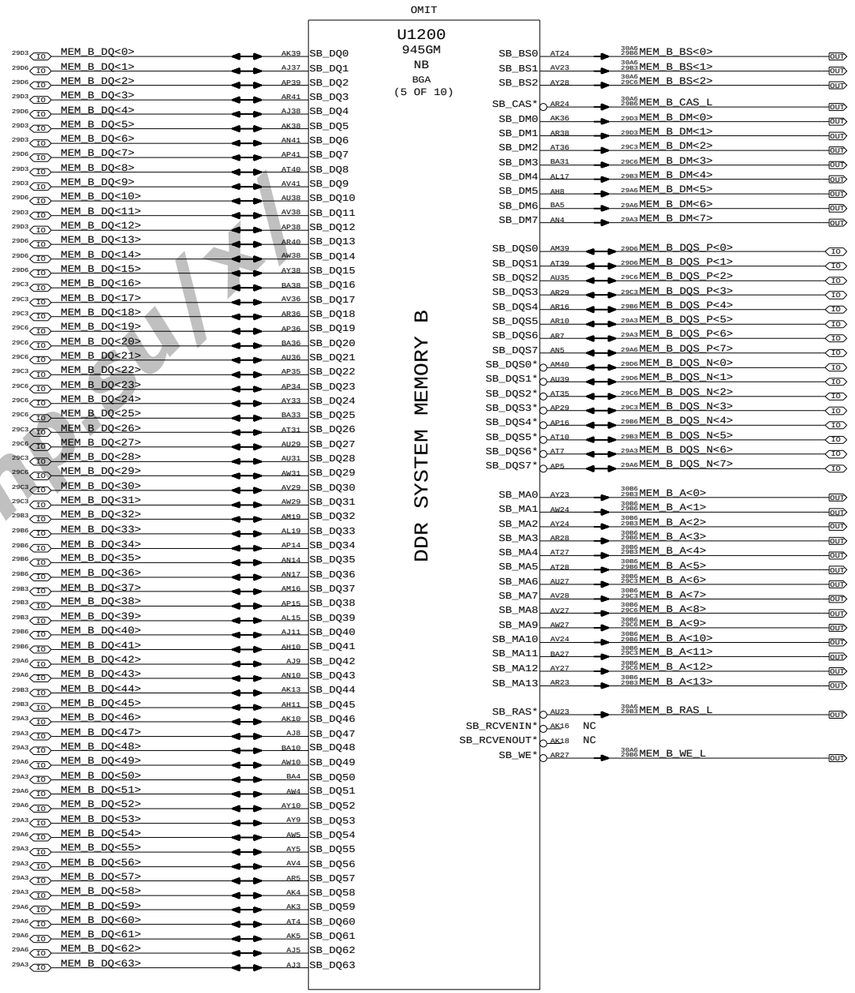
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	14	84



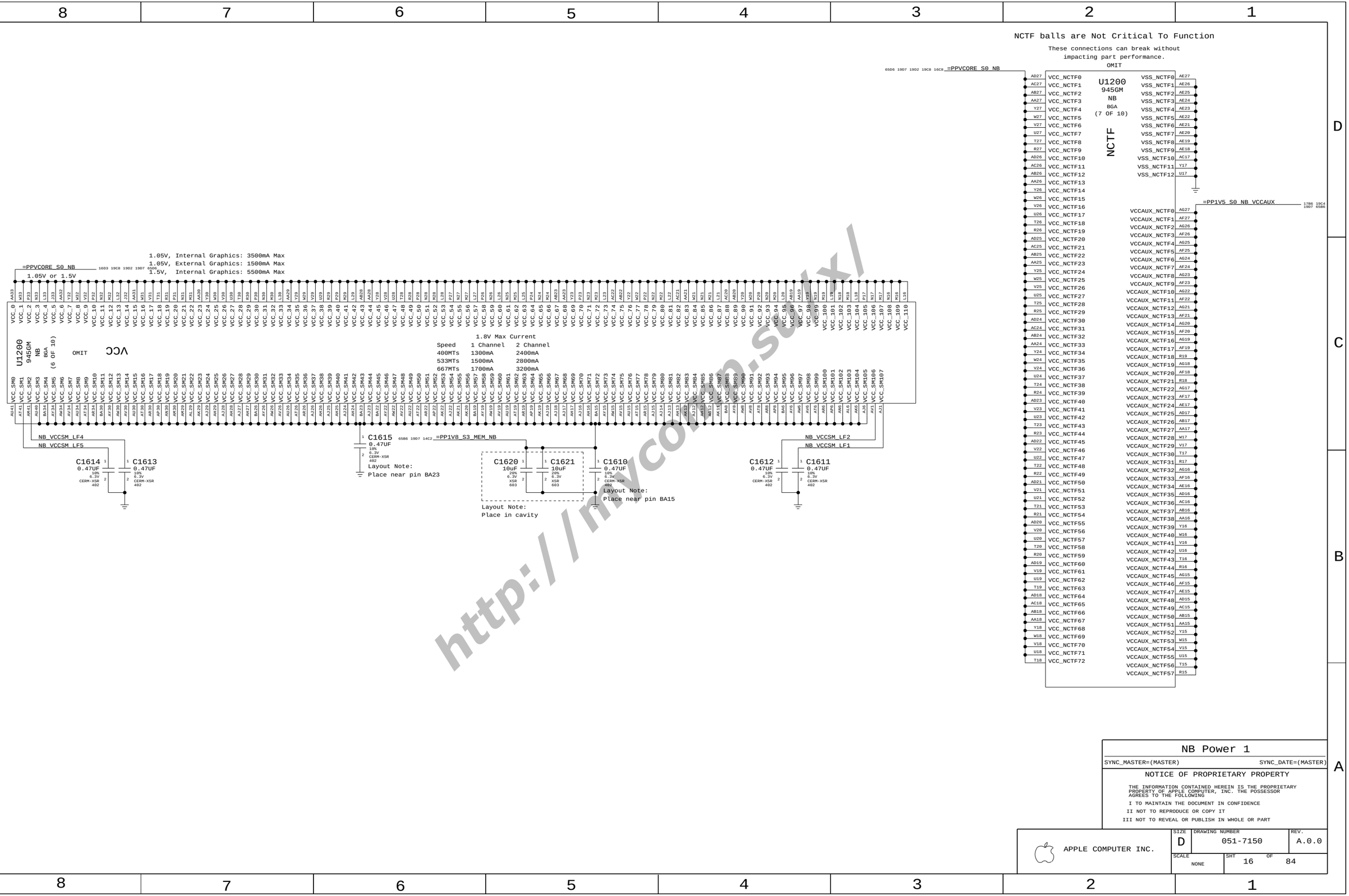


NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 15 OF 84	


NCTF balls are Not Critical To Function
These connections can break without impacting part performance.
OMIT
=PPVCORE_S0_NB
65D6 19D7 19D2 19C8 16C8
U1200
945GM
NB
BGA
(7 OF 10)
NCTF
VCC_NCTF0 AD27
VCC_NCTF1 AC27
VCC_NCTF2 AB27
VCC_NCTF3 AA27
VCC_NCTF4 Y27
VCC_NCTF5 W27
VCC_NCTF6 V27
VCC_NCTF7 U27
VCC_NCTF8 T27
VCC_NCTF9 R27
VCC_NCTF10 AD26
VCC_NCTF11 AC26
VCC_NCTF12 AB26
VCC_NCTF13 AA26
VCC_NCTF14 Y26
VCC_NCTF15 W26
VCC_NCTF16 V26
VCC_NCTF17 U26
VCC_NCTF18 T26
VCC_NCTF19 R26
VCC_NCTF20 AD25
VCC_NCTF21 AC25
VCC_NCTF22 AB25
VCC_NCTF23 AA25
VCC_NCTF24 Y25
VCC_NCTF25 W25
VCC_NCTF26 V25
VCC_NCTF27 U25
VCC_NCTF28 T25
VCC_NCTF29 R25
VCC_NCTF30 AD24
VCC_NCTF31 AC24
VCC_NCTF32 AB24
VCC_NCTF33 AA24
VCC_NCTF34 Y24
VCC_NCTF35 W24
VCC_NCTF36 V24
VCC_NCTF37 U24
VCC_NCTF38 T24
VCC_NCTF39 R24
VCC_NCTF40 AD23
VCC_NCTF41 V23
VCC_NCTF42 U23
VCC_NCTF43 T23
VCC_NCTF44 R23
VCC_NCTF45 AD22
VCC_NCTF46 V22
VCC_NCTF47 U22
VCC_NCTF48 T22
VCC_NCTF49 R22
VCC_NCTF50 AD21
VCC_NCTF51 V21
VCC_NCTF52 U21
VCC_NCTF53 T21
VCC_NCTF54 R21
VCC_NCTF55 AD20
VCC_NCTF56 V20
VCC_NCTF57 U20
VCC_NCTF58 T20
VCC_NCTF59 R20
VCC_NCTF60 AD19
VCC_NCTF61 V19
VCC_NCTF62 U19
VCC_NCTF63 T19
VCC_NCTF64 AD18
VCC_NCTF65 AC18
VCC_NCTF66 AB18
VCC_NCTF67 AA18
VCC_NCTF68 Y18
VCC_NCTF69 W18
VCC_NCTF70 V18
VCC_NCTF71 U18
VCC_NCTF72 T18
VSS_NCTF0 AE27
VSS_NCTF1 AE26
VSS_NCTF2 AE25
VSS_NCTF3 AE24
VSS_NCTF4 AE23
VSS_NCTF5 AE22
VSS_NCTF6 AE21
VSS_NCTF7 AE20
VSS_NCTF8 AE19
VSS_NCTF9 AE18
VSS_NCTF10 AC17
VSS_NCTF11 Y17
VSS_NCTF12 U17
=PP1V5_S0_NB_VCCAUX
17B6 19C4 19D7 65B6
VCCAUX_NCTF0 AG27
VCCAUX_NCTF1 AF27
VCCAUX_NCTF2 AG26
VCCAUX_NCTF3 AF26
VCCAUX_NCTF4 AG25
VCCAUX_NCTF5 AF25
VCCAUX_NCTF6 AG24
VCCAUX_NCTF7 AF24
VCCAUX_NCTF8 AG23
VCCAUX_NCTF9 AF23
VCCAUX_NCTF10 AG22
VCCAUX_NCTF11 AF22
VCCAUX_NCTF12 AG21
VCCAUX_NCTF13 AF21
VCCAUX_NCTF14 AG20
VCCAUX_NCTF15 AF20
VCCAUX_NCTF16 AG19
VCCAUX_NCTF17 AF19
VCCAUX_NCTF18 R19
VCCAUX_NCTF19 AG18
VCCAUX_NCTF20 AF18
VCCAUX_NCTF21 R18
VCCAUX_NCTF22 AG17
VCCAUX_NCTF23 AF17
VCCAUX_NCTF24 AE17
VCCAUX_NCTF25 AD17
VCCAUX_NCTF26 AB17
VCCAUX_NCTF27 AA17
VCCAUX_NCTF28 W17
VCCAUX_NCTF29 V17
VCCAUX_NCTF30 T17
VCCAUX_NCTF31 R17
VCCAUX_NCTF32 AG16
VCCAUX_NCTF33 AF16
VCCAUX_NCTF34 AE16
VCCAUX_NCTF35 AD16
VCCAUX_NCTF36 AC16
VCCAUX_NCTF37 AB16
VCCAUX_NCTF38 AA16
VCCAUX_NCTF39 Y16
VCCAUX_NCTF40 W16
VCCAUX_NCTF41 V16
VCCAUX_NCTF42 U16
VCCAUX_NCTF43 T16
VCCAUX_NCTF44 R16
VCCAUX_NCTF45 AG15
VCCAUX_NCTF46 AF15
VCCAUX_NCTF47 AE15
VCCAUX_NCTF48 AD15
VCCAUX_NCTF49 AC15
VCCAUX_NCTF50 AB15
VCCAUX_NCTF51 AA15
VCCAUX_NCTF52 Y15
VCCAUX_NCTF53 W15
VCCAUX_NCTF54 V15
VCCAUX_NCTF55 U15
VCCAUX_NCTF56 T15
VCCAUX_NCTF57 R15
1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max
=PPVCORE_S0_NB
16D3 19C8 19D2 19D7 65D6
1.05V or 1.5V
U1200
945GM
NB
BGA
(6 OF 10)
OMIT
VCC
VCC_0 AA33
VCC_1 AK3
VCC_2 AF33
VCC_3 AK33
VCC_4 L33
VCC_5 J33
VCC_6 AA32
VCC_7 Y32
VCC_8 W32
VCC_9 V32
VCC_10 P32
VCC_11 N32
VCC_12 M32
VCC_13 L32
VCC_14 J32
VCC_15 AA31
VCC_16 W31
VCC_17 V31
VCC_18 T31
VCC_19 R31
VCC_20 P31
VCC_21 N31
VCC_22 M31
VCC_23 AA30
VCC_24 V30
VCC_25 W30
VCC_26 V30
VCC_27 U30
VCC_28 T30
VCC_29 R30
VCC_30 P30
VCC_31 N30
VCC_32 L30
VCC_33 AA29
VCC_34 Y29
VCC_35 W29
VCC_36 V29
VCC_37 U29
VCC_38 R29
VCC_39 P29
VCC_40 M29
VCC_41 L29
VCC_42 AB28
VCC_43 AA28
VCC_44 Y28
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VCC_46 U28
VCC_47 T28
VCC_48 R28
VCC_49 P28
VCC_50 N28
VCC_51 M28
VCC_52 L28
VCC_53 P27
VCC_54 N27
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VCC_56 L27
VCC_57 P26
VCC_58 N26
VCC_59 L26
VCC_60 M25
VCC_61 L25
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VCC_67 AA23
VCC_68 Y23
VCC_69 V23
VCC_70 N23
VCC_71 M23
VCC_72 L23
VCC_73 AC22
VCC_74 AA22
VCC_75 AB22
VCC_76 Y22
VCC_77 W22
VCC_78 P22
VCC_79 N22
VCC_80 M22
VCC_81 L22
VCC_82 AC21
VCC_83 AA21
VCC_84 W21
VCC_85 V21
VCC_86 N21
VCC_87 L21
VCC_88 AC20
VCC_89 AB20
VCC_90 Y20
VCC_91 W20
VCC_92 P20
VCC_93 N20
VCC_94 M20
VCC_95 L20
VCC_96 AG19
VCC_97 AF19
VCC_98 AE19
VCC_99 AD19
VCC_100 L19
VCC_101 K19
VCC_102 K18
VCC_103 K17
VCC_104 L18
VCC_105 P17
VCC_106 N17
VCC_107 M17
VCC_108 N16
VCC_109 M16
VCC_110 L16
1.8V Max Current
Speed 1 Channel 2 Channel
400MTs 1300mA 2400mA
533MTs 1500mA 2800mA
667MTs 1700mA 3200mA
VCC_SM0 AU41
VCC_SM1 AT41
VCC_SM2 AM41
VCC_SM3 AU40
VCC_SM4 BA34
VCC_SM5 AT34
VCC_SM6 AM34
VCC_SM7 AV34
VCC_SM8 AU34
VCC_SM9 AT34
VCC_SM10 AR34
VCC_SM11 BA30
VCC_SM12 AY30
VCC_SM13 AW30
VCC_SM14 AV30
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VCC_SM16 AT30
VCC_SM17 AR30
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VCC_SM22 AL29
VCC_SM23 AK29
VCC_SM24 AJ29
VCC_SM25 AH29
VCC_SM26 AJ28
VCC_SM27 AH28
VCC_SM28 AJ27
VCC_SM29 AH27
VCC_SM30 BA26
VCC_SM31 AY26
VCC_SM32 AW26
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VCC_SM37 AJ26
VCC_SM38 AH26
VCC_SM39 AJ25
VCC_SM40 AH25
VCC_SM41 AJ24
VCC_SM42 AH24
VCC_SM43 BA23
VCC_SM44 AJ23
VCC_SM45 BA22
VCC_SM46 AY22
VCC_SM47 AM22
VCC_SM48 AV22
VCC_SM49 AU22
VCC_SM50 AT22
VCC_SM51 AR22
VCC_SM52 AP22
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VCC_SM59 AW19
VCC_SM60 AV19
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VCC_SM62 AJ19
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VCC_SM64 AP19
VCC_SM65 AK18
VCC_SM66 AJ18
VCC_SM67 AH17
VCC_SM68 AJ16
VCC_SM69 AH16
VCC_SM70 BA15
VCC_SM71 AY15
VCC_SM72 AV15
VCC_SM73 AU15
VCC_SM74 AM15
VCC_SM75 AV15
VCC_SM76 AU15
VCC_SM77 AT15
VCC_SM78 AR15
VCC_SM79 AJ15
VCC_SM80 AJ14
VCC_SM81 AJ13
VCC_SM82 AH13
VCC_SM83 AK12
VCC_SM84 AJ12
VCC_SM85 AM12
VCC_SM86 AK11
VCC_SM87 BA9
VCC_SM88 AY9
VCC_SM89 AW9
VCC_SM90 AV9
VCC_SM91 AU9
VCC_SM92 AT9
VCC_SM93 AR9
VCC_SM94 AP9
VCC_SM95 BA6
VCC_SM96 AY6
VCC_SM97 AW6
VCC_SM98 AV6
VCC_SM99 AU6
VCC_SM100 AM6
VCC_SM101 AP6
VCC_SM102 AL6
VCC_SM103 AK6
VCC_SM104 AJ6
VCC_SM105 AV1
VCC_SM106 AU1
VCC_SM107 AJ1
NB_VCCSM_LF4
NB_VCCSM_LF5
C1614 0.47UF 10% 6.3V CERM-X5R 402
C1613 0.47UF 10% 6.3V CERM-X5R 402
C1615 0.47UF 10% 6.3V CERM-X5R 402
65B6 19D7 14C2 =PP1V8_S3_MEM_NB
Layout Note:
Place near pin BA23
C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
Layout Note:
Place in cavity
C1610 0.47UF 10% 6.3V CERM-X5R 402
Layout Note:
Place near pin BA15
NB_VCCSM_LF2
NB_VCCSM_LF1
C1612 0.47UF 10% 6.3V CERM-X5R 402
C1611 0.47UF 10% 6.3V CERM-X5R 402
http://nvcom.su/
NB Power 1
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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SIZE D
DRAWING NUMBER 051-7150
REV. A.0.0
SCALE NONE
SHT 16 OF 84

70mA Max VCCA_CRTDAC/VCCSYNC

OMIT

U1200
945GM
NB
BGA
(8 OF 10)

POWER

19D7 19D1	=PP2V5_S0_NB_VCCSYNC	H22	VCCSYNC
65A6 19D7 19A6	=PP2V5_S0_NB_VCC_TXLVDS	C30	VCC_TXLVDS0
	60mA Max	B30	VCC_TXLVDS1
		A30	VCC_TXLVDS2
19B3	PP1V5_S0_NB_VCC3G	AJ41	VCC3G0
		AB41	VCC3G1
		Y41	VCC3G2
	1500mA Max VCC3G/3GPLL	V41	VCC3G3
		R41	VCC3G4
		N41	VCC3G5
		L41	VCC3G6
19B3	PP1V5_S0_NB_VCCA_3GPLL	AC33	VCCA_3GPLL
65A6 19D7 19C5	=PP2V5_S0_NB_VCCA_3GBG	G41	VCCA_3GBG 2mA Max
19A3	GND_NB_VSSA_3GBG	H41	VSSA_3GBG
19D1	PP2V5_S0_NB_VCCA_CRTDAC	F21	VCCA_CRTDAC0
		E21	VCCA_CRTDAC1 See VCCSYNC
19D1	GND_NB_VSSA_CRTDAC	G21	VSSA_CRTDAC
34B2 19A6	PP1V5_S0_NB_VCCA_DPLLA	B26	VCCA_DPLLA 50mA Max
19A6	PP1V5_S0_NB_VCCA_DPLLB	C39	VCCA_DPLLB 50mA Max
19B6	PP1V5_S0_NB_VCCA_HPLL	AF1	VCCA_HPLL 45mA Max
65A6 19A4	=PP2V5_S0_NB_VCCA_LVDS	A38	VCCA_LVDS 10mA Max
19A3	GND_NB_VSSA_LVDS	B39	VSSA_LVDS
19B6	PP1V5_S0_NB_VCCA_MPLL	AF2	VCCA_MPLL 45mA Max
19C1	PP3V3_S0_NB_VCCA_TVBG	H20	VCCA_TVBG
19C1	GND_NB_VSSA_TVBG	G20	VSSA_TVBG
19C1	PP3V3_S0_NB_VCCA_TVDACC	E20	VCCA_TVDACC0
		F20	VCCA_TVDACC1
19D1	PP3V3_S0_NB_VCCA_TVDACB	C20	VCCA_TVDACB0 120mA Max
		D20	VCCA_TVDACB1
19D1	PP3V3_S0_NB_VCCA_TVDACA	E19	VCCA_TVDACA0
		F19	VCCA_TVDACA1
65B6 19D7	=PP1V5_S0_NB_VCCD_HMPLL	AH1	VCCD_HMPLL0
		AH2	VCCD_HMPLL1 150mA Max
65B6 19A5	=PP1V5_S0_NB_VCCD_LVDS	A28	VCCD_LVDS0
	20mA Max	B28	VCCD_LVDS1
		C28	VCCD_LVDS2
19D1	PP1V5_S0_NB_VCCD_TVDAC	D21	VCCD_TVDAC
65B3 19C7 19C6	=PP3V3_S0_NB_VCC_HV	A23	VCC_HV0
	40mA Max	B23	VCC_HV1 24mA Max
		B25	VCC_HV2
19D1	PP1V5_S0_NB_VCCD_QTVDAC	H19	VCCD_QTVDAC
65B6 19D7 19C4 16D1	=PP1V5_S0_NB_VCCAUX	AK31	VCCAUX0
	1900mA Max	AF31	VCCAUX1
		AE31	VCCAUX2
		AC31	VCCAUX3
		AL30	VCCAUX4
		AK30	VCCAUX5
		AJ30	VCCAUX6
		AH30	VCCAUX7
		AG30	VCCAUX8
		AF30	VCCAUX9
		AE30	VCCAUX10
		AD30	VCCAUX11
		AC30	VCCAUX12
		AG29	VCCAUX13
		AF29	VCCAUX14
		AE29	VCCAUX15
		AD29	VCCAUX16
		AC29	VCCAUX17
		AG28	VCCAUX18
		AF28	VCCAUX19
		AE28	VCCAUX20
		AH22	VCCAUX21
		AJ21	VCCAUX22
		AH21	VCCAUX23
		AJ20	VCCAUX24
		AH20	VCCAUX25
		AH19	VCCAUX26
		P19	VCCAUX27
		P16	VCCAUX28
		AH15	VCCAUX29
		P15	VCCAUX30
		AH14	VCCAUX31
		AG14	VCCAUX32
		AF14	VCCAUX33
		AE14	VCCAUX34
		Y14	VCCAUX35
		AF13	VCCAUX36
		AE13	VCCAUX37
		AF12	VCCAUX38
		AE12	VCCAUX39
		AD12	VCCAUX40

=PP1V05_S0_NB_VTT	19C8 19D7 65D6		
800mA Max			
	VTT0	AC14	
	VTT1	AB14	
	VTT2	W14	
	VTT3	V14	
	VTT4	T14	
	VTT5	R14	
	VTT6	P14	
	VTT7	N14	
	VTT8	M14	
	VTT9	L14	
	VTT10	AD13	
	VTT11	AC13	
	VTT12	AB13	
	VTT13	AA13	
	VTT14	Y13	
	VTT15	W13	
	VTT16	V13	
	VTT17	U13	
	VTT18	T13	
	VTT19	R13	
	VTT20	N13	
	VTT21	M13	
	VTT22	L13	
	VTT23	AB12	
	VTT24	AA12	
	VTT25	Y12	
	VTT26	W12	
	VTT27	V12	
	VTT28	U12	
	VTT29	T12	
	VTT30	R12	
	VTT31	P12	
	VTT32	N12	
	VTT33	M12	
	VTT34	L12	
	VTT35	R11	
	VTT36	P11	
	VTT37	N11	
	VTT38	M11	
	VTT39	R10	
	VTT40	P10	
	VTT41	N10	
	VTT42	M10	
	VTT43	P9	
	VTT44	N9	
	VTT45	M9	
	VTT46	R8	
	VTT47	P8	
	VTT48	N8	
	VTT49	M8	
	VTT50	P7	
	VTT51	N7	
	VTT52	M7	
	VTT53	R6	
	VTT54	P6	
	VTT55	M6	
NB_VTTLF_CAP3	VTT56	A6	
	VTT57	R5	
	VTT58	P5	
	VTT59	N5	
	VTT60	M5	
	VTT61	P4	
	VTT62	N4	
	VTT63	M4	
	VTT64	R3	
	VTT65	P3	
	VTT66	N3	
	VTT67	M3	
	VTT68	R2	
	VTT69	P2	
	VTT70	M2	
NB_VTTLF_CAP2	VTT71	D2	
NB_VTTLF_CAP1	VTT72	AB1	
	VTT73	R1	
	VTT74	P1	
	VTT75	N1	
	VTT76	M1	

C1713 0.47UF 10% 6.3V CERM-X5R 402

C1711 0.47UF 10% 6.3V CERM-X5R 402

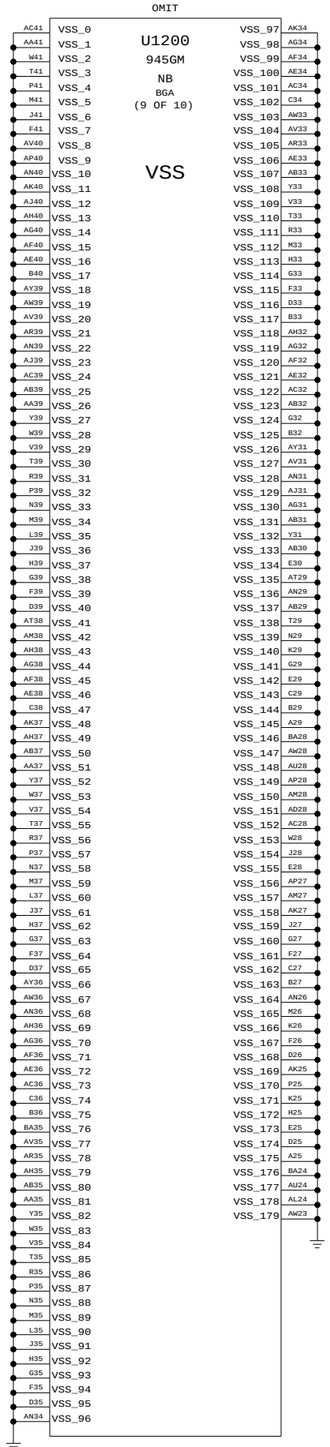
C1712 0.22uF 20% 6.3V X5R 402

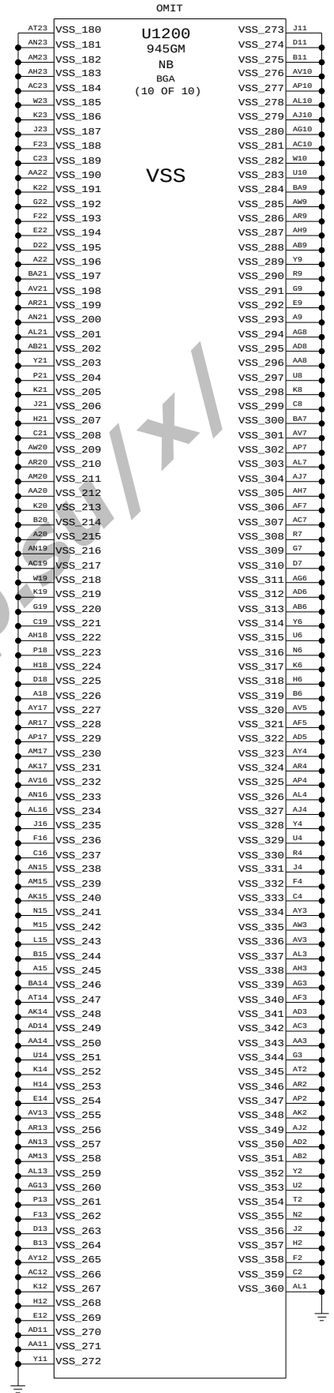
NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 17 OF 84	





NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 18 OF 84	

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	16C8 16D3 19C8 19D2 65D6	1500mA Max
	=PP1V05_S0_FSB_NB	12A7 12B7 12C2 14B8 34C6 34C9 65D5	10mA Max?
	=PP1V05_S0_NB_VTT	17D3 19C8 65D6	800mA Max
	=PP1V05_S0_NB_CRT	19D6 65D6	?mA Max
3674mA Max	=PP1V5_S0_NB	60A7 65C6 65C8	?mA Max
	=PP1V5_S0_NB_3G	19B5 65C6	1500mA Max
	=PP1V5_S0_NB_3GPLL	19B5 65C6	
	=PP1V5_S0_NB_PCIE	13D2 65C6	?mA Max
	=PP1V5_S0_NB_PLL	19B8 65B6	100mA Max
	=PP1V5_S0_NB_TVDAC	19D2 19D6 65B6	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	17C6 65B6	150mA Max
	=PP1V5_S0_NB_VCCAUX	16D1 17B6 19C4 65B6	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	14C2 16B6 65B6	3200mA Max
132mA Max	=PP2V5_S0_NB_VCCSYNC	17D6 19D1	70mA Max
	=PP2V5_S0_NB_VCC_TXLVDS	17D6 19A6 65A6	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	17D6 19C5 65A6	2mA Max
40mA Max?	=PP3V3_S0_NB	14C7 14D6 20A4 20B4 65B3	?mA Max
	=PP3V3_S0_NB_VCC_HV	17C6 19C6 65B3	40mA Max

=PP1V05_S0_NB_CRT (65D6 19D7)
- CRT_RED — 13B5
- CRT_GREEN — 13B5
- CRT_BLUE — 13B5
- CRT_RED_L — 13B5
- CRT_GREEN_L — 13B5
- CRT_BLUE_L — 13B5
- CRT_IREF — 13B5
- CRT_HSYNC_R — 13B5
- CRT_VSYNC_R — 13B5

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK — 13B5

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA — 13B5

=PP1V5_S0_NB_TVDAC (65B6 19D7 19D2)
- TV_DACA_OUT — 13C5
- TV_DACB_OUT — 13C5
- TV_DACC_OUT — 13C5
- TV_IREF — 13C5
- TV_IRTNA — 13C5
- TV_IRTNB — 13C5
- TV_IRTNC — 13C5

TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA — 13D5

TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB — 13D5

NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 — 14C6

NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 — 14C6

NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 — 14C6

NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 — 14C6

TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK — 14B6

TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA — 14B6

LVDS_IBG — 13D5

R1990 1.5K 1% 1/16W MF-LF 402

LVDS_VREFH — 13D5

LVDS_VREFL — 13D5

=PPVCORE_S0_NB (65D6 16C8 16D3 16C8) — (MCH CRTDAC ANALOG 2.5V PWR)
- PP2V5_S0_NB_VCCA_CRTDAC — 17D6
- GND_NB_VSSA_CRTDAC — 17D6

(MCH H/V SYNC 2.5V PWR)
- =PP2V5_S0_NB_VCCSYNC — 17D6 19D7

=PP1V5_S0_NB_TVDAC (65B6 19D7 19D6) — (MCH TVDAC DEDICATED PWR 1.5V)
- PP1V5_S0_NB_VCCD_TVDAC — 17C6

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
- PP1V5_S0_NB_VCCD_QTVDAC — 17B6

(MCH TV OUT CHANNEL A 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACA — 17C6

(MCH TV OUT CHANNEL B 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACB — 17C6

(MCH TV OUT CHANNEL C 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACC — 17C6

(MCH TV DAC BAND GAP 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVBG — 17C6
- GND_NB_VSSA_TVBG — 17C6

=PPVCORE_S0_NB (65D6 16C8 16D3 16C8 19D7 19D2) — 1500mA Max

GMCH CORE PWR 1.05V BYPASS

CRITICAL
- C1900 470uF 20% 2.5V TANT D2T
- C1902 10uF 20% 6.3V X5R 603
- C1903 10uF 20% 6.3V X5R 603
- C1904 1uF 10% 6.3V CERM 402
- C1905 0.22uF 20% 6.3V X5R 402
- C1906 0.22uF 20% 6.3V X5R 402
- C1907 0.22uF 20% 6.3V X5R 402

=PP1V05_S0_NB_VTT (65D6 19D7 17D3) — 800mA Max

MCH VTT BYPASS
(MCH FSB 1.05V PWR)
(SHARE C0940 470UF)

- C1965 4.7uF 20% 6.3V CERM 603
- C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

- C1967 0.22uF 20% 6.3V X5R 402

Layout Note: Place on the edge

=PP3V3_S0_NB_VCC_HV (65B3 19C7 17C6) — 40mA Max

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

- C1914 10uF 20% 6.3V X5R 603
- C1915 0.1uF 20% 10V CERM 402

=PP2V5_S0_NB_VCCA_3GBG (65A6 19D7 17D6) — 2mA Max

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

- C1916 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_VCCAUX (65B6 19D7 17B6 16D1) — 1900mA Max

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

- C1918 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_PLL (65B6 19D7) — 100mA Max

L1934 FERR-120-OHM-0.2A 0603

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL — 17C6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

45mA Max

- C1934 22UF 20% 6.3V CERM 805
- C1935 0.1uF 20% 10V CERM 402

L1936 FERR-120-OHM-0.2A 0603

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL — 17C6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

45mA Max

- C1936 22UF 20% 6.3V CERM 805
- C1937 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_3G (65C6 19D7) — 1500mA Max

L1970 91nH 1210

Layout Note: Place L and C close to MCH

- C1970 220UF 20% 2.5V POLY CASE-B2
- C1971 10uF 20% 6.3V X5R 603
- C1972 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G — 17D6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

1500mA Max

=PP1V5_S0_NB_3GPLL (65C6 19D7)

L1975 1.0UH-220MA-0.12-OHM 0805

PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.5V

R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL — 17D6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

- C1975 10uF 20% 6.3V XSR 603
- C1976 0.1uF 20% 10V CERM 402

GND_NB_VSSA_3GBG — 17D6

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

=PP2V5_S0_NB_DPLL (65A6)

CRITICAL
U1900 TPS73115 SOT23-5
IN — OUT — PP1V5_S0_NB_DPLL
EN — NR/FB — TPS73115_NR
GND

- C1950 1uF 10% 6.3V CERM 402
- C1951 0.01uF 10% 16V CERM 402
- C1952 10uF 20% 6.3V X5R 603
- C1953 0.1uF 20% 10V CERM 402
- C1954 0.1uF 20% 10V CERM 402

MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

NO STUFF
- R1953 0 5% 1/16W MF-LF 402

GMCH VCCA_DPLLA FILTER
(CRT/TVOUT PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLA — 17C6 34B2
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

50MA MAX

- R1954 0 5% 1/16W MF-LF 402

GMCH VCCA_DPLLB FILTER
(LVDS PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLB — 17C6 65A6 19D7 17D6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

50MA MAX

NO STUFF

MCH VCC_TXLVDS BYPASS
(MCH LVDS TRANSMITTER 2.5V PWR)

=PP2V5_S0_NB_VCC_TXLVDS — 60MA MAX

- C1990 4.7UF 20% 6.3V CERM 603
- C1991 0.1uF 20% 10V CERM 402

MCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)

=PP1V5_S0_NB_VCCD_LVDS (65B6 17C6) — 20MA MAX

- C1992 10uF 20% 6.3V XSR 603
- C1993 0.1uF 20% 10V CERM 402

MCH VCCA_LVDS BYPASS
(MCH LVDS ANALOG 2.5V PWR)

=PP2V5_S0_NB_VCCA_LVDS (65A6 17C6) — 10MA MAX

- C1994 0.01UF 20% 16V CERM 402
- C1995 0.1uF 20% 10V CERM 402

GND_NB_VSSA_LVDS — 17C6

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 19 OF 84	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402
1
2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 65B3
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 65B3
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14C7 14D6 19C7 20B4 65B3
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

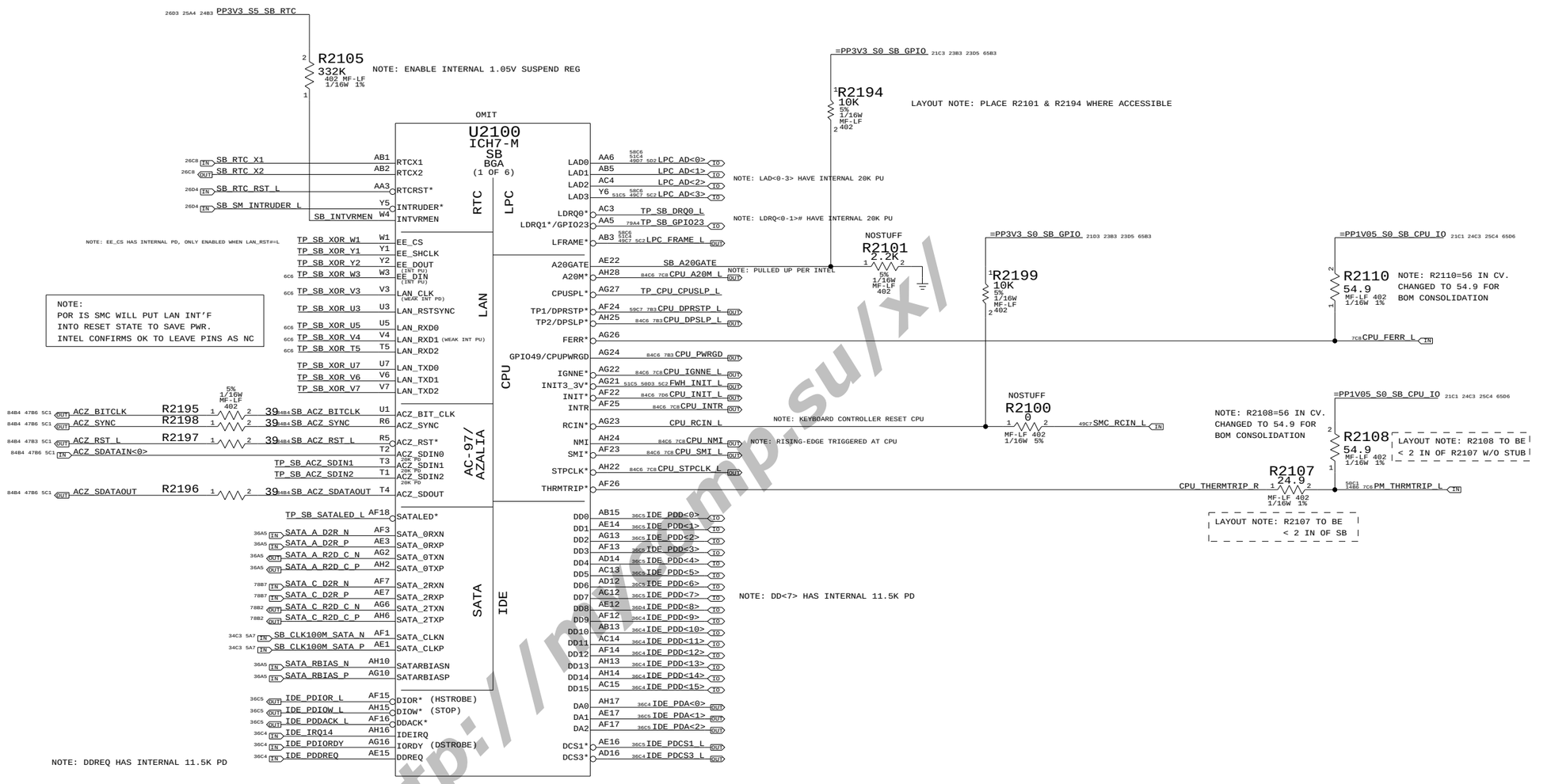
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 20 OF 84	



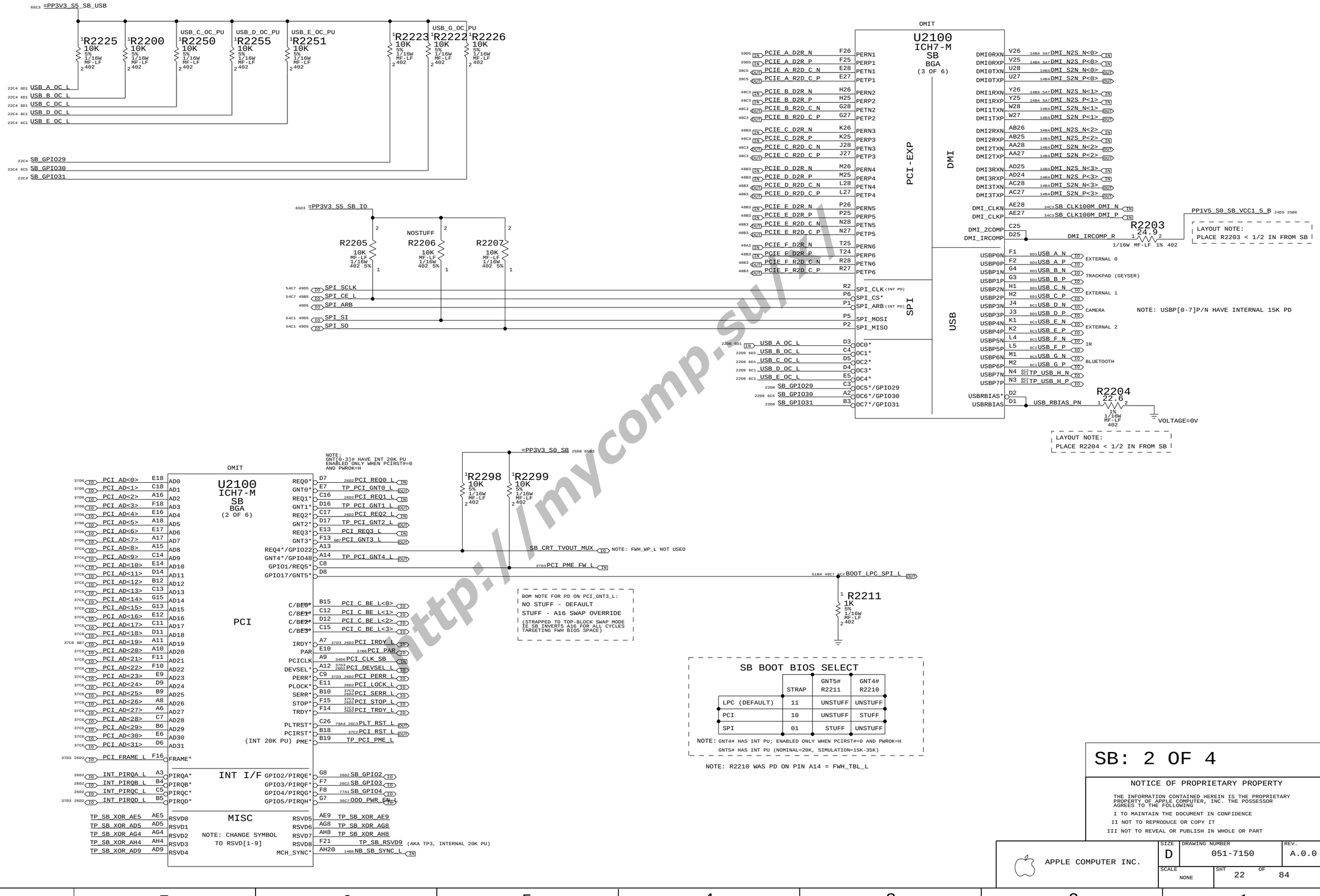
	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 21 OF 84	



SB: 2 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE

SHT 22 OF 84

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21C3 21D3 23B3 65B3

=PP3V3_S5_SB 23A7 23B7 23D8 25C8 65D3

65D3 25C8 23D4 23B7 23A7 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27D8 TO SMB_CLK — C22 SMBCLK
27D8 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1
PM_RI_L — A28 RI*

SB_SPKR — A19 SPKR (INT WEAK PD)
58C6 51B5 50A2 49C5 5C2 OUT PM_SUS_STAT_L — A27 SUS_STAT*
49B7 26C5 5B2 IN PM_SYSRST_L — A22 SYS_RST*
14B6 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

33C4 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
33C4 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23A6 BIOS_REC — B21 GPIO27
23A6 FWH_MFG_MODE — E23 GPIO28
58C6 51C4 49C5 5C2 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
26A4 TP_GPU_D3COLD_RST_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*
47C3 39C6 5B1 IN PCIE_WAKE_L — F20 WAKE*
58C6 51C5 49C7 5C2 TO INT_SERIRQ — AH21 SERIRQ
49B7 IN PM_THRM_L — AF20 THRM*
26B8 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
TO TP_SB_GPIO6 — AC21 GPIO6
49B7 IN SMC_RUNTIME_SCI_L — AC18 GPIO7
49B7 IN SMC_EXTSMI_L — E21 GPIO8

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
36B5 SATA_C_DET_L IN

CLKS
CLK14 — AC1 34A6 SB_CLK14P3M_TIMER IN
CLK48 — B2 34C7 SB_CLK48M_USBCTLR IN
SUSCLK — C20 6C6 SUS_CLK_SB OUT

SYS GPIO
PWR MNGT
SLP_S3* — B24 64C8 49C5 43B7 42A8 PM_SLP_S3_L OUT
SLP_S4* — D23 49C5 64B8 41B6 PM_SLP_S4_L OUT
SLP_S5* — F22 50A2 49C5 PM_SLP_S5_L OUT
PWROK — AA4 26A6 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 59C8 64C9 14B7 PM_DPRSLPVR OUT
TP0/BATLOW* — C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 49D7 PM_PWRBTN_L IN
LAN_RST* — C19 49D7 PM_LAN_ENABLE IN
RSMRST* — Y4

NOTE:
SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F
IN RESET STATE TO SAVE PWR

GPIO
GPIO9 — E20 5DB2 49B5 SMS_INT_L IN
GPIO10 — A20 49D7 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 48A3 LAN_ENERGY_DET IN
GPIO13 — E19
DEF=GPI GPIO14 — R4 36D5 IDE_RESET_L OUT
GPIO15 — E22 SV_SET_UP 5C2 23B6 51B5
GPIO24 — R3 CRB_SV_DET 23B6
GPIO25 — D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 33B4 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 23A3 SATA_C_PWR_EN_L OUT

=PP3V3_S5_SB_PM 11B5 26C5 65D3

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

49D7 PM_BATLOW_L IN
49D7 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
49D5 SMC_WAKE_SCI_L IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

65D3 25C8 23D8 23D4 23A7 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 5C2 23C3 51B5
CRB_SV_DET 23C3

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

65D3 25C8 23D8 23D4 23B7 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23C5
BIOS_REC 23C5

=PP3V3_S0_SB_GPIO 21C3 21D3 23D5 65B3

R2388 10K 5% 1/16W MF-LF 402

23B3 SATA_C_PWR_EN_L

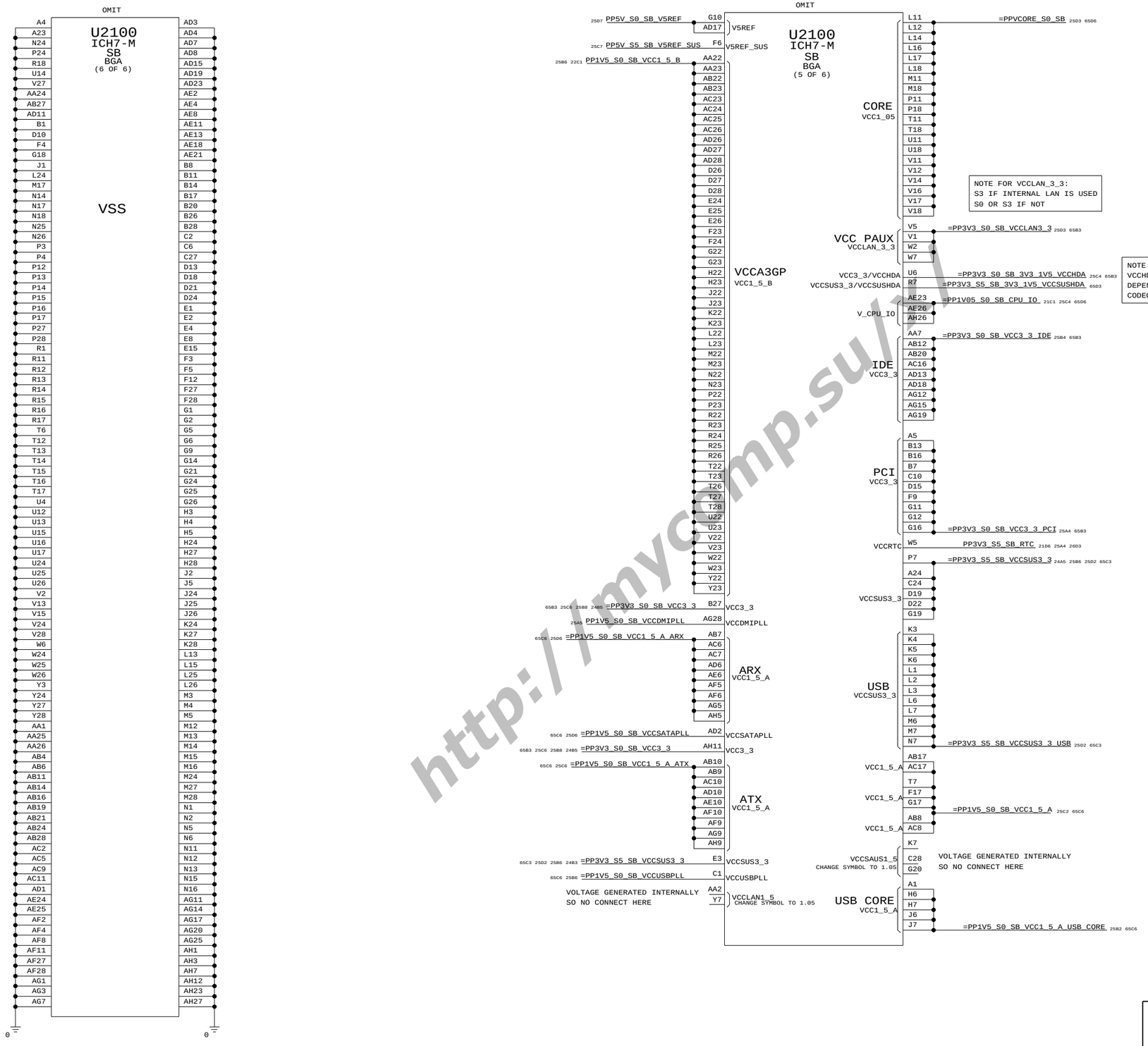
SB: 3 OF 4

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 23 OF 84

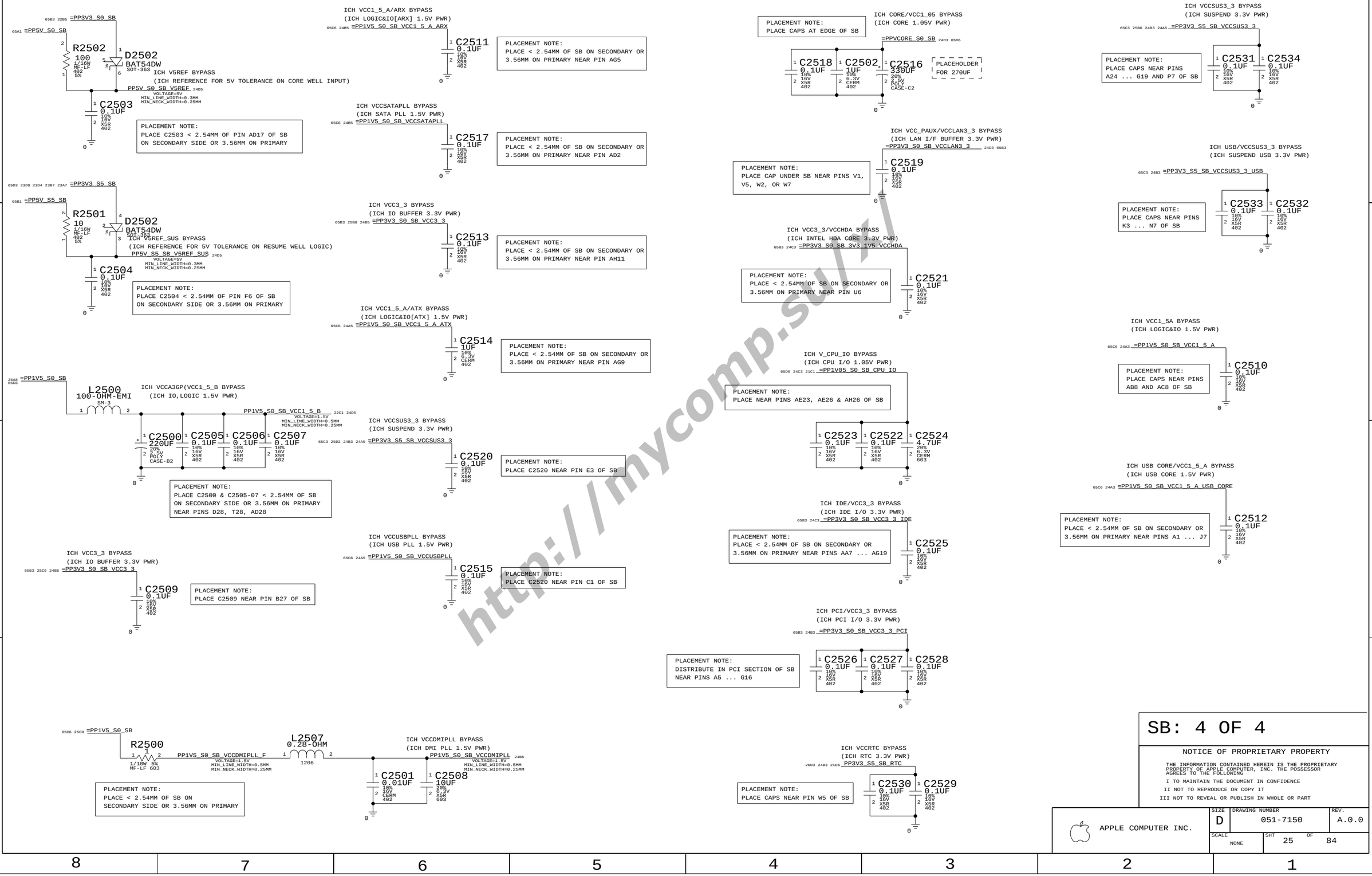


SB: 4 OF 4

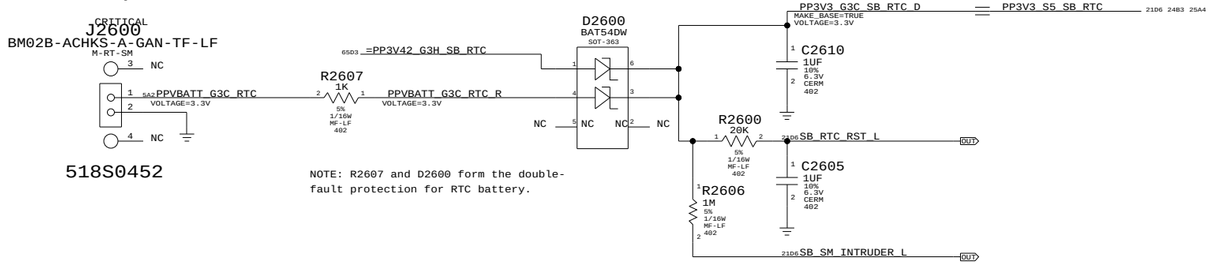
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

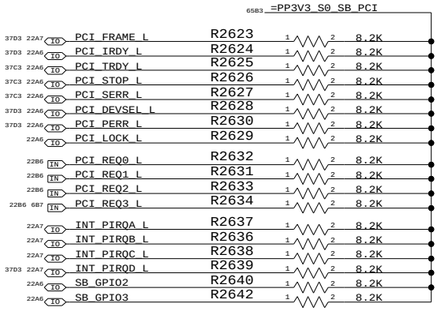
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 24 OF 84	



RTC Battery Connector

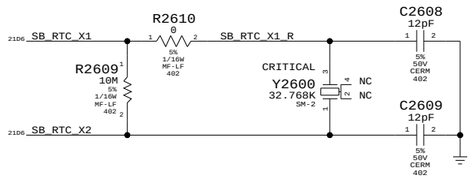


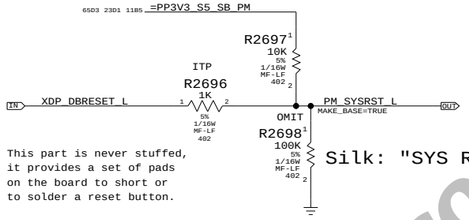
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit

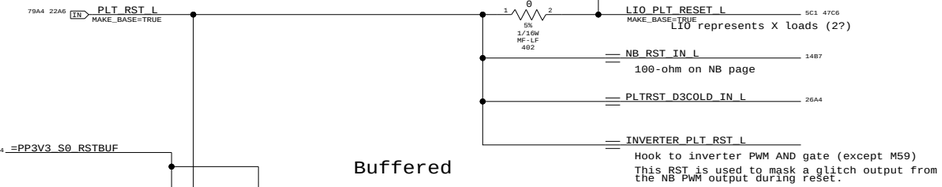




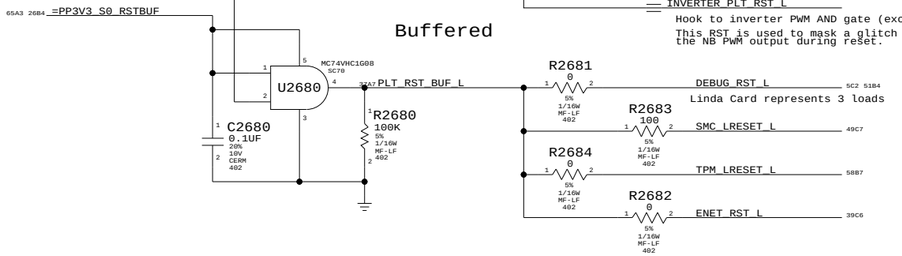
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Platform Reset Connections

Unbuffered

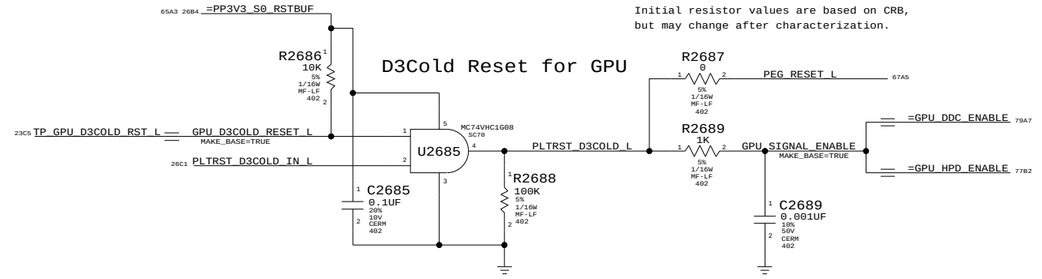


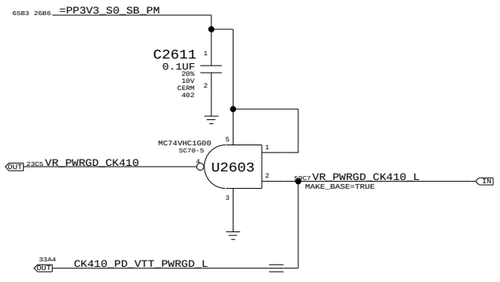
Buffered



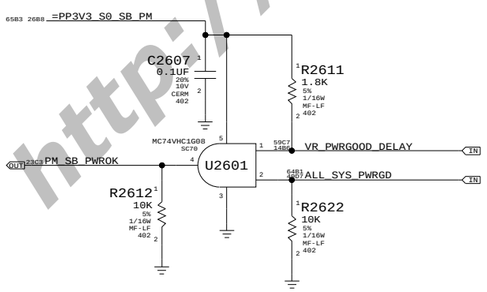
Initial resistor values are based on CRB, but may change after characterization.

D3Cold Reset for GPU





1G00 used as small & cheap inverter



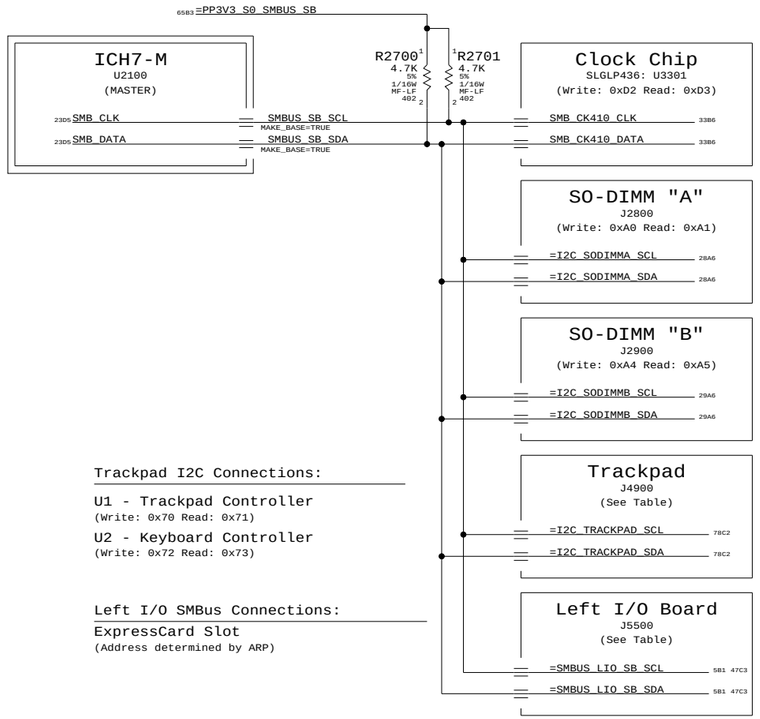
SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	A.0.0
SCALE: NONE	SHT 26 OF 84	

ICH7-M SMBus Connections



Trackpad I2C Connections:

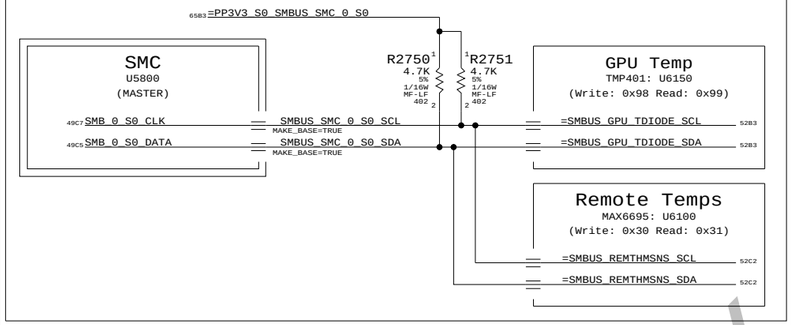
U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

Left I/O SMBus Connections:

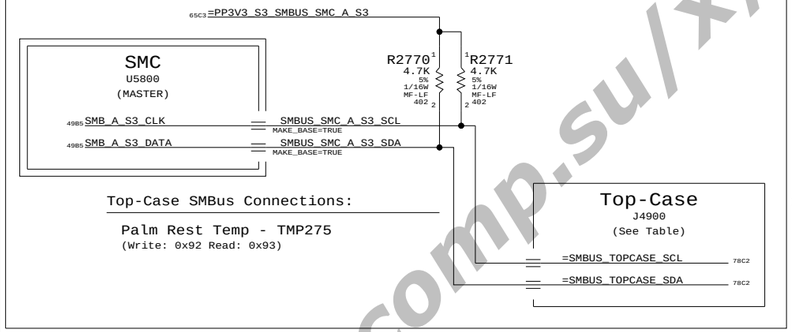
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

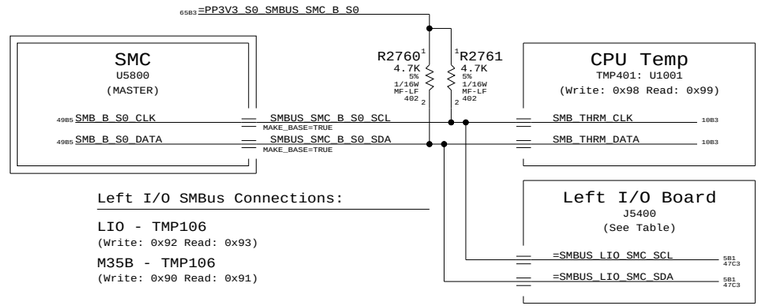
NOTE: SMC RMT bus remains powered and may be active in S3 state



Top-Case SMBus Connections:

Palm Rest Temp - TMP275
(Write: 0x92 Read: 0x93)

SMC "B" SMBus Connections

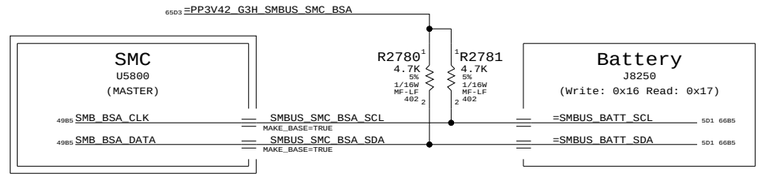


Left I/O SMBus Connections:

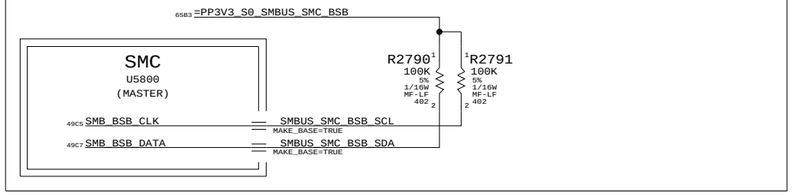
LIO - TMP106
(Write: 0x92 Read: 0x93)

M35B - TMP106
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 27 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Expansion" (surface-mount) slot

65B6 29D6 29D3 29B2 28D3 28B2 =PP1V8_S3_MEM

32B3 29D6 MEM_VREF

C2801 2.2uF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

CRITICAL
J2800
F-RT-SM-M9
DDR2-SODIMM-DUAL

203 201 NC

		1A	VREF	VSS0	2A		
		3A	VSS1	DQ4	4A	MEM_A_DQ<8>	15C7
15C7	MEM_A_DQ<14>	5A	DQ0	DQ5	6A	MEM_A_DQ<12>	15C7
15C7	MEM_A_DQ<13>	7A	DQ1	VSS2	8A		
		9A	VSS4	DM0	10A	MEM_A_DM<1>	15D5
15C5	MEM_A_DQS_N<1>	11A	DQS0*	VSS5	12A		
15C5	MEM_A_DQS_P<1>	13A	DQS0	DQ6	14A	MEM_A_DQ<15>	15C7
		15A	VSS6	DQ7	16A	MEM_A_DQ<9>	15C7
15C7	MEM_A_DQ<10>	17A	DQ2	VSS7	18A		
15C7	MEM_A_DQ<11>	19A	DQ3	DQ12	20A	MEM_A_DQ<2>	15D7
		21A	VSS8	DQ13	22A	MEM_A_DQ<3>	15D7
15D7	MEM_A_DQ<5>	23A	DQ8	VSS9	24A		
15D7	MEM_A_DQ<4>	25A	DQ9	DM1	26A	MEM_A_DM<0>	15D5
		27A	VSS10	VSS11	28A		
15C5	MEM_A_DQS_N<0>	29A	DQS1*	CK0	30A	MEM_CLK_P<0>	14D4
15C5	MEM_A_DQS_P<0>	31A	DQS1	CK0*	32A	MEM_CLK_N<0>	14D4
		33A	VSS12	VSS13	34A		
15D7	MEM_A_DQ<6>	35A	DQ10	DQ14	36A	MEM_A_DQ<1>	15D7
15D7	MEM_A_DQ<7>	37A	DQ11	DQ15	38A	MEM_A_DQ<0>	15D7
		39A	VSS14	VSS15	40A		
			KEY				
		41A	VSS16	VSS17	42A		
15C7	MEM_A_DQ<19>	43A	DQ16	DQ20	44A	MEM_A_DQ<23>	15C7
15C7	MEM_A_DQ<18>	45A	DQ17	DQ21	46A	MEM_A_DQ<22>	15C7
		47A	VSS18	VSS19	48A		
15C5	MEM_A_DQS_N<2>	49A	DQS2*	NC0	50A	DIMM_OVERTEMP_L	29C3 50D3
15C5	MEM_A_DQS_P<2>	51A	DQS2	DM2	52A	MEM_A_DM<2>	15D5
		53A	VSS21	VSS22	54A		
15C7	MEM_A_DQ<20>	55A	DQ18	DQ22	56A	MEM_A_DQ<21>	15C7
15C7	MEM_A_DQ<16>	57A	DQ19	DQ23	58A	MEM_A_DQ<17>	15C7
		59A	VSS23	VSS24	60A		
15C7	MEM_A_DQ<28>	61A	DQ24	DQ28	62A	MEM_A_DQ<29>	15C7
15C7	MEM_A_DQ<25>	63A	DQ25	DQ29	64A	MEM_A_DQ<24>	15C7
		65A	VSS25	VSS26	66A		
15C5	MEM_A_DM<3>	67A	DM3	DQS3*	68A	MEM_A_DQS_N<3>	15C5
	NC	69A	NC1	DQS3	70A	MEM_A_DQS_P<3>	15C5
		71A	VSS27	VSS28	72A		
15C7	MEM_A_DQ<27>	73A	DQ26	DQ30	74A	MEM_A_DQ<26>	15C7
15C7	MEM_A_DQ<30>	75A	DQ27	DQ31	76A	MEM_A_DQ<31>	15C7
		77A	VSS29	VSS30	78A		
30D6 14C4	MEM_CKE<0>	79A	CKE0	NC/CKE1	80A	MEM_CKE<1>	14C4 30D6
		81A	VDD0	VDD1	82A		
	NC	83A	NC2	NC/A15	84A	MEM_A_A<15>	6D6
30B6 15D5	MEM_A_BS<2>	85A	BA2	NC/A14	86A	MEM_A_A<14>	6D6
		87A	VDD2	VDD3	88A		
30C6 15B5	MEM_A_A<12>	89A	A12	A11	90A	MEM_A_A<11>	15B5 30C6
30C6 15B5	MEM_A_A<9>	91A	A9	A7	92A	MEM_A_A<7>	15B5 30C6
30C6 15B5	MEM_A_A<8>	93A	A8	A6	94A	MEM_A_A<6>	15B5 30C6
		95A	VDD4	VDD5	96A		
30C6 15B5	MEM_A_A<5>	97A	A5	A4	98A	MEM_A_A<4>	15B5 30C6
30C6 15B5	MEM_A_A<3>	99A	A3	A2	100A	MEM_A_A<2>	15C5 30C6
30C6 15C5	MEM_A_A<1>	101A	A1	A0	102A	MEM_A_A<0>	15C5 30C6
		103A	VDD6	VDD7	104A		
30C6 15B5	MEM_A_A<10>	105A	A10/AP	BA1	106A	MEM_A_BS<1>	15D5 30B6
30B6 15D5	MEM_A_BS<0>	107A	BA0	RAS*	108A	MEM_A_RAS_L	15B5 30B6
30B6 15B5	MEM_A_WE_L	109A	WE*	S0*	110A	MEM_CS_L<0>	14C4 30D6
		111A	VDD8	VDD9	112A		
30B6 15D5	MEM_A_CAS_L	113A	CAS*	ODT0	114A	MEM_ODT<0>	14C4 30C6
30D6 14C4	MEM_CS_L<1>	115A	NC/S1*	NC/A13	116A	MEM_A_A<13>	15B5 30C6
		117A	VDD10	VDD11	118A		
30C6 14C4	MEM_ODT<1>	119A	NC/ODT1	NC3	120A	NC	
		121A	VSS31	VSS32	122A		
15B7	MEM_A_DQ<35>	123A	DQ32	DQ36	124A	MEM_A_DQ<38>	15B7
15B7	MEM_A_DQ<39>	125A	DQ33	DQ37	126A	MEM_A_DQ<34>	15B7
		127A	VSS33	VSS34	128A		
15C5	MEM_A_DQS_N<4>	129A	DQS4*	DM4	130A	MEM_A_DM<4>	15C5
15C5	MEM_A_DQS_P<4>	131A	DQS4	VSS35	132A		
		133A	VSS36	DQ38	134A	MEM_A_DQ<32>	15C7
15B7	MEM_A_DQ<37>	135A	DQ34	DQ39	136A	MEM_A_DQ<36>	15B7
15C7	MEM_A_DQ<33>	137A	DQ35	VSS37	138A		
		139A	VSS38	DQ44	140A	MEM_A_DQ<57>	15B7
15A7	MEM_A_DQ<60>	141A	DQ40	DQ45	142A	MEM_A_DQ<63>	15A7
15B7	MEM_A_DQ<59>	143A	DQ41	VSS39	144A		
		145A	VSS40	DQS5*	146A	MEM_A_DQS_N<7>	15C5
15C5	MEM_A_DM<7>	147A	DM5	DQS5	148A	MEM_A_DQS_P<7>	15C5
		149A	VSS41	VSS42	150A		
15B7	MEM_A_DQ<58>	151A	DQ42	DQ46	152A	MEM_A_DQ<56>	15B7
15A7	MEM_A_DQ<61>	153A	DQ43	DQ47	154A	MEM_A_DQ<62>	15A7
		155A	VSS43	VSS44	156A		
15B7	MEM_A_DQ<43>	157A	DQ48	DQ52	158A	MEM_A_DQ<40>	15B7
15B7	MEM_A_DQ<45>	159A	DQ49	DQ53	160A	MEM_A_DQ<42>	15B7
		161A	VSS45	VSS46	162A		
	NC	163A	NC_TEST	CK1	164A	MEM_CLK_P<1>	14D4
		165A	VSS47	CK1*	166A	MEM_CLK_N<1>	14D4
15C5	MEM_A_DQS_N<5>	167A	DQS6*	VSS48	168A		
15C5	MEM_A_DQS_P<5>	169A	DQS6	DM6	170A	MEM_A_DM<5>	15C5
		171A	VSS49	VSS50	172A		
15B7	MEM_A_DQ<41>	173A	DQ50	DQ54	174A	MEM_A_DQ<47>	15B7
15B7	MEM_A_DQ<46>	175A	DQ51	DQ55	176A	MEM_A_DQ<44>	15B7
		177A	VSS51	VSS52	178A		
15B7	MEM_A_DQ<51>	179A	DQ56	DQ60	180A	MEM_A_DQ<54>	15B7
15B7	MEM_A_DQ<50>	181A	DQ57	DQ61	182A	MEM_A_DQ<55>	15B7
		183A	VSS53	VSS54	184A		
15C5	MEM_A_DM<6>	185A	DM7	DQS7*	186A	MEM_A_DQS_N<6>	15C5
		187A	VSS55	DQS7	188A	MEM_A_DQS_P<6>	15C5
15B7	MEM_A_DQ<53>	189A	DQ58	VSS56	190A		
15B7	MEM_A_DQ<48>	191A	DQ59	DQ62	192A	MEM_A_DQ<52>	15B7
65A3 29A6 29A3	=PPSPD_S0_MEM	193A	VSS57	DQ63	194A	MEM_A_DQ<49>	15B7
27D6	=I2C_SODIMMA_SDA	195A	SDA	VSS58	196A		
27D6	=I2C_SODIMMA_SCL	197A	SCL	SA0	198A		
		199A	VDDSPD	SA1	200A	ADDR=0xA0(WR)/0xA1(RD)	

202 204 NC

516S0471

=PP1V8_S3_MEM 28B2 28D6 29B2 29D3 29D6 65B6

DDR2 Bypass Caps

(For return current)

65B6 29D6 29D3 29B2 28D6 28D3 =PP1V8_S3_MEM

C2808 10UF 20% 6.3V X5R 603

C2809 10UF 20% 6.3V X5R 603

C2810 1UF 10% 6.3V CERM 402

C2811 1UF 10% 6.3V CERM 402

C2812 1UF 10% 6.3V CERM 402

C2813 1UF 10% 6.3V CERM 402

C2814 1UF 10% 6.3V CERM 402

C2815 1UF 10% 6.3V CERM 402

C2816 1UF 10% 6.3V CERM 402

C2817 1UF 10% 6.3V CERM 402

C2818 1UF 10% 6.3V CERM 402

C2819 1UF 10% 6.3V CERM 402

C2820 1UF 10% 6.3V CERM 402

C2821 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 28 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.

"Factory" (thru-hole) slot

65B6 29D3 29B2 28D6 28D3 28B2 =PP1V8_S3_MEM

32B3 28D6 MEM_VREF

C2901 2.2uF 20% 6.3V CERM1 603

C2900 0.1uF 20% 10V CERM 402

201 NC

CRITICAL
J2900
F-RT-TH1
DDR2-SODIMM-DUAL

	1B	VREF		2B	VSS0		
	3B	VSS1		4B	DQ4	MEM_B_DQ<9>	15C4
15C4	MEM_B_DQ<15>	5B	DQ0	6B	DQ5	MEM_B_DQ<11>	15C4
15C4	MEM_B_DQ<14>	7B	DQ1	8B	VSS2		
	9B	VSS4		10B	DM0	MEM_B_DM<1>	15D2
15C2	MEM_B_DQS_N<1>	11B	DQS0*	12B	VSS5		
15C2	MEM_B_DQS_P<1>	13B	DQS0	14B	DQ6	MEM_B_DQ<12>	15C4
	15B	VSS6		16B	DQ7	MEM_B_DQ<8>	15C4
15C4	MEM_B_DQ<10>	17B	DQ2	18B	VSS7		
15C4	MEM_B_DQ<13>	19B	DQ3	20B	DQ12	MEM_B_DQ<3>	15D4
	21B	VSS8		22B	DQ13	MEM_B_DQ<6>	15D4
15D4	MEM_B_DQ<7>	23B	DQ8	24B	VSS9		
15D4	MEM_B_DQ<2>	25B	DQ9	26B	DM1	MEM_B_DM<0>	15D2
	27B	VSS10		28B	VSS11		
15C2	MEM_B_DQS_N<0>	29B	DQS1*	30B	CK0	MEM_CLK_P<3>	14D4
15C2	MEM_B_DQS_P<0>	31B	DQS1	32B	CK0*	MEM_CLK_N<3>	14D4
	33B	VSS12		34B	VSS13		
15D4	MEM_B_DQ<1>	35B	DQ10	36B	DQ14	MEM_B_DQ<0>	15D4
15D4	MEM_B_DQ<4>	37B	DQ11	38B	DQ15	MEM_B_DQ<5>	15D4
	39B	VSS14		40B	VSS15		
			KEY				
	41B	VSS16		42B	VSS17		
15C4	MEM_B_DQ<21>	43B	DQ16	44B	DQ20	MEM_B_DQ<22>	15C4
15C4	MEM_B_DQ<19>	45B	DQ17	46B	DQ21	MEM_B_DQ<18>	15C4
	47B	VSS18		48B	VSS19		
15C2	MEM_B_DQS_N<2>	49B	DQS2*	50B	NC0	DIMM_OVERTEMP_L	29C3 50D3
15C2	MEM_B_DQS_P<2>	51B	DQS2	52B	DM2	MEM_B_DM<2>	15D2
	53B	VSS21		54B	VSS22		
15C4	MEM_B_DQ<20>	55B	DQ18	56B	DQ22	MEM_B_DQ<17>	15C4
15C4	MEM_B_DQ<23>	57B	DQ19	58B	DQ23	MEM_B_DQ<16>	15C4
	59B	VSS23		60B	VSS24		
15C4	MEM_B_DQ<29>	61B	DQ24	62B	DQ28	MEM_B_DQ<26>	15C4
15C4	MEM_B_DQ<24>	63B	DQ25	64B	DQ29	MEM_B_DQ<28>	15C4
	65B	VSS25		66B	VSS26		
15C2	MEM_B_DM<3>	67B	DM3	68B	DQS3*	MEM_B_DQS_N<3>	15C2
NC	69B	NC1		70B	DQS3	MEM_B_DQS_P<3>	15C2
	71B	VSS27		72B	VSS28		
15C4	MEM_B_DQ<27>	73B	DQ26	74B	DQ30	MEM_B_DQ<31>	15C4
15C4	MEM_B_DQ<25>	75B	DQ27	76B	DQ31	MEM_B_DQ<30>	15C4
	77B	VSS29		78B	VSS30		
30D6 14C4	MEM_CKE<2>	79B	CKE0	80B	NC/CKE1	MEM_CKE<3>	14C4 30D6
	81B	VDD0		82B	VDD1		
NC	83B	NC2		84B	NC/A15	MEM_B_A<15>	6D6
30A6 15D2	MEM_B_BS<2>	85B	BA2	86B	NC/A14	MEM_B_A<14>	6D6
	87B	VDD2		88B	VDD3		
30B6 15B2	MEM_B_A<12>	89B	A12	90B	A11	MEM_B_A<11>	15B2 30B6
30B6 15B2	MEM_B_A<9>	91B	A9	92B	A7	MEM_B_A<7>	15B2 30B6
30B6 15B2	MEM_B_A<8>	93B	A8	94B	A6	MEM_B_A<6>	15B2 30B6
	95B	VDD4		96B	VDD5		
30B6 15B2	MEM_B_A<5>	97B	A5	98B	A4	MEM_B_A<4>	15B2 30B6
30B6 15B2	MEM_B_A<3>	99B	A3	100B	A2	MEM_B_A<2>	15C2 30B6
30B6 15C2	MEM_B_A<1>	101B	A1	102B	A0	MEM_B_A<0>	15C2 30B6
	103B	VDD6		104B	VDD7		
30B6 15B2	MEM_B_A<10>	105B	A10/AP	106B	BA1	MEM_B_BS<1>	15D2 30A6
30A6 15D2	MEM_B_BS<0>	107B	BA0	108B	RAS*	MEM_B_RAS_L	15B2 30A6
30A6 15B2	MEM_B_WE_L	109B	WE*	110B	S0*	MEM_CS_L<2>	14C4 30D6
	111B	VDD8		112B	VDD9		
30A6 15D2	MEM_B_CAS_L	113B	CAS*	114B	ODT0	MEM_ODT<2>	14C4 30C6
30D6 14C4	MEM_CS_L<3>	115B	NC/S1*	116B	NC/A13	MEM_B_A<13>	15B2 30B6
	117B	VDD10		118B	VDD11		
30C6 14C4	MEM_ODT<3>	119B	NC/ODT1	120B	NC3	NC	
	121B	VSS31		122B	VSS32		
15B4	MEM_B_DQ<36>	123B	DQ32	124B	DQ36	MEM_B_DQ<32>	15C4
15C4	MEM_B_DQ<33>	125B	DQ33	126B	DQ37	MEM_B_DQ<37>	15B4
	127B	VSS33		128B	VSS34		
15C2	MEM_B_DQS_N<4>	129B	DQS4*	130B	DM4	MEM_B_DM<4>	15C2
15C2	MEM_B_DQS_P<4>	131B	DQS4	132B	VSS35		
	133B	VSS36		134B	DQ38	MEM_B_DQ<38>	15B4
15B4	MEM_B_DQ<34>	135B	DQ34	136B	DQ39	MEM_B_DQ<39>	15B4
15B4	MEM_B_DQ<35>	137B	DQ35	138B	VSS37		
	139B	VSS38		140B	DQ44	MEM_B_DQ<44>	15B4
15B4	MEM_B_DQ<40>	141B	DQ40	142B	DQ45	MEM_B_DQ<45>	15B4
15B4	MEM_B_DQ<41>	143B	DQ41	144B	VSS39		
	145B	VSS40		146B	DQS5*	MEM_B_DQS_N<5>	15C2
15C2	MEM_B_DM<5>	147B	DM5	148B	DQS5	MEM_B_DQS_P<5>	15C2
	149B	VSS41		150B	VSS42		
15B4	MEM_B_DQ<42>	151B	DQ42	152B	DQ46	MEM_B_DQ<46>	15B4
15B4	MEM_B_DQ<43>	153B	DQ43	154B	DQ47	MEM_B_DQ<47>	15B4
	155B	VSS43		156B	VSS44		
15A4	MEM_B_DQ<62>	157B	DQ48	158B	DQ52	MEM_B_DQ<58>	15B4
15B4	MEM_B_DQ<59>	159B	DQ49	160B	DQ53	MEM_B_DQ<63>	15A4
	161B	VSS45		162B	VSS46		
NC	163B	NC_TEST		164B	CK1	MEM_CLK_P<2>	14D4
	165B	VSS47		166B	CK1*	MEM_CLK_N<2>	14D4
15C2	MEM_B_DQS_N<7>	167B	DQS6*	168B	VSS48		
15C2	MEM_B_DQS_P<7>	169B	DQS6	170B	DM6	MEM_B_DM<7>	15C2
	171B	VSS49		172B	VSS50		
15A4	MEM_B_DQ<60>	173B	DQ50	174B	DQ54	MEM_B_DQ<56>	15B4
15A4	MEM_B_DQ<61>	175B	DQ51	176B	DQ55	MEM_B_DQ<57>	15B4
	177B	VSS51		178B	VSS52		
15B4	MEM_B_DQ<54>	179B	DQ56	180B	DQ60	MEM_B_DQ<55>	15B4
15B4	MEM_B_DQ<51>	181B	DQ57	182B	DQ61	MEM_B_DQ<50>	15B4
	183B	VSS53		184B	VSS54		
15C2	MEM_B_DM<6>	185B	DM7	186B	DQS7*	MEM_B_DQS_N<6>	15C2
	187B	VSS55		188B	DQS7	MEM_B_DQS_P<6>	15C2
15B4	MEM_B_DQ<52>	189B	DQ58	190B	VSS56		
15B4	MEM_B_DQ<49>	191B	DQ59	192B	DQ62	MEM_B_DQ<53>	15B4
	193B	VSS57		194B	DQ63	MEM_B_DQ<48>	15B4
65A3 29A3 28A6	=PPSPD_S0_MEM			196B	VSS58	Resistor prevents pwr-gnd short	
27C6	=I2C_SODIMMB_SDA	195B	SDA	198B	SA0		
27C6	=I2C_SODIMMB_SCL	197B	SCL	200B	SA1	SODIMM_A_SA1	
		199B	VDDSPD			ADDR=0xA4(WR)/0xA5(RD)	

516-0140

202 NC

=PP1V8_S3_MEM 28B2 28D3 28D6 29B2 29D6 65B6

=PPSPD_S0_MEM 28A6 29A6 65A3

R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

65B6 29D6 29D3 28D6 28D3 28B2 =PP1V8_S3_MEM

C2908 10UF 20% 5.3V XSR 603

C2909 10UF 20% 6.3V XSR 603

C2910 1UF 10% 6.3V CERM 402

C2911 0.1uF 20% 10V CERM 402

C2912 1UF 10% 6.3V CERM 402

C2913 1UF 10% 6.3V CERM 402

C2914 1UF 10% 6.3V CERM 402

C2915 1UF 10% 6.3V CERM 402

C2916 1UF 10% 6.3V CERM 402

C2917 0.1uF 20% 10V CERM 402

C2918 0.1uF 20% 10V CERM 402

C2919 0.1uF 20% 10V CERM 402

C2920 0.1uF 20% 10V CERM 402

C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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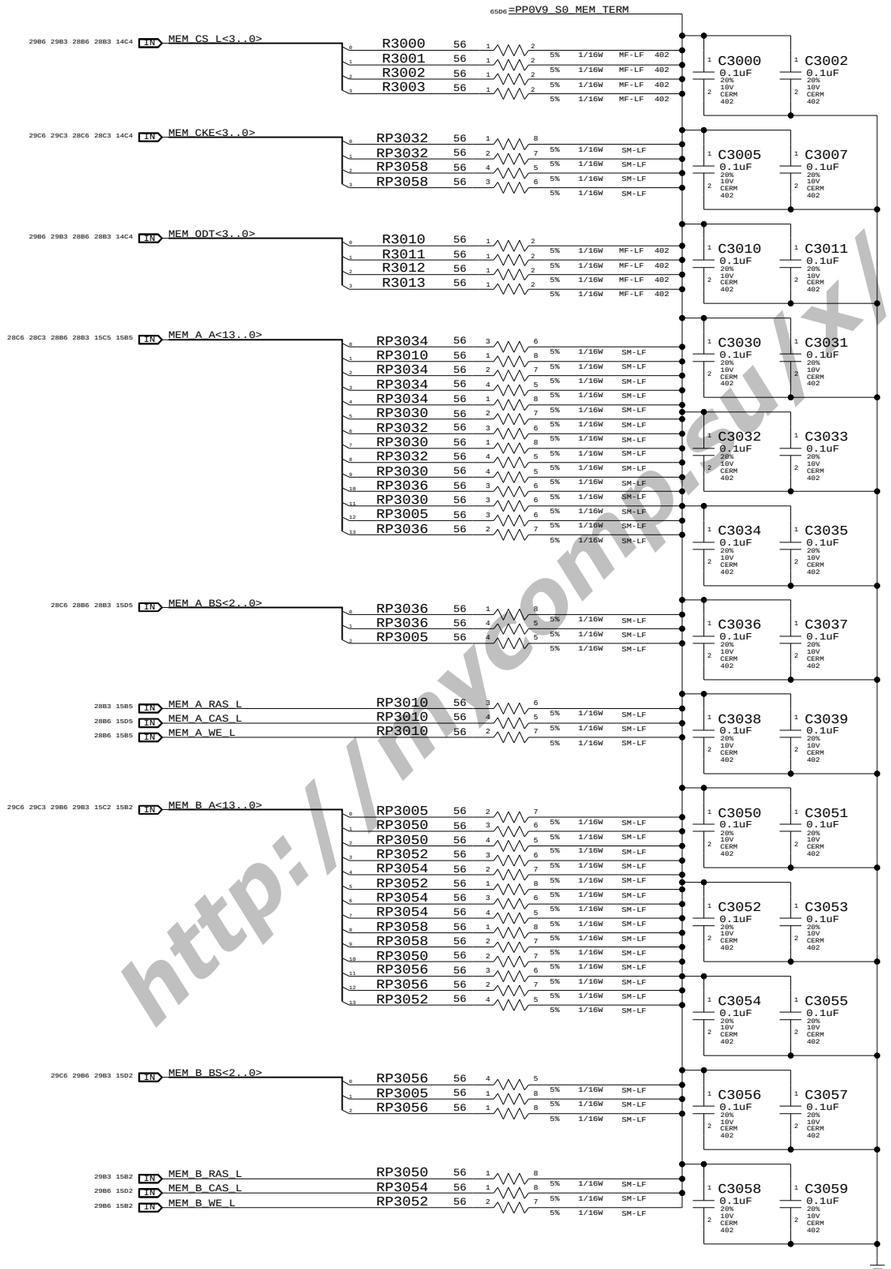
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 30 OF 84	

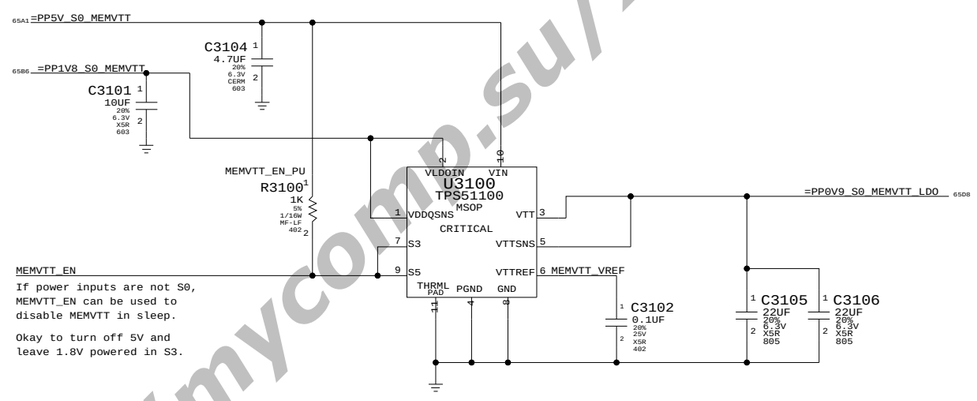
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



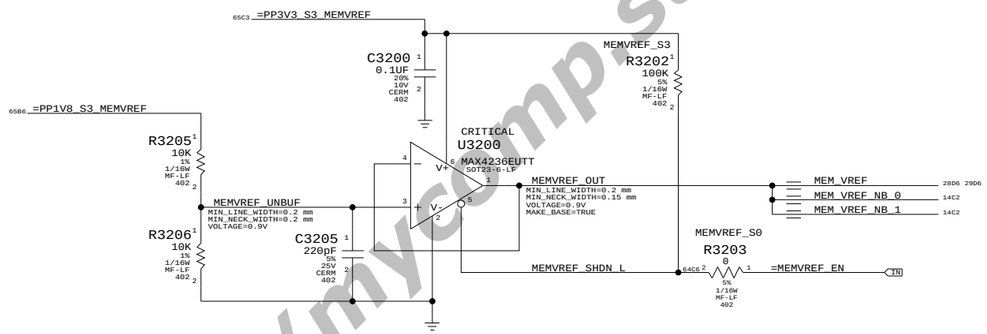
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 31 OF 84

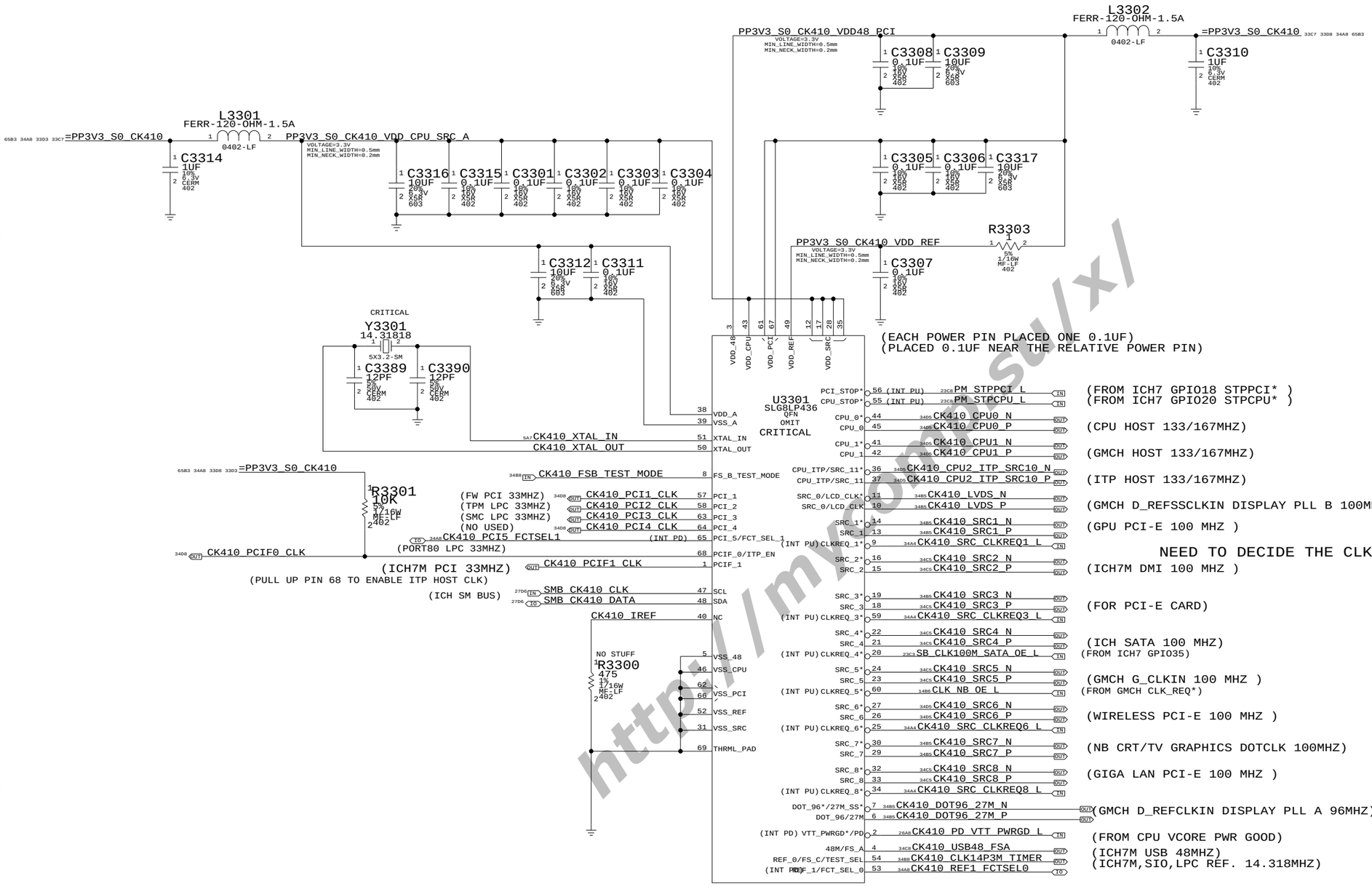


DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 32 OF 84	



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

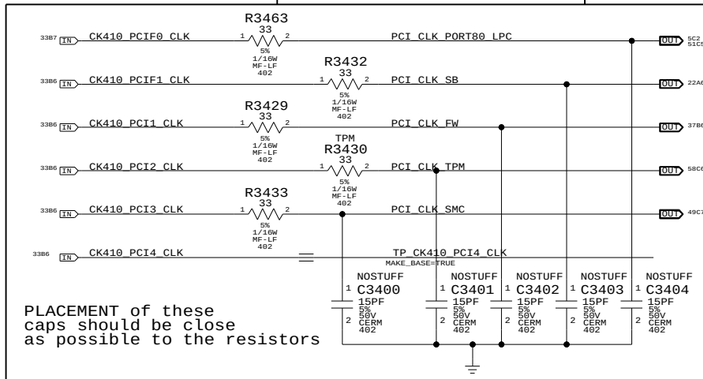
CLOCKS

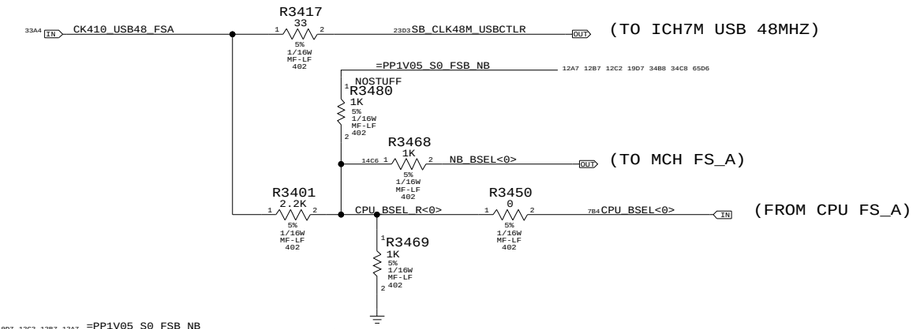
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

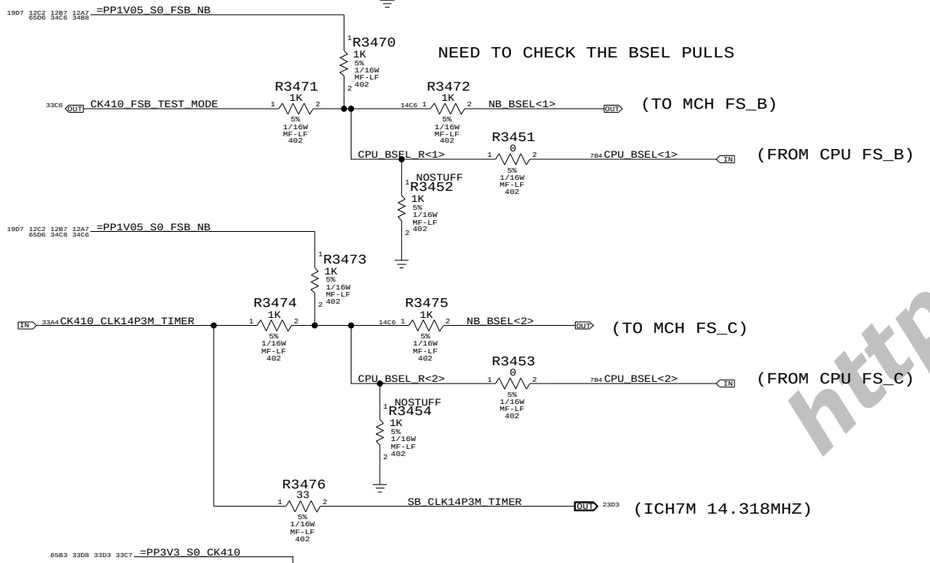
APPLE COMPUTER INC.

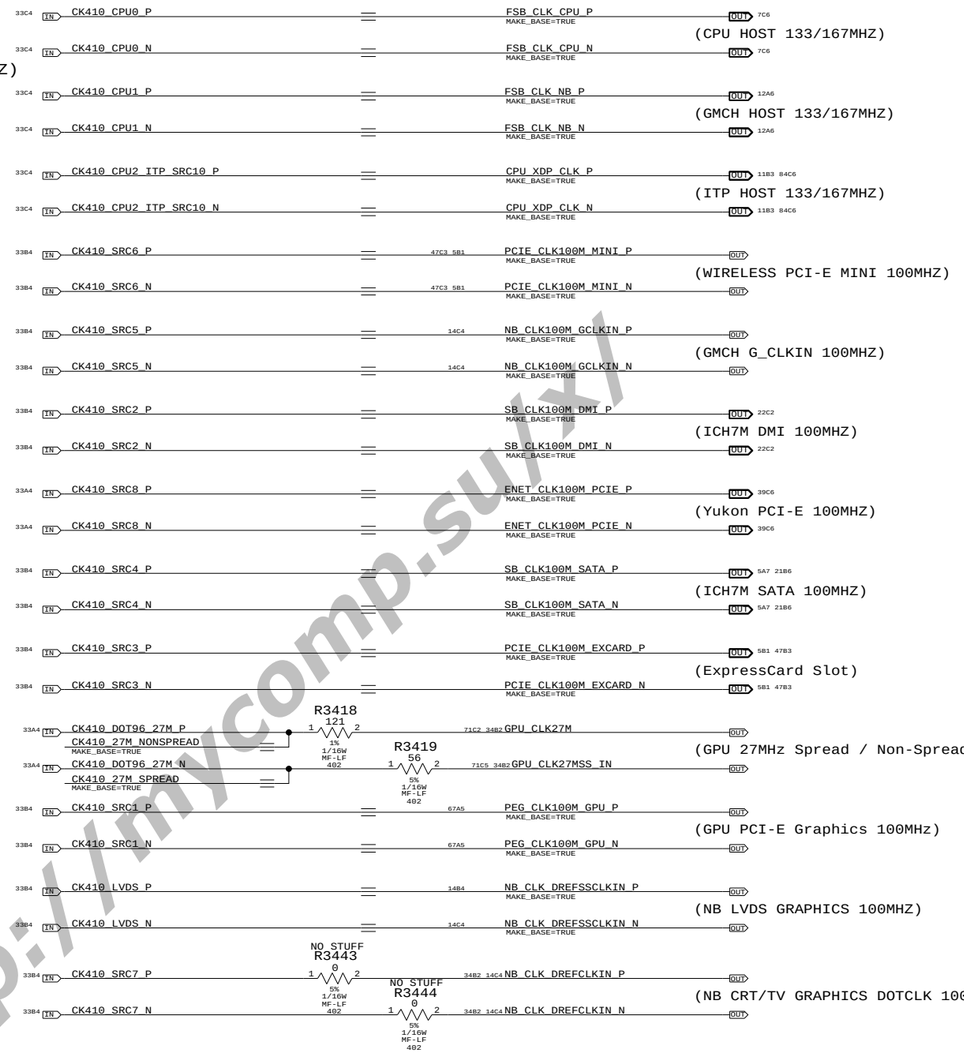
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

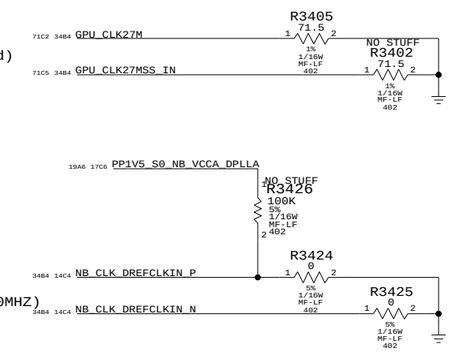
SCALE NONE SHT 33 OF 84







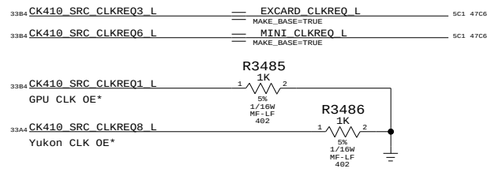




NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED



Clock Termination

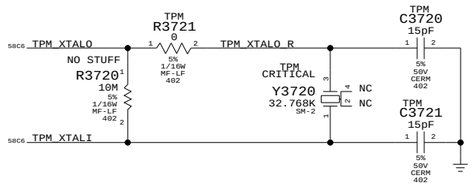
SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

APPLE COMPUTER INC.

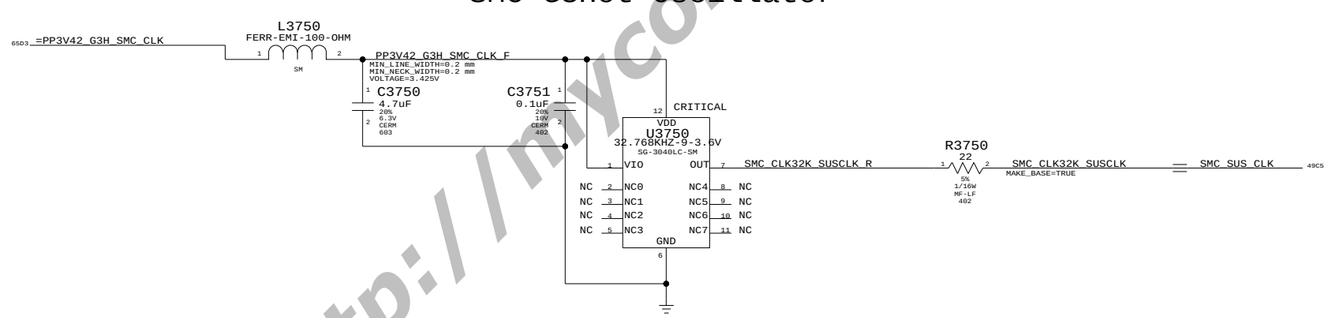
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 34 OF 84

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

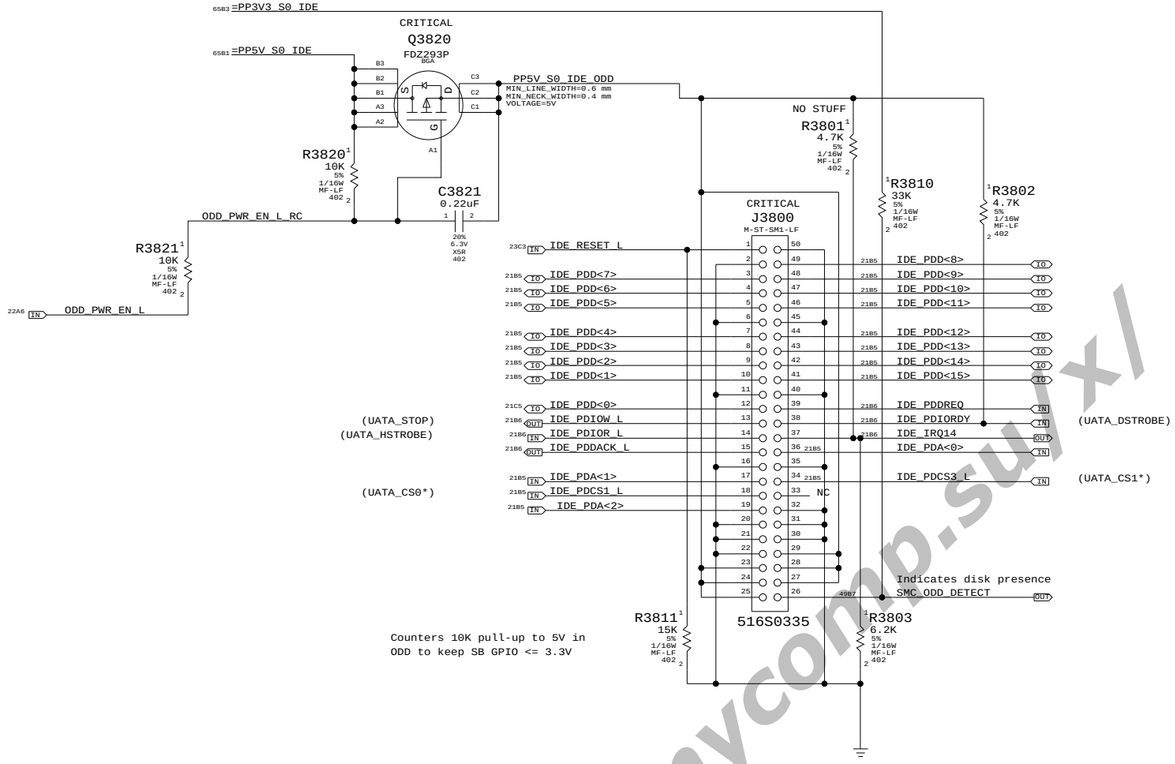
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

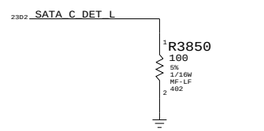
APPLE COMPUTER INC.

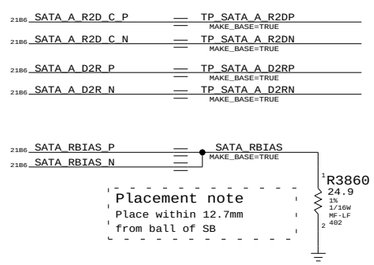
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	35	84

IDE (ODD) Connector







PATA Connector

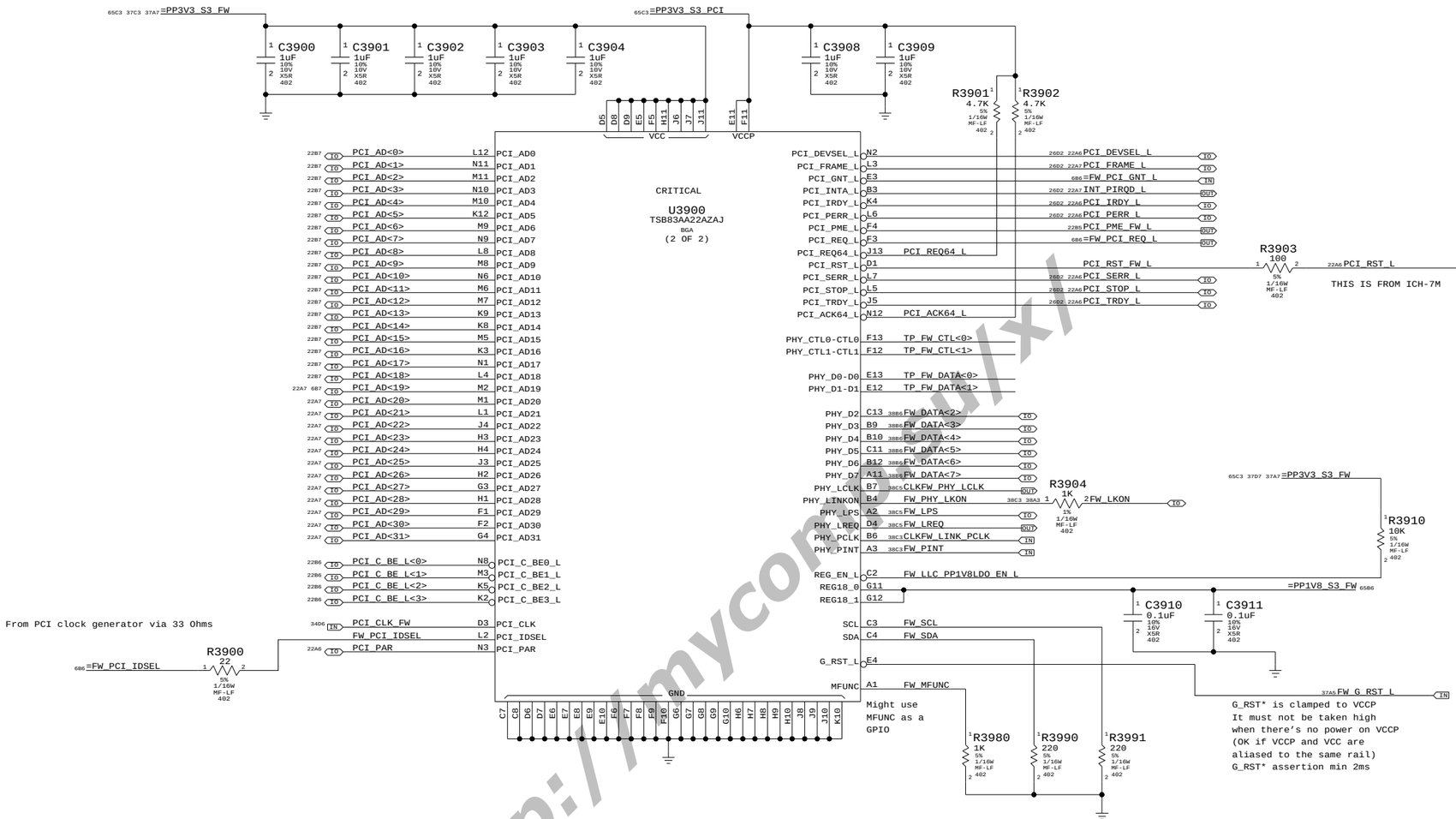
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE

SHT 36 OF 84

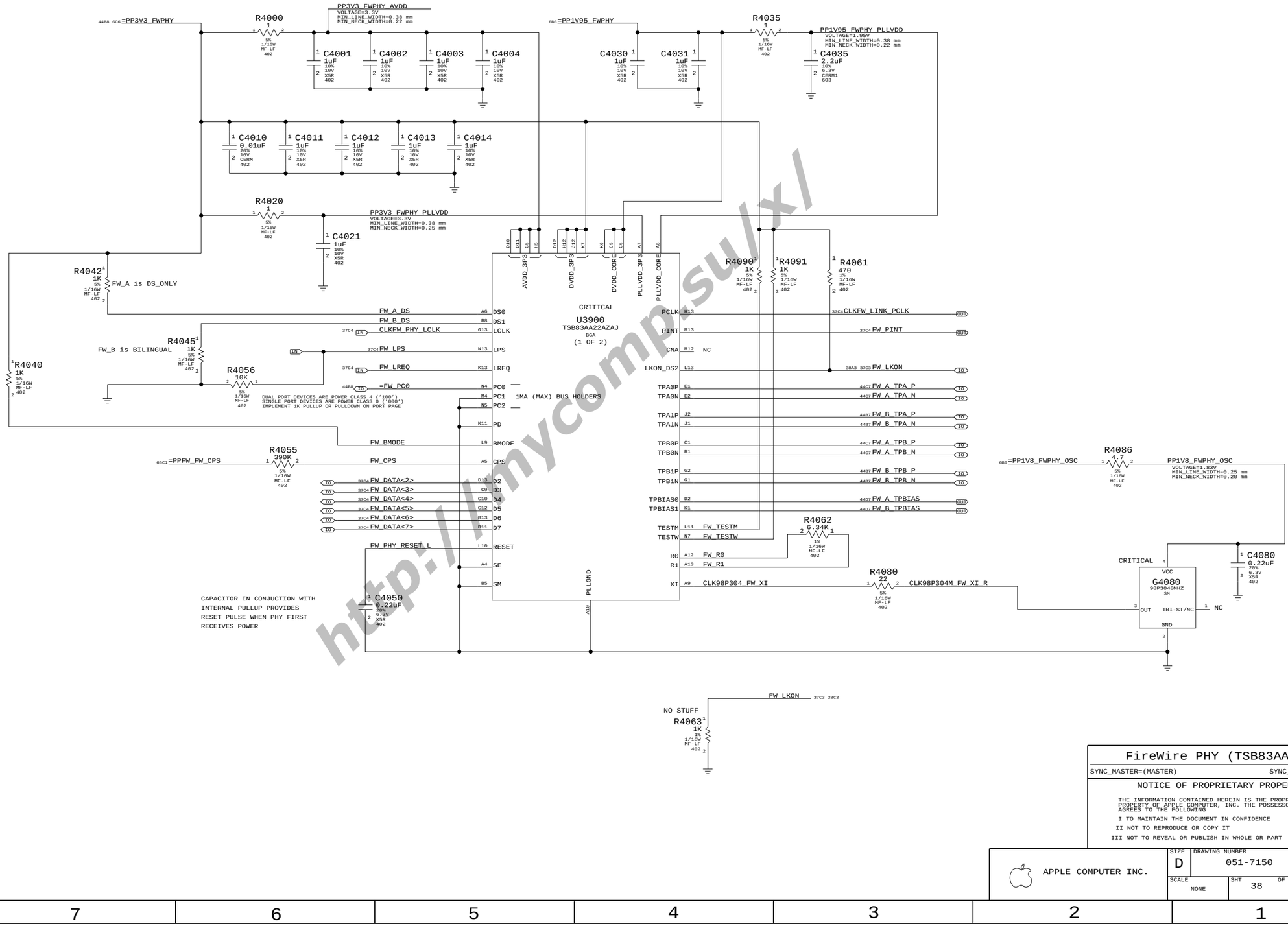


FireWire Link (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 37 OF 84	



FireWire PHY (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 38 OF 84	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

L4100
FERR-120-OHM-1.5A
0402-LF

=PP2V5_S3_ENET 65B6

40D5 =PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

PLACE C4107 NEAR U4101 AVDD

39D5 39A3 39A4 39B4 39B8 65D1 =PP3V3_S3_ENET

=PP1V2_S3_ENET 39A8 65D6

=PP3V3_S3_ENET 39D8 65D1 39A5 39B4 39B5 39B8

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P 1 2 22D4 PCIE_A_D2R_P OUT
PCIE_A_D2R_C_N 1 2 22D4 PCIE_A_D2R_N OUT

C4111 0.1UF 10% 16V X5R 402

C4112 0.1UF X5R 10% 16V 402

PCIE_A_R2D_P 1 2 22D4 PCIE_A_R2D_C_P IN
PCIE_A_R2D_N 1 2 22D4 PCIE_A_R2D_C_N IN

C4113 0.1UF 402 X5R 16V 10%

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

VDD7 58
VDD6 48
VDD5 44
VDD4 39
VDD3 33
VDD2 13
VDD1 7
VDD0 2
VDDQ_TTL4 61
VDDQ_TTL3 45
VDDQ_TTL2 40
VDDQ_TTL1 8
VDDQ_TTL0 1
AVDD 23
AVDDL6 57
AVDDL5 52
AVDDL4 51
AVDDL3 32
AVDDL2 28
AVDDL1 22
AVDDL0 19
VDD25 64

39B7 ENET_LOM_DIS_L 10 LOM_DISABLE*
12 VAUX_AVLBL
64C6 =ENET_VMAIN_AVLBL 47 VMAIN_AVLBL
NC 11 SWITCH_VCC
NC 9 SWITCH_VAUX
NC 24 HSDACP
NC 25 HSDACN

OMIT
CRITICAL
U4101
88E8053
QFN

ANALOG

OPTIONAL EXTERNAL LDO

OUT 6D4 ENET_CTRL25 4 CTRL25
OUT 6D4 ENET_CTRL12 3 CTRL12
ENET_RSET 16 RSET

R4102 4.87K 1% 1/10W MF-LF 402

NO PULL-UP NEEDED

NC 59 LED_ACT*
NC 60 LED_LINK10/100*
NC 62 LED_LINK1000*
NC 63 LINK*

LED

29 TSTPT
46 TESTMODE

TEST

PCI EXPRESS

TX_P 49
TX_N 50
RX_P 54
RX_N 53
REFCLKP 55 34C3 ENET_CLK100M_PCIE_P IN
REFCLKN 56 34C3 ENET_CLK100M_PCIE_N IN
WAKE* 6 47C3 23C8 5B1 PCIE_WAKE_L OUT
PERST* 5 26B1 ENET_RST_L IN

MEDIA

MDIP0 17
MDIN0 18
MDIP1 20
MDIN1 21
MDIP2 26
MDIN2 27
MDIP3 30
MDIN3 31

40D4 ENET_MDI_P<0> IO
40C4 40B7 ENET_MDI_N<0> IO
40C4 ENET_MDI_P<1> IO
40C4 40A7 ENET_MDI_N<1> IO
40C4 ENET_MDI_P<2> IO
40C4 ENET_MDI_N<2> IO
40C4 ENET_MDI_P<3> IO
40B4 ENET_MDI_N<3> IO

TWSI

VPD_CLK 38 ENET_VPD_CLK 39A2
VPD_DATA 41 ENET_VPD_DATA 39A2

TEST

PU_VDDO_TTL0 42 ENET_PU_VDD_TTL0 39A6
PU_VDDO_TTL1 43 ENET_PU_VDD_TTL1 39A6

ASF IS UNAVAILABLE ON 8053

SPI

SPI_DI 35 NC
SPI_DO 34 NC
SPI_CLK 37 NC
SPI_CS 36 NC

INTERNAL PULL-UP

MAIN CLK

XTALI 15
XTALO 14 ENET_XTALO

CRITICAL
ENET_XTALI

Y4101
SM-3.2X2.5MM
25.0000M

C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO
TRACE LENGTH <12MIL

2. DO NOT ROUTE UNDER CRYSTAL

THRML_PAD 65

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0 VOLTAGE=1.234V
ENET_MDI1 VOLTAGE=1.234V
ENET_MDI2 VOLTAGE=1.234V
ENET_MDI3 VOLTAGE=1.234V

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

Setting attribute VOLTAGE
to arbitrary value
to help constraint manager
find correct topolgy

PLACE RESISTORS CLOSE TO U4101

65D1 39D8 39D6 39B5 39B4 39A5 =PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

ENET_LOM_DIS_L 39C8

Q4100 2N7002 SOT23-LF

6C4 ENET_LOWPWR_EN

R4132 100K 5% 1/16W MF-LF 402

=PP3V3_S3_ENET 39A5 39B4 39B8 39D6 39D8 65D1

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

39C6 ENET_PU_VDD_TTL0
39B6 ENET_PU_VDD_TTL1

65D1 39D8 39D6 39B8 39B5 39A5 =PP3V3_S3_ENET

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL

R4122 10K 5% 1/16W MF-LF 402
R4123 10K 5% 1/16W MF-LF 402

U4102
M24C08
SO8

VCC 8
E2 3
NC1 2
NC0 1
WC* 7
VSS 4
SDA 5
SCL 6

ENET_VPD_DATA 39C6
ENET_VPD_CLK 39C6

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

65D6 39D7 =PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

65D1 39D8 39D6 39B8 39B5 39B4 =PP3V3_S3_ENET

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 39 OF 84	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 40D3
	ENETCONN	ENET_100D	ENETCONN_N<0> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<3> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<3> 40B3

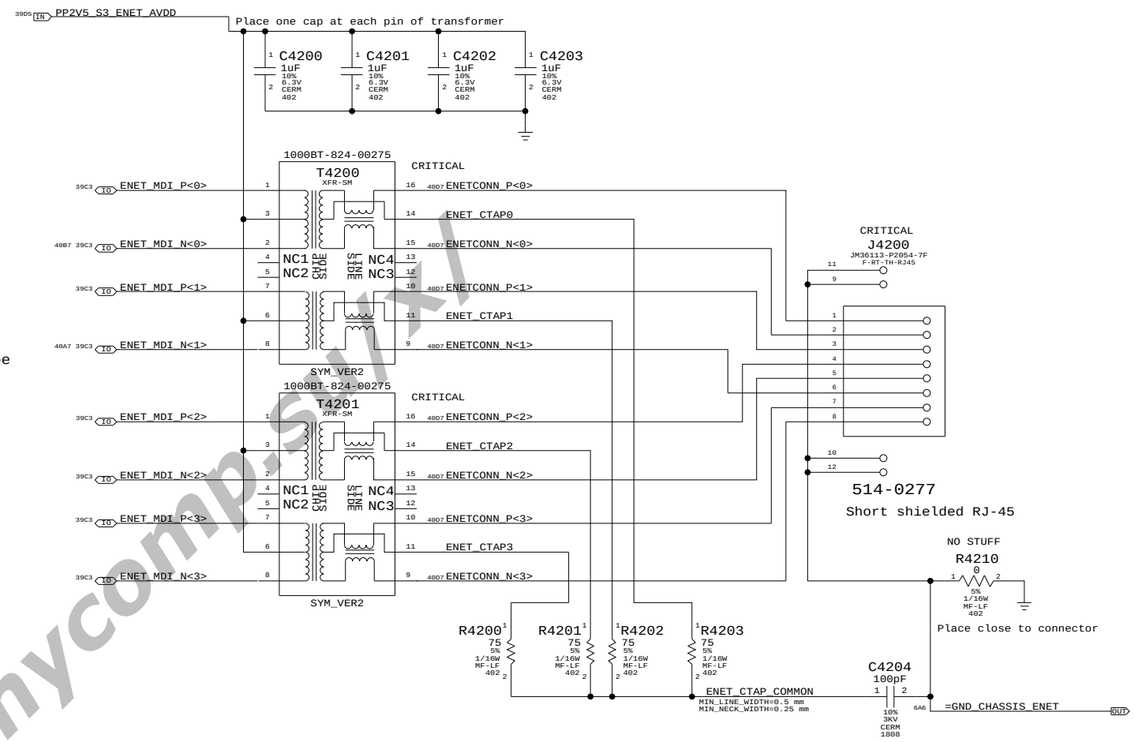
Page Notes

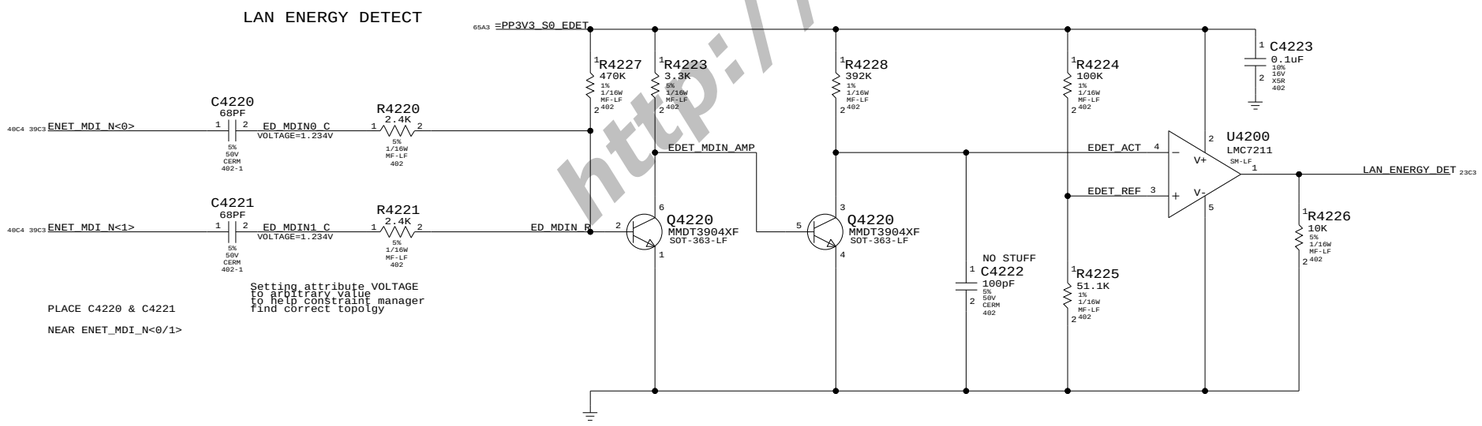
Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board





Ethernet Connector

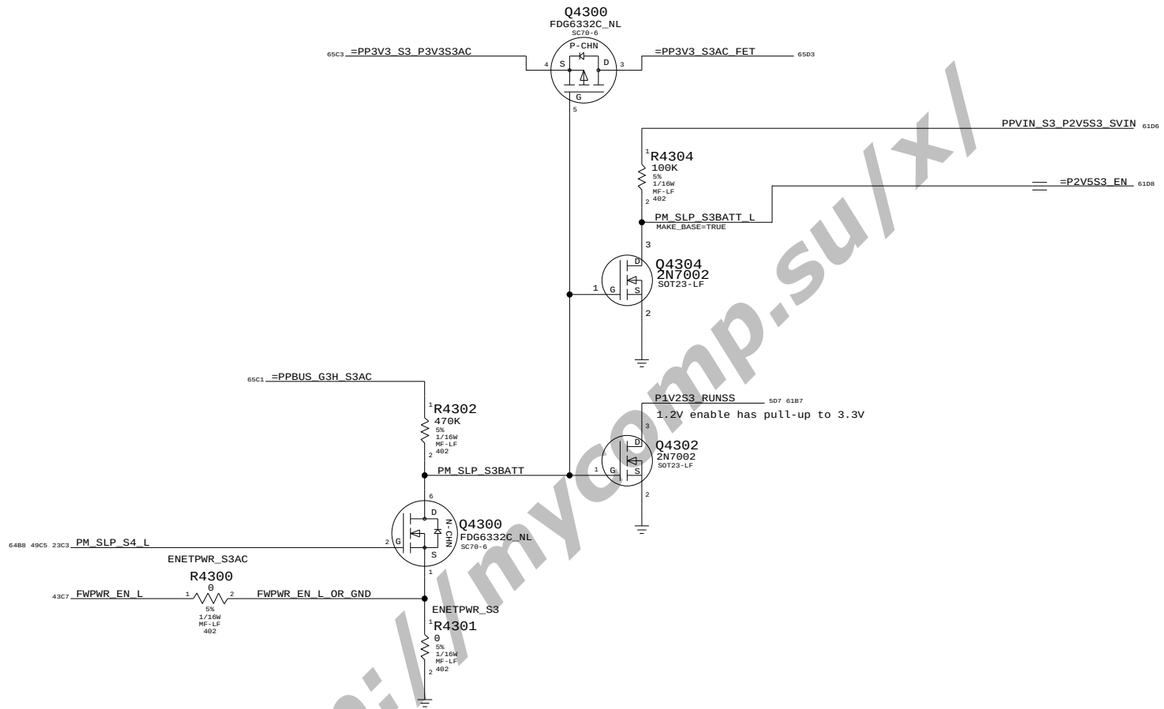
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 40 OF 84	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

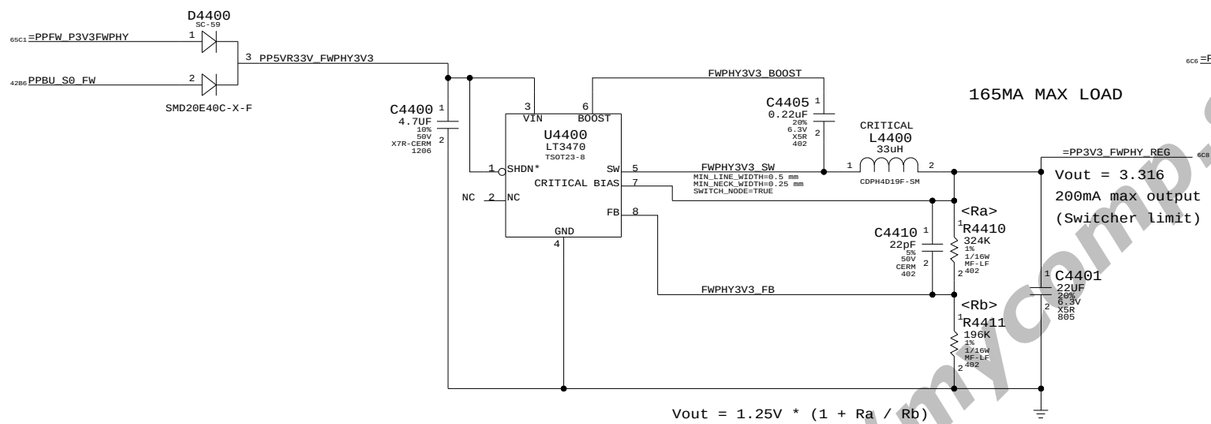
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

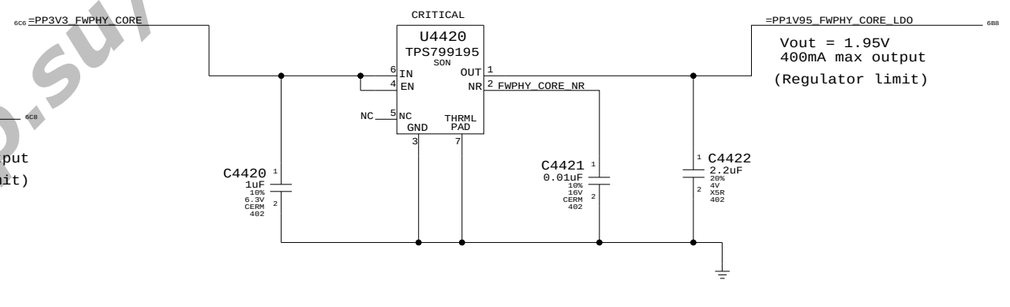
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	41	84

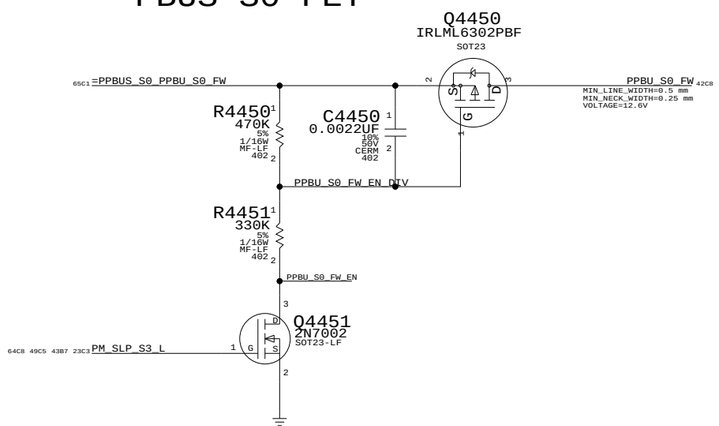
3.3V Supply for FWPHY



1.95V Supply for FW PHY



PBUS S0 FET



FW PHY Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	42	84

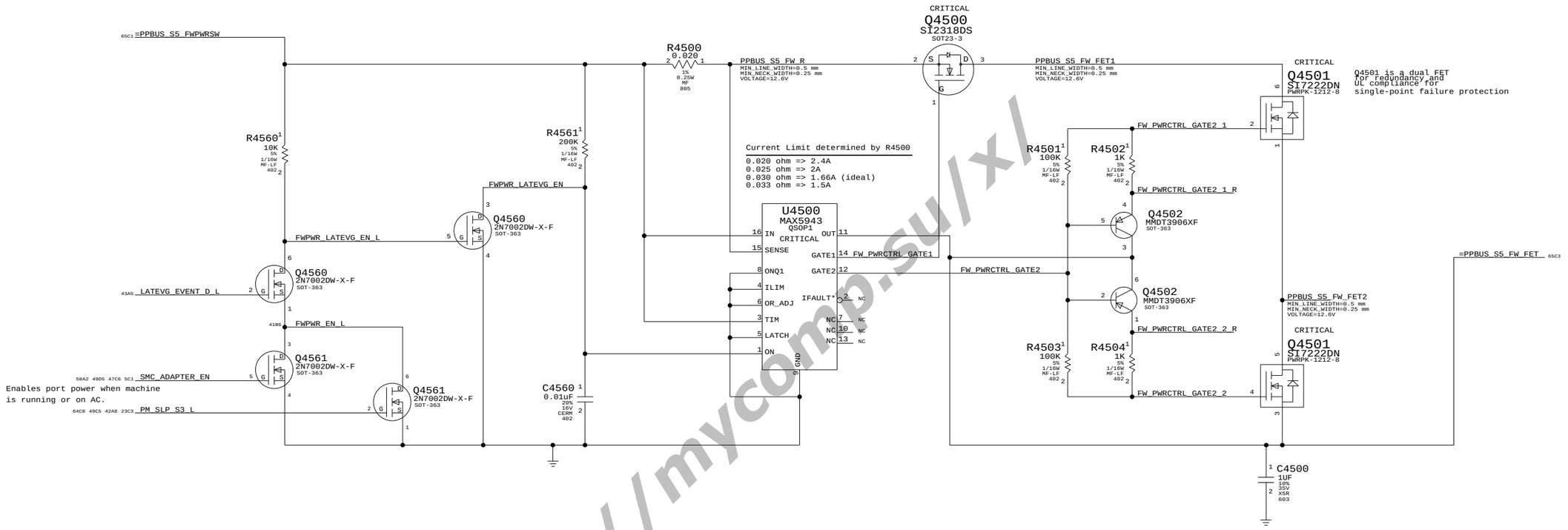
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

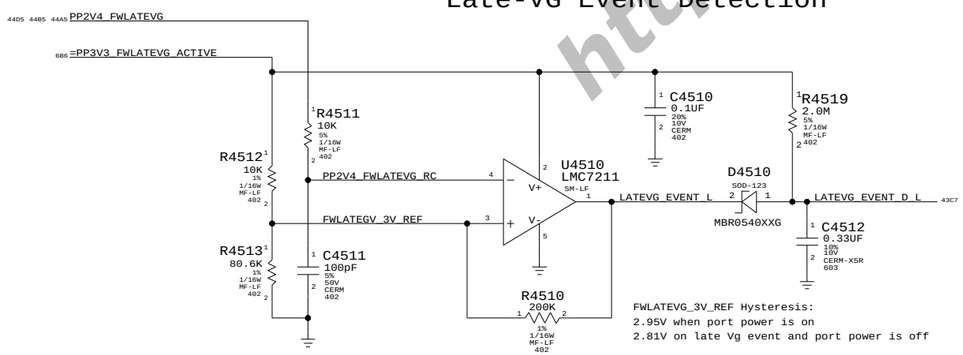
Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Current Limit/Active Late-VG Protection



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 43 OF 84	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED	FW	FW_110D	FW_PORT1_TPA_P	44B5 44C5
	FW	FW_110D	FW_PORT1_TPA_N	44B5 44C5
	FW	FW_110D	FW_PORT1_TPB_P	44B5 44C5
BY	FW	FW_110D	FW_PORT1_TPB_N	44B5 44C5
	FW	FW_110D	FW_PORT2_TPA_FL_P	44B2
PHY	FW	FW_110D	FW_PORT2_TPA_FL_N	44B2
	FW	FW_110D	FW_PORT2_TPB_FL_P	44B2
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_N	44B2

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

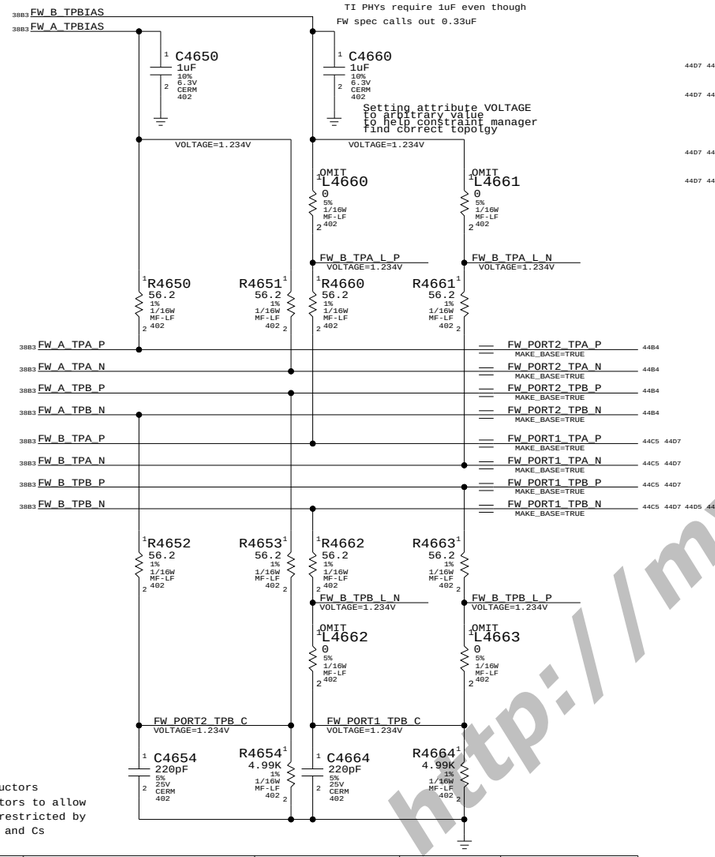
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

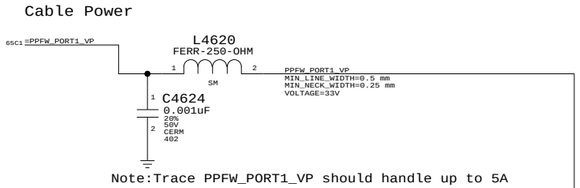
Place close to FireWire PHY



Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

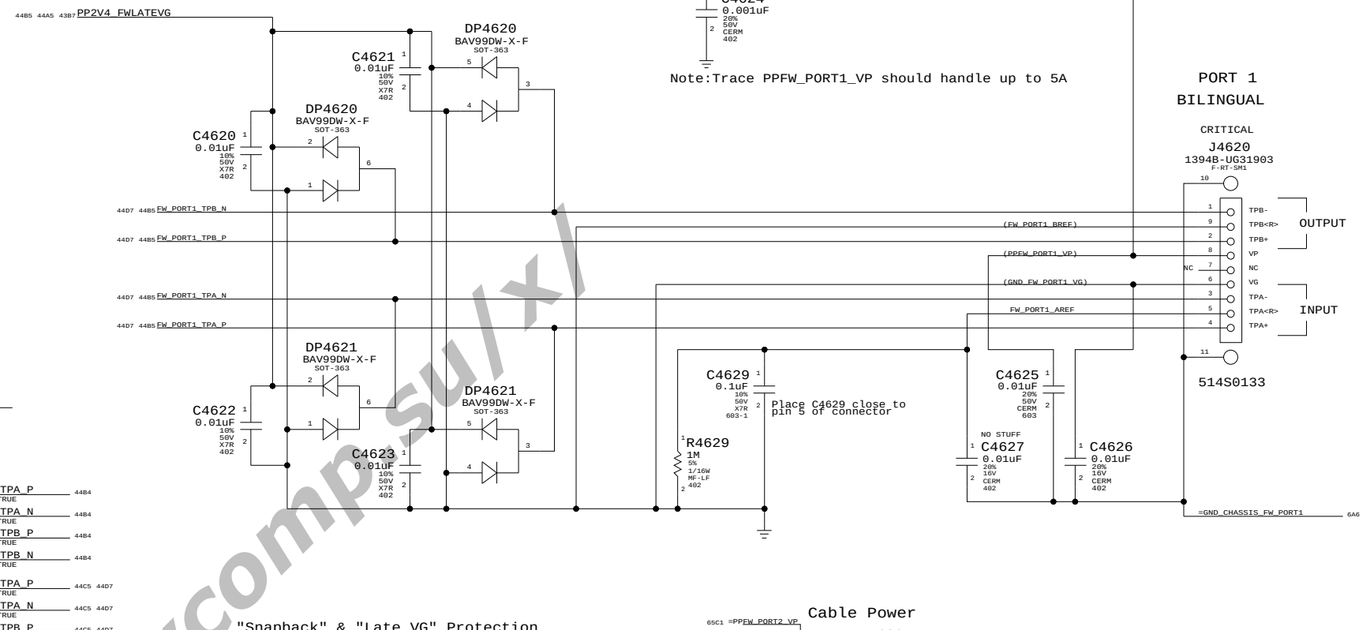
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

Cable Power



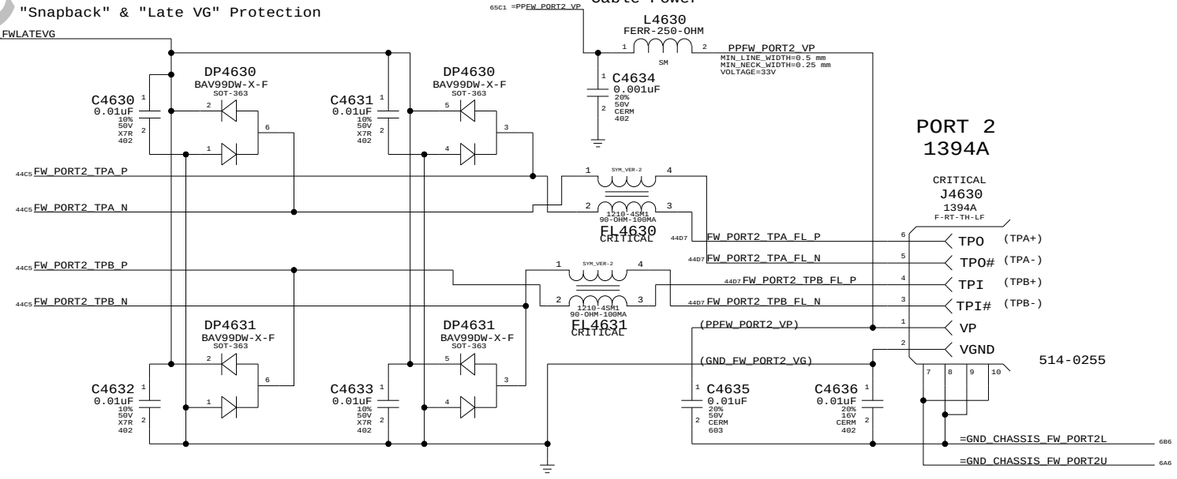
Note:Trace PPFW_PORT1_VP should handle up to 5A

"Snapback" & "Late VG" Protection

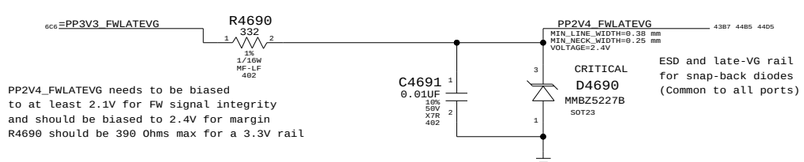


Cable Power

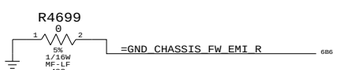
"Snapback" & "Late VG" Protection



Late-VG Protection Power



PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail



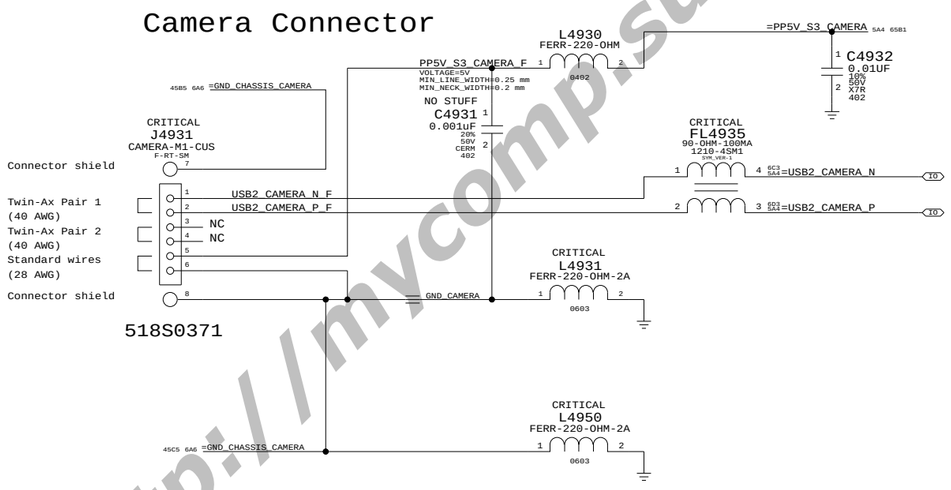
FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 44 OF 84	

Camera Connector



Camera Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

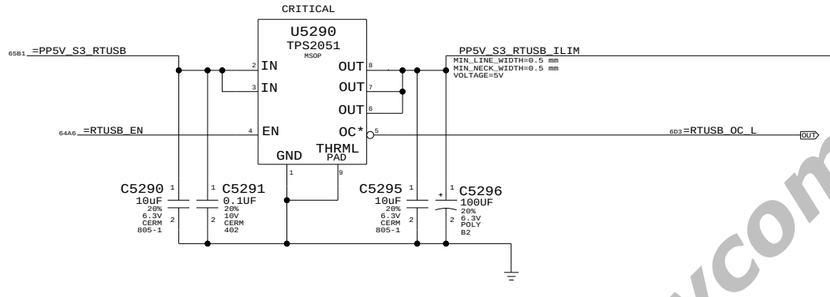
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

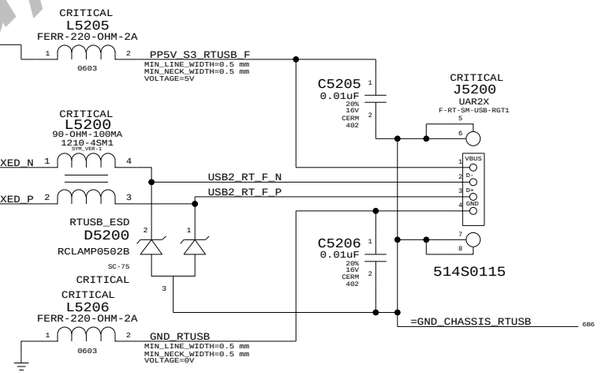
SCALE: NONE

SHT 45 OF 84

Port Power Switch

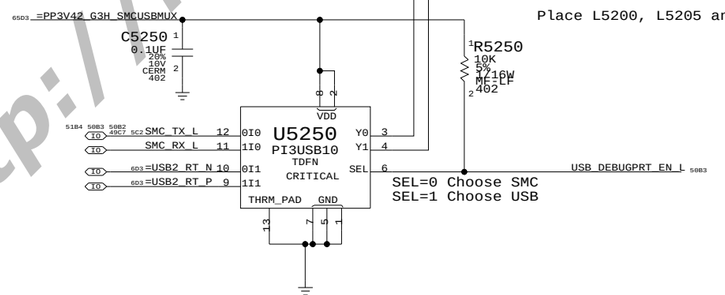


Right USB Port



Place L5200, L5205 and L5206 across moat

USB/SMC Debug Mux



External USB Connector

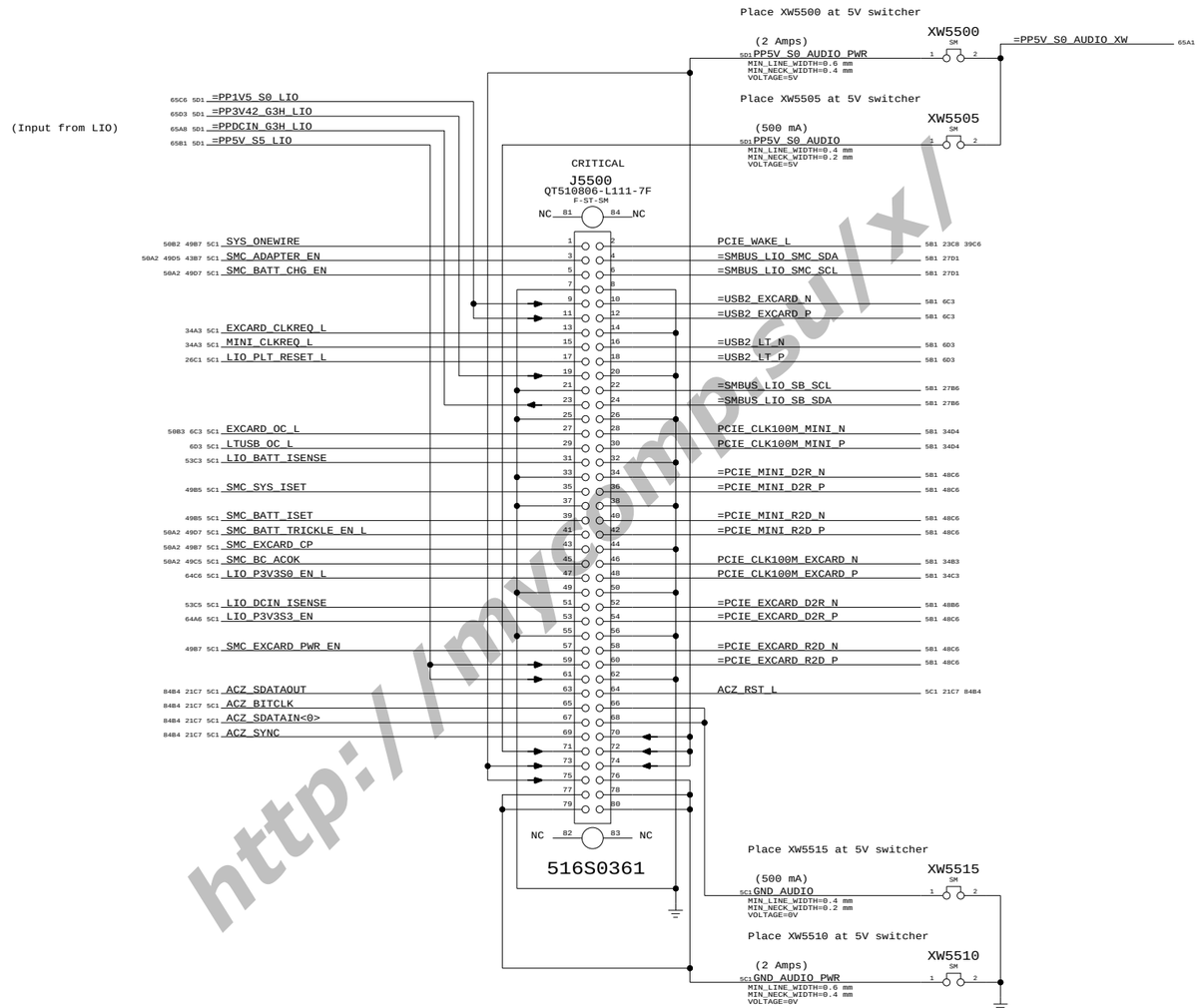
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	46	84

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	47	84

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

47B3 5B1	=PCIE_MINI_R2D_P	PCIE_MINI_R2D_C_P	MAKE_BASE=TRUE	PCIE_B_R2D_C_P	22D4
47B3 5B1	=PCIE_MINI_R2D_N	PCIE_MINI_R2D_C_N	MAKE_BASE=TRUE	PCIE_B_R2D_C_N	22D4
47C3 5B1	=PCIE_MINI_D2R_P	PCIE_MINI_D2R_P	MAKE_BASE=TRUE	PCIE_B_D2R_P	22D4
47C3 5B1	=PCIE_MINI_D2R_N	PCIE_MINI_D2R_N	MAKE_BASE=TRUE	PCIE_B_D2R_N	22D4

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

47B3 5B1	=PCIE_EXCARD_R2D_P	PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	PCIE_C_R2D_C_P	22D4
47B3 5B1	=PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	PCIE_C_R2D_C_N	22D4
47B3 5B1	=PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	PCIE_C_D2R_P	22D4
47B3 5B1	=PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	PCIE_C_D2R_N	22D4

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP	MAKE_BASE=TRUE	PCIE_D_R2D_C_P	22D4
TP_PCIE_D_R2DN	MAKE_BASE=TRUE	PCIE_D_R2D_C_N	22D4
TP_PCIE_D_D2RP	MAKE_BASE=TRUE	PCIE_D_D2R_P	22D4
TP_PCIE_D_D2RN	MAKE_BASE=TRUE	PCIE_D_D2R_N	22D4

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP	MAKE_BASE=TRUE	PCIE_E_R2D_C_P	22C4
TP_PCIE_E_R2DN	MAKE_BASE=TRUE	PCIE_E_R2D_C_N	22C4
TP_PCIE_E_D2RP	MAKE_BASE=TRUE	PCIE_E_D2R_P	22C4
TP_PCIE_E_D2RN	MAKE_BASE=TRUE	PCIE_E_D2R_N	22C4

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP	MAKE_BASE=TRUE	PCIE_F_R2D_C_P	22C4
TP_PCIE_F_R2DN	MAKE_BASE=TRUE	PCIE_F_R2D_C_N	22C4
TP_PCIE_F_D2RP	MAKE_BASE=TRUE	PCIE_F_D2R_P	22C4
TP_PCIE_F_D2RN	MAKE_BASE=TRUE	PCIE_F_D2R_N	22C4

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 48 OF 84

UNUSED PINS HAVE THE FORMAT
SMC_XXX WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN
	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN
	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	SPI_ARB
	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	SPI_SCLK
	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	SPI_SI
	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	SPI_SO
	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L
	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	SMC_CPU_INIT_3_3_L
	SMC_P20	D13	P20	P70/AN0	N12	SMC_CPU_ISENSE
	SMC_P21	D14	P21	P71/AN1	R13	SMC_CPU_VSENSE
	SMC_P22	D15	P22	P72/AN2	P13	SMC_GPU_ISENSE
	SMC_P23	E12	P23	P73/AN3	R14	SMC_GPU_VSENSE
	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE
	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE
	SMC_P26	E13	P26	P76/AN6	N13	SMC_BATT_ISENSE
	SMC_P27	F14	P27	P77/AN7	P15	SMC_NB1V5_ISENSE
	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L
	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	SMC_TPM_GPIO
	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L
	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L
	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SC_TX_L
	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SC_RX_L
	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	SMB_BSB_CLK
	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	SMC_ONOFF_L
	SMC_XDP_TMS	A5	P40/TMIO	P91/IRQ1*	J2	SMC_BC_ACOK
	SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	SMC_BS_ALRT_L
	SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	PM_SLP_S3_L
	SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	PM_SLP_S4_L
	SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	PM_SLP_S5_L
	SMC_XDP_TCK	C2	P45	P96/EXCL	H1	SMC_SUS_CLK
	SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	SMB_0_S0_DATA
	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1			
	SMC_TX_L	G1	P50			
	SMC_RX_L	G4	P51			
	SMB_0_S0_CLK	F2	P52/SCL0			

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SMC_H8S2116
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	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	SMC_CASE_OPEN
	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	SMC_TCK
	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI
	SMC_USB_DEBUG_MUX	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO
	PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS
	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0
	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1
	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID
	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L
	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET
	SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	SMC_BATT_VSET
	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET
	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	SMC_SYS_VSET
	SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	SPI_CE_L
	SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3
	SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	SMB_BSA_DATA
	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	SMB_BSA_CLK
	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	SMB_A_S3_DATA
	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	SMB_A_S3_CLK
	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	SMB_B_S0_DATA
	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	SMB_B_S0_CLK
	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	SMC_PROCHOT
	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	SMC_THRMTRIP
	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	SMC_FWE
	SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	ALS_GAIN
	SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	SMS_INT_L
	SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	SMS_ONOFF_L
	SMC_ANALOG_ID	N11	PD3/AN11			
	SMC_NB_ISENSE	P10	PD4/AN12			
	SMC_MEM_ISENSE	R10	PD5/AN13			
	ALS_LEFT	N10	PD6/AN14			
	ALS_RIGHT	M10	PD7/AN15			

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G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

65D3 50D7 50B1 49D4 49C2 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

65D3 50D7 50B1 49D3 49C2 =PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.35 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
PP3V3_AVREF_SMC 50B6
49D4 65D3 49D3 50D7 50B1 =PP3V3_S5_SMC
55C2 53D6 53C6 53C1 53B7 53B5 53B3 53B1 50B6 49B2 55C6 GND_SMC_AVSS

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

51B5 50D6 5C2	SMC_RST_L	E3	RES*		
50C8	SMC_XTAL	A2	XTAL		
50C8	SMC_EXTAL	B2	EXTAL		
				MD1	F2
				MD2	K1
				NMI	F4
				ETRST*	L1
				AVSS	P12
					R12

MD1 F2 — SMC_MD1 5C2 51B4
MD2 K1 — KBC_MDE
NMI F4 — 51B5 5C2 SMC_NMI
ETRST* L1 — 51B4 5C2 SMC_TRST_L
AVSS P12 R12 — VSS — D1 F4 R4 F12 F13 B13 A13 A4 B4 D2

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
R5898 10K 5% 1/16W MF-LF 402
NOSTUFF
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

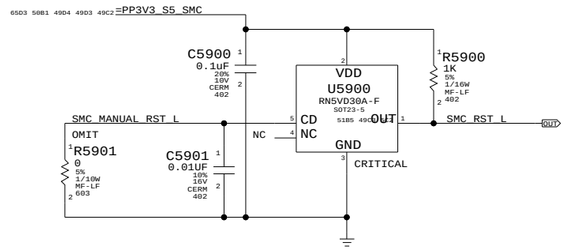
XW5800 SM
GND_SMC_AVSS 49C4 50B6 53B1 53B3 53B5 53B7 53C1 53C6 53D6 55C2 55C6

SMC

APPLE COMPUTER INC.

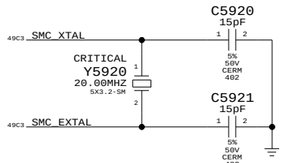
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 49 OF 84	

SMC Reset Button / Brownout Detect

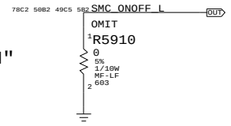


Silk: "SMC RST"

SMC Crystal Circuit

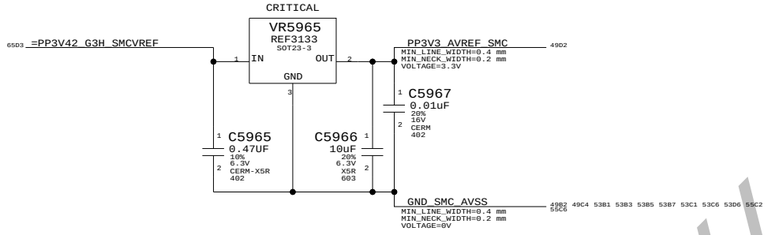


Debug Power Button

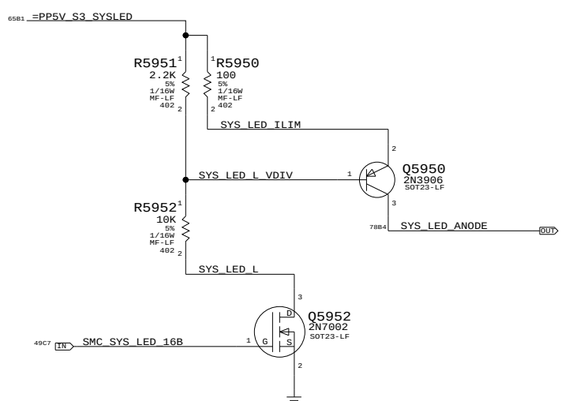


Silk: "PWR BTN"

SMC AVREF Supply

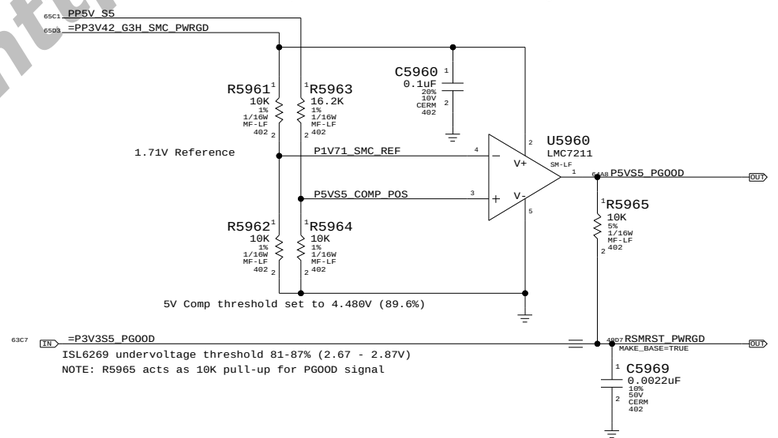


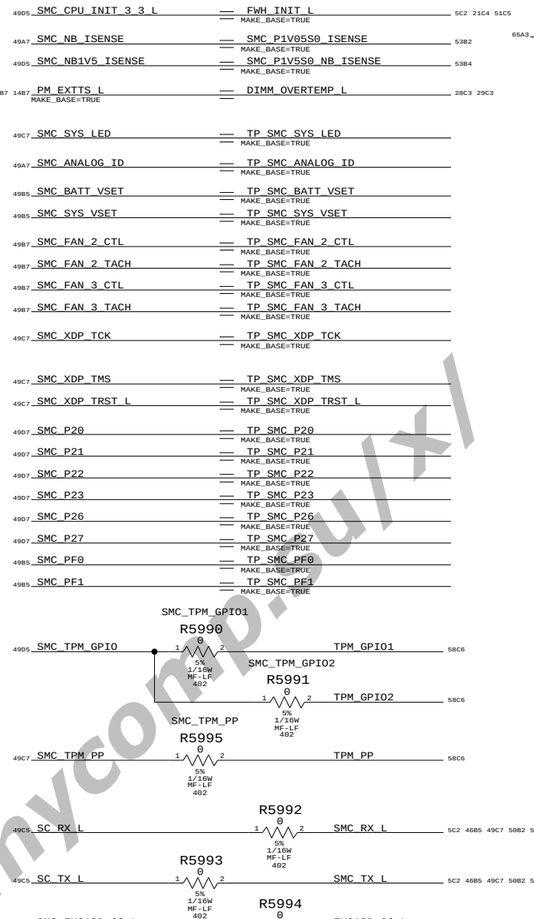
System (Sleep) LED Circuit



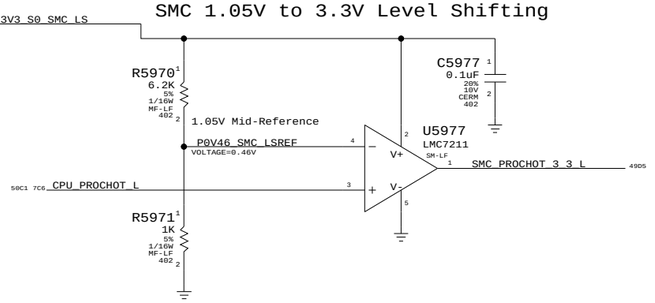
SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation

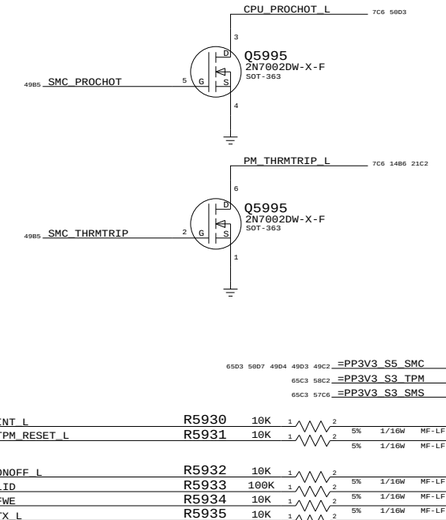


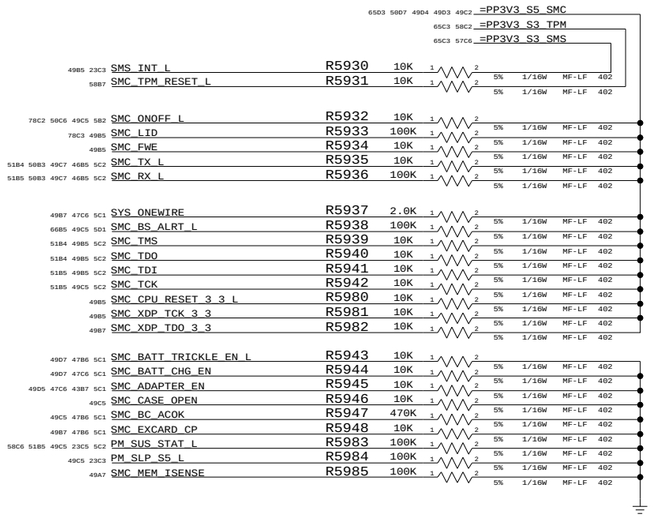


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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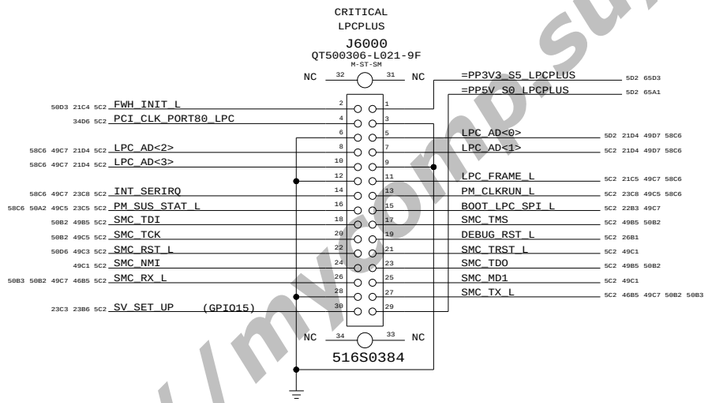
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 50 OF 84	



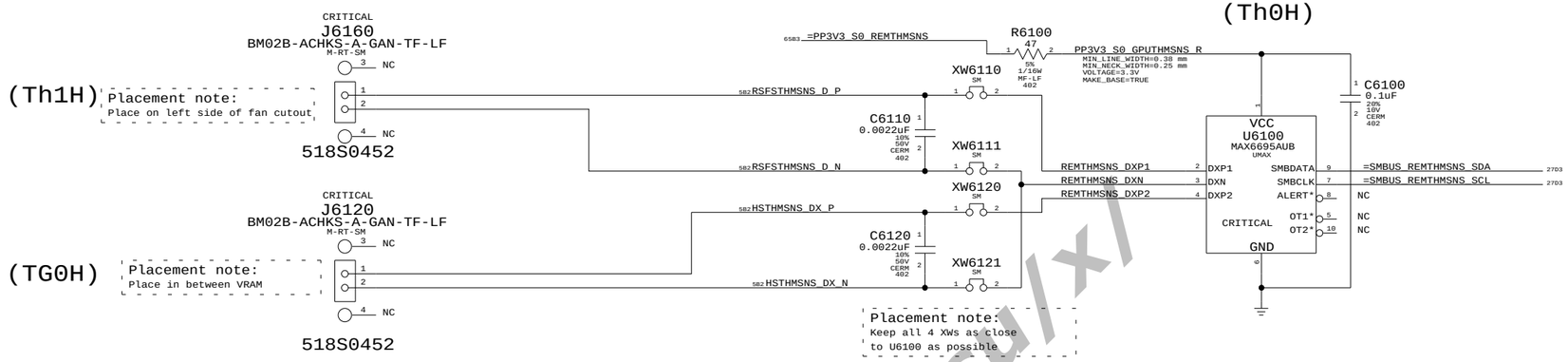
LPC+ Debug Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

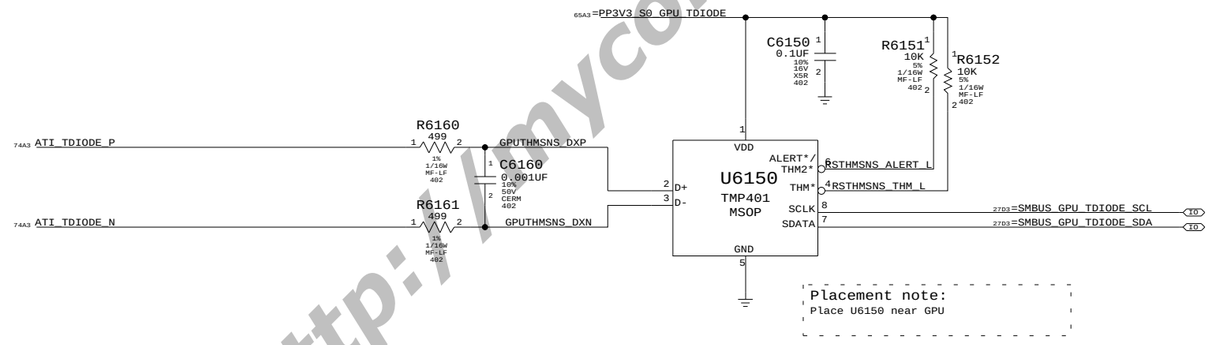
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 51 OF 84	

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE

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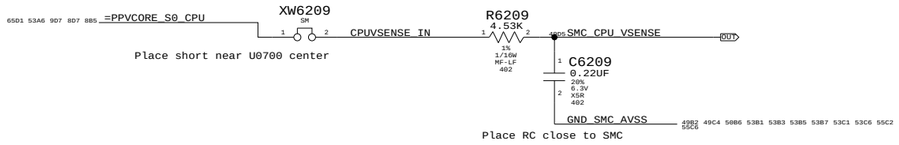
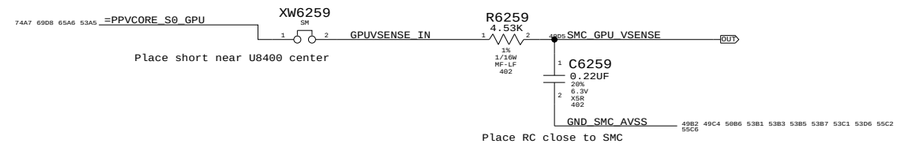
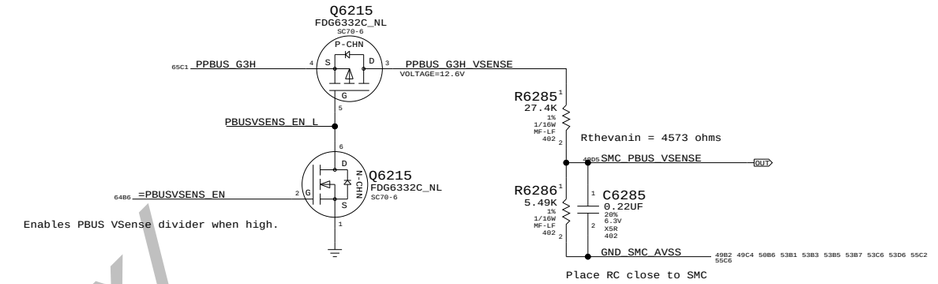
CPU Voltage Sense / Filter



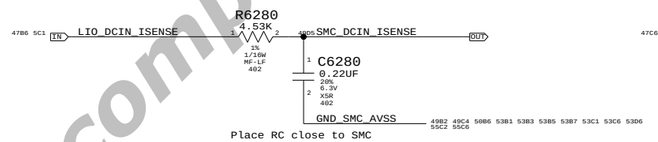
GPU Voltage Sense / Filter



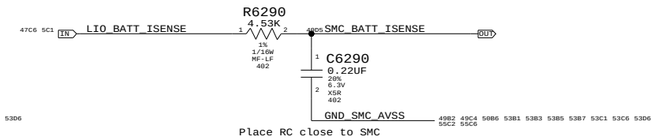
PBUS Voltage Sense Enable & Filter



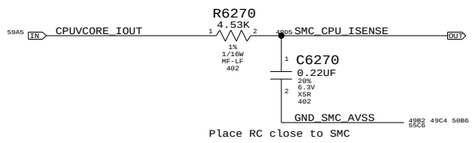
DCIN Current Sense Filter



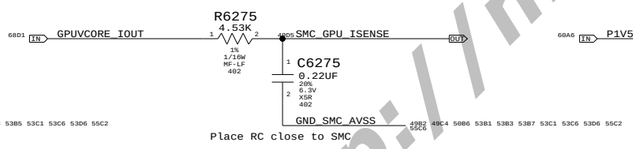
Battery Current Sense Filter



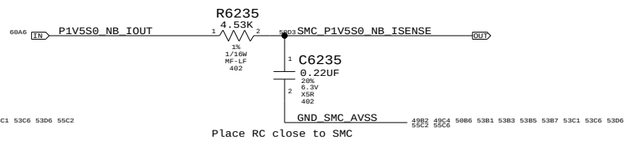
CPU Current Sense Filter



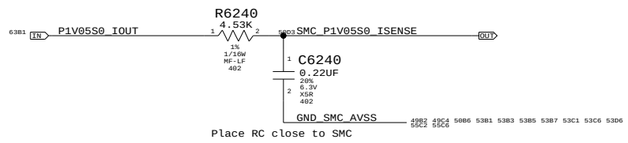
GPU Current Sense Filter



1.5V S0 (NB) Current Sense Filter

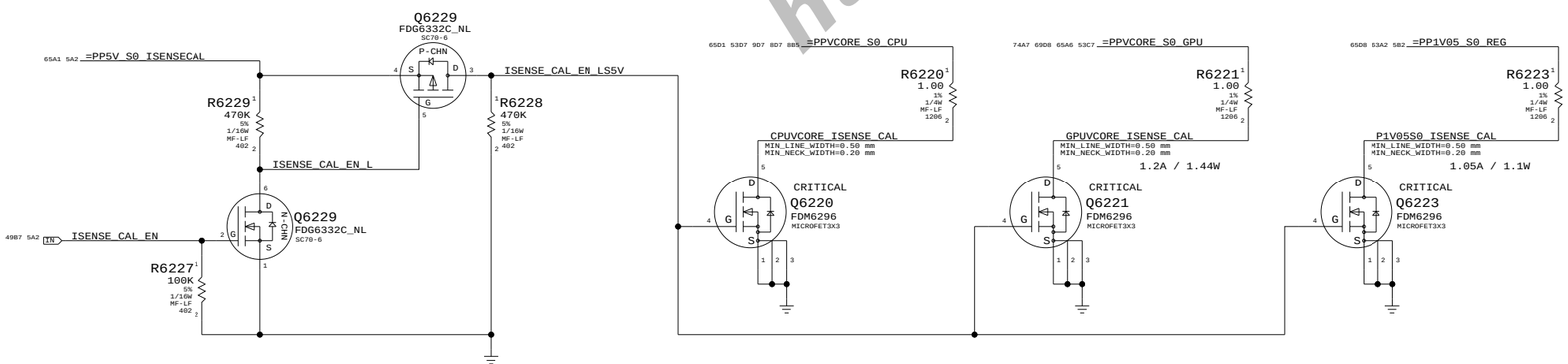


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

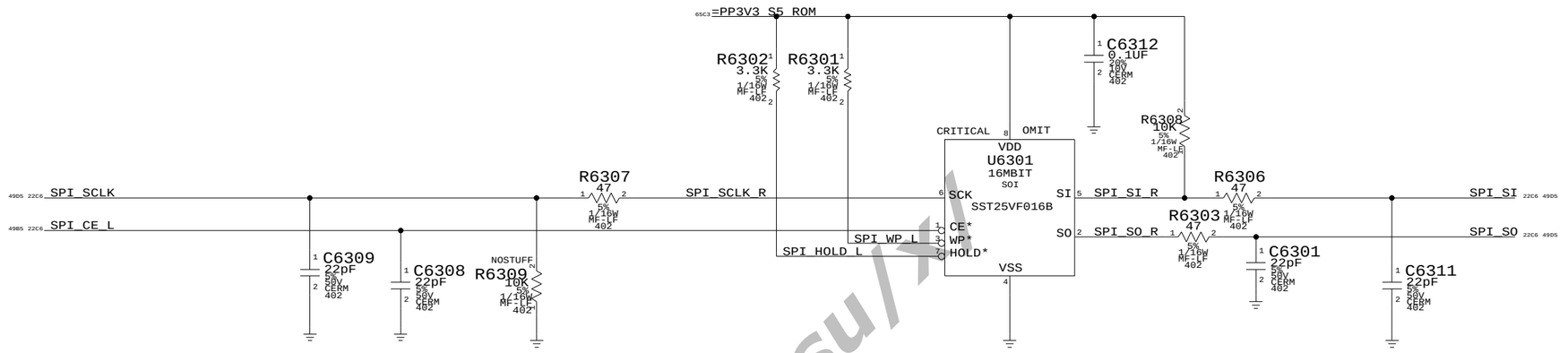


Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 53 OF 84	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

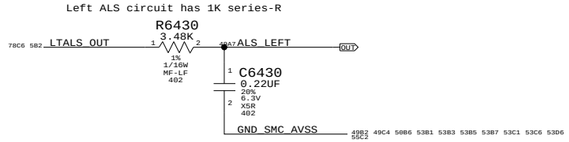
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE

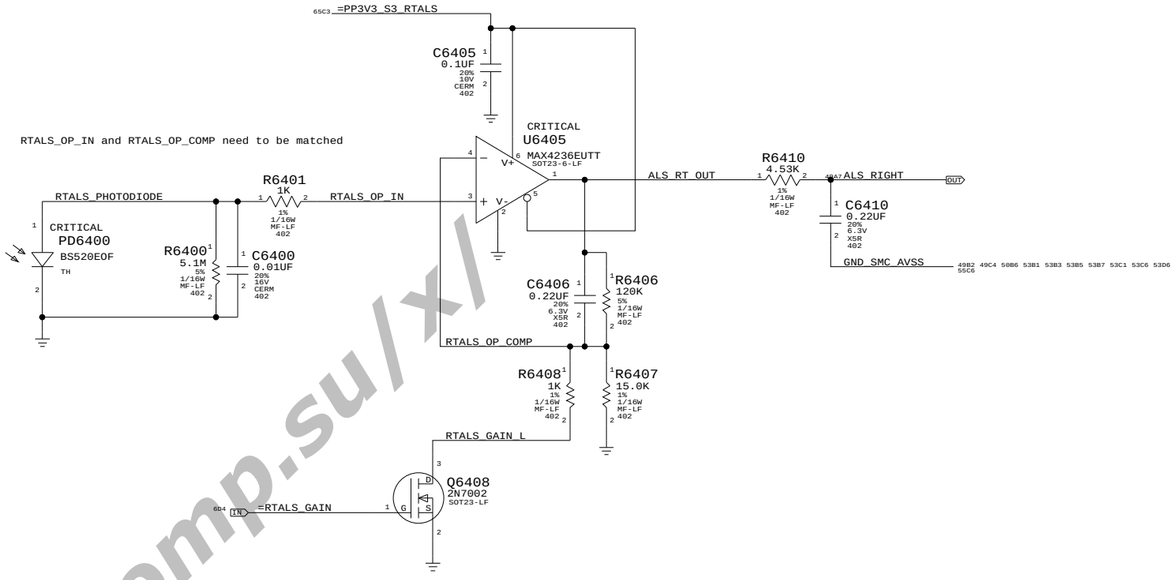
SHT 54 OF 84

Left ALS Filter

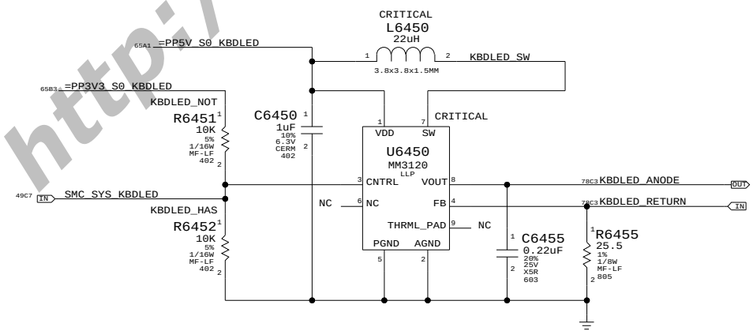
Left ALS circuit has 1K series-R



Right ALS Circuit



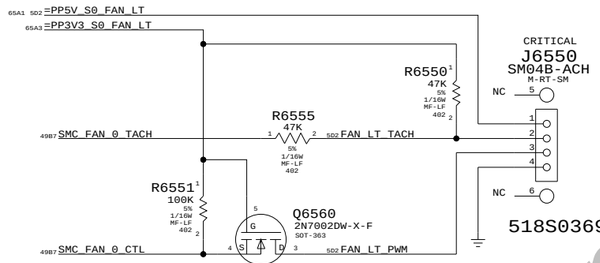
Keyboard LED Driver



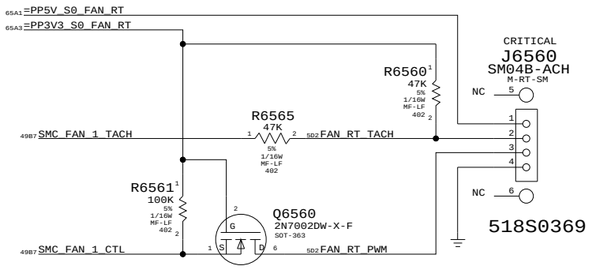
ALS Support			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
	SCALE: NONE	SHT 55 OF 84	

Left Fan



Right Fan



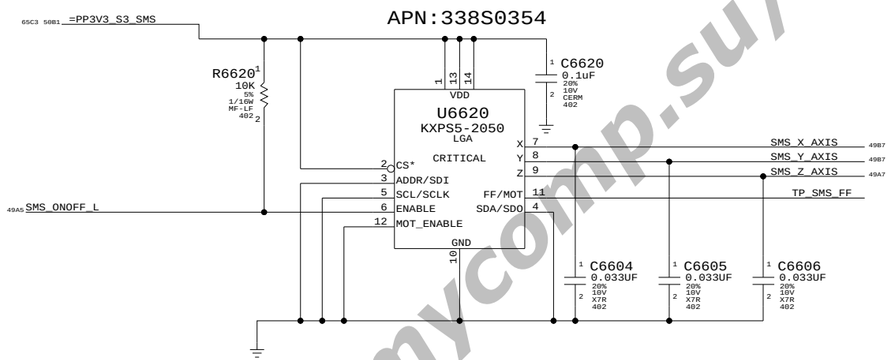
Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

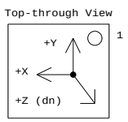
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	56	84



Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:



M59 placement: Bottom-side

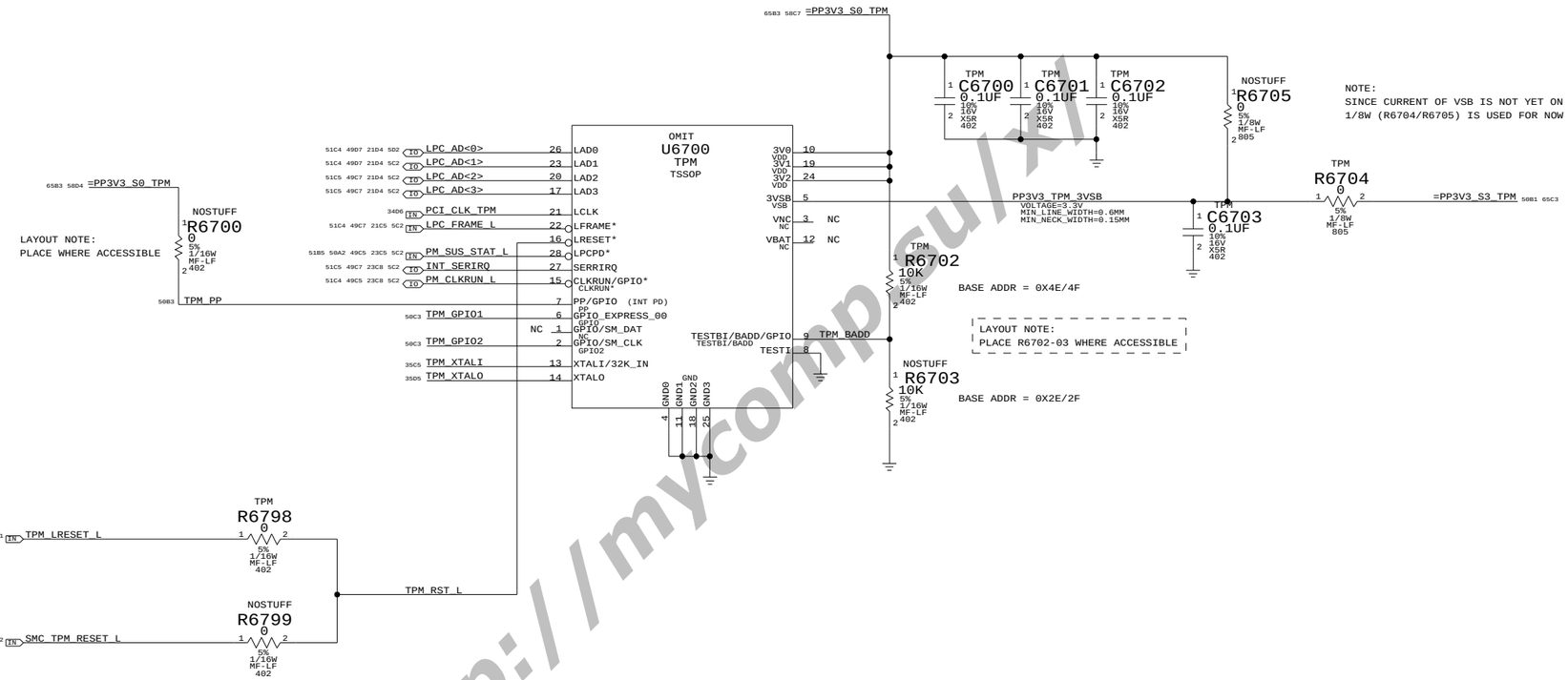
Sudden Motion Sensor (SMS)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 57 OF 84



TPM

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	58	84

DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

CPU VCore Current Sense

IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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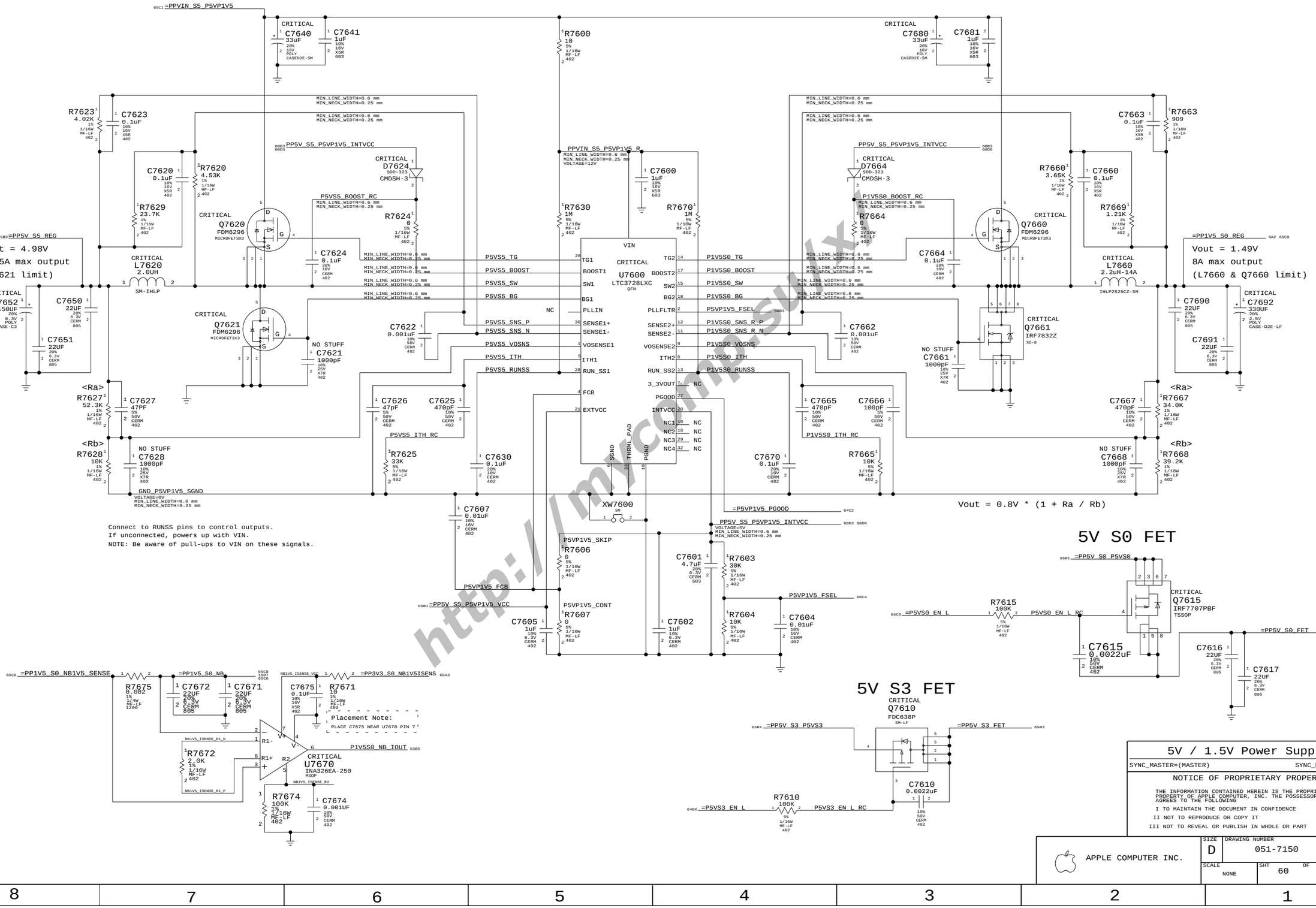
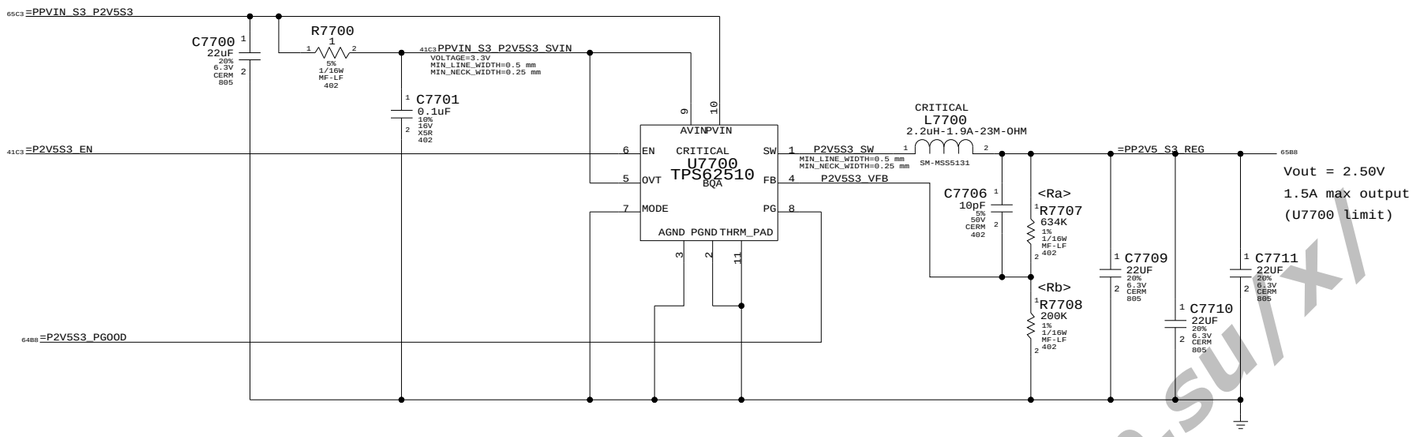
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 59 OF 84	

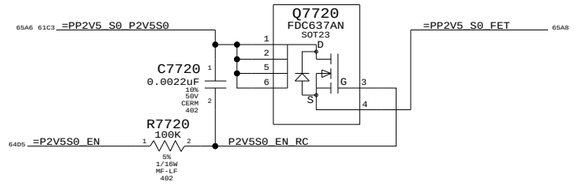


2.5V S3 Regulator

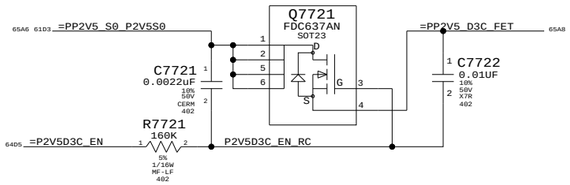


Vout = 0.6V * (1 + Ra / Rb)

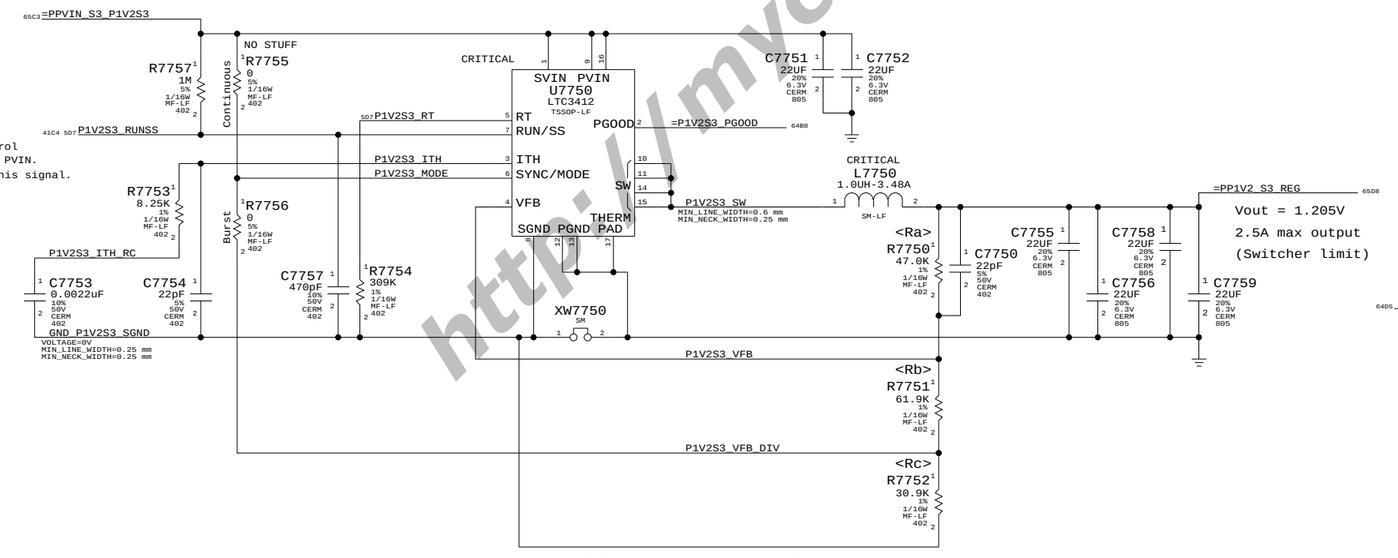
2.5V S0 FET



2.5V D3Cold FET

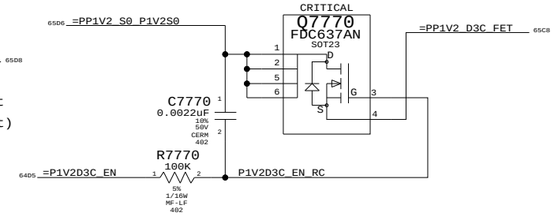


1.2V S3 Regulator



Vout = 0.8V * (1 + Ra / (Rb + Rc))

1.2V D3Cold FET



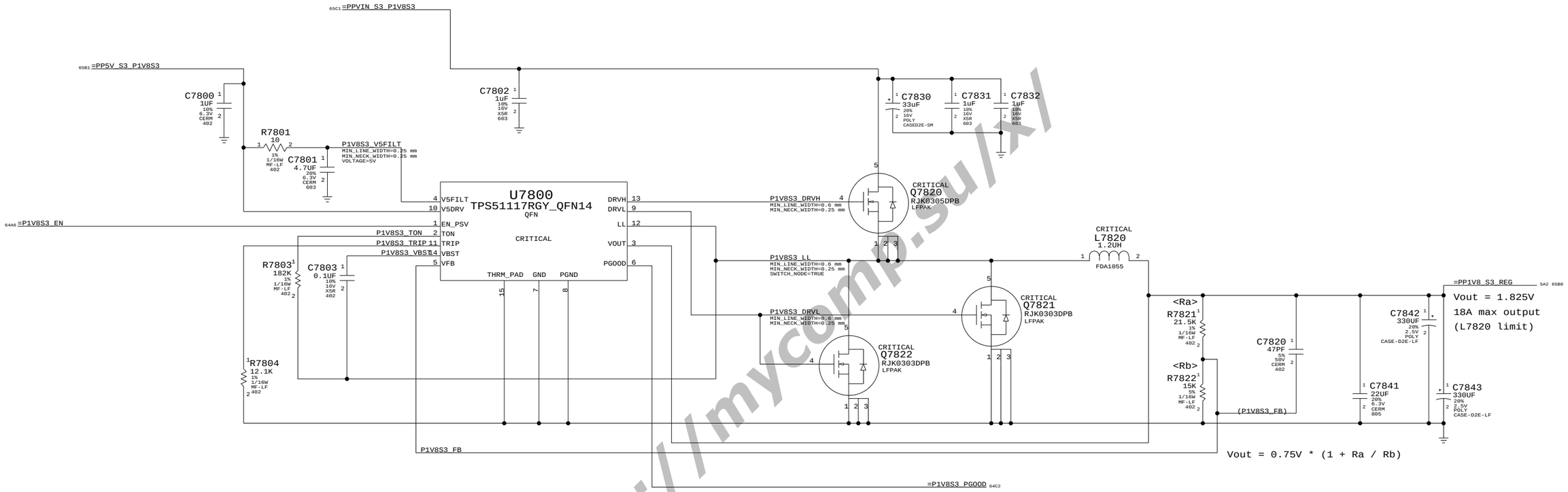
2.5V & 1.2V Regulators

SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

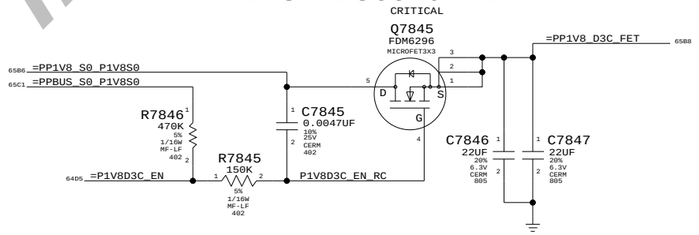
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 61 OF 84



1.8V D3Cold FET

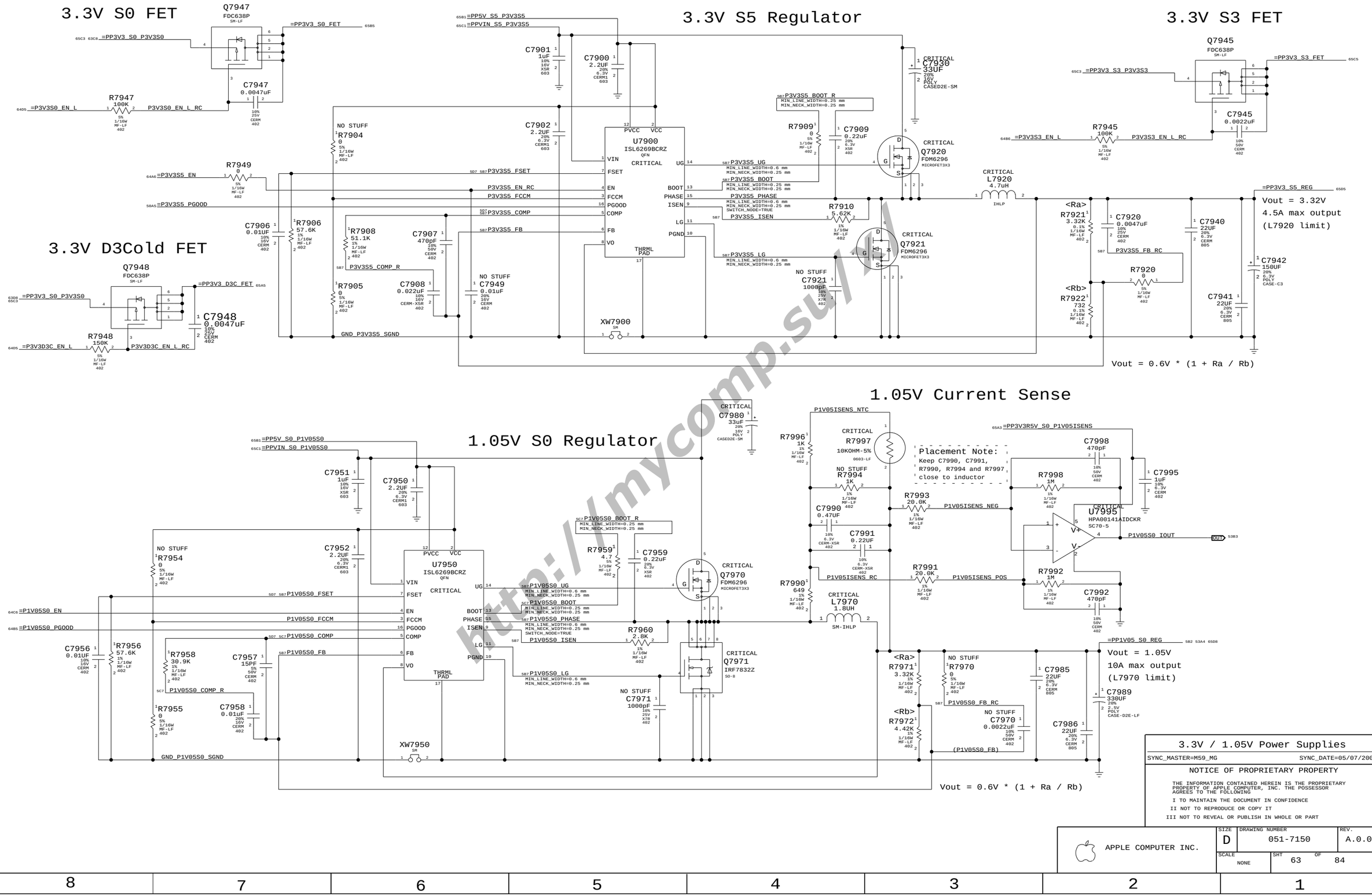


1.8V Supply

SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 62 OF 84	



Power Control Signals

=PP5V_S5_PWRCTL

R8050 10K 5% 1/16W MF-LF 402
R8051 10K 5% 1/16W MF-LF 402
R8052 10K 5% 1/16W MF-LF 402
R8068 10K 5% 1/16W MF-LF 402
R8069 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

=GPUVCORE_PGOOD

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V (MAKE_BASE=TRUE) → =P2V5D3C_EN
=P1V2D3C_EN
P3V3D3C_EN_L (MAKE_BASE=TRUE) → =P3V3D3C_EN_L
P1V8D3C_EN (MAKE_BASE=TRUE) → =P1V8D3C_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363
Q8056 2N7002DW-X-F SOT-363
Q8050 2N7002DW-X-F SOT-363
Q8058 2N7002DW-X-F SOT-363
Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE) → =P2V5S0_EN
P3V3S0_EN_L (MAKE_BASE=TRUE) → =P3V3S0_EN_L

=PP3V42_G3H_PWRCTL

PM_SLP_S3_LS5V (MAKE_BASE=TRUE) → =P5VS0_EN_L
LIO_P3V3S0_EN_L
P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

Q8050 2N7002DW-X-F SOT-363
R8054 100K 5% 1/16W MF-LF 402
Q8057 2N7002DW-X-F SOT-363
Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3_L
R8056 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) (MAKE_BASE=TRUE) → =P1V05S0_EN, =ENET_VMAIN_AVLBL, =MEMVREF_EN, =PBUSVSENS_EN

=PP3V3_S3_PWRCTL
=PP3V3_S0_PWRCTL
R8053 10K 5% 1/16W MF-LF 402
R8081 10K 5% 1/16W MF-LF 402
C8081 0.1uF 20% 10V CERM 402

=P2V5S3_PGOOD
=P1V2S3_PGOOD
TP_P2V5S3_P1V2S3_PGOOD (MAKE_BASE=TRUE)

This signal was used as an option previously to test for 2v5 and 1v2 S3 valid for GPUVCORE_EN. But was disconnected for C8053 placement.

PM_SLP_S3_L_GPUVCORE_EN
C8053 0.047UF 10% 16V CERM 402
TP_SB_GPIO38
SB_GPUVCORE_DISABLE_L (MAKE_BASE=TRUE)
U8081 MC74VHC1G08 SC70
GPUVCORE_EN (MAKE_BASE=TRUE) → =GPUVCORE_EN

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

=PP5V_S5_PWRCTL
R8055 10K 5% 1/16W MF-LF 402
PM_SLP_S4_LS5V (MAKE_BASE=TRUE) → =P3V3S3_EN_L, =P5VS3_EN_L
Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L
R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) (MAKE_BASE=TRUE) → =P1V8S3_EN, =RTUSB_EN, LIO_P3V3S3_EN

=PP3V42_G3H_PWRCTL
P5VS5_PGOOD
(P5VS5_PGOOD) (MAKE_BASE=TRUE) → =P3V3S5_EN
R8059 470K 5% 1/16W MF-LF 402
P5VS5_RUNSS
5V Enable has pull-up to PBUS
Q8059 2N7002DW-X-F SOT-363
SMC_PM_G2_EN_L
Q8059 2N7002DW-X-F SOT-363
SMC_PM_G2_EN
R8058 100K 5% 1/16W MF-LF 402

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

=PPVIN_G3H_P3V42G3H
C8000 10UF 10% 25V X5R 1206-1
U8000 LT3470 TSOT23-8
P3V42G3H5_BOOST
C8005 0.22uF 20% 6.3V X5R 402
CRITICAL L8010 33uH CDPH4D19F-SM
SHDN*
NC
SW — P3V42G3H_SW (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, SWITCH_NODE=TRUE)
BIAS
FB
GND
C8010 22pF 5% 50V CERM 402
<Ra> R8010 348K 1% 1/16W MF-LF 402
<Rb> R8011 200K 1% 1/16W MF-LF 402
P3V42G3H_FB
=PP3V42_G3H_REG
C8015 22UF 20% 6.3V CERM 805

Vout = 3.425
200mA max output
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

=PP3V3_S5_P1V5PG
PP1V5_S0
R8061 27.4K 1% 1/16W MF-LF 402
R8063 4.99K 1% 1/16W MF-LF 402
C8060 0.1uF 20% 10V CERM 402
0.89V Reference
P1V0_P1V5PG_REF
P1V5S0_COMP_POS
U8060 LMC7211 SM-LF
P1V5S0_PGOOD
R8062 10K 1% 1/16W MF-LF 402
R8064 10K 1% 1/16W MF-LF 402
R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

IMVP_PWRGD_IN (OUT 59C7)

=P1V05S0_PGOOD
P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

=P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)
=P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

=PP3V3_S0_ALLSYSPG
U8080 MC74VHC1G08 SC70
PGOOD_MUXED_S0_OR_S0D3C
ALL_SYS_PWRGD (OUT 26A5 49D7)
C8080 0.1UF 20% 10V CERM 402

PP3V3_S0
PP5V_S0
PP2V5_S0
PP0V9_S0
R8074 68.1K 1% 1/16W MF-LF 402
R8072 365K 1% 1/16W MF-LF 402
R8070 845K 1% 1/16W MF-LF 402
C8070 0.1uF 20% 10V CERM 402
R8076 10K 5% 1/16W MF-LF 402
U8070 LTC2903 TSOT-23
CRITICAL V1
S0PGOOD_5V_DIV
S0PGOOD_2V5_DIV
S0PGOOD_0V9_DIV
RST*
GND
S0PGOOD_PWROK (79A4 79D5)
R8075 100K 1% 1/16W MF-LF 402 — C8075 0.1UF 20% 10V CERM 402
R8073 100K 1% 1/16W MF-LF 402 — C8073 0.1UF 20% 10V CERM 402
R8071 100K 1% 1/16W MF-LF 402 — C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M59_MG SYNC_DATE=08/01/2006

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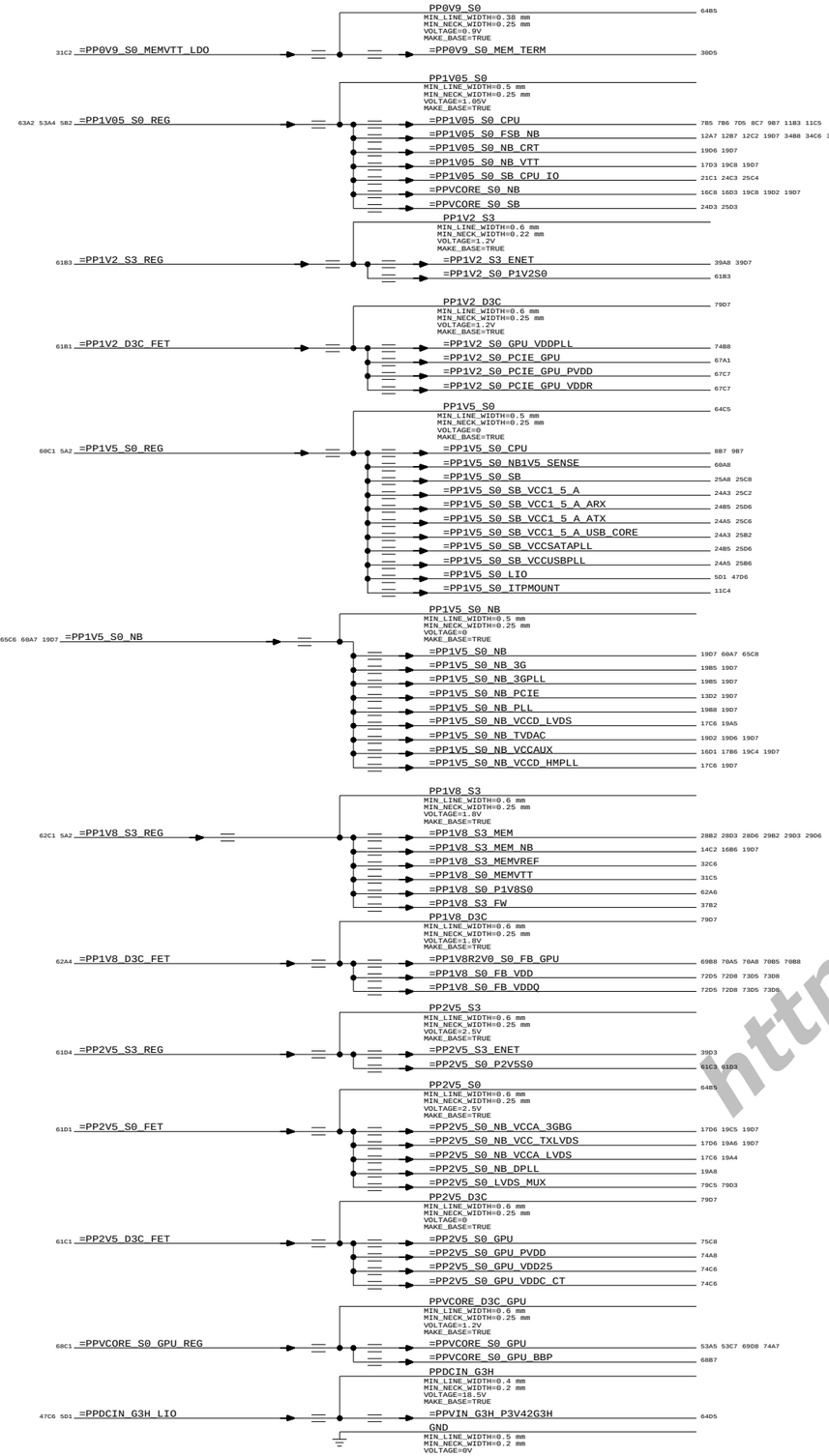
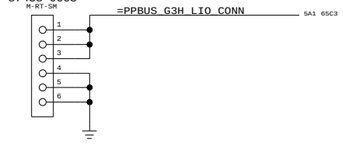
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 64 OF 84



Left I/O Power Connector

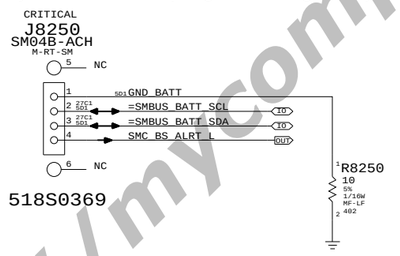
CRITICAL
J8200
87438-0663
M-RT-SM



518S0458

Battery Connector (Digital Signals)

CRITICAL
J8250
SM04B-ACH
M-RT-SM



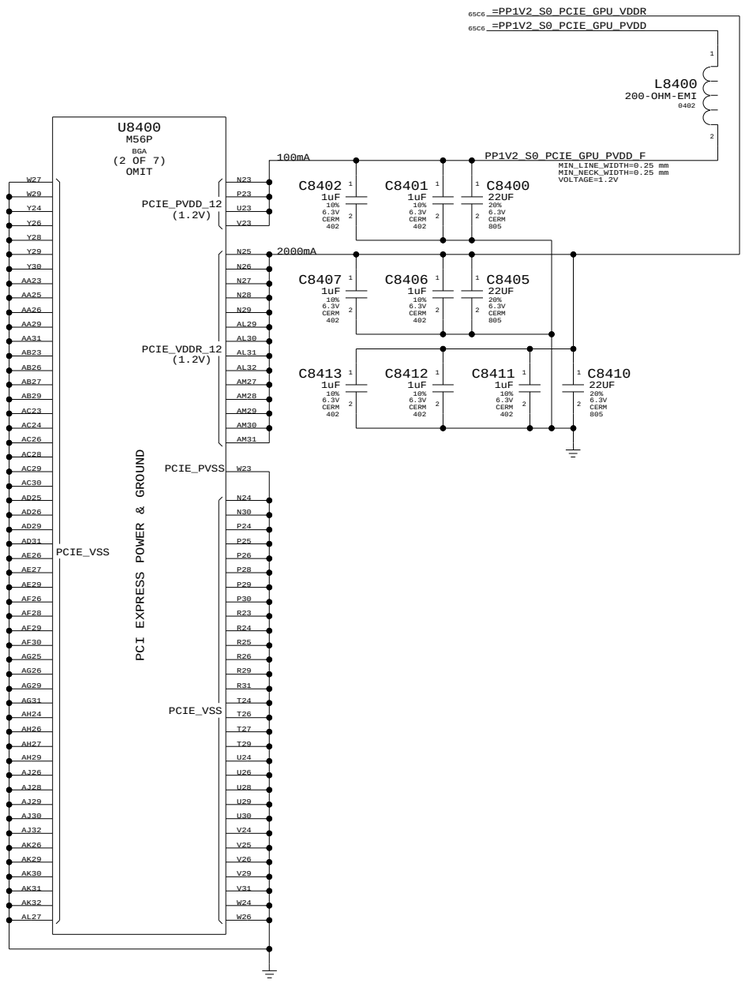
518S0369

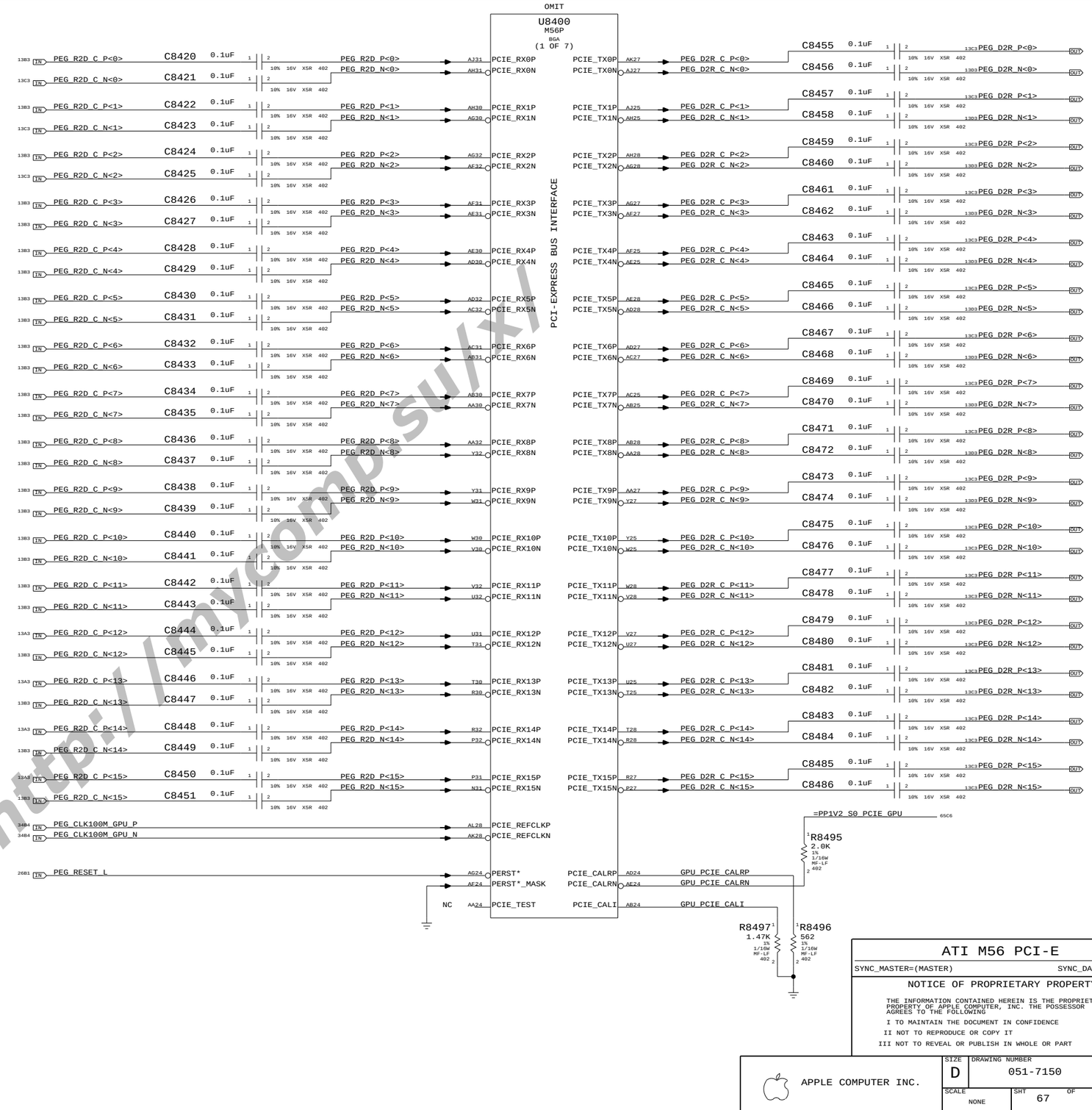
PBus-In,Batt. & 3G Pwr Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 66 OF 84	





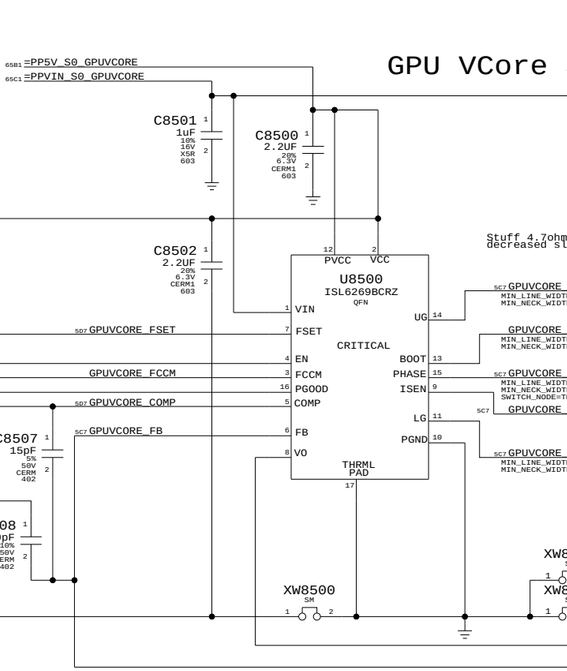
ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

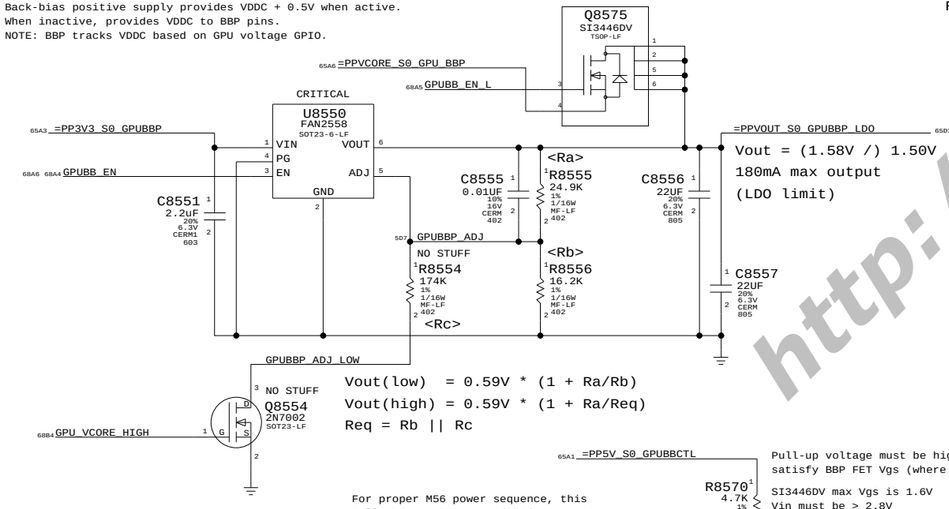
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 67 OF 84	

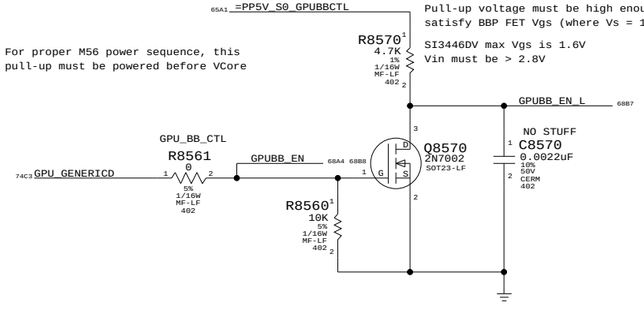
GPU VCore Current Sense



Back-Bias Positive Supply

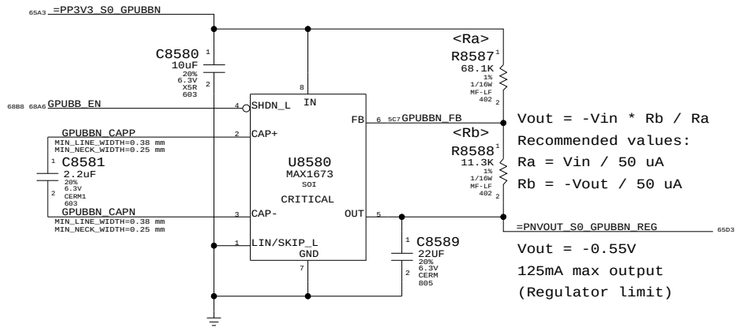
Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.





Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

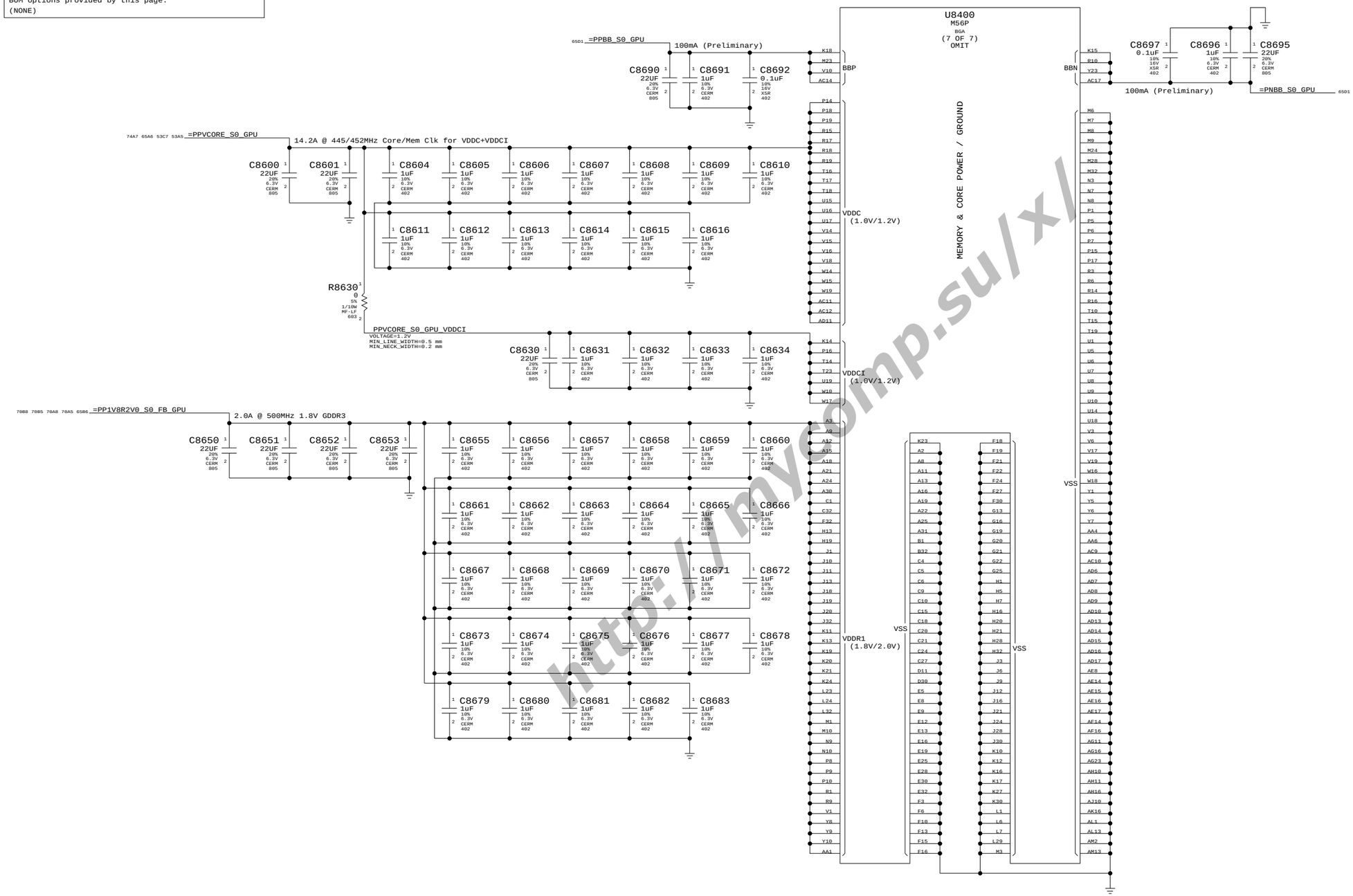
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 68 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 69 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8400
M56P
BGA
(3 OF 7)

MEMORY INTERFACE A

FB_A_DQ<0>	M31	DQA_0	
FB_A_DQ<1>	M30	DQA_1	
FB_A_DQ<2>	L31	DQA_2	
FB_A_DQ<3>	L30	DQA_3	
FB_A_DQ<4>	H30	DQA_4	
FB_A_DQ<5>	G31	DQA_5	
FB_A_DQ<6>	G30	DQA_6	
FB_A_DQ<7>	F31	DQA_7	
FB_A_DQ<8>	M27	DQA_8	
FB_A_DQ<9>	M29	DQA_9	
FB_A_DQ<10>	L28	DQA_10	
FB_A_DQ<11>	L27	DQA_11	
FB_A_DQ<12>	J27	DQA_12	
FB_A_DQ<13>	H29	DQA_13	
FB_A_DQ<14>	G29	DQA_14	
FB_A_DQ<15>	G27	DQA_15	
FB_A_DQ<16>	M26	DQA_16	
FB_A_DQ<17>	L26	DQA_17	
FB_A_DQ<18>	M25	DQA_18	
FB_A_DQ<19>	L25	DQA_19	
FB_A_DQ<20>	J25	DQA_20	
FB_A_DQ<21>	G28	DQA_21	
FB_A_DQ<22>	H27	DQA_22	
FB_A_DQ<23>	H26	DQA_23	
FB_A_DQ<24>	F26	DQA_24	
FB_A_DQ<25>	G26	DQA_25	
FB_A_DQ<26>	H25	DQA_26	
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FB_A_DQ<45>	B14	DQA_45	
FB_A_DQ<46>	C13	DQA_46	
FB_A_DQ<47>	B13	DQA_47	
FB_A_DQ<48>	D17	DQA_48	
FB_A_DQ<49>	E18	DQA_49	
FB_A_DQ<50>	E17	DQA_50	
FB_A_DQ<51>	F17	DQA_51	
FB_A_DQ<52>	E15	DQA_52	
FB_A_DQ<53>	E14	DQA_53	
FB_A_DQ<54>	F14	DQA_54	
FB_A_DQ<55>	D13	DQA_55	
FB_A_DQ<56>	H18	DQA_56	
FB_A_DQ<57>	H17	DQA_57	
FB_A_DQ<58>	G18	DQA_58	
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FB_A_DQ<60>	G15	DQA_60	
FB_A_DQ<61>	G14	DQA_61	
FB_A_DQ<62>	H14	DQA_62	
FB_A_DQ<63>	J14	DQA_63	

MAA_0	D26	FB_A_MA<0>	OUT
MAA_1	F28	FB_A_MA<1>	OUT
MAA_2	D28	FB_A_MA<2>	OUT
MAA_3	D25	FB_A_MA<3>	OUT
MAA_4	E24	FB_A_MA<4>	OUT
MAA_5	E26	FB_A_MA<5>	OUT
MAA_6	D27	FB_A_MA<6>	OUT
MAA_7	F25	FB_A_MA<7>	OUT
MAA_8	C26	FB_A_MA<8>	OUT
MAA_9	B26	FB_A_MA<9>	OUT
MAA_10	D29	FB_A_MA<10>	OUT
MAA_11	B27	FB_A_MA<11>	OUT
MAA_12	E27	TP_FB_A_MA12	OUT
MAA_13	E29	FB_A_BA<2>	OUT
MAA_14	B25	FB_A_BA<0>	OUT
MAA_15	C25	FB_A_BA<1>	OUT

READ STROBE

DQMA_0	H31	FB_A_DQM_L<0>	IO
DQMA_1	J29	FB_A_DQM_L<1>	IO
DQMA_2	J26	FB_A_DQM_L<2>	IO
DQMA_3	G23	FB_A_DQM_L<3>	IO
DQMA_4	E21	FB_A_DQM_L<4>	IO
DQMA_5	B15	FB_A_DQM_L<5>	IO
DQMA_6	D14	FB_A_DQM_L<6>	IO
DQMA_7	J17	FB_A_DQM_L<7>	IO

QSA_0	J31	FB_A_RDQS<0>	IN
QSA_1	K29	FB_A_RDQS<1>	IN
QSA_2	K25	FB_A_RDQS<2>	IN
QSA_3	F23	FB_A_RDQS<3>	IN
QSA_4	D20	FB_A_RDQS<4>	IN
QSA_5	B16	FB_A_RDQS<5>	IN
QSA_6	D16	FB_A_RDQS<6>	IN
QSA_7	H15	FB_A_RDQS<7>	IN

WRITE STROBE

QSA_0*	K31	FB_A_WDQS<0>	OUT
QSA_1*	K28	FB_A_WDQS<1>	OUT
QSA_2*	K26	FB_A_WDQS<2>	OUT
QSA_3*	G24	FB_A_WDQS<3>	OUT
QSA_4*	D21	FB_A_WDQS<4>	OUT
QSA_5*	C16	FB_A_WDQS<5>	OUT
QSA_6*	D15	FB_A_WDQS<6>	OUT
QSA_7*	J15	FB_A_WDQS<7>	OUT

CLKA0	D31	FB_A_CLK_P<0>	OUT
CLKA0*	E31	FB_A_CLK_N<0>	OUT
CSA0_0*	B29	FB_A_CS_L<0>	OUT
CSA0_1*	C28	NC	
CKEA0	B30	FB_A_CKE<0>	OUT
RASA0*	B28	FB_A_RAS_L<0>	OUT
CASA0*	C29	FB_A_CAS_L<0>	OUT
WEA0*	B31	FB_A_WE_L<0>	OUT
ODTA0	F29	TP_FB_A_ODT<0>	OUT
CLKA1	B20	FB_A_CLK_P<1>	OUT
CLKA1*	C19	FB_A_CLK_N<1>	OUT
CSA1_0*	B23	FB_A_CS_L<1>	OUT
CSA1_1*	C23	NC	
CKEA1	C22	FB_A_CKE<1>	OUT
RASA1*	B24	FB_A_RAS_L<1>	OUT
CASA1*	B22	FB_A_CAS_L<1>	OUT
WEA1*	B21	FB_A_WE_L<1>	OUT
ODTA1	D24	TP_FB_A_ODT<1>	OUT

=PP1V8R2V0_S0_FB_GPU

R8710 40.2 1% 1/16W MF-LF 402
R8712 40.2 1% 1/16W MF-LF 402
R8711 100 1% 1/16W MF-LF 402
C8711 0.1uF 10% 16V X5R 402
R8713 100 1% 1/16W MF-LF 402
C8713 0.1uF 10% 16V X5R 402

GPU_MVREFD0 → MVREFD_0
GPU_MVREFS0 → MVREFS_0
VDDRH0 (1.8V/2.0V)
VSSRH0

=PP1V8R2V0_S0_FB_GPU

L8715 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
PP1V8R2V0_S0_GPU_VDDRH0

C8715 1uF 10% 6.3V CERM 402
C8716 1uF 10% 6.3V CERM 402

XW8715 SM
GND_GPU_VSSRH0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

OMIT
U8400
M56P
BGA
(4 OF 7)

MEMORY INTERFACE B

FB_B_DQ<0>	B12	DQB_0	
FB_B_DQ<1>	C12	DQB_1	
FB_B_DQ<2>	B11	DQB_2	
FB_B_DQ<3>	C11	DQB_3	
FB_B_DQ<4>	C8	DQB_4	
FB_B_DQ<5>	B7	DQB_5	
FB_B_DQ<6>	C7	DQB_6	
FB_B_DQ<7>	B6	DQB_7	
FB_B_DQ<8>	F12	DQB_8	
FB_B_DQ<9>	D12	DQB_9	
FB_B_DQ<10>	E11	DQB_10	
FB_B_DQ<11>	F11	DQB_11	
FB_B_DQ<12>	F9	DQB_12	
FB_B_DQ<13>	D8	DQB_13	
FB_B_DQ<14>	D7	DQB_14	
FB_B_DQ<15>	F7	DQB_15	
FB_B_DQ<16>	G12	DQB_16	
FB_B_DQ<17>	G11	DQB_17	
FB_B_DQ<18>	H12	DQB_18	
FB_B_DQ<19>	H11	DQB_19	
FB_B_DQ<20>	H9	DQB_20	
FB_B_DQ<21>	E7	DQB_21	
FB_B_DQ<22>	F8	DQB_22	
FB_B_DQ<23>	G8	DQB_23	
FB_B_DQ<24>	G6	DQB_24	
FB_B_DQ<25>	G7	DQB_25	
FB_B_DQ<26>	H8	DQB_26	
FB_B_DQ<27>	J8	DQB_27	
FB_B_DQ<28>	K8	DQB_28	
FB_B_DQ<29>	L8	DQB_29	
FB_B_DQ<30>	K9	DQB_30	
FB_B_DQ<31>	L9	DQB_31	
FB_B_DQ<32>	K5	DQB_32	
FB_B_DQ<33>	L4	DQB_33	
FB_B_DQ<34>	K4	DQB_34	
FB_B_DQ<35>	L5	DQB_35	
FB_B_DQ<36>	N5	DQB_36	
FB_B_DQ<37>	N6	DQB_37	
FB_B_DQ<38>	P4	DQB_38	
FB_B_DQ<39>	R4	DQB_39	
FB_B_DQ<40>	P2	DQB_40	
FB_B_DQ<41>	R2	DQB_41	
FB_B_DQ<42>	T3	DQB_42	
FB_B_DQ<43>	T2	DQB_43	
FB_B_DQ<44>	W3	DQB_44	
FB_B_DQ<45>	W2	DQB_45	
FB_B_DQ<46>	Y3	DQB_46	
FB_B_DQ<47>	Y2	DQB_47	
FB_B_DQ<48>	T4	DQB_48	
FB_B_DQ<49>	R5	DQB_49	
FB_B_DQ<50>	T5	DQB_50	
FB_B_DQ<51>	T6	DQB_51	
FB_B_DQ<52>	V5	DQB_52	
FB_B_DQ<53>	W5	DQB_53	
FB_B_DQ<54>	W6	DQB_54	
FB_B_DQ<55>	Y4	DQB_55	
FB_B_DQ<56>	R8	DQB_56	
FB_B_DQ<57>	T8	DQB_57	
FB_B_DQ<58>	R7	DQB_58	
FB_B_DQ<59>	T7	DQB_59	
FB_B_DQ<60>	V7	DQB_60	
FB_B_DQ<61>	W7	DQB_61	
FB_B_DQ<62>	W8	DQB_62	
FB_B_DQ<63>	W9	DQB_63	

MAB_0	G4	FB_B_MA<0>	OUT
MAB_1	E6	FB_B_MA<1>	OUT
MAB_2	E4	FB_B_MA<2>	OUT
MAB_3	H4	FB_B_MA<3>	OUT
MAB_4	J5	FB_B_MA<4>	OUT
MAB_5	G5	FB_B_MA<5>	OUT
MAB_6	F4	FB_B_MA<6>	OUT
MAB_7	H6	FB_B_MA<7>	OUT
MAB_8	G3	FB_B_MA<8>	OUT
MAB_9	G2	FB_B_MA<9>	OUT
MAB_10	D4	FB_B_MA<10>	OUT
MAB_11	F2	FB_B_MA<11>	OUT
MAB_12	F5	TP_FB_B_MA12	OUT
MAB_13	D5	FB_B_BA<2>	OUT
MAB_14	H2	FB_B_BA<0>	OUT
MAB_15	H3	FB_B_BA<1>	OUT

READ STROBE

DQMB_0	B8	FB_B_DQM_L<0>	IO
DQMB_1	D9	FB_B_DQM_L<1>	IO
DQMB_2	G9	FB_B_DQM_L<2>	IO
DQMB_3	K7	FB_B_DQM_L<3>	IO
DQMB_4	M5	FB_B_DQM_L<4>	IO
DQMB_5	V2	FB_B_DQM_L<5>	IO
DQMB_6	W4	FB_B_DQM_L<6>	IO
DQMB_7	T9	FB_B_DQM_L<7>	IO

QSB_0	B9	FB_B_RDQS<0>	OUT
QSB_1	D10	FB_B_RDQS<1>	OUT
QSB_2	H10	FB_B_RDQS<2>	OUT
QSB_3	K6	FB_B_RDQS<3>	OUT
QSB_4	N4	FB_B_RDQS<4>	OUT
QSB_5	U2	FB_B_RDQS<5>	OUT
QSB_6	U4	FB_B_RDQS<6>	OUT
QSB_7	V8	FB_B_RDQS<7>	OUT

WRITE STROBE

QSB_0*	B10	FB_B_WDQS<0>	IN
QSB_1*	E10	FB_B_WDQS<1>	IN
QSB_2*	G10	FB_B_WDQS<2>	IN
QSB_3*	J7	FB_B_WDQS<3>	IN
QSB_4*	M4	FB_B_WDQS<4>	IN
QSB_5*	U3	FB_B_WDQS<5>	IN
QSB_6*	V4	FB_B_WDQS<6>	IN
QSB_7*	V9	FB_B_WDQS<7>	IN

CLKB0	B4	FB_B_CLK_P<0>	OUT
CLKB0*	B5	FB_B_CLK_N<0>	OUT
CSB0_0*	D2	FB_B_CS_L<0>	OUT
CSB0_1*	E3	NC	
CKEB0	C2	FB_B_CKE<0>	OUT
RASB0*	E2	FB_B_RAS_L<0>	OUT
CASB0*	D3	FB_B_CAS_L<0>	OUT
WEB0*	B2	FB_B_WE_L<0>	OUT
ODTB0	D6	TP_FB_B_ODT<0>	OUT
CLKB1	N2	FB_B_CLK_P<1>	OUT
CLKB1*	P3	FB_B_CLK_N<1>	OUT
CSB1_0*	K2	FB_B_CS_L<1>	OUT
CSB1_1*	K3	NC	
CKEB1	L3	FB_B_CKE<1>	OUT
RASB1*	J2	FB_B_RAS_L<1>	OUT
CASB1*	L2	FB_B_CAS_L<1>	OUT
WEB1*	M2	FB_B_WE_L<1>	OUT
ODTB1	J4	TP_FB_B_ODT<1>	OUT

=PP1V8R2V0_S0_FB_GPU

R8720 40.2 1% 1/16W MF-LF 402
R8722 40.2 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
C8721 0.1uF 10% 16V X5R 402
R8723 100 1% 1/16W MF-LF 402
C8723 0.1uF 10% 16V X5R 402

GPU_MVREFD1 → MVREFD_1
GPU_MVREFS1 → MVREFS_1
PP1V8R2V0_S0_GPU_VDDRH1 → VDDRH1 (1.8V/2.0V)
VSSRH1

GPU_TEST_MCLK → TEST_MCLK
GPU_TEST_YCLK → TEST_YCLK
GPU_MEMTEST → MEMTEST
DRAM_RST → FB_DRAM_RST

R8731 4.7K 5% 1/16W MF-LF 402
R8730 4.7K 5% 1/16W MF-LF 402
R8732 243 1% 1/16W MF-LF 402
R8733 4.7K 5% 1/16W MF-LF 402

=PP1V8R2V0_S0_FB_GPU

L8725 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

C8725 1uF 10% 6.3V CERM 402
C8726 1uF 10% 6.3V CERM 402

XW8725 SM
GND_GPU_VSSRH1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-7150	A.0.0
SCALE: NONE	SHT 70 OF 84	

ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

65A3 =PP3V3_D3C_GPU_GPIOS

R8800 10K 5% 1/16W MF-LF 402
R8801 10K 5% 1/16W MF-LF 402 GPU_DEEPMH_EN
R8802 10K 5% 1/16W MF-LF 402 NO STUFF
R8803 10K 5% 1/16W MF-LF 402 NO STUFF
R8804 10K 5% 1/16W MF-LF 402 NO STUFF
R8805 10K 5% 1/16W MF-LF 402
R8806 10K 5% 1/16W MF-LF 402 NO STUFF
R8808 10K 5% 1/16W MF-LF 402
R8809 10K 5% 1/16W MF-LF 402 NO STUFF
R8811 10K 5% 1/16W MF-LF 402 NO STUFF
R8812 10K 5% 1/16W MF-LF 402 GPU_MEM_256M
R8813 10K 5% 1/16W MF-LF 402 GPU_MEM_64M
R8824 10K 5% 1/16W MF-LF 402 GPU_MEM_256M
R8827 10K 5% 1/16W MF-LF 402 GPU_MEM_NOT_SAM

		Serial ROM	TestBus	Misc	Straps	
74D3	GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb	
74D3	GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN	
74D3	GPU_GPIO_2		TESTIN[2]		Reserved	
74D3	GPU_GPIO_3		TESTIN[3]		Reserved	
74D3	GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS	
74D3	GPU_GPIO_5		TESTIN[5]		Reserved	
74D3	GPU_GPIO_6		TESTIN[6]		Reserved	
74D3	GPU_GPIO_7	ENA_BL	TESTIN[7]			GPU_BLON (MAKE_BASE=TRUE) 79A4
74D3	GPU_GPIO_8	ROMSO	TESTWR		Reserved	
74C3	GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]	
74C3	GPU_GPIO_10	ROMSCK	TESTOUT[8]			TP_GPU_GPIO_10 (MAKE_BASE=TRUE) — Required for debug access
74C3	GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]	Required for debug access
74C3	GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]	Required for debug access
74C3	GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]	Required for debug access
74C3	GPU_GPIO_14		TESTIN[8]			NC_GPU_GPIO_14 (MAKE_BASE=TRUE) NO_TEST=TRUE
74C3	GPU_GPIO_15		TESTIN[9]	PWRCNTL		GPU_VCORE_LOW (MAKE_BASE=TRUE) 68B4
74C3	GPU_GPIO_16			SS_IN		GPU_CLK27MSS_IN (MAKE_BASE=TRUE) 34B2 34B4
74C3	GPU_GPIO_17			Thm Mon	Int	NC_GPU_GPIO_17 (MAKE_BASE=TRUE) NO_TEST=TRUE
74D5	GPU_GPIO_18					NC_GPU_GPIO_18
74D5	GPU_GPIO_19					NC_GPU_GPIO_19 (MAKE_BASE=TRUE NO_TEST=TRUE)
74D5	GPU_GPIO_20					NC_GPU_GPIO_20 (MAKE_BASE=TRUE NO_TEST=TRUE)
74D5	GPU_GPIO_21					NC_GPU_GPIO_21 (MAKE_BASE=TRUE NO_TEST=TRUE)
74D5	GPU_GPIO_22					NC_GPU_GPIO_22 (MAKE_BASE=TRUE NO_TEST=TRUE)
74D5	GPU_GPIO_23					NC_GPU_GPIO_23 (MAKE_BASE=TRUE NO_TEST=TRUE)
74D5	GPU_GPIO_24					GPU_MEM_256M (MAKE_BASE=TRUE)
74D5	GPU_GPIO_25					NC_GPU_GPIO_25 (MAKE_BASE=TRUE NO_TEST=TRUE)
74D5	GPU_GPIO_26					NC_GPU_GPIO_26 (MAKE_BASE=TRUE NO_TEST=TRUE)
74D5	GPU_GPIO_27					GPU_MEMID (MAKE_BASE=TRUE)
74D5	GPU_GPIO_28					NC_GPU_GPIO_28 (MAKE_BASE=TRUE NO_TEST=TRUE)
74C5	GPU_GPIO_29					NC_GPU_GPIO_29 (MAKE_BASE=TRUE NO_TEST=TRUE)
74C5	GPU_GPIO_30					NC_GPU_GPIO_30 (MAKE_BASE=TRUE NO_TEST=TRUE)
74C5	GPU_GPIO_31					NC_GPU_GPIO_31 (MAKE_BASE=TRUE NO_TEST=TRUE)
74C5	GPU_GPIO_32					NC_GPU_GPIO_32 (MAKE_BASE=TRUE NO_TEST=TRUE)
74C5	GPU_GPIO_33					NC_GPU_GPIO_33 (MAKE_BASE=TRUE NO_TEST=TRUE)
74C5	GPU_GPIO_34					NC_GPU_GPIO_34 (MAKE_BASE=TRUE NO_TEST=TRUE)

Renamed signals

34B4 34B2 GPU_CLK27M (MAKE_BASE=TRUE) — GPU_XTALIN 74A5

Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_XTALOUT 74A5
NC_ATI_ROMCS_L (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_ATI_ROMCS_L 74A3
NC_FB_A_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_A_MA12 70D5
NC_FB_B_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_B_MA12 70D1
NC_GPU_GENERICA (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICA 74C3
NC_GPU_GENERICB (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICB 74C3
NC_GPU_GENERICC (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICC 74C3
NC_GPU_VGA_R (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_R 75C3
NC_GPU_VGA_G (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_G 75C3
NC_GPU_VGA_B (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_B 75C3
TP_GPU_VGA_HSYNC (MAKE_BASE=TRUE)		GPU_VGA_HSYNC 75B3
TP_GPU_VGA_VSYNC (MAKE_BASE=TRUE)		GPU_VGA_VSYNC 75B3
NC_GPU_TV_Y (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_Y 75B3
NC_GPU_TV_C (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_C 75B3
NC_GPU_TV_COMP (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_COMP 75B3
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_P<3> 75B3
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_N<3> 75B3
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_P<3> 75A3
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_N<3> 75A3
NC_ATI_DVPCLK (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCLK 74C3
NC_ATI_DVPCNTL<2..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCNTL<2..0> 74B3 74C3
NC_ATI_DVPDATA<15..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPDATA<15..0> 74B3

Required for debug access

TP_ATI_DVPDATA<23..16> (MAKE_BASE=TRUE) — ATI_DVPDATA<23..16> 74A3 74B3

Also required: GPIO10 - GPIO13

65A3 =PP3V3_D3C_GPU

R8890 4.7K 5% 1/16W MF-LF 402
R8891 4.7K 5% 1/16W MF-LF 402

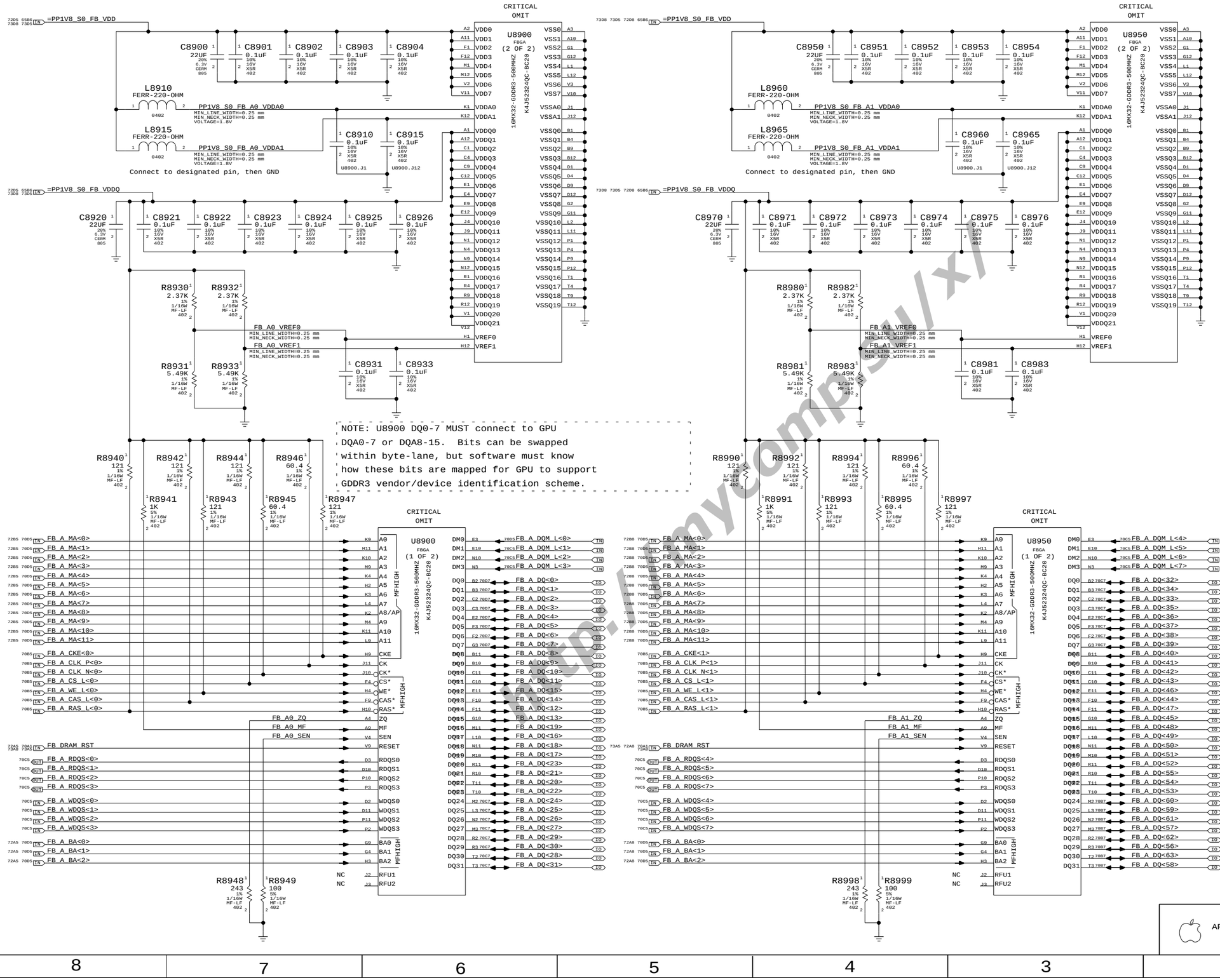
75A3 GPU_DDC_B_CLK
75A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 71 OF 84	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

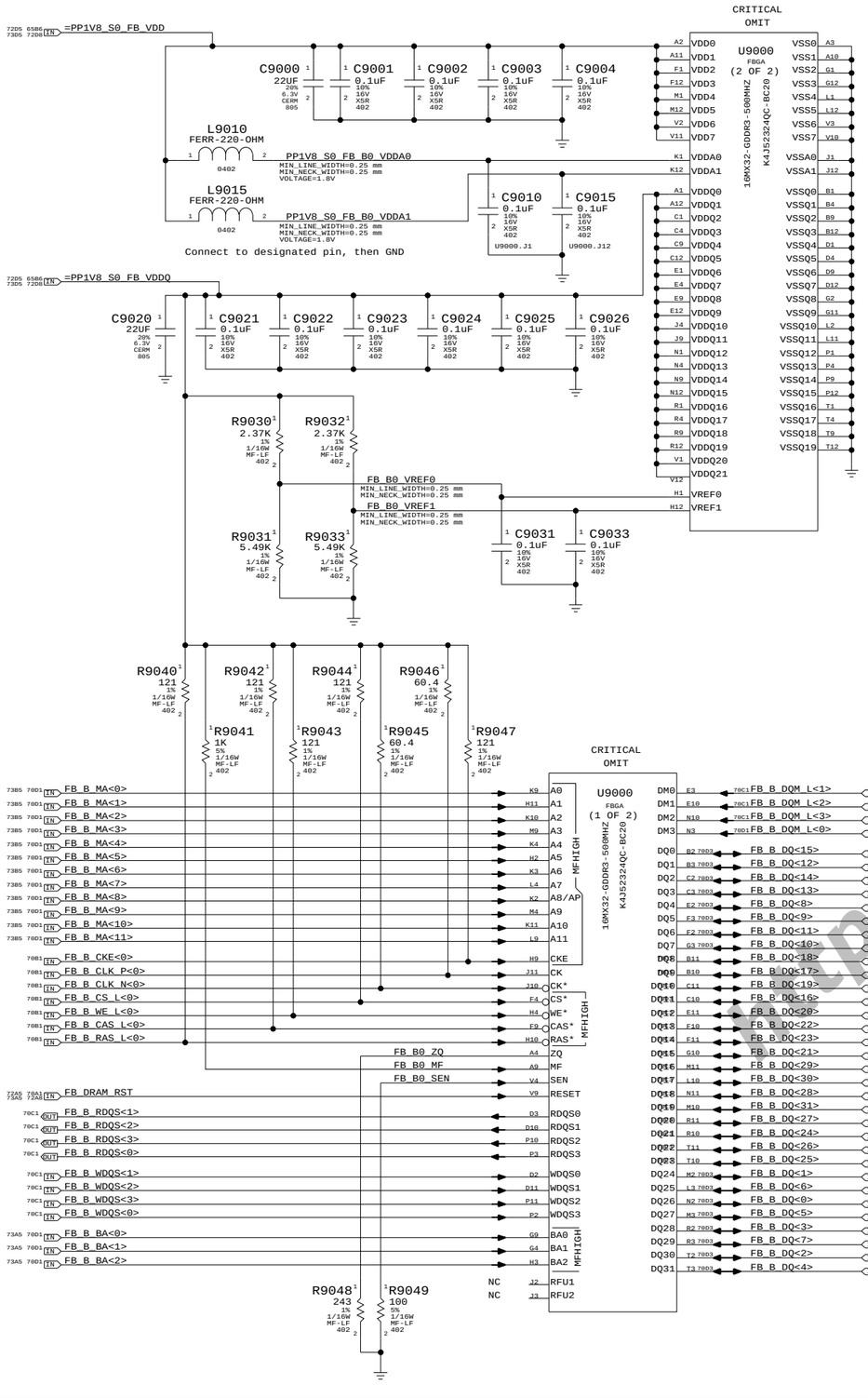
BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 72 OF 84	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

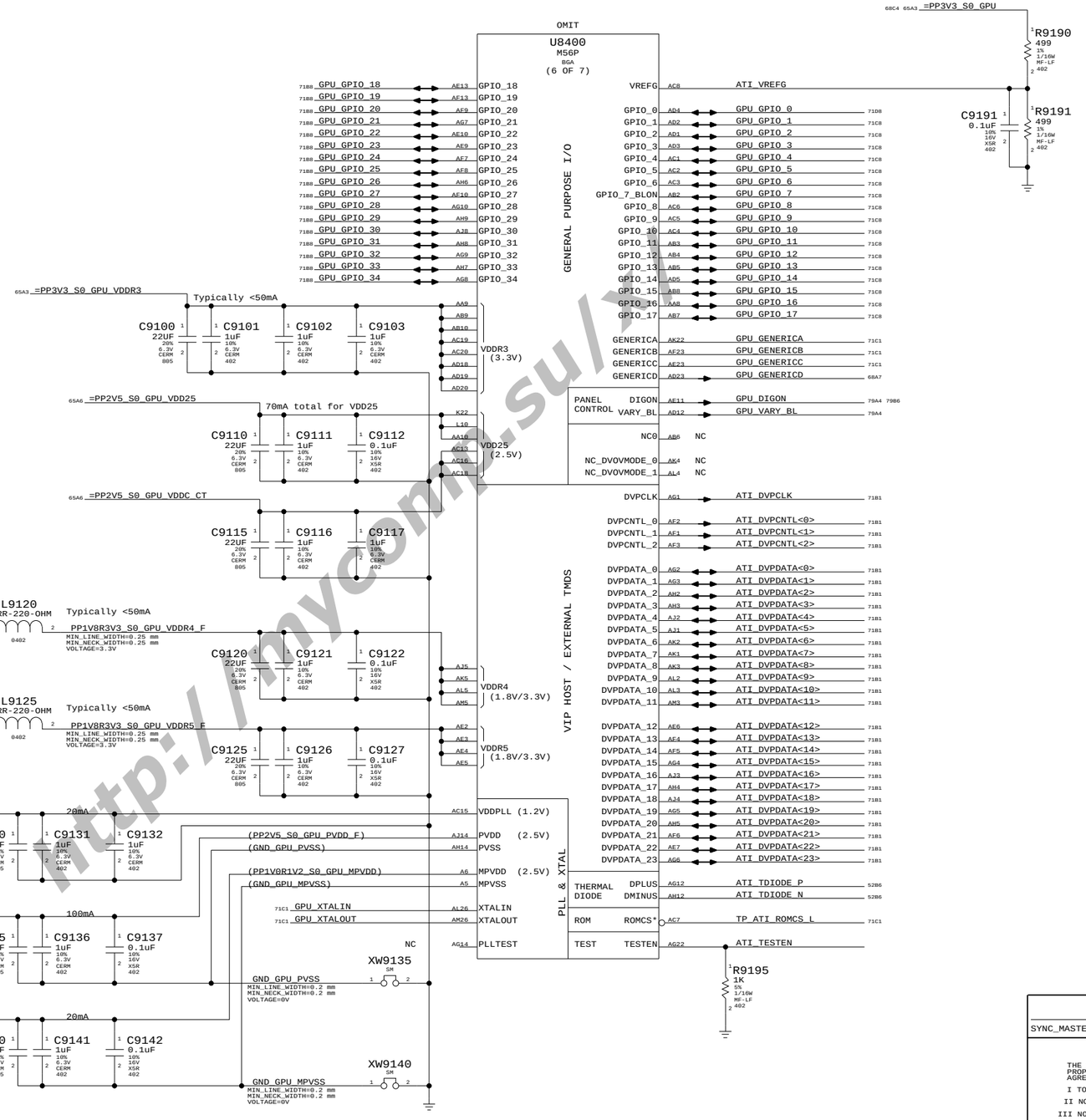
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 73 OF 84	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

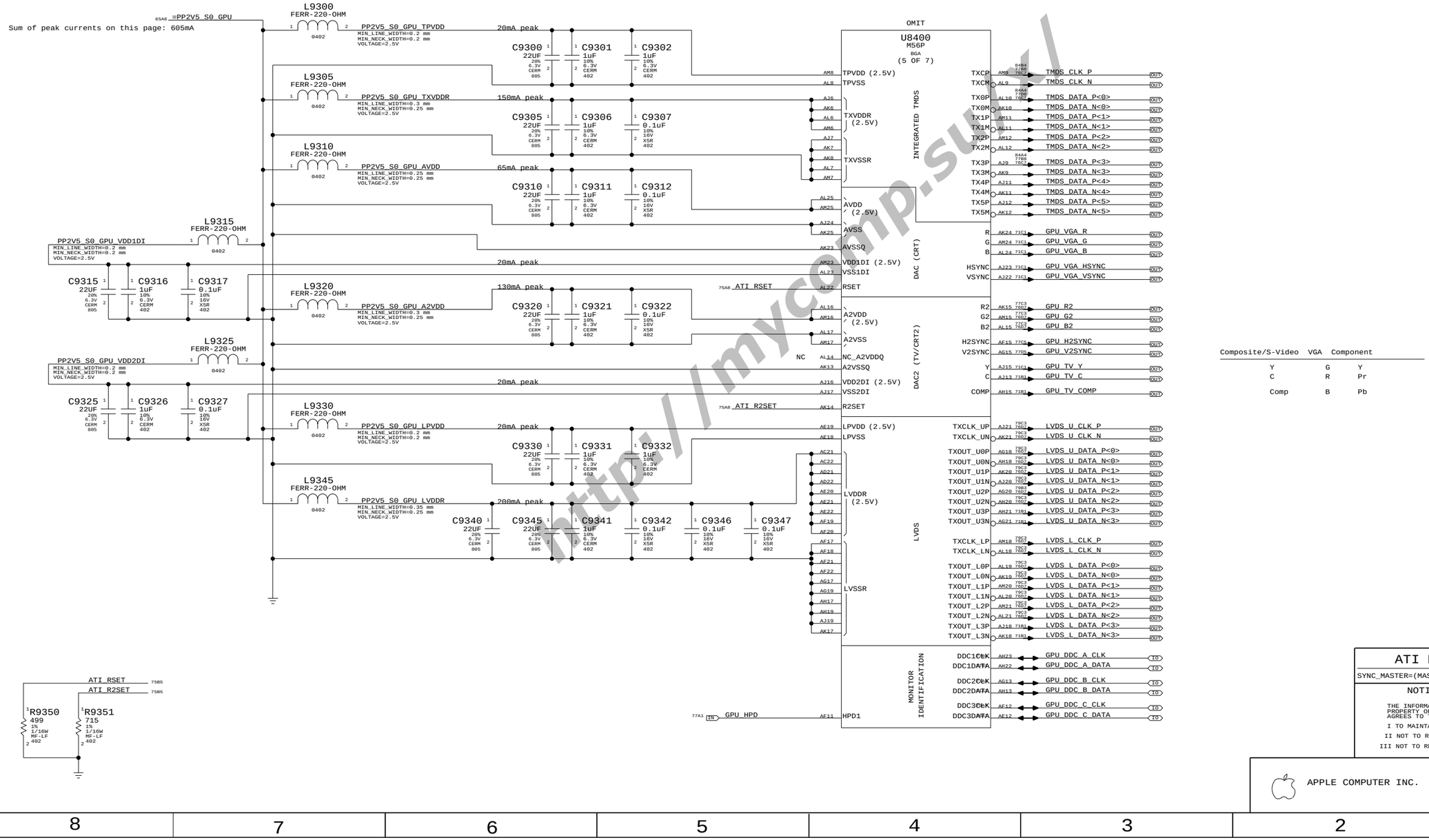
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 74 OF 84	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Video Interfaces

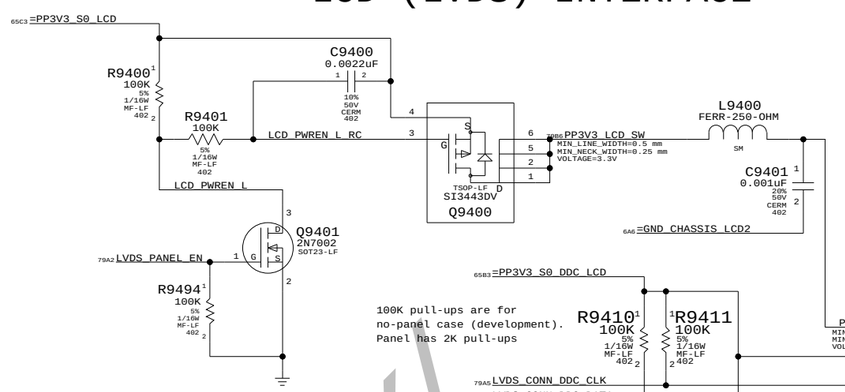
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

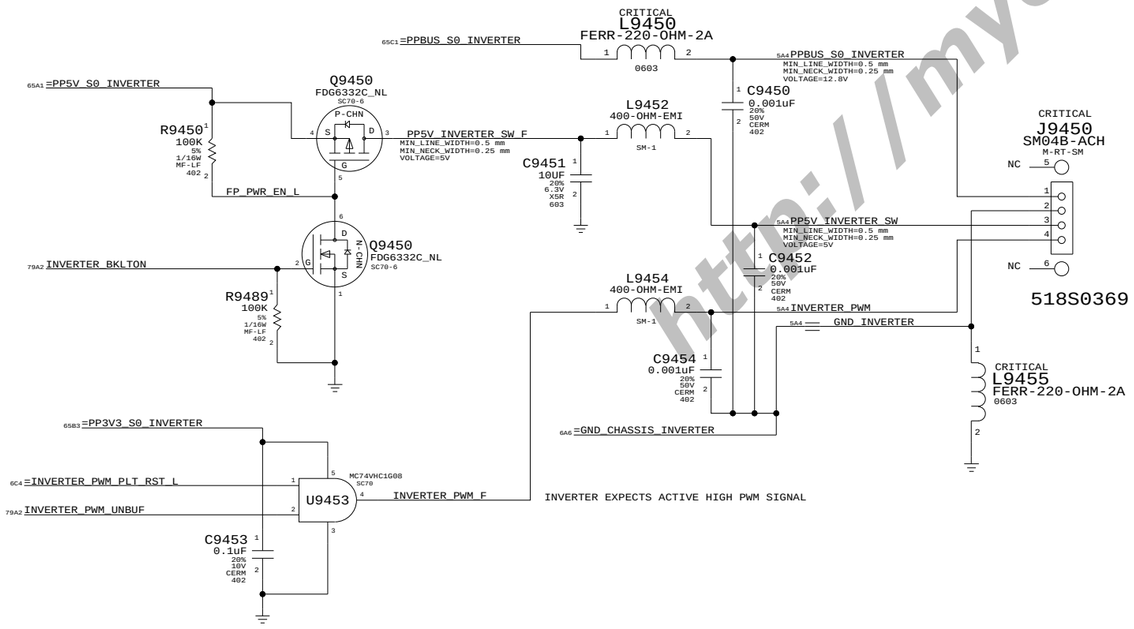
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 75 OF 84	

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	75B3 77C3
	VGA	VGA	GPU_G2	75B3 77C3
	VGA	VGA	GPU_B2	75B3 77C3
	LVDS	LVDS	LVDS_U_CLK_P	75B3 79C3
	LVDS	LVDS	LVDS_U_CLK_N	75B3 79C3
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	75B3 79B3 79C3
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	75B3 79C3
	LVDS	LVDS	LVDS_L_CLK_P	75A3 79C3
	LVDS	LVDS	LVDS_L_CLK_N	75A3 79C3
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	75A3 79C3
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	75A3 79C3
	LVDS	LVDS	LVDS_U_CLK_CONN_P	6B1 76B2 79C1
	LVDS	LVDS	LVDS_U_CLK_CONN_N	6B1 76B2 79C1
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	6B1 76B2 76C2 79C1 79D1
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	6B1 76C2 79C1 79D1
	LVDS	LVDS	LVDS_L_CLK_CONN_P	6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_CLK_CONN_N	6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	6A1 6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	6A1 76C2 79C1
	TMDS	TMDS	TMDS_CLK_P	75C3 77B8 84B4
	TMDS	TMDS	TMDS_CLK_N	75C3 77C8 84B4
	TMDS	TMDS	TMDS_DATA_P<5..3>	75C3 77A8 77B8 84A4
	TMDS	TMDS	TMDS_DATA_N<5..3>	75C3 77A8 77B8 84A4
	TMDS	TMDS	TMDS_DATA_P<2..0>	75C3 77C8 77D8 84A4
	TMDS	TMDS	TMDS_DATA_N<2..0>	75C3 77C8 77D8 84A4



INVERTER INTERFACE



Internal Display Connectors

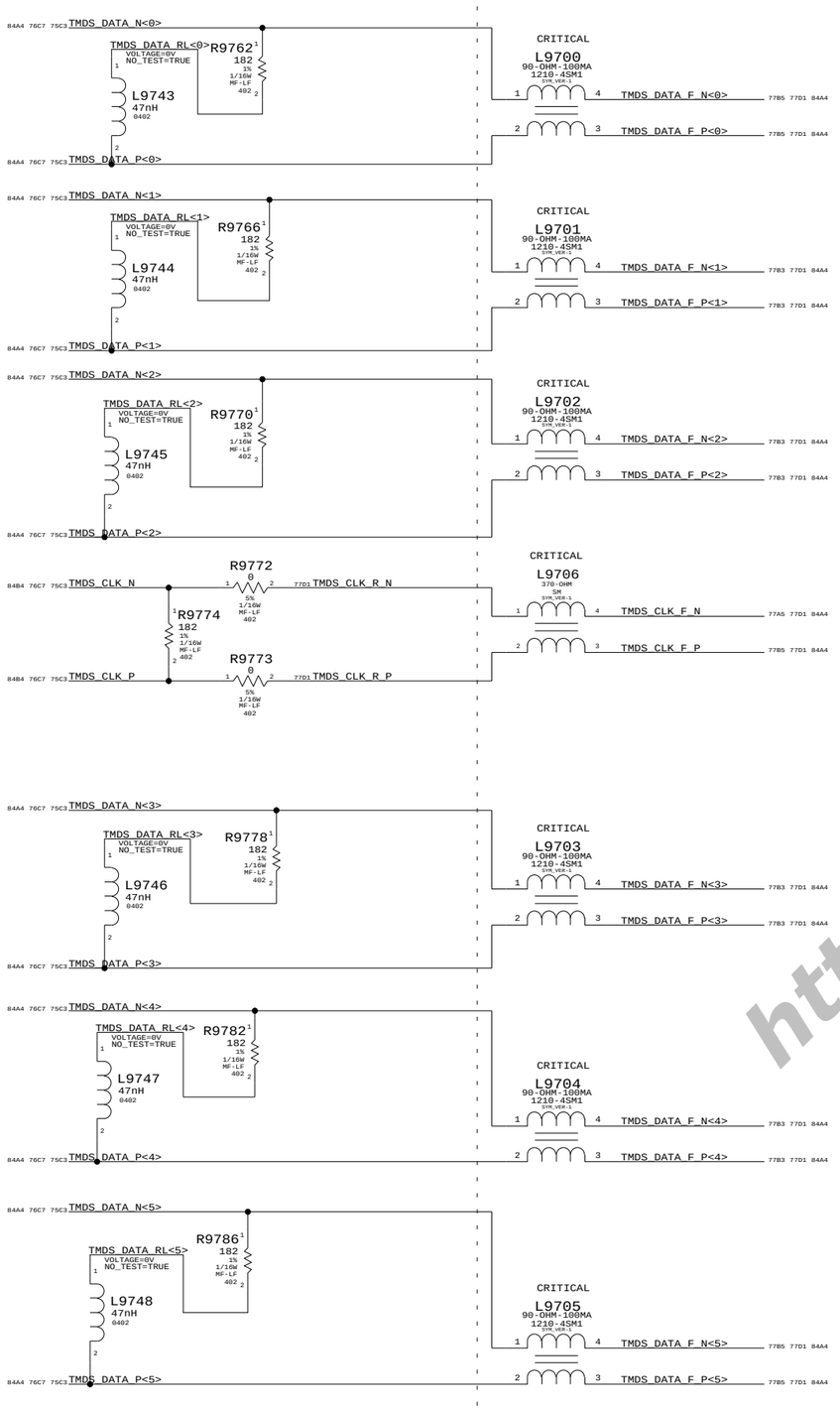
SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

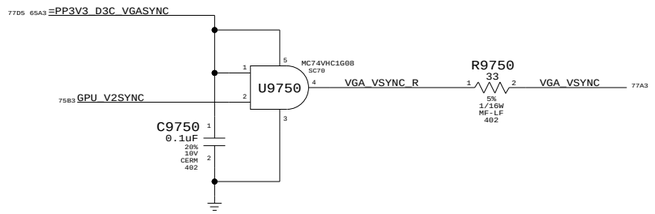
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 76 OF 84	

TMDS Filtering

Place termination components close to GPU, common mode chokes near connector.



VGA SYNC BUFFERS

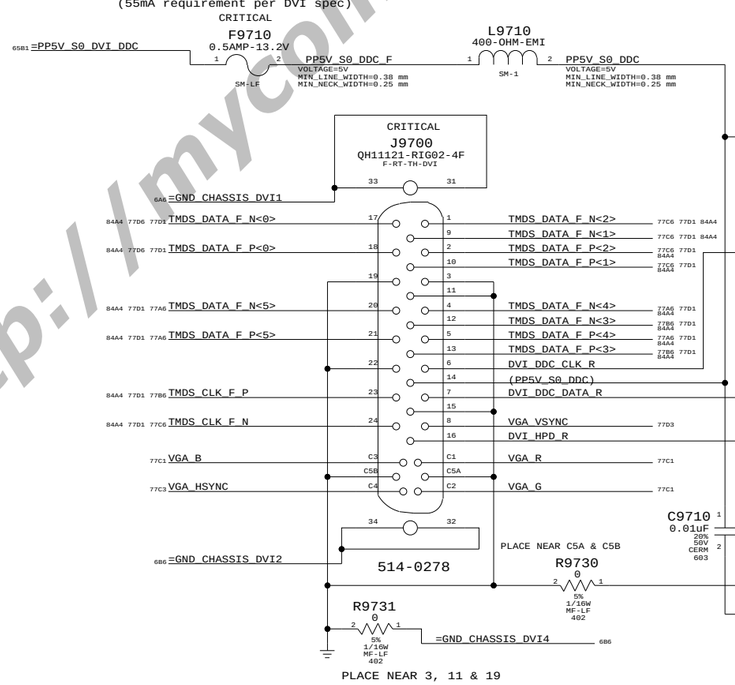


PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

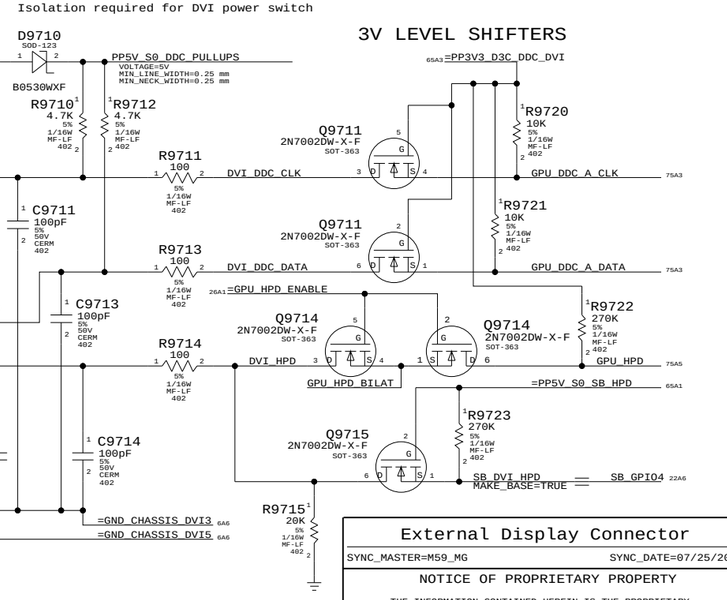
DVI INTERFACE

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

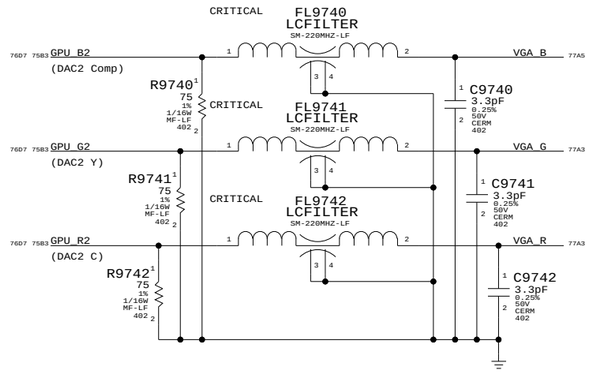


Isolation required for DVI power switch



ANALOG FILTERING

PLACE CLOSE TO CONNECTOR



NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	TMDS	TMDS	TMDS_CLK_R_P 77B7
	TMDS	TMDS	TMDS_CLK_R_N 77C7
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P 77B5 77B6 84A4
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N 77A5 77C6 84A4
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0> 77A6 77B3 77B5 77B6 77C6 77D6 84A4
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0> 77A6 77B3 77B5 77B6 77C6 77D6 84A4

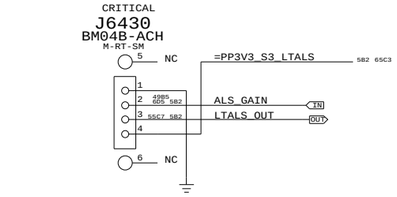
External Display Connector

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

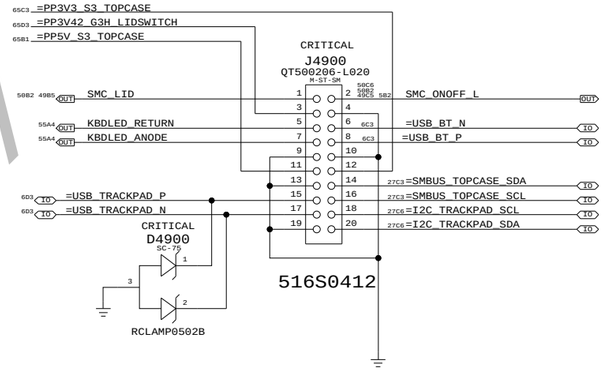
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT: 77 OF 84	

Left ALS Connector



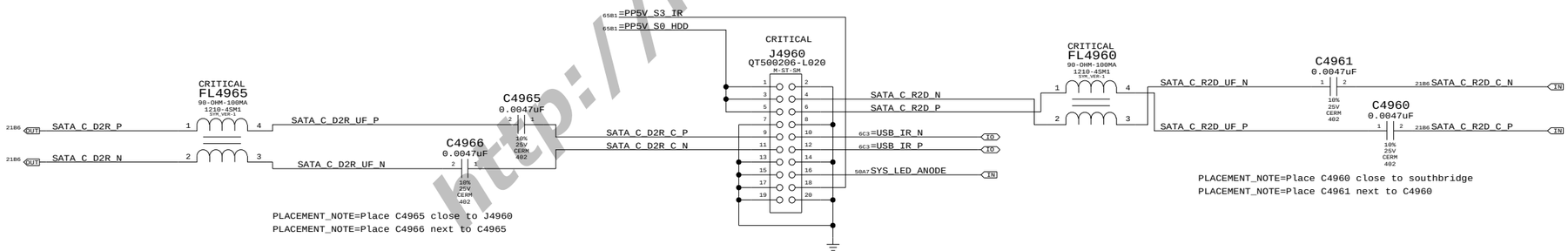
518S0469
white colored version of 518S0369

Top-Case Connector



516S0412

SATA HDD & IR & SIL Flex Connector



PLACEMENT_NOTE=Place C4965 close to J4960
PLACEMENT_NOTE=Place C4966 next to C4965

PLACEMENT_NOTE=Place C4960 close to southbridge
PLACEMENT_NOTE=Place C4961 next to C4960

516S0412

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M59 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE

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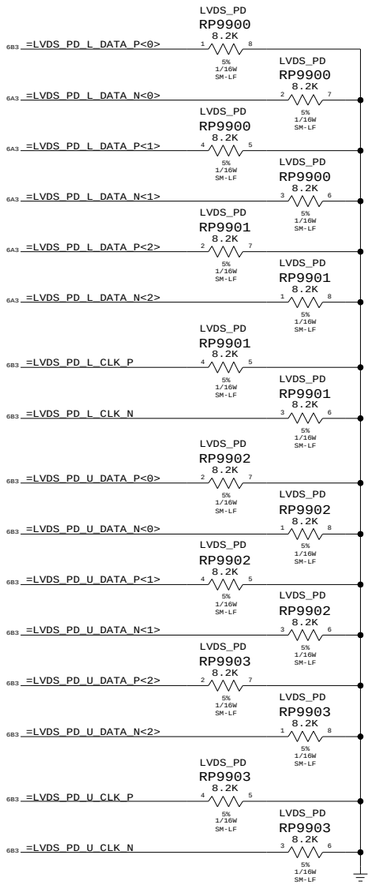
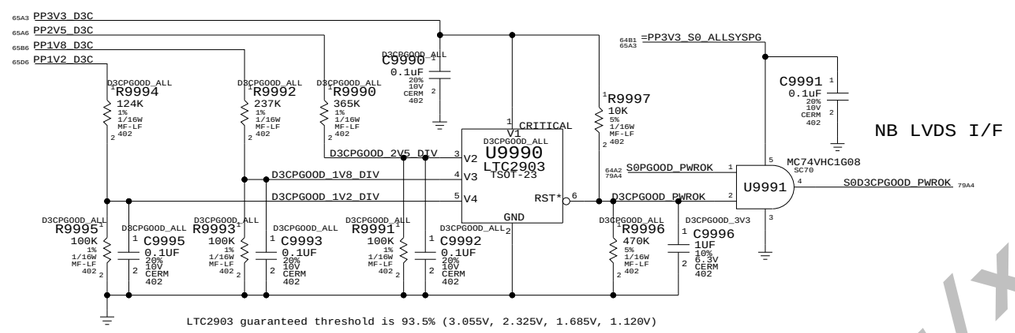
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



PGOOD Monitor for GPU Rails

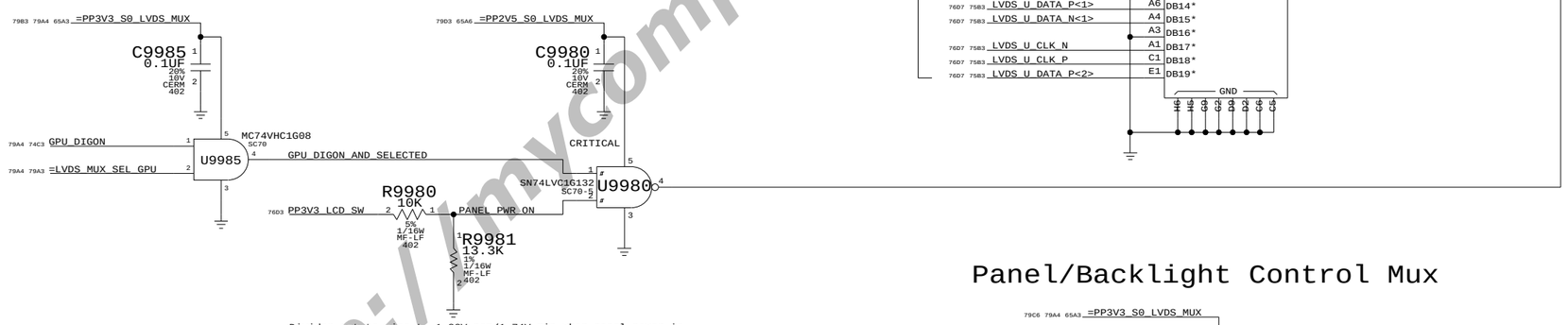
D3CPGOOD_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.
D3CPGOOD_3V3 BOM option uses only PP3V3_D3C to qualify D3CPGOOD.



LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

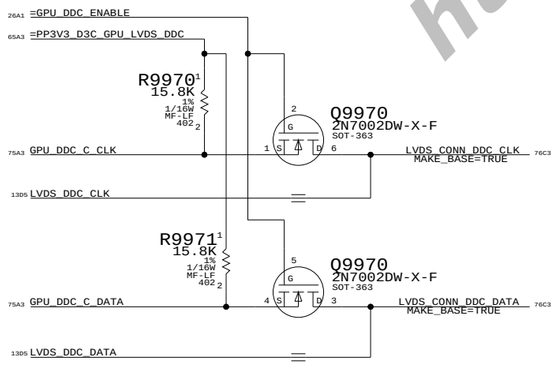
LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

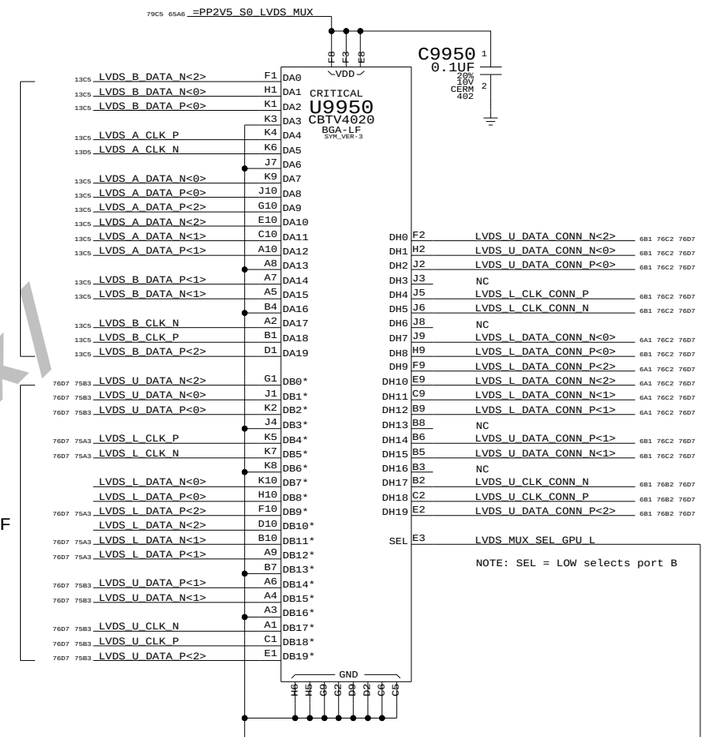


Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

GPU DDC Pass FETs



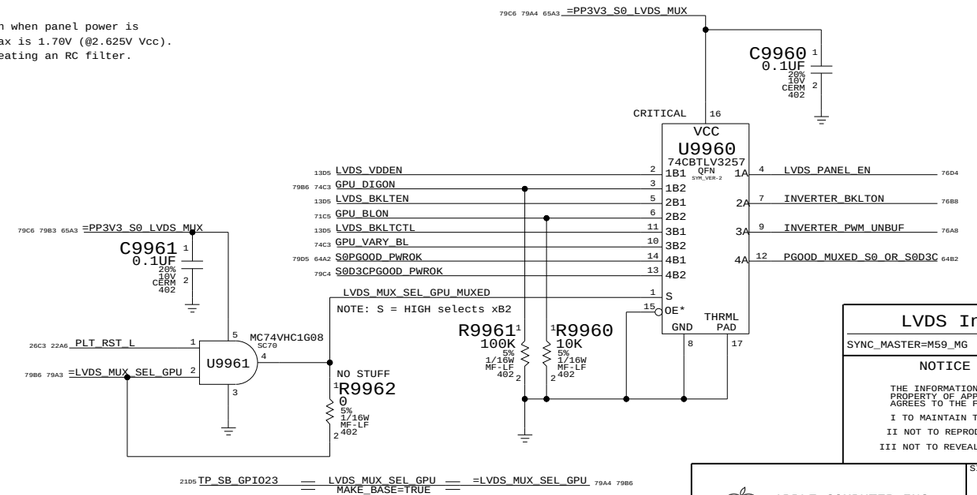
LVDS I/F Mux



NB LVDS I/F

GPU LVDS I/F

Panel/Backlight Control Mux



LVDS Interface Pull-downs	
SYNC_MASTER=M59_MG	SYNC_DATE=08/01/2006

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
	SCALE: NONE	SHT 79 OF 84	

Date	- Radar # - Description

DMS Release #01000

2006/05/26 - 4508681 - Release for Proto

DMS Release #04000

2006/06/30 - 4566939 - Release for EVT

DMS Release #07000

2006/08/07 - 4607952 - Release for DVT

DMS Release #0A000

2006/09/19 - 4726575 - Release for PVT

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 80 OF 84

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	
FSB_ADDR2ADDR	*	=2:1_SPACING	
FSB_ADSTB	*	=3:1_SPACING	
FSB_ADDR2ADSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	
FSB_DATA2DATA	*	=2:1_SPACING	
FSB_DSTB	*	=3:1_SPACING	
FSB_DATA2DSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	
CPU_COMP	*	25 MIL	
CPU_GTLREF	*	25 MIL	
CPU_ITP	*	=2:1_SPACING	
CPU_VCCSENSE	*	25 MIL	

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	
MEM_CTRL2CTRL	*	=2:1_SPACING	
MEM_CTRL2MEM	*	=3:1_SPACING	
MEM_CMD2CMD	*	=1.5:1_SPACING	
MEM_CMD2MEM	*	=3:1_SPACING	
MEM_DATA2DATA	*	=1.5:1_SPACING	
MEM_DATA2MEM	*	=3:1_SPACING	
MEM_DQS2MEM	*	=3:1_SPACING	
MEM_2OTHER	*	25 MIL	

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	
DMI	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	
SATA	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	
USB2_2CLK	*	25 MIL	

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	
SPI	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	
CLK_PCIE	*	20 MIL	
CLK_MED	*	20 MIL	
CLK_SLOW	*	10 MIL	

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	81	84

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_3SS_TO_5SS	*	Y	=3S_OHM_SE	=5S_OHM_SE	=3S_5S_OHM_SE	=STANDARD	=STANDARD
FB_4QS	*	Y	=4Q_OHM_SE	=4Q_OHM_SE	=4Q_OHM_SE	=STANDARD	=STANDARD
FB_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	
FB_CLK	*	=2.5:1_SPACING	
FB_DATA	*	=2.5:1_SPACING	

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	
TMDS	*	=3:1_SPACING	
VGA	*	15 MIL	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	
TMDS_PAIR2PAIR	*	25 MIL	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	
FW	*	=3:1_SPACING	

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-7150	A.0.0

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M59 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	
STANDARD	*	=DEFAULT	
BGA_P1MM	*	=DEFAULT	
BGA_P2MM	*	=DEFAULT	
BGA_P3MM	*	=DEFAULT	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	
1.8:1_SPACING	*	0.18 MM	
2:1_SPACING	*	0.2 MM	
2.5:1_SPACING	*	0.25 MM	
3:1_SPACING	*	0.3 MM	
4:1_SPACING	*	0.4 MM	

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	
1.8:1_SPACING	ISL2,ISL11	0.1 MM	
2:1_SPACING	ISL2,ISL11	0.1 MM	
2.5:1_SPACING	ISL2,ISL11	0.1 MM	
3:1_SPACING	ISL2,ISL11	0.1 MM	
4:1_SPACING	ISL2,ISL11	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	
CLK_PCIE	ISL2,ISL11	0.1 MM	
CLK_MED	ISL2,ISL11	0.1 MM	
CLK_SLOW	ISL2,ISL11	0.1 MM	
CPU_COMP	ISL2,ISL11	0.1 MM	
CPU_GTLREF	ISL2,ISL11	0.1 MM	
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	
DMI	ISL2,ISL11	0.1 MM	
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
MEM_2OTHER	ISL2,ISL11	0.1 MM	
PCIE	ISL2,ISL11	0.1 MM	
SATA	ISL2,ISL11	0.1 MM	
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
VGA	ISL2,ISL11	0.1 MM	

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_5SS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4SS OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_7OD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_8SD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M59 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5D5 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5D5 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5D5 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5D5 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14B7 23C3 59C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	59C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 34D3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 34D3
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 84B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 84B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 59B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 59A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	59A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	59A3

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 47B6
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 47B6
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 47B3
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 47B6
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 47B6

TMDS	TMDS	TMDS_CLK_P	75C3 76C7 77B8
TMDS	TMDS	TMDS_CLK_N	75C3 76C7 77C8
TMDS	TMDS	TMDS_DATA_P<5..3>	75C3 76C7 77A8 77B8
TMDS	TMDS	TMDS_DATA_N<5..3>	75C3 76C7 77A8 77B8
TMDS	TMDS	TMDS_DATA_P<2..0>	75C3 76C7 77C8 77D8
TMDS	TMDS	TMDS_DATA_N<2..0>	75C3 76C7 77C8 77D8
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	77B5 77B6 77D1
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	77A5 77C6 77D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	77A6 77B3 77B5 77B6 77D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	77A6 77B3 77B5 77B6 77D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	77B3 77B5 77C6 77D1 77D6
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	77B3 77B5 77C6 77D1 77D6

M59 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 84 OF 84	