1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

M9 MLB

4/12/2006

PVT

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7023	1	SCHEM,MLB,M9	SCH	CRITICAL	
820-2023	1	PCBF,MLB,M9	PCB	CRITICAL	

DRAWING
TITLE=SULLY
ABBREV=DRAWING
LAST_MODIFIED=Wed Apr 12 12:10:18 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

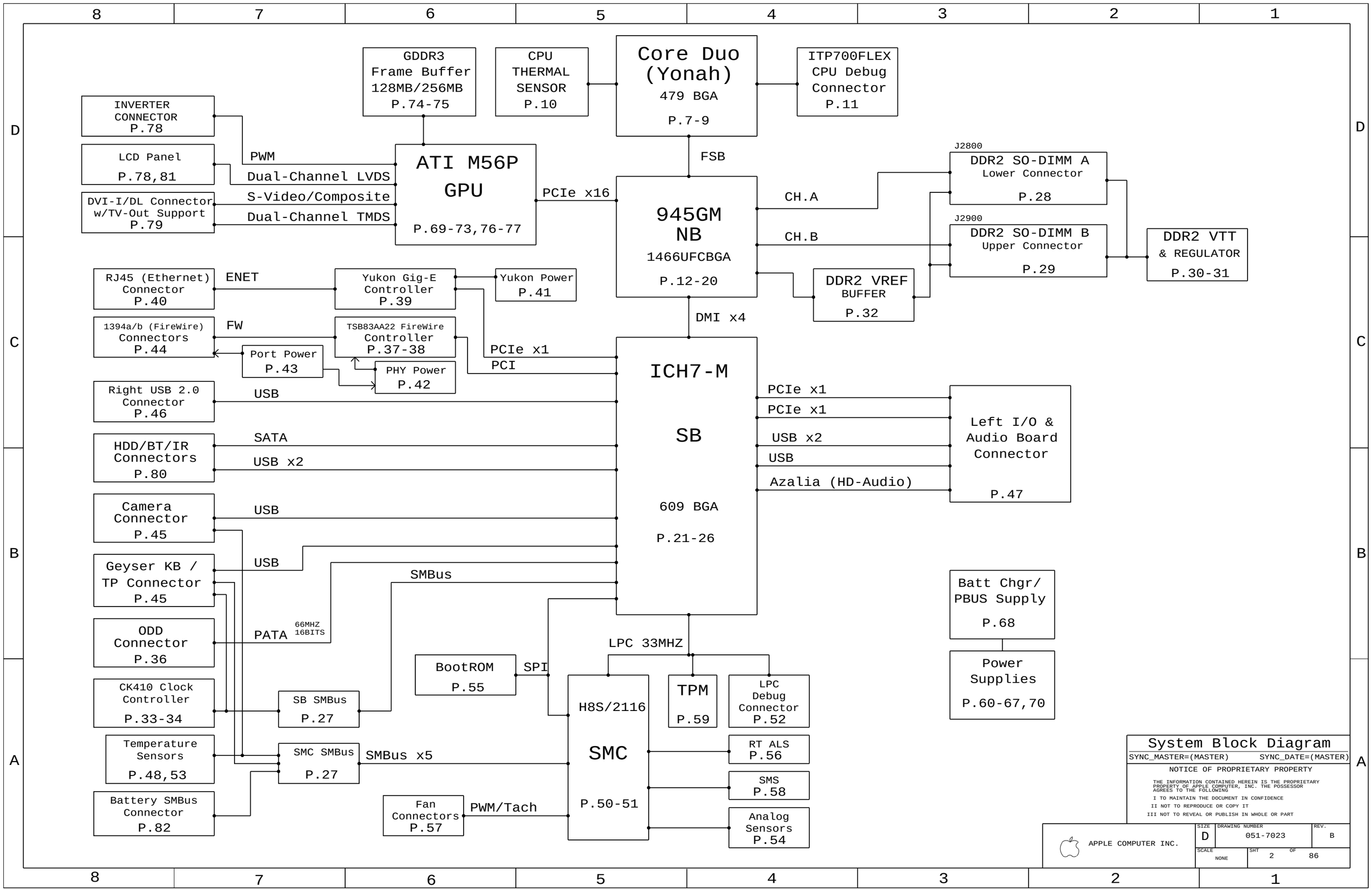
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,M9

DRAWING NUMBER 051-7023 REV. B

SHT 1 OF 86


GDDR3
Frame Buffer
128MB/256MB
P.74-75
CPU
THERMAL
SENSOR
P.10
Core Duo
(Yonah)
479 BGA
P.7-9
ITP700FLEX
CPU Debug
Connector
P.11
INVERTER
CONNECTOR
P.78
LCD Panel
P.78,81
DVI-I/DL Connector
w/TV-Out Support
P.79
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USB
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TP Connector
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ODD
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PATA
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16BITS
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System Block Diagram
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SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
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APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-7023
REV.
B
SCALE
NONE
SHT
2
OF
86

J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V

U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V

J8200
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V

SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
NC
PP5V_S5
5.0V
PP1V5_S0
1.5V

Q7610
PP5V_S3
5.0V
PM_SLP_S4_LS5V

Q7615
PP5V_S0
5.0V
PM_SLP_S3_LS5V

IMVP_VR_ON
IMVP_PWRGD_IN
U7530
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
VR_PWRGOOD_DELAY
PPVCORE_S0_CPU
?V

J5500
Inverter Connector
PM_SLP_S4_L

U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
NC
PP1V8_S3
1.8V

PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V

SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
RSMRST_PWRGD
PP3V3_S5
3.3V

PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
IMVP_PWRGD_IN/ALL_SYS_PWRGD
PP1V05_S0
1.05V

PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
NC
PPVCORE_S0_GPU
1.2V - 1.0V

Q7845
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L

Q7945
PP3V3_S3
3.3V
PM_SLP_S4_LS5V

U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
NC
PP2V5_S3
2.5V

Q7720
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L

U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
NC
PP1V2_S3
1.2V

Q7770
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L

Q7947
PP3V3_S0
3.3V
PM_SLP_S3_LS5V

Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN

Power Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	3	86

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7406	PCBA,2.16GHz,256VRAM,M9	VRAM_256SAM,M9_COMMON,CPU_2_16GHZ,EEE_UP1

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG
VRAM_128HY	GPU_MEM_HYNIX,VRAM_128_HYNIX
VRAM_256HY	GPU_MEM_HYNIX,GPU_MEM_256M,VRAM_256_HYNIX

BOM GROUP	BOM OPTIONS
M9_COMMON	ALTERNATE,COMMON,M9_COMMON1,M9_COMMON2,M9_COMMON3,M9_COMMON4,M9_DEBUG
M9_COMMON1	ENETPWR_S3AC,GPUTHM_A_GPU,GPU_BB_CTL,HSTHMSNS_HAS,INVERTER_BUF,ONEWIRE_PU
M9_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M9_COMMON3	LVDS_PD,M56_REV_B26_LP,FW_B_BILINGUAL,FW_A_DS_ONLY,FW_PORT_FAULT_PU,FW_PLTRST_GATED
M9_COMMON4	USB_G_OC_PU,LIO_TEMP,TMDS_PEAKING_IND,BOOTROM_DEVEL,SMC_DEVEL
M9_DEBUG	ITP,LPCPLUS

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNZ]	CRITICAL	EEE_UNZ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP0]	CRITICAL	EEE_UP0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP1]	CRITICAL	EEE_UP1
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP2]	CRITICAL	EEE_UP2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UYU]	CRITICAL	EEE_UYU

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0315	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B26_LP
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445		ALL	Vishay 2nd source
128S0083	128S0073		C2516	1.86 max alt to 1.9 max
128S0093	128S0092		ALL	Kemet is alt to Sanyo
128S0060	128S0094		ALL	Sanyo is alt to Panasonic
128S0095	128S0094		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	C2 package is alt to C3

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1876	1	IC,SMC,PRGRM,M9	U5800	CRITICAL	SMC_DEVEL
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1828	1	IC,EFI,BOOTROM DEVELOPMENT,M9	U6301	CRITICAL	BOOTROM_DEVEL
341S1829	1	IC,EFI,BOOTROM FINAL,M9	U6301	CRITICAL	BOOTROM_FINAL
353S1465	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3282	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_1_83GHZ
337S3267	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_2_0GHZ
337S3268	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_2_16GHZ
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	

BOM Configuration

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7023 | REV. B

SCALE NONE | SHT 4 OF 86

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	60
TRUE		P5VS5_RUNSS	61 65
TRUE		P1V5S0_RUNSS	61 65
TRUE		P2V5S3_MODE	62
TRUE		P2V5S3_SHDNRT	62
TRUE		P1V2S3_RT	62
TRUE		P1V2S3_RUNSS	41 62
TRUE		P1V8S3_COMP	63
TRUE		P1V8S3_FSET	63
TRUE		P3V3S5_COMP	64
TRUE		P3V3S5_FSET	64
TRUE		P1V05S0_COMP	64
TRUE		P1V05S0_FSET	64
TRUE		P3V42G3H_FB	65
TRUE		GPUVCORE_COMP	70
TRUE		GPUVCORE_FSET	70
TRUE		GPUBBP_ADJ	70

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 86
TRUE		FSB_ADS_L	7 12 86
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 86
TRUE		FSB_BNR_L	7 12 86
TRUE		FSB_BREQ0_L	7 12 86
TRUE		FSB_D_L<63..0>	7 12 86
TRUE		FSB_DBSY_L	7 12 86
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 86
TRUE		FSB_DRDY_L	7 12 86
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 86
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 86
TRUE		FSB_HIT_L	7 12 86
TRUE		FSB_HITM_L	7 12 86
TRUE		FSB_LOCK_L	7 12 86
TRUE		FSB_REQ_L<4..0>	7 12 86

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

Power Nets

FUNC_TEST		
TRUE	PP0V9_S0	30 31 65 66
TRUE	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24 29 34 54 64 66
TRUE	PP1V2_S0	62 65 66 69 76
TRUE	PP1V2_S3	5 39 62 66
TRUE	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 61 65 66
TRUE	PP1V8_S0	63 65 66 71 72 74 75
TRUE	PP1V8_S3	5 14 16 19 28 29 31 32 37 54 63 66
TRUE	PP2V5_S0	17 19 62 65 66 76 77
TRUE	PP2V5_S3	5 39 62 66
TRUE	PP3V3_S0	61 63 56 57 59 60 64 65 66 70
TRUE	PP3V3_S3	5 16 14 17 19 20 21 23 24 26 28 27 28 29 33 34 36 37 43 4870
TRUE	PP3V3_S5	27 32 37 41 45 51 56 58 59 62 63 64 66 80
TRUE	PP5V_S0	11 22 23 24 25 26 55 62 64 65 66 78 79 80
TRUE	PP5V_S3	5 25 31 36 42 47 52 54 56 57 60 61 65 66 67 70 78
TRUE	PP5V_S5	5 45 51 61 66 80
TRUE	PPBUS_G3H	5 25 46 51 61 63 64 65 66 67 70
TRUE	GND	5 41 43 47 54 60 61 63 64 66 68 70 78

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST		
TRUE	IMVP_VR_ON	50 60
TRUE	IMVP_DPRSLPVR	60 86
TRUE	PM_SLP_S3_L	23 32 39 43 50 54 64 65
TRUE	PM_SLP_S3BATT	41
TRUE	PM_SLP_S4_L	5 23 41 46 47 50 63 65
TRUE	PM_SLP_S5_L	23 50 51
TRUE	P1V5P1V05S0_PGOOD	60 64 65
TRUE	CPU_DPRSTP_L	7 21 60
TRUE	IMVP6_VID<6..0>	9 60
TRUE	FSB_CLK_CPU_N	7 34
TRUE	FSB_CLK_CPU_P	7 34
TRUE	PLT_RST_L	5 14 22 26
TRUE	PLT_RST_L	5 14 22 26
TRUE	PEG_RESET_L	26 69
TRUE	SMC_LRESET_L	26 50
TRUE	TPM_LRESET_L	26 59
TRUE	CPU_STPCLK_L	7 21 86
TRUE	FSB_CLK_NB_P	12 34
TRUE	FSB_CLK_NB_N	12 34
TRUE	CLK_NB_OE_L	14 33
TRUE	NB_CLK100M_GCLKIN_P	14 34
TRUE	NB_CLK100M_GCLKIN_N	14 34
TRUE	GND	
TRUE	GND	
TRUE	GND	
TRUE	GND	
TRUE	CPU_THERMTRIP_R	21
TRUE	TP_SB_SUS_CLK	6 23

MAC-1 TPs

FUNC_TEST		
TRUE	CPU_PWRGD	7 21 86
TRUE	TP_CPU_CPUSLP_L	21
TRUE	PM_DPRSLPVR	14 23 60 86
TRUE	CPU_DPSLP_L	7 21 86
TRUE	PM_LAN_ENABLE	23 50
TRUE	PCI_RST_L	22 37
TRUE	PM_RSMRST_L	23 50
TRUE	PM_SB_PWROK	23 26
TRUE	SB_RTC_RST_L	21 26
TRUE	PM_STPCPU_L	23 33
TRUE	PM_STPPCI_L	23 33
TRUE	VR_PWRGD_CK410	23 26
TRUE	VR_PWRGOOD_DELAY	14 26 60
TRUE	FSB_CPURST_L	7 11 12 86
TRUE	FSB_SLPCPU_L	7 12
TRUE	FSB_DPWR_L	7 12 86
TRUE	NB_SB_SYNC_L	14 22
TRUE	PP2V5_S0_GPU_TPVDD	77
TRUE	PP2V5_S0_GPU_TXVDDR	77
TRUE	PP2V5_S0_GPU_AVDD	77
TRUE	PP2V5_S0_GPU_A2VDD	77
TRUE	PP2V5_S0_GPU_LPVDD	77
TRUE	PP2V5_S0_GPU_LVDDR	60 64 65 66 70 78 79
TRUE	PP3V3_S0	23 32 39 43 50 54 64 65 (=PP3V3_S0_CK410)
TRUE	PP3V3_S0_CK410_VDD48	5 7 8 9 11 12 13 16 17 19 21 24 29 34 54 64 66
TRUE	PP3V3_S0_CK410_VDD_PCI	10 20 21 23 25 27 28 33 34 36 37 43 48 51 53 56 57 59
TRUE	PP3V3_S0_CK410_VDD_REF	33
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC	33
TRUE	PP3V3_S0_CK410_VDDA	33
TRUE	PP3V3_FWPHY	6 38 42 43 44
TRUE	PP3V3_FWPHY_AVDD	38
TRUE	PP3V3_FWPHY_PLLVDD	38
TRUE	PP1V95_FWPHY	6 38 42
TRUE	PP1V95_FWPHY_PLLVDD	38
TRUE	PP1V2_S3	5 39 62 66 (=PP1V2_S3_ENET)
TRUE	PP3V3_S3AC	39 41 66 (=PP3V3_S3_ENET)
TRUE	PP2V5_S3	5 39 62 66 (=PP2V5_S3_ENET)
TRUE	PP2V5_S3_ENET_AVDD	39 40

Fan Connectors

FUNC_TEST		
TRUE	PP5V_S0	67 70 78 79 80 5 25 31 36 42 47 52 54 56 57 60 61 65 66
TRUE	FAN_LT_PWM	57
TRUE	FAN_LT_TACH	57
TRUE	FAN_RT_PWM	57
TRUE	FAN_RT_TACH	57

LPC+ Debug Connector

FUNC_TEST		
TRUE	PP3V42_G3H	5 26 27 35 45 50 51 52 54 65 66 67 68
TRUE	PP5V_S0	67 70 78 79 80 5 25 31 36 42 47 52 54 56 57 60 61 65 66
TRUE	LPC_AD<0>	21 50 52 59
TRUE	LPC_AD<1>	21 50 52 59
TRUE	LPC_FRAME_L	21 50 52 59
TRUE	PM_CLKRUN_L	23 50 52 59
TRUE	BOOT_LPC_SPI_L	22 50 52
TRUE	SMC_TMS	50 51 52
TRUE	DEBUG_RST_L	26 52
TRUE	SMC_TRST_L	50 52
TRUE	SMC_TDO	50 51 52
TRUE	SMC_MD1	50 52
TRUE	SMC_TX_L	50 51 52
TRUE	FWH_INIT_L	21 50 51 52
TRUE	PCI_CLK_PORT80_LPC	34 52
TRUE	LPC_AD<2>	21 50 52 59
TRUE	LPC_AD<3>	21 50 52 59
TRUE	INT_SERIRQ	23 50 52 59
TRUE	PM_SUS_STAT_L	23 50 51 52 59
TRUE	SMC_TDI	50 51 52
TRUE	SMC_TCK	50 51 52
TRUE	SMC_RST_L	50 51 52
TRUE	SMC_NMI	50 52
TRUE	SMC_RX_L	50 51 52
TRUE	SV_SET_UP	23 52

Resistor Calibration

FUNC_TEST		
TRUE	PP5V_S0	67 70 78 79 80 5 25 31 36 42 47 52 54 56 57 60 61 65 66
TRUE	PP1V8_S3	5 14 16 19 28 29 31 32 37 54 63 66
TRUE	PP1V05_S0	64 66 5 7 8 9 11 12 13 16 17 19 21 24 29 34 54
TRUE	PPVCORE_S0_CPU	8 9 54 60 66
TRUE	PPVCORE_S0_GPU	54 66 70 71 76
TRUE	ISENSE_CAL_EN	50 54
TRUE	GND	

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST		
TRUE	PP5V_S3	5 45 51 61 66 80
TRUE	USB2_CAMERA_N	6 22 45
TRUE	USB2_CAMERA_P	6 22 45
TRUE	SMBUS_SMC_0_S0_SDA	27 45 50 53
TRUE	SMBUS_SMC_0_S0_SCL	27 50 53

Thermal Sensors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	53
TRUE	HSTHMSNS_DX_N	53
TRUE	RSFSTHMSNS_D_P	53
TRUE	RSFSTHMSNS_D_N	53

SMC TPs

FUNC_TEST		
TRUE	PM_SYSRST_L	23 26 50
TRUE	SMC_ONOFF_L	45 50 51 54

Battery Connector

FUNC_TEST		
TRUE	BATT_POS	67 68
TRUE	BATT_NEG	67 68
TRUE	SMC_BS_ALRT_L	50 51 67
TRUE	SMBUS_SMC_BSA_SCL	27 50 67
TRUE	SMBUS_SMC_BSA_SDA	27 50 67

Left I/O Data Connector

FUNC_TEST		
TRUE	PP1V5_S0	65 66 5 8 9 13 16 17 19 24 54 56 57 60 61 63 64 66 68 70 78
TRUE	PPBUS_G3H	5 41 43 47 54 60 61 63 64 66 68 70 78
TRUE	PP3V42_G3H	5 26 27 35 45 50 51 52 54 65 66
TRUE	PP5V_S0_AUDIO	67 68
TRUE	GND_AUDIO	47
TRUE	ALS_GAIN	6 47 50
TRUE	LTALS_OUT	47 56
TRUE	ACZ_SDATAIN<0>	21 47 86
TRUE	ACZ_SDATAOUT	21 47 86
TRUE	ACZ_BITCLK	21 47 86
TRUE	ACZ_RST_L	21 47 86
TRUE	EXCARD_OC_L	6 22 47 51
TRUE	LTUSB_OC_L	6 22 47
TRUE	LT2USB_OC_L	6 22 47
TRUE	PM_SLP_S3_LS5V	47 61 65
TRUE	PM_SLP_S4_L	5 23 41 46 47 50 63 65
TRUE	SYS_ONEWIRE	47 50 51
TRUE	MINI_CLKREQ_L	6 33 34 47
TRUE	SMC_EXCARD_CP	47 50 51
TRUE	EXCARD_CLKREQ_L	6 33 34 47
TRUE	SMC_EXCARD_PWR_EN	47 50
TRUE	LIO_PLT_RESET_L	26 47
TRUE	ACZ_SYNC	21 47 86
TRUE	USB2_LT_N	6 22 47
TRUE	USB2_LT_P	6 22 47
TRUE	USB2_EXCARD_N	6 22 47
TRUE	USB2_EXCARD_P	6 22 47
TRUE	PCIE_EXCARD_R2D_C_N	47 49
TRUE	PCIE_EXCARD_R2D_C_P	47 49
TRUE	PCIE_EXCARD_D2R_N	22 47 49
TRUE	PCIE_EXCARD_D2R_P	22 47 49
TRUE	PCIE_CLK100M_EXCARD_P	34 47
TRUE	PCIE_CLK100M_EXCARD_N	34 47
TRUE	USB2_LT2_N	6 22 47
TRUE	USB2_LT2_P	6 22 47
TRUE	PCIE_MINI_R2D_C_N	47 49
TRUE	PCIE_MINI_R2D_C_P	47 49
TRUE	PCIE_MINI_D2R_N	22 47 49
TRUE	PCIE_MINI_D2R_P	22 47 49
TRUE	PCIE_CLK100M_MINI_P	34 47
TRUE	PCIE_CLK100M_MINI_N	34 47
TRUE	SMBUS_SB_SCL	23 27 28 29 33 43 47
TRUE	SMBUS_SB_SDA	23 27 28 29 33 43 47
TRUE	PCIE_WAKE_L	23 39 47
TRUE	SMC_BC_ACOK	47 50 51 67 68

Left I/O Power Connector

FUNC_TEST		
TRUE	PP18V5_DCIN	67
TRUE	PP5V_S5	5 25 46 51 61 63 64 65 66 67 70
TRUE	PP5V_S0_AUDIO_PWR	67
TRUE	GND_AUDIO_PWR	67
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
	SCALE: NONE	SHT 5 OF 86	

NC_CPU_A32_L
NC_CPU_A33_L
NC_CPU_A34_L
NC_CPU_A35_L
NC_CPU_A36_L
NC_CPU_A37_L
NC_CPU_A38_L
NC_CPU_A39_L
NC_CPU_APM0_L
NC_CPU_APM1_L
NC_CPU_EXTBREF
NC_CPU_HFPLL
NC_CPU_SPARE0
NC_CPU_SPARE1
NC_CPU_SPARE2
NC_CPU_SPARE4

NC_MEM_A_A<15..14>
NC_MEM_B_A<15..14>
TP_NB_CFG<4..3>
TP_NB_CFG<6>
TP_NB_CFG<8>
TP_NB_CFG<11..10>
TP_NB_CFG<15..14>
TP_NB_CFG<17>

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12>
TP_SB_SUS_CLK

R0600
0
5%
1/16W
MF-LF
402
ALS_GAIN
RTALS_GAIN

NC_ENET_CTRL12
NC_ENET_CTRL25

Ethernet Powr Management Support

ENET_LOM_DISABLE
R0690
0
5%
1/16W
MF-LF
402
SB_GPIO30
ENET_LOM_DIS_L

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

NOTE: Software not expected to implement this feature

USB Port "A" (Debug Port) = Right USB 2.0 Port

USB2_RT_P
USB2_RT_N
RTUSB_OC_L

USB Port "B" = Trackpad (Geyser)

USB_TRACKPAD_P
USB_TRACKPAD_N
UNUSED_USB_B_OC_L

USB Port "C" = Left USB 2.0 Port

USB2_LT_P
USB2_LT_N
LTUSB_OC_L

USB Port "D" = Camera

USB2_CAMERA_P
USB2_CAMERA_N
UNUSED_USB_D_OC_L

USB Port "E" = ExpressCard

USB2_EXCARD_P
USB2_EXCARD_N
EXCARD_OC_L

USB Port "F" = IR Receiver

USB_IR_P
USB_IR_N

USB Port "G" = Bluetooth (M13P)

USB_BT_P
USB_BT_N

USB Port "H" = 2nd Left USB 2.0 Port

USB2_LT2_P
USB2_LT2_N
LT2USB_OC_L

Digital connection to be made at the heatsink or lower left frame screw as appropriate

MINI_CLKREQ_L
EXCARD_CLKREQ_L
NO STUFF
C0680
10pF
5%
50V
CERM
402
NO STUFF
C0681
10pF
5%
50V
CERM
402

Chassis connection to be made at the fan cutout near the right ALS

SH0601
EMI-SPRING
0G-502620R
GND_CHASSIS_FANFRAME
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
R0601
0
5%
1/10W
MF-LF
402

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
GND_CHASSIS_DVI_TOP
GND_CHASSIS_DVI_TOP
GND

Chassis connection to be made on FW shell

ZT0603
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
GND_CHASSIS_USB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
GND_CHASSIS_USB
GND_CHASSIS_USB
GND_CHASSIS_USB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS

SH0600
OG-503040
SHLD-SM-LF
GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
GND_CHASSIS_INVERTER

FireWire Aliases

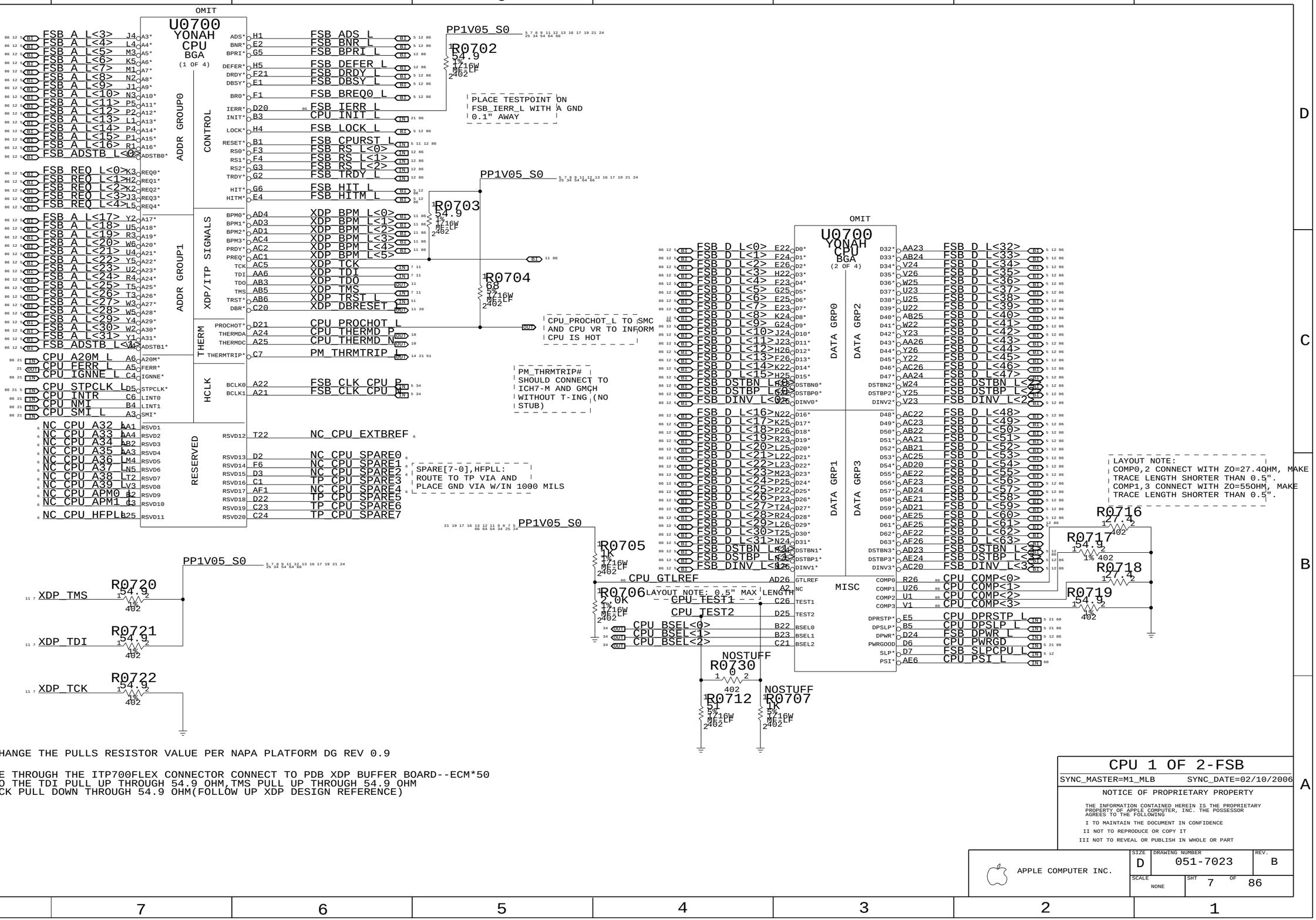
PPFW_PORTA_VP_UF
PPFW_PORTB_VP_UF
PP3V3_FWPHY
PP1V95_FWPHY
SMC_RSTGATE_L
PCI_AD<19>
=FW_PCI_IDSEL
PCI_GNT3_L
PCI_REQ3_L

Signal Aliases

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/11/2005)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 6 OF 86	



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

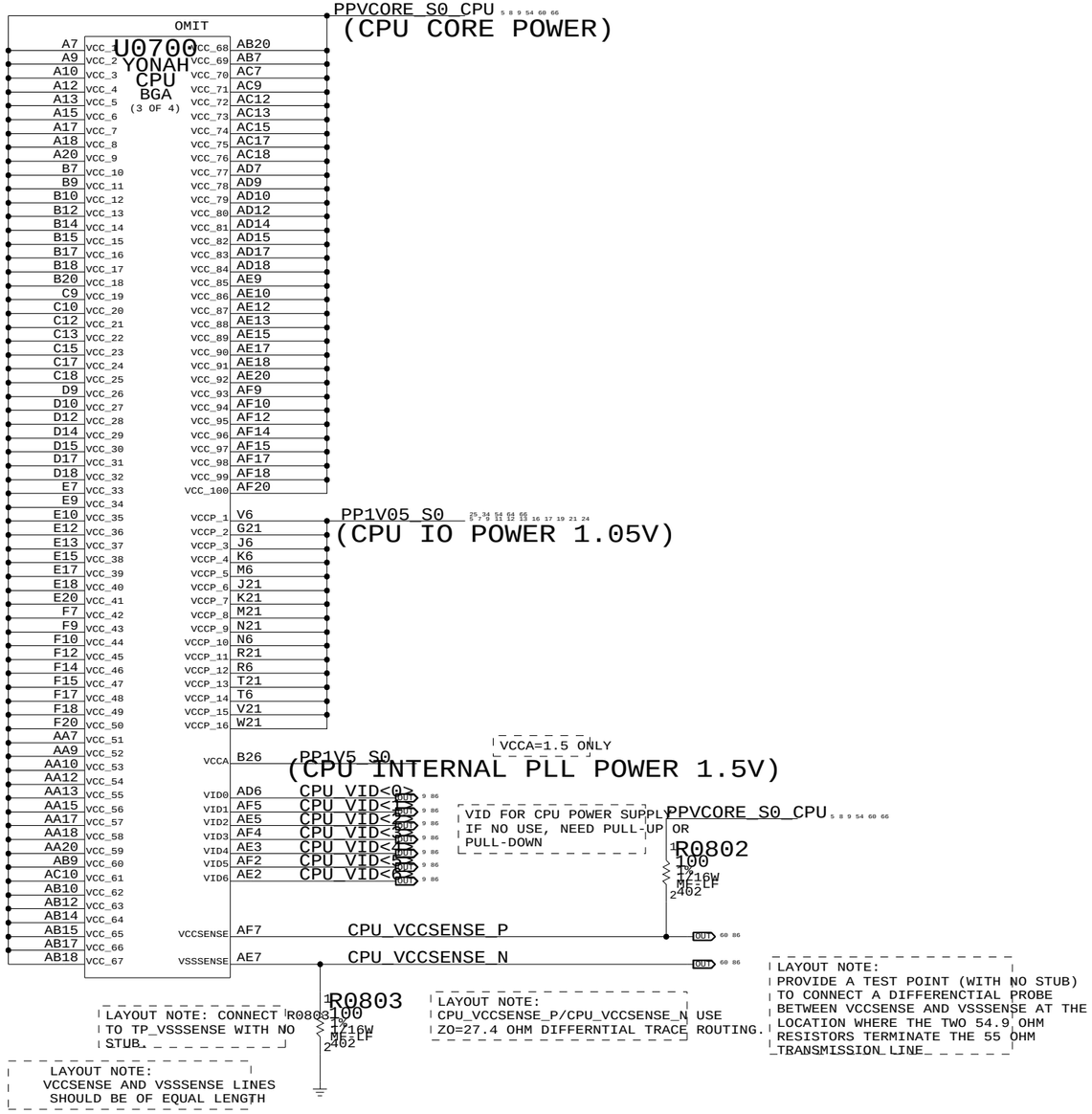
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

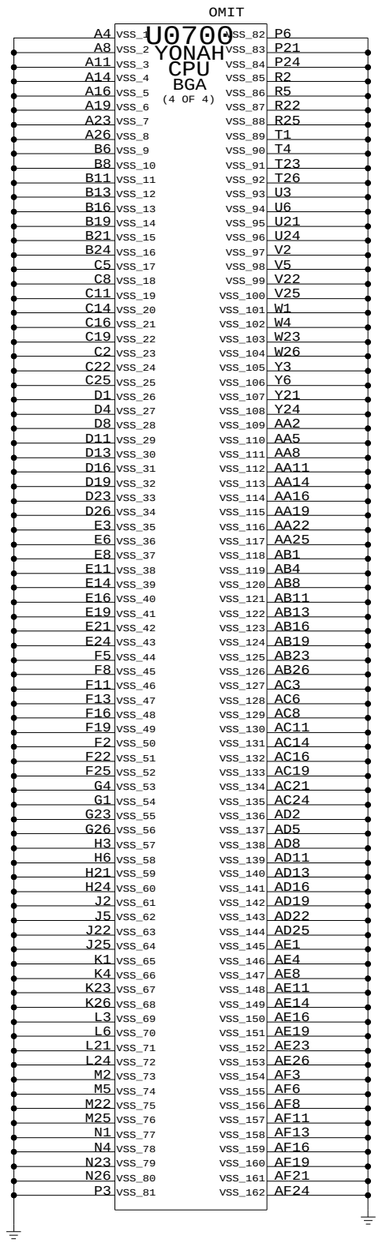
CPU 1 OF 2-FSB

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 7 OF 86	





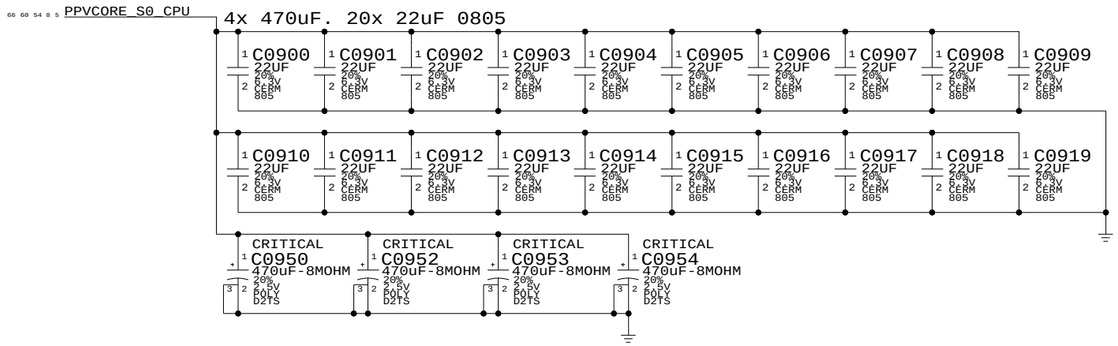
CPU 2 OF 2-PWR/GND

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

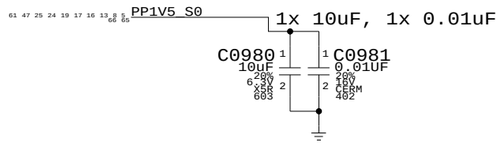
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 8 OF 86	

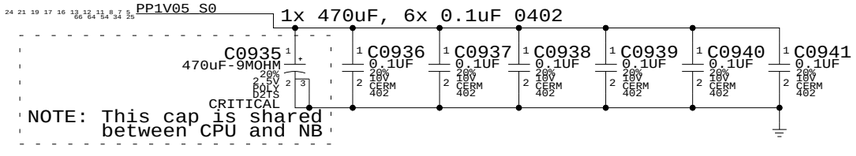
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

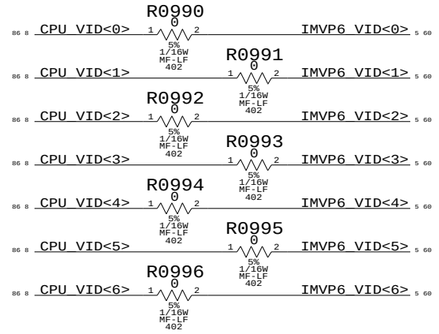


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



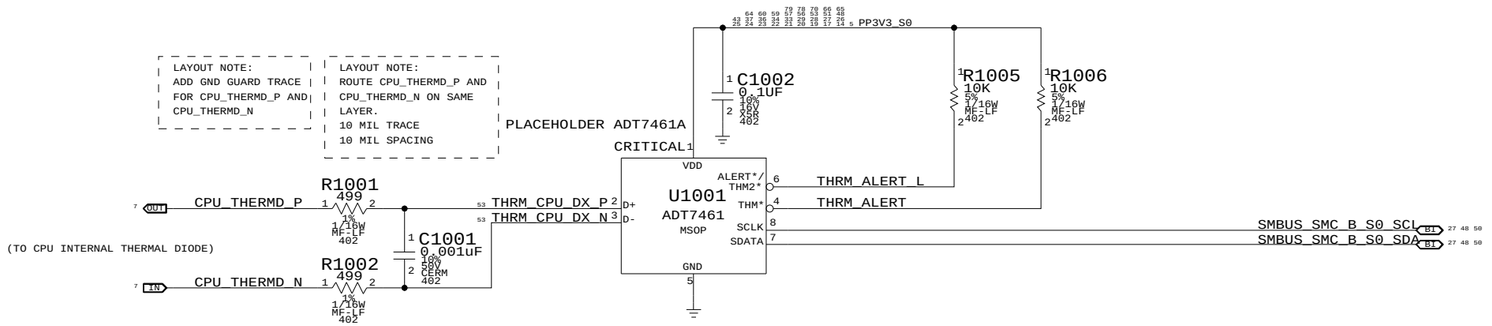
CPU Decoupling & VID

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 9 OF 86	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

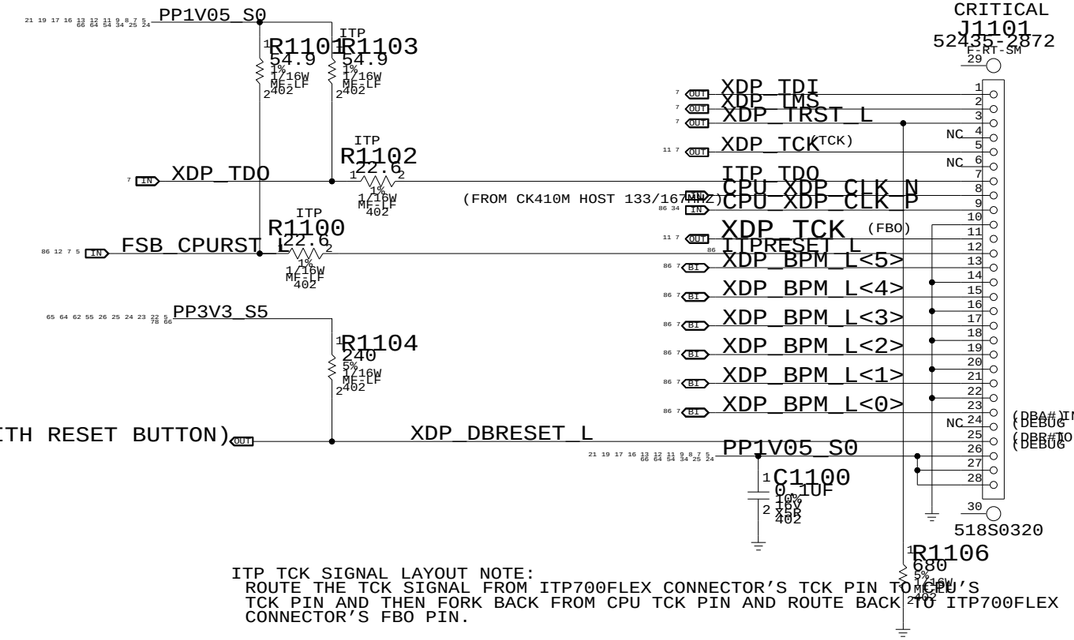
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	10	86

CPU ITP700FLEX DEBUG SUPPORT



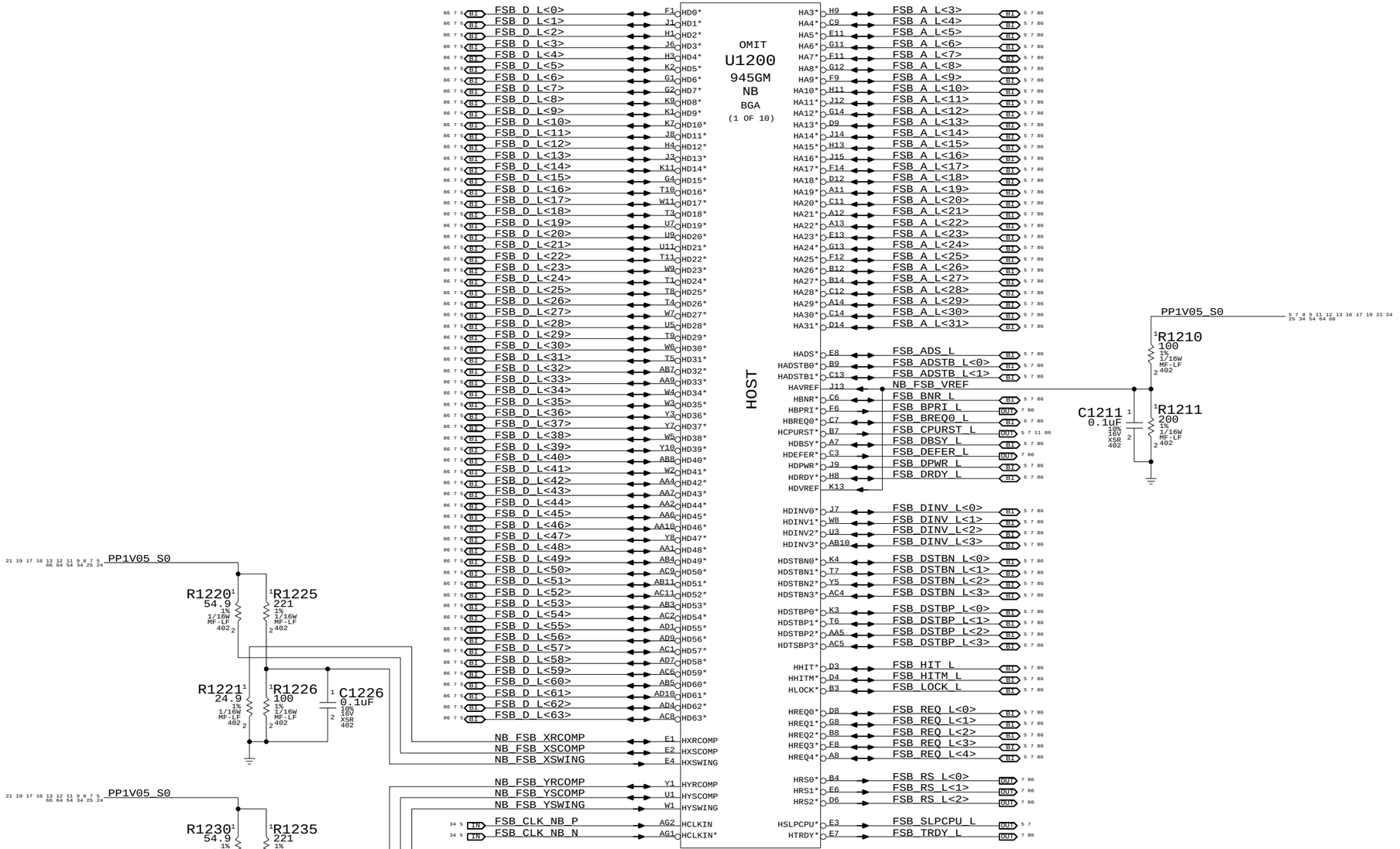
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MSYNC SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 11 OF 86	



NB CPU Interface

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 12 OF 86	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

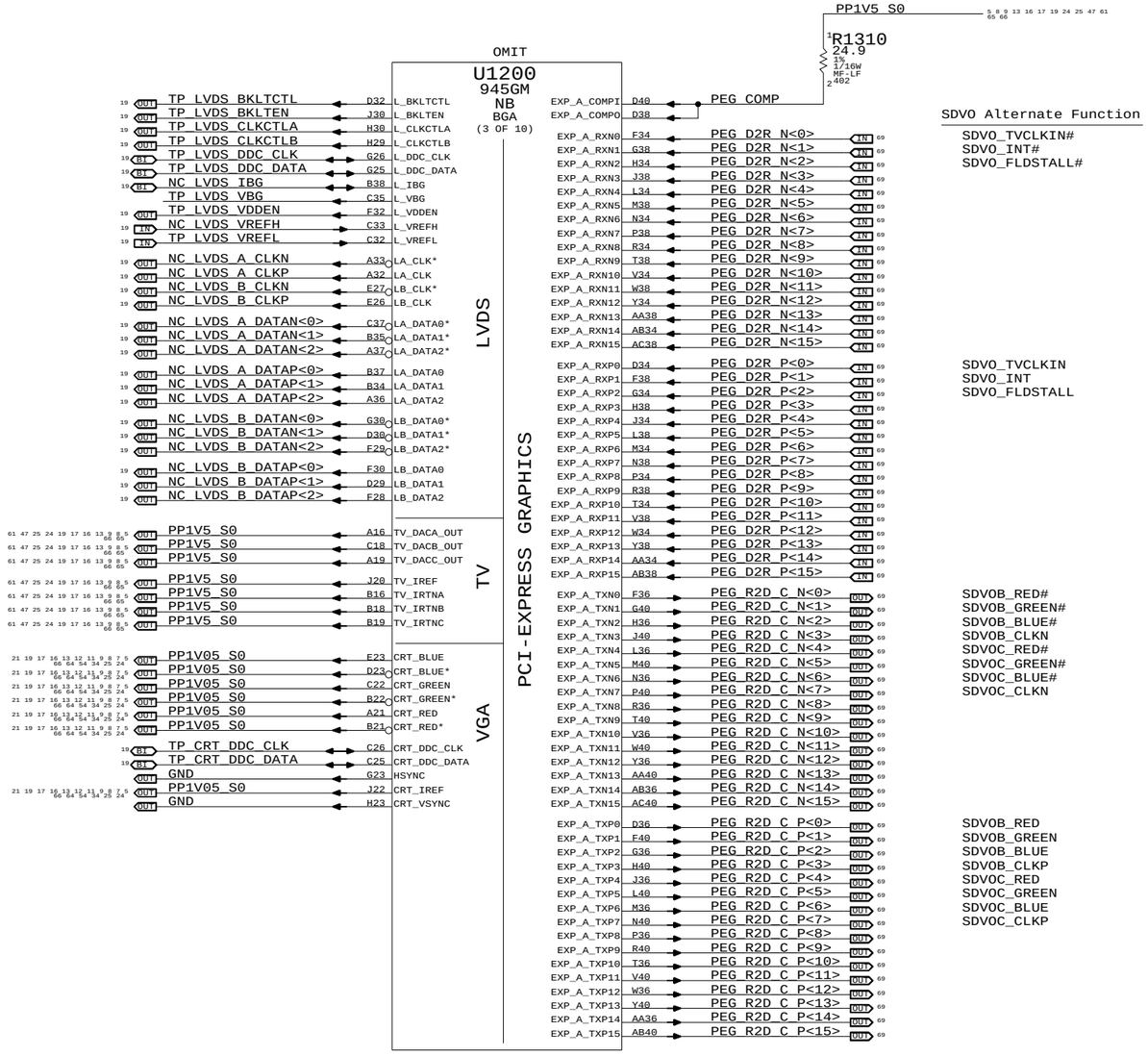
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



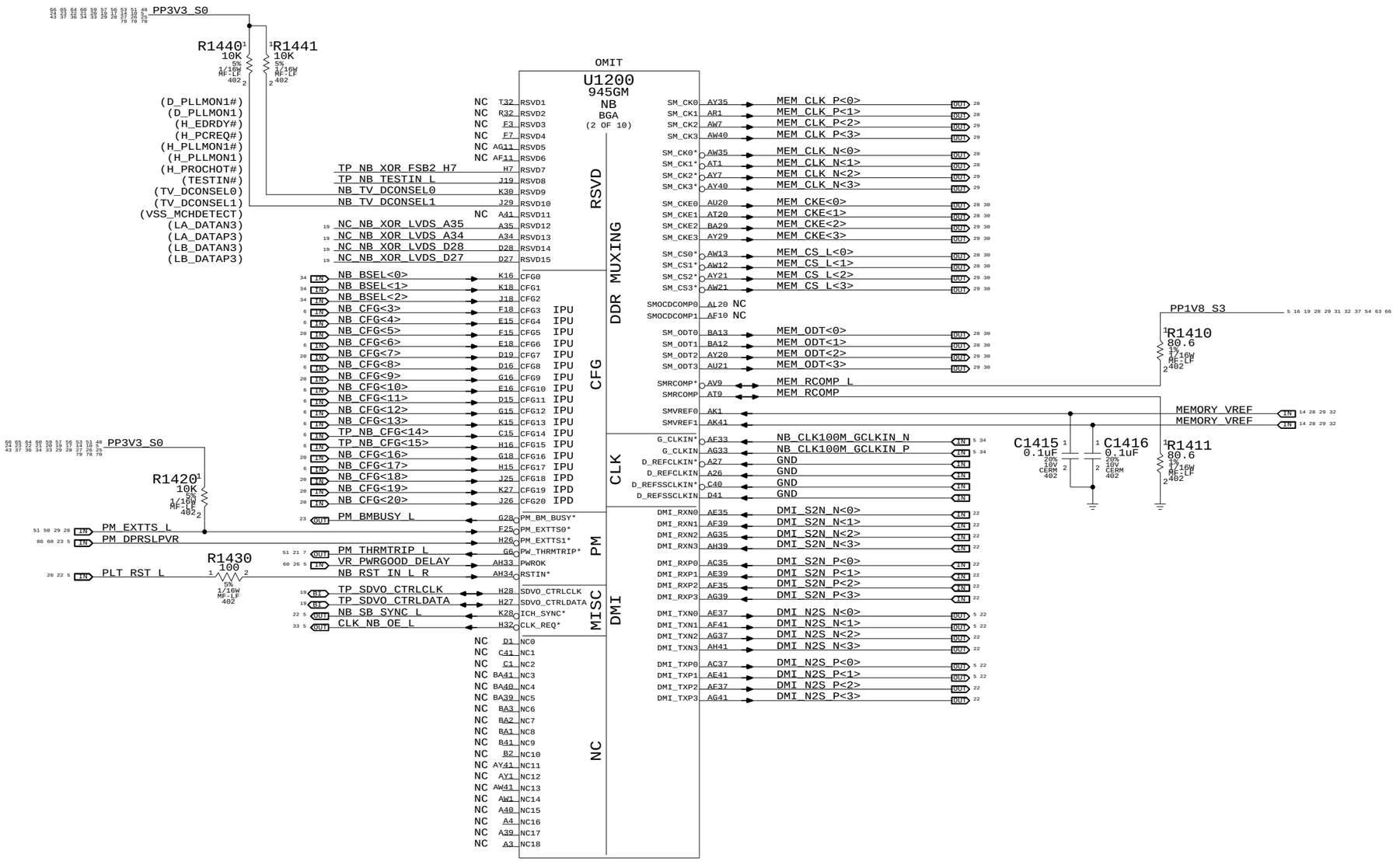
NB PEG / Video Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE NONE SHT 13 OF 86

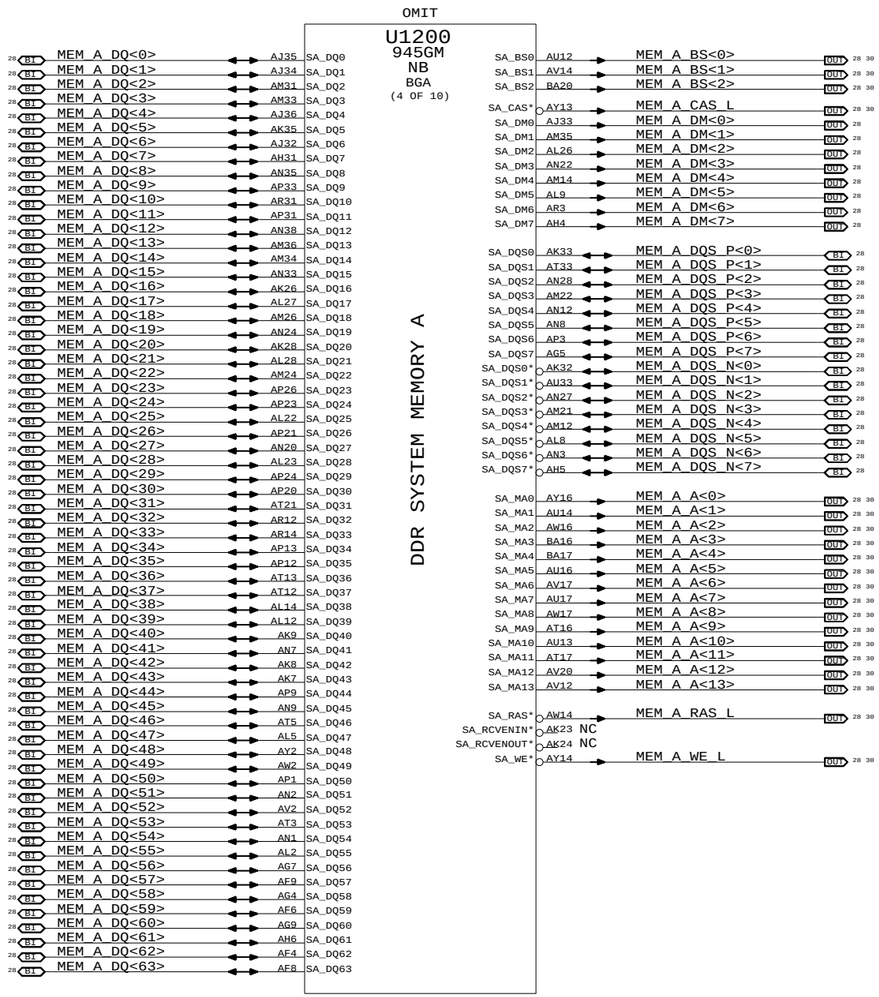


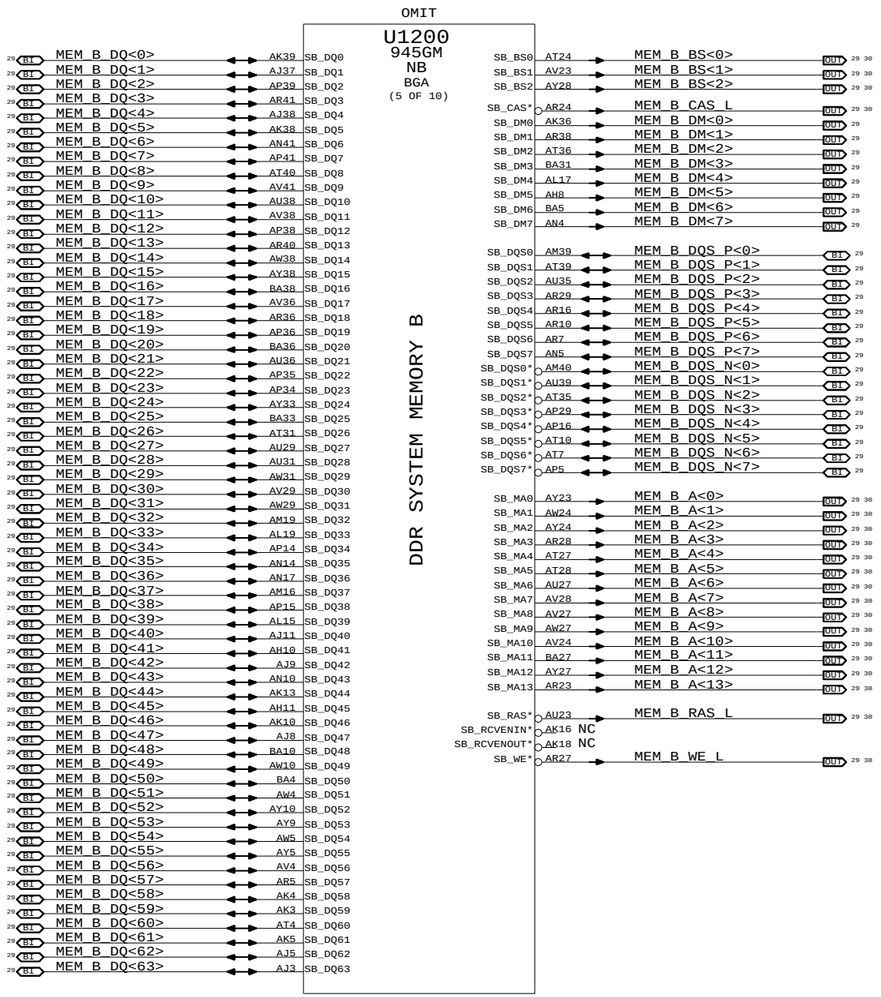
NB Misc Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 14 OF 86	





NB DDR2 Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	15	86

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

PP1V05_S0

OMIT

U1200
945GM
NB
BGA
(7 OF 10)

NCTF

AD27	VCC_NCTF0	VSS_NCTF0	AE27
AC27	VCC_NCTF1	VSS_NCTF1	AE26
AB27	VCC_NCTF2	VSS_NCTF2	AE25
AA27	VCC_NCTF3	VSS_NCTF3	AE24
Y27	VCC_NCTF4	VSS_NCTF4	AE23
W27	VCC_NCTF5	VSS_NCTF5	AE22
V27	VCC_NCTF6	VSS_NCTF6	AE21
U27	VCC_NCTF7	VSS_NCTF7	AE20
T27	VCC_NCTF8	VSS_NCTF8	AE19
R27	VCC_NCTF9	VSS_NCTF9	AE18
AD26	VCC_NCTF10	VSS_NCTF10	AC17
AC26	VCC_NCTF11	VSS_NCTF11	Y17
AB26	VCC_NCTF12	VSS_NCTF12	U17
AA26	VCC_NCTF13		
Y26	VCC_NCTF14		
W26	VCC_NCTF15		
V26	VCC_NCTF16		
U26	VCC_NCTF17		
T26	VCC_NCTF18		
R26	VCC_NCTF19		
AD25	VCC_NCTF20		
AC25	VCC_NCTF21		
AB25	VCC_NCTF22		
AA25	VCC_NCTF23		
Y25	VCC_NCTF24		
W25	VCC_NCTF25		
V25	VCC_NCTF26		
U25	VCC_NCTF27		
T25	VCC_NCTF28		
R25	VCC_NCTF29		
AD24	VCC_NCTF30		
AC24	VCC_NCTF31		
AB24	VCC_NCTF32		
AA24	VCC_NCTF33		
Y24	VCC_NCTF34		
W24	VCC_NCTF35		
V24	VCC_NCTF36		
U24	VCC_NCTF37		
T24	VCC_NCTF38		
R24	VCC_NCTF39		
AD23	VCC_NCTF40		
V23	VCC_NCTF41		
U23	VCC_NCTF42		
T23	VCC_NCTF43		
R23	VCC_NCTF44		
AD22	VCC_NCTF45		
V22	VCC_NCTF46		
U22	VCC_NCTF47		
T22	VCC_NCTF48		
R22	VCC_NCTF49		
AD21	VCC_NCTF50		
V21	VCC_NCTF51		
U21	VCC_NCTF52		
T21	VCC_NCTF53		
R21	VCC_NCTF54		
AD20	VCC_NCTF55		
V20	VCC_NCTF56		
U20	VCC_NCTF57		
T20	VCC_NCTF58		
R20	VCC_NCTF59		
AD19	VCC_NCTF60		
V19	VCC_NCTF61		
U19	VCC_NCTF62		
T19	VCC_NCTF63		
AD18	VCC_NCTF64		
AC18	VCC_NCTF65		
AB18	VCC_NCTF66		
AA18	VCC_NCTF67		
Y18	VCC_NCTF68		
W18	VCC_NCTF69		
V18	VCC_NCTF70		
U18	VCC_NCTF71		
T18	VCC_NCTF72		

PP1V5_S0

		VCCAUX_NCTF0	AG27
		VCCAUX_NCTF1	AF27
		VCCAUX_NCTF2	AG26
		VCCAUX_NCTF3	AF26
		VCCAUX_NCTF4	AG25
		VCCAUX_NCTF5	AF25
		VCCAUX_NCTF6	AG24
		VCCAUX_NCTF7	AF24
		VCCAUX_NCTF8	AG23
		VCCAUX_NCTF9	AF23
		VCCAUX_NCTF10	AG22
		VCCAUX_NCTF11	AF22
		VCCAUX_NCTF12	AG21
		VCCAUX_NCTF13	AF21
		VCCAUX_NCTF14	AG20
		VCCAUX_NCTF15	AF20
		VCCAUX_NCTF16	AG19
		VCCAUX_NCTF17	AF19
		VCCAUX_NCTF18	R19
		VCCAUX_NCTF19	AG18
		VCCAUX_NCTF20	AF18
		VCCAUX_NCTF21	R18
		VCCAUX_NCTF22	AG17
		VCCAUX_NCTF23	AF17
		VCCAUX_NCTF24	AE17
		VCCAUX_NCTF25	AD17
		VCCAUX_NCTF26	AB17
		VCCAUX_NCTF27	AA17
		VCCAUX_NCTF28	W17
		VCCAUX_NCTF29	V17
		VCCAUX_NCTF30	T17
		VCCAUX_NCTF31	R17
		VCCAUX_NCTF32	AG16
		VCCAUX_NCTF33	AF16
		VCCAUX_NCTF34	AE16
		VCCAUX_NCTF35	AD16
		VCCAUX_NCTF36	AC16
		VCCAUX_NCTF37	AB16
		VCCAUX_NCTF38	AA16
		VCCAUX_NCTF39	Y16
		VCCAUX_NCTF40	W16
		VCCAUX_NCTF41	V16
		VCCAUX_NCTF42	U16
		VCCAUX_NCTF43	T16
		VCCAUX_NCTF44	R16
		VCCAUX_NCTF45	AG15
		VCCAUX_NCTF46	AF15
		VCCAUX_NCTF47	AE15
		VCCAUX_NCTF48	AD15
		VCCAUX_NCTF49	AC15
		VCCAUX_NCTF50	AB15
		VCCAUX_NCTF51	AA15
		VCCAUX_NCTF52	Y15
		VCCAUX_NCTF53	W15
		VCCAUX_NCTF54	V15
		VCCAUX_NCTF55	U15
		VCCAUX_NCTF56	T15
		VCCAUX_NCTF57	R15

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

PP1V05_S0
1.05V or 1.5V

U1200
945GM
NB
BGA
(6 OF 10)

OMIT VCC

AA33	VCC_0	VCC_110	L16
W33	VCC_1	VCC_109	M16
P33	VCC_2	VCC_108	N16
N33	VCC_3	VCC_107	M17
L33	VCC_4	VCC_106	P17
J33	VCC_5	VCC_105	L18
AA32	VCC_6	VCC_104	M18
Y32	VCC_7	VCC_103	L19
W32	VCC_8	VCC_102	N18
V32	VCC_9	VCC_101	L19
P32	VCC_10	VCC_100	M19
N32	VCC_11	VCC_99	N19
M32	VCC_12	VCC_98	T19
L32	VCC_13	VCC_97	AB19
J32	VCC_14	VCC_96	AA19
AA31	VCC_15	VCC_95	T19
W31	VCC_16	VCC_94	M19
V31	VCC_17	VCC_93	L20
T31	VCC_18	VCC_92	M20
R31	VCC_19	VCC_91	P20
P31	VCC_20	VCC_90	M20
N31	VCC_21	VCC_89	L20
M31	VCC_22	VCC_88	AB19
AA30	VCC_23	VCC_87	AA19
Y30	VCC_24	VCC_86	T19
W30	VCC_25	VCC_85	M19
V30	VCC_26	VCC_84	N19
U30	VCC_27	VCC_83	L19
T30	VCC_28	VCC_82	M18
R30	VCC_29	VCC_81	L18
P30	VCC_30	VCC_80	P17
N30	VCC_31	VCC_79	N17
M30	VCC_32	VCC_78	M17
L30	VCC_33	VCC_77	N16
AA29	VCC_34	VCC_76	M16
Y29	VCC_35	VCC_75	L16
W29	VCC_36	VCC_74	AC22
V29	VCC_37	VCC_73	AB22
U29	VCC_38	VCC_72	L23
R29	VCC_39	VCC_71	M23
P29	VCC_40	VCC_70	P23
M29	VCC_41	VCC_69	T23
L29	VCC_42	VCC_68	AA23
AB28	VCC_43	VCC_67	AB23
AA28	VCC_44	VCC_66	M24
Y28	VCC_45	VCC_65	N24
V28	VCC_46	VCC_64	P24
U28	VCC_47	VCC_63	L25
T28	VCC_48	VCC_62	M25
R28	VCC_49	VCC_61	N25
P28	VCC_50	VCC_60	L26
N28	VCC_51	VCC_59	N26
M28	VCC_52	VCC_58	P26
L28	VCC_53	VCC_57	L27
P27	VCC_54	VCC_56	M27
N27	VCC_55	VCC_55	N27
M27	VCC_56	VCC_54	P27
L27	VCC_57	VCC_53	L28
P26	VCC_58	VCC_52	M28
N26	VCC_59	VCC_51	N28
L26	VCC_60	VCC_50	P28
M25	VCC_61	VCC_49	R28
L25	VCC_62	VCC_48	T28
P24	VCC_63	VCC_47	U28
M24	VCC_64	VCC_46	V28
N24	VCC_65	VCC_45	Y28
P24	VCC_66	VCC_44	AA28
AB23	VCC_67	VCC_43	AB28
AA23	VCC_68	VCC_42	L29
T23	VCC_69	VCC_41	M29
P23	VCC_70	VCC_40	P29
M23	VCC_71	VCC_39	R29
L23	VCC_72	VCC_38	U29
AC22	VCC_73	VCC_37	V29
AB22	VCC_74	VCC_36	W29
Y22	VCC_75	VCC_35	Y29
W22	VCC_76	VCC_34	AA29
P22	VCC_77	VCC_33	L30
N22	VCC_78	VCC_32	M30
M22	VCC_79	VCC_31	N30
L22	VCC_80	VCC_30	P30
AC21	VCC_81	VCC_29	R30
AA21	VCC_82	VCC_28	T30
W21	VCC_83	VCC_27	U30
N21	VCC_84	VCC_26	V30
M21	VCC_85	VCC_25	W30
L21	VCC_86	VCC_24	Y30
AC20	VCC_87	VCC_23	AA30
AB20	VCC_88	VCC_22	M31
Y20	VCC_89	VCC_21	N31
W20	VCC_90	VCC_20	P31
V20	VCC_91	VCC_19	R31
U20	VCC_92	VCC_18	T31
P20	VCC_93	VCC_17	V31
M20	VCC_94	VCC_16	W31
L20	VCC_95	VCC_15	AA31
AB19	VCC_96	VCC_14	J32
AA19	VCC_97	VCC_13	L32
T19	VCC_98	VCC_12	M32
M19	VCC_99	VCC_11	N32
N19	VCC_100	VCC_10	P32
L19	VCC_101	VCC_9	V32
M18	VCC_102	VCC_8	W32
L18	VCC_103	VCC_7	Y32
P17	VCC_104	VCC_6	AA32
N17	VCC_105	VCC_5	J33
M17	VCC_106	VCC_4	L33
N16	VCC_107	VCC_3	N33
M16	VCC_108	VCC_2	P33
L16	VCC_109	VCC_1	W33
		VCC_0	AA33

AU41	VCC_SM0	VCC_SM107	AJ1
AT41	VCC_SM1	VCC_SM106	AV1
AM41	VCC_SM2	VCC_SM105	AJ6
AU40	VCC_SM3	VCC_SM104	AK6
BA34	VCC_SM4	VCC_SM103	AL6
AY34	VCC_SM5	VCC_SM102	AN6
AW34	VCC_SM6	VCC_SM101	AP6
AV34	VCC_SM7	VCC_SM100	AR6
AU34	VCC_SM8	VCC_SM99	AT6
AT34	VCC_SM9	VCC_SM98	AV6
AR34	VCC_SM10	VCC_SM97	AW6
BA30	VCC_SM11	VCC_SM96	AY6
AY30	VCC_SM12	VCC_SM95	AP8
AW30	VCC_SM13	VCC_SM94	AK8
AV30	VCC_SM14	VCC_SM93	AJ8
AU30	VCC_SM15	VCC_SM92	AH8
AT30	VCC_SM16	VCC_SM91	AJ10
AR30	VCC_SM17	VCC_SM90	AH10
AP30	VCC_SM18	VCC_SM89	AJ12
AN30	VCC_SM19	VCC_SM88	AH12
AM30	VCC_SM20	VCC_SM87	AJ14
AM29	VCC_SM21	VCC_SM86	AH14
AL29	VCC_SM22	VCC_SM85	AJ16
AK29	VCC_SM23	VCC_SM84	AK16
AJ29	VCC_SM24	VCC_SM83	AK12
AH29	VCC_SM25	VCC_SM82	AJ13
AJ28	VCC_SM26	VCC_SM81	AJ11
AH28	VCC_SM27	VCC_SM80	AH13
AJ27	VCC_SM28	VCC_SM79	AJ15
AH27	VCC_SM29	VCC_SM78	AR15
BA26	VCC_SM30	VCC_SM77	AT15
AY26	VCC_SM31	VCC_SM76	AU15
AV26	VCC_SM32	VCC_SM75	AV15
AU26	VCC_SM33	VCC_SM74	AW15
AT26	VCC_SM34	VCC_SM73	AY15
AR26	VCC_SM35	VCC_SM72	AY16
AJ26	VCC_SM36	VCC_SM71	AH16
AH26	VCC_SM37	VCC_SM70	AJ17
AJ25	VCC_SM38	VCC_SM69	AH17
AH25	VCC_SM39	VCC_SM68	AJ18
AJ24	VCC_SM40	VCC_SM67	AH18
AH24	VCC_SM41	VCC_SM66	AJ19
BA23	VCC_SM42	VCC_SM65	AK19
AJ23	VCC_SM43	VCC_SM64	AP19
BA22	VCC_SM44	VCC_SM63	AR19
AY22	VCC_SM45	VCC_SM62	AU19
AV22	VCC_SM46	VCC_SM61	AV19
AW22	VCC_SM47	VCC_SM60	AY19
AV22	VCC_SM48	VCC_SM59	AW19
AU22	VCC_SM49	VCC_SM58	BA19
AT22	VCC_SM50	VCC_SM57	AK20
AP22	VCC_SM51	VCC_SM56	AK21
AR22	VCC_SM52	VCC_SM55	AJ22
AK22	VCC_SM53	VCC_SM54	AK24
AJ22	VCC_SM54	VCC_SM53	AK27
AK21	VCC_SM55	VCC_SM52	AP22
AK20	VCC_SM56	VCC_SM51	AT22
BA19	VCC_SM57	VCC_SM50	AU22
AY19	VCC_SM58	VCC_SM49	AV22
AW19	VCC_SM59	VCC_SM48	AW22
AV19	VCC_SM60	VCC_SM47	AV22
AU19	VCC_SM61	VCC_SM46	AY22
AT19	VCC_SM62	VCC_SM45	BA22
AR19	VCC_SM63	VCC_SM44	AJ23
AP19	VCC_SM64	VCC_SM43	AV23
AK19	VCC_SM65	VCC_SM42	AL23
AJ19	VCC_SM66	VCC_SM41	AH24
AJ18	VCC_SM67	VCC_SM40	AJ24
AJ17	VCC_SM68	VCC_SM39	AH25
AH17	VCC_SM69	VCC_SM38	AJ25
AJ16	VCC_SM70	VCC_SM37	AH26
AH16	VCC_SM71	VCC_SM36	AJ26
BA15	VCC_SM72	VCC_SM35	AR26
AY15	VCC_SM73	VCC_SM34	AT26
AW15	VCC_SM74	VCC_SM33	AU26
AV15	VCC_SM75	VCC_SM32	AV26
AU15	VCC_SM76	VCC_SM31	AW26
AT15	VCC_SM77	VCC_SM30	BA30
AR15	VCC_SM78	VCC_SM29	AY26
AJ15	VCC_SM79	VCC_SM28	BA26
AJ14	VCC_SM80	VCC_SM27	AJ27
AJ13	VCC_SM81	VCC_SM26	AH27
AH13	VCC_SM82	VCC_SM25	AJ28
AK12	VCC_SM83	VCC_SM24	AH29
AJ12	VCC_SM84	VCC_SM23	AK29
AH12	VCC_SM85	VCC_SM22	AL29
AG12	VCC_SM86	VCC_SM21	AM29
AK11	VCC_SM87	VCC_SM20	AM30
BA8	VCC_SM88	VCC_SM19	AN30
AY8	VCC_SM89	VCC_SM18	AP30
AW8	VCC_SM90	VCC_SM17	AR30
AV8	VCC_SM91	VCC_SM16	AT30
AR8	VCC_SM92	VCC_SM15	AU30
AP8	VCC_SM93	VCC_SM14	AV30
BA6	VCC_SM94	VCC_SM13	AW30
AY6	VCC_SM95	VCC_SM12	AY30
AV6	VCC_SM96	VCC_SM11	BA34
AT6	VCC_SM97	VCC_SM10	AR34
AR6	VCC_SM98	VCC_SM9	AT34
AP6	VCC_SM99	VCC_SM8	AU34
AN6	VCC_SM100	VCC_SM7	AV34
AL6	VCC_SM101	VCC_SM6	AW34
AK6	VCC_SM102	VCC_SM5	AY34
AJ6	VCC_SM103	VCC_SM4	BA34
AV1	VCC_SM104	VCC_SM3	AU40
AJ1	VCC_SM105	VCC_SM2	AM41
	VCC_SM106	VCC_SM1	AT41
	VCC_SM107	VCC_SM0	AU41

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 1 0.47uF 20% 6.3V CERM-X5R 402 2
C1613 1 0.47uF 20% 6.3V CERM-X5R 402 2

C1615 1 0.47uF 20% 6.3V CERM-X5R 402 2
PP1V8_S3
Layout Note: Place near pin BA23

C1620 1 10uF 20% 6.3V X5R 603 2
C1621 1 10uF 20% 6.3V X5R 603 2
Layout Note: Place in cavity

C1610 1 0.47uF 20% 6.3V CERM-X5R 402 2
Layout Note: Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 1 0.47uF 20% 6.3V CERM-X5R 402 2
C1611 1 0.47uF 20% 6.3V CERM-X5R 402 2

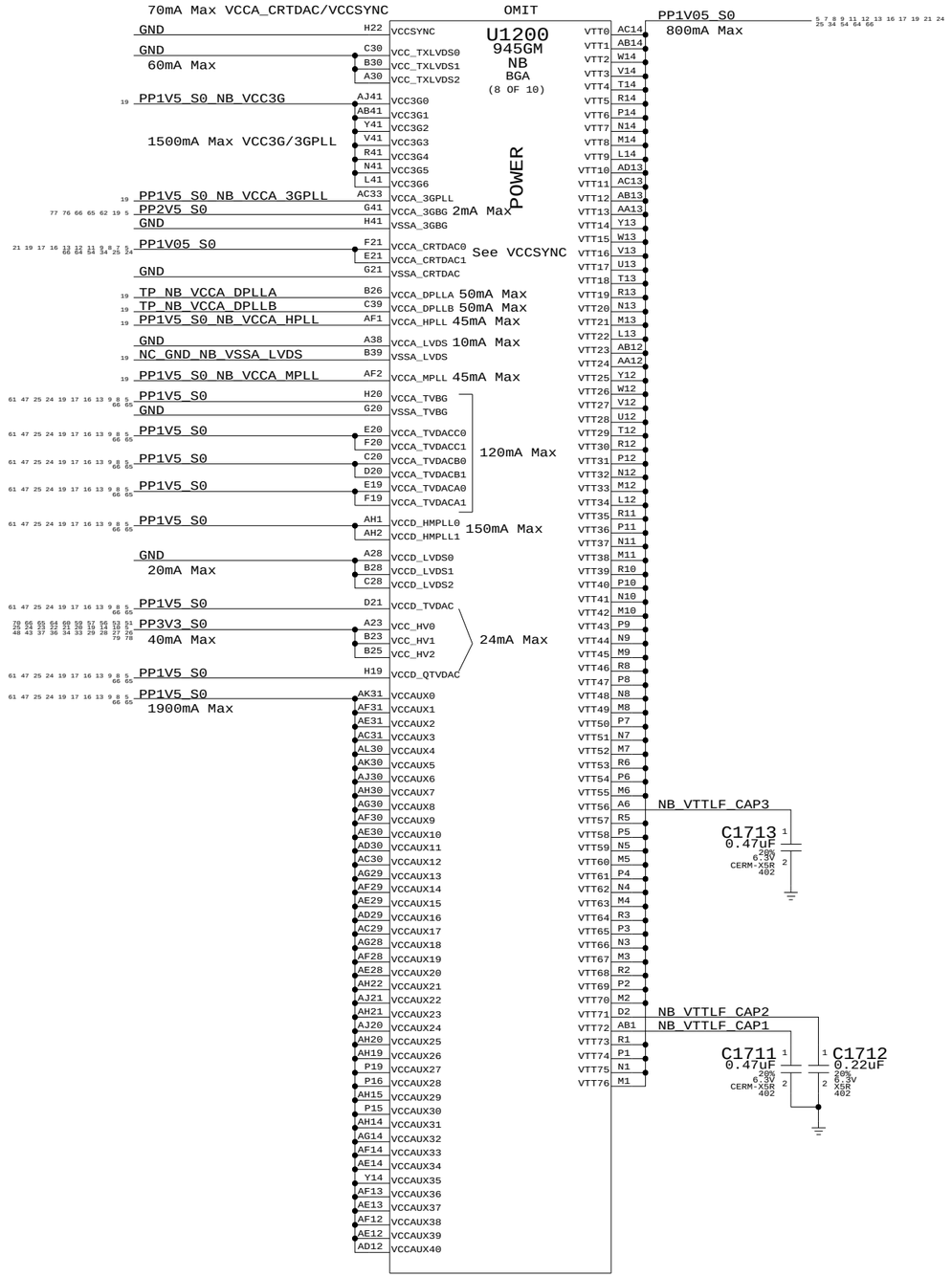
NB Power 1

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE NONE SHT 16 OF 86



NB Power 2

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 17 OF 86	

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945GM
NB
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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	B
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Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	PP1V05_S0	1500mA Max
	PP1V05_S0	10mA Max?
	PP1V05_S0	800mA Max
	PP1V05_S0	?mA Max
3674mA Max	PP1V5_S0	?mA Max
	PP1V5_S0	1500mA Max
	PP1V5_S0	?mA Max
	PP1V5_S0	100mA Max
	PP1V5_S0	24mA Max
	PP1V5_S0	150mA Max
	PP1V5_S0	1900mA Max
3200mA Max	PP1V8_S3	3200mA Max
132mA Max	GND	70mA Max
	GND	60mA Max
	PP2V5_S0	2mA Max
	PP3V3_S0	?mA Max
40mA Max?	PP3V3_S0	40mA Max

PP1V05_S0 → PP1V05_S0 ×7, GND ×2

TP_CRT_DDC_CLK → TP_CRT_DDC_CLK (MAKE_BASE=TRUE)

TP_CRT_DDC_DATA → TP_CRT_DDC_DATA (MAKE_BASE=TRUE)

PP1V5_S0 → PP1V5_S0 ×8

TP_LVDS_BKLTCTL	TP_LVDS_BKLTCTL	MAKE_BASE=TRUE
TP_LVDS_BKLTEN	TP_LVDS_BKLTEN	MAKE_BASE=TRUE
TP_LVDS_CLKCTLA	TP_LVDS_CLKCTLA	MAKE_BASE=TRUE
TP_LVDS_CLKCTLB	TP_LVDS_CLKCTLB	MAKE_BASE=TRUE
TP_LVDS_DDC_CLK	TP_LVDS_DDC_CLK	MAKE_BASE=TRUE
TP_LVDS_DDC_DATA	TP_LVDS_DDC_DATA	MAKE_BASE=TRUE
NC_LVDS_IBG	NC_LVDS_IBG	MAKE_BASE=TRUE NO_TEST=TRUE
TP_LVDS_VDDEN	TP_LVDS_VDDEN	MAKE_BASE=TRUE
NC_LVDS_VREFH	NC_LVDS_VREFH	MAKE_BASE=TRUE NO_TEST=TRUE
TP_LVDS_VREFL	TP_LVDS_VREFL	MAKE_BASE=TRUE
NC_LVDS_A_CLKP	NC_LVDS_A_CLKP	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_A_CLKN	NC_LVDS_A_CLKN	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_A_DATAP<2..0>	LVDS_A_DATA_P<2..0>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_A_DATAN<2..0>	LVDS_A_DATA_N<2..0>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_B_CLKP	NC_LVDS_B_CLKP	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_B_CLKN	NC_LVDS_B_CLKN	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_B_DATAP<2..0>	LVDS_B_DATA_P<2..0>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_B_DATAN<2..0>	LVDS_B_DATA_N<2..0>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_NB_XOR_LVDS_A34	NC_NB_XOR_LVDS_A34	MAKE_BASE=TRUE NO_TEST=TRUE
NC_NB_XOR_LVDS_A35	NC_NB_XOR_LVDS_A35	MAKE_BASE=TRUE NO_TEST=TRUE
NC_NB_XOR_LVDS_D27	NC_NB_XOR_LVDS_D27	MAKE_BASE=TRUE NO_TEST=TRUE
NC_NB_XOR_LVDS_D28	NC_NB_XOR_LVDS_D28	MAKE_BASE=TRUE NO_TEST=TRUE
TP_SDVO_CTRLCLK	TP_SDVO_CTRLCLK	MAKE_BASE=TRUE
TP_SDVO_CTRLDATA	TP_SDVO_CTRLDATA	MAKE_BASE=TRUE

(MCH LVDS DATA/CLK TX 2.5V PWR) → GND

(MCH LVDS DIGITAL 1.5V PWR) → GND

(MCH LVDS ANALOG 2.5V PWR) → GND

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE)

(MCH CRTDAC ANALOG 2.5V PWR) ← PP1V05_S0 → PP1V05_S0, GND

(MCH H/V SYNC 2.5V PWR) → GND

(MCH TVDAC DEDICATED PWR 1.5V) ← PP1V5_S0 → PP1V5_S0

(MCH TVDAC DIGITAL QUIET 1.5V PWR) → PP1V5_S0

(MCH TV OUT CHANNEL A 3.3V PWR) → PP1V5_S0

(MCH TV OUT CHANNEL B 3.3V PWR) → PP1V5_S0

(MCH TV OUT CHANNEL C 3.3V PWR) → PP1V5_S0

(MCH TV DAC BAND GAP 3.3V PWR) → PP1V5_S0

GND

(MCH DISPLAY A PLL 1.5V PWR) → TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE)

(MCH DISPLAY B PLL 1.5V PWR) → TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE)

GND ×4

GMCH CORE PWR 1.05V BYPASS

PP1V05_S0 (1500mA Max)

CRITICAL	C1900	C1902	C1903	C1904	C1905	C1906	C1907
	470uF-9MOHM	10uF	10uF	1uF	0.22uF	0.22uF	0.22uF
	20%	20%	20%	10%	10%	10%	10%
	2.5V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V
	POLY	X5R	X5R	CERM	X5R	X5R	X5R
	D2TS	603	603	402	402	402	402

MCH VTT BYPASS (MCH FSB 1.05V PWR) (SHARE C0940 470UF)

PP1V05_S0 (800mA Max)

C1965	4.7uF	20% 6.3V CERM 603
C1966	2.2uF	20% 6.3V CERM1 603
C1967	0.22uF	20% 6.3V X6S 402

Layout Note: Place in cavity

Layout Note: Place on the edge

MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

PP3V3_S0 (40mA Max)

C1914	10uF	20% 6.3V X5R 603
C1915	0.1uF	20% 10V CERM 402

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

PP2V5_S0 (2mA Max)

C1916: 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

PP1V5_S0 (1900mA Max)

C1918: 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)

PP1V5_S0 (100mA Max) → L1934 FERR-120-OHM-0.2A 0603

PP1V5_S0_NB_VCCA_HPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) (45mA Max)

C1934	22UF	20% 6.3V CERM 805
C1935	0.1uF	20% 10V CERM 402

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)

L1936 FERR-120-OHM-0.2A 0603

PP1V5_S0_NB_VCCA_MPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) (45mA Max)

C1936	22UF	20% 6.3V CERM 805
C1937	0.1uF	20% 10V CERM 402

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)

PP1V5_S0 (1500mA Max) → L1970 91nH 1210

Layout Note: Place L and C close to MCH

C1970	220UF	20% 2.5V POLY SMB2
C1971	10uF	20% 6.3V X6S 603
C1972	10uF	20% 6.3V X6S 603

Layout Note: 10uF caps should be close to MCH on opposite side.

PP1V5_S0_NB_VCC3G (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) (1500mA Max)

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)

PP1V5_S0 → L1975 1.0UH-220MA-0.12-OHM 0805

PP1V5_S0_NB_3GPLL_F (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V)

R1975: 0.51 1% 1/10W MF-LF 402

C1975	10uF	20% 6.3V X5R 603
C1976	0.1uF	20% 10V CERM 402

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

PP1V5_S0_NB_VCCA_3GPLL (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V)

NB (GM) Decoupling

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 19 OF 86	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075
2.2K
5%
1/16W
MF-LF
2 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<17>	RESERVED

PP3V3_S0
51,53,56,57,59,60,64,65,66,70
52,10,14,17,18,20,21,22,23,24,25
26,27,28,29,33,34,36,37,43,48
78,79

NBCFG_VCC_1V5
1 R2058
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

PP3V3_S0
37,43,48,51,53,56,57,59,60,64
5,10,14,16,17,20,21,22,23,24,25
26,27,28,29,33,34,36,37,43,48
65,66,70,78,79

NBCFG_DMI_REVERSE
1 R2059
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

PP3V3_S0
36,37,43,48,51,53,56,57,59,60
8,10,14,17,18,20,21,22,23,24,25
26,27,28,29,33,34
64,65,66,70,78,79

NBCFG_SDVO_AND_PCIE
1 R2060
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

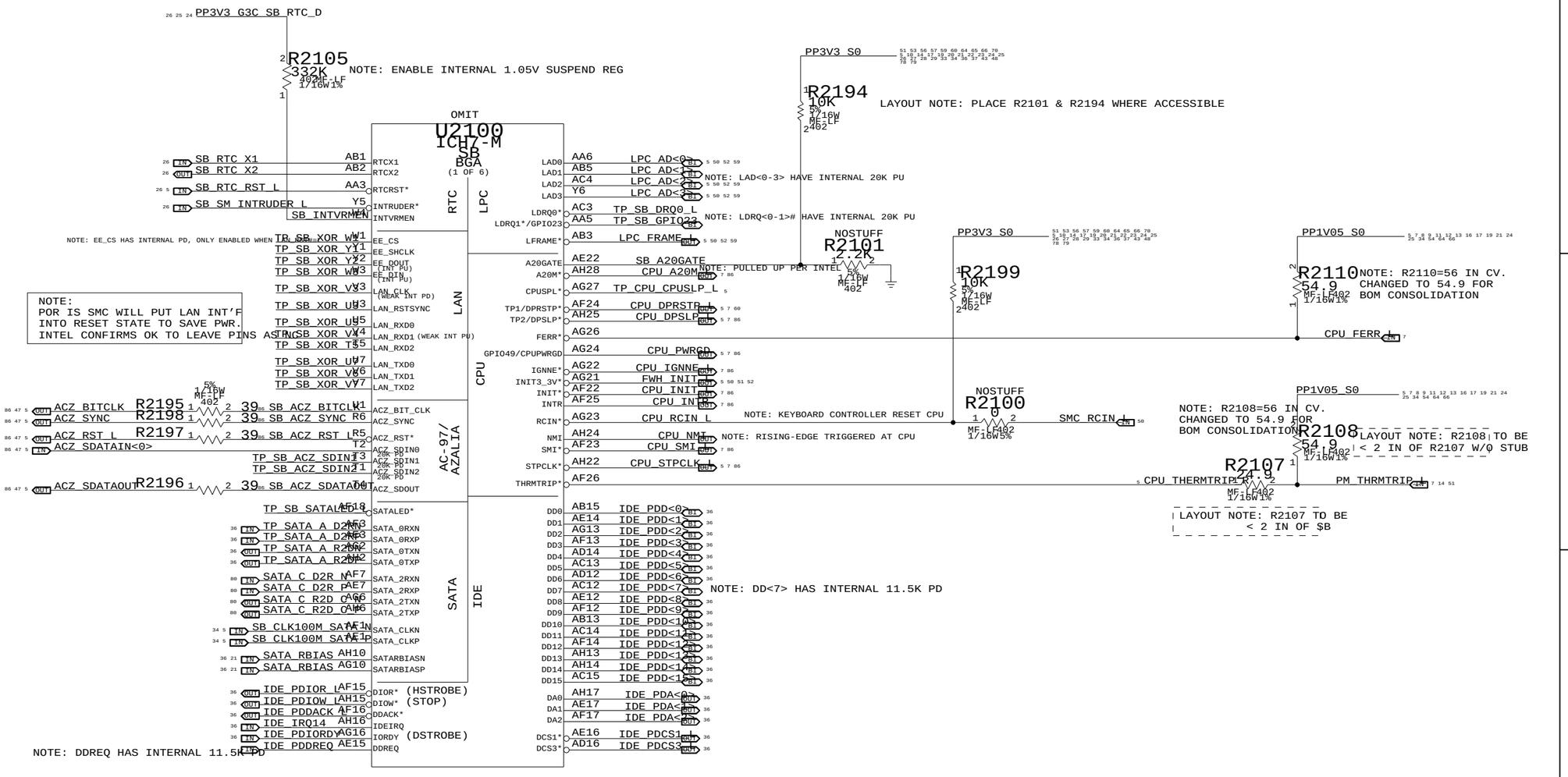
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 20 OF 86	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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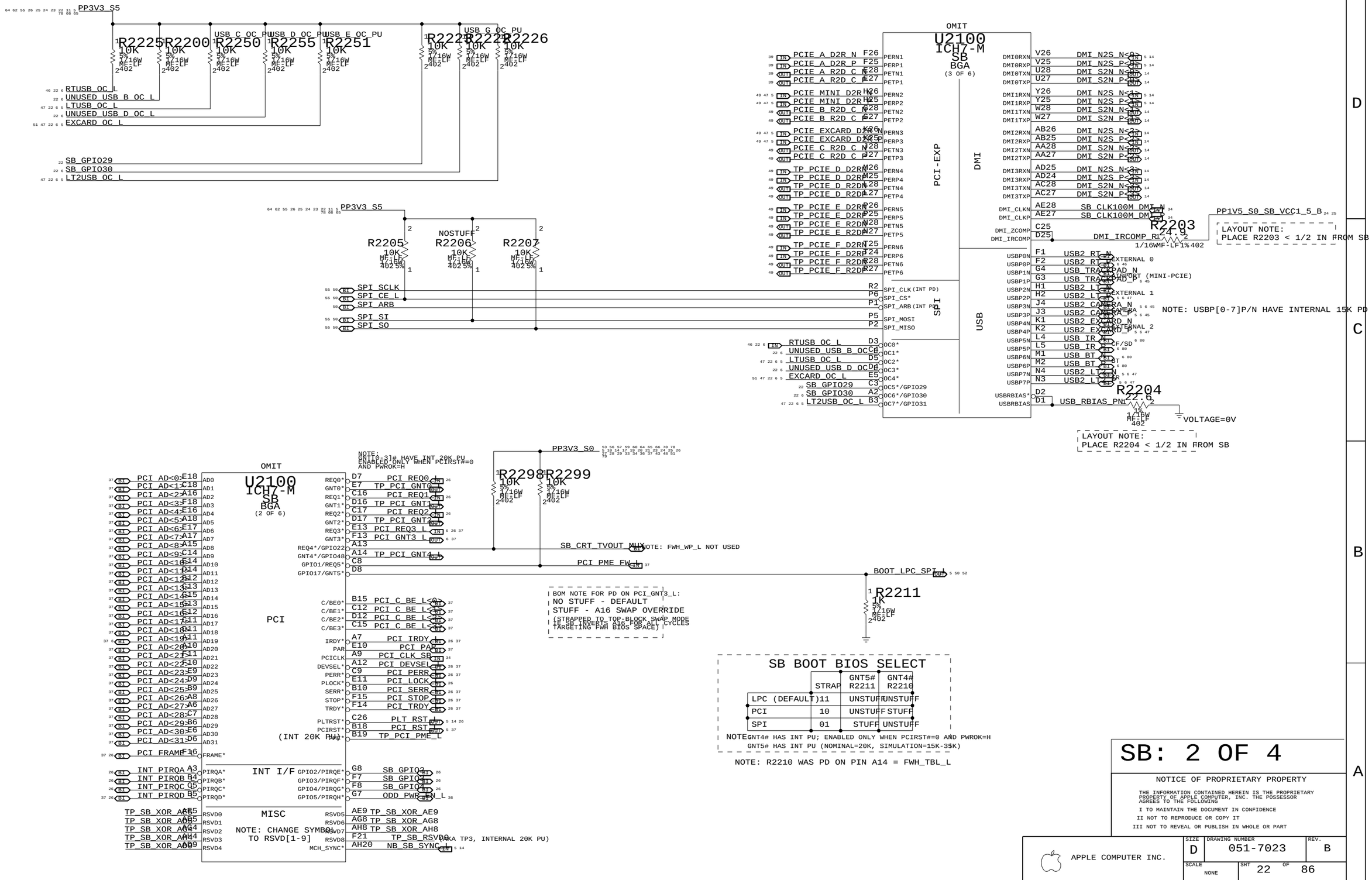
SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 21 OF 86	


PP3V3_S5
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2252 10K 5% 1/16W MF-LF 402
R2253 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_C_OC_PU
USB_D_OC_PU
USB_E_OC_PU
USB_G_OC_PU
RTUSB_OC_L
UNUSED_USB_B_OC_L
LTUSB_OC_L
UNUSED_USB_D_OC_L
EXCARD_OC_L
SB_GPIO29
SB_GPIO30
LT2USB_OC_L
PP3V3_S5
R2205 10K 1/16W 402 5%
NOSTUFF
R2206 10K 1/16W 402 5%
R2207 10K 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCI-EXP
PCIE_A_D2R_N F26
PCIE_A_D2R_P F25
PCIE_A_R2D_C_N E28
PCIE_A_R2D_C_P E27
PCIE_MINI_D2R_N H26
PCIE_MINI_D2R_P H25
PCIE_B_R2D_C_N G28
PCIE_B_R2D_C_P G27
PCIE_EXCARD_D2R_N K26
PCIE_EXCARD_D2R_P K25
PCIE_C_R2D_C_N J28
PCIE_C_R2D_C_P J27
TP_PCIE_D_D2R_N M26
TP_PCIE_D_D2R_P M25
TP_PCIE_D_R2D_N L28
TP_PCIE_D_R2D_P L27
TP_PCIE_E_D2R_N P26
TP_PCIE_E_D2R_P P25
TP_PCIE_E_R2D_N N28
TP_PCIE_E_R2D_P N27
TP_PCIE_F_D2R_N T25
TP_PCIE_F_D2R_P T24
TP_PCIE_F_R2D_N R28
TP_PCIE_F_R2D_P R27
SPI
SPI_CLK(INT PD) R2
SPI_CS* P6
SPI_ARB(INT PU) P1
SPI_MOSI P5
SPI_MISO P2
USB
RTUSB_OC_L D3
UNUSED_USB_B_OC_L C4
LTUSB_OC_L D5
UNUSED_USB_D_OC_L D4
EXCARD_OC_L E5
SB_GPIO29 C3
SB_GPIO30 A2
LT2USB_OC_L B3
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
DMI
DMI0RXN V26
DMI0RXP V25
DMI0TXN U28
DMI0TXP U27
DMI1RXN Y26
DMI1RXP Y25
DMI1TXN W28
DMI1TXP W27
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA28
DMI2TXP AA27
DMI3RXN AD25
DMI3RXP AD24
DMI3TXN AC28
DMI3TXP AC27
DMI_CLKN AE28
DMI_CLKP AE27
DMI_ZCOMP C25
DMI_IRCOMP D25
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
USB
USBP0N F1
USBP0P F2
USBP1N G4
USBP1P G3
USBP2N H1
USBP2P H2
USBP3N J4
USBP3P J3
USBP4N K1
USBP4P K2
USBP5N L4
USBP5P L5
USBP6N M1
USBP6P M2
USBP7N N4
USBP7P N3
USBRBIAS* D2
USBRBIAS D1
USB2_RT_N
USB2_RT_P
USB_TRACKPAD_N
USB_TRACKPAD_P
USB2_LT_N
USB2_LT_P
USB2_CAMERA_N
USB2_CAMERA_P
USB2_EXCARD_N
USB2_EXCARD_P
USB_IR_N
USB_IR_P
USB_BT_N
USB_BT_P
USB2_LT2_N
USB2_LT2_P
R2204 22.6 1/16W MF-LF 1% 402
USB_RBIAS_PN
VOLTAGE=0V
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
EXTERNAL 0
IR(MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
ER
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
PCI
PCI_AD<0> E18
PCI_AD<1> C18
PCI_AD<2> A16
PCI_AD<3> F18
PCI_AD<4> E16
PCI_AD<5> A18
PCI_AD<6> E17
PCI_AD<7> A17
PCI_AD<8> A15
PCI_AD<9> C14
PCI_AD<10> G14
PCI_AD<11> D14
PCI_AD<12> B12
PCI_AD<13> C13
PCI_AD<14> G15
PCI_AD<15> G13
PCI_AD<16> G12
PCI_AD<17> C11
PCI_AD<18> D11
PCI_AD<19> A11
PCI_AD<20> A10
PCI_AD<21> F11
PCI_AD<22> F10
PCI_AD<23> E9
PCI_AD<24> D9
PCI_AD<25> B9
PCI_AD<26> A8
PCI_AD<27> A6
PCI_AD<28> C7
PCI_AD<29> B6
PCI_AD<30> E6
PCI_AD<31> D6
PCI_FRAME_L F16
INT I/F
INT_PIRQA A3
INT_PIRQB B4
INT_PIRQC C5
INT_PIRQD B5
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
TP_SB_XOR_AE5
TP_SB_XOR_AG5
TP_SB_XOR_AG4
TP_SB_XOR_AH4
TP_SB_XOR_AH5
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
REQ0* D7 PCI_REQ0_L
GNT0* E7 TP_PCI_GNT0_L
REQ1* C16 PCI_REQ1_L
GNT1* D16 TP_PCI_GNT1_L
REQ2* C17 PCI_REQ2_L
GNT2* D17 TP_PCI_GNT2_L
REQ3* E13 PCI_REQ3_L
GNT3* F13 PCI_GNT3_L
REQ4*/GPIO22 A13
GNT4*/GPIO48 A14 TP_PCI_GNT4_L
GPIO1/REQ5* C8
GPIO17/GNT5* D8
C/BE0* B15 PCI_C_BE_L<0>
C/BE1* C12 PCI_C_BE_L<1>
C/BE2* D12 PCI_C_BE_L<2>
C/BE3* C15 PCI_C_BE_L<3>
IRDY* A7 PCI_IRDY_L
PAR E10 PCI_PAR
PCICLK A9 PCI_CLK_SB
DEVSEL* A12 PCI_DEVSEL_L
PERR* C9 PCI_PERR_L
PLOCK* E11 PCI_LOCK_L
SERR* B10 PCI_SERR_L
STOP* F15 PCI_STOP_L
TRDY* F14 PCI_TRDY_L
PLTRST* C26 PLT_RST_L
PCIRST* B18 PCI_RST_L
(INT 20K PU) B19 TP_PCI_PME_L
GPIO2/PIRQE* G8 SB_GPIO2
GPIO3/PIRQF* F7 SB_GPIO3
GPIO4/PIRQG* F8 SB_GPIO4
GPIO5/PIRQH* G7 ODD_PWR_EN_L
RSVD5 AE9 TP_SB_XOR_AE9
RSVD6 AG8 TP_SB_XOR_AG8
RSVD7 AH8 TP_SB_XOR_AH8
RSVD8 F21 TP_SB_RSVD8
MCH_SYNC* AH20 NB_SB_SYNC
(NOTE: TP_SB_RSVD8 IS TP_SB_XOR_AA TP3, INTERNAL 20K PU)
PP3V3_S0
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
SB_CRT_TVOUT_MUX
PCI_PME_FW_L
NOTE: FWH_WP_L NOT USED
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
SB BOOT BIOS SELECT
STRAP GNT5# R2211 GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
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SIZE D
DRAWING NUMBER 051-7023
REV. B
SCALE NONE
SHT 22 OF 86

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

PP3V3_S0
PP3V3_S5
NO_REBOOT_MODE

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 10K 1/16W 402 2MF-LF 5%
R2326 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%
NOSTUFF NOSTUFF
RP2300 10K 5% 1/16W 5M-LF

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

OMIT
U2100
ICH7-M SB
BGA
(4 OF 6)

SMBUS_SB_SCL
SMBUS_SB_SDA
SMB_LINK_ALERT_L
SMLINK<0>
SMLINK<1>
NOT USED
PM_RI_L
SB_SPKR
PM_SUS_STAT_L
PM_SYSRST_L
PM_BMBUSY_L
SMB_ALERT_L
NOTE: RESERVED FOR FUTURE

SMBCLK C22
SMBDATA B22
LINKALERT* A26
SMLINK0 B25
SMLINK1 A25
RI* A28
SPKR (INT WEAK PD) A19
SUS_STAT* A27
SYS_RST* A22
GPIO0/BM_BUSY* AB18
GPIO11/SMBALERT* B23
SMB

PM_STPPCI_L
PM_STPCPU_L
SB_GPIO26
BIOS_REC
FWH_MFG_MODE
PM_CLKRUN_L
TP_AZ_DOCK_EN
AZ_DOCK_RST_L
RESERVED FOR MOBILE
AZALIA DOCKING INTF

GPIO18/STPPCI* AC20
GPIO20/STPCPU* AF21
GPIO26 A21
GPIO27 B21
GPIO28 E23
GPIO32/CLKRUN* AG18
GPIO33/AZ_DOCK_EN* AC19
GPIO34/AZ_DOCK_RST* U2
SYS GPIO
PWR MNGT

PCIE_WAKE_L
INT_SERIRQ
PM_THRM_L
VR_PWRGD_CK410
TP_SB_GPIO6
SMC_RUNTIME_SCI_L
SMC_EXTSMI_L

WAKE* F20
SERIRQ AH21
THRM* AF20
VRMPWRGD AD22
GPIO6 AG21
GPIO7 AC18
GPIO8 E21

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

R2302 100K
R2303 100K
R2305 100K
SATA_C_DET_L

AF19 SB_GPIO21
AH18 SB_GPIO19
AH19
AE19 SB_GPIO37

CLKS
CLK14 AC1 SB_CLK14P3M_TIMER
CLK48 B2 SB_CLK48M_USBCLK
SUSCLK C20 TP_SB_SUS_CLK

SLP_S3* B24 PM_SLP_S3
SLP_S4* D23 PM_SLP_S4
SLP_S5* F22 PM_SLP_S5
PWROK AA4 PM_SB_PWROK
GPIO16/DPRSLPVR AC22 PM_DPRSLPVR
TP0/BATLOW* C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
PWRBTN* C23 PM_PWRBTN_L
LAN_RST* C19 PM_LAN_ENABLE NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4

GPIO9 E20 SMS_INT_L
GPIO10 A20 SMC_SB_NMI_L
GPIO12 F19 PATA_PWR_EN_L
GPIO13 E19
GPIO14 R4 IDE_RESET_L
GPIO15 E22 SV_SET_UP
GPIO24 R3 CRB_SV_DET
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
GPIO35 AD21 SB_CLK100M_SATA_OE_L
GPIO38 AD20 TP_SB_GPIO38
GPIO39 AE20 SATA_C_PWR_EN_L
GPIO
DEF=GPI
OD

PP3V3_S5
R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%
PM_BATLOW_L
R2399 100K 1/16W 402 2MF-LF 5%
PM_RSMRST_L
SMC_WAKE_SCI_L

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

PP3V3_S5
R2306 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2308 10K 1/16W 402 2MF-LF 5%
SV_SET_UP
CRB_SV_DET

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 2MF-LF 5%

PP3V3_S5
R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%
FWH_MFG_MODE
BIOS_REC

R2314 NOSTUFF 0 1/16W 402 2MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 2MF-LF 5%

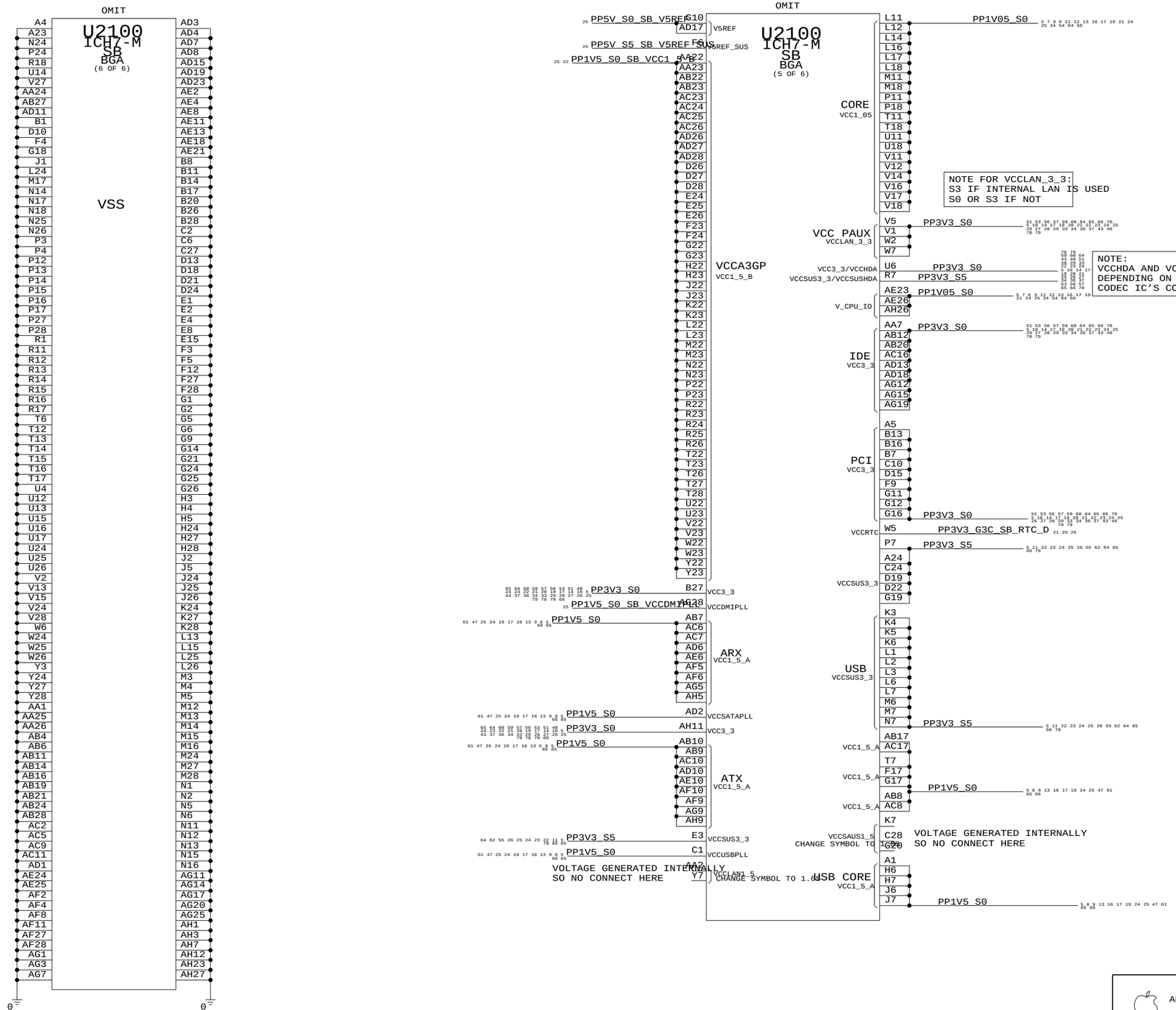
PP3V3_S5
R2390 10K 1/16W 402 2MF-LF 5%
PATA_PWR_EN_L

PP3V3_S0
R2388 10K 1/16W 402 2MF-LF 5%
SATA_C_PWR_EN_L

SB: 3 OF 4
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 23 OF 86	



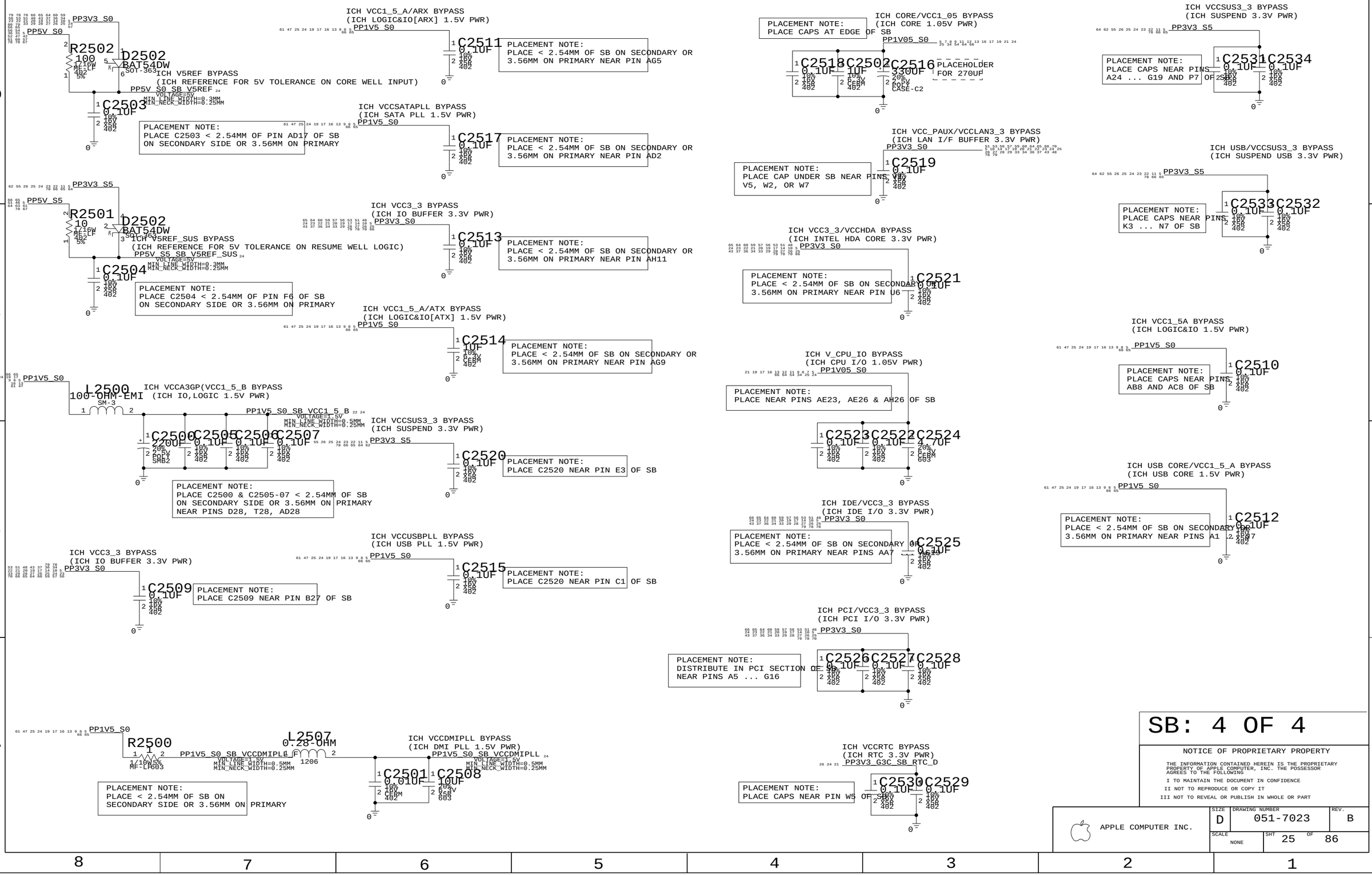
SB: 4 OF 4

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	24	86


PP3V3_S0
PP5V_S0
R2502
100
1/16W
MF-LF
402
5%
D2502
BAT54DW
SOT-363
C2503
0.1UF
10%
16V
X5R
402
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PP1V5_S0
C2511
0.1UF
16V
X5R
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
C2517
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
PP3V3_S5
PP5V_S5
R2501
10
D2502
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
C2504
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
C2513
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
C2514
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
L2500
100-OHM-EMI
SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500
270UF
20%
2.5V
POLY
SMB2
C2505
C2506
C2507
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
C2520
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
C2515
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
C2509
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
R2500
1/10W5%
MF-LF003
L2507
0.28-OHM
1206
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
C2501
0.01UF
C2508
10UF
6.3V
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PP1V05_S0
C2518
C2502
C2516
330UF
2.5V
POLY
CASE-C2
PLACEHOLDER
FOR 270UF
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
C2519
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS W4,
V5, W2, OR W7
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
C2521
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
C2523
C2522
C2524
4.7UF
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
C2525
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
C2526
C2527
C2528
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PP3V3_G3C_SB_RTC_D
C2530
C2529
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
C2531
C2534
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
C2533
C2532
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
C2510
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
C2512
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... A7
SB: 4 OF 4
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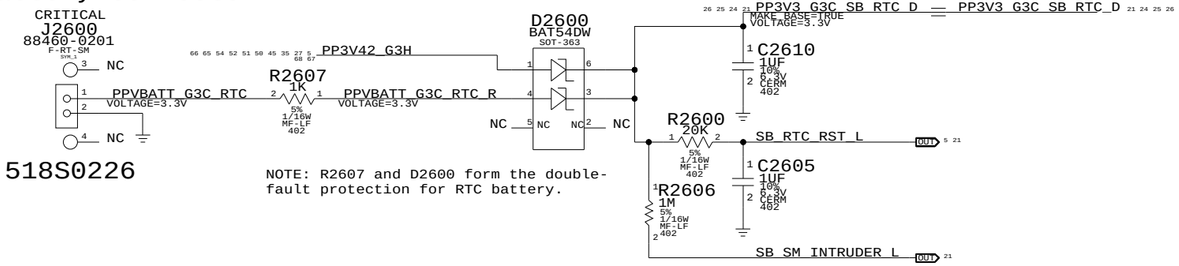
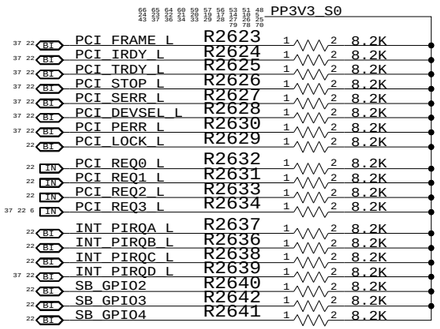
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7023
REV. B
SCALE NONE
SHT 25 OF 86

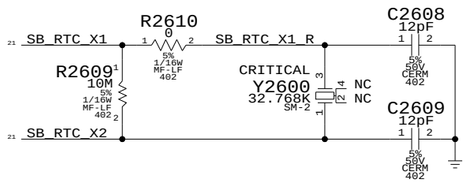
RTC Battery Connector

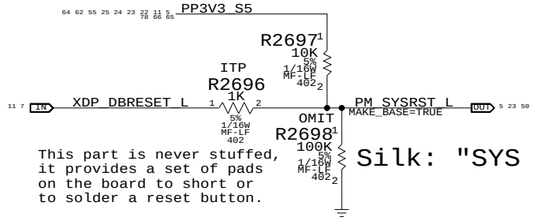


NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



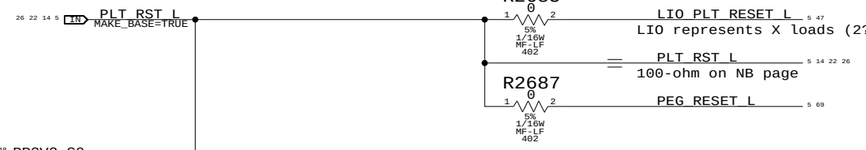


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

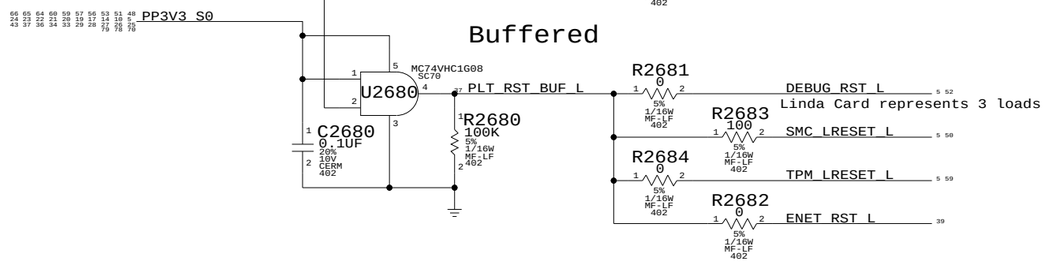
Silk: "SYS RST"

Platform Reset Connections

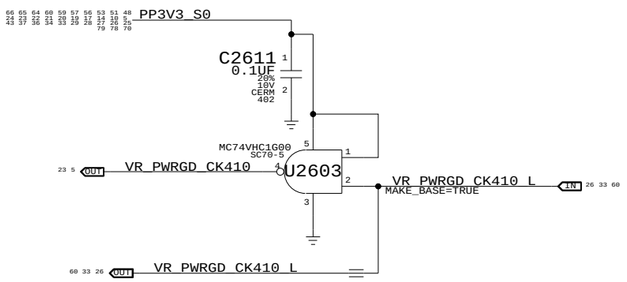
Unbuffered



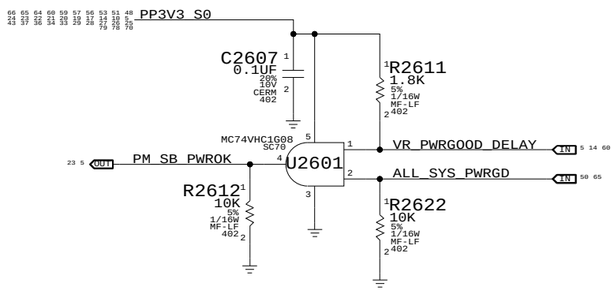
Buffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



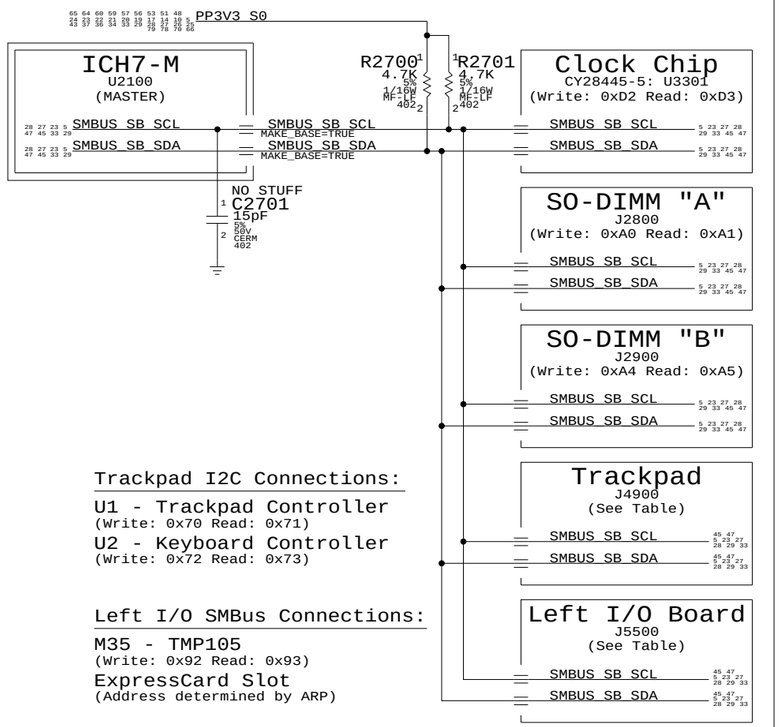
SB Misc

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 26 OF 86	

ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

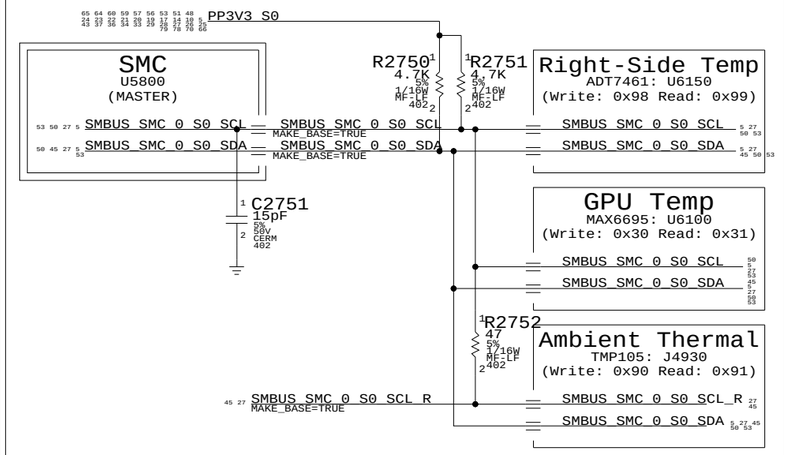
U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

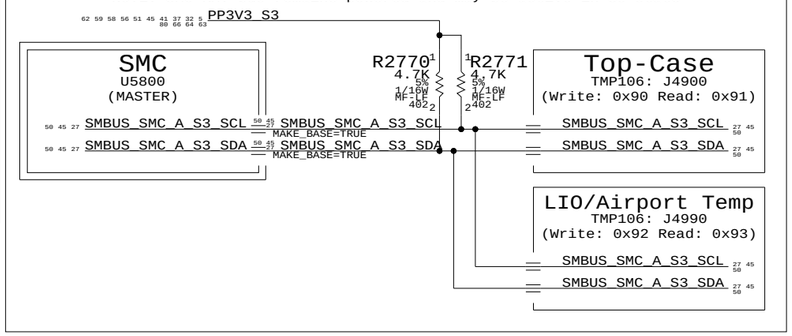
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections

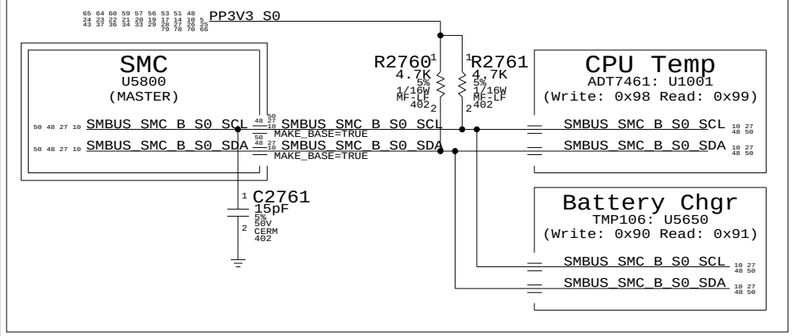


SMC "A" SMBus Connections

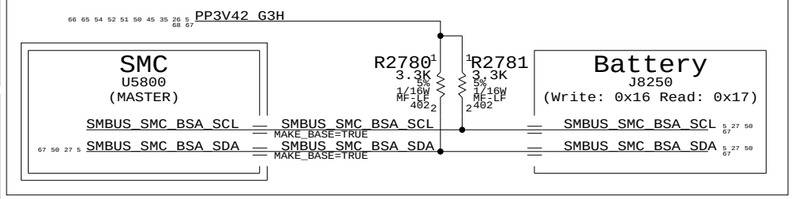
NOTE: SMC RMT bus remains powered and may be active in S3 state



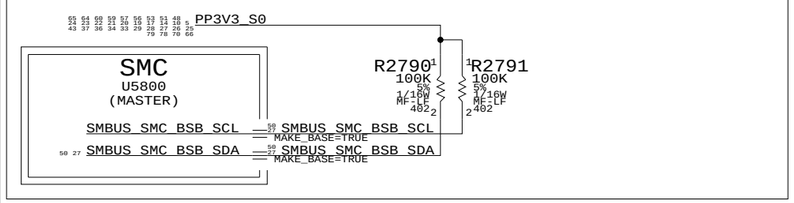
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M9 SMBus Connections

SYNC_MASTER=M1_MLB SYNC_DATE=01/04/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	27	86

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (surface-mount) slot

PP1V8_S3

MEMORY_VREF

C2801 2.2uF 20% 6.3V CERM 603

C2800 0.1uF 20% 10V CERM 402

NC

CRITICAL
J2800
F-RT-SM-M9

DDR2-SODIMM-DUAL

	1A	VREF		2A	VSS0		
	3A	VSS1		4A	DQ4	MEM_A_DQ<8>	15
15 MEM_A_DQ<14>	5A	DQ0		6A	DQ5	MEM_A_DQ<12>	15
15 MEM_A_DQ<13>	7A	DQ1		8A	VSS2		
	9A	VSS4		10A	DM0	MEM_A_DM<1>	15
15 MEM_A_DQS_N<1>	11A	DQS0*		12A	VSS5		
15 MEM_A_DQS_P<1>	13A	DQS0		14A	DQ6	MEM_A_DQ<15>	15
	15A	VSS6		16A	DQ7	MEM_A_DQ<9>	15
15 MEM_A_DQ<10>	17A	DQ2		18A	VSS7		
15 MEM_A_DQ<11>	19A	DQ3		20A	DQ12	MEM_A_DQ<2>	15
	21A	VSS8		22A	DQ13	MEM_A_DQ<3>	15
15 MEM_A_DQ<5>	23A	DQ8		24A	VSS9		
15 MEM_A_DQ<4>	25A	DQ9		26A	DM1	MEM_A_DM<0>	15
	27A	VSS10		28A	VSS11		
15 MEM_A_DQS_N<0>	29A	DQS1*		30A	CK0	MEM_CLK_P<0>	14
15 MEM_A_DQS_P<0>	31A	DQS1		32A	CK0*	MEM_CLK_N<0>	14
	33A	VSS12		34A	VSS13		
15 MEM_A_DQ<6>	35A	DQ10		36A	DQ14	MEM_A_DQ<1>	15
15 MEM_A_DQ<7>	37A	DQ11		38A	DQ15	MEM_A_DQ<0>	15
	39A	VSS14		40A	VSS15		
		KEY					
	41A	VSS16		42A	VSS17		
15 MEM_A_DQ<19>	43A	DQ16		44A	DQ20	MEM_A_DQ<23>	15
15 MEM_A_DQ<18>	45A	DQ17		46A	DQ21	MEM_A_DQ<22>	15
	47A	VSS18		48A	VSS19		
15 MEM_A_DQS_N<2>	49A	DQS2*		50A	NC0	PM_EXTTS_L	14 29 50 51
15 MEM_A_DQS_P<2>	51A	DQS2		52A	DM2	MEM_A_DM<2>	15
	53A	VSS21		54A	VSS22		
15 MEM_A_DQ<20>	55A	DQ18		56A	DQ22	MEM_A_DQ<21>	15
15 MEM_A_DQ<16>	57A	DQ19		58A	DQ23	MEM_A_DQ<17>	15
	59A	VSS23		60A	VSS24		
15 MEM_A_DQ<28>	61A	DQ24		62A	DQ28	MEM_A_DQ<29>	15
15 MEM_A_DQ<25>	63A	DQ25		64A	DQ29	MEM_A_DQ<24>	15
	65A	VSS25		66A	VSS26		
15 MEM_A_DM<3>	67A	DM3		68A	DQS3*	MEM_A_DQS_N<3>	15
NC	69A	NC1		70A	DQS3	MEM_A_DQS_P<3>	15
	71A	VSS27		72A	VSS28		
15 MEM_A_DQ<27>	73A	DQ26		74A	DQ30	MEM_A_DQ<26>	15
15 MEM_A_DQ<30>	75A	DQ27		76A	DQ31	MEM_A_DQ<31>	15
	77A	VSS29		78A	VSS30		
30 14 MEM_CKE<0>	79A	CKE0		80A	NC/CKE1	MEM_CKE<1>	14 30
	81A	VDD0		82A	VDD1		
NC	83A	NC2		84A	NC/A15	NC_MEM_A_A<15>	6
30 15 MEM_A_BS<2>	85A	BA2		86A	NC/A14	NC_MEM_A_A<14>	6
	87A	VDD2		88A	VDD3		
30 15 MEM_A_A<12>	89A	A12		90A	A11	MEM_A_A<11>	15 30
30 15 MEM_A_A<9>	91A	A9		92A	A7	MEM_A_A<7>	15 30
30 15 MEM_A_A<8>	93A	A8		94A	A6	MEM_A_A<6>	15 30
	95A	VDD4		96A	VDD5		
30 15 MEM_A_A<5>	97A	A5		98A	A4	MEM_A_A<4>	15 30
30 15 MEM_A_A<3>	99A	A3		100A	A2	MEM_A_A<2>	15 30
30 15 MEM_A_A<1>	101A	A1		102A	A0	MEM_A_A<0>	15 30
	103A	VDD6		104A	VDD7		
30 15 MEM_A_A<10>	105A	A10/AP		106A	BA1	MEM_A_BS<1>	15 30
30 15 MEM_A_BS<0>	107A	BA0		108A	RAS*	MEM_A_RAS_L	15 30
30 15 MEM_A_WE_L	109A	WE*		110A	S0*	MEM_CS_L<0>	14 30
	111A	VDD8		112A	VDD9		
30 15 MEM_A_CAS_L	113A	CAS*		114A	ODT0	MEM_ODT<0>	14 30
30 14 MEM_CS_L<1>	115A	NC/S1*		116A	NC/A13	MEM_A_A<13>	15 30
	117A	VDD10		118A	VDD11		
30 14 MEM_ODT<1>	119A	NC/ODT1		120A	NC3	NC	
	121A	VSS31		122A	VSS32		
15 MEM_A_DQ<35>	123A	DQ32		124A	DQ36	MEM_A_DQ<38>	15
15 MEM_A_DQ<39>	125A	DQ33		126A	DQ37	MEM_A_DQ<34>	15
	127A	VSS33		128A	VSS34		
15 MEM_A_DQS_N<4>	129A	DQS4*		130A	DM4	MEM_A_DM<4>	15
15 MEM_A_DQS_P<4>	131A	DQS4		132A	VSS35		
	133A	VSS36		134A	DQ38	MEM_A_DQ<32>	15
15 MEM_A_DQ<37>	135A	DQ34		136A	DQ39	MEM_A_DQ<36>	15
15 MEM_A_DQ<33>	137A	DQ35		138A	VSS37		
	139A	VSS38		140A	DQ44	MEM_A_DQ<57>	15
15 MEM_A_DQ<60>	141A	DQ40		142A	DQ45	MEM_A_DQ<63>	15
15 MEM_A_DQ<59>	143A	DQ41		144A	VSS39		
	145A	VSS40		146A	DQS5*	MEM_A_DQS_N<7>	15
15 MEM_A_DM<7>	147A	DM5		148A	DQS5	MEM_A_DQS_P<7>	15
	149A	VSS41		150A	VSS42		
15 MEM_A_DQ<58>	151A	DQ42		152A	DQ46	MEM_A_DQ<56>	15
15 MEM_A_DQ<61>	153A	DQ43		154A	DQ47	MEM_A_DQ<62>	15
	155A	VSS43		156A	VSS44		
15 MEM_A_DQ<43>	157A	DQ48		158A	DQ52	MEM_A_DQ<40>	15
15 MEM_A_DQ<45>	159A	DQ49		160A	DQ53	MEM_A_DQ<42>	15
	161A	VSS45		162A	VSS46		
NC	163A	NC_TEST		164A	CK1	MEM_CLK_P<1>	14
	165A	VSS47		166A	CK1*	MEM_CLK_N<1>	14
15 MEM_A_DQS_N<5>	167A	DQS6*		168A	VSS48		
15 MEM_A_DQS_P<5>	169A	DQS6		170A	DM6	MEM_A_DM<5>	15
	171A	VSS49		172A	VSS50		
15 MEM_A_DQ<41>	173A	DQ50		174A	DQ54	MEM_A_DQ<47>	15
15 MEM_A_DQ<46>	175A	DQ51		176A	DQ55	MEM_A_DQ<44>	15
	177A	VSS51		178A	VSS52		
15 MEM_A_DQ<51>	179A	DQ56		180A	DQ60	MEM_A_DQ<54>	15
15 MEM_A_DQ<50>	181A	DQ57		182A	DQ61	MEM_A_DQ<55>	15
	183A	VSS53		184A	VSS54		
15 MEM_A_DM<6>	185A	DM7		186A	DQS7*	MEM_A_DQS_N<6>	15
	187A	VSS55		188A	DQS7	MEM_A_DQS_P<6>	15
15 MEM_A_DQ<53>	189A	DQ58		190A	VSS56		
15 MEM_A_DQ<48>	191A	DQ59		192A	DQ62	MEM_A_DQ<52>	15
	193A	VSS57		194A	DQ63	MEM_A_DQ<49>	15
PP3V3_S0				196A	VSS58		
SMBUS_SB_SDA	195A	SDA		198A	SA0		
SMBUS_SB_SCL	197A	SCL		200A	SA1	ADDR=0xA0(WR)/0xA1(RD)	
	199A	VDDSPD					

516S0471 202 204 NC

203 201 NC

PP1V8_S3

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C2808 10UF 20% 6.3V X6S 603

C2809 10UF 20% 6.3V X6S 603

C2810 0.1uF 20% 10V CERM 402

C2811 0.1uF 20% 10V CERM 402

C2812 0.1uF 20% 10V CERM 402

C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402

C2815 0.1uF 20% 10V CERM 402

C2816 0.1uF 20% 10V CERM 402

C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402

C2819 0.1uF 20% 10V CERM 402

C2820 0.1uF 20% 10V CERM 402

C2821 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 28 OF 86	

Page Notes

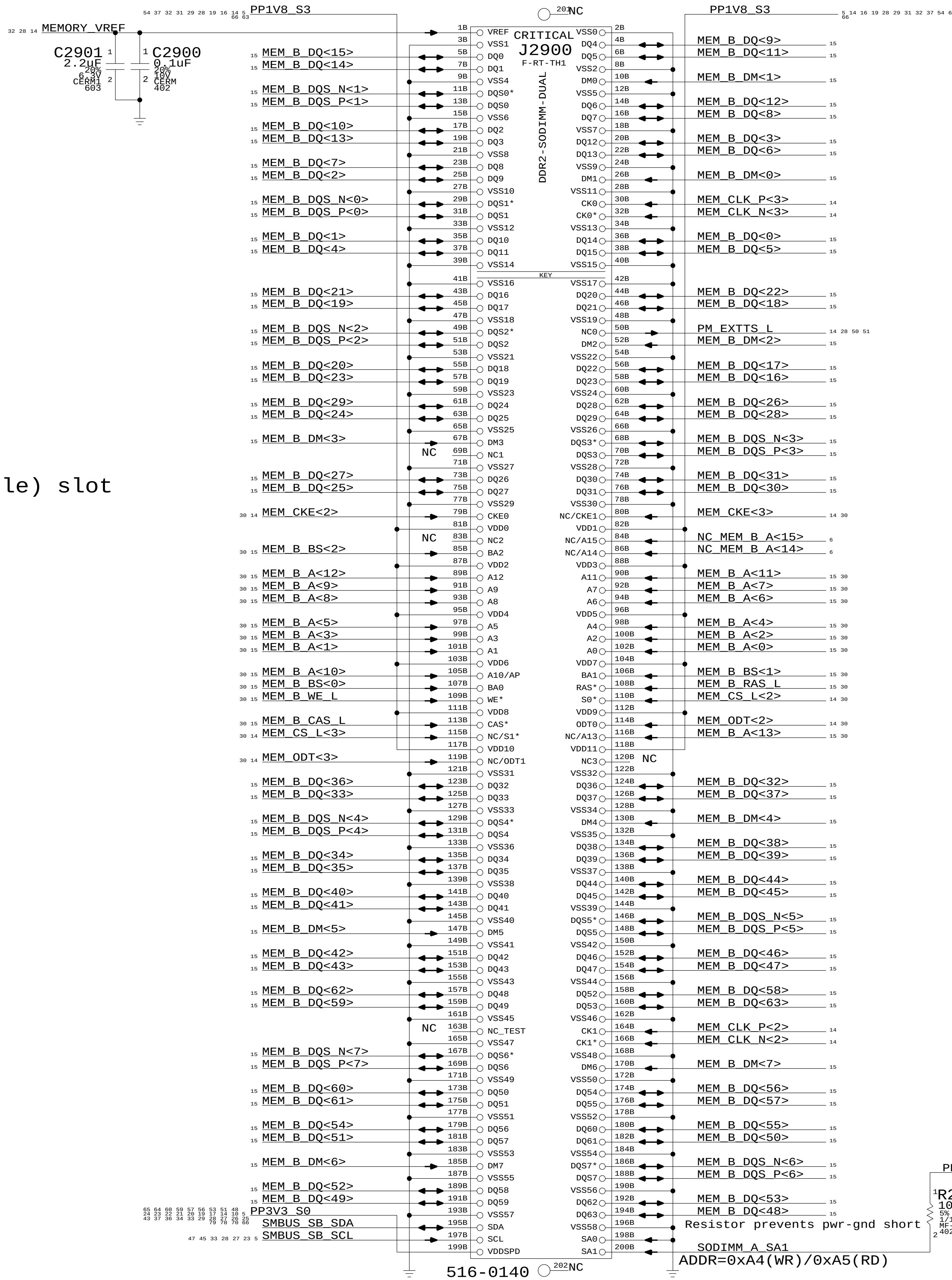
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

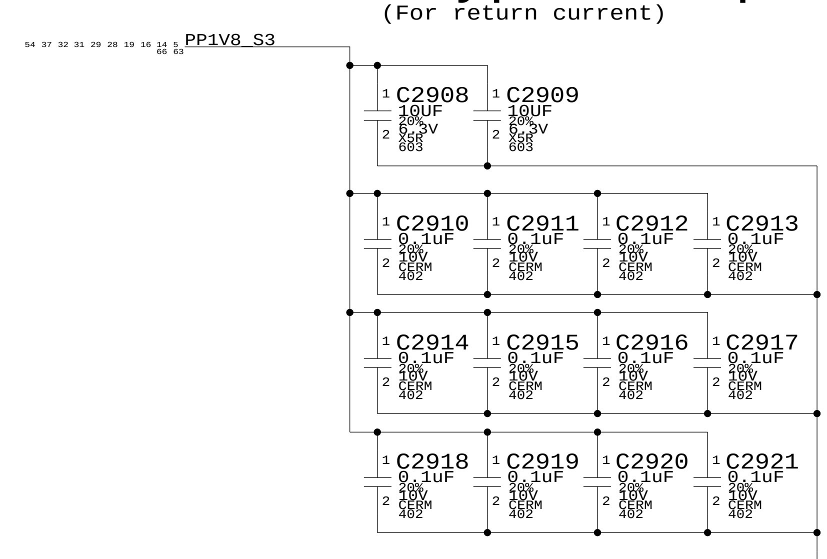
NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Upper" (thru-hole) slot



DDR2 Bypass Caps

(For return current)



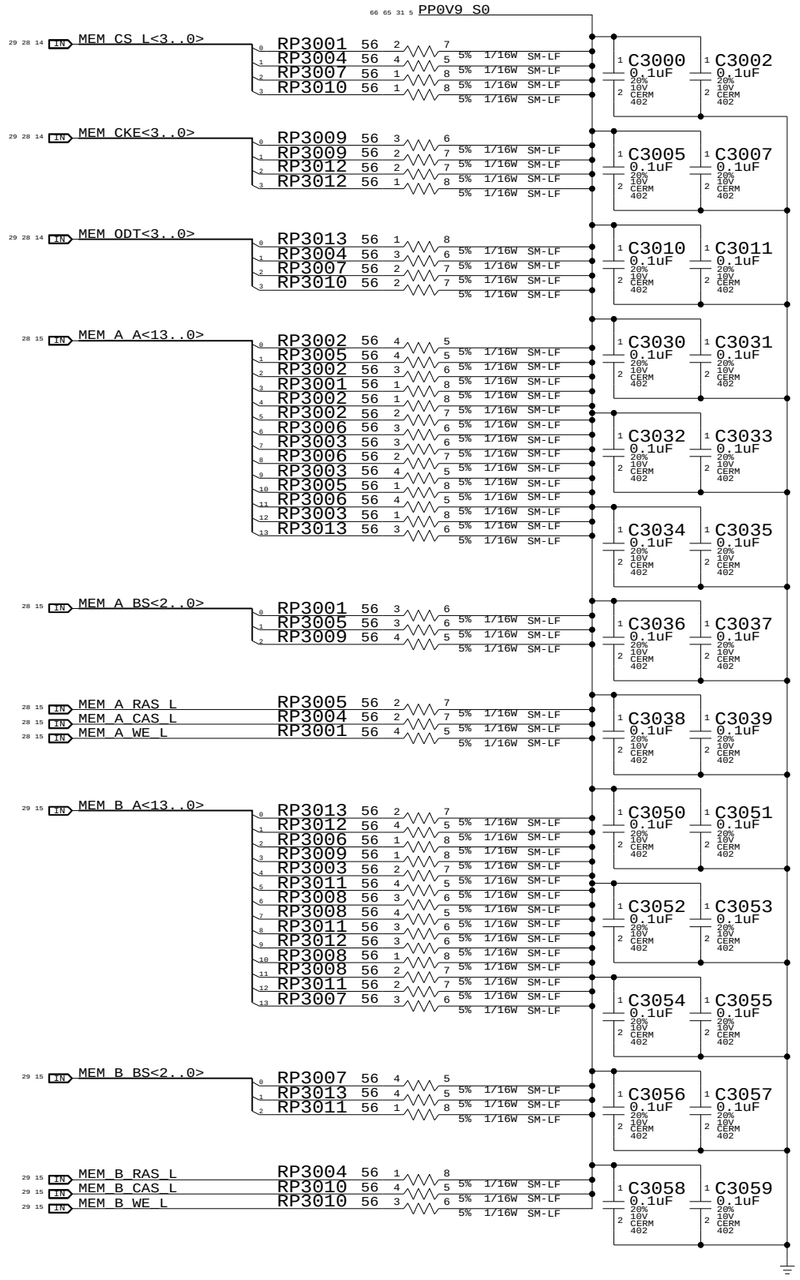
DDR2 SO-DIMM Connector B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHT 29	OF 86

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/07/2006)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 30 OF 86	

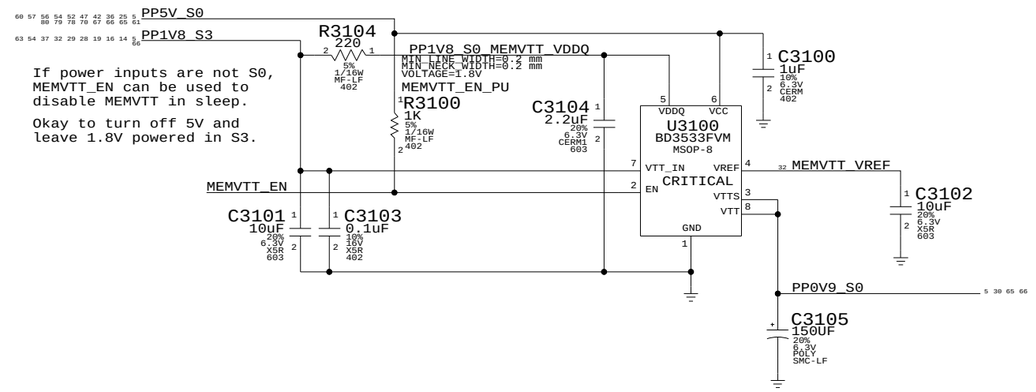
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

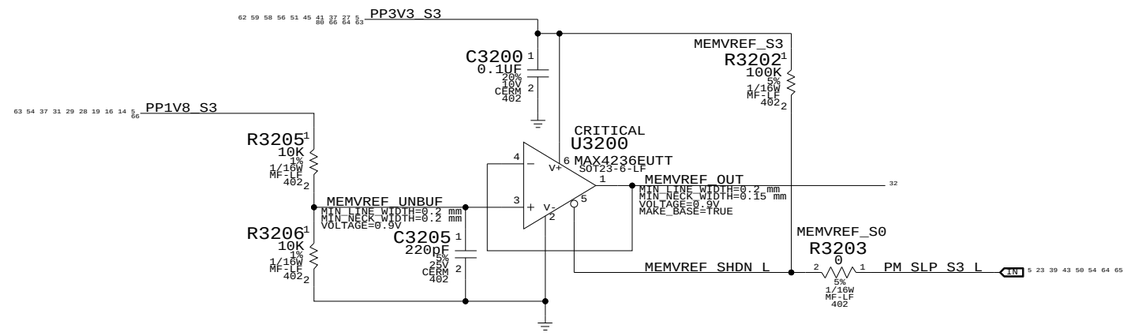
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE: NONE

SHT 31 OF 86

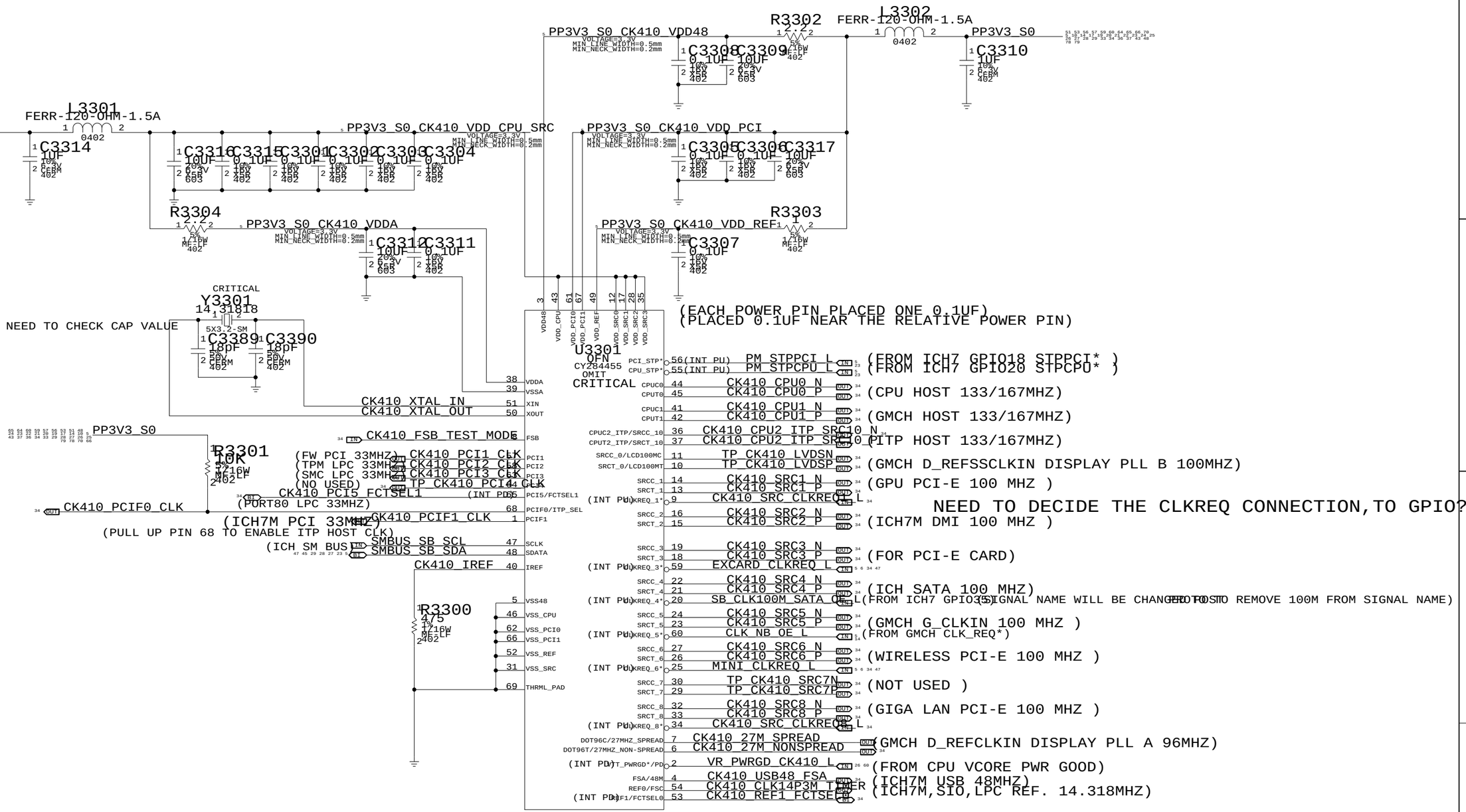


DDR2 VRef

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 32 OF 86	



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SS	T100MC_SS	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

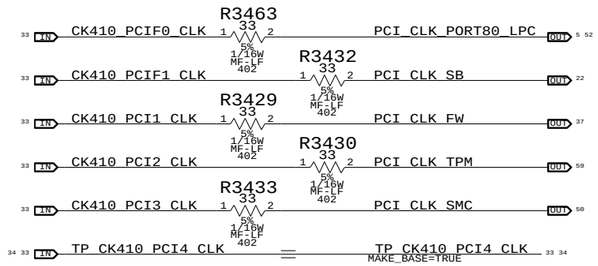
CLOCKS

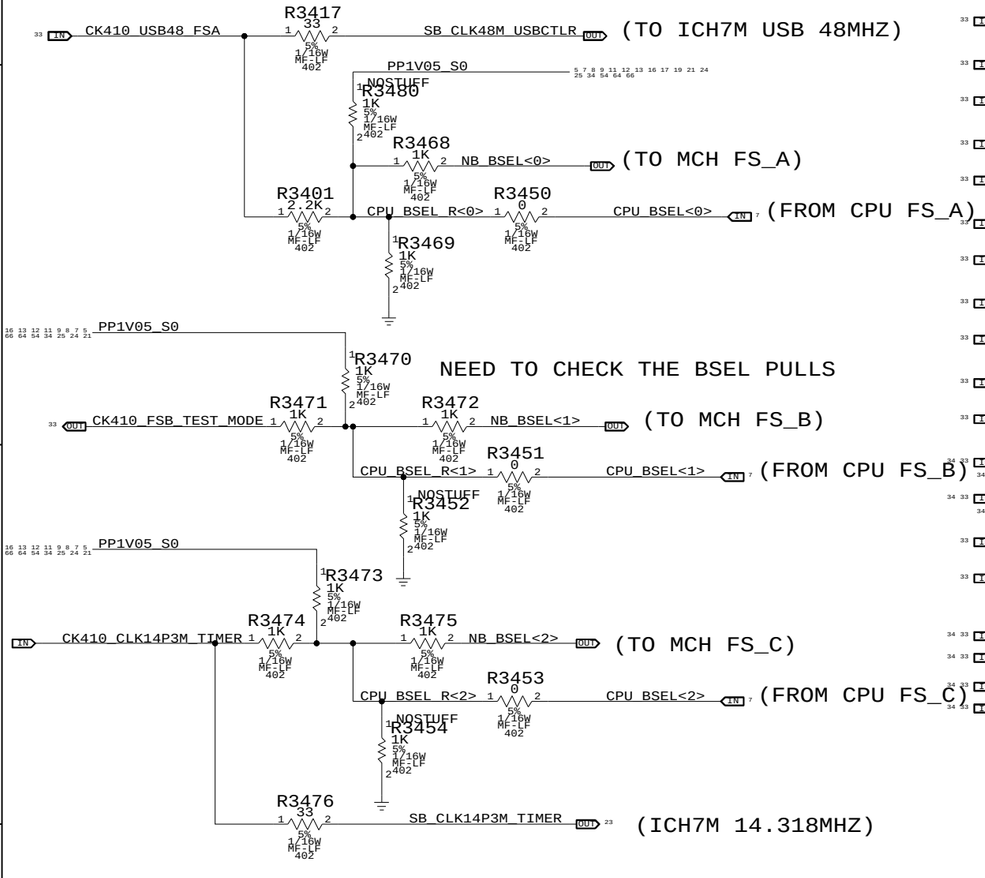
SYNC_MASTER=MS_NCB SYNC_DATE=02/10/2006

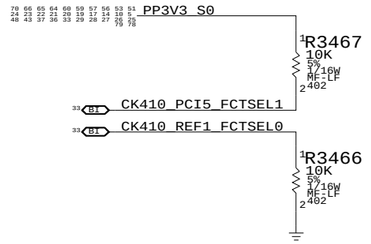
APPLE COMPUTER INC.

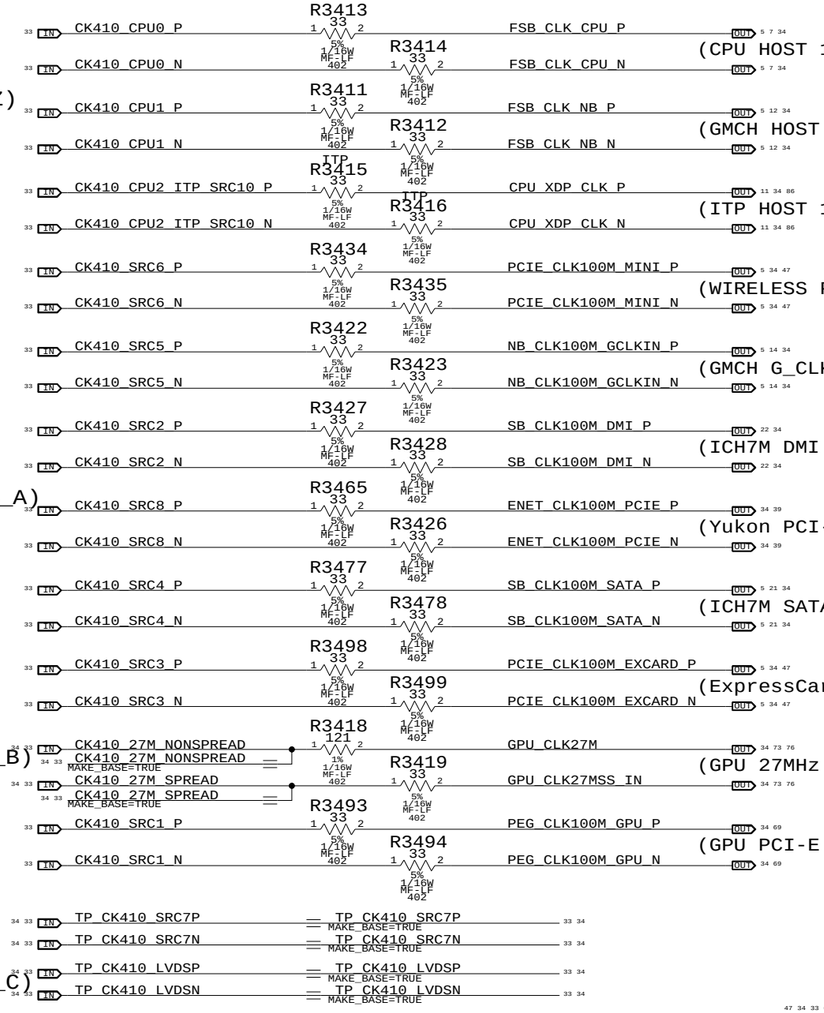
SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	33	86









NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

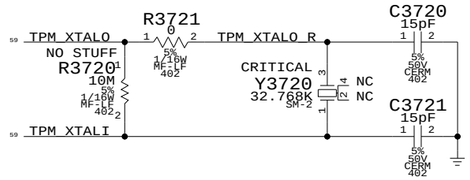
Clock Termination

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

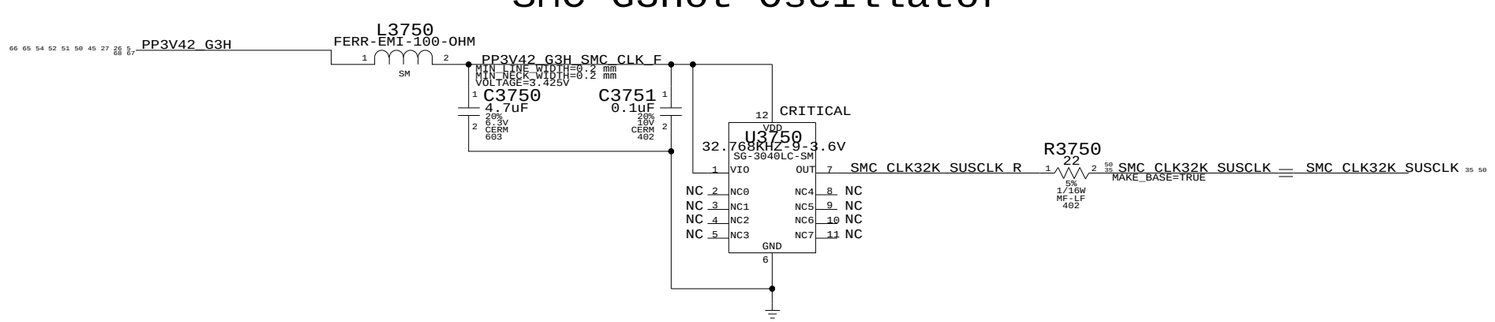
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 34 OF 86	

TPM Crystal Circuit



SMC G3Hot Oscillator



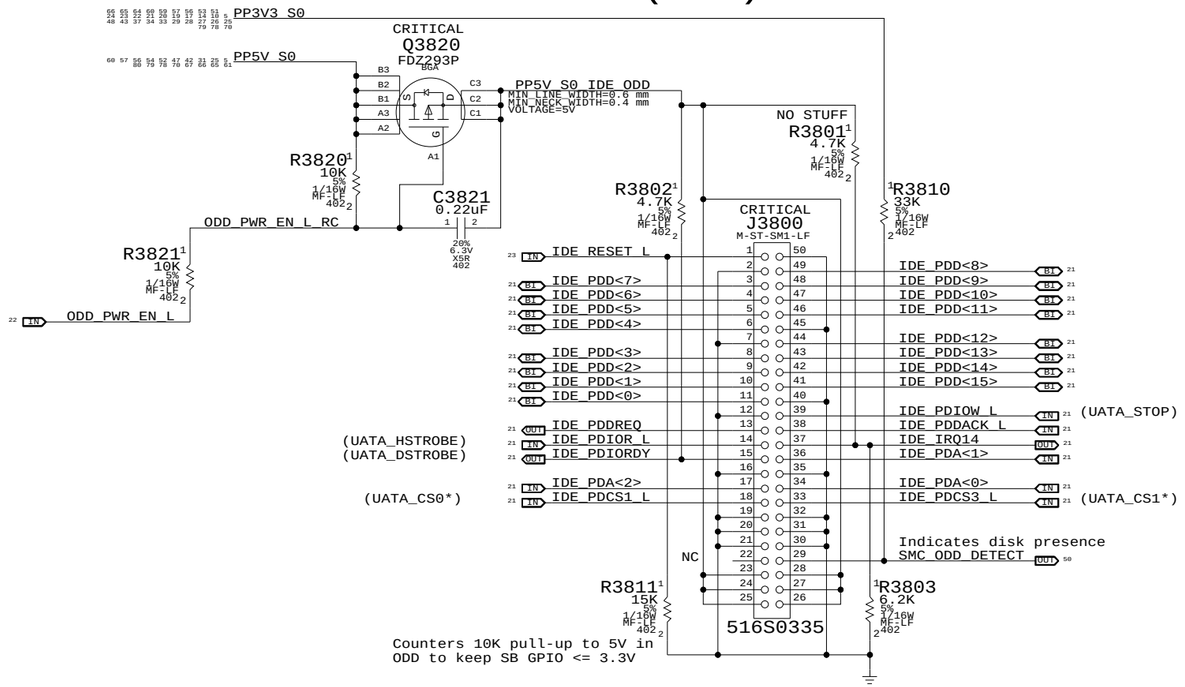
Mobile Clocking

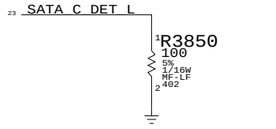
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

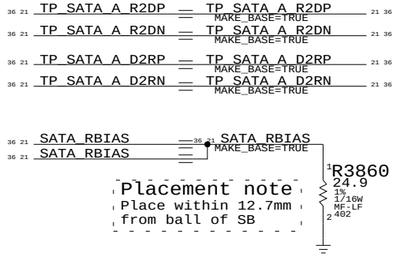
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 35 OF 86	

IDE (ODD) Connector





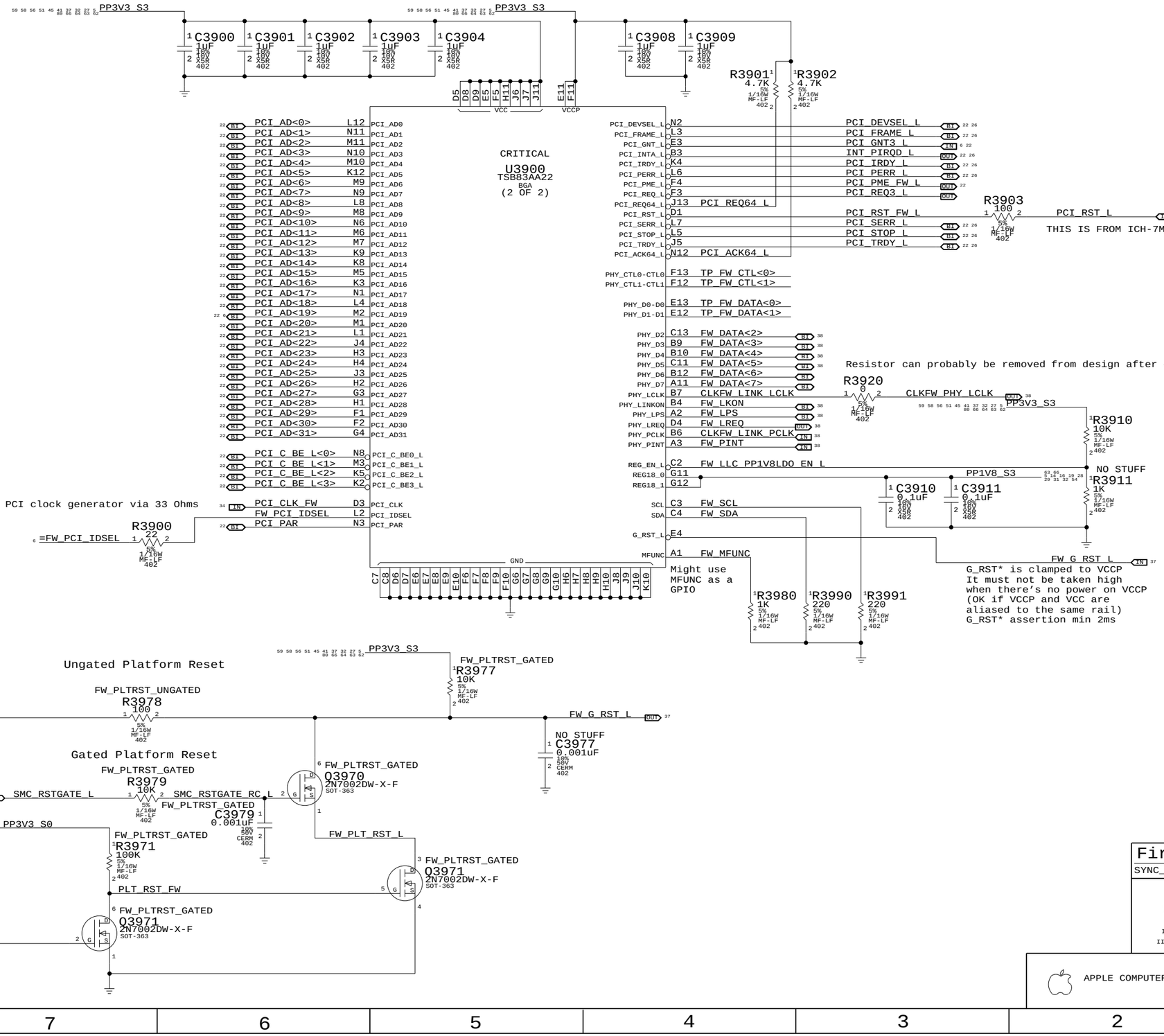


PATA Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 36 OF 86	


PP3V3_S3
C3900 1uF 16V X5R 402
C3901 1uF 16V X5R 402
C3902 1uF 16V X5R 402
C3903 1uF 16V X5R 402
C3904 1uF 16V X5R 402
C3908 1uF 16V X5R 402
C3909 1uF 16V X5R 402
R3901 4.7K 5% 1/16W MF-LF 402
R3902 4.7K 5% 1/16W MF-LF 402
D5 D8 D9 E5 F5 H11 J6 J7 J11
E11 F11
VCC
VCCP
CRITICAL
U3900
TSB83AA22
BGA
(2 OF 2)
PCI_AD<0> L12 PCI_AD0
PCI_AD<1> N11 PCI_AD1
PCI_AD<2> M11 PCI_AD2
PCI_AD<3> N10 PCI_AD3
PCI_AD<4> M10 PCI_AD4
PCI_AD<5> K12 PCI_AD5
PCI_AD<6> M9 PCI_AD6
PCI_AD<7> N9 PCI_AD7
PCI_AD<8> L8 PCI_AD8
PCI_AD<9> M8 PCI_AD9
PCI_AD<10> N6 PCI_AD10
PCI_AD<11> M6 PCI_AD11
PCI_AD<12> M7 PCI_AD12
PCI_AD<13> K9 PCI_AD13
PCI_AD<14> K8 PCI_AD14
PCI_AD<15> M5 PCI_AD15
PCI_AD<16> K3 PCI_AD16
PCI_AD<17> N1 PCI_AD17
PCI_AD<18> L4 PCI_AD18
PCI_AD<19> M2 PCI_AD19
PCI_AD<20> M1 PCI_AD20
PCI_AD<21> L1 PCI_AD21
PCI_AD<22> J4 PCI_AD22
PCI_AD<23> H3 PCI_AD23
PCI_AD<24> H4 PCI_AD24
PCI_AD<25> J3 PCI_AD25
PCI_AD<26> H2 PCI_AD26
PCI_AD<27> G3 PCI_AD27
PCI_AD<28> H1 PCI_AD28
PCI_AD<29> F1 PCI_AD29
PCI_AD<30> F2 PCI_AD30
PCI_AD<31> G4 PCI_AD31
PCI_C_BE_L<0> N8 PCI_C_BE0_L
PCI_C_BE_L<1> M3 PCI_C_BE1_L
PCI_C_BE_L<2> K5 PCI_C_BE2_L
PCI_C_BE_L<3> K2 PCI_C_BE3_L
From PCI clock generator via 33 Ohms
PCI_CLK_FW D3 PCI_CLK
FW_PCI_IDSEL L2 PCI_IDSEL
PCI_PAR N3 PCI_PAR
=FW_PCI_IDSEL
R3900 22 5% 1/16W MF-LF 402
GND
C7 C8 D6 D7 E6 E7 E8 E9 E10 F6 F7 F8 F9 F10 G6 G7 G8 G9 G10 H6 H7 H8 H9 H10 J8 J9 J10 K10
PCI_DEVSEL_L N2 PCI_DEVSEL_L
PCI_FRAME_L L3 PCI_FRAME_L
PCI_GNT_L E3 PCI_GNT3_L
PCI_INTA_L B3 INT_PIROD_L
PCI_IRDY_L K4 PCI_IRDY_L
PCI_PERR_L L6 PCI_PERR_L
PCI_PME_L F4 PCI_PME_FW_L
PCI_REQ_L F3 PCI_REQ3_L
PCI_REQ64_L J13 PCI_REQ64_L
PCI_RST_L D1 PCI_RST_FW_L
PCI_SERR_L L7 PCI_SERR_L
PCI_STOP_L L5 PCI_STOP_L
PCI_TRDY_L J5 PCI_TRDY_L
PCI_ACK64_L N12 PCI_ACK64_L
R3903 100 5% 1/16W MF-LF 402
PCI_RST_L
THIS IS FROM ICH-7M
PHY_CTL0-CTL0 F13 TP_FW_CTL<0>
PHY_CTL1-CTL1 F12 TP_FW_CTL<1>
PHY_D0-D0 E13 TP_FW_DATA<0>
PHY_D1-D1 E12 TP_FW_DATA<1>
PHY_D2 C13 FW_DATA<2>
PHY_D3 B9 FW_DATA<3>
PHY_D4 B10 FW_DATA<4>
PHY_D5 C11 FW_DATA<5>
PHY_D6 B12 FW_DATA<6>
PHY_D7 A11 FW_DATA<7>
PHY_LCLK B7 CLKFW_LINK_LCLK
PHY_LINKON B4 FW_LKON
PHY_LPS A2 FW_LPS
PHY_LREQ D4 FW_LREQ
PHY_PCLK B6 CLKFW_LINK_PCLK
PHY_PINT A3 FW_PINT
REG_EN_L C2 FW_LLC_PP1V8LDO_EN_L
REG18_0 G11
REG18_1 G12
SCL C3 FW_SCL
SDA C4 FW_SDA
G_RST_L E4
MFUNC A1 FW_MFUNC
Might use MFUNC as a GPIO
Resistor can probably be removed from design after evaluation
R3920 0 5% 1/16W MF-LF 402
CLKFW_PHY_LCLK
PP3V3_S3
R3910 10K 5% 1/16W MF-LF 402
NO STUFF
R3911 1K 5% 1/16W MF-LF 402
PP1V8_S3
C3910 0.1uF 10% 16V X5R 402
C3911 0.1uF 10% 16V X5R 402
FW_G_RST_L
G_RST* is clamped to VCCP
It must not be taken high when there's no power on VCCP (OK if VCCP and VCC are aliased to the same rail)
G_RST* assertion min 2ms
R3980 1K 5% 1/16W MF-LF 402
R3990 220 5% 1/16W MF-LF 402
R3991 220 5% 1/16W MF-LF 402
Ungated Platform Reset
PP3V3_S3
FW_PLTRST_GATED
R3977 10K 5% 1/16W MF-LF 402
FW_PLTRST_UNGATED
R3978 100 5% 1/16W MF-LF 402
PLT_RST_BUF_L
FW_G_RST_L
NO STUFF
C3977 0.001uF 10% 50V CERM 402
Gated Platform Reset
FW_PLTRST_GATED
R3979 10K 5% 1/16W MF-LF 402
SMC_RSTGATE_L
SMC_RSTGATE_RC_L
Q3970 2N7002DW-X-F SOT-363
C3979 0.001uF 10% 50V CERM 402
PP3V3_S0
R3971 100K 5% 1/16W MF-LF 402
FW_PLT_RST_L
Q3971 2N7002DW-X-F SOT-363
PLT_RST_FW
Q3971 2N7002DW-X-F SOT-363
FireWire Link (TSB83AA22)
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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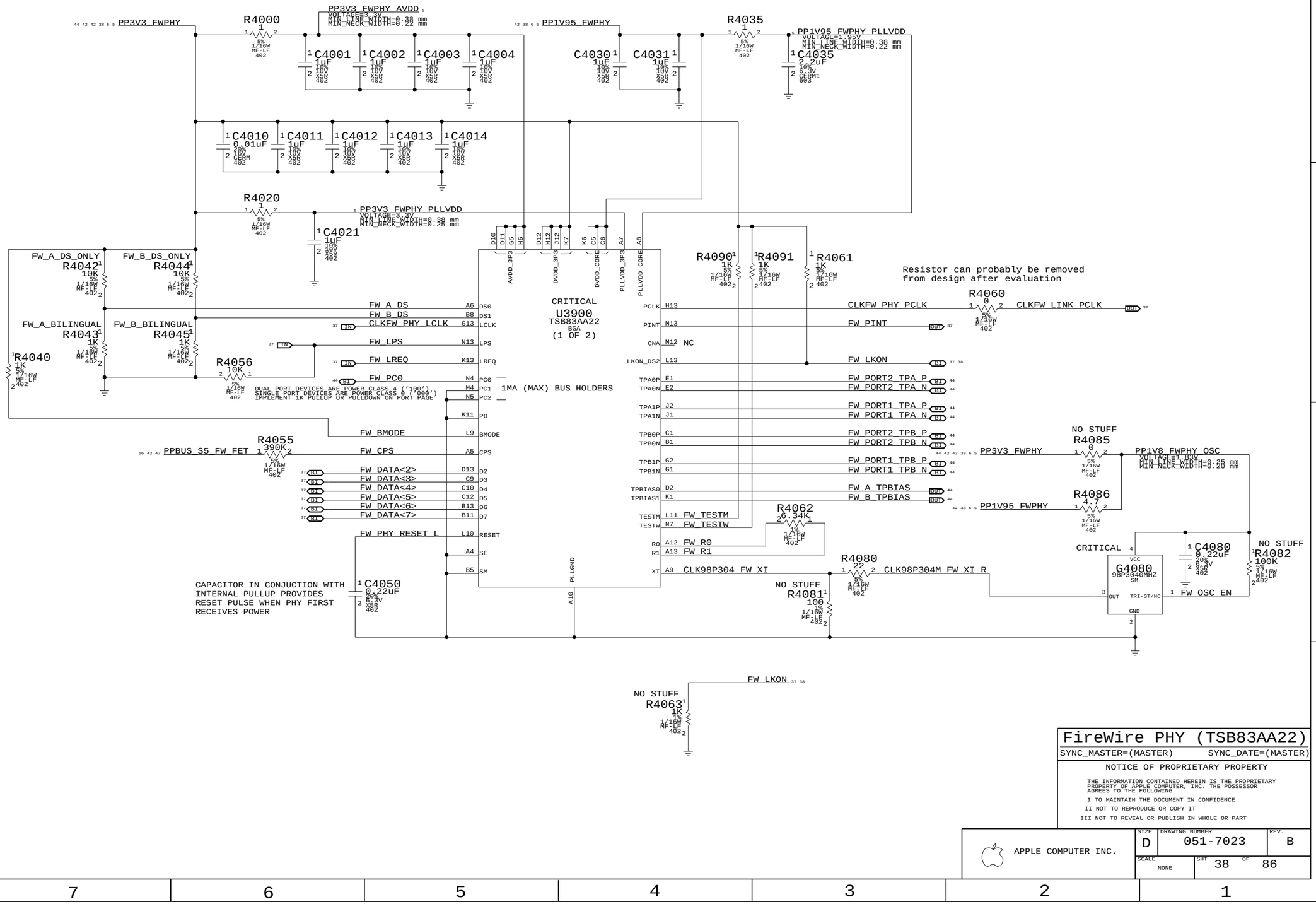
SIZE D
DRAWING NUMBER 051-7023
REV. B
SCALE NONE
SHT 37 OF 86



FireWire PHY (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 38 OF 86	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01 MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402 PP2V5_S3

PLACE C4107 NEAR U4101 AVDD

PP3V3_S3AC
R4101 4.7K 5% 1/16W MF-LF 402

PP1V2_S3
PP3V3_S3AC

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N

ENET_LOM_DIS_L
PM_SLP_S3_L

OMIT
CRITICAL
U4101
88E8053
QFN

OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED

ANALOG
PCI EXPRESS
LED
MEDIA
TEST
TWSI
SPI
MAIN CLK

PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

C4113 0.1UF 10% 16V X5R 402

NC_ENET_CTRL25
NC_ENET_CTRL12
ENET_RSET

R4102 4.87K 1% 1/16W MF-LF 402

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDIO
ENET_MDI1
ENET_MDI2
ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053
INTERNAL PULL-UP

CRITICAL
ENET_XTALI
ENET_XTALO

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

THRML_PAD

PLACE RESISTORS CLOSE TO U4101

PP3V3_S3AC
R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08
SO8

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

PP1V2_S3
C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

PP3V3_S3AC
C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 39 OF 86	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 40
	ENETCONN	ENET_100D	ENETCONN_N<0> 40
	ENETCONN	ENET_100D	ENETCONN_P<1> 40
	ENETCONN	ENET_100D	ENETCONN_N<1> 40
	ENETCONN	ENET_100D	ENETCONN_P<2> 40
	ENETCONN	ENET_100D	ENETCONN_N<2> 40
	ENETCONN	ENET_100D	ENETCONN_P<3> 40
	ENETCONN	ENET_100D	ENETCONN_N<3> 40

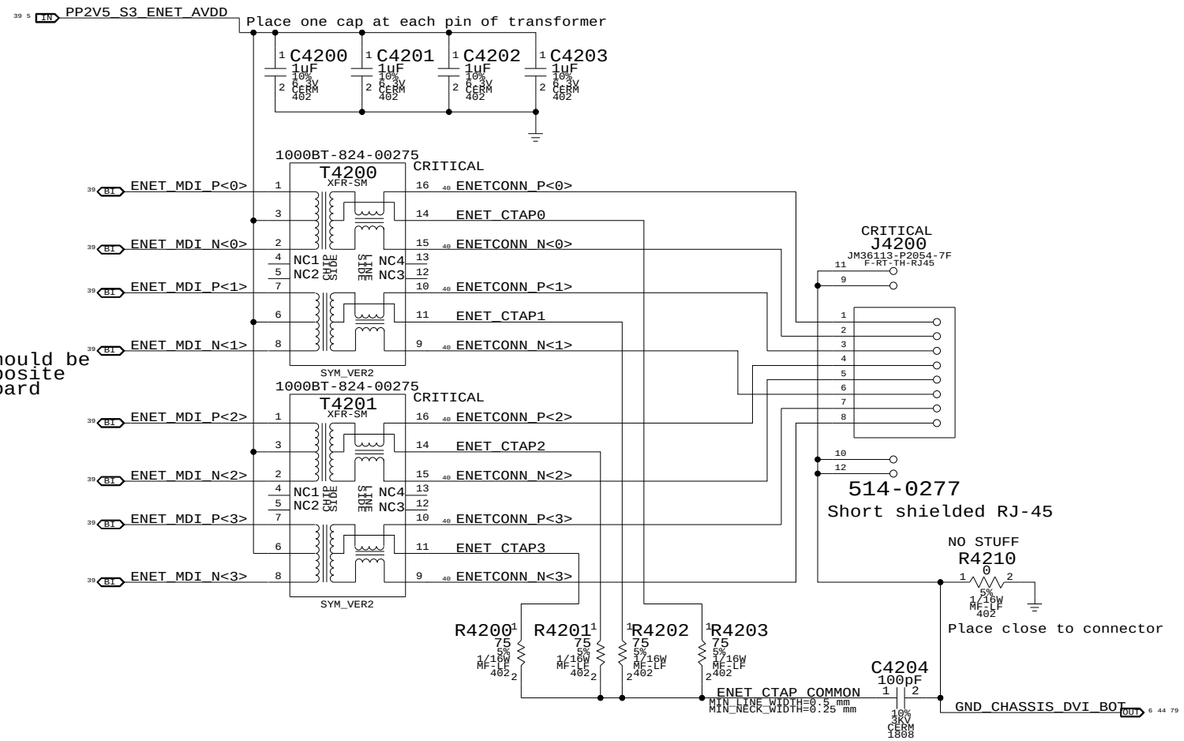
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

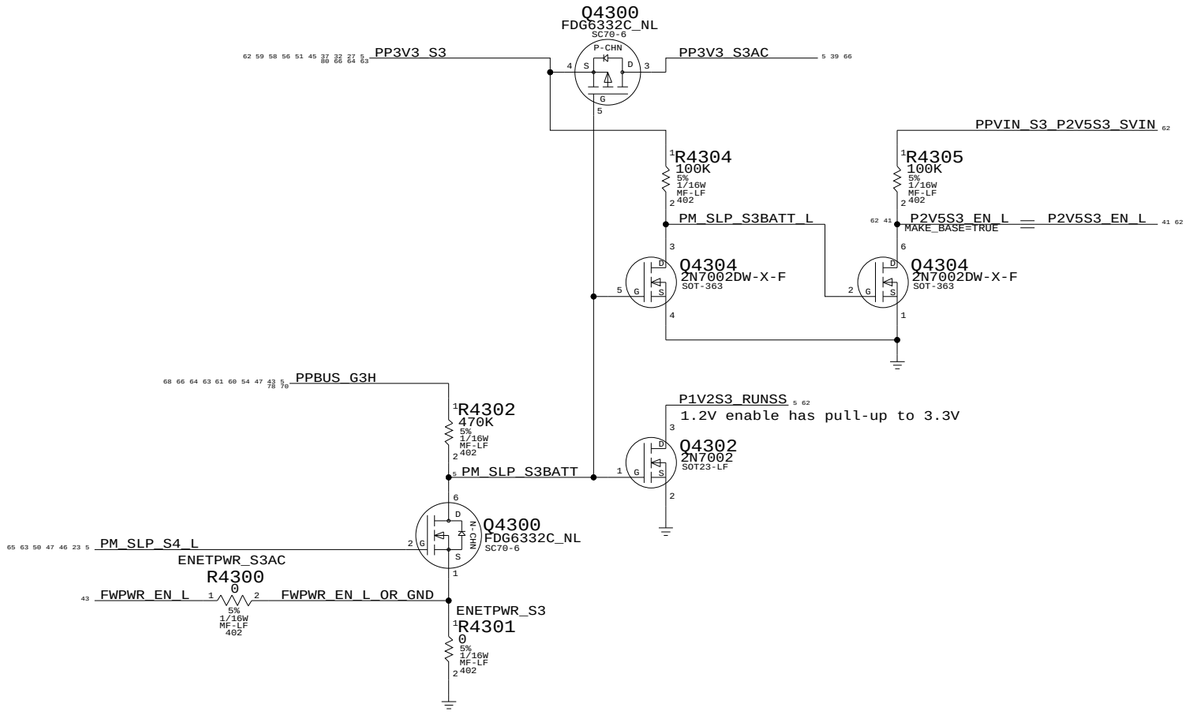
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 40 OF 86	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

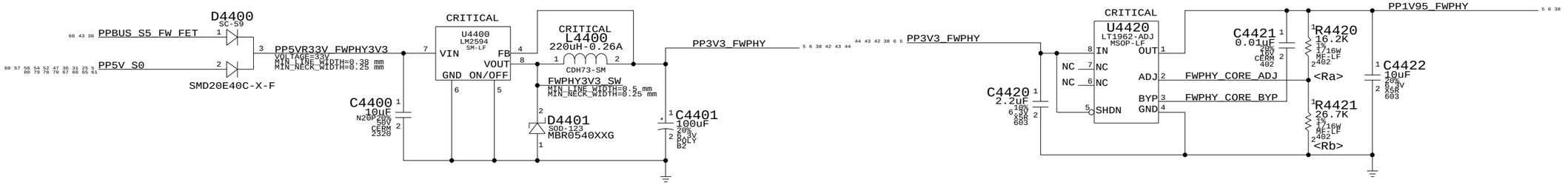
Yukon Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 41 OF 86	

165MA MAX LOAD



Vout = 1.22V * (1 + Ra/Rb) + (Iadj * Ra)
Iadj = 30nA @ 25 deg C

FW PHY Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 42 OF 86	

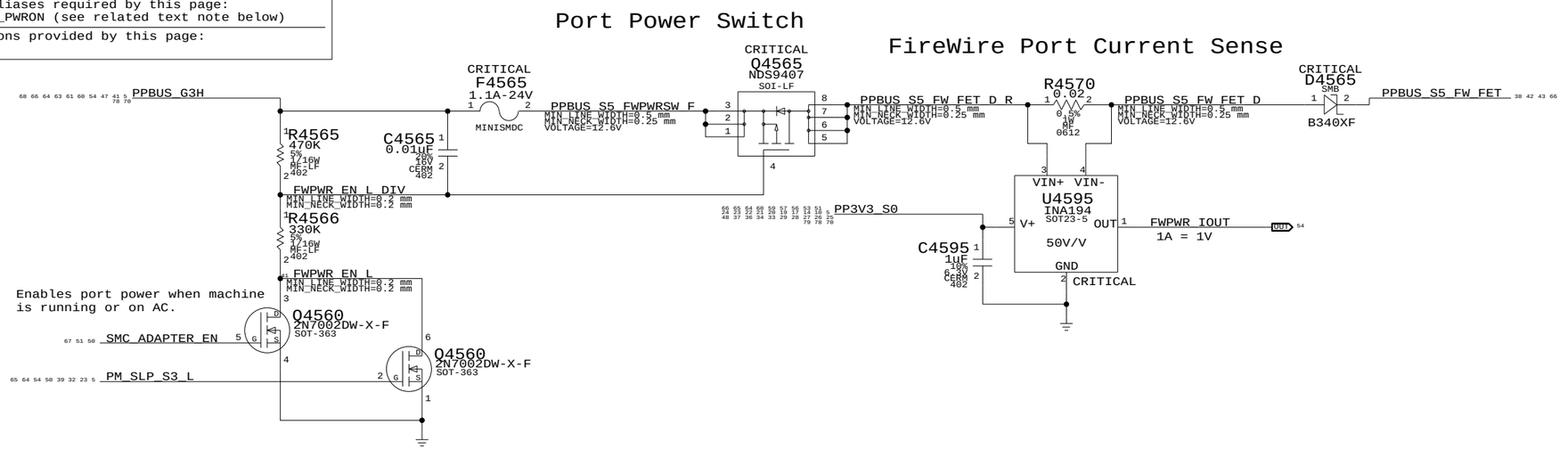
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

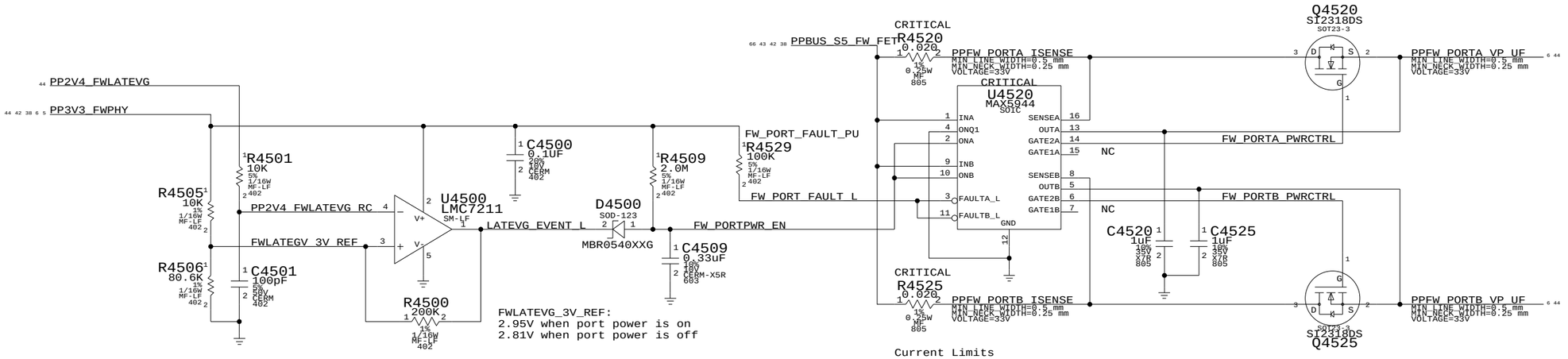
Port Power Switch



FireWire Port Current Sense

Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/03/2005)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 43 OF 86	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED	FW	FW_110D	FW_PORT1_TPA_FL_P 44
	FW	FW_110D	FW_PORT1_TPA_FL_N 44
BY	FW	FW_110D	FW_PORT1_TPB_FL_P 44
	FW	FW_110D	FW_PORT1_TPB_FL_N 44
PHY	FW	FW_110D	FW_PORT2_TPA_FL_P 44
	FW	FW_110D	FW_PORT2_TPA_FL_N 44
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_P 44
	FW	FW_110D	FW_PORT2_TPB_FL_N 44

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

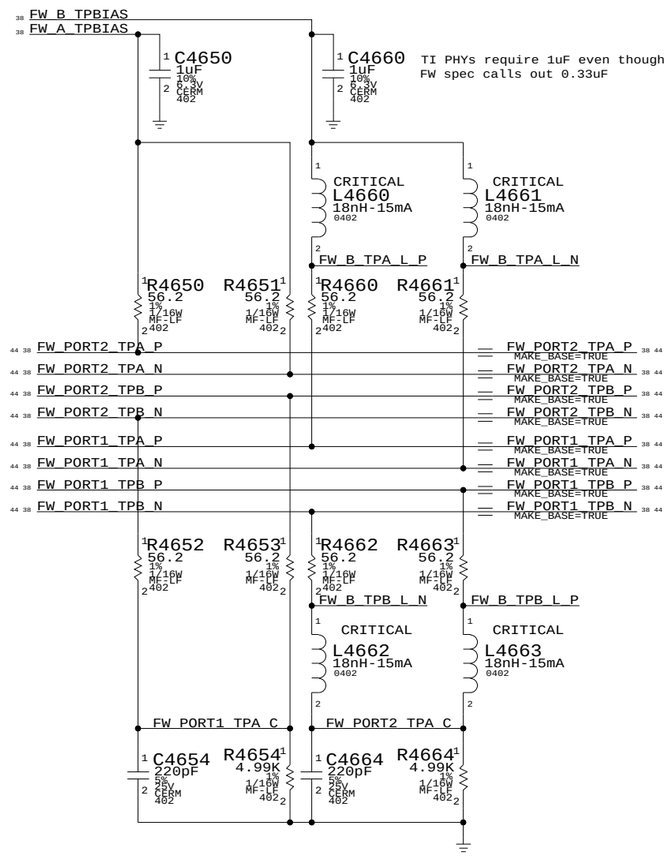
AREF needs to be isolated from all local grounds per 1394b spec

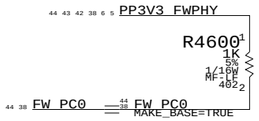
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Termination

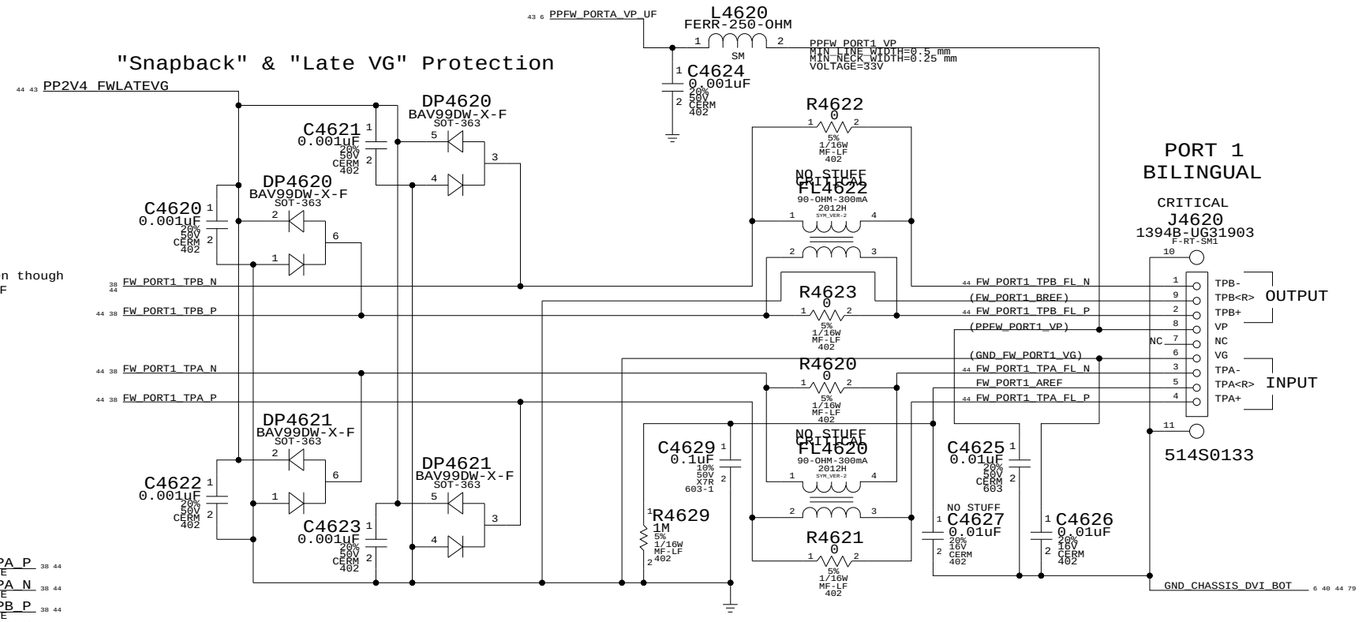
Place close to FireWire PHY





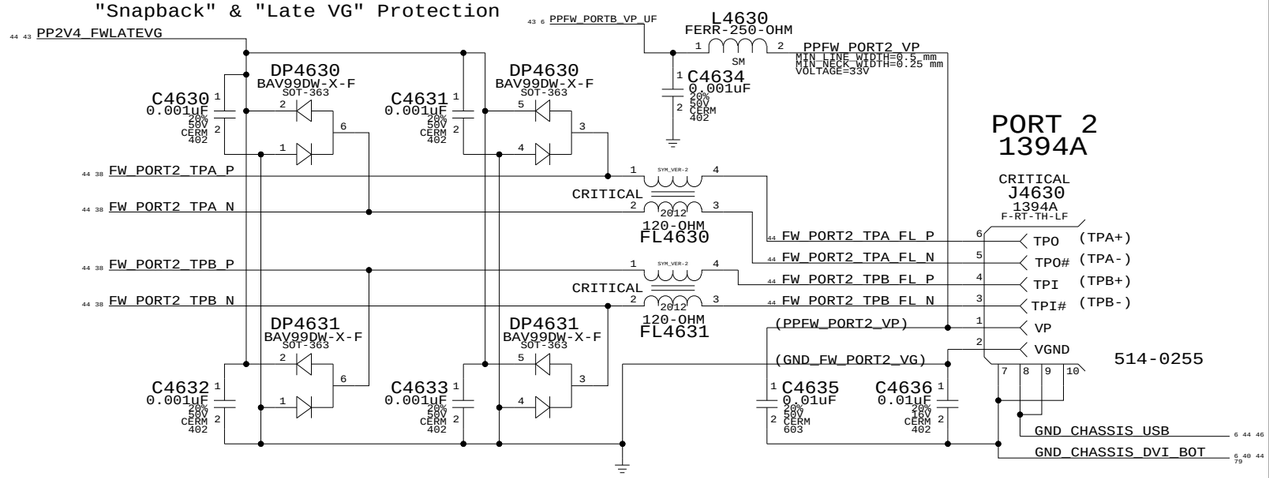
Cable Power

"Snapback" & "Late VG" Protection

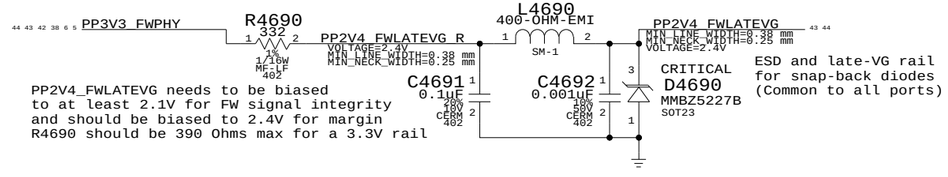


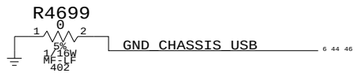
Cable Power

"Snapback" & "Late VG" Protection



Late-VG Protection Power





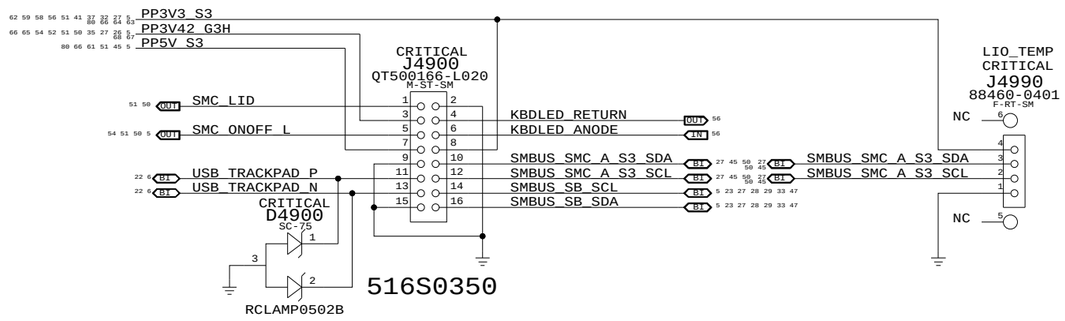
FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

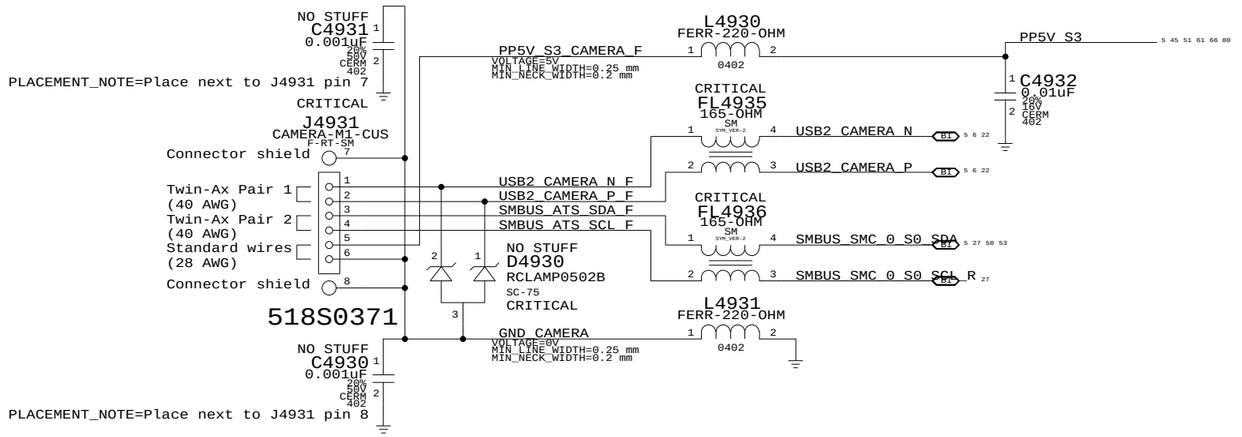
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 44 OF 86	

Top-Case Connector



Camera Connector



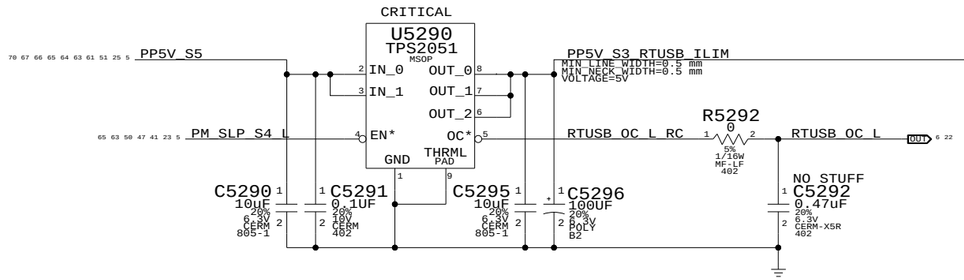
Internal USB Connections

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

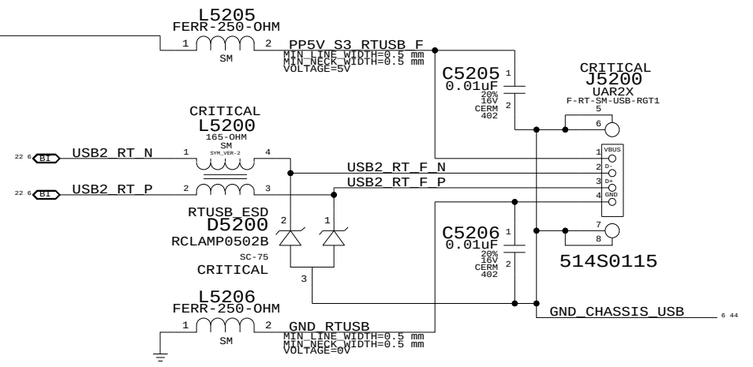
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 45 OF 86	

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

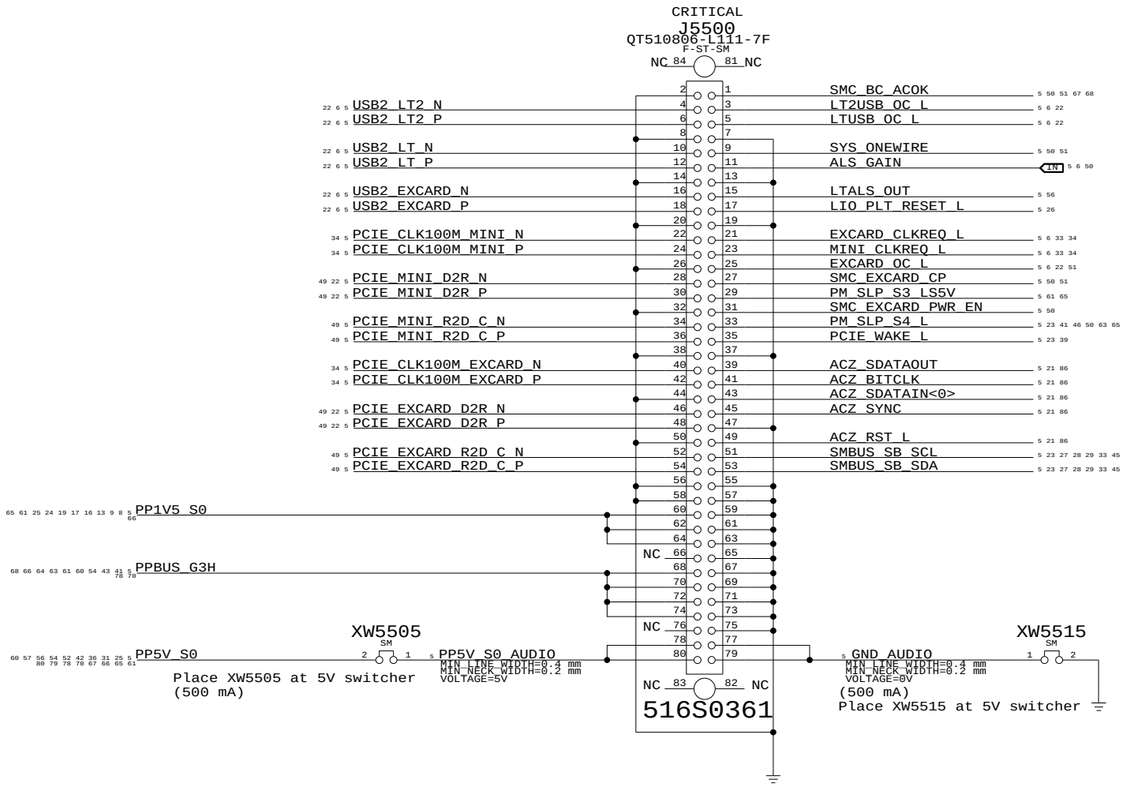
External USB Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 46 OF 86	

Left I/O Board Connector



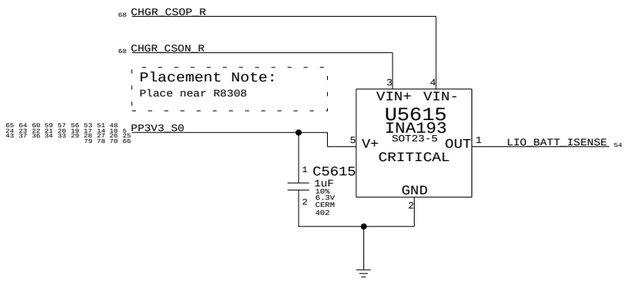
Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

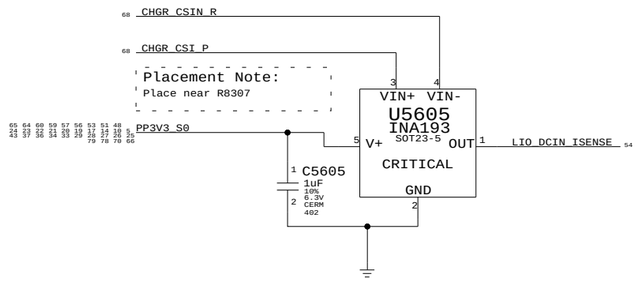
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 47 OF 86	

Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor

Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 48 OF 86	

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

PCIE_MINI_R2D_C_P — C5710 0.1uF 10% 16V X5R 402 — PCIE_MINI_R2D_C_P (MAKE_BASE=TRUE) — PCIE_B_R2D_C_P

PCIE_MINI_R2D_C_N — C5711 0.1uF 10% 16V X5R 402 — PCIE_MINI_R2D_C_N (MAKE_BASE=TRUE) — PCIE_B_R2D_C_N

Place caps close to SB

PCIE_MINI_D2R_P — PCIE_MINI_D2R_P (MAKE_BASE=TRUE) — PCIE_MINI_D2R_P

PCIE_MINI_D2R_N — PCIE_MINI_D2R_N (MAKE_BASE=TRUE) — PCIE_MINI_D2R_N

PCI-E x1 Port "C" = ExpressCard

PCIE_EXCARD_R2D_C_P — C5720 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_C_P (MAKE_BASE=TRUE) — PCIE_C_R2D_C_P

PCIE_EXCARD_R2D_C_N — C5721 0.1uF 10% 16V X5R 402 — PCIE_EXCARD_R2D_C_N (MAKE_BASE=TRUE) — PCIE_C_R2D_C_N

Place caps close to SB

PCIE_EXCARD_D2R_P — PCIE_EXCARD_D2R_P (MAKE_BASE=TRUE) — PCIE_EXCARD_D2R_P

PCIE_EXCARD_D2R_N — PCIE_EXCARD_D2R_N (MAKE_BASE=TRUE) — PCIE_EXCARD_D2R_N

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP (MAKE_BASE=TRUE) — TP_PCIE_D_R2DP

TP_PCIE_D_R2DN (MAKE_BASE=TRUE) — TP_PCIE_D_R2DN

TP_PCIE_D_D2RP (MAKE_BASE=TRUE) — TP_PCIE_D_D2RP

TP_PCIE_D_D2RN (MAKE_BASE=TRUE) — TP_PCIE_D_D2RN

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP (MAKE_BASE=TRUE) — TP_PCIE_E_R2DP

TP_PCIE_E_R2DN (MAKE_BASE=TRUE) — TP_PCIE_E_R2DN

TP_PCIE_E_D2RP (MAKE_BASE=TRUE) — TP_PCIE_E_D2RP

TP_PCIE_E_D2RN (MAKE_BASE=TRUE) — TP_PCIE_E_D2RN

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP (MAKE_BASE=TRUE) — TP_PCIE_F_R2DP

TP_PCIE_F_R2DN (MAKE_BASE=TRUE) — TP_PCIE_F_R2DN

TP_PCIE_F_D2RP (MAKE_BASE=TRUE) — TP_PCIE_F_D2RP

TP_PCIE_F_D2RN (MAKE_BASE=TRUE) — TP_PCIE_F_D2RN

PCI-E Connections

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

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SCALE: NONE	SHT 49 OF 86	

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	
SMC_RSTGATE_L	C13	P11	
ALL_SYS_PWRGD	A15	P12	
RSMRST_PWRGD	B14	P13	
SMC_SB_NMI	B15	P14	
PM_RSMRST_L	C14	P15	
IMVP_VR_ON	D12	P16	
PM_PWRBTN_L	C15	P17	
TP_SMC_P20	D13	P20	
TP_SMC_P21	D14	P21	
TP_SMC_P22	D15	P22	
TP_SMC_P23	E12	P23	
SMC_BATT_TRICKLE_EN	E14	P24	
SMC_BATT_CHG_EN	E15	P25	
TP_SMC_P26	E13	P26	
TP_SMC_P27	F14	P27	
LPC_AD<0>	D9	P30/LAD0	
LPC_AD<1>	C9	P31/LAD1	
LPC_AD<2>	A9	P32/LAD2	
LPC_AD<3>	B9	P33/LAD3	
LPC_FRAME_L	D8	P34/LFRAME*	
SMC_LRESET_L	C8	P35/LRESET*	
PCI_CLK_SMC	A8	P36/LCLK	
INT_SERIRQ	D7	P37/SERIRQ	
TP_SMC_XDP_TMS	A5	P40/TMI0	
SMC_SYS_LED_16B	B5	P41/TMO0	
SMBUS_SMC_BSB_SDA	D5	P42/SDA1	
SMC_TPM_PP	C3	P43/TMI1/EXSCKL	
TP_SMC_XDP_TRST_L	B1	P44/TMO1	
TP_SMC_XDP_TCK	C2	P45	
TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	
SMC_TX_L	G1	P50	
SMC_RX_L	G4	P51	
SMBUS_SMC_0_S0_SCL	F2	P52/SCL0	

P60/KIN0*	L13	SMC_PM_G2_EN	
P61/KIN1*	L14	SMC_ADAPTER_EN	
P62/KIN2*	L15	SPI_ARB	
P63/KIN3*	K12	SPI_SCLK	
P64/KIN4*	K13	SPI_SI	
P65/KIN5*	K14	SPI_SO	
P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3	
P67/IRQ7*/KIN7*	J13	FWH_INIT_L	
P70/AN0	N12	SMC_CPU_ISENSE	
P71/AN1	R13	SMC_CPU_VSENSE	
P72/AN2	P13	SMC_GPU_ISENSE	
P73/AN3	R14	SMC_GPU_VSENSE	
P74/AN4	P14	SMC_DCIN_ISENSE	
P75/AN5	R15	SMC_PBUS_VSENSE	
P76/AN6	N13	SMC_BATT_ISENSE	
P77/AN7	P15	SMC_FWIRE_ISENSE	
P80/PME*	C7	SMC_WAKE_SCI_L	
P81/GA20	A7	SMC_TPM_GPIO	
P82/CLKRUN*	B7	PM_CLKRUN_L	
P83/LPCPD*	D6	PM_SUS_STAT_L	
P84/IRQ3*/TXD1	C6	SC_TX_L	
P85/IRQ4*/RXD1	A6	SC_RX_L	
P86/IRQ5*/SCK1/SCL1	B6	SMBUS_SMC_BSB_SCL	
P90/IRQ2*	K4	SMC_ONOFF_L	
P91/IRQ1*	J2	SMC_BC_ACOK	
P92/IRQ0*	J1	SMC_BS_ALRT_L	
P93/IRQ12*	J3	PM_SLP_S3_L	
P94/IRQ13*	J4	PM_SLP_S4_L	
P95/IRQ14*	H2	PM_SLP_S5_L	
P96/EXCL	H1	SMC_CLK32K_SUSCLK	
P97/IRQ15*/SDA0	G2	SMBUS_SMC_0_S0_SDA	

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2PC	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	
SMC_EXTSMI_L	B10	PB0/LSMI*	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	
SMC_ODD_DETECT	D10	PB2	
ISENSE_CAL_EN	A11	PB3	
SMC_EXCARD_CP	B11	PB4	
SMC_EXCARD_PWR_EN	C11	PB5	
SMC_EXCARD_OC_L	A12	PB6	
SMC_XDP_TDO_3_3	D11	PB7	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	
TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	
TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	
TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	
TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	
SMS_X_AXIS	M11	PD0/AN8	
SMS_Y_AXIS	P11	PD1/AN9	
SMS_Z_AXIS	R11	PD2/AN10	
TP_SMC_ANALOG_ID	N11	PD3/AN11	
SMC_P1V05S0_ISENSE	P10	PD4/AN12	
SMC_P1V8S3_ISENSE	R10	PD5/AN13	
ALS_LEFT	N10	PD6/AN14	
ALS_RIGHT	M10	PD7/AN15	

PE0	M3	SMC_CASE_OPEN	
PE1*/ETCK	M2	SMC_TCK	
PE2*/ETDI	M1	SMC_TDI	
PE3*/ETDO	L4	SMC_TDO	
PE4*/ETMS	L2	SMC_TMS	
PF0/IRQ8*/PWM2	M7	TP_SMC_PF0	
PF1/IRQ9*/PWM3	P6	TP_SMC_PF1	
PF2/IRQ10*/TMOY	R6	SMC_LID	
PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L	
PF4/PWM4	M6	SMC_BATT_ISET	
PF5/PWM5	R5	TP_SMC_BATT_VSET	
PF6/PWM6	P5	SMC_SYS_ISET	
PF7/PWM7	N5	TP_SMC_SYS_VSET	
PG0/EXIRQ8*/TMIX	P9	SPI_CE_L	
PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3	
PG2/EXIRQ10*/SDA2	N9	SMBUS_SMC_BSA_SDA	
PG3/EXIRQ11*/SCL2	P8	SMBUS_SMC_BSA_SCL	
PG4/EXIRQ12*/EXSDAA	R8	SMBUS_SMC_A_S3_SDA	
PG5/EXIRQ13*/EXSCLA	M8	SMBUS_SMC_A_S3_SCL	
PG6/EXIRQ14*/EXSDAB	P7	SMBUS_SMC_B_S0_SDA	
PG7/EXIRQ15*/EXSCLB	R7	SMBUS_SMC_B_S0_SCL	
PH0/EXIRQ6*	E1	SMC_PROCHOT	
PH1/EXIRQ7*	F3	SMC_THRMTRIP	
PH2/FWE	K2	SMC_FWE	
PH3/EXEXCL	C4	ALS_GAIN	
PH4	D4	SMS_INT_L	
PH5	B3	SMS_ONOFF_L	

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

PP3V42_G3H
C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR RIN F1

SMC_VCL
C5807 0.47UF 20% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

VCL IS INTERNAL RAIL

PP3V42_G3H
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
PP3V42_G3H
R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

SMC_RST_L	E3	RES*	
SMC_XTAL	A2	XTAL	
SMC_EXTAL	B2	EXTAL	
MD1	E2		SMC_MD1
MD2	K1		KBC_MDE
NMI	F4		SMC_NMI
ETRST*	L1		SMC_TRST_L
AVSS	P12		
	R12		

R5898 10K 5% 1/16W MF-LF 402
R5803 10K 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402
NOSTUFF

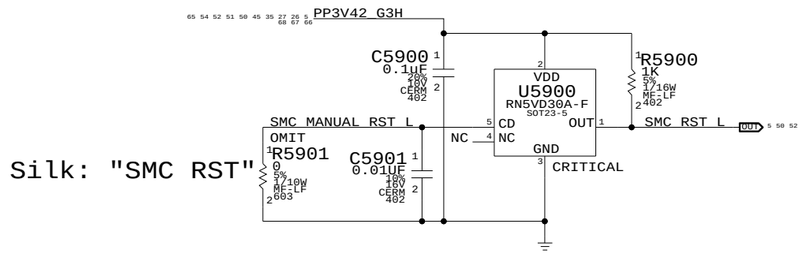
XW5800 SM
GND_SMC_AVSS

SMC

APPLE COMPUTER INC.

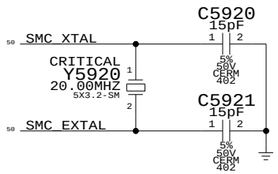
SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 50 OF 86	

SMC Reset Button / Brownout Detect

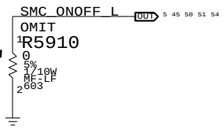


Silk: "SMC RST"

SMC Crystal Circuit

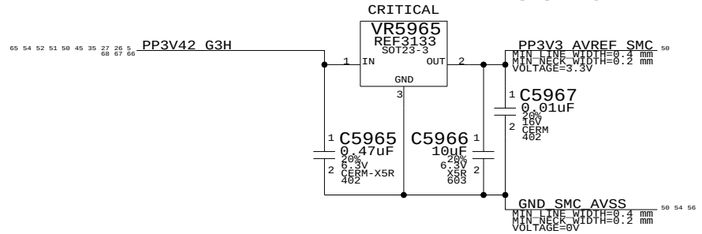


Debug Power Button

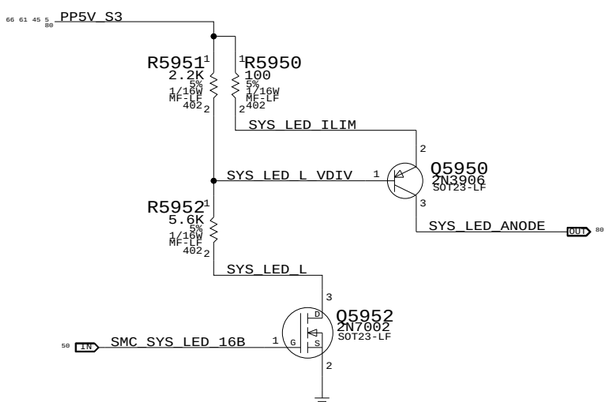


Silk: "PWR BTN"

SMC AVREF Supply



System (Sleep) LED Circuit



SMC Support

SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006

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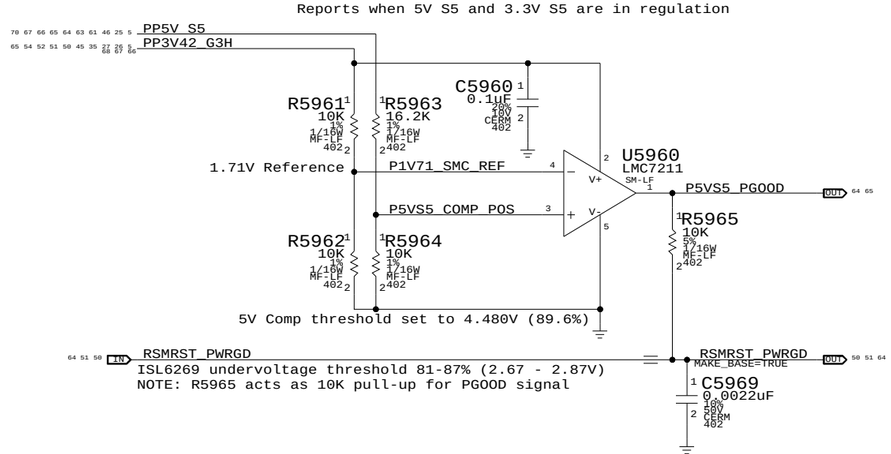
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

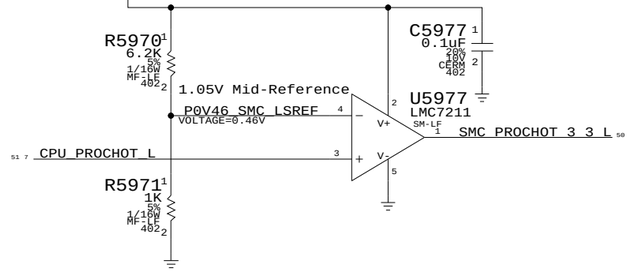
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
	SCALE: NONE	SHT 51 OF 86	

SMC PWRGD Circuit

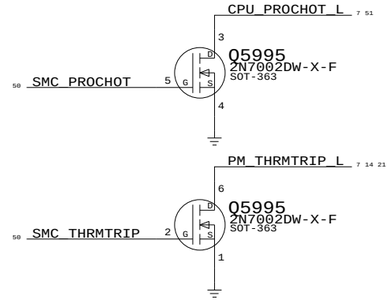
Reports when 5V S5 and 3.3V S5 are in regulation

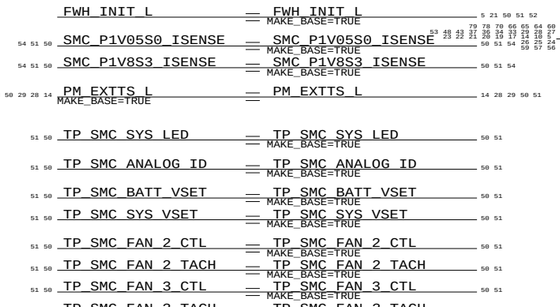


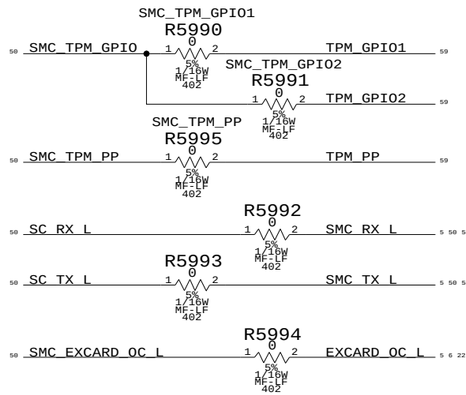
SMC 1.05V to 3.3V Level Shifting

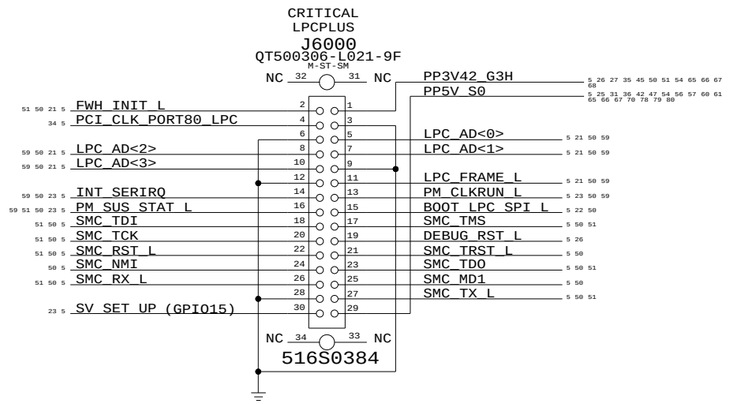


SMC 3.3V to 1.05V Level Shifting









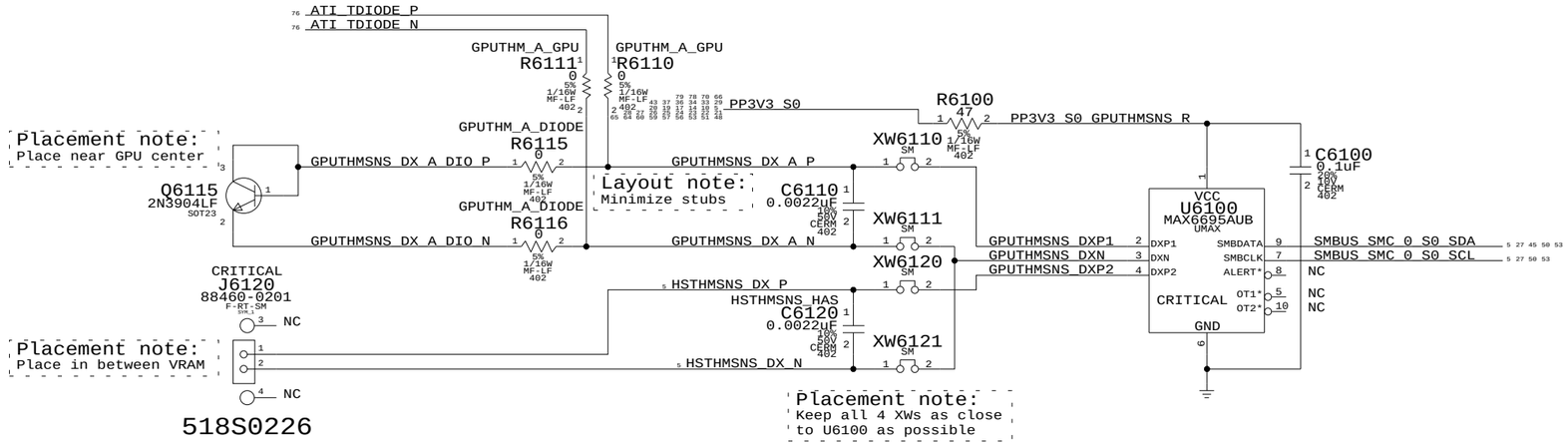
LPC+ Debug Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

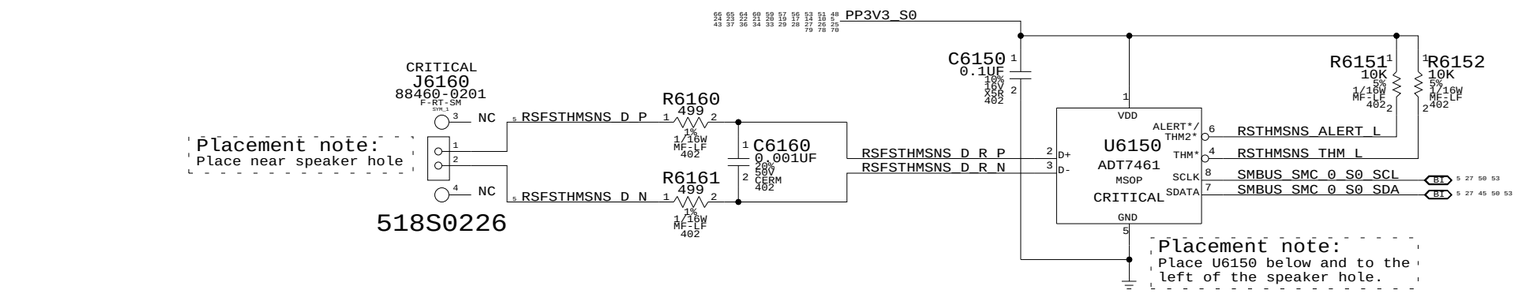
SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 52 OF 86	

GPU / Heat Pipe Thermal Sensor

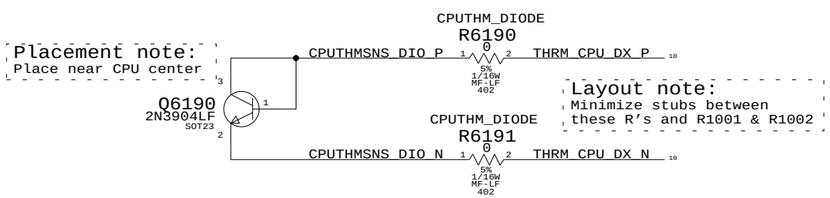


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

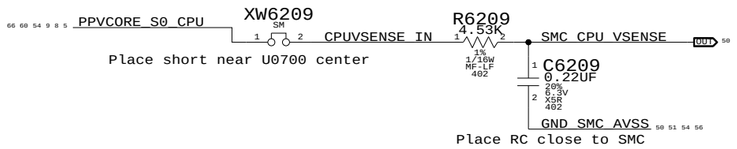
Thermal Sensors

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 53 OF 86	

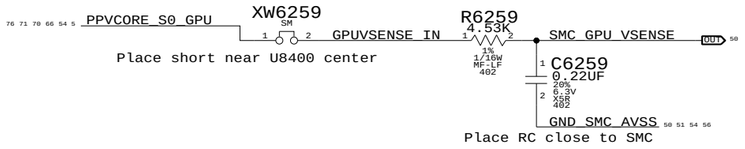
CPU Voltage Sense / Filter



Place short near U0700 center

Place RC close to SMC

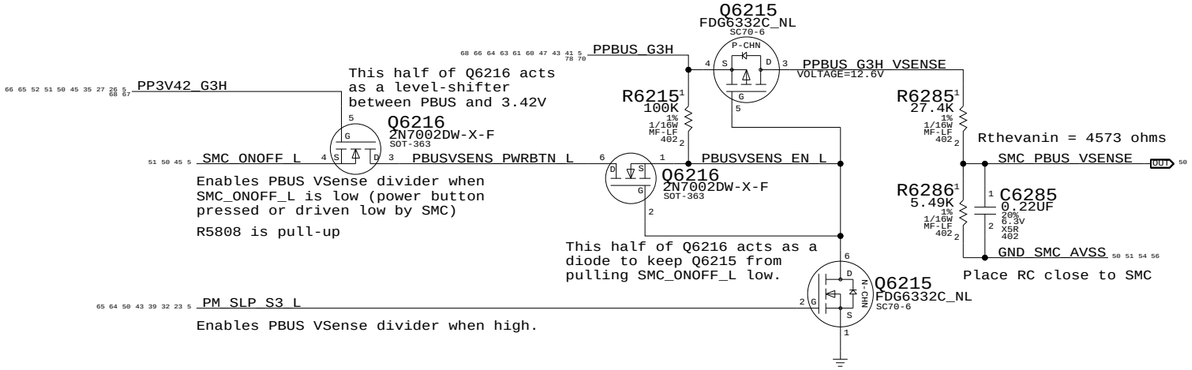
GPU Voltage Sense / Filter



Place short near U8400 center

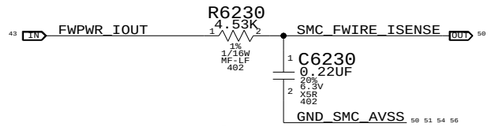
Place RC close to SMC

PBUS Voltage Sense Enable & Filter



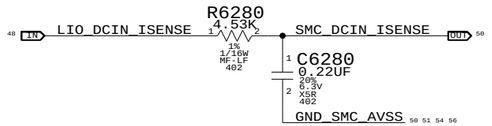
Place RC close to SMC

FireWire Current Sense Filter



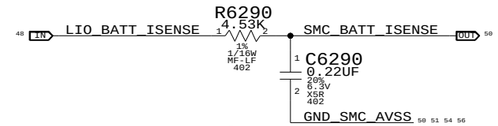
Place RC close to SMC

DCIN Current Sense Filter



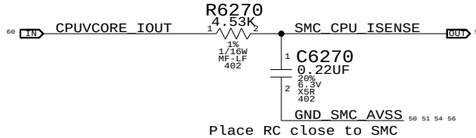
Place RC close to SMC

Battery Current Sense Filter



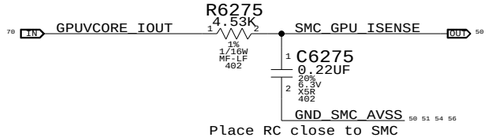
Place RC close to SMC

CPU Current Sense Filter



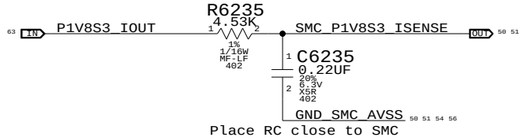
Place RC close to SMC

GPU Current Sense Filter



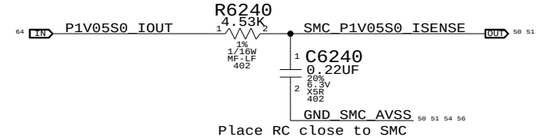
Place RC close to SMC

1.8V S3 (Memory) Current Sense Filter



Place RC close to SMC

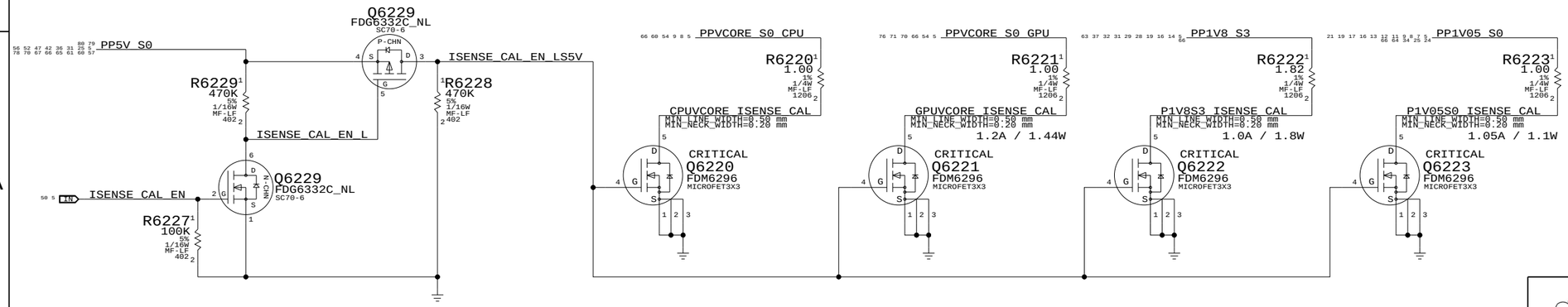
1.05V S0 (NB) Current Sense Filter



Place RC close to SMC

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing			
SYNC_MASTER=M1_MLB	SYNC_DATE=01/05/2006		
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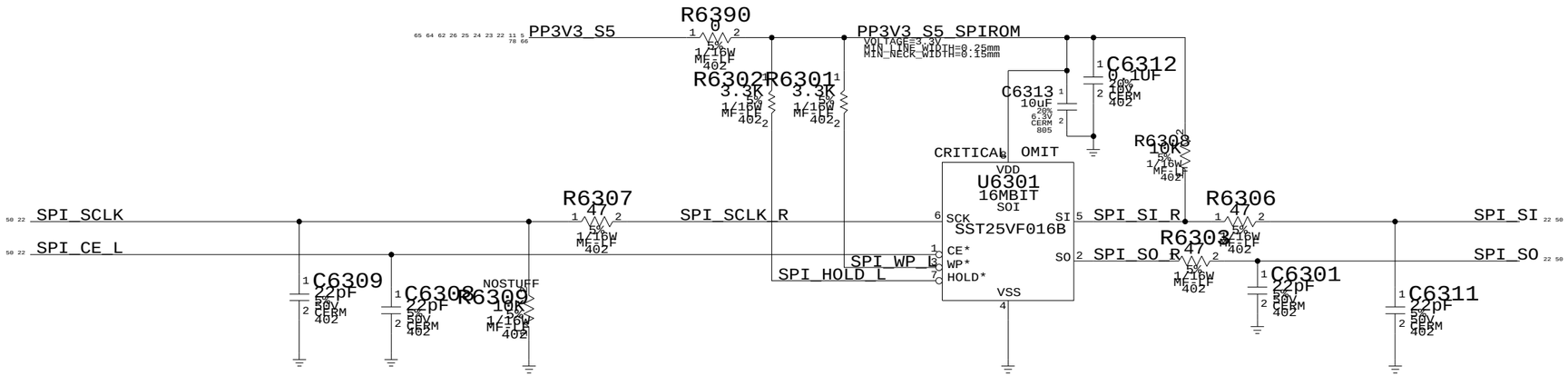
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7023	REV: B
	SCALE: NONE	SHT 54 OF 86	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

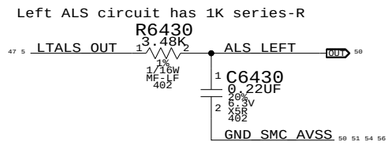
SYNC_MASTER=MS SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

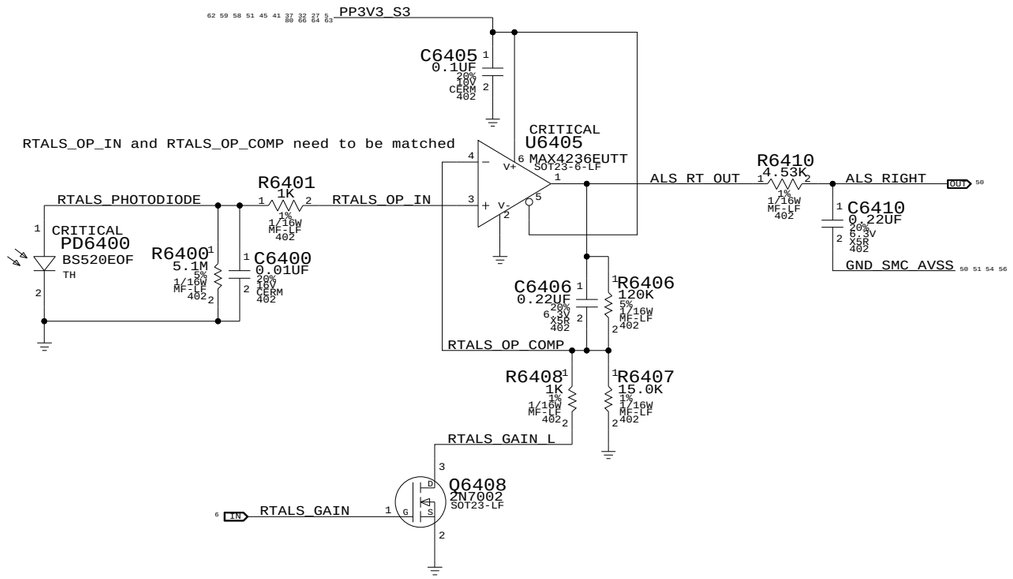
SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 55 OF 86	

Left ALS Filter

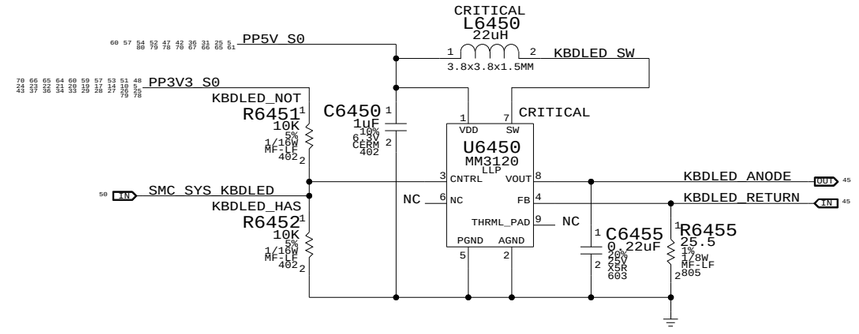
Left ALS circuit has 1K series-R



Right ALS Circuit



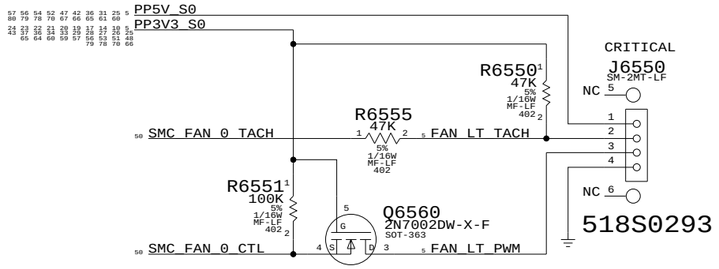
Keyboard LED Driver



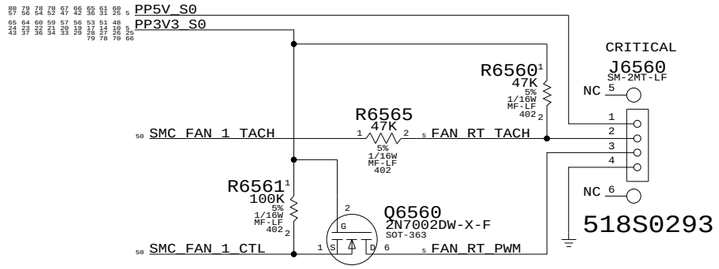
ALS Support			
SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006		

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
	SCALE: NONE	SHT 56 OF 86	

Left Fan



Right Fan



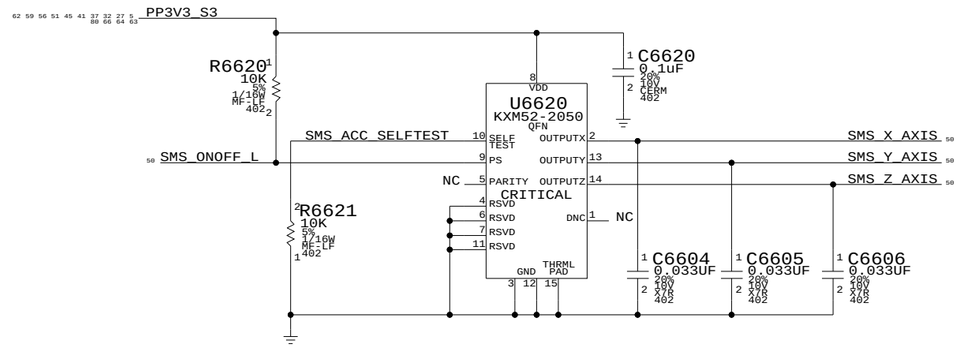
Fan Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

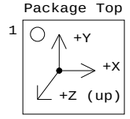
SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	57	86



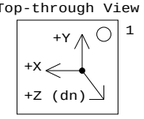
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

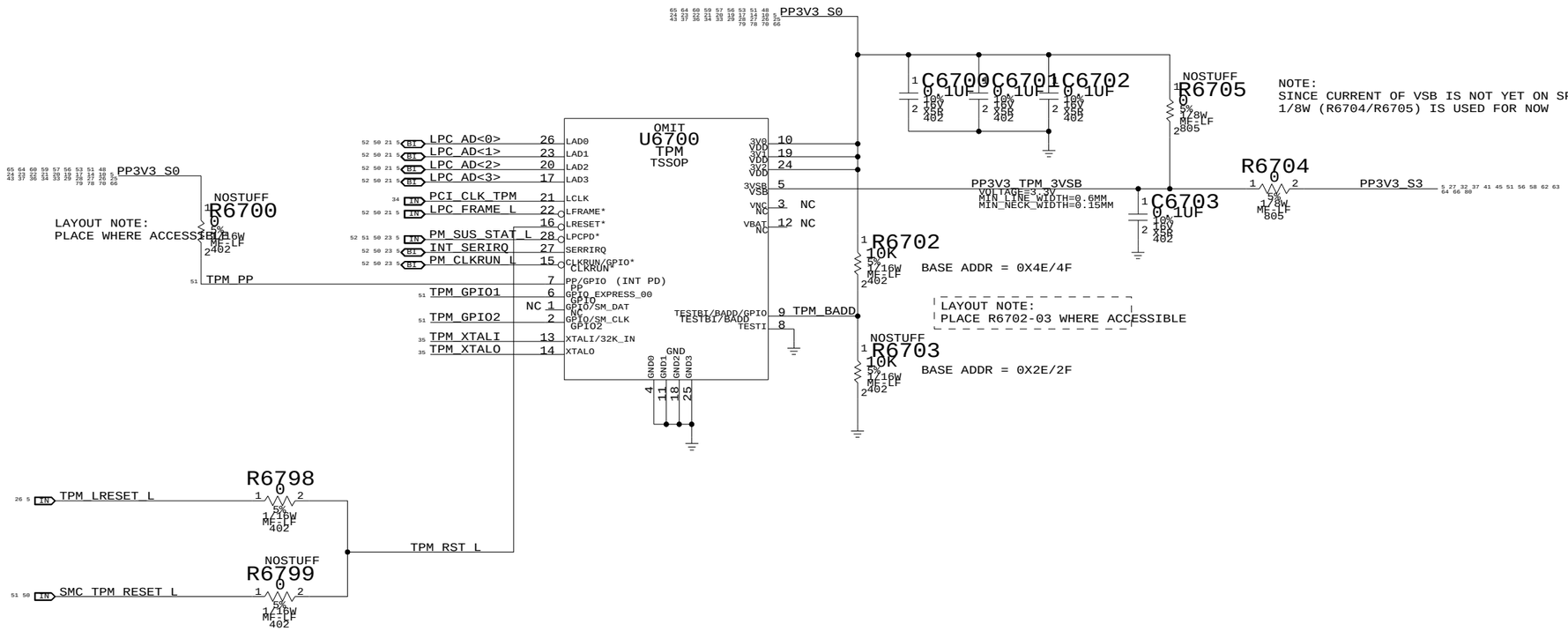
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE: NONE

SHT 58 OF 86



TPM

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	59	86

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

CPU VCore Current Sense

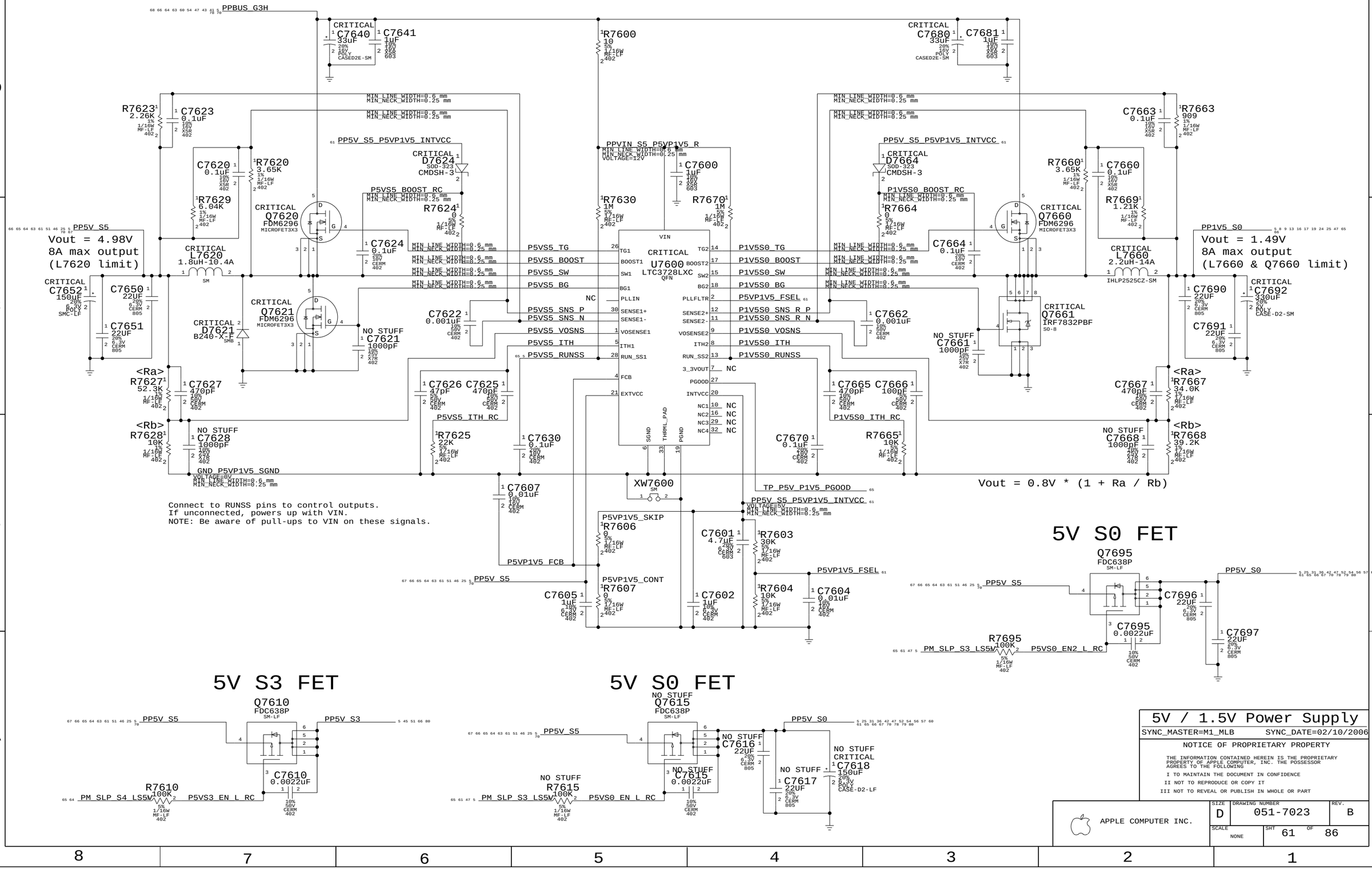
Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 60 OF 86	


PPBUS_G3H
CRITICAL C7640 33uF 20% 16V POLY CASED2E-SM
C7641 1uF 10% 16V X5R 603
R7600 10 5% 1/16W MF-LF 402
CRITICAL C7680 33uF 20% 16V POLY CASED2E-SM
C7681 1uF 10% 16V X5R 603
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
R7623 2.26K 1% 1/16W MF-LF 402
C7623 0.1uF 10% 16V X5R 402
PP5V_S5_P5VP1V5_INTVCC
CRITICAL D7624 SOD-323 CMDSH-3
C7620 0.1uF 10% 16V X5R 402
R7620 3.65K 1% 1/16W MF-LF 402
R7629 6.04K 1% 1/16W MF-LF 402
P5VS5_BOOST_RC
R7624 0 5% 1/16W MF-LF 402
PPVIN_S5_P5VP1V5_R
VOLTAGE=12V
C7600 1uF 10% 16V X5R 603
R7630 1M 5% 1/16W MF-LF 402
R7670 1M 5% 1/16W MF-LF 402
CRITICAL Q7620 FDM6296 MICROFET3X3
PP5V_S5
Vout = 4.98V
8A max output
(L7620 limit)
CRITICAL L7620 1.8uH-10.4A SM
C7624 0.1uF 20% 10V CERM 402
P5VS5_TG
P5VS5_BOOST
P5VS5_SW
P5VS5_BG
NC
P5VS5_SNS_P
P5VS5_SNS_N
P5VS5_VOSNS
P5VS5_ITH
P5VS5_RUNSS
VIN
CRITICAL U7600 LTC3728LXC QFN
TG1
BOOST1
SW1
BG1
PLLIN
SENSE1+
SENSE1-
VOSENSE1
ITH1
RUN_SS1
FCB
EXTVCC
TG2
BOOST2
SW2
BG2
PLLFLTR
SENSE2+
SENSE2-
VOSENSE2
ITH2
RUN_SS2
3_3VOUT
PGOOD
INTVCC
NC1
NC2
NC3
NC4
SGND
THRML_PAD
PGND
P1V5S0_TG
P1V5S0_BOOST
P1V5S0_SW
P1V5S0_BG
P5VP1V5_FSEL
P1V5S0_SNS_R_P
P1V5S0_SNS_R_N
P1V5S0_VOSNS
P1V5S0_ITH
P1V5S0_RUNSS
CRITICAL C7652 150uF 20% 6.3V POLY SMC-LF
C7650 22UF 20% 6.3V CERM 805
C7651 22UF 20% 6.3V CERM 805
CRITICAL D7621 B240-X-F SMB
CRITICAL Q7621 FDM6296 MICROFET3X3
NO_STUFF C7621 1000pF 10% 25V X7R 402
C7622 0.001uF 10% 16V CERM 402
C7662 0.001uF 10% 16V CERM 402
C7626 47pF 5% 50V CERM 402
C7625 470pF 10% 50V CERM 402
C7665 470pF 10% 50V CERM 402
C7666 100pF 5% 50V CERM 402
P5VS5_ITH_RC
P1V5S0_ITH_RC
R7625 22K 5% 1/16W MF-LF 402
C7630 0.1uF 20% 10V CERM 402
C7670 0.1uF 20% 10V CERM 402
R7665 10K 5% 1/16W MF-LF 402
<Ra>
R7627 52.3K 1% 1/16W MF-LF 402
C7627 470pF 10% 50V CERM 402
<Rb>
R7628 10K 1% 1/16W MF-LF 402
NO_STUFF C7628 1000pF 10% 25V X7R 402
GND_P5VP1V5_SGND
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
C7607 0.01uF 10% 16V CERM 402
XW7600 SM
TP_P5V_P1V5_PGOOD
PP5V_S5_P5VP1V5_INTVCC
VOLTAGE=5V
P5VP1V5_SKIP
R7606 0 5% 1/16W MF-LF 402
C7601 4.7uF 20% 6.3V CERM 603
R7603 30K 5% 1/16W MF-LF 402
P5VP1V5_FCB
P5VP1V5_CONT
R7607 0 5% 1/16W MF-LF 402
C7605 1uF 10% 6.3V CERM 402
C7602 1uF 10% 6.3V CERM 402
R7604 10K 5% 1/16W MF-LF 402
C7604 0.01uF 10% 16V CERM 402
P5VP1V5_FSEL
Connect to RUNSS pins to control outputs.
If unconnected, powers up with VIN.
NOTE: Be aware of pull-ups to VIN on these signals.
PP5V_S5_P5VP1V5_INTVCC
CRITICAL D7664 SOD-323 CMDSH-3
P1V5S0_BOOST_RC
R7664 0 5% 1/16W MF-LF 402
CRITICAL Q7660 FDM6296 MICROFET3X3
C7663 0.1uF 10% 16V X5R 402
R7663 909 1% 1/16W MF-LF 402
R7660 3.65K 1% 1/16W MF-LF 402
C7660 0.1uF 10% 16V X5R 402
R7669 1.21K 1% 1/16W MF-LF 402
C7664 0.1uF 20% 10V CERM 402
CRITICAL L7660 2.2uH-14A IHLP2525CZ-SM
PP1V5_S0
Vout = 1.49V
8A max output
(L7660 & Q7660 limit)
CRITICAL Q7661 IRF7832PBF SO-8
C7690 22UF 20% 6.3V CERM 805
CRITICAL C7692 330uF 20% 2V CASE-D2-SM
C7691 22UF 20% 6.3V CERM 805
NO_STUFF C7661 1000pF 10% 25V X7R 402
<Ra>
C7667 470pF 10% 50V CERM 402
R7667 34.0K 1% 1/16W MF-LF 402
<Rb>
NO_STUFF C7668 1000pF 10% 25V X7R 402
R7668 39.2K 1% 1/16W MF-LF 402
Vout = 0.8V * (1 + Ra / Rb)
5V S0 FET
Q7695 FDC638P SM-LF
PP5V_S5
PP5V_S0
C7696 22UF 20% 6.3V CERM 805
C7695 0.0022uF 10% 50V CERM 402
C7697 22UF 20% 6.3V CERM 805
R7695 100K 5% 1/16W MF-LF 402
PM_SLP_S3_LS5V
P5VS0_EN2_L_RC
5V S3 FET
Q7610 FDC638P SM-LF
PP5V_S5
PP5V_S3
C7610 0.0022uF 10% 50V CERM 402
R7610 100K 5% 1/16W MF-LF 402
PM_SLP_S4_LS5V
P5VS3_EN_L_RC
5V S0 FET
NO_STUFF
Q7615 FDC638P SM-LF
PP5V_S5
PP5V_S0
NO_STUFF C7616 22UF 20% 6.3V CERM 805
NO_STUFF CRITICAL C7618 150uF 20% 2V POLY CASE-D2-LF
NO_STUFF C7617 22UF 20% 6.3V CERM 805
NO_STUFF C7615 0.0022uF 10% 50V CERM 402
NO_STUFF R7615 100K 5% 1/16W MF-LF 402
PM_SLP_S3_LS5V
P5VS0_EN_L_RC
5V / 1.5V Power Supply
SYNC_MASTER=M1_MLB
SYNC_DATE=02/10/2006
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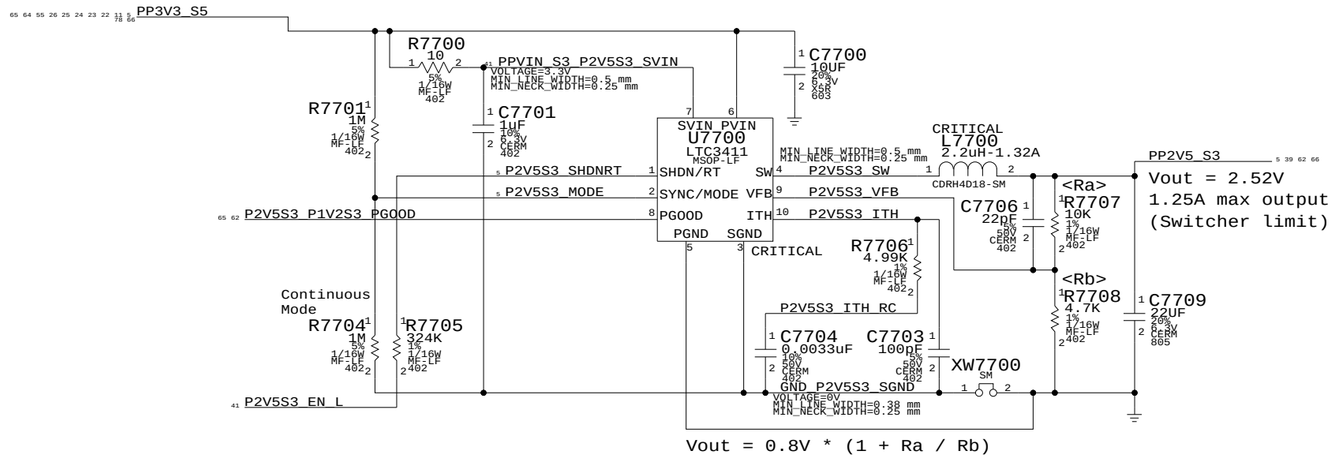
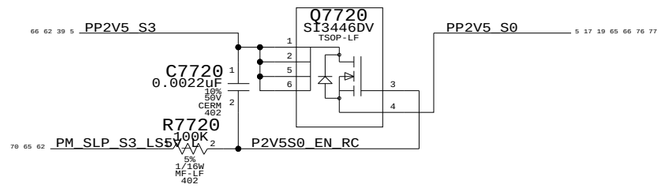
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7023
REV. B
SCALE NONE
SHT 61 OF 86

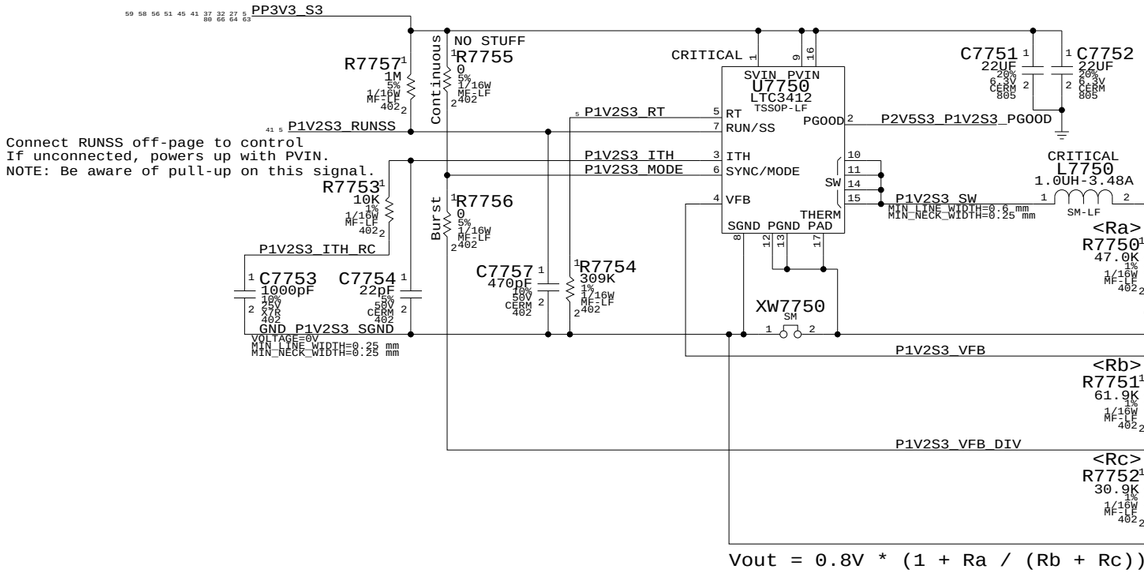
2.5V S3 Regulator



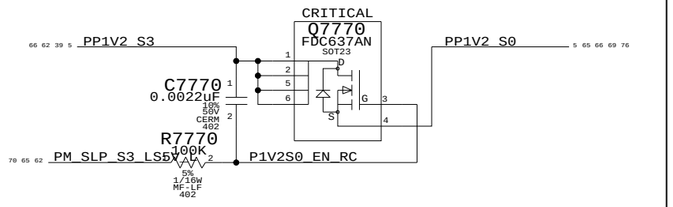
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



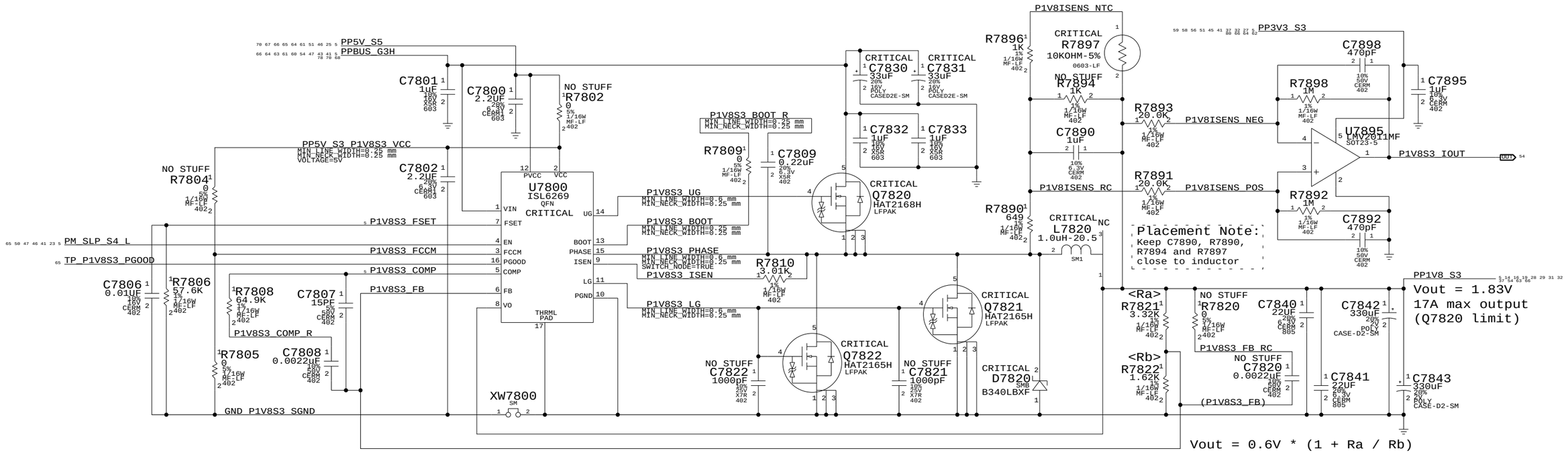
2.5V & 1.2V Regulators

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

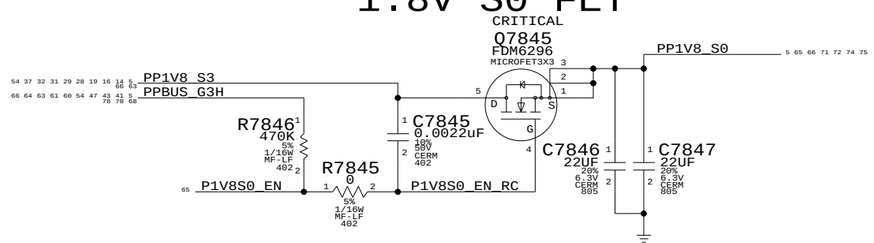
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 62 OF 86	

1.8V S3 Current Sense



1.8V S0 FET



1.8V Supply

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 63 OF 86	

3.3V S0 FET

Q7947
FDC638P
SM-LF

PP3V3_S5
PP3V3_S0
P3V3S0_EN_L
R7947 100K 5% 1/16W MF-LF 402
P3V3S0_EN_L_RC
C7947 0.0047uF 10% 25V CERM 402

3.3V S5 Regulator

PP5V_S5
PPBUS_G3H
C7901 1uF 10% 16V X5R 603
C7900 2.2uF 20% 6.3V CERM 603
NO STUFF R7902 0 5% 1/16W MF-LF 402

PP5V_S5_P3V3S5_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

NO STUFF R7904 0 5% 1/16W MF-LF 402
C7902 2.2uF 20% 6.3V CERM 603

R7949 0 5% 1/16W MF-LF 402
P5VS5_PGOOD
RSMRST_PWRGD

C7906 0.01UF 10% 16V CERM 402
R7906 57.6K 1% 1/16W MF-LF 402
R7908 51.1K 1% 1/16W MF-LF 402
C7907 470PF 10% 50V CERM 402
P3V3S5_COMP_R
R7905 0 5% 1/16W MF-LF 402
C7908 0.022UF 10% 16V CERM-X5R 402
NO STUFF C7949 0.01UF 20% 16V CERM 402

GND_P3V3S5_SGND

U7900
ISL6269
QFN
CRITICAL

1	VIN	UG	14
7	FSET	BOOT	13
4	EN	PHASE	15
3	FCCM	ISEN	9
16	PGOOD	LG	11
5	COMP	PGND	10
6	FB		
8	VO		
12	PVCC		
2	VCC		
17	THRML PAD		

P3V3S5_FSET
P3V3S5_EN_RC
P3V3S5_FCCM
P3V3S5_COMP
P3V3S5_FB

P3V3S5_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
P3V3S5_BOOT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
P3V3S5_PHASE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
P3V3S5_ISEN
P3V3S5_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

P3V3S5_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R7909 0 5% 1/16W MF-LF 402
C7909 0.22uF 20% 6.3V X5R 402

R7910 5.62K 1% 1/16W MF-LF 402

CRITICAL Q7920 FDM6296 MICROFET3X3
CRITICAL Q7921 FDM6296 MICROFET3X3
CRITICAL D7920 SMB MBRS140XXG

NO STUFF C7921 1000pF 10% 25V X7R 402

XW7900 SM

CRITICAL C7930 1uF 10% 16V X5R 603
CRITICAL C7931 33uF 20% 16V POLY CASED2E-SM

CRITICAL L7920 4.7uH IHLP

PP3V3_S5
Vout = 3.32V
4.5A max output
(L7920 limit)

<Ra> R7921 3.32K 1% 1/16W MF-LF 402
<Rb> R7922 732 1% 1/16W MF-LF 402
C7920 0.0047uF 10% 25V CERM 402
P3V3S5_FB_RC
R7920 0 5% 1/16W MF-LF 402
C7940 22UF 20% 6.3V CERM 805
C7941 22UF 20% 6.3V CERM 805
C7942 150UF 20% 6.3V POLY SMC-LF

Vout = 0.6V * (1 + Ra / Rb)

3.3V S3 FET

Q7945
FDC638P
SM-LF

PP3V3_S5
PP3V3_S3
PM_SLP_S4_LS5V
R7945 100K 5% 1/16W MF-LF 402
P3V3S3_EN_L_RC
C7945 0.0022uF 10% 50V CERM 402

1.05V Current Sense

P1V05ISENS_NTC
R7996 1K 1% 1/16W MF-LF 402
CRITICAL R7997 10KOHM-5% 0603-LF
NO STUFF R7994 1K 1% 1/16W MF-LF 402
C7990 1uF 10% 6.3V CERM 402

R7993 20.0K 1% 1/16W MF-LF 402
P1V05ISENS_NEG
R7991 20.0K 1% 1/16W MF-LF 402
P1V05ISENS_POS
P1V05ISENS_RC
R7990 649 1% 1/16W MF-LF 402

PP3V3_S0
C7998 470pF 10% 50V CERM 402
R7998 1M 1% 1/16W MF-LF 402
C7995 1uF 10% 6.3V CERM 402
U7995 LMV2011MF SOT23-5
P1V05S0_IOUT
R7992 1M 1% 1/16W MF-LF 402
C7992 470pF 10% 50V CERM 402

Placement Note:
Keep C7990, R7990, R7994 and R7997 close to inductor

CRITICAL L7970 1.53uH SM

1.05V S0 Regulator

PP5V_S5
PPBUS_G3H
C7951 1uF 10% 16V X5R 603
C7950 2.2UF 20% 6.3V CERM 603
NO STUFF R7952 0 5% 1/16W MF-LF 402
CRITICAL C7980 33uF 20% 2V POLY CASED2E-SM
C7981 1uF 10% 16V X5R 603

PP5V_S0_P1V05S0_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

NO STUFF R7954 0 5% 1/16W MF-LF 402
C7952 2.2UF 20% 6.3V CERM 603

P1V05S0_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R7959 0 5% 1/16W MF-LF 402
C7959 0.22uF 20% 6.3V X5R 402

U7950
ISL6269
QFN
CRITICAL

1	VIN	UG	14
7	FSET	BOOT	13
4	EN	PHASE	15
3	FCCM	ISEN	9
16	PGOOD	LG	11
5	COMP	PGND	10
6	FB		
8	VO		
12	PVCC		
2	VCC		
17	THRML PAD		

CRITICAL Q7970 FDM6296 MICROFET3X3

P1V05S0_FSET
PM_SLP_S3_L
P1V5P1V05S0_PGOOD
P1V05S0_FCCM
P1V05S0_COMP
P1V05S0_FB

P1V05S0_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
P1V05S0_BOOT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
P1V05S0_PHASE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
P1V05S0_ISEN
P1V05S0_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

R7960 2.8K 1% 1/16W MF-LF 402

CRITICAL Q7971 IRF7832PBF SO-8

NO STUFF C7971 1000pF 10% 25V X7R 402

C7956 0.01UF 10% 16V CERM 402
R7956 57.6K 1% 1/16W MF-LF 402
R7958 30.9K 1% 1/16W MF-LF 402
C7957 15PF 5% 50V CERM 402
P1V05S0_COMP_R
R7955 0 5% 1/16W MF-LF 402
C7958 0.01UF 10% 16V CERM 402

GND_P1V05S0_SGND

XW7950 SM

<Ra> R7971 3.32K 1% 1/16W MF-LF 402
<Rb> R7972 4.42K 1% 1/16W MF-LF 402
NO STUFF R7970 0 5% 1/16W MF-LF 402
P1V05S0_FB_RC
NO STUFF C7970 0.0022UF 10% 50V CERM 402
(P1V05S0_FB)

C7985 22UF 20% 6.3V CERM 805
C7986 22UF 20% 6.3V CERM 805
C7989 330UF 20% 2V POLY CASE-D2-SM

PP1V05_S0
Vout = 1.05V
10A max output
(Q7970 & L7970 limit)

Vout = 0.6V * (1 + Ra / Rb)

3.3V / 1.05V Power Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 64 OF 86	

Power Control Signals

PP5V_S5

R8050 10K 5% 1/10W MF-LF 402
R8051 10K 5% 1/10W MF-LF 402
R8052 10K 5% 1/10W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

PM_SLP_S3_LS5V_L (IN)

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE) → PM_SLP_S3_LS5V_L
P3V3S0_EN_L (MAKE_BASE=TRUE) → P3V3S0_EN_L
P1V8S0_EN (MAKE_BASE=TRUE) → P1V8S0_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363
Q8056 2N7002DW-X-F SOT-363
Q8050 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE) → PM_SLP_S3_LS5V

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363
R8054 100K 5% 1/10W MF-LF 402
Q8057 2N7002DW-X-F SOT-363

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

PM_SLP_S3_L (IN)

R8056 100K 5% 1/10W MF-LF 402

(PM_SLP_S3_L) (MAKE_BASE=TRUE) → PM_SLP_S3_L

R8053 10K 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD (IN)
P2V5S3_P1V2S3_PGOOD (IN)

NO STUFF
R8060 0 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD (MAKE_BASE=TRUE) → GPUVCORE_EN (MAKE_BASE=TRUE) → GPUVCORE_EN

Ensure 1.2V and 2.5V S3 supplies are up before enabling GPU VCore to support removing ethernet power in battery sleep.

PP5V_S5

R8055 10K 5% 1/10W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE) → PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L (IN)

R8057 100K 5% 1/10W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) (MAKE_BASE=TRUE) → PM_SLP_S4_L

PP3V42_G3H

P5VS5_PGOOD (IN)

(P5VS5_PGOOD) (MAKE_BASE=TRUE) → P5VS5_PGOOD

R8059 470K 5% 1/10W MF-LF 402

P5VS5_RUNSS

5V Enable has pull-up to PBUS

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN (IN)

R8058 100K 5% 1/10W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PPDCIN_G3H

C8000 10uF 10% 25V X5R 1206
C8001 10uF 10% 25V X5R 1206

U8000 LT3470 TSOT23-8
VIN, BOOST, SHDN*, SW, BIAS, NC, NC CRITICAL, FB, GND

P3V42G3H5_BOOST
C8005 0.22uF 20% 6.3V X5R 402
CRITICAL L8010 33uH CDPH4D19F-SM
P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

PP3V42_G3H
Vout = 3.425
200mA max output
(Switcher limit)

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402
<Rb> R8011 200K 1% 1/16W MF-LF 402

C8015 22UF 20% 6.3V CERM 805

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5
PP1V5_S0

R8061 27.4K 1% 1/10W MF-LF 402
R8063 4.99K 1% 1/16W MF-LF 402

0.89V Reference

U8060 LMC7211 SM-LF
P1V0_P1V5PG_REF
P1V5S0_COMP_POS
P1V5S0_PGOOD

C8060 0.1uF 10% 16V CERM 402

R8062 10K 1% 1/10W MF-LF 402
R8064 10K 1% 1/16W MF-LF 402

R8065 10K 5% 1/16W MF-LF 402

P1V5P1V05S0_PGOOD (OUT)

1.5V Comp threshold set to 1.32V (88%)

P1V5P1V05S0_PGOOD (IN)
P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE) → TP_P5V_P1V5_PGOOD
TP_P1V8S3_PGOOD (MAKE_BASE=TRUE) → TP_P1V8S3_PGOOD

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

PP5V_S0
PP3V3_S0
PP2V5_S0
PP1V8_S0
PP1V2_S0
PP0V9_S0

C8070 0.1uF 10% 16V CERM 402
C8071 0.1uF 10% 16V CERM 402

U8070 LTC2908 LLP
V1, V2, V3, V4 CRITICAL, VADJ1, VADJ2, RST*, GND, THRML PAD

R8074 68.1K 1% 1/10W MF-LF 402
R8072 124K 1% 1/16W MF-LF 402
R8075 100K 1% 1/10W MF-LF 402
R8073 100K 1% 1/16W MF-LF 402
R8076 549K 1% 1/16W MF-LF 402

S0PGOOD_1V2_DIV
S0PGOOD_0V9_DIV
S0PGOOD_PWROK

LTC2908 sources 6uA at 5.0V
R8076 serves as pull-down
and 3.3V level-shifter.

LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

PP3V3_S0

U8080 MC74VHC1G08 SC70
ALL_SYS_PWRGD (OUT)

C8080 0.1uF 10% 16V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7023 | REV. B

SCALE NONE | SHT 65 OF 86

"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PP0V9_S0
PP1V05_S0
PP1V2_S3
PP1V2_S0
PP1V5_S0
PP1V8_S3
PP1V8_S0
PP2V5_S3
PP2V5_S0
PPVCORE_S0_GPU
PPDCIN_G3H
GND

PP3V42_G3H
PP3V3_S5
PP3V3_S3
PP3V3_S0
PP3V3_S0_GPU

PP3V3_S3AC
PNBB_S0_GPU
PPBB_S0_GPU
PPVCORE_S0_CPU
PPBUS_G3H
PPBUS_S5_FW_FET
PP5V_S5
PP5V_S3
PP5V_S0

R8133
0
5%
1/8W
MF-LF
805
PLACEMENT_NOTE=Place on top-side of board

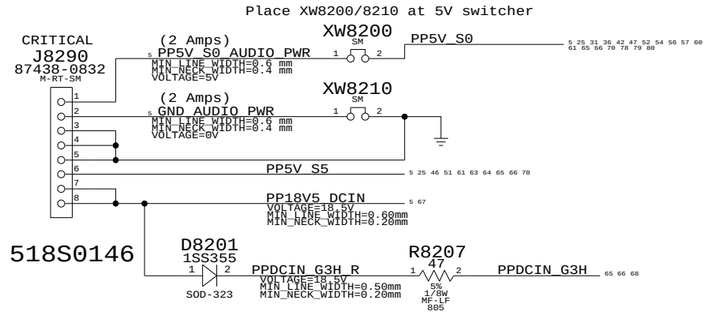
Power Aliases

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

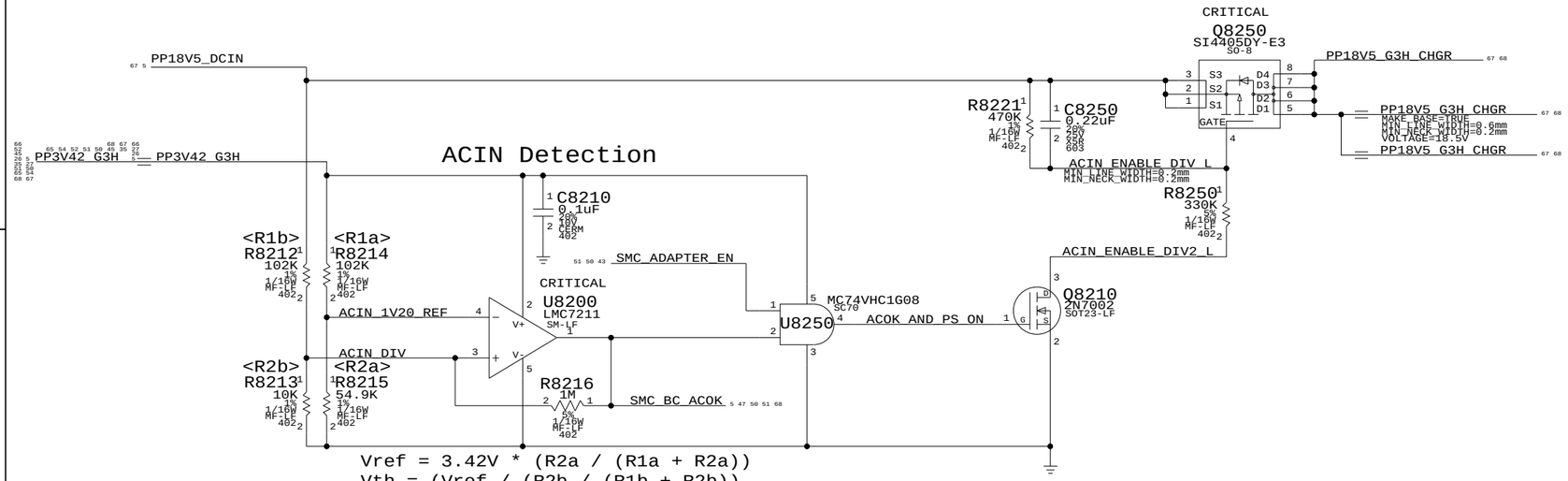
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 66 OF 86	

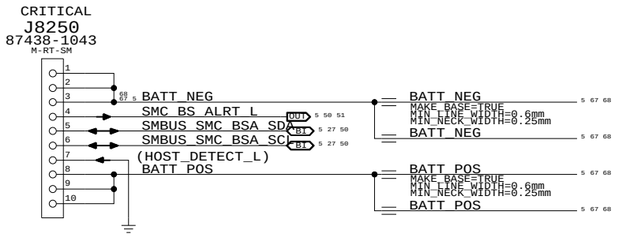
DC-In Connector



Inrush Limiter



Battery Connector



518S0391

DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 67 OF 86	

PBUS SUPPLY

BATTERY CHARGER

PP18V5_G3H_CHGR

CHGR_VDD

CHGR_SGND

CHGR_DCIN

CHGR_ACSET

CHGR_ACSET_D

CHGR_CSON_R

CHGR_DCSET

CHGR_ACLIM

CHGR_ICOMP

CHGR_VCOMP

CHGR_VADJ

CHGR_CSO_P

CHGR_CSO_N

CHGR_CHLIM

CHGR_VREF

CHGR_ACPRN

CHGR_ACSET

CHGR_SGATE

CHGR_CSI_P

CHGR_CSI_N

NC_CHGR_BGATE

NO_TEST=TRUE

CHGR_DCIN

CHGR_BOOT

CHGR_UGATE

CHGR_LGATE

CHGR_EN

CHGR_DCPRN

CHGR_DCSET

CHGR_PHASE

CHGR_VDDP

CHGR_CSIN_R

PPVDCIN_G3H_PRE

PPVDCIN_G3H_R

PPBUS_G3H

10A max, limited by L8300, Q8301

PPVBAT_G3H_CHGR_OUT

PPVBAT_G3H_PRE

PPVBAT_G3H_DIO

PPDCIN_G3H

PPVBAT_G3H_FET

PPVBAT_G3H_FUSE

BATT_POS

BATT_NEG

GND_BATT_CHGND

CHGR_CSON_R

CHGR_CSOP_R

CHGR_CSO_N

CHGR_CSO_P

CHG_EN_DIV_L

CHG_EN_DIV2_L

TCHG_EN_DIV_L

TCHG_EN_DIV2_L

SMC_SYS_ISET

SMC_BATT_ISET

SMC_BC_ACOK

SMC_BC_ACOK_R

SMC_BATT_CHG_EN

SMC_BATT_TRICKLE_EN_L

PP3V42_G3H

CHGR_VADJ

CHGR_EN

CHGR_ACPRN

CHGR_DCPRN

CHGR_CHLIM

CHGR_VREF

CHGR_SGND

Using PWM drive

As shown, Ichg = 3.9A max

If stuffed, R8364+R8365 > 70K so Iref < 100uA

MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm

MIN_LINE_WIDTH=0.2mm MIN_NECK_WIDTH=0.2mm

MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.2mm

MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm

SWITCH_NODE=TRUE

VOLTAGE=17.6V

Pbus Supply & Batt. Charger

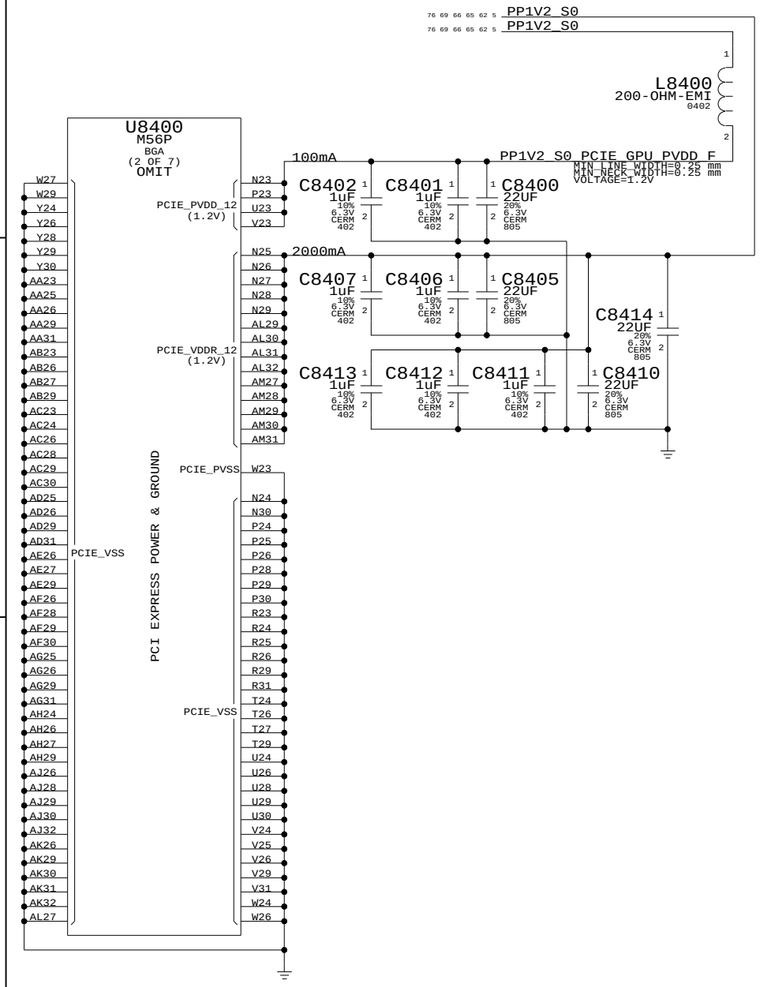
SYNC_MASTER=M1_LIO

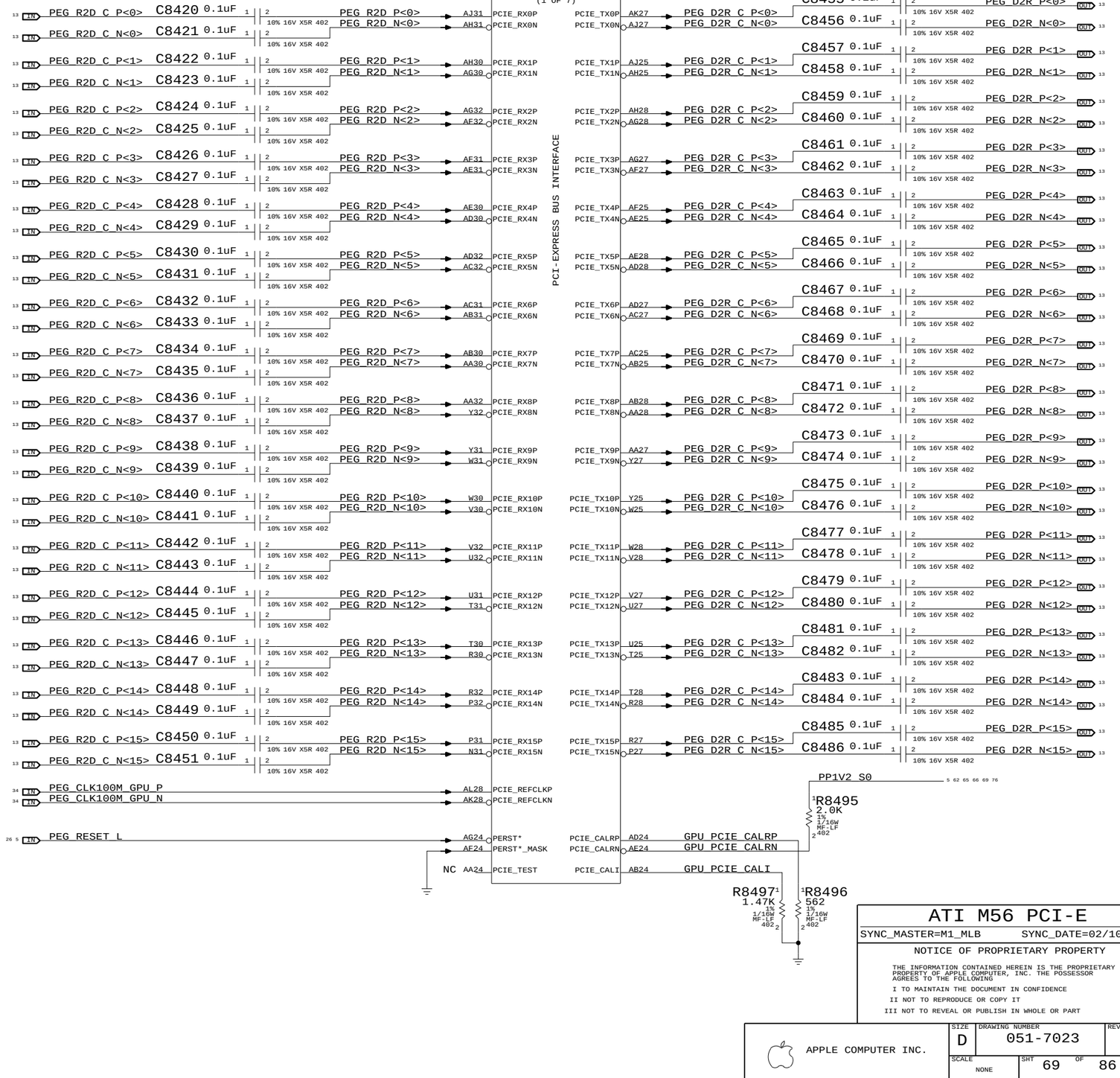
SYNC_DATE=12/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	68	86





ATI M56 PCI-E

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 69 OF 86	

GPU VCore Supply

PP5V_S5
PPBUS_G3H
C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM1 603
NO STUFF R8502 0 5% 1/16W MF-LF 402
PP5V_S0_GPUVCORE_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C8502 2.2UF 20% 6.3V CERM1 603
R8504 0 1% 1/16W MF-LF 402
GPUVCORE_EN
PM_SLP_S3_LS5V_L
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB
R8508 150K 1% 1/16W MF-LF 402
C8507 15pF 5% 50V CERM 402
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
GPUVCORE_COMP_R
NO STUFF R8505 0 5% 1/16W MF-LF 402
C8508 470pF 10% 50V CERM 402
GND_GPUVCORE_SGND
XW8500 SM
U8500 ISL6269 QFN
CRITICAL
PVCC VCC
VIN FSET EN FCCM PGOOD COMP FB VO
UG BOOT PHASE ISEN LG PGND
THRML PAD
GPUVCORE_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
GPUVCORE_BOOT
GPUVCORE_PHASE
SWITCH_NODE=TRUE
GPUVCORE_ISEN
GPUVCORE_LG
GPUVCORE_BOOT_R
R8509 0 5% 1/16W MF-LF 402
C8509 0.22UF 20% 6.3V X5R 402
C8530 1uF 10% 16V X5R 603
C8531 33uF 20% 16V POLY CASED2E-SM
C8532 1uF 10% 16V X5R 603
CRITICAL Q8520 HAT2168H LFPAK
R8510 3.01K 1% 1/16W MF-LF 402
CRITICAL Q8522 HAT2165H LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
NO STUFF C8521 1000pF 10% 25V X7R 402
CRITICAL Q8521 HAT2165H LFPAK
CRITICAL D8520 SMB B340LBXF
GPUISENS_NTC
R8596 1K 1% 1/16W MF-LF 402
CRITICAL R8597 10KOHM-5% 0603-LF
NO STUFF R8594 1K 1% 1/16W MF-LF 402
C8590 1uF 10% 6.3V CERM 402
GPUISENS_RC
R8590 649 1% 1/16W MF-LF 402
CRITICAL_NC L8520 1.0uH-20.5 SM1
R8593 20.0K 1% 1/16W MF-LF 402
GPUISENS_NEG
R8591 20.0K 1% 1/16W MF-LF 402
GPUISENS_POS
PP3V3_S0
C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
U8595 LMV2011MF SOT23-5
GPUVCORE_IOUT
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402
Placement Note:
Keep C8590, R8590, R8594 and R8597 close to inductor
PPVCORE_S0_GPU
Vout = 1.10V / 0.95V
17A max output
(Q8520 limit)
<Ra> R8521 3.01K 1% 1/16W MF-LF 402
<Rb> R8522 5.11K 1% 1/16W MF-LF 402
NO STUFF R8520 0 5% 1/16W MF-LF 402
GPUVCORE_FB_RC
C8540 22UF 20% 6.3V CERM 805
C8542 330uF 20% 2V POLY CASE-D2-SM
NO STUFF C8520 0.0022UF 10% 16V CERM 402
C8541 22UF 20% 6.3V CERM 805
C8543 330uF 20% 2V POLY CASE-D2-SM
(GPUVCORE_FB)
<Rc> R8523 12.4K 1% 1/16W MF-LF 402
GPUVCORE_FB_LOW

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

PP3V3_S0_GPU
R8526 10K 5% 1/16W MF-LF 402
R8525 10K 5% 1/16W MF-LF 402
GPU_VCORE_HIGH
GPU_VCORE_HIGH_RC
Q8523 2N7002DW-X-F SOT-363
C8523 0.022uF 10% 16V CERM-X5R 402
GPU_VCORE_LOW
Q8523 2N7002DW-X-F SOT-363
R8524 10K 5% 1/16W MF-LF 402

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

PPVCORE_S0_GPU
Q8575 SI3446DV TSOP-LF
GPUBB_EN_L
CRITICAL U8550 FAN2558 SOT23-6-LF
PP3V3_S0_GPU
VIN PG EN GND VOUT ADJ
GPUBB_EN
C8551 2.2uF 20% 6.3V CERM1 603
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22UF 20% 6.3V CERM 805
PPBB_S0_GPU
Vout = (1.58V /) 1.50V
180mA max output
(LDO limit)
GPUBBP_ADJ
NO STUFF R8554 174K 1% 1/16W MF-LF 402
<Rb> R8556 16.2K 1% 1/16W MF-LF 402
<Rc>
C8557 22UF 20% 6.3V CERM 805
GPUBBP_ADJ_LOW
NO STUFF Q8554 2N7002 SOT23-LF
GPU_VCORE_HIGH

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

PP5V_S0
R8570 100K 5% 1/16W MF-LF 402
GPUBB_EN_L
Q8570 2N7002 SOT23-LF
C8570 0.0022uF 10% 16V CERM 402
GPU_BB_CTL
R8561 0 5% 1/16W MF-LF 402
GPU_GENERICD
GPUBB_EN
R8560 10K 5% 1/16W MF-LF 402

For proper M56 power sequence, this pull-up must be powered before VCore

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.

PP3V3_S0_GPU
C8580 10UF 20% 6.3V X5R 603
GPUBB_EN
U8580 MAX1673 SOI
CRITICAL
SHDN_L IN CAP+ CAP- LIN/SKIP_L GND FB OUT
GPUBBN_CAPP
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
C8581 2.2uF 20% 6.3V CERM1 603
GPUBBN_CAPN
<Ra> R8587 68.1K 1% 1/16W MF-LF 402
GPUBBN_FB
<Rb> R8588 11.3K 1% 1/16W MF-LF 402
C8589 22UF 20% 6.3V CERM 805
PNBB_S0_GPU
Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA
Vout = -0.55V
125mA max output
(Regulator limit)

GPU (M56) Core Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

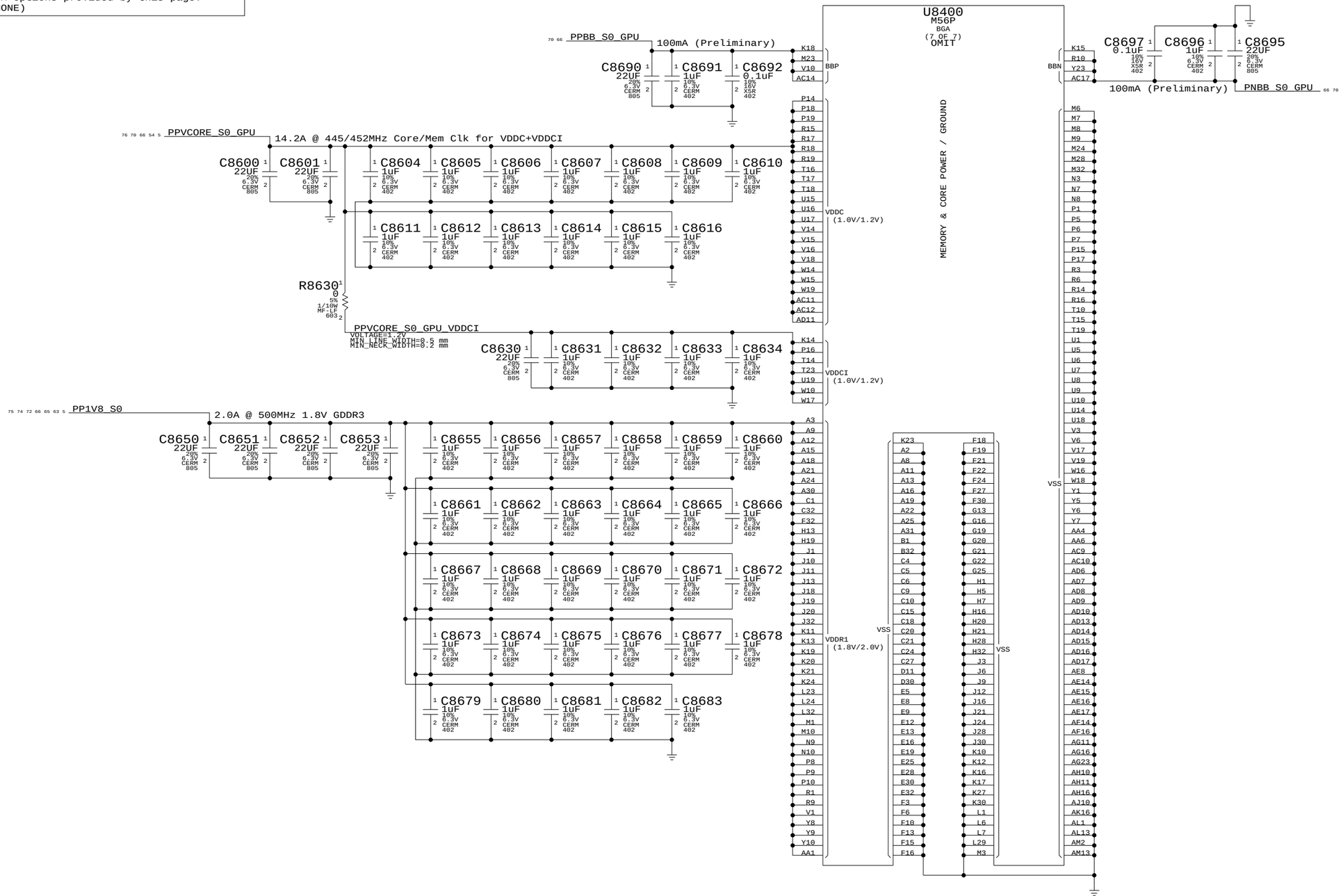
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7023
REV. B
SCALE NONE
SHT 70 OF 86

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

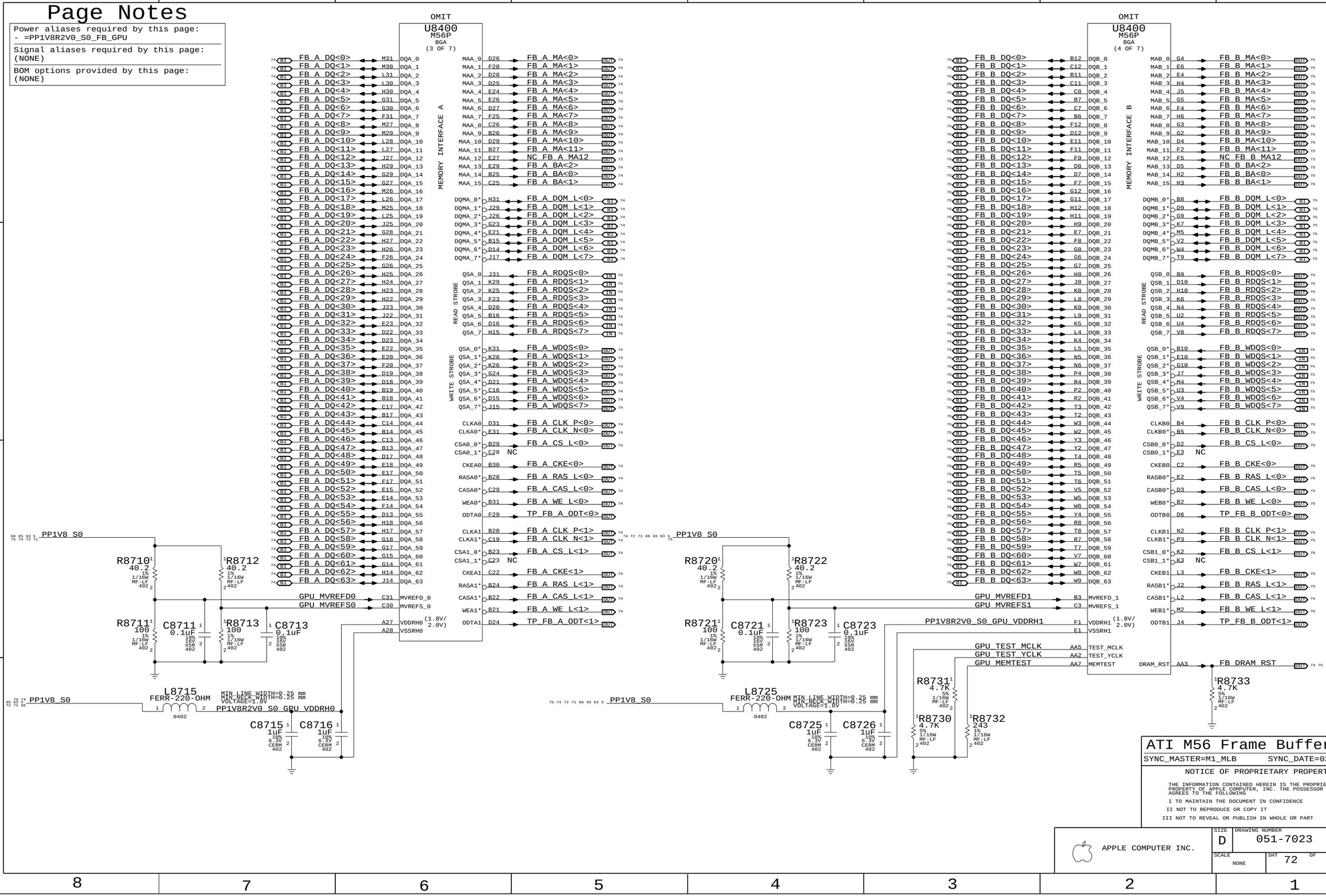
SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 71 OF 86	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 72 OF 86	

GPU Straps

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 73 OF 86	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CRITICAL
OMIT

U8900
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8950
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

PP1V8_S0

Connect to designated pin, then GND

L8910 FERR-220-OHM
L8915 FERR-220-OHM
L8960 FERR-220-OHM
L8965 FERR-220-OHM

PP1V8_S0_FB_A0_VDDA0
PP1V8_S0_FB_A0_VDDA1
PP1V8_S0_FB_A1_VDDA0
PP1V8_S0_FB_A1_VDDA1

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

C8900 C8901 C8902 C8903 C8904 C8910 C8915
C8920 C8921 C8922 C8923 C8924 C8925 C8926
C8931 C8933
C8950 C8951 C8952 C8953 C8954 C8960 C8965
C8970 C8971 C8972 C8973 C8974 C8975 C8976
C8981 C8983

22UF 20% 6.3V CERM 805
0.1uF 10% 16V X5R 402

R8930 R8932 R8931 R8933
R8980 R8982 R8981 R8983
2.37K 1% 1/16W MF-LF 402
5.49K 1% 1/16W MF-LF 402

FB_A0_VREF0
FB_A0_VREF1
FB_A1_VREF0
FB_A1_VREF1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R8940 R8942 R8944 R8946 R8947
R8990 R8992 R8994 R8996 R8997
121 1% 1/16W MF-LF 402
60.4 1% 1/16W MF-LF 402
1K 5% 1/16W MF-LF 402

R8941 R8943 R8945
R8991 R8993 R8995
121 1% 1/16W MF-LF 402
60.4 1% 1/16W MF-LF 402

R8948 R8949 R8998 R8999
243 1% 1/16W MF-LF 402
100 5% 1/16W MF-LF 402

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

FB_A_MA<0>
FB_A_MA<1>
FB_A_MA<2>
FB_A_MA<3>
FB_A_MA<4>
FB_A_MA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE<0>
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS_L<0>
FB_A_WE_L<0>
FB_A_CAS_L<0>
FB_A_RAS_L<0>
FB_A_CKE<1>
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_CS_L<1>
FB_A_WE_L<1>
FB_A_CAS_L<1>
FB_A_RAS_L<1>
FB_DRAM_RST
FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>
FB_A_RDQS<4>
FB_A_RDQS<5>
FB_A_RDQS<6>
FB_A_RDQS<7>
FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>
FB_A_WDQS<4>
FB_A_WDQS<5>
FB_A_WDQS<6>
FB_A_WDQS<7>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>
FB_A_DQM_L<0>
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>
FB_A_DQM_L<4>
FB_A_DQM_L<5>
FB_A_DQM_L<6>
FB_A_DQM_L<7>
FB_A_DQ<0>
FB_A_DQ<1>
FB_A_DQ<2>
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FB_A_DQ<56>
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FB_A_DQ<58>
FB_A_DQ<4>
FB_A_DQ<5>
FB_A_DQ<6>
FB_A_DQ<7>

FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN

NC
NC

GDDR3 Frame Buffer A

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

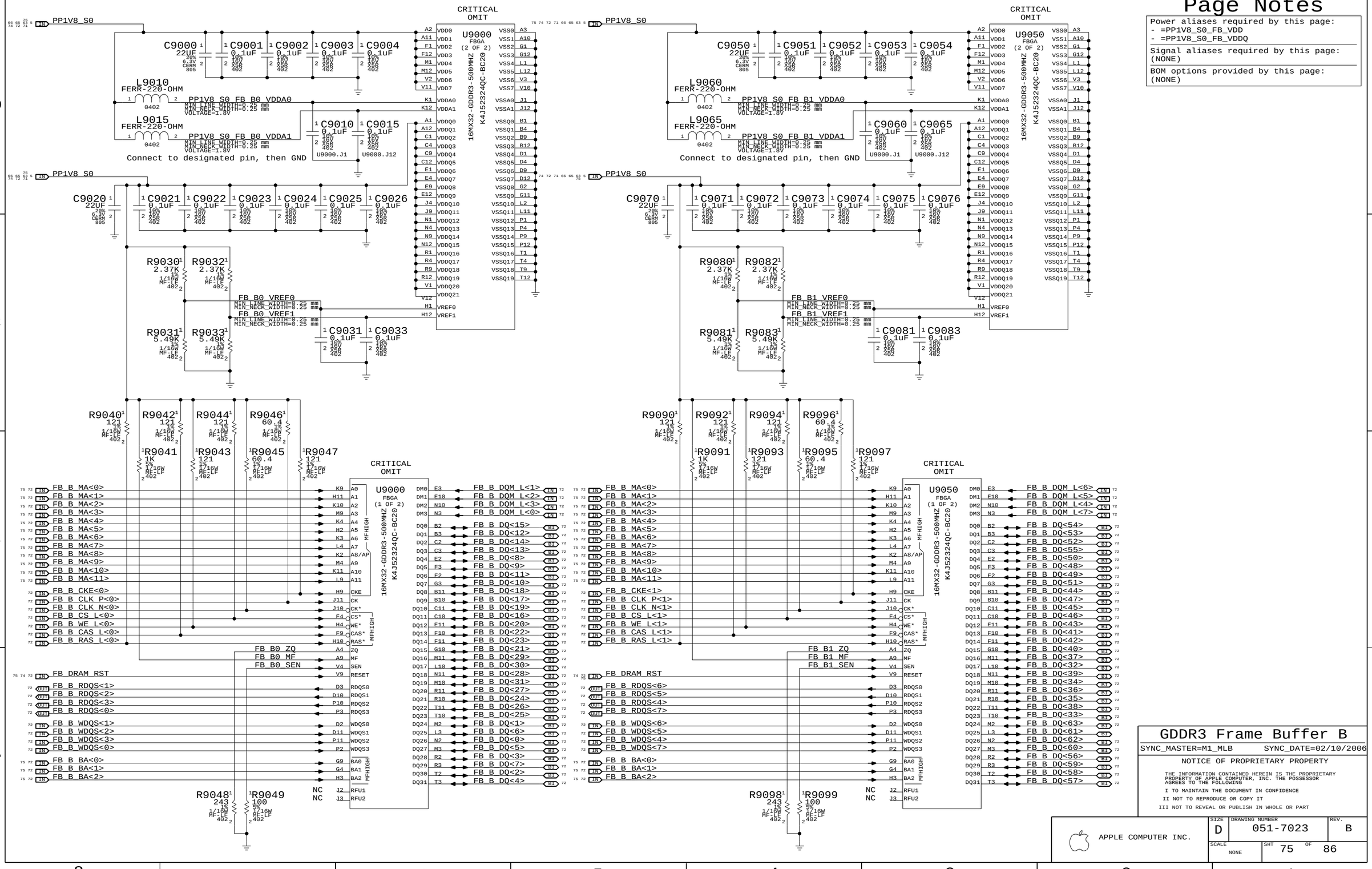
SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 74 OF 86	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

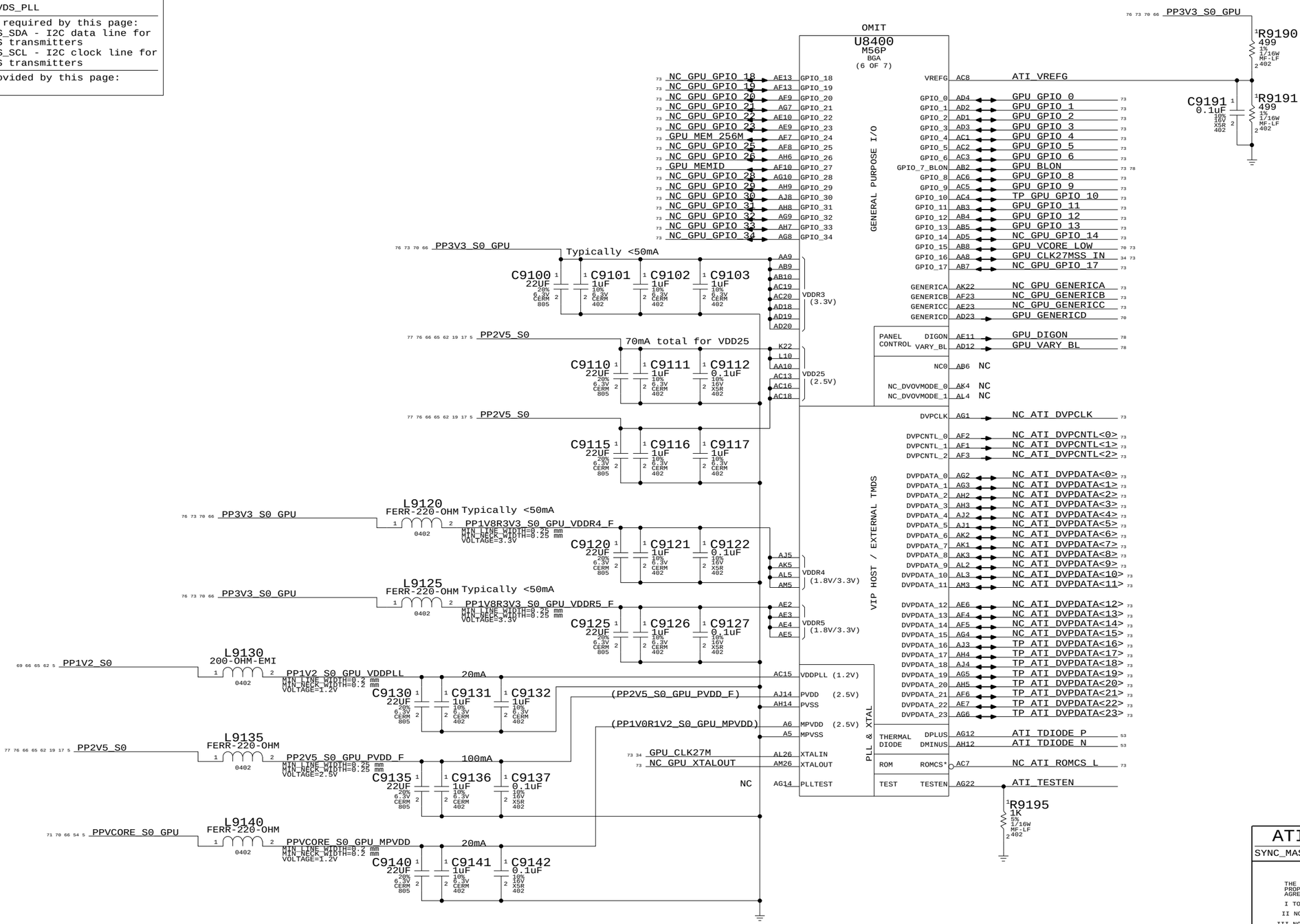
SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 75 OF 86	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006

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ATI M56 GPIO/DVO/Misc

APPLE COMPUTER INC.

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Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP2V5_S0
Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9300 22UF 20% 6.3V CERM 805; C9301 1UF 10% 6.3V CERM 402; C9302 1UF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
C9305 22UF 20% 6.3V CERM 805; C9306 1UF 10% 6.3V CERM 402; C9307 0.1UF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
C9310 22UF 20% 6.3V CERM 805; C9311 1UF 10% 6.3V CERM 402; C9312 0.1UF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22UF 20% 6.3V CERM 805; C9316 1UF 10% 6.3V CERM 402; C9317 0.1UF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
C9320 22UF 20% 6.3V CERM 805; C9321 1UF 10% 6.3V CERM 402; C9322 0.1UF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9325 22UF 20% 6.3V CERM 805; C9326 1UF 10% 6.3V CERM 402; C9327 0.1UF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9330 22UF 20% 6.3V CERM 805; C9331 1UF 10% 6.3V CERM 402; C9332 1UF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
C9340 22UF 20% 6.3V CERM 805; C9345 22UF 20% 6.3V CERM 805; C9341 1UF 10% 6.3V CERM 402; C9342 0.1UF 10% 16V X5R 402; C9346 0.1UF 10% 16V X5R 402; C9347 0.1UF 10% 16V X5R 402

OMIT
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR

DAC (CRT)
- AL25, AM25 AVDD (2.5V)
- AJ24, AK25 AVSS
- AK23 AVSSQ
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI
- 77 ATI RSET → AL22 RSET

DAC2 (TV/CRT2)
- AL16, AM16 A2VDD (2.5V)
- AL17, AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- 77 ATI R2SET → AK14 R2SET

LVDS
- AE19 LPVDD (2.5V)
- AE18 LPVSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20 LVDDR (2.5V)
- AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- 79 I/N GPU_HPD → AF11 HPD1

TMDS outputs:
- TXCP AM9 → TMDS_CLK_P (OUT) 78 79 86
- TXCM AL9 → TMDS_CLK_N (OUT) 78 79 86
- TX0P AL10 → TMDS_DATA0_P (OUT) 79
- TX0M AK10 → TMDS_DATA0_N (OUT) 79
- TX1P AM11 → TMDS_DATA1_P (OUT) 79
- TX1M AL11 → TMDS_DATA1_N (OUT) 79
- TX2P AM12 → TMDS_DATA2_P (OUT) 79
- TX2M AL12 → TMDS_DATA2_N (OUT) 79
- TX3P AJ9 → TMDS_DATA3_P (OUT) 79
- TX3M AK9 → TMDS_DATA3_N (OUT) 79
- TX4P AJ11 → TMDS_DATA4_P (OUT) 79
- TX4M AK11 → TMDS_DATA4_N (OUT) 79
- TX5P AJ12 → TMDS_DATA5_P (OUT) 79
- TX5M AK12 → TMDS_DATA5_N (OUT) 79

DAC (CRT) outputs:
- R AK24 → NC_GPU_VGA_R (OUT) 73
- G AM24 → NC_GPU_VGA_G (OUT) 73
- B AL24 → NC_GPU_VGA_B (OUT) 73
- HSYNC AJ23 → TP_GPU_VGA_HSYNC (OUT) 73
- VSYNC AJ22 → TP_GPU_VGA_VSYNC (OUT) 73

DAC2 (TV/CRT2) outputs:
- R2 AK15 → GPU_R2 (OUT) 78 79
- G2 AM15 → GPU_G2 (OUT) 78 79
- B2 AL15 → GPU_B2 (OUT) 78 79
- H2SYNC AF15 → GPU_H2SYNC (OUT) 79
- V2SYNC AG15 → GPU_V2SYNC (OUT) 79
- Y AJ15 → NC_GPU_TV_Y (OUT) 73
- C AJ13 → NC_GPU_TV_C (OUT) 73
- COMP AH15 → NC_GPU_TV_COMP (OUT) 73

LVDS outputs:
- TXCLK_UP AJ21 → LVDS_U_CLK_P (OUT) 78 81
- TXCLK_UN AK21 → LVDS_U_CLK_N (OUT) 78 81
- TXOUT_U0P AG18 → LVDS_U_DATA_P<0> (OUT) 78 81
- TXOUT_U0N AH18 → LVDS_U_DATA_N<0> (OUT) 78 81
- TXOUT_U1P AK20 → LVDS_U_DATA_P<1> (OUT) 78 81
- TXOUT_U1N AJ20 → LVDS_U_DATA_N<1> (OUT) 78 81
- TXOUT_U2P AG20 → LVDS_U_DATA_P<2> (OUT) 78 81
- TXOUT_U2N AH20 → LVDS_U_DATA_N<2> (OUT) 78 81
- TXOUT_U3P AH21 → NC_LVDS_U_DATAP<3> (OUT) 73
- TXOUT_U3N AG21 → NC_LVDS_U_DATAN<3> (OUT) 73
- TXCLK_LP AM18 → LVDS_L_CLK_P (OUT) 78 81
- TXCLK_LN AL18 → LVDS_L_CLK_N (OUT) 78 81
- TXOUT_L0P AL19 → LVDS_L_DATA_P<0> (OUT) 78 81
- TXOUT_L0N AK19 → LVDS_L_DATA_N<0> (OUT) 78 81
- TXOUT_L1P AM20 → LVDS_L_DATA_P<1> (OUT) 78 81
- TXOUT_L1N AL20 → LVDS_L_DATA_N<1> (OUT) 78 81
- TXOUT_L2P AM21 → LVDS_L_DATA_P<2> (OUT) 78 81
- TXOUT_L2N AL21 → LVDS_L_DATA_N<2> (OUT) 78 81
- TXOUT_L3P AJ18 → NC_LVDS_L_DATAP<3> (OUT) 73
- TXOUT_L3N AK18 → NC_LVDS_L_DATAN<3> (OUT) 73

DDC outputs:
- DDC1CLK AH23 ↔ GPU_DDC_A_CLK (BI) 79
- DDC1DATA AH22 ↔ GPU_DDC_A_DATA (BI) 79
- DDC2CLK AG13 ↔ GPU_DDC_B_CLK (BI) 73
- DDC2DATA AH13 ↔ GPU_DDC_B_DATA (BI) 73
- DDC3CLK AF12 ↔ GPU_DDC_C_CLK (BI) 78
- DDC3DATA AE12 ↔ GPU_DDC_C_DATA (BI) 78

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI_RSET 77
ATI_R2SET 77
R9350 499 1% 1/16W MF-LF 402
R9351 715 1% 1/16W MF-LF 402

ATI M56 Video Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

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D	051-7023	B
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LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_R2
	VGA	VGA	GPU_G2
	VGA	VGA	GPU_B2
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>

PP3V3_S5
R9400 100K 5% 1/16W MF-LF 402
C9400 0.0022uF 10% 50V CERM 402
R9401 100K 5% 1/16W MF-LF 402
LCD_PWREN_L_RC
LCD_PWREN_L
Q9401 2N7002DW-X-F SOT-363
GPU_DIGON
R9494 100K 5% 1/16W MF-LF 402
Q9400 SI3443DV TSOP-LF
PP3V3_LCD_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
L9400 FERR-250-OHM SM
C9401 0.001uF 20% 50V CERM 402
GND_CHASSIS_LVDS
PP3V3_S0
R9410 100K 5% 1/16W MF-LF 402
R9411 100K 5% 1/16W MF-LF 402
100K pull-ups are for no-panel case (development)
Panel has 2K pull-ups
GPU_DDC_C_CLK
GPU_DDC_C_DATA
C9410 0.001uF 20% 50V CERM 402
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
C9420 0.001uF 20% 50V CERM 402
CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM
PP3V3_LCD_CONN MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
NC
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_CLK_N
LVDS_L_CLK_P
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_P<2>
LVDS_U_CLK_N
LVDS_U_CLK_P
C9421 0.001uF 20% 50V CERM 402
518S0289
GND_CHASSIS_LVDS

INVERTER INTERFACE

PPBUS_G3H
L9450 FERR-1K-OHM-EMI SM
PPBUS_S0_INVERTER MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.8V
C9450 0.001uF 20% 50V CERM 402
PP5V_S0
Q9450 FDG6332C_NL SC70-6
R9450 100K 5% 1/16W MF-LF 402
PP5V_INVERTER_SW_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
L9452 400-OHM-EMI SM-1
C9451 10UF 20% 6.3V X5R 603
CRITICAL
J9450 SM-2MT-LF
NC
FP_PWR_EN_L
Q9450 FDG6332C_NL SC70-6
GPU_BLON
R9489 10K 5% 1/16W MF-LF 402
PP5V_INVERTER_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
C9452 0.001uF 20% 50V CERM 402
518S0293
L9454 400-OHM-EMI SM-1
INVERTER_PWM
GND_INVERTER MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
C9454 0.001uF 20% 50V CERM 402
C9455 0.001uF 20% 50V CERM 402
L9455 60-OHM-EMI SM
GND_CHASSIS_INVERTER
PP3V3_S0
INVERTER_BUF
U9453 MC74VHC1G08 SC70
GPU_VARY_BL
INVERTER_PWM_F
INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL
INVERTER_BUF
C9453 0.1uF 20% 25V CERM 402
INVERTER_UNBUF
R9496 0 5% 1/16W MF-LF 402

Internal Display Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=01/09/2006

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TMDS Filtering

Place series R's and differential termination close to GPU, common mode chokes near connector.

TMDS_DATA0_N → R9761 0 → TMDS_DATA0_R_N → L9700 90-OHM-300mA 2012H → TMDS_DATA0_F_N
TMDS_DATA0_P → R9760 182 → TMDS_DATA0_R_P → R9762 0 → TMDS_DATA0_F_P
TMDS_D0_L: OMIT L9760 47nH 0402 (VOLTAGE=0V, NO_TEST=TRUE)

TMDS_DATA1_N → R9765 0 → TMDS_DATA1_R_N → L9701 90-OHM-300mA 2012H → TMDS_DATA1_F_N
TMDS_DATA1_P → R9764 182 → TMDS_DATA1_R_P → R9766 0 → TMDS_DATA1_F_P
TMDS_D1_L: OMIT L9764 47nH 0402 (VOLTAGE=0V, NO_TEST=TRUE)

TMDS_DATA2_N → R9769 0 → TMDS_DATA2_R_N → L9702 90-OHM-300mA 2012H → TMDS_DATA2_F_N
TMDS_DATA2_P → R9768 182 → TMDS_DATA2_R_P → R9770 0 → TMDS_DATA2_F_P
TMDS_D2_L: OMIT L9768 47nH 0402 (VOLTAGE=0V, NO_TEST=TRUE)

TMDS_CLK_N → R9772 0 → TMDS_CLK_R_N → L9706 370-OHM SM 2012H → TMDS_CLK_F_N
TMDS_CLK_P → R9771 182 → TMDS_CLK_R_P → R9773 0 → TMDS_CLK_F_P
C9772 10pF 50V CERM 402 (TMDS_CLK_R_N)
C9773 10pF 50V CERM 402 (TMDS_CLK_R_P)

TMDS_DATA3_N → R9777 0 → TMDS_DATA3_R_N → L9703 90-OHM-300mA 2012H → TMDS_DATA3_F_N
TMDS_DATA3_P → R9776 182 → TMDS_DATA3_R_P → R9778 0 → TMDS_DATA3_F_P
TMDS_D3_L: OMIT L9776 47nH 0402 (VOLTAGE=0V, NO_TEST=TRUE)

TMDS_DATA4_N → R9781 0 → TMDS_DATA4_R_N → L9704 90-OHM-300mA 2012H → TMDS_DATA4_F_N
TMDS_DATA4_P → R9780 182 → TMDS_DATA4_R_P → R9782 0 → TMDS_DATA4_F_P
TMDS_D4_L: OMIT L9780 47nH 0402 (VOLTAGE=0V, NO_TEST=TRUE)

TMDS_DATA5_N → R9785 0 → TMDS_DATA5_R_N → L9705 90-OHM-300mA 2012H → TMDS_DATA5_F_N
TMDS_DATA5_P → R9784 182 → TMDS_DATA5_R_P → R9786 0 → TMDS_DATA5_F_P
TMDS_D5_L: OMIT L9784 47nH 0402 (VOLTAGE=0V, NO_TEST=TRUE)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0419	6	IND,47NH,2%,1.3OHM,0402,LF	L9760,L9764,L9768,L9776,L9780,L9784	CRITICAL	TMDS_PEAKING_IND
116S0004	6	RES,0OHM,5%,0402,LF	L9760,L9764,L9768,L9776,L9780,L9784		TMDS_NO_PEAKING_IND

VGA SYNC BUFFERS

PP3V3_S0 → U9750 MC74VHC1G08 SC70 (GPU_V2SYNC → VGA_VSYNC_R) → R9750 33 → VGA_VSYNC
C9750 0.1uF 20% 10V CERM 402

PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

PP3V3_S0 → U9751 MC74VHC1G08 SC70 (GPU_H2SYNC → VGA_HSYNC_R) → R9751 33 → VGA_HSYNC
C9751 0.1uF 20% 10V CERM 402

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_B2 (DAC2 Comp) → R9740 75 1% 1/10W MF-LF 402 → CRITICAL FL9740 LCFILTER SM-220MHZ-LF → VGA_B
C9740 3.3pF 0.25pF 50V CERM 402

GPU_G2 (DAC2 Y) → R9741 75 1% 1/10W MF-LF 402 → CRITICAL FL9741 LCFILTER SM-220MHZ-LF → VGA_G
C9741 3.3pF 0.25pF 50V CERM 402

GPU_R2 (DAC2 C) → R9742 75 1% 1/10W MF-LF 402 → CRITICAL FL9742 LCFILTER SM-220MHZ-LF → VGA_R
C9742 3.3pF 0.25pF 50V CERM 402

DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

PP5V_S0 → CRITICAL F9710 0.5AMP-13.2V SM-LF → PP5V_S0_DDC_F (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)
PP5V_S0_DDC_F → L9710 400-OHM-EMI SM-1 → PP5V_S0_DDC (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

Isolation required for DVI power switch

CRITICAL J9700 QH11121-RIG02-4F F-RT-TH-DVI

Pin	Signal
33	GND_CHASSIS_DVI_BOT
17	TMDS_DATA0_F_N
18	TMDS_DATA0_F_P
19	
20	TMDS_DATA5_F_N
21	TMDS_DATA5_F_P
22	
23	TMDS_CLK_F_P
24	TMDS_CLK_F_N
C3	VGA_B
C5B	
C4	VGA_HSYNC
34	GND_CHASSIS_DVI_TOP
1	TMDS_DATA2_F_N
9	TMDS_DATA1_F_N
2	TMDS_DATA2_F_P
10	TMDS_DATA1_F_P
3	
11	
4	TMDS_DATA4_F_N
12	TMDS_DATA3_F_N
5	TMDS_DATA4_F_P
13	TMDS_DATA3_F_P
6	DVI_DDC_CLK_R
14	(PP5V_S0_DDC)
7	DVI_DDC_DATA_R
15	
8	VGA_VSYNC
16	DVI_HPD_R
C1	VGA_R
C5A	
C2	VGA_G
32	

514-0278

R9731 0 5% 1/10W MF-LF 402 → GND_CHASSIS_DVI_TOP
PLACE NEAR 3, 11 & 19

PLACE NEAR C5A & C5B
R9730 0 5% 1/10W MF-LF 402 → GND_CHASSIS_DVI_BOT, GND

C9710 0.01uF 20% 50V CERM 603

3V LEVEL SHIFTERS

PP5V_S0_DDC_PULLUPS (VOLTAGE=5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm)
D9710 SOD-123 B0530WXF
R9710 4.7K 5% 1/16W MF-LF 402
R9712 4.7K 5% 1/16W MF-LF 402

PP3V3_S0 → R9720 10K 5% 1/16W MF-LF 402 → Q9711 2N7002DW-X-F SOT-363 (DVI_DDC_CLK → GPU_DDC_A_CLK)
R9711 100 5% 1/10W MF-LF 402
C9711 100pF 5% 50V CERM 402

PP3V3_S0 → R9721 10K 5% 1/16W MF-LF 402 → Q9711 2N7002DW-X-F SOT-363 (DVI_DDC_DATA → GPU_DDC_A_DATA)
R9713 100 5% 1/10W MF-LF 402
C9713 100pF 5% 50V CERM 402

PP3V3_S0 → R9722 100K 5% 1/16W MF-LF 402 → Q9714 2N7002DW-X-F SOT-363 (DVI_HPD → GPU_HPD)
R9714 100 5% 1/10W MF-LF 402
R9715 20K 5% 1/16W MF-LF 402
C9714 100pF 5% 50V CERM 402

External Display Connector

SYNC_MASTER=M1_MLB SYNC_DATE=11/18/2005

APPLE COMPUTER INC.

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D	051-7023	B
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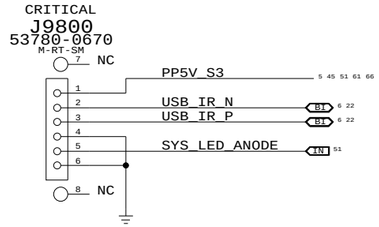
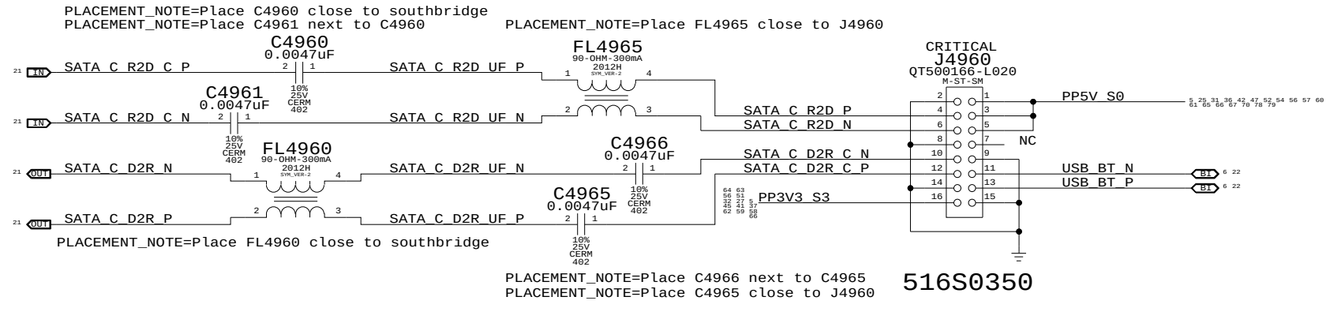
IR & Sleep LED Connector



518S0388

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M9 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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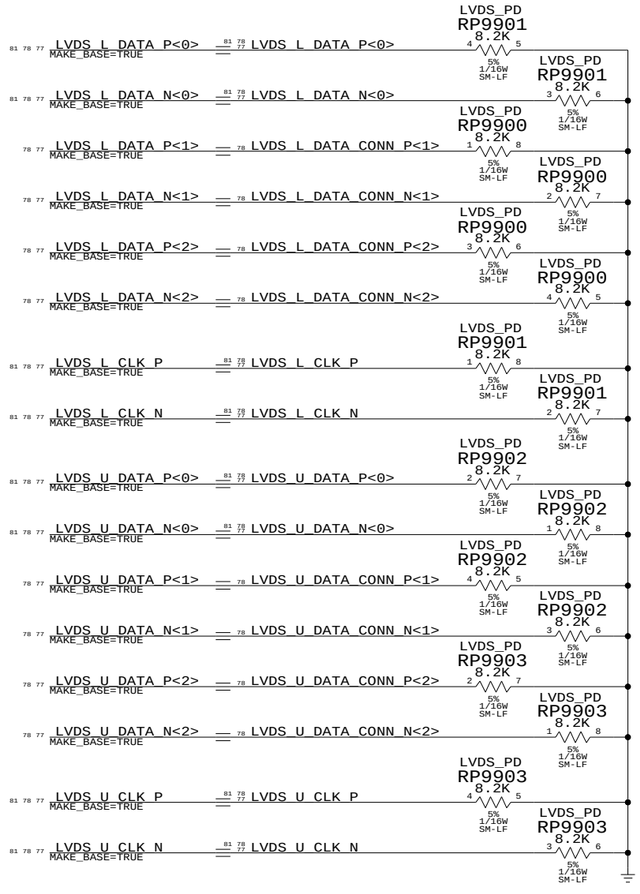
D	051-7023	B
SCALE: NONE	SHT 80 OF 86	

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs		
SYNC_MASTER=M1_MLB	SYNC_DATE=12/19/2005	

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 81 OF 86	

Revision History

Revision History

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE NONE	SHT 82 OF 86	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING		
CPU_2TO1	*	=2:1_SPACING	?	
CPU_COMP	*	25 MIL	?	DG recommends at least 25 mils, >50 mils preferred
CPU_GTLREF	*	25 MIL	?	
CPU_ITP	*	=2:1_SPACING	?	
CPU_VCCSENSE	*	25 MIL	?	

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B

SCALE	SHT	OF
NONE	83	86

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE: NONE	SHT 84 OF 86	

M9 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	?
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	?
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	?
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	?
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	?
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	?
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5 7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5 7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	5 7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	5 7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	5 14 23 60
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	5 60
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 86
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 86
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 60
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 60
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	60
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	60

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 47
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
AUDIO_55S	AUDIO	ACZ_SYNC	5 21 47
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
AUDIO_55S	AUDIO	ACZ_RST_L	5 21 47
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 47
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 47

TMDS	TMDS	TMDS_CLK_P	77 78 79
TMDS	TMDS	TMDS_CLK_N	77 78 79
TMDS	TMDS	TMDS_DATA_P<5..3>	78
TMDS	TMDS	TMDS_DATA_N<5..3>	78
TMDS	TMDS	TMDS_DATA_P<2..0>	78
TMDS	TMDS	TMDS_DATA_N<2..0>	78
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	79
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	79
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	

M9 Net Properties

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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