1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M42C MLB

11/27/2006 POST RAMP WITH LOCKED BOOTROM

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		474680	PRODUCTION RELEASED	11/27/06	?

EE DRIS:

RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFER
LT-LAWRENCE TAN
ES-ERIC SMITH
LD-LINDA DUNN

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7173	1	SCHEM,MACBOOK,MLB	SCH	
820-1889	1	PCBF,MACBOOK,MLB	PCB	

DRAWING
TITLE=U230
ABBREV=DRAWING
LAST_MODIFIED=Mon Nov 27 14:57:31 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

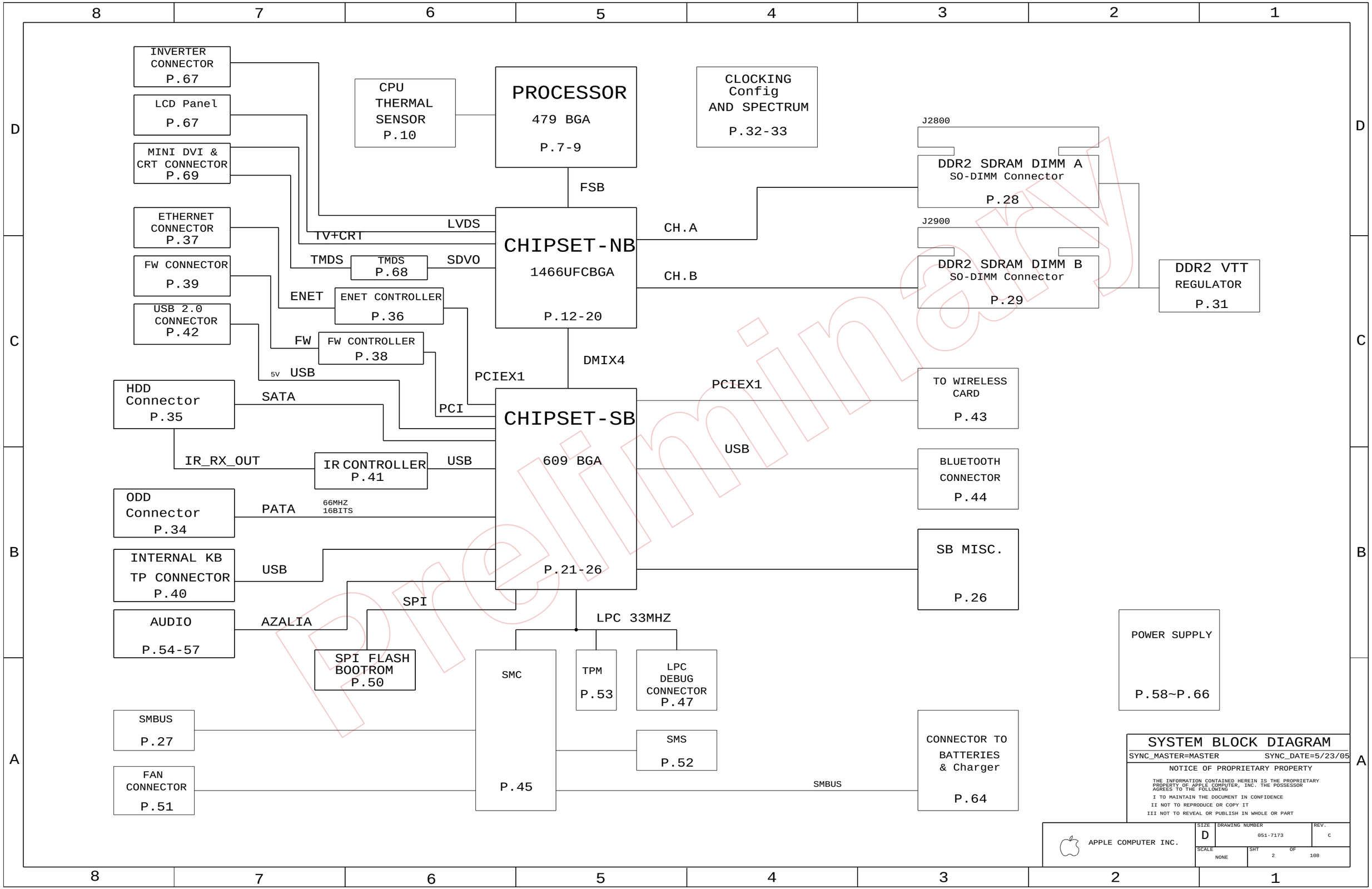
DRAFTER	DESIGN CK	ENG APPD	MFG APPD	QA APPD	DESIGNER	RELEASE	SCALE
							NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,MACBOOK

DRAWING NUMBER 051-7173
REV. C
SHT 1 OF 108



SYSTEM BLOCK DIAGRAM

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	2	108

M42A POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
DCIN
6A FUSE
U8370
SMC_DCIN_ISENSE
CHGR_EN (S5)
PBUS CONVERTER/ BATTERY CHARGER
ISL6255
U8300
(PAGE 65)
PPVBAT_S5_CHGR_REG
7A FUSE
U8310
PPBUSA_G3H
PBUSB_VSENSE
Q6150
ENABLE
3.425V G3HOT
LT3470
U8090
(PAGE 62)
PP3V42_G3H_REG
SMC PWRGD
MC33465N_30ATR
U5900
(PAGE 45)
SMC_RST_L
U8375
SMC_BATT_ISENSE
BATTERY
BATT_POS_F
3S2P / 3S3P
1V5S0_RUNSS (S0)
1V05S0_RUNSS (S0)
1.5V
1.05V
LTC3728
U7900
(PAGE 61)
PP1V5_S0
(6A MAX CURRENT)
PP1V05_S0
(8A MAX CURRENT)
1V51V05S0_PGOOD
PPBUSB_G3H
CPUVCORE
ISL6262
U7500
(PAGE 57)
U6100
SMC_CPU_VSENSE
SMC_CPU_ISENSE
PPVCORE_CPU_S0
(36A MAX CURRENT)
VR_PWRGD_CK410_L
VR_PWRGOOD_DELAY
IMVP_VR_ON (S0)
P5VS3_EN_L_RC (S3)
P5VS0_EN_RC (S0)
PP5V_S3
PP5V_S0
PP5V_S5
PP5V_S5_REG (5A MAX CURRENT)
PP3V3_S5_REG (4A MAX CURRENT)
5V
3.3V
LTC3728
U7600
(PAGE 58)
5VS5_RUNSS (S5)
3V3S5_RUNSS (S5)
RSMRST_PWRGD
5V3V3S5_PGOOD
TV 3.3V
MM157
U1901
(PAGE 19)
PP3V3_S0_NB_TVDAC
AUDIO 4.5V
TPS79501
VR6800
(PAGE 68)
PP4V5_AUDIO_ANALOG
PP3V3_S0_AUDIO (S0)
2.5V
MAX8887
U7700
(PAGE 59)
PP2V5_S3
(0.3A MAX CURRENT)
P3V3S3_EN_L_RC (S3)
PP3V3_S3
PP3V3_S0
P3V3S0_EN_RC (S0)
2.5V
MAX8887
U7701
(PAGE 59)
PP2V5_S0
PP2V5_S0_NB_DISP_PLL
MCH DPLL 1.5V
TPS73115
U1900
(PAGE 19)
PP1V5_S0_DPLL
LTC2908
U8070
(PAGE 62)
S0PWRGD_OK
1.8V
ISL6269
U7800
(PAGE 60)
PM_SLP_S4_L (S3)
PP1V8_S3_REG
PP1V8_S0
(8A MAX CURRENT)
P1V8S0_EN_L_RC (S0)
0.9V
BD3535FVM
U3100
(PAGE 31)
PP5V_S0_MEMVTT
PP0V9_S0
1.2V
MAX8516
U7720
(PAGE 59)
PP1V2_S3_ENET
PP1V2_S0
P1V2_S0_EN
PPBUS_S5_FWPWRSW
P1V2S0_EN
SMC
U5800
(PAGE 44)
SMC_PM_G2_ENABLE (S5)
LOGIC
CHGR_EN
ICH
SLP_S5_L
SLP_S4_L
SLP_S3_L
SLP_S4_L (S3)
SLP_S3_L (S0)
CLOCK
CY28445-5
U3301
(PAGE 33)
CK410_PD_VTT_PRGD_L
U2603
VR_PWRGD_CK410
U2601
PM_SB_PWROK
ICH
PLT_RST_L
CPU_PWRGD
CPU
PWRGOOD
RESET*
MCH
FSB_CPURST_L
U8080
ALL_SYS_PWRGD
SMC_ONOFF_L
BATTERY ONLY: 05
ADAPTER IN : 08-1
SMC
RSMRST_OUT(P15)
PWRGD(P12)→99ms DLY
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PWR_BUTTON(P90)
P17(BTN_OUT)
PM_RSMRST_L
IMVP_VR_ON
PM_PWRBTN_L
SMC_RST_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U5800
(PAGE 44)

SIGNAL DELAY TIME

IMVP_VR_ON	99ms
S0PWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS)TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=POWER SYNC_DATE=06/30/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 3 OF 108	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	V	V	V	V	V	V
5V3V3S3_CONT						
5V3V3S3_SKIP	V	V	V	V	V	V
ACCEL_KIONIX			V	V	V	
ACCEL_ST	V	V				V
INVERTER_BUF	V	V	V	V	V	V
INVERTER_UNBUF						
ITP						
LEMENU	V	V	V	V	V	V
MEMVTT_EN_PU	V	V	V	V	V	V
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	V	V	V	V	V	V
USB_D_OC_PU	V	V	V	V	V	V
USB_E_OC_PU	V	V	V	V	V	V
GOOD	V			V		
BETTER		V			V	
BEST			V			V
M42A_PGM	V	V	V	V	V	V
ONEWIRE_PULLUP	V	V	V	V	V	V
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	V	V	V	V	V	V
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	V	V	V	V	V	V
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	V	V	V	V	V	V
3V3_IND_3MM						
NORMAL	V	V		V	V	
FANCY			V			V
STANDOFF	V	V	V	V	V	V
FET_FDN6296	V	V	V	V	V	V
FET_STL8NH3LL						
GOOD-ST	V					
BETTER-ST		V				
BEST-KIONIX			V			
GOOD-KIONIX				V		
BETTER-KIONIX					V	
BEST-ST						V
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	V	V	V	V	V	V
M42						
M42A	V	V	V	V	V	V

BOARD STACK-UP AND CONSTRUCTION

Top		SIGNAL
2		GROUND
3		SIGNAL(High Speed)
4		SIGNAL(High Speed)
5		GROUND
6		POWER
7		POWER
8		GROUND
9		SIGNAL(High Speed)
10		SIGNAL(High Speed)
11		GROUND
BOTTOM		SIGNAL

MLB STACKUP

LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3387	1	IC,MEROM,CPU B2 DC 1.83GHZ,479 PGA	U0700	GOOD
337S3389	1	IC,MEROM,CPU B2 DC 2.0GHZ,479 PGA	U0700	BETTER
337S3389	1	IC,MEROM,CPU B2 DC 2.0GHZ,479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	LEMENU
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	LEMENU
359S0109	1	IC,SLG8LP436,CLOCK GEN,68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1942	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	M42A_PGM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	M42A_PGM
341S1946	1	IC,SMC,176P BGA,HS8/2116	U5800	M42A_PGM
341S1890	1	IC,PSOC+W/USB,56P,MLF,CY8C24794	U5100	M42A_PGM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:WES	CRITICAL	GOOD-ST
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:WET	CRITICAL	BETTER-ST
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:WEW	CRITICAL	BEST-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:WEV	CRITICAL	GOOD-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:W6V	CRITICAL	BETTER-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:WEU	CRITICAL	BEST-ST

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7173 | REV. C

SCALE NONE | SHT 4 OF 108

Functional Test Points

Power Supply NO_TESTs

NO_TEST

I93		IMVP6_RBIAS	58
I94		IMVP6_COMP	58
I95		5VS5_RUNSS	59 63
I96		1V5S0_RUNSS	62 63
I101		1V8S3_COMP	61
I102		1V8S3_FSET	61
I103	TRUE	3V3S5_COMP	
I104	TRUE	3V3S5_FSET	
I106	TRUE	1V05S0_COMP	
I105	TRUE	1V05S0_FSET	
I107	TRUE	P3V42G3H_FB	63

CLOCK NO_TESTS

NO_TEST

I111	TRUE	CK410_CPU0_N	32 33
I112	TRUE	CK410_CPU0_P	32 33
I113	TRUE	CK410_CPU1_N	32 33
I115	TRUE	CK410_CPU1_P	32 33
I114	TRUE	CK410_CPU2_ITP_SRC10_N	32 33
I116	TRUE	CK410_CPU2_ITP_SRC10_P	32 33
I117	TRUE	CK410_DOT96_27M_N	32 33
I118	TRUE	CK410_DOT96_27M_P	32 33
I119	TRUE	CK410_LVDS_N	32 33
I120	TRUE	CK410_LVDS_P	32 33
I122	TRUE	CK410_PCI4_CLK_SPN	
I122	TRUE	CK410_PCIF1_CLK	32 33
I123	TRUE	CK410_SRC1_N_SPN	6
I122	TRUE	CK410_SRC1_P_SPN	6
I125	TRUE	CK410_SRC2_N	32 33
I183	TRUE	CK410_SRC2_P	32 33
I185	TRUE	CK410_SRC3_N_SPN	6
I185	TRUE	CK410_SRC3_P_SPN	6
I186	TRUE	CK410_SRC4_N	32 33
I187	TRUE	CK410_SRC4_P	32 33
I188	TRUE	CK410_SRC5_N	32 33
I189	TRUE	CK410_SRC5_P	32 33
I190	TRUE	CK410_SRC6_N	32 33
I191	TRUE	CK410_SRC6_P	32 33
I192	TRUE	CK410_SRC7_N_SPN	6
I193	TRUE	CK410_SRC7_P_SPN	6
I194	TRUE	CK410_SRC8_N	32 33
I195	TRUE	CK410_SRC8_P	32 33
I196	TRUE	CK410_SRC_CLKREQ1_L_SPN	6
I197	TRUE	CK410_SRC_CLKREQ3_L_SPN	6
I198	TRUE	CK410_SRC_CLKREQ8_L	32 33

FIREWARE NO_TESTS

NO_TEST

I199	TRUE	FW_B_TPA_N_SPN	6
I200	TRUE	FW_B_TPA_P_SPN	6
I201	TRUE	FW_B_TPBIAS_SPN	6
I202	TRUE	FW_B_TPB_N_SPN	6
I203	TRUE	FW_B_TPB_P_SPN	6
I204	TRUE	FW_C_TPA_N_SPN	6
I205	TRUE	FW_C_TPA_P_SPN	6
I206	TRUE	FW_C_TPBIAS_SPN	6
I207	TRUE	FW_C_TPB_N_SPN	6
I208	TRUE	FW_C_TPB_P_SPN	6

LVDS NO_TESTS

NO_TEST

I209	TRUE	LVDS_B_CLK_N_SPN	6
I210	TRUE	LVDS_B_CLK_P_SPN	6
I211	TRUE	LVDS_B_DATA_N0_SPN	6
I212	TRUE	LVDS_B_DATA_N1_SPN	6
I213	TRUE	LVDS_B_DATA_N2_SPN	6
I214	TRUE	LVDS_B_DATA_P1_SPN	6
I215	TRUE	LVDS_B_DATA_P2_SPN	6

ETHERNET NO_TESTS

NO_TEST

I216	TRUE	ENET_MDI_TRAN_P<2>	37
I217	TRUE	ENET_MDI_TRAN_N<2>	37
I218	TRUE	ENET_MDI_TRAN_P<3>	37

NO_TEST

I219	TRUE	SMC_FAN_3_TACH	45 46
I220	TRUE	ALS_LEFT	45 46

Fan Connectors

FUNC_TEST

I12	TRUE	=PP5V_S0_FAN_RT	51 64
I15	TRUE	FAN_RT_PWM	51
I16	TRUE	FAN_RT_TACH	51
I17	TRUE	=PP3V3_S0_FAN_RT	51 64
I150	TRUE	SMC_FAN_1_CTL	45 51
I149	TRUE	SMC_FAN_1_TACH	45 51

LPC+ Debug Connector

FUNC_TEST

I20	TRUE	=PP3V42_G3H_LPCPLUS	47 64
I19	TRUE	=PP5V_S0_LPCPLUS	47 64
I18	TRUE	LPC_AD<0>	21 45 47 53
I17	TRUE	LPC_AD<1>	21 45 47 53
I71	TRUE	LPC_FRAME_L	21 45 47 53
I72	TRUE	PM_CLKRUN_L	23 38 45 47 53
I73	TRUE	BOOT_LPC_SPI_L	22 45 47
I74	TRUE	SMC_TMS	45 46 47
I75	TRUE	DEBUG_RST_L	26 47
I76	TRUE	SMC_TRST_L	45 47
I77	TRUE	SMC_TDO	45 46 47
I78	TRUE	SMC_MD1	45 47
I79	TRUE	SMC_TX_L	45 46 47
I80	TRUE	FWH_INIT_L	6 21 47
I81	TRUE	PCI_CLK_PORT80_LPC	33 47
I82	TRUE	LPC_AD<2>	21 45 47 53
I83	TRUE	LPC_AD<3>	21 45 47 53
I84	TRUE	INT_SERIRQ	23 45 47 53
I85	TRUE	PM_SUS_STAT_L	23 45 46 47 53
I86	TRUE	SMC_TDI	45 46 47
I87	TRUE	SMC_TCK	45 46 47
I88	TRUE	SMC_RST_L	45 46 47
I89	TRUE	SMC_NMI	45 47
I91	TRUE	SMC_RX_L	45 46 47
I90	TRUE	SV_SET_UP	23 47

Other Func Test Points

FUNC_TEST

I92	TRUE	=PP1V05_S0_REG	62 64

SMBus FUNC_TEST

I182

	TRUE	SMBUS_SMC_MLB_SCL	27
I183	TRUE	SMBUS_SMC_MLB_SDA	27

FIREWIRE FUNC_TEST

I152	TRUE	PPFW_SWITCH	39

SLEEP LED FUNC_TEST

I155	TRUE	SYS_LED_ANODE	35 46

SMC FUNC_TEST

I145	TRUE	SMC_LID	40 45 46 65
I146	TRUE	SMC_MANUAL_RST_L	46
I156	TRUE	SMC_CPU_VSENSE	45 48

Power Supply FUNC_TEST

I160	TRUE	ALL_SYS_PWRGD	26 45 63
I161	TRUE	PPVCORE_CPU_S0	64
I162	TRUE	PP1V05_S0	64
I140	TRUE	PP1V5_S0	64
I163	TRUE	PP1V8_S0	64
I165	TRUE	PP2V5_S0	64
I166	TRUE	PP3V3_S0	64
I167	TRUE	PP5V_S0	64
I168	TRUE	PP1V2_S3	64
I169	TRUE	PP1V8_S3	64
I170	TRUE	PP2V5_S3	64
I172	TRUE	PP3V3_S3	64
I171	TRUE	PP5V_S3	64
I177	TRUE	PP3V3_S5	64
I178	TRUE	PP5V_S5	64
I176	TRUE	PP3V42_G3H	64
I174	TRUE	PPBUSA_G3H	
I175	TRUE	PPBUSB_G3H	64
I179	TRUE	PP18V5_G3H	64
I181	TRUE	PP0V9_S0	64

Battery Digital Connector

FUNC_TEST

I1	TRUE	SMC_BS_ALRT_L	45 46 65
I3	TRUE	SMBUS_BATT_SCL_F	65
I4	TRUE	SMBUS_BATT_SDA_F	65
I2	TRUE	BATT_IN	
I177	TRUE	BATT_POS	65
I146	TRUE	BATT_NEG	65

Audio FUNC_TEST

I9	TRUE	PP5V_S0_AUDIO_PWR	
I13	TRUE	PP5V_S0_AUDIO	
I10	TRUE	GND_AUDIO_PWR	64
I21	TRUE	GND_AUDIO_CODEC	64
I22	TRUE	ACZ_SDATAIN<0>	21 54
I24	TRUE	ACZ_SDATAOUT	21 54
I23	TRUE	ACZ_BITCLK	21 54
I26	TRUE	ACZ_RST_L	21 54 57
I25	TRUE	ACZ_SYNC	21 54

Battery FUNC_TEST

I29	TRUE	SMC_BATT_ISET	45 66
I32	TRUE	SMC_BATT_CHG_EN	45 46 66
I31	TRUE	SMC_BC_ACOK	45 46 65 66
I33	TRUE	SMC_PS_ON	39 45 46 65
I36	TRUE	SMC_BATT_TRICKLE_EN_L	45 46 66
I38	TRUE	SYS_ONEWIRE	45 46 65

USB FUNC_TEST

I44	TRUE	TP_USBP_E	6
I47	TRUE	TP_USBN_E	6
I46	TRUE	TP_USBP_F	
I48	TRUE	TP_USBN_F	

DC-JACK FUNC_TEST

I57	TRUE	ACIN_ENABLE_GATE	65

Battery charger FUNC_TEST

I58	TRUE	PPVBAT_G3H_CHGR_OUT	66

INVERTER CONNECTOR FUNC_TEST

I60	TRUE	PPBUS_ALL_INV_CONN	67
I59	TRUE	INV_GND	67
I61	TRUE	PP5V_INV_F	67
I63	TRUE	INV_BKLIGHT_PWM_L	67

FUNC TEST 1 OF 2

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHT 5 OF 108	

(EMI PAD FOR INVERTER GONNECTOR)

67 INVT_CHGND — 1 ZS0620 EMI-SPRING CLIP-SM-M42

SPKR-MIC-CLIP-M42
NC — 1 ZS0621 SM

CHASSIS GND

BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_IO 6 — OMIT Z0606 5R2P3-7SQB 1

65 =GND_BATT_CHGND
56 =GND_CHASSIS_AUDIO_JACK
=GND_CHASSIS_AUDIO_SPKRCONN
57 =GND_CHASSIS_AUDIO_MIC
=GND_CHASSIS_AUDIO_SHIELD1
=GND_CHASSIS_AUDIO_SHIELD2
=GND_CHASSIS_AUDIO_SHIELD3
28 =GND_CHASSIS_DIPDIMM_LEFT

SATA,LVDS CONNECTOR CHASSIS GND

GND_CHASSIS_SATA 35 — OMIT Z0607 6P5R2P6-5P5B 1
VOLTAGE=0V MAKE_BASE=TRUE

67 =GND_CHASSIS_LVDS

C0607 0.1UF 10% 16V X5R 402
C0608 0.01uF 10% 16V CERM 402

DCIN CONNECTOR CHASSIS GND

GND_CHASSIS_DCIN — OMIT Z0602 5R2P3-7SQB 1
VOLTAGE=0V MAKE_BASE=TRUE

65 =GND_DCIN_CHGND
37 =GND_CHASSIS_RJ45
69 =GND_CHASSIS_TMDS_UPPER

C0630 0.1UF 10% 16V X5R 402

I/O CONNECTOR CHASSIS GND

GND_CHASSIS_IO 6 — OMIT Z0608 5P0R2P3-7BLB 1
VOLTAGE=0V MAKE_BASE=TRUE

39 =GND_CHASSIS_FW_DOWN
42 =GND_CHASSIS_USB

C0610 0.1UF 10% 16V X5R 402
C0611 0.01uF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_CENTER — OMIT Z0610 5R2P3-7SQB 1
VOLTAGE=0V MAKE_BASE=TRUE

29 28 =GND_CHASSIS_DIPDIMM_CENTER

C0616 0.1UF 10% 16V X5R 402
C0617 0.01uF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_RIGHT — OMIT Z0609 5R2P3-7SQB 1
VOLTAGE=0V MAKE_BASE=TRUE

29 =GND_CHASSIS_DIPDIMM_RIGHT

C0614 0.1UF 10% 16V X5R 402
C0615 0.01uF 10% 16V CERM 402

OMIT Z0601 5R2P3-7SQB
GND_CHASSIS_CPU 1

C0612 0.1UF 10% 16V X5R 402
C0613 0.01uF 10% 16V CERM 402

OMIT Z0611 5R2P3-7B
GND_CHASSIS_FANSCREW 1

C0618 0.1UF 10% 16V X5R 402
C0619 0.01uF 10% 16V CERM 402

DIGITAL GND SCREW HOLE

OMIT Z0603 STDOFF-4.5OD3.95H-1.1-3.7-TH1
NB_RIGHT_DOWN_SCREW 1
R0612 0 5% 1/16W MF-LF 402

OMIT Z0604 STDOFF-4.5OD3.95H-1.1-3.7-TH1
CPU_THERMAL_SCREW_UP 1
R0610 0 5% 1/16W MF-LF 402

OMIT Z0605 STDOFF-4.5OD3.95H-1.1-3.7-TH1
CPU_THERMAL_SCREW_DOWN 1
R0611 0 5% 1/16W MF-LF 402

OMIT Z0621 STDOFF-4.5OD3.95H-1.1-3.7-TH1
CPU_THERMAL_SCREW_RIGHT 1
R0621 0 5% 1/16W MF-LF 402

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

13	LVDS_B_CLK_N	LVDS_B_CLK_N_SPN	5
13	LVDS_B_CLK_P	LVDS_B_CLK_P_SPN	5
13	LVDS_B_DATA_N<0>	LVDS_B_DATA_N0_SPN	5
13	LVDS_B_DATA_N<1>	LVDS_B_DATA_N1_SPN	5
13	LVDS_B_DATA_N<2>	LVDS_B_DATA_N2_SPN	5
13	LVDS_B_DATA_P<0>	LVDS_B_DATA_P0_SPN	5
13	LVDS_B_DATA_P<1>	LVDS_B_DATA_P1_SPN	5
13	LVDS_B_DATA_P<2>	LVDS_B_DATA_P2_SPN	5

MAKE_BASE=TRUE

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

13	PEG_D2R_N<0>	PEG_D2R_N0_SPN
13	PEG_D2R_N<2>	PEG_D2R_N2_SPN
13	PEG_D2R_N<3>	PEG_D2R_N3_SPN
13	PEG_D2R_N<4>	PEG_D2R_N4_SPN
13	PEG_D2R_N<5>	PEG_D2R_N5_SPN
13	PEG_D2R_N<6>	PEG_D2R_N6_SPN
13	PEG_D2R_N<7>	PEG_D2R_N7_SPN
13	PEG_D2R_N<8>	PEG_D2R_N8_SPN
13	PEG_D2R_N<9>	PEG_D2R_N9_SPN
13	PEG_D2R_N<10>	PEG_D2R_N10_SPN
13	PEG_D2R_N<11>	PEG_D2R_N11_SPN
13	PEG_D2R_N<12>	PEG_D2R_N12_SPN
13	PEG_D2R_N<13>	PEG_D2R_N13_SPN
13	PEG_D2R_N<14>	PEG_D2R_N14_SPN
13	PEG_D2R_N<15>	PEG_D2R_N15_SPN
13	PEG_D2R_P<0>	PEG_D2R_P0_SPN
13	PEG_D2R_P<2>	PEG_D2R_P2_SPN
13	PEG_D2R_P<3>	PEG_D2R_P3_SPN
13	PEG_D2R_P<4>	PEG_D2R_P4_SPN
13	PEG_D2R_P<5>	PEG_D2R_P5_SPN
13	PEG_D2R_P<6>	PEG_D2R_P6_SPN
13	PEG_D2R_P<7>	PEG_D2R_P7_SPN
13	PEG_D2R_P<8>	PEG_D2R_P8_SPN
13	PEG_D2R_P<9>	PEG_D2R_P9_SPN
13	PEG_D2R_P<10>	PEG_D2R_P10_SPN
13	PEG_D2R_P<11>	PEG_D2R_P11_SPN
13	PEG_D2R_P<12>	PEG_D2R_P12_SPN
13	PEG_D2R_P<13>	PEG_D2R_P13_SPN
13	PEG_D2R_P<14>	PEG_D2R_P14_SPN
13	PEG_D2R_P<15>	PEG_D2R_P15_SPN
13	PEG_R2D_C_N<4>	PEG_R2D_C_N4_SPN
13	PEG_R2D_C_N<5>	PEG_R2D_C_N5_SPN
13	PEG_R2D_C_N<6>	PEG_R2D_C_N6_SPN
13	PEG_R2D_C_N<7>	PEG_R2D_C_N7_SPN
13	PEG_R2D_C_N<8>	PEG_R2D_C_N8_SPN
13	PEG_R2D_C_N<9>	PEG_R2D_C_N9_SPN
13	PEG_R2D_C_N<10>	PEG_R2D_C_N10_SPN
13	PEG_R2D_C_N<11>	PEG_R2D_C_N11_SPN
13	PEG_R2D_C_N<12>	PEG_R2D_C_N12_SPN
13	PEG_R2D_C_N<13>	PEG_R2D_C_N13_SPN
13	PEG_R2D_C_N<14>	PEG_R2D_C_N14_SPN
13	PEG_R2D_C_N<15>	PEG_R2D_C_N15_SPN
13	PEG_R2D_C_P<4>	PEG_R2D_C_P4_SPN
13	PEG_R2D_C_P<5>	PEG_R2D_C_P5_SPN
13	PEG_R2D_C_P<6>	PEG_R2D_C_P6_SPN
13	PEG_R2D_C_P<7>	PEG_R2D_C_P7_SPN
13	PEG_R2D_C_P<8>	PEG_R2D_C_P8_SPN
13	PEG_R2D_C_P<9>	PEG_R2D_C_P9_SPN
13	PEG_R2D_C_P<10>	PEG_R2D_C_P10_SPN
13	PEG_R2D_C_P<11>	PEG_R2D_C_P11_SPN
13	PEG_R2D_C_P<12>	PEG_R2D_C_P12_SPN
13	PEG_R2D_C_P<13>	PEG_R2D_C_P13_SPN
13	PEG_R2D_C_P<14>	PEG_R2D_C_P14_SPN
13	PEG_R2D_C_P<15>	PEG_R2D_C_P15_SPN

MAKE_BASE=TRUE

GND_CHASSIS_IO1
VOLTAGE=0V MAKE_BASE=TRUE

69 =GND_CHASSIS_TMDS_DOWN
I393
39 =GND_CHASSIS_FW_UPPER

OMIT Z0612 STDOFF-4.2OD2.15H-1.2-TH
NC 1

OMIT Z0613 STDOFF-4.2OD2.15H-1.2-TH
NC 1

NB CFG ALIASES

NO-CONNECT UNUSED CFG INTERFACE PORTS

14	NB_CFG<3>	TP_NB_CFG3
14	NB_CFG<4>	TP_NB_CFG4
14	NB_CFG<6>	TP_NB_CFG6
14	NB_CFG<8>	TP_NB_CFG8
14	NB_CFG<10>	TP_NB_CFG10
14	NB_CFG<11>	TP_NB_CFG11
14	NB_CFG<12>	TP_NB_CFG12
14	NB_CFG<13>	TP_NB_CFG13
14	NB_CFG<14>	TP_NB_CFG14
14	NB_CFG<15>	TP_NB_CFG15
14	NB_CFG<17>	TP_NB_CFG17

MAKE_BASE=TRUE

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

21	SATA_A_D2R_N	SATA_A_D2R_N_SPN
21	SATA_A_D2R_P	SATA_A_D2R_P_SPN
21	SATA_A_R2D_C_N	SATA_A_R2D_C_N_SPN
21	SATA_A_R2D_C_P	SATA_A_R2D_C_P_SPN

MAKE_BASE=TRUE

PCI_EXP ALIASES

NO-CONNECT UNUSED PCI_EXP INTERFACE PORTS

22	PCIE_C_D2R_N	PCIE_C_D2R_N_SPN
22	PCIE_C_D2R_P	PCIE_C_D2R_P_SPN
22	PCIE_C_R2D_C_N	PCIE_C_R2D_C_N_SPN
22	PCIE_C_R2D_C_P	PCIE_C_R2D_C_P_SPN
22	PCIE_D_D2R_N	PCIE_D_D2R_N_SPN
22	PCIE_D_D2R_P	PCIE_D_D2R_P_SPN
22	PCIE_D_R2D_C_N	PCIE_D_R2D_C_N_SPN
22	PCIE_D_R2D_C_P	PCIE_D_R2D_C_P_SPN
22	PCIE_E_D2R_N	PCIE_E_D2R_N_SPN
22	PCIE_E_D2R_P	PCIE_E_D2R_P_SPN
22	PCIE_E_R2D_C_N	PCIE_E_R2D_C_N_SPN
22	PCIE_E_R2D_C_P	PCIE_E_R2D_C_P_SPN
22	PCIE_F_D2R_N	PCIE_F_D2R_N_SPN
22	PCIE_F_D2R_P	PCIE_F_D2R_P_SPN
22	PCIE_F_R2D_C_N	PCIE_F_R2D_C_N_SPN
22	PCIE_F_R2D_C_P	PCIE_F_R2D_C_P_SPN

MAKE_BASE=TRUE

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

32	CK410_SRC1_N	CK410_SRC1_N_SPN 5
32	CK410_SRC1_P	CK410_SRC1_P_SPN 5
32	CK410_SRC3_N	CK410_SRC3_N_SPN 5
32	CK410_SRC3_P	CK410_SRC3_P_SPN 5
32	CK410_SRC7_N	CK410_SRC7_N_SPN 5
32	CK410_SRC7_P	CK410_SRC7_P_SPN 5
32	CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L_SPN 5
32	CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L_SPN 5

MAKE_BASE=TRUE

SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

23 SUS_CLK_SB — SUS_CLK_SB_SPN
MAKE_BASE=TRUE

SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

28	MEM_A_A<15>	MEM_A_A15_SPN
28	MEM_A_A<14>	MEM_A_A14_SPN
29	MEM_B_A<15>	MEM_B_A15_SPN
29	MEM_B_A<14>	MEM_B_A14_SPN

MAKE_BASE=TRUE

Ethernet ALIASES

36	ENET_CTRL12	ENET_CTRL12_SPN
36	ENET_CTRL25	ENET_CTRL25_SPN

MAKE_BASE=TRUE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0722	4	THERMAL STANDOFF	Z0603,Z0604,Z0605,Z0621	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0612	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0613	STANDOFF

FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

38	FW_B_TPBIAS	FW_B_TPBIAS_SPN	5
38	FW_B_TPA_P	FW_B_TPA_P_SPN	5
38	FW_B_TPA_N	FW_B_TPA_N_SPN	5
38	FW_B_TPB_P	FW_B_TPB_P_SPN	5
38	FW_B_TPB_N	FW_B_TPB_N_SPN	5
38	FW_C_TPBIAS	FW_C_TPBIAS_SPN	5
38	FW_C_TPA_P	FW_C_TPA_P_SPN	5
38	FW_C_TPA_N	FW_C_TPA_N_SPN	5
38	FW_C_TPB_P	FW_C_TPB_P_SPN	5
38	FW_C_TPB_N	FW_C_TPB_N_SPN	5

MAKE_BASE=TRUE

39 =FWPWR_PWRON — NC_FWPWR_PWRON
NO_TEST=TRUE MAKE_BASE=TRUE

USB PORT A = External USB2.0 Port

42 =USB2_EXTA_P — USB2_EXTA_P — USB_A_P 22
42 =USB2_EXTA_N — USB2_EXTA_N — USB_A_N 22
42 =EXTAUSB_OC_L — EXTAUSB_OC_L — USB_A_OC_L 22
MAKE_BASE=TRUE

USB PORT B = Trackpad(Geyser)

40 =USB2_GEYSER_P — USB2_GEYSER_P — USB_B_P 22
40 =USB2_GEYSER_N — USB2_GEYSER_N — USB_B_N 22
MAKE_BASE=TRUE

USB PORT C = External USB2.0 Port B

42 =USB2_EXTB_P — USB2_EXTB_P — USB_C_P 22
42 =USB2_EXTB_N — USB2_EXTB_N — USB_C_N 22
42 =EXTBUSB_OC_L — EXTBUSB_OC_L — USB_C_OC_L 22
MAKE_BASE=TRUE

USB PORT D = CAMERA

67 =USB2_CAMERA_P — USB2_CAMERA_P — USB_D_P 22
67 =USB2_CAMERA_N — USB2_CAMERA_N — USB_D_N 22
MAKE_BASE=TRUE

USB PORT "E" = Unused

5 TP_USBP_E — USB_E_P 22
MAKE_BASE=TRUE
5 TP_USBN_E — USB_E_N 22
MAKE_BASE=TRUE

USB PORT "F" = IR CONTROLLER

41 =USB2_IR_P — USB_IR_P — USB_F_P 22
41 =USB2_IR_N — USB_IR_N — USB_F_N 22
MAKE_BASE=TRUE

USB PORT "G" = BLUETOOTH

44 =USB2_BT_P — USB_BT_P — USB_G_P 22
44 =USB2_BT_N — USB_BT_N — USB_G_N 22
MAKE_BASE=TRUE

USB PORT "H" = PCI-E Mini Card

43 =USB2_AIRPORT_P — USB2_AIRPORT_P — USB_H_P 22
43 =USB2_AIRPORT_N — USB2_AIRPORT_N — USB_H_N 22
MAKE_BASE=TRUE

ANALOG SWITCH GPIO

69 =SB_GPIO22 — SB_GPIO22 — TP_SB_GPIO22 22
MAKE_BASE=TRUE

45 14 PM_EXTTS_L<0> — DIMM_OVERTEMP_L 28 29
MAKE_BASE=TRUE

47 21 5 FWH_INIT_L — SMC_CPU_INIT_3_3_L 45
MAKE_BASE=TRUE

SIGNAL ALIAS /RESET

SYNC_MASTER=ENET — SYNC_DATE=08/19/2005

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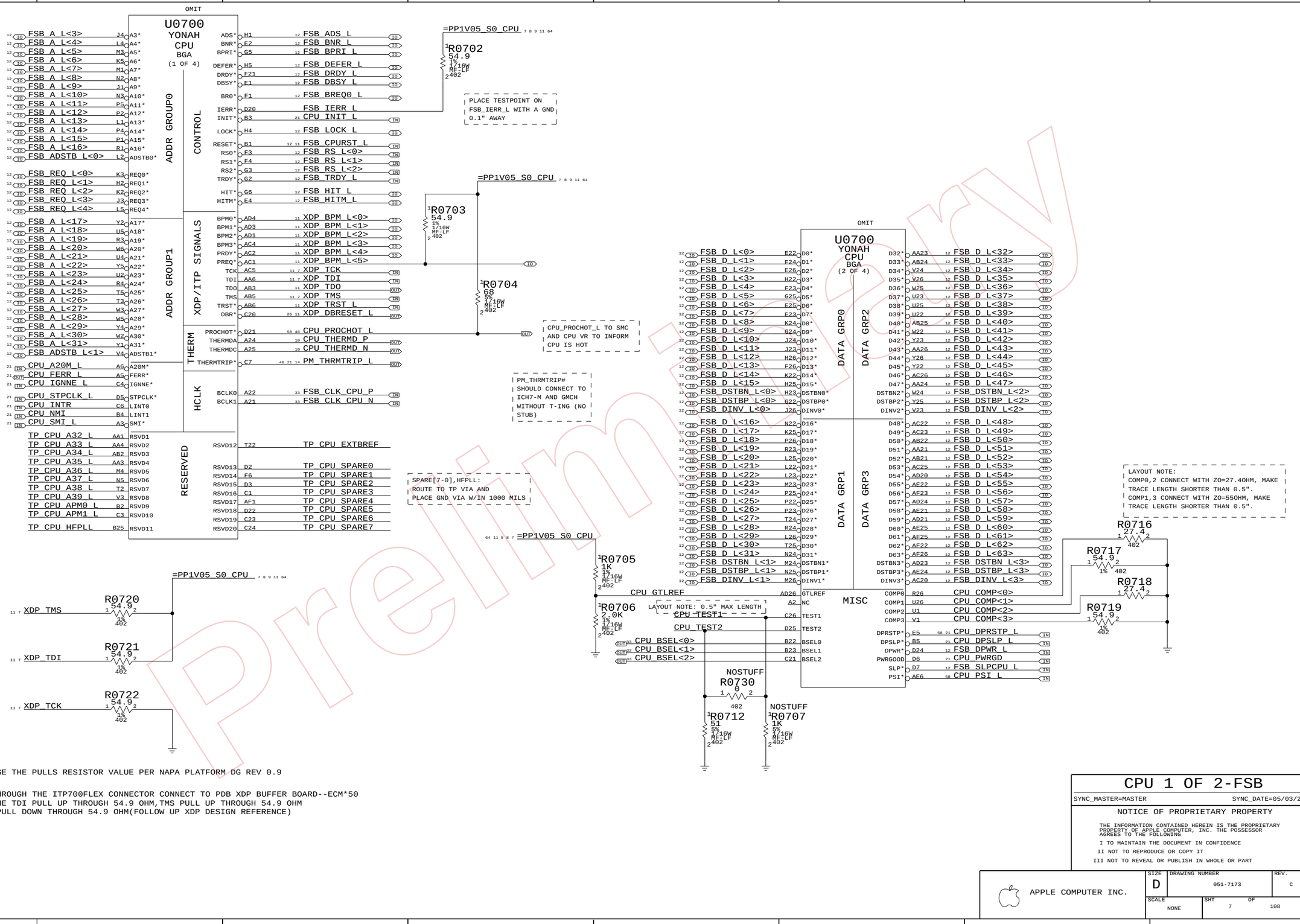
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 6 OF 108	



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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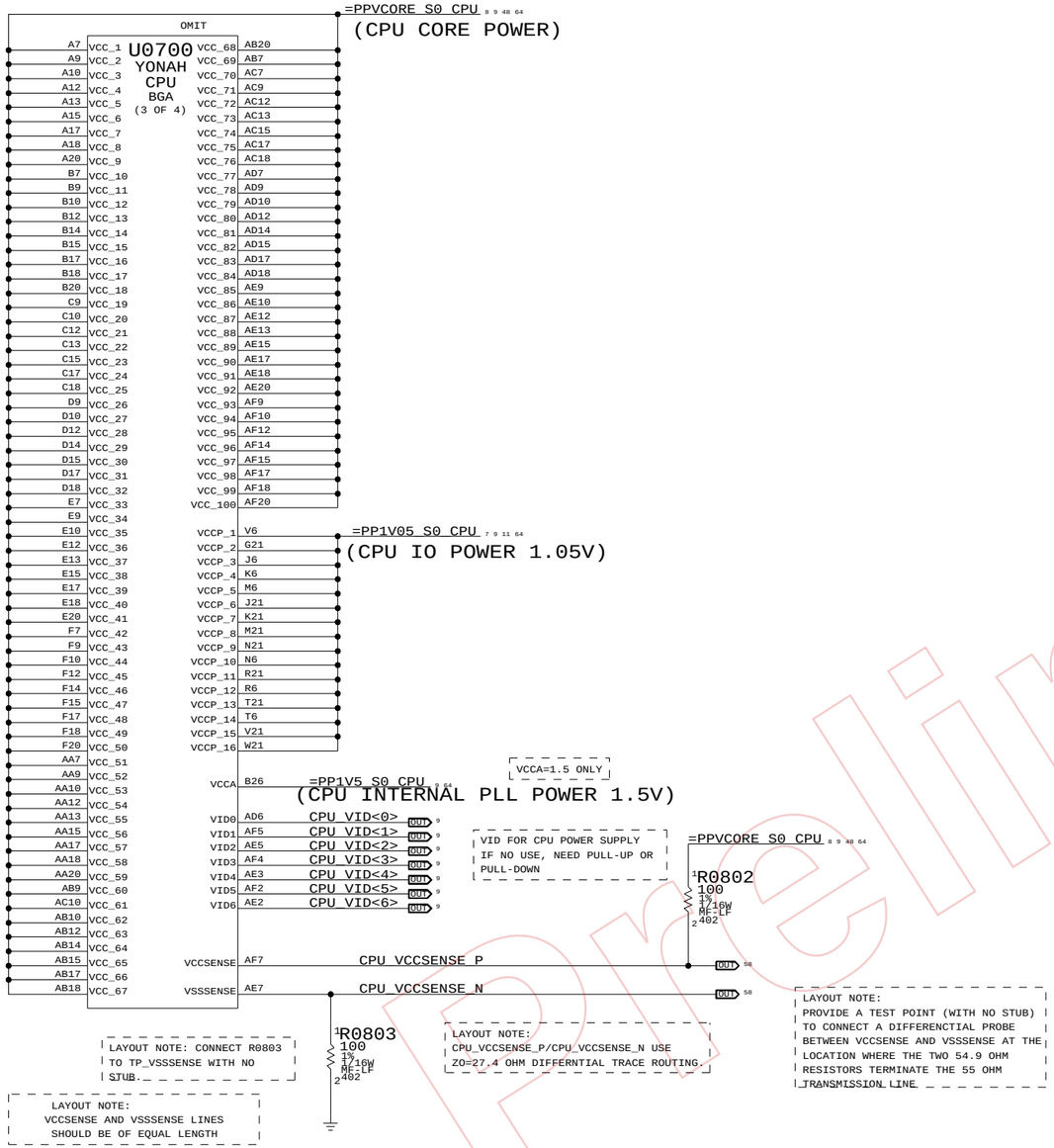
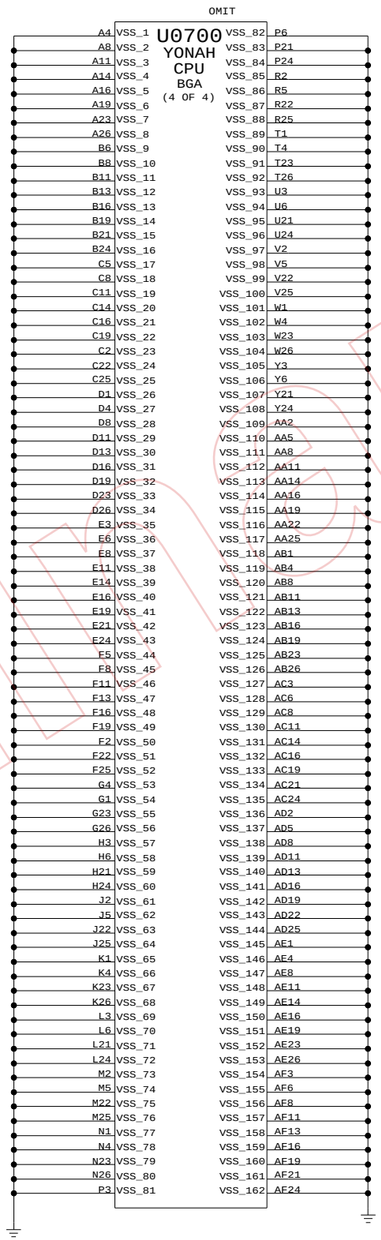
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 7 OF 108	





CPU 2 OF 2-PWR/GND

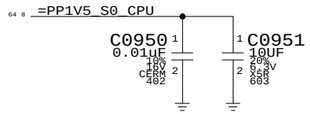
SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

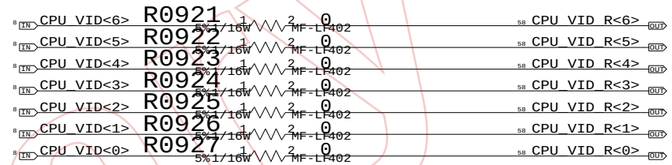
SCALE	SHT	OF
NONE	8	108

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY
138S0606	138S0602	?	ALL	USE TAIYO

CPU CORE VID<> SETTINGS

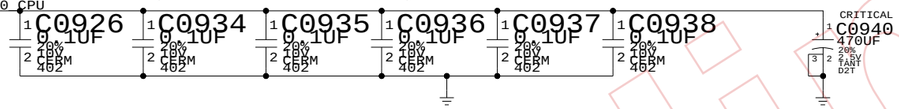


R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

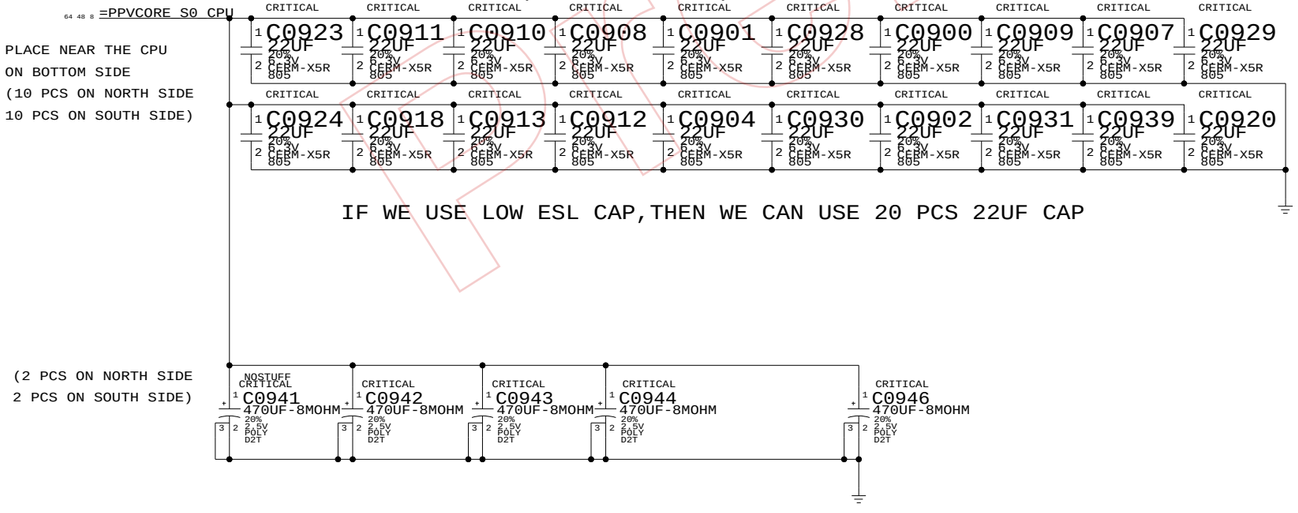
VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

THIS 470UF FOR CPU,GMCH FSB BUS 1.05V

PLACE NEAR THE NORTH BRIDGE
ON BOTTOM SIDE



VCC CORE DECOUPLING
(CPU CORE POWER)



IF WE USE LOW ESL CAP,THEN WE CAN USE 20 PCS 22UF CAP

		MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM	TBD		TBD
SINGLE CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM		TBD	
DUAL CORE LV CPU	VCCHFM	1.0		1.1625
	VCCLFM		TBD	
ULV CPU	VCCHFM	TBD		TBD
	VCCLFM		TBD	

UNIT: V

ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE(VCORE VOLTAGE)!
REFER TO YONAH PROCESSOR EMTS REV 1.0
VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
VCCLFM: VCORE AT LOWEST FREQUENCY MODE

CPU DECAPS & VID<>

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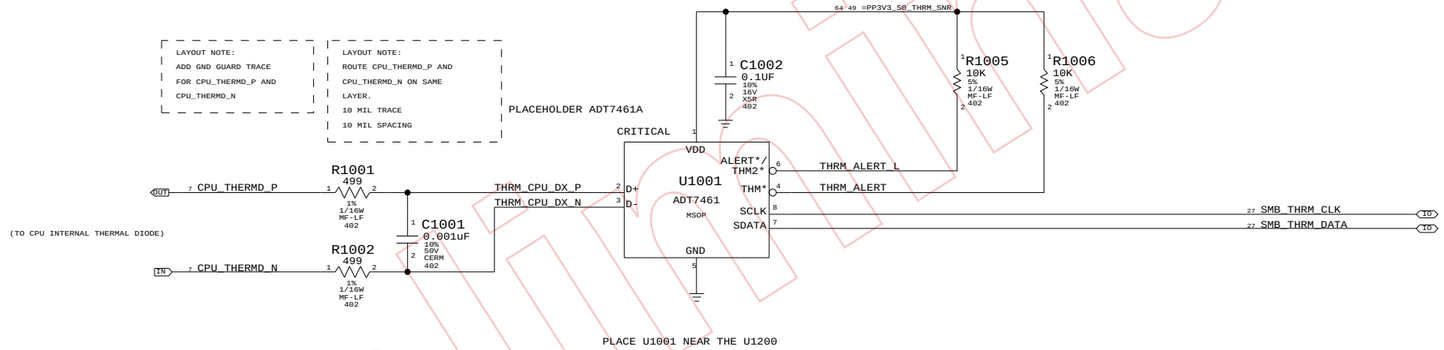
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 9 OF 108	

CPU ZONE THERMAL SENSOR



CPU MISC1-TEMP SENSOR

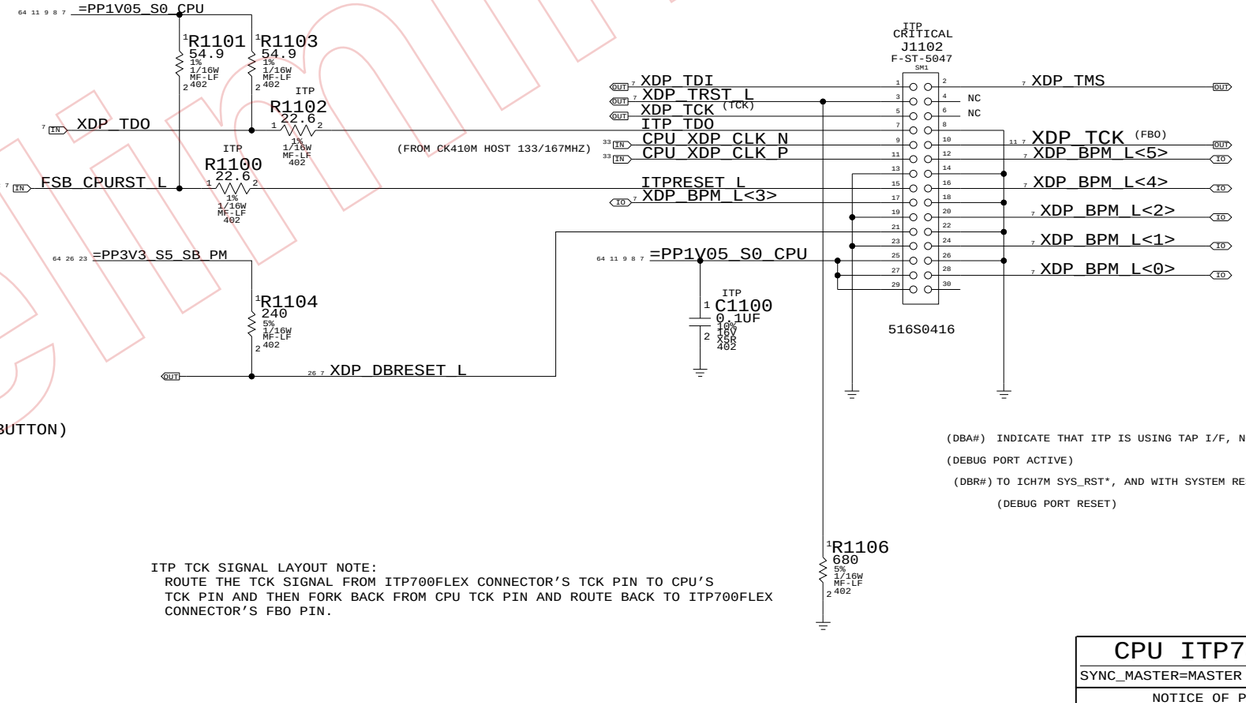
SYNC_MASTER=ENET SYNC_DATE=08/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	10	108

CPU ITP700FLEX DEBUG SUPPORT



(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.

(DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC

(DEBUG PORT RESET)

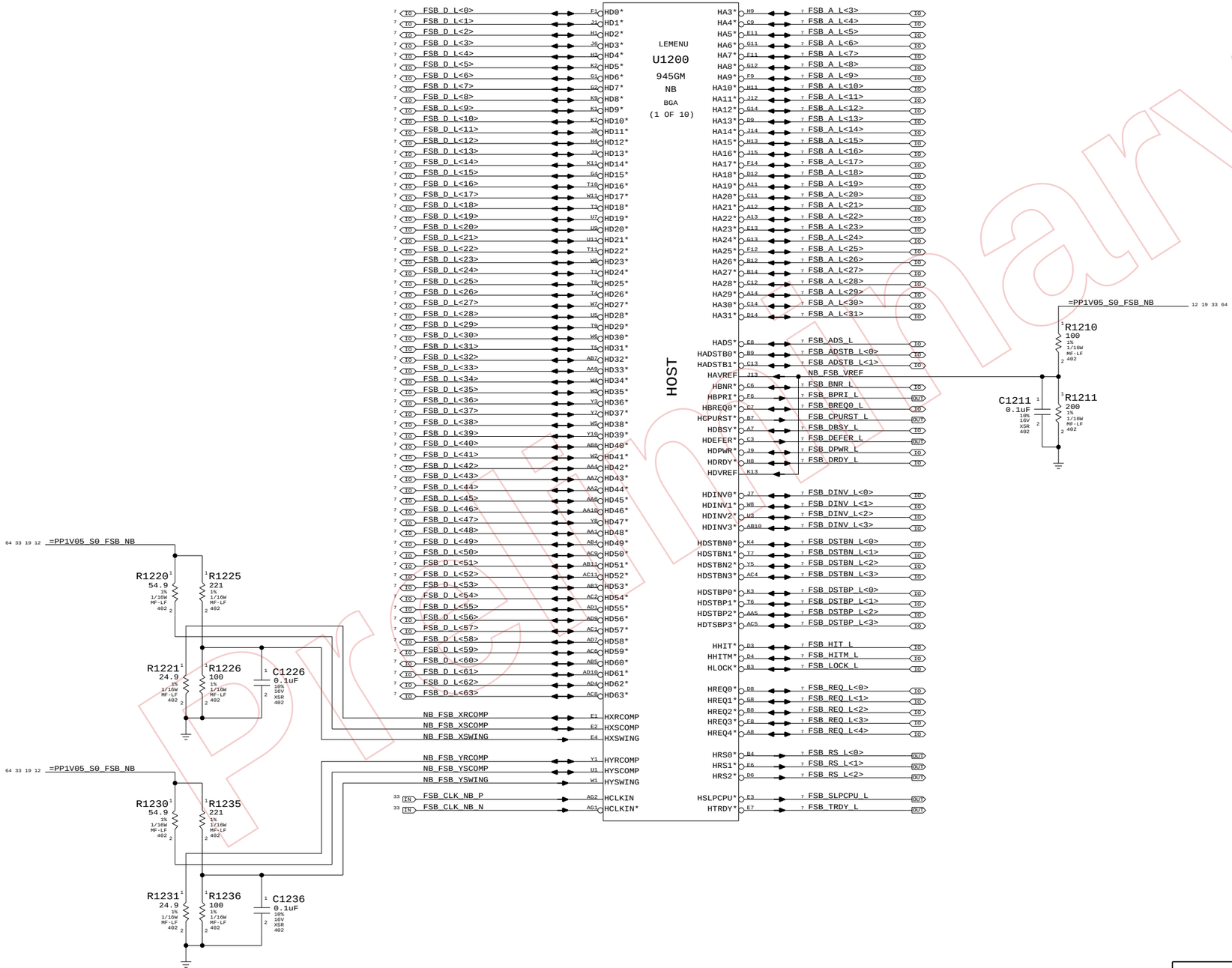
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 11 OF 108	



NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 12 OF 108	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

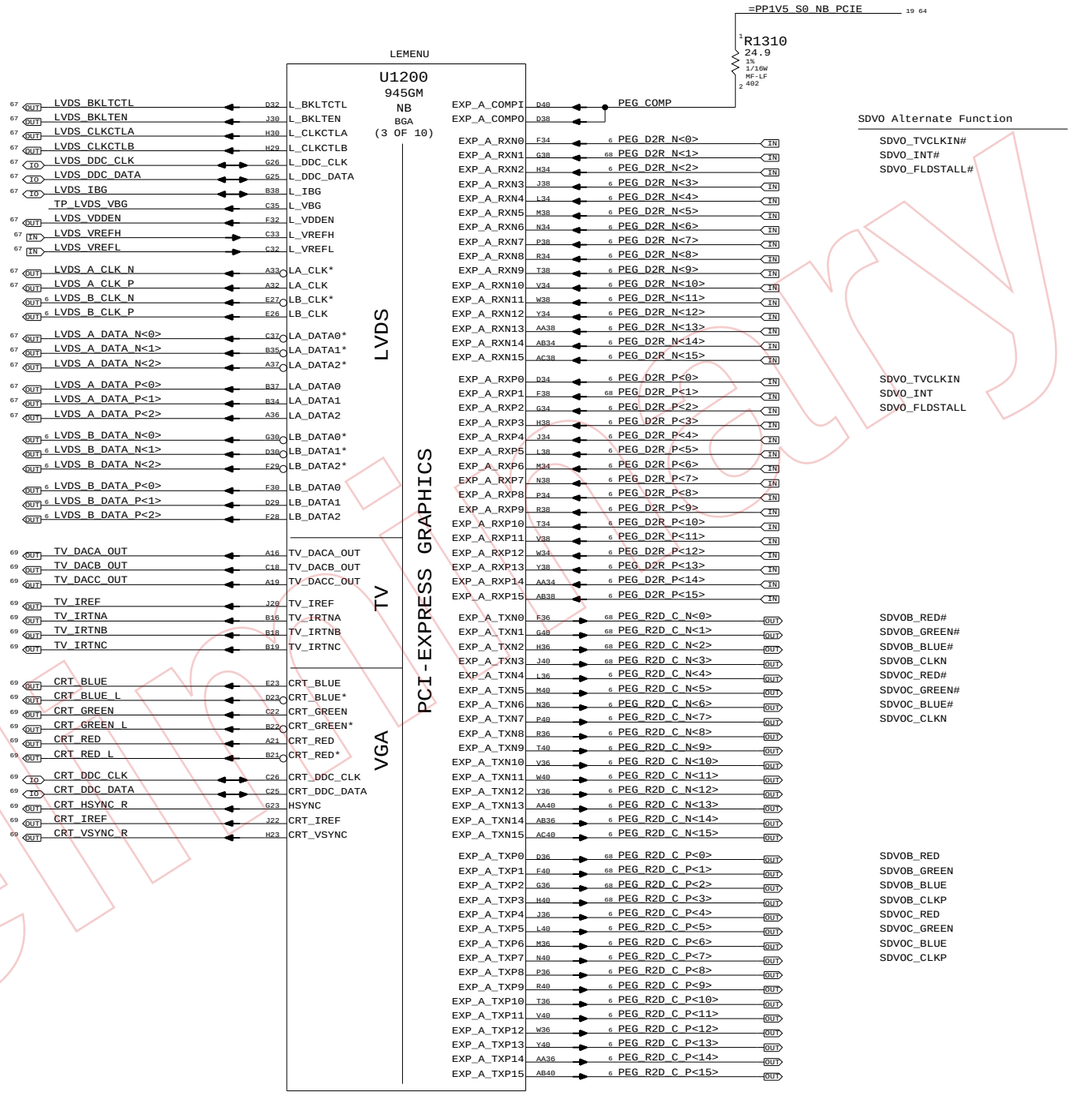
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

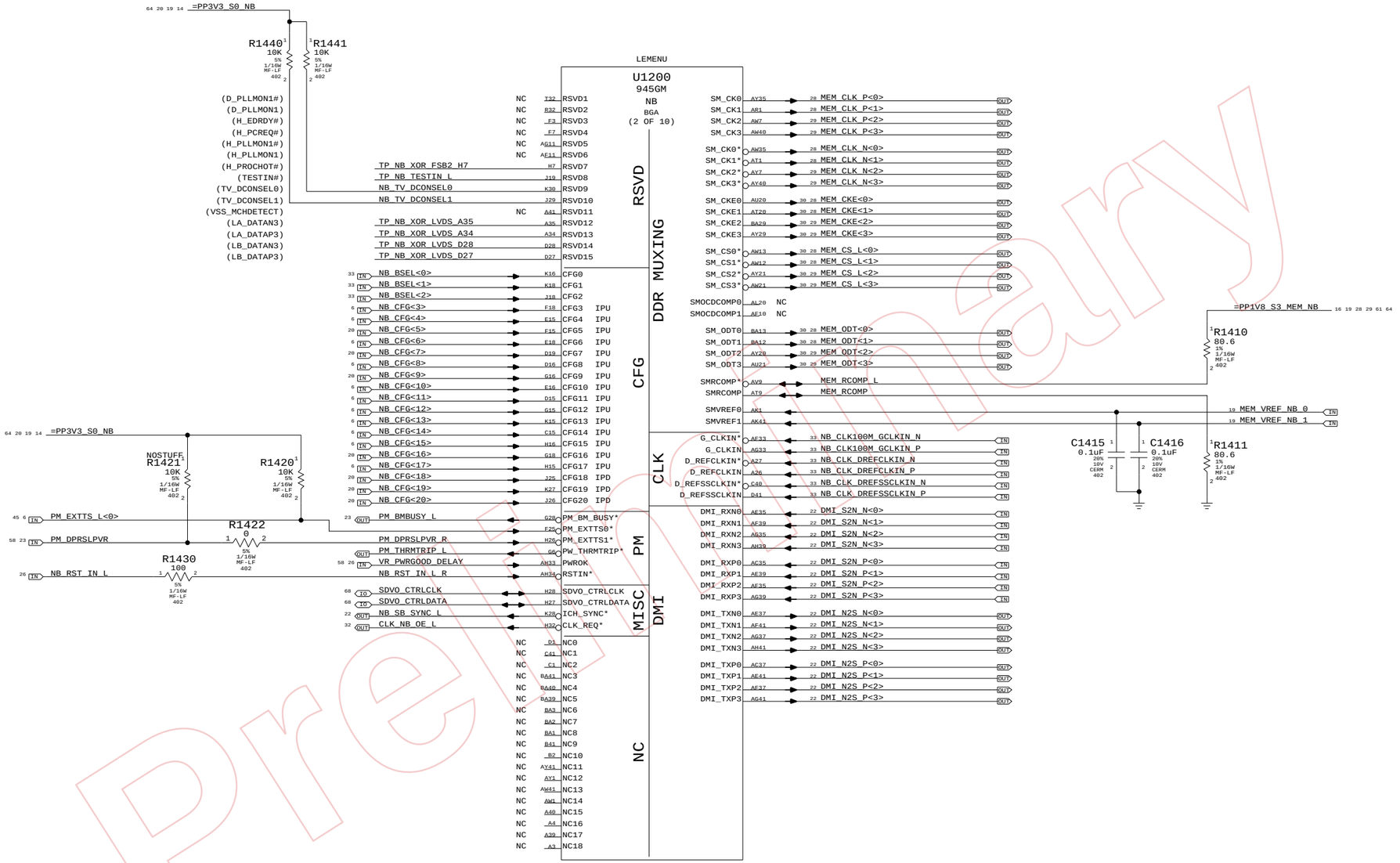


NB PEG / Video Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 13 OF 108	

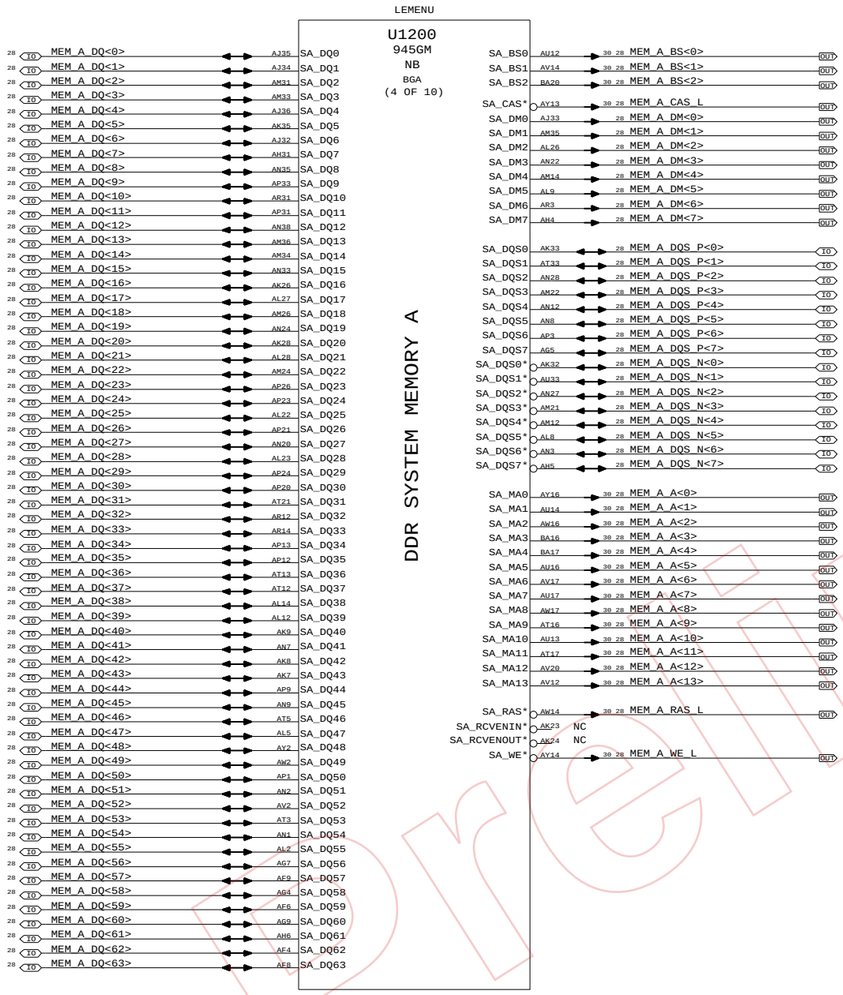


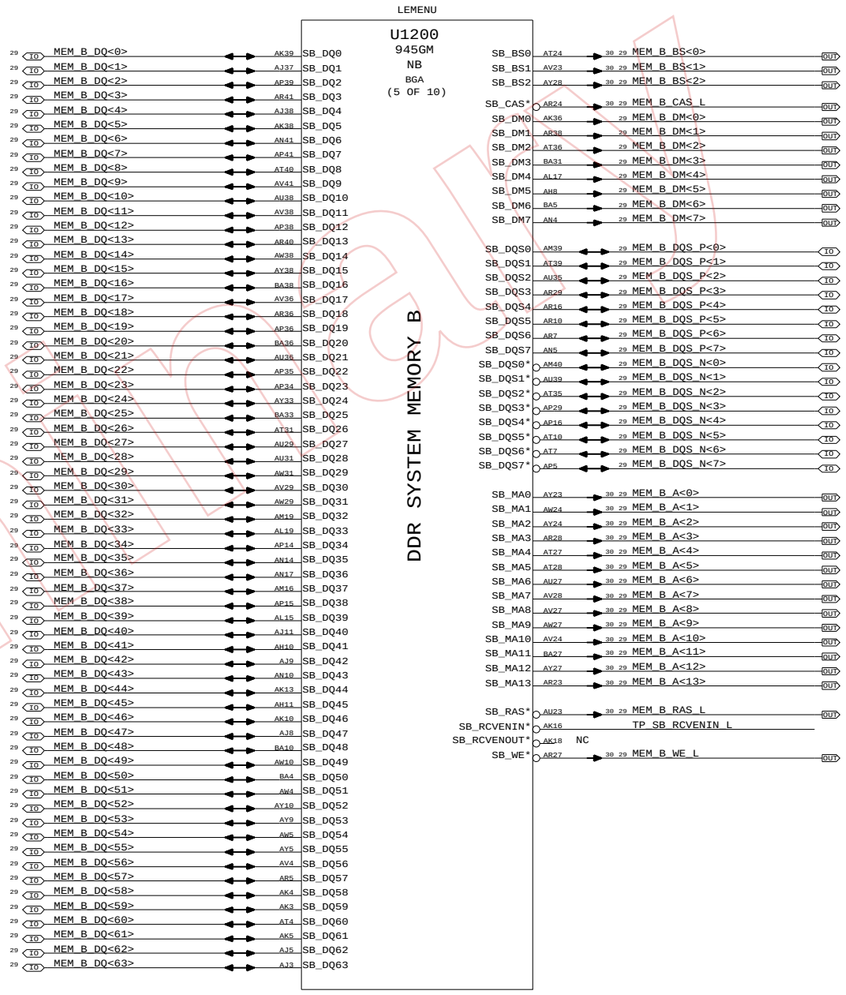
NB Misc Interfaces

SYNC_MASTER=NB SYNC_DATE=08/15/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 14 OF 108	





NB DDR2 Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 15 OF 108	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 16 19 64

1.05V or 1.5V

U1200 945GM NB BGA (6 OF 10) LEMENU VCC

VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98 VCC_99 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110

VCC_SM0 VCC_SM1 VCC_SM2 VCC_SM3 VCC_SM4 VCC_SM5 VCC_SM6 VCC_SM7 VCC_SM8 VCC_SM9 VCC_SM10 VCC_SM11 VCC_SM12 VCC_SM13 VCC_SM14 VCC_SM15 VCC_SM16 VCC_SM17 VCC_SM18 VCC_SM19 VCC_SM20 VCC_SM21 VCC_SM22 VCC_SM23 VCC_SM24 VCC_SM25 VCC_SM26 VCC_SM27 VCC_SM28 VCC_SM29 VCC_SM30 VCC_SM31 VCC_SM32 VCC_SM33 VCC_SM34 VCC_SM35 VCC_SM36 VCC_SM37 VCC_SM38 VCC_SM39 VCC_SM40 VCC_SM41 VCC_SM42 VCC_SM43 VCC_SM44 VCC_SM45 VCC_SM46 VCC_SM47 VCC_SM48 VCC_SM49 VCC_SM50 VCC_SM51 VCC_SM52 VCC_SM53 VCC_SM54 VCC_SM55 VCC_SM56 VCC_SM57 VCC_SM58 VCC_SM59 VCC_SM60 VCC_SM61 VCC_SM62 VCC_SM63 VCC_SM64 VCC_SM65 VCC_SM66 VCC_SM67 VCC_SM68 VCC_SM69 VCC_SM70 VCC_SM71 VCC_SM72 VCC_SM73 VCC_SM74 VCC_SM75 VCC_SM76 VCC_SM77 VCC_SM78 VCC_SM79 VCC_SM80 VCC_SM81 VCC_SM82 VCC_SM83 VCC_SM84 VCC_SM85 VCC_SM86 VCC_SM87 VCC_SM88 VCC_SM89 VCC_SM90 VCC_SM91 VCC_SM92 VCC_SM93 VCC_SM94 VCC_SM95 VCC_SM96 VCC_SM97 VCC_SM98 VCC_SM99 VCC_SM100 VCC_SM101 VCC_SM102 VCC_SM103 VCC_SM104 VCC_SM105 VCC_SM106 VCC_SM107

NB_VCCSM_LF4

NB_VCCSM_LF5

C1614 0.47UF 10% 6.3V CERM-X5R 402

C1613 0.47UF 10% 6.3V CERM-X5R 402

C1615 0.47UF 10% 6.3V CERM-X5R 402 61 29 28 19 14 64 =PP1V8_S3_MEM_NB

Layout Note: Place near pin BA23

C1620 10uF 20% 6.3V X5R 603

C1621 10uF 20% 6.3V X5R 603

C1610 0.47UF 10% 6.3V CERM-X5R 402

Layout Note: Place near pin BA15

Layout Note: Place in cavity (Need to better define cavity)

NB_VCCSM_LF2

NB_VCCSM_LF1

C1612 0.47UF 10% 6.3V CERM-X5R 402

C1611 0.47UF 10% 6.3V CERM-X5R 402

64 19 16 =PPVCORE_S0_NB

U1200 945GM NB BGA (7 OF 10) LEMENU NCTF

VCC_NCTF0 VCC_NCTF1 VCC_NCTF2 VCC_NCTF3 VCC_NCTF4 VCC_NCTF5 VCC_NCTF6 VCC_NCTF7 VCC_NCTF8 VCC_NCTF9 VCC_NCTF10 VCC_NCTF11 VCC_NCTF12 VCC_NCTF13 VCC_NCTF14 VCC_NCTF15 VCC_NCTF16 VCC_NCTF17 VCC_NCTF18 VCC_NCTF19 VCC_NCTF20 VCC_NCTF21 VCC_NCTF22 VCC_NCTF23 VCC_NCTF24 VCC_NCTF25 VCC_NCTF26 VCC_NCTF27 VCC_NCTF28 VCC_NCTF29 VCC_NCTF30 VCC_NCTF31 VCC_NCTF32 VCC_NCTF33 VCC_NCTF34 VCC_NCTF35 VCC_NCTF36 VCC_NCTF37 VCC_NCTF38 VCC_NCTF39 VCC_NCTF40 VCC_NCTF41 VCC_NCTF42 VCC_NCTF43 VCC_NCTF44 VCC_NCTF45 VCC_NCTF46 VCC_NCTF47 VCC_NCTF48 VCC_NCTF49 VCC_NCTF50 VCC_NCTF51 VCC_NCTF52 VCC_NCTF53 VCC_NCTF54 VCC_NCTF55 VCC_NCTF56 VCC_NCTF57 VCC_NCTF58 VCC_NCTF59 VCC_NCTF60 VCC_NCTF61 VCC_NCTF62 VCC_NCTF63 VCC_NCTF64 VCC_NCTF65 VCC_NCTF66 VCC_NCTF67 VCC_NCTF68 VCC_NCTF69 VCC_NCTF70 VCC_NCTF71 VCC_NCTF72

VSS_NCTF0 VSS_NCTF1 VSS_NCTF2 VSS_NCTF3 VSS_NCTF4 VSS_NCTF5 VSS_NCTF6 VSS_NCTF7 VSS_NCTF8 VSS_NCTF9 VSS_NCTF10 VSS_NCTF11 VSS_NCTF12

=PP1V5_S0_NB_VCCAUX 17 19 64

VCCAUX_NCTF0 VCCAUX_NCTF1 VCCAUX_NCTF2 VCCAUX_NCTF3 VCCAUX_NCTF4 VCCAUX_NCTF5 VCCAUX_NCTF6 VCCAUX_NCTF7 VCCAUX_NCTF8 VCCAUX_NCTF9 VCCAUX_NCTF10 VCCAUX_NCTF11 VCCAUX_NCTF12 VCCAUX_NCTF13 VCCAUX_NCTF14 VCCAUX_NCTF15 VCCAUX_NCTF16 VCCAUX_NCTF17 VCCAUX_NCTF18 VCCAUX_NCTF19 VCCAUX_NCTF20 VCCAUX_NCTF21 VCCAUX_NCTF22 VCCAUX_NCTF23 VCCAUX_NCTF24 VCCAUX_NCTF25 VCCAUX_NCTF26 VCCAUX_NCTF27 VCCAUX_NCTF28 VCCAUX_NCTF29 VCCAUX_NCTF30 VCCAUX_NCTF31 VCCAUX_NCTF32 VCCAUX_NCTF33 VCCAUX_NCTF34 VCCAUX_NCTF35 VCCAUX_NCTF36 VCCAUX_NCTF37 VCCAUX_NCTF38 VCCAUX_NCTF39 VCCAUX_NCTF40 VCCAUX_NCTF41 VCCAUX_NCTF42 VCCAUX_NCTF43 VCCAUX_NCTF44 VCCAUX_NCTF45 VCCAUX_NCTF46 VCCAUX_NCTF47 VCCAUX_NCTF48 VCCAUX_NCTF49 VCCAUX_NCTF50 VCCAUX_NCTF51 VCCAUX_NCTF52 VCCAUX_NCTF53 VCCAUX_NCTF54 VCCAUX_NCTF55 VCCAUX_NCTF56 VCCAUX_NCTF57

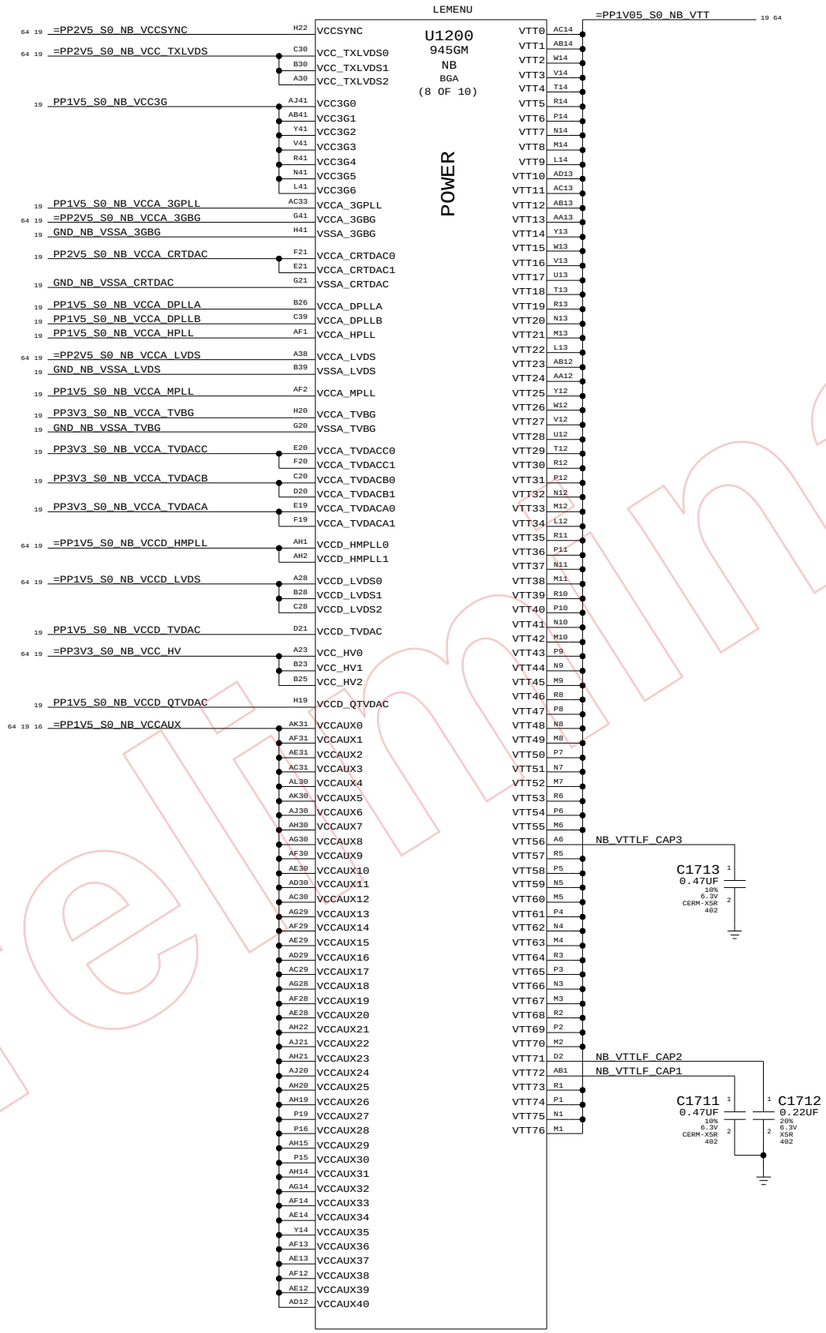
NB Power 1

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	16	108



NB Power 2

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 17 OF 108	

LEMENU

U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

LEMENU

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 18 OF 108	

Power Interface

These are the power signals that leave the NB "block"

IN =PP1V05_S0_FSB_NB 12 33 64
IN =PPVCORE_S0_NB 16 19 64
IN =PP1V05_S0_NB 19 64
IN =PP1V05_S0_NB_VTT 17 19 64
IN =PP1V5_S0_NB 19 64
IN =PP1V5_S0_NB_PCIE 13 64
IN =PP1V5_S0_NB_PLL 19 64
IN =PP1V5_S0_NB_TVDAC 19 64
IN =PP1V5_S0_NB_VCCD_HMPLL 17 64
IN =PP1V5_S0_NB_VCCD_LVDS 17 19 64
IN =PP1V5_S0_NB_VCCAUX 16 17 19 64
IN =PP1V8_S3_MEM_NB 14 16 28 29 61 64
IN =PP2V5_S0_NB_CRTDAC 19 64
IN =PP2V5_S0_NB_VCCSYNC 17 19 64
IN =PP2V5_S0_NB_VCC_TXLVDS 17 19 64
IN =PP2V5_S0_NB_VCCA_3GBG 17 19 64
IN =PP2V5_S0_NB_VCCA_LVDS 17 19 64
IN =PP3V3_S0_NB 14 20 64
IN =PP3V3_S0_NB_VCC_HV 17 19 64
IN =PP5V_S0_NB_TVDAC 19 64

MCH DISPLAY PLL POWER LDO

64 =PP2V5_S0_NB_DISP_PLL
CRITICAL
U1900
TPS73115
SOT23-5
IN OUT → PP1V5_S0_DPLL
EN NR/FB → TPS73115_NR
GND
C1950 1UF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603

R1950 0 5% 1/10W MF-LF 402 → PP1V5_S0_NB_VCCA_DPLLA
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1953 0.1uF 20% 10V CERM 402

MCH VCCA_DPLLA FILTER
(MCH DISPLAY A PLL 1.5V PWR)

R1951 0 5% 1/10W MF-LF 402 → PP1V5_S0_NB_VCCA_DPLLB
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1954 0.1uF 20% 10V CERM 402

GMCH VCCA_DPLL_B FILTER
(MCH DISPLAY B PLL 1.5V PWR)

Layout Note:
THESE 4 0.1UF CAPS SHOULD
be within 5 mm of NB edge

MCH VCCA_LVDS FILTER
(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS 17 19 64
C1980 0.1uF 20% 10V CERM 402
C1981 0.01uF 10% 16V CERM 402
GND_NB_VSSA_LVDS 17

Layout Note:
This 0.1uF cap should
be within 5 mm of NB edge

Layout Note: Route to caps, then GND

64 19 =PP2V5_S0_NB_CRTDAC
R1985 10 1% 1/16W MF-LF 402 → PP2V5_S0_NB_CRTDAC_FOLLOW
VOLTAGE=2.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363 =PP1V05_S0_NB 19 64
L1985 180-OHM-1.5A 0603 → PP2V5_S0_NB_CRTDAC_F
C1986 22000pF-1000mA 16V NFM18

MCH VCCA_CRTDAC BYPASS
(MCH CRTDAC ANALOG 2.5V PWR)
PP2V5_S0_NB_VCCA_CRTDAC 17
VOLTAGE=2.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1985 0.1uF 20% 10V CERM 402
GND_NB_VSSA_CRTDAC 17

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

Layout Note: Route to caps, then GND

64 19 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603
C1934 22UF 20% 6.3V CERM-X5R 805 CRITICAL
C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm

L1936 FERR-120-OHM-0.2A 0603
C1936 22UF 20% 6.3V CERM-X5R 805 CRITICAL
C1937 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm

64 19 =PP5V_S0_NB_TVDAC
CRITICAL
U1901
MM157
SOT23-5_LF
VIN VOUT → PP3V3_S0_NB_TVDAC
CONT NOISE → MM1573DN_NR
GND
C1940 1UF 10% 6.3V CERM 402
C1941 0.01uF 10% 16V CERM 402
C1942 1UF 10% 6.3V CERM 402

R1990 10 1% 1/16W MF-LF 402 → PP3V3_S0_NB_TVDAC_FOLLOW
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363 =PP1V5_S0_NB 19 64
L1990 180-OHM-1.5A 0603 → PP3V3_S0_NB_TVDAC_F
C1992 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1990 10uF 20% 6.3V X5R 603
C1991 0.1uF 20% 10V CERM 402

C1994 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1993 0.1uF 20% 10V CERM 402

Layout Note:
These 8 caps should be
within 6.35 mm of NB edge

C1996 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1995 0.1uF 20% 10V CERM 402

C1998 22000pF-1000mA 16V NFM18

MCH VCCA_TVBG FILTER
(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG 17
VOLTAGE=3.3V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1997 0.1uF 20% 10V CERM 402
GND_NB_VSSA_TVBG 17

Layout Note: Route to caps, then GND

GMCH CORE PWR 1.05V BYPASS
THIS 470UF FOR GMCH CORE 1.05V

64 19 16 =PPVCORE_S0_NB
CRITICAL
C1900 470UF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

GMCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)

64 19 17 =PP1V5_S0_NB_VCCD_LVDS
C1910 10uF 20% 6.3V X5R 603
C1911 0.1uF 20% 10V CERM 402

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

64 19 17 =PP3V3_S0_NB_VCC_HV
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

MCH VCCSYNC BYPASS
(MCH H/V SYNC 2.5V PWR)

64 19 17 =PP2V5_S0_NB_VCCSYNC
C1917 0.1uF 20% 10V CERM 402

945 EDS: 5 mOhm, 1nH (1210?)

GMCH VCCTX_LVDS BYPASS
(MCH LVDS DATA/CLK TX 2.5V PWR)

64 19 17 =PP2V5_S0_NB_VCC_TXLVDS
C1912 4.7uF 20% 6.3V CERM 603
C1913 0.1uF 20% 10V CERM 402

945 EDS: 1210?

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

64 19 17 =PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER
(MCH_DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

64 19 17 16 =PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402

64 29 28 19 =PP1V8_S3_MEM

PLACE THOSE COMPONENT
CLOSE TO GMCH

R1988 1K 1% 1/16W MF-LF 402 → MEM_VREF_NB_0 14
VOLTAGE=0.9V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
R1989 1K 1% 1/16W MF-LF 402

64 29 28 19 =PP1V8_S3_MEM
R1986 1K 1% 1/16W MF-LF 402 → MEM_VREF_NB_1 14
VOLTAGE=0.9V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
R1987 1K 1% 1/16W MF-LF 402

64 19 =PP1V5_S0_NB_TVDAC
C1921 22000pF-1000mA 16V NFM18

GMCH VCCD_TVDAC FILTER
(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1920 0.1uF 20% 10V CERM 402

Layout Note:
These 4 caps should be
within 6.35 mm of NB edge

L1922 180-OHM-1.5A 0603 → PP1V5_S0_NB_QTVDAC
C1923 22000pF-1000mA 16V NFM18

GMCH VCCD_QTVDAC FILTER
(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1922 0.1uF 20% 10V CERM 402

MCH VTT BYPASS
(MCH FSB 1.05V PWR) (SHARE C0940 470UF)

64 19 17 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603

Layout Note:
Place in cavity

C1967 0.22uF 20% 6.3V X5R 402

Layout Note:
Place on the edge

91NH, 20%, 20MOHM, 1.5A (1210 TYP)
CRITICAL
L1970 91nH 1210
C1970 220UF 20% 2.5V POLY SMB2

Layout Note:
Place L and C
close to MCH

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)

PP1V5_S0_NB_VCC3G 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1971 10uF 20% 6.3V 603
C1972 10uF 20% 6.3V X5R 603

Layout Note:
10uF caps should
be close to MCH
on opposite side.

1uH, 20%
L1975 1.0UH-220MA-0.12-OHM 0805
R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)

64 =PP1V5_S0_NB_3GPLL
PP1V5_S0_NB_3GPLL_F
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
PP1V5_S0_NB_VCCA_3GPLL 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=1.0 mm
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
GND_NB_VSSA_3GBG 17

Layout Note:
3GPLL 10uF cap should
be placed in cavity

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=NB SYNC_DATE=06/22/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 19 OF 108	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 64
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 64
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 64
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

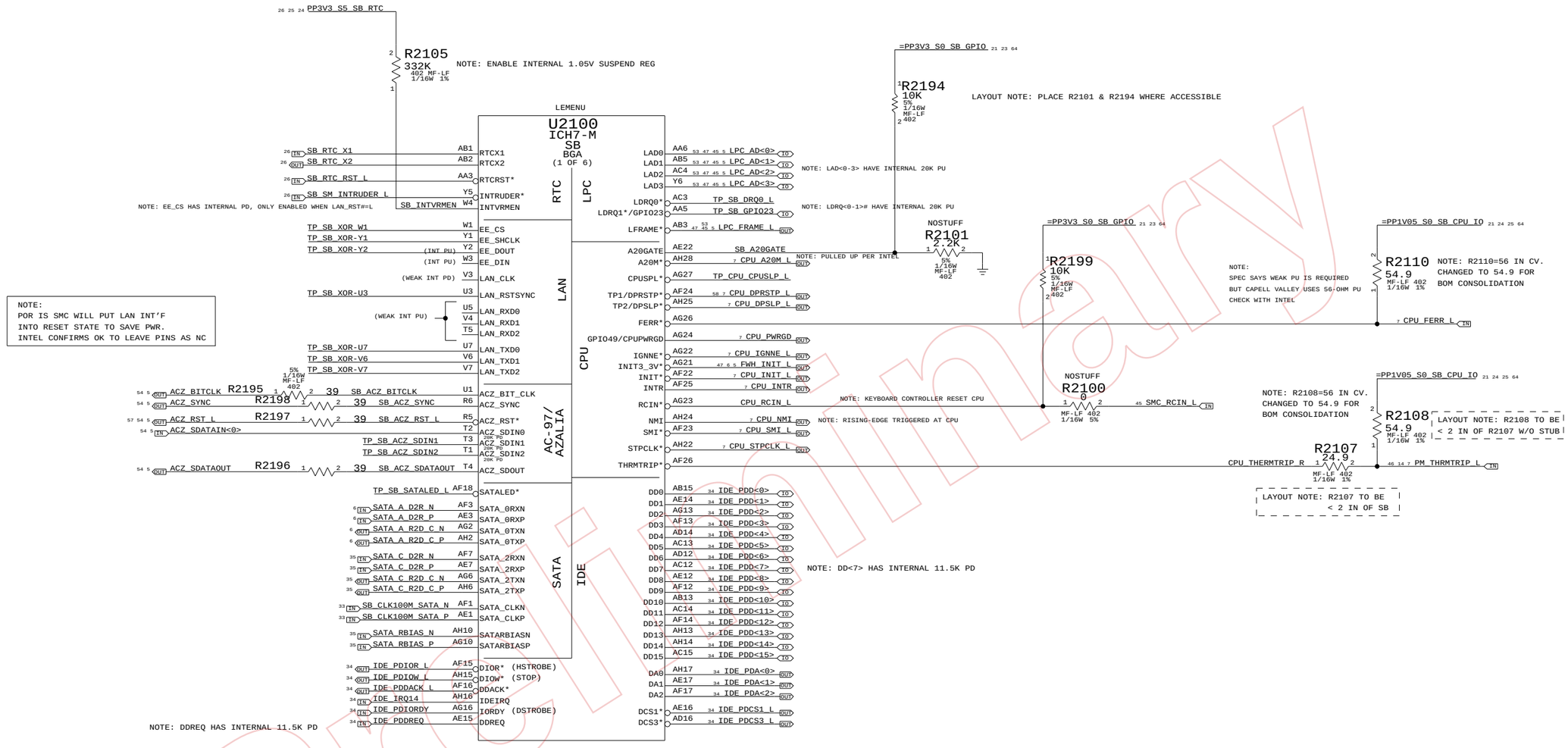
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=NB SYNC_DATE=06/28/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT: 20	OF: 108

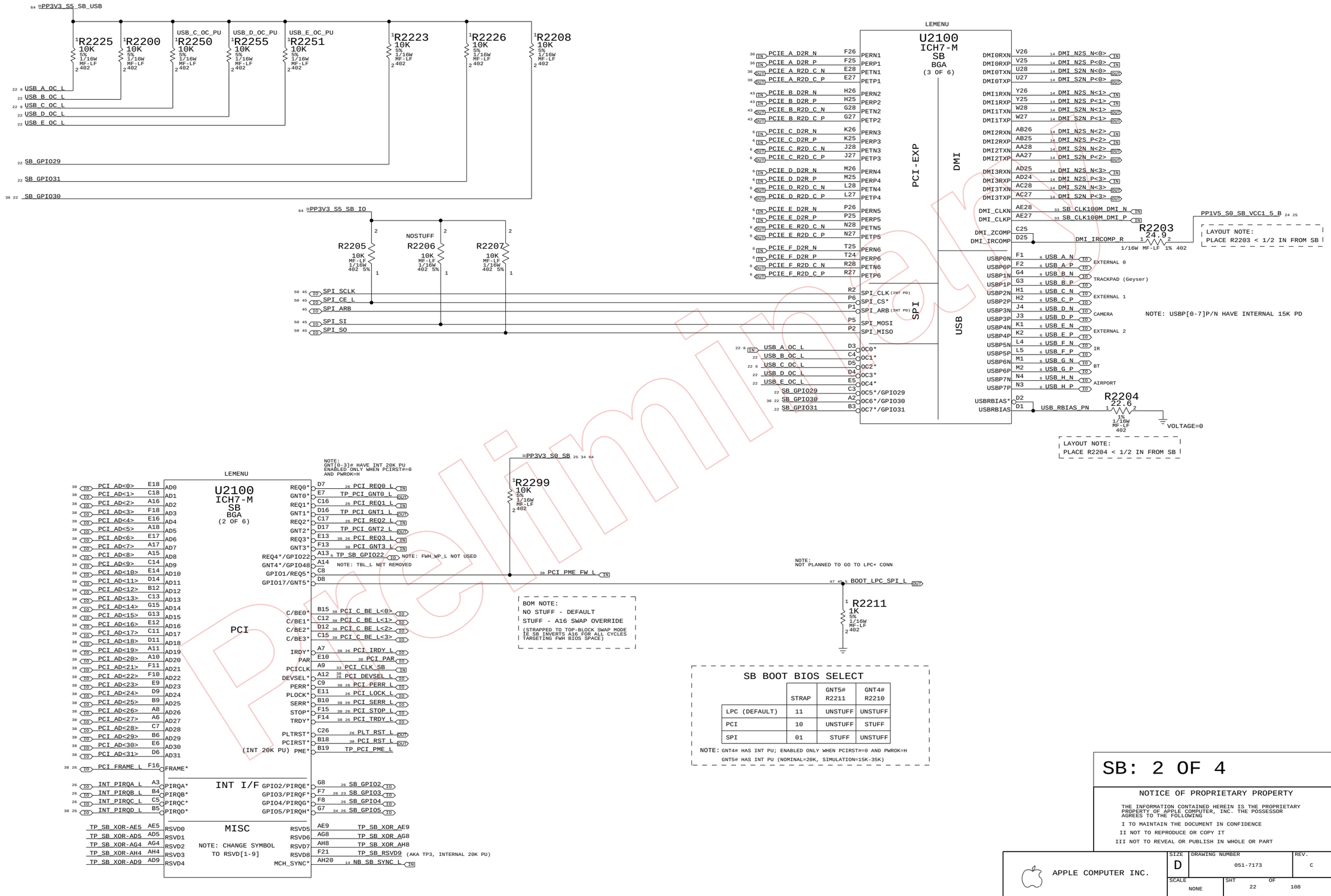


	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 21 OF 108	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
R2208 10K 5% 1/16W MF-LF 402
USB_C_OC_PU
USB_D_OC_PU
USB_E_OC_PU
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO31
SB_GPIO30
=PP3V3_S5_SB_IO
R2205 10K MF-LF 1/16W 402 5%
NOSTUFF
R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
LEMENU
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_B_D2R_N
PCIE_B_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_C_D2R_N
PCIE_C_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_D_D2R_N
PCIE_D_D2R_P
PCIE_D_R2D_C_N
PCIE_D_R2D_C_P
PCIE_E_D2R_N
PCIE_E_D2R_P
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_F_D2R_N
PCIE_F_D2R_P
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
PCI-EXP
DMI
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
R2203 24.9 1/16W MF-LF 1% 402
DMI_IRCOMP_R
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB
SPI
SPI_CLK (INT PD)
SPI_CS*
SPI_ARB (INT PD)
SPI_MOSI
SPI_MISO
USB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS*
USBRBIAS
USB_A_N
USB_A_P
USB_B_N
USB_B_P
USB_C_N
USB_C_P
USB_D_N
USB_D_P
USB_E_N
USB_E_P
USB_F_N
USB_F_P
USB_G_N
USB_G_P
USB_H_N
USB_H_P
EXTERNAL 0
TRACKPAD (Geyser)
EXTERNAL 1
CAMERA
EXTERNAL 2
IR
BT
AIRPORT
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
R2204 22.6 1% 1/16W MF-LF 402
USB_RBIAS_PN
VOLTAGE=0
LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
NOTE:
GNT[0-3]# HAVE INT 20K PU
ENABLED ONLY WHEN PCIRST#=0
AND PWROK=H
PCI
INT I/F
MISC
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME_L
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
TP_SB_XOR-AE5
TP_SB_XOR-AD5
TP_SB_XOR-AG4
TP_SB_XOR-AH4
TP_SB_XOR-AD9
NOTE: CHANGE SYMBOL
TO RSVD[1-9]
REQ0*
GNT0*
REQ1*
GNT1*
REQ2*
GNT2*
REQ3*
GNT3*
REQ4*/GPIO22
GNT4*/GPIO48
GPIO1/REQ5*
GPIO17/GNT5*
PCI_REQ0_L
TP_PCI_GNT0_L
PCI_REQ1_L
TP_PCI_GNT1_L
PCI_REQ2_L
TP_PCI_GNT2_L
PCI_REQ3_L
PCI_GNT3_L
TP_SB_GPIO22
NOTE: FWH_WP_L NOT USED
NOTE: TBL_L NET REMOVED
C/BE0*
C/BE1*
C/BE2*
C/BE3*
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
IRDY*
PAR
PCICLK
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLTRST*
PCIRST*
(INT 20K PU) PME*
PLT_RST_L
PCI_RST_L
TP_PCI_PME_L
PIRQA*
PIRQB*
PIRQC*
PIRQD*
GPIO2/PIRQE*
GPIO3/PIRQF*
GPIO4/PIRQG*
GPIO5/PIRQH*
SB_GPIO2
SB_GPIO3
SB_GPIO4
SB_GPIO5
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
MCH_SYNC*
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD9
(AKA TP3, INTERNAL 20K PU)
NB_SB_SYNC_L
=PP3V3_S0_SB
R2299 10K 5% 1/16W MF-LF 402
PCI_PME_FW_L
NOTE:
NOT PLANNED TO GO TO LPC+ CONN
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE
IE SB INVERTS A16 FOR ALL CYCLES
TARGETING FWH BIOS SPACE)
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
SB: 2 OF 4
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SIZE D
DRAWING NUMBER 051-7173
REV. C
SCALE NONE
SHT 22 OF 108

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 64

=PP3V3_S5_SB 23 25 64

64 25 23 =PP3V3_S5_SB

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

LEMENU

U2100
ICH7-M
SB
BGA
(4 OF 6)

27 IO SMB_CLK	C22	SMBCLK	SMB
27 IO SMB_DATA	B22	SMBDATA	
SMB_LINK_ALERT_L	A26	LINKALERT*	
SMLINK<0>	B25	SMLINK0	
SMLINK<1>	A25	SMLINK1	
NOT USED			
PM_RI_L	A28	RI*	
SB_SPKR	A19	SPKR (INT WEAK PD)	
53 47 46 45 5 OUT PM_SUS_STAT_L	A27	SUS_STAT*	
45 26 IN PM_SYSRST_L	A22	SYS_RST*	
14 IN PM_BMBUSY_L	AB18	GPIO0/BM_BUSY*	
SMB_ALERT_L NOTE: RESERVED FOR FUTURE	B23	GPIO11/SMBALERT*	
32 OUT PM_STPPCI_L	AC20	GPIO18/STPPCI*	
32 OUT PM_STPCPU_L	AF21	GPIO20/STPCPU*	
IN SB_GPIO26	A21	GPIO26	
23 BIOS_REC	B21	GPIO27	
23 FWH_MFG_MODE	E23	GPIO28	
53 47 45 38 5 IO PM_CLKRUN_L	AG18	GPIO32/CLKRUN*	
RESERVED FOR MOBILE AZALIA DOCKING INT'F: TP_AZ_DOCK_EN_L	AC19	GPIO33/AZ_DOCK_EN*	
TP_AZ_DOCK_RST_L	U2	GPIO34/AZ_DOCK_RST*	
43 36 IN PCIE_WAKE_L	F20	WAKE*	
53 47 45 5 IO INT_SERIRQ	AH21	SERIRQ	
45 IN PM_THRM_L	AF20	THRM*	
26 IN VR_PWRGD_CK410	AD22	VRMPWRGD	
IO TP_SB_GPIO6	AC21	GPIO6	GPIO
SB_RUNTIME_SCI_L	AC18	GPIO7	
	E21	GPIO8	

SATA GPIO

	AF19	GPIO21/SATA0GP	SB_GPIO21 100 R2302
	AH18	GPIO19/SATA1GP	SB_GPIO19 100 R2303
	AH19	GPIO36/SATA2GP	
	AE19	GPIO37/SATA3GP	SB_GPIO37 100 R2305

35 SATA_C_DET_L IN

CLKS

CLK14	AC1	33 SB_CLK14P3M_TIMER IN
CLK48	B2	33 SB_CLK48M_USBCTLR IN
SUSCLK	C20	6 SUS_CLK_SB OUT

PWR MNGT

SLP_S3*	B24	63 45 PM_SLP_S3_L OUT
SLP_S4*	D23	63 61 60 45 PM_SLP_S4_L OUT
SLP_S5*	F22	46 45 PM_SLP_S5_L OUT
PWROK	AA4	26 PM_SB_PWROK IN
GPIO16/DPRSLPVR	AC22	58 14 PM_DPRSLPVR OUT
TP0/BATLOW*	C21	NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN*	C23	45 PM_PWRBTN_L IN
LAN_RST*	C19	45 PM_LAN_ENABLE IN
RSMRST*	Y4	

NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR

SYS GPIO

GPIO9	E20	46 45 SMS_INT_L IN
GPIO10	A20	45 SMC_SB_NMI IN
DEF=GPI GPIO12	F19	23 PATA_PWR_EN_L OUT
GPIO13	E19	
DEF=GPI GPIO14	R4	23 SB_GPIO014 OUT
GPIO15	E22	SV_SET_UP 5 23 47
GPIO24	R3	CRB_SV_DET 23
GPIO25	D20	TP_SB_GPIO25_DO_NOT_USE
OD GPIO35	AD21	32 SB_CLK100M_SATA_OE_L OUT
GPIO38	AD20	TP_SB_GPIO38 IO
DEF=GPI GPIO39	AE20	23 SATA_C_PWR_EN_L OUT

NOTE: PATA_DET IS ACTUALLY CABLE TYPE DETECT

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

R2300 0
45 IN SMC_RUNTIME_SCI_L
45 IN SMC_EXTSMI_L

=PP3V3_S5_SB_PM 11 26 64

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

45 PM_BATLOW_L IN
45 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
45 SMC_WAKE_SCI_L IN

64 25 23 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 5 23 47
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

64 25 23 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S0_SB_GPIO 21 23 64

R2390 10K 5% 1/16W MF-LF 402
R2388 10K 5% 1/16W MF-LF 402

23 PATA_PWR_EN_L
23 SATA_C_PWR_EN_L

NOSTUFF R2312 0 5% 1/16W MF-LF 402
26 22 SB_GPIO3
IDE_RESET_L 34

R2315 0 5% 1/16W MF-LF 402
23 SB_GPIO14

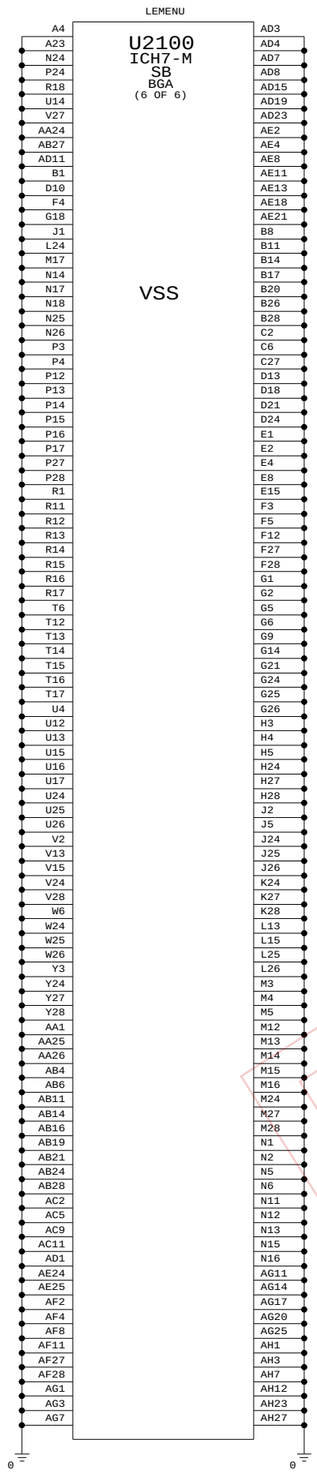
R2389 15K 5% 1/10W MF-LF 402

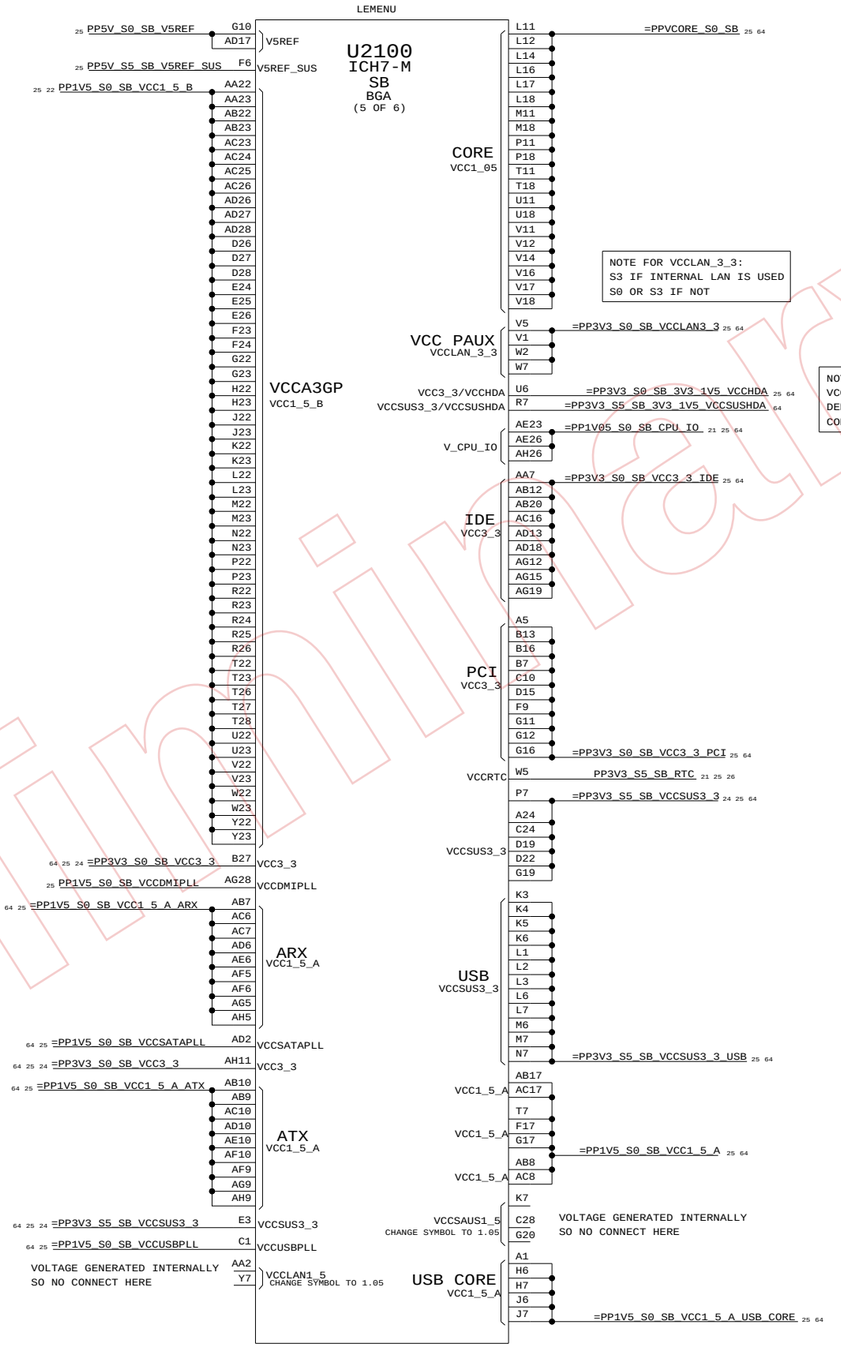
R2312,R2315 and R2389 close to SB

SB: 3 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 23 OF 108	

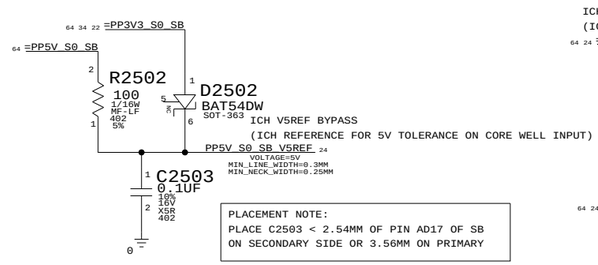


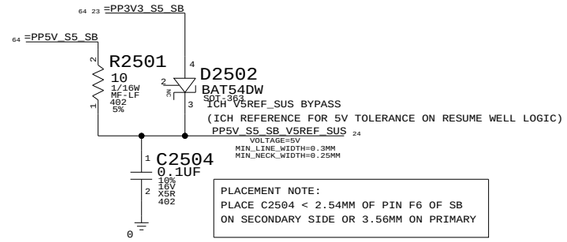


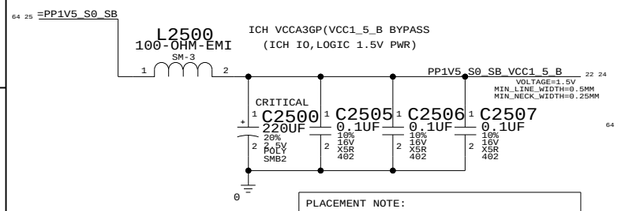
SB: 4 OF 4

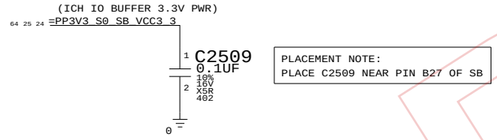
APPLE COMPUTER INC.

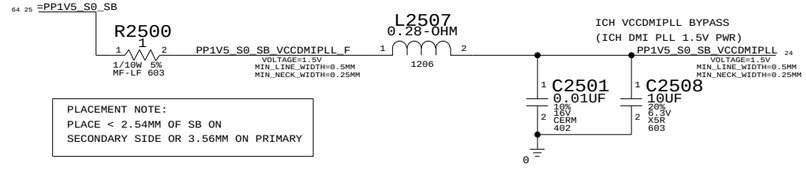
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 24 OF 108	

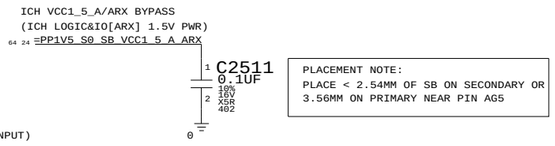


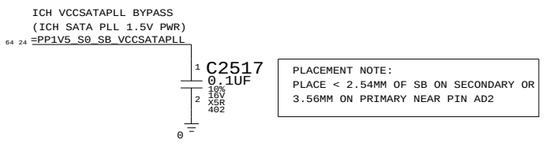


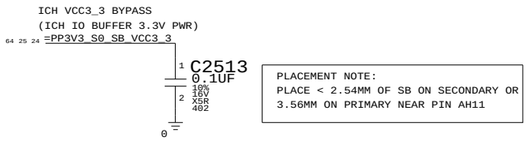


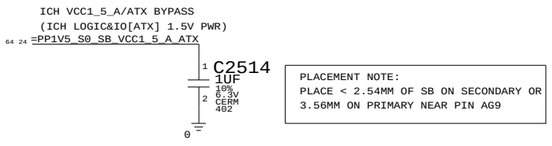


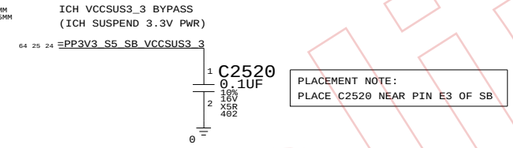


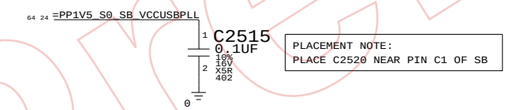


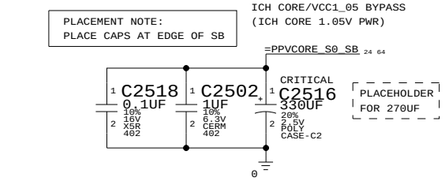


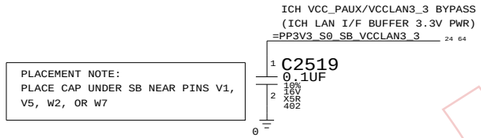


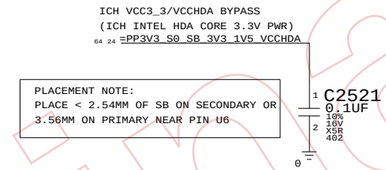


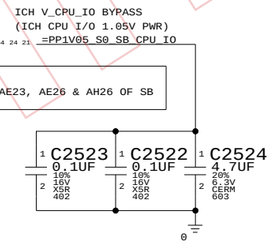


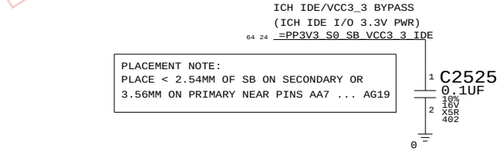


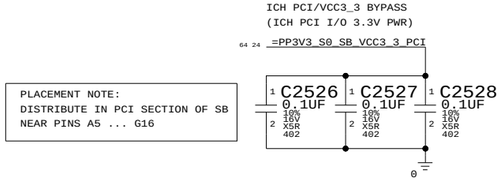


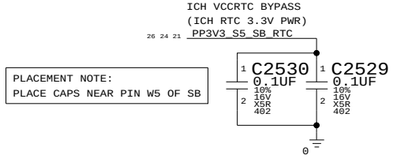


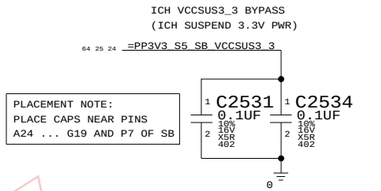


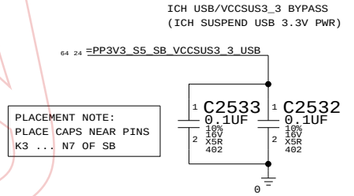


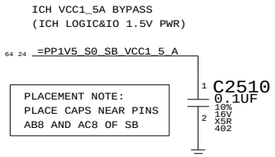


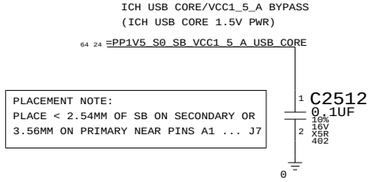












SB: 4 OF 4

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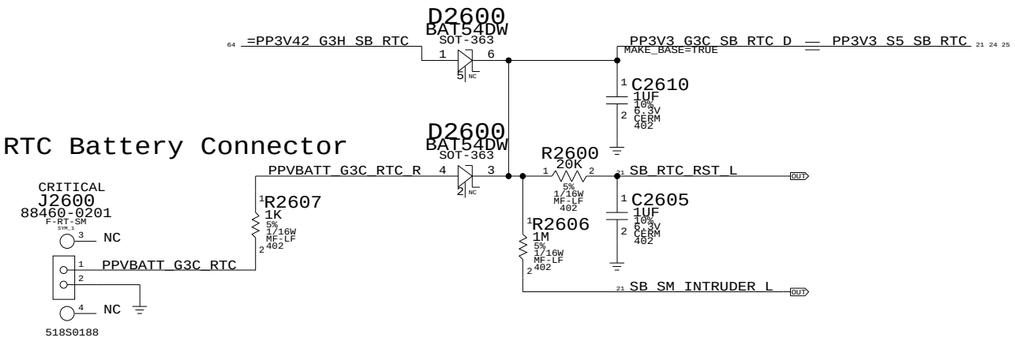
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

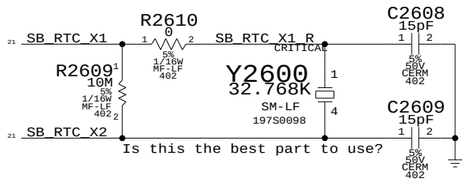
SIZE	DRAWING NUMBER	REV.
D	051-7173	C

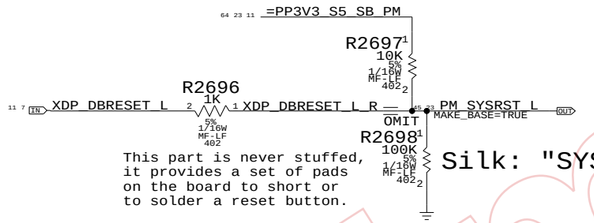
SCALE	SHT	OF
NONE	25	108

RTC Battery Connector



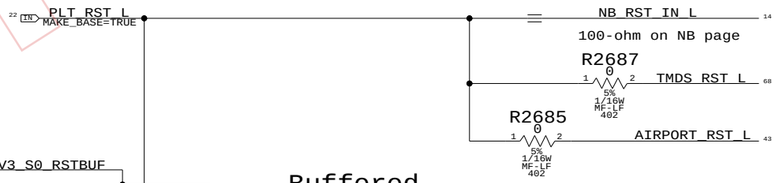
SB RTC Crystal Circuit



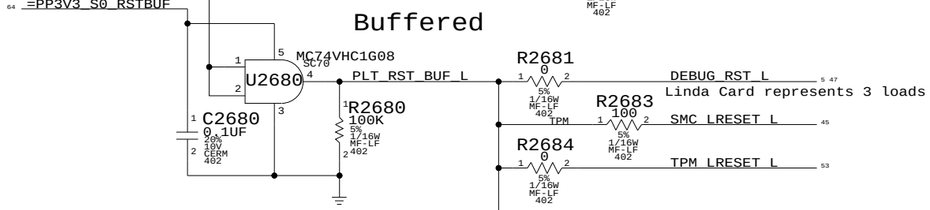


Platform Reset Connections

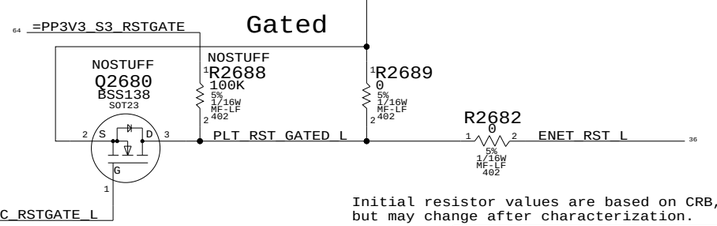
Unbuffered



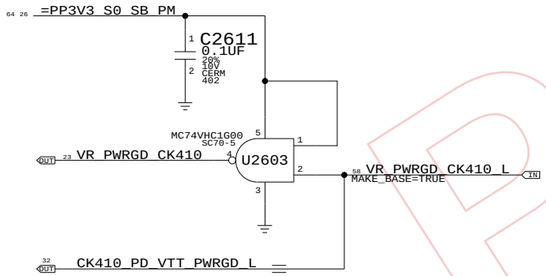
Buffered

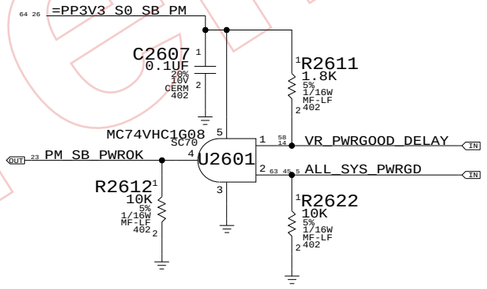


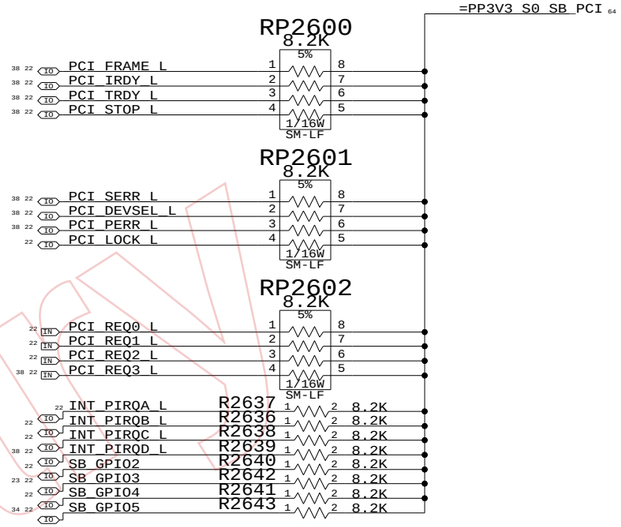
Gated



Initial resistor values are based on CRB,
but may change after characterization.







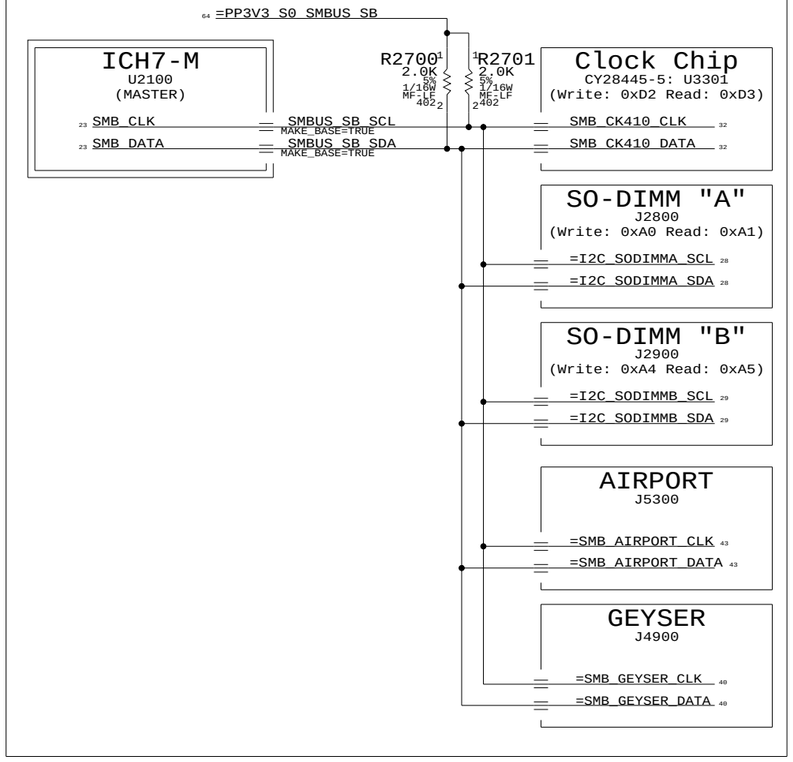
SB Misc

SYNC_MASTER=NB SYNC_DATE=07/26/2005

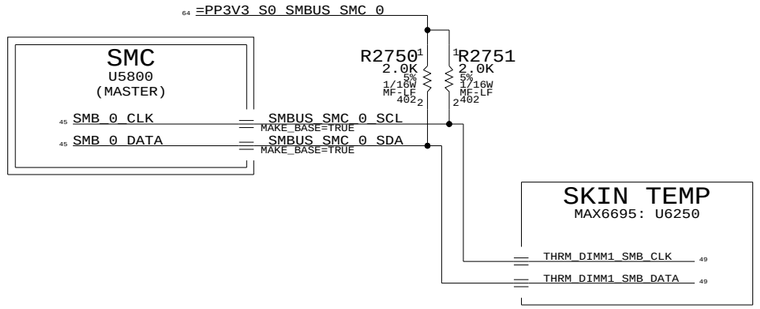
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 26 OF 108	

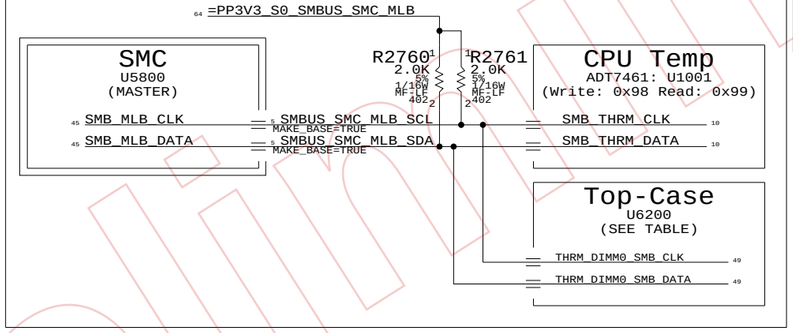
ICH7-M SMBus Connections



SMC "0" SMBus Connections

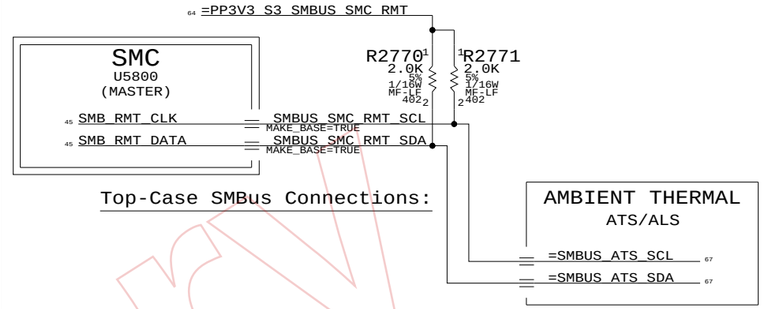


SMC "MLB" SMBus Connections

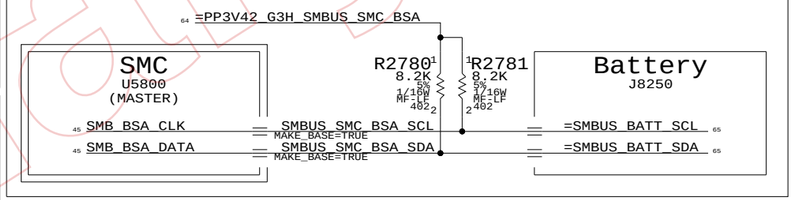


SMC "RMT" SMBus Connections

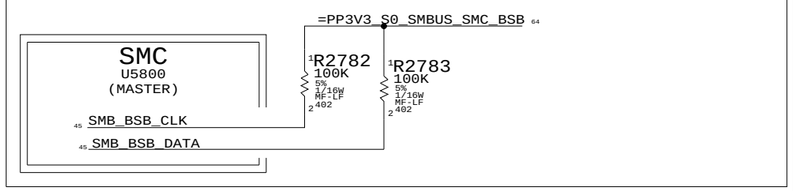
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections

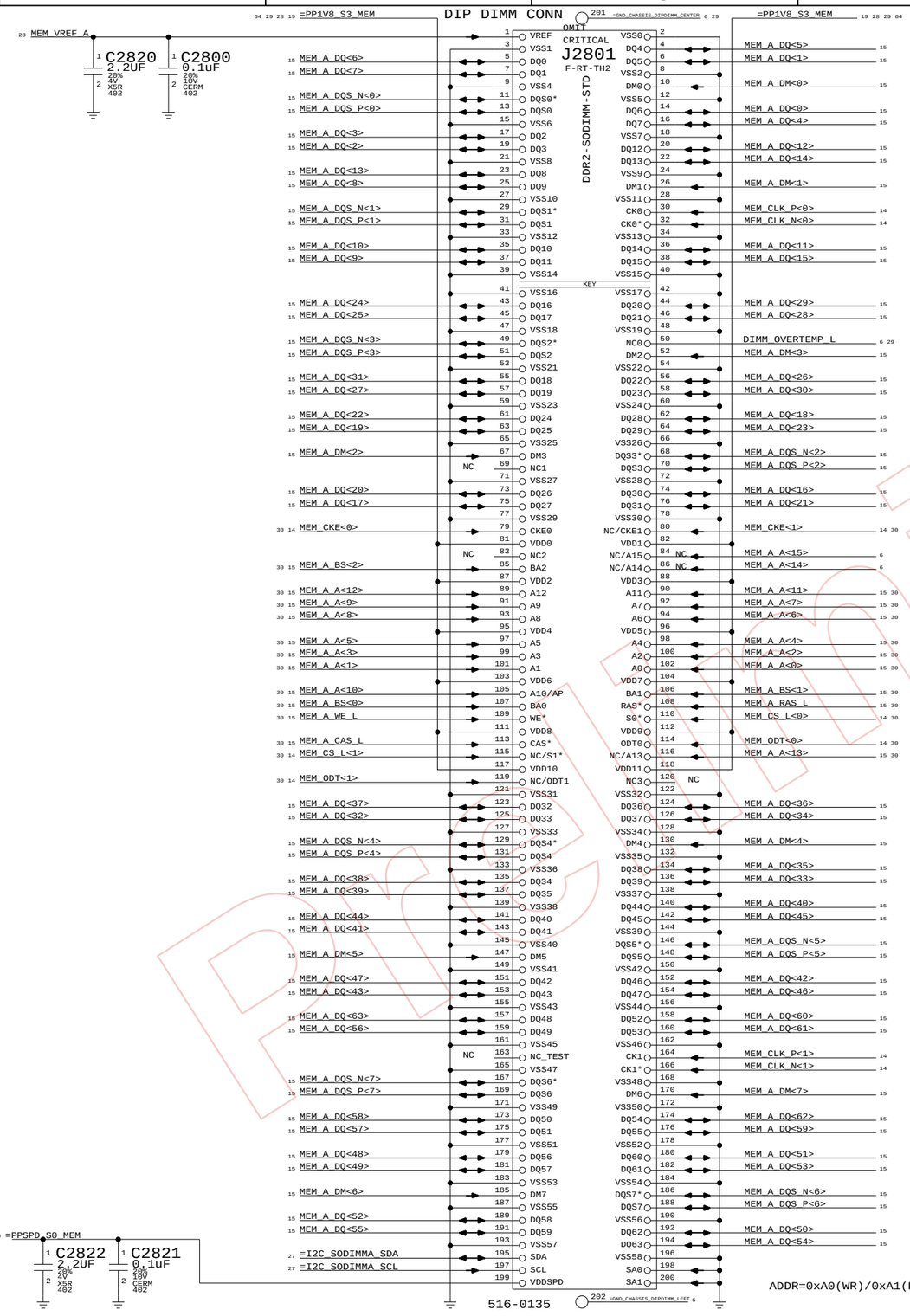


M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

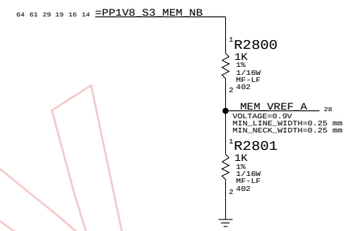
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 27 OF 108	



DDR2 VRef

One 0.1uF per connector



Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

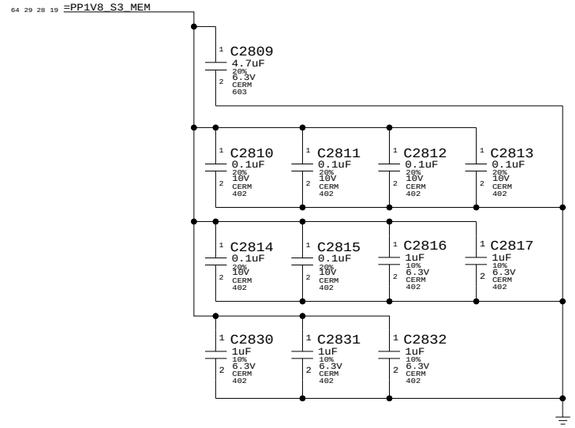
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

DDR2 SO-DIMM Connector A

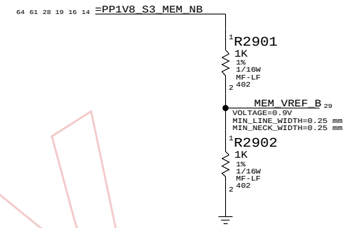
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 28 OF 108	

DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector



Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

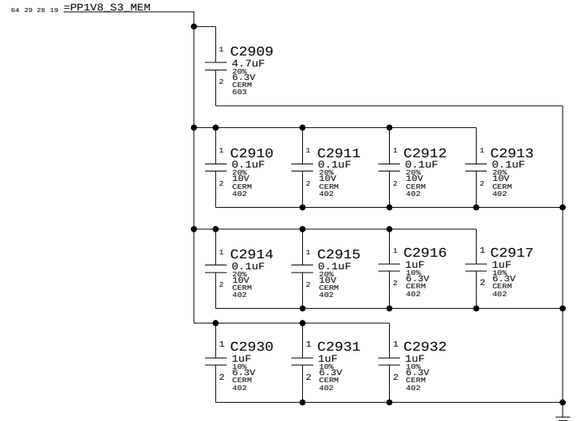
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2901	CRITICAL	POST-RAMP-DIMM35

Resistor prevents pwr-gnd short

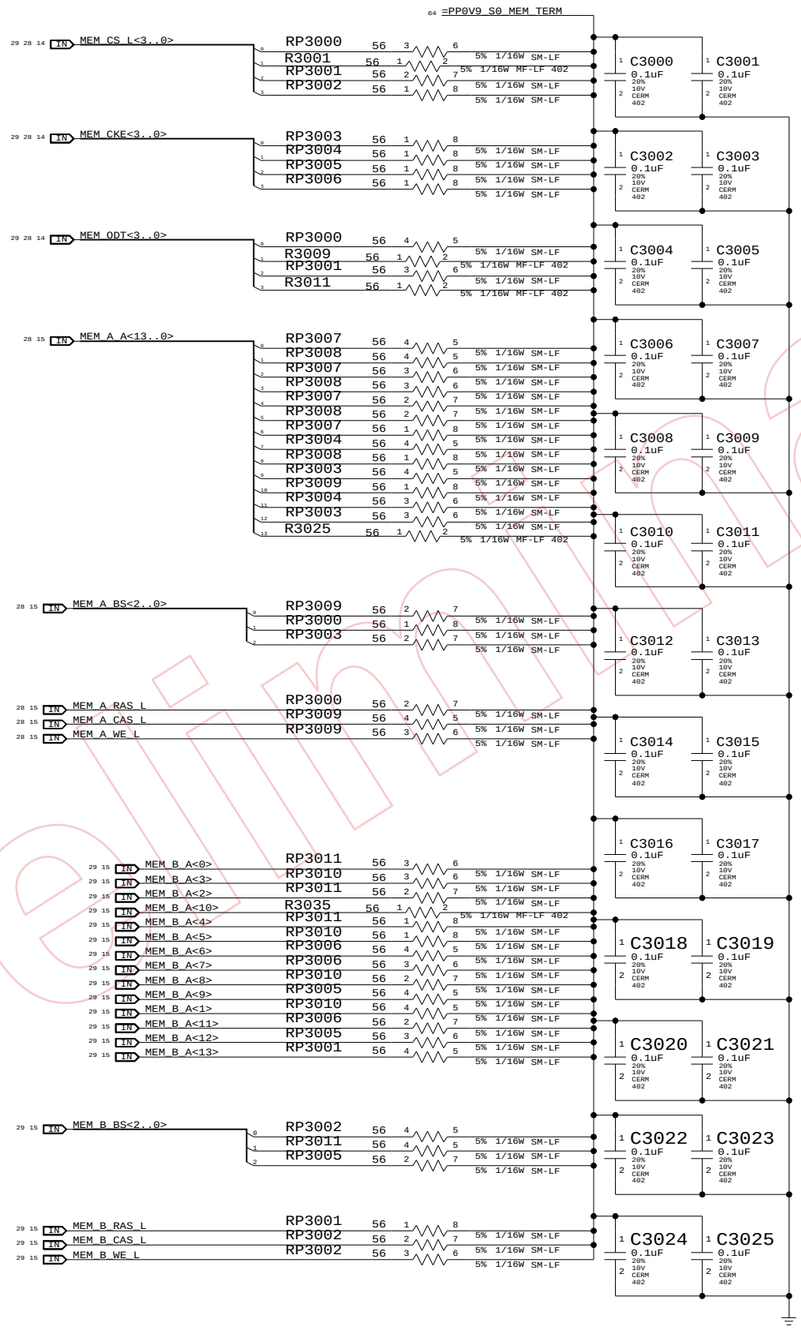
DDR2 SO-DIMM Connector B

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 29 OF 108	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE	SHT	OF
NONE	30	108

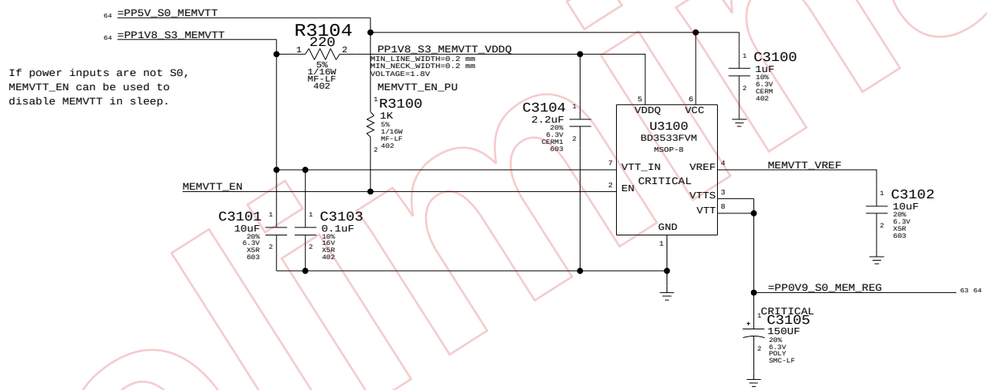
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



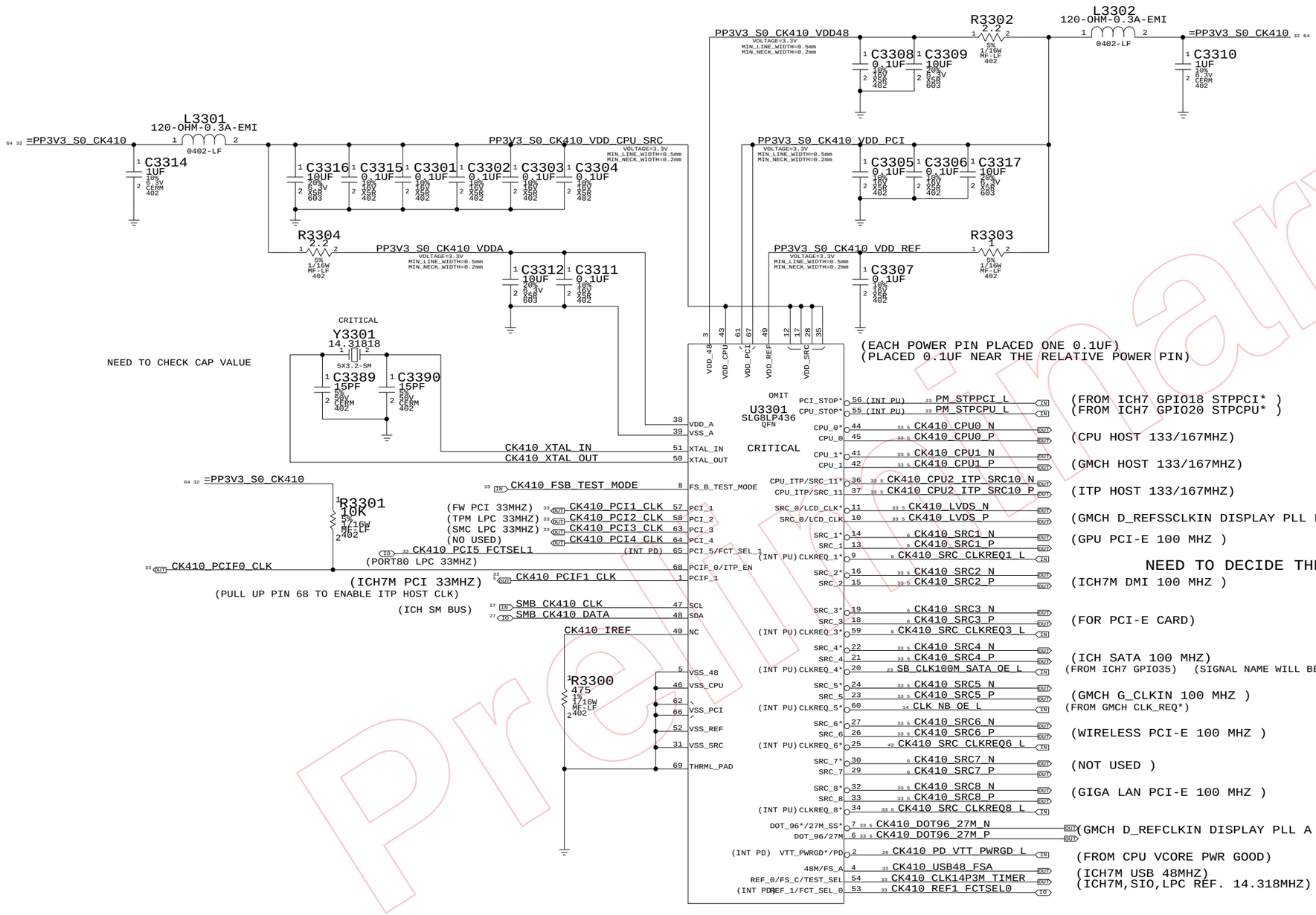
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	31	108



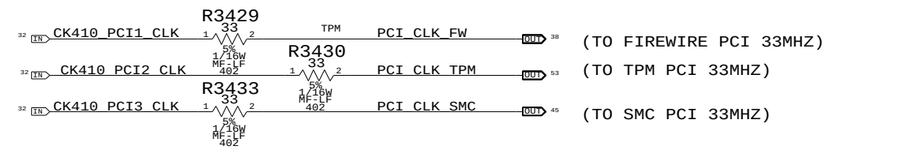
FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

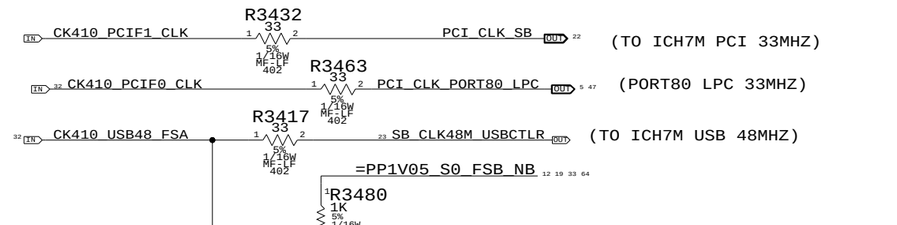
CLOCKS

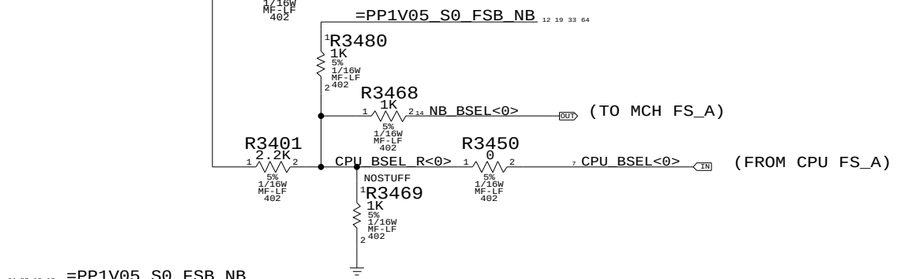
SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

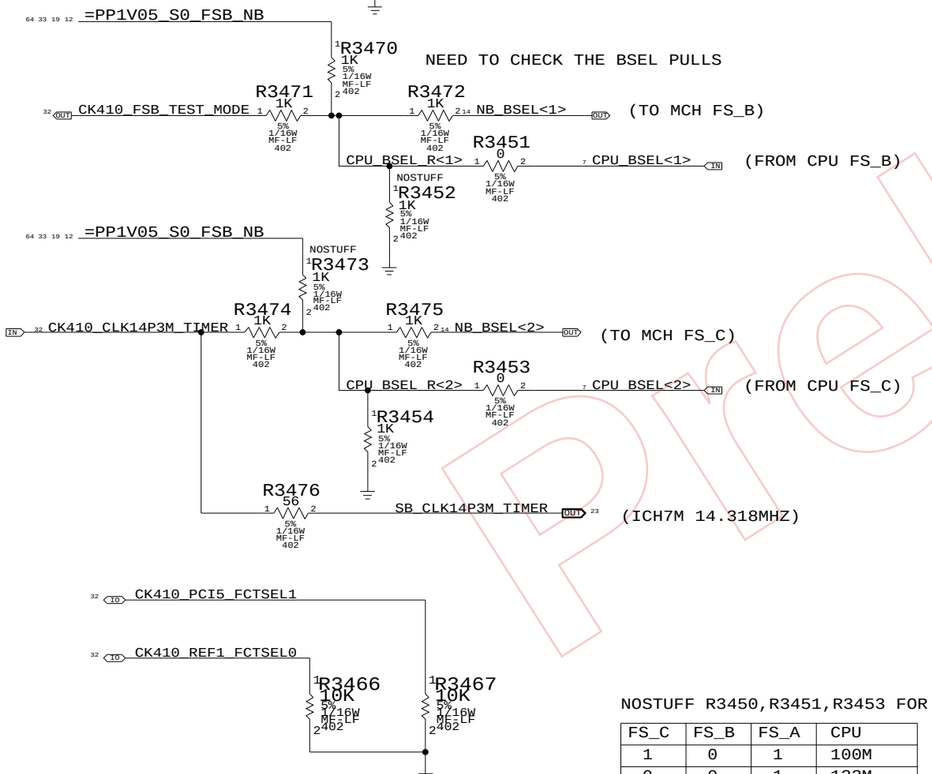
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 33 OF 108	







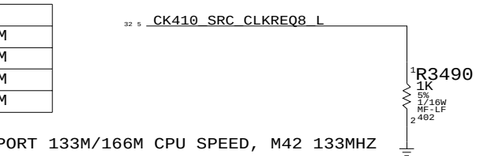


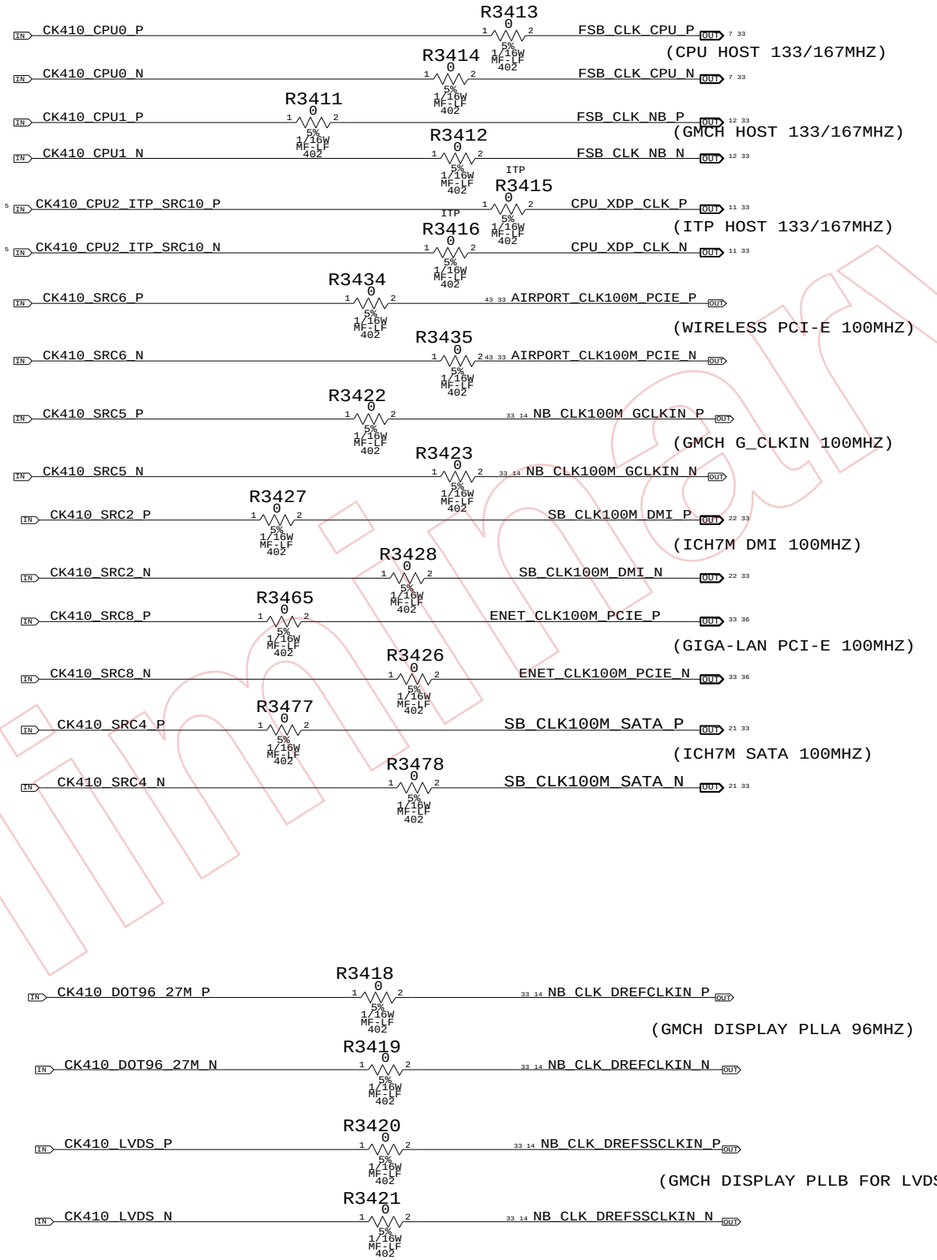
SET FCTSEL0,FCTSEL1 TO 00
EVEN THESE TWO PINS INTERNAL PULL DOWN,
CYPRESS RECOMMAND TO ADD EXTERNAL PULLS,

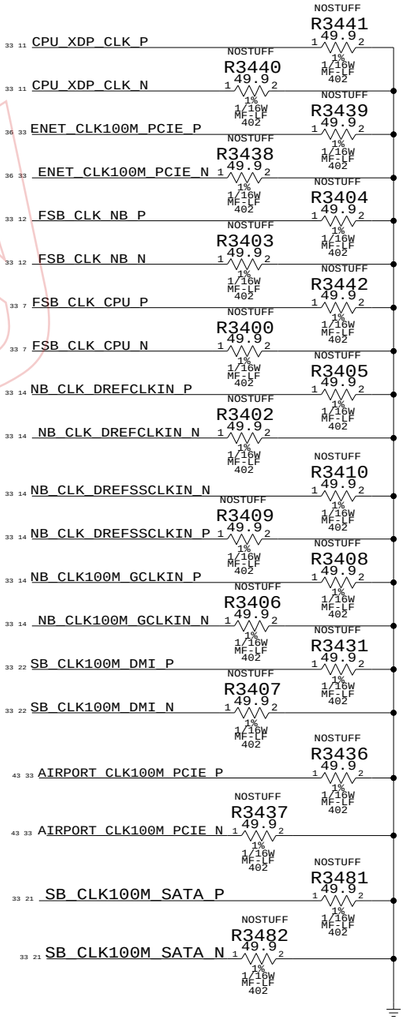
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	1	0	1	100M
	0	0	1	133M
#	0	1	1	166M
	0	1	0	200M

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ







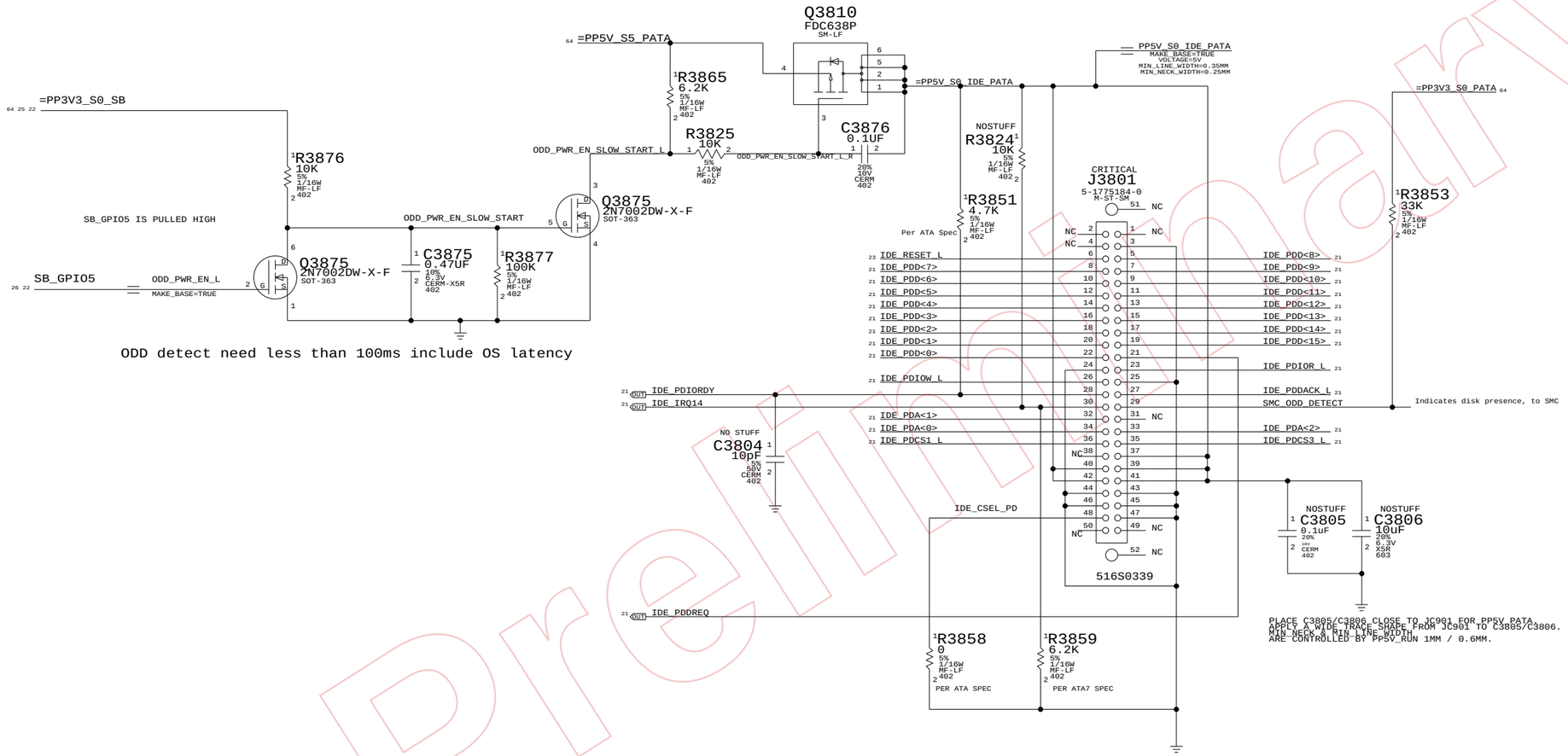
CLOCK TERMINATION

SYNC_MASTER=CLOCK SYNC_DATE=06/06/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	34	108

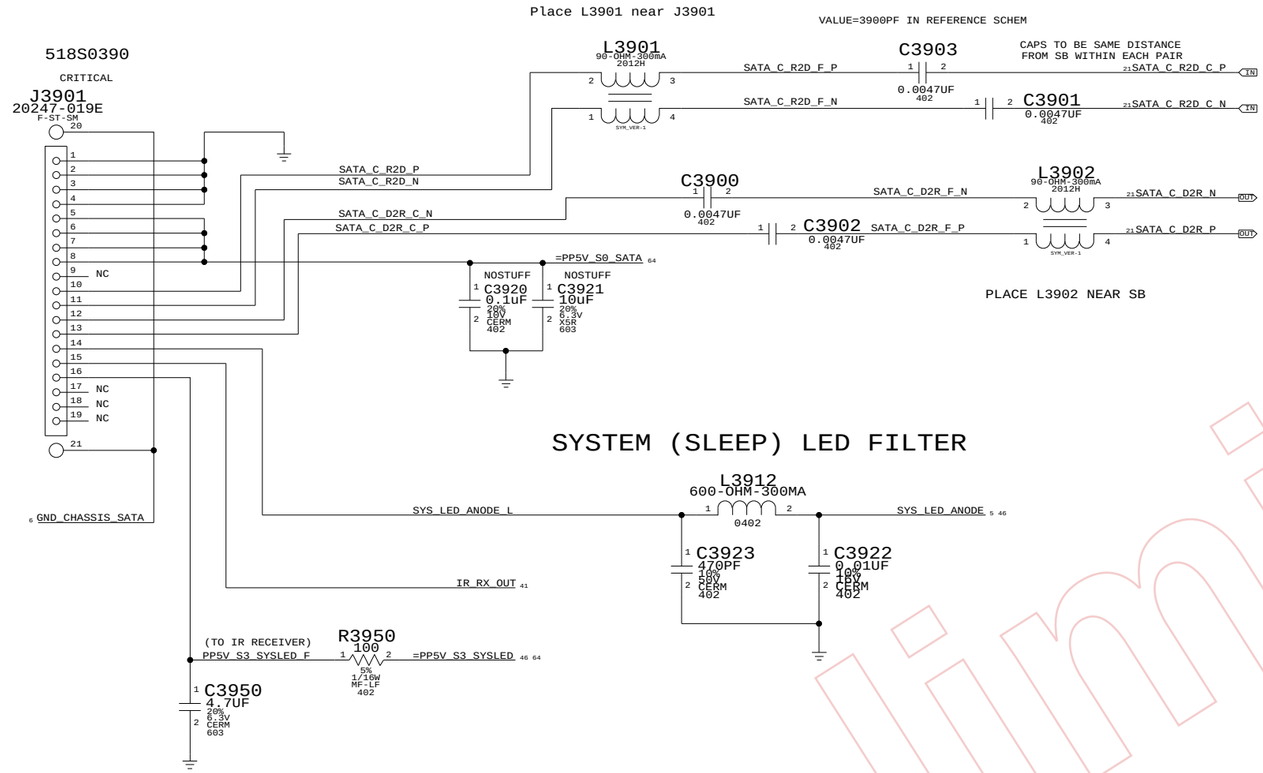


PATA CONNECTOR

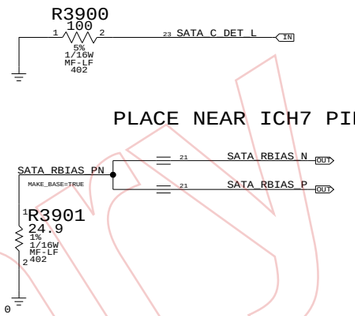
APPLE COMPUTER INC.

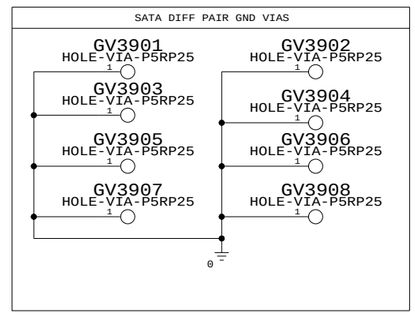
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 38 OF 108	

SATA CONNECTOR



SYSTEM (SLEEP) LED FILTER





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901,L3902	KEEP MAG.LAYER IN BOM

SATA CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 39 OF 108	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

37 PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402-LF

=PP2V5_S3_ENET 64

PLACE C4107 NEAR U4101 AVDD

64 36 =PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

=PP1V2_S3_ENET 36 64

=PP3V3_S3_ENET 36 64

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402

NOSTUFF
R4107 0 5% 1/16W MF-LF 402

22 SB_GPIO30 — ENET_LOM_DIS_L

PCIE_A_D2R_C_P — C4110 — PCIE_A_D2R_P (22) OUT
PCIE_A_D2R_C_N — C4111 0.1UF 10% 16V X5R 402 — PCIE_A_D2R_N (22) OUT

C4112 0.1UF X5R 10% 16V 402

PCIE_A_R2D_P — C4113 0.1UF 10% 16V X5R 402 — PCIE_A_R2D_C_P (22) IN
PCIE_A_R2D_N — PCIE_A_R2D_C_N (22) IN

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

64 36 =PP3V3_S3_ENET
64 =PP3V3_S0_ENET

OMIT
CRITICAL
U4101
88E8053
QFN

VDD7 48, VDD6 44, VDD5 39, VDD4 33, VDD3 13, VDD2 7, VDD1 2, VDD0 61
VDDO_TTL4 45, VDDO_TTL3 40, VDDO_TTL2 8, VDDO_TTL1 1, VDDO_TTL0 23
AVDD 57, AVDDL6 52, AVDDL5 51, AVDDL4 32, AVDDL3 28, AVDDL2 22, AVDDL1 19, AVDDL0 64
VDD25

10 LOM_DISABLE*
12 VAUX_AVLBL
47 VMAIN_AVLBL
NC 11 SWITCH_VCC
NC 9 SWITCH_VAUX
NC 24 HSDACP
NC 25 HSDACN
6 ENET_CTRL25 — 4 CTRL25
6 ENET_CTRL12 — 3 CTRL12
ENET_RSET — 16 RSET

OPTIONAL EXTERNAL LDO

ANALOG

PCI EXPRESS

TX_P 49
TX_N 50
RX_P 54
RX_N 53
REFCLKP 55 — 33 ENET_CLK100M_PCIE_P (IN)
REFCLKN 56 — 33 ENET_CLK100M_PCIE_N (IN)
WAKE* 6 — 43 23 PCIE_WAKE_L (OUT)
PERST* 5 — 26 ENET_RST_L (IN)

MDIP0 17 / MDIN0 18 — 37 ENET_MDI_P<0> / ENET_MDI_N<0> (IO)
MDIP1 20 / MDIN1 21 — 37 ENET_MDI_P<1> / ENET_MDI_N<1> (IO)
MDIP2 26 / MDIN2 27 — 37 ENET_MDI_P<2> / ENET_MDI_N<2> (IO)
MDIP3 30 / MDIN3 31 — 37 ENET_MDI_P<3> / ENET_MDI_N<3> (IO)

MEDIA

NO PULL-UP NEEDED
R4102 4.75K 1% 1/16W MF-LF 402

NC 59 LED_ACT*
NC 60 LED_LINK10/100*
NC 62 LED_LINK1000*
NC 63 LINK*

LED

29 TSTPT
46 TESTMODE

TEST

TWSI
VPD_CLK 38 — ENET_VPD_CLK 36
VPD_DATA 41 — ENET_VPD_DATA 36

TEST
PU_VDDO_TTL0 42 — ENET_PU_VDD_TTL0 36
PU_VDDO_TTL1 43 — ENET_PU_VDD_TTL1 36

ASF IS UNAVAILABLE ON 8053

SPI
SPI_DI 35 NC
SPI_DO 34 NC
SPI_CLK 37 NC
SPI_CS 36 NC

INTERNAL PULL-UP

MAIN CLK
XTALI 15 — ENET_XTALI
XTALO 14 — ENET_XTALO

CRITICAL

1. KEEP ENET_XTALI AND ENET_XTALO
TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

Y4101 25.0000M SM-3.2X2.5MM
C4150 15PF 5% 50V CERM 402
C4151 15PF 5% 50V CERM 402

THRML_PAD

R4106 49.9 1% 1/16W MF-LF 402 — ENET_MDI0
R4105 49.9 1% 1/16W MF-LF 402 — ENET_MDI0
R4104 49.9 1% 1/16W MF-LF 402 — ENET_MDI1
R4103 49.9 1% 1/16W MF-LF 402 — ENET_MDI1
R4120 49.9 1% 1/16W MF-LF 402 — ENET_MDI2
R4119 49.9 1% 1/16W MF-LF 402 — ENET_MDI2
R4118 49.9 1% 1/16W MF-LF 402 — ENET_MDI3
R4117 49.9 1% 1/16W MF-LF 402 — ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET 36 64

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

36 ENET_PU_VDD_TTL0
36 ENET_PU_VDD_TTL1

64 36 =PP3V3_S3_ENET

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08
SO8

VCC 8
E2 3
NC1 2
NC0 1
WC* 7
SDA 5 — ENET_VPD_DATA 36
SCL 6 — ENET_VPD_CLK 36
VSS 4

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

NOSTUFF
R4124 0 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

64 36 =PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

64 36 =PP3V3_S3_ENET

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=ENET
SYNC_DATE=12/06/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 41 OF 108	

L4250
120-OHM-0.3A-EMI
0402-LF

PP2V5_S3_ENET_AVDD
PP2V5_S3_ENET_AVDD_F

PLACE ONE CAP AT EACH PIN 3 AND 6 OF TRANSFORMERS

C4200 0.1UF 10% 16V X5R 402
C4201 0.1UF 10% 16V X5R 402
C4202 0.1UF 10% 16V X5R 402
C4203 0.1UF 10% 16V X5R 402

PLACE ONE CAP NEAR EACH PIN 3 AND 6 OF TRANSFORMERS

C4204 0.001UF 10% 50V CERM 402
C4205 0.001UF 10% 50V CERM 402
C4206 0.001UF 10% 50V CERM 402
C4207 0.001UF 10% 50V CERM 402

CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING

CRITICAL
1000BT-824-00275
T4201
XFR-SM

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
NC1 NC2 NC4 NC3
ENET_CENTER_TAP<0>
ENET_CENTER_TAP<1>
ENET_MDI_TRAN_P<0>
ENET_MDI_TRAN_N<0>
ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>

CRITICAL
1000BT-824-00275
T4202
XFR-SM

ENET_MDI_P<3>
ENET_MDI_N<3>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_CENTER_TAP<2>
ENET_CENTER_TAP<3>
ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_N<3>
ENET_MDI_TRAN_P<2>
ENET_MDI_TRAN_N<2>

OMIT
CRITICAL
J4200
RJ45
819B-3608-M280
F-RT-SM
SYM_VER-2
514S0119

R4200 75 1% 1/16W MF-LF 402
R4201 75 1% 1/16W MF-LF 402
R4202 75 1% 1/16W MF-LF 402
R4203 75 1% 1/16W MF-LF 402

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

C4210 0.001UF 20% 2KV CERM 1808

=GND_CHASSIS_RJ45

C4211 0.001UF 10% 50V CERM 402
C4212 0.001UF 10% 50V CERM 402

PLACE C4211 AND C4212
ON EACH SIDE OF J4200

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0037	157S0011	?	T4201,T4202	E&E AND DELTA TRANSFORMER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN,8P RJ-45 JACK,MIDPLANE,MG3,LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN,8P RJ-45 JACK,MIDPLANE,BLACK,LF	J4200	CRITICAL	FANCY

ETHERNET CONNECTOR

SYNC_MASTER=ENET
SYNC_DATE=11/14/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 42 OF 108	

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510R PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PCB CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

64 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 10V CERM 402
C4422 0.1UF 10% 10V CERM 402
C4426 0.1UF 10% 10V CERM 402
C4428 0.1UF 10% 10V CERM 402
C4430 0.1UF 10% 10V CERM 402
C4432 0.1UF 10% 10V CERM 402

L4400 600-OHM-300MA 0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

PP3V3_S3_FW_AVDD VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 10V X5R 402
C4429 0.1UF 10% 10V X5R 402
C4425 0.1UF 10% 10V X5R 402

64 =PP3V3_S3_PCI

G4 VDD0 · M1 VDD1 · M2 VDD2 · K5 VDD3 · K7 VDD4 · L13 VDD5 · H13 VDD6 · H7 VDD7 · A2 VDD8
D10 VDDA0 · A13 VDDA1 · B13 VDDA2 · A7 VDDA3 · A8 VDDA4 · D6 VDDA5

CONNECT TO VDD FOR 3.3V OPERATION

G13 PCI_VIOS

PCI_AD<0>	F10	PCI_AD0
PCI_AD<1>	G10	PCI_AD1
PCI_AD<2>	H10	PCI_AD2
PCI_AD<3>	H12	PCI_AD3
PCI_AD<4>	J13	PCI_AD4
PCI_AD<5>	J12	PCI_AD5
PCI_AD<6>	K13	PCI_AD6
PCI_AD<7>	K10	PCI_AD7
PCI_AD<8>	L12	PCI_AD8
PCI_AD<9>	M13	PCI_AD9
PCI_AD<10>	L11	PCI_AD10
PCI_AD<11>	M12	PCI_AD11
PCI_AD<12>	M11	PCI_AD12
PCI_AD<13>	N12	PCI_AD13
PCI_AD<14>	M10	PCI_AD14
PCI_AD<15>	N11	PCI_AD15
PCI_AD<16>	M4	PCI_AD16
PCI_AD<17>	N5	PCI_AD17
PCI_AD<18>	N4	PCI_AD18
PCI_AD<19>	M3	PCI_AD19
PCI_AD<20>	M2	PCI_AD20
PCI_AD<21>	N3	PCI_AD21
PCI_AD<22>	K4	PCI_AD22
PCI_AD<23>	M1	PCI_AD23
PCI_AD<24>	K2	PCI_AD24
PCI_AD<25>	J4	PCI_AD25
PCI_AD<26>	K1	PCI_AD26
PCI_AD<27>	J2	PCI_AD27
PCI_AD<28>	J1	PCI_AD28
PCI_AD<29>	H2	PCI_AD29
PCI_AD<30>	H4	PCI_AD30
PCI_AD<31>	H1	PCI_AD31
PCI_C_BE_L<0>	K12	PCI_CBE0*
PCI_C_BE_L<1>	M9	PCI_CBE1*
PCI_C_BE_L<2>	L3	PCI_CBE2*
PCI_C_BE_L<3>	L1	PCI_CBE3*
PCI_PAR	N10	PCI_PAR
PCI_FRAME_L	N6	PCI_FRAME*
PCI_IRDY_L	M6	PCI_IRDY*
PCI_TRDY_L	N7	PCI_TRDY*
PCI_DEVSEL_L	N8	PCI_DEVSEL*
PCI_STOP_L	M7	PCI_STOP*
FW_PCI_IDSEL	L2	PCI_IDSEL
PCI_REQ3_L	E2	PCI_REQ*
PCI_GNT3_L	E1	PCI_GNT*
PCI_PERR_L	M8	PCI_PERR*
PCI_SERR_L	N9	PCI_SERR*
PCI_CLK_FW	G2	PCI_CLK
PM_CLKRUN_L	D1	CLKRUN*
FW_PCI_RST_L	F1	PCI_RST*
INT_PIRQD_L	D2	PCI_INTA*
PCI_PME_FW_L	F2	PCI_PME*

R4431 22 5% 1/16W MF-LF 402

R4432 100 1% 1/16W MF-LF 402

THIS IS FROM ICH-7M

PLACE R4432 VERY CLOSE TO PIN B18 OF U2100

OMIT
CRITICAL
U4400
FW32306
BGA

197S0030 3.2MMX2.5MM
CRITICAL
Y4403
SM-3.2X2.5MM
24.576MHZ

R4400 390 5% 1/16W MF-LF 402
C4411 15pF 5% 50V C0G 402
C4412 15pF 5% 50V C0G 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5	FW_XI
XO	B5	FW_XO
RESET*	B4	FW_PWRON_RST_L
R1	A6	FW_R1
R0	B7	FW_R0

SPEC RECOMMENDS 2.49K

R4452 2.1K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 10V X5R 402
R4420 510K 5% 1/10W MF-LF 402

TPBIAS0	B8	FW_A_TPBIAS
TPA0_P	A9	FW_A_TPA_P
TPA0_N	B9	FW_A_TPA_N
TPB0_P	B10	FW_A_TPB_P
TPB0_N	A10	FW_A_TPB_N
TPBIAS1	D8	FW_B_TPBIAS
TPA1_P	A11	FW_B_TPA_P
TPA1_N	B11	FW_B_TPA_N
TPB1_P	B12	FW_B_TPB_P
TPB1_N	A12	FW_B_TPB_N
TPBIAS2	C13	FW_C_TPBIAS
TPA2_P	C11	FW_C_TPA_P
TPA2_N	C12	FW_C_TPA_N
TPB2_P	D13	FW_C_TPB_P
TPB2_N	D12	FW_C_TPB_N

MODE_420	M5	MODE FOR EXTERNAL LINK
MODE_A	B6	
PC0	E12	FW_PC0
PC1	F13	
PC2	F12	
CONTENDER	G12	LOW = NOT BUS MANAGER
CARDBUSN	B1	LOW = PCI OPERATION
MPCI_ACTN_323	E10	

DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)

MANUFACTURING TEST PINS

TEST0	C2
TEST1	C1
PTEST	A4
SE	A3
SM	B3

A1 VSS0 · B2 VSS1 · C3 VSS2 · D4 VSS3 · E4 VSS4 · E5 VSS5 · F4 VSS6 · F6 VSS7 · F7 VSS8 · F8 VSS9 · G1 VSS10 · G6 VSS11 · G7 VSS12 · G8 VSS13 · H6 VSS14 · H7 VSS15 · H8 VSS16 · J5 VSS17 · J9 VSS18 · J10 VSS19 · K8 VSS20 · K9 VSS21 · N13 VSS22
E13 VSSA0 · E9 VSSA1 · D9 VSSA2 · D7 VSSA3 · D5 VSSA4

FIREWIRE CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE COMPUTER INC.

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D	051-7173	C
SCALE: NONE	SHT 44 OF 108	

Page Notes

INPUT:

=PPBUS_FW - PORT POWER

=PP3V3_S5_FW - DIGITAL POWER

=GND_CHASSIS_FW_PORT0 - CHASSIS GROUND

=FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:

FW_TPA0_P/N,FW_TPB0_P/N,FW_TPBIAS0 - FIREWIRE DIFF PAIRS

OUTPUT:

FW_PC0 - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

PAGE HISTORY

5/19/05 - INITIAL REVISION
6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
6/22/05 - CONNECTED FW_PC0 FOR SINGLE PORT
7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1
7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
7/26/05 - SWITCHED TO 514-0124 FOR PRE-PROTO CONNECTOR
7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
7/26/05 - CHANGED FL4590 TO 1.1A VERSION
7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT
1 FOR DUAL PORT

38 OUT FW_PC0

PPBUS_S5_FWPWRSW_F
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

64 =PPBUS_S5_FWPWRSW
FL4590
1.1A-24V
MINISMDC

Q4590
FDC638P
SM-LF

PPFW_SWITCH
VOLTAGE=19V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

D4590
SMB
B340LBXF

64 =PP3V3_S0_FW
R4590 470K 5% 1/16W MF-LF 402
C4590 0.01uF 10% 16V CERM 402
R4593 100K 5% 1/16W MF-LF 402
FWPWR_EN_L_DIV
MIN_LINE_WIDTH=0.05MM
MIN_NECK_WIDTH=0.05MM
R4591 330K 5% 1/16W MF-LF 402

IF =FWPWR_PWRON IS NC:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC
IF =FWPWR_PWRON LOW WHEN OFF:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC AND NOT SHUTDOWN

D4591 BAS16TW-X-F SOT-363
FWPWR_RUN
6 =FWPWR_PWRON
FWPWR_EN_L 60
Q4591 2N7002 SOT23-LF
FWPWR_EN
65 46 45 5 SMC_PS_ON
R4594 10K 5% 1/16W MF-LF 402
FWPWR_ACIN
R4595 470K 5% 1/16W MF-LF 402

Enables port power whenever
machine AC Adapter is plugged
or system at run state with battery only

Cable Power
PPFW_PORT0_VP_F
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L4510 FERR-250-OHM SM
PPFW_PORT0_VP
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C4510 0.001uF 10% 50V CERM 402

"Snapback" & "Late VG" Protection

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A 0.5V DROP

39 PP3V3_S5_FWLATEVG
C4520 0.01UF 10% 16V CERM 402
D4520 BAV99DW-X-F SOT-363
C4521 0.01UF 10% 16V CERM 402
D4520 BAV99DW-X-F SOT-363

38 FW_A_TPBIAS
R4500 56.2 1% 1/16W MF-LF 402
R4501 56.2 1% 1/16W MF-LF 402
C4500 0.33UF 10% 6.3V CERM-X5R 402

38 FW_A_TPA_P
38 FW_A_TPA_N
38 FW_A_TPB_P
38 FW_A_TPB_N

FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N

120-OHM 2012 SYM_VER-2
FL4520
120-OHM 2012 SYM_VER-2
FL4521

FW_PORT0_TPA_P_FL
FW_PORT0_TPA_N_FL
FW_PORT0_TPB_P_FL
FW_PORT0_TPB_N_FL
(PPFW_PORT0_VP)
(GND_FW_PORT0_VGND)

PORT 0
1394A
OMIT
CRITICAL
J4500
1394A
F-RT-TH1
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
=GND_CHASSIS_FW_UPPER
Plexi: 514-0124
Enclosure: 514-0289
=GND_CHASSIS_FW_DOWN

R4502 56.2 1% 1/16W MF-LF 402
R4503 56.2 1% 1/16W MF-LF 402
FW_PORT0_TPB
C4501 220PF 5% 25V CERM 402
R4504 4.99K 1% 1/16W MF-LF 402

D4521 BAV99DW-X-F SOT-363
C4522 0.01UF 10% 16V CERM 402
D4521 BAV99DW-X-F SOT-363
C4523 0.01UF 10% 16V CERM 402
C4524 0.01UF 10% 50V X7R 603-1
C4525 0.01uF 10% 16V CERM 402

LATE-VG PROTECTION POWER

64 =PP3V3_S5_FWLATEVG
R4550 330 5% 1/16W MF-LF 402
PP3V3_S5_FWLATEVG_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM
L4550 400-OHM-EMI SM-1
PP3V3_S5_FWLATEVG
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM
39
NO STUFF C4551 0.1uF 20% 10V CERM 402
NO STUFF C4552 0.001uF 10% 50V CERM 402
D4550 SOT23 MMBZ5227B

CAPS MAY NOT BE NECESSARY.
NO STUFF FOR NOW THOUGH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN,6P 1394A RCPT,MIDPLANE,MG3,LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK,LF	J4500	CRITICAL	FANCY

FIREWIRE PORT

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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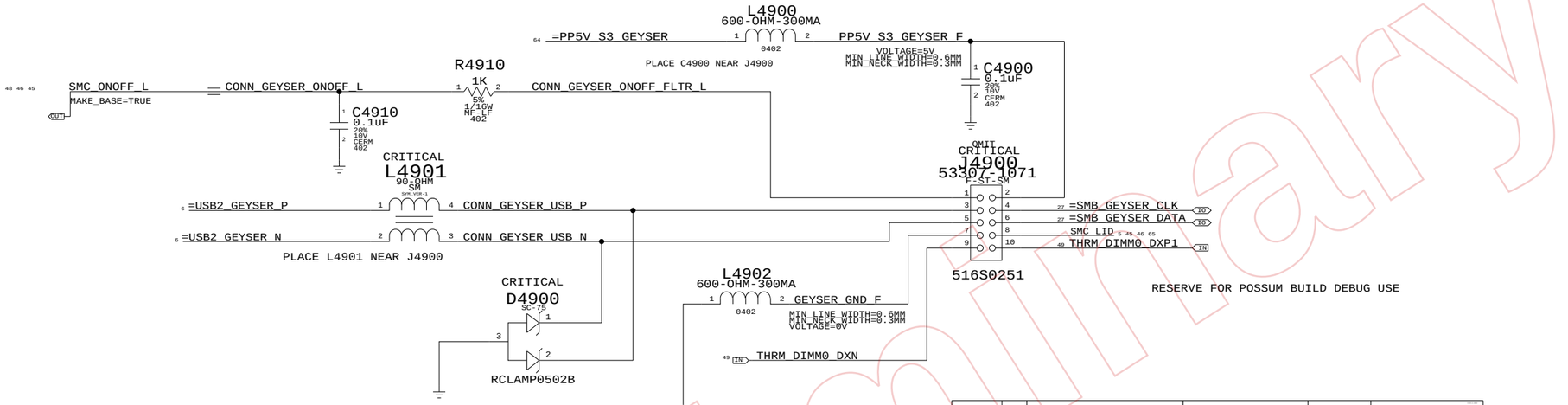
D	051-7173	C
SCALE: NONE	SHT 45 OF 108	

GEYSER AND DIMM0 REMOTE TEMP SENSORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY

CONNECTOR MISC

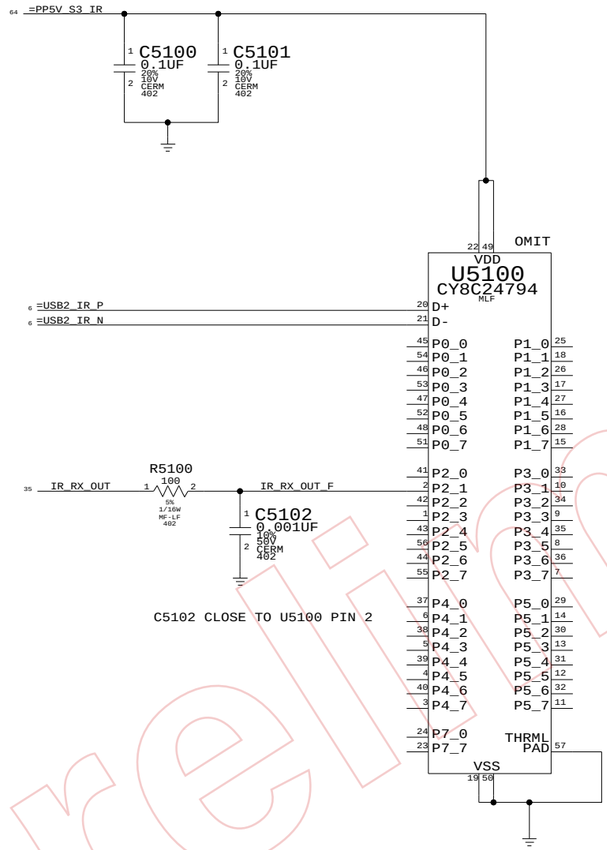
SYNC_MASTER=ENET SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	49	108

PLACE C5100 AND C5101
NEAR U5100 PIN 22 AND 49



IR CONTROLLER

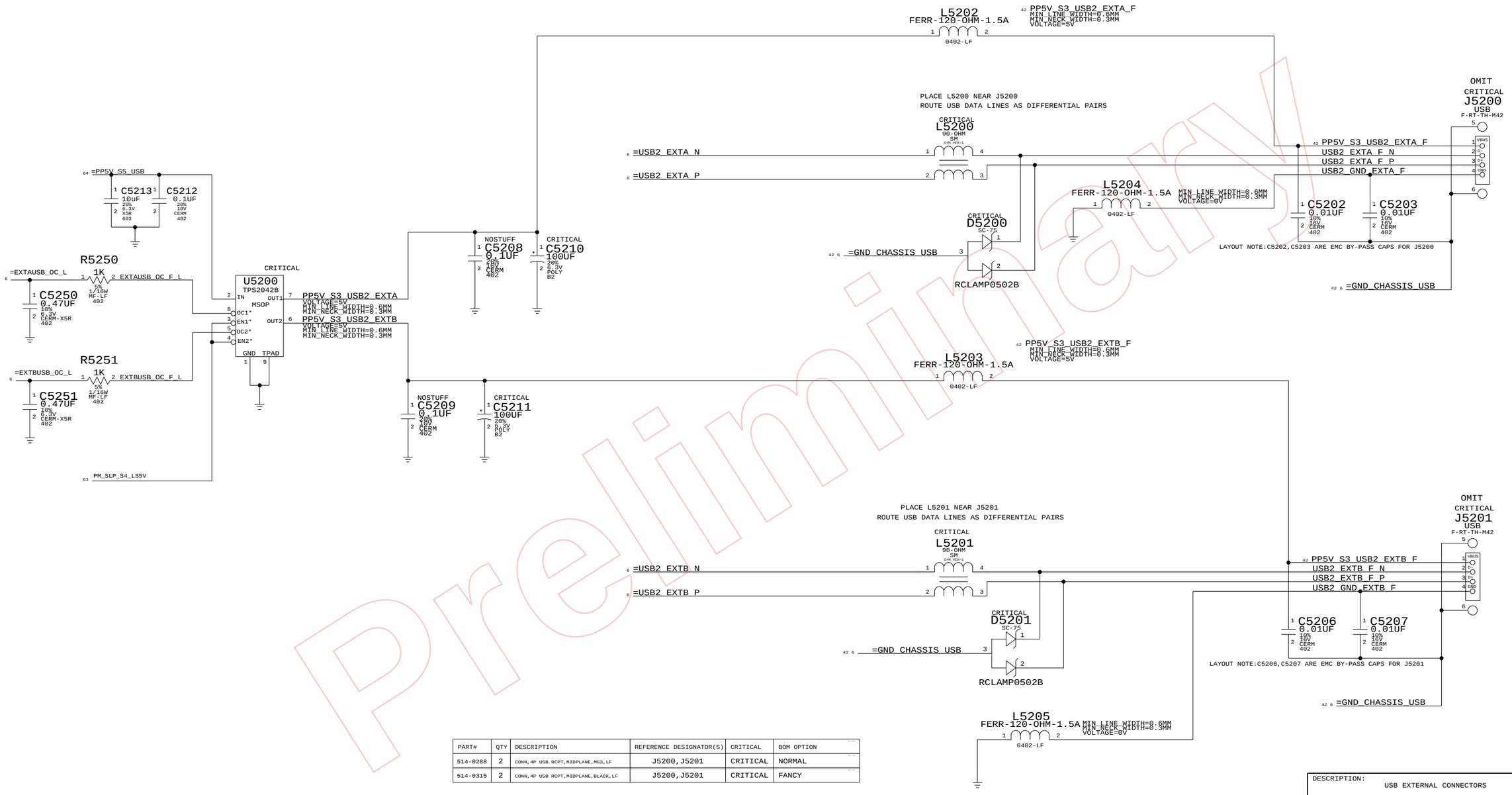
SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	51	108

USB 2.0 CONNECTORS

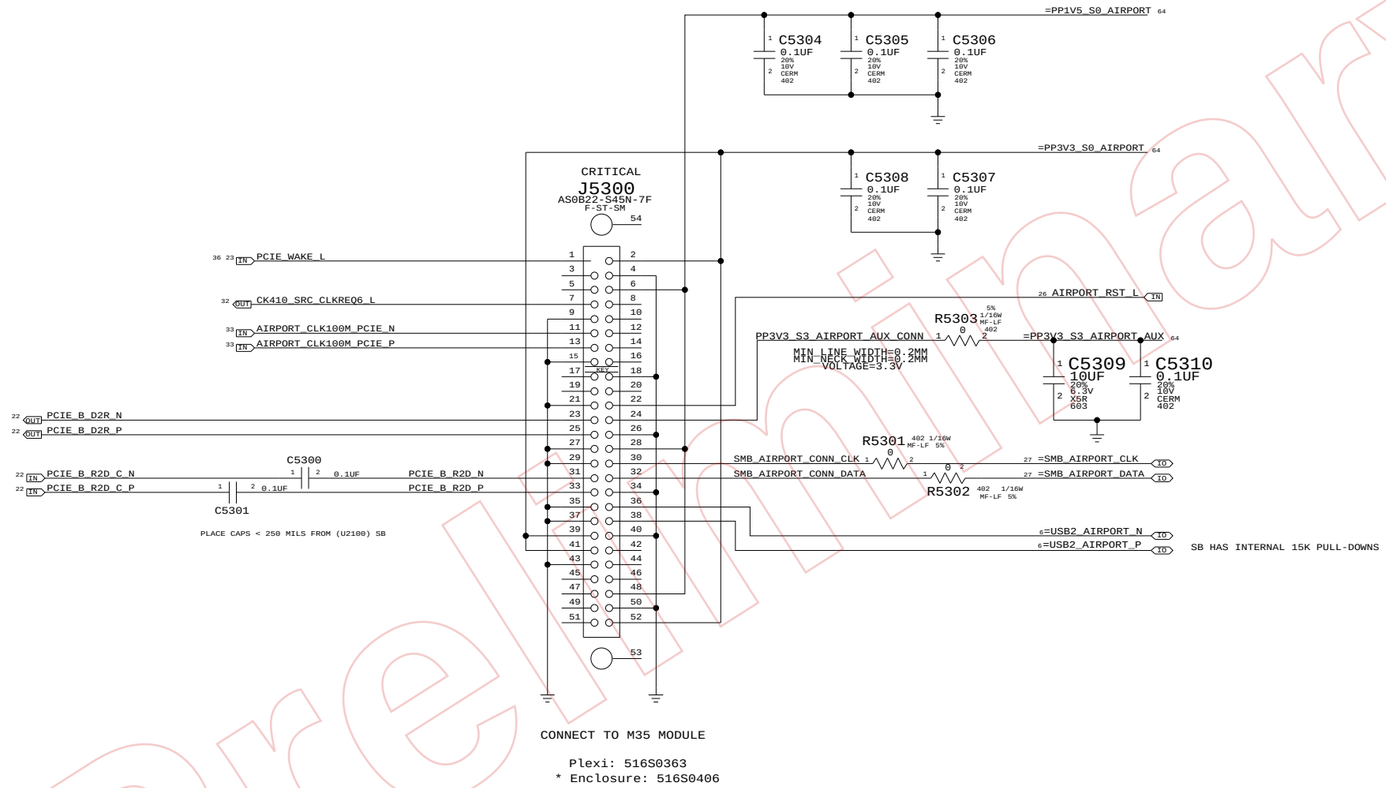


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN,4P USB RCPT,MIDPLANE,MG3,LF	J5200,J5201	CRITICAL	NORMAL
514-0315	2	CONN,4P USB RCPT,MIDPLANE,BLACK,LF	J5200,J5201	CRITICAL	FANCY

DESCRIPTION:
USB EXTERNAL CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 52 OF 108	

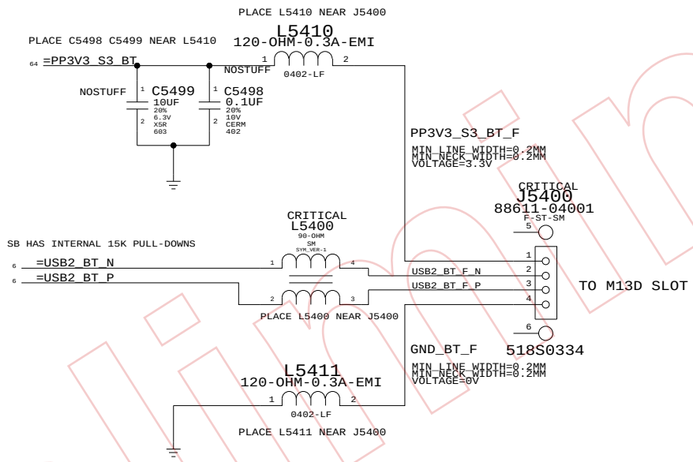


AIRPORT CONN

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	53	108



BLUETOOTH INTERFACE

APPLE COMPUTER INC.

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23 OUT	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	63	SMC_PM_G2_EN OUT
26 OUT	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	65 46 39 5	SMC_PS_ON (Enable AC adapter PWR) OUT
63 26 5 IN	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22	SPI_ARB OUT
59 46 IN	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	50 22	SPI_SCLK OUT
23 OUT	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	50 22	SPI_SI OUT
23 OUT	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	50 22	SPI_SO IN
58 OUT	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	46	SMC_PROCHOT_3_3_L IN
23 OUT	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	6	SMC_CPU_INIT_3_3_L IN
46	SMC_P20	D13	P20	P70/AN0	N12	48	SMC_CPU_ISENSE IN
46	SMC_P21	D14	P21	P71/AN1	R13	48 5	SMC_CPU_VSENSE IN
46	SMC_P22	D15	P22	P72/AN2	P13	46	SMC_GPU_ISENSE IN
46	SMC_P23	E12	P23	P73/AN3	R14	46	SMC_GPU_VSENSE IN
66 46 5 OUT	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	66	SMC_DCIN_ISENSE IN
66 46 5 OUT	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	48	SMC_PBUS_VSENSE IN
46	SMC_P26	E13	P26	P76/AN6	N13	66	SMC_BATT_ISENSE IN
46	SMC_P27	F14	P27	P77/AN7	P15	46	SMC_FWIRE_ISENSE IN
53 47 21 5 IO	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L OUT
53 47 21 5 IO	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	46	SMC_TPM_GPIO IO
53 47 21 5 IO	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	53 47 38 23 5	PM_CLKRUN_L IO
53 47 21 5 IO	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	53 47 46 23 5	PM_SUS_STAT_L IN
53 47 21 5 IN	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	46	SC_TX_L (Serial Port Transmit) IO
26 IN	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	46	SC_RX_L (Serial Port Receive) IO
33 IN	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27	SMB_BSB_CLK (BAT B SMBUS CLK) IO
53 47 23 5 OUT	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	48 46 40	SMC_ONOFF_L IN
OUT	SMC_DISPLAY_ENABLE	A5	P40/TMIO	P91/IRQ1*	J2	66 65 46 5	SMC_BC_ACOK (AC I/P detect) IN
46 OUT	SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	65 46 5	SMC_BS_ALRT_L IN
27 IO	SMB_BSB_DATA (BAT B SMBUS DATA)	D5	P42/SDA1	P93/IRQ12*	J3	63 23	PM_SLP_S3_L IN
53 OUT	SMC_TPM_PP (TPM physical presence)	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	63 61 60 23	PM_SLP_S4_L IN
46	SMC_P44	B1	P44/TMO1	P95/IRQ14*	H2	46 23	PM_SLP_S5_L IN
OUT	SMC_BKLIGHT_ENABLE	C2	P45	P96/EXCL	H1	46	SMC_SUS_CLK IN
46	SMC_P46	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27	SMB_0_DATA IO
47 46 5 OUT	SMC_TX_L (Debug feature,16550 Transmit)	C1	P47/PWX1/PWM1				
47 46 5 IN	SMC_RX_L (Debug feature,16550 Receive)	G1	P50				
27 IO	SMB_0_CLK	G4	P51				
		F2	P52/SCL0				

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21 IO	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3		SMC_CASE_OPEN (CASE OPEN/CLOSE DETECT) 46
47 22 5 IN	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	47 46 5	SMC_TCK IN
26 23 IN	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	47 46 5	SMC_TDI IN
53 46 OUT	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	47 46 5	SMC_TDO OUT
14 6 IN	PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	47 46 5	SMC_TMS IN
23 IO	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_DISP_BKLT_B 46
65 46 5 IO	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_DISP_BKLT_A OUT
23 OUT	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	65 46 40 5	SMC_LID (LID_OPEN/CLOSE SW) IN
23 IN	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	46	SMC_CPU_RESET_3_3_L IN
23 OUT	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	66 5	SMC_BATT_ISET OUT
34 IN	SMC_ODD_DETECT (Optical Disk Insert detect)	D10	PB2	PF5/PWM5	R5		SMC_BATT_VSET 46
48 OUT	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	66	SMC_SYS_ISET OUT
46	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5		SMC_SYS_VSET 46
46	SMC_EXCARD_PWR_EN	C11	PB5				
46	SMC_EXCARD_PWR_OC_L	A12	PB6	PG0/EXIRQ8*/TMIX	P9	50 22	SPI_CE_L IO
46	SMC_PB7	D11	PB7	PG1/EXIRQ9*/TMIY	R9		SMC_PG1 46
46	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG2/EXIRQ10*/SDA2	N9	27	SMB_BSA_DATA IO
51 5 OUT	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG3/EXIRQ11*/SCL2	P8	27	SMB_BSA_CLK IO
46	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG4/EXIRQ12*/EXSDAA	R8	27	SMB_RMT_DATA IO
46	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG5/EXIRQ13*/EXSCLA	M8	27	SMB_RMT_CLK IO
46	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG6/EXIRQ14*/EXSDAB	P7	27	SMB_MLB_DATA IO
51 5 IN	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PG7/EXIRQ15*/EXSCLB	R7	27	SMB_MLB_CLK IO
46	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH0/EXIRQ6*	E1	46	SMC_PROCHOT OUT
46 5	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH1/EXIRQ7*	F3	46	SMC_THRMTRIP OUT
52 IN	SMS_X_AXIS	M11	PD0/AN8	PH2/FWE	K2		SMC_FWE 46
52 IN	SMS_Y_AXIS	P11	PD1/AN9	PH3/EXEXCL	C4		ALS_GAIN 46
52 IN	SMS_Z_AXIS	R11	PD2/AN10	PH4	D4	46 23	SMS_INT_L OUT
46	SMC_PD3 (ANALOG_ID)	N11	PD3/AN11	PH5	B3	52	SMS_ONOFF_L OUT
62 46	SMC_NB_ISENSE	P10	PD4/AN12				
61 46	SMC_MEM_ISENSE	R10	PD5/AN13				
46 5	ALS_LEFT	N10	PD6/AN14				
46	ALS_RIGHT	M10	PD7/AN15				

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NC	G3	NC0	NC12	F15	NC
NC	H3	NC1	NC13	A14	NC
NC	K3	NC2	NC14	C12	NC
NC	L3	NC3	NC15	C10	NC
NC	N4	NC4	NC16	C5	NC
NC	M5	NC5	NC17	A3	NC
NC	N7	NC6	NC18	B8	NC
NC	M12	NC7	NC19	E4	NC
NC	M13	NC8	NC20	H4	NC
NC	L12	NC9	NC21	M9	NC
NC	K15	NC10	NC22	N8	NC
NC	J14	NC11			

64 48 46 45 =PP3V42_G3H_SMC

CRITICAL
C5802 22UF 20% 6.3V CERM-X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE R5899, C5820 NEAR SMC PIN N14, N15

(VCL IS INTERNAL RAIL)
SMC_VCL

C5807 0.47UF 10% 16V CERM-X5R 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

64 48 46 45 =PP3V42_G3H_SMC
R5899 4.7 5% 1/16W MF-LF 402

64 48 46 45 =PP3V42_G3H_SMC
R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402

PP3V3_AVREF_SMC 46

SMC_AVCC_RC

C5820 0.1UF 20% 16V CERM 402

66 62 61 48 46 45 GND_SMC_AVSS

47 5 SMC_MD1 (Should PD) (To debug card for mode select)
KBC_MDE (Should PU)

R5802 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
NOSTUFF

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AVCC N14, N15
VCC P2, P1, J15, A1, F1
VCL M14, M15
AVREF AVREF

MD1 E2
MD2 K1

47 46 5 IN SMC_RST_L — RES* E3
46 SMC_XTAL — XTAL A2
46 SMC_EXTAL — EXTAL B2

NMI F4 (Should PD) (To debug card for mode select) — 47 5 SMC_NMI IN

ETRST* L1 — 47 5 SMC_TRST_L IN

AVSS P12, R12

VSS D1, F4, R4, F12, F13, B13, A13, A4, B4, D2

R5898 10K 5% 1/16W MF-LF 402

XW5800 SM 1 2

GND_SMC_AVSS 45 46 48 61 62 66

SMC

SYNC_MASTER=SMC SYNC_DATE=08/18/2005

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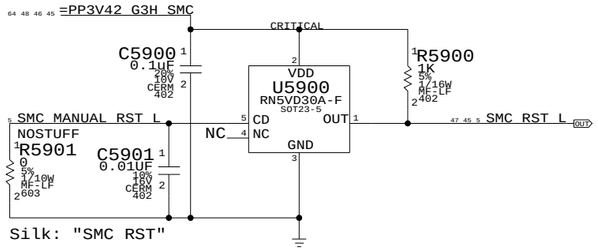
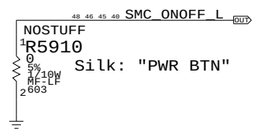
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE	SHT	OF
NONE	58	108

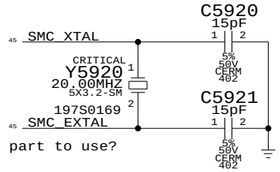
SMC Reset Button / Brownout Detect



Debug Power Button

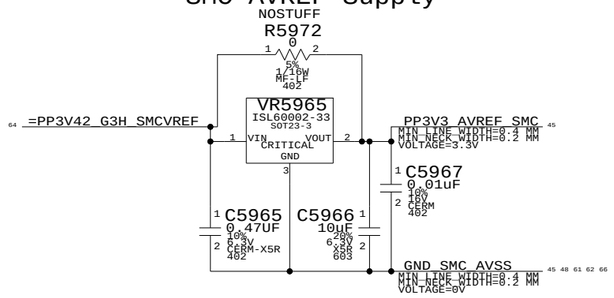


SMC Crystal Circuit



Is this the best part to use?

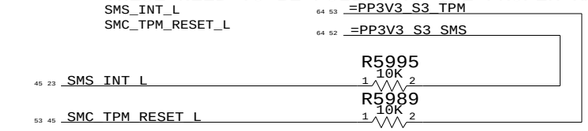
SMC AVREF Supply

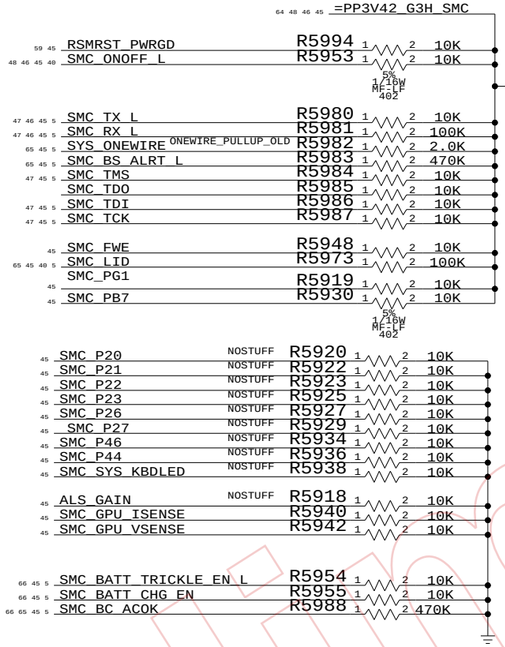


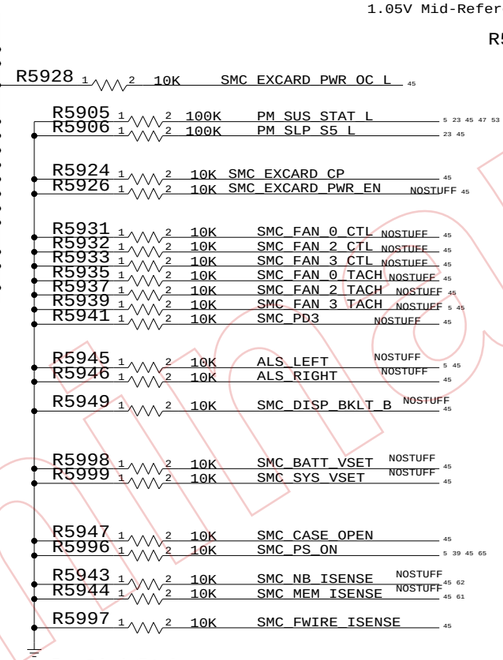
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

THESE NEED TO BE PULLED TO THE PROPER RAIL:

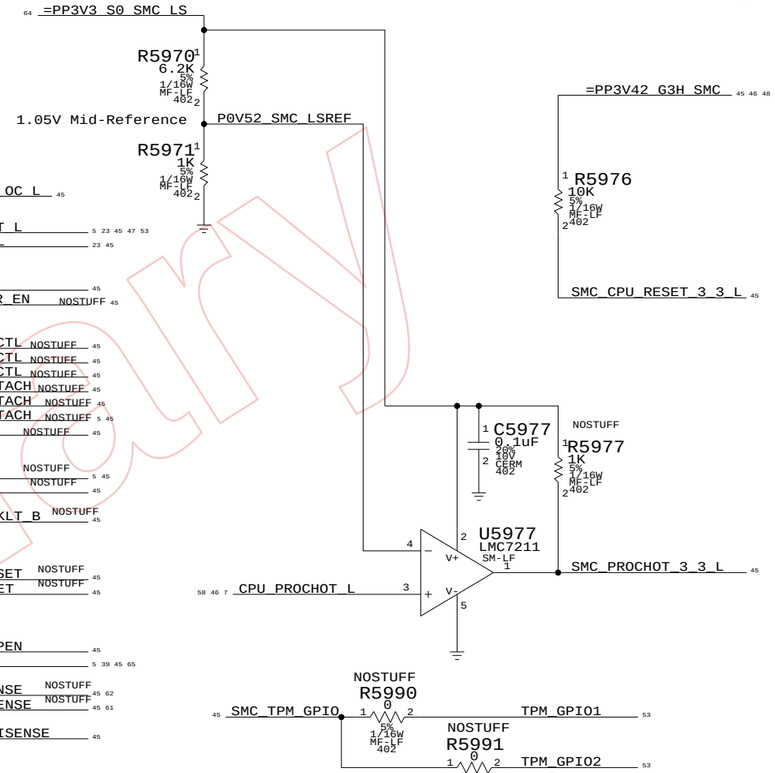
SMS_INT_L
SMC_TPM_RESET_L

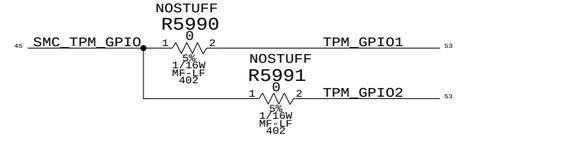






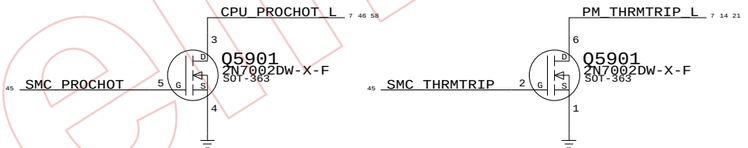
SMC 1.05V to 3.3V Level Shifting



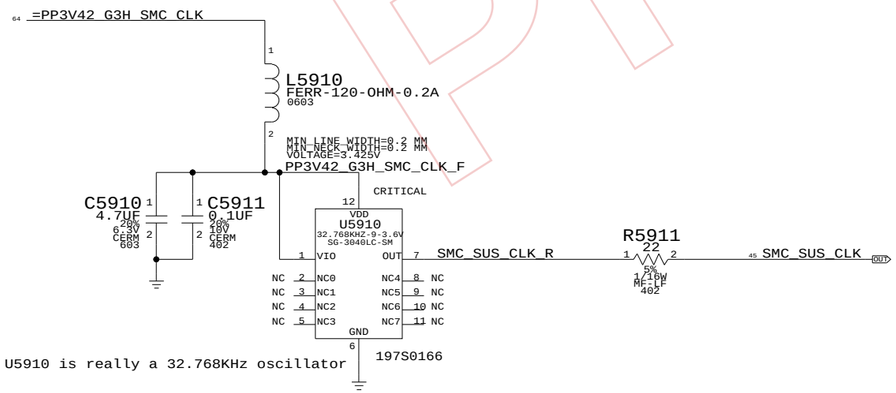


Stuff R5992, R5993 for development only

SMC 3.3V to 1.05V Level Shifting

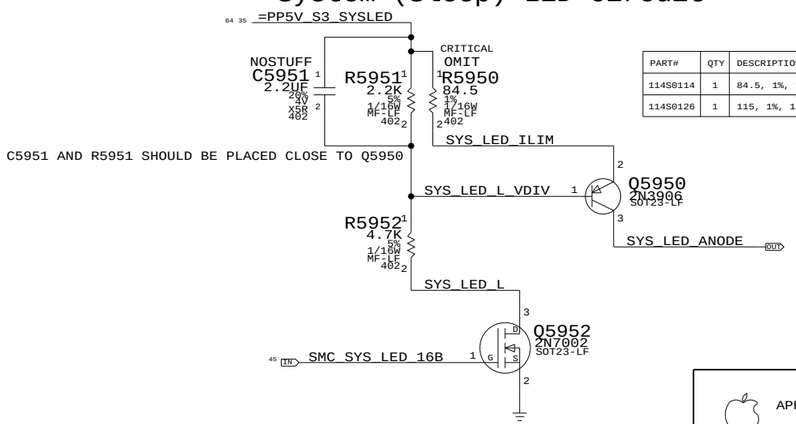


SMC G3HOT OSCILLATOR



U5910 is really a 32.768KHz oscillator

System (Sleep) LED Circuit



C5951 AND R5951 SHOULD BE PLACED CLOSE TO Q5950

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
114S0126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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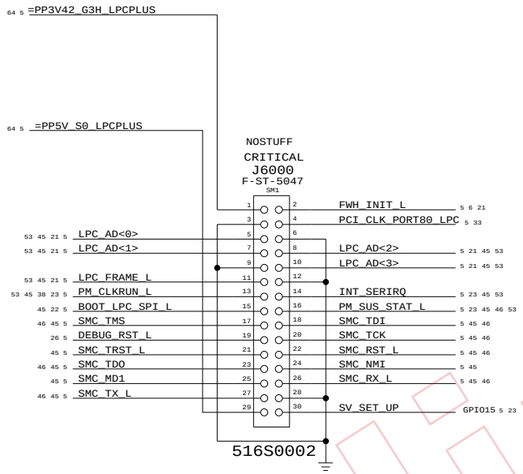
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 59 OF 108	



LPC+ Debug Connector

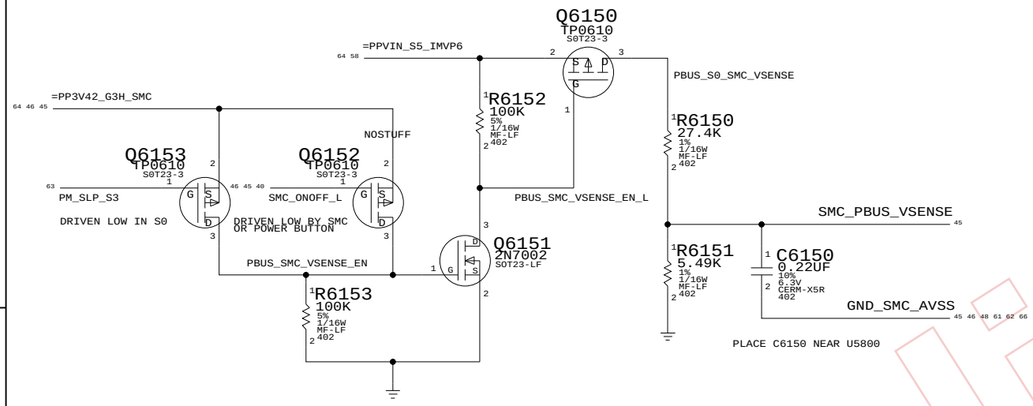
SYNC_MASTER=NB SYNC_DATE=06/30/2005

APPLE COMPUTER INC.

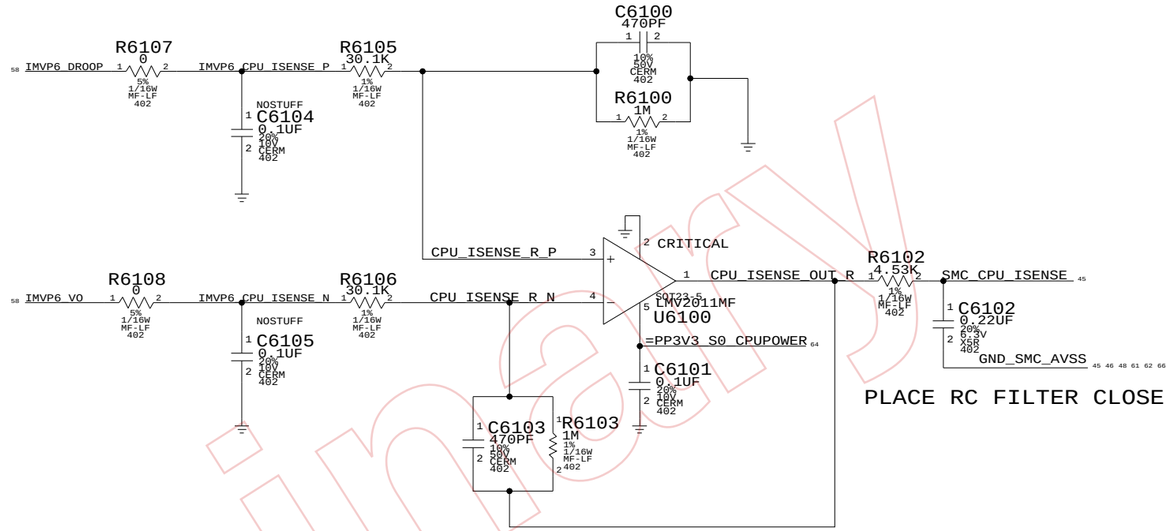
SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	60	108

PROCESSOR DCIN VOLTAGE SENSE



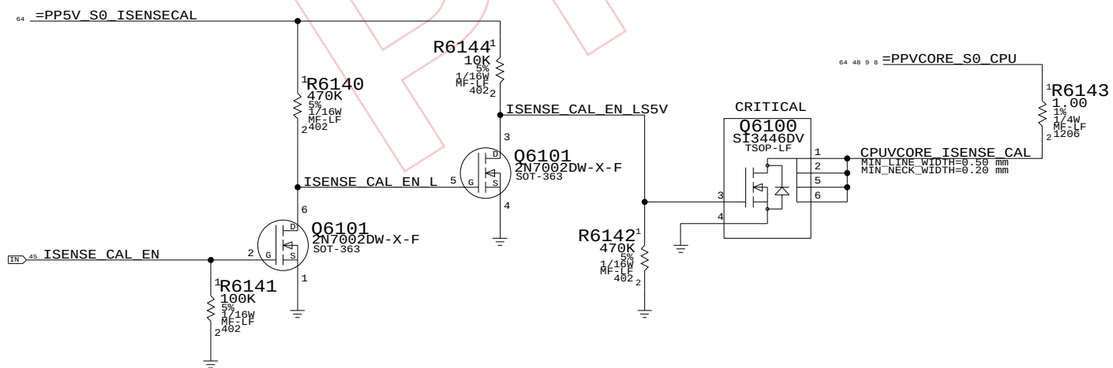
CPU CURRENT SENSE



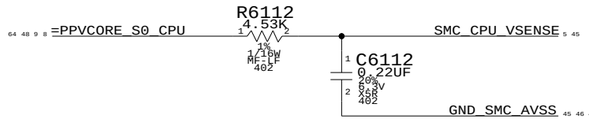
PLACE RC FILTER CLOSE TO SMC

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



CPU VOLTAGE SENSE



PLACE RC FILTER CLOSE TO SMC

CPU Current & Voltage Sense

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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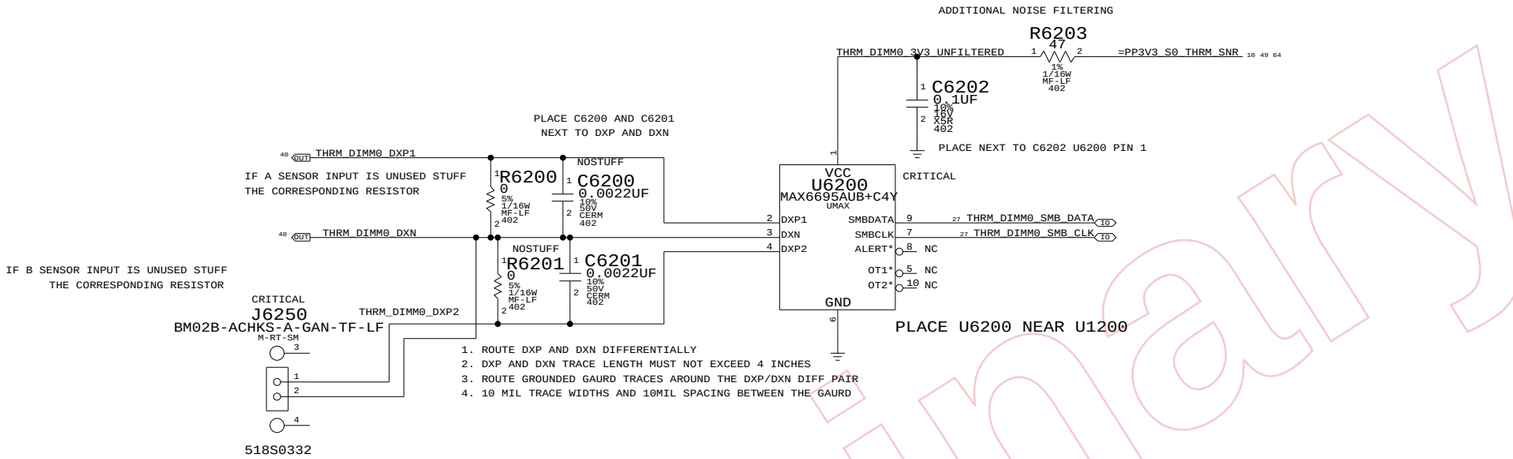
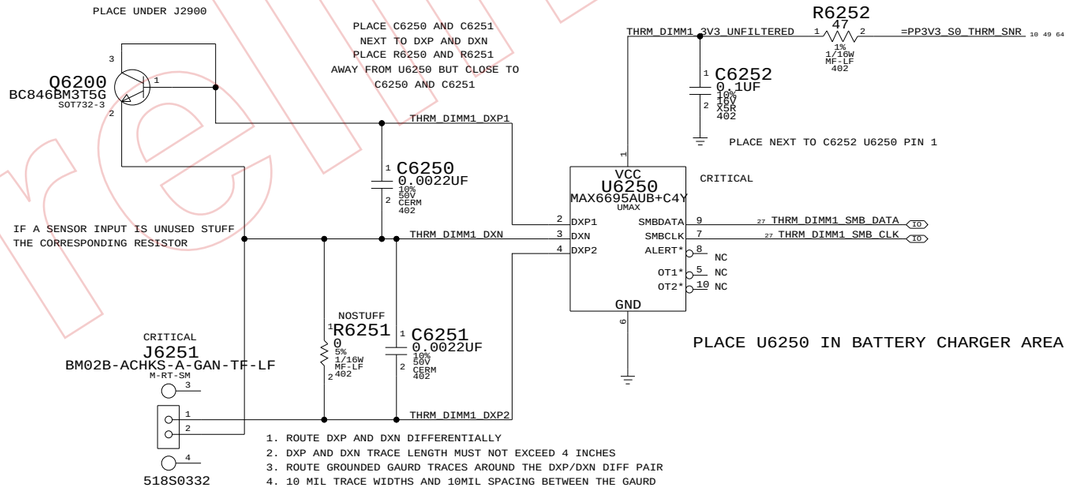
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 61 OF 108	

DIMM0 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452
AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

DIMM1 TEMPERATURE ZONE



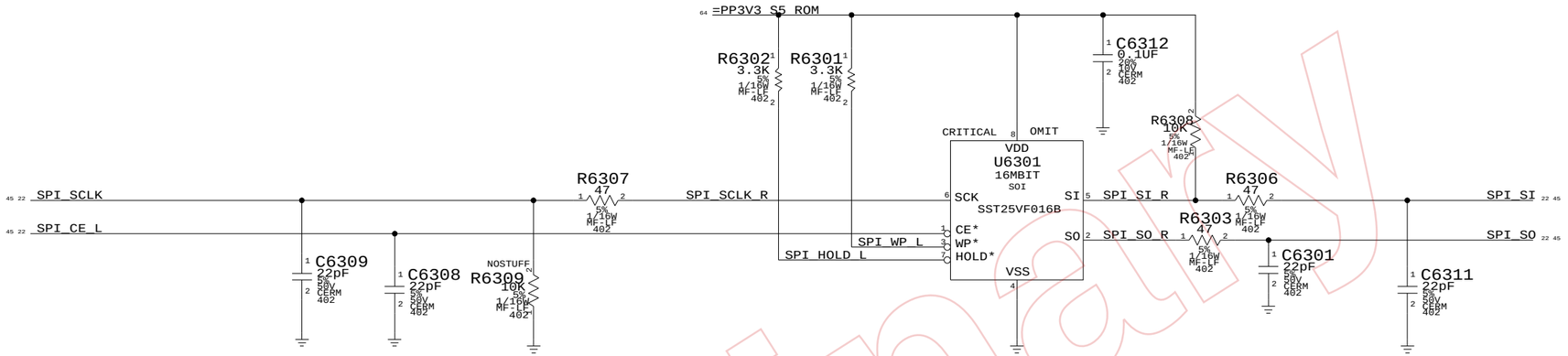
NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452
AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

TEMPERATURE SENSE

SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 62 OF 108	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

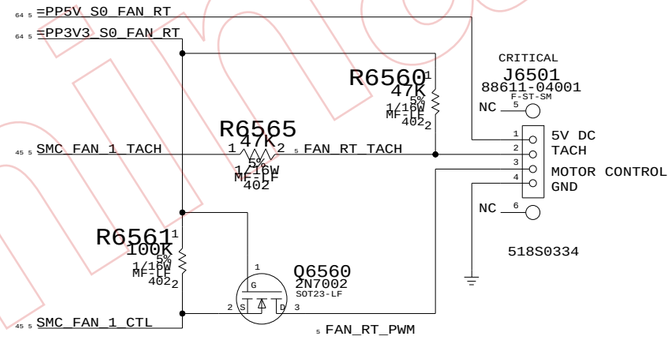
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 63 OF 108	



Fan

SYNC_MASTER=ENET SYNC_DATE=11/10/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 65 OF 108	

PAGE NOTES

INPUT

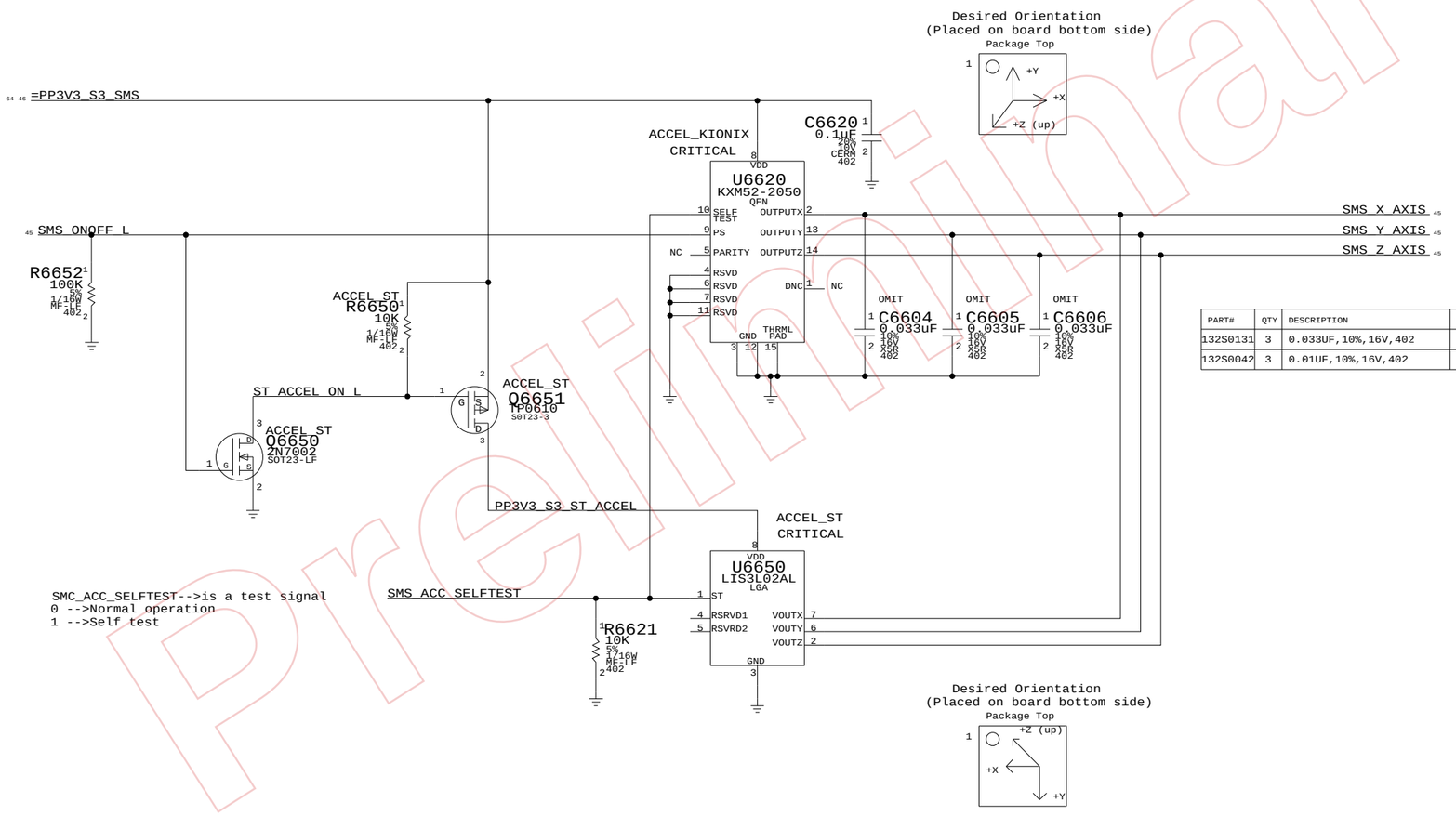
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

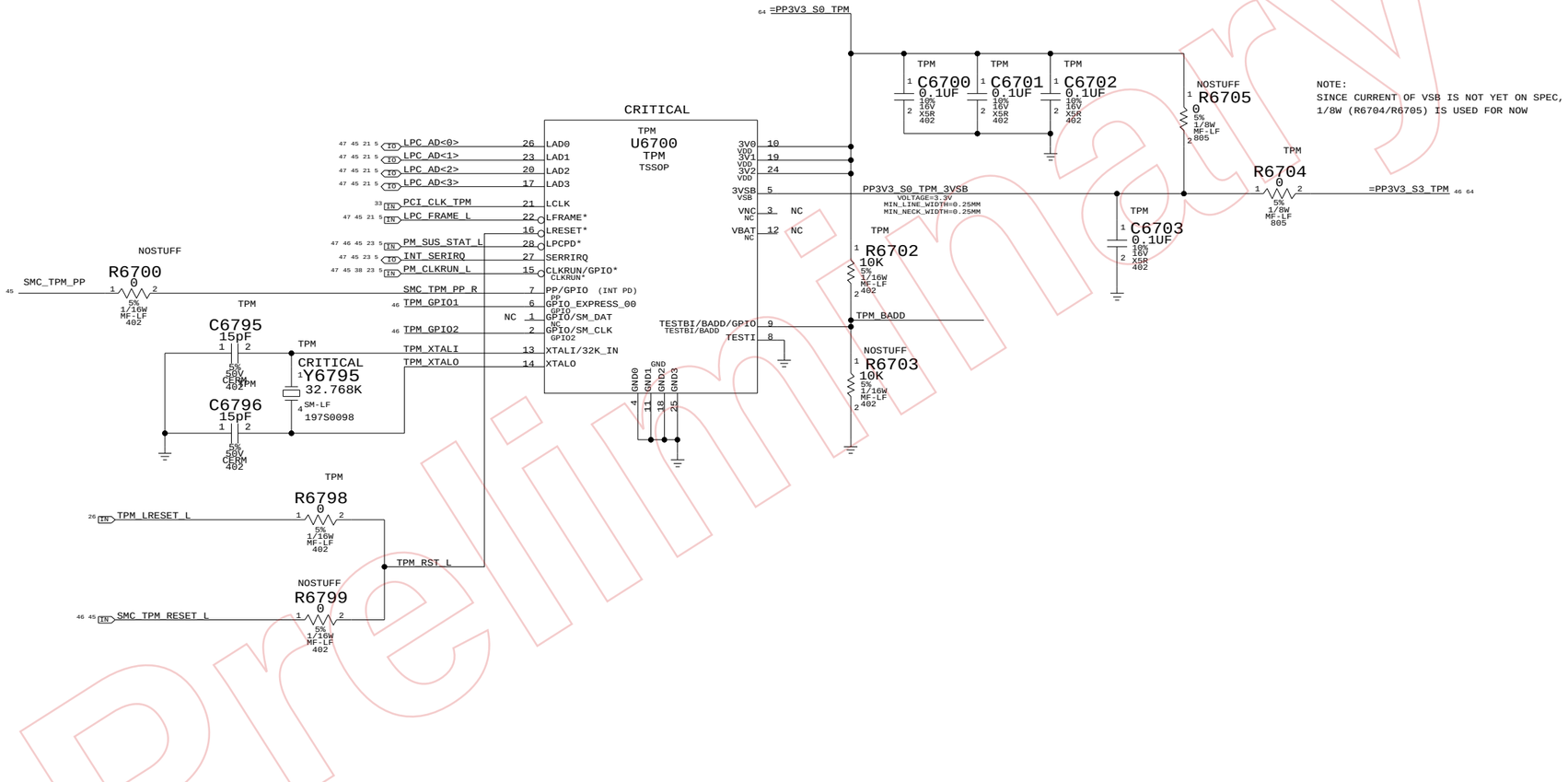
SMS

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE NONE SHT 66 OF 108



TPM

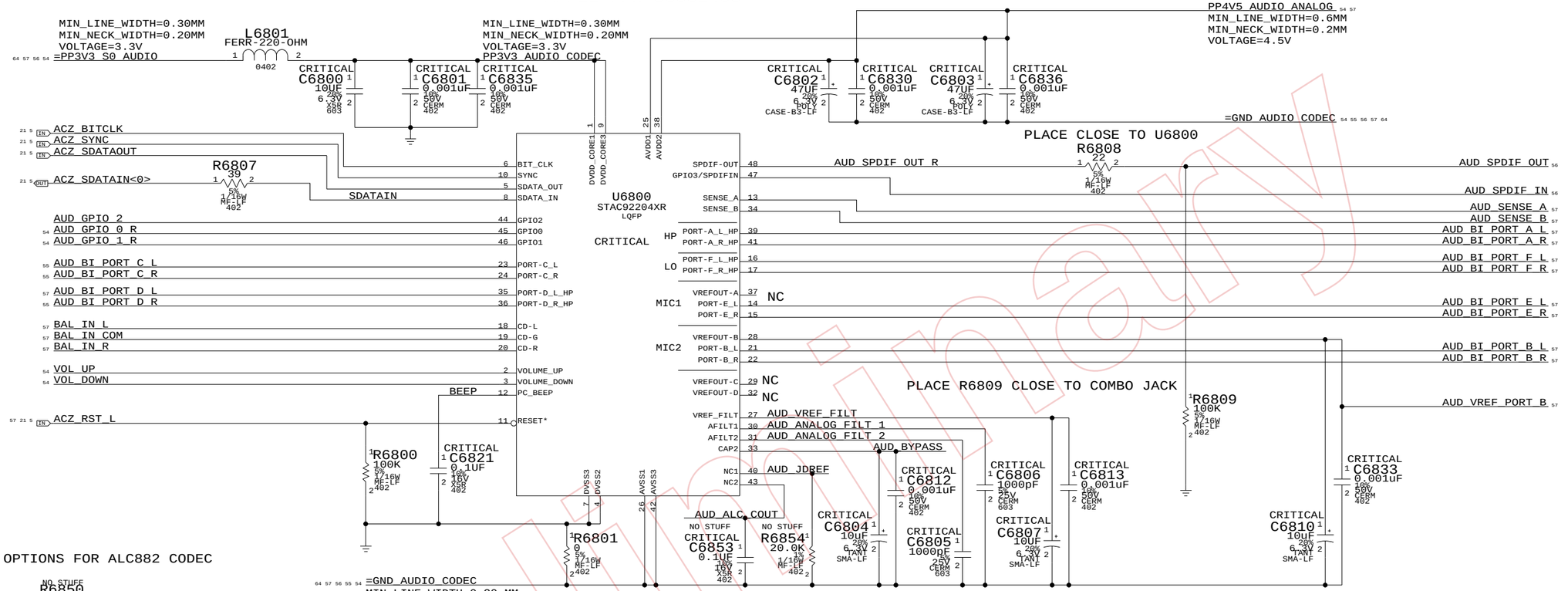
SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE COMPUTER INC.

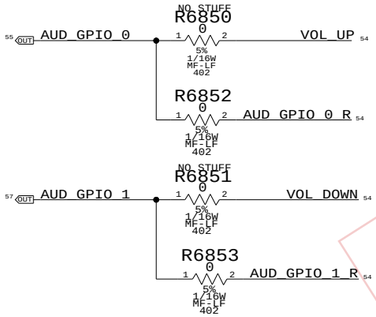
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 67 OF 108	

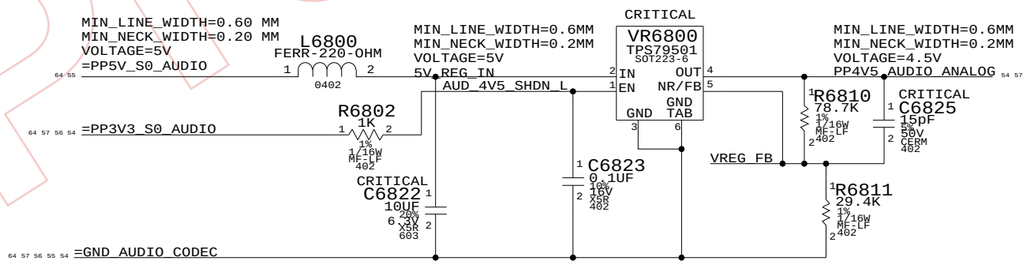
AUDIO CODEC

APPLE P/N 353S1458



STUFFING OPTIONS FOR ALC882 CODEC





USING DC OFFSET SCREENED PART AS PRIMARY OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1345	353S1458	?	U6800	DC OFFSET SCREEN PRTS

4.5V POWER SUPPLY FOR CODEC

AUDIO: CODEC

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

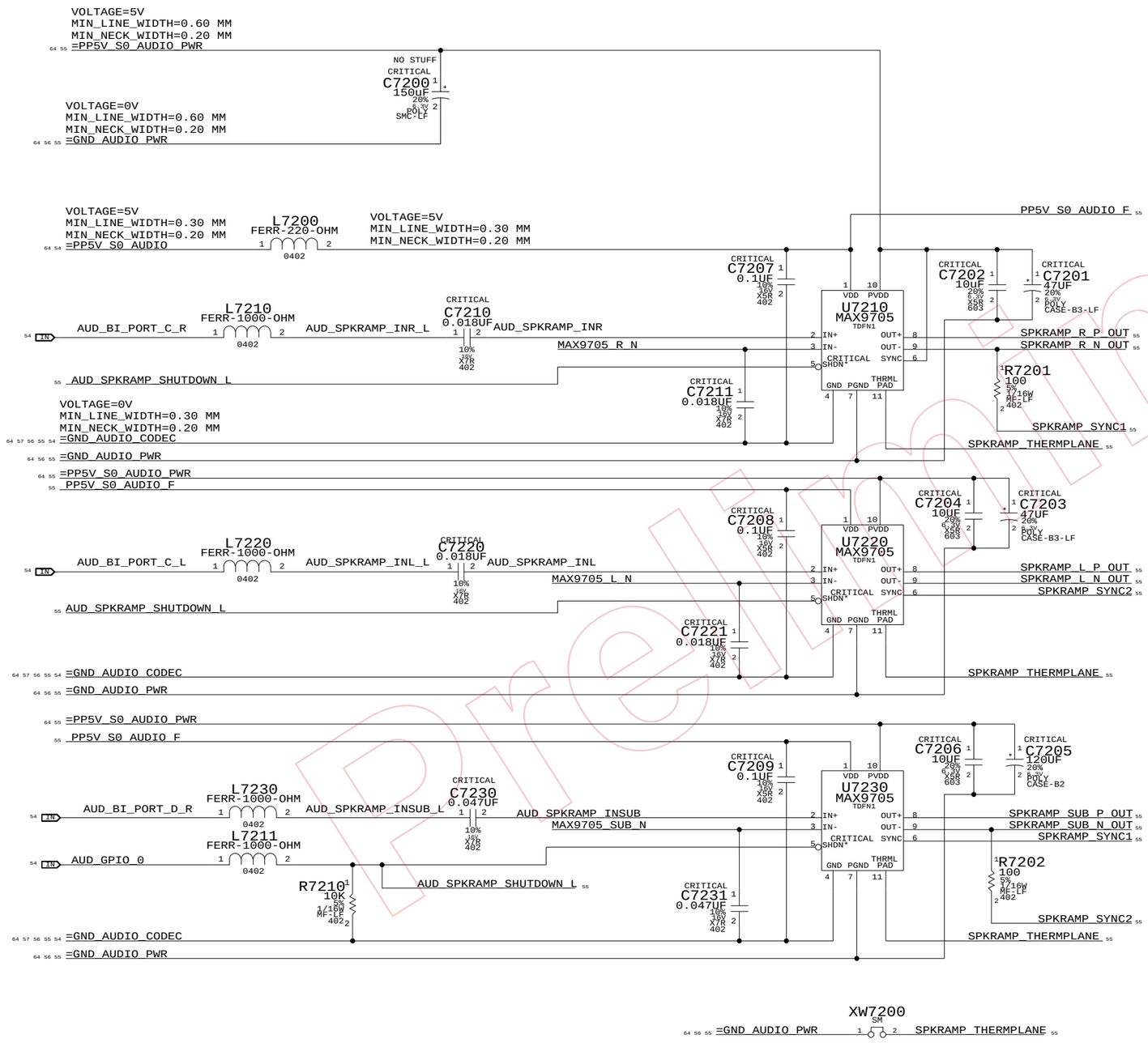
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

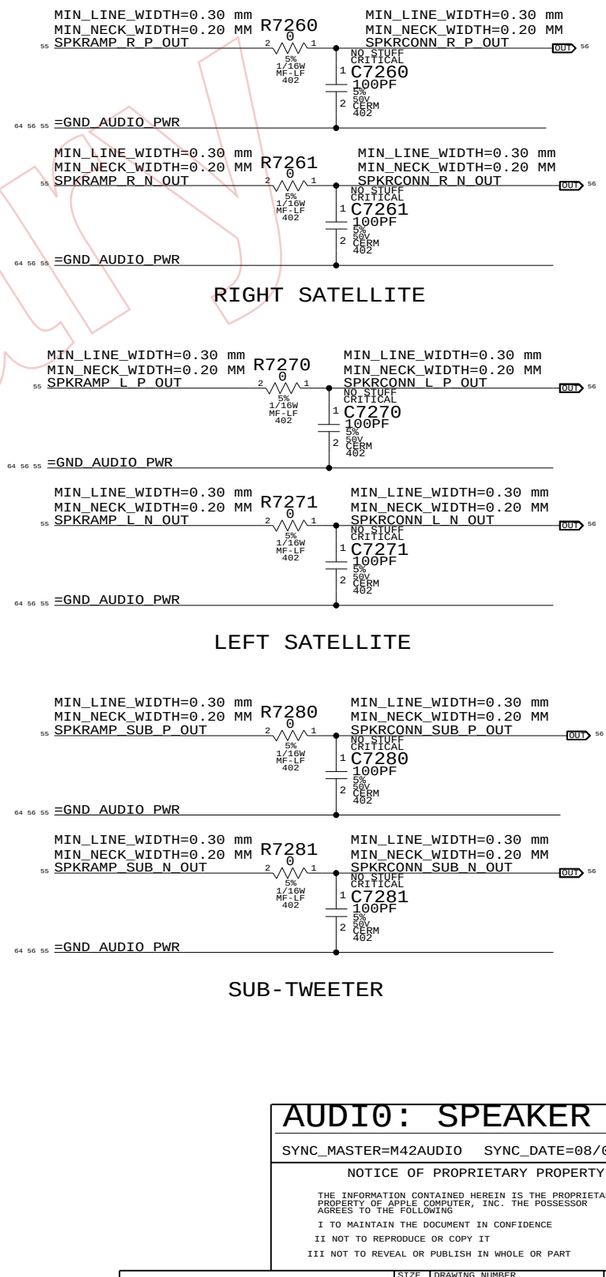
SCALE: NONE SHT 68 OF 108

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 442 Hz < FC < 736 Hz
SUB 169 Hz < FC < 282 Hz



SPEAKER OUTPUT EMI FILTERS



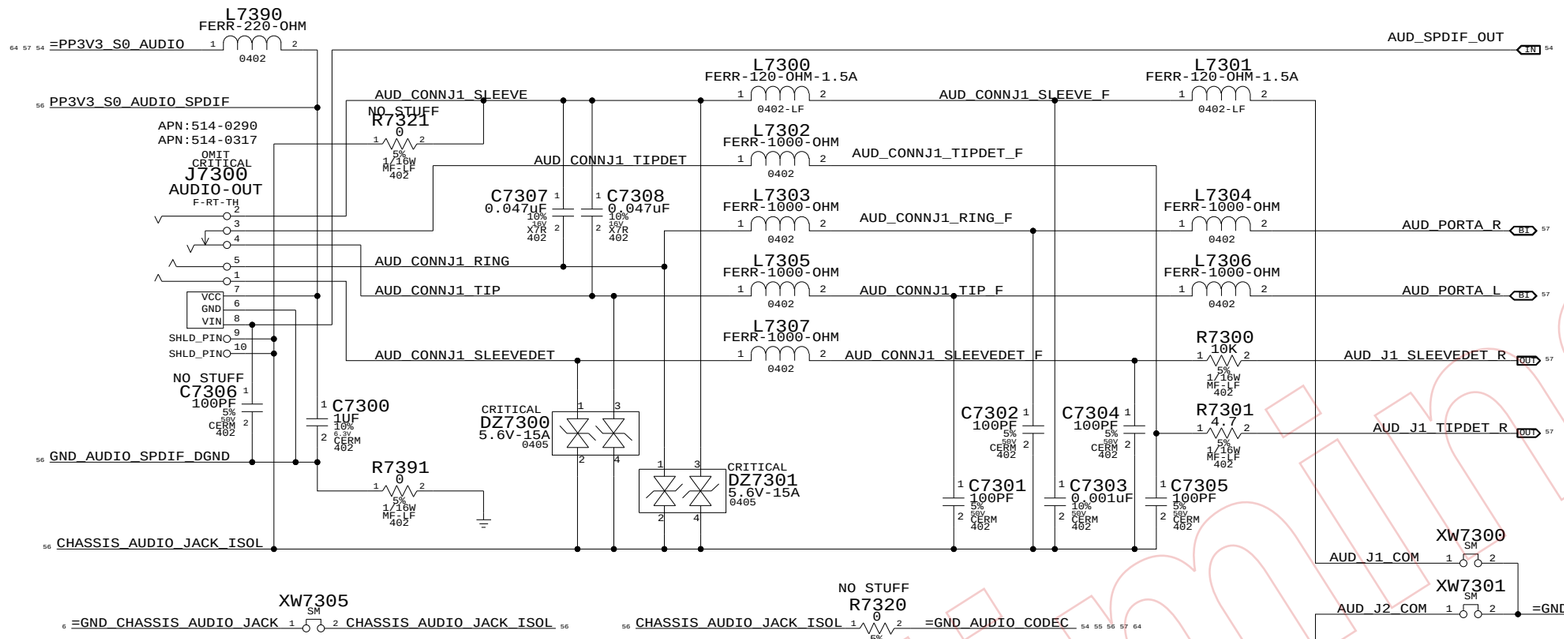
AUDIO: SPEAKER AMP

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

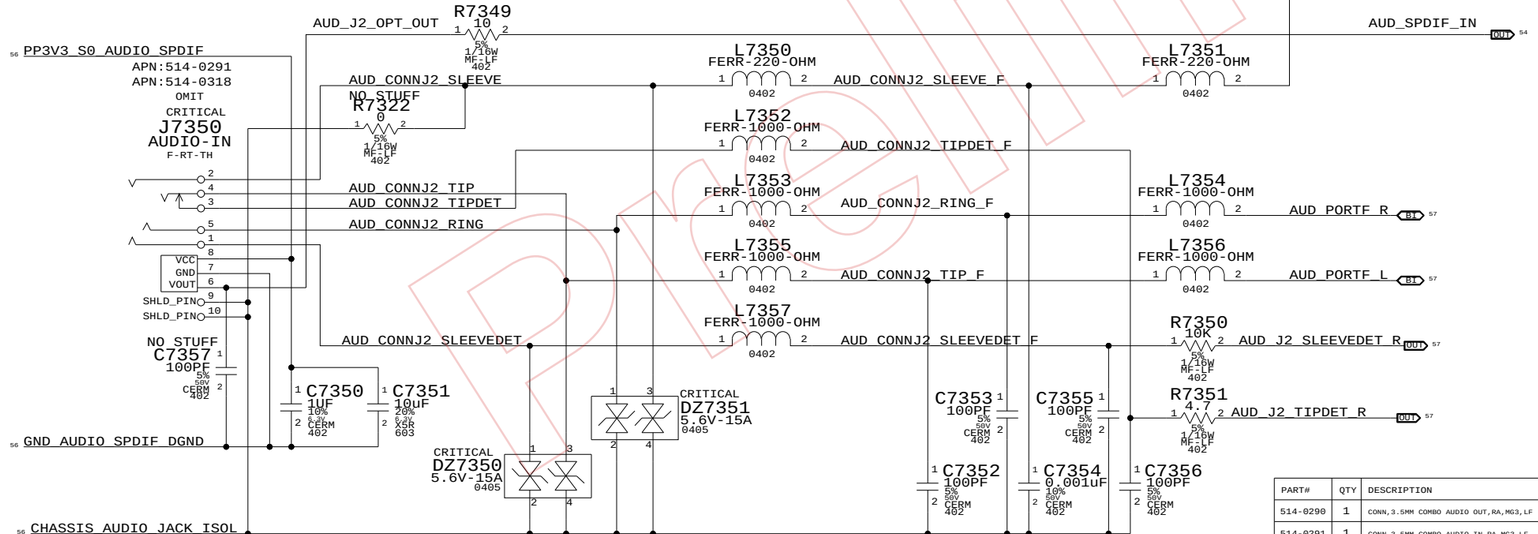
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 72 OF 108	

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

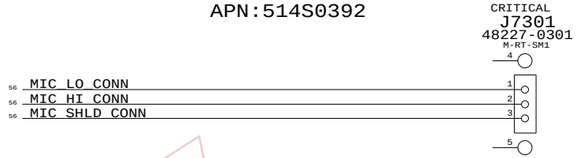


AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



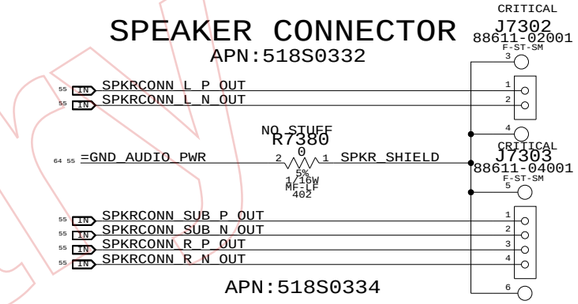
MIC CONNECTOR

APN:514S0392



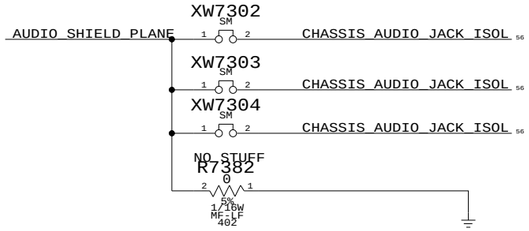
SPEAKER CONNECTOR

APN:518S0332

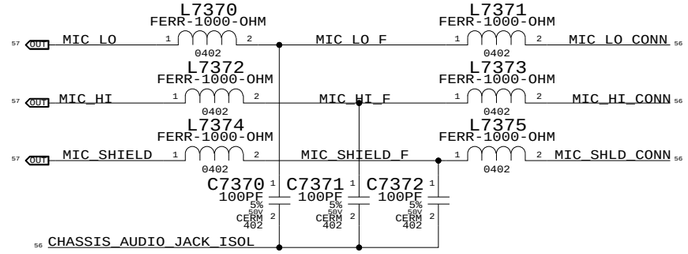


APN:518S0334

AUDIO SHIELD FILL



MIC EMI FILTER



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0290	1	CONN,3.5MM COMBO AUDIO OUT,RA,MG3,LF	J7300	CRITICAL	NORMAL
514-0291	1	CONN,3.5MM COMBO AUDIO IN,RA,MG3,LF	J7350	CRITICAL	NORMAL
514-0317	1	CONN,3.5MM COMBO AUDIO OUT,RA,BLACK,LF	J7300	CRITICAL	FANCY
514-0318	1	CONN,3.5MM COMBO AUDIO IN,RA,BLACK,LF	J7350	CRITICAL	FANCY

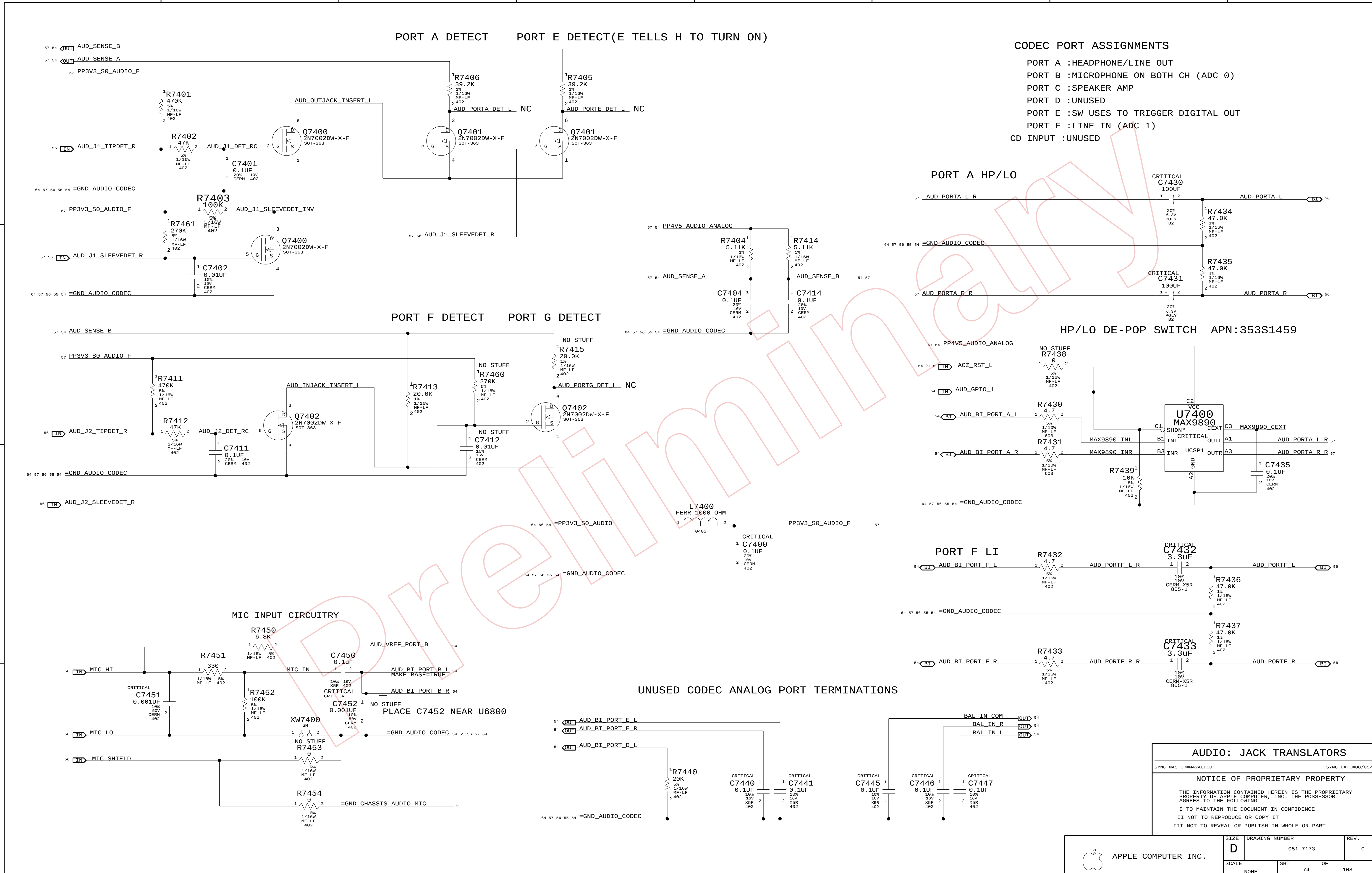
AUDIO: JACK

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	73	108


PORT A DETECT
PORT E DETECT(E TELLS H TO TURN ON)
CODEC PORT ASSIGNMENTS
PORT A :HEADPHONE/LINE OUT
PORT B :MICROPHONE ON BOTH CH (ADC 0)
PORT C :SPEAKER AMP
PORT D :UNUSED
PORT E :SW USES TO TRIGGER DIGITAL OUT
PORT F :LINE IN (ADC 1)
CD INPUT :UNUSED
PORT A HP/LO
PORT F DETECT
PORT G DETECT
HP/LO DE-POP SWITCH APN:353S1459
PORT F LI
MIC INPUT CIRCUITRY
PLACE C7452 NEAR U6800
UNUSED CODEC ANALOG PORT TERMINATIONS
AUD_SENSE_B
AUD_SENSE_A
PP3V3_S0_AUDIO_F
AUD_J1_TIPDET_R
AUD_J1_DET_RC
AUD_OUTJACK_INSERT_L
AUD_PORTA_DET_L NC
AUD_PORTE_DET_L NC
=GND_AUDIO_CODEC
AUD_J1_SLEEVEDET_INV
AUD_J1_SLEEVEDET_R
AUD_J2_TIPDET_R
AUD_J2_DET_RC
AUD_INJACK_INSERT_L
AUD_PORTG_DET_L NC
AUD_J2_SLEEVEDET_R
PP4V5_AUDIO_ANALOG
AUD_PORTA_L_R
AUD_PORTA_L
AUD_PORTA_R_R
AUD_PORTA_R
ACZ_RST_L
AUD_GPIO_1
AUD_BI_PORT_A_L
AUD_BI_PORT_A_R
MAX9890_INL
MAX9890_INR
MAX9890_CEXT
U7400
MAX9890
=PP3V3_S0_AUDIO
L7400
FERR-1000-OHM
PP3V3_S0_AUDIO_F
AUD_BI_PORT_F_L
AUD_PORTF_L_R
AUD_PORTF_L
AUD_BI_PORT_F_R
AUD_PORTF_R_R
AUD_PORTF_R
MIC_HI
MIC_IN
AUD_VREF_PORT_B
AUD_BI_PORT_B_L
MAKE_BASE=TRUE
AUD_BI_PORT_B_R
MIC_LO
MIC_SHIELD
=GND_CHASSIS_AUDIO_MIC
AUD_BI_PORT_E_L
AUD_BI_PORT_E_R
AUD_BI_PORT_D_L
BAL_IN_COM
BAL_IN_R
BAL_IN_L
Preliminary

AUDIO: JACK TRANSLATORS

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE NONE	SHT 74	OF 108

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7501,C7508	KEMET T520V336M016ATE045?650
128S0093	128S0092	?	C7509,C7517	KEMET T520V336M016ATE045?650

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

R0802/R0803 **on the CPU page** protect the IMVP6 if the CPU is not installed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCORE REGULATOR

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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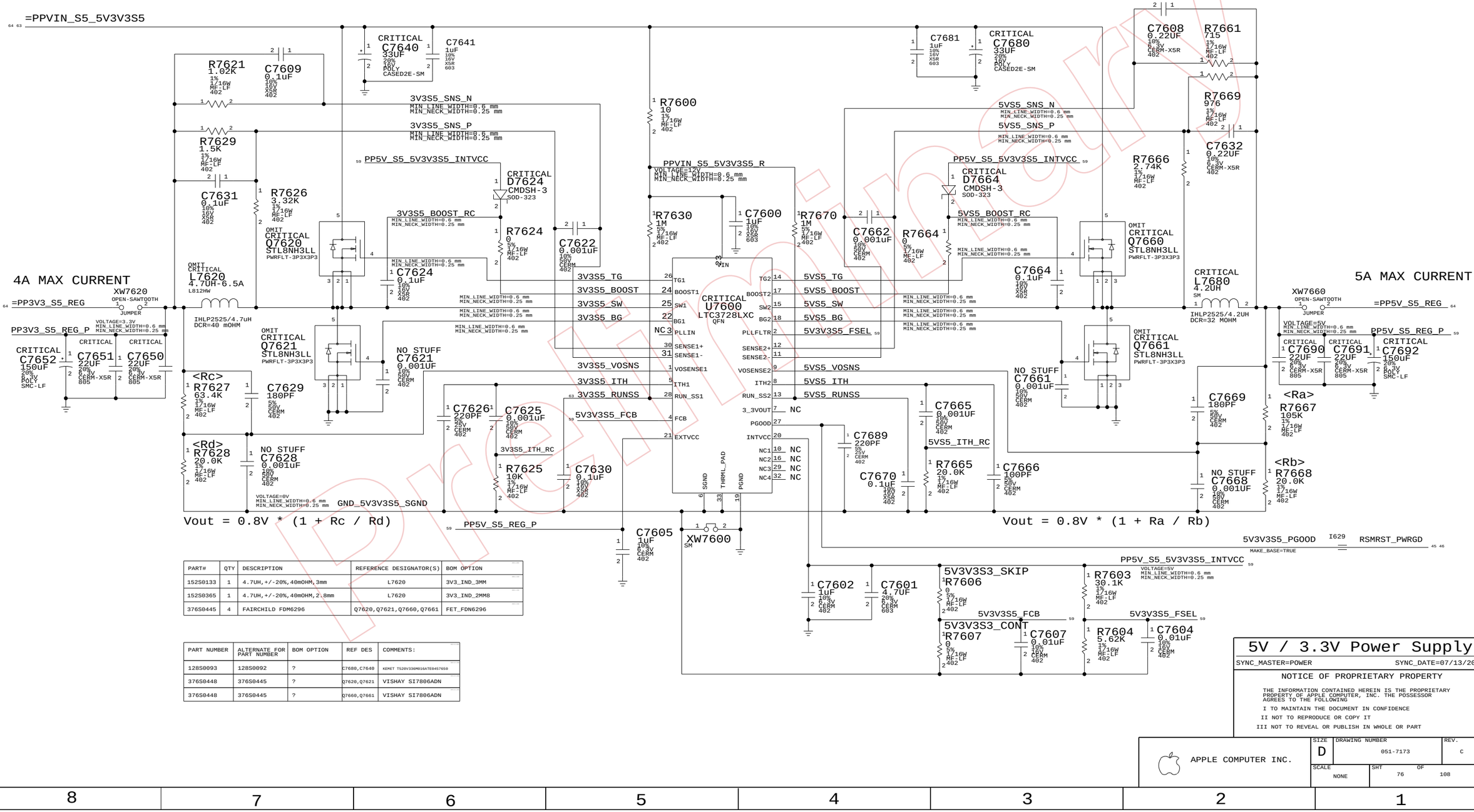
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE	SHT	OF
NONE	75	108

5V/3.3V POWER SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0133	1	4.7UH,+/-20%,40mOHM,3mm	L7620	3V3_IND_3MM
152S0365	1	4.7UH,+/-20%,40mOHM,2.8mm	L7620	3V3_IND_2MM8
376S0445	4	FAIRCHILD FDM6296	Q7620,Q7621,Q7660,Q7661	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7680,C7640	KEMET T520V336M016ATE0457650
376S0448	376S0445	?	Q7620,Q7621	VISHAY SI7806ADN
376S0448	376S0445	?	Q7660,Q7661	VISHAY SI7806ADN

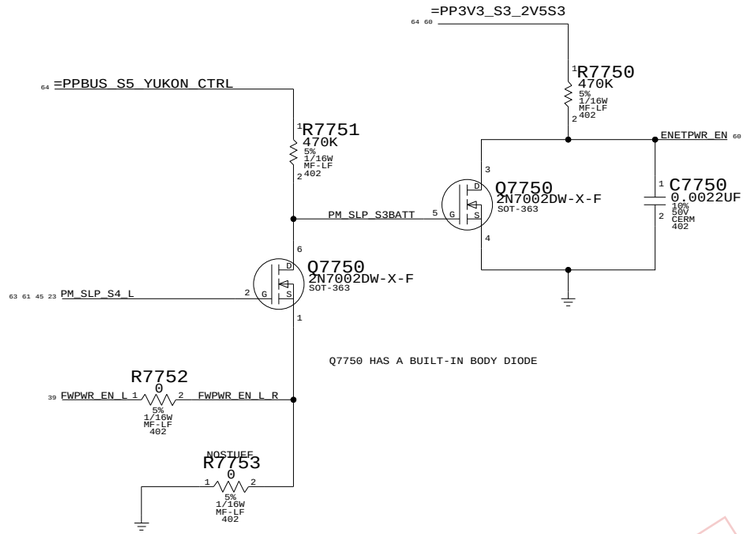
5V / 3.3V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 76 OF 108	

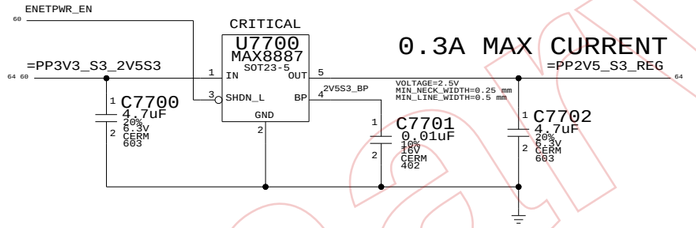
YUKON POWER CONTROL



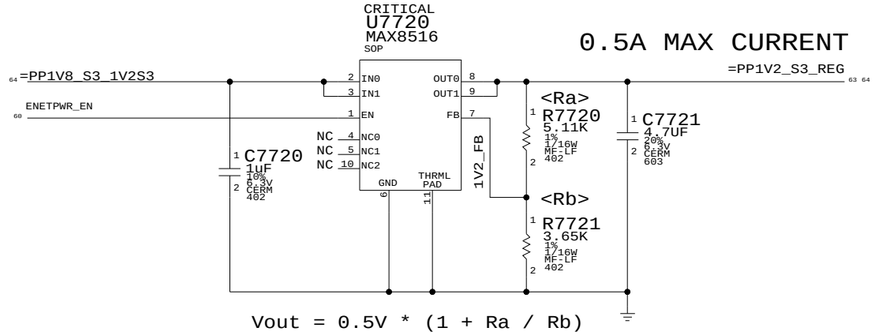
NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 | S0	~S0 | ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L

2.5V REGULATORS



1.2V REGULATOR



Vout = 0.5V * (1 + Ra / Rb)

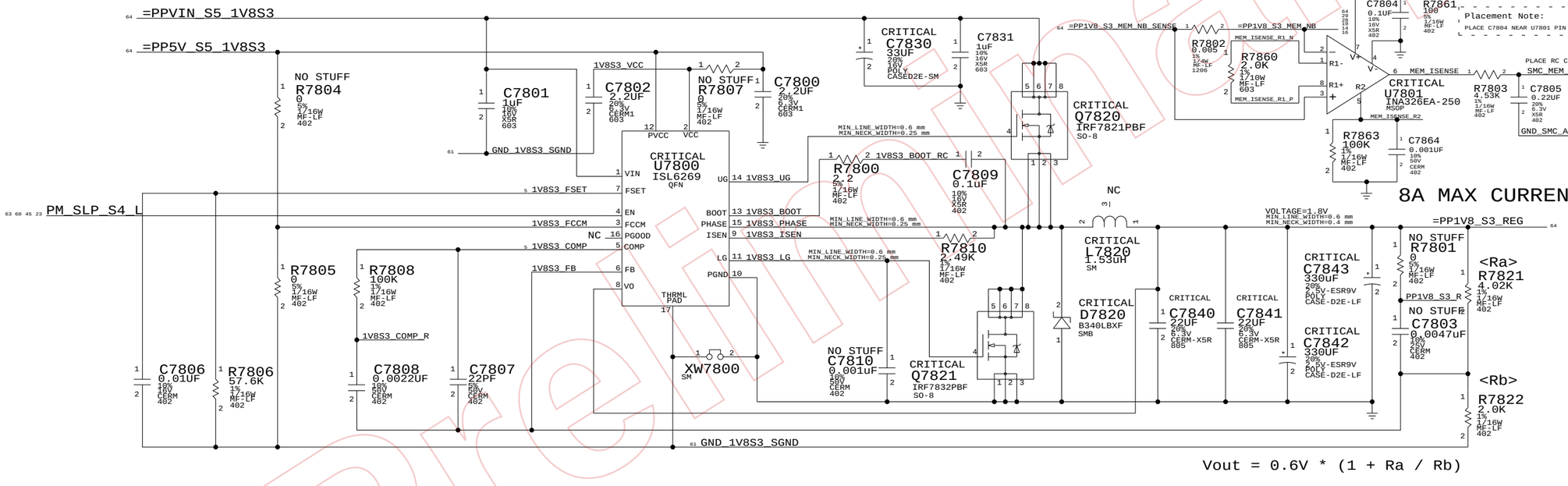
2.5V/1.2V Regulator

SYNC_MASTER=ENET SYNC_DATE=12/06/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 77 OF 108	

1.8V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	KEMET T520V336M016ATE045760

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331ER
128S0095	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331XE

1.8V Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 78 OF 108	

1.5V/1.05V POWER SUPPLY

=PPVIN_S5_1V51V05S0

CRITICAL C7940 33UF 20% 16V POLY CASED2E-SM
C7941 1uF 10% 16V X5R 603
C7981 1uF 10% 16V X5R 603
CRITICAL C7980 33UF 20% 16V POLY CASED2E-SM

R7921 1.07K 1% 1/16W MF-LF 402
C7909 0.22UF 10% 6.3V CERM-X5R 402
R7961 523 1% 1/16W MF-LF 402
C7908 0.22UF 10% 6.3V CERM-X5R 402

1V5S0_SNS_N
1V5S0_SNS_P
1V05S0_SNS_N
1V05S0_SNS_P
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

R7929 4.53K 1% 1/16W MF-LF 402
C7931 0.22UF 10% 6.3V CERM-X5R 402
R7926 1.43K 1% 1/16W MF-LF 402

PP5V_S5_1V51V05S0_INTVCC
CRITICAL D7924 CMDSH-3 SOD-323
CRITICAL D7964 CMDSH-3 SOD-323
C7932 0.22UF 10% 6.3V CERM-X5R 402
R7966 698 1% 1/16W MF-LF 402
R7969 2.1K 1% 1/16W MF-LF 402

1V5S0_BOOST_RC
1V05S0_BOOST_RC
R7924 0 5% 1/16W MF-LF 402
C7922 0.001uF 10% 50V CERM 402
C7924 0.1uF 10% 16V X5R 402

R7900 10 1% 1/16W MF-LF 402
PPVIN_S5_1V51V05S0_R
VOLTAGE=12V
R7930 1M 5% 1/16W MF-LF 402
C7900 1uF 10% 16V X5R 603
R7970 1M 5% 1/16W MF-LF 402
C7962 0.001uF 10% 50V CERM 402
R7964 0 5% 1/16W MF-LF 402
C7964 0.1uF 10% 16V X5R 402

VIN
1V5S0_TG
1V5S0_BOOST
1V5S0_SW
1V5S0_BG
1V5S0_VOSNS
1V5S0_ITH
1V5S0_RUNSS
1V51V05S0_FCB
1V05S0_TG
1V05S0_BOOST
1V05S0_SW
1V05S0_BG
1V51V05S0_FSEL
1V05S0_VOSNS
1V05S0_ITH
1V05S0_RUNSS

CRITICAL U7900 LTC3728LXC QFN
TG1 26
BOOST1 24
SW1 25
BG1 22
NC 3 PLLIN
SENSE1+ 30
SENSE1- 31
VOSENSE1 1
ITH1 5
RUN_SS1 28
FCB 4
EXTVCC 21
TG2 14
BOOST2 17
SW2 15
BG2 18
PLLFLTR 2
SENSE2+ 12
SENSE2- 11
VOSENSE2 9
ITH2 8
RUN_SS2 13
3_3VOUT 7 NC
PGOOD 27
INTVCC 20
NC1 10 NC
NC2 16 NC
NC3 29 NC
NC4 32 NC
SGND 6
THRML_PAD 33
PGND 19

CRITICAL Q7960 IRF7821PBF SO-8
CRITICAL Q7961 IRF7832PBF SO-8
CRITICAL D7961 B240-X-F SMB

6A MAX CURRENT
=PP1V5_S0_REG
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
PP1V5_S0_REG_R
XW7920 OPEN-SAWTOOTH JUMPER
CRITICAL C7950 22UF 20% 6.3V CERM-X5R 805
CRITICAL C7952 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF

CRITICAL L7920 2.8UH SM
Dtdc/2.8uH DCR=10.7 mOhm
CRITICAL L7960 1.53uH SM
PCI-1050 DCR=0.3 mOHM

CRITICAL Q7920 IRF7821PBF SO-8
CRITICAL Q7921 IRF7832PBF SO-8
CRITICAL D7921 B240-X-F SMB
NO STUFF C7921 0.001uF 10% 50V CERM 402
NO STUFF C7961 0.001uF 10% 50V CERM 402

8A MAX CURRENT
=PP1V05_S0_REG
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
CRITICAL C7992 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF

<Rc> R7927 17.8K 1% 1/16W MF-LF 402
C7929 180PF 5% 50V CERM 402
<Rd> R7928 20.0K 1% 1/16W MF-LF 402
NO STUFF C7928 0.001UF 10% 50V CERM 402

C7926 47pF 5% 50V CERM 402
C7925 470pF 10% 50V CERM 402
1V5S0_ITH_RC
R7925 24.3K 1% 1/16W MF-LF 402
C7930 0.1uF 10% 16V X5R 402

C7965 330PF 10% 50V CERM 402
1V05S0_ITH_RC
R7965 33.2K 1% 1/16W MF-LF 402
C7966 47PF 5% 50V CERM 402
C7969 0.0022UF 10% 50V CERM 402
<Ra> R7967 6.34K 1% 1/16W MF-LF 402
NO STUFF C7968 0.001uF 10% 50V CERM 402
<Rb> R7968 20.0K 1% 1/16W MF-LF 402

C7989 220PF 5% 25V CERM 402
C7970 0.1uF 10% 16V X5R 402

Vout = 0.8V * (1 + Rc / Rd)
GND_1V51V05S0_SGND
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
Vout = 0.8V * (1 + Ra / Rb)
=PP3V3_S0_1V51V05S0
R7901 10K 5% 1/16W MF-LF 402
1V51V05S0_PGOOD

=PP5V_1V51V05S0_VCC
C7905 1uF 10% 6.3V CERM 402
XW7900 SM

C7902 1uF 10% 6.3V CERM 402
C7901 4.7UF 20% 6.3V CERM 603
1V51V05S0_SKIP
R7906 0 5% 1/16W MF-LF 402
1V51V05S0_CONT
R7907 0 5% 1/16W MF-LF 402
C7907 0.01uF 10% 16V CERM 402
R7903 30.1K 1% 1/16W MF-LF 402
R7904 5.62K 1% 1/16W MF-LF 402
C7904 0.01uF 10% 16V CERM 402
PP5V_S5_1V51V05S0_INTVCC
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

=PP1V05_S0_CPU_NB_SENSE
R7902 0.002 1% 1/4W MF-LF 1206
=PP1V05_S0_CPU_NB
C7990 22UF 20% 6.3V CERM-X5R 805
C7991 22UF 20% 6.3V CERM-X5R 805
NB_ISENSE_VCC
=PP3V3_S0_PDCISENS
C7903 0.1UF 10% 16V X5R 402
R7990 100 1% 1/16W MF-LF 402
Placement Note:
PLACE C7903 NEAR U7901 PIN 7
PLACE RC CLOSE TO SMC
CRITICAL U7901 INA326EA-250 MSOP
NB_ISENSE_R1_N
NB_ISENSE_R1_P
NB_ISENSE_R2
R7992 2.0K 1% 1/16W MF-LF 603
R7991 100K 1% 1/16W MF-LF 402
C7999 0.001UF 10% 50V CERM 402
NB_ISENSE
R7905 4.53K 1% 1/16W MF-LF 402
C7906 0.22UF 20% 6.3V X5R 402
SMC_NB_ISENSE
GND_SMC_AVSS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7980,C7940	KEMET T520V336M016ATE0457650

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7952,C7992	PANASONIC EEFSX0D331ER
128S0095	128S0060	?	C7952,C7992	PANASONIC EEFSX0D331XE

1.5V / 1.05V Power Supply
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

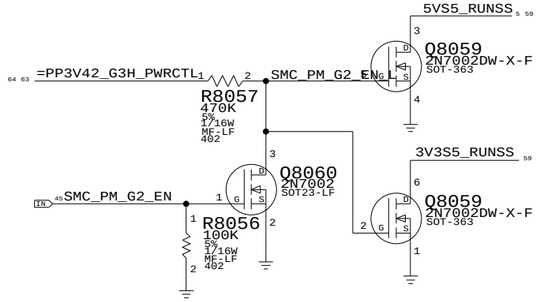
APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-7173 | REV. C
SCALE NONE | SHT 79 OF 108

POWER CONTROL SIGNALS

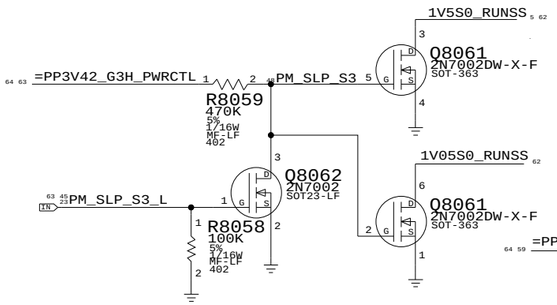
These rails are monitored by LTC2908

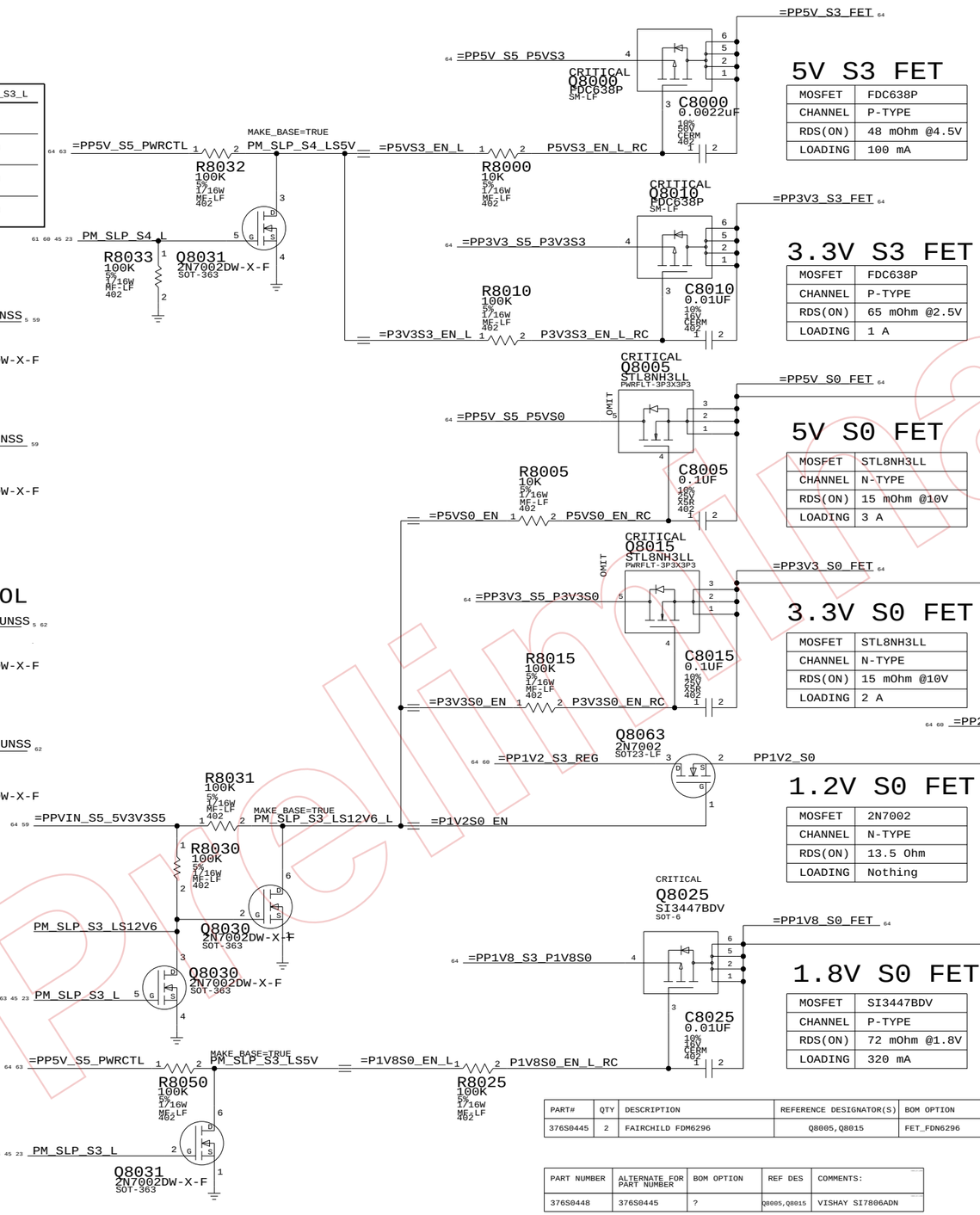
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V/3.3V S5 RUN/SS CONTROL



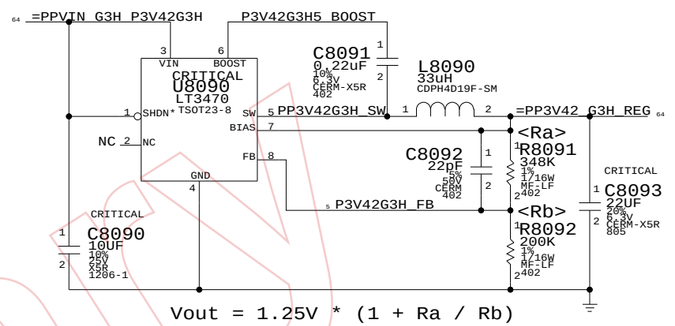
1.5V/1.05V S0 RUN/SS CONTROL



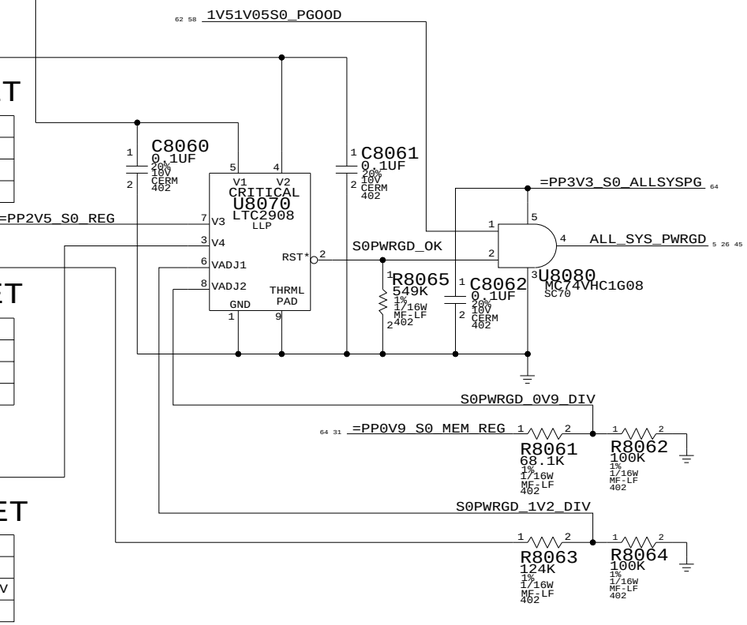


3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005,Q8015	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005,Q8015	VISHAY SI7806ADN

S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE NONE SHT 80 OF 108

"S0" RAILS ONLY ON IN RUN

PPVCORE_CPU_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(REGULATOR OUTPUT CPU VCORE PWR) =PPVOUT_S0_IMVP6_REG (58)
(CPU VCORE PWR) =PPVCORE_S0_CPU (8 9 48)

PP0V9_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(LDO OUTPUT 0.9V PWR) =PP0V9_S0_MEM_REG (63 31)
(DDR2 TERMINATION 0.9V PWR) =PP0V9_S0_MEM_TERM (30)

PP1V05_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.05V

(REGULATOR OUTPUT 1.05V PWR) =PP1V05_S0_REG (62 5)
(ICH CPU I/O 1.05V PWR) =PP1V05_S0_SB_CPU_IO (21 24 25)
(ICH VCORE 1.05V PWR) =PPVCORE_S0_SB (24 25)
=PP1V05_S0_CPU_NB_SENSE (62)

PP1V05_S0_CPU_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.05V

=PP1V05_S0_CPU_NB (62)
(MCH CORE 1.05V PWR) =PPVCORE_S0_NB (16 19)
(CPU FSB 1.05V PWR) =PP1V05_S0_CPU (7 8 9 11)
(MCH FSB 1.05V PWR) =PP1V05_S0_FSB_NB (12 19 33)
=PP1V05_S0_NB_VTT (17 19)
(MCH FSB 1.05V PWR) =PP1V05_S0_NB (19)

PP1V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.5V

(REGULATOR OUTPUT 1.5V PWR) =PP1V5_S0_REG (62)
(CPU AVDD 1.5V PWR) =PP1V5_S0_CPU (8 9)
(MCH PCIE GRAPHICS O/P COMPENSATION 1.5V PWR) =PP1V5_S0_NB_PCIE (13 19)
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V) =PP1V5_S0_NB_VCCAUX (16 17 19)
(MCH DIGITAL DIVIDER IN HMPLL 1.5V PWR) =PP1V5_S0_NB_VCCD_HMPLL (17 19)
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS (17 19)
(HOST/MEMORY PLL 1.5V PWR) =PP1V5_S0_NB_PLL (19)
=PP1V5_S0_NB (19)
(MCH TVDAC DEDICATED/QUIET PWR 1.5V) =PP1V5_S0_NB_TVDAC (19)
(MCH 3GIO[PCIE/DMI] 1.5V PWR) =PP1V5_S0_NB_3G (19)
(MCH 3GIO PLL 1.5V PWR) =PP1V5_S0_NB_3GPLL (19)
(ICH LOGIC&IO[ARX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ARX (24 25)
(ICH SATA PLL 1.5V PWR) =PP1V5_S0_SB_VCCSATAPLL (24 25)
(ICH LOGIC&IO[ATX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ATX (24 25)
(ICH USB PLL 1.5V PWR) =PP1V5_S0_SB_VCCUSBPLL (24 25)
(ICH USB CORE 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_USB_CORE (24 25)
(ICH LOGIC&IO 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A (24 25)
=PP1V5_S0_SB (25)
(WIRELESS CARD 1.5V PWR) =PP1V5_S0_AIRPORT (43)

PP1V8_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

(COME FROM S3 TO S0 MOSFET) =PP1V8_S0_FET (63)
(DDR2 TERMINATION REGULATOR 1.8V SWITCH PWR) =PP1V8_S0_TMDS (68)
(TMDS 1.8V PWR)

PP2V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(COME FROM S3 TO S0 MOSFET) =PP2V5_S0_REG (63 60)
(MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC (17 19)
(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS (17 19)
(MCH PCIE/DMI BAND GAP 2.5V PWR) =PP2V5_S0_NB_VCCA_3GBG (17 19)
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS (17 19)
(MCH CRTDAC ANALOG 2.5V PWR) =PP2V5_S0_NB_CRTDAC (19)
(TMDS 2.5V PWR) =PP2V5_S0_TMDS (68)
=PP2V5_S0_NB_DISP_PLL (19)

PP3V3_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

(COME FROM S5 TO S0 MOSFET) =PP3V3_S0_FET (63)
(MCH HV BUFFER 3.3V PWR) =PP3V3_S0_NB_VCC_HV (17 19)
=PP3V3_S0_SB (22 25 34)
(ICH GPIO PULLS 3.3V PWR) =PP3V3_S0_SB_GPIO (21 23)
(ICH IO BUFFER 3.3V PWR) =PP3V3_S0_SB_VCC3_3 (24 25)
(ICH PCI I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_PCI (24 25)
(ICH IDE I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_IDE (24 25)
(ICH PCI PULLS 3.3V PWR) =PP3V3_S0_SB_PCI (26)
(ICH PM PULLS 3.3V PWR) =PP3V3_S0_SB_PM (26)
(PATA PULLS 3.3V PWR) =PP3V3_S0_PATA (34)
(SATA 3.3V PWR) =PP3V3_S0_SMC_LS (46)
(MCH PULLS 3.3V PWR) =PP3V3_S0_NB (14 19 20)
(ICH LAN I/F 3.3V PWR, NEED TO CHECK INTEL) =PP3V3_S0_SB_VCCLAN3_3 (24 25)
(ICH INTEL HDA CORE 3.3V PWR) =PP3V3_S0_SB_3V3_1V5_VCCHDA (24 25)
(DIMM SPD 3.3V PWR) =PPSPD_S0_MEM (28 29)
(CLOCK GENERATOR 3.3V PWR) =PP3V3_S0_CK410 (32)
(WIRELESS CARD 3.3V PWR) =PP3V3_S0_AIRPORT (43)
(TPM 3.3V PWR) =PP3V3_S0_TPM (53)
(AUDIO 3.3V PWR) =PP3V3_S0_AUDIO (54 56 57)
(TMDS 3.3V PWR) =PP3V3_S0_TMDS (68 69)
(CPU THERMAL SENSOR 3.3V PWR) =PP3V3_S0_THRM_SNR (10 49)
(ISL6262 3V3) =PP3V3_S0_IMVP6 (58)
=PP3V3_S0_RSTBUF (26)
=PP3V3_S0_SMBUS_SB (27)
=PP3V3_S0_SMBUS_SMC_0 (27)
=PP3V3_S0_SMBUS_SMC_MLB (27)
=PP3V3_S0_ALLSYSPG (63)
=PP3V3_S0_FAN_RT (5 51)
=PP3V3_S0_LCD (67)
=PP3V3_S0_PBATTISENS (66)
=PP3V3_S0_PDCISENS (62 66)
=PP3V3_S0_CPUPOWER (48)
=PP3V3_S0_SMBUS_SMC_BSA (27)
=PP3V3_S0_1V51V05S0 (62)
=PP3V3_S0_2V5S0 (60)
=PP3V3_S0_FW (39)
(FIREWIRE DIGITAL 3.3V PWR) =PP3V3_S0_ENET (36)

PP5V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V

(COME FROM S5 TO S0 MOSFET) =PP5V_S0_FET (63)
=PP5V_S0_SB (25)
(SATA 5V PWR) =PP5V_S0_SATA (35)
(DDR2 TERMINATION) =PP5V_S0_MEMVTT (31)
(AUDIO 5V PWR) =PP5V_S0_AUDIO (54 55)
(AUDIO SPEAKER 5V PWR) =PP5V_S0_AUDIO_PWR (55)
(LPC DEBUG BOARD 5V PWR) =PP5V_S0_LPCPLUS (5 47)
(MCH TV 3.3V LDO) =PP5V_S0_NB_TVDAC (19)
(ISL6262 VDD) =PP5V_S0_IMVP6 (58)
(LTC3728LXC EXTVCC) =PP5V_1V51V05S0_VCC (62)
(TMDS 5V PWR) =PP5V_S0_TMDS (68 69)
=PP5V_S0_FAN_RT (5 51)
=PP5V_S0_LCD (67)
=PP5V_S0_ISENSECAL (48)

"S3" RAILS
ON IN RUN AND SLEEP

PP1V2_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.32MM
VOLTAGE=1.2V

(LDO OUTPUT 1.2V PWR) =PP1V2_S3_REG (63 60)
(ENET 1.2V PWR) =PP1V2_S3_ENET (36)

PP1V8_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

(REGULATOR OUTPUT 1.8V PWR) =PP1V8_S3_REG (61)
(DDR2 DIMM 1.8V PWR) =PP1V8_S3_MEM (19 28 29)
=PP1V8_S3_P1V8S0 (63)
=PP1V8_S3_MEMVTT (31)
=PP1V8_S3_MEM_NB_SENSE (61)
=PP1V8_S3_1V2S3 (60)

PP1V8_S3_MEM_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

=PP1V8_S3_MEM_NB (61 29 28 19 16 14)
(MCH DDR2 1.8V PWR)

PP2V5_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(REGULATOR OUTPUT 2.5V PWR) =PP2V5_S3_REG (60)
(ENET 2.5V PWR) =PP2V5_S3_ENET (36)

PP3V3_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.16 MM
VOLTAGE=3.3V

(COME FROM S5 TO S3 MOSFET) =PP3V3_S3_FET (63)
=PP3V3_S3_SMBUS_SMC_RMT (27)
(ETHERNET 3.3V PWR) =PP3V3_S3_ENET (36)
(BLUETOOTH 3.3V PWR) =PP3V3_S3_BT (44)
(ACCELEROMETER 3.3V PWR) =PP3V3_S3_SMS (46 52)
(TPM 3.3V SUSPEND PWR) =PP3V3_S3_TPM (46 53)
(TPS62050 VIN) =PP3V3_S3_2V5S3 (60)
(FIREWIRE CHIP PCI SIGNAL INDICATOR) =PP3V3_S3_PCI (38)
=PP3V3_S3_RSTGATE (26)
=PP3V3_S3_AIRPORT_AUX (43)
=PP3V3_S3_FW (38)
=PP3V3_S3_PDCISENS (61)

PP5V_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(COME FROM S5 TO S3 MOSFET) =PP5V_S3_FET (63)
(ISL6269 PVCC)
(SYSTEM LED PWR) =PP5V_S3_SYSLED (35 46)
(USB IO PORT 5V PWR) =PP5V_S3_CAMERA (67)
(USB IR CONTROLLER 5V PWR) =PP5V_S3_IR (41)
=PP5V_S3_GEYSER (40)

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP3V3_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=3.3V

(REGULATOR OUTPUT 3.3V PWR) =PP3V3_S5_REG (59)
=PP3V3_S5_SB (23 25)
(ICH USB CTL PULLS 3.3V PWR) =PP3V3_S5_SB_USB (22)
(ICH PM 3.3V PWR) =PP3V3_S5_SB_PM (11 23 26)
(ICH SUSPEND 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3 (24 25)
(ICH SUSPEND USB 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3_USB (24 25)
(ICH SUSPEND PULLS 3.3V PWR) =PP3V3_S5_SB_IO (22)
(ICH INTEL HDA SUSPEND 3.3V PWR) =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA (24)
(SPI BOOTROM PWR) =PP3V3_S5_ROM (50)
=PP3V3_S5_P3V3S3 (63)
=PP3V3_S5_P3V3S0 (63)
=PP3V3_S5_FWLATEVG (39)
=PP3V3_S5_LCD (67)

PP5V_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(REGULATOR OUTPUT 5 PWR) =PP5V_S5_REG (59)
=PP5V_S5_SB (25)
=PP5V_S5_P5VS3 (63)
=PP5V_S5_PWRCTL (63)
=PP5V_S5_P5VS0 (63)
=PP5V_S5_USB (42)
=PP5V_S5_PATA (PATA 5V PWR) (34)
=PP5V_S5_1V8S3 (61)

G3 HOT

PP3V42_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.425V

=PP3V42_G3H_REG (63)
=PP3V42_G3H_SMCVREF (46)
=PP3V42_G3H_SMBUS_SMC_BSA (27)
=PP3V42_G3H_PWRCTL (63)
=PP3V42_G3H_LIDSWITCH (65)
(LPC DEBUG BOARD) =PP3V42_G3H_LPCPLUS (5 47)
=PP3V42_G3H_SB_RTC (26)
=PP3V42_G3H_ACIN (65 66)
(SMC 32.768KHz OSC) =PP3V42_G3H_SMC_CLK (46)
(SMC 3.3V PWR) =PP3V42_G3H_SMC (45 46 48)

PBUS HOT

PPBUSB_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=12.6V

=PPBUSA_G3H (66)
(INVERTER PBUS PWR)
(ISL6262 VIN)
(LTC3728 VIN) =PPBUS_S5_INV (67)
=PPVIN_S5_IMVP6 (48 58)
=PPVIN_S5_1V51V05S0 (62)

=PPBUSB_G3H (66)
(LTC3728 VIN) =PPVIN_S5_5V3V3S5 (59 63)
(ISL6269 VIN) =PPVIN_S5_1V8S3 (61)
(FIREWIRE PORT PBUS PWR) =PPBUS_S5_FWPWRSW (39)
(YUKON POWER CONTROL) =PPBUS_S5_YUKON_CTRL (60)

PP18V5_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.5V

=PP18V5_G3H_INRUSH (65)
(DC-IN OUTPUT 18.5V PWR)
(CHARGER INPUT 18.5V PWR)
(SMC INPUT 18.5V PWR) =PP18V5_G3H_CHGR (66)

DCIN G3HOT

PPDCIN_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=18.5V

=PPDCIN_G3H (65)
=PPVBATT_G3H (66)
=PPVIN_G3H_P3V42G3H (63)

GND RAILS

XW8101
SM
=GND_AUDIO_CODEC (57 56 55 54) — GND_AUDIO_CODEC (5) — MAKE_BASE=TRUE — pins 1, 2

XW8102
SM
=GND_AUDIO_PWR (56 55) — GND_AUDIO_PWR (5) — MAKE_BASE=TRUE — pins 1, 2

Power Conn / Alias

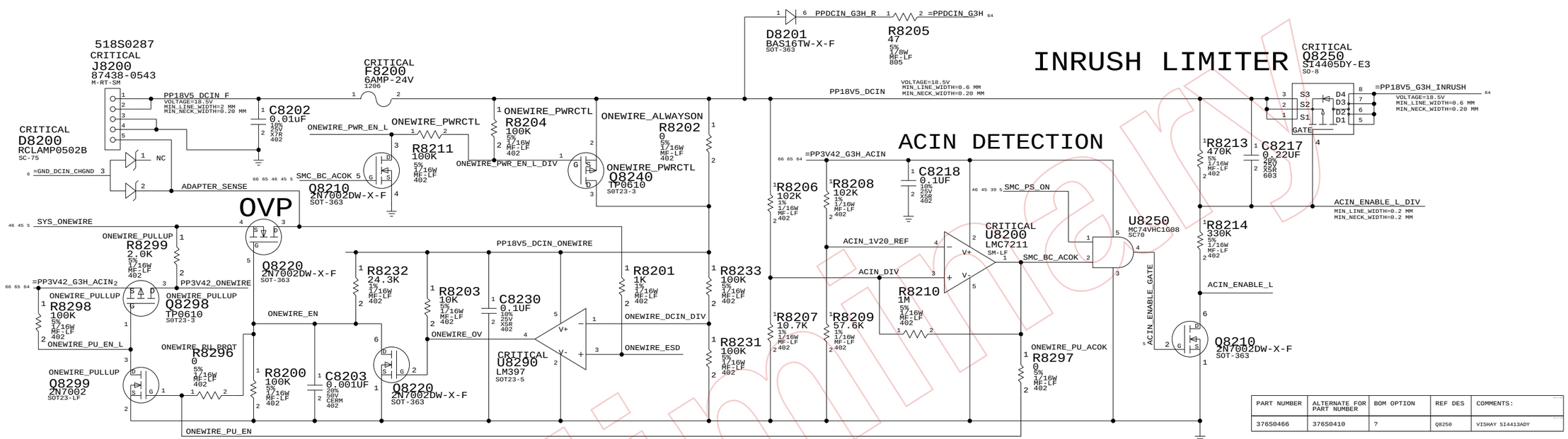
SYNC_MASTER=ENET SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

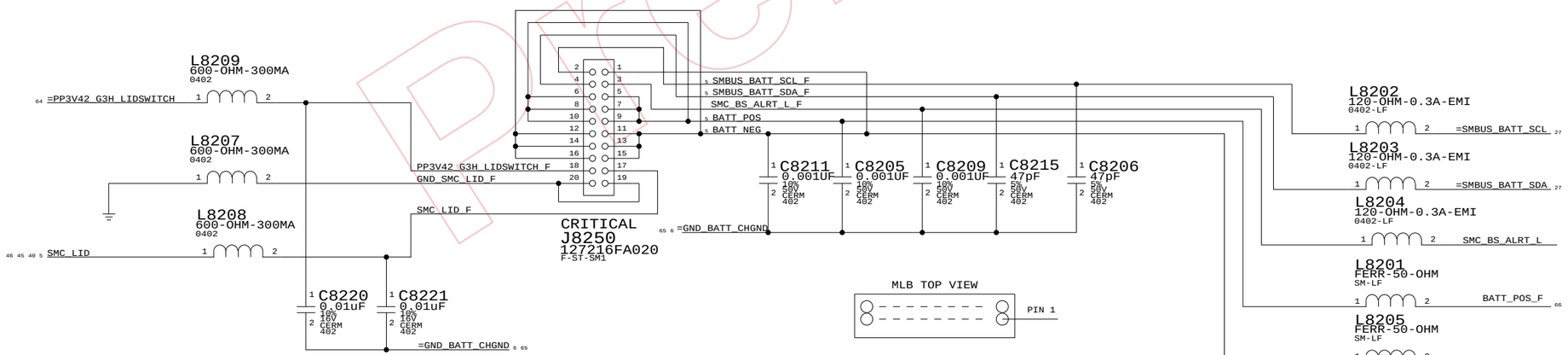
SCALE	SHT	OF
NONE	81	108

DC-JACK INTERFACE



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0466	376S0410	?	Q8250	VISHAY SI4413ADY

BATTERY INTERFACE



LID HALL EFFECT SENSOR

DC-In & Battery Connectors

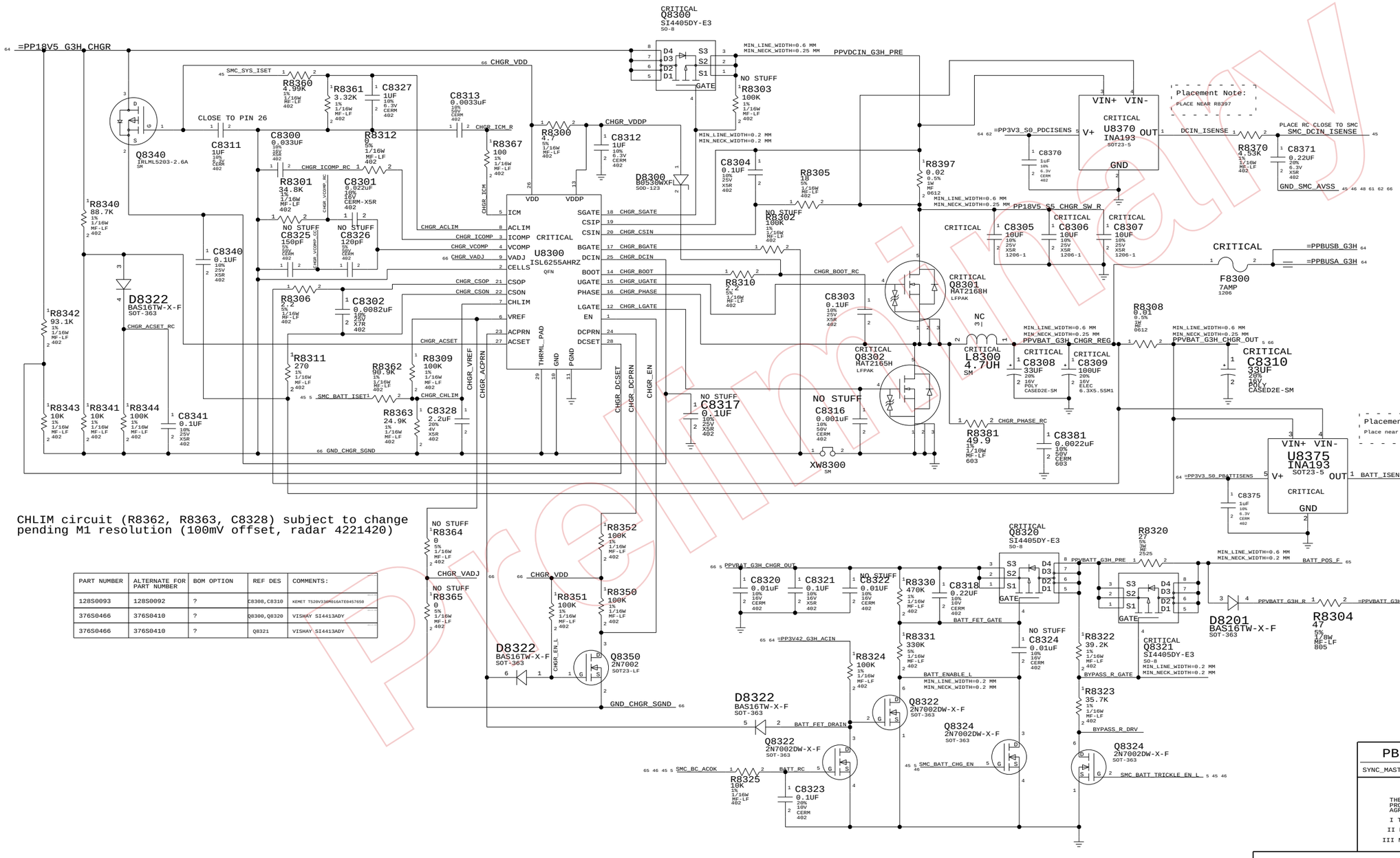
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C

SCALE: NONE SHT 82 OF 108

PBUS SUPPLY / BATTERY CHARGER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C8308,C8310	KEMET T520V336M016ATE045/650
376S0466	376S0410	?	Q8300,Q8320	VISHAY SI4413ADY
376S0466	376S0410	?	Q8321	VISHAY SI4413ADY

PBUS Supply/Battery Charger

SYNC_MASTER=SMC SYNC_DATE=08/19/2005

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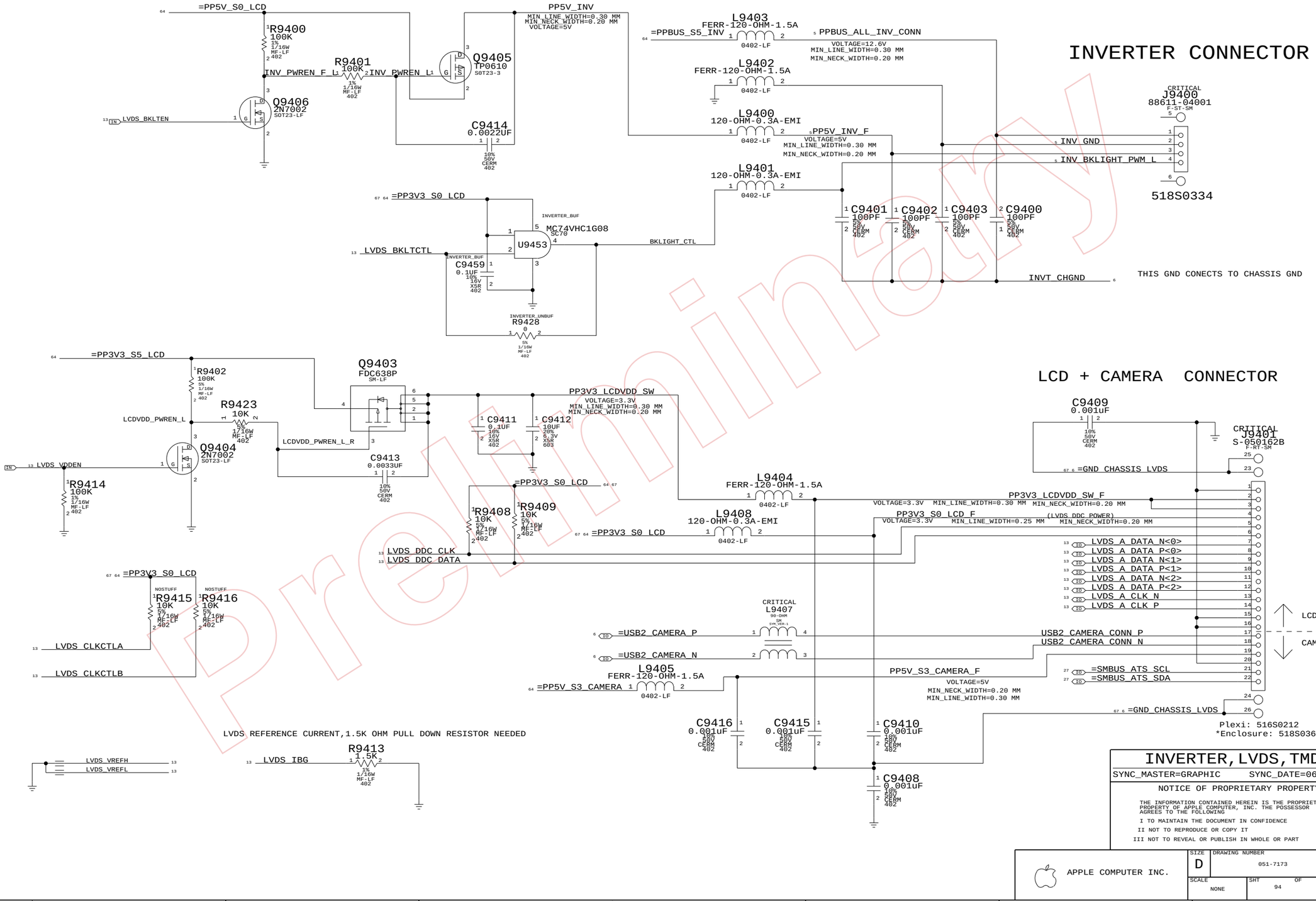
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 83 OF 108	

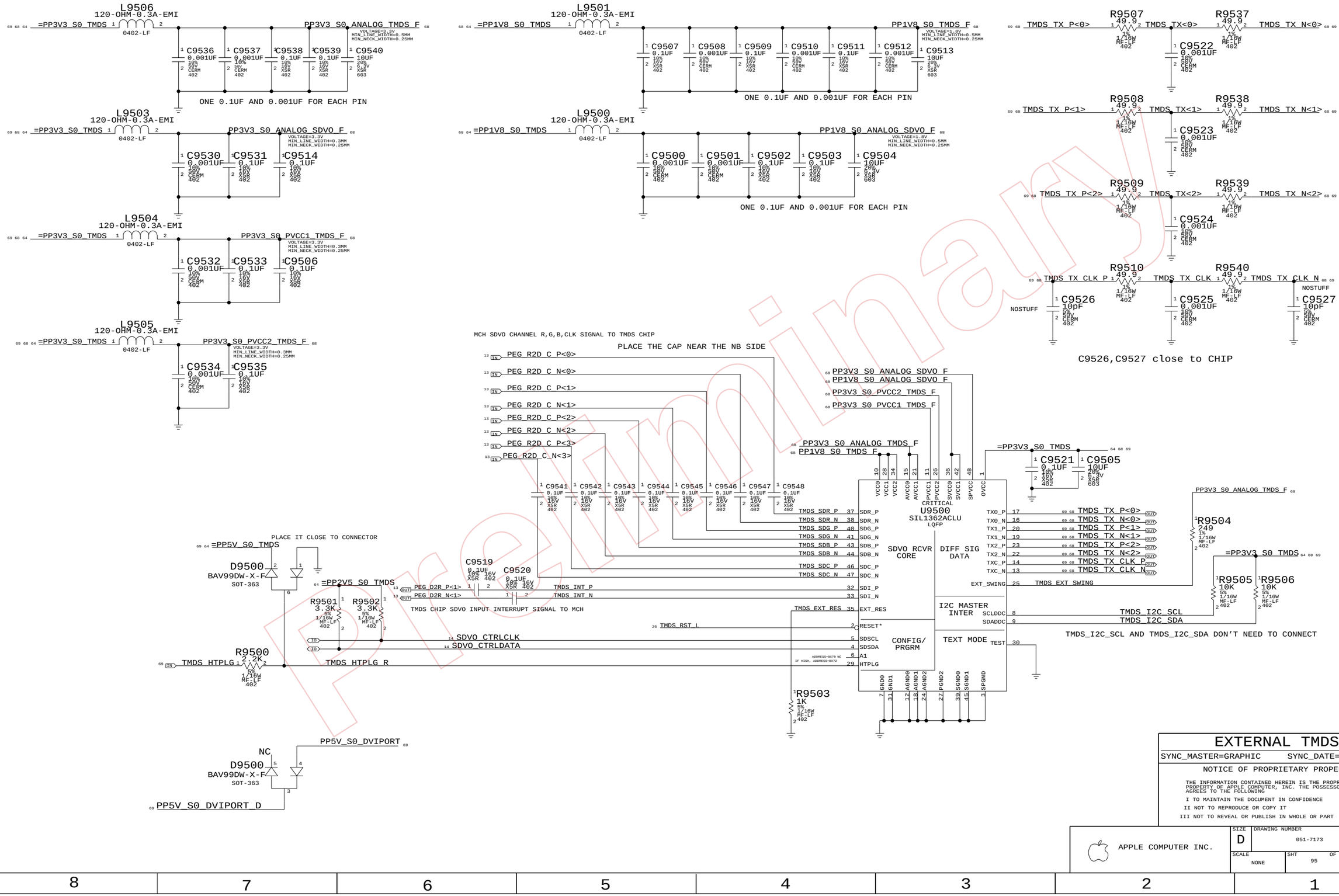


INVERTER, LVDS, TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE	SHT	OF
NONE	94	108



EXTERNAL TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 95 OF 108	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L9805, L9806, L9807	KEEP MAG.LAYER IN BOM

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

TMDS(MINI DVI) INTERFACE

=PP3V3_S0_TMDS 64 68 69

Q9801 2N7002DW-X-F SOT-363

R9821 2.2K 5% 1/16W MF-LF 402

R9822 2.2K 5% 1/16W MF-LF 402

GPU_CRT_DDC_CLK 69

GPU_CRT_DDC_DATA 69

13 CRT_DDC_CLK IO

13 CRT_DDC_DATA IO

Q9801 2N7002DW-X-F SOT-363

=PP5V_S0_TMDS 68 64

F9804 0.5AMP-13.2V SM-LF

VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

PP5V_S0_TMDS_FUSE

L9844 400-OHM-EMI SM-1

VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

PP5V_S0_DVIPORT 68 69

VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

C9804 0.1UF 20% 16V CERM 402

=GND_CHASSIS_TMDS_UPPER 6 69

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

=PP3V3_S0_TMDS 64 68 69

C9860 0.1UF 20% 16V CERM 402

13 CRT_HSYNC_R

R9860 39 5% 1/16W MF-LF 402

U9804 SN74LVC2G125DCU U8 VCC GND 125

CRT_HSYNC_LS

R9870 39 5% 1/16W MF-LF 402

VGA_HSYNC 69

NOSTUFF C9842 33PF 50V CERM 402

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

13 CRT_VSYNC_R

R9861 39 5% 1/16W MF-LF 402

U9804 SN74LVC2G125DCU U8 VCC GND 125

CRT_VSYNC_LS

R9871 39 5% 1/16W MF-LF 402

VGA_VSYNC 69

NOSTUFF C9843 33PF 50V CERM 402

A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

13 CRT_IREF

R9869 255 1% 1/16W MF-LF 402

TV REFERENCE CURRENT,USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS

13 TV_IREF

R9868 4.99K 1% 1/16W MF-LF 402

PP5V_S0_DVIPORT_D 68

DVI power DIODE on page 95 (D9500)

R9862 2.2K 5% 1/16W MF-LF 402

R9863 2.2K 5% 1/16W MF-LF 402

68 TMDS_HTPLG

C9808 0.001uF 10% 50V CERM 402

69 GPU_CRT_DDC_CLK

C9809 100pF 5% 50V CERM 402

69 GPU_CRT_DDC_DATA

C9812 100pF 5% 50V CERM 402

OMIT CRITICAL J9801 MINI-DVI RT-TH

69 68 PP5V_S0_DVIPORT

NC NC

TMDS_TX_CONN_P<2>

TMDS_TX_CONN_N<2>

TMDS_TX_CONN_P<1>

TMDS_TX_CONN_N<1>

TMDS_TX_CONN_P<0>

TMDS_TX_CONN_N<0>

TMDS_TX_CONN_CLK_P

TMDS_TX_CONN_CLK_N

CRITICAL L9805 90-OHM-300MA 2012H SYM_VER-1

TMDS_TX_P<2> 68

TMDS_TX_N<2> 68

CRITICAL L9807 90-OHM-300MA 2012H SYM_VER-1

TMDS_TX_P<1> 68

TMDS_TX_N<1> 68

CRITICAL L9806 90-OHM-300MA 2012H SYM_VER-1

TMDS_TX_P<0> 68

TMDS_TX_N<0> 68

CRITICAL L9804 370-OHM-280MA SM1

TMDS_TX_CLK_P 68

TMDS_TX_CLK_N 68

PLACE THE RESISTOR CLOSE TO GMCH

13 TV_DACA_OUT

13 CRT_BLUE

R9850 75 1% 1/16W MF-LF 402

R9851 75 1% 1/16W MF-LF 402

13 TV_IRTNA

13 CRT_BLUE_L

69 68 64 =PP3V3_S0_TMDS

C9839 0.1UF 10% 16V X5R 402

EXT_COMPVID_B

FL9800 LCFILTER SM-220MHZ-LF

NOSTUFF R9856 150 1% 1/16W MF-LF 402

VGA_B

VGA_HSYNC

C9824 3.3PF 0.25% 50V CERM 402

CRITICAL U9801 TS3V330 SOP

VCC 16

S1A 2 S2A 3 S1B 5 S2B 6 S1C 11 S2C 10 S1D 14 S2D 13

DA 4 DB 7 DC 9 DD 12 IN 1 EN_L 15 GND 8

PLACE THE RESISTOR CLOSE TO GMCH

13 TV_DACB_OUT

13 CRT_GREEN

R9852 75 1% 1/16W MF-LF 402

R9853 75 1% 1/16W MF-LF 402

13 TV_IRTNB

13 CRT_GREEN_L

EXT_Y_G

FL9801 LCFILTER SM-220MHZ-LF

NOSTUFF R9864 150 1% 1/16W MF-LF 402

VGA_G

VGA_VSYNC

C9834 3.3PF 0.25% 50V CERM 402

PLACE THE RESISTOR CLOSE TO GMCH

13 TV_DACC_OUT

13 CRT_RED

R9854 75 1% 1/16W MF-LF 402

R9855 75 1% 1/16W MF-LF 402

13 TV_IRTNC

13 CRT_RED_L

EXT_C_R

FL9802 LCFILTER SM-220MHZ-LF

NOSTUFF R9859 150 1% 1/16W MF-LF 402

VGA_R

C9820 3.3PF 0.25% 50V CERM 402

69 6 =GND_CHASSIS_TMDS_UPPER

6 =GND_CHASSIS_TMDS_DOWN

NOSTUFF C9821 0.1UF 10% 16V X5R 402

=SB_GPIO22 6

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN,32P MINI-DVI RCPT,RA,MG3,LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN,32P MINI-DVI RCPT,RA,BLACK,LF	J9801	CRITICAL	FANCY

MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE: NONE	SHT 98 OF 108	

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Title:        Basenet Report
Design:       m42a
Date:         Aug 5 16:01:17 2006

Base nets and synonyms for m42a_lib.M42A(@m42a_lib.m42a(sch_1))
Base Signal          Synonyms                            Location([Zone][dir])

1V2_FB               1V2_FB - @m42a_lib.M42A             60A3
1V05S0_BG            1V05S0_BG - @m42a_lib.M42A          62B4
1V05S0_BOOST         1V05S0_BOOST - @m42a_lib.M42A       62B4
1V05S0_BOOST_RC      1V05S0_BOOST_RC - @m42a_lib.M42A    62C3
1V05S0_COMP          1V05S0_COMP - @m42a_lib.M42A        5D7
1V05S0_FSET          1V05S0_FSET - @m42a_lib.M42A        5D7
1V05S0_ITH           1V05S0_ITH - @m42a_lib.M42A         62B4
1V05S0_ITH_RC        1V05S0_ITH_RC - @m42a_lib.M42A      62B3
1V05S0_RUNSS         1V05S0_RUNSS - @m42a_lib.M42A       62B4 63B7
1V05S0_SNS_N         1V05S0_SNS_N - @m42a_lib.M42A       62C3
1V05S0_SNS_P         1V05S0_SNS_P - @m42a_lib.M42A       62C3
1V05S0_SW            1V05S0_SW - @m42a_lib.M42A          62B4
1V05S0_TG            1V05S0_TG - @m42a_lib.M42A          62C4
1V05S0_VOSNS         1V05S0_VOSNS - @m42a_lib.M42A       62B4
1V5S0_BG             1V5S0_BG - @m42a_lib.M42A           62B5
1V5S0_BOOST          1V5S0_BOOST - @m42a_lib.M42A        62B5
1V5S0_BOOST_RC       1V5S0_BOOST_RC - @m42a_lib.M42A     62C6
1V5S0_ITH            1V5S0_ITH - @m42a_lib.M42A          62B5
1V5S0_ITH_RC         1V5S0_ITH_RC - @m42a_lib.M42A       62B5
1V5S0_RUNSS          1V5S0_RUNSS - @m42a_lib.M42A        5D7 62B5 63B7
1V5S0_SNS_N          1V5S0_SNS_N - @m42a_lib.M42A        62C6
1V5S0_SNS_P          1V5S0_SNS_P - @m42a_lib.M42A        62C6
1V5S0_SW             1V5S0_SW - @m42a_lib.M42A           62B5
1V5S0_TG             1V5S0_TG - @m42a_lib.M42A           62C5
1V5S0_VOSNS          1V5S0_VOSNS - @m42a_lib.M42A        62B5
1V8S3_BOOT           1V8S3_BOOT - @m42a_lib.M42A         61B5
1V8S3_BOOT_RC        1V8S3_BOOT_RC - @m42a_lib.M42A      61C4
1V8S3_COMP           1V8S3_COMP - @m42a_lib.M42A         5D7 61B6
1V8S3_COMP_R         1V8S3_COMP_R - @m42a_lib.M42A       61B6
1V8S3_FB             1V8S3_FB - @m42a_lib.M42A           61B6
1V8S3_FCCM           1V8S3_FCCM - @m42a_lib.M42A         61B6
1V8S3_FSET           1V8S3_FSET - @m42a_lib.M42A         5D7 61C6
1V8S3_ISEN           1V8S3_ISEN - @m42a_lib.M42A         61B5
1V8S3_LG             1V8S3_LG - @m42a_lib.M42A           61B5
1V8S3_PHASE          1V8S3_PHASE - @m42a_lib.M42A        61B5
1V8S3_UG             1V8S3_UG - @m42a_lib.M42A           61C5
1V8S3_VCC            1V8S3_VCC - @m42a_lib.M42A          61C6
1V51V05S0_FCB        1V51V05S0_FCB - @m42a_lib.M42A      62A3 62B5
1V51V05S0_FSEL       1V51V05S0_FSEL - @m42a_lib.M42A     62A2 62B4
1V51V05S0_PGOOD      1V51V05S0_PGOOD - @m42a_lib.M42A    58C7 62A1 63C2
2V5S0_BP             2V5S0_BP - @m42a_lib.M42A           60C3
2V5S3_BP             2V5S3_BP - @m42a_lib.M42A           60C3
3V3S5_BG             3V3S5_BG - @m42a_lib.M42A           59B5
3V3S5_BOOST          3V3S5_BOOST - @m42a_lib.M42A        59B5
3V3S5_BOOST_RC       3V3S5_BOOST_RC - @m42a_lib.M42A     59C6
3V3S5_COMP           3V3S5_COMP - @m42a_lib.M42A         5D7
3V3S5_FSET           3V3S5_FSET - @m42a_lib.M42A         5D7
3V3S5_ITH            3V3S5_ITH - @m42a_lib.M42A          59B5
3V3S5_ITH_RC         3V3S5_ITH_RC - @m42a_lib.M42A       59B5
3V3S5_RUNSS          3V3S5_RUNSS - @m42a_lib.M42A        59B5 63C7
3V3S5_SNS_N          3V3S5_SNS_N - @m42a_lib.M42A        59C6
3V3S5_SNS_P          3V3S5_SNS_P - @m42a_lib.M42A        59C6
3V3S5_SW             3V3S5_SW - @m42a_lib.M42A           59B5
3V3S5_TG             3V3S5_TG - @m42a_lib.M42A           59C5
3V3S5_VOSNS          3V3S5_VOSNS - @m42a_lib.M42A        59B5
5V3V3S5_FCB          5V3V3S5_FCB - @m42a_lib.M42A        59A3 59B5
5V3V3S5_FSEL         5V3V3S5_FSEL - @m42a_lib.M42A       59A2 59B4
5VS5_BG              5VS5_BG - @m42a_lib.M42A            59B4
5VS5_BOOST           5VS5_BOOST - @m42a_lib.M42A         59B4
5VS5_BOOST_RC        5VS5_BOOST_RC - @m42a_lib.M42A      59C3
5VS5_ITH             5VS5_ITH - @m42a_lib.M42A           59B4
5VS5_ITH_RC          5VS5_ITH_RC - @m42a_lib.M42A        59B3
5VS5_RUNSS           5VS5_RUNSS - @m42a_lib.M42A         5D7 59B4 63C7
5VS5_SNS_N           5VS5_SNS_N - @m42a_lib.M42A         59C3
5VS5_SNS_P           5VS5_SNS_P - @m42a_lib.M42A         59C3
5VS5_SW              5VS5_SW - @m42a_lib.M42A            59B4
5VS5_TG              5VS5_TG - @m42a_lib.M42A            59C4
5VS5_VOSNS           5VS5_VOSNS - @m42a_lib.M42A         59B4
5V_REG_IN            5V_REG_IN - @m42a_lib.M42A          54A5
=EXTBUSB_OC_L        =EXTBUSB_OC_L - @m42a_lib.M42A      6C2 42C8
                     USB_C_OC_L - @m42a_lib.M42A         6C1 22C4 22D8
                     EXTBUSB_OC_L - @m42a_lib.M42A       6C2
=FWPWR_PWRON         =FWPWR_PWRON - @m42a_lib.M42A       6D2 39C6
                     NC_FWPWR_PWRON - @m42a_lib.M42A     6D1
=GND_BATT_CHGND      =GND_BATT_CHGND - @m42a_lib.M42A    6D8 65A6 65A6
                     =GND_CHASSIS_AUDIO_JACK -           6D8 56B8
                     @m42a_lib.M42A
                     =GND_CHASSIS_AUDIO_MIC -            6D8 57A6
                     @m42a_lib.M42A
                     =GND_CHASSIS_DIPDIMM_LEFT -         6D8 28A5
                     @m42a_lib.M42A
                     GND_CHASSIS_IO - @m42a_lib.M42A     6C7 6D7
                     =GND_CHASSIS_USB - @m42a_lib.M42A   6C8 42A2 42A4 42C2 42C4
                     =GND_CHASSIS_FW_DOWN -              6C8 39A1
                     @m42a_lib.M42A
                     GND_CHASSIS_IO - @m42a_lib.M42A     6C7 6D7
                     =GND_CHASSIS_USB - @m42a_lib.M42A   6C8 42A2 42A4 42C2 42C4
                     =GND_CHASSIS_FW_DOWN -              6C8 39A1
                     @m42a_lib.M42A
                     =GND_CHASSIS_DIPDIMM_LEFT -         6D8 28A5
                     @m42a_lib.M42A
                     =GND_CHASSIS_AUDIO_SPKRCONN -       6D8
                     @m42a_lib.M42A
                     =GND_CHASSIS_AUDIO_SHIELD3 -        6D8
                     @m42a_lib.M42A
                     =GND_CHASSIS_AUDIO_SHIELD2 -        6D8
                     @m42a_lib.M42A
                     =GND_CHASSIS_AUDIO_SHIELD1 -        6D8
                     @m42a_lib.M42A
                     =GND_CHASSIS_AUDIO_MIC -            6D8 57A6
                     @m42a_lib.M42A
                     =GND_CHASSIS_AUDIO_JACK -           6D8 56B8
                     @m42a_lib.M42A
=GND_CHASSIS_DIPDIMM =GND_CHASSIS_DIPDIMM_CENTER -       6B8 28D5 29A5
_CENTER              @m42a_lib.M42A
                     GND_CHASSIS_CENTER - @m42a_lib.M42A 6B7
=GND_CHASSIS_DIPDIMM =GND_CHASSIS_DIPDIMM_RIGHT -        6B8 29D4
_RIGHT               @m42a_lib.M42A
                     GND_CHASSIS_RIGHT - @m42a_lib.M42A  6B7
=GND_CHASSIS_FW_UPPE =GND_CHASSIS_FW_UPPER -             6A6 39A1
R                    @m42a_lib.M42A
                     =GND_CHASSIS_TMDS_DOWN -            6A6 69A3
                     @m42a_lib.M42A
                     GND_CHASSIS_IO1 - @m42a_lib.M42A    6A5
                     =GND_CHASSIS_TMDS_DOWN -            6A6 69A3
                     @m42a_lib.M42A
=GND_CHASSIS_LVDS    =GND_CHASSIS_LVDS - @m42a_lib.M42A  6C8 67A2 67B2

                     GND_CHASSIS_SATA - @m42a_lib.M42A   6C7 35C8
=GND_CHASSIS_RJ45    =GND_CHASSIS_RJ45 - @m42a_lib.M42A  6C8 37A4
                     =GND_CHASSIS_TMDS_UPPER -           6C8 69A4 69C3
                     @m42a_lib.M42A
                     GND_CHASSIS_DCIN - @m42a_lib.M42A   6C7
                     =GND_DCIN_CHGND - @m42a_lib.M42A    6C8 65C8
                     GND_CHASSIS_DCIN - @m42a_lib.M42A   6C7
                     =GND_DCIN_CHGND - @m42a_lib.M42A    6C8 65C8
                     =GND_CHASSIS_TMDS_UPPER -           6C8 69A4 69C3
                     @m42a_lib.M42A
=P1V2S0_EN           =P1V2S0_EN - @m42a_lib.M42A         63B5
                     PM_SLP_S3_LS12V6_L - @m42a_lib.M42A 63B6
                     =P3V3S0_EN - @m42a_lib.M42A         63B5
                     =P5VS0_EN - @m42a_lib.M42A          63C5
                     PM_SLP_S3_LS12V6_L - @m42a_lib.M42A 63B6
=P1V8S0_EN_L         =P1V8S0_EN_L - @m42a_lib.M42A       63A5
                     PM_SLP_S3_LS5V - @m42a_lib.M42A     63A6
=P3V3S3_EN_L         =P3V3S3_EN_L - @m42a_lib.M42A       63C5
                     PM_SLP_S4_LS5V - @m42a_lib.M42A     42B8 63D6
                     =P5VS3_EN_L - @m42a_lib.M42A        63D5
                     PM_SLP_S4_LS5V - @m42a_lib.M42A     42B8 63D6
=PP1V05_S0_FSB_NB    =PP1V05_S0_FSB_NB - @m42a_lib.M42A  12A7 12B7 12C2 19D7 33B8
                                                         33C7 33C8 64D6
                     =PP1V05_S0_NB - @m42a_lib.M42A      19D1 19D7 64C6
                     =PP1V05_S0_CPU_NB - @m42a_lib.M42A  62A6 64D8
                     =PP1V05_S0_NB_VTT - @m42a_lib.M42A  17D3 19B5 19D7 64C6
                     =PP1V05_S0_CPU - @m42a_lib.M42A     7B5 7B6 7D5 7D5 8C7 9C8
                                                         11B3 11C5 64D6
                     =PPVCORE_S0_NB - @m42a_lib.M42A     16C8 16D3 19C8 19D7 64D6
                     PP1V05_S0_CPU_NB - @m42a_lib.M42A   64D7
                     =PPVCORE_S0_NB - @m42a_lib.M42A     16C8 16D3 19C8 19D7 64D6
                     =PP1V05_S0_NB_VTT - @m42a_lib.M42A  17D3 19B5 19D7 64C6
                     =PP1V05_S0_NB - @m42a_lib.M42A      19D1 19D7 64C6
                     =PP1V05_S0_CPU_NB - @m42a_lib.M42A  62A6 64D8
                     =PP1V05_S0_CPU - @m42a_lib.M42A     7B5 7B6 7D5 7D5 8C7 9C8
                                                         11B3 11C5 64D6
=PP1V05_S0_REG       =PP1V05_S0_REG - @m42a_lib.M42A     5B2 62B1 64D8
                     =PP1V05_S0_CPU_NB_SENSE -           62A8 64D6
                     @m42a_lib.M42A
                     =PP1V05_S0_SB_CPU_IO -              21C1 21C1 24C3 25C4 64D6
                     @m42a_lib.M42A
                     =PPVCORE_S0_SB - @m42a_lib.M42A     24D3 25D3 64D6
                     PP1V05_S0 - @m42a_lib.M42A          5B2 64D7
                     =PPVCORE_S0_SB - @m42a_lib.M42A     24D3 25D3 64D6
                     =PP1V05_S0_SB_CPU_IO -              21C1 21C1 24C3 25C4 64D6
                     @m42a_lib.M42A
                     =PP1V05_S0_CPU_NB_SENSE -           62A8 64D6
                     @m42a_lib.M42A
=PP1V5_S0_NB         =PP1V5_S0_NB - @m42a_lib.M42A       19C1 19D7 64C6
                     =PP1V5_S0_NB_PCIE - @m42a_lib.M42A  13D2 19D7 64C6
                     =PP1V5_S0_AIRPORT - @m42a_lib.M42A  43D3 64C6
                     =PP1V5_S0_SB_VCCSATAPLL -           24B5 25D6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCC1_5_A_ATX -         24A5 25C6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCCUSBPLL -            24A5 25B6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCC1_5_A_USB_CORE -    24A3 25B2 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCC1_5_A -             24A3 25C2 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB - @m42a_lib.M42A       25A8 25C8 64C6
                     =PP1V5_S0_NB_VCCAUX -               16D1 17B6 19B6 19D7 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_NB_VCCD_HMPLL -           17C6 19D7 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_NB_VCCD_LVDS -            17C6 19B8 19D7 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_NB_PLL - @m42a_lib.M42A   19C6 19D7 64C6
                     =PP1V5_S0_NB_TVDAC - @m42a_lib.M42A 19A8 19D7 64C6
                     =PP1V5_S0_NB_3G - @m42a_lib.M42A    19B5 64C6
                     =PP1V5_S0_NB_3GPLL - @m42a_lib.M42A 19A5 64C6
                     =PP1V5_S0_SB_VCC1_5_A_ARX -         24B5 25D6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_CPU - @m42a_lib.M42A      8B7 9D8 64C6
                     =PP1V5_S0_REG - @m42a_lib.M42A      62B8 64C8
                     PP1V5_S0 - @m42a_lib.M42A           5B2 64C7
                     =PP1V5_S0_SB_VCCUSBPLL -            24A5 25B6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCCSATAPLL -           24B5 25D6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCC1_5_A_USB_CORE -    24A3 25B2 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCC1_5_A_ATX -         24A5 25C6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCC1_5_A_ARX -         24B5 25D6 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB_VCC1_5_A -             24A3 25C2 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_SB - @m42a_lib.M42A       25A8 25C8 64C6
                     =PP1V5_S0_REG - @m42a_lib.M42A      62B8 64C8
                     =PP1V5_S0_NB_VCCD_LVDS -            17C6 19B8 19D7 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_NB_VCCD_HMPLL -           17C6 19D7 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_NB_VCCAUX -               16D1 17B6 19B6 19D7 64C6
                     @m42a_lib.M42A
                     =PP1V5_S0_NB_TVDAC - @m42a_lib.M42A 19A8 19D7 64C6
                     =PP1V5_S0_NB_PLL - @m42a_lib.M42A   19C6 19D7 64C6
                     =PP1V5_S0_NB_PCIE - @m42a_lib.M42A  13D2 19D7 64C6
                     =PP1V5_S0_NB_3GPLL - @m42a_lib.M42A 19A5 64C6
                     =PP1V5_S0_NB_3G - @m42a_lib.M42A    19B5 64C6
                     =PP1V5_S0_CPU - @m42a_lib.M42A      8B7 9D8 64C6
                     =PP1V5_S0_AIRPORT - @m42a_lib.M42A  43D3 64C6
=PP1V8_S3_MEM_NB     =PP1V8_S3_MEM_NB - @m42a_lib.M42A   14C2 16B6 19D7 28D2 29D2
                                                         61C2 64C6
                     PP1V8_S3_MEM_NB - @m42a_lib.M42A    64C4
=PP2V5_S0_NB_CRTDAC  =PP2V5_S0_NB_CRTDAC -               19D4 19D7 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_VCCA_3GBG -            17D6 19B7 19D7 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_VCC_TXLVDS -           17D6 19B8 19D7 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_DISP_PLL -             19D6 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_VCCA_LVDS -            17C6 19C7 19D1 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_TMDS - @m42a_lib.M42A     64B6 68B7
                     =PP2V5_S0_NB_VCCSYNC -              17D6 19B6 19D7 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_REG - @m42a_lib.M42A      60C2 63B3 64B8
                     PP2V5_S0 - @m42a_lib.M42A           5B2 64B7
                     =PP2V5_S0_TMDS - @m42a_lib.M42A     64B6 68B7
                     =PP2V5_S0_REG - @m42a_lib.M42A      60C2 63B3 64B8

                     =PP2V5_S0_NB_VCC_TXLVDS -           17D6 19B8 19D7 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_VCCSYNC -              17D6 19B6 19D7 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_VCCA_LVDS -            17C6 19C7 19D1 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_VCCA_3GBG -            17D6 19B7 19D7 64B6
                     @m42a_lib.M42A
                     =PP2V5_S0_NB_DISP_PLL -             19D6 64B6
                     @m42a_lib.M42A
=PP3V3_S0_FAN_RT     =PP3V3_S0_FAN_RT - @m42a_lib.M42A   5D2 51C4 64A6
                     =PP3V3_S0_ENET - @m42a_lib.M42A     36C8 64A6
                     =PP3V3_S0_FW - @m42a_lib.M42A       39C6 64A6
                     =PP3V3_S0_2V5S0 - @m42a_lib.M42A    60C4 64A6
                     =PP3V3_S0_1V51V05S0 -               62B1 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SMBUS_SMC_BSB -           27B1 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_RSTBUF - @m42a_lib.M42A   26B4 64A6
                     =PP3V3_S0_SMBUS_SB - @m42a_lib.M42A 27D8 64A6
                     =PP3V3_S0_SMBUS_SMC_0 -             27D5 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SMBUS_SMC_MLB -           27C5 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_ALLSYSPG - @m42a_lib.M42A 63B1 64A6
                     =PP3V3_S0_LCD - @m42a_lib.M42A      64A6 67B5 67B5 67B7 67C6
                     =PP3V3_S0_PBATTISENS -              64A6 66B3
                     @m42a_lib.M42A
                     =PP3V3_S0_PDCISENS - @m42a_lib.M42A 62A5 64A6 66C4
                     =PP3V3_S0_CPUPOWER - @m42a_lib.M42A 48C2 64A6
                     =PP3V3_S0_SB - @m42a_lib.M42A       22B5 25D8 34C8 64B6
                     =PP3V3_S0_SB_GPIO - @m42a_lib.M42A  21C3 21D3 23B2 23D5 64B6
                     =PP3V3_S0_SB_VCC3_3 -               24B5 24B5 25B8 25C6 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_VCC3_3_PCI -           24B3 25A4 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_VCC3_3_IDE -           24C3 25B4 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_PCI - @m42a_lib.M42A   26D1 64B6
                     =PP3V3_S0_SB_PM - @m42a_lib.M42A    26B6 26B8 64B6
                     =PP3V3_S0_PATA - @m42a_lib.M42A     34C2 64A6
                     =PP3V3_S0_SMC_LS - @m42a_lib.M42A   46D3 64A6
                     =PP3V3_S0_NB - @m42a_lib.M42A       14C7 14D6 19C7 20A4 20B4
                                                         20B4 64A6
                     =PP3V3_S0_SB_VCCLAN3_3 -            24D3 25D3 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_3V3_1V5_VCCHDA -       24C3 25C4 64A6
                     @m42a_lib.M42A
                     =PPSPD_S0_MEM - @m42a_lib.M42A      28A7 29A3 29A7 64A6
                     =PP3V3_S0_CK410 - @m42a_lib.M42A    32C7 32D3 32D8 64A6
                     =PP3V3_S0_AIRPORT - @m42a_lib.M42A  43C3 64A6
                     =PP3V3_S0_TPM - @m42a_lib.M42A      53D4 64A6
                     =PP3V3_S0_AUDIO - @m42a_lib.M42A    54A6 54D7 56D8 57B5 64A6
                     =PP3V3_S0_TMDS - @m42a_lib.M42A     64A6 68B1 68B2 68C8 68C8
                                                         68D8 68D8 69B7 69D1 69D5
                     =PP3V3_S0_THRM_SNR - @m42a_lib.M42A 10C4 49B3 49D3 64A6
                     =PP3V3_S0_IMVP6 - @m42a_lib.M42A    58D8 64A6
                     =PP3V3_S0_NB_VCC_HV -               17C6 19B7 19C7 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_FET - @m42a_lib.M42A      63C3 64B8
                     PP3V3_S0 - @m42a_lib.M42A           5A2 64B7
                     =PPSPD_S0_MEM - @m42a_lib.M42A      28A7 29A3 29A7 64A6
                     =PP3V3_S0_TPM - @m42a_lib.M42A      53D4 64A6
                     =PP3V3_S0_TMDS - @m42a_lib.M42A     64A6 68B1 68B2 68C8 68C8
                                                         68D8 68D8 69B7 69D1 69D5
                     =PP3V3_S0_THRM_SNR - @m42a_lib.M42A 10C4 49B3 49D3 64A6
                     =PP3V3_S0_SMC_LS - @m42a_lib.M42A   46D3 64A6
                     =PP3V3_S0_SMBUS_SMC_MLB -           27C5 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SMBUS_SMC_BSB -           27B1 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SMBUS_SMC_0 -             27D5 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SMBUS_SB - @m42a_lib.M42A 27D8 64A6
                     =PP3V3_S0_SB_VCCLAN3_3 -            24D3 25D3 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_VCC3_3_PCI -           24B3 25A4 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_VCC3_3_IDE -           24C3 25B4 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_VCC3_3 -               24B5 24B5 25B8 25C6 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB_PM - @m42a_lib.M42A    26B6 26B8 64B6
                     =PP3V3_S0_SB_PCI - @m42a_lib.M42A   26D1 64B6
                     =PP3V3_S0_SB_GPIO - @m42a_lib.M42A  21C3 21D3 23B2 23D5 64B6
                     =PP3V3_S0_SB_3V3_1V5_VCCHDA -       24C3 25C4 64A6
                     @m42a_lib.M42A
                     =PP3V3_S0_SB - @m42a_lib.M42A       22B5 25D8 34C8 64B6
                     =PP3V3_S0_RSTBUF - @m42a_lib.M42A   26B4 64A6
                     =PP3V3_S0_PDCISENS - @m42a_lib.M42A 62A5 64A6 66C4
                     =PP3V3_S0_PBATTISENS -              64A6 66B3
                     @m42a_lib.M42A
                     =PP3V3_S0_PATA - @m42a_lib.M42A     34C2 64A6
                     =PP3V3_S0_NB_VCC_HV -               17C6 19B7 19C7 64B6
                     @m42a_lib.M42A
                     =PP3V3_S0_NB - @m42a_lib.M42A       14C7 14D6 19C7 20A4 20B4
                                                         20B4 64A6
                     =PP3V3_S0_LCD - @m42a_lib.M42A      64A6 67B5 67B5 67B7 67C6
                     =PP3V3_S0_IMVP6 - @m42a_lib.M42A    58D8 64A6
                     =PP3V3_S0_FW - @m42a_lib.M42A       39C6 64A6
                     =PP3V3_S0_FET - @m42a_lib.M42A      63C3 64B8
                     =PP3V3_S0_ENET - @m42a_lib.M42A     36C8 64A6
                     =PP3V3_S0_CPUPOWER - @m42a_lib.M42A 48C2 64A6
                     =PP3V3_S0_CK410 - @m42a_lib.M42A    32C7 32D3 32D8 64A6
                     =PP3V3_S0_AUDIO - @m42a_lib.M42A    54A6 54D7 56D8 57B5 64A6
                     =PP3V3_S0_ALLSYSPG - @m42a_lib.M42A 63B1 64A6
                     =PP3V3_S0_AIRPORT - @m42a_lib.M42A  43C3 64A6
                     =PP3V3_S0_2V5S0 - @m42a_lib.M42A    60C4 64A6
                     =PP3V3_S0_1V51V05S0 -               62B1 64A6
                     @m42a_lib.M42A
=PP3V42_G3H_LPCPLUS  =PP3V42_G3H_LPCPLUS -               5D2 47C6 64D1
                     @m42a_lib.M42A
                     =PP3V42_G3H_SMCVREF -               46C8 64D1
                     @m42a_lib.M42A
                     =PP3V42_G3H_SMC - @m42a_lib.M42A    45D2 45D3 45D3 46D1 46D5
                                                         46D8 48C8 64D1
                     =PP3V42_G3H_SB_RTC - @m42a_lib.M42A 26D6 64D1
                     =PP3V42_G3H_ACIN - @m42a_lib.M42A   64D1 65C4 65C8 66A5
                     =PP3V42_G3H_SMC_CLK -               46A8 64D1
                     @m42a_lib.M42A
                     =PP3V42_G3H_LIDSWITCH -             64D1 65A8
                     @m42a_lib.M42A
                     =PP3V42_G3H_REG - @m42a_lib.M42A    63D1 64D3
                     =PP3V42_G3H_SMBUS_SMC_BSA -         27C3 64D1

                     @m42a_lib.M42A
                     =PP3V42_G3H_PWRCTL - @m42a_lib.M42A 63B8 63C8 64D1
                     PP3V42_G3H - @m42a_lib.M42A         5A2 64D1
                     =PP3V42_G3H_SMC_CLK -               46A8 64D1
                     @m42a_lib.M42A
                     =PP3V42_G3H_SMCVREF -               46C8 64D1
                     @m42a_lib.M42A
                     =PP3V42_G3H_SMC - @m42a_lib.M42A    45D2 45D3 45D3 46D1 46D5
                                                         46D8 48C8 64D1
                     =PP3V42_G3H_SMBUS_SMC_BSA -         27C3 64D1
                     @m42a_lib.M42A
                     =PP3V42_G3H_SB_RTC - @m42a_lib.M42A 26D6 64D1
                     =PP3V42_G3H_REG - @m42a_lib.M42A    63D1 64D3
                     =PP3V42_G3H_PWRCTL - @m42a_lib.M42A 63B8 63C8 64D1
                     =PP3V42_G3H_LIDSWITCH -             64D1 65A8
                     @m42a_lib.M42A
                     =PP3V42_G3H_ACIN - @m42a_lib.M42A   64D1 65C4 65C8 66A5
=PP5V_S0_FAN_RT      =PP5V_S0_FAN_RT - @m42a_lib.M42A    5D2 51C4 64D3
                     =PP5V_S0_ISENSECAL - @m42a_lib.M42A 48A8 64D3
                     =PP5V_S0_LCD - @m42a_lib.M42A       64D3 67D7
                     =PP5V_S0_TMDS - @m42a_lib.M42A      64D3 68B7 69C6
                     =PP5V_S0_IMVP6 - @m42a_lib.M42A     58D8 64D3
                     =PP5V_1V51V05S0_VCC -               62A8 64D3
                     @m42a_lib.M42A
                     =PP5V_S0_NB_TVDAC - @m42a_lib.M42A  19C4 19C7 64D3
                     =PP5V_S0_LPCPLUS - @m42a_lib.M42A   5D2 47C6 64D3
                     =PP5V_S0_AUDIO_PWR - @m42a_lib.M42A 55B8 55B8 55D8 64D3
                     =PP5V_S0_AUDIO - @m42a_lib.M42A     54A6 55C8 64D3
                     =PP5V_S0_MEMVTT - @m42a_lib.M42A    31C6 64D3
                     =PP5V_S0_FET - @m42a_lib.M42A       63C3 64D6
                     =PP5V_S0_SATA - @m42a_lib.M42A      35C6 64D3
                     =PP5V_S0_SB - @m42a_lib.M42A        25D8 64D3
                     PP5V_S0 - @m42a_lib.M42A            5A2 64D4
                     =PP5V_S0_TMDS - @m42a_lib.M42A      64D3 68B7 69C6
                     =PP5V_S0_SB - @m42a_lib.M42A        25D8 64D3
                     =PP5V_S0_SATA - @m42a_lib.M42A      35C6 64D3
                     =PP5V_S0_NB_TVDAC - @m42a_lib.M42A  19C4 19C7 64D3
                     =PP5V_S0_MEMVTT - @m42a_lib.M42A    31C6 64D3
                     =PP5V_S0_LPCPLUS - @m42a_lib.M42A   5D2 47C6 64D3
                     =PP5V_S0_LCD - @m42a_lib.M42A       64D3 67D7
                     =PP5V_S0_ISENSECAL - @m42a_lib.M42A 48A8 64D3
                     =PP5V_S0_IMVP6 - @m42a_lib.M42A     58D8 64D3
                     =PP5V_S0_FET - @m42a_lib.M42A       63C3 64D6
                     =PP5V_S0_AUDIO_PWR - @m42a_lib.M42A 55B8 55B8 55D8 64D3
                     =PP5V_S0_AUDIO - @m42a_lib.M42A     54A6 55C8 64D3
                     =PP5V_1V51V05S0_VCC -               62A8 64D3
                     @m42a_lib.M42A
=PP5V_S0_IDE_PATA    =PP5V_S0_IDE_PATA - @m42a_lib.M42A  34C5
                     PP5V_S0_IDE_PATA - @m42a_lib.M42A   34D3
=PPDCIN_G3H          =PPDCIN_G3H - @m42a_lib.M42A        64B3 65D3
                     =PPVBATT_G3H - @m42a_lib.M42A       64B3 66B2
                     =PPVIN_G3H_P3V42G3H -               63D3 64B1
                     @m42a_lib.M42A
                     PPDCIN_G3H - @m42a_lib.M42A         64B1
                     =PPVIN_G3H_P3V42G3H -               63D3 64B1
                     @m42a_lib.M42A
                     =PPVBATT_G3H - @m42a_lib.M42A       64B3 66B2
=SMBUS_ATS_SCL       =SMBUS_ATS_SCL - @m42a_lib.M42A     27D1 67A2
                     SMBUS_SMC_RMT_SCL - @m42a_lib.M42A  27D2
                     SMB_RMT_CLK - @m42a_lib.M42A        27D3 45B5
                     SMBUS_SMC_RMT_SCL - @m42a_lib.M42A  27D2
=SMBUS_ATS_SDA       =SMBUS_ATS_SDA - @m42a_lib.M42A     27C1 67A2
                     SMBUS_SMC_RMT_SDA - @m42a_lib.M42A  27D2
                     SMB_RMT_DATA - @m42a_lib.M42A       27D3 45B5
                     SMBUS_SMC_RMT_SDA - @m42a_lib.M42A  27D2
=SMB_AIRPORT_CLK     =SMB_AIRPORT_CLK - @m42a_lib.M42A   27C6 43B4
                     =SMB_GEYSER_CLK - @m42a_lib.M42A    27B6 40C4
                     SMBUS_SB_SCL - @m42a_lib.M42A       27D7
                     =I2C_SODIMMB_SCL - @m42a_lib.M42A   27C6 29A6
                     SMB_CLK - @m42a_lib.M42A            23D5 27D8
                     =I2C_SODIMMA_SCL - @m42a_lib.M42A   27D6 28A6
                     SMB_CK410_CLK - @m42a_lib.M42A      27D6 32B6
                     SMB_CLK - @m42a_lib.M42A            23D5 27D8
                     SMB_CK410_CLK - @m42a_lib.M42A      27D6 32B6
                     SMBUS_SB_SCL - @m42a_lib.M42A       27D7
                     =SMB_GEYSER_CLK - @m42a_lib.M42A    27B6 40C4
                     =I2C_SODIMMB_SCL - @m42a_lib.M42A   27C6 29A6
                     =I2C_SODIMMA_SCL - @m42a_lib.M42A   27D6 28A6
=SMB_AIRPORT_DATA    =SMB_AIRPORT_DATA - @m42a_lib.M42A  27C6 43B4
                     =SMB_GEYSER_DATA - @m42a_lib.M42A   27B6 40C4
                     SMBUS_SB_SDA - @m42a_lib.M42A       27D7
                     =I2C_SODIMMB_SDA - @m42a_lib.M42A   27C6 29A6
                     SMB_DATA - @m42a_lib.M42A           23D5 27D8
                     =I2C_SODIMMA_SDA - @m42a_lib.M42A   27C6 28A6
                     SMB_CK410_DATA - @m42a_lib.M42A     27D6 32B6
                     SMB_DATA - @m42a_lib.M42A           23D5 27D8
                     SMB_CK410_DATA - @m42a_lib.M42A     27D6 32B6
                     SMBUS_SB_SDA - @m42a_lib.M42A       27D7
                     =SMB_GEYSER_DATA - @m42a_lib.M42A   27B6 40C4
                     =I2C_SODIMMB_SDA - @m42a_lib.M42A   27C6 29A6
                     =I2C_SODIMMA_SDA - @m42a_lib.M42A   27C6 28A6
=USB2_AIRPORT_N      =USB2_AIRPORT_N - @m42a_lib.M42A    6B2 43B4
                     USB_H_N - @m42a_lib.M42A            6B1 22C2
                     USB2_AIRPORT_N - @m42a_lib.M42A     6B2
=USB2_AIRPORT_P      =USB2_AIRPORT_P - @m42a_lib.M42A    6B2 43B4
                     USB_H_P - @m42a_lib.M42A            6B1 22C2
                     USB2_AIRPORT_P - @m42a_lib.M42A     6B2
=USB2_CAMERA_N       =USB2_CAMERA_N - @m42a_lib.M42A     6C2 67A4
                     USB_D_N - @m42a_lib.M42A            6C1 22C2
                     USB2_CAMERA_N - @m42a_lib.M42A      6C2
=USB2_CAMERA_P       =USB2_CAMERA_P - @m42a_lib.M42A     6C2 67B4
                     USB_D_P - @m42a_lib.M42A            6C1 22C2
                     USB2_CAMERA_P - @m42a_lib.M42A      6C2
ACIN_1V20_REF        ACIN_1V20_REF - @m42a_lib.M42A      65C4
ACIN_DIV             ACIN_DIV - @m42a_lib.M42A           65C4
ACIN_ENABLE_GATE     ACIN_ENABLE_GATE - @m42a_lib.M42A   5C1 65C3
ACIN_ENABLE_L        ACIN_ENABLE_L - @m42a_lib.M42A      65C2
ACIN_ENABLE_L_DIV    ACIN_ENABLE_L_DIV - @m42a_lib.M42A  65C1
ACZ_BITCLK           ACZ_BITCLK - @m42a_lib.M42A         5C1 21C7 54D7
ACZ_RST_L            ACZ_RST_L - @m42a_lib.M42A          5C1 21C7 54C7 57C3
ACZ_SDATAIN<0>       ACZ_SDATAIN<0> - @m42a_lib.M42A     5D1 21C7 54D7
ACZ_SDATAOUT         ACZ_SDATAOUT - @m42a_lib.M42A       5D1 21C7 54D7
ACZ_SYNC             ACZ_SYNC - @m42a_lib.M42A           5C1 21C7 54D7
ADAPTER_SENSE        ADAPTER_SENSE - @m42a_lib.M42A      65C7
AIRPORT_CLK100M_PCIE AIRPORT_CLK100M_PCIE_N -            33B2 33C4 43C6
_N                   @m42a_lib.M42A
AIRPORT_CLK100M_PCIE AIRPORT_CLK100M_PCIE_P -            33B2 33D4 43C6
_P                   @m42a_lib.M42A
AIRPORT_RST_L        AIRPORT_RST_L - @m42a_lib.M42A      26B1 43C4
ALL_SYS_PWRGD        ALL_SYS_PWRGD - @m42a_lib.M42A      5B2 26A5 45D8 63B1
ALS_GAIN             ALS_GAIN - @m42a_lib.M42A           45B5 46C6
ALS_LEFT             ALS_LEFT - @m42a_lib.M42A           5A7 45A8 46C3
ALS_RIGHT            ALS_RIGHT - @m42a_lib.M42A          45A8 46C3
AUDIO_SHIELD_PLANE   AUDIO_SHIELD_PLANE - @m42a_lib.M42A 56C3
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AUD_4V5_SHDN_L       AUD_4V5_SHDN_L - @m42a_lib.M42A     54A5
AUD_ALC_COUT         AUD_ALC_COUT - @m42a_lib.M42A       54B5
AUD_ANALOG_FILT_1    AUD_ANALOG_FILT_1 - @m42a_lib.M42A  54C4
AUD_ANALOG_FILT_2    AUD_ANALOG_FILT_2 - @m42a_lib.M42A  54C4
AUD_BI_PORT_A_L      AUD_BI_PORT_A_L - @m42a_lib.M42A    54C1 57C3
AUD_BI_PORT_A_R      AUD_BI_PORT_A_R - @m42a_lib.M42A    54C1 57B3
AUD_BI_PORT_B_L      AUD_BI_PORT_B_L - @m42a_lib.M42A    54C1 57A6
                     AUD_BI_PORT_B_R - @m42a_lib.M42A    54C1 57A6
AUD_BI_PORT_C_L      AUD_BI_PORT_C_L - @m42a_lib.M42A    54C7 55B8
AUD_BI_PORT_C_R      AUD_BI_PORT_C_R - @m42a_lib.M42A    54C7 55C8
AUD_BI_PORT_D_L      AUD_BI_PORT_D_L - @m42a_lib.M42A    54C7 57A5
AUD_BI_PORT_D_R      AUD_BI_PORT_D_R - @m42a_lib.M42A    54C7 55A8
AUD_BI_PORT_E_L      AUD_BI_PORT_E_L - @m42a_lib.M42A    54C1 57A5
AUD_BI_PORT_E_R      AUD_BI_PORT_E_R - @m42a_lib.M42A    54C1 57A5
AUD_BI_PORT_F_L      AUD_BI_PORT_F_L - @m42a_lib.M42A    54C1 57B3
AUD_BI_PORT_F_R      AUD_BI_PORT_F_R - @m42a_lib.M42A    54C1 57A3
AUD_BYPASS           AUD_BYPASS - @m42a_lib.M42A         54C4
AUD_CONNJ1_RING      AUD_CONNJ1_RING - @m42a_lib.M42A    56C7
AUD_CONNJ1_RING_F    AUD_CONNJ1_RING_F - @m42a_lib.M42A  56C6
AUD_CONNJ1_SLEEVE    AUD_CONNJ1_SLEEVE - @m42a_lib.M42A  56D7
AUD_CONNJ1_SLEEVEDET AUD_CONNJ1_SLEEVEDET -              56C7
                     @m42a_lib.M42A
AUD_CONNJ1_SLEEVEDET AUD_CONNJ1_SLEEVEDET_F -            56C6
_F                   @m42a_lib.M42A
AUD_CONNJ1_SLEEVE_F  AUD_CONNJ1_SLEEVE_F -               56D5
                     @m42a_lib.M42A
AUD_CONNJ1_TIP       AUD_CONNJ1_TIP - @m42a_lib.M42A     56C7
AUD_CONNJ1_TIPDET    AUD_CONNJ1_TIPDET - @m42a_lib.M42A  56D7
AUD_CONNJ1_TIPDET_F  AUD_CONNJ1_TIPDET_F -               56D6
                     @m42a_lib.M42A
AUD_CONNJ1_TIP_F     AUD_CONNJ1_TIP_F - @m42a_lib.M42A   56C6
AUD_CONNJ2_RING      AUD_CONNJ2_RING - @m42a_lib.M42A    56B7
AUD_CONNJ2_RING_F    AUD_CONNJ2_RING_F - @m42a_lib.M42A  56B6
AUD_CONNJ2_SLEEVE    AUD_CONNJ2_SLEEVE - @m42a_lib.M42A  56B7
AUD_CONNJ2_SLEEVEDET AUD_CONNJ2_SLEEVEDET -              56A7
                     @m42a_lib.M42A
AUD_CONNJ2_SLEEVEDET AUD_CONNJ2_SLEEVEDET_F -            56A6
_F                   @m42a_lib.M42A
AUD_CONNJ2_SLEEVE_F  AUD_CONNJ2_SLEEVE_F -               56B6
                     @m42a_lib.M42A
AUD_CONNJ2_TIP       AUD_CONNJ2_TIP - @m42a_lib.M42A     56B7
AUD_CONNJ2_TIPDET    AUD_CONNJ2_TIPDET - @m42a_lib.M42A  56B7
AUD_CONNJ2_TIPDET_F  AUD_CONNJ2_TIPDET_F -               56B6
                     @m42a_lib.M42A
AUD_CONNJ2_TIP_F     AUD_CONNJ2_TIP_F - @m42a_lib.M42A   56B6
AUD_GPIO_0           AUD_GPIO_0 - @m42a_lib.M42A         54B8 55A8
AUD_GPIO_0_R         AUD_GPIO_0_R - @m42a_lib.M42A       54B7 54C7
AUD_GPIO_1           AUD_GPIO_1 - @m42a_lib.M42A         54B8 57C3
AUD_GPIO_1_R         AUD_GPIO_1_R - @m42a_lib.M42A       54A7 54C7
AUD_GPIO_2           AUD_GPIO_2 - @m42a_lib.M42A         54C7
AUD_INJACK_INSERT_L  AUD_INJACK_INSERT_L -               57C7
                     @m42a_lib.M42A
AUD_J1_COM           AUD_J1_COM - @m42a_lib.M42A         56C4
AUD_J1_DET_RC        AUD_J1_DET_RC - @m42a_lib.M42A      57D7
AUD_J1_SLEEVEDET_INV AUD_J1_SLEEVEDET_INV -              57C7
                     @m42a_lib.M42A
AUD_J1_SLEEVEDET_R   AUD_J1_SLEEVEDET_R - @m42a_lib.M42A 56C3 57C6 57C8
AUD_J1_TIPDET_R      AUD_J1_TIPDET_R - @m42a_lib.M42A    56C3 57D8
AUD_J2_COM           AUD_J2_COM - @m42a_lib.M42A         56B4
AUD_J2_DET_RC        AUD_J2_DET_RC - @m42a_lib.M42A      57B7
AUD_J2_OPT_OUT       AUD_J2_OPT_OUT - @m42a_lib.M42A     56B7
AUD_J2_SLEEVEDET_R   AUD_J2_SLEEVEDET_R - @m42a_lib.M42A 56A4 57B8
AUD_J2_TIPDET_R      AUD_J2_TIPDET_R - @m42a_lib.M42A    56A4 57B8
AUD_JDREF            AUD_JDREF - @m42a_lib.M42A          54C4
AUD_OUTJACK_INSERT_L AUD_OUTJACK_INSERT_L -              57D7
                     @m42a_lib.M42A
AUD_PORTA_DET_L      AUD_PORTA_DET_L - @m42a_lib.M42A    57D5
AUD_PORTA_L          AUD_PORTA_L - @m42a_lib.M42A        56C3 57D1
AUD_PORTA_L_R        AUD_PORTA_L_R - @m42a_lib.M42A      57B1 57D3
AUD_PORTA_R          AUD_PORTA_R - @m42a_lib.M42A        56C3 57C1
AUD_PORTA_R_R        AUD_PORTA_R_R - @m42a_lib.M42A      57B1 57C3
AUD_PORTE_DET_L      AUD_PORTE_DET_L - @m42a_lib.M42A    57D5
AUD_PORTF_L          AUD_PORTF_L - @m42a_lib.M42A        56B4 57B1
AUD_PORTF_L_R        AUD_PORTF_L_R - @m42a_lib.M42A      57B2
AUD_PORTF_R          AUD_PORTF_R - @m42a_lib.M42A        56B4 57A1
AUD_PORTF_R_R        AUD_PORTF_R_R - @m42a_lib.M42A      57A2
AUD_PORTG_DET_L      AUD_PORTG_DET_L - @m42a_lib.M42A    57C5
AUD_SENSE_A          AUD_SENSE_A - @m42a_lib.M42A        54C1 57C5 57D8
AUD_SENSE_B          AUD_SENSE_B - @m42a_lib.M42A        54C1 57C4 57C8 57D8
AUD_SPDIF_IN         AUD_SPDIF_IN - @m42a_lib.M42A       54C1 56B3
AUD_SPDIF_OUT        AUD_SPDIF_OUT - @m42a_lib.M42A      54D1 56D3
AUD_SPDIF_OUT_R      AUD_SPDIF_OUT_R - @m42a_lib.M42A    54D4
AUD_SPKRAMP_INL      AUD_SPKRAMP_INL - @m42a_lib.M42A    55B6
AUD_SPKRAMP_INL_L    AUD_SPKRAMP_INL_L - @m42a_lib.M42A  55B7
AUD_SPKRAMP_INR      AUD_SPKRAMP_INR - @m42a_lib.M42A    55C6
AUD_SPKRAMP_INR_L    AUD_SPKRAMP_INR_L - @m42a_lib.M42A  55C7
AUD_SPKRAMP_INSUB    AUD_SPKRAMP_INSUB - @m42a_lib.M42A  55A6
AUD_SPKRAMP_INSUB_L  AUD_SPKRAMP_INSUB_L -               55A7
                     @m42a_lib.M42A
AUD_SPKRAMP_SHUTDOWN AUD_SPKRAMP_SHUTDOWN_L -            55A6 55B8 55C8
_L                   @m42a_lib.M42A
AUD_VREF_FILT        AUD_VREF_FILT - @m42a_lib.M42A      54C4
AUD_VREF_PORT_B      AUD_VREF_PORT_B - @m42a_lib.M42A    54C1 57A6
BAL_IN_COM           BAL_IN_COM - @m42a_lib.M42A         54C7 57A3
BAL_IN_L             BAL_IN_L - @m42a_lib.M42A           54C7 57A3
BAL_IN_R             BAL_IN_R - @m42a_lib.M42A           54C7 57A3
BATT_ENABLE_L        BATT_ENABLE_L - @m42a_lib.M42A      66A4
BATT_FET_DRAIN       BATT_FET_DRAIN - @m42a_lib.M42A     66A5
BATT_FET_GATE        BATT_FET_GATE - @m42a_lib.M42A      66A4
BATT_IN              BATT_IN - @m42a_lib.M42A            5D1
BATT_ISENSE          BATT_ISENSE - @m42a_lib.M42A        66B2
BATT_NEG             BATT_NEG - @m42a_lib.M42A           5D1 65A6
BATT_POS             BATT_POS - @m42a_lib.M42A           5D1 65A6
BATT_POS_F           BATT_POS_F - @m42a_lib.M42A         65A2 66B2
BATT_RC              BATT_RC - @m42a_lib.M42A            66A5
BEEP                 BEEP - @m42a_lib.M42A               54C6
BIOS_REC             BIOS_REC - @m42a_lib.M42A           23A6 23C5
BKLIGHT_CTL          BKLIGHT_CTL - @m42a_lib.M42A        67C4
BOOT_LPC_SPI_L       BOOT_LPC_SPI_L - @m42a_lib.M42A     5C2 22B3 45C8 47C6
BYPASS_R_DRV         BYPASS_R_DRV - @m42a_lib.M42A       66A3
BYPASS_R_GATE        BYPASS_R_GATE - @m42a_lib.M42A      66A3
CHASSIS_AUDIO_JACK_I CHASSIS_AUDIO_JACK_ISOL -           56A3 56A8 56B1 56B6 56B6
SOL                  @m42a_lib.M42A                      56C1 56C1 56C8
CHGR_ACLIM           CHGR_ACLIM - @m42a_lib.M42A         66C6
CHGR_ACPRN           CHGR_ACPRN - @m42a_lib.M42A         66B6
CHGR_ACSET           CHGR_ACSET - @m42a_lib.M42A         66C6
CHGR_ACSET_RC        CHGR_ACSET_RC - @m42a_lib.M42A      66C8
CHGR_BGATE           CHGR_BGATE - @m42a_lib.M42A         66C5
CHGR_BOOT            CHGR_BOOT - @m42a_lib.M42A          66C5
CHGR_BOOT_RC         CHGR_BOOT_RC - @m42a_lib.M42A       66C4
CHGR_CHLIM           CHGR_CHLIM - @m42a_lib.M42A         66B6
CHGR_CSIN            CHGR_CSIN - @m42a_lib.M42A          66C5
CHGR_CSON            CHGR_CSON - @m42a_lib.M42A          66C6
CHGR_CSOP            CHGR_CSOP - @m42a_lib.M42A          66C6
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CHGR_DCIN            CHGR_DCIN - @m42a_lib.M42A          66C5
CHGR_DCPRN           CHGR_DCPRN - @m42a_lib.M42A         66B5
CHGR_DCSET           CHGR_DCSET - @m42a_lib.M42A         66B5
CHGR_EN              CHGR_EN - @m42a_lib.M42A            66B5
CHGR_EN_L            CHGR_EN_L - @m42a_lib.M42A          66A6
CHGR_ICM             CHGR_ICM - @m42a_lib.M42A           66C6
CHGR_ICM_R           CHGR_ICM_R - @m42a_lib.M42A         66C6
CHGR_ICOMP           CHGR_ICOMP - @m42a_lib.M42A         66C6
CHGR_ICOMP_RC        CHGR_ICOMP_RC - @m42a_lib.M42A      66C7
CHGR_LGATE           CHGR_LGATE - @m42a_lib.M42A         66C5
CHGR_PHASE           CHGR_PHASE - @m42a_lib.M42A         66C5
CHGR_PHASE_RC        CHGR_PHASE_RC - @m42a_lib.M42A      66B4
CHGR_SGATE           CHGR_SGATE - @m42a_lib.M42A         66C5
CHGR_UGATE           CHGR_UGATE - @m42a_lib.M42A         66C5
CHGR_VADJ            CHGR_VADJ - @m42a_lib.M42A          66B6 66C6
CHGR_VCOMP           CHGR_VCOMP - @m42a_lib.M42A         66C6
CHGR_VCOMP_CC        CHGR_VCOMP_CC - @m42a_lib.M42A      66C7
CHGR_VCOMP_RC        CHGR_VCOMP_RC - @m42a_lib.M42A      66C7
CHGR_VDD             CHGR_VDD - @m42a_lib.M42A           66B6 66D6
CHGR_VDDP            CHGR_VDDP - @m42a_lib.M42A          66C5
CHGR_VREF            CHGR_VREF - @m42a_lib.M42A          66B6
CK410_CLK14P3M_TIMER CK410_CLK14P3M_TIMER -              32A4 33B8
                     @m42a_lib.M42A
CK410_CPU0_N         CK410_CPU0_N - @m42a_lib.M42A       5C7 32C4 33D5
CK410_CPU0_P         CK410_CPU0_P - @m42a_lib.M42A       5C7 32C4 33D5
CK410_CPU1_N         CK410_CPU1_N - @m42a_lib.M42A       5C7 32C4 33D5
CK410_CPU1_P         CK410_CPU1_P - @m42a_lib.M42A       5C7 32C4 33D5
CK410_CPU2_ITP_SRC10 CK410_CPU2_ITP_SRC10_N -            5C7 32C4 33D5
_N                   @m42a_lib.M42A
CK410_CPU2_ITP_SRC10 CK410_CPU2_ITP_SRC10_P -            5C7 32C4 33D5
_P                   @m42a_lib.M42A
CK410_DOT96_27M_N    CK410_DOT96_27M_N - @m42a_lib.M42A  5C7 32A4 33B5
CK410_DOT96_27M_P    CK410_DOT96_27M_P - @m42a_lib.M42A  5C7 32A4 33B5
CK410_FSB_TEST_MODE  CK410_FSB_TEST_MODE -               32C6 33B8
                     @m42a_lib.M42A
CK410_IREF           CK410_IREF - @m42a_lib.M42A         32B6
CK410_LVDS_N         CK410_LVDS_N - @m42a_lib.M42A       5C7 32B4 33A5
CK410_LVDS_P         CK410_LVDS_P - @m42a_lib.M42A       5C7 32B4 33A5
CK410_PCI1_CLK       CK410_PCI1_CLK - @m42a_lib.M42A     32B6 33D8
CK410_PCI2_CLK       CK410_PCI2_CLK - @m42a_lib.M42A     32B6 33D8
CK410_PCI3_CLK       CK410_PCI3_CLK - @m42a_lib.M42A     32B6 33D8
CK410_PCI4_CLK       CK410_PCI4_CLK - @m42a_lib.M42A     32B6
CK410_PCI4_CLK_SPN   CK410_PCI4_CLK_SPN - @m42a_lib.M42A 5C7
CK410_PCI5_FCTSEL1   CK410_PCI5_FCTSEL1 - @m42a_lib.M42A 32B6 33A8
CK410_PCIF0_CLK      CK410_PCIF0_CLK - @m42a_lib.M42A    32B7 33D8
CK410_PCIF1_CLK      CK410_PCIF1_CLK - @m42a_lib.M42A    5C7 32B6 33D8
CK410_PD_VTT_PWRGD_L CK410_PD_VTT_PWRGD_L -              26A8 32A4
                     @m42a_lib.M42A
                     VR_PWRGD_CK410_L - @m42a_lib.M42A   26A7 58C7
CK410_REF1_FCTSEL0   CK410_REF1_FCTSEL0 - @m42a_lib.M42A 32A4 33A8
CK410_SRC1_N         CK410_SRC1_N - @m42a_lib.M42A       6B4 32B4
                     CK410_SRC1_N_SPN - @m42a_lib.M42A   5C7 6B3
CK410_SRC1_P         CK410_SRC1_P - @m42a_lib.M42A       6B4 32B4
                     CK410_SRC1_P_SPN - @m42a_lib.M42A   5C7 6B3
CK410_SRC2_N         CK410_SRC2_N - @m42a_lib.M42A       5C7 32B4 33C5
CK410_SRC2_P         CK410_SRC2_P - @m42a_lib.M42A       5C7 32B4 33C5
CK410_SRC3_N         CK410_SRC3_N - @m42a_lib.M42A       6B4 32B4
                     CK410_SRC3_N_SPN - @m42a_lib.M42A   5C7 6B3
CK410_SRC3_P         CK410_SRC3_P - @m42a_lib.M42A       6B4 32B4
                     CK410_SRC3_P_SPN - @m42a_lib.M42A   5C7 6B3
CK410_SRC4_N         CK410_SRC4_N - @m42a_lib.M42A       5C7 32B4 33B5
CK410_SRC4_P         CK410_SRC4_P - @m42a_lib.M42A       5C7 32B4 33B5
CK410_SRC5_N         CK410_SRC5_N - @m42a_lib.M42A       5C7 32B4 33C5
CK410_SRC5_P         CK410_SRC5_P - @m42a_lib.M42A       5C7 32B4 33C5
CK410_SRC6_N         CK410_SRC6_N - @m42a_lib.M42A       5C7 32B4 33C5
CK410_SRC6_P         CK410_SRC6_P - @m42a_lib.M42A       5C7 32B4 33D5
CK410_SRC7_N         CK410_SRC7_N - @m42a_lib.M42A       6B4 32B4
                     CK410_SRC7_N_SPN - @m42a_lib.M42A   5C7 6B3
CK410_SRC7_P         CK410_SRC7_P - @m42a_lib.M42A       6B4 32B4
                     CK410_SRC7_P_SPN - @m42a_lib.M42A   5C7 6B3
CK410_SRC8_N         CK410_SRC8_N - @m42a_lib.M42A       5B7 32A4 33C5
CK410_SRC8_P         CK410_SRC8_P - @m42a_lib.M42A       5B7 32A4 33C5
CK410_SRC_CLKREQ1_L  CK410_SRC_CLKREQ1_L -               6B4 32B4
                     @m42a_lib.M42A
                     CK410_SRC_CLKREQ1_L_SPN -           5B7 6B3
                     @m42a_lib.M42A
CK410_SRC_CLKREQ3_L  CK410_SRC_CLKREQ3_L -               6B4 32B4
                     @m42a_lib.M42A
                     CK410_SRC_CLKREQ3_L_SPN -           5B7 6B3
                     @m42a_lib.M42A
CK410_SRC_CLKREQ6_L  CK410_SRC_CLKREQ6_L -               32B4 43C6
                     @m42a_lib.M42A
CK410_SRC_CLKREQ8_L  CK410_SRC_CLKREQ8_L -               5B7 32A4 33A5
                     @m42a_lib.M42A
CK410_USB48_FSA      CK410_USB48_FSA - @m42a_lib.M42A    32A4 33C8
CK410_XTAL_IN        CK410_XTAL_IN - @m42a_lib.M42A      32C6
CK410_XTAL_OUT       CK410_XTAL_OUT - @m42a_lib.M42A     32C6
CLK_NB_OE_L          CLK_NB_OE_L - @m42a_lib.M42A        14B6 32B4
CONN_GEYSER_ONOFF_FL CONN_GEYSER_ONOFF_FLTR_L -          40C6
TR_L                 @m42a_lib.M42A
CONN_GEYSER_USB_N    CONN_GEYSER_USB_N - @m42a_lib.M42A  40C6
CONN_GEYSER_USB_P    CONN_GEYSER_USB_P - @m42a_lib.M42A  40C6
CPUVCORE_ISENSE_CAL  CPUVCORE_ISENSE_CAL -               48A5
                     @m42a_lib.M42A
CPU_A20M_L           CPU_A20M_L - @m42a_lib.M42A         7C8 21C4
CPU_BSEL<0>          CPU_BSEL<0> - @m42a_lib.M42A        7B4 33C6
CPU_BSEL<1>          CPU_BSEL<1> - @m42a_lib.M42A        7B4 33B6
CPU_BSEL<2>          CPU_BSEL<2> - @m42a_lib.M42A        7B4 33B6
CPU_BSEL_R<0>        CPU_BSEL_R<0> - @m42a_lib.M42A      33C7
CPU_BSEL_R<1>        CPU_BSEL_R<1> - @m42a_lib.M42A      33B7
CPU_BSEL_R<2>        CPU_BSEL_R<2> - @m42a_lib.M42A      33B7
CPU_COMP<0>          CPU_COMP<0> - @m42a_lib.M42A        7B3
CPU_COMP<1>          CPU_COMP<1> - @m42a_lib.M42A        7B3
CPU_COMP<2>          CPU_COMP<2> - @m42a_lib.M42A        7B3
CPU_COMP<3>          CPU_COMP<3> - @m42a_lib.M42A        7B3
CPU_DPRSTP_L         CPU_DPRSTP_L - @m42a_lib.M42A       7B3 21C4 58C7
CPU_DPSLP_L          CPU_DPSLP_L - @m42a_lib.M42A        7B3 21C4
CPU_FERR_L           CPU_FERR_L - @m42a_lib.M42A         7C8 21C2
CPU_GTLREF           CPU_GTLREF - @m42a_lib.M42A         7B4
CPU_IGNNE_L          CPU_IGNNE_L - @m42a_lib.M42A        7C8 21C4
CPU_INIT_L           CPU_INIT_L - @m42a_lib.M42A         7D6 21C4
CPU_INTR             CPU_INTR - @m42a_lib.M42A           7C8 21C4
CPU_ISENSE_OUT_R     CPU_ISENSE_OUT_R - @m42a_lib.M42A   48C3
CPU_ISENSE_R_N       CPU_ISENSE_R_N - @m42a_lib.M42A     48C3
CPU_ISENSE_R_P       CPU_ISENSE_R_P - @m42a_lib.M42A     48C3
CPU_NMI              CPU_NMI - @m42a_lib.M42A            7C8 21C4
CPU_PROCHOT_L        CPU_PROCHOT_L - @m42a_lib.M42A      7C6 46B5 46C2 58C8
CPU_PSI_L            CPU_PSI_L - @m42a_lib.M42A          7A3 58C7
CPU_PWRGD            CPU_PWRGD - @m42a_lib.M42A          7B3 21C4
CPU_RCIN_L           CPU_RCIN_L - @m42a_lib.M42A         21C4
CPU_SMI_L            CPU_SMI_L - @m42a_lib.M42A          7C8 21C4
CPU_STPCLK_L         CPU_STPCLK_L - @m42a_lib.M42A       7C8 21C4
CPU_TEST1            CPU_TEST1 - @m42a_lib.M42A          7B4
CPU_TEST2            CPU_TEST2 - @m42a_lib.M42A          7B4
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CPU_THERMAL_SCREW_DO CPU_THERMAL_SCREW_DOWN -            6A8
WN                   @m42a_lib.M42A
CPU_THERMAL_SCREW_RI CPU_THERMAL_SCREW_RIGHT -           6A7
GHT                  @m42a_lib.M42A
CPU_THERMAL_SCREW_UP CPU_THERMAL_SCREW_UP -              6A7
                     @m42a_lib.M42A
CPU_THERMD_N         CPU_THERMD_N - @m42a_lib.M42A       7C6 10B6
CPU_THERMD_P         CPU_THERMD_P - @m42a_lib.M42A       7C6 10B6
CPU_THERMTRIP_R      CPU_THERMTRIP_R - @m42a_lib.M42A    21C2
CPU_VCCSENSE_N       CPU_VCCSENSE_N - @m42a_lib.M42A     8B6 58A4 58A5
CPU_VCCSENSE_P       CPU_VCCSENSE_P - @m42a_lib.M42A     8B6 58A4 58A5
CPU_VID<0>           CPU_VID<0> - @m42a_lib.M42A         8B7 9C3
CPU_VID<1>           CPU_VID<1> - @m42a_lib.M42A         8B7 9C3
CPU_VID<2>           CPU_VID<2> - @m42a_lib.M42A         8B7 9C3
CPU_VID<3>           CPU_VID<3> - @m42a_lib.M42A         8B7 9C3
CPU_VID<4>           CPU_VID<4> - @m42a_lib.M42A         8B7 9C3
CPU_VID<5>           CPU_VID<5> - @m42a_lib.M42A         8B7 9D3
CPU_VID<6>           CPU_VID<6> - @m42a_lib.M42A         8B7 9D3
CPU_VID_R<0>         CPU_VID_R<0> - @m42a_lib.M42A       9C2 58C7
CPU_VID_R<0..6>      CPU_VID_R<0..6> - @m42a_lib.M42A    58A4
CPU_VID_R<1>         CPU_VID_R<1> - @m42a_lib.M42A       9C2 58C7
CPU_VID_R<2>         CPU_VID_R<2> - @m42a_lib.M42A       9C2 58C7
CPU_VID_R<3>         CPU_VID_R<3> - @m42a_lib.M42A       9C2 58C7
CPU_VID_R<4>         CPU_VID_R<4> - @m42a_lib.M42A       9C2 58C7
CPU_VID_R<5>         CPU_VID_R<5> - @m42a_lib.M42A       9D2 58C7
CPU_VID_R<6>         CPU_VID_R<6> - @m42a_lib.M42A       9D2 58C7
CPU_XDP_CLK_N        CPU_XDP_CLK_N - @m42a_lib.M42A      11B3 33D2 33D3
CPU_XDP_CLK_P        CPU_XDP_CLK_P - @m42a_lib.M42A      11B3 33D2 33D3
CRB_SV_DET           CRB_SV_DET - @m42a_lib.M42A         23B6 23C3
CRT_BLUE             CRT_BLUE - @m42a_lib.M42A           13B5 69B8
CRT_DDC_CLK          CRT_DDC_CLK - @m42a_lib.M42A        13B5 69D7
CRT_DDC_DATA         CRT_DDC_DATA - @m42a_lib.M42A       13B5 69D7
CRT_GREEN            CRT_GREEN - @m42a_lib.M42A          13B5 69A8
CRT_HSYNC_LS         CRT_HSYNC_LS - @m42a_lib.M42A       69C2
CRT_HSYNC_LS_R       CRT_HSYNC_LS_R - @m42a_lib.M42A     69C3
CRT_HSYNC_R          CRT_HSYNC_R - @m42a_lib.M42A        13B5 69C3
CRT_IREF             CRT_IREF - @m42a_lib.M42A           13B5 69C8
CRT_RED              CRT_RED - @m42a_lib.M42A            13B5 69A8
CRT_VSYNC_LS         CRT_VSYNC_LS - @m42a_lib.M42A       69C2
CRT_VSYNC_LS_R       CRT_VSYNC_LS_R - @m42a_lib.M42A     69C3
CRT_VSYNC_R          CRT_VSYNC_R - @m42a_lib.M42A        13B5 69C3
DCIN_ISENSE          DCIN_ISENSE - @m42a_lib.M42A        66C3
DEBUG_RST_L          DEBUG_RST_L - @m42a_lib.M42A        5C2 26B1 47C6
DMI_IRCOMP_R         DMI_IRCOMP_R - @m42a_lib.M42A       22C2
DMI_N2S_N<0>         DMI_N2S_N<0> - @m42a_lib.M42A       14B4 22D2
DMI_N2S_N<1>         DMI_N2S_N<1> - @m42a_lib.M42A       14B4 22D2
DMI_N2S_N<2>         DMI_N2S_N<2> - @m42a_lib.M42A       14B4 22D2
DMI_N2S_N<3>         DMI_N2S_N<3> - @m42a_lib.M42A       14B4 22D2
DMI_N2S_P<0>         DMI_N2S_P<0> - @m42a_lib.M42A       14B4 22D2
DMI_N2S_P<1>         DMI_N2S_P<1> - @m42a_lib.M42A       14B4 22D2
DMI_N2S_P<2>         DMI_N2S_P<2> - @m42a_lib.M42A       14B4 22D2
DMI_N2S_P<3>         DMI_N2S_P<3> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_N<0>         DMI_S2N_N<0> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_N<1>         DMI_S2N_N<1> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_N<2>         DMI_S2N_N<2> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_N<3>         DMI_S2N_N<3> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_P<0>         DMI_S2N_P<0> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_P<1>         DMI_S2N_P<1> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_P<2>         DMI_S2N_P<2> - @m42a_lib.M42A       14B4 22D2
DMI_S2N_P<3>         DMI_S2N_P<3> - @m42a_lib.M42A       14B4 22D2
ENETPWR_EN           ENETPWR_EN - @m42a_lib.M42A         60B5 60C5 60D4
ENET_BOB_SMITH_CAP   ENET_BOB_SMITH_CAP - @m42a_lib.M42A 37A5
ENET_CENTER_TAP<0>   ENET_CENTER_TAP<0> - @m42a_lib.M42A 37C6
ENET_CENTER_TAP<1>   ENET_CENTER_TAP<1> - @m42a_lib.M42A 37B6
ENET_CENTER_TAP<2>   ENET_CENTER_TAP<2> - @m42a_lib.M42A 37B6
ENET_CENTER_TAP<3>   ENET_CENTER_TAP<3> - @m42a_lib.M42A 37B6
ENET_CLK100M_PCIE_N  ENET_CLK100M_PCIE_N -               33C3 33D2 36C6
                     @m42a_lib.M42A
ENET_CLK100M_PCIE_P  ENET_CLK100M_PCIE_P -               33C3 33D2 36C6
                     @m42a_lib.M42A
ENET_CTRL12          ENET_CTRL12 - @m42a_lib.M42A        6A4 36C8
                     ENET_CTRL12_SPN - @m42a_lib.M42A    6A3
ENET_CTRL25          ENET_CTRL25 - @m42a_lib.M42A        6A4 36C8
                     ENET_CTRL25_SPN - @m42a_lib.M42A    6A3
ENET_LOM_DIS_L       ENET_LOM_DIS_L - @m42a_lib.M42A     36D8
ENET_MDI0            ENET_MDI0 - @m42a_lib.M42A          36B5
ENET_MDI1            ENET_MDI1 - @m42a_lib.M42A          36B4
ENET_MDI2            ENET_MDI2 - @m42a_lib.M42A          36B4
ENET_MDI3            ENET_MDI3 - @m42a_lib.M42A          36B3
ENET_MDI_N<0>        ENET_MDI_N<0> - @m42a_lib.M42A      36C3 37C8
ENET_MDI_N<1>        ENET_MDI_N<1> - @m42a_lib.M42A      36C3 37B8
ENET_MDI_N<2>        ENET_MDI_N<2> - @m42a_lib.M42A      36C3 37B8
ENET_MDI_N<3>        ENET_MDI_N<3> - @m42a_lib.M42A      36C3 37B8
ENET_MDI_P<0>        ENET_MDI_P<0> - @m42a_lib.M42A      36C3 37C8
ENET_MDI_P<1>        ENET_MDI_P<1> - @m42a_lib.M42A      36C3 37B8
ENET_MDI_P<2>        ENET_MDI_P<2> - @m42a_lib.M42A      36C3 37B8
ENET_MDI_P<3>        ENET_MDI_P<3> - @m42a_lib.M42A      36C3 37B8
ENET_MDI_TRAN_N<0>   ENET_MDI_TRAN_N<0> - @m42a_lib.M42A 37C5
ENET_MDI_TRAN_N<1>   ENET_MDI_TRAN_N<1> - @m42a_lib.M42A 37B5
ENET_MDI_TRAN_N<2>   ENET_MDI_TRAN_N<2> - @m42a_lib.M42A 5A7 37B5
ENET_MDI_TRAN_N<3>   ENET_MDI_TRAN_N<3> - @m42a_lib.M42A 37B5
ENET_MDI_TRAN_P<0>   ENET_MDI_TRAN_P<0> - @m42a_lib.M42A 37C5
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ENET_RST_L           ENET_RST_L - @m42a_lib.M42A         26A1 36C6
ENET_VPD_CLK         ENET_VPD_CLK - @m42a_lib.M42A       36A2 36C6
ENET_VPD_DATA        ENET_VPD_DATA - @m42a_lib.M42A      36A2 36C6
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EXTBUSB_OC_F_L       EXTBUSB_OC_F_L - @m42a_lib.M42A     42C8
EXT_COMPVID_B        EXT_COMPVID_B - @m42a_lib.M42A      69B6
EXT_C_R              EXT_C_R - @m42a_lib.M42A            69A6
EXT_Y_G              EXT_Y_G - @m42a_lib.M42A            69A6
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                     SMC_CPU_INIT_3_3_L - @m42a_lib.M42A 6B1 45D5
FWH_MFG_MODE         FWH_MFG_MODE - @m42a_lib.M42A       23A6 23C5
FWPWR_ACIN           FWPWR_ACIN - @m42a_lib.M42A         39C6
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FWPWR_EN_L_R	FWPWR_EN_L_R - @m42a_lib.M42A	60C7
FWPWR_RUN	FWPWR_RUN - @m42a_lib.M42A	39C6
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	FW_PORT0_TPA_N - @m42a_lib.M42A	39B5
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	FW_PORT0_TPA_P - @m42a_lib.M42A	39B5
FW_A_TPBIAS	FW_A_TPBIAS - @m42a_lib.M42A	38B3 39B6
FW_A_TPB_N	FW_A_TPB_N - @m42a_lib.M42A	38B3 39B6
	FW_PORT0_TPB_N - @m42a_lib.M42A	39B5
FW_A_TPB_P	FW_A_TPB_P - @m42a_lib.M42A	38B3 39B6
	FW_PORT0_TPB_P - @m42a_lib.M42A	39B5
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	FW_B_TPA_N_SPN - @m42a_lib.M42A	5B7 6D1
FW_B_TPA_P	FW_B_TPA_P - @m42a_lib.M42A	6D2 38B3
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	FW_B_TPB_N_SPN - @m42a_lib.M42A	5B7 6D1
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	FW_C_TPB_P_SPN - @m42a_lib.M42A	5B7 6D1
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FW_PORT0_TPB_N_FL	FW_PORT0_TPB_N_FL - @m42a_lib.M42A	39B2
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FW_PWRON_RST_L	FW_PWRON_RST_L - @m42a_lib.M42A	38C3
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GND_5V3V3S5_SGND	GND_5V3V3S5_SGND - @m42a_lib.M42A	59B7
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GND_BT_F	GND_BT_F - @m42a_lib.M42A	44B4
GND_CHASSIS_CPU	GND_CHASSIS_CPU - @m42a_lib.M42A	6B8
GND_CHASSIS_FANSCREW	GND_CHASSIS_FANSCREW - @m42a_lib.M42A	6B8
GND_CHGR_SGND	GND_CHGR_SGND - @m42a_lib.M42A	66A5 66B7
GND_IMVP6_SGND	GND_IMVP6_SGND - @m42a_lib.M42A	58A4 58B7 58C8
GND_SMC_AVSS	GND_SMC_AVSS - @m42a_lib.M42A	45C2 45C4 46B6 48A1 48B5 48C1 61C1 62A5 66B1 66C2
GND_SMC_LID_F	GND_SMC_LID_F - @m42a_lib.M42A	65A7
GPU_CRT_DDC_CLK	GPU_CRT_DDC_CLK - @m42a_lib.M42A	69B6 69D5
GPU_CRT_DDC_DATA	GPU_CRT_DDC_DATA - @m42a_lib.M42A	69B6 69D5
IDE_CSEL_PD	IDE_CSEL_PD - @m42a_lib.M42A	34B4
IDE_IRQ14	IDE_IRQ14 - @m42a_lib.M42A	21B6 34B6
IDE_PDA<0>	IDE_PDA<0> - @m42a_lib.M42A	21B5 34B5
IDE_PDA<1>	IDE_PDA<1> - @m42a_lib.M42A	21B5 34B5
IDE_PDA<2>	IDE_PDA<2> - @m42a_lib.M42A	21B5 34B3
IDE_PDCS1_L	IDE_PDCS1_L - @m42a_lib.M42A	21B5 34B5
IDE_PDCS3_L	IDE_PDCS3_L - @m42a_lib.M42A	21B5 34B3
IDE_PDD<0>	IDE_PDD<0> - @m42a_lib.M42A	21C5 34C5
IDE_PDD<1>	IDE_PDD<1> - @m42a_lib.M42A	21B5 34C5
IDE_PDD<2>	IDE_PDD<2> - @m42a_lib.M42A	21B5 34C5
IDE_PDD<3>	IDE_PDD<3> - @m42a_lib.M42A	21B5 34C5
IDE_PDD<4>	IDE_PDD<4> - @m42a_lib.M42A	21B5 34C5
IDE_PDD<5>	IDE_PDD<5> - @m42a_lib.M42A	21B5 34C5
IDE_PDD<6>	IDE_PDD<6> - @m42a_lib.M42A	21B5 34C5
IDE_PDD<7>	IDE_PDD<7> - @m42a_lib.M42A	21B5 34C5
IDE_PDD<8>	IDE_PDD<8> - @m42a_lib.M42A	21B5 34C3
IDE_PDD<9>	IDE_PDD<9> - @m42a_lib.M42A	21B5 34C3
IDE_PDD<10>	IDE_PDD<10> - @m42a_lib.M42A	21B5 34C3
IDE_PDD<11>	IDE_PDD<11> - @m42a_lib.M42A	21B5 34C3
IDE_PDD<12>	IDE_PDD<12> - @m42a_lib.M42A	21B5 34C3
IDE_PDD<13>	IDE_PDD<13> - @m42a_lib.M42A	21B5 34C3
IDE_PDD<14>	IDE_PDD<14> - @m42a_lib.M42A	21B5 34C3
IDE_PDD<15>	IDE_PDD<15> - @m42a_lib.M42A	21B5 34C3
IDE_PDDACK_L	IDE_PDDACK_L - @m42a_lib.M42A	21B6 34B3
IDE_PDDREQ	IDE_PDDREQ - @m42a_lib.M42A	21B6 34B6
IDE_PDIORDY	IDE_PDIORDY - @m42a_lib.M42A	21B6 34B6
IDE_PDIOR_L	IDE_PDIOR_L - @m42a_lib.M42A	21B6 34C3
IDE_PDIOW_L	IDE_PDIOW_L - @m42a_lib.M42A	21B6 34B5
IDE_RESET_L	IDE_RESET_L - @m42a_lib.M42A	23A3 34C5
IMVP6_BOOT1	IMVP6_BOOT1 - @m42a_lib.M42A	58A8 58C6
IMVP6_BOOT1_RC	IMVP6_BOOT1_RC - @m42a_lib.M42A	58D5
IMVP6_BOOT2	IMVP6_BOOT2 - @m42a_lib.M42A	58A6 58C6
IMVP6_BOOT2_RC	IMVP6_BOOT2_RC - @m42a_lib.M42A	58C5
IMVP6_COMP	IMVP6_COMP - @m42a_lib.M42A	5D7 58A4 58B7
IMVP6_COMP_RC	IMVP6_COMP_RC - @m42a_lib.M42A	58B8
IMVP6_CPU_ISENSE_N	IMVP6_CPU_ISENSE_N - @m42a_lib.M42A	48C4
IMVP6_CPU_ISENSE_P	IMVP6_CPU_ISENSE_P - @m42a_lib.M42A	48D4
IMVP6_DFB	IMVP6_DFB - @m42a_lib.M42A	58A4 58B6
IMVP6_DROOP	IMVP6_DROOP - @m42a_lib.M42A	48D5 58A4 58B6
IMVP6_FB	IMVP6_FB - @m42a_lib.M42A	58A4 58B7
IMVP6_FB2	IMVP6_FB2 - @m42a_lib.M42A	58A4 58B7
IMVP6_FET_RC1	IMVP6_FET_RC1 - @m42a_lib.M42A	58A8 58C2
IMVP6_FET_RC2	IMVP6_FET_RC2 - @m42a_lib.M42A	58A6 58B2
IMVP6_ISEN1	IMVP6_ISEN1 - @m42a_lib.M42A	58A8 58C6
IMVP6_ISEN2	IMVP6_ISEN2 - @m42a_lib.M42A	58A6 58C6
IMVP6_LGATE1	IMVP6_LGATE1 - @m42a_lib.M42A	58A8 58C6
IMVP6_LGATE2	IMVP6_LGATE2 - @m42a_lib.M42A	58A6 58C6
IMVP6_NTC	IMVP6_NTC - @m42a_lib.M42A	58C7
IMVP6_NTC_R	IMVP6_NTC_R - @m42a_lib.M42A	58C7
IMVP6_OCSET	IMVP6_OCSET - @m42a_lib.M42A	58A4 58B6
IMVP6_PHASE1	IMVP6_PHASE1 - @m42a_lib.M42A	58A8 58C6
IMVP6_PHASE2	IMVP6_PHASE2 - @m42a_lib.M42A	58A6 58C6
IMVP6_RBIAS	IMVP6_RBIAS - @m42a_lib.M42A	5D7 58A4 58B7
IMVP6_RTN	IMVP6_RTN - @m42a_lib.M42A	58A4 58B6
IMVP6_SOFT	IMVP6_SOFT - @m42a_lib.M42A	58A4 58C7
IMVP6_UGATE1	IMVP6_UGATE1 - @m42a_lib.M42A	58A8 58C6
IMVP6_UGATE2	IMVP6_UGATE2 - @m42a_lib.M42A	58A6 58C6
IMVP6_VDIFF	IMVP6_VDIFF - @m42a_lib.M42A	58A4 58B7
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m42a_lib.M42A	58B7
IMVP6_VO	IMVP6_VO - @m42a_lib.M42A	48C5 58A4 58B6
IMVP6_VO_R	IMVP6_VO_R - @m42a_lib.M42A	58B4
IMVP6_VO_R1	IMVP6_VO_R1 - @m42a_lib.M42A	58A8
IMVP6_VO_R2	IMVP6_VO_R2 - @m42a_lib.M42A	58A6
IMVP6_VR_TT	IMVP6_VR_TT - @m42a_lib.M42A	58C7
IMVP6_VSEN	IMVP6_VSEN - @m42a_lib.M42A	58A4 58B5
IMVP6_VSUM	IMVP6_VSUM - @m42a_lib.M42A	58A4 58C6
IMVP6_VSUM_R1	IMVP6_VSUM_R1 - @m42a_lib.M42A	58A8
IMVP6_VSUM_R2	IMVP6_VSUM_R2 - @m42a_lib.M42A	58A6
IMVP6_VW	IMVP6_VW - @m42a_lib.M42A	58A4 58B7
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @m42a_lib.M42A	58C7
IMVP_VR_ON	IMVP_VR_ON - @m42a_lib.M42A	45D8 58C7
INT_PIRQA_L	INT_PIRQA_L - @m42a_lib.M42A	22A7 26C3
INT_PIRQB_L	INT_PIRQB_L - @m42a_lib.M42A	22A7 26C3
INT_PIRQC_L	INT_PIRQC_L - @m42a_lib.M42A	22A7 26C3
INT_PIRQD_L	INT_PIRQD_L - @m42a_lib.M42A	22A7 26C3 38A5
INT_SERIRQ	INT_SERIRQ - @m42a_lib.M42A	5C2 23C8 45C8 47C5 53C6
INVT_CHGND	INVT_CHGND - @m42a_lib.M42A	6D8 67C2
INV_BKLIGHT_PWM_L	INV_BKLIGHT_PWM_L - @m42a_lib.M42A	5B1 67D2
INV_GND	INV_GND - @m42a_lib.M42A	5B1 67D2
INV_PWREN_F_L	INV_PWREN_F_L - @m42a_lib.M42A	67D6
INV_PWREN_L	INV_PWREN_L - @m42a_lib.M42A	67D6
IR_RX_OUT	IR_RX_OUT - @m42a_lib.M42A	35C6 41C6
IR_RX_OUT_F	IR_RX_OUT_F - @m42a_lib.M42A	41C5
ISENSE_CAL_EN	ISENSE_CAL_EN - @m42a_lib.M42A	45B8 48A8
ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @m42a_lib.M42A	48A7
ISENSE_CAL_EN_LS5V	ISENSE_CAL_EN_LS5V - @m42a_lib.M42A	48A6
ITPRESET_L	ITPRESET_L - @m42a_lib.M42A	11B3
ITP_TDO	ITP_TDO - @m42a_lib.M42A	11B3
J2900_SA1	J2900_SA1 - @m42a_lib.M42A	29A4
KBC_MDE	KBC_MDE - @m42a_lib.M42A	45C2
LCDVDD_PWREN_L	LCDVDD_PWREN_L - @m42a_lib.M42A	67B7
LCDVDD_PWREN_L_R	LCDVDD_PWREN_L_R - @m42a_lib.M42A	67B6
LPC_AD<0>	LPC_AD<0> - @m42a_lib.M42A	5D2 21D4 45D8 47C6 53C6
LPC_AD<1>	LPC_AD<1> - @m42a_lib.M42A	5D2 21D4 45D8 47C6 53C6
LPC_AD<2>	LPC_AD<2> - @m42a_lib.M42A	5C2 21D4 45D8 47C5 53C6
LPC_AD<3>	LPC_AD<3> - @m42a_lib.M42A	5C2 21D4 45D8 47C5 53C6
LPC_FRAME_L	LPC_FRAME_L - @m42a_lib.M42A	5C2 21C5 45C8 47C6 53C6
LVDS_A_CLK_N	LVDS_A_CLK_N - @m42a_lib.M42A	13D5 67B2
LVDS_A_CLK_P	LVDS_A_CLK_P - @m42a_lib.M42A	13C5 67B2
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @m42a_lib.M42A	13C5 67B2
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @m42a_lib.M42A	13C5 67B2
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @m42a_lib.M42A	13C5 67B2
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @m42a_lib.M42A	13C5 67B2
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @m42a_lib.M42A	13C5 67B2
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @m42a_lib.M42A	13C5 67B2
LVDS_BKLTCTL	LVDS_BKLTCTL - @m42a_lib.M42A	13D5 67C6
LVDS_BKLTEN	LVDS_BKLTEN - @m42a_lib.M42A	13D5 67D7
LVDS_B_CLK_N	LVDS_B_CLK_N - @m42a_lib.M42A	6D6 13C5
	LVDS_B_CLK_N_SPN - @m42a_lib.M42A	5A7 6D5
LVDS_B_CLK_P	LVDS_B_CLK_P - @m42a_lib.M42A	6D6 13C5
	LVDS_B_CLK_P_SPN - @m42a_lib.M42A	5A7 6D5
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @m42a_lib.M42A	6D6 13C5
	LVDS_B_DATA_N0_SPN - @m42a_lib.M42A	5A7 6D5
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m42a_lib.M42A	6D6 13C5
	LVDS_B_DATA_N1_SPN - @m42a_lib.M42A	5A7 6D5
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m42a_lib.M42A	6D6 13C5
	LVDS_B_DATA_N2_SPN - @m42a_lib.M42A	5A7 6D5
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @m42a_lib.M42A	6D6 13C5
	LVDS_B_DATA_P0_SPN - @m42a_lib.M42A	6D5
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @m42a_lib.M42A	6D6 13C5
	LVDS_B_DATA_P1_SPN - @m42a_lib.M42A	5A7 6D5
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @m42a_lib.M42A	6D6 13C5
	LVDS_B_DATA_P2_SPN - @m42a_lib.M42A	5A7 6D5
LVDS_CLKCTLA	LVDS_CLKCTLA - @m42a_lib.M42A	13D5 67A7
LVDS_CLKCTLB	LVDS_CLKCTLB - @m42a_lib.M42A	13D5 67A7
LVDS_DDC_CLK	LVDS_DDC_CLK - @m42a_lib.M42A	13D5 67B6
LVDS_DDC_DATA	LVDS_DDC_DATA - @m42a_lib.M42A	13D5 67B6
LVDS_IBG	LVDS_IBG - @m42a_lib.M42A	13D5 67A6
LVDS_VDDEN	LVDS_VDDEN - @m42a_lib.M42A	13D5 67B7
MAX9705_L_N	MAX9705_L_N - @m42a_lib.M42A	55B6
MAX9705_R_N	MAX9705_R_N - @m42a_lib.M42A	55C6
MAX9705_SUB_N	MAX9705_SUB_N - @m42a_lib.M42A	55A6
MAX9890_CEXT	MAX9890_CEXT - @m42a_lib.M42A	57B1
MAX9890_INL	MAX9890_INL - @m42a_lib.M42A	57B2
MAX9890_INR	MAX9890_INR - @m42a_lib.M42A	57B2
MEMVTT_EN	MEMVTT_EN - @m42a_lib.M42A	31B5
MEMVTT_VREF	MEMVTT_VREF - @m42a_lib.M42A	31C4
MEM_A_A<0>	MEM_A_A<0> - @m42a_lib.M42A	15C5 28B4
MEM_A_A<13..0>	MEM_A_A<13..0> - @m42a_lib.M42A	30C6
MEM_A_A<1>	MEM_A_A<1> - @m42a_lib.M42A	15C5 28B6
MEM_A_A<2>	MEM_A_A<2> - @m42a_lib.M42A	15C5 28B4
MEM_A_A<3>	MEM_A_A<3> - @m42a_lib.M42A	15B5 28B6
MEM_A_A<4>	MEM_A_A<4> - @m42a_lib.M42A	15B5 28B4
MEM_A_A<5>	MEM_A_A<5> - @m42a_lib.M42A	15B5 28B6
MEM_A_A<6>	MEM_A_A<6> - @m42a_lib.M42A	15B5 28C4
MEM_A_A<7>	MEM_A_A<7> - @m42a_lib.M42A	15B5 28C4
MEM_A_A<8>	MEM_A_A<8> - @m42a_lib.M42A	15B5 28C6
MEM_A_A<9>	MEM_A_A<9> - @m42a_lib.M42A	15B5 28C6
MEM_A_A<10>	MEM_A_A<10> - @m42a_lib.M42A	15B5 28B6
MEM_A_A<11>	MEM_A_A<11> - @m42a_lib.M42A	15B5 28C4
MEM_A_A<12>	MEM_A_A<12> - @m42a_lib.M42A	15B5 28C6
MEM_A_A<13>	MEM_A_A<13> - @m42a_lib.M42A	15B5 28B4
MEM_A_A<14>	MEM_A_A<14> - @m42a_lib.M42A	6A4 28C4
	MEM_A_A14_SPN - @m42a_lib.M42A	6A3
MEM_A_A<15>	MEM_A_A<15> - @m42a_lib.M42A	6A4 28C4
	MEM_A_A15_SPN - @m42a_lib.M42A	6A3
MEM_A_BS<0>	MEM_A_BS<0> - @m42a_lib.M42A	15D5 28B6
MEM_A_BS<2..0>	MEM_A_BS<2..0> - @m42a_lib.M42A	30C6
MEM_A_BS<1>	MEM_A_BS<1> - @m42a_lib.M42A	15D5 28B4
MEM_A_BS<2>	MEM_A_BS<2> - @m42a_lib.M42A	15D5 28C6
MEM_A_CAS_L	MEM_A_CAS_L - @m42a_lib.M42A	15D5 28B6 30B6
MEM_A_DM<0>	MEM_A_DM<0> - @m42a_lib.M42A	15D5 28D4
MEM_A_DM<1>	MEM_A_DM<1> - @m42a_lib.M42A	15D5 28D4
MEM_A_DM<2>	MEM_A_DM<2> - @m42a_lib.M42A	15D5 28C6
MEM_A_DM<3>	MEM_A_DM<3> - @m42a_lib.M42A	15C5 28C4
MEM_A_DM<4>	MEM_A_DM<4> - @m42a_lib.M42A	15C5 28B4
MEM_A_DM<5>	MEM_A_DM<5> - @m42a_lib.M42A	15C5 28B6
MEM_A_DM<6>	MEM_A_DM<6> - @m42a_lib.M42A	15C5 28A6
MEM_A_DM<7>	MEM_A_DM<7> - @m42a_lib.M42A	15C5 28A4
MEM_A_DQ<0>	MEM_A_DQ<0> - @m42a_lib.M42A	15D7 28D4
MEM_A_DQ<1>	MEM_A_DQ<1> - @m42a_lib.M42A	15D7 28D4
MEM_A_DQ<2>	MEM_A_DQ<2> - @m42a_lib.M42A	15D7 28D6
MEM_A_DQ<3>	MEM_A_DQ<3> - @m42a_lib.M42A	15D7 28D6
MEM_A_DQ<4>	MEM_A_DQ<4> - @m42a_lib.M42A	15D7 28D4
MEM_A_DQ<5>	MEM_A_DQ<5> - @m42a_lib.M42A	15D7 28D4
MEM_A_DQ<6>	MEM_A_DQ<6> - @m42a_lib.M42A	15D7 28D6
MEM_A_DQ<7>	MEM_A_DQ<7> - @m42a_lib.M42A	15D7 28D6
MEM_A_DQ<8>	MEM_A_DQ<8> - @m42a_lib.M42A	15C7 28D6
MEM_A_DQ<9>	MEM_A_DQ<9> - @m42a_lib.M42A	15C7 28D6
MEM_A_DQ<10>	MEM_A_DQ<10> - @m42a_lib.M42A	15C7 28D6
MEM_A_DQ<11>	MEM_A_DQ<11> - @m42a_lib.M42A	15C7 28D4
MEM_A_DQ<12>	MEM_A_DQ<12> - @m42a_lib.M42A	15C7 28D4
MEM_A_DQ<13>	MEM_A_DQ<13> - @m42a_lib.M42A	15C7 28D6
MEM_A_DQ<14>	MEM_A_DQ<14> - @m42a_lib.M42A	15C7 28D4
MEM_A_DQ<15>	MEM_A_DQ<15> - @m42a_lib.M42A	15C7 28D4
MEM_A_DQ<16>	MEM_A_DQ<16> - @m42a_lib.M42A	15C7 28C4
MEM_A_DQ<17>	MEM_A_DQ<17> - @m42a_lib.M42A	15C7 28C6
MEM_A_DQ<18>	MEM_A_DQ<18> - @m42a_lib.M42A	15C7 28C4
MEM_A_DQ<19>	MEM_A_DQ<19> - @m42a_lib.M42A	15C7 28C6
MEM_A_DQ<20>	MEM_A_DQ<20> - @m42a_lib.M42A	15C7 28C6
MEM_A_DQ<21>	MEM_A_DQ<21> - @m42a_lib.M42A	15C7 28C4
MEM_A_DQ<22>	MEM_A_DQ<22> - @m42a_lib.M42A	15C7 28C6
MEM_A_DQ<23>	MEM_A_DQ<23> - @m42a_lib.M42A	15C7 28C4
MEM_A_DQ<24>	MEM_A_DQ<24> - @m42a_lib.M42A	15C7 28D6
MEM_A_DQ<25>	MEM_A_DQ<25> - @m42a_lib.M42A	15C7 28C6
MEM_A_DQ<26>	MEM_A_DQ<26> - @m42a_lib.M42A	15C7 28C4
MEM_A_DQ<27>	MEM_A_DQ<27> - @m42a_lib.M42A	15C7 28C6
MEM_A_DQ<28>	MEM_A_DQ<28> - @m42a_lib.M42A	15C7 28C4
MEM_A_DQ<29>	MEM_A_DQ<29> - @m42a_lib.M42A	15C7 28D4
MEM_A_DQ<30>	MEM_A_DQ<30> - @m42a_lib.M42A	15C7 28C4
MEM_A_DQ<31>	MEM_A_DQ<31> - @m42a_lib.M42A	15C7 28C6
MEM_A_DQ<32>	MEM_A_DQ<32> - @m42a_lib.M42A	15C7 28B6
MEM_A_DQ<33>	MEM_A_DQ<33> - @m42a_lib.M42A	15C7 28B4
MEM_A_DQ<34>	MEM_A_DQ<34> - @m42a_lib.M42A	15B7 28B4
MEM_A_DQ<35>	MEM_A_DQ<35> - @m42a_lib.M42A	15B7 28B4
MEM_A_DQ<36>	MEM_A_DQ<36> - @m42a_lib.M42A	15B7 28B4
MEM_A_DQ<37>	MEM_A_DQ<37> - @m42a_lib.M42A	15B7 28B6
MEM_A_DQ<38>	MEM_A_DQ<38> - @m42a_lib.M42A	15B7 28B6
MEM_A_DQ<39>	MEM_A_DQ<39> - @m42a_lib.M42A	15B7 28B6
MEM_A_DQ<40>	MEM_A_DQ<40> - @m42a_lib.M42A	15B7 28B4
MEM_A_DQ<41>	MEM_A_DQ<41> - @m42a_lib.M42A	15B7 28B6
MEM_A_DQ<42>	MEM_A_DQ<42> - @m42a_lib.M42A	15B7 28A4
MEM_A_DQ<43>	MEM_A_DQ<43> - @m42a_lib.M42A	15B7 28A6
MEM_A_DQ<44>	MEM_A_DQ<44> - @m42a_lib.M42A	15B7 28B6
MEM_A_DQ<45>	MEM_A_DQ<45> - @m42a_lib.M42A	15B7 28B4
MEM_A_DQ<46>	MEM_A_DQ<46> - @m42a_lib.M42A	15B7 28A4
MEM_A_DQ<47>	MEM_A_DQ<47> - @m42a_lib.M42A	15B7 28A6
MEM_A_DQ<48>	MEM_A_DQ<48> - @m42a_lib.M42A	15B7 28A6
MEM_A_DQ<49>	MEM_A_DQ<49> - @m42a_lib.M42A	15B7 28A6
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MEM_A_DQ<55>	MEM_A_DQ<55> - @m42a_lib.M42A	15B7 28A6
MEM_A_DQ<56>	MEM_A_DQ<56> - @m42a_lib.M42A	15B7 28A6
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MEM_A_DQ<59>	MEM_A_DQ<59> - @m42a_lib.M42A	15B7 28A4
MEM_A_DQ<60>	MEM_A_DQ<60> - @m42a_lib.M42A	15A7 28A4
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MEM_A_DQ<62>	MEM_A_DQ<62> - @m42a_lib.M42A	15A7 28A4
MEM_A_DQ<63>	MEM_A_DQ<63> - @m42a_lib.M42A	15A7 28A6
MEM_A_DQS_N<0>	MEM_A_DQS_N<0> - @m42a_lib.M42A	15C5 28D6
MEM_A_DQS_N<1>	MEM_A_DQS_N<1> - @m42a_lib.M42A	15C5 28D6
MEM_A_DQS_N<2>	MEM_A_DQS_N<2> - @m42a_lib.M42A	15C5 28C4
MEM_A_DQS_N<3>	MEM_A_DQS_N<3> - @m42a_lib.M42A	15C5 28C6
MEM_A_DQS_N<4>	MEM_A_DQS_N<4> - @m42a_lib.M42A	15C5 28B6
MEM_A_DQS_N<5>	MEM_A_DQS_N<5> - @m42a_lib.M42A	15C5 28B4
MEM_A_DQS_N<6>	MEM_A_DQS_N<6> - @m42a_lib.M42A	15C5 28A4
MEM_A_DQS_N<7>	MEM_A_DQS_N<7> - @m42a_lib.M42A	15C5 28A6
MEM_A_DQS_P<0>	MEM_A_DQS_P<0> - @m42a_lib.M42A	15C5 28D6
MEM_A_DQS_P<1>	MEM_A_DQS_P<1> - @m42a_lib.M42A	15C5 28D6
MEM_A_DQS_P<2>	MEM_A_DQS_P<2> - @m42a_lib.M42A	15C5 28C4
MEM_A_DQS_P<3>	MEM_A_DQS_P<3> - @m42a_lib.M42A	15C5 28C6
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MEM_A_DQS_P<5>	MEM_A_DQS_P<5> - @m42a_lib.M42A	15C5 28B4
MEM_A_DQS_P<6>	MEM_A_DQS_P<6> - @m42a_lib.M42A	15C5 28A4
MEM_A_DQS_P<7>	MEM_A_DQS_P<7> - @m42a_lib.M42A	15C5 28A6
MEM_A_RAS_L	MEM_A_RAS_L - @m42a_lib.M42A	15B5 28B4 30B6
MEM_A_WE_L	MEM_A_WE_L - @m42a_lib.M42A	15B5 28B6 30B6
MEM_B_A<0>	MEM_B_A<0> - @m42a_lib.M42A	15C2 29B4 30B5
MEM_B_A<1>	MEM_B_A<1> - @m42a_lib.M42A	15C2 29B6 30B5
MEM_B_A<2>	MEM_B_A<2> - @m42a_lib.M42A	15C2 29B4 30B5
MEM_B_A<3>	MEM_B_A<3> - @m42a_lib.M42A	15B2 29B6 30B5
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MEM_B_A<5>	MEM_B_A<5> - @m42a_lib.M42A	15B2 29B6 30B5
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MEM_B_A<12>	MEM_B_A<12> - @m42a_lib.M42A	15B2 29C6 30A5
MEM_B_A<13>	MEM_B_A<13> - @m42a_lib.M42A	15B2 29B4 30A5
MEM_B_A<14>	MEM_B_A<14> - @m42a_lib.M42A	6A4 29C4
	MEM_B_A14_SPN - @m42a_lib.M42A	6A3
MEM_B_A<15>	MEM_B_A<15> - @m42a_lib.M42A	6A4 29C4
	MEM_B_A15_SPN - @m42a_lib.M42A	6A3
MEM_B_BS<0>	MEM_B_BS<0> - @m42a_lib.M42A	15D2 29B6
MEM_B_BS<2..0>	MEM_B_BS<2..0> - @m42a_lib.M42A	30A6
MEM_B_BS<1>	MEM_B_BS<1> - @m42a_lib.M42A	15D2 29B4
MEM_B_BS<2>	MEM_B_BS<2> - @m42a_lib.M42A	15D2 29C6
MEM_B_CAS_L	MEM_B_CAS_L - @m42a_lib.M42A	15D2 29B6 30A6
MEM_B_DM<0>	MEM_B_DM<0> - @m42a_lib.M42A	15D2 29D4
MEM_B_DM<1>	MEM_B_DM<1> - @m42a_lib.M42A	15D2 29D4
MEM_B_DM<2>	MEM_B_DM<2> - @m42a_lib.M42A	15D2 29C4
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MEM_B_DM<4>	MEM_B_DM<4> - @m42a_lib.M42A	15C2 29A4
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MEM_B_DM<7>	MEM_B_DM<7> - @m42a_lib.M42A	15C2 29B4
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MEM_B_DQ<60>	MEM_B_DQ<60> - @m42a_lib.M42A	15A4 29B6
MEM_B_DQ<61>	MEM_B_DQ<61> - @m42a_lib.M42A	15A4 29B4
MEM_B_DQ<62>	MEM_B_DQ<62> - @m42a_lib.M42A	15A4 29B6
MEM_B_DQ<63>	MEM_B_DQ<63> - @m42a_lib.M42A	15A4 29B4
MEM_B_DQS_N<0>	MEM_B_DQS_N<0> - @m42a_lib.M42A	15C2 29D6
MEM_B_DQS_N<1>	MEM_B_DQS_N<1> - @m42a_lib.M42A	15C2 29D6
MEM_B_DQS_N<2>	MEM_B_DQS_N<2> - @m42a_lib.M42A	15C2 29C6
MEM_B_DQS_N<3>	MEM_B_DQS_N<3> - @m42a_lib.M42A	15C2 29C4
MEM_B_DQS_N<4>	MEM_B_DQS_N<4> - @m42a_lib.M42A	15C2 29A6
MEM_B_DQS_N<5>	MEM_B_DQS_N<5> - @m42a_lib.M42A	15C2 29A4
MEM_B_DQS_N<6>	MEM_B_DQS_N<6> - @m42a_lib.M42A	15C2 29B4
MEM_B_DQS_N<7>	MEM_B_DQS_N<7> - @m42a_lib.M42A	15C2 29B6
MEM_B_DQS_P<0>	MEM_B_DQS_P<0> - @m42a_lib.M42A	15C2 29D6
MEM_B_DQS_P<1>	MEM_B_DQS_P<1> - @m42a_lib.M42A	15C2 29D6
MEM_B_DQS_P<2>	MEM_B_DQS_P<2> - @m42a_lib.M42A	15C2 29C6
MEM_B_DQS_P<3>	MEM_B_DQS_P<3> - @m42a_lib.M42A	15C2 29C4
MEM_B_DQS_P<4>	MEM_B_DQS_P<4> - @m42a_lib.M42A	15C2 29A6
MEM_B_DQS_P<5>	MEM_B_DQS_P<5> - @m42a_lib.M42A	15C2 29A4
MEM_B_DQS_P<6>	MEM_B_DQS_P<6> - @m42a_lib.M42A	15C2 29A4
MEM_B_DQS_P<7>	MEM_B_DQS_P<7> - @m42a_lib.M42A	15C2 29B6
MEM_B_RAS_L	MEM_B_RAS_L - @m42a_lib.M42A	15B2 29B4 30A6
MEM_B_WE_L	MEM_B_WE_L - @m42a_lib.M42A	15B2 29B6 30A6
MEM_CKE<0>	MEM_CKE<0> - @m42a_lib.M42A	14C4 28C6
MEM_CKE<3..0>	MEM_CKE<3..0> - @m42a_lib.M42A	30D6
MEM_CKE<1>	MEM_CKE<1> - @m42a_lib.M42A	14C4 28C4
MEM_CKE<2>	MEM_CKE<2> - @m42a_lib.M42A	14C4 29C6
MEM_CKE<3>	MEM_CKE<3> - @m42a_lib.M42A	14C4 29C4
MEM_CLK_N<0>	MEM_CLK_N<0> - @m42a_lib.M42A	14D4 28D4
MEM_CLK_N<1>	MEM_CLK_N<1> - @m42a_lib.M42A	14D4 28A4
MEM_CLK_N<2>	MEM_CLK_N<2> - @m42a_lib.M42A	14D4 29A4
MEM_CLK_N<3>	MEM_CLK_N<3> - @m42a_lib.M42A	14D4 29D4
MEM_CLK_P<0>	MEM_CLK_P<0> - @m42a_lib.M42A	14D4 28D4
MEM_CLK_P<1>	MEM_CLK_P<1> - @m42a_lib.M42A	14D4 28A4
MEM_CLK_P<2>	MEM_CLK_P<2> - @m42a_lib.M42A	14D4 29A4
MEM_CLK_P<3>	MEM_CLK_P<3> - @m42a_lib.M42A	14D4 29D4
MEM_CS_L<0>	MEM_CS_L<0> - @m42a_lib.M42A	14C4 28B4
MEM_CS_L<3..0>	MEM_CS_L<3..0> - @m42a_lib.M42A	30D6
MEM_CS_L<1>	MEM_CS_L<1> - @m42a_lib.M42A	14C4 28B6
MEM_CS_L<2>	MEM_CS_L<2> - @m42a_lib.M42A	14C4 29B4
MEM_CS_L<3>	MEM_CS_L<3> - @m42a_lib.M42A	14C4 29B6
MEM_ISENSE	MEM_ISENSE - @m42a_lib.M42A	61C2
MEM_ISENSE_R1_N	MEM_ISENSE_R1_N - @m42a_lib.M42A	61C3
MEM_ISENSE_R1_P	MEM_ISENSE_R1_P - @m42a_lib.M42A	61C3
MEM_ISENSE_R2	MEM_ISENSE_R2 - @m42a_lib.M42A	61C2
MEM_ISENSE_VCC	MEM_ISENSE_VCC - @m42a_lib.M42A	61C2
MEM_ODT<0>	MEM_ODT<0> - @m42a_lib.M42A	14C4 28B4
MEM_ODT<3..0>	MEM_ODT<3..0> - @m42a_lib.M42A	30D6
MEM_ODT<1>	MEM_ODT<1> - @m42a_lib.M42A	14C4 28B6
MEM_ODT<2>	MEM_ODT<2> - @m42a_lib.M42A	14C4 29B4
MEM_ODT<3>	MEM_ODT<3> - @m42a_lib.M42A	14C4 29B6
MEM_RCOMP	MEM_RCOMP - @m42a_lib.M42A	14C4
MEM_RCOMP_L	MEM_RCOMP_L - @m42a_lib.M42A	14C4
MEM_VREF_A	MEM_VREF_A - @m42a_lib.M42A	28D1 28D7
MEM_VREF_B	MEM_VREF_B - @m42a_lib.M42A	29D1 29D7
MEM_VREF_NB_0	MEM_VREF_NB_0 - @m42a_lib.M42A	14C2 19C7
MEM_VREF_NB_1	MEM_VREF_NB_1 - @m42a_lib.M42A	14C2 19C6
MIC_HI	MIC_HI - @m42a_lib.M42A	56B3 57A8
MIC_HI_CONN	MIC_HI_CONN - @m42a_lib.M42A	56B1 56D3
MIC_HI_F	MIC_HI_F - @m42a_lib.M42A	56B2
MIC_IN	MIC_IN - @m42a_lib.M42A	57A7
MIC_LO	MIC_LO - @m42a_lib.M42A	56B3 57A8
MIC_LO_CONN	MIC_LO_CONN - @m42a_lib.M42A	56B1 56D3
MIC_LO_F	MIC_LO_F - @m42a_lib.M42A	56B2
MIC_SHIELD	MIC_SHIELD - @m42a_lib.M42A	56B3 57A8
MIC_SHIELD_F	MIC_SHIELD_F - @m42a_lib.M42A	56B2
MIC_SHLD_CONN	MIC_SHLD_CONN - @m42a_lib.M42A	56B1 56D3
MM1573DN_NR	MM1573DN_NR - @m42a_lib.M42A	19C3
NB_BSEL<0>	NB_BSEL<0> - @m42a_lib.M42A	14C6 33C7
NB_BSEL<1>	NB_BSEL<1> - @m42a_lib.M42A	14C6 33B7
NB_BSEL<2>	NB_BSEL<2> - @m42a_lib.M42A	14C6 33B7
NB_CFG<3>	NB_CFG<3> - @m42a_lib.M42A	6D4 14C6
	TP_NB_CFG3 - @m42a_lib.M42A	6D3
NB_CFG<4>	NB_CFG<4> - @m42a_lib.M42A	6D4 14C6
	TP_NB_CFG4 - @m42a_lib.M42A	6D3
NB_CFG<5>	NB_CFG<5> - @m42a_lib.M42A	14C6 20C7
NB_CFG<6>	NB_CFG<6> - @m42a_lib.M42A	6D4 14C6
	TP_NB_CFG6 - @m42a_lib.M42A	6D3
NB_CFG<7>	NB_CFG<7> - @m42a_lib.M42A	14C6 20C7
NB_CFG<8>	NB_CFG<8> - @m42a_lib.M42A	6D4 14C6
	TP_NB_CFG8 - @m42a_lib.M42A	6D3
NB_CFG<9>	NB_CFG<9> - @m42a_lib.M42A	14C6 20B7

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NB_CFG<10>           NB_CFG<10> - @m42a_lib.M42A         6D4 14C6
                     TP_NB_CFG10 - @m42a_lib.M42A        6D3
NB_CFG<11>           NB_CFG<11> - @m42a_lib.M42A         6D4 14C6
                     TP_NB_CFG11 - @m42a_lib.M42A        6D3
NB_CFG<12>           NB_CFG<12> - @m42a_lib.M42A         6D4 14C6
                     TP_NB_CFG12 - @m42a_lib.M42A        6D3
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                     TP_NB_CFG13 - @m42a_lib.M42A        6D3
NB_CFG<14>           NB_CFG<14> - @m42a_lib.M42A         6D4 14C6
                     TP_NB_CFG14 - @m42a_lib.M42A        6D3
NB_CFG<15>           NB_CFG<15> - @m42a_lib.M42A         6D4 14C6
                     TP_NB_CFG15 - @m42a_lib.M42A        6D3
NB_CFG<16>           NB_CFG<16> - @m42a_lib.M42A         14C6 20C5
NB_CFG<17>           NB_CFG<17> - @m42a_lib.M42A         6D4 14C6
                     TP_NB_CFG17 - @m42a_lib.M42A        6D3
NB_CFG<18>           NB_CFG<18> - @m42a_lib.M42A         14C6 20B5
NB_CFG<19>           NB_CFG<19> - @m42a_lib.M42A         14C6 20B5
NB_CFG<20>           NB_CFG<20> - @m42a_lib.M42A         14B6 20A5
NB_CLK100M_GCLKIN_N  NB_CLK100M_GCLKIN_N -               14C4 33B2 33C4
                     @m42a_lib.M42A
NB_CLK100M_GCLKIN_P  NB_CLK100M_GCLKIN_P -               14C4 33C2 33C4
                     @m42a_lib.M42A
NB_CLK_DREFCLKIN_N   NB_CLK_DREFCLKIN_N - @m42a_lib.M42A 14C4 33B3 33C2
NB_CLK_DREFCLKIN_P   NB_CLK_DREFCLKIN_P - @m42a_lib.M42A 14C4 33B3 33C2
NB_CLK_DREFSSCLKIN_N NB_CLK_DREFSSCLKIN_N -              14C4 33A4 33C2
                     @m42a_lib.M42A
NB_CLK_DREFSSCLKIN_P NB_CLK_DREFSSCLKIN_P -              14B4 33A3 33C2
                     @m42a_lib.M42A
NB_FSB_VREF          NB_FSB_VREF - @m42a_lib.M42A        12C4
NB_FSB_XRCOMP        NB_FSB_XRCOMP - @m42a_lib.M42A      12A6
NB_FSB_XSCOMP        NB_FSB_XSCOMP - @m42a_lib.M42A      12A6
NB_FSB_XSWING        NB_FSB_XSWING - @m42a_lib.M42A      12A6
NB_FSB_YRCOMP        NB_FSB_YRCOMP - @m42a_lib.M42A      12A6
NB_FSB_YSCOMP        NB_FSB_YSCOMP - @m42a_lib.M42A      12A6
NB_FSB_YSWING        NB_FSB_YSWING - @m42a_lib.M42A      12A6
NB_ISENSE            NB_ISENSE - @m42a_lib.M42A          62A6
NB_ISENSE_R1_N       NB_ISENSE_R1_N - @m42a_lib.M42A     62A7
NB_ISENSE_R1_P       NB_ISENSE_R1_P - @m42a_lib.M42A     62A7
NB_ISENSE_R2         NB_ISENSE_R2 - @m42a_lib.M42A       62A6
NB_ISENSE_VCC        NB_ISENSE_VCC - @m42a_lib.M42A      62A6
NB_RIGHT_DOWN_SCREW  NB_RIGHT_DOWN_SCREW -               6A8
                     @m42a_lib.M42A
NB_RST_IN_L_R        NB_RST_IN_L_R - @m42a_lib.M42A      14B6
NB_SB_SYNC_L         NB_SB_SYNC_L - @m42a_lib.M42A       14B6 22A6
NB_TV_DCONSEL0       NB_TV_DCONSEL0 - @m42a_lib.M42A     14D6
NB_TV_DCONSEL1       NB_TV_DCONSEL1 - @m42a_lib.M42A     14C6
NB_VCCSM_LF1         NB_VCCSM_LF1 - @m42a_lib.M42A       16B4
NB_VCCSM_LF2         NB_VCCSM_LF2 - @m42a_lib.M42A       16B4
NB_VCCSM_LF4         NB_VCCSM_LF4 - @m42a_lib.M42A       16B8
NB_VCCSM_LF5         NB_VCCSM_LF5 - @m42a_lib.M42A       16B8
NB_VTTLF_CAP1        NB_VTTLF_CAP1 - @m42a_lib.M42A      17A4
NB_VTTLF_CAP2        NB_VTTLF_CAP2 - @m42a_lib.M42A      17A4
NB_VTTLF_CAP3        NB_VTTLF_CAP3 - @m42a_lib.M42A      17B4
ODD_PWR_EN_SLOW_STAR ODD_PWR_EN_SLOW_START -             34C7
T                    @m42a_lib.M42A
ODD_PWR_EN_SLOW_STAR ODD_PWR_EN_SLOW_START_L -           34C6
T_L                  @m42a_lib.M42A
ODD_PWR_EN_SLOW_STAR ODD_PWR_EN_SLOW_START_L_R -         34C5
T_L_R                @m42a_lib.M42A
ONEWIRE_DCIN_DIV     ONEWIRE_DCIN_DIV - @m42a_lib.M42A   65C5
ONEWIRE_EN           ONEWIRE_EN - @m42a_lib.M42A         65C7
ONEWIRE_ESD          ONEWIRE_ESD - @m42a_lib.M42A        65C5
ONEWIRE_OV           ONEWIRE_OV - @m42a_lib.M42A         65C6
ONEWIRE_PU_EN        ONEWIRE_PU_EN - @m42a_lib.M42A      65B7
ONEWIRE_PU_EN_L      ONEWIRE_PU_EN_L - @m42a_lib.M42A    65C8
ONEWIRE_PWR_EN_L     ONEWIRE_PWR_EN_L - @m42a_lib.M42A   65C7
ONEWIRE_PWR_EN_L_DIV ONEWIRE_PWR_EN_L_DIV -              65C6
                     @m42a_lib.M42A
P0V52_SMC_LSREF      P0V52_SMC_LSREF - @m42a_lib.M42A    46D3
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P3V3S0_EN_RC         P3V3S0_EN_RC - @m42a_lib.M42A       63B5
P3V3S3_EN_L_RC       P3V3S3_EN_L_RC - @m42a_lib.M42A     63C5
P3V42G3H5_BOOST      P3V42G3H5_BOOST - @m42a_lib.M42A    63D2
P3V42G3H_FB          P3V42G3H_FB - @m42a_lib.M42A        5D7 63D2
P5VS0_EN_RC          P5VS0_EN_RC - @m42a_lib.M42A        63C5
P5VS3_EN_L_RC        P5VS3_EN_L_RC - @m42a_lib.M42A      63D5
PATA_PWR_EN_L        PATA_PWR_EN_L - @m42a_lib.M42A      23B3 23C3
PBUS_S0_SMC_VSENSE   PBUS_S0_SMC_VSENSE - @m42a_lib.M42A 48C6
PBUS_SMC_VSENSE_EN   PBUS_SMC_VSENSE_EN - @m42a_lib.M42A 48C8
PBUS_SMC_VSENSE_EN_L PBUS_SMC_VSENSE_EN_L -              48C7
                     @m42a_lib.M42A
PCIE_A_D2R_C_N       PCIE_A_D2R_C_N - @m42a_lib.M42A     36D6
PCIE_A_D2R_C_P       PCIE_A_D2R_C_P - @m42a_lib.M42A     36D6
PCIE_A_D2R_N         PCIE_A_D2R_N - @m42a_lib.M42A       22D4 36D5
PCIE_A_D2R_P         PCIE_A_D2R_P - @m42a_lib.M42A       22D4 36D5
PCIE_A_R2D_C_N       PCIE_A_R2D_C_N - @m42a_lib.M42A     22D4 36C5
PCIE_A_R2D_C_P       PCIE_A_R2D_C_P - @m42a_lib.M42A     22D4 36C5
PCIE_A_R2D_N         PCIE_A_R2D_N - @m42a_lib.M42A       36C6
PCIE_A_R2D_P         PCIE_A_R2D_P - @m42a_lib.M42A       36C6
PCIE_B_D2R_N         PCIE_B_D2R_N - @m42a_lib.M42A       22D4 43C7
PCIE_B_D2R_P         PCIE_B_D2R_P - @m42a_lib.M42A       22D4 43C7
PCIE_B_R2D_C_N       PCIE_B_R2D_C_N - @m42a_lib.M42A     22D4 43B7
PCIE_B_R2D_C_P       PCIE_B_R2D_C_P - @m42a_lib.M42A     22D4 43B7
PCIE_B_R2D_N         PCIE_B_R2D_N - @m42a_lib.M42A       43B6
PCIE_B_R2D_P         PCIE_B_R2D_P - @m42a_lib.M42A       43B6
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                     PCIE_C_D2R_N_SPN - @m42a_lib.M42A   6C3
PCIE_C_D2R_P         PCIE_C_D2R_P - @m42a_lib.M42A       6C4 22D4
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PCIE_C_R2D_C_P       PCIE_C_R2D_C_P - @m42a_lib.M42A     6C4 22D4
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                     PCIE_E_R2D_C_P_SPN - @m42a_lib.M42A 6C3
PCIE_F_D2R_N         PCIE_F_D2R_N - @m42a_lib.M42A       6C4 22C4
                     PCIE_F_D2R_N_SPN - @m42a_lib.M42A   6C3
PCIE_F_D2R_P         PCIE_F_D2R_P - @m42a_lib.M42A       6C4 22C4
                     PCIE_F_D2R_P_SPN - @m42a_lib.M42A   6C3
PCIE_F_R2D_C_N       PCIE_F_R2D_C_N - @m42a_lib.M42A     6C4 22C4
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                     PCIE_F_R2D_C_P_SPN - @m42a_lib.M42A 6B3
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PCI_CLK_SB           PCI_CLK_SB - @m42a_lib.M42A         22A6 33D6
PCI_CLK_SMC          PCI_CLK_SMC - @m42a_lib.M42A        33D6 45C8
PCI_CLK_TPM          PCI_CLK_TPM - @m42a_lib.M42A        33D6 53C6
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PCI_C_BE_L<3>        PCI_C_BE_L<3> - @m42a_lib.M42A      22B6 38B5
PCI_DEVSEL_L         PCI_DEVSEL_L - @m42a_lib.M42A       22A6 26D3 38A5
PCI_FRAME_L          PCI_FRAME_L - @m42a_lib.M42A        22A7 26D3 38A5
PCI_GNT3_L           PCI_GNT3_L - @m42a_lib.M42A         22B6 38A5
PCI_IRDY_L           PCI_IRDY_L - @m42a_lib.M42A         22A6 26D3 38A5
PCI_LOCK_L           PCI_LOCK_L - @m42a_lib.M42A         22A6 26D3
PCI_PAR              PCI_PAR - @m42a_lib.M42A            22A6 38B5
PCI_PERR_L           PCI_PERR_L - @m42a_lib.M42A         22A6 26D3 38A5
PCI_PME_FW_L         PCI_PME_FW_L - @m42a_lib.M42A       22B5 38A5
PCI_REQ0_L           PCI_REQ0_L - @m42a_lib.M42A         22B6 26C3
PCI_REQ1_L           PCI_REQ1_L - @m42a_lib.M42A         22B6 26C3
PCI_REQ2_L           PCI_REQ2_L - @m42a_lib.M42A         22B6 26C3
PCI_REQ3_L           PCI_REQ3_L - @m42a_lib.M42A         22B6 26C3 38A5
PCI_RST_L            PCI_RST_L - @m42a_lib.M42A          22A6 38A6
PCI_SERR_L           PCI_SERR_L - @m42a_lib.M42A         22A6 26D3 38A5
PCI_STOP_L           PCI_STOP_L - @m42a_lib.M42A         22A6 26D3 38A5
PCI_TRDY_L           PCI_TRDY_L - @m42a_lib.M42A         22A6 26D3 38A5
PEG_COMP             PEG_COMP - @m42a_lib.M42A           13D3
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PEG_D2R_N<3>         PEG_D2R_N<3> - @m42a_lib.M42A       6C6 13D3
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                     PEG_R2D_C_N4_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_N<5>       PEG_R2D_C_N<5> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_N5_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_N<6>       PEG_R2D_C_N<6> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_N6_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_N<7>       PEG_R2D_C_N<7> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_N7_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_N<8>       PEG_R2D_C_N<8> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_N8_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_N<9>       PEG_R2D_C_N<9> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_N9_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_N<10>      PEG_R2D_C_N<10> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_N10_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_N<11>      PEG_R2D_C_N<11> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_N11_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_N<12>      PEG_R2D_C_N<12> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_N12_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_N<13>      PEG_R2D_C_N<13> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_N13_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_N<14>      PEG_R2D_C_N<14> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_N14_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_N<15>      PEG_R2D_C_N<15> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_N15_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_P<0>       PEG_R2D_C_P<0> - @m42a_lib.M42A     13B3 68C6
PEG_R2D_C_P<1>       PEG_R2D_C_P<1> - @m42a_lib.M42A     13B3 68C6
PEG_R2D_C_P<2>       PEG_R2D_C_P<2> - @m42a_lib.M42A     13B3 68B6
PEG_R2D_C_P<3>       PEG_R2D_C_P<3> - @m42a_lib.M42A     13B3 68B6
PEG_R2D_C_P<4>       PEG_R2D_C_P<4> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_P4_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_P<5>       PEG_R2D_C_P<5> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_P5_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_P<6>       PEG_R2D_C_P<6> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_P6_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_P<7>       PEG_R2D_C_P<7> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_P7_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_P<8>       PEG_R2D_C_P<8> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_P8_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_P<9>       PEG_R2D_C_P<9> - @m42a_lib.M42A     6B6 13B3
                     PEG_R2D_C_P9_SPN - @m42a_lib.M42A   6B5
PEG_R2D_C_P<10>      PEG_R2D_C_P<10> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_P10_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_P<11>      PEG_R2D_C_P<11> - @m42a_lib.M42A    6B6 13B3
                     PEG_R2D_C_P11_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_P<12>      PEG_R2D_C_P<12> - @m42a_lib.M42A    6B6 13A3
                     PEG_R2D_C_P12_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_P<13>      PEG_R2D_C_P<13> - @m42a_lib.M42A    6B6 13A3
                     PEG_R2D_C_P13_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_P<14>      PEG_R2D_C_P<14> - @m42a_lib.M42A    6B6 13A3
                     PEG_R2D_C_P14_SPN - @m42a_lib.M42A  6B5
PEG_R2D_C_P<15>      PEG_R2D_C_P<15> - @m42a_lib.M42A    6B6 13A3
                     PEG_R2D_C_P15_SPN - @m42a_lib.M42A  6B5
PLT_RST_BUF_L        PLT_RST_BUF_L - @m42a_lib.M42A      26B3
PLT_RST_GATED_L      PLT_RST_GATED_L - @m42a_lib.M42A    26A3
PLT_RST_L            PLT_RST_L - @m42a_lib.M42A          22A6 26C3
                     NB_RST_IN_L - @m42a_lib.M42A        14B7 26C1
PM_BATLOW_L          PM_BATLOW_L - @m42a_lib.M42A        23C1 45B8
PM_BMBUSY_L          PM_BMBUSY_L - @m42a_lib.M42A        14B6 23C5
PM_CLKRUN_L          PM_CLKRUN_L - @m42a_lib.M42A        5C2 23C8 38A5 45D5 47C6
                                                         53C6
PM_DPRSLPVR          PM_DPRSLPVR - @m42a_lib.M42A        14B7 23C3 58D8
PM_DPRSLPVR_R        PM_DPRSLPVR_R - @m42a_lib.M42A      14B6
PM_EXTTS_L<0>        PM_EXTTS_L<0> - @m42a_lib.M42A      6B2 14B7 45B8
                     DIMM_OVERTEMP_L - @m42a_lib.M42A    6B1 28C4 29C4
PM_LAN_ENABLE        PM_LAN_ENABLE - @m42a_lib.M42A      23C3 45D8
PM_PWRBTN_L          PM_PWRBTN_L - @m42a_lib.M42A        23C3 45D8
PM_RI_L              PM_RI_L - @m42a_lib.M42A            23D5
PM_RSMRST_L          PM_RSMRST_L - @m42a_lib.M42A        23C1 45D8
PM_SB_PWROK          PM_SB_PWROK - @m42a_lib.M42A        23C3 26A6
PM_SLP_S3            PM_SLP_S3 - @m42a_lib.M42A          48C8 63B7
PM_SLP_S3BATT        PM_SLP_S3BATT - @m42a_lib.M42A      60C7
PM_SLP_S3_L          PM_SLP_S3_L - @m42a_lib.M42A        23C3 45C5 63A7 63A7 63B8
PM_SLP_S3_LS12V6     PM_SLP_S3_LS12V6 - @m42a_lib.M42A   63B7
PM_SLP_S4_L          PM_SLP_S4_L - @m42a_lib.M42A        23C3 45C5 60C8 61B8 63D6
PM_SLP_S5_L          PM_SLP_S5_L - @m42a_lib.M42A        23C3 45C5 46D3
PM_STPCPU_L          PM_STPCPU_L - @m42a_lib.M42A        23C8 32C4
PM_STPPCI_L          PM_STPPCI_L - @m42a_lib.M42A        23C8 32C4
PM_SUS_STAT_L        PM_SUS_STAT_L - @m42a_lib.M42A      5C2 23C5 45D5 46D3 47C5
                                                         53C6
PM_SYSRST_L          PM_SYSRST_L - @m42a_lib.M42A        23C5 26C5 45C8
                     XDP_DBRESET_L_R - @m42a_lib.M42A    26C6
PM_THRMTRIP_L        PM_THRMTRIP_L - @m42a_lib.M42A      7C6 14B6 21C2 46B3
PM_THRM_L            PM_THRM_L - @m42a_lib.M42A          23C8 45B8
PP0V9_S0             PP0V9_S0 - @m42a_lib.M42A           5A2 64D7
                     =PP0V9_S0_MEM_TERM - @m42a_lib.M42A 30D4 64D6
                     =PP0V9_S0_MEM_REG - @m42a_lib.M42A  31B3 63B2 64D8
                     =PP0V9_S0_MEM_TERM - @m42a_lib.M42A 30D4 64D6
                     =PP0V9_S0_MEM_REG - @m42a_lib.M42A  31B3 63B2 64D8
PP1V2_S0             PP1V2_S0 - @m42a_lib.M42A           63B4
PP1V2_S3             PP1V2_S3 - @m42a_lib.M42A           5A2 64C4
                     =PP1V2_S3_REG - @m42a_lib.M42A      60B2 63B5 64C6
                     =PP1V2_S3_ENET - @m42a_lib.M42A     36A8 36D7 64C3
                     =PP1V2_S3_REG - @m42a_lib.M42A      60B2 63B5 64C6
                     =PP1V2_S3_ENET - @m42a_lib.M42A     36A8 36D7 64C3
PP1V5_S0_DPLL        PP1V5_S0_DPLL - @m42a_lib.M42A      19D5
PP1V5_S0_NB_3GPLL_F  PP1V5_S0_NB_3GPLL_F -               19A4
                     @m42a_lib.M42A
PP1V5_S0_NB_QTVDAC   PP1V5_S0_NB_QTVDAC - @m42a_lib.M42A 19A7
PP1V5_S0_NB_VCC3G    PP1V5_S0_NB_VCC3G - @m42a_lib.M42A  17D6 19B2
PP1V5_S0_NB_VCCA_3GP PP1V5_S0_NB_VCCA_3GPLL -            17D6 19A2
LL                   @m42a_lib.M42A
PP1V5_S0_NB_VCCA_DPL PP1V5_S0_NB_VCCA_DPLLA -            17C6 19D4
LA                   @m42a_lib.M42A
PP1V5_S0_NB_VCCA_DPL PP1V5_S0_NB_VCCA_DPLLB -            17C6 19D4
LB                   @m42a_lib.M42A
PP1V5_S0_NB_VCCA_HPL PP1V5_S0_NB_VCCA_HPLL -             17C6 19C4
L                    @m42a_lib.M42A
PP1V5_S0_NB_VCCA_MPL PP1V5_S0_NB_VCCA_MPLL -             17C6 19C4
L                    @m42a_lib.M42A
PP1V5_S0_NB_VCCD_QTV PP1V5_S0_NB_VCCD_QTVDAC -           17B6 19A5
DAC                  @m42a_lib.M42A
PP1V5_S0_NB_VCCD_TVD PP1V5_S0_NB_VCCD_TVDAC -            17C6 19A5
AC                   @m42a_lib.M42A
PP1V5_S0_REG_P       PP1V5_S0_REG_P - @m42a_lib.M42A     62B8
PP1V5_S0_SB_VCC1_5_B PP1V5_S0_SB_VCC1_5_B -              22C1 24D5 25B6
                     @m42a_lib.M42A
PP1V5_S0_SB_VCCDMIPL PP1V5_S0_SB_VCCDMIPLL -             24B5 25A5
L                    @m42a_lib.M42A
PP1V5_S0_SB_VCCDMIPL PP1V5_S0_SB_VCCDMIPLL_F -           25A7
L_F                  @m42a_lib.M42A
```

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PP1V8_S0             PP1V8_S0 - @m42a_lib.M42A           5B2 64C7
                     =PP1V8_S0_TMDS - @m42a_lib.M42A     64B6 68D6 68D6
                     =PP1V8_S0_FET - @m42a_lib.M42A      63B3 64B8
                     =PP1V8_S0_TMDS - @m42a_lib.M42A     64B6 68D6 68D6
                     =PP1V8_S0_FET - @m42a_lib.M42A      63B3 64B8
PP1V8_S0_ANALOG_SDVO PP1V8_S0_ANALOG_SDVO_F -            68C4 68D3
_F                   @m42a_lib.M42A
PP1V8_S0_TMDS_F      PP1V8_S0_TMDS_F - @m42a_lib.M42A    68B4 68D3
PP1V8_S3             PP1V8_S3 - @m42a_lib.M42A           5A2 64C4
                     =PP1V8_S3_1V2S3 - @m42a_lib.M42A    60B5 64C3
                     =PP1V8_S3_MEM_NB_SENSE -            61C4 64C3
                     @m42a_lib.M42A
                     =PP1V8_S3_MEMVTT - @m42a_lib.M42A   31C6 64C3
                     =PP1V8_S3_P1V8S0 - @m42a_lib.M42A   63A5 64C3
                     =PP1V8_S3_REG - @m42a_lib.M42A      61B1 64C6
                     =PP1V8_S3_MEM - @m42a_lib.M42A      19C7 19C8 28B2 28D4 28D6
                                                         29B2 29D4 29D6 64C3
                     =PP1V8_S3_REG - @m42a_lib.M42A      61B1 64C6
                     =PP1V8_S3_P1V8S0 - @m42a_lib.M42A   63A5 64C3
                     =PP1V8_S3_MEM_NB_SENSE -            61C4 64C3
                     @m42a_lib.M42A
                     =PP1V8_S3_MEMVTT - @m42a_lib.M42A   31C6 64C3
                     =PP1V8_S3_MEM - @m42a_lib.M42A      19C7 19C8 28B2 28D4 28D6
                                                         29B2 29D4 29D6 64C3
                     =PP1V8_S3_1V2S3 - @m42a_lib.M42A    60B5 64C3
PP1V8_S3_MEMVTT_VDDQ PP1V8_S3_MEMVTT_VDDQ -              31C5
                     @m42a_lib.M42A
PP1V8_S3_R           PP1V8_S3_R - @m42a_lib.M42A         61B2
PP2V5_S0_NB_CRTDAC_F PP2V5_S0_NB_CRTDAC_F -              19D3
                     @m42a_lib.M42A
PP2V5_S0_NB_CRTDAC_F PP2V5_S0_NB_CRTDAC_FOLLOW -         19D3
OLLOW                @m42a_lib.M42A
PP2V5_S0_NB_VCCA_CRT PP2V5_S0_NB_VCCA_CRTDAC -           17D6 19D1
DAC                  @m42a_lib.M42A
PP2V5_S3             PP2V5_S3 - @m42a_lib.M42A           5A2 64C4
                     =PP2V5_S3_REG - @m42a_lib.M42A      60C2 64C6
                     =PP2V5_S3_ENET - @m42a_lib.M42A     36D3 64C3
                     =PP2V5_S3_REG - @m42a_lib.M42A      60C2 64C6
                     =PP2V5_S3_ENET - @m42a_lib.M42A     36D3 64C3
PP2V5_S3_ENET_AVDD   PP2V5_S3_ENET_AVDD - @m42a_lib.M42A 36D5 37D8
PP2V5_S3_ENET_AVDD_F PP2V5_S3_ENET_AVDD_F -              37D7
                     @m42a_lib.M42A
PP3V3_AUDIO_CODEC    PP3V3_AUDIO_CODEC - @m42a_lib.M42A  54D6
PP3V3_AVREF_SMC      PP3V3_AVREF_SMC - @m42a_lib.M42A    45D2 46C6
PP3V3_G3C_SB_RTC_D   PP3V3_G3C_SB_RTC_D - @m42a_lib.M42A 26D4
                     PP3V3_S5_SB_RTC - @m42a_lib.M42A    21D6 24B3 25A4 26D3
PP3V3_LCDVDD_SW      PP3V3_LCDVDD_SW - @m42a_lib.M42A    67C5
PP3V3_LCDVDD_SW_F    PP3V3_LCDVDD_SW_F - @m42a_lib.M42A  67B2
PP3V3_S0_ANALOG_SDVO PP3V3_S0_ANALOG_SDVO_F -            68C4 68D6
_F                   @m42a_lib.M42A
PP3V3_S0_ANALOG_TMDS PP3V3_S0_ANALOG_TMDS_F -            68B1 68B4 68D6
_F                   @m42a_lib.M42A
PP3V3_S0_AUDIO_F     PP3V3_S0_AUDIO_F - @m42a_lib.M42A   57B3 57C8 57C8 57D8
PP3V3_S0_AUDIO_SPDIF PP3V3_S0_AUDIO_SPDIF -              56B8 56D8
                     @m42a_lib.M42A
PP3V3_S0_CK410_VDD48 PP3V3_S0_CK410_VDD48 -              32D5
                     @m42a_lib.M42A
PP3V3_S0_CK410_VDDA  PP3V3_S0_CK410_VDDA -               32C7
                     @m42a_lib.M42A
PP3V3_S0_CK410_VDD_C PP3V3_S0_CK410_VDD_CPU_SRC -        32D6
PU_SRC               @m42a_lib.M42A
PP3V3_S0_CK410_VDD_P PP3V3_S0_CK410_VDD_PCI -            32D5
CI                   @m42a_lib.M42A
PP3V3_S0_CK410_VDD_R PP3V3_S0_CK410_VDD_REF -            32C5
EF                   @m42a_lib.M42A
PP3V3_S0_IMVP6_3V3   PP3V3_S0_IMVP6_3V3 - @m42a_lib.M42A 58D7
PP3V3_S0_LCD_F       PP3V3_S0_LCD_F - @m42a_lib.M42A     67B3
PP3V3_S0_NB_TVDAC    PP3V3_S0_NB_TVDAC - @m42a_lib.M42A  19C3
PP3V3_S0_NB_TVDAC_F  PP3V3_S0_NB_TVDAC_F -               19C2
                     @m42a_lib.M42A
PP3V3_S0_NB_TVDAC_FO PP3V3_S0_NB_TVDAC_FOLLOW -          19C3
LLOW                 @m42a_lib.M42A
PP3V3_S0_NB_VCCA_TVB PP3V3_S0_NB_VCCA_TVBG -             17C6 19B1
G                    @m42a_lib.M42A
PP3V3_S0_NB_VCCA_TVD PP3V3_S0_NB_VCCA_TVDACA -           17C6 19C1
ACA                  @m42a_lib.M42A
PP3V3_S0_NB_VCCA_TVD PP3V3_S0_NB_VCCA_TVDACB -           17C6 19B1
ACB                  @m42a_lib.M42A
PP3V3_S0_NB_VCCA_TVD PP3V3_S0_NB_VCCA_TVDACC -           17C6 19B1
ACC                  @m42a_lib.M42A
PP3V3_S0_PVCC1_TMDS_ PP3V3_S0_PVCC1_TMDS_F -             68C4 68C6
F                    @m42a_lib.M42A
PP3V3_S0_PVCC2_TMDS_ PP3V3_S0_PVCC2_TMDS_F -             68C4 68C7
F                    @m42a_lib.M42A
PP3V3_S0_TPM_3VSB    PP3V3_S0_TPM_3VSB - @m42a_lib.M42A  53C4
PP3V3_S3             PP3V3_S3 - @m42a_lib.M42A           5A2 64B4
                     =PP3V3_S3_PDCISENS - @m42a_lib.M42A 61C1 64B3
                     =PP3V3_S3_FW - @m42a_lib.M42A       38D5 64B3
                     =PP3V3_S3_AIRPORT_AUX -             43C3 64B3
                     @m42a_lib.M42A
                     =PP3V3_S3_RSTGATE - @m42a_lib.M42A  26B3 64B3
                     =PP3V3_S3_PCI - @m42a_lib.M42A      38C5 64B3
                     =PP3V3_S3_SMS - @m42a_lib.M42A      46D5 52C7 64B3
                     =PP3V3_S3_TPM - @m42a_lib.M42A      46D5 53C2 64B3
                     =PP3V3_S3_2V5S3 - @m42a_lib.M42A    60C4 60D6 64B3
                     =PP3V3_S3_ENET - @m42a_lib.M42A     36A5 36B4 36B5 36C8 36D6
                                                         36D8 64B3
                     =PP3V3_S3_BT - @m42a_lib.M42A       44C6 64B3
                     =PP3V3_S3_FET - @m42a_lib.M42A      63D3 64B6
                     =PP3V3_S3_SMBUS_SMC_RMT -           27D3 64B3
                     @m42a_lib.M42A
                     =PP3V3_S3_TPM - @m42a_lib.M42A      46D5 53C2 64B3
                     =PP3V3_S3_SMS - @m42a_lib.M42A      46D5 52C7 64B3
                     =PP3V3_S3_SMBUS_SMC_RMT -           27D3 64B3
                     @m42a_lib.M42A
                     =PP3V3_S3_RSTGATE - @m42a_lib.M42A  26B3 64B3
                     =PP3V3_S3_PDCISENS - @m42a_lib.M42A 61C1 64B3
                     =PP3V3_S3_PCI - @m42a_lib.M42A      38C5 64B3
                     =PP3V3_S3_FW - @m42a_lib.M42A       38D5 64B3
                     =PP3V3_S3_FET - @m42a_lib.M42A      63D3 64B6
                     =PP3V3_S3_ENET - @m42a_lib.M42A     36A5 36B4 36B5 36C8 36D6
                                                         36D8 64B3
                     =PP3V3_S3_BT - @m42a_lib.M42A       44C6 64B3
                     =PP3V3_S3_AIRPORT_AUX -             43C3 64B3
                     @m42a_lib.M42A
                     =PP3V3_S3_2V5S3 - @m42a_lib.M42A    60C4 60D6 64B3
PP3V3_S3_AIRPORT_AUX PP3V3_S3_AIRPORT_AUX_CONN -         43C4
_CONN                @m42a_lib.M42A
PP3V3_S3_BT_F        PP3V3_S3_BT_F - @m42a_lib.M42A      44C4
PP3V3_S3_FW_AVDD     PP3V3_S3_FW_AVDD - @m42a_lib.M42A   38D3
PP3V3_S3_ST_ACCEL    PP3V3_S3_ST_ACCEL - @m42a_lib.M42A  52B6
PP3V3_S5             PP3V3_S5 - @m42a_lib.M42A           5A2 64A4
                     =PP3V3_S5_LCD - @m42a_lib.M42A      64A3 67C7
                     =PP3V3_S5_FWLATEVG - @m42a_lib.M42A 39A8 64A3
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                      =PP3V3_S5_P3V3S3 - @m42a_lib.M42A   63D5 64A3
                      =PP3V3_S5_P3V3S0 - @m42a_lib.M42A   63C5 64A3
                      =PP3V3_S5_ROM - @m42a_lib.M42A      50D4 64A3
                      =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA -    24C3 64A3
                      @m42a_lib.M42A
                      =PP3V3_S5_SB_IO - @m42a_lib.M42A    22C6 64A3
                      =PP3V3_S5_SB_VCCSUS3_3_USB -        24B3 25D2 64A3
                      @m42a_lib.M42A
                      =PP3V3_S5_SB_PM - @m42a_lib.M42A    11B5 23D1 26C5 64A3
                      =PP3V3_S5_SB_VCCSUS3_3 -            24A5 24B3 25B6 25D2 64A3
                      @m42a_lib.M42A
                      =PP3V3_S5_REG - @m42a_lib.M42A      59B8 64A6
                      =PP3V3_S5_SB - @m42a_lib.M42A       23A7 23B7 23D4 23D8 25C8
                                                          64A3
                      =PP3V3_S5_SB_USB - @m42a_lib.M42A   22D8 64A3
                      =PP3V3_S5_SB_VCCSUS3_3_USB -        24B3 25D2 64A3
                      @m42a_lib.M42A
                      =PP3V3_S5_SB_VCCSUS3_3 -            24A5 24B3 25B6 25D2 64A3
                      @m42a_lib.M42A
                      =PP3V3_S5_SB_USB - @m42a_lib.M42A   22D8 64A3
                      =PP3V3_S5_SB_PM - @m42a_lib.M42A    11B5 23D1 26C5 64A3
                      =PP3V3_S5_SB_IO - @m42a_lib.M42A    22C6 64A3
                      =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA -    24C3 64A3
                      @m42a_lib.M42A
                      =PP3V3_S5_SB - @m42a_lib.M42A       23A7 23B7 23D4 23D8 25C8
                                                          64A3
                      =PP3V3_S5_ROM - @m42a_lib.M42A      50D4 64A3
                      =PP3V3_S5_REG - @m42a_lib.M42A      59B8 64A6
                      =PP3V3_S5_P3V3S3 - @m42a_lib.M42A   63D5 64A3
                      =PP3V3_S5_P3V3S0 - @m42a_lib.M42A   63C5 64A3
                      =PP3V3_S5_LCD - @m42a_lib.M42A      64A3 67C7
                      =PP3V3_S5_FWLATEVG - @m42a_lib.M42A 39A8 64A3
PP3V3_S5_FWLATEVG     PP3V3_S5_FWLATEVG - @m42a_lib.M42A  39A6 39B5
PP3V3_S5_FWLATEVG_F   PP3V3_S5_FWLATEVG_F -               39A7
                      @m42a_lib.M42A
PP3V3_S5_REG_P        PP3V3_S5_REG_P - @m42a_lib.M42A     59B8
PP3V42G3H_SW          PP3V42G3H_SW - @m42a_lib.M42A       63D2
PP3V42_G3H_LIDSWITCH  PP3V42_G3H_LIDSWITCH_F -            65A7
_F                    @m42a_lib.M42A
PP3V42_G3H_SMC_CLK_F  PP3V42_G3H_SMC_CLK_F -              46A7
                      @m42a_lib.M42A
PP3V42_ONEWIRE        PP3V42_ONEWIRE - @m42a_lib.M42A     65C7
PP4V5_AUDIO_ANALOG    PP4V5_AUDIO_ANALOG - @m42a_lib.M42A 54A3 54D2 57C3 57C5
PP5V_INV              PP5V_INV - @m42a_lib.M42A           67D5
PP5V_INV_F            PP5V_INV_F - @m42a_lib.M42A         5B1 67D3
PP5V_S0_AUDIO         PP5V_S0_AUDIO - @m42a_lib.M42A      5D1
PP5V_S0_AUDIO_F       PP5V_S0_AUDIO_F - @m42a_lib.M42A    55B8 55B8 55C4
PP5V_S0_AUDIO_PWR     PP5V_S0_AUDIO_PWR - @m42a_lib.M42A  5D1
PP5V_S0_DVIPORT       PP5V_S0_DVIPORT - @m42a_lib.M42A    68A6 69B4 69C3
PP5V_S0_DVIPORT_D     PP5V_S0_DVIPORT_D - @m42a_lib.M42A  68A8 69C5
PP5V_S0_IMVP6_VDD     PP5V_S0_IMVP6_VDD - @m42a_lib.M42A  58D7
PP5V_S0_SB_V5REF      PP5V_S0_SB_V5REF - @m42a_lib.M42A   24D5 25D7
PP5V_S0_TMDS_FUSE     PP5V_S0_TMDS_FUSE - @m42a_lib.M42A  69C5
PP5V_S3               PP5V_S3 - @m42a_lib.M42A            5A2 64B4
                      =PP5V_S3_IR - @m42a_lib.M42A        41D6 64B3
                      =PP5V_S3_GEYSER - @m42a_lib.M42A    40D6 64B3
                      =PP5V_S3_CAMERA - @m42a_lib.M42A    64B3 67A5
                      =PP5V_S3_FET - @m42a_lib.M42A       63D3 64B6
                      =PP5V_S3_SYSLED - @m42a_lib.M42A    35B6 46B4 64B3
                      =PP5V_S3_IR - @m42a_lib.M42A        41D6 64B3
                      =PP5V_S3_GEYSER - @m42a_lib.M42A    40D6 64B3
                      =PP5V_S3_FET - @m42a_lib.M42A       63D3 64B6
                      =PP5V_S3_CAMERA - @m42a_lib.M42A    64B3 67A5
PP5V_S3_CAMERA_F      PP5V_S3_CAMERA_F - @m42a_lib.M42A   67A3
PP5V_S3_GEYSER_F      PP5V_S3_GEYSER_F - @m42a_lib.M42A   40D5
PP5V_S3_SYSLED_F      PP5V_S3_SYSLED_F - @m42a_lib.M42A   35B8
PP5V_S3_USB2_EXTA     PP5V_S3_USB2_EXTA - @m42a_lib.M42A  42C7
PP5V_S3_USB2_EXTA_F   PP5V_S3_USB2_EXTA_F -               42D2 42D3
                      @m42a_lib.M42A
PP5V_S3_USB2_EXTB     PP5V_S3_USB2_EXTB - @m42a_lib.M42A  42C7
PP5V_S3_USB2_EXTB_F   PP5V_S3_USB2_EXTB_F -               42B2 42C3
                      @m42a_lib.M42A
PP5V_S5               PP5V_S5 - @m42a_lib.M42A            5A2 64A4
                      =PP5V_S5_1V8S3 - @m42a_lib.M42A     61C7 64A3
                      =PP5V_S5_PATA - @m42a_lib.M42A      34D6 64A3
                      =PP5V_S5_USB - @m42a_lib.M42A       42C8 64A3
                      =PP5V_S5_P5VS0 - @m42a_lib.M42A     63C5 64A3
                      =PP5V_S5_PWRCTL - @m42a_lib.M42A    63A7 63D6 64A3
                      =PP5V_S5_REG - @m42a_lib.M42A       59B1 64A6
                      =PP5V_S5_P5VS3 - @m42a_lib.M42A     63D5 64A3
                      =PP5V_S5_SB - @m42a_lib.M42A        25C8 64A3
                      =PP5V_S5_USB - @m42a_lib.M42A       42C8 64A3
                      =PP5V_S5_SB - @m42a_lib.M42A        25C8 64A3
                      =PP5V_S5_REG - @m42a_lib.M42A       59B1 64A6
                      =PP5V_S5_PWRCTL - @m42a_lib.M42A    63A7 63D6 64A3
                      =PP5V_S5_PATA - @m42a_lib.M42A      34D6 64A3
                      =PP5V_S5_P5VS3 - @m42a_lib.M42A     63D5 64A3
                      =PP5V_S5_P5VS0 - @m42a_lib.M42A     63C5 64A3
                      =PP5V_S5_1V8S3 - @m42a_lib.M42A     61C7 64A3
PP5V_S5_1V51V05S0_IN  PP5V_S5_1V51V05S0_INTVCC -          62A2 62C3 62C6
TVCC                  @m42a_lib.M42A
PP5V_S5_5V3V3S5_INTV  PP5V_S5_5V3V3S5_INTVCC -            59A2 59C3 59C6
CC                    @m42a_lib.M42A
PP5V_S5_REG_P         PP5V_S5_REG_P - @m42a_lib.M42A      59A6 59B1
PP5V_S5_SB_V5REF_SUS  PP5V_S5_SB_V5REF_SUS -              24D5 25C7
                      @m42a_lib.M42A
PP18V5_DCIN           PP18V5_DCIN - @m42a_lib.M42A        65D4
PP18V5_DCIN_F         PP18V5_DCIN_F - @m42a_lib.M42A      65D7
PP18V5_DCIN_ONEWIRE   PP18V5_DCIN_ONEWIRE -               65C6
                      @m42a_lib.M42A
PP18V5_G3H            PP18V5_G3H - @m42a_lib.M42A         5A2 64C1
                      =PP18V5_G3H_INRUSH - @m42a_lib.M42A 64C3 65D1
                      =PP18V5_G3H_CHGR - @m42a_lib.M42A   64C1 66D8
                      =PP18V5_G3H_INRUSH - @m42a_lib.M42A 64C3 65D1
                      =PP18V5_G3H_CHGR - @m42a_lib.M42A   64C1 66D8
PP18V5_S5_CHGR_SW_R   PP18V5_S5_CHGR_SW_R -               66C4
                      @m42a_lib.M42A
PPBUSA_G3H            PPBUSA_G3H - @m42a_lib.M42A         5A2
PPBUSB_G3H            PPBUSB_G3H - @m42a_lib.M42A         5A2 64C1
                      =PPBUS_S5_YUKON_CTRL -              60C8 64C1
                      @m42a_lib.M42A
                      =PPVIN_S5_IMVP6 - @m42a_lib.M42A    48C7 58C2 58D5 58D8 64C1
                      =PPVIN_S5_1V51V05S0 -               62D8 64C1
                      @m42a_lib.M42A
                      =PPBUSB_G3H - @m42a_lib.M42A        64C3 66C2
                      =PPBUS_S5_INV - @m42a_lib.M42A      64C1 67D4
                      =PPBUS_S5_FWPWRSW - @m42a_lib.M42A  39D6 64C1
                      =PPVIN_S5_5V3V3S5 - @m42a_lib.M42A  59D8 63B7 64C1
                      =PPVIN_S5_1V8S3 - @m42a_lib.M42A    61C7 64C1
                      =PPVIN_S5_IMVP6 - @m42a_lib.M42A    48C7 58C2 58D5 58D8 64C1
                      =PPVIN_S5_5V3V3S5 - @m42a_lib.M42A  59D8 63B7 64C1
                      =PPVIN_S5_1V8S3 - @m42a_lib.M42A    61C7 64C1
                      =PPVIN_S5_1V51V05S0 -               62D8 64C1
                      @m42a_lib.M42A
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                      =PPBUS_S5_YUKON_CTRL -              60C8 64C1
                      @m42a_lib.M42A
                      =PPBUS_S5_INV - @m42a_lib.M42A      64C1 67D4
                      =PPBUS_S5_FWPWRSW - @m42a_lib.M42A  39D6 64C1
                      =PPBUSB_G3H - @m42a_lib.M42A        64C3 66C2
                      =PPBUSA_G3H - @m42a_lib.M42A        64C3 66C2
PPBUS_ALL_INV_CONN    PPBUS_ALL_INV_CONN - @m42a_lib.M42A 5B1 67D3
PPBUS_S5_FWPWRSW_F    PPBUS_S5_FWPWRSW_F - @m42a_lib.M42A 39D6
PPDCIN_G3H_R          PPDCIN_G3H_R - @m42a_lib.M42A       65D4
PPFW_PORT0_VP         PPFW_PORT0_VP - @m42a_lib.M42A      39C2
PPFW_PORT0_VP_F       PPFW_PORT0_VP_F - @m42a_lib.M42A    39C3
PPFW_SWITCH           PPFW_SWITCH - @m42a_lib.M42A        5B2 39D4
PPVBATT_G3C_RTC       PPVBATT_G3C_RTC - @m42a_lib.M42A    26D6
PPVBATT_G3C_RTC_R     PPVBATT_G3C_RTC_R - @m42a_lib.M42A  26D5
PPVBATT_G3H_PRE       PPVBATT_G3H_PRE - @m42a_lib.M42A    66B3
PPVBATT_G3H_R         PPVBATT_G3H_R - @m42a_lib.M42A      66B2
PPVBAT_G3H_CHGR_OUT   PPVBAT_G3H_CHGR_OUT -               5C1 66B5 66C2
                      @m42a_lib.M42A
PPVBAT_G3H_CHGR_REG   PPVBAT_G3H_CHGR_REG -               66C4
                      @m42a_lib.M42A
PPVCORE_CPU_S0        PPVCORE_CPU_S0 - @m42a_lib.M42A     5B2 64D7
                      =PPVCORE_S0_CPU - @m42a_lib.M42A    8B5 8D7 9B8 48A5 48B3
                                                          64D6
                      =PPVOUT_S0_IMVP6_REG -              58D1 64D8
                      @m42a_lib.M42A
                      =PPVCORE_S0_CPU - @m42a_lib.M42A    8B5 8D7 9B8 48A5 48B3
                                                          64D6
PPVDCIN_G3H_PRE       PPVDCIN_G3H_PRE - @m42a_lib.M42A    66D4
PPVIN_S5_1V51V05S0_R  PPVIN_S5_1V51V05S0_R -              62C5
                      @m42a_lib.M42A
PPVIN_S5_5V3V3S5_R    PPVIN_S5_5V3V3S5_R - @m42a_lib.M42A 59C5
PPVIN_S5_IMVP6_VIN    PPVIN_S5_IMVP6_VIN - @m42a_lib.M42A 58D7
RSMRST_PWRGD          RSMRST_PWRGD - @m42a_lib.M42A       45D8 46D6 59A1
                      5V3V3S5_PGOOD - @m42a_lib.M42A      59A2
S0PWRGD_0V9_DIV       S0PWRGD_0V9_DIV - @m42a_lib.M42A    63B2
S0PWRGD_1V2_DIV       S0PWRGD_1V2_DIV - @m42a_lib.M42A    63A2
S0PWRGD_OK            S0PWRGD_OK - @m42a_lib.M42A         63B2
SATA_A_D2R_N          SATA_A_D2R_N - @m42a_lib.M42A       6C4 21B6
                      SATA_A_D2R_N_SPN - @m42a_lib.M42A   6C3
SATA_A_D2R_P          SATA_A_D2R_P - @m42a_lib.M42A       6C4 21B6
                      SATA_A_D2R_P_SPN - @m42a_lib.M42A   6C3
SATA_A_R2D_C_N        SATA_A_R2D_C_N - @m42a_lib.M42A     6C4 21B6
                      SATA_A_R2D_C_N_SPN - @m42a_lib.M42A 6C3
SATA_A_R2D_C_P        SATA_A_R2D_C_P - @m42a_lib.M42A     6C4 21B6
                      SATA_A_R2D_C_P_SPN - @m42a_lib.M42A 6C3
SATA_C_D2R_C_N        SATA_C_D2R_C_N - @m42a_lib.M42A     35D7
SATA_C_D2R_C_P        SATA_C_D2R_C_P - @m42a_lib.M42A     35C7
SATA_C_D2R_F_N        SATA_C_D2R_F_N - @m42a_lib.M42A     35D5
SATA_C_D2R_F_P        SATA_C_D2R_F_P - @m42a_lib.M42A     35C5
SATA_C_D2R_N          SATA_C_D2R_N - @m42a_lib.M42A       21B6 35D4
SATA_C_D2R_P          SATA_C_D2R_P - @m42a_lib.M42A       21B6 35C4
SATA_C_DET_L          SATA_C_DET_L - @m42a_lib.M42A       23D2 35D2
SATA_C_PWR_EN_L       SATA_C_PWR_EN_L - @m42a_lib.M42A    23A3 23B3
SATA_C_R2D_C_N        SATA_C_R2D_C_N - @m42a_lib.M42A     21B6 35D4
SATA_C_R2D_C_P        SATA_C_R2D_C_P - @m42a_lib.M42A     21B6 35D4
SATA_C_R2D_F_N        SATA_C_R2D_F_N - @m42a_lib.M42A     35D6
SATA_C_R2D_F_P        SATA_C_R2D_F_P - @m42a_lib.M42A     35D6
SATA_C_R2D_N          SATA_C_R2D_N - @m42a_lib.M42A       35D7
SATA_C_R2D_P          SATA_C_R2D_P - @m42a_lib.M42A       35D7
SATA_RBIAS_N          SATA_RBIAS_N - @m42a_lib.M42A       21B6 35D2
                      SATA_RBIAS_P - @m42a_lib.M42A       21B6 35D2
                      SATA_RBIAS_PN - @m42a_lib.M42A      35D3
                      SATA_RBIAS_P - @m42a_lib.M42A       21B6 35D2
SB_A20GATE            SB_A20GATE - @m42a_lib.M42A         21C4
SB_ACZ_BITCLK         SB_ACZ_BITCLK - @m42a_lib.M42A      21C6
SB_ACZ_RST_L          SB_ACZ_RST_L - @m42a_lib.M42A       21C6
SB_ACZ_SDATAOUT       SB_ACZ_SDATAOUT - @m42a_lib.M42A    21C6
SB_ACZ_SYNC           SB_ACZ_SYNC - @m42a_lib.M42A        21C6
SB_CLK14P3M_TIMER     SB_CLK14P3M_TIMER - @m42a_lib.M42A  23D3 33A6
SB_CLK48M_USBCTLR     SB_CLK48M_USBCTLR - @m42a_lib.M42A  23D3 33C7
SB_CLK100M_DMI_N      SB_CLK100M_DMI_N - @m42a_lib.M42A   22C2 33B2 33C3
SB_CLK100M_DMI_P      SB_CLK100M_DMI_P - @m42a_lib.M42A   22C2 33B2 33C3
SB_CLK100M_SATA_N     SB_CLK100M_SATA_N - @m42a_lib.M42A  21B6 33B2 33B3
SB_CLK100M_SATA_OE_L  SB_CLK100M_SATA_OE_L -              23C3 32B4
                      @m42a_lib.M42A
SB_CLK100M_SATA_P     SB_CLK100M_SATA_P - @m42a_lib.M42A  21B6 33B2 33B3
SB_GPIO2              SB_GPIO2 - @m42a_lib.M42A           22A6 26C3
SB_GPIO3              SB_GPIO3 - @m42a_lib.M42A           22A6 23A4 26C3
SB_GPIO4              SB_GPIO4 - @m42a_lib.M42A           22A6 26C3
SB_GPIO5              SB_GPIO5 - @m42a_lib.M42A           22A6 26C3 34C8
                      ODD_PWR_EN_L - @m42a_lib.M42A       34C8
SB_GPIO14             SB_GPIO14 - @m42a_lib.M42A          23A4 23C3
SB_GPIO19             SB_GPIO19 - @m42a_lib.M42A          23D3
SB_GPIO21             SB_GPIO21 - @m42a_lib.M42A          23D3
SB_GPIO26             SB_GPIO26 - @m42a_lib.M42A          23C8
SB_GPIO29             SB_GPIO29 - @m42a_lib.M42A          22C4 22D8
SB_GPIO30             SB_GPIO30 - @m42a_lib.M42A          22C4 22D8 36D8
SB_GPIO31             SB_GPIO31 - @m42a_lib.M42A          22C4 22D8
SB_GPIO37             SB_GPIO37 - @m42a_lib.M42A          23D3
SB_INTVRMEN           SB_INTVRMEN - @m42a_lib.M42A        21D6
SB_RTC_RST_L          SB_RTC_RST_L - @m42a_lib.M42A       21D6 26D4
SB_RTC_X1             SB_RTC_X1 - @m42a_lib.M42A          21D6 26C8
SB_RTC_X1_R           SB_RTC_X1_R - @m42a_lib.M42A        26C7
SB_RTC_X2             SB_RTC_X2 - @m42a_lib.M42A          21D6 26C8
SB_RUNTIME_SCI_L      SB_RUNTIME_SCI_L - @m42a_lib.M42A   23C5
SB_SM_INTRUDER_L      SB_SM_INTRUDER_L - @m42a_lib.M42A   21D6 26D4
SB_SPKR               SB_SPKR - @m42a_lib.M42A            23C5
SC_RX_L               SC_RX_L - @m42a_lib.M42A            45C5 46B1
SC_TX_L               SC_TX_L - @m42a_lib.M42A            45C5 46B1
SDATAIN               SDATAIN - @m42a_lib.M42A            54C6
SDVO_CTRLCLK          SDVO_CTRLCLK - @m42a_lib.M42A       14B6 68A6
SDVO_CTRLDATA         SDVO_CTRLDATA - @m42a_lib.M42A      14B6 68A6
SMBUS_BATT_SCL_F      SMBUS_BATT_SCL_F - @m42a_lib.M42A   5D1 65B6
SMBUS_BATT_SDA_F      SMBUS_BATT_SDA_F - @m42a_lib.M42A   5D1 65A6
SMB_0_CLK             SMB_0_CLK - @m42a_lib.M42A          27D6 45C8
                      SMBUS_SMC_0_SCL - @m42a_lib.M42A    27D5
                      THRM_DIMM1_SMB_CLK - @m42a_lib.M42A 27D3 49B4
                      SMBUS_SMC_0_SCL - @m42a_lib.M42A    27D5
SMB_0_DATA            SMB_0_DATA - @m42a_lib.M42A         27D6 45C5
                      SMBUS_SMC_0_SDA - @m42a_lib.M42A    27D5
                      THRM_DIMM1_SMB_DATA -               27C3 49B4
                      @m42a_lib.M42A
                      SMBUS_SMC_0_SDA - @m42a_lib.M42A    27D5
SMB_AIRPORT_CONN_CLK  SMB_AIRPORT_CONN_CLK -              43B5
                      @m42a_lib.M42A
SMB_AIRPORT_CONN_DAT  SMB_AIRPORT_CONN_DATA -             43B5
A                     @m42a_lib.M42A
SMB_ALERT_L           SMB_ALERT_L - @m42a_lib.M42A        23C5
SMB_BSA_CLK           SMB_BSA_CLK - @m42a_lib.M42A        27C3 45B5
                      SMBUS_SMC_BSA_SCL - @m42a_lib.M42A  27C2
                      =SMBUS_BATT_SCL - @m42a_lib.M42A    27C1 65A2
                      SMBUS_SMC_BSA_SCL - @m42a_lib.M42A  27C2
                      =SMBUS_BATT_SCL - @m42a_lib.M42A    27C1 65A2
SMB_BSA_DATA          SMB_BSA_DATA - @m42a_lib.M42A       27C3 45B5
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                      SMBUS_SMC_BSA_SDA - @m42a_lib.M42A  27C2
                      =SMBUS_BATT_SDA - @m42a_lib.M42A    27C1 65A2
                      SMBUS_SMC_BSA_SDA - @m42a_lib.M42A  27C2
                      =SMBUS_BATT_SDA - @m42a_lib.M42A    27C1 65A2
SMB_BSB_CLK           SMB_BSB_CLK - @m42a_lib.M42A        27B3 45C5
SMB_BSB_DATA          SMB_BSB_DATA - @m42a_lib.M42A       27B3 45C8
SMB_LINK_ALERT_L      SMB_LINK_ALERT_L - @m42a_lib.M42A   23D5
SMB_MLB_CLK           SMB_MLB_CLK - @m42a_lib.M42A        27C6 45B5
                      THRM_DIMM0_SMB_CLK - @m42a_lib.M42A 27B3 49C4
                      SMBUS_SMC_MLB_SCL - @m42a_lib.M42A  5B2 27C5
                      SMB_THRM_CLK - @m42a_lib.M42A       10B3 27C3
                      THRM_DIMM0_SMB_CLK - @m42a_lib.M42A 27B3 49C4
                      SMB_THRM_CLK - @m42a_lib.M42A       10B3 27C3
                      SMBUS_SMC_MLB_SCL - @m42a_lib.M42A  5B2 27C5
SMB_MLB_DATA          SMB_MLB_DATA - @m42a_lib.M42A       27B6 45B5
                      THRM_DIMM0_SMB_DATA -               27B3 49C4
                      @m42a_lib.M42A
                      SMBUS_SMC_MLB_SDA - @m42a_lib.M42A  5B2 27B5
                      SMB_THRM_DATA - @m42a_lib.M42A      10B3 27B3
                      THRM_DIMM0_SMB_DATA -               27B3 49C4
                      @m42a_lib.M42A
                      SMB_THRM_DATA - @m42a_lib.M42A      10B3 27B3
                      SMBUS_SMC_MLB_SDA - @m42a_lib.M42A  5B2 27B5
SMC_AVCC_RC           SMC_AVCC_RC - @m42a_lib.M42A        45D3
SMC_BATT_CHG_EN       SMC_BATT_CHG_EN - @m42a_lib.M42A    5C1 45D8 46B6 66A4
SMC_BATT_ISENSE       SMC_BATT_ISENSE - @m42a_lib.M42A    45D5 66B1
SMC_BATT_ISET         SMC_BATT_ISET - @m42a_lib.M42A      5C1 45B5 66B7
SMC_BATT_TRICKLE_EN_  SMC_BATT_TRICKLE_EN_L -             5C1 45D8 46B6 66A3
L                     @m42a_lib.M42A
SMC_BATT_VSET         SMC_BATT_VSET - @m42a_lib.M42A      45B5 46C3
SMC_BC_ACOK           SMC_BC_ACOK - @m42a_lib.M42A        5C1 45C5 46B6 65C3 65C7
                                                          66A5
SMC_BKLIGHT_ENABLE    SMC_BKLIGHT_ENABLE - @m42a_lib.M42A 45C8
SMC_BS_ALRT_L         SMC_BS_ALRT_L - @m42a_lib.M42A      5D1 45C5 46C6 65A2
SMC_BS_ALRT_L_F       SMC_BS_ALRT_L_F - @m42a_lib.M42A    65A6
SMC_CASE_OPEN         SMC_CASE_OPEN - @m42a_lib.M42A      45C5 46B3
SMC_CPU_ISENSE        SMC_CPU_ISENSE - @m42a_lib.M42A     45D5 48C1
SMC_CPU_RESET_3_3_L   SMC_CPU_RESET_3_3_L -               45B5 46C1
                      @m42a_lib.M42A
SMC_CPU_VSENSE        SMC_CPU_VSENSE - @m42a_lib.M42A     5B2 45D5 48B1
SMC_DCIN_ISENSE       SMC_DCIN_ISENSE - @m42a_lib.M42A    45D5 66C2
SMC_DISPLAY_ENABLE    SMC_DISPLAY_ENABLE - @m42a_lib.M42A 45C8
SMC_DISP_BKLT_A       SMC_DISP_BKLT_A - @m42a_lib.M42A    45B5
SMC_DISP_BKLT_B       SMC_DISP_BKLT_B - @m42a_lib.M42A    45B5 46C3
SMC_EXCARD_CP         SMC_EXCARD_CP - @m42a_lib.M42A      45B8 46C3
SMC_EXCARD_PWR_EN     SMC_EXCARD_PWR_EN - @m42a_lib.M42A  45B8 46C3
SMC_EXCARD_PWR_OC_L   SMC_EXCARD_PWR_OC_L -               45B8 46D3
                      @m42a_lib.M42A
SMC_EXTAL             SMC_EXTAL - @m42a_lib.M42A          45C4 46C7
SMC_EXTSMI_L          SMC_EXTSMI_L - @m42a_lib.M42A       23B8 45B8
SMC_FAN_0_CTL         SMC_FAN_0_CTL - @m42a_lib.M42A      45B8 46C3
SMC_FAN_0_TACH        SMC_FAN_0_TACH - @m42a_lib.M42A     45B8 46C3
SMC_FAN_1_CTL         SMC_FAN_1_CTL - @m42a_lib.M42A      5D2 45B8 51B4
SMC_FAN_1_TACH        SMC_FAN_1_TACH - @m42a_lib.M42A     5D2 45B8 51C4
SMC_FAN_2_CTL         SMC_FAN_2_CTL - @m42a_lib.M42A      45B8 46C3
SMC_FAN_2_TACH        SMC_FAN_2_TACH - @m42a_lib.M42A     45B8 46C3
SMC_FAN_3_CTL         SMC_FAN_3_CTL - @m42a_lib.M42A      45B8 46C3
SMC_FAN_3_TACH        SMC_FAN_3_TACH - @m42a_lib.M42A     5A7 45B8 46C3
SMC_FWE               SMC_FWE - @m42a_lib.M42A            45B5 46C6
SMC_FWIRE_ISENSE      SMC_FWIRE_ISENSE - @m42a_lib.M42A   45D5 46B3
SMC_GPU_ISENSE        SMC_GPU_ISENSE - @m42a_lib.M42A     45D5 46C6
SMC_GPU_VSENSE        SMC_GPU_VSENSE - @m42a_lib.M42A     45D5 46C6
SMC_LID               SMC_LID - @m42a_lib.M42A            5B2 40C4 45B5 46C6 65A8
SMC_LID_F             SMC_LID_F - @m42a_lib.M42A          65A7
SMC_LRESET_L          SMC_LRESET_L - @m42a_lib.M42A       26B1 45C8
SMC_MANUAL_RST_L      SMC_MANUAL_RST_L - @m42a_lib.M42A   5B2 46D8
SMC_MD1               SMC_MD1 - @m42a_lib.M42A            5C2 45C2 47B6
SMC_MEM_ISENSE        SMC_MEM_ISENSE - @m42a_lib.M42A     45A8 46B3 61C1
SMC_NB_ISENSE         SMC_NB_ISENSE - @m42a_lib.M42A      45B8 46B3 62A5
SMC_NMI               SMC_NMI - @m42a_lib.M42A            5C2 45C1 47B5
SMC_ODD_DETECT        SMC_ODD_DETECT - @m42a_lib.M42A     34B3 45B8
SMC_ONOFF_L           SMC_ONOFF_L - @m42a_lib.M42A        40C8 45C5 46C8 46D6 48C8
                      CONN_GEYSER_ONOFF_L -               40C7
                      @m42a_lib.M42A
SMC_P20               SMC_P20 - @m42a_lib.M42A            45D8 46C6
SMC_P21               SMC_P21 - @m42a_lib.M42A            45D8 46C6
SMC_P22               SMC_P22 - @m42a_lib.M42A            45D8 46C6
SMC_P23               SMC_P23 - @m42a_lib.M42A            45D8 46C6
SMC_P26               SMC_P26 - @m42a_lib.M42A            45D8 46C6
SMC_P27               SMC_P27 - @m42a_lib.M42A            45D8 46C6
SMC_P44               SMC_P44 - @m42a_lib.M42A            45C8 46C6
SMC_P46               SMC_P46 - @m42a_lib.M42A            45C8 46C6
SMC_PB7               SMC_PB7 - @m42a_lib.M42A            45B8 46C6
SMC_PBUS_VSENSE       SMC_PBUS_VSENSE - @m42a_lib.M42A    45D5 48C5
SMC_PD3               SMC_PD3 - @m42a_lib.M42A            45B8 46C3
SMC_PG1               SMC_PG1 - @m42a_lib.M42A            45B5 46C6
SMC_PM_G2_EN          SMC_PM_G2_EN - @m42a_lib.M42A       45D5 63C8
SMC_PM_G2_EN_L        SMC_PM_G2_EN_L - @m42a_lib.M42A     63C7
SMC_PROCHOT           SMC_PROCHOT - @m42a_lib.M42A        45B5 46B6
SMC_PROCHOT_3_3_L     SMC_PROCHOT_3_3_L - @m42a_lib.M42A  45D5 46C1
SMC_PS_ON             SMC_PS_ON - @m42a_lib.M42A          5C1 39C6 45D5 46B3 65C3
SMC_RCIN_L            SMC_RCIN_L - @m42a_lib.M42A         21C3 45C8
SMC_RSTGATE_L         SMC_RSTGATE_L - @m42a_lib.M42A      26A3 45D8
SMC_RST_L             SMC_RST_L - @m42a_lib.M42A          5C2 45C3 46D7 47C5
SMC_RUNTIME_SCI_L     SMC_RUNTIME_SCI_L - @m42a_lib.M42A  23C8 45B8
SMC_RX_L              SMC_RX_L - @m42a_lib.M42A           5C2 45C8 46B2 46D6 47B5
SMC_SB_NMI            SMC_SB_NMI - @m42a_lib.M42A         23C3 45D8
SMC_SUS_CLK           SMC_SUS_CLK - @m42a_lib.M42A        45C5 46A6
SMC_SUS_CLK_R         SMC_SUS_CLK_R - @m42a_lib.M42A      46A7
SMC_SYS_ISET          SMC_SYS_ISET - @m42a_lib.M42A       45B5 66D7
SMC_SYS_KBDLED        SMC_SYS_KBDLED - @m42a_lib.M42A     45C8 46C6
SMC_SYS_LED_16B       SMC_SYS_LED_16B - @m42a_lib.M42A    45C8 46A4
SMC_SYS_VSET          SMC_SYS_VSET - @m42a_lib.M42A       45B5 46C3
SMC_TCK               SMC_TCK - @m42a_lib.M42A            5C2 45C5 46C6 47C5
SMC_TDI               SMC_TDI - @m42a_lib.M42A            5C2 45C5 46C6 47C5
SMC_TDO               SMC_TDO - @m42a_lib.M42A            5C2 45C5 46C6 47B6
SMC_THRMTRIP          SMC_THRMTRIP - @m42a_lib.M42A       45B5 46B5
SMC_TMS               SMC_TMS - @m42a_lib.M42A            5C2 45B5 46C6 47C6
SMC_TPM_GPIO          SMC_TPM_GPIO - @m42a_lib.M42A       45D5 46B2
SMC_TPM_PP            SMC_TPM_PP - @m42a_lib.M42A         45C8 53C7
SMC_TPM_PP_R          SMC_TPM_PP_R - @m42a_lib.M42A       53C6
SMC_TPM_RESET_L       SMC_TPM_RESET_L - @m42a_lib.M42A    45C8 46D6 53B7
SMC_TRST_L            SMC_TRST_L - @m42a_lib.M42A         5C2 45C1 47C6
SMC_TX_L              SMC_TX_L - @m42a_lib.M42A           5C2 45C8 46B2 46D6 47B6
SMC_VCL               SMC_VCL - @m42a_lib.M42A            45D3
SMC_WAKE_SCI_L        SMC_WAKE_SCI_L - @m42a_lib.M42A     23C1 45D5
SMC_XTAL              SMC_XTAL - @m42a_lib.M42A           45C4 46C7
SMLINK<0>             SMLINK<0> - @m42a_lib.M42A          23D5
SMLINK<1>             SMLINK<1> - @m42a_lib.M42A          23D5
SMS_ACC_SELFTEST      SMS_ACC_SELFTEST - @m42a_lib.M42A   52B6
SMS_INT_L             SMS_INT_L - @m42a_lib.M42A          23C3 45B5 46D6
SMS_ONOFF_L           SMS_ONOFF_L - @m42a_lib.M42A        45B5 52C7
SMS_X_AXIS            SMS_X_AXIS - @m42a_lib.M42A         45B8 52C2
SMS_Y_AXIS            SMS_Y_AXIS - @m42a_lib.M42A         45B8 52C2
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SMS_Z_AXIS            SMS_Z_AXIS - @m42a_lib.M42A         45B8 52C2
SPI_ARB               SPI_ARB - @m42a_lib.M42A            22C6 45D5
SPI_CE_L              SPI_CE_L - @m42a_lib.M42A           22C6 45B5 50C7
SPI_HOLD_L            SPI_HOLD_L - @m42a_lib.M42A         50C4
SPI_SCLK              SPI_SCLK - @m42a_lib.M42A           22C6 45D5 50C7
SPI_SCLK_R            SPI_SCLK_R - @m42a_lib.M42A         50C4
SPI_SI                SPI_SI - @m42a_lib.M42A             22C6 45D5 50C1
SPI_SI_R              SPI_SI_R - @m42a_lib.M42A           50C3
SPI_SO                SPI_SO - @m42a_lib.M42A             22C6 45D5 50C1
SPI_SO_R              SPI_SO_R - @m42a_lib.M42A           50C3
SPI_WP_L              SPI_WP_L - @m42a_lib.M42A           50C4
SPKRAMP_L_N_OUT       SPKRAMP_L_N_OUT - @m42a_lib.M42A    55B4 55C3
SPKRAMP_L_P_OUT       SPKRAMP_L_P_OUT - @m42a_lib.M42A    55B4 55C3
SPKRAMP_R_N_OUT       SPKRAMP_R_N_OUT - @m42a_lib.M42A    55C3 55C4
SPKRAMP_R_P_OUT       SPKRAMP_R_P_OUT - @m42a_lib.M42A    55C4 55D3
SPKRAMP_SUB_N_OUT     SPKRAMP_SUB_N_OUT - @m42a_lib.M42A  55A4 55B3
SPKRAMP_SUB_P_OUT     SPKRAMP_SUB_P_OUT - @m42a_lib.M42A  55A4 55B3
SPKRAMP_SYNC1         SPKRAMP_SYNC1 - @m42a_lib.M42A      55A4 55C4
SPKRAMP_SYNC2         SPKRAMP_SYNC2 - @m42a_lib.M42A      55A4 55B4
SPKRAMP_THERMPLANE    SPKRAMP_THERMPLANE - @m42a_lib.M42A 55A4 55A4 55B4 55C4
SPKRCONN_L_N_OUT      SPKRCONN_L_N_OUT - @m42a_lib.M42A   55C1 56D2
SPKRCONN_L_P_OUT      SPKRCONN_L_P_OUT - @m42a_lib.M42A   55C1 56D2
SPKRCONN_R_N_OUT      SPKRCONN_R_N_OUT - @m42a_lib.M42A   55C1 56C2
SPKRCONN_R_P_OUT      SPKRCONN_R_P_OUT - @m42a_lib.M42A   55D1 56C2
SPKRCONN_SUB_N_OUT    SPKRCONN_SUB_N_OUT - @m42a_lib.M42A 55B1 56C2
SPKRCONN_SUB_P_OUT    SPKRCONN_SUB_P_OUT - @m42a_lib.M42A 55B1 56C2
SPKR_SHIELD           SPKR_SHIELD - @m42a_lib.M42A        56C2
ST_ACCEL_ON_L         ST_ACCEL_ON_L - @m42a_lib.M42A      52B6
SUS_CLK_SB            SUS_CLK_SB - @m42a_lib.M42A         6B4 23C3
                      SUS_CLK_SB_SPN - @m42a_lib.M42A     6B3
SV_SET_UP             SV_SET_UP - @m42a_lib.M42A          5C2 23B6 23C3 47B5
SYS_LED_ANODE         SYS_LED_ANODE - @m42a_lib.M42A      5B2 35C5 46A3
SYS_LED_ANODE_L       SYS_LED_ANODE_L - @m42a_lib.M42A    35C7
SYS_LED_ILIM          SYS_LED_ILIM - @m42a_lib.M42A       46A3
SYS_LED_L             SYS_LED_L - @m42a_lib.M42A          46A3
SYS_LED_L_VDIV        SYS_LED_L_VDIV - @m42a_lib.M42A     46A3
SYS_ONEWIRE           SYS_ONEWIRE - @m42a_lib.M42A        5C1 45B8 46D6 65C8
THRM_ALERT            THRM_ALERT - @m42a_lib.M42A         10B4
THRM_ALERT_L          THRM_ALERT_L - @m42a_lib.M42A       10C4
THRM_CPU_DX_N         THRM_CPU_DX_N - @m42a_lib.M42A      10B5
THRM_CPU_DX_P         THRM_CPU_DX_P - @m42a_lib.M42A      10B5
THRM_DIMM0_3V3_UNFIL  THRM_DIMM0_3V3_UNFILTERED -         49D4
TERED                 @m42a_lib.M42A
THRM_DIMM0_DXN        THRM_DIMM0_DXN - @m42a_lib.M42A     40C5 49C6
THRM_DIMM0_DXP1       THRM_DIMM0_DXP1 - @m42a_lib.M42A    40C4 49D6
THRM_DIMM0_DXP2       THRM_DIMM0_DXP2 - @m42a_lib.M42A    49C6
THRM_DIMM1_3V3_UNFIL  THRM_DIMM1_3V3_UNFILTERED -         49B4
TERED                 @m42a_lib.M42A
THRM_DIMM1_DXN        THRM_DIMM1_DXN - @m42a_lib.M42A     49B5
THRM_DIMM1_DXP1       THRM_DIMM1_DXP1 - @m42a_lib.M42A    49B5
THRM_DIMM1_DXP2       THRM_DIMM1_DXP2 - @m42a_lib.M42A    49A5
TMDS_EXT_RES          TMDS_EXT_RES - @m42a_lib.M42A       68B4
TMDS_EXT_SWING        TMDS_EXT_SWING - @m42a_lib.M42A     68B3
TMDS_HTPLG            TMDS_HTPLG - @m42a_lib.M42A         68A7 69C6
TMDS_HTPLG_R          TMDS_HTPLG_R - @m42a_lib.M42A       68A7
TMDS_I2C_SCL          TMDS_I2C_SCL - @m42a_lib.M42A       68B2
TMDS_I2C_SDA          TMDS_I2C_SDA - @m42a_lib.M42A       68B2
TMDS_INT_N            TMDS_INT_N - @m42a_lib.M42A         68B5
TMDS_INT_P            TMDS_INT_P - @m42a_lib.M42A         68B5
TMDS_RST_L            TMDS_RST_L - @m42a_lib.M42A         26B1 68B5
TMDS_SDB_N            TMDS_SDB_N - @m42a_lib.M42A         68B4
TMDS_SDB_P            TMDS_SDB_P - @m42a_lib.M42A         68B4
TMDS_SDC_N            TMDS_SDC_N - @m42a_lib.M42A         68B4
TMDS_SDC_P            TMDS_SDC_P - @m42a_lib.M42A         68B4
TMDS_SDG_N            TMDS_SDG_N - @m42a_lib.M42A         68B4
TMDS_SDG_P            TMDS_SDG_P - @m42a_lib.M42A         68B4
TMDS_SDR_N            TMDS_SDR_N - @m42a_lib.M42A         68B4
TMDS_SDR_P            TMDS_SDR_P - @m42a_lib.M42A         68B4
TMDS_TX<0>            TMDS_TX<0> - @m42a_lib.M42A         68D2
TMDS_TX<1>            TMDS_TX<1> - @m42a_lib.M42A         68D2
TMDS_TX<2>            TMDS_TX<2> - @m42a_lib.M42A         68C2
TMDS_TX_CLK           TMDS_TX_CLK - @m42a_lib.M42A        68C2
TMDS_TX_CLK_N         TMDS_TX_CLK_N - @m42a_lib.M42A      68B2 68C1 69A2
TMDS_TX_CLK_P         TMDS_TX_CLK_P - @m42a_lib.M42A      68B2 68C3 69A2
TMDS_TX_CONN_CLK_N    TMDS_TX_CONN_CLK_N - @m42a_lib.M42A 69B3
TMDS_TX_CONN_CLK_P    TMDS_TX_CONN_CLK_P - @m42a_lib.M42A 69B3
TMDS_TX_CONN_N<0>     TMDS_TX_CONN_N<0> - @m42a_lib.M42A  69B3
TMDS_TX_CONN_N<1>     TMDS_TX_CONN_N<1> - @m42a_lib.M42A  69B3
TMDS_TX_CONN_N<2>     TMDS_TX_CONN_N<2> - @m42a_lib.M42A  69B3
TMDS_TX_CONN_P<0>     TMDS_TX_CONN_P<0> - @m42a_lib.M42A  69B3
TMDS_TX_CONN_P<1>     TMDS_TX_CONN_P<1> - @m42a_lib.M42A  69B3
TMDS_TX_CONN_P<2>     TMDS_TX_CONN_P<2> - @m42a_lib.M42A  69B3
TMDS_TX_N<0>          TMDS_TX_N<0> - @m42a_lib.M42A       68B2 68D1 69B2
TMDS_TX_N<1>          TMDS_TX_N<1> - @m42a_lib.M42A       68B2 68D1 69B2
TMDS_TX_N<2>          TMDS_TX_N<2> - @m42a_lib.M42A       68B2 68C1 69B2
TMDS_TX_P<0>          TMDS_TX_P<0> - @m42a_lib.M42A       68B2 68D3 69B2
TMDS_TX_P<1>          TMDS_TX_P<1> - @m42a_lib.M42A       68B2 68D3 69B2
TMDS_TX_P<2>          TMDS_TX_P<2> - @m42a_lib.M42A       68B2 68C3 69B2
TPM_BADD              TPM_BADD - @m42a_lib.M42A           53C3
TPM_GPIO1             TPM_GPIO1 - @m42a_lib.M42A          46B1 53C6
TPM_GPIO2             TPM_GPIO2 - @m42a_lib.M42A          46B1 53C6
TPM_LRESET_L          TPM_LRESET_L - @m42a_lib.M42A       26B1 53B7
TPM_RST_L             TPM_RST_L - @m42a_lib.M42A          53B6
TPM_XTALI             TPM_XTALI - @m42a_lib.M42A          53C6
TPM_XTALO             TPM_XTALO - @m42a_lib.M42A          53C6
TPS73115_NR           TPS73115_NR - @m42a_lib.M42A        19D5
TP_AZ_DOCK_EN_L       TP_AZ_DOCK_EN_L - @m42a_lib.M42A    23C5
TP_AZ_DOCK_RST_L      TP_AZ_DOCK_RST_L - @m42a_lib.M42A   23C5
TP_CPU_A32_L          TP_CPU_A32_L - @m42a_lib.M42A       7C8
TP_CPU_A33_L          TP_CPU_A33_L - @m42a_lib.M42A       7B8
TP_CPU_A34_L          TP_CPU_A34_L - @m42a_lib.M42A       7B8
TP_CPU_A35_L          TP_CPU_A35_L - @m42a_lib.M42A       7B8
TP_CPU_A36_L          TP_CPU_A36_L - @m42a_lib.M42A       7B8
TP_CPU_A37_L          TP_CPU_A37_L - @m42a_lib.M42A       7B8
TP_CPU_A38_L          TP_CPU_A38_L - @m42a_lib.M42A       7B8
TP_CPU_A39_L          TP_CPU_A39_L - @m42a_lib.M42A       7B8
TP_CPU_APM0_L         TP_CPU_APM0_L - @m42a_lib.M42A      7B8
TP_CPU_APM1_L         TP_CPU_APM1_L - @m42a_lib.M42A      7B8
TP_CPU_CPUSLP_L       TP_CPU_CPUSLP_L - @m42a_lib.M42A    21C4
TP_CPU_EXTBREF        TP_CPU_EXTBREF - @m42a_lib.M42A     7B6
TP_CPU_HFPLL          TP_CPU_HFPLL - @m42a_lib.M42A       7B8
TP_CPU_SPARE0         TP_CPU_SPARE0 - @m42a_lib.M42A      7B6
TP_CPU_SPARE1         TP_CPU_SPARE1 - @m42a_lib.M42A      7B6
TP_CPU_SPARE2         TP_CPU_SPARE2 - @m42a_lib.M42A      7B6
TP_CPU_SPARE3         TP_CPU_SPARE3 - @m42a_lib.M42A      7B6
TP_CPU_SPARE4         TP_CPU_SPARE4 - @m42a_lib.M42A      7B6
TP_CPU_SPARE5         TP_CPU_SPARE5 - @m42a_lib.M42A      7B6
TP_CPU_SPARE6         TP_CPU_SPARE6 - @m42a_lib.M42A      7B6
TP_CPU_SPARE7         TP_CPU_SPARE7 - @m42a_lib.M42A      7B6
TP_LVDS_VBG           TP_LVDS_VBG - @m42a_lib.M42A        13D5
TP_NB_TESTIN_L        TP_NB_TESTIN_L - @m42a_lib.M42A     14D6
TP_NB_XOR_FSB2_H7     TP_NB_XOR_FSB2_H7 - @m42a_lib.M42A  14D6
TP_NB_XOR_LVDS_A34    TP_NB_XOR_LVDS_A34 - @m42a_lib.M42A 14C6
TP_NB_XOR_LVDS_A35    TP_NB_XOR_LVDS_A35 - @m42a_lib.M42A 14C6
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TP_NB_XOR_LVDS_D27	TP_NB_XOR_LVDS_D27 - @m42a_lib.M42A	14C6
TP_NB_XOR_LVDS_D28	TP_NB_XOR_LVDS_D28 - @m42a_lib.M42A	14C6
TP_PCI_GNT0_L	TP_PCI_GNT0_L - @m42a_lib.M42A	22B6
TP_PCI_GNT1_L	TP_PCI_GNT1_L - @m42a_lib.M42A	22B6
TP_PCI_GNT2_L	TP_PCI_GNT2_L - @m42a_lib.M42A	22B6
TP_PCI_PME_L	TP_PCI_PME_L - @m42a_lib.M42A	22A6
TP_SB_ACZ_SDIN1	TP_SB_ACZ_SDIN1 - @m42a_lib.M42A	21C6
TP_SB_ACZ_SDIN2	TP_SB_ACZ_SDIN2 - @m42a_lib.M42A	21C6
TP_SB_DRQ0_L	TP_SB_DRQ0_L - @m42a_lib.M42A	21D4
TP_SB_GPIO6	TP_SB_GPIO6 - @m42a_lib.M42A	23C5
TP_SB_GPIO22	TP_SB_GPIO22 - @m42a_lib.M42A	6B1 22B6
	=SB_GPIO22 - @m42a_lib.M42A	6B2 69A6
	SB_GPIO22 - @m42a_lib.M42A	6B2
	=SB_GPIO22 - @m42a_lib.M42A	6B2 69A6
TP_SB_GPIO23	TP_SB_GPIO23 - @m42a_lib.M42A	21D5
TP_SB_GPIO25_DO_NOT_	TP_SB_GPIO25_DO_NOT_USE -	23C3
USE	@m42a_lib.M42A	
TP_SB_GPIO38	TP_SB_GPIO38 - @m42a_lib.M42A	23C3
TP_SB_RCVENIN_L	TP_SB_RCVENIN_L - @m42a_lib.M42A	15B2
TP_SB_RSVD9	TP_SB_RSVD9 - @m42a_lib.M42A	22A6
TP_SB_SATALED_L	TP_SB_SATALED_L - @m42a_lib.M42A	21C6
TP_SB_XOR-AD5	TP_SB_XOR-AD5 - @m42a_lib.M42A	22A7
TP_SB_XOR-AD9	TP_SB_XOR-AD9 - @m42a_lib.M42A	22A7
TP_SB_XOR-AE5	TP_SB_XOR-AE5 - @m42a_lib.M42A	22A7
TP_SB_XOR-AG4	TP_SB_XOR-AG4 - @m42a_lib.M42A	22A7
TP_SB_XOR-AH4	TP_SB_XOR-AH4 - @m42a_lib.M42A	22A7
TP_SB_XOR-U3	TP_SB_XOR-U3 - @m42a_lib.M42A	21C6
TP_SB_XOR-U7	TP_SB_XOR-U7 - @m42a_lib.M42A	21C6
TP_SB_XOR-V6	TP_SB_XOR-V6 - @m42a_lib.M42A	21C6
TP_SB_XOR-V7	TP_SB_XOR-V7 - @m42a_lib.M42A	21C6
TP_SB_XOR-Y1	TP_SB_XOR-Y1 - @m42a_lib.M42A	21C6
TP_SB_XOR-Y2	TP_SB_XOR-Y2 - @m42a_lib.M42A	21C6
TP_SB_XOR_AE9	TP_SB_XOR_AE9 - @m42a_lib.M42A	22A6
TP_SB_XOR_AG8	TP_SB_XOR_AG8 - @m42a_lib.M42A	22A6
TP_SB_XOR_AH8	TP_SB_XOR_AH8 - @m42a_lib.M42A	22A6
TP_SB_XOR_W1	TP_SB_XOR_W1 - @m42a_lib.M42A	21C6
TP_USBN_F	TP_USBN_F - @m42a_lib.M42A	5C1
TP_USBP_F	TP_USBP_F - @m42a_lib.M42A	5C1
TV_DACA_OUT	TV_DACA_OUT - @m42a_lib.M42A	13C5 69B8
TV_DACB_OUT	TV_DACB_OUT - @m42a_lib.M42A	13C5 69A8
TV_DACC_OUT	TV_DACC_OUT - @m42a_lib.M42A	13C5 69A8
TV_IREF	TV_IREF - @m42a_lib.M42A	13C5 69C8
USB2_BT_F_N	USB2_BT_F_N - @m42a_lib.M42A	44C4
USB2_BT_F_P	USB2_BT_F_P - @m42a_lib.M42A	44B4
USB2_CAMERA_CONN_N	USB2_CAMERA_CONN_N - @m42a_lib.M42A	67A2
USB2_CAMERA_CONN_P	USB2_CAMERA_CONN_P - @m42a_lib.M42A	67B2
USB2_EXTA_F_N	USB2_EXTA_F_N - @m42a_lib.M42A	42C2
USB2_EXTA_F_P	USB2_EXTA_F_P - @m42a_lib.M42A	42C2
USB2_EXTB_F_N	USB2_EXTB_F_N - @m42a_lib.M42A	42B2
USB2_EXTB_F_P	USB2_EXTB_F_P - @m42a_lib.M42A	42B2
USB2_GND_EXTA_F	USB2_GND_EXTA_F - @m42a_lib.M42A	42C2
USB2_GND_EXTB_F	USB2_GND_EXTB_F - @m42a_lib.M42A	42B2
USB_A_N	USB_A_N - @m42a_lib.M42A	6C1 22C2
	=USB2_EXTA_N - @m42a_lib.M42A	6C2 42C5
	USB2_EXTA_N - @m42a_lib.M42A	6C2
	=USB2_EXTA_N - @m42a_lib.M42A	6C2 42C5
USB_A_OC_L	USB_A_OC_L - @m42a_lib.M42A	6C1 22C4 22D8
	=EXTAUSB_OC_L - @m42a_lib.M42A	6C2 42C8
	EXTAUSB_OC_L - @m42a_lib.M42A	6C2
	=EXTAUSB_OC_L - @m42a_lib.M42A	6C2 42C8
USB_A_P	USB_A_P - @m42a_lib.M42A	6C1 22C2
	=USB2_EXTA_P - @m42a_lib.M42A	6C2 42C5
	USB2_EXTA_P - @m42a_lib.M42A	6C2
	=USB2_EXTA_P - @m42a_lib.M42A	6C2 42C5
USB_B_N	USB_B_N - @m42a_lib.M42A	6C1 22C2
	=USB2_GEYSER_N - @m42a_lib.M42A	6C2 40C7
	USB2_GEYSER_N - @m42a_lib.M42A	6C2
	=USB2_GEYSER_N - @m42a_lib.M42A	6C2 40C7
USB_B_OC_L	USB_B_OC_L - @m42a_lib.M42A	22C4 22D8
USB_B_P	USB_B_P - @m42a_lib.M42A	6C1 22C2
	=USB2_GEYSER_P - @m42a_lib.M42A	6C2 40C7
	USB2_GEYSER_P - @m42a_lib.M42A	6C2
	=USB2_GEYSER_P - @m42a_lib.M42A	6C2 40C7
USB_C_N	USB_C_N - @m42a_lib.M42A	6C1 22C2
	=USB2_EXTB_N - @m42a_lib.M42A	6C2 42B5
	USB2_EXTB_N - @m42a_lib.M42A	6C2
	=USB2_EXTB_N - @m42a_lib.M42A	6C2 42B5
USB_C_P	USB_C_P - @m42a_lib.M42A	6C1 22C2
	=USB2_EXTB_P - @m42a_lib.M42A	6C2 42B5
	USB2_EXTB_P - @m42a_lib.M42A	6C2
	=USB2_EXTB_P - @m42a_lib.M42A	6C2 42B5
USB_D_OC_L	USB_D_OC_L - @m42a_lib.M42A	22C4 22D8
USB_E_N	USB_E_N - @m42a_lib.M42A	6C1 22C2
	TP_USBN_E - @m42a_lib.M42A	5C1 6C2
USB_E_OC_L	USB_E_OC_L - @m42a_lib.M42A	22C4 22D8
USB_E_P	USB_E_P - @m42a_lib.M42A	6C1 22C2
	TP_USBP_E - @m42a_lib.M42A	5C1 6C2
USB_F_N	USB_F_N - @m42a_lib.M42A	6C1 22C2
	=USB2_IR_N - @m42a_lib.M42A	6C2 41C6
	USB_IR_N - @m42a_lib.M42A	6C2
	=USB2_IR_N - @m42a_lib.M42A	6C2 41C6
USB_F_P	USB_F_P - @m42a_lib.M42A	6C1 22C2
	=USB2_IR_P - @m42a_lib.M42A	6C2 41C6
	USB_IR_P - @m42a_lib.M42A	6C2
	=USB2_IR_P - @m42a_lib.M42A	6C2 41C6
USB_G_N	USB_G_N - @m42a_lib.M42A	6B1 22C2
	=USB2_BT_N - @m42a_lib.M42A	6B2 44C6
	USB_BT_N - @m42a_lib.M42A	6B2
	=USB2_BT_N - @m42a_lib.M42A	6B2 44C6
USB_G_P	USB_G_P - @m42a_lib.M42A	6B1 22C2
	=USB2_BT_P - @m42a_lib.M42A	6C2 44C6
	USB_BT_P - @m42a_lib.M42A	6C2
	=USB2_BT_P - @m42a_lib.M42A	6C2 44C6
USB_RBIAS_PN	USB_RBIAS_PN - @m42a_lib.M42A	22C2
VGA_B	VGA_B - @m42a_lib.M42A	69B4
VGA_G	VGA_G - @m42a_lib.M42A	69B4
VGA_HSYNC	VGA_HSYNC - @m42a_lib.M42A	69B4 69C1
VGA_R	VGA_R - @m42a_lib.M42A	69A4
VGA_VSYNC	VGA_VSYNC - @m42a_lib.M42A	69B4 69C1
VOL_DOWN	VOL_DOWN - @m42a_lib.M42A	54B7 54C7
VOL_UP	VOL_UP - @m42a_lib.M42A	54B7 54C7
VREG_FB	VREG_FB - @m42a_lib.M42A	54A4
VR_PWRGD_CK410	VR_PWRGD_CK410 - @m42a_lib.M42A	23C5 26A8
VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @m42a_lib.M42A	14B6 26B5 58C7
XDP_BPM_L<0>	XDP_BPM_L<0> - @m42a_lib.M42A	7C6 11B2
XDP_BPM_L<1>	XDP_BPM_L<1> - @m42a_lib.M42A	7C6 11B2
XDP_BPM_L<2>	XDP_BPM_L<2> - @m42a_lib.M42A	7C6 11B2
XDP_BPM_L<3>	XDP_BPM_L<3> - @m42a_lib.M42A	7C6 11B3
XDP_BPM_L<4>	XDP_BPM_L<4> - @m42a_lib.M42A	7C6 11B2
XDP_BPM_L<5>	XDP_BPM_L<5> - @m42a_lib.M42A	7C6 11B2
XDP_DBRESET_L	XDP_DBRESET_L - @m42a_lib.M42A	7C6 11B4 26C6
XDP_TCK	XDP_TCK - @m42a_lib.M42A	7A8 7C6 11B2 11B3
XDP_TDI	XDP_TDI - @m42a_lib.M42A	7B8 7C6 11B3
XDP_TDO	XDP_TDO - @m42a_lib.M42A	7C6 11B5

XDP_TMS	XDP_TMS - @m42a_lib.M42A	7B8 7C6 11B2
XDP_TRST_L	XDP_TRST_L - @m42a_lib.M42A	7C6 11B3

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C0608	CAP_402	m42a[6C7]
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C0901	CAP_805	m42a[9B6]
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C0929	CAP_805	m42a[9B4]
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C0937	CAP_402	m42a[9B6]
C0938	CAP_402	m42a[9B5]
C0939	CAP_805	m42a[9A4]
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C0941	CAP_P_3P_D2T	m42a[9A7]
C0942	CAP_P_3P_D2T	m42a[9A7]
C0943	CAP_P_3P_D2T	m42a[9A6]
C0944	CAP_P_3P_D2T	m42a[9A6]
C0946	CAP_P_3P_D2T	m42a[9A5]
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C0951	CAP_603	m42a[9D7]
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C1002	CAP_402	m42a[10C4]
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C1211	CAP_402	m42a[12C3]
C1226	CAP_402	m42a[12B6]
C1236	CAP_402	m42a[12A6]
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C1416	CAP_402	m42a[14C2]
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C1615	CAP_402	m42a[16B6]
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C1912	CAP_603	m42a[19B8]
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C1914	CAP_603	m42a[19B6]
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C1918	CAP_402	m42a[19B5]
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C1922	CAP_402	m42a[19A6]
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C1966	CAP_603	m42a[19B4]
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C1971	CAP_603	m42a[19A3]
C1972	CAP_603	m42a[19A3]
C1975	CAP_603	m42a[19A3]
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C1986	FILTER_3P_A_NFM18	m42a[19D2]
C1990	CAP_603	m42a[19C2]
C1991	CAP_402	m42a[19C2]
C1992	FILTER_3P_A_NFM18	m42a[19C2]
C1993	CAP_402	m42a[19B2]
C1994	FILTER_3P_A_NFM18	m42a[19B2]
C1995	CAP_402	m42a[19B2]
C1996	FILTER_3P_A_NFM18	m42a[19B2]
C1997	CAP_402	m42a[19A2]
C1998	FILTER_3P_A_NFM18	m42a[19A2]
C2500	CAP_P_SMB2	m42a[25B8]
C2501	CAP_402	m42a[25A6]
C2502	CAP_402	m42a[25D4]
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C3009	CAP_402	m42a[30C3]
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C3011	CAP_402	m42a[30C3]
C3012	CAP_402	m42a[30B4]
C3013	CAP_402	m42a[30B3]
C3014	CAP_402	m42a[30B4]
C3015	CAP_402	m42a[30B3]
C3016	CAP_402	m42a[30B4]
C3017	CAP_402	m42a[30B3]
C3018	CAP_402	m42a[30B4]
C3019	CAP_402	m42a[30B3]
C3020	CAP_402	m42a[30A4]
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C3024	CAP_402	m42a[30A4]
C3025	CAP_402	m42a[30A3]
C3100	CAP_402	m42a[31C4]
C3101	CAP_603	m42a[31B5]
C3102	CAP_603	m42a[31B3]
C3103	CAP_402	m42a[31B5]
C3104	CAP_603	m42a[31C4]
C3105	CAP_P_SMC-LF	m42a[31B4]
C3301	CAP_402	m42a[32D6]
C3302	CAP_402	m42a[32D6]
C3303	CAP_402	m42a[32D6]
C3304	CAP_402	m42a[32D6]
C3305	CAP_402	m42a[32D4]
C3306	CAP_402	m42a[32D4]
C3307	CAP_402	m42a[32C4]
C3308	CAP_402	m42a[32D4]
C3309	CAP_603	m42a[32D4]
C3310	CAP_402	m42a[32D3]
C3311	CAP_402	m42a[32C6]
C3312	CAP_603	m42a[32C6]
C3314	CAP_402	m42a[32D8]
C3315	CAP_402	m42a[32D7]
C3316	CAP_603	m42a[32D7]
C3317	CAP_603	m42a[32D4]
C3389	CAP_402	m42a[32C7]
C3390	CAP_402	m42a[32C7]
C3804	CAP_402	m42a[34B5]
C3805	CAP_402	m42a[34B3]
C3806	CAP_603	m42a[34B3]
C3875	CAP_402	m42a[34C7]
C3876	CAP_402	m42a[34C5]
C3900	CAP_402	m42a[35D6]
C3901	CAP_402	m42a[35D5]
C3902	CAP_402	m42a[35C6]
C3903	CAP_402	m42a[35D5]
C3920	CAP_402	m42a[35C7]
C3921	CAP_603	m42a[35C6]
C3922	CAP_402	m42a[35C5]
C3923	CAP_402	m42a[35C6]
C3950	CAP_603	m42a[35B8]
C4100	CAP_402	m42a[36D6]
C4101	CAP_402	m42a[36D6]
C4102	CAP_402	m42a[36D5]
C4103	CAP_402	m42a[36D5]
C4104	CAP_402	m42a[36D5]
C4105	CAP_402	m42a[36D5]
C4106	CAP_402	m42a[36D4]
C4107	CAP_402	m42a[36D4]
C4110	CAP_402	m42a[36D5]
C4111	CAP_402	m42a[36D5]
C4112	CAP_402	m42a[36C5]
C4113	CAP_402	m42a[36C5]
C4115	CAP_402	m42a[36B4]
C4116	CAP_402	m42a[36B4]
C4117	CAP_402	m42a[36B3]
C4118	CAP_402	m42a[36B3]
C4126	CAP_402	m42a[36A8]
C4127	CAP_402	m42a[36A8]
C4128	CAP_402	m42a[36A7]
C4129	CAP_402	m42a[36A7]
C4130	CAP_402	m42a[36A7]
C4131	CAP_402	m42a[36A6]
C4132	CAP_402	m42a[36A6]
C4133	CAP_402	m42a[36A6]
C4134	CAP_402	m42a[36A6]
C4135	CAP_402	m42a[36A5]
C4136	CAP_402	m42a[36A5]
C4137	CAP_402	m42a[36A4]
C4138	CAP_402	m42a[36A4]
C4139	CAP_402	m42a[36A4]
C4140	CAP_402	m42a[36B3]
C4150	CAP_402	m42a[36B6]
C4151	CAP_402	m42a[36B6]
C4200	CAP_402	m42a[37C7]
C4201	CAP_402	m42a[37C6]
C4202	CAP_402	m42a[37C6]
C4203	CAP_402	m42a[37C6]
C4204	CAP_402	m42a[37C7]
C4205	CAP_402	m42a[37C6]
C4206	CAP_402	m42a[37C6]
C4207	CAP_402	m42a[37C6]
C4210	CAP_1808	m42a[37A6]
C4211	CAP_402	m42a[37A6]
C4212	CAP_402	m42a[37A5]
C4411	CAP_402	m42a[38C2]
C4412	CAP_402	m42a[38C2]
C4416	CAP_603	m42a[38D4]
C4417	CAP_402	m42a[38D4]
C4418	CAP_402	m42a[38D4]
C4420	CAP_402	m42a[38C3]
C4422	CAP_402	m42a[38D4]
C4424	CAP_603	m42a[38D5]
C4425	CAP_402	m42a[38D3]
C4426	CAP_402	m42a[38D4]
C4428	CAP_402	m42a[38D3]
C4429	CAP_402	m42a[38D3]
C4430	CAP_402	m42a[38D3]
C4432	CAP_402	m42a[38D3]
C4500	CAP_402	m42a[39B5]
C4501	CAP_402	m42a[39A5]
C4519	CAP_402	m42a[39C3]
C4520	CAP_402	m42a[39B4]
C4521	CAP_402	m42a[39B3]
C4522	CAP_402	m42a[39A4]
C4523	CAP_402	m42a[39A3]
C4524	CAP_603-1	m42a[39A2]
C4525	CAP_402	m42a[39A2]
C4551	CAP_402	m42a[39A7]
C4552	CAP_402	m42a[39A7]
C4590	CAP_402	m42a[39C5]
C4900	CAP_402	m42a[40C4]
C4910	CAP_402	m42a[40C6]
C5100	CAP_402	m42a[41D6]
C5101	CAP_402	m42a[41D6]
C5102	CAP_402	m42a[41B5]
C5202	CAP_402	m42a[42C2]
C5203	CAP_402	m42a[42C2]
C5206	CAP_402	m42a[42B2]
C5207	CAP_402	m42a[42B2]
C5208	CAP_402	m42a[42C6]
C5209	CAP_402	m42a[42B6]
C5210	CAP_P_B2	m42a[42C6]
C5211	CAP_P_B2	m42a[42B6]
C5212	CAP_402	m42a[42C8]
C5213	CAP_603	m42a[42C8]
C5250	CAP_402	m42a[42C8]
C5251	CAP_402	m42a[42B8]
C5300	CAP_402	m42a[43B6]
C5301	CAP_402	m42a[43B6]
C5304	CAP_402	m42a[43D4]
C5305	CAP_402	m42a[43D4]
C5306	CAP_402	m42a[43D4]
C5307	CAP_402	m42a[43C4]
C5308	CAP_402	m42a[43C4]
C5309	CAP_603	m42a[43C3]
C5310	CAP_402	m42a[43C3]
C5498	CAP_402	m42a[44C5]
C5499	CAP_603	m42a[44C5]
C5802	CAP_805	m42a[45D3]
C5803	CAP_402	m42a[45D2]
C5804	CAP_402	m42a[45D2]
C5805	CAP_402	m42a[45D2]
C5806	CAP_402	m42a[45D1]
C5807	CAP_402	m42a[45D2]
C5820	CAP_402	m42a[45C3]
C5900	CAP_402	m42a[46D8]
C5901	CAP_402	m42a[46D8]
C5910	CAP_603	m42a[46A7]
C5911	CAP_402	m42a[46A7]
C5920	CAP_402	m42a[46C6]
C5921	CAP_402	m42a[46C6]
C5951	CAP_402	m42a[46A4]
C5965	CAP_402	m42a[46B8]
C5966	CAP_603	m42a[46B7]
C5967	CAP_402	m42a[46B7]
C5977	CAP_402	m42a[46C2]
C6100	CAP_402	m42a[48D3]
C6101	CAP_402	m42a[48C3]
C6102	CAP_402	m42a[48C2]
C6103	CAP_402	m42a[48C3]
C6104	CAP_402	m42a[48D4]
C6105	CAP_402	m42a[48C4]
C6112	CAP_402	m42a[48B2]
C6150	CAP_402	m42a[48C6]
C6200	CAP_402	m42a[49C5]
C6201	CAP_402	m42a[49C5]
C6202	CAP_402	m42a[49D4]
C6250	CAP_402	m42a[49B5]
C6251	CAP_402	m42a[49A5]
C6252	CAP_402	m42a[49B4]
C6301	CAP_402	m42a[50C2]
C6308	CAP_402	m42a[50C5]
C6309	CAP_402	m42a[50C6]
C6311	CAP_402	m42a[50C2]
C6312	CAP_402	m42a[50D3]
C6604	CAP_402	m42a[52B4]
C6605	CAP_402	m42a[52B4]
C6606	CAP_402	m42a[52B4]
C6620	CAP_402	m42a[52C4]
C6700	CAP_402	m42a[53C4]
C6701	CAP_402	m42a[53C4]
C6702	CAP_402	m42a[53C3]
C6703	CAP_402	m42a[53C3]
C6795	CAP_402	m42a[53C6]
C6796	CAP_402	m42a[53B6]
C6800	CAP_603	m42a[54D6]
C6801	CAP_402	m42a[54D6]
C6802	CAP_P_CASE-B3-LF	m42a[54D4]
C6803	CAP_P_CASE-B3-LF	m42a[54D3]
C6804	CAP_P_SMA-LF	m42a[54B4]
C6805	CAP_603	m42a[54B4]
C6806	CAP_603	m42a[54B3]
C6807	CAP_P_SMA-LF	m42a[54B3]
C6810	CAP_P_SMA-LF	m42a[54B2]
C6812	CAP_402	m42a[54B4]
C6813	CAP_402	m42a[54B3]
C6821	CAP_402	m42a[54C6]
C6822	CAP_603	m42a[54A5]
C6823	CAP_402	m42a[54A5]
C6825	CAP_402	m42a[54A4]
C6830	CAP_402	m42a[54D4]
C6833	CAP_402	m42a[54B2]
C6835	CAP_402	m42a[54D6]
C6836	CAP_402	m42a[54D3]
C6853	CAP_402	m42a[54B4]
C7200	CAP_P_SMC-LF	m42a[55D6]
C7201	CAP_P_CASE-B3-LF	m42a[55C4]
C7202	CAP_603	m42a[55C4]
C7203	CAP_P_CASE-B3-LF	m42a[55B4]
C7204	CAP_603	m42a[55B4]
C7205	CAP_P_CASE-B2	m42a[55B4]
C7206	CAP_603	m42a[55B4]
C7207	CAP_402	m42a[55C5]
C7208	CAP_402	m42a[55B5]
C7209	CAP_402	m42a[55A5]
C7210	CAP_402	m42a[55C6]
C7211	CAP_402	m42a[55C5]
C7220	CAP_402	m42a[55B6]
C7221	CAP_402	m42a[55B5]
C7230	CAP_402	m42a[55A6]
C7231	CAP_402	m42a[55A5]
C7260	CAP_402	m42a[55D2]
C7261	CAP_402	m42a[55C2]
C7270	CAP_402	m42a[55C2]
C7271	CAP_402	m42a[55B2]
C7280	CAP_402	m42a[55B2]
C7281	CAP_402	m42a[55B2]
C7300	CAP_402	m42a[56C7]
C7301	CAP_402	m42a[56C5]
C7302	CAP_402	m42a[56C5]
C7303	CAP_402	m42a[56C5]
C7304	CAP_402	m42a[56C5]
C7305	CAP_402	m42a[56C5]
C7306	CAP_402	m42a[56C8]
C7307	CAP_402	m42a[56C6]
C7308	CAP_402	m42a[56C6]
C7350	CAP_402	m42a[56A7]
C7351	CAP_603	m42a[56A7]
C7352	CAP_402	m42a[56A5]
C7353	CAP_402	m42a[56A5]
C7354	CAP_402	m42a[56A5]
C7355	CAP_402	m42a[56A5]
C7356	CAP_402	m42a[56A5]
C7357	CAP_402	m42a[56A8]
C7370	CAP_402	m42a[56A2]
C7371	CAP_402	m42a[56A2]
C7372	CAP_402	m42a[56A1]
C7400	CAP_402	m42a[57B4]
C7401	CAP_402	m42a[57D7]
C7402	CAP_402	m42a[57C7]
C7404	CAP_402	m42a[57C4]
C7411	CAP_402	m42a[57B7]
C7412	CAP_402	m42a[57B6]
C7414	CAP_402	m42a[57C4]
C7430	CAP_P_B2	m42a[57D2]
C7431	CAP_P_B2	m42a[57C2]
C7432	CAP_805-1	m42a[57B2]
C7433	CAP_805-1	m42a[57A2]
C7435	CAP_402	m42a[57B1]
C7440	CAP_402	m42a[57A4]
C7441	CAP_402	m42a[57A4]
C7445	CAP_402	m42a[57A3]
C7446	CAP_402	m42a[57A3]
C7447	CAP_402	m42a[57A3]
C7450	CAP_402	m42a[57A6]
C7451	CAP_402	m42a[57A7]
C7452	CAP_402	m42a[57A6]
C7500	CAP_402	m42a[58C4]
C7501	CAP_P_CASED2E-SM	m42a[58C3]
C7502	CAP_402	m42a[58B4]
C7503	CAP_402	m42a[58C2]
C7504	CAP_402	m42a[58B2]
C7505	CAP_402	m42a[58C8]
C7506	CAP_402	m42a[58B8]

C7507	CAP_402	m42a[58B7]
C7508	CAP_P_CASED2E-SM	m42a[58C3]
C7509	CAP_P_CASED2E-SM	m42a[58D3]
C7510	CAP_402	m42a[58C8]
C7511	CAP_402	m42a[58B3]
C7512	CAP_402	m42a[58C3]
C7513	CAP_402	m42a[58B7]
C7514	CAP_402	m42a[58B8]
C7515	CAP_402	m42a[58C5]
C7516	CAP_402	m42a[58B4]
C7517	CAP_P_CASED2E-SM	m42a[58D3]
C7518	CAP_603	m42a[58D2]
C7521	CAP_402	m42a[58A6]
C7526	CAP_603	m42a[58D7]
C7527	CAP_402	m42a[58C5]
C7528	CAP_402	m42a[58B5]
C7529	CAP_402	m42a[58B5]
C7530	CAP_402	m42a[58C7]
C7531	CAP_402	m42a[58B5]
C7532	CAP_402	m42a[58B6]
C7533	CAP_402	m42a[58B6]
C7534	CAP_402	m42a[58B5]
C7535	CAP_603	m42a[58B6]
C7590	CAP_402	m42a[58C3]
C7592	CAP_402	m42a[58B3]
C7596	CAP_402	m42a[58D7]
C7599	CAP_603	m42a[58C2]
C7600	CAP_603	m42a[59C4]
C7601	CAP_603	m42a[59A4]
C7602	CAP_402	m42a[59A4]
C7604	CAP_402	m42a[59A2]
C7605	CAP_402	m42a[59A5]
C7607	CAP_402	m42a[59A3]
C7608	CAP_402	m42a[59D2]
C7609	CAP_402	m42a[59D7]
C7621	CAP_402	m42a[59B6]
C7622	CAP_402	m42a[59C5]
C7624	CAP_402	m42a[59C6]
C7625	CAP_402	m42a[59B6]
C7626	CAP_402	m42a[59B6]
C7628	CAP_402	m42a[59B7]
C7629	CAP_402	m42a[59B7]
C7630	CAP_402	m42a[59B5]
C7631	CAP_402	m42a[59C7]
C7632	CAP_402	m42a[59C2]
C7640	CAP_P_CASED2E-SM	m42a[59D6]
C7641	CAP_603	m42a[59D6]
C7650	CAP_805	m42a[59B7]
C7651	CAP_805	m42a[59B8]
C7652	CAP_P_SMC-LF	m42a[59B8]
C7661	CAP_402	m42a[59B3]
C7662	CAP_402	m42a[59C4]
C7664	CAP_402	m42a[59C3]
C7665	CAP_402	m42a[59B4]
C7666	CAP_402	m42a[59B3]
C7668	CAP_402	m42a[59B2]
C7669	CAP_402	m42a[59B2]
C7670	CAP_402	m42a[59B4]
C7680	CAP_P_CASED2E-SM	m42a[59D3]
C7681	CAP_603	m42a[59D4]
C7689	CAP_402	m42a[59B4]
C7690	CAP_805	m42a[59B2]
C7691	CAP_805	m42a[59B1]
C7692	CAP_P_SMC-LF	m42a[59B1]
C7700	CAP_603	m42a[60C4]
C7701	CAP_402	m42a[60C3]
C7702	CAP_603	m42a[60C3]
C7703	CAP_603	m42a[60C4]
C7704	CAP_402	m42a[60C3]
C7705	CAP_603	m42a[60C3]
C7720	CAP_402	m42a[60B4]
C7721	CAP_603	m42a[60B3]
C7750	CAP_402	m42a[60C6]
C7800	CAP_603	m42a[61C5]
C7801	CAP_603	m42a[61C6]
C7802	CAP_603	m42a[61C5]
C7803	CAP_402	m42a[61B2]
C7804	CAP_402	m42a[61C2]
C7805	CAP_402	m42a[61C2]
C7806	CAP_402	m42a[61B7]
C7807	CAP_402	m42a[61B6]
C7808	CAP_402	m42a[61B6]
C7809	CAP_402	m42a[61C4]
C7810	CAP_402	m42a[61B4]
C7830	CAP_P_CASED2E-SM	m42a[61C4]
C7831	CAP_603	m42a[61C4]
C7840	CAP_805	m42a[61B3]
C7841	CAP_805	m42a[61B3]
C7842	CAP_P_CASE-D2E-LF	m42a[61B3]
C7843	CAP_P_CASE-D2E-LF	m42a[61B2]
C7864	CAP_402	m42a[61C2]
C7900	CAP_603	m42a[62C4]
C7901	CAP_603	m42a[62A4]
C7902	CAP_402	m42a[62A4]
C7903	CAP_402	m42a[62A6]
C7904	CAP_402	m42a[62A2]
C7905	CAP_402	m42a[62A5]
C7906	CAP_402	m42a[62A6]
C7907	CAP_402	m42a[62A3]
C7908	CAP_402	m42a[62D2]
C7909	CAP_402	m42a[62C7]
C7921	CAP_402	m42a[62B6]
C7922	CAP_402	m42a[62C5]
C7924	CAP_402	m42a[62C6]
C7925	CAP_402	m42a[62B6]
C7926	CAP_402	m42a[62B6]
C7928	CAP_402	m42a[62B7]
C7929	CAP_402	m42a[62B7]
C7930	CAP_402	m42a[62B5]
C7931	CAP_402	m42a[62C7]
C7932	CAP_402	m42a[62C2]
C7940	CAP_P_CASED2E-SM	m42a[62C6]
C7941	CAP_603	m42a[62C6]
C7950	CAP_805	m42a[62B8]
C7952	CAP_P_CASE-D2E-LF	m42a[62B8]
C7961	CAP_402	m42a[62B3]
C7962	CAP_402	m42a[62C4]
C7964	CAP_402	m42a[62C3]
C7965	CAP_402	m42a[62B3]
C7966	CAP_402	m42a[62B3]
C7968	CAP_402	m42a[62B2]
C7969	CAP_402	m42a[62B2]
C7970	CAP_402	m42a[62B4]
C7980	CAP_P_CASED2E-SM	m42a[62C4]

C7981	CAP_603	m42a[62C4]
C7989	CAP_402	m42a[62B4]
C7990	CAP_805	m42a[62A7]
C7991	CAP_805	m42a[62A7]
C7992	CAP_P_CASE-D2E-LF	m42a[62B1]
C7999	CAP_402	m42a[62A6]
C8000	CAP_402	m42a[63D4]
C8005	CAP_402	m42a[63C4]
C8010	CAP_402	m42a[63C4]
C8015	CAP_402	m42a[63B4]
C8025	CAP_402	m42a[63A4]
C8060	CAP_402	m42a[63B3]
C8061	CAP_402	m42a[63B2]
C8062	CAP_402	m42a[63B2]
C8090	CAP_1206-1	m42a[63C3]
C8091	CAP_402	m42a[63D2]
C8092	CAP_402	m42a[63D1]
C8093	CAP_805	m42a[63D1]
C8202	CAP_402	m42a[65D7]
C8203	CAP_402	m42a[65C7]
C8205	CAP_402	m42a[65A5]
C8206	CAP_402	m42a[65A4]
C8209	CAP_402	m42a[65A5]
C8211	CAP_402	m42a[65A5]
C8215	CAP_402	m42a[65A4]
C8217	CAP_603	m42a[65C2]
C8218	CAP_402	m42a[65C4]
C8220	CAP_402	m42a[65A7]
C8221	CAP_402	m42a[65A7]
C8230	CAP_402	m42a[65C6]
C8300	CAP_402	m42a[66C7]
C8301	CAP_402	m42a[66C7]
C8302	CAP_402	m42a[66C7]
C8303	CAP_402	m42a[66C4]
C8304	CAP_402	m42a[66C5]
C8305	CAP_1206-1	m42a[66C4]
C8306	CAP_1206-1	m42a[66C3]
C8307	CAP_1206-1	m42a[66C3]
C8308	CAP_P_CASED2E-SM	m42a[66B4]
C8309	CAP_P_6.3X5.5SM1	m42a[66B3]
C8310	CAP_P_CASED2E-SM	m42a[66B3]
C8311	CAP_402	m42a[66C7]
C8312	CAP_402	m42a[66C5]
C8313	CAP_402	m42a[66C6]
C8316	CAP_402	m42a[66B4]
C8317	CAP_402	m42a[66B5]
C8318	CAP_402	m42a[66B4]
C8320	CAP_402	m42a[66B5]
C8321	CAP_402	m42a[66B5]
C8322	CAP_402	m42a[66B4]
C8323	CAP_402	m42a[66A5]
C8324	CAP_402	m42a[66A4]
C8325	CAP_402	m42a[66C7]
C8326	CAP_402	m42a[66C7]
C8327	CAP_402	m42a[66D7]
C8328	CAP_402	m42a[66B6]
C8340	CAP_402	m42a[66C7]
C8341	CAP_402	m42a[66B8]
C8370	CAP_402	m42a[66C3]
C8371	CAP_402	m42a[66C2]
C8372	CAP_402	m42a[66B1]
C8375	CAP_402	m42a[66B3]
C8381	CAP_603	m42a[66B3]
C9400	CAP_402	m42a[67C3]
C9401	CAP_402	m42a[67C3]
C9402	CAP_402	m42a[67C3]
C9403	CAP_402	m42a[67C3]
C9408	CAP_402	m42a[67A3]
C9409	CAP_402	m42a[67B2]
C9410	CAP_402	m42a[67A3]
C9411	CAP_402	m42a[67B5]
C9412	CAP_603	m42a[67B5]
C9413	CAP_402	m42a[67B6]
C9414	CAP_402	m42a[67D5]
C9415	CAP_402	m42a[67A3]
C9416	CAP_402	m42a[67A4]
C9459	CAP_402	m42a[67C5]
C9500	CAP_402	m42a[68D5]
C9501	CAP_402	m42a[68D4]
C9502	CAP_402	m42a[68D4]
C9503	CAP_402	m42a[68D4]
C9504	CAP_603	m42a[68D4]
C9505	CAP_603	m42a[68B2]
C9506	CAP_402	m42a[68C7]
C9507	CAP_402	m42a[68D5]
C9508	CAP_402	m42a[68D5]
C9509	CAP_402	m42a[68D4]
C9510	CAP_402	m42a[68D4]
C9511	CAP_402	m42a[68D4]
C9512	CAP_402	m42a[68D3]
C9513	CAP_603	m42a[68D3]
C9514	CAP_402	m42a[68D7]
C9519	CAP_402	m42a[68B6]
C9520	CAP_402	m42a[68B6]
C9521	CAP_402	m42a[68B3]
C9522	CAP_402	m42a[68D2]
C9523	CAP_402	m42a[68D2]
C9524	CAP_402	m42a[68C2]
C9525	CAP_402	m42a[68C2]
C9526	CAP_402	m42a[68C3]
C9527	CAP_402	m42a[68C1]
C9530	CAP_402	m42a[68D7]
C9531	CAP_402	m42a[68D7]
C9532	CAP_402	m42a[68C7]
C9533	CAP_402	m42a[68C7]
C9534	CAP_402	m42a[68C7]
C9535	CAP_402	m42a[68C7]
C9536	CAP_402	m42a[68D7]
C9537	CAP_402	m42a[68D7]
C9538	CAP_402	m42a[68D7]
C9539	CAP_402	m42a[68D7]
C9540	CAP_603	m42a[68D6]
C9541	CAP_402	m42a[68B5]
C9542	CAP_402	m42a[68B5]
C9543	CAP_402	m42a[68B5]
C9544	CAP_402	m42a[68B5]
C9545	CAP_402	m42a[68B5]
C9546	CAP_402	m42a[68B4]
C9547	CAP_402	m42a[68B4]
C9548	CAP_402	m42a[68B4]
C9804	CAP_402	m42a[69C4]
C9808	CAP_402	m42a[69C5]
C9809	CAP_402	m42a[69B5]
C9812	CAP_402	m42a[69B5]

C9820	CAP_402	m42a[69A4]
C9821	CAP_402	m42a[69A3]
C9824	CAP_402	m42a[69B5]
C9834	CAP_402	m42a[69A4]
C9839	CAP_402	m42a[69B7]
C9842	CAP_402	m42a[69C1]
C9843	CAP_402	m42a[69C1]
C9860	CAP_402	m42a[69C2]
D1986	DIODE_SCHOT_6PB_SOT-363	m42a[19C2 19D2]
D2502	DIODE_SCHOT_6PB_SOT-363	m42a[25C8 25D8]
D2600	DIODE_SCHOT_6PB_SOT-363	m42a[26D5 26D5]
D4520	DIODE_DUAL_6P_SOT-363	m42a[39B4 39B3]
D4521	DIODE_DUAL_6P_SOT-363	m42a[39A4 39A3]
D4550	ZENER_SOT23	m42a[39A6]
D4590	DIODE_SCHOT_SMB	m42a[39D4]
D4591	DPAK3P_SOT-363	m42a[39C5 39C5 39C5]
D4900	DIODE_SCHOT_3P_A_SC-75	m42a[40C6]
D5200	DIODE_SCHOT_3P_A_SC-75	m42a[42C3]
D5201	DIODE_SCHOT_3P_A_SC-75	m42a[42A3]
D7500	DIODE_SCHOT_SMB	m42a[58C3]
D7501	DIODE_SCHOT_SMB	m42a[58B3]
D7624	DIODE_SCHOT_SOD-323	m42a[59C6]
D7664	DIODE_SCHOT_SOD-323	m42a[59C3]
D7820	DIODE_SCHOT_SMB	m42a[61B4]
D7921	DIODE_SMB	m42a[62B7]
D7924	DIODE_SCHOT_SOD-323	m42a[62C6]
D7961	DIODE_SMB	m42a[62B2]
D7964	DIODE_SCHOT_SOD-323	m42a[62C3]
D8200	DIODE_SCHOT_3P_A_SC-75	m42a[65C7]
D8201	DPAK3P_SOT-363	m42a[65D4]
D8201	DPAK3P_SOT-363	m42a[66B3]
D8300	DIODE_SCHOT_SOD-123	m42a[66C5]
D8322	DPAK3P_SOT-363	m42a[66C8 66A5 66A6]
D9500	DIODE_DUAL_6P_SOT-363	m42a[68A7 68B7]
DZ7300	SUPPR_TRANSIENT_4P1_0405	m42a[56C6]
DZ7301	SUPPR_TRANSIENT_4P1_0405	m42a[56C6]
DZ7350	SUPPR_TRANSIENT_4P1_0405	m42a[56A6]
DZ7351	SUPPR_TRANSIENT_4P1_0405	m42a[56A6]
F8200	FUSE_1206	m42a[65D6]
F8300	FUSE_1206	m42a[66C3]
F9804	FUSE_SM-LF	m42a[69C5]
FL4520	FILTER_4P_2012	m42a[39B3]
FL4521	FILTER_4P_2012	m42a[39B3]
FL4590	FUSE_MINISMDC	m42a[39D5]
FL9800	FILTER_LC_SM-220MHZ-LF	m42a[69B5]
FL9801	FILTER_LC_SM-220MHZ-LF	m42a[69A5]
FL9802	FILTER_LC_SM-220MHZ-LF	m42a[69A5]
GV3901	HOLE_VIA	m42a[35C2]
GV3902	HOLE_VIA	m42a[35C2]
GV3903	HOLE_VIA	m42a[35C2]
GV3904	HOLE_VIA	m42a[35C2]
GV3905	HOLE_VIA	m42a[35B2]
GV3906	HOLE_VIA	m42a[35B2]
GV3907	HOLE_VIA	m42a[35B2]
GV3908	HOLE_VIA	m42a[35B2]
J1102	CON_F30STSM_5047_SM1	m42a[11B2]
J2600	CON_F2RT_S2MT_SM_F-RT-SM	m42a[26D6]
J2801	CON_F200RT_DDR2DIMM_TH1_F-RT-TH2	m42a[28D6]
J2901	CON_F200RT_DDR2DIMM_TH1_F-RT-TH2	m42a[29D5]
J3801	CON_M50ST_D2MT_SM_M-ST-SM	m42a[34C4]
J3901	CON_F19ST_S2MT_SM_F-ST-SM	m42a[35D8]
J4200	CON_RJ45_8RT_S2MT_SM_F-RT-SM	m42a[37C2]
J4500	CON_F6RT_S2MT_TH_F-RT-TH1	m42a[39B2]
J4900	CON_F10ST_D_SMA_F-ST-SM	m42a[40C4]
J5200	CON_F4RT_USB_S2MT_TH_F-RT-TH-M42	m42a[42D1]
J5201	CON_F4RT_USB_S2MT_TH_F-RT-TH-M42	m42a[42B1]
J5300	CON_F52RT_D2MT_SM_F-ST-SM	m42a[43C5]
J5400	CON_F4ST_S2MT_SM_F-ST-SM	m42a[44C4]
J6000	CON_F30STSM_5047_SM1	m42a[47C6]
J6250	CON_F2ST_S2MT_SM_F-ST-SM	m42a[49C6]
J6251	CON_F2ST_S2MT_SM_F-ST-SM	m42a[49A6]
J6501	CON_F4ST_S2MT_SM_F-ST-SM	m42a[51C3]
J7300	CON_F8RT_2MT_AUDIOUT_TH_F-RT-TH	m42a[56C8]
J7301	CON_M3RT_S2MT_SM_M-ST-SM1	m42a[56D1]
J7302	CON_F2ST_S2MT_SM_F-ST-SM	m42a[56D1]
J7303	CON_F4ST_S2MT_SM_F-ST-SM	m42a[56C1]
J7350	CON_F8RT_2MT_AUDIOIN_TH_F-RT-TH	m42a[56B8]
J8200	CON_M5RT_S_SM_M-RT-SM	m42a[65D7]
J8250	CON_F20ST_D_SM_F-ST-SM1	m42a[65B6]
J9400	CON_F4ST_S2MT_SM_F-ST-SM	m42a[67D2]
J9401	CON_F22RT_S4MT_SM_F-RT-SM	m42a[67B1]
J9801	CON_DVI_30RT_Q4MT_TH_1_RT-TH	m42a[69B4]

L1922	IND_0603	m42a[19A7]
L1934	IND_0603	m42a[19C5]
L1936	IND_0603	m42a[19C5]
L1970	IND_1210	m42a[19B4]
L1975	IND_0805	m42a[19A4]
L1985	IND_0603	m42a[19D3]
L1990	IND_0603	m42a[19C3]
L2500	IND_SM-3	m42a[25B8]
L2507	IND_1206	m42a[25A7]
L3301	IND_0402-LF	m42a[32D7]
L3302	IND_0402-LF	m42a[32D3]
L3901	FILTER_4P_2012H	m42a[35D6]
L3902	FILTER_4P_2012H	m42a[35D5]
L3912	IND_0402	m42a[35C6]
L4100	IND_0402-LF	m42a[36D3]
L4250	IND_0402-LF	m42a[37D7]
L4400	IND_0402	m42a[38D4]
L4510	IND_SM	m42a[39C3]
L4550	IND_SM-1	m42a[39A7]
L4900	IND_0402	m42a[40D5]
L4901	FILTER_4P_SM	m42a[40C6]
L4902	IND_0402	m42a[40C5]
L5200	FILTER_4P_SM	m42a[42C4]
L5201	FILTER_4P_SM	m42a[42B4]
L5202	IND_0402-LF	m42a[42D4]
L5203	IND_0402-LF	m42a[42C4]
L5204	IND_0402-LF	m42a[42C3]
L5205	IND_0402-LF	m42a[42A3]
L5400	FILTER_4P_SM	m42a[44B5]
L5410	IND_0402-LF	m42a[44C5]
L5411	IND_0402-LF	m42a[44B5]
L5910	IND_0603	m42a[46A7]
L6800	IND_0402	m42a[54A5]
L6801	IND_0402	m42a[54D6]
L7200	IND_0402	m42a[55C7]
L7210	IND_0402	m42a[55C7]
L7211	IND_0402	m42a[55A7]
L7220	IND_0402	m42a[55B7]
L7230	IND_0402	m42a[55A7]
L7300	IND_0402-LF	m42a[56D6]
L7301	IND_0402-LF	m42a[56D4]
L7302	IND_0402	m42a[56D6]
L7303	IND_0402	m42a[56C6]
L7304	IND_0402	m42a[56C4]
L7305	IND_0402	m42a[56C6]
L7306	IND_0402	m42a[56C4]
L7307	IND_0402	m42a[56C6]
L7350	IND_0402	m42a[56B6]
L7351	IND_0402	m42a[56B4]
L7352	IND_0402	m42a[56B6]
L7353	IND_0402	m42a[56B6]
L7354	IND_0402	m42a[56B4]
L7355	IND_0402	m42a[56B6]
L7356	IND_0402	m42a[56B4]
L7357	IND_0402	m42a[56A6]
L7370	IND_0402	m42a[56B2]
L7371	IND_0402	m42a[56B1]
L7372	IND_0402	m42a[56B2]
L7373	IND_0402	m42a[56B1]
L7374	IND_0402	m42a[56B2]
L7375	IND_0402	m42a[56B1]
L7390	IND_0402	m42a[56D8]
L7400	IND_0402	m42a[57B4]
L7500	IND_SM	m42a[58D2]
L7501	IND_SM	m42a[58B2]
L7620	IND_L812HW	m42a[59B7]
L7680	IND_SM	m42a[59B2]
L7820	IND_3P_SM	m42a[61B3]
L7920	IND_SM	m42a[62B7]
L7960	IND_3P_SM	m42a[62B2]
L8090	IND_CDPH4D19F-SM	m42a[63D1]
L8201	IND_SM-LF	m42a[65A3]
L8202	IND_0402-LF	m42a[65A3]
L8203	IND_0402-LF	m42a[65A3]
L8204	IND_0402-LF	m42a[65A3]
L8205	IND_SM-LF	m42a[65A3]
L8207	IND_0402	m42a[65A7]
L8208	IND_0402	m42a[65A7]
L8209	IND_0402	m42a[65A7]
L8300	IND_3P_SM	m42a[66C4]
L9400	IND_0402-LF	m42a[67D4]
L9401	IND_0402-LF	m42a[67C4]
L9402	IND_0402-LF	m42a[67D4]
L9403	IND_0402-LF	m42a[67D4]
L9404	IND_0402-LF	m42a[67B4]
L9405	IND_0402-LF	m42a[67A4]
L9407	FILTER_4P_SM	m42a[67A4]
L9408	IND_0402-LF	m42a[67B4]
L9500	IND_0402-LF	m42a[68D5]
L9501	IND_0402-LF	m42a[68D5]
L9503	IND_0402-LF	m42a[68D8]
L9504	IND_0402-LF	m42a[68C8]
L9505	IND_0402-LF	m42a[68C8]
L9506	IND_0402-LF	m42a[68D8]
L9804	FILTER_4P_SM1	m42a[69A2]
L9805	FILTER_4P_2012H	m42a[69B2]
L9806	FILTER_4P_2012H	m42a[69B2]
L9807	FILTER_4P_2012H	m42a[69B2]
L9844	IND_SM-1	m42a[69C4]
Q2680	TRA_SINGLE_MOSFET_NC_SOT23	m42a[26A3]
Q3810	TRA_FDC638P_SM-LF	m42a[34C5]
Q3875	TRA_2N7002DW_SOT-363	m42a[34C6 34C7]
Q4590	TRA_FDC638P_SM-LF	m42a[39D5]
Q4591	TRA_2N7002_SOT23-LF	m42a[39C5]
Q5901	TRA_2N7002DW_SOT-363	m42a[46B4 46B5]
Q5950	TRA_2N3906_SOT23-LF	m42a[46A3]
Q5952	TRA_2N7002_SOT23-LF	m42a[46A3]
Q6100	TRA_SI3446DV_TSOP-LF	m42a[48A5]
Q6101	TRA_2N7002DW_SOT-363	m42a[48A6 48A7]
Q6150	TRA_TP0610_SOT23-3	m42a[48C6]
Q6151	TRA_2N7002_SOT23-LF	m42a[48C7]
Q6152	TRA_TP0610_SOT23-3	m42a[48C7]
Q6153	TRA_TP0610_SOT23-3	m42a[48C8]
Q6200	TRA_BC846BM3T5G_NPN_SOT732-3	m42a[49B6]
Q6560	TRA_2N7002_SOT23-LF	m42a[51B3]
Q6650	TRA_2N7002_SOT23-LF	m42a[52B6]
Q6651	TRA_TP0610_SOT23-3	m42a[52B6]
Q7400	TRA_2N7002DW_SOT-363	m42a[57C7 57D7]
Q7401	TRA_2N7002DW_SOT-363	m42a[57D5 57D6]
Q7402	TRA_2N7002DW_SOT-363	m42a[57B7 57C5]
Q7500	TRA_HAT2168H_LFPAK	m42a[58D3]
Q7501	TRA_HAT2165H_LFPAK	m42a[58D4]

Q7502	TRA_HAT2168H_LFPAK	m42a[58C3]
Q7503	TRA_HAT2165H_LFPAK	m42a[58B4]
Q7504	TRA_HAT2165H_LFPAK	m42a[58D3]
Q7505	TRA_HAT2165H_LFPAK	m42a[58B3]
Q7620	TRA_STL8NH3LL_COMBO_PWRFLT-3P3X3P3	m42a[59C7]
Q7621	TRA_STL8NH3LL_COMBO_PWRFLT-3P3X3P3	m42a[59B7]
Q7660	TRA_STL8NH3LL_COMBO_PWRFLT-3P3X3P3	m42a[59C3]
Q7661	TRA_STL8NH3LL_COMBO_PWRFLT-3P3X3P3	m42a[59B3]
Q7750	TRA_2N7002DW_SOT-363	m42a[60C6 60C7]
Q7820	TRA_IRF7821_SO-8	m42a[61C4]
Q7821	TRA_IRF7832_SO-8	m42a[61B4]
Q7920	TRA_IRF7821_SO-8	m42a[62C6]
Q7921	TRA_IRF7832_SO-8	m42a[62B6]
Q7960	TRA_IRF7821_SO-8	m42a[62C3]
Q7961	TRA_IRF7832_SO-8	m42a[62B3]
Q8000	TRA_FDC638P_SM-LF	m42a[63D4]
Q8005	TRA_STL8NH3LL_COMBO_PWRFLT-3P3X3P3	m42a[63C4]
Q8010	TRA_FDC638P_SM-LF	m42a[63D4]
Q8015	TRA_STL8NH3LL_COMBO_PWRFLT-3P3X3P3	m42a[63C4]
Q8025	TRA_SI3447BDV_SOT-6	m42a[63A4]
Q8030	TRA_2N7002DW_SOT-363	m42a[63A6 63B6]
Q8031	TRA_2N7002DW_SOT-363	m42a[63D6 63A6]
Q8059	TRA_2N7002DW_SOT-363	m42a[63C7 63C7]
Q8060	TRA_2N7002_SOT23-LF	m42a[63C8]
Q8061	TRA_2N7002DW_SOT-363	m42a[63B7 63B7]
Q8062	TRA_2N7002_SOT23-LF	m42a[63B8]
Q8063	TRA_2N7002_SOT23-LF	m42a[63B4]
Q8210	TRA_2N7002DW_SOT-363	m42a[65C6 65C3]
Q8220	TRA_2N7002DW_SOT-363	m42a[65C7 65C6]
Q8240	TRA_TP0610_SOT23-3	m42a[65C5]
Q8250	TRA_SI4405DY_SO-8	m42a[65D2]
Q8298	TRA_TP0610_SOT23-3	m42a[65C7]
Q8299	TRA_2N7002_SOT23-LF	m42a[65C7]
Q8300	TRA_SI4405DY_SO-8	m42a[66D5]
Q8301	TRA_HAT2168H_LFPAK	m42a[66C4]
Q8302	TRA_HAT2165H_LFPAK	m42a[66B4]
Q8320	TRA_SI4405DY_SO-8	m42a[66B3]
Q8321	TRA_SI4405DY_SO-8	m42a[66B3]
Q8322	TRA_2N7002DW_SOT-363	m42a[66A4 66A4]
Q8324	TRA_2N7002DW_SOT-363	m42a[66A3 66A4]
Q8340	TRA_IRLML5203_SM	m42a[66C8]
Q8350	TRA_2N7002_SOT23-LF	m42a[66A6]
Q9403	TRA_FDC638P_SM-LF	m42a[67B6]
Q9404	TRA_2N7002_SOT23-LF	m42a[67B7]
Q9405	TRA_TP0610_SOT23-3	m42a[67D5]
Q9406	TRA_2N7002_SOT23-LF	m42a[67D6]
Q9801	TRA_2N7002DW_SOT-363	m42a[69D6 69D6]
R0610	RES_402	m42a[6A7]
R0611	RES_402	m42a[6A8]
R0612	RES_402	m42a[6A8]
R0621	RES_402	m42a[6A7]
R0702	RES_402	m42a[7D5]
R0703	RES_402	m42a[7C5]
R0704	RES_402	m42a[7C5]
R0705	RES_402	m42a[7B4]
R0706	RES_402	m42a[7B4]
R0707	RES_402	m42a[7A4]
R0712	RES_402	m42a[7A4]
R0716	RES_402	m42a[7B2]
R0717	RES_402	m42a[7B2]
R0718	RES_402	m42a[7B2]
R0719	RES_402	m42a[7B2]
R0720	RES_402	m42a[7B7]
R0721	RES_402	m42a[7B7]
R0722	RES_402	m42a[7A7]
R0730	RES_402	m42a[7A4]
R0802	RES_402	m42a[8B6]
R0803	RES_402	m42a[8A7]
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R0923	RES_402	m42a[9C2]
R0924	RES_402	m42a[9C2]
R0925	RES_402	m42a[9C2]
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R1002	RES_402	m42a[10B6]
R1005	RES_402	m42a[10C4]
R1006	RES_402	m42a[10C3]
R1100	RES_402	m42a[11B5]
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R1102	RES_402	m42a[11B4]
R1103	RES_402	m42a[11C5]
R1104	RES_402	m42a[11B5]
R1106	RES_402	m42a[11A3]
R1210	RES_402	m42a[12C3]
R1211	RES_402	m42a[12C3]
R1220	RES_402	m42a[12B7]
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R1225	RES_402	m42a[12B7]
R1226	RES_402	m42a[12B7]
R1230	RES_402	m42a[12A7]
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R1236	RES_402	m42a[12A7]
R1310	RES_402	m42a[13D3]
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R1440	RES_402	m42a[14D6]
R1441	RES_402	m42a[14D6]
R1950	RES_402	m42a[19D5]
R1951	RES_402	m42a[19D5]
R1975	RES_402	m42a[19A4]
R1985	RES_402	m42a[19D3]
R1986	RES_402	m42a[19C6]
R1987	RES_402	m42a[19C6]
R1988	RES_402	m42a[19C7]
R1989	RES_402	m42a[19C7]
R1990	RES_402	m42a[19C3]
R2058	RES_402	m42a[20B4]
R2059	RES_402	m42a[20B4]
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R2105	RES_402	m42a[21D6]
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R2195	RES_402	m42a[21C6]
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R2255	RES_402	m42a[22D7]
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R2300	RES_402	m42a[23C7]
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R2303	RES_402	m42a[23D3]
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R2327	RES_402	m42a[23D6]
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R2389	RES_402	m42a[23A4]
R2390	RES_402	m42a[23B3]
R2395	RES_402	m42a[23D7]
R2396	RES_402	m42a[23D6]
R2397	RES_402	m42a[23D6]
R2398	RES_402	m42a[23D8]
R2399	RES_402	m42a[23C1]
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R2612	RES_402	m42a[26A5]
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R2636	RES_402	m42a[26C2]
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R2697	RES_402	m42a[26C5]
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R2783	RES_402	m42a[27B2]
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R3035	RES_402	m42a[30B4]
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R3300	RES_402	m42a[32B6]
R3301	RES_402	m42a[32B7]
R3302	RES_402	m42a[32D4]
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R3304	RES_402	m42a[32C7]
R3400	RES_402	m42a[33C1]
R3401	RES_402	m42a[33C7]
R3402	RES_402	m42a[33C1]
R3403	RES_402	m42a[33C1]
R3404	RES_402	m42a[33D1]
R3405	RES_402	m42a[33C1]
R3406	RES_402	m42a[33B1]
R3407	RES_402	m42a[33B1]
R3408	RES_402	m42a[33C1]
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R3478	RES_402	m42a[33B4]
R3480	RES_402	m42a[33C7]
R3481	RES_402	m42a[33B1]
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R3490	RES_402	m42a[33A4]
R3824	RES_402	m42a[34C4]
R3825	RES_402	m42a[34C5]
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R3865	RES_402	m42a[34C6]
R3876	RES_402	m42a[34C7]
R3877	RES_402	m42a[34C6]
R3900	RES_402	m42a[35D3]
R3901	RES_402	m42a[35C3]
R3950	RES_402	m42a[35B7]
R4101	RES_402	m42a[36D8]
R4102	RES_402	m42a[36C8]
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R4104	RES_402	m42a[36B4]
R4105	RES_402	m42a[36B4]
R4106	RES_402	m42a[36B5]
R4107	RES_402	m42a[36D8]
R4117	RES_402	m42a[36B3]
R4118	RES_402	m42a[36B3]
R4119	RES_402	m42a[36B3]
R4120	RES_402	m42a[36B4]
R4122	RES_402	m42a[36A3]
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R4124	RES_402	m42a[36A2]
R4130	RES_402	m42a[36B6]
R4131	RES_402	m42a[36B6]
R4200	RES_402	m42a[37A6]
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R4203	RES_402	m42a[37A5]
R4400	RES_402	m42a[38C3]
R4420	RES_402	m42a[38C2]
R4431	RES_402	m42a[38A6]
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R4452	RES_402	m42a[38C3]
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R4550	RES_402	m42a[39A7]
R4590	RES_402	m42a[39C5]
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R5250	RES_402	m42a[42C8]
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R5303	RES_402	m42a[43C4]
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R5898	RES_402	m42a[45C2]
R5899	RES_402	m42a[45D3]
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R5910	RES_603	m42a[46C8]
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R5998	RES_402	m42a[46C4]
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R6704	RES_805	m42a[53C2]
R6705	RES_805	m42a[53C3]
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R6802	RES_402	m42a[54A5]
R6807	RES_402	m42a[54D7]
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R7261	RES_402	m42a[55C2]
R7270	RES_402	m42a[55C2]
R7271	RES_402	m42a[55C2]
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R7322	RES_402	m42a[56B7]
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R7382	RES_402	m42a[56B2]
R7391	RES_402	m42a[56C7]
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R7403	RES_402	m42a[57C7]
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R7405	RES_402	m42a[57D5]
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R7411	RES_402	m42a[57C8]
R7412	RES_402	m42a[57B7]
R7413	RES_402	m42a[57C6]
R7414	RES_402	m42a[57C4]
R7415	RES_402	m42a[57C5]
R7430	RES_603	m42a[57C3]
R7431	RES_603	m42a[57B3]
R7432	RES_402	m42a[57B3]
R7433	RES_402	m42a[57A3]
R7434	RES_402	m42a[57C2]
R7435	RES_402	m42a[57C2]
R7436	RES_402	m42a[57B2]
R7437	RES_402	m42a[57B2]
R7438	RES_402	m42a[57C2]
R7439	RES_402	m42a[57B2]
R7440	RES_402	m42a[57A5]
R7450	RES_402	m42a[57A7]
R7451	RES_402	m42a[57A7]
R7452	RES_402	m42a[57A7]
R7453	RES_402	m42a[57A7]
R7454	RES_402	m42a[57A7]
R7460	RES_402	m42a[57C6]
R7461	RES_402	m42a[57C7]
R7500	RES_402	m42a[58C2]
R7501	RES_402	m42a[58C2]
R7502	RES_805	m42a[58B3]
R7503	RES_805	m42a[58D3]
R7504	RES_402	m42a[58C1]
R7505	RES_402	m42a[58B2]
R7506	RES_402	m42a[58C7]
R7507	RES_402	m42a[58B1]
R7508	RES_402	m42a[58B8]
R7509	RES_402	m42a[58B8]
R7510	RES_402	m42a[58B6]
R7511	RES_402	m42a[58B8]
R7512	RES_402	m42a[58D7]
R7513	RES_402	m42a[58B7]
R7514	RES_402	m42a[58B8]
R7515	RES_402	m42a[58B5]
R7516	RES_402	m42a[58B4]
R7517	RES_402	m42a[58B5]
R7518	RES_402	m42a[58B5]
R7519	RES_402	m42a[58C7]
R7520	RES_402	m42a[58D7]
R7521	RES_402	m42a[58D8]
R7522	RES_402	m42a[58A5]
R7523	RES_402	m42a[58A6]
R7524	RES_402	m42a[58D5]
R7525	RES_402	m42a[58C5]
R7526	THERMISTER_402	m42a[58C7]
R7527	RES_402	m42a[58C8]
R7530	RES_402	m42a[58B4]
R7531	THERMISTER_0603-LF	m42a[58B4]
R7543	RES_402	m42a[58B2]
R7545	RES_402	m42a[58C7]
R7600	RES_402	m42a[59C5]
R7603	RES_402	m42a[59A3]
R7604	RES_402	m42a[59A3]
R7606	RES_402	m42a[59A3]
R7607	RES_402	m42a[59A3]
R7621	RES_402	m42a[59C7]
R7624	RES_402	m42a[59C6]
R7625	RES_402	m42a[59B6]
R7626	RES_402	m42a[59C7]
R7627	RES_402	m42a[59B7]
R7628	RES_402	m42a[59B7]
R7629	RES_402	m42a[59C7]
R7630	RES_402	m42a[59C5]
R7661	RES_402	m42a[59C2]
R7664	RES_402	m42a[59C3]
R7665	RES_402	m42a[59B4]
R7666	RES_402	m42a[59C2]
R7667	RES_402	m42a[59B2]
R7668	RES_402	m42a[59B2]
R7669	RES_402	m42a[59C2]
R7670	RES_402	m42a[59C4]
R7720	RES_402	m42a[60B3]
R7721	RES_402	m42a[60A3]
R7750	RES_402	m42a[60C6]
R7751	RES_402	m42a[60C7]
R7752	RES_402	m42a[60C7]
R7753	RES_402	m42a[60B7]
R7800	RES_402	m42a[61C4]
R7801	RES_402	m42a[61B2]
R7802	RES_1206	m42a[61C3]
R7803	RES_402	m42a[61C2]
R7804	RES_402	m42a[61C7]
R7805	RES_402	m42a[61B7]
R7806	RES_402	m42a[61B7]
R7807	RES_402	m42a[61C5]
R7808	RES_402	m42a[61B6]
R7810	RES_402	m42a[61B4]
R7821	RES_402	m42a[61B2]
R7822	RES_402	m42a[61B2]
R7860	RES_603	m42a[61C3]
R7861	RES_402	m42a[61C2]
R7863	RES_402	m42a[61C2]
R7900	RES_402	m42a[62C5]
R7901	RES_402	m42a[62B1]
R7902	RES_1206	m42a[62A7]

R7903	RES_402	m42a[62A3]
R7904	RES_402	m42a[62A3]
R7905	RES_402	m42a[62A6]
R7906	RES_402	m42a[62A3]
R7907	RES_402	m42a[62A3]
R7921	RES_402	m42a[62C7]
R7924	RES_402	m42a[62C6]
R7925	RES_402	m42a[62B6]
R7926	RES_402	m42a[62C7]
R7927	RES_402	m42a[62B8]
R7928	RES_402	m42a[62B8]
R7929	RES_402	m42a[62C7]
R7930	RES_402	m42a[62C5]
R7961	RES_402	m42a[62C2]
R7964	RES_402	m42a[62C3]
R7965	RES_402	m42a[62B3]
R7966	RES_402	m42a[62C2]
R7967	RES_402	m42a[62B2]
R7968	RES_402	m42a[62B2]
R7969	RES_402	m42a[62C2]
R7970	RES_402	m42a[62C4]
R7990	RES_402	m42a[62A6]
R7991	RES_402	m42a[62A6]
R7992	RES_603	m42a[62A7]
R8000	RES_402	m42a[63D5]
R8005	RES_402	m42a[63C5]
R8010	RES_402	m42a[63C5]
R8015	RES_402	m42a[63B5]
R8025	RES_402	m42a[63A5]
R8030	RES_402	m42a[63B6]
R8031	RES_402	m42a[63B6]
R8032	RES_402	m42a[63D6]
R8033	RES_402	m42a[63D6]
R8050	RES_402	m42a[63A6]
R8056	RES_402	m42a[63C8]
R8057	RES_402	m42a[63C8]
R8058	RES_402	m42a[63B8]
R8059	RES_402	m42a[63B8]
R8061	RES_402	m42a[63B1]
R8062	RES_402	m42a[63B1]
R8063	RES_402	m42a[63A1]
R8064	RES_402	m42a[63A1]
R8065	RES_402	m42a[63B2]
R8091	RES_402	m42a[63D1]
R8092	RES_402	m42a[63C1]
R8200	RES_402	m42a[65B7]
R8201	RES_402	m42a[65C5]
R8202	RES_402	m42a[65C5]
R8203	RES_402	m42a[65C6]
R8204	RES_402	m42a[65C6]
R8205	RES_805	m42a[65D4]
R8206	RES_402	m42a[65C4]
R8207	RES_402	m42a[65C4]
R8208	RES_402	m42a[65C4]
R8209	RES_402	m42a[65C4]
R8210	RES_402	m42a[65C4]
R8211	RES_402	m42a[65C6]
R8213	RES_402	m42a[65C2]
R8214	RES_402	m42a[65C2]
R8231	RES_402	m42a[65C5]
R8232	RES_402	m42a[65C6]
R8233	RES_402	m42a[65C5]
R8296	RES_402	m42a[65B7]
R8297	RES_402	m42a[65C3]
R8298	RES_402	m42a[65C8]
R8299	RES_402	m42a[65C7]
R8300	RES_402	m42a[66C6]
R8301	RES_402	m42a[66C7]
R8302	RES_402	m42a[66C5]
R8303	RES_402	m42a[66C5]
R8304	RES_805	m42a[66B2]
R8305	RES_402	m42a[66C5]
R8306	RES_402	m42a[66C7]
R8308	RES_0612	m42a[66C3]
R8309	RES_402	m42a[66B6]
R8310	RES_402	m42a[66C5]
R8311	RES_402	m42a[66B7]
R8312	RES_402	m42a[66C7]
R8320	RES_2525	m42a[66B3]
R8322	RES_402	m42a[66A3]
R8323	RES_402	m42a[66A3]
R8324	RES_402	m42a[66A4]
R8325	RES_402	m42a[66A5]
R8330	RES_402	m42a[66B4]
R8331	RES_402	m42a[66A4]
R8340	RES_402	m42a[66C8]
R8341	RES_402	m42a[66B8]
R8342	RES_402	m42a[66C8]
R8343	RES_402	m42a[66B8]
R8344	RES_402	m42a[66B8]
R8350	RES_402	m42a[66B5]
R8351	RES_402	m42a[66B6]
R8352	RES_402	m42a[66B5]
R8360	RES_402	m42a[66D7]
R8361	RES_402	m42a[66C7]
R8362	RES_402	m42a[66B7]
R8363	RES_402	m42a[66B6]
R8364	RES_402	m42a[66B6]
R8365	RES_402	m42a[66B6]
R8367	RES_402	m42a[66C6]
R8370	RES_402	m42a[66C2]
R8371	RES_402	m42a[66B2]
R8381	RES_603	m42a[66B4]
R8397	RES_0612	m42a[66C4]
R9400	RES_402	m42a[67D6]
R9401	RES_402	m42a[67D6]
R9402	RES_402	m42a[67C7]
R9408	RES_402	m42a[67B5]
R9409	RES_402	m42a[67B5]
R9413	RES_402	m42a[67A6]
R9414	RES_402	m42a[67B7]
R9415	RES_402	m42a[67B7]
R9416	RES_402	m42a[67B7]
R9423	RES_402	m42a[67B6]
R9428	RES_402	m42a[67C5]
R9500	RES_402	m42a[68A7]
R9501	RES_402	m42a[68B6]
R9502	RES_402	m42a[68B6]
R9503	RES_402	m42a[68A4]
R9504	RES_402	m42a[68B2]
R9505	RES_402	m42a[68B2]
R9506	RES_402	m42a[68B1]
R9507	RES_402	m42a[68D2]
R9508	RES_402	m42a[68D2]

R9509	RES_402	m42a[68C2]
R9510	RES_402	m42a[68C2]
R9537	RES_402	m42a[68D1]
R9538	RES_402	m42a[68D1]
R9539	RES_402	m42a[68C1]
R9540	RES_402	m42a[68C1]
R9821	RES_402	m42a[69D7]
R9822	RES_402	m42a[69D6]
R9850	RES_402	m42a[69B8]
R9851	RES_402	m42a[69B8]
R9852	RES_402	m42a[69A8]
R9853	RES_402	m42a[69A8]
R9854	RES_402	m42a[69A8]
R9855	RES_402	m42a[69A8]
R9856	RES_402	m42a[69B6]
R9859	RES_402	m42a[69A6]
R9860	RES_402	m42a[69C3]
R9861	RES_402	m42a[69C3]
R9862	RES_402	m42a[69C5]
R9863	RES_402	m42a[69C5]
R9864	RES_402	m42a[69A6]
R9868	RES_402	m42a[69C8]
R9869	RES_402	m42a[69C8]
R9870	RES_402	m42a[69C1]
R9871	RES_402	m42a[69C1]
RP2300	RPAK4P_SM-LF	m42a[23D5]
RP2600	RPAK4P_SM-LF	m42a[26D2]
RP2601	RPAK4P_SM-LF	m42a[26D2]
RP2602	RPAK4P_SM-LF	m42a[26C2]
RP3000	RPAK4P_SM-LF	m42a[30B4 30C4 30D4 30D4]
RP3001	RPAK4P_SM-LF	m42a[30C4 30A4 30A4 30D4]
RP3002	RPAK4P_SM-LF	m42a[30A4 30A4 30A4 30D4]
RP3003	RPAK4P_SM-LF	m42a[30C4 30C4 30C4 30D4]
RP3004	RPAK4P_SM-LF	m42a[30C4 30C4 30D4]
RP3005	RPAK4P_SM-LF	m42a[30B4 30A4 30A4 30D4]
RP3006	RPAK4P_SM-LF	m42a[30B4 30B4 30A4 30D4]
RP3007	RPAK4P_SM-LF	m42a[30C4 30C4 30C4 30C4]
RP3008	RPAK4P_SM-LF	m42a[30C4 30C4 30C4 30C4]
RP3009	RPAK4P_SM-LF	m42a[30B4 30B4 30C4 30C4]
RP3010	RPAK4P_SM-LF	m42a[30B4 30B4 30B4 30B4]
RP3011	RPAK4P_SM-LF	m42a[30B4 30A4 30B4 30B4]
T4201	XFR_1000BT_82400275_ XFR-SM	m42a[37C6]
T4202	XFR_1000BT_82400275_ XFR-SM	m42a[37B6]
U0700	CPU_YONAH_BGA	m42a[7C3 7D7]
U0700	CPU_YONAH_BGA	m42a[8D8 8D4]
U1001	ADT7461_MSOP	m42a[10C5]
U1200	NB_945GM_BGA	m42a[12D5]
U1200	NB_945GM_BGA	m42a[13D4]
U1200	NB_945GM_BGA	m42a[14D5]
U1200	NB_945GM_BGA	m42a[15D3 15D7]
U1200	NB_945GM_BGA	m42a[16D2 16C8]
U1200	NB_945GM_BGA	m42a[17D5]
U1200	NB_945GM_BGA	m42a[18D4 18D7]
U1900	LREG_TPS73115_SOT23-5	m42a[19D6]
U1901	MM157_SOT23-5-LF	m42a[19C4]
U2100	SB_ICH7M_BGA	m42a[21D6]
U2100	SB_ICH7M_BGA	m42a[22B7 22D3]
U2100	SB_ICH7M_BGA	m42a[23D4]
U2100	SB_ICH7M_BGA	m42a[24D4 24D7]
U2601	MC74VHC1G08_SC70	m42a[26A5]
U2603	MC74VHC1G00_SC70-5	m42a[26A7]
U2680	MC74VHC1G08_SC70	m42a[26B3]
U3100	LREG_BD3533FVM_MSOP-8	m42a[31C4]
U3301	CLK_SYN_SLG8LP436_QFN	m42a[32C5]
U4101	88E8053_QFN	m42a[36D6]
U4102	EEPROM_M24C08_SO8	m42a[36A3]
U4400	FW32306_BGA_BGA	m42a[38C5]
U5100	CY8C24794_MLF	m42a[41C5]
U5200	SWI_TPS2042B_MSOP	m42a[42C7]
U5800	SMC_H8S2116_BGA	m42a[45A8 45C3 45C7 45D7]
U5900	VDET_RN5VD_SOT23-5	m42a[46D7]
U5910	OSC_12P_SG-3040LC-SM	m42a[46A7]
U5977	COMPARATOR_LMC7211_SM-LF	m42a[46C2]
U6100	OPAMP_LMV2011_SOT23-5	m42a[48C3]
U6200	MAX6695_UMAX	m42a[49D4]
U6250	MAX6695_UMAX	m42a[49B4]
U6301	FLASH_SST25VF016B_SOI	m42a[50D3]
U6620	KXM52_QFN	m42a[52C5]
U6650	LIS3L02AL_LGA	m42a[52B5]
U6700	TPM_TSSOP	m42a[53C5]
U6800	AUDIO_STAC92204XR_LQFP	m42a[54D5]
U7210	MAX9705_TDFN1	m42a[55C5]
U7220	MAX9705_TDFN1	m42a[55B5]
U7230	MAX9705_TDFN1	m42a[55A5]
U7400	MAX9890_UCSP1	m42a[57C2]
U7500	ISL6262_QFN	m42a[58C6]
U7600	LTC3728L_QFN	m42a[59C5]
U7700	MAX8887_SOT23-5	m42a[60D4]
U7701	MAX8887_SOT23-5	m42a[60C4]
U7720	LREG_MAX8516_SOP	m42a[60B3]
U7800	ISL6269_QFN	m42a[61C5]
U7801	AMP_INA326_MSOP	m42a[61C2]
U7900	LTC3728L_QFN	m42a[62C5]
U7901	AMP_INA326_MSOP	m42a[62A6]
U8070	LTC2908_LLP	m42a[63B2]
U8080	MC74VHC1G08_SC70	m42a[63B1]
U8090	LT3470_TSOT23-8	m42a[63D3]
U8200	COMPARATOR_LMC7211_SM-LF	m42a[65C4]
U8250	MC74VHC1G08_SC70	m42a[65C3]
U8290	COMPARATOR_LM397_SOT23-5	m42a[65C5]
U8300	ISL6255_QFN	m42a[66C6]
U8370	INA193_SOT23-5	m42a[66C3]
U8375	INA193_SOT23-5	m42a[66B2]
U9453	MC74VHC1G08_SC70	m42a[67C5]
U9500	SIL1362_LQFP	m42a[68B4]
U9801	VIDEO_TS3V330_SOP	m42a[69B7]
U9804	SN74LVC2G125_US	m42a[69C2 69C2]
VR5965	VREF_ISL6000233_SOT23-3	m42a[46C7]
VR6800	LREG_TPS79501_SOT223-6	m42a[54A5]
XW5800	SHORT_SM	m42a[45C3]
XW7200	SHORT_SM	m42a[55A5]

XW7300	SHORT_SM	m42a[56C4]
XW7301	SHORT_SM	m42a[56B4]
XW7302	SHORT_SM	m42a[56C2]
XW7303	SHORT_SM	m42a[56C2]
XW7304	SHORT_SM	m42a[56B2]
XW7305	SHORT_SM	m42a[56B7]
XW7400	SHORT_SM	m42a[57A7]
XW7500	SHORT_SM	m42a[58A6]
XW7600	SHORT_SM	m42a[59A5]
XW7620	JUMPER_OPEN-SAWTOOTH	m42a[59B8]
XW7660	JUMPER_OPEN-SAWTOOTH	m42a[59B1]
XW7800	SHORT_SM	m42a[61B5]
XW7900	SHORT_SM	m42a[62A5]
XW7920	JUMPER_OPEN-SAWTOOTH	m42a[62B8]
XW8101	SHORT_SM	m42a[64B2]
XW8102	SHORT_SM	m42a[64B2]
XW8300	SHORT_SM	m42a[66B4]
Y2600	CRYSTAL_4PIN_SM-LF	m42a[26C7]
Y3301	CRYSTAL_5X3.2-SM	m42a[32C7]
Y4101	CRYSTAL_4PIN_SM-3.2X2.5MM	m42a[36B6]
Y4403	CRYSTAL_4PIN_SM-3.2X2.5MM	m42a[38C2]
Y5920	CRYSTAL_5X3.2-SM	m42a[46C7]
Y6795	CRYSTAL_4PIN_SM-LF	m42a[53B6]
Z0601	MTGHOLE	m42a[6B8]
Z0602	MTGHOLE	m42a[6C6]
Z0603	PCB_STANDOFF	m42a[6A8]
Z0604	PCB_STANDOFF	m42a[6A6]
Z0605	PCB_STANDOFF	m42a[6A8]
Z0606	MTGHOLE	m42a[6D6]
Z0607	MTGHOLE	m42a[6C6]
Z0608	MTGHOLE	m42a[6C6]
Z0609	MTGHOLE	m42a[6B7]
Z0610	MTGHOLE	m42a[6B6]
Z0611	MTGHOLE	m42a[6B7]
Z0612	PCB_STANDOFF	m42a[6A6]
Z0613	PCB_STANDOFF	m42a[6A5]
Z0621	PCB_STANDOFF	m42a[6A6]
ZS0620	SPRING_CLIP_1P_EMI_CLIP-SM-M42	m42a[6D7]
ZS0621	CLIP_SM	m42a[6D6]