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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, HARP, Q41C

06/02/05



REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
02		38423	ENGINEERING RELEASED	06/02/05	05

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
815-7053	1	ALS DUST COVER	DC1	?

PAGE CONTENTS

1	TITLE PAGE AND CONTENTS
2	PCB NOTES
3	USB / SENSOR
4	POWER CONNECTOR
5	SIGNAL CONSTRAINTS
6	POWER CONSTRAINTS
7	COMPONENT LOCATIONS
8	SIGNAL LOCATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6852	1	SCHEM, HARP, Q41C	SCH1	
820-1825	1	PCBF, HARP, Q41C	PCB1	

DIMENSIONS ARE IN MILLIMETERS		METRIC		 Apple Computer Inc.	
XX :	_____	DRAPTR	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-6852	REV. 02
SHEET 1 OF 8					

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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC: FR-4
 LAYER COUNT: 12
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

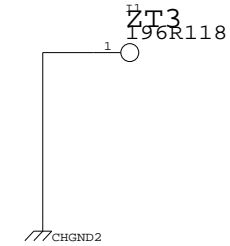
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1	SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL) GROUND (1/2 OZ)
3	LAMINATE (4MIL) SIGNAL (1/2 OZ)
4	PREPREG (3MIL) SIGNAL (1/2 OZ)
5	LAMINATE (4MIL) GROUND (1/2 OZ)
6	PREPREG (2MIL) CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL) CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL) GROUND (1/2 OZ)
9	LAMINATE (4MIL) SIGNAL (1/2 OZ)
10	PREPREG (3MIL) SIGNAL (1/2 OZ)
11	LAMINATE (4MIL) GROUND (1/2 OZ)
12	PREPREG (3MIL) SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES

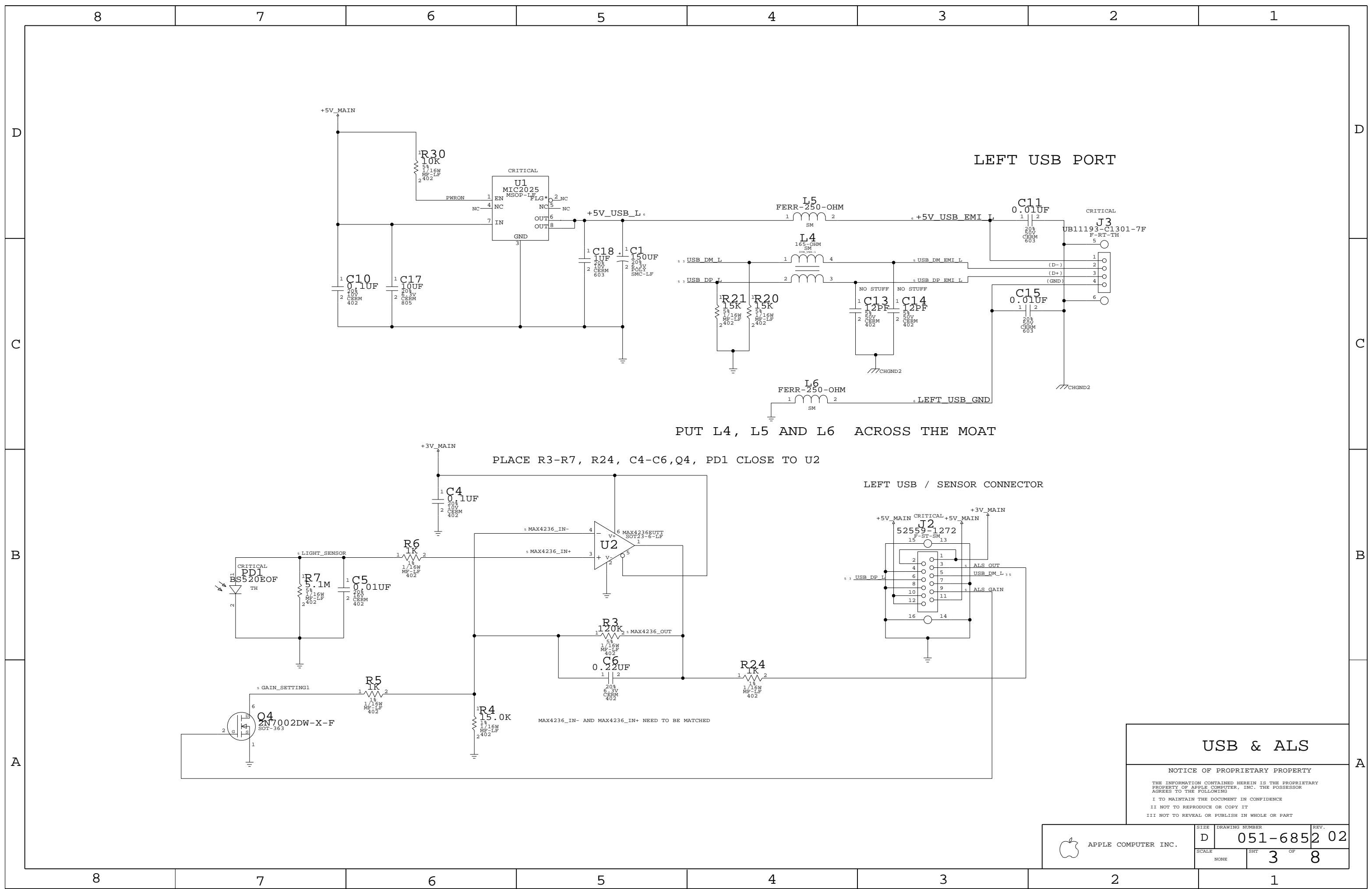


PCB BOARD STANDOFFS

BOARD INFORMATION

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6852	02
SCALE	SHT		OF
NONE	2		8



PUT L4, L5 AND L6 ACROSS THE MOAT

PLACE R3-R7, R24, C4-C6, Q4, PD1 CLOSE TO U2

USB & ALS

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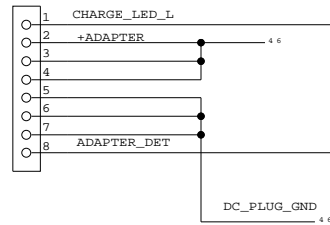
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NONE	3	8	

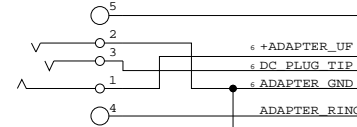
POWER CONNECTOR

CRITICAL
J4
87437-0843
M-ST-SM

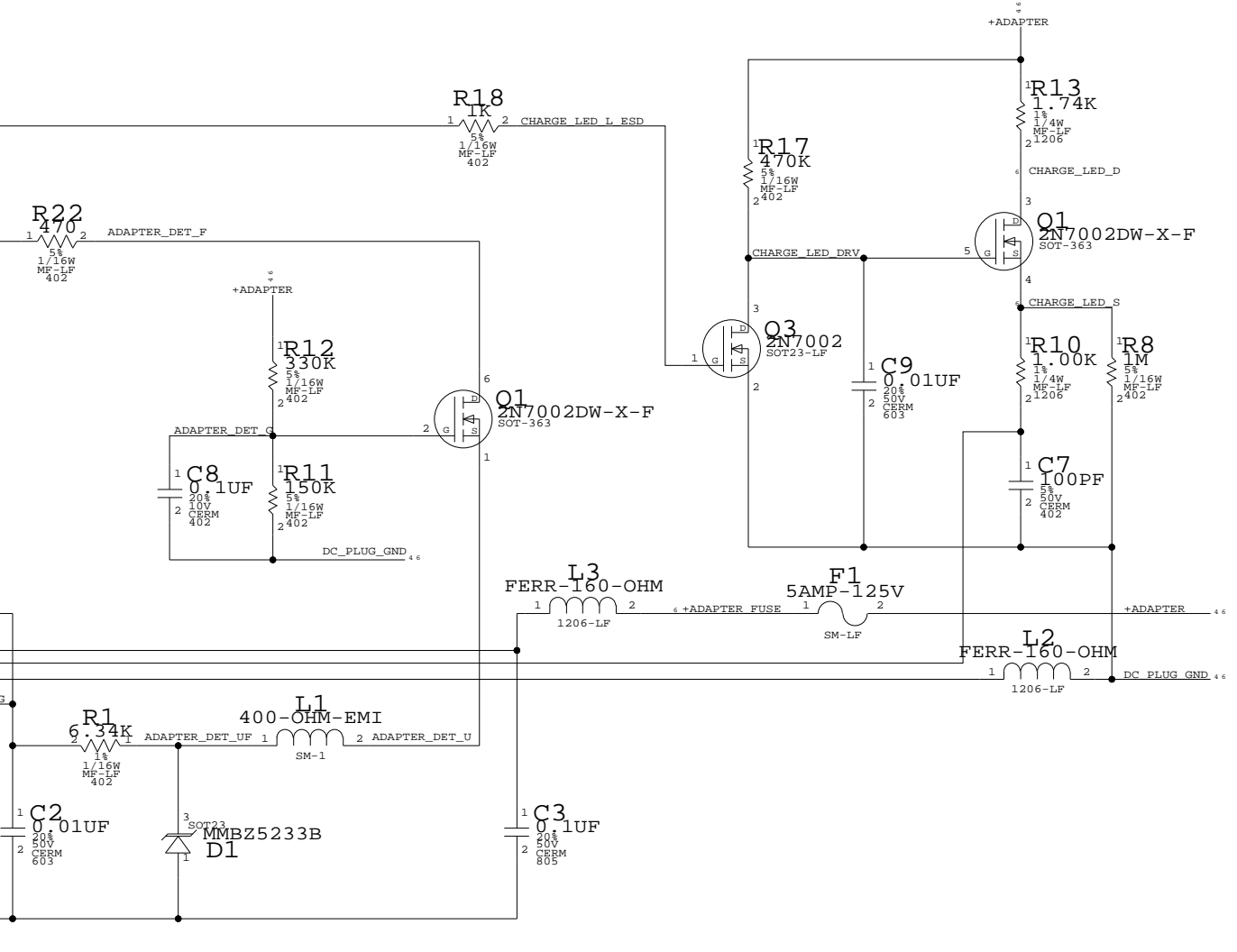


DC POWER JACK

CRITICAL
J1
JPD1133-W01
F-RT-TH-LF



CHARGE LED SUPPORT



PLACE C2, C3 AND C16 CLOSE TO J1
PLACE L1, L2 AND L3 CLOSE TO J1

DC POWER INTERFACE

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8

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Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	MIN_LINE_WIDTH	NET_SPACING_TYPE	NET_PHYSICAL_TYPE
USB						
	USB_DM_L	USB_D1	USB_DM:J2.4:L4.1:0.5		USB2_PAIR	USB2
	USB_DP_L	USB_D1	USB_DP:J2.3:L4.2:0.5		USB2_PAIR	USB2
	USB_DM_EMI_L	USB_D1_EMI	USB_D1_EMI:L4.4:J3.2:0.5		USB2_EMI_PAIR	USB2_EMI
	USB_DP_EMI_L	USB_D1_EMI	USB_D1_EMI:L4.3:J3.3:0.5		USB2_EMI_PAIR	USB2_EMI

ALS SIGNALS

GROUP	SIG_NAME	DELAY_RULE	MATCHED_DELAY	STUB_LENGTH	MIN_LINE_WIDTH	MIN_NECK_WIDTH
ALS						
	LIGHT_SENSOR				MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	GAIN_SETTING1				MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	MAX4236_IN+				MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	MAX4236_IN-				MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	MAX4236_OUT				MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.5MM
	ALS_GAIN				MIN_LINE_WIDTH=0.125MM	MIN_NECK_WIDTH=0.125MM
	ALS_OUT				MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM

FOR USB DIFFERENTIAL TRACES (ZSINGLE=45 OHM +- 10%, ZDIFF=90 OHM +- 15%)

	MICROSTRIP (OUTER LAYERS)	STRIPLINE (INTERNAL LAYERS)
TRACE WIDTH	4 MIL	5 MIL
SEPARATION OF TRACES	8 MIL	10 MIL

SIGNAL CONSTRAINTS - PAGE 3

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NONE	5	8

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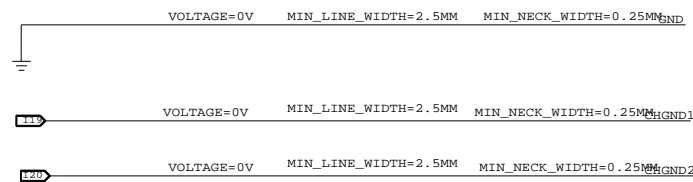
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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
ADAPTER	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=0.6MM	MIN_NECK_WIDTH=0.25MM
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=0.6MM	MIN_NECK_WIDTH=0.25MM
	+ADAPTER_UF	VOLTAGE=24V	MIN_LINE_WIDTH=2.5MM	MIN_NECK_WIDTH=0.25MM
	+ADAPTER_FUSE	VOLTAGE=24V	MIN_LINE_WIDTH=2.5MM	MIN_NECK_WIDTH=0.25MM
	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=2.5MM	MIN_NECK_WIDTH=0.25MM
	ADAPTER_GND	VOLTAGE=0V	MIN_LINE_WIDTH=2.5MM	MIN_NECK_WIDTH=0.25MM
	CHARGE_LED_D	VOLTAGE=	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	CHARGE_LED_S	VOLTAGE=	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	DC_PLUG_TIP	VOLTAGE=	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	DC_PLUG_GND	VOLTAGE=0V	MIN_LINE_WIDTH=2.5MM	MIN_NECK_WIDTH=0.25MM
USB	+5V_USB_L	VOLTAGE=5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	+5V_USB_EMI_L	VOLTAGE=5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	LEFT_USB_GND	VOLTAGE=0V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM



CHANGE HISTORY

1. IMPORTED 051-6474
2. CHANGED LM3526 TO MIC2025
3. ADDED ASL DUST COVER (815-7053) FOR THE BOM
4. SCHEMATIC RELEASED FOR PROTO
4. LEAD FREE PARTS. SCHEMATIC RELEASED FOR EVT.

SIGNAL CONSTRAINTS - PAGE 4

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