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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
02		384232	ENGINEERING RELEASED	06/02/05?	

# SCHEM, BASSOON, Q41C

## 06/02/2005

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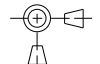
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PAGE	CONTENTS
1	TITLE PAGE AND CONTENTS
2	PCB NOTES AND HOLES
3	BACK UP BATTERY
4	RIGHT USB PORT
5	CONSTRAINTS / REVISION HISTORY
6	SIGNAL LOCATIONS
7	COMPONENT LOCATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6851	1	SCHEM, BASSOON, Q41C	SCH1	
820-1824	1	PCBF, BASSOON, Q41C	PCB1	

DIMENSIONS ARE IN MILLIMETERS		<b>METRIC</b>		 Apple Computer Inc.	
XX : _____		DRAPTER	DESIGN CK	<b>NOTICE OF PROPRIETARY PROPERTY</b> THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX : _____		ENG APPD	MFG APPD		
X.XXX : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING			NONE	<b>SCHEM, BASSOON, Q41C</b>	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE			
				DRAWING NUMBER	REV.
				<b>051-6851</b>	<b>02</b>
				SHT 1 OF 7	

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# PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN  
 1/2 OZ CU THICKNESS: 0.7 MILS  
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%  
 DIELECTRIC: FR-4  
 LAYER COUNT: 12  
 SIGNAL TRACE WIDTH: 4 MILS  
 SIGNAL TRACE SPACING: 4 MILS  
 PREPREG THICKNESS: 2-3 MILS

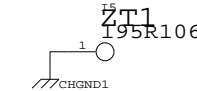
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

## BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1	SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL) GROUND (1/2 OZ)
3	LAMINATE (4MIL) SIGNAL (1/2 OZ)
4	PREPREG (3MIL) SIGNAL (1/2 OZ)
5	LAMINATE (4MIL) GROUND (1/2 OZ)
6	PREPREG (2MIL) CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL) CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL) GROUND (1/2 OZ)
9	LAMINATE (4MIL) SIGNAL (1/2 OZ)
10	PREPREG (3MIL) SIGNAL (1/2 OZ)
11	LAMINATE (4MIL) GROUND (1/2 OZ)
12	PREPREG (3MIL) SIGNAL (1/3 OZ + COPPER PLATING)

## BOARD HOLES



## PCB BOARD STANDOFFS

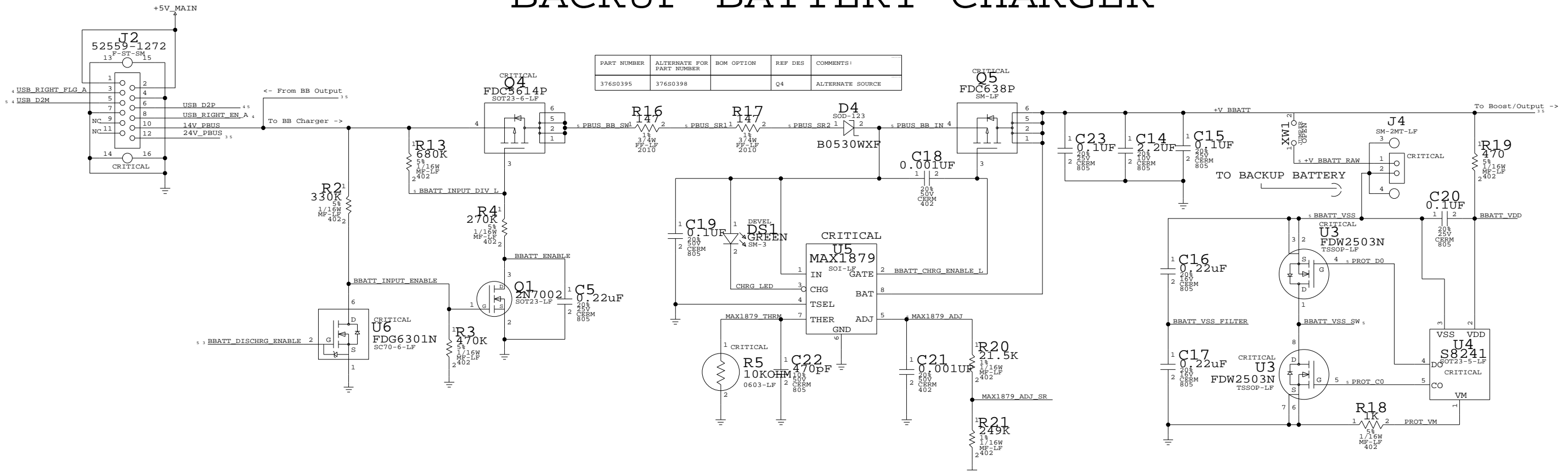
## BOARD INFORMATION

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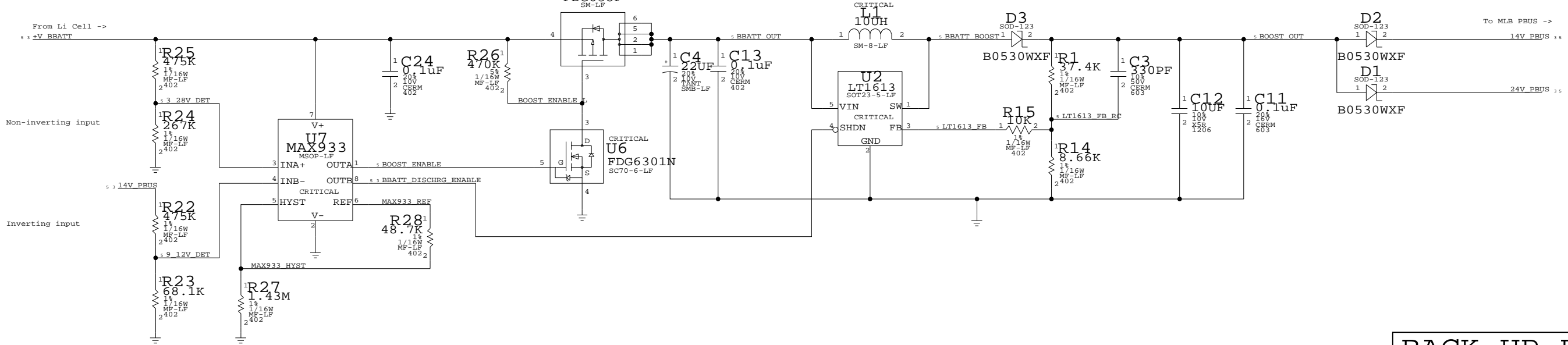
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6851	02
SCALE	SHT	OF	
NONE	2	7	

# BACKUP BATTERY CHARGER

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0395	376S0398		Q4	ALTERNATE SOURCE



$I(REF) = 1.182V / (R28 + R27) = 0.799UA$   
 HYSTERESIS BAND VOLTAGE (VHB) =  $2 * I(REF) * R28 = 77.9mV$   
 Both inputs are compared to REF - Hysteresis voltage (1.182V +/- 0.5 \* VHB)

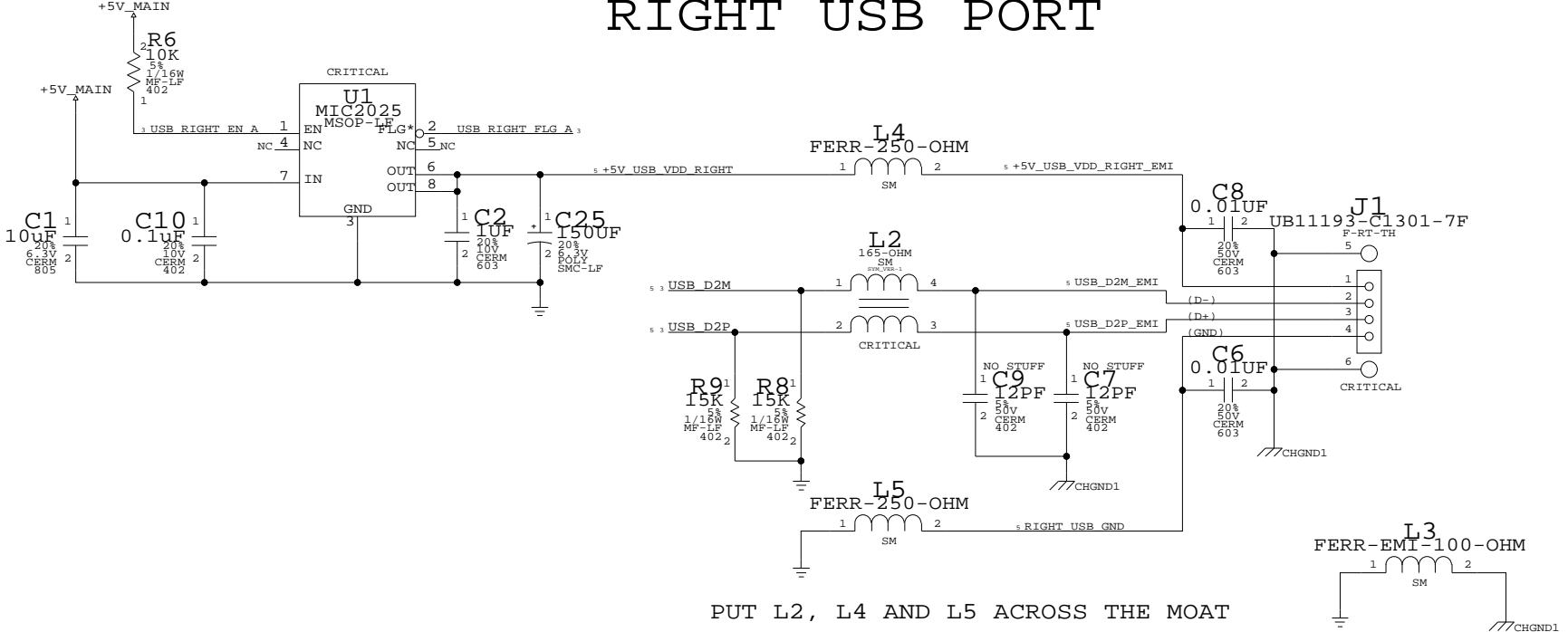


## BACK UP BATTERY

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6851	02
SCALE	NONE	SHT	OF
		3	7

# RIGHT USB PORT



PUT L2, L4 AND L5 ACROSS THE MOAT

## USB CONNECTOR

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	D	051-6851	02
SCALE	SHT		OF
NONE	4		7

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Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY
USB	USB_D2M	USB_D2	USB_D2:J2.5:L2.1:5 USB2 PAIR 14
	USB_D2P	USB_D2	USB_D2:J2.6:L2.2:5 USB2 PAIR 14
	USB_D2M_EMI	USB_D2_EMI	USB_D2_EMI:L2.4:J1.2:5 USB2 EMI PAIR
	USB_D2P_EMI	USB_D2_EMI	USB_D2_EMI:L2.3:J1.3:5 USB2 EMI PAIR

REVISION HISTORY

- 02/18/05 - SCHEMATIC ORIGINATED FROM Q41B 051-6753-A
- 02/21/05 - REMOVED R6 AND J3 FOR SUPERCAP
- REMOVED R7
- 02/22/05 - CORRECTED THE NOTE
- 03/09/05 - CHANGED CONSTRAINT FOR 14V\_PBUS
- 04/25/05 - SCHEMATIC RELEASE FOR PROTO
- 06/02/05 - SCHEMATIC RELEASE FOR EVT. LEAD FREE PARTS.

Power Signals

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
BATTERY	24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	14V_PBUS	VOLTAGE=14V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	PBUS_BB_IN	VOLTAGE=14V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	PBUS_SR2	VOLTAGE=14V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	PBUS_SR1	VOLTAGE=14V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	PBUS_BB_SW	VOLTAGE=14V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	+V_BBATT	VOLTAGE=4.2V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	+V_BBATT_RAW	VOLTAGE=4.2V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	BBATT_VSS	VOLTAGE=0V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	BBATT_VSS_SW	VOLTAGE=0V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
MAX1879	MAX1879_ADJ	VOLTAGE=1.4V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
	BBATT_INPUT_DIV_L	VOLTAGE=14V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
S8241	PROT_D0	VOLTAGE=4.2V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
	PROT_C0	VOLTAGE=4.2V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
	9_12V_DET	VOLTAGE=1.2V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
MAX933	3_28V_DET	VOLTAGE=1.2V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
	BOOST_ENABLE	VOLTAGE=4.2V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
	BBATT_DISCHRG_ENABLE	VOLTAGE=4.2V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
LT1613	BBATT_OUT	VOLTAGE=4.2V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	BBATT_BOOST	VOLTAGE=6.5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	BOOST_OUT	VOLTAGE=6.5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	LT1613_FB	VOLTAGE=1.3V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
USB	LT1613_FB_RC	VOLTAGE=1.3V	MIN_LINE_WIDTH=0.25MM	MIN_NECK_WIDTH=0.25MM
	+5V_USB_VDD_SW	VOLTAGE=5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	+5V_USB_VDD_RIGHT	VOLTAGE=5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	+5V_USB_VDD_RIGHT_EMI	VOLTAGE=5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	RIGHT_USB_GND	VOLTAGE=0V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM
	GND	VOLTAGE=0V	MIN_LINE_WIDTH=0.5MM	MIN_NECK_WIDTH=0.25MM

SIGNAL CONSTRAINTS

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D	051-6851	02
SCALE	SHT	OF
NONE	5	7

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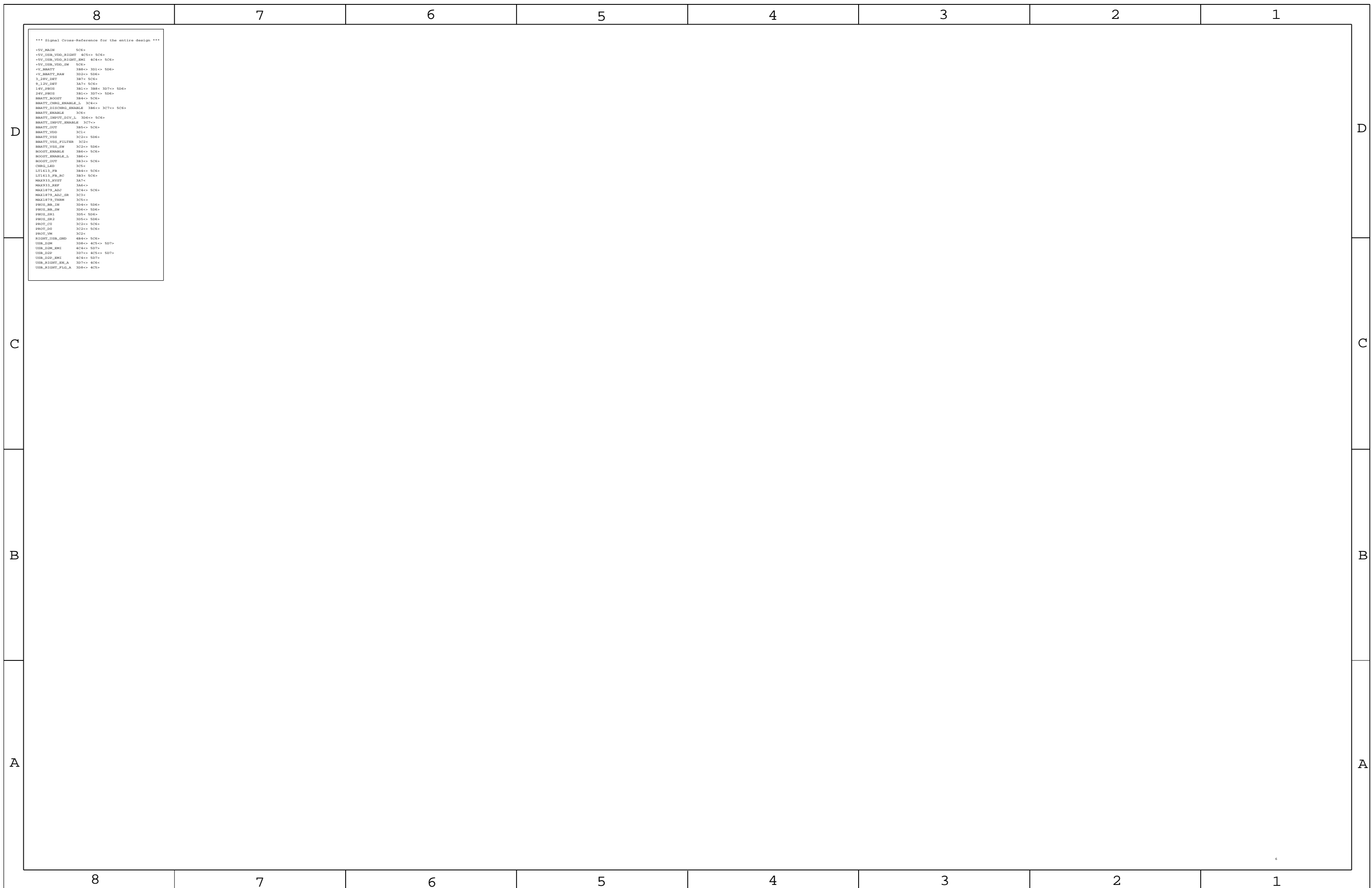
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\*\*\* Signal Cross-Reference for the entire design \*\*\*

```

+SV_MAIN 5C6>
+SV_USB_VDD_RIGHT 4C5<> 5C6>
+SV_USB_VDD_RIGHT_EMI 4C4<> 5C6>
+SV_USB_VDD_SW 5C6>
+V_BBATT 3B8<> 3D1<> 5D6>
+V_BBATT_RAM 3D2<> 5D6>
3_2RV_DET 3B7<> 5C6>
0_1RV_DET 3A7<> 5C6>
14V_PBUS 3B1<> 3B8< 3D7<> 5D6>
24V_PBUS 3B1<> 3D7<> 5D6>
BBATT_BOOT 3B4<> 5C6>
BBATT_CHRG_ENABLE_L 3C4<>
BBATT_DISCHRG_ENABLE 3B6<> 3C7<> 5C6>
BBATT_ENABLE 3C6<>
BBATT_INPUT_DIV_L 3D6<> 5C6>
BBATT_OUT 3B5<> 5C6>
BBATT_VDD 3C1<>
BBATT_VSS 3C2<> 5D6>
BBATT_VSS_FILTER 3C2<>
BBATT_VSS_SW 3C2<> 5D6>
BOOT_ENABLE 3B6<> 5C6>
BOOT_ENABLE_L 3B8<>
BOOT_OUT 3B3<> 5C6>
CHRG_LED 3C5<>
LT1611_FB 3B4<> 5C6>
LT1611_FB_RC 3B3<> 5C6>
MAX9313_RST 3A7<>
MAX9313_SEP 3A6<>
MAX1879_ADJ 3C4<> 5C6>
MAX1879_ADJ_SR 3C1<>
MAX1879_THERM 3C5<>
PWR0_BB_IN 3D4<> 5D6>
PWR0_BB_SW 3D6<> 5D6>
PWR0_SR1 3D5<> 5D6>
PWR0_SR2 3D5<> 5D6>
PWR0_V0 3C2<> 5C6>
PWR0_V0 3C2<> 5C6>
PWR0_VN 3C2<>
RIGHT_USB_GND 4B4<> 5C6>
USB_D2M 3D8<> 4C5<> 5D7>
USB_D2M_EMI 4C4<> 5D7>
USB_D2M 3D7<> 4C5<> 5D7>
USB_D22_EMI 4C4<> 5D7>
USB_RIGHT_EN_A 3D7<> 4C6>
USB_RIGHT_FLG_A 3D8<> 4C5>

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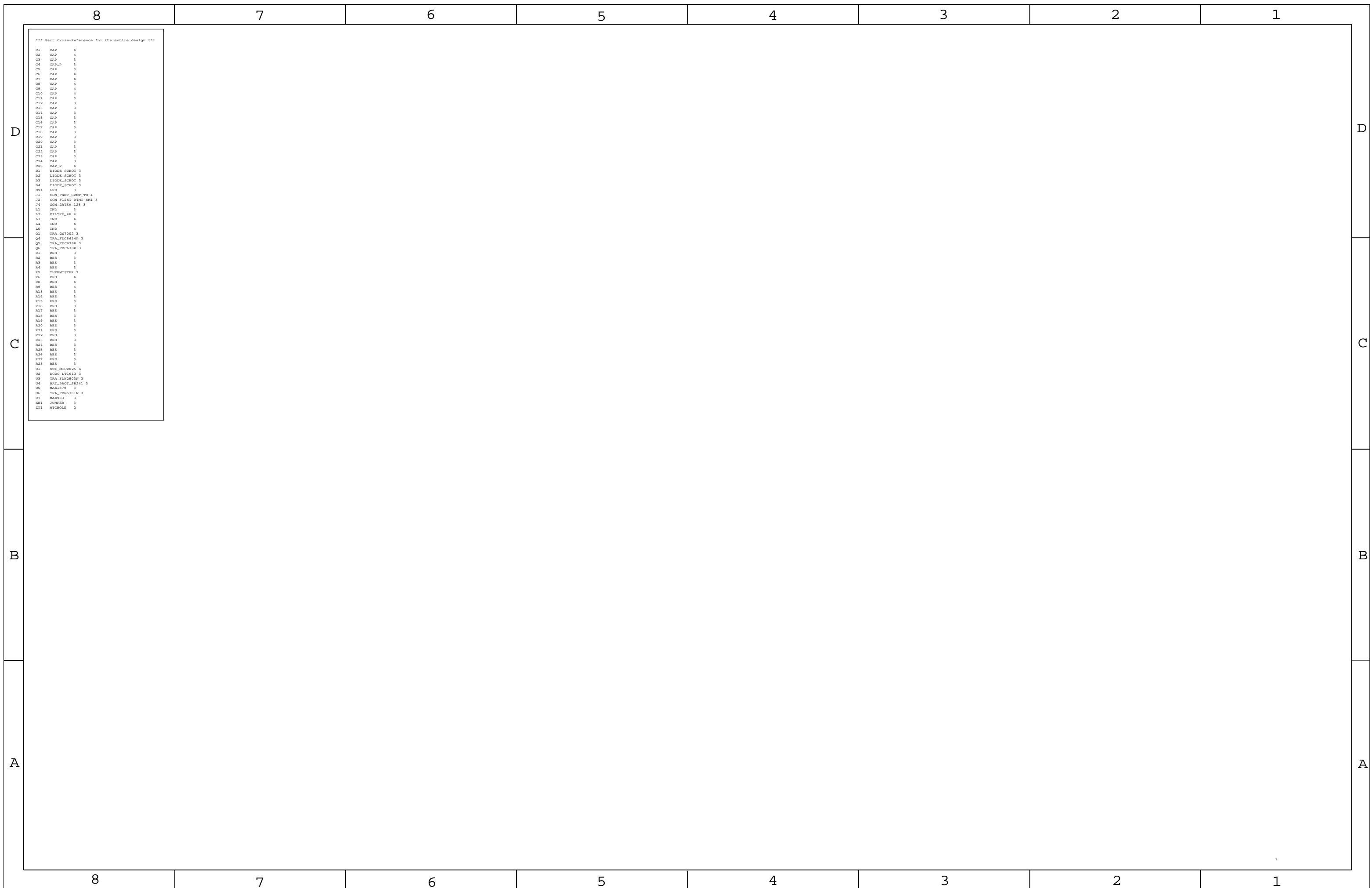
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\*\*\* Part Cross-Reference for the entire design \*\*\*

C1	CAP	4
C2	CAP	4
C3	CAP	3
C4	CAP_P	3
C5	CAP	3
C6	CAP	4
C7	CAP	4
C8	CAP	4
C9	CAP	4
C10	CAP	4
C11	CAP	3
C12	CAP	3
C13	CAP	3
C14	CAP	3
C15	CAP	3
C16	CAP	3
C17	CAP	3
C18	CAP	3
C19	CAP	3
C20	CAP	3
C21	CAP	3
C22	CAP	3
C23	CAP	3
C24	CAP	3
C25	CAP_P	4
D1	DIODE_SCHOT	3
D2	DIODE_SCHOT	3
D3	DIODE_SCHOT	3
D4	DIODE_SCHOT	3
D5	DIODE_SCHOT	3
D6	LED	3
J1	CON_F12ST_24MT_TW	4
J2	CON_F12ST_24MT_SM1	3
J4	CON_2RTDM_125	3
L1	IND	3
L2	FILTER_4P	4
L3	IND	4
L4	IND	4
L5	IND	4
Q1	TRA_2N7002	3
Q4	TRA_FDC634D	3
Q5	TRA_FDC634D	3
Q6	TRA_FDC634D	3
R1	RES	3
R2	RES	3
R3	RES	3
R4	RES	3
R5	THERMISTOR	3
R6	RES	4
R8	RES	4
R9	RES	4
R13	RES	3
R14	RES	3
R15	RES	3
R16	RES	3
R17	RES	3
R18	RES	3
R19	RES	3
R20	RES	3
R21	RES	3
R22	RES	3
R23	RES	3
R24	RES	3
R25	RES	3
R26	RES	3
R27	RES	3
R28	RES	3
U1	SMI_M1C2025	4
U2	DCDC_I71613	3
U3	TRA_FDC634D	3
U4	REG_3V3	3
U5	MAX1879	3
U6	TRA_FDC634D	3
U7	MAX933	3
XM1	JUMPER	3
ZT1	WTHOLE	2

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