1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,BKUP BATT/RT USB,PB17"

12/16/2004

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		356260	PRODUCTION RELEASED	12/16/04?	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6753	1	SCHEM,JADE,PB17	SCH1	
820-1734	1	PCBF,JADE,PB17	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,BKUP BATT/RT USB,PB17

DRAWING NUMBER 051-6753 REV. A

SHT 1 OF 7

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

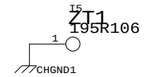
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



PCB BOARD STANDOFFS

BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6753	A

SCALE	SHT	OF
NONE	2	7

BACKUP BATTERY CHARGER

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0272	1	TRA_IRF5803	TRA-TSOP-6F	(XSTR,MSFT,P-CH,40V,2.7A,100_MOHM,TSOP-6)	IRF5803				Q4	CRITICAL	BACKUP_BATT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0060	376S0272	BACKUP_BATT	Q4	ALTERNATE SOURCE

THE PADS OF J3 AND R6 ARE COVERED BY SOLDER MASK TO PREVENT SHORTING TO BACKUP BATTERY CELL IF SUPERCAP IS NEEDED, FAB HAS TO BE MODIFIED.

I(REF) = 1.182V / (R7 + R5) = 0.799uA
Hysteresis band voltage (VHB) = 2 * I(REF) * R7 = 77.9mV
Both inputs are compared to REF - Hysteresis voltage (1.182V +/- 0.5 * VHB)

Non-inverting input

Inverting input

BACK UP BATTERY

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II NOT TO REPRODUCE OR COPY IT

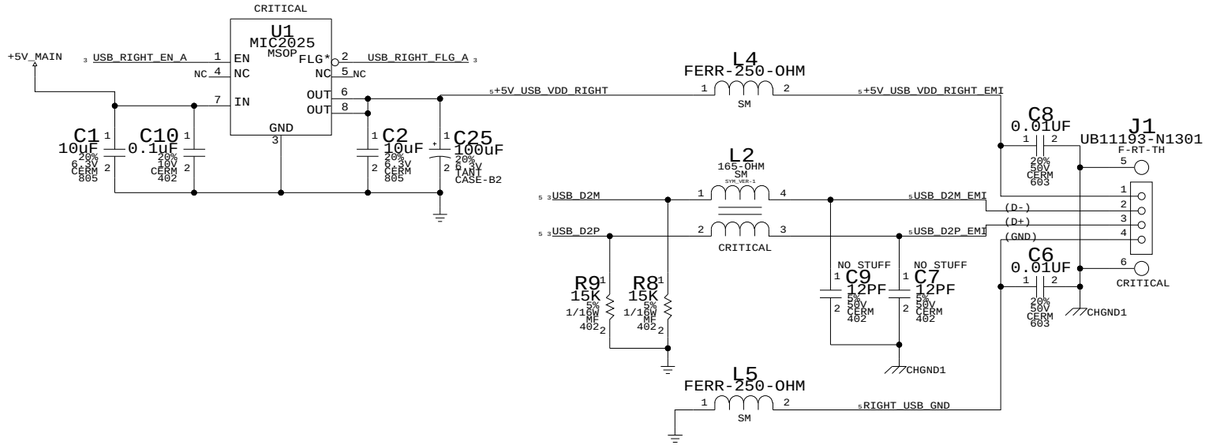
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

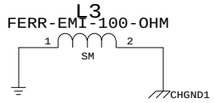
SIZE	DRAWING NUMBER	REV.
D	051-6753	A

SCALE	SHT	OF
NONE	3	7

RIGHT USB PORT



PUT L2, L4 AND L5 ACROSS THE MOAT



USB CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6753	A
SCALE: NONE	SHT 4 OF 7	

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	
USB	USB_D2M	USB_D2	USB_D2:J2.5:L2.1:200	3 4
	USB_D2P	USB_D2	USB_D2:J2.6:L2.2:200	3 4
	USB_D2M_EMI	USB_D2_EMI	USB_D2_EMI:L2.4:J1.2:200	4
	USB_D2P_EMI	USB_D2_EMI	USB_D2_EMI:L2.3:J1.3:200	4

Power Signals

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
BATTERY	24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	14V_PBUS	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	PBUS_BB_IN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	PBUS_SR2	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	PBUS_SR1	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	PBUS_BB_SW	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	+V_BBATT	VOLTAGE=4.2V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	+V_BBATT_RAW	VOLTAGE=4.2V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	BBATT_VSS	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	BBATT_VSS_SW	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	+5_5V_SUPERCAP	VOLTAGE=5.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	+PWR_SUPERCAP	VOLTAGE=5.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
MAX1879	MAX1879_ADJ	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
	BBATT_INPUT_DIV_L	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
S8241	PROT_D0	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
	PROT_C0	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
	9_12V_DET	VOLTAGE=1.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
MAX933	3_28V_DET	VOLTAGE=1.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
	BOOST_ENABLE	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
	BBATT_DISCHRG_ENABLE	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
LT1613	BBATT_OUT	VOLTAGE=4.2V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	BBATT_BOOST	VOLTAGE=6.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	BOOST_OUT	VOLTAGE=6.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	3
	LT1613_FB	VOLTAGE=1.3V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
	LT1613_FB_RC	VOLTAGE=1.3V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10	3
USB	+5V_USB_VDD_SW	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	+5V_USB_VDD_RIGHT	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	4
	+5V_USB_VDD_RIGHT_EMI	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	4
	RIGHT_USB_GND	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	4
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	GND	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

REVISION HISTORY

EVT
12/15/03 - DESIGN ORIGINATED FROM 051-6475
12/15/03 - (PG. 4) UPDATED USB POWER SWITCH TO MIC2025
13/15/03 - (PG. 3) SWAPPED PINS 3 & 9 ON J2
03/29/04 - (PG. 3) ADDED ALTERNATE FOR FAIRCHILD FET (Q4)
03/29/04 - PRODUCTION RELEASE

****

09/23/04 - SCHEMATIC FROM Q41A DOB
09/23/04 - ADD SUPERCAP

****

12/16/04 - SCHEMATIC RELEASE FOR PRODUCTION

SIGNAL CONSTRAINTS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6753	A

SCALE	SHT	OF
NONE	5	7

*** Signal Cross-Reference for the entire design ***

+5V_MAIN 5C6>
+5V_USB_VDD_RIGHT 4C5<> 5C6>
+5V_USB_VDD_RIGHT_EMI 4C4<> 5C6>
+5V_USB_VDD_SW 5C6>
+5_5V_SUPERCAP 5C6>
+PWR_SUPERCAP 3C7<> 3D7< 5C6>
+V_BBATT 3B8<> 3D1<> 5D6>
+V_BBATT_RAW 3D2<> 5D6>
3_28V_DET 3B7< 5C6>
9_12V_DET 3A7< 5C6>
14V_PBUS 3B1<> 3B8< 3D7<> 5D6>
24V_PBUS 3B1<> 3D7< 5D6>
24V_PBUS_CONN 3D7<>
BBATT_BOOST 3B4<> 5C6>
BBATT_CHRG_ENABLE_L 3C4<>
BBATT_DISCHRG_ENABLE 3B6<> 3C7<> 5C6>
BBATT_ENABLE 3C6<
BBATT_INPUT_DIV_L 3D6<> 5C6>
BBATT_INPUT_ENABLE 3C7<>
BBATT_OUT 3B5<> 5C6>
BBATT_VDD 3C1<
BBATT_VSS 3C2<> 5D6>
BBATT_VSS_FILTER 3C2<
BBATT_VSS_SW 3C2<> 5D6>
BOOST_ENABLE 3B6<> 5C6>
BOOST_ENABLE_L 3B6<>
BOOST_OUT 3B3<> 5C6>
CHRG_LED 3C5<
LT1613_FB 3B4<> 5C6>
LT1613_FB_RC 3B3< 5C6>
MAX933_HYST 3A7<
MAX933_REF 3A6<>
MAX1879_ADJ 3C4<> 5C6>
MAX1879_ADJ_SR 3C3<
MAX1879_THRM 3C5<>
PBUS_BB_IN 3D4<> 5D6>
PBUS_BB_SW 3D6<> 5D6>
PBUS_SR1 3D5< 5D6>
PBUS_SR2 3D5<> 5D6>
PROT_C0 3C2<> 5C6>
PROT_D0 3C2<> 5C6>
PROT_VM 3C2<
RIGHT_USB_GND 4B4<> 5C6>
USB_D2M 3D8<> 4C5<> 5D7>
USB_D2M_EMI 4C4<> 5D7>
USB_D2P 3D7<> 4C5<> 5D7>
USB_D2P_EMI 4C4<> 5D7>
USB_RIGHT_EN_A 3D7<> 4C6<
USB_RIGHT_FLG_A 3D8<> 4C5>

*** Part Cross-Reference for the entire design ***

BT1 BATTERY_3PA 3
C1 CAP 4
C2 CAP 4
C3 CAP 3
C4 CAP_P 3
C5 CAP 3
C6 CAP 4
C7 CAP 4
C8 CAP 4
C9 CAP 4
C10 CAP 4
C11 CAP 3
C12 CAP 3
C13 CAP 3
C14 CAP 3
C15 CAP 3
C16 CAP 3
C17 CAP 3
C18 CAP 3
C19 CAP 3
C20 CAP 3
C21 CAP 3
C22 CAP 3
C23 CAP 3
C24 CAP 3
C25 CAP_P 4
D1 DIODE_SCHOT 3
D2 DIODE_SCHOT 3
D3 DIODE_SCHOT 3
D4 DIODE_SCHOT 3
DS1 LED 3
J1 CON_F4RT_S2MT_TH 4
J2 CON_F12ST_D4RT_SM1 3
J3 CON_2RTSM_125 3
L1 IND 3
L2 FILTER_4P 4
L3 IND 4
L4 IND 4
L5 IND 4
Q1 TRA_2N7002 3
Q4 TRA_FDC5614P 3
Q5 TRA_FDC63BP 3
Q6 TRA_FDC63BP 3
R1 RES 3
R2 RES 3
R3 RES 3
R4 RES 3
R5 THERMISTER 3
R6 RES 3
R7 RES 3
R8 RES 4
R9 RES 4
R13 RES 3
R14 RES 3
R15 RES 3
R16 RES 3
R17 RES 3
R18 RES 3
R19 RES 3
R20 RES 3
R21 RES 3
R22 RES 3
R23 RES 3
R24 RES 3
R25 RES 3
R26 RES 3
R27 RES 3
R28 RES 3
U1 SWI_MIC2025 4
U2 DCDC_LT1613 3
U3 TRA_FDW2503N 3
U4 BAT_PROT_S8241 3
U5 MAX1879 3
U6 TRA_FDG6301N 3
U7 MAX933 3
XW1 JUMPER 3
ZT1 MTGHOLE 2