

# SCHEM, DC-IN/LT USB, PB17"

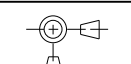

## 07/24/03

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
B		285243	PRODUCTION RELEASED	07/25/03	?

PAGE CONTENTS	
1	TITTLE PAGE AND CONTENTS
2	PCB NOTES
3	USB / SENSOR
4	POWER CONNECTOR
5	SIGNAL CONSTRAINTS
6	POWER CONSTRAINTS
7	COMPONENT LOCATIONS
8	SIGNAL LOCATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6474	1	SCHEM, DC-IN/LT USB, PB17INCH	SCH1	
820-1536	1	PCBF, DC-IN/LT USB, PB17INCH	PCB1	

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <div style="text-align: center;">  <p>THIRD ANGLE PROJECTION</p> </div>	<p><b>METRIC</b></p>	<p style="text-align: center;"> Apple Computer Inc.</p> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <p style="text-align: center;">TITLE</p> <p style="text-align: center; font-weight: bold;">SCHEM, DC-IN/LT USB, PB17INCH</p> <p style="text-align: center;">DRAWING NUMBER <b>051-6474</b> REV. <b>B</b></p> <p style="text-align: right; font-size: x-small;">SHT 1 OF 8</p>																	
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAFTER</td> <td style="width: 25%; text-align: center;">/</td> <td style="width: 25%;">DESIGN CK</td> <td style="width: 25%; text-align: center;">/</td> </tr> <tr> <td>ENG APPD</td> <td style="text-align: center;">/</td> <td>MFG APPD</td> <td style="text-align: center;">/</td> </tr> <tr> <td>QA APPD</td> <td style="text-align: center;">/</td> <td>DESIGNER</td> <td style="text-align: center;">/</td> </tr> <tr> <td>RELEASE</td> <td style="text-align: center;">/</td> <td>SCALE</td> <td style="text-align: center;">NONE</td> </tr> </table>	DRAFTER	/	DESIGN CK	/	ENG APPD	/	MFG APPD	/	QA APPD	/	DESIGNER	/	RELEASE	/	SCALE	NONE	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">MATERIAL/FINISH NOTED AS APPLICABLE</td> <td style="width: 50%;">SIZE D</td> </tr> </table>	MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D
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QA APPD	/	DESIGNER	/																
RELEASE	/	SCALE	NONE																
MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D																		

# PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN  
 1/2 OZ CU THICKNESS: 0.7 MILS  
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%  
 DIELECTRIC: FR-4  
 LAYER COUNT: 12  
 SIGNAL TRACE WIDTH: 4 MILS  
 SIGNAL TRACE SPACING: 4 MILS  
 PREPREG THICKNESS: 2-3 MILS

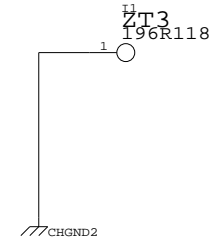
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

## BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1	SIGNAL (1/3 OZ + COPPER PLATING)
2 PREPREG (3MIL)	GROUND (1/2 OZ)
3 LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4 PREPREG (3MIL)	SIGNAL (1/2 OZ)
5 LAMINATE (4MIL)	GROUND (1/2 OZ)
6 PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7 LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8 PREPREG (2MIL)	GROUND (1/2 OZ)
9 LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10 PREPREG (3MIL)	SIGNAL (1/2 OZ)
11 LAMINATE (4MIL)	GROUND (1/2 OZ)
12 PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

## BOARD HOLES

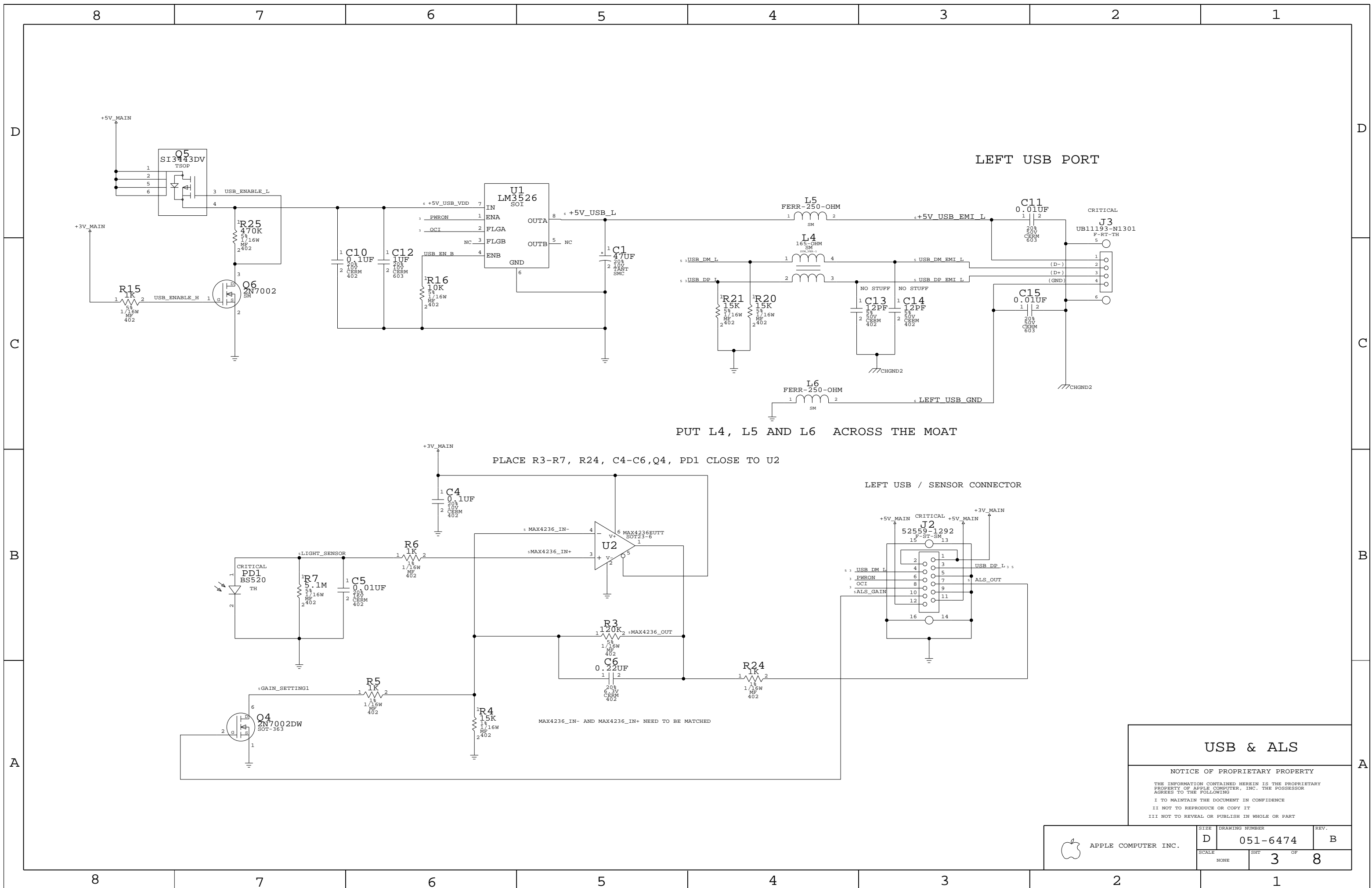


## PCB BOARD STANDOFFS

### BOARD INFORMATION

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	D	051-6474	B
SCALE	SHT	OF	
NONE	2	8	



**USB & ALS**

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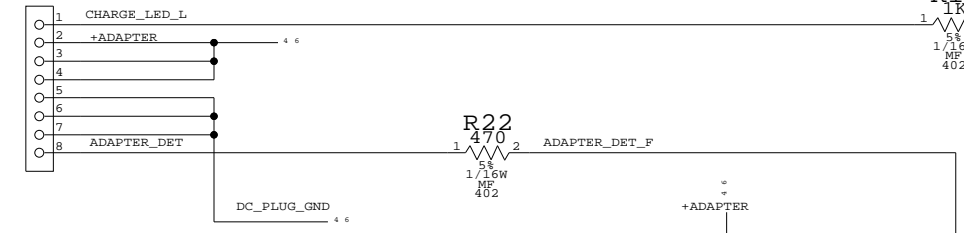
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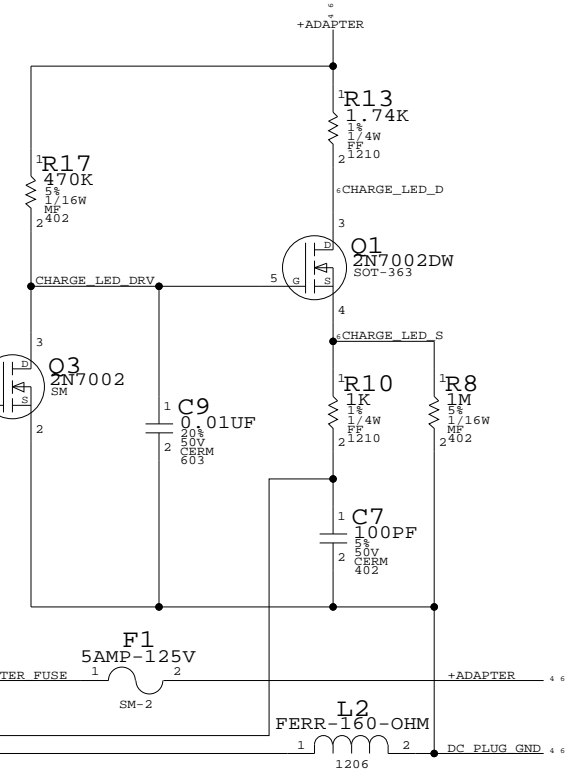
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6474	REV. B
	SCALE NONE	SHEET 3	OF 8

POWER CONNECTOR

CRITICAL  
J4  
87437-0833  
M-ST-SM

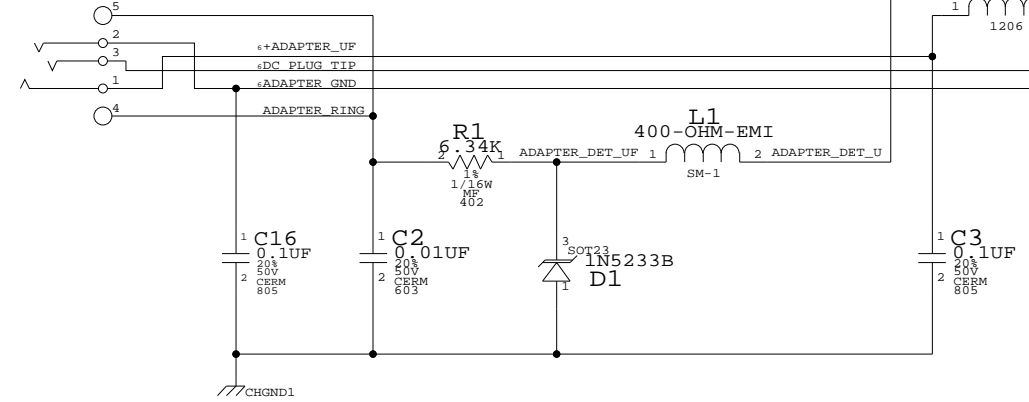


CHARGE LED SUPPORT



DC POWER JACK

CRITICAL  
J1  
JPD1133-W01  
F-RT-TH



PLACE C2, C3 AND C16 CLOSE TO J1  
PLACE L1, L2 AND L3 CLOSE TO J1

DC POWER INTERFACE

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6474	B
SCALE	SHT		OF
NONE	4		8

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## Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	MIN_LINE_WIDTH	NET_SPACING_TYPE	MAX_VIAS
USB						
	USB_DM L	USB_D1	USB_DM:J1.4:L4.1:20	MIN_LINE_WIDTH=5	10 MIL SPACING	
	USB_DP L	USB_D1	USB_DP:J1.3:L4.2:20	MIN_LINE_WIDTH=5	10 MIL SPACING	3
	USB_DM_EMI L	USB_D1_EMI	USB_D1_EMI:L4.4:J3.2:20	MIN_LINE_WIDTH=5	10 MIL SPACING	3
	USB_DP_EMI L	USB_D1_EMI	USB_D1_EMI:L4.3:J3.3:20	MIN_LINE_WIDTH=5	10 MIL SPACING	3

## REVISION HISTORY

04/22/03 - DESIGN ORIGINATED FROM 051-6282  
 04/28/03 - PG 3 - REPLACED R19 & R23 WITH 250-OHM 2A FERRITES (TABLE ITEM)  
 PG 4 - CHANGED C3 TO 0.1UF 0805 (WAS 0.01UF 0603)  
 04/29/03 - PG 4 - REPLACED R2 WITH C16 0.1UF 0805 (WAS 0-OHM 0402)  
 04/29/03 - PG 4 - REPLACED R19 & R23 WITH L5 & L6 (PAD CHANGE FOR FERRITES)  
 CHANGED L2 & L3 FROM 50-OHM FERRITES TO 160-OHM  
 07/24/03 - PRODUCTION RELEASE

## ALS SIGNALS

GROUP	SIG_NAME	DELAY_RULE	MATCHED_DELAY	STUB_LENGTH	MIN_LINE_WIDTH	NET_SPACING_TYPE
ALS						
	LIGHT_SENSOR				MIN_LINE_WIDTH=20	
	GAIN_SETTING1				MIN_LINE_WIDTH=20	
	MAX4236_IN+				MIN_LINE_WIDTH=20	
	MAX4236_IN-				MIN_LINE_WIDTH=20	
	MAX4236_OUT				MIN_LINE_WIDTH=20	
	ALS_GAIN				MIN_LINE_WIDTH=5	
	ALS_OUT				MIN_LINE_WIDTH=10	

FOR USB DIFFERENTIAL TRACES (ZSINGLE=45 OHM +- 10%, ZDIFF=90 OHM +- 15%)

	MICROSTRIP (OUTER LAYERS)	STRIPLINE (INTERNAL LAYERS)
TRACE WIDTH	4 MIL	5 MIL
SEPARATION OF TRACES	8 MIL	10 MIL

SIGNAL CONSTRAINTS - PAGE 3

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SIZE DRAWING NUMBER REV.

D 051-6474 B

SCALE NONE SHT 5 OF 8

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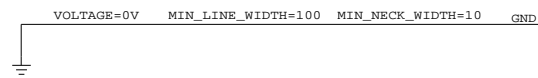
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# POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
ADAPTER	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+ADAPTER_UF	VOLTAGE=24V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=10
	+ADAPTER_FUSE	VOLTAGE=24V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=10
	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=10
	ADAPTER_GND	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=10
	CHARGE_LED_D	VOLTAGE=	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	CHARGE_LED_S	VOLTAGE=	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	DC_PLUG_TIP	VOLTAGE=	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	DC_PLUG_GND	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=10
USB	+5V_USB_VDD	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+5V_USB_L	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+5V_USB_EMI_L	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LEFT_USB_GND	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10



SIGNAL CONSTRAINTS - PAGE 4

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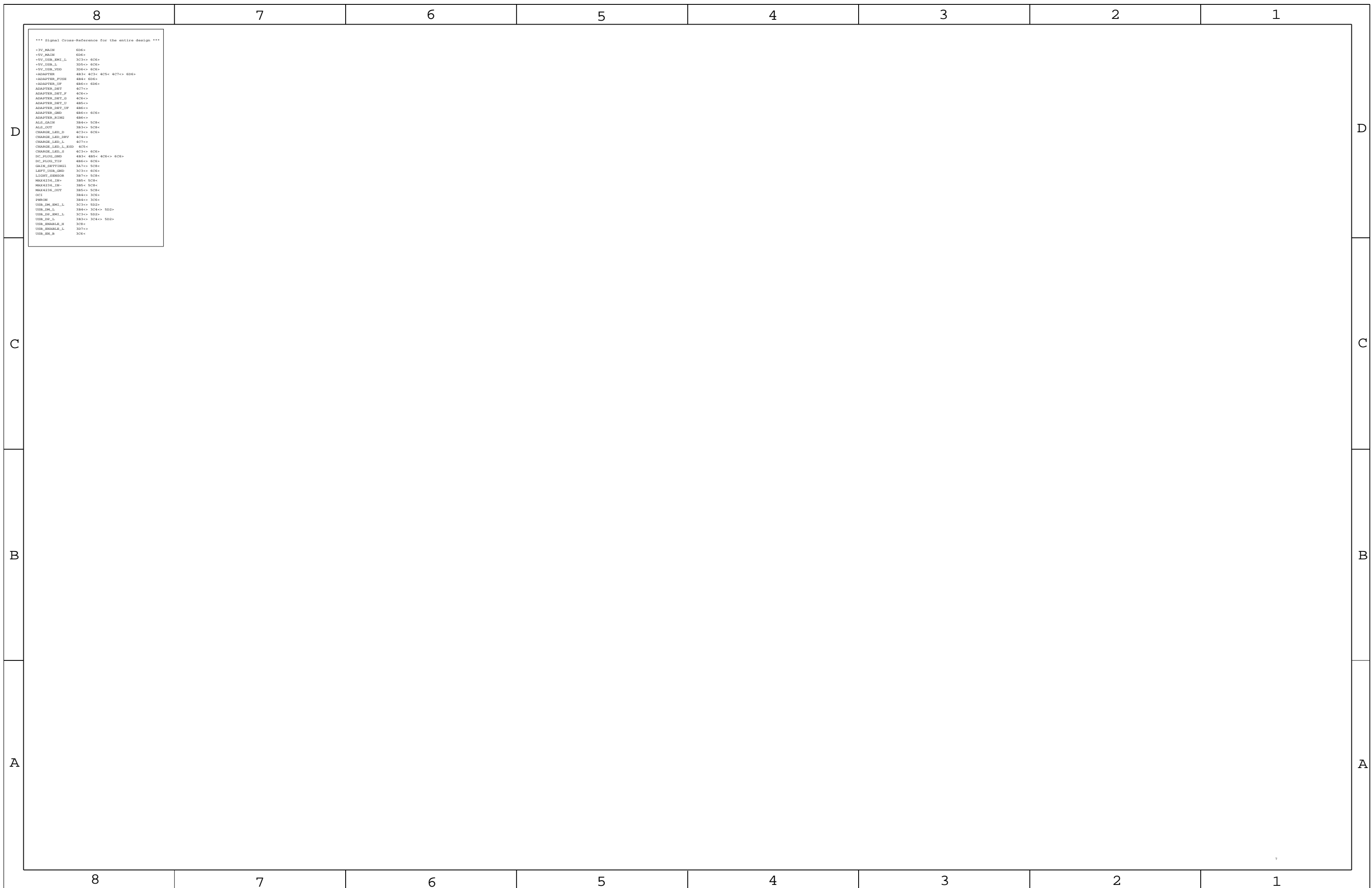
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SIZE D	DRAWING NUMBER 051-6474	REV. B
SCALE NONE	SHT 6	OF 8



\*\*\* Signal Cross-Reference for the entire design \*\*\*

+3V_MAIN	6D6>
+5V_MAIN	6D6>
+5V_USB_EMI_L	3C3<> 6C6>
+5V_USB_L	3D5<> 6C6>
+5V_USB_VDD	3D5<> 6C6>
*ADAPTER	4B3< 4C3< 4C5< 4C7<> 6D6>
+ADAPTER_FUSE	4B4< 6D6>
+ADAPTER_SF	4B6<> 6D6>
ADAPTER_DET	4C7<>
ADAPTER_DET_P	4C6<>
ADAPTER_DET_S	4C6<>
ADAPTER_DET_U	4B5<>
ADAPTER_DET_UP	4B6<>
ADAPTER_GND	4B6<> 6C6>
ADAPTER_RING	4B6<>
ALS_GAIN	3B4<> 5C8<
ALS_OUT	3B3<> 5C8<
CHANGE_LED_D	4C3<> 6C6>
CHANGE_LED_DRV	4C4<>
CHANGE_LED_L	4C7<>
CHANGE_LED_L_RSD	4C5<
CHANGE_LED_S	4C3<> 6C6>
DC_PLUG_GND	4B3< 4B5< 4C8<> 6C6>
DC_PLUG_TIP	4B6<> 6C6>
GAIN_SETTING1	3A7<> 5C8<
LEFT_USB_GND	3C3<> 6C6>
LIGHT_SENSOR	3B7<> 5C8<
MAX4236_IN+	3B5<> 5C8<
MAX4236_IN-	3B5<> 5C8<
MAX4236_OUT	3B5<> 5C8<
OC1	3B4<> 3D6>
PRSRGN	3B4<> 3C6<
USB_DM_EMI_L	3C3<> 5D2>
USB_DM_L	3B4<> 3C4<> 5D2>
USB_DP_EMI_L	3C3<> 5D2>
USB_DP_L	3B3<> 3C4<> 5D2>
USB_ENABLE_H	3C8<
USB_ENABLE_L	3D7<>
USB_EN_B	3C6<

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