1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J113 MLB SCHEMATIC
10/03/14

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00385	1	SCHEM,MLB,J43A	SCH	CRITICAL	
820-00165	1	PCBF,MLB,J43	PCB	CRITICAL	

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Oct 3 11:36:00 2014

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 121
SHEET: 1 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:PVT,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TBTHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS,SSD_LPSR:S3
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	XDP,SAMCONN
MLB_DEBUG:PVT	BKLT:PROD,XDP,SAMCONN,ISNS:ENG,DBGLED,XDP_CONN
MLB_DEBUG:PROD	BKLT:PROD,SAMCONN,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,PSVSS_ISNS:YES,A3PORT_ISNS:YES,SSD_ISNS:YES,LCDBKLT_ISNS:YES,P3V3SS_ISNS:YES,3V3SS_ISNS:YES,OTHER_HS_ISNS:YES,CAM_ISNS:YES,CPUDDR_ISNS:YES,PANEL_ISNS:YES
ISNS:PROD	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,PSVSS_ISNS:NO,A3PORT_ISNS:NO,SSD_ISNS:YES,LCDBKLT_ISNS:NO,P3V3SS_ISNS:NO,3V3SS_ISNS:NO,OTHER_HS_ISNS:NO,CAM_ISNS:NO,CPUDDR_ISNS:NO,PANEL_ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:MICRON_8GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:MICRON_8GB
DDR3:HYNIX_16GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_16GB
DDR3:SAMSUNG_16GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:SAMSUNG_16GB
DDR3:ELPIDA_16GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_16GB
DDR3:MICRON_16GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:MICRON_16GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0915	1	EEPROM,4MBIT,SPI,50MHZ,1.8V,USON8	U2890	CRITICAL	TBTROM:BLANK
341S00159	1	T29,EEPROM,FALCON RIDGE(V27.1), PROto 0,J110/J113	U2890	CRITICAL	TBTROM:PROG
338S1214	1	IC,SMC12-B1,40MHZ/50OMIPS MCU,157BGA	U5000	CRITICAL	SMC:BLANK
335S00006	1	IC,SERIAL FLASH,64 MBIT 3V,WSON,QE=1	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S00007	1	IC,SERIAL FLASH,64 MBIT 3V,WSON,QE=1	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S00153	1	IC,EFI ROM(V0108)), PROTO 0,J110/J113	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00029	1	BDW,QGH9,DD,1.8,15W,2+2,0.7,4M,BI16B	U0500	CRITICAL	CPU:2.1GHZ
337S00073	1	BDW,QGHB,DD,1.6,15W,2+2,0.6,4M,BI16B	U0500	CRITICAL	CPU:1.6GHZ
338S00069	1	IC,TBT,FR-2C,288,12x12 ,FC-CSP,TRAY	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2KFEB4G,S2 CMRA,8XB,208FCBGA	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J113_MLB
946-5477	1	UV GLUE,MLB,J41_J43	GLUE	CRITICAL	
825-7987	1	LABEL,MLB,J41/J43	NEW_LABEL		
376S00036	2	MOSFET,N-CH,30V,52A,5.9M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S00037	2	MOSFET,N-CH,30V,64A,3.5M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S00001	4	IC,SDRAM,23NM,8GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S00003	4	IC,SDRAM,23NM,16GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0793	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0791	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0793	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0791	4	IC,SDRAM,16GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_8GB
333S0789	4	IC,SDRAM,25nm,32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_16GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
4GB	0	0
8GB	0	1
16GB	1	0
RSVD	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Vale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	20Mhz Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S00014	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
870-5074	870-1938		ALL	ALT PDGQ PIN W_O CAP
860-3428	860-1327		ALL	ALT STANDOFF W_O MYLAR
333S0787	333S0677	DRAM_TYPE:HYNIX_4GB	ALL	ALT STANDOFF W_O MYLAR
860-3690	860-1328		ALL	ALT STANDOFF W_O MYLAR
333S0785	333S0681	DRAM_TYPE:HYNIX_8GB	ALL	ALT STANDOFF W_O MYLAR
353S3814	353S3812		ALL	ALT TBT PORT MUX
311S00008	311S0271		ALL	ALT AND GATE
311S00007	311S0426		ALL	ALT SNGL BUFFER
311S00015	311S0450		ALL	ALT 2-INPT AND
311S00013	311S0508		ALL	ALT SNGL BUFFER
311S00014	311S0515		ALL	ALT DUAL BUFFER
353S00133	353S2741		ALL	ALT PWR DIST SW

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 2 OF 121

SHEET 2 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00623	PCBA,MLB,BEST,HY-4GB,X430	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_4GB,ALTERNATE
639-00624	PCBA,MLB,BEST,HY-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_8GB,ALTERNATE
639-00625	PCBA,MLB,BEST,HY-16GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_16GB
639-00626	PCBA,MLB,BEST,SM-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_4GB,ALTERNATE
639-00627	PCBA,MLB,BEST,SM-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_8GB,ALTERNATE
639-00628	PCBA,MLB,BEST,MI-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_4GB
639-00629	PCBA,MLB,BEST,MI-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_8GB
639-00630	PCBA,MLB,BEST,MI-16GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_16GB
639-00631	PCBA,MLB,BEST,EL-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_4GB
639-00632	PCBA,MLB,BEST,EL-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_8GB
639-00633	PCBA,MLB,BETTER,HY-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_4GB,ALTERNATE
639-00634	PCBA,MLB,BETTER,HY-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_8GB,ALTERNATE
639-00635	PCBA,MLB,BETTER,HY-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_16GB
639-00636	PCBA,MLB,BETTER,SM-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_4GB,ALTERNATE
639-00637	PCBA,MLB,BETTER,SM-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_8GB,ALTERNATE
639-00638	PCBA,MLB,BETTER,MI-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_4GB
639-00639	PCBA,MLB,BETTER,MI-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_8GB
639-00640	PCBA,MLB,BETTER,MI-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_16GB
639-00641	PCBA,MLB,BETTER,EL-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_4GB
639-00642	PCBA,MLB,BETTER,EL-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_8GB
685-00046	CMN PTS,PCBA,MLB,X433	MLB_COMMON,J113_MLB
685-00047	VCORE FET,REN,X433	VCORE_FET:REN
685-00048	VCORE FET,VSHY,X433	VCORE_FET:VSHY
639-00697	PCBA,MLB,BETTER,EL-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_16GB

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00047	685-00048		ALL	Renesas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S1246	1	IC,GL3219,USB3 SD CARD READER,46P,LQFN	U4500	CRITICAL	

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00148	1	IC,SMC-B1,EXT(Vxxxx),PROTO 0,J113	U5000	CRITICAL	SMC:PROG

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00046	1	CMN PTS,PCBA,MLB,J113	CMNPTS	CRITICAL	MLB_CMNPTS
685-00048	1	VCORE FET,VSHY,J113	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

BOM Variants

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 3 OF 121

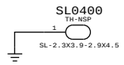
SHEET 3 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

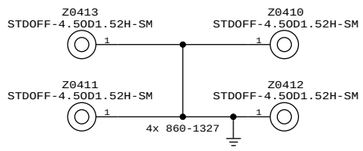
PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	

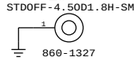
Plated Board Slot



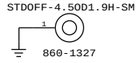
CPU Heat Sink Mounting Bosses



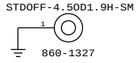
Fan Boss



X21 Boss



SSD Boss



EMI I/O Pogo Pins

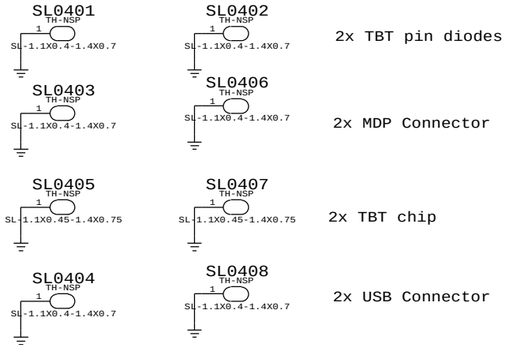
DisplayPort Pogo

CRITICAL

USB/SD Card Pogo

CRITICAL

Can Slots



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

PD PARTS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

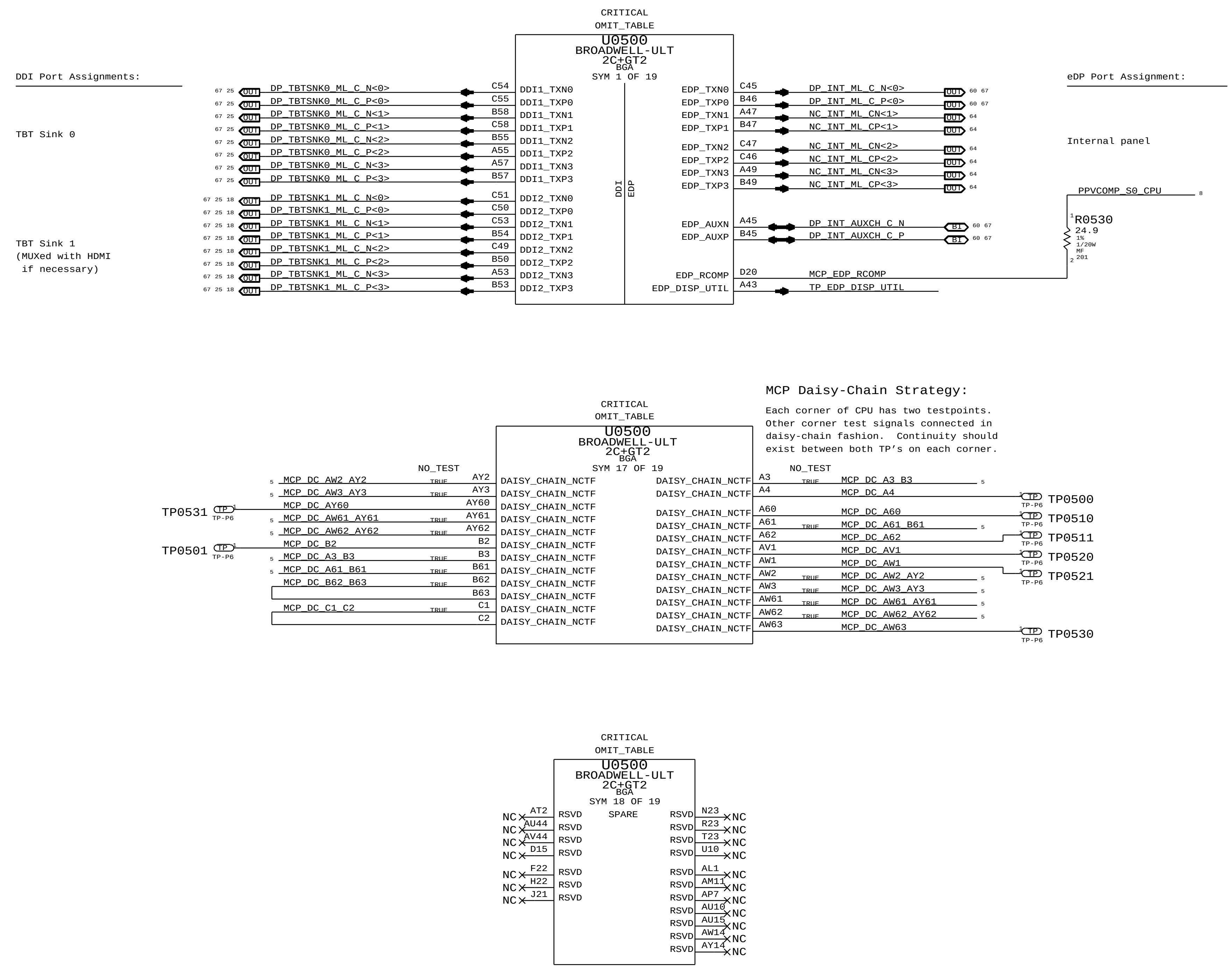
BRANCH <BRANCH>

PAGE 4 OF 121

SHEET 4 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


DDI Port Assignments:
TBT Sink 0
TBT Sink 1
(MUXed with HDMI
if necessary)
CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 1 OF 19
DDI
EDP
DP_TBTSNK0_ML_C_N<0>
DP_TBTSNK0_ML_C_P<0>
DP_TBTSNK0_ML_C_N<1>
DP_TBTSNK0_ML_C_P<1>
DP_TBTSNK0_ML_C_N<2>
DP_TBTSNK0_ML_C_P<2>
DP_TBTSNK0_ML_C_N<3>
DP_TBTSNK0_ML_C_P<3>
DP_TBTSNK1_ML_C_N<0>
DP_TBTSNK1_ML_C_P<0>
DP_TBTSNK1_ML_C_N<1>
DP_TBTSNK1_ML_C_P<1>
DP_TBTSNK1_ML_C_N<2>
DP_TBTSNK1_ML_C_P<2>
DP_TBTSNK1_ML_C_N<3>
DP_TBTSNK1_ML_C_P<3>
DDI1_TXN0 DDI1_TXP0 DDI1_TXN1 DDI1_TXP1 DDI1_TXN2 DDI1_TXP2 DDI1_TXN3 DDI1_TXP3
DDI2_TXN0 DDI2_TXP0 DDI2_TXN1 DDI2_TXP1 DDI2_TXN2 DDI2_TXP2 DDI2_TXN3 DDI2_TXP3
C54 C55 B58 C58 B55 A55 A57 B57 C51 C50 C53 B54 C49 B50 A53 B53
EDP_TXN0 EDP_TXP0 EDP_TXN1 EDP_TXP1 EDP_TXN2 EDP_TXP2 EDP_TXN3 EDP_TXP3
EDP_AUXN EDP_AUXP EDP_RCOMP EDP_DISP_UTIL
C45 B46 A47 B47 C47 C46 A49 B49 A45 B45 D20 A43
DP_INT_ML_C_N<0>
DP_INT_ML_C_P<0>
NC_INT_ML_CN<1>
NC_INT_ML_CP<1>
NC_INT_ML_CN<2>
NC_INT_ML_CP<2>
NC_INT_ML_CN<3>
NC_INT_ML_CP<3>
DP_INT_AUXCH_C_N
DP_INT_AUXCH_C_P
MCP_EDP_RCOMP
TP_EDP_DISP_UTIL
eDP Port Assignment:
Internal panel
PPVCOMP_S0_CPU
R0530
24.9
1%
1/20W
MF
201
MCP Daisy-Chain Strategy:
Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.
CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 17 OF 19
NO_TEST
DAISY_CHAIN_NCTF
MCP_DC_AW2_AY2
MCP_DC_AW3_AY3
MCP_DC_AY60
MCP_DC_AW61_AY61
MCP_DC_AW62_AY62
MCP_DC_B2
MCP_DC_A3_B3
MCP_DC_A61_B61
MCP_DC_B62_B63
MCP_DC_C1_C2
AY2 AY3 AY60 AY61 AY62 B2 B3 B61 B62 B63 C1 C2
TP0531
TP0501
TP-P6
A3 A4 A60 A61 A62 AV1 AW1 AW2 AW3 AW61 AW62 AW63
MCP_DC_A4
MCP_DC_A60
MCP_DC_A62
MCP_DC_AV1
MCP_DC_AW1
MCP_DC_AW63
TP0500
TP0510
TP0511
TP0520
TP0521
TP0530
CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 18 OF 19
SPARE
RSVD
AT2 AU44 AV44 D15 F22 H22 J21
N23 R23 T23 U10 AL1 AM11 AP7 AU10 AU15 AW14 AY14
NC

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE

CPU GFX/NCTF/RSVD

Apple Inc.

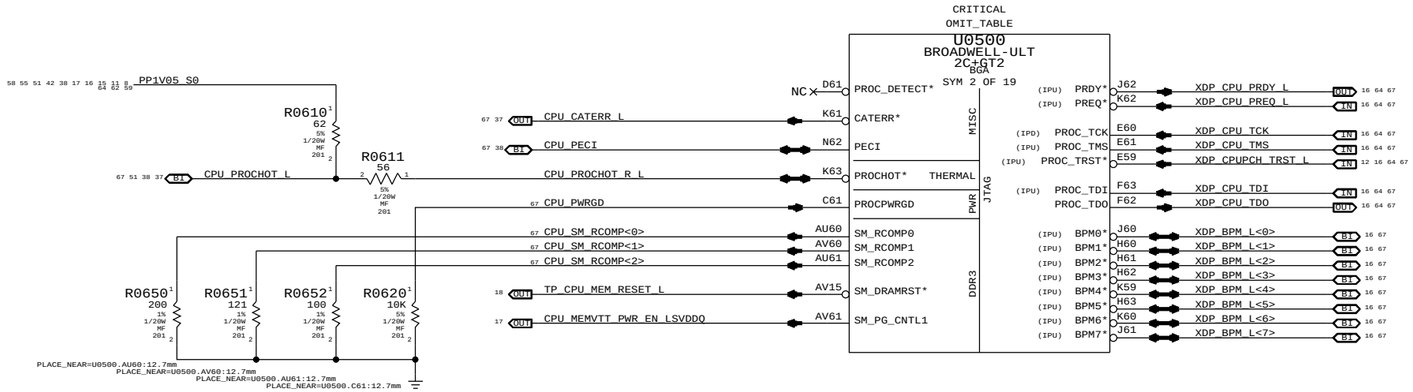
DRAWING NUMBER <SCH_NUM> SIZE D

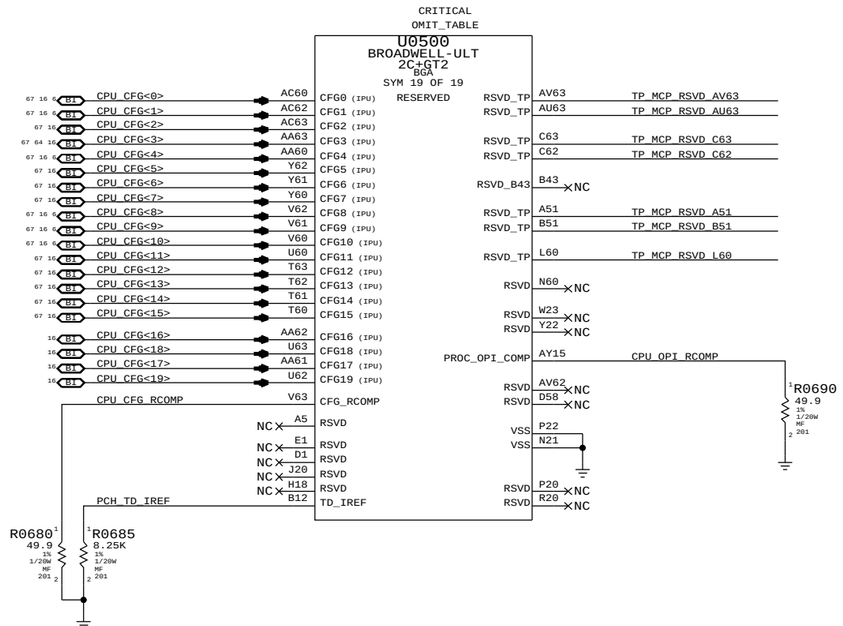
REVISION <E4LABEL>

BRANCH <BRANCH>

NOTICE OF PROPRIETARY PROPERTY:

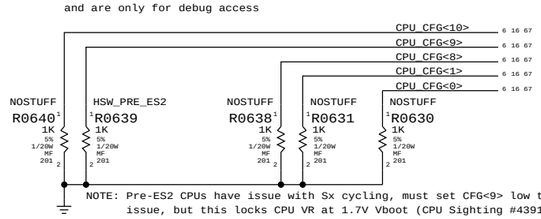
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



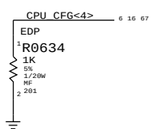


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE

CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

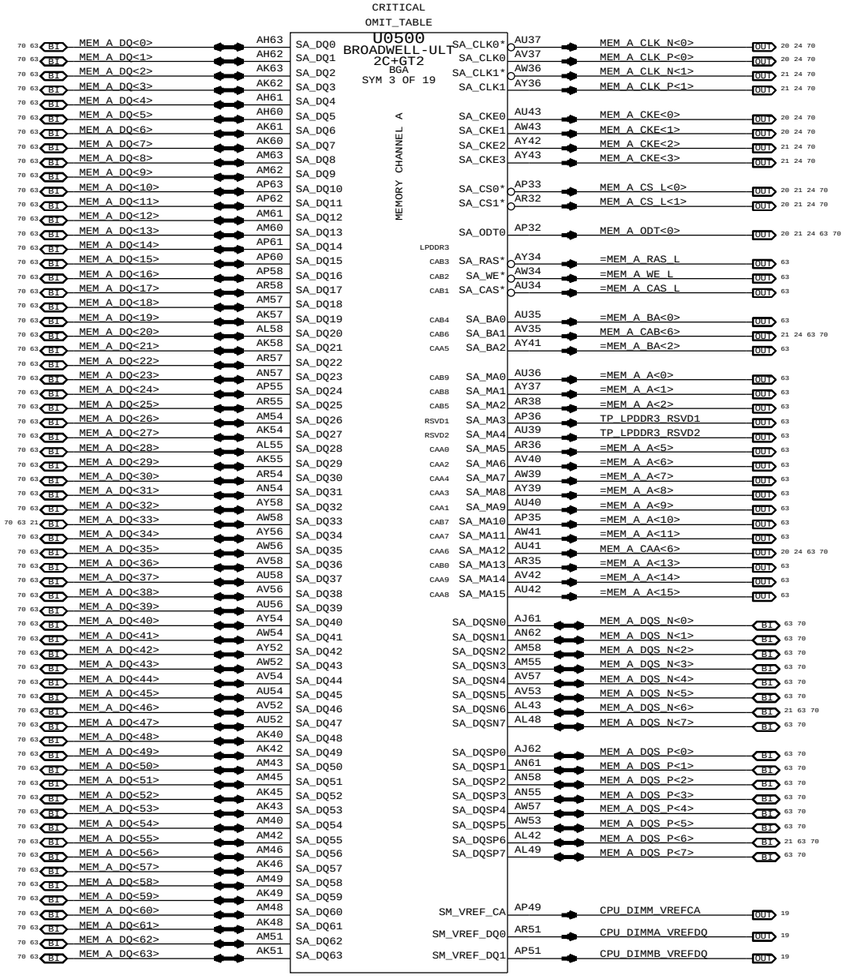
BRANCH <BRANCH>

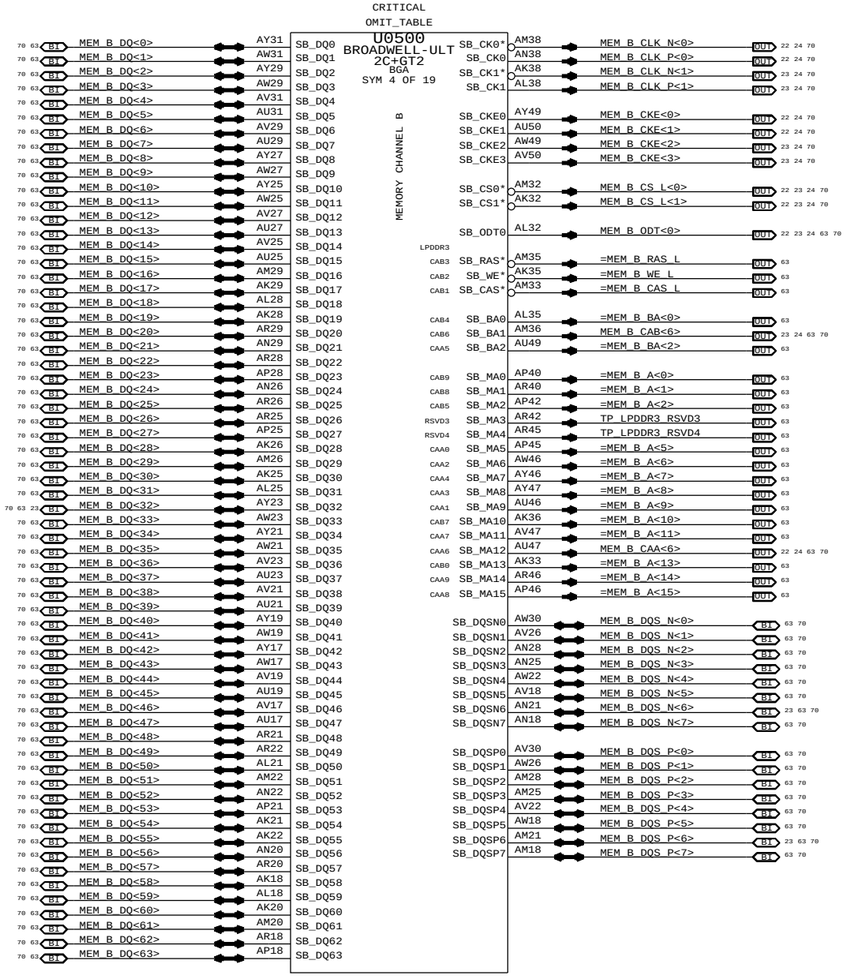
PAGE 6 OF 121

SHEET 6 OF 76

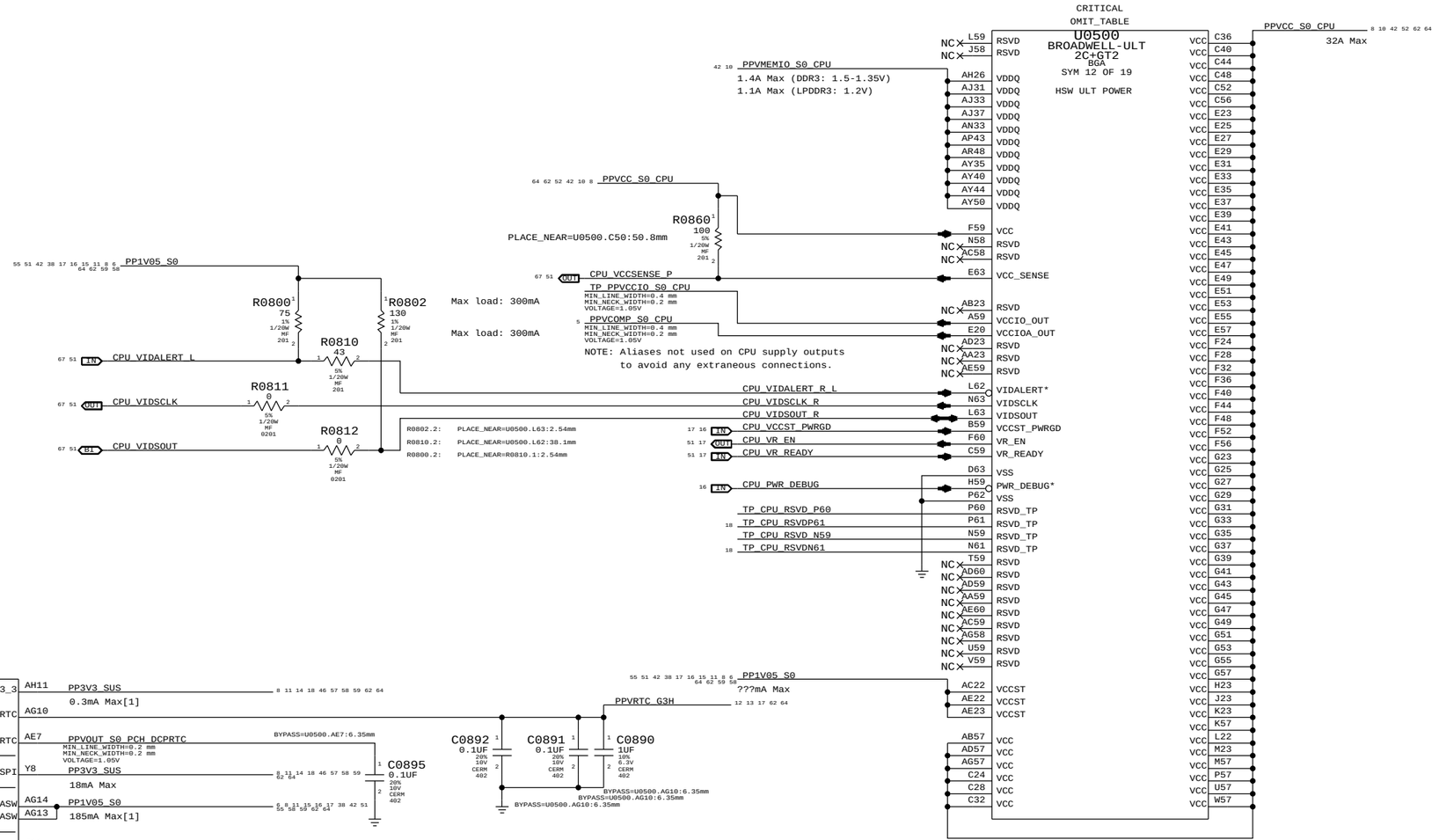
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 3 OF 19
MEMORY CHANNEL A
SA_DQ0 SA_DQ1 SA_DQ2 SA_DQ3 SA_DQ4 SA_DQ5 SA_DQ6 SA_DQ7 SA_DQ8 SA_DQ9 SA_DQ10 SA_DQ11 SA_DQ12 SA_DQ13 SA_DQ14 SA_DQ15 SA_DQ16 SA_DQ17 SA_DQ18 SA_DQ19 SA_DQ20 SA_DQ21 SA_DQ22 SA_DQ23 SA_DQ24 SA_DQ25 SA_DQ26 SA_DQ27 SA_DQ28 SA_DQ29 SA_DQ30 SA_DQ31 SA_DQ32 SA_DQ33 SA_DQ34 SA_DQ35 SA_DQ36 SA_DQ37 SA_DQ38 SA_DQ39 SA_DQ40 SA_DQ41 SA_DQ42 SA_DQ43 SA_DQ44 SA_DQ45 SA_DQ46 SA_DQ47 SA_DQ48 SA_DQ49 SA_DQ50 SA_DQ51 SA_DQ52 SA_DQ53 SA_DQ54 SA_DQ55 SA_DQ56 SA_DQ57 SA_DQ58 SA_DQ59 SA_DQ60 SA_DQ61 SA_DQ62 SA_DQ63
MEM_A_DQ<0> MEM_A_DQ<1> MEM_A_DQ<2> MEM_A_DQ<3> MEM_A_DQ<4> MEM_A_DQ<5> MEM_A_DQ<6> MEM_A_DQ<7> MEM_A_DQ<8> MEM_A_DQ<9> MEM_A_DQ<10> MEM_A_DQ<11> MEM_A_DQ<12> MEM_A_DQ<13> MEM_A_DQ<14> MEM_A_DQ<15> MEM_A_DQ<16> MEM_A_DQ<17> MEM_A_DQ<18> MEM_A_DQ<19> MEM_A_DQ<20> MEM_A_DQ<21> MEM_A_DQ<22> MEM_A_DQ<23> MEM_A_DQ<24> MEM_A_DQ<25> MEM_A_DQ<26> MEM_A_DQ<27> MEM_A_DQ<28> MEM_A_DQ<29> MEM_A_DQ<30> MEM_A_DQ<31> MEM_A_DQ<32> MEM_A_DQ<33> MEM_A_DQ<34> MEM_A_DQ<35> MEM_A_DQ<36> MEM_A_DQ<37> MEM_A_DQ<38> MEM_A_DQ<39> MEM_A_DQ<40> MEM_A_DQ<41> MEM_A_DQ<42> MEM_A_DQ<43> MEM_A_DQ<44> MEM_A_DQ<45> MEM_A_DQ<46> MEM_A_DQ<47> MEM_A_DQ<48> MEM_A_DQ<49> MEM_A_DQ<50> MEM_A_DQ<51> MEM_A_DQ<52> MEM_A_DQ<53> MEM_A_DQ<54> MEM_A_DQ<55> MEM_A_DQ<56> MEM_A_DQ<57> MEM_A_DQ<58> MEM_A_DQ<59> MEM_A_DQ<60> MEM_A_DQ<61> MEM_A_DQ<62> MEM_A_DQ<63>
SA_CLK0* SA_CLK0 SA_CLK1* SA_CLK1 SA_CKE0 SA_CKE1 SA_CKE2 SA_CKE3 SA_CS0* SA_CS1* SA_ODT0 SA_RAS* SA_WE* SA_CAS* SA_BA0 SA_BA1 SA_BA2 SA_MA0 SA_MA1 SA_MA2 SA_MA3 SA_MA4 SA_MA5 SA_MA6 SA_MA7 SA_MA8 SA_MA9 SA_MA10 SA_MA11 SA_MA12 SA_MA13 SA_MA14 SA_MA15 SA_DQSN0 SA_DQSN1 SA_DQSN2 SA_DQSN3 SA_DQSN4 SA_DQSN5 SA_DQSN6 SA_DQSN7 SA_DQSP0 SA_DQSP1 SA_DQSP2 SA_DQSP3 SA_DQSP4 SA_DQSP5 SA_DQSP6 SA_DQSP7
MEM_A_CLK_N<0> MEM_A_CLK_P<0> MEM_A_CLK_N<1> MEM_A_CLK_P<1> MEM_A_CKE<0> MEM_A_CKE<1> MEM_A_CKE<2> MEM_A_CKE<3> MEM_A_CS_L<0> MEM_A_CS_L<1> MEM_A_ODT<0> =MEM_A_RAS_L =MEM_A_WE_L =MEM_A_CAS_L =MEM_A_BA<0> MEM_A_CAB<6> =MEM_A_BA<2> =MEM_A_A<0> =MEM_A_A<1> =MEM_A_A<2> TP_LPDDR3_RSVD1 TP_LPDDR3_RSVD2 =MEM_A_A<5> =MEM_A_A<6> =MEM_A_A<7> =MEM_A_A<8> =MEM_A_A<9> =MEM_A_A<10> =MEM_A_A<11> MEM_A_CAA<6> =MEM_A_A<13> =MEM_A_A<14> =MEM_A_A<15> MEM_A_DQS_N<0> MEM_A_DQS_N<1> MEM_A_DQS_N<2> MEM_A_DQS_N<3> MEM_A_DQS_N<4> MEM_A_DQS_N<5> MEM_A_DQS_N<6> MEM_A_DQS_N<7> MEM_A_DQS_P<0> MEM_A_DQS_P<1> MEM_A_DQS_P<2> MEM_A_DQS_P<3> MEM_A_DQS_P<4> MEM_A_DQS_P<5> MEM_A_DQS_P<6> MEM_A_DQS_P<7>
SM_VREF_CA SM_VREF_DQ0 SM_VREF_DQ1
CPU_DIMM_VREFCA CPU_DIMMA_VREFDQ CPU_DIMMB_VREFDQ


CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 4 OF 19
MEMORY CHANNEL B
SB_DQ0 SB_DQ1 SB_DQ2 SB_DQ3 SB_DQ4 SB_DQ5 SB_DQ6 SB_DQ7 SB_DQ8 SB_DQ9 SB_DQ10 SB_DQ11 SB_DQ12 SB_DQ13 SB_DQ14 SB_DQ15 SB_DQ16 SB_DQ17 SB_DQ18 SB_DQ19 SB_DQ20 SB_DQ21 SB_DQ22 SB_DQ23 SB_DQ24 SB_DQ25 SB_DQ26 SB_DQ27 SB_DQ28 SB_DQ29 SB_DQ30 SB_DQ31 SB_DQ32 SB_DQ33 SB_DQ34 SB_DQ35 SB_DQ36 SB_DQ37 SB_DQ38 SB_DQ39 SB_DQ40 SB_DQ41 SB_DQ42 SB_DQ43 SB_DQ44 SB_DQ45 SB_DQ46 SB_DQ47 SB_DQ48 SB_DQ49 SB_DQ50 SB_DQ51 SB_DQ52 SB_DQ53 SB_DQ54 SB_DQ55 SB_DQ56 SB_DQ57 SB_DQ58 SB_DQ59 SB_DQ60 SB_DQ61 SB_DQ62 SB_DQ63
MEM_B_DQ<0> MEM_B_DQ<1> MEM_B_DQ<2> MEM_B_DQ<3> MEM_B_DQ<4> MEM_B_DQ<5> MEM_B_DQ<6> MEM_B_DQ<7> MEM_B_DQ<8> MEM_B_DQ<9> MEM_B_DQ<10> MEM_B_DQ<11> MEM_B_DQ<12> MEM_B_DQ<13> MEM_B_DQ<14> MEM_B_DQ<15> MEM_B_DQ<16> MEM_B_DQ<17> MEM_B_DQ<18> MEM_B_DQ<19> MEM_B_DQ<20> MEM_B_DQ<21> MEM_B_DQ<22> MEM_B_DQ<23> MEM_B_DQ<24> MEM_B_DQ<25> MEM_B_DQ<26> MEM_B_DQ<27> MEM_B_DQ<28> MEM_B_DQ<29> MEM_B_DQ<30> MEM_B_DQ<31> MEM_B_DQ<32> MEM_B_DQ<33> MEM_B_DQ<34> MEM_B_DQ<35> MEM_B_DQ<36> MEM_B_DQ<37> MEM_B_DQ<38> MEM_B_DQ<39> MEM_B_DQ<40> MEM_B_DQ<41> MEM_B_DQ<42> MEM_B_DQ<43> MEM_B_DQ<44> MEM_B_DQ<45> MEM_B_DQ<46> MEM_B_DQ<47> MEM_B_DQ<48> MEM_B_DQ<49> MEM_B_DQ<50> MEM_B_DQ<51> MEM_B_DQ<52> MEM_B_DQ<53> MEM_B_DQ<54> MEM_B_DQ<55> MEM_B_DQ<56> MEM_B_DQ<57> MEM_B_DQ<58> MEM_B_DQ<59> MEM_B_DQ<60> MEM_B_DQ<61> MEM_B_DQ<62> MEM_B_DQ<63>
SB_CK0* SB_CK0 SB_CK1* SB_CK1 SB_CKE0 SB_CKE1 SB_CKE2 SB_CKE3 SB_CS0* SB_CS1* SB_ODT0 SB_RAS* SB_WE* SB_CAS* SB_BA0 SB_BA1 SB_BA2 SB_MA0 SB_MA1 SB_MA2 SB_MA3 SB_MA4 SB_MA5 SB_MA6 SB_MA7 SB_MA8 SB_MA9 SB_MA10 SB_MA11 SB_MA12 SB_MA13 SB_MA14 SB_MA15 SB_DQSN0 SB_DQSN1 SB_DQSN2 SB_DQSN3 SB_DQSN4 SB_DQSN5 SB_DQSN6 SB_DQSN7 SB_DQSP0 SB_DQSP1 SB_DQSP2 SB_DQSP3 SB_DQSP4 SB_DQSP5 SB_DQSP6 SB_DQSP7
MEM_B_CLK_N<0> MEM_B_CLK_P<0> MEM_B_CLK_N<1> MEM_B_CLK_P<1> MEM_B_CKE<0> MEM_B_CKE<1> MEM_B_CKE<2> MEM_B_CKE<3> MEM_B_CS_L<0> MEM_B_CS_L<1> MEM_B_ODT<0> =MEM_B_RAS_L =MEM_B_WE_L =MEM_B_CAS_L =MEM_B_BA<0> MEM_B_CAB<6> =MEM_B_BA<2> =MEM_B_A<0> =MEM_B_A<1> =MEM_B_A<2> TP_LPDDR3_RSVD3 TP_LPDDR3_RSVD4 =MEM_B_A<5> =MEM_B_A<6> =MEM_B_A<7> =MEM_B_A<8> =MEM_B_A<9> =MEM_B_A<10> =MEM_B_A<11> MEM_B_CAA<6> =MEM_B_A<13> =MEM_B_A<14> =MEM_B_A<15> MEM_B_DQS_N<0> MEM_B_DQS_N<1> MEM_B_DQS_N<2> MEM_B_DQS_N<3> MEM_B_DQS_N<4> MEM_B_DQS_N<5> MEM_B_DQS_N<6> MEM_B_DQS_N<7> MEM_B_DQS_P<0> MEM_B_DQS_P<1> MEM_B_DQS_P<2> MEM_B_DQS_P<3> MEM_B_DQS_P<4> MEM_B_DQS_P<5> MEM_B_DQS_P<6> MEM_B_DQS_P<7>
SYNC_MASTER=WILL J43
SYNC_DATE=09/13/2012
PAGE TITLE
CPU DDR3/LPDDR3 Interfaces
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
7 OF 121
SHEET
7 OF 76
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J43_MLB	SYNC_DATE=10/02/2012
PAGE TITLE	CPU/PCH POWER
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 8 OF 121
	SHEET 8 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N
OUT 51 67

R0960
100
5%
1/20W
MF
201
2 1

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 9 OF 121
SHEET 9 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

64 62 52 42 8 PPVCC_S0_CPU

CRITICAL C1000 10UF 20% 4V X6S 0402
CRITICAL C1001 10UF 20% 4V X6S 0402
CRITICAL C1002 10UF 20% 4V X6S 0402
NO STUFF C1003 10UF 20% 4V X6S 0402
CRITICAL C1004 10UF 20% 4V X6S 0402
NO STUFF C1005 10UF 20% 4V X6S 0402
NO STUFF C1006 10UF 20% 4V X6S 0402
CRITICAL C1007 10UF 20% 4V X6S 0402
NO STUFF C1008 10UF 20% 4V X6S 0402
NO STUFF C1009 10UF 20% 4V X6S 0402
CRITICAL C1010 10UF 20% 4V X6S 0402
NO STUFF C1011 10UF 20% 4V X6S 0402
CRITICAL C1012 10UF 20% 4V X6S 0402
NO STUFF C1013 10UF 20% 4V X6S 0402
CRITICAL C1014 10UF 20% 4V X6S 0402
NO STUFF C105A 10UF 20% 4V X6S 0402
NO STUFF C105B 10UF 20% 4V X6S 0402
NO STUFF C105C 10UF 20% 4V X6S 0402
NO STUFF C105D 10UF 20% 4V X6S 0402
NO STUFF C105E 10UF 20% 4V X6S 0402
NO STUFF C105F 10UF 20% 4V X6S 0402

NO STUFF C1015 10UF 20% 4V X6S 0402
CRITICAL C1016 10UF 20% 4V X6S 0402
CRITICAL C1017 10UF 20% 4V X6S 0402
CRITICAL C1018 10UF 20% 4V X6S 0402
NO STUFF C1019 10UF 20% 4V X6S 0402
NO STUFF C1020 10UF 20% 4V X6S 0402
CRITICAL C1021 10UF 20% 4V X6S 0402
NO STUFF C1030 10UF 20% 4V X6S 0402
NO STUFF C104A 10UF 20% 4V X6S 0402
NO STUFF C104B 10UF 20% 4V X6S 0402
NO STUFF C104C 10UF 20% 4V X6S 0402
NO STUFF C104D 10UF 20% 4V X6S 0402
NO STUFF C104E 10UF 20% 4V X6S 0402
NO STUFF C104F 10UF 20% 4V X6S 0402
NO STUFF C106A 10UF 20% 4V X6S 0402
NO STUFF C106B 10UF 20% 4V X6S 0402
NO STUFF C106C 10UF 20% 4V X6S 0402
NO STUFF C106D 10UF 20% 4V X6S 0402
NO STUFF C106E 10UF 20% 4V X6S 0402

NO STUFF C1070 10UF 20% 4V X6S 0402
NO STUFF C1071 10UF 20% 4V X6S 0402
NO STUFF C1072 10UF 20% 4V X6S 0402
NO STUFF C1073 10UF 20% 4V X6S 0402
NO STUFF C1074 10UF 20% 4V X6S 0402
NO STUFF C1075 10UF 20% 4V X6S 0402
CRITICAL C1076 10UF 20% 4V X6S 0402
CRITICAL C1077 10UF 20% 4V X6S 0402
NO STUFF C1078 10UF 20% 4V X6S 0402
NO STUFF C1079 10UF 20% 4V X6S 0402
NO STUFF C1080 10UF 20% 4V X6S 0402
NO STUFF C1081 10UF 20% 4V X6S 0402
NO STUFF C1082 10UF 20% 4V X6S 0402
CRITICAL C1083 10UF 20% 4V X6S 0402
CRITICAL C1084 10UF 20% 4V X6S 0402

NO STUFF C1085 10UF 20% 4V X6S 0402
NO STUFF C1086 10UF 20% 4V X6S 0402
NO STUFF C1087 10UF 20% 4V X6S 0402
CRITICAL C1088 10UF 20% 4V X6S 0402
CRITICAL C1089 10UF 20% 4V X6S 0402
NO STUFF C1090 10UF 20% 4V X6S 0402
NO STUFF C1091 10UF 20% 4V X6S 0402
NO STUFF C1092 10UF 20% 4V X6S 0402
NO STUFF C1093 10UF 20% 4V X6S 0402
NO STUFF C1094 10UF 20% 4V X6S 0402
NO STUFF C1095 10UF 20% 4V X6S 0402
NO STUFF C1096 10UF 20% 4V X6S 0402
NO STUFF C1097 10UF 20% 4V X6S 0402

NO STUFF C1022 10UF 20% 4V X6S 0402
NO STUFF C1023 10UF 20% 4V X6S 0402
NO STUFF C1024 10UF 20% 4V X6S 0402
NO STUFF C1025 10UF 20% 4V X6S 0402
NO STUFF C1026 10UF 20% 4V X6S 0402
NO STUFF C1027 10UF 20% 4V X6S 0402
NO STUFF C1028 10UF 20% 4V X6S 0402
NO STUFF C1029 10UF 20% 4V X6S 0402
NO STUFF C1032 10UF 20% 4V X6S 0402
NO STUFF C1033 10UF 20% 4V X6S 0402
NO STUFF C1034 10UF 20% 4V X6S 0402
NO STUFF C1035 10UF 20% 4V X6S 0402
NO STUFF C1036 10UF 20% 4V X6S 0402
NO STUFF C1037 10UF 20% 4V X6S 0402
NO STUFF C1038 10UF 20% 4V X6S 0402

NO STUFF C1039 10UF 20% 4V X6S 0402
NO STUFF C1044 10UF 20% 4V X6S 0402
NO STUFF C1045 10UF 20% 4V X6S 0402
NO STUFF C1046 10UF 20% 4V X6S 0402
NO STUFF C1047 10UF 20% 4V X6S 0402
NO STUFF C1048 10UF 20% 4V X6S 0402
NO STUFF C1049 10UF 20% 4V X6S 0402

NO STUFF C1056 10UF 20% 4V X6S 0402
NO STUFF C1057 10UF 20% 4V X6S 0402
NO STUFF C1058 10UF 20% 4V X6S 0402
NO STUFF C1059 10UF 20% 4V X6S 0402
NO STUFF C1062 10UF 20% 4V X6S 0402
NO STUFF C1063 10UF 20% 4V X6S 0402
NO STUFF C1064 10UF 20% 4V X6S 0402
NO STUFF C1065 10UF 20% 4V X6S 0402
NO STUFF C1066 10UF 20% 4V X6S 0402
NO STUFF C1067 10UF 20% 4V X6S 0402
NO STUFF C1068 10UF 20% 4V X6S 0402
NO STUFF C1069 10UF 20% 4V X6S 0402
NO STUFF C1098 10UF 20% 4V X6S 0402
NO STUFF C1099 10UF 20% 4V X6S 0402
NO STUFF C109A 10UF 20% 4V X6S 0402

NO STUFF C109B 10UF 20% 4V X6S 0402
NO STUFF C109C 10UF 20% 4V X6S 0402
NO STUFF C109D 10UF 20% 4V X6S 0402
NO STUFF C109E 10UF 20% 4V X6S 0402
NO STUFF C109F 10UF 20% 4V X6S 0402
NO STUFF C108A 10UF 20% 4V X6S 0402
NO STUFF C108B 10UF 20% 4V X6S 0402
NO STUFF C108C 10UF 20% 4V X6S 0402
NO STUFF C108D 10UF 20% 4V X6S 0402
NO STUFF C108E 10UF 20% 4V X6S 0402
NO STUFF C108F 10UF 20% 4V X6S 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

42 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM
NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

2x Bulk nostuff per Harris Beach v1.0 schematic

SYNC_MASTER=WILL_J43 SYNC_DATE=01/08/2013
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 10 OF 121
SHEET: 10 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
42 34 29 28 18 17 16 15 13 8 74 64 62 60 59 58 57
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
64 62 59 58 57 46 18 14 11 8
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500.Y8:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
64 62 59 58 57 46 18 14 11 8
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9:12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
64 62 59 58 57 46 18 14 11 8
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11:6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
74 65 64 62 61 36 30 26 18 17 15 11 12 11 9 59 56 45 44 43 42 41 40 39 38
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA
58 17 8
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
74 65 64 62 61 36 30 26 18 17 15 11 12 11 9 59 56 45 44 43 42 41 40 39 38
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8:12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
74 65 64 62 61 36 30 26 18 17 15 11 12 11 9 59 56 45 44 43 42 41 40 39 38
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.K14:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
55 51 42 38 17 16 15 11 8 6 64 62 59 58
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AE9:12.7mm
BYPASS=U0500.AE9:6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
55 51 42 38 17 16 15 11 8 6 64 62 59 58
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11:12.7mm
BYPASS=U0500.J11:6.35mm
BYPASS=U0500.AE8:6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO
62 58 11 8
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9:6.35mm
BYPASS=U0500.L10:6.35mm
BYPASS=U0500.M9:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
55 51 42 38 17 16 15 11 8 6 64 62 59 58
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
55 51 42 38 17 16 15 11 8 6 64 62 59 58
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17:6.35mm
BYPASS=U0500.R21:6.35mm

PP1V05_S0
55 51 42 38 17 16 15 11 8 6 64 62 59 58
??mA Max
R1270 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:12.7mm
BYPASS=U0500.A20:6.35mm
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
8 12
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

R1275 0 5% 1/10W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:12.7mm
BYPASS=U0500.J18:6.35mm
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
8
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

R1280 0 5% 1/10W MF-LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
NO STUFF C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:12.7mm
BYPASS=U0500.AA21:6.35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
8
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

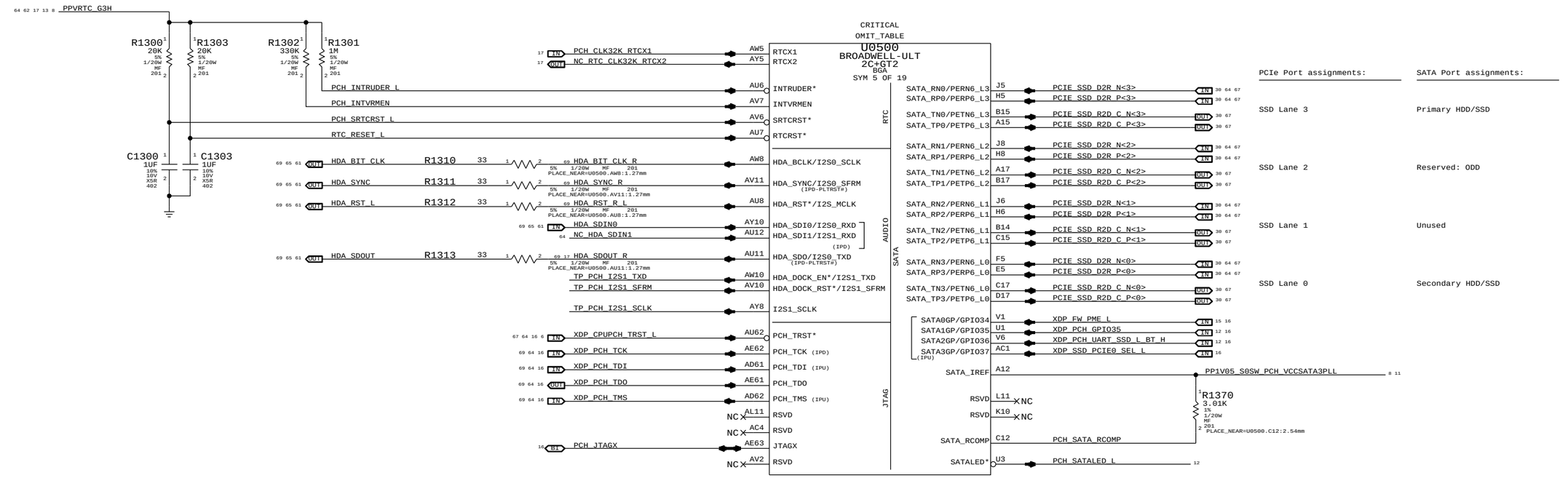
PP1V05_S0SW_PCH_HSIO
62 58 11 8
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
NO STUFF C1290 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:12.7mm
BYPASS=U0500.B11:6.35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
8 12
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

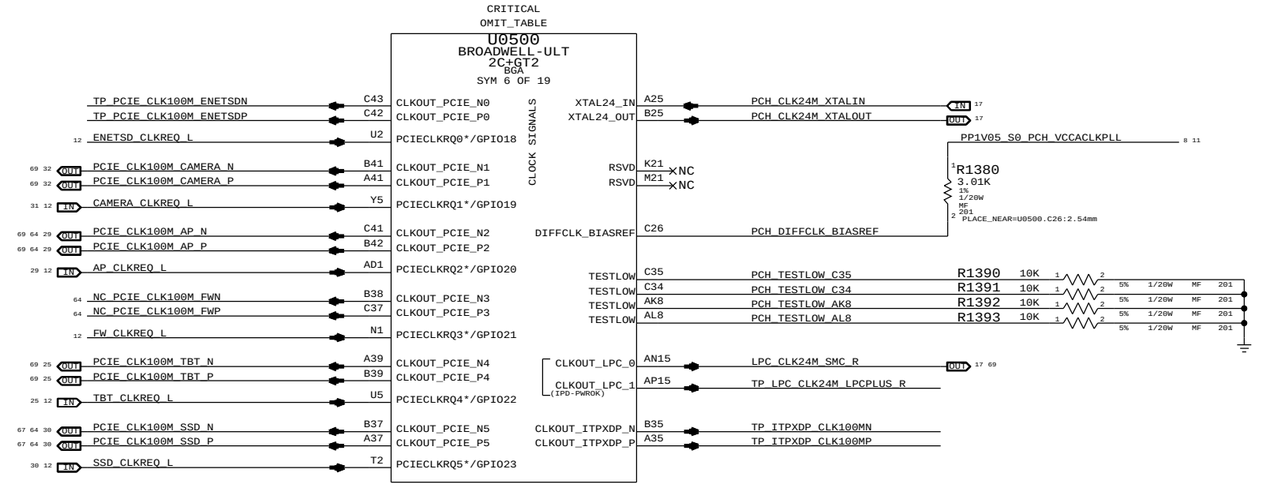
CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
NO STUFF C1295 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:12.7mm
BYPASS=U0500.B18:6.35mm
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
8 14
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

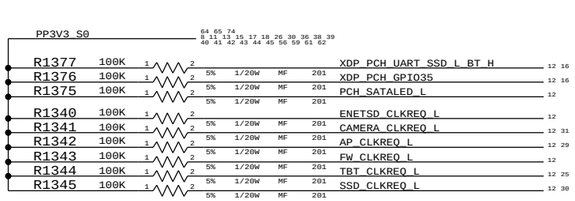
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J41_MLB SYNC_DATE=02/07/2013
PAGE TITLE
PCH Decoupling
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 12 OF 121
SHEET 11 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED







SYNC MASTER=WILL_J43 SYNC DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

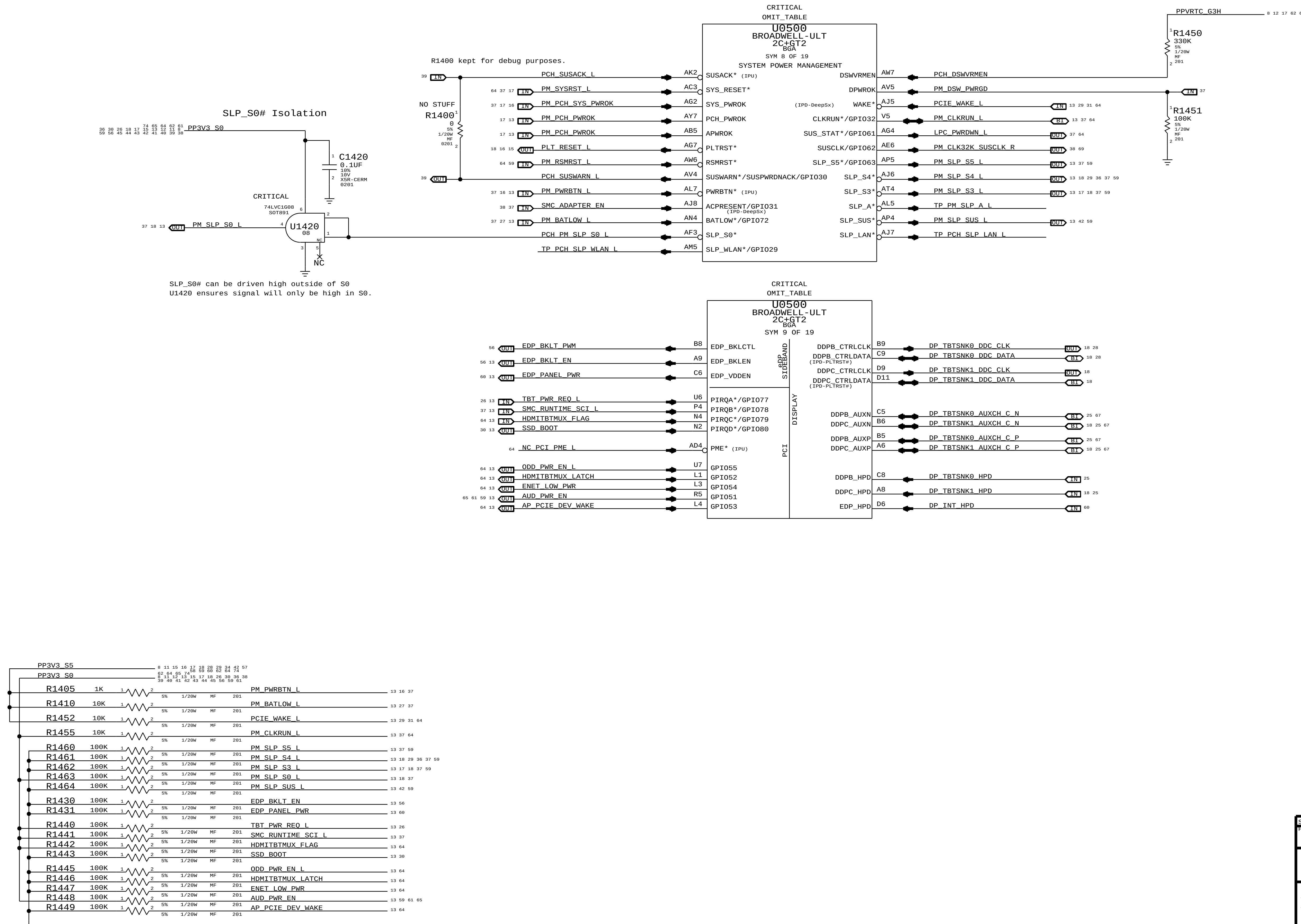
BRANCH <BRANCH>

PAGE 13 OF 121

SHEET 12 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 8 OF 19
SYSTEM POWER MANAGEMENT
R1400 kept for debug purposes.
NO STUFF
R1400
SLP_S0# Isolation
PP3V3_S0
C1420
0.1UF
CRITICAL
74LVC1G08
SOT891
U1420
PM_SLP_S0_L
NC
SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.
PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PLT_RESET_L
PM_RSMRST_L
PCH_SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_PM_SLP_S0_L
TP_PCH_SLP_WLAN_L
SUSACK*
SYS_RESET*
SYS_PWROK
PCH_PWROK
APWROK
PLTRST*
RSMRST*
SUSWARN*/SUSPWRDNACK/GPIO30
PWRBTN*
ACPRESENT/GPIO31
BATLOW*/GPIO72
SLP_S0*
SLP_WLAN*/GPIO29
DSWVRMEN
DPWROK
WAKE*
CLKRUN*/GPIO32
SUS_STAT*/GPIO61
SUSCLK/GPIO62
SLP_S5*/GPIO63
SLP_S4*
SLP_S3*
SLP_A*
SLP_SUS*
SLP_LAN*
PCH_DSWVRMEN
PM_DSW_PWRGD
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
TP_PCH_SLP_LAN_L
PPVRTC_G3H
R1450
330K
R1451
100K
SYM 9 OF 19
EDP_BKLT_PWM
EDP_BKLT_EN
EDP_PANEL_PWR
TBT_PWR_REQ_L
SMC_RUNTIME_SCI_L
HDMITBTMUX_FLAG
SSD_BOOT
NC_PCI_PME_L
ODD_PWR_EN_L
HDMITBTMUX_LATCH
ENET_LOW_PWR
AUD_PWR_EN
AP_PCIE_DEV_WAKE
EDP_BKLTCTL
EDP_BKLEN
EDP_VDDEN
PIRQA*/GPIO77
PIRQB*/GPIO78
PIRQC*/GPIO79
PIRQD*/GPIO80
PME*
GPIO55
GPIO52
GPIO54
GPIO51
GPIO53
eDP SIDEBAND
DISPLAY
PCI
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPB_AUXN
DDPC_AUXN
DDPB_AUXP
DDPC_AUXP
DDPB_HPD
DDPC_HPD
EDP_HPD
DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA
DP_TBTSNK0_AUXCH_C_N
DP_TBTSNK1_AUXCH_C_N
DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK0_HPD
DP_TBTSNK1_HPD
DP_INT_HPD
PP3V3_S5
PP3V3_S0
R1405 1K PM_PWRBTN_L
R1410 10K PM_BATLOW_L
R1452 10K PCIE_WAKE_L
R1455 10K PM_CLKRUN_L
R1460 100K PM_SLP_S5_L
R1461 100K PM_SLP_S4_L
R1462 100K PM_SLP_S3_L
R1463 100K PM_SLP_S0_L
R1464 100K PM_SLP_SUS_L
R1430 100K EDP_BKLT_EN
R1431 100K EDP_PANEL_PWR
R1440 100K TBT_PWR_REQ_L
R1441 100K SMC_RUNTIME_SCI_L
R1442 100K HDMITBTMUX_FLAG
R1443 100K SSD_BOOT
R1445 100K ODD_PWR_EN_L
R1446 100K HDMITBTMUX_LATCH
R1447 100K ENET_LOW_PWR
R1448 100K AUD_PWR_EN
R1449 100K AP_PCIE_DEV_WAKE

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

PCH PM/PCI/GFX

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader
(& Ethernet if combo)

Camera

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 11 OF 19

PCI-E
USB

69 25 IN	PCIE_TBT_D2R_N<0>	F10 PERN5_L0
69 25 IN	PCIE_TBT_D2R_P<0>	E10 PERP5_L0
69 25 OUT	PCIE_TBT_R2D_C_N<0>	C23 PETN5_L0
69 25 OUT	PCIE_TBT_R2D_C_P<0>	C22 PETP5_L0
69 25 IN	PCIE_TBT_D2R_N<1>	F8 PERN5_L1
69 25 IN	PCIE_TBT_D2R_P<1>	E8 PERP5_L1
69 25 OUT	PCIE_TBT_R2D_C_N<1>	B23 PETN5_L1
69 25 OUT	PCIE_TBT_R2D_C_P<1>	A23 PETP5_L1
69 25 IN	PCIE_TBT_D2R_N<2>	H10 PERN5_L2
69 25 IN	PCIE_TBT_D2R_P<2>	G10 PERP5_L2
69 25 OUT	PCIE_TBT_R2D_C_N<2>	B21 PETN5_L2
69 25 OUT	PCIE_TBT_R2D_C_P<2>	C21 PETP5_L2
69 25 IN	PCIE_TBT_D2R_N<3>	E6 PERN5_L3
69 25 IN	PCIE_TBT_D2R_P<3>	F6 PERP5_L3
69 25 OUT	PCIE_TBT_R2D_C_N<3>	B22 PETN5_L3
69 25 OUT	PCIE_TBT_R2D_C_P<3>	A21 PETP5_L3
69 64 29 IN	PCIE_AP_D2R_N	G11 PERN3
69 64 29 IN	PCIE_AP_D2R_P	F11 PERP3
69 29 OUT	PCIE_AP_R2D_C_N	C29 PETN3
69 29 OUT	PCIE_AP_R2D_C_P	B30 PETP3
64	NC_PCIE_FW_D2RN	F13 PERN4
64	NC_PCIE_FW_D2RP	G13 PERP4
64	NC_PCIE_FW_R2D_CN	B29 PETN4
64	NC_PCIE_FW_R2D_CP	A29 PETP4
68 65 34 IN	USB3_SD_D2R_N	G17 PERN1/USB3RN3
68 65 34 IN	USB3_SD_D2R_P	F17 PERP1/USB3RP3
68 65 34 OUT	USB3_SD_R2D_C_N	C30 PETN1/USB3TN3
68 65 34 OUT	USB3_SD_R2D_C_P	C31 PETP1/USB3TP3
69 32 IN	PCIE_CAMERA_D2R_N	F15 PERN2/USB3RN4
69 32 IN	PCIE_CAMERA_D2R_P	G15 PERP2/USB3RP4
69 32 OUT	PCIE_CAMERA_R2D_C_N	B31 PETN2/USB3TN4
69 32 OUT	PCIE_CAMERA_R2D_C_P	A31 PETP2/USB3TP4
NC		E15 RSVD
NC		E13 RSVD
	PCH_PCIE_RCOMP	A27 PCIE_RCOMP
		B27 PCIE_IREF

USB2N0	AN8	USB_EXTA_N (BI 35 68)
USB2P0	AM8	USB_EXTA_P (BI 35 68)
USB2N1	AR7	USB_EXTB_N (BI 61 65 68)
USB2P1	AT7	USB_EXTB_P (BI 61 65 68)
USB2N2	AR8	USB_BT_N (BI 29 68)
USB2P2	AP8	USB_BT_P (BI 29 68)
USB2N3	AR10	NC_USB_IRN (BI 64)
USB2P3	AT10	NC_USB_IRP (BI 64)
USB2N4	AM15	USB_TPAD_N (BI 36 64 68)
USB2P4	AL15	USB_TPAD_P (BI 36 64 68)
USB2N5	AM13	TP_USB_5N
USB2P5	AN13	TP_USB_5P
USB2N6	AP11	NC_USB_CAMERAN (64)
USB2P6	AN11	NC_USB_CAMERAP (64)
USB2N7	AR13	NC_USB_SDN (64)
USB2P7 (IPD)	AP13	NC_USB_SDP (64)
USB3RN1	G20	USB3_EXTA_D2R_N (IN 35 68)
USB3RP1	H20	USB3_EXTA_D2R_P (IN 35 68)
USB3TN1	C33	USB3_EXTA_R2D_C_N (OUT 35 68)
USB3TP1	B34	USB3_EXTA_R2D_C_P (OUT 35 68)
USB3RN2	E18	USB3_EXTB_D2R_N (IN 61 65 68)
USB3RP2	F18	USB3_EXTB_D2R_P (IN 61 65 68)
USB3TN2	B33	USB3_EXTB_R2D_C_N (OUT 61 65 68)
USB3TP2	A33	USB3_EXTB_R2D_C_P (OUT 61 65 68)
USBRBIAS*	AJ10	68 PCH_USB_RBIAS
USBRBIAS	AJ11	
RSVD	AN10	NC
RSVD	AM10	NC
OC0*/GPIO40	AL3	XDP_USB_EXTA_OC_L (IN 14 16 35)
OC1*/GPIO41	AT1	XDP_USB_EXTB_OC_L (IN 14 16 61 65)
OC2*/GPIO42	AH2	XDP_USB_EXTC_OC_L (IN 14 16)
OC3*/GPIO43	AV3	XDP_USB_EXTD_OC_L (IN 14 16)

PLACE_NEAR=U0500.AJ10:2.54mm
R1570 22.6 1% 1/20W MF 201

11 8 PP1V05_S0SW_PCH_VCCUSB3PLL

R1500 3.01K 1% 1/20W MF 201
PLACE_NEAR=U0500.A27:2.54mm

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 7 OF 19

LPC
SMBUS
SPI
C-LINK

69 64 37 BI	LPC_AD<0>	R1540 33 5% 1/20W MF 201 — LPC_AD_R<0> AU14 (IPU) LAD0
69 64 37 BI	LPC_AD<1>	R1541 33 5% 1/20W MF 201 — LPC_AD_R<1> AW12 LAD1
69 64 37 BI	LPC_AD<2>	R1542 33 5% 1/20W MF 201 — LPC_AD_R<2> AY12 LAD2
69 64 37 BI	LPC_AD<3>	R1543 33 5% 1/20W MF 201 — LPC_AD_R<3> AW11 LAD3
69 64 37 OUT	LPC_FRAME_L	R1544 33 5% 1/20W MF 201 — LPC_FRAME_R_L AV12 LFRAME*
69 46 OUT	SPI_CLK_R	AA3 SPI_CLK (IPU)
69 46 OUT	SPI_CS0_R_L	Y7 SPI_CS0* (IPU)
	TP_SPI_CS1_L	Y4 SPI_CS1* (IPU)
	TP_SPI_CS2_L	AC2 SPI_CS2* (IPU)
69 46 BI	SPI_MOSI_R	AA2 SPI_MOSI (IPU/IPD)
69 46 BI	SPI_MISO	AA4 SPI_MISO (IPU)
69 46 14 BI	SPI_IO<2>	Y6 SPI_IO2 (IPU)
69 46 14 BI	SPI_IO<3>	AF1 SPI_IO3 (IPU)

	SMBALERT*/GPIO11	AN2 PCH_SMBALERT_L (14)
SMBCLK	AP2	SMBUS_PCH_CLK (OUT 16 19 40 56 69)
SMBDATA	AH1	SMBUS_PCH_DATA (BI 16 19 40 56 69)
	SML0ALERT*/GPIO60	AL2 WOL_EN (OUT 14 64)
SML0CLK	AN1	SML_PCH_0_CLK (OUT 40 69)
SML0DATA	AK1	SML_PCH_0_DATA (BI 40 69)
	SML1ALERT*/PCHHOT*/GPIO73	AU4 PCH_SML1ALERT_L (OUT 18 39)
SML1CLK_GPIO75	AU3	SMBUS_SMC_1_S0_SCL (OUT 32 37 40 43 44 64 69 73)
SML1DATA/GPIO74	AH3	SMBUS_SMC_1_S0_SDA (BI 32 37 40 43 44 64 69 73)
(IPU/IPD) CL_CLK	AF2	NC_CLINK_CLK (64)
(IPU/IPD) CL_DATA	AD2	NC_CLINK_DATA (64)
CL_RST*	AF4	NC_CLINK_RESET_L (64)

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

PP3V3_SUS (8 11 14 18 46 57 58 59 62 64)
PP3V3_SUS (8 11 14 18 46 57 58 59 62 64)

R1580	100K	XDP_USB_EXTA_OC_L (14 16 35)
R1581	100K	XDP_USB_EXTB_OC_L (14 16 61 65)
R1582	100K	XDP_USB_EXTC_OC_L (14 16)
R1583	100K	XDP_USB_EXTD_OC_L (14 16)
R1548	1K	SPI_IO<2> (14 46 69)
R1549	1K	SPI_IO<3> (14 46 69)
R1590	100K	PCH_SMBALERT_L (14)
R1591	100K	WOL_EN (14 64)

All: 5% 1/20W MF 201

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 15 OF 121
SHEET 14 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H — R1631 100K 5% 1/20W MF 201
RAMCFG2:H — R1636 100K 5% 1/20W MF 201
RAMCFG1:H — R1635 100K 5% 1/20W MF 201
RAMCFG0:H — R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

PP3V3_S3
SSD_LPSR:S3
R1696 100K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT 2C+GT2
BGA
SYM 10 OF 19

XDP_PCH_GPIO76	P1	BMBUSY*/GPIO76
XDP_MLB_RAMCFG0	AU2	GPIO8
HDMITBTMUX_SEL_TBT	AM7	LAN_PHY_PWR_CTRL/GPIO12
TP_MEM_VDD_SEL_1V5_L	AD6	GPIO15 (IPD-RSMRST#)
XDP_LPCPLUS_GPIO	Y1	GPIO16
XDP_PCH_GPIO17	T3	GPIO17
SD_RESET_L	AD5	GPIO24
SMC_WAKE_SCI_L	AN5	GPIO27 (IPD-DeepSx)
TPAD_SPI_INT_GPIO28_L	AD7	GPIO28
TPAD_USB_IF_EN	AN3	GPIO26
SSD_PWR_EN	AG6	GPIO56
PCH_TBT_PCIE_RESET_L	AP1	GPIO57
HDD_PWR_EN	AL4	GPIO58
XDP_SDCONN_STATE_CHANGE_L	AT5	GPIO59
SD_PWR_EN	AK4	GPIO44
TBT_PWR_EN	AB6	GPIO47
XDP_JTAG_ISP_TCK	U4	GPIO48
XDP_JTAG_ISP_TDI	Y3	GPIO49
JTAG_TBT_TMS_PCH	P3	GPIO50
PCH_HSIO_PWR_EN	Y2	HSIOPC/GPIO71
TPAD_SPI_IF_EN	AT3	GPIO13
XDP_MLB_RAMCFG3	AH4	GPIO14
SPIROM_USE_MLB	AM4	GPIO25
CAMERA_PWR_EN_PCH	AG5	GPIO45
TPAD_SPI_INT_GPIO46_L	AG3	GPIO46
XDP_MLB_RAMCFG1	AM3	GPIO9
XDP_MLB_RAMCFG2	AM2	GPIO10
SSD_SR_EN_L	P2	DEVSLP0/GPIO33
AP_S0IX_WAKE_SEL	C4	SDIO_POWER_EN/GPIO70
SSD_RESET_L	L2	DEVSLP1/GPIO38
CAM_PCIE_RESET_L	N5	DEVSLP2/GPIO39
PCH_TCO_TIMER_DISABLE	V2	SPKR/GPIO81 (IPD-PLTRST#)

PLT_RESET_L
R1621 100K 5% 1/20W MF 201

TPAD_SPI_INT_GPIO28_L
R1681 0 5% 1/20W MF 0201
TPAD_SPI_INT_L
R1682 0 5% 1/20W MF 0201
TPAD_SPI_INT_GPIO46_L

R1639 100K 5% 1/20W MF 201
R1680 100K 5% 1/20W MF 201

PP3V3_S0
R1641 1K 5% 1/20W MF 201

PP3V3_S5
PP3V3_S3
PP3V3_S0SW_SD
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
PP3V3_S0

TBTLC for CR, S0 for RR

R1610	100K	XDP_PCH_GPIO76	
R1614	100K	XDP_LPCPLUS_GPIO	
R1615	100K	XDP_PCH_GPIO17	
SD_ON_MLB			
R1616	100K	SD_RESET_L	R1616 should also be stuffed if platform does not use SD card
R1617	100K	SMC_WAKE_SCI_L	
R1618	100K	TPAD_SPI_INT_L	
R1619	100K	TPAD_USB_IF_EN	
R1620	100K	SSD_PWR_EN	SSD_LPSR:S0 BOM option is on R1620
SSD_LPSR:S0			
R1622	100K	HDD_PWR_EN	
R1623	100K	XDP_SDCONN_STATE_CHANGE_L	
R1624	100K	SD_PWR_EN	
R1625	100K	TBT_PWR_EN	
R1626	100K	XDP_JTAG_ISP_TCK	
R1627	100K	XDP_JTAG_ISP_TDI	
R1628	100K	JTAG_TBT_TMS_PCH	
R1629	100K	PCH_HSIO_PWR_EN	
R1630	100K	TPAD_SPI_IF_EN	
R1632	100K	SPIROM_USE_MLB	Stuffed R1632
R1633	100K	CAMERA_PWR_EN_PCH	
R1634	100K	TPAD_SPI_INT_GPIO46_L	No-Stuffed R1634
NOSTUFF			
R1637	100K	SSD_SR_EN_L	
R1638	100K	AP_S0IX_WAKE_SEL	
R1640	100K	XDP_FW_PME_L	
R1652	10K	LPC_SERIRQ	
R1691	100K	BT_PWRRST_L	
R1693	100K	ENET_MEDIA_SENSE	
R1694	100K	LCD_IRQ_L	
R1695	100K	LCD_PSR_EN	

PP1V05_S0
R1650 1K 5% 1/20W MF 201

CPU/MISC

THERMTRIP*	D60	PM_THRMTRIP_L	OUT
RCIN*/GPIO82	V4	TBT_CIO_PLUG_EVENT_L	IN
SERIRQ	T4	LPC_SERIRQ	BI
PCH_OPI_COMP	AW15	PCH_OPI_COMP	
RSVD	AF20	NC	
RSVD	AB21	NC	

PLACE_NEAR=U0500.AW15:2.54mm
R1655 49.9 1% 1/20W MF 201

GPIO / LPIO

GSPI0_CS*/GPIO83	R6	AUD_SPI_CS_L	
GSPI0_CLK/GPIO84	L6	AUD_SPI_CLK	
GSPI0_MISO/GPIO85 (IPD)	N6	AUD_SPI_MISO	
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	L8	AUD_SPI_MOSI	
GSPI1_CS*/GPIO87	R7	TPAD_SPI_CS_L	OUT
GSPI1_CLK/GPIO88	L5	TPAD_SPI_CLK	OUT
GSPI1_MISO/GPIO89 (IPD)	N7	TPAD_SPI_MISO	IN
GSPI_MOSI/GPIO90	K2	TPAD_SPI_MOSI	OUT
UART0_RXD/GPIO91	J1	PCH_BT_UART_D2R	
UART0_TXD/GPIO92	K3	PCH_BT_UART_R2D	
UART0_RTS*/GPIO93	J2	PCH_BT_UART_RTS_L	
UART0_CTS*/GPIO94	G1	PCH_BT_UART_CTS_L	
UART1_RXD/GPIO00	K4	PCH_UART1_RXD	
UART1_TXD/GPIO1	G2	PCH_UART1_TXD	
UART1_RST*/GPIO2	J3	JTAG_ISP_TDO	IN
UART1_CTS*/GPIO3	J4	PCH_UART1_CTS_L	
I2C0_SDA/GPIO4	F2	AP_S0IX_WAKE_L	IN
I2C0_SCL/GPIO5	F3	AP_RESET_L	OUT
I2C1_SDA/GPIO6	G4	PCH_I2C1_SDA	
I2C1_SCL/GPIO7	F1	PCH_I2C1_SCL	
SDIO_CLK/GPIO64	E3	TBT_POC_RESET_L	OUT
SDIO_CMD/GPIO65	F4	BT_PWRRST_L	OUT
SDIO_D0/GPIO66 (IPD-PLTRST#)	D3	PCH_STRP_TOPBLK_SWP_L	IN
SDIO_D1/GPIO67	E4	ENET_MEDIA_SENSE	IN
SDIO_D2/GPIO68	C3	LCD_IRQ_L	IN
SDIO_D3/GPIO69	E2	LCD_PSR_EN	OUT

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLT_RESET_L
R1671 100K 5% 1/20W MF 201

Pull-up on TBT page

Requires connection to SMC via 1K series R

PP3V3_S0

AUD_SPI_CS_L	R1660	100K	
AUD_SPI_CLK	R1661	100K	
AUD_SPI_MISO	R1662	100K	
AUD_SPI_MOSI	R1663	100K	
TPAD_SPI_CS_L	R1664	47K	
TPAD_SPI_CLK	R1665	47K	
TPAD_SPI_MISO	R1666	47K	
TPAD_SPI_MOSI	R1667	47K	
PCH_BT_UART_D2R	R1668	47K	
PCH_BT_UART_R2D	R1669	47K	
PCH_UART1_RXD	R1672	47K	
PCH_UART1_TXD	R1673	47K	
JTAG_ISP_TDO	R1674	100K	
PCH_UART1_CTS_L	R1675	47K	
AP_S0IX_WAKE_L	R1676	100K	
PCH_I2C1_SDA	R1678	2.2K	
PCH_I2C1_SCL	R1679	2.2K	
PCH_BT_UART_RTS_L	R1670	47K	
PCH_BT_UART_CTS_L	R1677	47K	

SYNC_MASTER=WILL_J43 SYNC_DATE=01/14/2013

PAGE TITLE: PCH GPIO/MISC/LPIO

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 16 OF 121
SHEET: 15 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Merged (CPU/PCH) Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

PP1V05_S0

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

R1830 150 5% 1/16W MF-LF 402

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CPU_VCCST_PWRGD → R1800 1K (PLACE_NEAR=U0500.C61:2.54mm)
PM_PWRBTN_L → R1802 0 (PLACE_NEAR=U5000.J3:2.54mm)
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402
XDP_CPU_TCK
PCH_JTAGX → R1835 0 (PLACE_NEAR=J1800.58:28mm)
(XDP, 5% 1/20W MF 0201)

XDP_CPU_TDO → R1810 51 (PLACE_NEAR=U0500.F62:28mm)
XDP_CPU_TCK → R1813 51 (PLACE_NEAR=U0500.E60:28mm)
(XDP, 5% 1/20W MF 201)

TDI and TMS are terminated in CPU.

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

R1805 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.AG7:2.54mm)
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_CPU_TDO (PLACE_NEAR=J1800.51:28MM)

CRITICAL
Q1840
DMN5L06VK-7
SOT563
VER 3

XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)
XDP_CPUPCH_TRST_L
XDP_CPUPCH_TRST_L
XDP_CPU_TDI (PLACE_NEAR=J1800.55:28mm)

Q1842
DMN5L06VK-7
SOT563
VER 3

XDP_CPU_TMS

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD

C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, A, Y, NC, NC, GND)
R1845 330K 5% 1/20W MF 201
XDP_JTAG_CPU_ISOL_L
NC → NC

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF

(PLACE_NEAR=U0500.AE63:28mm / AE62:28mm / AD61:28mm / AD62:28mm / AE62:28mm / AU62:28mm; 5% 1/20W MF 201)

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L		XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L		XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L		XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK		XDP_JTAG_ISP_TCK
XDP_FW_PME_L	TP1879	
XDP_PCH_GPIO35	TP1880	
XDP_PCH_UART_SSD_L_BT_H	TP1881	
XDP_SSD_PCIE0_SEL_L	R1884 1K	
XDP_LPCPLUS_GPIO		XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI		XDP_JTAG_ISP_TDI

(MAKE_BASE=TRUE; TP-P6)

NOTE: Must not short XDP pins together!

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 18 OF 121
SHEET: 16 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenCLK 25MHz Power — PP3V3_S5RS3RS0_SYSCLKGEN
Must be powered if any VDDIO is powered.

CAM XTAL Power — PP1V2_CAM_XTALPCIEVDD
TBT XTAL Power — PP3V3_TBTLC

C1924 0.1UF 10% 16V X5R-CERM 0201
C1922 0.1UF 10% 16V X5R-CERM 0201
C1902 1UF 20% 6.3V X5R 0201

U1900 SLG3NB148CV TQFN CRITICAL
NC, VDD, VG3HOT
VIOE_25M_A, VIOE_25M_B, VIOE_25M_C
32.768K
25M_A, 25M_B, 25M_C
VOUT
GND, THRM PAD

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

CKPLUS_WAIVE=PwrTerm2Gnd

PCH_CLK32K_RTCX1 (OUT)
SYSCLK_CLK25M_CAMERA (OUT)
SYSCLK_CLK25M_TBT (OUT)
PPVRTC_G3H (OUT) — For SB RTC Power

C1910 1UF 20% 6.3V X5R 0201

C1905 12PF 5% 25V CERM 0201
C1906 12PF 5% 25V CERM 0201
Y1905 CRITICAL 25.000MHZ-12PF-20PPM SM-3.2X2.5MM
R1905 0 5% 1/20W MF 0201 — NO STUFF
R1906 1M 5% 1/20W MF 201

SYSCLK_CLK25M_X2 → SYSCLK_CLK25M_X2_R → X2
SYSCLK_CLK25M_X1 → X1

NOTE: 30 PPM or better required for RTC accuracy

NC_RTC_CLK32K_RTCX2 — MAKE_BASE=TRUE — NO_TEST=TRUE — NC_RTC_CLK32K_RTCX2 (LN)

PCH 24MHz Crystal

C1915 6.8PF +/-0.1PF 25V C0G 0201
C1916 6.8PF +/-0.1PF 25V C0G 0201
Y1915 CRITICAL 24.000MHZ-20PPM-6PF 3.20X2.50MM-SM1
R1915 0 5% 1/20W MF 0201
R1916 1M 5% 1/20W MF 201

PCH_CLK24M_XTALOUT_R → PCH_CLK24M_XTALOUT (LN)
PCH_CLK24M_XTALIN (OUT)

PCH 24MHz Outputs

R1927 22 5% 1/20W MF 201

LPC_CLK24M_SMC_R (LN) — PLACE_NEAR=U0500.AN15:1mm
LPC_CLK24M_SMC — MAKE_BASE=TRUE
LPC_CLK24M_SMC (OUT)

PCH Reset Button

PP3V3_S0
R1995 10K 5% 1/20W MF 201
XDP
R1996 0 1/20W 0201 MF 5%
XDP_DBRESET_L (LN)
PM_SYSRST_L (BI)
NO STUFF
R1997 0 5% 1/16W MF-LF 402
SILK_PART=SYS RESET

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

PP1V2_S3
C1970 0.1UF 10% 16V X5R-CERM 0201
U1970 74AUP1G07GF SOT891 (VCC, A, Y, NC, NC, NC, GND)
CPU_MEMVTT_PWR_EN_LSVDDQ (LN)
PP3V3_S0
R1970 330K 5% 1/20W MF 201
MEMVTT_PWR_EN — MAKE_BASE=TRUE
MEMVTT_PWR_EN (OUT)

TPS51916 I(leak) = +/- 1uA, Vih(min) = 1.8V
33uW when driven-low

PCH ME Disable Strap

PP5V_S0
R1920 100K 5% 1/20W MF 201
Q1920 DMN5L06VK-7 SOT563 VER 3
SPI_DESCRIPTOR_OVERRIDE_LS5V
PP1V5_S0SW_AUDIO_HDA
SPI_DESCRIPTOR_OVERRIDE
Q1920 DMN5L06VK-7 SOT563 VER 3
R1921 1K 5% 1/20W MF 201
HDA_SDOUT_R (OUT) — IPD = 9-50k
SPI_DESCRIPTOR_OVERRIDE_L (LN)

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD

PP3V3_S5
C1930 0.1UF 10% 16V X5R-CERM 0201
U1930 CRITICAL 74AUP1G09 SOT891 (VCC, A, B, NC, Y, GND)
ALL_SYS_PWRGD (LN)
PM_SLP_S3_L (LN)
PP1V05_S0
R1931 10K 5% 1/20W MF 201
CPU_VCCST_PWRGD (OUT)

PCH PWROK Generation

PP3V42_G3H
PP3V3_S0
C1950 0.1UF 10% 16V X5R-CERM 0201 — BYPASS=U1950:5MM
R1950 10K 5% 1/20W MF 201
CPU_VR_EN (LN)
R1955 10K 5% 1/20W MF 201
NO STUFF R1951 0 5% 1/20W MF 0201
CPU_VR_READY (OUT) — MAKE_BASE=TRUE
CPU_VR_READY (LN)
ALL_SYS_PWRGD (LN)
CPUVR_PGOOD_R
U1950 74LVC2G08GT/SS05 SOT833
PM_S0_PGOOD
NO STUFF R1961 100K 5% 1/20W MF 201
R1963 0 5% 1/20W MF 0201
NO STUFF R1960 0 5% 1/20W MF 0201 — WF: Do we need this?
CKPLUS_WAIVE=UNCONNECTED_PINS
U1950 74LVC2G08GT/SS05 SOT833
SYS_PWROK_R
R1962 1K 5% 1/20W MF 201
PM_PCH_SYS_PWROK (OUT)
PM_PCH_PWROK (OUT) — MAKE_BASE=TRUE
PM_PCH_PWROK (OUT)
SMC_DELAYED_PWRGD (LN)

SYNC_MASTER=J43_MLB1 SYNC_DATE=01/09/2013
PAGE TITLE: Chipset Support
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 19 OF 121
SHEET: 17 OF 76

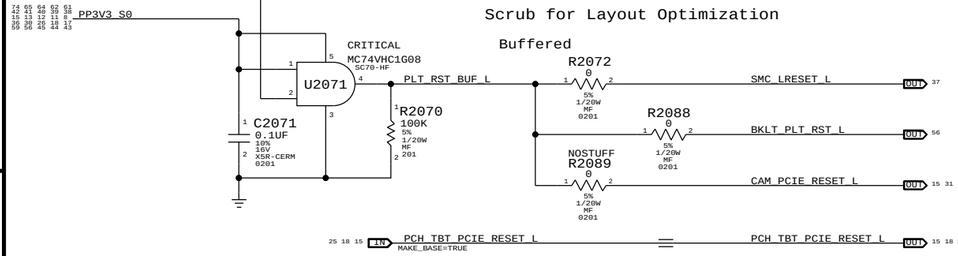
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

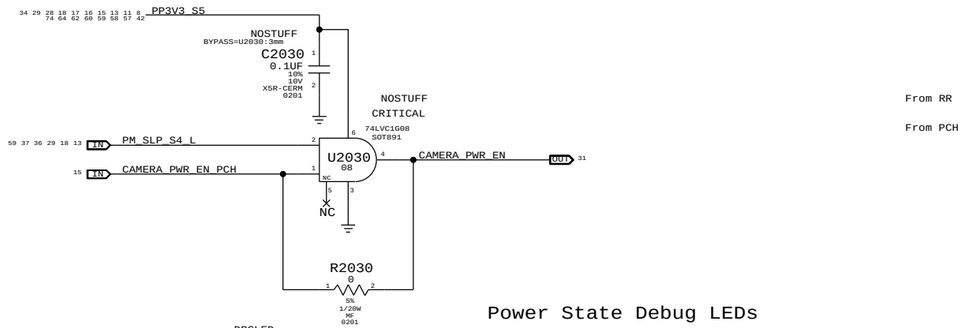
Platform Reset Connections

Unbuffered

Scrub for Layout Optimization

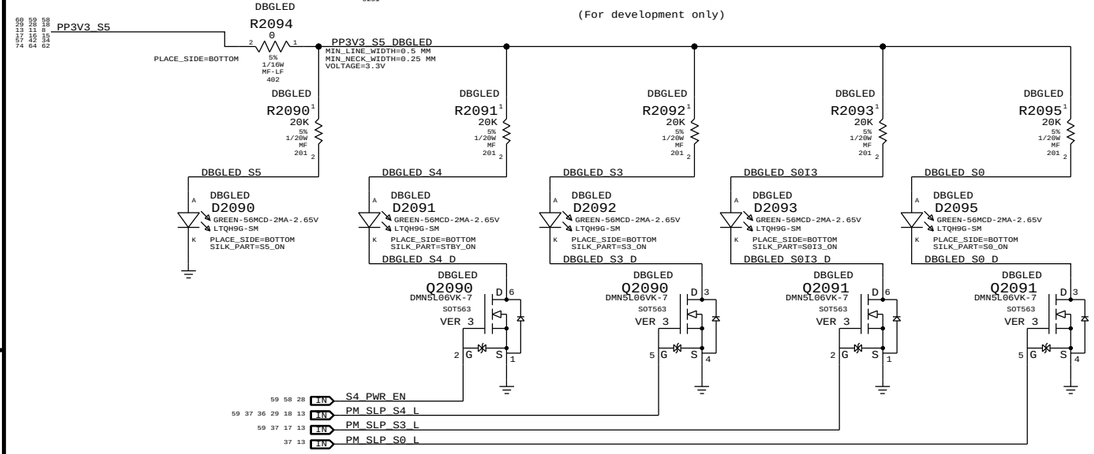
Buffered



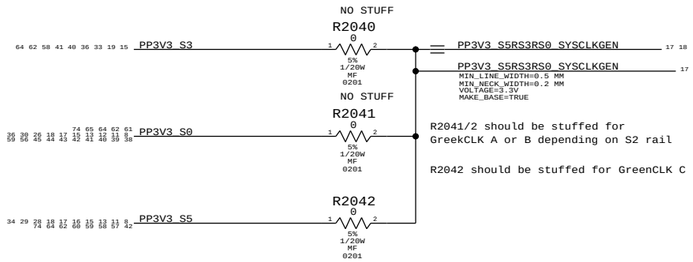


Power State Debug LEDs

(For development only)



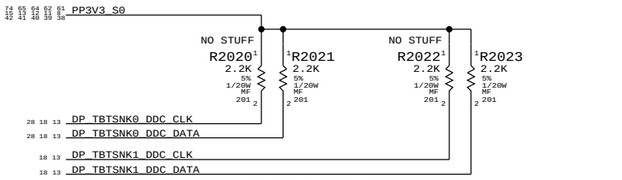
GreenCLK 25MHz Power



DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

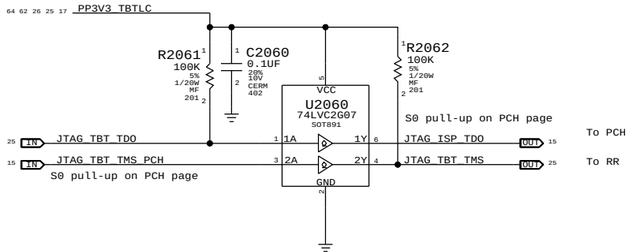


TBTSNK1_DDC is pulled-up just to indicate that
DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so
DDC_CLK pull-ups are unstuffed.

Redwood Ridge JTAG Isolation

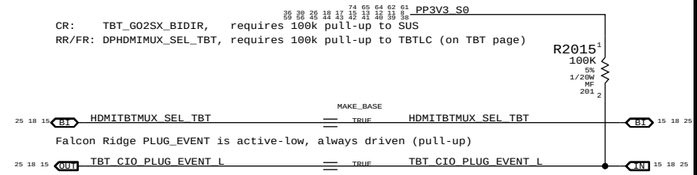
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH



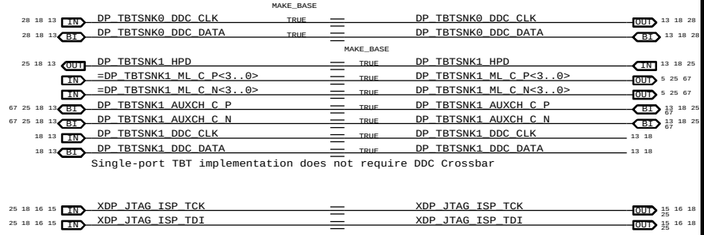
NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary.

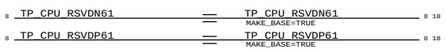
Thunderbolt Pull-up/downs



TBT Aliases

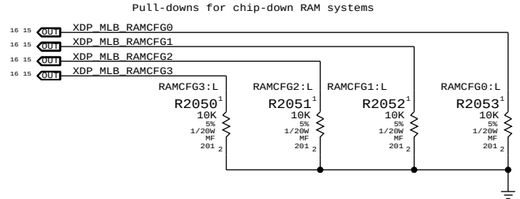


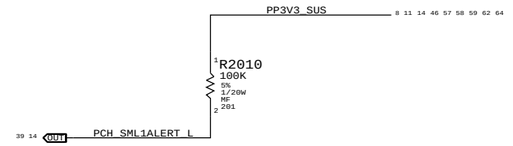
Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property



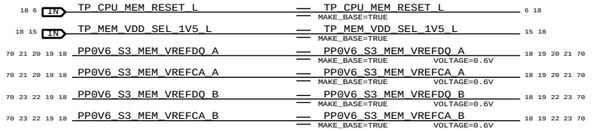
RAM Configuration Straps

Pull-downs for chip-down RAM systems





LPDDR3 Alias Support



SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE

Project Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 20 OF 121

SHEET 18 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

Q2220 DMN5L06VK-7 SOT563 CRITICAL VER 3
Q2260 DMN5L06VK-7 SOT563 CRITICAL VER 3
Q2220 DMN5L06VK-7 SOT563 CRITICAL VER 3
Q2260 DMN5L06VK-7 SOT563 CRITICAL VER 3

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

CPU_MEM_VREFDQ_A_ISOL
CPU_MEM_VREFDQ_B_ISOL
CPU_MEM_VREFCA_A_ISOL
CPU_MEM_VREFCA_B_ISOL

EN RC's to avoid drain glitches
May not be necessary due to C22x0

DDRVREF_DAC R2225 100K 1% 1/20W MF 201 — VREFMRGN_DQ_A_EN_RC — DDRVREF_DAC C2225 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm

DDRVREF_DAC R2245 100K 1% 1/20W MF 201 — VREFMRGN_DQ_B_EN_RC — DDRVREF_DAC C2245 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

DDRVREF_DAC R2265 100K 1% 1/20W MF 201 — VREFMRGN_CA_A_EN_RC — DDRVREF_DAC C2265 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2215 100K 5% 1/20W MF 201

DDRVREF_DAC R2285 100K 1% 1/20W MF 201 — VREFMRGN_CA_B_EN_RC — DDRVREF_DAC C2285 0.1UF 10% 6.3V CERM-X5R 0201
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
(All 4 R's)

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.
OMIT

PP3V3_S3 — R2218 SHORT NONE NONE NONE 402 — PP3V3_S3_VREFMRGN_DAC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 MSOP DAC5574 — VDD, GND
SMBUS_PCH_CLK — SCL — VOUTA — VREFMRGN_DQ_A
SMBUS_PCH_DATA — SDA — VOUTB — VREFMRGN_DQ_B
A0 — VOUTC — VREFMRGN_CA_AB
A1 — VOUTD — VREFMRGN_MEMVREG

Addr=0x98(WR)/0x99(RD)

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRVREF_DAC R2226 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_A_RDIV
DDRVREF_DAC R2246 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_B_RDIV
DDRVREF_DAC R2266 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_A_RDIV
DDRVREF_DAC R2286 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_B_RDIV

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2201 PCA9557 QFN (OD) — VCC, GND, THRM PAD
R2200 100K 5% 1/20W MF 201

Addr=0x30(WR)/0x31(RD)

SMBUS_PCH_CLK — SCL
SMBUS_PCH_DATA — SDA
A0, A1, A2

P0 VREFMRGN_CPU_EN
P1 VREFMRGN_DQ_A_EN
P2 VREFMRGN_DQ_B_EN
P3 VREFMRGN_CA_A_EN
P4 VREFMRGN_CA_B_EN
P5 VREFMRGN_MEMVREG_EN
P6 VREFMRGN_SPARE_EN
P7 NC
RESET* — PCA9557D_RESET_L

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PP3V3_S3
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP — V+, V-
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 38.3K 1% 1/20W MF 201 — DDRREG_FB — PLACE_NEAR=R7415.2:1mm

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP — V+, V-
VREFMRGN_SPARE_BUF
DDRVREF_DAC R2217 1M 5% 1/20W MF 201

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2212 100K 5% 1/20W MF 201

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

VRef Dividers

Always used, regardless of margining option.

PP1V2_S3

R2223 10 1% 1/20W MF 201 — PLACE_NEAR=Q2220.6:2mm — C2220 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_A_RC
R2221 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2220.6:3mm — PP0V6_S3_MEM_VREFDQ_A — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2222 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2221.2:1mm
R2220 24.9 1% 1/20W MF 201

R2243 10 1% 1/20W MF 201 — PLACE_NEAR=Q2260.6:2mm — C2240 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFDQ_B_RC
R2241 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2260.6:3mm — PP0V6_S3_MEM_VREFDQ_B — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2242 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2241.2:1mm
R2240 24.9 1% 1/20W MF 201

R2263 10 1% 1/20W MF 201 — PLACE_NEAR=Q2220.3:2mm — C2260 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_A_RC
R2261 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2220.3:3mm — PP0V6_S3_MEM_VREFCA_A — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2262 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2261.2:1mm
R2260 24.9 1% 1/20W MF 201

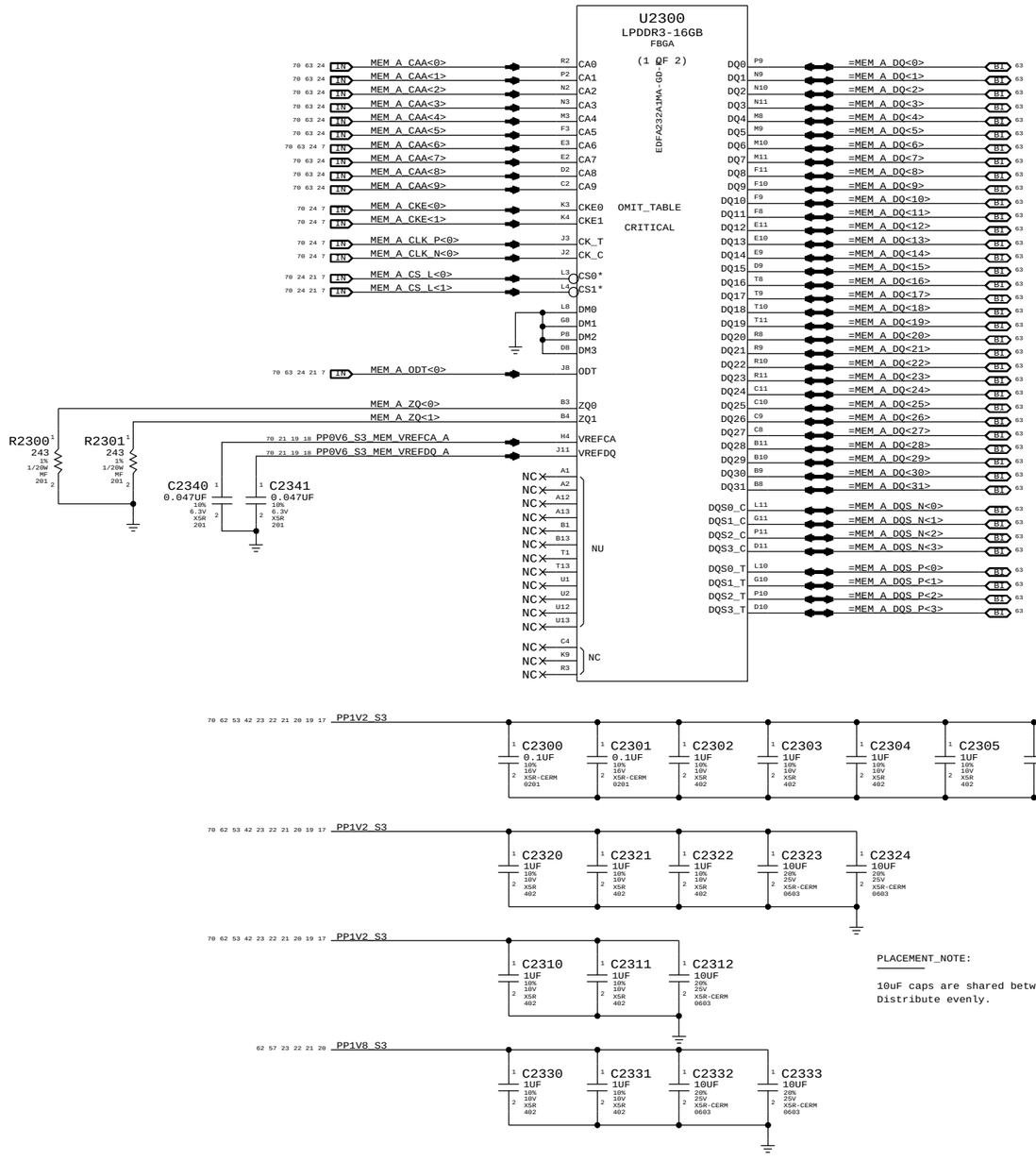
R2283 10 1% 1/20W MF 201 — PLACE_NEAR=Q2260.3:2mm — C2280 0.022UF 10% 6.3V X5R-CERM 0201 — MEM_VREFCA_B_RC
R2281 8.2K 1% 1/20W MF 201 — PLACE_NEAR=Q2260.3:3mm — PP0V6_S3_MEM_VREFCA_B — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2282 8.2K 1% 1/20W MF 201 — PLACE_NEAR=R2281.2:1mm
R2280 24.9 1% 1/20W MF 201

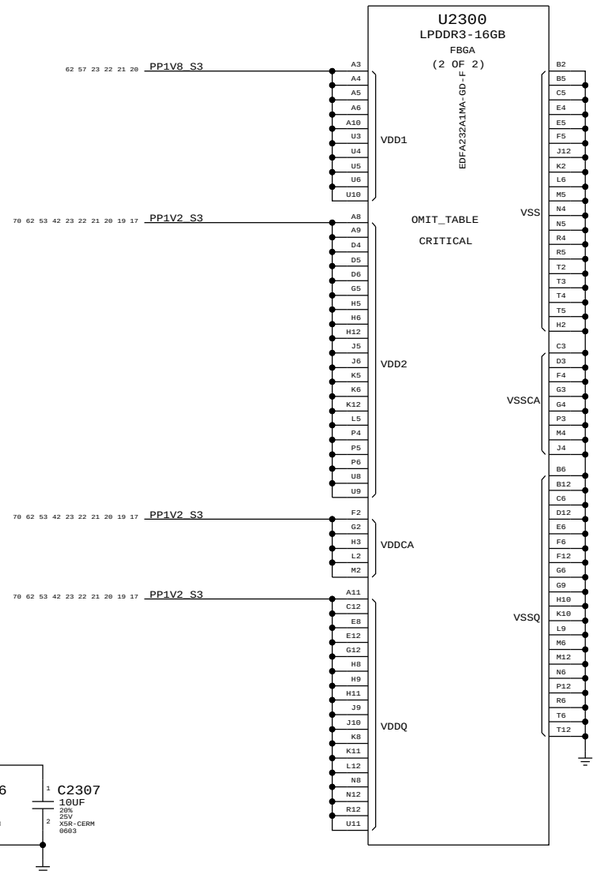
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

SYNC_MASTER=J41_MLB SYNC_DATE=02/12/2013
PAGE TITLE: DDR3 VREF MARGINING
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 22 OF 121
SHEET: 19 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL A (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

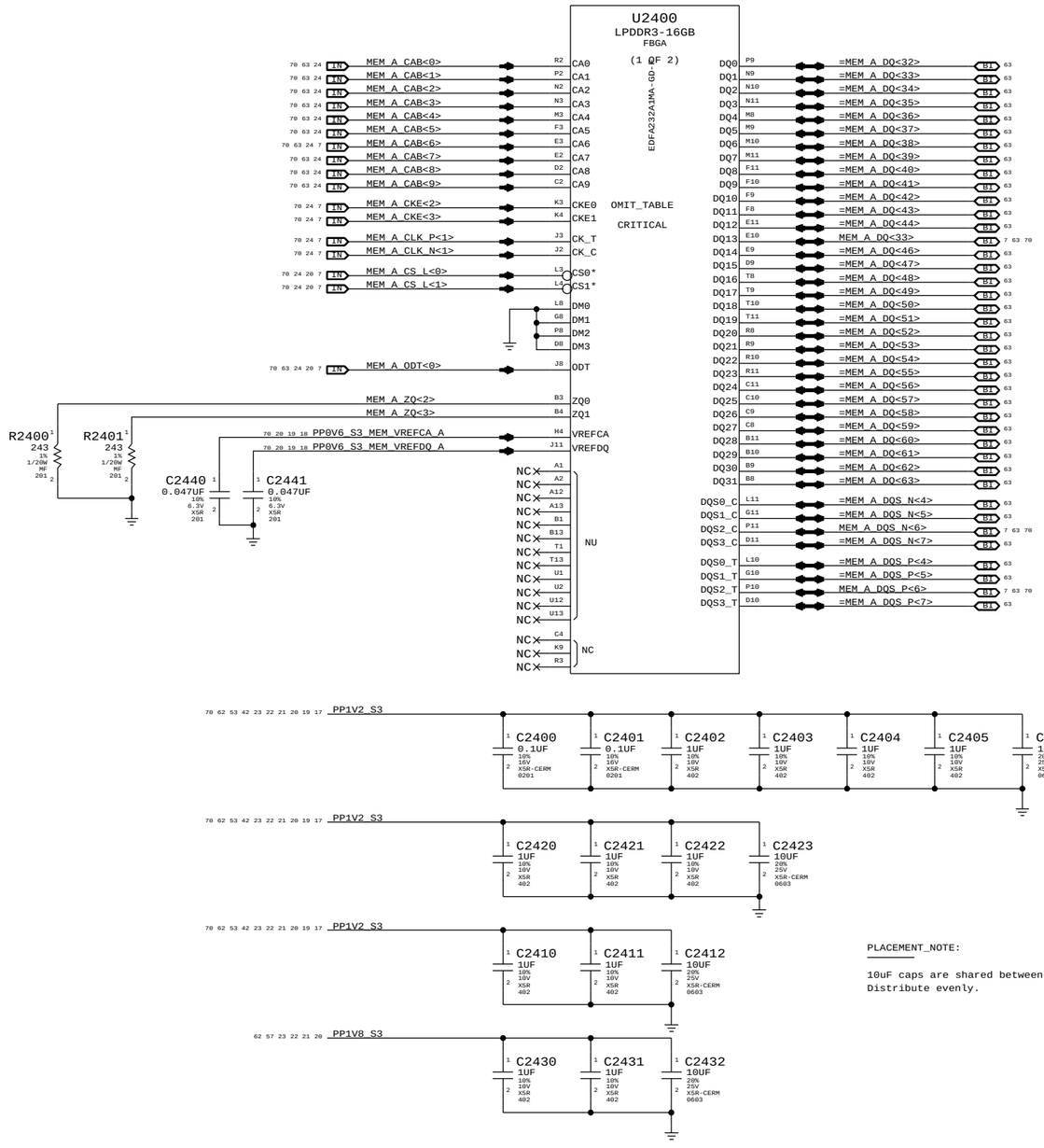
PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 23 OF 121
SHEET 20 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

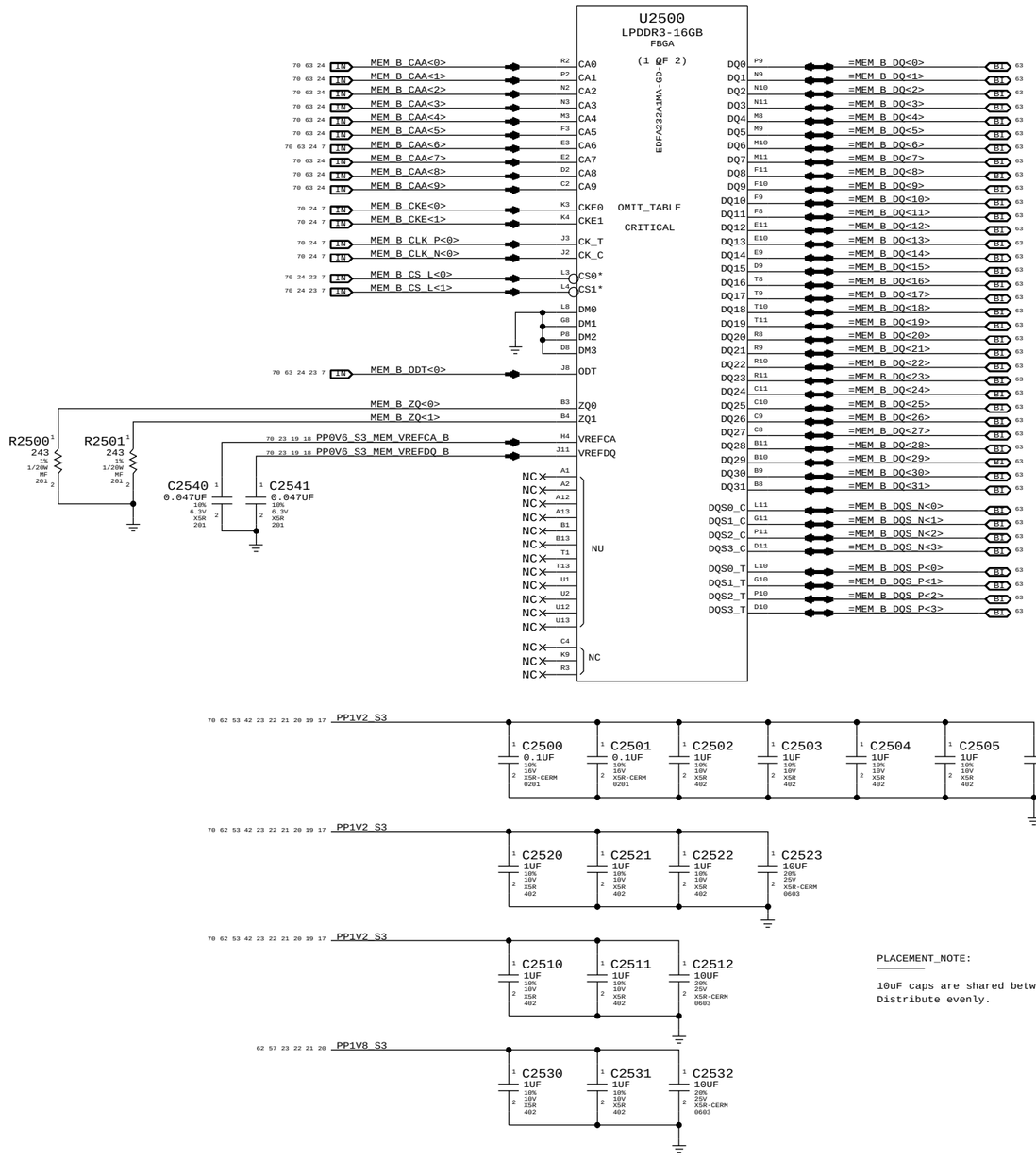
PAGE 24 OF 121

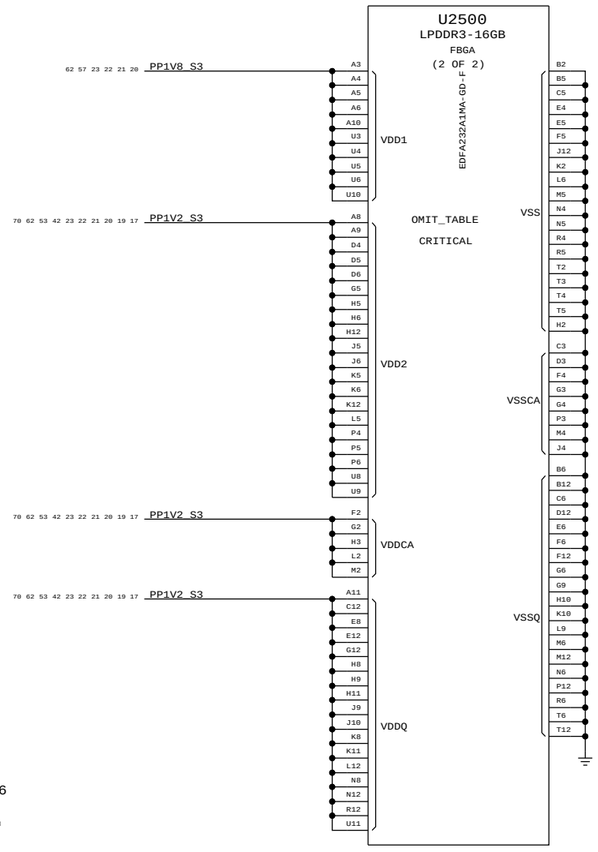
SHEET 21 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL B (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

LPDDR3 DRAM Channel B (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

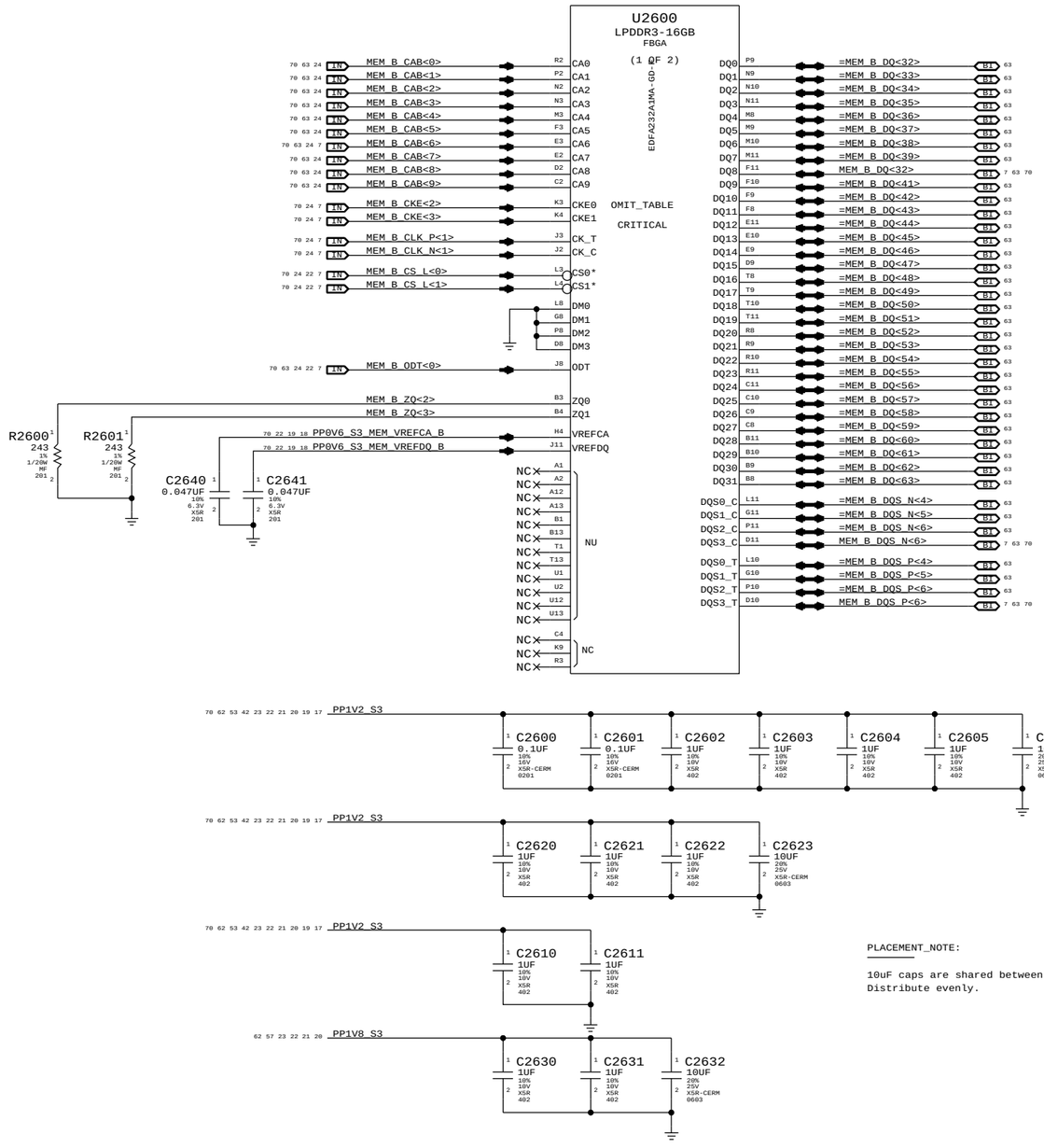
PAGE 25 OF 121

SHEET 22 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 26 OF 121

SHEET 23 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

62 53 24 PP0V6_S0_DDRVTT

70 63 20	IN	MEM_A_CAA<9>	RP2701	56	4	5	5%	1/32W	4X0201-HF
70 63 20	IN	MEM_A_CAA<8>	RP2701	56	3	6	5%	1/32W	4X0201-HF
70 63 20 7	IN	MEM_A_CAA<6>	RP2701	56	2	7	5%	1/32W	4X0201-HF
70 63 20	IN	MEM_A_CAA<7>	RP2701	56	1	8	5%	1/32W	4X0201-HF
70 63 20	IN	MEM_A_CAA<5>	R2700	56	1	2	5%	1/32W	4X0201-HF
70 20 7	IN	MEM_A_CLK_P<0>	R2701	39	1	2	5%	1/20W	201 MF
70 20 7	IN	MEM_A_CLK_N<0>	R2702	39	1	2	5%	1/20W	201 MF
70 20 7	IN	MEM_A_CKE<1>	R2703	82	1	2	5%	1/20W	201 MF
70 20 7	IN	MEM_A_CKE<0>	R2704	82	1	2	5%	1/20W	201 MF
70 63 20	IN	MEM_A_CAA<4>	R2705	56	1	2	5%	1/20W	201 MF
70 63 20	IN	MEM_A_CAA<3>	R2706	56	1	2	5%	1/20W	201 MF
70 63 20	IN	MEM_A_CAA<2>	RP2703	56	4	5	5%	1/32W	4X0201-HF
70 63 20	IN	MEM_A_CAA<1>	RP2703	56	3	6	5%	1/32W	4X0201-HF
70 63 20	IN	MEM_A_CAA<0>	RP2703	56	2	7	5%	1/32W	4X0201-HF
70 63 21	IN	MEM_A_CAB<9>	R2725	56	1	2	5%	1/20W	201 MF
70 63 21	IN	MEM_A_CAB<8>	RP2707	56	4	5	5%	1/32W	4X0201-HF
70 63 21 7	IN	MEM_A_CAB<6>	RP2707	56	3	6	5%	1/32W	4X0201-HF
70 63 21	IN	MEM_A_CAB<7>	RP2707	56	2	7	5%	1/32W	4X0201-HF
70 63 21	IN	MEM_A_CAB<5>	RP2707	56	1	8	5%	1/32W	4X0201-HF
70 21 7	IN	MEM_A_CLK_P<1>	R2707	39	1	2	5%	1/20W	201 MF
70 21 7	IN	MEM_A_CLK_N<1>	R2708	39	1	2	5%	1/20W	201 MF
70 21 7	IN	MEM_A_CKE<2>	R2709	82	1	2	5%	1/20W	201 MF
70 21 7	IN	MEM_A_CKE<3>	R2720	82	1	2	5%	1/20W	201 MF
70 63 21	IN	MEM_A_CAB<4>	R2721	56	1	2	5%	1/20W	201 MF
70 63 21	IN	MEM_A_CAB<2>	RP2704	56	4	5	5%	1/32W	4X0201-HF
70 63 21	IN	MEM_A_CAB<3>	RP2704	56	3	6	5%	1/32W	4X0201-HF
70 63 21	IN	MEM_A_CAB<1>	RP2704	56	2	7	5%	1/32W	4X0201-HF
70 63 21	IN	MEM_A_CAB<0>	RP2704	56	1	8	5%	1/32W	4X0201-HF
70 21 20 7	IN	MEM_A_CS_L<0>	R2722	82	1	2	5%	1/20W	201 MF
70 21 20 7	IN	MEM_A_CS_L<1>	R2723	82	1	2	5%	1/20W	201 MF
70 63 21 20 7	IN	MEM_A_ODT<0>	R2724	82	1	2	5%	1/20W	201 MF

1 C2700 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2701 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2702 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2703 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2704 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2705 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2706 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2707 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2708 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2709 0.47UF 20% 4V CERM-X5R-1 201 — 2

CRITICAL
1 C2720 22UF 20% 6.3V X5R-CERM-1 603 — 2

Spare
RP2703
56
NC — 1 — 8 — NC
5% 1/32W 4X0201-HF

PLACE_NEAR=RP2701.5:4mm

62 53 24 PP0V6_S0_DDRVTT

70 63 22	IN	MEM_B_CAA<9>	RP2712	56	4	5	5%	1/32W	4X0201-HF
70 63 22	IN	MEM_B_CAA<8>	RP2712	56	3	6	5%	1/32W	4X0201-HF
70 63 22	IN	MEM_B_CAA<7>	RP2712	56	2	7	5%	1/32W	4X0201-HF
70 63 22 7	IN	MEM_B_CAA<6>	RP2712	56	1	8	5%	1/32W	4X0201-HF
70 63 22	IN	MEM_B_CAA<5>	R2710	56	1	2	5%	1/32W	4X0201-HF
70 22 7	IN	MEM_B_CLK_P<0>	R2711	39	1	2	5%	1/20W	201 MF
70 22 7	IN	MEM_B_CLK_N<0>	R2712	39	1	2	5%	1/20W	201 MF
70 22 7	IN	MEM_B_CKE<1>	R2713	82	1	2	5%	1/20W	201 MF
70 22 7	IN	MEM_B_CKE<0>	R2714	82	1	2	5%	1/20W	201 MF
70 63 22	IN	MEM_B_CAA<4>	R2715	56	1	2	5%	1/20W	201 MF
70 63 22	IN	MEM_B_CAA<2>	R2716	56	1	2	5%	1/20W	201 MF
70 63 22	IN	MEM_B_CAA<3>	RP2713	56	4	5	5%	1/32W	4X0201-HF
70 63 22	IN	MEM_B_CAA<1>	RP2713	56	3	6	5%	1/32W	4X0201-HF
70 63 22	IN	MEM_B_CAA<0>	RP2713	56	2	7	5%	1/32W	4X0201-HF
70 63 23	IN	MEM_B_CAB<9>	R2735	56	1	2	5%	1/20W	201 MF
70 63 23	IN	MEM_B_CAB<8>	RP2717	56	4	5	5%	1/32W	4X0201-HF
70 63 23	IN	MEM_B_CAB<7>	RP2717	56	3	6	5%	1/32W	4X0201-HF
70 63 23 7	IN	MEM_B_CAB<6>	RP2717	56	2	7	5%	1/32W	4X0201-HF
70 63 23	IN	MEM_B_CAB<5>	RP2717	56	1	8	5%	1/32W	4X0201-HF
70 23 7	IN	MEM_B_CLK_N<1>	R2717	39	1	2	5%	1/20W	201 MF
70 23 7	IN	MEM_B_CLK_P<1>	R2718	39	1	2	5%	1/20W	201 MF
70 23 7	IN	MEM_B_CKE<2>	R2719	82	1	2	5%	1/20W	201 MF
70 23 7	IN	MEM_B_CKE<3>	R2730	82	1	2	5%	1/20W	201 MF
70 63 23	IN	MEM_B_CAB<4>	R2731	56	1	2	5%	1/20W	201 MF
70 63 23	IN	MEM_B_CAB<2>	RP2714	56	4	5	5%	1/32W	4X0201-HF
70 63 23	IN	MEM_B_CAB<3>	RP2714	56	3	6	5%	1/32W	4X0201-HF
70 63 23	IN	MEM_B_CAB<1>	RP2714	56	2	7	5%	1/32W	4X0201-HF
70 63 23	IN	MEM_B_CAB<0>	RP2714	56	1	8	5%	1/32W	4X0201-HF
70 23 22 7	IN	MEM_B_CS_L<0>	R2732	82	1	2	5%	1/20W	201 MF
70 23 22 7	IN	MEM_B_CS_L<1>	R2733	82	1	2	5%	1/20W	201 MF
70 63 23 22 7	IN	MEM_B_ODT<0>	R2734	82	1	2	5%	1/20W	201 MF

1 C2710 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2711 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2712 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2713 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2714 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2715 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2716 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2717 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2718 0.47UF 20% 4V CERM-X5R-1 201 — 2

1 C2719 0.47UF 20% 4V CERM-X5R-1 201 — 2

CRITICAL
1 C2740 22UF 20% 6.3V X5R-CERM-1 603 — 2

Spare
RP2713
56
NC — 1 — 8 — NC
5% 1/32W 4X0201-HF

PLACE_NEAR=RP2714.8:4mm

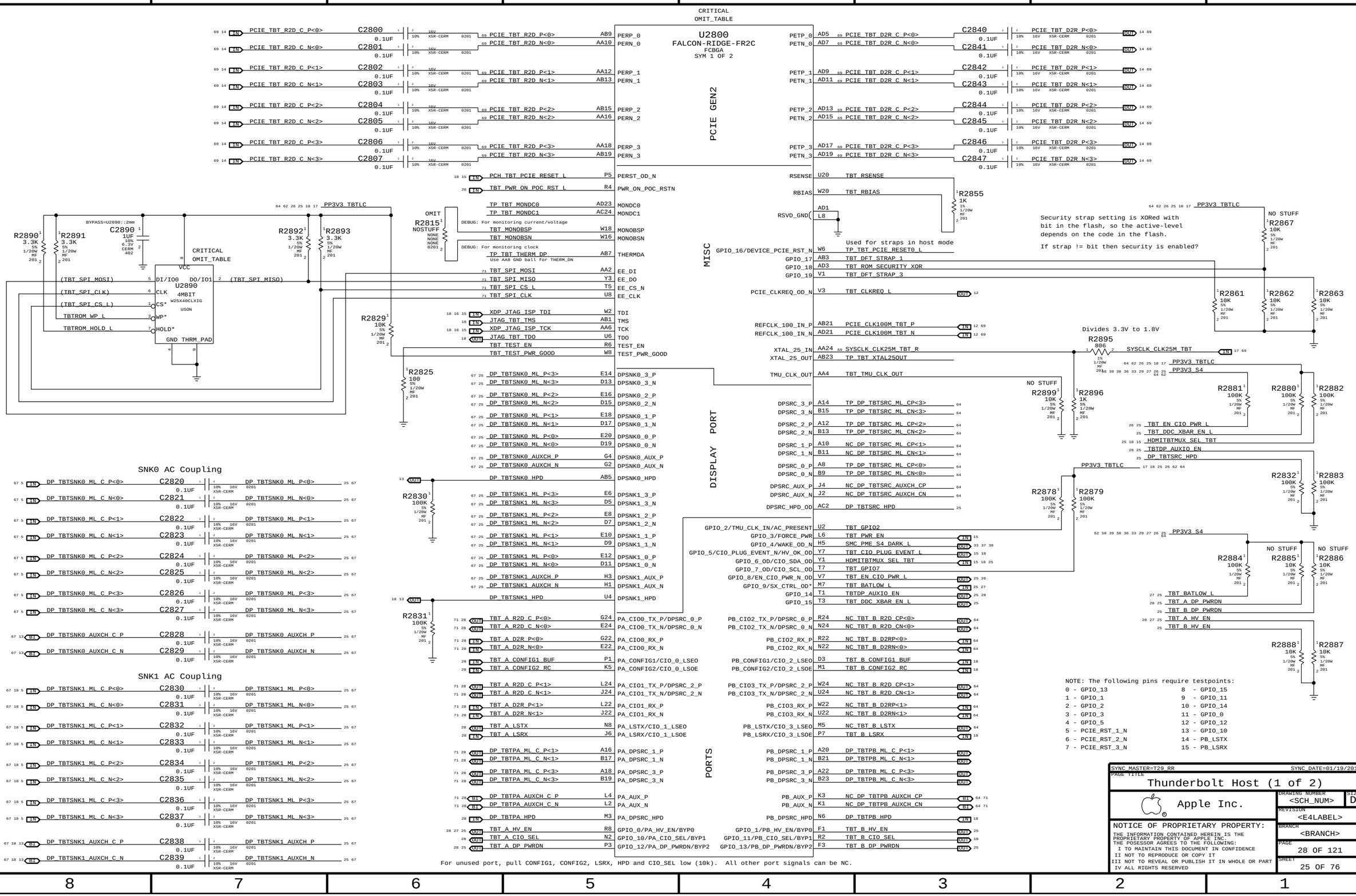
SYNC MASTER=J41_MLB SYNC DATE=02/06/2013

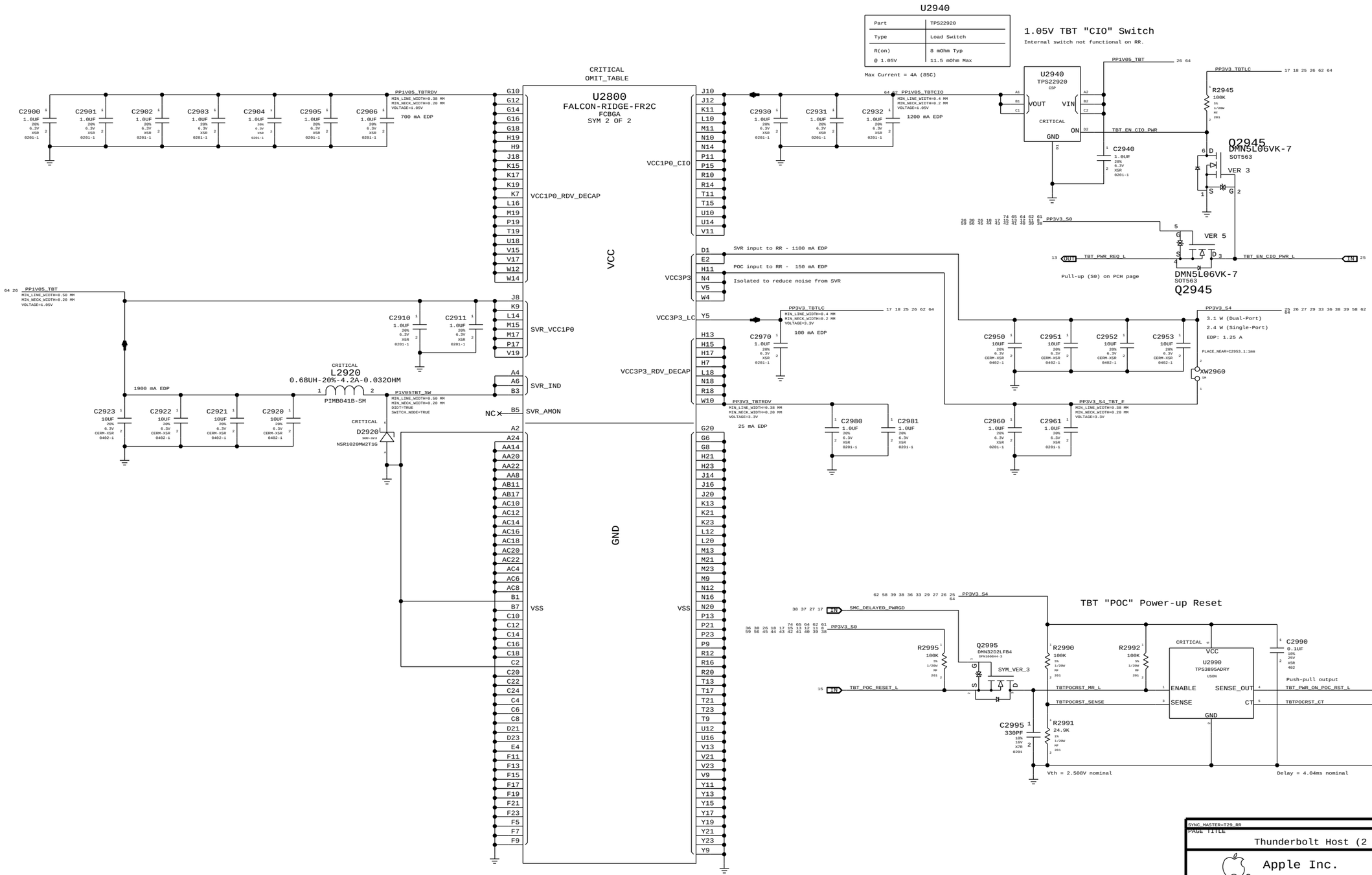
PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 27 OF 121
SHEET 24 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


CRITICAL
OMIT_TABLE
U2800
FALCON-RIDGE-FR2C
FCBGA
SYM 1 OF 2
PCIE GEN2
MISC
DISPLAY PORT
PORTS
PERP_0
PERN_0
PERP_1
PERN_1
PERP_2
PERN_2
PERP_3
PERN_3
PERST_OD_N
PWR_ON_POC_RSTN
MONDC0
MONDC1
MONOBSP
MONOBSN
THERMDA
EE_DI
EE_DO
EE_CS_N
EE_CLK
TDI
TMS
TCK
TDO
TEST_EN
TEST_PWR_GOOD
DPSNK0_3_P
DPSNK0_3_N
DPSNK0_2_P
DPSNK0_2_N
DPSNK0_1_P
DPSNK0_1_N
DPSNK0_0_P
DPSNK0_0_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
DPSNK1_3_P
DPSNK1_3_N
DPSNK1_2_P
DPSNK1_2_N
DPSNK1_1_P
DPSNK1_1_N
DPSNK1_0_P
DPSNK1_0_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
PA_CIO0_TX_P/DPSRC_0_P
PA_CIO0_TX_N/DPSRC_0_N
PA_CIO0_RX_P
PA_CIO0_RX_N
PA_CONFIG1/CIO_0_LSEO
PA_CONFIG2/CIO_0_LSOE
PA_CIO1_TX_P/DPSRC_2_P
PA_CIO1_TX_N/DPSRC_2_N
PA_CIO1_RX_P
PA_CIO1_RX_N
PA_LSTX/CIO_1_LSEO
PA_LSRX/CIO_1_LSOE
PA_DPSRC_1_P
PA_DPSRC_1_N
PA_DPSRC_3_P
PA_DPSRC_3_N
PA_AUX_P
PA_AUX_N
PA_DPSRC_HPD
GPIO_0/PA_HV_EN/BYP0
GPIO_10/PA_CIO_SEL/BYP1
GPIO_12/PA_DP_PWRDN/BYP2
PB_CIO2_TX_P/DPSRC_0_P
PB_CIO2_TX_N/DPSRC_0_N
PB_CIO2_RX_P
PB_CIO2_RX_N
PB_CONFIG1/CIO_2_LSEO
PB_CONFIG2/CIO_2_LSOE
PB_CIO3_TX_P/DPSRC_2_P
PB_CIO3_TX_N/DPSRC_2_N
PB_CIO3_RX_P
PB_CIO3_RX_N
PB_LSTX/CIO_3_LSEO
PB_LSRX/CIO_3_LSOE
PB_DPSRC_1_P
PB_DPSRC_1_N
PB_DPSRC_3_P
PB_DPSRC_3_N
PB_AUX_P
PB_AUX_N
PB_DPSRC_HPD
GPIO_1/PB_HV_EN/BYP0
GPIO_11/PB_CIO_SEL/BYP1
GPIO_13/PB_DP_PWRDN/BYP2
PETP_0
PETN_0
PETP_1
PETN_1
PETP_2
PETN_2
PETP_3
PETN_3
RSENSE
RBIAS
RSVD_GND
GPIO_16/DEVICE_PCIE_RST_N
GPIO_17
GPIO_18
GPIO_19
PCIE_CLKREQ_OD_N
REFCLK_100_IN_P
REFCLK_100_IN_N
XTAL_25_IN
XTAL_25_OUT
TMU_CLK_OUT
DPSRC_3_P
DPSRC_3_N
DPSRC_2_P
DPSRC_2_N
DPSRC_1_P
DPSRC_1_N
DPSRC_0_P
DPSRC_0_N
DPSRC_AUX_P
DPSRC_AUX_N
DPSRC_HPD_OD
GPIO_2/TMU_CLK_IN/AC_PRESENT
GPIO_3/FORCE_PWR
GPIO_4/WAKE_OD_N
GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD
GPIO_6_OD/CIO_SDA_OD
GPIO_7_OD/CIO_SCL_OD
GPIO_8/EN_CIO_PWR_N_OD
GPIO_9/SX_CTRL_OD*
GPIO_14
GPIO_15
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PCH_TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TP_TBT_MONDC0
TP_TBT_MONDC1
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TP_TBT_THERM_DP
Use AA8 GND ball for THERM_DN
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
XDP_JTAG_ISP_TDI
JTAG_TBT_TMS
XDP_JTAG_ISP_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_HPD
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_HPD
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_CONFIG1_BUF
TBT_A_CONFIG2_RC
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_C_N
DP_TBTPA_HPD
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_RSENSE
TBT_RBIAS
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT_R
TP_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
TP_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>
NC_DP_TBTSRC_ML_CP<1>
NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>
NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN
DP_TBTSRC_HPD
TBT_GPIO2
TBT_PWR_EN
SMC_PME_S4_DARK_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
NC_TBT_B_R2D_CP<0>
NC_TBT_B_R2D_CN<0>
NC_TBT_B_D2RP<0>
NC_TBT_B_D2RN<0>
TBT_B_CONFIG1_BUF
TBT_B_CONFIG2_RC
NC_TBT_B_R2D_CP<1>
NC_TBT_B_R2D_CN<1>
NC_TBT_B_D2RP<1>
NC_TBT_B_D2RN<1>
NC_TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
NC_DP_TBTPB_AUXCH_CP
NC_DP_TBTPB_AUXCH_CN
DP_TBTPB_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
PP3V3_TBTLC
BYPASS=U2890::2mm
VCC
U2890
4MBIT
W25X40CLXIG
USON
DI/IO0
DO/IO1
CLK
CS*
WP*
HOLD*
GND
THRM_PAD
(TBT_SPI_MOSI)
(TBT_SPI_MISO)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
R2890 3.3K
R2891 3.3K
C2890 1UF
R2892 3.3K
R2893 3.3K
R2829 10K
R2825 100
OMIT
R2815 NOSTUFF
R2855 1K
Used for straps in host mode
Security strap setting is XORed with
bit in the flash, so the active-level
depends on the code in the flash.
If strap != bit then security is enabled?
NO STUFF
R2867 10K
R2861 10K
R2862 10K
R2863 10K
Divides 3.3V to 1.8V
R2895 806
SYSCLK_CLK25M_TBT
PP3V3_S4
R2896 1K
R2899 10K
R2881 100K
R2880 100K
R2882 100K
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
R2878 100K
R2879 100K
R2832 100K
R2883 100K
R2884 100K
R2885 10K
R2886 10K
TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R2888 10K
R2887 10K
R2830 100K
R2831 100K
SNK0 AC Coupling
SNK1 AC Coupling
C2800 0.1UF
C2801 0.1UF
C2802 0.1UF
C2803 0.1UF
C2804 0.1UF
C2805 0.1UF
C2806 0.1UF
C2807 0.1UF
C2820 0.1UF
C2821 0.1UF
C2822 0.1UF
C2823 0.1UF
C2824 0.1UF
C2825 0.1UF
C2826 0.1UF
C2827 0.1UF
C2828 0.1UF
C2829 0.1UF
C2830 0.1UF
C2831 0.1UF
C2832 0.1UF
C2833 0.1UF
C2834 0.1UF
C2835 0.1UF
C2836 0.1UF
C2837 0.1UF
C2838 0.1UF
C2839 0.1UF
C2840 0.1UF
C2841 0.1UF
C2842 0.1UF
C2843 0.1UF
C2844 0.1UF
C2845 0.1UF
C2846 0.1UF
C2847 0.1UF
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=T29_RR
SYNC_DATE=01/19/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
28 OF 121
SHEET
25 OF 76
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=T29_RR SYNC_DATE=12/17/2012

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 29 OF 121

SHEET 26 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

TBT 15V Boost Regulator

62 56 50 49 42 41 64 PPBUS_G3H
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/20W MF 201
C3080 0.1UF 10% 25V X5R 402
R3081 150K 5% 1/20W MF 201
TBTBST_PWREN_DIV_L
TBTBST_PWREN_L

Q3005 DMN32D2LFB4 SYM_VER_2
28 25 IN TBT_A_HV_EN

CRITICAL
Q3080 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_S4SW_TBTBST_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

R3091 200K 1% 1/20W MF 201 <R1>
R3092 73.2K 1% 1/20W MF 201 <R2>

CRITICAL
L3095 6.8UH-4.0A PIMB062D-SM

CRITICAL
D3095 POWERDI-123 DFLS230L

PP15V_TBT 28 62 64
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

TBTBST_SNS1
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

R3089 0 5% 1/20W MF 0201

TBTBST_SNS2
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

XW3095 SM PLACE_NEAR=C3095.1:2 mm

TBTBST_VSNS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

CRITICAL
U3090 LT3957 QFN

27	VIN	SNS1	6
8	SW	SNS2	3
9	SW	NC	1, 2, 16, 35, 36
20	SW	FBX	31
21	SW		
38	SW		
25	EN/UVLO		
28	INTVCC		
30	VC		
33	RT		
32	SS		
34	SYNC		
4, 23, 24, 37	SGND		
12, 13, 14, 15, 16, 17	GND		

SGND shorted to GND inside package, no XW necessary.

R3090 49.9K 1% 1/16W MF-LF 402
C3088 22PF 5% 50V CER-C0G 0402
TBTBST_VSNS_RC
TBTBST_FBX
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

R3095 133K 1% 1/16W MF-LF 402 <Ra>
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>
NO STUFF
C3089 100PF 5% 50V CERM 402

Vout = 1.6V * (1 + Ra / Rb)

C3095 10UF 20% 25V X5R-CERM 0603
C3097 10UF 20% 25V X5R-CERM 0603
C3096 10UF 20% 25V X5R-CERM 0603
C3098 10UF 20% 25V X5R-CERM 0603
C3084 10UF 20% 25V X5R-CERM 0603
C3309A 10UF 20% 25V X5R-CERM 0603
C3099 0.001UF 10% 50V X7R-CERM 0402
C3085 10UF 20% 25V X5R-CERM 0603
C3309B 10UF 20% 25V X5R-CERM 0603

C3081 2.2UF 20% 10V X5R-CERM 402
C3092 2.2UF 20% 10V X5R-CERM 402
C3087 47PF 5% 25V C0G 0201
C3082 2.2UF 20% 10V X5R-CERM 402
C3093 3300PF 10% 10V X7R-CERM 0201
R3093 10K 1% 1/20W MF 201
R3094 41.2K 1% 1/20W MF 201
C3094 0.33UF 10% 6.3V CERM-X5R 402

TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Q3088 DMN5L06VK-7 SOT563 VER 3
Max Vgs: 10V
R3088 330K 5% 1/20W MF 201
TBTBST_SHDN_DIV
R3087 330K 5% 1/20W MF 201
Q3088 DMN5L06VK-7 SOT563 VER 3
SMC_DELAYED_PWRGD
IN 17 26 37 38

BATLOW# Isolation

Q3000 DMN32D2LFB4 SYM_VER_3
PP3V3_S4 25 26 29 33 36 38 39 58 62 64
Pull-up on RR page
37 13 IN PM_BATLOW_L
TBT_BATLOW_L OUT 25 27
TBT_BATLOW_L 25 27
MAKE_BASE=TRUE

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012
PAGE TITLE: TBT Power Support
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 30 OF 121
SHEET: 27 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
CRITICAL
C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V XSR-CERM-1 603
C3281 0.1UF 10% 16V XSR-CERM 0201
PP15V_TBT 15.75V Max
C3215 4.7UF 10% 25V XSR-CERM 0603
C3210 0.1UF 10% 25V XSR 402
CRITICAL
U3210
CD3211A1RGP
QFN
V3P3
VHV
ENHVU
EN
HV_EN
S0
V3P3OUT
OUT
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
C3285 0.1UF 10% 16V XSR-CERM 0201
C3286 10UF 20% 6.3V CERM-XSR 0402
C3211 0.1UF 10% 25V XSR 402
PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_BUF_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
R3210 22.6K 1% 1/20W MF 201
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
12V: See below
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/20W MF 201 <RHVS3>
R3214 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210.
Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V XSR-CERM 0201
SIGNAL_MODEL=TBT_MUX
VDD
CRITICAL
U3220
CBTL05024
HVQFN24-COMBO
TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX (IPU)
LSRX (IPO)
HPDOUT
TB_ENA
AUXIO_EN
DP_PD
(IPU) AUXIO-
(IPD) AUXIO+
CA_DET
DPML0+
DPML0-
HPD
GND THMPAD
TBT: RX_1
TBT: LSX_A_R2P/P2R (P/N)

GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V CERM-XSR-1 201
C3276 0.47UF 20% 4V CERM-XSR-1 201
C3230 0.1UF 10% 16V XSR-CERM 0201
C3231 0.1UF 10% 16V XSR-CERM 0201
C3232 0.22UF 20% 6.3V XSR 0201
C3233 0.22UF 20% 6.3V XSR 0201
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTSNK0_DDC_DATA
DP_TBTSNK0_DDC_CLK
TBT_A_CONFIG1_BUF
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT_A_CONFIG1_RC
TBT_A_LSX_ML_P<1>
TBT_A_LSX_ML_N<1>
TBT_A_HPD

Thunderbolt Connector A

CRITICAL
L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F
C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC
R3201 12 5% 1/20W MF 201
TBT Dir
DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
C3202 0.01UF 10% 16V XSR-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

J3200
MDP-J11
F-RT-TH
CRITICAL
514-0818
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS

GND_VOID=TRUE (Both C's)
C3274 0.47UF 20% 4V CERM-XSR-1 201
C3275 0.47UF 20% 4V CERM-XSR-1 201
C3278 0.22UF 20% 6.3V XSR 0201
C3279 0.22UF 20% 6.3V XSR 0201
R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R 0201
C3295 330PF 10% 16V X7R 0201
R3241 100K 5% 1/20W MF 201

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3205 0.01UF 10% 25V XSR-CERM 0201
C3206 0.01UF 10% 25V XSR-CERM 0201
TBTACONN_7_C
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_0
TBT: TX_1
C3270 0.22UF 20% 6.3V XSR 0201
C3271 0.22UF 20% 6.3V XSR 0201
C3272 0.22UF 20% 6.3V XSR 0201
C3273 0.22UF 20% 6.3V XSR 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=T29_RR SYNC_DATE=10/26/2012
PAGE TITLE: Thunderbolt Connector A
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 32 OF 121
SHEET: 28 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Sense resistor on sensor page

PP3V3_WLAN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
37 38 39 41 64

PP3V3_WLAN_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
Max Current = 2A (85C)

U3550
TPS22924
CSP
CRITICAL
A1 VOUT
B1
A2 VIN
B2 ON
C2
GND
C1

PP3V3_S5
8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 64 74

SMC_WIFI_PWR_EN
IN 29 37 39

C3550
1.0UF
20%
6.3V
X5R
0201-1

514S0335
CRITICAL
J3501
SSD-K99
F-RT-SM1

C3521
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:5mm

AIRPORT

		WIFI_EVENT_L	OUT 37 38 64
69 64 PCIE_AP_R2D_N	C3531 0.1UF 10% XSR-CERM 16V 0201	PCIE_AP_R2D_C_N	IN 14 69
69 64 PCIE_AP_R2D_P	C3530 0.1UF 10% XSR-CERM 16V 0201	PCIE_AP_R2D_C_P	IN 14 69
		PCIE_CLK100M_AP_N	IN 12 64 69
		PCIE_CLK100M_AP_P	IN 12 64 69
		PCIE_AP_D2R_P	OUT 14 64 69
		PCIE_AP_D2R_N	OUT 14 64 69

PP3V3_S4
25 26 27 29 33 36 38 39 58 62 64

C3532
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:1.5mm

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

APCLKRQ:ISOL
R3553
100K
5%
1/20W
MF
201

R3554
232K
1%
1/20W
MF
201

P3V3WLAN_VMON

PP3V3_S5
8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 64 74

C3540
0.1UF
10%
6.3V
CERM-X5R
0201

U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND

R3558
0
5%
1/20W
MF
0201

64 AP_RESET_CONN_L
AP_RESET_CONN_R_L
AP_RESET_L
IN 15

SMC_WIFI_PWR_EN
IN 29 37 39

64 AP_CLKREQ_Q_L
AP_CLKREQ_R_L

R3555
100K
1%
1/20W
MF
201

APCLKRQ:ISOL
R3556
0
5%
1/20W
MF
0201

APCLKRQ:BIDIR
R3557
0
5%
1/20W
MF
0201

AP_CLKREQ_L
BI 12

NOSTUFF
R3559
0
5%
1/20W
MF
0201

PCIe Wake Muxing

60 59 58 13 11 10 PP3V3_S5 17 16 15 57 42 33 74 64 62

R3561
100K
5%
1/20W
MF
201

C3560
0.1UF
10%
6.3V
CERM-X5R
0201

U3560
NC7SB3157P6XG
SC70
VER-3
CRITICAL
VCC
GND
S
B0
B1
A

SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

AP_S0IX_WAKE_SEL
IN 15

PCIE_WAKE_L
OUT 13 31 64

AP_S0IX_WAKE_L
OUT 15

AP_PCIE_WAKE_L

NOSTUFF
R3560
0
5%
1/20W
MF
0201

36 33 29 27 26 25 33 38 PP3V3_S4

BLUETOOTH

C3510
0.1UF
10%
6.3V
CERM-X5R
0201

U3510
USB3740
DFN
CRITICAL
VDD
DP
DM
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
NC

USB_BT_P
BI 14 68

USB_BT_N
BI 14 68

68 64 USB_BT_CONN_P
68 64 USB_BT_CONN_N

BT_WAKE

PM_SLP_S4_L
IN 13 18 36 37 59

SIGNAL_MODEL=BT_MUX

SEL	OUTPUT
L	BT_WAKE (1)
H	USB_BT (2)

SMC_PME_S4_WAKE_L
OUT 36 37 39

NO_XNET_CONNECTION=TRUE
Q3510
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
D
G
S

R3512
15K
1%
1/20W
MF
201

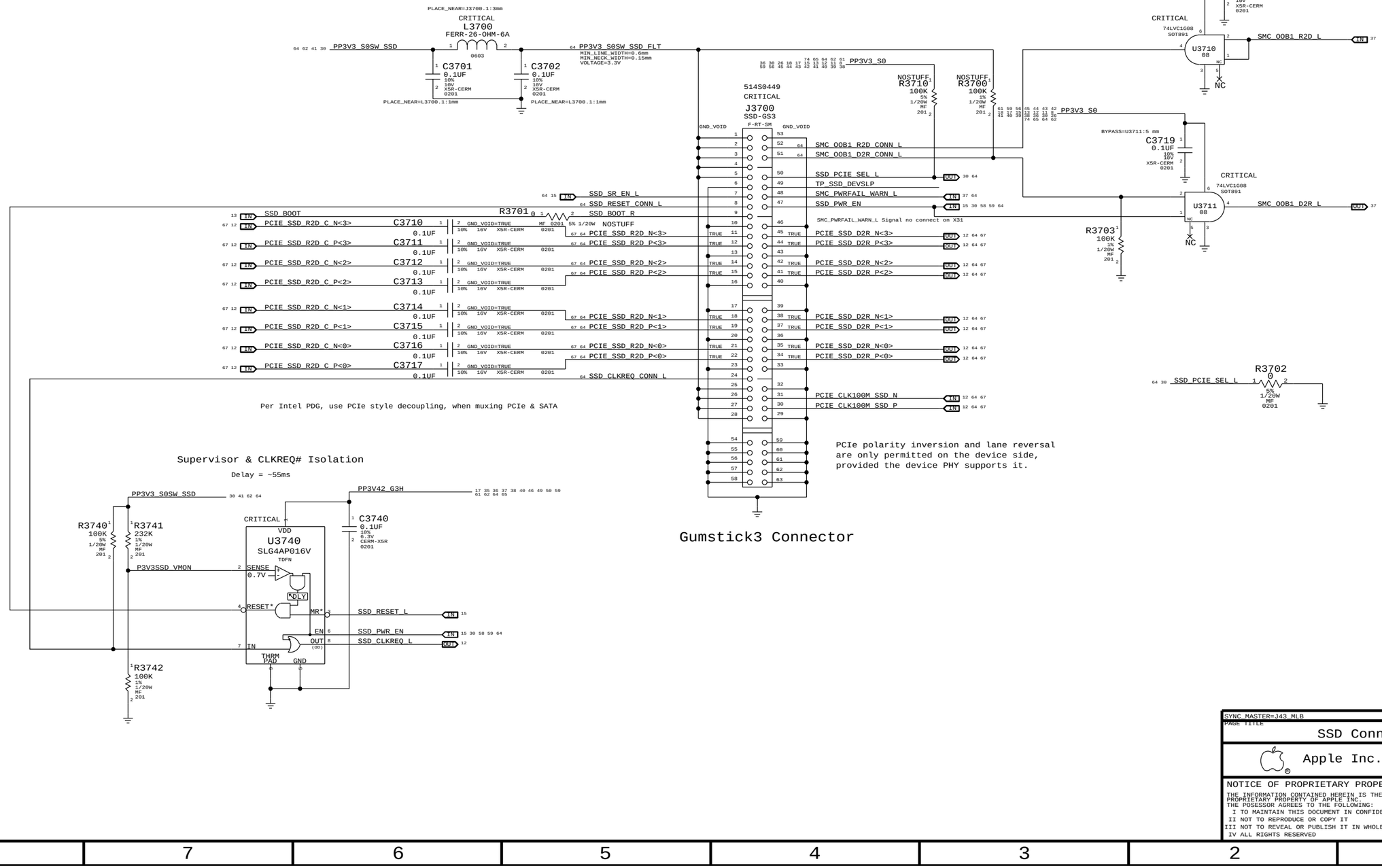
SYNC_MASTER=J41_MLB
SYNC_DATE=02/06/2013

PAGE TITLE
Wireless Connector

Apple Inc.

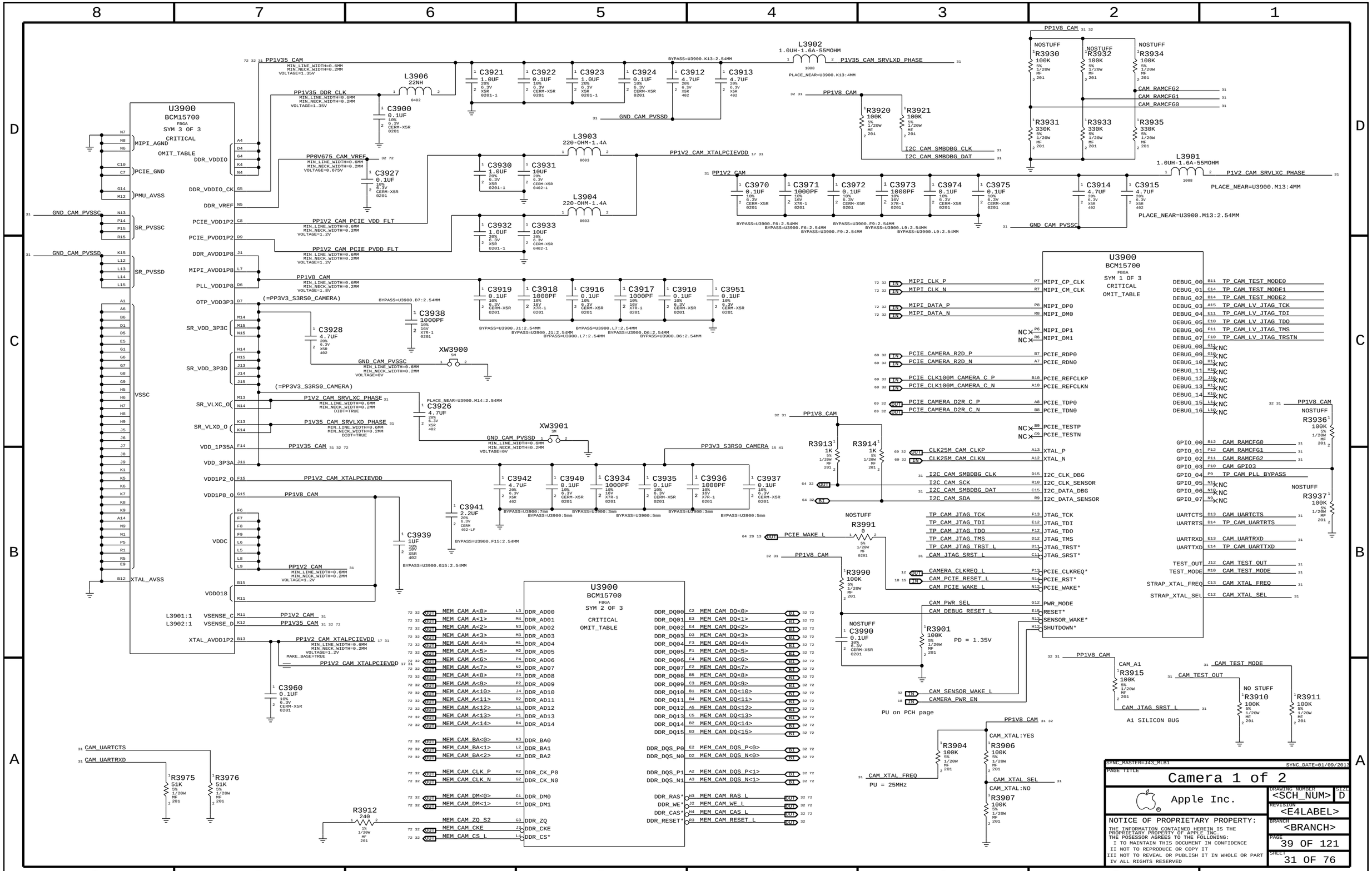
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 35 OF 121
SHEET 29 OF 76

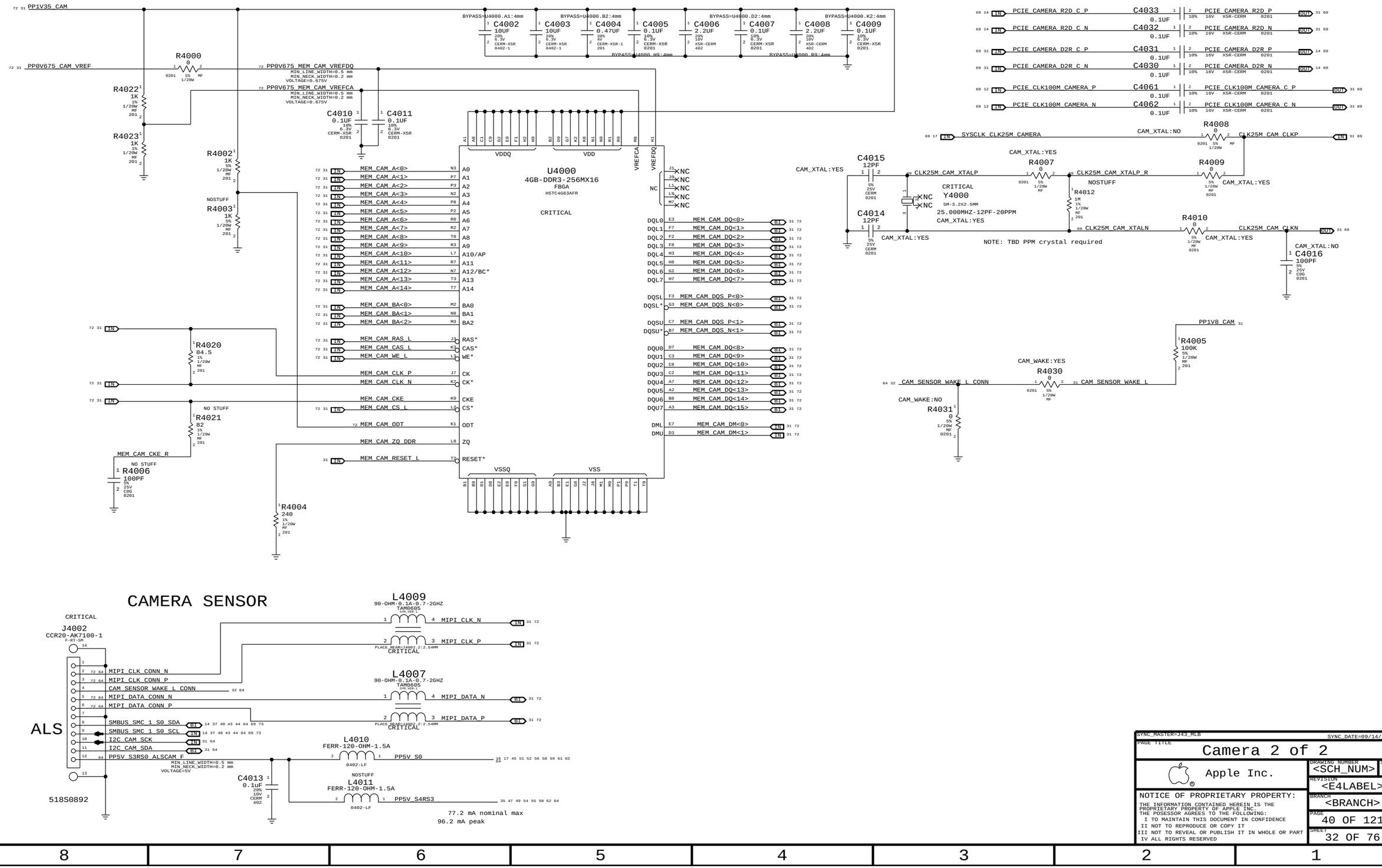
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

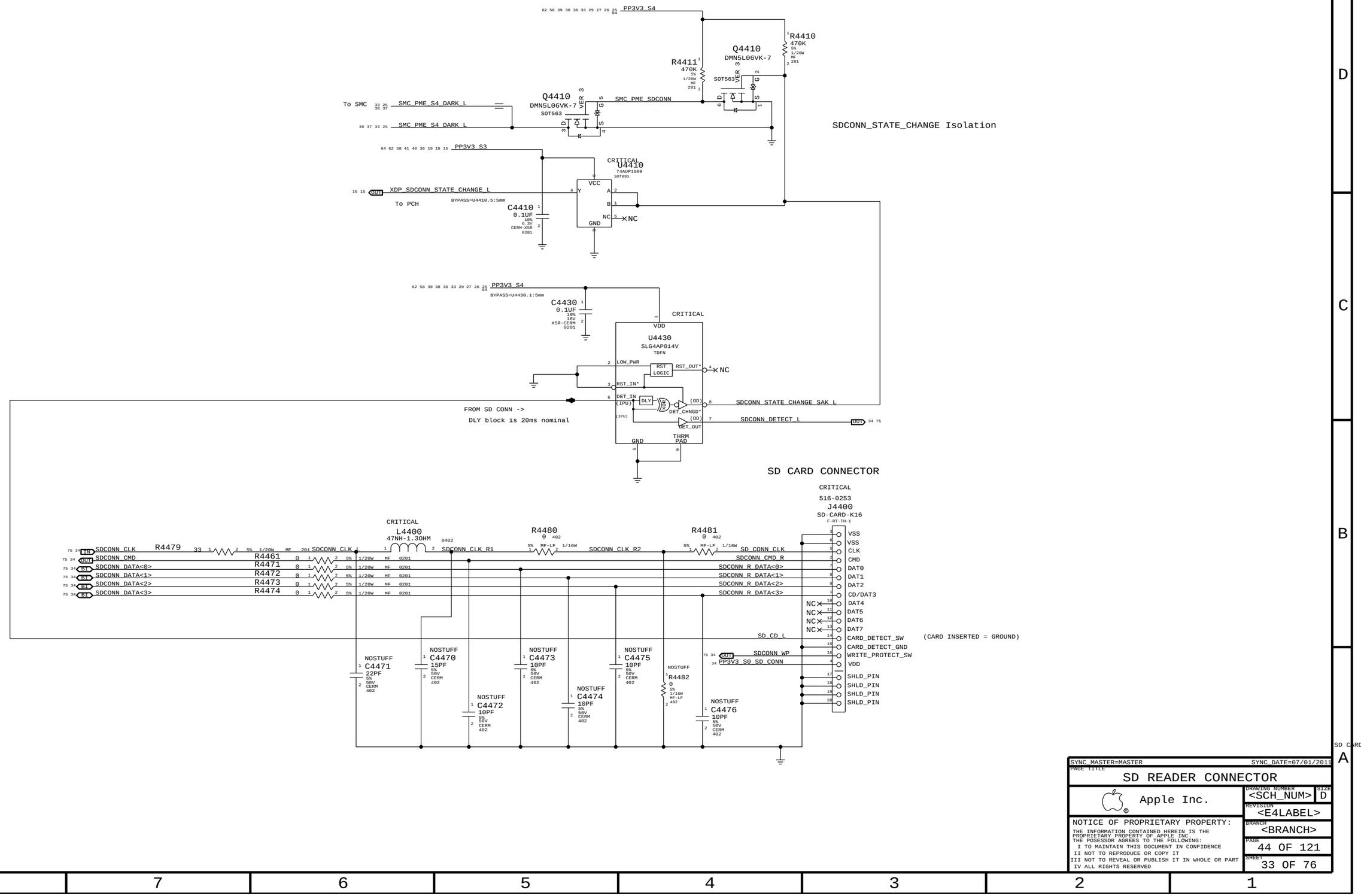


SYNC_MASTER=J43_MLB	SYNC_DATE=02/20/2013
PAGE TITLE	SSD Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 37 OF 121
	SHEET 30 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
MIPI_AGND
PCIE_GND
PMU_AVSS
SR_PVSSC
SR_PVSSD
VSSC
DDR_VDDIO
DDR_VDDIO_CK
DDR_VREF
PCIE_VDD1P2
PCIE_PVDD1P2
DDR_AVDD1P8
MIPI_AVDD1P8
PLL_VDD1P8
OTP_VDD3P3
SR_VDD_3P3C
SR_VDD_3P3D
SR_VLXC_0
SR_VLXD_0
VDD_1P35A
VDD_3P3A
VDD1P2_O
VDD1P8_O
VDDC
VDD018
XTAL_AVSS
XTAL_AVDD1P2
PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP1V8_CAM
PP1V2_CAM_XTALPCIEVDD
PP1V2_CAM_SRVLXC_PHASE
PP1V35_CAM_SRVLXD_PHASE
PP1V2_CAM
PP1V8_CAM
PP3V3_S3RS0_CAMERA
GND_CAM_PVSSC
GND_CAM_PVSSD
GND_CAM_PVSSD
L3902
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
L3901
1.0UH-1.6A-55MOHM
L3902:1 VSENSE_C
L3902:1 VSENSE_D
XW3900
XW3901
R3912
240
R3913
1K
R3914
1K
R3920
100K
R3921
100K
R3930
100K
R3931
330K
R3932
100K
R3933
330K
R3934
100K
R3935
330K
R3936
100K
R3937
100K
R3975
51K
R3976
51K
C3900
0.1UF
C3927
0.1UF
C3928
4.7UF
C3938
1000PF
C3926
4.7UF
C3939
1UF
C3941
2.2UF
C3960
0.1UF
C3921
1.0UF
C3922
0.1UF
C3923
1.0UF
C3924
0.1UF
C3912
4.7UF
C3913
4.7UF
C3930
1.0UF
C3931
10UF
C3932
1.0UF
C3933
10UF
C3970
0.1UF
C3971
1000PF
C3972
0.1UF
C3973
1000PF
C3974
0.1UF
C3975
0.1UF
C3914
4.7UF
C3915
4.7UF
C3919
0.1UF
C3918
1000PF
C3916
0.1UF
C3917
1000PF
C3910
0.1UF
C3951
0.1UF
C3942
4.7UF
C3940
0.1UF
C3934
1000PF
C3935
0.1UF
C3936
1000PF
C3937
0.1UF
C3990
0.1UF
NOSTUFF
R3991
0
R3990
100K
R3901
100K
PD = 1.35V
R3904
100K
R3906
100K
CAM_XTAL:YES
R3907
100K
CAM_XTAL:NO
R3915
100K
CAM_A1
R3910
100K
NO STUFF
R3911
100K
CAM_JTAG_SRST_L
A1 SILICON BUG
PU on PCH page
PU = 25MHz
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
DDR_AD00
DDR_AD01
DDR_AD02
DDR_AD03
DDR_AD04
DDR_AD05
DDR_AD06
DDR_AD07
DDR_AD08
DDR_AD09
DDR_AD10
DDR_AD11
DDR_AD12
DDR_AD13
DDR_AD14
DDR_BA0
DDR_BA1
DDR_BA2
DDR_CK_P0
DDR_CK_N0
DDR_DM0
DDR_DM1
DDR_ZQ
DDR_CKE
DDR_CS*
MEM_CAM_DQ<0>
MEM_CAM_DQ<1>
MEM_CAM_DQ<2>
MEM_CAM_DQ<3>
MEM_CAM_DQ<4>
MEM_CAM_DQ<5>
MEM_CAM_DQ<6>
MEM_CAM_DQ<7>
MEM_CAM_DQ<8>
MEM_CAM_DQ<9>
MEM_CAM_DQ<10>
MEM_CAM_DQ<11>
MEM_CAM_DQ<12>
MEM_CAM_DQ<13>
MEM_CAM_DQ<14>
MEM_CAM_DQ<15>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
DDR_DQ00
DDR_DQ01
DDR_DQ02
DDR_DQ03
DDR_DQ04
DDR_DQ05
DDR_DQ06
DDR_DQ07
DDR_DQ08
DDR_DQ09
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQS_P0
DDR_DQS_N0
DDR_DQS_P1
DDR_DQS_N1
DDR_RAS*
DDR_WE*
DDR_CAS*
DDR_RESET*
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
PCIE_WAKE_L
CAM_UARTCTS
CAM_UARTRXD
I2C_CAM_SMBDBG_CLK
I2C_CAM_SMBDBG_DAT
CAM_RAMCFG2
CAM_RAMCFG1
CAM_RAMCFG0
CAM_TEST_MODE
CAM_TEST_OUT
CAM_XTAL_FREQ
CAM_XTAL_SEL
SYNC_MASTER=J43_MLB1
SYNC_DATE=01/09/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
39 OF 121
SHEET
31 OF 76


PP1V35_CAM
PP0V675_CAM_VREF
R4000
R4022
1K
R4023
1K
R4002
1K
NOSTUFF
R4003
1K
PP0V675_MEM_CAM_VREFDQ
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.675V
PP0V675_MEM_CAM_VREFCA
C4010 0.1UF
C4011 0.1UF
BYPASS=U4000.A1:4mm
C4002 10UF
BYPASS=U4000.B2:4mm
C4003 10UF
C4004 0.47UF
C4005 0.1UF
BYPASS=U4000.D2:4mm
C4006 2.2UF
C4007 0.1UF
BYPASS=U4000.K2:4mm
C4008 2.2UF
C4009 0.1UF
BYPASS=U4000.H9:4mm
BYPASS=U4000.R9:4mm
U4000
4GB-DDR3-256MX16
FBGA
H5TC4G63AFR
CRITICAL
VDDQ
VDD
VREFCA
VREFDQ
NC
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC*
A13
A14
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
BA0
BA1
BA2
MEM_CAM_RAS_L
MEM_CAM_CAS_L
MEM_CAM_WE_L
RAS*
CAS*
WE*
MEM_CAM_CLK_P
MEM_CAM_CLK_N
CK
CK*
MEM_CAM_CKE
MEM_CAM_CS_L
CKE
CS*
MEM_CAM_ODT
ODT
MEM_CAM_ZQ_DDR
ZQ
MEM_CAM_RESET_L
RESET*
DQL0 MEM_CAM_DQ<0>
DQL1 MEM_CAM_DQ<1>
DQL2 MEM_CAM_DQ<2>
DQL3 MEM_CAM_DQ<3>
DQL4 MEM_CAM_DQ<4>
DQL5 MEM_CAM_DQ<5>
DQL6 MEM_CAM_DQ<6>
DQL7 MEM_CAM_DQ<7>
DQSL MEM_CAM_DQS_P<0>
DQSL* MEM_CAM_DQS_N<0>
DQSU MEM_CAM_DQS_P<1>
DQSU* MEM_CAM_DQS_N<1>
DQU0 MEM_CAM_DQ<8>
DQU1 MEM_CAM_DQ<9>
DQU2 MEM_CAM_DQ<10>
DQU3 MEM_CAM_DQ<11>
DQU4 MEM_CAM_DQ<12>
DQU5 MEM_CAM_DQ<13>
DQU6 MEM_CAM_DQ<14>
DQU7 MEM_CAM_DQ<15>
DML MEM_CAM_DM<0>
DMU MEM_CAM_DM<1>
VSSQ
VSS
R4020 84.5
R4021 82
NO STUFF
MEM_CAM_CKE_R
R4006 100PF
R4004 240
PCIE_CAMERA_R2D_C_P
PCIE_CAMERA_R2D_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
PCIE_CLK100M_CAMERA_P
PCIE_CLK100M_CAMERA_N
C4033 0.1UF
C4032 0.1UF
C4031 0.1UF
C4030 0.1UF
C4061 0.1UF
C4062 0.1UF
SYSCLK_CLK25M_CAMERA
R4008
CAM_XTAL:NO
CLK25M_CAM_CLKP
CAM_XTAL:YES
C4015 12PF
C4014 12PF
CLK25M_CAM_XTALP
CLK25M_CAM_XTALN
CRITICAL
Y4000
SM-3.2X2.5MM
25.000MHZ-12PF-20PPM
R4007
R4012 1M
NOSTUFF
R4009
R4010
CLK25M_CAM_CLKN
C4016 100PF
NOTE: TBD PPM crystal required
PP1V8_CAM
R4005 100K
CAM_WAKE:YES
R4030
CAM_SENSOR_WAKE_L_CONN
CAM_SENSOR_WAKE_L
CAM_WAKE:NO
R4031
CAMERA SENSOR
J4002
CCR20-AK7100-1
F-RT-SM
MIPI_CLK_CONN_N
MIPI_CLK_CONN_P
CAM_SENSOR_WAKE_L_CONN
MIPI_DATA_CONN_N
MIPI_DATA_CONN_P
SMBUS_SMC_1_S0_SDA
SMBUS_SMC_1_S0_SCL
I2C_CAM_SCK
I2C_CAM_SDA
PP5V_S3RS0_ALSCAM_F
ALS
518S0892
L4009
90-OHM-0.1A-0.7-2GHZ
TAM0605
MIPI_CLK_N
MIPI_CLK_P
L4007
MIPI_DATA_N
MIPI_DATA_P
L4010
FERR-120-OHM-1.5A
PP5V_S0
L4011
PP5V_S4RS3
C4013 0.1uF
77.2 mA nominal max
96.2 mA peak
SYNC_MASTER=J43_MLB
SYNC_DATE=09/14/2012
PAGE TITLE
Camera 2 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
40 OF 121
SHEET
32 OF 76
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=MASTER SYNC_DATE=07/01/2011

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

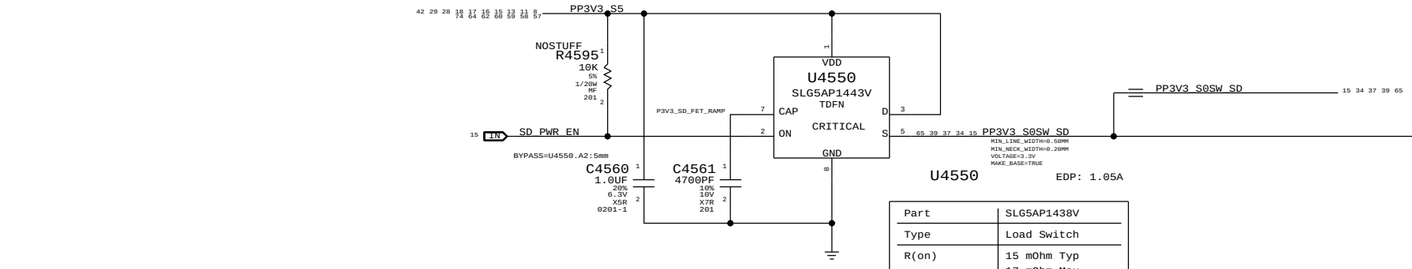
PAGE 44 OF 121

SHEET 33 OF 76

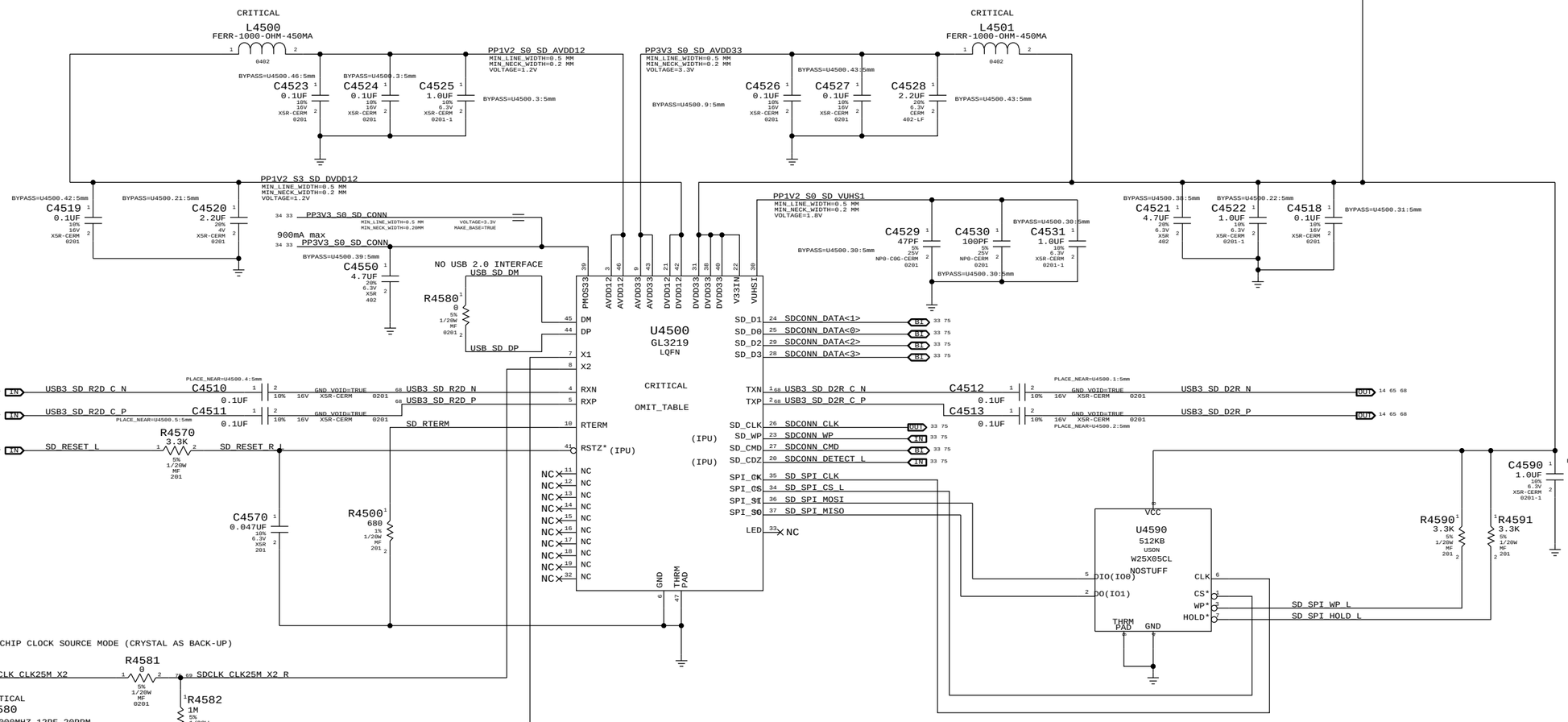
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

3.3V S3 SD Card Switch



Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

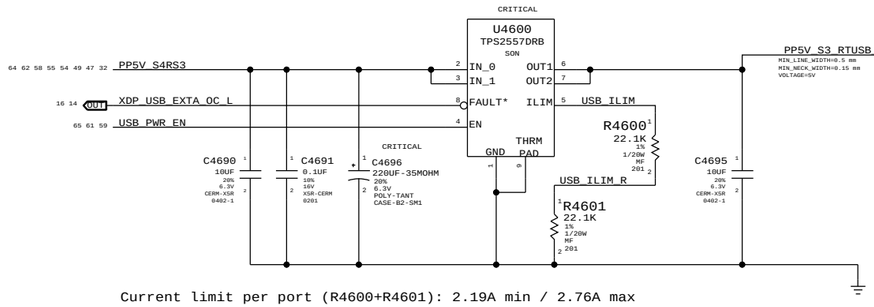


SYNC_MASTER=MASTER	SYNC_DATE=10/11/2010
PAGE TITLE	SD CONTROLLER (GL3219)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 45 OF 121
	SHEET 34 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

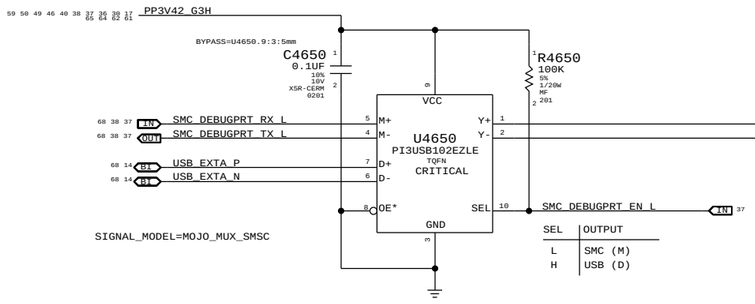
Right USB Port A

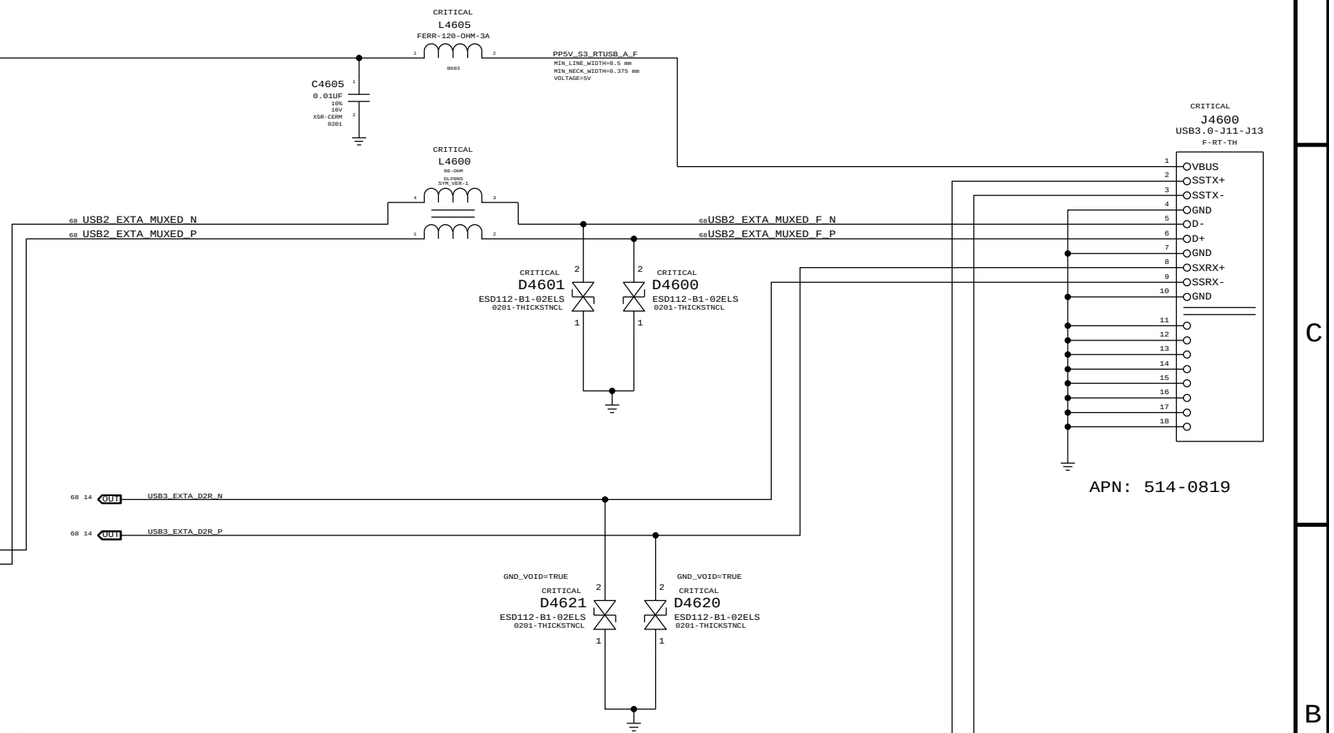
USB Port Power Switch



Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux





SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE: External A USB3 Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 46 OF 121

SHEET: 35 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

IPD Flex Connector

PLACE_NEAR=J4800.10:1.5MM
R4830
0
62 58 39 38 36 33 29 27 26 23 64 PP3V3_S4
5% 1/20W MF 0201
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm
C4800 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=J4800.10:1.5MM
PLACE_NEAR=J4800.14:1.5MM

L4820
FERR-120-OHM-1.5A
62 54 53 PP5V_S5
0402-LF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4810 0.1UF 10% 16V X5R-CERM 0201
PLACE_NEAR=J4800.14:1.5MM
50 49 46 40 38 37 35 30 17 65 64 62 61 59 PP3V42_G3H
BYPASS=J4800.19:1.5MM
C4820 0.1UF 10% 6.3V CERM-X5R 0201

TPAD_INTWAKE:SPLIT
PLACE_NEAR=R4844.1:1.5MM
R4841
0
(TPAD_WAKE_L)
5% 1/20W MF 0201

TPAD_INTWAKE:SHARED
R4843
0
39 37 29 OUT SMC_PME_S4_WAKE_L
To SMC
(TPAD_SPI_INT_S4_WAKE_L_CONN)
PLACE_NEAR=R4841.1:1.5MM

TPAD_INTWAKE:SHARED
R4844
0
PLACE_NEAR=J4800.8:1.5MM

TPAD_INTWAKE:SHARED
64 62 58 41 40 36 33 19 18 15 PP3V3_S3
Q4800
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
15 OUT TPAD_SPI_INT_L
To PCH
PLACE_NEAR=R4842.2:5MM

TPAD_INTWAKE:SPLIT
R4842
0
PLACE_NEAR=R4843.2:1.5MM

62 58 39 38 36 33 29 27 26 25 64 PP3V3_S4
C4841 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U4810:3mm

CRITICAL
74LVC2G08GT/S505
SOT833
59 37 36 29 18 13 IN PM_SLP_S4_L
15 IN TPAD_USB_IF_EN
From PCH
U4810
08
(TPAD_USB_IF_EN_CONN)
NOSTUFF
R4810
100K
5% 1/20W MF 201
CKPLUS_WAIVE=UNCONNECTED_PINS

74LVC2G08GT/S505
SOT833
59 37 36 29 18 13 IN PM_SLP_S4_L
15 IN TPAD_SPI_IF_EN
From PCH
U4810
08
(TPAD_SPI_IF_EN_CONN)

64 62 58 41 40 36 33 19 18 15 PP3V3_S3
R4860
100K
5% 1/20W MF 201
38 30 26 18 17 15 13 12 11 8 61 59 56 45 44 43 42 41 40 39 PP3V3_S0
Q4860
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
15 IN TPAD_SPI_CS_L
TPAD_SPI_CS_CONN_L

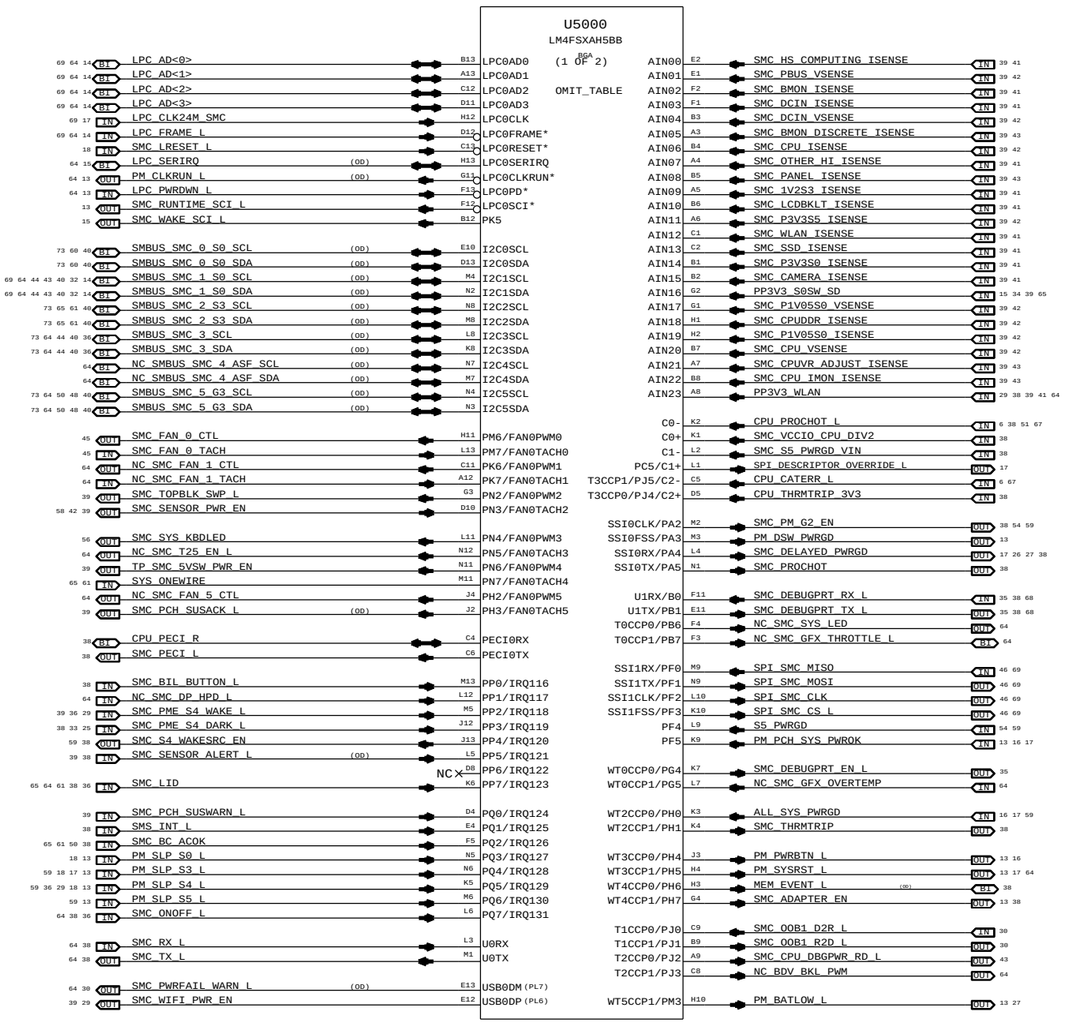
R4850
33
65 64 61 38 37 36 IN SMC_LID
15 68 OUT TPAD_SPI_MISO
5% 1/20W MF 201
PLACE_NEAR=J4800.2:2.54mm
64 TPAD_SPI_MISO_R
68 64 14 BI USB_TPAD_P
68 64 14 BI USB_TPAD_N
R4851
15 68 IN TPAD_SPI_CLK
PLACE_NEAR=J4800.7:2.54mm
64 TPAD_SPI_CLK_R
64 TPAD_WAKE_L
R4852
15 68 IN TPAD_SPI_MOSI
PLACE_NEAR=J4800.9:2.54mm
64 TPAD_SPI_MOSI_R
64 PP3V3_S4_IPD
R4853
PLACE_NEAR=J4800.12:2.54mm
64 TPAD_SPI_CS_R_L
64 TPAD_SPI_IF_EN_CONN
64 TPAD_SPI_INT_S4_WAKE_L_CONN
64 PP5V_S4_IPD
64 TPAD_USB_IF_EN_CONN
73 64 44 40 37 36 BI SMBUS_SMC_3_SDA
73 64 44 40 37 36 BI SMBUS_SMC_3_SCL
64 38 36 OUT SMC_LSOC_RST_L
(=PP3V42_G3H_IPD)
64 38 37 36 OUT SMC_ONOFF_L

CRITICAL
518S0884
J4800
TF13BS-20S-0.4SH
F-RT-SM-1
22
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21

SMBUS_SMC_3_SDA 36 37 40 44 64 73
SMBUS_SMC_3_SCL 36 37 40 44 64 73
SMC_ONOFF_L 36 37 38 64
SMC_LID 36 37 38 61 64 65
SMC_LSOC_RST_L 36 38 64
NOSTUFF C4832 100PF 5% 25V C0G 0201 BYPASS=J4800.6:1.5MM
NOSTUFF C4833 100PF 5% 25V C0G 0201 BYPASS=J4800.5:1.5MM
C4834 100PF 5% 25V C0G 0201 BYPASS=J4800.4:1.5MM
C4835 100PF 5% 25V C0G 0201 BYPASS=J4800.3:8.5MM
C4836 100PF 5% 25V C0G 0201 BYPASS=J4800.1:1.5MM

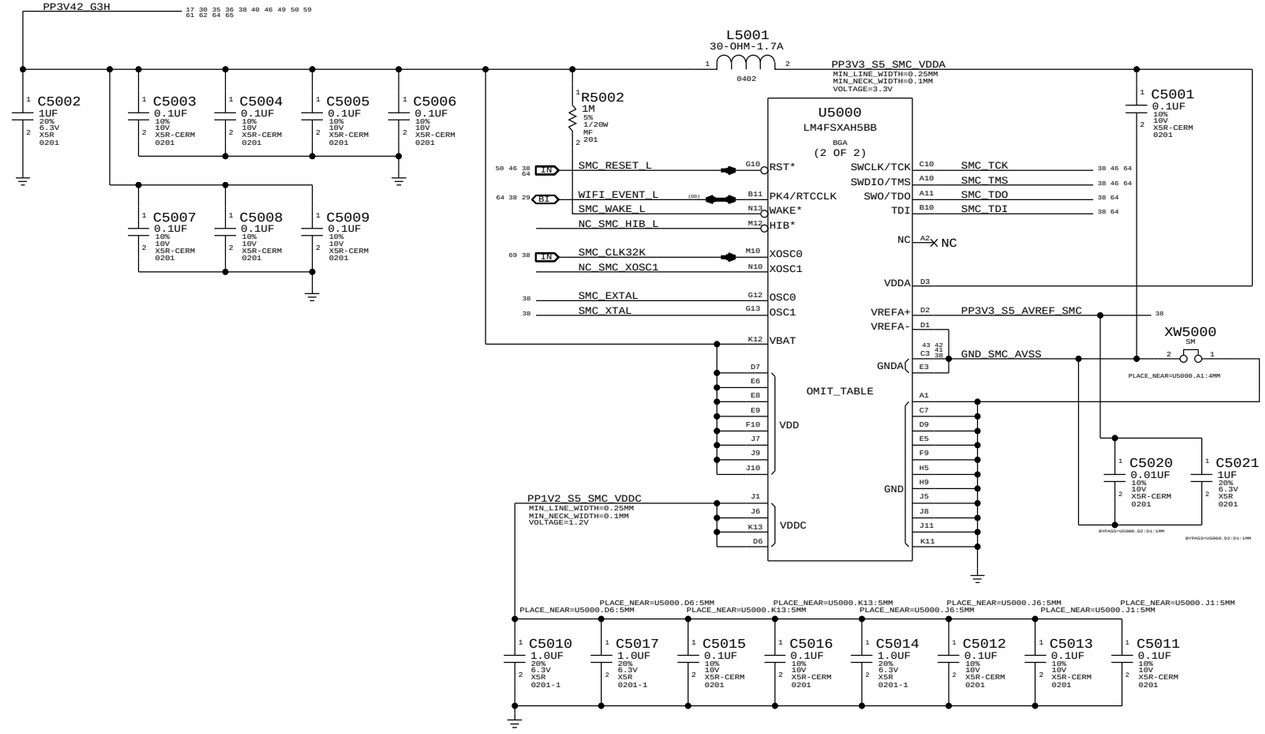
SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013
PAGE TITLE
IPD Connector
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 48 OF 121
SHEET 36 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

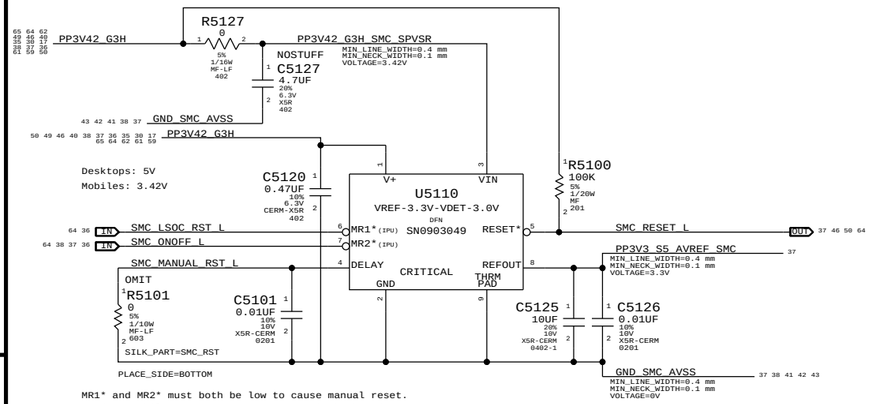
PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 50 OF 121
SHEET 37 OF 76

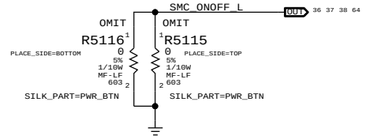
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SMC Reset "Button", Supervisor & AVREF Supply



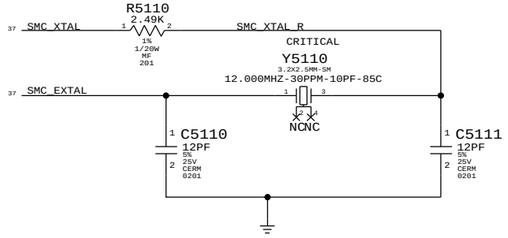
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

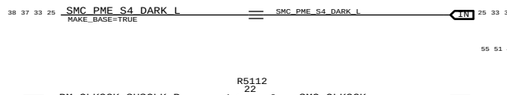
Debug Power "Buttons"

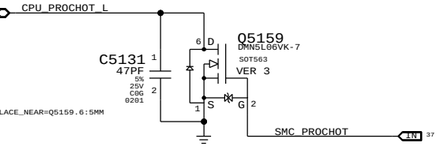


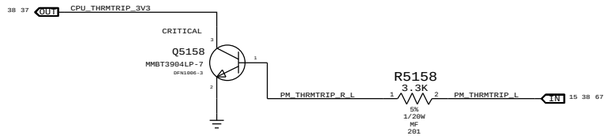
SMC Crystal Circuit

SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz

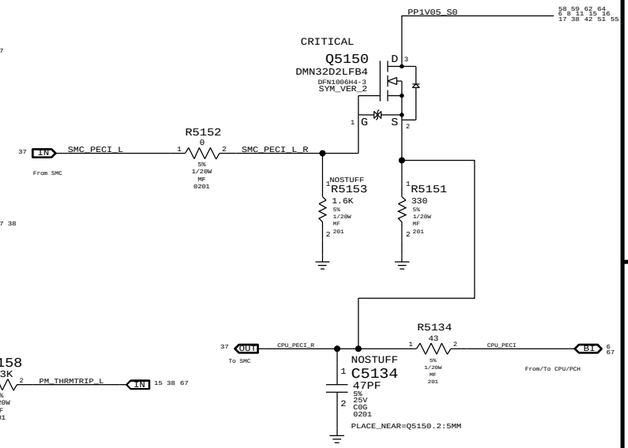


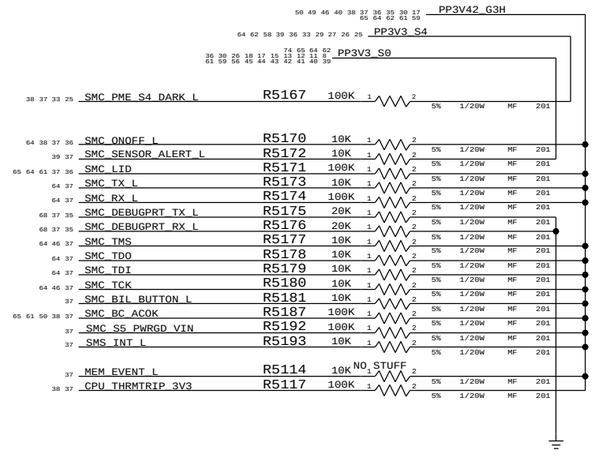






SMC12 PECI Support





SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

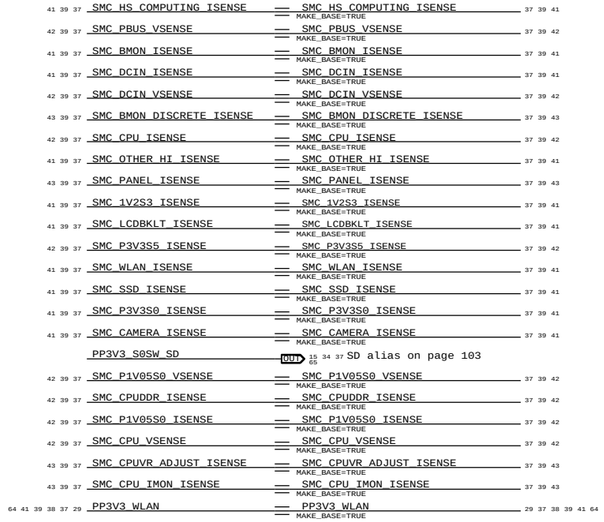
PAGE TITLE: SMC Shared Support

Apple Inc.

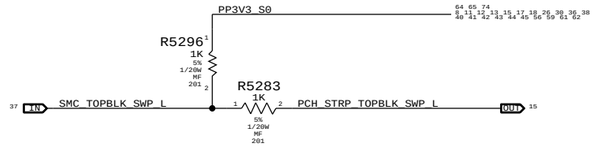
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 51 OF 121
SHEET: 38 OF 76

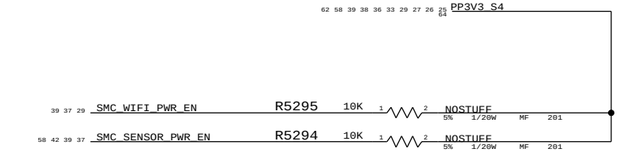
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

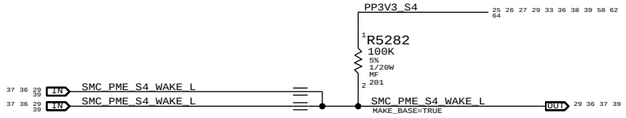
8	7	6	5	4	3	2	1

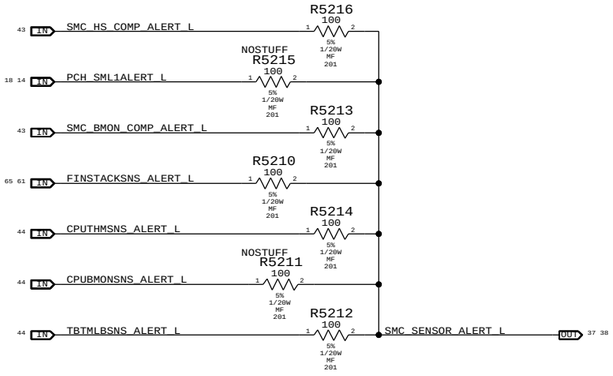


Top-Block Swap









SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE: SMC Project Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

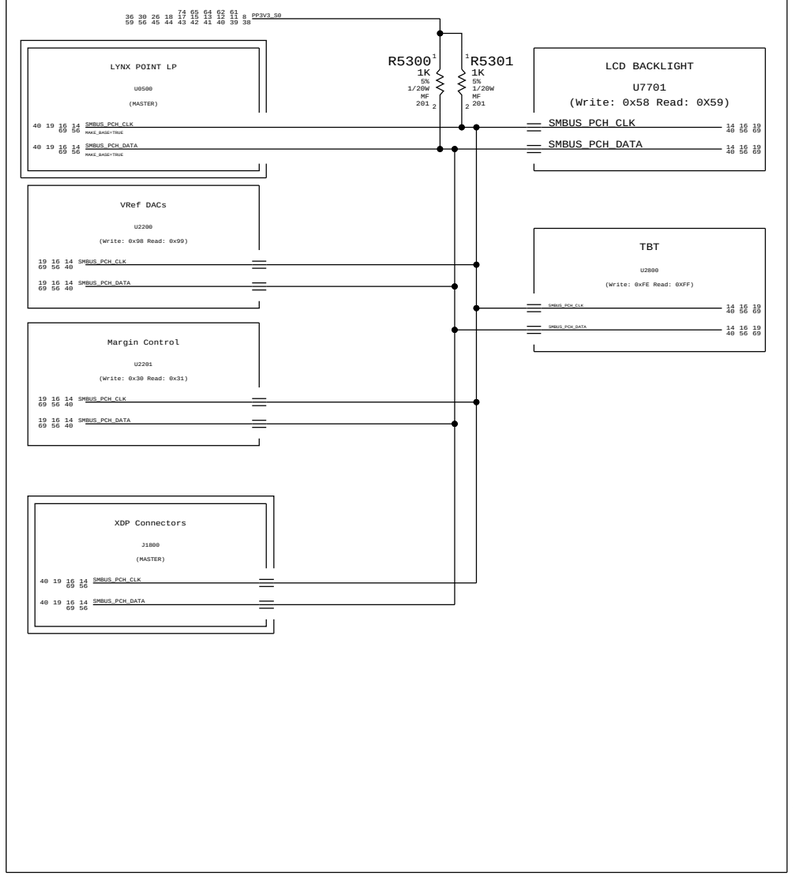
BRANCH: <BRANCH>

PAGE: 52 OF 121

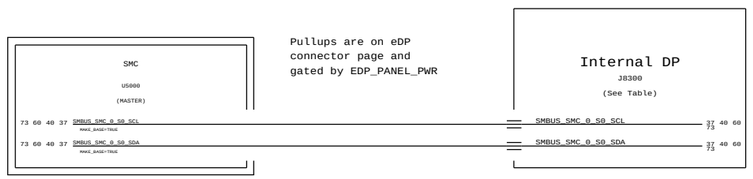
SHEET: 39 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LYNX POINT LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections

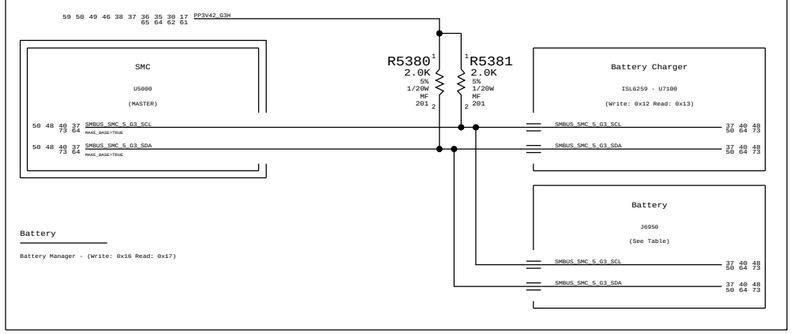


(* = Multiple options)

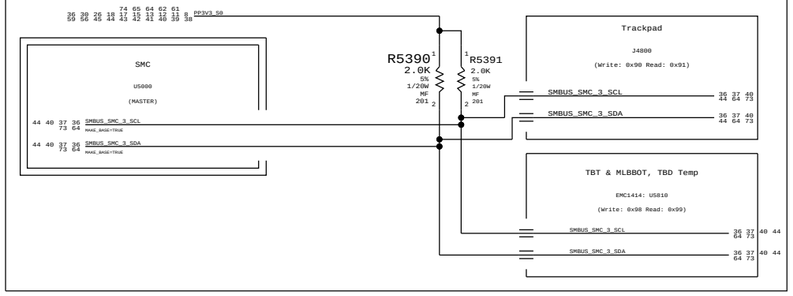
Internal DP

		J43			J41	
		Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x8B)	N	Y	*	Y	*	
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*	
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	*	Y	N	

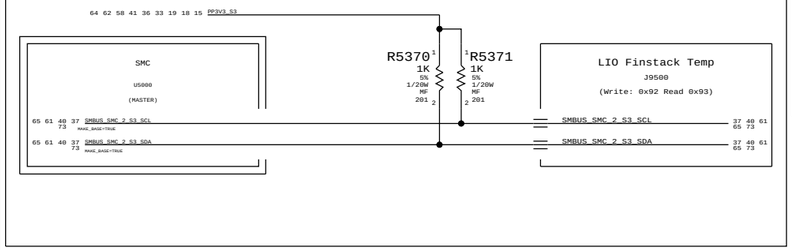
SMC "5" SMBus G3H Connections



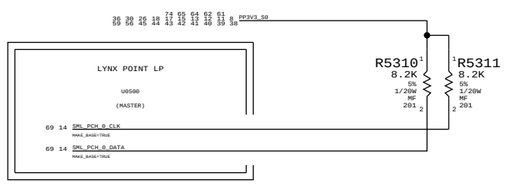
SMC "3" SMBus S0 Connections



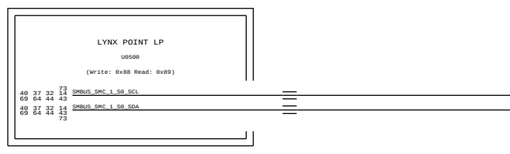
SMC "2" SMBus S3 Connections



LYNX POINT LP S0 "SMLink 0" Connections



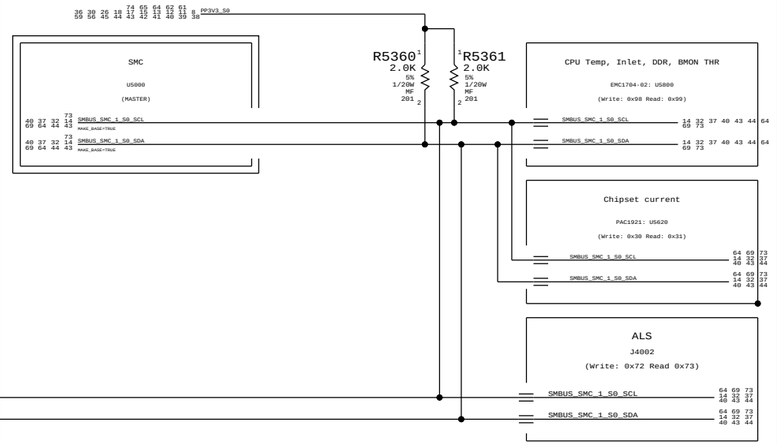
LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to

access PCH

SMC S0 "1" SMBus Connections



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

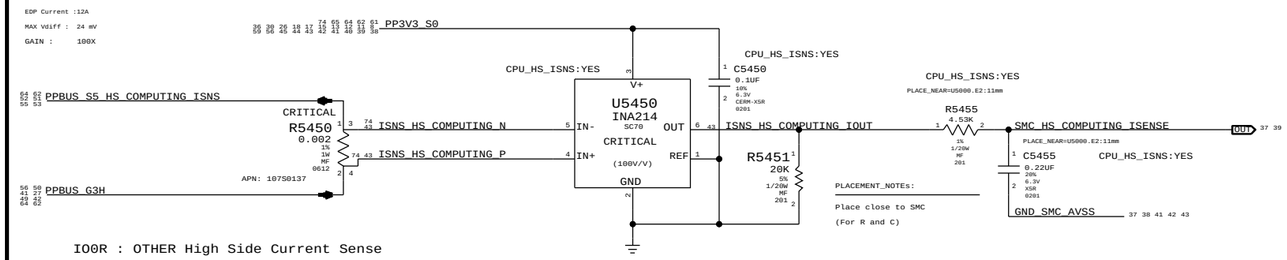
PAGE 53 OF 121

SHEET 40 OF 76

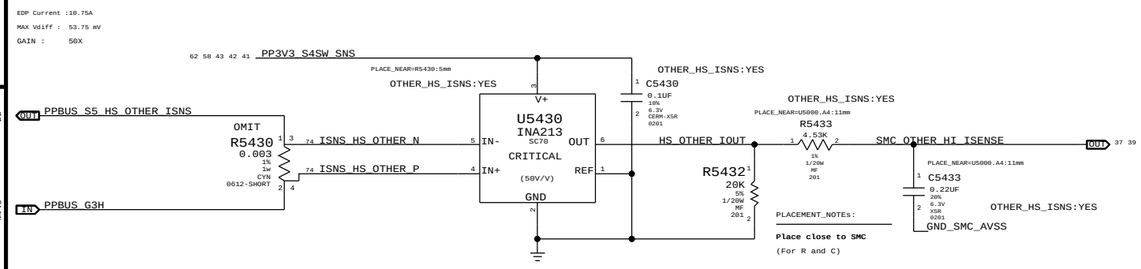
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

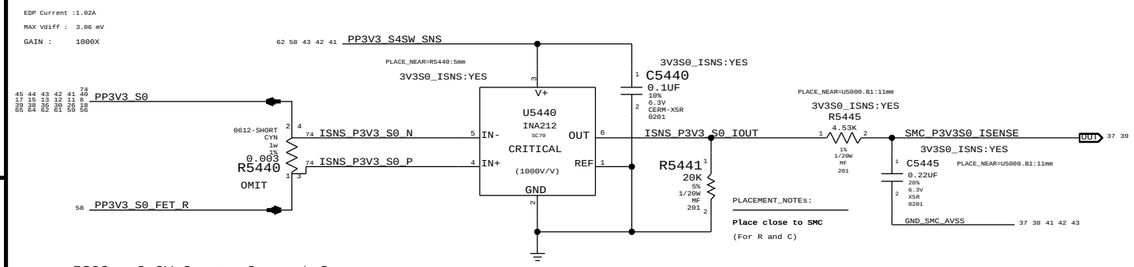
IC0R : COMPUTING High Side Current Sense



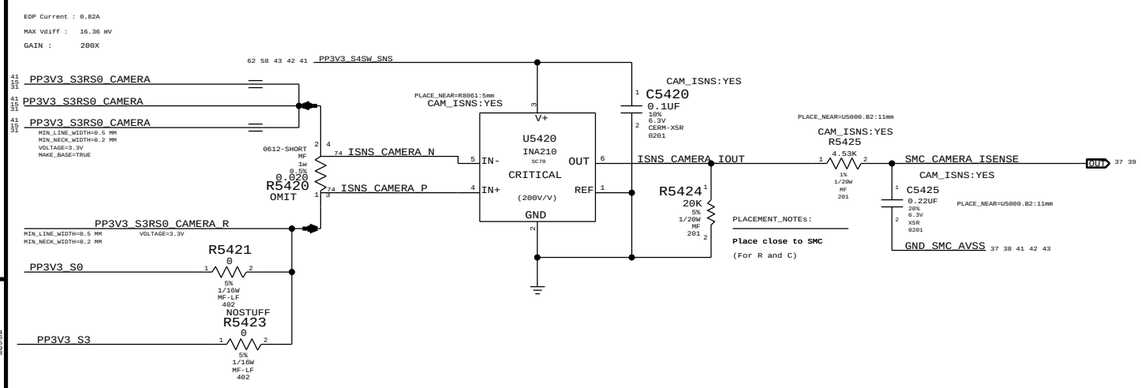
IO0R : OTHER High Side Current Sense



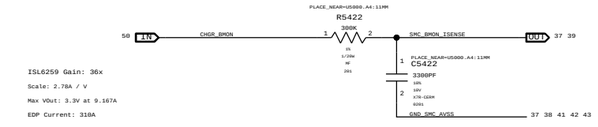
IR0C : 3.3V S0 FET Current Sense



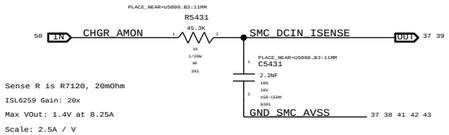
IS2C : 3.3V Camera Current Sense



CHARGER BMON High Side Current Sense

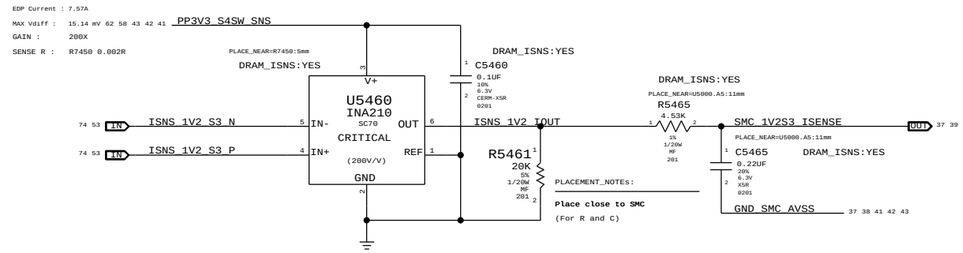


DC-IN (AMON) Current Sense

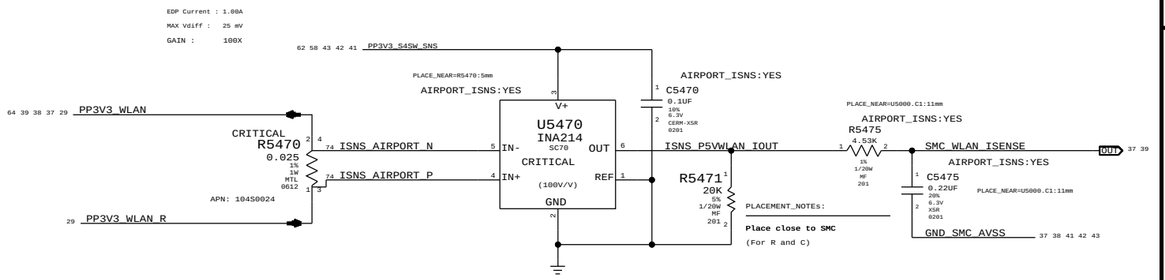


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

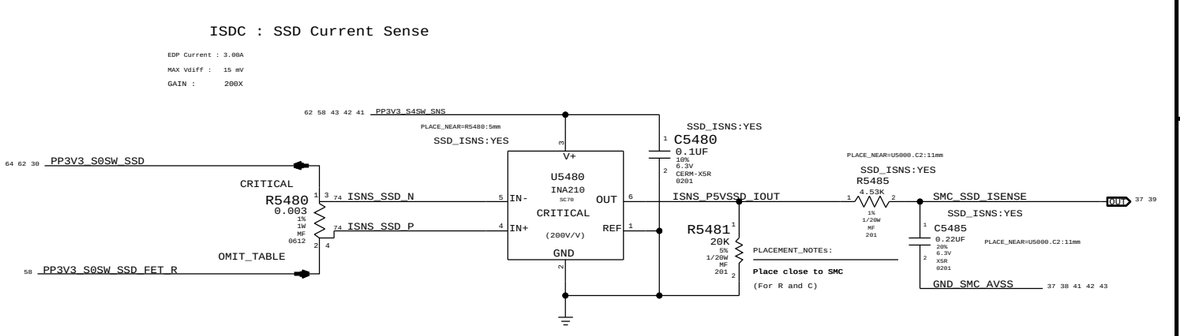
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)



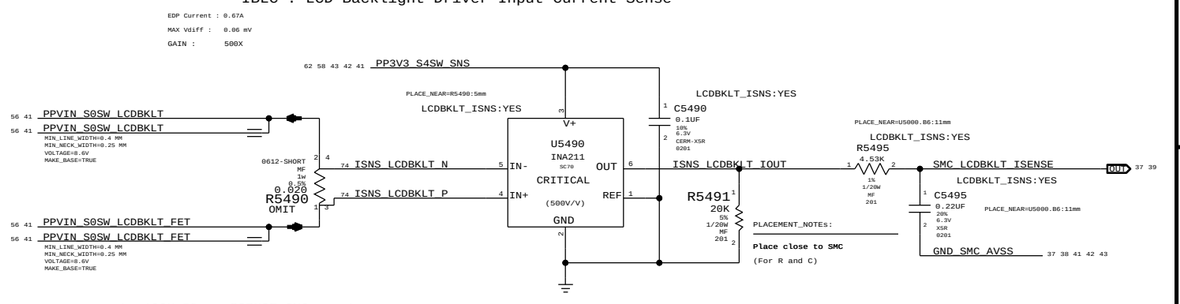
IAPC :AirPort Current Sense



ISDC : SSD Current Sense



IBLC : LCD Backlight Driver Input Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC_MASTER=J41_MLB SYNC_DATE=03/28/2013

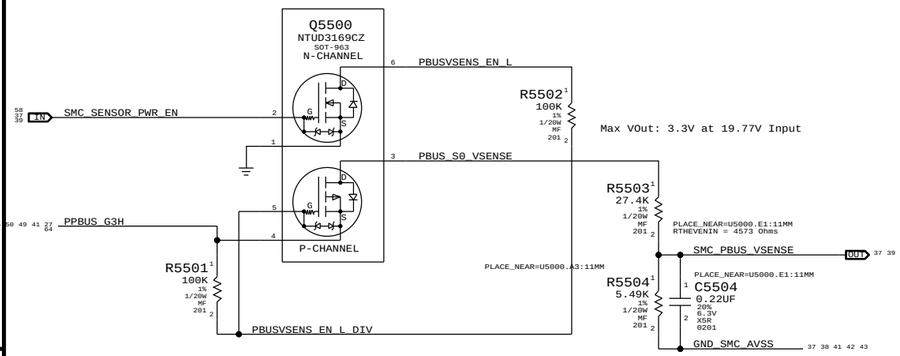
PAGE TITLE: High Side Current Sensing

Apple Inc.

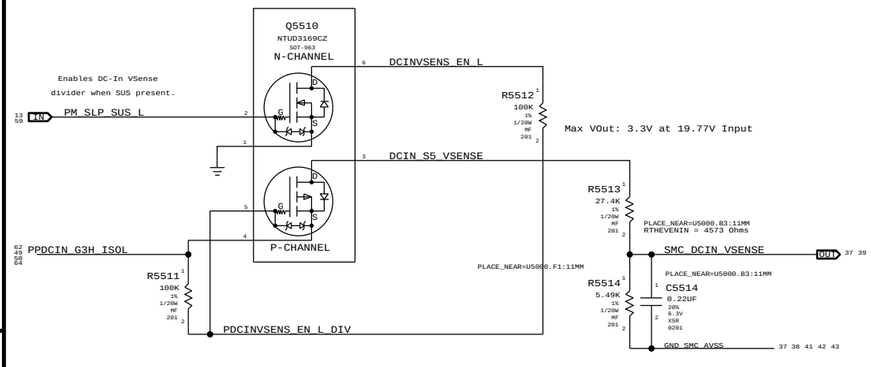
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 54 OF 121
SHEET: 41 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

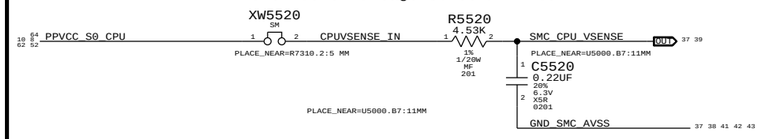
VP0R: PBUS Voltage Sense Enable & Filter



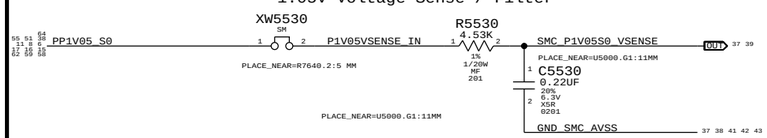
VD0R: DC-In Voltage Sense Enable & Filter



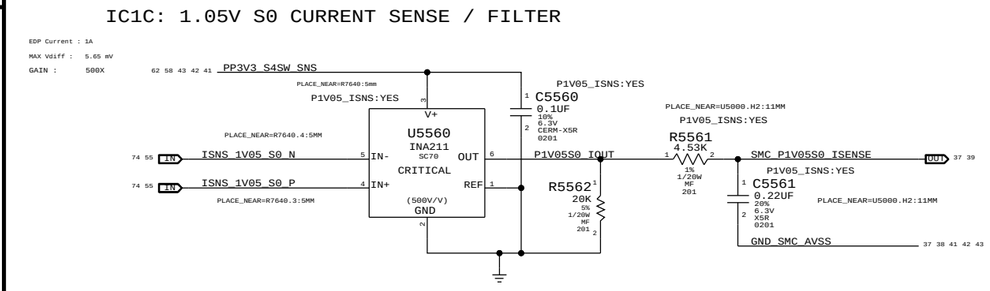
CPU Vcore Voltage Sense / Filter



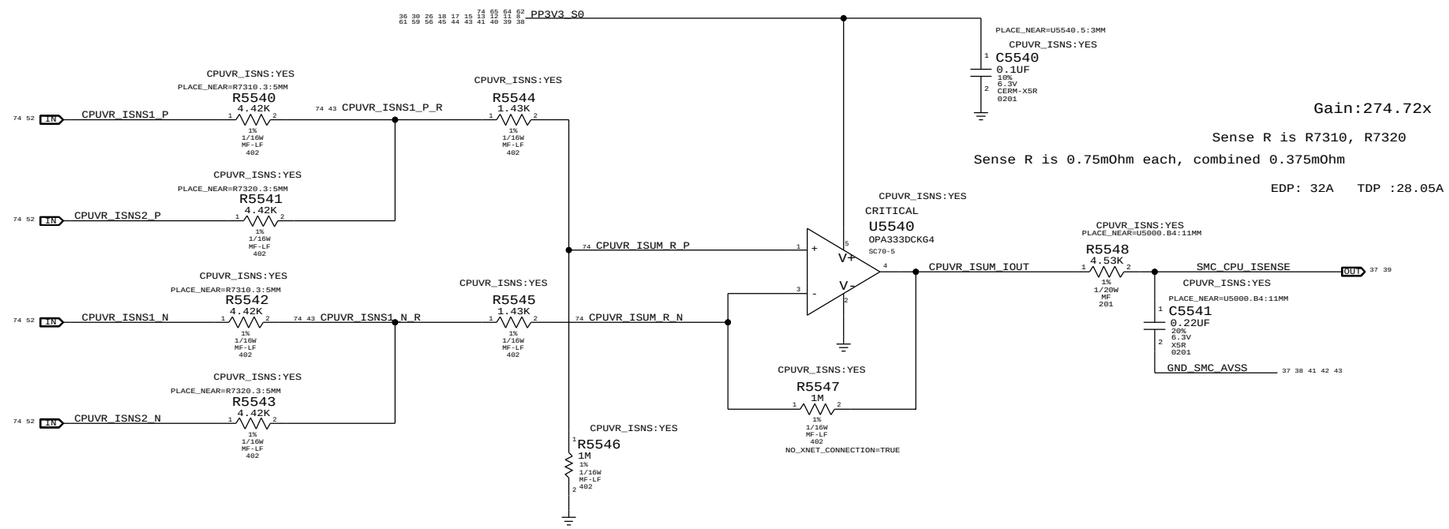
1.05V Voltage Sense / Filter



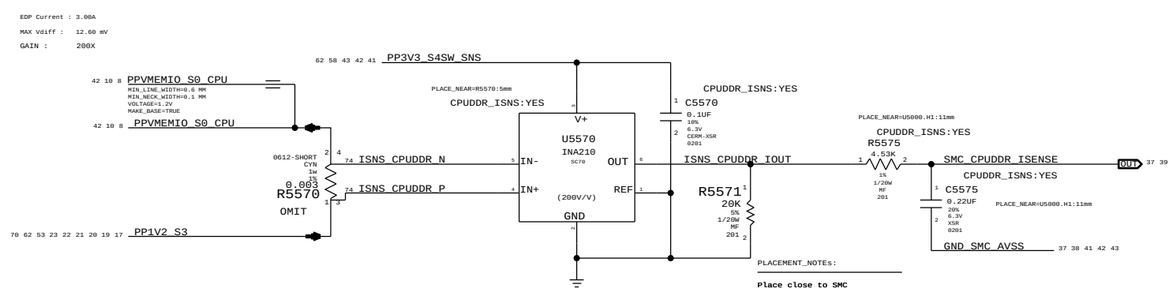
IC1C: 1.05V S0 CURRENT SENSE / FILTER



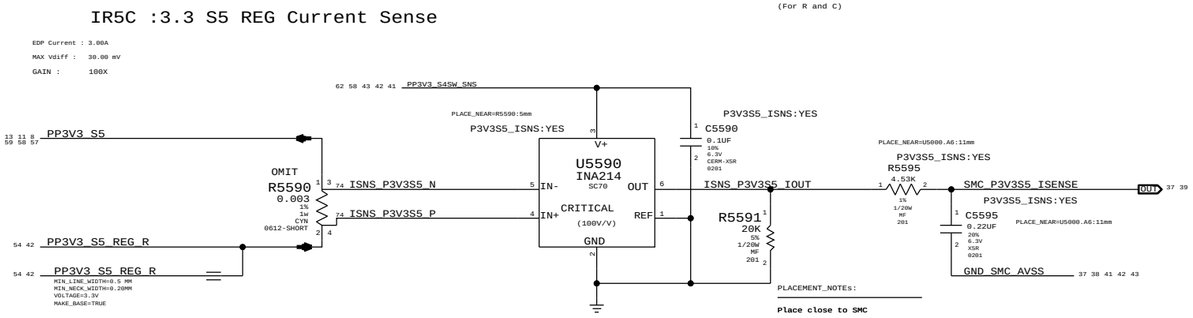
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C :3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

SYNC_MASTER=J41_MLB SYNC_DATE=03/28/2013

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 55 OF 121

SHEET: 42 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

ICS3 : Adjustable Gain CPU VR Current

R5821: ADDR - 0x56/0x57 (r/w)

PP3V3_S4SW_SNS → R5620 100 1% 1/16W MF-LF 402 → PP3V3_SNS_CPUVR_ADJUST_ISNS

C5620 1.0UF 20% 6.3V X5R 0201-1 (BYPASS=U5620.1:5:3MM)

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
VOLTAGE=3.3V

R5621 4.3K 5% 1/20W MF 201 (CPUVRSNS_ADDR_SEL)

U5620 PAC1921-1-AIA DFN

Pin	Name	Net
1	VDD	
6	ADDR_SEL/GAIN_SEL	
2	SENSE+	CPUVR_ISNS1_P_R (74 42 IN)
3	SENSE-	CPUVR_ISNS1_N_R (74 42 IN)
4	OUT	SMC_CPUVR_ADJUST_ISENSE_R
8	READ*/INT	SMC_CPU_DBGPWR_RD_L (IN 37)
10	SM_CLK/INT_SEL	SMBUS_SMC_1_S0_SCL (BI 14 32 37 40 44 64 69 73)
9	SM_DATA/OUT_SEL	SMBUS_SMC_1_S0_SDA (BI 14 32 37 40 44 64 69 73)
7	COMM_SEL	
5	GND	
11	EPAD	

PLACE_NEAR=U5540.1:5MM

PU: SMBus mode

R5625 0 5% 1/20W MF 0201 (PLACE_NEAR=U5000.A7:5MM) → SMC_CPUVR_ADJUST_ISENSE (OUT 37 39)

C5625 0.22UF 20% 6.3V X5R 0201 (NO STUFF, PLACE_NEAR=U5000.A7:5MM)

GND_SMC_AVSS (37 38 41 42 43)

Sense Pins gain stage for U5800 (EMC1704)

PP3V3_S0 (36 38 26 18 17 15 13 12 11 8 / 59 56 45 44 43 42 41 40 39 38 / 74 65 64 62 61) → R5660 0 5% 1/20W MF 0201

C5660 0.1UF 10% 6.3V CERM-XSR 0201 (PLACE_NEAR=U5660.3:5MM)

U5660 INA211 SC70 CRITICAL (500V/V) (PLACE_NEAR=R7150:5MM)

Pin	Name	Net
5	IN-	CKPLUS_WAIVE=NdifPr_badTerm; ISNS_HS_COMPUTING_P (74 43 41 IN)
4	IN+	CKPLUS_WAIVE=NdifPr_badTerm; ISNS_HS_COMPUTING_N (74 43 41 IN)
6	OUT	ISNS_HS_GAIN_OUT
1	REF	GND
2	GND	
3	V+	

R5663 20K 5% 1/20W MF 201

R5665 0 5% 1/20W MF 0201 (ISNS_HS_GAIN_OUT → ISNS_HS_GAIN_OUT_R, NO STUFF)

C5665 0.22UF 20% 6.3V X5R 0201

R5666 0 5% 1/20W MF 0201 (ISNS_HS_GAIN_P_R → ISNS_HS_GAIN_P → OUT 44 74)

R5662 1K 1% 1/20W MF 201 (74 41 43 IN ISNS_HS_COMPUTING_P)

R5667 0 5% 1/20W MF 0201 (NO STUFF)

R5668 0 5% 1/20W MF 0201 (ISNS_HS_GAIN_N_R → ISNS_HS_GAIN_N → OUT 44 74)

R5661 27K 1% 1/20W MF 201 (74 41 43 IN ISNS_HS_COMPUTING_N)

R5669 0 5% 1/20W MF 0201 (NO STUFF)

GAIN: 500X

In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

ILDC :LCD Panel Current Sense / Filter

PP3V3_S4SW_SNS (62 58 43 42 41) → C5670 0.1UF 10% 6.3V CERM-X5R 0201 (PANEL_ISNS:YES, PLACE_NEAR=R5470:5MM)

PP3V3_S0SW_LCD (60 43) (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)

R5670 0.020 0.5% 1W MF 0612-SHORT (OMIT)

U5670 INA210 SC70 CRITICAL (200V/V)

Pin	Name	Net
5	IN-	ISNS_PANEL_N (74 IN)
4	IN+	ISNS_PANEL_P (74 IN)
6	OUT	ISNS_PANEL_IOUT
1	REF	GND
2	GND	
3	V+	

R5671 20K 5% 1/20W MF 201

Gain: 200x
Scale: 0.25A / V
MAX VOUT: 3V AT 0.825A
PLACEMENT_NOTES:
Place close to SMC
(For R and C)

R5675 4.53K 1% 1/20W MF 201 (PANEL_ISNS:YES, PLACE_NEAR=U5000.C1:11mm) → SMC_PANEL_ISENSE (OUT 37 39)

C5675 0.22UF 20% 6.3V X5R 0201 (PANEL_ISNS:YES, PLACE_NEAR=U5000.C1:11mm)

GND_SMC_AVSS (37 38 41 42 43)

EDP Current: 0.750 A
Max Vdiff: 15 mV

VR IMON Current Sense Filter

CPUVR_IMON (51 IN) → R5641 0 5% 1/20W MF 0201 (PLACE_NEAR=U5000.B8:5MM) → SMC_CPU_IMON_ISENSE (OUT 37 39)

C5641 2.2NF 10% 16V X5R-CERM 0201 (NO STUFF, PLACE_NEAR=U5000.B8:5MM)

GND_SMC_AVSS (37 38 41 42 43)

Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

Discrete High side Current threshold

PP3V3_S0 (74 65 64 62 61 / 59 56 45 44 43 42 41 40 39 38 / 36 38 26 18 17 15 13 12 11 8) → C5613 0.1UF 10% 6.3V CERM-X5R 0201 (BYPASS=U5601:3MM)

R5614 294K 1% 1/16W MF-LF 402 (HS_COMP_VREF)

R5615 49.9K 1% 1/16W MF-LF 402

R5616 10.2K 1% 1/16W MF-LF 402 (HS_COMP_FB)

U5611 MCP6541T SC70-5 → HS_COMP_OUT

R5619 255K 1% 1/16W MF-LF 402

C5611 0.22UF 20% 6.3V X5R 0201 (NO STUFF)

U5612 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 (SMC_HS_COMP_ALERT_L → OUT 39)

HS_IOUT_R → C5610 0.1UF 10% 25V X5R 402 (NOSTUFF)

R5610 0 5% 1/20W MF 0201

R5617 0 5% 1/20W MF 0201 (NOSTUFF)

HS_IOUT_D → D5617 RB521ES-30 (NOSTUFF)

ISNS_HS_COMPUTING_IOUT (41 IN)

Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

BMON : Discrete BMON Current Sense / Filter

PP3V3_S0 (36 38 26 18 17 15 13 12 11 8 / 59 56 45 44 43 42 41 40 39 38 / 74 65 64 62 61)

C5603 0.1UF 10% 6.3V CERM-X5R 0201 (BYPASS=U5601:3MM)

R5604 100K 1% 1/16W MF-LF 402

R5605 100K 1% 1/16W MF-LF 402 (BMON_COMP_VREF)

R5606 10.2K 1% 1/16W MF-LF 402

U5601 MCP6541T SC70-5 → BMON_COMP_OUT

C5601 0.22UF 20% 6.3V X5R 0201 (NO STUFF)

R5609 200K 1% 1/16W MF-LF 402 (BMON_COMP_FB)

U5602 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 (SMC_BMON_COMP_ALERT_L → OUT 39)

BMON_IOUT_R → C5600 0.1UF 10% 25V X5R 402 (NOSTUFF)

R5600 0 5% 1/20W MF 0201

R5607 0 5% 1/20W MF 0201 (NOSTUFF)

BMON_IOUT_D → D5607 RB521ES-30 (NOSTUFF)

C5606 0.1UF 10% 6.3V CERM-X5R 0201 (BYPASS=U5600:3MM)

CHGR_CSO_R_P/N are swapped on purpose to measure power into the system

U5600 INA213 SC70 CRITICAL (50V/V)

Pin	Name	Net
5	IN-	CKPLUS_WAIVE=NdifPr_badTerm; CHGR_CSO_R_P (73 50 IN)
4	IN+	CKPLUS_WAIVE=NdifPr_badTerm; CHGR_CSO_R_N (73 50 IN)
6	OUT	BMON_IOUT
1	REF	GND
2	GND	
3	V+	

R5601 20K 5% 1/20W MF 201

R5608 4.53K 1% 1/20W MF 201 (PLACE_NEAR=U5000.A3:5MM) → SMC_BMON_DISCRETE_ISENSE (OUT 37 39)

C5602 0.22UF 20% 6.3V X5R 0201 (PLACE_NEAR=U5000.A3:5MM)

GND_SMC_AVSS (43 37 38 39 42)

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=J41_MLB SYNC_DATE=03/28/2013

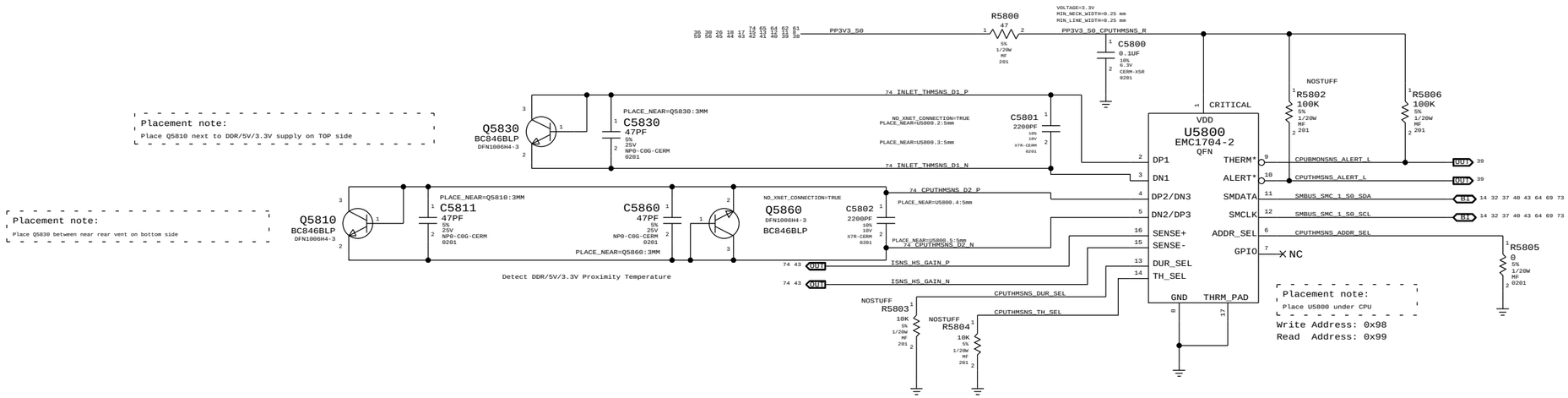
PAGE TITLE: Debug Sensors 1

Apple Inc.

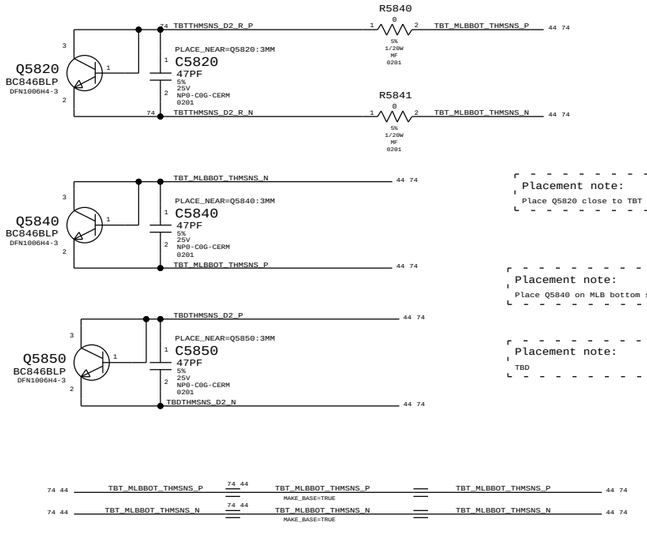
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 56 OF 121
SHEET: 43 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

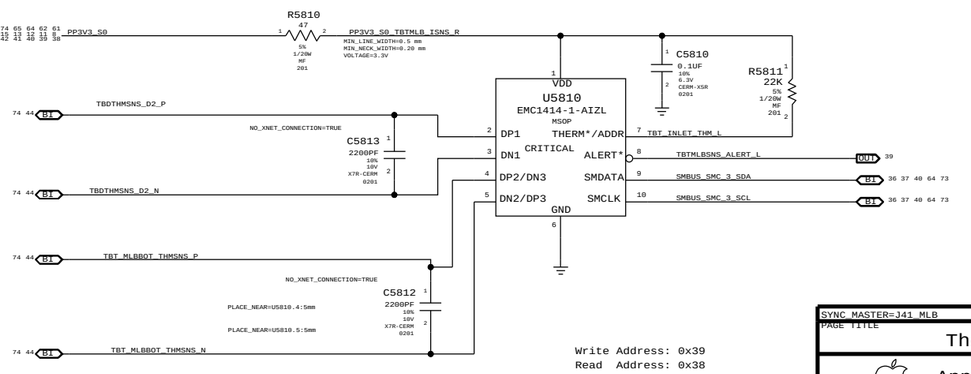
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors



TBT, MLBBOT and TBD Temp Sensor



TBT_MLBBOT_THMSNS_P — MAKE_BASE=TRUE — TBT_MLBBOT_THMSNS_P

TBT_MLBBOT_THMSNS_N — MAKE_BASE=TRUE — TBT_MLBBOT_THMSNS_N

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 58 OF 121

SHEET 44 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING:

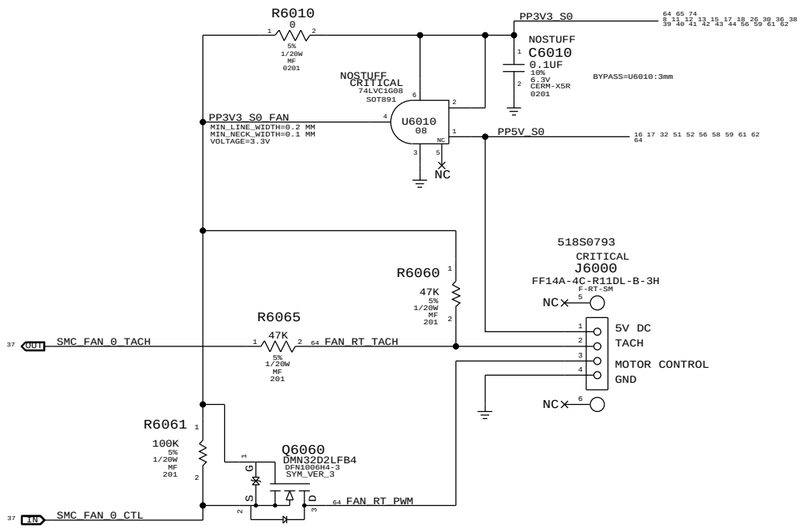
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

FAN CONNECTOR



SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 60 OF 121

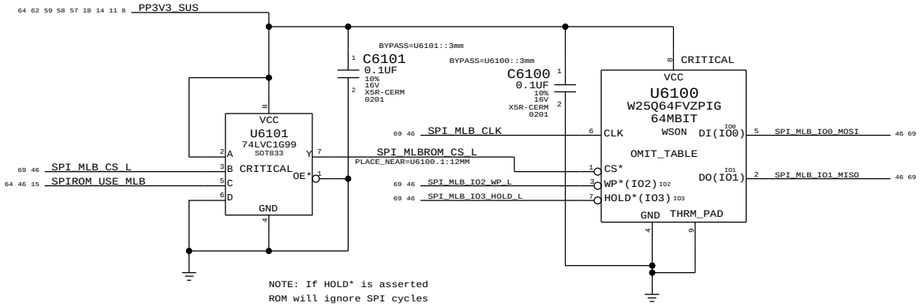
SHEET 45 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SPI ROM

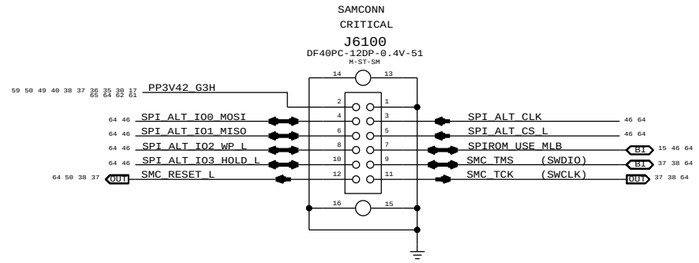
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



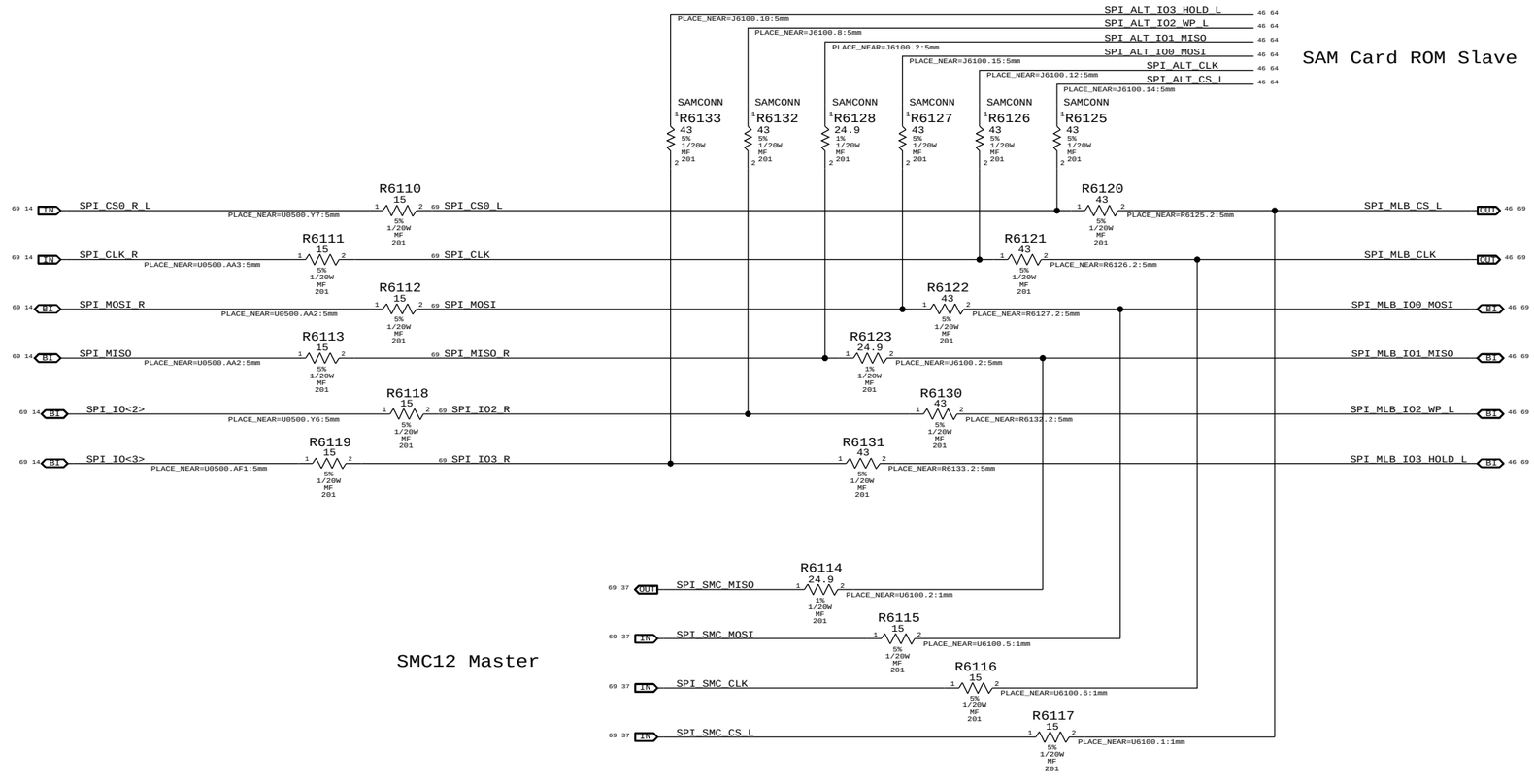
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination



BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 61 OF 121
SHEET: 46 OF 76

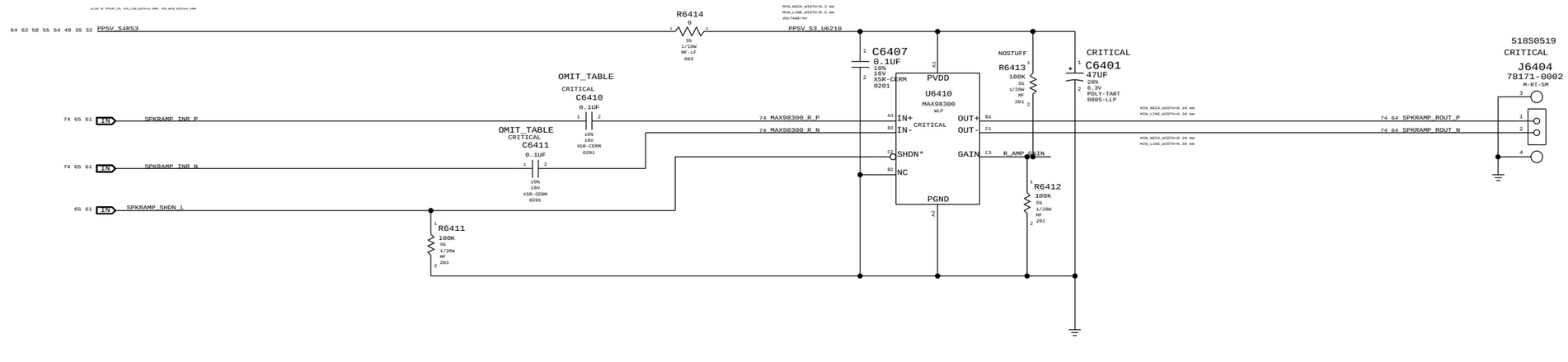
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0460	2	CAP,CER,X5R,0.1UF,10%,16V,0201,MURATA	C6410,C6411	CRITICAL	

SYNC_MASTER=J41_MLB SYNC_DATE=04/26/2013

PAGE TITLE

Audio: Speaker Amp

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 64 OF 121

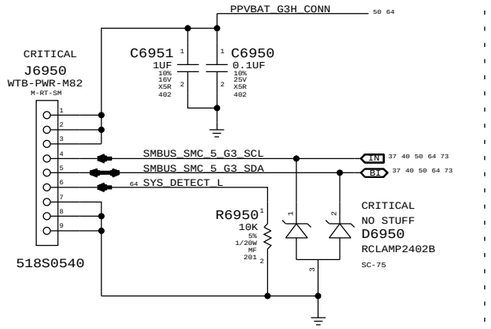
SHEET 47 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

13" SPECIFIC

Battery Connector



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Battery Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

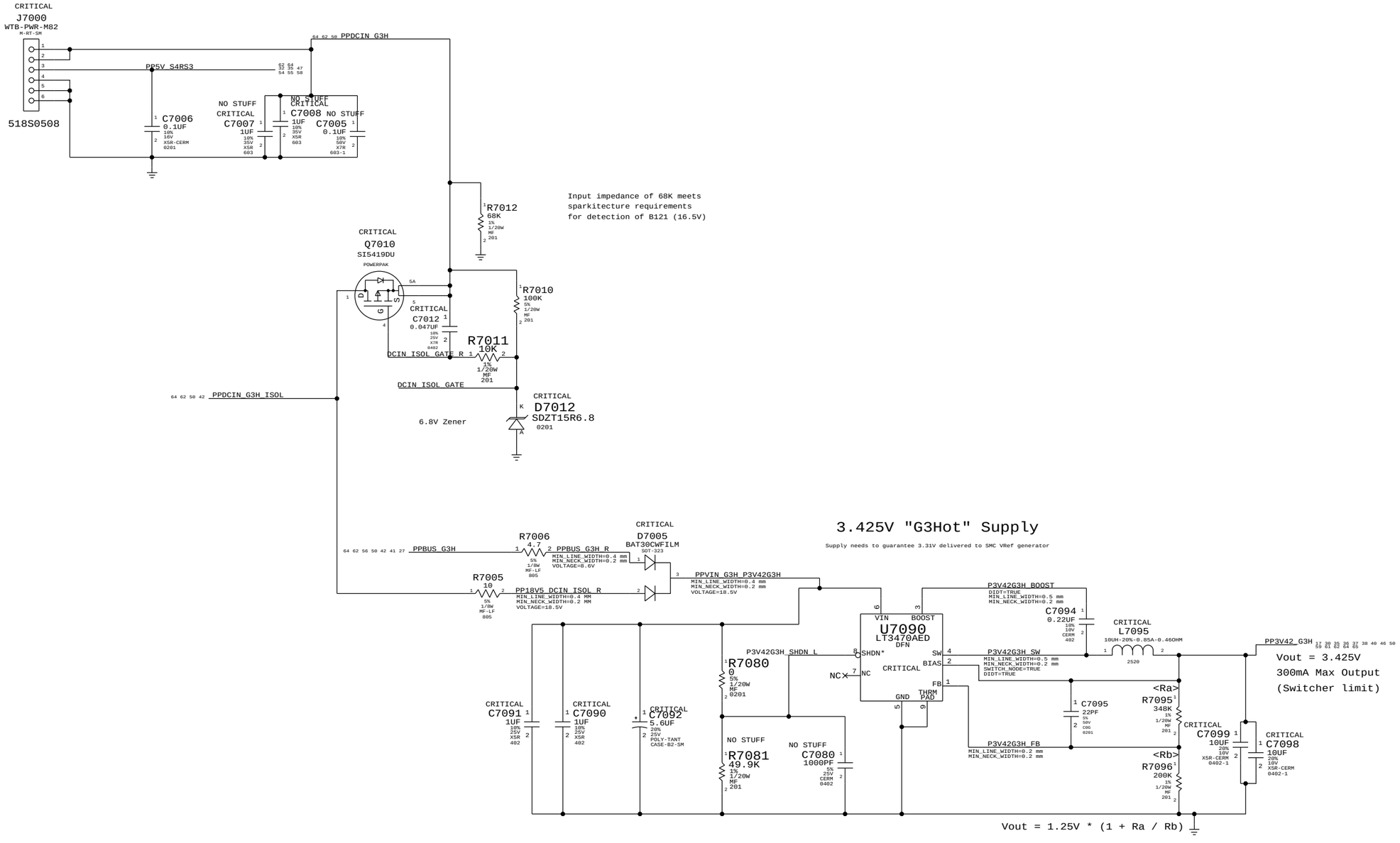
PAGE 69 OF 121

SHEET 48 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MLB to LIO Power Cable Connector



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE: DC-In & G3H Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 70 OF 121

SHEET: 49 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Reverse-Current Protection

Need to stuff R7192 if either PP5V5_DCIN:YES or PP5V5_VDDP are used!

Inrush Limiter

FROM ADAPTER

64 62 49 _PPDCIN_G3H

R7185 470K

C7185 0.1UF

CRITICAL Q7180 IRF9395TRPBF DIRECTFET-MC

CHGR_AGATE_DIV

R7186 332K

64 62 49 42 _PPDCIN_G3H_ISOL

CRITICAL D7105 BAT30CWFILM SOT-323

50 PPCHGR_DCIN_D_R

PP5V5_DCIN:NO

R7105 20 5% 1/10W MF-LF 603

(CHGR_DCIN)

PPDCIN_G3H_INRUSH

R7180 100K

C7184 4.7UF

CHGR_SGATE_DIV

R7181 62K

(CHGR_AGATE)

(CHGR_SGATE)

NO STUFF R7192 0

PPCHGR_DCIN_D_R

CHGR_DCIN

NO STUFF C7190 4.7UF

5.5v "G3Hot" Supply
For Erp Lot6 spec

U7190 LT3470A DFN

VIN BOOST SHDN* SW BIAS NC FB THRM GND PAD

CRITICAL

PP5V1_BOOST

PP5V1_SW

PP5V1_FB

NO STUFF C7194 0.22UF

CRITICAL L7195 10UH-20%-0.85A-0.46OHM 2520

NO STUFF C7195 22PF

NO STUFF <Ra> R7195 681K

<Rb> R7196 200K

Vout = 1.25V * (1 + Ra / Rb)

NO STUFF CRITICAL C7198 10UF

NO STUFF CRITICAL C7199 10UF

PP5V5_DCIN:YES

R7190 0

CHGR_DCIN 50

PP5V5_VDDP

R7191 0

PP5V1_CHGR_VDDP 50

PP5V5_CHGR_VDDP

Vout = 5.50V
200MA MAX OUTPUT
(Switcher limit)

ACIN pin threshold is 3.2V, +/- 50mV

DIVIDER SETS ACIN THRESHOLD AT 13.55V

30mA max load

PP5V1_CHGR_VDD

R7101 4.7

50 PP5V1_CHGR_VDDP

C7101 1UF

59 49 46 40 38 37 36 35 30 17 65 64 62 61 PP3V42_G3H

R7110 130K 1%

NO STUFF R7102 100K

R7100 0

64 46 38 37 SMC_RESET_L

CHGR_RST_L

SMBUS_SMC_5_G3_SCL

SMBUS_SMC_5_G3_SDA

CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

CRITICAL U7100 ISL6259 TQFN

VHST	12		
SMB_RST_N	13		
SCL	11		
SDA	10		
VFRQ	4		
CELL	6		
ACIN	3		
ICOMP	5		
VCOMP	7		
VNEG	8		
CSOP	18		
CSON	17		
DCIN	2	28	CHGR_DCIN
SGATE	26		CHGR_SGATE
AGATE	1		CHGR_AGATE
CSIP	28	73	CHGR_CSI_P
CSIN	27	73	CHGR_CSI_N
BOOT	25		CHGR_BOOT
UGATE	24		CHGR_UGATE
PHASE	23		CHGR_PHASE
LGATE	21		CHGR_LGATE
BGATE	16		CHGR_BGATE
AMON	9		CHGR_AMON
BMON	15		CHGR_BMON
ACOK	14		SMC_BC_ACOK
(AGND) THRM_PAD	29		
(PGND)	22		

20V/V 36V/V (08)

R7111 46.4K

R7113 100

R7115 255K

R7142 1K

R7116 10K

CHGR_VCOMP_R

CHGR_ICOMP_R

CHGR_VNEG_R

C7115 470PF

C7116 470PF

C7150 0.47UF

C7102 1UF

XW7100 SM

(GND)

R7121 10

R7122 10

73 CHGR_CSI_R_P

73 CHGR_CSI_R_N

C7120 0.047UF

C7122 0.1UF

C7121 0.1UF

CRITICAL R7120 0.020 0.5% 1W MF-LF 0612

PPDCIN_G3H_CHGR

CRITICAL C7130 33UF-0.006OHM POLY-TANT CASE-D3L

CRITICAL C7131 33UF-0.006OHM POLY-TANT CASE-D3L

C7135 1UF

C7136 1UF

C7137 0.001UF

BYPASS=Q7130:1.5mm

Max Current = 8A

f = 400 kHz

CRITICAL Q7130 NTMFD4902NF DFN

C7125 0.22UF

CRITICAL L7130 4.7UH-17A PIMC104T4R7MN-SM

TO SYSTEM

CRITICAL F7140 8AMP-24V 1206

PPBUS_G3H 27 41 42 49 56 62 64

PPVBAT_G3H_CHGR_REG

C7140 620UF-0.023OHM TANT-POLY CASE-B2S

C7141 620UF-0.023OHM TANT-POLY CASE-B2S

C7143 620UF-0.023OHM TANT-POLY CASE-B2S

C7145 1000PF

BYPASS=L7130:Q7130:1.5mm

R7150 0.01

PPVBAT_G3H_CHGR_R

CRITICAL Q7155 SI7137DP SO-8

TO/FROM BATTERY

PPVBAT_G3H_CONN 48 64

R7151 2.2 201

R7152 0

73 43 CHGR_CSO_R_P

73 43 CHGR_CSO_R_N

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

C7142 0.1UF

C7111 0.01UF

C7100 1UF

C7105 0.22UF

C7126 1000PF

GND_CHGR_AGND

C7117 10UF

C7114 1UF

C7113 0.1UF

C7112 0.01UF

* R7151 HAS 2.20HM TO COMPENSATE UNBALANCED VOLTAGE
DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

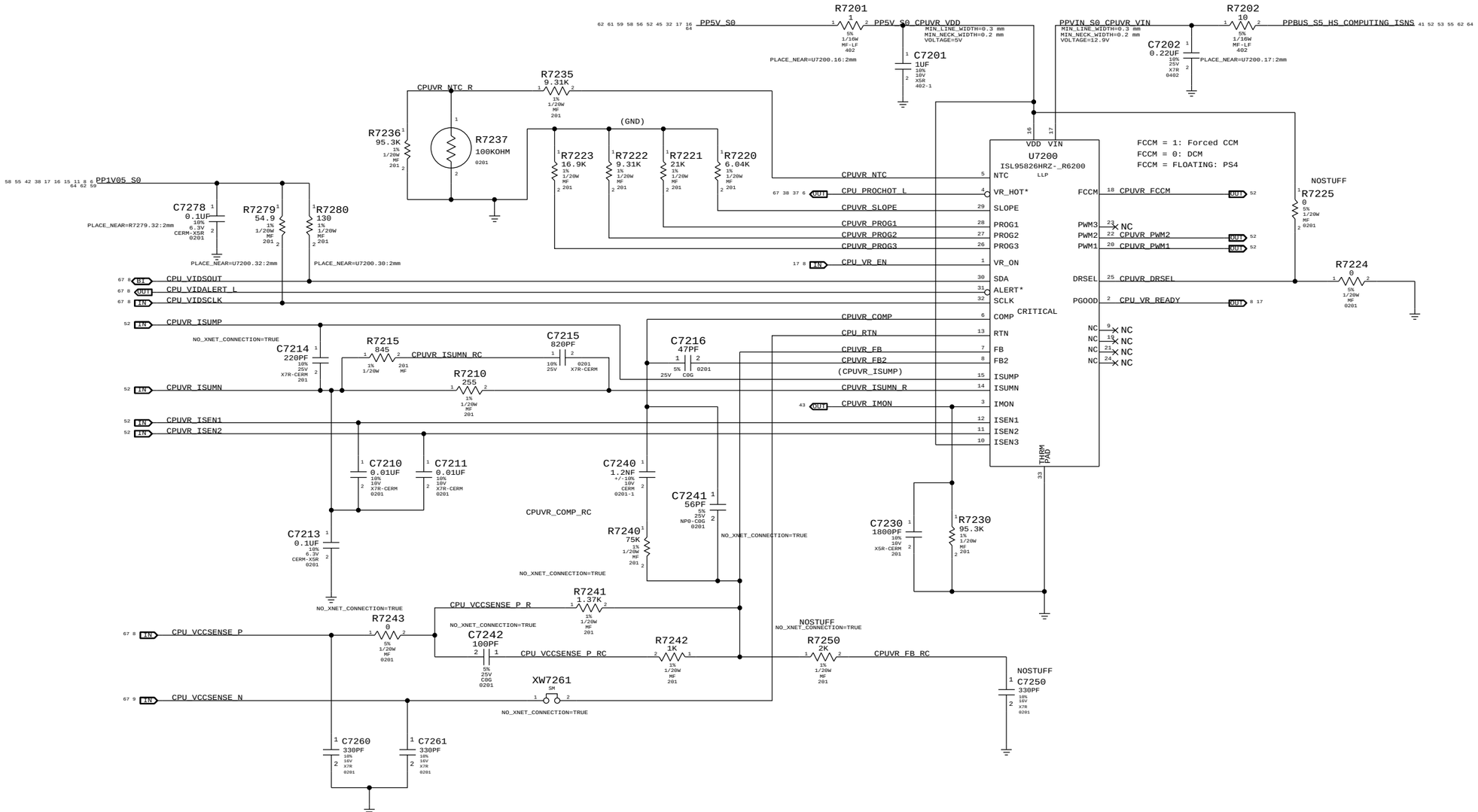
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 71 OF 121

SHEET 50 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



8	7	6	5	4	3	2	1

SYNC_MASTER=J43_MLB SYNC_DATE=10/09/2012

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

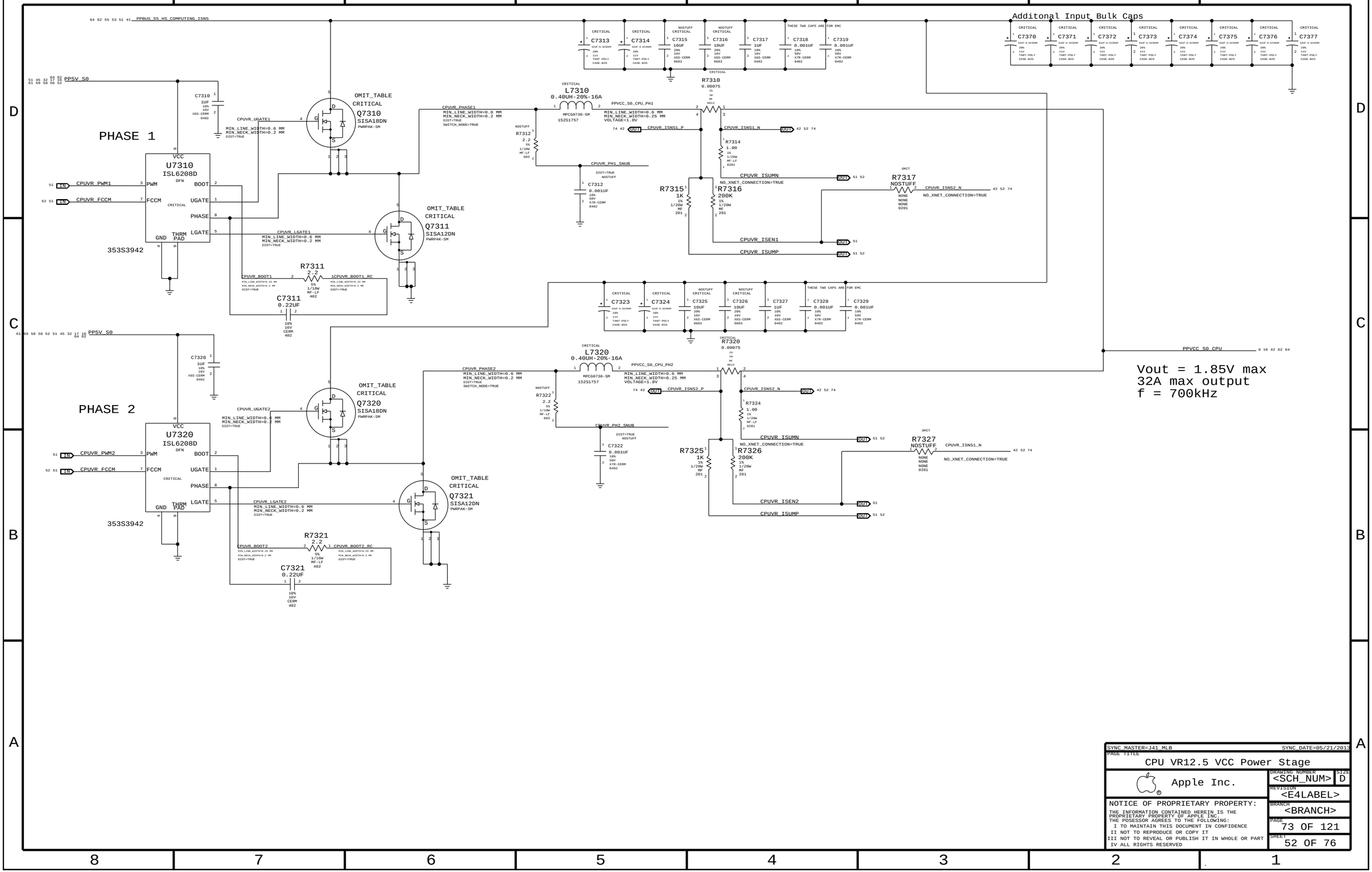
BRANCH <BRANCH>

PAGE 72 OF 121

SHEET 51 OF 76

NOTICE OF PROPRIETARY PROPERTY:

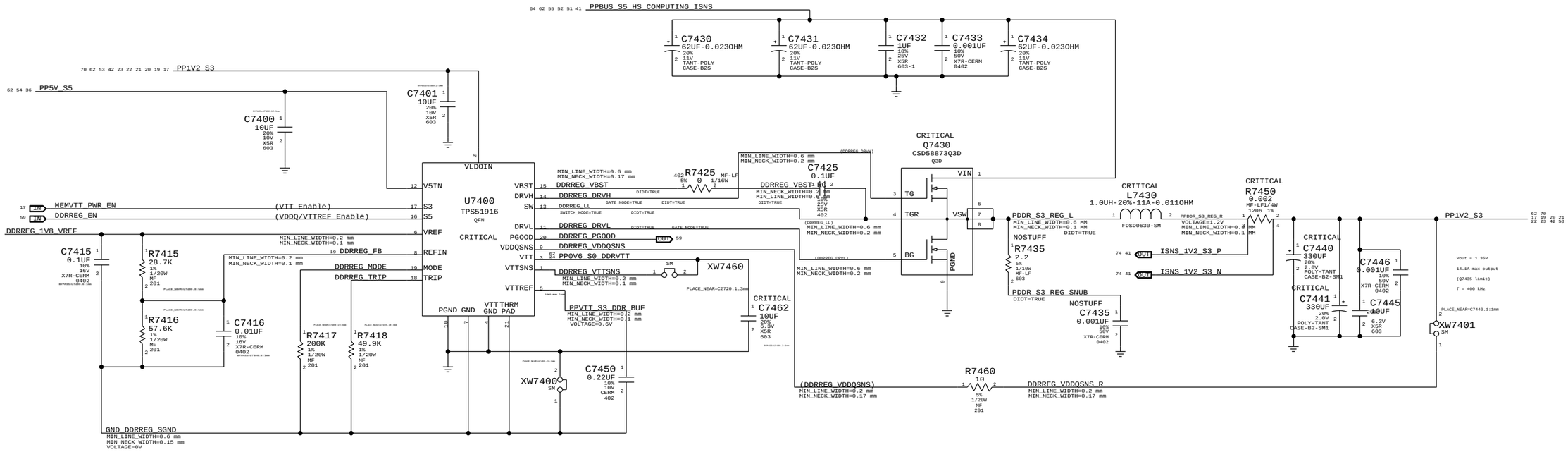
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J41_MLB	SYNC_DATE=05/21/2013
PAGE TITLE	CPU VR12.5 VCC Power Stage
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 73 OF 121
	SHEET 52 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J41_MLB	SYNC_DATE=05/21/2013
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 74 OF 121
	SHEET 53 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SKIPSEL Strap	
VREF2	Auto Skip (Higher Efficiency)
VREG3	OOA Auto Skip (Lower Efficiency)

F=400KHZ

Vout = 5.0V

7.2A MAX OUTPUT

F=400KHZ

Vout = 3.3V

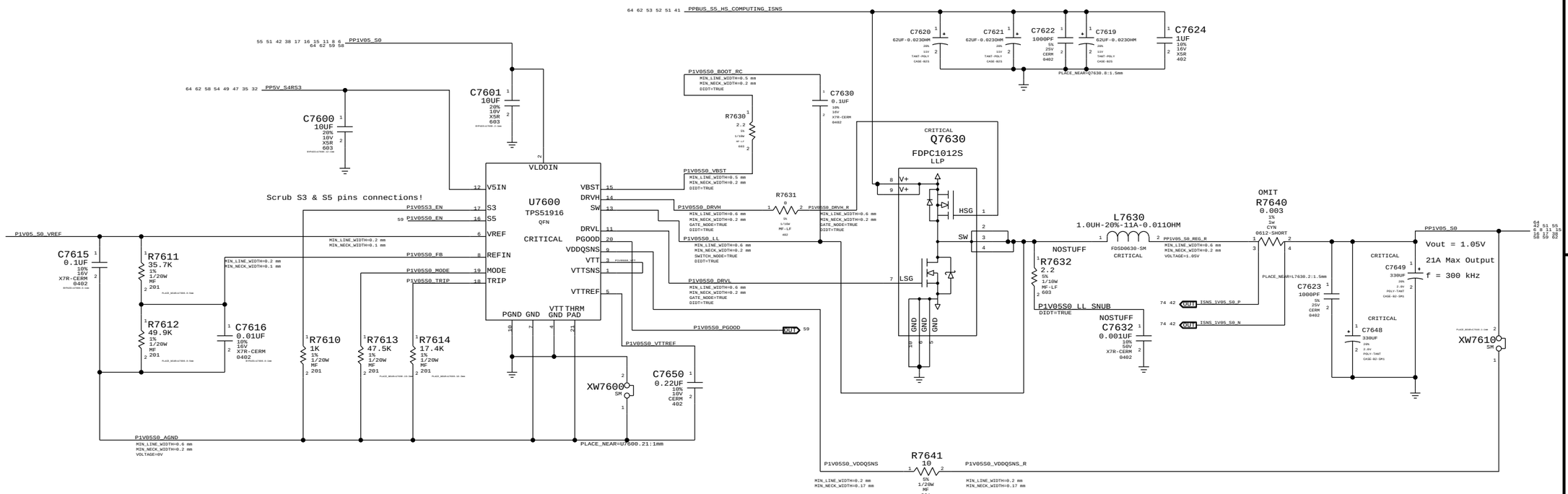
6.5A MAX OUTPUT

SYNC_MASTER=J41_MLB	SYNC_DATE=09/17/2012
PAGE TITLE	5V S4RS3 / 3.3V S5 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 75 OF 121
	SHEET 54 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.05V S0 Regulator



SYNC_MASTER=J41_MLB SYNC_DATE=05/21/2013

PAGE TITLE

1.05V S0 Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 76 OF 121

SHEET 55 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PPBUS S0 LCDBklt FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

CRITICAL
Q7706
FDC638APZ_SBMS001
SSOT6-HF

F7700
3AMP-32V-467
603-HF
PLACE_SIDE=BOTTOM
PPBUS_G3H
PPVIN_S0SW_LCDBKLTFET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

R7788 301K 1% 1/20W MF 201
C7782 0.1UF 10% 16V X7R-CERM 0402
LCDBKLT_EN_DIV_L
R7789 147K 1% 1/20W MF 201
LCDBKLT_EN_L

Q7707
DMN5L06VK-7
SOT563
VER 3
EDP_BKLT_EN
LCDBKLT_DISABLE

Q7707
DMN5L06VK-7
SOT563
VER 3
BKLT_PLT_RST_L

PPVIN_S0SW_LCDBKLT_FET
THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

CRITICAL
L7701
15UH-2.8A
PIMB053T-SM
PPVIN_S0SW_LCDBKLT
LCDBKLT_BOOST
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.150 MM
VOLTAGE=50V
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL C7712 10UF 10% 25V X5R 805
C7713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L7701.1:3mm

CRITICAL
D7701
SOD-123
RB160M-60G
PLACE_NEAR=L7701.2:3mm

C7796 220PF 10% 50V X7R-CERM 0402
CRITICAL C7797 10UF 10% 50V X5R 1210-1
CRITICAL C7799 10UF 10% 50V X5R 1210-1
PPHV_S0SW_LCDBKLT
PLACE_NEAR=U7701.A5:3mm
PLACE_NEAR=D7701.2:5mm
PLACE_NEAR=D7701.2:3mm

XW7720
SM
PPVOUT_SW_LCDBKLT_FB
VOLTAGE=50V
MIN_LINE_WIDTH=0.1 MM
MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=C7797.1:5mm

PP5V_S0
C7710 1UF 10% 25V X5R 603-1
BYPASS=U7701.D1:5mm
C7714 0.01UF 10% 10V X5R-CERM 0201
BYPASS=U7701.D1:3mm

PP3V3_S0
C7711 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U7701.C4:4mm

(GND_BKL_SGND)

U7701
25-BUMP-MICRO
LP8550
VDDIO VLDO VIN
VSYNC FILTER ISET FSET SCLK SDA PWM EN FAULT
SW_0 SW_1 FB
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6
BKL_ISEN1 BKL_ISEN2 BKL_ISEN3 BKL_ISEN4 BKL_ISEN5 BKL_ISEN6
GND_S GND_L GND_SW GND_SW

R7741 10K 5% 1/20W MF 201
R7753 0 5% 1/20W MF 0201
R7757 0 5% 1/20W MF 0201
SMBUS_PCH_CLK
SMBUS_PCH_DATA
Addr: 0x58(Wr)/0x59(Rd)
R7731 200K 1% 1/20W MF 201
R7715 100K 1% 1/20W MF 201
PPVIN_S0SW_LCDBKLT
R7704 33 5% 1/20W MF 201
EDP_BKLT_PWM
C7704 33PF 5% 25V NP0-C0G 0201

TP7701 TP-P6
PLACE_SIDE=BOTTOM
I_LED=17.1mA
Fpwm=9.62kHz
see spec for others
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

R7755 10K 5% 1/20W MF 201
R7714 21.5K 1% 1/20W MF 201
R7716 90.9K 1% 1/20W MF 201
GND_BKL_SGND
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
XW7710 SM

PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R771B,R7719		BKLT:ENG
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

R7717 0 BKLT:PROD LED_RETURN_1
R7718 0 BKLT:PROD LED_RETURN_2
R7719 0 BKLT:PROD LED_RETURN_3
R7720 0 BKLT:PROD LED_RETURN_4
R7721 0 BKLT:PROD LED_RETURN_5
R7722 0 BKLT:PROD LED_RETURN_6
5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm

Keyboard Backlight Driver & Detection

CRITICAL
L7750
10UH-0.58A-0.35OHM
1098AS-SM
PP5V_S0
BYPASS=U7750.1:2:2 MM
KBDLED_SW
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.225 MM
SWITCH_NODE=TRUE
DIDT=TRUE

C7750 1UF 10% 10V X5R 402-1
U7750
SPN0350076
MLF
CRITICAL
VIN EN FB NC GND THRM PAD SW OUT
SMC_SYS_KBDLED
KBDLED_FB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=40V
KBDLED_ANODE
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=40V
R7700 4.7 5% 1/16W MF-LF 402
C7755 0.22UF 10% 50V XSR-CERM 0603-1
C7756 0.22UF 10% 50V XSR-CERM 0603-1

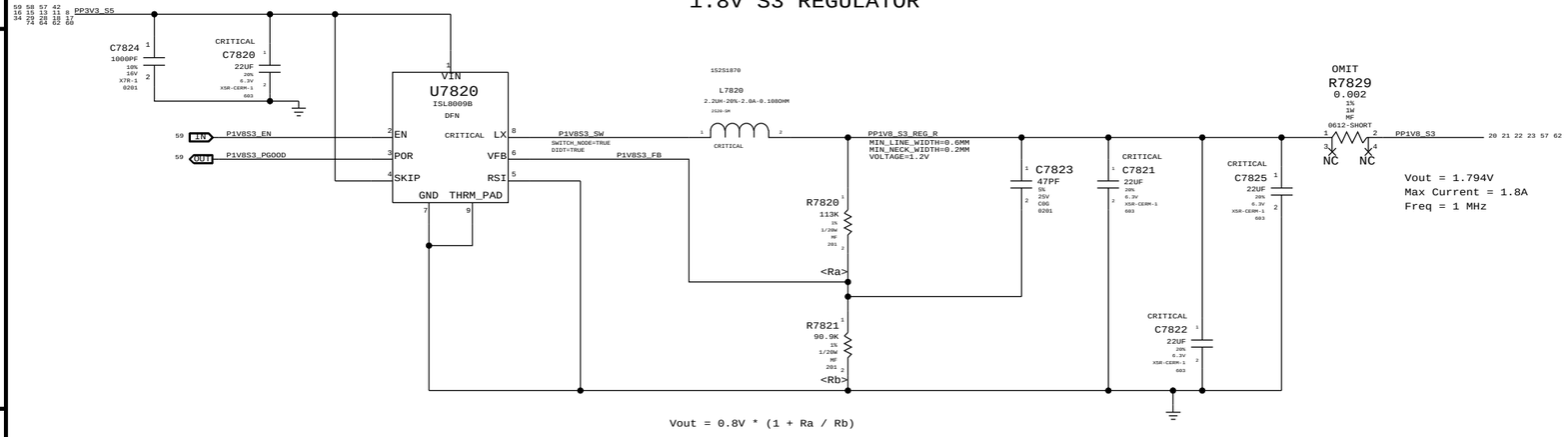
Keyboard Backlight Connector

CRITICAL
J7715
FF14A-4C-R11DL-B-3H
F-RT-SM
NC
518S0793

SYNC_MASTER=J43_MLB
SYNC_DATE=09/13/2012
PAGE TITLE
LCD/KBD Backlight Driver
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 77 OF 121
SHEET 56 OF 76

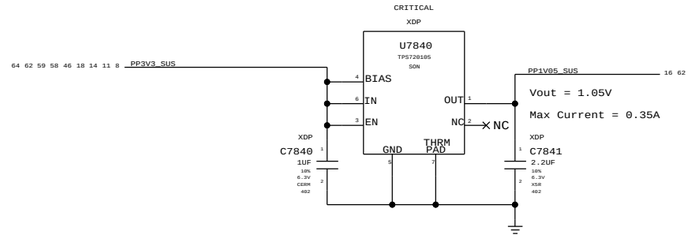
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.8V S3 REGULATOR

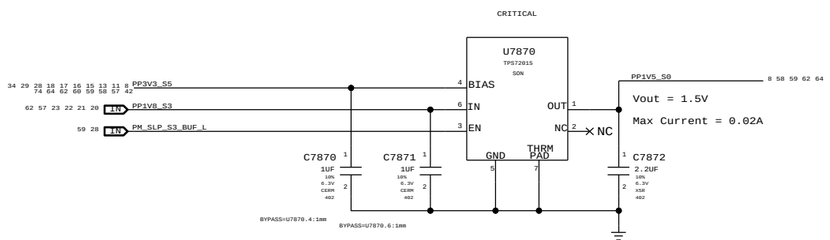


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO

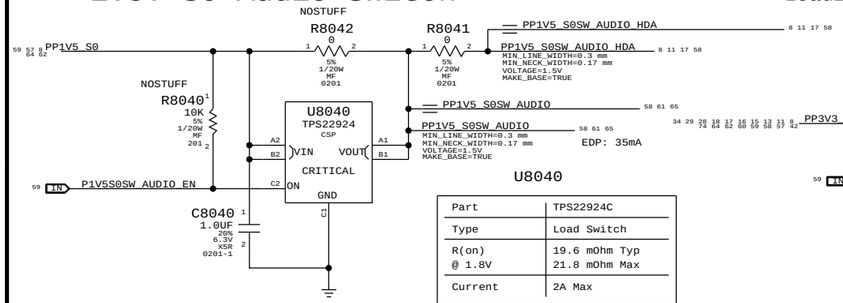


SYNC_MASTER=J43_MLB	SYNC_DATE=10/04/2012
PAGE TITLE: Misc Power Supplies	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 78 OF 121
	SHEET: 57 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.5V S0 Audio Switch

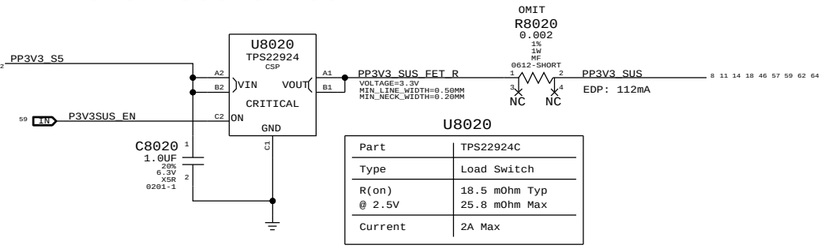
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

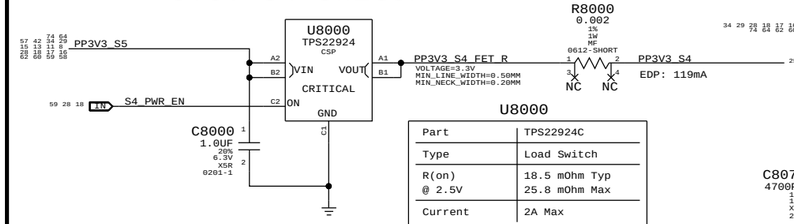
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

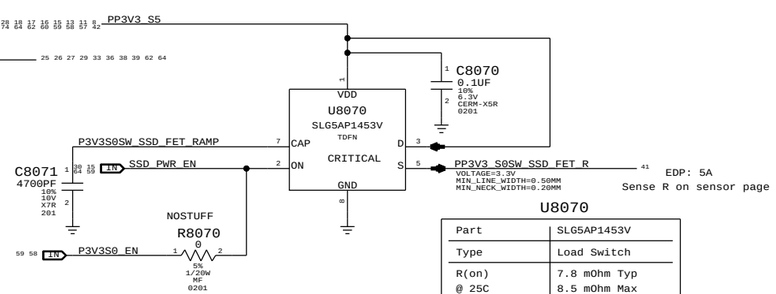
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

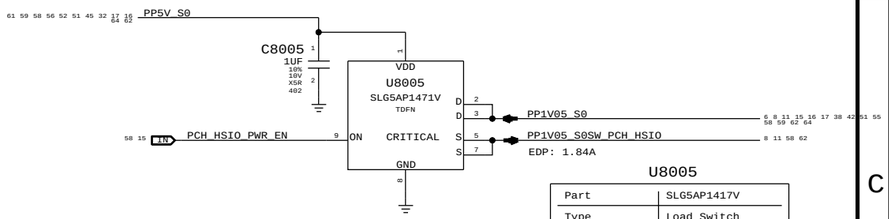
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

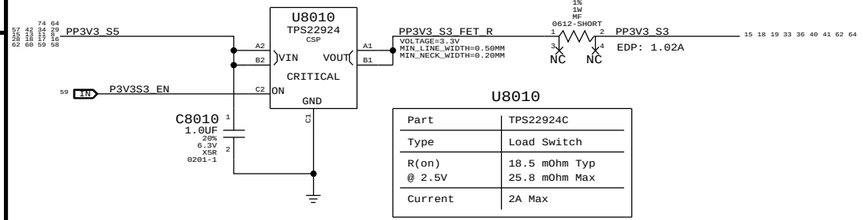


U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

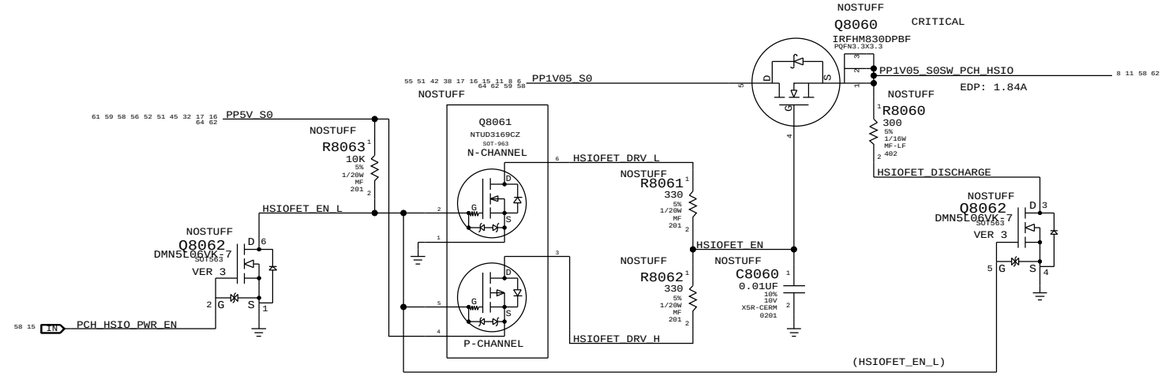
HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

3.3V S3 Switch

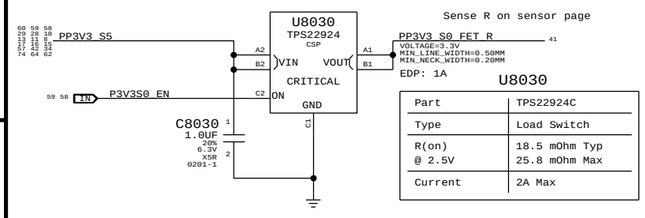


U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max



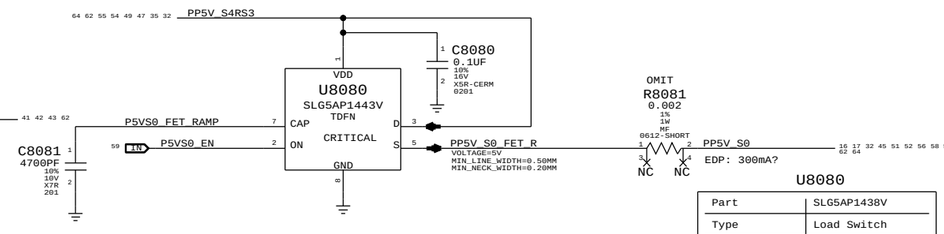
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

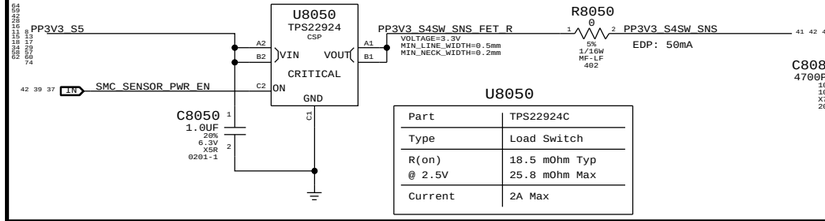
5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

3.3V Sensor Switch



U8050

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

SYNC_MASTER=J41_MLB SYNC_DATE=02/06/2013

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

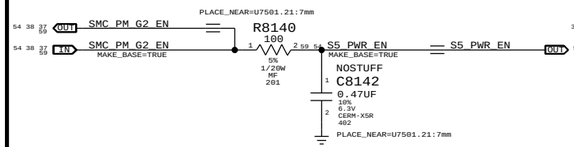
PAGE 80 OF 121

SHEET 58 OF 76

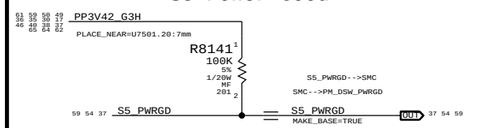
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

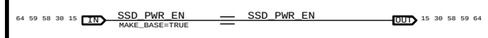
S5 Enables



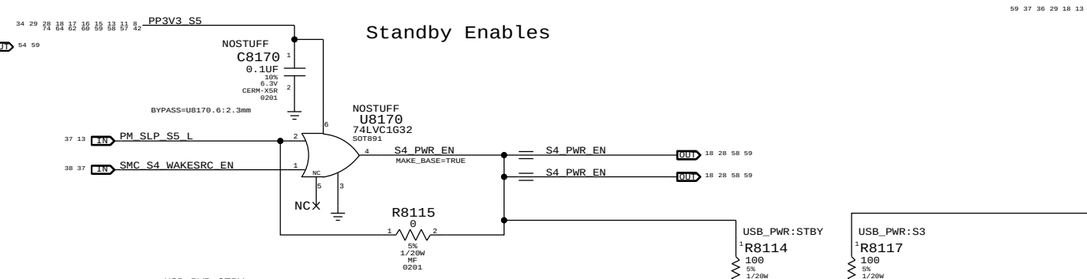
S5 Power Good



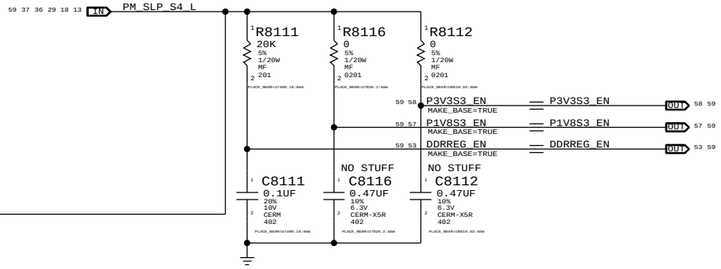
SSD Enable



Standby Enables



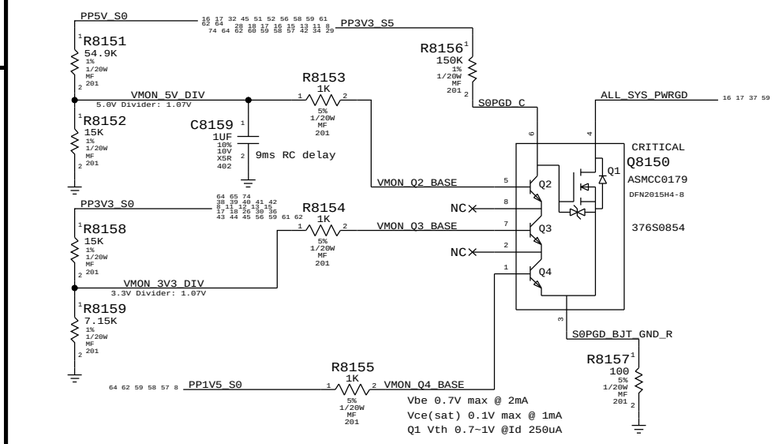
S3 Enables



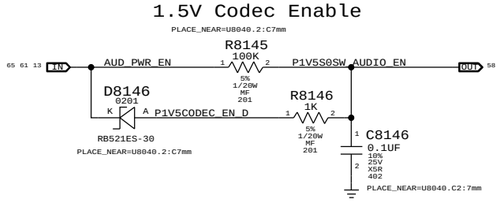
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S5_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (S3mtnAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (S3mnt)	1	0	0	0	0	0	0

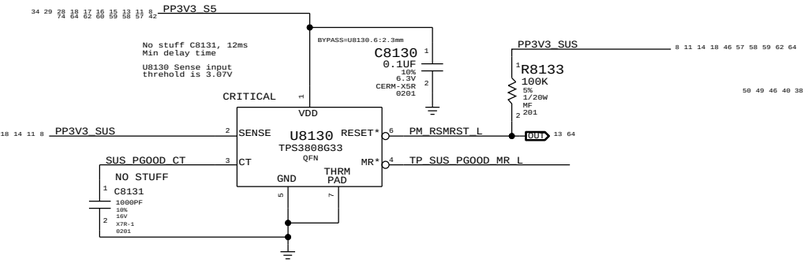
S0 Rail PGOOD (BJT Version)



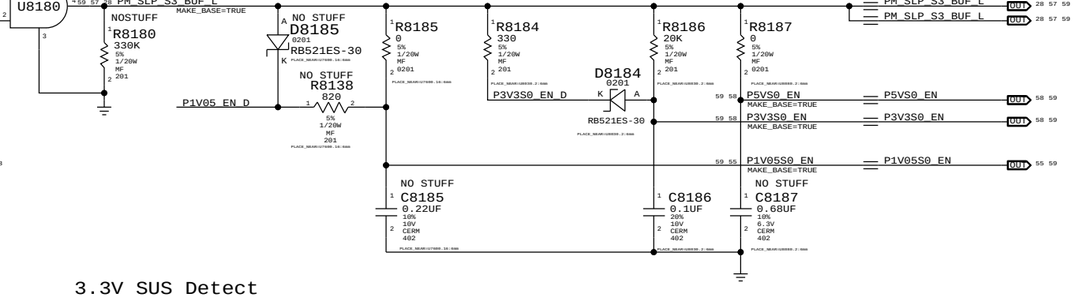
1.5V Codec Enable



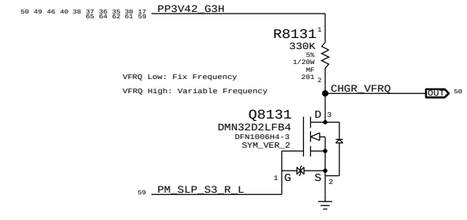
3.3V SUS Detect



S0 Enables



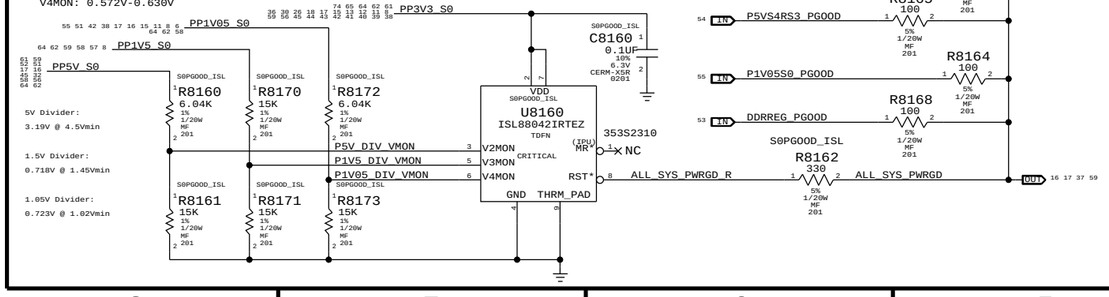
CHGR VFRQ Generation



S0 Rail PGOOD Circuitry

(ISL version used for development)

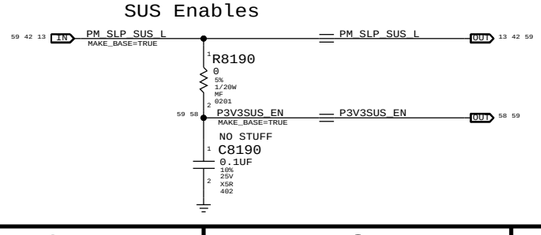
Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V



S5 Rail PGOOD Circuitry

S0 Rail Enable

SUS Enables



SYNC_MASTER=J43_MLB SYNC_DATE=09/16/2013

PAGE TITLE

Power Control

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

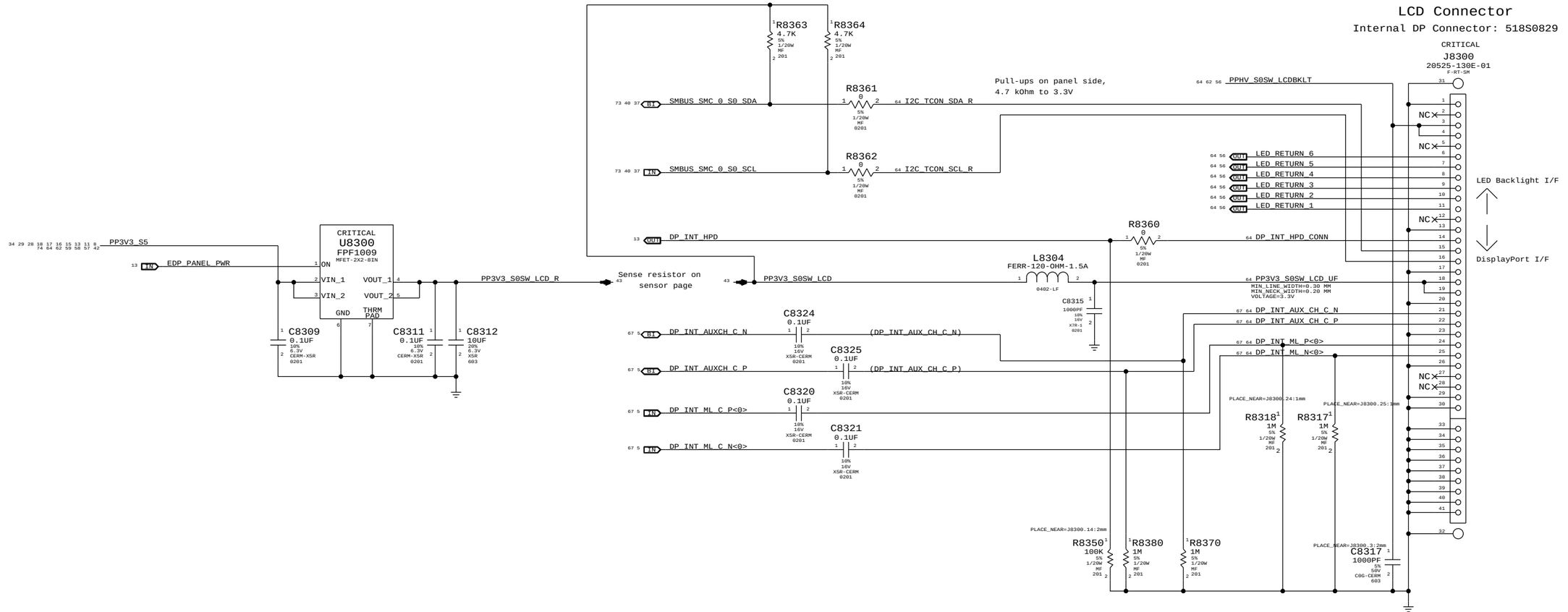
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 81 OF 121

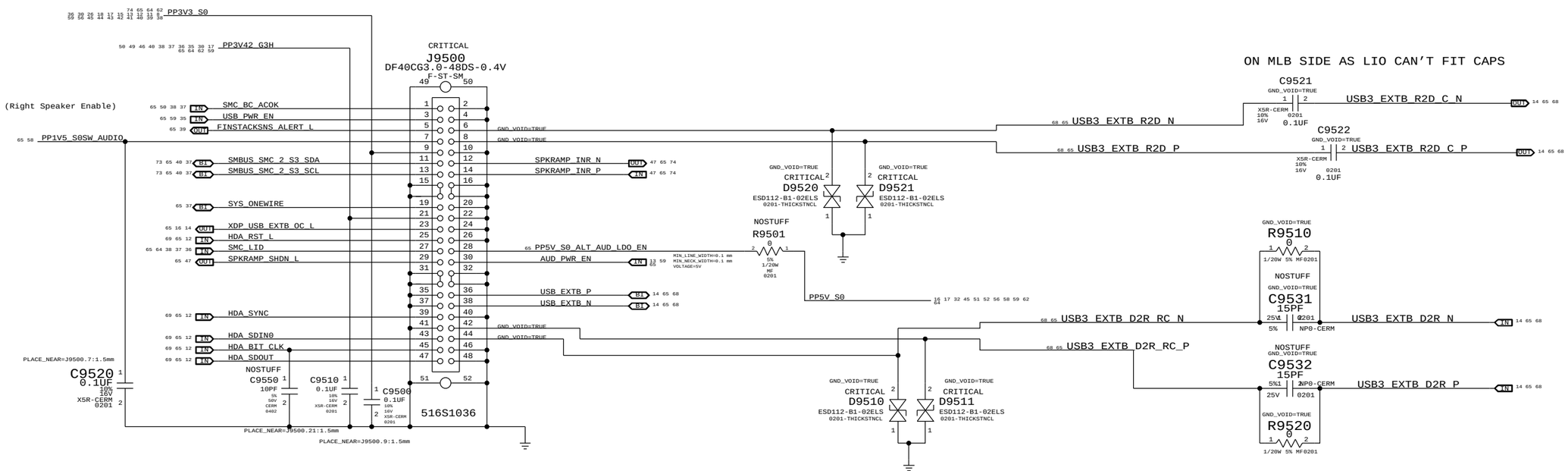
SHEET 59 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB	SYNC_DATE=09/11/2012
PAGE TITLE	Internal DisplayPort Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 83 OF 121
	SHEET 60 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



IO Ports

SYNC_MASTER=CLEAN_J43 SYNC_DATE=11/13/2012

PAGE TITLE
Left I/O (LIO) Connector

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 95 OF 121
SHEET 61 OF 76

"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H
PPBUS_G3H

PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS

PPBUS_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_OTHER_ISNS

PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H_ISOL
PPDCIN_G3H_ISOL

PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H

PP3V42_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP3V42_G3H ×16

PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE

PPVRTC_G3H

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S5
PP5V_S5

PP5V_S4RS3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4RS3 ×5

PP5V_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0 ×10

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S5 ×30

PP3V3_S4
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4 ×10

PP3V3_SUS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_SUS ×20

PP3V3_S3
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3 ×20

PP3V3_S0
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0 ×50

PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4SW_SNS ×20

PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_SSD ×2

PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4_TBTAPWR

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S3
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

2A max supply

PP1V8_S3 ×3

PP1V2_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_S3 ×10

PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_SUS ×2

PP1V5_S0
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V5_S0 ×4

PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP0V6_S0_DDRVTT ×3

PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_S0 ×20

PP1V05_S0SW_PCH_HSIO
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

1.84A

PP1V05_S0SW_PCH_HSIO ×2

LCDBKLT Rail

PPHV_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=56V
MAKE_BASE=TRUE

PPHV_S0SW_LCDBKLT
PPHV_S0SW_LCDBKLT

TBT Rails (off when no cable)

PP15V_TBT
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE

PP15V_TBT
PP15V_TBT

PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_TBTLC
PP3V3_TBTLC

PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVIN_SW_TBTBST
VOLTAGE=12.8V

CPU "VCORE" RAILS

PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCC_S0_CPU
PPVCC_S0_CPU

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 100 OF 121
SHEET 62 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 Command/Address

	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>		20 24 70
	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>		20 24 70
	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>		20 24 70
	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>		20 24 70
	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>		20 24 70
	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>		20 24 70
70 63 24 20 7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>		7 20 24 63 70
	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>		20 24 70
	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>		20 24 70
	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>		20 24 70
	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>		21 24 70
	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>		21 24 70
	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>		21 24 70
	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>		21 24 70
	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>		21 24 70
	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>		21 24 70
70 63 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>		7 21 24 63 70
	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>		21 24 70
	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>		21 24 70
	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>		21 24 70
70 63 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>		7 20 21 24 63 70
63 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1		7 63
63 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2		7 63
	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>		22 24 70
	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>		22 24 70
	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>		22 24 70
	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>		22 24 70
	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>		22 24 70
	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>		22 24 70
70 63 24 22 7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>		7 22 24 63 70
	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>		22 24 70
	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>		22 24 70
	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>		22 24 70
	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>		23 24 70
	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>		23 24 70
	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>		23 24 70
	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>		23 24 70
	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>		23 24 70
	=MEM_B_A<2>	TRUE	MEM_B_CAB<5>		23 24 70
70 63 24 23 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>		7 23 24 63 70
	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>		23 24 70
	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>		23 24 70
	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>		23 24 70
70 63 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>		7 22 23 24 63 70
63 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3		7 63
63 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4		7 63

Memory Bit/Byte Swizzle

20	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<9>		7 70
20	=MEM_A_DQ<1>	TRUE	MEM_A_DQ<12>		7 70
20	=MEM_A_DQ<2>	TRUE	MEM_A_DQ<10>		7 70
20	=MEM_A_DQ<3>	TRUE	MEM_A_DQ<11>		7 70
20	=MEM_A_DQ<4>	TRUE	MEM_A_DQ<8>		7 70
20	=MEM_A_DQ<5>	TRUE	MEM_A_DQ<13>		7 70
20	=MEM_A_DQ<6>	TRUE	MEM_A_DQ<14>		7 70
20	=MEM_A_DQ<7>	TRUE	MEM_A_DQ<15>		7 70
20	=MEM_A_DQ<8>	TRUE	MEM_A_DQ<0>		7 70
20	=MEM_A_DQ<9>	TRUE	MEM_A_DQ<1>		7 70
20	=MEM_A_DQ<10>	TRUE	MEM_A_DQ<2>		7 70
20	=MEM_A_DQ<11>	TRUE	MEM_A_DQ<7>		7 70
20	=MEM_A_DQ<12>	TRUE	MEM_A_DQ<4>		7 70
20	=MEM_A_DQ<13>	TRUE	MEM_A_DQ<5>		7 70
20	=MEM_A_DQ<14>	TRUE	MEM_A_DQ<3>		7 70
20	=MEM_A_DQ<15>	TRUE	MEM_A_DQ<6>		7 70
20	=MEM_A_DQ<16>	TRUE	MEM_A_DQ<29>		7 70
20	=MEM_A_DQ<17>	TRUE	MEM_A_DQ<28>		7 70
20	=MEM_A_DQ<18>	TRUE	MEM_A_DQ<27>		7 70
20	=MEM_A_DQ<19>	TRUE	MEM_A_DQ<31>		7 70
20	=MEM_A_DQ<20>	TRUE	MEM_A_DQ<24>		7 70
20	=MEM_A_DQ<21>	TRUE	MEM_A_DQ<25>		7 70
20	=MEM_A_DQ<22>	TRUE	MEM_A_DQ<26>		7 70
20	=MEM_A_DQ<23>	TRUE	MEM_A_DQ<30>		7 70
20	=MEM_A_DQ<24>	TRUE	MEM_A_DQ<18>		7 70
20	=MEM_A_DQ<25>	TRUE	MEM_A_DQ<21>		7 70
20	=MEM_A_DQ<26>	TRUE	MEM_A_DQ<16>		7 70
20	=MEM_A_DQ<27>	TRUE	MEM_A_DQ<23>		7 70
20	=MEM_A_DQ<28>	TRUE	MEM_A_DQ<20>		7 70
20	=MEM_A_DQ<29>	TRUE	MEM_A_DQ<19>		7 70
20	=MEM_A_DQ<30>	TRUE	MEM_A_DQ<22>		7 70
20	=MEM_A_DQ<31>	TRUE	MEM_A_DQ<17>		7 70
21	=MEM_A_DQ<32>	TRUE	MEM_A_DQ<41>		7 70
21	=MEM_A_DQ<33>	TRUE	MEM_A_DQ<44>		7 70
21	=MEM_A_DQ<34>	TRUE	MEM_A_DQ<46>		7 70
21	=MEM_A_DQ<35>	TRUE	MEM_A_DQ<47>		7 70
21	=MEM_A_DQ<36>	TRUE	MEM_A_DQ<40>		7 70
21	=MEM_A_DQ<37>	TRUE	MEM_A_DQ<45>		7 70
21	=MEM_A_DQ<38>	TRUE	MEM_A_DQ<42>		7 70
21	=MEM_A_DQ<39>	TRUE	MEM_A_DQ<43>		7 70
21	=MEM_A_DQ<40>	TRUE	MEM_A_DQ<36>		7 70
21	=MEM_A_DQ<41>	TRUE	MEM_A_DQ<37>		7 70
21	=MEM_A_DQ<42>	TRUE	MEM_A_DQ<34>		7 70
21	=MEM_A_DQ<43>	TRUE	MEM_A_DQ<39>		7 70
21	=MEM_A_DQ<44>	TRUE	MEM_A_DQ<32>		7 70
70 63 21 7	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>		7 21 63 70
21	=MEM_A_DQ<46>	TRUE	MEM_A_DQ<35>		7 70
21	=MEM_A_DQ<47>	TRUE	MEM_A_DQ<38>		7 70
21	=MEM_A_DQ<48>	TRUE	MEM_A_DQ<52>		7 70
21	=MEM_A_DQ<49>	TRUE	MEM_A_DQ<51>		7 70
21	=MEM_A_DQ<50>	TRUE	MEM_A_DQ<48>		7 70
21	=MEM_A_DQ<51>	TRUE	MEM_A_DQ<49>		7 70
21	=MEM_A_DQ<52>	TRUE	MEM_A_DQ<53>		7 70
21	=MEM_A_DQ<53>	TRUE	MEM_A_DQ<50>		7 70
21	=MEM_A_DQ<54>	TRUE	MEM_A_DQ<54>		7 70
21	=MEM_A_DQ<55>	TRUE	MEM_A_DQ<55>		7 70
21	=MEM_A_DQ<56>	TRUE	MEM_A_DQ<58>		7 70
21	=MEM_A_DQ<57>	TRUE	MEM_A_DQ<62>		7 70
21	=MEM_A_DQ<58>	TRUE	MEM_A_DQ<60>		7 70
21	=MEM_A_DQ<59>	TRUE	MEM_A_DQ<61>		7 70
21	=MEM_A_DQ<60>	TRUE	MEM_A_DQ<59>		7 70
21	=MEM_A_DQ<61>	TRUE	MEM_A_DQ<63>		7 70
21	=MEM_A_DQ<62>	TRUE	MEM_A_DQ<57>		7 70
21	=MEM_A_DQ<63>	TRUE	MEM_A_DQ<56>		7 70
20	=MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<1>		7 70
20	=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<1>		7 70
20	=MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<0>		7 70
20	=MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<0>		7 70
20	=MEM_A_DQS_P<2>	TRUE	MEM_A_DQS_P<3>		7 70
20	=MEM_A_DQS_N<2>	TRUE	MEM_A_DQS_N<3>		7 70
20	=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<2>		7 70
20	=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<2>		7 70
21	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<5>		7 70
21	=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<5>		7 70
21	=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<4>		7 70
21	=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<4>		7 70
70 63 21 7	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>		7 21 63 70
70 63 21 7	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>		7 21 63 70
21	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<7>		7 70
21	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<7>		7 70

22	=MEM_B_DQ<0>	TRUE	MEM_B_DQ<12>		7 70
22	=MEM_B_DQ<1>	TRUE	MEM_B_DQ<9>		7 70
22	=MEM_B_DQ<2>	TRUE	MEM_B_DQ<10>		7 70
22	=MEM_B_DQ<3>	TRUE	MEM_B_DQ<11>		7 70
22	=MEM_B_DQ<4>	TRUE	MEM_B_DQ<13>		7 70
22	=MEM_B_DQ<5>	TRUE	MEM_B_DQ<8>		7 70
22	=MEM_B_DQ<6>	TRUE	MEM_B_DQ<14>		7 70
22	=MEM_B_DQ<7>	TRUE	MEM_B_DQ<15>		7 70
22	=MEM_B_DQ<8>	TRUE	MEM_B_DQ<0>		7 70
22	=MEM_B_DQ<9>	TRUE	MEM_B_DQ<1>		7 70
22	=MEM_B_DQ<10>	TRUE	MEM_B_DQ<2>		7 70
22	=MEM_B_DQ<11>	TRUE	MEM_B_DQ<7>		7 70
22	=MEM_B_DQ<12>	TRUE	MEM_B_DQ<4>		7 70
22	=MEM_B_DQ<13>	TRUE	MEM_B_DQ<5>		7 70
22	=MEM_B_DQ<14>	TRUE	MEM_B_DQ<6>		7 70
22	=MEM_B_DQ<15>	TRUE	MEM_B_DQ<3>		7 70
22	=MEM_B_DQ<16>	TRUE	MEM_B_DQ<28>		7 70
22	=MEM_B_DQ<17>	TRUE	MEM_B_DQ<29>		7 70
22	=MEM_B_DQ<18>	TRUE	MEM_B_DQ<30>		7 70
22	=MEM_B_DQ<19>	TRUE	MEM_B_DQ<27>		7 70
22	=MEM_B_DQ<20>	TRUE	MEM_B_DQ<24>		7 70
22	=MEM_B_DQ<21>	TRUE	MEM_B_DQ<25>		7 70
22	=MEM_B_DQ<22>	TRUE	MEM_B_DQ<31>		7 70
22	=MEM_B_DQ<23>	TRUE	MEM_B_DQ<26>		7 70
22	=MEM_B_DQ<24>	TRUE	MEM_B_DQ<20>		7 70
22	=MEM_B_DQ<25>	TRUE	MEM_B_DQ<16>		7 70
22	=MEM_B_DQ<26>	TRUE	MEM_B_DQ<23>		7 70
22	=MEM_B_DQ<27>	TRUE	MEM_B_DQ<22>		7 70
22	=MEM_B_DQ<28>	TRUE	MEM_B_DQ<21>		7 70
22	=MEM_B_DQ<29>	TRUE	MEM_B_DQ<17>		7 70
22	=MEM_B_DQ<30>	TRUE	MEM_B_DQ<18>		7 70
22	=MEM_B_DQ<31>	TRUE	MEM_B_DQ<19>		7 70
23	=MEM_B_DQ<32>	TRUE	MEM_B_DQ<44>		7 70
23	=MEM_B_DQ<33>	TRUE	MEM_B_DQ<41>		7 70
23	=MEM_B_DQ<34>	TRUE	MEM_B_DQ<42>		7 70
23	=MEM_B_DQ<35>	TRUE	MEM_B_DQ<43>		7 70
23	=MEM_B_DQ<36>	TRUE	MEM_B_DQ<45>		7 70
23	=MEM_B_DQ<37>	TRUE	MEM_B_DQ<40>		7 70
23	=MEM_B_DQ<38>	TRUE	MEM_B_DQ<46>		7 70
23	=MEM_B_DQ<39>	TRUE	MEM_B_DQ<47>		7 70
70 63 23 7	MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>		7 23 63 70
23	=MEM_B_DQ<41>	TRUE	MEM_B_DQ<33>		7 70
23	=MEM_B_DQ<42>	TRUE	MEM_B_DQ<34>		7 70
23	=MEM_B_DQ<43>	TRUE	MEM_B_DQ<39>		7 70
23	=MEM_B_DQ<44>	TRUE	MEM_B_DQ<36>		7 70
23	=MEM_B_DQ<45>	TRUE	MEM_B_DQ<37>		7 70
23	=MEM_B_DQ<46>	TRUE	MEM_B_DQ<38>		7 70
23	=MEM_B_DQ<47>	TRUE	MEM_B_DQ<35>		7 70
23	=MEM_B_DQ<48>	TRUE	MEM_B_DQ<57>		7 70
23	=MEM_B_DQ<49>	TRUE	MEM_B_DQ<56>		7 70
23	=MEM_B_DQ<50>	TRUE	MEM_B_DQ<60>		7 70
23	=MEM_B_DQ<51>	TRUE	MEM_B_DQ<59>		7 70
23	=MEM_B_DQ<52>	TRUE	MEM_B_DQ<63>		7 70
23	=MEM_B_DQ<53>	TRUE	MEM_B_DQ<62>		7 70
23	=MEM_B_DQ<54>	TRUE	MEM_B_DQ<58>		7 70
23	=MEM_B_DQ<55>	TRUE	MEM_B_DQ<61>		7 70
23	=MEM_B_DQ<56>	TRUE	MEM_B_DQ<49>		7 70
23	=MEM_B_DQ<57>	TRUE	MEM_B_DQ<51>		7 70
23	=MEM_B_DQ<58>	TRUE	MEM_B_DQ<48>		7 70
23	=MEM_B_DQ<59>	TRUE	MEM_B_DQ<53>		7 70
23	=MEM_B_DQ<60>	TRUE	MEM_B_DQ<52>		7 70
23	=MEM_B_DQ<61>	TRUE	MEM_B_DQ<55>		7 70
23	=MEM_B_DQ<62>	TRUE	MEM_B_DQ<50>		7 70
23	=MEM_B_DQ<63>	TRUE	MEM_B_DQ<54>		7 70
22	=MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<1>		7 70
22	=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<1>		7 70
22	=MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<0>		7 70
22	=MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<0>		7 70
22	=MEM_B_DQS_P<2>	TRUE	MEM_B_DQS_P<3>		7 70
22	=MEM_B_DQS_N<2>	TRUE	MEM_B_DQS_N<3>		7 70
22	=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<2>		7 70
22	=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<2>		7 70
23	=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<5>		7 70
23	=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<5>		7 70
23	=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<4>		7 70
23	=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<4>		7 70
23	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<7>		7 70
23	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<7>		7 70
70 63 23 7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>		7 23 63 70
70 63 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>		7 23 63 70

SYNC_MASTER=J41_MLB SYNC_DATE=08/30/2012

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 102 OF 121

SHEET 63 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Functional Test Points

J3501: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN	(Need 6 TPs)	29 37 38 39 41
TRUE	WIFI_EVENT_L		29 37 38
TRUE	PCIE_AP_R2D_N		29 69
TRUE	PCIE_AP_R2D_P		29 69
TRUE	PCIE_CLK100M_AP_N		12 29 69
TRUE	PCIE_CLK100M_AP_P		12 29 69
TRUE	PCIE_AP_D2R_P		14 29 69
TRUE	PCIE_AP_D2R_N		14 29 69
TRUE	PCIE_WAKE_L		13 29 31
TRUE	AP_RESET_CONN_L		29
TRUE	AP_CLKREQ_O_L		29
TRUE	USB_BT_CONN_P		29 68
TRUE	USB_BT_CONN_N		29 68
TRUE	PP3V3_S4		25 26 27 29 33 36 38 39 58 62 64

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC_TEST

TRUE	PP3V3_S0SW_SSD_FLT	(Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>		30 67
TRUE	PCIE_SSD_R2D_P<3..0>		30 67
TRUE	PP3V3_S0		42 43 44 45 56 59 61 62 64 65 74
TRUE	SSD_RESET_CONN_L		13 17 18 26 30 36 38 39 40 41 30
TRUE	SSD_CLKREQ_CONN_L		30
TRUE	SMC_OOB1_R2D_CONN_L		30
TRUE	SMC_OOB1_D2R_CONN_L		30
TRUE	SSD_PCIE_SEL_L		30
TRUE	SSD_SR_EN_L		15 30
TRUE	SMC_PWRFAIL_WARN_L		30 37
TRUE	SSD_PWR_EN		15 30 58 59
TRUE	PCIE_SSD_D2R_N<3..0>		12 30 67
TRUE	PCIE_SSD_D2R_P<3..0>		12 30 67
TRUE	PCIE_CLK100M_SSD_N		12 30 67
TRUE	PCIE_CLK100M_SSD_P		12 30 67

(Need to add 6 GND TPS)

J4002: Camera Connector

FUNC_TEST

TRUE	MIPI_CLK_CONN_N		32 72
TRUE	MIPI_CLK_CONN_P		32 72
TRUE	CAM_SENSOR_WAKE_L_CONN		32
TRUE	MIPI_DATA_CONN_N		32 72
TRUE	MIPI_DATA_CONN_P		32 72
TRUE	SMBUS_SMC_1_S0_SDA		14 32 37 40 43 44 69 73
TRUE	SMBUS_SMC_1_S0_SCL		14 32 37 40 43 44 69 73
TRUE	I2C_CAM_SCK		31 32
TRUE	I2C_CAM_SDA		31 32
TRUE	PP5V_S3RS0_ALSCAM_F	(Need TBD TPs)	32

(Need to add TBD GND TPs)

J6100: LPC+SPI Connector

FUNC_TEST

TRUE	SPI_ALT_IO2_WP_L	46
TRUE	SPI_ALT_IO3_HOLD_L	46
TRUE	LPC_AD<3..0>	14 37 69
TRUE	SPI_ALT_IO0_MOSI	46
TRUE	XDP_LPCPLUS_GPIO	15 16
TRUE	LPCPLUS_RESET_L	69
TRUE	SMC_TDO	37 38
TRUE	TP_SMC_TRST_L	
TRUE	TP_SMC_MD1	
TRUE	SMC_TX_L	37 38
TRUE	SPI_ALT_IO1_MISO	46
TRUE	LPC_FRAME_L	14 37 69
TRUE	SPIROM_USE_MLB	15 46
TRUE	PM_CLKRUN_L	13 37
TRUE	SPI_ALT_CLK	46
TRUE	SPI_ALT_CS_L	46
TRUE	LPC_SERIRQ	15 37
TRUE	LPC_PWRDWN_L	13 37
TRUE	SMC_TDI	37 38
TRUE	SMC_TCK	37 38 46
TRUE	SMC_RESET_L	37 38 46 50
TRUE	SMC_ROMBOOT	
TRUE	SMC_RX_L	37 38
TRUE	SMC_TMS	37 38 46

(Need to add 6 GND TPs)

J6000: Fan Connector

FUNC_TEST

TRUE	PP5V_S0		16 17 32 45 51 52 56 58 59 61 62
TRUE	FAN_RT_TACH		45
TRUE	FAN_RT_PWM		45

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC_TEST

TRUE	SMC_LID		36 37 38 61 65
TRUE	TPAD_SPI_MISO_R		36
TRUE	USB_TPAD_P		14 36 68
TRUE	USB_TPAD_N		14 36 68
TRUE	TPAD_SPI_CLK_R		36
TRUE	TPAD_WAKE_L		36
TRUE	TPAD_SPI_MOSI_R		36
TRUE	PP3V3_S4_IPD		36
TRUE	TPAD_SPI_CS_R_L		36
TRUE	TPAD_SPI_IF_EN_CONN		36
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN		36
TRUE	PP5V_S4_IPD		36
TRUE	TPAD_USB_IF_EN_CONN		36
TRUE	SMBUS_SMC_3_SDA		36 37 40 44 73
TRUE	SMBUS_SMC_3_SCL		36 37 40 44 73
TRUE	SMC_LSOC_RST_L		36 38
TRUE	PP3V42_G3H		17 30 35 36 37 38 40 46 49 50 59 61 62 64 65
TRUE	SMC_ONOFF_L		36 37 38

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC_TEST

TRUE	PPDCIN_G3H	(Need 4 TPs)	49 50 62 64
TRUE	PP5V_S4RS3	(Need 3 TPs)	32 35 47 49 54 55 58 62

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	47 74
TRUE	SPKRAMP_ROUT_N	47 74

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	(Need 4 TPs)	48 50
TRUE	SMBUS_SMC_5_G3_SCL		37 40 48 50 73
TRUE	SMBUS_SMC_5_G3_SDA		37 40 48 50 73
TRUE	SYS_DETECT_L		48

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC_TEST

TRUE	PPHV_S0SW_LCDBKLT	(Need 2 TPs)	56 60 62
TRUE	LED_RETURN_6		56 60
TRUE	LED_RETURN_5		56 60
TRUE	LED_RETURN_4		56 60
TRUE	LED_RETURN_3		56 60
TRUE	LED_RETURN_2		56 60
TRUE	LED_RETURN_1		56 60
TRUE	DP_INT_HPD_CONN		60
TRUE	I2C_TCON_SDA_R		60
TRUE	I2C_TCON_SCL_R		60
TRUE	PP3V3_S0SW_LCD_UF	(Need 2 TPs)	60
TRUE	DP_INT_AUX_CH_C_N		60 67
TRUE	DP_INT_AUX_CH_C_P		60 67
TRUE	DP_INT_ML_P<0>		60 67
TRUE	DP_INT_ML_N<0>		60 67

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_ANODE	56
TRUE	KBDLED_FB	56

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC_TEST

TP76	TRUE	XDP_CPU_TCK	6 16 67
TP77	TRUE	XDP_PCH_TCK	12 16 69
TP78	TRUE	XDP_CPU_TDI	6 16 67
TP79	TRUE	XDP_CPU_TDO	6 16 67
TP80	TRUE	XDP_CPUPCH_TRST_L	6 12 16 67
TP81	TRUE	XDP_CPU_TMS	6 16 67
TP82	TRUE	XDP_PCH_TMS	12 16 69
TP83	TRUE	XDP_PCH_TDI	12 16 69
TP84	TRUE	XDP_PCH_TDO	12 16 69
TP85	TRUE	XDP_CPU_PREQ_L	6 16 67
TP86	TRUE	XDP_CPU_PRDY_L	6 16 67
TP87	TRUE	XDP_CPU_VCCST_PWRGD	16
TP88	TRUE	PM_RSMRST_L	13 59
TP89	TRUE	XDP_SYS_PWROK	16
TP90	TRUE	PM_SYSRST_L	13 17 37
TP91	TRUE	CPU_CFG<3>	6 16 67
TP92	TRUE	PP1V05_S0	6 8 11 15 16 17 38 42 51 55 58 59 62 64

(Need to add 2 GND TPs)

TP93 TRUE GND

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	27 41 42 49 50 56 62
TRUE	PPVIN_SW_TBTBST	62
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	41 51 52 53 55 62
TRUE	PPDCIN_G3H	49 50 62 64
TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50 59 61 62 64 65
TRUE	PPVRTC_G3H	8 12 13 17 62
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 34 42 57 58 59 60 62 74
TRUE	PP3V3_SUS	8 11 14 18 46 57 58 59 62
TRUE	PP3V3_S3	15 18 19 33 36 40 41 58 62
TRUE	PP3V3_S0	62 64 65 74
TRUE	PP3V3_S0SW_SSD	8 12 13 15 16 17 18 26 30 36 38 39 40 41 42 43 44 45 56 59 61
TRUE	PP1V5_S0	30 41 62
TRUE	PP1V05_S0	8 57 58 59 62
TRUE	PP15V_TBT	6 8 11 15 16 17 38 42 51 55 58 59 62 64
TRUE	PP3V3_TBTLC	27 28 62
TRUE	PP1V05_TBT	17 18 25 26 62
TRUE	PPVCC_S0_CPU	26
TRUE	PP1V05_TBTCIO	8 10 42 52 62
TRUE	PPBUS_S5_HS_OTHER_ISNS	26 62
TRUE	PPDCIN_G3H_ISOL	41 54 62
TRUE	PP3V3_S4	42 49 50 62

(Need to add 27 GND TPs)

25 26 27 29 33 36 38 39 58 62 64

NO_TEST Nets

NO_TEST
MAKE_BASE

64	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	64	CPU/PCH
64	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	64	
64 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 64	
64 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 64	
64 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 64	
64 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 64	
64 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 64	
64 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 64	
64 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 64	
64 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 64	
64 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 64	
64 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 64	
64 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 64	
64 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 64	
67	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5	
67	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5	
64 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 64	
64 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 64	
64 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 64	
64 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 64	
64 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 64	
64 37	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	37 64	SMC
64	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	64	
64	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	64	
64	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	64	
64 37	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	37 64	
64 37	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	37 64	
64 37	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	37 64	
64 37	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	37 64	
64 37	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	37 64	
64	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	64	
64	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	64	
64	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	64	
64 37	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	37 64	
64 37	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	37 64	
64 37	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	37 64	
64 37	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	37 64	
64 37	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	37 64	
71	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25	TBT
71	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25	
71	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25	
71	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25	
64 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 64	
71 64	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	64 71	
71 64	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	64 71	
71 64 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 64 71	
71 64 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 64 71	
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>		
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>		
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>		
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>		
64 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 64	
64 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 64	
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>		
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>		
64 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 64	
64 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 64	

Unused nets with offpage

(Nets with offpages not used on this project)

PCH_BT_UART_D2R	15	
PCH_BT_UART_R2D	15	
PCH_BT_UART_RTS_L	15	
PCH_BT_UART_CTS_L	15	
AUD_SPI_CS_L	15	
AUD_SPI_CLK	15	
AUD_SPI_MISO	15	
AUD_SPI_MOSI	15	
HDMITBTMUX_LATCH	13	
HDD_PWR_EN	15	
WOL_EN	14	
BT_PWRRST_L	15	
HDMITBTMUX_FLAG	13	
FW_PWR_EN		
FW_PME_L		
ENET_MEDIA_SENSE	15	
LCD_PSR_EN	15	
LCD_IRQ_L	15	
ODD_PWR_EN_L	13	
ENET_LOW_PWR	13	
AUD_IP_PERIPHERAL_DET		
AUD_I2C_INT_L		
AP_PCIE_DEV_WAKE	13	

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE

Func Test / No Test

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 104 OF 121

SHEET 64 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Functional Test Points

J9500: LIO Connector

FUNC_TEST

TRUE	PP3V42_G3H	17 30 35 36 37 38 40 46 49 50	
TRUE	PP3V3_S0	62 64 74 59 61 63 66	
TRUE	PP1V5_S0SW_AUDIO	9 11 12 13 15 17 18 26 30 36 38 39 40 41 42 43 44 45 56 59 61	
TRUE	SYS_ONEWIRE	37 61	
TRUE	SMC_BC_ACOK	37 38 50 61	
TRUE	USB_PWR_EN	35 59 61	
TRUE	SMBUS_SMC_2_S3_SDA	37 40 61 73	
TRUE	SMBUS_SMC_2_S3_SCL	37 40 61 73	
TRUE	SPKRAMP_SHDN_L	47 61	
TRUE	FINSTACKSNS_ALERT_L	39 61	
TRUE	SPKRAMP_INR_N	47 61 74	
TRUE	SPKRAMP_INR_P	47 61 74	
TRUE	USB_EXTB_N	14 61 68	
TRUE	USB_EXTB_P	14 61 68	
TRUE	PP5V_S0_ALT_AUD_LDO_EN	61	
TRUE	SMC_LID	36 37 38 61 64	
TRUE	HDA_SDOUT	12 61 69	
TRUE	HDA_BIT_CLK	12 61 69	
TRUE	HDA_SDIN0	12 61 69	
TRUE	XDP_USB_EXTB_OC_L	14 16 61	
TRUE	HDA_RST_L	12 61 69	
TRUE	HDA_SYNC	12 61 69	
TRUE	USB3_EXTB_D2R_RC_P	61 65 68	
TRUE	USB3_EXTB_D2R_RC_N	61 65 68	
TRUE	USB3_EXTB_R2D_P	61 65 68	
TRUE	USB3_EXTB_R2D_N	61 65 68	
TRUE	AUD_PWR_EN	13 59 61	

(Need to add 5 GND TPs)

SD Card Aliases

			MAKE_BASE		
68 65 34 14	USB3_SD_D2R_P		TRUE	USB3_SD_D2R_P	14 34 65 68
68 65 34 14	USB3_SD_D2R_N		TRUE	USB3_SD_D2R_N	14 34 65 68
68 65 34 14	USB3_SD_R2D_C_P		TRUE	USB3_SD_R2D_C_P	14 34 65 68
68 65 34 14	USB3_SD_R2D_C_N		TRUE	USB3_SD_R2D_C_N	14 34 65 68
65 39 37 34 15	PP3V3_S0SW_SD			PP3V3_S0SW_SD	15 34 37 39 65

(MAKE_BASE=TRUE on page 45)

Bead Probes

68 61 14	USB3_EXTB_D2R_N	TP	BEAD-PROBE	BPA511
68 61 14	USB3_EXTB_D2R_P	TP	BEAD-PROBE	BPA510
68 65 61	USB3_EXTB_D2R_RC_N	TP	BEAD-PROBE	BPA520
68 65 61	USB3_EXTB_D2R_RC_P	TP	BEAD-PROBE	BPA521
68 61 14	USB3_EXTB_R2D_C_N	TP	BEAD-PROBE	BPA513
68 61 14	USB3_EXTB_R2D_C_P	TP	BEAD-PROBE	BPA512
68 65 61	USB3_EXTB_R2D_N	TP	BEAD-PROBE	BPA523
68 65 61	USB3_EXTB_R2D_P	TP	BEAD-PROBE	BPA522

SYNC_MASTER=J41_MLB SYNC_DATE=09/13/2012

PAGE TITLE

Project FCT/NC/Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 105 OF 121

SHEET 65 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

SYNC MASTER=CONSTRAINTS SYNC DATE=10/24/2012

PAGE TITLE: PCB Rule Definitions

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 110 OF 121

SHEET: 66 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 38
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_ITP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 16 64
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 16 64
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
	CPU_45S	CPU_ITP	CPU_CFG<11..0>	6 16 64
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 37
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 37 38 51
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_AGTL	PM_THRMTRIP_L	15 38
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16 64
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16 64
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16 64
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16 64
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 12 16 64
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	
	CPU_45S	CPU_ITP	CPU_CFG<15..12>	6 16
(ESB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 51
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 51
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 51
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 51
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 51
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 64
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 64
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 64
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 64
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	60 64
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	60 64
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 60 64
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	60 64
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 60
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 60
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 111 OF 121

SHEET 67 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	14 29
USB_BT	USB_80D	USB	USB_BT_N	14 29
	USB_80D	USB	USB_BT_CONN_P	29 64
	USB_80D	USB	USB_BT_CONN_N	29 64
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 36 64
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 36 64
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
	USB_80D	USB	TPAD_SPI_MOSI_USB_P	
	USB_80D	USB	TPAD_SPI_MISO_USB_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
	SPI_45S	SPI	TPAD_SPI_MOSI	15 36
	SPI_45S	SPI	TPAD_SPI_MISO	15 36
	SPI_45S	SPI	TPAD_SPI_CLK	15 36
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 35
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 35
	UART_45S	UART	SMC_DEBUGPRT_TX_L	35 37 38
	UART_45S	UART	SMC_DEBUGPRT_RX_L	35 37 38
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	35
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	35
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 35
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 35
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	35
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	35
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 35
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 35
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 61 65
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 61 65
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 61 65
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 61 65
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	61 65
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	61 65
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	61 65
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	61 65
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 61 65
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 61 65
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_P	14 34 65
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3_SD_D2R_N	14 34 65
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_P	14 34 65
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3_SD_R2D_C_N	14 34 65
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	34
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	34
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	34
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	34
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC_MASTER=CLEAN_J43 SYNC_DATE=11/13/2012

PAGE TITLE: PCH Constraints 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 112 OF 121

SHEET: 68 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 37 64
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 37 64
	LPC_45S	LPC	LPCPLUS_RESET_L	64
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 19 40 56
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 19 40 56
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 40
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 40
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 37 40 43 44 64 73
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 37 40 43 44 64 73
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 61 65
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 61 65
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 61 65
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 61 65
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 61 65
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 38
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	37 38
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 46
	SPI_45S	SPI	SPI_CLK	46
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 46
	SPI_45S	SPI	SPI_MOSI	46
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 46
	SPI_45S	SPI	SPI_MISO_R	46
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 46
	SPI_45S	SPI	SPI_CS0_L	46
	SPI_45S	SPI	SPI_SMC_CLK	37 46
	SPI_45S	SPI	SPI_SMC_MOSI	37 46
	SPI_45S	SPI	SPI_SMC_MISO	37 46
	SPI_45S	SPI	SPI_SMC_CS_L	37 46
	SPI_45S	SPI	SPI_MLB_CLK	46
	SPI_45S	SPI	SPI_MLB_IO0_MOSI	46
	SPI_45S	SPI	SPI_MLB_IO1_MISO	46
	SPI_45S	SPI	SPI_MLB_CS_L	46
	SPI_45S	SPI	SPI_IO<2>	14 46
	SPI_45S	SPI	SPI_IO2_R	46
	SPI_45S	SPI	SPI_MLB_IO2_WP_L	46
	SPI_45S	SPI	SPI_IO<3>	14 46
	SPI_45S	SPI	SPI_IO3_R	46
	SPI_45S	SPI	SPI_MLB_IO3_HOLD_L	46
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	29 64
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	29 64
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 29
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 29 64
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 29 64
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 29 64
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16 64
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16 64
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16 64
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16 64
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	31 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	31 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	34
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	34 75
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	34

SYNC_MASTER=J41_MLB SYNC_DATE=12/14/2012

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 113 OF 121

SHEET: 69 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 20 21 24 63
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	7 20 24 63
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	7 21 24 63
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 63
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 63
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 63
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 63
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 21 63
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 63
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 63
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 63
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 63
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 63
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 63
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 63
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 63
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 63
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 63
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 63
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 63
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 63
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 63
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 63
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 21 63
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 21 63
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 63
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 63
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 22 23 24 63
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	7 22 24 63
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	7 23 24 63
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 63
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 63
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 63
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 63
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 23 63
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 63
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 63
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 63
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 63
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 63
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 63
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 63
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 63
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 63
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 63
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 63
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 63
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 63
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 63
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 63
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 23 63
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 23 63
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 63
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 63
	MEM_PWR		PP1V2_S3	17 19 20 21 22 23 42 63 65
	MEM_PWR		PP0V6_S3_MEM_VREFCA_A	18 19 20 21
	MEM_PWR		PP0V6_S3_MEM_VREFDQ_A	18 19 20 21
	MEM_PWR		PP0V6_S3_MEM_VREFCA_B	18 19 22 23
	MEM_PWR		PP0V6_S3_MEM_VREFDQ_B	18 19 22 23

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 114 OF 121

SHEET: 70 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	64
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	64
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2>	64
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2>	64
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	64
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	64
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP	25 64
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN	25 64
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 115 OF 121

SHEET: 71 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 64
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 64
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 64
		S2_MEM_PWR	PP1V35_CAM	31 32
		S2_MEM_PWR	PP0V675_CAM_VREF	31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32

SYNC_MASTER=J41_MLB SYNC_DATE=01/30/2013

PAGE TITLE: Camera Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 116 OF 121

SHEET: 72 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SCL	37 40 60
SMBUS_SMC_0_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SDA	37 40 60
SMBUS_SMC_1_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 37 40 43 44 64 69
SMBUS_SMC_1_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 37 40 43 44 64 69
SMBUS_SMC_2_S3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SCL	37 40 61 65
SMBUS_SMC_2_S3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SDA	37 40 61 65
SMBUS_SMC_3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_3_SCL	36 37 40 44 64
SMBUS_SMC_3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_3_SDA	36 37 40 44 64
SMBUS_SMC_5_G3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SCL	37 40 48 50 64
SMBUS_SMC_5_G3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SDA	37 40 48 50 64

SMBus Charger Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SENSE_DIFFPAIR			CHGR_CSI_P	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N	50
	2TO1_DIFFPAIR		CHGR_CSI_R_P	50
	2TO1_DIFFPAIR		CHGR_CSI_R_N	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P	50
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N	50
	2TO1_DIFFPAIR		CHGR_CSO_R_P	43 50
	2TO1_DIFFPAIR		CHGR_CSO_R_N	43 50

SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 117 OF 121

SHEET 73 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.300 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	44
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P	42 52
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N	42 52
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	42 52
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	42 52
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R	42 43
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R	42 43
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P	42
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P	41
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P	42 55
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N	42 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	41 43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	41 43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N	41 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P	41 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N	43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P	43
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	43 44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	43 44
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	47 61 65
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	47 61 65
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	47
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	47
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	47 64
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	47 64
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 34 42 62 64 65
		SB_POWER	PP3V3_S0	8 11 12 13 15 17 18 26 30 36 38 39 40 41 42 43 44 45 56 59 61
	GND		GND	

SYNC_MASTER=J41_MLB SYNC_DATE=12/07/2012

PAGE TITLE: Project Specific Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 118 OF 121

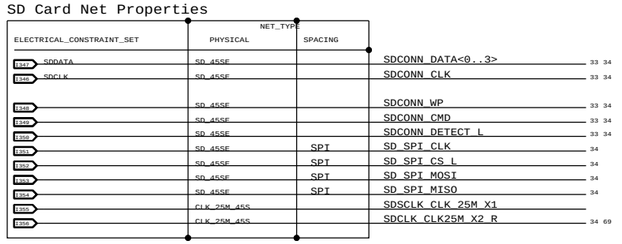
SHEET: 74 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE		

SD Card Net Properties



SYNC_MASTER=CONSTRAINTS SYNC_DATE=09/25/2012

PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 119 OF 121

SHEET 75 OF 76

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Change List:

<RDAR://COMPONENT/508934> J43 HW EE SCHEMATIC | PROTO 0
<RDAR://COMPONENT/508937> J43 HW EE SCHEMATIC | PROTO 1
<RDAR://COMPONENT/508941> J43 HW EE SCHEMATIC | EVT
<RDAR://COMPONENT/508945> J43 HW EE SCHEMATIC | DVT

Kismet:

afp://kismet.apple.com/Kismet-Projects/J41-J43

Useful Wiki Links:

Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

<rdar://component/497591> MobileMac HW | Task
<rdar://component/497587> MobileMac HW | Schematic
<rdar://component/497585> MobileMac HW | New Bugs
<rdar://component/497588> MobileMac HW | Layout
<rdar://component/497590> MobileMac HW | Investigation
<rdar://component/497589> MobileMac HW | Architecture

Other Info:

Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations

SYNC_MASTER=J41_MLB SYNC_DATE=07/03/2012

PAGE TITLE: Reference

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 121 OF 121
SHEET: 76 OF 76

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED