

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0002265654	ENGINEERING RELEASED	2013-08-22

SCHEM, MLB_KEPLER, J45G

8/22/2013 DVT

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0675	1	SCHEM, MLB_KEPLER, J45G	SCH	CRITICAL	
820-3787	1	PCBP, MLB_KEPLER, J45G	PCB	CRITICAL	

DRAWING
 TITLE=MLB
 ABBREV=ABBREV
 PART_MODIFIED=THU Aug 22 12:19:14 2013

DRAWING TITLE		SCHEM, MLB, KEPLER, J45G	
Apple Inc.	DRAWING NUMBER	051-0675	SIZE D
	REVISION	6.0.0	
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BOM Variants

Table with columns: BOM NUMBER, BOM NAME, BOM OPTIONS. Lists variants for J45G_COMMON, J45G_DEVEL:DVT, and various CPU_CRW, CPU_CTO, MICRON, and HYNIX options.

J45G BOM Groups

Table with columns: BOM GROUP, BOM OPTIONS. Lists groups like J45G_COMMON, J45G_COMMON1, J45G_COMMON2, J45G_PVT, J45G_PROGPARTS, J45G_DEVEL:ENG, J45G_DEVEL:DVT, GFX_BM, and XDP_DEBUG.

Module Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists various ICs, SDRAM, and GPUs with their quantities and criticality.

DRAM SPD Straps

Table with columns: BOM GROUP, BOM OPTIONS. Lists memory configurations for RAM: 2Gb_HYNIX_1600, RAM: 2Gb_SAMSUNG_1600, RAM: 2Gb_ELPIDA_1600, RAM: 2Gb_MICRON_1600, RAM: 4Gb_HYNIX_1600_S, RAM: 4Gb_SAMSUNG_1600_S, RAM: 4Gb_ELPIDA_1600_S, RAM: 4Gb_MICRON_1600_S, RAM: 4Gb_HYNIX_1600, RAM: 4Gb_SAMSUNG_1600, RAM: 4Gb_ELPIDA_1600, RAM: 4Gb_MICRON_1600.

Development/Base BOM

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists development and base BOM items.

BOM Configuration metadata including SYNC MASTER, SYNC DATE, Apple Inc. logo, drawing number (051-0675), revision (6.0.0), and page information (2 OF 119).

D C B A

D C B A

Programmables - All builds

341S3920	1	IC,EEPROM,FALCON RIDGE (V13.1),J44/J45	U2890	CRITICAL	TBTROM:PROG
335S0915	1	EEPROM,SPI FLASH ROM,4Mbit,50MHZ,US088	U2890	CRITICAL	TBTROM:BLANK
335S0852	1	IC,GPUROM,D2,BLANK	U9101	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C,(RENEASAS) V3.2.8,DVB,D2	U9600	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9600	CRITICAL	DPMUXMCU:BLANK
341S3856	1	IC,TRKPD/KYBD CNTRLR,CU only,V225,J45	U4801	CRITICAL	TPAD_PSOC:PROG
337S4587	1	IC,TP PSOC,QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK

SMC

338S1214	1	IC,SMC-A3,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3901	1	IC,SMC-B1,SCPL,EXT,V2.16Q13,PROTO4,J45G	U5000	CRITICAL	SMC_PROG:PROTO4
341S3741	1	IC,SMC-A3,SCPL,EXT,VX3XX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT


EFI ROM

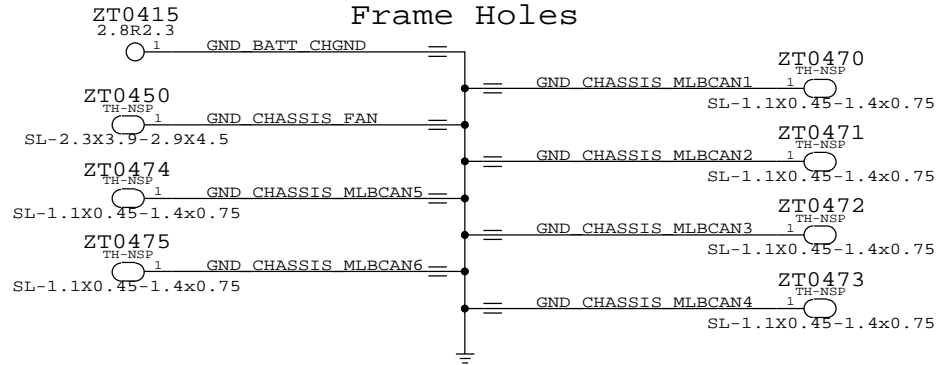
335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SDP,FUSE,L	U6100	CRITICAL	BOOTROM_PROG:BLANK
335S0812	1	64MBIT SPI SRL DUAL I/O FLSH,SOIC8,Z	U6100	CRITICAL	BOOTROM_PROG:BLANK2
341S3712	1	IC,EFI ROM(V0008)PROTO 0,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO
341S3742	1	IC,EFI ROM(V0013) PROTO 1,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3890	1	IC,EFI ROM(V0100) PROTO 3-J45 & EVT-J45	U6100	CRITICAL	BOOTROM_PROG:PROTO3
341S3904	1	IC,EFI ROM(V0106) PROTO 4,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO4

Alternate Parts

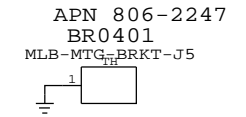
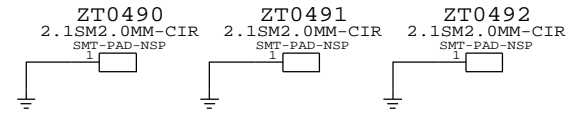
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376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	EPSON alt to NDK
371S0713	371S0558		ALL	DDR alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
376S1032	376S0855		ALL	Tohiba alt to Diodes
376S1129	376S0855		ALL	NEP alt to Diodes
376S1089	376S1128		ALL	NEP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Spida Alt die
138S0803	138S0639		ALL	Samsung Alt to Murata
138S0843	138S0674		ALL	Samsung Alt to Murata
138S0846	138S0811		ALL	Samsung Alt to Murata
127S0164	127S0162		ALL	Rohm Alt to Vishay
138S0732	138S0715		ALL	Rohm Alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HY616 0400
353S3527	353S3528		ALL	Pericom eDP MIX
353S3526	353S3528		ALL	TI eDP MIX
197S0466	197S0464		ALL	EPSON alt to NDK
311S0649	311S0541		ALL	ON alt to Toshiba (U2030,U7000)
197S0479	197S0478		ALL	EPSON alt to NDK

FROM J15

SYNC MASTER=J15 REFERENCE		SYNC DATE=07/31/2012	
BOM Configuration			
 Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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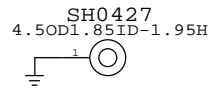


SMT GND TEST POINTS

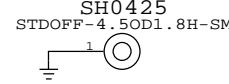


J45 THERMAL MODULE STANDOFF

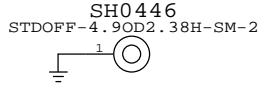
GPU BOSS APN 860-4772



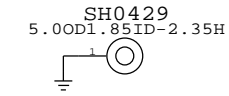
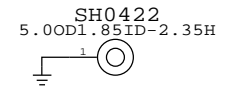
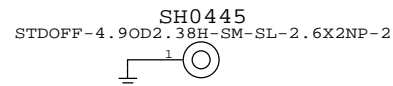
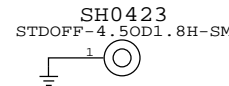
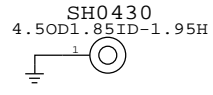
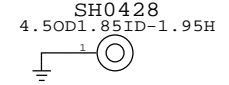
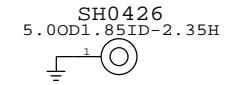
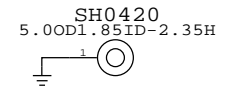
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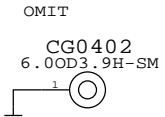
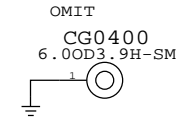
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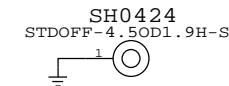
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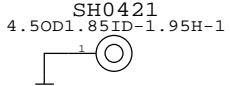
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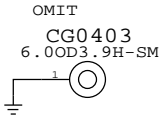
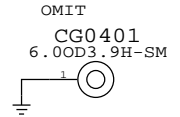


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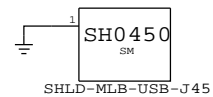


PD parts

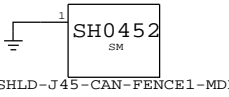
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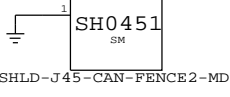
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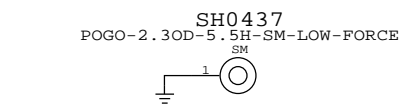
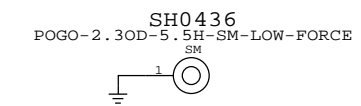
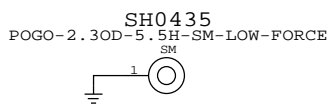
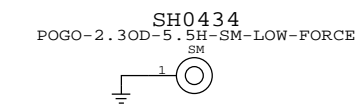
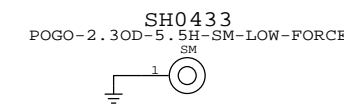
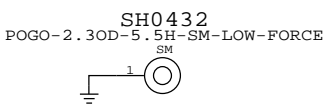
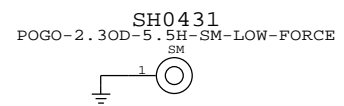


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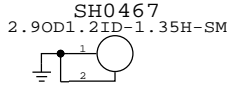
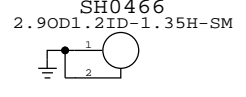
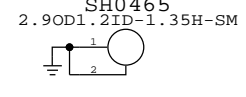
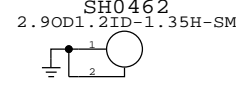
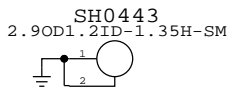
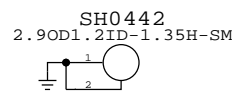
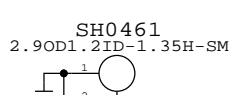
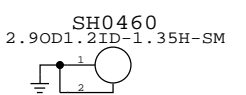
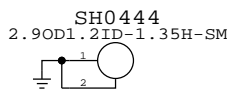
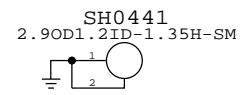
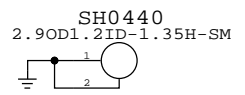
J45 POGO PINS

APN 870-2451



J45 STANDOFF

APN 860-1448



SYNC MASTER=CLEAN J45 SYNC DATE=05/03/2013

PD Parts

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

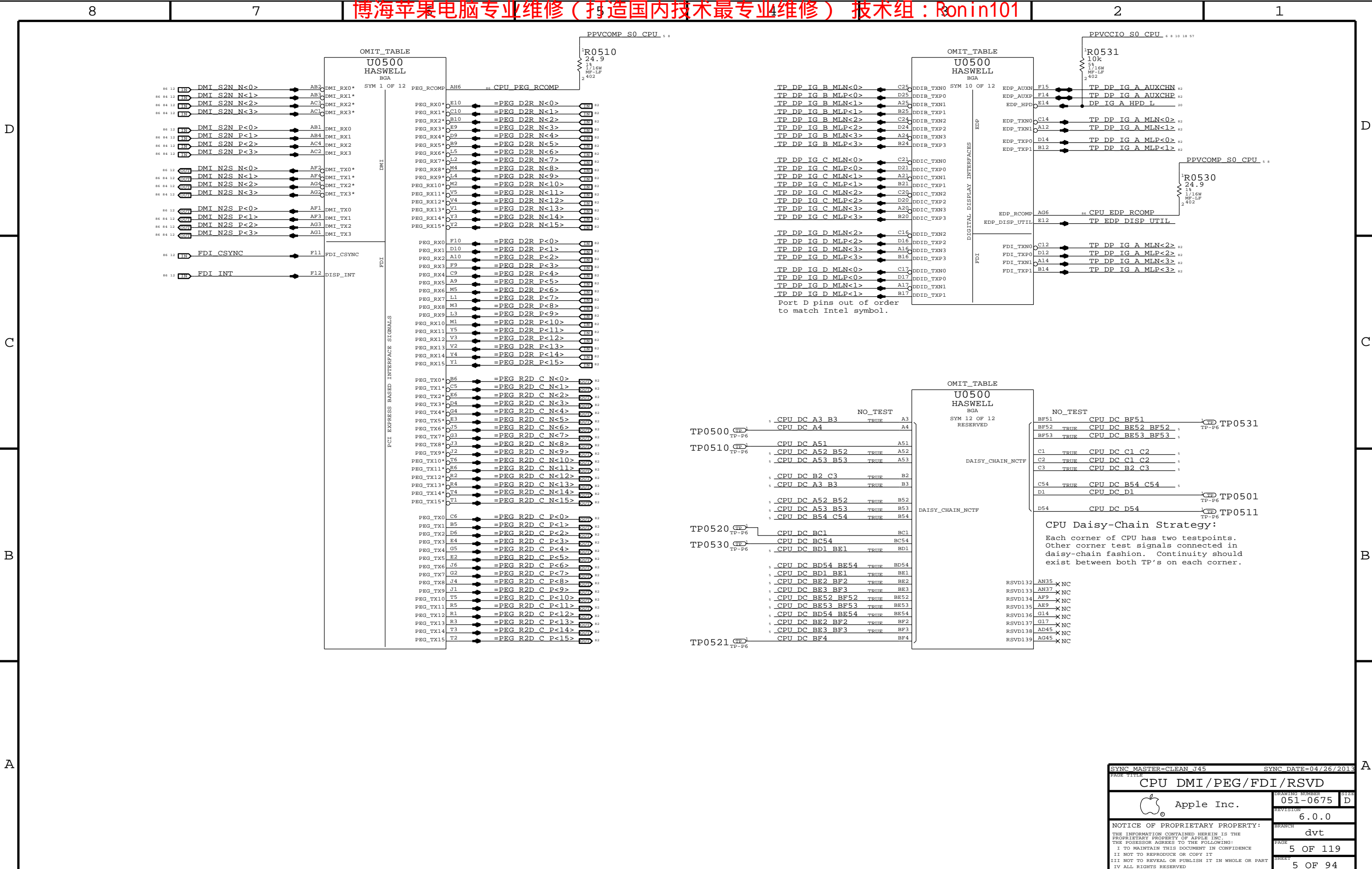
REVISION: 6.0.0

BRANCH: dvt

PAGE: 4 OF 119

SHEET: 4 OF 94

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SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE			
CPU DMI / PEG / FDI / RSVD			
DRAWING NUMBER		SIZE	
051-0675		D	
REVISION		PAGE	
6.0.0		5 OF 119	
BRANCH		SHEET	
dvt		5 OF 94	
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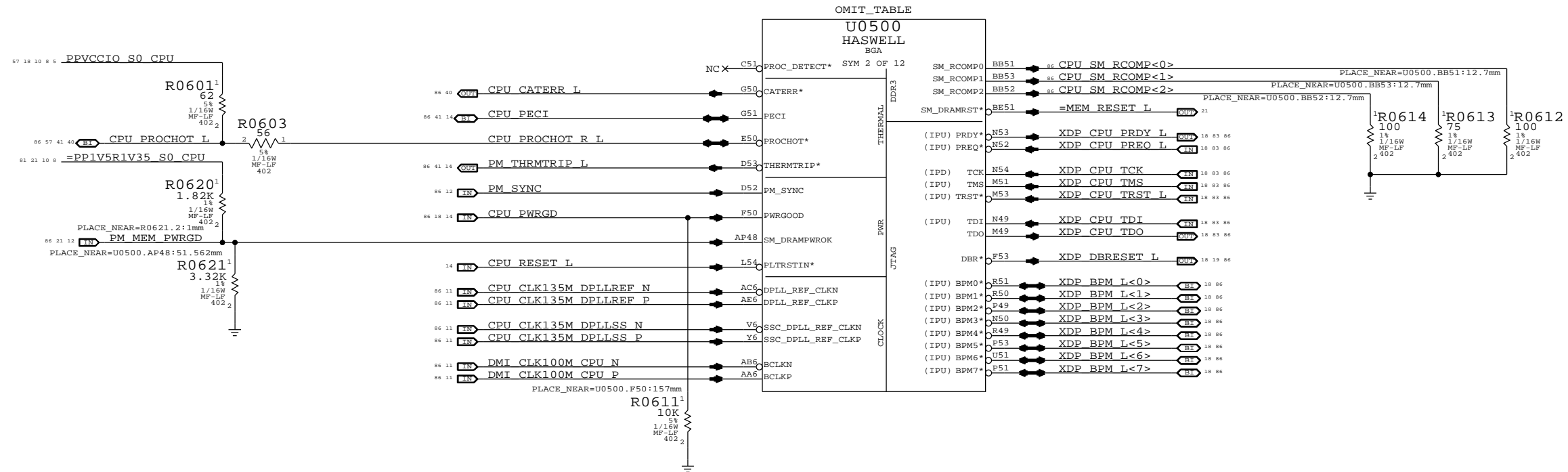
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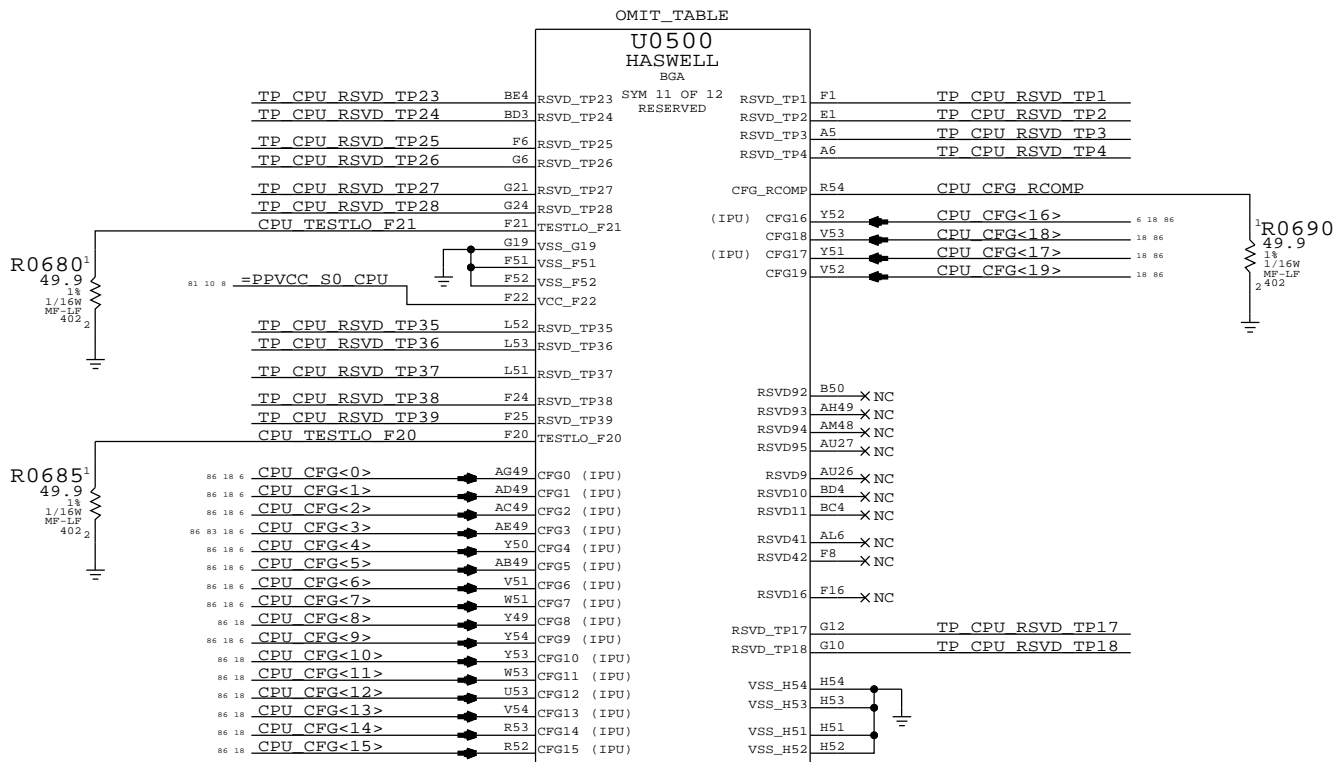
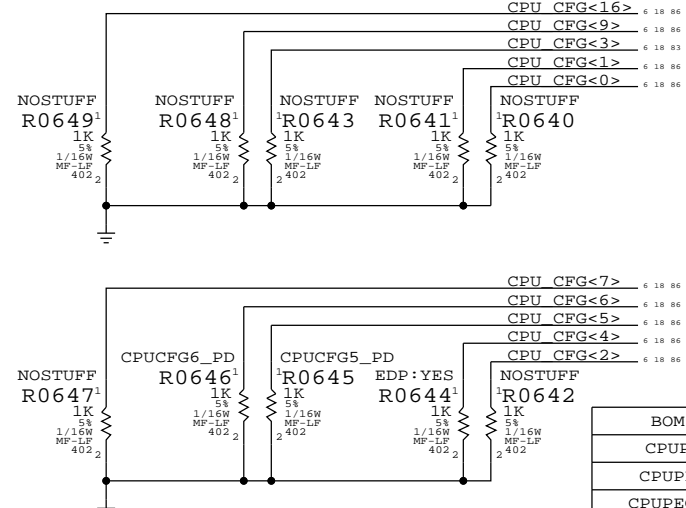
A

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CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER XCRESETB 0 = WAIT FOR BIOS
 CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
 CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
 CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
 CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CUPEG:X16	CPUCFG5_PD
CUPEG:X8X8	CPUCFG6_PD, CPUCFG5_PD
CUPEG:X8X4X4	

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

CPU Clock/Misc/JTAG/CFG

Apple Inc.

051-0675

6.0.0

dvt

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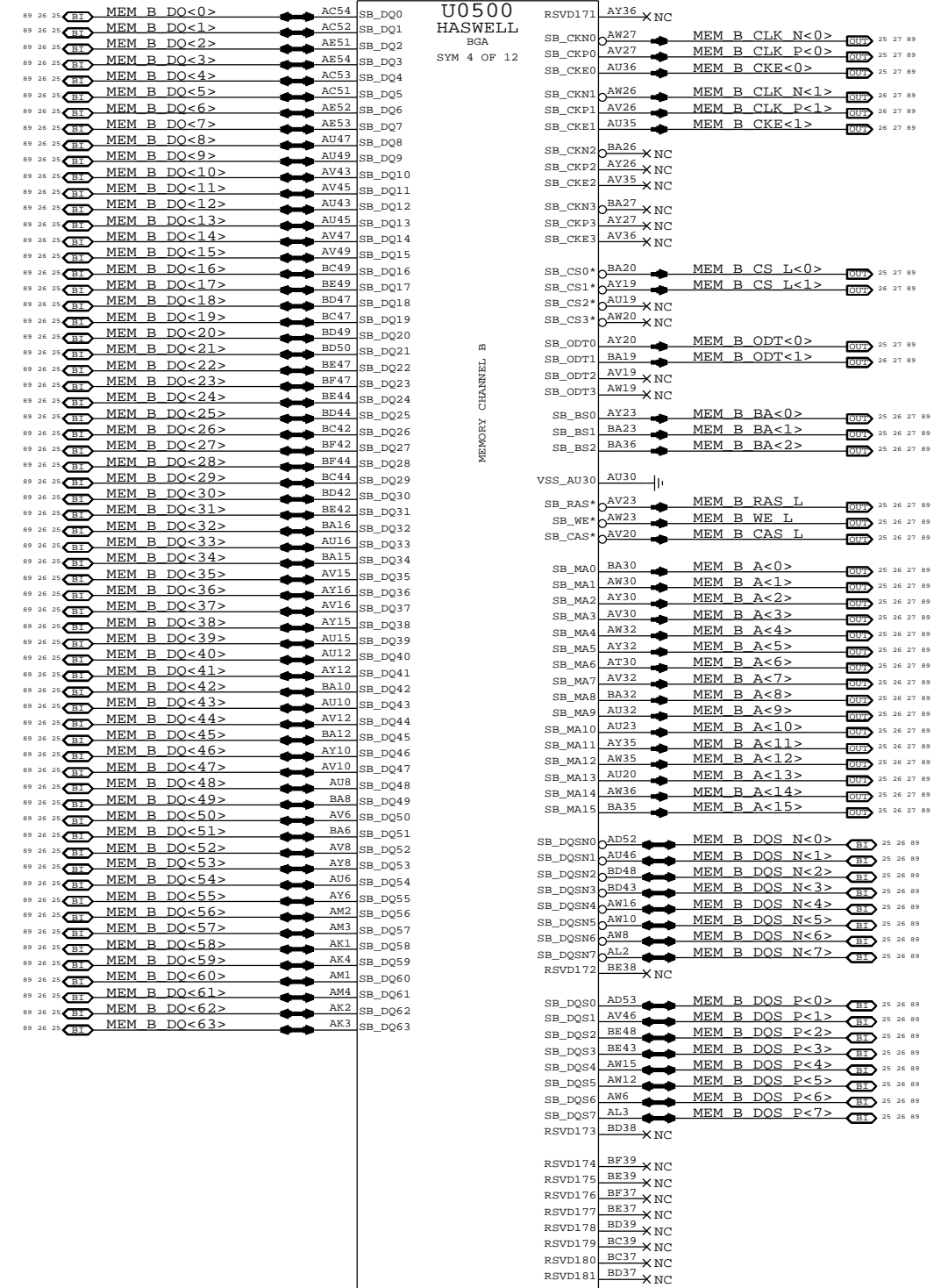
6 OF 94

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OMIT_TABLE



OMIT_TABLE



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

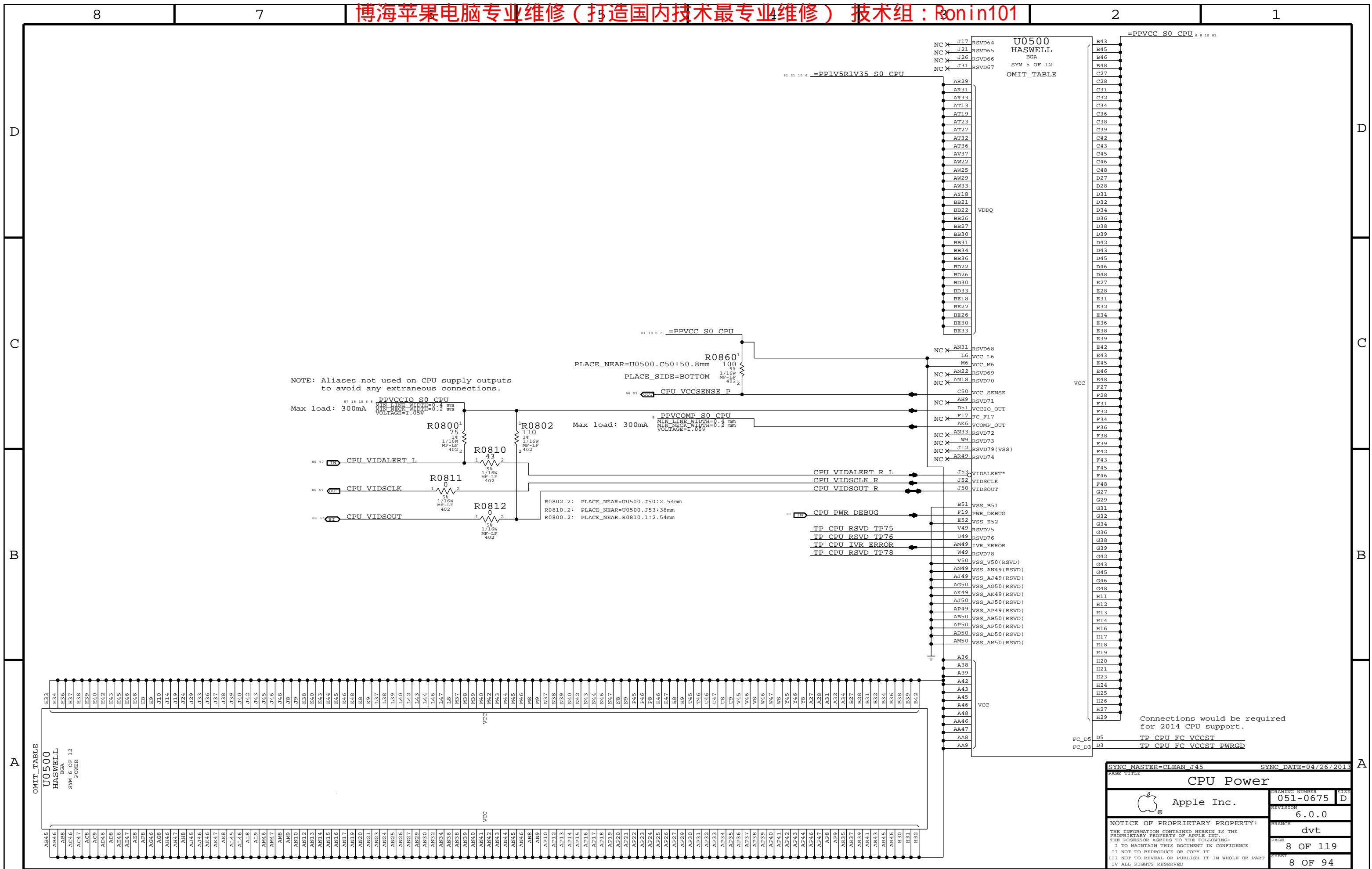
CPU DDR3 Interfaces

Apple Inc.

DRAWING NUMBER: 051-0675
REVISION: 6.0.0

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BRANCH: dvt
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SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
CPU Power			
Apple Inc.		DRAWING NUMBER	SIZE
051-0675		D	
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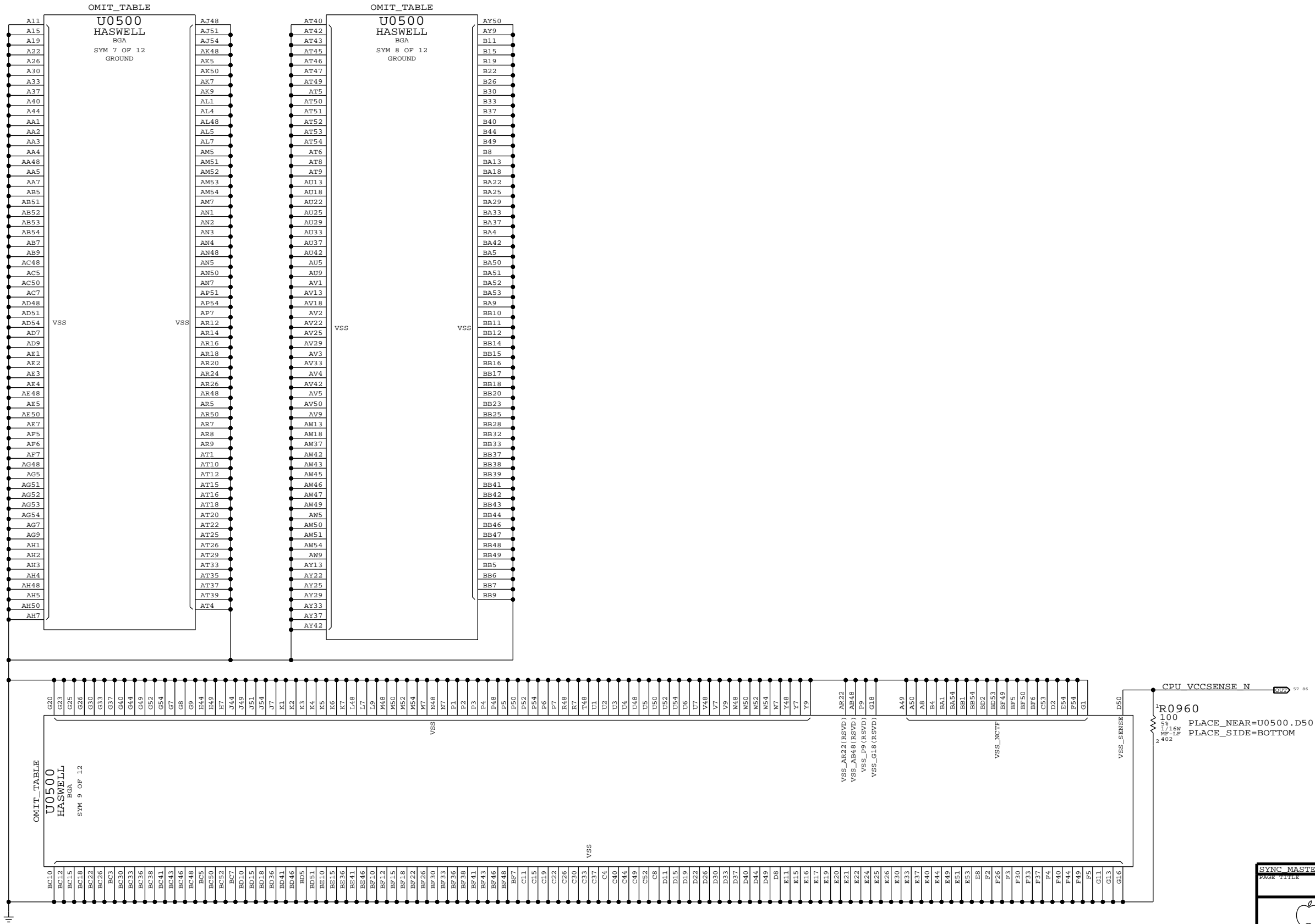
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CPU VCCSENSE N 57 86

R0960
 100
 1/16W
 2402

PLACE_NEAR=U0500.D50:50.8mm
 PLACE_SIDE=BOTTOM

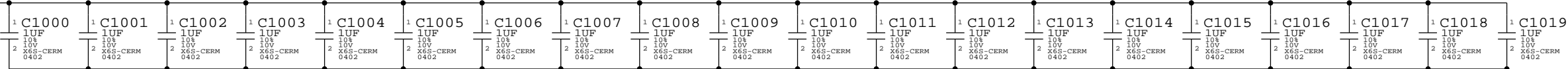
SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
CPU Ground			
Apple Inc.		DRAWING NUMBER	051-0675
NOTICE OF PROPRIETARY PROPERTY: <small>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED</small>		REVISION	6.0.0
		BRANCH	dvt
		PAGE	9 OF 119
		SHEET	9 OF 94

CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge), 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

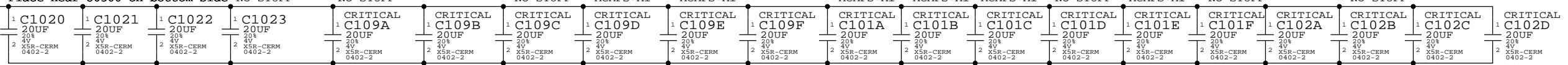
PLACEMENT_NOTE (C1000-C1019):

Place on bottom side of U0500



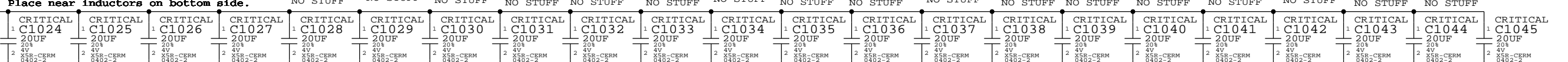
NO STUFF NO STUFF NO STUFF
PLACEMENT_NOTE (C1020-C1023):

Place near U0500 on bottom side



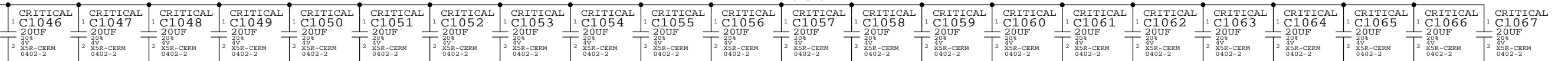
NO STUFF NO STUFF NO STUFF
PLACEMENT_NOTE (C1024-C1045):

Place near inductors on bottom side.



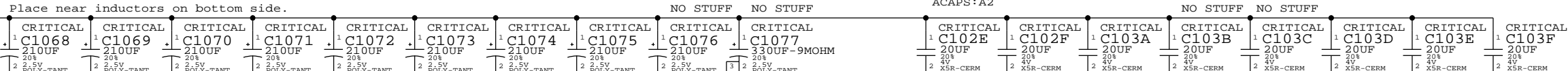
PLACEMENT_NOTE (C1046-C1067):

Place near inductors on bottom side.



NO STUFF NO STUFF NO STUFF
PLACEMENT_NOTE (C1068-C1076):

Place near inductors on bottom side.

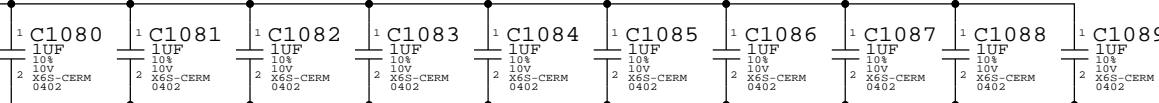


CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

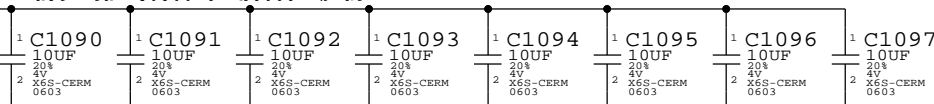
PLACEMENT_NOTE (C1080-C1089):

Place on bottom side of U0500



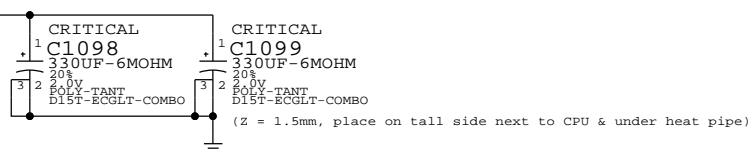
PLACEMENT_NOTE (C1090-C1097):

Place near U0500 on bottom side



PLACEMENT_NOTE (C1098-C1099):

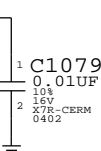
Place near U0500 on bottom side



CPU VCCIO Decoupling

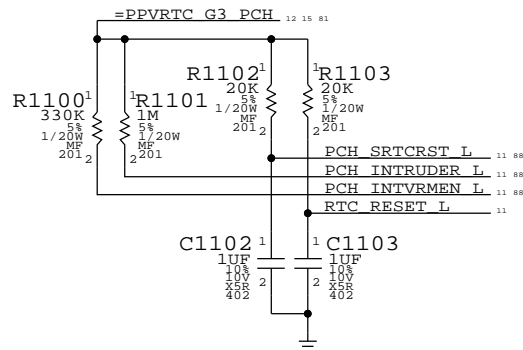
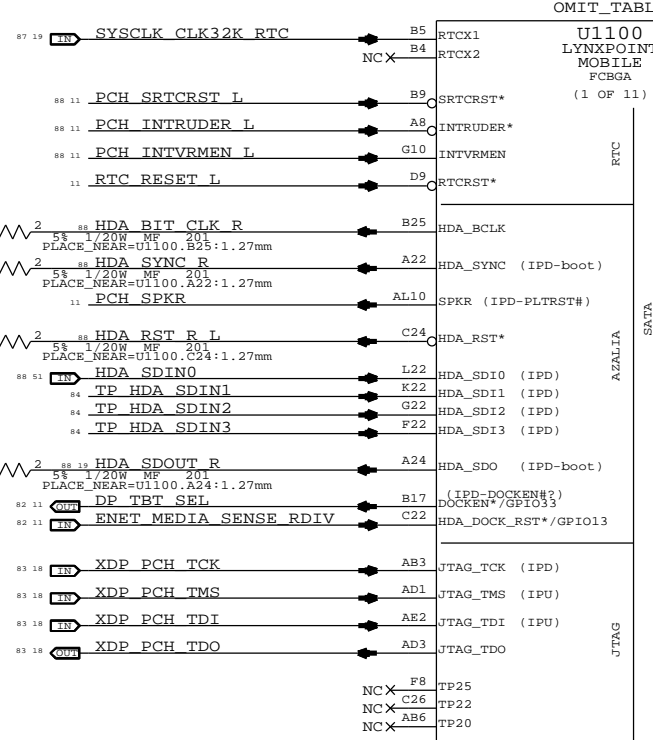
Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

PLACEMENT_NOTE (C1098-C1099):

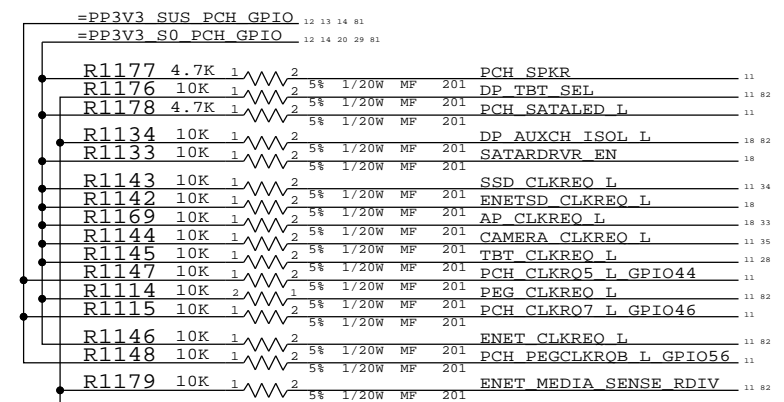


NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

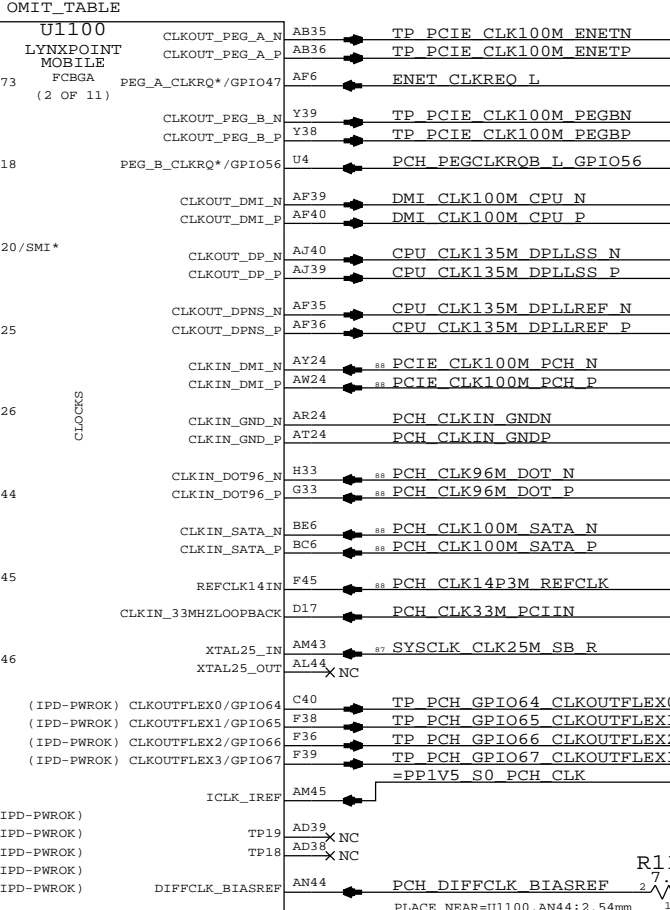
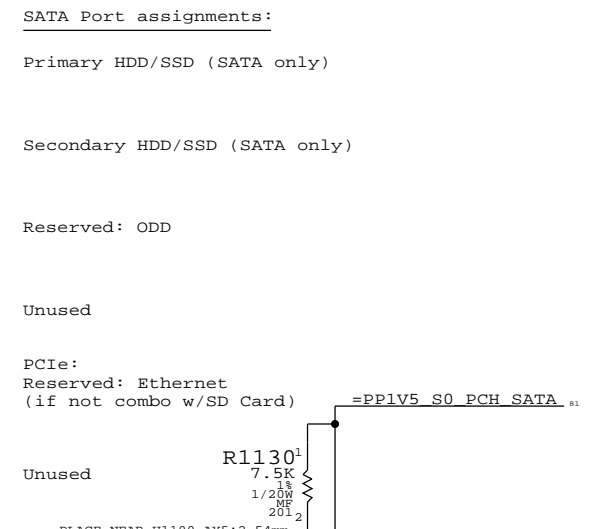
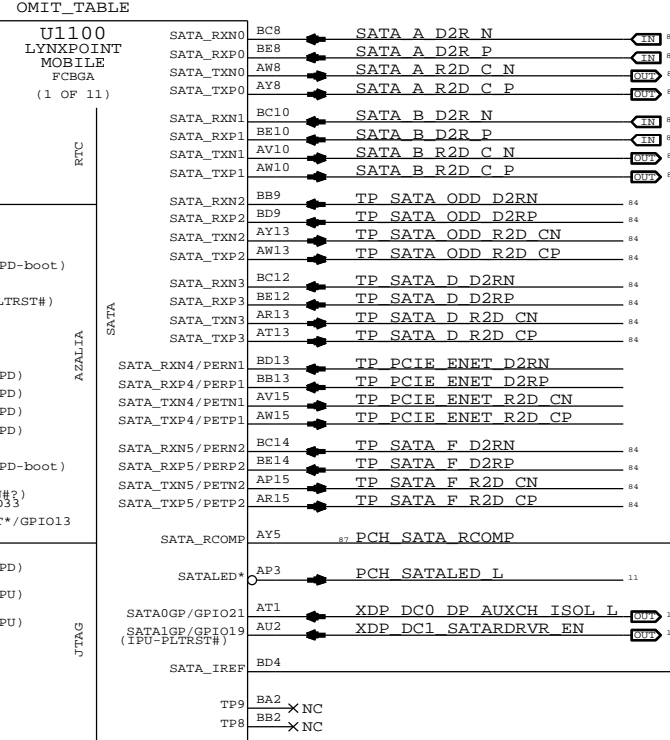
PAGE TITLE		SYNC DATE=05/02/2013	
CPU Decoupling			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	6.0.0
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		PAGE	10 OF 119
		SHEET	10 OF 94



NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks. PEG-attached (CPU) PCIe devices must use one set, while PCH-attached PCIe devices use the other set. If 2 or less devices are attached to PEG the CLKOUT_PEG outputs can be used for those devices.



Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.



NOTE: ENET pair only used if SD Card Reader is USB3.



SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK

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DRAWING NUMBER: 051-0675 SIZE: D

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BRANCH: dvt

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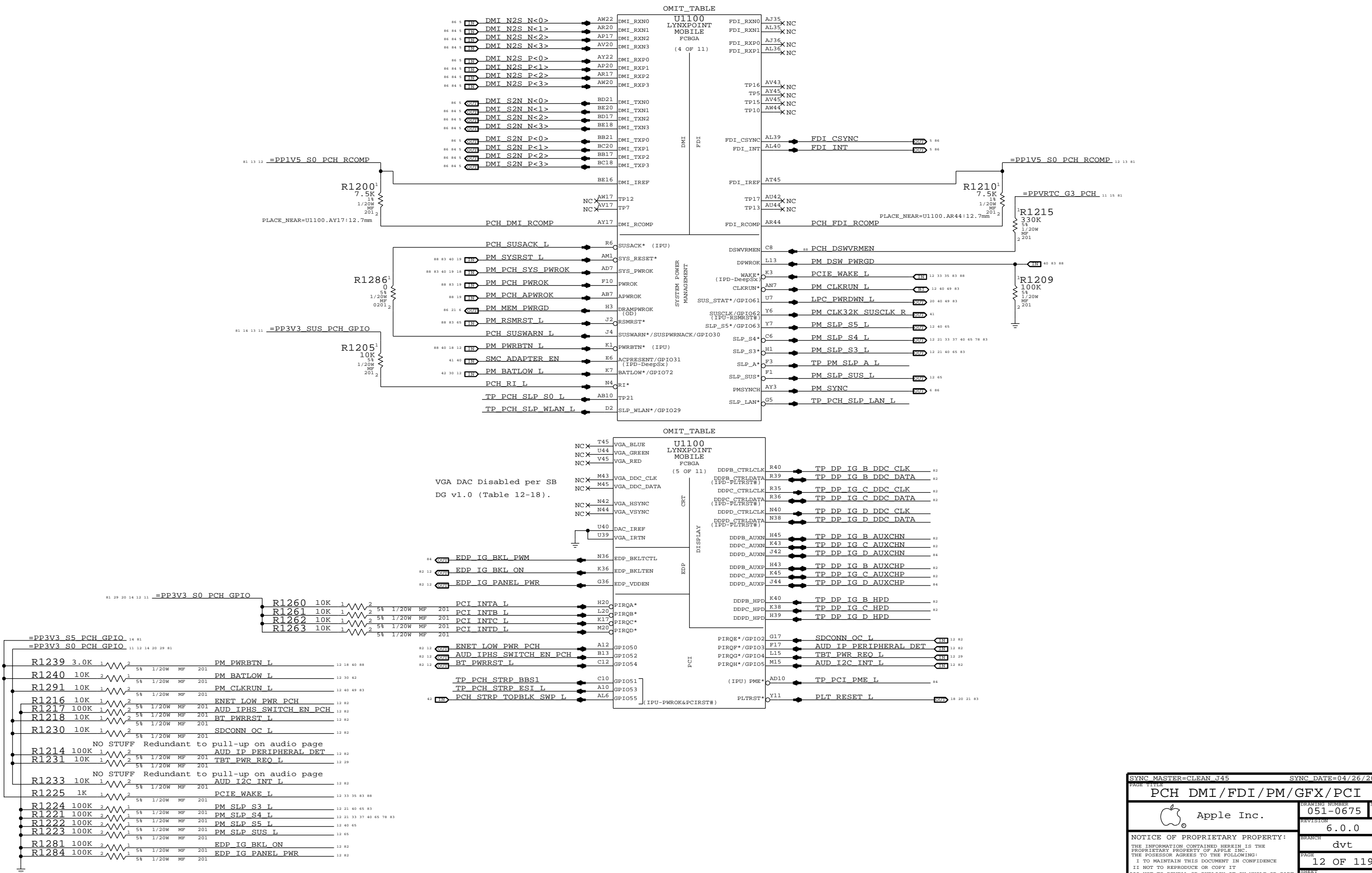
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SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE: PCH DMI / FDI / PM / GFX / PCI

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USB3 Port Assignments:

Unused

PCIe/USB3 Port Assignments:

SD Card Reader (& Ethernet if combo)

PCIe Port Assignments:

AirPort

Camera

SSD (Gumstick) Lane 0 (PCIe-only) Or PCIe switch if TBT/SSD

SSD (Gumstick) Lane 1 (PCIe-only) Or PCIe switch if TBT/SSD

SSD (Gumstick) Lane 2 (PCIe-only) Or PCIe switch if TBT/SSD

SSD (Gumstick) Lane 3 (PCIe-only) Or PCIe switch if TBT/SSD

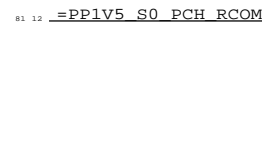
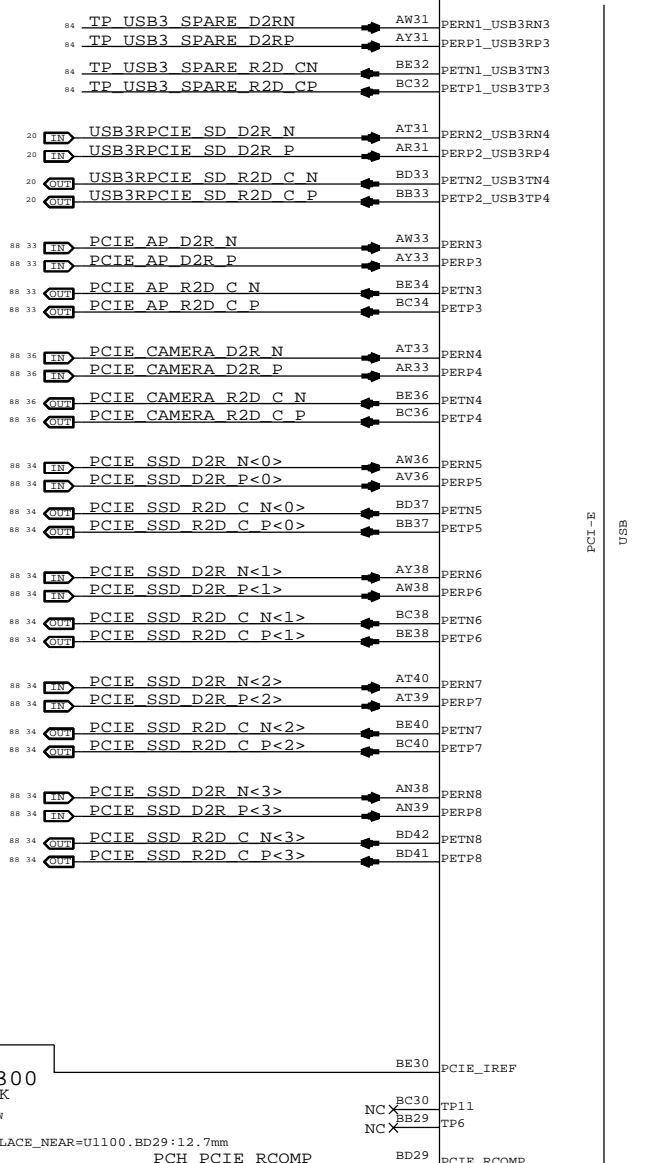


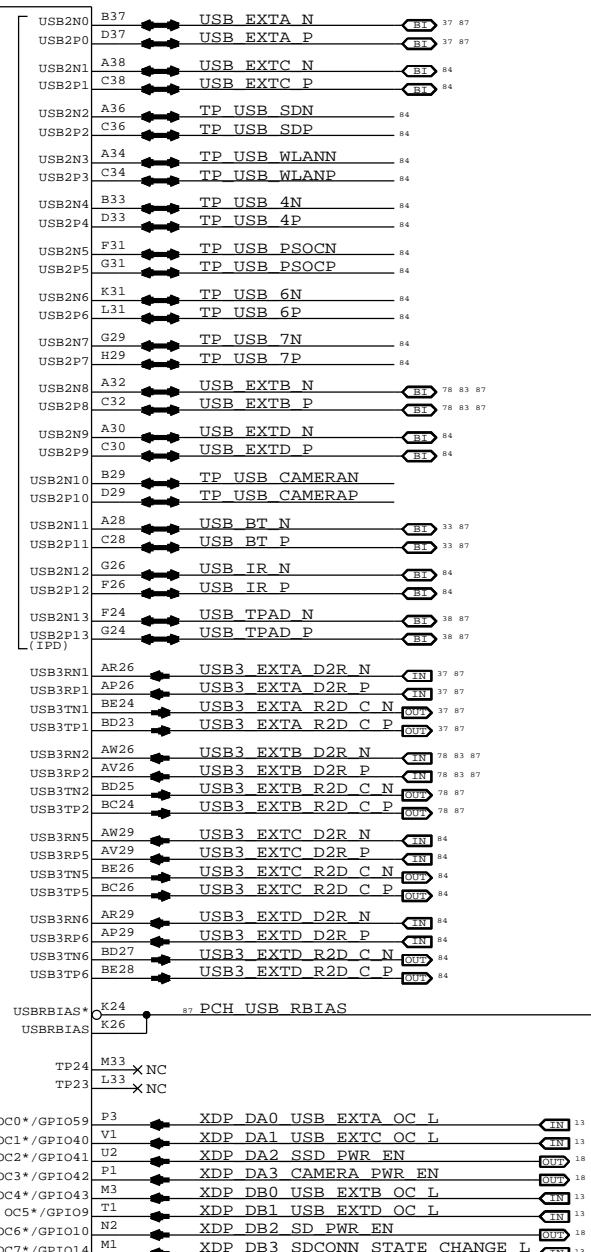
Table listing LPC AD R<0> through R<3> and LPC FRAME L components with their pin numbers and values.

Table listing various components like R1350, R1351, R1360, R1361, R1362, R1368, R1320, R1321, R1367, R1369, R1392, R1393, R1353, R1354, R1355 with their values and functions.



OMIT_TABLE

U1100 LYNXPPOINT MOBILE FCBGA (9 OF 11)



USB Port Assignments:

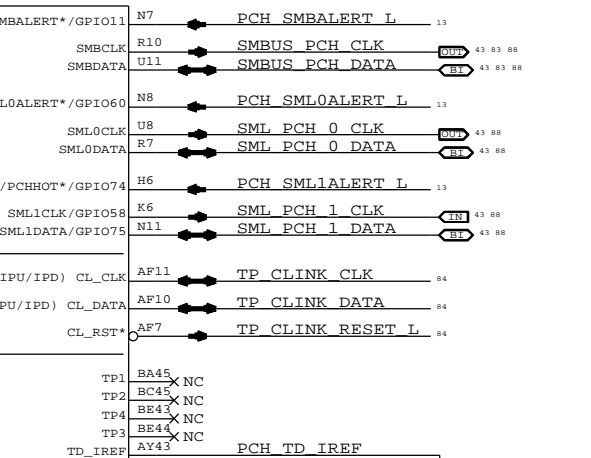
- List of USB port assignments including Ext A (LS/FS/HS), Ext C (LS/FS/HS), Reserved: SD (HS), Reserved: WiFi (HS), Unused, Reserved: PSOC (Legacy Trackpad), Unused, Reserved: Camera, BT, IR, Trackpad.

USB3 Port Assignments:

- List of USB3 port assignments including Ext A (SS), Ext B (SS), Ext C (SS), Ext D (SS).

OMIT_TABLE

U1100 LYNXPPOINT MOBILE FCBGA (3 OF 11)



Technical drawing header and footer containing Apple Inc. logo, drawing number 051-0675, revision 6.0.0, and page information (13 OF 119).

Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

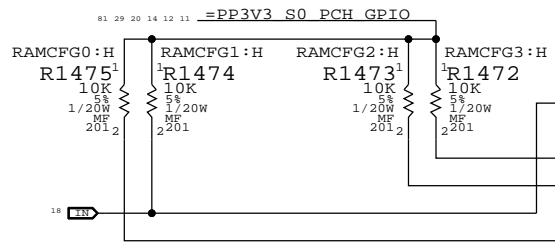
Pin	Signal	Pin	Signal
20	TBT_CIO_PLUG_EVENT_ISOL	AT8	BMBUSY*/GPIO0
82 14	FW PME L	F13	TACH1/GPIO1
82 79 14	DPMUX_UC_IRO	A14	TACH2/GPIO6
40 14	SMC_RUNTIME_SCI_L	G15	TACH3/GPIO7
10	XDP_FC0_HDD_PWR_EN	Y1	GPIO8 (IPU-RSMRST#)
82 14	WOL_EN	K13	LAN_PHY_PWR_CTRL/GPIO12
82 14	MEM_VDD_SEL_1V5_L	AB11	GPIO15
18 14	XDP_DDO_SSD_PCIE_SEL_L	AN2	SATA4GP/GPIO16 (IPU-Boot/SATA4GP?)
83 49 14	LPCPLUS_GPIO	C14	TACH0/GPIO17
20 14	JTAG_TBT_TMS_PCH	BB4	SCLOCK/GPIO22
82 14	TBT_GO2SX_BIDIR	Y10	GPIO24
40 14	SMC_WAKE_SCI_L	R11	GPIO27 (IPU-DeepSx)
21	ISOLATE_CPU_MEM_L	AD11	GPIO28
29	TBT_POC_RESET_L	AN6	GPIO34
18	XDP_FC1_GPU_GOOD	AP1	GPIO35/NMI*
18	XDP_DC2_ODD_PWR_EN_L	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)
18	XDP_DC3_JTAG_ISP_TCK	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)
20 14	JTAG_ISP_TDO	AT7	SLOAD/GPIO38
20 14	JTAG_ISP_TDI	AM3	SDATAOUT0/GPIO39
82 14	FW_PWR_EN_PCH	AN4	SDATAOUT1/GPIO48
83 49 14	XDP_DD1_MLB_RAMCFG1	AK3	SATA5GP/GPIO49 (IPU-Boot/SATA5GP?)
20 14	SPIROM_USE_MLB	U12	GPIO57
20 14	MLB_RAMCFG3	C16	TACH4/GPIO68
20 14	MLB_RAMCFG2	D13	TACH5/GPIO69
20 14	SD_SEL_PCIE_L_USB_H	G13	TACH6/GPIO70 (IPU-Boot?)
20 14	MLB_RAMCFG0	H15	TACH7/GPIO71 (IPU-Boot?)

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(6 OF 11)

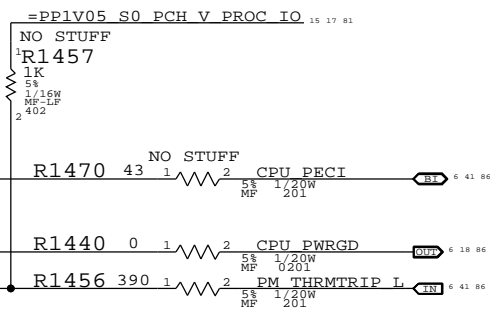
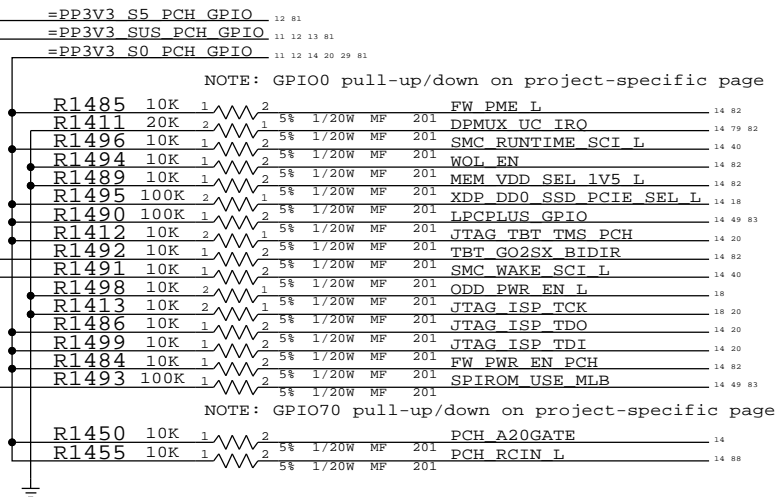
CPU/MISC

GPIO



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.



SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PAGE TITLE: PCH GPIO/MISC/NCTF

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DRAWING NUMBER: 051-0675

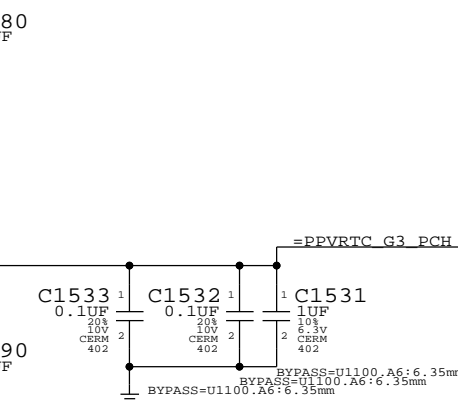
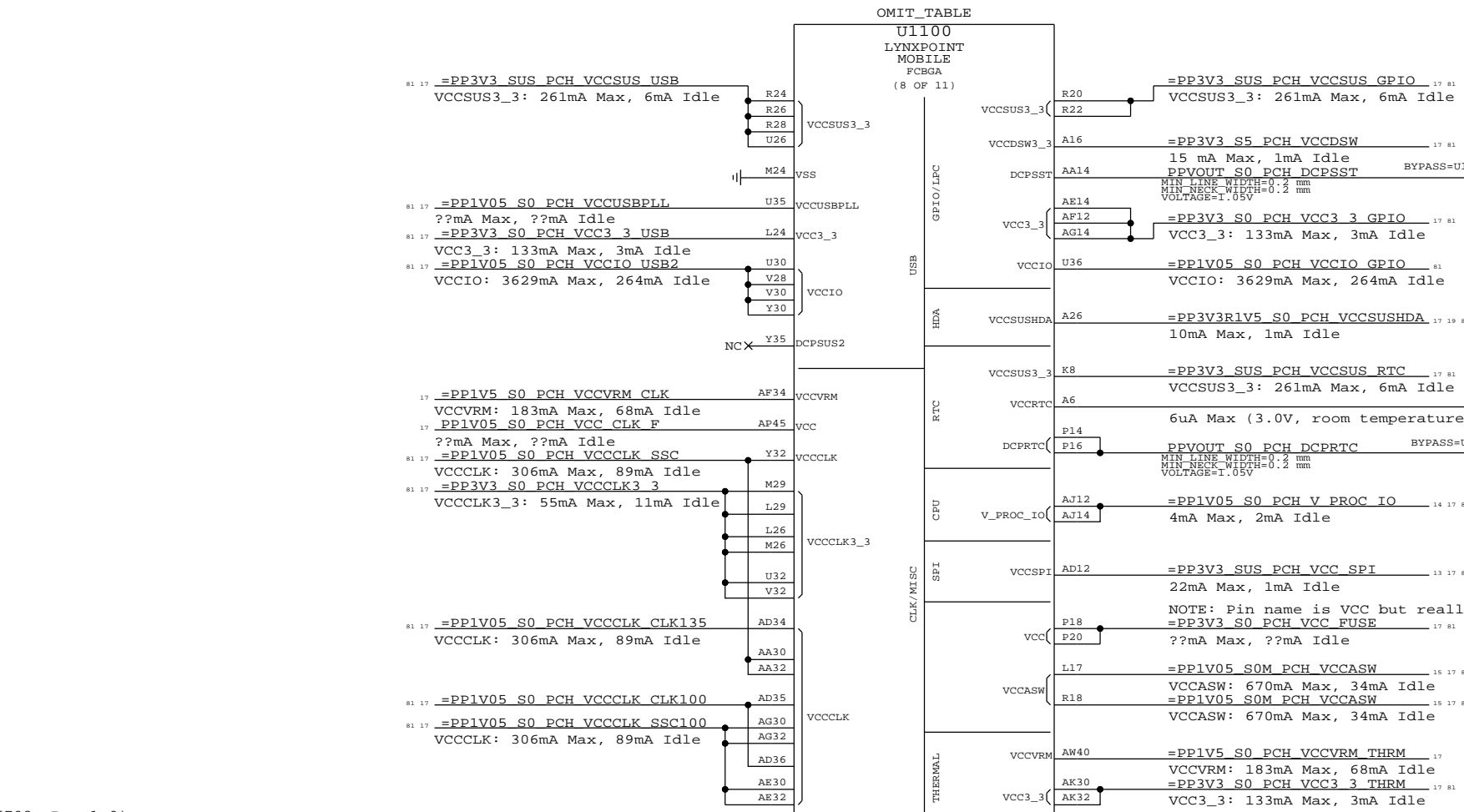
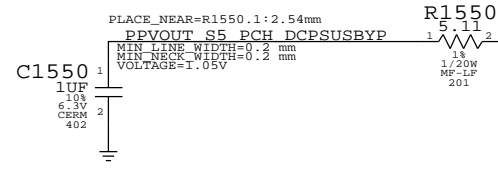
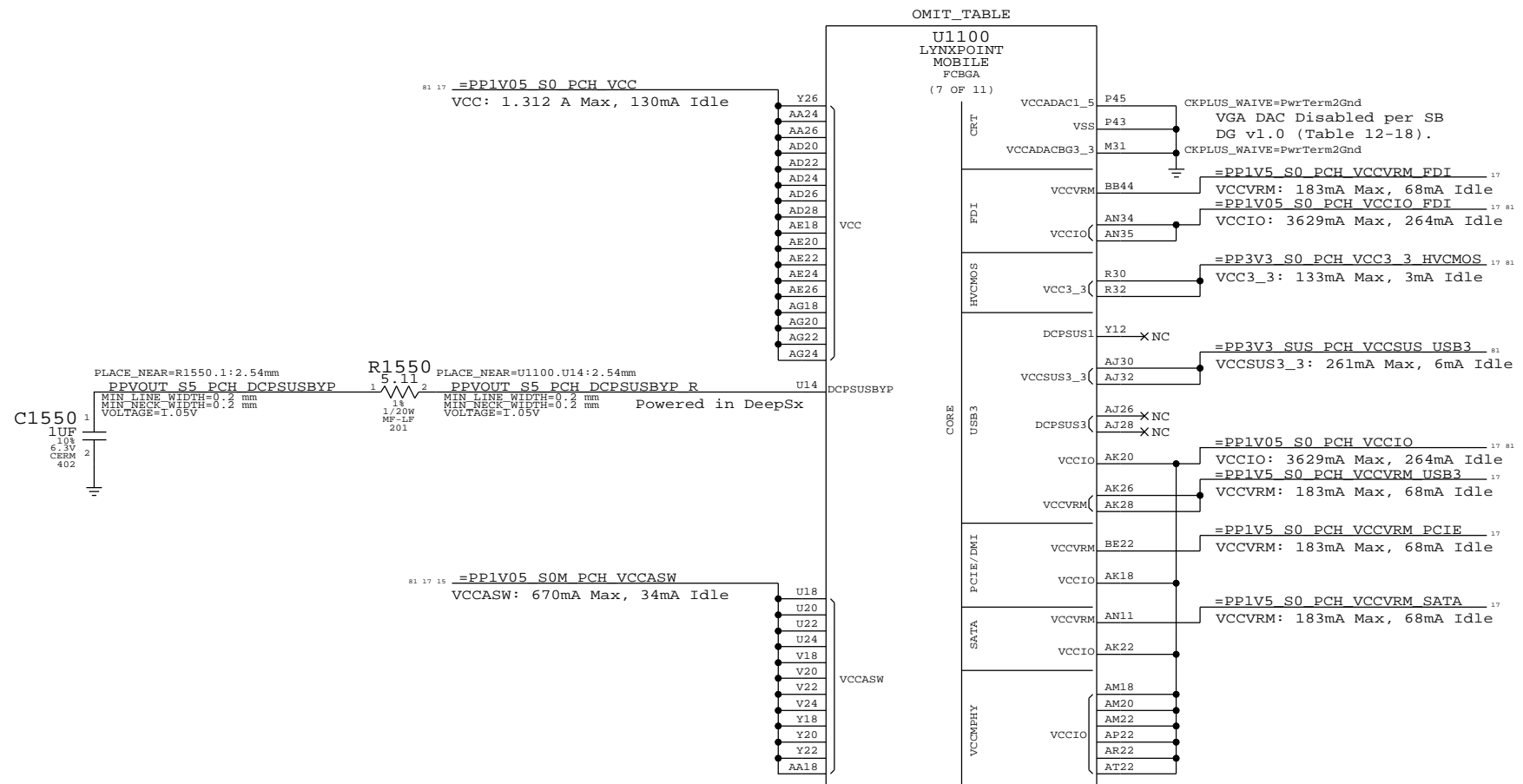
REVISION: 6.0.0

BRANCH: dvt

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SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PAGE TITLE: PCH Power

Apple Inc. DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

PAGE: 15 OF 119

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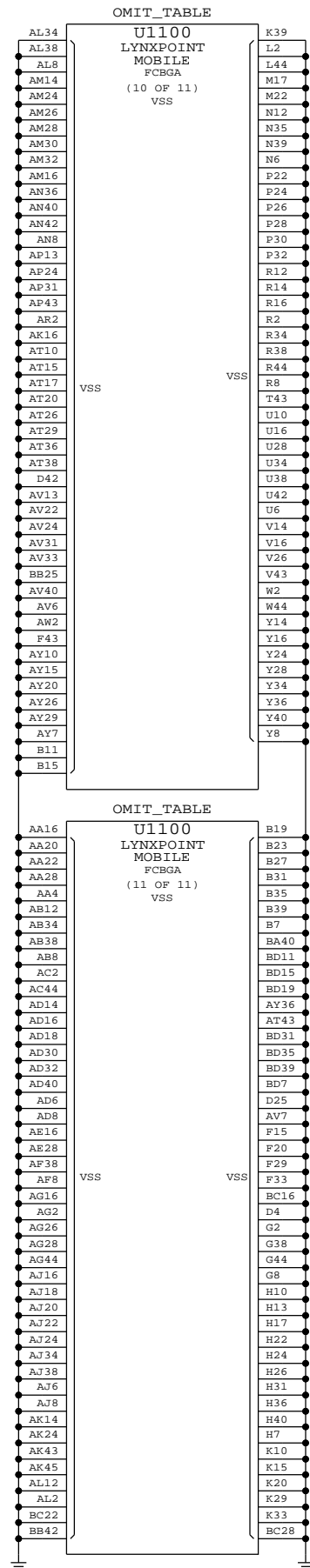
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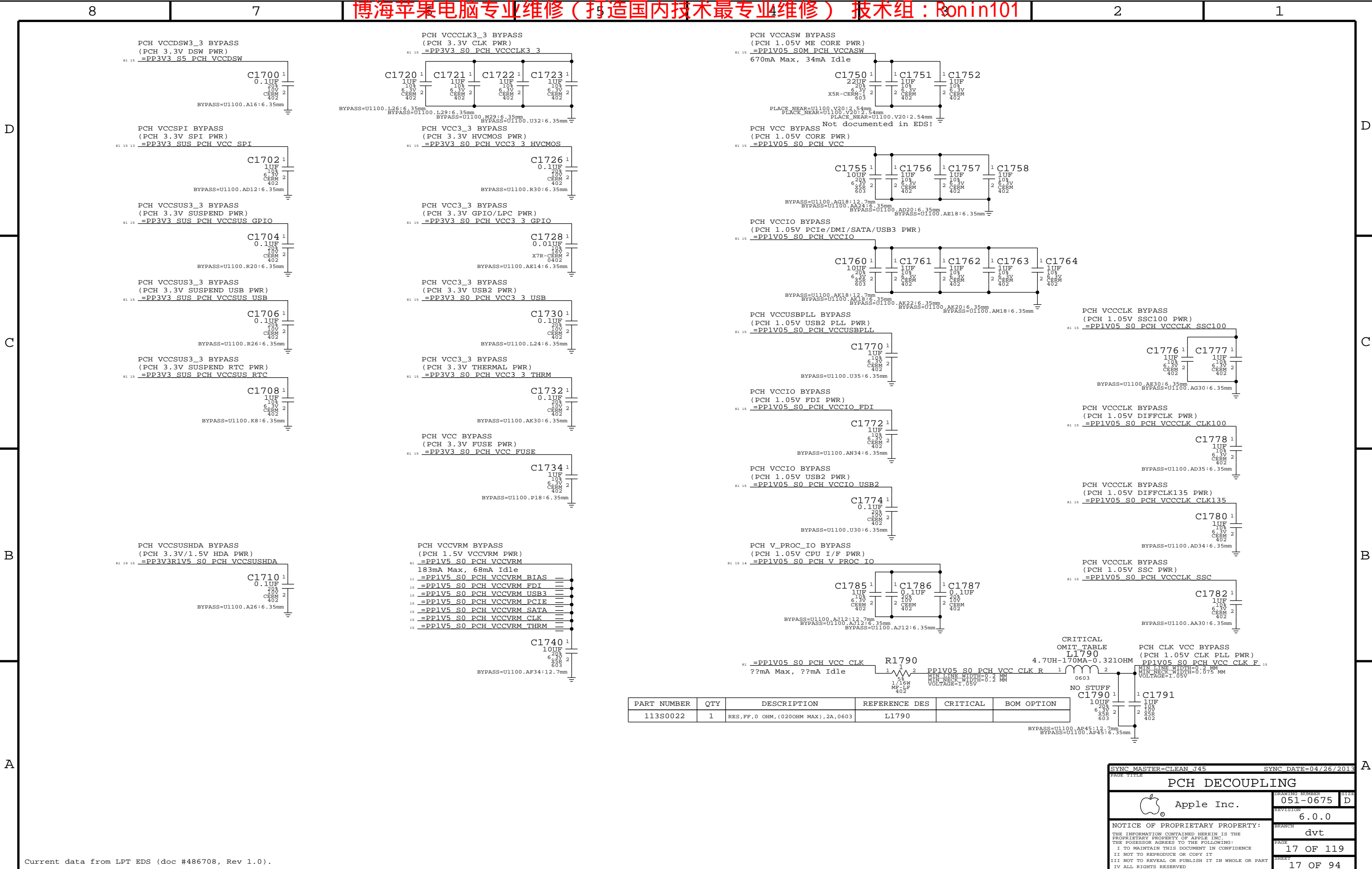
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SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PCH Grounds			
 Apple Inc.	DRAWING NUMBER	051-0675	SIZE D
	REVISION	6.0.0	
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	SHEET	16 OF 94	



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PCH DECOUPLING

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

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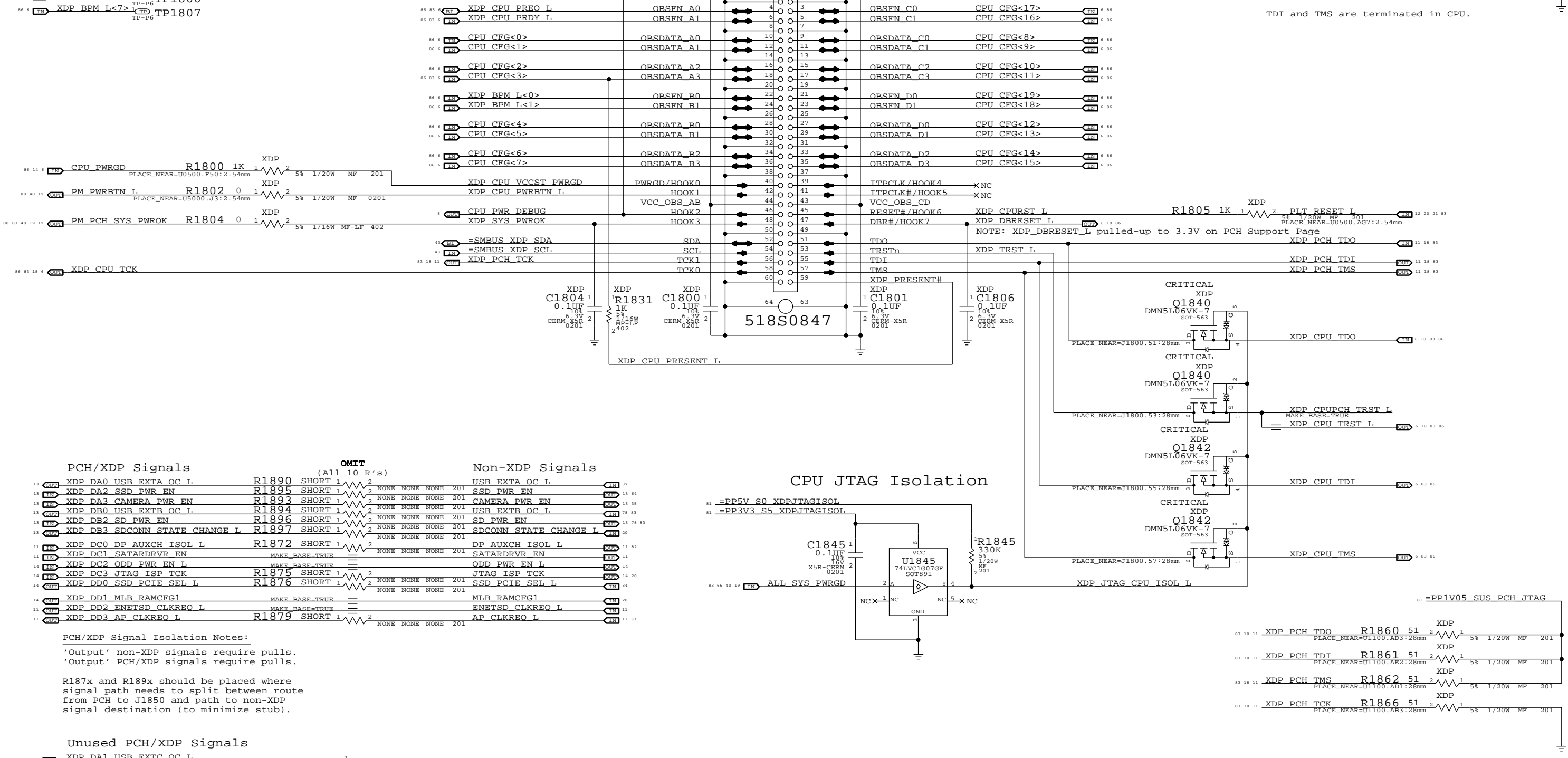
SHEET: 17 OF 94

Extra BPM Testpoints

- XDP_BPM_L<2> TP1802
- XDP_BPM_L<3> TP1803
- XDP_BPM_L<4> TP1804
- XDP_BPM_L<5> TP1805
- XDP_BPM_L<6> TP1806
- XDP_BPM_L<7> TP1807

Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.



PCH/XDP Signals

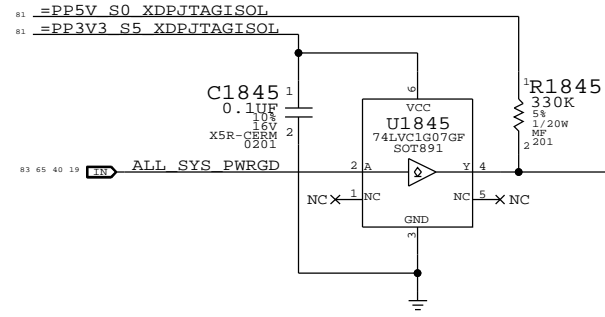
Signal	Component	Notes	Destination
XDP_DA0 USB EXTA OC L	R1890	SHORT 1	201
XDP_DA2 SSD PWR EN	R1895	SHORT 1	201
XDP_DA3 CAMERA PWR EN	R1893	SHORT 1	201
XDP_DB0 USB EXTB OC L	R1894	SHORT 1	201
XDP_DB2 SD PWR EN	R1896	SHORT 1	201
XDP_DB3 SDCONN STATE CHANGE L	R1897	SHORT 1	201
XDP_DC0 DP AUXCH ISOL L	R1872	SHORT 1	201
XDP_DC1 SATARDVR EN	MAKE_BASE=TRUE		201
XDP_DC2 ODD PWR EN L	MAKE_BASE=TRUE		201
XDP_DC3 JTAG ISP TCK	R1875	SHORT 1	201
XDP_DD0 SSD PCIE SEL L	R1876	SHORT 1	201
XDP_DD1 MLB RAMCFG1	MAKE_BASE=TRUE		201
XDP_DD2 ENETSD CLKREQ L	MAKE_BASE=TRUE		201
XDP_DD3 AP CLKREQ L	R1879	SHORT 1	201

PCH/XDP Signal Isolation Notes:
 'Output' non-XDP signals require pulls.
 'Output' PCH/XDP signals require pulls.
 R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

- XDP_DA1 USB EXTC OC L TP1810
- XDP_DB1 USB EXTD OC L TP1811
- XDP_FC0 HDD PWR EN TP1812
- XDP_FC1 GPU GOOD TP1813

CPU JTAG Isolation



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

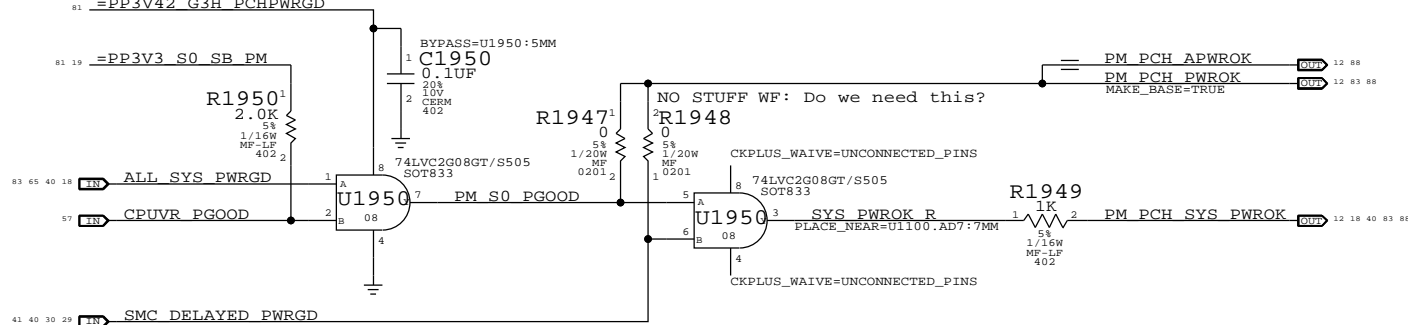
CPU & PCH XDP

Apple Inc.

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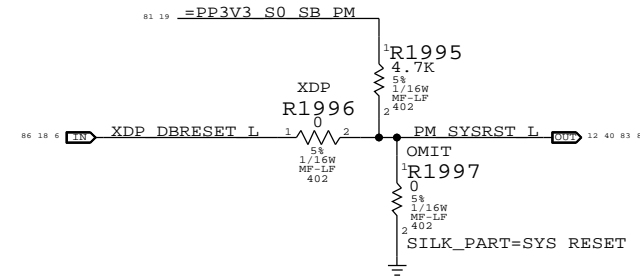
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PCH PWROK Generation



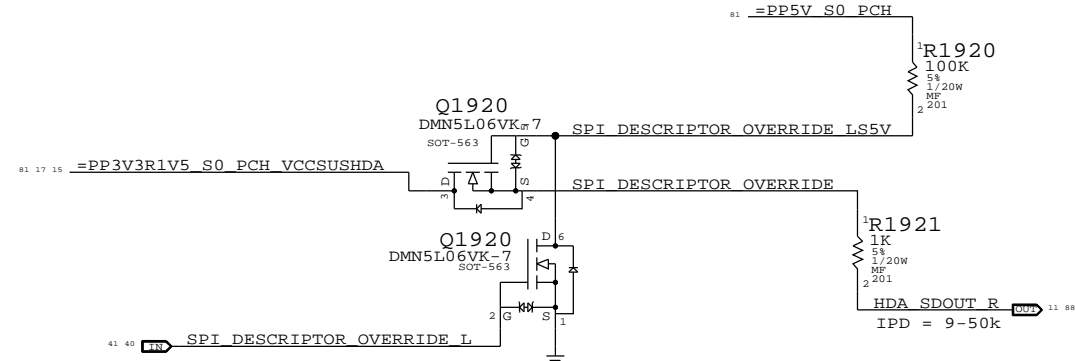
NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

PCH Reset Button

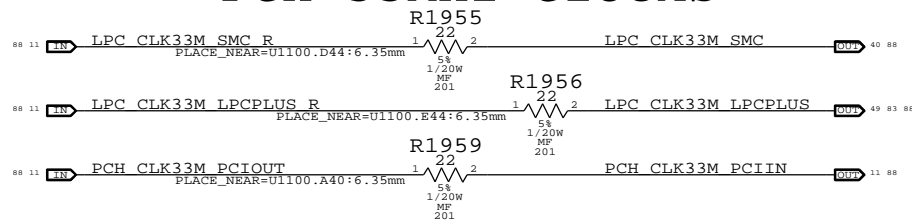


PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



PCH 33MHz Clocks

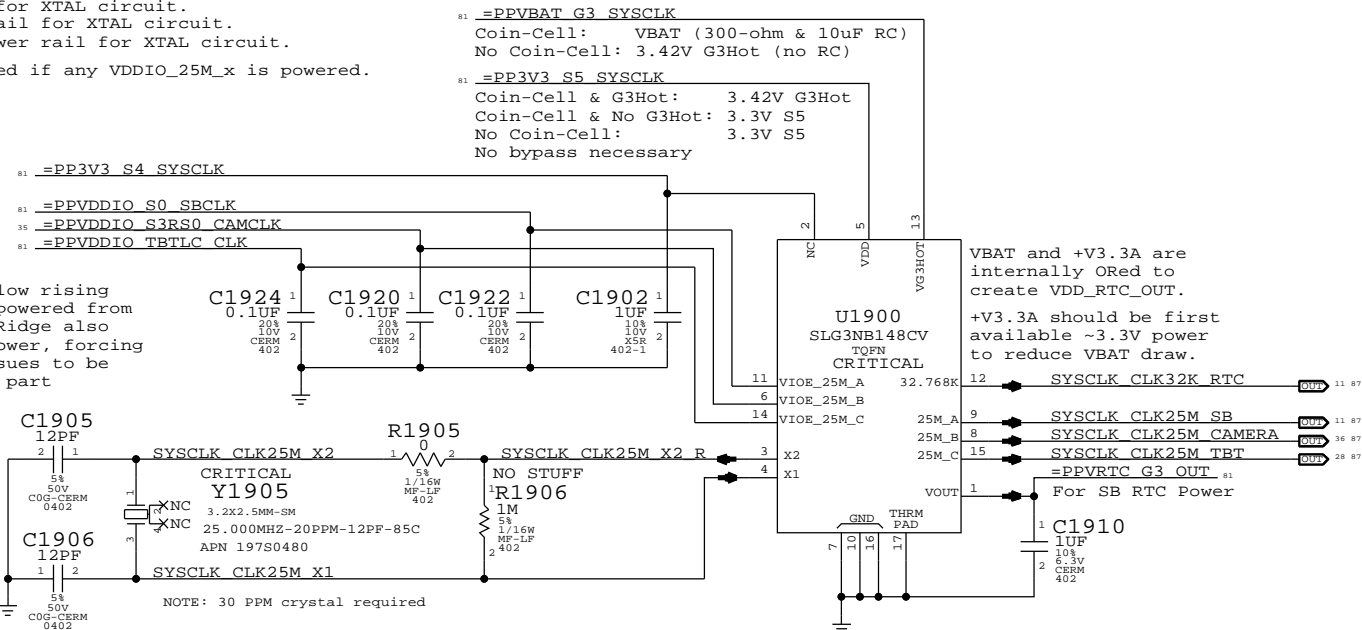


System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

GreenClk 25MHz Power
SB XTAL Power
Camera XTAL Power
TBT XTAL Power

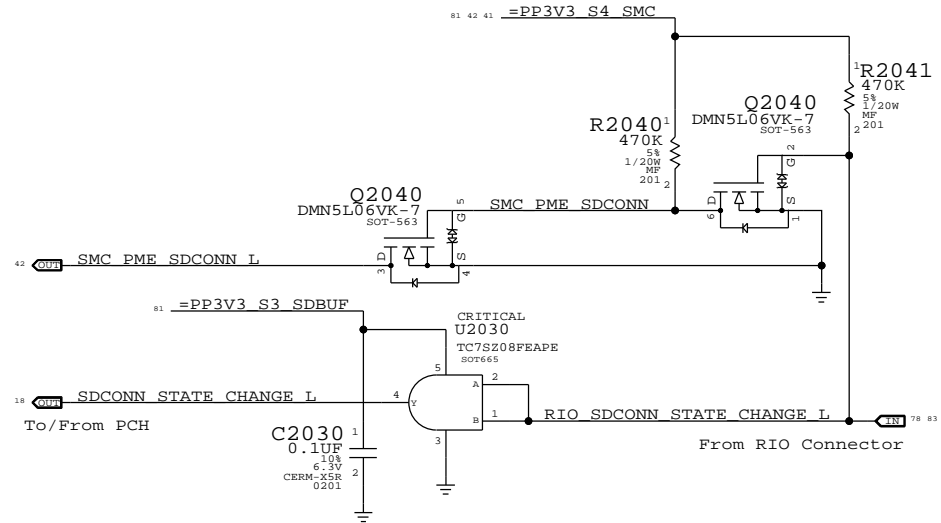
NOTE: SLG3NB148A provides slow rising edge on 25MHz_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).



VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.
+V3.3A should be first available ~3.3V power to reduce VBAT draw.

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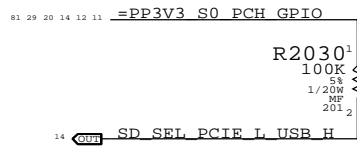
RIO SD Card Reader Support



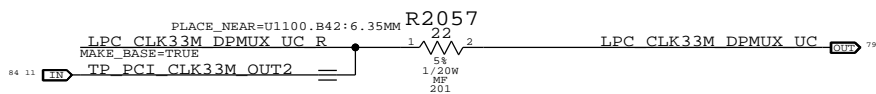
Flexible I/O Aliases
SD Card Reader is always USB3 in this implementation.

- USB3RPCIE SD D2R P == USB3 SD D2R P
- USB3RPCIE SD D2R N == USB3 SD D2R N
- USB3RPCIE SD R2D C P == USB3 SD R2D C P
- USB3RPCIE SD R2D C N == USB3 SD R2D C N

Flexible I/O Configuration Strap
Must pull signal correctly even if always USB or PCIe

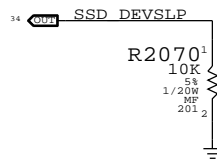


PCH 33MHz Clock for DPMUX

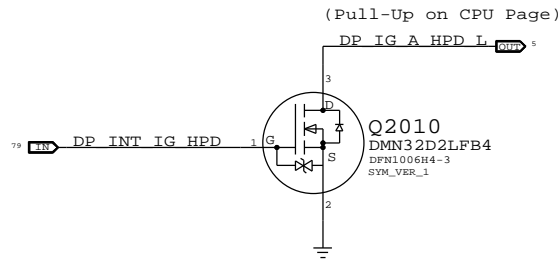


GS3 Connector Support

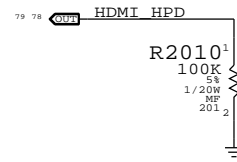
DEVSLP not supported on LPT-H



LCD HPD Inverter

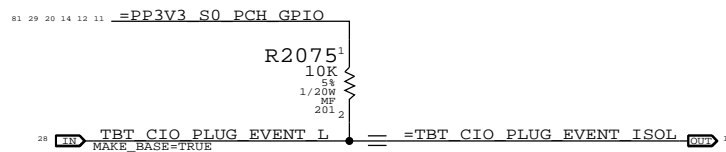


HDMI HPD pull-down



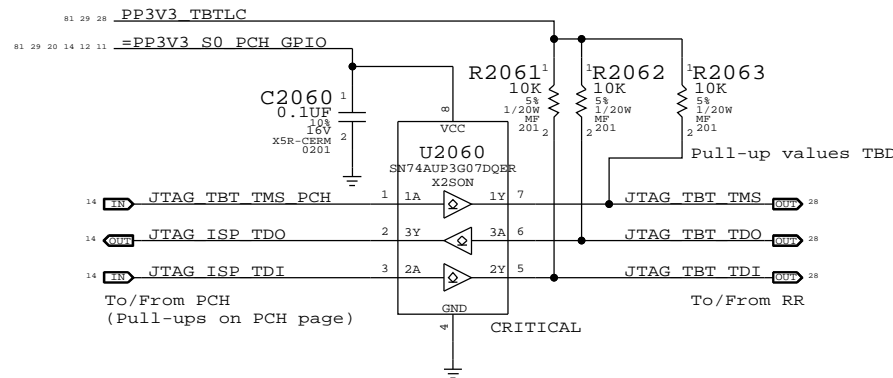
Redwood Ridge Support

RR output is open-drain, no isolation necessary

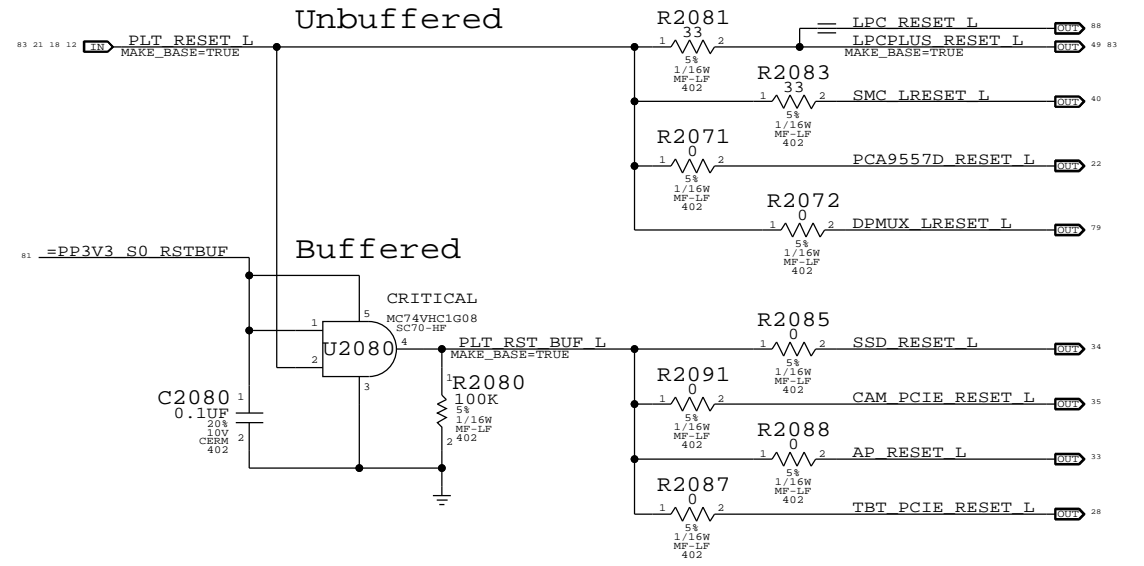


Redwood Ridge JTAG Isolation

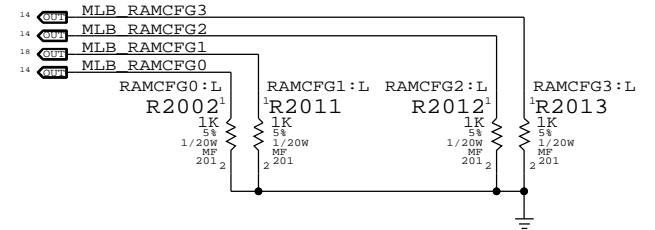
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



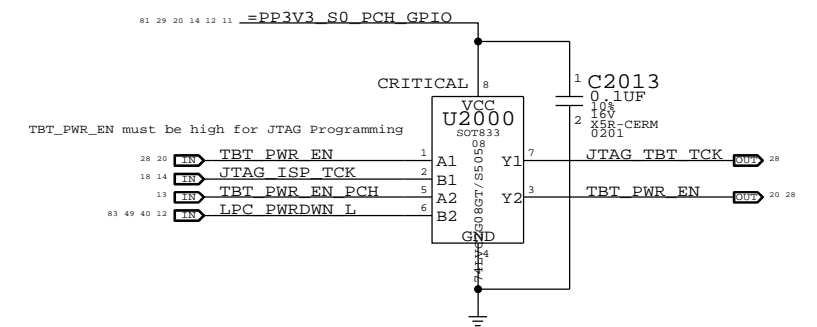
Platform Reset Connections



RAM Configuration Straps



GPIO Glitch Prevention

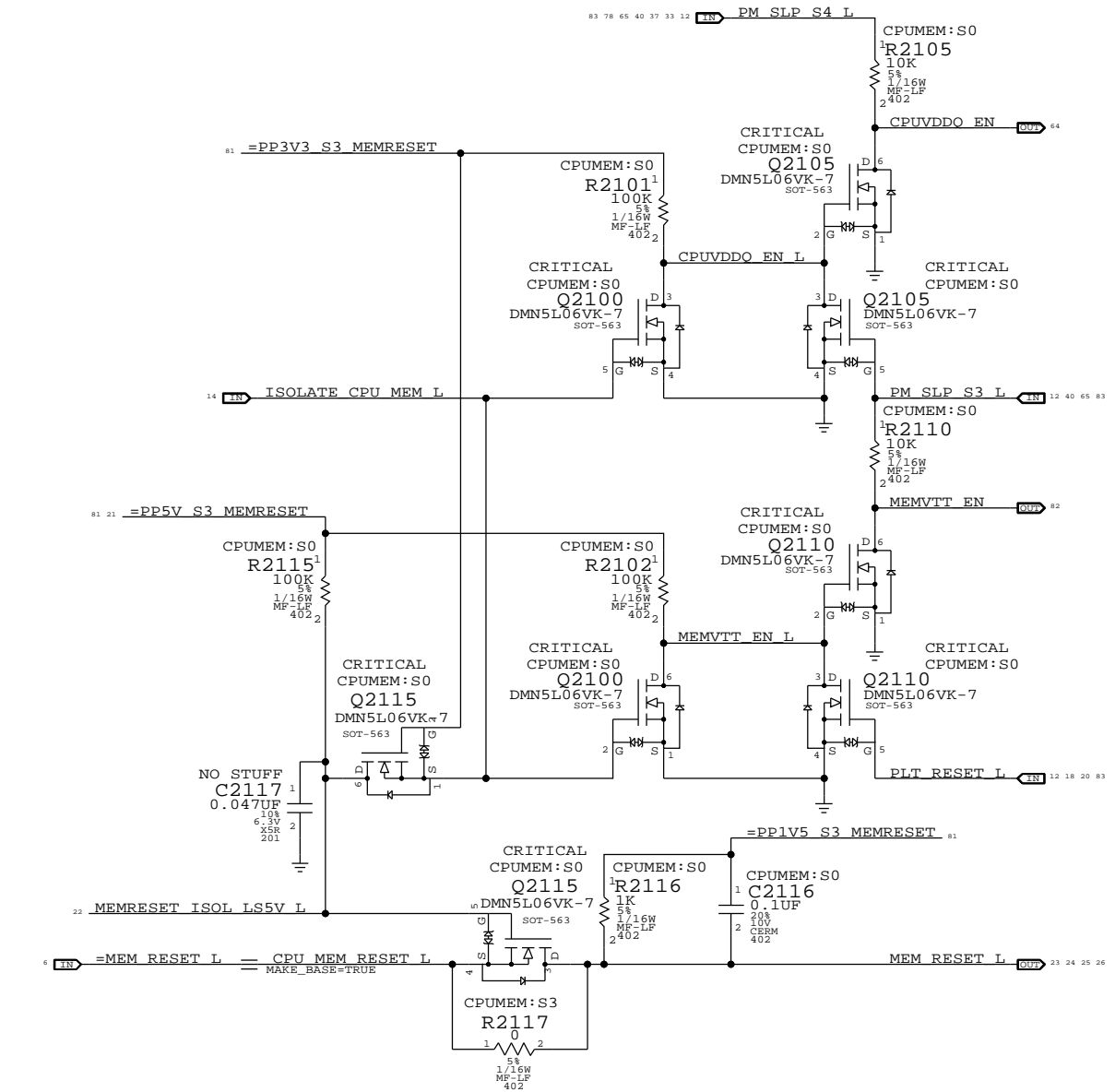


SYNC MASTER=CLEAN_J45		SYNC DATE=04/26/2013	
Project Chipset Support			
Apple Inc.		DRAWING NUMBER	051-0675
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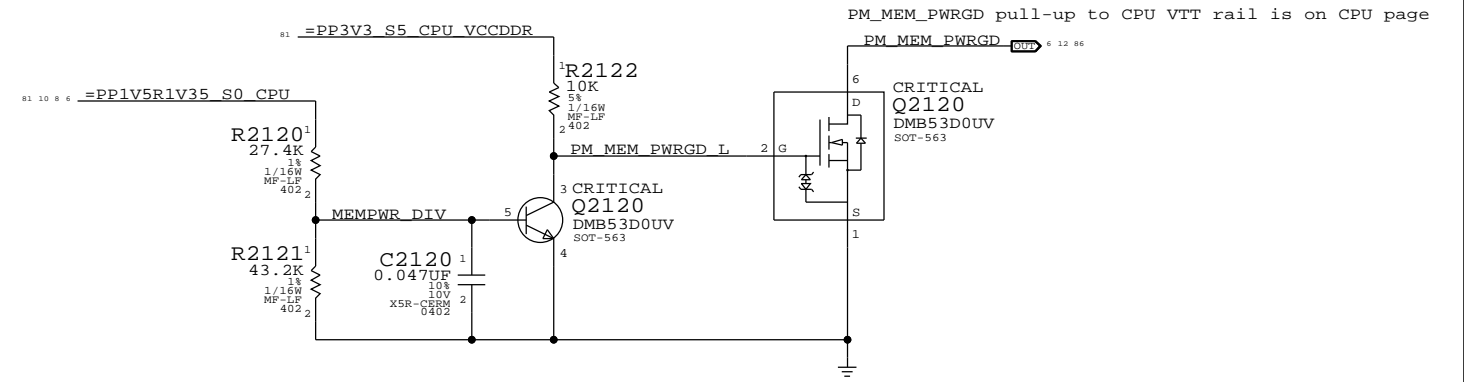
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals. WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated. WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

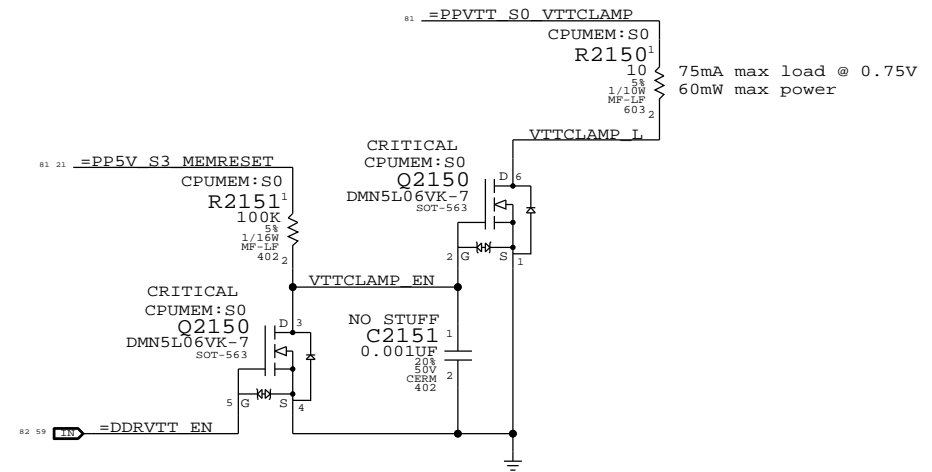
CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



MEM S0 "PGOOD" for CPU



MEMVTT Clamp Ensures CKE signals are held low in S3



Timing table with columns: Step, ISOLATE_CPU_MEM_L, PLT_RESET_L, PM_SLP_S3_L, PM_SLP_S4_L, CPU_MEM_RESET_L, MEM_RESET_L, MEMVTT_EN, CPUVDDQ_EN. Rows show signal states for transitions S0 to S3 and S3 to S0.

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

Technical drawing header and footer containing Apple logo, Apple Inc., drawing number 051-0675, revision 6.0.0, and page information (21 OF 119 SHEET 21 OF 94).

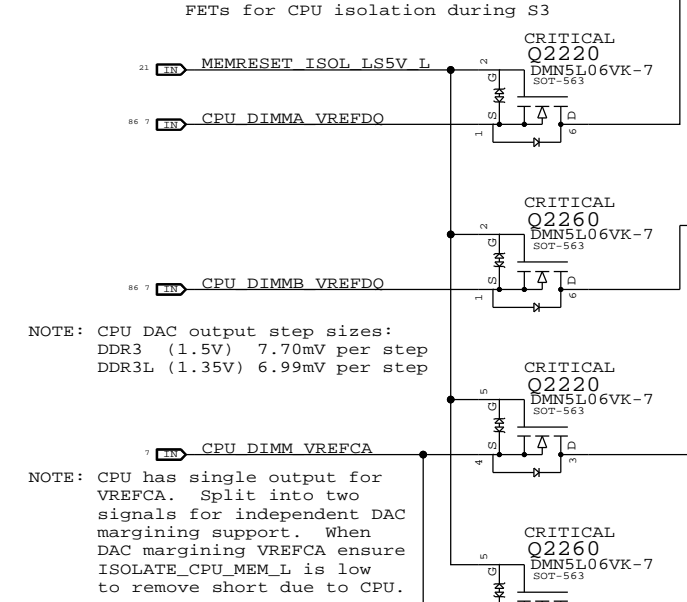
Page Notes

Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPDDR_S3_MEMVREF

Signal aliases required by this page:
 - =I2C_VREFDAC_SCL
 - =I2C_VREFDAC_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

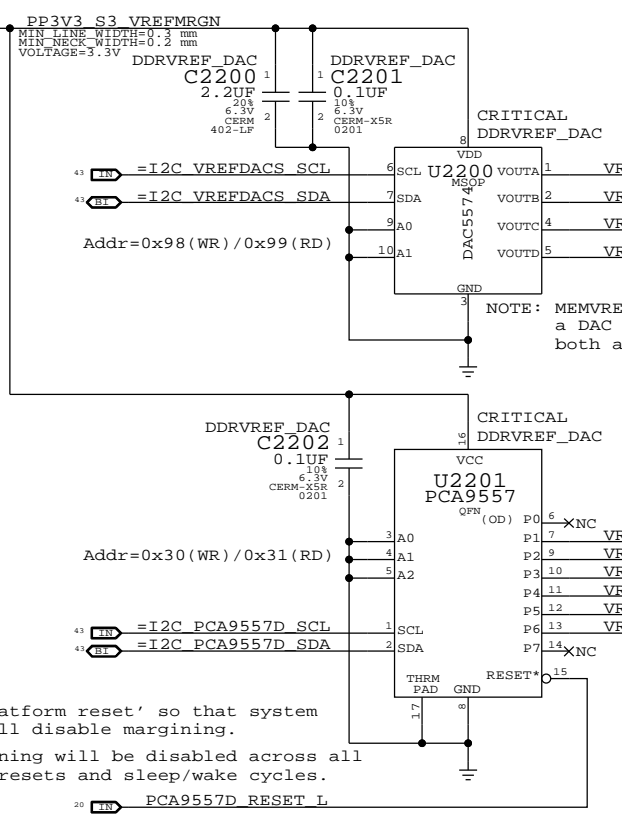
BOM options provided by this page:
 - DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining



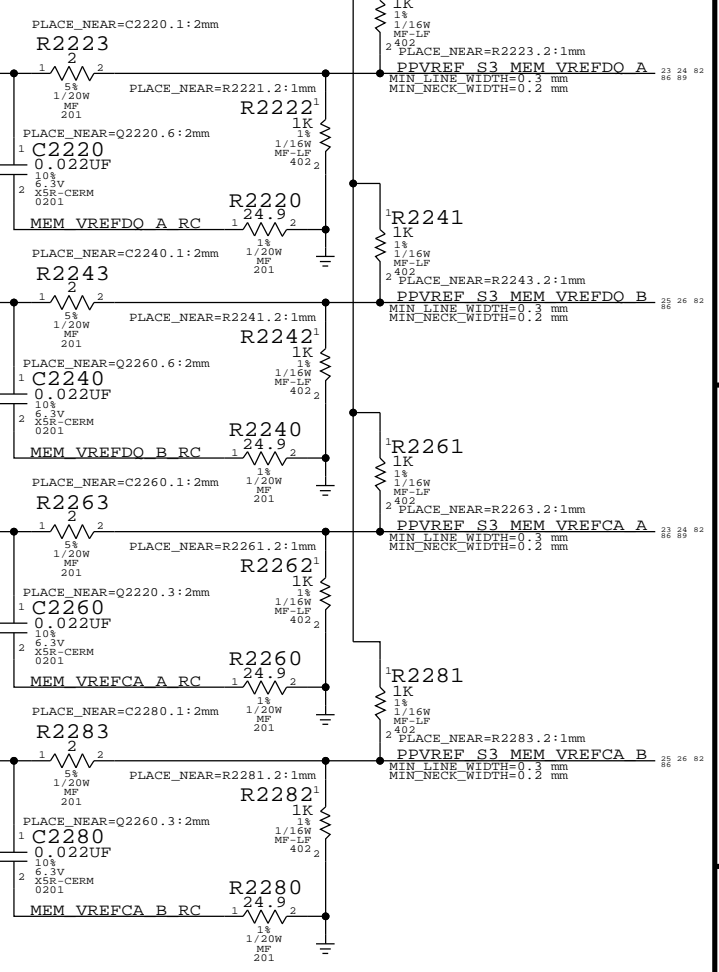
DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



VRef Dividers

Always used, regardless of margining option.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
	DDR3 (1.5V)		DDR3L (1.35V)		
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)
VREF current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
 DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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DDR3 VREF MARGINING

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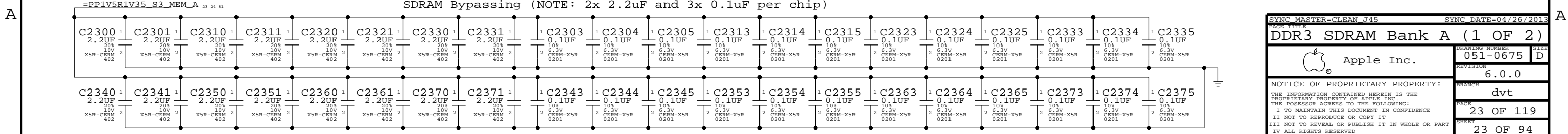
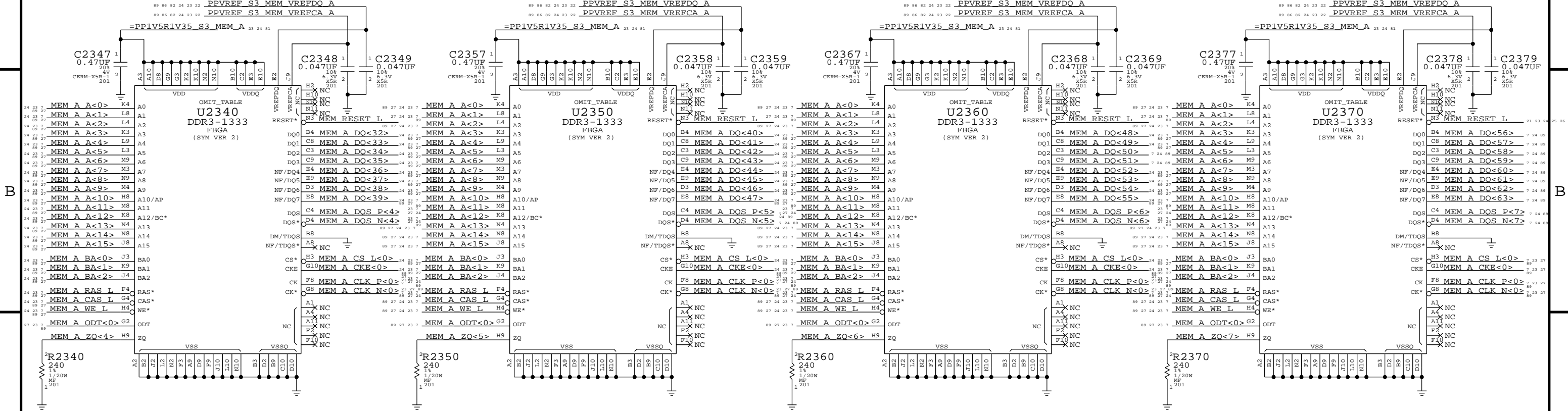
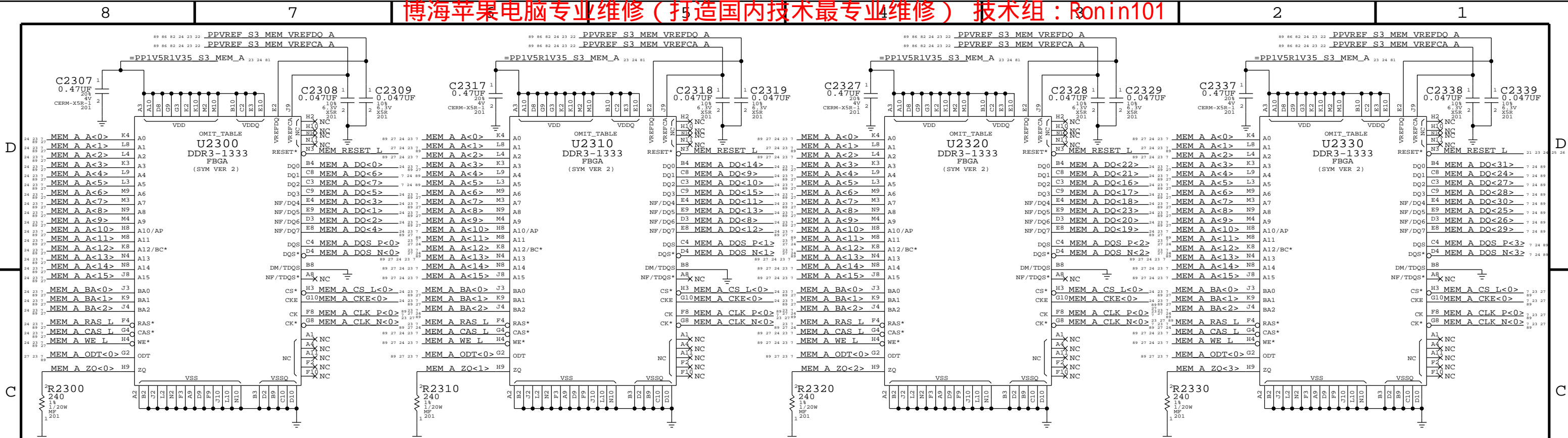
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DDR3 SDRAM Bank A (1 OF 2)

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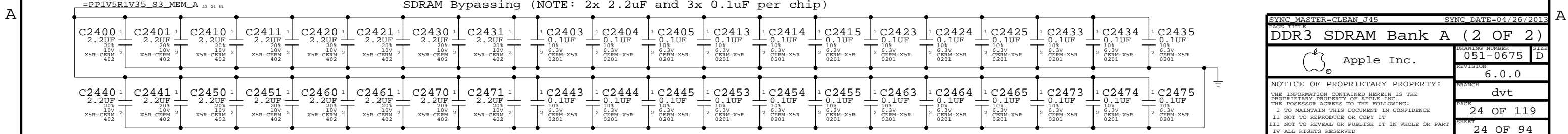
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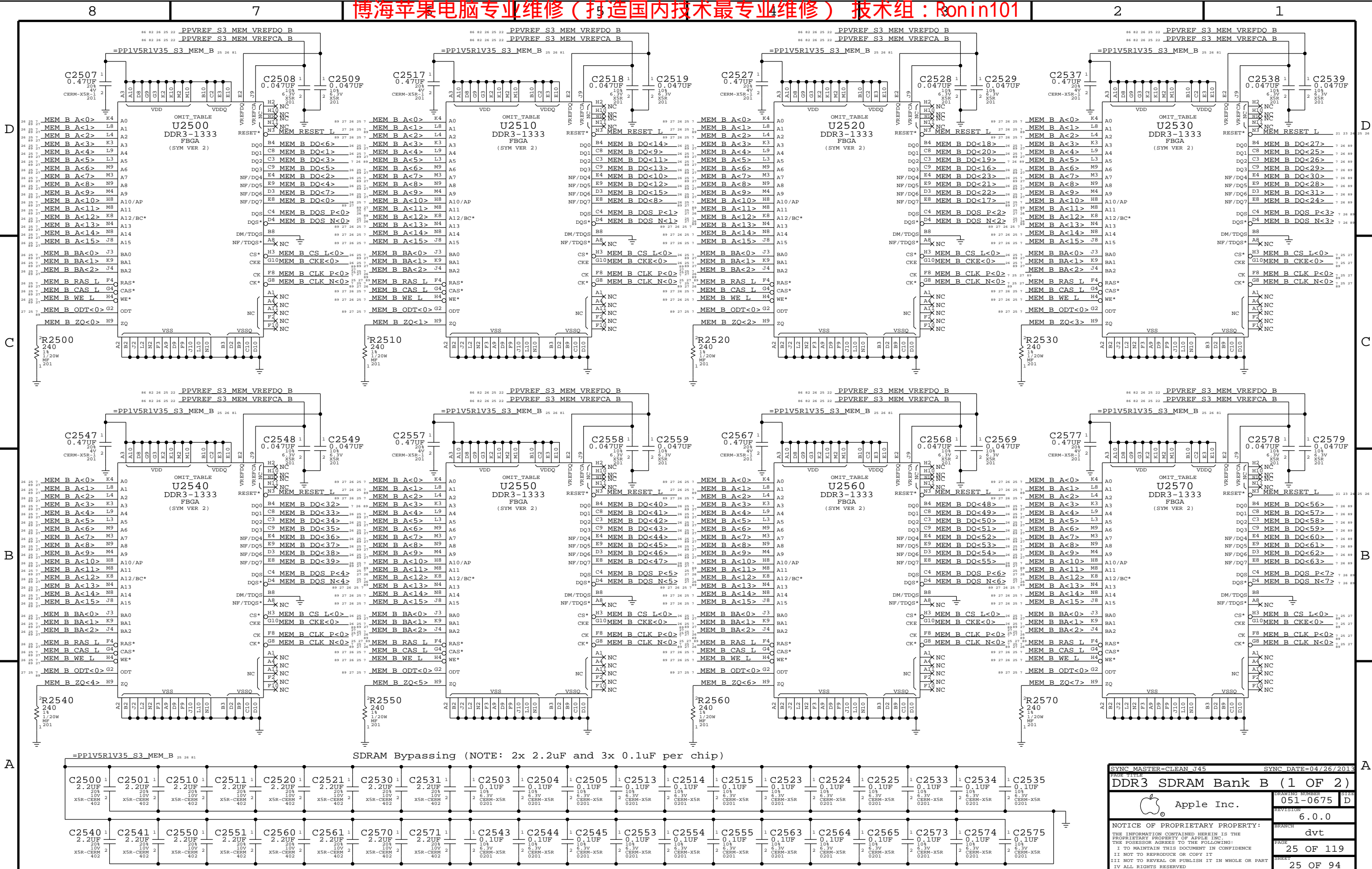
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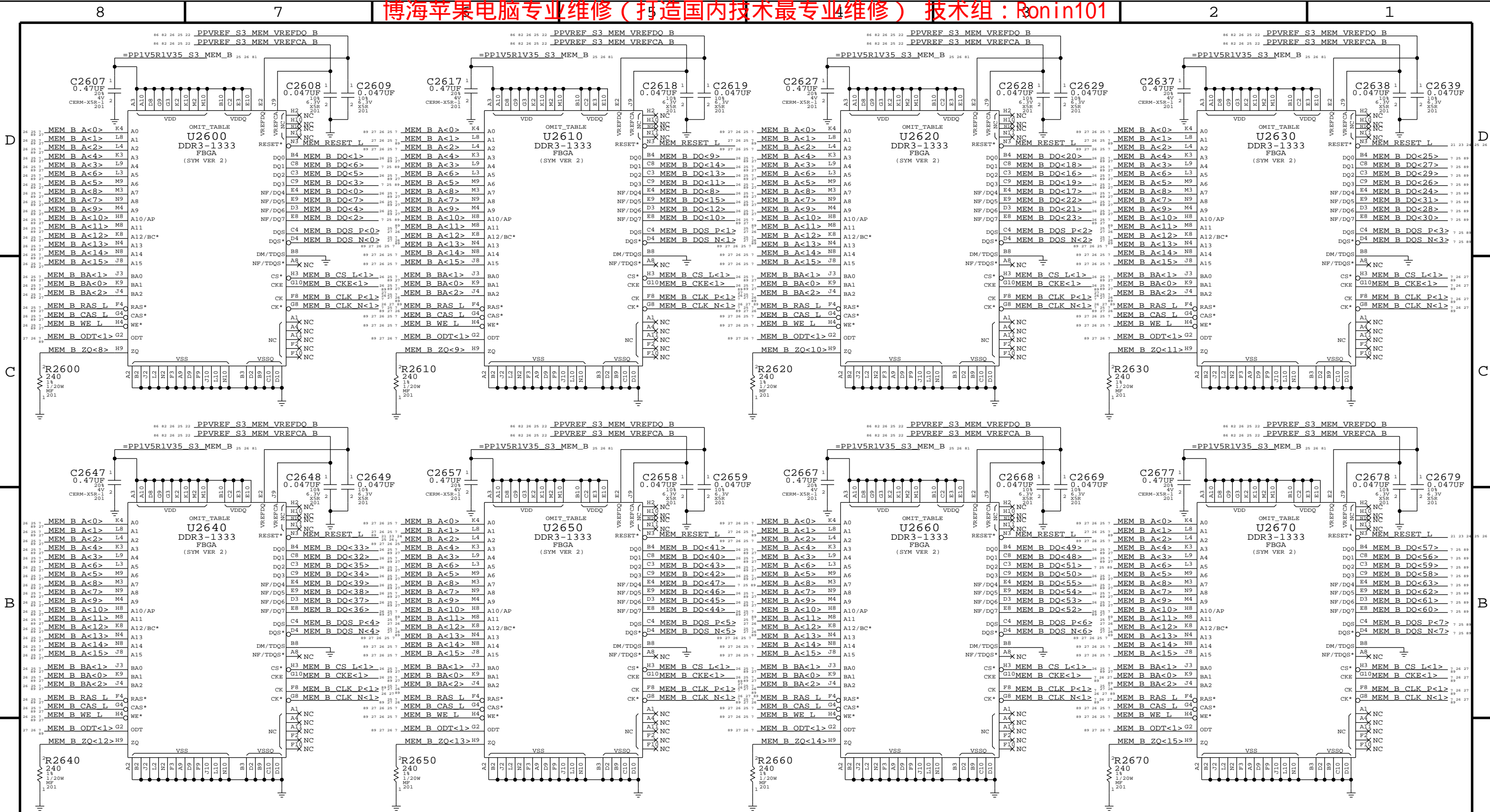
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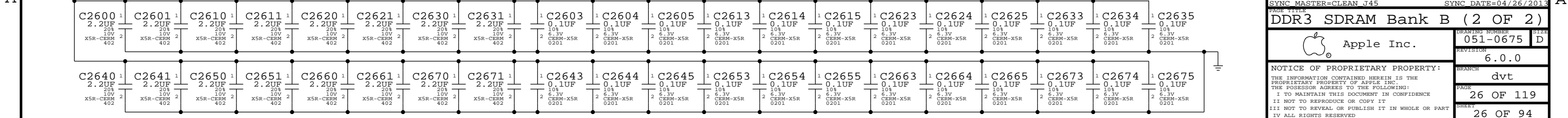
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SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)



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DDR3 SDRAM Bank B (2 OF 2)

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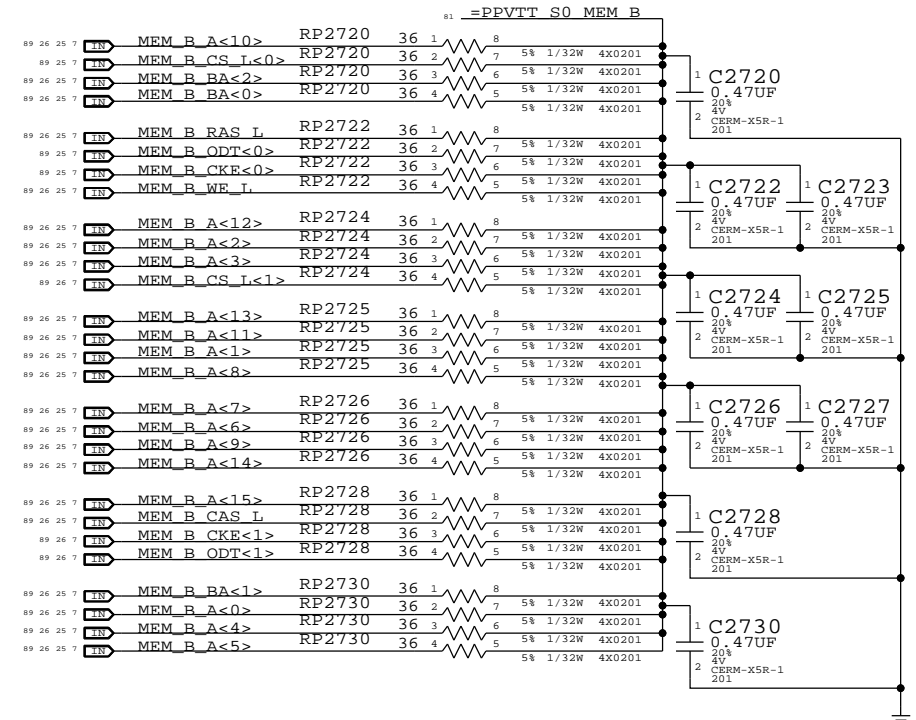
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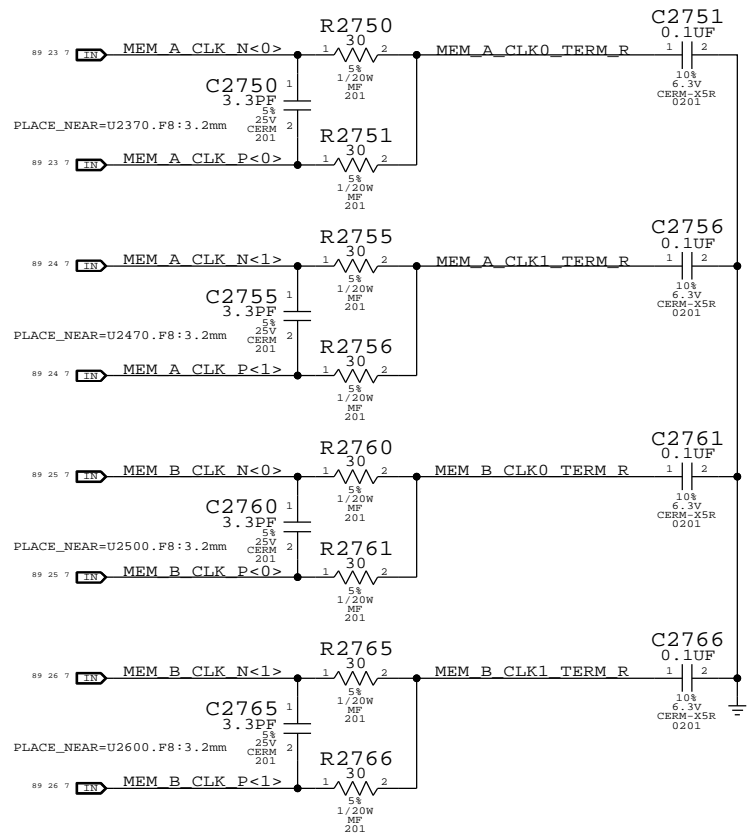
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JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



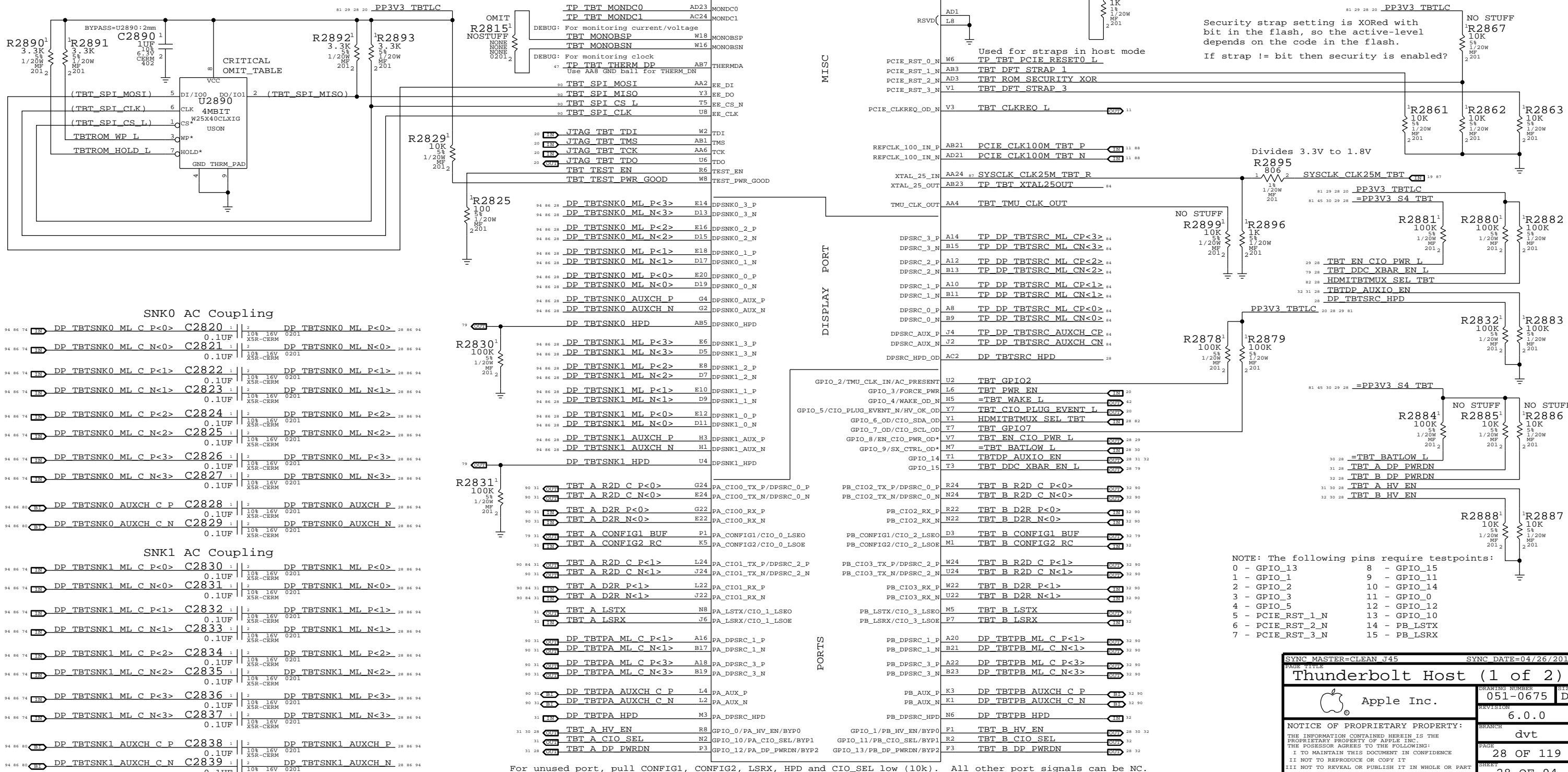
MEM Clock Termination
 Place RC end termination after last DRAM
 Place Source Cterm at neckdown at first DRAM



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DDR3 Termination			
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CRITICAL OMIT_TABLE

Table listing pin connections for U2800 REDWOOD-RIDGE, including PCIE TBT R2D C P<0> through C P<3> and N<0> through N<3>.



SNK0 AC Coupling

Table listing pin connections for SNK0 AC Coupling, including DP TBTSNK0 ML C P<0> through C P<3> and N<0> through N<3>.

SNK1 AC Coupling

Table listing pin connections for SNK1 AC Coupling, including DP TBTSNK1 ML C P<0> through C P<3> and N<0> through N<3>.

DISPLAY PORT

Table listing pin connections for DISPLAY PORT, including DP TBTSNK0 ML P<0> through C P<3> and N<0> through N<3>.

PORTS

Table listing pin connections for PORTS, including TBT A R2D C P<0> through C P<3> and N<0> through N<3>.

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash. If strap != bit then security is enabled?

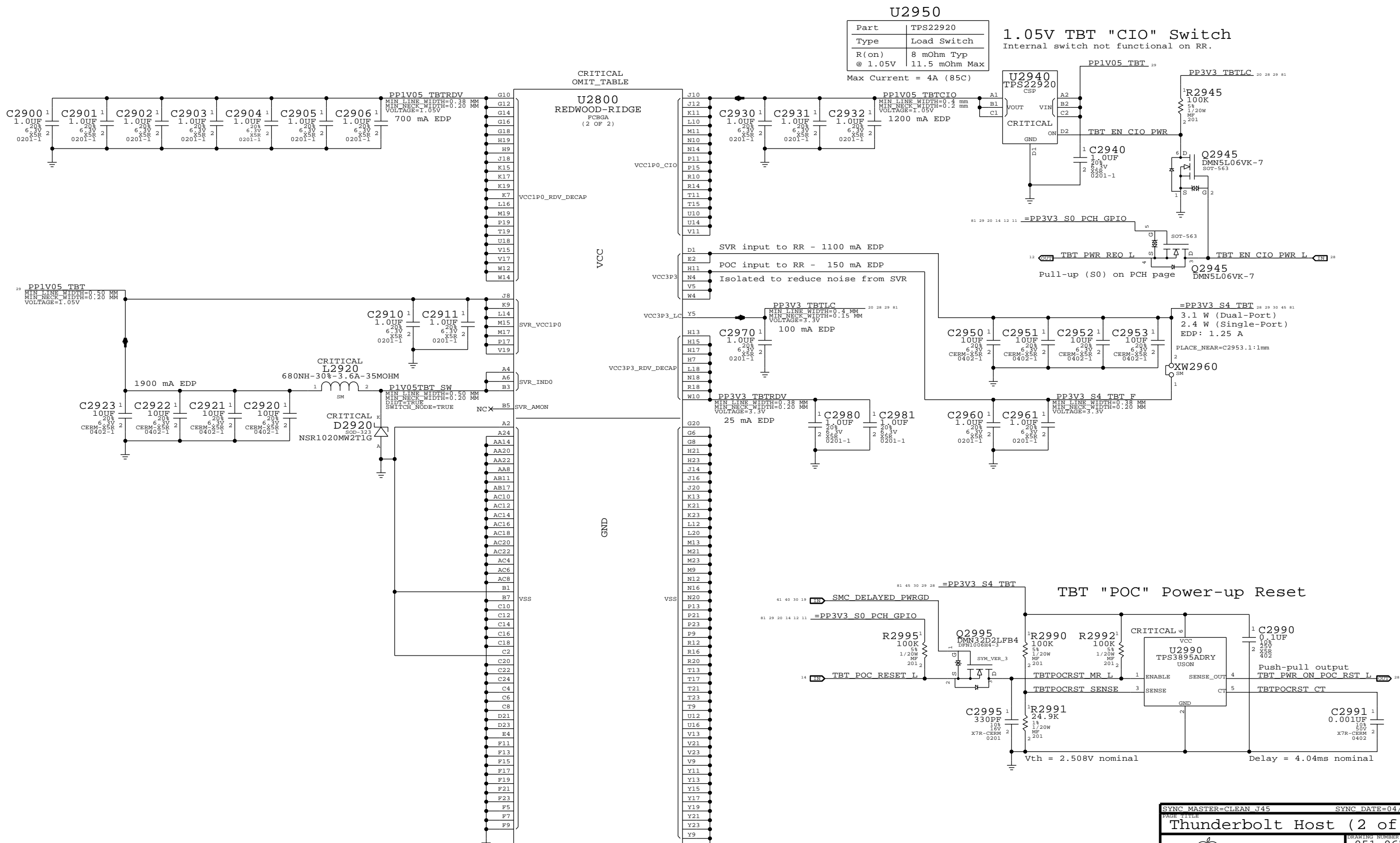
Divides 3.3V to 1.8V

- NOTE: The following pins require testpoints: 0 - GPIO_13, 1 - GPIO_1, 2 - GPIO_2, 3 - GPIO_3, 4 - GPIO_5, 5 - PCIE_RST_1_N, 6 - PCIE_RST_2_N, 7 - PCIE_RST_3_N, 8 - GPIO_15, 9 - GPIO_11, 10 - GPIO_14, 11 - GPIO_0, 12 - GPIO_12, 13 - GPIO_10, 14 - PB_LSTX, 15 - PB_LSRX

Technical drawing header for 'Thunderbolt Host (1 of 2)' by Apple Inc., including drawing number 051-0675, revision 6.0.0, and page information.

D
C
B
A

D
C
B
A



U2950	
Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max
Max Current = 4A (85C)	

1.05V TBT "CIO" Switch
Internal switch not functional on RR.

PP3V3 S4 TBT F
3.1 W (Dual-Port)
2.4 W (Single-Port)
EDP: 1.25 A
PLACE_NEAR=C2953.1:1mm

TBT "POC" Power-up Reset
Vth = 2.508V nominal
Delay = 4.04ms nominal

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
Thunderbolt Host (2 of 2)			
Apple Inc.		DRAWING NUMBER	051-0675
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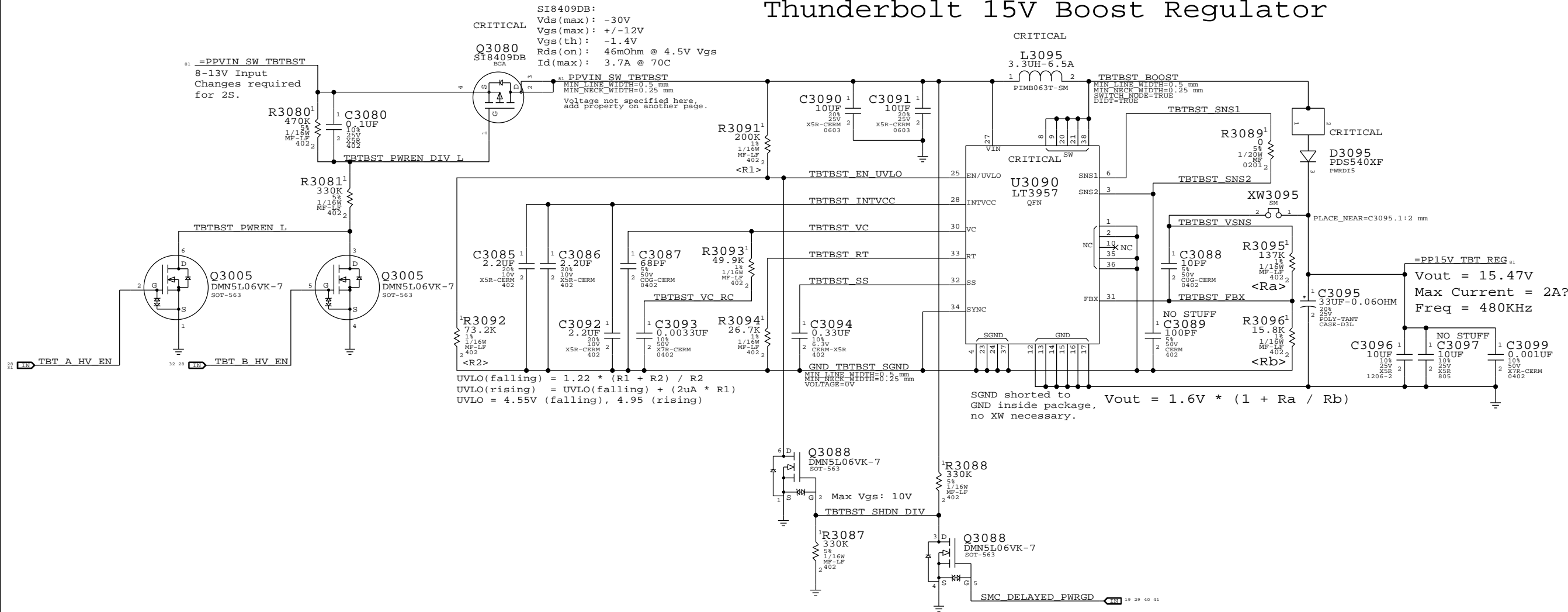
Page Notes

Power aliases required by this page:
 - =PPVIN_SW_TBTBST (8-13V Boost Input)
 - =PP15V_TBT_REG (15V Boost Output)

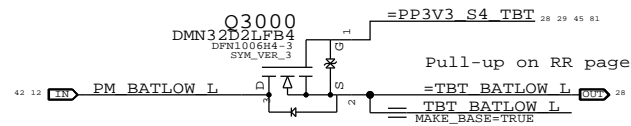
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Thunderbolt 15V Boost Regulator



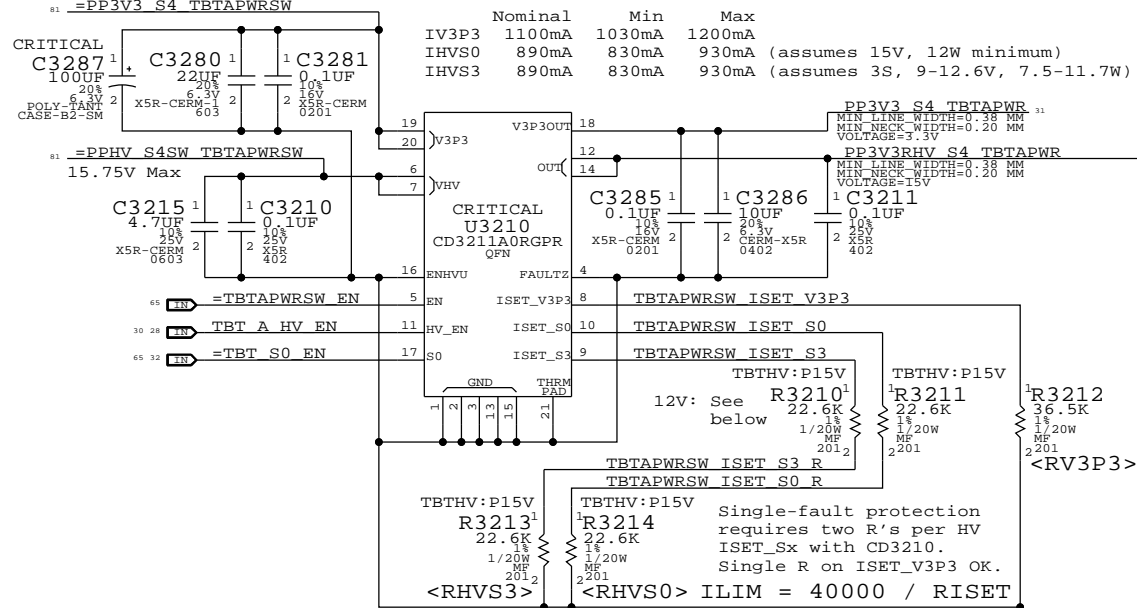
BATLOW# Isolation



SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
Thunderbolt Mobile Support			
Apple Inc.	DRAWING NUMBER	051-0675	SIZE
	REVISION	6.0.0	D
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

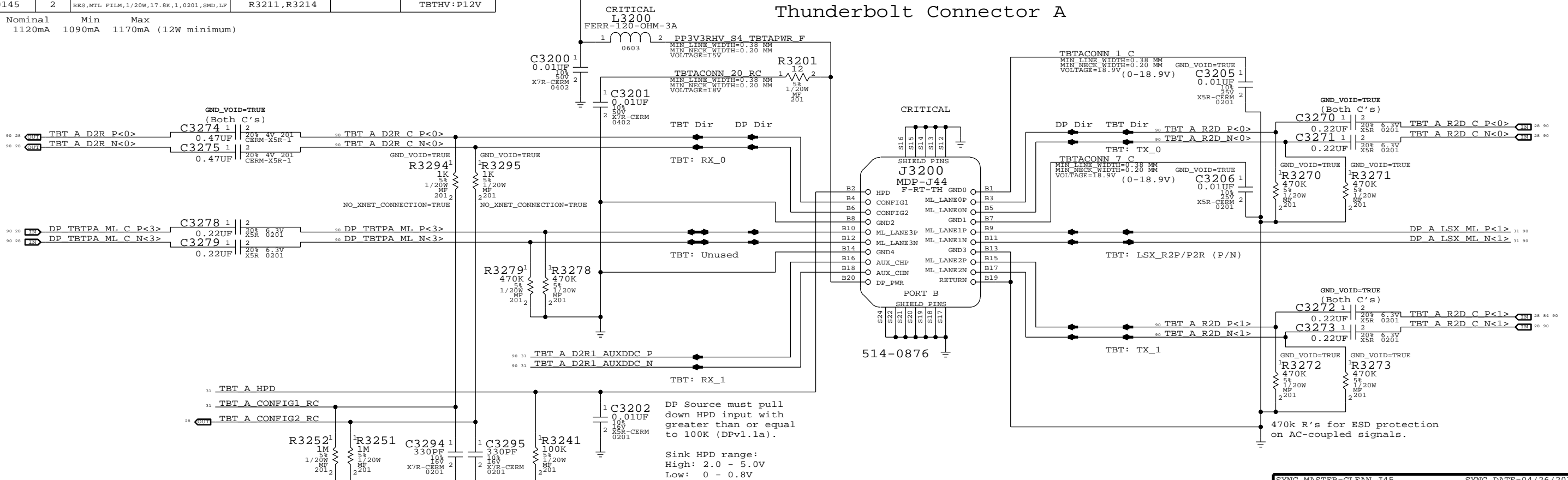


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

Thunderbolt Connector A



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

Thunderbolt Connector A

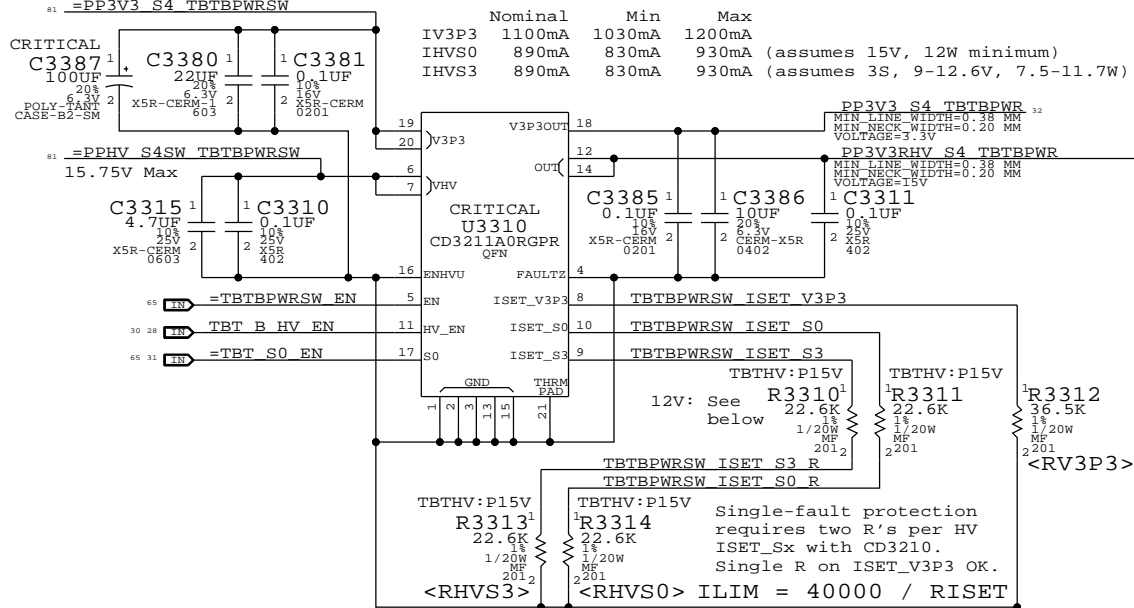
Apple Inc.

051-0675
 REVISION 6.0.0
 BRANCH dvt
 PAGE 32 OF 119
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

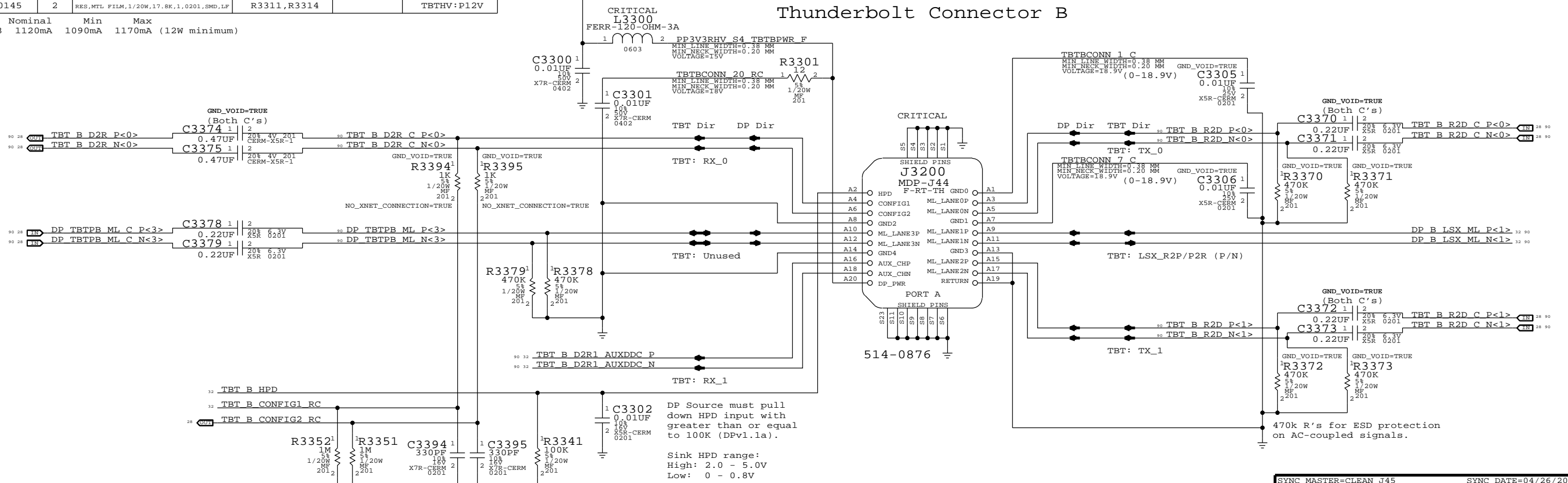


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

Thunderbolt Connector B



DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

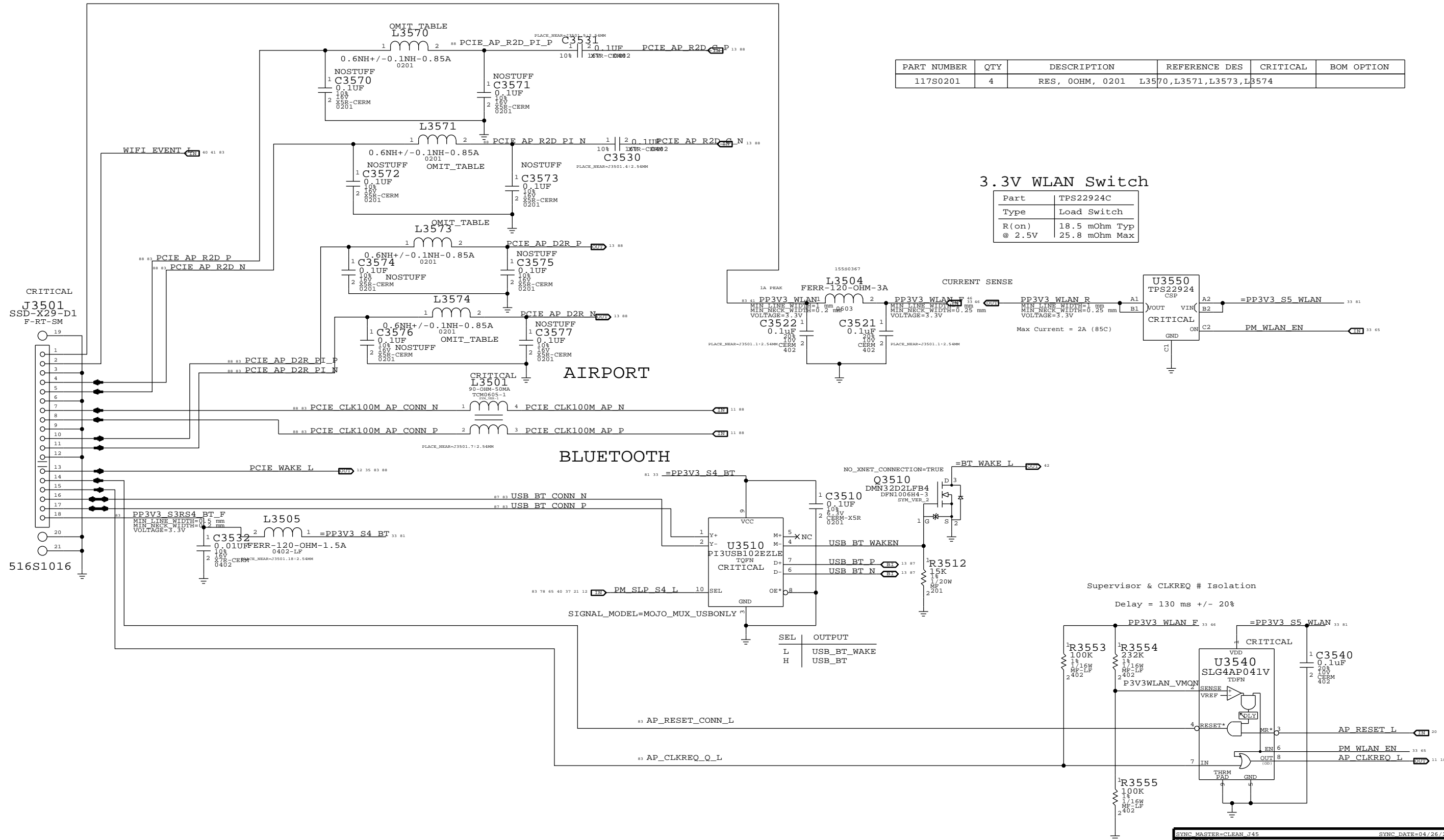
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 00HM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

Supervisor & CLKREQ # Isolation
Delay = 130 ms +/- 20%

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

X29C CONNECTOR

Apple Inc.

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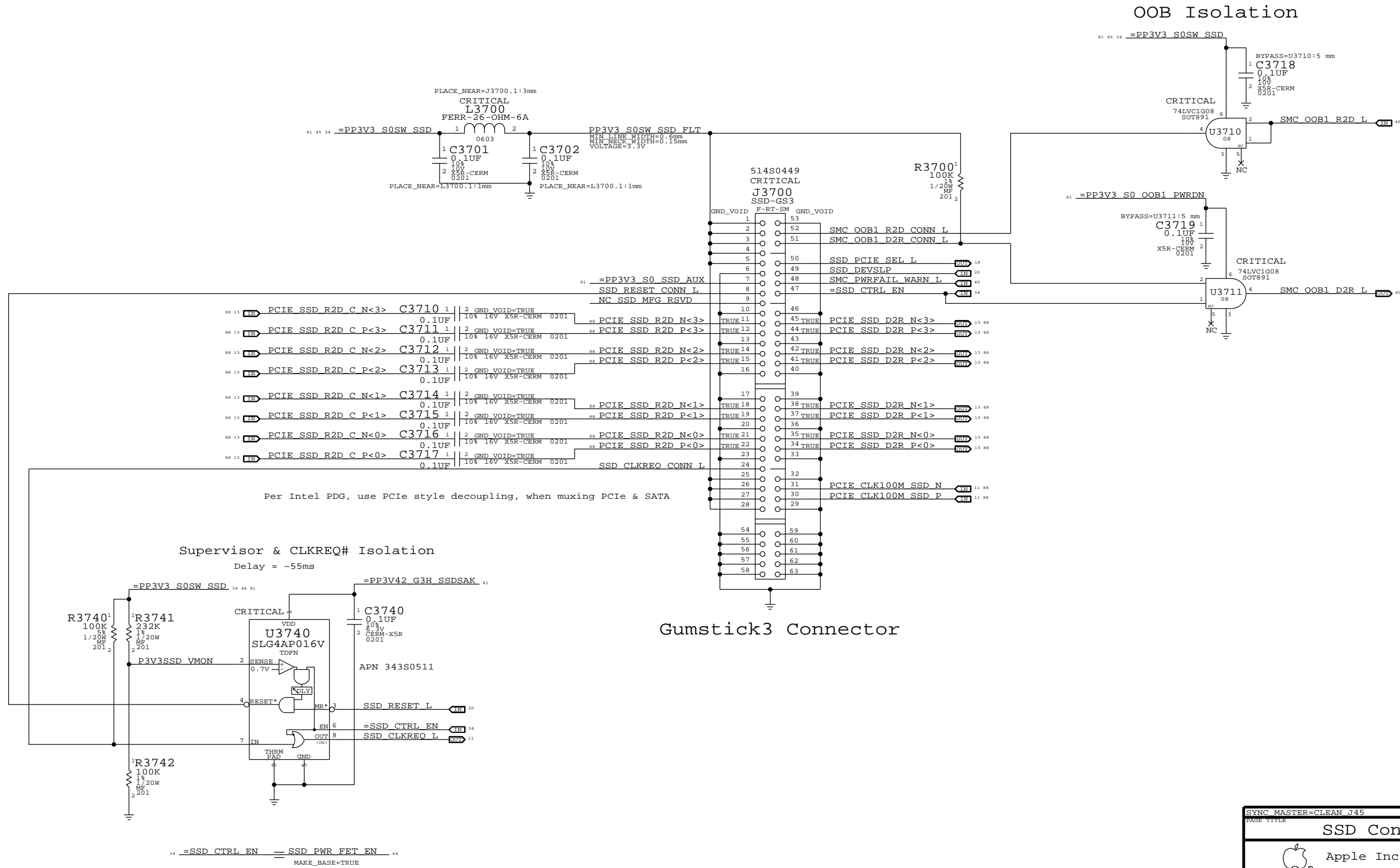
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BRANCH: dvt

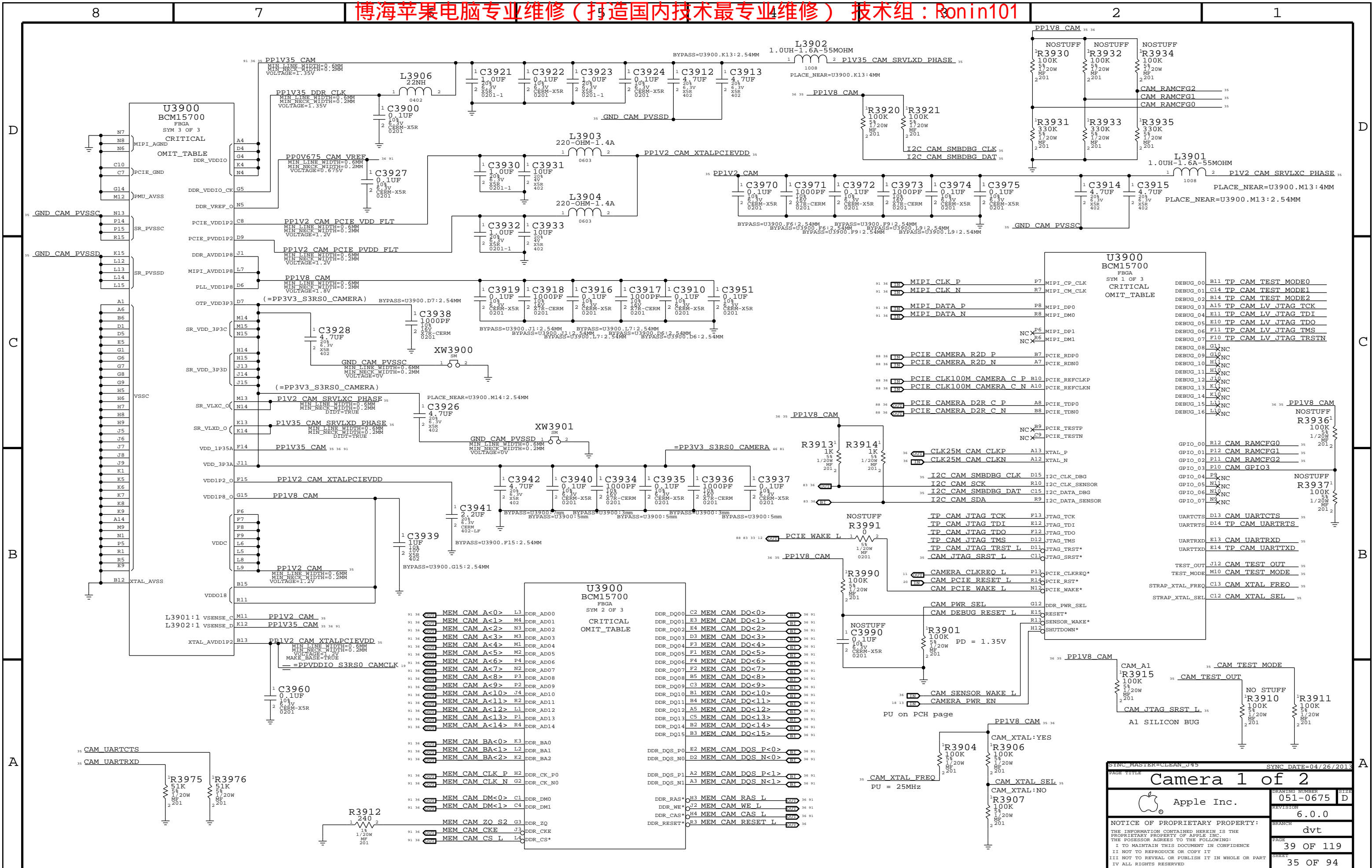
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PAGE TITLE SSD Connector			
DRAWING NUMBER 051-0675		SIZE D	
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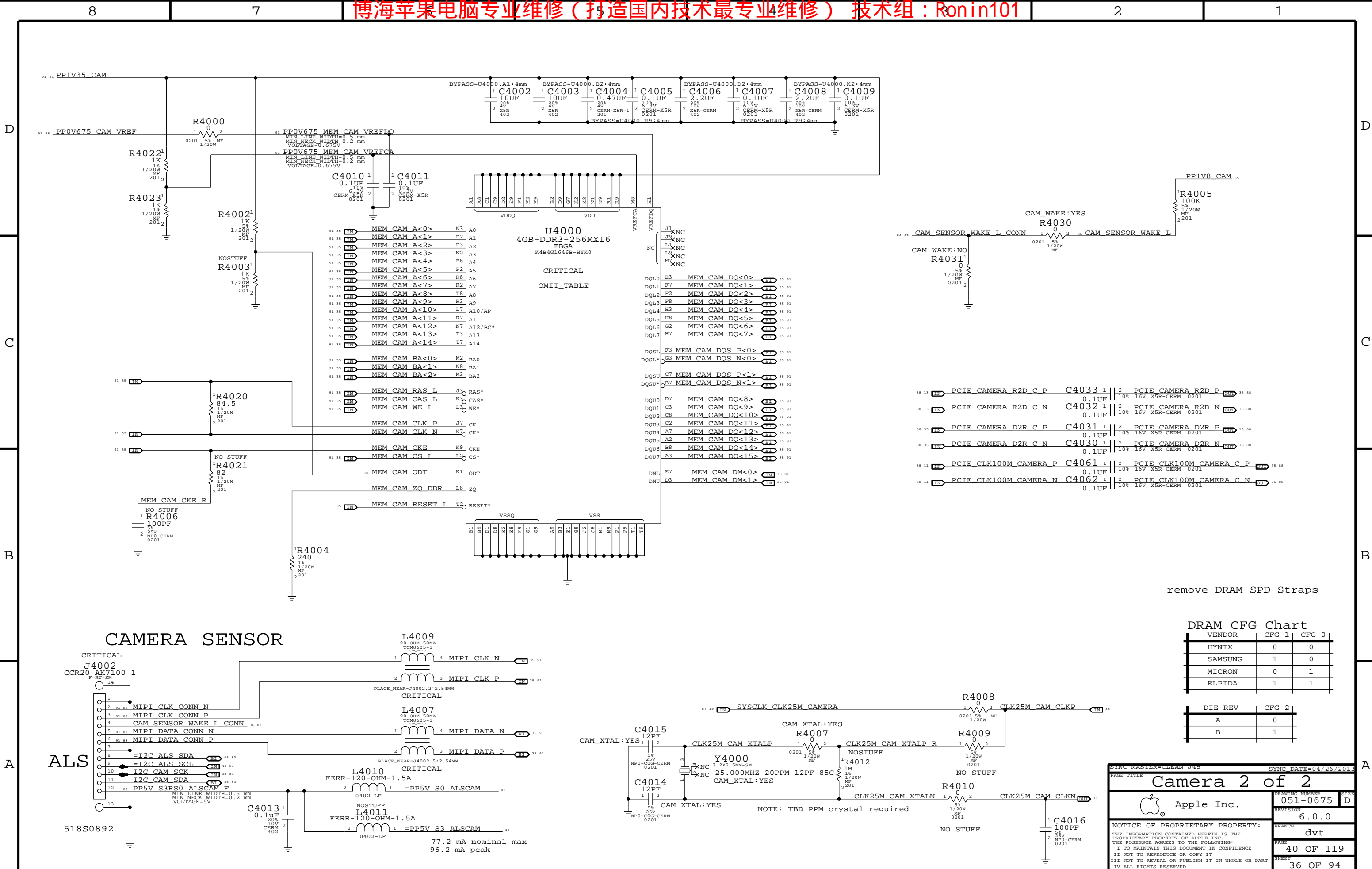
Camera 1 of 2

Apple Inc.

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REVISION: 6.0.0
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SYNCS_MASTER=CLEAN_045 SYNCS_DATE=04/26/2013



remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

Camera 2 of 2

Apple Inc.

051-0675

6.0.0

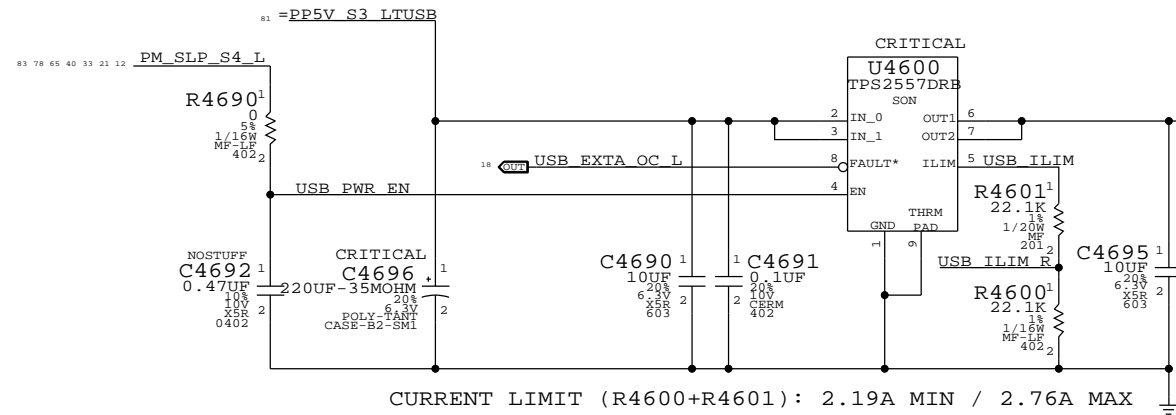
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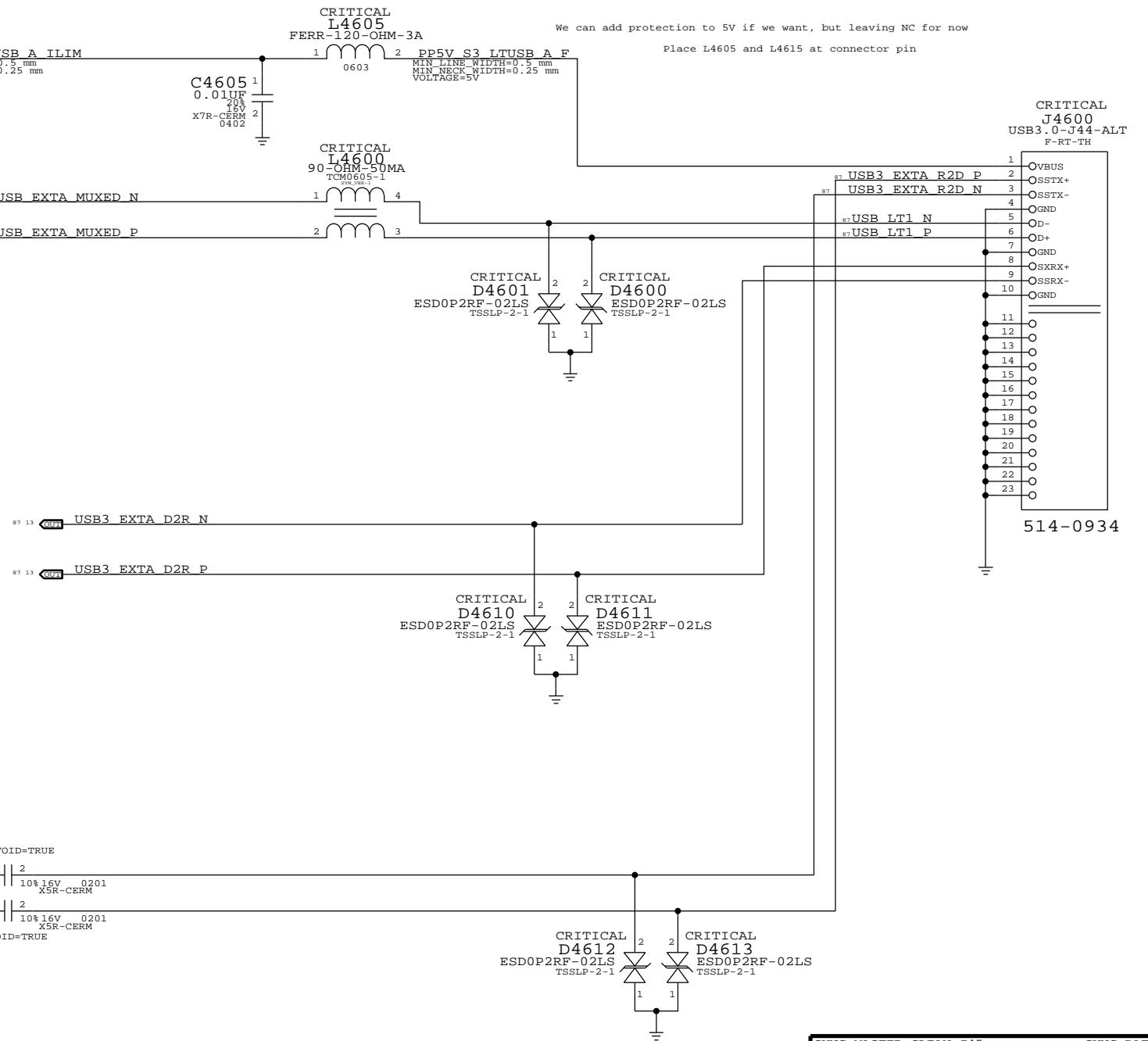
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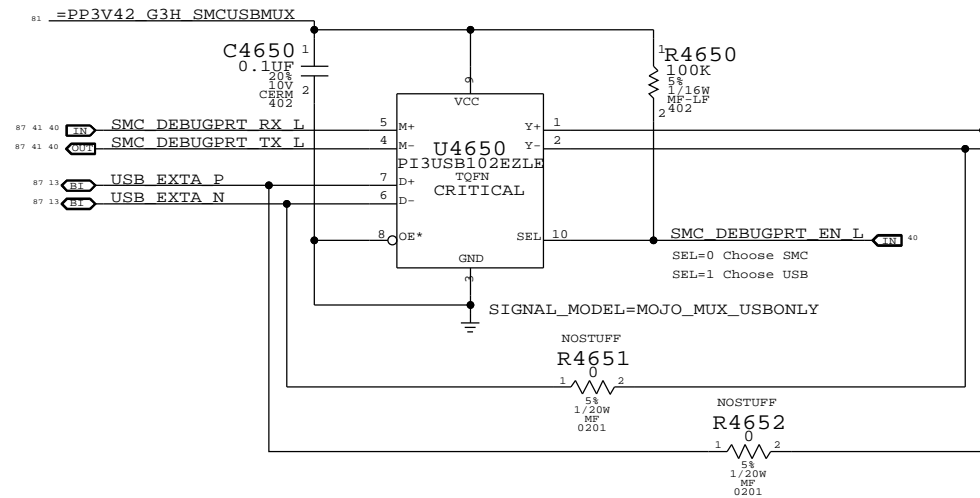
USB Port Power Switch



Left USB Port A

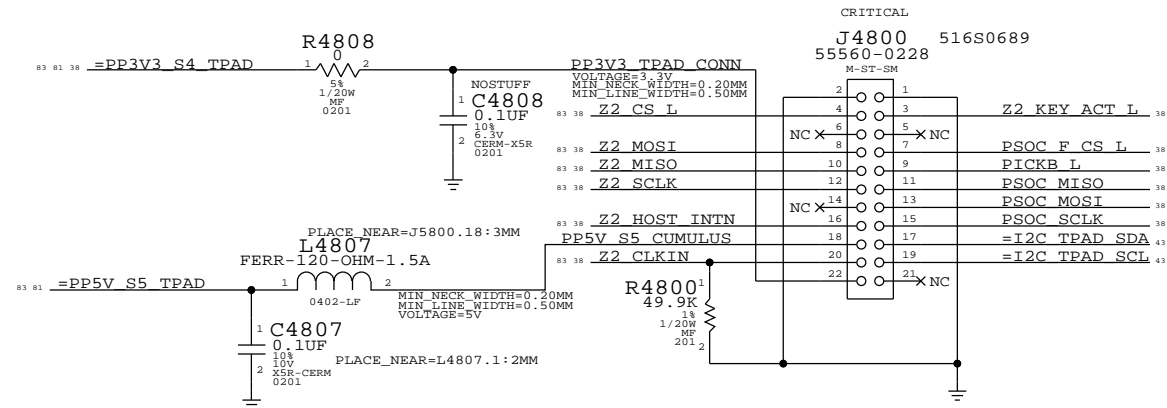


USB/SMC Debug Mux



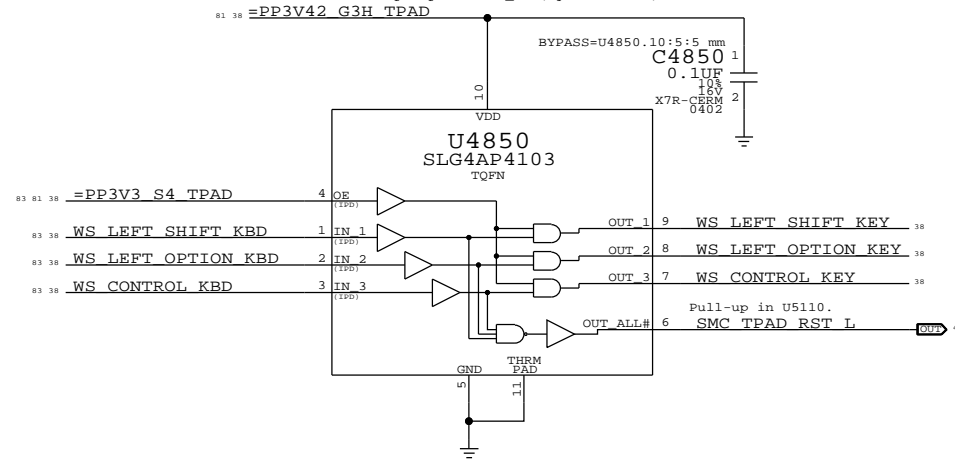
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USB 3.0 CONNECTORS			
Apple Inc.		DRAWING NUMBER	051-0675
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IPD Flex Connector

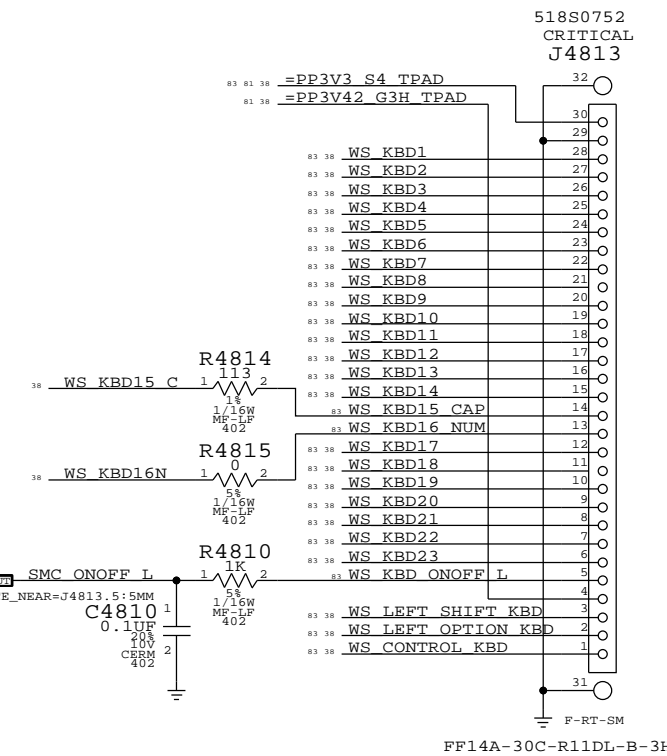


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSoC power to isolate when PSoC is not powered.

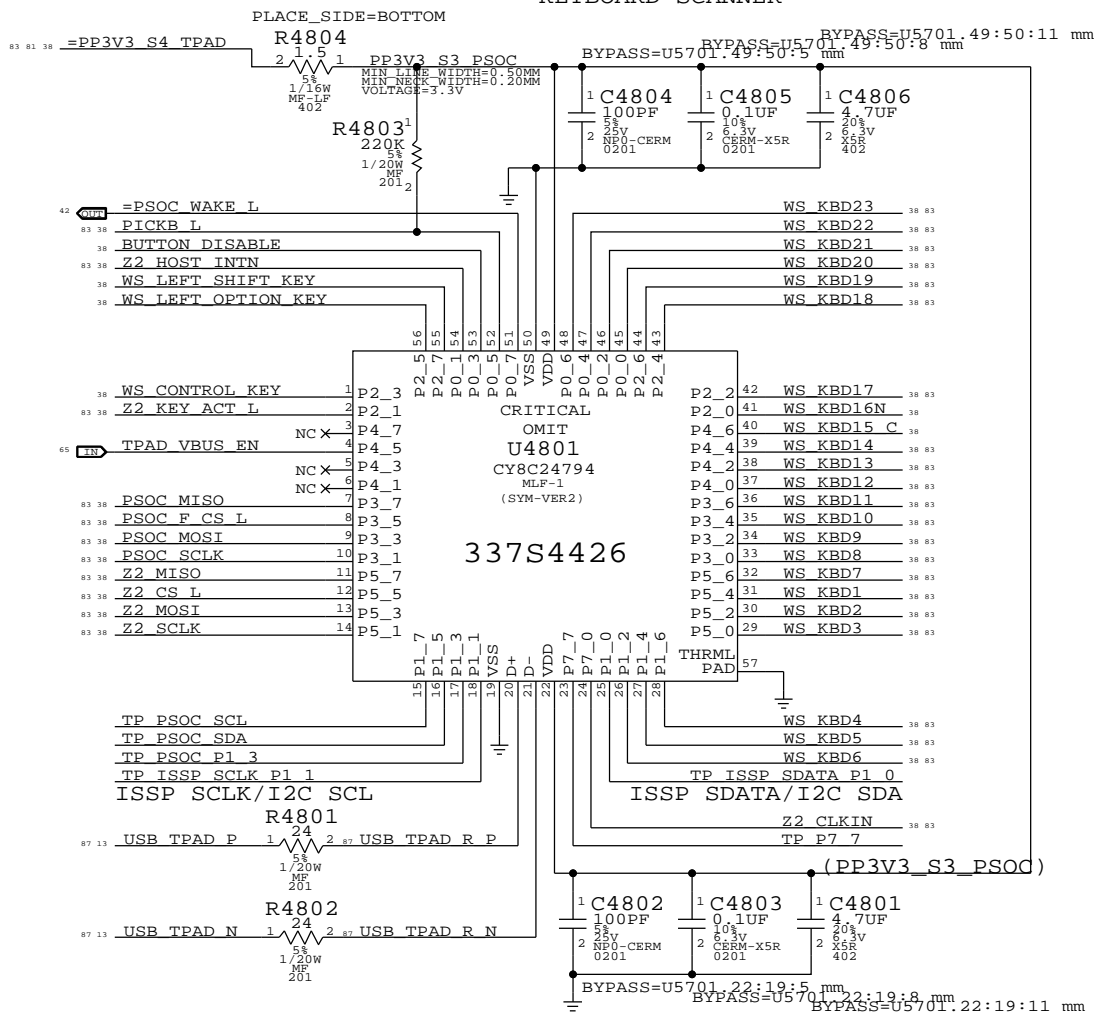


Keyboard Connector



PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

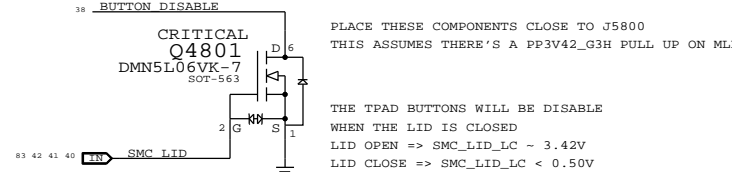
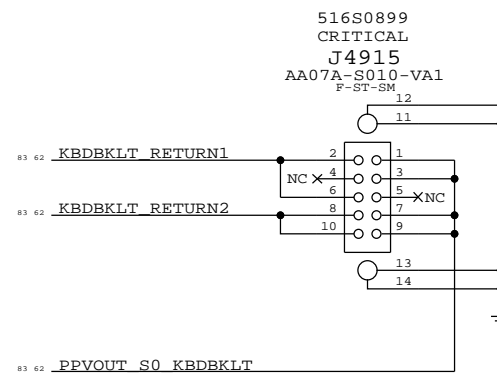


Table with 6 columns: IC, PIN, NAME, CURRENT, R_SNS, V_SNS, POWER. It lists power requirements for components like TMP102, 3V3 LDO, PSOC, and 18V BOOSTER.

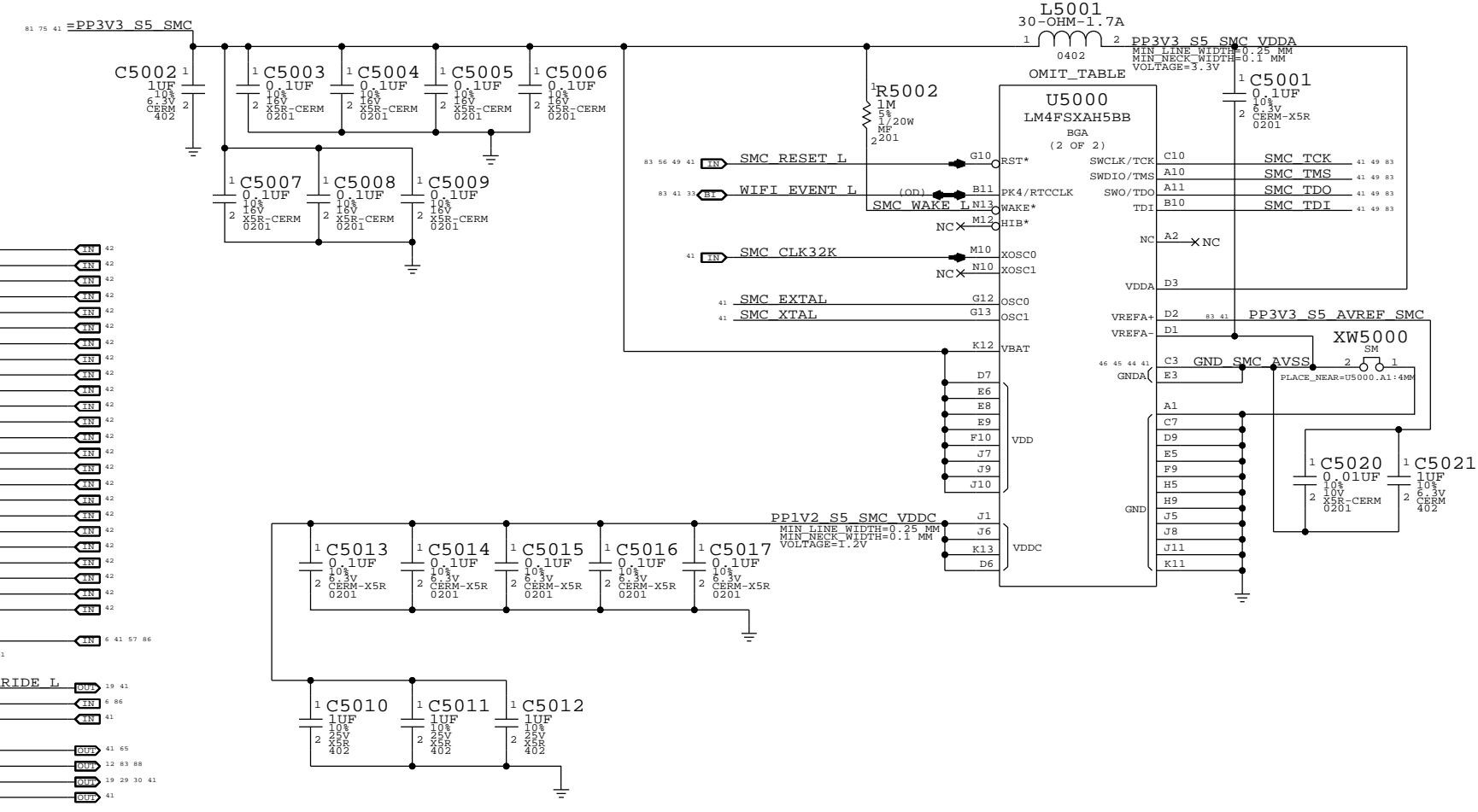
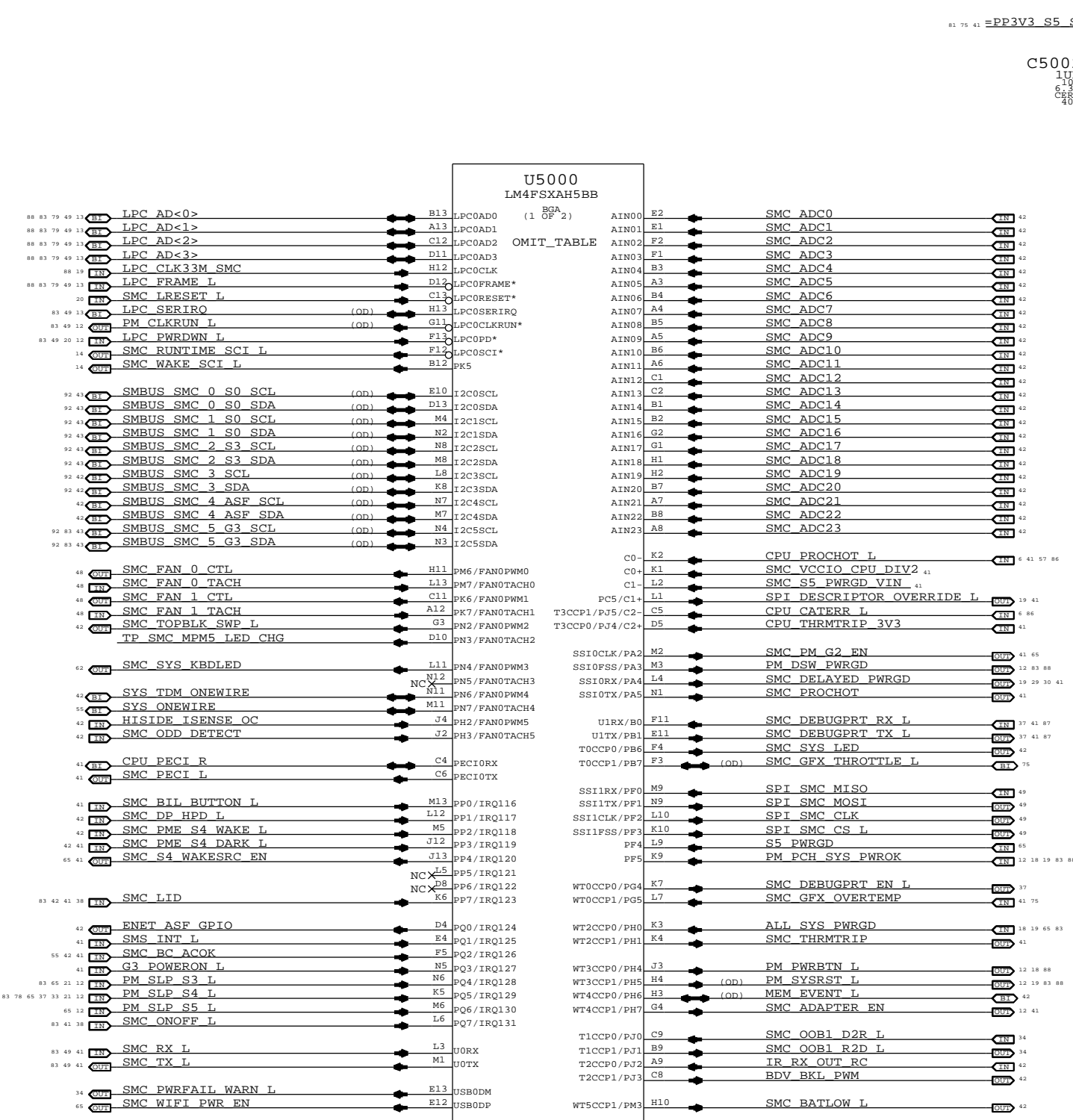
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Keyboard Backlight Connector



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PAGE TITLE KEYBOARD/TRACKPAD (2 OF 2)			
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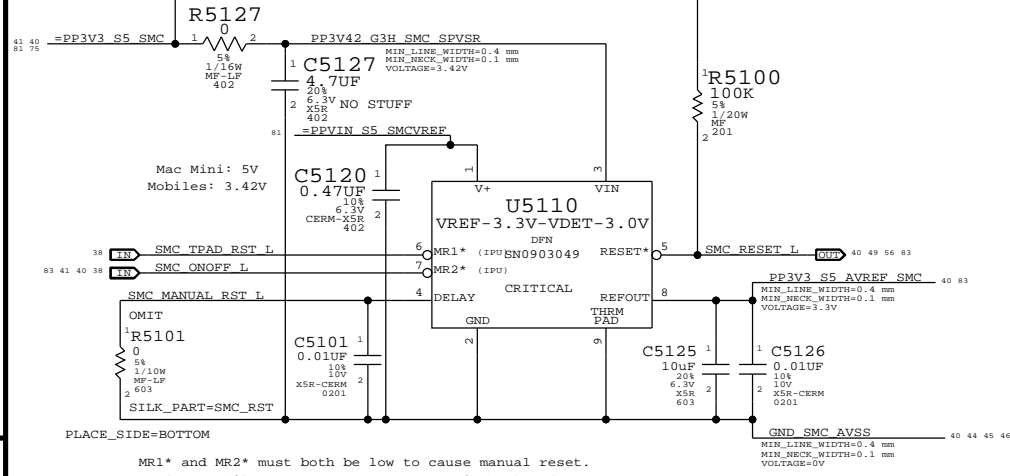
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



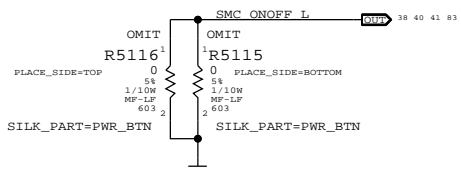
NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

PAGE TITLE		SYNC DATE=04/26/2013	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
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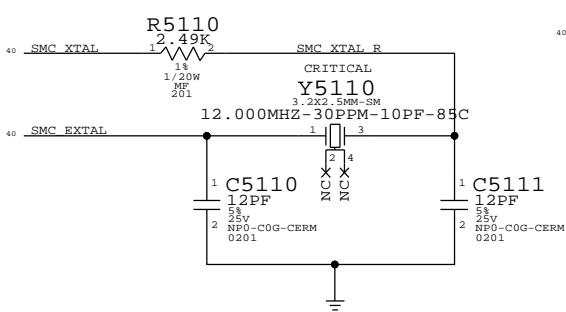
SMC Reset "Button", Supervisor & AVREF Supply



Debug Power "Buttons"

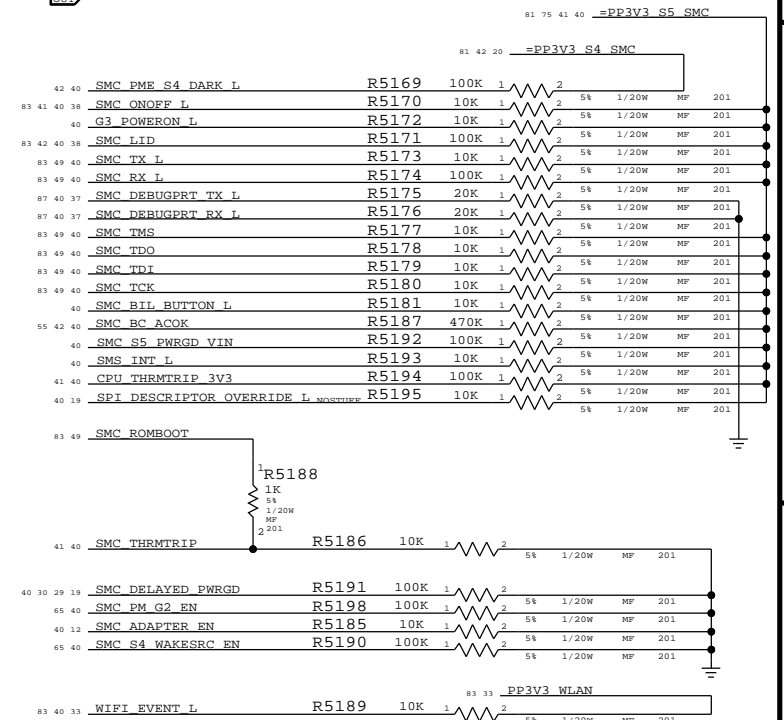
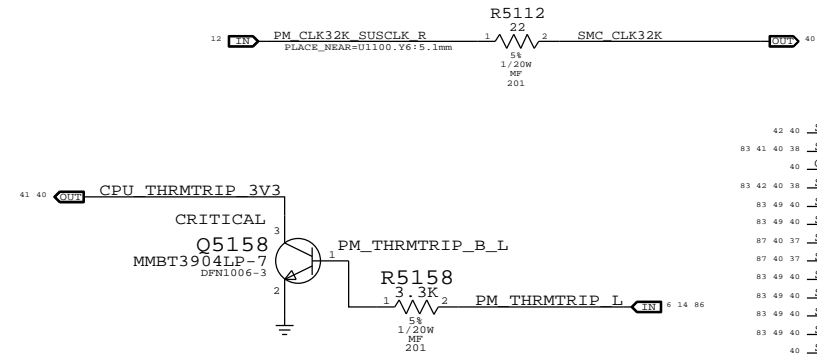
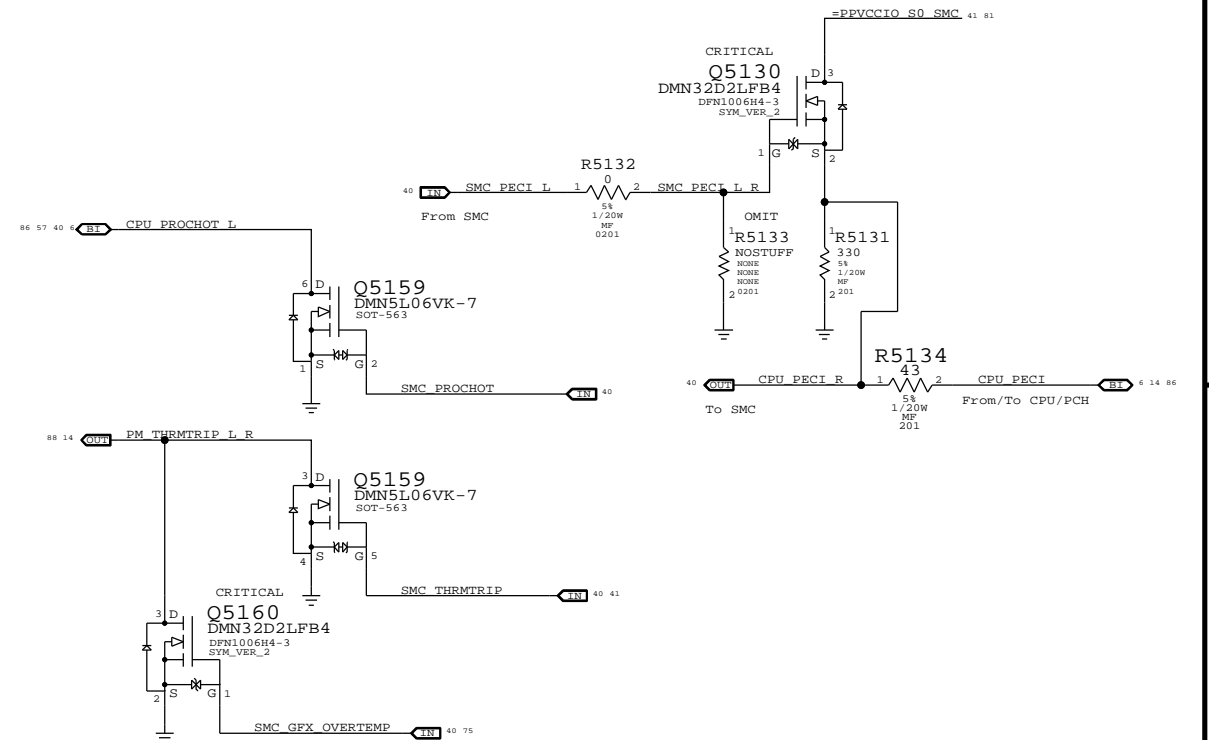


SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES: 5,6,8,10,12,16,18,20,24,25 MHZ

SMC12 PECEI SUPPORT



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

SMC Shared Support

Apple Inc.

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REVISION: 6.0.0

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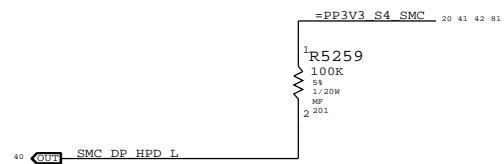
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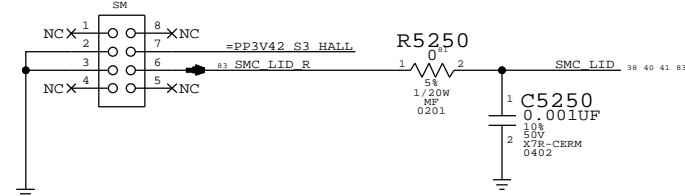
56	=CHGR_ACOK	== SMC_BC_ACOK	40 41 55	40	_ENET_ASF_GPIO	== NC_ENET_ASF_GPIO	
		MAKE_BASE=TRUE				MAKE_BASE=TRUE NO_TEST=TRUE	
40	HISIDE_ISENSE_OC	== NC_HISIDE_ISENSE_OC		40	_SMC_SYS_LED	== NC_SMC_SYS_LED	
		MAKE_BASE=TRUE NO_TEST=TRUE				MAKE_BASE=TRUE NO_TEST=TRUE	
40	_SMC_ADC0	== SMC_CPUPKG_VSENSE	45	40	_MEM_EVENT_L	== NC_MEM_EVENT_L	
		MAKE_BASE=TRUE				MAKE_BASE=TRUE NO_TEST=TRUE	
40	_SMC_ADC1	== SMC_CPUPKG_ISENSE	45	40	_SMC_ODD_DETECT	== NC_SMC_ODD_DETECT	
		MAKE_BASE=TRUE				MAKE_BASE=TRUE NO_TEST=TRUE	
40	_SMC_ADC2	== SMC_GPU_HI_ISENSE	44	40	_IR_RX_OUT_RC	== NC_IR_RX_OUT_RC	
		MAKE_BASE=TRUE NO_TEST=TRUE				MAKE_BASE=TRUE NO_TEST=TRUE	
40	_SMC_ADC3	== SMC_DCIN_VSENSE	44	40	_SYS_TDM_ONEWIRE	== NC_SYS_TDM_ONEWIRE	
		MAKE_BASE=TRUE				MAKE_BASE=TRUE NO_TEST=TRUE	
40	_SMC_ADC4	== SMC_DCIN_ISENSE	44				
		MAKE_BASE=TRUE					
40	_SMC_ADC5	== SMC_PBUS_VSENSE	44				
		MAKE_BASE=TRUE					
40	_SMC_ADC6	== SMC_SSD_ISENSE	45				
		MAKE_BASE=TRUE					
40	_SMC_ADC7	== SMC_CHGR_BMON_ISENSE	44				
		MAKE_BASE=TRUE					
40	_SMC_ADC8	== SMC_CPU_HI_ISENSE	44				
		MAKE_BASE=TRUE					
40	_SMC_ADC9	== SMC_OTHER3V3_HI_ISENSE	44				
		MAKE_BASE=TRUE					
40	_SMC_ADC10	== SMC_PLV35MEM_ISENSE	45				
		MAKE_BASE=TRUE					
40	_SMC_ADC11	== SMC_CPUDDR_ISENSE	46				
		MAKE_BASE=TRUE NO_TEST=TRUE					
40	_SMC_ADC12	== SMC_LCDPANEL_ISENSE	46				
		MAKE_BASE=TRUE					
40	_SMC_ADC13	== SMC_OTHER5V_HI_ISENSE	44				
		MAKE_BASE=TRUE NO_TEST=TRUE					
40	_SMC_ADC14	== SMC_GPUCORE_VSENSE	45				
		MAKE_BASE=TRUE					
40	_SMC_ADC15	== SMC_GPUCORE_ISENSE	46				
		MAKE_BASE=TRUE					
40	_SMC_ADC16	== NC_SMC_ADC16					
		MAKE_BASE=TRUE NO_TEST=TRUE					
40	_SMC_ADC17	== SMC_LCDBKLT_ISENSE	46				
		MAKE_BASE=TRUE					
40	_SMC_ADC18	== SMC_GPU_FB_VSENSE	45				
		MAKE_BASE=TRUE					
40	_SMC_ADC19	== SMC_GPU_FB_ISENSE	45				
		MAKE_BASE=TRUE					
40	_SMC_ADC20	== SMC_S2_ISENSE	46				
		MAKE_BASE=TRUE NO_TEST=TRUE					
40	_SMC_ADC21	== SMC_GPU1V05_ISENSE	46				
		MAKE_BASE=TRUE					
40	_SMC_ADC22	== SMC_X29_ISENSE	46				
		MAKE_BASE=TRUE					
40	_SMC_ADC23	== SMC_TBT_ISENSE	45				
		MAKE_BASE=TRUE					
40	_SMBUS_SMC_4_ASF_SCL	== NC_SMBUS_SMC_4_ASF_SCL					
		MAKE_BASE=TRUE NO_TEST=TRUE					
40	_SMBUS_SMC_4_ASF_SDA	== NC_SMBUS_SMC_4_ASF_SDA					
		MAKE_BASE=TRUE NO_TEST=TRUE					
92	_SMBUS_SMC_3_SCL	== NC_SMBUS_SMC_3_SCL					
		MAKE_BASE=TRUE NO_TEST=TRUE					
92	_SMBUS_SMC_3_SDA	== NC_SMBUS_SMC_3_SDA					
		MAKE_BASE=TRUE NO_TEST=TRUE					
40	_BDV_BKL_PWM	== NC_BDV_BKL_PWM					
		MAKE_BASE=TRUE NO_TEST=TRUE					
40	_SMC_PME_S4_DARK_L	== SMC_PME_SDCONN_L	20				
	MAKE_BASE=TRUE						
		==TBT_WAKE_L	28				

Spare S4 IRQ

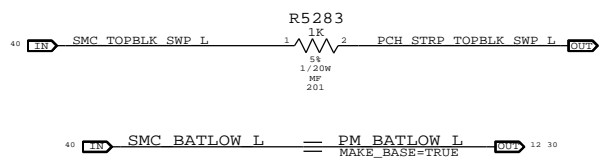
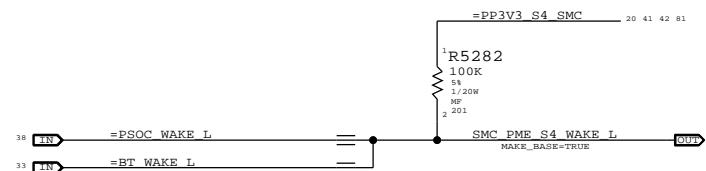


Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	



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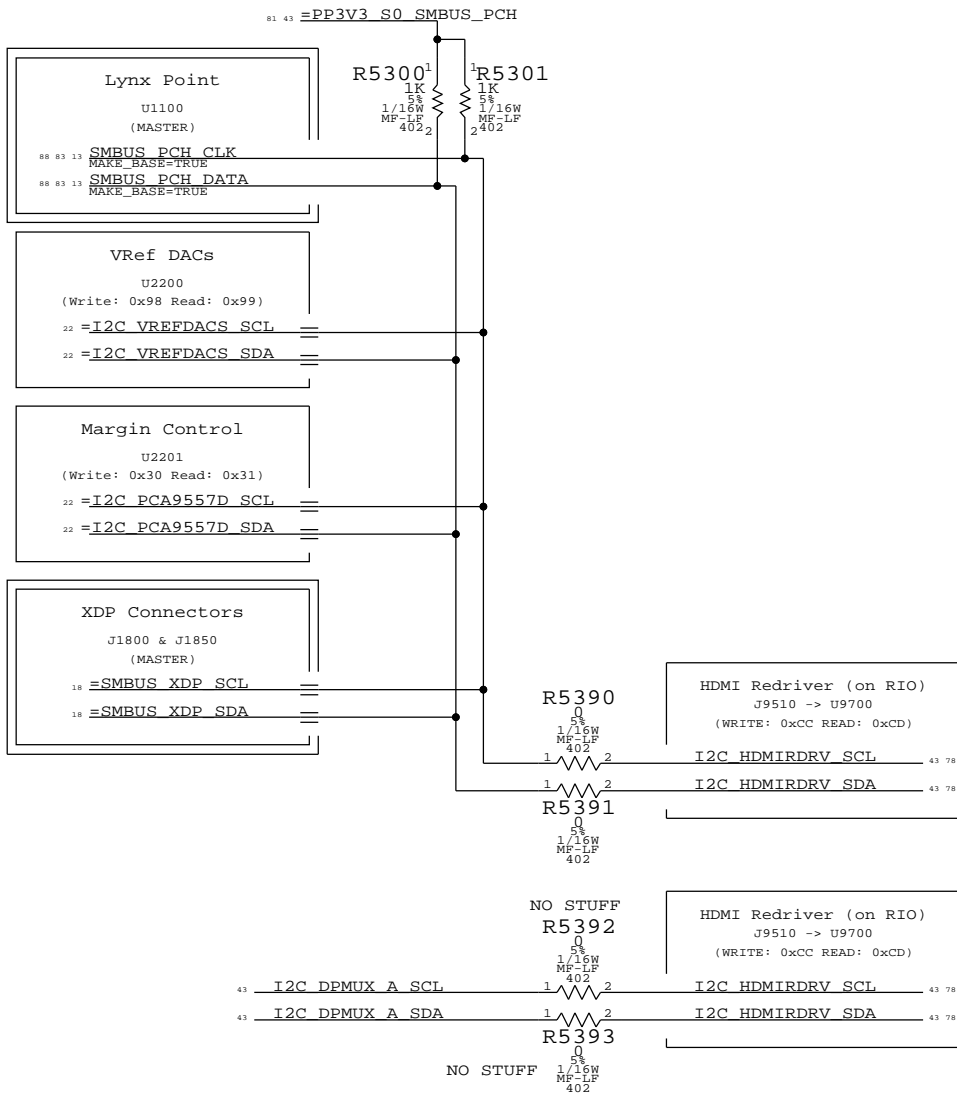
8

7

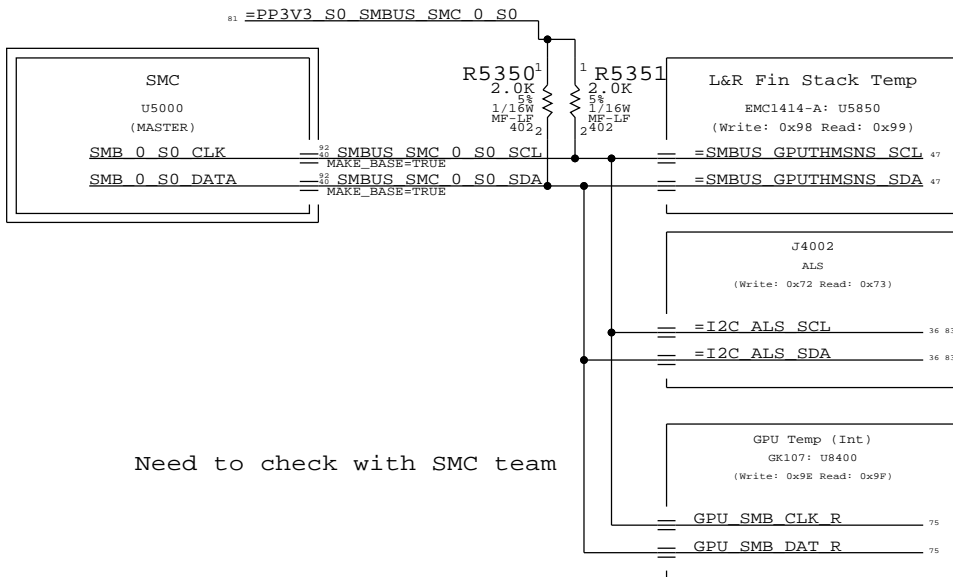
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1

PCH SMBus "0" Connections

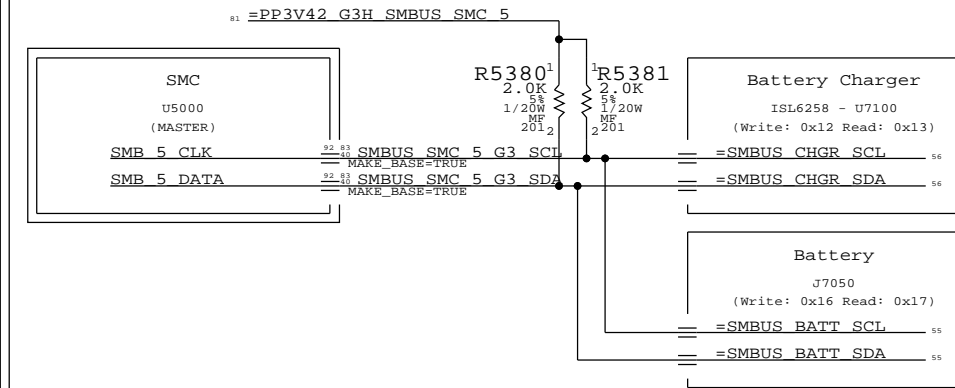


SMC "0" SMBus Connections

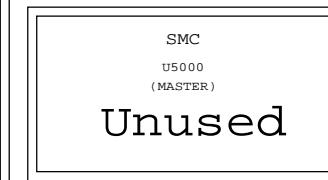


Need to check with SMC team

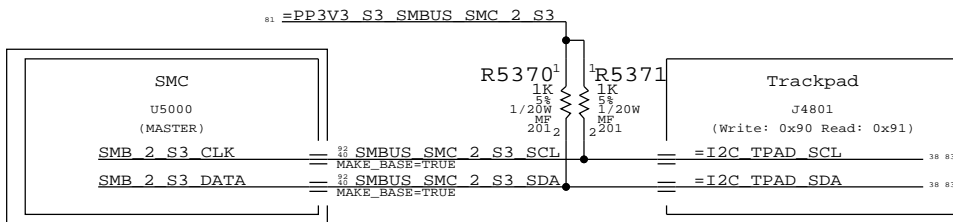
SMC "5" SMBUS CONNECTIONS



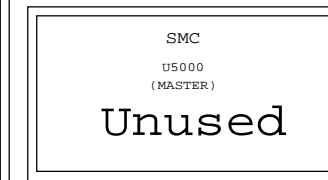
SMC "4" SMBUS CONNECTIONS



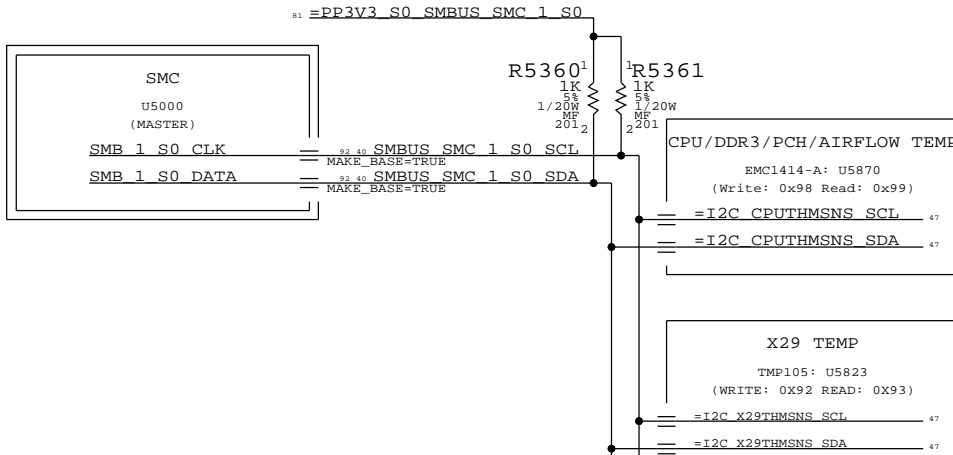
SMC "2" SMBUS CONNECTIONS



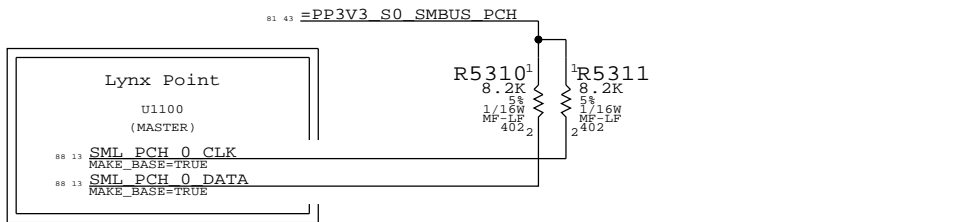
SMC "3" SMBUS CONNECTIONS



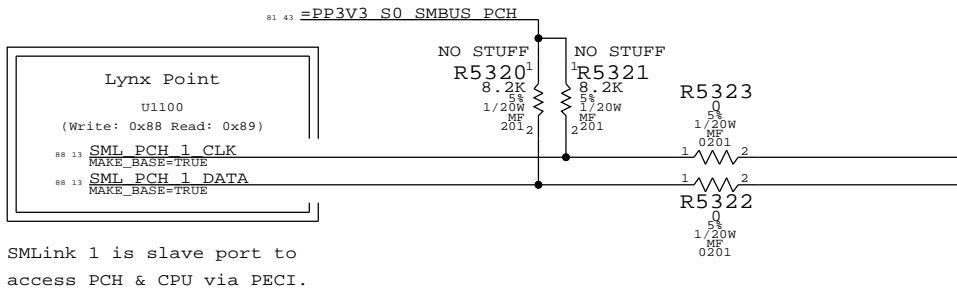
SMC "1" SMBUS CONNECTIONS



PCH "SMLink 0" Connections

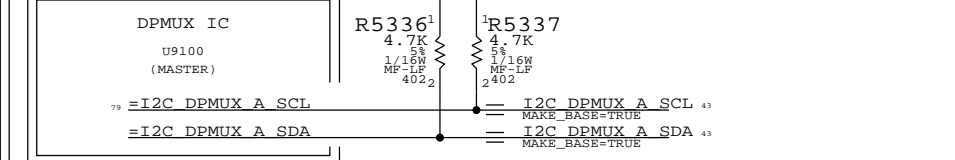


PCH "SMLink 1" Connections

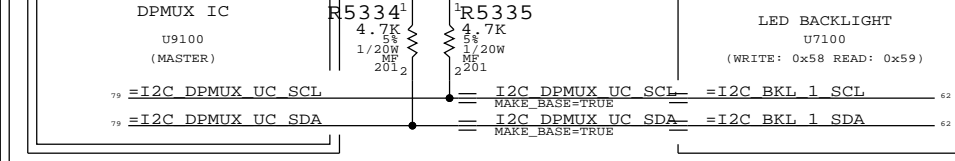


SMLink 1 is slave port to access PCH & CPU via PECl.

SMC "1" SMBUS CONNECTIONS

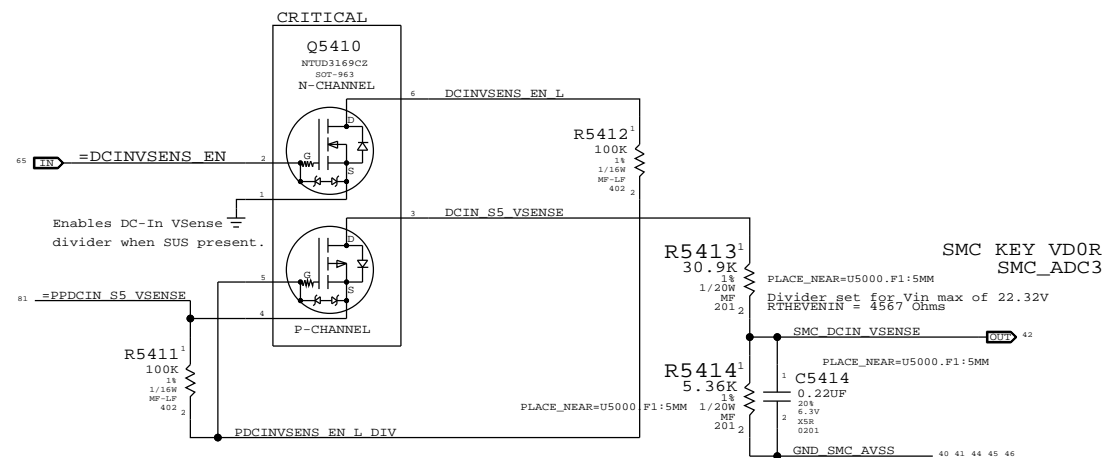


SMC "1" SMBUS CONNECTIONS

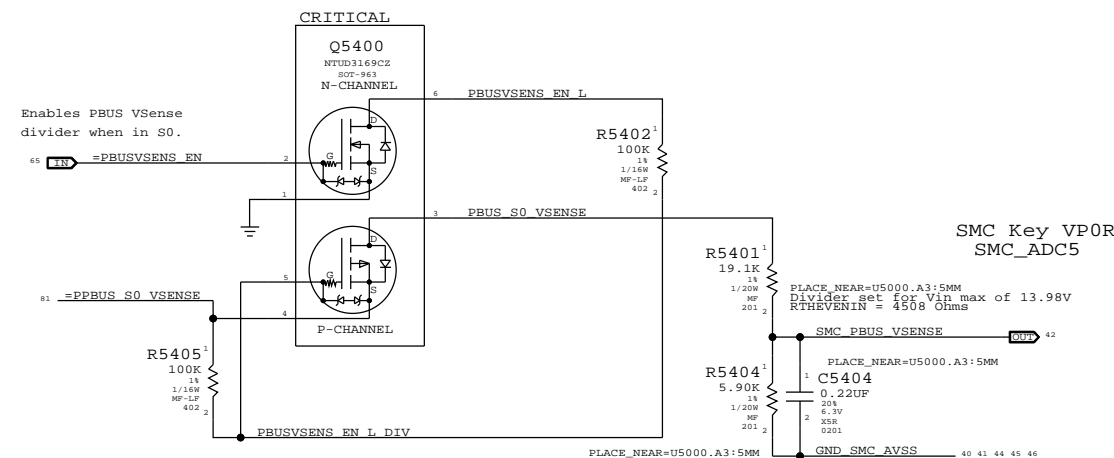


PAGE TITLE		SYNC DATE=04/26/2013	
SYNC MASTER=CLEAN J45		DRAWING NUMBER	
SMBus Connections		051-0675	
Apple Inc.		REVISION	
		6.0.0	
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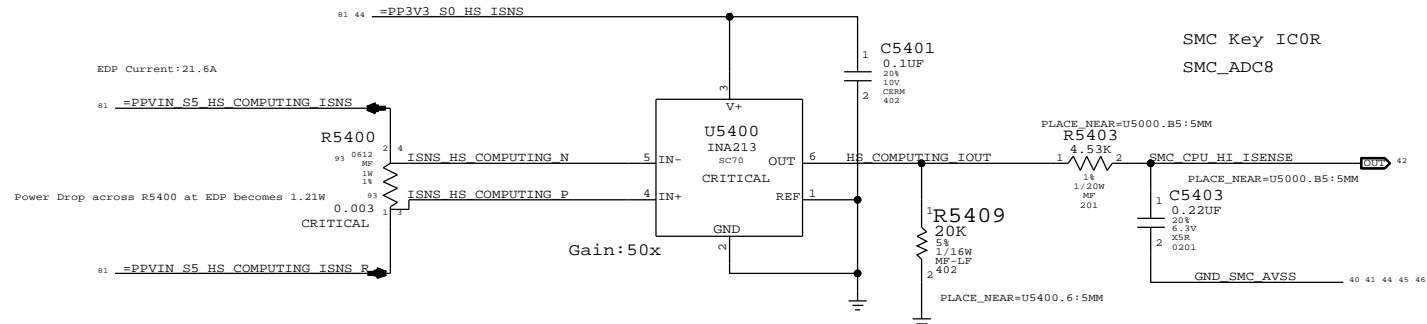
DC-In Voltage Sense Enable & Filter



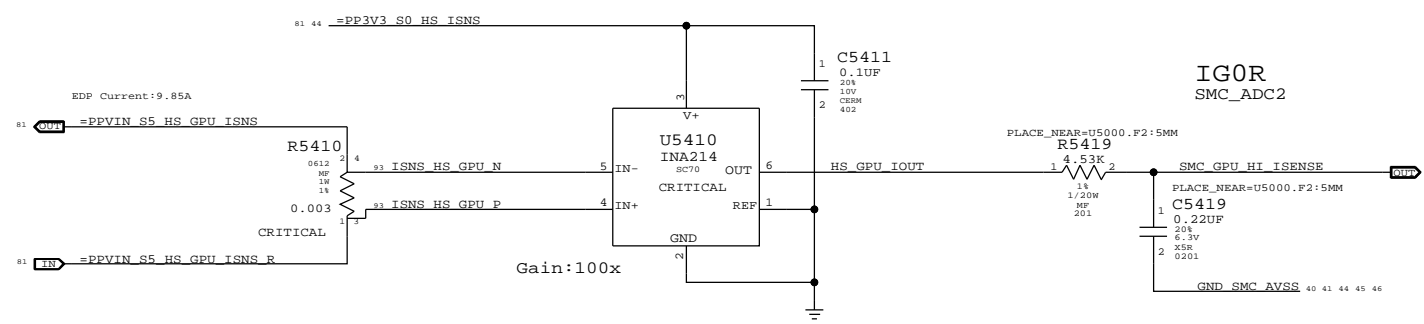
PBUS Voltage Sense Enable & Filter



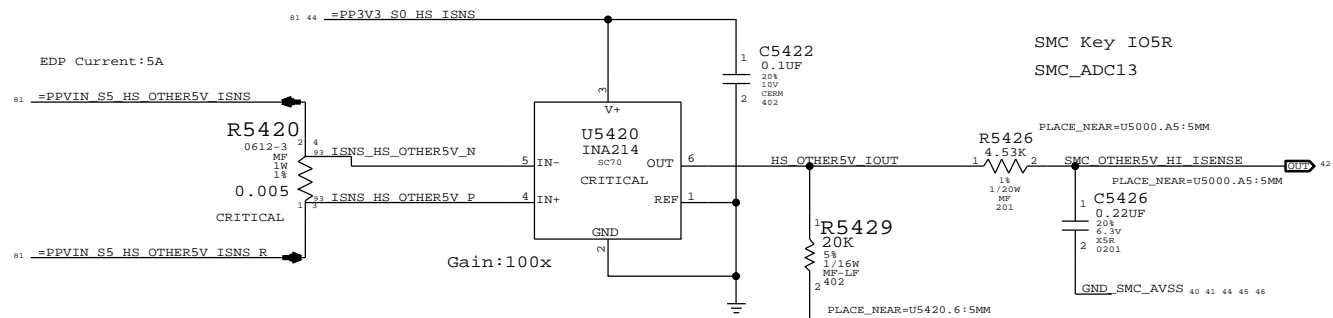
COMPUTING High Side Current Sense / Filter



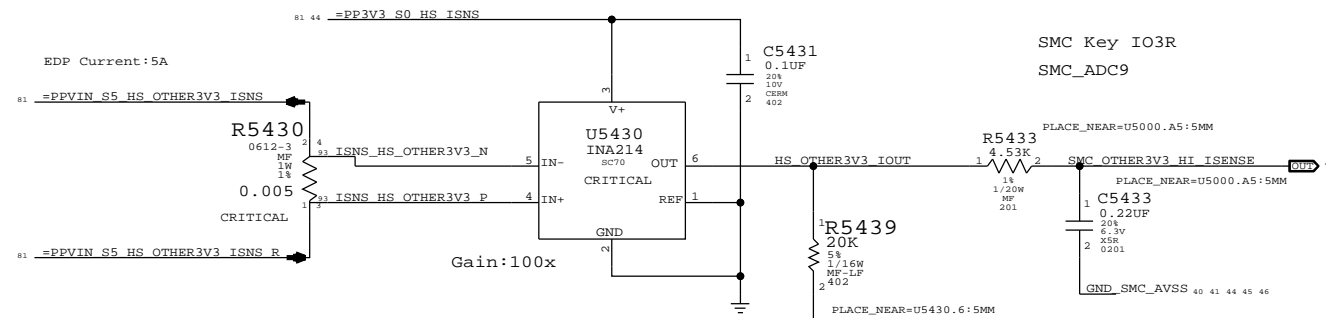
GRAPHICS High Side Current Sense / Filter



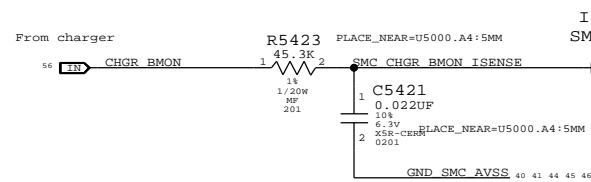
OTHERS (5V) High Side Current Sense / Filter



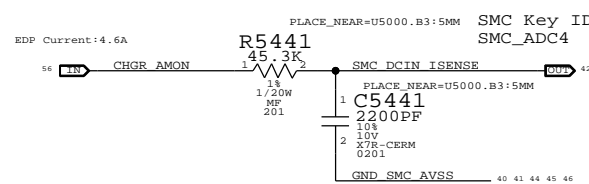
OTHERS (3.3V) High Side Current Sense / Filter



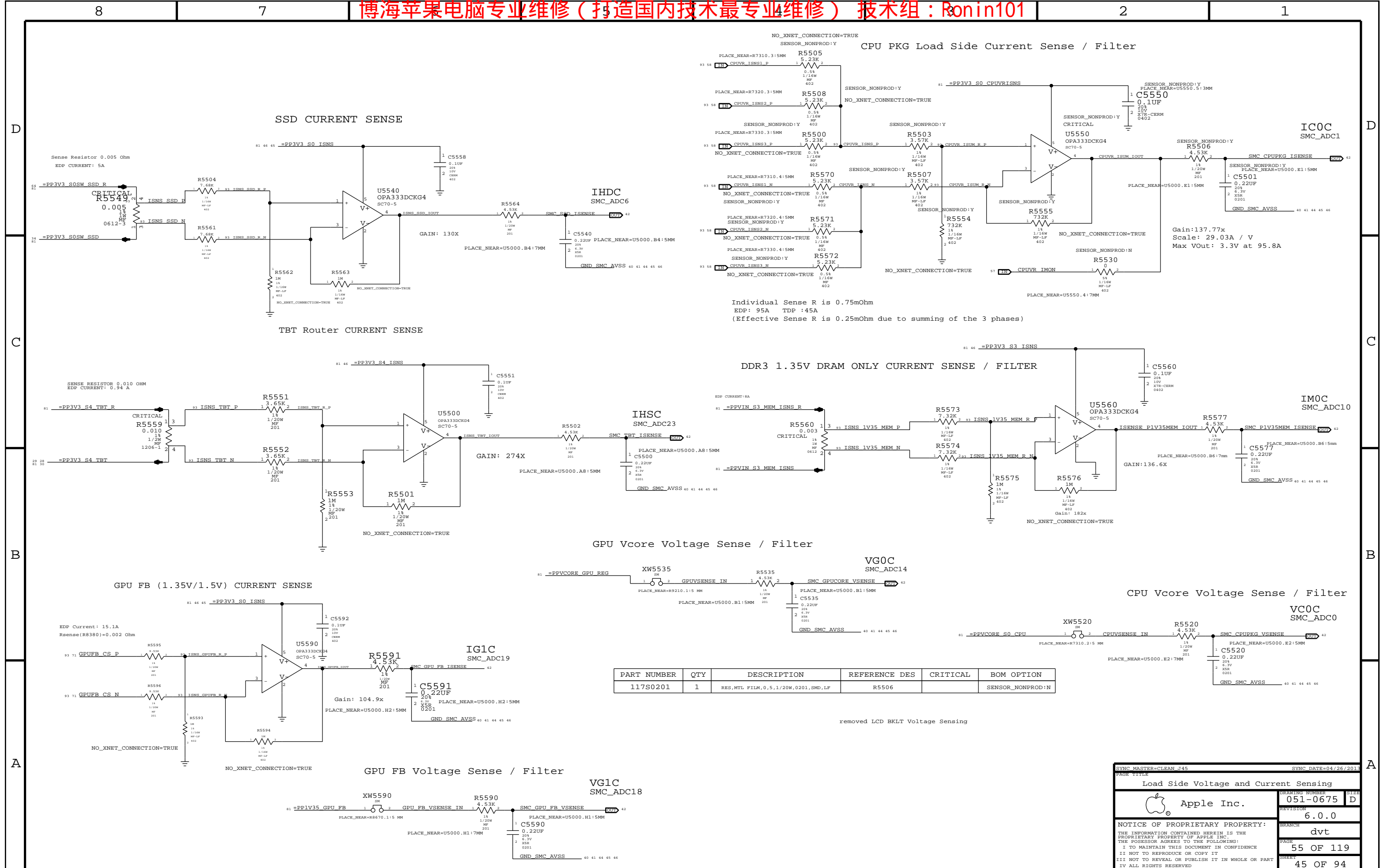
CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE			
High Side Voltage and Current Sensing			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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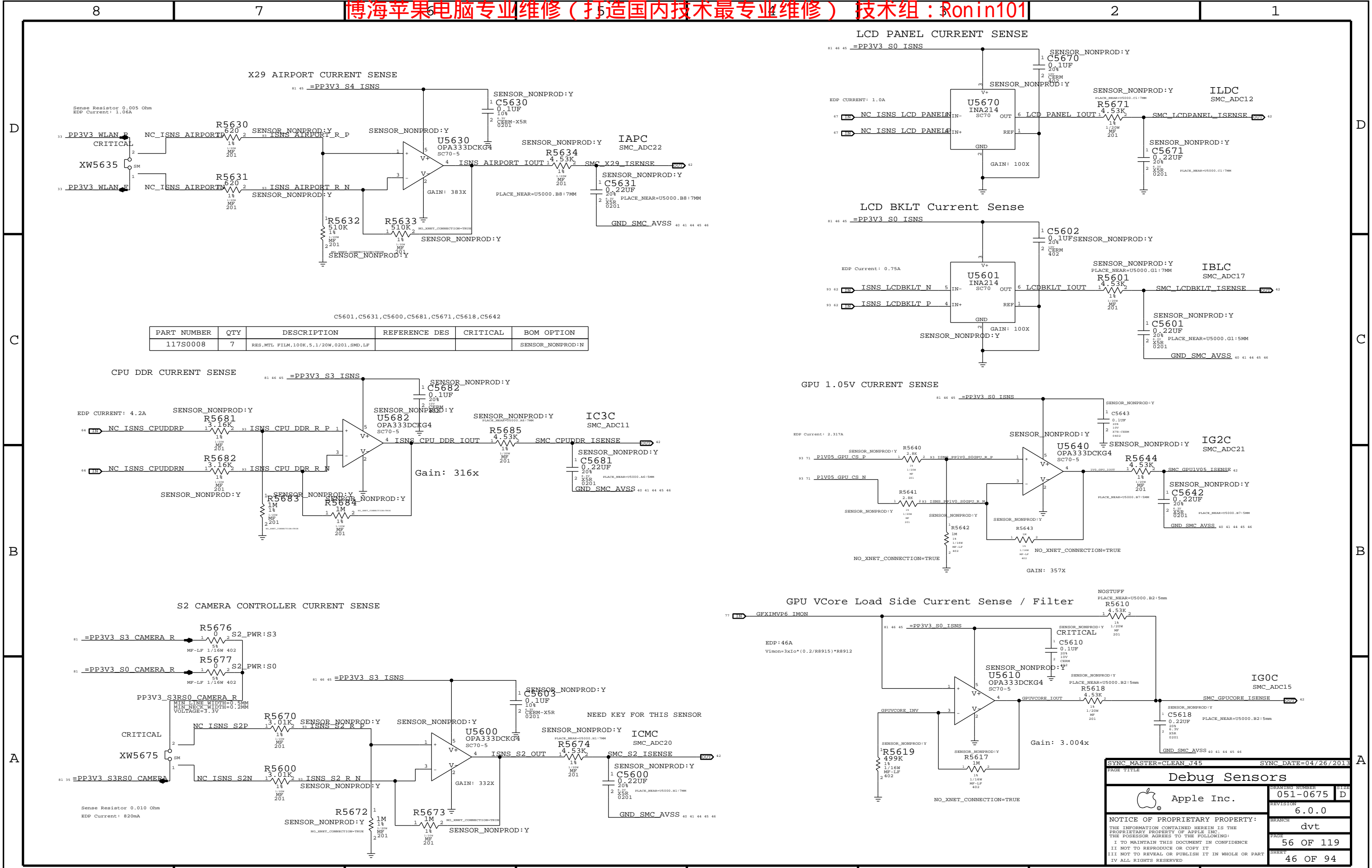
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MTL FILM,0,5,1/20W,0201,SMD,LF	R5506		SENSOR_NONPROD:N

removed LCD BKLT Voltage Sensing

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013
PAGE TITLE: Load Side Voltage and Current Sensing

Apple Inc.
DRAWING NUMBER: 051-0675
REVISION: 6.0.0
BRANCH: dvt
PAGE: 55 OF 119
SHEET: 45 OF 94

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5.1/20W,0201,SMD,LF			SENSOR_NONPROD:N

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

Apple Inc.

Debug Sensors

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

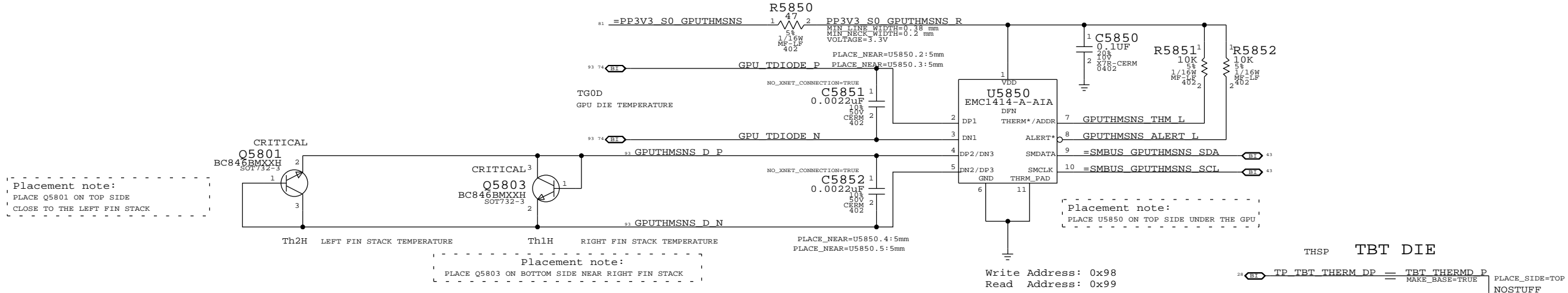
BRANCH: dvt

PAGE: 56 OF 119

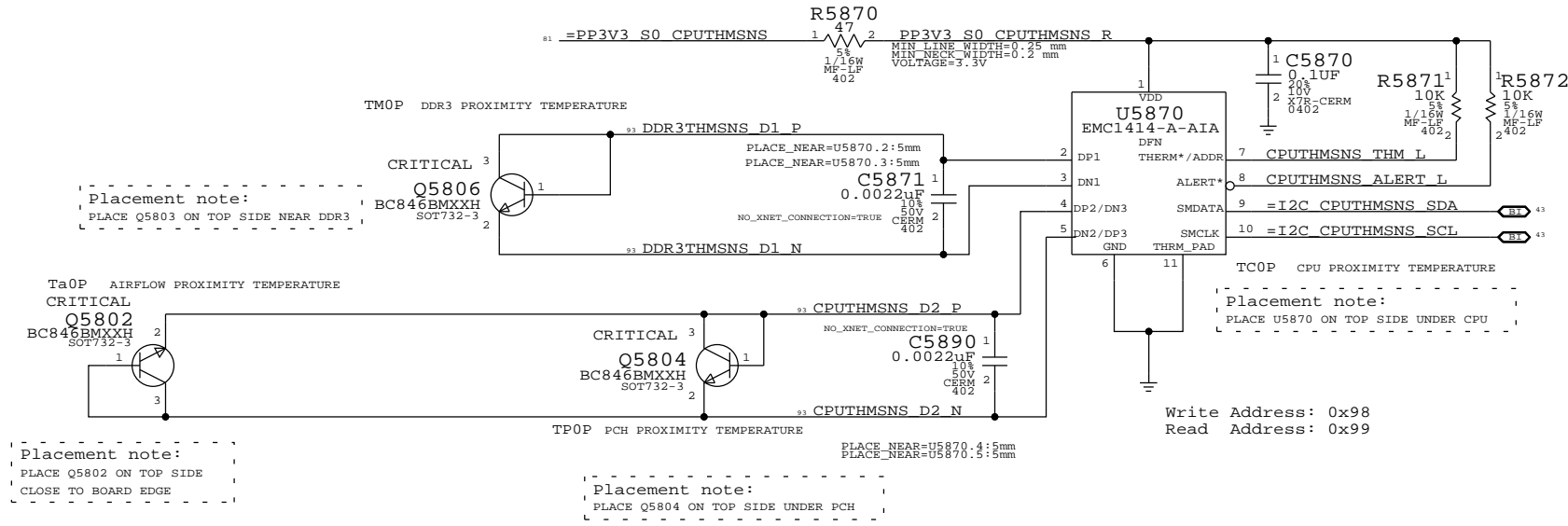
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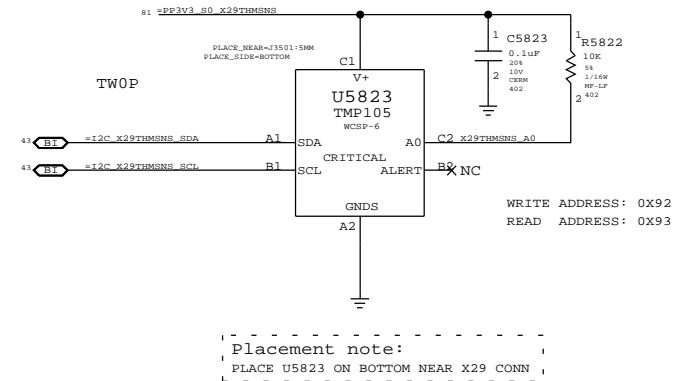
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY

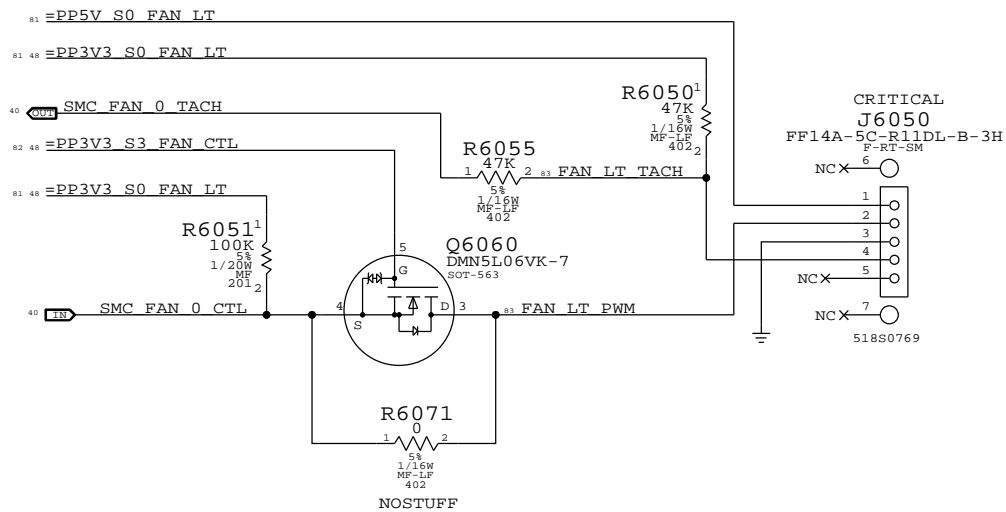


X29 PROXIMITY

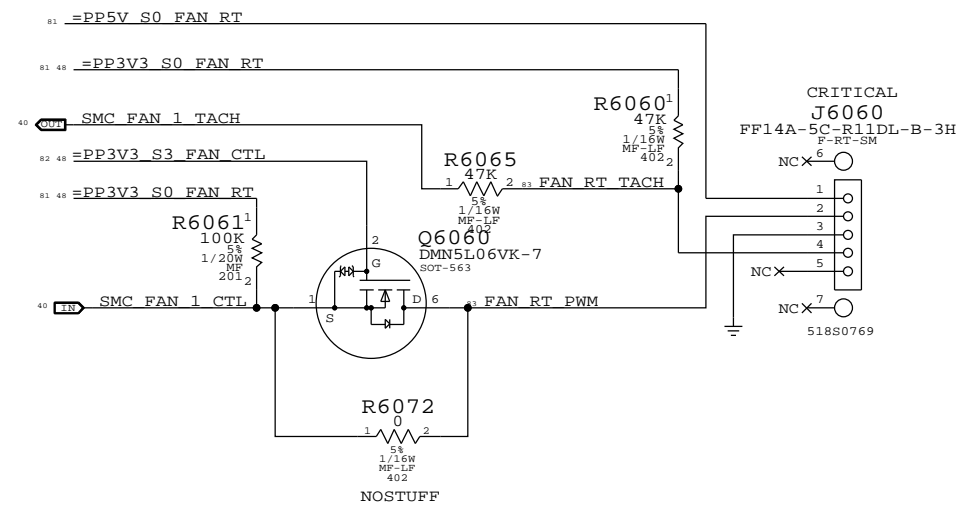


SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE Thermal Sensors			
Apple Inc.		DRAWING NUMBER 051-0675	SIZE D
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		SHEET 47 OF 94	

Left Fan

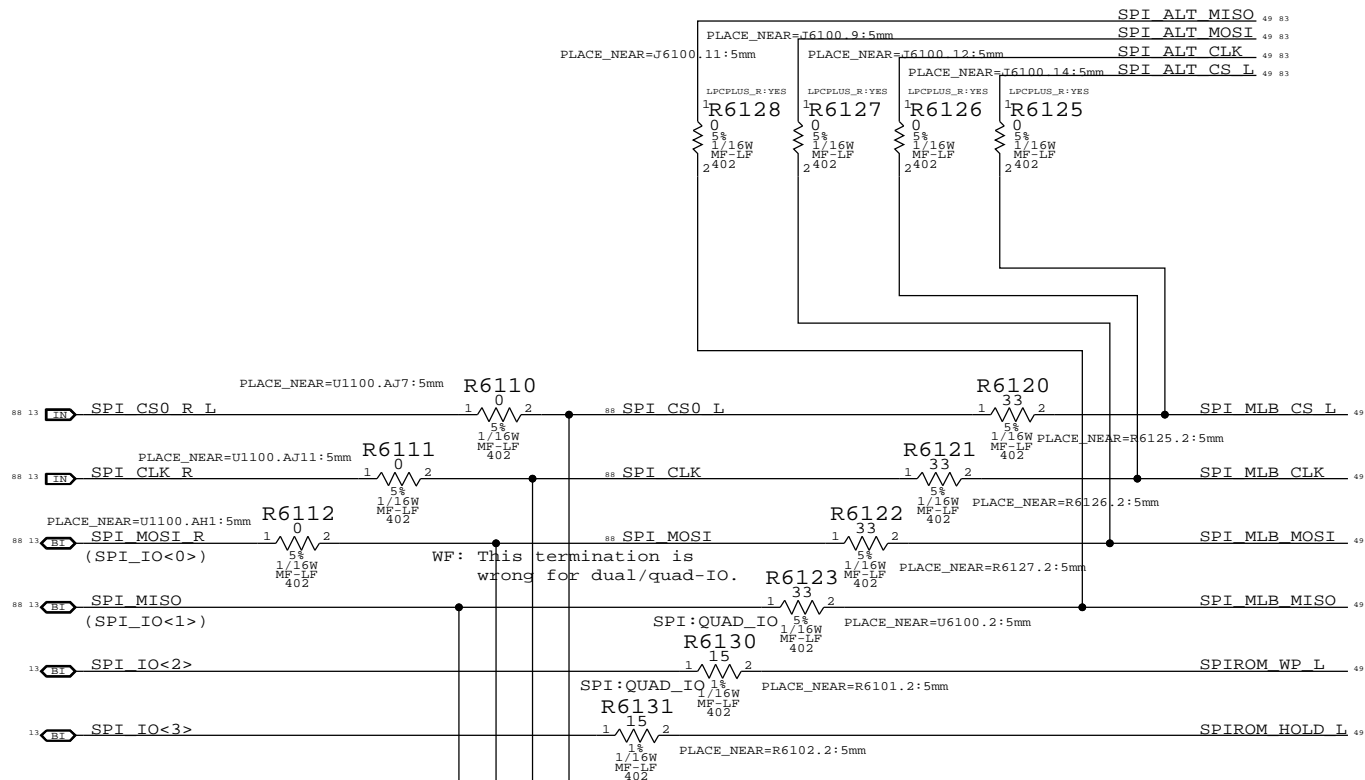


Right Fan

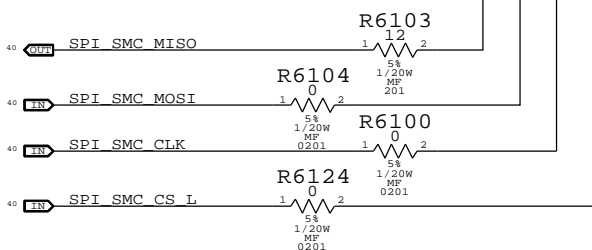


SYNC MASTER=CLEAN J45		SYNC DATE=06/23/2013	
Fan Connectors			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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		PAGE	60 OF 119
		SHEET	48 OF 94

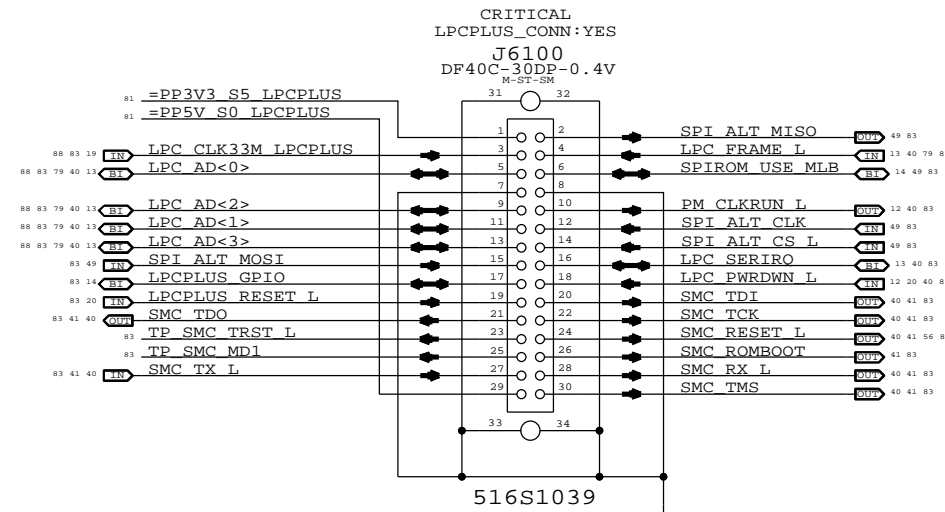
SPI Bus Series Termination



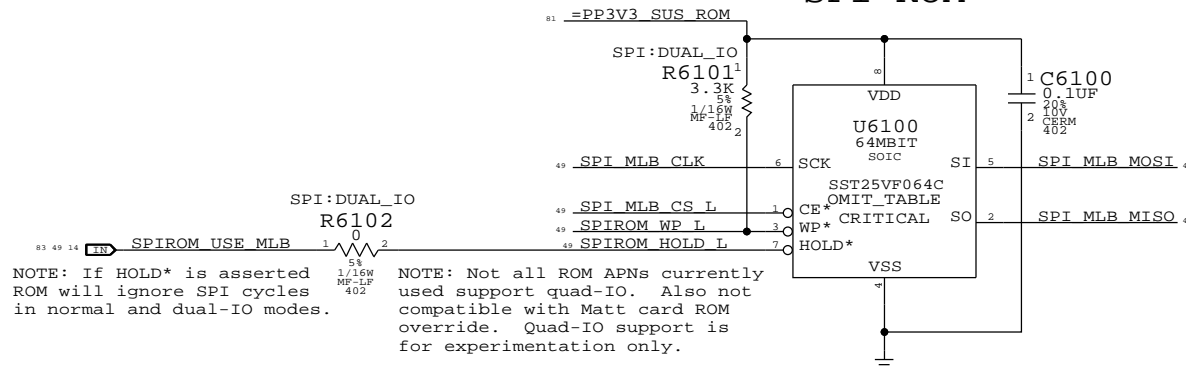
SMC12 SPI SUPPORT



LPC+SPI Connector

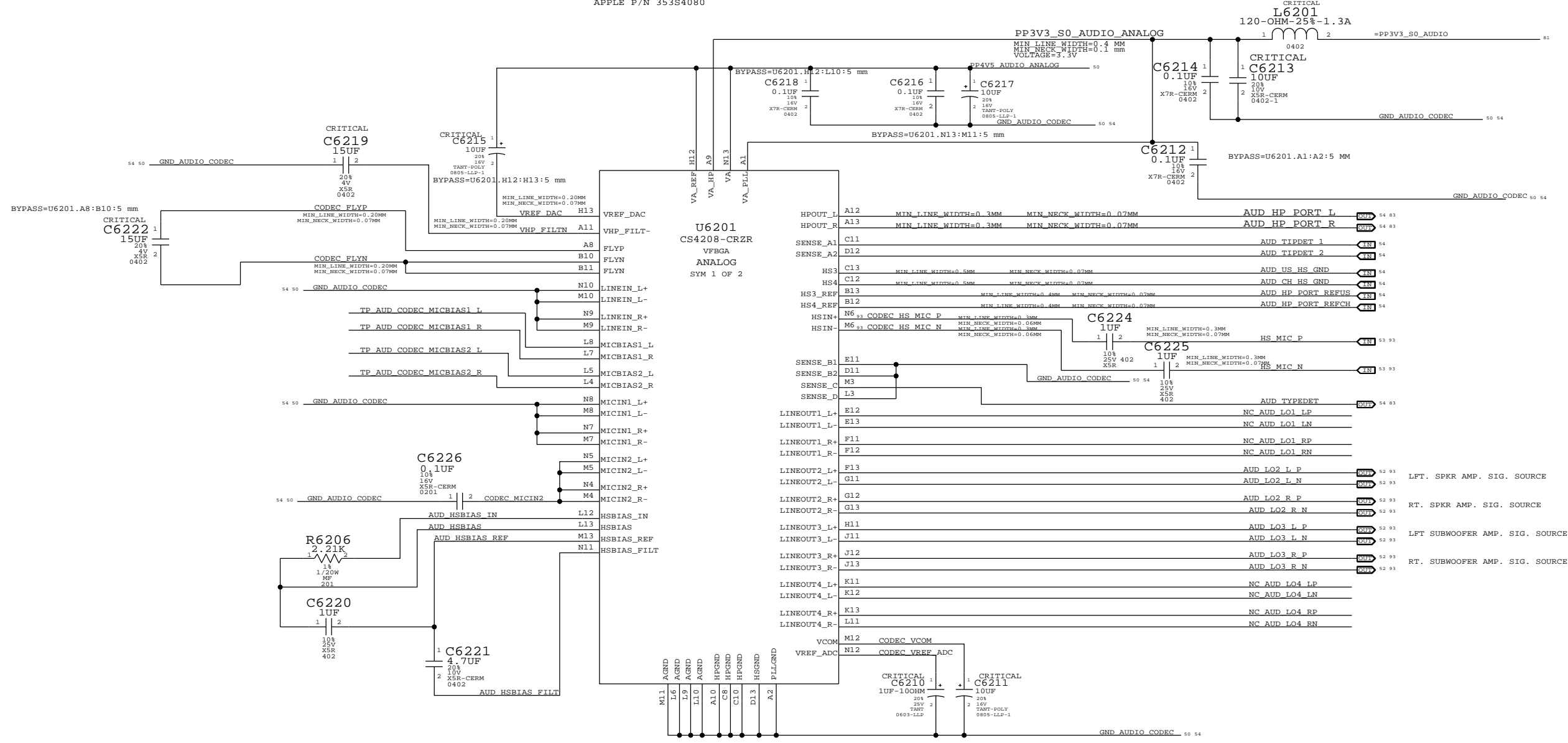


SPI ROM



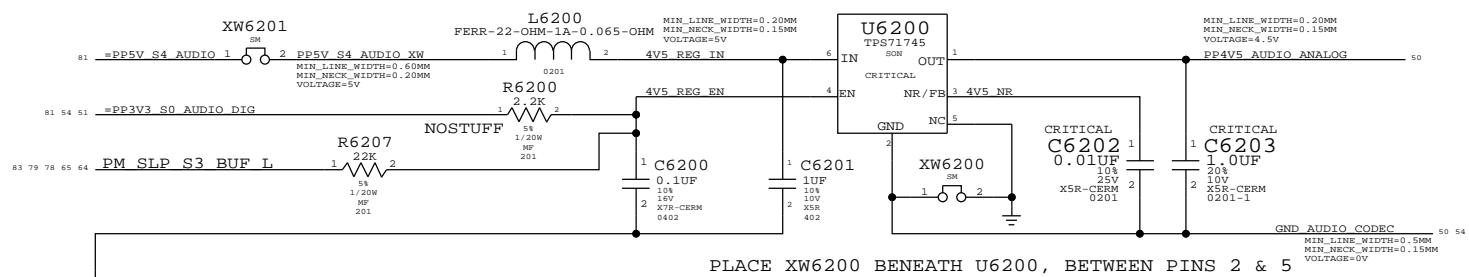
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PAGE TITLE SPI ROM / LPC+SPI Conn.			
Apple Inc.		DRAWING NUMBER 051-0675	SIZE D
		REVISION 6.0.0	
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AUDIO CODEC, ANALOG BLOCKS
APPLE P/N 353S4080



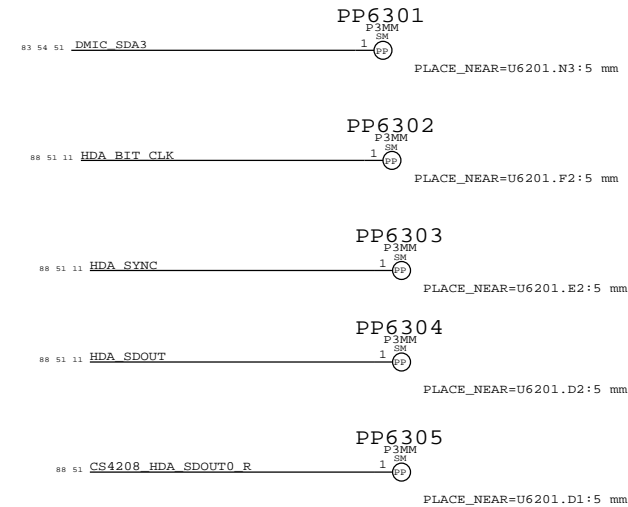
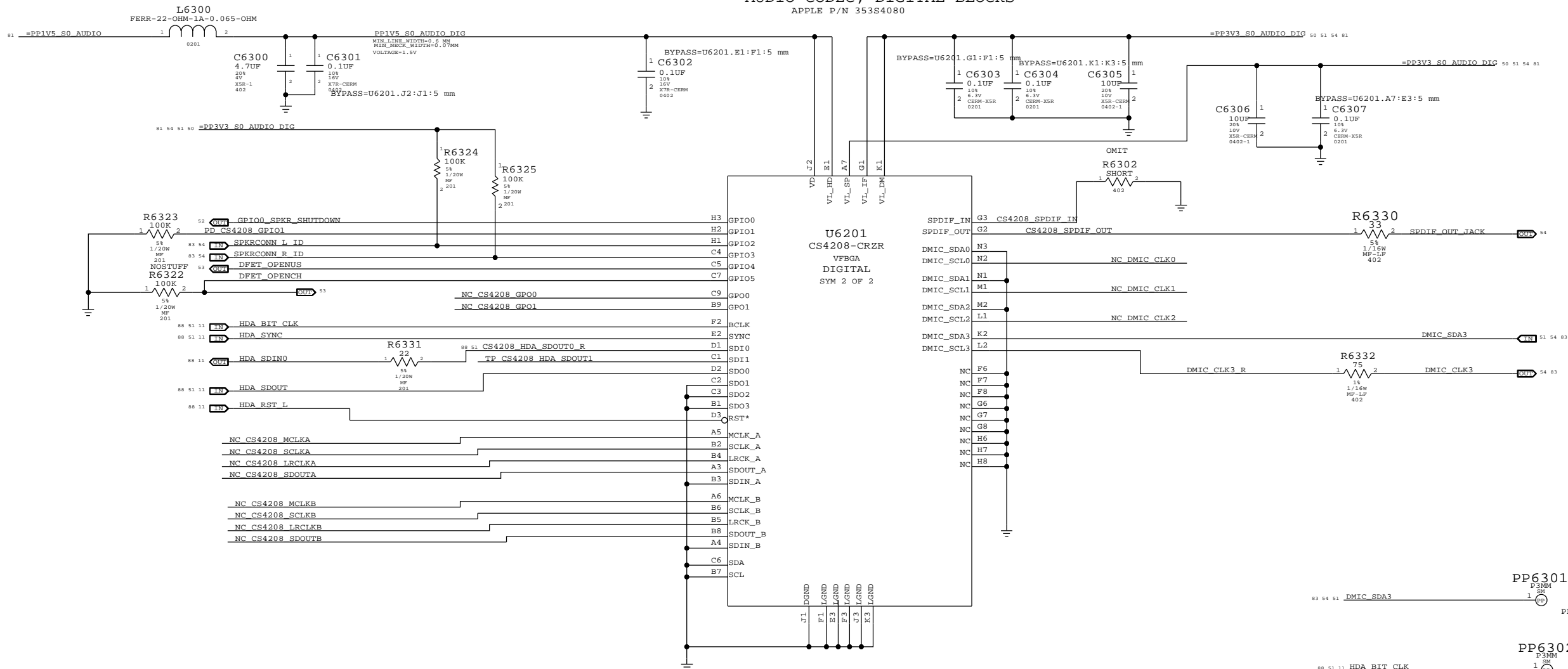
4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



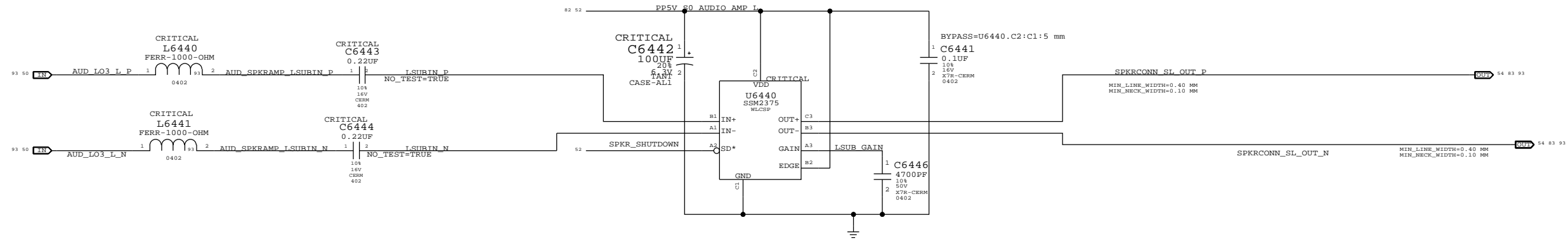
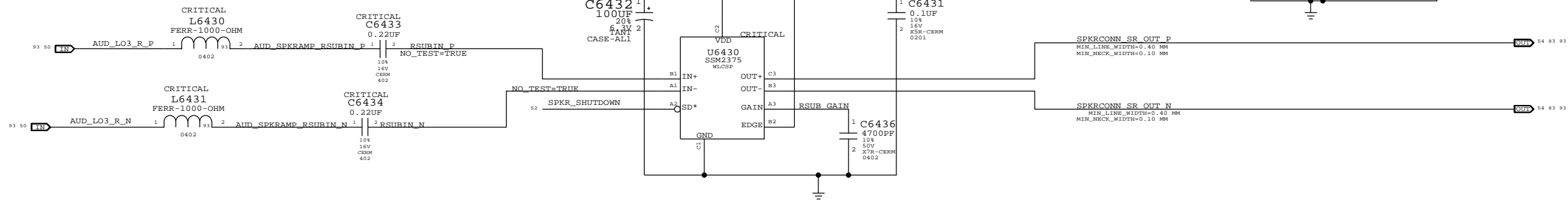
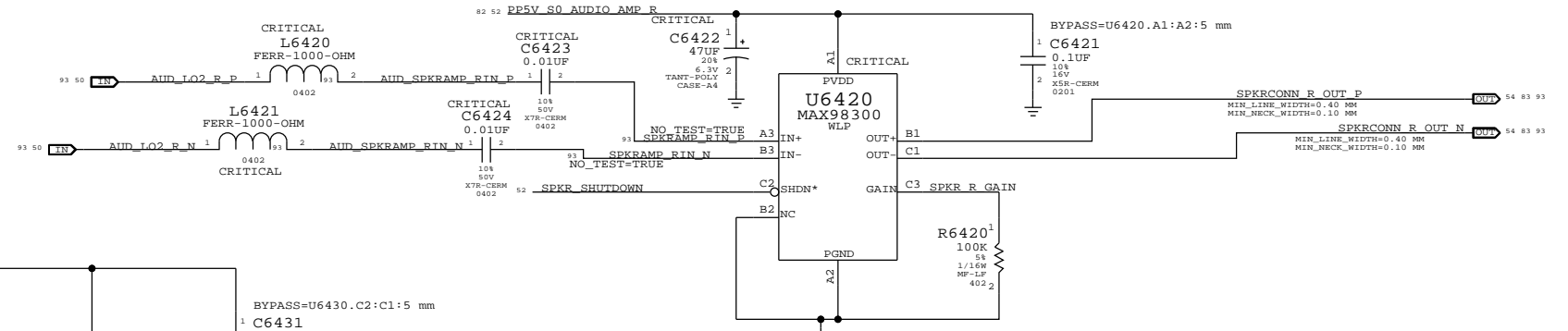
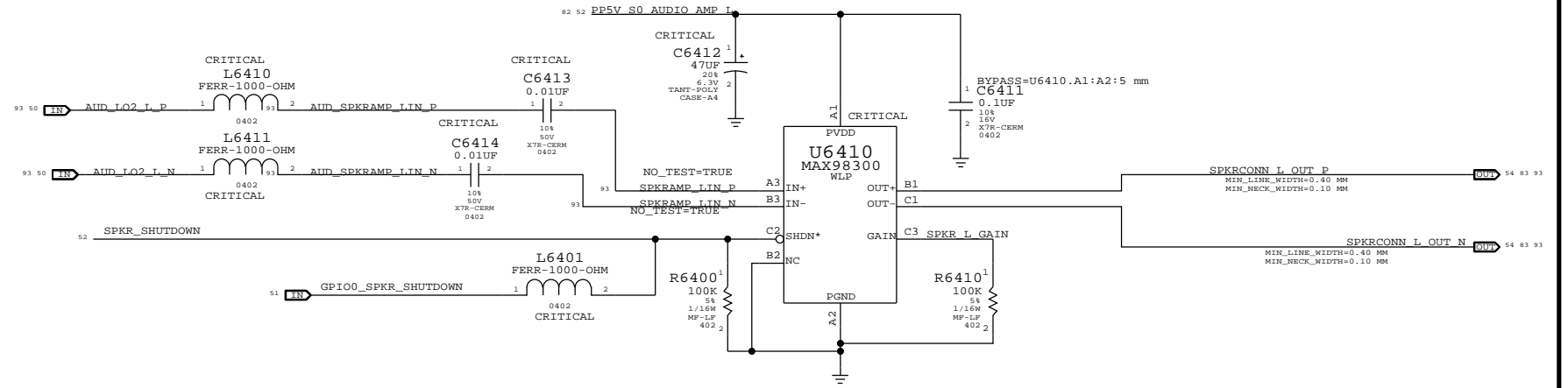
PAGE TITLE		SYNC DATE=04/26/2013	
AUDIO:CODEC, ANALOG		DRAWING NUMBER	SIZE
Apple Inc.		051-0675	D
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AUDIO CODEC, DIGITAL BLOCKS
APPLE P/N 353S4080

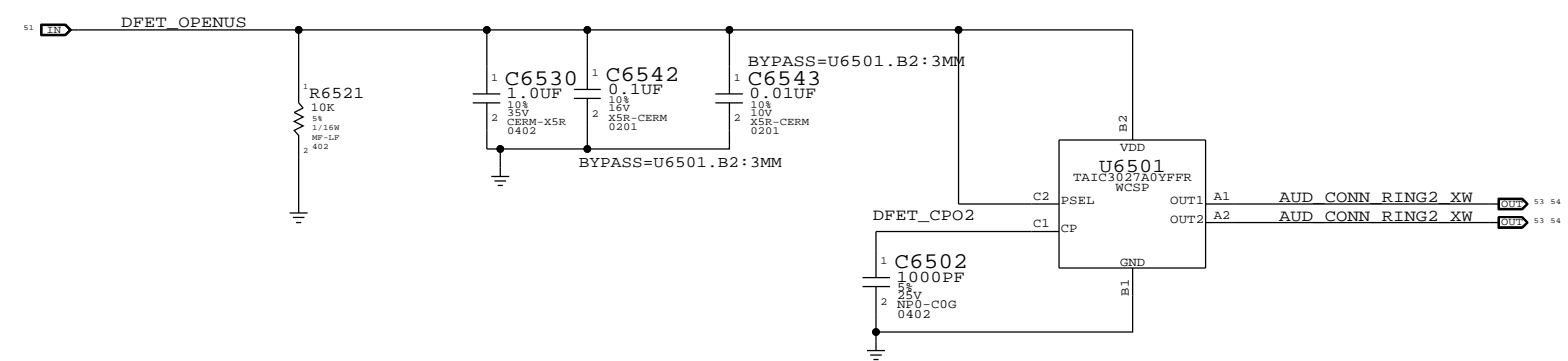
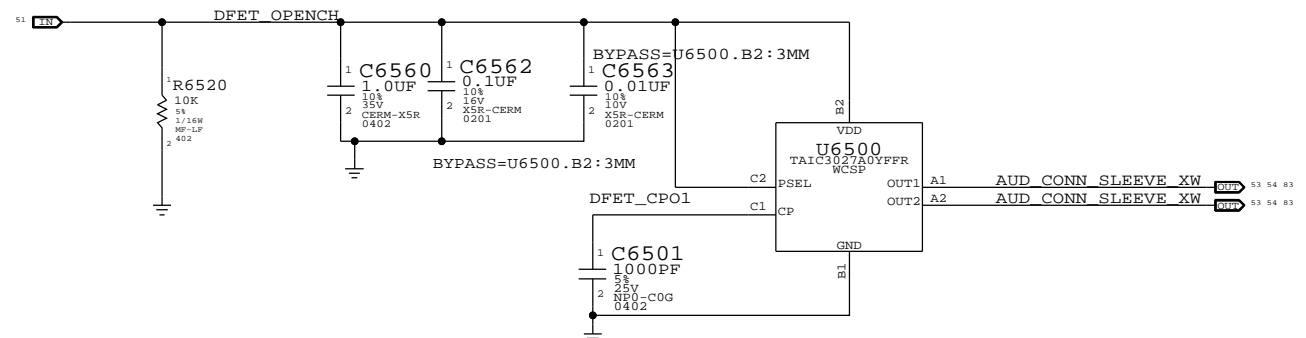
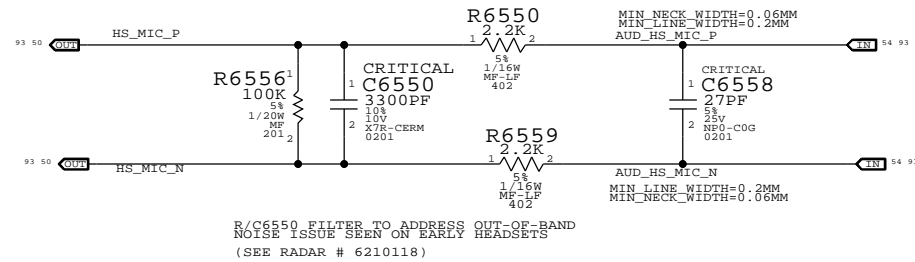


SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE AUDIO:CODEC, DIGITAL			
DRAWING NUMBER 051-0675		SIZE D	
REVISION 6.0.0		BRANCH dvt	
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4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
 APN: 353S2888 & 353S2958
 GAIN = +3 DB
 1ST ORDER FC (L&R) = NOM 569 HZ
 1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=CLEAN_J45		SYNC DATE=04/26/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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AUDIO: JACK			
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		PAGE	65 OF 119
		SHEET	53 OF 94

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPI02	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPI03	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPI04	OUTPUT	HIGH = DFET'S OPEN

2-MIC CONNECTOR
APN: 518S0769

SPEAKER CONNECTOR
HP=80HZ
APN: 518S0672

CRITICAL
J6602
78171-6006
M-RT-SM

CRITICAL
J6603
78171-6006
M-RT-SM

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

NCX

AUDIO
9 VIN
10 VDD
11 GND

OPERATING VOLTAGE 3.3
POF

SHELL
PINS

C6600
1UF
10%
10V
X5R
402-1

C6601
0.1UF
10%
6.3V
CERM-X5R
0201

R6601
10K
5%
1/16W
NP0-CERM
402

CRITICAL
DZ6607
ESDALC5-1BM2
SOD882

C6603
100PF
25V
NPO-CERM
0201

C6605
100PF
25V
NPO-CERM
0201

CRITICAL
DZ6603
ESDALC5-1BM2
SOD882

CRITICAL
DZ6606
ESDALC5-1BM2
SOD882

C6607
100PF
25V
NPO-CERM
0201

C6602
100PF
25V
NPO-CERM
0201

CRITICAL
DZ6601
ESDALC5-1BM2
SOD882

C6604
100PF
25V
NPO-CERM
0201

CRITICAL
DZ6602
ESDALC5-1BM2
SOD882

C6606
100PF
25V
NPO-CERM
0201

CRITICAL
DZ6605
ESDALC5-1BM2
SOD882

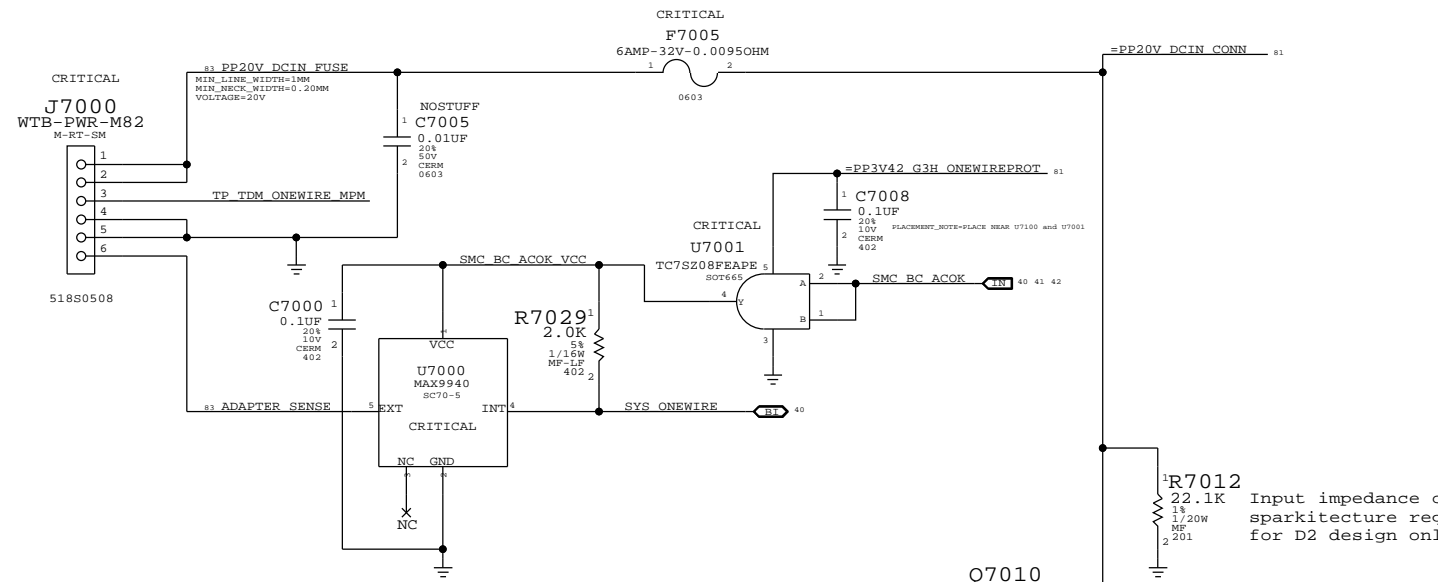
C6608
100PF
25V
NPO-CERM
0201

CRITICAL
DZ6604
ESDALC5-1BM2
SOD882

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

AUDIO: JACK TRANSLATORS		DRAWING NUMBER	051-0675	SIZE	D
Apple Inc.		REVISION	6.0.0		
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MagSafe DC Power Jack



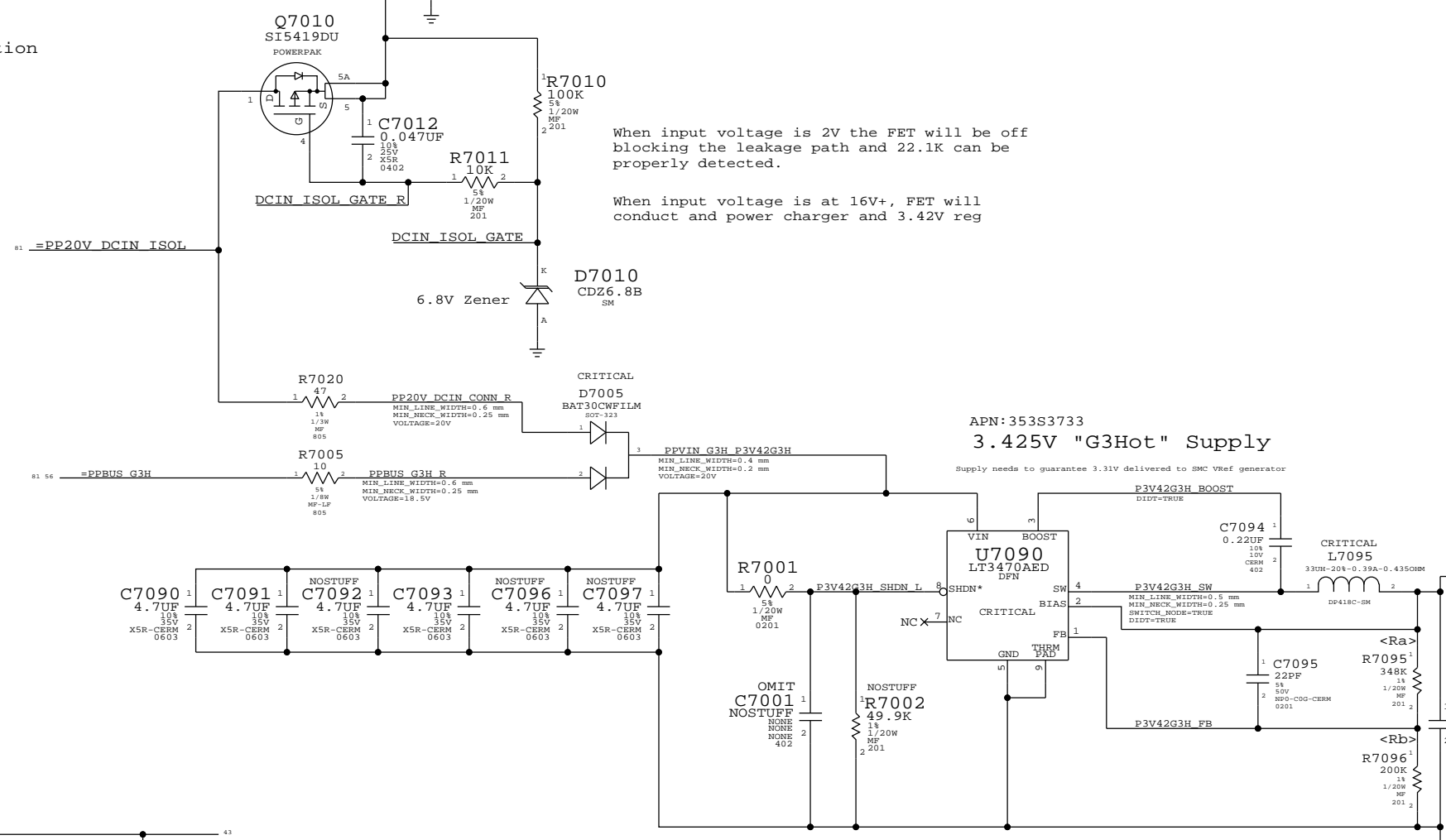
1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

Input impedance of 22.1K meets sparkiterture requirements for D2 design only

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

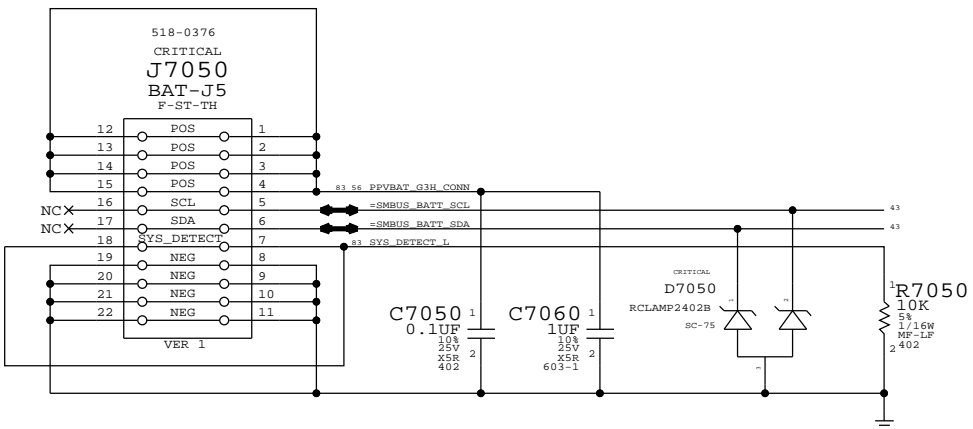


APN: 353S3733
3.425V "G3Hot" Supply

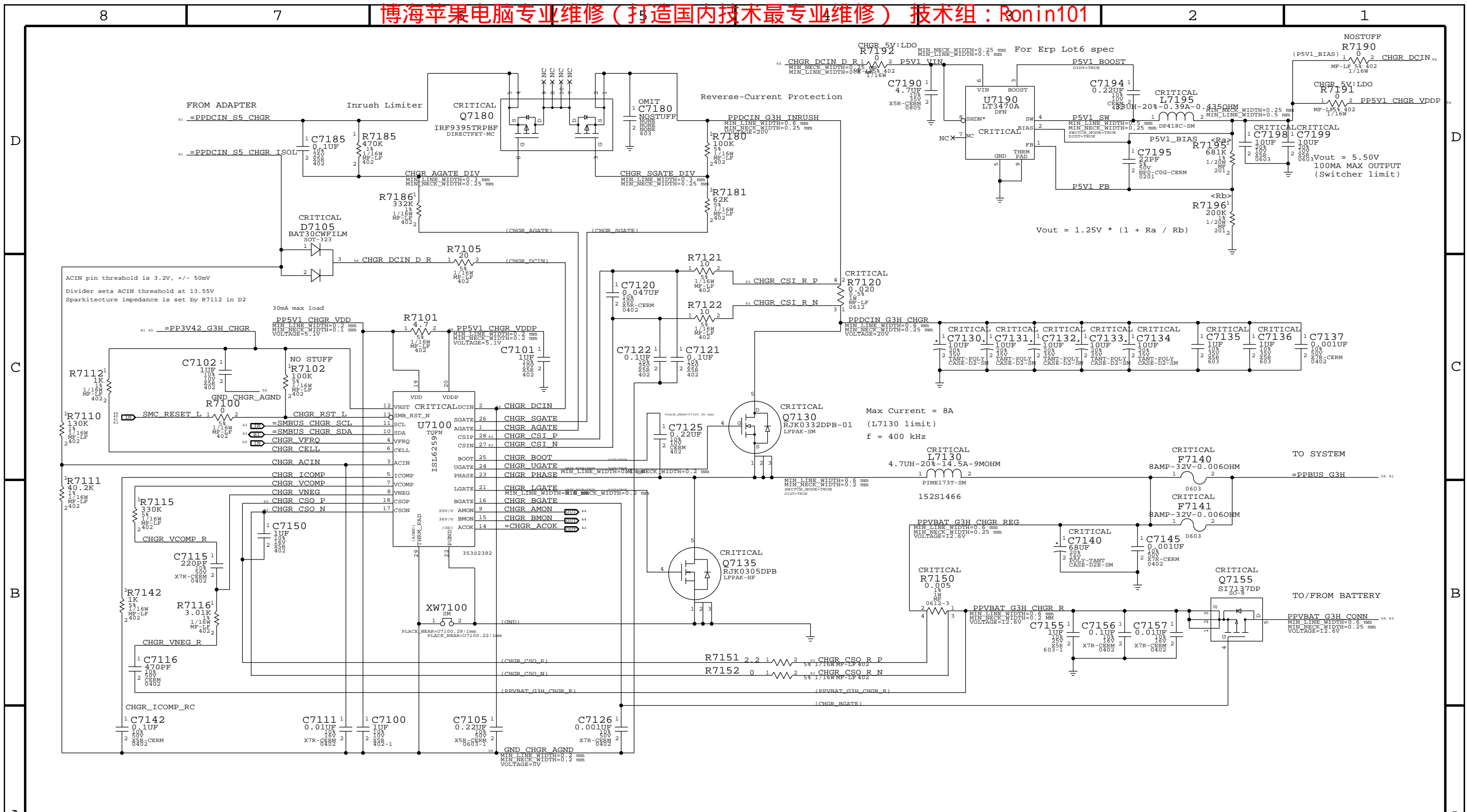
Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

$V_{out} = 1.25V * (1 + R_a / R_b)$

BATTERY CONNECTOR

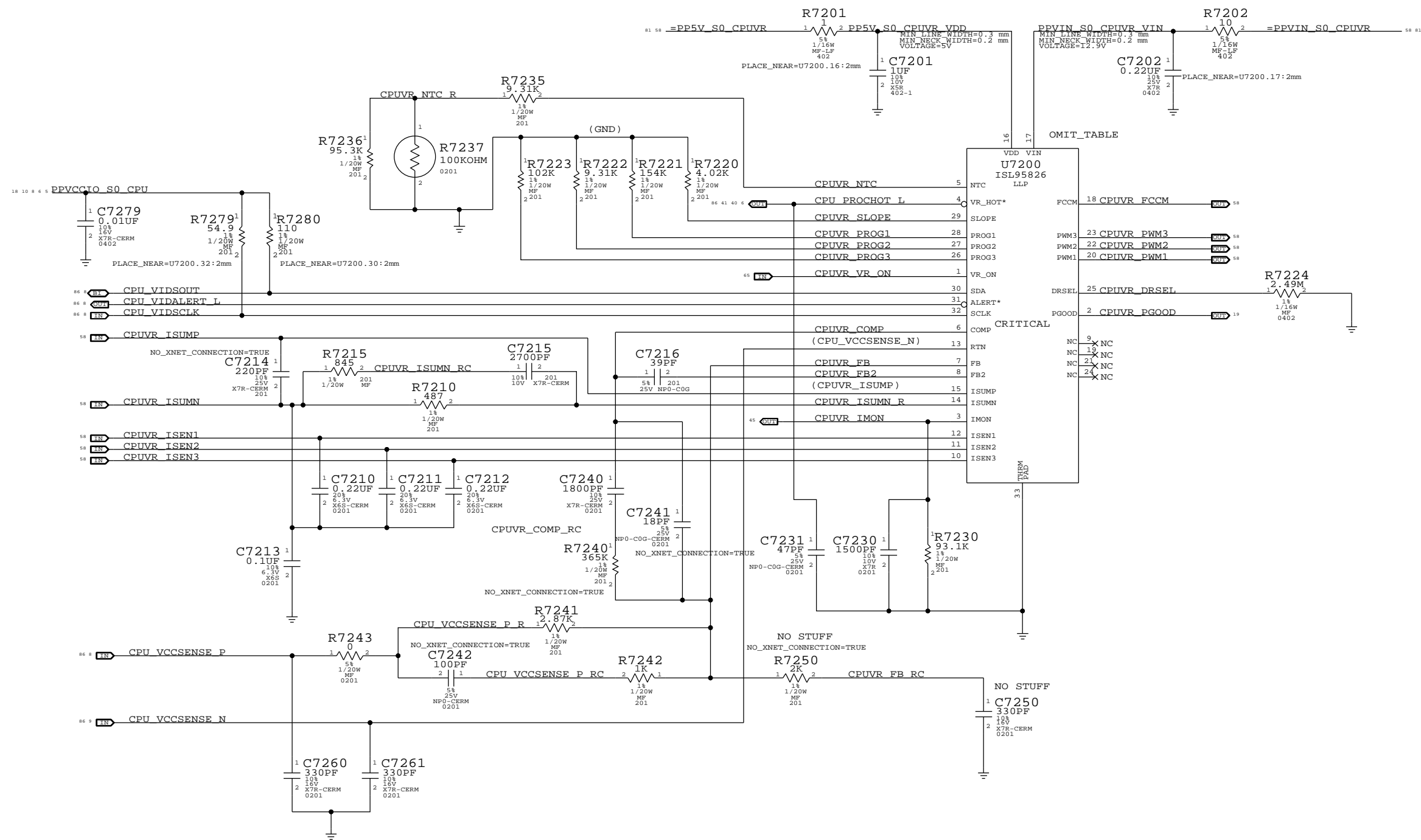


PAGE TITLE DC-In & Battery Connectors		DRAWING NUMBER 051-0675	SIZE D
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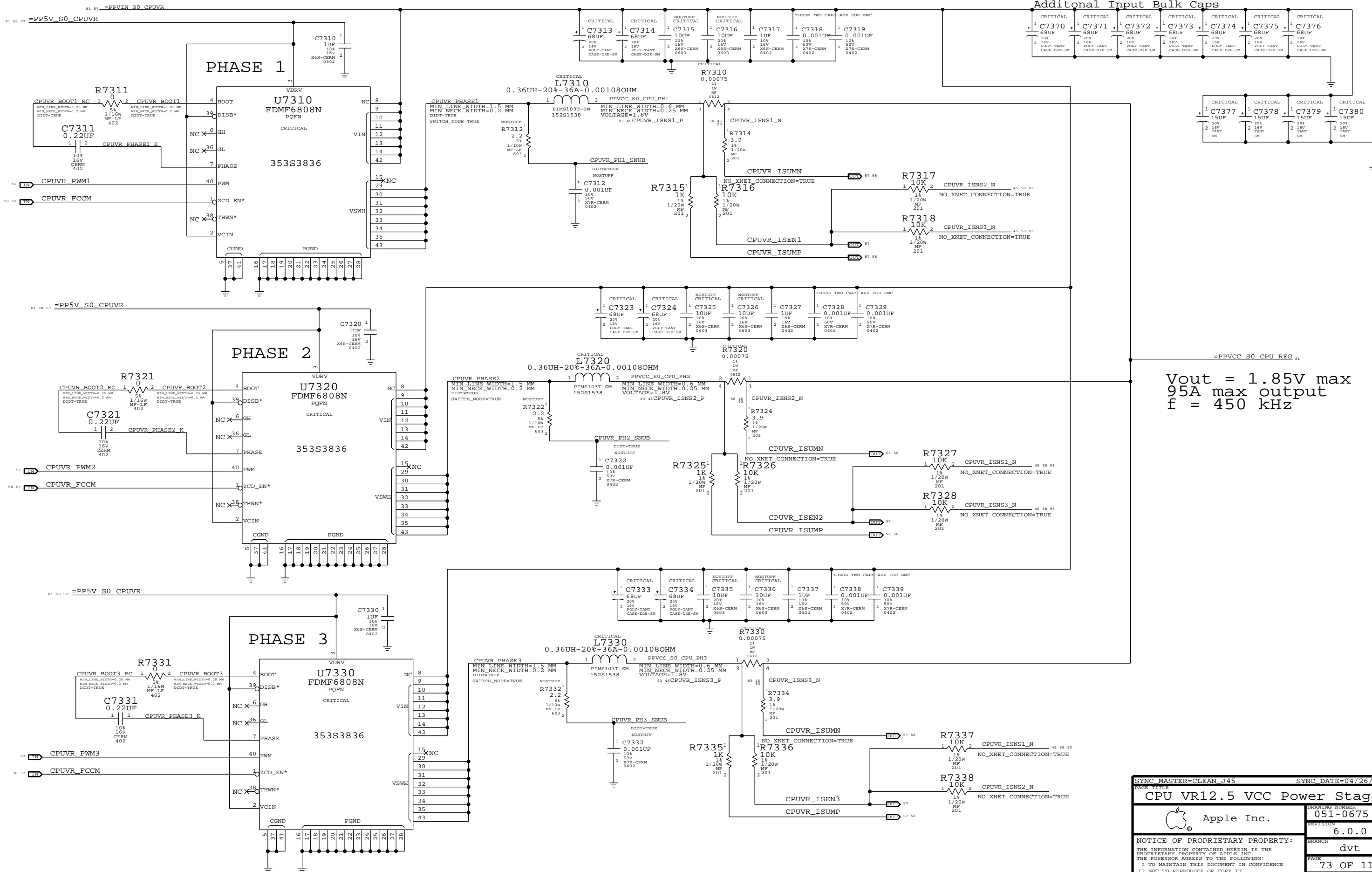


SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER	SIZE
		051-0675	D
		REVISION	
		6.0.0	
		BRANCH	
		dvt	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC, ISL95826R6200, PWM, PGOOD, SCREEN, 32P, QFN	U7200	CRITICAL	

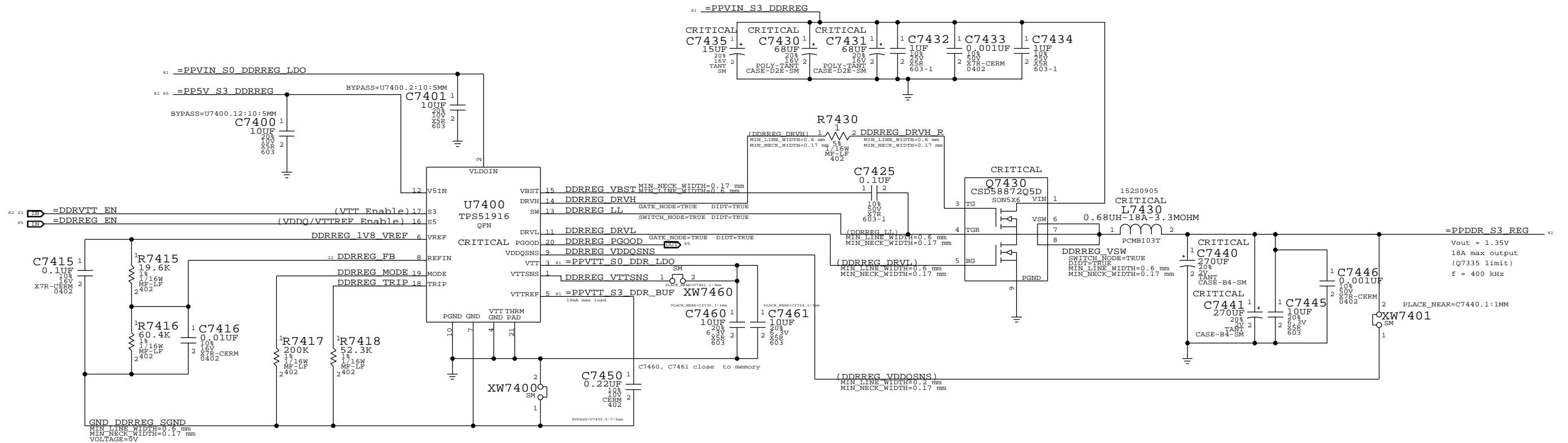


SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
CPU VR12.5 VCC Regulator IC			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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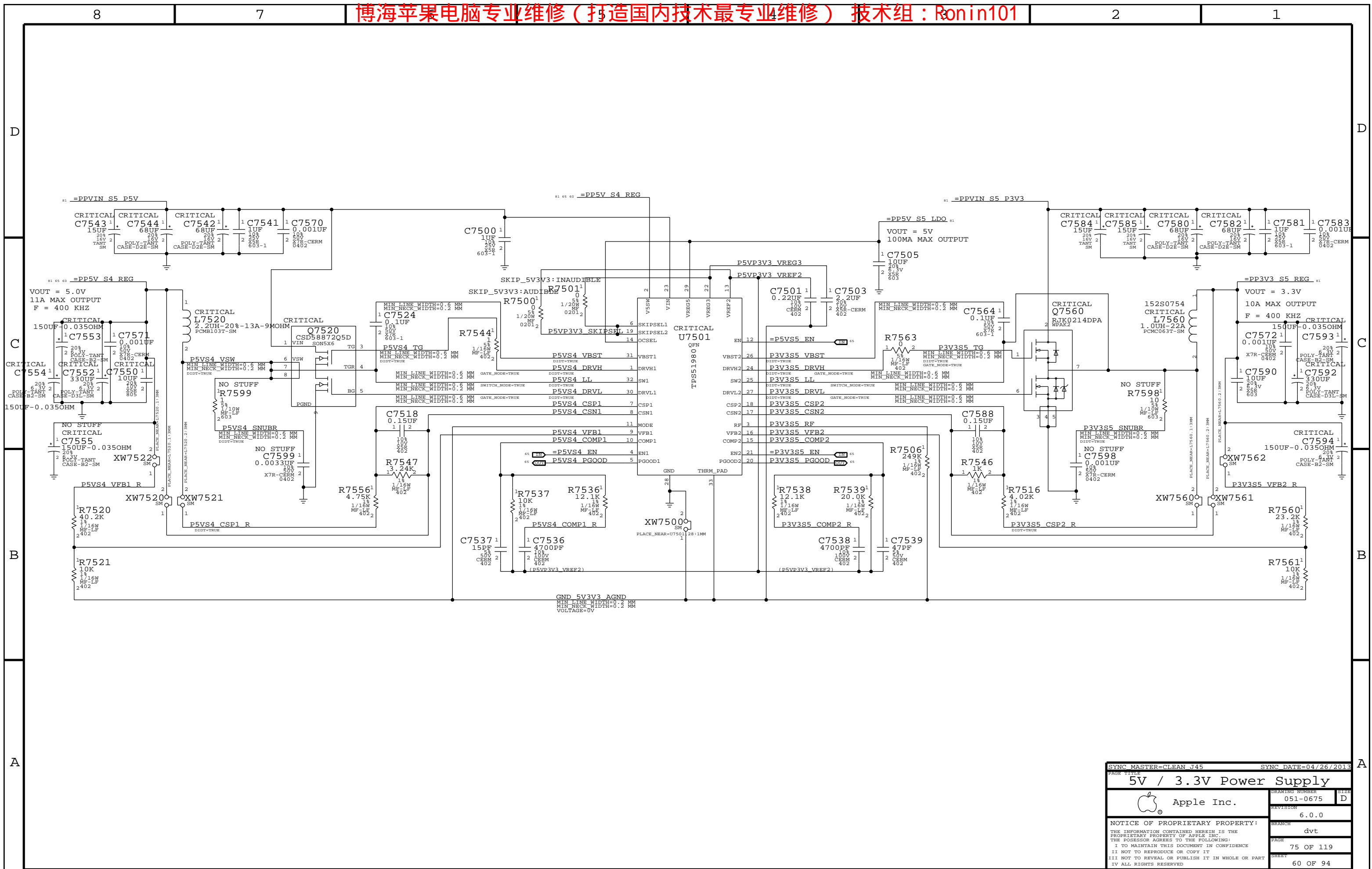


SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
CPU VR12.5 VCC Power Stage			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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DDR3L (1V35 S3) REGULATOR

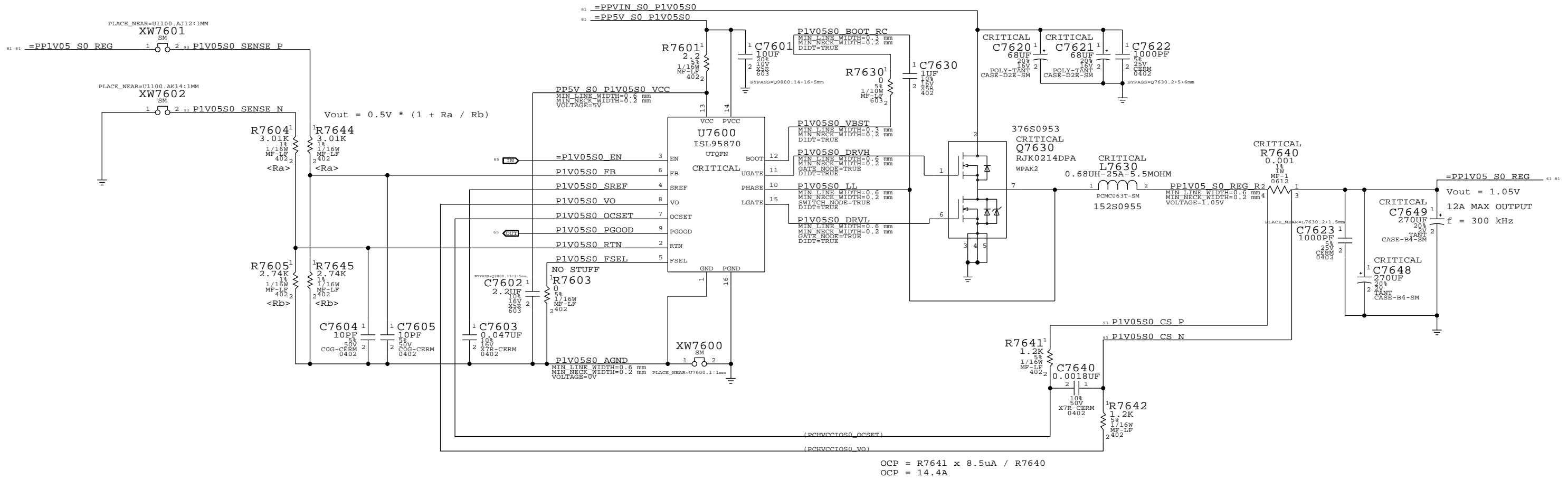


SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
1.35V DDR3L SUPPLY			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
5V / 3.3V Power Supply			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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1V05 S0 REGULATOR



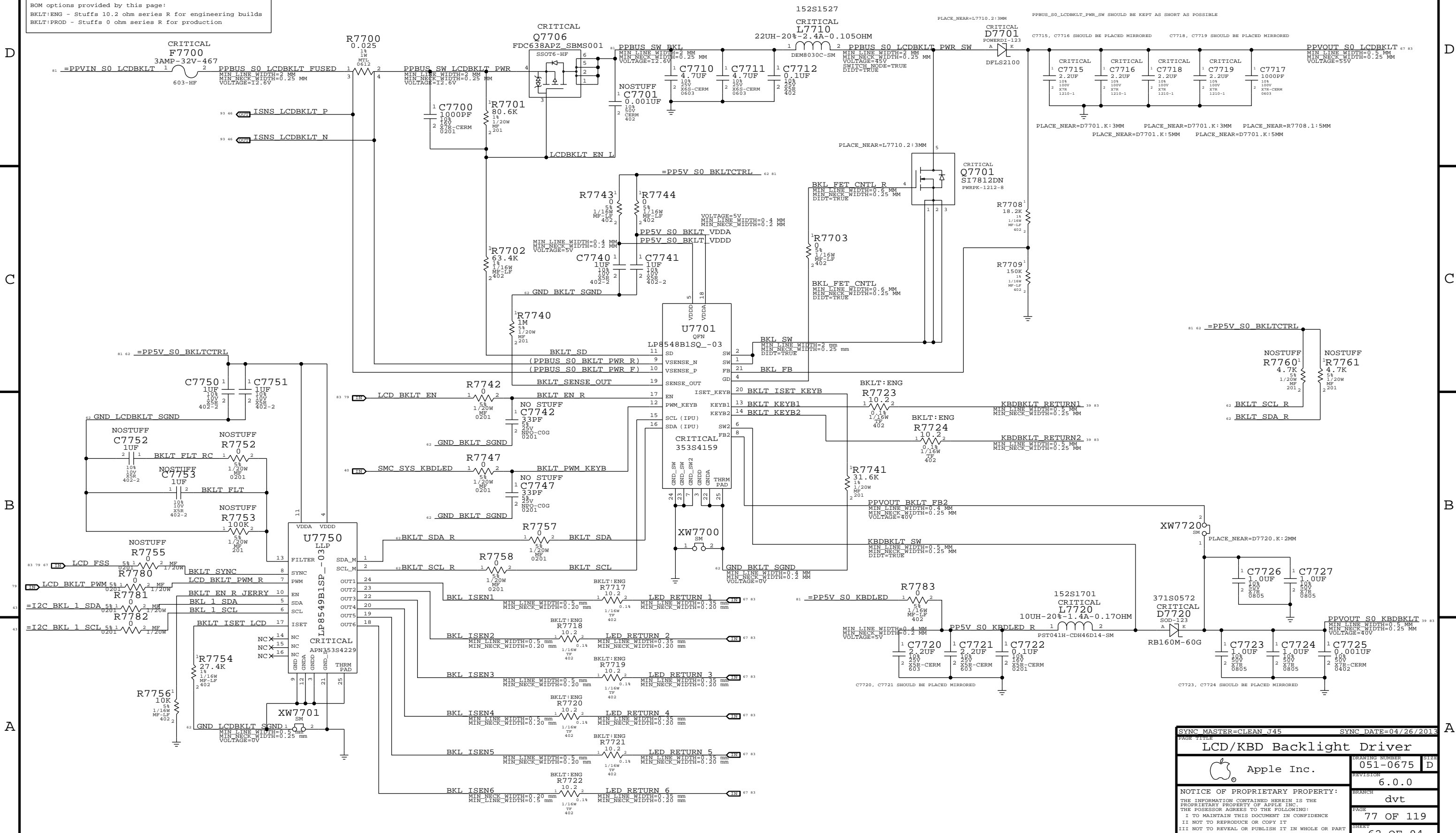
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PAGE TITLE 1V05V POWER SUPPLY			
DRAWING NUMBER 051-0675		SIZE D	
REVISION 6.0.0		BRANCH dvt	
PAGE 76 OF 119		SHEET 61 OF 94	
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Page Notes

Power aliases required by this page:
 - =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
 - =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
 - =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
 BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
 BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	PP5V_S0_BKLTCTRL		BKLT:PROD



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

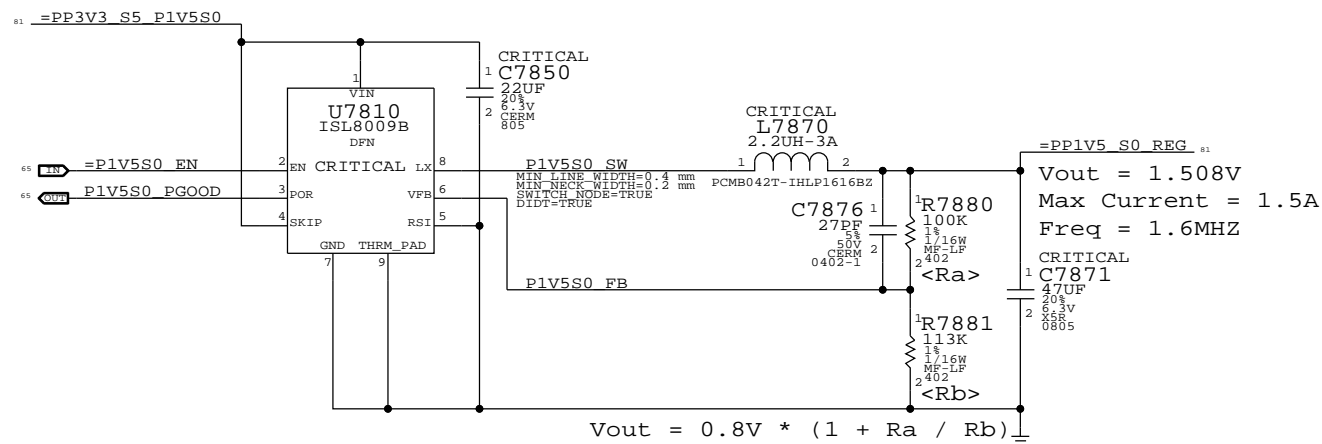
BRANCH: dvt

PAGE: 77 OF 119

SHEET: 62 OF 94

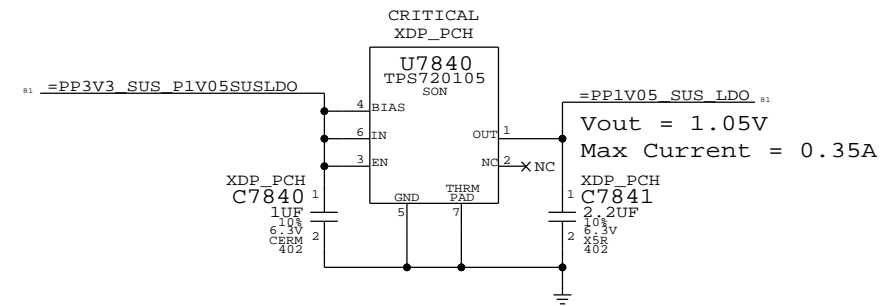
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1.5V S0 Regulator

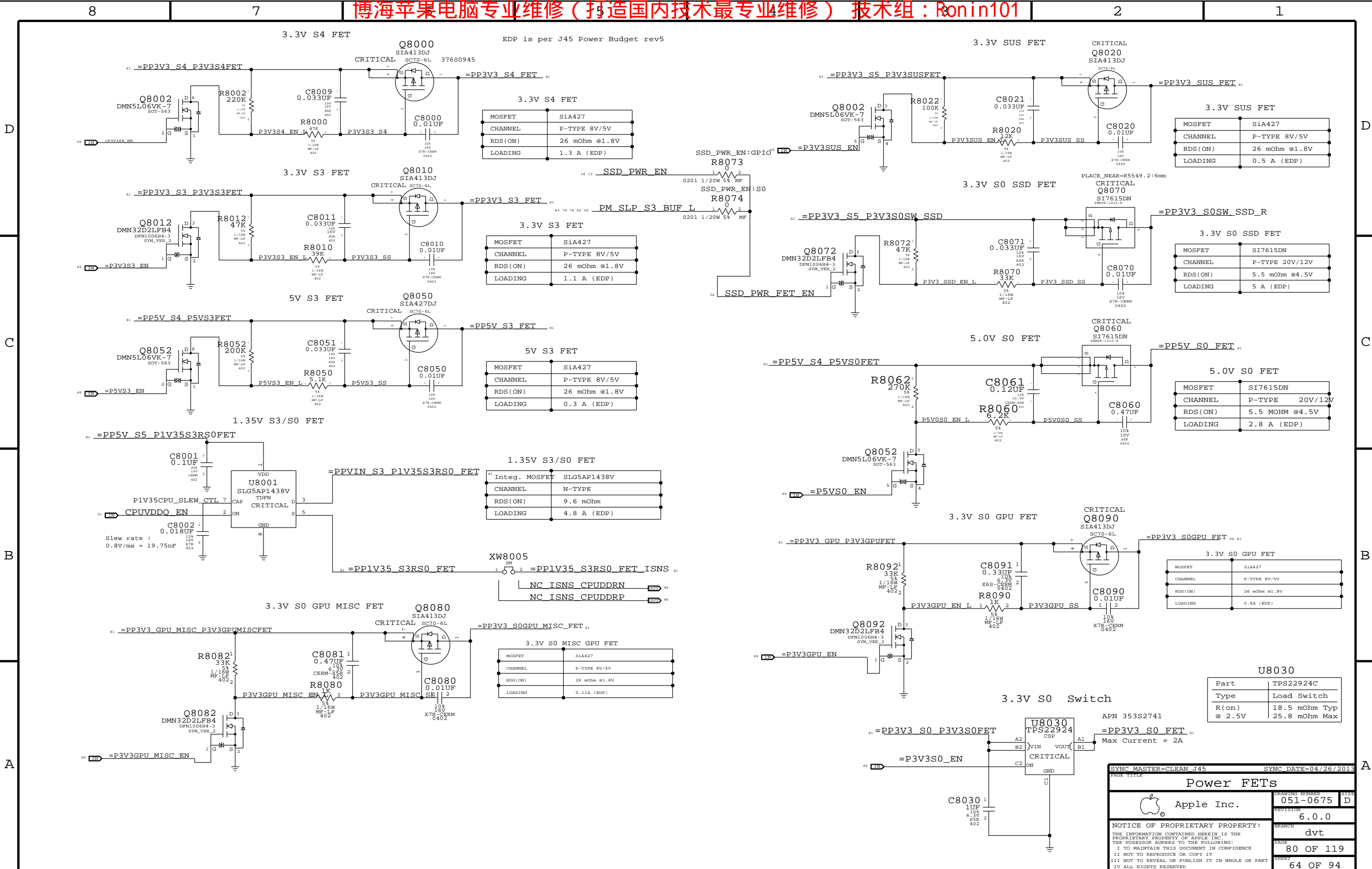


1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE Misc Power Supplies			
DRAWING NUMBER 051-0675		SIZE D	
REVISION 6.0.0		BRANCH dvt	
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3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

MOSFET	Integ. MOSFET SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

XW8005

NC ISNS CPUDDRn	ON
NC ISNS CPUDDRp	ON

3.3V S0 GPU MISC FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 GPU FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.6A (EDP)

U8030

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

Power FETs

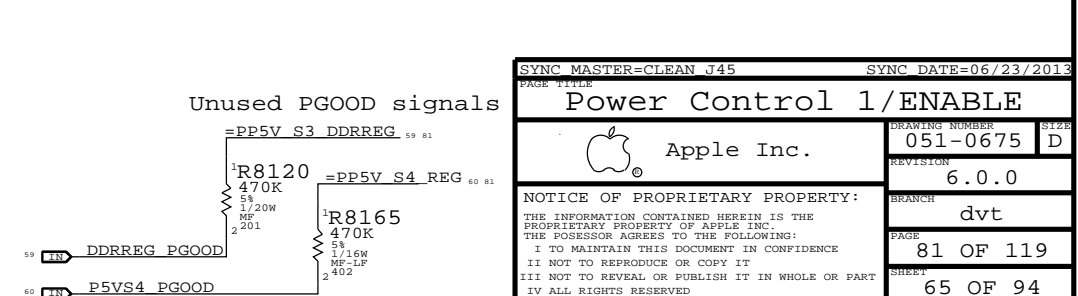
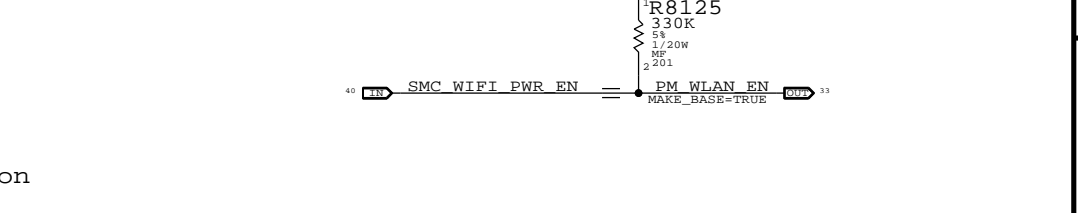
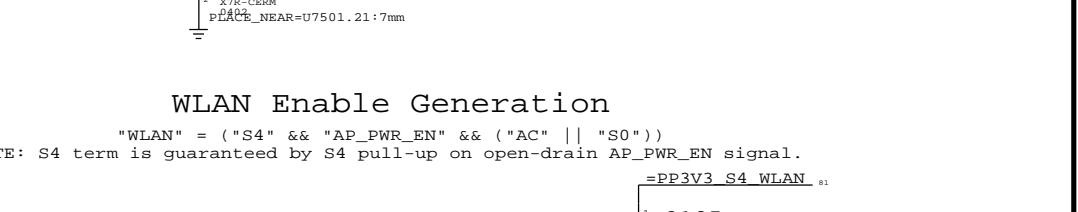
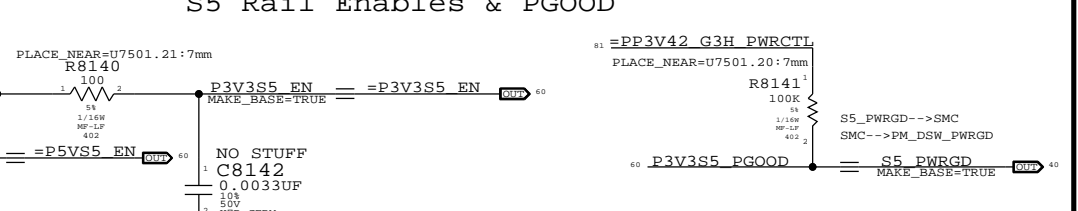
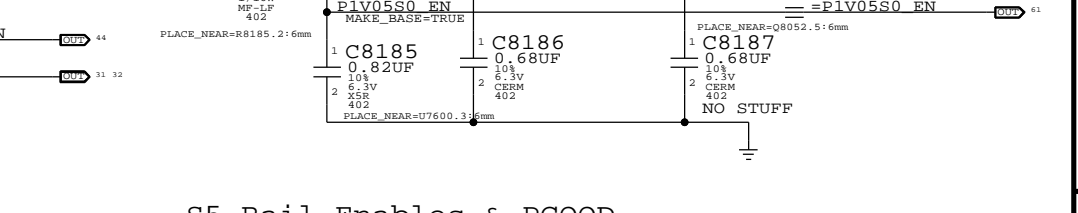
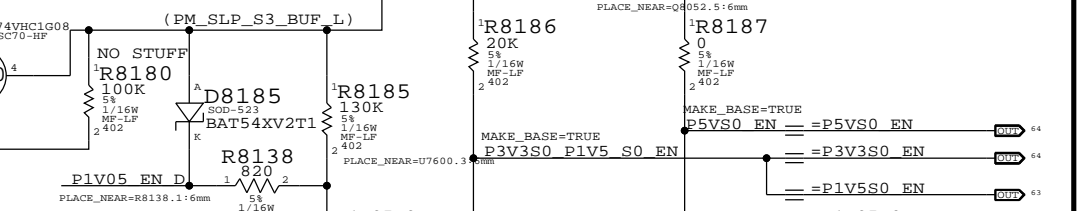
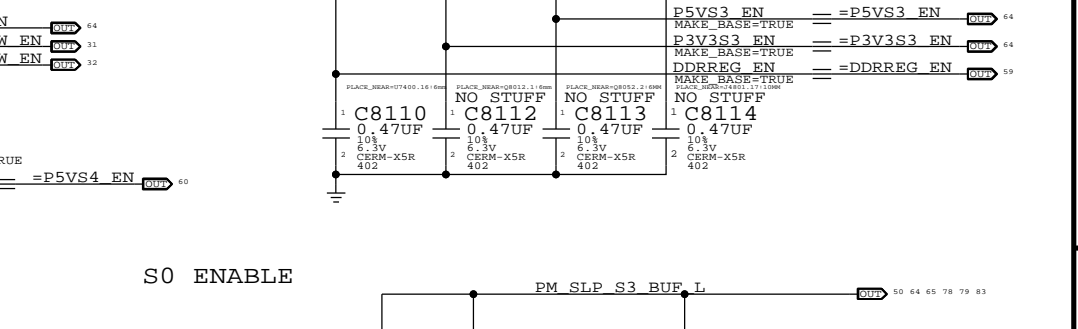
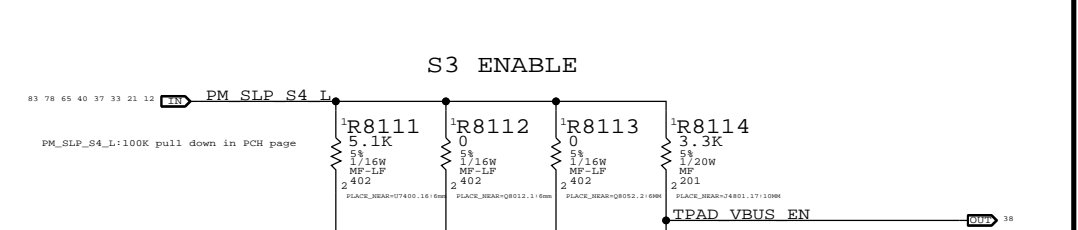
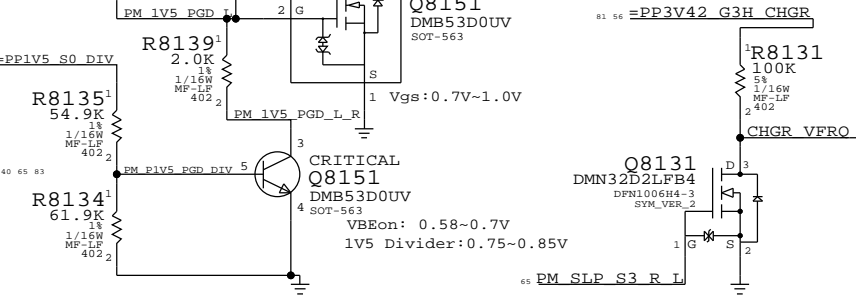
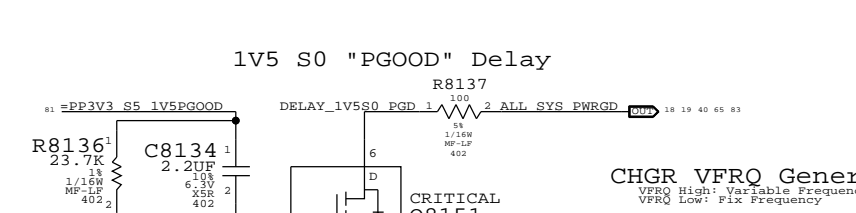
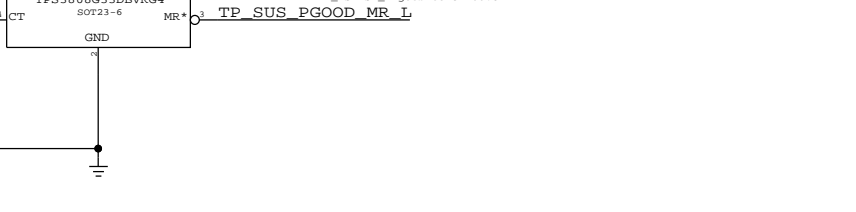
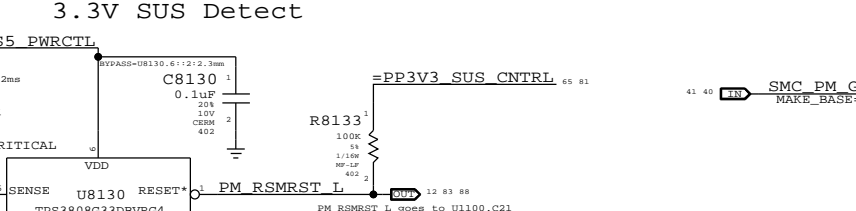
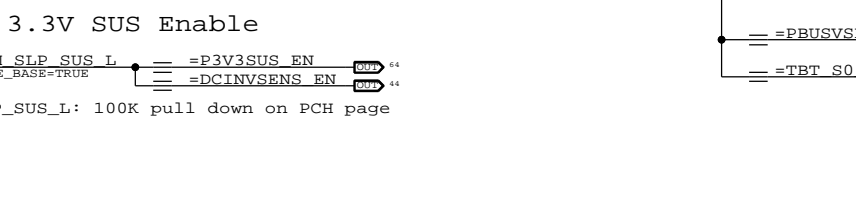
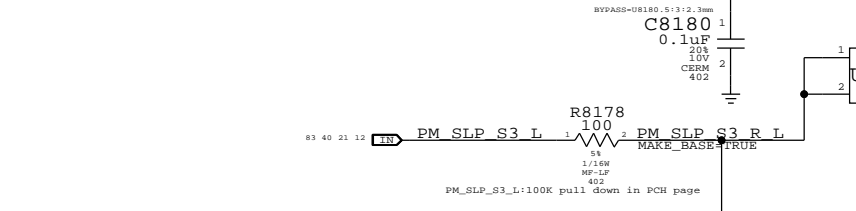
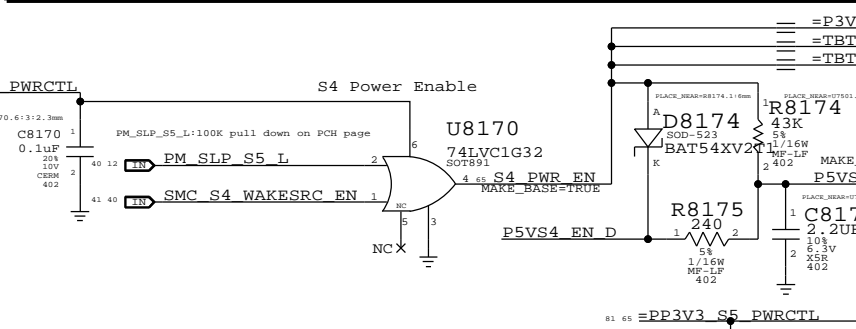
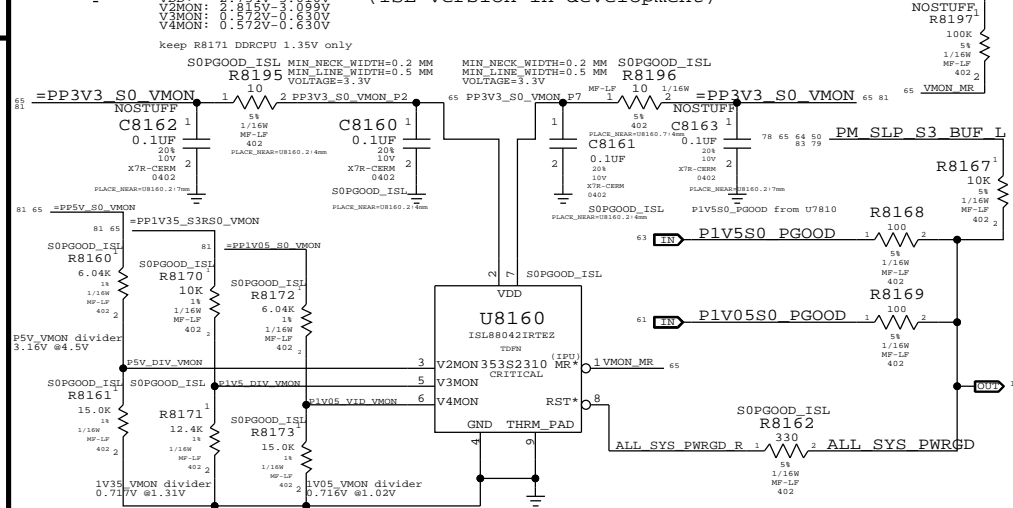
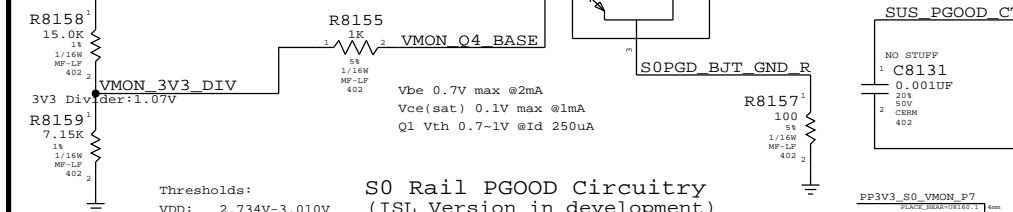
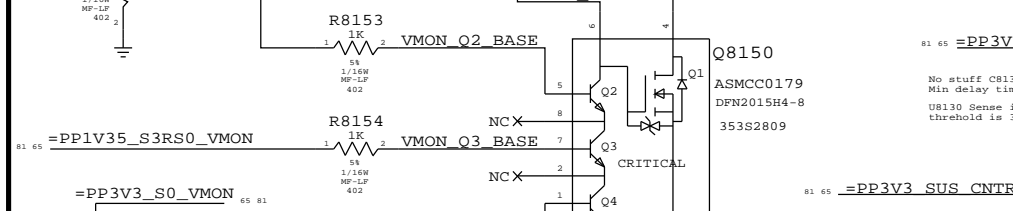
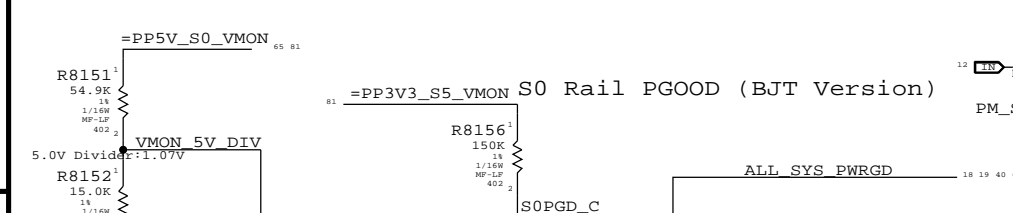
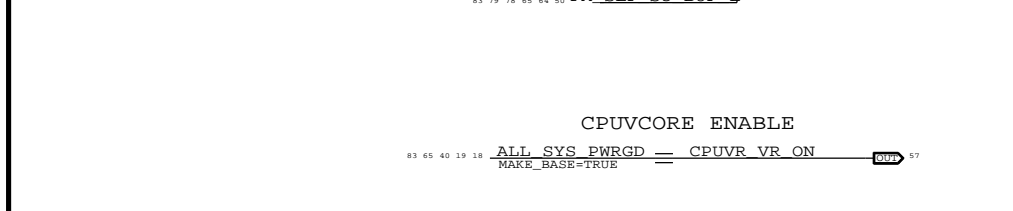
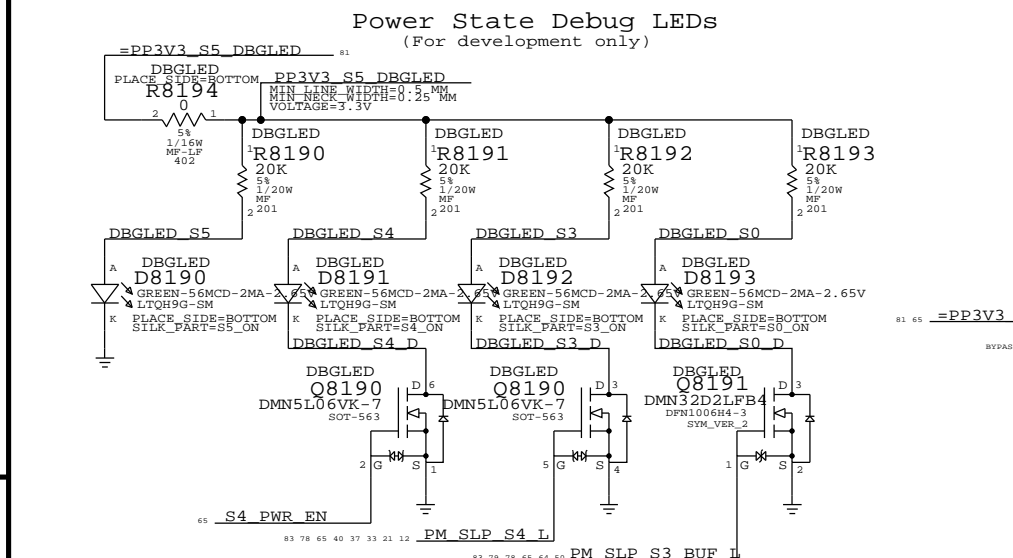
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PAGE	80 OF 119	SHEET	64 OF 94

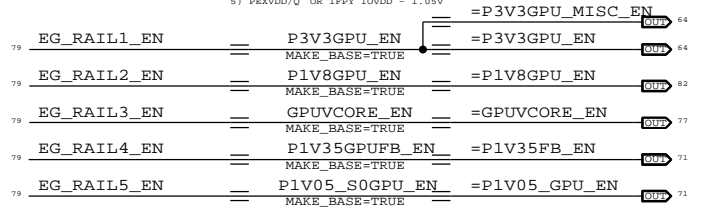
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_S5_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4C)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0



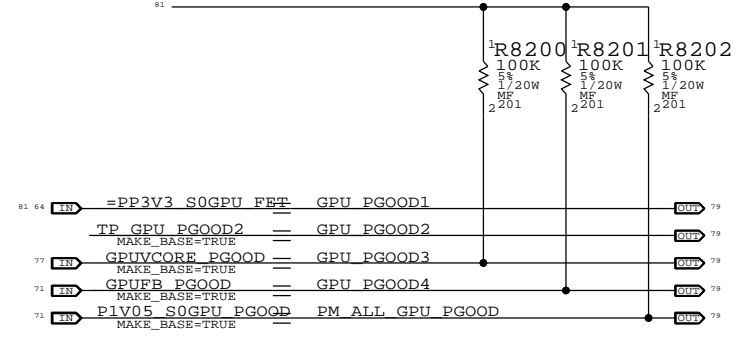
GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME UP in the following order:
 1) GPU_3.3V
 2) IFX IOVDD - 1.8V
 3) GPUVCORE
 4) FBVDDQ/GDDR5 1.35V
 5) PERVDD/Q OR IFFY IOVDD - 1.05V



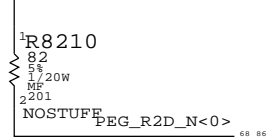
NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

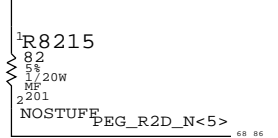


NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.
 NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

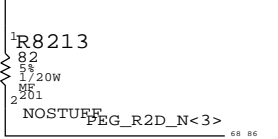
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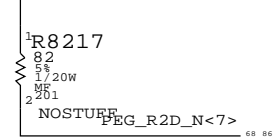
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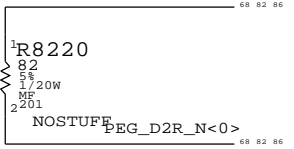
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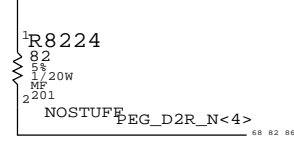
PLACE R8210 - R8217 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

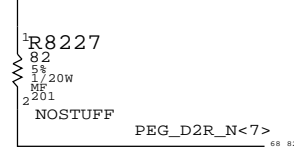
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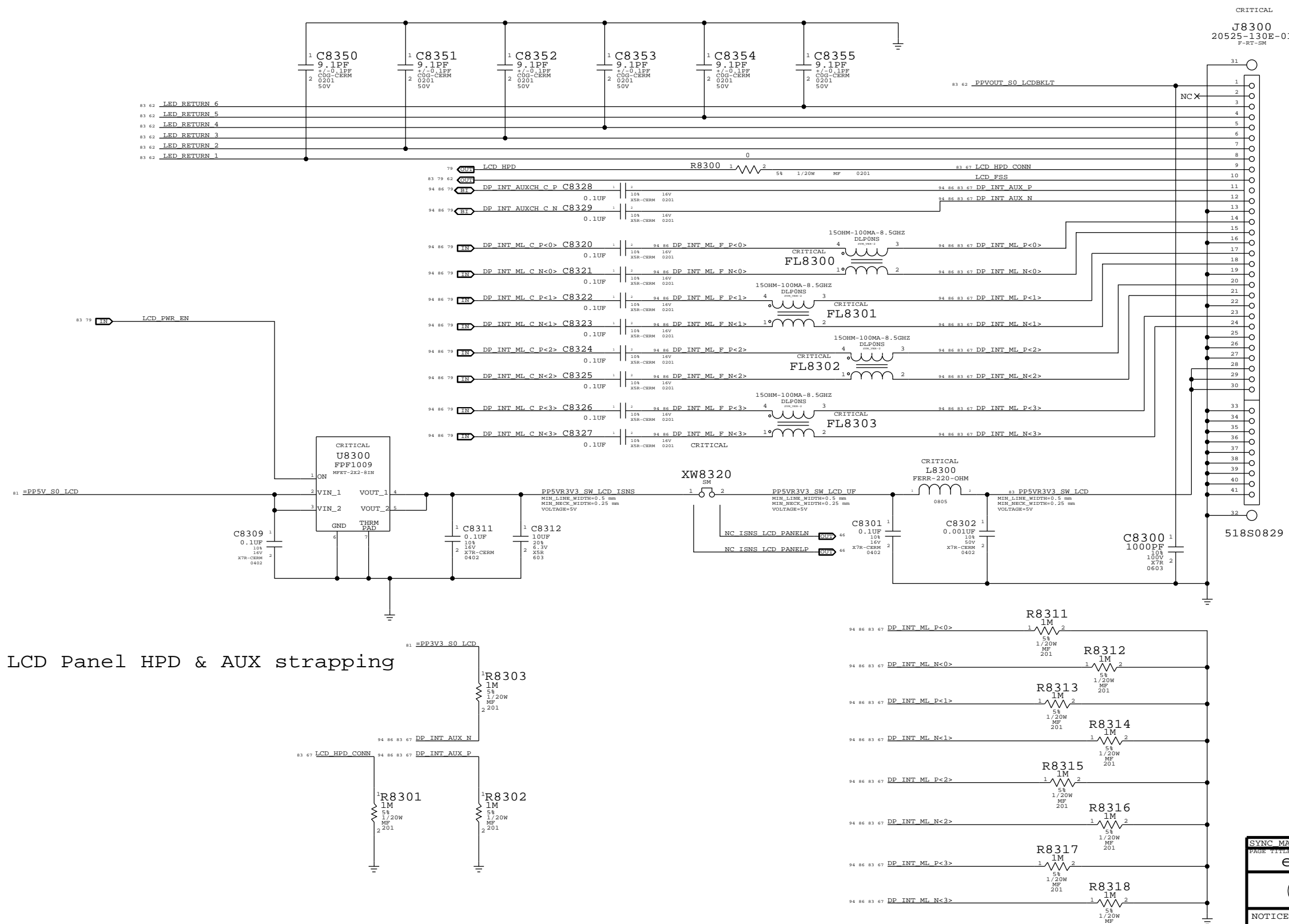
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PLACE R8220 - R8227 CLOSE TO U1000

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Power Sequencing EG/PCH S0			
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LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping

CRITICAL
J8300
20525-130E-01
F-RT-SM

SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
PAGE TITLE eDP Display Connector			
Apple Inc.		DRAWING NUMBER 051-0675	SIZE D
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Page Notes

Power aliases required by this page:
 --PP3V3_GPU_VDD33

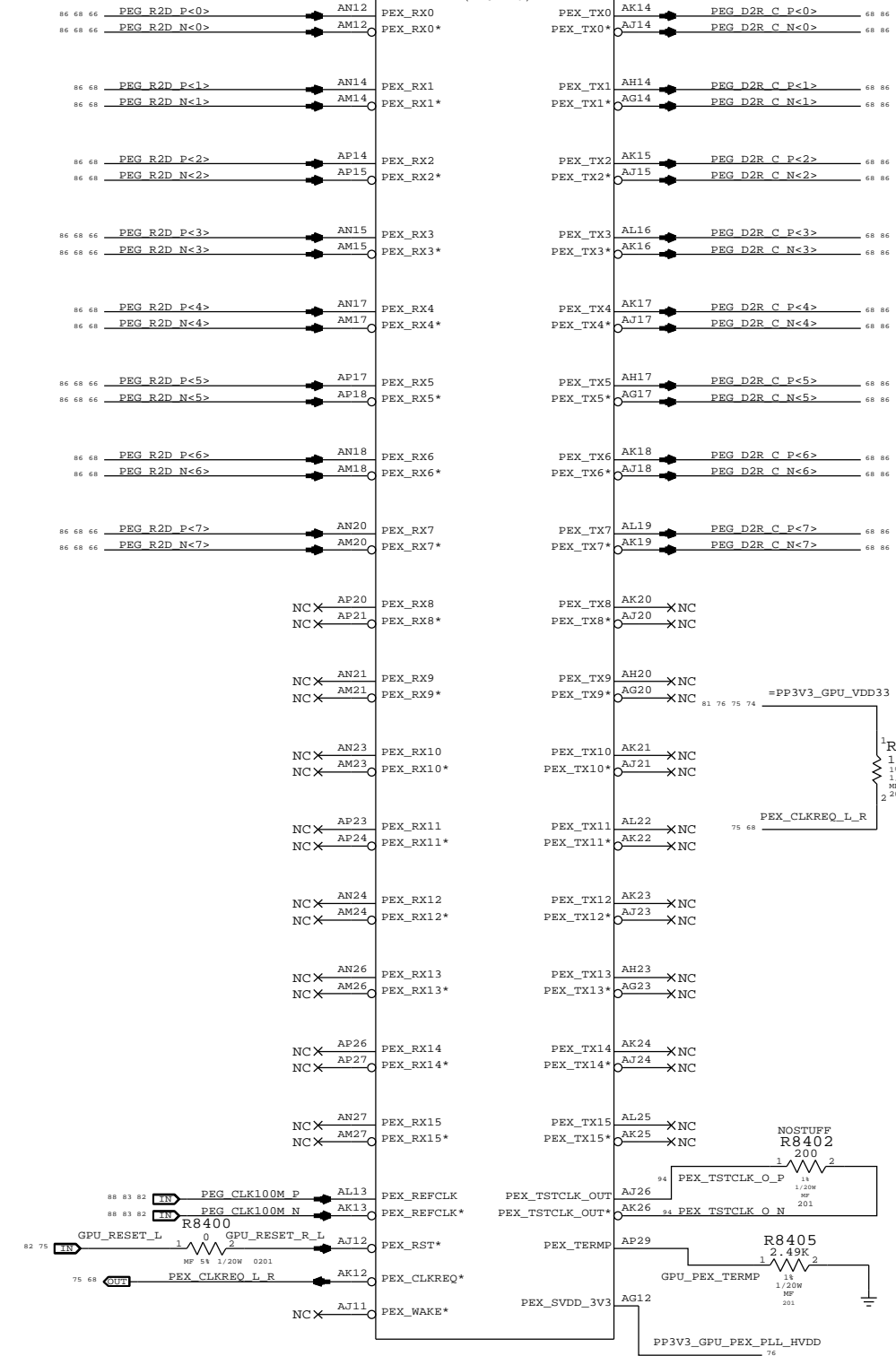
Signal aliases required by this page:
 (NONE)

ROM options provided by this page:
 (NONE)

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86 68		PEG D2R C N<3>	C8462	0.22UF	1	2	PEG D2R N<3>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C P<4>	C8463	0.22UF	1	2	PEG D2R P<4>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C N<4>	C8464	0.22UF	1	2	PEG D2R N<4>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C P<5>	C8465	0.22UF	1	2	PEG D2R P<5>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C N<5>	C8466	0.22UF	1	2	PEG D2R N<5>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C P<6>	C8467	0.22UF	1	2	PEG D2R P<6>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C N<6>	C8468	0.22UF	1	2	PEG D2R N<6>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C P<7>	C8469	0.22UF	1	2	PEG D2R P<7>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								
86 68		PEG D2R C N<7>	C8470	0.22UF	1	2	PEG D2R N<7>	66 82 86
GND_VOID=TRUE 204 6.3V X6S-CERR 0201								

OMIT_TABLE

U8400 NV-GK107 BGA (1 OF 10)



SYNC MASTER=D2_MLR SYNC DATE=07/31/2012

KEPLER PCI-E

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

PAGE: 84 OF 119

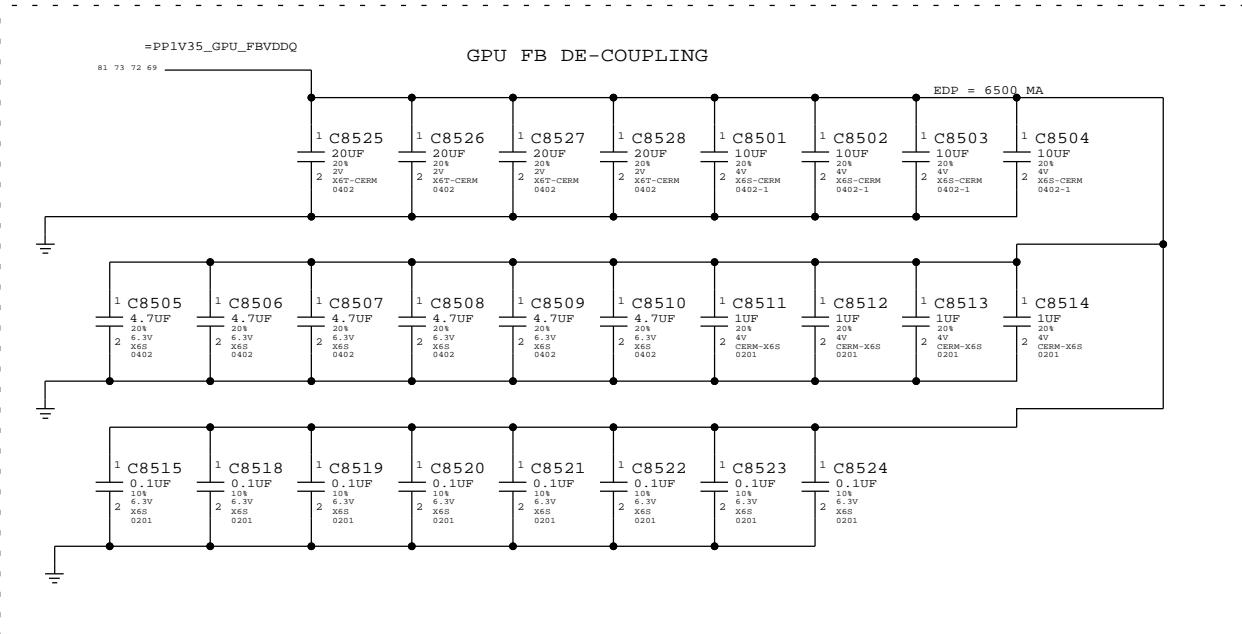
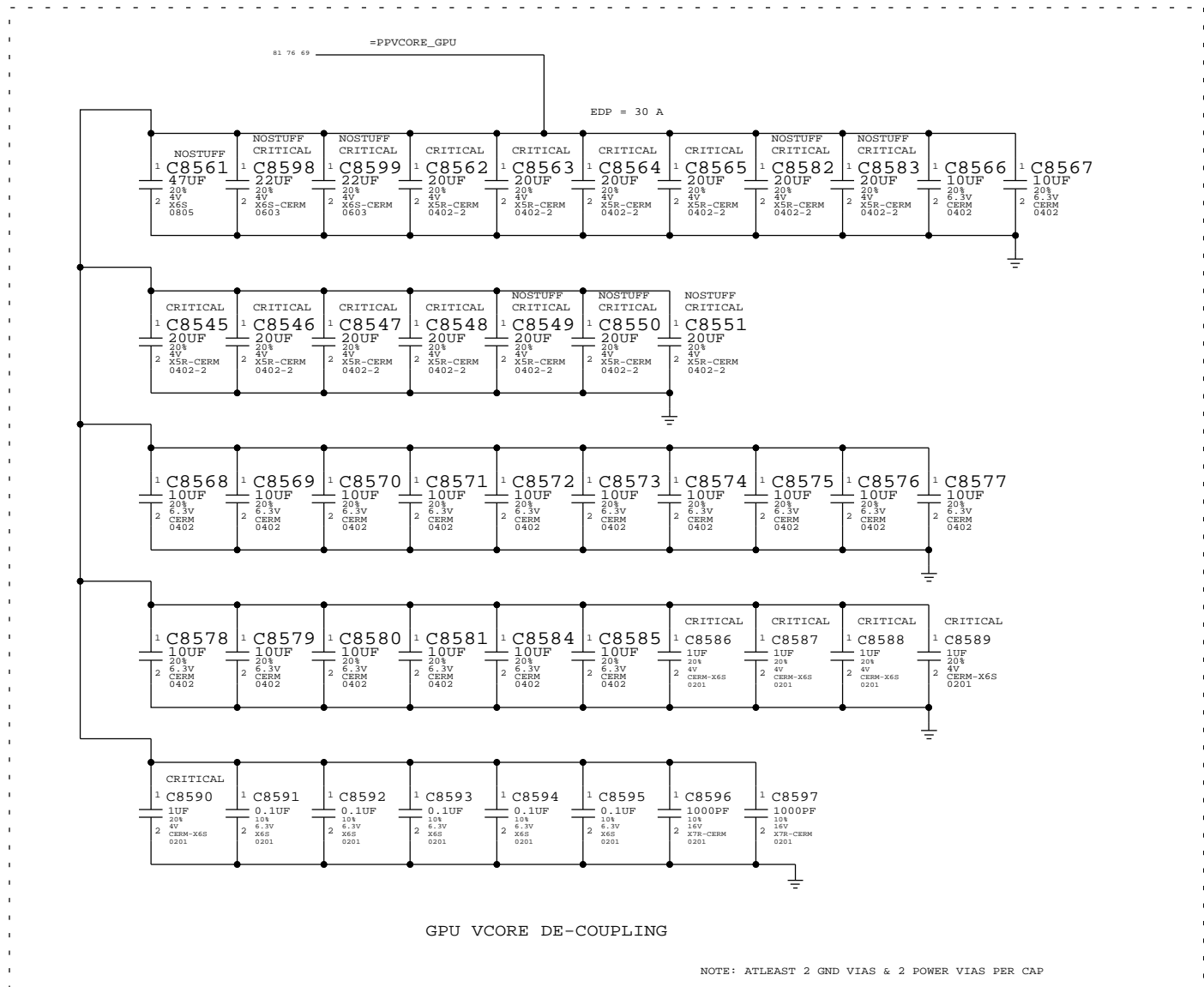
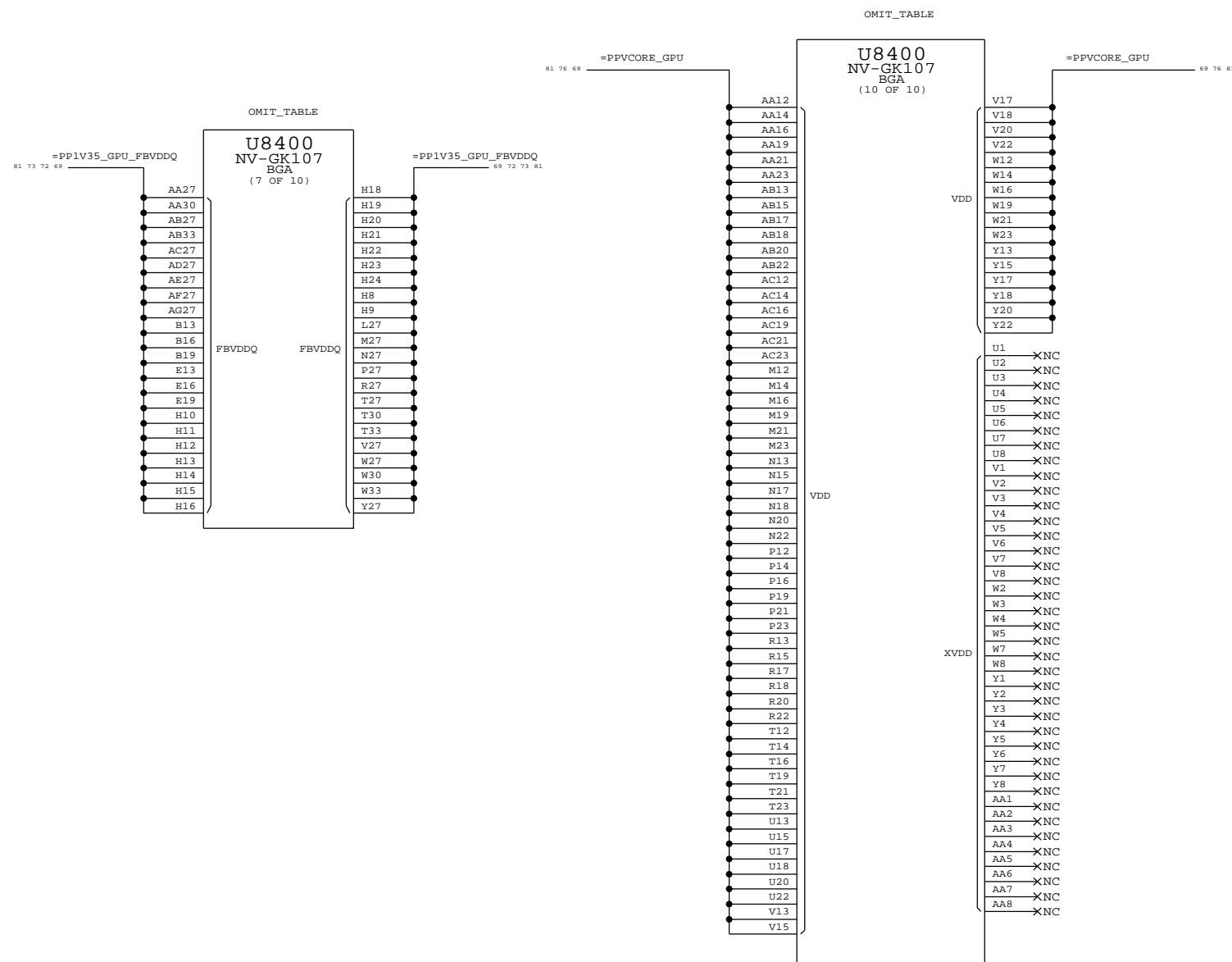
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SHEET: 68 OF 94

Power aliases required by this page:
 - =PPVCORE_GPU
 - =PPV35_GPU_FBDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



SYNC MASTER=D2 MLR		SYNC DATE=07/31/2012	
KEPLER CORE/FB POWER			
Apple Inc.		DRAWING NUMBER	SIZE
		051-0675	D
		REVISION	
		6.0.0	
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		dvt	
		PAGE	85 OF 119
		SHEET	69 OF 94

Power aliases required by this page:
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- PPIV05_GPU_FB_AVDD

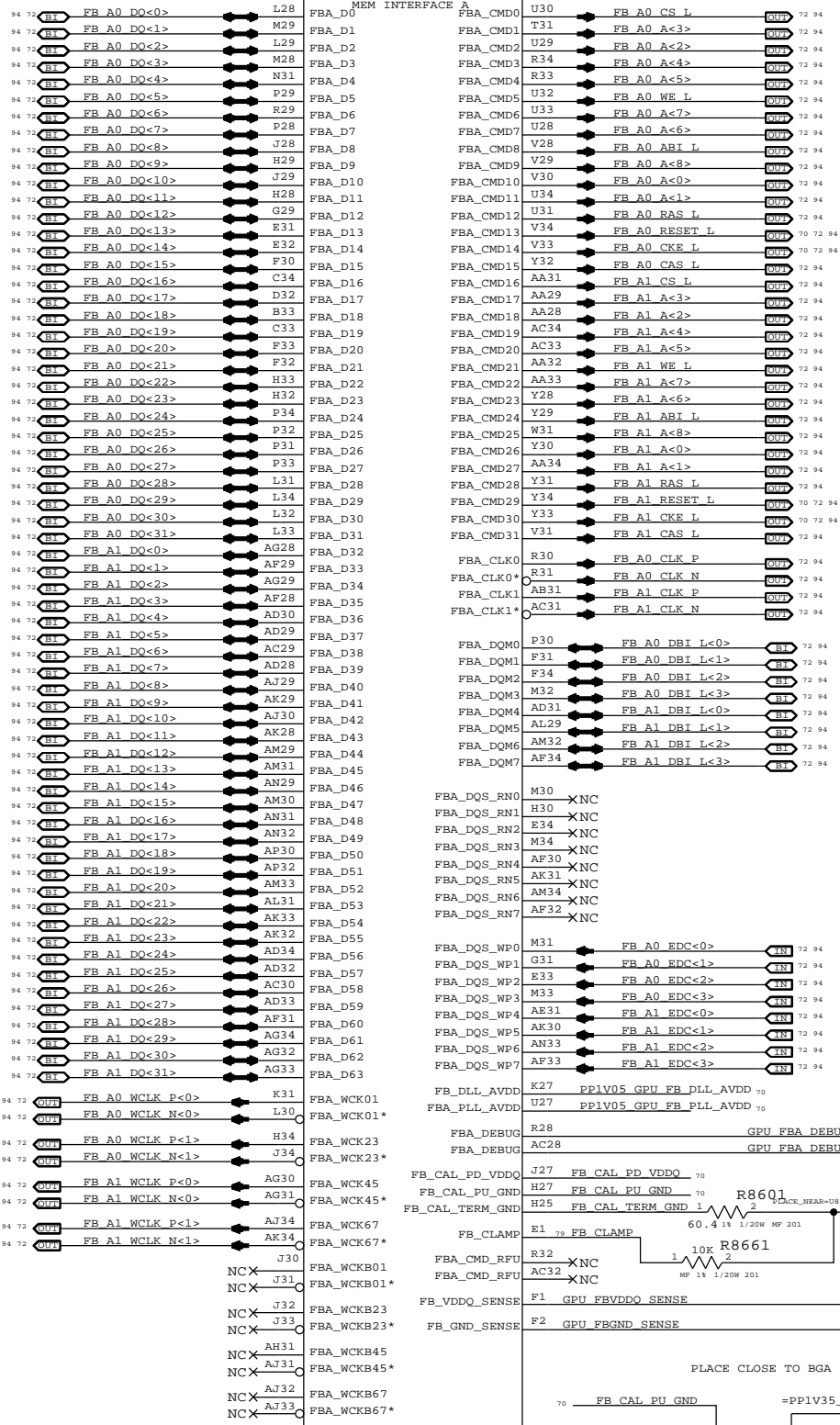
Signal aliases required by this page:
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BOM options provided by this page:
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NOTE:GDDR5 MODE H MAPPING

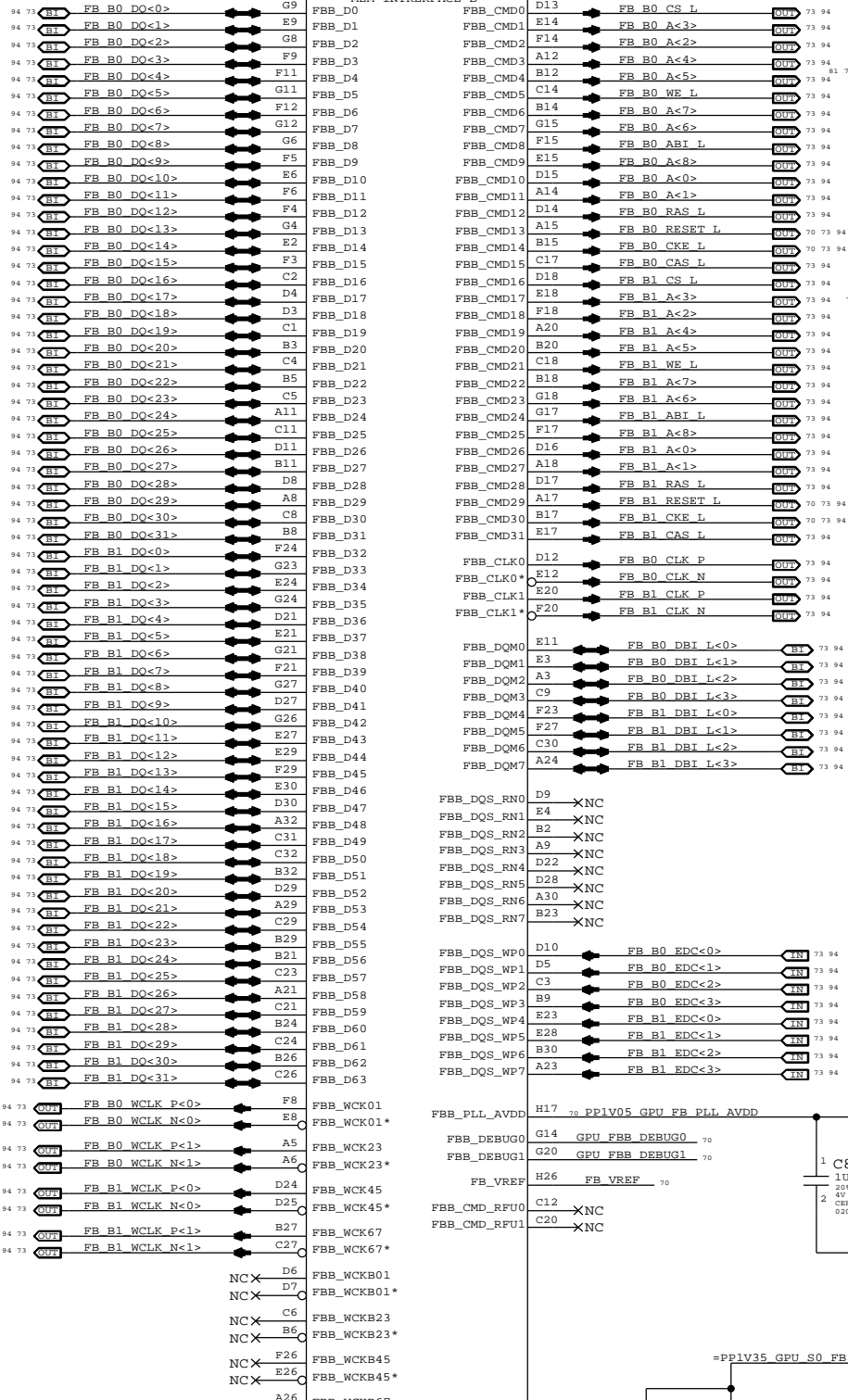
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U8400 NV-GK107 BGA (3 OF 10)



OMIT_TABLE

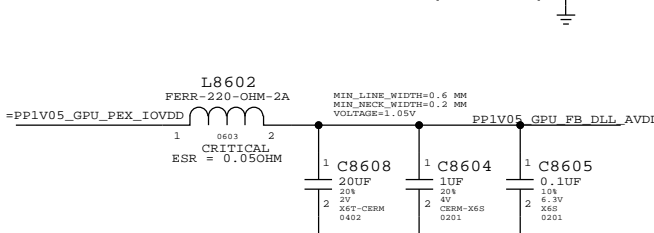
U8400 NV-GK107 BGA (4 OF 10)



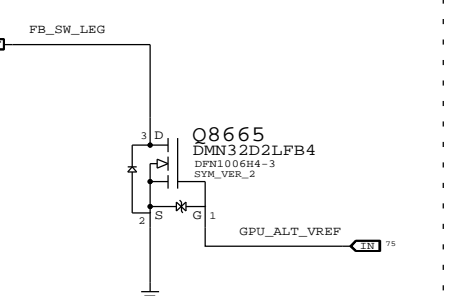
FB VREF GEN (TEST ONLY)



FB PLL & DLL VDD



MEM VREFC & VREFD SWITCH



KEPLER FRAME BUFFER I/F Apple Inc. 051-0675 D 6.0.0 dvt 86 OF 119 70 OF 94

D

D

C

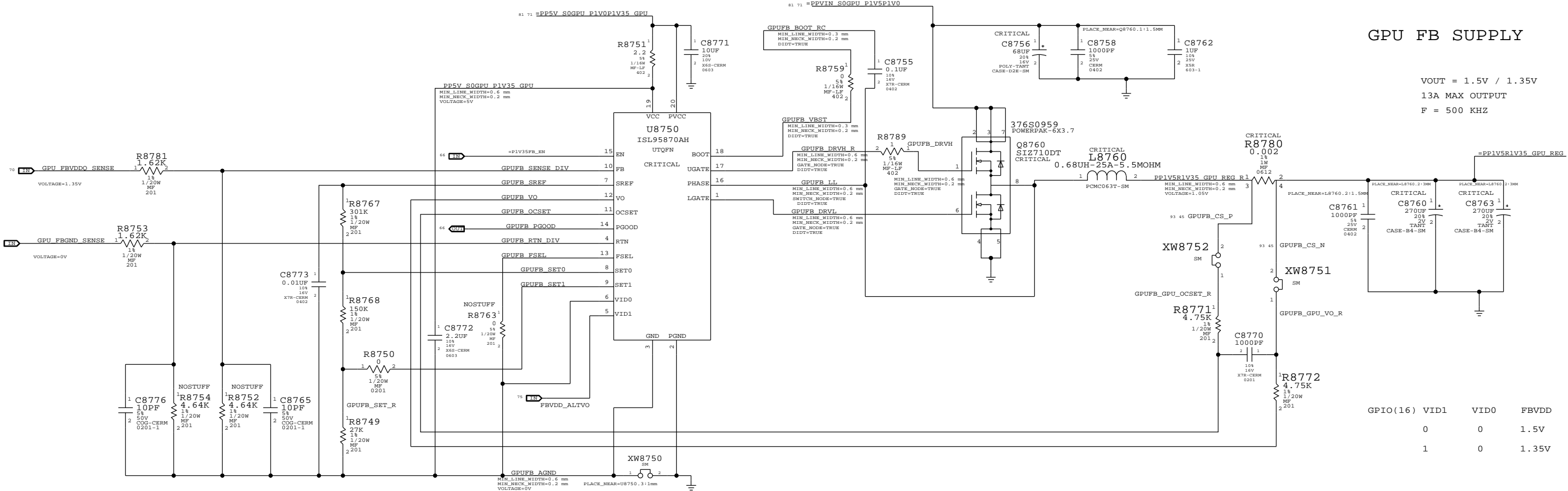
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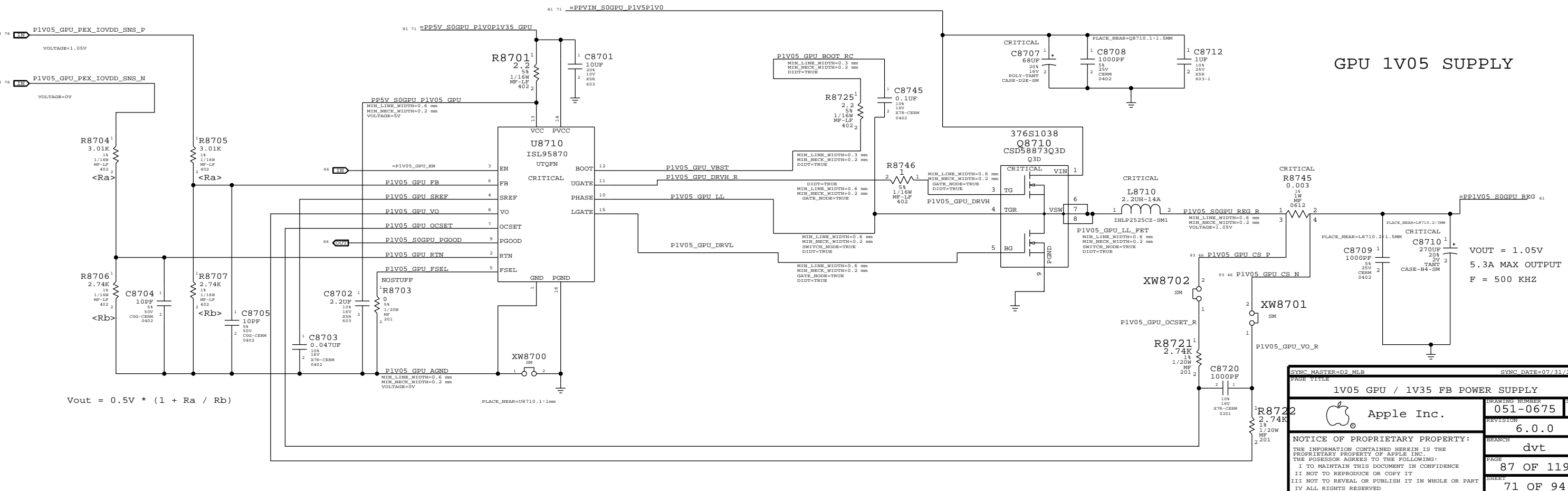
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GPU FB SUPPLY

VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ

GPIO(16)	VID1	VID0	FBVDD
0	0	0	1.5V
1	0	0	1.35V



GPU 1V05 SUPPLY

VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ

SYNC MASTER=D2 MLR SYNC DATE=07/31/2012

1V05 GPU / 1V35 FB POWER SUPPLY

Apple Inc.

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REVISION: 6.0.0

BRANCH: dvt

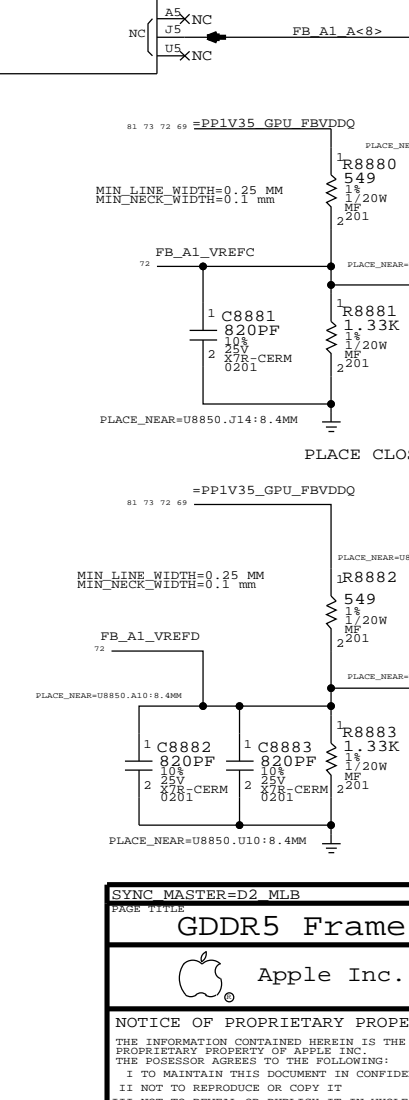
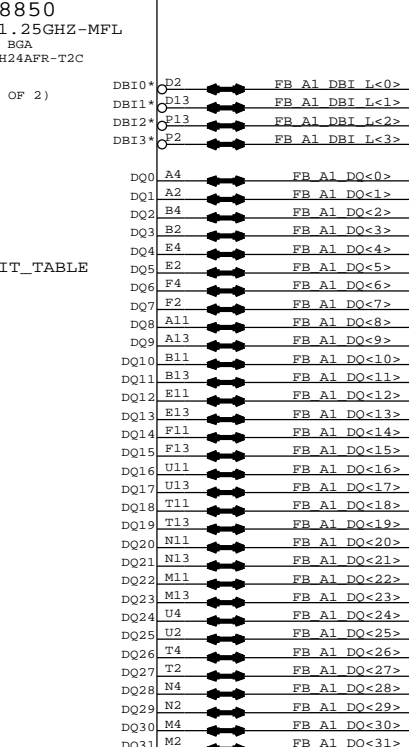
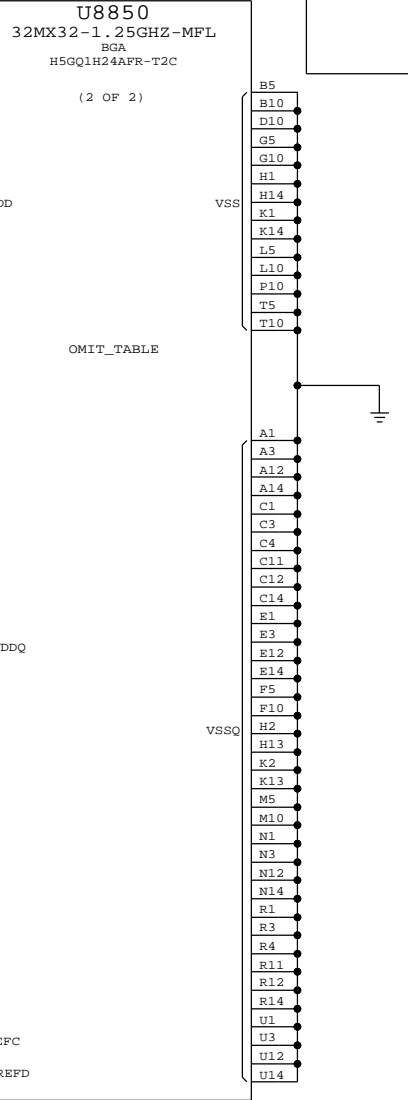
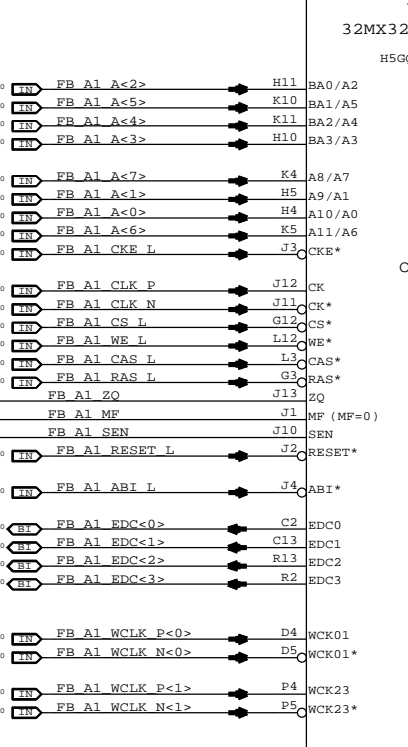
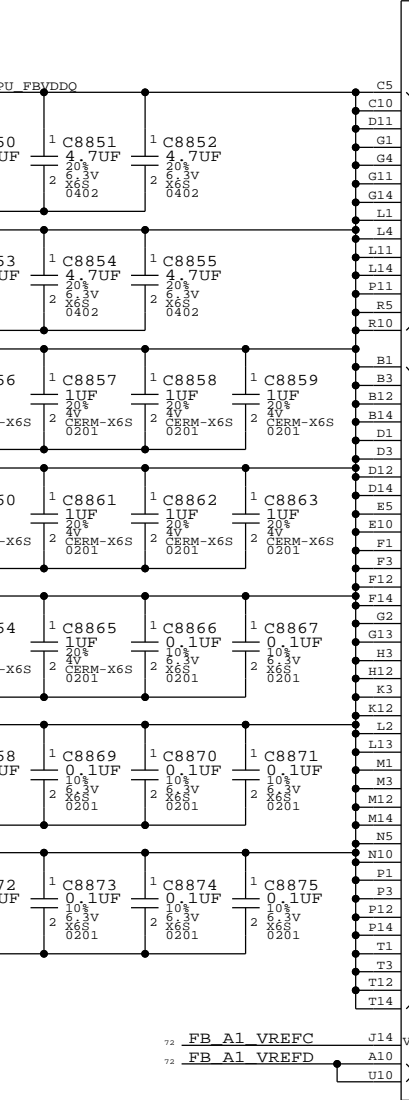
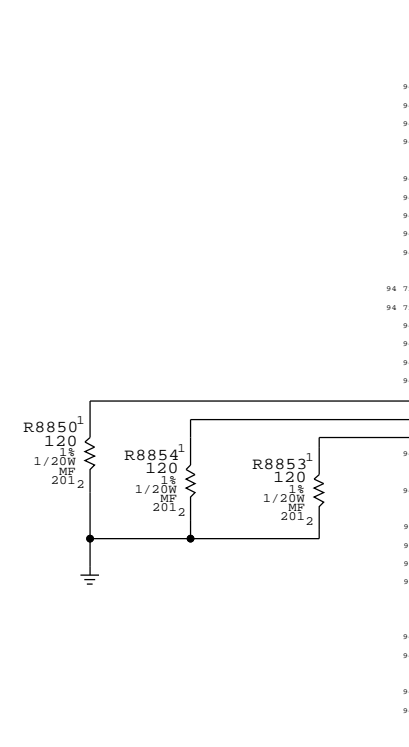
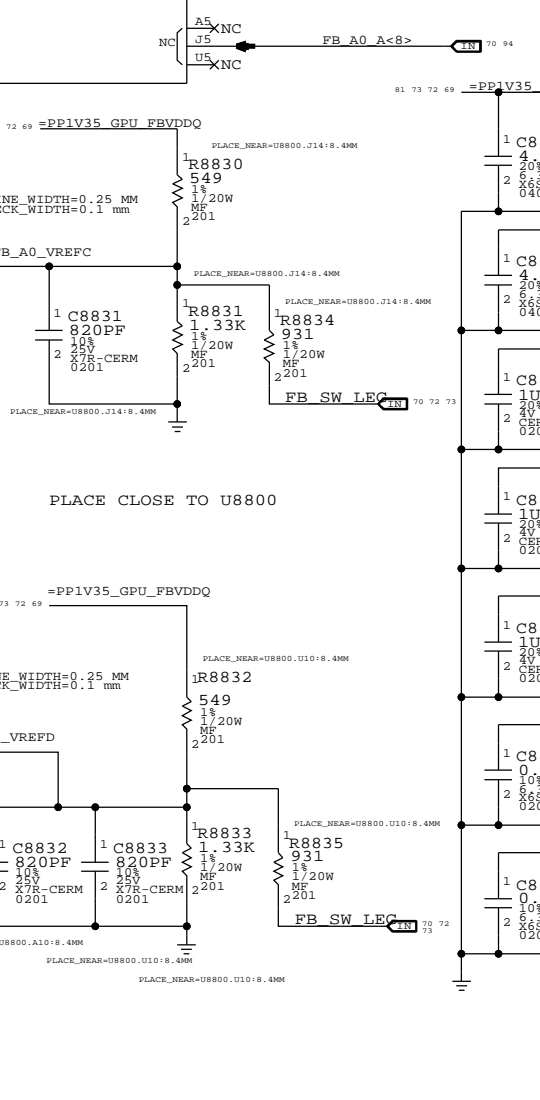
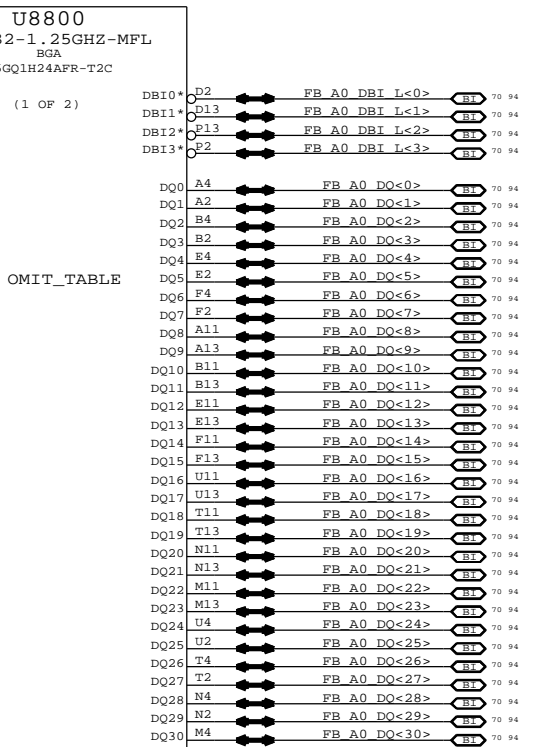
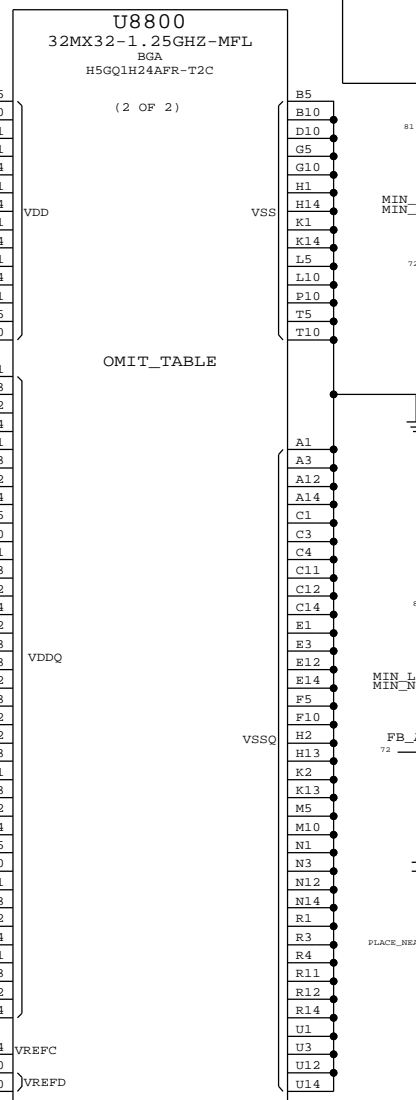
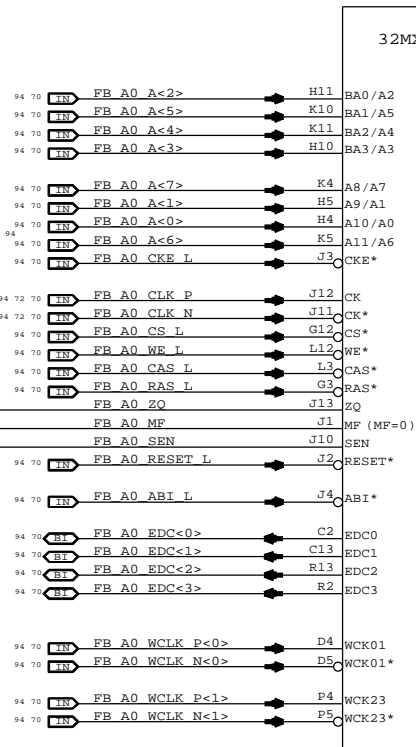
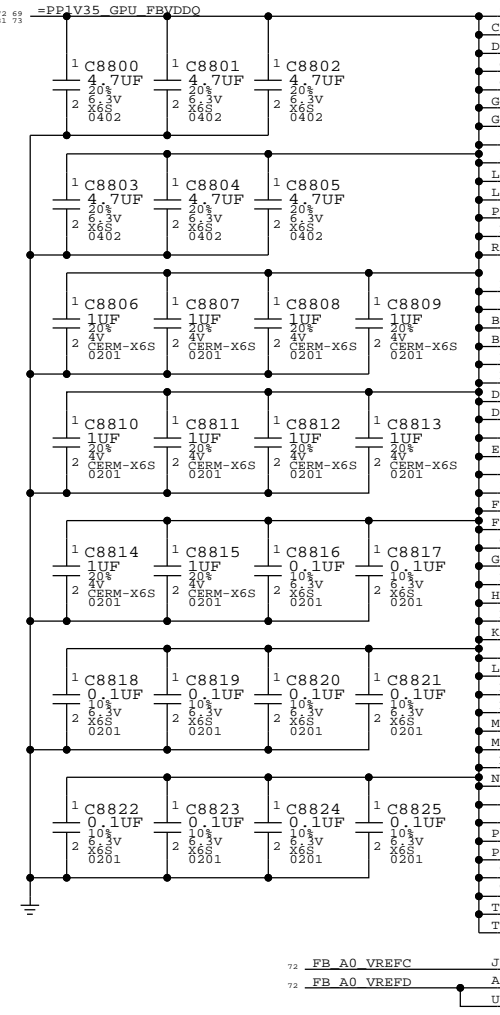
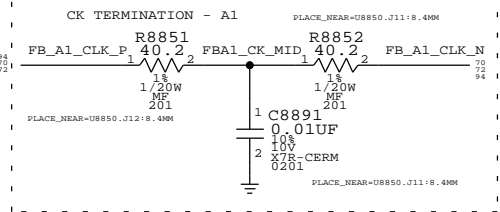
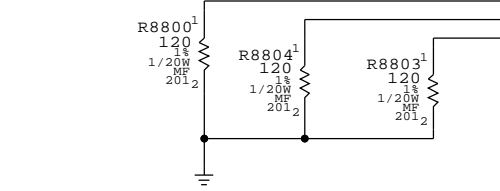
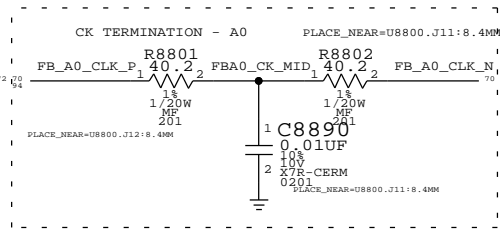
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SHEET: 71 OF 94

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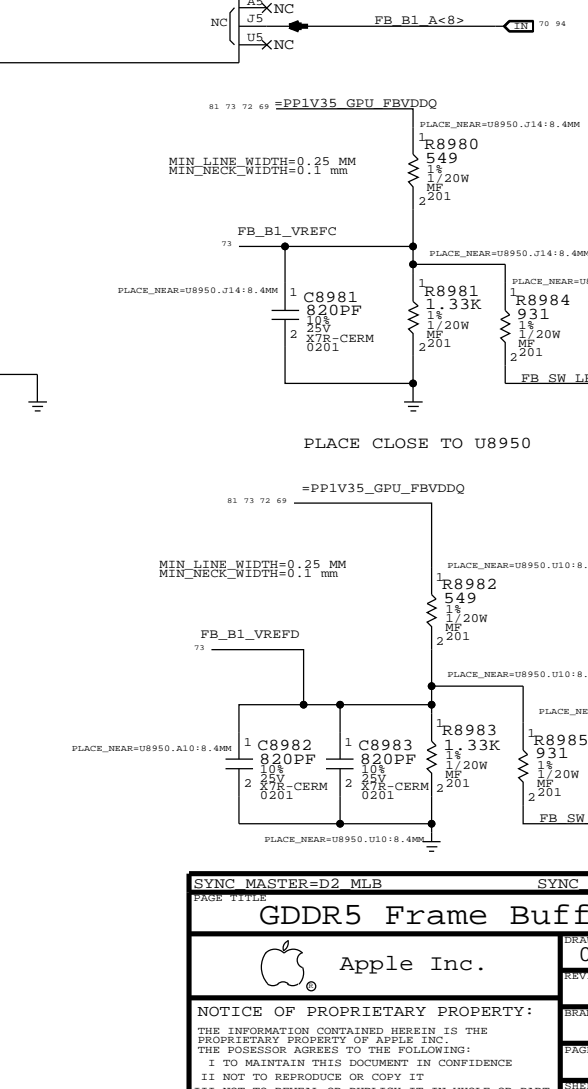
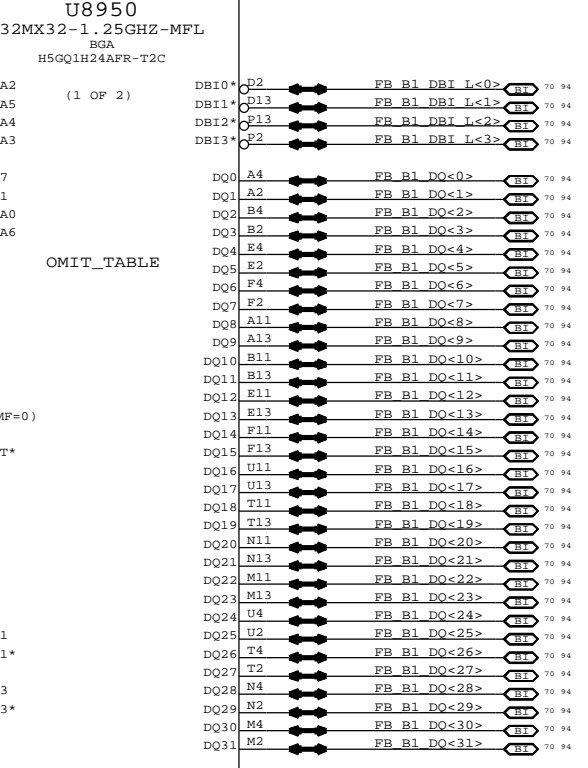
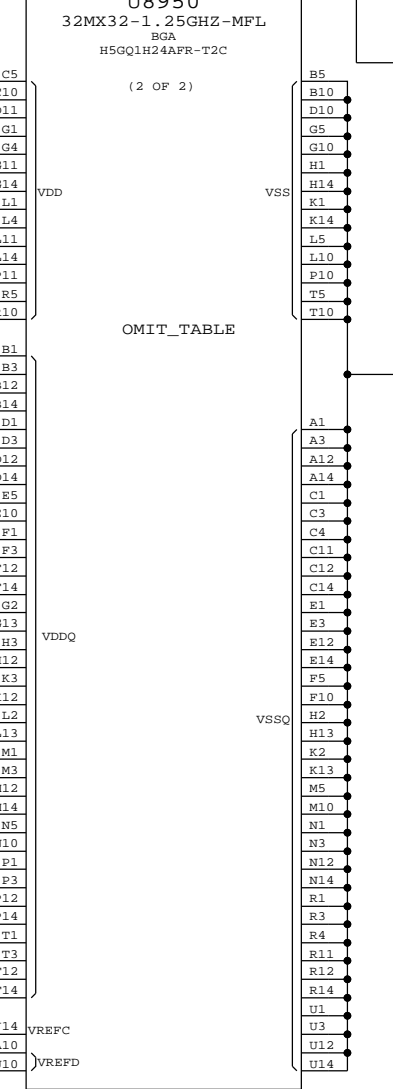
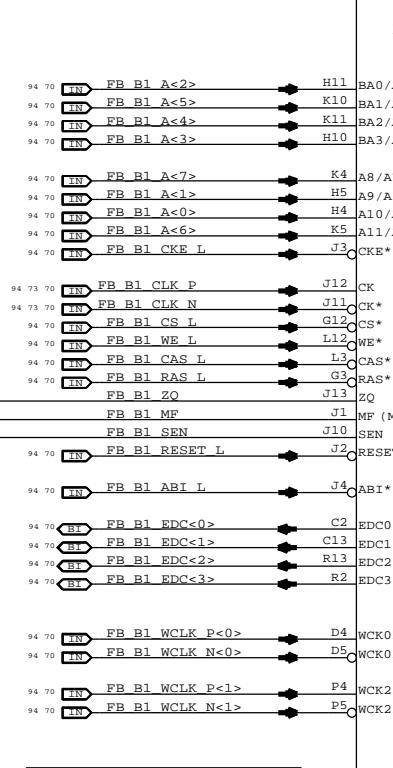
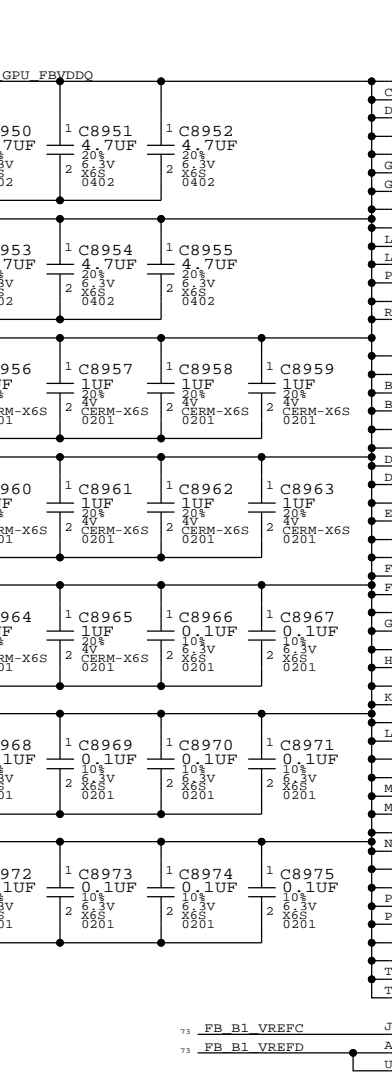
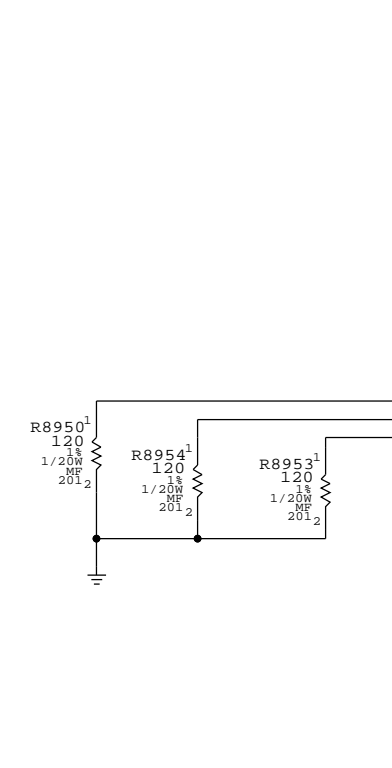
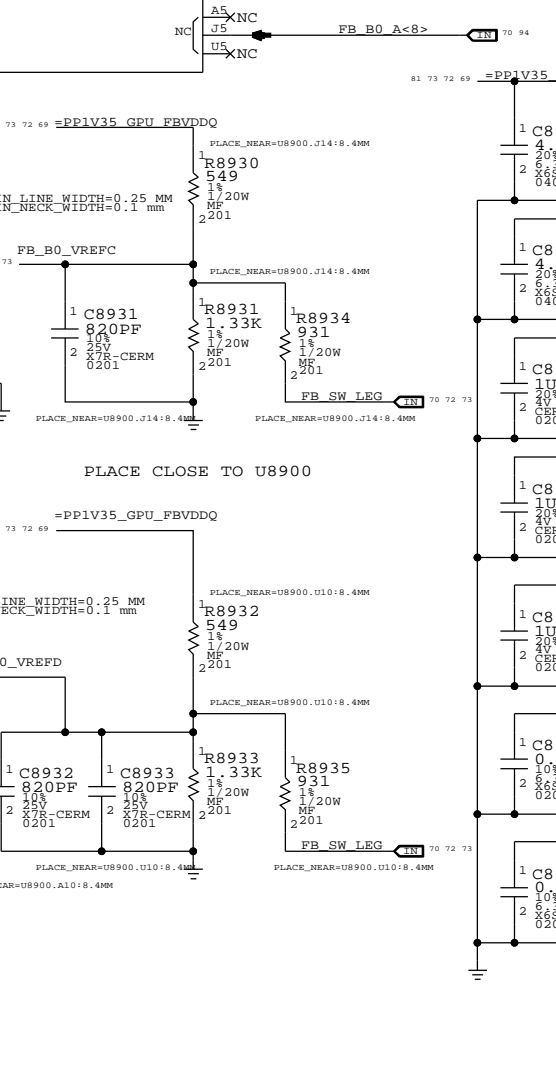
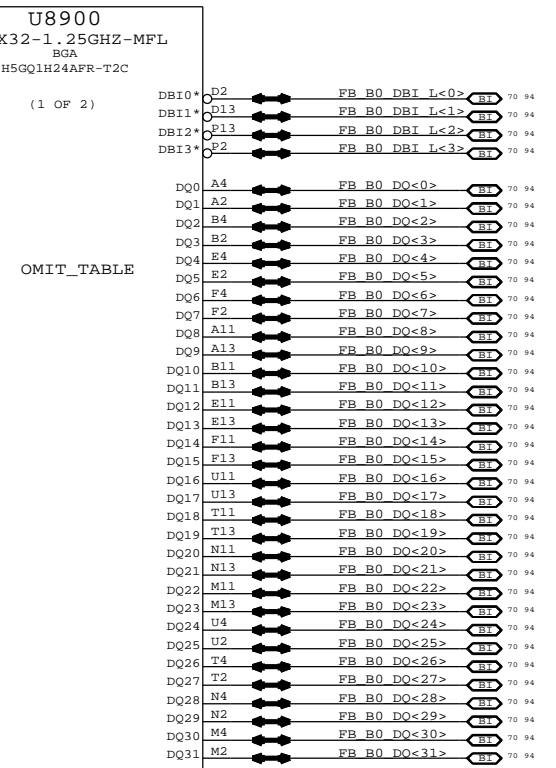
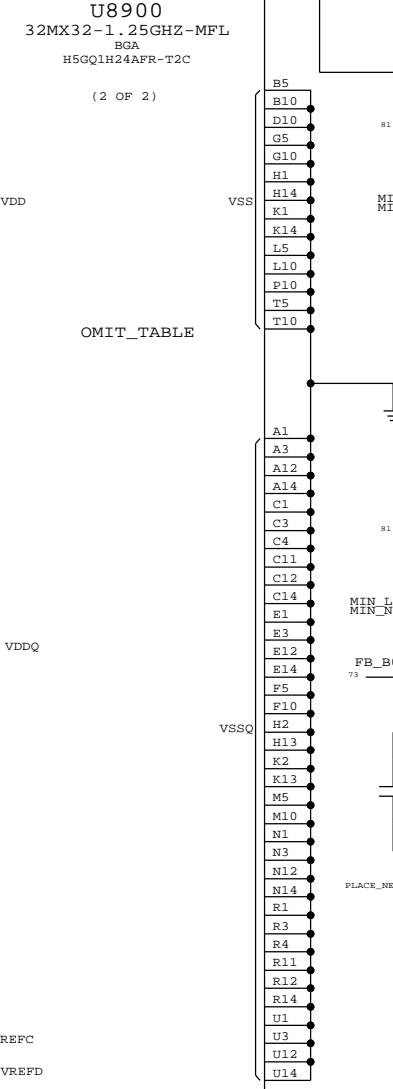
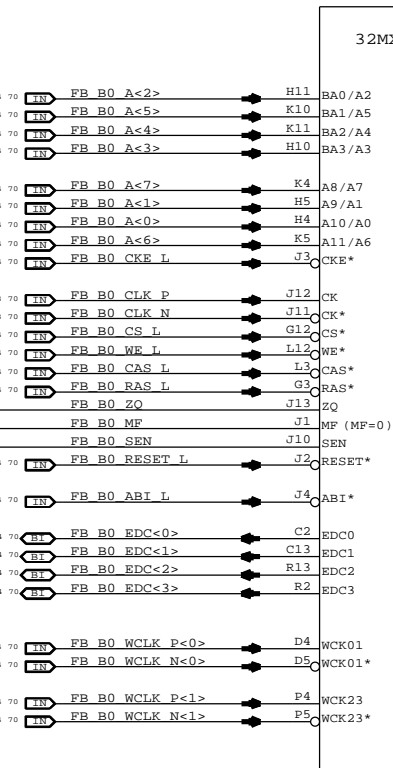
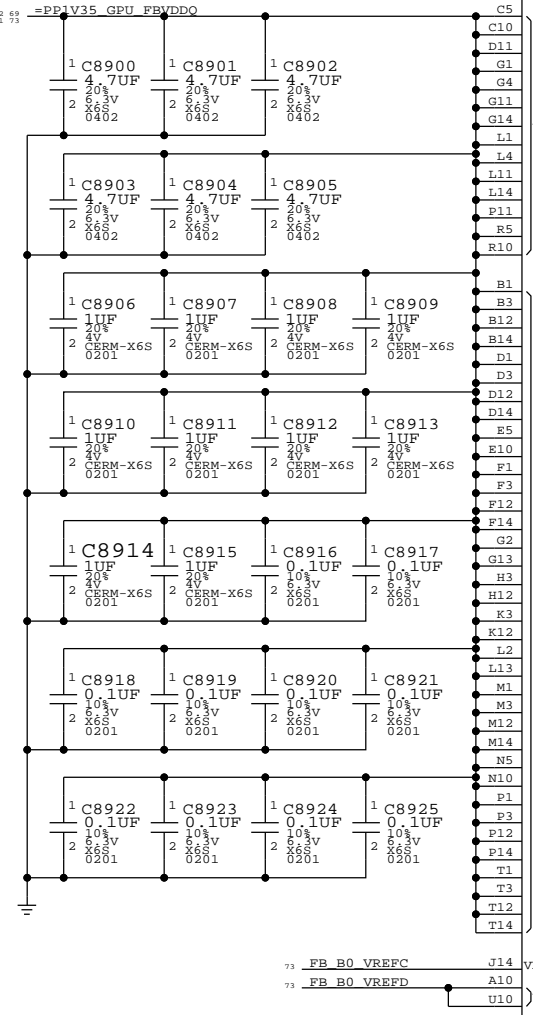
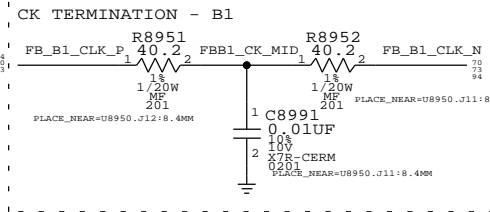
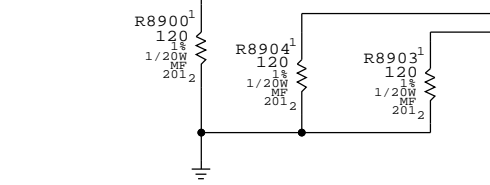
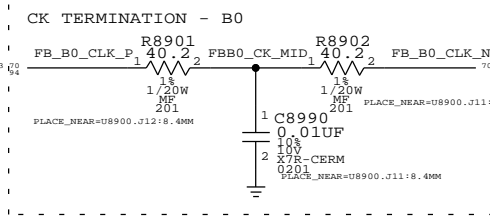
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Signal aliases required by this page:
BOM options provided by this page:



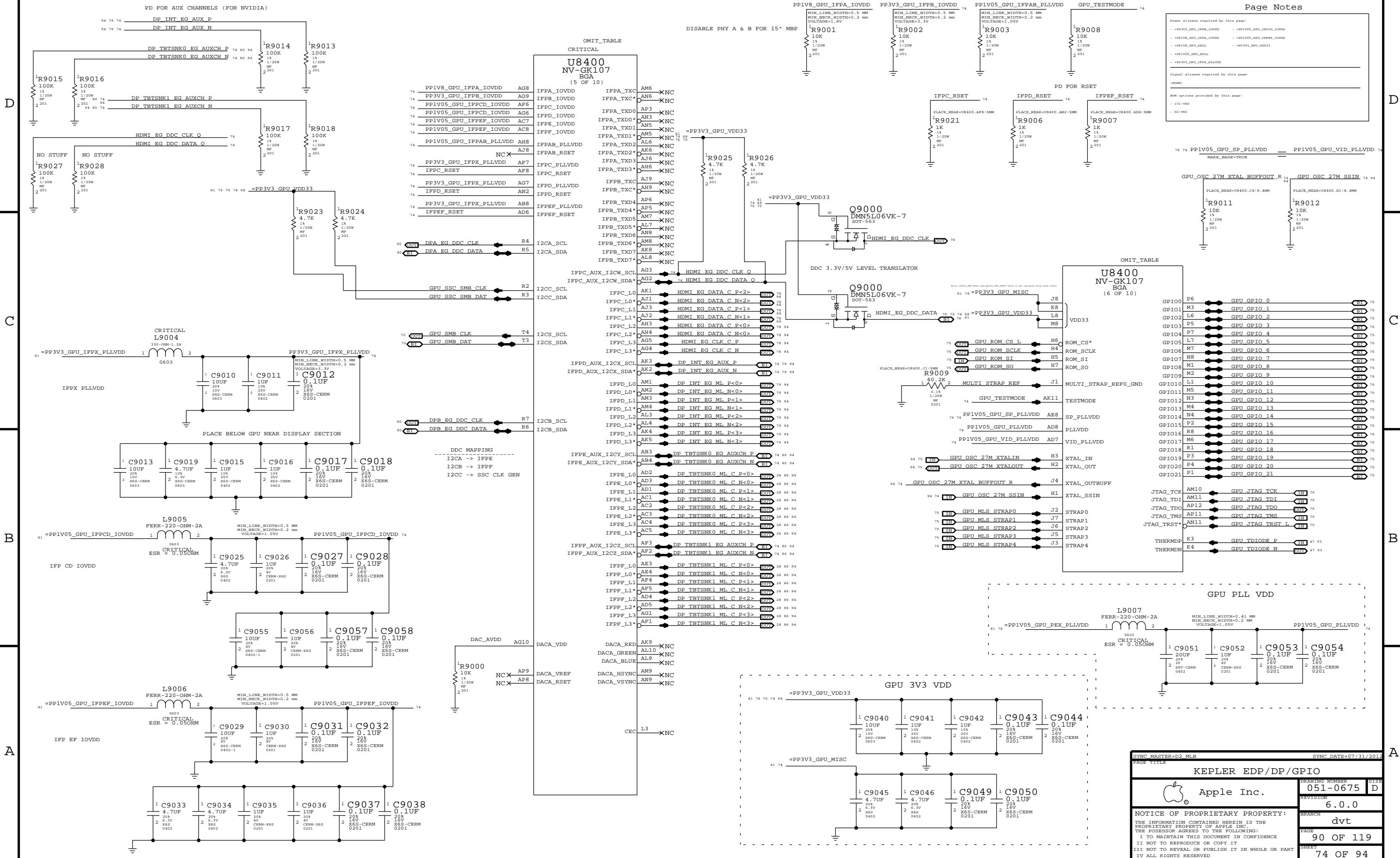
Apple Inc. GDDR5 Frame Buffer A
DRAWING NUMBER: 051-0675
REVISION: 6.0.0
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Apple Inc. GDDR5 Frame Buffer B
DRAWING NUMBER: 051-0675
REVISION: 6.0.0
PAGE: 89 OF 119
SYNCH MASTER=D2, MLEB
SYNC DATE=07/31/2012



Page Notes

Power aliases required by this page:

- PP3V3_GPU_IPFB_IOVDD
- PP3V3_GPU_IPFC_IOVDD
- PP3V3_GPU_IPFB_PLLVDD
- PP3V3_GPU_IPFE_IOVDD
- PP3V3_GPU_IPFB_PLVVDD
- PP3V3_GPU_IPFE_PLVVDD
- PP3V3_GPU_IPFB_PLVVDD
- PP3V3_GPU_IPFE_PLVVDD

Signal aliases required by this page:

(NONE)

SNW options provided by this page:

- J31YES
- D31YES

SYNC MASTER=D2 MLR SYNC DATE=07/31/2012

KEPLER EDP/DP/GPIO

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

PAGE: 90 OF 119

SHEET: 74 OF 94

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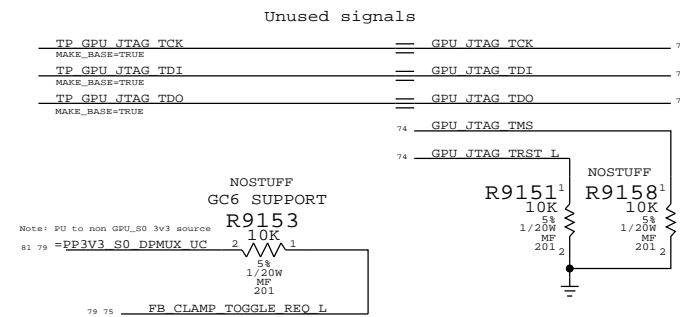
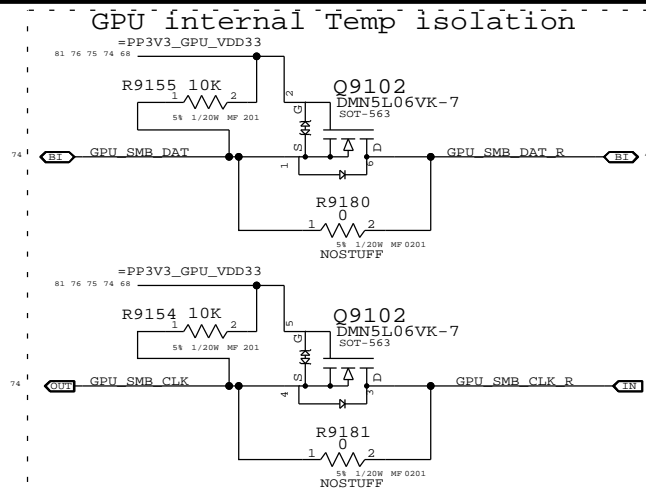
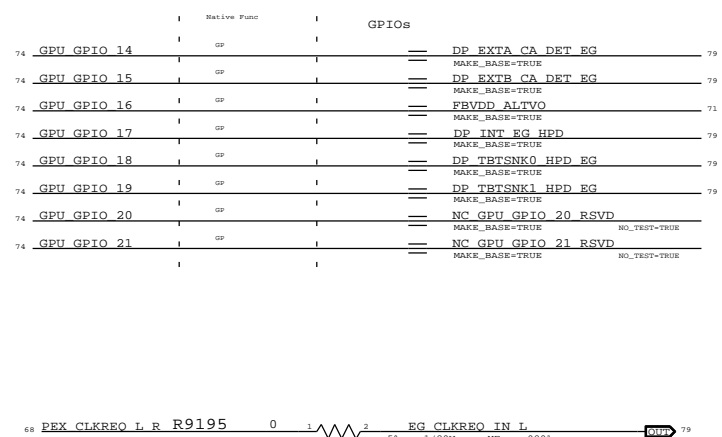
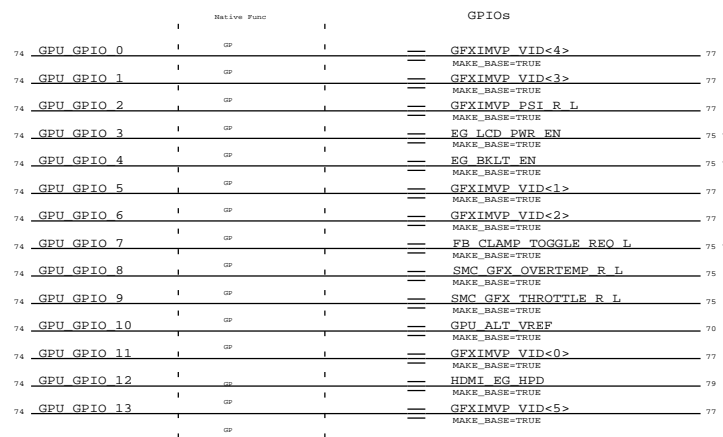
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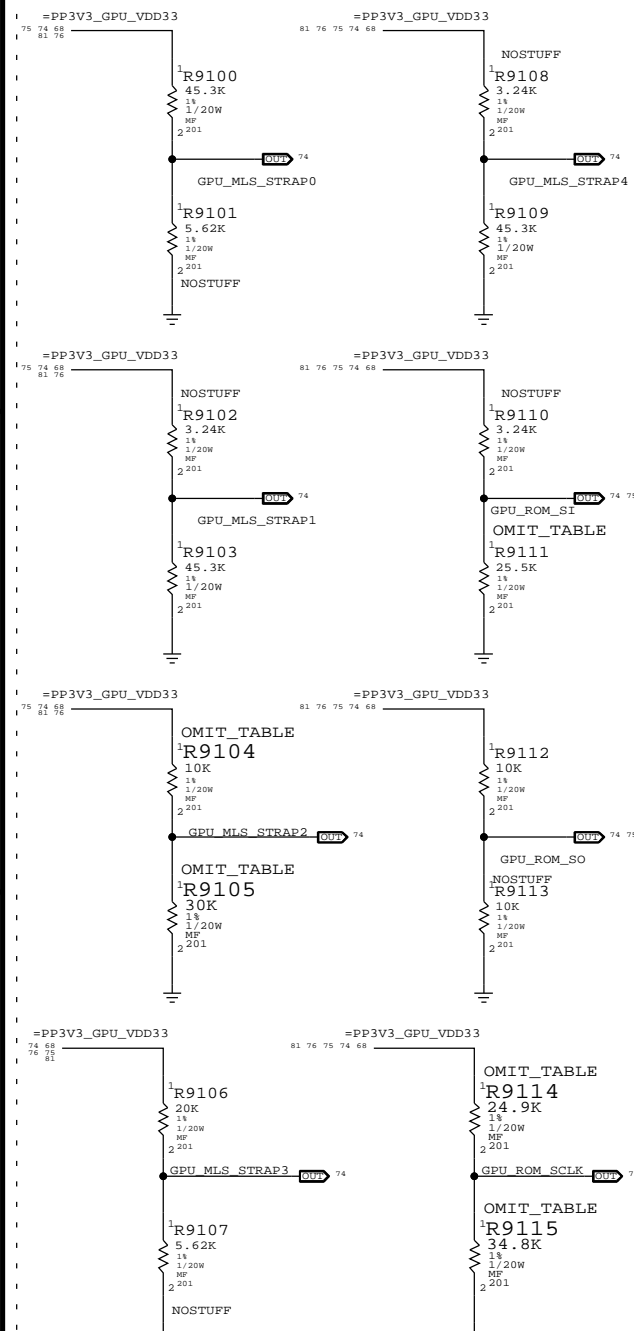
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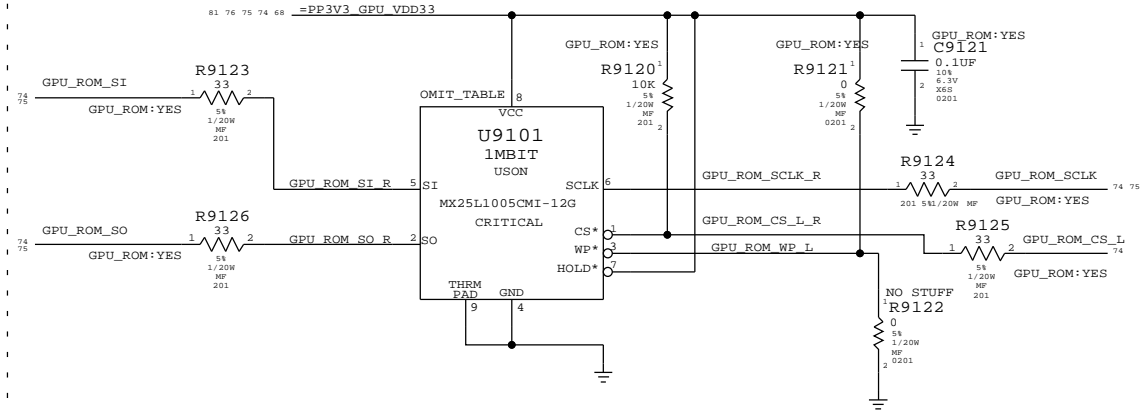


CONFIG STRAPS - MLPS



Straps for GK107. GF108 support has been removed.

GPU GC6 ROM

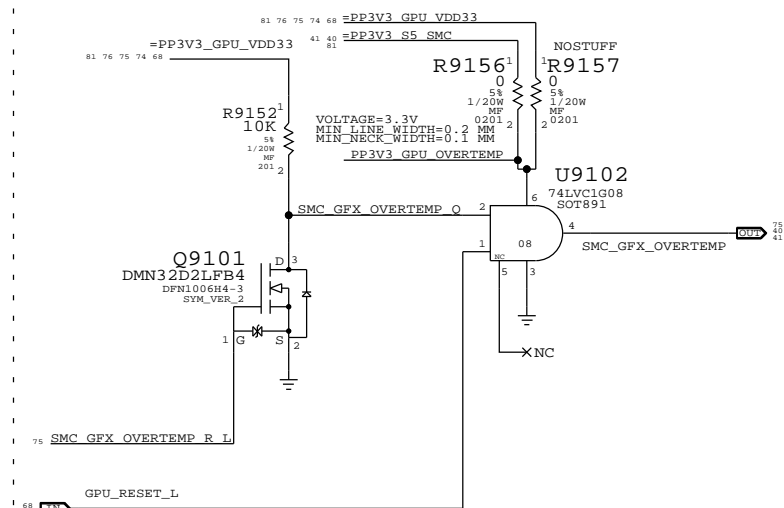


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118S0280	1	RES, MF, 30.1KOHM, 1.1/20W, 0201, 1%	R9111		FB_2G_ELPIDA
118S0013	1	RES, 10KOHM, 0201, 1%	R9111		FB_2G_HYNIX_29nm
118S0409	1	RES, 4.99 KOHM, 0201, 1%	R9111		FB_2G_ELPIDA_29nm
118S0105	1	RES, 15.0 KOHM, 0201, 1%	R9111		FB_4G_HYNIX
118S0013	1	RES, 10KOHM, 0201, 1%	R9104		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201, 1%	R9105		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201, 1%	R9105		GK107:GT
118S0013	1	RES, 10KOHM, 0201, 1%	R9114		GK107:GT

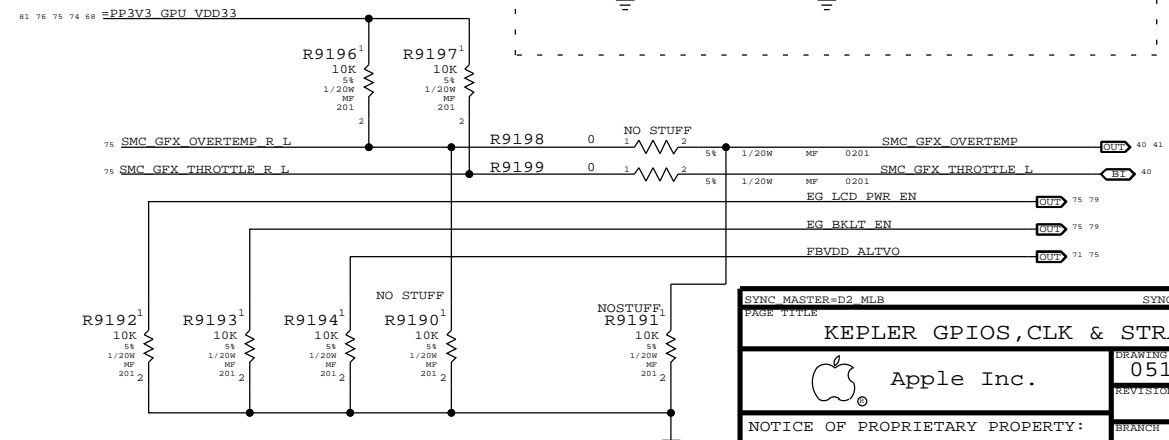
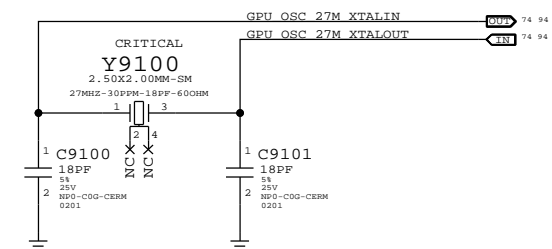
Die Rev	Strap
Hynix	0x4
ELPIDA	0x5
Hynix_29nm	0x1
ELPIDA_29nm	0x0

STRAP NOTES:
CURRENTLY STUFFED FOR GF108a/GK107-GTX
STUFF R9104 FOR THICK DIE
STUFF R9105 FOR THIN DIE

GPU overtemp masking



GPU XTAL 27 MHZ



SYNC MASTER=D2 MLB SYNC DATE=07/31/2012

KEPLER GPIOs, CLK & STRAPS

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

PAGE: 91 OF 119

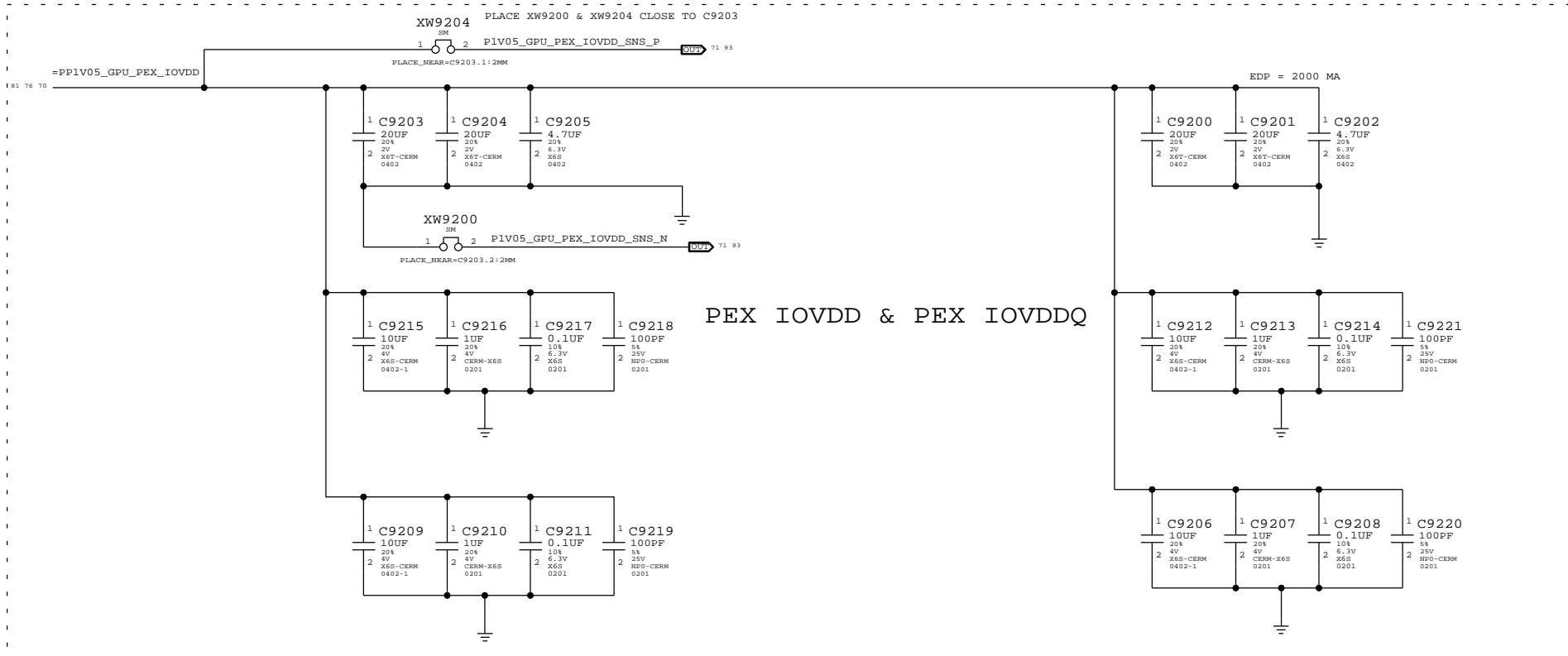
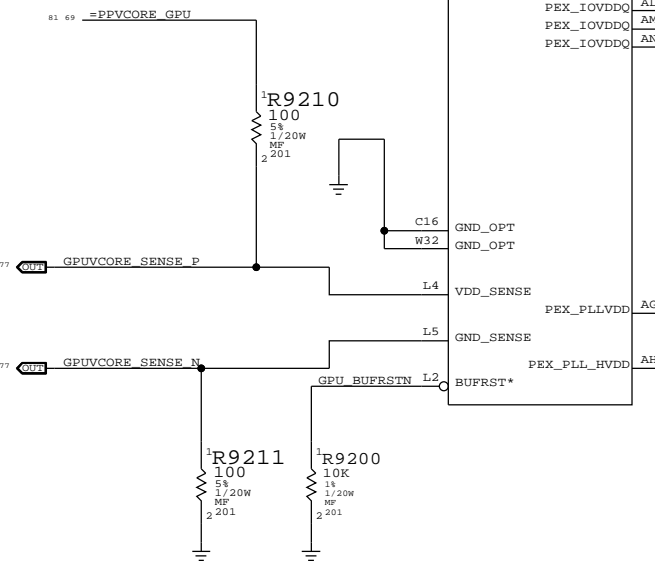
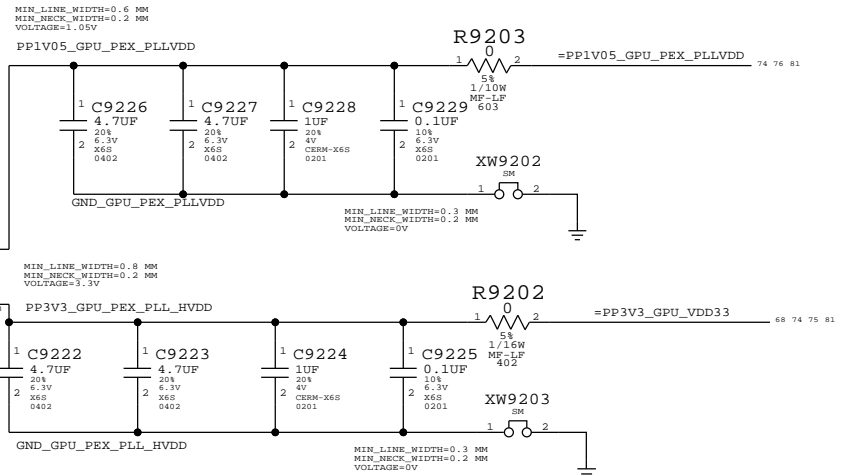
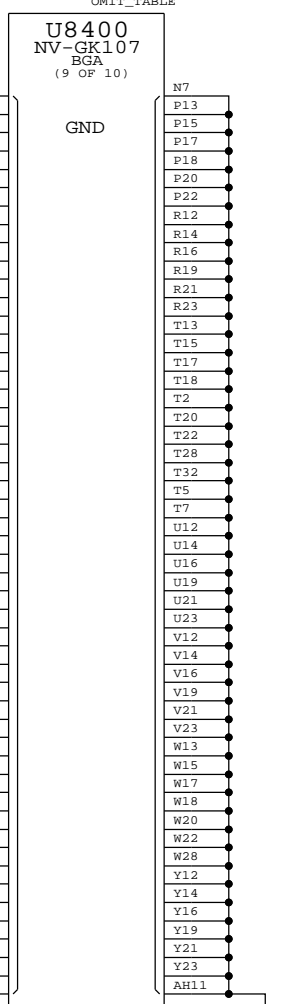
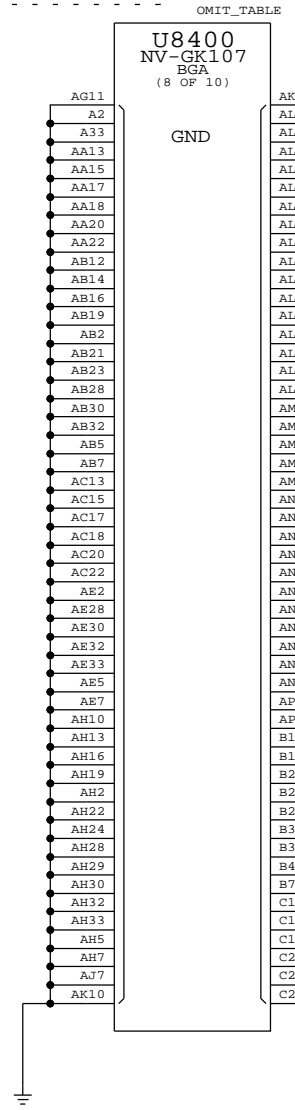
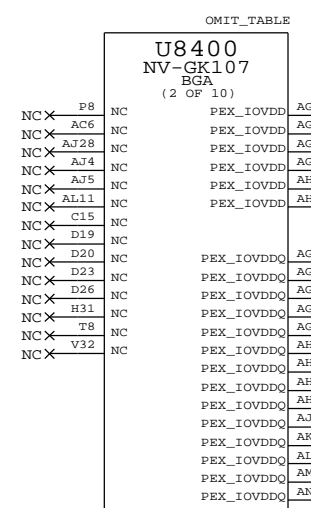
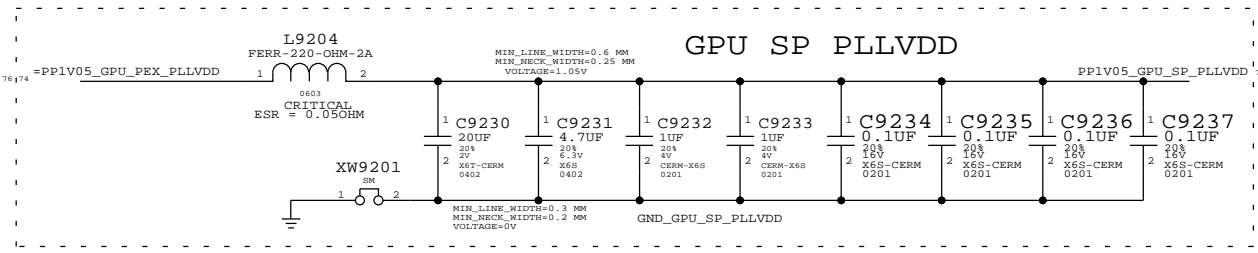
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Power aliases required by this page:
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 --PP1V05_GPU_PEX_PLLVDD
 --PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:
 (NONE)

Net options provided by this page:
 (NONE)



SYNC MASTER=D2_MLR		SYNC DATE=07/31/2012	
KEPLER PEX PWR/GNDS			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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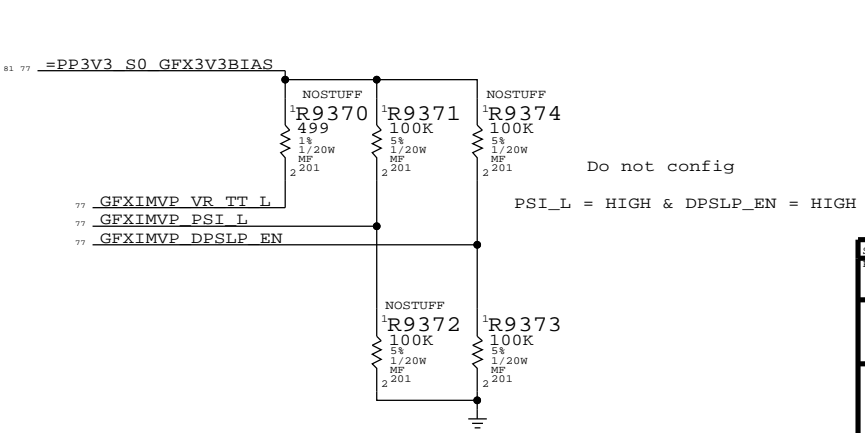
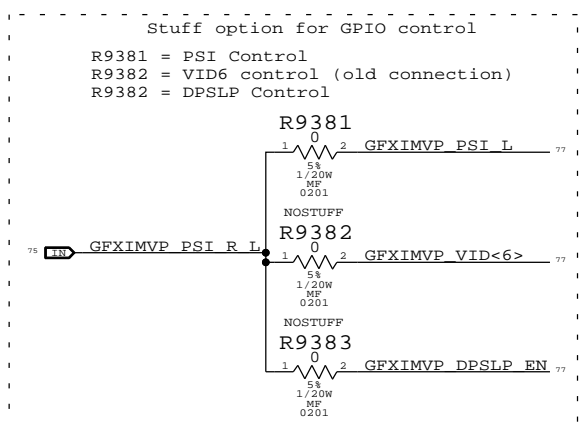
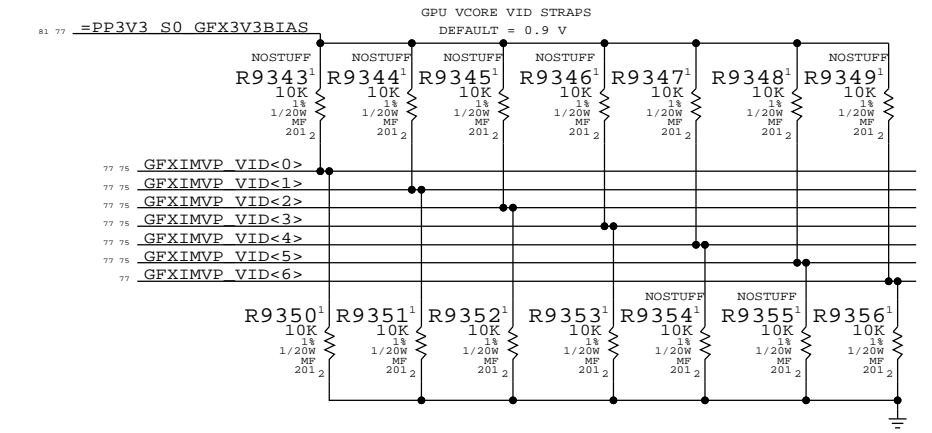
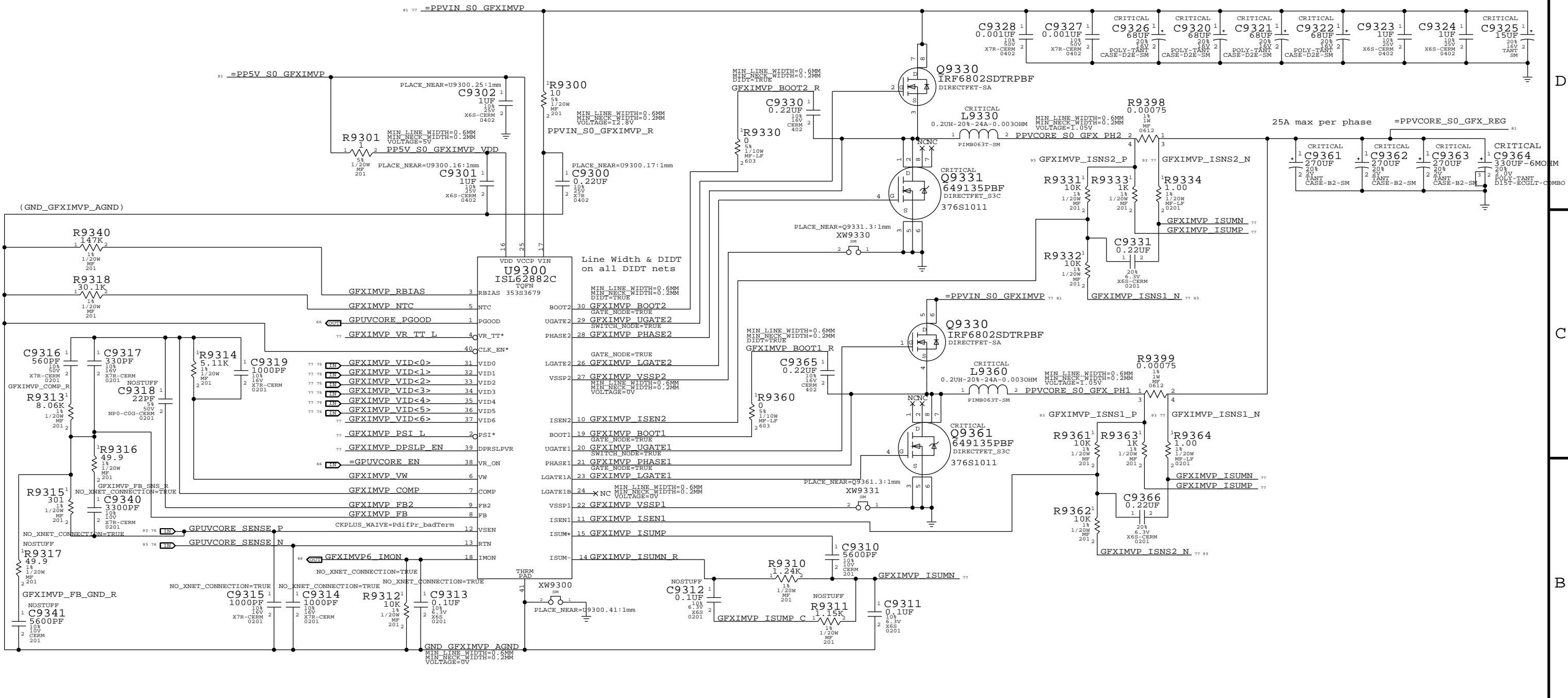
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B

B

A

A



SYNC MASTER=D2_MLB		SYNC DATE=07/31/2012	
PAGE TITLE			
GFX IMVP VCore Regulator			
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D

D

C

C

B

B

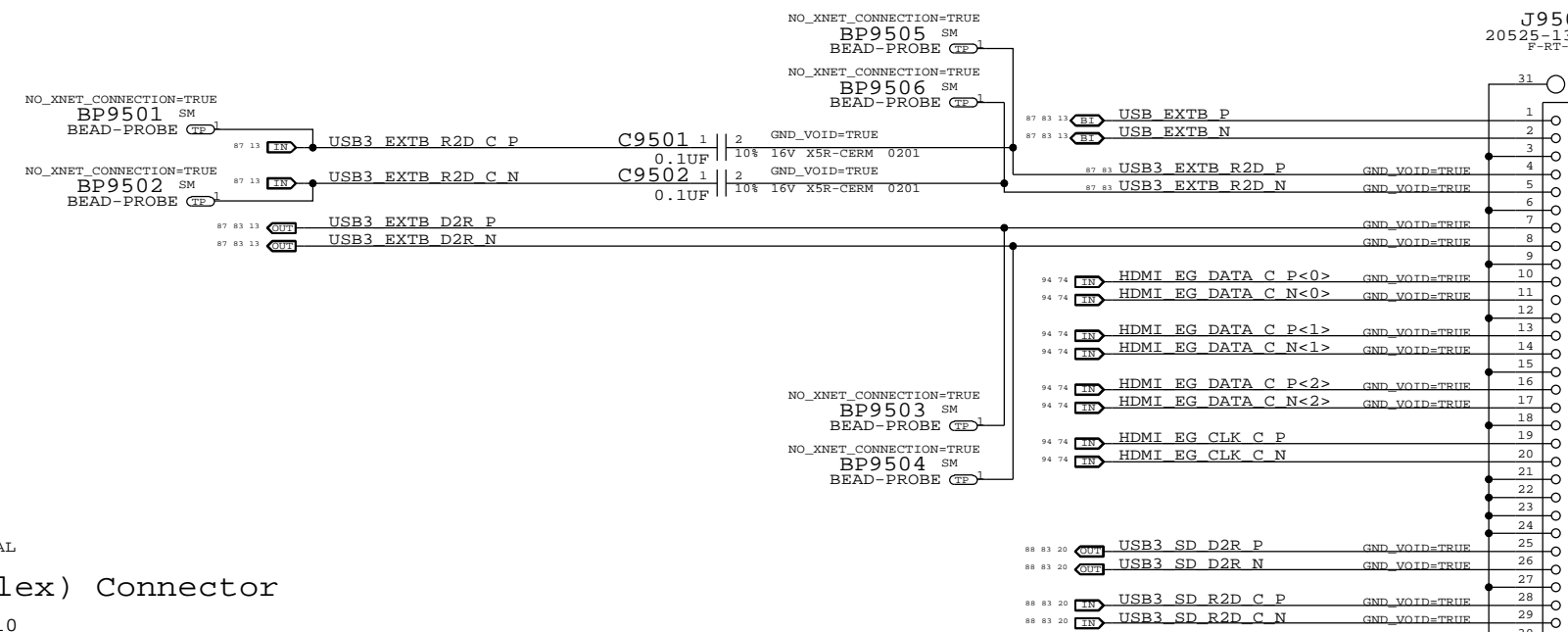
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Wire-to-Board (Micro-coax) Connector

CRITICAL

J9500
20525-130E-01
P-RT-SM

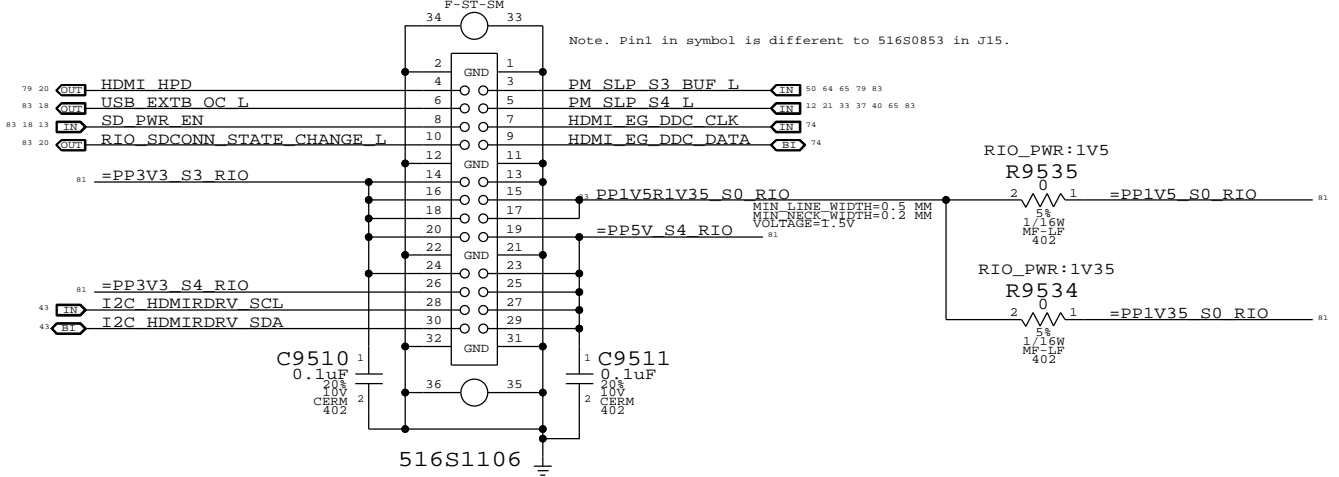


Board-to-Board (Flex) Connector

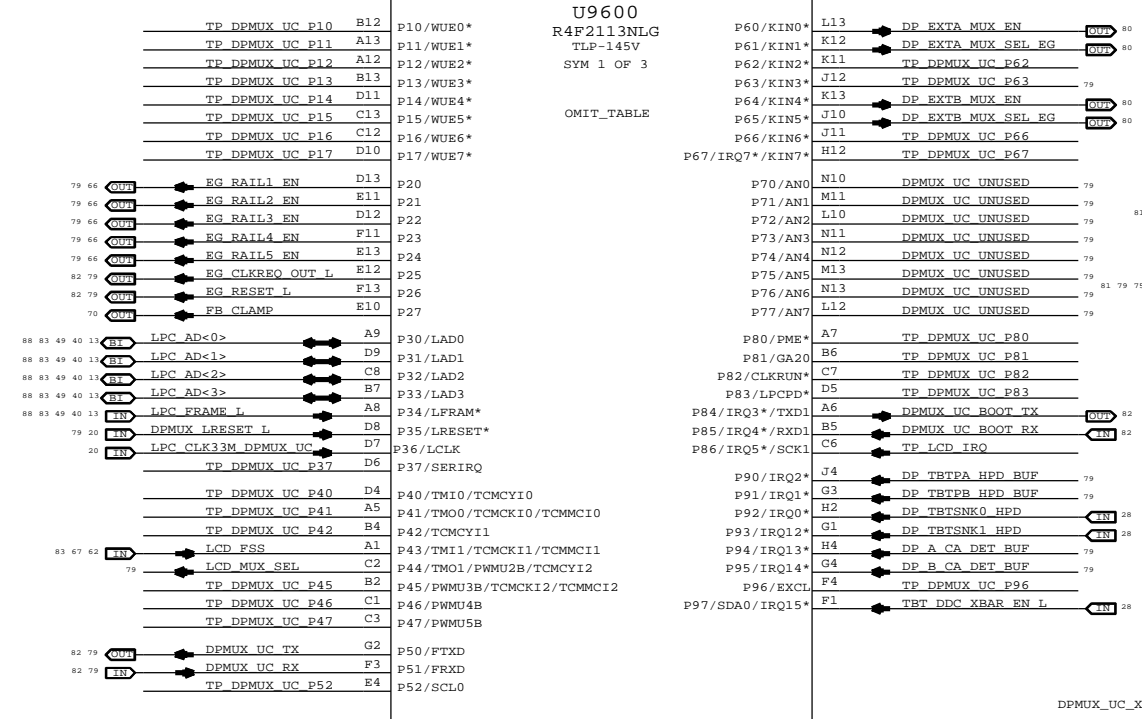
CRITICAL

J9510
20590-032E-25
F-ST-SM

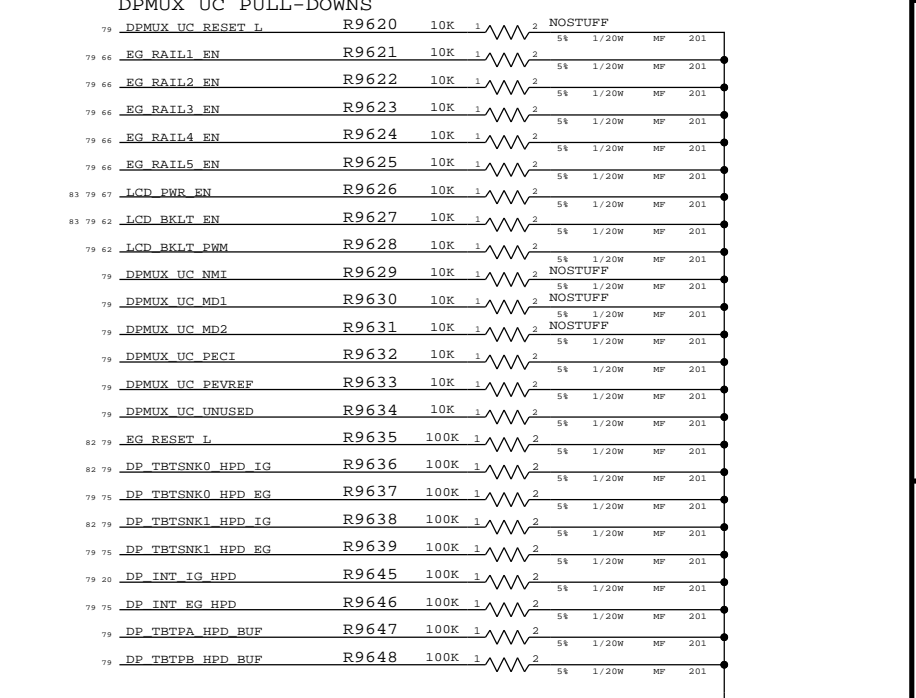
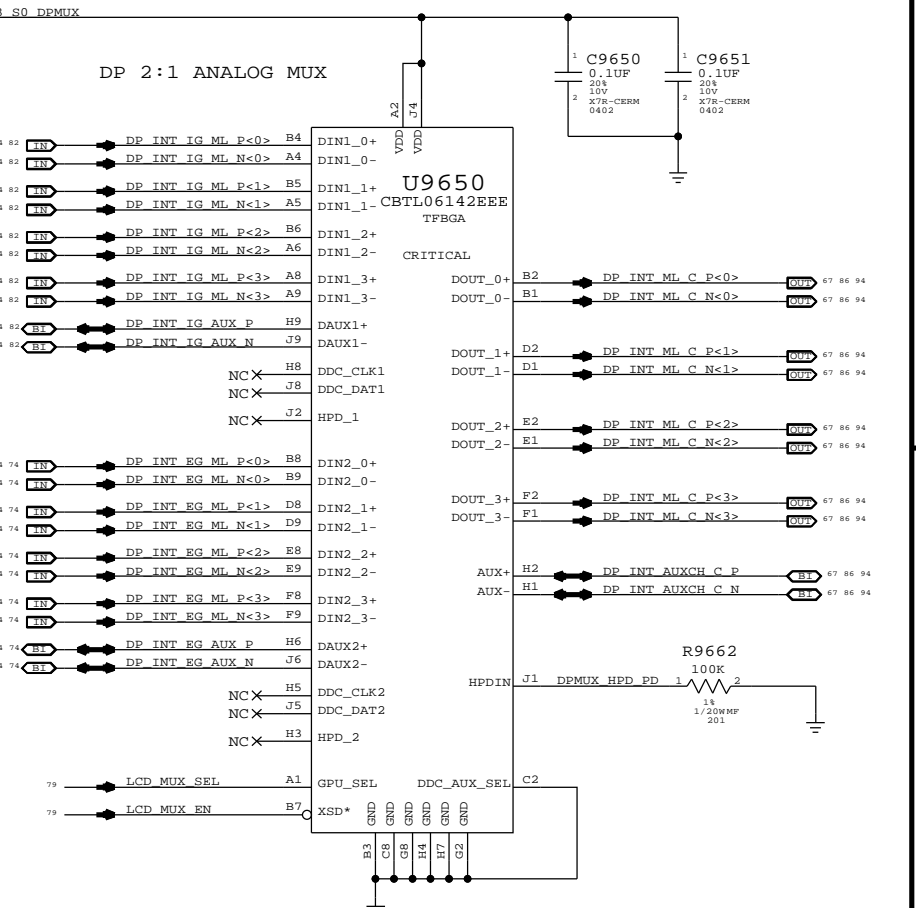
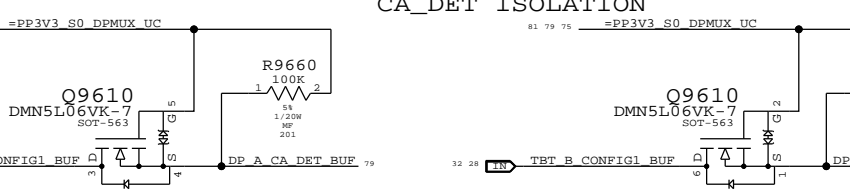
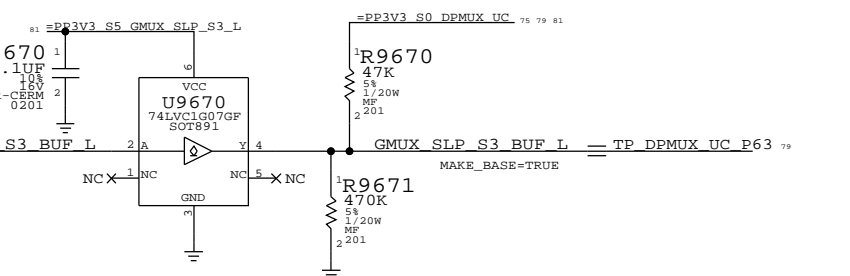
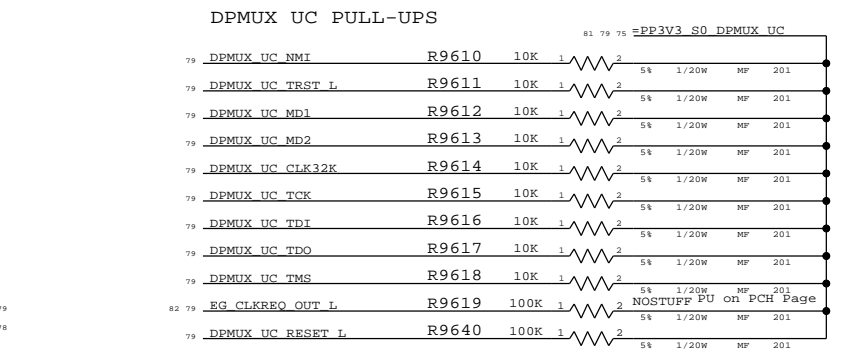
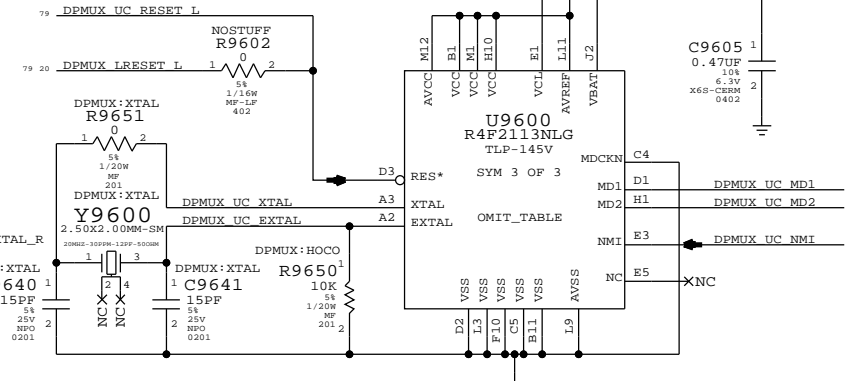
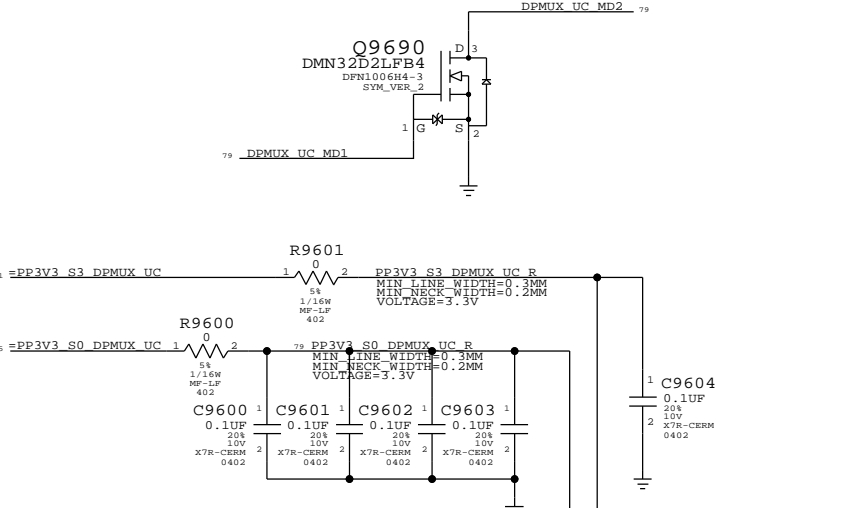
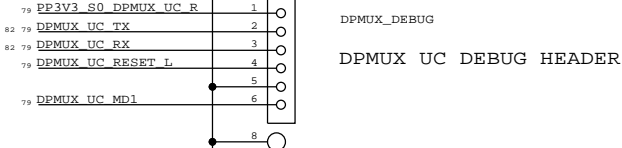
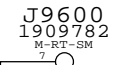
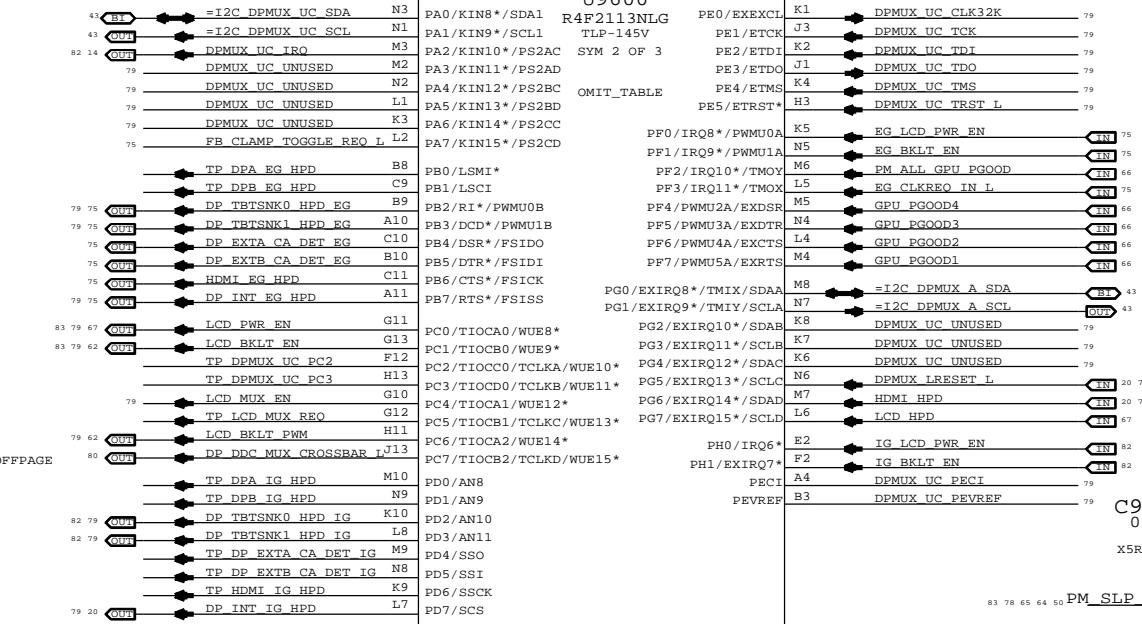
Note: Pin1 in symbol is different to 516S0853 in J15.



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RIO Connectors			
Apple Inc.	DRAWING NUMBER	051-0675	SIZE D
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CONNECT I2C TO LCD BKLT IC



Apple Inc. eDP Mux

Apple logo

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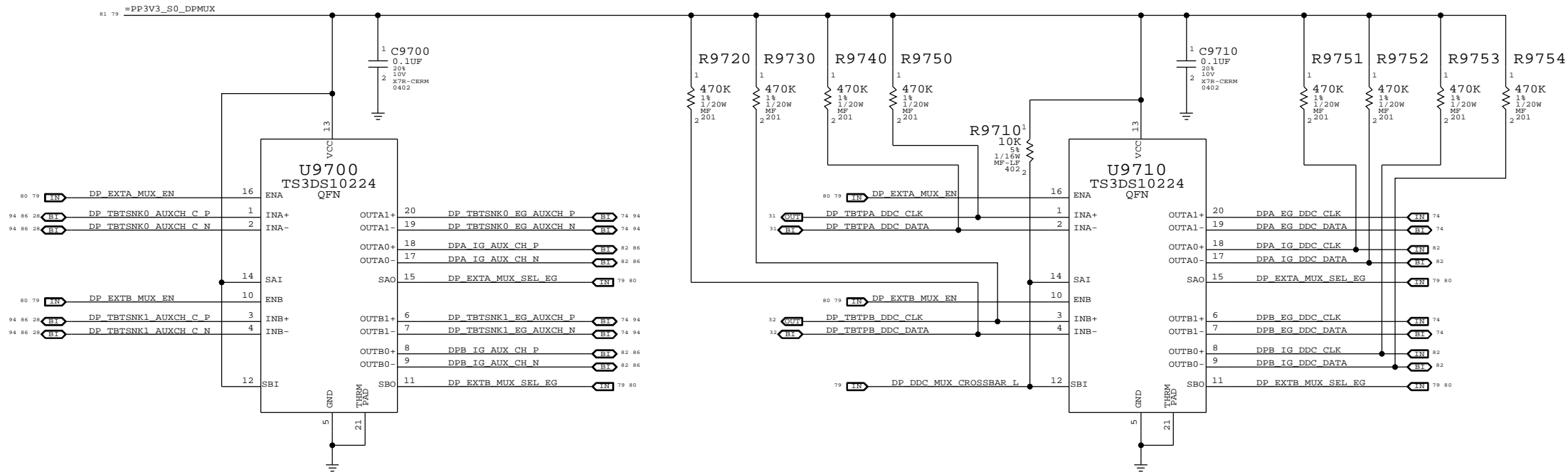
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DP A & DP B AUX MUX

DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC MASTER=CLEAN D2 SYNC DATE=08/14/2012

eDP Muxed Graphics Support

Apple Inc.

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REVISION: 6.0.0

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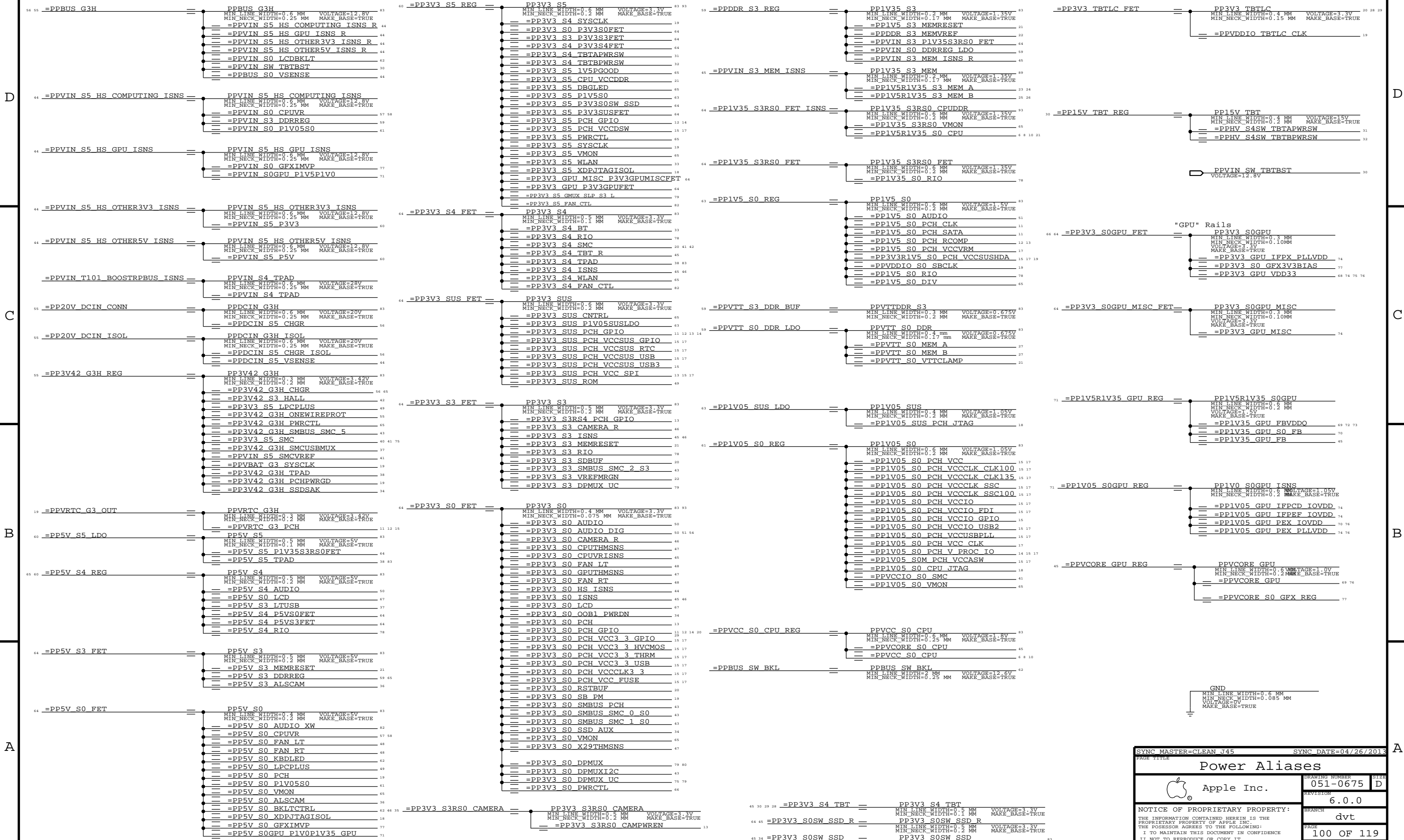
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G3H/5V Rails

3.3V Rails

1.5V/1.35V/1.05V/VCORE/BKLT Rails

TBT RAILS



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Power Aliases

Apple Inc.

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Display Aliases

```

12 EDP_IG_PANEL_PWR == IG_LCD_PWR_EN 79
MAKE_BASE=TRUE
12 EDP_IG_BKL_ON == IG_BKLT_EN 79
MAKE_BASE=TRUE

79 DP_INT_IG_ML_P<3..0> == TP_DP_IG_A_MLP<3..0> 5
MAKE_BASE=TRUE
79 DP_INT_IG_ML_N<3..0> == TP_DP_IG_A_MLN<3..0> 5
MAKE_BASE=TRUE
79 DP_INT_IG_AUX_P == TP_DP_IG_A_AUXCHP 5
MAKE_BASE=TRUE
79 DP_INT_IG_AUX_N == TP_DP_IG_A_AUXCHN 5
MAKE_BASE=TRUE

80 DPA_IG_AUX_CH_P == TP_DP_IG_B_AUXCHP 12
MAKE_BASE=TRUE
80 DPA_IG_AUX_CH_N == TP_DP_IG_B_AUXCHN 12
MAKE_BASE=TRUE
80 DPB_IG_AUX_CH_P == TP_DP_IG_C_AUXCHP 12
MAKE_BASE=TRUE
80 DPB_IG_AUX_CH_N == TP_DP_IG_C_AUXCHN 12
MAKE_BASE=TRUE
80 DPA_IG_DDC_CLK == TP_DP_IG_B_DDC_CLK 12
MAKE_BASE=TRUE
80 DPA_IG_DDC_DATA == TP_DP_IG_B_DDC_DATA 12
MAKE_BASE=TRUE
80 DPB_IG_DDC_CLK == TP_DP_IG_C_DDC_CLK 12
MAKE_BASE=TRUE
80 DPB_IG_DDC_DATA == TP_DP_IG_C_DDC_DATA 12
MAKE_BASE=TRUE

79 DP_TBTSNK0_HPD_IG == TP_DP_IG_B_HPD 12
MAKE_BASE=TRUE
79 DP_TBTSNK1_HPD_IG == TP_DP_IG_C_HPD 12
MAKE_BASE=TRUE

79 DPMUX_UC_RX == DPMUX_UC_BOOT_RX 79
MAKE_BASE=TRUE
79 DPMUX_UC_TX == DPMUX_UC_BOOT_TX 79
MAKE_BASE=TRUE

79 EG_RESET_L == GPU_RESET_L 68 75
MAKE_BASE=TRUE
81 PEG_CLKREQ_L == EG_CLKREQ_OUT_L 79
MAKE_BASE=TRUE

11 DP_AUXCH_ISOL_L == DP_AUXIO_EN
MAKE_BASE=TRUE

```

```

CPU signals
21 MEMVTT_EN == DDRVTT_EN 21 59
MAKE_BASE=TRUE

```

```

86 66 PEG_D2R_P<7..0> == PEG_D2R_P<7..0> 5
MAKE_BASE=TRUE
86 66 PEG_D2R_N<7..0> == PEG_D2R_N<7..0> 5
MAKE_BASE=TRUE
86 66 PEG_R2D_C_P<7..0> == PEG_R2D_C_P<7..0> 5
MAKE_BASE=TRUE
86 66 PEG_R2D_C_N<7..0> == PEG_R2D_C_N<7..0> 5
MAKE_BASE=TRUE

```

```

NC_PCIE_PEG_D2RP<15..12> == PEG_D2R_P<15..12> 5
MAKE_BASE=TRUE NO_TEST=TRUE
NC_PCIE_PEG_D2RN<15..12> == PEG_D2R_N<15..12> 5
MAKE_BASE=TRUE NO_TEST=TRUE
NC_PCIE_PEG_R2D_CP<15..12> == PEG_R2D_C_P<15..12> 5
MAKE_BASE=TRUE NO_TEST=TRUE
NC_PCIE_PEG_R2D_CN<15..12> == PEG_R2D_C_N<15..12> 5
MAKE_BASE=TRUE NO_TEST=TRUE

```

Thunderbolt Signals Through PEG

```

86 28 PCIE_TBT_D2R_P<3..0> == PEG_D2R_P<11..8> 5
MAKE_BASE=TRUE
86 28 PCIE_TBT_D2R_N<3..0> == PEG_D2R_N<11..8> 5
MAKE_BASE=TRUE
86 28 PCIE_TBT_R2D_C_P<3..0> == PEG_R2D_C_P<11..8> 5
MAKE_BASE=TRUE
86 28 PCIE_TBT_R2D_C_N<3..0> == PEG_R2D_C_N<11..8> 5
MAKE_BASE=TRUE

```

```

88 68 PEG_CLK100M_N == TP_PCIE_CLK100M_GPUN 11
MAKE_BASE=TRUE
88 68 PEG_CLK100M_P == TP_PCIE_CLK100M_GPUP 11
MAKE_BASE=TRUE

```

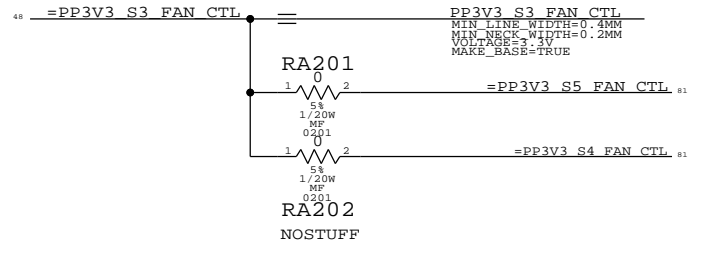
```

TP_P1V8GPU_EN == P1V8GPU_EN 66

```

Unused signals

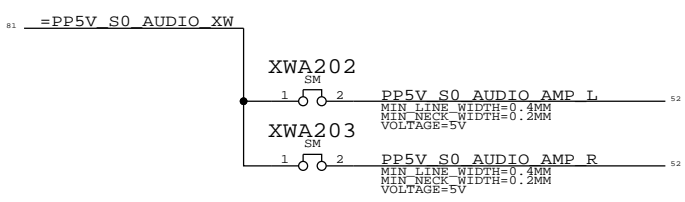
- 12 BT_PWRST_L
- 14 MEM_VDD_SEL_1V5_L
- 14 FW_PWR_EN_PCH
- 14 WOL_EN
- 14 FW_PME_L
- 14 DP_TBTT_SEL
- 11 ENET_MEDIA_SENSE_RDIV
- 12 AUD_IPHS_SWITCH_EN_PCH
- 12 AUD_IP_PERIPHERAL_DET
- 12 AUD_I2C_INT_L
- 14 TBT_GO2SX_BIDIR
- 79 14 DPMUX_UC_IRO
- 82 11 PEG_CLKREQ_L
- 11 ENET_CLKREQ_L
- 12 ENET_LOW_PWR_PCH
- 28 HDMITBTMUX_SEL_TBT
- 12 SDCONN_OC_L



```

89 86 24 23 22 PPVREF_S3_MEM_VREFDQ_A == 0.675V TRUE PP0V75_S3_MEM_VREFDQ_A
86 26 25 22 PPVREF_S3_MEM_VREFDQ_B == 0.675V TRUE PP0V75_S3_MEM_VREFDQ_B
89 86 24 23 22 PPVREF_S3_MEM_VREFCA_A == 0.675V TRUE PP0V75_S3_MEM_VREFCA_A
86 26 25 22 PPVREF_S3_MEM_VREFCA_B == 0.675V TRUE PP0V75_S3_MEM_VREFCA_B

```



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Signal Aliases			
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Functional Test Points

J3501 - airport		
TRUE	AP CLKREQ O L	33
TRUE	AP RESET CONN L	33
TRUE	PCIE AP D2R PI N	33 88
TRUE	PCIE AP D2R PI P	33 88
TRUE	PCIE AP R2D N	33 88
TRUE	PCIE AP R2D P	33 88
TRUE	PCIE CLK100M AP CONN N	33 88
TRUE	PCIE CLK100M AP CONN P	33 88
TRUE	PCIE WAKE L	12 33 88
TRUE	PP3V3 S3RS4 BT F	33
TRUE	PP3V3 WLAN	33 41
TRUE	USB BT CONN N	33 87
TRUE	USB BT CONN P	33 87
TRUE	WIFI EVENT L	33 40 41
TRUE	GND	4X

J4002 - Camera		
TRUE	MIPI CLK CONN N	36 91
TRUE	MIPI CLK CONN P	36 91
TRUE	CAM SENSOR WAKE L CONN	36
TRUE	MIPI DATA CONN N	36 91
TRUE	MIPI DATA CONN P	36 91
TRUE	=I2C ALS SDA	36 43
TRUE	=I2C ALS SCL	36 43
TRUE	I2C CAM SCK	35 36
TRUE	I2C CAM SDA	35 36
TRUE	PP5V S3RS0 ALSCAM F	36
TRUE	GND	

J9500 - rio coax		
TRUE	HDMI CLK N	86
TRUE	HDMI CLK P	86
TRUE	HDMI DATA N<0>	86
TRUE	HDMI DATA N<1>	86
TRUE	HDMI DATA N<2>	86
TRUE	HDMI DATA P<0>	86
TRUE	HDMI DATA P<1>	86
TRUE	HDMI DATA P<2>	86

USB3 SD D2R		
TRUE	USB3 SD D2R N	20 78 88
TRUE	USB3 SD D2R P	20 78 88
TRUE	USB3 SD R2D C N	20 78 88
TRUE	USB3 SD R2D C P	20 78 88
TRUE	USB3 EXTB D2R N	13 78 87
TRUE	USB3 EXTB D2R P	13 78 87
TRUE	USB3 EXTB R2D N	78 87
TRUE	USB3 EXTB R2D P	78 87
TRUE	USB EXTB N	13 78 87
TRUE	USB EXTB P	13 78 87
TRUE	GND	19X

J9510 - rio flex		
TRUE	SD PWR EN	13 18 78
TRUE	PP1V5R1V35 S0 RIO	78
TRUE	HDMI DDC CLK	
TRUE	HDMI DDC DATA	
TRUE	HDMI HPD L	
TRUE	SMBUS PCH CLK	13 43 88
TRUE	SMBUS PCH DATA	13 43 88
TRUE	PM SLP S3 BUF L	50 64 65 78 79
TRUE	PM SLP S4 L	12 21 33 37 40 65 78
TRUE	PP3V3 S3	3X 81 83
TRUE	PP3V3 S4	81 83
TRUE	PP5V S4	5X 81
TRUE	RIO SDCONN STATE CHANGE L	20 78
TRUE	USB EXTB OC L	18 78
TRUE	GND	10X

J5150 - hall effect		
TRUE	PP3V42 G3H	81 83
TRUE	SMC LID R	42
TRUE	GND	

J6050 - left fan		
TRUE	FAN LT PWM	48
TRUE	FAN LT TACH	48
TRUE	PP5V S0	3X 81 83
TRUE	GND	5X

J6060 - right fan		
TRUE	FAN RT PWM	48
TRUE	FAN RT TACH	48
TRUE	PP5V S0	3X 81 83
TRUE	GND	5X

J6100 - lpc + spi		
TRUE	LPCPLUS GPIO	14 49
TRUE	LPCPLUS RESET L	20 49
TRUE	LPC AD<0>	13 40 49 79 88
TRUE	LPC AD<1>	13 40 49 79 88
TRUE	LPC AD<2>	13 40 49 79 88
TRUE	LPC AD<3>	13 40 49 79 88
TRUE	LPC CLK33M LPCPLUS	19 49 88
TRUE	LPC FRAME L	13 40 49 79 88
TRUE	LPC PWRDWN L	13 40 49 79 88
TRUE	LPC SERIRO	13 40 49
TRUE	PM CLKRUN L	13 40 49
TRUE	PP5V S0	81 83
TRUE	SMC RESET L	40 41 49 56
TRUE	SMC ROMBOOT	41 49
TRUE	SMC RX L	40 41 49
TRUE	SMC TCK	40 41 49
TRUE	SMC TDI	40 41 49
TRUE	SMC TDO	40 41 49
TRUE	SMC TMS	40 41 49
TRUE	SMC TX L	40 41 49
TRUE	SPIROM USE MLB	14 49
TRUE	SPI ALT CLK	49
TRUE	SPI ALT CS L	49
TRUE	SPI ALT MISO	49
TRUE	SPI ALT MOSI	49
TRUE	TP SMC MD1	49
TRUE	TP SMC TRST L	49
TRUE	GND	2X

J4800 - ipd flex		
TRUE	Z2 CS L	38
TRUE	Z2 MOSI	38
TRUE	Z2 MISO	38
TRUE	Z2 SCLK	38
TRUE	Z2 HOST INTN	38
TRUE	Z2 CLKIN	38
TRUE	Z2 KEY ACT L	38
TRUE	PSOC F CS L	38
TRUE	PICKB L	38
TRUE	PSOC MOSI	38
TRUE	PSOC MISO	38
TRUE	PSOC SCLK	38
TRUE	=I2C TPAD SCL	38 43
TRUE	=I2C TPAD SDA	38 43
TRUE	SMC LID	38 40 41 42
TRUE	SMC T101 COM 1	
TRUE	=PP3V3 S4 TPAD	38 81
TRUE	=PP5V S5 TPAD	38 81
TRUE	GND	2X

J4813 - keyboard		
TRUE	PP3V3 S4	81 83
TRUE	PP3V42 G3H	81 83
TRUE	WS CONTROL KBD	38
TRUE	WS KBD1	38
TRUE	WS KBD10	38
TRUE	WS KBD11	38
TRUE	WS KBD12	38
TRUE	WS KBD13	38
TRUE	WS KBD14	38
TRUE	WS KBD15 CAP	38
TRUE	WS KBD16 NUM	38
TRUE	WS KBD17	38
TRUE	WS KBD18	38
TRUE	WS KBD19	38
TRUE	WS KBD2	38
TRUE	WS KBD20	38
TRUE	WS KBD21	38
TRUE	WS KBD22	38
TRUE	WS KBD23	38
TRUE	WS KBD3	38
TRUE	WS KBD4	38
TRUE	WS KBD5	38
TRUE	WS KBD6	38
TRUE	WS KBD7	38
TRUE	WS KBD8	38
TRUE	WS KBD9	38
TRUE	WS KBD ONOFF L	38
TRUE	WS LEFT OPTION KBD	38
TRUE	WS LEFT SHIFT KBD	38
TRUE	GND	2X

J4915 - kbd bklt		
TRUE	KBDBKLT RETURN1	2X 39 42
TRUE	KBDBKLT RETURN2	2X 39 42
TRUE	PPVOUT S0 KBDBKLT	39 42
TRUE	GND	4X

J6701 - audio flex		
TRUE	AUD HP PORT L	50 54
TRUE	AUD HP PORT R	50 54
TRUE	AUD SPDIF OUT JACK	
TRUE	AUD TYPDET INV	
TRUE	AUD TYPDET	50 54
TRUE	AUD CONN MIC XW	4X
TRUE	CH HS MIC	
TRUE	PP3V3 S0	81 83 93
TRUE	AUD CONN SLEEVE XW	4X 53 54
TRUE	US HS MIC	
TRUE	GND	2X GND

J6601 - mic		
TRUE	DMIC CLK3	51 54
TRUE	PP3V3 S0	81 83 93
TRUE	DMIC SDA2	54
TRUE	DMIC SDA3	51 54
TRUE	GND	

J6602 - L speaker		
TRUE	SPKRCONN L ID	51 54
TRUE	SPKRCONN L OUT N	52 54 93
TRUE	SPKRCONN L OUT P	52 54 93
TRUE	SPKRCONN SL OUT N	52 54 93
TRUE	SPKRCONN SL OUT P	52 54 93
TRUE	GND	

J6603 - R speaker		
TRUE	SPKRCONN R ID	51 54
TRUE	SPKRCONN R OUT N	52 54 93
TRUE	SPKRCONN R OUT P	52 54 93
TRUE	SPKRCONN SR OUT N	52 54 93
TRUE	SPKRCONN SR OUT P	52 54 93
TRUE	GND	

J7000 - DC PWR		
TRUE	ADAPTER SENSE	55
TRUE	PP20V DCIN FUSE	2X 55
TRUE	GND	2X

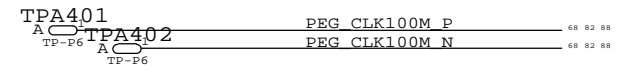
J7050 - battery		
TRUE	PPVBAT G3H CONN	8X 55 66
TRUE	SMBUS SMC 5 G3 SCL	40 43 92
TRUE	SMBUS SMC 5 G3 SDA	40 43 92
TRUE	SYS DETECT L	55
TRUE	GND	8X

J8300 - eDP		
TRUE	DP INT AUX N	67 86 94
TRUE	DP INT AUX P	67 86 94
TRUE	DP INT ML N<0>	67 86 94
TRUE	DP INT ML N<1>	67 86 94
TRUE	DP INT ML N<2>	67 86 94
TRUE	DP INT ML N<3>	67 86 94
TRUE	DP INT ML P<0>	67 86 94
TRUE	DP INT ML P<1>	67 86 94
TRUE	DP INT ML P<2>	67 86 94
TRUE	DP INT ML P<3>	67 86 94
TRUE	LCD FSS	62 67 79
TRUE	LCD HPD CONN	67
TRUE	LED RETURN 1	62 67
TRUE	LED RETURN 2	62 67
TRUE	LED RETURN 3	62 67
TRUE	LED RETURN 4	62 67
TRUE	LED RETURN 5	62 67
TRUE	LED RETURN 6	62 67
TRUE	PP5VR3V3 SW LCD	3X 67
TRUE	PPVOUT S0 LCDBKLT	62 67
TRUE	GND	16X

Power Rails		
TRUE	PM SLP S3 L	12 21 40 65
TRUE	PPVTT S0 DDR	81
TRUE	PP3V3 S0	81 83 93
TRUE	PP3V3 S3	81 83
TRUE	PP3V3 S5	81 83
TRUE	PP3V3 S5 AVREF SMC	40 41
TRUE	PP3V42 G3H	81 83
TRUE	PP5V S0	81 83
TRUE	PP5V S3	81
TRUE	PP5V S5	81
TRUE	PPBUS G3H	81
TRUE	PPDCIN G3H	81
TRUE	PPVCC S0 CPU	81
TRUE	PPVTDDR S3	81
TRUE	PP3V3 S0SW SSD	81
TRUE	PP1V5 S0	81
TRUE	PP1V35 S3	81

XDP		
TRUE	XDP CPU TCK	6 18 86
TRUE	XDP PCH TCK	11 18
TRUE	XDP CPU TDI	6 18 86
TRUE	XDP CPU TDO	6 18 86
TRUE	XDP CPU TRST L	6 18 86
TRUE	XDP CPU TMS	6 18 86
TRUE	XDP PCH TMS	11 18
TRUE	XDP PCH TDI	11 18
TRUE	XDP PCH TDO	11 18
TRUE	XDP CPU PREQ L	6 18 86
TRUE	XDP CPU PRDY L	6 18 86
TRUE	PM RSMRST L	12 65 88
TRUE	PM PCH PWROK	12 19 88
TRUE	PM SYSRST L	12 19 40 88
TRUE	CPU CFG<3>	6 18 86
TRUE	PP1V05 S0	81
TRUE	GND	2X GND

Power Sequence		
TRUE	SMC ONOFF L	38 40 41
TRUE	PM DSW PWRGD	12 40 88
TRUE	ALL SYS PWRGD	18 19 40 65
TRUE	PM PCH SYS PWROK	12 18 19 40 88
TRUE	PLT RESET L	12 18 20 21
TRUE	LCD PWR EN	67 79
TRUE	LCD BKLT EN	62 79



SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

Functional Test Points

Apple Inc.

DRAWING NUMBER: 051-0675
REVISION: 6.0.0

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NC NO_TESTS

PCH

	NO_TEST	MAKE_BASE		
13	TP_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
13	TP_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
13	TP_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
13	TP_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
13	USB3_EXTC_D2R_N	TRUE	TRUE	NC_USB3_EXTC_D2RN
13	USB3_EXTC_D2R_P	TRUE	TRUE	NC_USB3_EXTC_D2RP
13	USB3_EXTC_R2D_C_N	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
13	USB3_EXTC_R2D_C_P	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
13	USB3_EXTD_D2R_N	TRUE	TRUE	NC_USB3_EXTD_D2RN
13	USB3_EXTD_D2R_P	TRUE	TRUE	NC_USB3_EXTD_D2RP
13	USB3_EXTD_R2D_C_N	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
13	USB3_EXTD_R2D_C_P	TRUE	TRUE	NC_USB3_EXTD_R2D_CP

PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP

11	SATA_A_D2R_N	TRUE	TRUE	NC_SATA_A_D2RN
11	SATA_A_D2R_P	TRUE	TRUE	NC_SATA_A_D2RP
11	SATA_A_R2D_C_N	TRUE	TRUE	NC_SATA_A_R2D_CN
11	SATA_A_R2D_C_P	TRUE	TRUE	NC_SATA_A_R2D_CP
11	SATA_B_D2R_N	TRUE	TRUE	NC_SATA_B_D2RN
11	SATA_B_D2R_P	TRUE	TRUE	NC_SATA_B_D2RP
11	SATA_B_R2D_C_N	TRUE	TRUE	NC_SATA_B_R2D_CN
11	SATA_B_R2D_C_P	TRUE	TRUE	NC_SATA_B_R2D_CP
11	TP_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
11	TP_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
11	TP_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
11	TP_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
11	TP_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
11	TP_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
11	TP_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
11	TP_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
11	TP_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
11	TP_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
11	TP_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
11	TP_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP

13	USB_EXTC_N	TRUE	TRUE	NC_USB_EXTCN
13	USB_EXTC_P	TRUE	TRUE	NC_USB_EXTCP
13	TP_USB_SDN	TRUE	TRUE	NC_USB_SDN
13	TP_USB_SDP	TRUE	TRUE	NC_USB_SDP
13	TP_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
13	TP_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
13	TP_USB_6N	TRUE	TRUE	NC_USB_6N
13	TP_USB_6P	TRUE	TRUE	NC_USB_6P
13	TP_USB_7N	TRUE	TRUE	NC_USB_7N
13	TP_USB_7P	TRUE	TRUE	NC_USB_7P
13	USB_EXTD_N	TRUE	TRUE	NC_USB_EXTDN
13	USB_EXTD_P	TRUE	TRUE	NC_USB_EXTDP
13	TP_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
13	TP_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
13	USB_IR_N	TRUE	TRUE	NC_USB_IRN
13	USB_IR_P	TRUE	TRUE	NC_USB_IRP

86	ITPXDP_CLK100M_N	TRUE	TRUE	NC_ITPXDP_CLK100MN
86	ITPXDP_CLK100M_P	TRUE	TRUE	NC_ITPXDP_CLK100MP
12	TP_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
20	TP_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
21	TP_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
11	TP_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
11	TP_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
11	TP_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
13	TP_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
13	TP_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
13	TP_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
13	TP_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L

12	EDP_IG_BKL_PWM	TRUE	TRUE	NC_EDP_IG_BKL_PWM
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87	USB_SMC_P	TRUE	TRUE	NC_USB_SMCP
87	USB_SMC_N	TRUE	TRUE	NC_USB_SMCN

SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2
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Thunderbolt

	NO_TEST	MAKE_BASE		
28	TP_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT

28	TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
28	TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
28	TP_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
28	TP_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN

12	TP_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
12	TP_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP

11	TP_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
11	TP_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
11	PCIE_CLK100M_ENETSD_N	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
11	PCIE_CLK100M_ENETSD_P	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
11	TP_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
11	TP_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
11	TP_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
11	TP_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
11	TP_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
11	TP_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP

11	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
11	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
11	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
11	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

13	TP_USB_4N	TRUE	TRUE	NC_USB_4N
13	TP_USB_4P	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	28	86
TRUE	PCIE_TBT_R2D_N<3..0>	28	86
TRUE	PCIE_TBT_D2R_C_P<3..0>	28	86
TRUE	PCIE_TBT_D2R_C_N<3..0>	28	86

TRUE	DMI_S2N_P<3..1>	5	12	86
TRUE	DMI_S2N_N<3..1>	5	12	86
TRUE	DMI_N2S_P<3..1>	5	12	86
TRUE	DMI_N2S_N<3..1>	5	12	86

PLACEABLE BEAD-PROBES FOR TBT

90	11	28	TBT_A_R2D_C_P<1>	CTD _{SM}	BEAD-PROBE	BPA535	NO_XNET_CONNECTION=TRUE
90	11	28	TBT_A_D2R_P<1>	CTD _{SM}	BEAD-PROBE	BPA531	NO_XNET_CONNECTION=TRUE
90	11	28	TBT_A_D2R_N<1>	CTD _{SM}	BEAD-PROBE	BPA532	NO_XNET_CONNECTION=TRUE

D

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C

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B

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A

A

SYNC_MASTER=CLEAN_J45		SYNC_DATE=04/26/2013	
PAGE TITLE			
NC & No Test			
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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL. OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, P65BGA			MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE_ADJ	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE_ADJ	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM	0.120 MM	0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM	0.120 MM	0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM	0.120 MM	0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.096 MM	0.096 MM	0.126 MM	0.126 MM	0.126 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.096 MM	0.096 MM	0.126 MM	0.126 MM	0.126 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM	0.160 MM	0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM	0.120 MM	0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM	0.120 MM	0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM	0.125 MM	0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM	0.200 MM	0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM	0.200 MM	0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM	0.180 MM	0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal, Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1X_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2, ISL11, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC MASTER=CLEAN J45 SYNC DATE=04/26/2013

PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	20 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?	DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?	DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKL2N2S	*	=6X_DIELECTRIC	?	DMICKL2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKL2S2N	*	=3X_DIELECTRIC	?	DMICKL2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICKL2OTHER	*	=4X_DIELECTRIC	?	DMICKL2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICKL2N2S
CLK_DMI	DMI_S2N	*	DMICKL2S2N
CLK_DMI	*	*	DMICKL2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?	PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?	PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?	PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?	PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3X_DIELECTRIC	?	DP_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DP_2OTHER	*	=4X_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKL_2CLK	*	=7X_DIELECTRIC	?	HDMICKL_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
HDMICKL_2DP	*	=4X_DIELECTRIC	?	HDMICKL_2DP	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKL_2OTHER	*	=7X_DIELECTRIC	?	HDMICKL_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICKL_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICKL_2DP
HDMI_CLK	*	*	HDMICKL_2OTHER

DisplayPort/TMS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54mm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMS TRACKS: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>
DMI_N2S	CPU_85D	DMI_N2S	DMI N2S P<3:0>
DMI_N2S	CPU_85D	DMI_N2S	DMI N2S N<3:0>
FDI_INT	CPU_50S	CPU_AGTL	FDI INT
FDI_CSVMC	CPU_50S	CPU_AGTL	FDI CSVMC
CLK_DMI	CPU_85D	CLK_DMI	DMI CLK100M CPU P
CLK_DMI	CPU_85D	CLK_DMI	DMI CLK100M CPU N
CLK_DMI	CPU_85D	CLK_DMI	CPU CLK135M DPLLREF N
CLK_DMI	CPU_85D	CLK_DMI	CPU CLK135M DPLLREF P
CLK_DMI	CPU_85D	CLK_DMI	CPU CLK135M DPLLSS N
CLK_DMI	CPU_85D	CLK_DMI	CPU CLK135M DPLLSS P
EDP_COMP	CPU_27P4S	CPU_COMP	CPU EDP RCOMP
EDP_COMP	CPU_27P4S	CPU_COMP	CPU PEG RCOMP
CFG	CPU_45S	CPU_ITP	CPU CFG<19..0>
XDP_CLK_BCH	CLK_BCH_85D	CLK_BCH	ITPXDP CLK100M P
XDP_CLK_BCH	CLK_BCH_85D	CLK_BCH	ITPXDP CLK100M N
XDP_TDI	CPU_45S	CPU_ITP	XDP CPU TDI
XDP_TDO	CPU_45S	CPU_ITP	XDP CPU TDO
XDP_TMS	CPU_45S	CPU_ITP	XDP CPU TMS
XDP_TCK	CPU_45S	CPU_ITP	XDP CPU TCK
XDP_TRST_L	CPU_45S	CPU_ITP	XDP CPU TRST L
XDP_BPM	CPU_45S	CPU_ITP	XDP BPM L<3..0>
XDP_BPM	CPU_45S	CPU_ITP	XDP BPM L<7..4>
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP DBRESET L
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP CPU PRDY L
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP CPU PREQ L
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU CATERR L
CPU_PECI	CPU_45S	CPU_VID	CPU Peci
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU PROCHOT L
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU PWRGD
PM_THRMTRIP_L	CPU_45S	CPU_AGTL	PM THRMTRIP L
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM MEM_PWRGD
PM_SYNC	CPU_45S	CPU_AGTL	PM SYNC
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM_RCOMP<2..0>
CPU_VID	CPU_45S	CPU_VID	CPU VIDSOUT
CPU_VID	CPU_45S	CPU_VID	CPU VIDCLK
CPU_VID	CPU_45S	CPU_VID	CPU VIDALERT L
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N
CPU_MEM_VREF	CPU_27P4S	CPU_VREF	CPU DIMM VREFDQ
CPU_MEM_VREF	CPU_27P4S	CPU_VREF	CPU DIMM VREFDQ
CPU_MEM_VREF	CPU_27P4S	CPU_VREF	PPVREF S3 MEM VREFDQ A
CPU_MEM_VREF	CPU_27P4S	CPU_VREF	PPVREF S3 MEM VREFDQ B
CPU_MEM_VREF	CPU_27P4S	CPU_VREF	PPVREF S3 MEM VREFCA A
CPU_MEM_VREF	CPU_27P4S	CPU_VREF	PPVREF S3 MEM VREFCA B
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R P<7..0>
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R N<7..0>
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R C P<7..0>
PEG_D2R	PEG_80D	PEG_D2R	PEG D2R C N<7..0>
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D P<7..0>
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D N<7..0>
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D C P<7..0>
PEG_R2D	PEG_80D	PEG_R2D	PEG R2D C N<7..0>
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIe TBT D2R P<3..0>
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIe TBT D2R N<3..0>
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIe TBT R2D P<3..0>
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIe TBT R2D N<3..0>
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIe TBT R2D C P<3..0>
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIe TBT R2D C N<3..0>

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML C P<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML C N<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML P<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML N<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML F P<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML F N<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML P<3..0>
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP INT ML N<3..0>
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH C P
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH C N
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH P
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP INT AUXCH N
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA IG AUX CH P
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA IG AUX CH N
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB IG AUX CH P
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB IG AUX CH N

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI DATA P<2..0>
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI DATA N<2..0>
HDMI_CLK	DP_85D	HDMI_CLK	HDMI CLK P
HDMI_CLK	DP_85D	HDMI_CLK	HDMI CLK N
DP_TBT_ML_0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>
DP_TBT_ML_0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>
DP_TBT_ML_0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>
DP_TBT_ML_0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>
DP_TBT_ML_1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>
DP_TBT_ML_1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>
DP_TBT_ML_1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>
DP_TBT_ML_1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH P
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH N
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C P
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK0 AUXCH C N
TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH P
TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH N
TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C P
TBTSNK1_AUXCH	DP_85D	DISPLAYPORT	DP TBTSNK1 AUXCH C N

CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=6X_DIELECTRIC	?	SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?	SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?	USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
WT_WAKE	*	=4X_DIELECTRIC	?	WT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4X_DIELECTRIC	?
CLK_25M	*	=5X_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
NC SATA A R2D CP	SATA_85D	SATA_R2D	SATA_85D
NC SATA A R2D CN	SATA_85D	SATA_R2D	SATA_85D
NC SATA A D2RP	SATA_85D	SATA_D2R	SATA_85D
NC SATA A D2RN	SATA_85D	SATA_D2R	SATA_85D
NC SATA B R2D CP	SATA_85D	SATA_R2D	SATA_85D
NC SATA B R2D CN	SATA_85D	SATA_R2D	SATA_85D
NC SATA B D2RP	SATA_85D	SATA_D2R	SATA_85D
NC SATA B D2RN	SATA_85D	SATA_D2R	SATA_85D
PCH SATA RCOMP	SATA_45SE	SATA_RCOMP	SATA_45SE
USB EXTA P	USB_85D	USB	USB_85D
USB EXTA N	USB_85D	USB	USB_85D
USB EXTA MIXED P	USB_85D	USB	USB_85D
USB EXTA MIXED N	USB_85D	USB	USB_85D
USB LT1 P	USB_85D	USB	USB_85D
USB LT1 N	USB_85D	USB	USB_85D
NC USB EXTCP	USB_85D	USB	USB_85D
NC USB EXTCN	USB_85D	USB	USB_85D
NC USB SDP	USB_85D	USB	USB_85D
NC USB SDN	USB_85D	USB	USB_85D
SMC DEBUGPRT RX L	CPU_45S	CPU_ITP	CPU_45S
SMC DEBUGPRT TX L	CPU_45S	CPU_ITP	CPU_45S
USB SMC P	USB_85D	USB	USB_85D
USB SMC N	USB_85D	USB	USB_85D
NC USB 6P	USB_85D	USB	USB_85D
NC USB 6N	USB_85D	USB	USB_85D
NC USB 7P	USB_85D	USB	USB_85D
NC USB 7N	USB_85D	USB	USB_85D
USB EXTB P	USB_85D	USB	USB_85D
USB EXTB N	USB_85D	USB	USB_85D
NC USB EXTDP	USB_85D	USB	USB_85D
NC USB EXTDN	USB_85D	USB	USB_85D
USB BT P	USB_85D	USB	USB_85D
USB BT N	USB_85D	USB	USB_85D
USB BT CONN P	USB_85D	USB	USB_85D
USB BT CONN N	USB_85D	USB	USB_85D
NC USB IRP	USB_85D	USB	USB_85D
NC USB IRN	USB_85D	USB	USB_85D
USB TPAD P	USB_85D	USB	USB_85D
USB TPAD N	USB_85D	USB	USB_85D
USB TPAD R P	USB_85D	USB	USB_85D
USB TPAD R N	USB_85D	USB	USB_85D
PCH USB RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS
USB3 EXTA D2R P	USB_85D	USB3_D2R	USB_85D
USB3 EXTA D2R N	USB_85D	USB3_D2R	USB_85D
USB3 EXTA D2R C P	USB_85D	USB3_D2R	USB_85D
USB3 EXTA D2R C N	USB_85D	USB3_D2R	USB_85D
USB3 EXTA R2D P	USB_85D	USB3_R2D	USB_85D
USB3 EXTA R2D N	USB_85D	USB3_R2D	USB_85D
USB3 EXTA R2D C P	USB_85D	USB3_R2D	USB_85D
USB3 EXTA R2D C N	USB_85D	USB3_R2D	USB_85D
USB3 EXTB D2R P	USB_85D	USB3_D2R	USB_85D
USB3 EXTB D2R N	USB_85D	USB3_D2R	USB_85D
USB3 EXTB D2R C P	USB_85D	USB3_D2R	USB_85D
USB3 EXTB D2R C N	USB_85D	USB3_D2R	USB_85D
USB3 EXTB R2D P	USB_85D	USB3_R2D	USB_85D
USB3 EXTB R2D N	USB_85D	USB3_R2D	USB_85D
USB3 EXTB R2D C P	USB_85D	USB3_R2D	USB_85D
USB3 EXTB R2D C N	USB_85D	USB3_R2D	USB_85D
NC USB3 EXTC D2RP	USB_85D	USB3_D2R	USB_85D
NC USB3 EXTC D2RN	USB_85D	USB3_D2R	USB_85D
NC USB3 EXTC R2D CP	USB_85D	USB3_R2D	USB_85D
NC USB3 EXTC R2D CN	USB_85D	USB3_R2D	USB_85D
NC USB3 EXT D2RP	USB_85D	USB3_D2R	USB_85D
NC USB3 EXT D2RN	USB_85D	USB3_D2R	USB_85D
NC USB3 EXT R2D CP	USB_85D	USB3_R2D	USB_85D
NC USB3 EXT R2D CN	USB_85D	USB3_R2D	USB_85D
SYSCLK CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	CLK_SLOW_45S
SYSCLK CLK25M_SB	CLK_25M_45S	CLK_25M	CLK_25M_45S
SYSCLK CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK_25M_45S
SYSCLK CLK25M_TBT	CLK_25M_45S	CLK_25M	CLK_25M_45S

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
SYSCLK CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	CLK_SLOW_45S
SYSCLK CLK25M_SB	CLK_25M_45S	CLK_25M	CLK_25M_45S
SYSCLK CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK_25M_45S
SYSCLK CLK25M_TBT	CLK_25M_45S	CLK_25M	CLK_25M_45S

SYNC MASTER=CLEAN_J45 SYNC DATE=04/26/2013

PCH Constraints 1

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LPC Bus Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include LPC_45S and CLK_LPC_45S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include LPC and CLK_LPC.

SMBus Interface Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes SMB_45S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes SMB.

HD Audio Interface Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes HDA_45S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes HDA.

SPI Interface Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes SPI_45S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes SPI.

PCH Single Net Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes PCH_45S.

Table with 8 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include PCH_SE and PCH_SE with TOP,BOTTOM layer.

PCI-Express

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include PCIE_85D and CLK_PCIE_85D.

Table with 8 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include PCIE_2SAME, PCIE_TXRX, PCIE_2OTHER, PCIE_2CLK, and PCIECLK_2OTHER.

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include PCIE_*, PCIE_R2D, PCIE_*, PCIE_*, and CLK_PCIE.

PCH Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, NET_TYPE. Lists various net types like LPC_AD, SMBUS_PCH_CLK, HDA_BIT_CLK, SPI_CLK, USB3_SD_R2D, PCIE_CAMERA_R2D, and PCIE_CLK100M.

PCH Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, NET_TYPE. Lists various net types like PCH_PM_NET, PCIE_D2R_SSD, and PCIE_CAMERA_R2D.

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Memory Bus Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW_ROUTE_ON_LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include MEM_37S, MEM_40S, MEM_72D, MEM_45S, MEM_85D.

Spacing Rule Sets

Two tables side-by-side. Left table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Right table: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include MEM_DATA2SELF, MEM_DQS2OWNDATA, MEM_CMD2CMD, MEM_CTRL2CTRL, MEM_CLK2CLK, MEM_2OTHERMEM, MEM_2PWR, MEM_2GND, MEM_2OTHER.

Memory Bus Spacing Group Assignments

Two tables side-by-side. Left table: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Right table: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_*_DATA_*, MEM_*_DQS_*, MEM_CMD, MEM_CTRL, MEM_CLK, MEM_*.

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair. DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement. DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm]. CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm. CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs. A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs. DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric. Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max. SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_PWR, MEM_*, MEM_PWR.

Memory to GND Spacing

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include GND, MEM_*.

Memory Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Rows include MEM_A_CLK0, MEM_A_CMD, MEM_A_DATA_0, MEM_A_DQS_0, MEM_B_CLK0, MEM_B_CMD, MEM_B_DATA_0, MEM_B_DQS_0, MEM_PWR.

Metadata box containing: SYNC MASTER=CLEAN J45, SYNC DATE=04/26/2013, Apple Inc., Drawing Number: 051-0675, Revision: 6.0.0, Page: 114 OF 119, Sheet: 89 OF 94.

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3x_DIELECTRIC	?
TBTDP_TXRX	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C P<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D C N<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D P<1..0>
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT A R2D N<1..0>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML P<1>
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML N<1>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<3>
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<3>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<0>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<0>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R P<0>
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT A D2R N<0>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C P<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R C N<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R P<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R N<1>
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC P
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT A D2R1 AUXDDC N
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C P
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH C N
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH P
TBT_A_AUXCH	DP_85D		DP TBTPA AUXCH N
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C P<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D C N<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D P<1..0>
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT B R2D N<1..0>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML P<1>
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML N<1>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<3>
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<3>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<0>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<0>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R P<0>
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT B D2R N<0>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C P<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R C N<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R P<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R N<1>
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC P
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT B D2R1 AUXDDC N
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH C P
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH C N
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH P
TBT_B_AUXCH	DP_85D		DP TBTPB AUXCH N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
DP_85D	DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P
DP_85D	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT SPI CLK
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT SPI MISO
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT SPI CS L

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=CLEAN J45		SYNC DATE=04/26/2013	
Thunderbolt Constraints			
Apple Inc.		DRAWING NUMBER	051-0675
		REVISION	6.0.0
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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?	MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?	MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?	MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?	S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?	S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?	S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?	S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?	S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?	S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?	S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?	S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?	S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK P
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK N
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CKE
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CS L
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM CAM ODT
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CAS L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM RAS L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM WE L
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<0>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<1>
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<2>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS P<0>
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS N<0>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS P<1>
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS N<1>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DM<0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DM<1>
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM CAM A<14..0>
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DO<7..0>
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DO<15..8>
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA N
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN P
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK N
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN P
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN N
		S2_MEM_PWR	P1V35 CAM
		S2_MEM_PWR	P0V675 CAM VREF
		S2_MEM_PWR	P0V675 MEM CAM VREFCA
		S2_MEM_PWR	P0V675 MEM CAM VREFDO

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

Camera Constraints

Apple Inc.

DRAWING NUMBER: 051-0675

REVISION: 6.0.0

BRANCH: dvt

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	40 43 83
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	40 43 83
SMBUS_SMC_3_SCL	SMB_45S	SMB	SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_45S	SMB	SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1T01_DIEPPAIR		CHGR_CSI_P	56
	1T01_DIEPPAIR		CHGR_CSI_N	56
CHGR_CSO	1T01_DIEPPAIR		CHGR_CSO_P	56
	1T01_DIEPPAIR		CHGR_CSO_N	56

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SYNC_MASTER=CLEAN_J45		SYNC_DATE=04/26/2013	
PAGE TITLE SMC Constraints			
Apple Inc.	DRAWING NUMBER	051-0675	SIZE D
	REVISION	6.0.0	
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PHYSICAL_RULE_SET table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP

SPACING_RULE_SET table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT

SPACING_RULE_SET table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT

SPACING_RULE_SET table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT

NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET table

NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET table

PHYSICAL_RULE_SET table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP

NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET table

J15 Specific Net Properties

J15 Specific Net Properties table with columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING, and various net names like SENSE_DIEFFAIR, THERM_1T01_45S, etc.

J15 Specific Net Properties

J15 Specific Net Properties table with columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING, and various net names like AUDIO_DIEFFAIR, THERM_1T01_45S, etc.

Project Specific Constraints metadata including Apple Inc. logo, drawing number 051-0675, revision 6.0.0, and page 118 of 119.

GDDR5 Frame Buffer Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include GDDR5_45R50SE, GDDR5_45SE, and GDDR5_80D.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include GDDR5_CLK, GDDR5_CMD, GDDR5_DATA, and GDDR5_EDC.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include GDDR5_CLK, GDDR5_CMD, GDDR5_DATA, and GDDR5_EDC.

GDDR5 FB A Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, NET_TYPE. Lists various signal constraints for FB A, such as FB A0_CLK, FB A1_CMD, FB A0_CMD_R, etc.

GDDR5 FB B Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, NET_TYPE. Lists various signal constraints for FB B, such as FB B0_CLK, FB B1_CMD, FB B0_CMD_R, etc.

MUXGFX & DP AUX MUX NET PROPERTIES

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, NET_TYPE. Lists constraints for DP and TBT signals, such as DP_INT_ML_C, DP_INT_ML_F, DP_INT_ML_P, etc.

Kepler Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING, NET_TYPE. Lists constraints for GPU and HDMI signals, such as GPU_CLK27M, HDMI_DATA, HDMI_CLK, etc.

GPU (Kepler) Constraints metadata box containing Apple Inc. logo, drawing number 051-0675, revision 6.0.0, and a notice of proprietary property.