1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,X425

08/06/2014 PROTO1A

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00330	1	SCHEM MLB X305	SCH	CRITICAL	
820-00138	1	PCBF MLB X305	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST MODIFIED=Wed Aug 6 13 00 04 2014

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00039	COMMON PARTS,MLB,X425	X425_COMMON
985-00043	DEV,MLB,X425	X425_DEVEL:ENG
639-00534	PCBA,MLB,CTO,16G-HYN,X425	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1866
639-00535	PCBA,MLB,CTO,16G-MIC,X425	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1866

X425 BOM Groups

BOM GROUP	BOM OPTIONS
X425_COMMON	ALTERNATE,COMMON,X425_COMMON1,X425_COMMON2,X425_PROGPARTS
X425_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CPUPEG:X8X8,S2_PWR:S0,SMC_SUSACK:YES
X425_COMMON2	EDP:YES,XDP,SSD_PWR_EN:GPIO,CAM_WAKE:NO,SAMCONN,APCLKRQ:ISOL,DDRREG_PGD:N,CRW_SPRT,WLAN_SW:SIL
X425_PVT	BKLT:PROD,SENSOR_NONPROD:N
X425_PROGPARTS	SMC_PROG:BASE,BOOTROM_PROG:PROTO1A,TBTROM:PROG
X425_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,X249:BOOST
X425_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
X425_DEVEL:PVT	XDP_DEBUG
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00057	1	CRW SR1ZW PRQ C0 2 2 47W 4+3E 1 2 6M BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S00058	1	CRW SR1ZX PRQ C0 2 5 47W 4+3E 1 2 6M BGA	U0500	CRITICAL	CPU_CRW:BEST
337S00059	1	CRW SR1ZY PRQ C0 2 8 47W 4+3E 1 2 6M BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC QEWV LPT M HM87 C2 SR199 PRQ FCBGA	U1100	CRITICAL	
338S1247	1	IC TBT FR 4C A0 PRQ CIO SR1JC FCBGA288	U2800	CRITICAL	
338S1264	1	IC BCM15700A2 S2 PCIE CMRA 8X8 208FCBGA	U3900	CRITICAL	
333S0700	1	IC SDRAM 4GBIT DDR3L 1600 GEMMA 96B FBGA	U4000	CRITICAL	
333S0802	16	IC SDRAM 25NM 512MX8 DDR3L 1866 78B FBGA		CRITICAL	HYNIX_1866_S
333S0719	16	IC SDRAM 4GBIT DDR3 1866 V80A 78B FBGA		CRITICAL	MICRON_1866_S
333S0802	32	IC SDRAM 25NM 512MX8 DDR3L 1866 78B FBGA		CRITICAL	HYNIX_1866
333S0719	32	IC SDRAM 4GBIT DDR3 1866 V80A 78B FBGA		CRITICAL	MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1866_S	HYNIX_1866_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1866_S	MICRON_1866_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:HYNIX_1866	HYNIX_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1866	MICRON_1866,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00039	1	COMMON PARTS MLB X425	BASE	CRITICAL	BASE_BOM
985-00043	1	DEV MLB X425	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=CLEAN X305 SYNC DATE=05/30/2014

PAGE TITLE
BOM Configuration

Apple Inc.

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S00133	1	T29,FALCON RIDGE(VXXXX)PROTO 1A,X425	U2890	CRITICAL	TBTROM:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BLANK
341S00125	1	IC,SMC-B1,EXT (V2.24A31) PROTO 1A,X425	U5000	CRITICAL	SMC_PROG:BASE

EFI ROM

335S00007	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:WIN
335S00006	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:MAC
341S00131	1	IC,EFI ROM (VXXXX) PROTO 1A,X425	U6100	CRITICAL	BOOTROM_PROG:PROTO1A

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S00008		ALL	Panasonic alt to TDK
376S1217	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
128S0371	128S0376		ALL	Kemet alt to Sanyo
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX
311S0649	311S0541		ALL	ON alt to Toshiba
376S00014	376S0761		ALL	Toshiba alt to Vishay
740S00003	740S0135		ALL	AEM alt to Tyco
377S0155	377S00011		ALL	On Semi alt to Infineon
377S0184	377S00011		ALL	Infineon alt to Infineon

SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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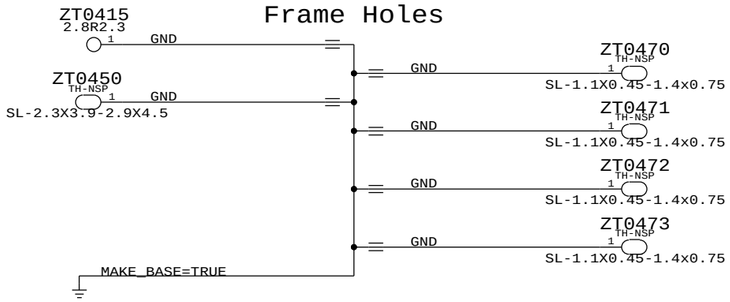
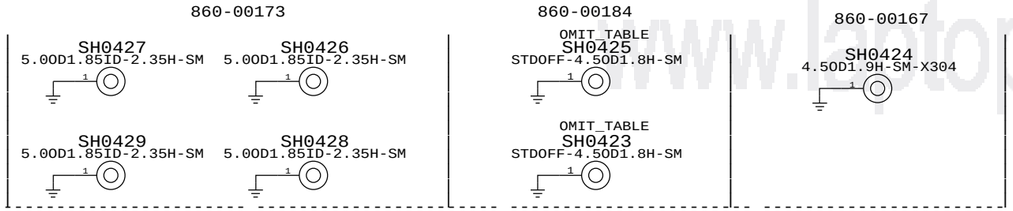
Frame Holes

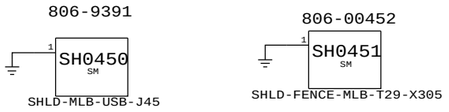


X425 THERMAL MODULE STANDOFF

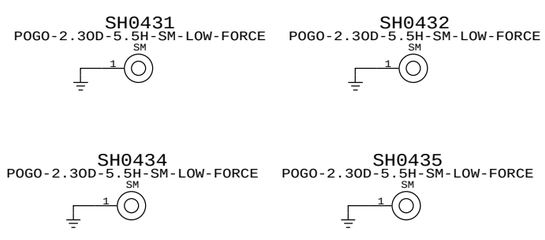


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-00184	2	STANDOFF,THERMAL/FAN,W/O MYLAR,X305	SH0423,SH0425	CRITICAL	

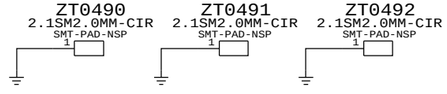
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	



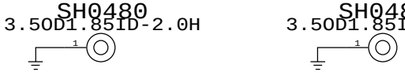
X425 POGO PINS



SMT GND TEST PONTS

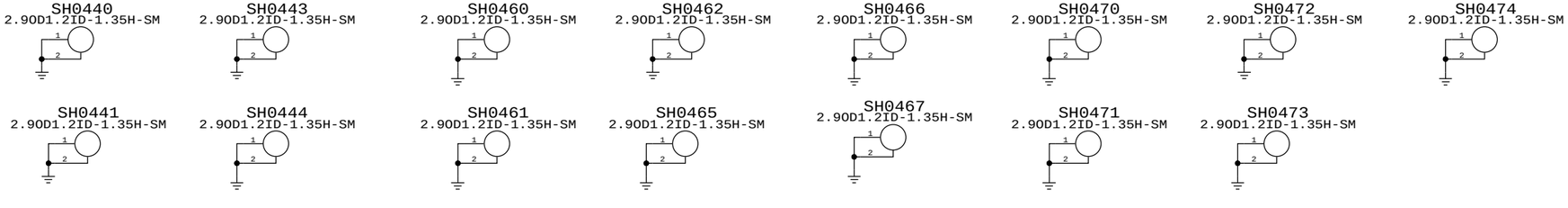


RIO FLEX BRACKET BOSS (860-00166)



X425 StAND OFF

860-1448



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: PD Parts

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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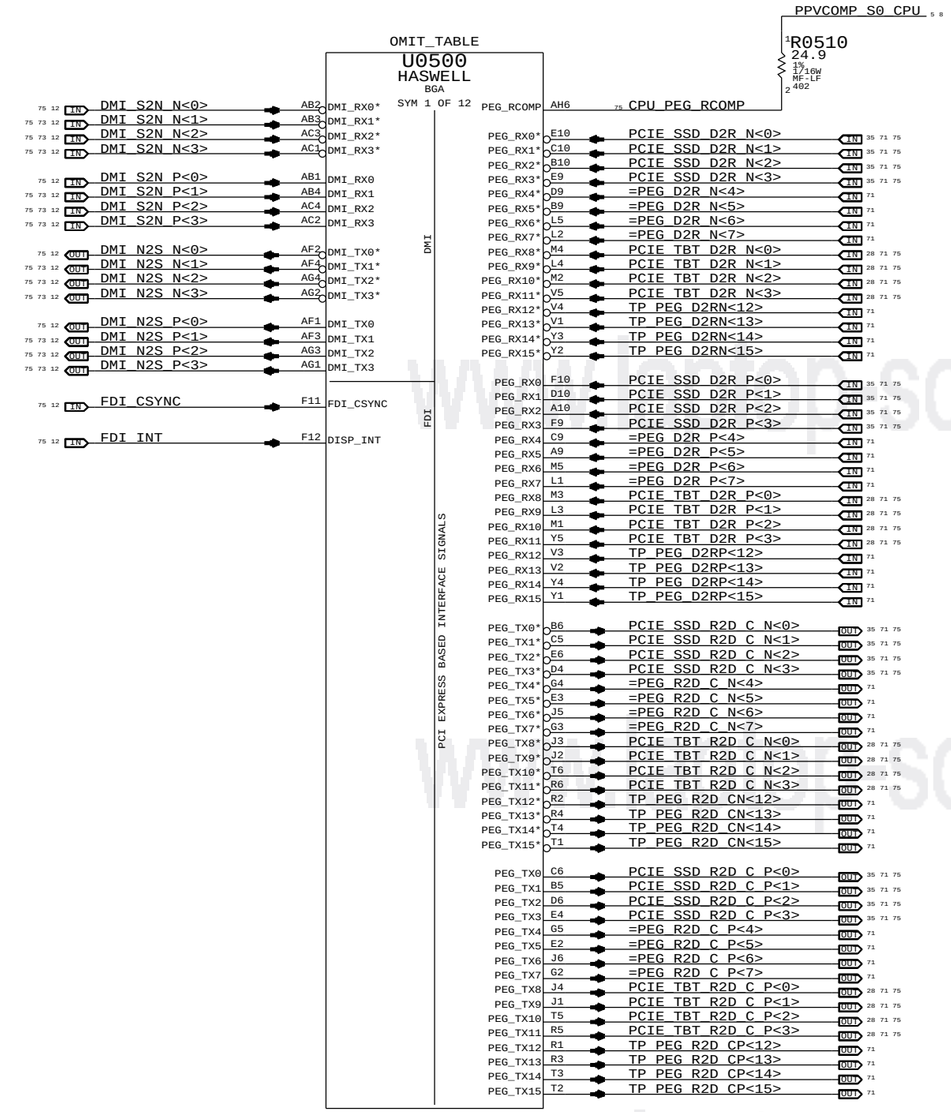

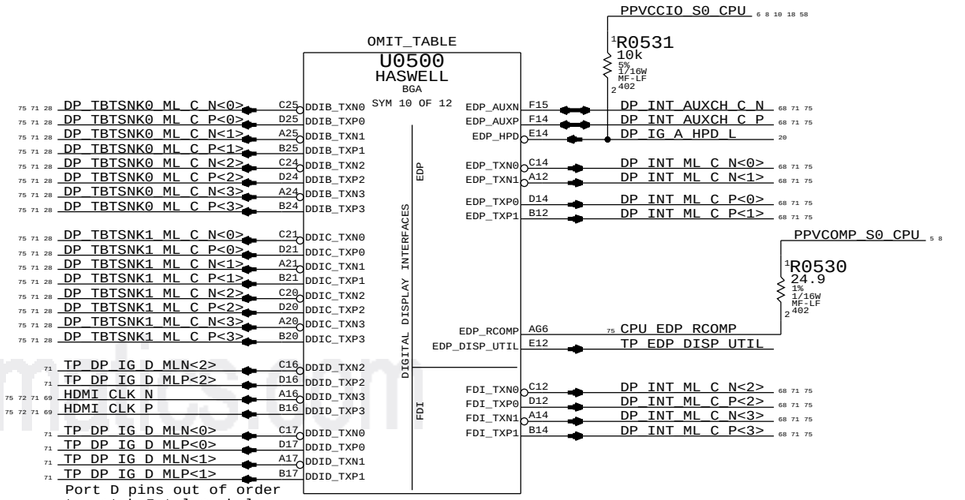

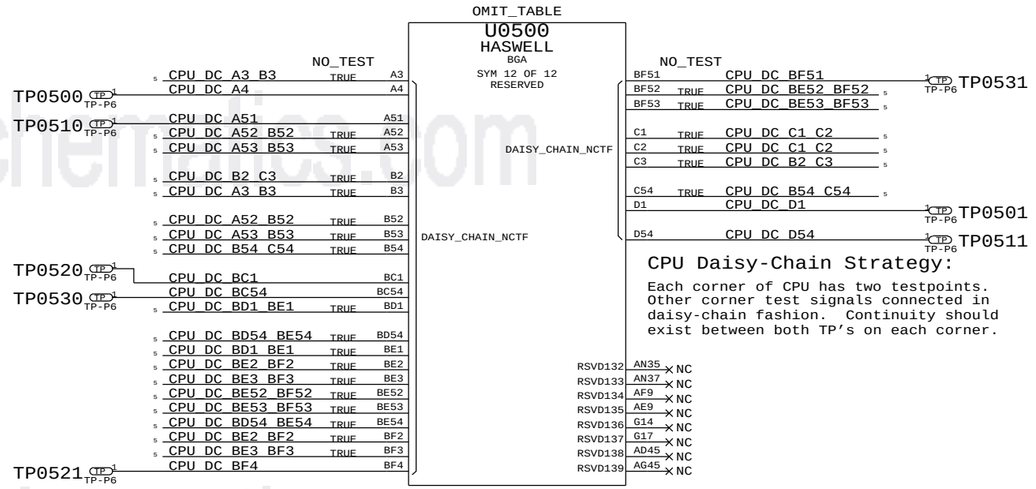

SYNC_MASTER=CLEAN X305 PEG SYNC_DATE=02/18/2014

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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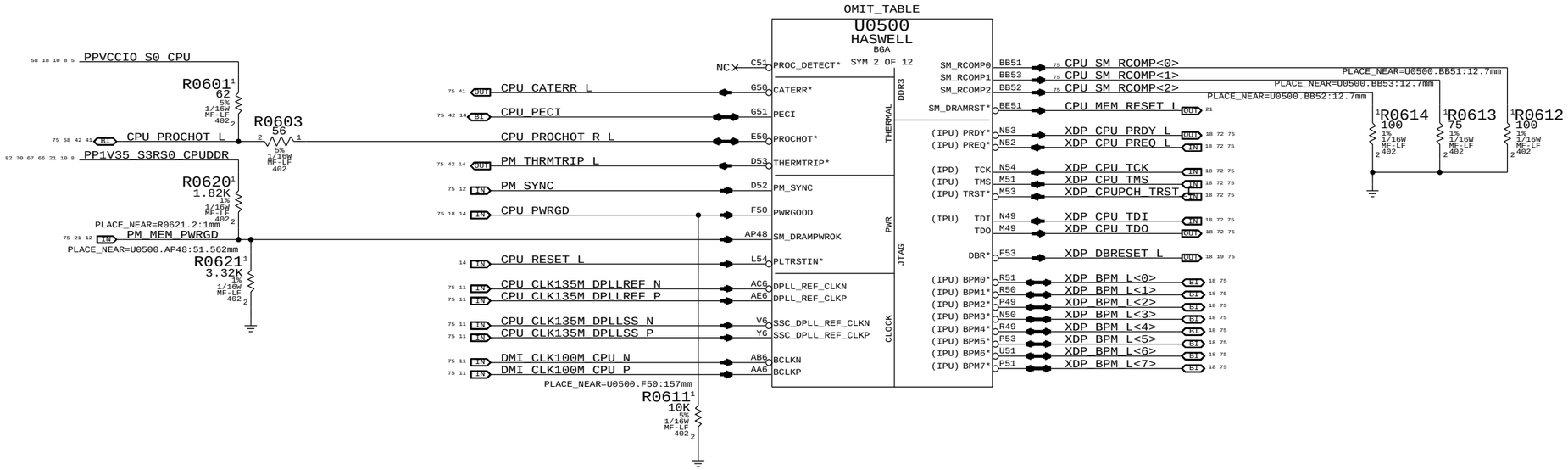
OMIT_TABLE
U0500
HASWELL
BGA
SYM 2 OF 12
PPVCCIO_S0_CPU
R0601 62 5% 1/16W MF-LF 402
R0603 56 5% 1/16W MF-LF 402
CPU_PROCHOT_L
CPU_PROCHOT_R_L
PP1V35_S3RS0_CPUDDR
R0620 1.82K 1% 1/16W MF-LF 402
PLACE_NEAR=R0621.2:1mm
PM_MEM_PWRGD
PLACE_NEAR=U0500.AP48:51.562mm
R0621 3.32K 1% 1/16W MF-LF 402
NC
PROC_DETECT*
CPU_CATERR_L
CATERR*
CPU_PECI
PECI
PROCHOT*
PM_THRMTRIP_L
THERMTRIP*
PM_SYNC
PWRGOOD
SM_DRAMPWROK
CPU_RESET_L
PLTRSTIN*
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
DPLL_REF_CLKN
DPLL_REF_CLKP
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
SSC_DPLL_REF_CLKN
SSC_DPLL_REF_CLKP
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
BCLKN
BCLKP
PLACE_NEAR=U0500.F50:157mm
R0611 10K 5% 1/16W MF-LF 402
THERMAL
DDR3
PWR
JTAG
CLOCK
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
CPU_SM_RCOMP<0>
CPU_SM_RCOMP<1>
CPU_SM_RCOMP<2>
PLACE_NEAR=U0500.BB51:12.7mm
PLACE_NEAR=U0500.BB53:12.7mm
PLACE_NEAR=U0500.BB52:12.7mm
R0614 100 1% 1/16W MF-LF 402
R0613 75 1% 1/16W MF-LF 402
R0612 100 1% 1/16W MF-LF 402
SM_DRAMRST*
CPU_MEM_RESET_L
(IPU) PRDY*
(IPU) PREQ*
XDP_CPU_PRDY_L
XDP_CPU_PREQ_L
(IPD) TCK
(IPU) TMS
(IPU) TRST*
XDP_CPU_TCK
XDP_CPU_TMS
XDP_CPUPCH_TRST_L
(IPU) TDI
TDO
XDP_CPU_TDI
XDP_CPU_TDO
DBR*
XDP_DBRESET_L
(IPU) BPM0*
(IPU) BPM1*
(IPU) BPM2*
(IPU) BPM3*
(IPU) BPM4*
(IPU) BPM5*
(IPU) BPM6*
(IPU) BPM7*
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>
OMIT_TABLE
U0500
HASWELL
BGA
SYM 11 OF 12
RESERVED
TP_CPU_RSVD_TP23
TP_CPU_RSVD_TP24
TP_CPU_RSVD_TP25
TP_CPU_RSVD_TP26
TP_CPU_RSVD_TP27
TP_CPU_RSVD_TP28
CPU_TESTLO_F21
R0680 49.9 1% 1/16W MF-LF 402
PPVCC_S0_CPU
TP_CPU_RSVD_TP35
TP_CPU_RSVD_TP36
TP_CPU_RSVD_TP37
TP_CPU_RSVD_TP38
TP_CPU_RSVD_TP39
CPU_TESTLO_F20
R0685 49.9 1% 1/16W MF-LF 402
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
NC
RSVD50
RSVD51
RSVD52
RSVD_TP1
RSVD_TP2
RSVD_TP3
RSVD_TP4
TP_CPU_RSVD_TP1
TP_CPU_RSVD_TP2
TP_CPU_RSVD_TP3
TP_CPU_RSVD_TP4
CFG_RCOMP
CPU_CFG_RCOMP
(IPU) CFG16
CFG18
(IPU) CFG17
CFG19
CPU_CFG<16>
CPU_CFG<18>
CPU_CFG<17>
CPU_CFG<19>
R0690 49.9 1% 1/16W MF-LF 402
RSVD92
RSVD93
RSVD94
RSVD95
RSVD9
RSVD10
RSVD11
RSVD41
RSVD42
RSVD16
RSVD_TP17
RSVD_TP18
TP_CPU_RSVD_TP17
TP_CPU_RSVD_TP18
VSS_H54
VSS_H53
VSS_H51
VSS_H52
RSVD47
RSVD48
RSVD49
TP_CPU_RSVD_TP47
TP_CPU_RSVD_TP48
TP_CPU_RSVD_TP49
CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
These can be placed close to
J1800 and only for debug access
NOSTUFF R0649 1K
NOSTUFF R0648 1K
R0643 1K
NOSTUFF R0641 1K
NOSTUFF R0640 1K
CPUCFG6_PD R0646 1K
CPUCFG5_PD R0645 1K
EDP:YES R0644 1K
NOSTUFF R0647 1K
NOSTUFF R0642 1K
BOM GROUP
BOM OPTIONS
CPUPEG:X8X8
CPUCFG5_PD
CPUPEG:X8X4X4
CPUCFG6_PD,CPUCFG5_PD
To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.
SYNC_MASTER=J15 REFERENCE
SYNC_DATE=12/18/2012
PAGE TITLE
CPU Clock/Misc/JTAG/CFG
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 6 OF 82
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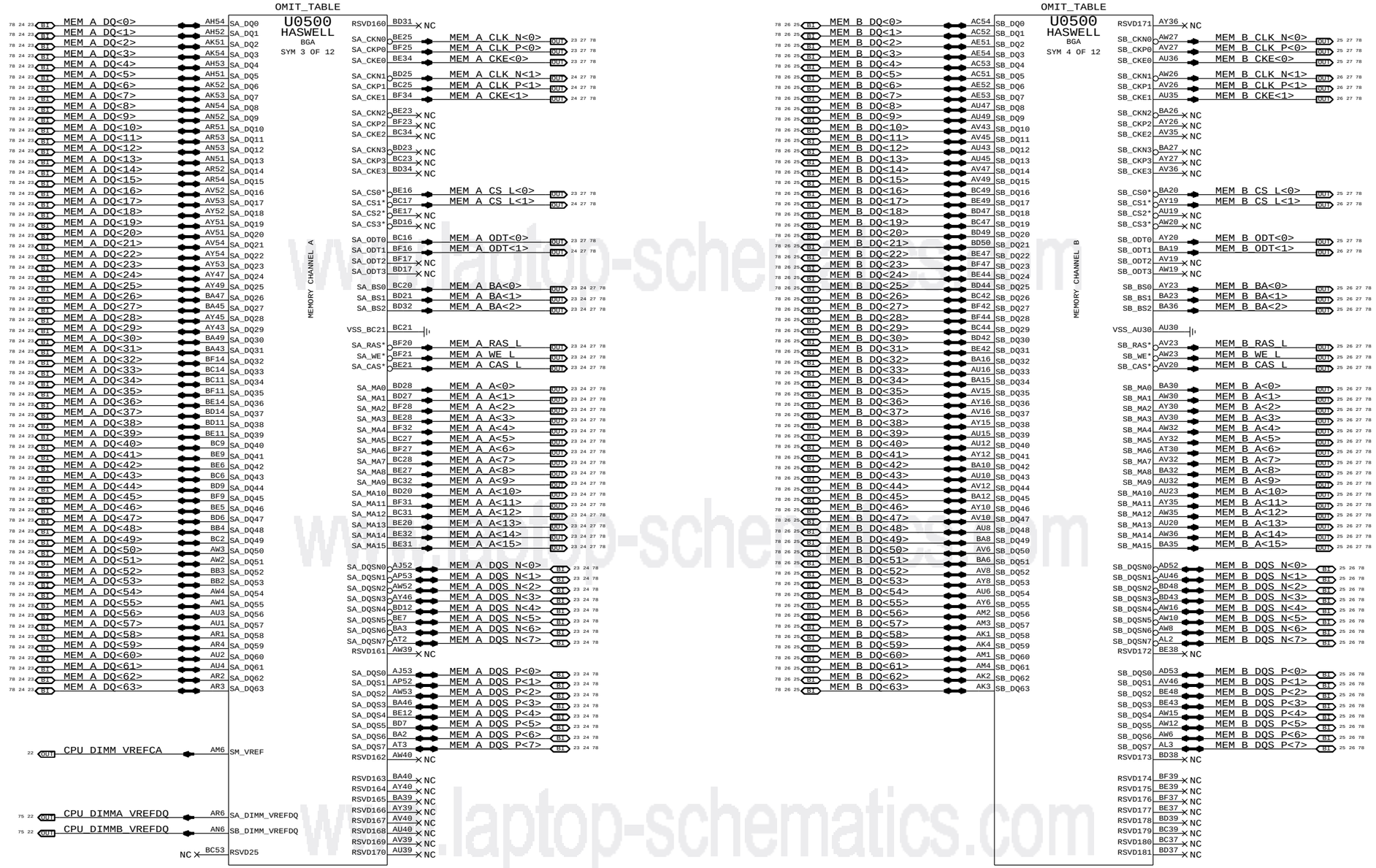

SYNC_MASTER=J15 REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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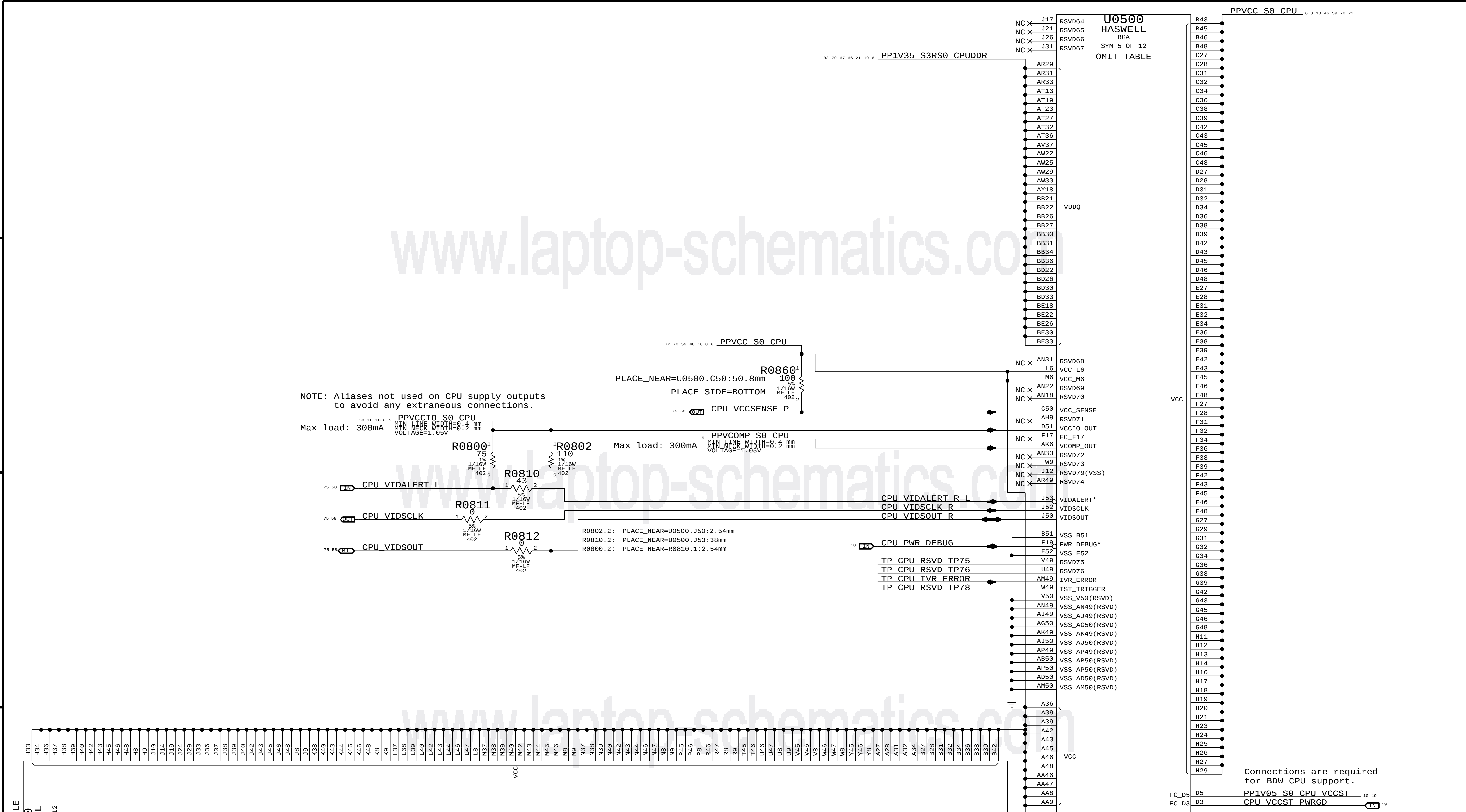

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PAGE TITLE

CPU Power

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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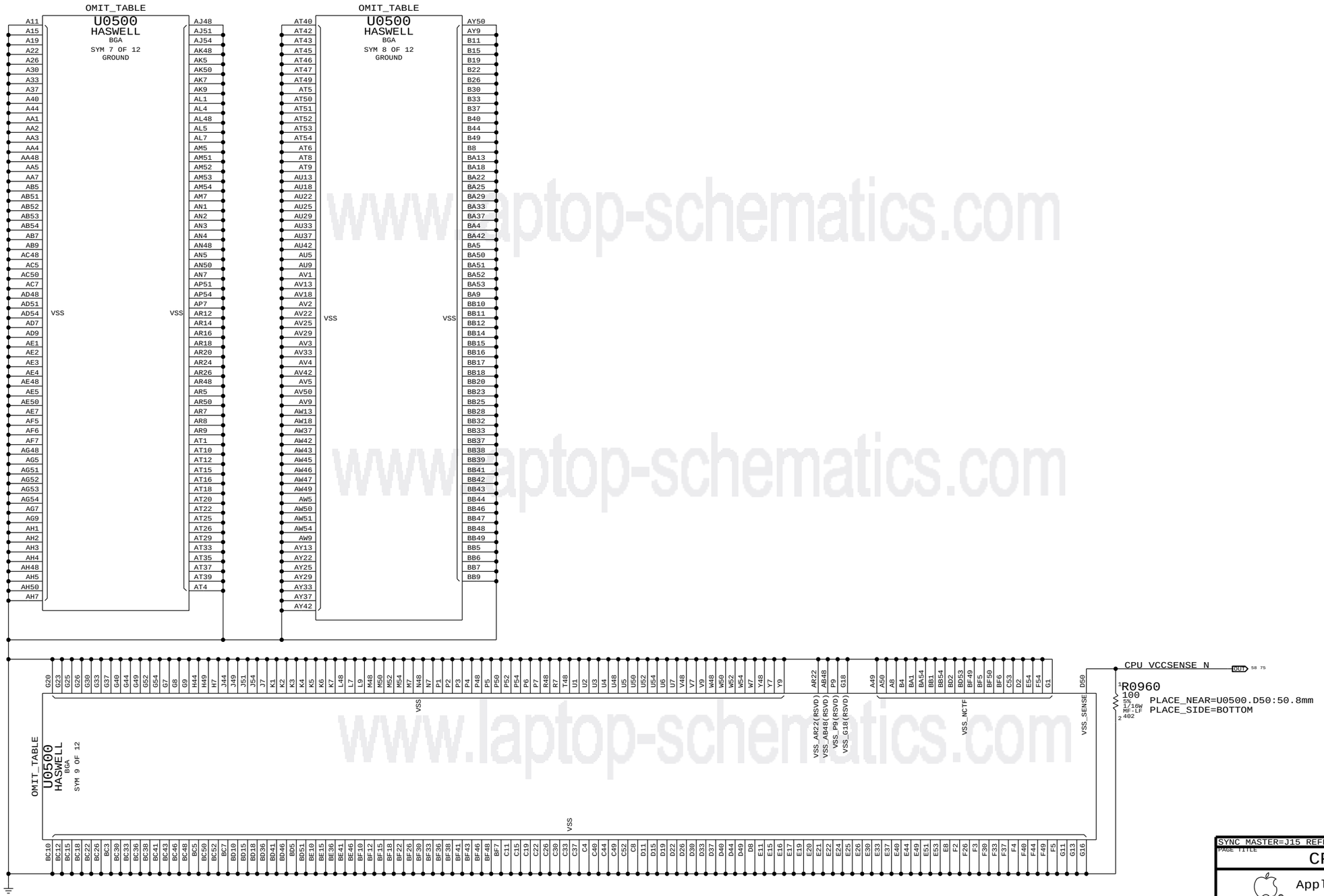

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Ground

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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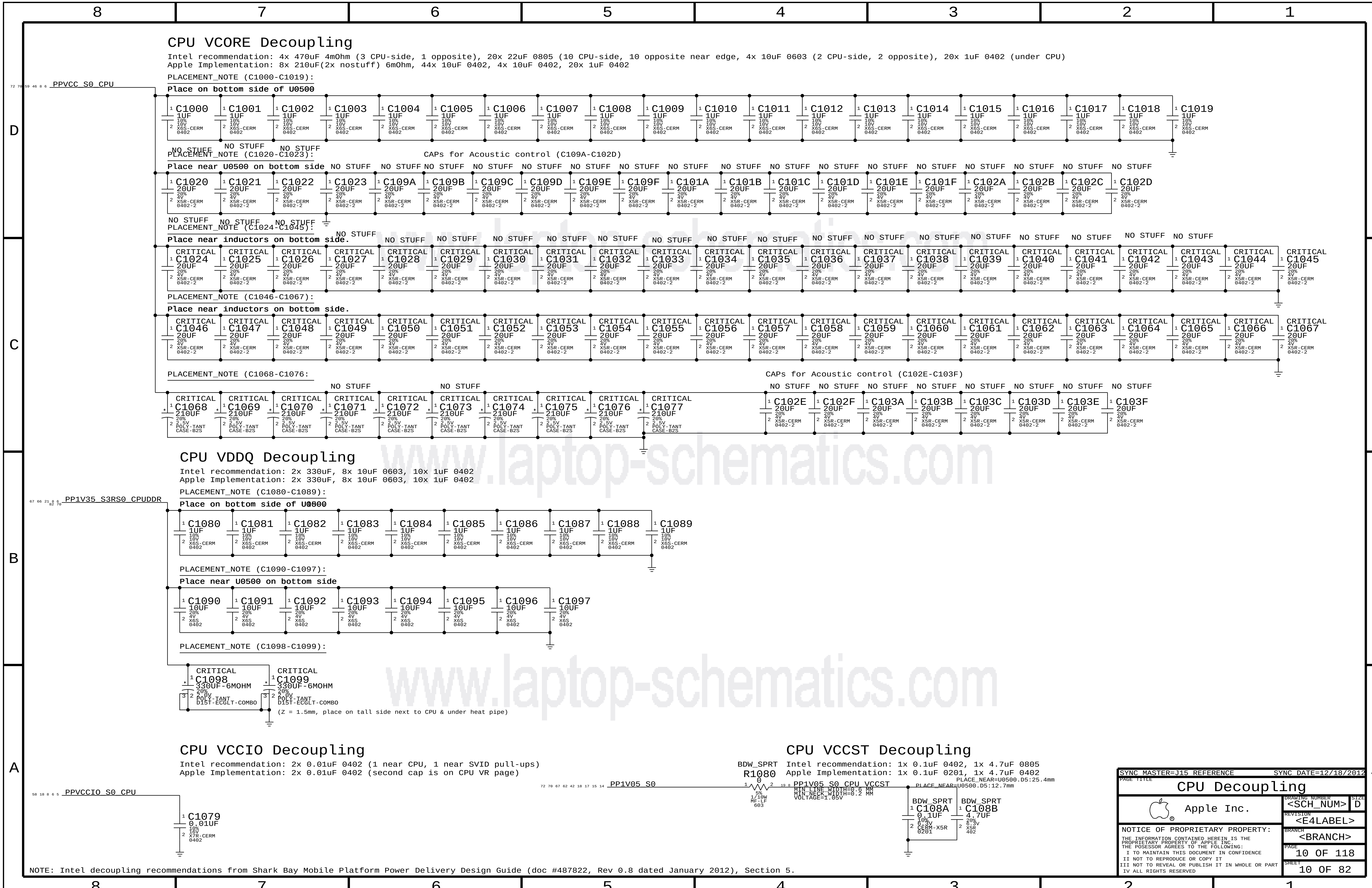

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(1 OF 11)

SYSCLK_CLK32K_RTC — RTCX1 B5; RTCX2 B4 NC
PCH_SRTCRST_L — SRTCRST* B9
PCH_INTRUDER_L — INTRUDER* A8
PCH_INTVRMEN_L — INTVRMEN G10
RTC_RESET_L — RTCRST* D9

HDA_BIT_CLK — R1110 33 — HDA_BIT_CLK_R — HDA_BCLK B25
HDA_SYNC — R1111 33 — HDA_SYNC_R — HDA_SYNC A22 (IPD-boot)
PCH_SPKR — SPKR AL10 (IPD-PLTRST#)
HDA_RST_L — R1112 33 — HDA_RST_R_L — HDA_RST* C24
HDA_SDIN0 — HDA_SDI0 L22 (IPD)
NC_HDA_SDIN1 — HDA_SDI1 K22 (IPD)
NC_HDA_SDIN2 — HDA_SDI2 G22 (IPD)
NC_HDA_SDIN3 — HDA_SDI3 F22 (IPD)
HDA_SDOUT — R1113 33 — HDA_SDOUT_R — HDA_SDO A24 (IPD-boot)
DP_TBT_SEL — (IPD-DOCKEN#?) B17
ENET_MEDIA_SENSE_RDIV — DOCKEN*/GPIO33 C22 — HDA_DOCK_RST*/GPIO13

XDP_PCH_TCK — JTAG_TCK AB3 (IPD)
XDP_PCH_TMS — JTAG_TMS AD1 (IPU)
XDP_PCH_TDI — JTAG_TDI AE2 (IPU)
XDP_PCH_TDO — JTAG_TDO AD3
TP25 F8; TP22 C26; TP20 AB6 NC

RTC / AZALIA / JTAG

SATA_RXN0 BC8 — NC_SATA_A_D2RN
SATA_RXP0 BE8 — NC_SATA_A_D2RP
SATA_TXN0 AW8 — NC_SATA_A_R2D_CN
SATA_TXP0 AY8 — NC_SATA_A_R2D_CP
SATA_RXN1 BC10 — NC_SATA_B_D2RN
SATA_RXP1 BE10 — NC_SATA_B_D2RP
SATA_TXN1 AV10 — NC_SATA_B_R2D_CN
SATA_TXP1 AW10 — NC_SATA_B_R2D_CP
SATA_RXN2 BB9 — NC_SATA_ODD_D2RN
SATA_RXP2 BD9 — NC_SATA_ODD_D2RP
SATA_TXN2 AY13 — NC_SATA_ODD_R2D_CN
SATA_TXP2 AW13 — NC_SATA_ODD_R2D_CP
SATA_RXN3 BC12 — NC_SATA_D_D2RN
SATA_RXP3 BE12 — NC_SATA_D_D2RP
SATA_TXN3 AR13 — NC_SATA_D_R2D_CN
SATA_TXP3 AT13 — NC_SATA_D_R2D_CP
SATA_RXN4/PERN1 BD13 — TP_PCIE_ENET_D2RN
SATA_RXP4/PERP1 BB13 — TP_PCIE_ENET_D2RP
SATA_TXN4/PETN1 AV15 — TP_PCIE_ENET_R2D_CN
SATA_TXP4/PETP1 AW15 — TP_PCIE_ENET_R2D_CP
SATA_RXN5/PERN2 BC14 — NC_SATA_F_D2RN
SATA_RXP5/PERP2 BE14 — NC_SATA_F_D2RP
SATA_TXN5/PETN2 AP15 — NC_SATA_F_R2D_CN
SATA_TXP5/PETP2 AR15 — NC_SATA_F_R2D_CP
SATA_RCOMP AY5 — PCH_SATA_RCOMP
SATALED* AP3 — PCH_SATALED_L
SATA0GP/GPIO21 AT1 — XDP_DC0_DP_AUXCH_ISOL_L
SATA1GP/GPIO19 (IPU-PLTRST#) AU2 — XDP_DC1_SATARDRVR_EN
SATA_IREF BD4

SATA Port assignments:

Primary HDD/SSD (SATA only)

Secondary HDD/SSD (SATA only)

Reserved: ODD

Unused

PCIe:
Reserved: Ethernet
(if not combo w/SD Card)

Unused

PP1V5_S0 — R1130 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.AY5:2.54mm

PPVRTC_G3H — R1100 330K 5% 1/20W MF 201; R1101 1M 5% 1/20W MF 201; R1102 20K 5% 1/20W MF 201; R1103 20K 5% 1/20W MF 201
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
C1102 1UF 10% 10V X5R 402; C1103 1UF 10% 10V X5R 402

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
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PCIE_CLK100M_SSD_N — CLKOUT_PCIE_N0 Y43
PCIE_CLK100M_SSD_P — CLKOUT_PCIE_P0 Y45
SSD_CLKREQ_L — PCIECLKRQ0*/GPIO73 AB1
NC_PCIE_CLK100M_ENETSDN — CLKOUT_PCIE_N1 AA44
NC_PCIE_CLK100M_ENETSDP — CLKOUT_PCIE_P1 AA42
XDP_DD2_ENETSD_CLKREQ_L — PCIECLKRQ1*/GPIO18 AF1
PCIE_CLK100M_AP_N — CLKOUT_PCIE_N2 AB43
PCIE_CLK100M_AP_P — CLKOUT_PCIE_P2 AB45
XDP_DD3_AP_CLKREQ_L — PCIECLKRQ2*/GPIO20/SMI* AF3
PCIE_CLK100M_CAMERA_N — CLKOUT_PCIE_N3 AD43
PCIE_CLK100M_CAMERA_P — CLKOUT_PCIE_P3 AD45
CAMERA_CLKREQ_L — PCIECLKRQ3*/GPIO25 T3
NC_PCIE_CLK100M_GPUN — CLKOUT_PCIE_N4 AF43
NC_PCIE_CLK100M_GPUP — CLKOUT_PCIE_P4 AF45
TBT_CLKREQ_L — PCIECLKRQ4*/GPIO26 V3
NC_PCIE_CLK100M_PE5N — CLKOUT_PCIE_N5 AE44
NC_PCIE_CLK100M_PE5P — CLKOUT_PCIE_P5 AE42
PCH_CLKRQ5_L_GPIO44 — PCIECLKRQ5*/GPIO44 (IPU-RSMRST#) AA2
NC_PCIE_CLK100M_SWN — CLKOUT_PCIE_N6 AB40
NC_PCIE_CLK100M_SWP — CLKOUT_PCIE_P6 AB39
PEG_CLKREQ_L — PCIECLKRQ6*/GPIO45 AE4
PCIE_CLK100M_TBT_N — CLKOUT_PCIE_N7 AJ44
PCIE_CLK100M_TBT_P — CLKOUT_PCIE_P7 AJ42
PCH_CLKRQ7_L_GPIO46 — PCIECLKRQ7*/GPIO46 (IPU-RSMRST#) Y3
NC_ITPXDP_CLK100MN — CLKOUT_ITPXDP_N AH43 (IPD-PWROK)
NC_ITPXDP_CLK100MP — CLKOUT_ITPXDP_P AH45 (IPD-PWROK)
LPC_CLK33M_SMC_R — CLKOUT_33MHZ0 D44 (IPD-PWROK)
NC_LPC_CLK33M_LPCPLUS_R — CLKOUT_33MHZ1 E44 (IPD-PWROK)
NC_PCI_CLK33M_OUT2 — CLKOUT_33MHZ2 B42 (IPD-PWROK)
NC_PCI_CLK33M_OUT3 — CLKOUT_33MHZ3 F41 (IPD-PWROK)
PCH_CLK33M_PCIOUT — CLKOUT_33MHZ4 A40 (IPD-PWROK)

CLOCKS

CLKOUT_PEG_A_N AB35 — NC_PCIE_CLK100M_ENETN
CLKOUT_PEG_A_P AB36 — NC_PCIE_CLK100M_ENETP
PEG_A_CLKRQ*/GPIO47 AF6 — ENET_CLKREQ_L
CLKOUT_PEG_B_N Y39 — NC_PCIE_CLK100M_PEGBN
CLKOUT_PEG_B_P Y38 — NC_PCIE_CLK100M_PEGBP
PEG_B_CLKRQ*/GPIO56 U4 — PCH_PEGCLKRQB_L_GPIO56
CLKOUT_DMI_N AF39 — DMI_CLK100M_CPU_N
CLKOUT_DMI_P AF40 — DMI_CLK100M_CPU_P
CLKOUT_DP_N AJ40 — CPU_CLK135M_DPLLSS_N
CLKOUT_DP_P AJ39 — CPU_CLK135M_DPLLSS_P
CLKOUT_DPNS_N AF35 — CPU_CLK135M_DPLLREF_N
CLKOUT_DPNS_P AF36 — CPU_CLK135M_DPLLREF_P
CLKIN_DMI_N AY24 — PCIE_CLK100M_PCH_N
CLKIN_DMI_P AW24 — PCIE_CLK100M_PCH_P
CLKIN_GND_N AR24 — PCH_CLKIN_GNDN
CLKIN_GND_P AT24 — PCH_CLKIN_GNDP
CLKIN_DOT96_N H33 — PCH_CLK96M_DOT_N
CLKIN_DOT96_P G33 — PCH_CLK96M_DOT_P
CLKIN_SATA_N BE6 — PCH_CLK100M_SATA_N
CLKIN_SATA_P BC6 — PCH_CLK100M_SATA_P
REFCLK14IN F45 — PCH_CLK14P3M_REFCLK
CLKIN_33MHZLOOPBACK D17 — PCH_CLK33M_PCIIN
XTAL25_IN AM43 — SYSCLK_CLK25M_SB_R
XTAL25_OUT AL44 NC
(IPD-PWROK) CLKOUTFLEX0/GPIO64 C40 — NC_PCH_GPIO64_CLKOUTFLEX0
(IPD-PWROK) CLKOUTFLEX1/GPIO65 F38 — NC_PCH_GPIO65_CLKOUTFLEX1
(IPD-PWROK) CLKOUTFLEX2/GPIO66 F36 — NC_PCH_GPIO66_CLKOUTFLEX2
(IPD-PWROK) CLKOUTFLEX3/GPIO67 F39 — NC_PCH_GPIO67_CLKOUTFLEX3
ICLK_IREF AM45 — PP1V5_S0
TP19 AD39 NC; TP18 AD38 NC
DIFFCLK_BIASREF AN44 — PCH_DIFFCLK_BIASREF — R1190 7.5K 1% 1/20W MF 201 — PP1V5_S0
PLACE_NEAR=U1100.AN44:2.54mm

Unused clock terminations for FCIM Mode

R1196 10K — PCIE_CLK100M_PCH_N
R1195 10K — PCIE_CLK100M_PCH_P
R1171 10K — PCH_CLKIN_GNDN
R1170 10K — PCH_CLKIN_GNDP
R1192 10K — PCH_CLK96M_DOT_N
R1191 10K — PCH_CLK96M_DOT_P
R1194 10K — PCH_CLK100M_SATA_N
R1193 10K — PCH_CLK100M_SATA_P
R1197 10K — PCH_CLK14P3M_REFCLK
5% 1/20W MF 201

R1172 340 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB
1.5V -> 1.1V
R1173 1K 1% 1/20W MF 201

NOTE: ENET pair only used if SD Card Reader is USB3.

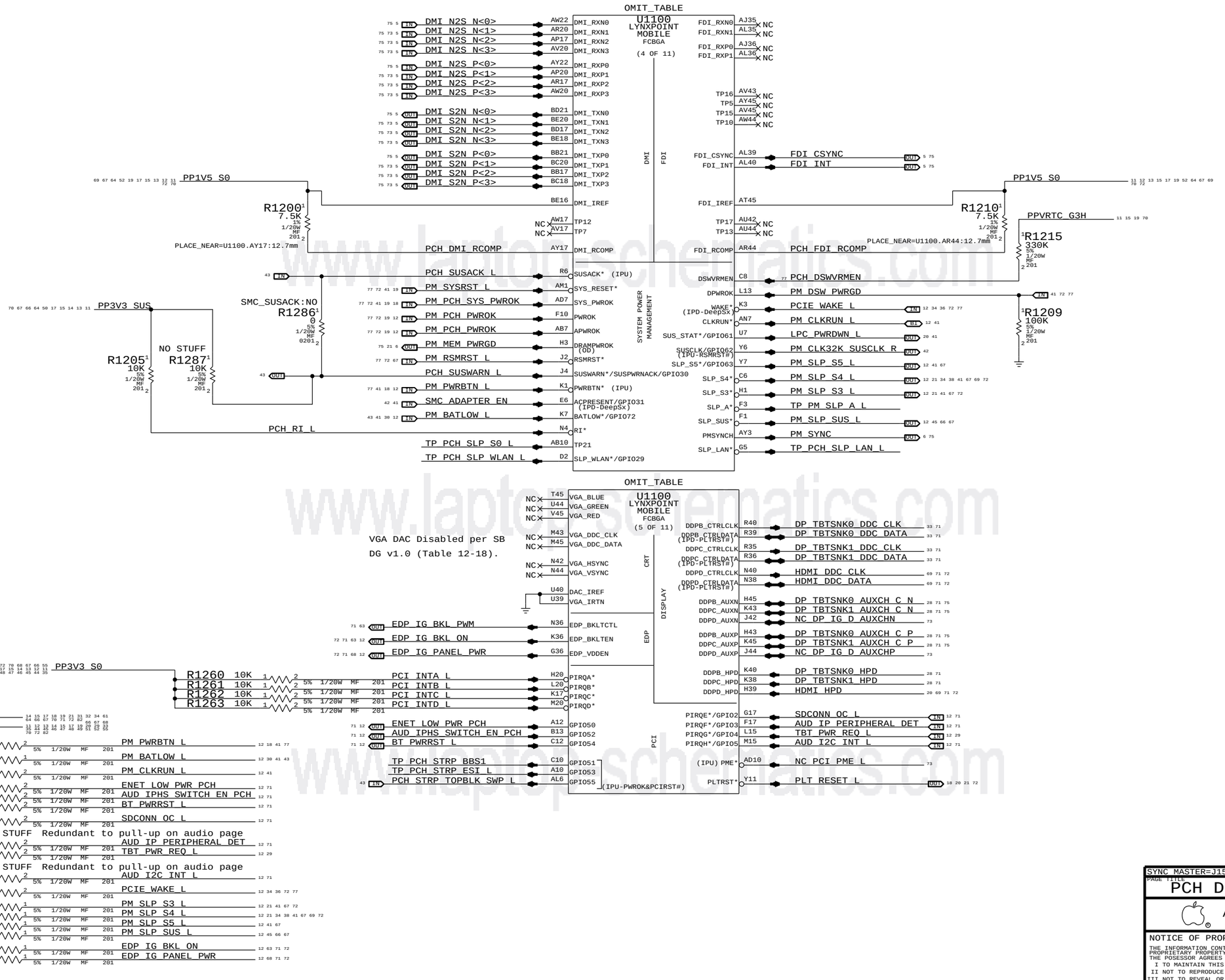
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

PP3V3_SUS
PP3V3_S0

R1177 4.7K — PCH_SPKR
R1176 10K — DP_TBT_SEL
R1178 4.7K — PCH_SATALED_L
R1134 10K — DP_AUXCH_ISOL_L
R1133 10K — XDP_DC1_SATARDRVR_EN
R1143 10K — SSD_CLKREQ_L
R1142 10K — XDP_DD2_ENETSD_CLKREQ_L
R1169 10K — AP_CLKREQ_L
R1144 10K — CAMERA_CLKREQ_L
R1145 10K — TBT_CLKREQ_L
R1147 10K — PCH_CLKRQ5_L_GPIO44
R1114 10K — PEG_CLKREQ_L
R1115 10K — PCH_CLKRQ7_L_GPIO46
R1146 10K — ENET_CLKREQ_L
R1148 10K — PCH_PEGCLKRQB_L_GPIO56
R1179 10K — ENET_MEDIA_SENSE_RDIV
5% 1/20W MF 201

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012
PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 11 OF 118
SHEET: 11 OF 82



SYNC_MASTER=J15 REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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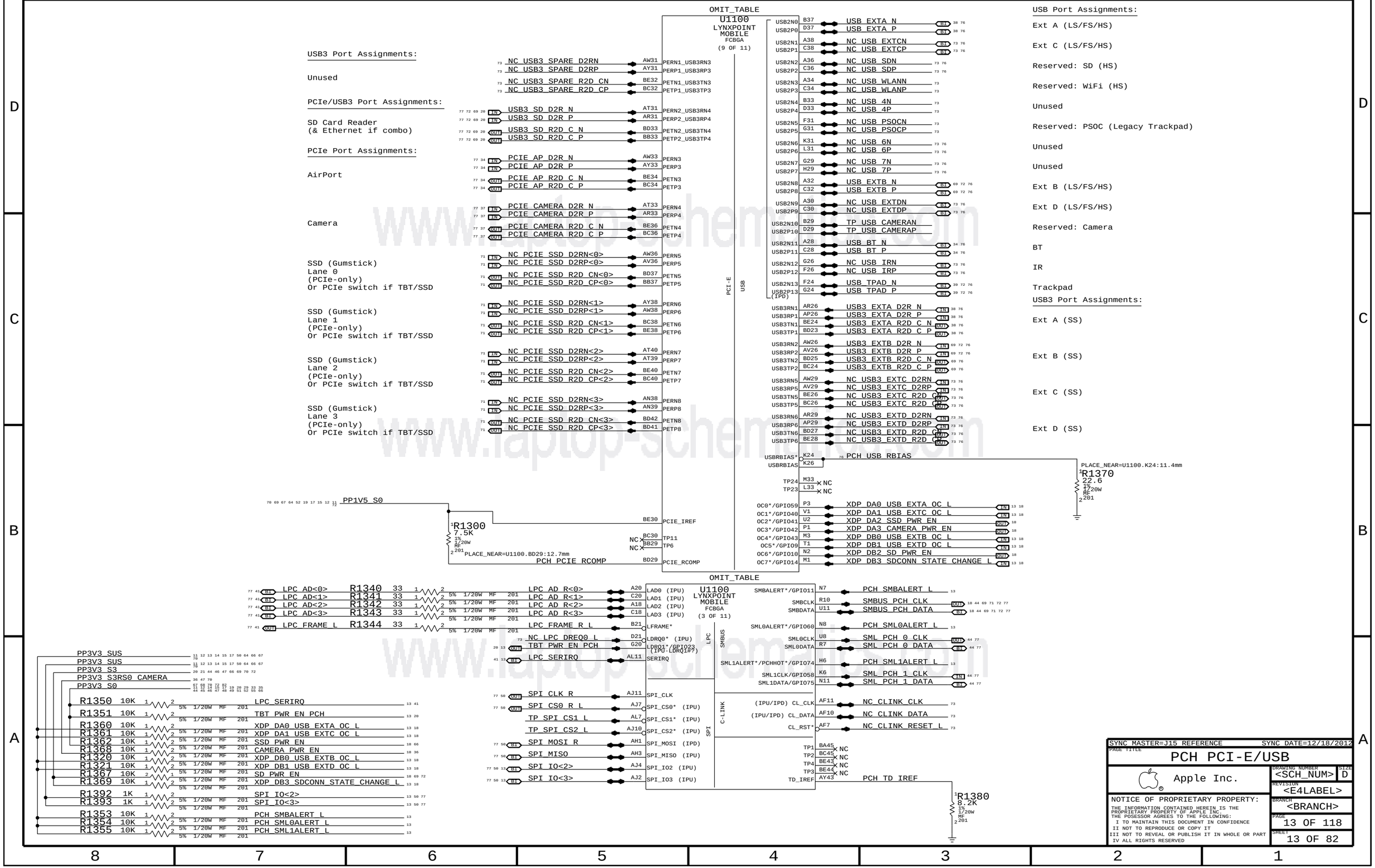
SHEET 12 OF 82


OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
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PCI-E
USB
USB3 Port Assignments:
Unused
PCIe/USB3 Port Assignments:
SD Card Reader
(& Ethernet if combo)
PCIe Port Assignments:
AirPort
Camera
SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD
NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP
USB3_SD_D2R_N
USB3_SD_D2R_P
USB3_SD_R2D_C_N
USB3_SD_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_CAMERA_D2R_N
PCIE_CAMERA_D2R_P
PCIE_CAMERA_R2D_C_N
PCIE_CAMERA_R2D_C_P
NC_PCIE_SSD_D2RN<0>
NC_PCIE_SSD_D2RP<0>
NC_PCIE_SSD_R2D_CN<0>
NC_PCIE_SSD_R2D_CP<0>
NC_PCIE_SSD_D2RN<1>
NC_PCIE_SSD_D2RP<1>
NC_PCIE_SSD_R2D_CN<1>
NC_PCIE_SSD_R2D_CP<1>
NC_PCIE_SSD_D2RN<2>
NC_PCIE_SSD_D2RP<2>
NC_PCIE_SSD_R2D_CN<2>
NC_PCIE_SSD_R2D_CP<2>
NC_PCIE_SSD_D2RN<3>
NC_PCIE_SSD_D2RP<3>
NC_PCIE_SSD_R2D_CN<3>
NC_PCIE_SSD_R2D_CP<3>
PERN1_USB3RN3
PERP1_USB3RP3
PETN1_USB3TN3
PETP1_USB3TP3
PERN2_USB3RN4
PERP2_USB3RP4
PETN2_USB3TN4
PETP2_USB3TP4
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
PP1V5_S0
R1300
7.5K
1% 1/20W MF 201
PLACE_NEAR=U1100.BD29:12.7mm
PCH_PCIE_RCOMP
PCIE_IREF
PCIE_RCOMP
NC
TP11
TP6
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Reserved: SD (HS)
Reserved: WiFi (HS)
Unused
Reserved: PSOC (Legacy Trackpad)
Unused
Unused
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
Reserved: Camera
BT
IR
Trackpad
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
USB2N0
USB2P0
USB2N1
USB2P1
USB2N2
USB2P2
USB2N3
USB2P3
USB2N4
USB2P4
USB2N5
USB2P5
USB2N6
USB2P6
USB2N7
USB2P7
USB2N8
USB2P8
USB2N9
USB2P9
USB2N10
USB2P10
USB2N11
USB2P11
USB2N12
USB2P12
USB2N13
USB2P13
(IPD)
USB_EXTA_N
USB_EXTA_P
NC_USB_EXTCN
NC_USB_EXTCP
NC_USB_SDN
NC_USB_SDP
NC_USB_WLANN
NC_USB_WLANP
NC_USB_4N
NC_USB_4P
NC_USB_PSOCN
NC_USB_PSOCP
NC_USB_6N
NC_USB_6P
NC_USB_7N
NC_USB_7P
USB_EXTB_N
USB_EXTB_P
NC_USB_EXTDN
NC_USB_EXTDP
TP_USB_CAMERAN
TP_USB_CAMERAP
USB_BT_N
USB_BT_P
NC_USB_IRN
NC_USB_IRP
USB_TPAD_N
USB_TPAD_P
USB3RN1
USB3RP1
USB3TN1
USB3TP1
USB3RN2
USB3RP2
USB3TN2
USB3TP2
USB3RN5
USB3RP5
USB3TN5
USB3TP5
USB3RN6
USB3RP6
USB3TN6
USB3TP6
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
USB3_EXTB_D2R_N
USB3_EXTB_D2R_P
USB3_EXTB_R2D_C_N
USB3_EXTB_R2D_C_P
NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP
USBRBIAS*
USBRBIAS
PCH_USB_RBIAS
PLACE_NEAR=U1100.K24:11.4mm
R1370
22.6
1% 1/20W MF 201
TP24
TP23
M33
L33
NC
OC0*/GPIO59
OC1*/GPIO40
OC2*/GPIO41
OC3*/GPIO42
OC4*/GPIO43
OC5*/GPIO9
OC6*/GPIO16
OC7*/GPIO14
XDP_DA0_USB_EXTA_OC_L
XDP_DA1_USB_EXTC_OC_L
XDP_DA2_SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L
XDP_DB1_USB_EXTD_OC_L
XDP_DB2_SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(3 OF 11)
LPC
SMBUS
C-LINK
SPI
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
R1340
R1341
R1342
R1343
R1344
33
5% 1/20W MF 201
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
NC_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
LAD0 (IPU)
LAD1 (IPU)
LAD2 (IPU)
LAD3 (IPU)
LFRAME*
LDRQ0* (IPU)
LDRQ1*/GPIO23 (IPD-LDRQ1#?)
SERIRQ
SPI_CLK
SPI_CS0* (IPU)
SPI_CS1* (IPU)
SPI_CS2* (IPU)
SPI_MOSI (IPD)
SPI_MISO (IPU)
SPI_IO2 (IPU)
SPI_IO3 (IPU)
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
TP_SPI_CS2_L
SPI_MOSI_R
SPI_MISO
SPI_IO<2>
SPI_IO<3>
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPU/IPD) CL_CLK
(IPU/IPD) CL_DATA
CL_RST*
TP1
TP2
TP3
TP4
TD_IREF
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
PCH_SML0ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH_SML1ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
NC_CLINK_CLK
NC_CLINK_DATA
NC_CLINK_RESET_L
PCH_TD_IREF
R1380
9.2K
1% 1/20W MF 201
PP3V3_SUS
PP3V3_SUS
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
R1350 10K LPC_SERIRQ
R1351 10K TBT_PWR_EN_PCH
R1360 10K XDP_DA0_USB_EXTA_OC_L
R1361 10K XDP_DA1_USB_EXTC_OC_L
R1362 10K SSD_PWR_EN
R1368 10K CAMERA_PWR_EN
R1320 10K XDP_DB0_USB_EXTB_OC_L
R1321 10K XDP_DB1_USB_EXTD_OC_L
R1367 10K SD_PWR_EN
R1369 10K XDP_DB3_SDCONN_STATE_CHANGE_L
R1392 1K SPI_IO<2>
R1393 1K SPI_IO<3>
R1353 10K PCH_SMBALERT_L
R1354 10K PCH_SML0ALERT_L
R1355 10K PCH_SML1ALERT_L
5% 1/20W MF 201
SYNC MASTER=J15 REFERENCE
SYNC DATE=12/18/2012
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
13 OF 118
SHEET
13 OF 82
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Pull-up/down on chipset support page (depends on TBT controller)
Falcon Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(6 OF 11)

28 20	IN	TBT_CIO_PLUG_EVENT_L	AT8 BMBUSY*/GPIO0
71 14	IN	FW_PME_L	F13 TACH1/GPIO1
71 14	IN	DPMUX_UC_IRQ	A14 TACH2/GPIO6
41 14	IN	SMC_RUNTIME_SCI_L	G15 TACH3/GPIO7
18	OUT	XDP_FC0_HDD_PWR_EN	Y1 GPIO8 (IPU-RSMRST#)
71 14	OUT	WOL_EN	K13 LAN_PHY_PWR_CTRL/GPIO12
71 14	OUT	MEM_VDD_SEL_1V5_L	AB11 GPIO15
18 14	IN	XDP_DD0_SSD_PCIE_SEL_L	AN2 SATA4GP/GPIO16 (IPU-Boot/SATA4GP?)
71 14	BI	LPCPLUS_GPIO	C14 TACH0/GPIO17
20 14	OUT	JTAG_TBT_TMS_PCH	BB4 SCLOCK/GPIO22
71 14	BI	TBT_GO2SX_BIDIR	Y10 GPIO24
41 14	IN	SMC_WAKE_SCI_L	R11 GPIO27 (IPU-DeepSx)
21	OUT	ISOLATE_CPU_MEM_L	AD11 GPIO28
20	OUT	TBT_POC_RESET_L	AN6 GPIO34
18	OUT	XDP_FC1_GPU_GOOD	AP1 GPIO35/NMI*
18 14	OUT	XDP_DC2_ODD_PWR_EN_L	AT3 SATA2GP/GPIO36 (IPD-PLTRST#)
18	OUT	XDP_DC3_JTAG_ISP_TCK	AK1 SATA3GP/GPIO37 (IPD-PLTRST#)
20 14	IN	JTAG_ISP_TDO	AT7 SLOAD/GPIO38
20 14	OUT	JTAG_ISP_TDI	AM3 SDATAOUT0/GPIO39
71 14	OUT	FW_PWR_EN_PCH	AN4 SDATAOUT1/GPIO48
		XDP_DD1_MLB_RAMCFG1	AK3 SATA5GP/GPIO49 (IPD-Boot/SATA5GP?)
72 50 14	BI	SPIROM_USE_MLB	U12 GPIO57
20		MLB_RAMCFG3	C16 TACH4/GPIO68
20		MLB_RAMCFG2	D13 TACH5/GPIO69
20	IN	SD_SEL_PCIE_L_USB_H	G13 TACH6/GPIO70 (IPU-Boot?)
20		MLB_RAMCFG0	H15 TACH7/GPIO71 (IPU-Boot?)

CPU/MISC

GPIO

TP14	AN10	PCH_A20GATE	14
(IPD) PECI	AY1	PCH_PECI	BI 6 42 75
RCIN*	AT6	PCH_RCIN_L	14 77
PROCPWRGD	AV3	PCH_PROCPWRGD	OUT 6 18 75
THRMTRIP*	AV1	PM_THRMTRIP_L_R	72 42
PLTRST_PROC*	AU4	CPU_RESET_L	OUT 6
VSS	N10		
	A2		
	A41		
	A43		
	A44		
	B1		
	B2		
	B44		
	B45		
	BA1		
	BC1		
	BD1		
	BD2		
	BD44		
	BD45		
	BE2		
	BE3		
	D1		
	E1		
	E45		
	A4		
VSS	BE41		
	BE5		
	C45		
	A5		

PP1V05_S0 (10 15 17 18 42 62 67 70 72)
BDW_SPRT
R1457 1K 5% 1/16W MF-LF 402

R1470 43 5% 1/20W MF 201 — NO STUFF — CPU_PECI (BI 6 42 75)
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD (OUT 6 18 75)
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L (IN 6 42 75)
CRW_SPRT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R1456		BDW_SPRT

PP3V3_S0 (33 29 20 19 17 15 14 13 12 11 52 51 49 48 47 46 45 44 35 82 72 70 68 67 66 56 55)

RAMCFG0:H	R1475 10K 5% 1/20W MF 201	
RAMCFG1:H	R1474 10K 5% 1/20W MF 201	20 18 IN
RAMCFG2:H	R1473 10K 5% 1/20W MF 201	
RAMCFG3:H	R1472 10K 5% 1/20W MF 201	

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP3V3_S5 (12 15 17 18 19 21 31 32 34 61 64 66 67 70 71 72 82)
PP3V3_SUS (11 12 13 15 17 50 64 66 67 70)
PP3V3_S0 (66 67 68 70 72 82 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55)

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K 5% 1/20W MF 201	FW_PME_L	14 71
R1411	20K 5% 1/20W MF 201	DPMUX_UC_IRQ	14 71
R1496	10K 5% 1/20W MF 201	SMC_RUNTIME_SCI_L	14 41
R1494	10K 5% 1/20W MF 201	WOL_EN	14 71
R1489	10K 5% 1/20W MF 201	MEM_VDD_SEL_1V5_L	14 71
R1495	100K 5% 1/20W MF 201	XDP_DD0_SSD_PCIE_SEL_L	14 18
R1490	100K 5% 1/20W MF 201	LPCPLUS_GPIO	14 71
R1412	10K 5% 1/20W MF 201	JTAG_TBT_TMS_PCH	14 20
R1492	10K 5% 1/20W MF 201	TBT_GO2SX_BIDIR	14 71
R1491	10K 5% 1/20W MF 201	SMC_WAKE_SCI_L	14 41
R1498	10K 5% 1/20W MF 201	XDP_DC2_ODD_PWR_EN_L	14 18
R1413	10K 5% 1/20W MF 201	JTAG_ISP_TCK	18 20
R1486	10K 5% 1/20W MF 201	JTAG_ISP_TDO	14 20
R1499	10K 5% 1/20W MF 201	JTAG_ISP_TDI	14 20
R1484	10K 5% 1/20W MF 201	FW_PWR_EN_PCH	14 71
R1493	100K 5% 1/20W MF 201	SPIROM_USE_MLB	14 50 72

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K 5% 1/20W MF 201	PCH_A20GATE	14
R1455	10K 5% 1/20W MF 201	PCH_RCIN_L	14 77

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(7 OF 11)

PP1V05_S0
VCC: 1.312 A Max, 130mA Idle

Y26, AA24, AA26, AD20, AD22, AD24, AD26, AD28, AE18, AE20, AE22, AE24, AE26, AG18, AG20, AG22, AG24 → VCC

PLACE_NEAR=R1550.1:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

C1550
1UF
±10%
6.3V
CERM
402

R1550
5.11
1%
1/20W
MF-LF
201

PLACE_NEAR=U1100.U14:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

Powered in DeepSx

U14 → DCPSUSBYP

PP1V05_S0
VCCASW: 670mA Max, 34mA Idle

U18, U20, U22, U24, V18, V20, V22, V24, Y18, Y20, Y22, AA18 → VCCASW

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(8 OF 11)

PP3V3_SUS
VCCSUS3_3: 261mA Max, 6mA Idle

R24, R26, R28, U26 → VCCSUS3_3

M24 → VSS

PP1V05_S0
??mA Max, ??mA Idle

U35 → VCCUSBPLL

PP3V3_S0
VCC3_3: 133mA Max, 3mA Idle

L24 → VCC3_3

PP1V05_S0
VCCIO: 3629mA Max, 264mA Idle

U30, V28, V30, Y30 → VCCIO

NC → Y35 → DCPSUS2

PP1V5_S0
VCCVRM: 183mA Max, 68mA Idle

AF34 → VCCVRM

PP1V05_S0_PCH_VCC_CLK_F
??mA Max, ??mA Idle

AP45 → VCC

PP1V05_S0
VCCCLK: 306mA Max, 89mA Idle

Y32 → VCCCLK

PP3V3_S0
VCCCLK3_3: 55mA Max, 11mA Idle

M29, L29, L26, M26, U32, V32 → VCCCLK3_3

PP1V05_S0
VCCCLK: 306mA Max, 89mA Idle

AD34, AA30, AA32 → VCCCLK

PP1V05_S0
VCCCLK: 306mA Max, 89mA Idle

AD35, AG30, AG32, AD36, AE30, AE32 → VCCCLK

CORE: CRT
- VCCADAC1_5 P45 — CKPLUS_WAIVE=PwrTerm2Gnd
- VSS P43 — VGA DAC Disabled per SB DG v1.0 (Table 12-18).
- VCCADACBG3_3 M31 — CKPLUS_WAIVE=PwrTerm2Gnd

CORE: FDI
- VCCVRM BB44 — PP1V5_S0 — VCCVRM: 183mA Max, 68mA Idle
- VCCIO AN34, AN35 — PP1V05_S0 — VCCIO: 3629mA Max, 264mA Idle

CORE: HVCMOS
- VCC3_3 R30, R32 — PP3V3_S0 — VCC3_3: 133mA Max, 3mA Idle

CORE: USB3
- DCPSUS1 Y12 — NC
- VCCSUS3_3 AJ30, AJ32 — PP3V3_SUS — VCCSUS3_3: 261mA Max, 6mA Idle
- DCPSUS3 AJ26, AJ28 — NC, NC
- VCCIO AK20 — PP1V05_S0 — VCCIO: 3629mA Max, 264mA Idle
- VCCVRM AK26, AK28 — PP1V5_S0 — VCCVRM: 183mA Max, 68mA Idle

CORE: PCIE/DMI
- VCCVRM BE22 — PP1V5_S0 — VCCVRM: 183mA Max, 68mA Idle
- VCCIO AK18

CORE: SATA
- VCCVRM AN11 — PP1V5_S0 — VCCVRM: 183mA Max, 68mA Idle
- VCCIO AK22

CORE: VCCMPHY
- VCCIO AM18, AM20, AM22, AP22, AR22, AT22

USB: GPIO/LPC
- VCCSUS3_3 R20, R22 — PP3V3_SUS — VCCSUS3_3: 261mA Max, 6mA Idle
- VCCDSW3_3 A16 — PP3V3_S5 — 15 mA Max, 1mA Idle
- DCPSST AA14 — PPVOUT_S0_PCH_DCPSST — BYPASS=U1100.AA14::6.35mm
  MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V
- VCC3_3 AE14, AF12, AG14 — PP3V3_S0 — VCC3_3: 133mA Max, 3mA Idle
- VCCIO U36 — PP1V05_S0 — VCCIO: 3629mA Max, 264mA Idle

C1580 0.1UF 20% 10V CERM 402

USB: HDA
- VCCSUSHDA A26 — PP1V5_S0 — 10mA Max, 1mA Idle

USB: RTC
- VCCSUS3_3 K8 — PP3V3_SUS — VCCSUS3_3: 261mA Max, 6mA Idle
- VCCRTC A6 — PPVRTC_G3H — 6uA Max (3.0V, room temperature)
- DCPRTC P14, P16 — PPVOUT_S0_PCH_DCPRTC — BYPASS=U1100.P14::6.35mm
  MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V

C1590 0.1UF 20% 10V CERM 402

C1533 0.1UF 20% 10V CERM 402
C1532 0.1UF 20% 10V CERM 402
C1531 1UF 10% 6.3V CERM 402
BYPASS=U1100.A6::6.35mm

CPU
- V_PROC_IO AJ12, AJ14 — PP1V05_S0 — 4mA Max, 2mA Idle

SPI
- VCCSPI AD12 — PP3V3_SUS — 22mA Max, 1mA Idle

CLK/MISC
- NOTE: Pin name is VCC but really is 3.3V
- VCC P18, P20 — PP3V3_S0 — ??mA Max, ??mA Idle
- VCCASW L17 — PP1V05_S0 — VCCASW: 670mA Max, 34mA Idle
- VCCASW R18 — PP1V05_S0 — VCCASW: 670mA Max, 34mA Idle

THERMAL
- VCCVRM AW40 — PP1V5_S0 — VCCVRM: 183mA Max, 68mA Idle
- VCC3_3 AK30, AK32 — PP3V3_S0 — VCC3_3: 133mA Max, 3mA Idle

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: PCH Power

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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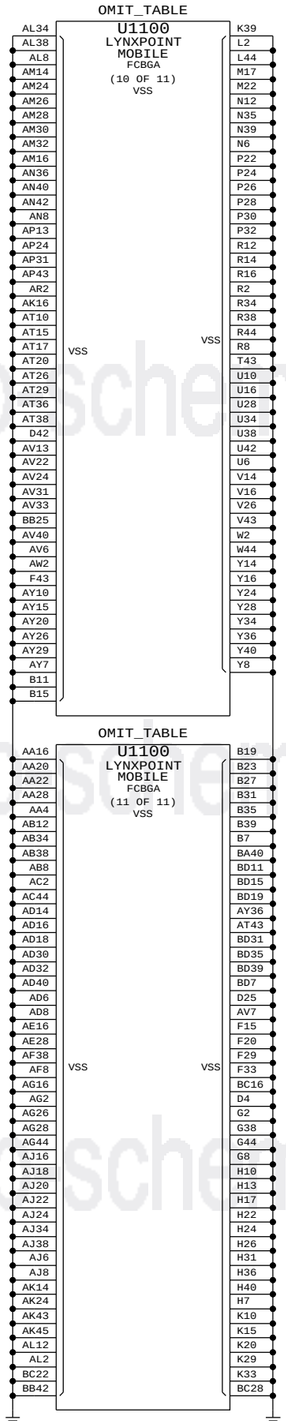

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 10% 16V CERM 402
BYPASS=U1100.R20::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 10% 16V CERM 402
BYPASS=U1100.R26::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8::6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26::6.35mm
BYPASS=U1100.L29::6.35mm
BYPASS=U1100.M29::6.35mm
BYPASS=U1100.U32::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 10% 16V CERM 402
BYPASS=U1100.R30::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 10% 16V CERM 402
BYPASS=U1100.L24::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 10% 16V CERM 402
BYPASS=U1100.AK30::6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18::6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18::12.7mm
BYPASS=U1100.AG22::6.35mm
BYPASS=U1100.AD20::6.35mm
BYPASS=U1100.AE18::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18::12.7mm
BYPASS=U1100.AK22::6.35mm
BYPASS=U1100.AK20::6.35mm
BYPASS=U1100.AM18::6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30::6.35mm
BYPASS=U1100.AG30::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26::6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34::12.7mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12::12.7mm
BYPASS=U1100.AJ12::6.35mm
BYPASS=U1100.AJ12::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30::6.35mm

PP1V05_S0
??mA Max, ??mA Idle
R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603
PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45::12.7mm
BYPASS=U1100.AP45::6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

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PAGE TITLE
PCH DECOUPLING

Apple Inc.

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05_S0 → R1830 150 5% 1/16W MF-LF 402

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 XDP (PLACE_NEAR=U0500.F50:2.54mm)
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 XDP (PLACE_NEAR=U5000.J3:2.54mm)
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402 XDP

C1804 0.1UF 10% 6.3V CERM-X5R 0201 XDP
R1831 1K 5% 1/16W MF-LF 402 XDP
C1800 0.1UF 10% 6.3V CERM-X5R 0201 XDP
C1801 0.1UF 10% 6.3V CERM-X5R 0201 XDP
C1806 0.1UF 10% 6.3V CERM-X5R 0201 XDP

XDP_CPU_PRESENT_L

PP1V05_S0 → R1820 51 5% 1/20W MF 201 XDP (PLACE_NEAR=U0500.M49:28mm) → XDP_CPU_TDO
R1823 51 5% 1/20W MF 201 XDP (PLACE_NEAR=U0500.N54:28mm) → XDP_CPU_TCK
R1824 51 5% 1/20W MF 201 XDP (PLACE_NEAR=U0500.M53:28mm) → XDP_CPUPCH_TRST_L

TDI and TMS are terminated in CPU.

R1805 1K 5% 1/20W MF 201 XDP (PLACE_NEAR=U0500.A67:2.54mm) PLT_RESET_L

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL Q1840 DMN5L06VK-7 SOT563 VER 5 XDP (PLACE_NEAR=J1800.51:28mm) → XDP_CPU_TDO
CRITICAL Q1840 DMN5L06VK-7 SOT563 VER 5 XDP (PLACE_NEAR=J1800.53:28mm) → XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)
CRITICAL Q1842 DMN5L06VK-7 SOT563 VER 5 XDP (PLACE_NEAR=J1800.55:28mm) → XDP_CPU_TDI
CRITICAL Q1842 DMN5L06VK-7 SOT563 VER 5 XDP (PLACE_NEAR=J1800.57:28mm) → XDP_CPU_TMS

PCH/XDP Signals

OMIT (All 10 R's)

			Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L	R1890 SHORT		USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895 SHORT		SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893 SHORT		CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894 SHORT		USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896 SHORT		SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897 SHORT		SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872 SHORT		DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN	MAKE_BASE=TRUE		XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L	MAKE_BASE=TRUE		XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875 SHORT		JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876 SHORT		SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1	MAKE_BASE=TRUE		XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L	MAKE_BASE=TRUE		XDP_DD2_ENETSD_CLKREQ
XDP_DD3_AP_CLKREQ_L	R1879 SHORT		AP_CLKREQ_L

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC)
R1845 330K 5% 1/20W MF 201
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS
XDP_PCH_TDO → R1860 51 5% 1/20W MF 201 XDP (PLACE_NEAR=U1100.AD3:28mm)
XDP_PCH_TDI → R1861 51 5% 1/20W MF 201 XDP (PLACE_NEAR=U1100.AE2:28mm)
XDP_PCH_TMS → R1862 51 5% 1/20W MF 201 XDP (PLACE_NEAR=U1100.AD1:28mm)
XDP_PCH_TCK → R1866 51 5% 1/20W MF 201 XDP (PLACE_NEAR=U1100.AB3:28mm)

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: CPU & PCH XDP

Apple Inc.

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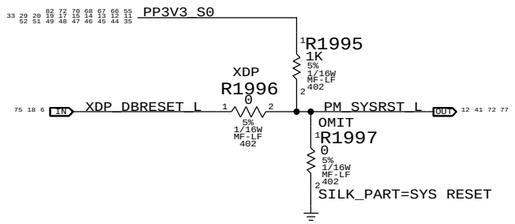
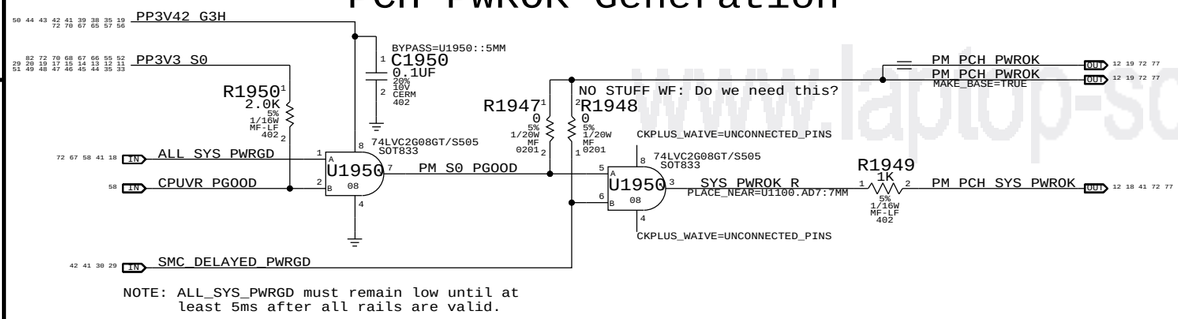
PCH Reset Button

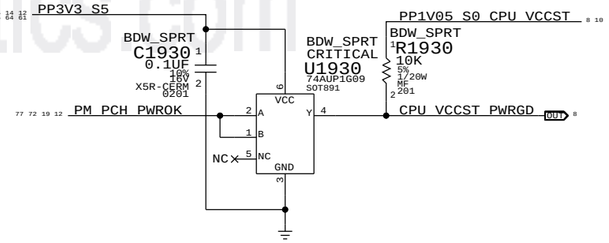


PCH PWROK Generation

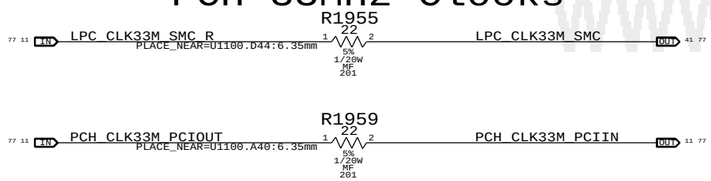


NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

VCCST (1.05V S0) PWRGD



PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

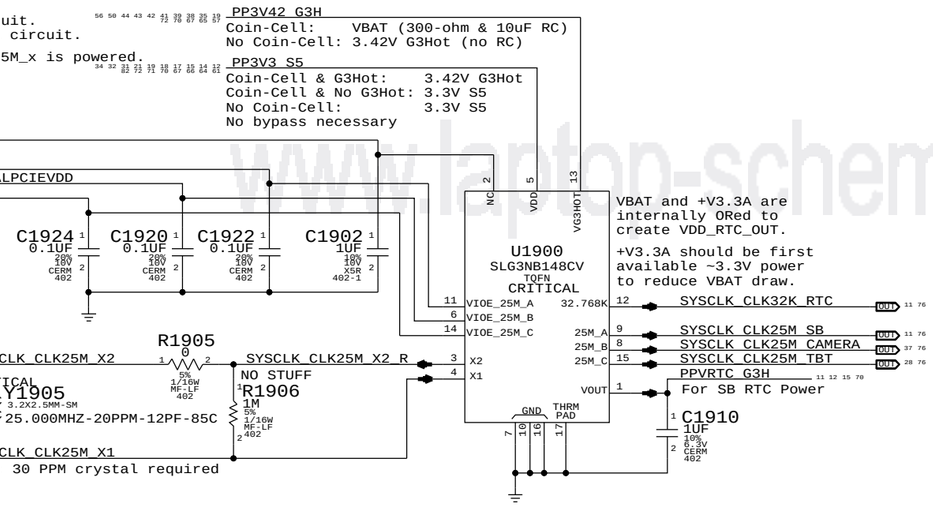
PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenClk 25MHz Power — PP3V3_S5

SB XTAL Power — PP1V5_S0
Camera XTAL Power — PP1V2_CAM_XTALPCIEVDD
TBT XTAL Power — PP3V3_TBTLC

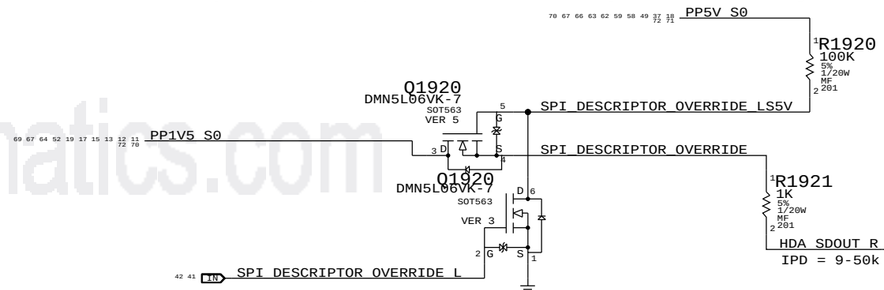
NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Falcon Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).



NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=J15_REFERENCE — SYNC_DATE=12/18/2012

PAGE TITLE: Chipset Support

Apple Inc.

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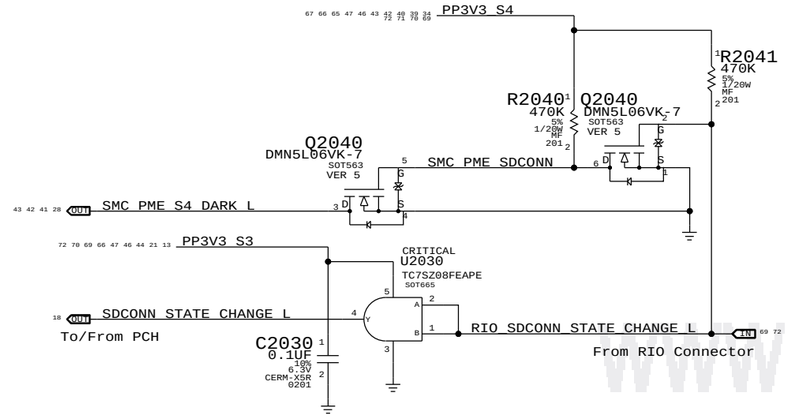
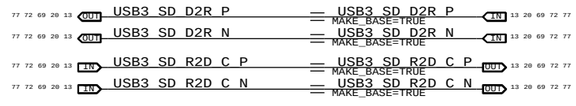
RIO SD Card Reader Support



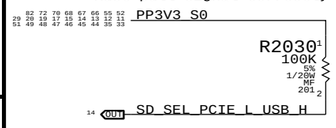
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



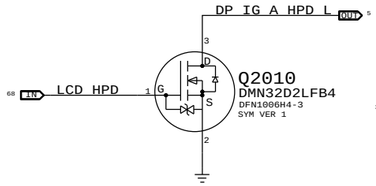
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe

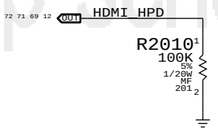


LCD HPD Inverter

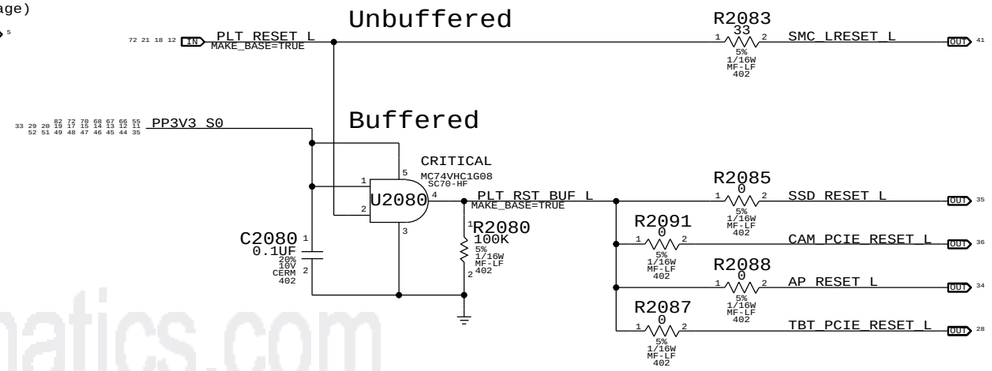
(Pull-Up on CPU Page)



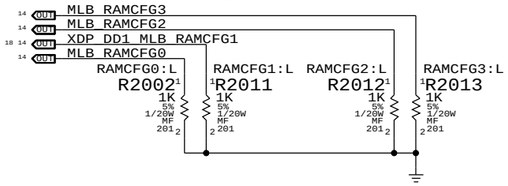
HDMI HPD pull-down



Platform Reset Connections

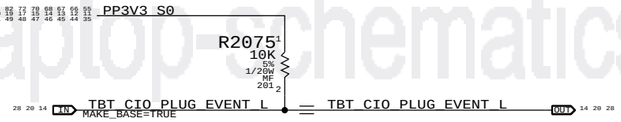


RAM Configuration Straps



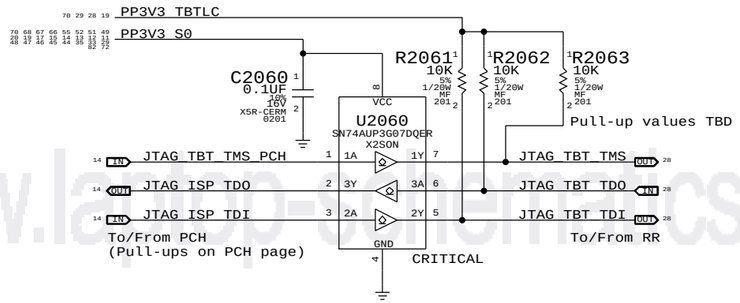
Falcon Ridge Support

RR output is open-drain, no isolation necessary

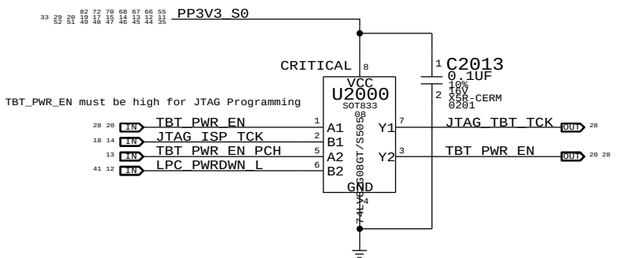


Falcon Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V

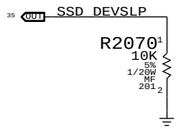


GPIO Glitch Prevention



GS3 Connector Support

DEVSLP not supported on LPT-H



SYNC_MASTER=J15_REFERENCE SYNC_DATE=01/14/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

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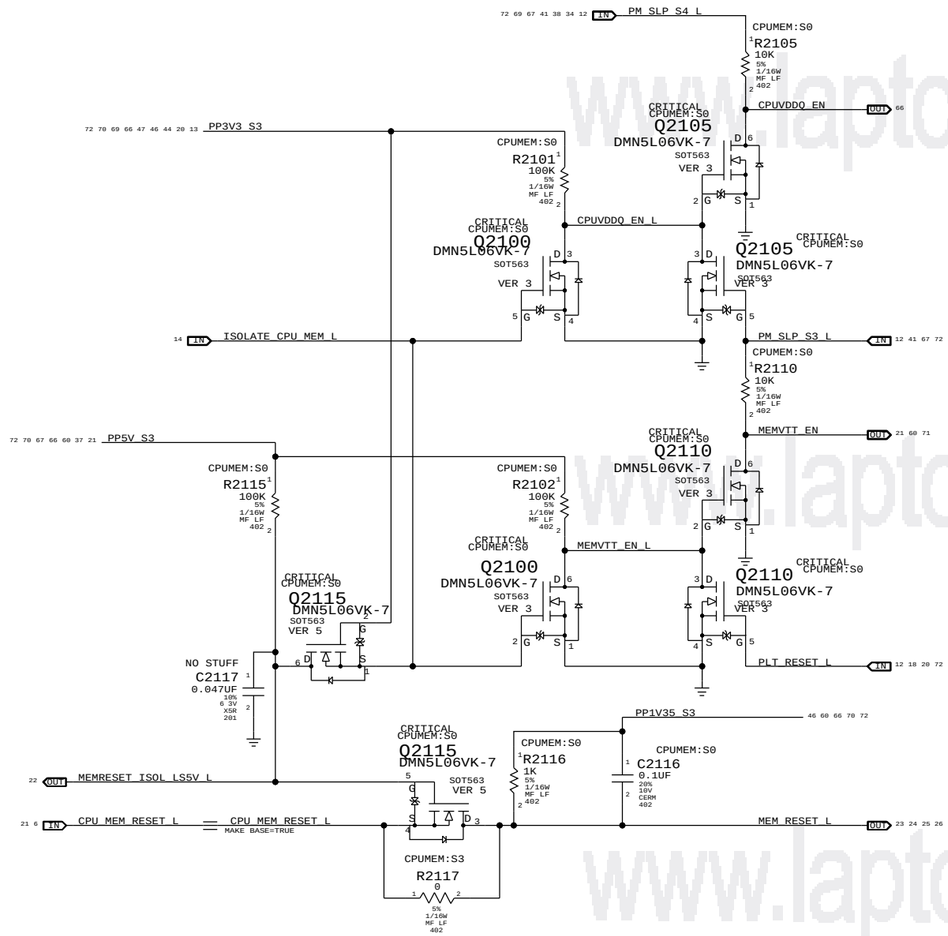
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

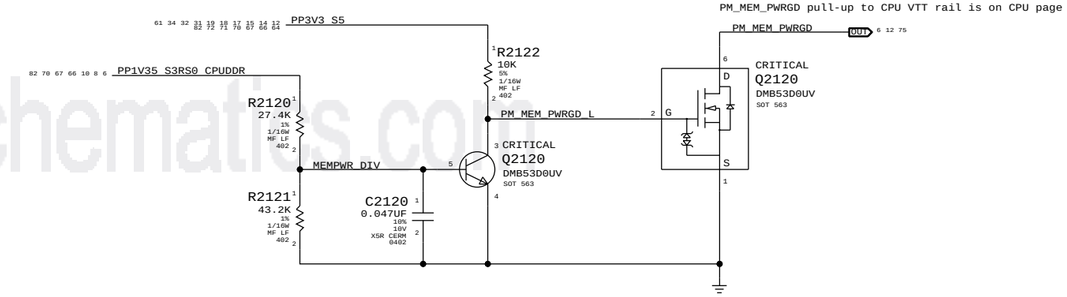
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



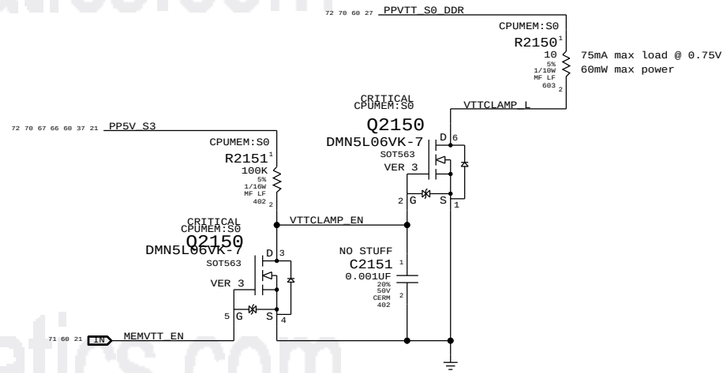
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
to	4	0	0	1	1	X	1	0	1
S0	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=CLEAN_X305G SYNC_DATE=07/01/2014

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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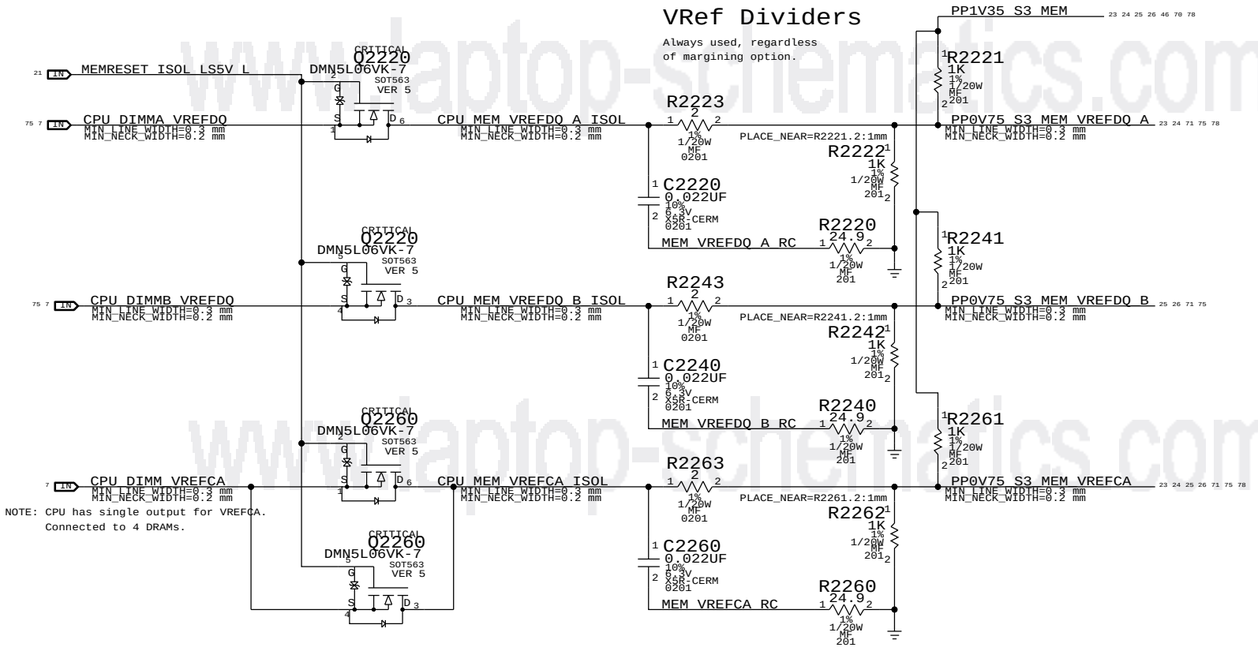
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step



NOTE: CPU has single output for VREFCA.
Connected to 4 DRAMs.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/14/2014

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

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PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA
PP1V35_S3_MEM

C2307 0.47UF 20% 4V CERM-X5R-1 201
C2308 0.047UF 10% 6.3V X5R 201
C2309 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2300
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L
MEM_A_ODT<0>
MEM_A_ZQ<0>
MEM_RESET_L
MEM_A_DQ<0> MEM_A_DQ<6> MEM_A_DQ<7> MEM_A_DQ<5> MEM_A_DQ<3> MEM_A_DQ<1> MEM_A_DQ<2> MEM_A_DQ<4>
MEM_A_DQS_P<0> MEM_A_DQS_N<0>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2300 240 1% 1/20W MF 201

C2317 0.47UF 20% 4V CERM-X5R-1 201
C2318 0.047UF 10% 6.3V X5R 201
C2319 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2310
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
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MEM_RESET_L
MEM_A_DQ<14> MEM_A_DQ<9> MEM_A_DQ<10> MEM_A_DQ<15> MEM_A_DQ<11> MEM_A_DQ<13> MEM_A_DQ<8> MEM_A_DQ<12>
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MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2310 240 1% 1/20W MF 201

C2327 0.47UF 20% 4V CERM-X5R-1 201
C2328 0.047UF 10% 6.3V X5R 201
C2329 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2320
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
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MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2320 240 1% 1/20W MF 201

C2337 0.47UF 20% 4V CERM-X5R-1 201
C2338 0.047UF 10% 6.3V X5R 201
C2339 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2330
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
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MEM_RESET_L
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MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2330 240 1% 1/20W MF 201

C2347 0.47UF 20% 4V CERM-X5R-1 201
C2348 0.047UF 10% 6.3V X5R 201
C2349 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2340
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
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MEM_A_ODT<0>
MEM_A_ZQ<4>
MEM_RESET_L
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MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2340 240 1% 1/20W MF 201

C2357 0.47UF 20% 4V CERM-X5R-1 201
C2358 0.047UF 10% 6.3V X5R 201
C2359 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2350
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L
MEM_A_ODT<0>
MEM_A_ZQ<5>
MEM_RESET_L
MEM_A_DQ<40> MEM_A_DQ<41> MEM_A_DQ<42> MEM_A_DQ<43> MEM_A_DQ<44> MEM_A_DQ<45> MEM_A_DQ<46> MEM_A_DQ<47>
MEM_A_DQS_P<5> MEM_A_DQS_N<5>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2350 240 1% 1/20W MF 201

C2367 0.47UF 20% 4V CERM-X5R-1 201
C2368 0.047UF 10% 6.3V X5R 201
C2369 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2360
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L
MEM_A_ODT<0>
MEM_A_ZQ<6>
MEM_RESET_L
MEM_A_DQ<48> MEM_A_DQ<49> MEM_A_DQ<50> MEM_A_DQ<51> MEM_A_DQ<52> MEM_A_DQ<53> MEM_A_DQ<54> MEM_A_DQ<55>
MEM_A_DQS_P<6> MEM_A_DQS_N<6>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2360 240 1% 1/20W MF 201

C2377 0.47UF 20% 4V CERM-X5R-1 201
C2378 0.047UF 10% 6.3V X5R 201
C2379 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2370
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L
MEM_A_ODT<0>
MEM_A_ZQ<7>
MEM_RESET_L
MEM_A_DQ<56> MEM_A_DQ<57> MEM_A_DQ<58> MEM_A_DQ<59> MEM_A_DQ<60> MEM_A_DQ<61> MEM_A_DQ<62> MEM_A_DQ<63>
MEM_A_DQS_P<7> MEM_A_DQS_N<7>
MEM_A_CS_L<0> MEM_A_CKE<0>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>

R2370 240 1% 1/20W MF 201

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

C2300 C2301 C2310 C2311 C2320 C2321 C2330 C2331 2.2UF 20% 10V X5R-CERM 402
C2303 C2304 C2305 C2313 C2314 C2315 C2323 C2324 C2325 C2333 C2334 C2335 0.1UF 10% 6.3V CERM-X5R 0201
C2340 C2341 C2350 C2351 C2360 C2361 C2370 C2371 2.2UF 20% 10V X5R-CERM 402
C2343 C2344 C2345 C2353 C2354 C2355 C2363 C2364 C2365 C2373 C2374 C2375 0.1UF 10% 6.3V CERM-X5R 0201

SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE_TITLE	DDR3 SDRAM Bank A (1 OF 2)
Apple Inc.	DRAWING_NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA
PP1V35_S3_MEM

C2407 0.47UF 20% 4V CERM-X5R-1 201
C2408 0.047UF 10% 6.3V X5R 201
C2409 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2400
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<8> H9

MEM_RESET_L
MEM_A_DQ<6>
MEM_A_DQ<0>
MEM_A_DQ<5>
MEM_A_DQ<7>
MEM_A_DQ<4>
MEM_A_DQ<2>
MEM_A_DQ<1>
MEM_A_DQ<3>
MEM_A_DQS_P<0>
MEM_A_DQS_N<0>
MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2400 240 1% 1/20W MF 201

C2417 0.47UF 20% 4V CERM-X5R-1 201
C2418 0.047UF 10% 6.3V X5R 201
C2419 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2410
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<9> H9

MEM_RESET_L
MEM_A_DQ<9>
MEM_A_DQ<14>
MEM_A_DQ<15>
MEM_A_DQ<10>
MEM_A_DQ<12>
MEM_A_DQ<8>
MEM_A_DQ<13>
MEM_A_DQ<11>
MEM_A_DQS_P<1>
MEM_A_DQS_N<1>
MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2410 240 1% 1/20W MF 201

C2427 0.47UF 20% 4V CERM-X5R-1 201
C2428 0.047UF 10% 6.3V X5R 201
C2429 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2420
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<10> H9

MEM_RESET_L
MEM_A_DQ<21>
MEM_A_DQ<22>
MEM_A_DQ<17>
MEM_A_DQ<16>
MEM_A_DQ<19>
MEM_A_DQ<20>
MEM_A_DQ<23>
MEM_A_DQ<18>
MEM_A_DQS_P<2>
MEM_A_DQS_N<2>
MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2420 240 1% 1/20W MF 201

C2437 0.47UF 20% 4V CERM-X5R-1 201
C2438 0.047UF 10% 6.3V X5R 201
C2439 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2430
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<11> H9

MEM_RESET_L
MEM_A_DQ<24>
MEM_A_DQ<31>
MEM_A_DQ<28>
MEM_A_DQ<27>
MEM_A_DQ<29>
MEM_A_DQ<26>
MEM_A_DQ<25>
MEM_A_DQ<30>
MEM_A_DQS_P<3>
MEM_A_DQS_N<3>
MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2430 240 1% 1/20W MF 201

C2447 0.47UF 20% 4V CERM-X5R-1 201
C2448 0.047UF 10% 6.3V X5R 201
C2449 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2440
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<12> H9

MEM_RESET_L
MEM_A_DQ<33>
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MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2440 240 1% 1/20W MF 201

C2457 0.47UF 20% 4V CERM-X5R-1 201
C2458 0.047UF 10% 6.3V X5R 201
C2459 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2450
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<13> H9

MEM_RESET_L
MEM_A_DQ<41>
MEM_A_DQ<40>
MEM_A_DQ<43>
MEM_A_DQ<42>
MEM_A_DQ<47>
MEM_A_DQ<46>
MEM_A_DQ<45>
MEM_A_DQ<44>
MEM_A_DQS_P<5>
MEM_A_DQS_N<5>
MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2450 240 1% 1/20W MF 201

C2467 0.47UF 20% 4V CERM-X5R-1 201
C2468 0.047UF 10% 6.3V X5R 201
C2469 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2460
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<14> H9

MEM_RESET_L
MEM_A_DQ<49>
MEM_A_DQ<48>
MEM_A_DQ<51>
MEM_A_DQ<50>
MEM_A_DQ<55>
MEM_A_DQ<54>
MEM_A_DQ<53>
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MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2460 240 1% 1/20W MF 201

C2477 0.47UF 20% 4V CERM-X5R-1 201
C2478 0.047UF 10% 6.3V X5R 201
C2479 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2470
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<15> H9

MEM_RESET_L
MEM_A_DQ<57>
MEM_A_DQ<56>
MEM_A_DQ<59>
MEM_A_DQ<58>
MEM_A_DQ<63>
MEM_A_DQ<62>
MEM_A_DQ<61>
MEM_A_DQ<60>
MEM_A_DQS_P<7>
MEM_A_DQS_N<7>
MEM_A_CS_L<1>
MEM_A_CKE<1>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>

R2470 240 1% 1/20W MF 201

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

PP1V35_S3_MEM

C2400 C2401 C2410 C2411 C2420 C2421 C2430 C2431 2.2UF 20% 10V X5R-CERM 402
C2403 C2404 C2405 C2413 C2414 C2415 C2423 C2424 C2425 C2433 C2434 C2435 0.1UF 10% 6.3V CERM-X5R 0201
C2440 C2441 C2450 C2451 C2460 C2461 C2470 C2471 2.2UF 20% 10V X5R-CERM 402
C2443 C2444 C2445 C2453 C2454 C2455 C2463 C2464 C2465 C2473 C2474 C2475 0.1UF 10% 6.3V CERM-X5R 0201

SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012

PAGE_TITLE
DDR3 SDRAM Bank A (2 OF 2)

Apple Inc.

DRAWING_NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
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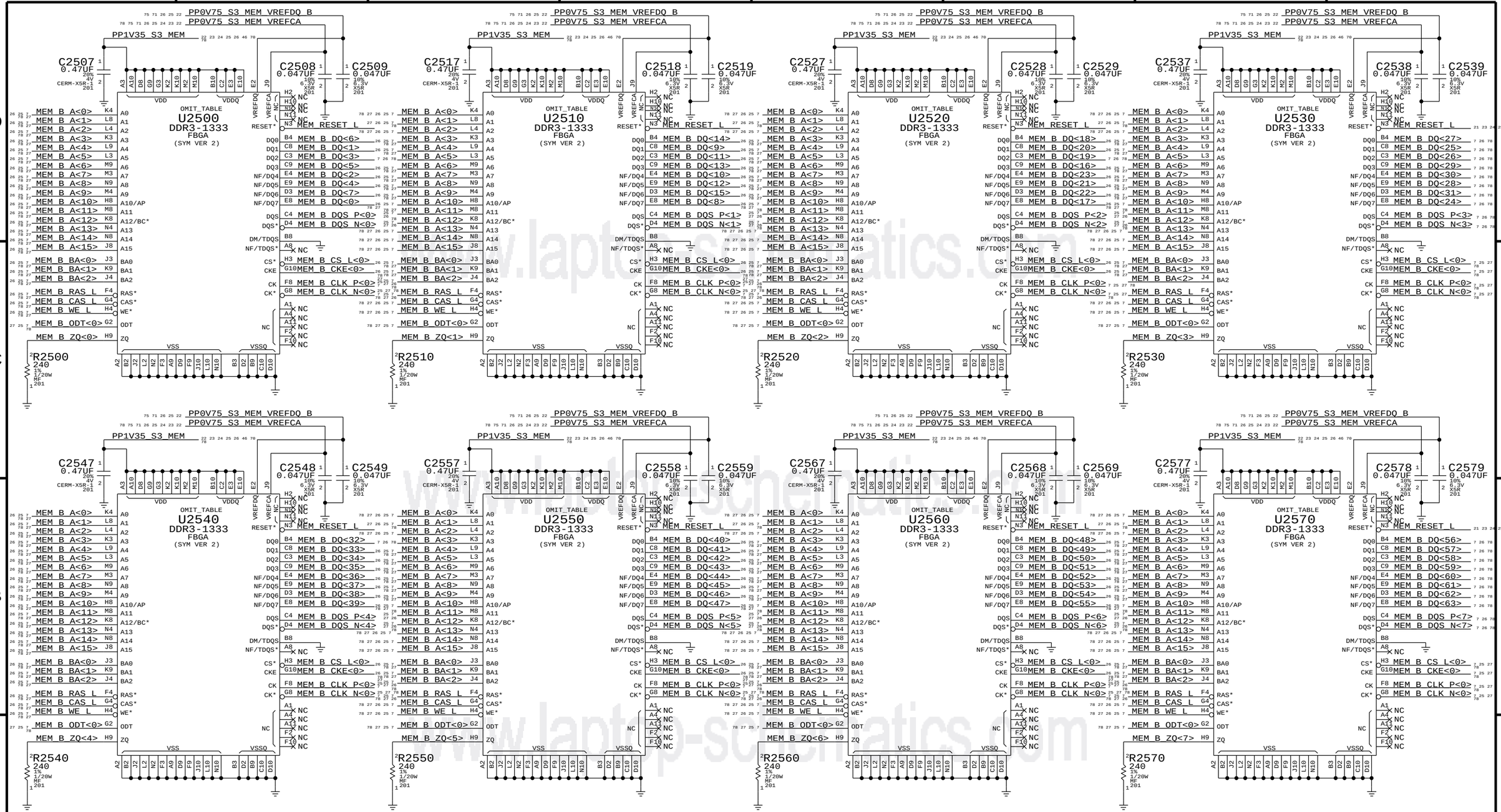

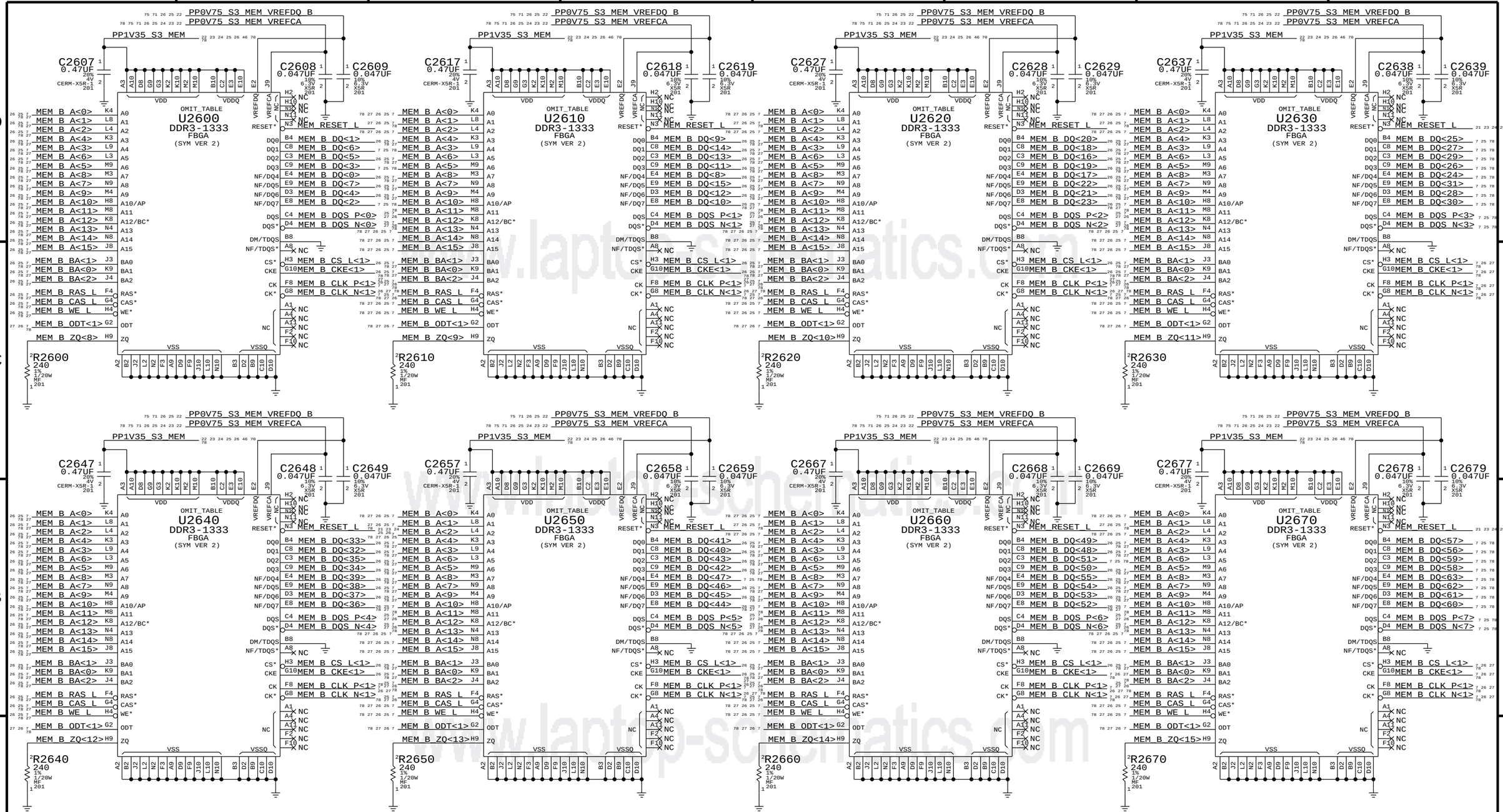

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DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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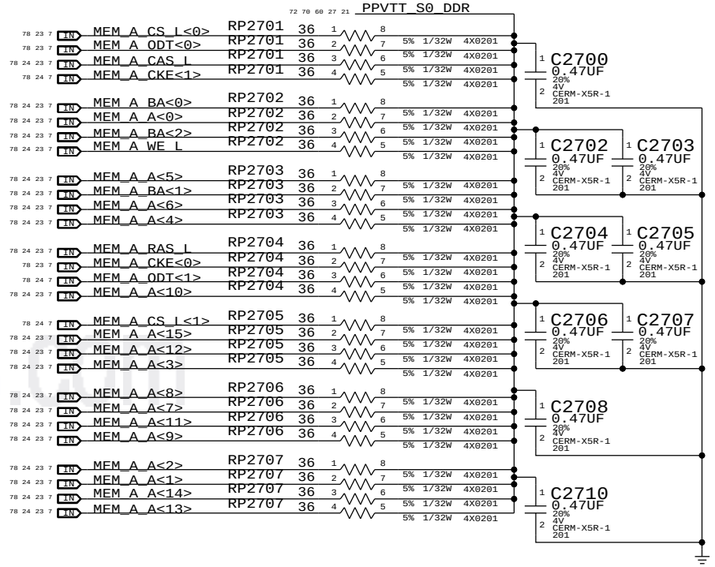
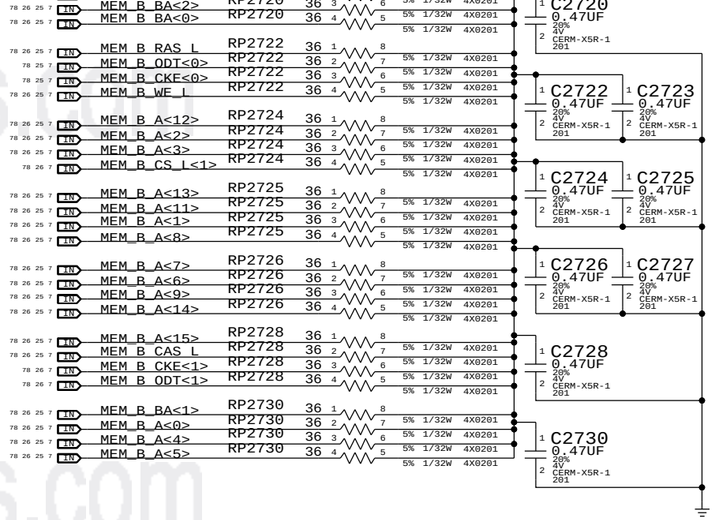
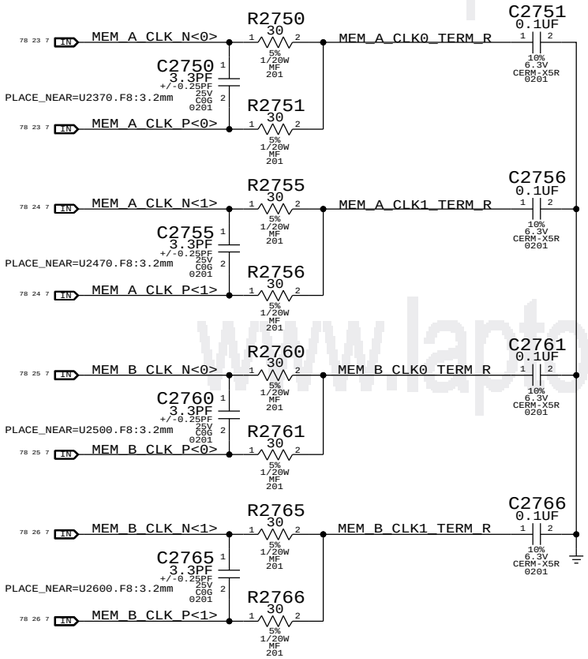
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE

DDR3 Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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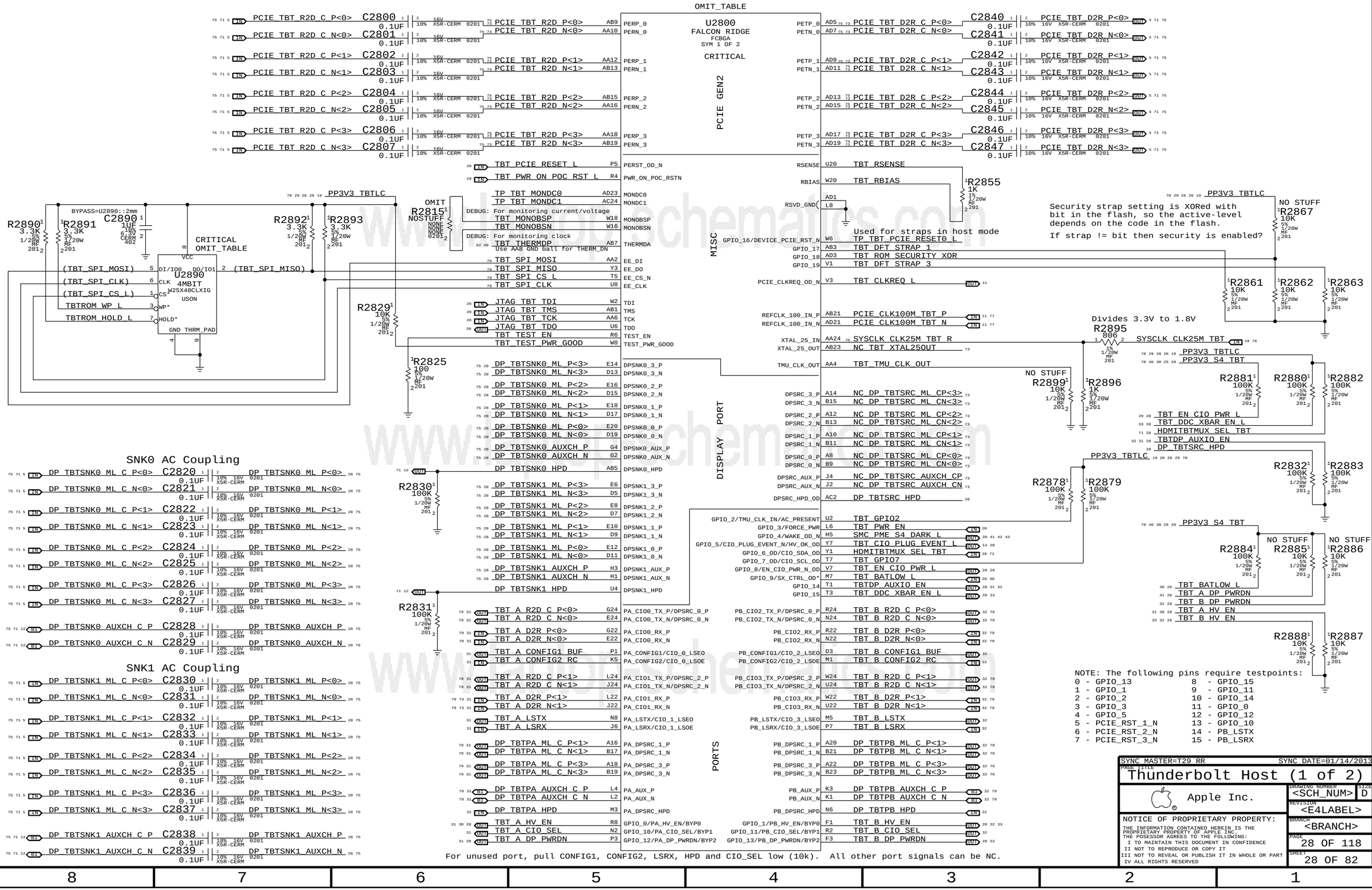

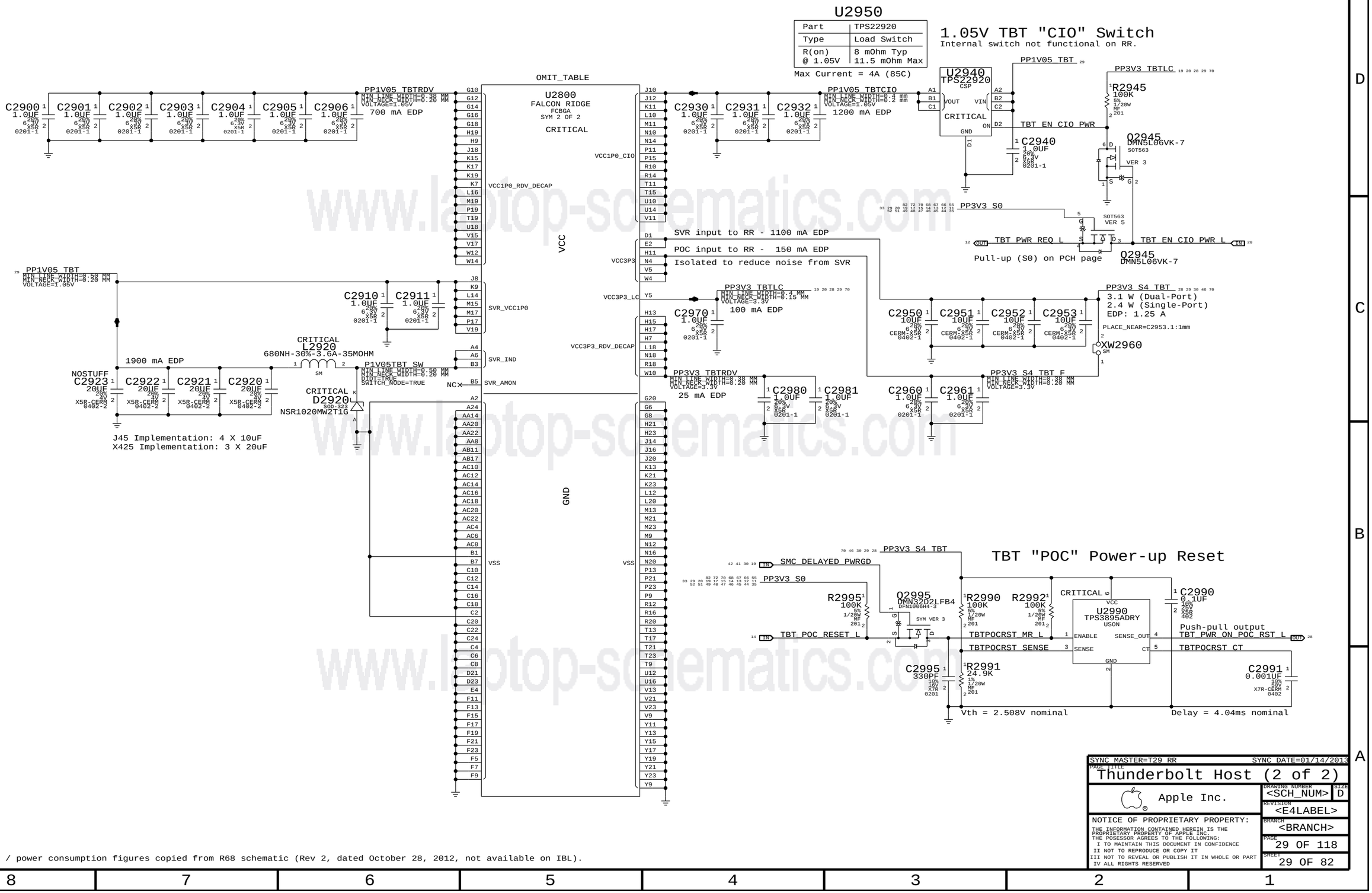

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

CRITICAL
Q3080
SI8409DB
BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPBUS_G3H
8-13V Input
Changes required
for 2S.

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here
add property on another page.

R3080 470K 5% 1/16W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

Q3005
DMN32D2LFB4
DFN1006H4-3
SYM VER 2
TBT_A_HV_EN
Second FET needed for
dual-port designs.

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V CERM 0402
R3093 49.9K 1% 1/16W MF-LF 402
R3092 73.2K 1% 1/16W MF-LF 402 <R2>
C3092 2.2UF 20% 10V X5R-CERM 402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3094 26.7K 1% 1/16W MF-LF 402
C3094 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603
R3091 200K 1% 1/16W MF-LF 402 <R1>

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC

CRITICAL
L3095
3.3UH-6.5A
PIMB063T-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090
LT3957
QFN
VIN
SW
EN/UVLO
INTVCC
VC
RT
SS
SYNC
SGND
GND
SNS1
SNS2
FBX
NC

TBTBST_SNS1
R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5
TBTBST_SNS2
R3097 10 5% 1/16W MF-LF 402
NOTE: Change R3097 to XW3095 at PVT
TBTBST_VSNS
C3088 10PF 5% 50V CERM 0402
R3095 137K 1% 1/16W MF-LF 402 <Ra>
NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>

SGND shorted to
GND inside package,
no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

PP15V_TBT
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz

C3096 10UF 20% 25V X5R-CERM 0603
NO STUFF
C3097 10UF 10% 25V X7R-CERM 1206
C3099 0.001UF 10% 50V X7R-CERM 0402
C3098 10UF 20% 25V X5R-CERM 0603
PLACE_SIDE=BOTTOM
PLACE_SIDE=TOP
NOTE: MIRROR C3096 and C3098

Q3088
DMN5L06VK-7
SOT563
VER 3
Max Vgs: 10V
R3088 330K 5% 1/10W MF-LF 402
TBTBST_SHDN_DIV
R3087 330K 5% 1/10W MF-LF 402
Q3088
DMN5L06VK-7
SOT563
VER 3
SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000
DMN32D2LFB4
DFN1006H4-3
SYM VER 3
PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_X305	SYNC_DATE=06/24/2014
PAGE_TITLE	Thunderbolt Mobile Support
Apple Inc.	DRAWING_NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

PP3V3_S5

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 0603
C3281 0.1UF 10% 16V X5R-CERM 0201

PP15V_TBT
15.75V Max

C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 16V X5R 402

CRITICAL U3210 CD3211A1RGP QFN

Pin	Name
19, 20	V3P3
18	V3P3OUT
6, 7	VHV
12, 14	OUT
16	ENHVU
4	FAULTZ
5	EN
8	ISET_V3P3
11	HV_EN
10	ISET_S0
17	S0
9	ISET_S3
1, 2, 3, 13, 15	GND
21	THRM PAD

C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V X5R 402

PP3V3_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V)
PP3V3RHV_S4_TBTAPWR (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)

S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_R_L

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3

TBTHV:P15V
R3210 22.6K 1% 1/20W MF 2012
R3211 22.6K 1% 1/20W MF 2012
R3212 36.5K 1% 1/20W MF 2012 <RV3P3>

12V: See below

TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

R3213 22.6K 1% 1/20W MF 2012 <RHVS3>
R3214 22.6K 1% 1/20W MF 2012 <RHVS0>

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

<RHVS0> ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V)

C3200 0.01UF 10% 16V X7R-CERM 0402
C3201 0.01UF 10% 16V X7R-CERM 0402
R3201 12 5% 1/20W MF 201

TBTACONN_20_RC (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V)

TBT Dir DP Dir

TBT: RX_0

GND_VOID=TRUE (Both C's)

TBT_A_D2R_P<0> / TBT_A_D2R_N<0>
C3274 0.47UF 20% 4V 201 CERM-X5R-1
C3275 0.47UF 20% 4V 201 CERM-X5R-1
TBT_A_D2R_C_P<0> / TBT_A_D2R_C_N<0>

R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE

DP_TBTPA_ML_C_P<3> / DP_TBTPA_ML_C_N<3>
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<3> / DP_TBTPA_ML_N<3>

R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201

TBT: Unused

TBT_A_D2R1_AUXDDC_P / TBT_A_D2R1_AUXDDC_N

TBT: RX_1

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R 0201
C3295 330PF 10% 16V X7R 0201
R3241 100K 5% 1/20W MF 201

C3202 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL J3200 MDP-J44 F-RT-TH SHIELD PINS S12-S16 PORT B SHIELD PINS S17-S24 514-0876

Pin	Name
B2	HPD
B4	CONFIG1
B6	CONFIG2
B8	GND2
B10	ML_LANE3P
B12	ML_LANE3N
B14	GND4
B16	AUX_CHP
B18	AUX_CHN
B20	DP_PWR
B1	GND0
B3	ML_LANE0P
B5	ML_LANE0N
B7	GND1
B9	ML_LANE1P
B11	ML_LANE1N
B13	GND3
B15	ML_LANE2P
B17	ML_LANE2N
B19	RETURN

TBTACONN_1_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)
C3205 0.01UF 10% 25V X5R-CERM 0201 GND_VOID=TRUE (0-18.9V)

TBTACONN_7_C (MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V)
C3206 0.01UF 10% 25V X5R-CERM 0201 GND_VOID=TRUE (0-18.9V)

DP Dir TBT Dir
TBT_A_R2D_P<0> / TBT_A_R2D_N<0>
TBT: TX_0

TBT_A_R2D_P<1> / TBT_A_R2D_N<1>
TBT: TX_1

DP_A_LSX_ML_P<1> / DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

GND_VOID=TRUE (Both C's)
C3270 0.22UF 20% 6.3V X5R 0201 TBT_A_R2D_C_P<0>
C3271 0.22UF 20% 6.3V X5R 0201 TBT_A_R2D_C_N<0>
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)
C3272 0.22UF 20% 6.3V X5R 0201 TBT_A_R2D_C_P<1>
C3273 0.22UF 20% 6.3V X5R 0201 TBT_A_R2D_C_N<1>
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201

CRITICAL U3220 CBTL05024 HVQFN24-COMBO SIGNAL_MODEL=TBT_MUX

Pin	Name
3	VDD
7	TB-
8	TB+
1	AUX-
2	AUX+
4	DDC_DAT
5	DDC_CLK
16	CA_DETOUT
11	DP+
10	DP-
14	LSTX (IPU)
13	LSRX (IPD)
12	HPDOUT
15	TB_ENA
24	AUXIO_EN
6	DP_PD
23	(IPU) AUXIO-
22	(IPD) AUXIO+
18	CA_DET
19	DPML0+
20	DPML0-
17	HPD
9, 21, 25	GND THMPAD

TBT_A_D2R_C_N<1> / TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N / DP_TBTPA_AUXCH_C_P
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_DDC_DATA / DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1> / DP_TBTPA_ML_N<1>
TBT_A_LSTX / TBT_A_LSRX
DP_TBTPA_HPD

TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N / TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
TBT_A_HPD

SYNC_MASTER=CLEAN X305 SYNC_DATE=06/24/2014

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT
15.75V Max
CRITICAL U3310 CD3211A1RGP QFN
S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_R_L
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTHV:P15V R3310 22.6K 1% 1/20W MF 2012
TBTHV:P15V R3311 22.6K 1% 1/20W MF 2012
R3312 36.5K 1% 1/20W MF 2012 <RV3P3>
12V: See below
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V R3313 22.6K 1% 1/20W MF 2012 <RHVS3>
TBTHV:P15V R3314 22.6K 1% 1/20W MF 2012 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET
PP3V3RHV_S4_TBTBPWR
PP3V3_S4_TBTBPWR

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

CRITICAL L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F
C3300 0.01UF 10% 16V X7R-CERM 0402
C3301 0.01UF 10% 16V X7R-CERM 0402
TBTBCONN_20_RC
R3301 12 5% 1/20W MF 201
TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
TBT: TX_0
TBT: TX_1
TBT: LSX_R2P/P2R (P/N)
TBTBCONN_1_C
TBTBCONN_7_C
(0-18.9V)
CRITICAL J3200 MDP-J44 F-RT-TH 514-0876
SHIELD PINS
PORT A
C3305 0.01UF 10% 25V X5R-CERM 0201
C3306 0.01UF 10% 25V X5R-CERM 0201
GND_VOID=TRUE (Both C's)
C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1
C3376 0.47UF 20% 4V 201 CERM-X5R-1
C3377 0.47UF 20% 4V 201 CERM-X5R-1
C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
C3330 0.1UF 10% 16V X5R-CERM 0201
C3331 0.1UF 10% 16V X5R-CERM 0201
C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
R3394 1K 5% 1/20W MF 201
R3395 1K 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201
C3320 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3320 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
TBT_B_CIO_SEL
TBTDP_AUXIO_EN
TBT_B_DP_PWRDN
TBT_B_D2R1_AUXDDC_N
TBT_B_D2R1_AUXDDC_P
TBT: RX_1
TBT_B_CONFIG1_RC
TBT_B_HPD
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_B_D2R_C_N<1>
TBT_B_D2R_C_P<1>
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD
TBT_B_D2R_C_N<0>
TBT_B_D2R_C_P<0>
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_D2R_N<0>
TBT_B_D2R_P<0>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
TBT_B_D2R_N<3>
TBT_B_D2R_P<3>
TBT_B_D2R_C_N<3>
TBT_B_D2R_C_P<3>
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R 0201
C3395 330PF 10% 16V X7R 0201
R3341 100K 5% 1/20W MF 201
C3302 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

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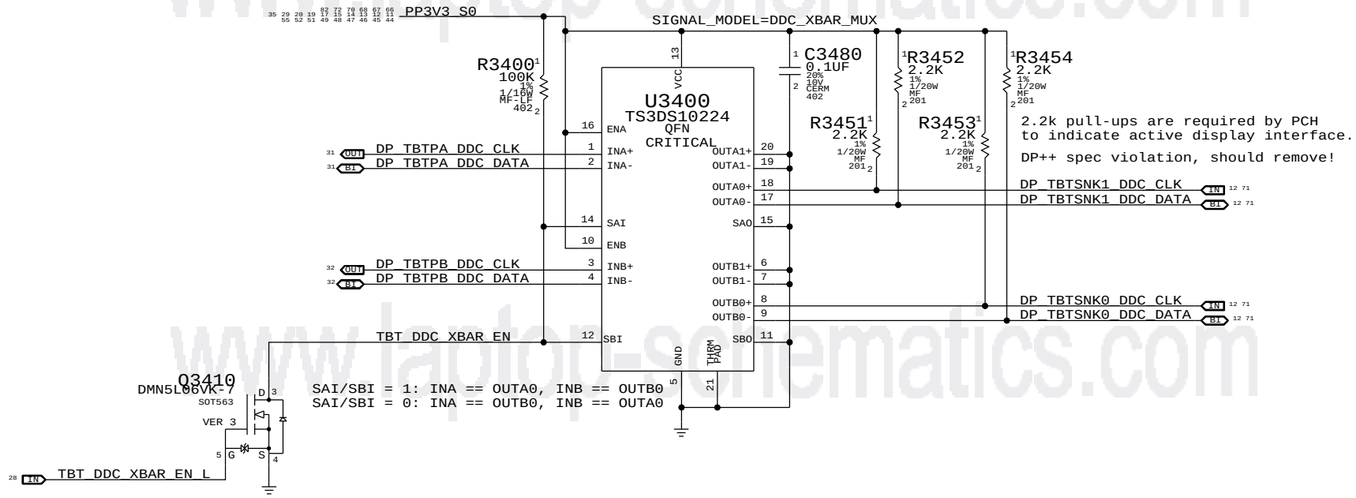
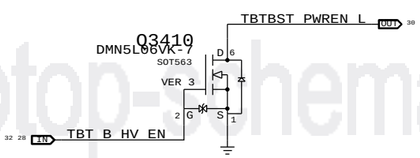
DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



SYNC MASTER=J15 REFERENCE SYNC DATE=11/16/2012

PAGE TITLE: DDC Crossbar

Apple Inc.

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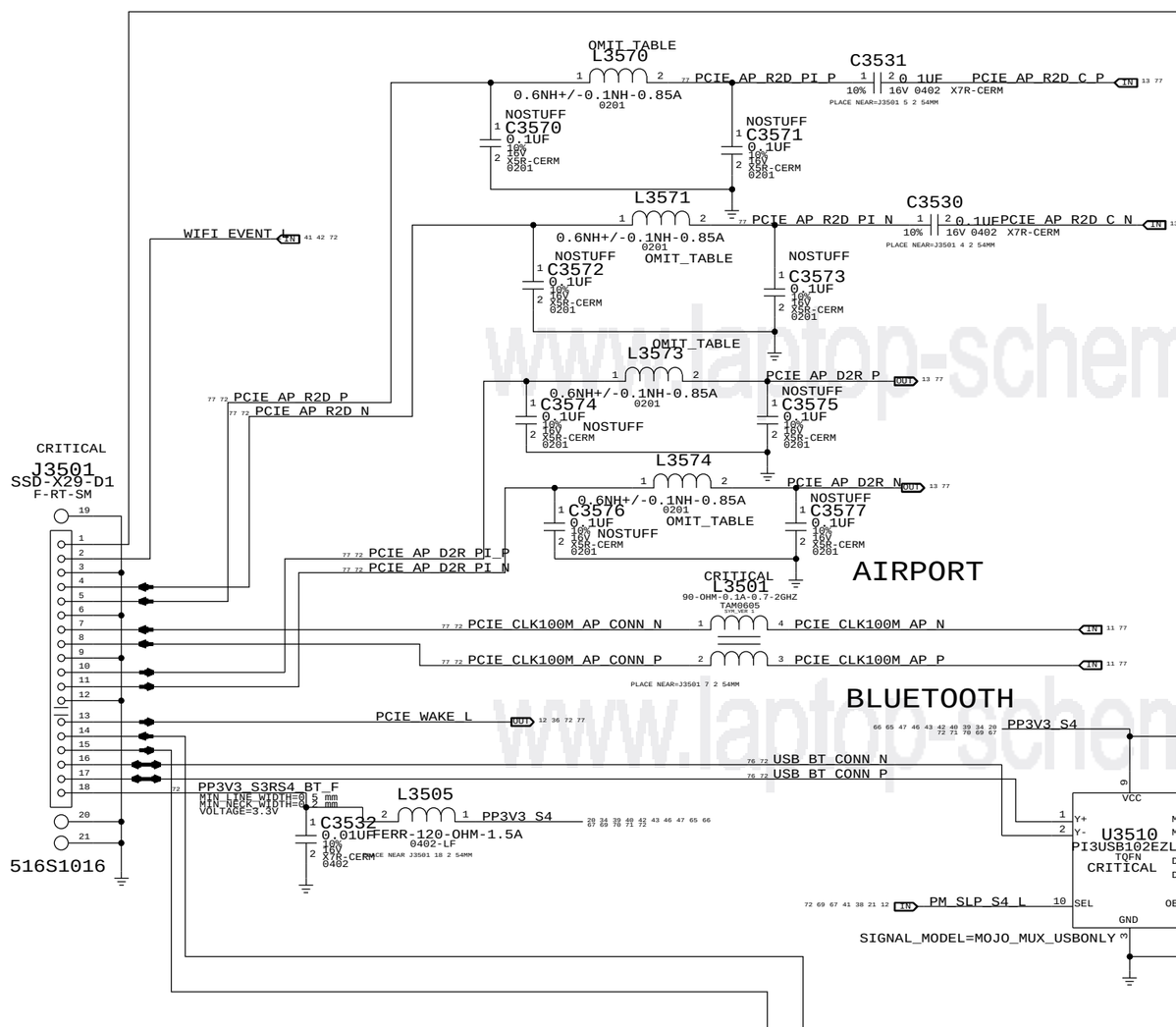
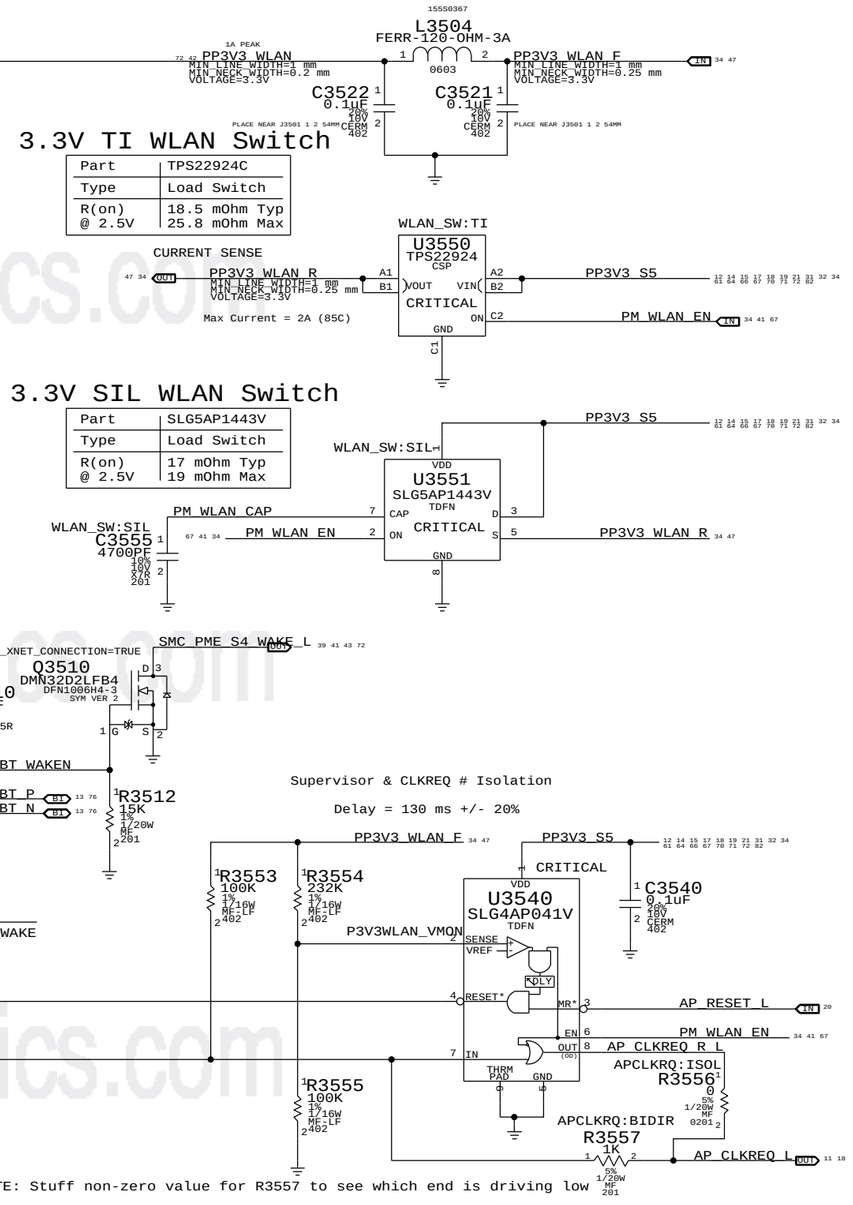
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		





SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

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Apple Inc.

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FOR DESENSE IMPROVEMENT

C3722 12PF 5% 50V C0G 0201 — PLACE_NEAR J3700 3 2mm
C3723 12PF 5% 50V C0G 0201 — PLACE_NEAR J3700 4 2mm
C3724 12PF 5% 50V C0G 0201 — PLACE_NEAR J3700 5 2mm

PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700 FERR-26-OHM-6A 0603

72 70 46 35 PP3V3 S0SW SSD

C3701 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=L3700.1:1mm
C3702 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=L3700.1:1mm

PP3V3 S0SW SSD FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V

514S0449
CRITICAL
J3700 SSD-GS3 F-RT-SM

NOSTUFF R3700 100K 1% 1/20W MF 201

33 29 20 82 72 70 68 67 66 55 52 51 49 48 47 46 45 44 35 PP3V3 S0

GND_VOID 1
2 SMC_OOB1_R2D_CONN_L
3
4
5
6
7 PP3V3_S0
8 SSD_RESET_CONN_L
9 NC_SSD_MFG_RSVD
NO_TEST=TRUE
10

11	TRUE	75 PCIE_SSD_R2D_N<3>	45	TRUE	PCIE_SSD_D2R_N<3> OUT 5 71 75
12	TRUE	75 PCIE_SSD_R2D_P<3>	44	TRUE	PCIE_SSD_D2R_P<3> OUT 5 71 75
13			43		
14	TRUE	75 PCIE_SSD_R2D_N<2>	42	TRUE	PCIE_SSD_D2R_N<2> OUT 5 71 75
15	TRUE	75 PCIE_SSD_R2D_P<2>	41	TRUE	PCIE_SSD_D2R_P<2> OUT 5 71 75
16			40		
17			39		
18	TRUE	75 PCIE_SSD_R2D_N<1>	38	TRUE	PCIE_SSD_D2R_N<1> OUT 5 71 75
19	TRUE	75 PCIE_SSD_R2D_P<1>	37	TRUE	PCIE_SSD_D2R_P<1> OUT 5 71 75
20			36		
21	TRUE	75 PCIE_SSD_R2D_N<0>	35	TRUE	PCIE_SSD_D2R_N<0> OUT 5 71 75
22	TRUE	75 PCIE_SSD_R2D_P<0>	34	TRUE	PCIE_SSD_D2R_P<0> OUT 5 71 75
23			33		
24		SSD_CLKREQ_CONN_L			
25			32		
26			31		PCIE_CLK100M_SSD_N IN 11 77
27			30		PCIE_CLK100M_SSD_P IN 11 77
28			29		
54			59		
55			60		
56			61		
57			62		
58			63		

Gumstick3 Connector

75 71 5 IN	PCIE_SSD_R2D_C_N<3>	C3710 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
75 71 5 IN	PCIE_SSD_R2D_C_P<3>	C3711 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
75 71 5 IN	PCIE_SSD_R2D_C_N<2>	C3712 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
75 71 5 IN	PCIE_SSD_R2D_C_P<2>	C3713 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
75 71 5 IN	PCIE_SSD_R2D_C_N<1>	C3714 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
75 71 5 IN	PCIE_SSD_R2D_C_P<1>	C3715 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
75 71 5 IN	PCIE_SSD_R2D_C_N<0>	C3716 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
75 71 5 IN	PCIE_SSD_R2D_C_P<0>	C3717 0.22UF	2 GND_VOID=TRUE 20% 6.3V X6S-CERM 0201

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

OOB Isolation

72 70 46 35 PP3V3 S0SW SSD

BYPASS=U3710::5 mm
C3718 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3710 08
SMC_OOB1_R2D_L IN 41
NC

33 29 20 82 72 70 68 67 66 55 52 51 49 48 47 46 45 44 35 PP3V3 S0

BYPASS=U3711::5 mm
C3719 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3711 08
SMC_OOB1_D2R_L OUT 41
NC

R3701 100K 1% 1/20W MF 201

Supervisor & CLKREQ# Isolation

Delay = ~55ms

35 46 70 72 PP3V3 S0SW SSD

R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201

P3V3SSD_VMON

CRITICAL
U3740 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND

APN 343S0511

PP3V42_G3H 19 38 39 41 42 43 44 50 56 57 65 67 70 72

C3740 0.1UF 10% 6.3V CERM-X5R 0201

SSD_RESET_L IN 20
SSD_PWR_FET_EN IN 35 66
SSD_CLKREQ_L OUT 11

R3742 100K 1% 1/20W MF 201

66 35 SSD_PWR_FET_EN = SSD_PWR_FET_EN 35 66
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN X305 PEG SYNC_DATE=02/18/2014

PAGE TITLE: SSD Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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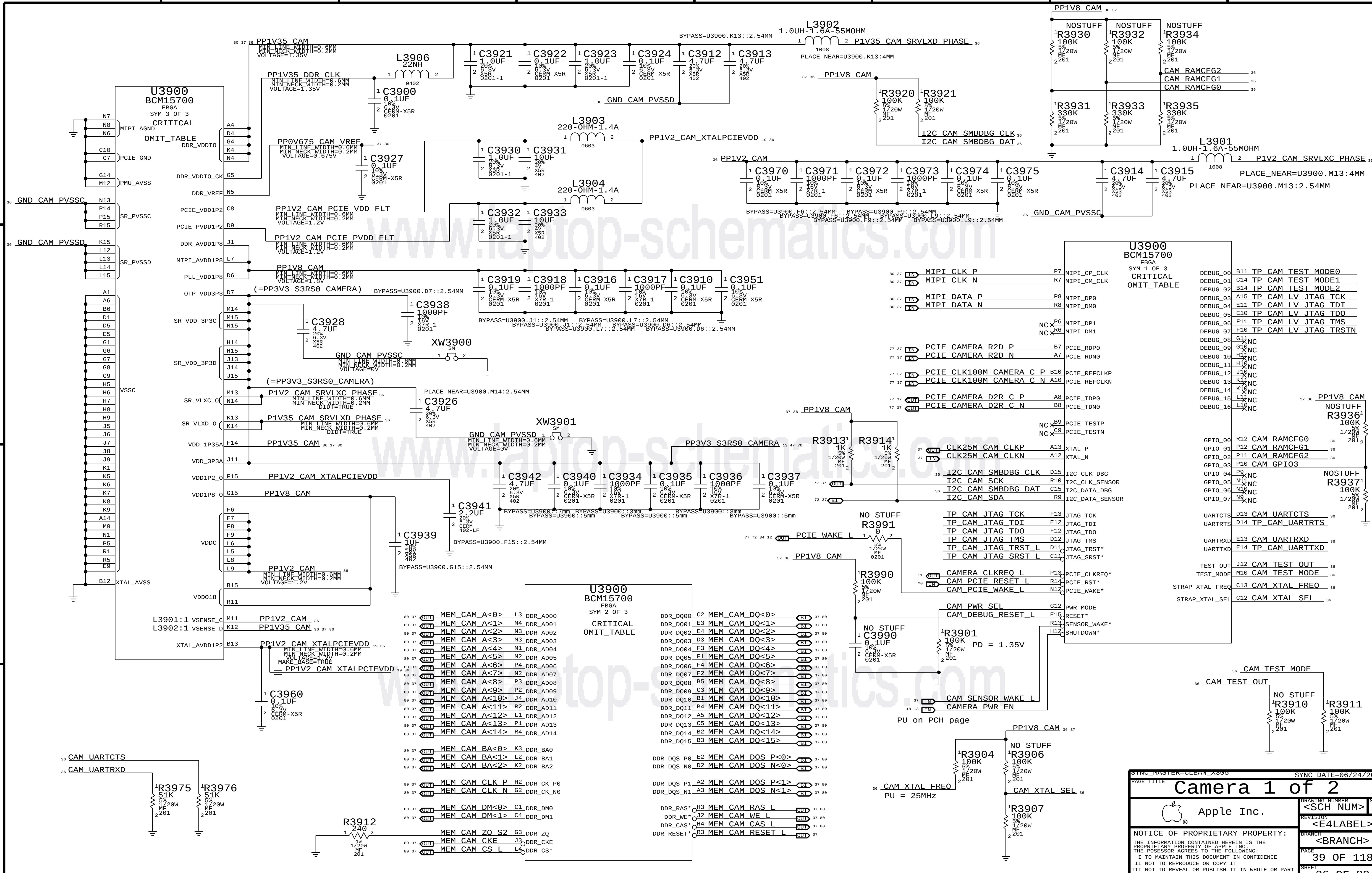

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE

Camera 1 of 2

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PP1V35_CAM

PP0V675_CAM_VREF

R4000 0 0201 5% 1/20W MF

PP0V675_MEM_CAM_VREFDQ
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.675V

PP0V675_MEM_CAM_VREFCA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.675V

R4022 1K 1% 1/20W MF 201
R4023 1K 1% 1/20W MF 201

C4010 0.1UF 10% 6.3V CERM-X5R 0201
C4011 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U4000.A1::4mm
C4002 10UF 20% 6.3V X5R 402

BYPASS=U4000.B2::4mm
C4003 10UF 20% 6.3V X5R 402
C4004 0.47UF 20% 6.3V CERM-X5R-1 201

C4005 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U4000.D2::4mm
C4006 2.2UF 20% 6.3V X5R-CERM 402
C4007 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U4000.K2::4mm
C4008 2.2UF 20% 6.3V X5R-CERM 402
C4009 0.1UF 10% 6.3V CERM-X5R 0201

BYPASS=U4000.H9::4mm
BYPASS=U4000.R9::4mm

R4002 1K 5% 1/20W MF 201

NOSTUFF
R4003 1K 5% 1/20W MF 201

U4000
4GB-DDR3-256MX16
FBGA
K4B4G1646B-HYK0

CRITICAL

OMIT_TABLE

VDDQ: A1 A8 C1 D2 E9 F1 H2 H9
VDD: B2 D9 G7 K2 K8 M1 N9 R1 R9
VREFCA: M8
VREFDQ: H1

MEM_CAM_A<0>	N3	A0	
MEM_CAM_A<1>	P7	A1	
MEM_CAM_A<2>	P3	A2	
MEM_CAM_A<3>	N2	A3	
MEM_CAM_A<4>	P8	A4	
MEM_CAM_A<5>	P2	A5	
MEM_CAM_A<6>	R8	A6	
MEM_CAM_A<7>	R2	A7	
MEM_CAM_A<8>	T8	A8	
MEM_CAM_A<9>	R3	A9	
MEM_CAM_A<10>	L7	A10/AP	
MEM_CAM_A<11>	R7	A11	
MEM_CAM_A<12>	N7	A12/BC*	
MEM_CAM_A<13>	T3	A13	
MEM_CAM_A<14>	T7	A14	
MEM_CAM_BA<0>	M2	BA0	
MEM_CAM_BA<1>	N8	BA1	
MEM_CAM_BA<2>	M3	BA2	
MEM_CAM_RAS_L	J3	RAS*	
MEM_CAM_CAS_L	K3	CAS*	
MEM_CAM_WE_L	L3	WE*	
MEM_CAM_CLK_P	J7	CK	
MEM_CAM_CLK_N	K7	CK*	
MEM_CAM_CKE	K9	CKE	
MEM_CAM_CS_L	L2	CS*	
MEM_CAM_ODT	K1	ODT	
MEM_CAM_ZQ_DDR	L8	ZQ	
MEM_CAM_RESET_L	T2	RESET*	

NC: J1 J9 L1 L9 M7

DQL0	E3	MEM_CAM_DQ<0>	B1
DQL1	F7	MEM_CAM_DQ<1>	B1
DQL2	F2	MEM_CAM_DQ<2>	B1
DQL3	F8	MEM_CAM_DQ<3>	B1
DQL4	H3	MEM_CAM_DQ<4>	B1
DQL5	H8	MEM_CAM_DQ<5>	B1
DQL6	G2	MEM_CAM_DQ<6>	B1
DQL7	H7	MEM_CAM_DQ<7>	B1
DQSL	F3	MEM_CAM_DQS_P<0>	B1
DQSL*	G3	MEM_CAM_DQS_N<0>	B1
DQSU	C7	MEM_CAM_DQS_P<1>	B1
DQSU*	B7	MEM_CAM_DQS_N<1>	B1
DQU0	D7	MEM_CAM_DQ<8>	B1
DQU1	C3	MEM_CAM_DQ<9>	B1
DQU2	C8	MEM_CAM_DQ<10>	B1
DQU3	C2	MEM_CAM_DQ<11>	B1
DQU4	A7	MEM_CAM_DQ<12>	B1
DQU5	A2	MEM_CAM_DQ<13>	B1
DQU6	B8	MEM_CAM_DQ<14>	B1
DQU7	A3	MEM_CAM_DQ<15>	B1
DML	E7	MEM_CAM_DM<0>	IN
DMU	D3	MEM_CAM_DM<1>	IN

VSSQ: B1 B9 D1 D8 E2 E8 F9 G1 G9
VSS: A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9

R4020 84.5 1% 1/20W MF 201

NO STUFF
R4021 82 1% 1/20W MF 201

MEM_CAM_CKE_R

NO STUFF
C4026 100PF 5% 25V C0G 0201

R4004 240 1% 1/20W MF 201

PP1V8_CAM

R4005 100K 5% 1/20W MF 201

CAM_WAKE:YES
R4030 0 0201 5% 1/20W MF

CAM_SENSOR_WAKE_L_CONN → CAM_SENSOR_WAKE_L

CAM_WAKE:NO
R4031 0 1/20W 5% MF 0201

PCIE_CAMERA_R2D_C_P	C4033 0.1UF	PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_C_N	C4032 0.1UF	PCIE_CAMERA_R2D_N
PCIE_CAMERA_D2R_C_P	C4031 0.1UF	PCIE_CAMERA_D2R_P
PCIE_CAMERA_D2R_C_N	C4030 0.1UF	PCIE_CAMERA_D2R_N
PCIE_CLK100M_CAMERA_P	C4061 0.1UF	PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_N	C4062 0.1UF	PCIE_CLK100M_CAMERA_C_N

(10% 16V X5R-CERM 0201)

remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR

CRITICAL
J4002
CCR20-AK7100-1
F-RT-SM

1		
2	MIPI_CLK_CONN_N	72
3	MIPI_CLK_CONN_P	72
4	CAM_SENSOR_WAKE_L_CONN	37 72
5	MIPI_DATA_CONN_N	72
6	MIPI_DATA_CONN_P	72
7		
8	SMBUS_SMC_0_S0_SDA	41 44 48 68 71 72 81
9	SMBUS_SMC_0_S0_SCL	41 44 48 68 71 72 81
10	I2C_CAM_SCK	36 72
11	I2C_CAM_SDA	36 72
12	PP5V_S3RS0_ALSCAM_F	72
13		
14		

518S0892

ALS

CRITICAL
L4009
90-OHM-0.1A-0.7-2GHZ
TAM0605

MIPI_CLK_N
MIPI_CLK_P
PLACE_NEAR=J4002.2:2.54MM

CRITICAL
L4007
90-OHM-0.1A-0.7-2GHZ
TAM0605

MIPI_DATA_N
MIPI_DATA_P
PLACE_NEAR=J4002.5:2.54MM

L4010
FERR-120-OHM-1.5A
0402-LF

PP5V_S0

C4013 0.1UF 20% 10V CERM 0201
C4012 12PF 5% 50V NP0-C0G 0201 25V
PLACE_NEAR=J4002.12:2mm

NOSTUFF
L4011
FERR-120-OHM-1.5A
0402-LF

PP5V_S3

77.2 mA nominal max
96.2 mA peak

SYSCLK_CLK25M_CAMERA

NO STUFF
C4015 12PF 5% 25V CERM 0201

CLK25M_CAM_XTALP

NO STUFF
R4007 0 0201 5% 1/20W MF

CLK25M_CAM_XTALP_R

CRITICAL
Y4000
SM-3.2X2.5MM
25.000MHZ-12PF-20PPM
NO STUFF

NO STUFF
R4012 1M 1% 1/20W MF 201

R4008 0 0201 5% 1/20W MF

CLK25M_CAM_CLKP

R4009 0 5% 1/20W MF 0201
NO STUFF

R4010 0 5% 1/20W MF 0201
NO STUFF

CLK25M_CAM_XTALN → CLK25M_CAM_CLKN

C4016 100PF 5% 25V C0G 0201

C4014 12PF 5% 25V CERM 0201
NO STUFF

NOTE: TBD PPM crystal required

SYNC_MASTER=CLEAN_X305
SYNC_DATE=06/24/2014

PAGE TITLE: Camera 2 of 2

Apple Inc.

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SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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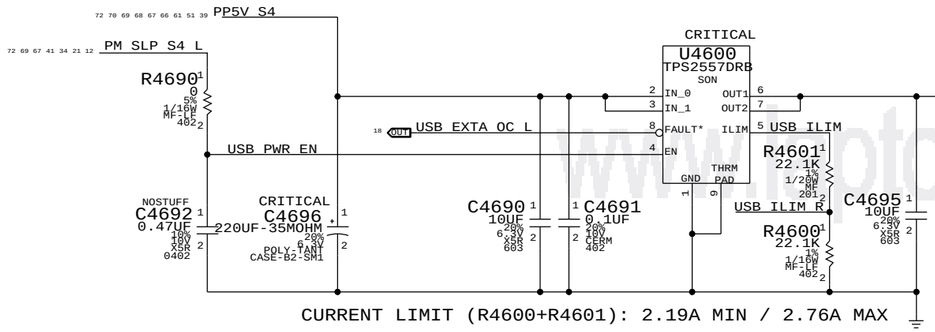
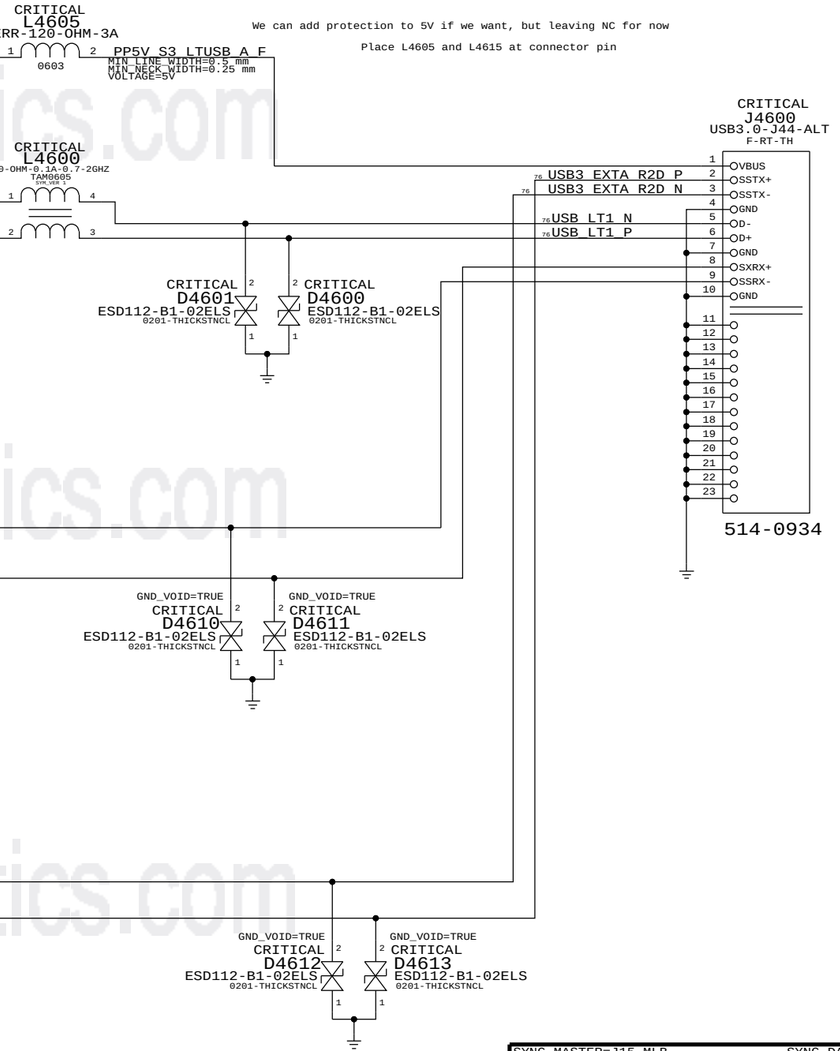
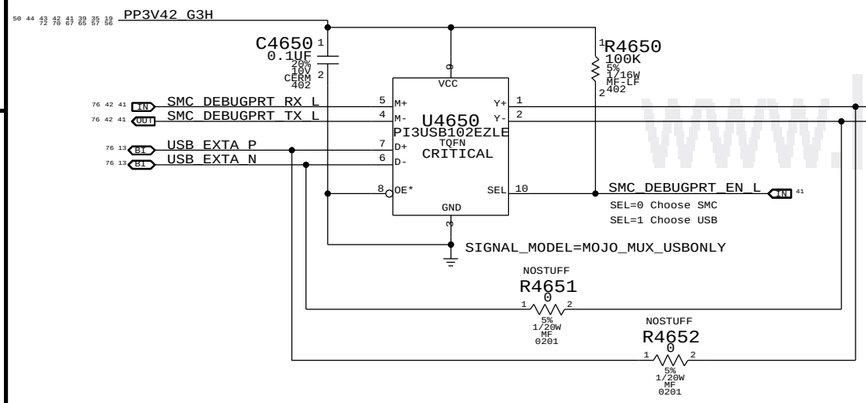
USB Port Power Switch

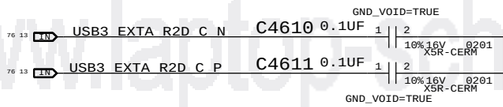


Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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IPD CONNECTOR

CRITICAL
J4801
502250-8041
F-RT-SM

TPAD_SPI_MOSI
TPAD_SPI_MISO
TPAD_SPI_SCLK
TPAD_SPI_INT_L
I2C_IOXP_SDA
I2C_IOXP_SCL
USB_TPAD_N
USB_TPAD_P
PP3V3_S4
TPAD_SPI_CS_L
TPAD_SPI_BUS_EN
TPAD_NC4
IOXP2_INT_L
TPAD_NC3
SMBUS_SMC_2_S3_SDA
TPAD_VBUS_EN
GND_ACTUATOR
PPVIN_S4_TPAD
SMC_PME_S4_WAKE_L
SMBUS_SMC_2_S3_SCL
TPAD_ACTUATOR_THRMTRIP_L
SMC_ACTUATOR_EN_R_L

R4893 100K 5% 1/20W MF 0201 — NOSTUFF
R4808 0 5% 1/20W MF 0201 — SMC_ACTUATOR_EN_L
C4801 100PF 5% 25V C0G 0201 — SMC_LID
C4808 1.0UF 10% 35V CERM-X5R 0402 — PLACE_NEAR=J4801.35:5mm
C4806 0.1UF 10% 35V CER-X5R 0201 — PLACE_NEAR=J4801.35:5mm
C4807 0.1UF 10% 35V CER-X5R 0201 — PLACE_NEAR=J4801.35:5mm
GND_ACTUATOR

R4890 0 5% 1/10W MF-LF 402 — NOSTUFF
R4891 0 5% 1/10W MF-LF 402 — NOSTUFF
PLACE_NEAR=C4809.1:2MM
R4809 0 5% 1/20W MF 0201 — TPAD_VBUS_EN_R
C4809 100PF 5% 25V C0G 0201 — NOSTUFF
PLACE_NEAR=J4801.26:2MM
XW4801 SM
PLACE_NEAR=J4801:3MM
PPVIN_S4_TPAD
L4803 FERR-120-OHM-1.5A 0402-LF
PP5V_S4_TPAD_F — MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5V
PP5V_S4
C4803 0.1UF 20% 10V CERM 402

Keyboard Connector

518S0752
CRITICAL
J4813

PP3V3_S4
PP3V42_G3H
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
F-RT-SM
FF14A-30C-R11DL-B-3H

R4814 113 1% 1/10W MF-LF 402 — WS_KBD15_C
R4815 0 5% 1/10W MF-LF 402 — WS_KBD16N
R4810 1K 5% 1/10W MF-LF 402 — SMC_ONOFF_L
C4810 0.1UF 20% 10V CERM 402

SMC Manual Reset & Isolation

LEFT SHIFT, OPTION & CONTROL KEYS COMBINED WITH POWER BUTTON CAUSE SMC RESET# ASSERTION.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

PP3V42_G3H
C4850 0.1UF 10% 10V X7R-CERM 0402 — BYPASS=U4850.10:5:5 mm
U4850
SLG4AP4103
TQFN
PP3V3_S4 — OE (IPD)
WS_LEFT_SHIFT_KBD — IN_1 (IPD)
WS_LEFT_OPTION_KBD — IN_2 (IPD)
WS_CONTROL_KBD — IN_3 (IPD)
OUT_1 WS_LEFT_SHIFT_KEY
OUT_2 WS_LEFT_OPTION_KEY
OUT_3 WS_CONTROL_KEY
OUT_ALL# SMC_TPAD_RST_L
Pull-up in U5110.
GND PAD THRM PAD

IO EXPANDER / KEYBOARD INTERFACE

PP3V3_S4
R4831 10K 5% 1/20W MF 201 — IOXP2_INT_L
R4830 100K 5% 1/20W MF 201 — IOXP2_RESET_L
C4830 1UF 10% 6.3V CERM 402 — BYPASS=U4830.B4:E2:5MM
C4831 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=U4830.B3:E2:2MM
C4832 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=U4830.B4:E2:2MM
U4830
PCAL6416A
VFBGA
INT* ADDR SCL SDA RESET*
VCCI VCCP
P0_0 WS_KBD5
P0_1 WS_KBD6
P0_2 WS_KBD7
P0_3 WS_KBD9
P0_4 WS_KBD12
P0_5 WS_KBD8
P0_6 WS_KBD17
P0_7 WS_KBD18
P1_0 WS_KBD19
P1_1 WS_KBD10
P1_2 WS_KBD14
P1_3 WS_KBD13
P1_4 WS_KBD11
P1_5
P1_6 WS_CONTROL_KEY
P1_7 WS_LEFT_OPTION_KEY
WS_LEFT_SHIFT_KEY
GND E2
311S0597
(Write: 0x42 Read: 0x43)
C4834 0.01UF 10% 16V X5R-CERM 0201 — NOSTUFF

PP3V3_S4
R4802 10K 5% 1/20W MF 201
R4801 10K 5% 1/20W MF 201
R4852 10K 5% 1/20W MF 201
R4853 10K 5% 1/20W MF 201
R4854 10K 5% 1/20W MF 201
R4855 10K 5% 1/20W MF 201
R4856 10K 5% 1/20W MF 201
R4857 10K 5% 1/20W MF 201

PP3V3_S4
R4858 10K 5% 1/20W MF 201
R4859 10K 5% 1/20W MF 201
R4860 10K 5% 1/20W MF 201
R4861 10K 5% 1/20W MF 201
R4862 10K 5% 1/20W MF 201

PP3V3_S4
R4821 10K 5% 1/20W MF 201
R4820 100K 5% 1/20W MF 201 — BYPASS=U4820.B4:E2:5MM
C4820 1UF 10% 6.3V CERM 402 — BYPASS=U4820.B4:E2:5MM
C4821 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=U4820.B3:E2:2MM
C4822 0.1UF 10% 6.3V CERM-X5R 0201 — BYPASS=U4820.B4:E2:2MM
R4822 2.0K 5% 1/20W MF 201
R4823 2.0K 5% 1/20W MF 201
U4820
PCAL6416A
VFBGA
IOXP1_INT_L
I2C_IOXP_SCL
I2C_IOXP_SDA
IOXP1_RESET_L
P0_0 WS_KBD23
P0_1 WS_KBD2
P0_2 WS_KBD1
P0_3 WS_KBD3
P0_4 WS_KBD4
P0_5 WS_KBD20
P0_6 WS_KBD22
P0_7 WS_KBD21
P1_0 TP_IOXP1_0
P1_1 TP_IOXP1_1
P1_2 TP_IOXP1_2
P1_3 TP_IOXP1_3
P1_4 TP_IOXP1_4
P1_5 IOXP1_DEBUG
P1_6 WS_KBD16N
P1_7 IOXP1_LED_DRV
VCCI VCCP
GND E2
311S0597
(Write: 0x40 Read: 0x41)
C4824 0.01UF 10% 16V X5R-CERM 0201 — NOSTUFF
R4824 0 5% 1/20W MF 0201 — NOSTUFF
SMC_ONOFF_L
Q4840 DMN32D2LFB4 DFN1006H4-3 SYM VER 2
WS_KBD15_C
R4840 100K 1% 1/16W MF-LF 402

SYNC_MASTER=CLEAN_X305_PEG
SYNC_DATE=02/18/2014
PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
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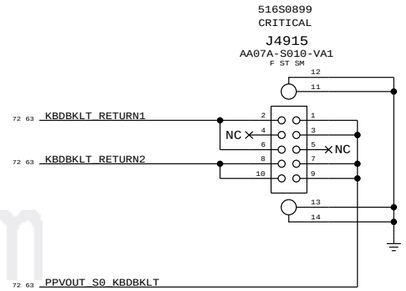
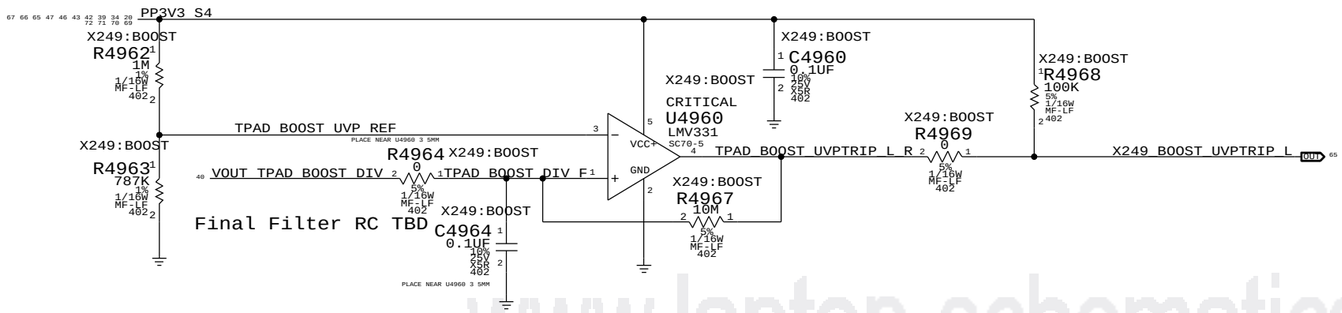
Keyboard Backlight Connector

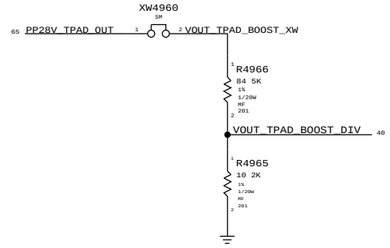


X249 BOOST UVP TRIP



Trip set at 13.5V (divider set for 1.45V)

X249 Boost Voltage Sense



SYNC_MASTER=CLEAN_X305	SYNC_DATE=05/30/2014
PAGE TITLE	KEYBOARD/TRACKPAD (2 OF 2)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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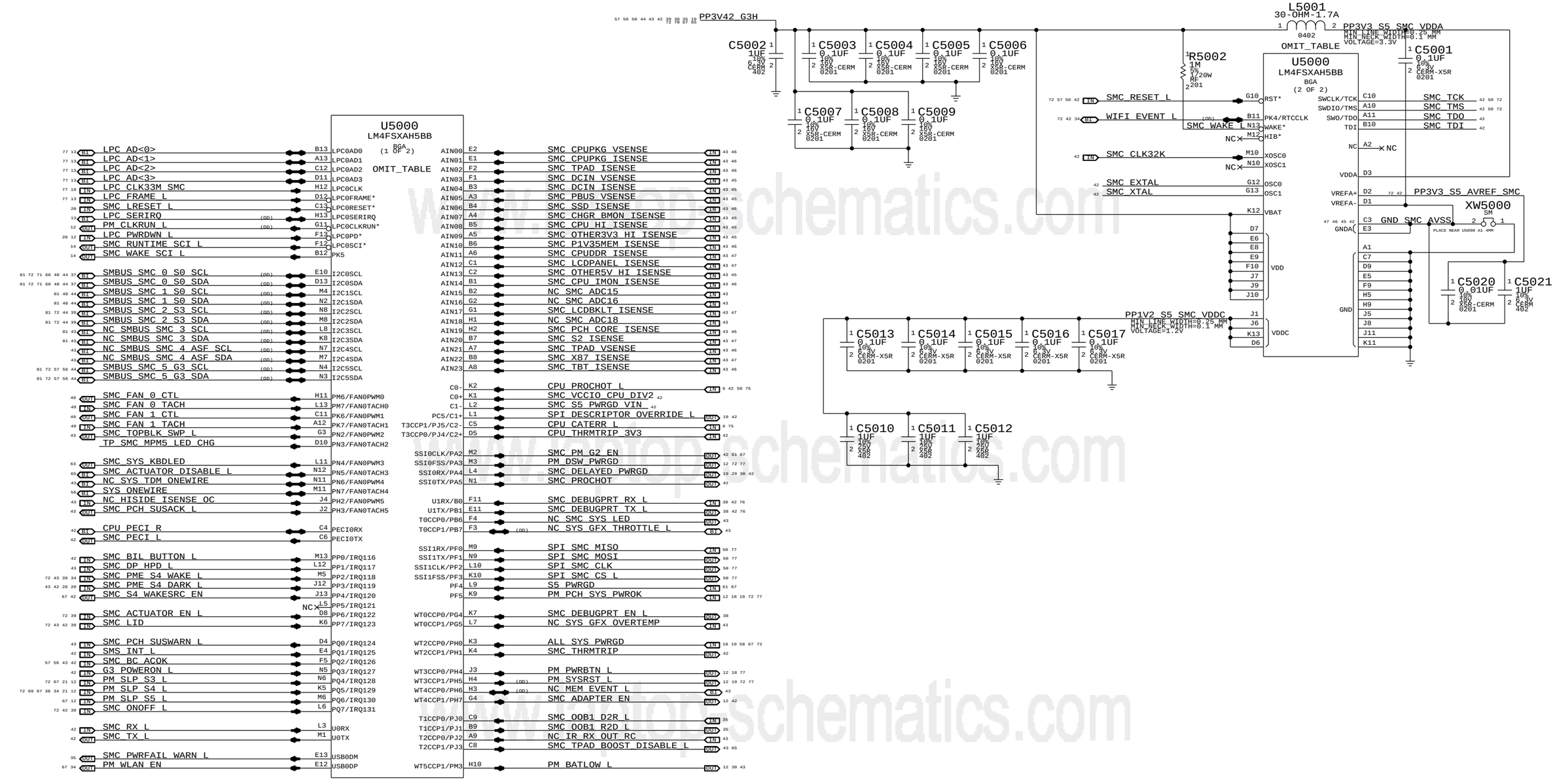
NOTE Unused pins have "SMC Pxx" names Unused
pins designed as outputs can be left floating
those designated as inputs require pull ups



NOTE SMS Interrupt can be active high or low rename net accordingly
If SMS interrupt is not used pull up to SMC rail

SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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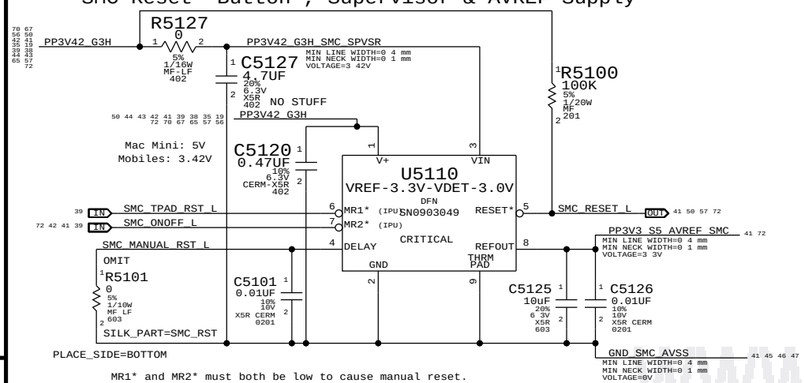
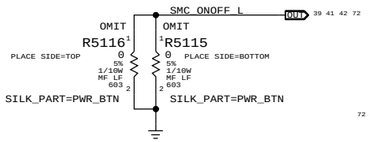
SMC Reset "Button", Supervisor & AVREF Supply



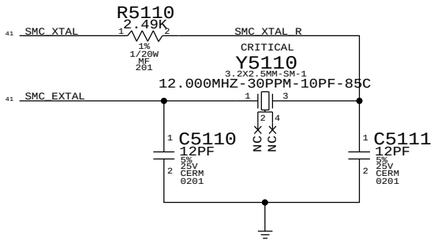
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

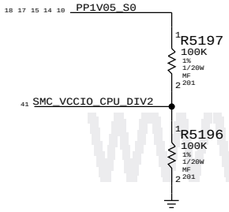
Debug Power "Buttons"



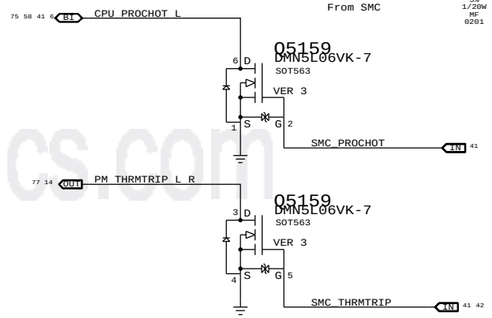
SMC Crystal Circuit

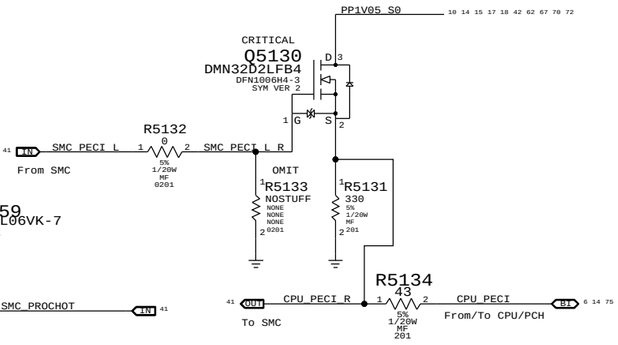


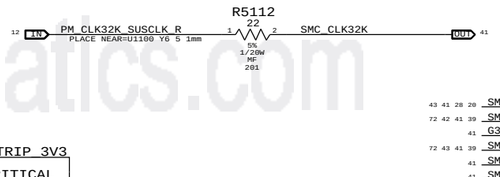
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

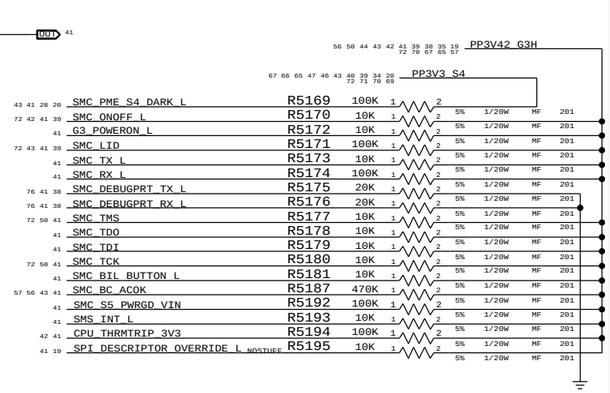


SMC12 PECI SUPPORT









SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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SMC_BC_ACOK — SMC_BC_ACOK (MAKE_BASE=TRUE)
NC_HISIDE_ISENSE_OC — NC_HISIDE_ISENSE_OC (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_CPUPKG_VSENSE — SMC_CPUPKG_VSENSE (MAKE_BASE=TRUE)
SMC_CPUPKG_ISENSE — SMC_CPUPKG_ISENSE (MAKE_BASE=TRUE)
SMC_TPAD_ISENSE — SMC_TPAD_ISENSE (MAKE_BASE=TRUE)
SMC_DCIN_VSENSE — SMC_DCIN_VSENSE (MAKE_BASE=TRUE)
SMC_DCIN_ISENSE — SMC_DCIN_ISENSE (MAKE_BASE=TRUE)
SMC_PBUS_VSENSE — SMC_PBUS_VSENSE (MAKE_BASE=TRUE)
SMC_SSD_ISENSE — SMC_SSD_ISENSE (MAKE_BASE=TRUE)
SMC_CHGR_BMON_ISENSE — SMC_CHGR_BMON_ISENSE (MAKE_BASE=TRUE)
SMC_CPU_HI_ISENSE — SMC_CPU_HI_ISENSE (MAKE_BASE=TRUE)
SMC_OTHER3V3_HI_ISENSE — SMC_OTHER3V3_HI_ISENSE (MAKE_BASE=TRUE)
SMC_P1V35MEM_ISENSE — SMC_P1V35MEM_ISENSE (MAKE_BASE=TRUE)
SMC_CPUDDR_ISENSE — SMC_CPUDDR_ISENSE (MAKE_BASE=TRUE)
SMC_LCDPANEL_ISENSE — SMC_LCDPANEL_ISENSE (MAKE_BASE=TRUE)
SMC_OTHER5V_HI_ISENSE — SMC_OTHER5V_HI_ISENSE (MAKE_BASE=TRUE)
SMC_CPU_IMON_ISENSE — SMC_CPU_IMON_ISENSE (MAKE_BASE=TRUE)
NC_SMC_ADC15 — NC_SMC_ADC15 (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMC_ADC16 — NC_SMC_ADC16 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_LCDBKLT_ISENSE — SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE)
NC_SMC_ADC18 — NC_SMC_ADC18 (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_PCH_CORE_ISENSE — SMC_PCH_CORE_ISENSE (MAKE_BASE=TRUE)
SMC_S2_ISENSE — SMC_S2_ISENSE (MAKE_BASE=TRUE)
SMC_TPAD_VSENSE — SMC_TPAD_VSENSE (MAKE_BASE=TRUE)
SMC_X87_ISENSE — SMC_X87_ISENSE (MAKE_BASE=TRUE)
SMC_TBT_ISENSE — SMC_TBT_ISENSE (MAKE_BASE=TRUE)
NC_SMBUS_SMC_4_ASF_SCL — NC_SMBUS_SMC_4_ASF_SCL (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_4_ASF_SDA — NC_SMBUS_SMC_4_ASF_SDA (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_3_SCL — NC_SMBUS_SMC_3_SCL (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SMBUS_SMC_3_SDA — NC_SMBUS_SMC_3_SDA (MAKE_BASE=TRUE NO_TEST=TRUE)
SMC_TPAD_BOOST_DISABLE — SMC_TPAD_BOOST_DISABLE_L (MAKE_BASE=TRUE)
SMC_PME_S4_DARK_L (MAKE_BASE=TRUE) — SMC_PME_S4_DARK_L
SMC_PME_S4_DARK_L

NC_SMC_SYS_LED — NC_SMC_SYS_LED (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_MEM_EVENT_L — NC_MEM_EVENT_L (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_IR_RX_OUT_RC — NC_IR_RX_OUT_RC (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_TDM_ONEWIRE — NC_SYS_TDM_ONEWIRE (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_GFX_THROTTLE_L — NC_SYS_GFX_THROTTLE_L (MAKE_BASE=TRUE NO_TEST=TRUE)
NC_SYS_GFX_OVERTEMP — NC_SYS_GFX_OVERTEMP (MAKE_BASE=TRUE NO_TEST=TRUE)

SMC_SUSACK:YES
R5230 0 5% 1/20W MF 201
SMC_PCH_SUSWARN_L (OUT) — PCH_SUSWARN_L (IN)
R5231 0 5% 1/20W MF 201
SMC_PCH_SUSACK_L (IN) — PCH_SUSACK_L (OUT)
SMC_SUSACK:YES

Spare S4 IRQ

PP3V3_S4
R5259 100K 5% 1/20W MF 201
SMC_DP_HPD_L (OUT)

Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99
SM
NC, NC, NC, NC
PP3V42_G3H
R5250 0 5% 1/20W MF 0201
SMC_LID_R — SMC_LID
C5250 0.001UF 10% 50V X7R CERM 0402

PP3V3_S4
R5282 100K 5% 1/20W MF 201
SMC_PME_S4_WAKE_L (IN) — SMC_PME_S4_WAKE_L (OUT) (MAKE_BASE=TRUE)
SMC_PME_S4_WAKE_L (IN)

R5283 1K 5% 1/20W MF 201
SMC_TOPBLK_SWP_L (IN) — PCH_STRP_TOPBLK_SWP_L (OUT)

PM_BATLOW_L (IN) — PM_BATLOW_L (OUT) (MAKE_BASE=TRUE)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

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PCH SMBus "0" Connections

PP3V3_S0

Lynx Point
U1100
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA
MAKE_BASE=TRUE

R5300 1K 5% 1/10W MF-LF 402
R5301 1K 5% 1/16W ME-LF 402

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

XDP Connectors
J1800 & J1850
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

SMC "0" SMBus Connections

PP3V3_S0

SMC
U5000
(MASTER)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5350 2.0K 5% 1/10W MF-LF 402
R5351 2.0K 5% 1/16W ME-LF 402

L&R Fin Stack Temp
EMC1412-A: U5860
(Write: 0x98 Read: 0x99)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

eDP Connector
J8300
(Write: 0x86 Read: 0x87)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

J4002
ALS
(Write 0x72 Read 0x73)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

SMC "5" SMBUS CONNECTIONS

PP3V42_G3H

SMC
U5000
(MASTER)
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
MAKE_BASE=TRUE

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

Battery Charger
ISL6258 - U7100
(Write: 0x12 Read: 0x13)
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA

Battery
J7050
(Write: 0x16 Read: 0x17)
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA

SMC "2" SMBUS CONNECTIONS

NOTE SMC_RMT bus remains powered and may be active in S3 state

PP3V3_S3

SMC
U5000
(MASTER)
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
MAKE_BASE=TRUE

R5370 1K 5% 1/20W MF 201
R5371 1K 5% 1/20W MF 201

Trackpad
J4801
(Write: 0x98 Read: 0x99)
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA

SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

PCH "SMLink 0" Connections

PP3V3_S0

Lynx Point
U1100
(MASTER)
SML_PCH_0_CLK
SML_PCH_0_DATA
MAKE_BASE=TRUE

R5310 8.2K 5% 1/10W MF-LF 402
R5311 8.2K 5% 1/16W ME-LF 402

SMC "1" SMBUS CONNECTIONS

PP3V3_S0

SMC
U5000
(MASTER)
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
MAKE_BASE=TRUE

R5360 1K 5% 1/20W MF 201
R5361 1K 5% 1/20W MF 201

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5870
(Write: 0x98 Read: 0x99)
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA

X87 TEMP
TMP105: U5823
(WRITE: 0x92 READ: 0x93)
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA

PCH "SMLink 1" Connections

PP3V3_S0

Lynx Point
U1100
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA
MAKE_BASE=TRUE

NO STUFF
R5320 8.2K 5% 1/20W MF 201
NO STUFF
R5321 8.2K 5% 1/20W MF 201

R5323 0 5% 1/20W MF 0201
R5322 0 5% 1/20W MF 0201

SMLink 1 is slave port to access PCH & CPU via PECI.

SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

PAGE TITLE: SMBus Connections

Apple Inc.

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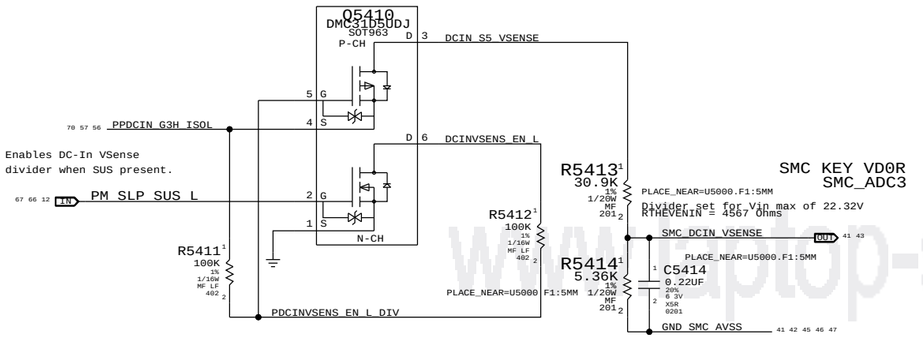
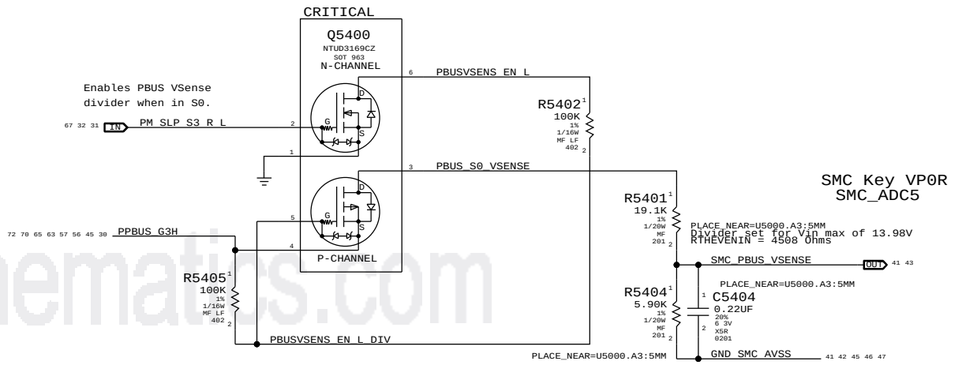
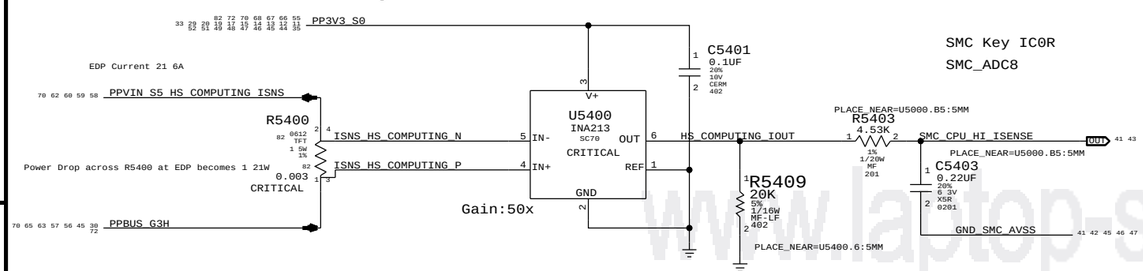
DC-In Voltage Sense Enable & Filter



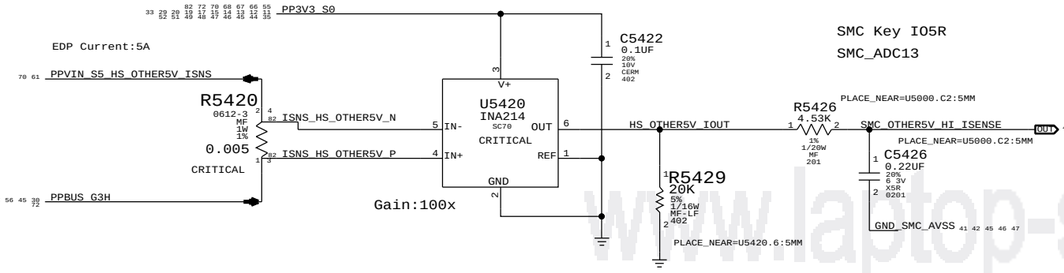
PBUS Voltage Sense Enable & Filter



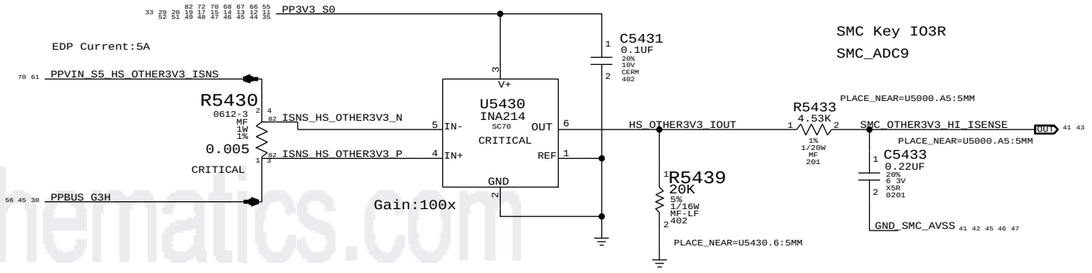
COMPUTING High Side Current Sense / Filter



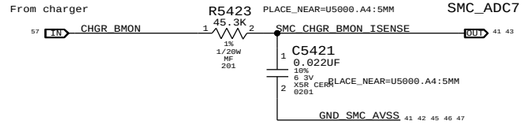
OTHERS (5V) High Side Current Sense / Filter



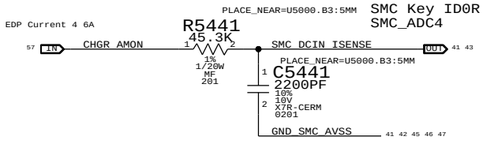
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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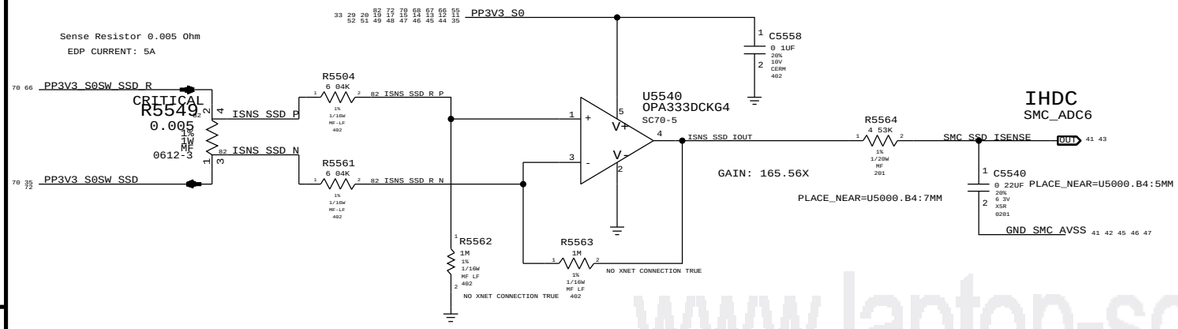
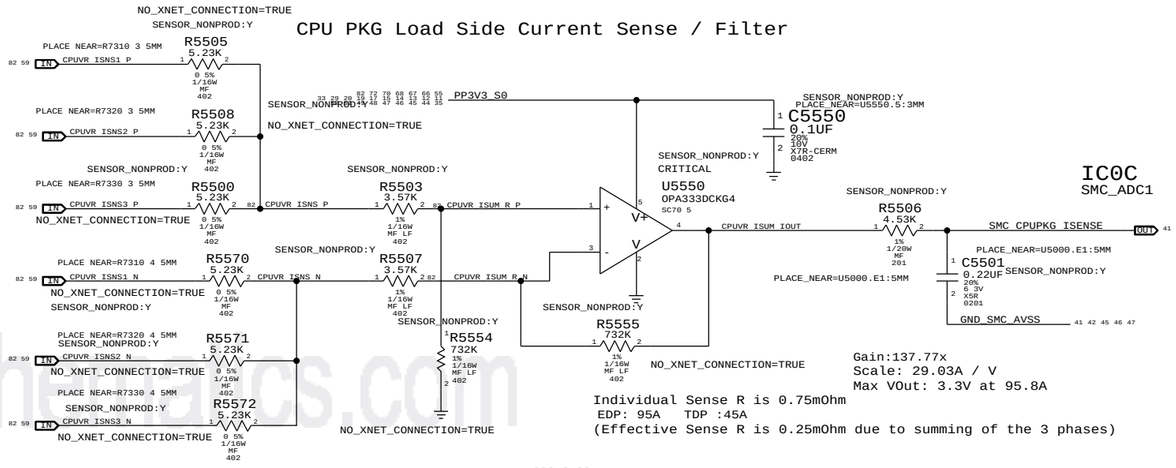
SSD CURRENT SENSE

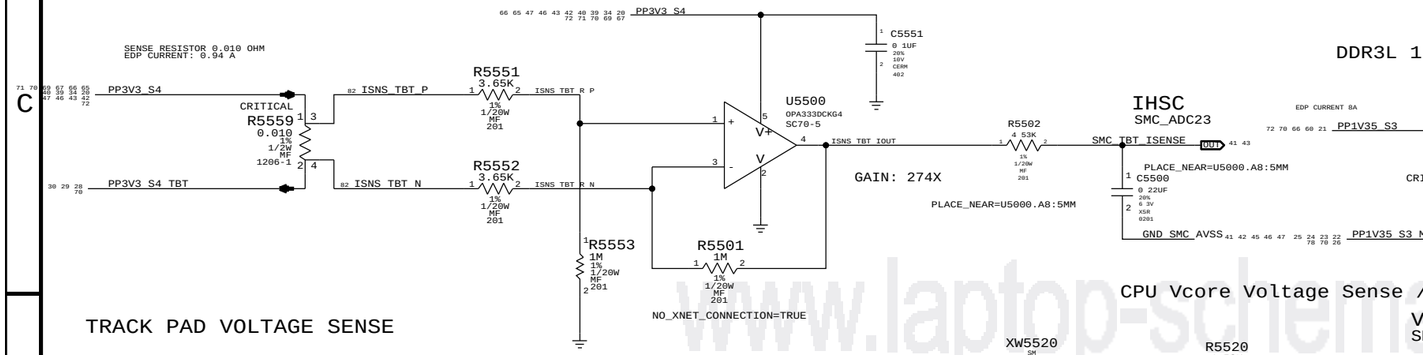


TBT Router CURRENT SENSE

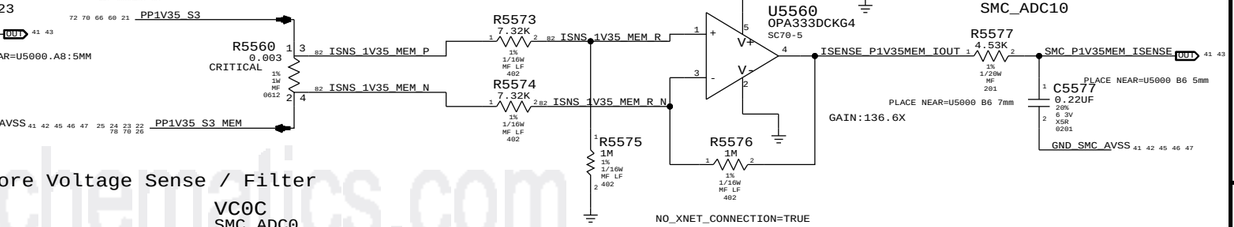
CPU PKG Load Side Current Sense / Filter



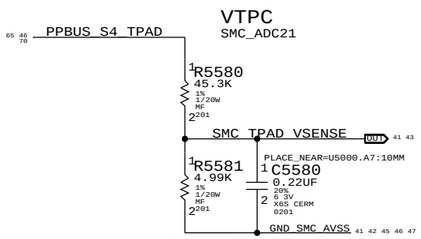
DDR3L 1.35V DRAM ONLY CURRENT SENSE / FILTER



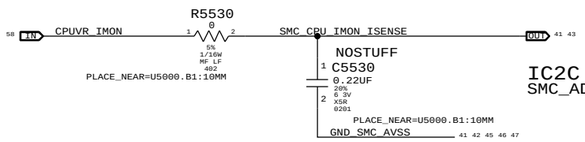
CPU Vcore Voltage Sense / Filter



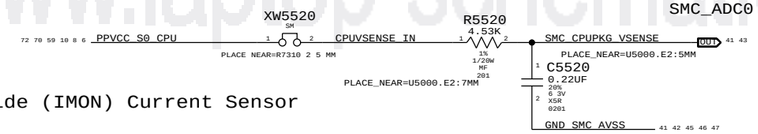
TRACK PAD VOLTAGE SENSE



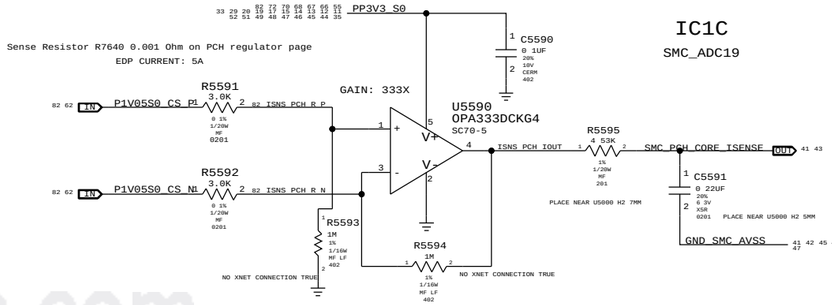
CPU Load Side (IMON) Current Sensor



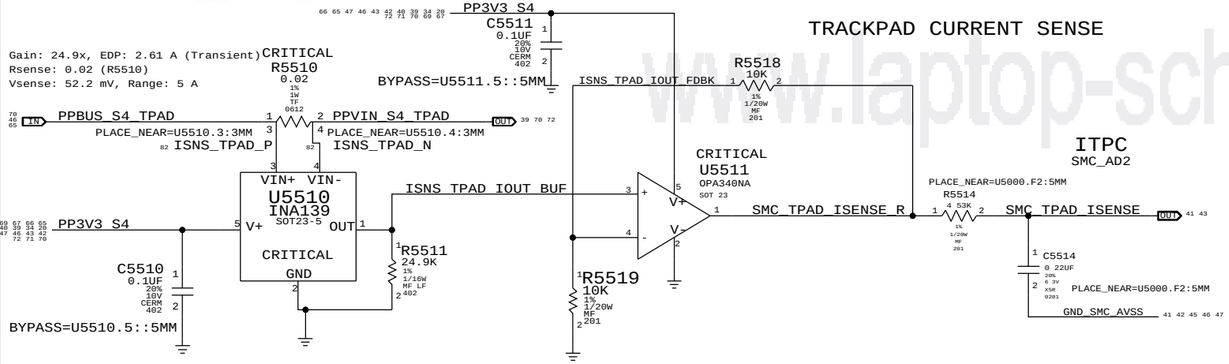
CPU Vcore Voltage Sense / Filter



PCH CORE CURRENT SENSE



TRACKPAD CURRENT SENSE



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: Load Side Voltage and Current Sensing

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DRAWING NUMBER: <SCH_NUM> SIZE: D
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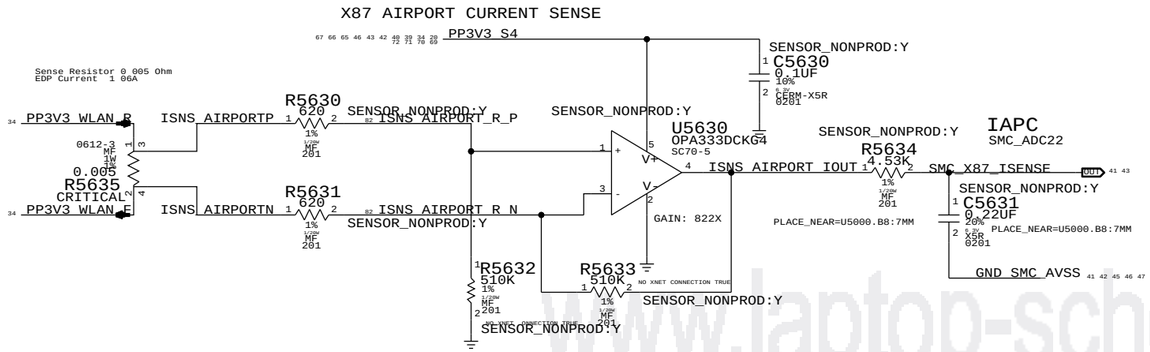
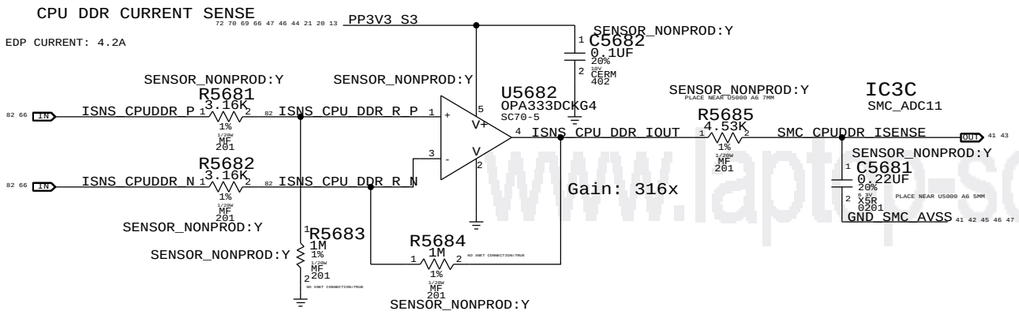
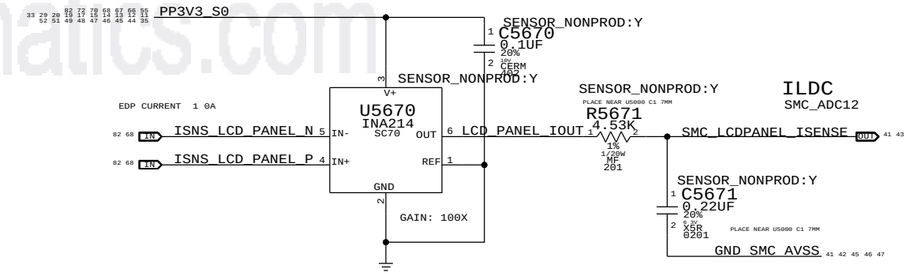
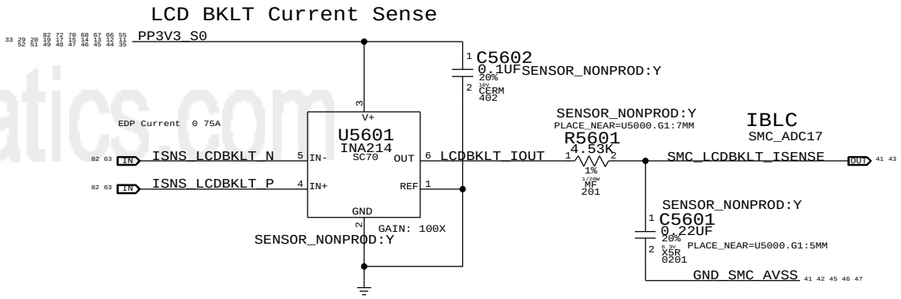
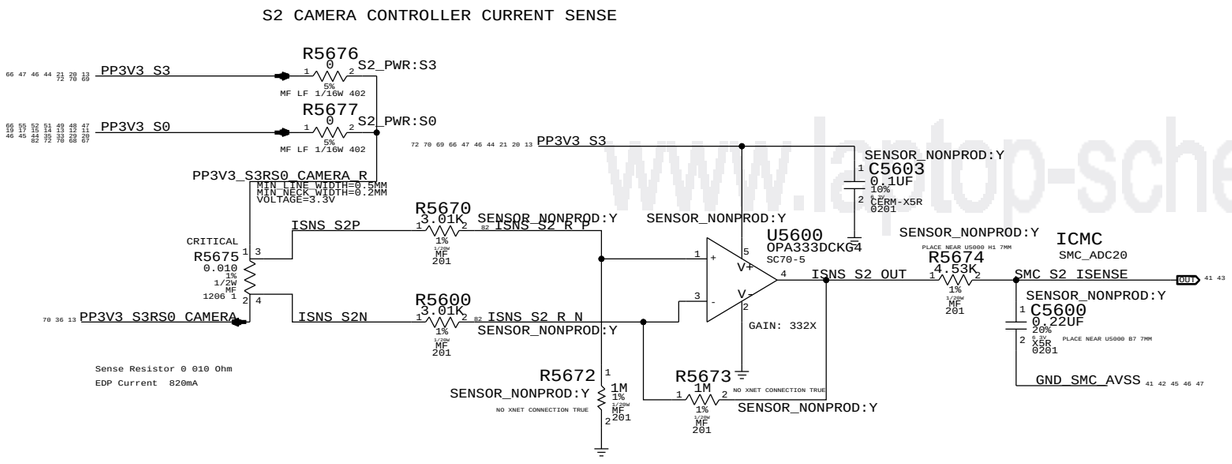


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES MTL FILM 100K 5 1/20W 0201 SMD LF	C5601 C5631 C5600 C5681 C5671		SENSOR_NONPROD:N



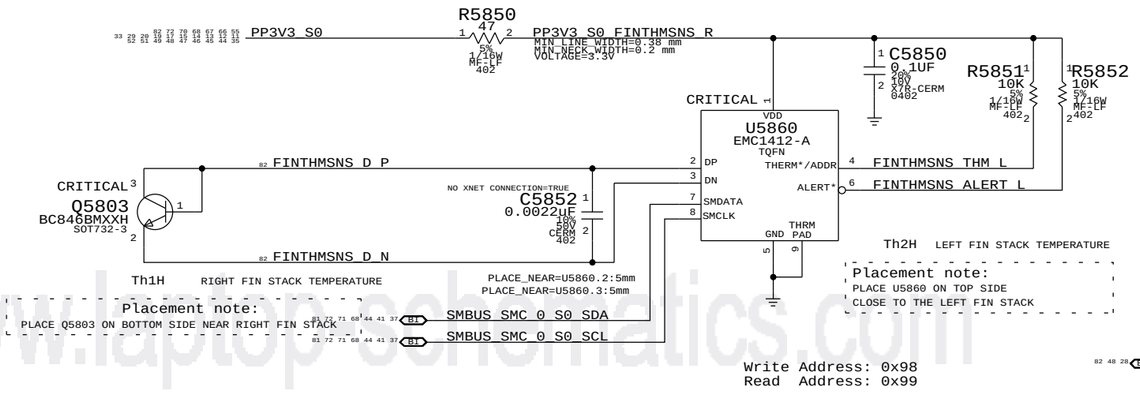




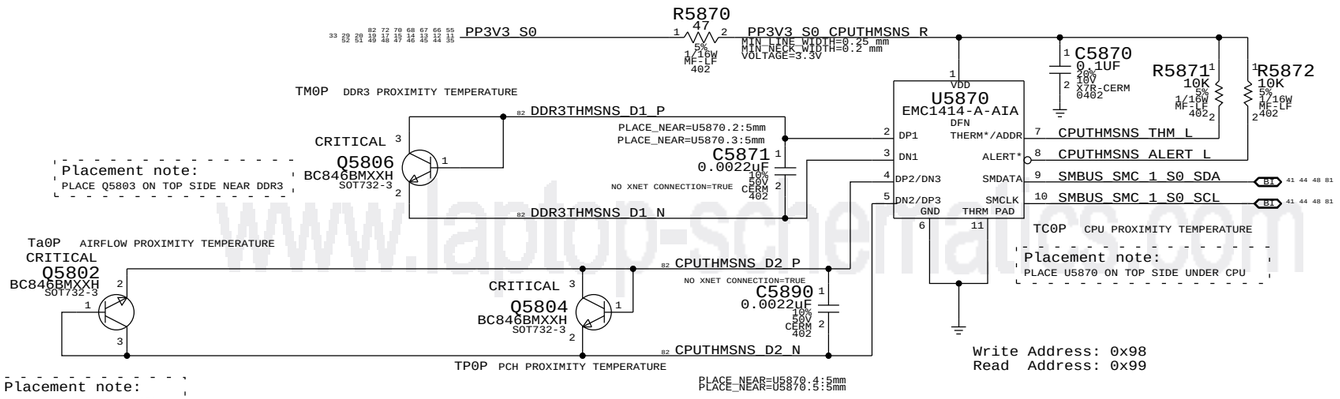


SYNC MASTER=CLEAN X305	SYNC DATE=01/14/2014
PAGE TITLE	Debug Sensors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 56 OF 118
	SHEET 47 OF 82

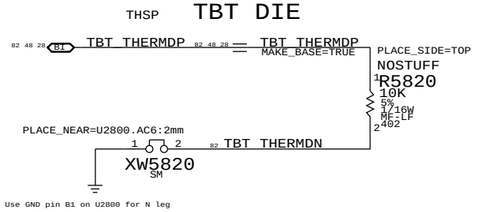
LEFT FIN STACK/RIGHT FIN STACK



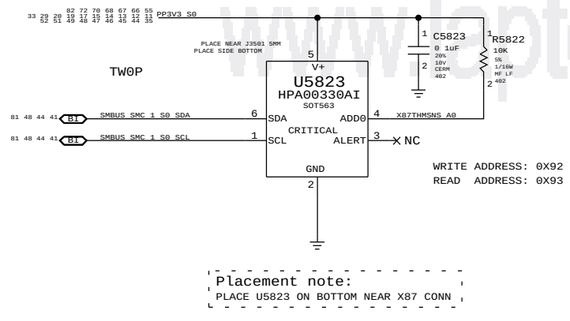
DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



TBT DIE



X87 PROXIMITY



SYNC_MASTER=CHANG J45 SYNC_DATE=11/26/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

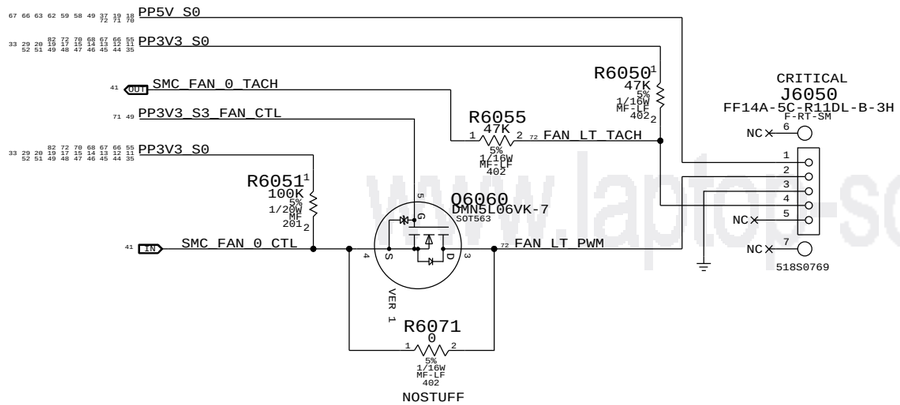
REVISION: <E4LABEL>

BRANCH: <BRANCH>

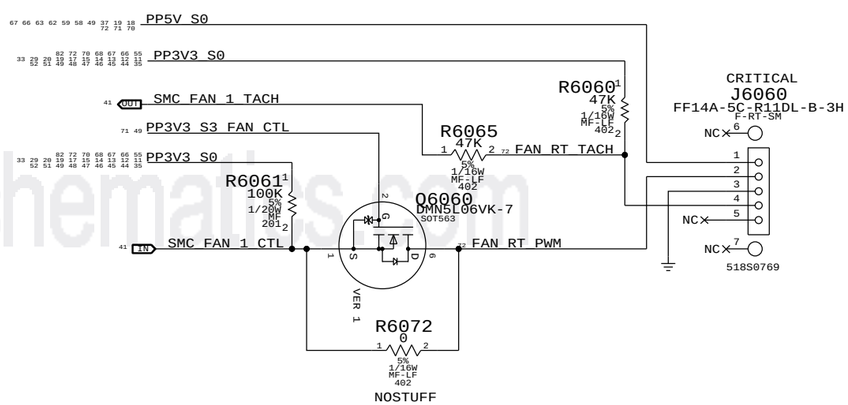
PAGE: 58 OF 118

SHEET: 48 OF 82

Left Fan



Right Fan



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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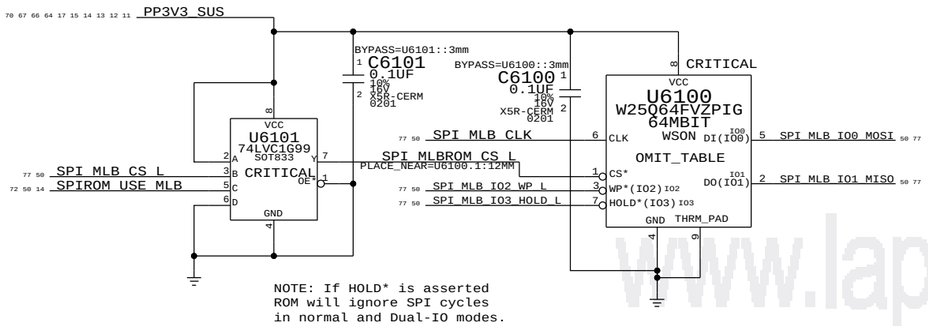
SPI ROM

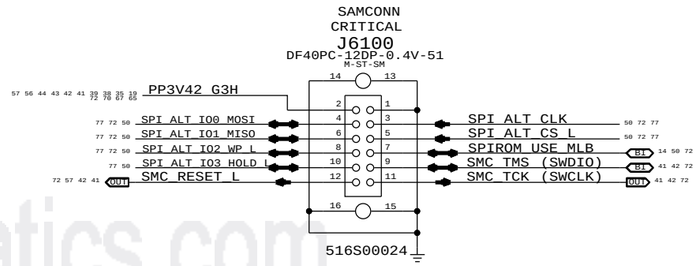
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



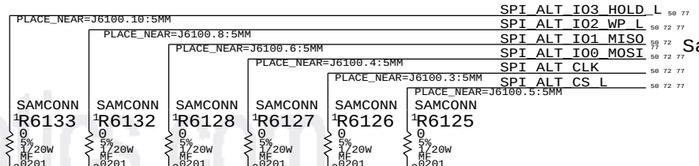
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector

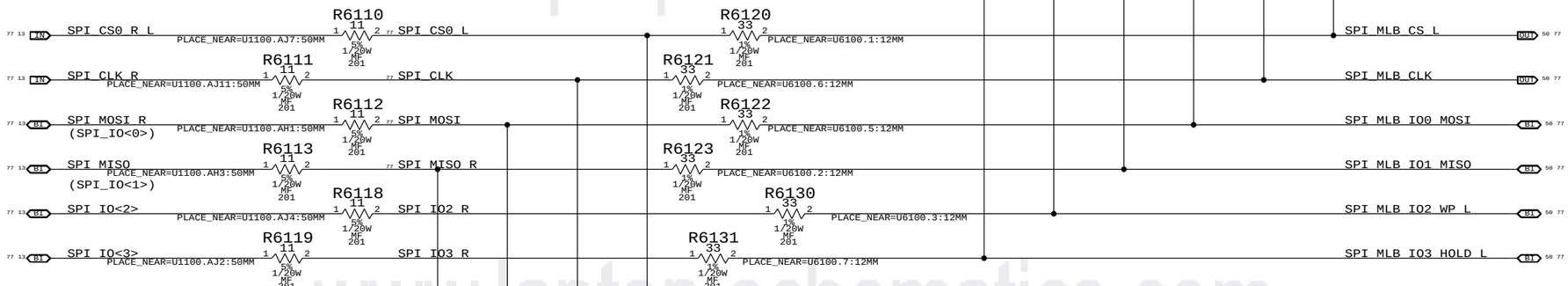


SPI Bus Series Termination



Sam Card ROM Slave

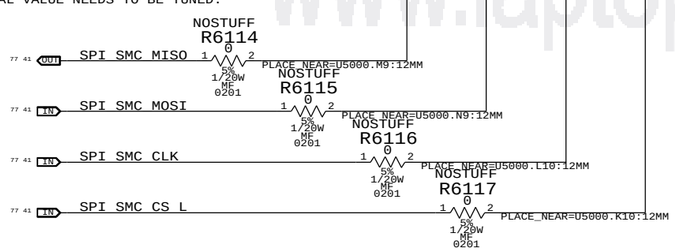
PCH Master



SPI ROM Slave

OVER/UNDER-SHOOT WAS OBSERVED ON IO2 AND IO3.
0HOM WERE ADDED FOR R6118&R6119 AS PLACEHOLDER.
FINAL VALUE NEEDS TO BE TUNED.

SMC12 Master



SYNC MASTER=CLEAN X305 PEG SYNC DATE=02/18/2014

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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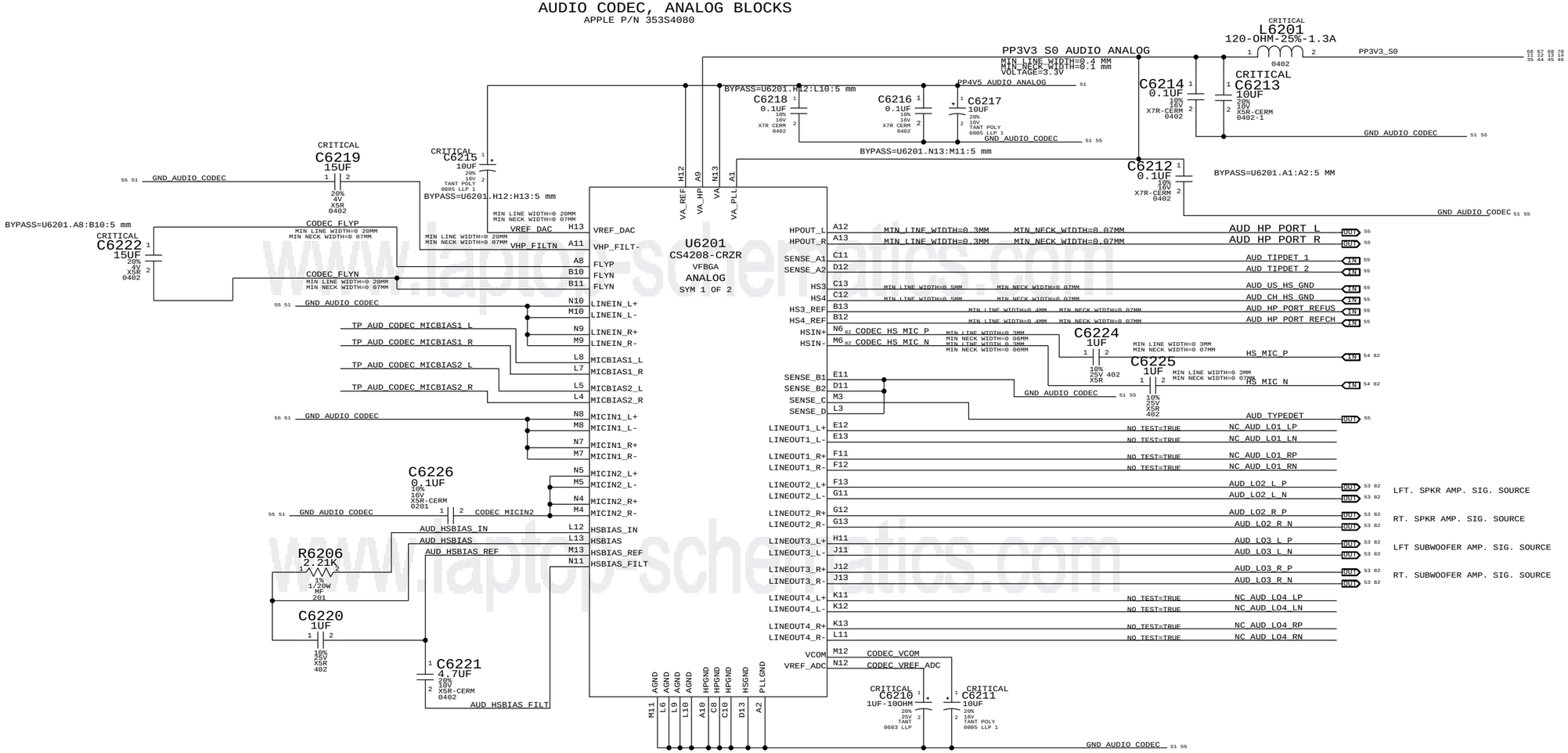
AUDIO CODEC, ANALOG BLOCKS

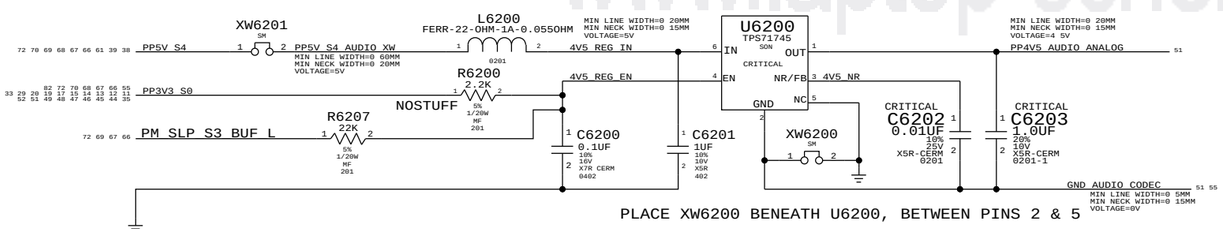
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

SYNC MASTER=JOE J45	SYNC DATE=07/30/2013
PAGE TITLE	AUDIO:CODEC, ANALOG
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.055OHM
0201

PP1V5_S0 → C6300 4.7UF 20% 4V X5R 1 402 → C6301 0.1UF 10% 10V X7R CERM 0201
PP1V5_S0_AUDIO_DIG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.07MM
VOLTAGE=1 5V
BYPASS=U6201.J2:J1:5 mm

BYPASS=U6201.E1:F1:5 mm
C6302 0.1UF 10% 16V X7R CERM 0402

BYPASS=U6201.G1:F1:5 mm
C6303 0.1UF 10% 6.3V CERM X5R 0201
C6304 0.1UF 10% 6.3V CERM X5R 0201
BYPASS=U6201.K1:K3:5 mm
C6305 10UF 20% 10V X5R CERM 0402 1

PP3V3_S0
C6306 10UF 20% 10V X5R CERM 0402 1
BYPASS=U6201.A7:E3:5 mm
C6307 0.1UF 10% 6.3V CERM X5R 0201

PP3V3_S0
R6324 100K 5% 1/20W MF 201
R6325 100K 5% 1/20W MF 201

OMIT
R6302 SHORT 402

R6323 100K 5% 1/20W MF 201
PD_CS4208_GPIO1
NOSTUFF
R6322 100K 5% 1/20W MF 201

R6330 33 5% 1/10W MF-LF 402

R6331 22 5% 1/20W MF 201

R6332 75 1% 1/10W MF LF 402

U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

GPIO0_SPKR_SHUTDOWN	H3 GPIO0	
SPKRCONN_L_ID	H2 GPIO1	
SPKRCONN_R_ID	H1 GPIO2	
DFET_OPENUS	C4 GPIO3	
DFET_OPENCH	C5 GPIO4	
	C7 GPIO5	
NC_CS4208_GPO0 NO_TEST=TRUE	C9 GPO0	
NC_CS4208_GPO1 NO_TEST=TRUE	B9 GPO1	
HDA_BIT_CLK	F2 BCLK	
HDA_SYNC	E2 SYNC	
CS4208_HDA_SDOUT0_R	D1 SDI0	
HDA_SDIN0 / TP_CS4208_HDA_SDOUT1	C1 SDI1	
HDA_SDOUT	D2 SDO0	
	C2 SDO1	
	C3 SDO2	
HDA_RST_L	B1 SDO3	
	D3 RST*	
NC_CS4208_MCLKA NO_TEST=TRUE	A5 MCLK_A	
NC_CS4208_SCLKA NO_TEST=TRUE	B2 SCLK_A	
NC_CS4208_LRCLKA NO_TEST=TRUE	B4 LRCK_A	
NC_CS4208_SDOUTA NO_TEST=TRUE	A3 SDOUT_A	
	B3 SDIN_A	
NC_CS4208_MCLKB NO_TEST=TRUE	A6 MCLK_B	
NC_CS4208_SCLKB NO_TEST=TRUE	B6 SCLK_B	
NC_CS4208_LRCLKB NO_TEST=TRUE	B5 LRCK_B	
NC_CS4208_SDOUTB NO_TEST=TRUE	B8 SDOUT_B	
	A4 SDIN_B	
	C6 SDA	
	B7 SCL	
	J1 DGND	
	F1 LGND	
	E3 LGND	
	F3 LGND	
	J3 LGND	
	K3 LGND	
	VD J2	
	VL_HD E1	
	VL_SP A7	
	VL_IF G1	
	VL_DM K1	
SPDIF_IN	G3 CS4208_SPDIF_IN	
SPDIF_OUT	G2 CS4208_SPDIF_OUT	
DMIC_SDA0	N3	
DMIC_SCL0 NO_TEST=TRUE	N2 NC_DMIC_CLK0	
DMIC_SDA1	N1	
DMIC_SCL1 NO_TEST=TRUE	M1 NC_DMIC_CLK1	
DMIC_SDA2	M2	
DMIC_SCL2 NO_TEST=TRUE	L1 NC_DMIC_CLK2	
DMIC_SDA3	K2	
DMIC_SCL3	L2	
	NC F6	
	NC F7	
	NC F8	
	NC G6	
	NC G7	
	NC G8	
	NC H6	
	NC H7	
	NC H8	

SPDIF_OUT_JACK
DMIC_SDA3
DMIC_CLK3_R → DMIC_CLK3

PP6301 P3MMSM — DMIC_SDA3 — PLACE_NEAR=U6201.N3:5 mm
PP6302 P3MMSM — HDA_BIT_CLK — PLACE_NEAR=U6201.F2:5 mm
PP6303 P3MMSM — HDA_SYNC — PLACE_NEAR=U6201.E2:5 mm
PP6304 P3MMSM — HDA_SDOUT — PLACE_NEAR=U6201.D2:5 mm
PP6305 P3MMSM — CS4208_HDA_SDOUT0_R — PLACE_NEAR=U6201.D1:5 mm

SYNC_MASTER=JOE J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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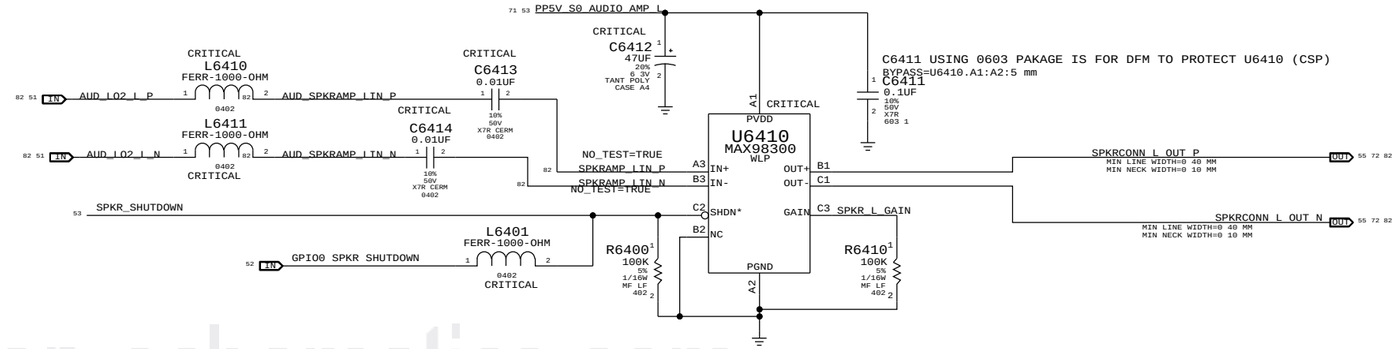
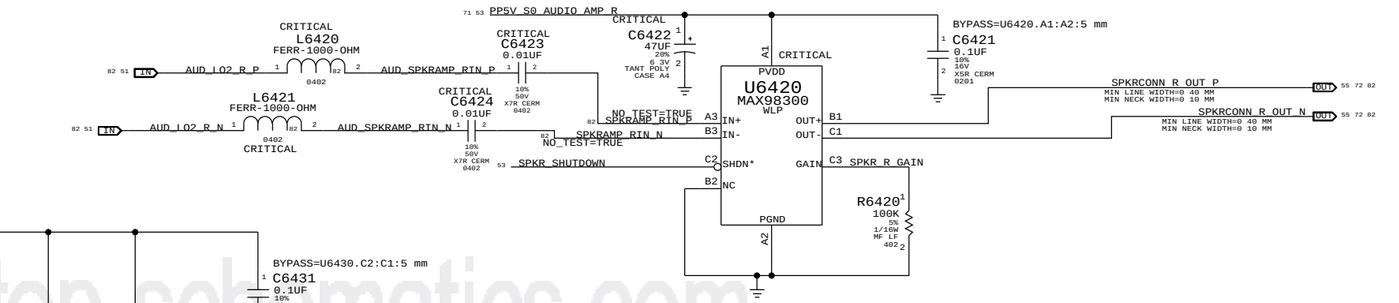
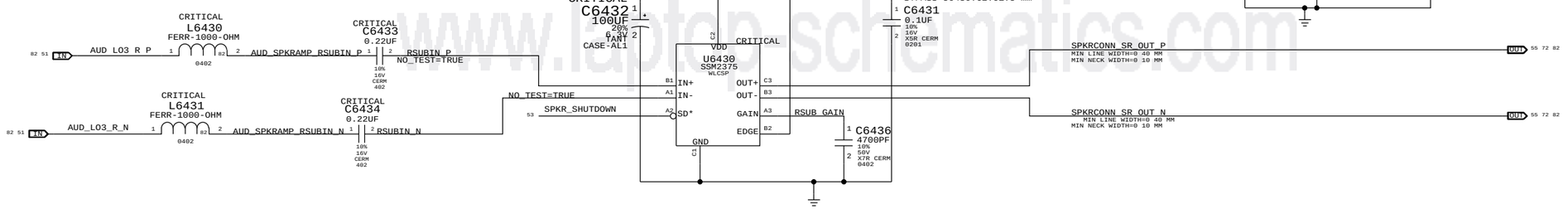
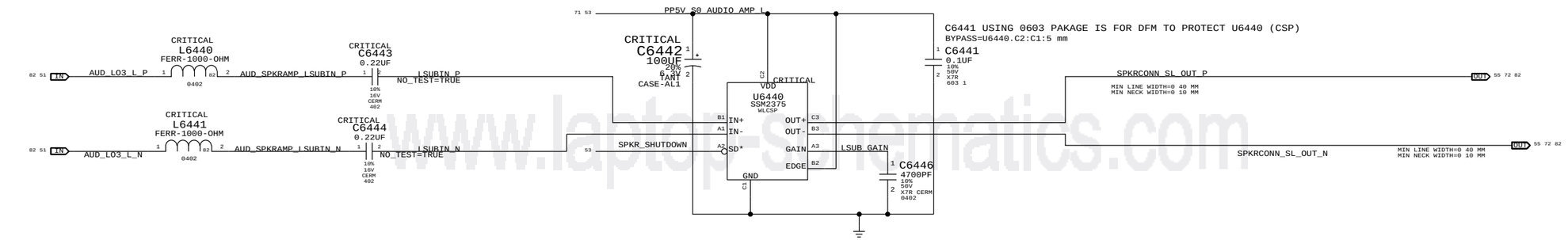
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC MASTER=JOE J45 SYNC DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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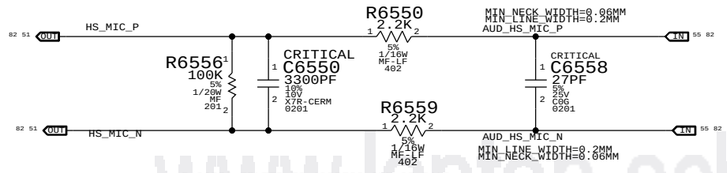
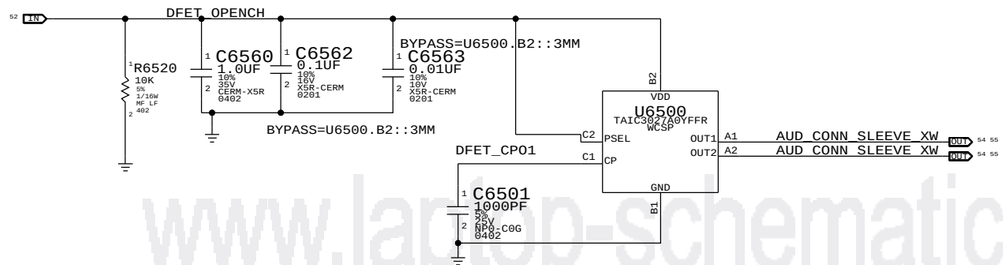
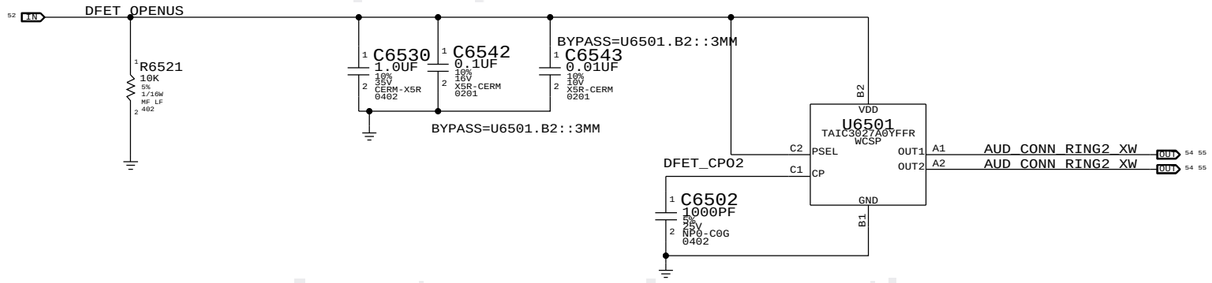


R/C6550 FILTER TO ADDRESS OUT-OF-BAND
NOISE ISSUE SEEN ON EARLY HEADSETS
(SEE RADAR # 6210118)





SYNC MASTER=CLEAN_X305 SYNC DATE=06/24/2014

PAGE TITLE
AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3 3V
DMIC 2	0X09 (9)	0X1C (28)	3 3V
HEADSET MIC	0X07 (7)	0X18 (24)	2 7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG LOW = MERRY	
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG LOW = MERRY	
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETs OPEN	

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

PP3V3_S0
DMIC_SDA3
DMIC_SDA2
DMIC_CLK3
OMIT
R6680
SHORT
402

L6611 120-OHM-25%-1.3A CRITICAL 0402
AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
XW6600 SM PLACE_NEAR=J6600.3:2.54mm
L6612 120-OHM-25%-1.3A CRITICAL 0402
AUD_CH_HS_GND
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
XW6601 SM
AUD_HS_MIC_P

L6613 120-OHM-25%-1.3A CRITICAL 0402
AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
XW6602 SM PLACE_NEAR=J6600.5:2.54mm
L6614 120-OHM-25%-1.3A CRITICAL 0402
AUD_US_HS_GND
AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
XW6603 SM
AUD_HS_MIC_N

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC
VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF
SHELL PINS

L6604 120-OHM-25%-1.3A CRITICAL 0402
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
R6602 2.2K 5% 1/20W MF 201
L6608 FERR-470-OHM CRITICAL 0201
AUD_TIPDET_2
AUD_CONN_TIPDET_2
GND_AUDIO_CODEC
L6607 FERR-470-OHM CRITICAL 0201
AUD_TIPDET_1
AUD_CONN_TIPDET_1
R6603 2.2K 5% 1/20W MF 201
L6605 120-OHM-25%-1.3A CRITICAL 0402
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
L6606 FERR-470-OHM CRITICAL 0201
AUD_TYPEDET
AUD_CONN_TYPEDET
SPDIF_OUT_JACK
PP3V3_S0

R6601 10K 5% 1/16W MF_LF 402

DZ6607 ESDALC5-1BM2 SOD882 CRITICAL
DZ6601 ESDALC5-1BM2 SOD882 CRITICAL
DZ6602 ESDALC5-1BM2 SOD882 CRITICAL
DZ6603 ESDALC5-1BM2 SOD882 CRITICAL
DZ6606 ESDALC5-1BM2 SOD882 CRITICAL
DZ6605 ESDALC5-1BM2 SOD882 CRITICAL
DZ6604 ESDALC5-1BM2 SOD882 CRITICAL

C6602 100PF 5% 25V C0G 0201
C6603 100PF 5% 25V C0G 0201
C6604 100PF 5% 25V C0G 0201
C6605 100PF 5% 25V C0G 0201
C6606 100PF 5% 25V C0G 0201
C6607 100PF 5% 25V C0G 0201
C6608 100PF 5% 25V C0G 0201
C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

SYNC_MASTER=CLEAN X305 SYNC_DATE=06/24/2014
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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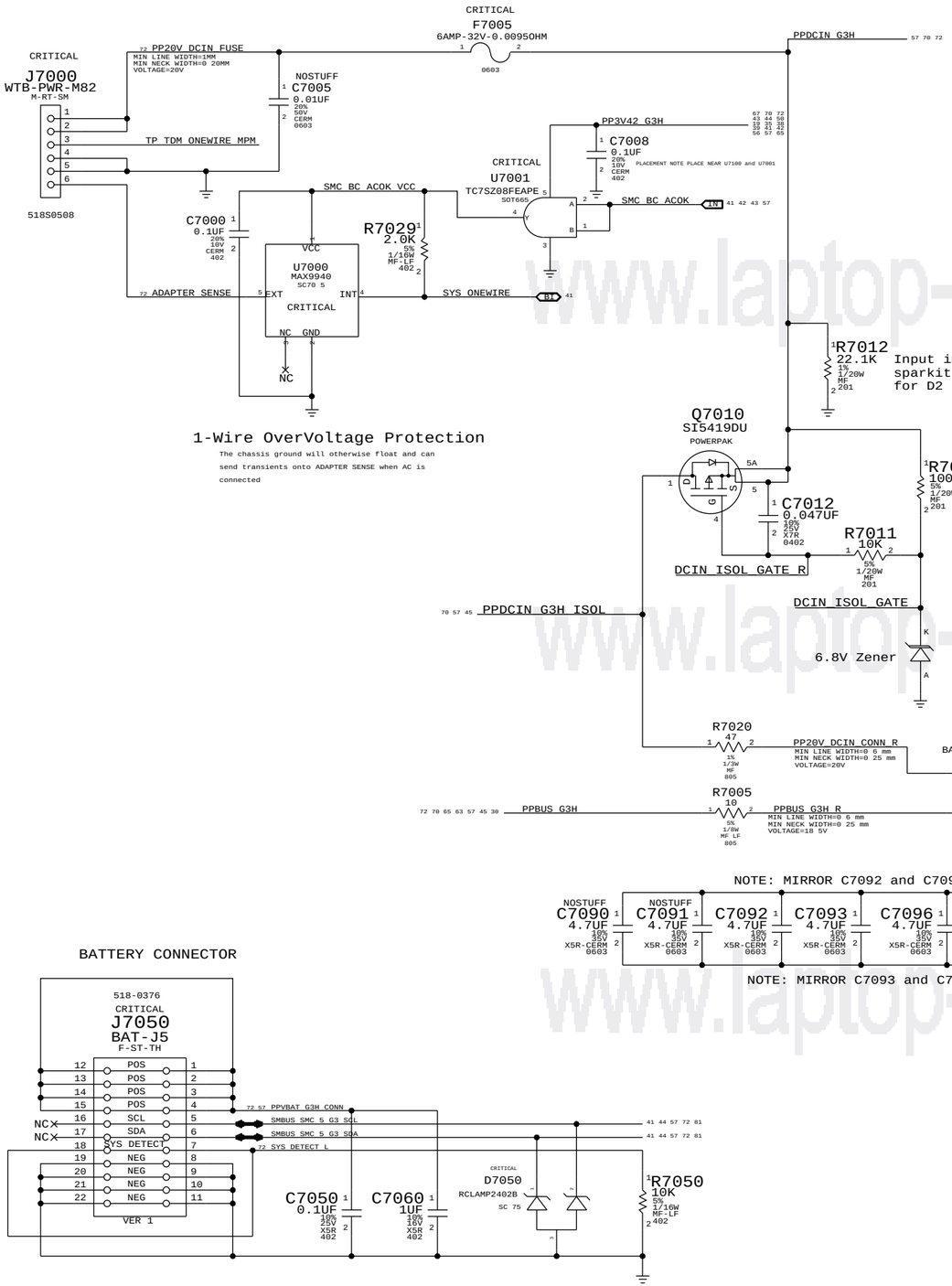
MagSafe DC Power Jack



SYNC_MASTER=CLEAN X305 PEG SYNC_DATE=02/18/2014

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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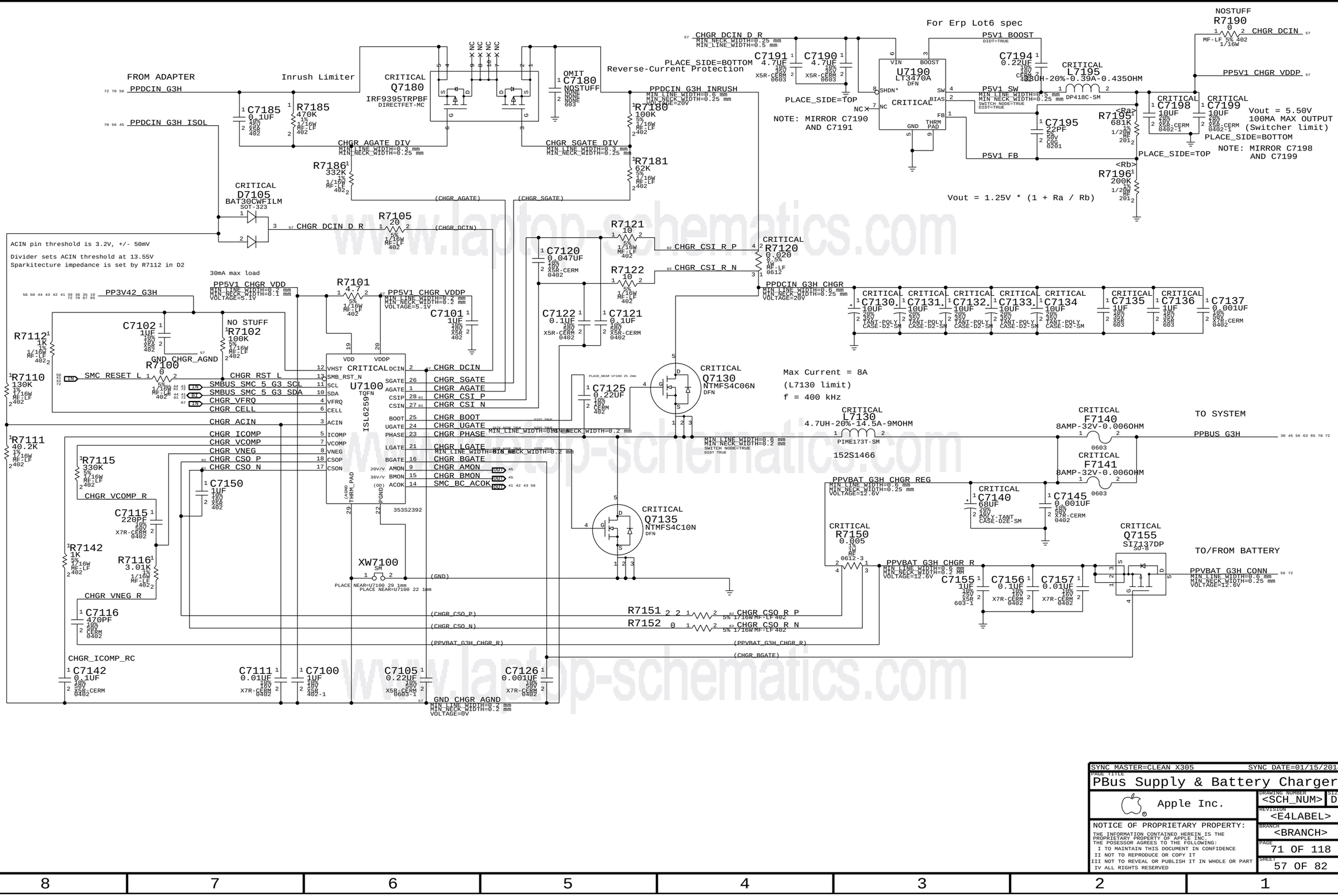

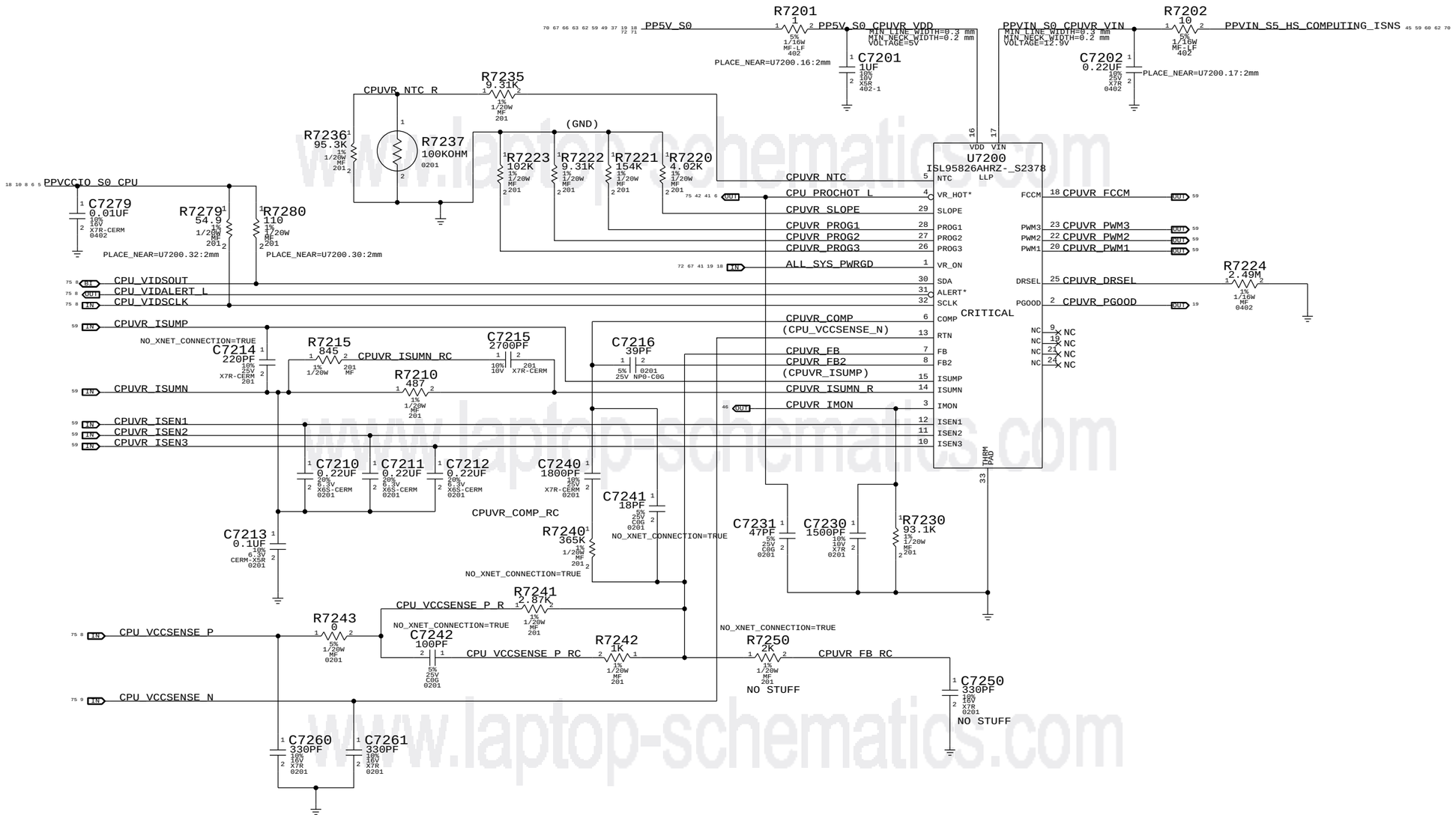

SYNC MASTER=CLEAN X305 PEG SYNC DATE=02/24/2014

PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 72 OF 118
SHEET 58 OF 82

PP5V_S0
PPVIN_S5_HS_COMPUTING_ISNS

PHASE 1

U7310 FDMF6808N PQFN CRITICAL
353S3836

R7311 0 5% 1/10W MF-LF 402 CPUVR_BOOT1_RC ↔ CPUVR_BOOT1
C7311 0.22UF 10% 16V CERM 402 CPUVR_PHASE1_K
C7310 1UF 10% 16V X6S CERM 0402

CPUVR_PWM1 (58)
CPUVR_FCCM (59 58)

L7310 0.36UH-20%-36A-0.001080HM CRITICAL
PIMS103T-SM 152S1538
CPUVR_PHASE1: MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH NODE=TRUE
PPVCC_S0_CPU_PH1: MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.8V

R7310 0.00075 1% 1W MF 0612 1 CRITICAL
R7312 2.2 5% 1/10W MF LF 603 NOSTUFF
C7312 0.001UF 10% 50V X7R CERM 0402 DIDT=TRUE NOSTUFF
CPUVR_PH1_SNUB

CPUVR_ISNS1_P (82 46 OUT)
CPUVR_ISNS1_N (OUT 46 59 82)
R7314 3.9 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN (OUT 58 59)
R7315 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7316 10K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
CPUVR_ISEN1 (OUT 58)
CPUVR_ISUMP (OUT 58 59)
R7317 10K 1% 1/20W MF 201 CPUVR_ISNS2_N NO_XNET_CONNECTION=TRUE (46 59 82)
R7318 10K 1% 1/20W MF 201 CPUVR_ISNS3_N NO_XNET_CONNECTION=TRUE (46 59 82)

C7313 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7314 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7315 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL
C7316 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL
C7317 1UF 10% 16V X6S CERM 0402
C7318 0.001UF 10% 50V X7R CERM 0402 THESE TWO CAPS ARE FOR EMC
C7319 0.001UF 10% 50V X7R CERM 0402

Additonal Input Bulk Caps
C7370 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7371 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7372 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7373 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7374 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7375 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7376 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7377 15UF 20% 16V TANT SM CRITICAL
C7378 15UF 20% 16V TANT SM CRITICAL
C7379 15UF 20% 16V TANT SM CRITICAL
C7380 15UF 20% 16V TANT SM CRITICAL
C7381 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7382 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7383 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7384 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL

PHASE 2

U7320 FDMF6808N PQFN CRITICAL
353S3836

R7321 0 5% 1/10W MF-LF 402 CPUVR_BOOT2_RC ↔ CPUVR_BOOT2
C7321 0.22UF 10% 16V CERM 402 CPUVR_PHASE2_K
C7320 1UF 10% 16V X6S CERM 0402

CPUVR_PWM2 (58)
CPUVR_FCCM (59 58)

L7320 0.36UH-20%-36A-0.001080HM CRITICAL
PIMS103T-SM 152S1538
CPUVR_PHASE2: MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH NODE=TRUE
PPVCC_S0_CPU_PH2: MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.8V

R7320 0.00075 1% 1W MF 0612 1 CRITICAL
R7322 2.2 5% 1/10W MF LF 603 NOSTUFF
C7322 0.001UF 10% 50V X7R CERM 0402 DIDT=TRUE NOSTUFF
CPUVR_PH2_SNUB

CPUVR_ISNS2_P (82 46 OUT)
CPUVR_ISNS2_N (OUT 46 59 82)
R7324 3.9 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN (OUT 58 59)
R7325 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7326 10K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
CPUVR_ISEN2 (OUT 58)
CPUVR_ISUMP (OUT 58 59)
R7327 10K 1% 1/20W MF 201 CPUVR_ISNS1_N NO_XNET_CONNECTION=TRUE (46 59 82)
R7328 10K 1% 1/20W MF 201 CPUVR_ISNS3_N NO_XNET_CONNECTION=TRUE (46 59 82)

C7323 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7324 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7325 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL
C7326 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL
C7327 1UF 10% 16V X6S CERM 0402
C7328 0.001UF 10% 50V X7R CERM 0402 THESE TWO CAPS ARE FOR EMC
C7329 0.001UF 10% 50V X7R CERM 0402

PHASE 3

U7330 FDMF6808N PQFN CRITICAL
353S3836

R7331 0 5% 1/10W MF-LF 402 CPUVR_BOOT3_RC ↔ CPUVR_BOOT3
C7331 0.22UF 10% 16V CERM 402 CPUVR_PHASE3_K
C7330 1UF 10% 16V X6S CERM 0402

CPUVR_PWM3 (58)
CPUVR_FCCM (59 58)

L7330 0.36UH-20%-36A-0.001080HM CRITICAL
PIMS103T-SM 152S1538
CPUVR_PHASE3: MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH NODE=TRUE
PPVCC_S0_CPU_PH3: MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.8V

R7330 0.00075 1% 1W MF 0612 1 CRITICAL
R7332 2.2 5% 1/10W MF LF 603 NOSTUFF
C7332 0.001UF 10% 50V X7R CERM 0402 DIDT=TRUE NOSTUFF
CPUVR_PH3_SNUB

CPUVR_ISNS3_P (82 46 OUT)
CPUVR_ISNS3_N (OUT 46 59 82)
R7334 3.9 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN (OUT 58 59)
R7335 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7336 10K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
CPUVR_ISEN3 (OUT 58)
CPUVR_ISUMP (OUT 58 59)
R7337 10K 1% 1/20W MF 201 CPUVR_ISNS1_N NO_XNET_CONNECTION=TRUE (46 59 82)
R7338 10K 1% 1/20W MF 201 CPUVR_ISNS2_N NO_XNET_CONNECTION=TRUE (46 59 82)

C7333 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7334 68UF 20% 16V POLY TANT CASE D2E SM CRITICAL
C7335 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL
C7336 10UF 20% 16V X6S CERM 0603 NOSTUFF CRITICAL
C7337 1UF 10% 16V X6S CERM 0402
C7338 0.001UF 10% 50V X7R CERM 0402 THESE TWO CAPS ARE FOR EMC
C7339 0.001UF 10% 50V X7R CERM 0402

PPVCC_S0_CPU (6 8 10 46 70 72)

Vout = 1.85V max
95A max output
f = 450 kHz

SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE_TITLE	CPU VR12.5 VCC Power Stage
Apple Inc.	DRAWING_NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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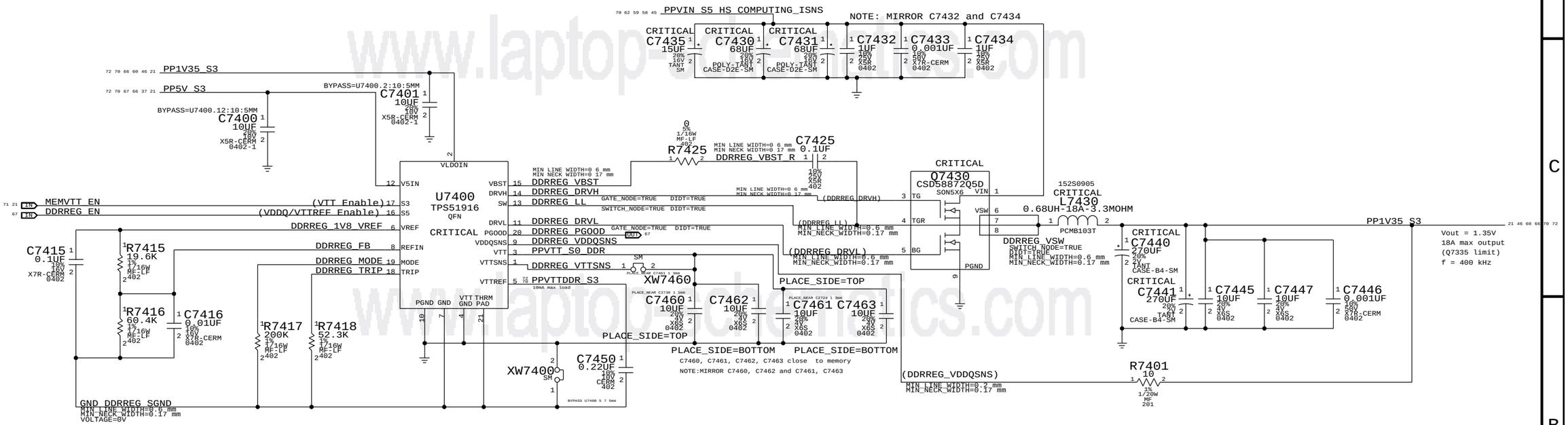
DDR3L (1V35 S3) REGULATOR



SYNC MASTER=CLEAN X305	SYNC DATE=01/15/2014
PAGE TITLE	1.35V DDR3L SUPPLY
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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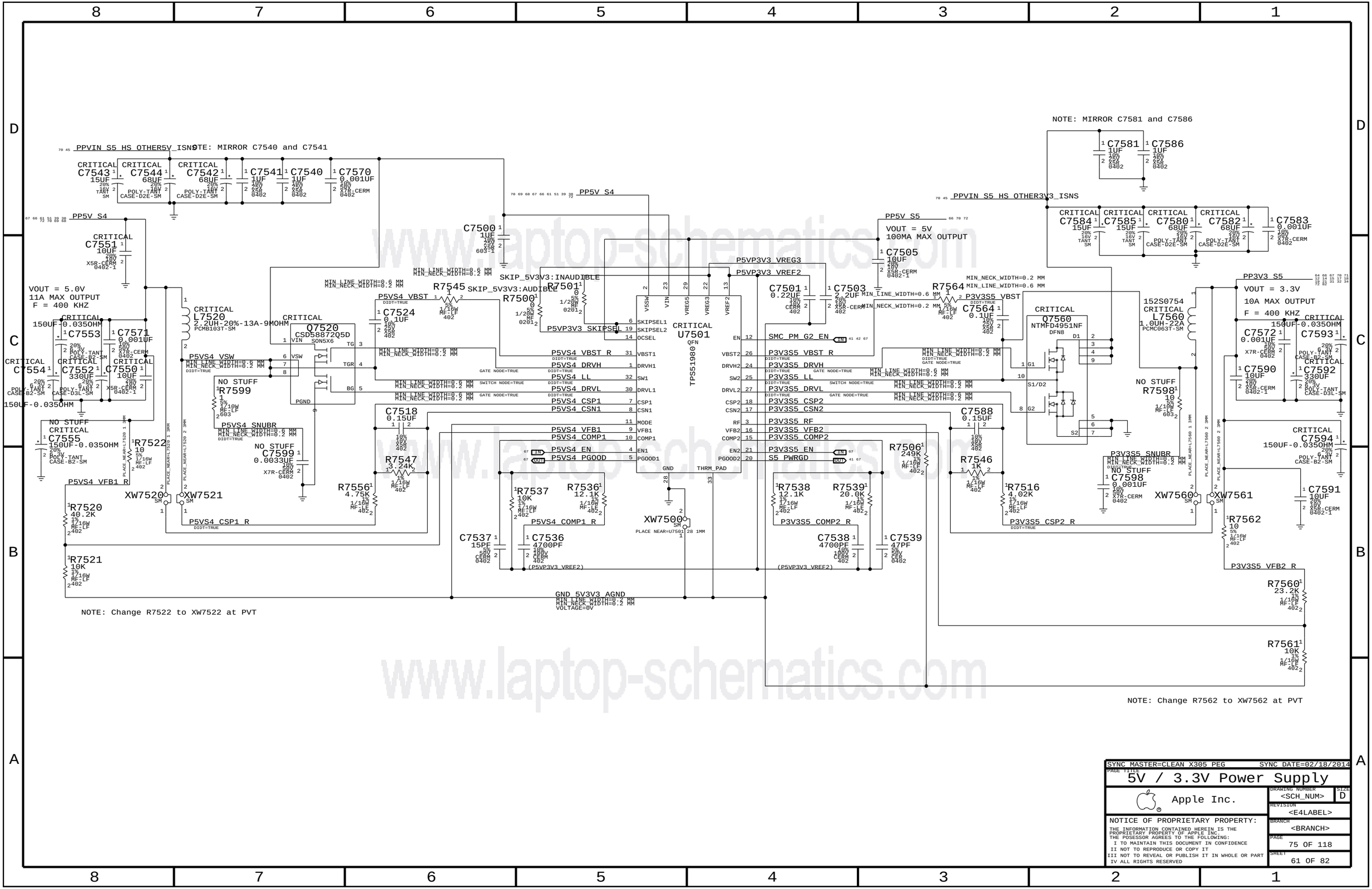
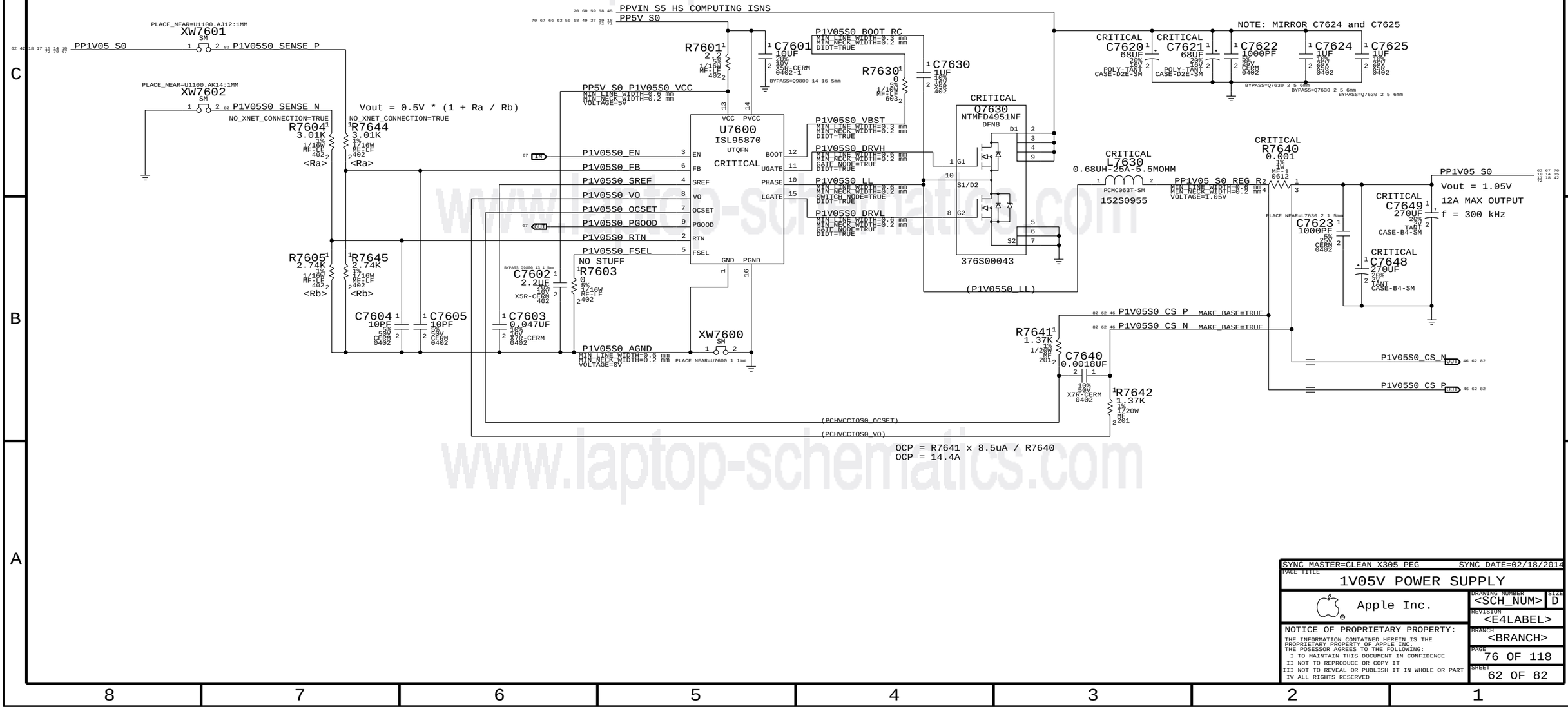


1V05 S0 REGULATOR



SYNC MASTER=CLEAN_X305_PEG SYNC DATE=02/18/2014

PAGE TITLE: 1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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Page Notes

Power aliases required by this page
- =PPVIN S0 LCDBKLT (9 12 6V LCD Backlight Input)
- =PP5V S0 BKLTCTRL (5V Backlight Driver Input)
- =PP5V S0 KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page
- BKLT ENG Stuffs 10 2 ohm series R for engineering builds
- BKLT PROD Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7723,R7724		BKLT:PROD

PPBUS_G3H — CRITICAL F7700 3AMP-32V-467 603-HF — PPBUS_S0_LCDBKLT_FUSED (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.6V)

R7700 0.025 1% 1W MTL 0612 — PPBUS_SW_LCDBKLT_PWR (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.6V)

CRITICAL Q7706 FDC638APZ SBMS001 SSOT6-HF

PPBUS_SW_BKL (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=12.6V)

C7700 1000PF 10% 16V X7R-1 0201

R7701 80.6K 1% 1/20W MF 0201

NOSTUFF C7701 0.001UF 10% 50V CERM 402

C7710 4.7UF 10% 25V X5S-CERM 0603

C7711 4.7UF 10% 25V X5S-CERM 0603

C7712 0.1UF 10% 25V X5R 402

152S1527 CRITICAL L7710 22UH-20%-2.4A-0.105OHM DEM8030C-SM

PPBUS_S0_LCDBKLT_PWR_SW (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=45V, SWITCH_NODE=TRUE, DIDT=TRUE)

PLACE NEAR L7710 2 3MM — CRITICAL D7701 POWERDI-123 DFLS2100

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

CRITICAL C7715 2.2UF 10% 16V X7R 1210-1 — PLACE NEAR=D7701 K 3MM

CRITICAL C7716 2.2UF 10% 16V X7R 1210-1 — PLACE NEAR=D7701 K 5MM

CRITICAL C7718 2.2UF 10% 16V X7R 1210-1 — PLACE NEAR=D7701 K 3MM

CRITICAL C7719 2.2UF 10% 16V X7R 1210-1 — PLACE NEAR=D7701 K 5MM

C7717 1000PF 10% 16V X7R-CERM 0603 — PLACE NEAR=D7701 K 5MM

PPVOUT_S0_LCDBKLT (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=55V)

ISNS_LCDBKLT_P (OUT)

ISNS_LCDBKLT_N (OUT)

LCDBKLT_EN_L

PP5V_S0

R7743 0 5% 1/16W MF-LF 402 — R7744 0 5% 1/16W MF-LF 402 — VOLTAGE=5V, MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM

PP5V_S0_BKLT_VDDA

PP5V_S0_BKLT_VDDD

R7702 63.4K 1% 1/16W MF-LF 402 — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V

C7740 1UF 10% 16V X5R 402-2 — C7741 1UF 10% 16V X5R 402-2

GND_BKLT_SGND

R7740 1M 5% 1/20W MF 201

U7701 LLP LP8548B1SQ_-04

BKLT_SD — (PPBUS_S0_BKLT_PWR_R) — (PPBUS_S0_BKLT_PWR_F)

BKLT_SENSE_OUT

R7742 0 1/20W MF 0201 — EDP_IG_BKL_ON (IN) — BKLT_EN_R

NO STUFF C7742 33PF 5% 25V NPO-C0G 0201

GND_BKLT_SGND

R7747 0 5% 1/20W MF 0201 — SMC_SYS_KBDLED (IN) — BKLT_PWM_KEYB

NO STUFF C7747 33PF 5% 25V NPO-C0G 0201

GND_BKLT_SGND

CRITICAL 353S4160

R7741 31.6K 1% 1/20W MF 201

PPVOUT_BKLT_FB2 (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V)

XW7700 SM

KBDBKLT_SW (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)

GND_BKLT_SGND (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V)

PP5V_S0

R7760 2.4K 5% 1/20W MF 201 — R7761 2.4K 5% 1/20W MF 201

R7758 0 5% 1/20W MF 0201 — I2C_BKLT_SCL (IN) — BKLT_SCL

R7757 0 5% 1/20W MF 0201 — I2C_BKLT_SDA (BI) — BKLT_SDA

PP5V_S0

R7783 0 5% 1/16W MF-LF 402

152S1701 CRITICAL L7720 10UH-20%-1.4A-0.17OHM PST041H-CDH46D14-SM

371S0572 CRITICAL D7720 SOD-123 RB160M-60G

XW7720 SM — PLACE NEAR=D7720 K 2MM

C7726 1.0UF 10% 16V X7R 0805 — C7727 1.0UF 10% 16V X7R 0805

PPVOUT_S0_KBDBKLT (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=40V)

MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V

C7720 2.2UF 10% 25V X5R-CERM 603 — C7721 2.2UF 10% 25V X5R-CERM 603 — C7722 0.1UF 10% 16V X5R-CERM 0201

C7720 C7721 SHOULD BE PLACED MIRRORED

C7723 1.0UF 10% 50V X7R 0805 — C7724 1.0UF 10% 50V X7R 0805 — C7725 0.001UF 10% 100V X7R-CERM 0402

C7723 C7724 SHOULD BE PLACED MIRRORED

BKL_SW (MIN_LINE_WIDTH=2 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)

BKL_FB

BKL_FET_CNTL_R (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)

CRITICAL Q7701 SI7812DN PWRPK-1212-8

R7703 0 5% 1/16W MF-LF 402

BKL_FET_CNTL (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE)

R7708 18.2K 1% 1/16W MF-LF 402

R7709 150K 1% 1/16W MF-LF 402

BKLT_ISET_KEYB

BKLT:ENG R7723 10.2 5% 1/16W MF 402 — KBDBKLT_RETURN1 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM)

BKLT:ENG R7724 10.2 5% 1/16W MF 402 — KBDBKLT_RETURN2 (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM)

BKLT_KEYB1

BKLT_KEYB2

R7780 0 5% 1/20W MF 0201 — EDP_IG_BKL_PWM (IN) — LCD_BKLT_PWM_R (OUT)

SYNC_MASTER	CLEAN_X305_PEG
SYNC_DATE	02/19/2014
PAGE_TITLE	LCD/KBD Backlight Driver
	Apple Inc.
DRAWING_NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
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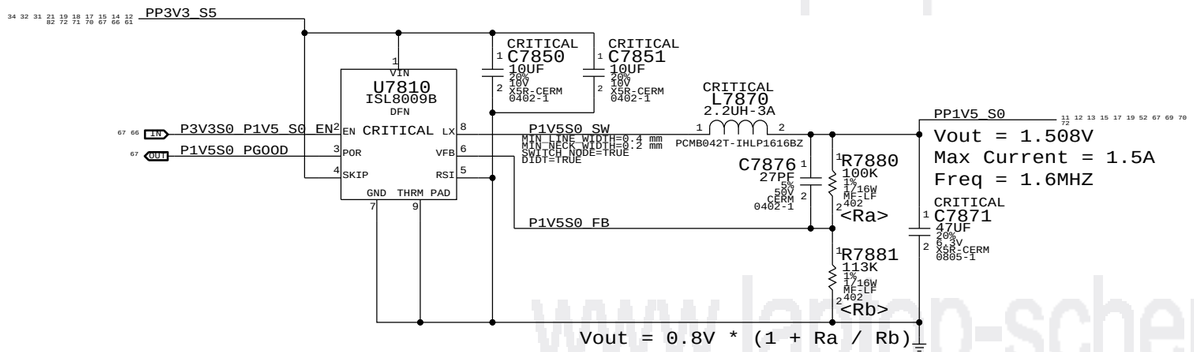
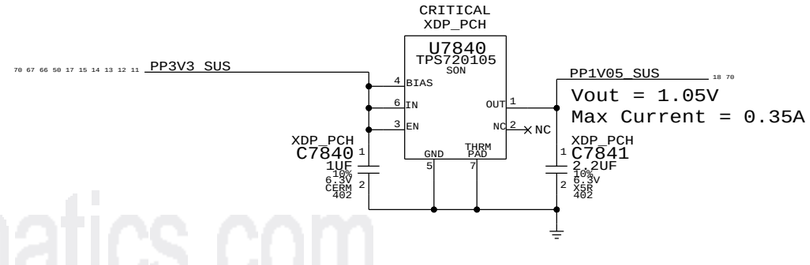
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC MASTER=CLEAN X305 SYNC DATE=01/15/2014

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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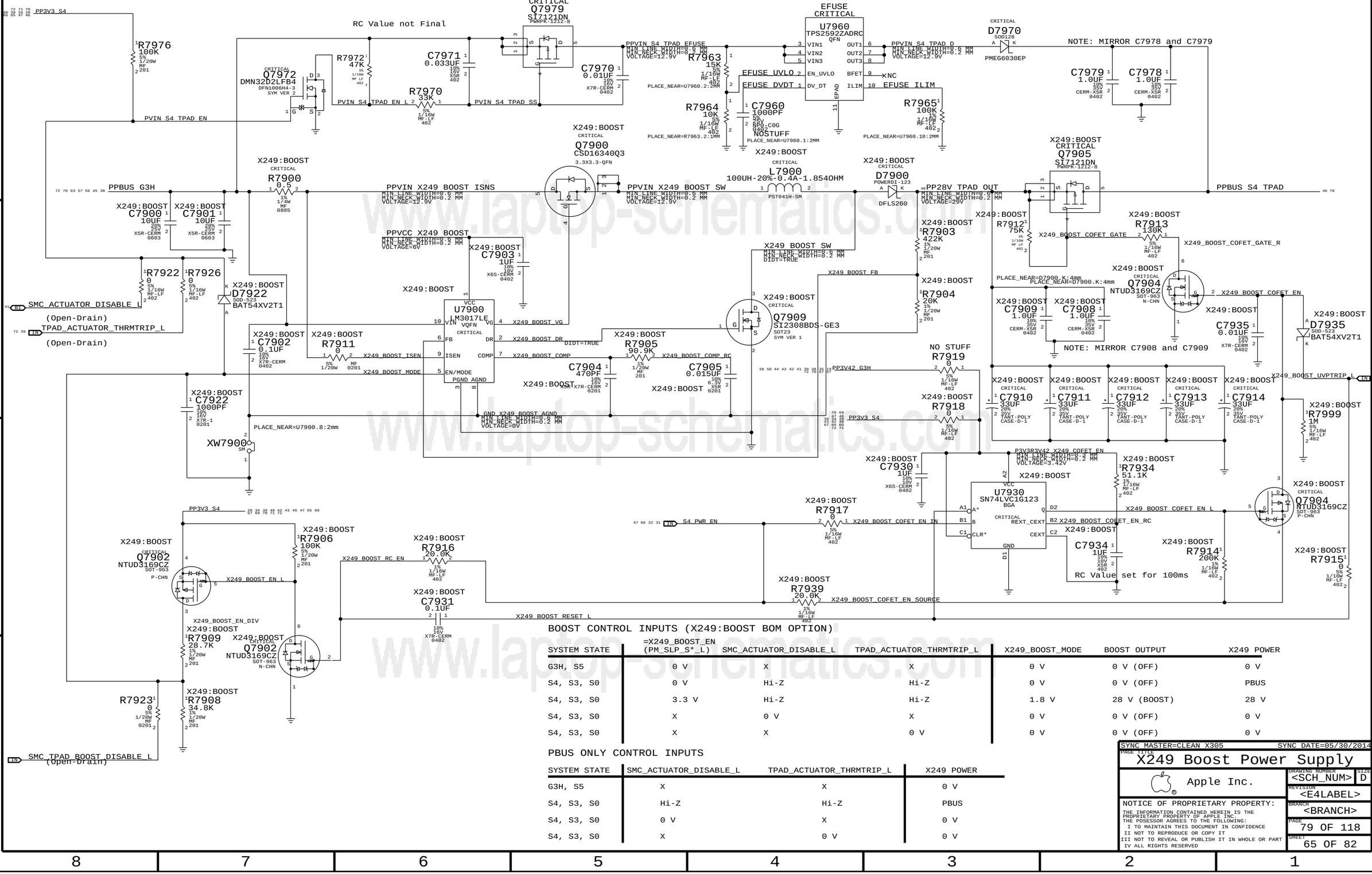

BOOST CONTROL INPUTS (X249:BOOST BOM OPTION)

SYSTEM STATE	=X249_BOOST_EN (PM_SLP_S*_L)	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	X249_BOOST_MODE	BOOST OUTPUT	X249 POWER
G3H, S5	0 V	X	X	0 V	0 V (OFF)	0 V
S4, S3, S0	0 V	Hi-Z	Hi-Z	0 V	0 V (OFF)	PBUS
S4, S3, S0	3.3 V	Hi-Z	Hi-Z	1.8 V	28 V (BOOST)	28 V
S4, S3, S0	X	0 V	X	0 V	0 V (OFF)	0 V
S4, S3, S0	X	X	0 V	0 V	0 V (OFF)	0 V

PBUS ONLY CONTROL INPUTS

SYSTEM STATE	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	X249 POWER
G3H, S5	X	X	0 V
S4, S3, S0	Hi-Z	Hi-Z	PBUS
S4, S3, S0	0 V	X	0 V
S4, S3, S0	X	0 V	0 V

SYNC_MASTER=CLEAN X305 SYNC_DATE=05/30/2014

PAGE TITLE: X249 Boost Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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3.3V S4 FET

376S0945
CRITICAL
Q8000
SIA413DJ
SC70-6L

EDP is per X305 Power Budget rev??

PP3V3_S5 → Q8002 DMN5L06VK-7 SOT563 VER 3 (D 6, G 2, S 1)
R8002 220K 5% 1/16W MF LF 402
C8009 0.033UF 10% 16V X5R 402
R8000 47K 5% 1/16W MF LF 402
C8000 0.01UF 10% 16V X7R CERM 0402
EN: S4_PWR_EN
P3V3S4_EN_L
P3V3S3_S4
PP3V3_S4

3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

CRITICAL
Q8010
SIA413DJ
SC70_6L

PP3V3_S5 → Q8012 DMN32D2LFB4 DFN1006H4-3 SYM VER 2 (D 3, G 1, S 2)
R8012 47K 5% 1/16W MF LF 402
C8011 0.033UF 10% 16V X5R 402
R8010 39K 5% 1/16W MF LF 402
C8010 0.01UF 10% 16V X7R CERM 0402
EN: P3V3S3_EN
P3V3S3_EN_L
P3V3S3_SS
PP3V3_S3

3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

CRITICAL
Q8050
SIA427DJ
SC70_6L

PP5V_S4 → Q8052 DMN5L06VK-7 SOT563 VER 3 (D 6, G 2, S 1)
R8052 200K 5% 1/16W MF LF 402
C8051 0.033UF 10% 16V X5R 402
R8050 5.1K 5% 1/16W MF LF 402
C8050 0.01UF 10% 16V X7R CERM 0402
EN: P5VS3_EN
P5VS3_EN_L
P5VS3_SS
PP5V_S3

5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

PP5V_S5
C8001 0.1UF 20% 10V CERM 402
U8001 SLG5AP1438V TDFN CRITICAL (VDD, CAP, ON, GND, D, S)
P1V35CPU_SLEW_CTL
EN: CPUVDDQ_EN
C8002 0.018UF 10% 16V X7R 402
Slew rate
0 8V/ms = 19 75nF
PP1V35_S3

1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R
R8005 0.002 1% 1W MF-1 0612
PP1V35_S3RS0_FET → PP1V35_S3RS0_CPUDDR
ISNS_CPUDDR_N (OUT)
ISNS_CPUDDR_P (OUT)

3.3V SUS FET

CRITICAL
Q8020
SIA413DJ
SC70_6L

PP3V3_S5 → Q8002 DMN5L06VK-7 SOT563 VER 3 (D 3, G 5, S 4)
R8022 100K 5% 1/16W MF-LF 402
C8021 0.033UF 10% 16V X5R 402
R8020 12K 5% 1/16W MF LF 402
C8020 0.01UF 10% 16V X7R CERM 0402
EN: PM_SLP_SUS
P3V3SUS_EN_L
P3V3SUS_SS
PP3V3_SUS

3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

SSD_PWR_EN:GPIO

SSD_PWR_EN → R8073 0 0201 1/20W 5% MF → SSD_PWR_EN_S
R8074 0 0201 1/20W 5% MF
SSD_PWR_FET_EN

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm

CRITICAL
Q8070
SI7615DN
PWRPK 1212 8

PP3V3_S5 → Q8072 DMN32D2LFB4 DFN1006H4-3 SYM VER 2 (D 3, G 1, S 2)
R8072 47K 5% 1/16W MF LF 402
C8071 0.033UF 10% 16V X5R 402
R8070 33K 5% 1/16W MF LF 402
C8070 0.01UF 10% 16V X7R CERM 0402
P3V3_SSD_EN_L
P3V3_SSD_SS
PP3V3_S0SW_SSD_R

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

CRITICAL
Q8060
SI7615DN
PWRPK 1212 8

PP5V_S4 → R8062 270K 5% 1/16W MF LF 402
C8061 0.12UF 10% 10V X5R 402
R8060 6.2K 5% 1/16W MF LF 402
C8060 0.47UF 10% 10V X5R 0402
P5V0S0_EN_L
P5V0S0_SS
PP5V_S0

Q8052 DMN5L06VK-7 SOT563 VER 3 (D 3, G 5, S 4)
EN: P5VS0_EN

5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 Switch

APN 353S2741

U8030 TPS22924 CSP CRITICAL (VIN, VOUT, ON, GND, A2, B2, C2, A1, B1)
PP3V3_S5
EN: P3V3S0_P1V5_S0_EN
PP3V3_S0
Max Current = 2A
C8030 1UF 10% 6.3V X5R 402

U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: Power FETs

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Power State Debug LEDs
(For development only)

PP3V3_S5 → R8194 0 5% 1/16W MF-LF 402 (PLACE_SIDE=BOTTOM; PP3V3_S5_DBGLED: MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0	
R8190 20K 5% 1/20W MF 201	R8191 20K 5% 1/20W MF 201	R8192 20K 5% 1/20W MF 201	R8193 20K 5% 1/20W MF 201	
D8190	D8191	D8192	D8193	GREEN-56MCD-2MA-2.65V LTQH9G-SM (PLACE_SIDE=BOTTOM, SILK_PART=S5_ON)
Q8190	Q8191	Q8192	Q8193	DMN5L06VK-7 SOT563 VER 3 (DBGLED_S4_D, DBGLED_S3_D); DMN32D2LFB4 DFN1006H4-3 SYM VER 2 (DBGLED_S0_D)

S4_PWR_EN, PM_SLP_S4_L, PM_SLP_S3_BUF_L

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

PP3V3_S5 → C8170 0.1uF 20% 10V CERM 402 (BYPASS=U8170 6 3 2 3mm; PM_SLP_S5_L 100K pull down on PCH page)

U8170 74LVC1G32 SOT891: PM_SLP_S5_L, SMC_S4_WAKESRC_EN → S4_PWR_EN (MAKE_BASE=TRUE); NC

S4_PWR_EN → D8174 BAT54XV2T1 SOD-523; R8174 43K 5% 1/16W MF-LF 402; P5VS4_EN_D → R8175 240 5% 1/10W MF-LF 402; C8174 2.2UF 10% 6.3V X5R 402; P5VS4_EN = P5VS4_EN (MAKE_BASE=TRUE)

S4_PWR_EN = S4_PWR_EN = S4_PWR_EN = S4_PWR_EN

S3 ENABLE

PM_SLP_S4_L (PM_SLP_S4 L 100K pull down in PCH page) → R8111 5.1K, R8112 0, R8113 0, R8114 3.3K (1/16W MF-LF 402)

TPAD_VBUS_EN_R

P5VS3_EN = P5VS3_EN (MAKE_BASE=TRUE)

P3V3S3_EN = P3V3S3_EN (MAKE_BASE=TRUE)

DDRREG_EN = DDRREG_EN (MAKE_BASE=TRUE)

C8110 0.47UF, C8112 0.47UF, C8113 0.47UF, C8114 0.47UF (10% 6.3V CERM-X5R 402; NO STUFF)

S0 ENABLE

PP3V3_S5 → C8180 0.1uF 20% 10V CERM 402 (BYPASS=U8180 8 3 2 3mm; PM_SLP_S3_L 100K pull down in PCH page)

R8178 100 5% 1/16W MF LF 402: PM_SLP_S3_L → PM_SLP_S3_R_L (MAKE_BASE=TRUE)

U8180 MC74VHC1G08 SC70-HF: (PM_SLP_S3_BUF_L) → PM_SLP_S3_R_L

PM_SLP_S3_BUF_L

R8180 100K 5% 1/16W MF-LF 402 (NO STUFF)

D8185 SOD-523 BAT54XV2T1

R8185 130K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7600 3 6mm)

R8186 20K 5% 1/16W MF-LF 402 (MAKE_BASE=TRUE)

R8187 0 5% 1/16W MF-LF 402 (PLACE_NEAR=Q8052 5 6mm; MAKE_BASE=TRUE)

P5VS0_EN = P5VS0_EN

P3V3S0_P1V5_S0_EN = P3V3S0_P1V5_S0_EN = P3V3S0_P1V5_S0_EN

P1V05_EN_D → R8138 820 5% 1/10W MF-LF 402 (PLACE_NEAR=R8138 1 6mm)

P1V05S0_EN = P1V05S0_EN (MAKE_BASE=TRUE)

C8185 0.82UF 10% 6.3V X5R 402; C8186 0.68UF 10% 6.3V CERM 402; C8187 0.68UF 10% 6.3V CERM 402 (NO STUFF)

PM_SLP_S3_R_L = PM_SLP_S3_R_L = PM_SLP_S3_R_L

CPUVCORE ENABLE

ALL_SYS_PWRGD = ALL_SYS_PWRGD (MAKE_BASE=TRUE)

3.3V SUS Enable

PM_SLP_SUS_L (MAKE_BASE=TRUE) = PM_SLP_SUS_L = PM_SLP_SUS_L

PM_SLP_SUS_L: 100K pull down on PCH page

S0 Rail PGOOD (BJT Version)

PP5V_S0 → R8151 54.9K 1% 1/16W MF LF 402 → VMON_5V_DIV (5.0V Divider:1.07V) → R8152 15.0K

PP3V3_S5 → R8156 150K 1% 1/16W MF LF 402 → S0PGD_C → ALL_SYS_PWRGD

R8153 1K 5% 1/16W MF LF 402: VMON_Q2_BASE ← PP1V35_S3RS0_CPUDDR

R8154 1K: VMON_Q3_BASE (NC)

R8155 1K: VMON_Q4_BASE (NC)

Q8150 ASMCC0179 DFN2015H4-8 353S2809 (Q1 Q2 Q3 CRITICAL Q4)

S0PGD_BJT_GND_R

PP3V3_S0 → R8158 15.0K 1% 1/16W MF LF 402 → VMON_3V3_DIV (3V3 Divider:1.07V) → R8159 7.15K

Vbe 0.7V max @2mA
Vce(sat) 0.1V max @1mA
Q1 Vth 0.7~1V @Id 250uA

3.3V SUS Detect

PP3V3_S5 → C8130 0.1uF 20% 10V CERM 402 (BYPASS=U8130 6 2 2 3mm)

PP3V3_SUS → R8133 100K 5% 1/16W MF LF 402 → PM_RSMRST_L (PM RSMRST L goes to U1100 C21)

U8130 TPS3808G33DBVRG4 SOT23 6: SENSE ← PP3V3_SUS; RESET* → PM_RSMRST_L; CT ← SUS_PGOOD_CT; MR* ← TP_SUS_PGOOD_MR_L; GND; VDD (CRITICAL)

C8131 0.001UF 20% 50V CERM 402 (NO STUFF)

S5 Rail Enables & PGOOD

SMC_PM_G2_EN (MAKE_BASE=TRUE) → R8140 100 5% 1/16W MF LF 402 (PLACE_NEAR=U7501.21:7mm) = SMC_PM_G2_EN

C8142 0.0033UF 10% 50V X7R CERM 402 (NO STUFF; PLACE_NEAR=U7501.21:7mm)

P3V3S5_EN = P3V3S5_EN (MAKE_BASE=TRUE)

PP3V42_G3H (PLACE_NEAR=U7501.20:7mm) → R8141 100K 5% 1/16W MF LF 402 (S5_PWRGD-->SMC, SMC-->PM_DSW_PWRGD)

S5_PWRGD = S5_PWRGD (MAKE_BASE=TRUE)

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

PP3V3_S4 → R8125 330K 5% 1/20W MF 201 → PM_WLAN_EN = PM_WLAN_EN (MAKE_BASE=TRUE)

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 0.815V-3.000V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

keep R8171 DDRCPU 1 35V only

PP3V3_S0 → C8162 0.1UF 20% 10V X7R CERM 0402 (NOSTUFF; PLACE_NEAR=U8160 2 4mm; S0PGOOD_ISL MIN_NECK_WIDTH=0.2 MM, MIN_LINE_WIDTH=0.5 MM, VOLTAGE=3.3V)

R8195 10 5% 1/16W MF LF 402 → PP3V3_S0_VMON_P2 → C8160 0.1UF (PLACE_NEAR=U8160 2 7mm)

PP3V3_S0_VMON_P7 → R8197 100K 5% 1/16W MF LF 402 (NOSTUFF)

PP3V3_S0 → C8161 0.1UF 20% 10V X7R CERM 0402 (PLACE_NEAR=U8160 7 6mm; S0PGOOD_ISL; PLACE_NEAR=U8160 2 6mm)

R8196 10 5% 1/16W MF LF 402 → PP3V3_S0_VMON_P7 → C8163 0.1UF (PLACE_NEAR=U8160 2 7mm)

PP1V35_S3RS0_CPUDDR → R8160 6.04K 1% 1/16W MF LF 402 (P5V_VMON divider 3.16V @4.5V)

PP1V05_S0 → R8172 6.04K 1% 1/16W MF LF 402 (P5V_DIV_VMON)

R8170 10K 1% 1/16W MF LF 402 (P1V05_VID_VMON)

R8161 15.0K 1% 1/16W MF LF 402 (1V35_VMON divider @ 731V @1.31V)

R8171 12.4K 1% 1/16W MF LF 402

R8173 15.0K 1% 1/16W MF LF 402 (1V05_VMON divider @ 716V @1.02V)

U8160 ISL88042IRTEZ TDFN (CRITICAL): VDD, V2MON 353S2310 (CPU), V3MON, V4MON, GND THRM_PAD; 1VMON_MR, DDRREG_PGOOD, S0PGOOD_ISL, RST*

R8168 100 5% 1/16W MF LF 402: P1V5S0_PGOOD → PM_SLP_S3_BUF_L

R8169 100: P1V05S0_PGOOD

R8167 10K 5% 1/16W MF LF 402 (PP1V5_S0)

R8120 100 5% 1/16W MF LF 402: DDRREG_PGOOD:Y

R8162 330 5% 1/16W MF LF 402: S0PGOOD_ISL → ALL_SYS_PWRGD_R → ALL_SYS_PWRGD

1V5 S0 "PGOOD" Delay

PP3V3_S5 → C8180 0.1uF 20% 10V CERM 402 (BYPASS=U8180 8 3 2 3mm)

U8180 MC74VHC1G08 SC70-HF

R8137 100 5% 1/16W MF LF 402: DELAY_1V5S0_PGD → ALL_SYS_PWRGD

R8136 23.7K 1% 1/16W MF-LF 402 → PM_1V5_PGD_L

C8134 2.2UF 10% 6.3V X5R 402

R8139 2.0K 1% 1/16W MF-LF 402 → PM_1V5_PGD_L_R

Q8151 DMB53D0UV SOT-563 (CRITICAL): Vgs:0.7V~1.0V

R8135 54.9K 1% 1/16W MF-LF 402 → PM_1V5_PGD_DIV

R8134 61.9K 1% 1/16W MF-LF 402

Q8151 DMB53D0UV DFN1006H4-3 SOT-563 (CRITICAL): VBEon: 0.58~0.7V, 1V5 Divider:0.75~0.85V

PM_SLP_S3_R_L

CHGR VFRQ Generation

VFRQ High: Variable Frequency
VFRQ Low: Fix Frequency

PP3V42_G3H → R8131 100K 5% 1/16W MF-LF 402 → CHGR_VFRQ

Unused PGOOD signals

Q8131 DMN32D2LFB4 DFN1006H4-3 SYM VER 2

PP5V_S3 → R8166 470K 5% 1/20W MF 201 → DDRREG_PGOOD

PP5V_S4 → R8165 470K 5% 1/16W MF-LF 402 → P5VS4_PGOOD

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LCD PANEL INTERFACE (eDP)

3.3V TCON Switch

TCON 3V3 <30mA

U8300

Part	SLG5AP1443V
Type	Load Switch
R(on) @100mA	17 mOhm Typ 19 mOhm Max
Current	2.5 A Max

U8310

Part	TPS22904
Type	Load Switch
R(on) @ 3.6V	66 mOhm Typ 90 mOhm Max
Current	0.5A Max

LCD Panel HPD & AUX strapping

SYNC_MASTER=CLEAN_X305_PEG	SYNC_DATE=02/10/2014
PAGE TITLE	eDP Display Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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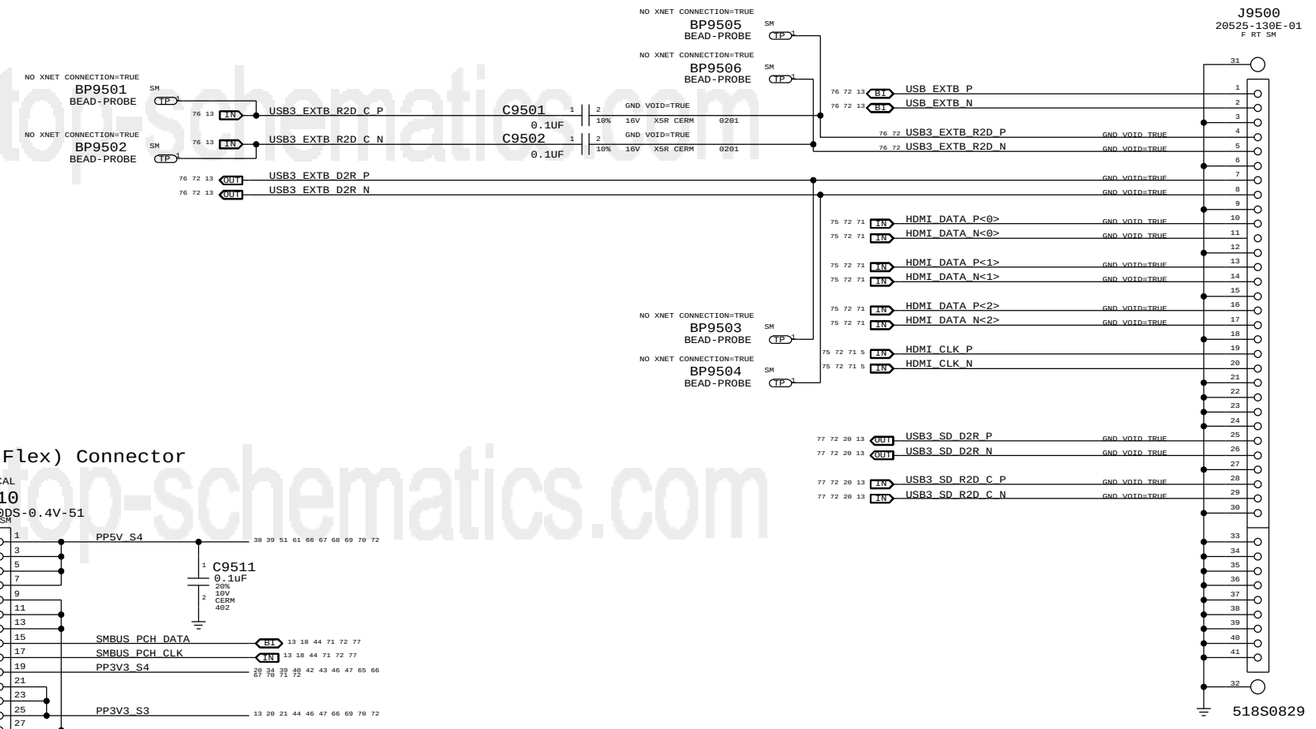
Wire-to-Board (Micro-coax) Connector

CRITICAL

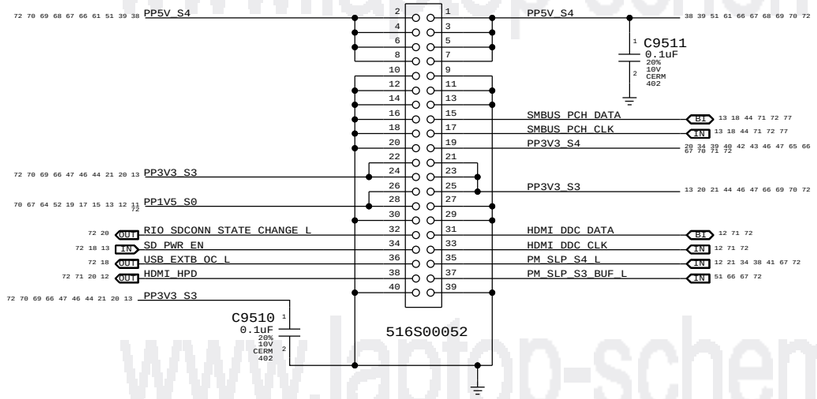
J9500
20525-130E-01
F RT SM



Board-to-Board (Flex) Connector

CRITICAL

J9510
DF40HC-3.0-40DS-0.4V-51
F-ST-SM



SYNC_MASTER=CLEAN_X305G SYNC_DATE=01/14/2014

PAGE TITLE

RIO Connectors

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Power Aliases

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Display Aliases

72 71 68 12	EDP_IG_PANEL_PWR	MAKE_BASE=TRUE	EDP_IG_PANEL_PWR	12 68 71 72
72 71 63 12	EDP_IG_BKL_ON	MAKE_BASE=TRUE	EDP_IG_BKL_ON	12 63 71 72
71 63 12	EDP_IG_BKL_PWM	MAKE_BASE=TRUE	EDP_IG_BKL_PWM	12 63 71
75 68 5	DP_INT_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLP<3..0>	
75 68 5	DP_INT_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLN<3..0>	
75 71 68 5	DP_INT_AUXCH_C_P	MAKE_BASE=TRUE	DP_INT_AUXCH_C_P	5 68 71 75
75 71 68 5	DP_INT_AUXCH_C_N	MAKE_BASE=TRUE	DP_INT_AUXCH_C_N	5 68 71 75
71 28 12	DP_TBTSNK0_HPD	MAKE_BASE=TRUE	DP_TBTSNK0_HPD	12 28 71
75 28 5	DP_TBTSNK0_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLP<3..0>	
75 28 5	DP_TBTSNK0_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLN<3..0>	
75 71 28 12	DP_TBTSNK0_AUXCH_C_P	MAKE_BASE=TRUE	DP_TBTSNK0_AUXCH_C_P	12 28 71 75
75 71 28 12	DP_TBTSNK0_AUXCH_C_N	MAKE_BASE=TRUE	DP_TBTSNK0_AUXCH_C_N	12 28 71 75
71 33 12	DP_TBTSNK0_DDC_DATA	MAKE_BASE=TRUE	DP_TBTSNK0_DDC_DATA	12 33 71
71 33 12	DP_TBTSNK0_DDC_CLK	MAKE_BASE=TRUE	DP_TBTSNK0_DDC_CLK	12 33 71
71 28 12	DP_TBTSNK1_HPD	MAKE_BASE=TRUE	DP_TBTSNK1_HPD	12 28 71
75 28 5	DP_TBTSNK1_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLP<3..0>	
75 28 5	DP_TBTSNK1_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_C_MLN<3..0>	
75 71 28 12	DP_TBTSNK1_AUXCH_C_P	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_P	12 28 71 75
75 71 28 12	DP_TBTSNK1_AUXCH_C_N	MAKE_BASE=TRUE	DP_TBTSNK1_AUXCH_C_N	12 28 71 75
71 33 12	DP_TBTSNK1_DDC_DATA	MAKE_BASE=TRUE	DP_TBTSNK1_DDC_DATA	12 33 71
71 33 12	DP_TBTSNK1_DDC_CLK	MAKE_BASE=TRUE	DP_TBTSNK1_DDC_CLK	12 33 71
72 71 69 20 12	HDMI_HPD	MAKE_BASE=TRUE	HDMI_HPD	12 20 69 71 72
75 72 69	HDMI_DATA_P<0..2>	MAKE_BASE=TRUE	TP_DP_IG_D_MLP<2..0>	5
75 72 69	HDMI_DATA_N<0..2>	MAKE_BASE=TRUE	TP_DP_IG_D_MLN<2..0>	5
75 72 71 69 5	HDMI_CLK_P	MAKE_BASE=TRUE	HDMI_CLK_P	5 69 71 72 75
75 72 71 69 5	HDMI_CLK_N	MAKE_BASE=TRUE	HDMI_CLK_N	5 69 71 72 75
72 71 69 12	HDMI_DDC_CLK	MAKE_BASE=TRUE	HDMI_DDC_CLK	12 69 71 72
72 71 69 12	HDMI_DDC_DATA	MAKE_BASE=TRUE	HDMI_DDC_DATA	12 69 71 72

Unused TPAD SPI

66 65 47 46 43 42 40 39 34 20 72 71 70 69 67 — PP3V3_S4

RA294 100K 1% 1/20W MF 201 (2–1)
RA295 100K 1% 1/20W MF 201 (2–1)
RA296 100K 1% 1/20W MF 201 (2–1)
RA297 100K 1% 1/20W MF 201 (2–1)
RA298 100K 1% 1/20W MF 201 (2–1)
RA299 100K 1% 1/20W MF 201 (2–1)

				MAKE_BASE
72 71 39	TPAD_SPI_BUS_EN	71 39 72	TPAD_SPI_BUS_EN	TRUE
77 72 71 39	TPAD_SPI_CS_L	72 71 39 74	TPAD_SPI_CS_L	TRUE
72 71 39	TPAD_SPI_INT_L	72 71 39	TPAD_SPI_INT_L	TRUE
77 72 71 39	TPAD_SPI_MISO	72 71 39 74	TPAD_SPI_MISO	TRUE
77 72 71 39	TPAD_SPI_MOSI	72 71 39 74	TPAD_SPI_MOSI	TRUE
77 72 71 39	TPAD_SPI_SCLK	72 71 39 74	TPAD_SPI_SCLK	TRUE

78 75 71 24 23 22	PP0V75_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 71 75 78
75 71 26 25 22	PP0V75_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 71 75
78 75 71 26 25 24 23 22	PP0V75_S3_MEM_VREFCA	0.675V	TRUE	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 71 75 78
78 75 71 26 25 24 23 22	PP0V75_S3_MEM_VREFCA				
78 75 71 26 25 24 23 22	PP0V75_S3_MEM_VREFCA				

EDP CABLE

72 71 68 63	I2C_BKLT_SCL	MAKE_BASE=TRUE	I2C_BKLT_SCL 63 68 71 72
72 71 68 63	I2C_BKLT_SDA	MAKE_BASE=TRUE	I2C_BKLT_SDA 63 68 71 72
81 72 71 68 48 44 41 37	SMBUS_SMC_0_S0_SCL		SMBUS_SMC_0_S0_SCL 37 41 44 48 68 71 72 81
81 72 71 68 48 44 41 37	SMBUS_SMC_0_S0_SDA		SMBUS_SMC_0_S0_SDA 37 41 44 48 68 71 72 81

CPU signals

71 60 21	MEMVTT_EN	MAKE_BASE=TRUE	MEMVTT_EN 21 60 71

J9510 RIO FLEX CONN

77 72 71 69 44 18 13	SMBUS_PCH_DATA		SMBUS_PCH_DATA 13 18 44 69 71 72 77
77 72 71 69 44 18 13	SMBUS_PCH_CLK		SMBUS_PCH_CLK 13 18 44 69 71 72 77

SSD Signals Through PEG

75 35 5	PCIE_SSD_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<3..0>
75 35 5	PCIE_SSD_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<3..0>
75 35 5	PCIE_SSD_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<3..0>
75 35 5	PCIE_SSD_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<3..0>

Thunderbolt Signals Through PEG

75 28 5	PCIE_TBT_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<11..8>
75 28 5	PCIE_TBT_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<11..8>
75 28 5	PCIE_TBT_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<11..8>
75 28 5	PCIE_TBT_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<11..8>

Unused PEG Lanes

	TP_PEG_D2RP<7..4>	MAKE_BASE=TRUE	=PEG_D2R_P<7..4> 5
	TP_PEG_D2RN<7..4>	MAKE_BASE=TRUE	=PEG_D2R_N<7..4> 5
	TP_PEG_R2D_CP<7..4>	MAKE_BASE=TRUE	=PEG_R2D_C_P<7..4> 5
	TP_PEG_R2D_CN<7..4>	MAKE_BASE=TRUE	=PEG_R2D_C_N<7..4> 5
5	TP_PEG_D2RP<15..12>	MAKE_BASE=TRUE	=PEG_D2R_P<15..12>
5	TP_PEG_D2RN<15..12>	MAKE_BASE=TRUE	=PEG_D2R_N<15..12>
5	TP_PEG_R2D_CP<15..12>	MAKE_BASE=TRUE	=PEG_R2D_C_P<15..12>
5	TP_PEG_R2D_CN<15..12>	MAKE_BASE=TRUE	=PEG_R2D_C_N<15..12>

Unused PCH PCIE Lanes

		MAKE_BASE	NO_TEST	
13	NC_PCIE_SSD_D2RP<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_P<3..0>
13	NC_PCIE_SSD_D2RN<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_N<3..0>
13	NC_PCIE_SSD_R2D_CP<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_P<3..0>
13	NC_PCIE_SSD_R2D_CN<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_N<3..0>

71 49 — PP3V3_S3_FAN_CTL — PP3V3_S3_FAN_CTL 49 71
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

RA201 0 5% 1/20W MF 0201 (1–2) — PP3V3_S5 — 12 14 15 17 18 19 21 31 32 34 61 64 66 67 70 72 82
RA202 0 5% 1/20W MF 0201 (1–2) — PP3V3_S4 — 20 34 39 40 42 43 46 47 65 66 67 69 70 71 72
RA202 NOSTUFF

67 66 63 62 59 58 49 37 19 18 72 70 — PP5V_S0

XWA202 SM (1–2) — PP5V_S0_AUDIO_AMP_L — 53
XWA203 SM (1–2) — PP5V_S0_AUDIO_AMP_R — 53
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
14	DPMUX_UC_IRQ
14	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L
14	LPCPLUS_GPIO

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

Apple Inc.

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Functional Test Points

J3501 - airport

FUNC_TEST

TRUE	AP_CLKREQ_Q_L	34
TRUE	AP_RESET_CONN_L	34
TRUE	PCIE_AP_D2R_PI_N	34 77
TRUE	PCIE_AP_D2R_PI_P	34 77
TRUE	PCIE_AP_R2D_N	34 77
TRUE	PCIE_AP_R2D_P	34 77
TRUE	PCIE_CLK100M_AP_CONN_N	34 77
TRUE	PCIE_CLK100M_AP_CONN_P	34 77
TRUE	PCIE_WAKE_L	12 34 36 77
TRUE	PP3V3_S3RS4_BT_F	34
TRUE	PP3V3_WLAN	34 42
TRUE	USB_BT_CONN_N	34 76
TRUE	USB_BT_CONN_P	34 76
TRUE	WIFI_EVENT_L	34 41 42
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	37 80
TRUE	MIPI_CLK_CONN_P	37 80
TRUE	CAM_SENSOR_WAKE_L_CONN	37
TRUE	MIPI_DATA_CONN_N	37 80
TRUE	MIPI_DATA_CONN_P	37 80
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72 81
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72 81
TRUE	I2C_CAM_SCK	36 37
TRUE	I2C_CAM_SDA	36 37
TRUE	PP5V_S3RS0_ALSCAM_F	37
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	5 69 71 75
TRUE	HDMI_CLK_P	5 69 71 75
TRUE	HDMI_DATA_N<0>	69 71 75
TRUE	HDMI_DATA_N<1>	69 71 75
TRUE	HDMI_DATA_N<2>	69 71 75
TRUE	HDMI_DATA_P<0>	69 71 75
TRUE	HDMI_DATA_P<1>	69 71 75
TRUE	HDMI_DATA_P<2>	69 71 75
TRUE	USB3_SD_D2R_N	13 20 69 77
TRUE	USB3_SD_D2R_P	13 20 69 77
TRUE	USB3_SD_R2D_C_N	13 20 69 77
TRUE	USB3_SD_R2D_C_P	13 20 69 77
TRUE	USB3_EXTB_D2R_N	13 69 76
TRUE	USB3_EXTB_D2R_P	13 69 76
TRUE	USB3_EXTB_R2D_N	69 76
TRUE	USB3_EXTB_R2D_P	69 76
TRUE	USB_EXTB_N	13 69 76
TRUE	USB_EXTB_P	13 69 76
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 69
TRUE	HDMI_DDC_CLK	12 69 71
TRUE	HDMI_DDC_DATA	12 69 71
TRUE	HDMI_HPD	12 20 69 71
TRUE	SMBUS_PCH_CLK	13 18 44 69 71 77
TRUE	SMBUS_PCH_DATA	13 18 44 69 71 77
TRUE	PM_SLP_S3_BUF_L	51 66 67 69
TRUE	PM_SLP_S4_L	12 21 34 38 41 67 69
TRUE	PP3V3_S3	3X 13 20 21 44 46 47 66 69 70 72
TRUE	PP3V3_S4	20 34 39 40 42 43 46 47 65 66 67 69 70 71 72
TRUE	PP5V_S4	5X 38 39 51 61 66 67 68 69 70 72
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 69
TRUE	USB_EXTB_OC_L	18 69
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	SMC_LID_R	43
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 58 59 62 63 66 67 70 71 72
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 58 59 62 63 66 67 70 71 72
TRUE	GND	5X

J6100 - spi

FUNC_TEST

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	SMC_RESET_L	41 42 50 57
TRUE	SMC_TCK	41 42 50
TRUE	SMC_TMS	41 42 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	SPI_ALT_CLK	50 77
TRUE	SPI_ALT_CS_L	50 77
TRUE	SPI_ALT_IO0_MOSI	50 77
TRUE	SPI_ALT_IO1_MISO	50 77
TRUE	SPI_ALT_IO2_WP_L	50 77
TRUE	SPI_ALT_IO1_HOLD_L	50 77
TRUE	GND	2X

J4801 - ipd flex

TRUE	TPAD_SPI_INT_L	39 71
TRUE	TPAD_SPI_CS_L	39 71 77
TRUE	TPAD_SPI_MOSI	39 71 77
TRUE	TPAD_SPI_MISO	39 71 77
TRUE	TPAD_SPI_SCLK	39 71 77
TRUE	TPAD_SPI_BUS_EN	39 71
TRUE	USB_TPAD_N	13 39 76
TRUE	USB_TPAD_P	13 39 76
TRUE	IOXP2_INT_L	39
TRUE	I2C_IOXP_SCL	39
TRUE	I2C_IOXP_SDA	39
TRUE	SMC_PME_S4_WAKE_L	34 39 41 43
TRUE	TPAD_ACTUATOR_THRMTRIP_L	39 65
TRUE	TPAD_VBUS_EN	39
TRUE	SMBUS_SMC_2_S3_SCL	39 41 44 81
TRUE	SMBUS_SMC_2_S3_SDA	39 41 44 81
TRUE	SMC_LID	39 41 42 43
TRUE	SMC_ACTUATOR_EN_L	39 41
TRUE	PPVIN_S4_TPAD	4X 39 46 70
TRUE	GND_ACTUATOR	4X 39
TRUE	PP3V3_S4	20 34 39 40 42 43 46 47 65 66 67 69 70 71 72
TRUE	PP5V_S4	38 39 51 61 66 67 68 69 70 72
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 34 39 40 42 43 46 47 65 66 67 69 70 71 72
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	WS_CONTROL_KBD	39
TRUE	WS_KBD1	39
TRUE	WS_KBD10	39
TRUE	WS_KBD11	39
TRUE	WS_KBD12	39
TRUE	WS_KBD13	39
TRUE	WS_KBD14	39
TRUE	WS_KBD15_CAP	39
TRUE	WS_KBD16_NUM	39
TRUE	WS_KBD17	39
TRUE	WS_KBD18	39
TRUE	WS_KBD19	39
TRUE	WS_KBD2	39
TRUE	WS_KBD20	39
TRUE	WS_KBD21	39
TRUE	WS_KBD22	39
TRUE	WS_KBD23	39
TRUE	WS_KBD3	39
TRUE	WS_KBD4	39
TRUE	WS_KBD5	39
TRUE	WS_KBD6	39
TRUE	WS_KBD7	39
TRUE	WS_KBD8	39
TRUE	WS_KBD9	39
TRUE	WS_KBD_ONOFF_L	39
TRUE	WS_LEFT_OPTION_KBD	39
TRUE	WS_LEFT_SHIFT_KBD	39
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 40 63
TRUE	KBDBKLT_RETURN2	2X 40 63
TRUE	PPVOUT_S0_KBDBKLT	40 63
TRUE	GND	4X

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	66 67 68 70 72 82 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 82
TRUE	SPKRCONN_L_OUT_P	53 55 82
TRUE	SPKRCONN_SL_OUT_N	53 55 82
TRUE	SPKRCONN_SL_OUT_P	53 55 82
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 82
TRUE	SPKRCONN_R_OUT_P	53 55 82
TRUE	SPKRCONN_SR_OUT_N	53 55 82
TRUE	SPKRCONN_SR_OUT_P	53 55 82
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	41 44 56 57 81
TRUE	SMBUS_SMC_5_G3_SDA	41 44 56 57 81
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	68 75
TRUE	DP_INT_AUX_P	68 75
TRUE	DP_INT_ML_N<0>	68 75
TRUE	DP_INT_ML_N<1>	68 75
TRUE	DP_INT_ML_N<2>	68 75
TRUE	DP_INT_ML_N<3>	68 75
TRUE	DP_INT_ML_P<0>	68 75
TRUE	DP_INT_ML_P<1>	68 75
TRUE	DP_INT_ML_P<2>	68 75
TRUE	DP_INT_ML_P<3>	68 75
TRUE	LCD_IRQ_L	68
TRUE	LCD_HPD_CONN	68
TRUE	LCD_BKLT_PWM_R	63 68
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72 81
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72 81
TRUE	I2C_BKLT_SDA	63 68 71
TRUE	I2C_BKLT_SCL	63 68 71
TRUE	PP5VR3V3_SW_LCD	3X 68
TRUE	PPVOUT_S0_LCDBKLT	63 68
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 41 67
TRUE	PPVTT_S0_DDR	21 27 60 70
TRUE	PP3V3_S0	66 67 68 70 72 82 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 44 46 47 66 69 70 72
TRUE	PP3V3_S5	17 34 35 37 38 39 41 42 43 44 50 56 61 64 66 67 70 71 72
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 65 67 70 72
TRUE	PP5V_S0	18 19 37 49 58 59 62 63 66 67 70 71 72
TRUE	PP5V_S3	21 37 60 66 67 70
TRUE	PP5V_S5	61 66 70
TRUE	PPBUS_G3H	30 45 56 57 63 65 70
TRUE	PPDCIN_G3H	56 57 70
TRUE	PPVCC_S0_CPU	6 8 10 46 59 70
TRUE	PPVTTDDR_S3	60 70
TRUE	PP3V3_S0SW_SSD	35 46 70
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 67 69 70
TRUE	PP1V35_S3	21 46 60 66 70

XDP

FUNC_TEST

TRUE	XDP_CPU_TCK	6 18 75
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 75
TRUE	XDP_CPU_TDO	6 18 75
TRUE	XDP_CPUPCH_TRST_L	6 18 75
TRUE	XDP_CPU_TMS	6 18 75
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 75
TRUE	XDP_CPU_PRDY_L	6 18 75
TRUE	PM_RSMRST_L	12 67 77
TRUE	PM_PCH_PWROK	12 19 77
TRUE	PM_SYSRST_L	12 19 41 77
TRUE	CPU_CFG<3>	6 18 75
TRUE	PP1V05_S0	10 14 15 17 18 42 62 67 70
TRUE	GND	2X GND

Power Sequence

FUNC_TEST

TRUE	SMC_ONOFF_L	39 41 42
TRUE	PM_DSW_PWRGD	12 41 77
TRUE	ALL_SYS_PWRGD	18 19 41 58 67
TRUE	PM_PCH_SYS_PWROK	12 18 19 41 77
TRUE	PLT_RESET_L	12 18 20 21
TRUE	EDP_IG_PANEL_PWR	12 68 71
TRUE	EDP_IG_BKL_ON	12 63 71

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Functional Test Points

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NC NO_TESTs

PCH

		NO_TEST	MAKE_BASE	
NC_USB3_SPARE_D2RN		TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP		TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN		TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP		TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN		TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP		TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN		TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP		TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN		TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP		TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN		TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP		TRUE	TRUE	NC_USB3_EXTD_R2D_CP

NC_PCIE_ENET_D2RN		TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP		TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN		TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP		TRUE	TRUE	NC_PCIE_ENET_R2D_CP

NC_SATA_A_D2RN		TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP		TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN		TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP		TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN		TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP		TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN		TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP		TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN		TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP		TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN		TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP		TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN		TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP		TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN		TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP		TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN		TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP		TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN		TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP		TRUE	TRUE	NC_SATA_F_R2D_CP

NC_USB_EXTCN		TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP		TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN		TRUE	TRUE	NC_USB_SDN
NC_USB_SDP		TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN		TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP		TRUE	TRUE	NC_USB_WLANP
NC_USB_6N		TRUE	TRUE	NC_USB_6N
NC_USB_6P		TRUE	TRUE	NC_USB_6P
NC_USB_7N		TRUE	TRUE	NC_USB_7N
NC_USB_7P		TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN		TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP		TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN		TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP		TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN		TRUE	TRUE	NC_USB_IRN
NC_USB_IRP		TRUE	TRUE	NC_USB_IRP

NC_ITPXDP_CLK100MN		TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP		TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L		TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2		TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3		TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1		TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2		TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3		TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L		TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK		TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA		TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L		TRUE	TRUE	NC_CLINK_RESET_L
NC_LPC_CLK33M_LPCPLUS_R		TRUE	TRUE	NC_LPC_CLK33M_LPCPLUS_R

NC_USB_SMCP		TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN		TRUE	TRUE	NC_USB_SMCN

NC_SMC_INTERFACE_2		TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

		NO_TEST	MAKE_BASE	
NC_TBT_XTAL25OUT		TRUE	TRUE	NC_TBT_XTAL25OUT

TP_DP_TBTSRC_ML_CP<3..0>		TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>		TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP		TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN		TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN

NC_DP_IG_D_AUXCHN		TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP		TRUE	TRUE	NC_DP_IG_D_AUXCHP

NC_PCIE_CLK100M_GPUN		TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP		TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N		TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P		TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN		TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP		TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN		TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP		TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN		TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP		TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN		TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP		TRUE	TRUE	NC_PCIE_CLK100M_SWP

NC_PCH_GPIO64_CLKOUTFLEX0		TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1		TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2		TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3		TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

NC_USB_4N		TRUE	TRUE	NC_USB_4N
NC_USB_4P		TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>	
TRUE	PCIE_TBT_R2D_N<3..0>	
TRUE	PCIE_TBT_D2R_C_P<3..0>	
TRUE	PCIE_TBT_D2R_C_N<3..0>	

TRUE	DMI_S2N_P<3..1>	
TRUE	DMI_S2N_N<3..1>	
TRUE	DMI_N2S_P<3..1>	
TRUE	DMI_N2S_N<3..1>	

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_D2R_P<1>	1	SM	BEAD-PROBE BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	1	SM	BEAD-PROBE BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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X425 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.053 MM	?
1X_DIELECTRIC	ISL5 ISL6 ISL7 ISL8 ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65 BGA

SYNC MASTER=SIDLE J45 SYNC DATE=12/10/2012

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
CPU 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CPU 27P4S	*	=27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	7 MIL	7 MIL
CPU 85D	*	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU AGTL	*	=STANDARD	?
CPU 8MIL	*	8 MIL	?
CPU COMP	*	20 MIL	?
CPU ITP	*	=2 1 SPACING	?
CPU VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU AGTL	TOP BOTTOM	=2x DIELECTRIC	?
CPU VID	*	0 457 MM	?
CPU VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG 2SAME	*	=3X DIELECTRIC	?
PEG TXRX	*	=6X DIELECTRIC	?
PEG 2OTHER	*	=4X DIELECTRIC	?
PEG 2CLK	*	=7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG 2SAME	TOP BOTTOM	=4X DIELECTRIC	?
PEG TXRX	TOP BOTTOM	=10X DIELECTRIC	?
PEG 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
PEG 2CLK	TOP BOTTOM	=10X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3 2SAME	*	=4X DIELECTRIC	?
PEG3 TXRX	*	=8X DIELECTRIC	?
PEG3 2OTHER	*	=5X DIELECTRIC	?
PEG3 2CLK	*	=8X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3 2SAME	TOP BOTTOM	=6X DIELECTRIC	?
PEG3 TXRX	TOP BOTTOM	=12X DIELECTRIC	?
PEG3 2OTHER	TOP BOTTOM	=8X DIELECTRIC	?
PEG3 2CLK	TOP BOTTOM	=12X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG3_*	=SAME	*	PEG3_2SAME
PEG3_R2D	PEG3_D2R	*	PEG3_TXRX
PEG3_*	*	*	PEG3_2OTHER
PEG3_*	CLK_*	*	PEG3_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 85D	*	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2SAME	*	=3x DIELECTRIC	?
DP 2OTHER	*	=4x DIELECTRIC	?
HDMICLK 2CLK	*	=7x DIELECTRIC	?
HDMICLK 2DP	*	=4x DIELECTRIC	?
HDMICLK 2OTHER	*	=7x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
DP 2OTHER	TOP BOTTOM	=6x DIELECTRIC	?
HDMICLK 2CLK	TOP BOTTOM	=10x DIELECTRIC	?
HDMICLK 2DP	TOP BOTTOM	=6x DIELECTRIC	?
HDMICLK 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra pair matching should be 0 127mm Inter pair matching should be within 2 54cm Max Length 241 3mm
DIsplayPort AUX CH intra pair matching should be 0 127mm Max length 330 2mm
SOURCE Calpella SFF DG Rev 1 5 (407364) and Family GPU DG 04202 001 v04
MAX LENGTH OF DISPLAYPORT/TMDS TRACES 13 INCHES

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 73
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 73
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 73
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 73
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 72
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 73
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 73
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 72
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 72
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 72
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 72
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 72
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 72
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 72
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTI	PM_THRMTRIP_L	6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		MEM_12MTI	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		MEM_12MTI	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 71 78
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 71
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 71 75 78
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 71 75 78

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_P<3..0>	5 35 71
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_N<3..0>	5 35 71
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_P<3..0>	5 35 71
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_N<3..0>	5 35 71
	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_P<3..0>	35
	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_N<3..0>	35
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 71
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 71
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 73
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 73
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 73
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 73
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 71
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 71

DP AUX NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 68 71
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 68 71
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	68 72 75
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	68 72 75
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	68
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	68
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	68 72 75
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	68 72 75
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 68 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 68 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	68 72
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	68 72

DP / HDMI NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	69 71 72
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	69 71 72
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 69 71 72
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 69 71 72
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 71
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 71
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 71
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 71
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
	DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 71
	DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 71
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
	DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 71
	DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 71

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PAGE TITLE: CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
SATA 37SE	*	37 OHM SE	=37 OHM SE	=37 OHM SE	=37 OHM SE	=37 OHM SE	=37 OHM SE
SATA 45SE	*	45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA 2SAME	*	=3X DIELECTRIC	?
SATA TXRX	*	=6X DIELECTRIC	?
SATA 2OTHER	*	=4X DIELECTRIC	?
SATA RCOMP	*	=6X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
SATA TXRX	TOP BOTTOM	=10X DIELECTRIC	?
SATA 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
SATA RCOMP	TOP BOTTOM	=10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH USB RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X DIELECTRIC	?
USB RBIAS	*	=6X DIELECTRIC	?
BT WAKE	*	=4X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	=6X DIELECTRIC	?
USB RBIAS	TOP BOTTOM	=10X DIELECTRIC	?
BT WAKE	TOP BOTTOM	=6X DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 2SAME	*	=3X DIELECTRIC	?
USB3 TXRX	*	=6X DIELECTRIC	?
USB3 2OTHER	*	=4X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
USB3 TXRX	TOP BOTTOM	=10X DIELECTRIC	?
USB3 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 73
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 73
I277	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 73
I277	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 73
I299	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 73
I299	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 73
I300	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 73
I300	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 73
I213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_EXTA	USB_85D	USB	USB_EXTA_P	13 38
	USB_EXTA	USB_85D	USB	USB_EXTA_N	13 38
I245	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	38
I247	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	38
I243	USB_EXTA	USB_85D	USB	USB_LT1_P	38
I244	USB_EXTA	USB_85D	USB	USB_LT1_N	38
	USB_NC	USB_85D	USB	NC_USB_EXTCP	13 73
	USB_NC	USB_85D	USB	NC_USB_EXTCN	13 73
I233	USB_NC	USB_85D	USB	NC_USB_SDP	13 73
I235	USB_NC	USB_85D	USB	NC_USB_SDN	13 73
I277		CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
I274		CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_SMC	USB_85D	USB	NC_USB_SMCP	73
	USB_SMC	USB_85D	USB	NC_USB_SMCN	73
I281	USB_NC	USB_85D	USB	NC_USB_6P	13 73
I281	USB_NC	USB_85D	USB	NC_USB_6N	13 73
I281	USB_NC	USB_85D	USB	NC_USB_7P	13 73
I281	USB_NC	USB_85D	USB	NC_USB_7N	13 73
	USB_EXTB	USB_85D	USB	USB_EXTB_P	13 69 72
	USB_EXTB	USB_85D	USB	USB_EXTB_N	13 69 72
I250	USB_NC	USB_85D	USB	NC_USB_EXTDP	13 73
I250	USB_NC	USB_85D	USB	NC_USB_EXTDN	13 73
	USB_BT	USB_85D	USB	USB_BT_P	13 34
	USB_BT	USB_85D	USB	USB_BT_N	13 34
		USB_85D	USB	USB_BT_CONN_P	34 72
		USB_85D	USB	USB_BT_CONN_N	34 72
I281	USB_NC	USB_85D	USB	NC_USB_IRP	13 73
I281	USB_NC	USB_85D	USB	NC_USB_IRN	13 73
I281	USB_TPAD	USB_85D	USB	USB_TPAD_P	13 39 72
I281	USB_TPAD	USB_85D	USB	USB_TPAD_N	13 39 72
I302		USB_85D	USB	USB_TPAD_R_P	
I303		USB_85D	USB	USB_TPAD_R_N	
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
I222	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
I223	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
I267		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
I268		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
I233	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
I222	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
I268		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
I268		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
I222	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 69 72
I223	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 69 72
I267		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
I268		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
I222	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	69 72
I223	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	69 72
I268		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 69
I268		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 69
I281	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 73
I281	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 73
I267		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 73
I267		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 73
I281	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 73
I281	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 73
I268		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 73
I267		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 73

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I256 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
I255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
I255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
I255 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
I253 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
I256	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

SYNC_MASTER=SIDLE J45 SYNC_DATE=12/10/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CLK LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?
SPI3X	*	=3x DIELECTRIC	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH SE	*	=2x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH SE	TOP BOTTOM	=3x DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
CLK PCIE 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE 2SAME	*	=2X DIELECTRIC	?
PCIE TXRX	*	=6X DIELECTRIC	?
PCIE 2OTHER	*	=4X DIELECTRIC	?
PCIE 2CLK	*	=7X DIELECTRIC	?
PCIECLK 2OTHER	*	=7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE 2SAME	TOP BOTTOM	=4X DIELECTRIC	?
PCIE TXRX	TOP BOTTOM	=10X DIELECTRIC	?
PCIE 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
PCIE 2CLK	TOP BOTTOM	=10X DIELECTRIC	?
PCIECLK 2OTHER	TOP BOTTOM	=10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41
	LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41
	SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 44 69 71 72
	SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 44 69 71 72
	SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
	SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
	SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
	SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
		HDA_45S	HDA	HDA_BIT_CLK_R	11
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
		HDA_45S	HDA	HDA_SYNC_R	11
		HDA_45S	HDA	HDA_RST_R_L	11
	HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
	HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
	HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
		HDA_45S	HDA	HDA_SDOUT_R	11 19
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 69 72
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 69 72
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 69 72
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 69 72
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 72
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 72
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
1304		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
1305		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
1275		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 72
1276		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 72
1275	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
1276	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
1277		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
1278		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
1279	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
1280	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
1281		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
1282		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
		CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
1283		CLK_LPC_45S	CLK_LPC	NC_LPC_CLK33M_LPCPLUS_R	11 73
1248	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
1252	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
1250	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
1253	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
1254	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
1255	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
1256	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
1257	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
1258	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
1259	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
1260	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
1600		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 72
1250		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 72
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
1535		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
1536		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
1287	PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
1288		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1315	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
1314	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
1316	PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
1317	PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
1309	PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 67 72
1307	PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 72
1311	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 72 77
1312	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 72 77
1313	PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 72
1310	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 72
1318	PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
1308	PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
1306	PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 72
1320	PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
1336	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CLK	50 72
1326	SPI_MLB	SPI_45S	SPI	SPI_CLK	50
1328	SPI_MLB	SPI_45S	SPI	SPI_CLK_R	13 50
1335	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CLK	50
1325	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CLK	41 50
1333	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CS_L	50 72
1329	SPI_MLB	SPI_45S	SPI	SPI_CS0_L	50
1330	SPI_MLB	SPI_45S	SPI	SPI_CS0_R_L	13 50
1327	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CS_L	50
1331	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CS_L	41 50
1338	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO1_MISO	50 72
1339	SPI_MLB	SPI_45S	SPI	SPI_MISO	13 50
1340	SPI_MLB	SPI_45S	SPI	SPI_MISO_R	50
1337	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO1_MISO	50
1332	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MISO	41 50
1386	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO0_MOSI	50 72
1324	SPI_MLB	SPI_45S	SPI	SPI_MOSI	50
1323	SPI_MLB	SPI_45S	SPI	SPI_MOSI_R	13 50
1322	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO0_MOSI	50
1321	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MOSI	41 50
1334	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_IO<2>	13 50
1342	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_MLB_IO2_WP_L	50
1341	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_ALT_IO2_WP_L	50 72
1343	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_IO<3>	13 50
1344	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_MLB_IO3_HOLD_L	50
1345	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_ALT_IO3_HOLD_L	50
1346	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_SCLK	39 71 72
1347	SPI_TPAD_CS	SPI_45S	SPI	TPAD_SPI_CS_L	39 71 72
1348	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MISO	39 71 72
1349	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MOSI	39 71 72

SYNC_MASTER=CLEAN X305 PEG SYNC_DATE=02/18/2014

PAGE TITLE: PCH Constraints 2

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 71 75
		MEM_PWR	PP0V75_S3_MEM_VREFCA 22 23 24 25 26 71 75
		MEM_PWR	PP1V35_S3_MEM 22 23 24 25 26 46 70

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP 2SAME	*	=3X DIELECTRIC	?
TBTDP TXRX	*	=6X DIELECTRIC	?
TBTDP 2OTHER	*	=4X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP 2SAME	TOP BOTTOM	=4x DIELECTRIC	?
TBTDP TXRX	TOP BOTTOM	=10X DIELECTRIC	?
TBTDP 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 73
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 73
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	*	=4X DIELECTRIC	?
MIPI 2CLK	*	=6X DIELECTRIC	?
MIPICLK 2OTHER	*	=7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	TOP BOTTOM	=6X DIELECTRIC	?
MIPI 2CLK	TOP BOTTOM	=8X DIELECTRIC	?
MIPICLK 2OTHER	TOP BOTTOM	=10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 36 37
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 36 37
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 36 37
T161	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 36 37
T162		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 37
T163	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 36 37
T164	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 36 37
T165	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 36 37
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 36 37
T166	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 36 37
T167	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 36 37
T168	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 36 37
T169	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 36 37
T147	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 36 37
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 36 37
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 36 37
T127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 36 37
T128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 36 37
T129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 37 72
T130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 37 72
T131	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 36 37
T132	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 36 37
T133		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 37 72
T134		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 37 72
T140			S2_MEM_PWR	PP1V35_CAM 36 37
T141			S2_MEM_PWR	PP0V675_CAM_VREF 36 37
T142			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 37
T143			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 37

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 72
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 72
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 68 71 72
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 68 71 72
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	41 44 56 57 72
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 72
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE 1TO1 50S	*	1 1_DIFFPAIR	50 OHM SE	50 OHM SE	50 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
THERM 1TO1 50S	*	1 1_DIFFPAIR	50 OHM SE	50 OHM SE	50 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
DIFFPAIR	*	1 1 DIFFPAIR			1 1 DIFFPAIR	1 1 DIFFPAIR	1 1 DIFFPAIR
AUDIODIFF	*	1 1_DIFFPAIR	0 1 MM	0 1 MM	10 MM	0 1 MM	0 1 MM
THERM 45S CPUVRISNS1	*	1 1_DIFFPAIR	45 OHM SE	45 OHM SE	45 OHM SE	0 2 MM	0 2 MM
THERM 1TO1 45S	*	1 1_DIFFPAIR	45 OHM SE	45 OHM SE	45 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
SENSE 1TO1 45S	*	1 1_DIFFPAIR	45 OHM SE	45 OHM SE	45 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	2X DIELECTRIC	?
THERM	*	2X DIELECTRIC	?
AUDIO	*	2X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU COMP	GND	*	GND P2MM
CPU VCCSENSE	GND	*	GND P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK PCIE	GND	*	GND P2MM
GND	PCIE *	*	GND P2MM
GND	SATA *	*	GND P2MM
USB	GND	*	GND P2MM
CLK PCIE	SB POWER	*	PWR P2MM
SB POWER	SATA *	*	PWR P2MM
USB	SB POWER	*	PWR P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND P2MM	*	0 20 MM	1000
PWR P2MM	*	0 20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

X425 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47 66
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47 66
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	47 68 82
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	47 68 82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	47 68 82
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	47 68 82
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PCH_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PCH_N	
	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
			DIFFERENTIAL PAIR	
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1 CPUVR_ISNS1_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1 CPUVR_ISNS1_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2 CPUVR_ISNS2_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2 CPUVR_ISNS2_N	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3 CPUVR_ISNS3_P	46 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3 CPUVR_ISNS3_N	46 59
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	82
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	82
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	46 62
	THERM_1TO1_45S	THERM	P1V05S0_CS_N	46 62
			DIFFERENTIAL PAIR	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_P	62
	THERM_1TO1_45S	THERM	P1V05S0_SENSE P1V05S0_SENSE_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMDP	28 48
	THERM_1TO1_45S	THERM	TBT_THERMDN	48
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
	AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

X425 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
	AUDIODIFF	AUDIO	RSUBIN_P	53
	AUDIODIFF	AUDIO	RSUBIN_N	53
	AUDIODIFF	AUDIO	LSUBIN_P	53
	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 72
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
	DIFFPAIR	AUDIO	HS_MIC_P	51 54
	DIFFPAIR	AUDIO	HS_MIC_N	51 54
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53

SB_POWER	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 66 67 70 71 72	
SB_POWER	PP3V3_S0	6 11 12 13 14 15 17 19 29 30 33 35 44 45 46 47 48 49 51 52 55 66 67 68	
SB_POWER	PP1V35_S3RS0_CPUDDR	70 72 8 10 21 66 67 70	
GND	GND		

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