1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J92 MLB NEWARK - DVT

11/21/2014

ALIASES RESOLVED

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00107	1	SCHEM,MLB-NEWARK,J92	SCH	CRITICAL	
820-00045	1	PCBF,MLB-NEWARK,J92	PCB	CRITICAL	

DRAWING TITLE: <PART_DESCRIPTION>

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,CCSAK,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS,EQ:4CH
MLB_MISC	CAM_FREQ:24M,CAM_XTAL:NO,EDP,RSMRST:SMC,PGOOD8:SLP_S4,SSD_LPSR:S3
MLB_DEBUG:ENG	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PVT	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PROD	XDP

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DRAM:HYN_2GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_2GB
DRAM:HYN_4GB_QDP	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB_QDP
DRAM:HYN_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_4GB
DRAM:HYN_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:HYNIX_8GB
DRAM:ELP_2GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_2GB
DRAM:ELP_4GB_QDP	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB_QDP
DRAM:ELP_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_4GB
DRAM:ELP_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4638	1	IC,MCU,LPC11U37,128KB/12KB,TFBGA48	U4600	CRITICAL	HPM:BLANK
341S00190	1	IC,HPM (VXXX) DVT,X261	U4600	CRITICAL	HPM:PROG
338S1231	1	IC,SMC12-B1,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00031	1	IC,SMC-B1,EXTERNAL (VXXXX) PROTO2A, J92	U5000	CRITICAL	SMC:PROG
335S1009	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_WIN:BLANK
335S1010	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S1029	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MIC:BLANK
341S00191	1	EFI ROM,MLB (VXXX) DVT,X261	U6100	CRITICAL	BOOTROM:PROG
335S0948	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLBGA	U8800	CRITICAL	SSDROM_WIN:BLANK
335S0966	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLCSP	U8800	CRITICAL	SSDROM_MAC:BLANK
341S00091	1	S1-X SSD BOOTROM, U164	U8800	CRITICAL	SSDROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00054	1	IC,CPU,BW,QGKE,QS,E0,2/2,0.8,4.5W,.8,B1234	U0500	CRITICAL	CPU:0.8GHZ
337S00099	1	IC,CPU,BW,QH2Z,PRQ,F0,2/2,1.1,5W,.85,B1234	U0500	CRITICAL	CPU:1.1GHZ
337S00098	1	IC,CPU,BW,QH2V,PRQ,F0,2/2,1.2,5W,.9,B1234	U0500	CRITICAL	CPU:1.2GHZ
337S00097	1	IC,CPU,BW,QH2R,PRQ,F0,2/2,1.3,5W,.9,B1234	U0500	CRITICAL	CPU:1.3GHZ
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7995	1	LABEL,BARCODE,2D,1D,CONFIG,MLB,X261	LABEL		

SSD POP Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S0243	1	POP,S1-X CONTROLLER+4GBITS ELP,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_ELP
339S0244	1	POP,S1-X CONTROLLER+4GBITS HYN,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_HYN
685-00003	1	POP,MLB,S1X-A1,ELP-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_ELP
685-00004	1	POP,MLB,S1X-A1,HYN-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_HYN
338S1288	1	IC,S1-X,CONTROLLER,A1,841(312)B,FCCSP	SSD_CTRL	CRITICAL	S1X:A1
338S00055	1	IC,S1-X,CONTROLLER,A2,841(312)B,FCBGA	SSD_CTRL	CRITICAL	S1X:A2
333S0733	1	IC,LPDDR2,128MX32,1.2V,ELPIDA 28NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:ELPIDA
333S0694	1	IC,LPDDR2,128MX32,1.2V,HYNIX 29NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:HYNIX
870-00878	1	TAPE,CONDUCTIVE,SSD,REEL,X261	SSD_TAPE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-6486	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S00028	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB_QDP
998-6453	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_2GB
998-6454	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB_QDP
333S0730	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0731	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0740	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0741	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_8GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
2GB	0	0
4GB QDP	0	1
4GB DDP	1	0
8GB	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00074	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
128S0393	128S0334		ALL	Kemet alt to Sanyo
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
197S0590	197S0588		ALL	Epson alt to TXC
197S0591	197S0588		ALL	NDK alt to TXC
107S0249	107S0251		ALL	TFT alt to Cyntec
138S0789	138S0941		ALL	Samsung alt to Murata
333S0700	333S0704		ALL	Hynix CAM DRAM alt to Elpida
333S00016	333S0704		ALL	Elpida new die CAM DRAM alt
333S00030	333S0704		ALL	Hynix new die CAM DRAM alt
339S0243	339S0244		ALL	Elpida SSD DRAM alt to Hynix
335S0948	335S0966		ALL	Winbond alt to Macronix
128S0631	128S0351		ALL	NEC alt to Sanyo
128S00008	128S0380		ALL	NEC alt to Sanyo
311S00007	311S0426		ALL	Sanyo alt to NEC
311S00008	311S0271		ALL	Samsung alt to Murata
311S00018	311S0409		ALL	Diodes alt to NXP
740S00004	740S0134		ALL	Kemet alt to Sanyo
740S00005	740S0190		ALL	Polytronics alt to Wayon
128S0296	128S0487		ALL	Sanyo alt to NEC
128S00012	128S0487		ALL	ROHM alt to NEC
128S00025	128S0469		ALL	Kemet alt to Sanyo
128S0374	128S0469		ALL	NEC alt to Sanyo
376S00007	376S1179		ALL	AOS alt to Vishay
376S1080	376S0820		ALL	Diodes alt to Onsemi
376S00036	376S1194		ALL	Vishay alt to Onsemi
376S00037	376S1193		ALL	Vishay alt to Onsemi
685-00004	685-00003	SSDRAM:A1_ELP	ALL	Hynix SSD DRAM alt to Elpida
337S00061	337S00054	CPU:0.8GHZ	ALL	2.4G turbo CPU alt to 2.0G

SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE: BOM Configuration

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Top level BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-6568	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6569	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6570	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6571	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6572	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6573	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6574	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6575	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6576	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6577	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6578	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6579	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6580	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6581	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6582	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6583	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6584	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6585	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6586	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6587	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6588	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6589	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6590	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6591	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6592	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6593	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6594	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6595	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6596	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6597	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6598	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6599	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6600	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6601	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6602	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6603	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6604	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6605	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6606	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6607	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6608	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6609	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6610	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6611	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6612	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6613	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6614	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6615	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP

Partial & development BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00014	CMN PTS,PCBA,MLB-NEWARK,J92	MLB_COMMON
685-00003	POP,MLB,S1X-A2,ELP-4GBIT,X261	S1X:A2,S1X_DRAM:ELPIDA
685-00004	POP,MLB,S1X-A2,HYN-4GBIT,X261	S1X:A2,S1X_DRAM:HYNIX
939-00043	PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261	ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG

Common BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00014	1	CMN PTS,PCBA,MLB-NEWARK,J92	CMNPTS	CRITICAL	CMN

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00196	1	BT ROM (VXX) DVT,2MBIT,X261	U3570	CRITICAL	BT:PROG
341S00197	1	WIFI ROM (PXXXX) DVT,WW1,X261	U3580	CRITICAL	WIFI:FCC
341S00198	1	WIFI ROM (PXXXX) DVT,WW2,X261	U3580	CRITICAL	WIFI:ETSI
341S00199	1	WIFI ROM (PXXXX) DVT,WW3,X261	U3580	CRITICAL	WIFI:APAC
341S00200	1	WIFI ROM (PXXXX) DVT,IND,X261	U3580	CRITICAL	WIFI:IND

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

PAGE TITLE: J92 BOM Variants

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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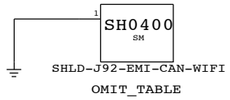
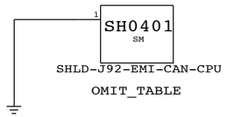
WIFI EMI CAN



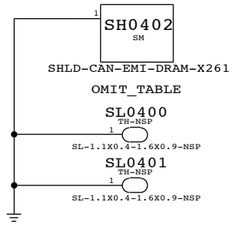
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-7064	1	CAN,EMI,WIFI,X261	SH0400	CRITICAL	

CPU EMI CAN



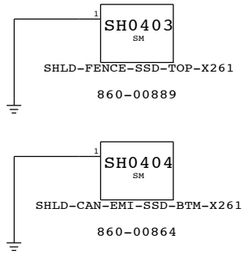
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00112	1	CAN,EMI,CPU,X261	SH0401	CRITICAL	

DRAM EMI CAN & SLOTs

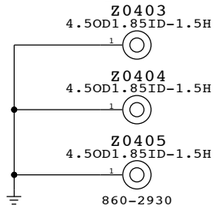


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00400	1	CAN,EMI,DRAM,TALL,X261	SH0402	CRITICAL	

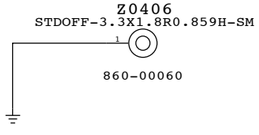
SSD EMI FENCE & CAN



CPU Heat Spreader Bosses



E85 BTB Connector Boss



SYNC MASTER=J43 MLB SYNC DATE=10/24/2012

PAGE TITLE: PD PARTS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(1 OF 20)

DP_TBTSNK0_ML_C_N<0>	AD25	DDI1_TXN[0]	
DP_TBTSNK0_ML_C_P<0>	AC25	DDI1_TXP[0]	
DP_TBTSNK0_ML_C_N<1>	AD26	DDI1_TXN[1]	
DP_TBTSNK0_ML_C_P<1>	AC26	DDI1_TXP[1]	
DP_TBTSNK0_ML_C_N<2>	AG25	DDI1_TXN[2]	
DP_TBTSNK0_ML_C_P<2>	AE25	DDI1_TXP[2]	
DP_TBTSNK0_ML_C_N<3>	AG26	DDI1_TXN[3]	
DP_TBTSNK0_ML_C_P<3>	AE26	DDI1_TXP[3]	
NC_DP_TBTSNK1_ML_CN<0>	AD22	DDI2_TXN[0]	
NC_DP_TBTSNK1_ML_CP<0>	AC22	DDI2_TXP[0]	
NC_DP_TBTSNK1_ML_CN<1>	AG22	DDI2_TXN[1]	
NC_DP_TBTSNK1_ML_CP<1>	AE22	DDI2_TXP[1]	
NC_DP_TBTSNK1_ML_CN<2>	AD21	DDI2_TXN[2]	
NC_DP_TBTSNK1_ML_CP<2>	AC21	DDI2_TXP[2]	
NC_DP_TBTSNK1_ML_CN<3>	AG21	DDI2_TXN[3]	
NC_DP_TBTSNK1_ML_CP<3>	AE21	DDI2_TXP[3]	

DDI / EDP

EDP_TXN0	AD17	DP_INT_ML_C_N<0>	
EDP_TXP0	AC17	DP_INT_ML_C_P<0>	
EDP_TXN1	AG18	DP_INT_ML_C_N<1>	
EDP_TXP1	AE18	DP_INT_ML_C_P<1>	
EDP_TXN2	AD18	DP_INT_ML_C_N<2>	
EDP_TXP2	AC18	DP_INT_ML_C_P<2>	
EDP_TXN3	AA17	DP_INT_ML_C_N<3>	
EDP_TXP3	W17	DP_INT_ML_C_P<3>	
EDP_AUXN	AG16	DP_INT_AUXCH_C_N	
EDP_AUXP	AE17	DP_INT_AUXCH_C_P	
EDP_RCOMP	AP41	MCP_EDP_RCOMP	
EDP_DISP_UTIL	Y21	TP_EDP_DISP_UTIL	

eDP Port Assignment:

Internal panel

PPVCOMP_S0_CPU

R0530
24.9
1% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(18 OF 20)

TP_ULX_SPARE1	CB11	RSVD_CB11		A44	TP_MCP_DC_A44
TP_ULX_SSP_SPARE	H15	RSVD_H15		C43	MCP_DC_C43_D44
NO_TEST				C45	TP_MCP_DC_C45
MCP_DC_H2_F3	F3	DAISY_CHAIN_NCTF_F3	DAISY_CHAIN_NCTF_F45	F45	
MCP_DC_F43_F45	F43	DAISY_CHAIN_NCTF_F43	DAISY_CHAIN_NCTF_D2	D2	TP_MCP_DC_D2
	H2	DAISY_CHAIN_NCTF_H2	DAISY_CHAIN_NCTF_D44	D44	
TP_MCP_DC_H44	H44	DAISY_CHAIN_NCTF_H44	DAISY_CHAIN_NCTF_F1	F1	TP_MCP_DC_F1

TRUE

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

NO_TEST

SYNC_MASTER=J92 WILL SYNC_DATE=04/10/2013

PAGE TITLE: CPU GFX/DC_TEST

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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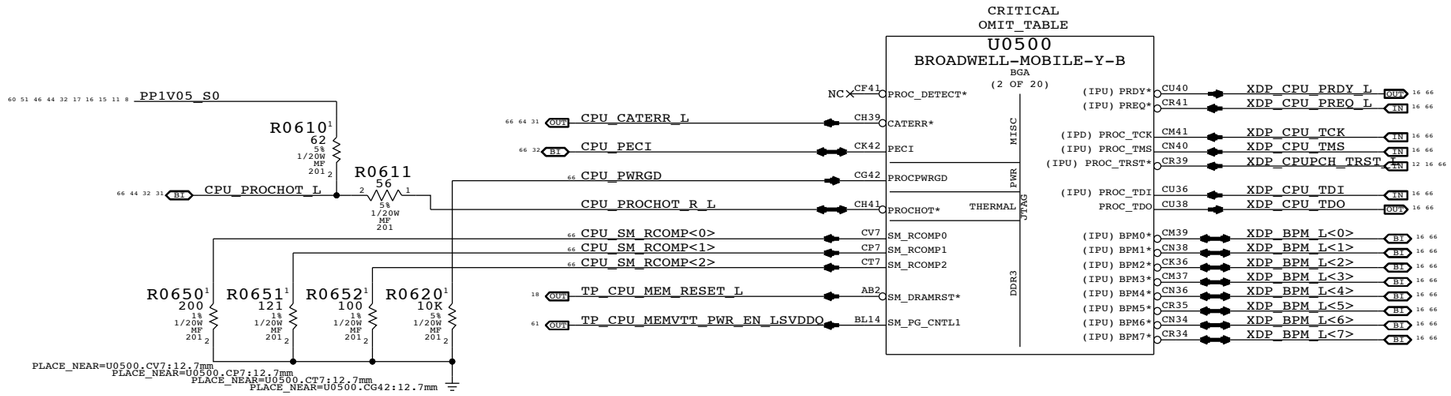
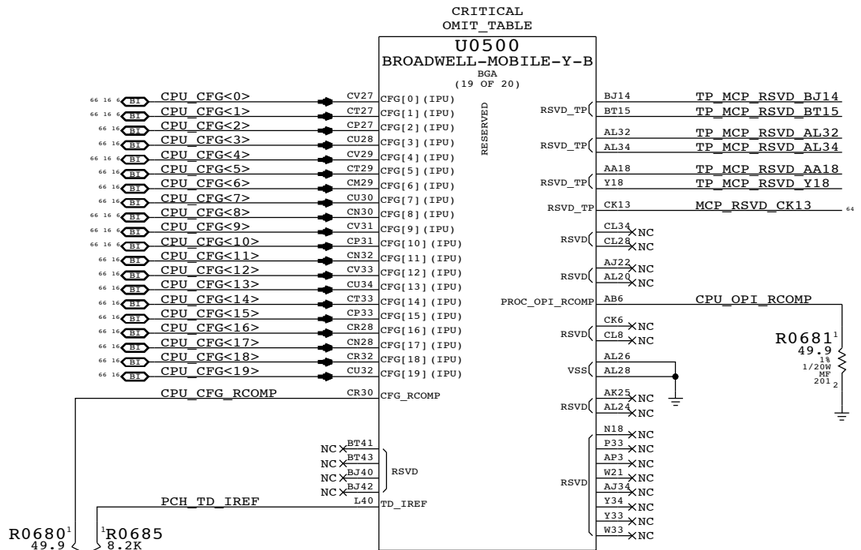
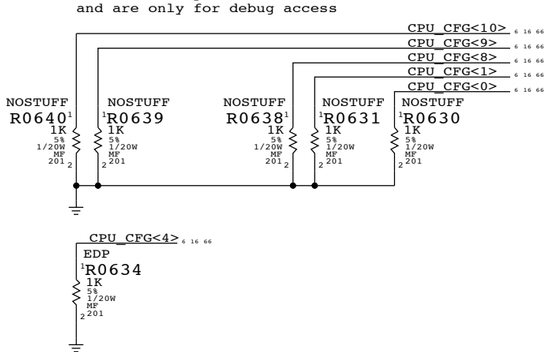




TBD: Confirm w/ Intel which still apply for BDW-Y

CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 =	POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 =	VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 =	NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 =	ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 =	PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 =	STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



SYNC MASTER=J92 WILL SYNC DATE=04/10/2013

PAGE TITLE
CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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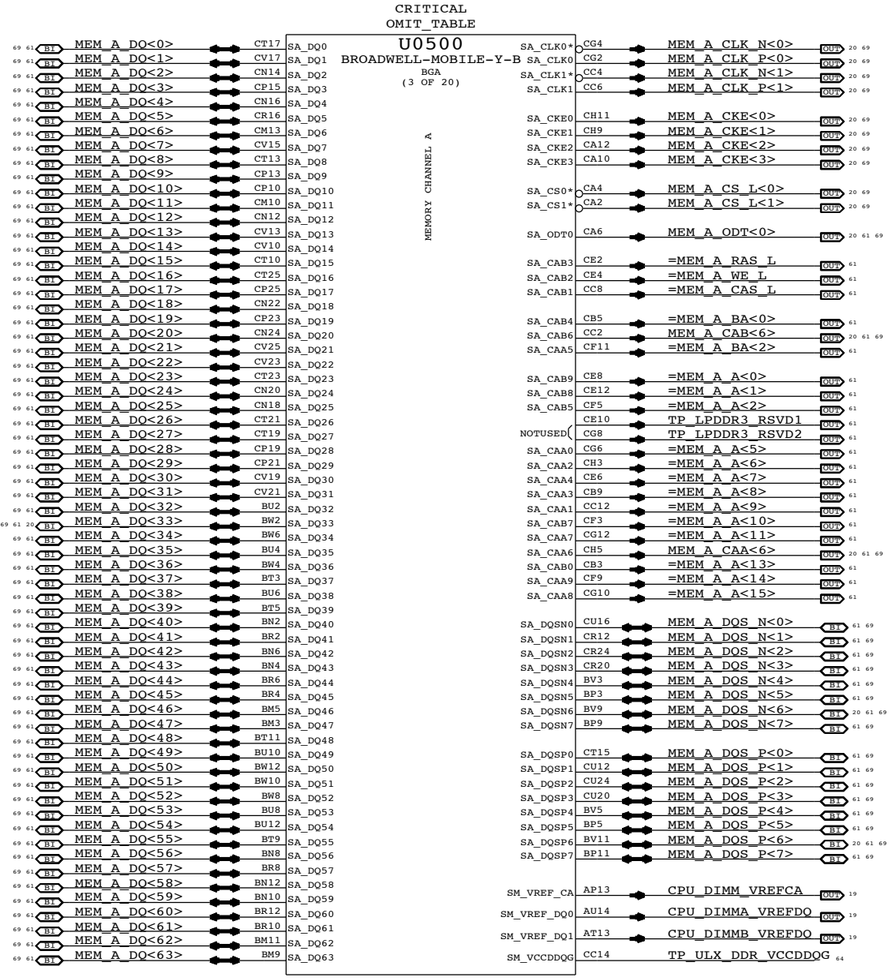

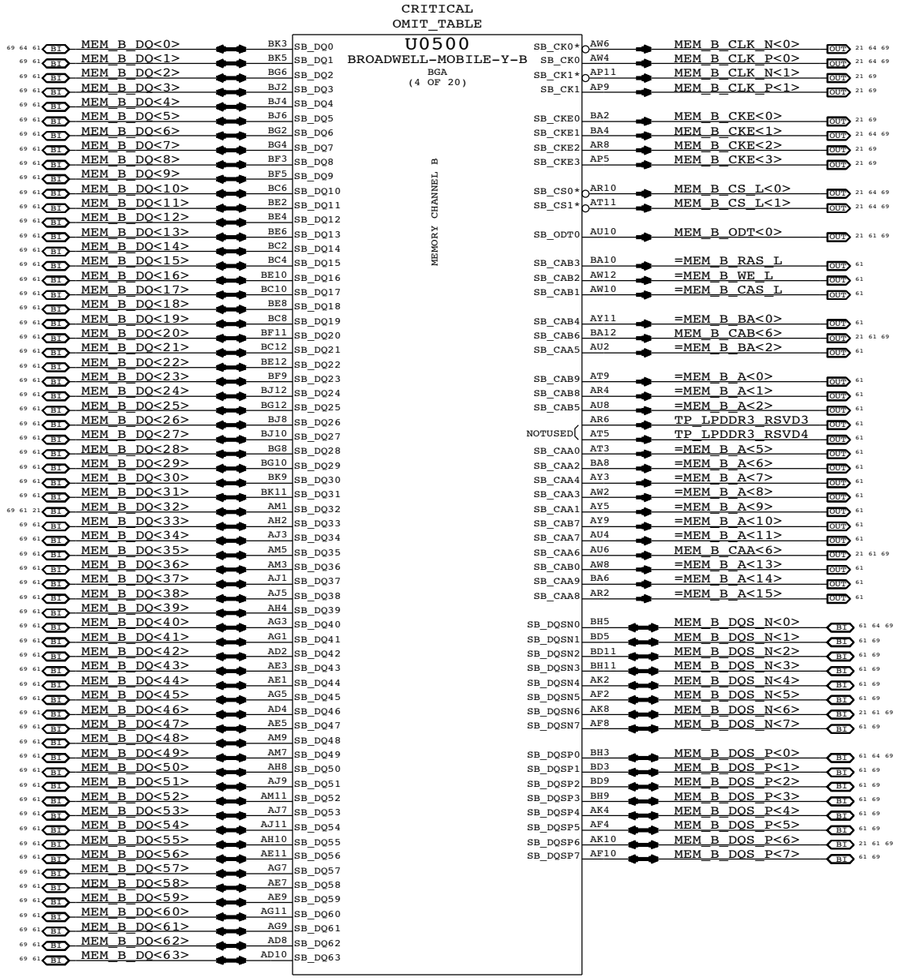

SYNC_MASTER=J92 LS MLB SYNC_DATE=07/17/2013

PAGE TITLE
CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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BRANCH <BRANCH>
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SHEET 7 OF 75

HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(12 OF 20)
BRW ULX POWER

1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)
PP1V2_S3
TP_MCP_DC_CY3
TP_MCP_DC_CW1
PPVCC_S0_CPU
R0860 100 5% 1/20W MF 201
PLACE_NEAR=U0500.CH45:50.8mm
CPU_VCCSENSE_P
TP_PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Max load: 300mA
PPVCOMP_S0_CPU
Max load: 300mA
PP1V05_S0
R0800 75 1% 1/20W MF 201
R0802 130 1% 1/20W MF 201
R0810 43 5% 1/20W MF 201
CPU_VIDALERT_L
R0811 0 5% 1/20W MF 0201
CPU_VIDSCLK
R0812 0 5% 1/20W MF 0201
CPU_VIDSOUT
R0802.2: PLACE_NEAR=U0500.CE40:2.54mm
R0810.2: PLACE_NEAR=U0500.CD43:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCST_PWRGD
CPU_VR_EN
CPU_VR_READY
R0850 10K 5% 1/20W MF 201
CPU_PWR_DEBUG_L
TP_MCP_RSVD_CJ22
TP_MCP_RSVD_CK23
TP_IVR_ERROR
TP_IST_TRIGGER
PPVCC_S0_CPU
32A Max
MCP_DC_CV45
TP_MCP_DC_CY44

CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(13 OF 20)
WPT LP POWER

PP1V05_S0SW_PCH_PCIE
PP1V05_S0SW_PCH_SATA
PP1V05_S0SW_PCH_USB3
PP1V05_S0
PP1V05_S0SW_PCH_VCCSATA3PLL
PP1V05_S0SW_PCH_VCCUSB3PLL
PP1V05_S0_PCH_VCCAPLL_OPI
PP1V05_SUS
PP1V5_S0
PP3V3_SUS
PP3V3_S5
PP3V3_S0
PP1V05_S0_PCH_VCC_ICC
PP1V05_S0_PCH_VCCACLKPLL
PP3V3_SUS
PP3V3_SUS
PPVRTC_G3H
C0892 0.1UF 10% 10V X5R-CERM 0201
C0891 0.1UF 10% 10V X5R-CERM 0201
C0890 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AA15::6.35mm
C0895 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U0500.AE15::6.35mm
BYPASS=U0500.V15::6.35mm
PP1V05_S0
???mA Max
PP3V3_S5
C0897 0.47UF 10% 6.3V CERM-X5R 0201
PLACE_NEAR=U0500.AG13:6.35mm
R0896 0 5% 1/20W MF 0201
PP1V05_S5_PCH_VCCDSW
MIN_LINE_WIDTH=0.7 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
PP1V05_S5_PCH_VCCDSW_R
MIN_LINE_WIDTH=0.7 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.05V
C0896 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AG13::6.35mm

SYNC_MASTER=J92_DEVMLB	SYNC_DATE=10/01/2013
PAGE TITLE	CPU/PCH POWER
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(14 OF 20)

AH29			AY13
AM19			AY15
AH6			AY39
AH31			BA44
AH30			BB3
AH33			BB5
AH32			BB7
AH34			BB9
AH44			BB11
AJ39			BB13
AJ30			BB15
AJ37			BB39
AK6			BC44
AJ18			BD1
AM17			BD7
AN6			BD13
AR42			BD15
AK12			BD39
AK21			BE40
AK27			BE42
BE44			BF7
AM13			BF13
BL8			BF15
CJ18			BF39
CJ24			BG14
AM21			BG44
AM23			BH1
AM25			BH7
AM27			BH13
AM29			BH15
AM31	VSS	VSS	BH39
AM35			BH41
CJ30			BH43
AM45			BJ44
CL5			BK7
AN2			BK13
AN4			BK15
CL24			BK39
AN8			BL2
AN10			BL4
AN12			BL6
AN14			BL10
AN40			BL12
AN42			BL40
AN44			BL42
AP7			BL44
AP15			BM1
AP43			BM7
CN1			BM13
AT1			BM39
AT7			BN44
AT15			BP13
AT39			CH1
AT45			CH15
AU44			CV39
AV13			CV41
AV15			CW12
AV39			CW14
AW44			CW16
CU1			CW18
AY1			AJ24
AY7			AP39
CV3			

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(15 OF 20)

L24		CW20
L16		AM39
H10		L32
H36		CN42
CN26		CP3
BP7		CP17
BP39		CP29
BR44		CR8
BT1		CR14
BT7		CR18
BT13		CR22
J16		CR26
BT39		CR37
BU44		CT31
BV7		CU8
BV13		CU14
BV15		CU18
BV39		CU22
BY1		CU26
BY3		CU42
BY5		CV35
BY7		CV37
BY9		CW5
BY11		CW8
BY13		CW22
BY15		CW24
BY39	VSS	CW26
C16		CW28
C20		CW32
C24		CW34
C28		CY7
C32	VSS	CY10
C36		D10
CB7		G28
CB13		J24
CB15		J28
CB39		CD9
CC40		CD5
CC42		CD3
CC44		CC10
CD1		CA8
CD7		AW14
CD13		AR14
CD15		AG39
CD39		BU40
CE44		BU42
CF7		L2
CF13		L20
CF15		L28
CG44		CD11
CH13		G32
CJ26		CW30
CK3		J20
CK10		J32
CK38		
CK44		
CL12		
CM15		
CM17		
CM19		
CM21		
CM23		
CM25		
CM31		
CM35		
CM43		
CN8		

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(20 OF 20)

T23		AD32
AR12		AH14
AU12		AH12
AV3		AG37
AV5		AG35
AV9		AG32
AC1		AG28
AC24		AG24
AC19		AG19
AH15		AF44
AB16		AF16
AB15		AF14
AB12		AF12
AB8		AF6
AA37		AE37
AA35		AE35
AC13		AE32
AA34		AE28
AA33		AE24
AA32		AE19
AA30		AE16
AA29		AD44
AA28		AD28
AB40		AD24
AA26		AD19
AA25	VSS	AD16
AA24		AD12
AA22		AD6
AA21	VSS	AC43
AA19		AC41
AA7		AC37
AA5		AC35
AA39		AC9
AA3		AC7
A40		AC3
A36		AB44
A20		AC28
A10		AD14
BM15		AC11
BP15		AC5
CN5		W18
CR5		W16
CU5		V44
W28		U20
W24		U14
W19		T19
AH22		AH28
AH21		AH27
AH20		AH26
AH19		AH25
AH17		AH23
		AV11
		AH16
		H4
		A16
		T29

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(16 OF 20)

U22		CH7
G20		V2
E20		E16
N24		U24
N28		R30
N32		N20
P35		AK15
R2		AM33
R4		AK44
R6		CA14
R8	VSS	U28
R10	VSS	U32
E24		V17
R16		V40
R22		R44
E28		T15
R24		F5
R26		G16
R28		R18
AV7		U26
E32		U34
E36		G24
R20		N16
		AJ13
		AC32
VSS_SENSE		CH43

CPU_VCCSENSE_N OUT

R0960
100
5% 1/20W MF 201
PLACE_NEAR=U0500.CH43:50.8mm

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(17 OF 20)

J43		CL32
J1		CL30
D42		CK33
A42		CK29
Y44		CJ34
W32		CG14
W35		CE14
Y2		BW14
Y12		BR14
Y14	VSS	BN14
Y16	VSS	AF36
W34		AA11
W30		Y19
T13		Y24
L38		Y28
Y42		Y32
A6		Y40
D4		J3
H42		J45

SYNC_MASTER=J92 WILL SYNC_DATE=04/10/2013

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 9 OF 75

All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 16x 10uF 0402 stuff, 12x 10uF 0402 nostuff

60 45 35 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402-1
CRITICAL C1001 10UF 20% 4V X6S 0402-1
CRITICAL C1002 10UF 20% 4V X6S 0402-1
CRITICAL C1003 10UF 20% 4V X6S 0402-1
CRITICAL C1004 10UF 20% 4V X6S 0402-1
NO STUFF C1005 10UF 20% 4V X6S 0402-1
NO STUFF C1006 10UF 20% 4V X6S 0402-1
CRITICAL C1007 10UF 20% 4V X6S 0402-1
NO STUFF C1008 10UF 20% 4V X6S 0402-1
CRITICAL C1009 10UF 20% 4V X6S 0402-1
C1011 10UF 20% 4V X6S 0402-1
C1012 10UF 20% 4V X6S 0402-1
NO STUFF C1013 10UF 20% 4V X6S 0402-1
C1014 10UF 20% 4V X6S 0402-1

NO STUFF C1015 10UF 20% 4V X6S 0402-1
CRITICAL C1016 10UF 20% 4V X6S 0402-1
NO STUFF C1017 10UF 20% 4V X6S 0402-1
CRITICAL C1018 10UF 20% 4V X6S 0402-1
CRITICAL C1019 10UF 20% 4V X6S 0402-1
CRITICAL C1020 10UF 20% 4V X6S 0402-1
NO STUFF C1021 10UF 20% 4V X6S 0402-1
CRITICAL C1022 10UF 20% 4V X6S 0402-1
CRITICAL C1023 10UF 20% 4V X6S 0402-1
NO STUFF C1025 10UF 20% 4V X6S 0402-1
C1026 10UF 20% 4V X6S 0402-1
NO STUFF C1027 10UF 20% 4V X6S 0402-1
NO STUFF C1028 10UF 20% 4V X6S 0402-1
NO STUFF C1029 10UF 20% 4V X6S 0402-1
C1030 12PF 5% 25V CERM 0201

CRITICAL C1031 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1032 210UF 20% 2.5V POLY-TANT CASE-B2S

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

59 52 46 21 20 19 8 69 60 PP1V2_S3

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

Added 2 extra 2.2uF per Harris Beach v0.9 schematic

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

SYNC_MASTER=J92 DEVMLB SYNC_DATE=10/01/2013

PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 10 OF 130
SHEET: 10 OF 75

PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
C1200 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AA1::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
C1202 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A24::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 20UF 20% 6.3V CERM-X5R 0402
BYPASS=U0500.U18::12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AC15::6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A32::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0
C1210 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U0500.W1::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 0.1UF 10% 6.3V X6S 0201
C1215 0.1UF 10% 6.3V X6S 0201
C1216 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.A30::12.7mm
BYPASS=U0500.A28::6.35mm
BYPASS=U0500.T27::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.AB36::6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe PWR)
PP1V05_S0SW_PCH_PCIE
C1260 1UF 20% 4V CERM-X6S 0201
C1266 0.1UF 10% 6.3V X6S 0201
C1267 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AB38::6.35mm
BYPASS=U0500.AB39::6.35mm
BYPASS=U0500.AB38::6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V SATA PWR)
PP1V05_S0SW_PCH_SATA
C1261 1UF 20% 4V CERM-X6S 0201
C1263 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.N45::6.35mm
BYPASS=U0500.N45::6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V USB3 PWR)
PP1V05_S0SW_PCH_USB3
C1262 1UF 20% 4V CERM-X6S 0201
C1268 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.AC45::6.35mm
BYPASS=U0500.AC45::6.35mm

PP1V05_S0
??mA Max
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603

PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max
C1270 20UF 20% 4V X5R-CERM 0402
C1271 20UF 20% 4V X5R-CERM 0402
C1273 20UF 20% 4V X5R-CERM 0402
C1274 20UF 20% 4V X5R-CERM 0402
C1272 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::12.7mm
BYPASS=U0500.AK35::6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V CERM-X6S 0402
C1257 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.Y22::12.7mm
BYPASS=U0500.Y22::6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NOSTUFF
C1250 20UF 20% 4V X5R-CERM 0402
C1251 0.1UF 10% 6.3V X6S 0201
C1252 0.1UF 10% 6.3V X6S 0201
BYPASS=U0500.T1::12.7mm
BYPASS=U0500.W14::6.35mm
BYPASS=U0500.N1::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AE13::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1220 1UF 20% 6.3V X5R 0201
C1221 1UF 20% 6.3V X5R 0201
C1222 1UF 20% 6.3V X5R 0201
C1223 1UF 20% 6.3V X5R 0201
C1224 1UF 20% 6.3V X5R 0201
C1225 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AJ26::6.35mm
BYPASS=U0500.AL39::6.35mm
BYPASS=U0500.AJ28::6.35mm
BYPASS=U0500.AL30::6.35mm
BYPASS=U0500.AK31::6.35mm
BYPASS=U0500.AK23::6.35mm

PCH VCCAIDLE BYPASS
PP1V05_S0
C1265 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T31::6.35mm

PCH VCC BYPASS
(PCH 1.05V SUS PWR)
PP1V05_SUS
C1229 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AG14::6.35mm

PCH VCC BYPASS
(PCH 1.05V SUS USB3 PWR)
PP1V05_SUS
C1226 10UF 20% 6.3V CERM-X6S 0402
C1227 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.U30::12.7mm
BYPASS=U0500.U30::6.35mm

PCH VCC BYPASS
(PCH 1.05V SUS PWR)
PP1V05_SUS
C1228 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.U16::6.35mm

PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
C1275 20UF 20% 4V X5R-CERM 0402
C1276 20UF 20% 4V X5R-CERM 0402
C1278 20UF 20% 4V X5R-CERM 0402
C1279 20UF 20% 4V X5R-CERM 0402
C1277 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::12.7mm
BYPASS=U0500.AL37::6.35mm

PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max
R1280 0 5% 1/10W MF-LF 603
NO STUFF C1280 20UF 20% 4V X5R-CERM 0402
NO STUFF C1281 20UF 20% 4V X5R-CERM 0402
NO STUFF C1288 20UF 20% 4V X5R-CERM 0402
NO STUFF C1289 20UF 20% 4V X5R-CERM 0402
C1282 1UF 20% 4V CERM-X6S 0201
C1283 1UF 20% 4V CERM-X6S 0201
C1284 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::12.7mm
BYPASS=U0500.AK19::6.35mm
BYPASS=U0500.AK17::6.35mm
BYPASS=U0500.AK29::6.35mm

PP1V05_S0SW_PCH_SATA
??mA Max
R1290 0 5% 1/10W MF-LF 603
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max
NOSTUFF C1290 20UF 20% 4V X5R-CERM 0402
NOSTUFF C1291 20UF 20% 4V X5R-CERM 0402
NOSTUFF C1292 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T33::12.7mm
BYPASS=U0500.T33::12.7mm
BYPASS=U0500.T33::6.35mm

PP1V05_S0SW_PCH_USB3
??mA Max
CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max
C1295 20UF 20% 4V X5R-CERM 0402
C1296 20UF 20% 4V X5R-CERM 0402
NOSTUFF C1297 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T35::12.7mm
BYPASS=U0500.T35::12.7mm
BYPASS=U0500.T35::6.35mm

PP1V05_SUS
??mA Max
R1285 0 5% 1/10W MF-LF 603
PCH VCCA OSC FILTER/BYPASS
(PCH 1.05V SUS VCCA OSC)
PP1V05_SUS_PCH_VCCAOSCSUS
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max
NO STUFF C1285 20UF 20% 4V X5R-CERM 0402
NO STUFF C1286 20UF 20% 4V X5R-CERM 0402
NO STUFF C1293 20UF 20% 4V X5R-CERM 0402
NO STUFF C1294 20UF 20% 4V X5R-CERM 0402
C1287 1UF 20% 4V CERM-X6S 0201
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::12.7mm
BYPASS=U0500.T21::6.21mm

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/23/2013
PAGE TITLE
PCH Decoupling
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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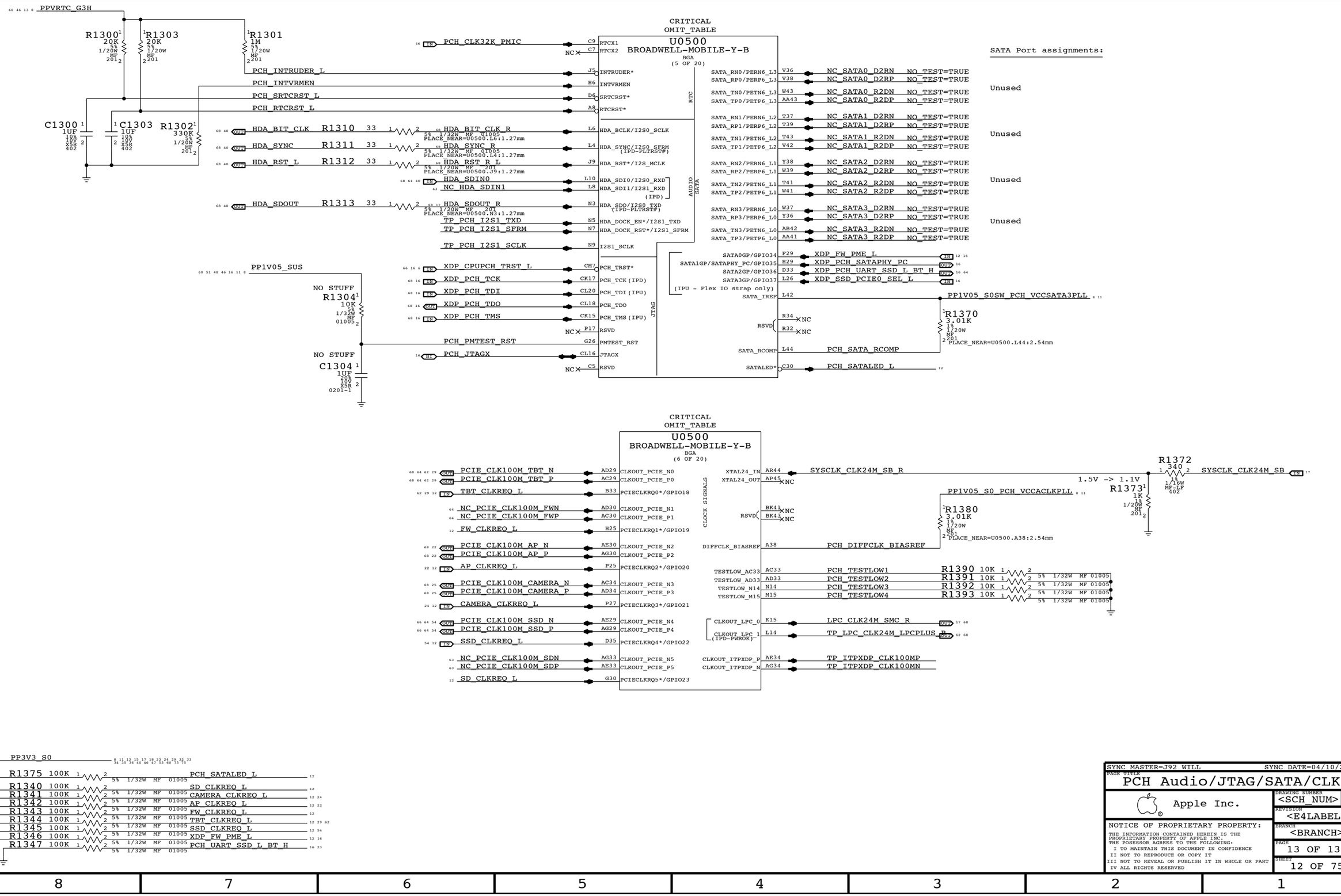

SYNC_MASTER=J92 WILL SYNC_DATE=04/10/2013

PAGE TITLE
PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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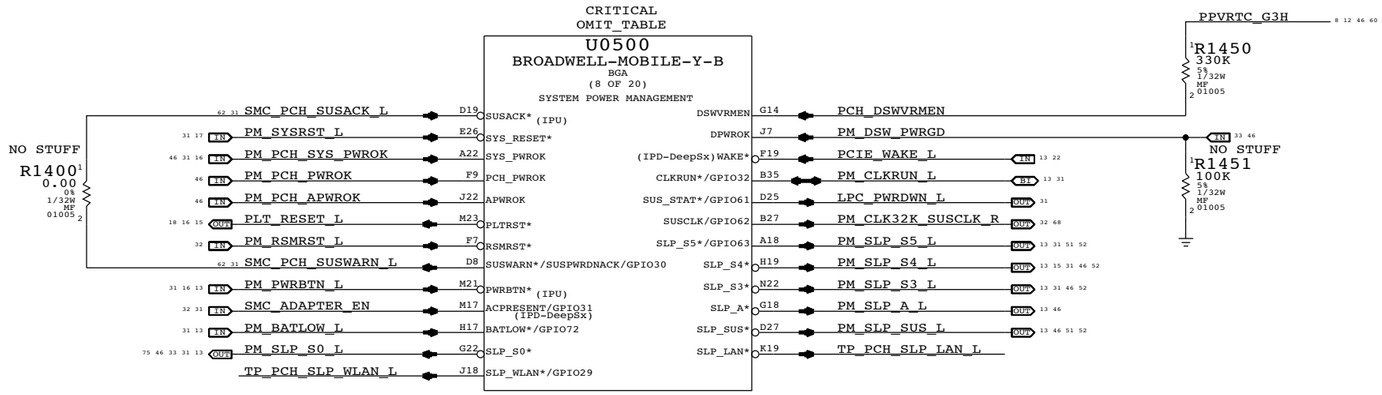

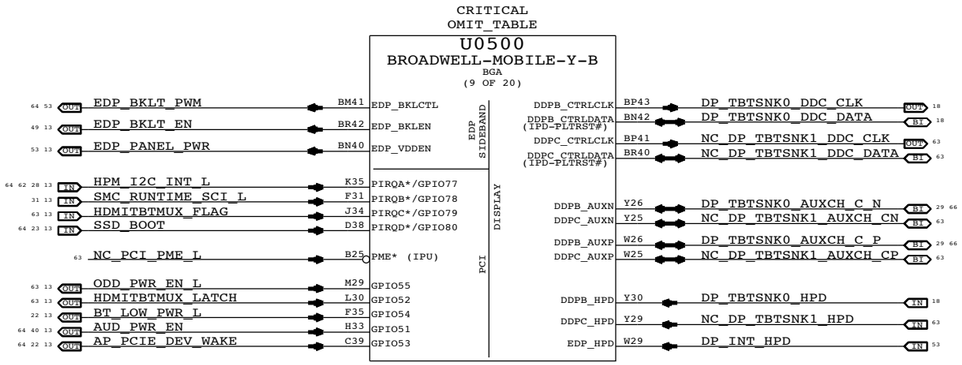

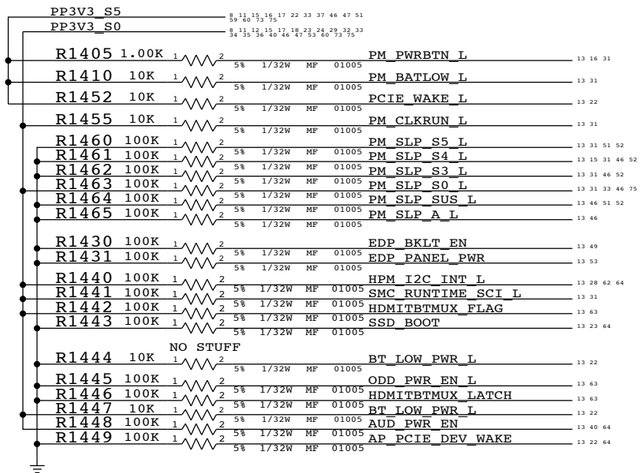

SYNC_MASTER=J92_WILL SYNC_DATE=04/10/2013

PAGE TITLE
PCH PM/PCI/GFX

Apple Inc.

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PCIe Port Assignments:

SSD lane 0
PCIE_SSD_D2R_N<0> AF40 PERN5_L0
PCIE_SSD_D2R_P<0> AG41 PERP5_L0
PCIE_SSD_R2D_C_N<0> AU40 PETN5_L0
PCIE_SSD_R2D_C_P<0> AU42 PETP5_L0

SSD lane 1
PCIE_SSD_D2R_N<1> AD40 PERN5_L1
PCIE_SSD_D2R_P<1> AE41 PERP5_L1
PCIE_SSD_R2D_C_N<1> AW40 PETN5_L1
PCIE_SSD_R2D_C_P<1> AW42 PETP5_L1

SSD lane 2
PCIE_SSD_D2R_N<2> AE43 PERN5_L2
PCIE_SSD_D2R_P<2> AD42 PERP5_L2
PCIE_SSD_R2D_C_N<2> BA42 PETN5_L2
PCIE_SSD_R2D_C_P<2> BA40 PETP5_L2

SSD lane 3
PCIE_SSD_D2R_N<3> AF42 PERN5_L3
PCIE_SSD_D2R_P<3> AG43 PERP5_L3
PCIE_SSD_R2D_C_N<3> BB41 PETN5_L3
PCIE_SSD_R2D_C_P<3> BB43 PETP5_L3

AirPort
PCIE_AP_D2R_N AD38 PERN3
PCIE_AP_D2R_P AC39 PERP3
PCIE_AP_R2D_C_N AY41 PETN3
PCIE_AP_R2D_C_P AY43 PETP3

Camera
PCIE_CAMERA_D2R_N AH38 PERN4
PCIE_CAMERA_D2R_P AH40 PERP4
PCIE_CAMERA_R2D_C_N AV41 PETN4
PCIE_CAMERA_R2D_C_P AV43 PETP4

Thunderbolt lane 0
PCIE_TBT_D2R_N<0> AP38 PERN1/USB3RN3
PCIE_TBT_D2R_P<0> AE39 PERP1/USB3RP3
PCIE_TBT_R2D_C_N<0> BD41 PETN1/USB3TN3
PCIE_TBT_R2D_C_P<0> BD43 PETP1/USB3TP3

Thunderbolt lane 1
USB3_EXTD_D2R_N AH42 PERN2/USB3RN4
USB3_EXTD_D2R_P AJ43 PERP2/USB3RP4
USB3_EXTD_R2D_C_N BC40 PETN2/USB3TN4
USB3_EXTD_R2D_C_P BC42 PETP2/USB3TP4

NC AT41
NC AT43
RSVD

PCH_PCIE_RCOMP F41 PCIE_RCOMP
C41 PCIE_IREF
PP1V05_S0SW_PCH_VCCUSB3PLL
R1500 3.01K 1% 1/20W MF 201
PLACE_NEAR=U0500.F41:2.54mm

CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(11 OF 20)
PCI-E
USB

USB Port Assignments:

Ext A (LS/FS/HS)
USB2N0 W12 USB_EXTA_N
USB2P0 V12 USB_EXTA_P

Ext B (LS/FS/HS)
USB2N1 T9 NC_USB_EXTBN
USB2P1 V10 NC_USB_EXTBP

BT
USB2N2 Y10 USB_BT_N
USB2P2 Y8 USB_BT_P

IR
USB2N3 AB10 NC_USB_IRN
USB2P3 AA9 NC_USB_IRP

Trackpad
USB2N4 W9 NC_USB_TPADN
USB2P4 W7 NC_USB_TPADP

Unused
USB2N5 V8 TP_USB_5N
USB2P5 T7 TP_USB_5P

Reserved: Camera
USB2N6 V6 NC_USB_CAMERAN
USB2P6 T5 NC_USB_CAMERAP

Reserved: SD (HS)
USB2N7 Y6 NC_USB_SDN
USB2P7 W5 NC_USB_SDP

Unused
USB2N8 V4 TP_USB_8N
USB2P8 T3 TP_USB_8P

Unused
USB2N9 Y4 TP_USB_9N
USB2P9 W3 TP_USB_9P
(IPD)

USB3 Port Assignments:

Ext A (SS)
USB3RN1 AJ41 USB3_EXTA_D2R_N
USB3RP1 AM41 USB3_EXTA_D2R_P
USB3TN1 BG42 USB3_EXTA_R2D_C_N
USB3TP1 BG40 USB3_EXTA_R2D_C_P

Unused
USB3RN2 AM43 NC_USB3_EXTB_D2RN
USB3RP2 AK42 NC_USB3_EXTB_D2RP
USB3TN2 BF41 NC_USB3_EXTB_R2D_CN
USB3TP2 BF43 NC_USB3_EXTB_R2D_CP

USBRBIAS* B13 PCH_USB_RBIAS
USBRBIAS D13
PLACE_NEAR=U0500.B13:2.54mm
R1570 22.6 1% 1/20W MF 201

RSVD H13 NC
RSVD F13 NC

OC0*/GPIO40 E18 XDP_USB_EXTA_OC_L
OC1*/GPIO41 E22 XDP_USB_EXTB_OC_L
OC2*/GPIO42 H21 XDP_USB_EXTC_OC_L
OC3*/GPIO43 D21 XDP_USB_EXTD_OC_L

CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(7 OF 20)
LPC
SMBUS
SPI
C-LINK

LPC_AD<0> R1540 33 5% 1/32W MF 01005 LPC_AD_R<0>
LPC_AD<1> R1541 33 5% 1/20W MF 201 LPC_AD_R<1>
LPC_AD<2> R1542 33 5% 1/32W MF 01005 LPC_AD_R<2>
LPC_AD<3> R1543 33 5% 1/32W MF 01005 LPC_AD_R<3>
LPC_FRAME_L R1544 33 5% 1/32W MF 01005 LPC_FRAME_R_L

(IPU) LAD0 P13
LAD1 M13
LAD2 R14
LAD3 K13
LFRAME* P15

SPI_CLK_R C26 SPI_CLK (IPU)
SPI_CS0_R_L H27 SPI_CS0* (IPU)
TP_SPI_CS1_L M27 SPI_CS1* (IPU)
TP_SPI_CS2_L K27 SPI_CS2* (IPU)
SPI_MOSI_R D31 SPI_MOSI (IPU/IPD)
SPI_MISO B23 SPI_MISO (IPU)
SPI_IO<2> F27 SPI_IO2 (IPU)
SPI_IO<3> J26 SPI_IO3 (IPU)

SMBALERT*/GPIO11 K21 PCH_SMBALERT_L
SMBCLK P21 SMBUS_PCH_CLK
SMBDATA B21 SMBUS_PCH_DATA
SML0ALERT*/GPIO60 F21 WOL_EN
SML0CLK P19 SML_PCH_0_CLK
SML0DATA B19 SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO73 H8 PCH_SML1ALERT_L
SML1CLK/GPIO75 C14 SMBUS_SMC_1_S0_SCL
SML1DATA/GPIO74 A14 SMBUS_SMC_1_S0_SDA

(IPU/IPD) CL_CLK D23 NC_CLINK_CLK
(IPU/IPD) CL_DATA H23 NC_CLINK_DATA
CL_RST* K23 NC_CLINK_RESET_L

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

PP3V3_SUS
PP3V3_SUS
R1580 100K 5% 1/32W MF 01005 XDP_USB_EXTA_OC_L
R1581 100K 5% 1/32W MF 01005 XDP_USB_EXTB_OC_L
R1582 100K 5% 1/32W MF 01005 XDP_USB_EXTC_OC_L
R1583 100K 5% 1/32W MF 01005 XDP_USB_EXTD_OC_L
R1548 1.00K 5% 1/32W MF 01005 SPI_IO<2>
R1549 1.00K 5% 1/32W MF 01005 SPI_IO<3>
R1590 100K 5% 1/32W MF 01005 PCH_SMBALERT_L
R1591 100K 5% 1/32W MF 01005 WOL_EN

SYNC_MASTER=J92_DEVMLB SYNC_DATE=06/28/2013
PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H R1631 100K 5% 1/20W MF 201
RAMCFG2:H R1636 100K 5% 1/20W MF 201
RAMCFG1:H R1635 100K 5% 1/20W MF 201
RAMCFG0:H R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

PM_SLP_S4_L

SSD_LPSR:S3
R1634 100K 5% 1/32W MF 01005

CRITICAL
OMIT_TABLE

U0500
BROADWELL-MOBILE-Y-B
BGA
(10 OF 20)

XDP_PCH_USB3PHY_PC	J30	BMBUSY*/USB3PHY_PC/GPIO76
XDP_MLB_RAMCFG0	C18	GPIO8
PCH_GPIO12	J14	LAN_PHY_PWR_CTRL/GPIO12
TP_MEM_VDD_SEL_1V5_L	K25	GPIO15 (IPD-RSMRST#)
XDP_LPCPLUS_GPIO	N26	GPIO16
XDP_PCH_GPIO17	H31	GPIO17
SD_RESET_L	C22	GPIO24
SMC_WAKE_SCI_L	K17	GPIO27 (IPD-DeepSx)
TPAD_SPI_INT_L	M25	GPIO28
TPAD_USB_IF_EN	B15	GPIO26
SSD_PWR_EN	F25	GPIO56
PCH_TBT_PCIE_RESET_L	F23	GPIO57
AUD_WAKE_L	F15	GPIO58
XDP_SDCONN_STATE_CHANGE_L	D15	GPIO59
SD_PWR_EN	L18	GPIO44
TBT_PWR_EN	B29	GPIO47
XDP_JTAG_ISP_TCK	K29	GPIO48
XDP_JTAG_ISP_TDI	B31	GPIO49
JTAG_TBT_TMS_PCH	F33	GPIO50
PCH_PCIEPHY_PC	D29	HSIOPC/PCIEPHY_PC/GPIO71
TPAD_SPI_IF_EN	E14	GPIO13
XDP_MLB_RAMCFG3	M19	GPIO14
SPIROM_USE_MLB	F17	GPIO25
CAMERA_PWR_EN	P23	GPIO45
	L22	GPIO46
XDP_MLB_RAMCFG1	D17	GPIO9
XDP_MLB_RAMCFG2	B17	GPIO10
SSD_SR_EN_L	E30	DEVSLP0/GPIO33
AP_S0IX_WAKE_SEL	R36	SDIO_POWER_EN/GPIO70
SSD_RESET_L	K31	DEVSLP1/GPIO38
CAMERA_RESET_L	J41	DEVSLP2/GPIO39
PCH_TCO_TIMER_DISABLE	A34	SPKR/GPIO81 (IPD-PLTRST#)

PLT_RESET_L
R1621 100K 5% 1/32W MF 01005

R1639 100K 5% 1/32W MF 01005
R1629 100K 5% 1/32W MF 01005

PP3V3_S0
R1641 1.00K 5% 1/32W MF 01005

PP1V05_S0
R1650 1.00K 5% 1/32W MF 01005

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE_NEAR=U0500.AB4:2.54mm
R1655 49.9 1% 1/20W MF 201

CPU/MISC

THERMTRIP*	CG40	PM_THRMTRIP_L
RCIN*/GPIO82	C34	TBT_CIO_PLUG_EVENT_L
SERIRQ	E34	LPC_SERIRQ
PCH_OPI_RCOMP	AB4	PCH_OPI_COMP
RSVD	AJ14	NC
	AL18	NC

GPIO

GSPI0_CS*/GPIO83	D40	MIKEY_SPI_CS_L
GSPI0_CLK/GPIO84	G34	MIKEY_SPI_CLK
GSPI0_MISO/GPIO85 (IPD)	L36	MIKEY_SPI_MISO
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	K33	MIKEY_SPI_MOSI
GSPI1_CS*/GPIO87	L34	TPAD_SPI_CS_L
GSPI1_CLK/GPIO88	M31	TPAD_SPI_CLK
GSPI1_MISO/GPIO89 (IPD)	F37	TPAD_SPI_MISO
GSPI_MOSI/GPIO90	H35	TPAD_SPI_MOSI
UART0_RXD/GPIO91	M35	PCH_BT_UART_D2R
UART0_TXD/GPIO92	F39	PCH_BT_UART_R2D
UART0_RTS*/GPIO93	N43	PCH_BT_UART_RTS_L
UART0_CTS*/GPIO94	N41	PCH_BT_UART_CTS_L
UART1_RXD/GPIO0	P29	PCH_UART1_D2R
UART1_TXD/GPIO1	H38	PCH_UART1_R2D
UART1_RST*/GPIO2	N39	JTAG_ISP_TDO
UART1_CTS*/GPIO3	N30	PCH_UART1_CTS_L

LPIO

I2C0_SDA/GPIO4	N36	AP_S0IX_WAKE_L
I2C0_SCL/GPIO5	R42	AP_RESET_L
I2C1_SDA/GPIO6	J37	I2C_PCH_1_SDA
I2C1_SCL/GPIO7	M33	I2C_PCH_1_SCL
SDIO_CLK/GPIO64	N34	QR_SWITCH_EN
SDIO_CMD/GPIO65	H40	BT_PWRRST_L
SDIO_D0/GPIO66 (IPD-PLTRST#)	R40	PCH_STRP_TOPBLK_SWP_L
SDIO_D1/GPIO67	R38	ENET_MEDIA_SENSE
SDIO_D2/GPIO68	J39	LCD_IRQ_L
SDIO_D3/GPIO69	P31	LCD_PSR_EN

PLT_RESET_L
R1691 100K 5% 1/32W MF 01005

Requires connection to SMC via 1K series R

PP3V3_S5
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_SUS
PP3V3_S0
PP3V3_S0

R1608 100K	PCH_SATAPHY_PC	
R1609 100K	PCH_PCIEPHY_PC	
R1610 100K	PCH_USB3PHY_PC	
R1613 100K	BT_PWRRST_L	
R1612 100K	PCH_GPIO12	
R1614 100K	XDP_LPCPLUS_GPIO	
R1615 100K	XDP_PCH_GPIO17	
R1616 100K	SD_RESET_L	
R1617 100K	SMC_WAKE_SCI_L	
R1618 100K	TPAD_SPI_INT_L	
R1619 100K	TPAD_USB_IF_EN	

SSD_LPSR:S0

R1620 100K	SSD_PWR_EN	
R1622 100K	AUD_WAKE_L	
R1623 100K	XDP_SDCONN_STATE_CHANGE_L	
R1624 100K	SD_PWR_EN	
R1625 100K	TBT_PWR_EN	
R1626 100K	XDP_JTAG_ISP_TCK	
R1627 100K	XDP_JTAG_ISP_TDI	
R1628 100K	JTAG_TBT_TMS_PCH	
R1630 100K	TPAD_SPI_IF_EN	
R1632 100K	SPIROM_USE_MLB	
R1633 100K	CAMERA_PWR_EN	
R1637 100K	SSD_SR_EN_L	
R1638 100K	AP_S0IX_WAKE_SEL	
R1640 100K	QR_SWITCH_EN	
R1652 10K	LPC_SERIRO	
R1693 100K	ENET_MEDIA_SENSE	
R1694 10K	LCD_IRQ_L	
R1695 100K	LCD_PSR_EN	

All: 5% 1/32W MF 01005

PP3V3_S0

MIKEY_SPI_CS_L	R1660 47.0K	
MIKEY_SPI_CLK	R1661 47.0K	
MIKEY_SPI_MISO	R1662 47.0K	
MIKEY_SPI_MOSI	R1663 47.0K	
TPAD_SPI_CS_L	R1664 47K	
TPAD_SPI_CLK	R1665 47K	
TPAD_SPI_MISO	R1666 47K	
TPAD_SPI_MOSI	R1667 47K	
PCH_BT_UART_D2R	R1668 47.0K	
PCH_BT_UART_R2D	R1669 47.0K	
PCH_BT_UART_RTS_L	R1670 47.0K	
PCH_BT_UART_CTS_L	R1671 47.0K	
PCH_UART1_D2R	R1672 47.0K	
PCH_UART1_R2D	R1673 47.0K	
JTAG_ISP_TDO	R1674 100K	
PCH_UART1_CTS_L	R1675 47.0K	
AP_S0IX_WAKE_L	R1676 100K	
TBT_CIO_PLUG_EVENT_L	R1677 100K	
I2C_PCH_1_SDA	R1678 10K	
I2C_PCH_1_SCL	R1679 10K	

All: 5% 1/32W MF 01005 (R1664–R1667: 5% 1/20W MF 201)

SYNC MASTER=J92_DEVMLB SYNC DATE=08/14/2013

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Extra BPM Probepoints

XDP_BPM_L<2> → PP1802
XDP_BPM_L<3> → PP1803
XDP_BPM_L<4> → PP1804
XDP_BPM_L<5> → PP1805
XDP_BPM_L<6> → PP1806
XDP_BPM_L<7> → PP1807
(P2MM SM)

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

R1830 150 5% 1/20W MF 201

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>

XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4 → NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5 → NC
	VCC_OBS_AB	VCC_OBS_CD
CPU_PWR_DEBUG_L	HOOK2	RESET#/HOOK6 → XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7 → XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO → XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn ← XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI ← XDP_PCH_TDI
	TCK0	TMS ← XDP_PCH_TMS
		XDP_PRESENT# → XDP_CPU_PRESENT_L

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05_S0
XDP_CPU_TDO — R1810 51 — XDP — PLACE_NEAR=U0500.CU38:28mm
XDP_CPU_TCK — R1813 51 — XDP — PLACE_NEAR=U0500.CM41:28mm
TDI and TMS are terminated in CPU.

CPU_VCCST_PWRGD — R1800 1K — XDP — PLACE_NEAR=U0500.BU14:2.54mm
PM_PWRBTN_L — R1802 0 — XDP — PLACE_NEAR=U5000.K1:2.54mm
PM_PCH_SYS_PWROK — R1804 0 — XDP
XDP_CPU_TCK
PCH_JTAGX — R1835 0 — XDP — PLACE_NEAR=J1800.58:28mm
(5% 1/20W MF 0201)

C1804 0.1UF 10% 6.3V CERM-X5R 0201 — XDP
R1831 1K 5% 1/20W MF 201 — XDP
C1800 0.1UF 10% 6.3V CERM-X5R 0201 — XDP
C1801 0.1UF 10% 6.3V CERM-X5R 0201 — XDP
C1806 0.1UF 10% 6.3V CERM-X5R 0201 — XDP

XDP_CPU_PRESENT_L
NOSTUFF
R1832 0 5% 1/20W MF 0201

R1805 1K — XDP — PLT_RESET_L — PLACE_NEAR=U0500.AG7:2.54mm
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CRITICAL
Q1840 DMN5L06VK-7 SOT563 VER — XDP
PLACE_NEAR=J1800.55:28mm
XDP_CPU_TDO

CRITICAL
Q1840 DMN5L06VK-7 SOT563 VER — XDP
PLACE_NEAR=J1800.55:28mm
XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)
XDP_CPUPCH_TRST_L

CRITICAL
Q1842 DMN5L06VK-7 SOT563 VER — XDP
PLACE_NEAR=J1800.55:28mm
XDP_CPU_TDI

CRITICAL
Q1842 DMN5L06VK-7 SOT563 VER — XDP
PLACE_NEAR=J1800.55:28mm
XDP_CPU_TMS

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC, A, Y)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS
PCH_JTAGX — R1899 1K — NO STUFF — PLACE_NEAR=U0500.CL16:28mm
XDP_PCH_TDO — R1890 51 — XDP — PLACE_NEAR=U0500.CL18:28mm
XDP_PCH_TDI — R1891 51 — XDP — PLACE_NEAR=U0500.CL20:28mm
XDP_PCH_TMS — R1892 51 — XDP — PLACE_NEAR=U0500.CK15:28mm
XDP_PCH_TCK — R1896 51 — NO STUFF — PLACE_NEAR=U0500.CK17:28mm
XDP_CPUPCH_TRST — R1897 51 — NO STUFF — PLACE_NEAR=U0500.CM7:28mm
(5% 1/20W MF 201)

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0		
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	→ PP1873	
XDP_USB_EXTD_OC_L	→ PP1874	
XDP_SDCONN_STATE_CHANGE_L	→ PP1875	
XDP_MLB_RAMCFG1		
XDP_MLB_RAMCFG2		
XDP_MLB_RAMCFG3		
XDP_JTAG_ISP_TCK	→ PP1879	
XDP_FW_PME_L	→ PP1880	
XDP_PCH_SATAPHY_PC	R1881 SHORT — OMIT	PCH_SATAPHY_PC
XDP_PCH_UART_SSD_L_BT_H	R1882 SHORT — OMIT	PCH_UART_SSD_L_BT_H
XDP_SSD_PCIE0_SEL_L	R1883 1K (5% 1/20W MF 201)	
XDP_LPCPLUS_GPIO	→ PP1884	
XDP_PCH_GPIO17	→ PP1885	
XDP_PCH_USB3PHY_PC	R1886 SHORT — OMIT	PCH_USB3PHY_PC
XDP_JTAG_ISP_TDI	→ PP1887	

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

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PAGE TITLE: CPU/PCH Merged XDP

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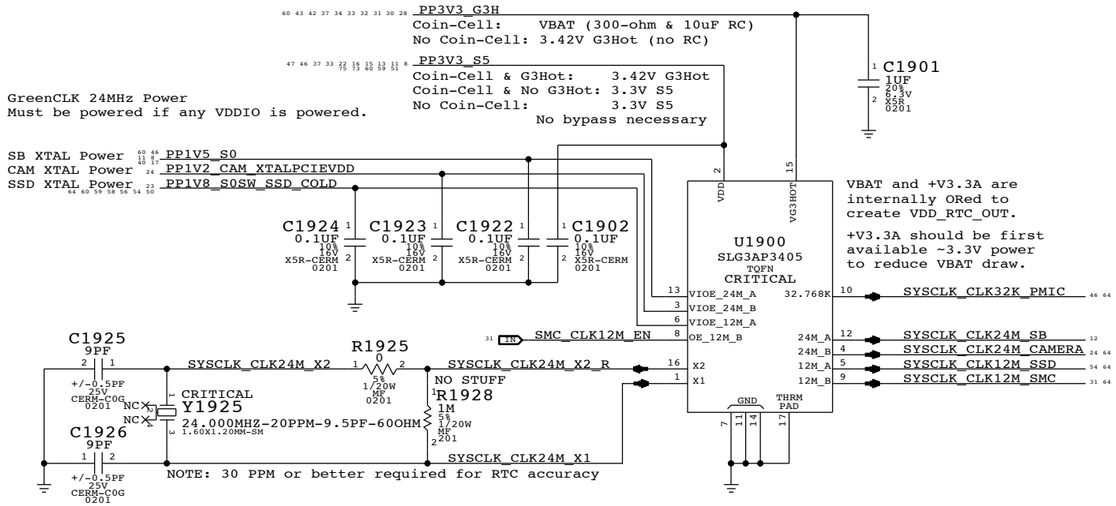
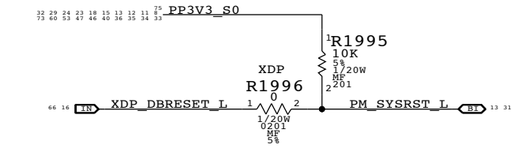
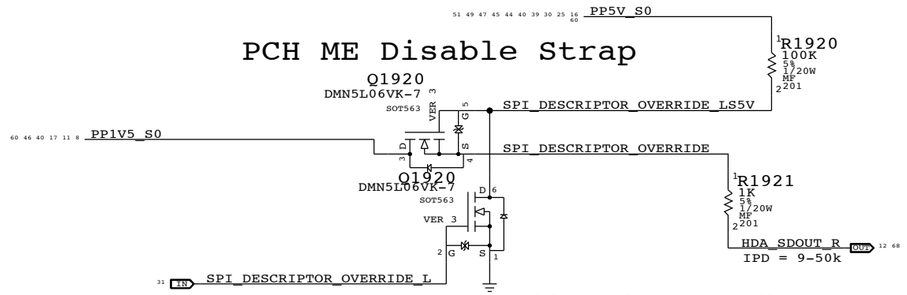
System 32kHz / 12MHz / 24MHz Clock Generator

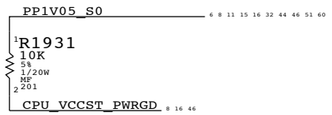




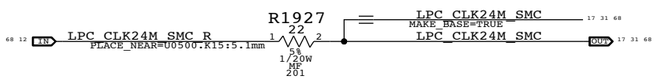
PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



PCH 24MHz Outputs



SYNC_MASTER=J92_DEVMLB SYNC_DATE=06/28/2013

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Apple Inc.

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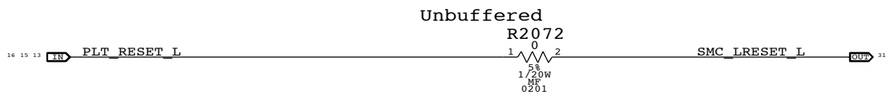
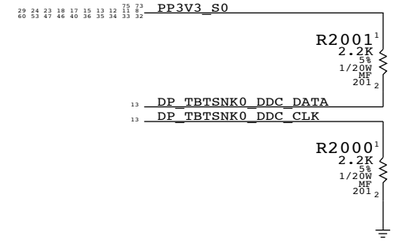
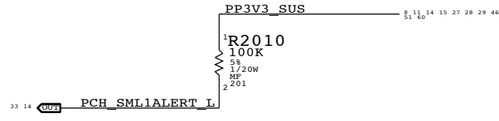
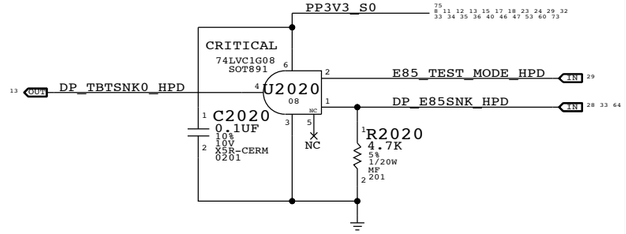
Platform Reset Connections

Unbuffered



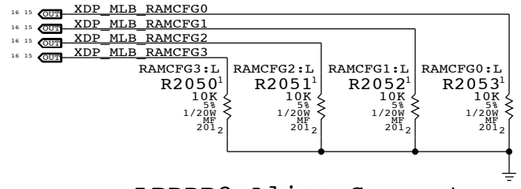




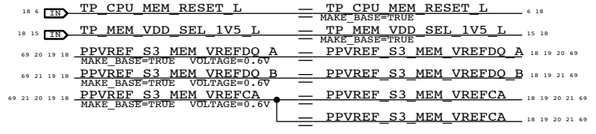


RAM Configuration Straps

Pull-downs for chip-down RAM systems



LPDDR3 Alias Support



SYNC_MASTER=J92_DEVMLB SYNC_DATE=08/01/2013

PAGE TITLE

Project Chipset Support

Apple Inc.

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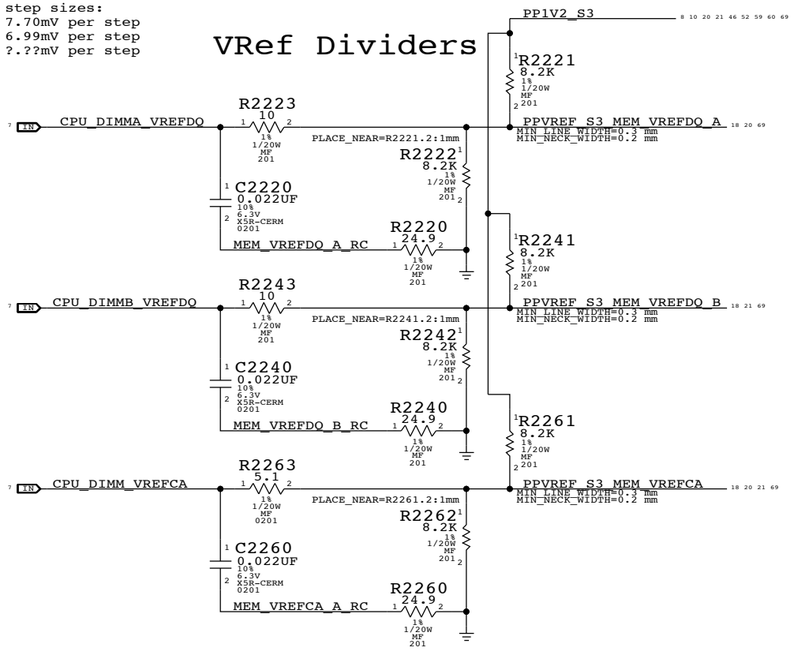
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



SYNC MASTER=J92 DEVMLB SYNC DATE=06/28/2013

PAGE TITLE
LPDDR3 VREF MARGINING

Apple Inc.

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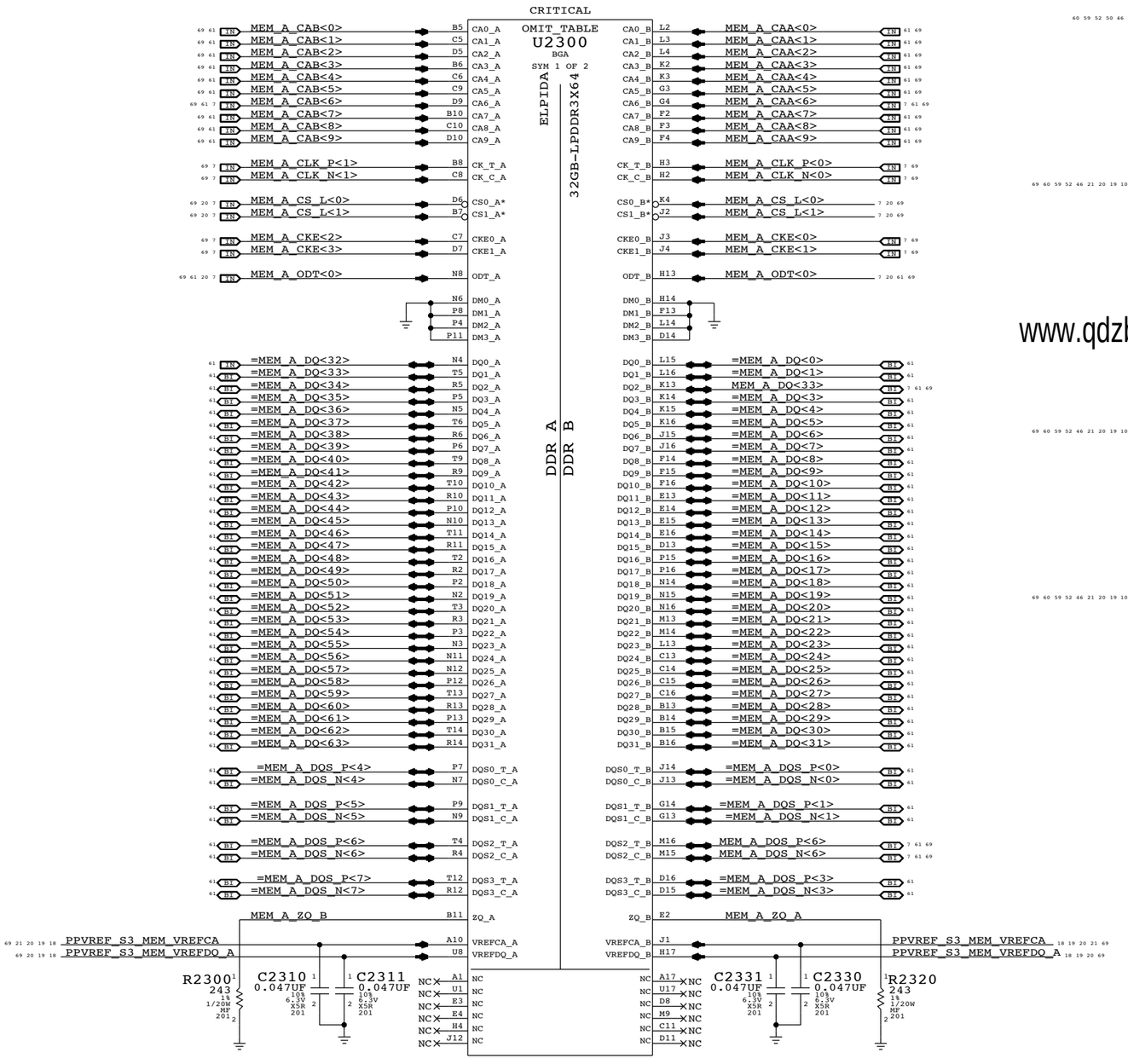

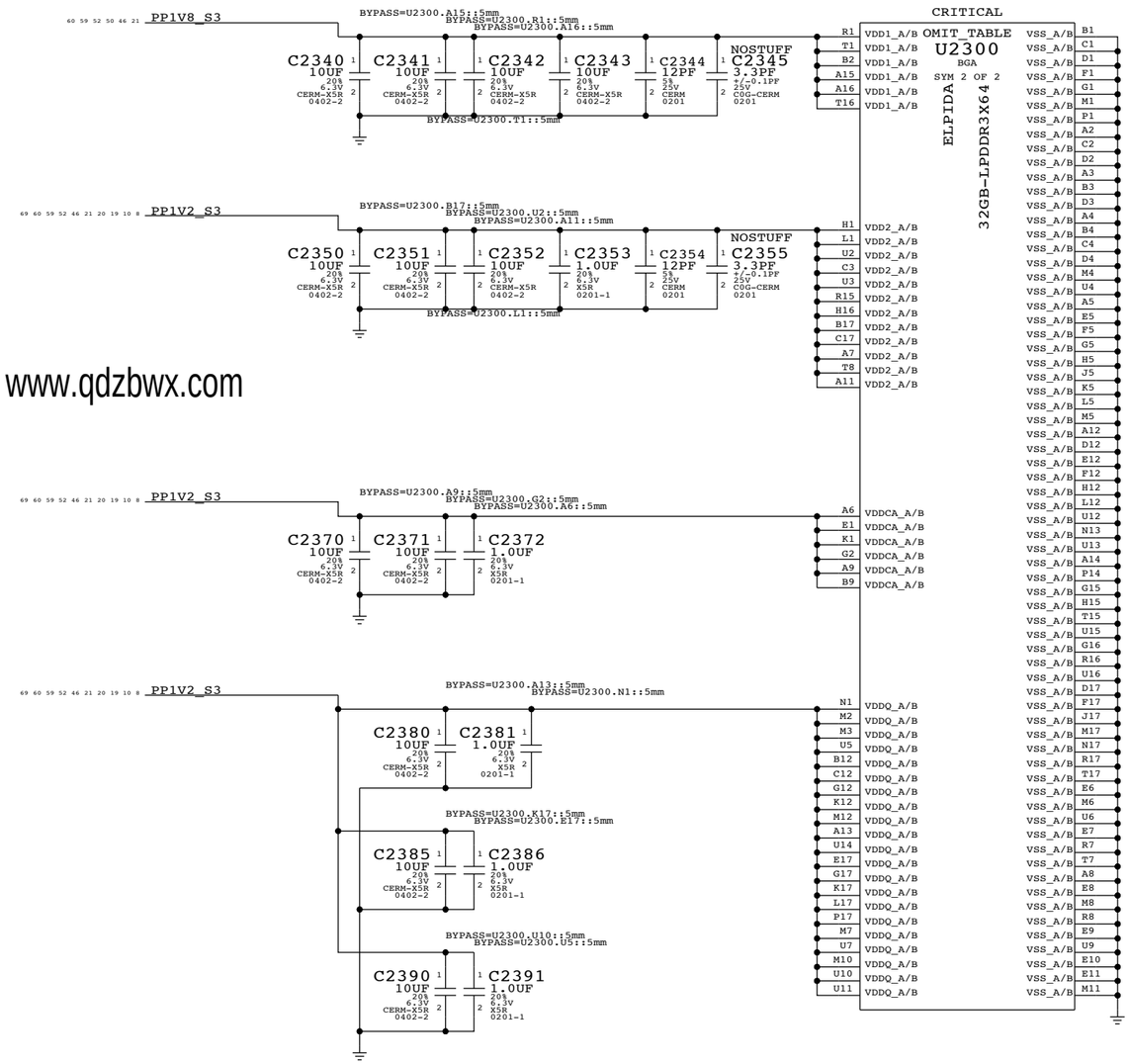

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE

LPDDR3 DRAM Channel A (0-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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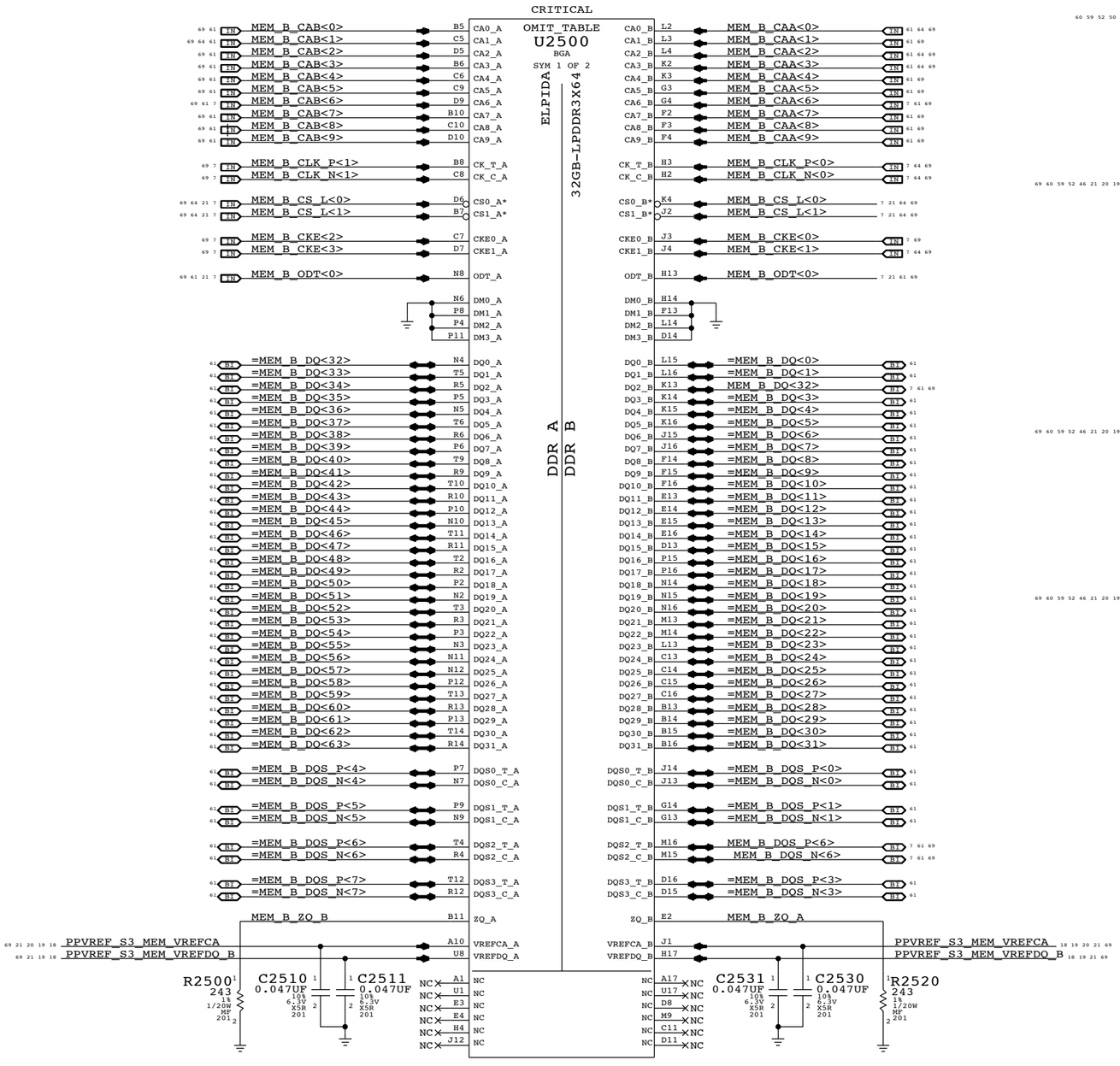
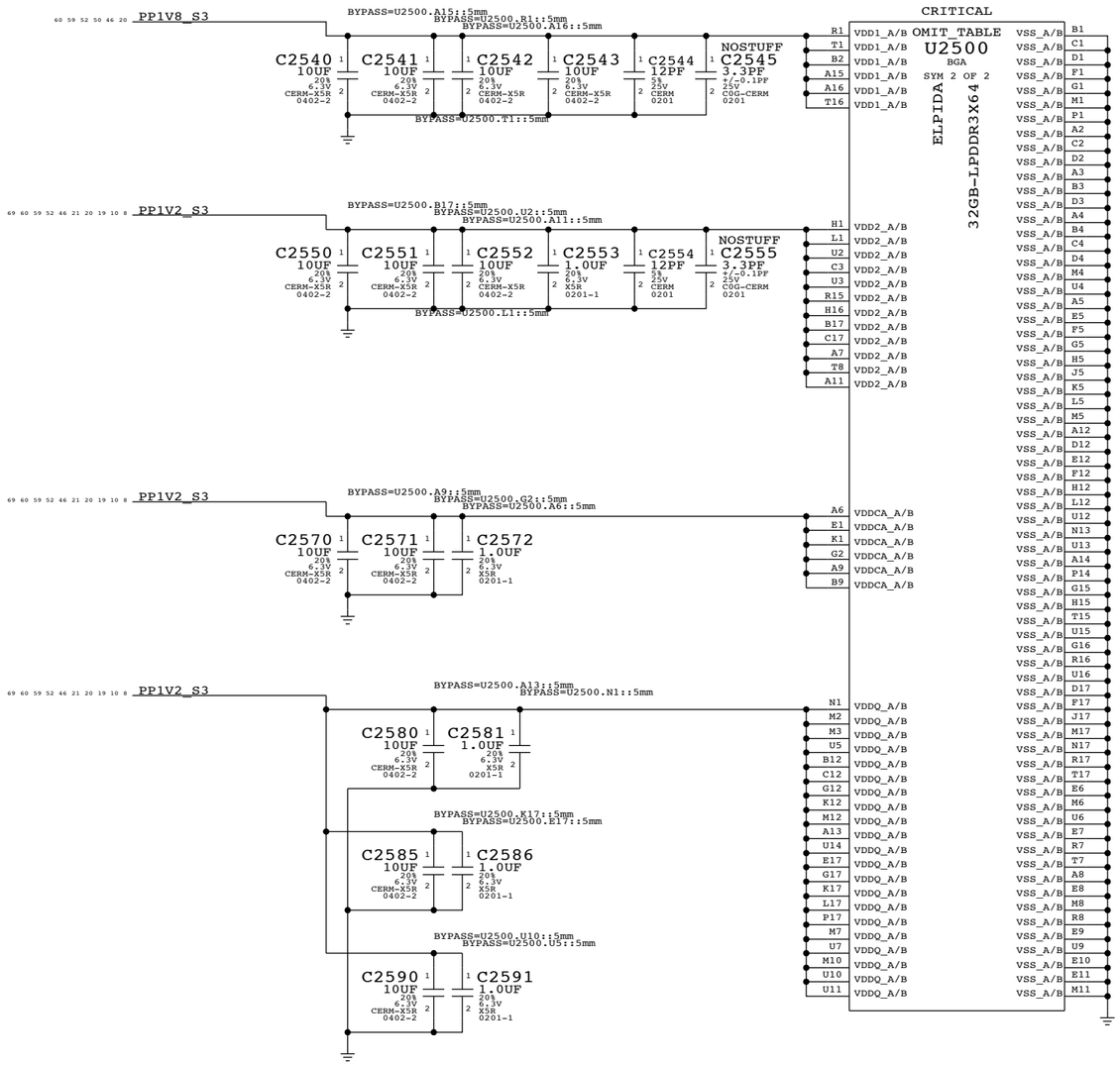
SHEET 20 OF 75





SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE

LPDDR3 DRAM Channel B (0-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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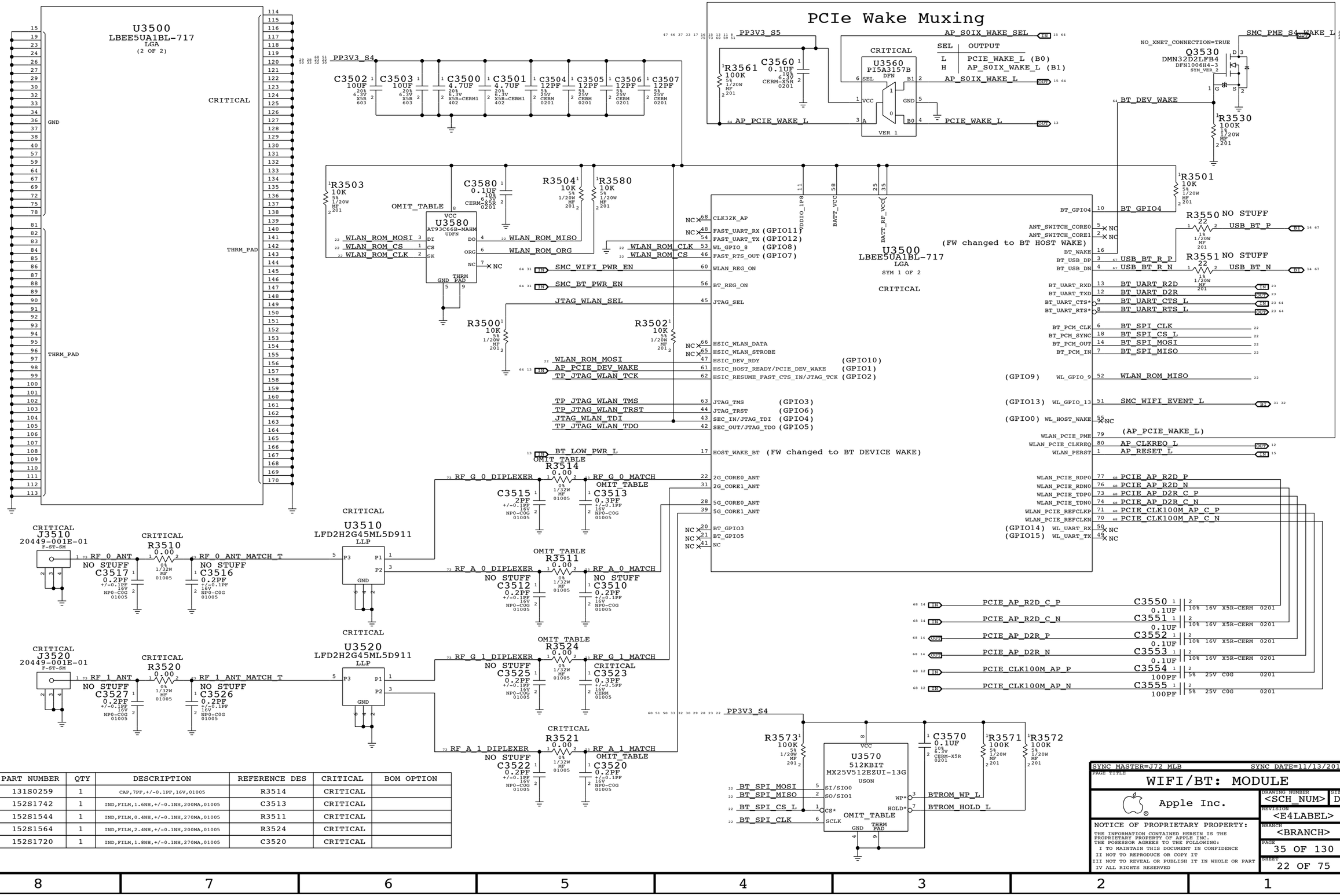
PCIe Wake Muxing



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S0259	1	CAP,7PF,+/-0.1PF,16V,01005	R3514	CRITICAL	
152S1742	1	IND,FILM,1.6NH,+/-0.1NH,200MA,01005	C3513	CRITICAL	
152S1544	1	IND,FILM,0.4NH,+/-0.1NH,270MA,01005	R3511	CRITICAL	
152S1564	1	IND,FILM,2.4NH,+/-0.1NH,200MA,01005	R3524	CRITICAL	
152S1720	1	IND,FILM,1.8NH,+/-0.1NH,270MA,01005	C3520	CRITICAL	

SYNC_MASTER=J72_MLB SYNC_DATE=11/13/2012

PAGE TITLE

WIFI/BT: MODULE

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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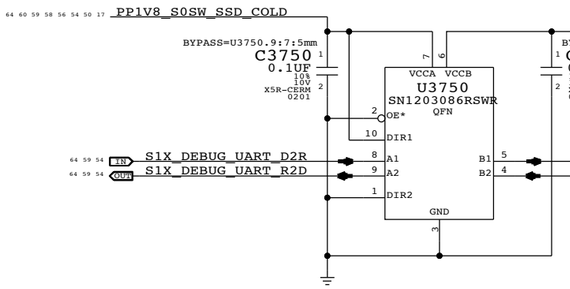
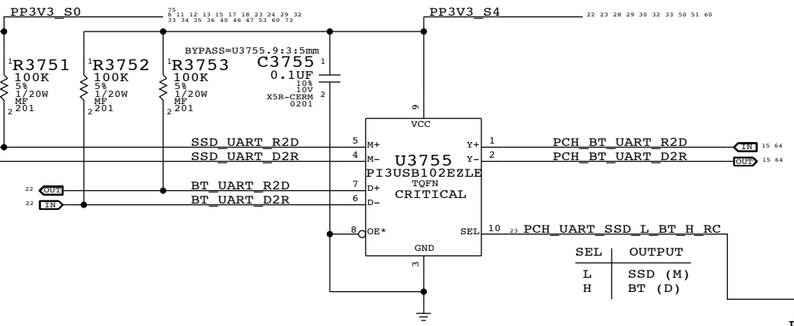
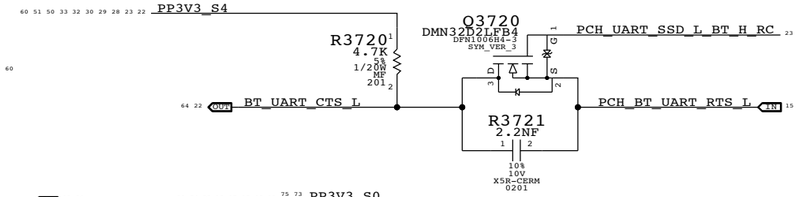
SSD/PCH Level Shifter



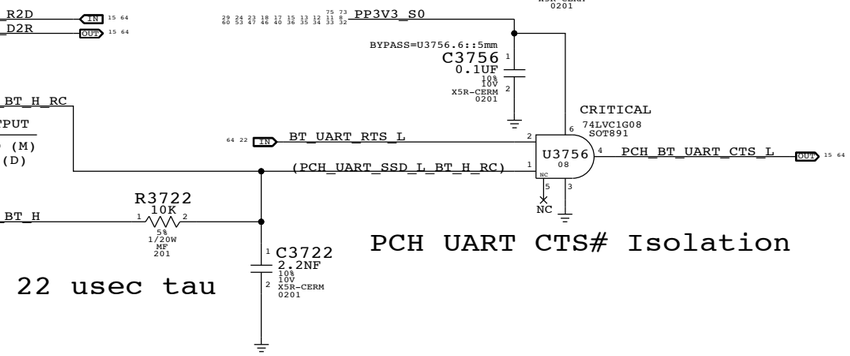
PCH UART BT/SSD MUX



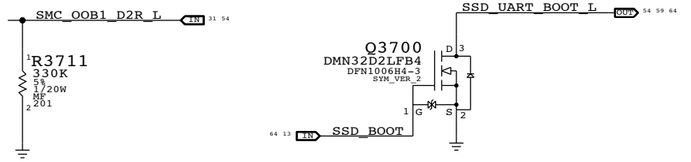
BT UART CTS# Isolation

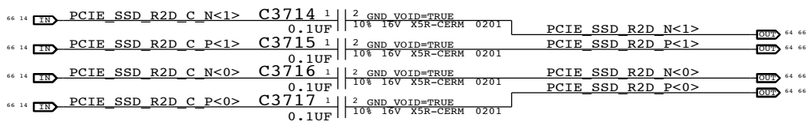


PCH UART CTS# Isolation



Bootloader Enable





SYNC MASTER=J92_DEVMLB SYNC DATE=09/11/2013

PAGE TITLE: SSD Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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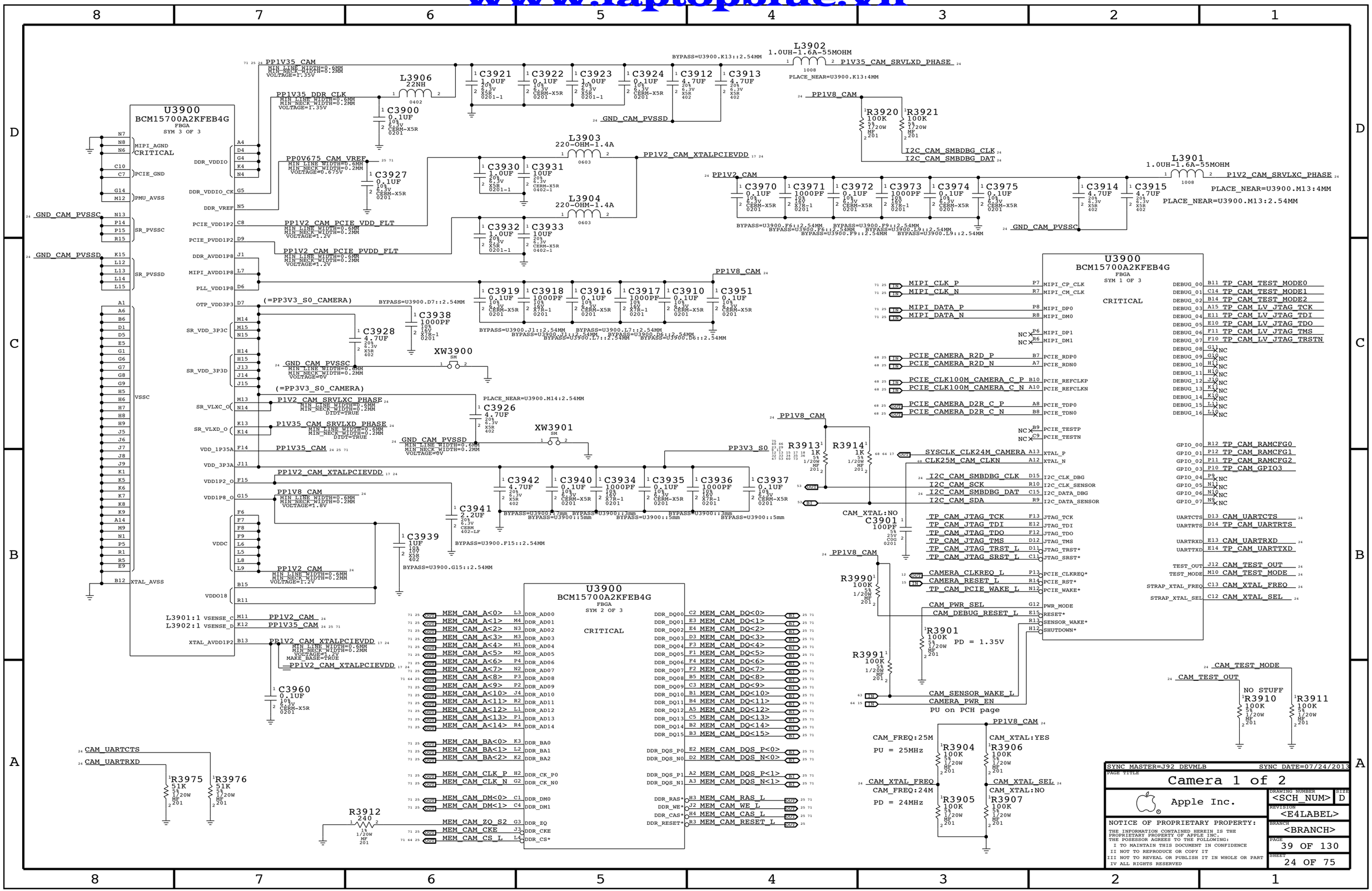
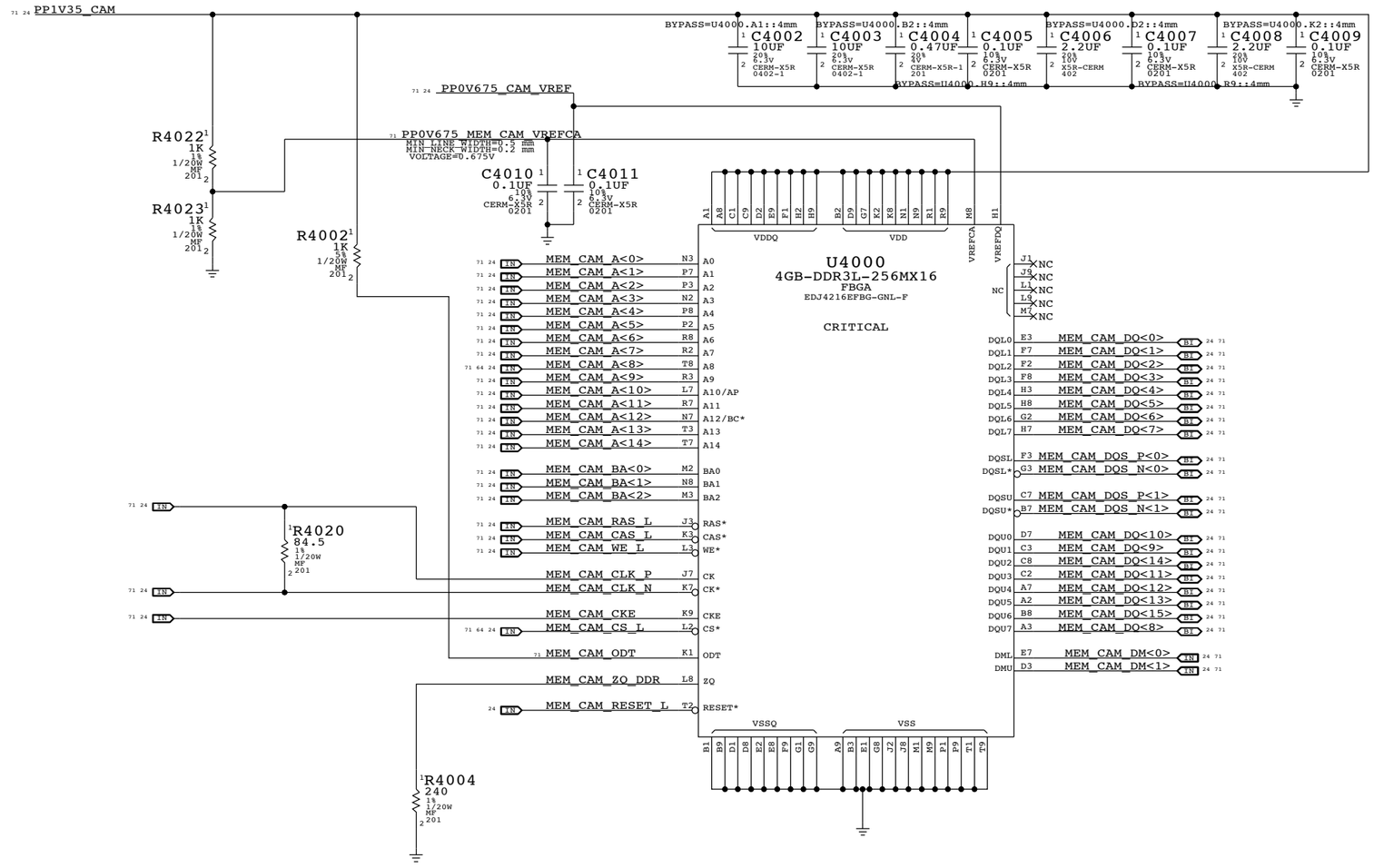
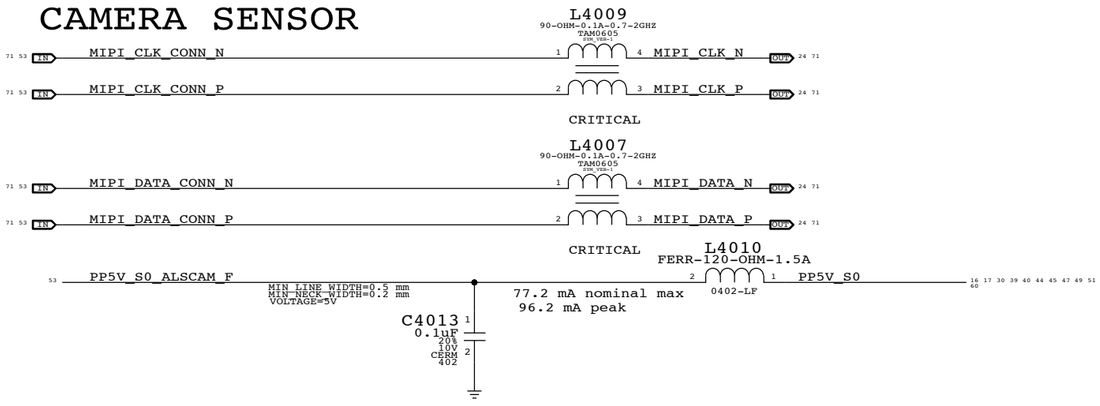




CAMERA SENSOR



SYNC_MASTER=J92_DEVMLB	SYNC_DATE=10/10/2013
PAGE TITLE	Camera 2 of 2
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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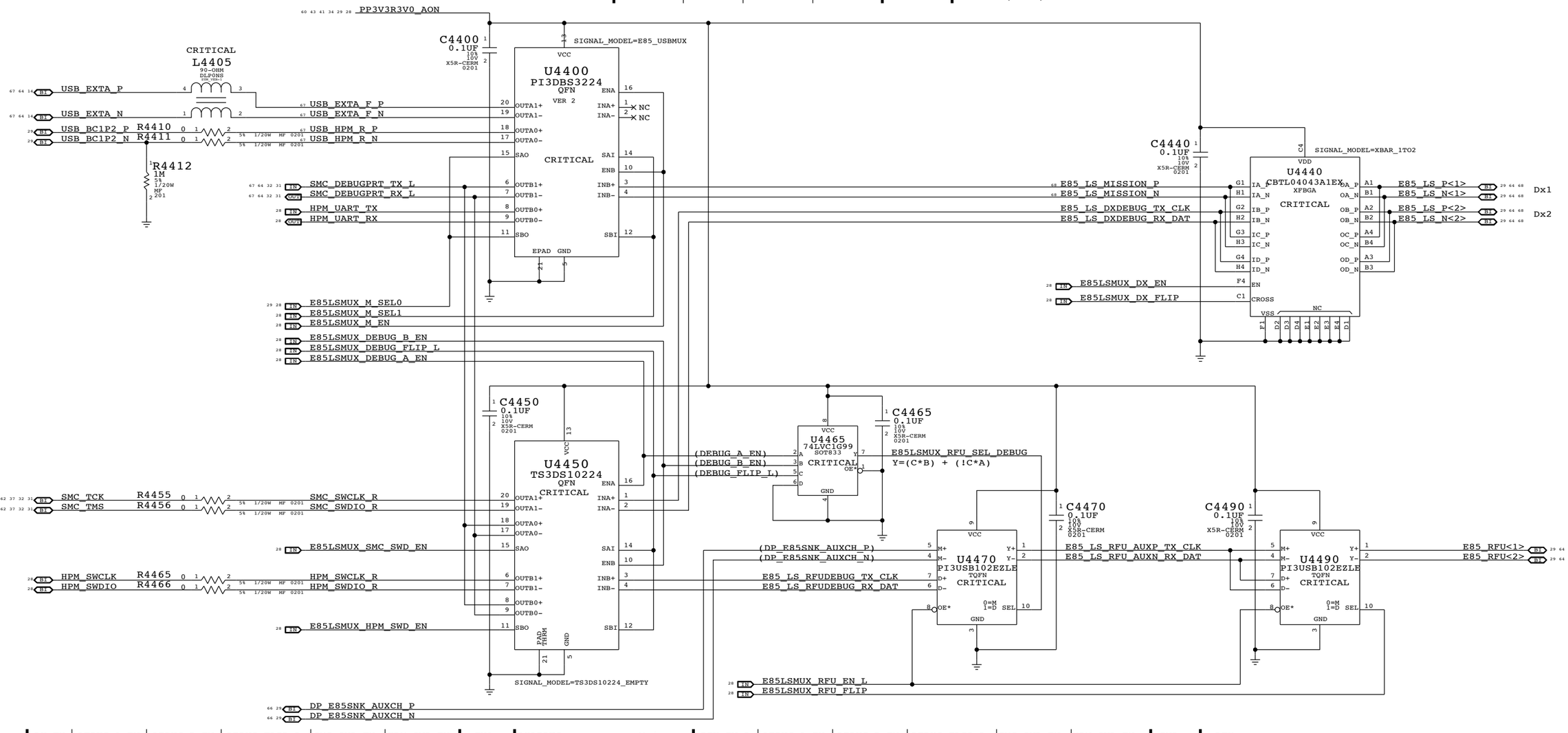
	SHEET 25 OF 75

Mode	DX_EN	M_EN	M_SEL0	M_SEL1	INB	Mission
Empty	0	0	X	X	Hi-Z	Hi-Z
Mojo	1	1	1	1	OUTB1	UART (SMC)
USB (Host)	1	1	1	0	OUTA1	USB (PCH)
USB (Device)	1	1	0	0	OUTA0	USB (HPM)
HPM UART	1	1	0	1	OUTB0	UART (HPM)



Mode	DX_EN	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INA	DXDEBUG
Empty	0	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
No Debug	1	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
SMC SWD	1	1	X	1	1	X	OUTA1	SWD (SMC)
Mojo	1	1 X	X 1	1 0	0 X	X 0	OUTA0 OUTB0	UART (SMC)
HPM SWD	1	X	1	0	X	1	OUTB1	SWD (HPM)

Mode	RFU_EN_L	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INB	RFU
Empty	1	X 0	0 X	1 0	X	X	Hi-Z	Hi-Z
DP	0	X 0	0 X	1 0	X	X	Hi-Z	AUX+/HPD
HPM SWD	0	X	1	1	X	1	OUTB1	SWD (HPM)
Mojo	0	X 1	1 X	1 0	X 0	0 X	OUTB0 OUTA0	UART (SMC)
SMC SWD	0	1	X	0	1	X	OUTA1	SWD (SMC)

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE: Low Speed MUXing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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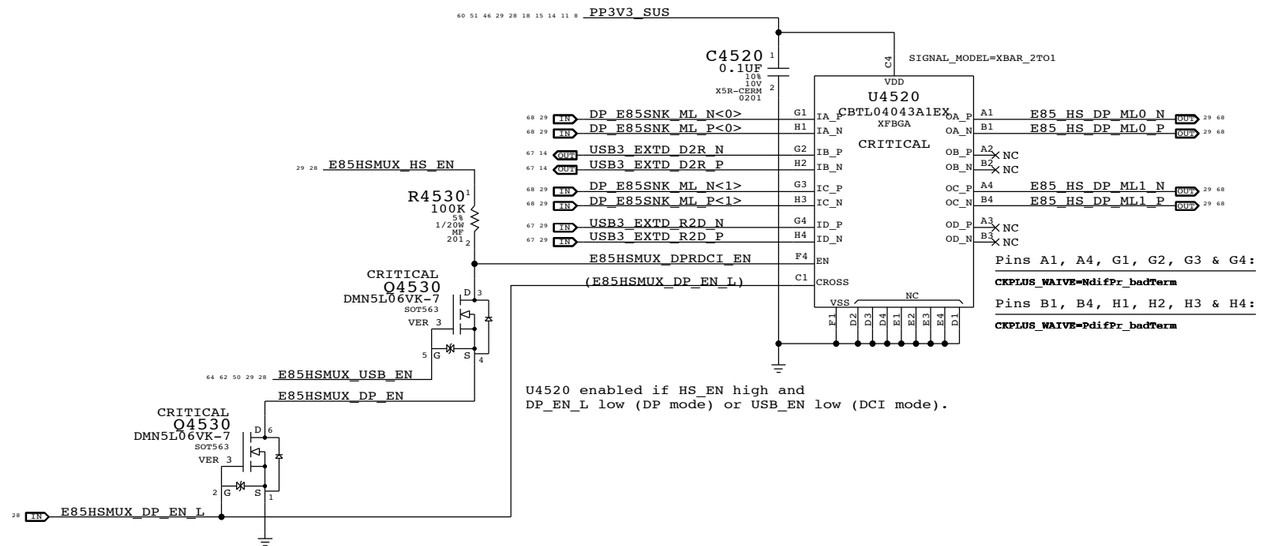

HS_FLIP swaps Tx1/2 and Rx1/2

Mode	HS_EN	DP_EN_L	USB_EN	SSTx1	SSRx1	SSTx2	SSRx2
Empty	0	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
USB3	1	1	1	R2D	D2R	Hi-Z	Hi-Z
USB3/DPx2	1	0	1	R2D	D2R	ML1	ML0
DPx4 (Passive)	1	0	0	ML2	ML3	ML1	ML0
DCI (Debug)	1	1	0	(ML2)	(ML3)	DCI-R2D	DCI-D2R

NOTE: Invert HS_FLIP in DCI mode to put DCI-USB on USB3 pins. USB3 and DP not usable in DCI mode.

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE: High Speed MUXing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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HPM SWITCH_EN Isolation

Allows HPM to monitor QR_SWITCH_EN
without creating leakage path.

CRITICAL
Q4635
DMN5L06VK-7
SOT563
VER 3

Pull-up in U4600

From MLB
QR_SWITCH_EN
VBUSFET_VDET

HPMVBUS:VDET
R4620 0 5% 1/20W MF 0201

PPDCIN_G3H
HPMVBUS:ADC
R4625 274K 1% 1/20W MF 201
R4626 45.3K 1% 1/20W MF 201
C4626 0.1UF 10% 10V X5R-CERM 0201

R4600 10K 5% 1/20W MF 201
PP3V3R3V0_AON

CRITICAL
OMIT_TABLE
U4600
LPC11U37FET48-CP3316
TFBGA

HPM_RESET_L	C1	RESET*/PIO0_0	
TS_HIPWR_EN	C2	PIO0_1_CLKOUT_CT32B0_MAT2_USB_FTOGGLE	
SMC_AID	F1	PIO0_2/SSEL0/CT16B0_CAP0	
HPM_PIO0_3	H2	PIO0_3/USB_VBUS	
I2C_PCH_1_SCL	G3	PIO0_4/SCL	
I2C_PCH_1_SDA	H3	PIO0_5/SDA	
HPM_SWITCH_EN_L	H6	PIO0_6/USB_CONNECT*/SCK0	
HPM_PIO0_7	G7	PIO0_7/CTS*	
HPM_PIO0_8	F8	PIO0_8/MISO0/CT16B0_MAT0	
BBPD_SPI_MOSI	F7	PIO0_9/MOSI0/CT16B0_MAT1	
HPM_SWCLK	E7	SWCLK/PIO0_10/SCK0/CT16B0_MAT2	
D- V-Sense	D8	TDI/PIO0_11/AD0/CT32B0_MAT3	
D+ V-Sense	C7	TMS/PIO0_12/AD1/CT32B1_CAP0	
I2C_HPM_SCL	C8	TDO/PIO0_13/AD2/CT32B1_MAT0	
I2C_HPM_SDA	B7	TRST*/PIO0_14/AD3/CT32B1_MAT1	
HPM_SWDIO	B6	SWDIO/PIO0_15/AD4/CT32B1_MAT2	
HPM_VBUS_VDET	A6	PIO0_16/AD5/CT32B1_MAT3/WAKEUP	
BBPD_PD_EN	A3	PIO0_17/RTS*/CT32B0_CAP0/SCLK	
HPM_UART_RX	B3	PIO0_18/RXD/CT32B0_MAT0	
HPM_UART_TX	B2	PIO0_19/TXD/CT32B0_MAT1	
BBPD_DET1_A	F2	PIO0_20/CT16B1_CAP0	
BBPD_DET1_B	G4	PIO0_21/CT16B1_MAT0/MOSI1	
BBPD_DET2_A	E8	PIO0_22/AD6/CT16B1_MAT1/MISO1	
BBPD_DET2_B	A5	PIO0_23/AD7	

VDD B4, E2 — VSS B5, D2

C4600 0.1UF 10% 10V X5R-CERM 0201
C4601 0.1UF 10% 10V X5R-CERM 0201
R4610 1.5K 5% 1/20W MF 201

NO_XNET_CONNECTION=TRUE

Pull-down on PIO1_5
indicates test-lio board.

PIO1_5/CT32B1_CAP1	H8	E85_TEST_MODE_L	
PIO1_13/DTR*/CT16B0_MAT0/TXD	B8	HPM_POWER_GATE_EN	
PIO1_14/DSR*/CT16B0_MAT1/RXD	A8	HPM_VBUSFET_EN	
PIO1_15/DCD*/CT16B0_MAT2/SCK1	A4	BBPD_VCONN_EN	
PIO1_16/RI*/CT16B0_CAP0	A2	XDP_USB_EXTA_OC_L	
PIO1_19/DTR*/SSEL1	B1	SMC_PME_S4_DARK_L	
PIO1_20/DSR*/SCK1	H1	BBPD_CON_DET_L	
PIO1_21/DCD*/MISO1	G8	BBPD_IPU_EN	
PIO1_22/RI*/MOSI1	A7	BBPD_RPD_EN	
PIO1_23/CT16B1_MAT1/SSEL1	H4	DP_E85SNK_HPD	
PIO1_24/CT32B0_MAT0	G6	HPM_VBUSFET_OC_L	
PIO1_25/CT32B0_MAT1	A1	HPM_VCFET_OC_L	
PIO1_26/CT32B0_MAT2/RXD	G2	E85HSMUX_HS_EN	
PIO1_27/CT32B0_MAT3/TXD	G1	E85LSMUX_DX_EN	
PIO1_28/CT32B0_CAP0/SCLK	H7	E85LSMUX_RFU_EN_L	
PIO1_29/SCK0/CT32B0_CAP1	D7	HPM_PIO1_29	

CKPLUS_WAIVE=NdifPr_badTerm
USB_DP H5 — USB_HPM_N
USB_DM G5 — USB_HPM_P
CKPLUS_WAIVE=PdifPr_badTerm

XTALIN D1 — GND
XTALOUT E1 — TP_HPM_XTALOUT

Polarity swap is intentional, required
to support low-speed USB on LPC11U37.

Allows SAK to override HPM
outputs (connector unplug)

R4631 1K 5% 1/20W MF 201 — TS_POWER_GATE_EN
CRITICAL
Q4630
DMN5L06VK-7
SOT563
VER 3

R4630 1K 5% 1/20W MF 201 — VBUSFET_EN
CRITICAL
Q4630
DMN5L06VK-7
SOT563
VER 3

SSP/IOH Steering Resistors

BBPD_RX_L_TX_H	R4615 0	HPM_PIO0_3
BBPD_SPI_SCLK	R4616 0	
	R4617 0	
	R4618 0	HPM_PIO1_29
HPM_I2C_INT_L	R4621 0	HPM_PIO0_7
BBPD_SPI_MISO	R4622 0	
	R4623 0	
	R4624 0	HPM_PIO0_8

HPMBB:SSP0 - Use LPC SSP0 SPI controller (PoR)
HPMBB:IOH - Use LPC I/O Handler for BB SPI (CYA)

PIO0_3 pull-down ensures MCU does not enter USB ISP mode when blank.

NO STUFF

R4640 4.7K	HPM_PIO0_3	
R4639 4.7K	HPM_PIO1_29	
R4641 4.7K	HPM_VBUSFET_EN	
R4642 4.7K	BBPD_VCONN_EN	
R4643 4.7K	BBPD_IPU_EN	

NO STUFF Do not stuff if parasitic CC pull-down is active.

R4644 4.7K	BBPD_RPD_EN
R4645 4.7K	HPM_POWER_GATE_EN
R4646 4.7K	BBPD_PD_EN
R4647 4.7K	E85HSMUX_HS_EN
R4648 4.7K	E85LSMUX_DX_EN

For bring-up, allows default HPM SWD connection on RFU

RFU_EN_PD NOTE: Must be unstuffed before production!

R4649 4.7K	E85LSMUX_RFU_EN_L
R4637 470K	HPM_SWCLK
R4638 470K	HPM_SWDIO

4.7k pull-downs ensure signals are low when MCU
boots to counter internal 10-85uA pull-ups.

PP3V3R3V0_AON
C4650 0.1UF 10% 10V X5R-CERM 0201

U4650
PCAL6416A
VFBGA
CRITICAL

Addr=0x40(Wr)/0x41(Rd)
I2C_HPM_SCL
I2C_HPM_SDA

P0_0	A1	E85LSMUX_M_SEL0
P0_1	C3	E85LSMUX_M_SEL1
P0_2	B1	E85LSMUX_DX_FLIP
P0_3	C1	E85LSMUX_DEBUG_FLIP_L
P0_4	C2	E85LSMUX_HPM_SWD_EN
P0_5	D1	E85LSMUX_SMC_SWD_EN
P0_6	E1	E85LSMUX_DEBUG_B_EN
P0_7	D2	E85LSMUX_RFU_FLIP
P1_0	E3	E85LSMUX_M_EN
P1_1	E4	E85LSMUX_DEBUG_A_EN
P1_2	D3	E85HSMUX_DP_EN_L
P1_3	E5	E85HSMUX_USB_EN
P1_4	D4	E85HSMUX_HS_FLIP
P1_5	D5	BBPD_PD_SEL_CC2
P1_6	C5	P5VOUT_EN_L
P1_7	C4	EXPANDER_P1_7

PP3V3_G3H
R4670 100K 5% 1/20W MF 201
P5VOUT_EN

CRITICAL
Q4635
DMN5L06VK-7
SOT563
VER 3

PP3V3R3V0_AON
PP3V3_G3H
PP3V3_SUS
PP3V3_S4

		Domain
R4650 100K	E85LSMUX_M_SEL0	AON
R4651 100K	E85LSMUX_M_SEL1	AON
R4652 100K	E85LSMUX_DX_FLIP	AON
R4653 100K	E85LSMUX_DEBUG_FLIP_L	AON
R4654 100K	E85LSMUX_HPM_SWD_EN	AON
R4655 100K	E85LSMUX_SMC_SWD_EN	AON
R4656 100K	E85LSMUX_DEBUG_B_EN	AON
R4657 100K	E85LSMUX_RFU_FLIP	AON
R4660 100K	E85LSMUX_M_EN	AON
R4661 100K	E85LSMUX_DEBUG_A_EN	AON
R4662 100K	E85HSMUX_DP_EN_L	SUS
R4663 100K	E85HSMUX_USB_EN	S4
R4664 100K	E85HSMUX_HS_FLIP	SUS
R4665 100K	BBPD_PD_SEL_CC2	AON
R4666 100K	P5VOUT_EN_L	AON
R4667 100K	EXPANDER_P1_7	G3H

All non-AON signals are open-drain to avoid leakage.
P1_7 in G3H domain for initial detection of G3H power.

SYNC_MASTER=DEV LIO SYNC_DATE=04/30/2014

PAGE TITLE: Host Port Micro

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 46 OF 130
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E85 AC coupled signals

DP_E85SNK_AUXCH_P → C4710 0.1UF 10% 10V X5R-CERM 0201 → DP_TBTSNK0_AUXCH_C_P
DP_E85SNK_AUXCH_N → C4711 0.1UF 10% 10V X5R-CERM 0201 → DP_TBTSNK0_AUXCH_C_N
GND_VOID

DP_E85SNK_ML_P<0> → C4712 0 5% 1/20W MF 0201 TRUE → DP_TBTSNK0_ML_C_P<0>
DP_E85SNK_ML_N<0> → C4713 0 5% 1/20W MF 0201 TRUE → DP_TBTSNK0_ML_C_N<0>
DP_E85SNK_ML_P<1> → C4714 0.1UF 10% 10V X5R-CERM 0201 TRUE → DP_TBTSNK0_ML_C_P<1>
DP_E85SNK_ML_N<1> → C4715 0.1UF 10% 10V X5R-CERM 0201 TRUE → DP_TBTSNK0_ML_C_N<1>
DP_E85SNK_ML_P<2> → C4716 0.1UF 10% 10V X5R-CERM 0201 TRUE → DP_TBTSNK0_ML_C_P<2>
DP_E85SNK_ML_N<2> → C4717 0.1UF 10% 10V X5R-CERM 0201 TRUE → DP_TBTSNK0_ML_C_N<2>
DP_E85SNK_ML_P<3> → C4718 0 5% 1/20W MF 0201 TRUE → DP_TBTSNK0_ML_C_P<3>
DP_E85SNK_ML_N<3> → C4719 0 5% 1/20W MF 0201 TRUE → DP_TBTSNK0_ML_C_N<3>

USB3_EXTA_R2D_P → C4720 0.1UF 10% 10V X5R-CERM 0201 → USB3_EXTA_R2D_C_P
USB3_EXTA_R2D_N → C4721 0.1UF 10% 10V X5R-CERM 0201 → USB3_EXTA_R2D_C_N
USB3_EXTD_R2D_P → C4722 0.1UF 10% 10V X5R-CERM 0201 → USB3_EXTD_R2D_C_P
USB3_EXTD_R2D_N → C4723 0.1UF 10% 10V X5R-CERM 0201 → USB3_EXTD_R2D_C_N

NO_XNET_CONNECTION=TRUE
R4725 100K 5% 1/20W MF 201 — PP3V3_S4
R4726 100K 5% 1/20W MF 201 — PP3V3_S4
NO_XNET_CONNECTION=TRUE

E85 PCIe CLKREQ_L isolation

Q4700 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
PP3V3_S0 → Q4700 → TBT_CLKREQ_L

516S1183 E85 B2B RECEPTACLE

CRITICAL J4700 AA21-S054VA1 F-ST-SM

PP5V1_S4SW_CC2	2	1	GND_VOID
PCH_TBT_PCIE_RESET_L	4	3	TRUE E85_HS_DP_ML1_N
E85_RFU<2>	6	5	TRUE E85_HS_DP_ML1_P
E85_TEST_MODE_L	8	7	
	10	9	TRUE DP_E85SNK_ML_N<2>
	12	11	TRUE DP_E85SNK_ML_P<2>
	14	13	
=PCIE_E85_R2D_P	16	15	E85_LS_P<2>
=PCIE_E85_R2D_N	18	17	E85_LS_N<2>
	20	19	
PCIE_CLK100M_TBT_P	22	21	TRUE USB3_EXTA_D2R_P
PCIE_CLK100M_TBT_N	24	23	TRUE USB3_EXTA_D2R_N
	26	25	
=PCIE_E85_D2R_N	28	27	E85_LS_P<1>
=PCIE_E85_D2R_P	30	29	E85_LS_N<1>
	32	31	
E85_TEST_MODE_HPD	34	33	TRUE USB3_EXTA_R2D_P
PP1V05_S4SW	36	35	TRUE USB3_EXTA_R2D_N
PP3V3_SUS	38	37	
E85HSMUX_HS_EN	40	39	TRUE DP_E85SNK_ML_P<3>
E85HSMUX_USB_EN	42	41	TRUE DP_E85SNK_ML_N<3>
	44	43	
	46	45	TRUE E85_HS_DP_ML0_P
PPVBUS_E85	48	47	TRUE E85_HS_DP_ML0_N
PP5V1_S4SW_CC1	50	49	
SMC_ONOFF_L	52	51	E85HSMUX_HS_FLIP
	54	53	E85_RFU<1>
	56	55	
	58	57	

PP3V3_SUS → R4727 100K 5% 1/20W MF 201 → CRITICAL J4700

R4750 51.1 1% 1/4W MF 0603 — CRITICAL
PPDCIN_G3H → Q4750 SI8487DB BGA
35mohm max @ Vgs = -4.5V
Max Ids = 4.9A
PPDCIN_E85_SS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=20V
CRITICAL F4700 4A-32V 0603
R4755 330K 1% 1/20W MF 201 — C4755 1UF 20% 16V CERM-X5R 0201
CRITICAL D4750 X3DFN06032 GDZ8V2BLP3 8.2V ZENER
C4750 1.0UF 10% 10V CERM-X5R 0402
PDCIN_E85_SS_DIV
R4756 30K 1% 1/20W MF 201

USB VBUS & BC 1.2 Charger Detection

PP3V3R3V0_AON → C4780 0.1UF 10% 10V X5R-CERM 0201

U4780 PI3USB9281AGE CSP
VDDIO VBAT GND VBUSOUT VBUSIN DPH DNH SDA SCL INTB VBUSDET ENB D+ D- ID

TP_BC1P2_VBUSOUT → VBUSOUT
PPVBUS_E85 ← VBUSIN
USB_HPM_P → DPH
USB_HPM_N → DNH
I2C_HPM_SDA → SDA
I2C_HPM_SCL → SCL
TP_BC1P2_INTB → INTB
VBUSFET_VDET ← VBUSDET
E85LSMUX_M_SEL0 → ENB
MAKE_BASE=TRUE
USB_BC1P2_P = USB_BC1P2_P
USB_BC1P2_N = USB_BC1P2_N
MAKE_BASE=TRUE
TP_BC1P2_ID

PP3V3R3V0_AON → CRITICAL U4701 74LVC1G08 SOT891
BBPD_SPI_MISO → U4701 → BBPD_SPI_MISO_BUF
24mA max output
C4701 0.1UF 10% 10V X5R-CERM 0201

CCSAK CRITICAL U4700 SLG4AP6645AV STQFN

BBPD_IPU_EN	15	IH_EN	
BBPD_RPD_EN	17	RD_EN	
BBPD_VCONN_EN	9	VCONN_EN	
BBPD_PD_SEL_CC2	13	PD_SEL_CC2	
BBPD_PD_EN	2	PD_EN	
BBPD_RX_L_TX_H	20	TX/RX*	
BBPD_MISO_LS1V1	16	MISO	
BBPD_SPI_MOSI	19	MOSI	
BBPD_SPI_SCLK	18	SCLK	
BBPD_DET1_A	6	DET1_A	
BBPD_DET1_B	7	DET1_B	
BBPD_DET2_A	3	DET2_A	
BBPD_DET2_B	4	DET2_B	
BBPD_CON_DET_L	14	CON_DET*	
	1	VDD	
	11	GND	
BBPD_VCONN1_EN	8	VCONN1_EN	
BBPD_VCONN2_EN	5	VCONN2_EN	
E85_CC1	10	CC1	
E85_CC2	12	CC2	

TX level-shift and slew-rate control
R4705 220 1% 1/20W MF 201 — CCSAK
R4706 120 1% 1/20W MF 201
C4705 1000PF 10% 16V X7R-1 0201
NO STUFF
R4709 100 1% 1/20W MF 201
C4700 0.1UF 10% 10V X5R-CERM 0201
C4706 220PF 2% 50V C0G 0201
C4707 220PF 2% 50V C0G 0201

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014
PAGE TITLE: E85 FLEX CONNECTOR
Apple Inc.
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IPD ZIF CONNECTOR

Bottom side contacts used
Pinout reversed from flex

518S0854
CRITICAL
J4801
502250-8041
F-RT-SM

TPAD_SPI_CS_L
TPAD_SPI_IF_EN
SMC_PME_S4_WAKE_L
PP3V3_S4_TPAD_F
TP_USB_TPADN
SMC_ACTUATOR_DISABLE_L
SMBUS_SMC_3_SDA
PP3V3_G3H_KBD_F
PP5V_S0_KBD_F

TPAD_SPI_MISO_R
TPAD_SPI_MOSI_R
TPAD_SPI_CLK_R
TPAD_SPI_INT_L
PP3V3_S4_TPAD_F
TP_USB_TPADP
PP5V_S4_TPAD_F
SMBUS_SMC_3_SCL
SMC_LSOC_RST
SMC_ONOFF_L
PP5V_S0_KBD_F
SMC_LID
TP_USB_VBUS_EN

R4802 15 1% 1/20W MF 201 — TPAD_SPI_MISO
R4801 15 1% 1/20W MF 201 — TPAD_SPI_MOSI
R4803 15 1% 1/20W MF 201 — TPAD_SPI_CLK
R4870 100K 5% 1/20W MF 201

CRITICAL
F4800
3A-6A-9V-0.05OHM
0603
PPBUS_G3H — PPBUS_G3H_TPAD_FUSED
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=8.7V

CRITICAL
L4800
30-OHM-5A
0603
PPBUS_G3H_TPAD_FLT
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=8.7V

C4800 0.1uF 20% 10V CERM 402

XW4801
SM
GND_ACTUATOR
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=0V

CRITICAL
L4801
FERR-120-OHM-1.5A
0402-LF
PP3V3_G3H_KBD_F — PP3V3_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C4801 0.1uF 20% 10V CERM 402

CRITICAL
L4802
FERR-120-OHM-1.5A
0402-LF
PP3V3_S4_TPAD_F — PP3V3_S4
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C4802 0.1uF 20% 10V CERM 402

CRITICAL
L4803
FERR-120-OHM-1.5A
0402-LF
PP5V_S4_TPAD_F — PP5V_S4
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4803 0.1uF 20% 10V CERM 402

CRITICAL
L4804
FERR-120-OHM-1.5A
0402-LF
PP5V_S0_KBD_F — PP5V_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4804 0.1uF 20% 10V CERM 402

BYPASS=J4801::1.5MM
BYPASS=J4801::1.5MM
BYPASS=J4801::1.5MM
SMC_LSOC_RST
SMC_ONOFF_L
SMC_LID
C4810 100PF 5% 25V C0G 0201
C4811 100PF 5% 25V C0G 0201
C4812 100PF 5% 25V C0G 0201

SYNC_MASTER=J92_DEVMLB SYNC_DATE=03/26/2014

PAGE TITLE: Keyboard & Trackpad Conn

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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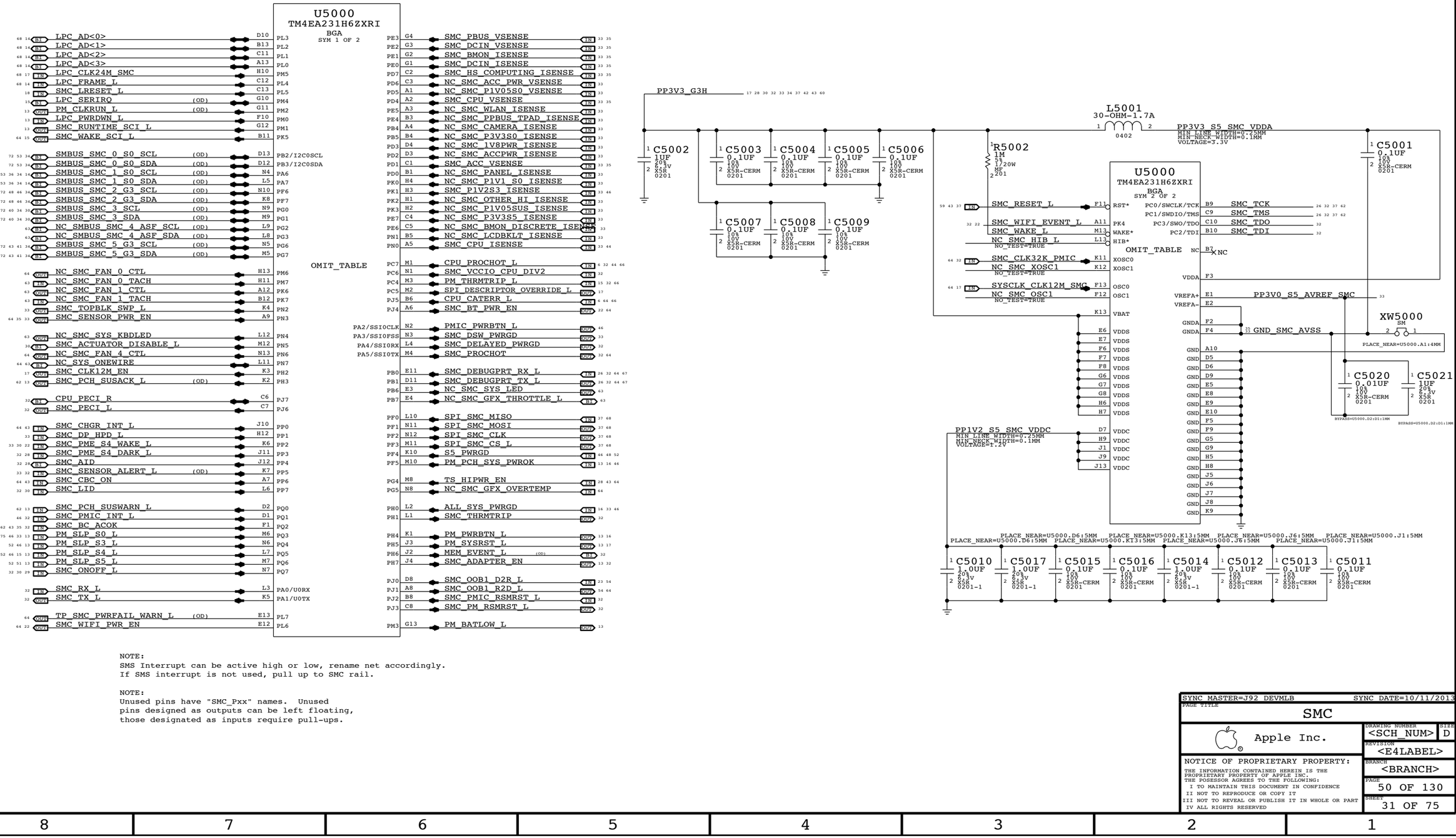

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/11/2013

PAGE TITLE
SMC

Apple Inc.

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RSMRST:DIRECT
R5130 0 5% 1/20W MF 0201
46 IN PMIC_RSMRST_L
PM_RSMRST_L OUT 13
RSMRST:SMC
R5131 0 5% 1/20W MF 0201
RSMRST:SMC
R5132 0 5% 1/20W MF 0201
31 OUT SMC_PMIC_RSMRST_L
SMC_PM_RSMRST_L IN 31

CPU_PROCHOT_L
C5131 47PF 5% 25V C0G 0201
PLACE_NEAR=Q5159.6:5MM
Q5159 DMN5L06VK-7 SOT563 VER 3
SMC_PROCHOT IN 31 64

PM_THRMTRIP_L
Q5159 DMN5L06VK-7 SOT563 VER 3
SMC_THRMTRIP IN 31 32

SMC12 PECI Support

PP1V05_S0
CRITICAL
Q5150 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
R5152 0 5% 1/20W MF 0201
31 IN SMC_PECI_L
From SMC
SMC_PECI_L_R
NOSTUFF R5153 1.6K 5% 1/20W MF 201
R5151 330 5% 1/20W MF 201
R5134 43 5% 1/20W MF 201
31 OUT CPU_PECI_R
To SMC
CPU_PECI BI 6 66
From/To CPU/PCH
NOSTUFF C5134 47PF 5% 25V C0G 0201
PLACE_NEAR=Q5150.2:5MM

Debug Power "Buttons"

SMC_ONOFF_L OUT 29 30 31 32
OMIT R5116 0 5% 1/10W LF 0603-ZERO-HGT
PLACE_SIDE=BOTTOM
SILK_PART=PWR_BTN
OMIT R5115 0 5% 1/10W LF 0603-ZERO-HGT
PLACE_SIDE=TOP
SILK_PART=PWR_BTN

62 43 35 32 31 SMC_BC_ACOK — SMC_BC_ACOK 31 32 35 43 62
MAKE_BASE=TRUE

32 31 28 SMC_PME_S4_DARK_L — SMC_PME_S4_DARK_L IN 28 31 32
MAKE_BASE=TRUE

68 13 IN PM_CLK32K_SUSCLK_R
R5112 22 5% 1/20W MF 201
PLACE_NEAR=U0500.B27:5.1mm
SMC_CLK32K_PMIC OUT 31 64

51 46 44 32 17 16 15 11 8 6 65 PP1V05_S0
R5197 100K 1% 1/20W MF 201
31 SMC_VCCIO_CPU_DIV2
R5196 100K 1% 1/20W MF 201

60 43 42 37 34 33 31 30 28 17 PP3V3_G3H
60 51 50 33 30 29 28 23 22 PP3V3_S4
29 24 23 18 17 15 13 12 12 11 8 75 73 60 53 47 46 40 36 35 34 33 PP3V3_S0

31	MEM_EVENT_L	R5114	10K	NO STUFF
32 31 28	SMC_PME_S4_DARK_L	R5167	100K	5% 1/20W MF 201
31 22	SMC_WIFI_EVENT_L	R5168	100K	5% 1/20W MF 201
46 31	SMC_PMIC_INT_L	R5169	100K	5% 1/20W MF 201
32 31 30 29	SMC_ONOFF_L	R5170	10K	5% 1/20W MF 201
33 31	SMC_SENSOR_ALERT_L	R5172	10K	5% 1/20W MF 201
31 30	SMC_LID	R5171	100K	5% 1/20W MF 201
31	SMC_TX_L	R5173	10K	5% 1/20W MF 201
31	SMC_RX_L	R5174	100K	5% 1/20W MF 201
67 64 31 26	SMC_DEBUGPRT_TX_L	R5175	20K	5% 1/20W MF 201
67 64 31 26	SMC_DEBUGPRT_RX_L	R5176	20K	5% 1/20W MF 201
62 37 31 26	SMC_TMS	R5177	10K	5% 1/20W MF 201
31	SMC_TDO	R5178	10K	5% 1/20W MF 201
31	SMC_TDI	R5179	10K	5% 1/20W MF 201
62 37 31 26	SMC_TCK	R5180	10K	5% 1/20W MF 201
62 43 35 32 31	SMC_BC_ACOK	R5187	100K	5% 1/20W MF 201
31 28	SMC_AID	R5192	2.2K	5% 1/20W MF 201

31 13	SMC_ADAPTER_EN	R5185	100K	5% 1/20W MF 201
32 31	SMC_THRMTRIP	R5186	10K	5% 1/20W MF 201
31	SMC_DELAYED_PWRGD	R5191	100K	5% 1/20W MF 201

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/11/2013
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SMC Shared Support

Apple Inc.

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SMC_PBUS_VSENSE — SMC_PBUS_VSENSE (MAKE_BASE=TRUE)
SMC_DCIN_VSENSE — SMC_DCIN_VSENSE (MAKE_BASE=TRUE)
SMC_BMON_ISENSE — SMC_BMON_ISENSE (MAKE_BASE=TRUE)
SMC_DCIN_ISENSE — SMC_DCIN_ISENSE (MAKE_BASE=TRUE)
SMC_HS_COMPUTING_ISENSE — SMC_HS_COMPUTING_ISENSE (MAKE_BASE=TRUE)
NC_SMC_ACC_PWR_VSENSE — NC_SMC_ACC_PWR_VSENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_P1V05S0_VSENSE — NC_SMC_P1V05S0_VSENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_CPU_VSENSE — SMC_CPU_VSENSE (MAKE_BASE=TRUE)
NC_SMC_WLAN_ISENSE — NC_SMC_WLAN_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_PPBUS_TPAD_ISENSE — NC_SMC_PPBUS_TPAD_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_CAMERA_ISENSE — NC_SMC_CAMERA_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_P3V3S0_ISENSE — NC_SMC_P3V3S0_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_1V8PWR_ISENSE — NC_SMC_1V8PWR_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_ACCPWR_ISENSE — NC_SMC_ACCPWR_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_ACC_VSENSE — SMC_ACC_VSENSE (MAKE_BASE=TRUE)
NC_SMC_PANEL_ISENSE — NC_SMC_PANEL_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_P1V1_S0_ISENSE — NC_SMC_P1V1_S0_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_P1V2S3_ISENSE — SMC_P1V2S3_ISENSE (MAKE_BASE=TRUE) — SMC_P1V2S3_ISENSE
NC_SMC_OTHER_HI_ISENSE — NC_SMC_OTHER_HI_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_P1V05SUS_ISENSE — NC_SMC_P1V05SUS_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_P3V3S5_ISENSE — NC_SMC_P3V3S5_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_BMON_DISCRETE_ISENSE — SMC_BMON_DISCRETE_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_LCDBKLT_ISENSE — NC_SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE)
SMC_CPU_ISENSE — SMC_CPU_ISENSE (MAKE_BASE=TRUE, NO_TEST=TRUE) — SMC_CPU_ISENSE
SMC_SENSOR_PWR_EN — SMC_SENSOR_PWR_EN (MAKE_BASE=TRUE)

SMC AVREF Supply

PP3V3_G3H → U5265 REF3330 QFN CRITICAL (IN, OUT, GND, NC0–NC4)
C5265 1.0UF 20% 6.3V X5R 0201-1
C5266 10UF 20% 6.3V CERM-X5R 0402-1
C5267 0.1UF 10% 10V X5R-CERM 0201
PP3V0_S5_AVREF_SMC (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.0V)
GND_SMC_AVSS (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V)

Top-Block Swap

PP3V3_S0 → R5296 1K 5% 1/20W MF 201 → R5283 1K 5% 1/20W MF 201 → SMC_TOPBLK_SWP_L (IN) / PCH_STRP_TOPBLK_SWP_L (OUT)

PP3V3_S4 → R5220 100K 5% 1/20W MF 201 → SMC_DP_HPD_L (OUT)
CRITICAL Q5220 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 (D, G, S)
DP_E85SNK_HPD (IN)

PP3V3_S4 → R5282 100K 5% 1/20W MF 201 → SMC_PME_S4_WAKE_L (IN) / SMC_PME_S4_WAKE_L (OUT)
SMC_PME_S4_WAKE_L (IN)
SMC_PME_S4_WAKE_L MAKE_BASE=TRUE

PP3V3_S5 → C5250 0.1UF 10% 10V X5R-CERM 0201
U5250 74LVC1G57 SOT891 CRITICAL (VCC, GND)
ALL_SYS_PWRGD (IN) → A
PM_SLP_S0_L (IN) → C
Y → P1V05_ULQ_L (OUT)
NOSTUFF R5250 0 5% 1/20W MF 0201

Truth table

ASPGD	S0_L	ULQ_L	P1V05_SUS
0	0	1	1.05V
0	1	1	1.05V
1	0	0	0.95V
1	1	1	1.05V

PP3V3_S5 → C5280 0.1UF 10% 10V X5R-CERM 0201
U5280 74LVC1G07GF SOT891 CRITICAL (VCC, GND, NC)
SMC_DSW_PWRGD (IN) → A
Y → PM_DSW_PWRGD (OUT)
R5280 100K 5% 1/20W MF 201

NOSTUFF R5215 100 5% 1/20W MF 201 — PCH_SML1ALERT_L (IN)
NOSTUFF R5213 100 5% 1/20W MF 201 — NAND_OVERTMP_ALERT_L (IN)
NOSTUFF R5214 100 5% 1/20W MF 201 — CPUTHMSNS_ALERT_L (IN)
NOSTUFF R5211 100 5% 1/20W MF 201 — CPUBMONSNS_ALERT_L (IN)
→ SMC_SENSOR_ALERT_L (OUT)

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012
PAGE TITLE: SMC Project Support
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
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Wildcat Point LP S0 SMBus "0" Connections

PP3V3_S0

Wildcat Point LP
U0500
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA
MAKE_BASE=TRUE

R5300 1K 5% 1/20W MF 201
R5301 1K 5% 1/20W MF 201

XDP Connectors
J1800
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

SMC "0" SMBus S0 Connections

SMC
U5000
(MASTER)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

Pullups are on eDP connector page and gated by EDP_PANEL_PWR

Internal DP
J8300
(See Table)
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

(* = Multiple options)

Internal DP

	J43		J41		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "5" SMBus G3H Connections

PP3V3_G3H

SMC
U5000
(MASTER)
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
MAKE_BASE=TRUE

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

Battery Charger
BANSURI - U7100
(Write: 0x12 Read: 0x13)

Battery
J6950

Battery
Battery Manager - (Write: 0x16 Read: 0x17)

Wildcat Point LP S0 I2C "1" Connections

Wildcat Point LP
U0500
(MASTER)
I2C_PCH_1_SCL
I2C_PCH_1_SDA
MAKE_BASE=TRUE

S0 Pull-ups on PCH page 16

HPM
U4600
(Write: 0x?? Read: 0X??)
I2C_PCH_1_SCL
I2C_PCH_1_SDA

SMC "2" SMBus S3 Connections

PP3V3_G3H

SMC
U5000
(MASTER)
SMBUS_SMC_2_G3_SCL
SMBUS_SMC_2_G3_SDA
MAKE_BASE=TRUE

R5370 2.2K 5% 1/20W MF 201
R5371 2.2K 5% 1/20W MF 201

PMICs
U7400/U7600
(See Table)
SMBUS_SMC_2_G3_SCL
SMBUS_SMC_2_G3_SDA

SMC "3" SMBus S0 Connections

PP3V3_S0

SMC
U5000
(MASTER)
SMBUS_SMC_3_SCL
SMBUS_SMC_3_SDA
MAKE_BASE=TRUE

R5390 2.0K 5% 1/20W MF 201
R5391 2.0K 5% 1/20W MF 201

Trackpad
J4800
(Write: 0x90 Read: 0x91)

RIO
J6799
(Write: 0x?? Read: 0x??)

Wildcat Point LP S0 "SMLink 0" Connections

PP3V3_S0

Wildcat Point LP
U0500
(MASTER)
SML_PCH_0_CLK
SML_PCH_0_DATA
MAKE_BASE=TRUE

R5310 8.2K 5% 1/20W MF 201
R5311 8.2K 5% 1/20W MF 201

SMC S0 "1" SMBus Connections

PP3V3_S0

SMC
U5000
(MASTER)
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
MAKE_BASE=TRUE

R5360 4.7K 5% 1/20W MF 201
R5361 4.7K 5% 1/20W MF 201

CPU Temp, Inlet, DDR, BMON THR
EMC1704-02: U5800
(Write: 0x98 Read: 0x99)

NAND Temp Sense
HPA0033AI: U5880
(Write: 0x92 Read: 0x93)

ALS
J4002
(Write: 0x72 Read 0x73)

HPM Master Bus

PP3V3R3V0_AON

HPM
LPC11U37 - U4600
(MASTER)
I2C_HPM_SCL
I2C_HPM_SDA
MAKE_BASE=TRUE

R5340 2.0K 5% 1/20W MF 201
R5341 2.0K 5% 1/20W MF 201

I/O Expander
PCAL6516A - U5350
(Write: 0x40 Read: 0x41)

BC1.2 Detector
PI3USB9281 - U5680
(Write: 0x4A Read: 0x4B)

Wildcat Point LP S0 "SMLink 1" Connections

Wildcat Point LP
U0500
(Write: 0x88 Read: 0x89)
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA

SMLink 1 is slave port to access PCH

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

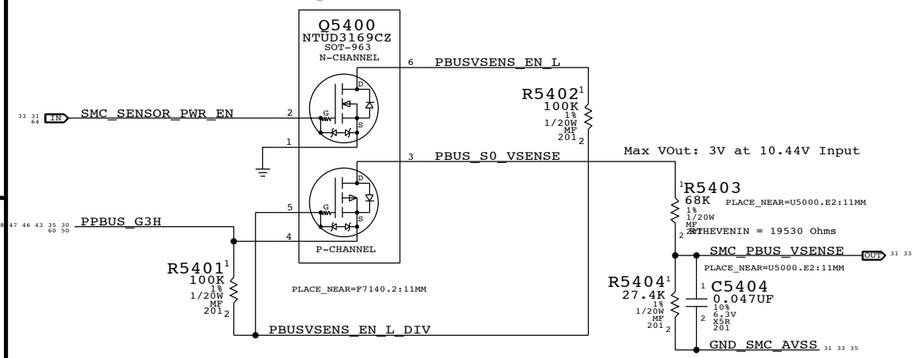
PAGE TITLE: SMBus Connections

Apple Inc.

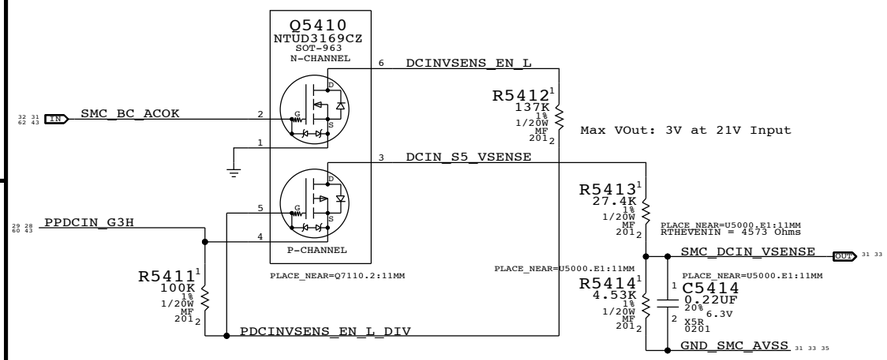
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 53 OF 130
SHEET: 34 OF 75

POR VOLTAGE / CURRENT SENSORS : TO BE USED IN PRODUCTION

VP0R: PBUS Voltage Sense Enable & Filter

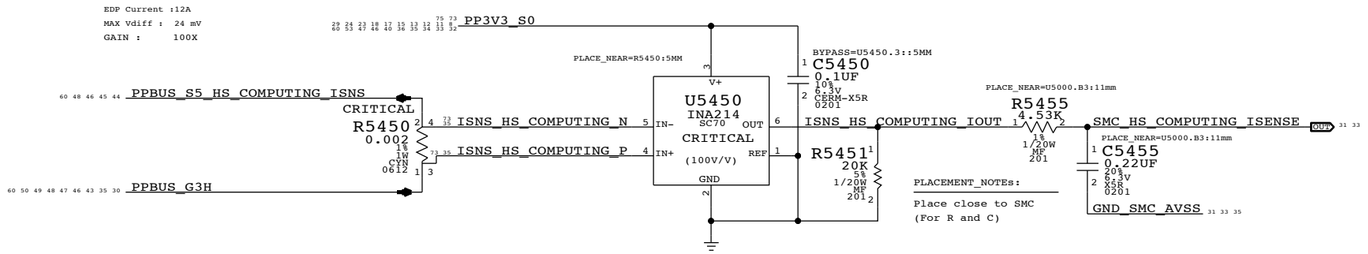


VD0R: DC-In Voltage Sense Enable & Filter



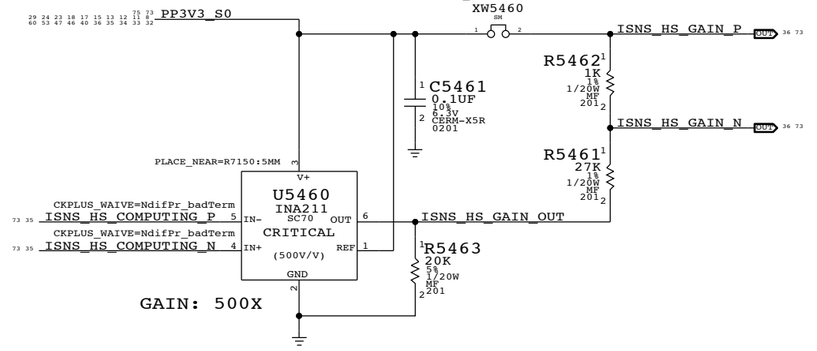
IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X



Need to set gains for ULX

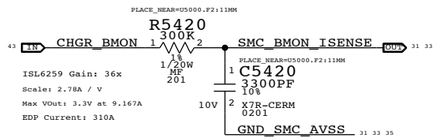
EMC1704 Computing High Side Gain Stage



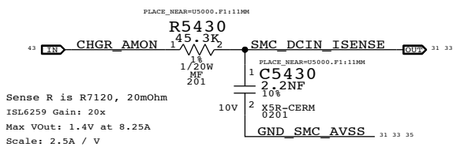
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

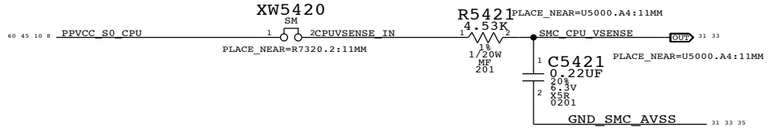
CHARGER BMON High Side Current Sense



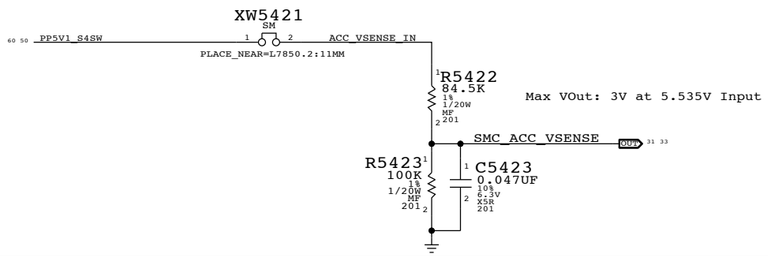
DC-IN (AMON) Current Sense



VCFR CPU Vcore Voltage Sense / Filter



ACC Voltage Sense



SYNC_MASTER=J92_DEVMLB SYNC_DATE=02/07/2014

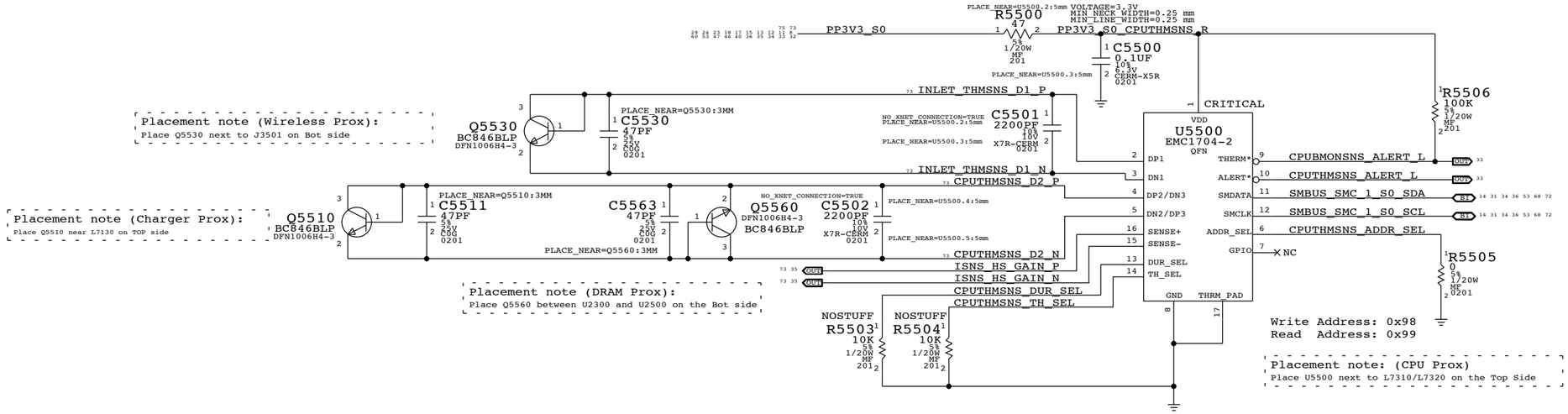
PAGE TITLE: Voltage & Current Sensing

Apple Inc.

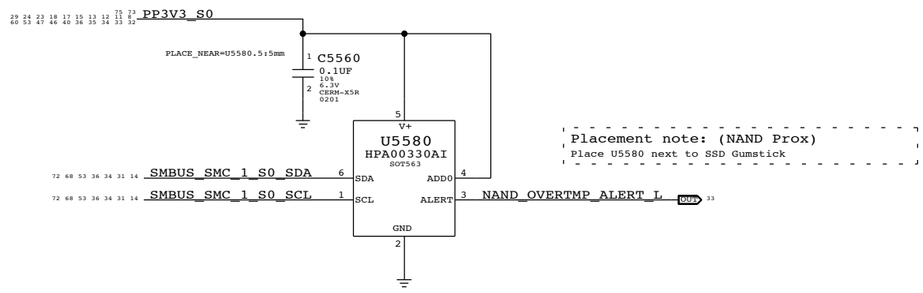
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 54 OF 130
SHEET: 35 OF 75

POR THERMAL SENSORS : TO BE USED IN PRODUCTION

CPU Proximity, Inlet ,DDR and BMON THR Sensor



NAND Temp Sensor



SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/12/2013

PAGE TITLE: Temperature Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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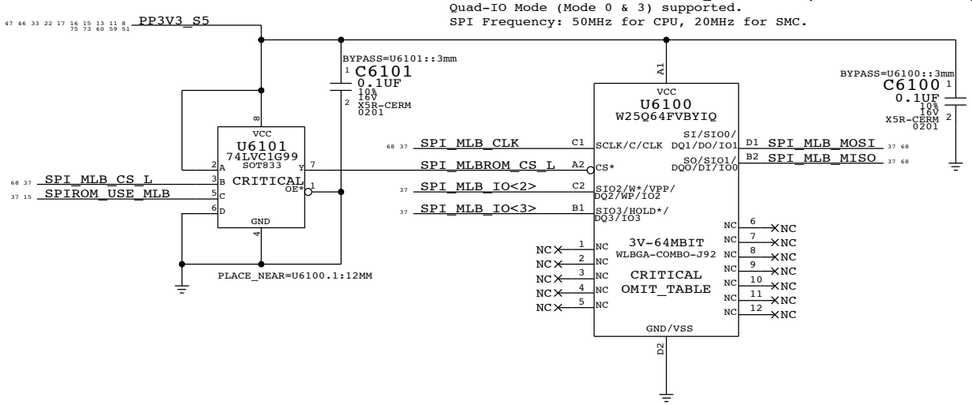
SHEET: 36 OF 75

SPI ROM - Combo BGA Footprint (3 vendors)

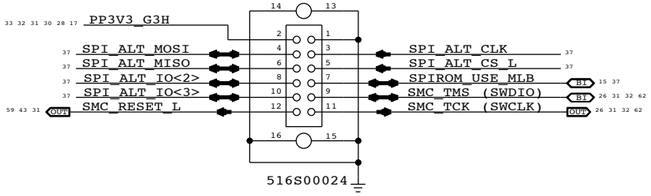
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



SPI+SWD SAM Connector

CRITICAL

J6100
DF40PC-12DP-0.4V-51
M-ST-SM



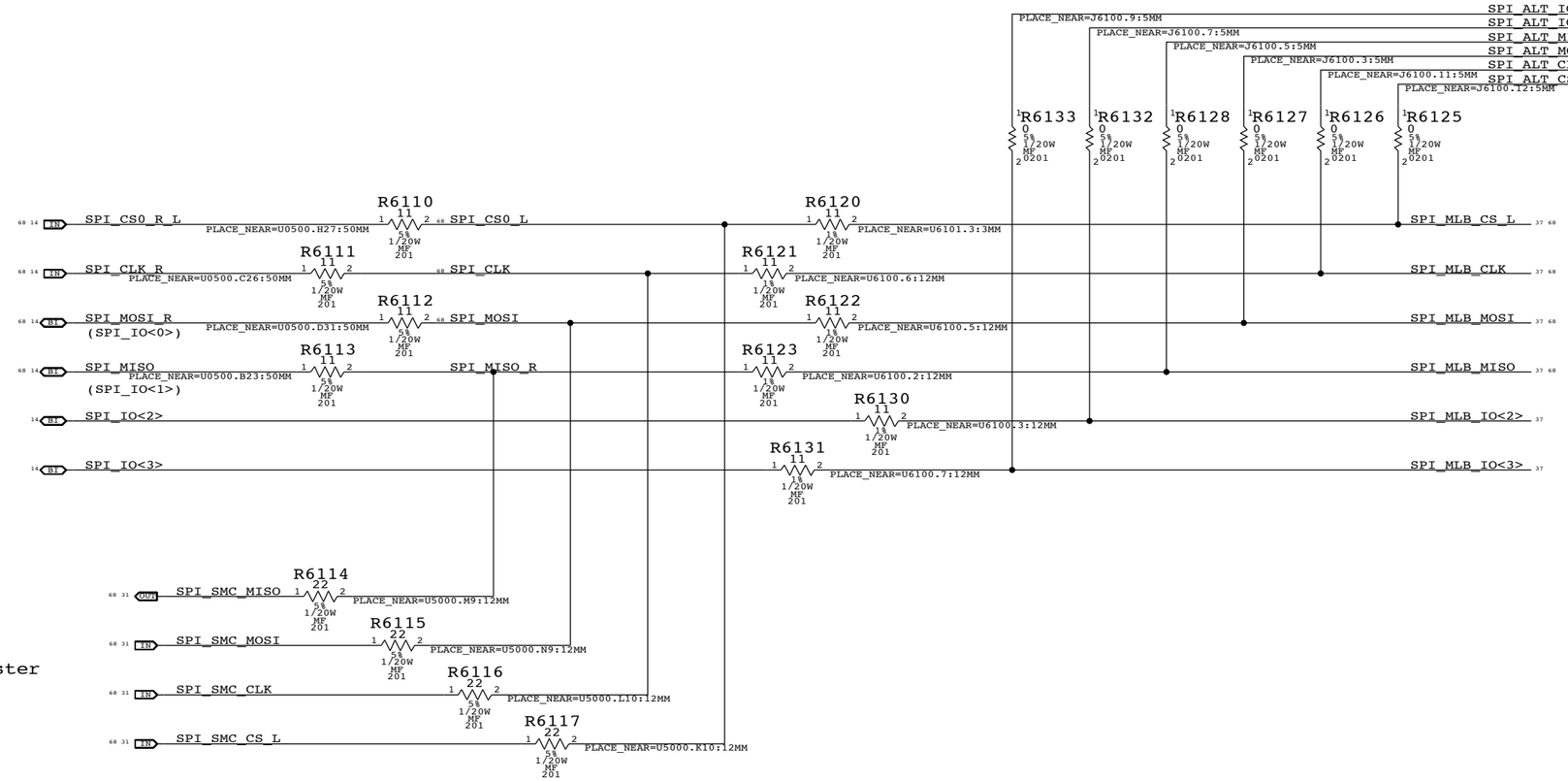
BootROM SPI Bus Series Termination

CPU Master

SMC12 Master

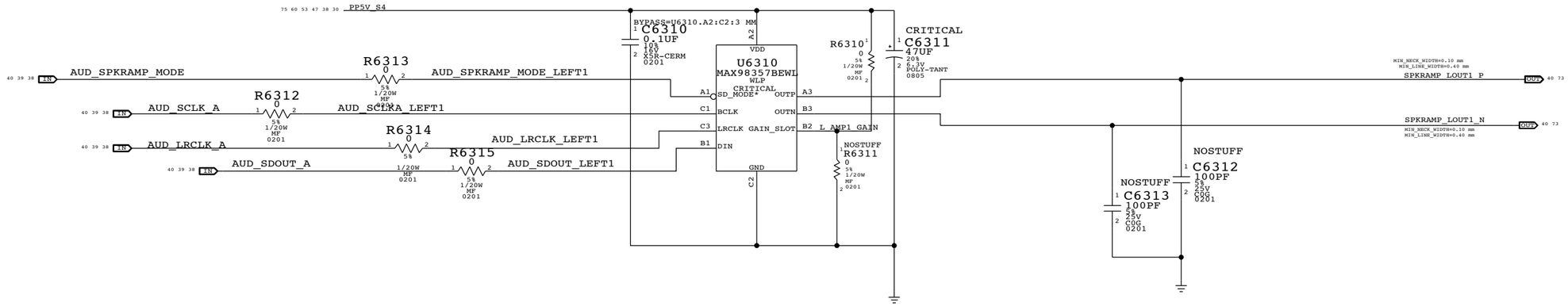
Sam Card ROM Slave

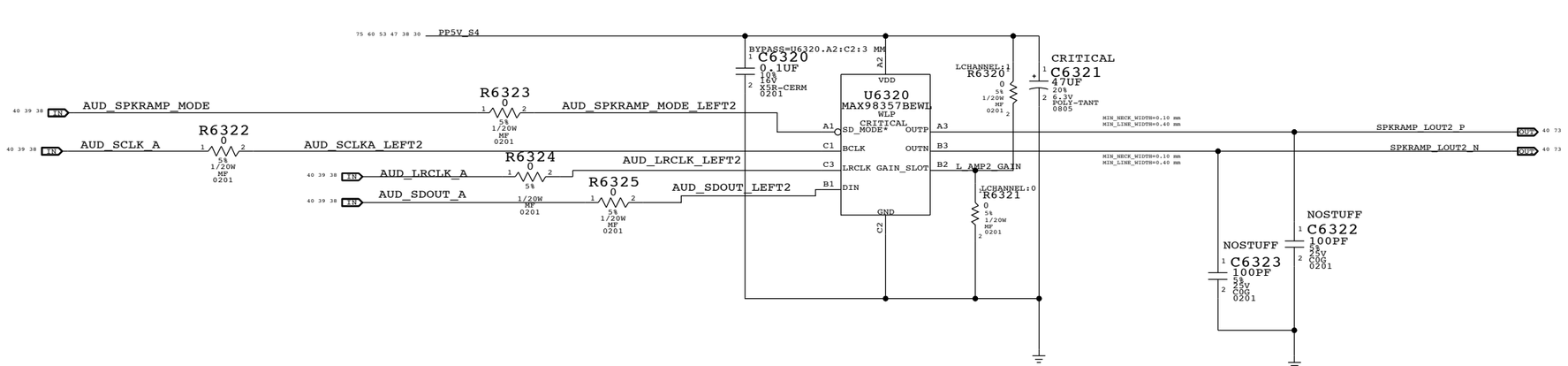
SPI ROM Slave



Left Speaker Amps

APPLE P/N 353S4265





SPEAKER CONFIGS

BOM GROUP	BOM OPTIONS
EQ:2CH	LCHANNEL:1,RCHANNEL:3
EQ:4CH	LCHANNEL:0,RCHANNEL:4

SYNC MASTER=J92 DEVMLB SYNC DATE=09/19/2013

PAGE TITLE: Audio:Left Speaker Amps

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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BRANCH: <BRANCH>

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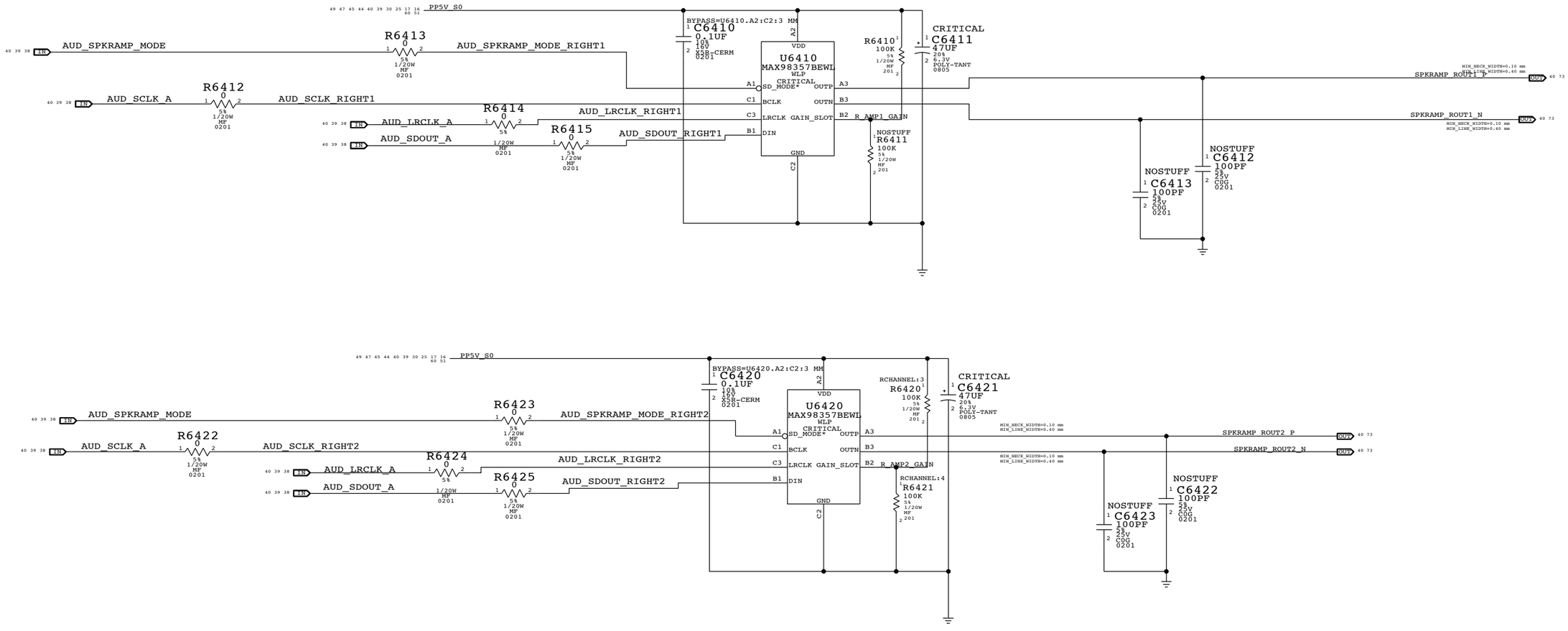
Right Speaker Amps

APPLE P/N 353S4265



SYNC_MASTER=J92_DEVMLB	SYNC_DATE=09/19/2013
PAGE TITLE	Audio:Right Speaker Amps
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY:	BRANCH <BRANCH>
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	SHEET 39 OF 75

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)		0X09 (A)
SPEAKERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A

CODEC INPUT SIGNAL PATHS

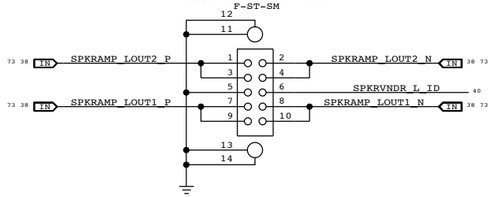
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SOUTHBRIDGE RESOURCE/PIN ALLOCATIONS

FUNCTION	NET NAME	SB GPIO/INT
PERIPHERAL/EXTRACTION DETECT	AUD_IP_PERIPHERAL_DET	GPIO 3
MIKEY INTERRUPT	AUD_I2C_INT_L	GPIO 5
MIKEY ENABLE	AUD_IPHS_SWITCH_EN	GPIO 16
MIKEY I2C BUS	I2C_MIKEY_SDA/SCL	2CH SMBUS 0

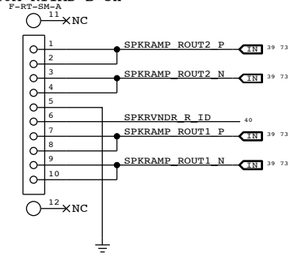
LEFT SPEAKER CONN

516S0899
CRITICAL
J6750
AA07A-S010-VA1
F-ST-SM

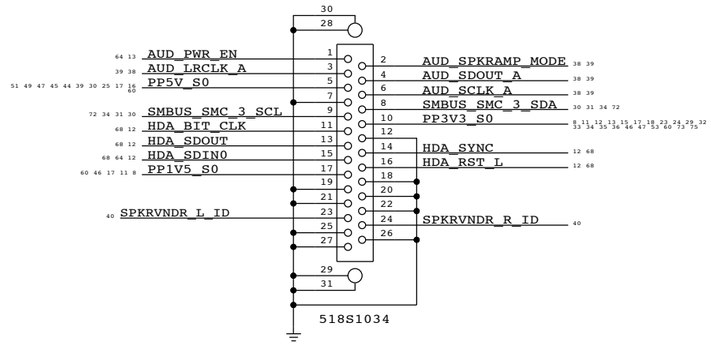


RIGHT SPEAKER CONN

518S00014
CRITICAL
J6751
FF18-10A-R11AD-B-3H
F-RT-SM-A



CRITICAL
J6799
502250-8027
F-RT-SM



518S1034

RIO FLEX CONN

SYNC_MASTER=CARA J92 SYNC_DATE=04/17/2014

PAGE TITLE
AUDIO: CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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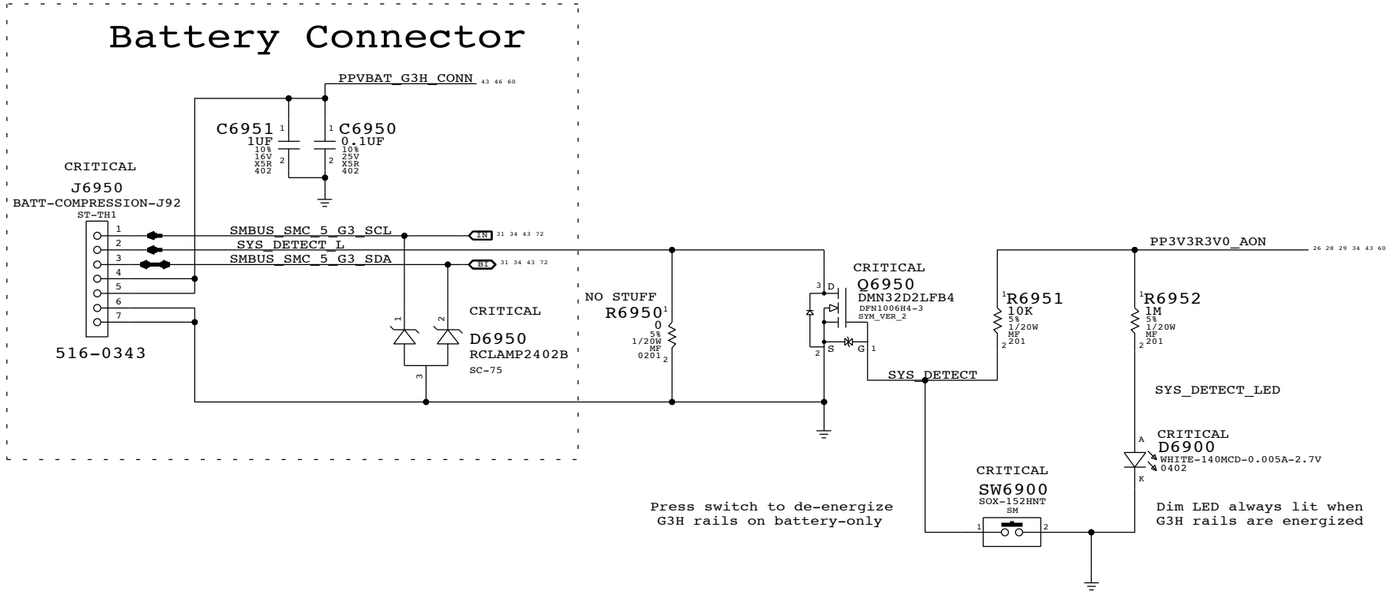
Battery Connector



SYNC MASTER=J43_MLB SYNC DATE=10/24/2012

PAGE TITLE: Battery Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 69 OF 130

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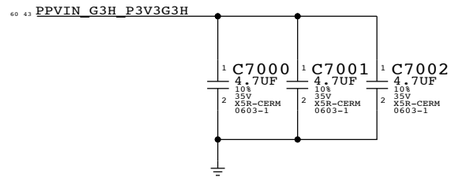
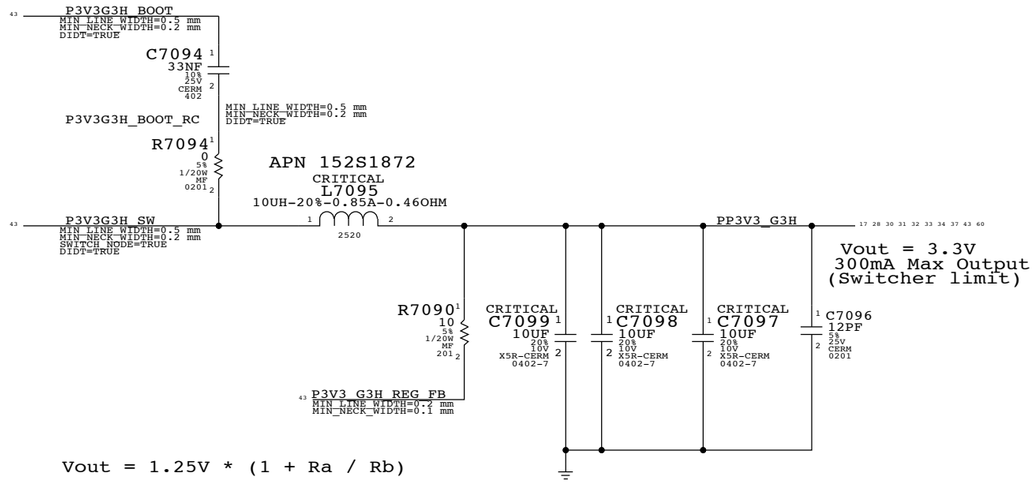
3.3V G3H VR - Bansuri





Vout = 1.25V * (1 + Ra / Rb)

SYNC MASTER=J92 WILL SYNC DATE=02/04/2013

PAGE TITLE
3.3V G3Hot Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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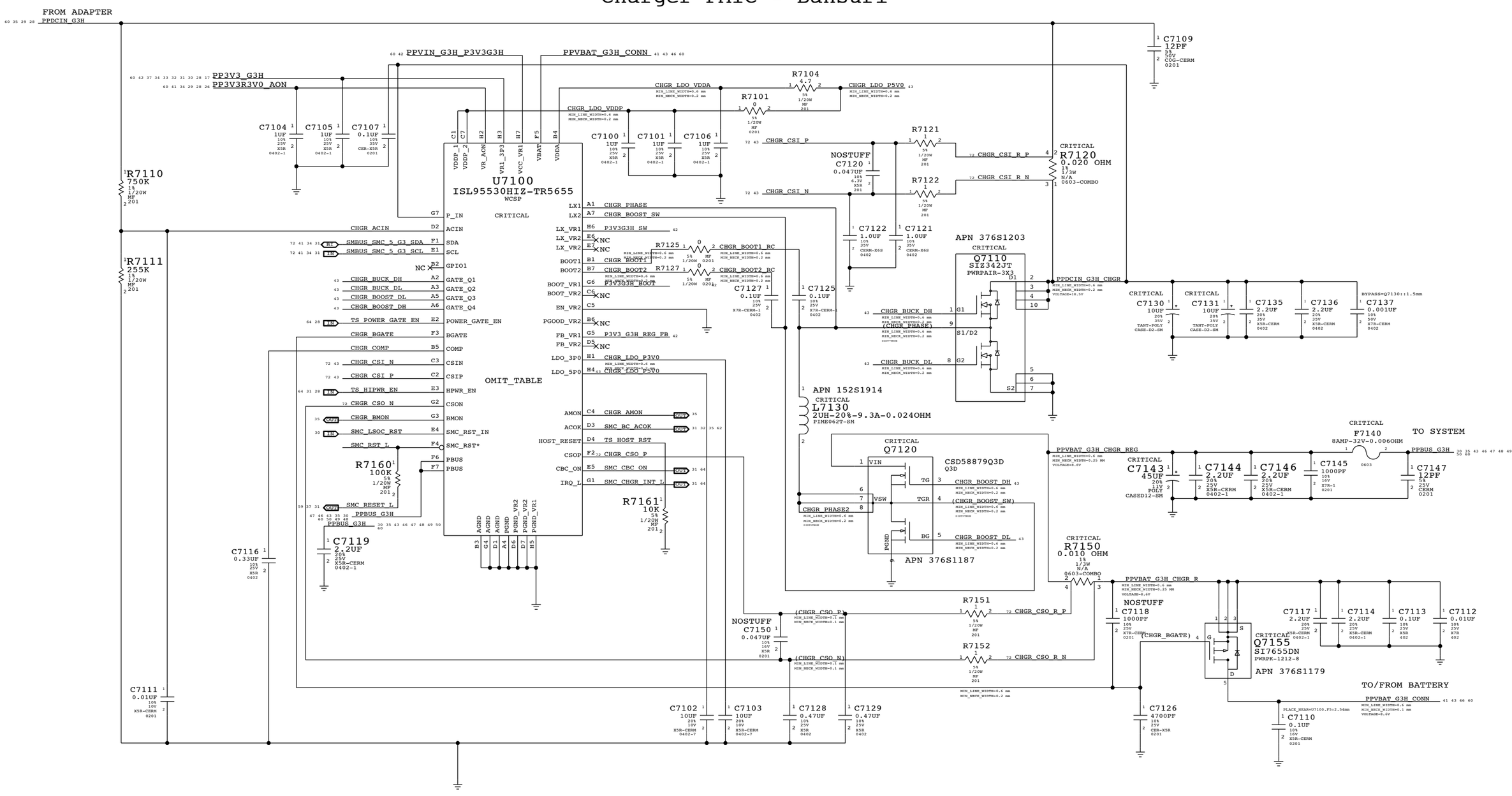
Charger PMIC - Bansuri



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00347	1	IC,ISL95530B1T11,CHGR PMU,BANSURI,WCSP56	U7100	CRITICAL	

SYNC_MASTER=J92_DEVMLB SYNC_DATE=04/04/2014

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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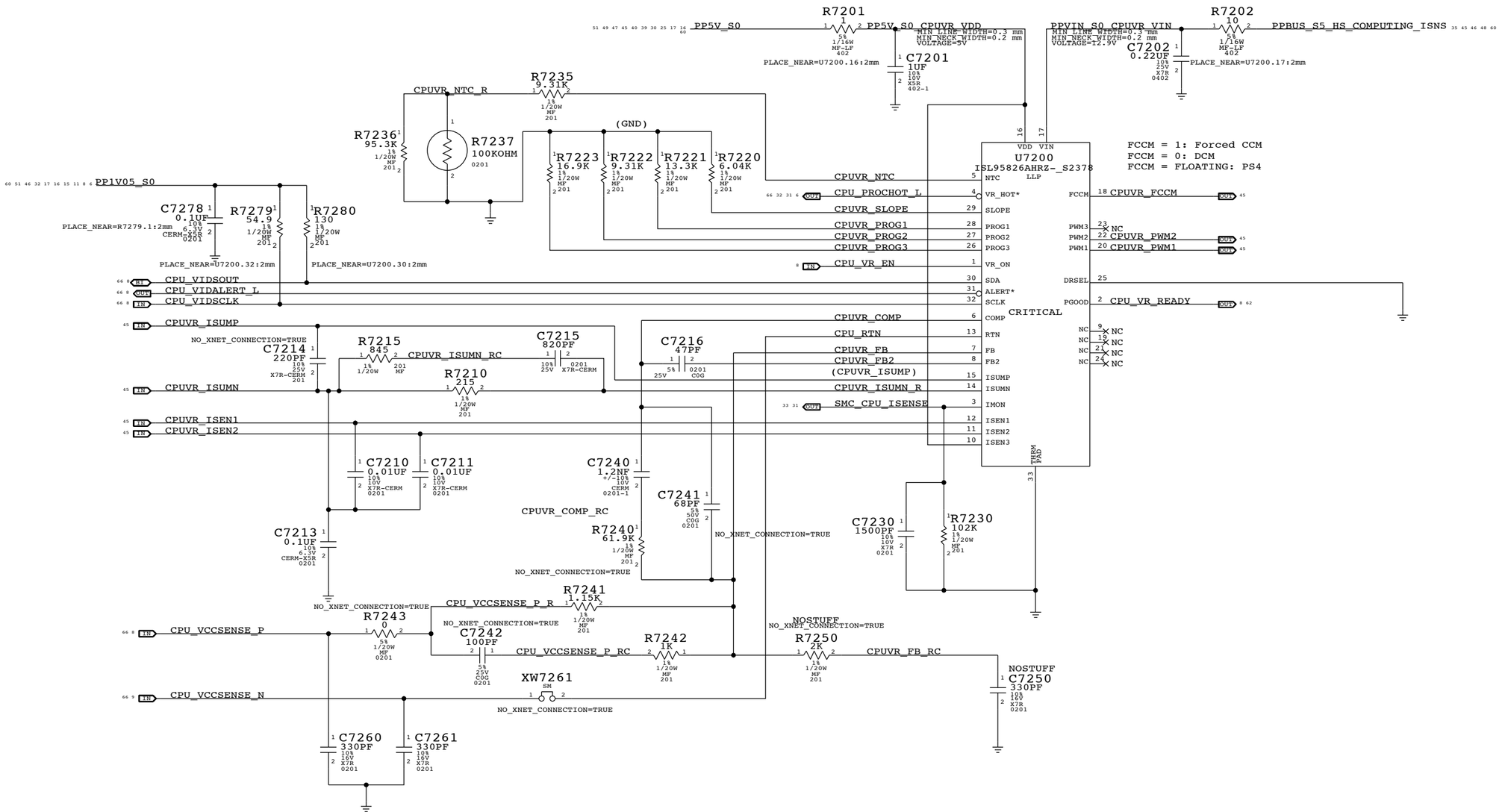

SYNC_MASTER=J43_MLB SYNC_DATE=10/09/2012

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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PPBUS_S5_HS_COMPUTING_ISNS

PP5V_S0

PHASE 1

U7310 ISL6208D DFN

CPUVR_PWM1

CPUVR_FCCM

CPUVR_UGATE1

CPUVR_LGATE1

CPUVR_BOOT1

CRITICAL Q7310 SISA18JN_GE3 PWRPAK-SM

CRITICAL Q7311 SISA12JN_GE3 PWRPAK-SM

353S3942

C7310 1UF 10% 16V X6S-CERM 0402

R7311 2.2 5% 1/16W MF-LF 402

C7311 0.22UF 10% 16V CERM 402

CRITICAL C7370 45UF 20% 11V POLY CASED12-SM

CRITICAL C7372 45UF 20% 11V POLY CASED12-SM

C7315 2.2UF 20% 25V X5R 0402-1

152S1915 CRITICAL L7310 0.4UH-20%-14A-0.005OHM PILE062T-SM

CPUVR_PHASE1

PPVCC_S0_CPU_PH1

CRITICAL R7310 0.00075 1% 1W MF 0612-1

CPUVR_ISNS1_P

CPUVR_ISNS1_N

NO_XNET_CONNECTION=TRUE

R7314 1.00 1% 1/20W MF-LP 0201

CPUVR_ISUMN

R7315 1K 1% 1/20W MF 201

R7316 200K 1% 1/20W MF 201

OMIT R7317 NOSTUFF NONE NONE NONE 0201

CPUVR_ISNS2_N

CPUVR_ISEN1

CPUVR_ISUMP

CRITICAL C7323 45UF 20% 11V POLY CASED12-SM

C7325 2.2UF 20% 25V X5R 0402-1

PHASE 2

U7320 ISL6208D DFN

CPUVR_PWM2

CPUVR_FCCM

CPUVR_UGATE2

CPUVR_LGATE2

CPUVR_BOOT2

CRITICAL Q7320 SISA18JN_GE3 PWRPAK-SM

CRITICAL Q7321 SISA12JN_GE3 PWRPAK-SM

353S3942

C7320 1UF 10% 16V X6S-CERM 0402

R7321 2.2 5% 1/16W MF-LF 402

C7321 0.22UF 10% 16V CERM 402

152S1915 CRITICAL L7320 0.4UH-20%-14A-0.005OHM PILE062T-SM

CPUVR_PHASE2

PPVCC_S0_CPU_PH2

CRITICAL R7320 0.00075 1% 1W MF 0612-1

CPUVR_ISNS2_P

CPUVR_ISNS2_N

NO_XNET_CONNECTION=TRUE

R7324 1.00 1% 1/20W MF-LP 0201

CPUVR_ISUMN

R7325 1K 1% 1/20W MF 201

R7326 200K 1% 1/20W MF 201

OMIT R7327 NOSTUFF NONE NONE NONE 0201

CPUVR_ISNS1_N

CPUVR_ISEN2

CPUVR_ISUMP

PPVCC_S0_CPU

Vout = 1.85V max
27A max load
f = 700kHz

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE: CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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TPS650811 (Walrus):

- OTP
- Power-up State Machine
- 32kHz / 24MHz
- RTC Domain
- Coin Cell Charger
- Overtemp V12.6 Interface
- Power Button
- AC/DC Detection
- EC RESET
- Emergency RESET Handler
- V3 Converter (V5Dx_WP)
- V6 Converter (V3.3Dx_SSD)
- V7 Converter (V1.8U)
- V10 Controller (V1.2U)
- V11 LDO (V0.6Dx)
- V12 LDO (2.5V/1.5V)
- Ref Sys
- GPIOs
- ADC
- Power Monitor Unit
- Interrupt Handler
- Battery Detection
- Digital Block
- I2C

- 3V LDO
- 5V LDO

V10 (V1.2U VR)

V12 LDO (1.5V)

SYNC MASTER=J92_DEVMLB	SYNC DATE=04/04/2014
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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PPBUS_G3H

CRITICAL
C7540 45UF 20% 11V POLY CASED12-SM
V4
C7541 2.2UF 20% 25V X5R-CERM 0402-1
C7544 2.2UF 20% 25V X5R-CERM 0402-1
C7570 1000PF 10% 16V X7R-1 0201
V3
C7542 2.2UF 20% 25V X5R-CERM 0402-1
C7543 2.2UF 20% 25V X5R-CERM 0402-1
C7573 1000PF 10% 16V X7R-1 0201

CRITICAL
C7580 45UF 20% 11V POLY CASED12-SM
NOSTUFF
C7587 2.2UF 20% 25V X5R-CERM 0402-1
V6
C7581 2.2UF 20% 25V X5R-CERM 0402-1
C7583 1000PF 10% 16V X7R-1 0201
V5
C7582 2.2UF 20% 25V X5R-CERM 0402-1
NOSTUFF
C7588 2.2UF 20% 25V X5R-CERM 0402-1
C7584 1000PF 10% 16V X7R-1 0201
V2
C7585 2.2UF 20% 25V X5R-CERM 0402-1
C7589 2.2UF 20% 25V X5R-CERM 0402-1
C7586 1000PF 10% 16V X7R-1 0201

5V S4 - 2.7A

CRITICAL
L7510 2.2UH-20%-4.8A-0.105OHM SM-PIME041B

Vout = 5.0V
F = ??? KHZ

75 60 53 38 30 PP5V_S4
C7510 47UF 20% 6.3V POLY-TANT 0805
C7513 47UF 20% 6.3V POLY-TANT 0805
C7514 2.2UF 20% 25V X5R-CERM 0402-1
C7511 2.2UF 20% 25V X5R-CERM 0402-1
R7510 10 5% 1/20W MF 201
V2
C7512 4700PF 10% 10V X7R 201
P5VS4_PHASE 48 MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm DIDT=TRUE
P5VS4_BOOT 48 MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
P5V_S4_REG_FB 48 MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm

5V S0 - 2.9A

CRITICAL
L7520 2.2UH-20%-4.8A-0.105OHM SM-PIME041B

51 49 45 44 40 39 30 25 17 16 60 PP5V_S0
C7552 47UF 20% 6.3V POLY-TANT 0805
C7553 47UF 20% 6.3V POLY-TANT 0805
C7550 2.2UF 20% 25V X5R-CERM 0402-1
PLACE_NEAR=L7520.1:1.5mm
C7551 2.2UF 20% 25V X5R-CERM 0402-1
C7571 1000PF 10% 16V X7R-1 0201
R7520 10 5% 1/20W MF 201
V3
C7520 4700PF 10% 10V X7R 201
P5VS0_PHASE 46 MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm DIDT=TRUE
P5VS0_BOOT 46 MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
P5V_S0_REG_FB 46 MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm

3.3V S0 - 1A

CRITICAL
L7562 2.2UH-2.2A PIFE32251B

V5
48 P3V3S0_PHASE MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm DIDT=TRUE
C7562 4700PF 10% 10V X7R 201
R7562 10 5% 1/20W MF 201
48 P3V3S0_BOOT MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
48 P3V3_S0_REG_FB MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
60 53 46 40 36 35 34 33 32 29 24 23 8 PP3V3_S0
C7595 2.2UF 20% 25V X5R-CERM 0402-1
NOSTUFF
C7569 2.2UF 20% 25V X5R-CERM 0402-1
C7598 47UF 20% 6.3V POLY-TANT 0805
C7599 47UF 20% 6.3V POLY-TANT 0805
C7563 12PF 5% 25V CERM 0201
NOSTUFF
C7564 12PF 5% 25V CERM 0201

3.3V SSD - 2A

CRITICAL
L7561 2.2UH-20%-3.8A-0.083OHM PIME041B-SM

V6
46 P3V3SSD_PHASE MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm DIDT=TRUE
C7561 4700PF 10% 10V X7R 201
R7561 10 5% 1/20W MF 201
46 P3V3SSD_BOOT MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
46 P3V3_SSD_REG_FB MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
60 59 58 50 PP3V3_S0SW_SSD
C7592 2.2UF 20% 25V X5R 0402-1
C7594 2.2UF 20% 25V X5R 0402-1
C7596 47UF 20% 6.3V POLY-TANT 0805
C7597 47UF 20% 6.3V POLY-TANT 0805
C7566 47UF 20% 6.3V POLY-TANT 0805
C7567 47UF 20% 6.3V POLY-TANT 0805

Vout = 3.3V

3.3V S5 - 1.5A

CRITICAL
L7560 2.2UH-2.2A PIFE32251B

PP3V3_S5
8 11 13 15 16 17 22 33 37 46 51 59 60 73 75
F = ??? KHZ

V4
48 P3V3S5_PHASE MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm DIDT=TRUE
C7560 4700PF 10% 10V X7R 201
R7560 10 5% 1/20W MF 201
48 P3V3S5_BOOT MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
48 P3V3_S5_REG_FB MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm
C7590 2.2UF 20% 25V X5R-CERM 0402-1
C7568 2.2UF 20% 25V X5R-CERM 0402-1
PLACE_NEAR=L7560.2:1.5mm
C7572 1000PF 10% 16V X7R-1 0201
C7591 47UF 20% 6.3V POLY-TANT 0805
C7593 47UF 20% 6.3V POLY-TANT 0805

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE: 5V & 3.3V Power Supplies

Apple Inc.

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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SHEET: 47 OF 75

TPS650801 (Dolphin):
- OTP
- I2C
- LED Drivers
- V2 Converter (V5A_DS3)
- V4 Converter (V3.3A_DSW)
- V5 Converter (V3.3Dx)
- V8 Converter (V1.5S - UNUSED)
- V9 Controller (V1.05A)
- 3V LDO
- 5V LDO
- Digital Block
- Ref Sys

CRITICAL
U7600
SN650801
BGA
SYM 2 OF 2
DEVICE CONTROL
INTERNAL BIASING

PMIC_ADC_EN F3
AGND_PMIC H4
PMIC2_READY H3
PMIC2_CRITTEMP H10
PMIC2_PROCHOT K4
PMIC2_THERMP E10
PMIC2_THERMN F10
PMIC_VREF3V3 A11 B10
PMIC2_VCTRL K6
PMIC2_VCTRL02 G3
PMIC_VREF3V3_RC K1
SMBUS_SMC_2_G3_SCL J8
SMBUS_SMC_2_G3_SDA H8
(Float = 0x34/0x35) NCX J3
TP_PMIC_LEDDRV1 K9
TP_PMIC_LEDDRV2 J7
TP_PMIC_LEDDRV3 K8
TP_PMIC_LEDDRV4 J6

IMON_EN VLDO3.3V_EN RDY CRITTEMP HOT TP TN VDDIO VDDIO VIN5V VCTRL2 VIN3.VA SCL SDA SLAVEADDR LEDDRV1 LEDDRV2 LEDDRV3 LEDDRV4

VIN L9
VINLDO3.3V D8
VLDO3.3V B11
VREF1.25V D9
VCTRL0 J2
VCTRL K7
AGND J1
AGND K10
AGND L11
GND F9 H2 L10 D5 D6 E4 E5 E6 E7 E8 F4 F5 F6 F7 F8 G4 G5 G6 G7 G8 H5 H6 H7

PPBUS_G3H
PMIC_VREF3V3
PMIC2_VREF1V25
PMIC2_VCTRL02
PMIC2_VCTRL
AGND_PMIC

C7603 10UF 20% 6.3V CERM-X6S 0402
C7608 10UF 20% 6.3V CERM-X6S 0402
C7607 10UF 20% 6.3V CERM-X6S 0402
C7604 1UF 20% 10V X5R 0201
C7605 1UF 20% 10V X5R 0201
C7606 2.2UF 20% 6.3V X5R-CERM 0201
C7600 2.2UF 20% 25V X5R-CERM 0402-1

R7602 10 5% 1/16W MF-LF 402
C7601 0.1UF 10% 10V X5R-CERM 0201
C7602 1.0UF 20% 6.3V X5R 0201-1
XW7699 SM

CRITICAL
U7600
SN650801
BGA
SYM 1 OF 2

V2_EN V2_MODE PGOOD2 V2_IMON — V2-V5A_DS3
VIN2 L6 VIN2 L7 BOOTSTRAP2 L8 LX2 L4 LX2 L5 PGND2 L2 PGND2 L3 VOUT2 K3 FB2 L1 FB2 K2
P5V_S4_EN K5
P5V_S4_MODE J5
P5V_S4_PGOOD J4
P5V_S4_IMON C10
PPBUS_G3H
P5VS4_BOOT
P5VS4_PHASE
P5V_S4_REG_FB

V4_EN V4_MODE PGOOD4 V4_IMON — V4-V3.3A-DSW
VIN4 E11 VIN4 F11 BOOTSTRAP4 D11 LX4 G11 LX4 H11 PGND4 J11 PGND4 K11 VOUT4 J9 FB4 J10
P3V3_S5_EN G10
P3V3_S5_MODE G9
S5_PWRGD H9
P3V3_S5_IMON E9
P3V3S5_BOOT
P3V3S5_PHASE
P3V3_S5_REG_FB

V5_EN V5_MODE PGOOD5 V5_IMON — V5-V3.3DX
VIN5 F1 VIN5 G1 BOOTSTRAP5 H1 LX5 D1 LX5 E1 PGND5 B1 PGND5 C1 VOUT5 C2 FB5 A1 FB5 B2
P3V3_S0_EN E3
P3V3_S0_MODE E2
P3V3_S0_PGOOD D3
P3V3_S0_IMON C11
P3V3S0_BOOT
P3V3S0_PHASE
P3V3_S0_REG_FB

V8_EN V8_MODE V8SEL PGOOD8 V8_IMON — V8-V1.5S
VIN8 A5 VIN8 A6 BOOTSTRAP8 B6 LX8 A7 LX8 A8 PGND8 A9 PGND8 A10 VOUT8 B9 FB8 C9
B7 C8 D2 D7 D10
NC NC NC NC NC
PPBUS_G3H
R7635 8.66K 1% 1/20W MF 201

V9_EN V9_MODE PGOOD9 V9_IMON V9_ULQ ILIMSET9 — V9-V1.05A
VBST9 B4 SW9 A4 DRVH9 B5 DRVL9 A2 PGND9 A3 ISP9 C4 ISM9 C5 FB9 C6
P1V05_SUS_EN B8
P1V05_SUS_MODE C7
P1V05_SUS_PGOOD G2
P1V05_SUS_IMON D4
P1V05_ULQ_L F2
P1V05_SUS_ILIM B3
ISNS_1V05_SUS_P
ISNS_1V05_SUS_N

V9 (V1.05A VR)

PPBUS_S5_HS_COMPUTING_ISNS
C7620 45UF 20% 11V POLY CASED12-SM
C7622 1000PF 5% 25V CERM 0402
C7624 2.2UF 20% 25V X5R-CERM 0402-1
C7625 2.2UF 20% 25V X5R-CERM 0402-1 NOSTUFF

P1V05SUS_BOOT_RC
C7630 0.1UF 10% 16V X7R-CERM 0402
R7630 0 5% 1/16W MF 402
P1V05SUS_VBST
P1V05SUS_DRVH
P1V05SUS_LL
P1V05SUS_DRVL

APN 376S00012
CRITICAL
Q7630
CSD58889Q3D
Q3D
VIN 1 TG 3 TGR 4 VSW 6 7 8 BG 5 PGND 9

APN 152S1913
CRITICAL
L7630
1UH-20%-10.2A-0.014OHM
PIME052T-SM
P1V05_SUS_PHASE
XW7601 SM
P1V05_SUS_PHASE_XW
R7634 121K 1% 1/20W MF 201
XW7600 SM BB: to 12nF
NO_XNET_CONNECTION=TRUE
C7634 0.015UF 10% 6.3V X5R 0201
ISNS_1V05_SUS_RC
NO_XNET_CONNECTION=TRUE
R7636 0201 100KOHM
ISNS_1V05_SUS_NTC
R7640 31.6K 1% 1/20W MF 201
R7637 20K 1% 1/20W MF 201
XW7610 SM
NO_XNET_CONNECTION=TRUE

PP1V05_SUS
Vout = 1.05V
5A Max Output
f = ? kHz
C7626 10UF 20% 10V X5R-CERM 0402-1
C7623 10UF 20% 10V X5R-CERM 0402-1
CRITICAL C7648 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C7649 270UF 20% 2V TANT CASE-B2-SM
C7647 12PF 5% 25V CERM 0201

R7641 10 1% 1/20W MF 201
P1V05SUS_VDDQSNS
P1V05SUS_VDDQSNS_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm

C7636 0.47UF 10% 6.3V CERM-X5R 0201
AGND_PMIC

SYNC_MASTER=J92_DEVMLB SYNC_DATE=04/04/2014
PAGE TITLE: 1.05V S0 Power Supply
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
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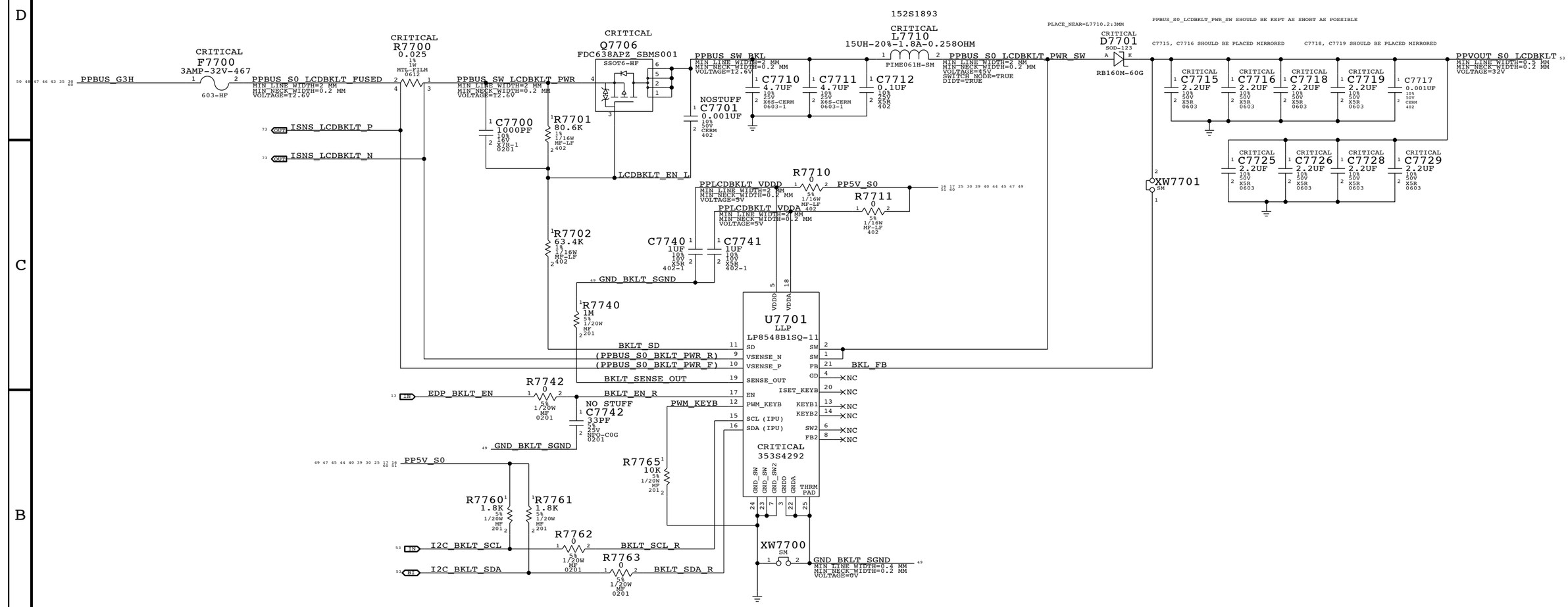
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (6-8.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production



SYNC MASTER=J92 DEVMLB SYNC DATE=10/01/2013

PAGE TITLE
LCD Backlight Driver

Apple Inc.

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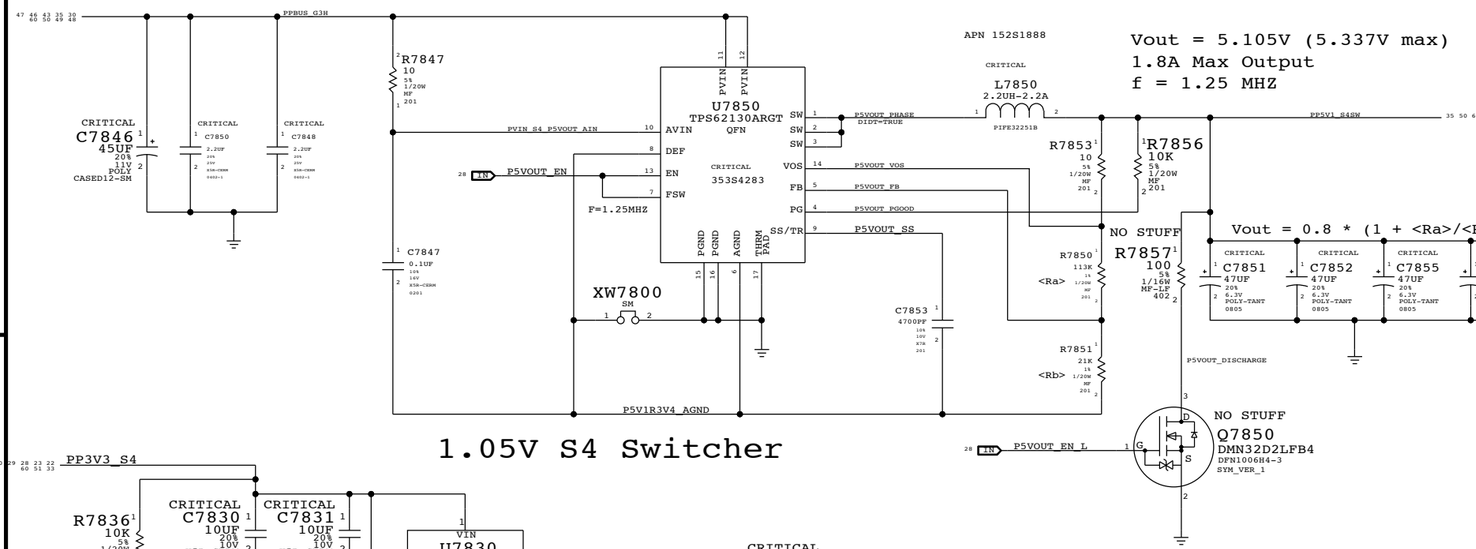
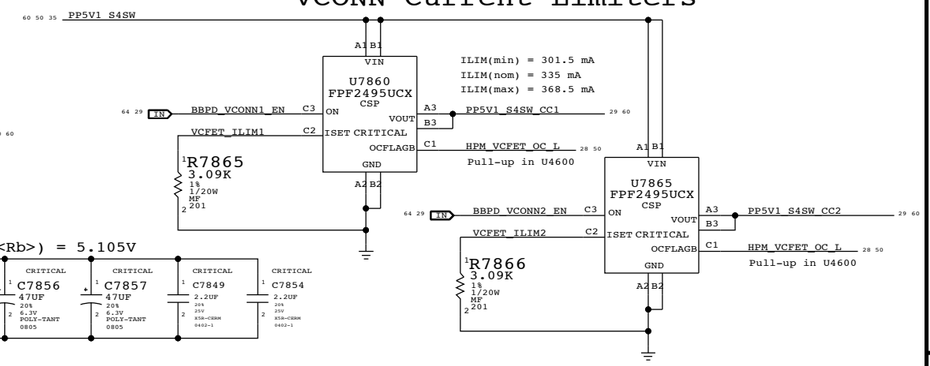
E85 VBUS/VCONN 5V VR

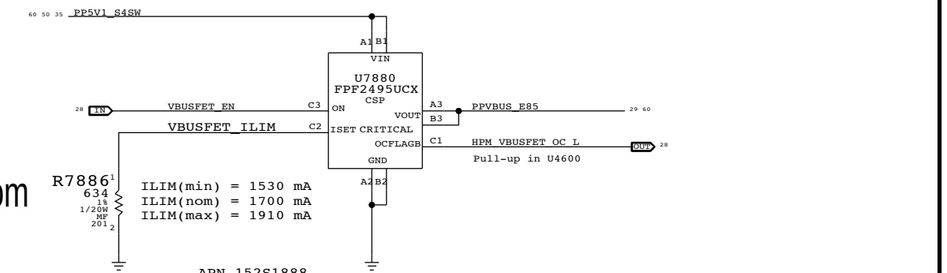


1.05V S4 Switcher

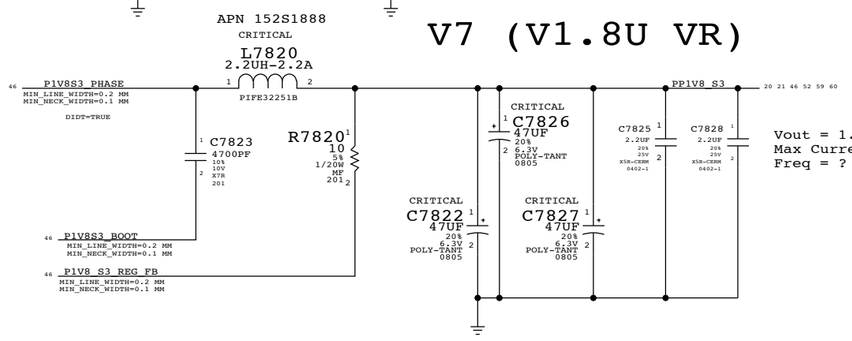
VCONN Current Limiters



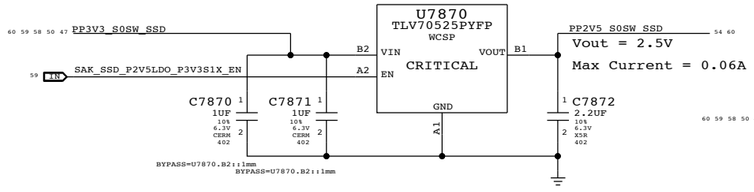
VBUS Current Limiter/OVP IC



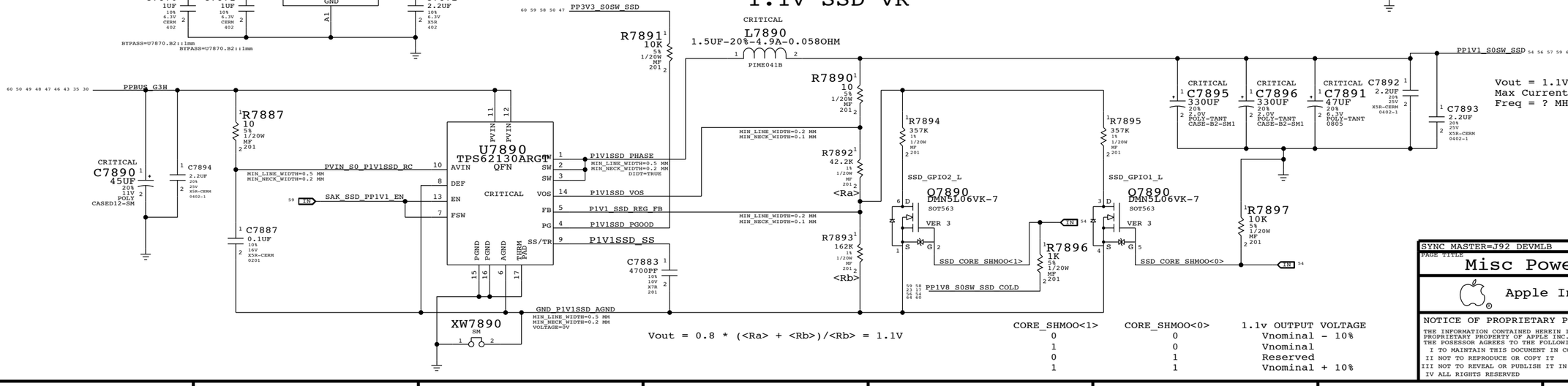
V7 (V1.8U VR)



2.5V SSD LDO



1.1V SSD VR



CORE_SHMOO<1>	CORE_SHMOO<0>	1.1v OUTPUT VOLTAGE
0	0	Vnominal - 10%
1	0	Vnominal
0	1	Reserved
1	1	Vnominal + 10%

SYNC_MASTER=J92_DEVMLB SYNC_DATE=04/04/2014

PAGE TITLE: Misc Power Supplies

Apple Inc.

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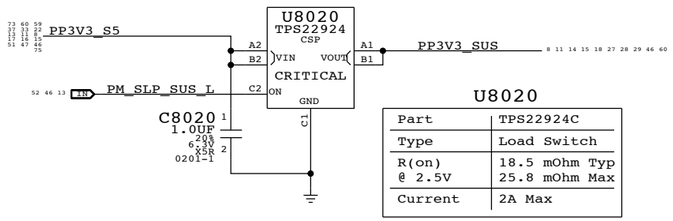
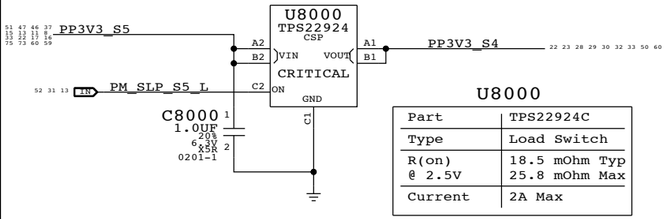
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

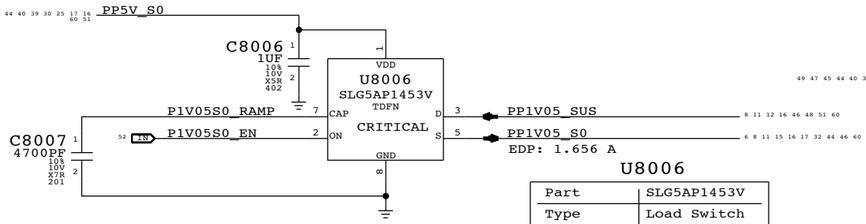
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

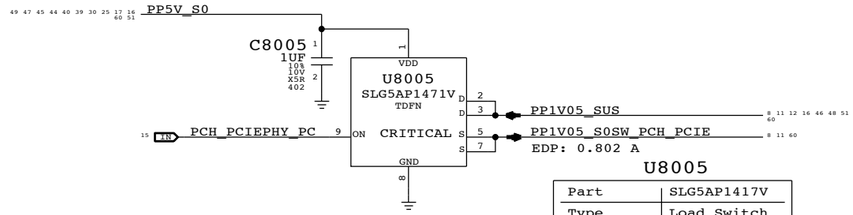
1.05V S0 Switch



U8006

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH PCIe Switch

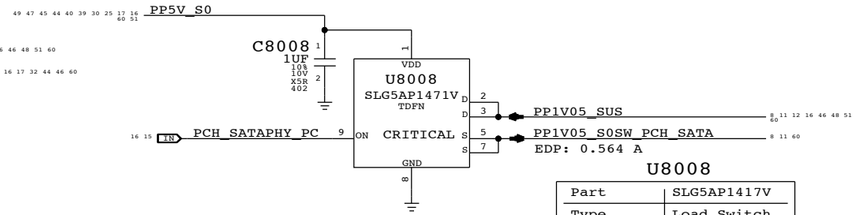


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH SATA Switch

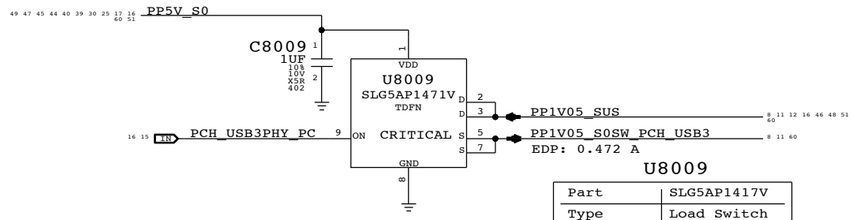


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8008

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH USB3 Switch



HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8009

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/24/2013

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SUS & S4 Enables

52 51 31 13 IN PM_SLP_S5_L — MAKE_BASE=TRUE — PM_SLP_S5_L OUT 13 31 51 52

52 51 46 13 IN PM_SLP_SUS_L — MAKE_BASE=TRUE — PM_SLP_SUS_L OUT 13 46 51 52

S3 Enables

46 IN PMIC_V8_EN

R8117 0 5% 1/20W MF 0201

46 31 15 13 IN PM_SLP_S4_L

NO STUFF D8115 0201 RB521ES-30

P1V8S3_EN_D

NO STUFF R8116 30K 5% 1/20W MF 201

NO STUFF R8115 1K 5% 1/20W MF 201

52 46 P1V8S3_EN — MAKE_BASE=TRUE — P1V8S3_EN OUT 46 52

NO STUFF C8116 0.1UF 10% 6.3V CERM-X5R 0201

S5 Power Good

52 48 46 31 IN S5_PWRGD — MAKE_BASE=TRUE — S5_PWRGD OUT 31 46 48 52

S0 Enables

46 31 13 IN PM_SLP_S3_L

D8182 0201 RB521ES-30 — P1V5S0_EN_D — R8182 4.99K 1% 1/20W MF 201 — R8185 30K 5% 1/20W MF 201

D8181 0201 RB521ES-30 — P3V3S0_EN_D — R8181 2.0K 5% 1/20W MF 201 — R8186 20K 5% 1/20W MF 201

D8183 0201 RB521ES-30 — P1V05S0_EN_D — R8183 1K 5% 1/20W MF 201 — R8184 10K 5% 1/20W MF 201

R8187 0 5% 1/20W MF 201

C8185 0.1UF 10% 6.3V CERM-X5R 0201

C8186 0.1UF 10% 6.3V CERM-X5R 0201

C8184 0.1UF 10% 6.3V CERM-X5R 0201

NO STUFF C8187 0.1UF 10% 6.3V CERM-X5R 0201

52 46 P5VS0_EN — MAKE_BASE=TRUE — P5VS0_EN OUT 46 52

52 51 P1V05S0_EN — MAKE_BASE=TRUE — P1V05S0_EN OUT 51 52

52 46 P3V3S0_EN — MAKE_BASE=TRUE — P3V3S0_EN OUT 46 52

52 46 P1V5S0_EN — MAKE_BASE=TRUE — P1V5S0_EN OUT 46 52

LPDDR power down sequencing support

PP1V8_S3 20 21 46 50 59 60

NO STUFF D8170 SOD-962 PMEG1201AESF

PP1V2_S3 8 10 19 20 21 46 59 60 69

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/20/2013

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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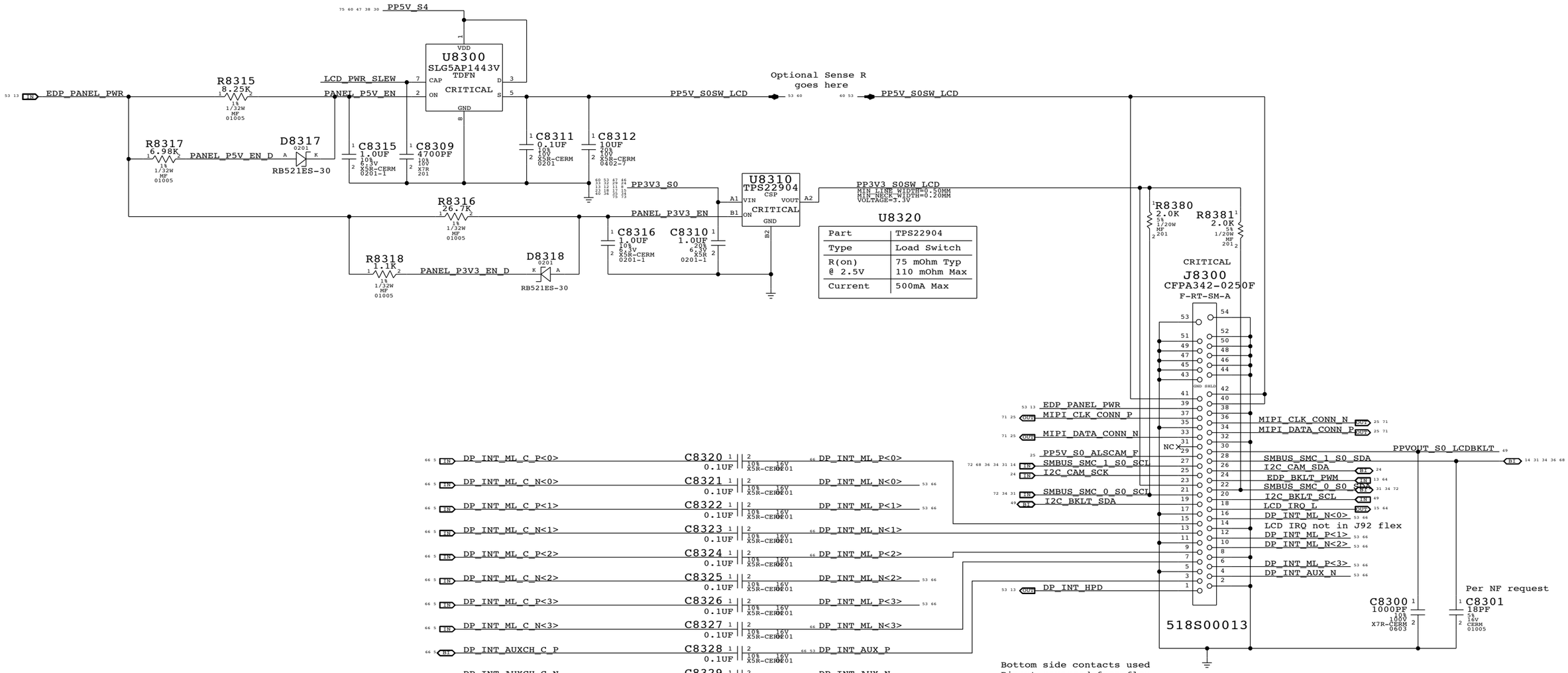
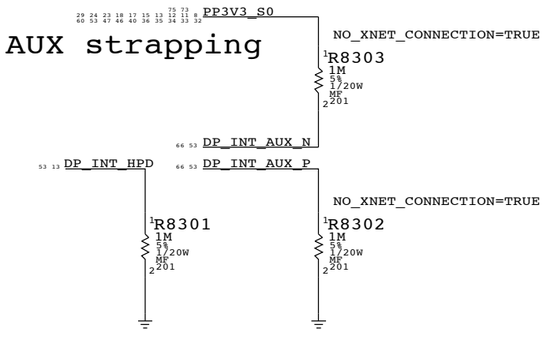
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



LCD Panel HPD & AUX strapping



SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/25/2013

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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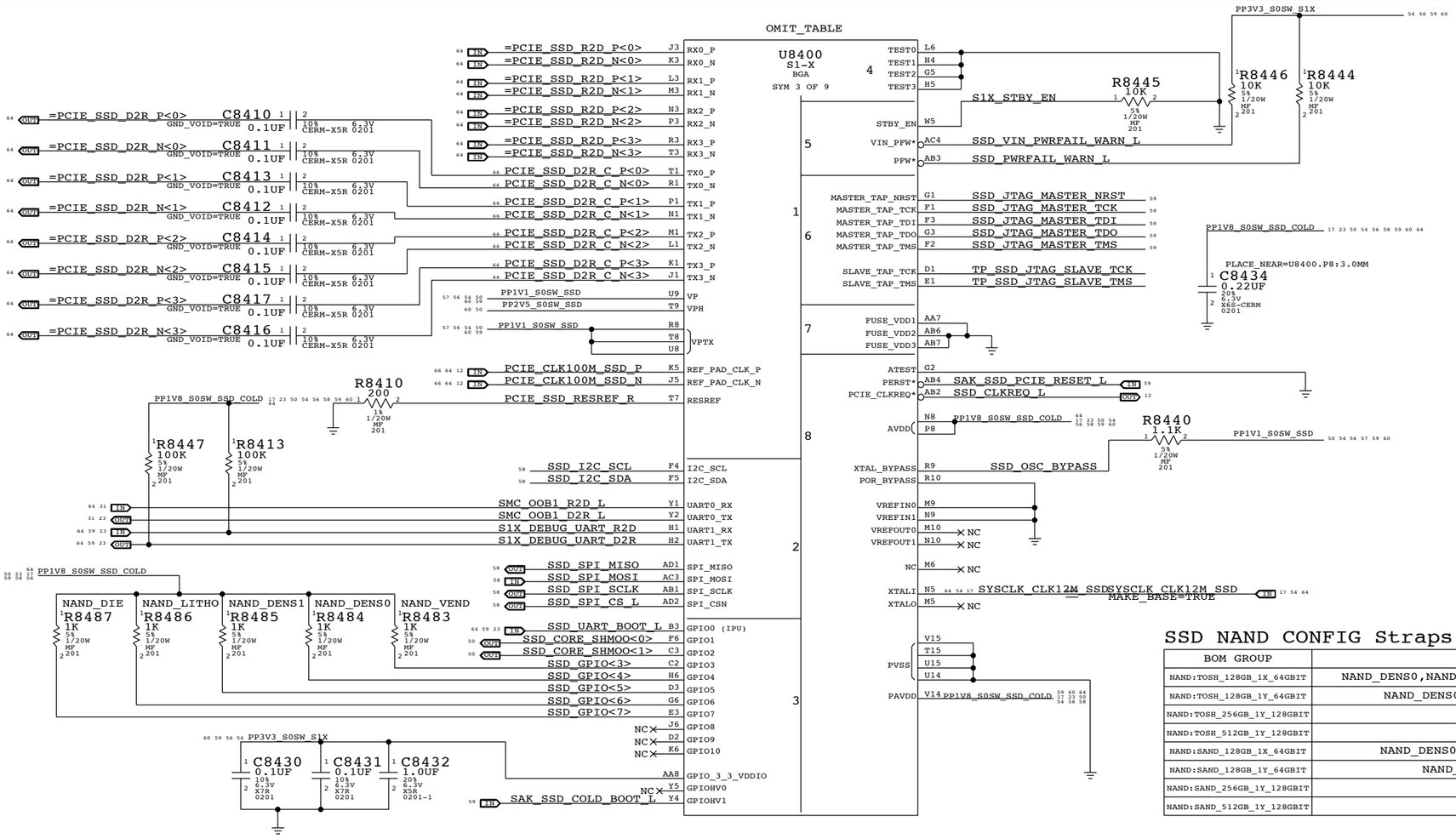

SSD NAND CONFIG Straps

BOM GROUP	BOM OPTIONS
NAND:TOSH_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_LITHO,NAND_DIE,NAND_TYPE:TOSH_128GB_1X_64GBIT
NAND:TOSH_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_DIE,NAND_TYPE:TOSH_128GB_1Y_64GBIT
NAND:TOSH_256GB_1Y_128GBIT	NAND_VEND,NAND_DENS1,NAND_TYPE:TOSH_256GB_1Y_128GBIT
NAND:TOSH_512GB_1Y_128GBIT	NAND_VEND,NAND_DENS0,NAND_TYPE:TOSH_512GB_1Y_128GBIT
NAND:SAND_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_LITHO,NAND_DIE,NAND_TYPE:SAND_128GB_1X_64GBIT
NAND:SAND_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_DIE,NAND_TYPE:SAND_128GB_1Y_64GBIT
NAND:SAND_256GB_1Y_128GBIT	NAND_DENS1,NAND_TYPE:SAND_256GB_1Y_128GBIT
NAND:SAND_512GB_1Y_128GBIT	NAND_DENS0,NAND_TYPE:SAND_512GB_1Y_128GBIT

S1-X GPIO[10:1] IPD

VENDOR	NAND_VEND(GPIO3)
TOSHIBA	1
SANDISK	0

DENSITY	NAND_DENS0(GPIO4)	NAND_DENS1(GPIO5)
128GB	1	1
256GB	0	1
512GB	1	0

LITHO	NAND_LITHO(GPIO6)
1X	1
1Y	0

DIE SIZE	NAND_DIE(GPIO7)
64Gb	1
128Gb	0

# NAND_CH	(GPIO8)
8 (X56)	1
4 (J92)	0

SSD NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-7360	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1X_64GBIT
335S00004	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1Y_64GBIT
335S1031	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_256GB_1Y_128GBIT
335S1032	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_512GB_1Y_128GBIT
998-7361	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1X_64GBIT
335S1044	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1Y_64GBIT
335S1041	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_256GB_1Y_128GBIT
335S1045	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_512GB_1Y_128GBIT

SYNC MASTER=J92 SSD SYNC DATE=02/11/2014

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Apple Inc.

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REVISION: <E4LABEL>
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70 58 OUT	ANI0_ALE	F18	ANI0_ALE	ANI2_ALE	E12	NC	
70 58 OUT	ANI0_CLE	D19	ANI0_CLE	ANI2_CLE	D11	NC	
70 58 BI	ANI0_DQS_N	B20	ANI0_DQS_N	ANI2_DQS_N	B14	NC	
70 58 BI	ANI0_DQS_P	A20	ANI0_DQS_P	ANI2_DQS_P	A14	NC	
70 58 BI	ANI0_IO<0>	B22	ANI0_IO0	ANI2_IO0	A16	NC	
70 58 BI	ANI0_IO<1>	A23	ANI0_IO1	ANI2_IO1	A11	NC	
70 58 BI	ANI0_IO<2>	B21	ANI0_IO2	ANI2_IO2	B16	NC	
70 58 BI	ANI0_IO<3>	A22	ANI0_IO3	ANI2_IO3	B11	NC	
70 58 BI	ANI0_IO<4>	A21	ANI0_IO4	ANI2_IO4	A12	NC	
70 58 BI	ANI0_IO<5>	B18	ANI0_IO5	ANI2_IO5	B12	NC	
70 58 BI	ANI0_IO<6>	A18	ANI0_IO6	ANI2_IO6	B15	NC	
70 58 BI	ANI0_IO<7>	C18	ANI0_IO7	ANI2_IO7	A15	NC	
70 58 OUT	ANI0_NCE<0>	E23	ANI0_NCE0	ANI2_NCE0	E16	NC	
70 58 OUT	ANI0_NCE<1>	D22	ANI0_NCE1	ANI2_NCE1	D15	NC	
70 58 OUT	ANI0_NCE<2>	E22	ANI0_NCE2	ANI2_NCE2	E15	NC	
70 58 OUT	ANI0_NCE<3>	D21	ANI0_NCE3	ANI2_NCE3	D14	NC	
NC		E21	ANI0_NCE4	ANI2_NCE4	E14	NC	
NC		D20	ANI0_NCE5	ANI2_NCE5	D13	NC	
NC		E20	ANI0_NCE6	ANI2_NCE6	E13	NC	
NC		E19	ANI0_NCE7	ANI2_NCE7	D12	NC	
70 58 BI	ANI0_NRE_N	B19	ANI0_NRE_N	ANI2_NRE_N	B13	NC	
70 58 BI	ANI0_NRE_P	A19	ANI0_NRE_P	ANI2_NRE_P	A13	NC	
70 58 OUT	ANI0_NWE	D23	ANI0_NWE	ANI2_NWE	D16	NC	
NC		D18	ANI0_PPM_IN	ANI2_PPM_IN	E11	NC	
NC		E18	ANI0_PPM_OUT	ANI2_PPM_OUT	F11	NC	
70 58 OUT	ANI1_ALE	D25	ANI1_ALE	ANI3_ALE	D5	NC	
70 58 OUT	ANI1_CLE	D26	ANI1_CLE	ANI3_CLE	E5	NC	
70 58 BI	ANI1_DQS_N	E28	ANI1_DQS_N	ANI3_DQS_N	B6	NC	
70 58 BI	ANI1_DQS_P	E29	ANI1_DQS_P	ANI3_DQS_P	A6	NC	
70 58 BI	ANI1_IO<0>	G28	ANI1_IO0	ANI3_IO0	B4	NC	
70 58 BI	ANI1_IO<1>	J29	ANI1_IO1	ANI3_IO1	A7	NC	
70 58 BI	ANI1_IO<2>	G29	ANI1_IO2	ANI3_IO2	C4	NC	
70 58 BI	ANI1_IO<3>	L29	ANI1_IO3	ANI3_IO3	B9	NC	
70 58 BI	ANI1_IO<4>	J28	ANI1_IO4	ANI3_IO4	B8	NC	
70 58 BI	ANI1_IO<5>	B26	ANI1_IO5	ANI3_IO5	A9	NC	
70 58 BI	ANI1_IO<6>	C26	ANI1_IO6	ANI3_IO6	A4	NC	
70 58 BI	ANI1_IO<7>	B25	ANI1_IO7	ANI3_IO7	A8	NC	
70 58 OUT	ANI1_NCE<0>	J25	ANI1_NCE0	ANI3_NCE0	D9	NC	
70 58 OUT	ANI1_NCE<1>	J26	ANI1_NCE1	ANI3_NCE1	E9	NC	
70 58 OUT	ANI1_NCE<2>	H25	ANI1_NCE2	ANI3_NCE2	D8	NC	
70 58 OUT	ANI1_NCE<3>	H26	ANI1_NCE3	ANI3_NCE3	E8	NC	
NC		G25	ANI1_NCE4	ANI3_NCE4	D7	NC	
NC		G26	ANI1_NCE5	ANI3_NCE5	E7	NC	
NC		F25	ANI1_NCE6	ANI3_NCE6	D6	NC	
NC		F26	ANI1_NCE7	ANI3_NCE7	E6	NC	
70 58 BI	ANI1_NRE_N	D27	ANI1_NRE_N	ANI3_NRE_N	B5	NC	
70 58 BI	ANI1_NRE_P	C27	ANI1_NRE_P	ANI3_NRE_P	A5	NC	
70 58 OUT	ANI1_NWE	K25	ANI1_NWE	ANI3_NWE	F9	NC	
NC		E26	ANI1_PPM_IN	ANI3_PPM_IN	D4	NC	
NC		E25	ANI1_PPM_OUT	ANI3_PPM_OUT	E4	NC	

0 2

1 3

OMIT_TABLE

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NC	AE12	ANI4_ALE	ANI6_ALE	AF25	ANI6_ALE	OUT	58 70
NC	AF11	ANI4_CLE	ANI6_CLE	AF26	ANI6_CLE	OUT	58 70
NC	AH14	ANI4_DQS_N	ANI6_DQS_N	AE28	ANI6_DQS_N	BI	58 70
NC	AJ14	ANI4_DQS_P	ANI6_DQS_P	AE29	ANI6_DQS_P	BI	58 70
NC	AJ11	ANI4_IO0	ANI6_IO0	W29	ANI6_IO<0>	BI	58 70
NC	AJ16	ANI4_IO1	ANI6_IO1	AC29	ANI6_IO<1>	BI	58 70
NC	AH11	ANI4_IO2	ANI6_IO2	AA28	ANI6_IO<2>	BI	58 70
NC	AH16	ANI4_IO3	ANI6_IO3	AG26	ANI6_IO<3>	BI	58 70
NC	AJ15	ANI4_IO4	ANI6_IO4	AH26	ANI6_IO<4>	BI	58 70
NC	AH15	ANI4_IO5	ANI6_IO5	AH25	ANI6_IO<5>	BI	58 70
NC	AJ12	ANI4_IO6	ANI6_IO6	AA29	ANI6_IO<6>	BI	58 70
NC	AH12	ANI4_IO7	ANI6_IO7	AC28	ANI6_IO<7>	BI	58 70
NC	AE16	ANI4_NCE0	ANI6_NCE0	AA25	ANI6_NCE<0>	OUT	58 70
NC	AF15	ANI4_NCE1	ANI6_NCE1	AA26	ANI6_NCE<1>	OUT	58 70
NC	AE15	ANI4_NCE2	ANI6_NCE2	AB25	ANI6_NCE<2>	OUT	58 70
NC	AF14	ANI4_NCE3	ANI6_NCE3	AB26	ANI6_NCE<3>	OUT	58 70
NC	AE14	ANI4_NCE4	ANI6_NCE4	AC25	NC		
NC	AF13	ANI4_NCE5	ANI6_NCE5	AC26	NC		
NC	AE13	ANI4_NCE6	ANI6_NCE6	AD25	NC		
NC	AF12	ANI4_NCE7	ANI6_NCE7	AD26	NC		
NC	AH13	ANI4_NRE_N	ANI6_NRE_N	AF27	ANI6_NRE_N	BI	58 70
NC	AJ13	ANI4_NRE_P	ANI6_NRE_P	AG27	ANI6_NRE_P	BI	58 70
NC	AF16	ANI4_NWE	ANI6_NWE	W25	ANI6_NWE	OUT	58 70
NC	AE11	ANI4_PPM_IN	ANI6_PPM_IN	AE26	NC		
NC	AD11	ANI4_PPM_OUT	ANI6_PPM_OUT	AE25	NC		
NC	AF5	ANI5_ALE	ANI7_ALE	AD18	ANI7_ALE	OUT	58 70
NC	AE5	ANI5_CLE	ANI7_CLE	AF19	ANI7_CLE	OUT	58 70
NC	AH7	ANI5_DQS_N	ANI7_DQS_N	AH21	ANI7_DQS_N	BI	58 70
NC	AJ7	ANI5_DQS_P	ANI7_DQS_P	AJ21	ANI7_DQS_P	BI	58 70
NC	AH5	ANI5_IO0	ANI7_IO0	AJ23	ANI7_IO<0>	BI	58 70
NC	AJ8	ANI5_IO1	ANI7_IO1	AH23	ANI7_IO<1>	BI	58 70
NC	AH4	ANI5_IO2	ANI7_IO2	AH22	ANI7_IO<2>	BI	58 70
NC	AH8	ANI5_IO3	ANI7_IO3	AJ22	ANI7_IO<3>	BI	58 70
NC	AJ9	ANI5_IO4	ANI7_IO4	AJ19	ANI7_IO<4>	BI	58 70
NC	AH9	ANI5_IO5	ANI7_IO5	AH19	ANI7_IO<5>	BI	58 70
NC	AJ4	ANI5_IO6	ANI7_IO6	AJ18	ANI7_IO<6>	BI	58 70
NC	AJ5	ANI5_IO7	ANI7_IO7	AH18	ANI7_IO<7>	BI	58 70
NC	AF9	ANI5_NCE0	ANI7_NCE0	AE23	ANI7_NCE<0>	OUT	58 70
NC	AE9	ANI5_NCE1	ANI7_NCE1	AF22	ANI7_NCE<1>	OUT	58 70
NC	AF8	ANI5_NCE2	ANI7_NCE2	AE22	ANI7_NCE<2>	OUT	58 70
NC	AE8	ANI5_NCE3	ANI7_NCE3	AF21	ANI7_NCE<3>	OUT	58 70
NC	AF7	ANI5_NCE4	ANI7_NCE4	AE21	NC		
NC	AE7	ANI5_NCE5	ANI7_NCE5	AF20	NC		
NC	AF6	ANI5_NCE6	ANI7_NCE6	AE20	NC		
NC	AE6	ANI5_NCE7	ANI7_NCE7	AE19	NC		
NC	AH6	ANI5_NRE_N	ANI7_NRE_N	AH20	ANI7_NRE_N	BI	58 70
NC	AJ6	ANI5_NRE_P	ANI7_NRE_P	AJ20	ANI7_NRE_P	BI	58 70
NC	AD9	ANI5_NWE	ANI7_NWE	AF23	ANI7_NWE	OUT	58 70
NC	AF4	ANI5_PPM_IN	ANI7_PPM_IN	AF18	NC		
NC	AE4	ANI5_PPM_OUT	ANI7_PPM_OUT	AE18	NC		

4 6

5 7

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/10/2013

PAGE TITLE
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Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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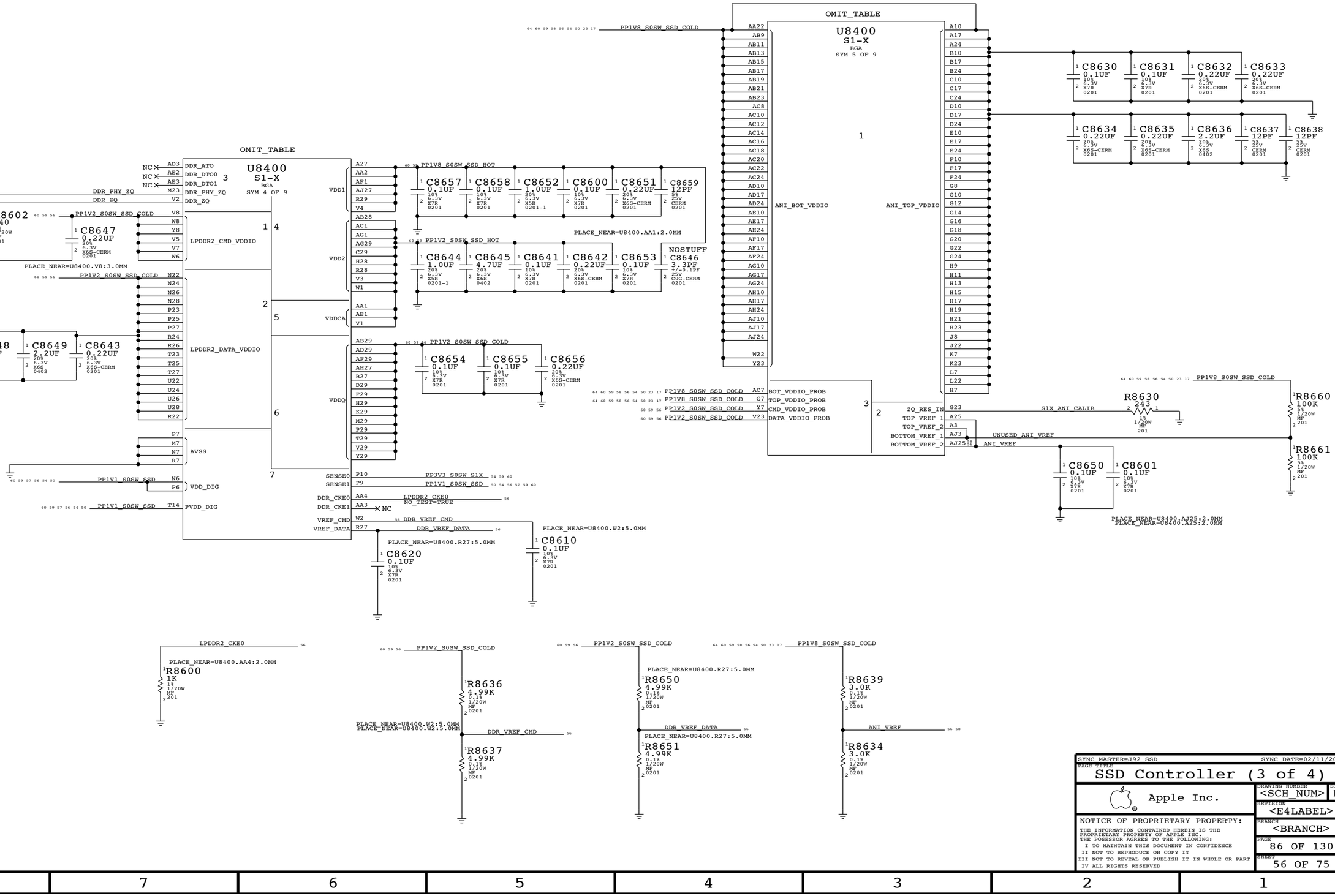

SYNC MASTER=J92 SSD | SYNC DATE=02/11/2014

PAGE TITLE: SSD Controller (3 of 4)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> | SIZE: D

REVISION: <E4LABEL>

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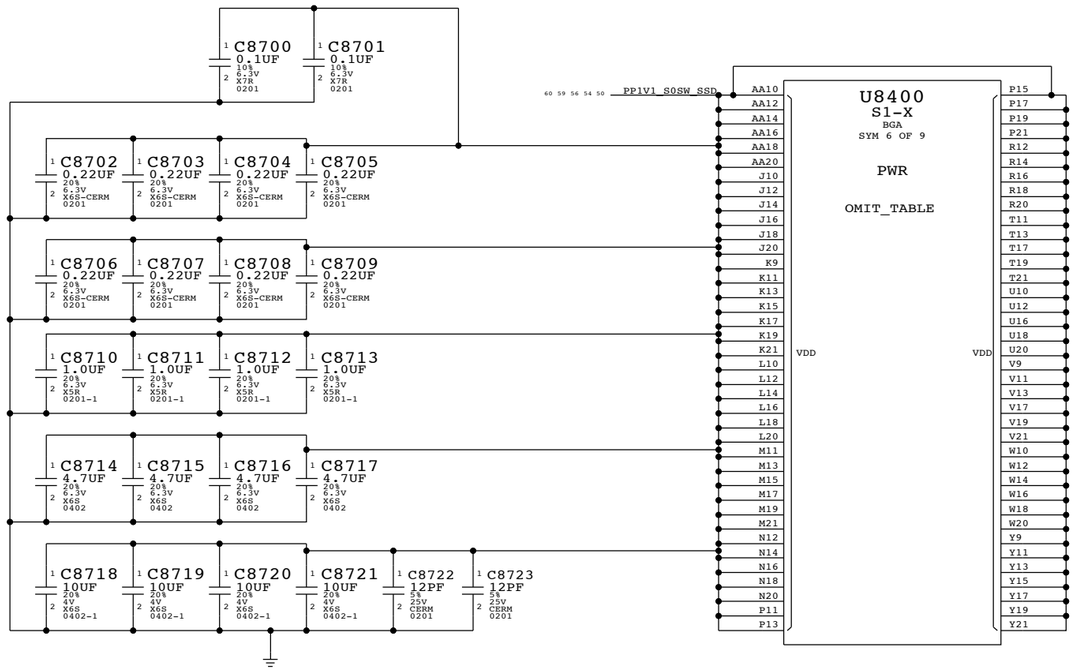

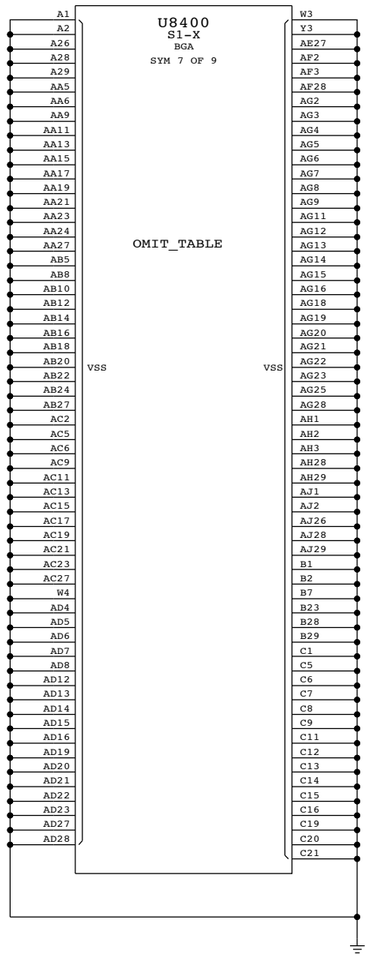

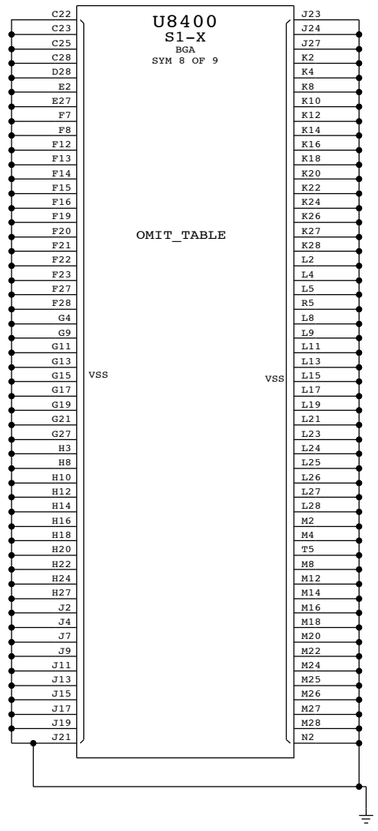

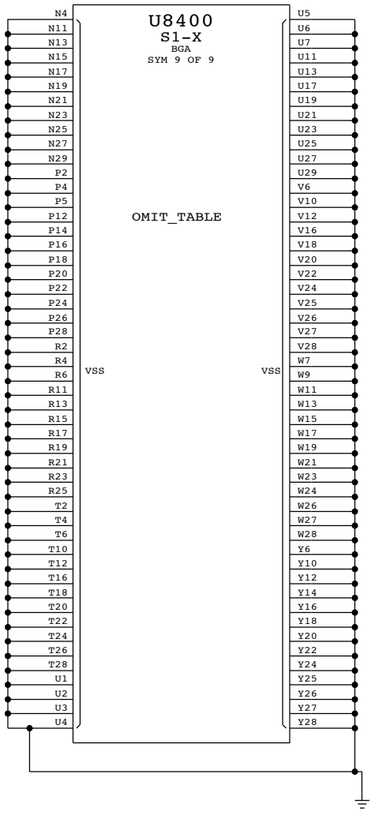

SYNC MASTER=J92 DEVMLB SYNC DATE=10/10/2013

PAGE TITLE
SSD Controller (4 of 4)

Apple Inc.

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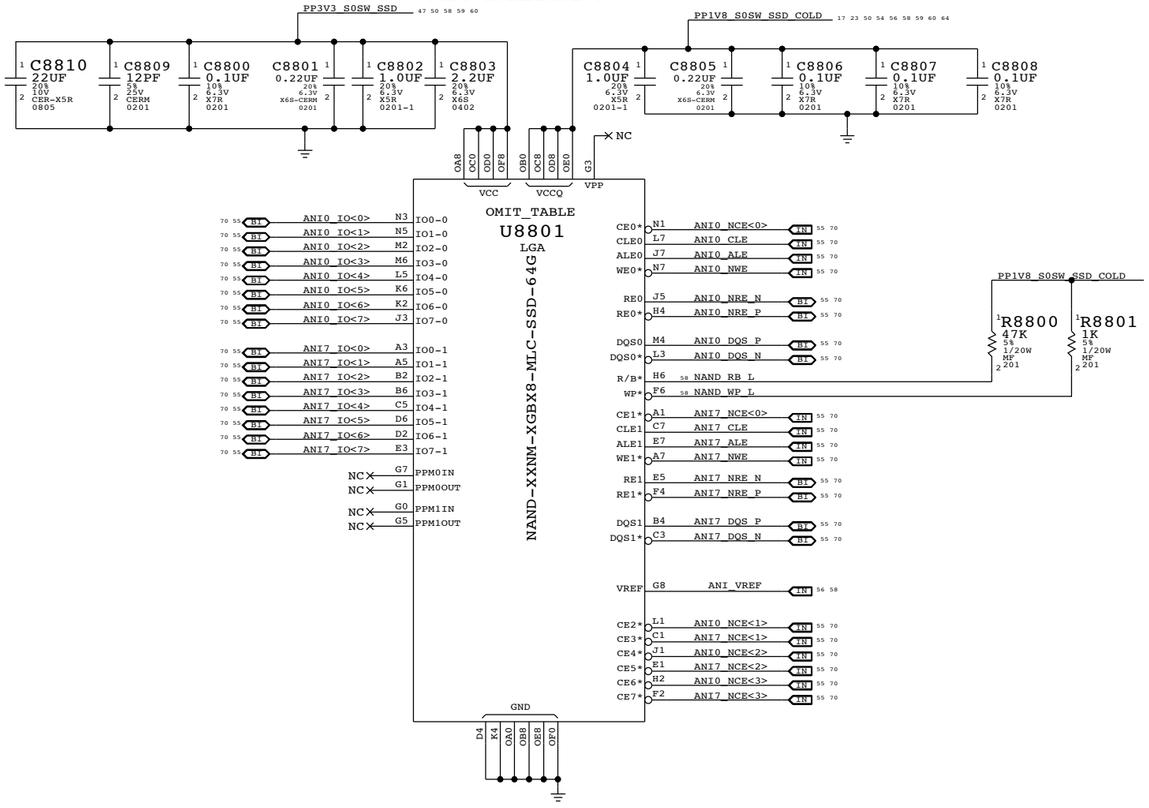
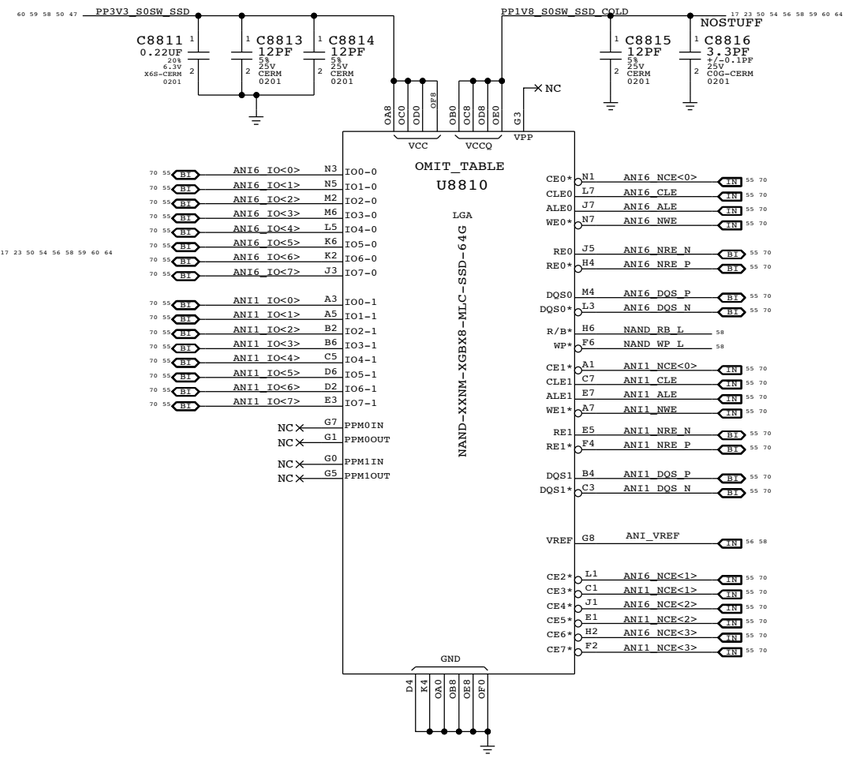
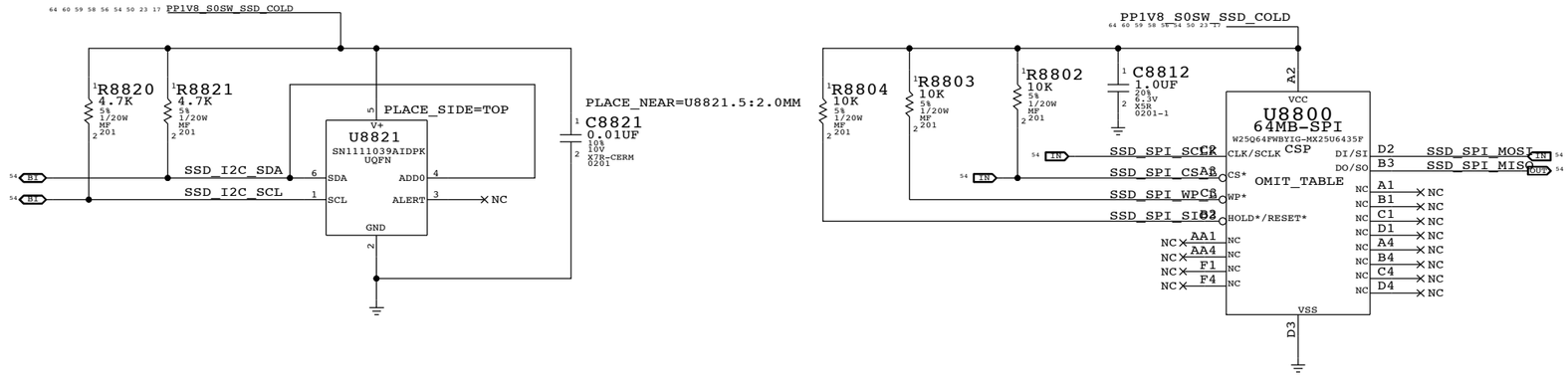
NAND INTERFACE 0/7



NAND INTERFACE 6/1





SYNC MASTER=J92 SSD | SYNC DATE=10/07/2013

PAGE TITLE: SSD NAND Flash & ROM

Apple Inc.

DRAWING NUMBER: <SCH_NUM> | SIZE: D

REVISION: <E4LABEL>

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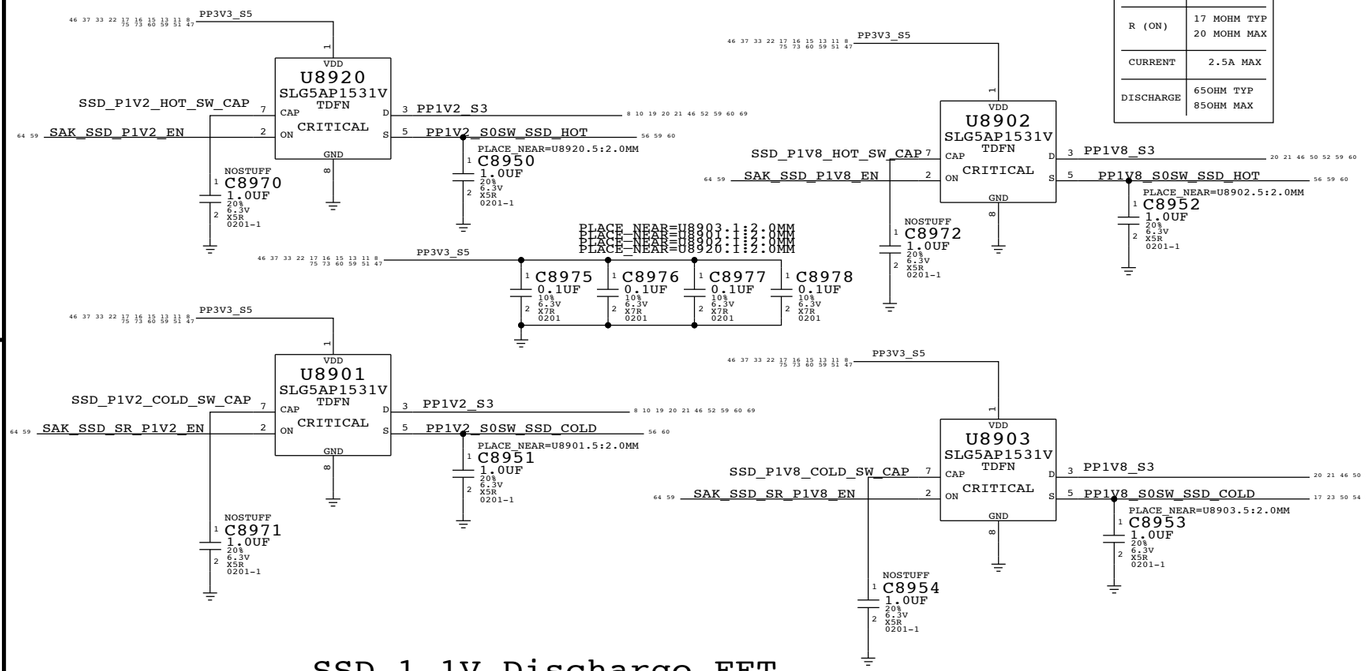
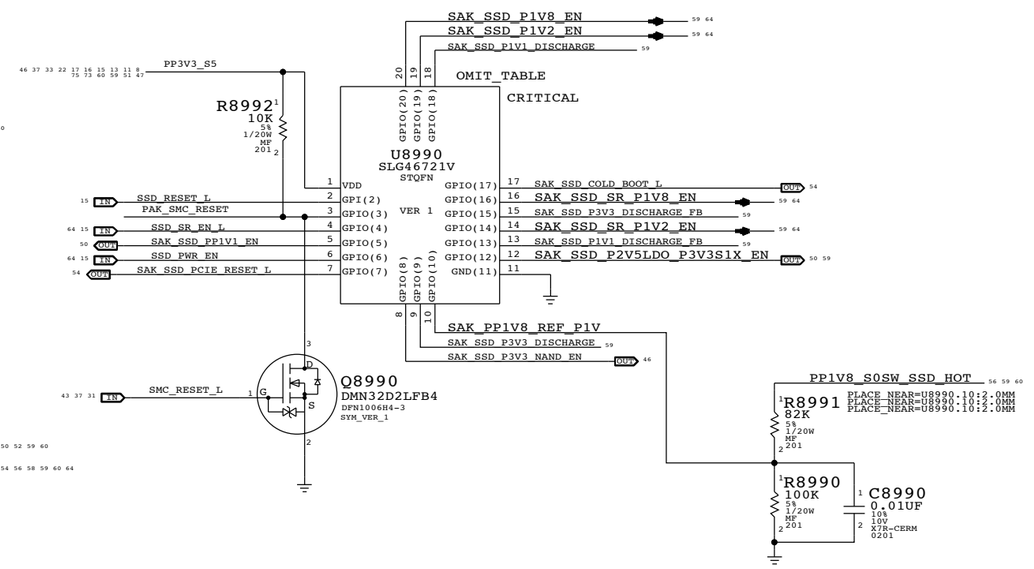
LPDDR2 1.2V & 1.8V LOAD SWITCHES FOR SEQUENCING, SR SUPPORT

PART	SLG5AP1531V
R (ON)	17 MOHM TYP 20 MOHM MAX
CURRENT	2.5A MAX
DISCHARGE	65OHM TYP 85OHM MAX

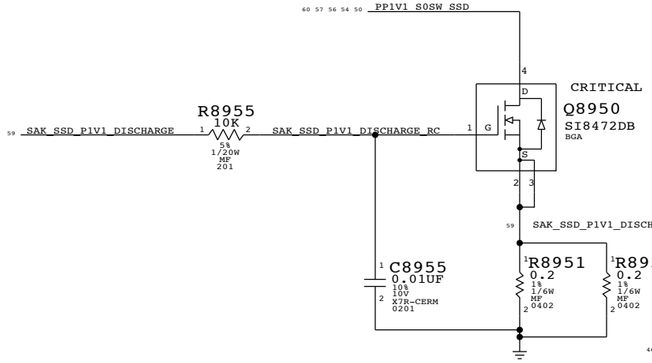


SILEGO GREEN PAK3 FOR POWER SEQUENCING, SR

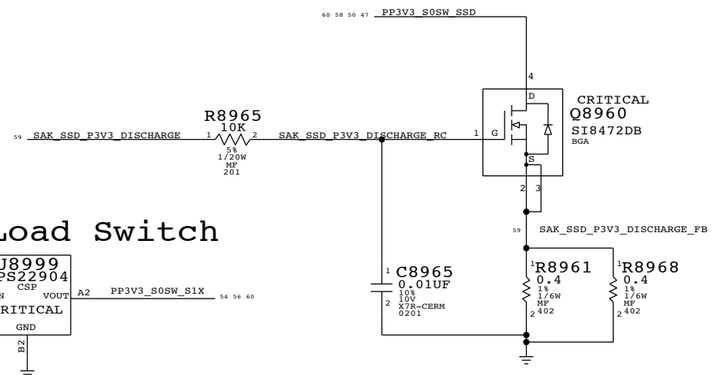


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00030	1	IC,SLG4AP4547V,PWR RAIL SEQUENCER,STQFN-20	U8990	CRITICAL	

SSD 1.1V Discharge FET

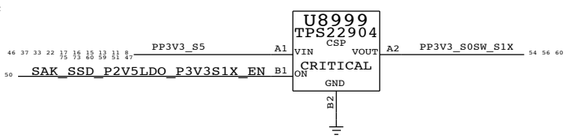


SSD 3.3V Discharge FET

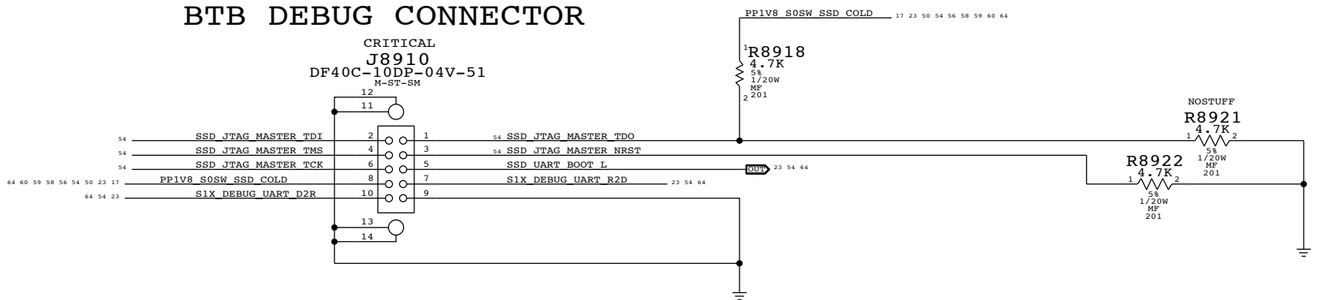


SSD 1.2V/1.8V HOT protection diode

S1X 3.3V Load Switch



BTB DEBUG CONNECTOR



SYNC MASTER=J92_DEVMLB SYNC DATE=02/12/2014

PAGE TITLE: SSD SR, Power, & Debug

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
PPVIN_G3H_P3V3G3H
PPBUS_S5_HS_COMPUTING_ISNS
PPVBUS_E85
PPDCIN_G3H
PP3V3_G3H
PP3V3R3V0_AON
PPVRTC_G3H

5V Rails

PP5V_G3H_LDO
PP5V_S0SW_LCD
PP5V_S4
PP5V_S0

3.3V Rails

PP3V3_S5
PP3V3_SUS
PP3V3_S4
PP3V3_S0

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S3 — 2A max supply
PP1V5_S0 — 2 mA
PP1V2_S3
PP1V05_SUS — ? mA
PP1V05_S4SW — 100 mA

SSD Rails

PP3V3_S0SW_SSD
PP3V3_S0SW_S1X
PP2V5_S0SW_SSD
PP1V8_S0SW_SSD_COLD
PP1V8_S0SW_SSD_HOT
PP1V2_S0SW_SSD_COLD
PP1V2_S0SW_SSD_HOT
PP1V1_S0SW_SSD

CPU "VCORE" RAILS

PPVCC_S0_CPU

USB-C PWR (5.1V)

PP5V1_S4SW
PP5V1_S4SW_CC1
PP5V1_S4SW_CC2
XWA001 SM E85_CC1
XWA002 SM E85_CC2
PP1V05_S0SW_PCH_PCIE
PP1V05_S0SW_PCH_SATA
PP1V05_S0SW_PCH_USB3

PPBVAT_G3H_CONN

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

SYNC_MASTER=J43_MLB
SYNC_DATE=10/24/2012
PAGE TITLE: Power Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
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Memory Bit/Byte Swizzle

LPDDR3 Command/Address

MAKE_BASE

IN	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	OUT	20 69
IN	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	OUT	20 69
IN	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	OUT	20 69
IN	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	OUT	20 69
IN	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	OUT	20 69
IN	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	OUT	20 69
IN	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	OUT	7 20 61 69
IN	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	OUT	20 69
IN	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	OUT	20 69
IN	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	OUT	20 69
IN	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	OUT	20 69
IN	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	OUT	20 69
IN	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	OUT	20 69
IN	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	OUT	20 69
IN	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	OUT	20 69
IN	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	OUT	20 69
IN	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	OUT	7 20 61 69
IN	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	OUT	20 69
IN	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	OUT	20 69
IN	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	OUT	20 69
IN	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	OUT	7 20 61 69
IN	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1		7 61
IN	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2		7 61
IN	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	OUT	21 64 69
IN	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>	OUT	21 69
IN	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>	OUT	21 64 69
IN	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>	OUT	21 64 69
IN	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>	OUT	21 69
IN	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>	OUT	21 69
IN	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	OUT	7 21 61 69
IN	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	OUT	21 69
IN	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>	OUT	21 69
IN	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>	OUT	21 69
IN	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	OUT	21 69
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IN	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	OUT	21 69
IN	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	OUT	21 69
IN	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>	OUT	21 69
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IN	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	OUT	7 21 61 69
IN	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	OUT	21 69
IN	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>	OUT	21 69
IN	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>	OUT	21 69
IN	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	OUT	7 21 61 69
IN	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3		7 61
IN	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4		7 61

MAKE_BASE

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B2	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	B1	7 20 61 69
B2	=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<7>	B1	7 69
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B2	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<0>	B1	7 69
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MAKE_BASE

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MAKE_BASE=TRUE

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE
Memory Signal Swaps

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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Pages	Net	MAKE_BASE	Alias	Pages
64 62 28 15	QR_SWITCH_EN	TRUE	QR_SWITCH_EN	15 28 62 64
62 44 8	CPU_VR_READY	TRUE	CPU_VR_READY	8 44 62
62 31 13	SMC_PCH_SUSWARN_L	TRUE	SMC_PCH_SUSWARN_L	13 31 62
62 31 13	SMC_PCH_SUSACK_L	TRUE	SMC_PCH_SUSACK_L	13 31 62
62 43 35 32 31	SMC_BC_ACOK	TRUE	SMC_BC_ACOK	31 32 35 43 62
62 5	TP_ULX_SPARE1	TRUE	TP_ULX_SPARE1	5 62
62 5	TP_ULX_SSP_SPARE	TRUE	TP_ULX_SSP_SPARE	5 62
68 62 12	TP_LPC_CLK24M_LPCPLUS_R	TRUE	TP_LPC_CLK24M_LPCPLUS_R	12 62 68
64 62 28 13	HPM_I2C_INT_L	TRUE	HPM_I2C_INT_L	13 28 62 64
64 62 28 13	HPM_I2C_INT_L			
63 62 28 16 14 64	XDP_USB_EXTA_OC_L	TRUE	XDP_USB_EXTA_OC_L	14 16 28 62 63 64
62 37 32 31 26	SMC_TCK	TRUE	SMC_TCK	26 31 32 37 62
62 37 32 31 26	SMC_TMS	TRUE	SMC_TMS	26 31 32 37 62
62 28	TP_HPM_XTALOUT	TRUE	TP_HPM_XTALOUT	28 62
	GND	TRUE	GND	
68 64 62 29 12	PCIE_CLK100M_TBT_P	TRUE	PCIE_CLK100M_TBT_P	12 29 62 64 68
68 64 62 29 12	PCIE_CLK100M_TBT_N	TRUE	PCIE_CLK100M_TBT_N	12 29 62 64 68
29	=PCIE_E85_D2R_P	TRUE	PCIE_TBT_D2R_P<0>	14 68
29	=PCIE_E85_D2R_N	TRUE	PCIE_TBT_D2R_N<0>	14 68
29	=PCIE_E85_R2D_P	TRUE	PCIE_TBT_R2D_C_P<0>	14 68
29	=PCIE_E85_R2D_N	TRUE	PCIE_TBT_R2D_C_N<0>	14 68
62 29 12	TBT_CLKREQ_L	TRUE	TBT_CLKREQ_L	12 29 62
62 29 15	PCH_TBT_PCIE_RESET_L	TRUE	PCH_TBT_PCIE_RESET_L	15 29 62
64 62 29 28	E85_TEST_MODE_L	TRUE	E85_TEST_MODE_L	28 29 62 64

64 62 50 29 28 27 IN E85HSMUX_USB_EN MAKE_BASE=TRUE — E85HSMUX_USB_EN OUT 27 28 29 50 62 64

SYNC_MASTER=J92_DEVMLB	SYNC_DATE=07/08/2014
PAGE TITLE	J92 Signal Aliases
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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NO_TEST Nets

		NO_TEST	MAKE_BASE			
63 12	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	12 63	CPU/PCH
63 12	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	12 63	
63	NC_PCIE_TBT_D2RP<1>	TRUE	TRUE	NC_PCIE_TBT_D2RP<1>	63	
63	NC_PCIE_TBT_D2RN<1>	TRUE	TRUE	NC_PCIE_TBT_D2RN<1>	63	
63	NC_PCIE_TBT_R2D_CP<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CP<1>	63	
63	NC_PCIE_TBT_R2D_CN<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CN<1>	63	
63 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 63	
63 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 63	
63 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 63	
63 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 63	
63 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 63	
63 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 63	
63 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 63	
63 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 63	
63 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 63	
	=DP_TBTSNK1_ML_C_P<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CP<3..0>	5	
	=DP_TBTSNK1_ML_C_N<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CN<3..0>	5	
63 13	NC_DP_TBTSNK1_DDC_CLK	TRUE	TRUE	NC_DP_TBTSNK1_DDC_CLK	13 63	
63 13	NC_DP_TBTSNK1_DDC_DATA	TRUE	TRUE	NC_DP_TBTSNK1_DDC_DATA	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CP	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CN	13 63	
63 13	NC_DP_TBTSNK1_HPD	TRUE	TRUE	NC_DP_TBTSNK1_HPD	13 63	
63 31	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	31 63	SMC
63	NC_SMC_DEBUGPRT_EN_L	TRUE	TRUE	NC_SMC_DEBUGPRT_EN_L	63	
63 31	NC_SMC_SYS_KBDLED	TRUE	TRUE	NC_SMC_SYS_KBDLED	31 63	
63	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	63	
63 31	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	31 63	
63 31	NC_SMC_FAN_0_TACH	TRUE	TRUE	NC_SMC_FAN_0_TACH	31 63	
63 31	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	31 63	
63 31	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	31 63	
64 63 31	NC_SYS_ONEWIRE	TRUE	TRUE	NC_SYS_ONEWIRE	31 63 64	

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
SD_PWR_EN	15
ENET_MEDIA_SENSE	15
BT_PWRRST_L	15
TPAD_USB_IF_EN	15
PCH_GPIO12	15
TBT_PWR_EN	15
TBT_CIO_PLUG_EVENT_L	15
JTAG_TBT_TMS_PCH	15
ODD_PWR_EN_L	13
HDMITBTMUX_FLAG	13
HDMITBTMUX_LATCH	13
CAM_SENSOR_WAKE_L	24
LCD_PSR_EN	15
XDP_USB_EXTA_OC_L	14 16 28 62 64
AUD_WAKE_L	15
MIKEY_SPI_CS_L	15
MIKEY_SPI_CLK	15
MIKEY_SPI_MISO	15
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EE Chaz Probe Points

PPA501	P3V3S3_EN	MAKE_BASE=TRUE	= P3V3S3_EN	46 64
PPA502	PMIC2_READY			46 48
PPA503	P1V05SUS_DRVH			48
PPA504	SMC_CBC_ON			31 43
PPA505	SMC_CHGR_INT_L			31 43
PPA506	MEM_B_CAA<0>			21 61 69
PPA507	MEM_B_CLK_P<0>			7 21 69
PPA508	MEM_B_CLK_N<0>			7 21 69
PPA509	MEM_B_CS_L<0>			7 21 69
PPA510	MEM_B_DQ<0>			7 61 69
PPA511	MEM_B_DQS_P<0>			7 61 69
PPA512	MEM_B_DQS_N<0>			7 61 69
PPA513	AP_PCIE_DEV_WAKE			13 22
PPA514	AP_S0IX_WAKE_L			15 22
PPA515	AP_S0IX_WAKE_SEL			15 22
PPA516	E85HSMUX_USB_EN			27 28 29 50 62

PPA519	PCH_BT_UART_D2R			15 23
PPA520	BT_UART_CTS_L			22 23
PPA521	PCH_UART1_R2D			15
PPA522	PCIE_CAMERA_D2R_P			14 25 68
PPA523	PCIE_CLK100M_SSD_P			12 54 64 66
PPA524	PCIE_CLK100M_TBT_P			12 29 62 68

64 48 46	AGND_PMIC	MAKE_BASE=TRUE	= AGND_PMIC	46 48 64
64 48 46	AGND_PMIC		=	
64 48 46	AGND_PMIC		=	
64 48 46	AGND_PMIC		=	
64 48 46	AGND_PMIC		=	
64 43 31 28	TS_HIPWR_EN	MAKE_BASE=TRUE	= TS_HIPWR_EN	28 31 43 64
64 43 28	TS_POWER_GATE_EN	MAKE_BASE=TRUE	= TS_POWER_GATE_EN	28 43
64 59 15	SSD_PWR_EN	MAKE_BASE=TRUE	= SSD_PWR_EN	15 59
64 59 54 23	SSD_UART_BOOT_L	MAKE_BASE=TRUE	= SSD_UART_BOOT_L	23 54 59 64
64 59 54 23	S1X_DEBUG_UART_D2R	MAKE_BASE=TRUE	= S1X_DEBUG_UART_D2R	23 54 59 64
64 59 54 23	S1X_DEBUG_UART_R2D	MAKE_BASE=TRUE	= S1X_DEBUG_UART_R2D	23 54 59 64
58 56 54 50 23 17	PP1V8_S0SW_SSD_COLD	MAKE_BASE=TRUE	= PP1V8_S0SW_SSD_COLD	64 58 56 54 50 23 17 64 60 59 59 54 50 23 60
66 64 54 12	PCIE_CLK100M_SSD_P	MAKE_BASE=TRUE	= PCIE_CLK100M_SSD_P	12 54 64 66
66 64 54 12	PCIE_CLK100M_SSD_N	MAKE_BASE=TRUE	= PCIE_CLK100M_SSD_N	12 54 64 66
54	=PCIE_SSD_D2R_P<0..3>	MAKE_BASE=TRUE	= PCIE_SSD_D2R_P<0..3>	14 64 66
54	=PCIE_SSD_D2R_N<0..3>	MAKE_BASE=TRUE	= PCIE_SSD_D2R_N<0..3>	14 64 66
54	=PCIE_SSD_R2D_P<0..3>	MAKE_BASE=TRUE	= PCIE_SSD_R2D_P<0..3>	23 66
54	=PCIE_SSD_R2D_N<0..3>	MAKE_BASE=TRUE	= PCIE_SSD_R2D_N<0..3>	23 66
64 46	P1V1_S0_DLPN_PGOOD	MAKE_BASE=TRUE	= P1V1_S0_DLPN_PGOOD	46 64
68 64 24 17	SYSCLK_CLK24M_CAMERA	MAKE_BASE=TRUE	= SYSCLK_CLK24M_CAMERA	17 24 64 68
64 46 17	SYSCLK_CLK32K_PMIC	MAKE_BASE=TRUE	= SYSCLK_CLK32K_PMIC	17 46 64
64 31	TP_SMC_PWRFAIL_WARN_L	MAKE_BASE=TRUE	= TP_SMC_PWRFAIL_WARN_L	31 64

PPA525	E85_RFU<1>	26 29
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PPA527	E85_CC1	29 60 68
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PPA531	CAMERA_PWR_EN	15 24
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PPA533	EDP_BKLT_PWM	13 53
PPA534	HDA_SDIN0	12 40 68
PPA535	I2C_PCH_1_SCL	15 28 34
PPA536	I2C_PCH_1_SDA	15 28 34
PPA537	LCD_IRQ_L	15 53
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PPA549	PCIE_CLK100M_SSD_N	12 54 64 66
PPA550	PCIE_CLK100M_TBT_N	12 29 62 68
PPA551	PCIE_SSD_D2R_N<0>	14 64 66
PPA552	PCIE_SSD_D2R_P<0>	14 64 66

PPA555	OR_SWITCH_EN	15 28 62
PPA556	SAK_SSD_P1V2_EN	59
PPA557	SAK_SSD_P1V8_EN	59
PPA558	SAK_SSD_SR_P1V2_EN	59
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PPA560	SMC_BT_PWR_EN	22 31
PPA561	SMC_CLK32K_PMIC	31 32
PPA562	SMC_OOB1_R2D_L	31 54
PPA563	SMC_PROCHOT	31 32
PPA564	SMC_SENSOR_PWR_EN	31 33 35
PPA565	SMC_WAKE_SCI_L	15 31
PPA566	SMC_WIFI_PWR_EN	22 31
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PPA569	SSD_SR_EN_L	15 59
PPA570	SYSCLK_CLK12M_SMC	17 31
PPA571	SYSCLK_CLK12M_SSD	17 54
PPA572	SYSCLK_CLK24M_CAMERA	17 24 64 68
PPA573	SYSCLK_CLK32K_PMIC	17 46 64
PPA574	BT_DEV_WAKE	22
PPA575	TPAD_SPI_CS_L	15 30
PPA576	TPAD_SPI_INT_L	15 30

PPA577	USB3_EXTA_D2R_N	14 29 67
PPA578	USB3_EXTA_D2R_P	14 29 67
PPA579	CPU_CATERR_L	6 31 66
PPA580	E85_TEST_MODE_L	28 29 62
PPA581	MEM_B_CS_L<1>	7 21 69
PPA582	MEM_B_CKE<1>	7 21 69
PPA583	MEM_B_CAB<1>	21 61 69
PPA584	MEM_B_CAA<2>	21 61 69
PPA585	MCP_RSVD_CK13 MAKE_BASE=TRUE	= MCP_RSVD_CK13 6 64
PPA586	MCP_DC_CV45 MAKE_BASE=TRUE	= MCP_DC_CV45 8 64
PPA587	MEM_B_CAA<3>	21 61 69
PPA588	E85_LS_P<1>	26 29 68
PPA589	E85_LS_N<1>	26 29 68
PPA590	E85_LS_P<2>	26 29 68
PPA591	E85_LS_N<2>	26 29 68
PPA592	XDP_PCH_UART_SSD_L_BT_H	12 16
PPA593	DP_E85SNK_HPD	18 28 33
PPA594	XDP_USB_EXTA_OC_L	14 16 28 62 63
PPA595	XDP_USB_EXTB_OC_L	14 16 64
PPA596	USB_EXTA_P	14 26 67
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PPA5A3	BBPD_PD_SEL_CC2	28 29
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PPA5A5	BBPD_RX_L_TX_H	28 29
PPA5A6	BBPD_SPI_MOSI	28 29
PPA5A7	BBPD_VCONN1_EN	29 50
PPA5A8	BBPD_VCONN2_EN	29 50
PPA5A9	BBPD_VCONN_EN	28 29

64 7	TP_ULX_DDR_VCCDDQG	TRUE	TP_ULX_DDR_VCCDDQG	7 64
67 64 32 31 26	SMC_DEBUGPRT_TX_L	TRUE	SMC_DEBUGPRT_TX_L	26 31 32 64 67
67 64 32 31 26	SMC_DEBUGPRT_RX_L	TRUE	SMC_DEBUGPRT_RX_L	26 31 32 64 67

NO_TEST Nets

	NO_TEST	MAKE_BASE			
67 64 14	NC_USB3_EXTB_D2RP	TRUE	TRUE	NC_USB3_EXTB_D2RP	67 14 64
67 64 14	NC_USB3_EXTB_D2RN	TRUE	TRUE	NC_USB3_EXTB_D2RN	67 14 64
67 64 14	NC_USB3_EXTB_R2D_CP	TRUE	TRUE	NC_USB3_EXTB_R2D_CP	14 64 67
67 64 14	NC_USB3_EXTB_R2D_CN	TRUE	TRUE	NC_USB3_EXTB_R2D_CN	14 64 67
	NO_TEST	MAKE_BASE			
64 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 64
64 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	67 14 64
67 64 14	NC_USB_EXTBP	TRUE	TRUE	NC_USB_EXTBP	14 64 67
67 64 14	NC_USB_EXTBN	TRUE	TRUE	NC_USB_EXTBN	67 14 64
	NO_TEST	MAKE_BASE			
67 64 14	NC_USB_TPADP	TRUE	TRUE	NC_USB_TPADP	67 14 64
67 64 14	NC_USB_TPADN	TRUE	TRUE	NC_USB_TPADN	14 64 67
64 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 64
64 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 64

CPU/PCH

64 63 31	NC_SYS_ONEWIRE	TRUE	TRUE	NC_SYS_ONEWIRE 31 63 64
64 46	NC_PMIC_CLK32K_XTALIN	TRUE	TRUE	NC_PMIC_CLK32K_XTALIN 46 64
64 31	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP 31 64
64 31	NC_SMC_FAN_0_CTL	TRUE	TRUE	NC_SMC_FAN_0_CTL 31 64
64 31	NC_SMC_FAN_4_CTL	TRUE	TRUE	NC_SMC_FAN_4_CTL 31 64

Unused nets with offpage

(Nets with offpages not used on this project)

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J92 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL6,ISL8,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL4	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	Y	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.260 MM			
27P4_OHM_SE	ISL6,ISL8,ISL10	Y	0.134 MM	0.134 MM			
27P4_OHM_SE	ISL3,ISL4	Y	0.190 MM	0.190 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.144 MM	0.144 MM			
40_OHM_SE	ISL6	Y	0.070 MM	0.070 MM			
40_OHM_SE	ISL8	Y	0.073 MM	0.073 MM			
40_OHM_SE	ISL10	Y	0.071 MM	0.071 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.095 MM			
45_OHM_SE	ISL6	Y	0.057 MM	0.057 MM			
45_OHM_SE	ISL8	Y	0.058 MM	0.058 MM			
45_OHM_SE	ISL10	Y	0.057 MM	0.057 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
50_OHM_SE_RF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.147 MM	0.060 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL6	Y	0.082 MM	0.082 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL8	Y	0.085 MM	0.085 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL10	Y	0.081 MM	0.081 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
85_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL10	Y	0.057 MM	0.057 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Note: 80ohm copied from 85ohm (pending stack-up calcs)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
80_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL10	Y	0.056 MM	0.056 MM	=STANDARD	0.101 MM	0.101 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.057 MM	?
1x_DIELECTRIC	ISL2,ISL11	0.057 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.057 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.054 MM	?
1x_DIELECTRIC	ISL5,ISL8	0.058 MM	?
1x_DIELECTRIC	ISL6,ISL7	0.051 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

Note: DisplayPort tables are on Page 113

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 32
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_TTP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	6 16
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	6 16
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
CPU_CFG	CPU_45S	CPU_TTP	CPU_CFG<2..0>	6 16
CPU_CFG3	CPU_45S	CPU_TTP	CPU_CFG<3>	6 16
CPU_CFG	CPU_45S	CPU_TTP	CPU_CFG<19..4>	6 16
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 31 64
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 31 32 44
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	15 31 32
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI	6 16
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	6 16
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS	6 16
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	6 16
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPUPCH_TRST_L	6 12 16
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_TTP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 44
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 44
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 44
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 44
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 44
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	14 23
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	14 23
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	23 64
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	23 64
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	54
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	54
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	14 64
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	14 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 54 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 54 64

PCIe SSD

I120 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_P	26 29
I120 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_N	26 29
I120	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 29
I120	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 29
I120 DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	
I120 DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	
I120	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	
I120	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	
I120 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	
I119 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	
I119	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	
I119	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	53
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	53
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 53
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 53
I121 DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	
I121 DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 53
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 53
	DP_80D	DP_AUX	DP_INT_AUX_P	53
	DP_80D	DP_AUX	DP_INT_AUX_N	53

DP

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE: CPU Constraints

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

E85 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
E85_HS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
E85_LS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	*	=6x_DIELECTRIC	?
E85_LS	*	=4x_DIELECTRIC	?
E85_CC	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	TOP,BOTTOM	=10x_DIELECTRIC	?
E85_LS	TOP,BOTTOM	=6x_DIELECTRIC	?
E85_CC	TOP,BOTTOM	=6x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_45S	SPI	TPAD_SPI_MOSI	15 30
	SPI_45S	SPI	TPAD_SPI_MISO	15 30
	SPI_45S	SPI	TPAD_SPI_CLK	15 30
USB_BT	USB_80D	USB	USB_BT_P	14 22
USB_BT	USB_80D	USB	USB_BT_N	14 22
	USB_80D	USB	USB_BT_R_P	22
	USB_80D	USB	USB_BT_R_N	22
USB_BT	USB_80D	USB	USB_BT_CONN_P	
USB_BT	USB_80D	USB	USB_BT_CONN_N	
USB_TPAD	USB_80D	USB	NC_USB_TPADP	14 64
USB_TPAD	USB_80D	USB	NC_USB_TPADN	14 64
USB_HPM	USB_85D	USB	USB_HPM_P	28 29
USB_HPM	USB_85D	USB	USB_HPM_N	28 29
	USB_85D	USB	USB_HPM_R_P	26
	USB_85D	USB	USB_HPM_R_N	26
	USB_80D	USB	USB_EXTA_P	14 26 64
	USB_80D	USB	USB_EXTA_N	14 26 64
	USB_85D	USB	USB_EXTA_F_P	26
	USB_85D	USB	USB_EXTA_F_N	26
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 29 64
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 29 64
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_N	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	29
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	29
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 29
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 29
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_P	14 27
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_N	14 27
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_P	27 29
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_N	27 29
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_P	14 29
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_N	14 29
	UART_45S	UART	SMC_DEBUGPRT_TX_L	26 31 32 64
	UART_45S	UART	SMC_DEBUGPRT_RX_L	26 31 32 64
USB_EXTB	USB_80D	USB	NC_USB_EXTBP	14 64
USB_EXTB	USB_80D	USB	NC_USB_EXTBN	14 64
USB_EXTB	USB_80D	USB	USB2_EXTB_F_P	
USB_EXTB	USB_80D	USB	USB2_EXTB_F_N	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RP	14 64
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RN	14 64
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CP	14 64
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CN	14 64
USB_EXTC	USB_80D	USB	USB2_EXTC_P	
USB_EXTC	USB_80D	USB	USB2_EXTC_N	
USB_EXTC	USB_80D	USB	USB2_EXTC_F_P	
USB_EXTC	USB_80D	USB	USB2_EXTC_F_N	
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_P	
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_N	
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_P	
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_N	
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_P	
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_N	
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_P	
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_N	
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_P	
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_N	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

TP SPI

Internal USB

I/O Port Device USB

I/O Port Host USB

I/O Port DCI

USB EXTB nets (Left USB port)

USB EXTC nets (Left USB port)

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE: PCH Constraints 1

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DRAWING NUMBER: <SCH_NUM> SIZE: D

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 31
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 31
	LPC_45S	LPC	LPCPLUS_RESET_L	
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 31
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	
	CLK_LPC_45S	CLK_LPC	TP_LPC_CLK24M_LPCPLUS_R	12 62
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 34
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 34
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 34
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 34
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 31 34 36 53 72
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 31 34 36 53 72
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 40
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 40
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 40
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 40 64
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 40
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 32
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 37
	SPI_45S	SPI	SPI_CLK	37
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 37
	SPI_45S	SPI	SPI_MOSI	37
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 37
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 37
	SPI_45S	SPI	SPI_CS0_L	37
	SPI_45S	SPI	SPI_SMC_CLK	31 37
	SPI_45S	SPI	SPI_SMC_MOSI	31 37
	SPI_45S	SPI	SPI_SMC_MISO	31 37
	SPI_45S	SPI	SPI_SMC_CS_L	31 37
	SPI_45S	SPI	SPI_MLB_CLK	37
	SPI_45S	SPI	SPI_MLB_MOSI	37
	SPI_45S	SPI	SPI_MLB_MISO	37
	SPI_45S	SPI	SPI_MLB_CS_L	37
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	22
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	22
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 22
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 22
H402	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_P	22
H403	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_N	22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 22
H399	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_P	22
H400	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_N	22
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 62
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 62
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 29 62 64
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 29 62 64
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	24 25
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	24 25
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 25
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 25 64
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 25 64
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	24 25
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	24 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	24 25
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	24 25
PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_P	
PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_N	
H383 DP_TBT_ML	DP_80D	DP_TX	DP_ML_P<3..0>	
H384 DP_TBT_ML	DP_80D	DP_TX	DP_ML_N<3..0>	
H386 DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_P<3..0>	
H387 DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_N<3..0>	
H391 DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_P<3..0>	
H392 DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_N<3..0>	
H393 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_P	
H394 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_N	
H395 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_P	
H396 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_N	
H397 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_P	
H398 DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_N	

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK24M_CAMERA	17 24 64
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	24
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

E85 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<0>	5 29
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<0>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<1>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<1>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<3..2>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<3..2>	5 29
	DP_85D	DP_TX	DP_E85SNK_ML_P<3..0>	27 29
	DP_85D	DP_TX	DP_E85SNK_ML_N<3..0>	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_N	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_N	27 29
E85_LS	E85_LS_85D	E85_LS	E85_LS_P<2..1>	26 29 64
E85_LS	E85_LS_85D	E85_LS	E85_LS_N<2..1>	26 29 64
	E85_LS_85D	E85_LS	E85_LS_MISSION_P	26
	E85_LS_85D	E85_LS	E85_LS_MISSION_N	26
		E85_CC	E85_CC1	29 60 64
		E85_CC	E85_CC2	29 60 64

Note: 80ohm constraints are actually 85ohm

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_70D
MEM_40S	MEM_TERM	MEM_50S

Note: changed MEM_TERM physical rule to MEM_70D from MEM_73D temporarily

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CS0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>
MEM_A_CS1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>
MEM_A_ODT	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>
MEM_B_CS0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>
MEM_B_CS1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>
MEM_B_ODT	MEM_40S	MEM_CTRL	MEM_B_ODT<0>
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>
MEM_B_DQS7	MEM_70D		MEM_B_DQS_N<7>
		MEM_PWR	PP1V2_S3
		MEM_PWR	PPVREF_S3_MEM_VREFCA
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A
		MEM_PWR	PPVREF_S3_MEM_VREFCA
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_B

SYNC MASTER=J92 LS MLB SYNC DATE=05/07/2013

PAGE TITLE: Memory Constraints

Apple Inc.

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NAND BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
NAND_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
NAND_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NAND_DQS	*	0.100 MM	?
NAND_IO	*	0.100 MM	?
NAND_CMD	*	0.100 MM	?

NAND:

DQS_P/N MAX LENGTH 3"
IO<7..0> SIGNALS SHOULD MATCH +/- 50MIL FROM DQS_P/N
IO<7..0> AND ASSOCIATED DQS_P/N ROUTE ON SAME LAYER. NO MORE THAN 2 VIA TRANSITIONS.
NCE<7..0>,ALE,CLE SHOULD MATCH +/- 250MIL FROM NWE
DQS_P/N & NRE_P/N SHOULD MATCH +/- 100MIL FROM NWE

NAND NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ANI0_IO	NAND_45S	NAND_IO	ANI0_IO<7..0>
DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0_DQS_P
DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0_DQS_N
DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0_NRE_P
DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0_NRE_N
ANI0_NWE	NAND_45S	NAND_CMD	ANI0_NWE
ANI0_NCE	NAND_45S	NAND_CMD	ANI0_NCE<3..0>
ANI0_ALE	NAND_45S	NAND_CMD	ANI0_ALE
ANI0_CLE	NAND_45S	NAND_CMD	ANI0_CLE
ANI1_IO	NAND_45S	NAND_IO	ANI1_IO<7..0>
DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1_DQS_P
DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1_DQS_N
DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1_NRE_P
DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1_NRE_N
ANI1_NWE	NAND_45S	NAND_CMD	ANI1_NWE
ANI1_NCE	NAND_45S	NAND_CMD	ANI1_NCE<3..0>
ANI1_ALE	NAND_45S	NAND_CMD	ANI1_ALE
ANI1_CLE	NAND_45S	NAND_CMD	ANI1_CLE
ANI2_IO	NAND_45S	NAND_IO	ANI2_IO<7..0>
DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2_DQS_P
DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2_DQS_N
DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2_NRE_P
DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2_NRE_N
ANI2_NWE	NAND_45S	NAND_CMD	ANI2_NWE
ANI2_NCE	NAND_45S	NAND_CMD	ANI2_NCE<3..0>
ANI2_ALE	NAND_45S	NAND_CMD	ANI2_ALE
ANI2_CLE	NAND_45S	NAND_CMD	ANI2_CLE
ANI3_IO	NAND_45S	NAND_IO	ANI3_IO<7..0>
DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3_DQS_P
DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3_DQS_N
DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3_NRE_P
DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3_NRE_N
ANI3_NWE	NAND_45S	NAND_CMD	ANI3_NWE
ANI3_NCE	NAND_45S	NAND_CMD	ANI3_NCE<3..0>
ANI3_ALE	NAND_45S	NAND_CMD	ANI3_ALE
ANI3_CLE	NAND_45S	NAND_CMD	ANI3_CLE

NAND NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ANI4_IO	NAND_45S	NAND_IO	ANI4_IO<7..0>
DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4_DQS_P
DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4_DQS_N
DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4_NRE_P
DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4_NRE_N
ANI4_NWE	NAND_45S	NAND_CMD	ANI4_NWE
ANI4_NCE	NAND_45S	NAND_CMD	ANI4_NCE<3..0>
ANI4_ALE	NAND_45S	NAND_CMD	ANI4_ALE
ANI4_CLE	NAND_45S	NAND_CMD	ANI4_CLE
ANI5_IO	NAND_45S	NAND_IO	ANI5_IO<7..0>
DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5_DQS_P
DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5_DQS_N
DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5_NRE_P
DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5_NRE_N
ANI5_NWE	NAND_45S	NAND_CMD	ANI5_NWE
ANI5_NCE	NAND_45S	NAND_CMD	ANI5_NCE<3..0>
ANI5_ALE	NAND_45S	NAND_CMD	ANI5_ALE
ANI5_CLE	NAND_45S	NAND_CMD	ANI5_CLE
ANI6_IO	NAND_45S	NAND_IO	ANI6_IO<7..0>
DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6_DQS_P
DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6_DQS_N
DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6_NRE_P
DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6_NRE_N
ANI6_NWE	NAND_45S	NAND_CMD	ANI6_NWE
ANI6_NCE	NAND_45S	NAND_CMD	ANI6_NCE<3..0>
ANI6_ALE	NAND_45S	NAND_CMD	ANI6_ALE
ANI6_CLE	NAND_45S	NAND_CMD	ANI6_CLE
ANI7_IO	NAND_45S	NAND_IO	ANI7_IO<7..0>
DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7_DQS_P
DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7_DQS_N
DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7_NRE_P
DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7_NRE_N
ANI7_NWE	NAND_45S	NAND_CMD	ANI7_NWE
ANI7_NCE	NAND_45S	NAND_CMD	ANI7_NCE<3..0>
ANI7_ALE	NAND_45S	NAND_CMD	ANI7_ALE
ANI7_CLE	NAND_45S	NAND_CMD	ANI7_CLE

SYNC MASTER=MASTER SYNC DATE=11/16/2011

PAGE TITLE: NAND CONSTRAINTS

Apple Inc.

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 24 25
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 24 25
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 24 25
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 24 25 64
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 25
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 24 25
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 24 25
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 24 25
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 24 25
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 24 25
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 24 25
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 24 25
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 24 25
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 24 25
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 24 25
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 24 25
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 24 25
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 24 25 64
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 24 25
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 24 25
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 24 25
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 24 25
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 25 53
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 25 53
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 24 25
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 24 25
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 25 53
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 25 53
		S2_MEM_PWR	PP1V35_CAM 24 25
		S2_MEM_PWR	PP0V675_CAM_VREF 24 25
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 25

SYNC_MASTER=J92_DEVMLB SYNC_DATE=08/01/2013

PAGE TITLE: Camera Constraints

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	0.1 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL 31 34 53
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA 31 34 53
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 14 31 34 36 53 68
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 14 31 34 36 53 68
SMBUS_SMC_2_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL 31 34 46 48
SMBUS_SMC_2_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA 31 34 46 48
SMBUS_SMC_2_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL_R
SMBUS_SMC_2_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA_R
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL 30 31 34 40
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA 30 31 34 40
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL 31 34 41 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA 31 34 41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_P 43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_N 43
	1TO1_DIFFPAIR		CHGR_CSI_R_P 43
	1TO1_DIFFPAIR		CHGR_CSI_R_N 43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_P 43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_N 43
	1TO1_DIFFPAIR		CHGR_CSO_R_P 43
	1TO1_DIFFPAIR		CHGR_CSO_R_N 43

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P3MM	*	=1TO1_DIFFPAIR	0.300 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.400 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

RF Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
RF_50S	*	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
RF	*	0.15 MM	?

J92 MLB Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
		NET_TYPE	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P 35 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N 35 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N 35
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P 35
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P 36
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N 36
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_P 46
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_N 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P 49
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N 49
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_P 48
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_N 48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_P 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_N 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N 36
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_P 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_N 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_P 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_N 39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_P 38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_N 38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_P 38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_N 38 40
		SB_POWER	PP3V3_S5 8 11 13 15 16 17 22 33 37 46 47 51 59 60 75
		SB_POWER	PP3V3_S0 8 11 12 13 15 17 18 23 24 29 32 33 34 35 36 40 46 47 53 60 75
		GND	GND
	RF_50S	RF	RF_A_0_DIPLEXER 22
	RF_50S	RF	RF_A_0_MATCH 22
	RF_50S	RF	RF_G_0_DIPLEXER 22
	RF_50S	RF	RF_G_0_MATCH 22
	RF_50S	RF	RF_0_ANT 22
	RF_50S	RF	RF_0_ANT_MATCH_T 22
	RF_50S	RF	RF_A_1_DIPLEXER 22
	RF_50S	RF	RF_A_1_MATCH 22
	RF_50S	RF	RF_G_1_DIPLEXER 22
	RF_50S	RF	RF_G_1_MATCH 22
	RF_50S	RF	RF_1_ANT 22
	RF_50S	RF	RF_1_ANT_MATCH_T 22
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_P<1..0>
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_N<1..0>
	DP_80D	DP_TX	DP_EXT_ML_C_P<1..0>
	DP_80D	DP_TX	DP_EXT_ML_C_N<1..0>
USB_EXTA	USB_80D	USB	DPRUSB_EXTA_P
USB_EXTA	USB_80D	USB	DPRUSB_EXTA_N
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	DPRUSB3_EXTA_D2R_P
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	DPRUSB3_EXTA_D2R_N
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	DPRUSB3_EXTA_R2D_P
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	DPRUSB3_EXTA_R2D_N

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<radar://component/XXXXXX> J92 HW EE SCHEMATIC | PROTO 0

Kismet:
<afp://kismet.apple.com/Kismet-Projects/J92/>

Useful Wiki Links:
Schematic Conventions - <https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions>
Schematic Design Wiki - <https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design>

MobileMac HW Radar:
<radar://component/497591> MobileMac HW | Task
<radar://component/497587> MobileMac HW | Schematic
<radar://component/497585> MobileMac HW | New Bugs
<radar://component/497588> MobileMac HW | Layout
<radar://component/497590> MobileMac HW | Investigation
<radar://component/497589> MobileMac HW | Architecture

Other Info:
Page Allocations - <radar:11791318> 2012 Schematic Page Allocations

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Reference

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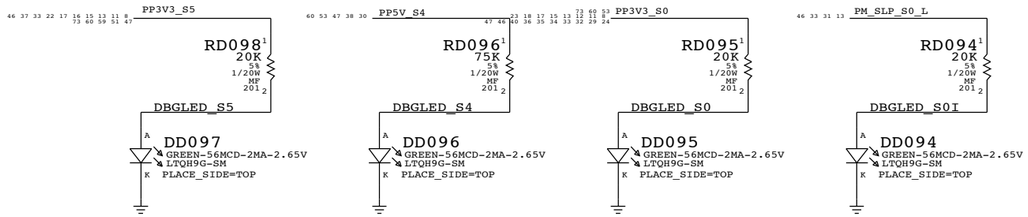
Power State Debug LEDs



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