

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

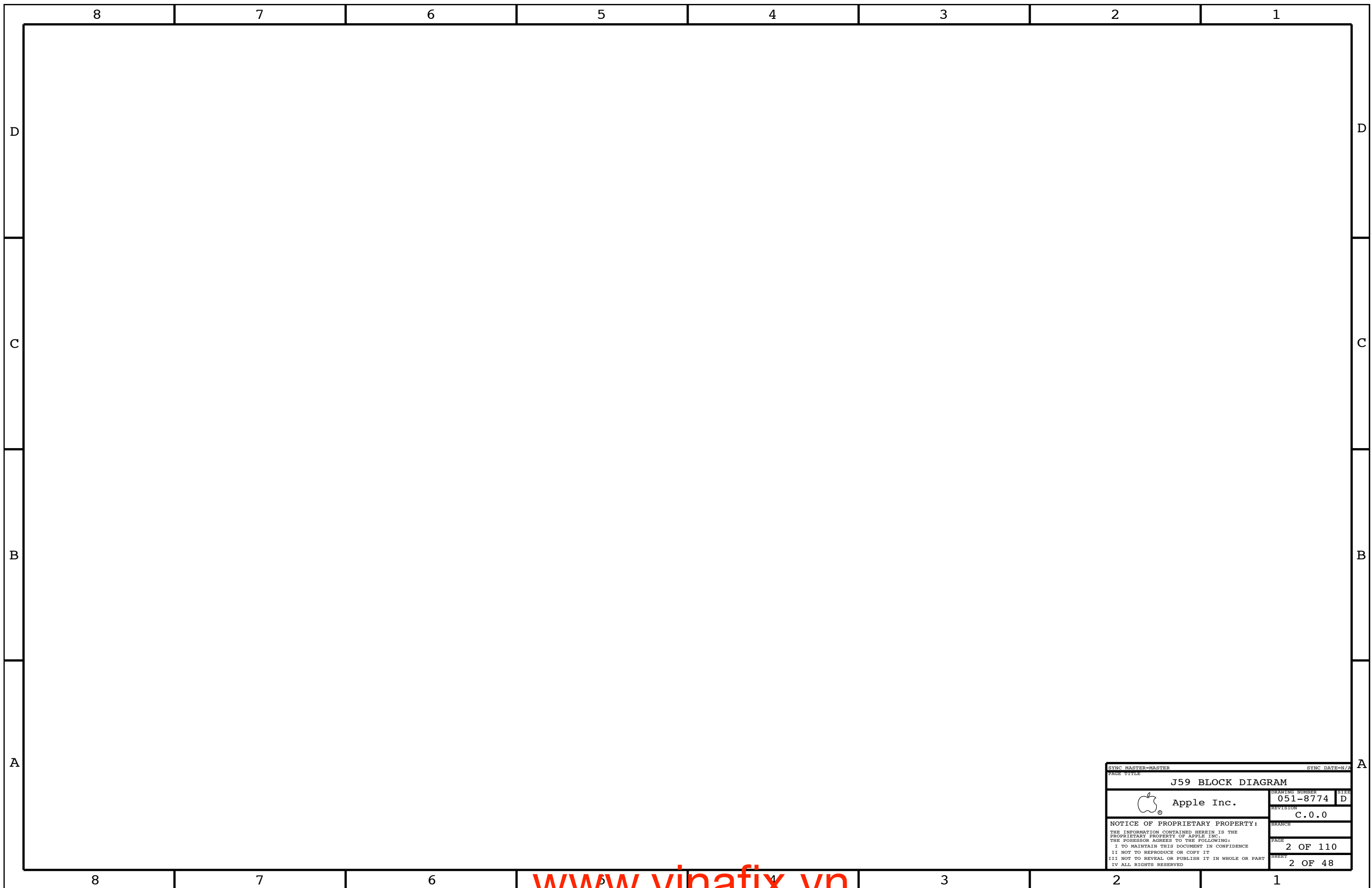
REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
C	0001188998	PRODUCTION RELEASED	2011-07-22


J59

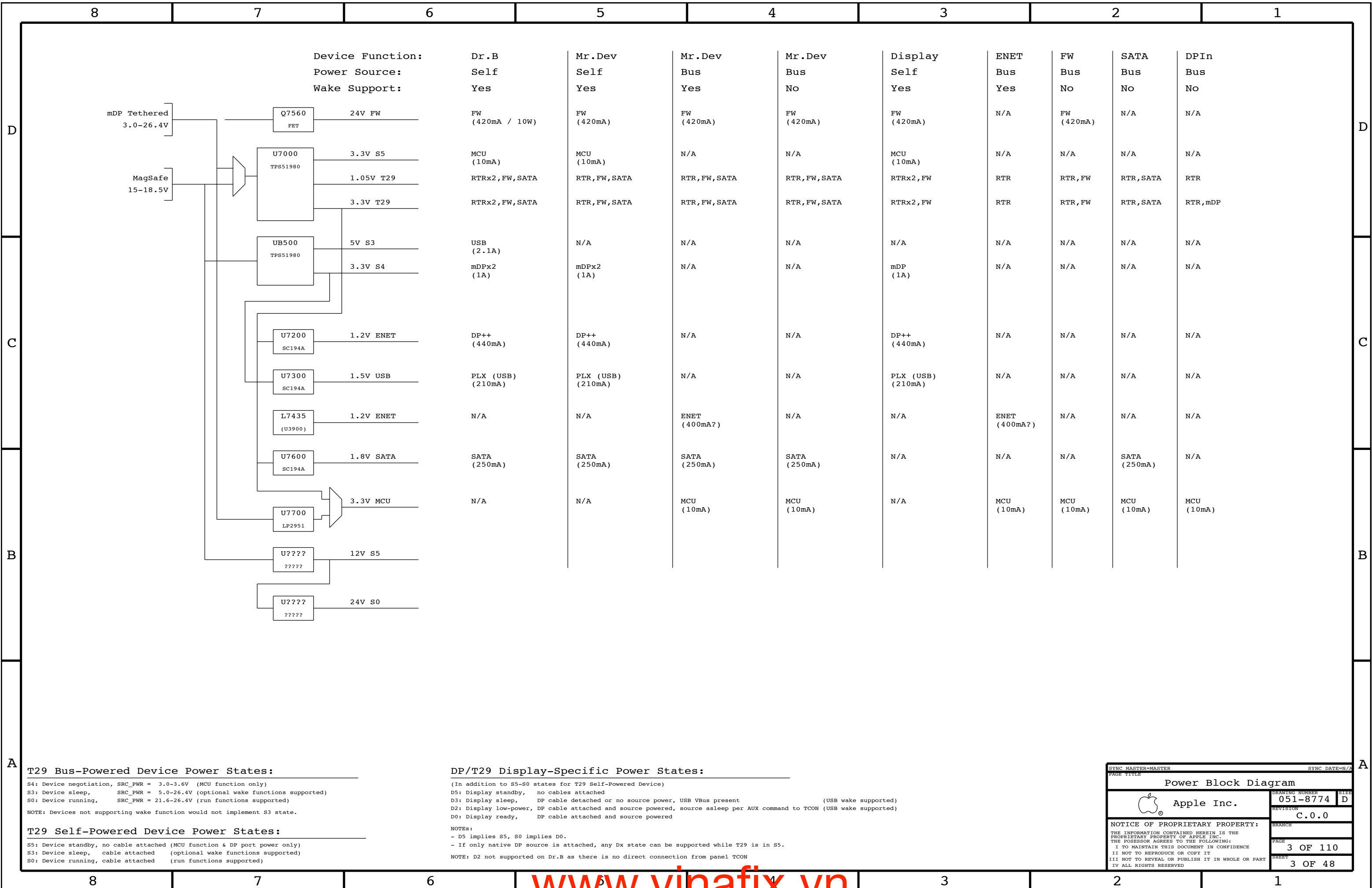
(7/22/2011)

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DRAWING TITLE		SCH, J59, MLB	
DRAWING NUMBER	051-8774	REVISION	C.0.0
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PAGE TITLE J59 BLOCK DIAGRAM			
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T29 Bus-Powered Device Power States:
 S4: Device negotiation, SRC_PWR = 3.0-3.6V (MCU function only)
 S3: Device sleep, SRC_PWR = 5.0-26.4V (optional wake functions supported)
 S0: Device running, SRC_PWR = 21.6-26.4V (run functions supported)
 NOTE: Devices not supporting wake function would not implement S3 state.

T29 Self-Powered Device Power States:
 S5: Device standby, no cable attached (MCU function & DP port power only)
 S3: Device sleep, cable attached (optional wake functions supported)
 S0: Device running, cable attached (run functions supported)

DP/T29 Display-Specific Power States:
 (In addition to S5-S0 states for T29 Self-Powered Device)
 D5: Display standby, no cables attached
 D3: Display sleep, DP cable detached or no source power, USB VBUS present (USB wake supported)
 D2: Display low-power, DP cable attached and source powered, source asleep per AUX command to TCON (USB wake supported)
 D0: Display ready, DP cable attached and source powered

NOTES:
 - D5 implies S5, S0 implies D0.
 - If only native DP source is attached, any Dx state can be supported while T29 is in S5.

NOTE: D2 not supported on Dr.B as there is no direct connection from panel TCON

Device Function:	Dr.B	Mr.Dev	Mr.Dev	Mr.Dev	Display	ENET	FW	SATA	DPIn
Power Source:	Self	Self	Bus	Bus	Self	Bus	Bus	Bus	Bus
Wake Support:	Yes	Yes	Yes	No	Yes	Yes	No	No	No
Q7560 FET 24V FW	FW (420mA / 10W)	FW (420mA)	FW (420mA)	FW (420mA)	FW (420mA)	N/A	FW (420mA)	N/A	N/A
U7000 TPS51980 3.3V S5	MCU (10mA)	MCU (10mA)	N/A	N/A	MCU (10mA)	N/A	N/A	N/A	N/A
1.05V T29	RTRx2, FW, SATA	RTR, FW, SATA	RTR, FW, SATA	RTR, FW, SATA	RTRx2, FW	RTR	RTR, FW	RTR, SATA	RTR
3.3V T29	RTRx2, FW, SATA	RTR, FW, SATA	RTR, FW, SATA	RTR, FW, SATA	RTRx2, FW	RTR	RTR, FW	RTR, SATA	RTR, mDP
UB500 TPS51980 5V S3	USB (2.1A)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3.3V S4	mDPx2 (1A)	mDPx2 (1A)	N/A	N/A	mDP (1A)	N/A	N/A	N/A	N/A
U7200 SC194A 1.2V ENET	DP++ (440mA)	DP++ (440mA)	N/A	N/A	DP++ (440mA)	N/A	N/A	N/A	N/A
U7300 SC194A 1.5V USB	PLX (USB) (210mA)	PLX (USB) (210mA)	N/A	N/A	PLX (USB) (210mA)	N/A	N/A	N/A	N/A
L7435 (U3900) 1.2V ENET	N/A	N/A	ENET (400mA?)	N/A	N/A	ENET (400mA?)	N/A	N/A	N/A
U7600 SC194A 1.8V SATA	SATA (250mA)	SATA (250mA)	SATA (250mA)	SATA (250mA)	N/A	N/A	N/A	SATA (250mA)	N/A
U7700 LP2951 3.3V MCU	N/A	N/A	MCU (10mA)	MCU (10mA)	N/A	MCU (10mA)	MCU (10mA)	MCU (10mA)	MCU (10mA)
U???? ????? 12V S5									
U???? ????? 24V S0									

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Power Block Diagram			
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BOM NUMBER	BOM NAME	BOM OPTIONS
639-1575	PCBA, MLB, J59	BASIC
085-2422	PCBA, MLB, DEV, J59	DEVELOPMENT

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE, T29HV:P12V, BIT_BANG_I2C, ENET_WAKE:PCIE, PIUSB_REV:B, PRODUCTION

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0945	1	IC, T29-PRQ, 220 FCBGA, 15X15MM	U3600	CRITICAL	
338S0753	1	IC, FW43-E, 1394B PHY/GBIC LINE/PCI-E, 12	U4100	CRITICAL	
343S0549	1	IC, ASIC, CRIT ENET, QFN-48, 6X6, BCS1761 B0	U3900	CRITICAL	
338S0977	1	PCI EXPRESS TO USB 2.0 HOST CONTROLLER (REV B)	U4600	CRITICAL	

FLASH	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
RAW: 335S0550	341T0376	1	IC, EEPROM, 359 PRIMARY, SPI, 32KBIT, MLP8	U3690	CRITICAL	
RAW: 335S0800	341T0331	1	ENET FLASH, C-IV, NO SD, J59	U3990	CRITICAL	
RAW: 335S0559	341T0375	1	IC, EEPROM, FW43-E2 GUID, I2C, 2KBIT, MLP8	U4290	CRITICAL	
RAW: 337S4115	341T0385	1	IC, MCU, 32B, LPC1114, 32KB/KB, HQQF33, J59	U5000	CRITICAL	
RAW: 337S4115	341T0385	1	IC, PRCMD, LPC1114, T29 SUPER MCU, HQQF33	U9330	CRITICAL	
RAW: 337S3558	341T0378	1	IC, PRCMD, LPC2144, J59 SYSTEM MCU	U2617	CRITICAL	
RAW: 353S2320	341T0369	1	IC, PRCMD, PRC0161, AUDIO/VID, PRC048	U1400	CRITICAL	

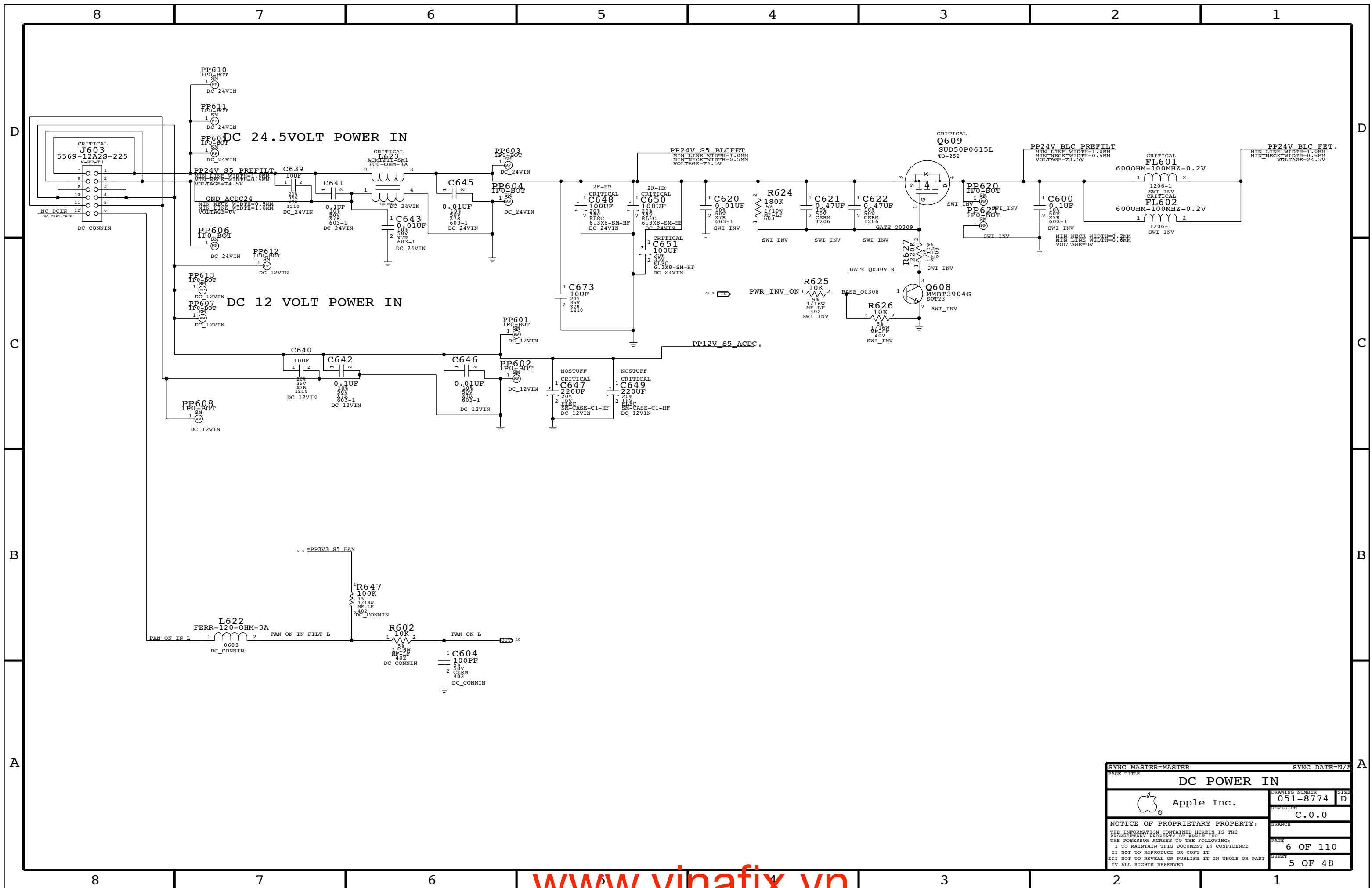
ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0977	376S0859		ALL	DIODES INC ALT FET
376S0972	376S0612		ALL	ROHM ALT FET
377S0107	377S0066		ALL	ON SEMI ALT RCLAMP
155S0431	155S0289		L1204	ALTERNATE CM CHOKE
376S1029	376S0953		ALL	ALTERNATE DC/DC FET
376S1030	376S0801		ALL	ALTERNATE DC/DC FET
376S1017	376S0612		ALL	ALTERNATE TOSH SS FET
377S0124	377S0057		ALL	ALTERNATE VARISTOR
152S1483	152S1376		ALL	ALTERNATE INDUCTOR
155S0691	155S0183		ALL	ALT BEAD FOR BL FILT
128S0262	128S0220		ALL	ADDS KEMET TO SANYO
138S0684	138S0660		ALL	ADDS MURATA TO TAIYO
155S0571	155S0309		ALL	ALTERNATE FERRITE
353S3477	353S3207		ALL	ALTERNATE FAB U9410

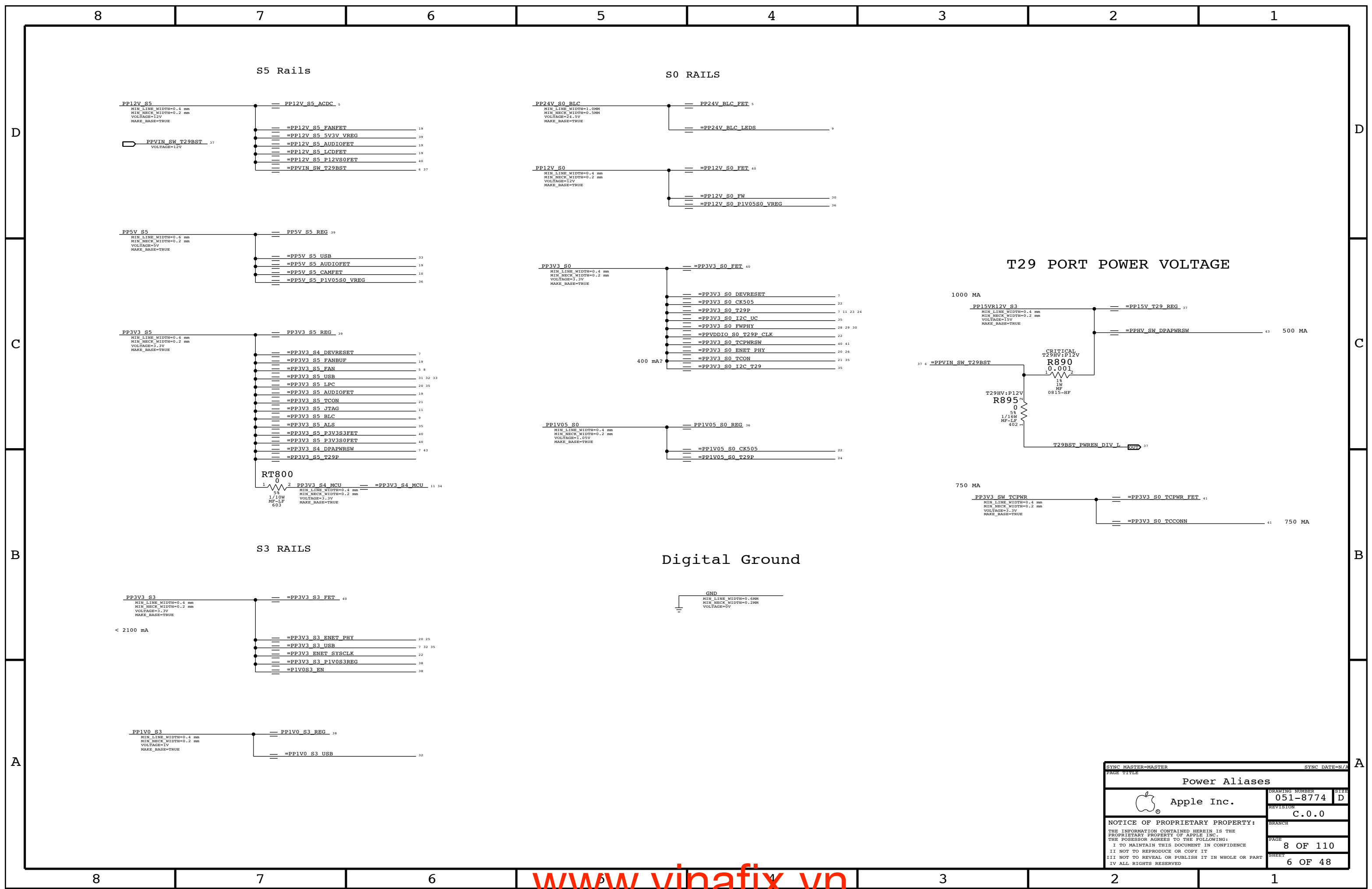
Schematic / PCB / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
820-2997	1	PCBF, MLB, J59	PCB1	CRITICAL	
051-8774	1	SCH, MLB, J59	SCH1	CRITICAL	
825-7122	1	MLB LABEL, 48.0MM X 4.8MM	[EEEE_DHMY]	CRITICAL	

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BOM Configuration & Misc			
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S5 Rails

S0 RAILS

T29 PORT POWER VOLTAGE

Digital Ground

S3 RAILS

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Power Aliases			
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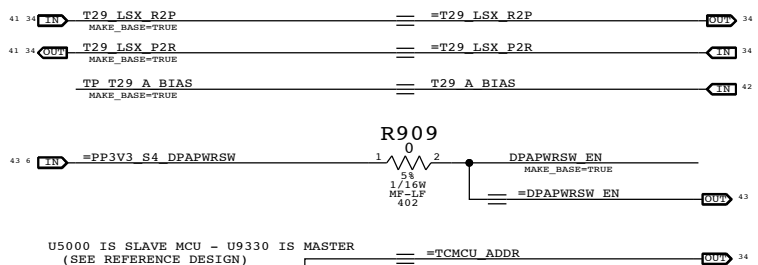
PCIe Assignments

IN	PCIE T29 R2D C P<0>	==	PCIE USB R2D C P	OUT	32 46
IN	PCIE T29 R2D C N<0>	==	PCIE USB R2D C N	OUT	32 46
OUT	PCIE T29 D2R P<0>	==	PCIE USB D2R P	IN	32 46
OUT	PCIE T29 D2R N<0>	==	PCIE USB D2R N	IN	32 46
IN	T29_PCIE_RESET L<0>	==	USB RESET L	OUT	32
IN	PCIE T29 R2D C P<1>	==	PCIE ENET R2D C P	OUT	26 46
IN	PCIE T29 R2D C N<1>	==	PCIE ENET R2D C N	OUT	26 46
OUT	PCIE T29 D2R P<1>	==	PCIE ENET D2R P	IN	26 46
OUT	PCIE T29 D2R N<1>	==	PCIE ENET D2R N	IN	26 46
IN	T29_PCIE_RESET L<1>	==	ENET RESET L	OUT	26
IN	PCIE T29 R2D C P<2>	==	PCIE FW R2D C P	OUT	28 46
IN	PCIE T29 R2D C N<2>	==	PCIE FW R2D C N	OUT	28 46
OUT	PCIE T29 D2R P<2>	==	PCIE FW D2R P	IN	28 46
OUT	PCIE T29 D2R N<2>	==	PCIE FW D2R N	IN	28 46
IN	T29_PCIE_RESET L<2>	==	FW RESET L	OUT	28
IN	PCIE T29 R2D C P<3>	==	NC_PCIE_T29_R2D_C_P3		
IN	PCIE T29 R2D C N<3>	==	NC_PCIE_T29_R2D_C_N3		
OUT	PCIE T29 D2R P<3>	==	NC_PCIE_T29_D2R_P3		
OUT	PCIE T29 D2R N<3>	==	NC_PCIE_T29_D2R_N3		
IN	T29_PCIE_RESET L<3>	==	NC_T29_PCIE_RESET_L3		

INTERNAL DP PANEL SOURCE MUX BYPASS

IN	DP T29SRCA ML C P<0>	==	DP INT ML C P<0>	OUT	7 44
IN	DP T29SRCA ML C N<0>	==	DP INT ML C N<0>	OUT	7 44
IN	DP T29SRCA ML C P<1>	==	DP INT ML C P<1>	OUT	7 44
IN	DP T29SRCA ML C N<1>	==	DP INT ML C N<1>	OUT	7 44
IN	DP T29SRCA ML C P<2>	==	DP INT ML C P<2>	OUT	7 44
IN	DP T29SRCA ML C N<2>	==	DP INT ML C N<2>	OUT	7 44
IN	DP T29SRCA ML C P<3>	==	DP INT ML C P<3>	OUT	7 44
IN	DP T29SRCA ML C N<3>	==	DP INT ML C N<3>	OUT	7 44
IN	DP T29SRCA AUXCH C P	==	DP INT AUXCH C P	OUT	7 44
IN	DP T29SRCA AUXCH C N	==	DP INT AUXCH C N	OUT	7 44
OUT	DP T29SRCA HPD	==	DP INT HPD	IN	21

MISC T29 ALIAS CONNECTIONS

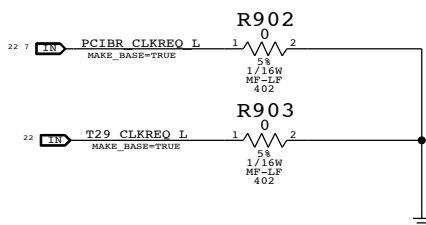


U5000 IS SLAVE MCU - U9330 IS MASTER (SEE REFERENCE DESIGN)

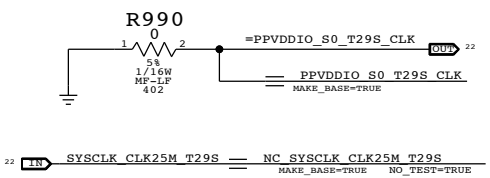
CLOCKS

IN	PCIE_CLK100M_PCIBR_P	==	PCIE_CLK100M_USB_P	OUT	32 46
IN	PCIE_CLK100M_PCIBR_N	==	PCIE_CLK100M_USB_N	OUT	32 46
OUT	PCIBR_CLKREQ_L	==	PCIE_CLKREQ4		
IN	PCIE_CLK100M_T29S_P	==	NC_PCIE_CLK100M_SRC6P		
IN	PCIE_CLK100M_T29S_N	==	NC_PCIE_CLK100M_SRC6N		
OUT	T29S_CLKREQ_L	==	PCIE_CLKREQ6		
IN	PCIE_CLK100M_SLOT_P	==	NC_PCIE_CLK100M_SRC1P		
IN	PCIE_CLK100M_SLOT_N	==	NC_PCIE_CLK100M_SRC1N		
OUT	PCIESLOT_CLKREQ_L	==	PCIE_CLKREQ1		
IN	PCIE_CLK100M_SATA_P	==	NC_PCIE_CLK100M_SRC9P		
IN	PCIE_CLK100M_SATA_N	==	NC_PCIE_CLK100M_SRC9N		
OUT	SATA_CLKREQ_L	==	PCIE_CLKREQ9		
IN	FW_CLK24P576M	==	NC_FW_CLK24P576M		
IN	PS161_CLK27M_R	==	NC_CLK27M		
IN	PCI_CLK33M_PCIBR	==	NC_PCIE_CLK33M		
IN	PCI_CLK33M_NECUSB	==	NC_PCIE_CLK33M		

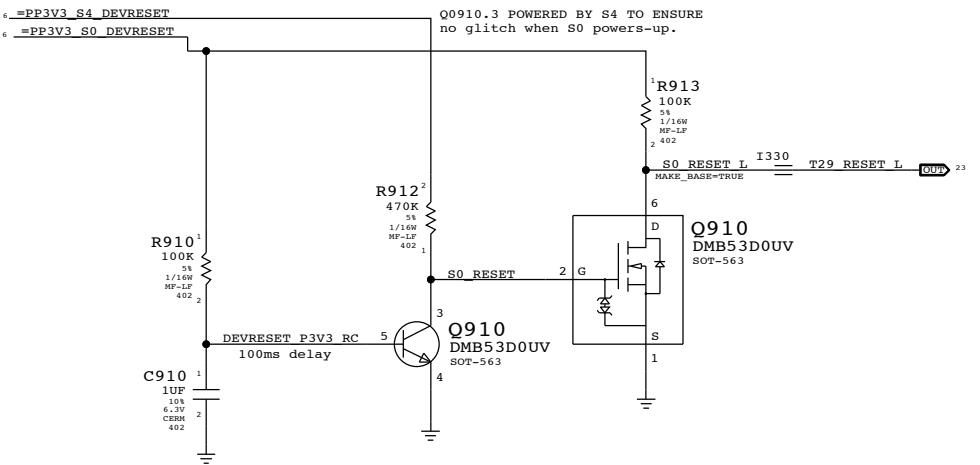
PCIe CLKREQ ENABLING



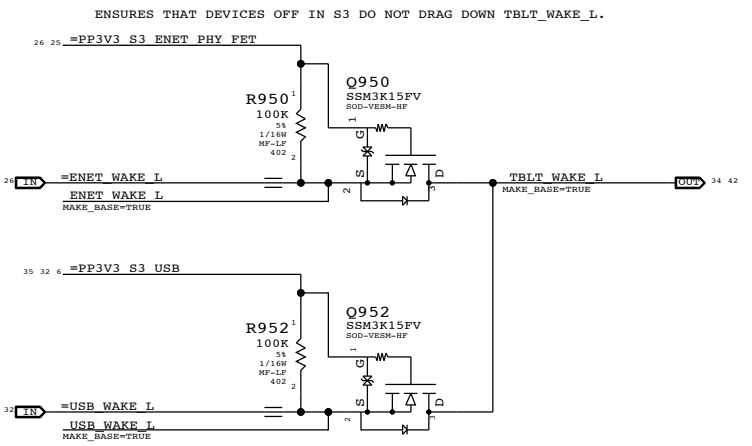
UNUSED T29S GREENCLK



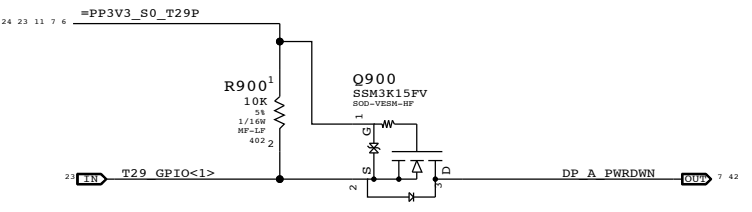
Power-Up Reset Generation



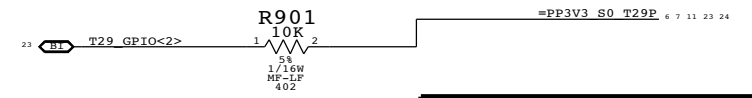
Wake Sources Power State Isolation



T29 GPIO TO DETECT ERRANT PASSIVE DP CABLE CONNECTION



UNUSED T29 ROUTER GPIOs



INTERNAL DP PANEL AC COUPLING CAPS

IN	DP_INT_ML_C_P<0>	C900	DP_INT_ML_C_P<0>	OUT	21 44 48
IN	DP_INT_ML_C_N<0>	C901	DP_INT_ML_C_N<0>	OUT	21 44 48
IN	DP_INT_ML_C_P<1>	C902	DP_INT_ML_C_P<1>	OUT	21 44 48
IN	DP_INT_ML_C_N<1>	C903	DP_INT_ML_C_N<1>	OUT	21 44 48
IN	DP_INT_ML_C_P<2>	C904	DP_INT_ML_C_P<2>	OUT	21 44 48
IN	DP_INT_ML_C_N<2>	C905	DP_INT_ML_C_N<2>	OUT	21 44 48
IN	DP_INT_ML_C_P<3>	C906	DP_INT_ML_C_P<3>	OUT	21 44 48
IN	DP_INT_ML_C_N<3>	C907	DP_INT_ML_C_N<3>	OUT	21 44 48
IN	DP_INT_AUXCH_C_P	C908	DP_INT_AUXCH_C_P	OUT	21 44 48
IN	DP_INT_AUXCH_C_N	C909	DP_INT_AUXCH_C_N	OUT	21 44 48

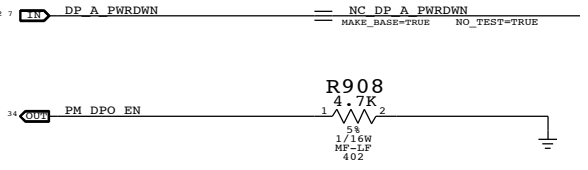
Misc Ethernet Aliases

OUT	ENET_LOW_PWR	==	TP_ENET_LOW_PWR		
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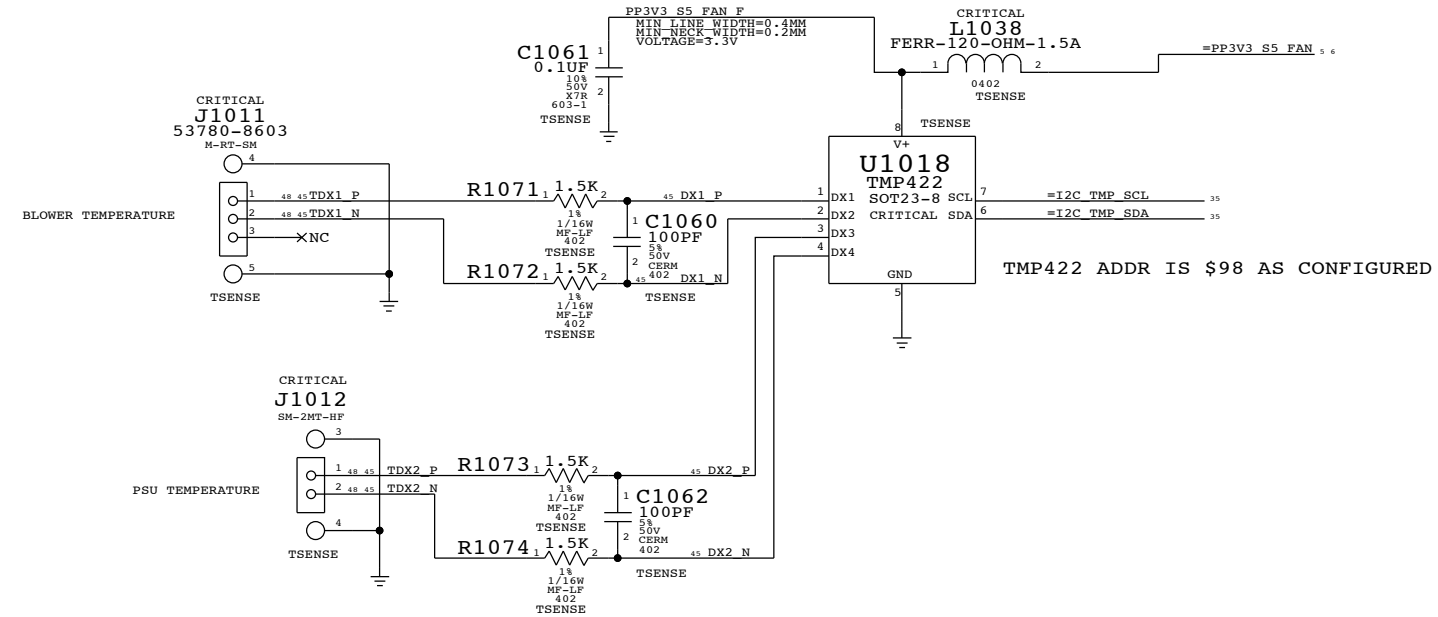
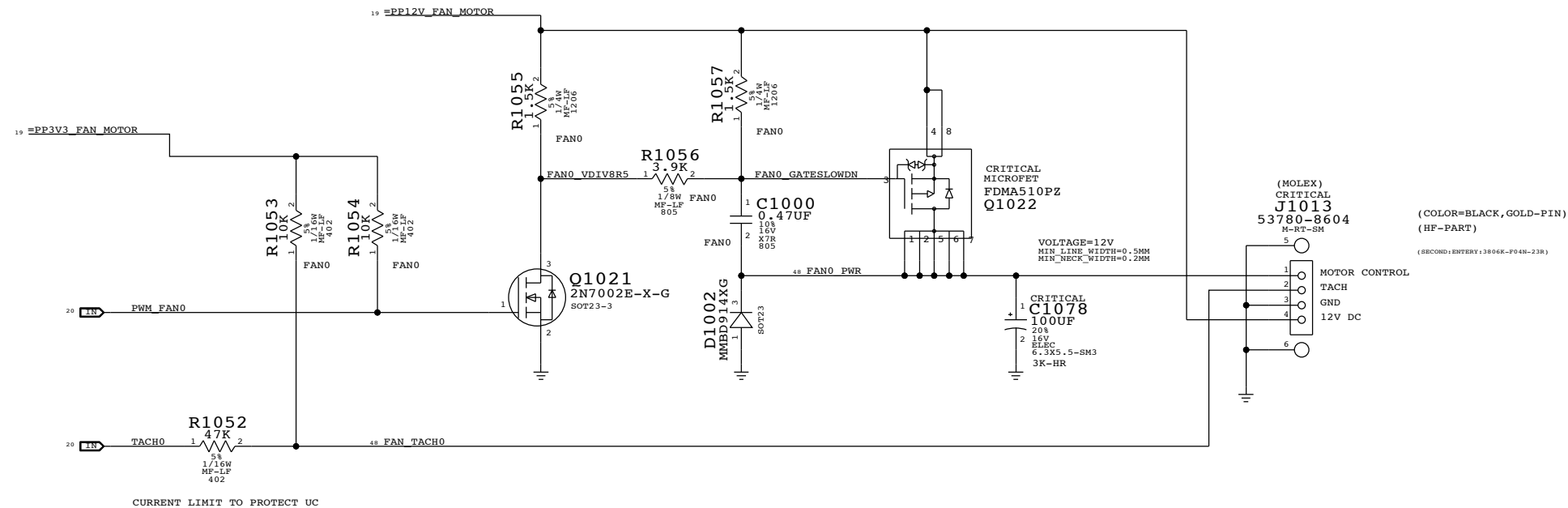
Misc FireWire Aliases

IN	FW_PME_L	==	TP_FW_WAKE_L		
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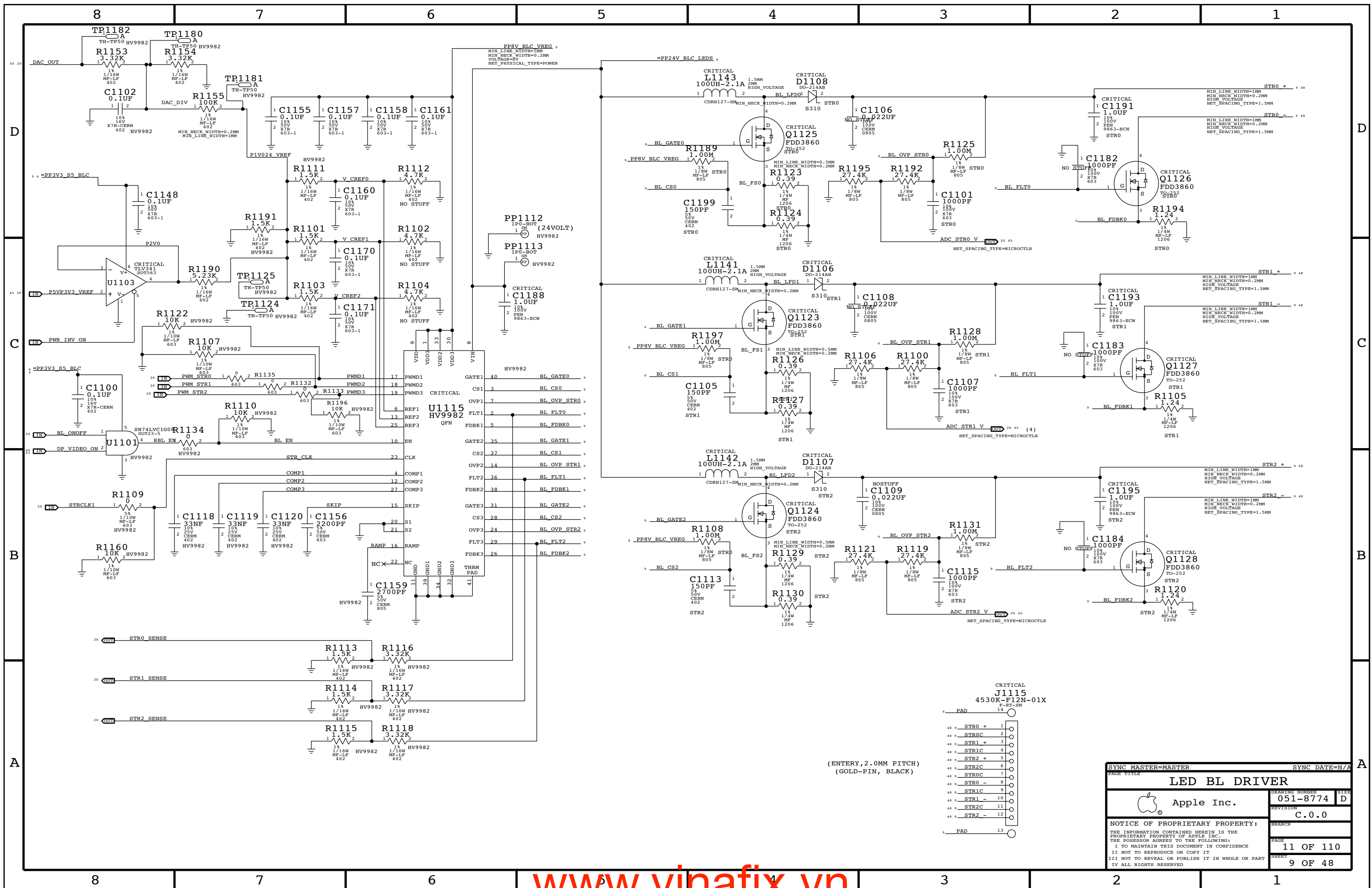
T29 NOCONNECTS DUE TO SINGLE PORT AND NO DPOUT



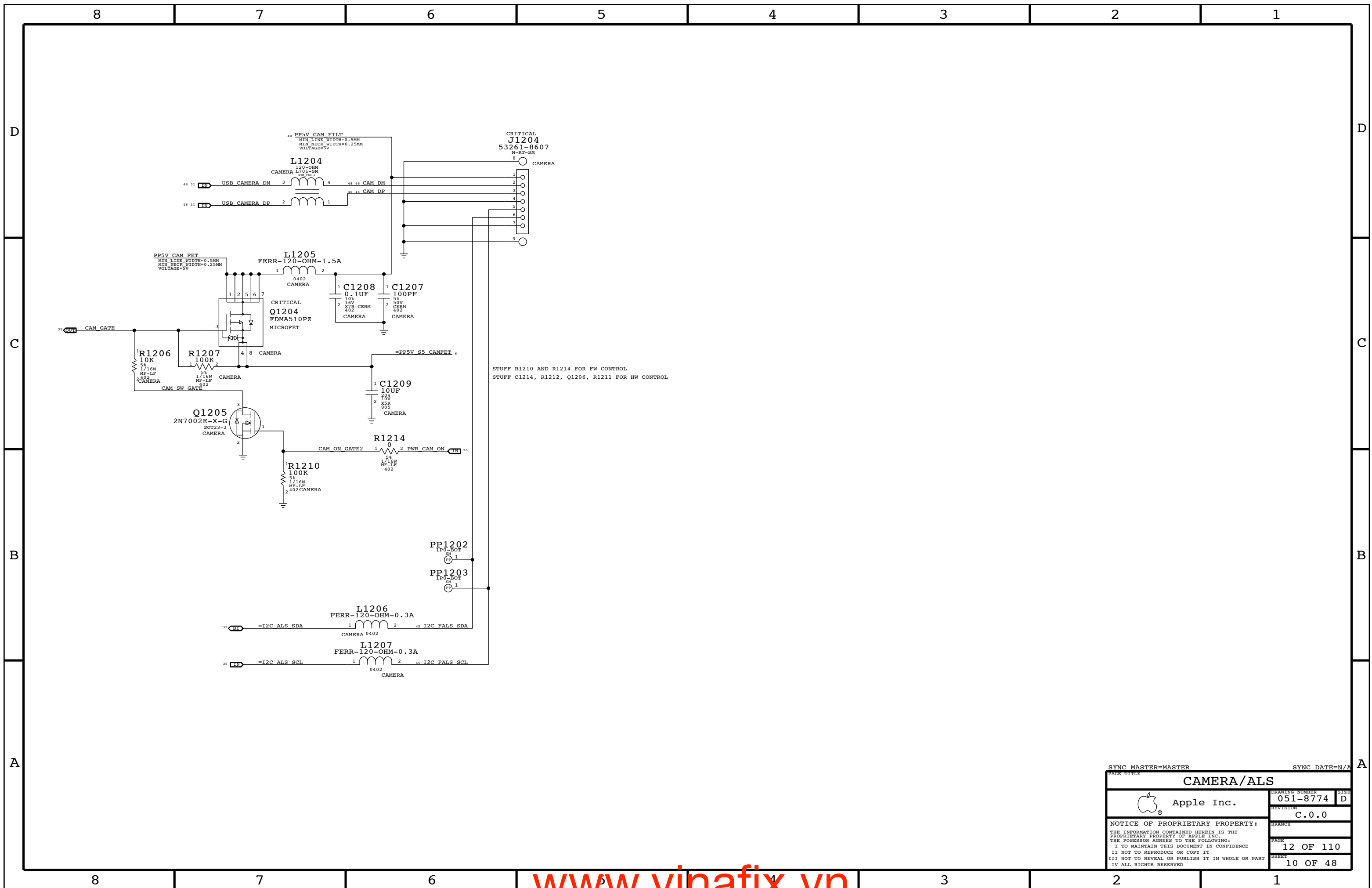
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LED BL DRIVER			
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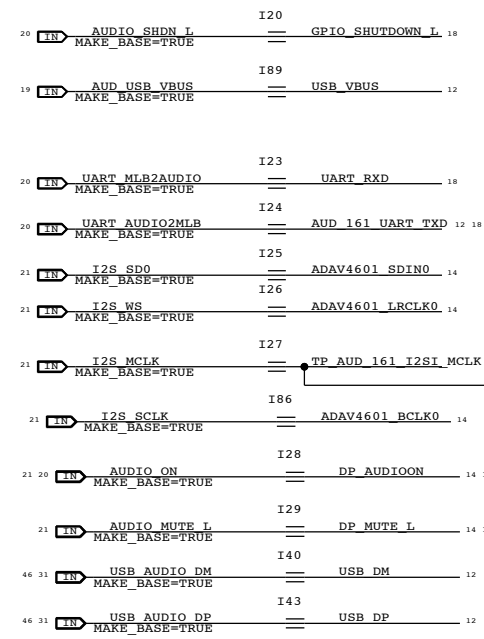


STUFF R1210 AND R1214 FOR FW CONTROL
 STUFF C1214, R1212, Q1206, R1211 FOR HW CONTROL

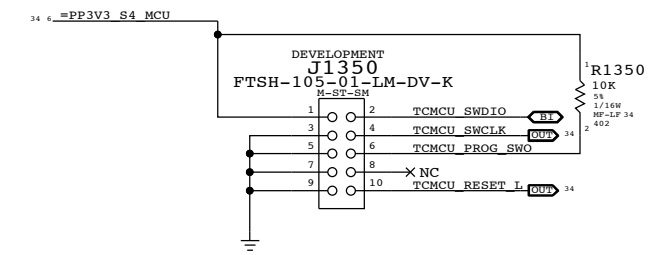
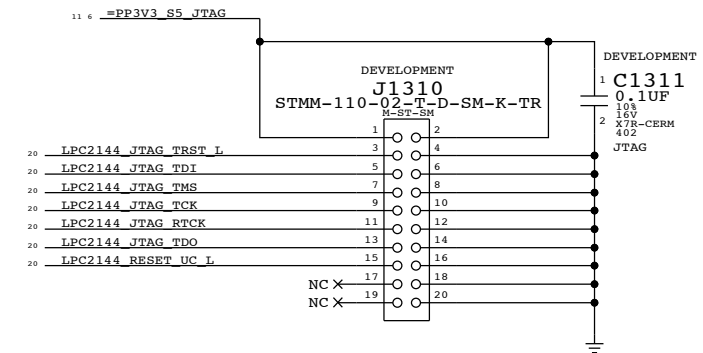
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		SHEET	10 OF 48

T29 JTAG AND DEBUG

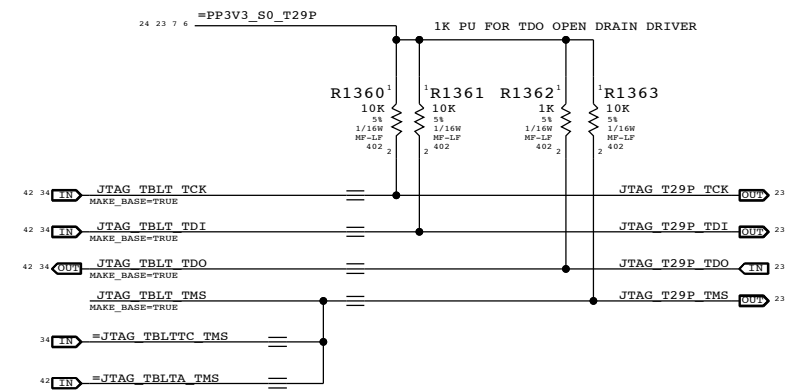
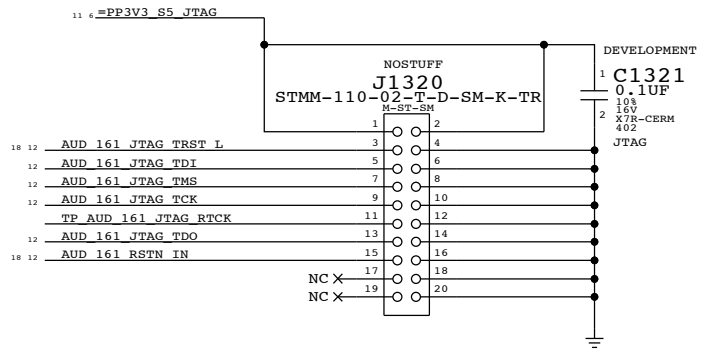
AUDIO ALIASES



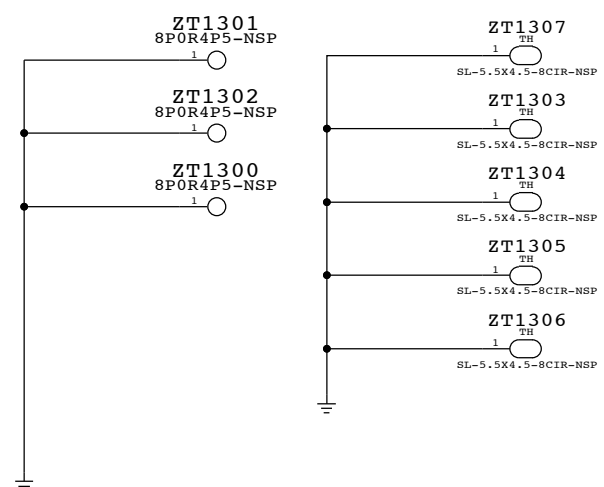
SYSTEM MICRO JTAG



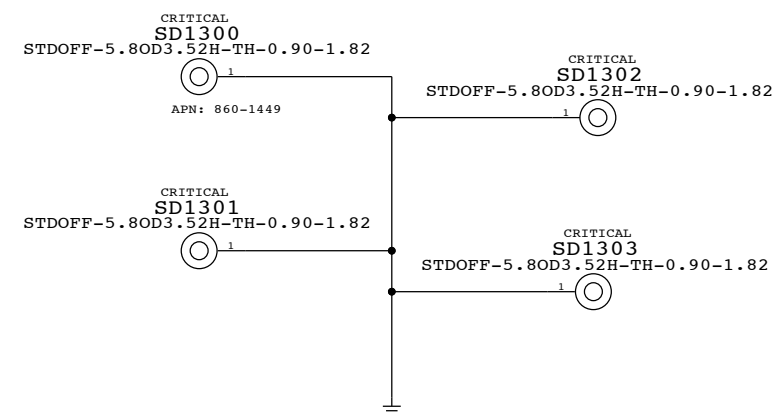
AUDIO JTAG



MOUNTING HOLES



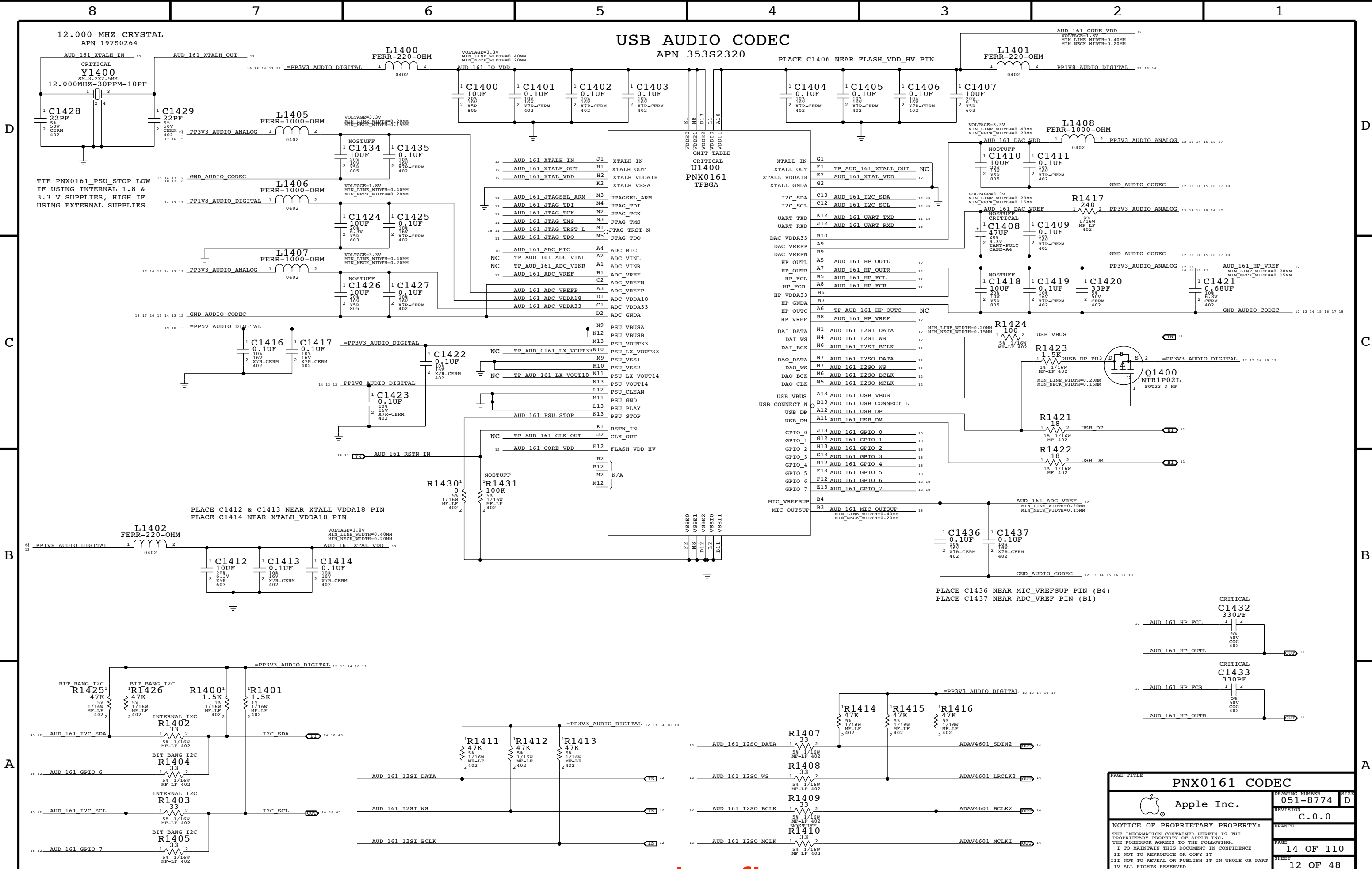
J9000 TETHERED CABLE CLAMP STANDOFFS



PAGE TITLE		SYNC DATE=08/22/2010	
DEBUG, MISC & JTAG			
Apple Inc.		DRAWING NUMBER	051-8774
		REVISION	C.0.0
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USB AUDIO CODEC

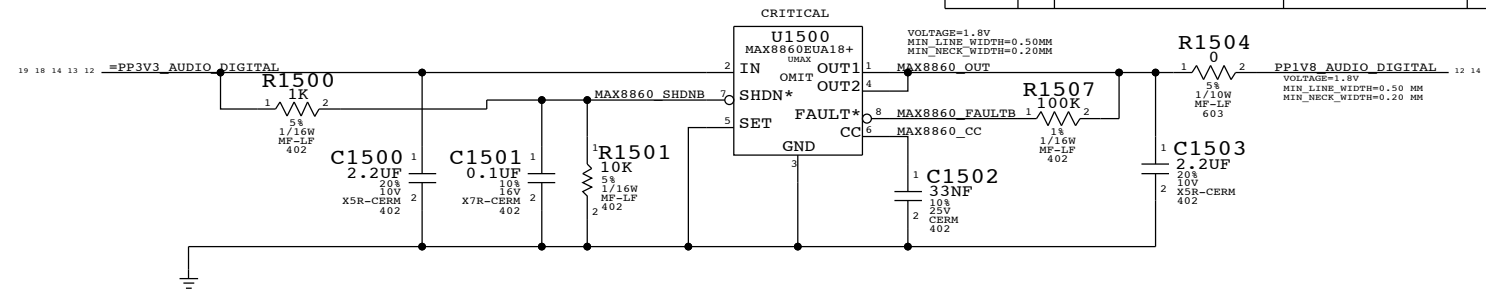
APN 353S2320



PAGE TITLE	
PNX0161 CODEC	
Apple Inc.	
DRAWING NUMBER	051-8774
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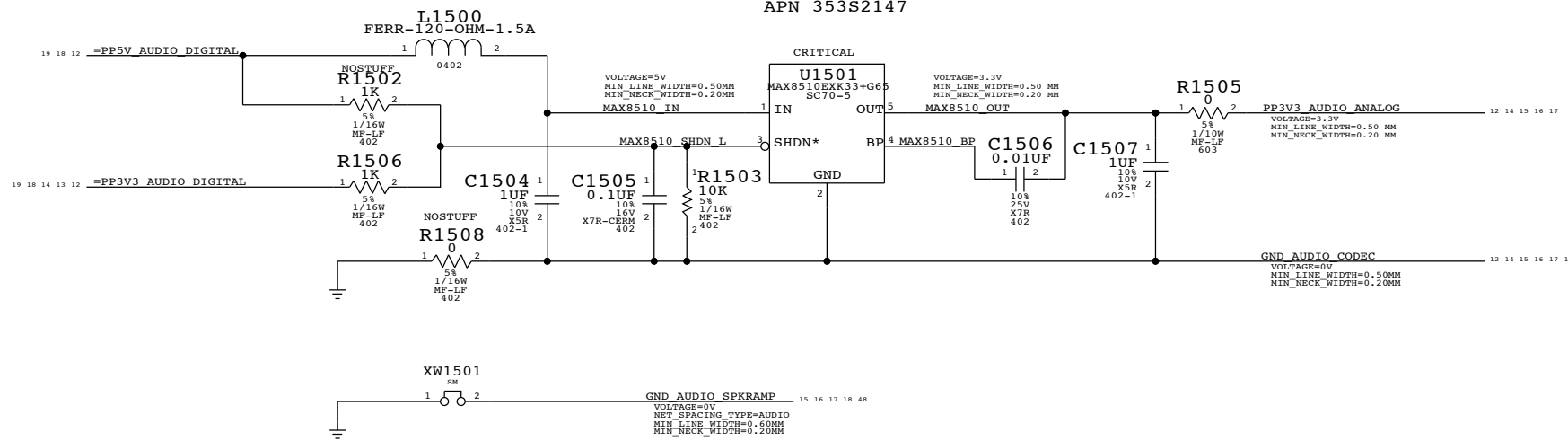
1.8 V REGULATOR
APN 353S2847

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S2847	1	HF MAX8860EUA18+G65	U1500	



6/16 IT'S UNCLEAR IF ANALOG 3.3 V NEEDS TO COME UP WITH DIGITAL 3.3 V,
OR IF IT CAN COME UP INDEPENDENTLY (WITH 3.3 V)
ANALOG 3.3 COMES UP WITH DIGITAL 3.3 --> POPULATE R1506
ANALOG 3.3 COMES UP INDEPENDENTLY --> POPULATE R1502

3.3 V REGULATOR
APN 353S2147



D

D

C

C

B

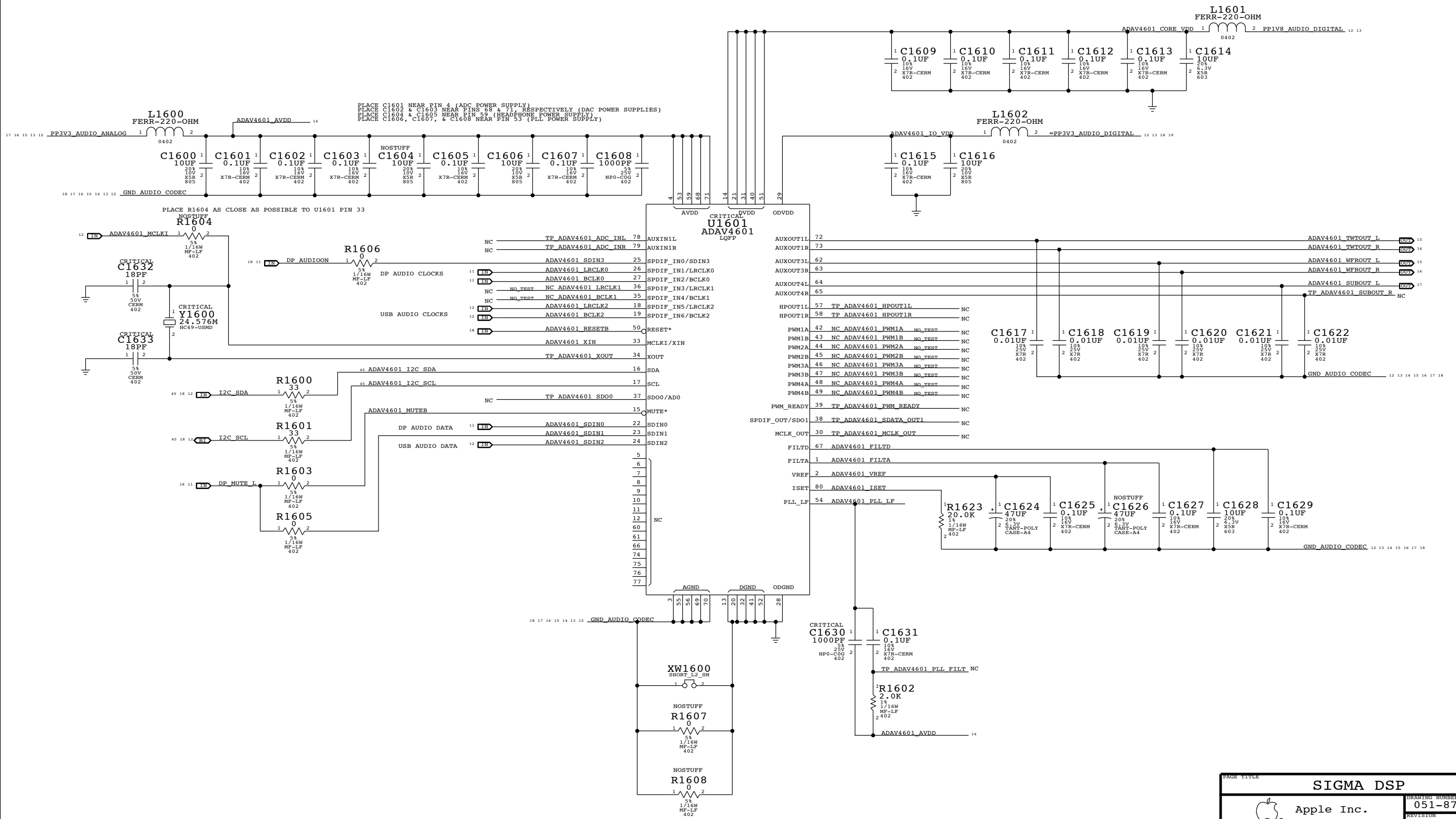
B

A

A

PAGE TITLE		
AUDIO DC-DC REGULATORS		
Apple Inc.	DRAWING NUMBER	051-8774
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AUDIO SIGNAL PROCESSOR
APN 337S3285



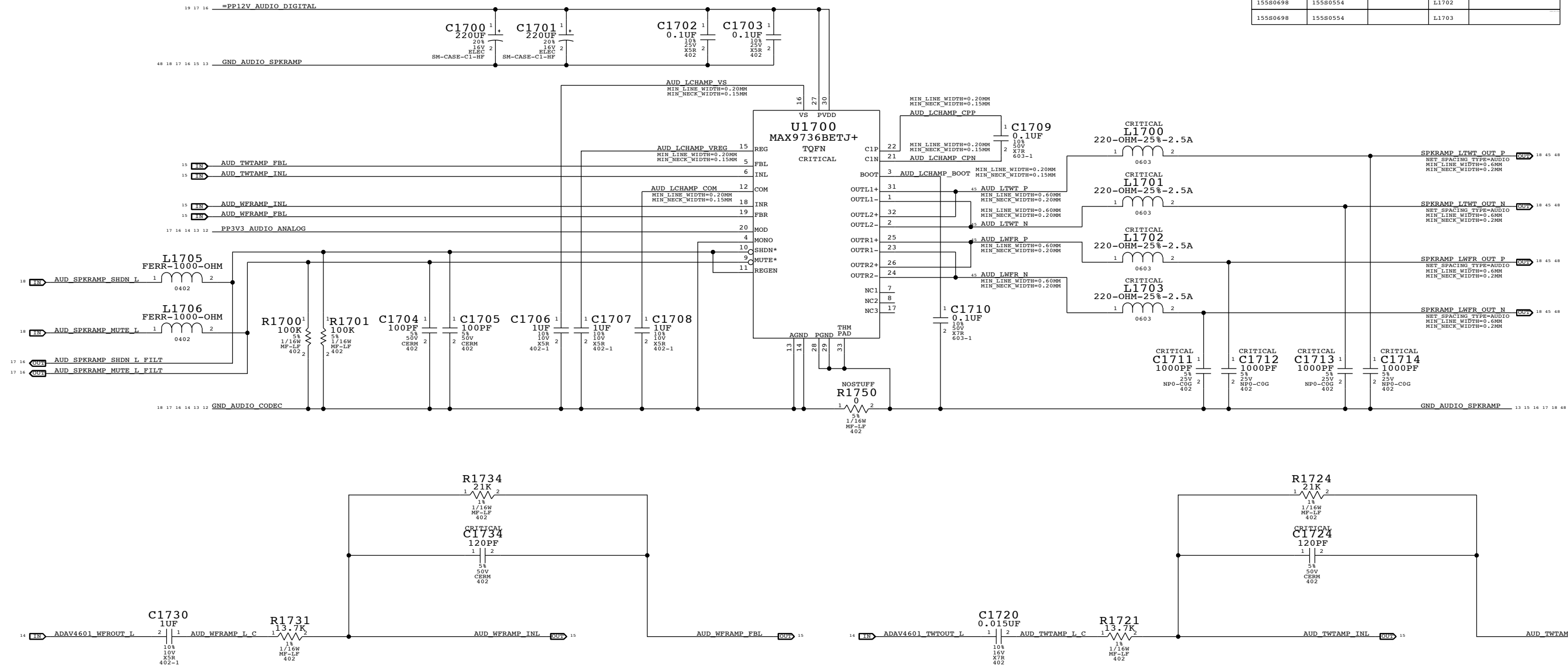
GND CONNECTIONS WERE ADDED TO ADDRESS EMI CONCERNS ON K59

PAGE TITLE		SIGMA DSP	
Apple Inc.		DRAWING NUMBER	051-8774
		REVISION	C.0.0
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LEFT SPEAKER AMP

APN 353S2042
 GAIN = 7.36 V/V (+17.33 DB)
 FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580698	15580554		L1700	
15580698	15580554		L1701	
15580698	15580554		L1702	
15580698	15580554		L1703	

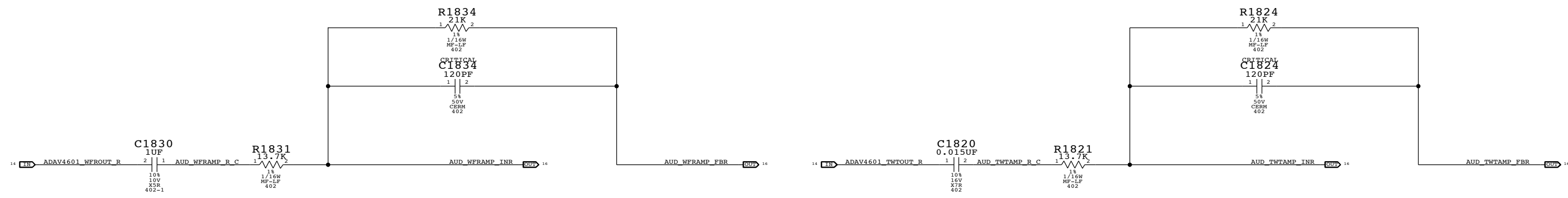
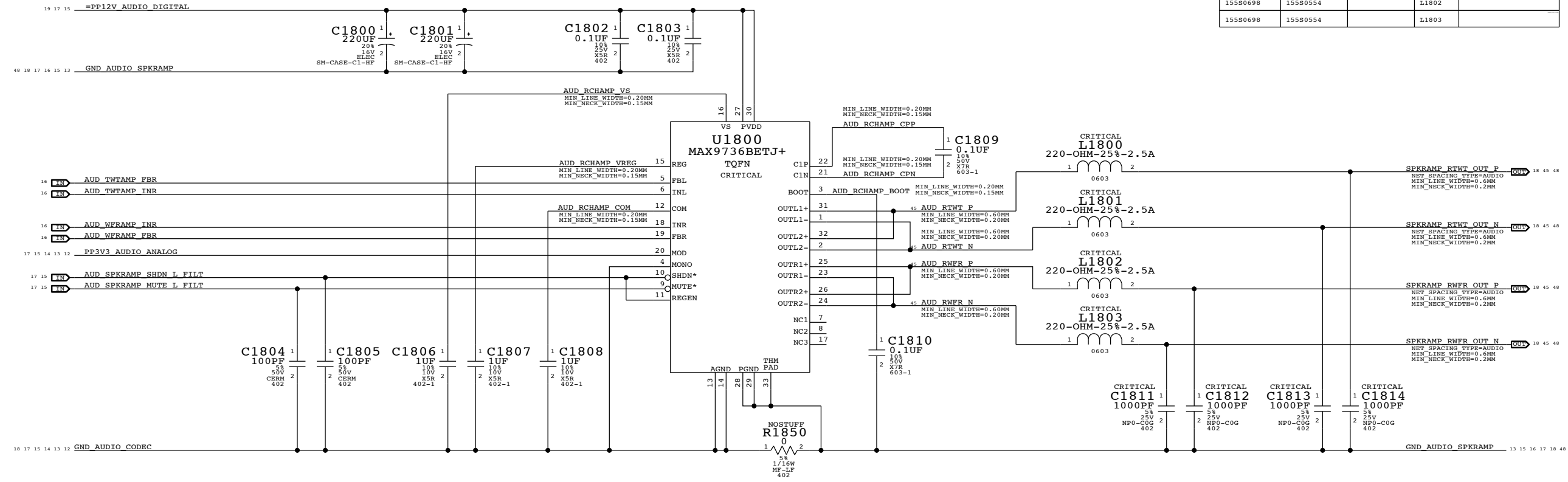


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LEFT SPEAKER AMP		051-8774		D
Apple Inc.		REVISION		C.0.0
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RIGHT SPEAKER AMP

APN 353S2042
 GAIN = 7.36 V/V (+17.33 DB)
 FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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15580698	15580554		L1801	
15580698	15580554		L1802	
15580698	15580554		L1803	

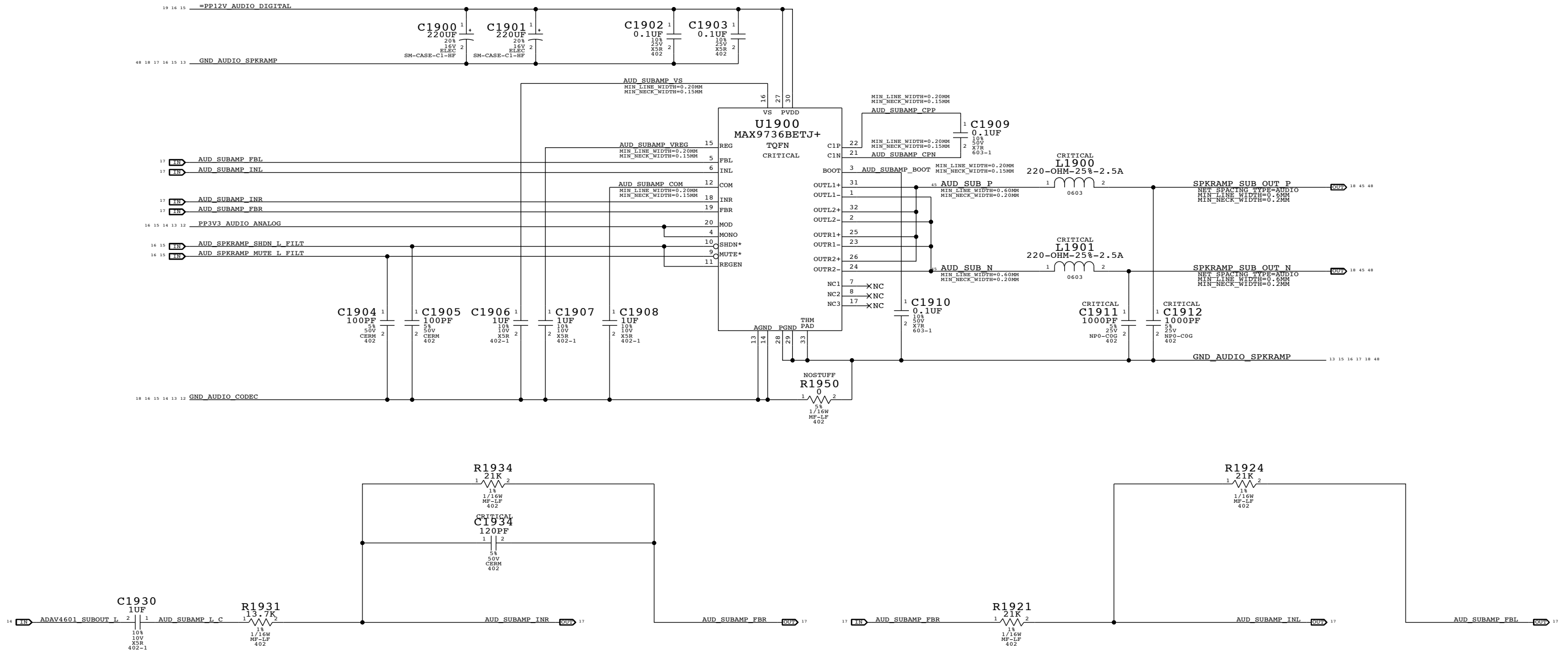


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RIGHT SPEAKER AMP		051-8774		D
Apple Inc.		REVISION		C.0.0
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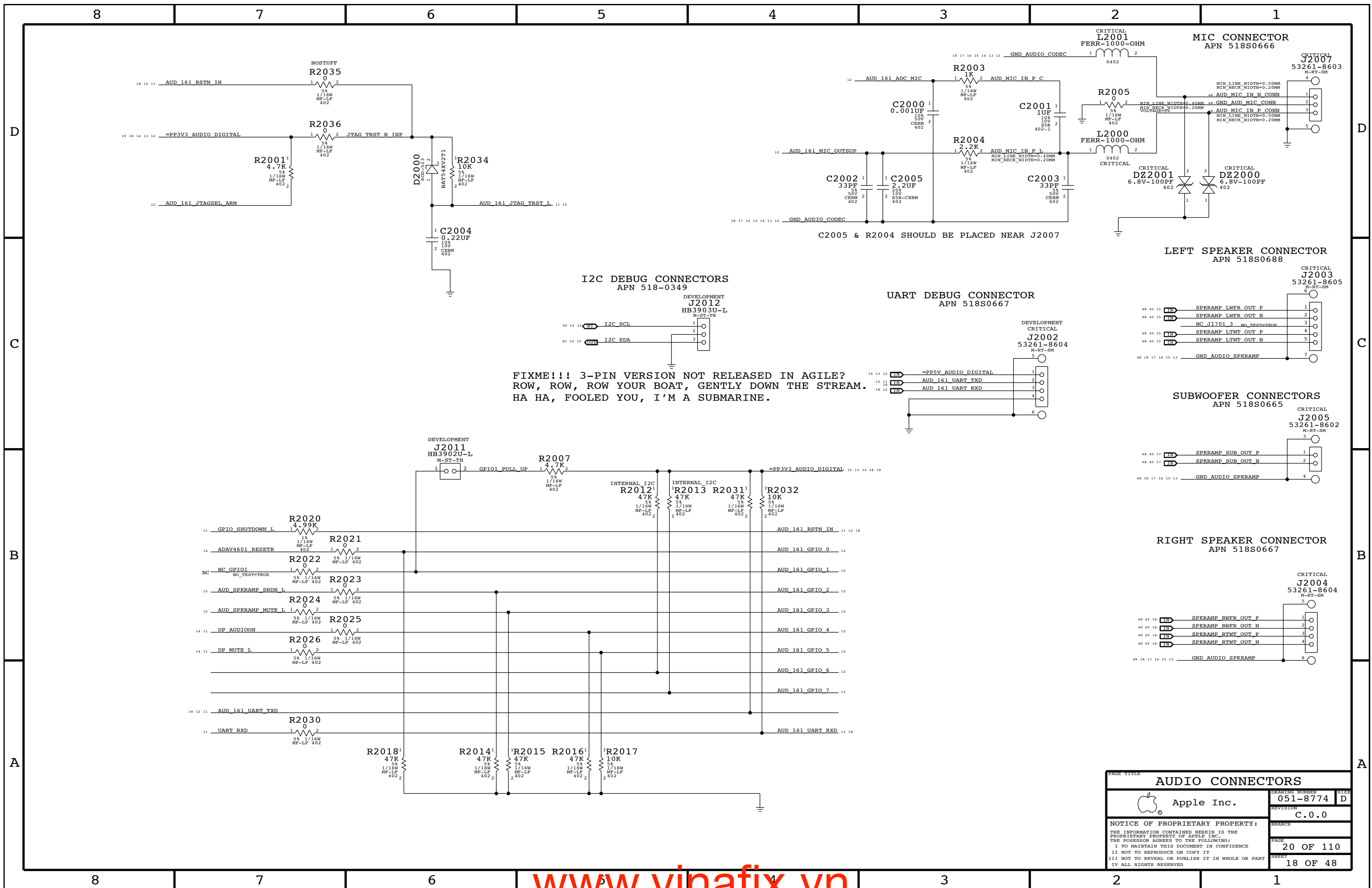
SUBWOOFER SPEAKER AMP

APN 353S2042
 GAIN = 7.36 V/V (+17.33 DB)
 FC = ~12 HZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1900	
155S0698	155S0554		L1901	



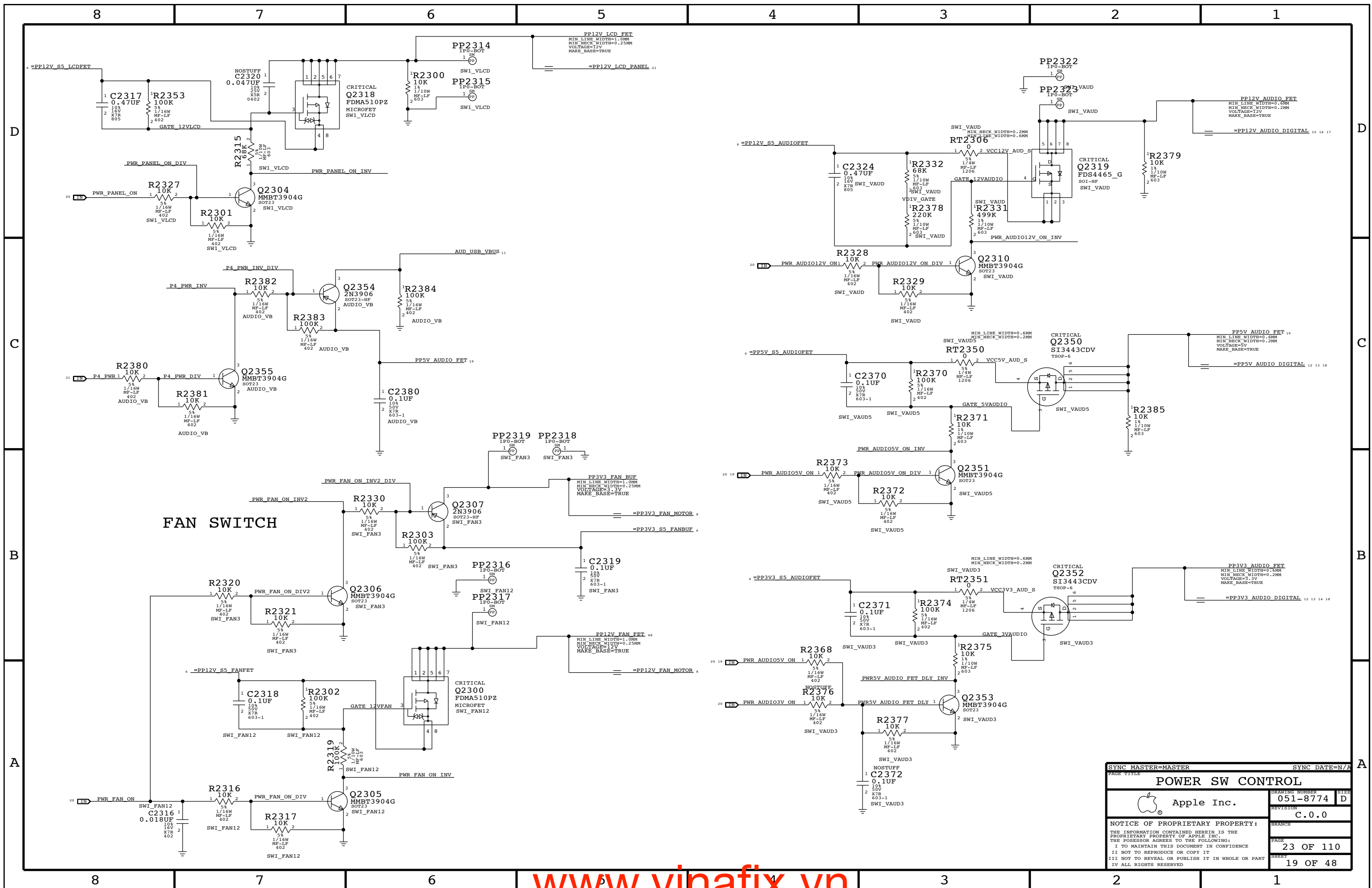
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SUBWOOFER SPEAKER AMP		051-8774		D
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		PAGE		19 OF 110
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FIXME!!! 3-PIN VERSION NOT RELEASED IN AGILE?
 ROW, ROW, ROW YOUR BOAT, GENTLY DOWN THE STREAM.
 HA HA, FOOLED YOU, I'M A SUBMARINE.

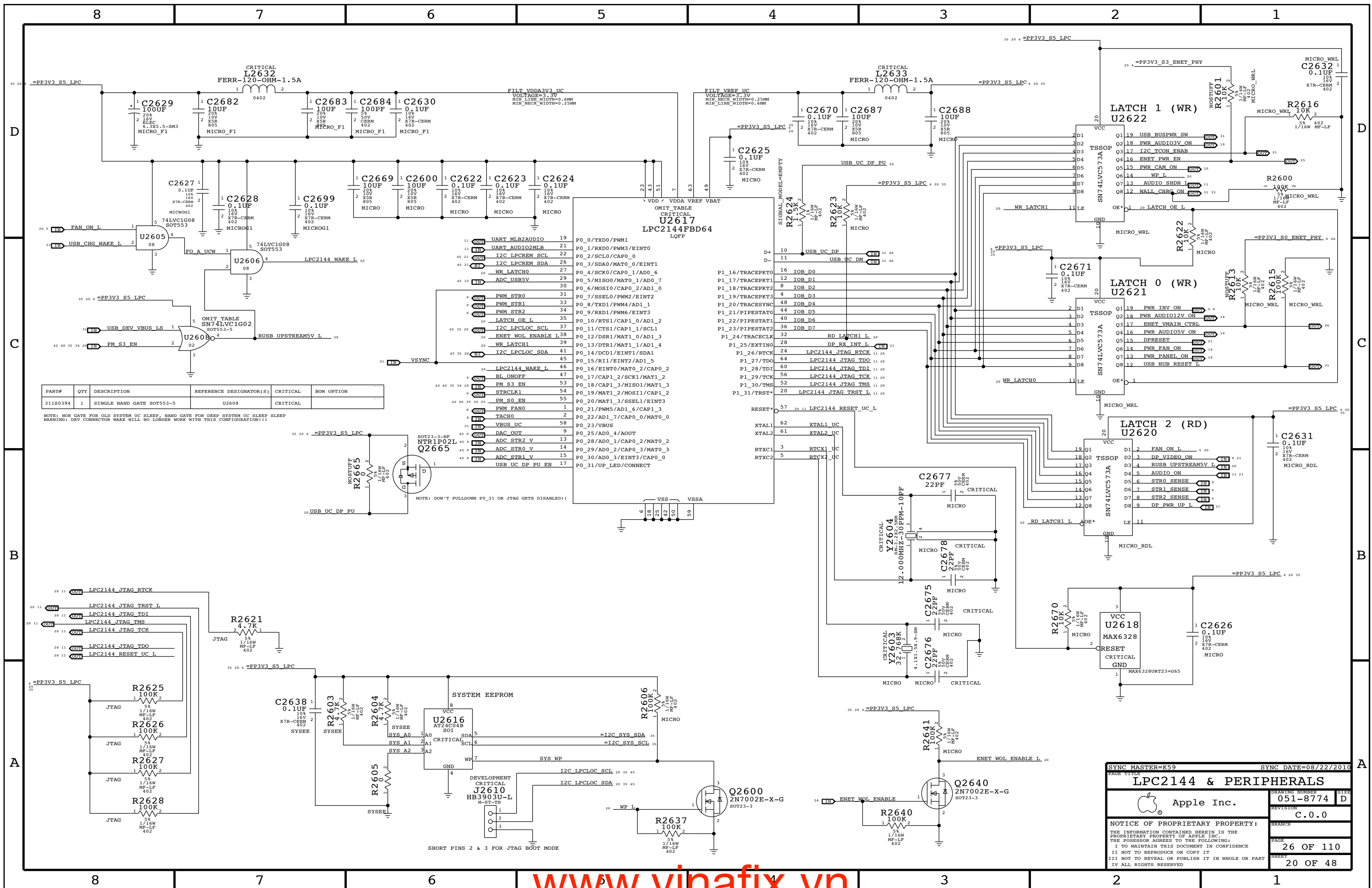
C2005 & R2004 SHOULD BE PLACED NEAR J2007

PAGE TITLE		
AUDIO CONNECTORS		
Apple Inc.	DRAWING NUMBER	051-8774
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FAN SWITCH

PAGE TITLE		SYNC DATE=N/A	
POWER SW CONTROL		DRAWING NUMBER	SIZE
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		C.0.0	23 OF 110
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
31150394	1	SINGLE NAND GATE SOT553-5	U2608	CRITICAL	

NOTE: NOR GATE FOR OLD SYSTEM UC SLEEP, NAND GATE FOR DEEP SYSTEM UC SLEEP SLEEP WARNING: DEV CONNECTOR WAKE WILL NO LONGER WORK WITH THIS CONFIGURATION!!!

OMIT TABLE
CRITICAL
U2617
LPC2144FBD64
LQFP

19	UART MLB2AUDIO	P0_0/TXD0/PWM1
21	UART AUDIO2MLB	P0_1/RXD0/PWM3/EINT0
22	I2C LPCREM_SCL	P0_2/SCL0/CAPO_0
26	I2C LPCREM_SDA	P0_3/SDA0/MATO_0/EINT1
27	WR LATCH0	P0_4/SCK0/CAPO_1/AD0_6
29	ADC USB5V	P0_5/MISO0/MATO_1/AD0_7
30		P0_6/MOSI0/CAPO_2/AD1_0
31	PWM_STR0	P0_7/SSEL0/PWM2/EINT2
33	PWM_STR1	P0_8/TXD1/PWM4/AD1_1
34	PWM_STR2	P0_9/RXD1/PWM6/EINT3
35	LATCH_OR_L	P0_10/RTS1/CAP1_0/AD1_2
37	I2C LPCLOC_SCL	P0_11/CTS1/CAP1_1/SCL1
38	ENET WOL ENABLE_L38	P0_12/DSR1/MAT1_0/AD1_3
39	WR LATCH1	P0_13/TRD1/MAT1_1/AD1_4
41	I2C LPCLOC_SDA	P0_14/DCD1/EINT1/SDA1
45		P0_15/RI1/EINT2/AD1_5
46	LEPC2144_WAKE_L	P0_16/EINT0/MATO_2/CAPO_2
47	BL_ONOFF	P0_17/CAP1_2/SCK1/MAT1_2
53	PM_S3_EN	P0_18/CAP1_3/MISO1/MAT1_3
54	STRCLK1	P0_19/MAT1_2/MOSI1/CAP1_2
55	PM_S0_EN	P0_20/MAT1_3/SSEL1/EINT3
57	PWM_FANO	P0_21/PWM5/AD1_6/CAP1_3
2	TACH0	P0_22/AD1_7/CAPO_0/MATO_0
58	VBUS_UC	P0_23/VBUS
9	DAC_OUT	P0_25/AD0_4/AOUT
13	ADC_STR2_V	P0_28/AD0_1/CAPO_2/MATO_2
14	ADC_STR0_V	P0_29/AD0_2/CAPO_3/MATO_3
15	ADC_STR1_V	P0_30/AD0_3/EINT3/CAPO_0
17	USB_UC_DP_PU_EN	P0_31/UP_LED/CONNECT

SYNC MASTER=K59 SYNC DATE=08/22/2010

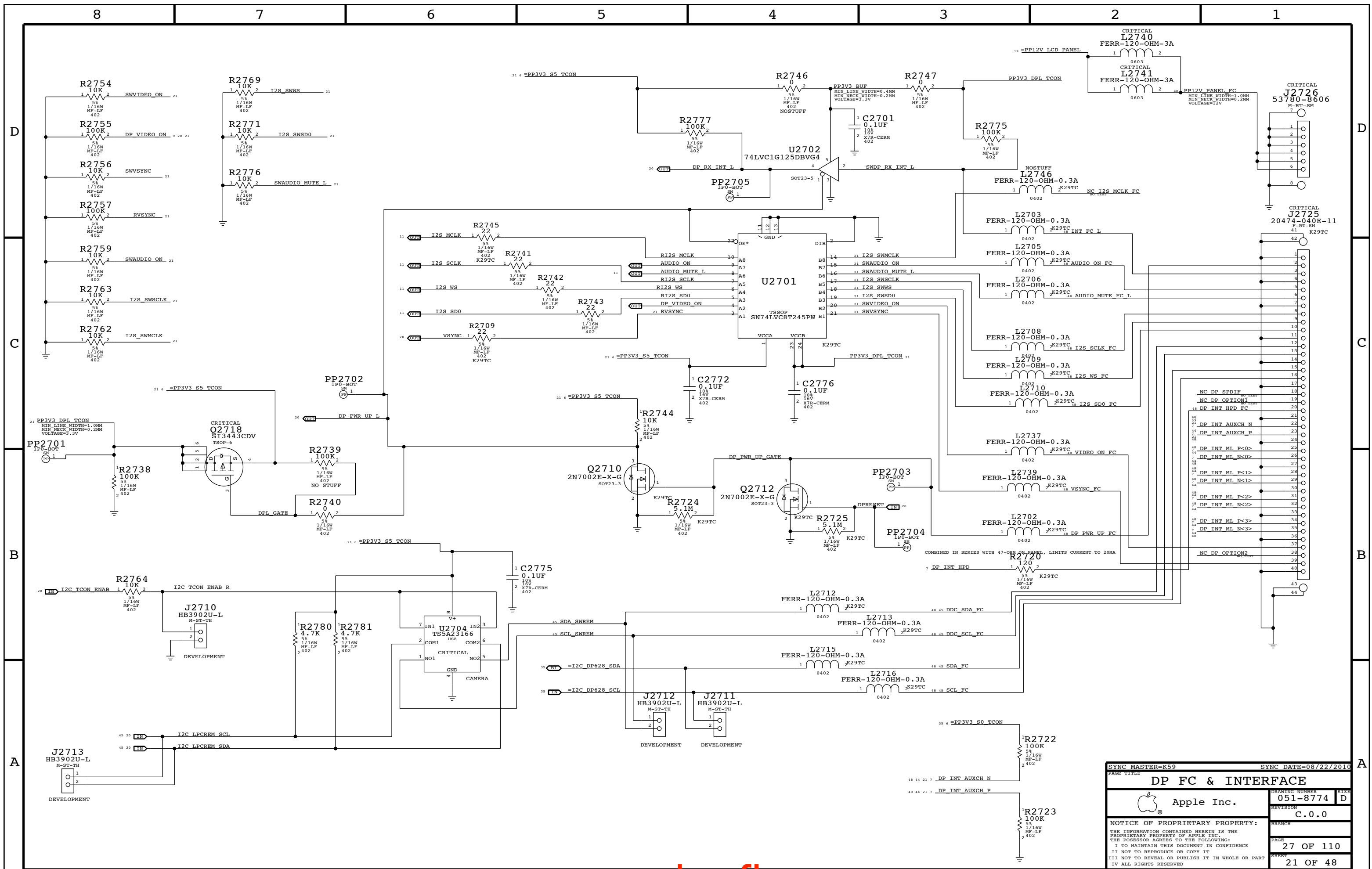
LPC2144 & PERIPHERALS

Apple Inc.

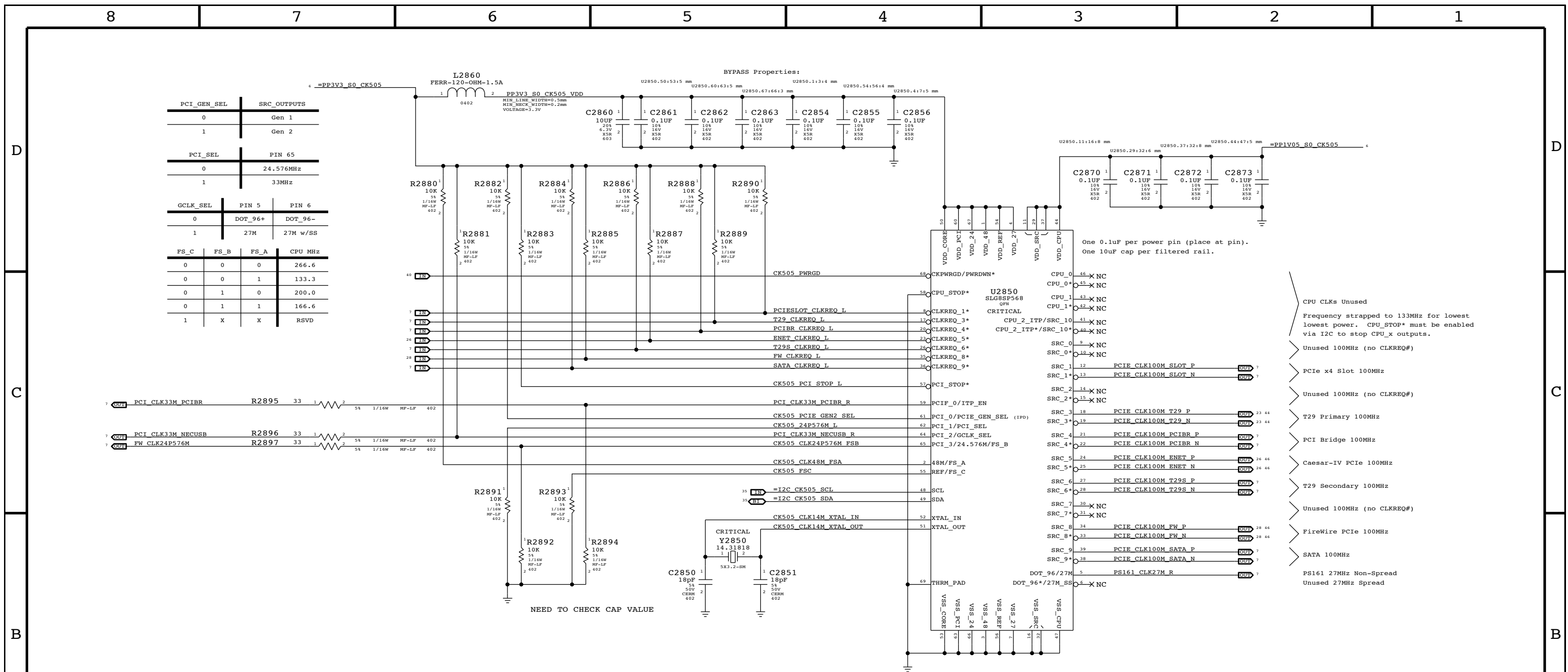
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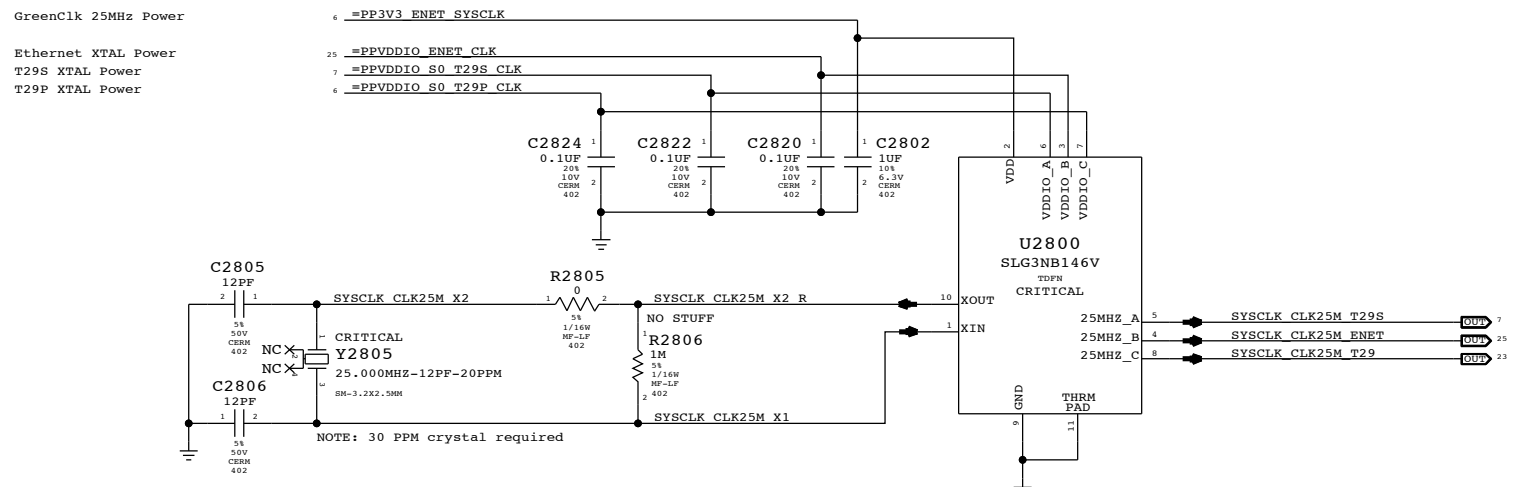
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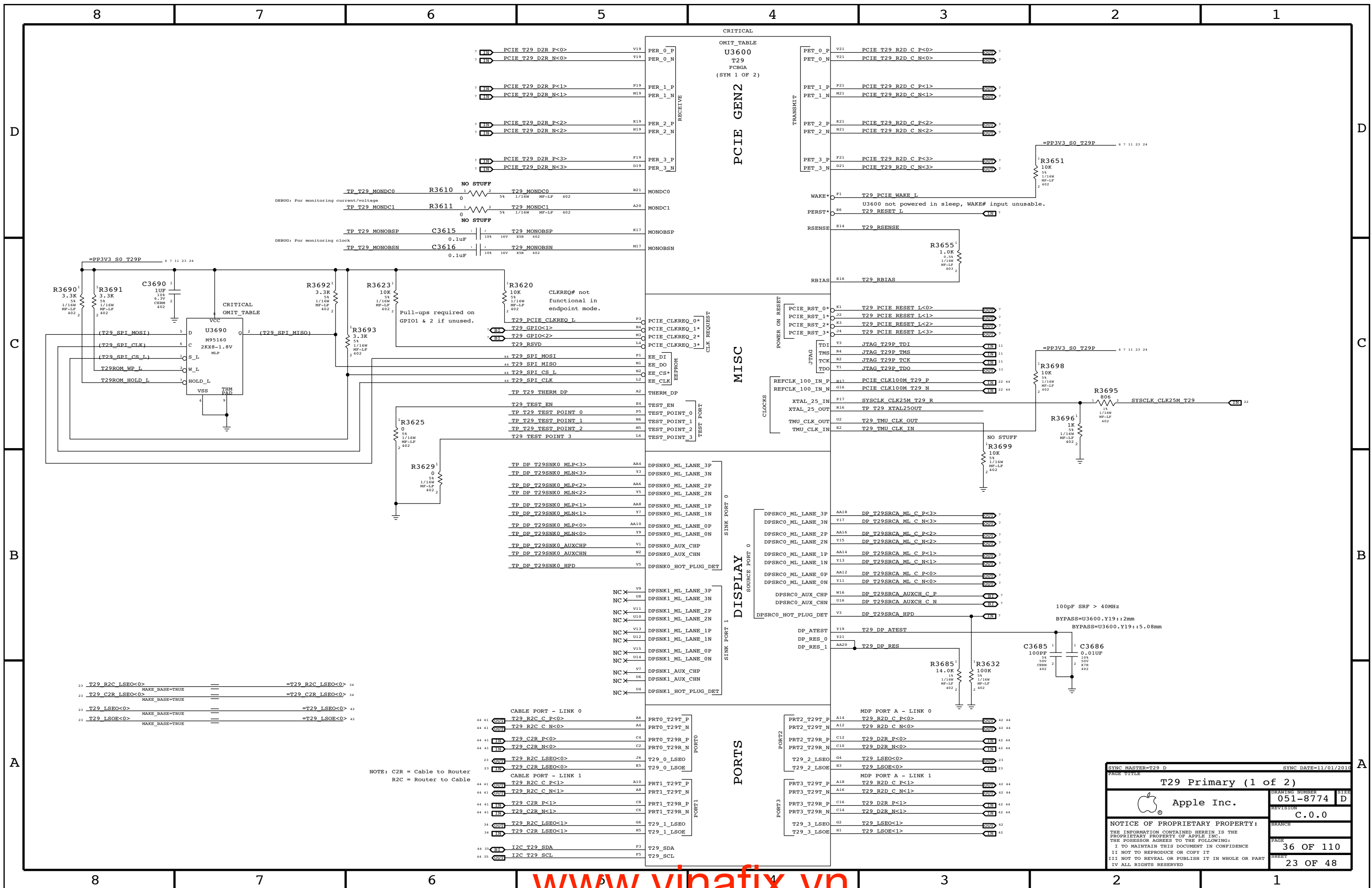
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DP FC & INTERFACE			
		DRAWING NUMBER	051-8774
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System 25MHz Clock Generator



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T29 Clocking		DRAWING NUMBER	SIZE
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CRITICAL
 OMIT_TABLE
 U3600
 T29
 PCBGA
 (SYM 1 OF 2)

PCIE GEN2

MISC

DISPLAY

PORTS

DEBUG: For monitoring current/voltage
 TP T29 MONDC0 R3610 NO STUFF
 TP T29 MONDC1 R3611 NO STUFF
 DEBUG: For monitoring clock
 TP T29 MONOBSP C3615 NO STUFF
 TP T29 MONOBSN C3616 NO STUFF

CRITICAL
 OMIT_TABLE
 U3690
 M95160
 2KX8-1.8V
 M.L.P.
 Pull-ups required on
 GPIO1 & 2 if unused.
 CLKREQ# not
 functional in
 endpoint mode.

T29 PCIE CLKREQ L
 T29 GPIO<1>
 T29 GPIO<2>
 T29 RSVD
 T29 SPI MOSI
 T29 SPI MISO
 T29 SPI CS L
 T29 SPI CLK
 T29 THERM DP
 T29 TEST EN
 TP T29 TEST POINT 0
 TP T29 TEST POINT 1
 TP T29 TEST POINT 2
 TP T29 TEST POINT 3

TP DP T29SNK0 MLP<3>
 TP DP T29SNK0 MLN<3>
 TP DP T29SNK0 MLP<2>
 TP DP T29SNK0 MLN<2>
 TP DP T29SNK0 MLP<1>
 TP DP T29SNK0 MLN<1>
 TP DP T29SNK0 MLP<0>
 TP DP T29SNK0 MLN<0>
 TP DP T29SNK0 AUXCHP
 TP DP T29SNK0 AUXCHN
 TP DP T29SNK0 HPD

DPSNK0_ML_LANE_3P
 DPSNK0_ML_LANE_3N
 DPSNK0_ML_LANE_2P
 DPSNK0_ML_LANE_2N
 DPSNK0_ML_LANE_1P
 DPSNK0_ML_LANE_1N
 DPSNK0_ML_LANE_0P
 DPSNK0_ML_LANE_0N
 DPSNK0_AUX_CHP
 DPSNK0_AUX_CHN
 DPSNK0_HOT_PLUG_DET

CABLE PORT - LINK 0
 T29 R2C P<0>
 T29 R2C C N<0>
 T29 C2R P<0>
 T29 C2R N<0>
 T29 R2C LSEO<0>
 T29 C2R LSEO<0>
 T29_0_LSEO
 T29_0_LSOE
 CABLE PORT - LINK 1
 T29 R2C P<1>
 T29 R2C C N<1>
 T29 C2R P<1>
 T29 C2R N<1>
 T29 R2C LSEO<1>
 T29 C2R LSEO<1>
 T29_1_LSEO
 T29_1_LSOE
 I2C T29 SDA
 I2C T29 SCL

NOTE: C2R = Cable to Router
 R2C = Router to Cable

SYNC MASTER=T29 D SYNC DATE=11/01/2011

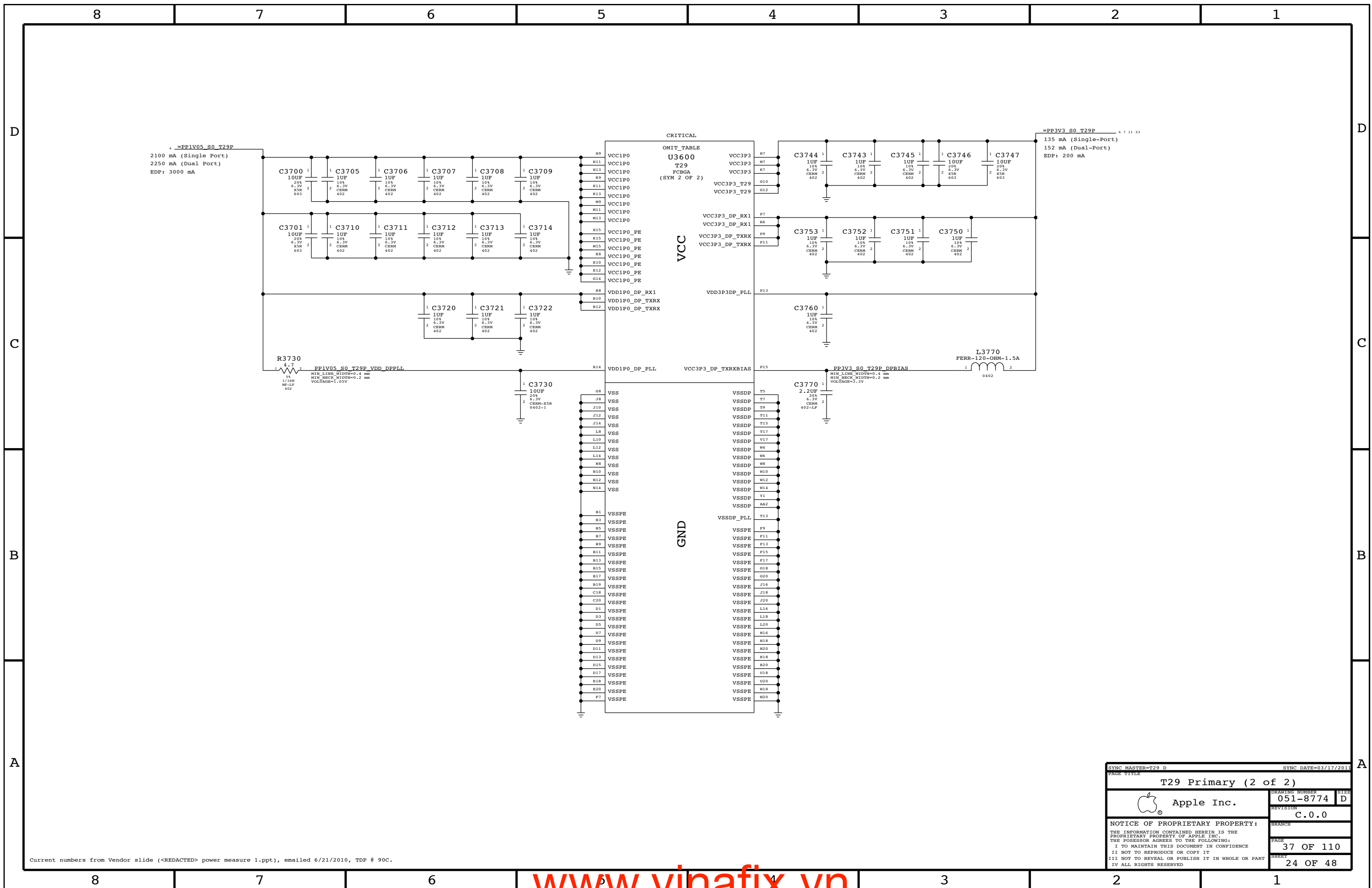
T29 Primary (1 of 2)

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PP3V3 S0 T29P
 135 mA (Single-Port)
 152 mA (Dual-Port)
 EDP: 200 mA

R3730
 PP3V3 S0 T29P VDD DEPLL
 MIN_LINE_WIDTH=0.4 mm
 MIN_NECK_WIDTH=0.2 mm
 VOLTAGE=1.05V

PP3V3 S0 T29P
 135 mA (Single-Port)
 152 mA (Dual-Port)
 EDP: 200 mA

PP3V3 S0 T29P DEBIAS
 MIN_LINE_WIDTH=0.4 mm
 MIN_NECK_WIDTH=0.2 mm
 VOLTAGE=3.3V

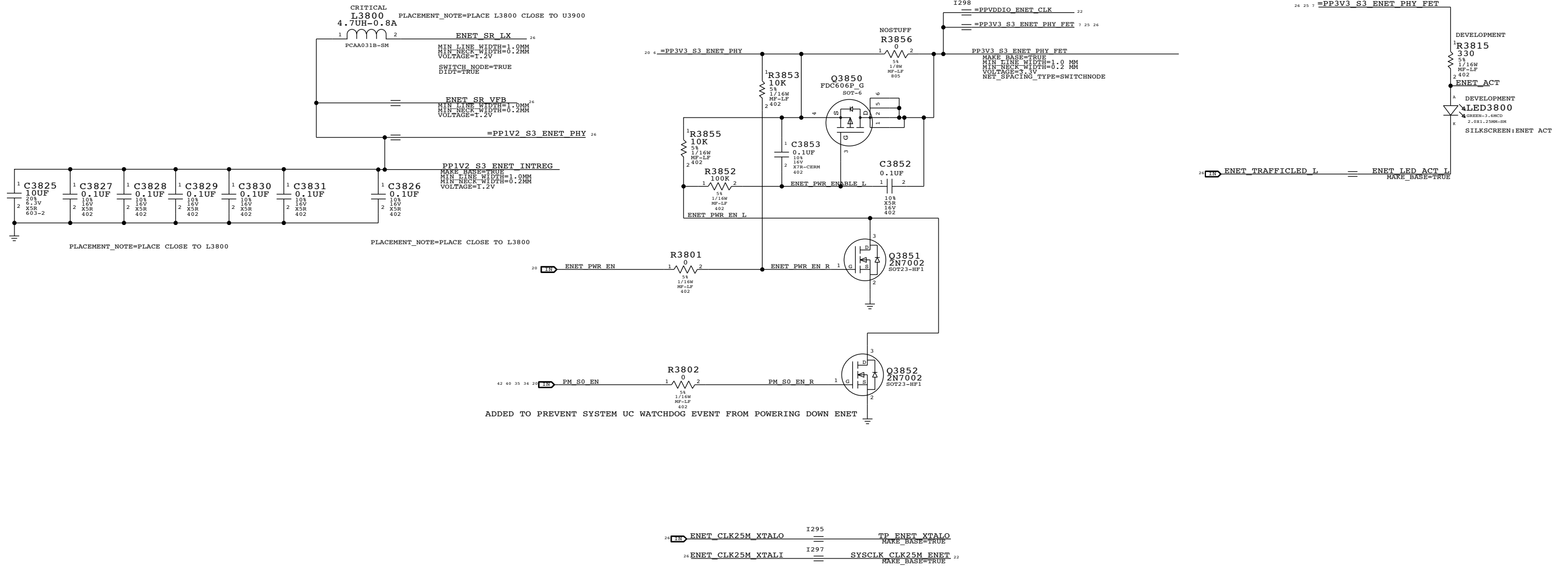
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PAGE TITLE			
T29 Primary (2 of 2)			
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Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

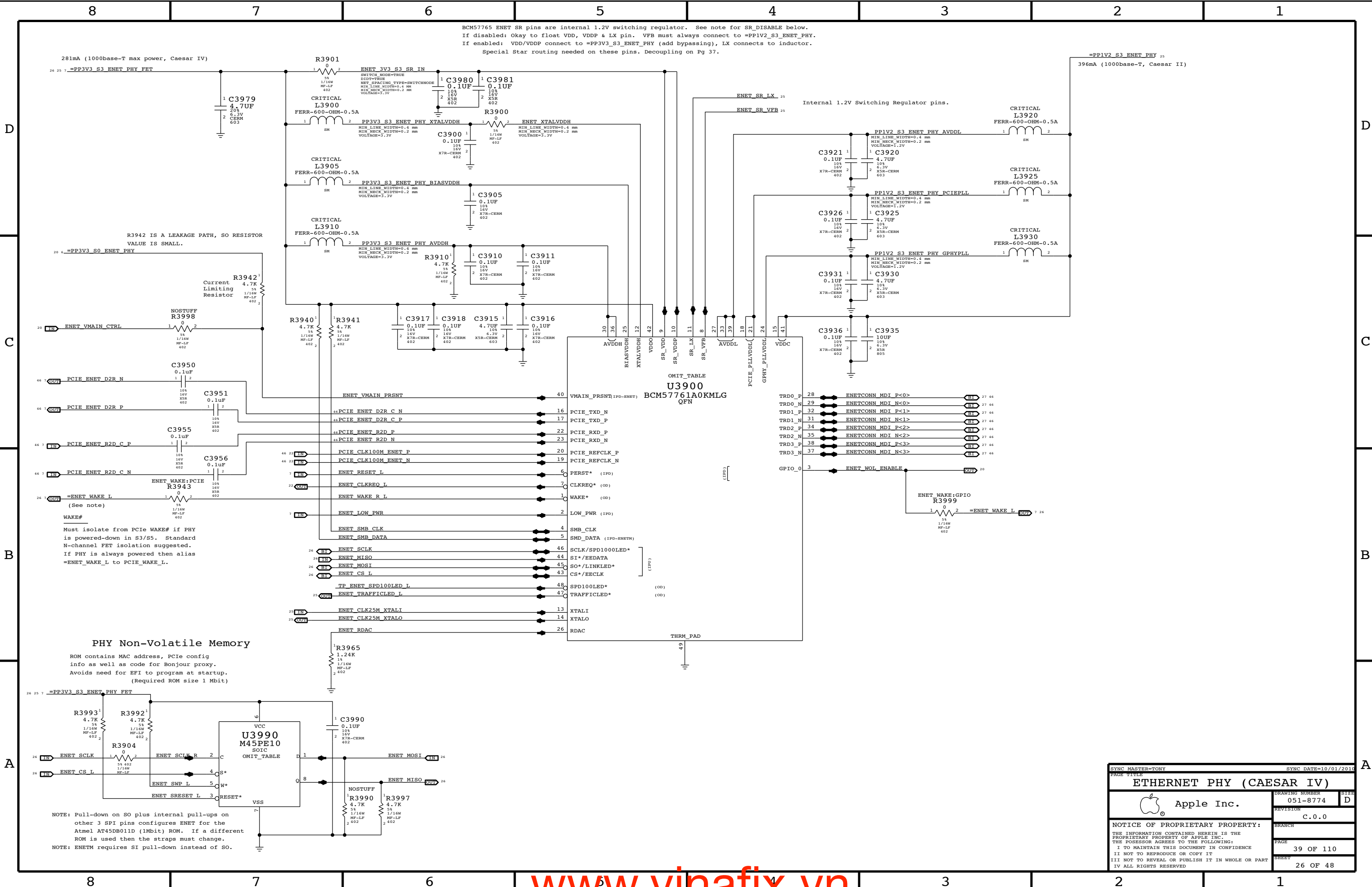
CAESAR IV 1.2V INT.VR CMPTS

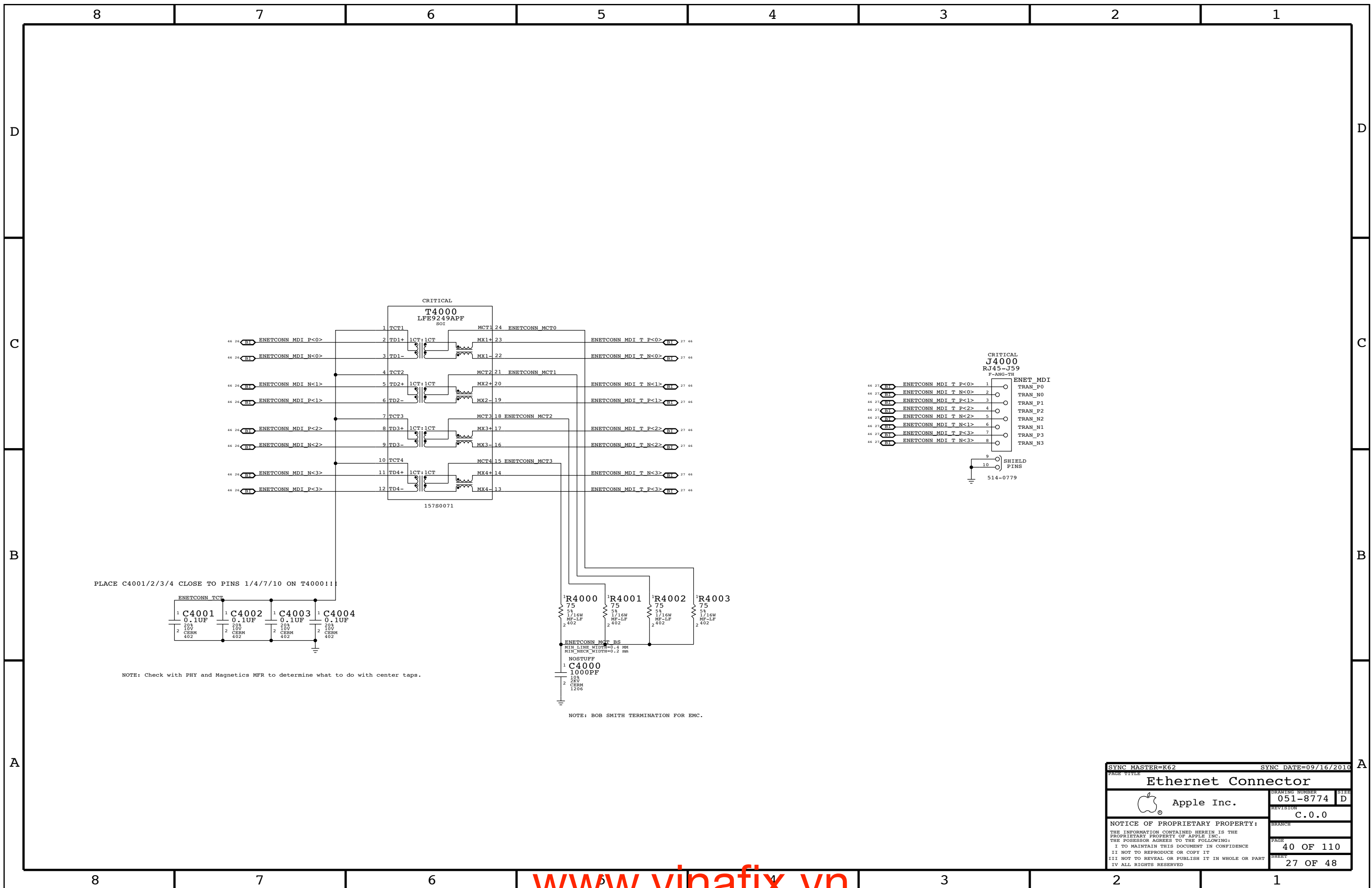
CAESAR IV POWER ENABLE CIRCUIT

CAESAR IV ACTIVITY LED

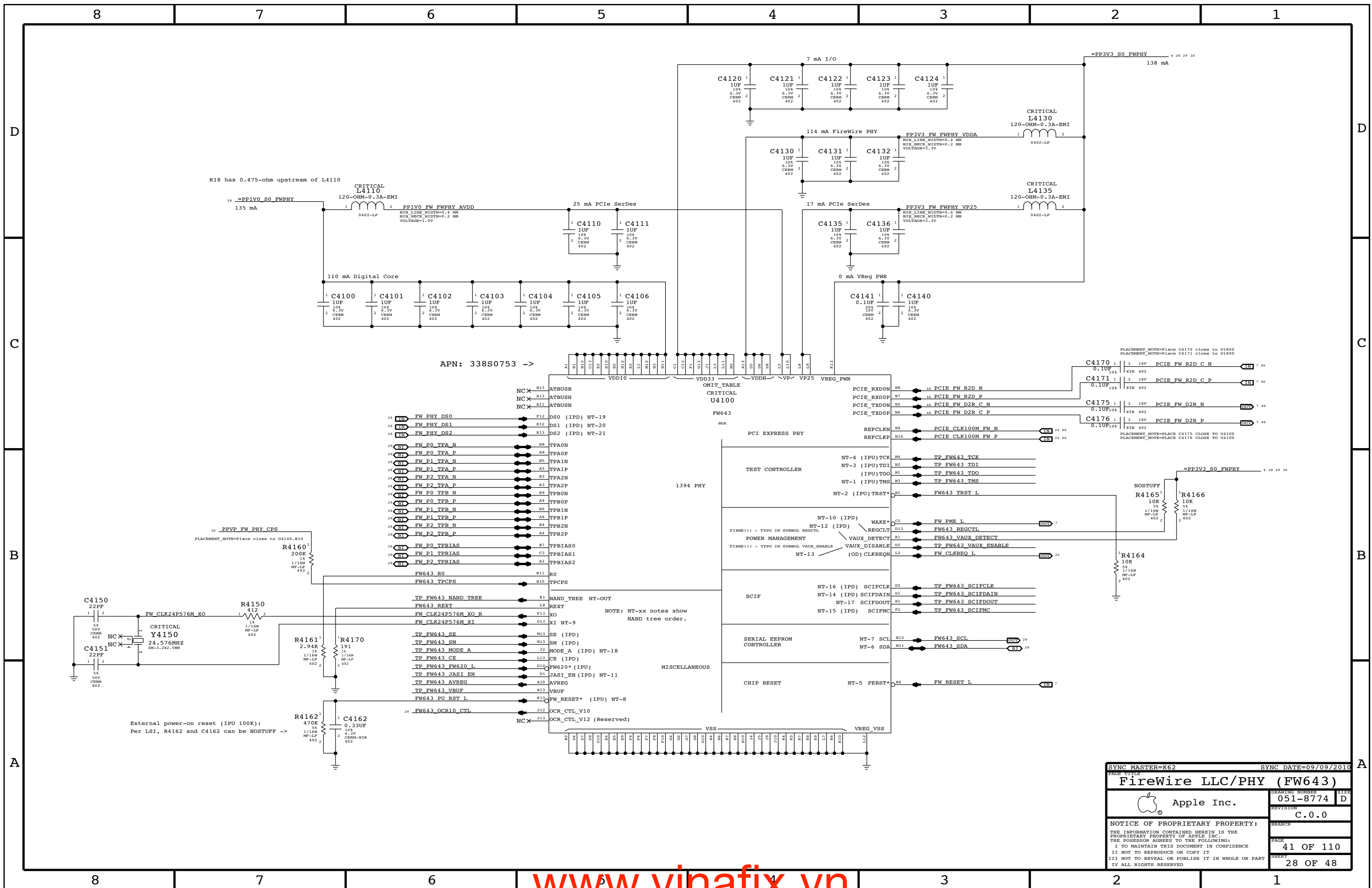


SYNC MASTER=K62		SYNC DATE=09/16/2010	
CAESAR IV SUPPORT			
	DRAWING NUMBER	051-8774	SIZE
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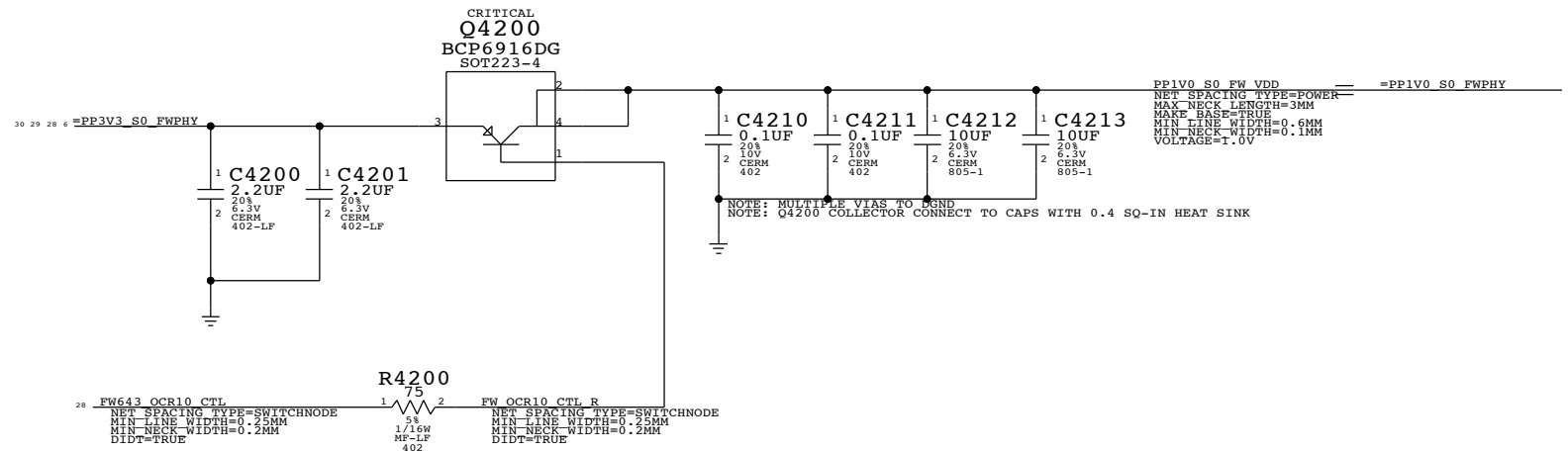


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Ethernet Connector				DRAWING NUMBER	SIZE
Apple Inc.				051-8774	D
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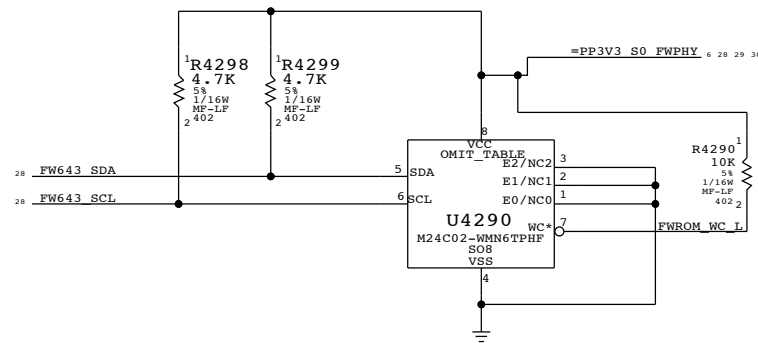


SYNC MASTER=K62		SYNC DATE=09/09/2010	
PAGE TITLE			
FireWire LLC/PHY (FW643)			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8774	D
		REVISION	
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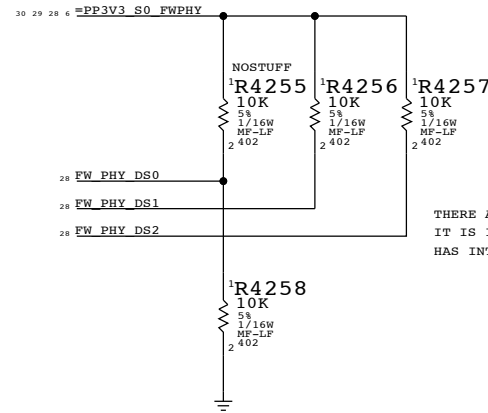
FW643 1.0V GENERATION



FW643 GUID ROM

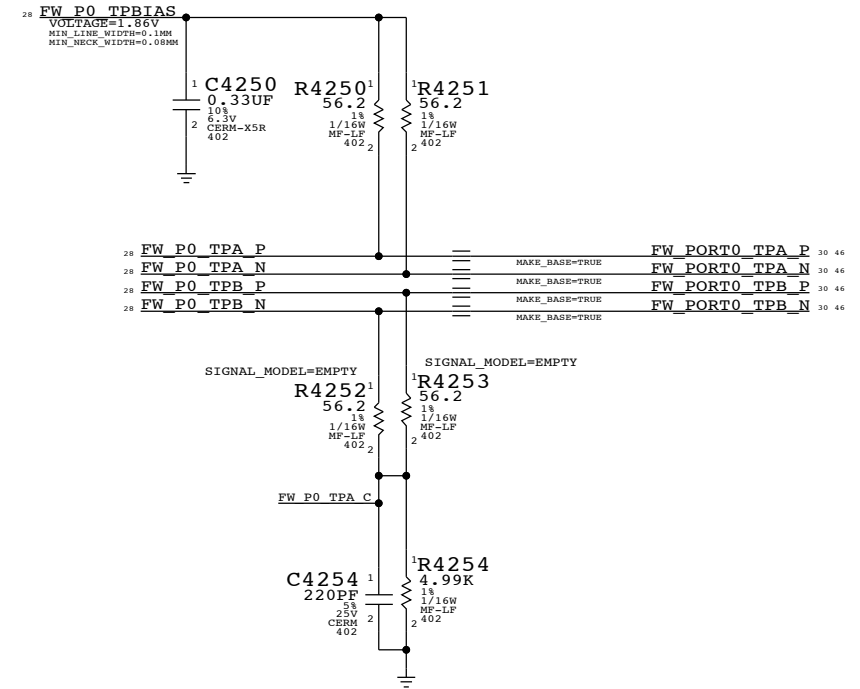


1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED. NO STUFF MEANS THAT IT IS IN BILINGUAL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

Termination
Place close to FireWire PHY

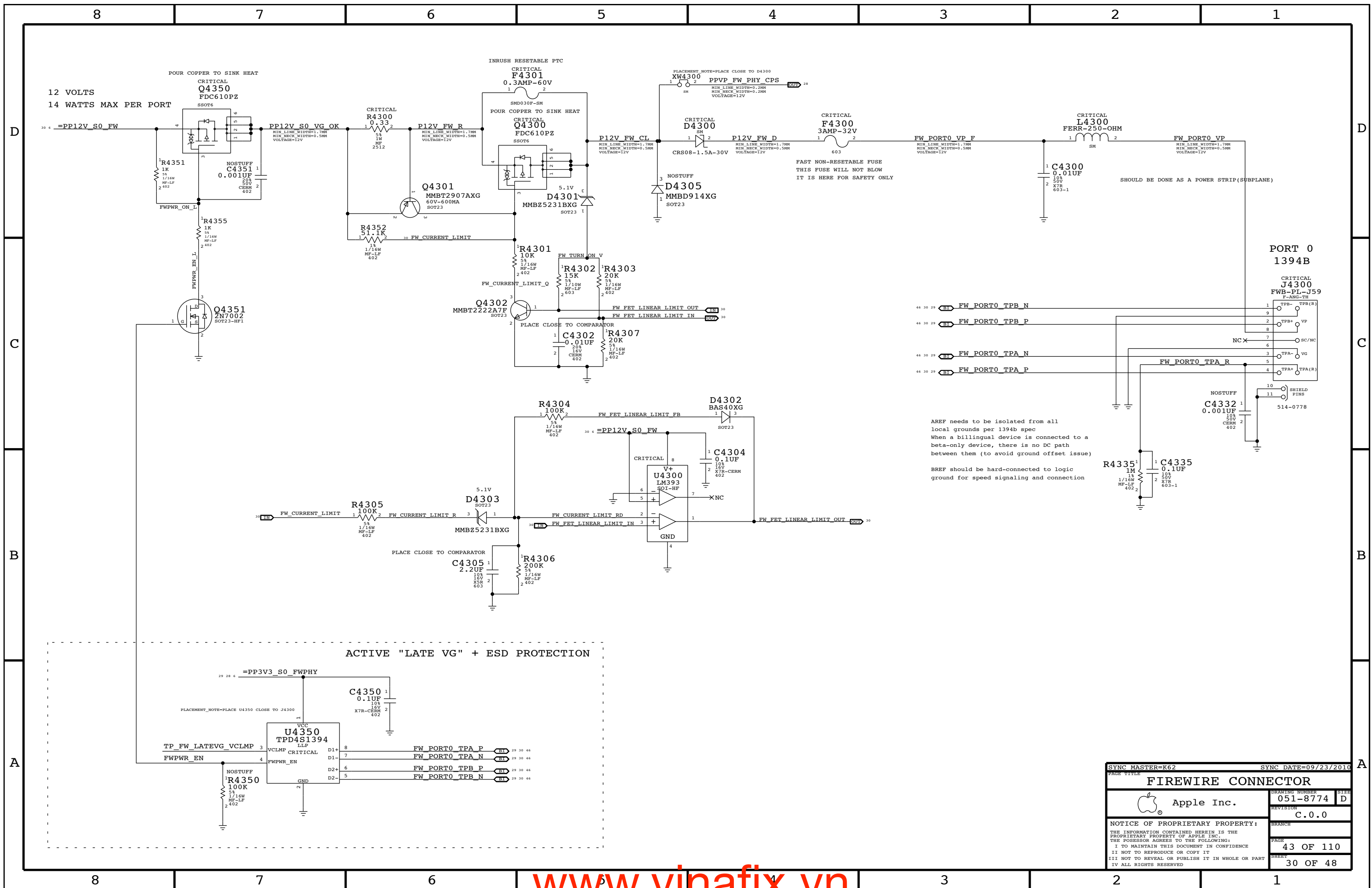


2ND & 3RD TPA/TPB PAIR UNUSED

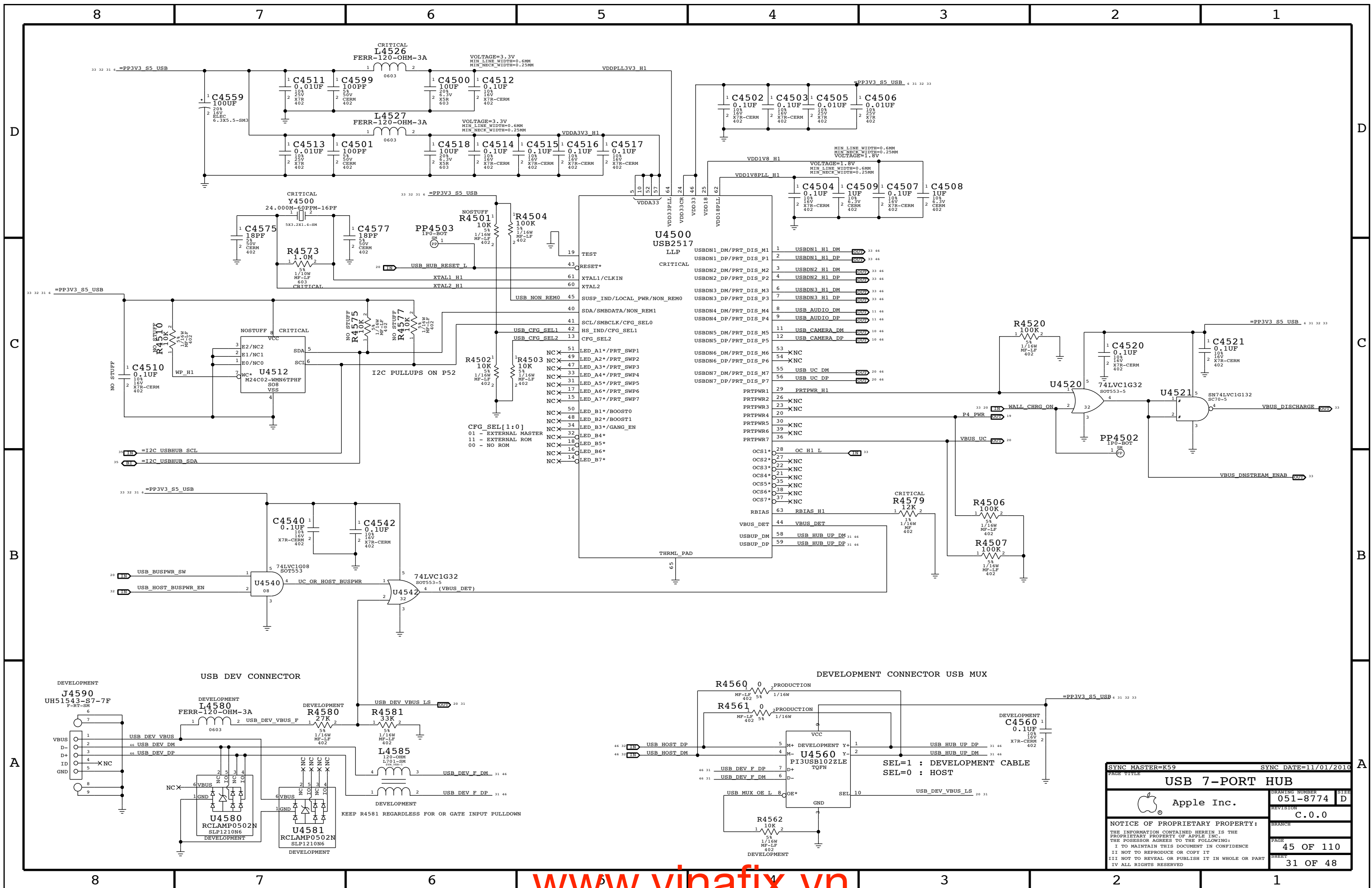
- FW_P1_TPBias == NC_FW_PORT1_TPBias
- FW_P1_TPA_P == NC_FW_PORT1_TPA_P
- FW_P1_TPA_N == NC_FW_PORT1_TPA_N
- FW_P1_TPB_P == NC_FW_PORT1_TPB_P
- FW_P1_TPB_N == NC_FW_PORT1_TPB_N
- FW_P2_TPBias == NC_FW_PORT2_TPBias
- FW_P2_TPA_P == NC_FW_PORT2_TPA_P
- FW_P2_TPA_N == NC_FW_PORT2_TPA_N
- FW_P2_TPB_P == NC_FW_PORT2_TPB_P
- FW_P2_TPB_N == NC_FW_PORT2_TPB_N

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

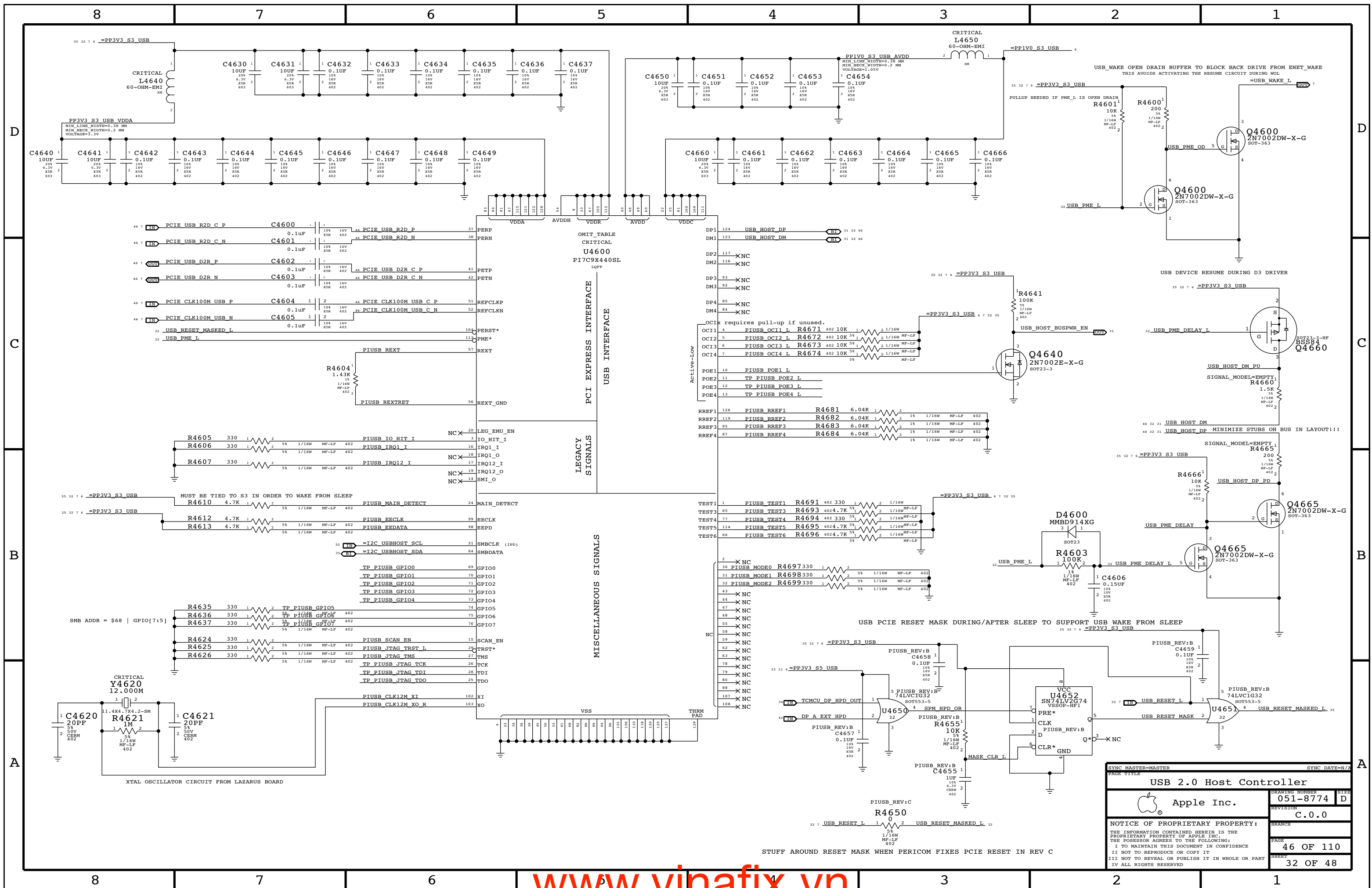
SYNC MASTER=K62		SYNC DATE=09/23/2010	
PAGE TITLE FireWire: 1394B MISC			
DRAWING NUMBER 051-8774		SIZE D	
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FIREWIRE CONNECTOR			DRAWING NUMBER	051-8774	SIZE
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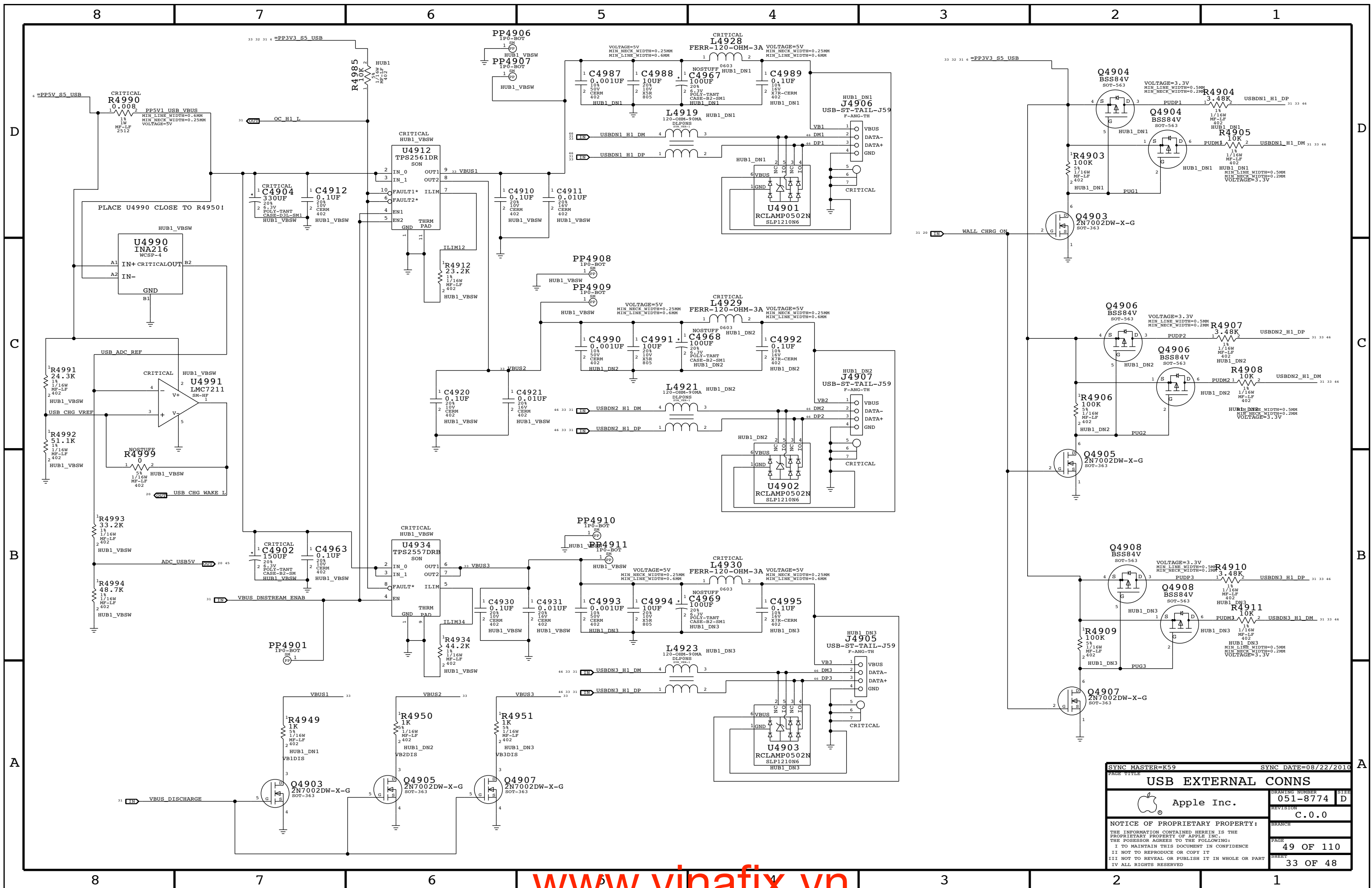


SYNC MASTER=K59		SYNC DATE=11/01/2010	
USB 7-PORT HUB			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8774	D
		REVISION	
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		SHEET	31 OF 48
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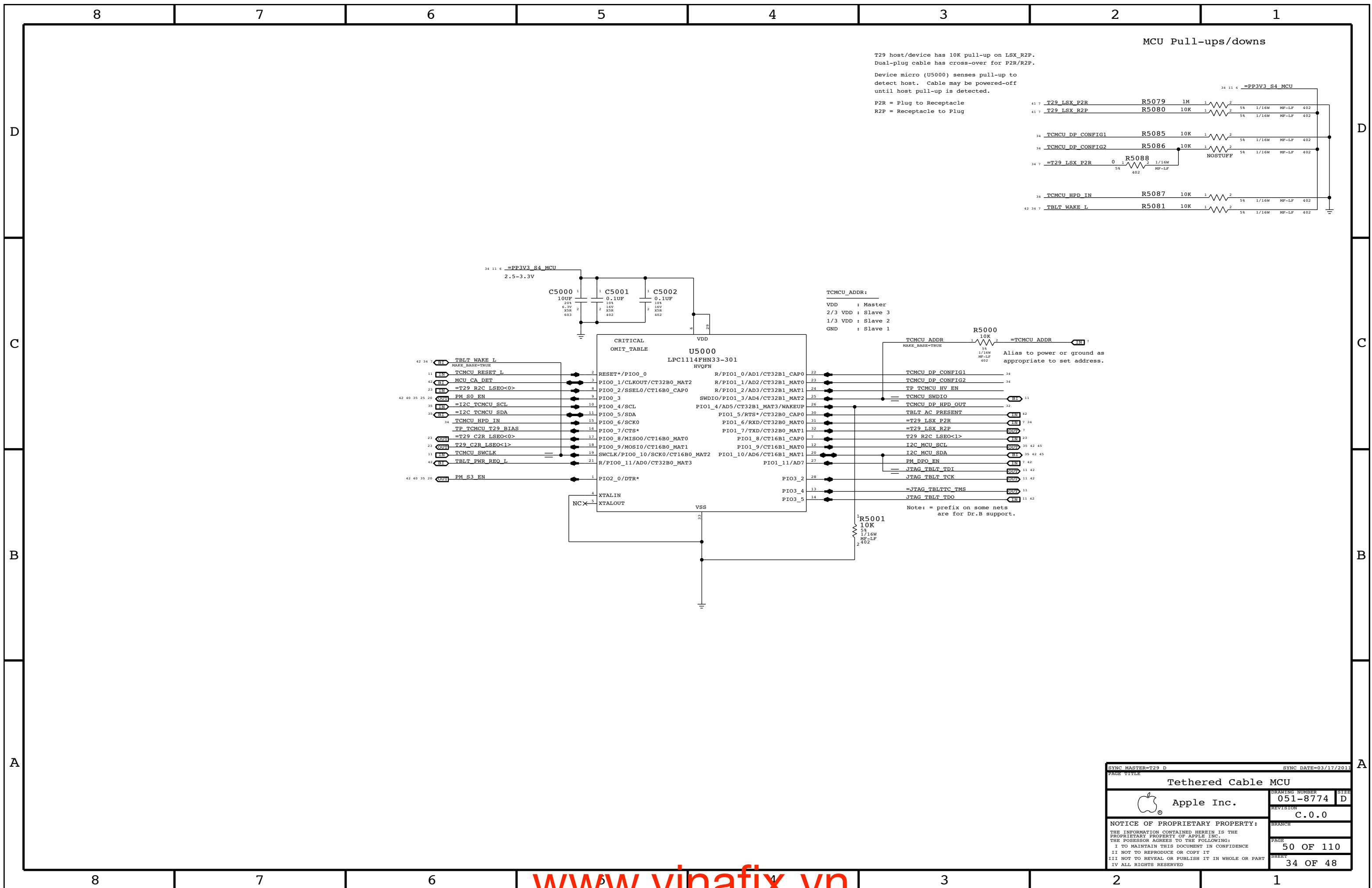


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PAGE TITLE			
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		REVISION	
		C.0.0	
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STUFF AROUND RESET MASK WHEN PERICOM FIXES PCIE RESET IN REV C

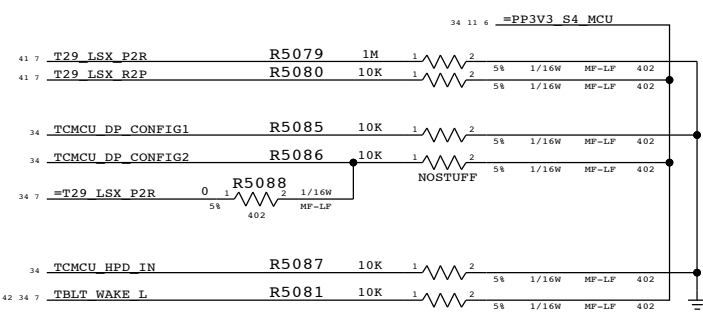


SYNC MASTER=K59		SYNC DATE=08/22/2010	
PAGE TITLE			
USB EXTERNAL CONNS			
Apple Inc.		DRAWING NUMBER	051-8774
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T29 host/device has 10K pull-up on LSX_R2P.
 Dual-plug cable has cross-over for P2R/R2P.
 Device micro (U5000) senses pull-up to
 detect host. Cable may be powered-off
 until host pull-up is detected.
 P2R = Plug to Receptacle
 R2P = Receptacle to Plug

MCU Pull-ups/downs



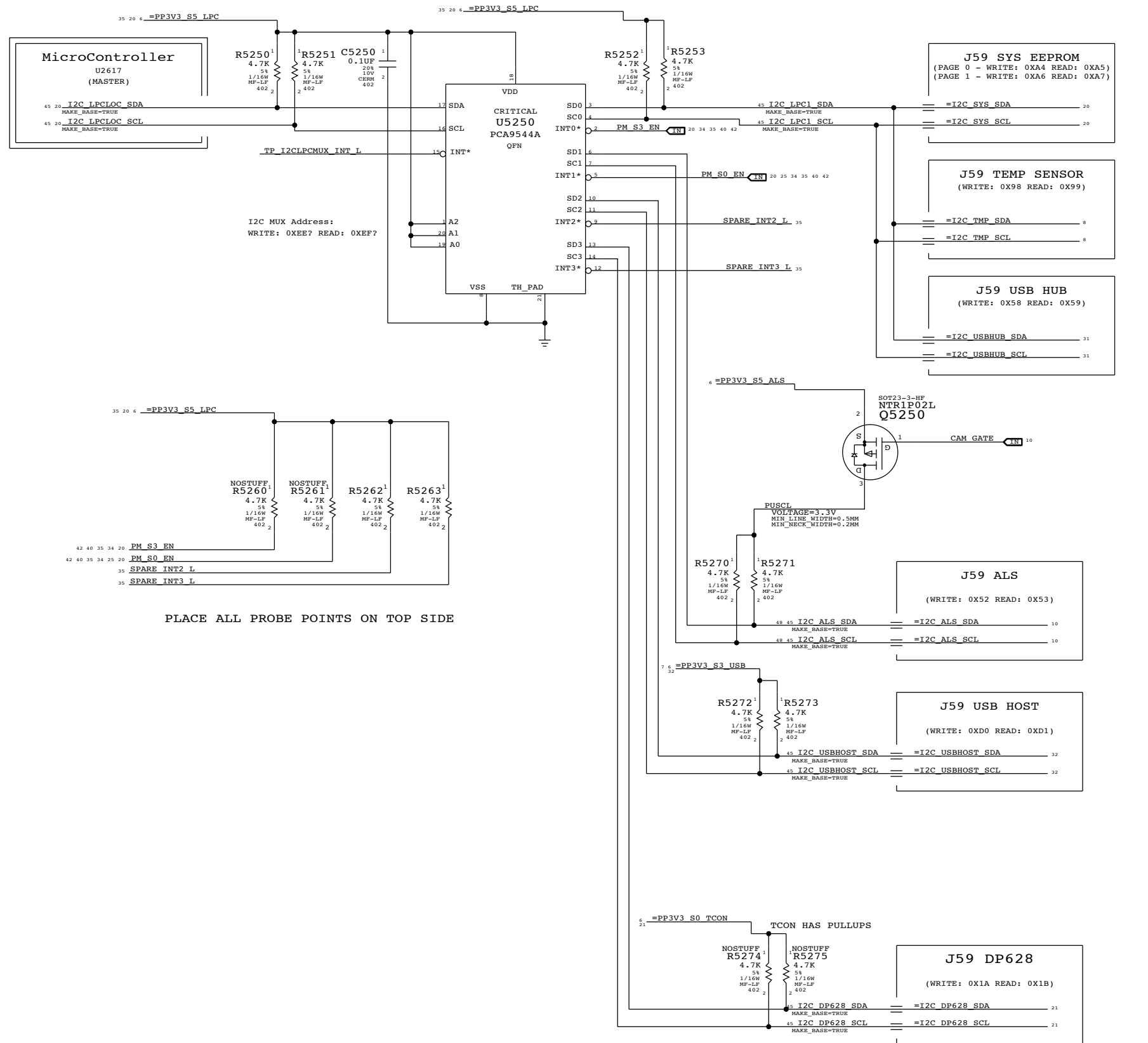
TCMCU_ADDR:
 VDD : Master
 2/3 VDD : Slave 3
 1/3 VDD : Slave 2
 GND : Slave 1

R5000
 MAKE_BASE=TRUE
 Alias to power or ground as
 appropriate to set address.

Note: = prefix on some nets
 are for Dr.B support.

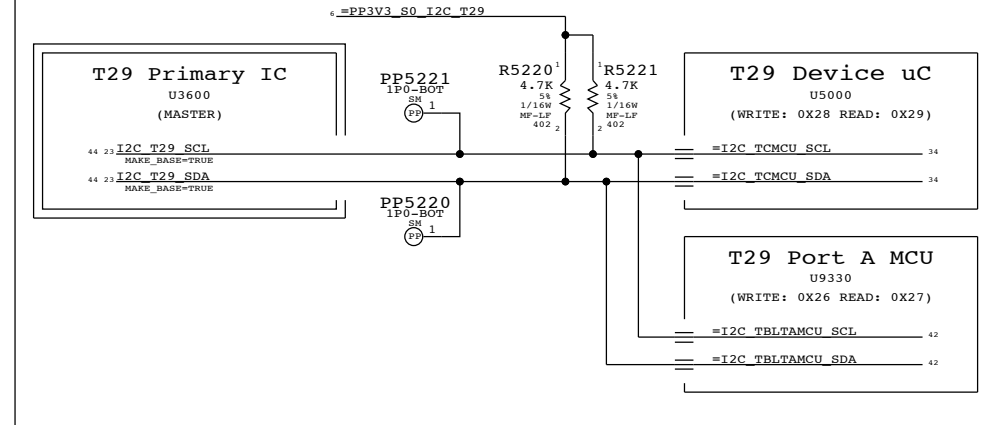
SYNC MASTER=T29 D		SYNC DATE=03/17/2011	
Tethered Cable MCU			
Apple Inc.		DRAWING NUMBER	051-8774
		REVISION	C.0.0
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LPC I2C CONNECTIONS



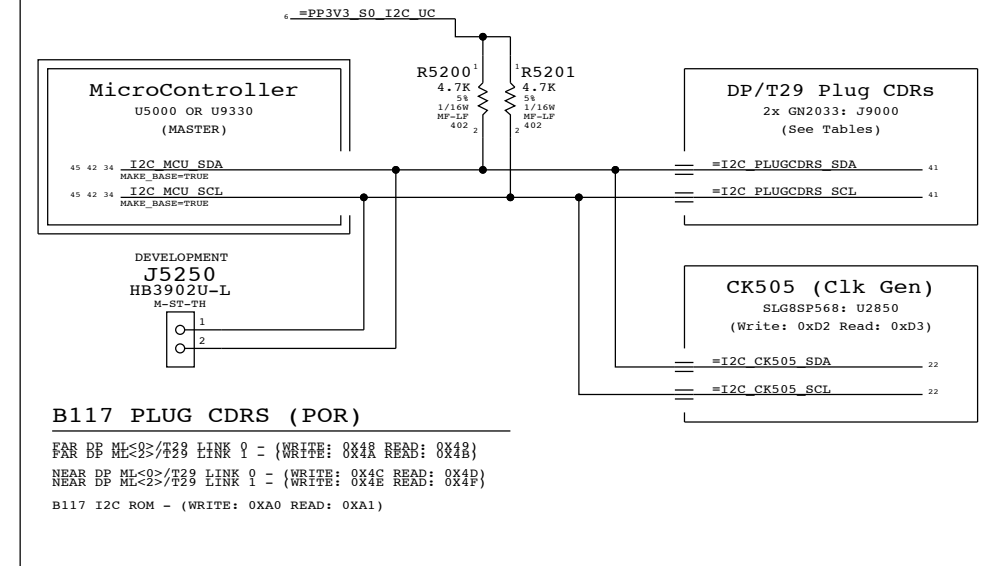
PLACE ALL PROBE POINTS ON TOP SIDE

T29 IC I2C Connections

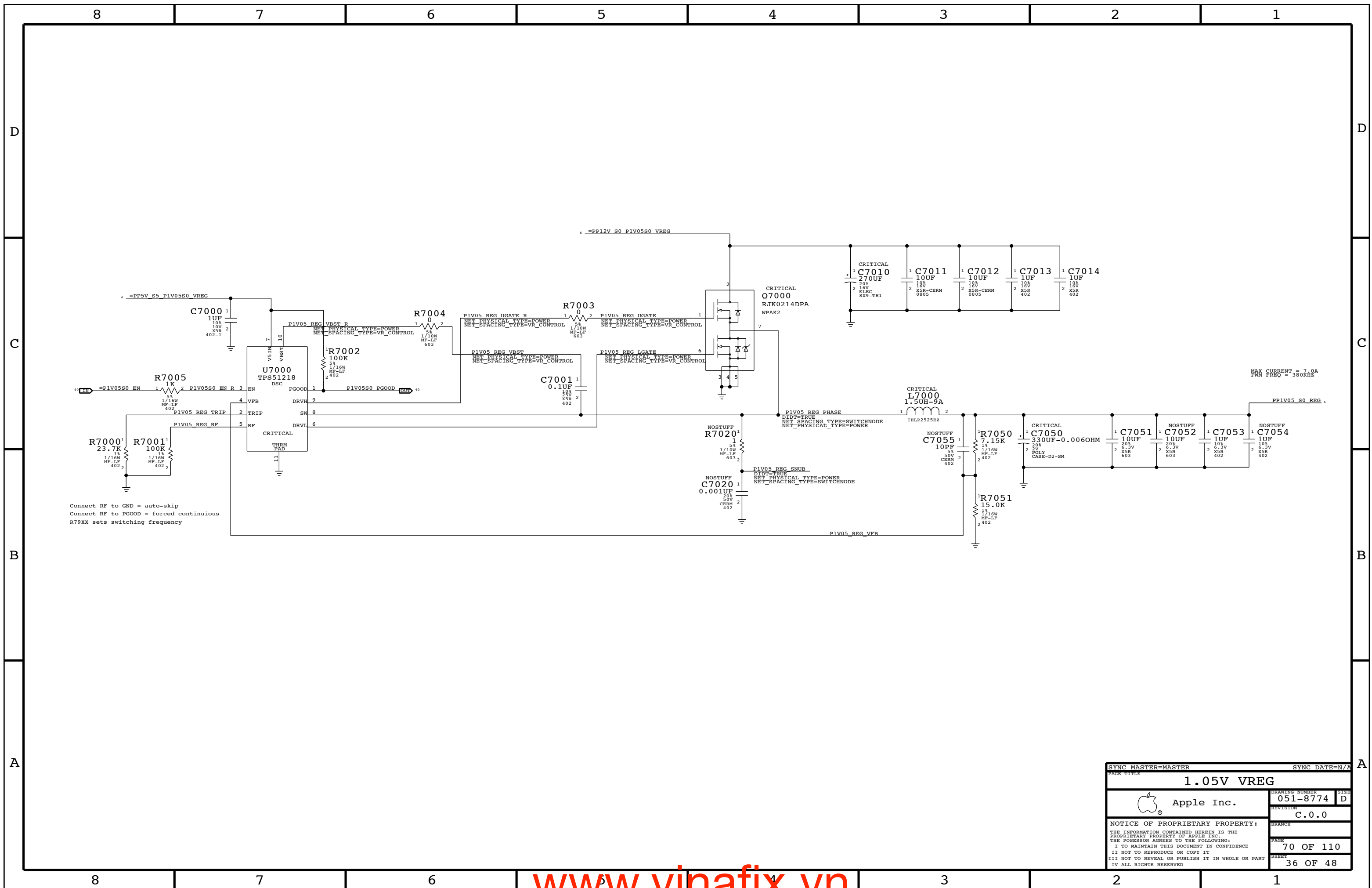


PLACE ALL I2C PROBE POINTS ON TOP SIDE

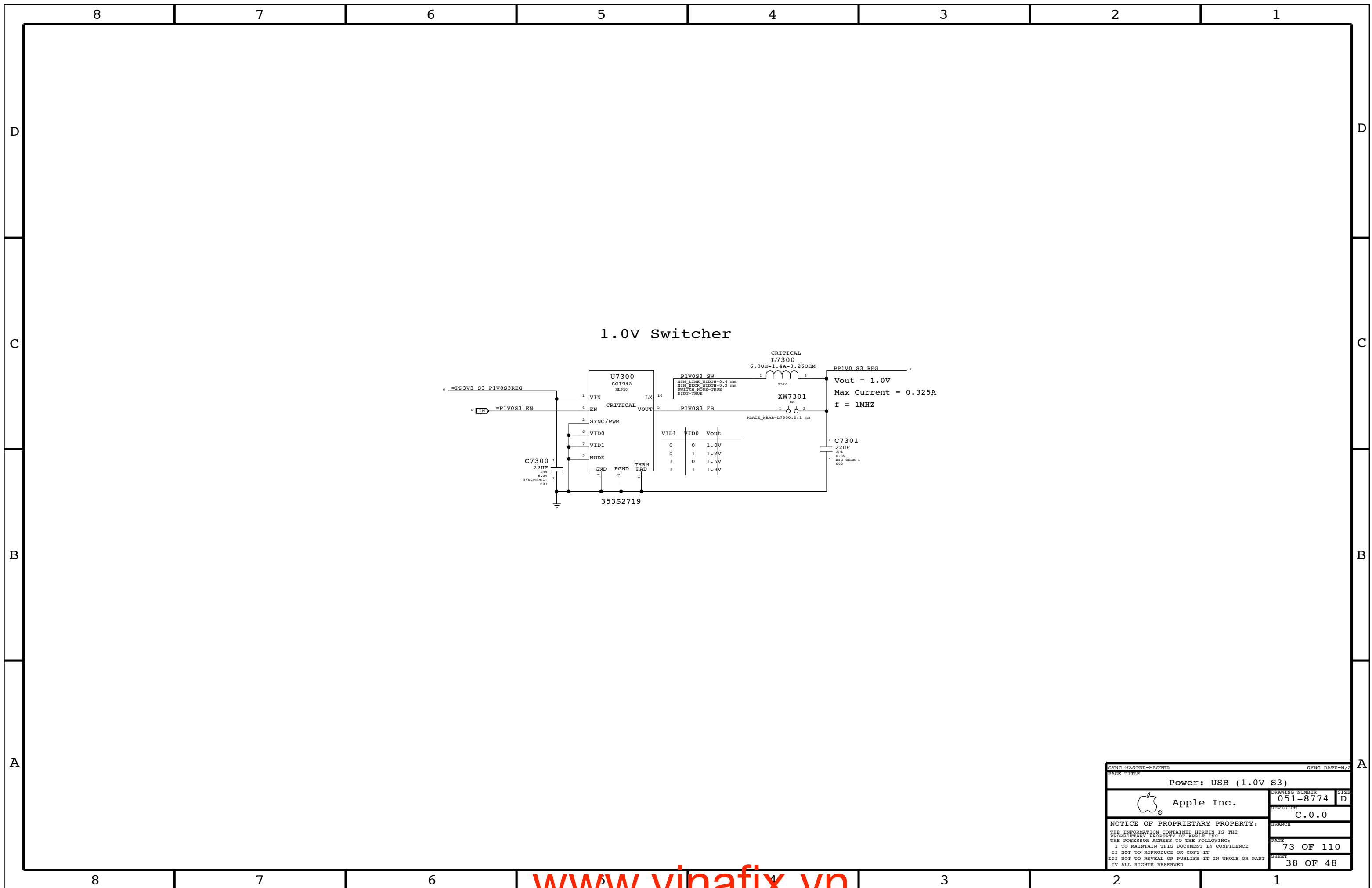
T29 MCU I2C CONNECTIONS



SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE J59 & T29 SMBUS CONNECTIONS			
DRAWING NUMBER 051-8774		SIZE D	
REVISION C.0.0		BRANCH	
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SYNC MASTER=MASTER		SYNC DATE=N/A	
1.05V VREG			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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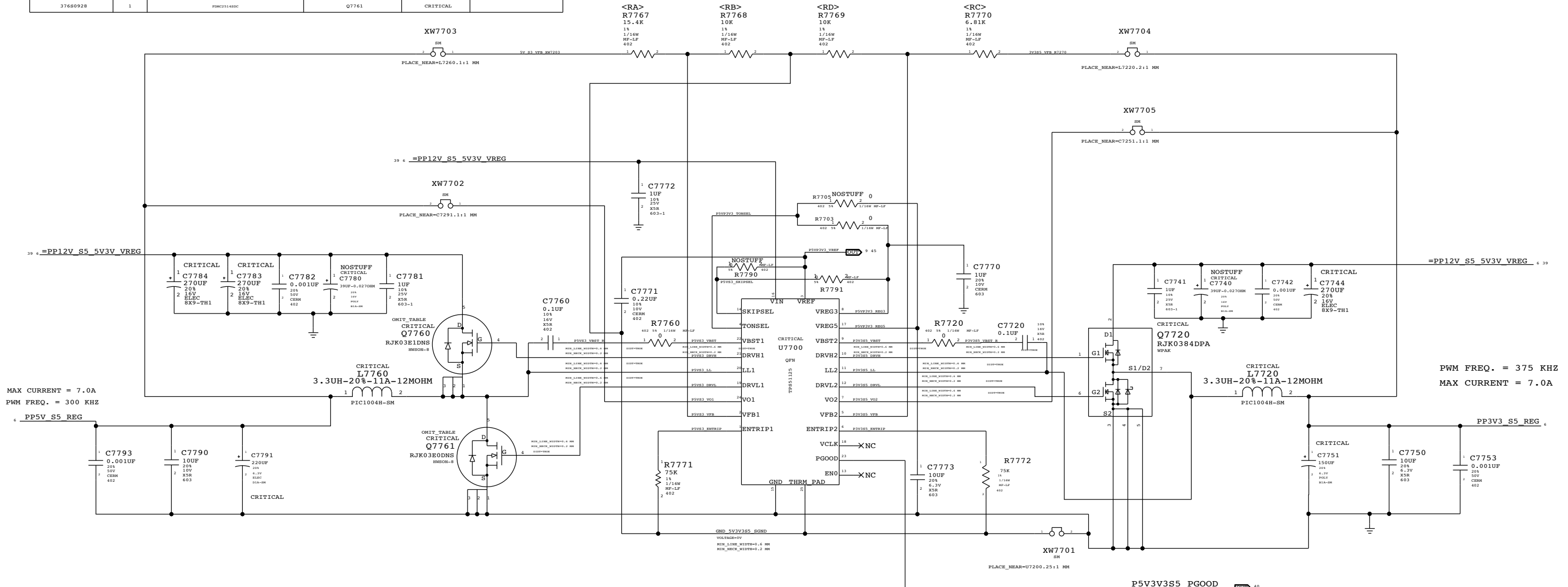
SYNC MASTER=MASTER		SYNC DATE=N/A	
Power: USB (1.0V S3)			
Apple Inc.	DRAWING NUMBER	051-8774	
	REVISION	C.0.0	
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5V_S3/3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
37680927	1	F0M03100C	Q7760	CRITICAL	
37680928	1	F0M031450C	Q7761	CRITICAL	

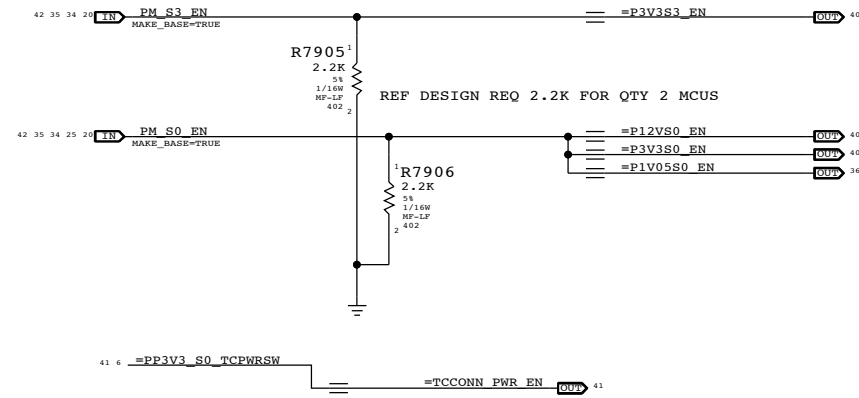


MAX CURRENT = 7.0A
PWM FREQ. = 300 KHZ

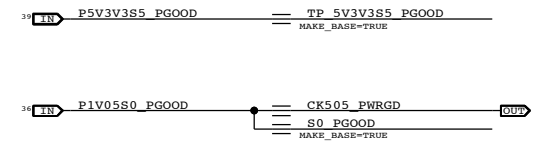
PWM FREQ. = 375 KHZ
MAX CURRENT = 7.0A

5V/3.3V SUPPLY	
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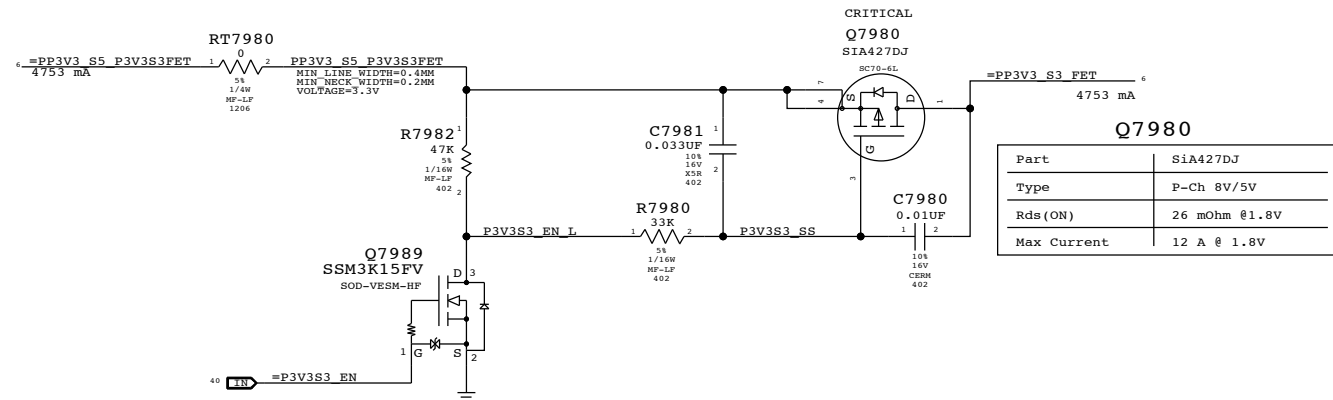
T29 / Device Rails



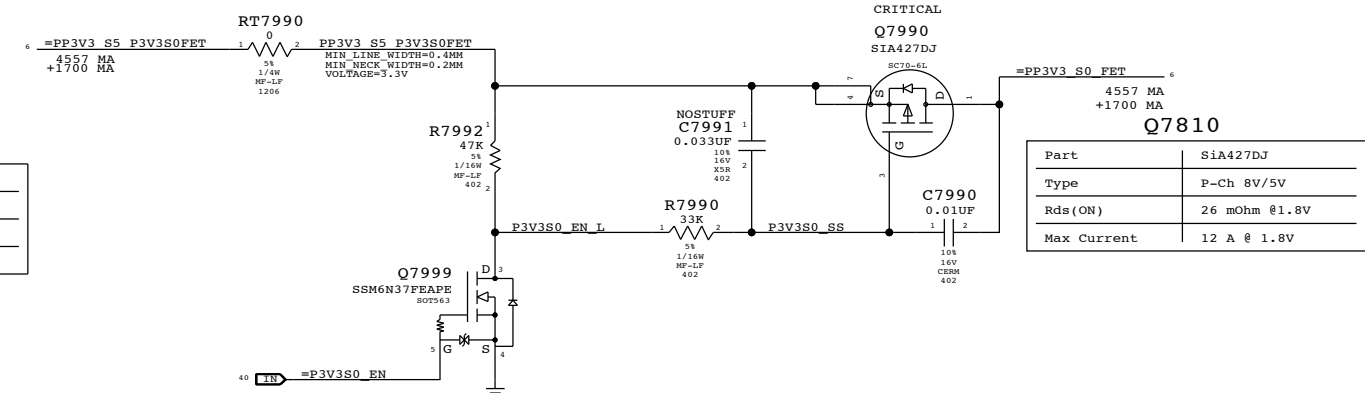
Power Goods



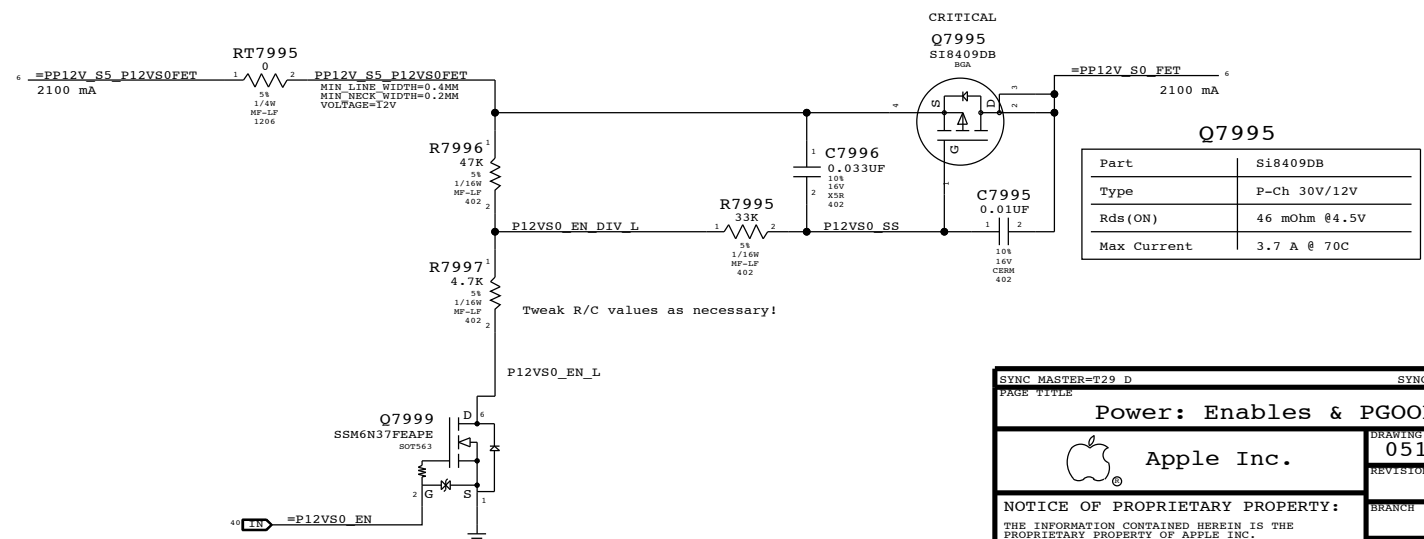
3.3V S3 FET



3.3V S0 FET

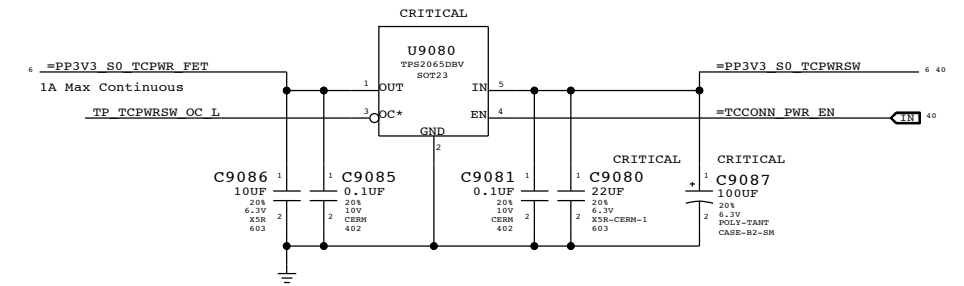


12V S0 FET

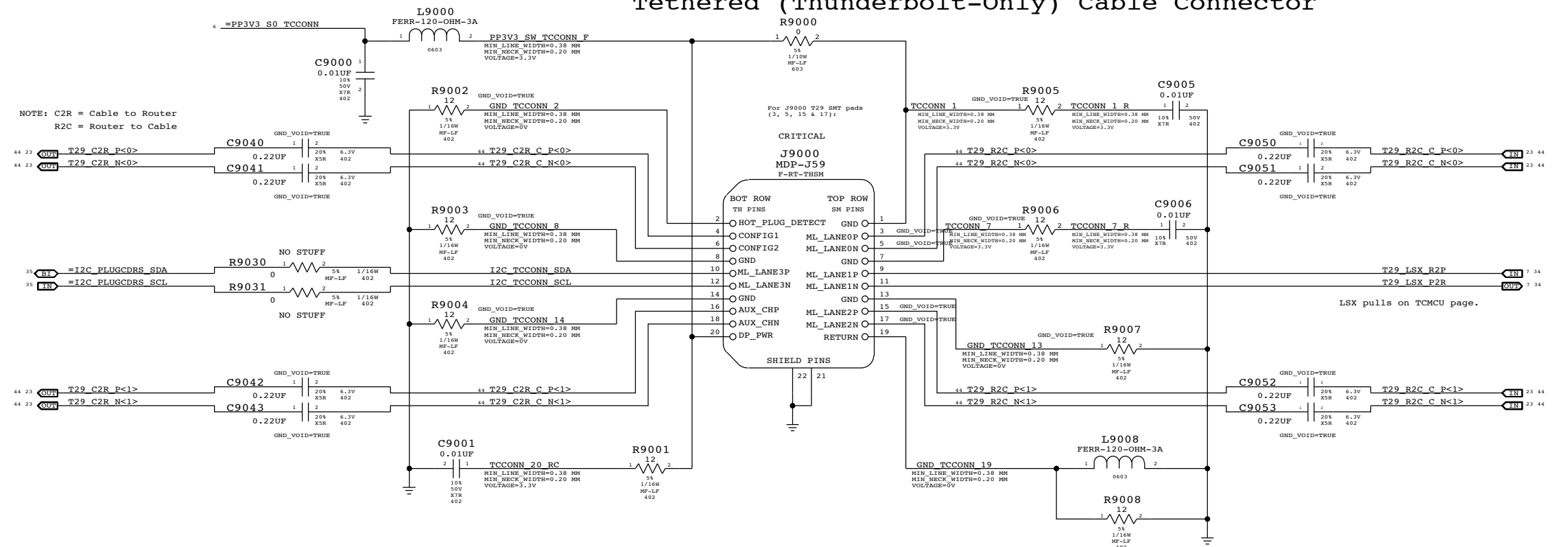


SYNC MASTER=T29 D		SYNC DATE=09/30/2010	
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Power: Enables & PGOOD			
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Cable 3.3V Power Switch



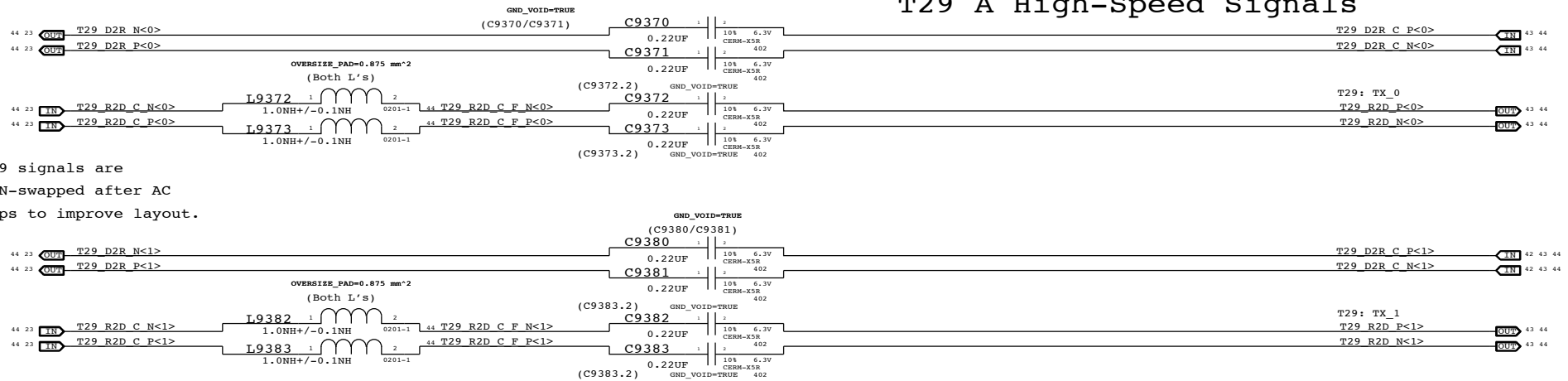
Tethered (Thunderbolt-Only) Cable Connector



SYNC MASTER=T29 D		SYNC DATE=03/17/2011	
PAGE TITLE			
Tethered Cable Connector			
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T29 A High-Speed Signals

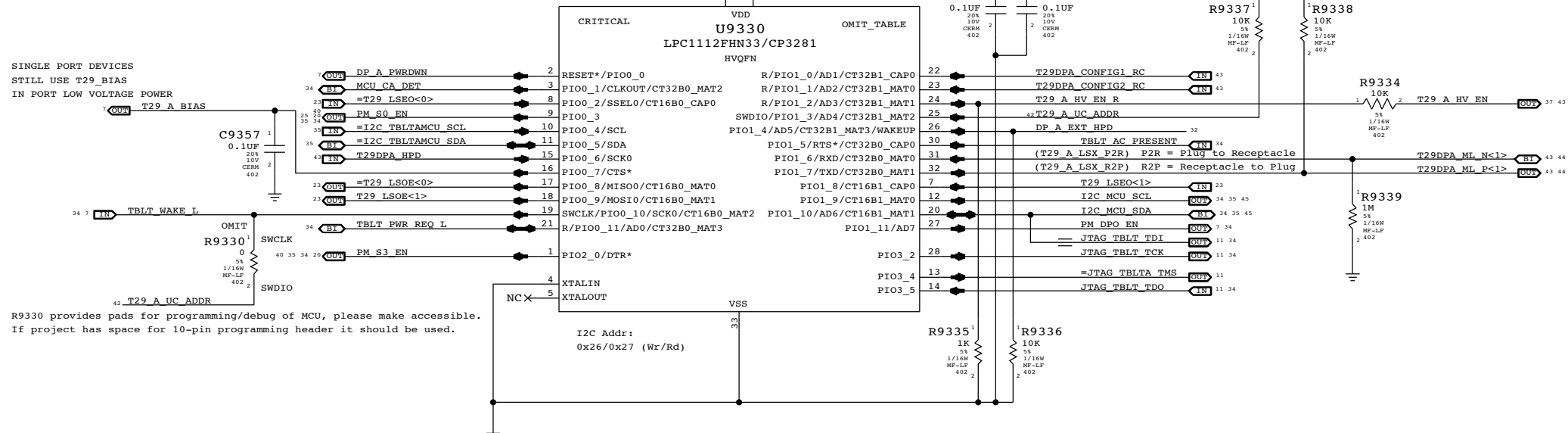
T29 signals are P/N-swapped after AC caps to improve layout.



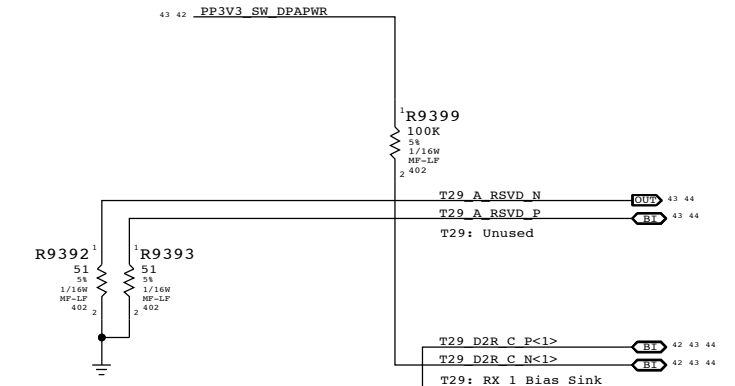
Port A MCU

43 42 PP3V3 SW DPAPWR Must be 3.3V DP A port power

SINGLE PORT DEVICES STILL USE T29_BIAS IN PORT LOW VOLTAGE POWER



R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.



SYNC MASTER=T29 D		SYNC DATE=11/01/2010	
PAGE TITLE			
T29 A PORT MICROCONTROLLER		DRAWING NUMBER	051-8774
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3.3V/HV Power MUX

Port A 3.3V Power Switch

Port A HV Power Switch

	Nominal	Min	Max
IFLT	2A	1.8A	2.2A
ILIM	829mA	687mA	971mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance @ 210K per TI

SI8409DB:
 Vds(max): -30V
 Vgs(max): +/-12V
 Vgs(th): -1.4V
 Rds(on): 65mOhm @ 2.5V Vgs
 Id(max): 3.7A @ 70C
 Blocking FET, off when Source >3.4V or HV_EN high.

3.3V/HV MUXed

Bleeder Resistor
 2.5V / 249 ohm = 10mA
 P = -27mW

Note: Bleeder active when T29_A_HV_EN is LOW and DPAPRSW_P3V3_ON_L is HIGH (>0.8V).

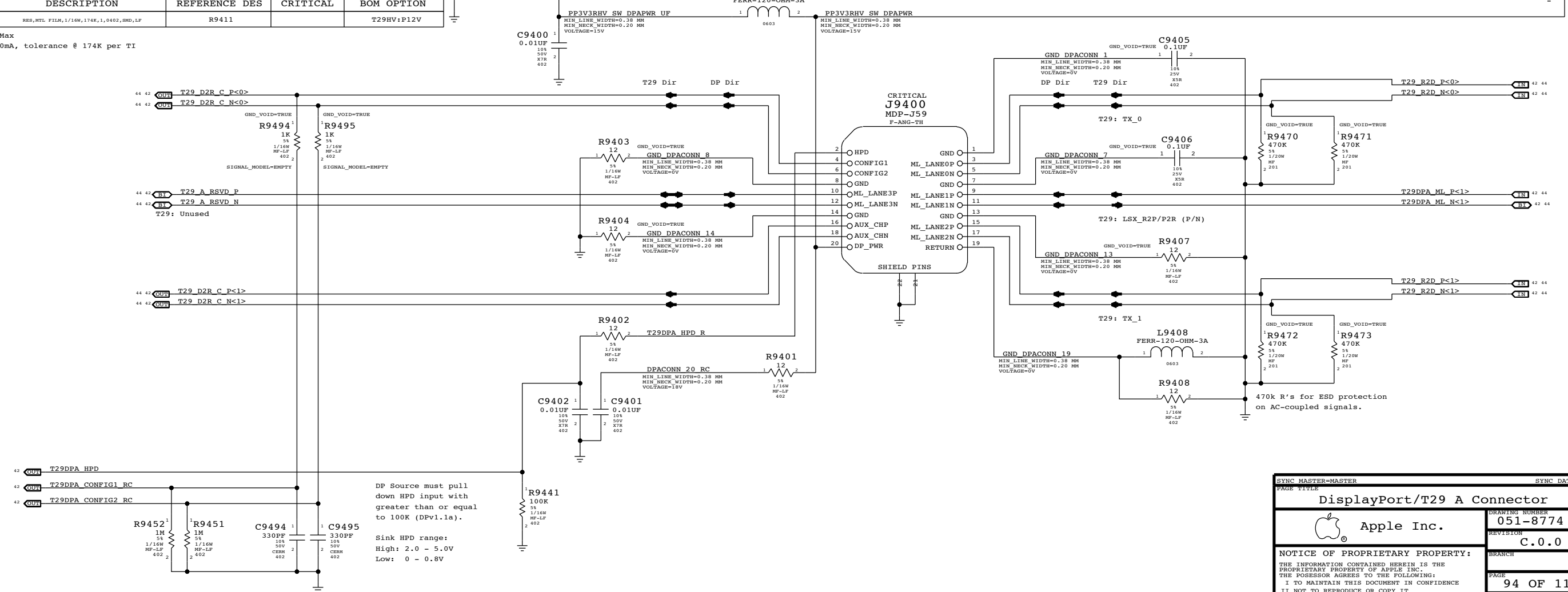
DPAPRSW HVEN L

For 12V systems:
 ILIM = 201k / RLIM = 1033mA +/- 156mA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0434	1	RES,MTL, FILM, 1/16W, 174K, 1, 0402, SMD, LF	R9411		T29HV:P12V

Nominal Min Max
 ILIM 1033mA 877mA 1190mA, tolerance @ 174K per TI

DisplayPort/T29 A Connector



DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
 Sink HPD range:
 High: 2.0 - 5.0V
 Low: 0 - 0.8V

SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE			
DisplayPort/T29 A Connector		DRAWING NUMBER	SIZE
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PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIEG2_85D	*	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIEG2_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIEG2	*	=3X_DIELECTRIC	?	PCIEG2	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
I2C_55SE	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	0.1MM	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_90D	*	N	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
T29DP_90D	TOP,BOTTOM	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DP CONNECTOR SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4:1_SPACING	?	DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?

T29 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P	23 23
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N	23 23
	I2C_55SE	I2C	I2C T29_SCL	23 35
	I2C_55SE	I2C	I2C T29_SDA	23 35
T29_SPT_CLK	T29_SPT_55S	T29_SPT	T29 SPI_CLK	23
T29_SPT_MOSI	T29_SPT_55S	T29_SPT	T29 SPI MOSI	23
T29_SPT_MISO	T29_SPT_55S	T29_SPT	T29 SPI MISO	23
T29_SPT_CS_L	T29_SPT_55S	T29_SPT	T29 SPI_CS_L	23
	T29DP_90D	T29DP	T29 R2D C P<3..0>	23 42
	T29DP_90D	T29DP	T29 R2D C N<3..0>	23 42
	T29DP_90D	T29DP	T29 D2R P<3..0>	23 42
	T29DP_90D	T29DP	T29 D2R N<3..0>	23 42
T29_R2D0	T29DP_90D	T29DP	T29 R2D P<0>	42 43
T29_R2D0	T29DP_90D	T29DP	T29 R2D N<0>	42 43
T29_R2D1	T29DP_90D	T29DP	T29 R2D P<1>	42 43
T29_R2D1	T29DP_90D	T29DP	T29 R2D N<1>	42 43
	T29DP_90D	T29DP	T29 R2D C F P<1..0>	42
	T29DP_90D	T29DP	T29 R2D C F N<1..0>	42
T29_D2R0	T29DP_90D	T29DP	T29 D2R C P<0>	42 43
T29_D2R0	T29DP_90D	T29DP	T29 D2R C N<0>	42 43
T29_D2R1	T29DP_90D	T29DP	T29 D2R C P<1>	42 43
T29_D2R1	T29DP_90D	T29DP	T29 D2R C N<1>	42 43
DP_90D	DISPLAYPORT	DISPLAYPORT	T29DPA ML P<1>	42 43
DP_90D	DISPLAYPORT	DISPLAYPORT	T29DPA ML N<1>	42 43
USB2_90D	USB2	USB2	T29 A_RSVD P	42 43
USB2_90D	USB2	USB2	T29 A_RSVD N	42 43
	T29DP_90D	T29DP	T29 R2C P<1..0>	41
	T29DP_90D	T29DP	T29 R2C N<1..0>	41
T29_R2C0	T29DP_90D	T29DP	T29 R2C C P<0>	23 41
T29_R2C0	T29DP_90D	T29DP	T29 R2C C N<0>	23 41
T29_R2C1	T29DP_90D	T29DP	T29 R2C C P<1>	23 41
T29_R2C1	T29DP_90D	T29DP	T29 R2C C N<1>	23 41
T29_C2R0	T29DP_90D	T29DP	T29 C2R P<0>	23 41
T29_C2R0	T29DP_90D	T29DP	T29 C2R N<0>	23 41
T29_C2R1	T29DP_90D	T29DP	T29 C2R P<1>	23 41
T29_C2R1	T29DP_90D	T29DP	T29 C2R N<1>	23 41
	T29DP_90D	T29DP	T29 C2R C P<1..0>	41
	T29DP_90D	T29DP	T29 C2R C N<1..0>	41

T29 DP AND DOWNSTREAM PORTS
T29/DP TETHERED CABLE

INTERNAL PANEL PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
DP_90D	DISPLAYPORT	DISPLAYPORT	DP INT ML C P<3..0>	7
DP_90D	DISPLAYPORT	DISPLAYPORT	DP INT ML C N<3..0>	7
DP_INT_ML	DP_90D	DISPLAYPORT	DP INT ML P<3..0>	7 21 48
DP_INT_ML	DP_90D	DISPLAYPORT	DP INT ML N<3..0>	7 21 48
DP_INT_AUXCH	DP_90D	DISPLAYPORT	DP INT_AUXCH C P	7
DP_INT_AUXCH	DP_90D	DISPLAYPORT	DP INT_AUXCH C N	7
DP_INT_AUXCH	DP_90D	DISPLAYPORT	DP INT_AUXCH P	7 21 48
DP_INT_AUXCH	DP_90D	DISPLAYPORT	DP INT_AUXCH N	7 21 48

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Temp Sensor Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMPSENS_PAIR	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	20MM	0.25MM	0.10MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMPSENS	*	=2x_DIELECTRIC	?

Temp Sensor Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
E29D	TEMPSENS_PAIR	TEMPSENS	DX1_P
E29D	TEMPSENS_PAIR	TEMPSENS	DX1_N
E29D	TEMPSENS_PAIR	TEMPSENS	TDX1_P
E29D	TEMPSENS_PAIR	TEMPSENS	TDX1_N
E29D	TEMPSENS_PAIR	TEMPSENS	DX2_P
E29D	TEMPSENS_PAIR	TEMPSENS	DX2_N
E29D	TEMPSENS_PAIR	TEMPSENS	TDX2_P
E29D	TEMPSENS_PAIR	TEMPSENS	TDX2_N

Temp sensor routes

AUDIO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.6 MM	0.2 MM	10 MM	0.2 MM	0.2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.2 MM	?

AUDIO NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
E2E9	AUDIODIFF	AUDIO	AUD_LTWT_N
E2E9	AUDIODIFF	AUDIO	AUD_LTWT_P
E2E9	AUDIODIFF	AUDIO	AUD_LWFR_N
E2E9	AUDIODIFF	AUDIO	AUD_LWFR_P
E2E9	AUDIODIFF	AUDIO	AUD_RTWT_N
E2E9	AUDIODIFF	AUDIO	AUD_RTWT_P
E2E9	AUDIODIFF	AUDIO	AUD_RWFR_N
E2E9	AUDIODIFF	AUDIO	AUD_RWFR_P
E2E9	AUDIODIFF	AUDIO	AUD_SUB_N
E2E9	AUDIODIFF	AUDIO	AUD_SUB_P

SPEAKER NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
E2E9	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT_N
E2E9	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT_P
E2E9	AUDIODIFF	AUDIO	SPKRAMP_LWFR_OUT_N
E2E9	AUDIODIFF	AUDIO	SPKRAMP_LWFR_OUT_P
E2E9	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT_N
E2E9	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT_P
E2E9	AUDIODIFF	AUDIO	SPKRAMP_RWFR_OUT_N
E2E9	AUDIODIFF	AUDIO	SPKRAMP_RWFR_OUT_P
E2E9	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT_N
E2E9	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT_P

I2C Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
I2C_558E	I2C	I2C	I2C LPCREEM_SDA
I2C_558E	I2C	I2C	I2C LPCREEM_SCL
I2C_558E	I2C	I2C	DDC_SDA_FC
I2C_558E	I2C	I2C	DDC_SCL_FC
I2C_558E	I2C	I2C	SDA_FC
I2C_558E	I2C	I2C	SCL_FC
I2C_558E	I2C	I2C	SDA_SWREM
I2C_558E	I2C	I2C	SCL_SWREM
I2C_558E	I2C	I2C	I2C DP628_SDA
I2C_558E	I2C	I2C	I2C DP628_SCL
I2C_558E	I2C	I2C	I2C LPCLOC_SDA
I2C_558E	I2C	I2C	I2C LPCLOC_SCL
I2C_558E	I2C	I2C	I2C FALS_SDA
I2C_558E	I2C	I2C	I2C FALS_SCL
I2C_558E	I2C	I2C	I2C LFC1_SDA
I2C_558E	I2C	I2C	I2C LFC1_SCL
I2C_558E	I2C	I2C	I2C ALS_SCL
I2C_558E	I2C	I2C	I2C ALS_SDA
I2C_558E	I2C	I2C	I2C USBHOST_SCL
I2C_558E	I2C	I2C	I2C USBHOST_SDA

I2C pairs from LPC

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
I2C_558E	I2C	I2C	ADAV4601_I2C_SDA
I2C_558E	I2C	I2C	ADAV4601_I2C_SCL
I2C_558E	I2C	I2C	I2C_SDA
I2C_558E	I2C	I2C	I2C_SCL
I2C_558E	I2C	I2C	AUD_161_I2C_SDA
I2C_558E	I2C	I2C	AUD_161_I2C_SCL
I2C_558E	I2C	I2C	I2C MCU_SCL
I2C_558E	I2C	I2C	I2C MCU_SDA

Audio I2C pairs

MicroCtrl Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
MICROCTRL_558E	MICROCTRL	MICROCTRL	ADC_STR0_V
MICROCTRL_558E	MICROCTRL	MICROCTRL	ADC_STR1_V
MICROCTRL_558E	MICROCTRL	MICROCTRL	ADC_STR2_V
MICROCTRL_558E	MICROCTRL	MICROCTRL	DAC_OUT
MICROCTRL_558E	MICROCTRL	MICROCTRL	ADC_USB5V
MICROCTRL_558E	MICROCTRL	MICROCTRL	F5VP3V3_VREF

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Ethernet MDI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

PCie Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
ENET	PCIE_R5D	PCIE	PCIE ENET R2D P	26
ENET	PCIE_R5D	PCIE	PCIE ENET R2D N	26
ENET	PCIE_ENET_R2D	PCIE	PCIE ENET R2D C P	7 26
ENET	PCIE_ENET_R2D	PCIE	PCIE ENET R2D C N	7 26
ENET	PCIE_ENET_D2R	PCIE	PCIE ENET D2R P	7 26
ENET	PCIE_ENET_D2R	PCIE	PCIE ENET D2R N	7 26
ENET	PCIE_R5D	PCIE	PCIE ENET D2R C P	26
ENET	PCIE_R5D	PCIE	PCIE ENET D2R C N	26
ENET	PCIE_CLK100M_ENET	CLK_PCIE_R5D	PCIE CLK100M ENET P	22 26
ENET	PCIE_CLK100M_ENET	CLK_PCIE_R5D	PCIE CLK100M ENET N	22 26

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FIREWIRE PCIE NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
FW	PCIE_R5D	PCIE	PCIE FW R2D P	28
FW	PCIE_R5D	PCIE	PCIE FW R2D N	28
FW	PCIE_FW_R2D	PCIE	PCIE FW R2D C P	7 28
FW	PCIE_FW_R2D	PCIE	PCIE FW R2D C N	7 28
FW	PCIE_FW_D2R	PCIE	PCIE FW D2R P	7 28
FW	PCIE_FW_D2R	PCIE	PCIE FW D2R N	7 28
FW	PCIE_R5D	PCIE	PCIE FW D2R C P	28
FW	PCIE_R5D	PCIE	PCIE FW D2R C N	28
FW	PCIE_CLK100M_FW	CLK_PCIE_R5D	PCIE CLK100M FW P	22 28
FW	PCIE_CLK100M_FW	CLK_PCIE_R5D	PCIE CLK100M FW N	22 28

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?

USB PCIE NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
USB	PCIEG2_R5D	PCIEG2	PCIE USB D2R C P	32
USB	PCIEG2_R5D	PCIEG2	PCIE USB D2R C N	32
USB	PCIEG2_R5D	PCIEG2	PCIE USB R2D P	32
USB	PCIEG2_R5D	PCIEG2	PCIE USB R2D N	32
USB	PCIE_USB_R2D	PCIEG2	PCIE USB R2D C P	7 32
USB	PCIE_USB_R2D	PCIEG2	PCIE USB R2D C N	7 32
USB	PCIE_USB_D2R	PCIEG2	PCIE USB D2R P	7 32
USB	PCIE_USB_D2R	PCIEG2	PCIE USB D2R N	7 32
USB	PCIE_CLK100M_USB	CLK_PCIE_R5D	PCIE CLK100M USB P	7 32
USB	PCIE_CLK100M_USB	CLK_PCIE_R5D	PCIE CLK100M USB N	7 32
USB	PCIE_CLK100M_USB	CLK_PCIE_R5D	PCIE CLK100M USB C P	32
USB	PCIE_CLK100M_USB	CLK_PCIE_R5D	PCIE CLK100M USB C N	32

Ethernet MDI Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN MDI P<3..0>	26 27
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN MDI N<3..0>	26 27
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN MDI T P<3..0>	27
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN MDI T N<3..0>	27

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
FW	FW_R0_TPA	FW_TP	FW PORT0 TPA P	29 30
FW	FW_R0_TPA	FW_TP	FW PORT0 TPA N	29 30
FW	FW_R0_TPB	FW_TP	FW PORT0 TPB P	29 30
FW	FW_R0_TPB	FW_TP	FW PORT0 TPB N	29 30

USB Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
USB	USB2_90D	USB2	USB_HUB_UP_DP	31
USB	USB2_90D	USB2	USB_HUB_UP_DM	31
USB	USB2_90D	USB2	USB_DEV_DP	31
USB	USB2_90D	USB2	USB_DEV_DM	31
USB	USB2_90D	USB2	USB_DEV_F_DP	31
USB	USB2_90D	USB2	USB_DEV_F_DM	31
USB	USB2_90D	USB2	USB_HOST_DP	31 32
USB	USB2_90D	USB2	USB_HOST_DM	31 32
USB	USB2_90D	USB2	USBBDN1_H1_DP	31 33
USB	USB2_90D	USB2	USBBDN1_H1_DM	31 33
USB	USB2_90D	USB2	USBBDN2_H1_DP	31 33
USB	USB2_90D	USB2	USBBDN2_H1_DM	31 33
USB	USB2_90D	USB2	USBBDN3_H1_DP	31 33
USB	USB2_90D	USB2	USBBDN3_H1_DM	31 33
USB	USB2_90D	USB2	USB_UC_DP	20 31
USB	USB2_90D	USB2	USB_UC_DM	20 31
USB	USB2_90D	USB2	USB_AUDIO_DP	11 31
USB	USB2_90D	USB2	USB_AUDIO_DM	11 31
USB	USB2_90D	USB2	USB_CAMERA_DP	10 31
USB	USB2_90D	USB2	USB_CAMERA_DM	10 31
USB	USB2_90D	USB2	CAM_DP	10 48
USB	USB2_90D	USB2	CAM_DM	10 48
USB	USB2_90D	USB2	AUD_161_USB_DP	12
USB	USB2_90D	USB2	AUD_161_USB_DM	12
USB	USB2_90D	USB2	DM1	33
USB	USB2_90D	USB2	DP1	33
USB	USB2_90D	USB2	DM2	33
USB	USB2_90D	USB2	DP2	33
USB	USB2_90D	USB2	DM3	33
USB	USB2_90D	USB2	DP3	33

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T29 Dr.B-Specific Physical & Spacing Constraints

BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM			NO_TYPE			MM	15.7

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	6.35 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL6	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL6	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL6	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL6	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL6	Y	0.067 MM	0.067 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

Standard Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
2:1_SPACING	*	0.2 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.355 MM	?
2X_DIELECTRIC	*	0.152 MM	?
3X_DIELECTRIC	*	0.228 MM	?
4X_DIELECTRIC	*	0.304 MM	?
5X_DIELECTRIC	*	0.380 MM	?

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FUNCTIONAL TEST POINTS

NC AND NO_TEST NETS

FLIP SIDE PCI BRIDGE AND USB CONTROLLER MOUNTING AND ROUTING MAKES TEST VIRTUALLY IMPOSSIBLE

J1013 ODD FAN

8 **FN** FAN0_PWR FUNC_TEST=TRUE
 8 **FN** FAN_TACHO FUNC_TEST=TRUE
 19 **FN** PP12V_FAN_FET FUNC_TEST=TRUE
 MIN_ALLOWED_TPS=3
 3 GROUND TESTPOINTS NEAR J1013

J1115 BLC CONNECTOR

9 **FN** STR0_+ FUNC_TEST=TRUE
 9 **FN** STR0_- FUNC_TEST=TRUE
 9 **FN** STR0C FUNC_TEST=TRUE
 9 **FN** STR1_+ FUNC_TEST=TRUE
 9 **FN** STR1_- FUNC_TEST=TRUE
 9 **FN** STR1C FUNC_TEST=TRUE
 9 **FN** STR2_+ FUNC_TEST=TRUE
 9 **FN** STR2_- FUNC_TEST=TRUE
 9 **FN** STR2C FUNC_TEST=TRUE
 2 GROUND TESTPOINTS NEAR J1013

J1204 USB CAMERA

10 **FN** PP5V_CAM_FLIT FUNC_TEST=TRUE
 MIN_ALLOWED_TPS=1
 46 **FN** CAM_DM FUNC_TEST=TRUE
 46 **FN** CAM_DP FUNC_TEST=TRUE
 45 **FN** I2C_ALS_SCL FUNC_TEST=TRUE
 45 **FN** I2C_ALS_SDA FUNC_TEST=TRUE
 4 GROUND TESTPOINTS NEAR J1204

J2007 MICROPHONE

18 **FN** AUD_MIC_IN_N_CONN FUNC_TEST=TRUE
 18 **FN** GND_AUD_MIC_CONN FUNC_TEST=TRUE
 18 **FN** AUD_MIC_IN_P_CONN FUNC_TEST=TRUE
 2 GROUND TESTPOINTS NEAR J2007

J2003 AUDIO LEFT SPEAKER

45 18 **FN** SPKRAMP_LWFR_OUT_P FUNC_TEST=TRUE
 45 18 **FN** SPKRAMP_LWFR_OUT_N FUNC_TEST=TRUE
 45 18 **FN** SPKRAMP_LTWI_OUT_P FUNC_TEST=TRUE
 45 18 **FN** SPKRAMP_LTWI_OUT_N FUNC_TEST=TRUE

J2004 AUDIO RIGHT SPEAKER

45 18 **FN** SPKRAMP_RWFR_OUT_P FUNC_TEST=TRUE
 45 18 **FN** SPKRAMP_RWFR_OUT_N FUNC_TEST=TRUE
 45 18 **FN** SPKRAMP_RTWI_OUT_P FUNC_TEST=TRUE
 45 18 **FN** SPKRAMP_RTWI_OUT_N FUNC_TEST=TRUE

J2005 AUDIO SUBWOOFER

45 18 **FN** SPKRAMP_SUB_OUT_P FUNC_TEST=TRUE
 45 18 **FN** SPKRAMP_SUB_OUT_N FUNC_TEST=TRUE
 18 17 16 15 **FN** GND_AUDIO_SPKRAMP FUNC_TEST=TRUE
 MIN_ALLOWED_TPS=6

J1011 BLOWER TEMP SENSOR

45 **FN** TDX1_N FUNC_TEST=TRUE
 45 **FN** TDX1_P FUNC_TEST=TRUE
 2 GROUND TESTPOINTS NEAR J1011

J1012 PSU TEMP SENSOR

45 **FN** TDX2_N FUNC_TEST=TRUE
 45 **FN** TDX2_P FUNC_TEST=TRUE
 2 GROUND TESTPOINTS NEAR J1012

J2726 PANEL POWER

21 **FN** PP12V_PANEL_FC FUNC_TEST=TRUE
 MIN_ALLOWED_TPS=4
 4 GROUND TESTPOINTS NEAR J2726


J2725 INTERNAL DP PANEL

44 21 **FN** DP_INT_ML_P<3..0> FUNC_TEST=TRUE
 44 21 **FN** DP_INT_ML_N<3..0> FUNC_TEST=TRUE
 44 21 **FN** DP_INT_AUXCH_P FUNC_TEST=TRUE
 44 21 **FN** DP_INT_AUXCH_N FUNC_TEST=TRUE
 45 21 **FN** DDC_SCL_FC FUNC_TEST=TRUE
 45 21 **FN** DDC_SDA_FC FUNC_TEST=TRUE
 45 21 **FN** SCL_FC FUNC_TEST=TRUE
 45 21 **FN** SDA_FC FUNC_TEST=TRUE
 21 **FN** AUDIO_ON_FC FUNC_TEST=TRUE
 21 **FN** AUDIO_MUTE_FC_L FUNC_TEST=TRUE
 21 **FN** I2S_SCLK_FC FUNC_TEST=TRUE
 21 **FN** I2S_WS_FC FUNC_TEST=TRUE
 21 **FN** I2S_SDO_FC FUNC_TEST=TRUE
 21 **FN** DP_PWR_UP_FC FUNC_TEST=TRUE
 21 **FN** INT_FC_L FUNC_TEST=TRUE
 21 **FN** DP_INT_HPD_FC FUNC_TEST=TRUE
 21 **FN** VIDEO_ON_FC FUNC_TEST=TRUE
 21 **FN** VSYNC_FC FUNC_TEST=TRUE
 17 GROUND TESTPOINTS NEAR J2725

GND 36 TR/S FUNC_TEST=TRUE
 MIN_ALLOWED_TPS=36

TP_PCIBR_WAKE_L == NC_PCIBR_WAKE_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_EECS_L == NC_PEX8112_EECS_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_EECLK == NC_PEX8112_EECLK
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_EERDDATA == NC_PEX8112_EERDDATA
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_EEWRDATA == NC_PEX8112_EEWRDATA
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_GPI00 == NC_PEX8112_GPI00
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_GPI01 == NC_PEX8112_GPI01
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_GPI02 == NC_PEX8112_GPI02
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_GPI03 == NC_PEX8112_GPI03
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_PWR_OK == NC_PEX8112_PWR_OK
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_BAR0ENB_L == NC_PEX8112_BAR0ENB_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_PCLK062SEL_L == NC_PEX8112_PCLK062SEL_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_PMEOUT_L == NC_PEX8112_PMEOUT_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_GNT1_L == NC_PEX8112_GNT1_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_GNT2_L == NC_PEX8112_GNT2_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_GNT3_L == NC_PEX8112_GNT3_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_PEX8112_PCLK0 == NC_PEX8112_PCLK0
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_SMI_L == NC_NECUSB_SMI_L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_PPON1 == NC_NECUSB_PPON1
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_PPON2 == NC_NECUSB_PPON2
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_PPON3 == NC_NECUSB_PPON3
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_SRCLK == NC_NECUSB_SRCLK
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_SRPTA == NC_NECUSB_SRPTA
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_SRMOD == NC_NECUSB_SRMOD
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_TESTEN == NC_NECUSB_TESTEN
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_TEST3 == NC_NECUSB_TEST3
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NECUSB_TEST4 == NC_NECUSB_TEST4
 MAKE_BASE=TRUE
 NO_TEST=TRUE

NO_TEST=TRUE PCI_ADR<31..0>
 NO_TEST=TRUE PCI_C_BE<1:3..0>
 NO_TEST=TRUE PCI_PAR
 NO_TEST=TRUE PCI_FRAME_L
 NO_TEST=TRUE PCI_IRDY_L
 NO_TEST=TRUE PCI_TRDY_L
 NO_TEST=TRUE PCI_DEVSEL_L
 NO_TEST=TRUE PCI_STOP_L
 NO_TEST=TRUE PCI_PERR_L
 NO_TEST=TRUE PCI_SERR_L
 NO_TEST=TRUE PCI_NECUSB_REQ_L
 NO_TEST=TRUE PCI_NECUSB_GNT_L
 NO_TEST=TRUE PCI_NECUSB_INT_L
 NO_TEST=TRUE PCI_CLKRUN_L
 NO_TEST=TRUE PCI_RESET_L

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