

# Compal confidential

## ISKAA LA-3481P Schematics Document

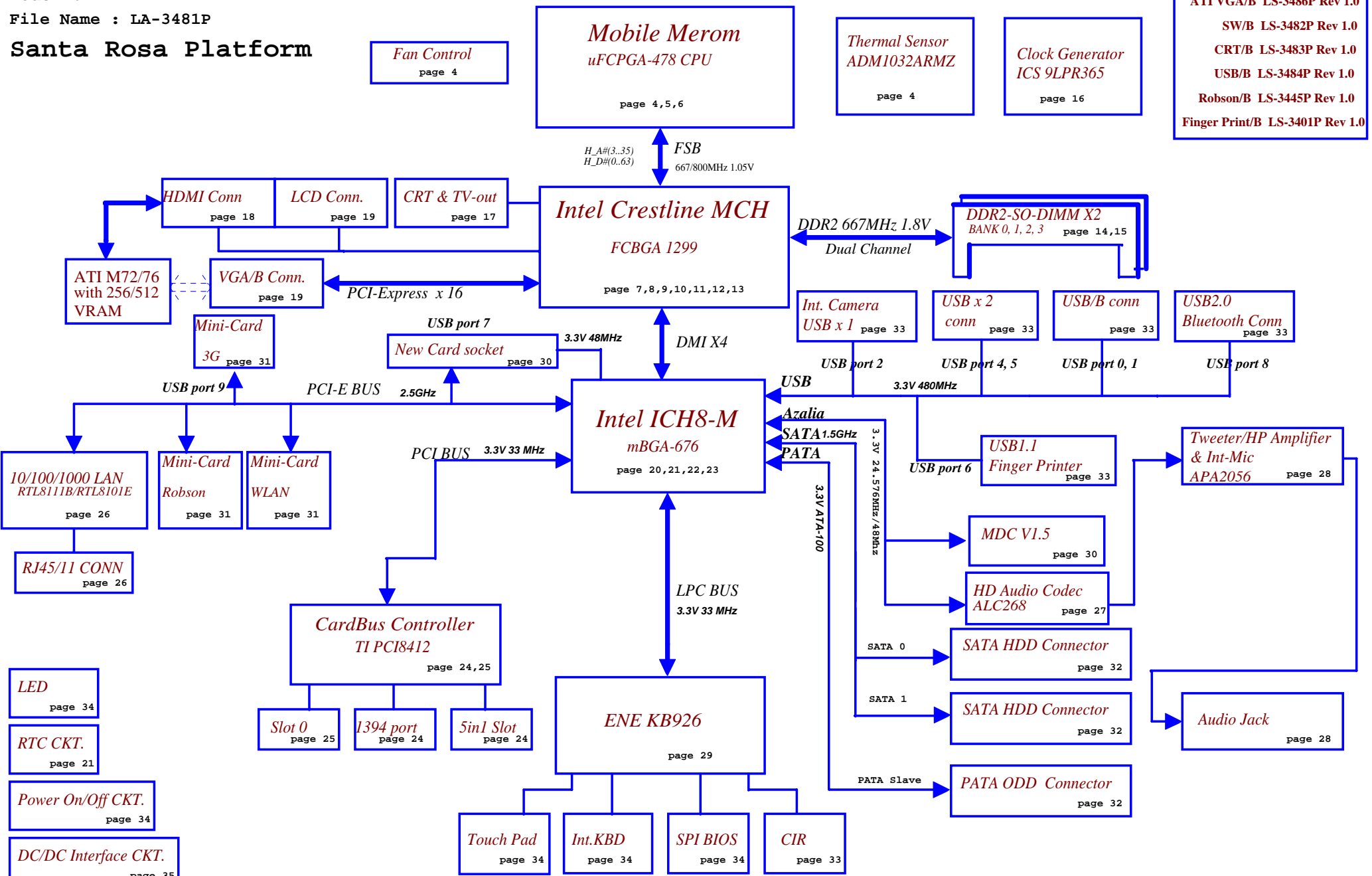
Mobile Merom uFCPGA with Intel  
Crestline\_PM+ICH8-M core logic

2007-06-23

REV: 2.0A

Security Classification	Compal Secret Data			Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Cover Sheet	
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				LA-3481P	2.0
Date: Saturday, June 23, 2007				Sheet	1 of 47

*ISKAA Sub-board*  
 ATI VGA/B LS-3481P Rev 1.0  
 ATI VGA/B LS-3486P Rev 1.0  
 SW/B LS-3482P Rev 1.0  
 CRT/B LS-3483P Rev 1.0  
 USB/B LS-3484P Rev 1.0  
 Robson/B LS-3445P Rev 1.0  
 Finger Print/B LS-3401P Rev 1.0



- LED page 34
- RTC CKT. page 21
- Power On/Off CKT. page 34
- DC/DC Interface CKT. page 35
- Power Circuit DC/DC Page 36-43

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Date:	Tuesday, May 22, 2007	Sheet	2	of 47

**Compal Electronics, Inc.**  
**Block Diagram**

## Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.05VS	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+1.25VS	1.25V power rail for MCH/ICH core power	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C,D
CARD BUS	D4	AD20	2	A,B,C,D
SIN1	D4	AD20	2	A,B,C,D

## KB926 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1010000 X b
SM1 SMART BATTERY	16H	0001011 X b
SM2 ADM0132	98H	1001100 X b
CPU THERMAL MONITOR		

## ICH8-M SM Bus address

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 1%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0.100 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	2.0
6	2A
7	

## SKU ID Table

SKU ID	SKU
0	10
1	10G
2	
3	
4	
5	
6	
7	

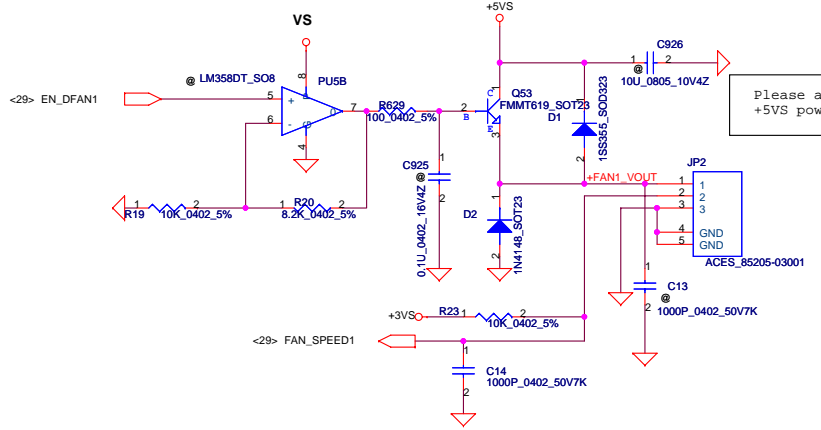
## BTO Option Table

BTO Item	BOM Structure
2nd HDD	2HDD@
LAN	100M@ 1000M@
WLAN	WLAN@
NB	GM@ PM@
BT	BT@
MIC	MIC@
CIR	CIR@
FINGER PRINT	FP@
HDMI	HDMI@
Camera	Camera@
Robson	Robson@
Express Card	NEWCARD@
HD-DVD	3G@

## USB PORT LIST

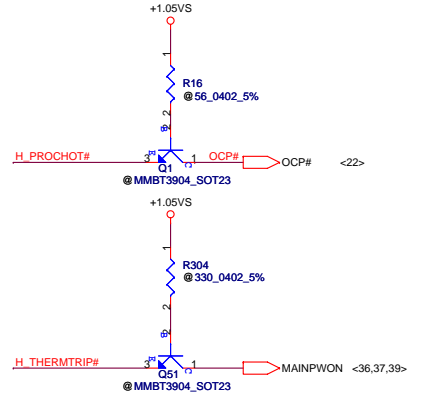
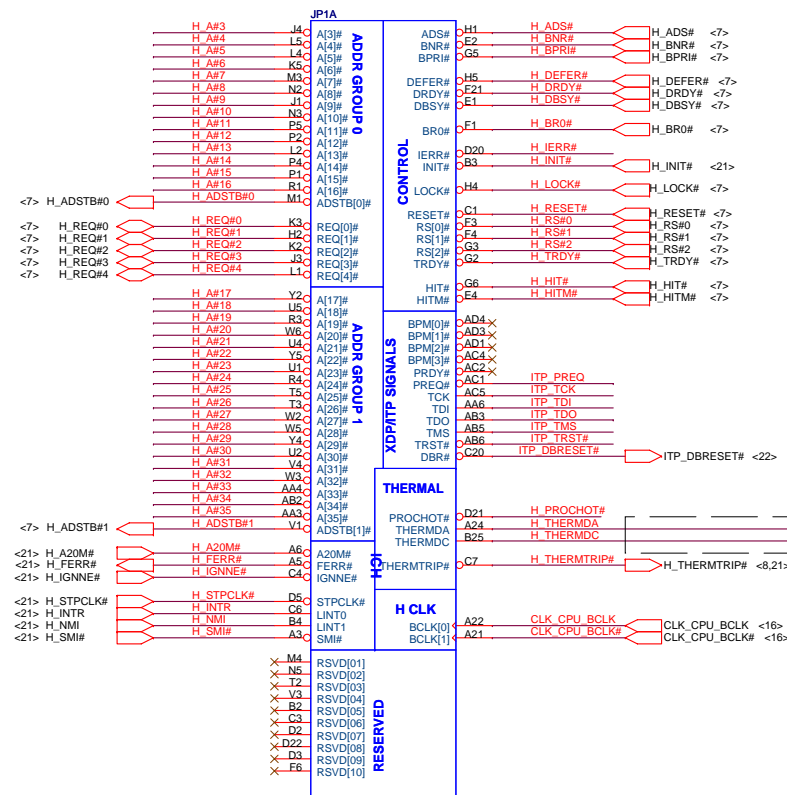
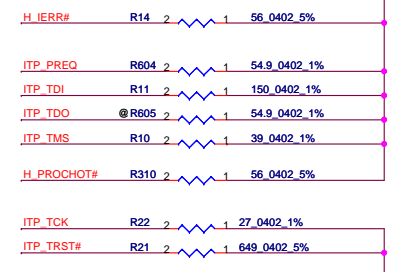
PORT	DEVICE
0	RIGHT USB Port (Samll Board)
1	RIGHT USB Port (Samll Board)
2	3G Card
3	N.C.
4	LEFT USB Port
5	LEFT USB Port
6	Fingerprint or Felica
7	Blue Tooth
8	Internal Camera
9	New Card

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Date:	Tuesday, May 22, 2007	Sheet	3	of 47



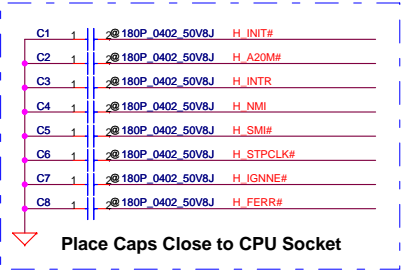
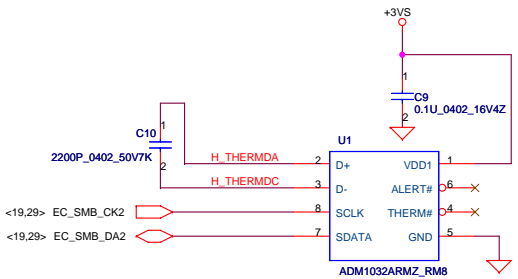
Please add the 10uF capacitor if the +5VS power source not stable.

Place close to CPU within 500mil



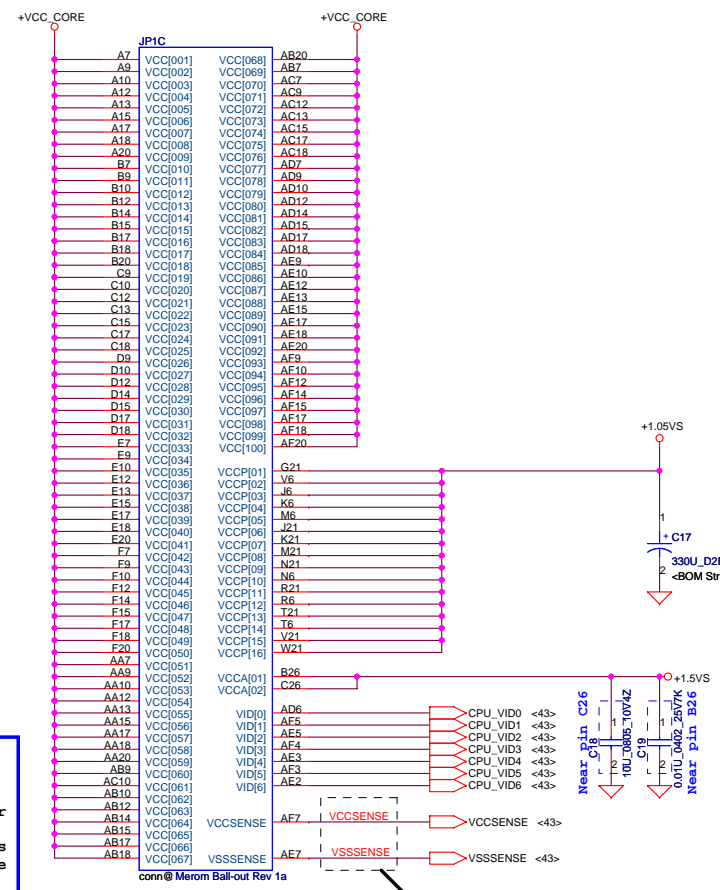
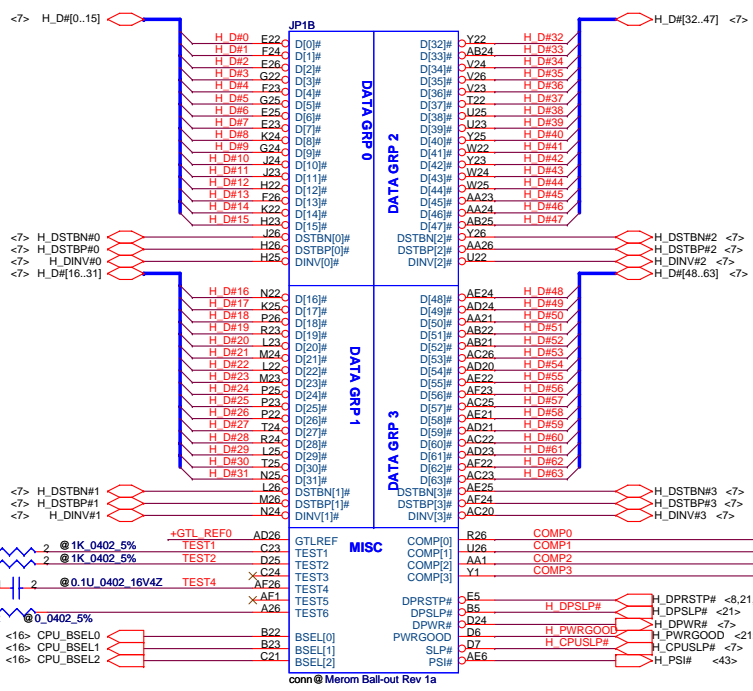
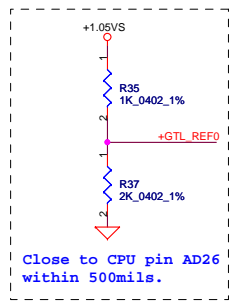
H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

### Thermal Sensor ADM1032ARM



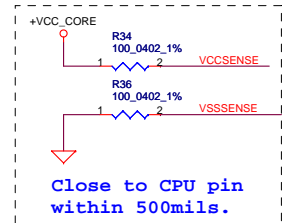
Place Caps Close to CPU Socket

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			Sheet 4 of 47



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

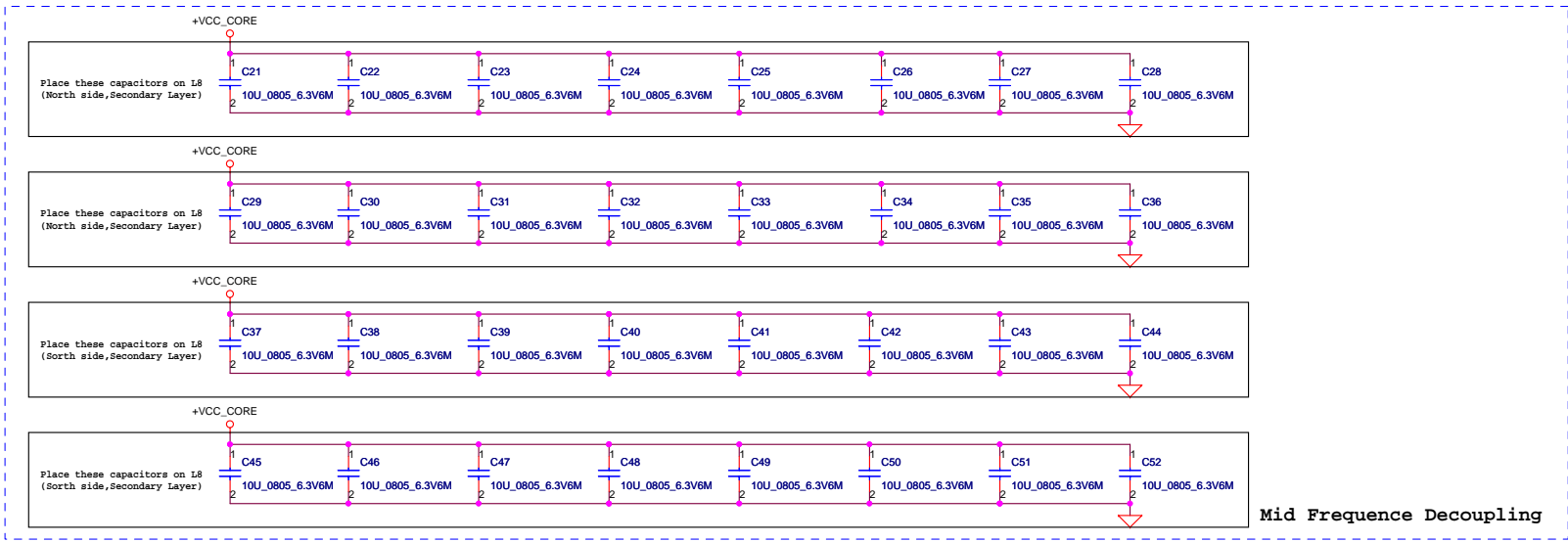
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



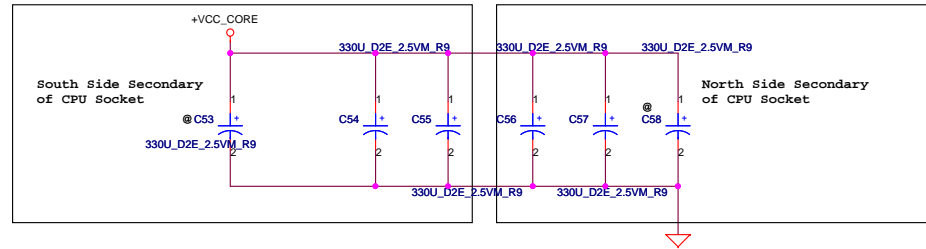
Length match within 25 mils. The trace width/space/other is 20/7/25.

JP1D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A16	VSS[004]	VSS[085]
A19	VSS[005]	VSS[086]
A23	VSS[006]	VSS[087]
AF2	VSS[007]	VSS[088]
B6	VSS[008]	VSS[089]
B8	VSS[009]	VSS[090]
B11	VSS[010]	VSS[091]
B12	VSS[011]	VSS[092]
B16	VSS[012]	VSS[093]
B19	VSS[013]	VSS[094]
B21	VSS[014]	VSS[095]
B24	VSS[015]	VSS[096]
C5	VSS[016]	VSS[097]
C6	VSS[017]	VSS[098]
C11	VSS[018]	VSS[099]
C14	VSS[019]	VSS[100]
C16	VSS[020]	VSS[101]
C19	VSS[021]	VSS[102]
C2	VSS[022]	VSS[103]
C22	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D4	VSS[026]	VSS[107]
D8	VSS[027]	VSS[108]
D9	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D19	VSS[031]	VSS[112]
D23	VSS[032]	VSS[113]
D28	VSS[033]	VSS[114]
E3	VSS[034]	VSS[115]
E6	VSS[035]	VSS[116]
E8	VSS[036]	VSS[117]
E11	VSS[037]	VSS[118]
E14	VSS[038]	VSS[119]
E16	VSS[039]	VSS[120]
E19	VSS[040]	VSS[121]
E21	VSS[041]	VSS[122]
E24	VSS[042]	VSS[123]
F5	VSS[043]	VSS[124]
F8	VSS[044]	VSS[125]
F11	VSS[045]	VSS[126]
F13	VSS[046]	VSS[127]
F16	VSS[047]	VSS[128]
F19	VSS[048]	VSS[129]
F2	VSS[049]	VSS[130]
F22	VSS[050]	VSS[131]
F25	VSS[051]	VSS[132]
G4	VSS[052]	VSS[133]
G1	VSS[053]	VSS[134]
G23	VSS[054]	VSS[135]
G26	VSS[055]	VSS[136]
H3	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H21	VSS[058]	VSS[139]
H24	VSS[059]	VSS[140]
J2	VSS[060]	VSS[141]
J5	VSS[061]	VSS[142]
J22	VSS[062]	VSS[143]
J25	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K23	VSS[066]	VSS[147]
K26	VSS[067]	VSS[148]
L3	VSS[068]	VSS[149]
L6	VSS[069]	VSS[150]
L21	VSS[070]	VSS[151]
L24	VSS[071]	VSS[152]
M2	VSS[072]	VSS[153]
M5	VSS[073]	VSS[154]
M22	VSS[074]	VSS[155]
M25	VSS[075]	VSS[156]
N1	VSS[076]	VSS[157]
N4	VSS[077]	VSS[158]
N23	VSS[078]	VSS[159]
N26	VSS[079]	VSS[160]
P3	VSS[080]	VSS[161]
	VSS[081]	VSS[162]
		VSS[163]

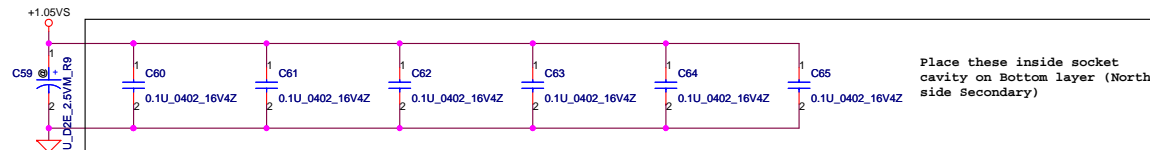
conn @ Merom Ball-out Rev 1a



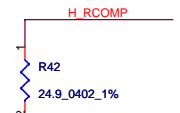
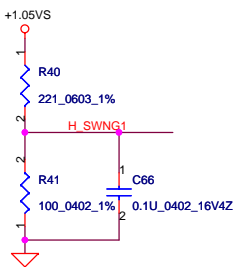
Mid Frequency Decoupling



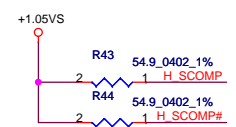
ESR <= 1.5m ohm  
Capacitor > 1980uF  
330uF ESR 7m ohm X 6 PCS



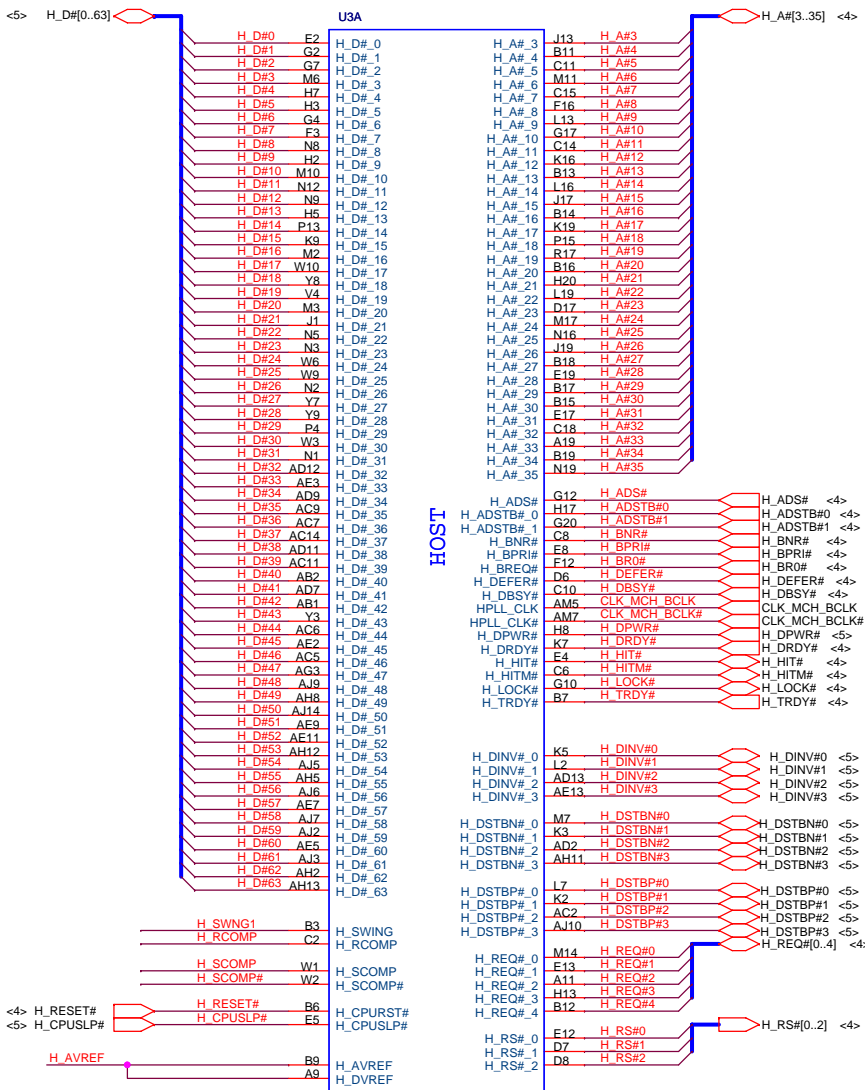
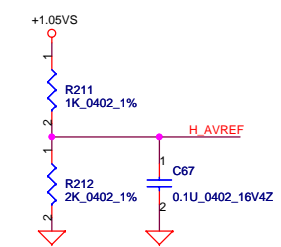
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				Rev 2.0
				LA-3481P
Date: Tuesday, May 22, 2007				Sheet 6 of 47



10-mil wide with 20-mil spacing



impedance is 55 ohm  
Width is 10mil

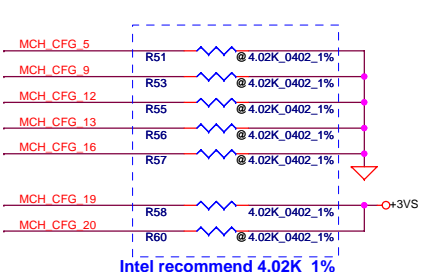


HOST

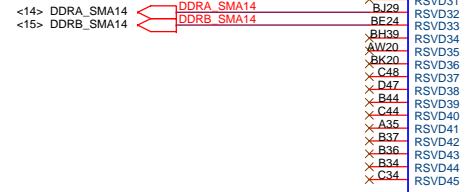
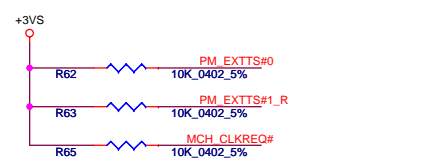
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				LA-3481P	2.0
Date:	Tuesday, May 22, 2007	Sheet	7	of	47

# Strap Pin Table

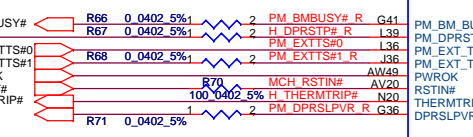
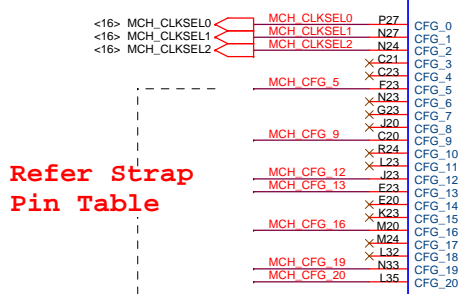
<b>CFG[2:0]</b>	011 = 667MT/s FSB 010 = 800MT/s FSB
<b>CFG5</b>	0 = DMI x 2 1 = DMI x 4 * (Default)
<b>CFG9</b>	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
<b>CFG[13:12]</b>	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
<b>CFG16</b>	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
<b>CFG19</b>	0 = Normal Operation 1 = DMI Lane Reversal Enable * (Default)
<b>CFG20 (PCIe/SDVO select)</b>	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.
<b>SDVO_CTRLDATA</b>	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present



CFG[17:3] have internal pull up  
CFG[19:18] have internal pull down



Refer Strap Pin Table



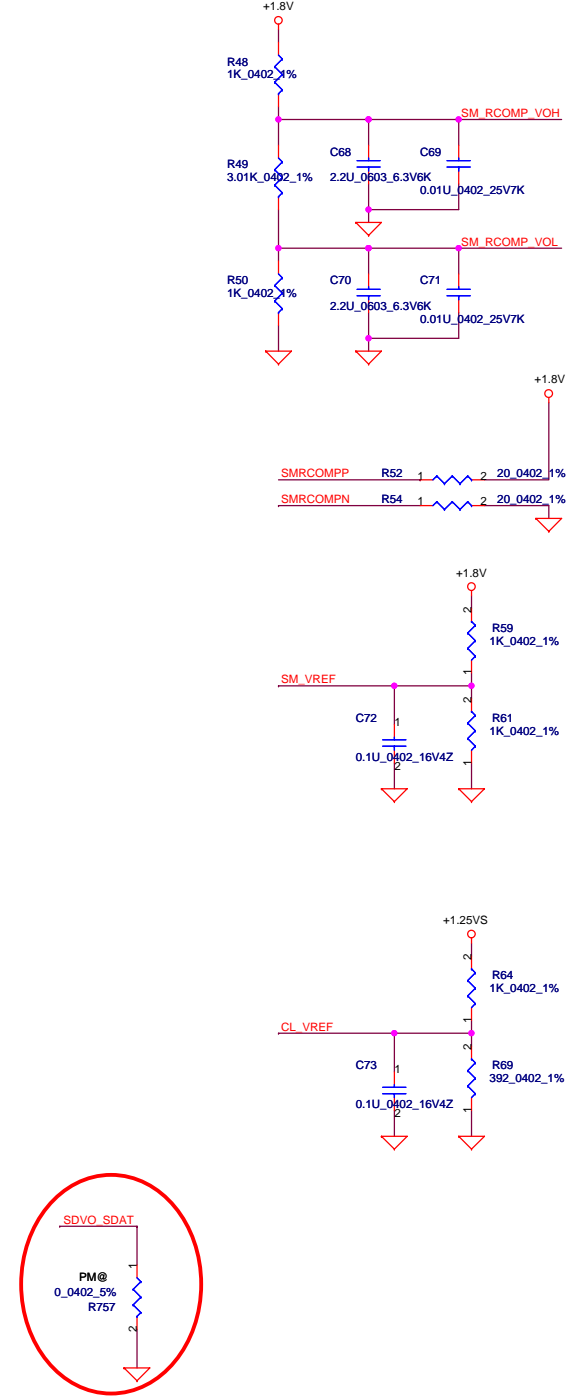
## U3B

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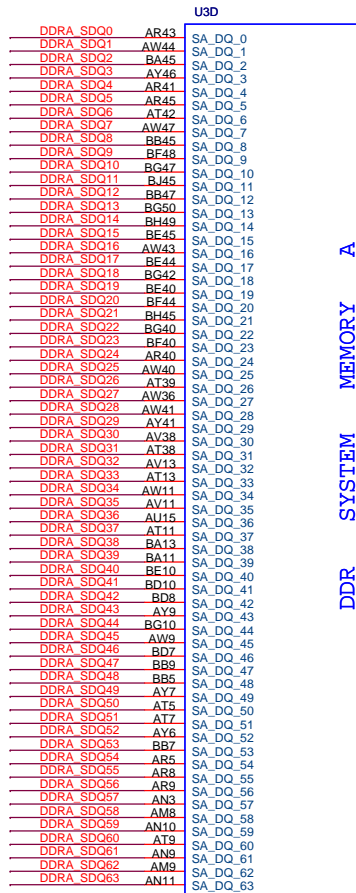
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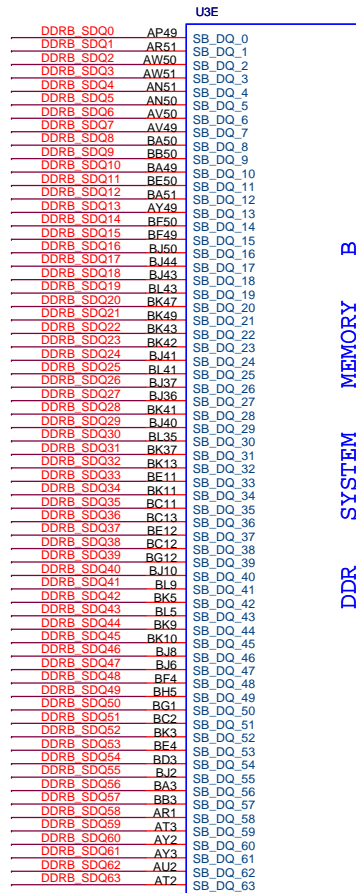




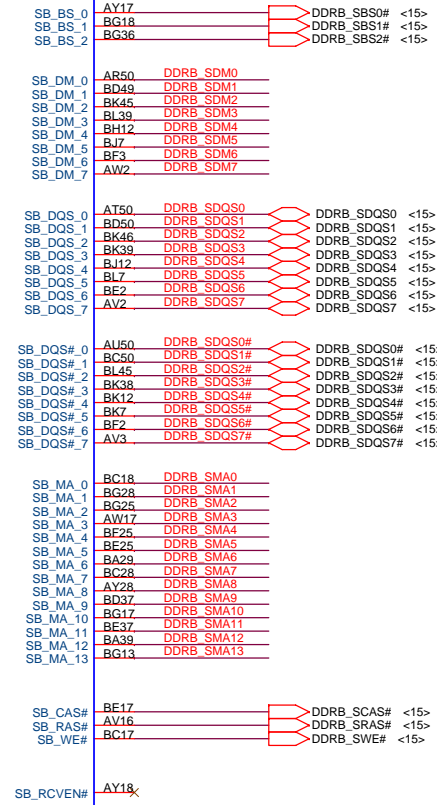
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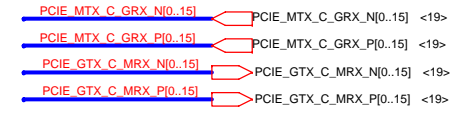
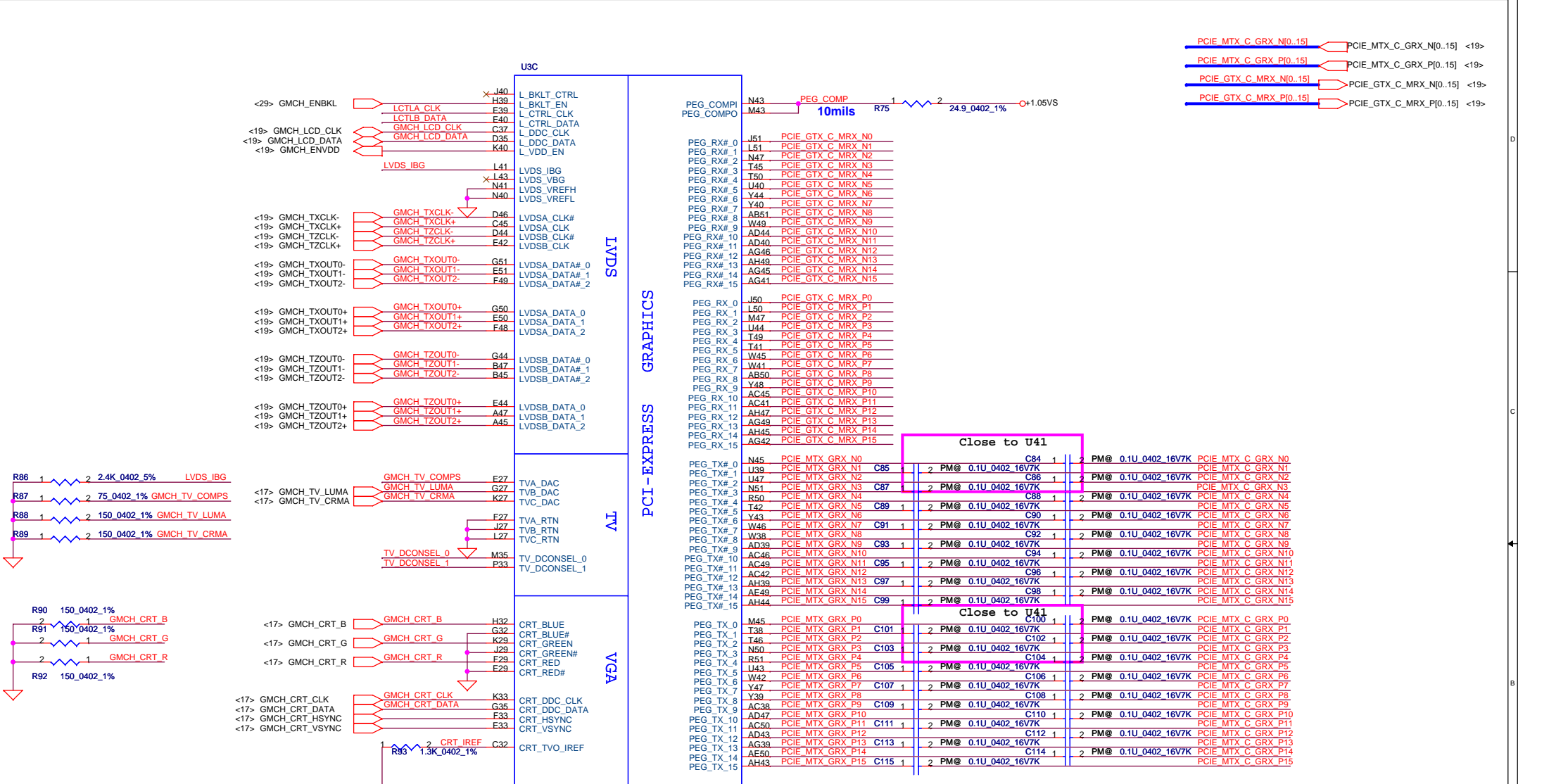


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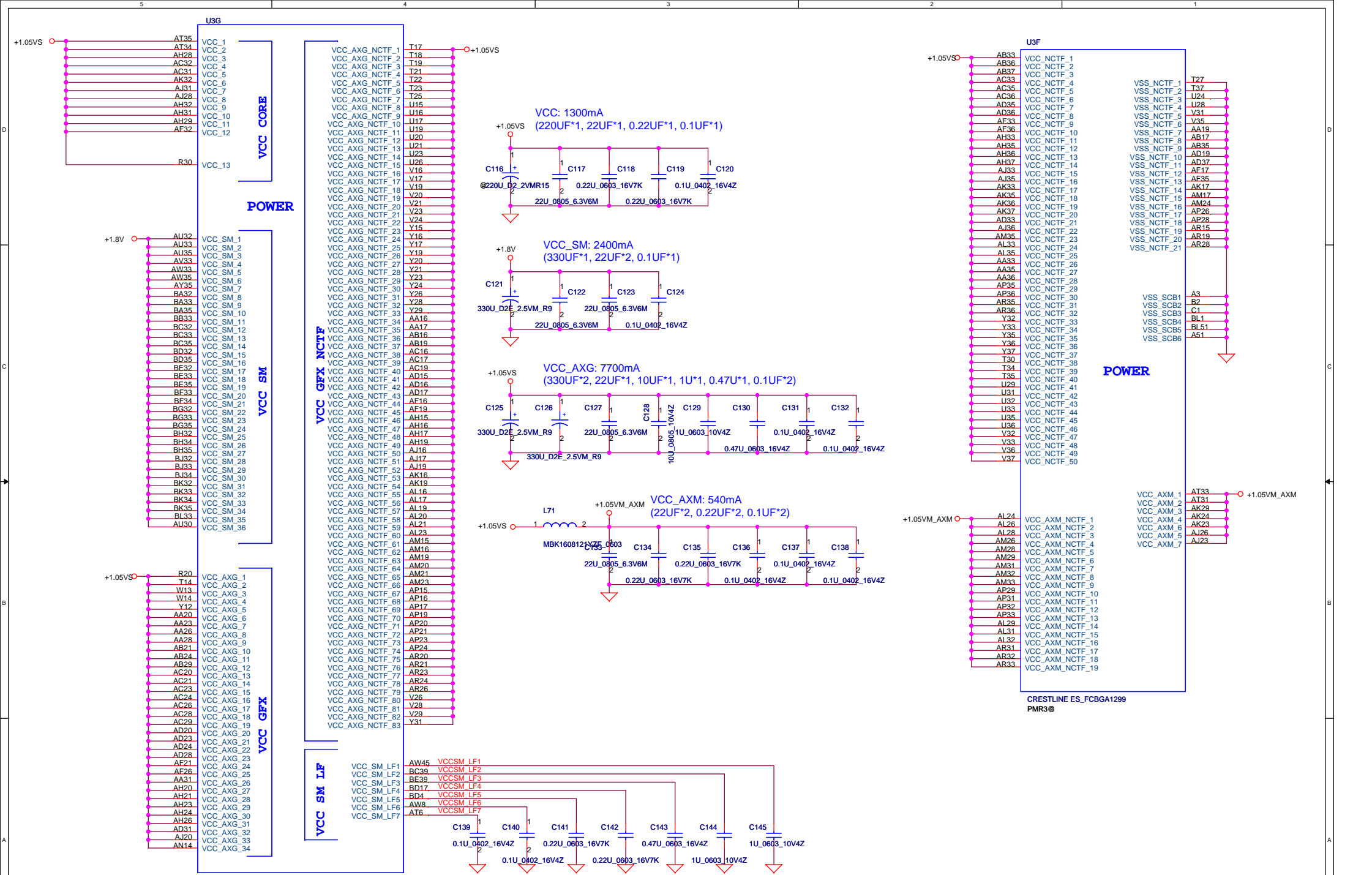
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Date:	Tuesday, May 22, 2007	Sheet	9	of	47



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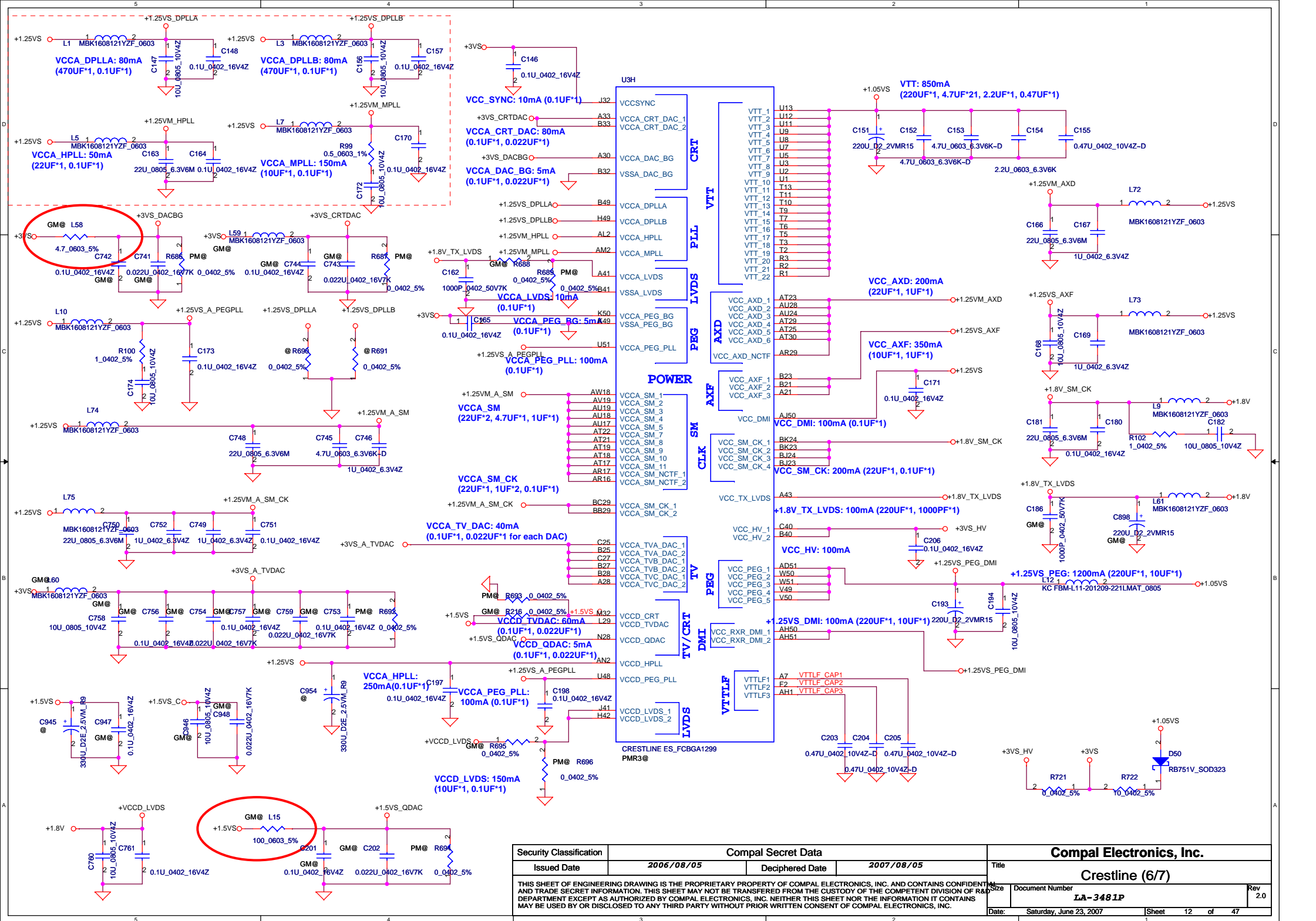
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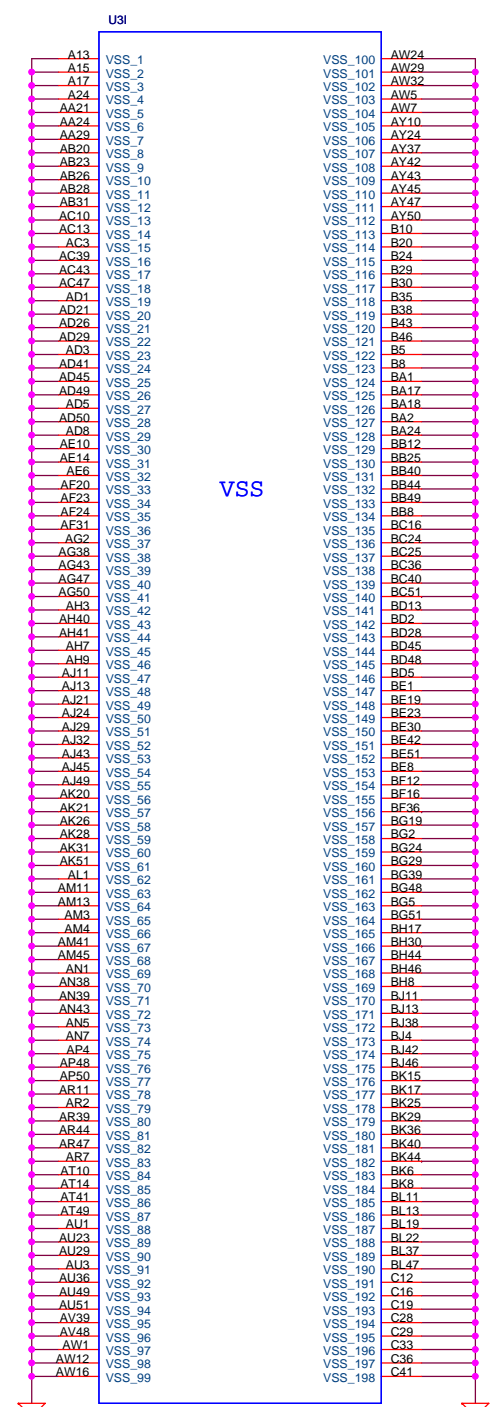


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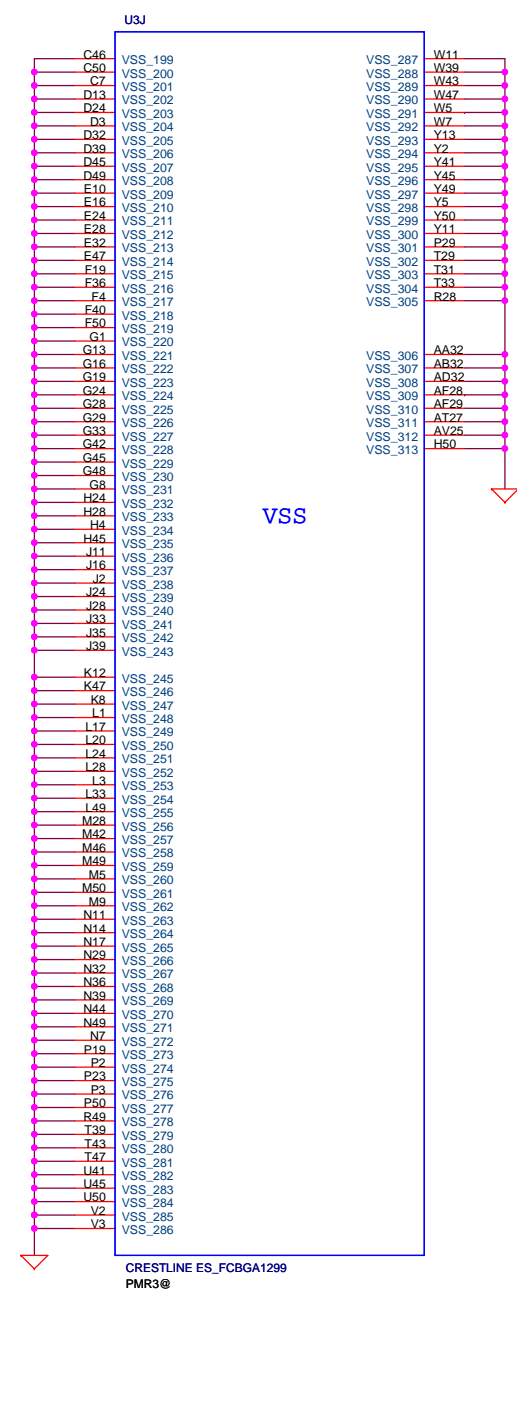
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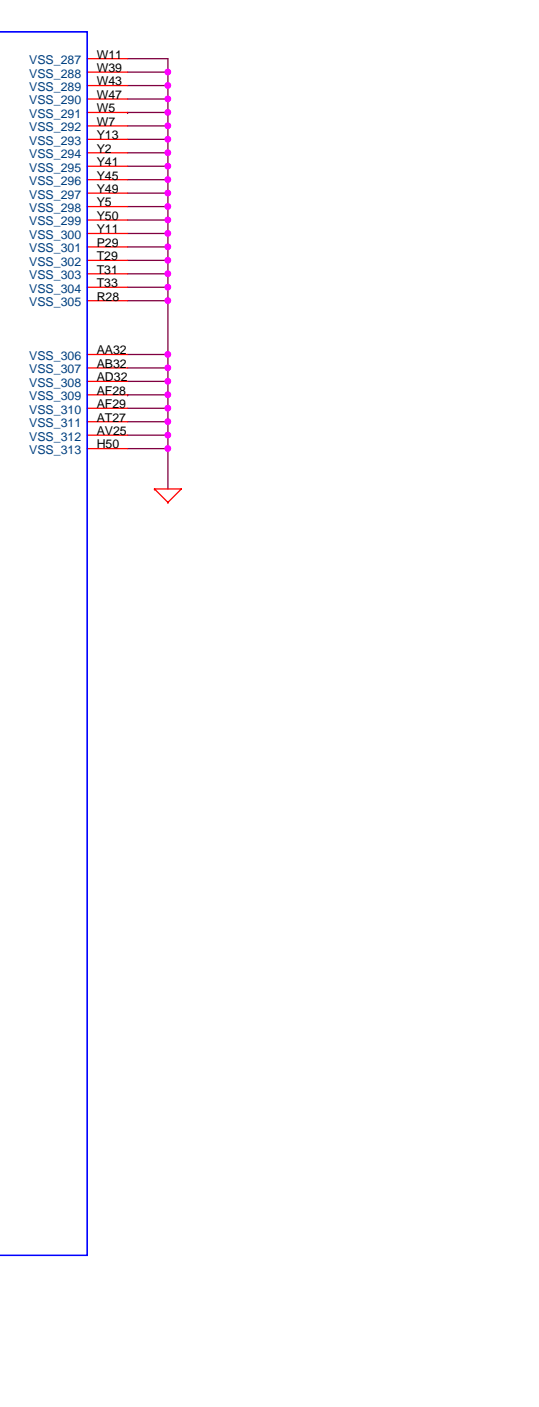
Date	Saturday, June 23, 2007	Sheet	12 of 47
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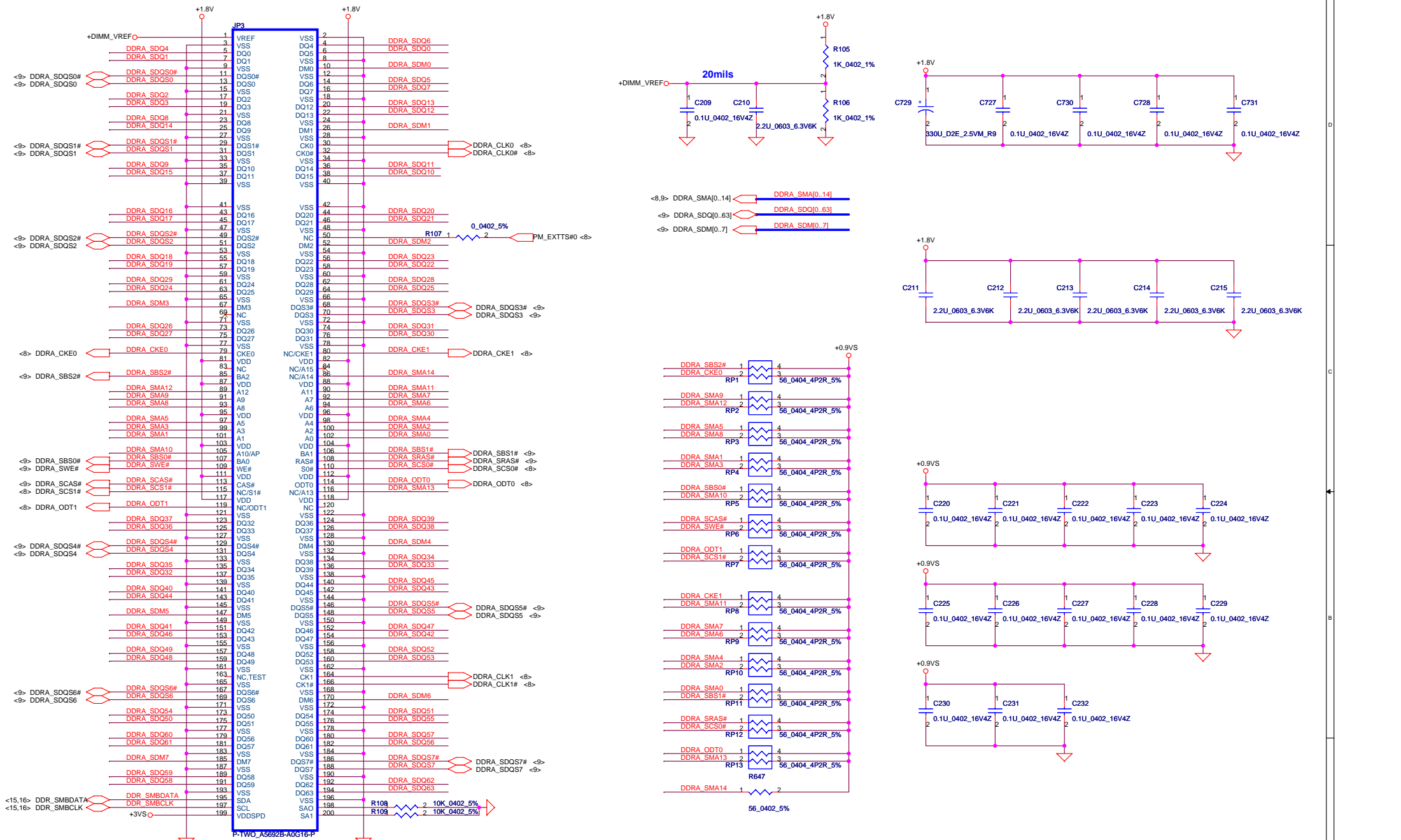


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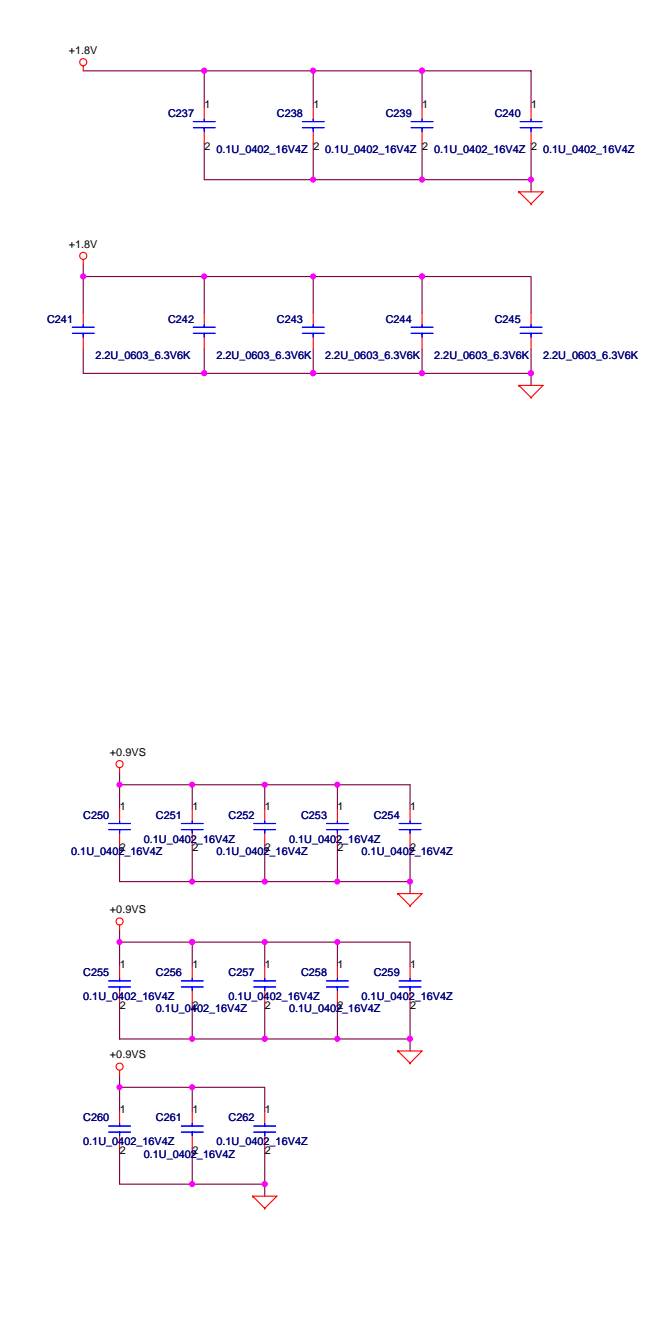
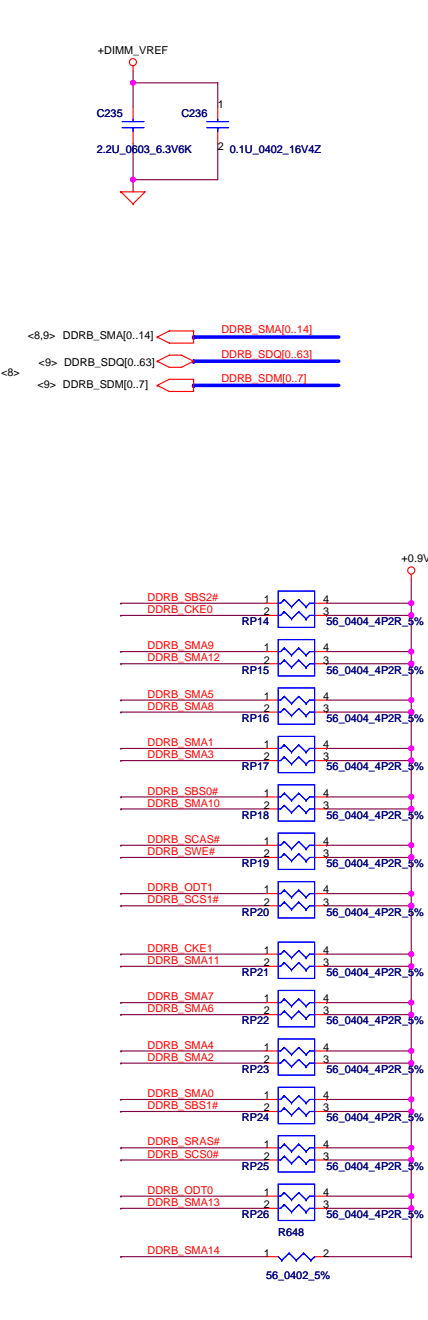
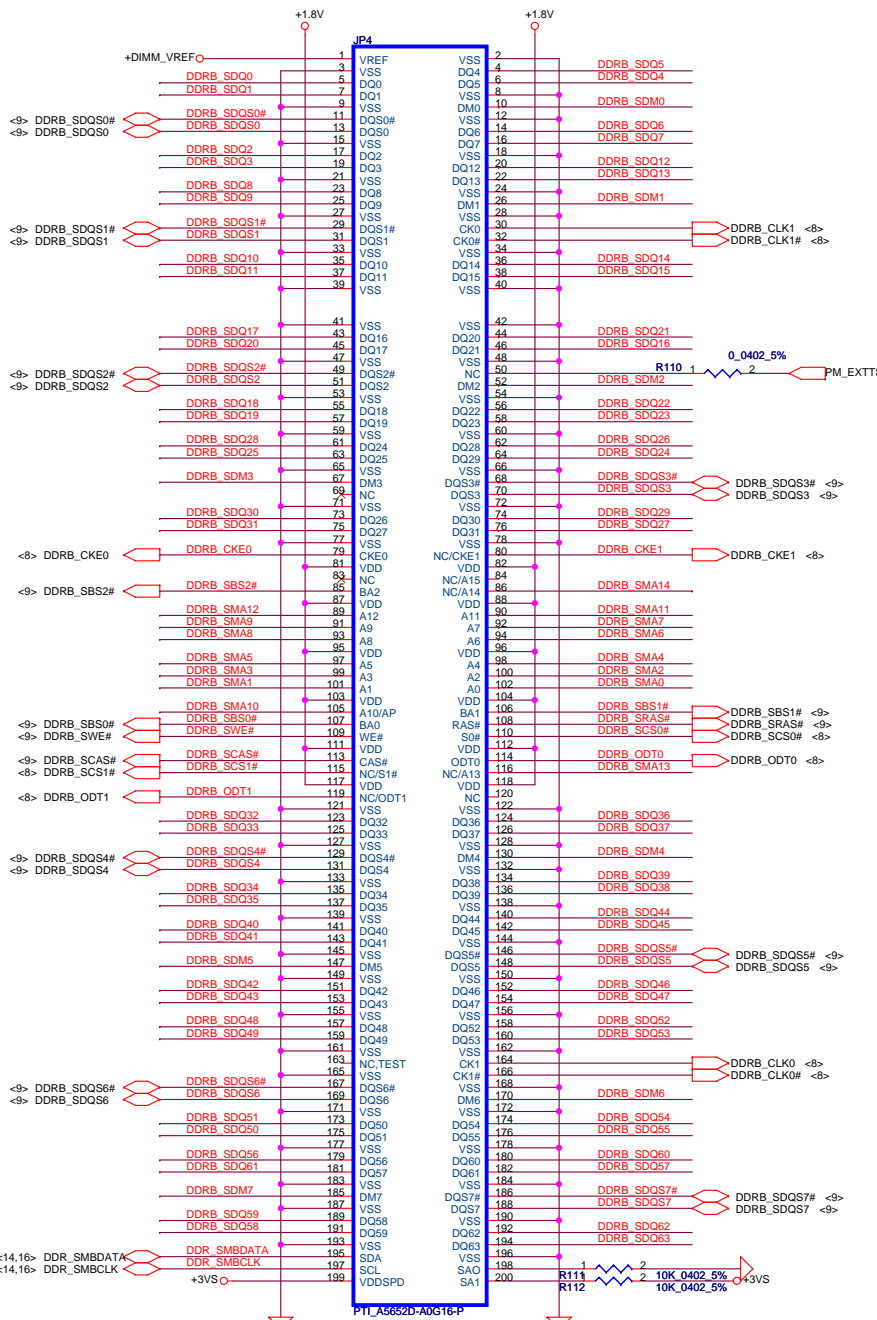
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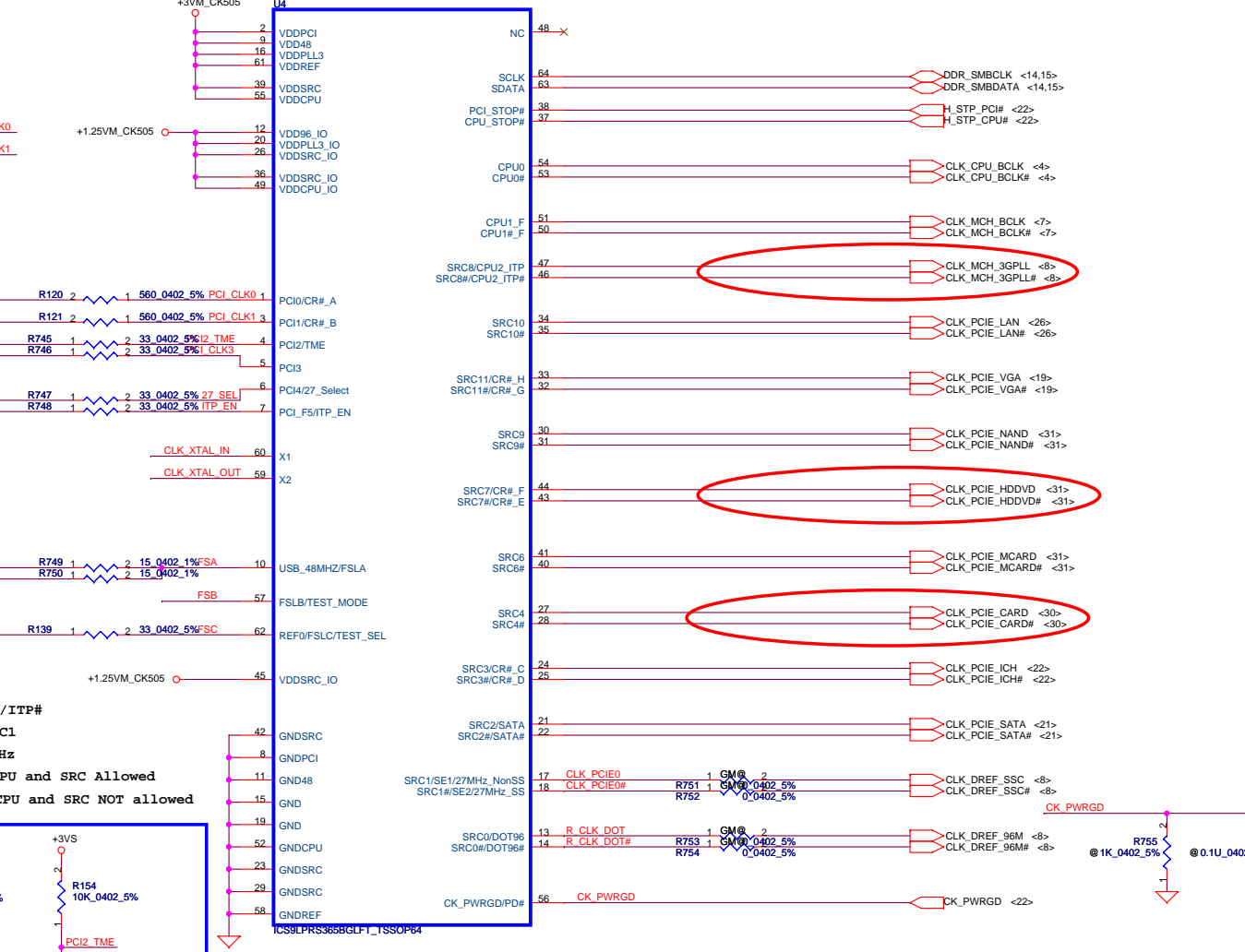
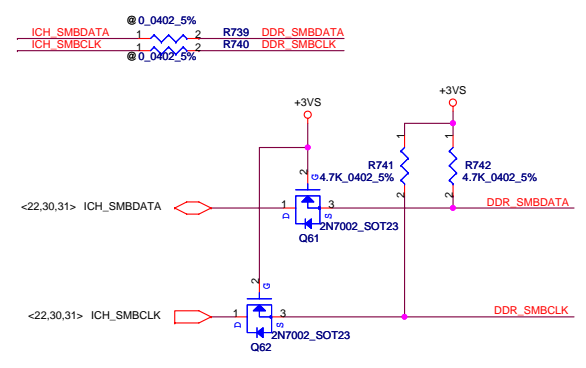
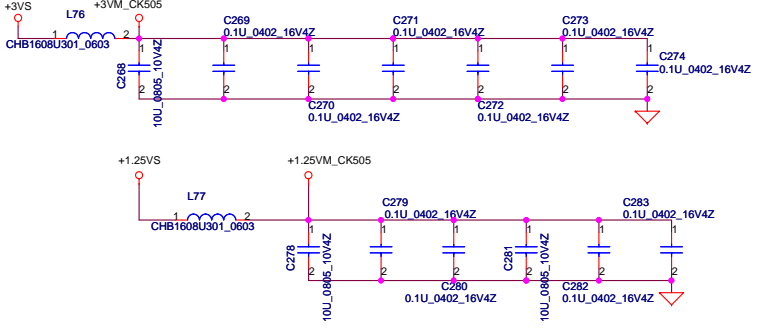
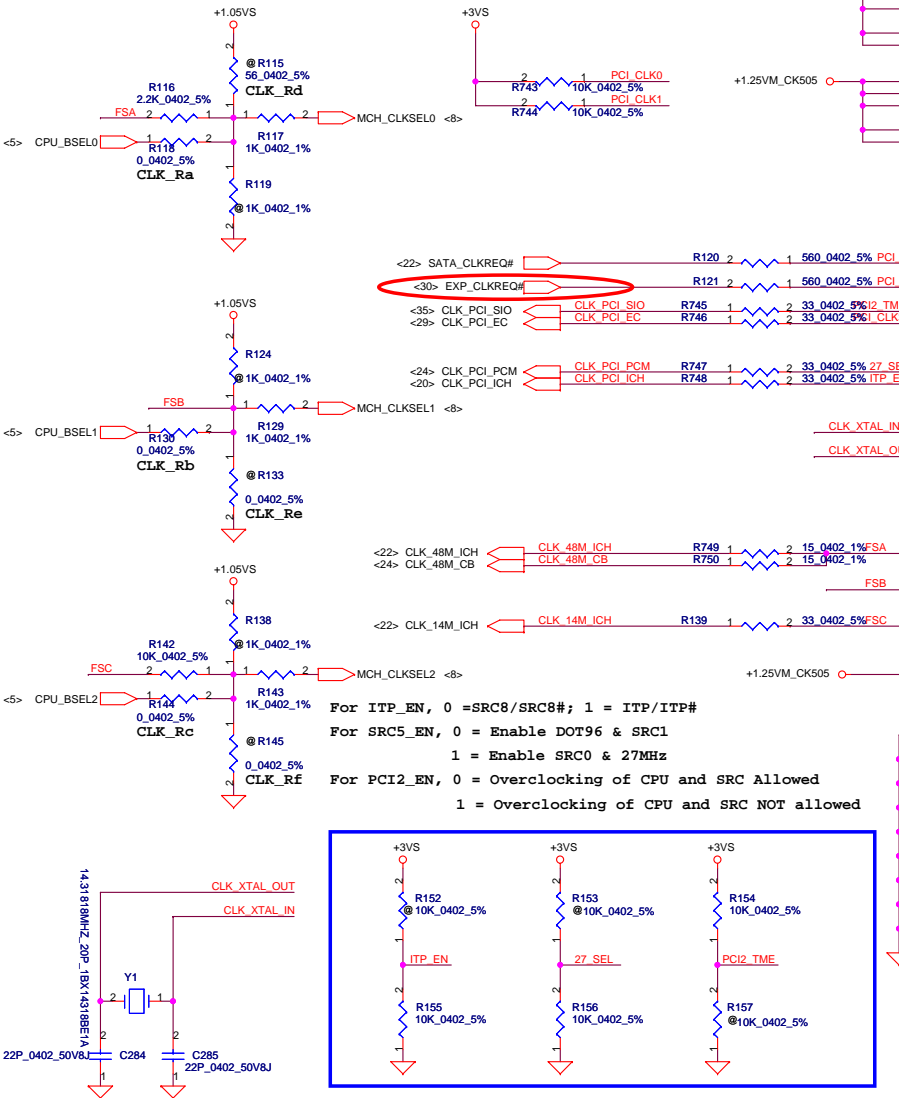
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Date:	Tuesday, May 22, 2007	Sheet	15 of 47	

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

**FSB Frequency Selet:**

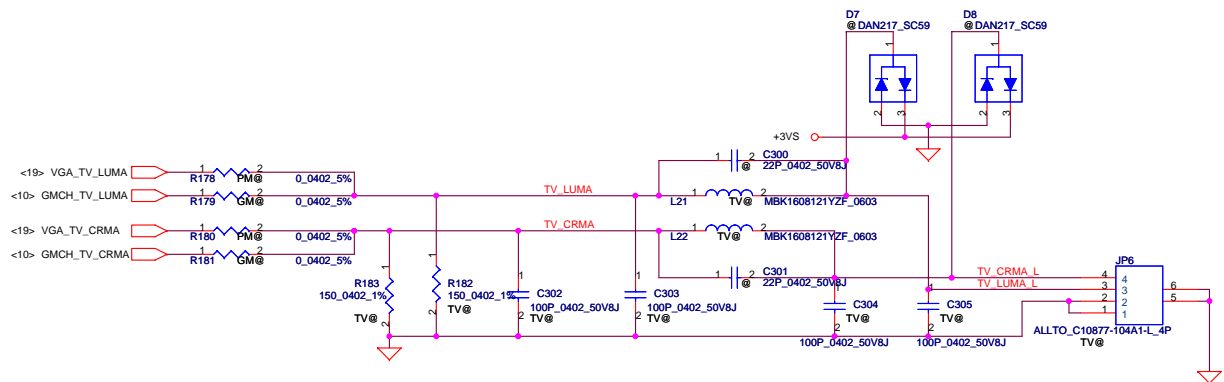
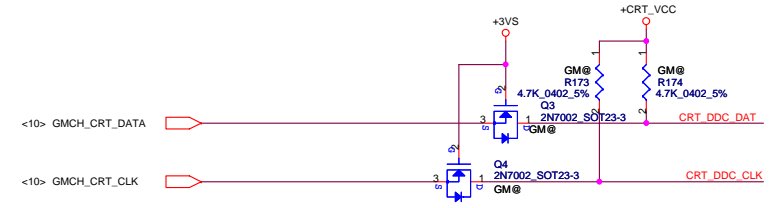
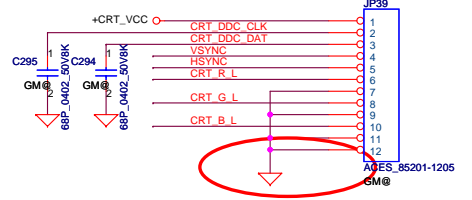
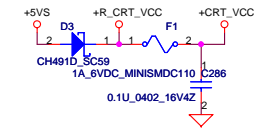
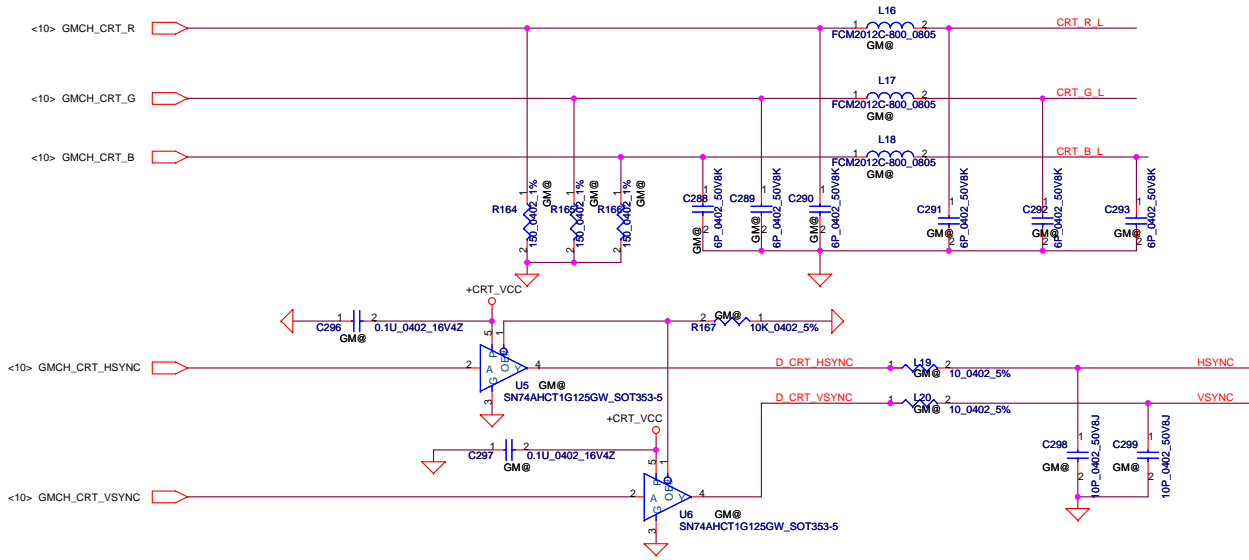
CPU Driven	Stuff	R118	R130	R144
* (Default)	No Stuff	R115	R119	R124 R145
667MHz	Stuff	R1689	R1696	R1734 R1737
	No Stuff	R1694	R1705	R1716 R1719 R1726
800MHz	Stuff			R1734 R1737
	No Stuff	R1689	R1694	R1696 R1705 R1716 R1726 R1719



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Date: Tuesday, May 22, 2007			Rev 2.0
Sheet 16 of 47			

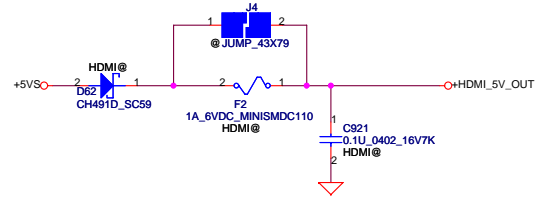
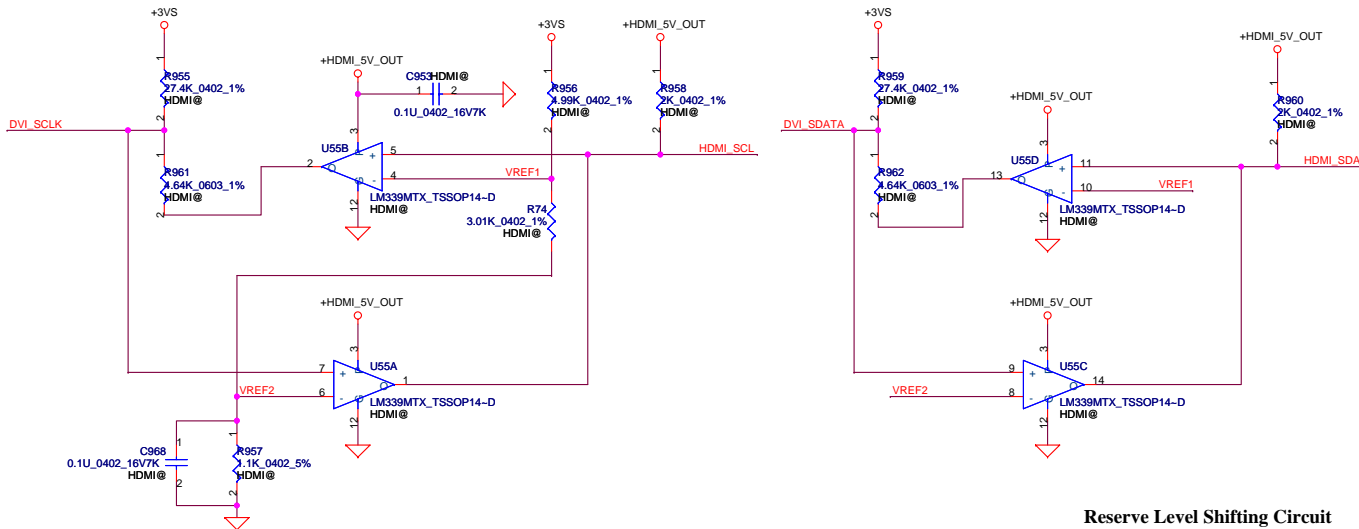


# CRT CONNECTOR

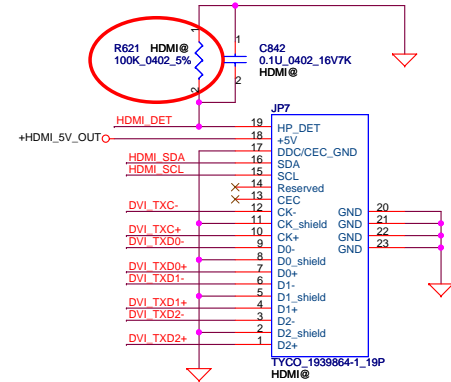


**TV-OUT Conn.**  
 1. Y ground  
 2. C ground  
 3. Y (luminance+sync)  
 4. C (chrominance)

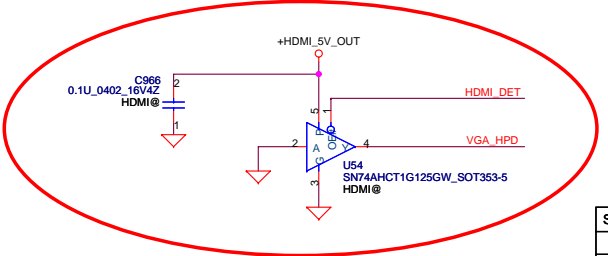
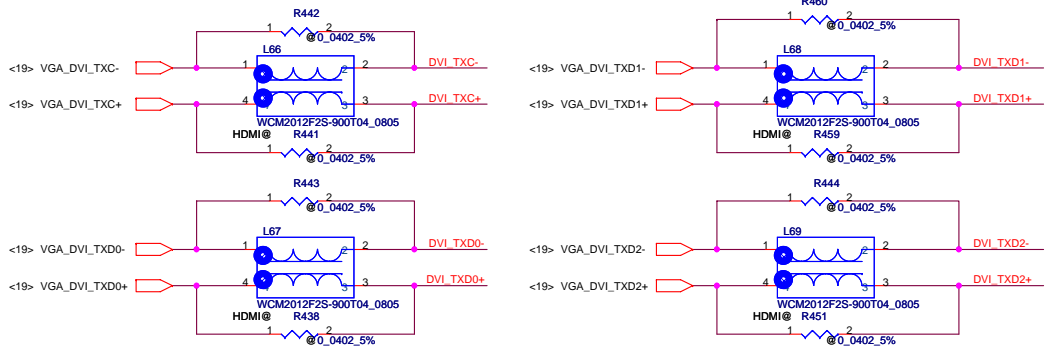
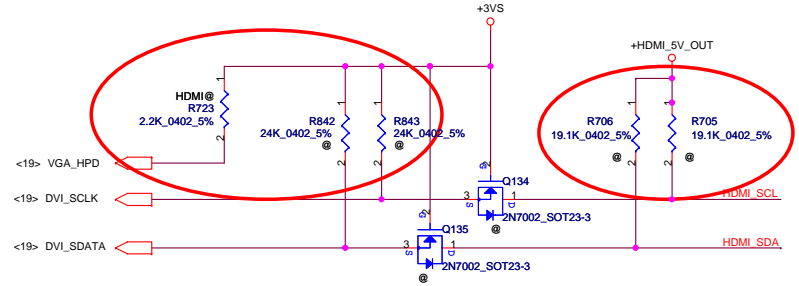
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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	CRT & Tvout Connector	
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Document Number				LA-3481P	Rev	2.0
Date	Wednesday, May 23, 2007	Sheet	17	of	47	



### HDMI Connector



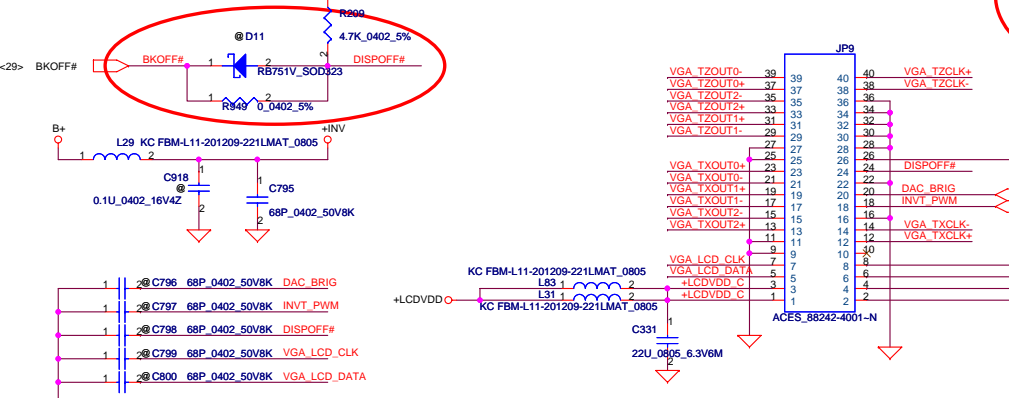
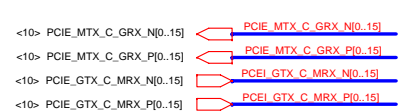
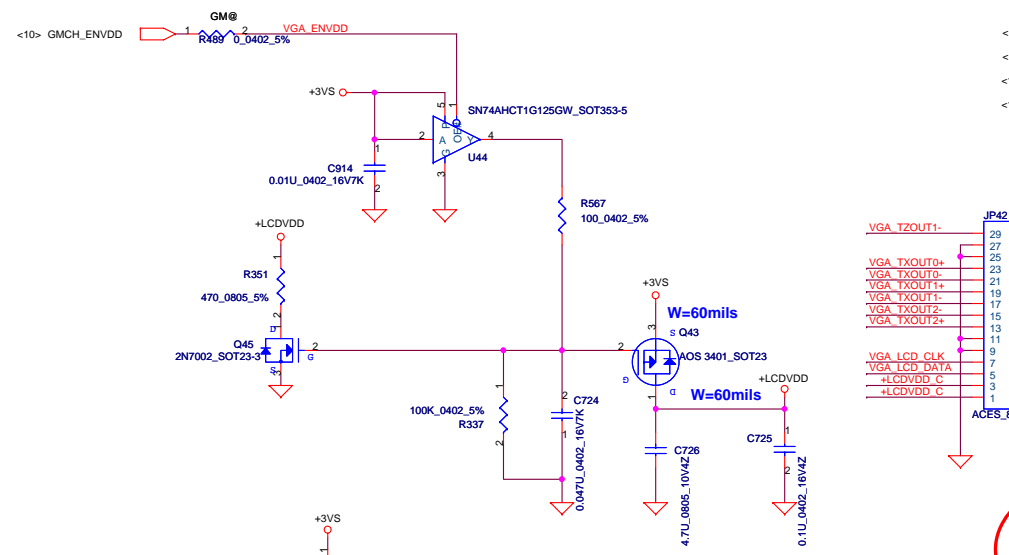
### Reserve Level Shifting Circuit



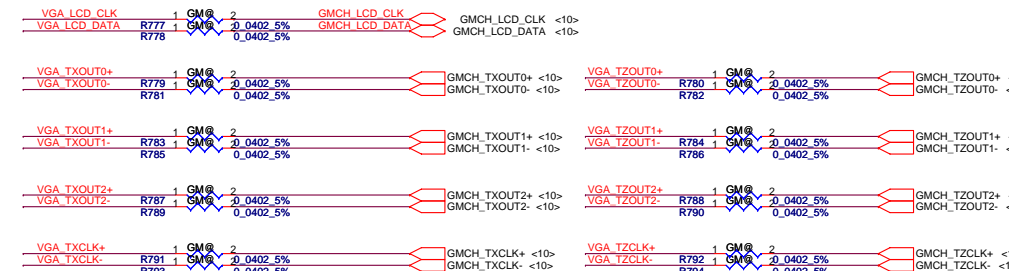
For HDMI Hot Plug Issue

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				LA-3481P	2.0
Date: Saturday, June 23, 2007				Sheet	18 of 47

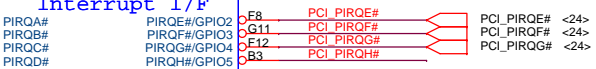
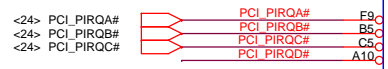
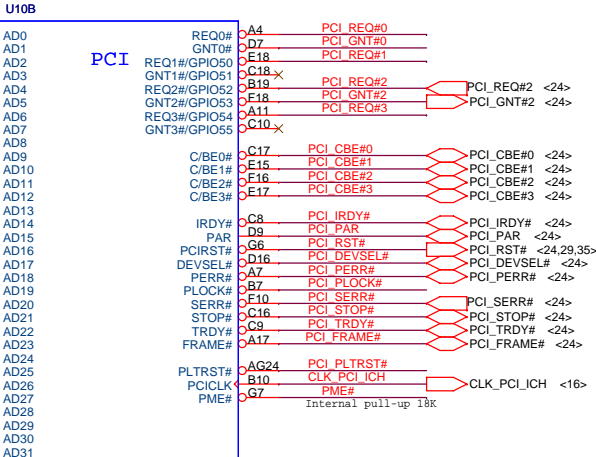
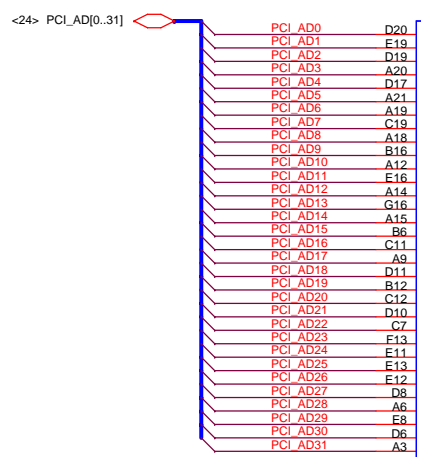
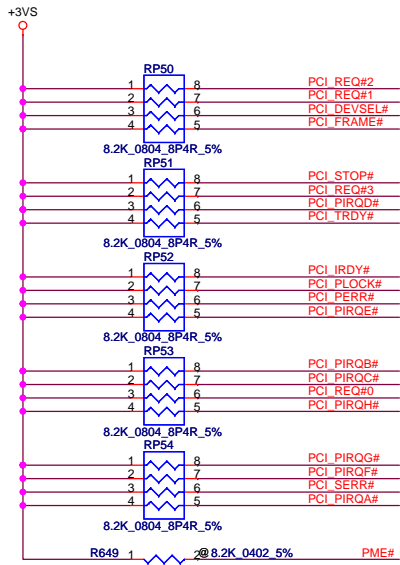
# LCD POWER CIRCUIT



ALL R CLOSE TO VGA CONNECTOR

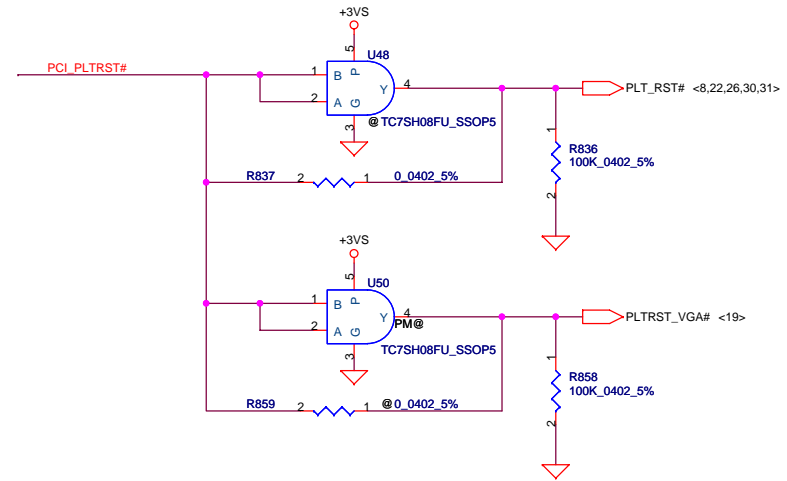
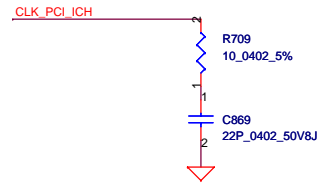


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Document Number	LA-3481P	Rev	2.0	Date	Saturday, June 23, 2007
			Sheet	19	of 47

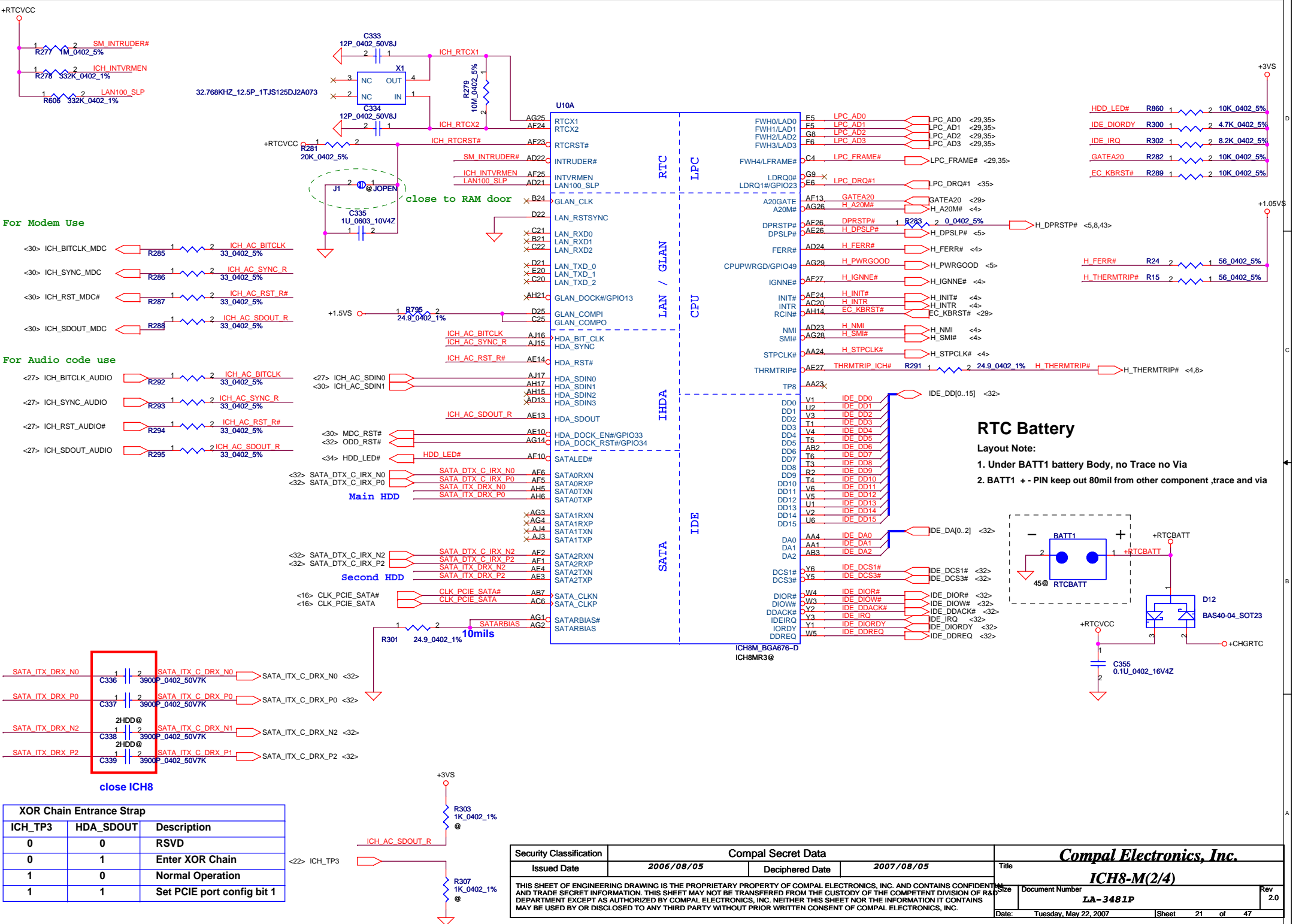


ICH8M\_BGA676-D  
ICH8MR3@

PCI_GNT0#	SPI_CS#0	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

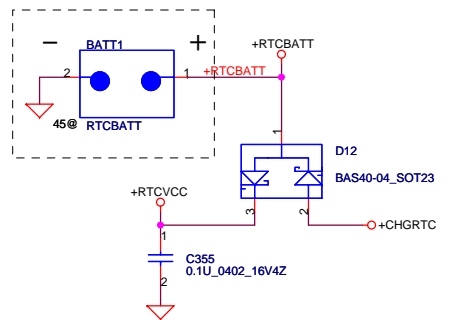


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				ICH8-M(1/4)	
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				LA-3481P	2.0
Date:	Tuesday, May 22, 2007	Sheet	20	of	47

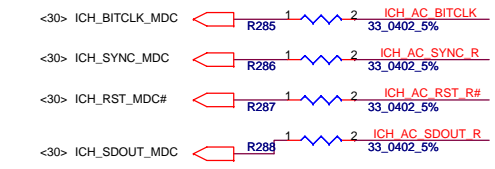


### RTC Battery

- Layout Note:**
- Under BATT1 battery Body, no Trace no Via
  - BATT1 + - PIN keep out 80mil from other component ,trace and via



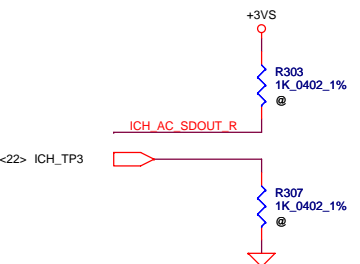
#### For Modem Use



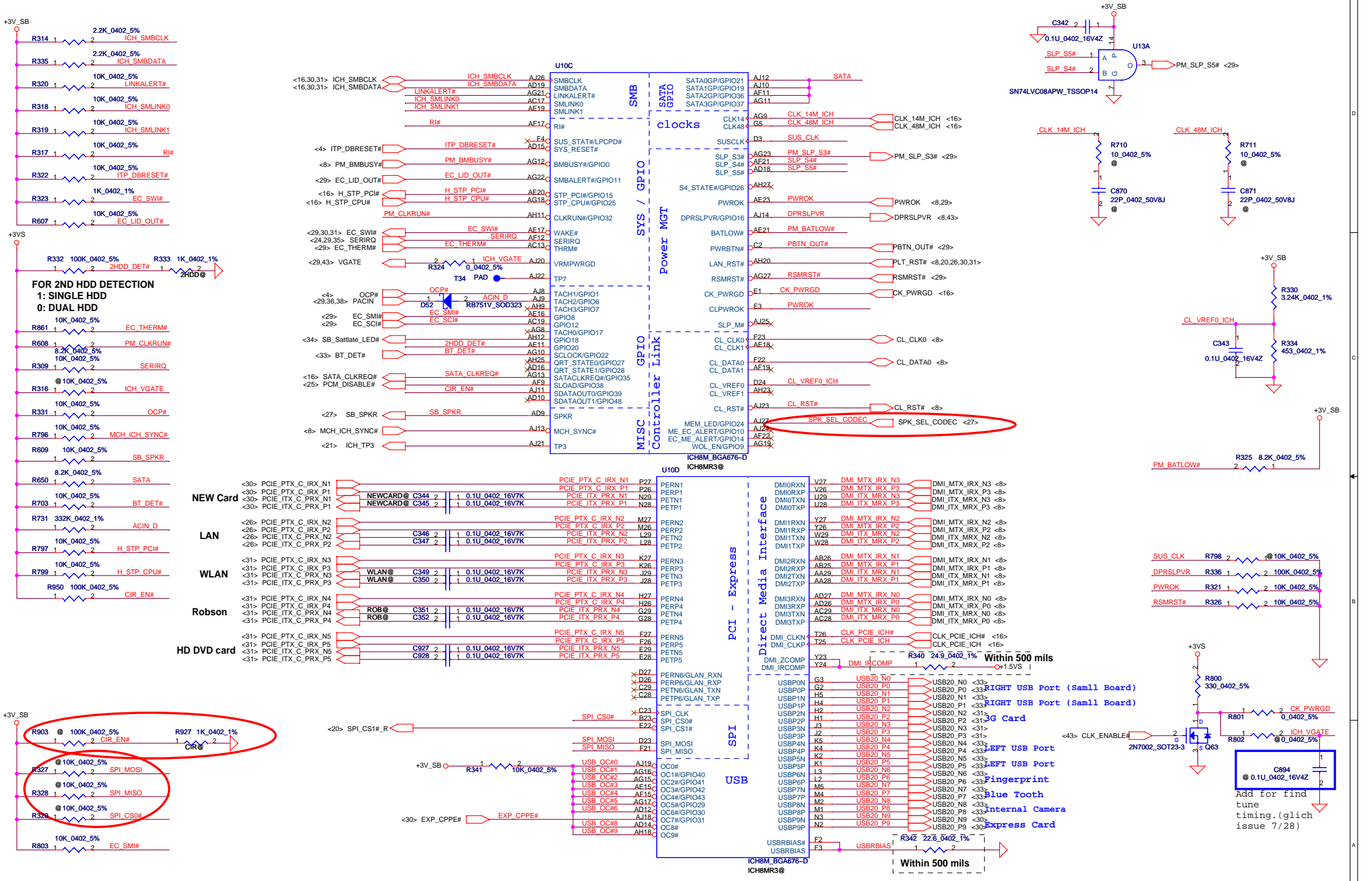
#### For Audio code use



ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIe port config bit 1



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Date: Tuesday, May 22, 2007				Sheet 21 of 47	

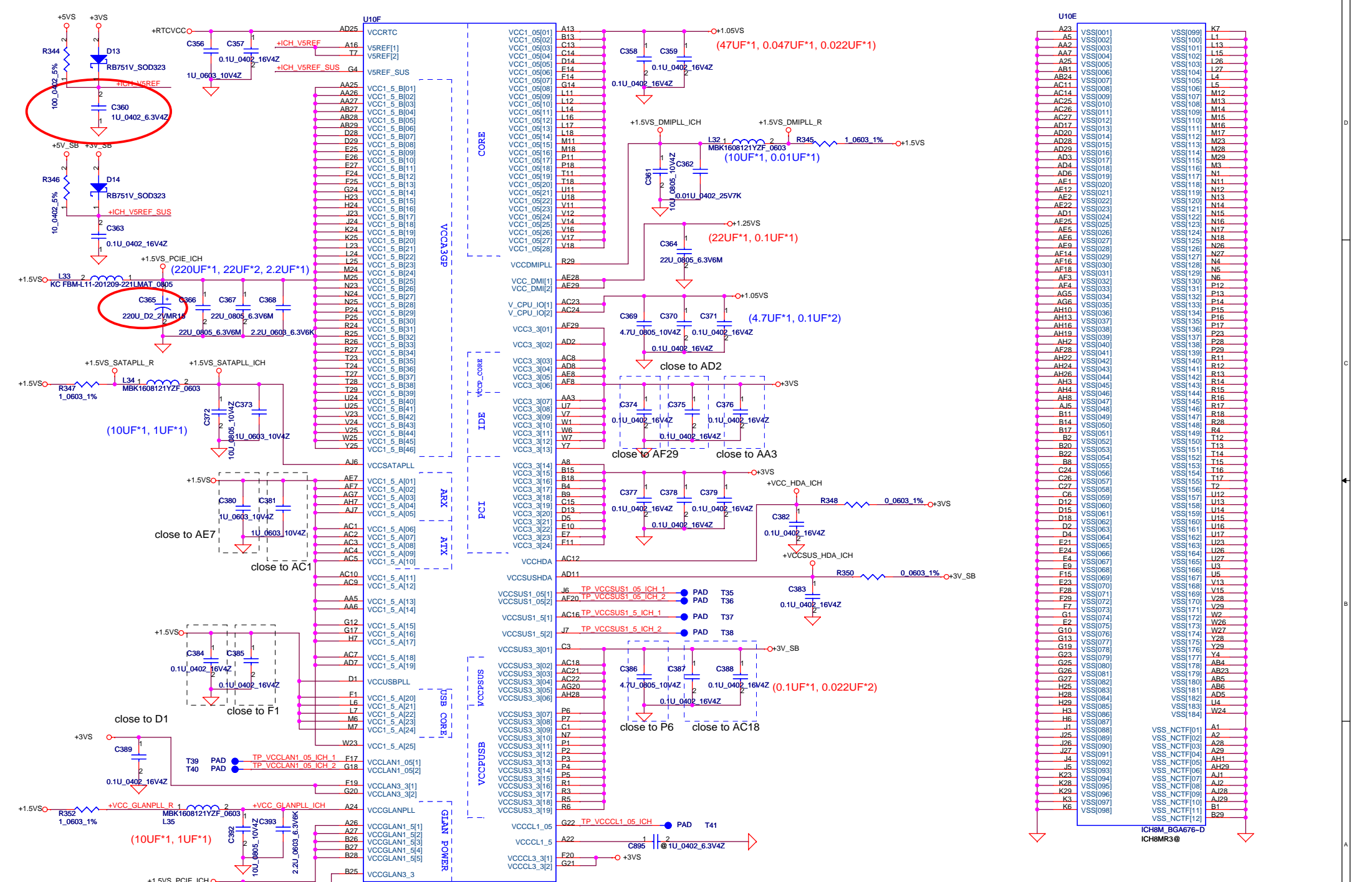


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Date	Saturday, June 23, 2007	Sheet	22 of 47

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**ICH8-M(3/4)**

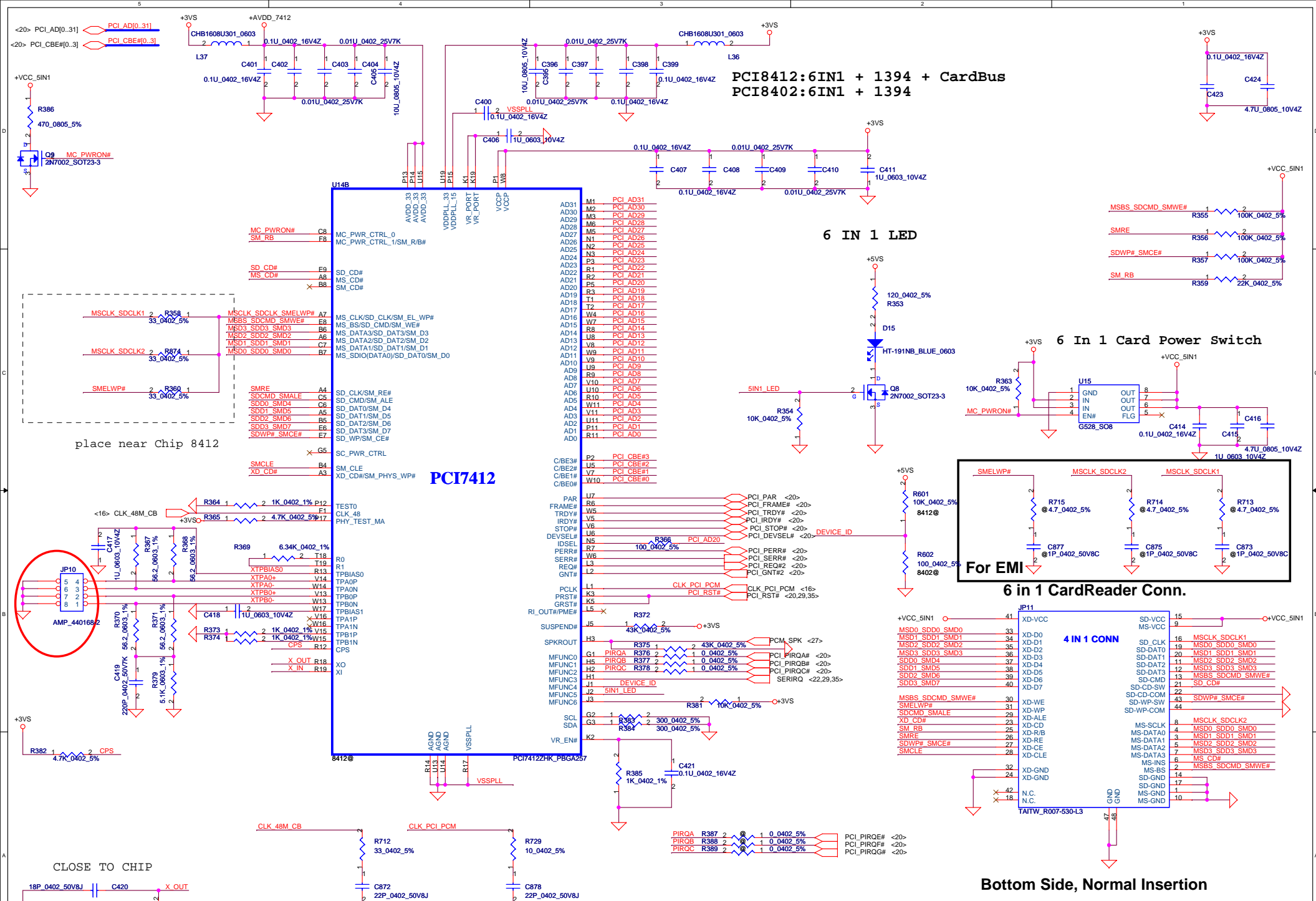
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<b>ICH8-M(4/4)</b>	
Document Number	Rev 2.0
LA-3481P	
Date: Monday, May 28, 2007	Sheet 23 of 47



PCI8412:6IN1 + 1394 + CardBus  
 PCI8402:6IN1 + 1394

6 IN 1 LED

6 In 1 Card Power Switch

6 in 1 CardReader Conn.  
 For EMI

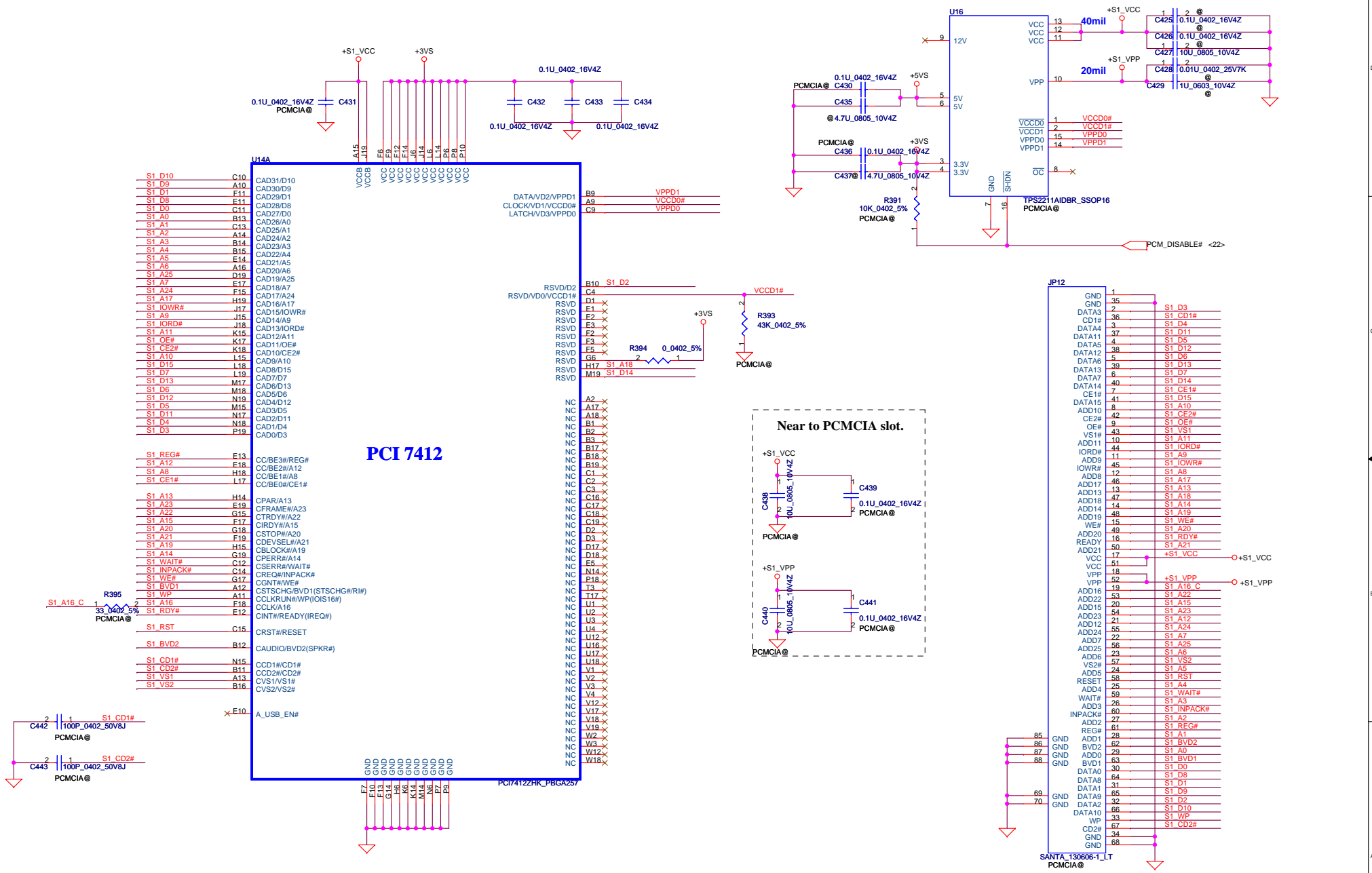
4 IN 1 CONN

Bottom Side, Normal Insertion

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				LA-3481P	2.0
Date: Tuesday, May 22, 2007				Sheet	24 of 47



# CardBus Power Switch

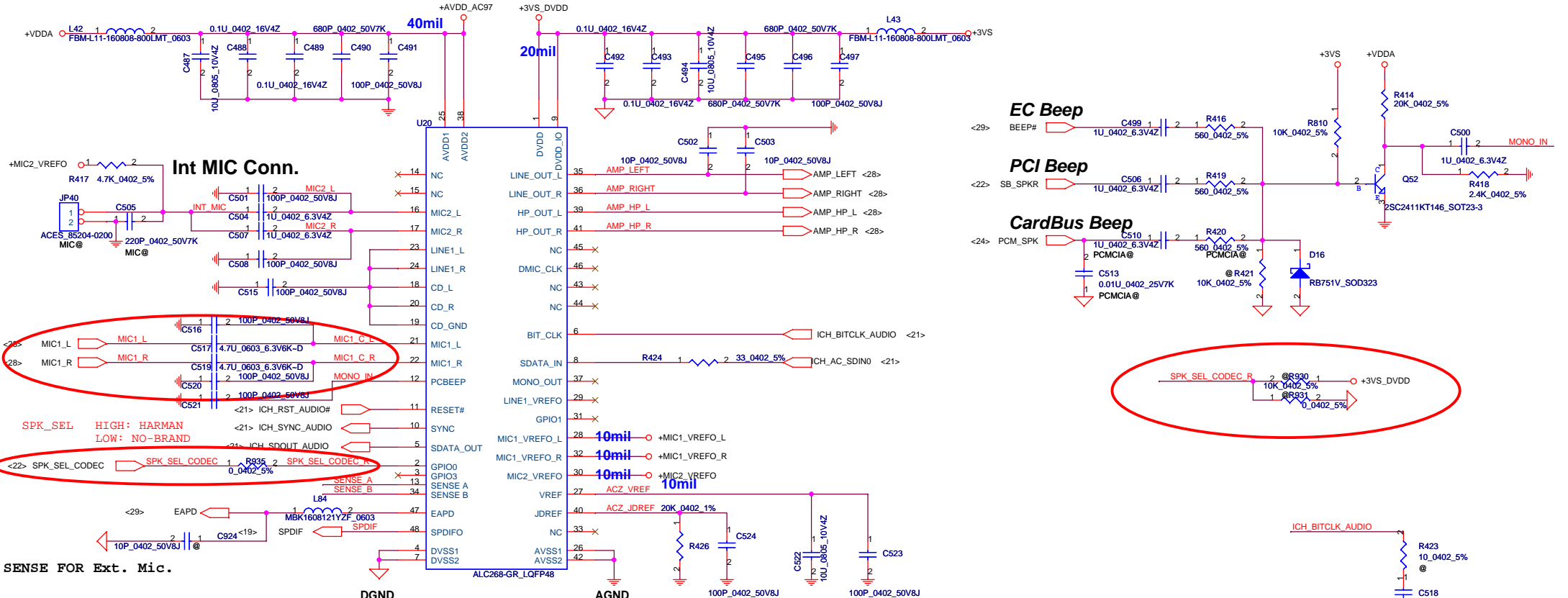


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Issued Date	2006/08/05	Deciphered Date	2007/08/05	<b>TI PC18412/CB socket</b>	
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Date: Tuesday, May 22, 2007				Sheet	25 of 47

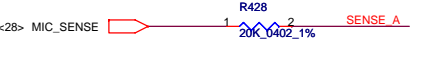
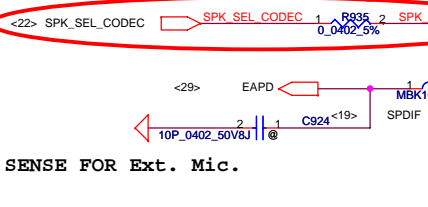
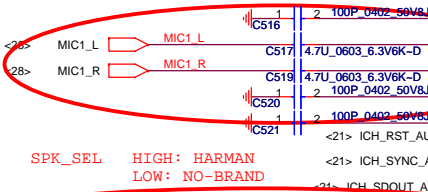
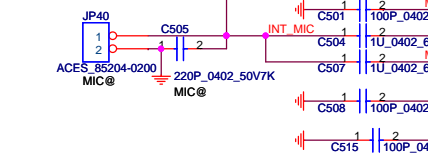
LA-3481P  
Rev 2.0



# HD Audio Codec

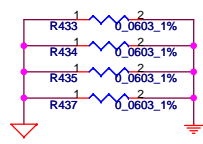


## Int MIC Conn.



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

## Moat Bridge



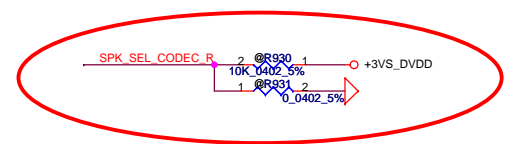
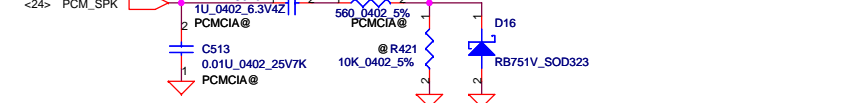
## EC Bleep



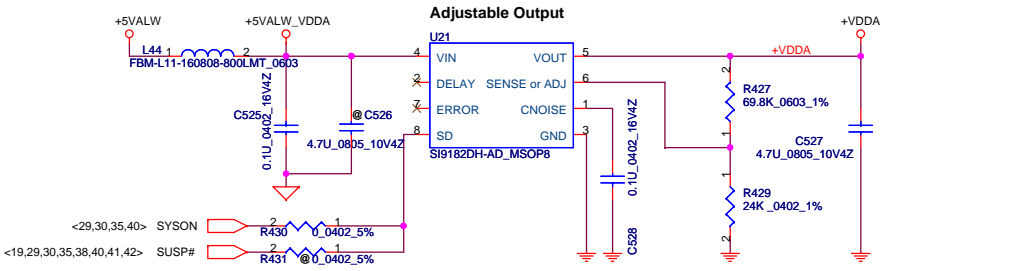
## PCI Bleep



## CardBus Bleep



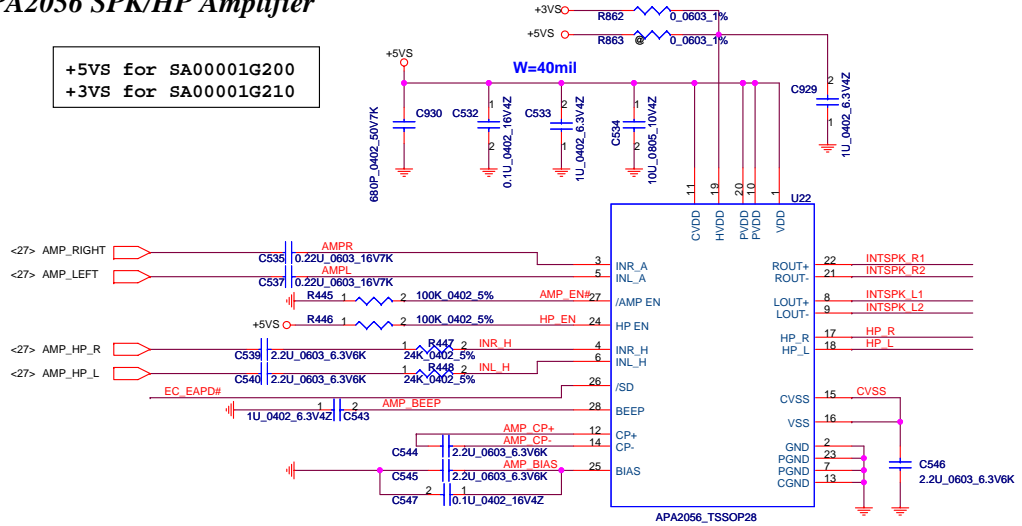
## Regulator for CODEC



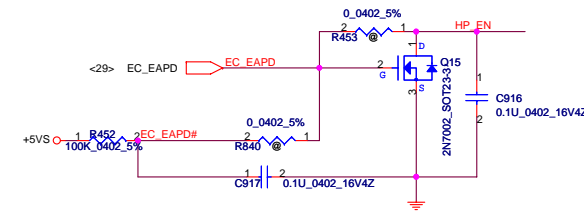
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Size	Document Number	Rev		
	LA-3481P	2.0		
Date:	Tuesday, May 22, 2007	Sheet	27 of 47	

# APA2056 SPK/HP Amplifier

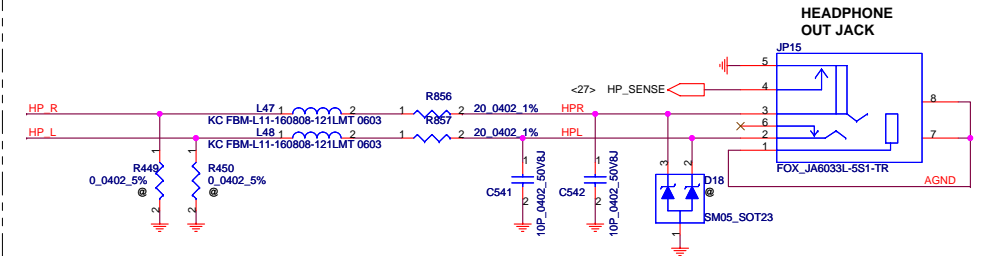
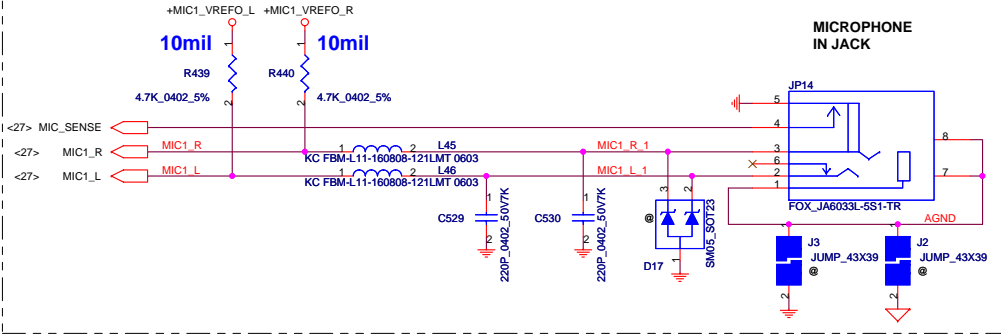
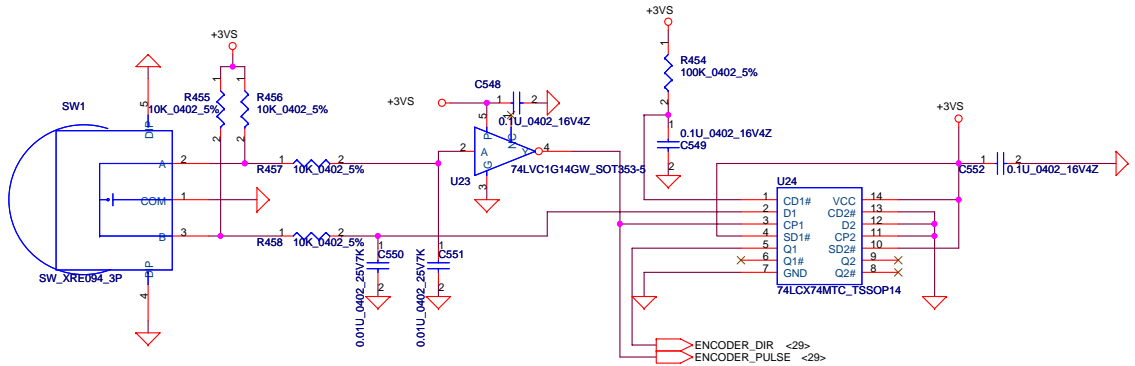
**+5VS for SA00001G200**  
**+3VS for SA00001G210**



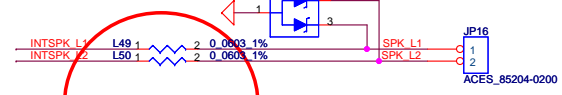
**IN\_A Gain = 10dB (Internal Speaker)**  
**IN\_H Gain = 0dB (Headphone)**



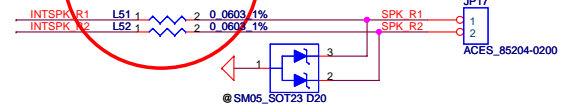
## Volume Control



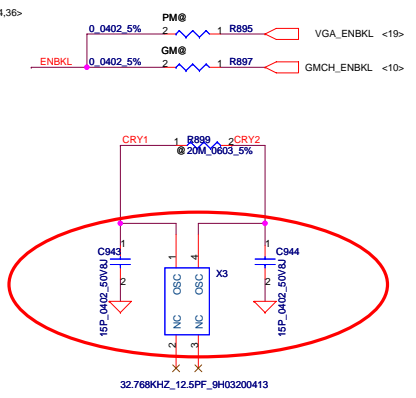
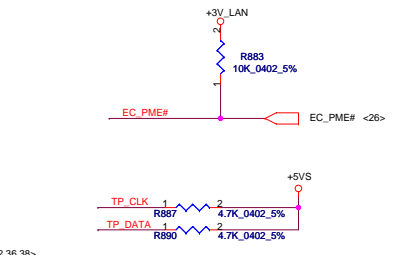
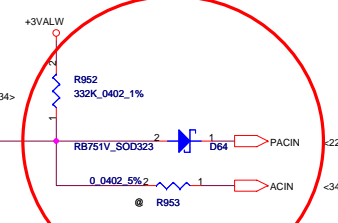
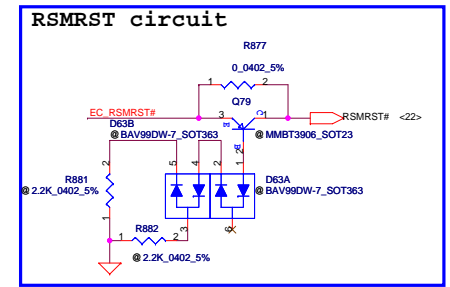
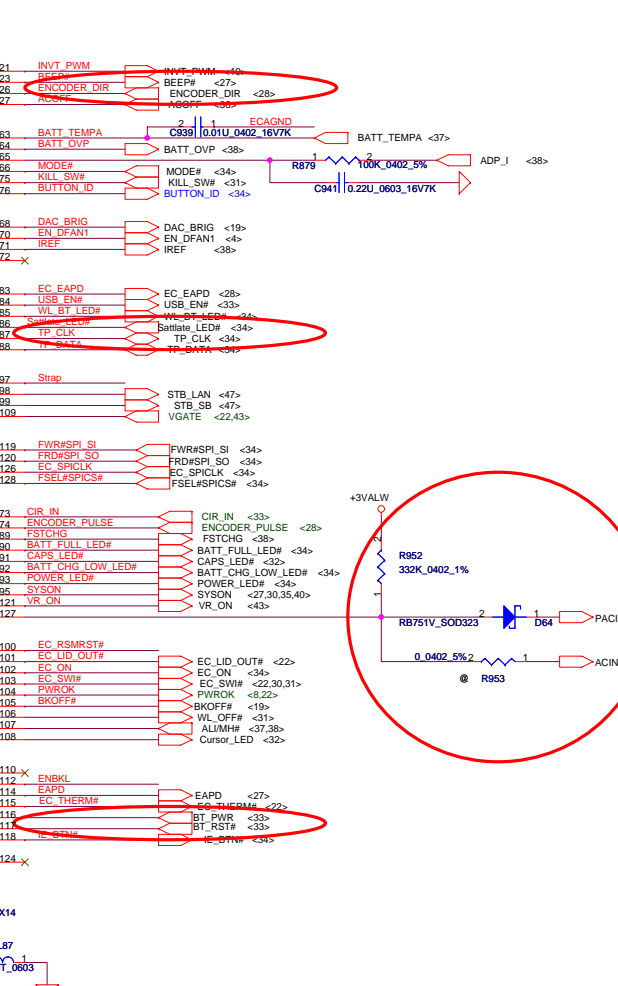
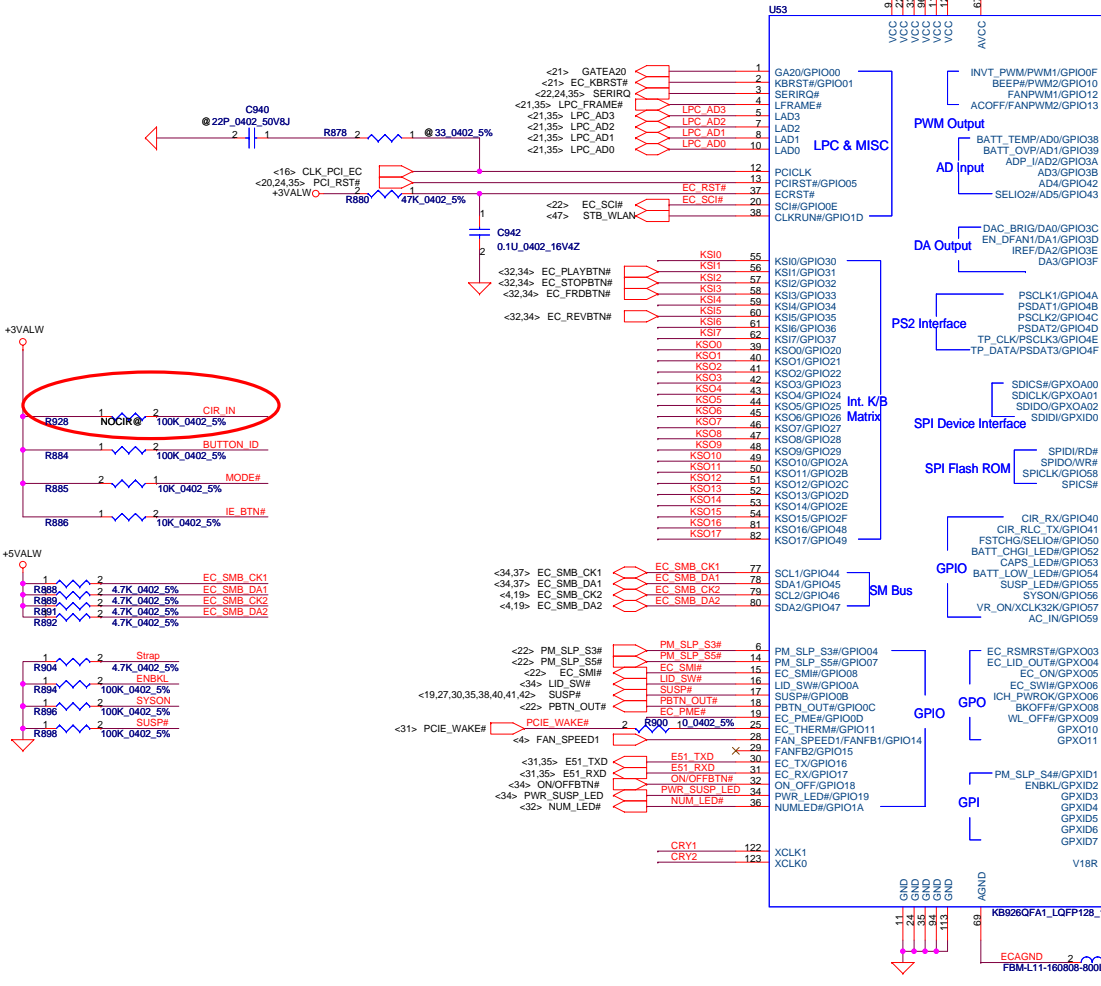
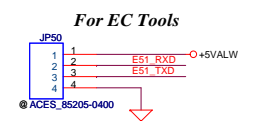
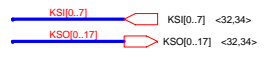
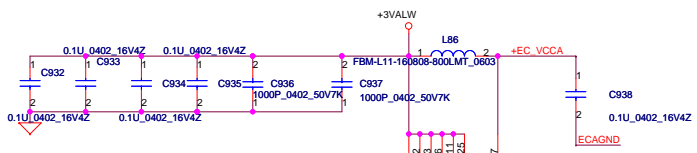
## Right Speaker Connector



## Left Speaker Connector

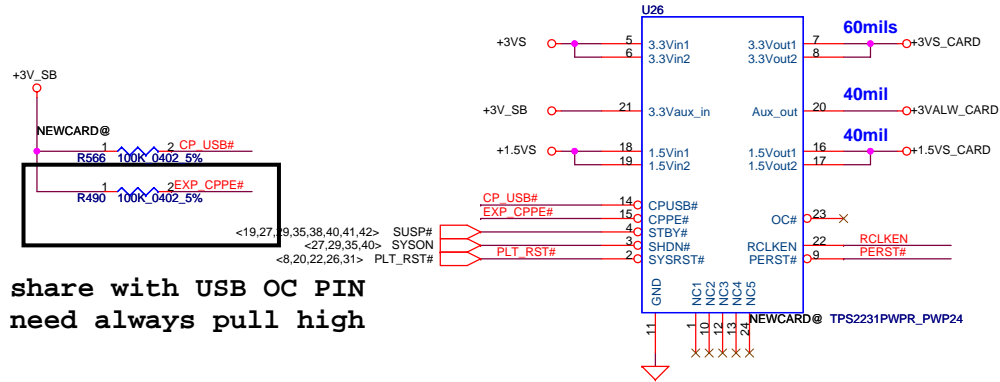


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Document Number			Rev	
LA-3481P			2.0	
Date: Saturday, June 02, 2007			Sheet 28 of 47	

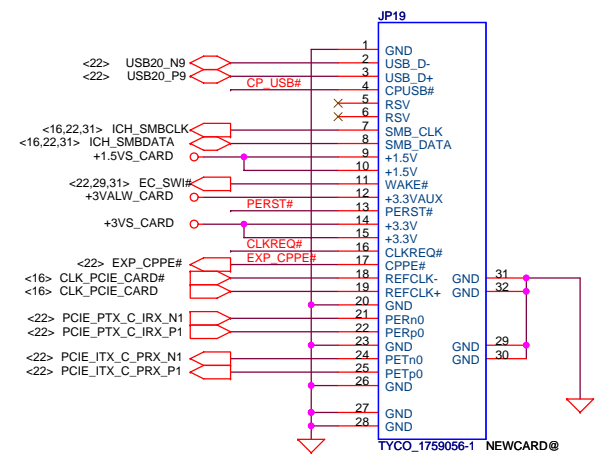
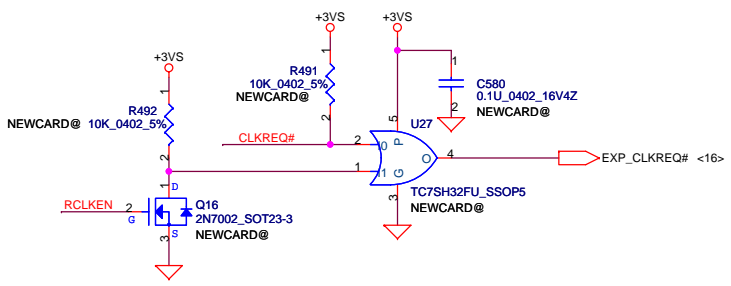
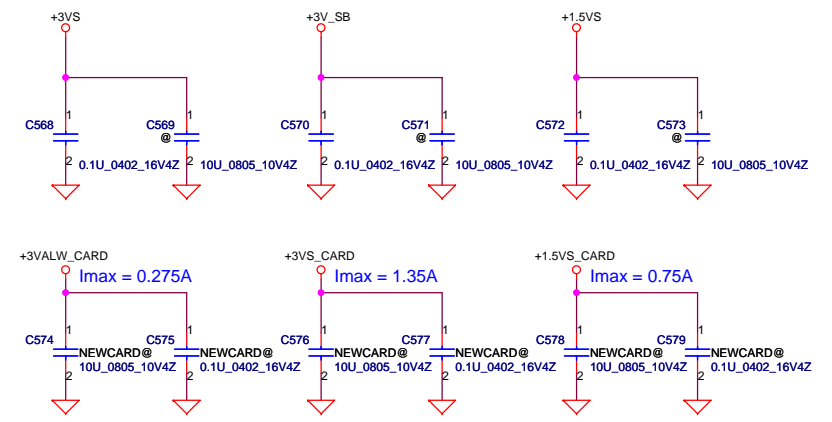


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LA-3481P				Sheet 29 of 47

# New Card

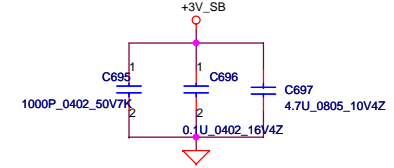
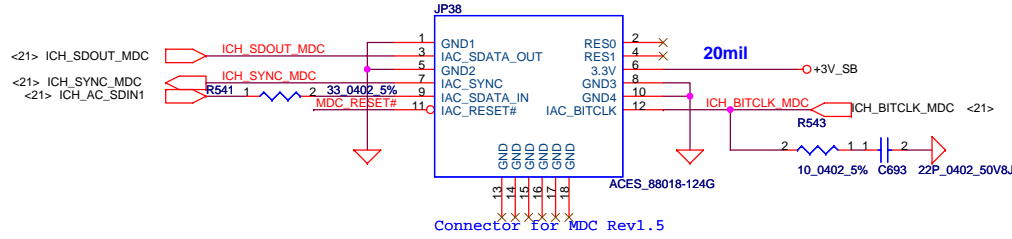
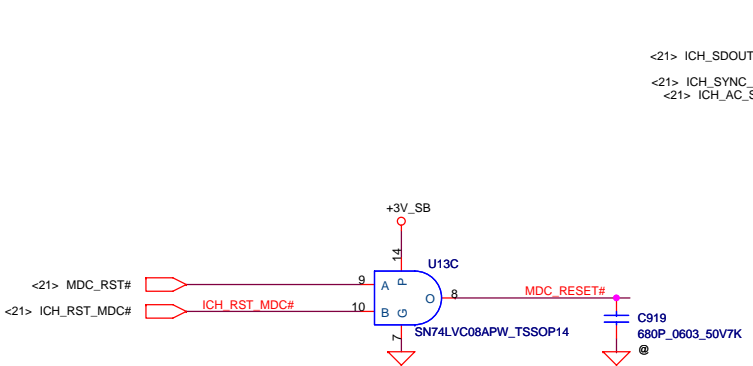


share with USB OC PIN  
need always pull high



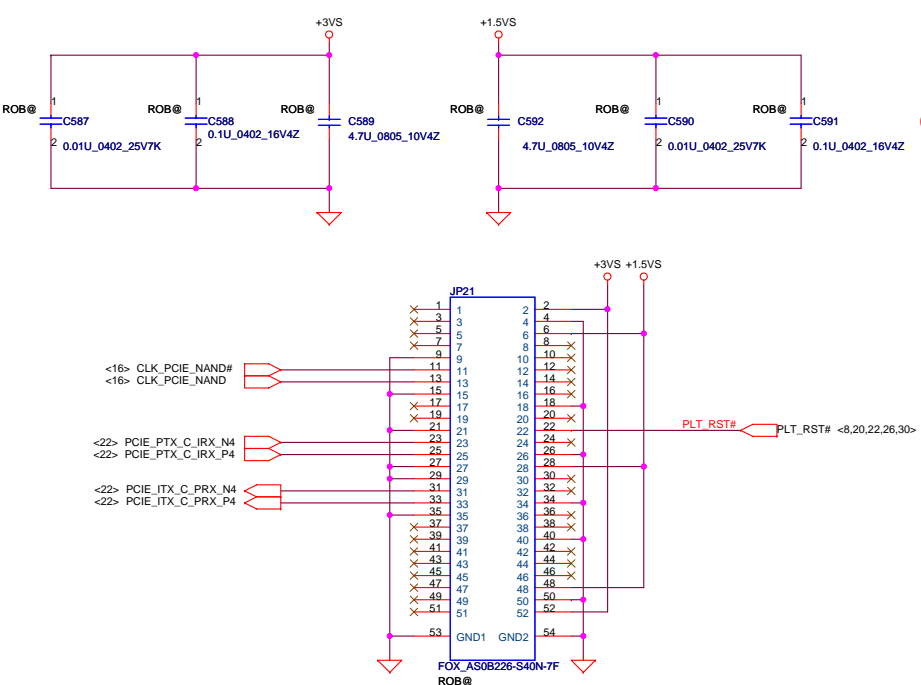
# MDC

## MDC Conn.

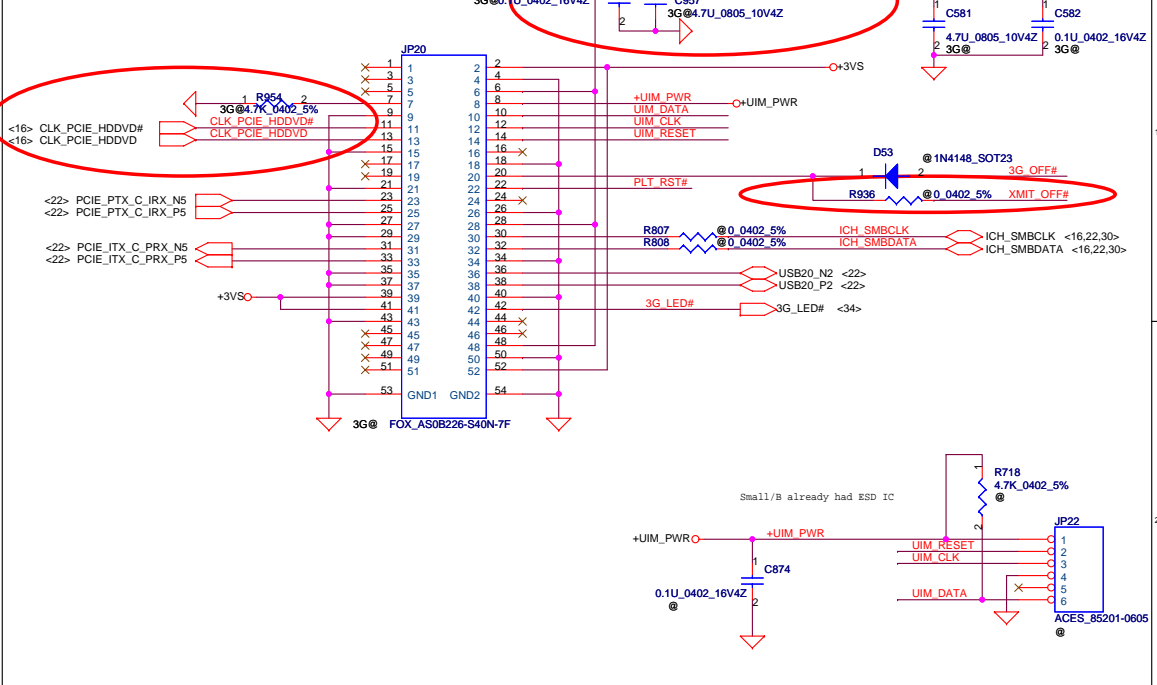


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				LA-3481P	
Date	Tuesday, May 22, 2007	Sheet	30	of	47

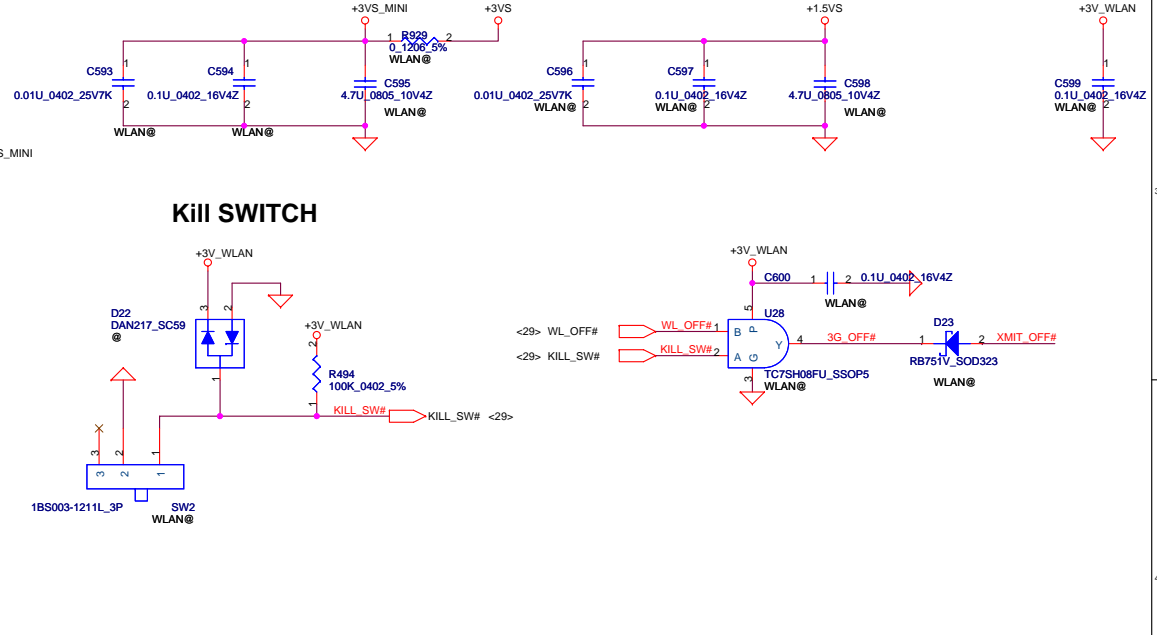
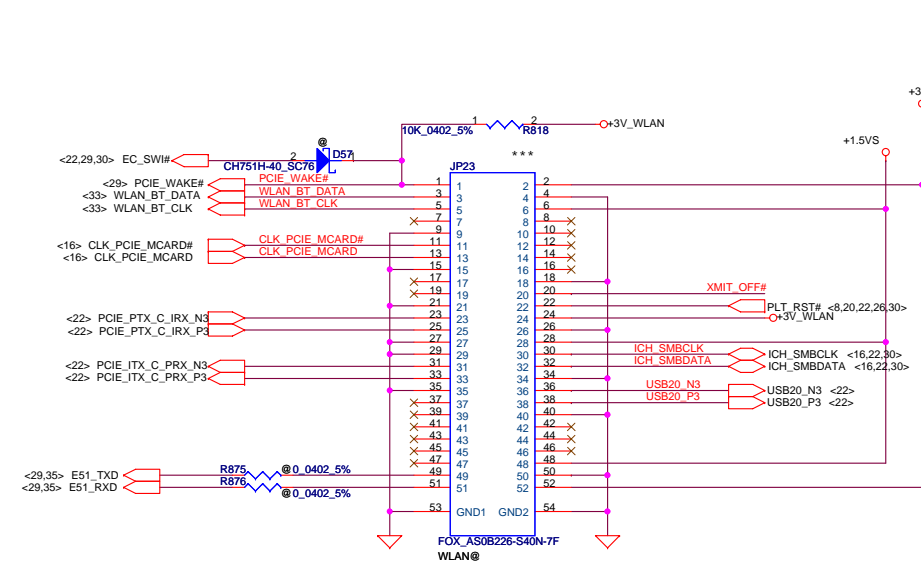
# NAND mini Card(Robson support)



# Mini-Express Card for 3G

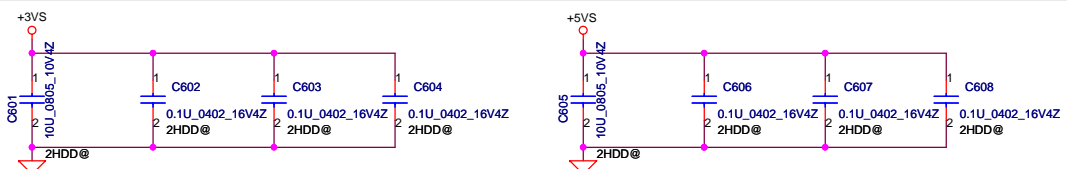


# Mini-Express Card for WLAN

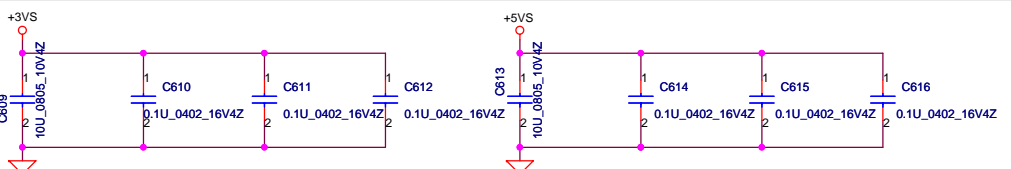


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				LA-3481P	2.0
Date: Tuesday, May 22, 2007				Sheet	31 of 47



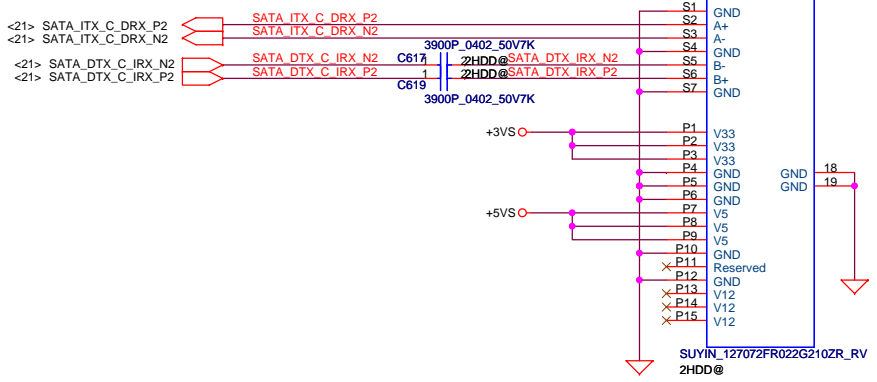


Place Components closely to SATA Conn.

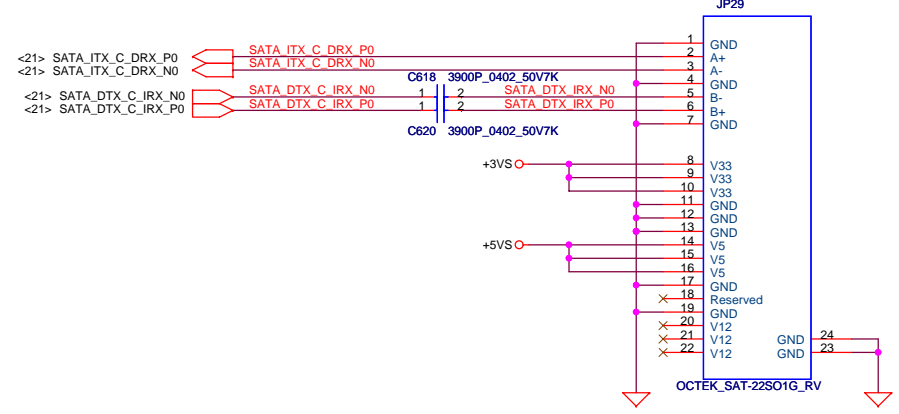


Place Components closely to SATA Conn.

### SATA HDD-2 Conn.

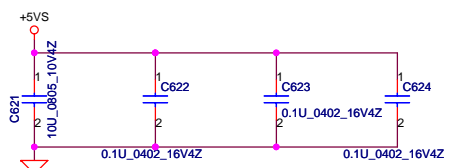


### SATA HDD Conn.

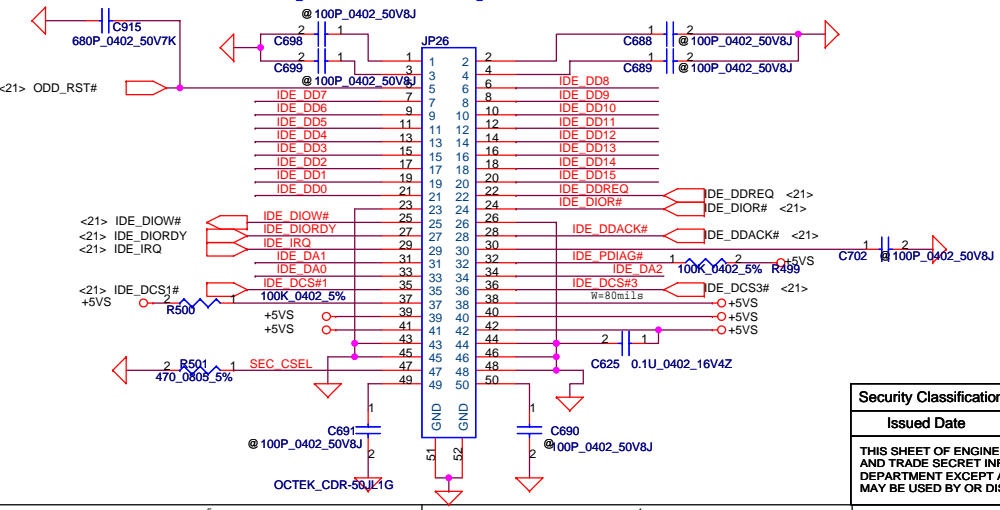


- <21> IDE\_DD[0..15] IDE\_DD[0..15]
- <21> IDE\_DA[0..2] IDE\_DA[0..2]

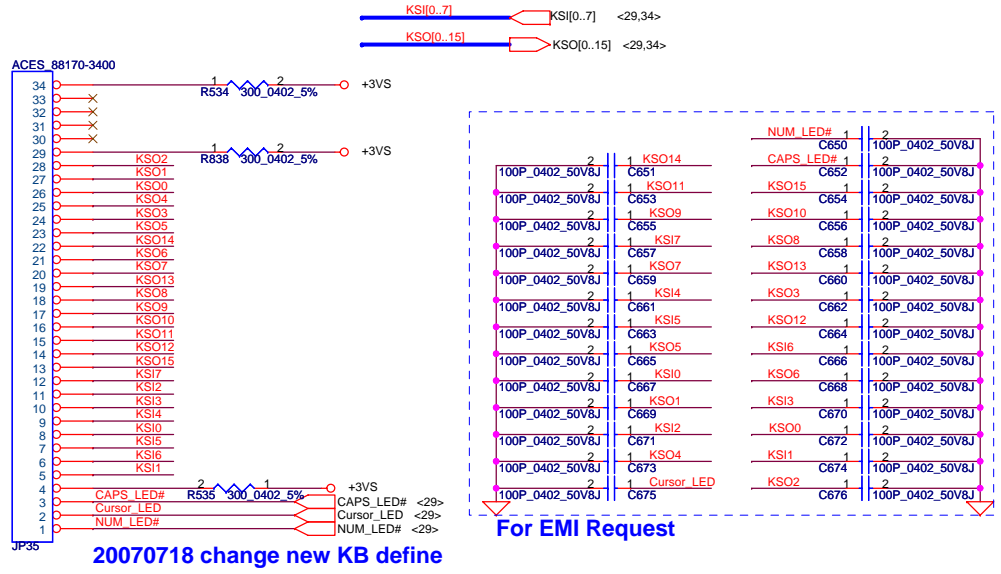
### ODD CONN



Place Components closely to ODD Conn.



### KEYBOARD CONN.



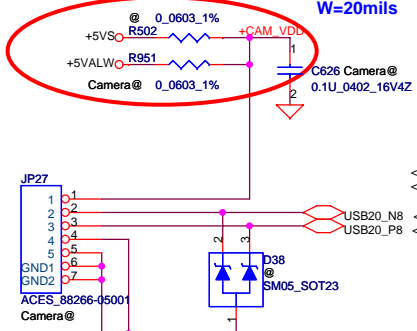
20070718 change new KB define

For EMI Request

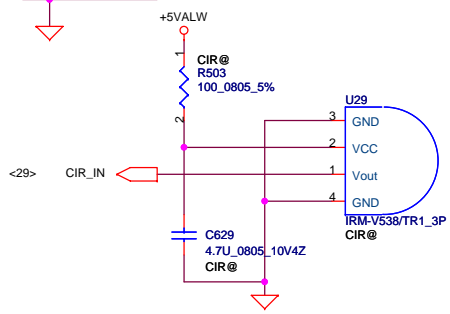
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		LA-3481P		2.0	
Date:		Tuesday, May 22, 2007		Sheet 32 of 47	



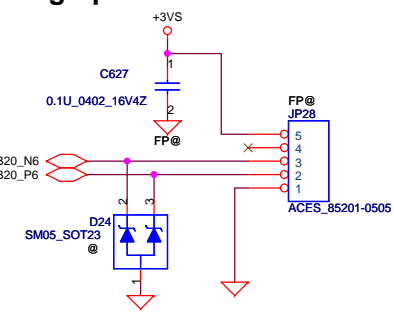
### Int. Camera Conn



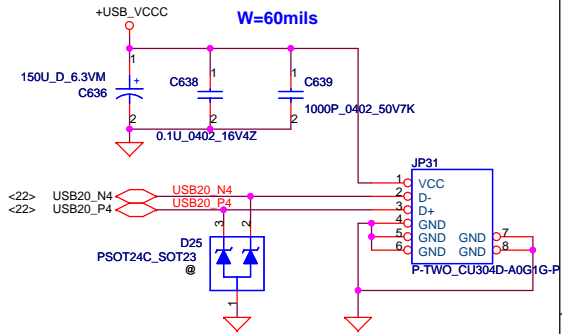
### CIR



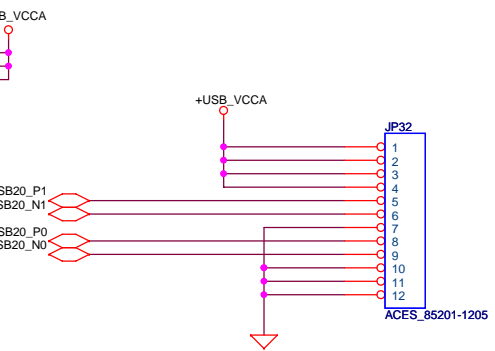
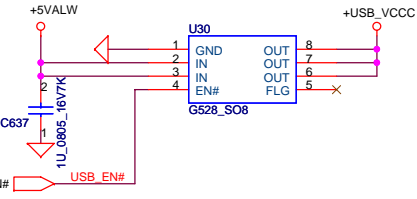
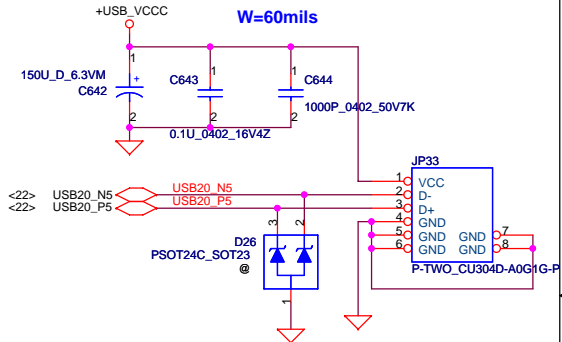
### Fingerprint Conn



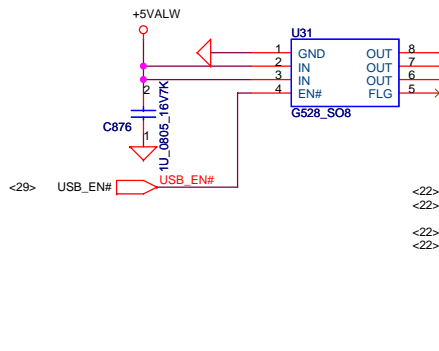
### USB CONN. 1



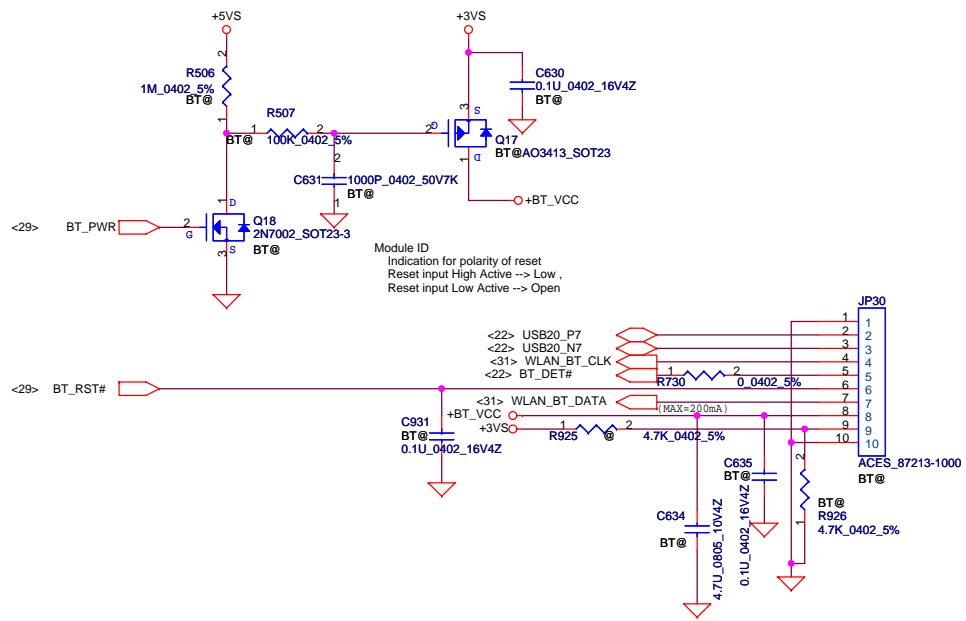
### USB CONN.2



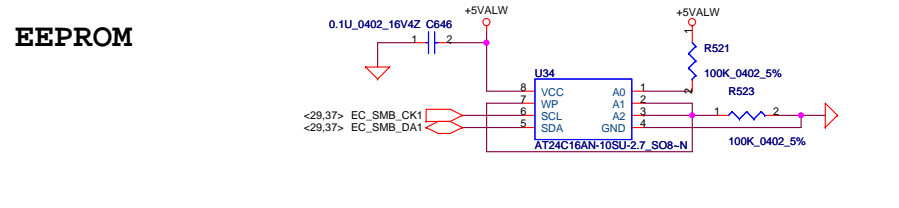
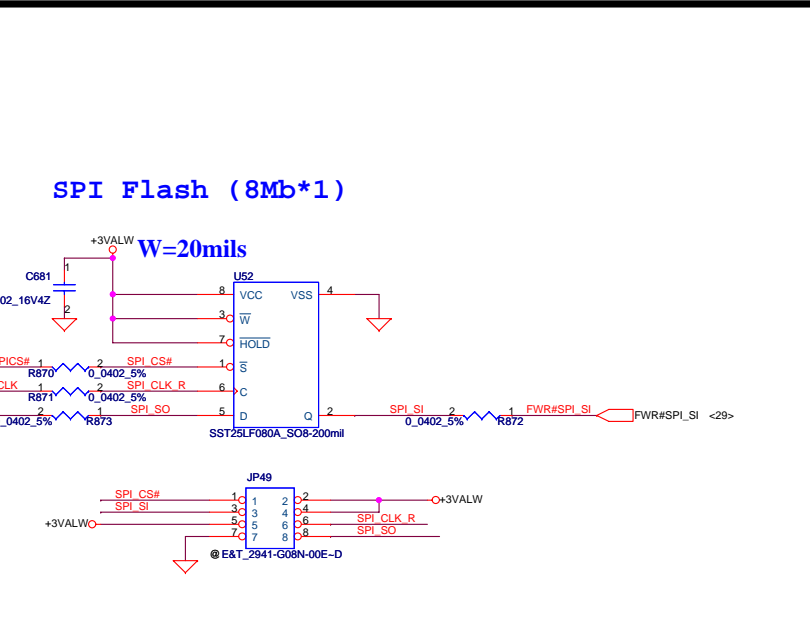
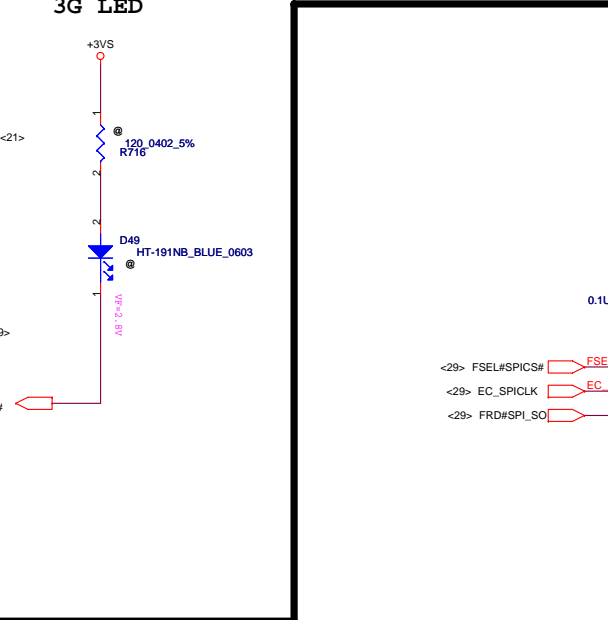
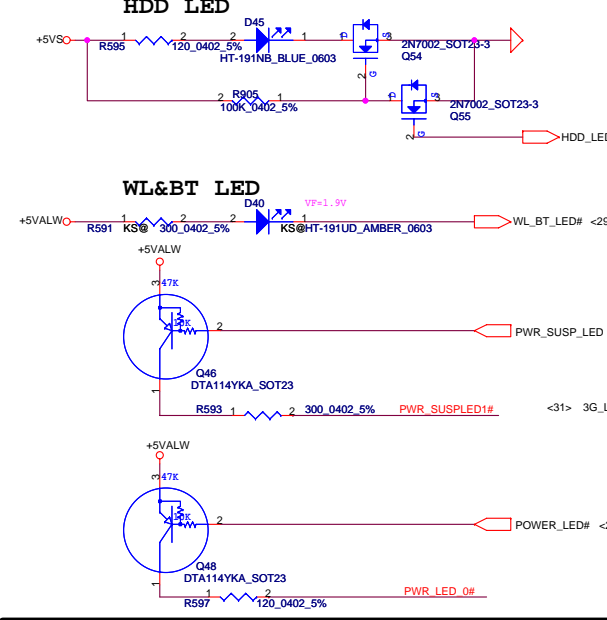
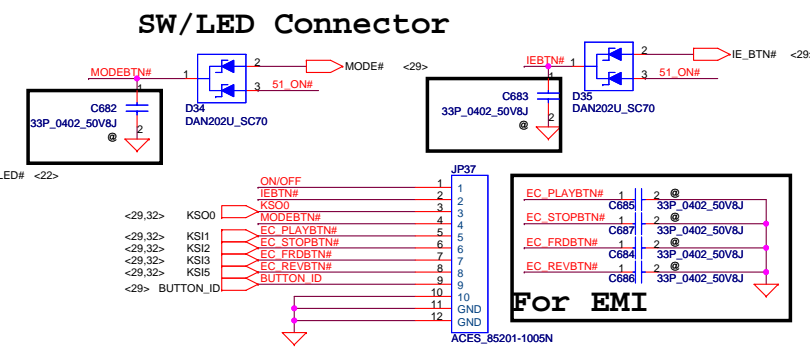
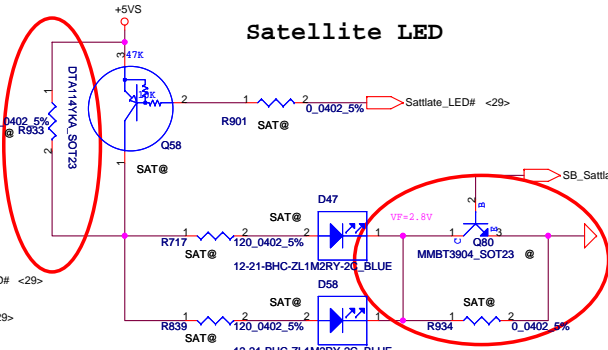
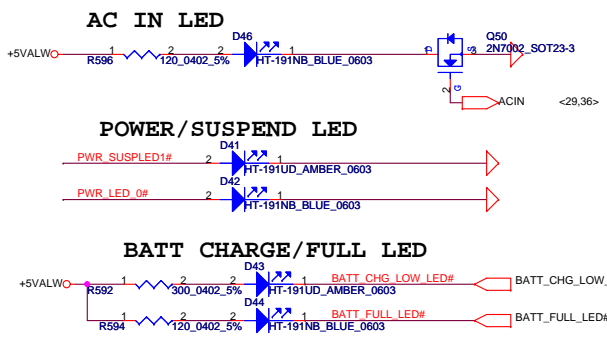
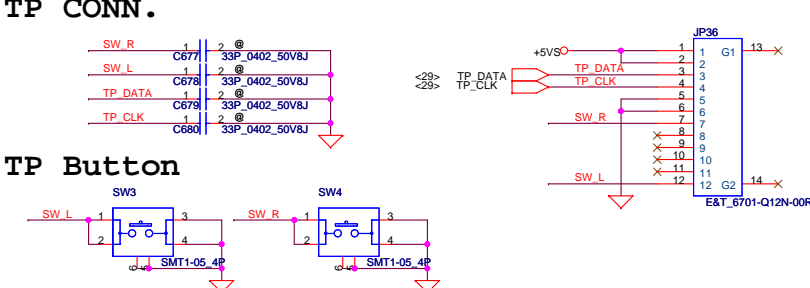
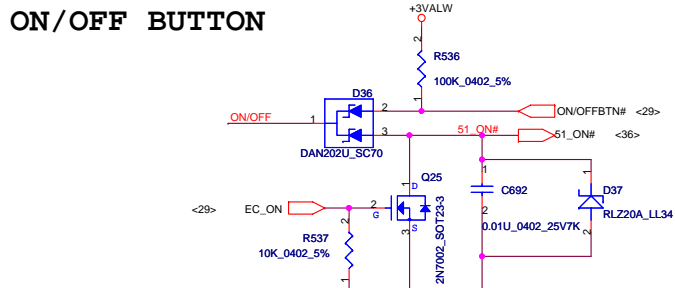
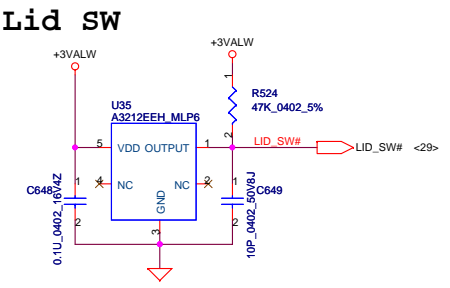
### USB Small Board



### BlueTooth Interface



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				LA-3481P	2.0
Date:	Tuesday, May 22, 2007	Sheet	33	of	47



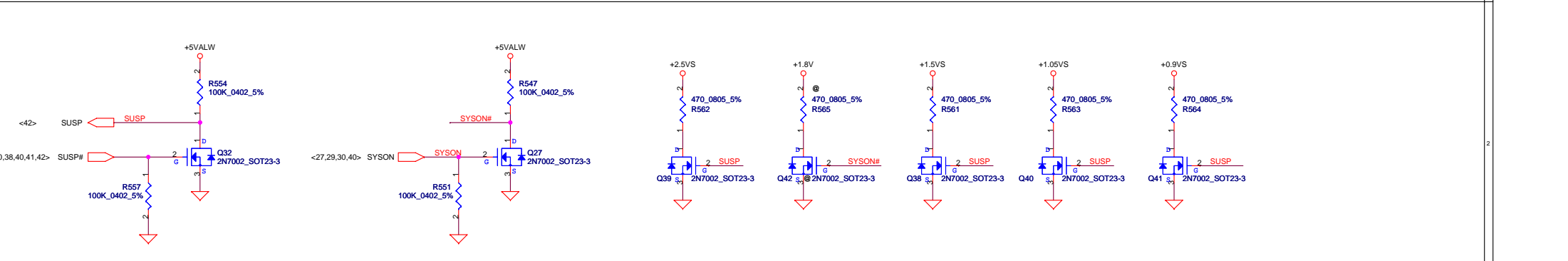
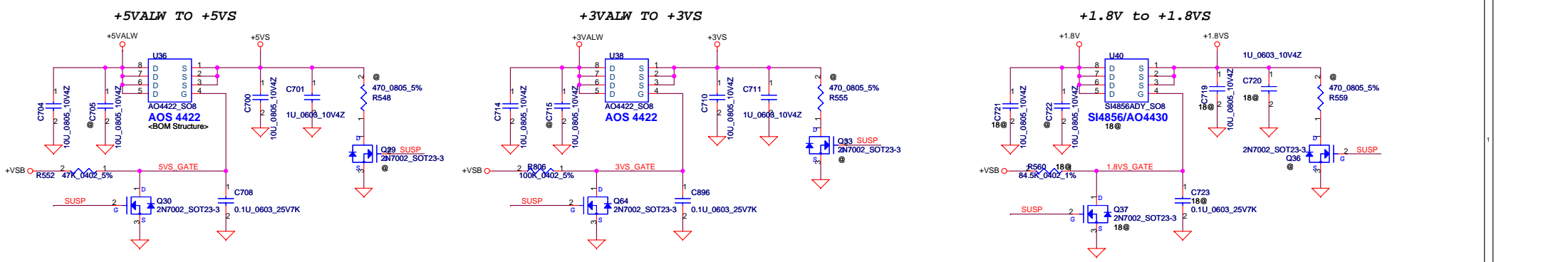
### Security Classification

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### EEPROM/TP/LID/KB/LED/SW-B

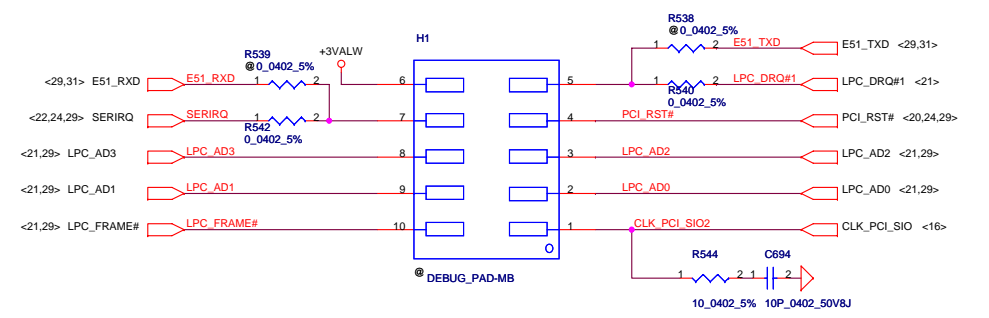
Document Number	LA-3481P
Rev	2.0

Date: Saturday, June 23, 2007 Sheet 34 of 47



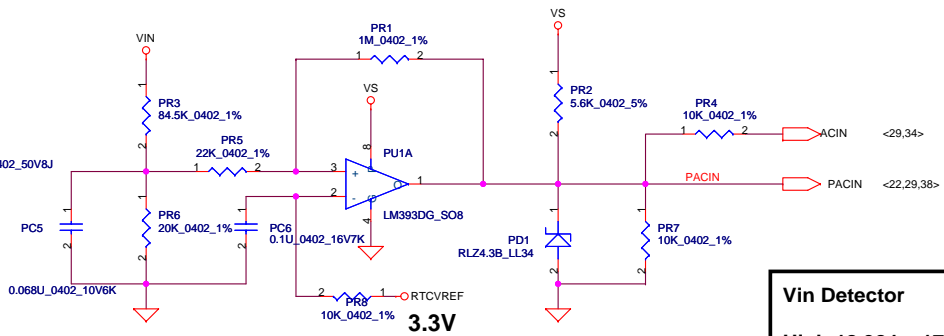
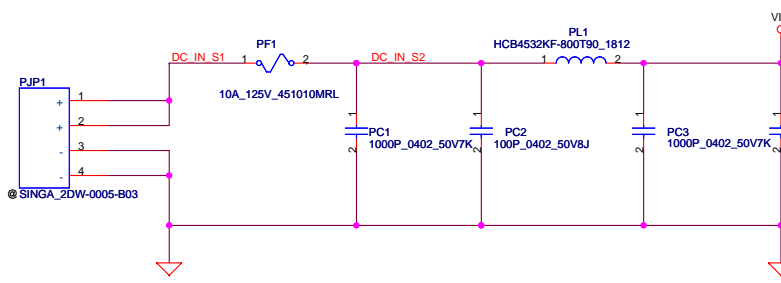
**Debug Port**

**New LPC Debug Pad ---- MB side For EE**

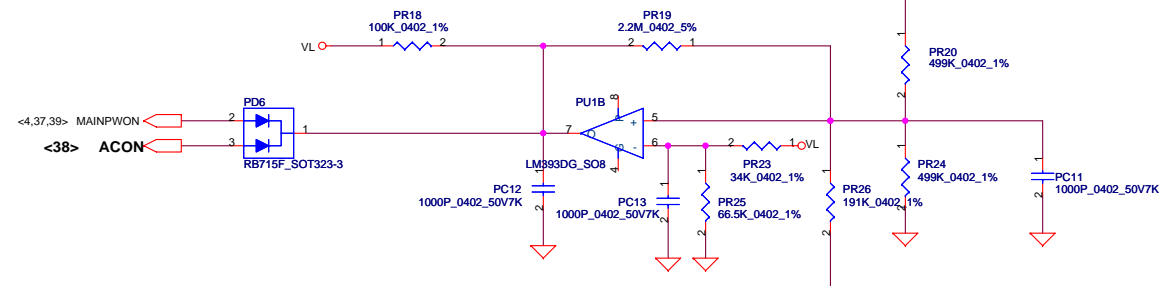
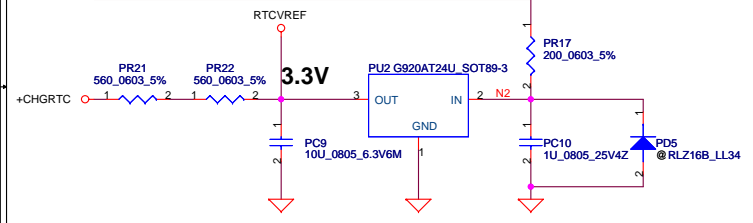
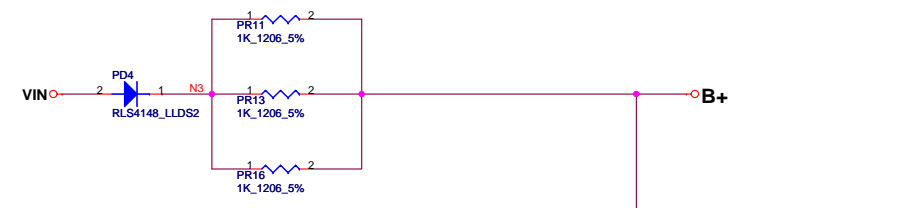
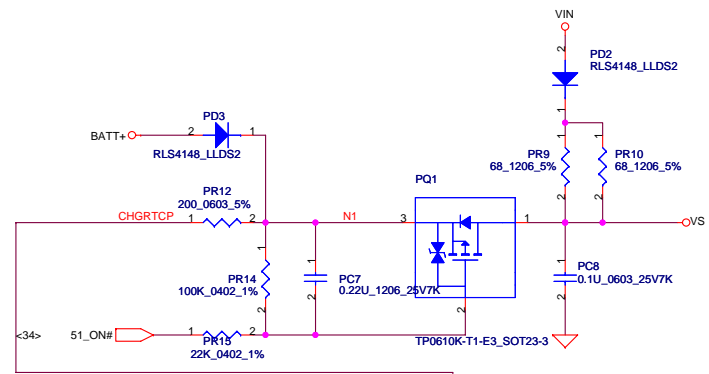


**Under DDR ME Assigment Area**  
**Keep Resistor near Debug Pad and in the same side**  
**Reverse Side DIMM ---- Pin 1 keep away DIMM**

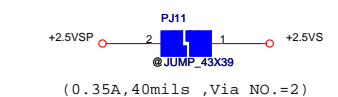
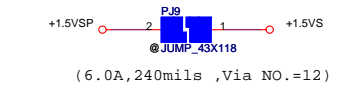
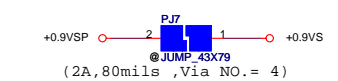
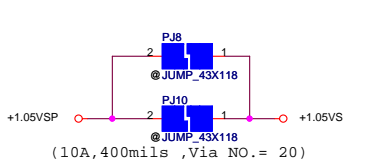
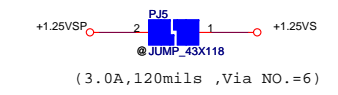
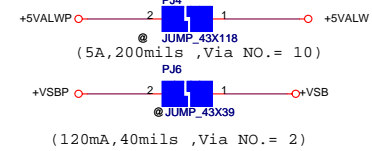
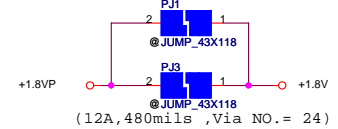
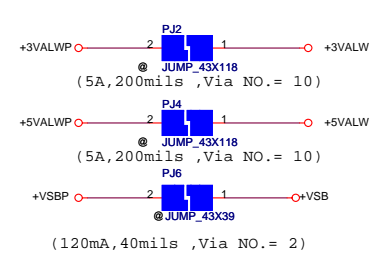
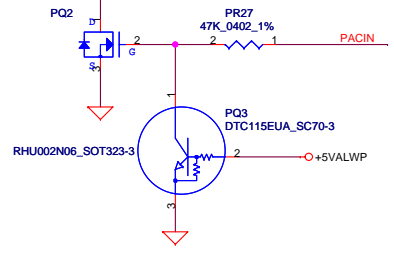
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Date:	Tuesday, May 22, 2007	Sheet	35 of 47



**Vin Detector**  
 High 18.384 17.901 17.430  
 Low 17.728 17.257 16.976

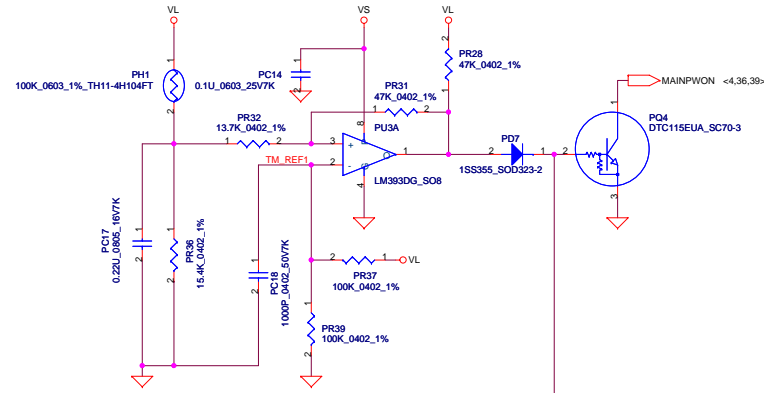
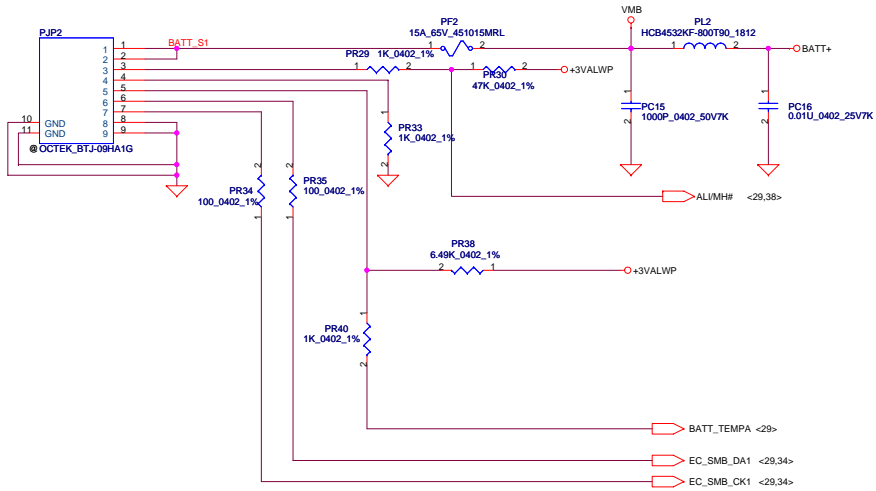


**Precharge detector**  
 15.97V/14.84V FOR ADAPTOR

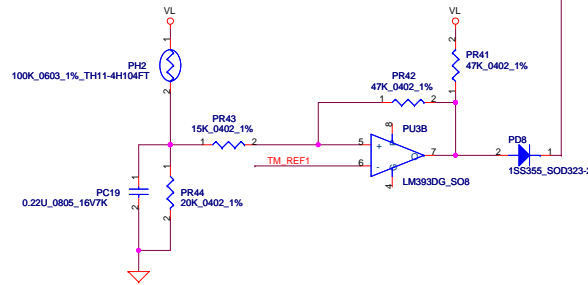
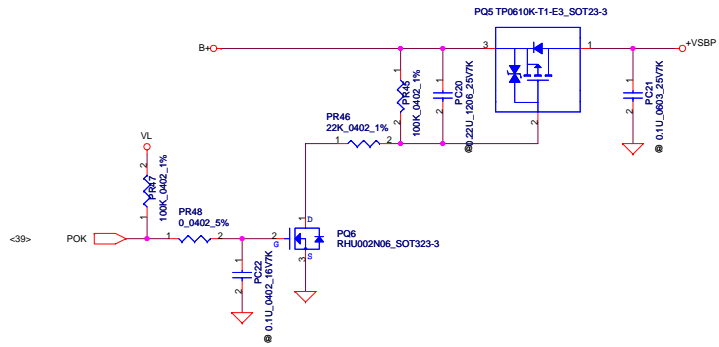


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Date:	Tuesday, May 22, 2007	Sheet	36	of 47

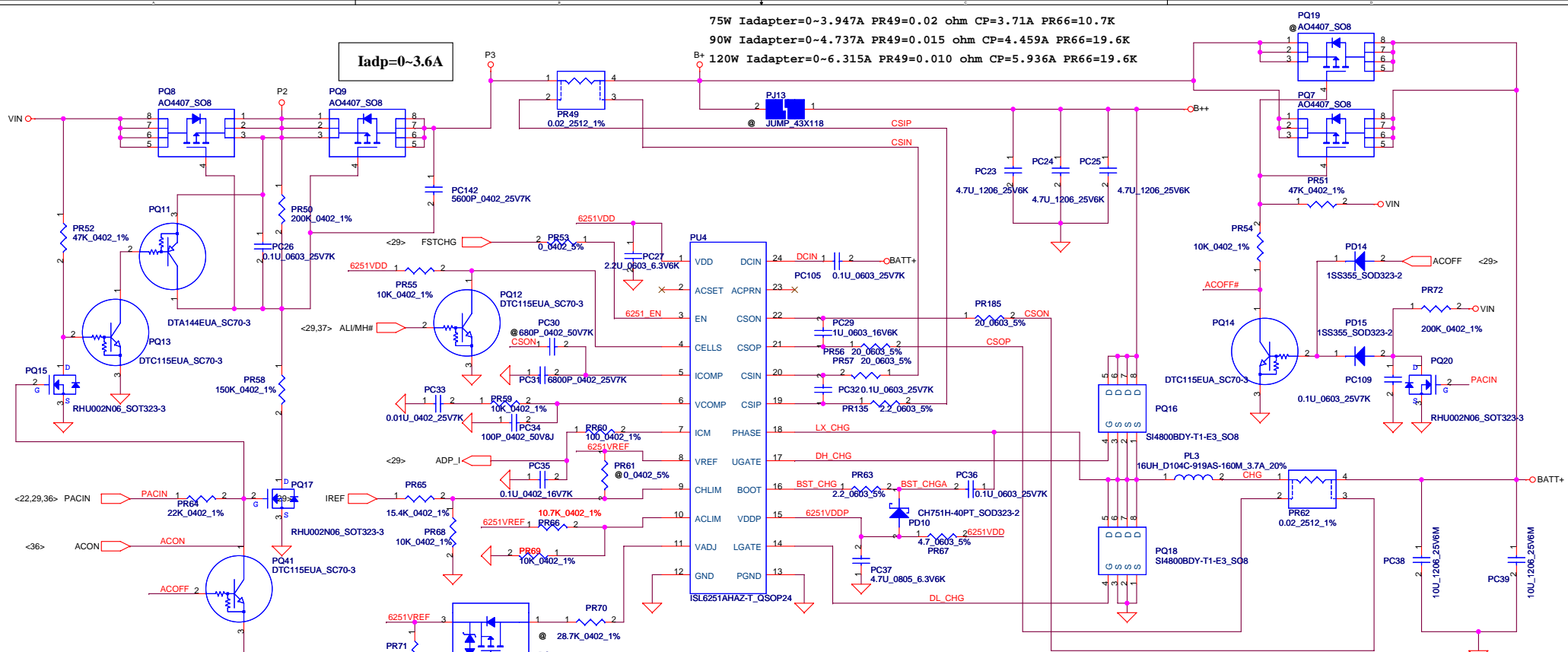
PH1 under CPU bottom side :  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



PH2 near main Battery CONN :  
 BAT. thermal protection at 92 degree C  
 Recovery at 47 degree C



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				Rev 2.0
Date: Tuesday, May 22, 2007				Sheet 37 of 47



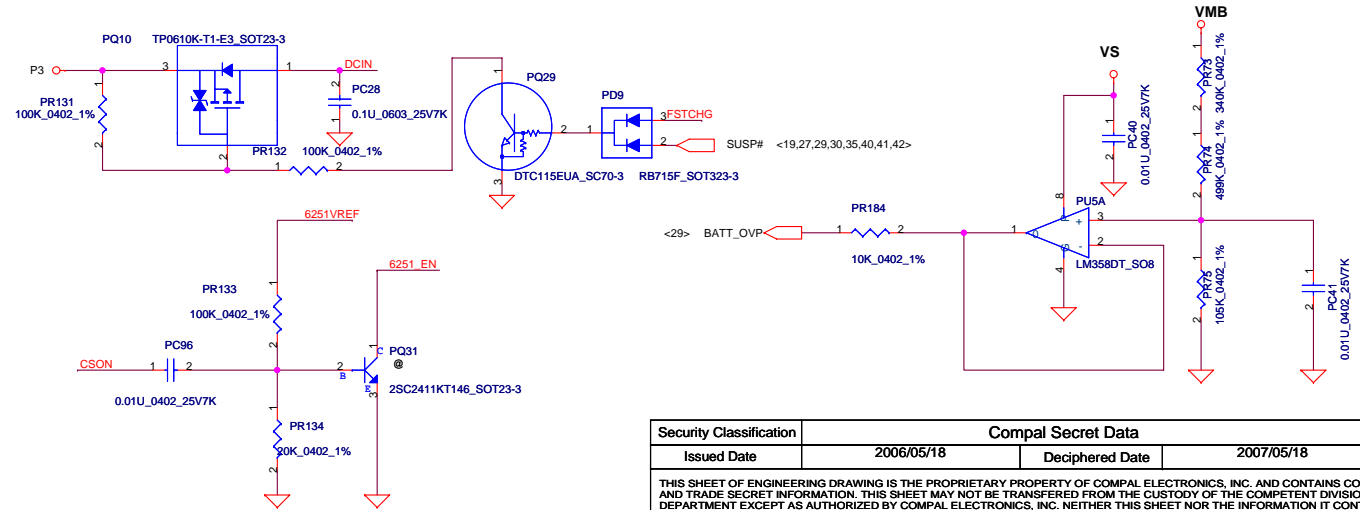
Iadp=0~3.6A

75W Iadapter=0~3.947A PR49=0.02 ohm CP=3.71A PR66=10.7K  
 90W Iadapter=0~4.737A PR49=0.015 ohm CP=4.459A PR66=19.6K  
 120W Iadapter=0~6.315A PR49=0.010 ohm CP=5.936A PR66=19.6K

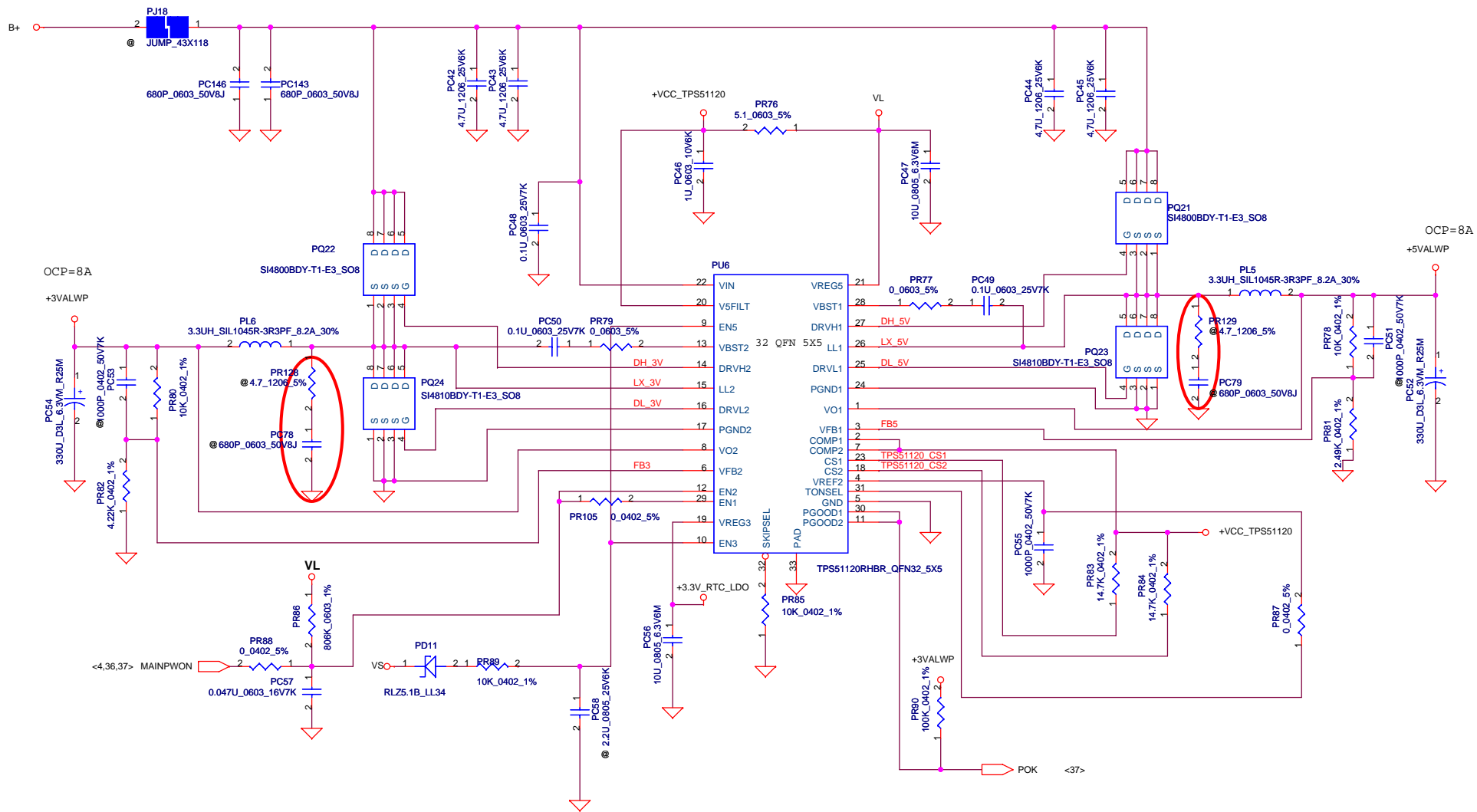
IREF=1.016\*Icharge  
 IREF=0.508V~3.048V

CC=0.5~3A  
 CV=12.6V(6 CELLS LI-ION)

BATT Type	AL/MH#	Charge Current	IREF
3 CELL	3.3V	1.5A	1.524V
6 CELL	3.3V	3.0A	3.048V
9 CELL	3.3V	3.0A	3.048V

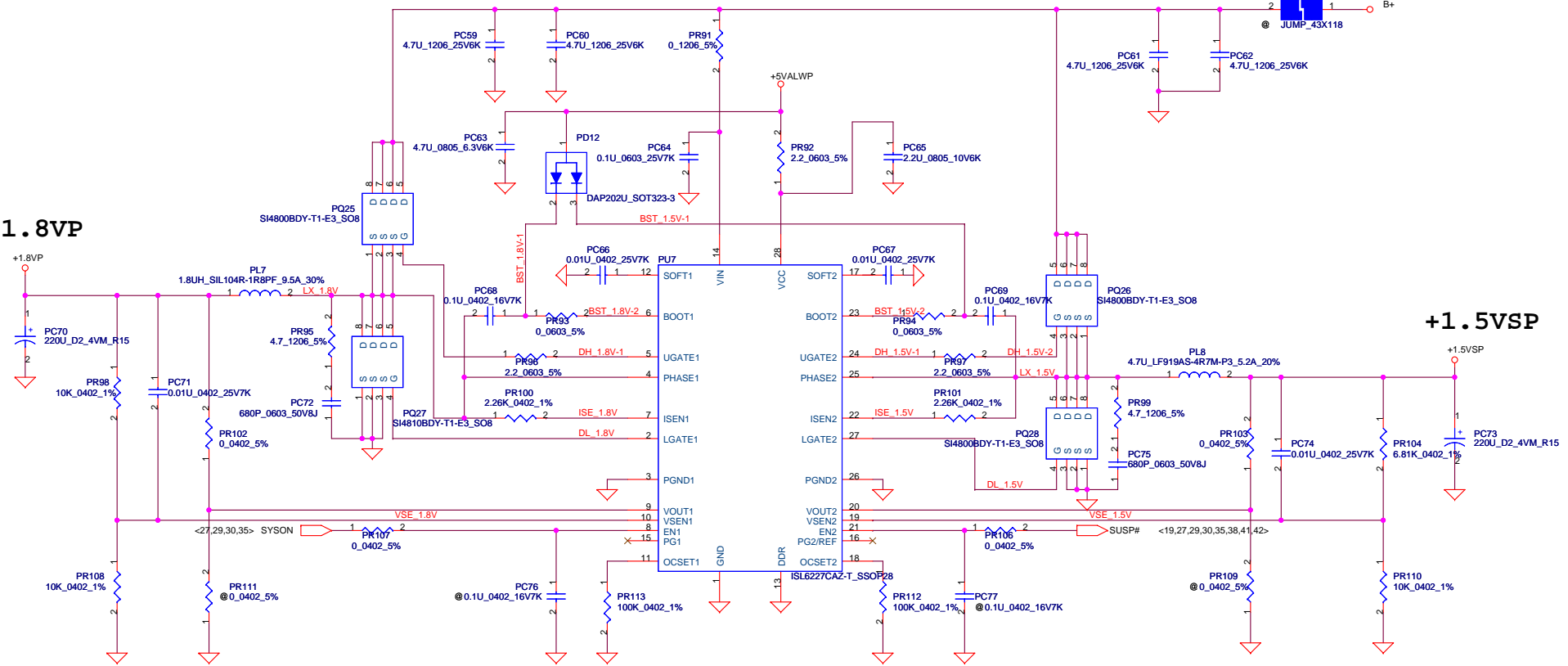


LI-3S :1.3.5V---BATT-OVP=1.5V  
 BATT-OVP=0.111\*BATT+



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Size	Document Number	Date		Rev	
Custom	LA-3481P	Tuesday, May 22, 2007		2.0	
Sheet 39 of 47					

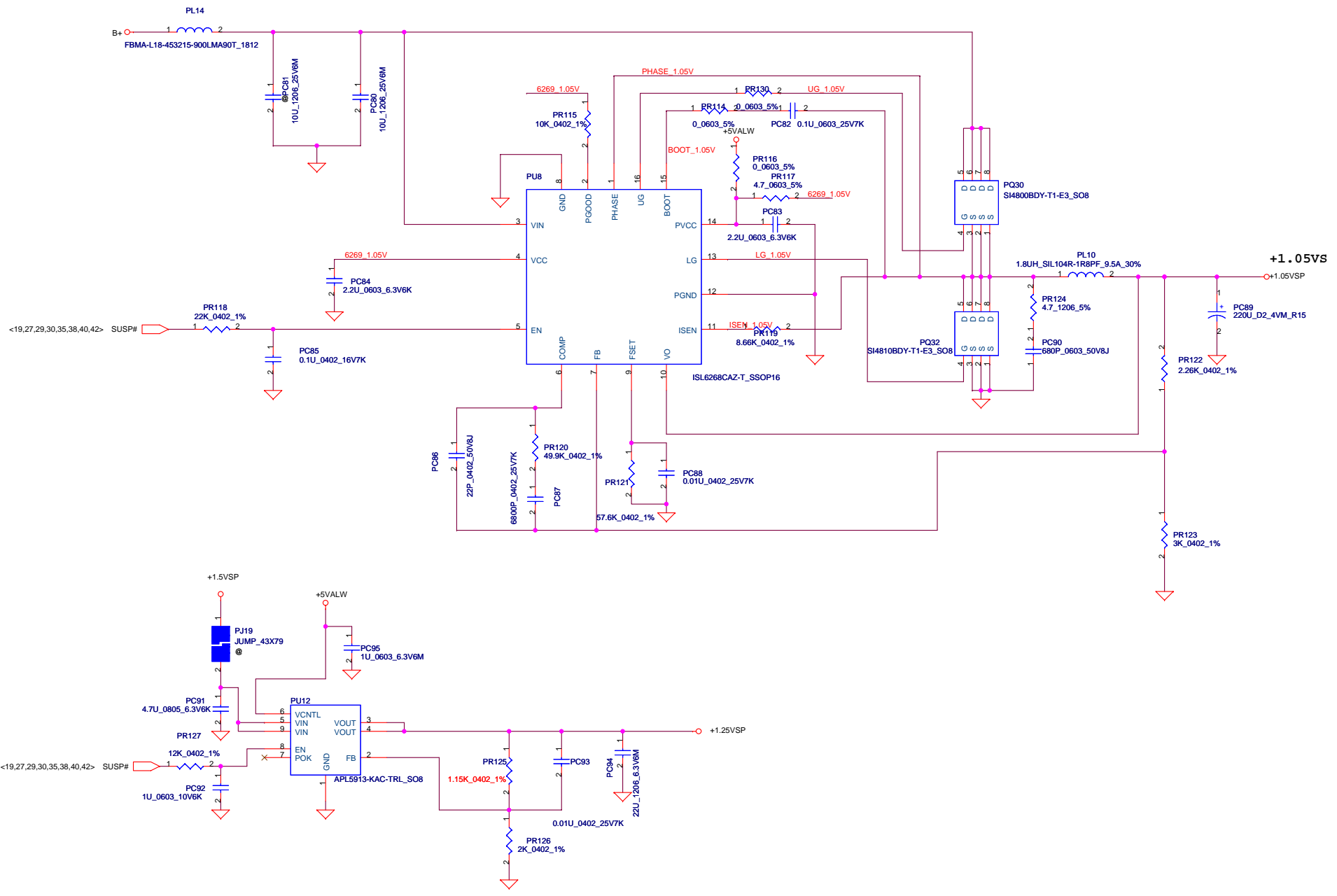
**+1.8VP**



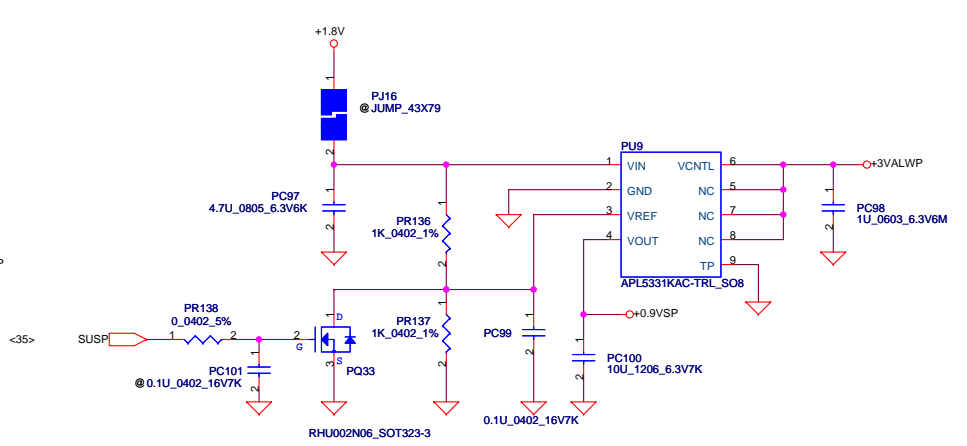
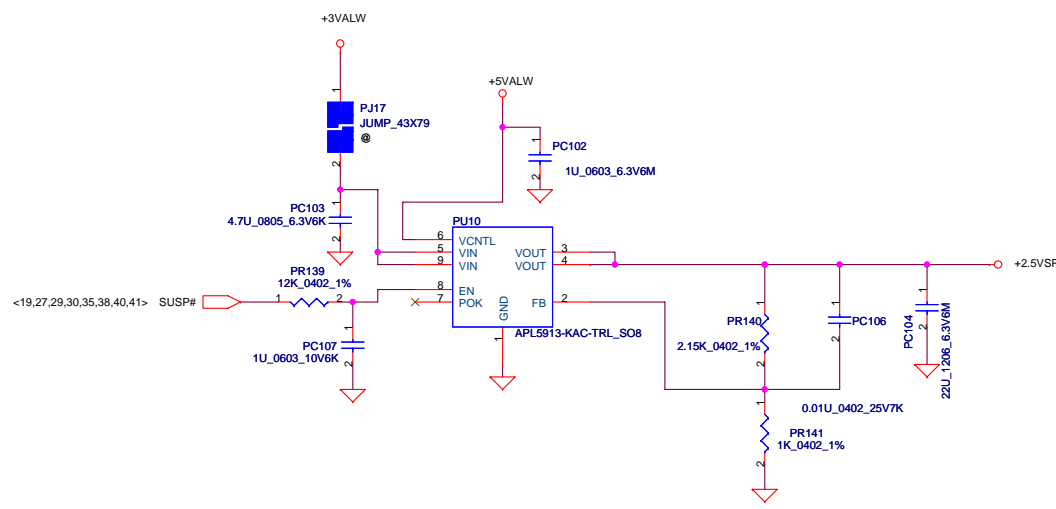
**+1.5VSP**

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Date:	Tuesday, May 22, 2007	Sheet	40	of	47

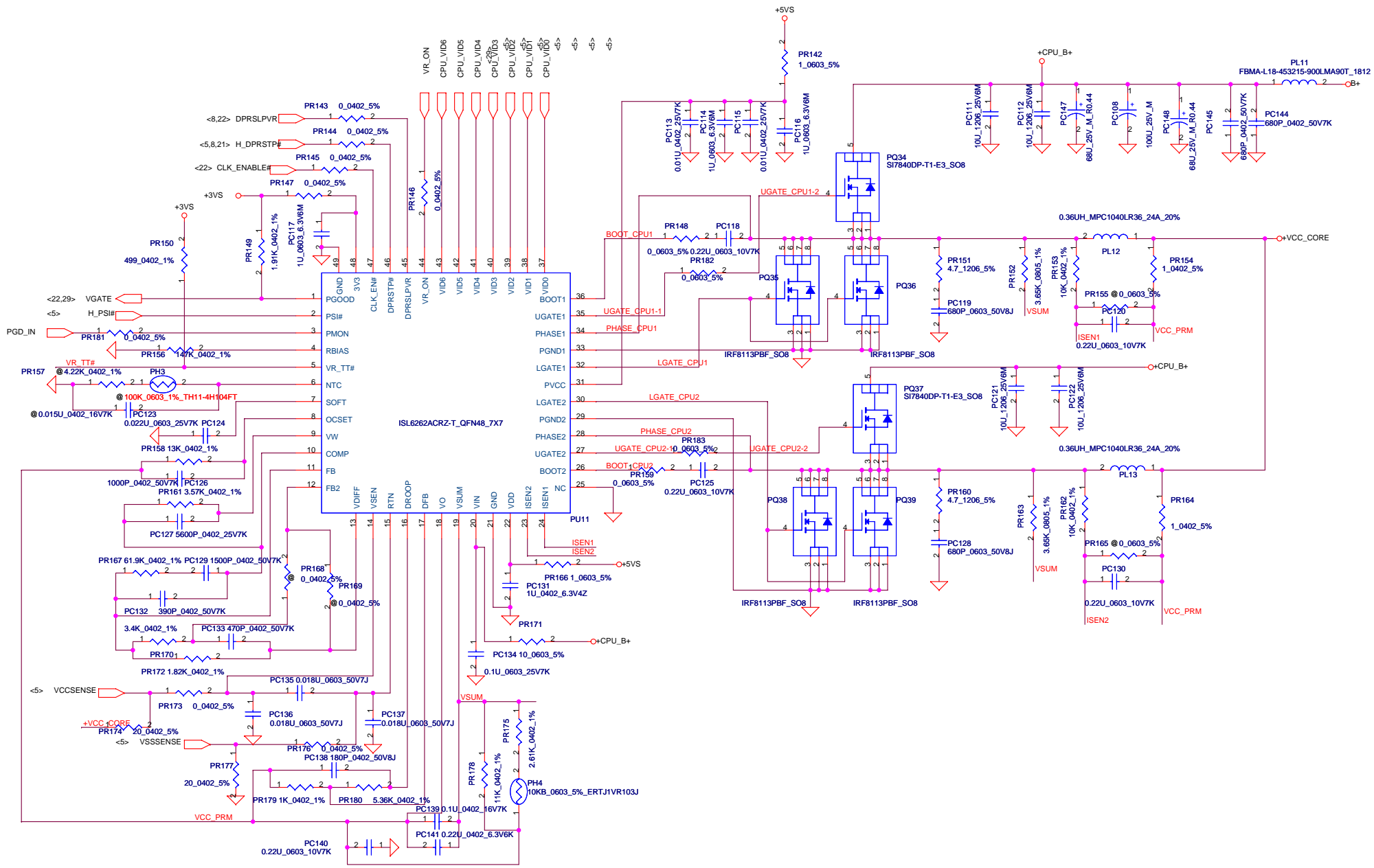




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Date: Tuesday, May 22, 2007				Sheet	41 of 47



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Date: Tuesday, May 22, 2007				Sheet 42 of 47



Security Classification	Compal Secret Data		Title	
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Document Number	LA-3481P	Rev	2.0	
Date:	Tuesday, May 22, 2007	Sheet	43	of 47

# HW4 Product Improvement Record (P.I.R.)

ISKAA LA-3481P SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1 TO 2A

## Rev 0.1 to 0.2

NO	PAGE	MODIFICATION LIST	PURPOSE
1	17	Add JP39	Add CRT Board
2	22	Change R322 from 150 ohm to 10K ohm	From Intel recommend
3	12	Delete L13, L14, C199, C140	1.25VS_DMI share with 1.25VS_PEG
4	31	Modify PCI-E for WLAN and Robson	Design issue
5	15	Delete C234	Share with C729

## Rev 0.2 to 0.3

NO	PAGE	MODIFICATION LIST	PURPOSE
1	11	Remove C116	From Intel recommend
2	16	Change EXP_CLKREQ# from U4.44 to U4.3	Common design with ISRAA
3	16	Change CLK_MCH_3GPLL from U4.27 to U4.47	Common design with ISRAA
4	16	Change CLK_PCIE_CARD from U4.47 to U4.27	Common design with ISRAA
5	19	Add R949 and Remove D11	Design change
6	19	Add JP42	Co-layout 30 pin LVDS connector
7	24	Add R874	Reserve the resistor for EMI
8	29	Change EC from KB910 to KB926	Design change
9	34	Change SPI BIOS U52	Design change
10	34	Add Q54, Q55	HDD LED controlled by SB
11	47	Add Energy Star circuit	Design change
12	10	Change C84-C115 from Y5V to X7R	For VGA thermal issue

## Rev 0.3 to 0.4

NO	PAGE	MODIFICATION LIST	PURPOSE
1	12	Modify L58 to 4.7 ohm	For TV-out wave line issue
2	12	Change R686 to 2.2uf	For TV-out wave line issue
3	12	Modify L15 to 100 ohm	from Intel recommend for new chip set
4	12	Change R694 to 1uf	from Intel recommend for new chip set
5	26	Reserve L92,R941,R944,R946,R947, C965,C963,R937,C962,C964	Reserve for LAN controller 811C
6	33	Modify Camera power from +5Vs to +5VALW	Change for Camera can't detect from S3 resume
7	29	Add R928	For CIR issue
7	22	Add R903 and R927	For CIR issue

## Rev 0.4 to 1.0

NO	PAGE	MODIFICATION LIST	PURPOSE
		Change PCB 0.4 to 1.0	Modify Revision for MP
1	27	Add R935	Design for speaker select
2	28	Change L49, L50, L51, L52 to 0 ohm	For speaker issue
3	27	Change C517 and C519 from 1uf to 4.7uf	From Realtek recommend for THD+N issue
4	31	Add R954	For HD-DVD function

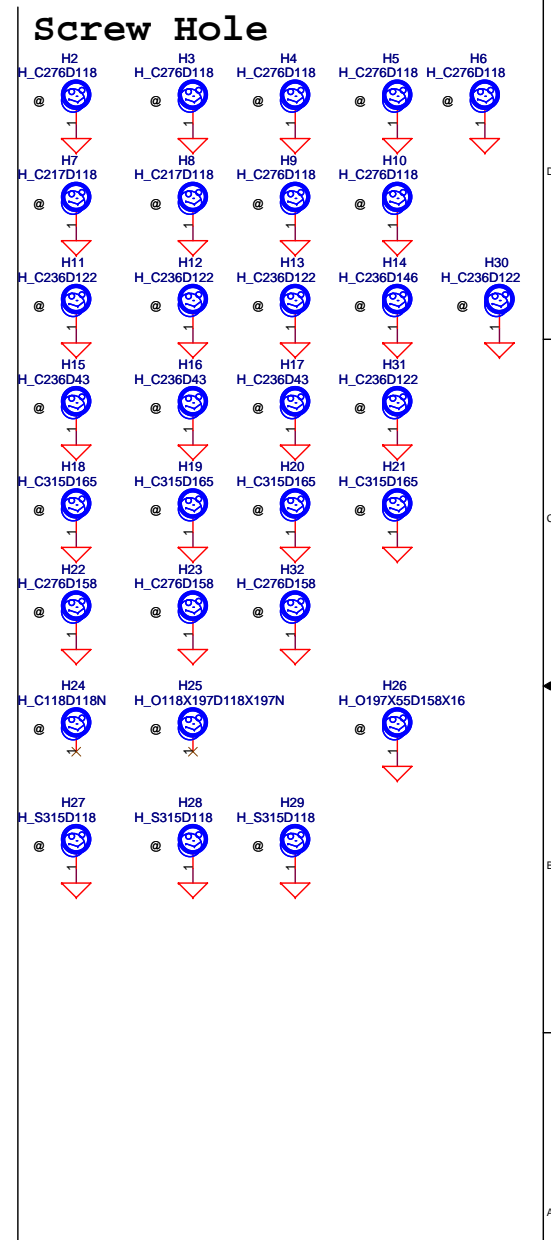
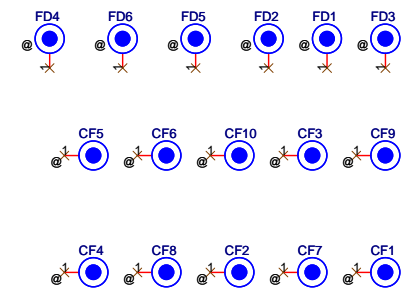
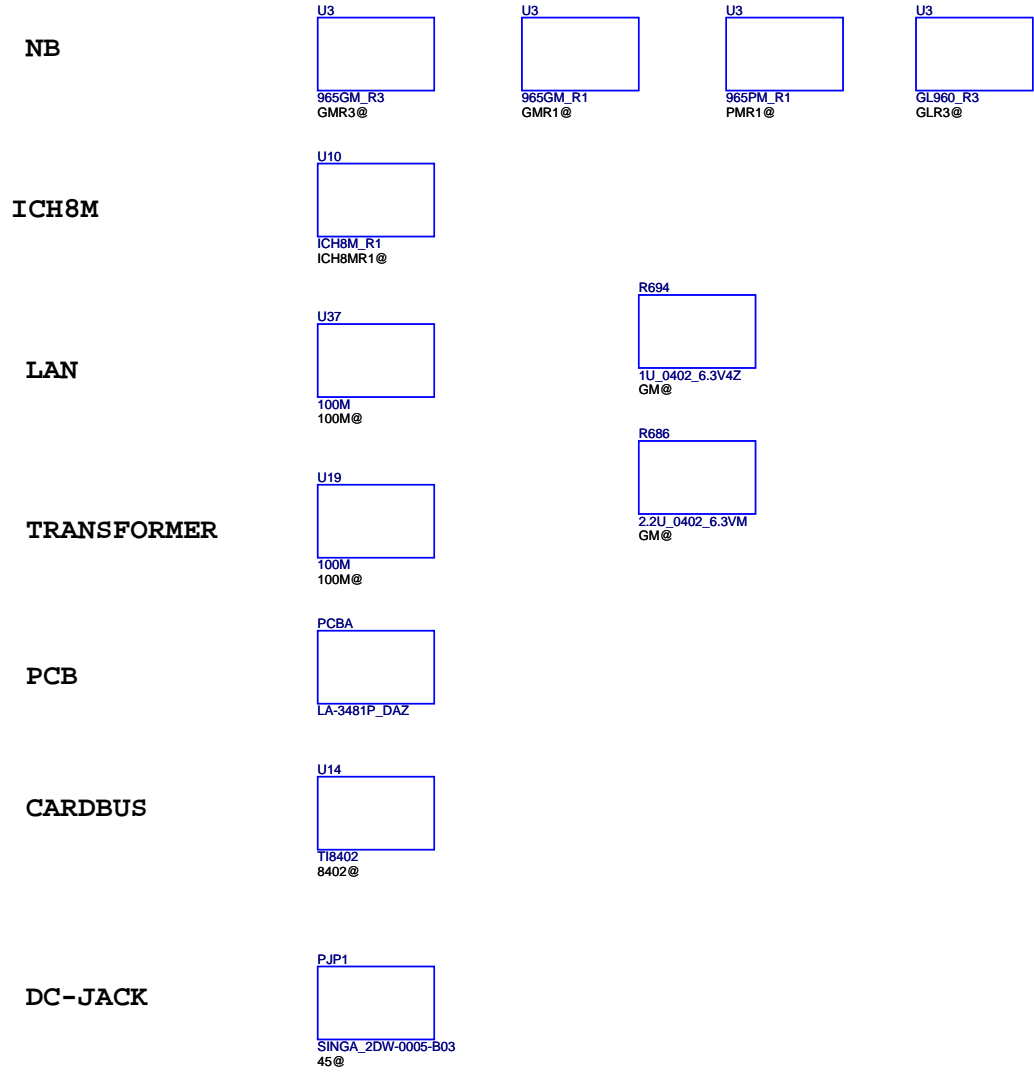
## Rev 1.0 to 2.0

NO	PAGE	MODIFICATION LIST	PURPOSE
1	18	Add U54 and C966	For HDMI hot plug issue
2	18	Remove 1932 circuit	M72 and M76 has internal HDMI
3	18	Remove CMD circuit	For EMI issue
4	18	Add L66, L67, L68, L69	For EMI issue
5	18	Add Q134,Q135 level-shifting circuit	For HDMI level-shifting
6	18	Change R705 and R706 to 19.1K ohm	From ATI recommend
7	24	Reserve R713, R714, R715, C873, C875, C877	For EMI issue
8	32	Reserve C650-C676	For EMI issue
9	34	Reserve C682-C687	For EMI issue
10	18	Change R621 to 100K ohm and R723 to 2.2K ohm	For HDMI level-shifting

## Rev 2.0 to 2A

NO	PAGE	MODIFICATION LIST	PURPOSE
1	18	Add U55 level-shifting circuit	For HDMI level-shifting
2	29	Change C943 and C944 from 10pf to 15pf	From ENE recommend for crystal issue
3	23	Change C360 from 0.1uf to 1uf	From Intel recommend for boot-up issue
4	22	Remove R327, R328, R329	For leakage issue

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Document Number			LA-3481P	
Date: Saturday, June 23, 2007				Sheet 44 of 47

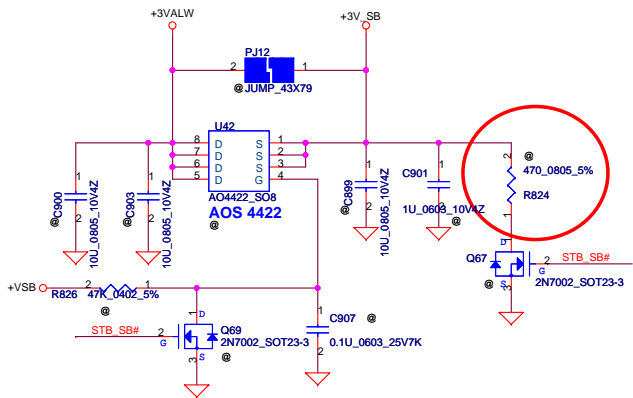


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				LA-3481P	2.0
				Date: Tuesday, May 22, 2007	Sheet 45 of 47

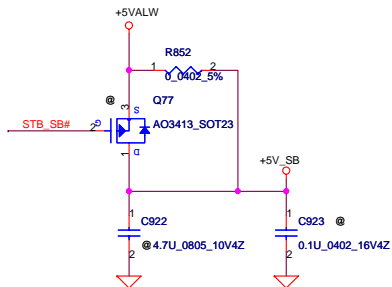
NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
9/14		P.39	Change PACIN to GND	Change to AUTO-SKIP mode
9/14		P.39	Add PR105 0_0402_5%	Reserve control sequence pin
9/14		P.37	Change PF2 to 15A	Increase design margine
10/24		P.36,37,43	Change PL1,PL2,PL11 to Tai-Tech	Buyer request
10/24		P.39,43	Add PC143,PC144,PC145	EMI request
10/24		P.41,43	Add snubber PR124,PC90,PR151,PC119,PR160,PC128	EMI request
10/24		P.41	Change PR119 to 5.49K	Modify 1.05V OCP point
10/24		P.40	Change PC70 to 330U_D2_9m ohm	Reduce the 1.8V ripple

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Date: Tuesday, May 22, 2007				Sheet	46	of 47

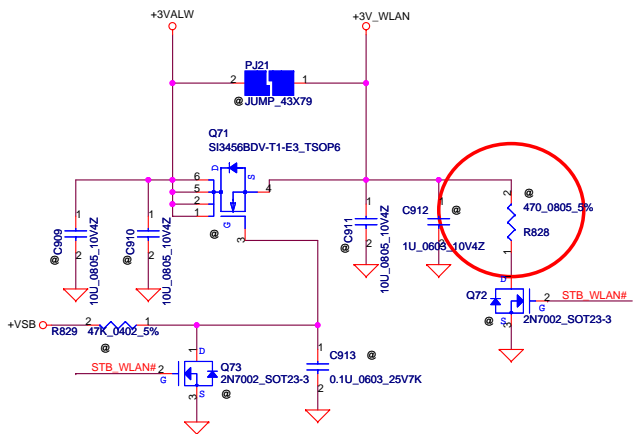
**+3VALW TO +3V\_SB**



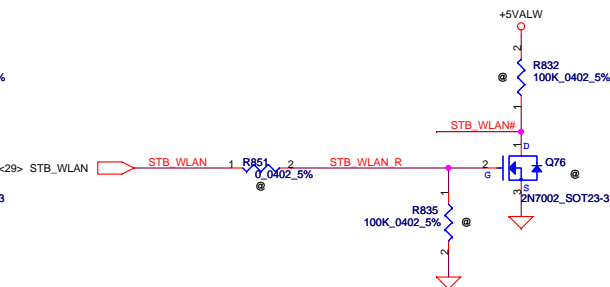
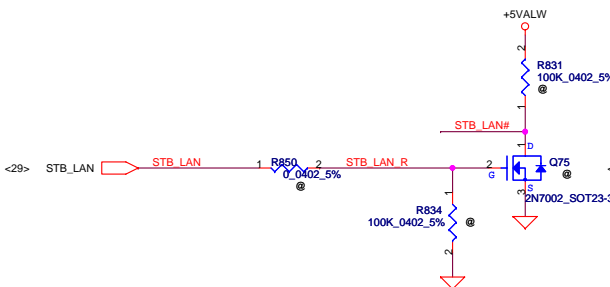
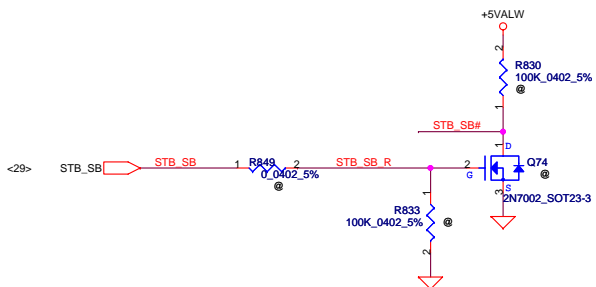
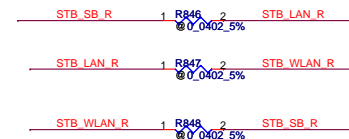
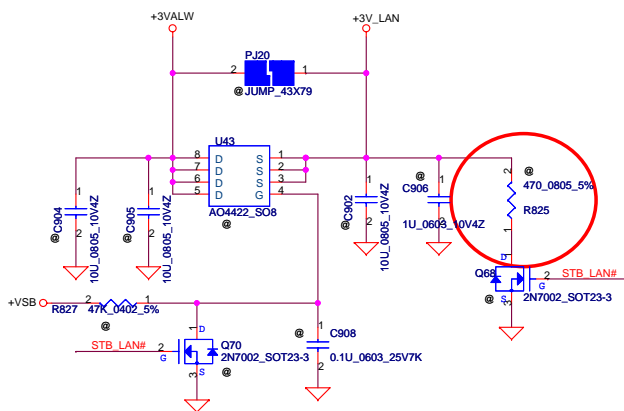
**+5VALW TO +5V\_SB**



**+3VALW TO +3V\_WLAN**



**+3VALW TO +3V\_LAN**



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Rev	Document Number	Rev
2.0	LA-348IP	2.0
Date:	Tuesday, May 22, 2007	Sheet 47 of 47