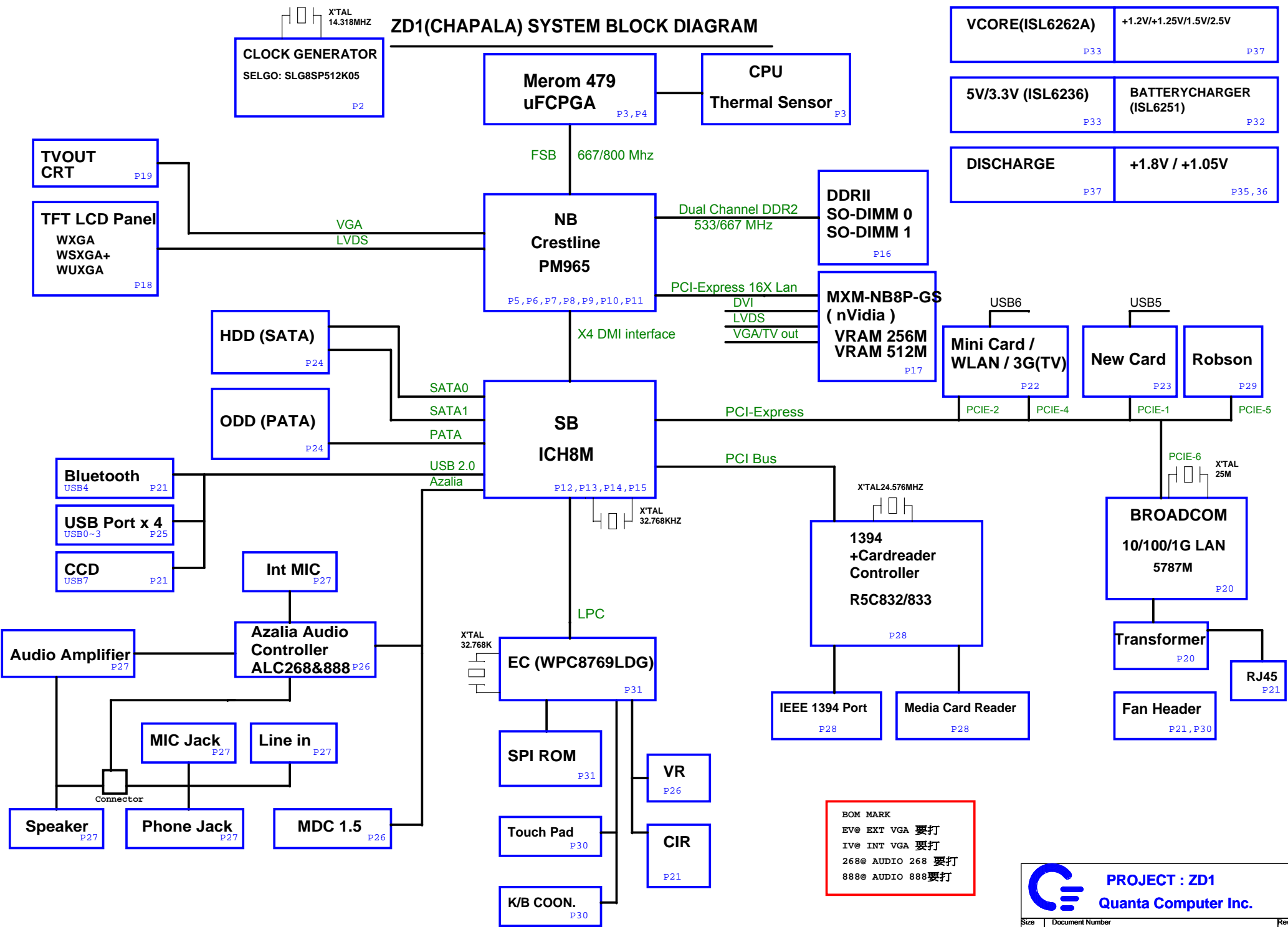


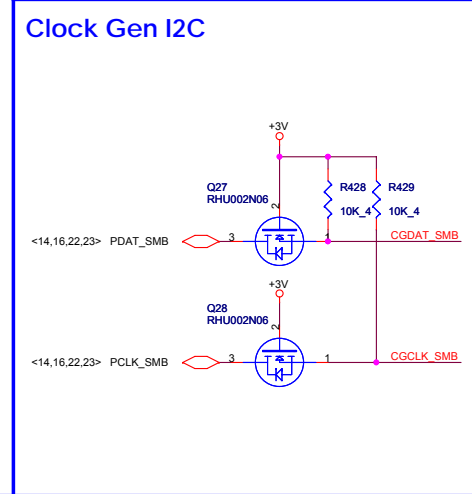
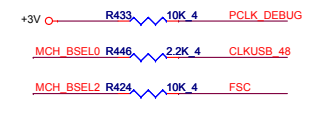
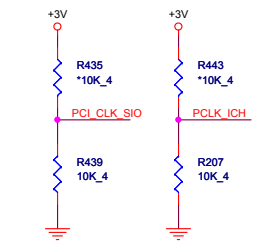
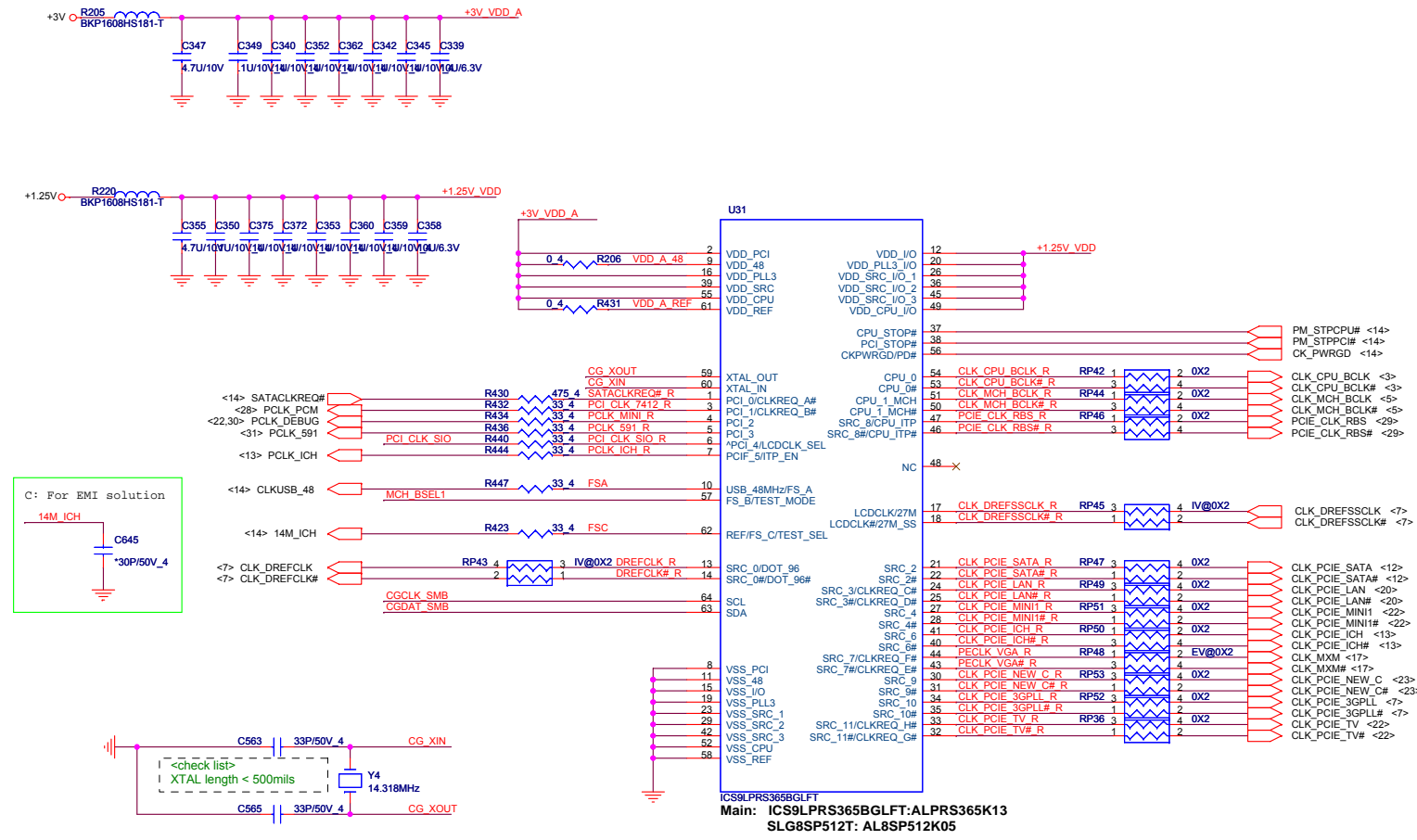
ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM



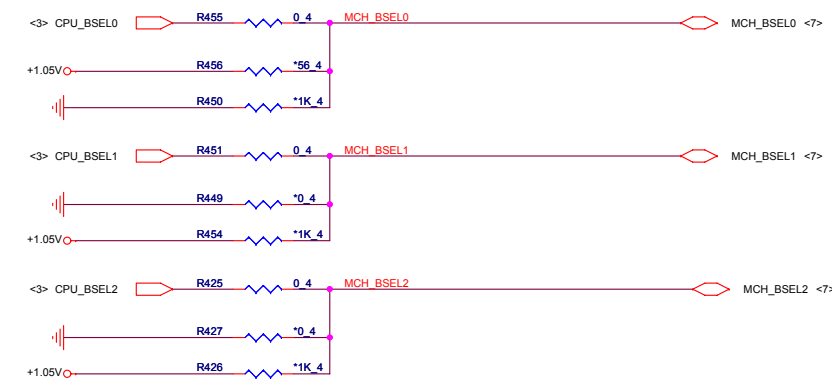
BOM MARK
 EV@ EXT VGA 要打
 IV@ INT VGA 要打
 268@ AUDIO 268 要打
 888@ AUDIO 888 要打

Clock Generator

Change list:
 B-test
 1.Change U31 P/N to ALPRS365K13 (ICS)



CPU Clock select



BSEL Frequency Select Table

| FSC | FSB | FSA | Frequency |
|-----|-----|-----|-----------|
| 0 | 0 | 0 | 266Mhz |
| 0 | 0 | 1 | 1.33Mhz |
| 0 | 1 | 1 | 1.66Mhz |
| 0 | 1 | 0 | 2.00Mhz |
| 1 | 1 | 0 | 4.00Mhz |
| 1 | 1 | 1 | Reserved |
| 1 | 0 | 1 | 1.00Mhz |
| 1 | 0 | 0 | 3.33Mhz |

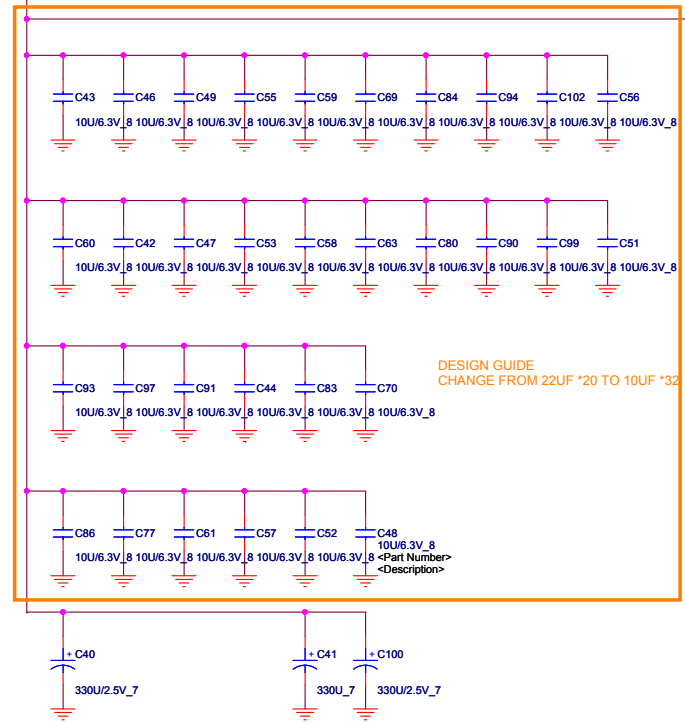
PROJECT : ZD1
Quanta Computer Inc.

Size: Document Number: **CLOCK GENERATOR CK505 W/REGULATOR** Rev: E

Date: Monday, May 07, 2007 Sheet: 2 of 38

CPU(Power)

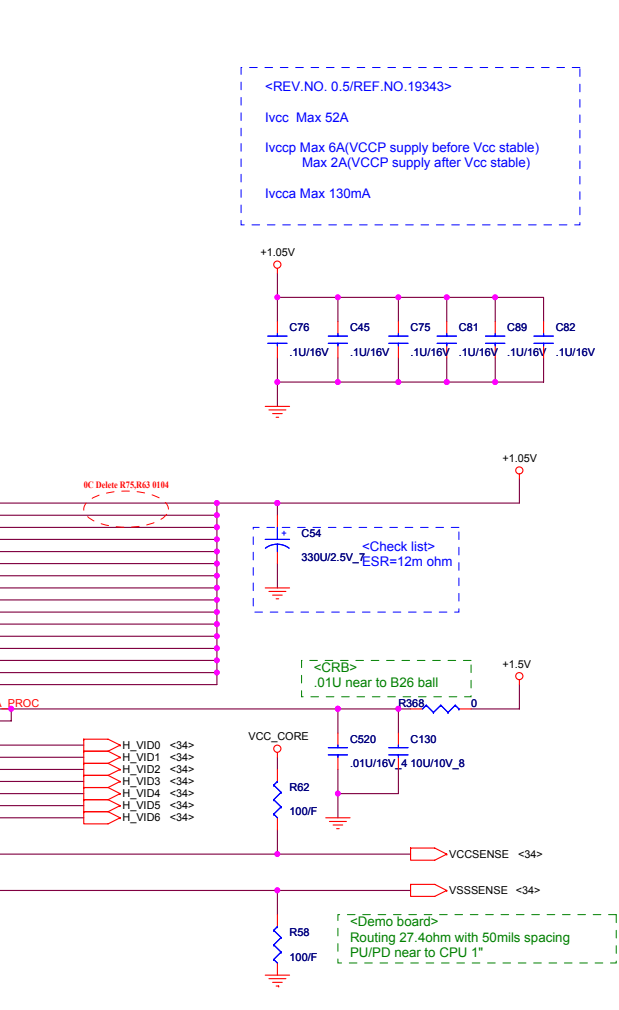
VCC_CORE



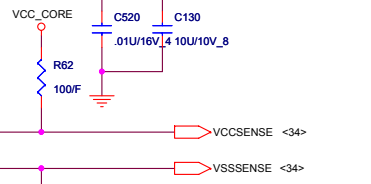
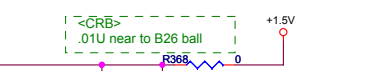
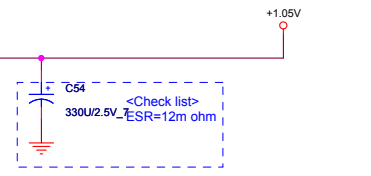
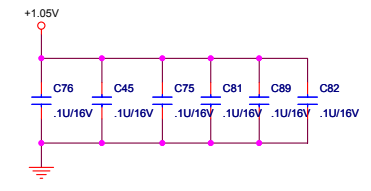
DESIGN GUIDE
CHANGE FROM 22UF *20 TO 10UF *32

<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

| U22C | | |
|------|----------|----------|
| A7 | VCC[001] | VCC[068] |
| A8 | VCC[002] | VCC[069] |
| A9 | VCC[003] | VCC[070] |
| A10 | VCC[004] | VCC[071] |
| A11 | VCC[005] | VCC[072] |
| A12 | VCC[006] | VCC[073] |
| A13 | VCC[007] | VCC[074] |
| A14 | VCC[008] | VCC[075] |
| A15 | VCC[009] | VCC[076] |
| A16 | VCC[010] | VCC[077] |
| A17 | VCC[011] | VCC[078] |
| A18 | VCC[012] | VCC[079] |
| A19 | VCC[013] | VCC[080] |
| A20 | VCC[014] | VCC[081] |
| B7 | VCC[015] | VCC[082] |
| B8 | VCC[016] | VCC[083] |
| B9 | VCC[017] | VCC[084] |
| B10 | VCC[018] | VCC[085] |
| B11 | VCC[019] | VCC[086] |
| B12 | VCC[020] | VCC[087] |
| B13 | VCC[021] | VCC[088] |
| B14 | VCC[022] | VCC[089] |
| B15 | VCC[023] | VCC[090] |
| B16 | VCC[024] | VCC[091] |
| B17 | VCC[025] | VCC[092] |
| B18 | VCC[026] | VCC[093] |
| C9 | VCC[027] | VCC[094] |
| C10 | VCC[028] | VCC[095] |
| C11 | VCC[029] | VCC[096] |
| C12 | VCC[030] | VCC[097] |
| C13 | VCC[031] | VCC[098] |
| C14 | VCC[032] | VCC[099] |
| C15 | VCC[033] | VCC[100] |
| C16 | VCC[034] | VCCP[01] |
| C17 | VCC[035] | VCCP[02] |
| C18 | VCC[036] | VCCP[03] |
| C19 | VCC[037] | VCCP[04] |
| C20 | VCC[038] | VCCP[05] |
| C21 | VCC[039] | VCCP[06] |
| C22 | VCC[040] | VCCP[07] |
| C23 | VCC[041] | VCCP[08] |
| C24 | VCC[042] | VCCP[09] |
| C25 | VCC[043] | VCCP[10] |
| C26 | VCC[044] | VCCP[11] |
| C27 | VCC[045] | VCCP[12] |
| C28 | VCC[046] | VCCP[13] |
| C29 | VCC[047] | VCCP[14] |
| C30 | VCC[048] | VCCP[15] |
| C31 | VCC[049] | VCCP[16] |
| C32 | VCC[050] | VCCA[01] |
| C33 | VCC[051] | VCCA[02] |
| C34 | VCC[052] | VID[0] |
| C35 | VCC[053] | VID[1] |
| C36 | VCC[054] | VID[2] |
| C37 | VCC[055] | VID[3] |
| C38 | VCC[056] | VID[4] |
| C39 | VCC[057] | VID[5] |
| C40 | VCC[058] | VID[6] |
| C41 | VCC[059] | VCCSENSE |
| C42 | VCC[060] | |
| C43 | VCC[061] | |
| C44 | VCC[062] | |
| C45 | VCC[063] | |
| C46 | VCC[064] | |
| C47 | VCC[065] | |
| C48 | VCC[066] | |
| C49 | VCC[067] | VSSSENSE |
| C50 | | |
| C51 | | |
| C52 | | |
| C53 | | |
| C54 | | |
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| C97 | | |
| C98 | | |
| C99 | | |
| C100 | | |



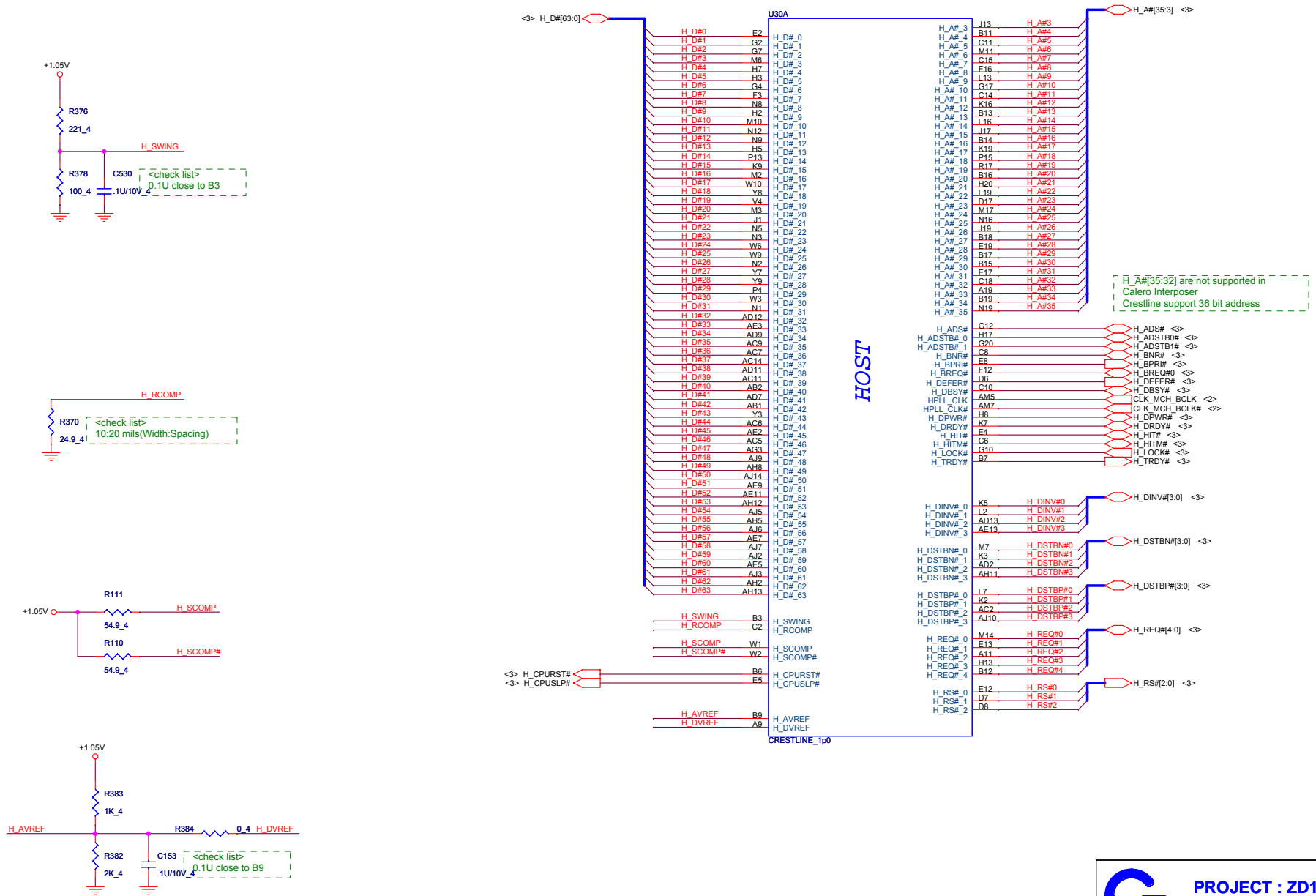
<REV.NO. 0.5/REF.NO.19343>
Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA



<Demo board>
Routing 27.4ohm with 50mils spacing
PU/PD near to CPU 1"

| U22D | | |
|------|----------|----------|
| A4 | VSS[001] | VSS[082] |
| A5 | VSS[002] | VSS[083] |
| A6 | VSS[003] | VSS[084] |
| A7 | VSS[004] | VSS[085] |
| A8 | VSS[005] | VSS[086] |
| A9 | VSS[006] | VSS[087] |
| A10 | VSS[007] | VSS[088] |
| A11 | VSS[008] | VSS[089] |
| A12 | VSS[009] | VSS[090] |
| A13 | VSS[010] | VSS[091] |
| A14 | VSS[011] | VSS[092] |
| A15 | VSS[012] | VSS[093] |
| A16 | VSS[013] | VSS[094] |
| A17 | VSS[014] | VSS[095] |
| A18 | VSS[015] | VSS[096] |
| A19 | VSS[016] | VSS[097] |
| A20 | VSS[017] | VSS[098] |
| B7 | VSS[018] | VSS[099] |
| B8 | VSS[019] | VSS[100] |
| B9 | VSS[020] | VSS[101] |
| B10 | VSS[021] | VSS[102] |
| B11 | VSS[022] | VSS[103] |
| B12 | VSS[023] | VSS[104] |
| B13 | VSS[024] | VSS[105] |
| B14 | VSS[025] | VSS[106] |
| B15 | VSS[026] | VSS[107] |
| B16 | VSS[027] | VSS[108] |
| B17 | VSS[028] | VSS[109] |
| B18 | VSS[029] | VSS[110] |
| B19 | VSS[030] | VSS[111] |
| B20 | VSS[031] | VSS[112] |
| B21 | VSS[032] | VSS[113] |
| B22 | VSS[033] | VSS[114] |
| B23 | VSS[034] | VSS[115] |
| B24 | VSS[035] | VSS[116] |
| B25 | VSS[036] | VSS[117] |
| B26 | VSS[037] | VSS[118] |
| B27 | VSS[038] | VSS[119] |
| B28 | VSS[039] | VSS[120] |
| B29 | VSS[040] | VSS[121] |
| B30 | VSS[041] | VSS[122] |
| B31 | VSS[042] | VSS[123] |
| B32 | VSS[043] | VSS[124] |
| B33 | VSS[044] | VSS[125] |
| B34 | VSS[045] | VSS[126] |
| B35 | VSS[046] | VSS[127] |
| B36 | VSS[047] | VSS[128] |
| B37 | VSS[048] | VSS[129] |
| B38 | VSS[049] | VSS[130] |
| B39 | VSS[050] | VSS[131] |
| B40 | VSS[051] | VSS[132] |
| B41 | VSS[052] | VSS[133] |
| B42 | VSS[053] | VSS[134] |
| B43 | VSS[054] | VSS[135] |
| B44 | VSS[055] | VSS[136] |
| B45 | VSS[056] | VSS[137] |
| B46 | VSS[057] | VSS[138] |
| B47 | VSS[058] | VSS[139] |
| B48 | VSS[059] | VSS[140] |
| B49 | VSS[060] | VSS[141] |
| B50 | VSS[061] | VSS[142] |
| B51 | VSS[062] | VSS[143] |
| B52 | VSS[063] | VSS[144] |
| B53 | VSS[064] | VSS[145] |
| B54 | VSS[065] | VSS[146] |
| B55 | VSS[066] | VSS[147] |
| B56 | VSS[067] | VSS[148] |
| B57 | VSS[068] | VSS[149] |
| B58 | VSS[069] | VSS[150] |
| B59 | VSS[070] | VSS[151] |
| B60 | VSS[071] | VSS[152] |
| B61 | VSS[072] | VSS[153] |
| B62 | VSS[073] | VSS[154] |
| B63 | VSS[074] | VSS[155] |
| B64 | VSS[075] | VSS[156] |
| B65 | VSS[076] | VSS[157] |
| B66 | VSS[077] | VSS[158] |
| B67 | VSS[078] | VSS[159] |
| B68 | VSS[079] | VSS[160] |
| B69 | VSS[080] | VSS[161] |
| B70 | VSS[081] | VSS[162] |
| B71 | VSS[082] | VSS[163] |

Merom Ball-out Rev 1a



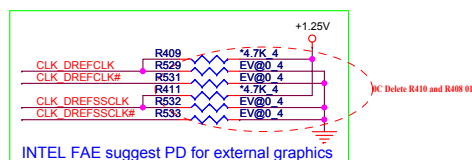
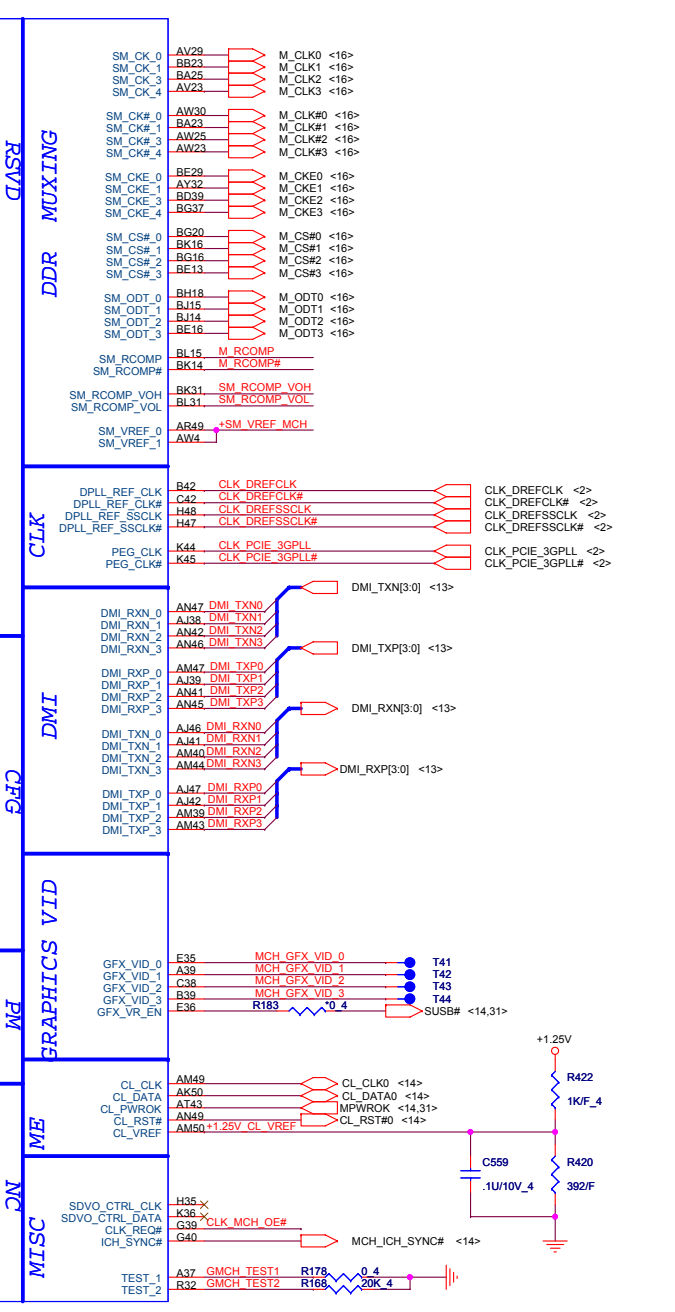
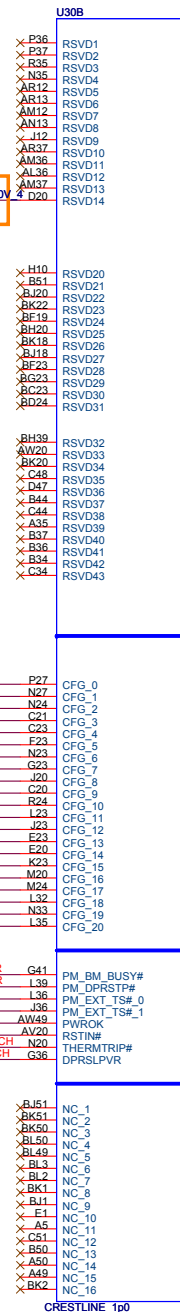
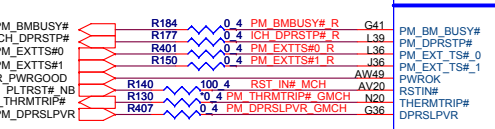
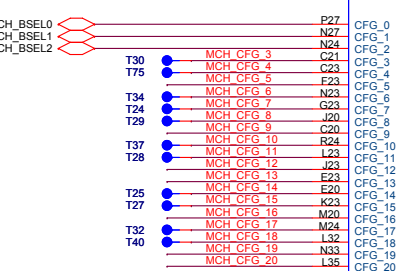
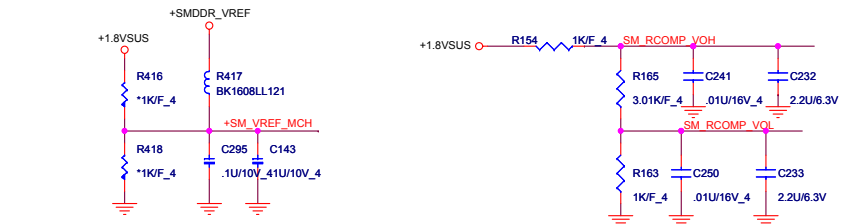
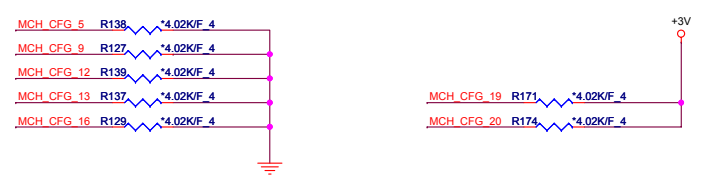
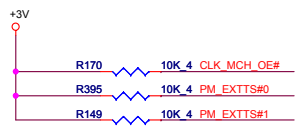
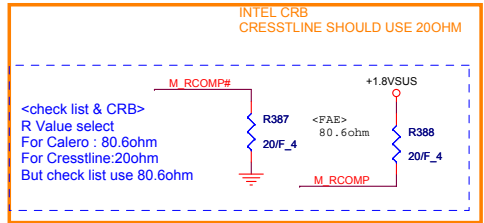
PROJECT : ZD1
Quanta Computer Inc.

| | | |
|-------|-----------------------|---------------|
| Size | Document Number | Rev |
| | GMCH HOST(1/7) | E |
| Date: | Monday, May 07, 2007 | Sheet 5 of 38 |

Strapping table

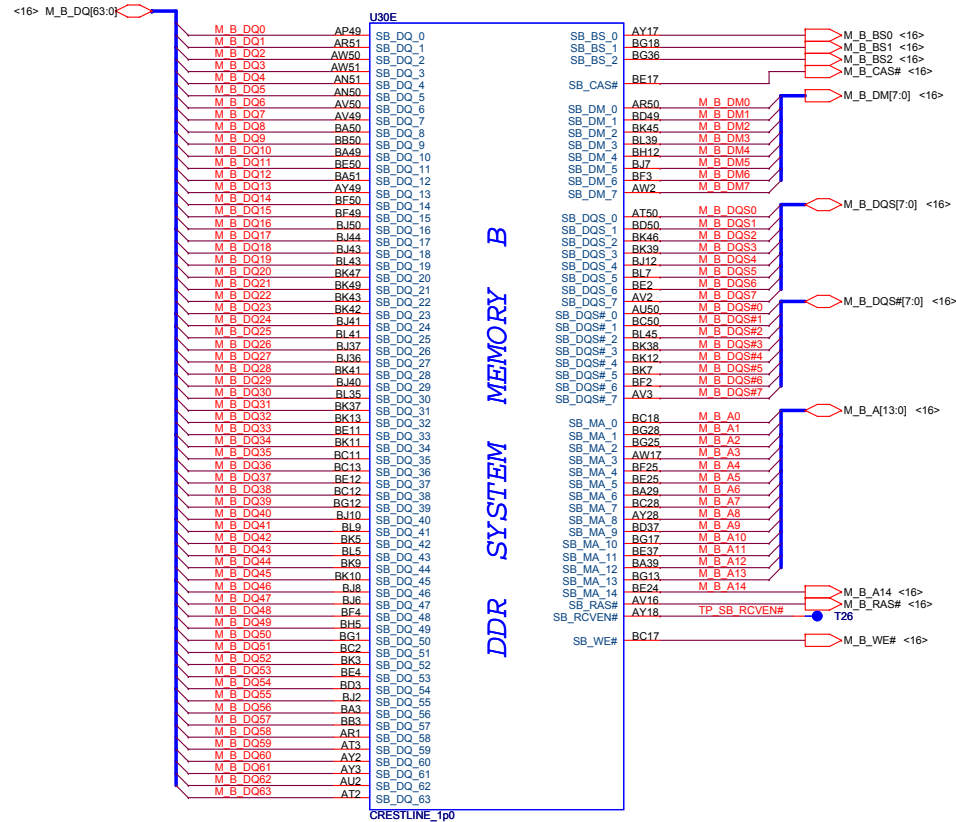
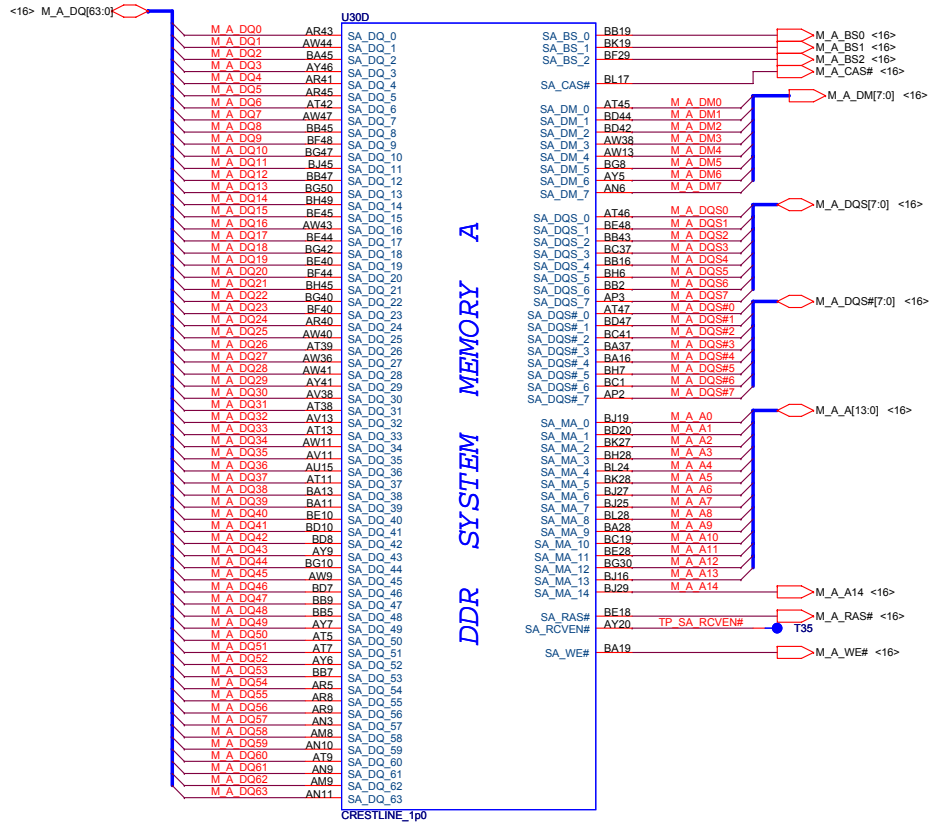
All strap are sampled with respect to the leading edge of the GMCH power ok signal
 CFG[17:3] have internal pull-up
 CFG[18:19] have internal pull-down
 Any CFG signal strapping option not list below should be left NC pin

| Pin Name | Strap Description | Configuration |
|---------------|------------------------------------|---|
| CFG[2:0] | FSB Frequency Select | 010 = FSB 800MHz 011 = FSB 667MHz |
| CEG[4:3] | Reserved | |
| CFG5 | DMI X2 Select | 0 = DMI X2 1 = DMI X4 (Default) |
| CFG6 | Reserved | |
| CFG7 | CPU Strap | 0 = Mobile 1 = Reserved CPU (Default) |
| CFG8 | Low Power PCI Express | 0 = Normal mode 1 = Low Power mode |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reserved Lanes 1 = Normal operation (Default) |
| CFG[11:10] | Reserved | |
| CFG[13:12] | XOR/ ALLZ/ Clock Un gating | 00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal C operation (Default) |
| CFG[15:14] | Reserved | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default) |
| CFG[18:17] | Reserved | |
| CFG19 | DMI Lane Reversal | 0 = Normal operation 1 = Reverse Lanes (Default) |
| CFG20 | SDVO/PCIe concurrent | 0 = Only SDVO or PCIe x1 is operation (Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card present (Default) 1 = SDVO Card Present |

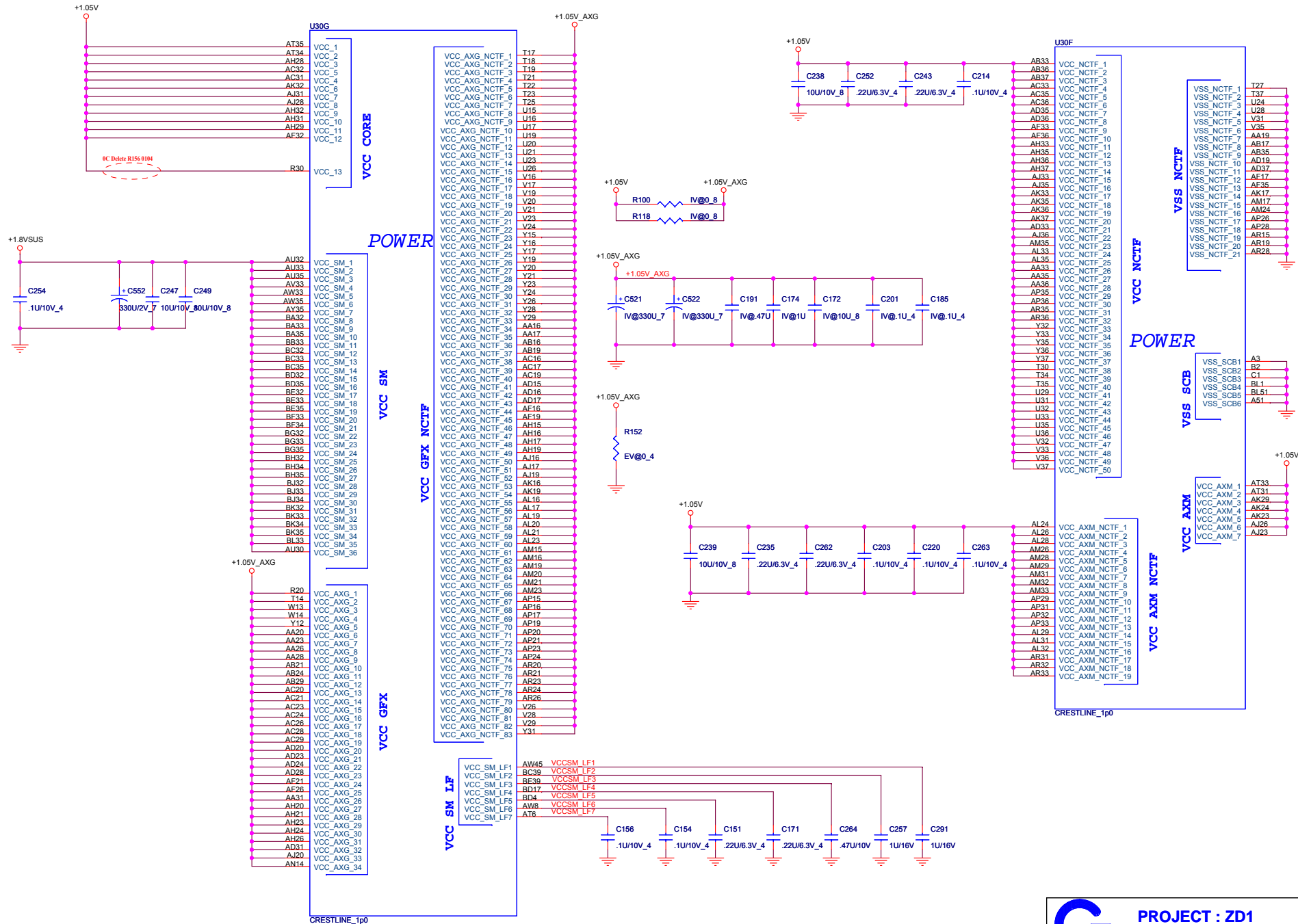


PROJECT : ZD1
Quanta Computer Inc.

| | | |
|-------|-----------------------------------|---------------|
| Size | Document Number | Rev |
| | GMCH (STRAPPING/OTHER 3/7) | E |
| Date: | Monday, May 07, 2007 | Sheet 7 of 38 |

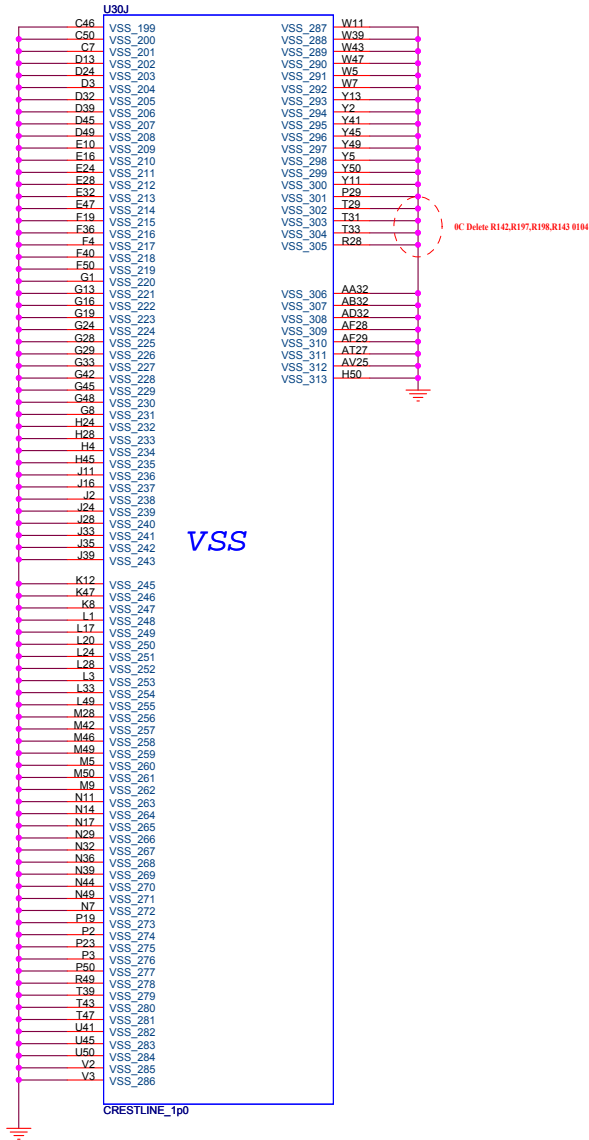
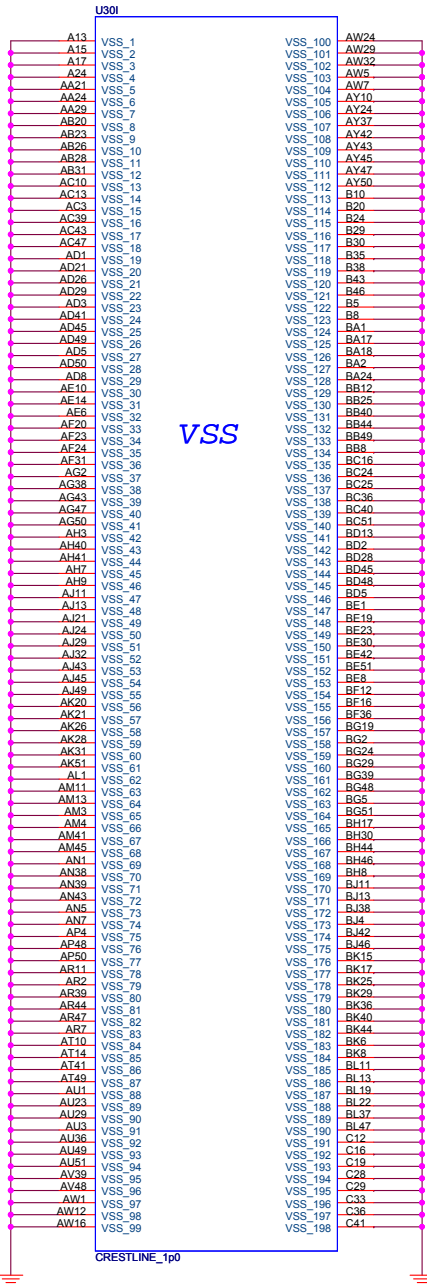


NB(Power-1)

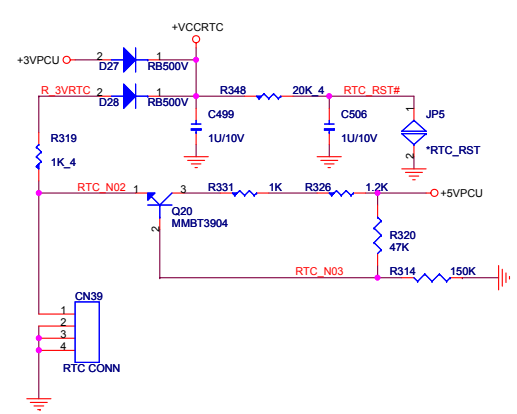


PROJECT : ZD1
Quanta Computer Inc.

| | | |
|-------|---------------------------|---------------|
| Size | Document Number | Rev |
| | GMCH Power-1(5/7) | E |
| Date: | Wednesday, April 25, 2007 | Sheet 9 of 38 |



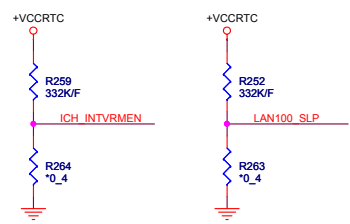
RTC



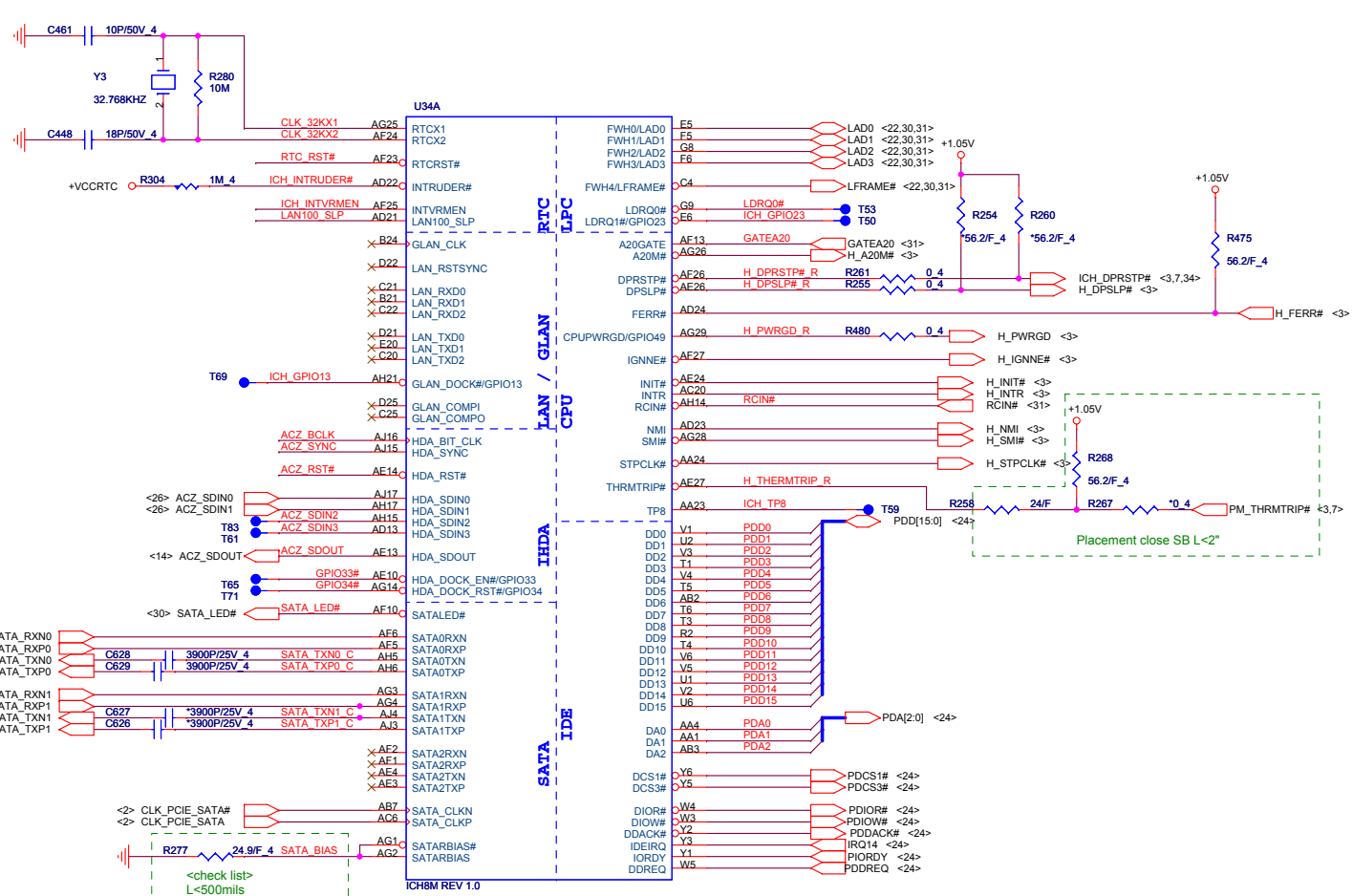
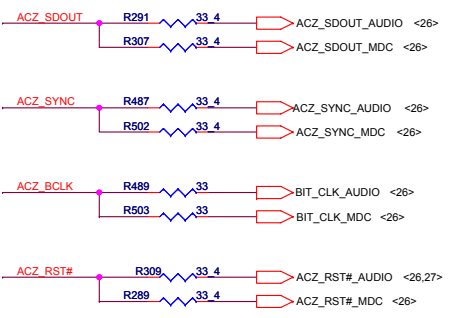
SB Strap

| | |
|----------|---|
| INTVRMEN | Low = Internal VR disable High = Internal VR enable(Default) |
|----------|---|

| | |
|------------|---|
| LAN100_SLP | Low = Internal VR disable High = Internal VR enable(Default) |
|------------|---|



HDA

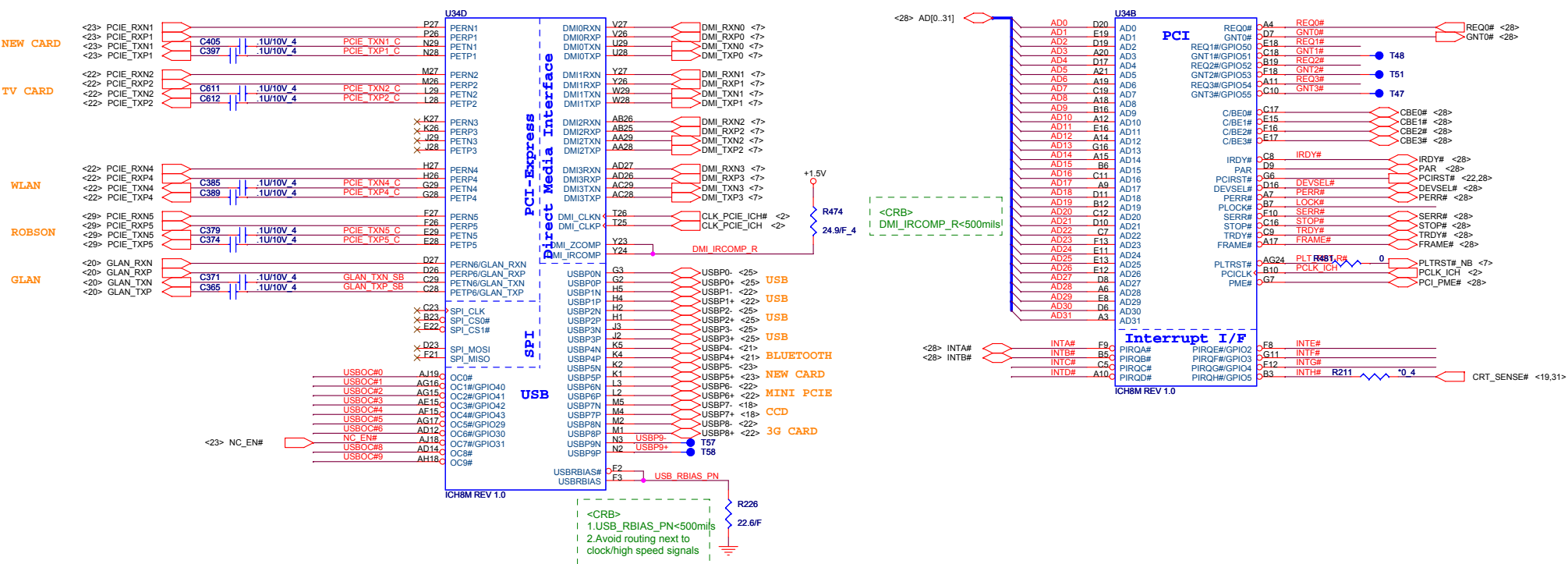


0810 UR FAE:
RCIN# DOESN'T NEED PU



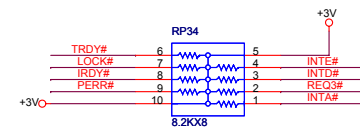
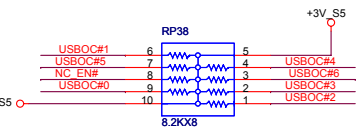
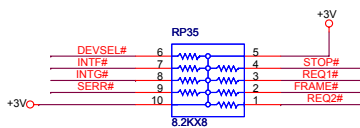
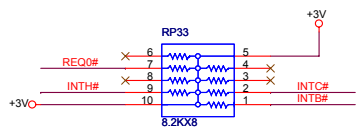
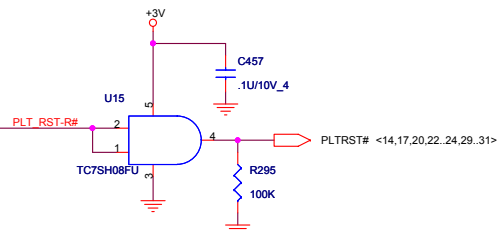
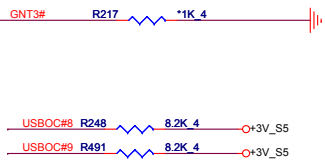
SB-PCIE/USB/DMI

SB-PCI



A16 SWAP Override strap

| | |
|-----------|---|
| PCI_GNT#3 | Low = A16 swap override enabled High = Default |
|-----------|---|

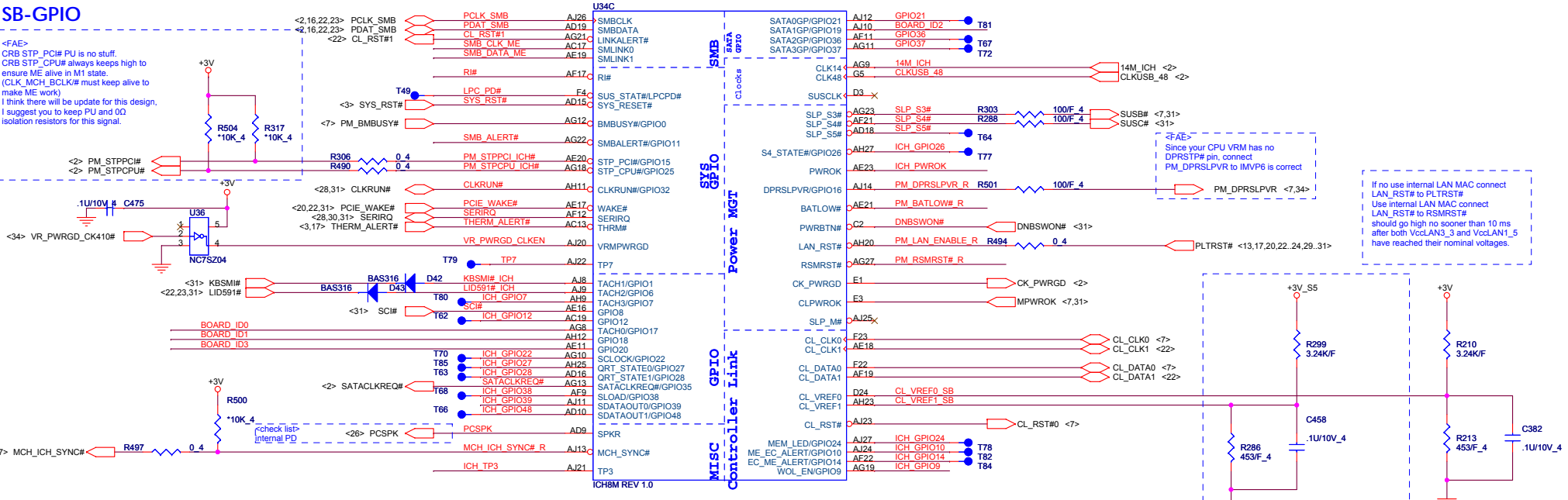


PROJECT : ZD1
Quanta Computer Inc.

| | | |
|-------|-------------------------------|----------------|
| Size | Document Number | Rev |
| | ICH8M PCIE/PC/USB(2/4) | E |
| Date: | Monday, May 07, 2007 | Sheet 13 of 38 |

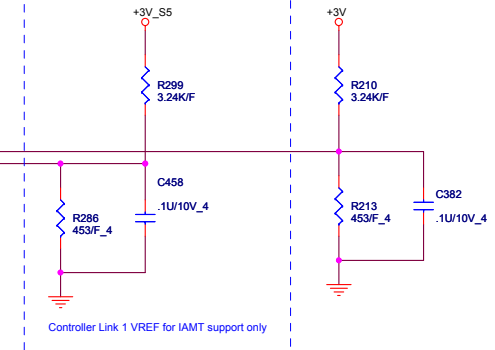
SB-GPIO

<FAE>
 CRB STP_CPU# PU is no stuff.
 CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
 (CLK_MCH_BCLK# must keep alive to make ME work)
 I think there will be update for this design.
 I suggest you to keep PU and 0Ω isolation resistors for this signal.



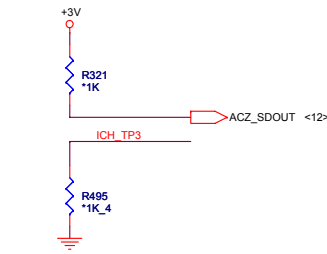
<FAE>
 Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

If no use internal LAN MAC connect LAN_RST# to PLTRST#
 Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.



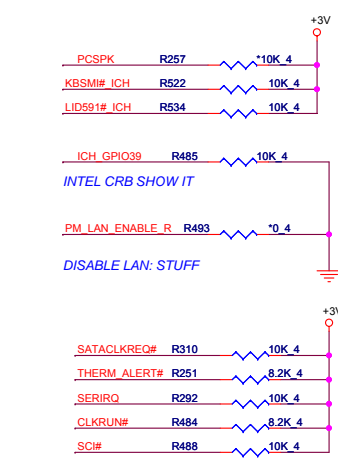
XOR Chain Entrance Strap

| ICH_RSVD0 | HDA_SDOUT | Description |
|-----------|-----------|----------------------------|
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal operation(Default) |
| 1 | 1 | Set PCIe port config bit 1 |

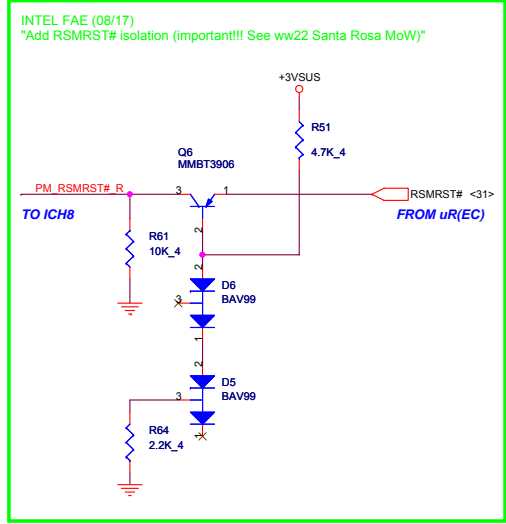
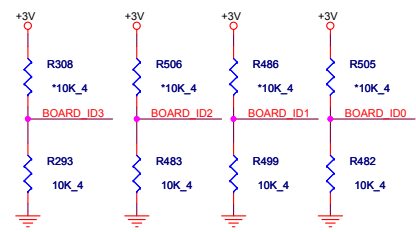


No Reboot strap

| | |
|----------|-----------------------------------|
| HDA_SPKR | Low = Default High = No Reboot |
|----------|-----------------------------------|

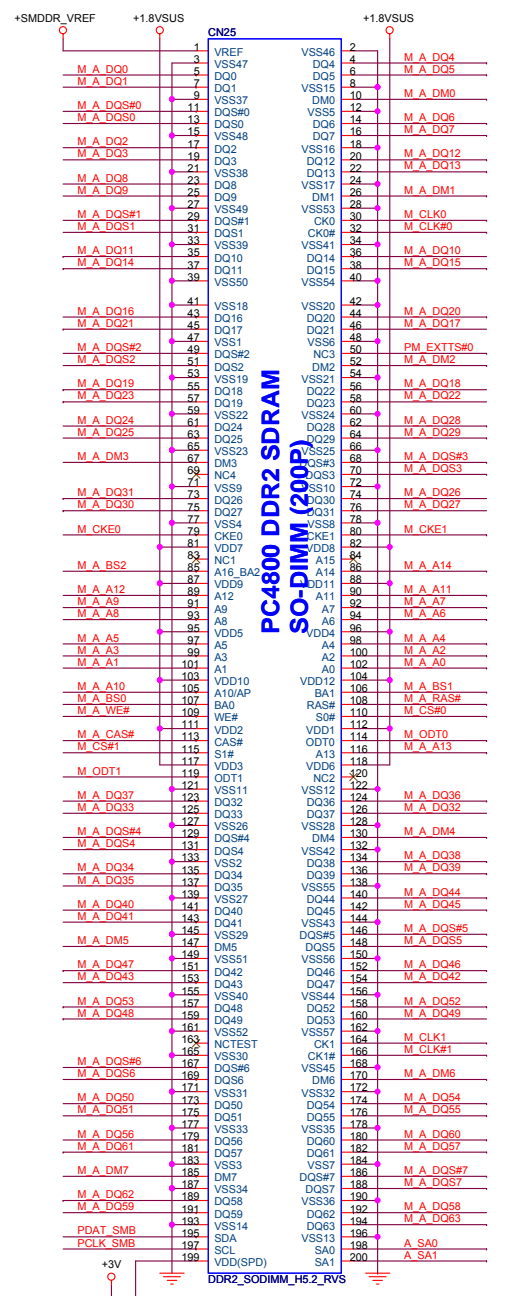


| Board ID | ID3 | ID2 | ID1 | ID0 |
|----------|-----|-----|-----|-----|
| | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 1 |
| | 0 | 0 | 1 | 0 |
| | 0 | 0 | 1 | 1 |
| | 0 | 1 | 0 | 0 |



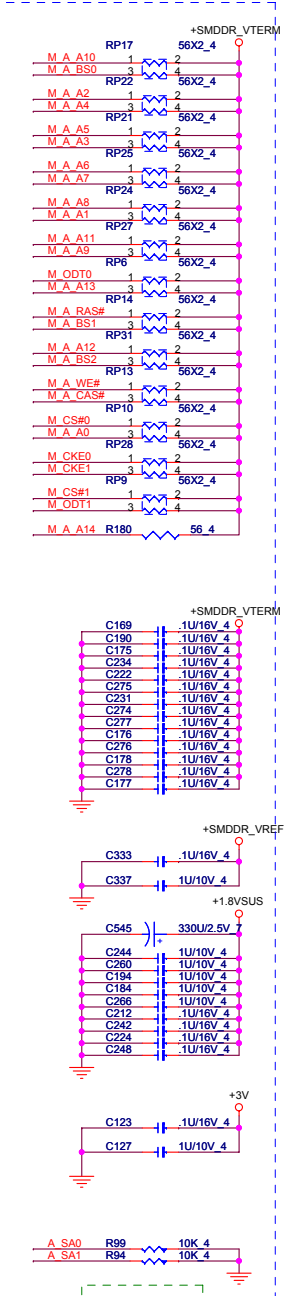
PROJECT : ZD1
Quanta Computer Inc.

Size: Document Number
ICH8M GPIO(3/4)
 Date: Monday, May 07, 2007 Sheet 14 of 38 Rev E



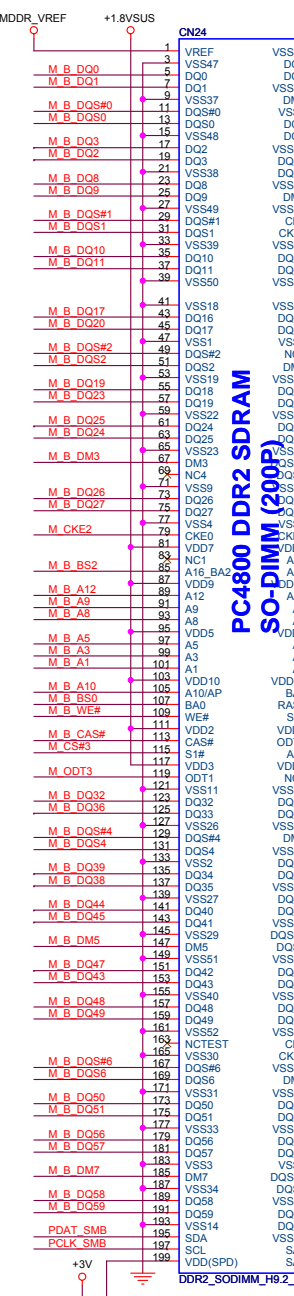
SO-DIMM0

SMbus address A0



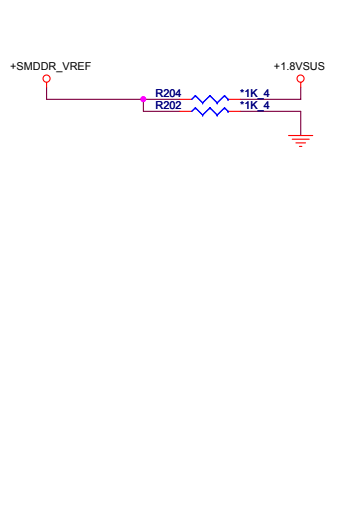
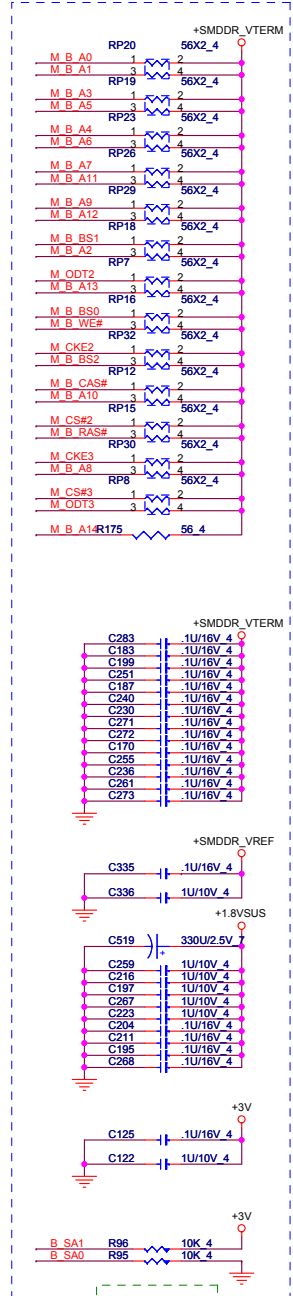
SO-DIMM1

SMbus address A2



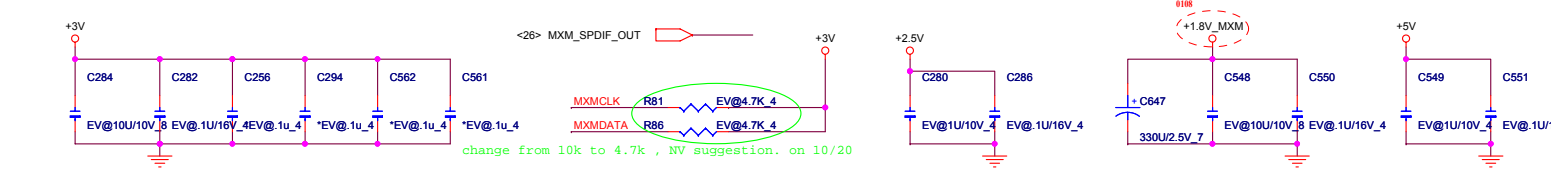
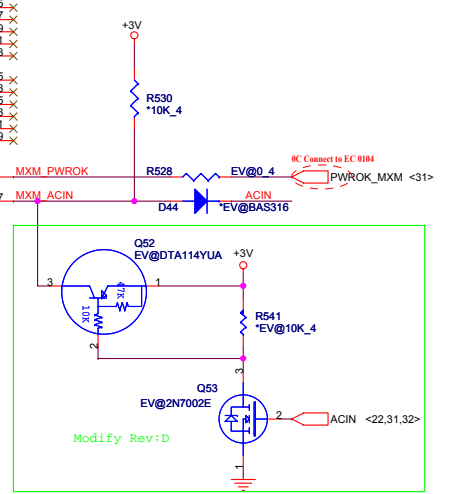
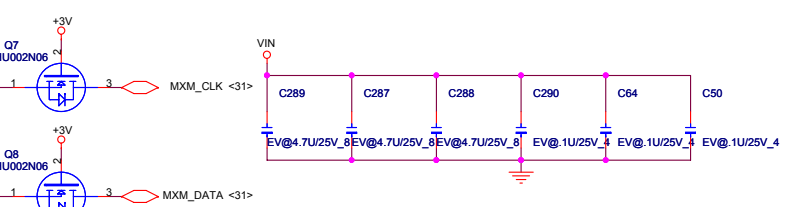
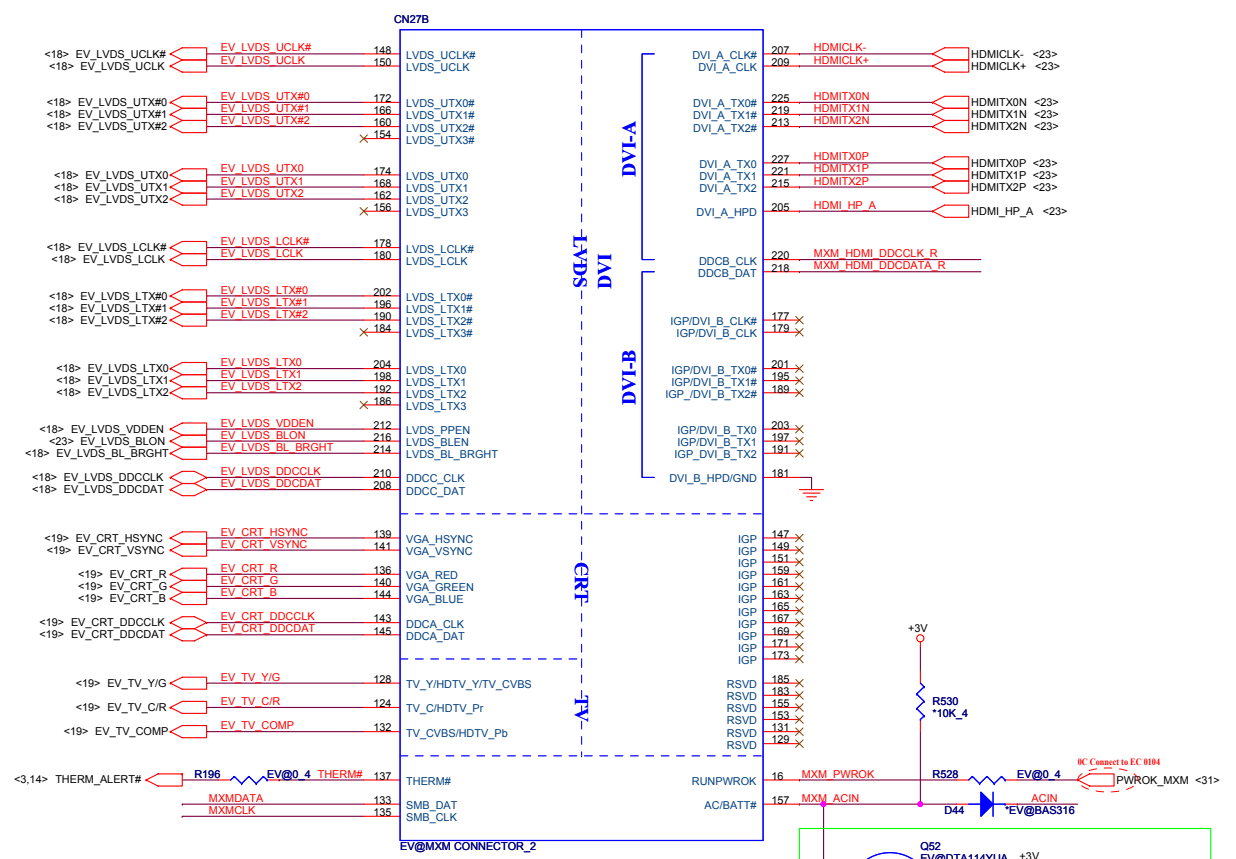
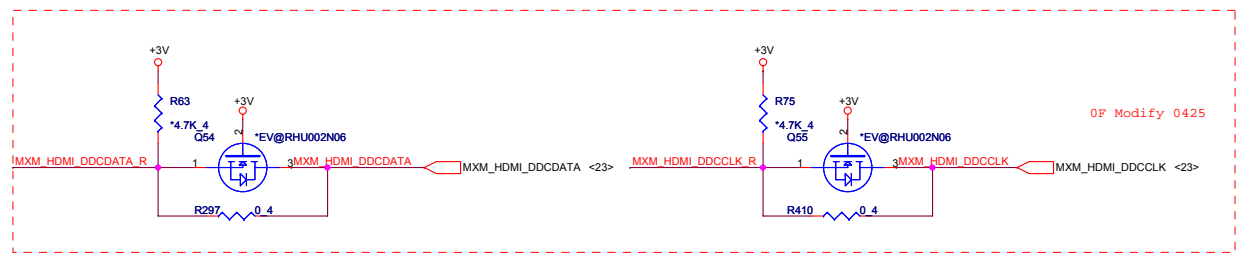
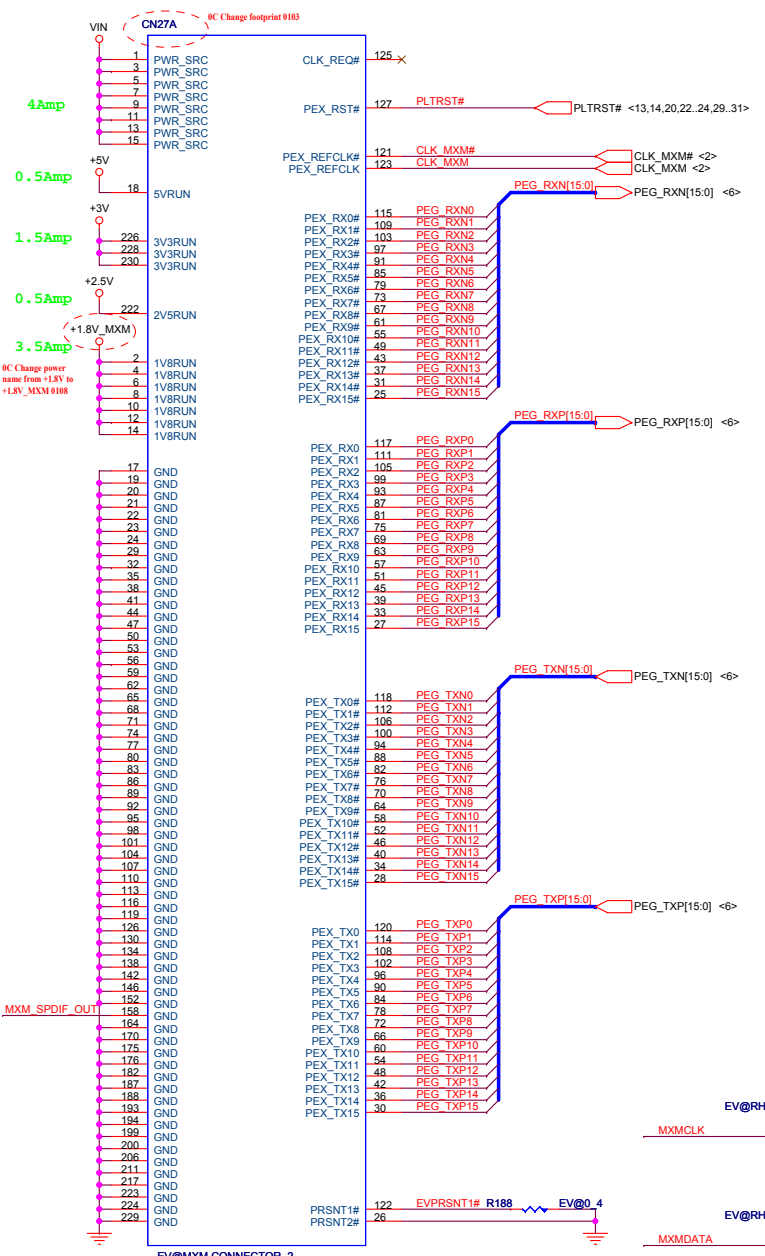
SO-DIMM2

SMbus address A2



- <7> PM_EXTTS#1 PM_EXTTS#1
- <7> PM_EXTTS#0 PM_EXTTS#0
- <2,14,22,23> PDAT_SMB PDAT_SMB
- <2,14,22,23> PCLK_SMB PCLK_SMB
- <7> M_CS#(3:0) M_CS#(3:0)
- <7> M_ODT(3:0) M_ODT(3:0)
- <7> M_CKE(3:0) M_CKE(3:0)
- <7> M_CLK#(3:0) M_CLK#(3:0)
- <7> M_CLK(3:0) M_CLK(3:0)
- <8> M_A_CAS# M_A_CAS#
- <8> M_A_RAS# M_A_RAS#
- <8> M_A_WE# M_A_WE#
- <8> M_A_BS(2:0) M_A_BS(2:0)
- <8> M_A_DM(7:0) M_A_DM(7:0)
- <8> M_A_DQS(7:0) M_A_DQS(7:0)
- <8> M_A_A[14:0] M_A_A[14:0]
- <8> M_A_DQ(63:0) M_A_DQ(63:0)
- <8> M_B_CAS# M_B_CAS#
- <8> M_B_RAS# M_B_RAS#
- <8> M_B_WE# M_B_WE#
- <8> M_B_BS(2:0) M_B_BS(2:0)
- <8> M_B_DM(7:0) M_B_DM(7:0)
- <8> M_B_DQS(7:0) M_B_DQS(7:0)
- <8> M_B_A[14:0] M_B_A[14:0]
- <8> M_B_DQ(63:0) M_B_DQ(63:0)

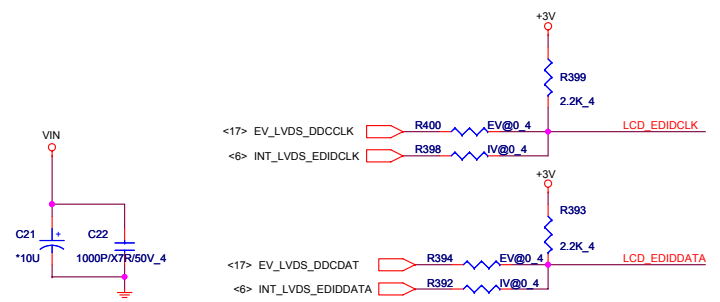
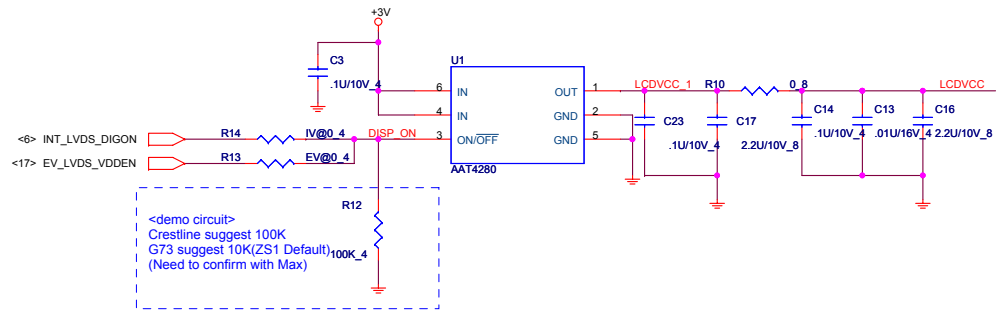
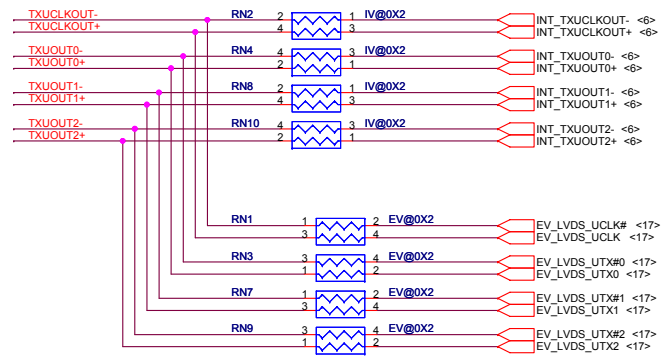
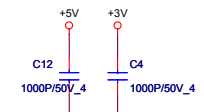
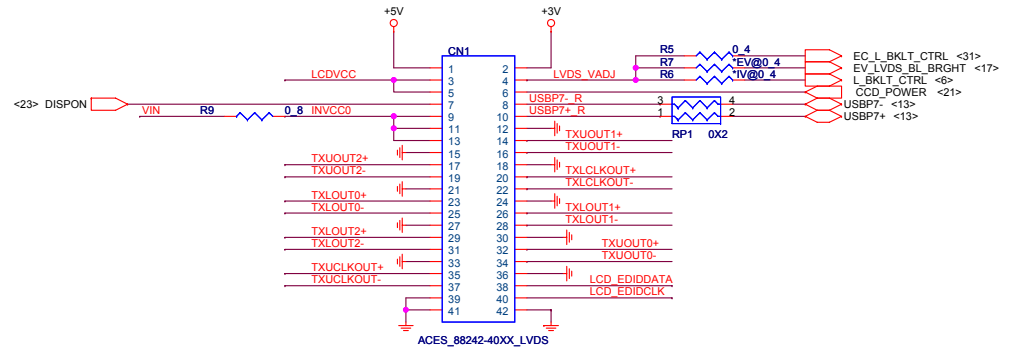
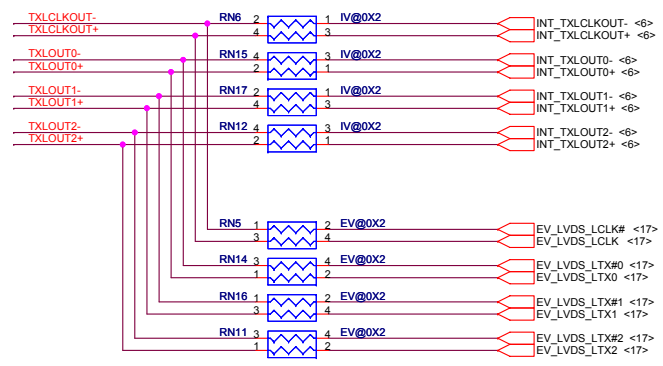
PROJECT : ZD1
Quanta Computer Inc.



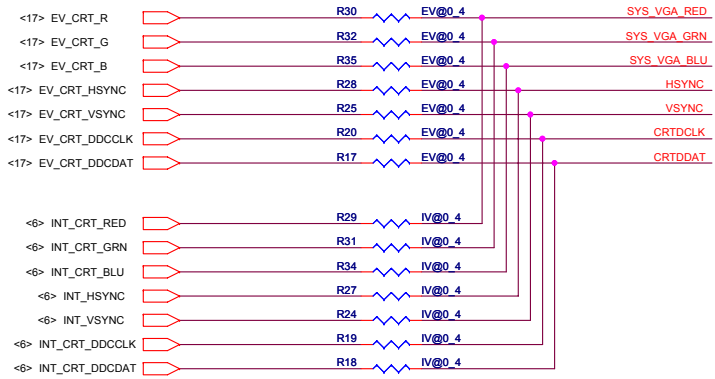
PROJECT : ZD1
Quanta Computer Inc.

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|------|-----------------|-----|
| Size | Document Number | Rev |
| | MXM | E |

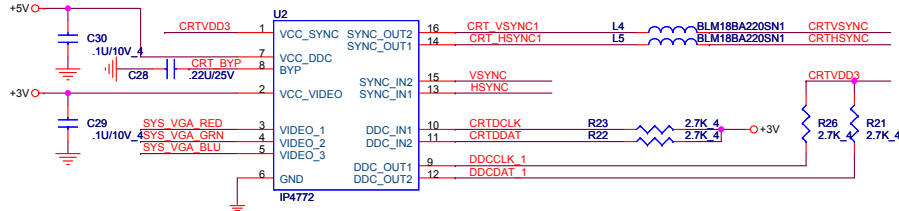
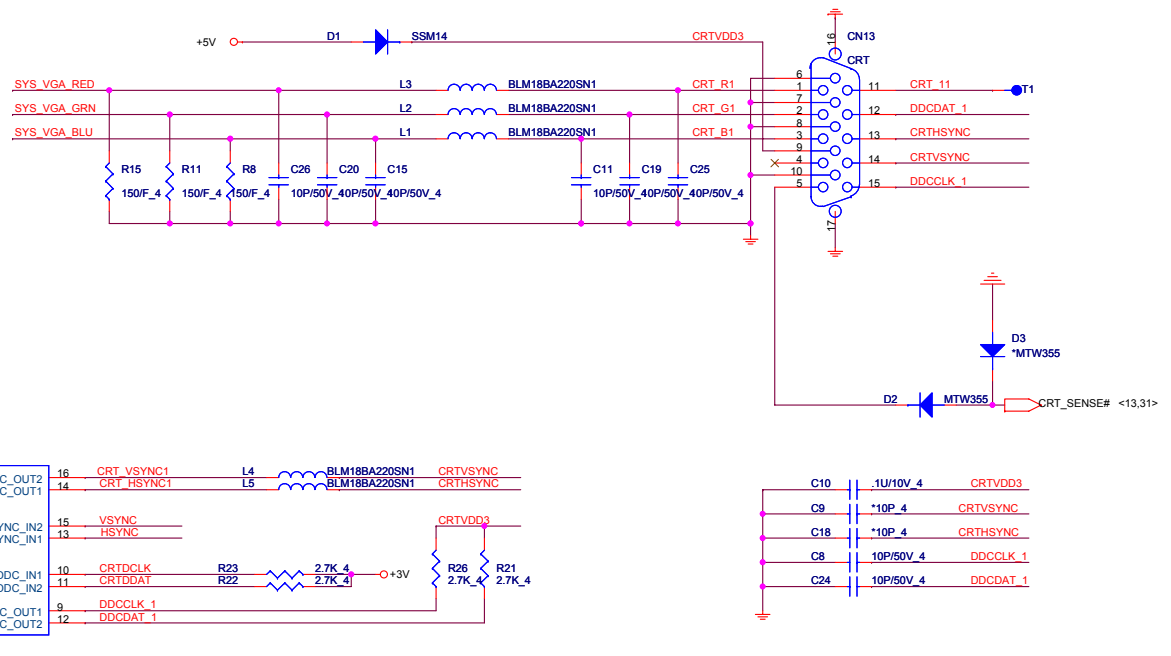
Date: Monday, May 07, 2007 Sheet 17 of 38



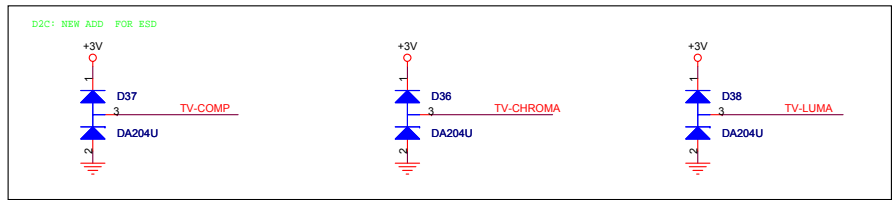
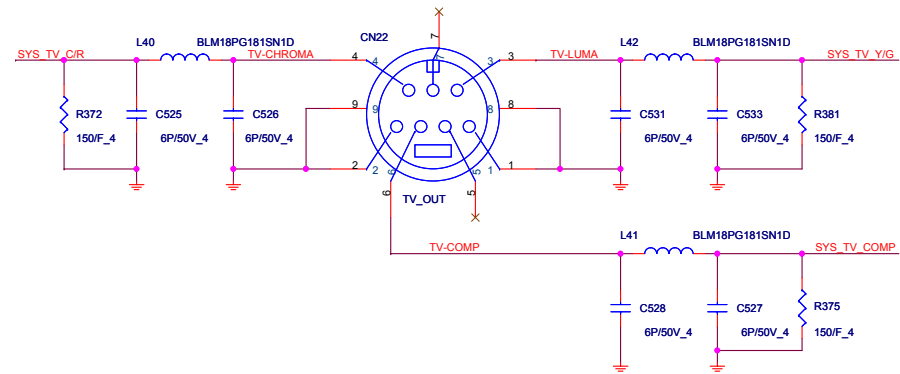
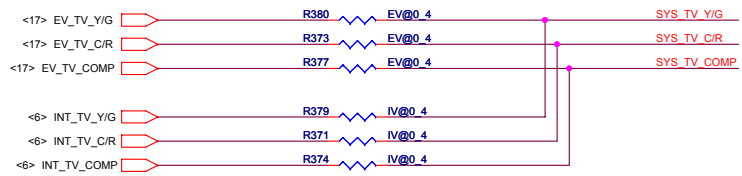
CRT Select



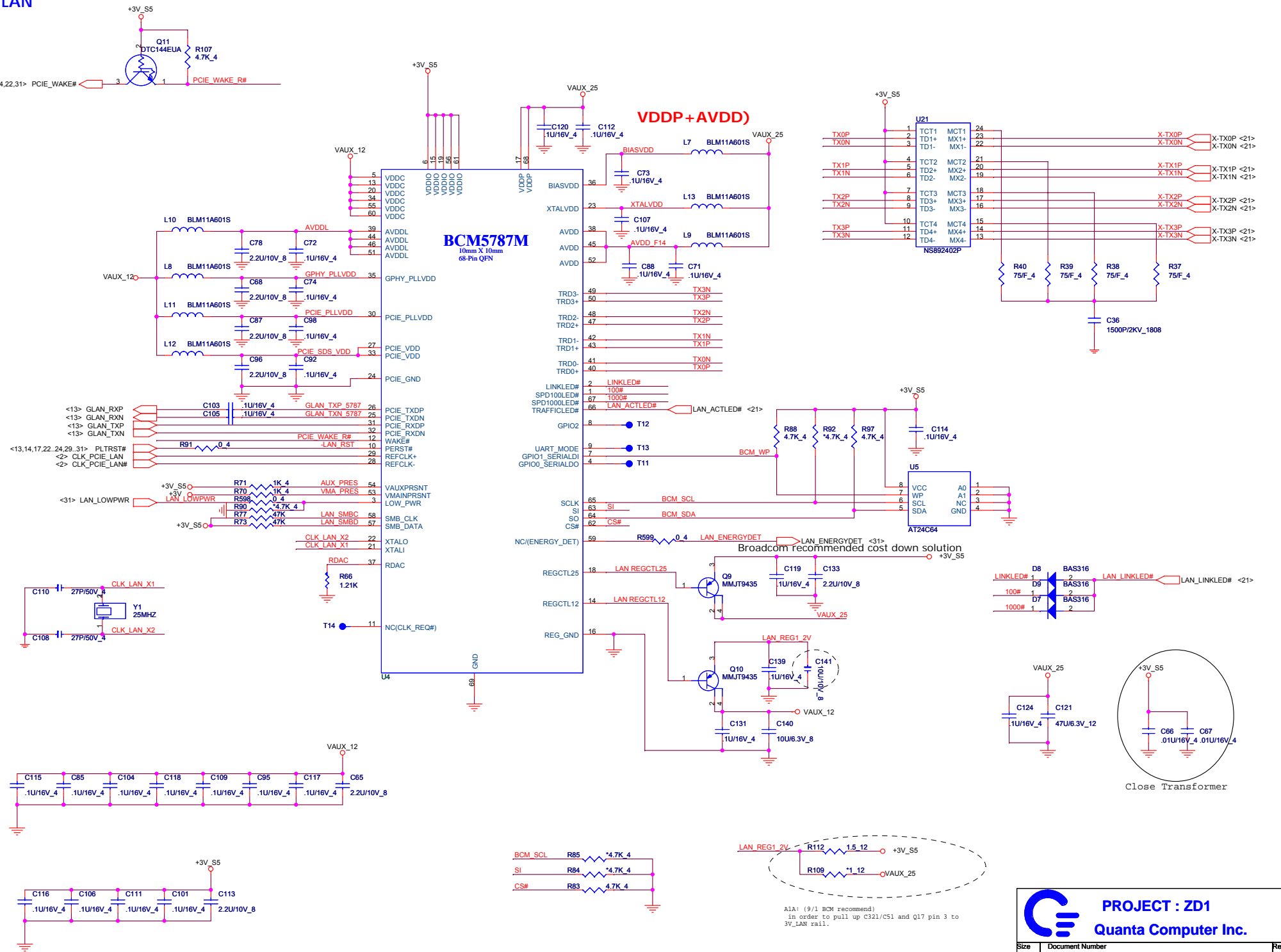
CRT CONNECTOR AND ESD



TV Out (SVHS) MiniDIN 7-pin



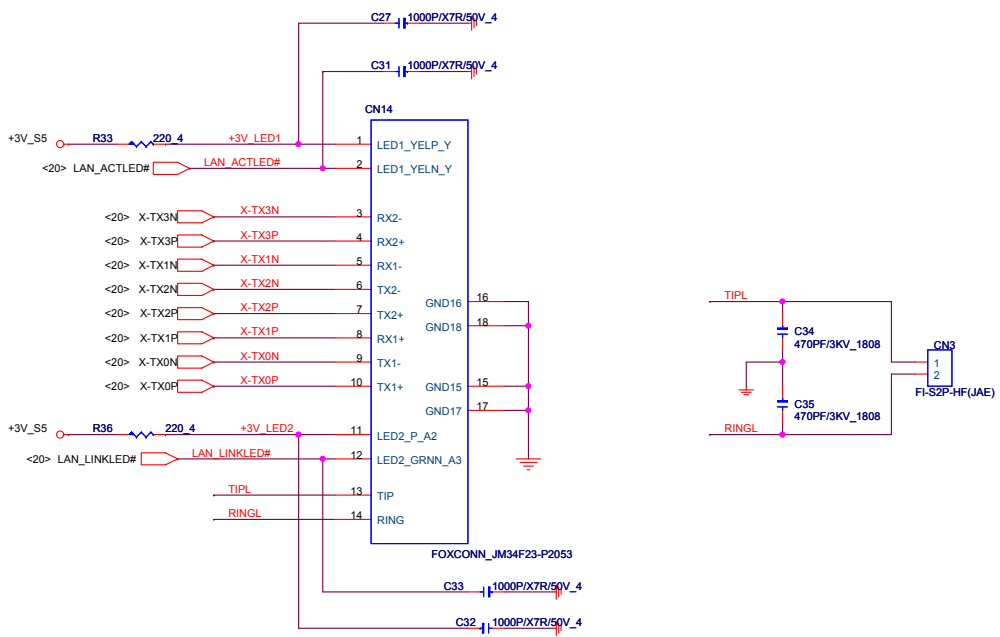
PROJECT : ZD1
Quanta Computer Inc.
 Size: Document Number: **CRT/TVOUT** Rev: E
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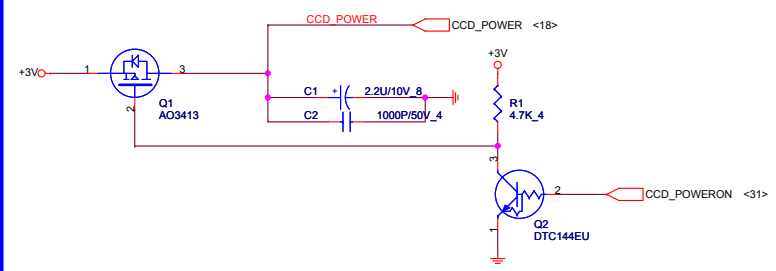
PROJECT : ZD1
Quanta Computer Inc.

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|-------|--------------------------------|----------------|
| Size | Document Number | Rev |
| | BCM5787 LAN/TRANSFORMER | E |
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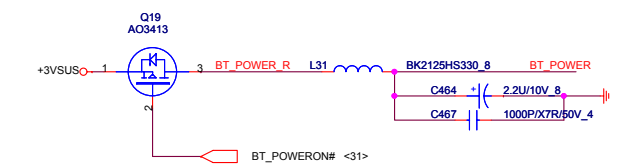
RJ45-11



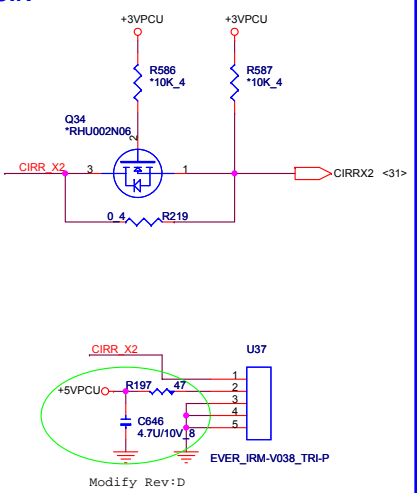
CAMERA MODULE CONNECTOR



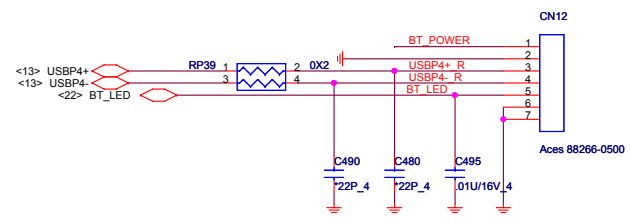
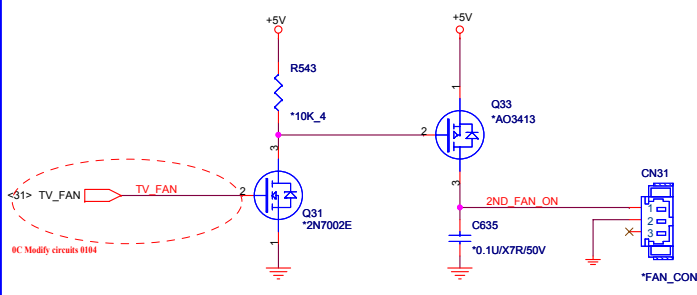
BLUETOOTH MODULE CONNECTOR



CIR



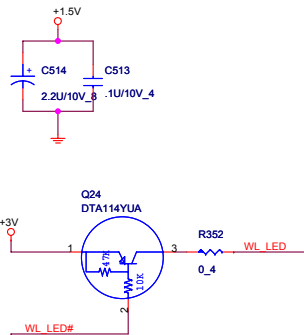
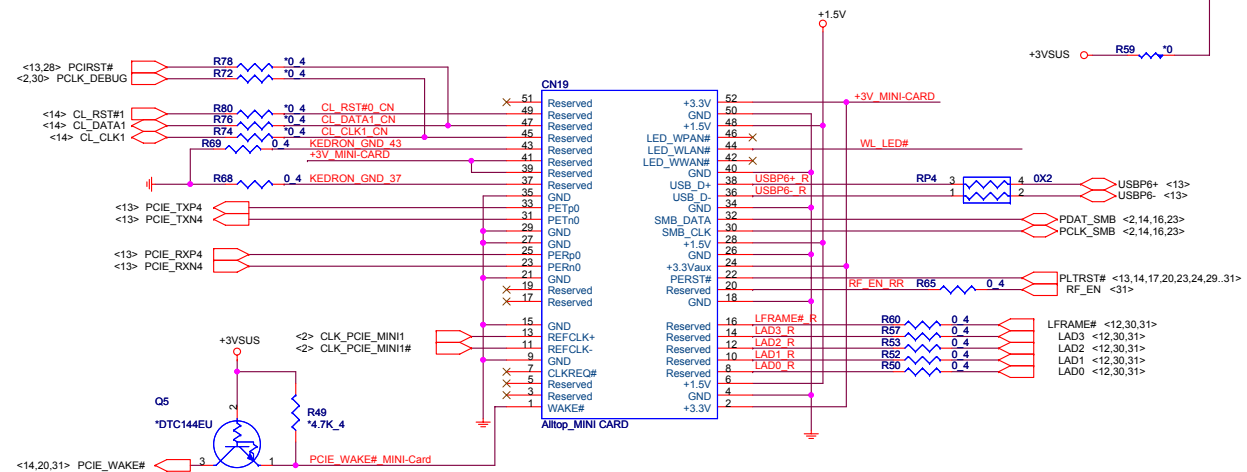
2nd FAN



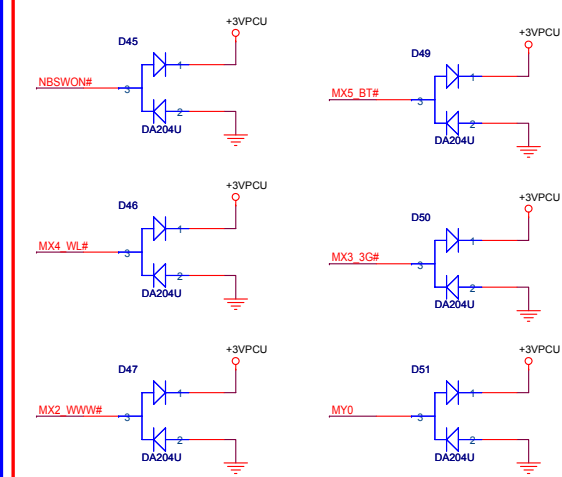
PROJECT : ZD1
Quanta Computer Inc.

| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | BT/CCD/RJ45-11/CIR/2nd FAN | E |
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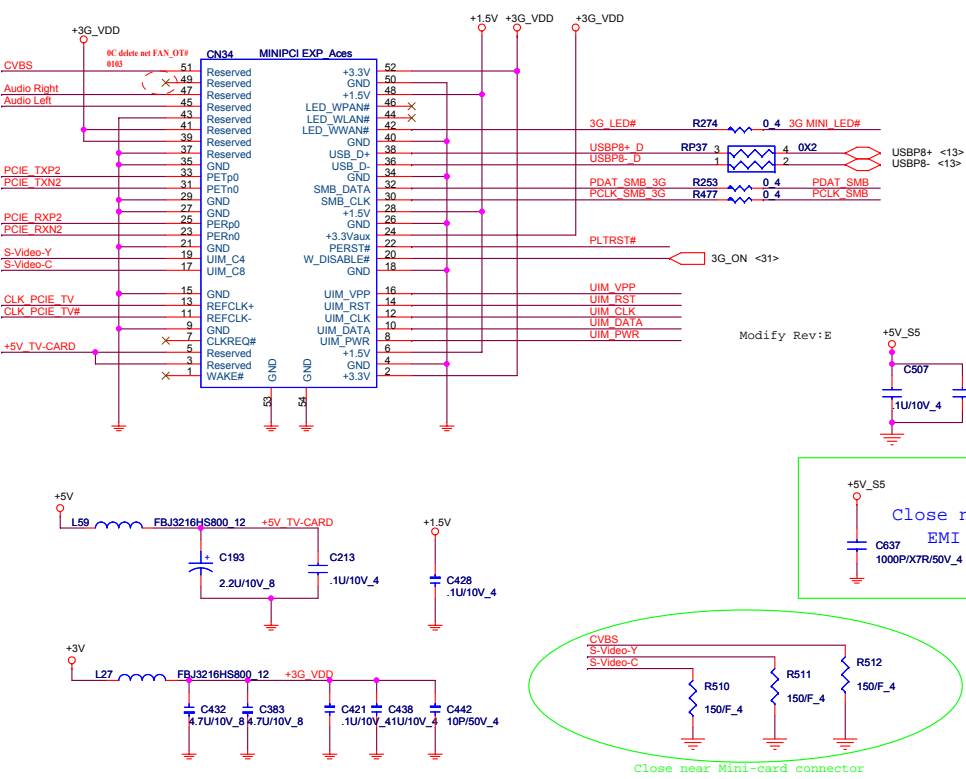
MINI-Card



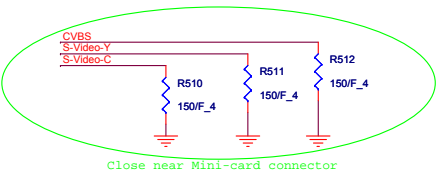
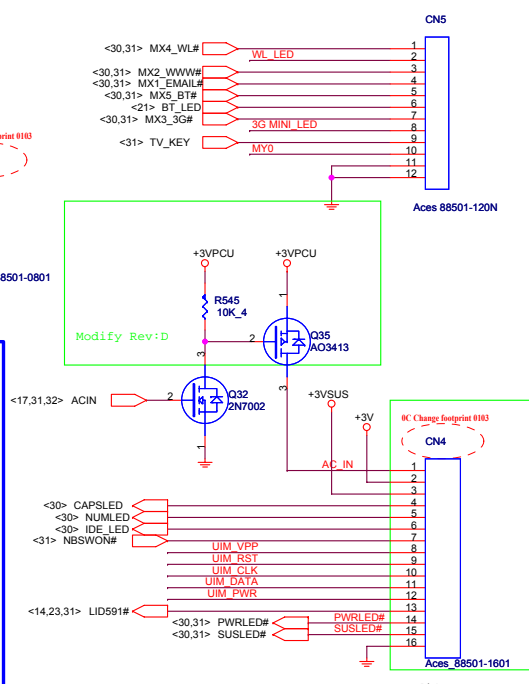
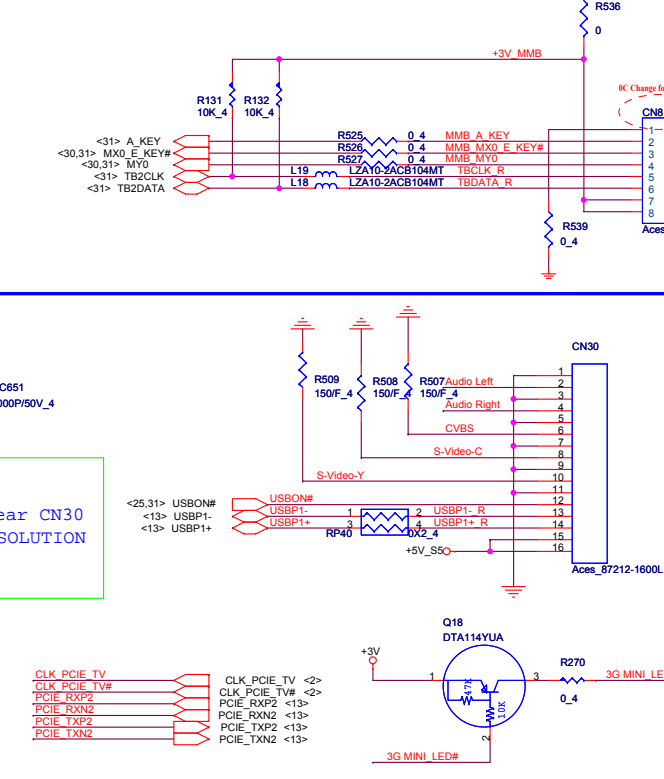
For ESD close to conn. side



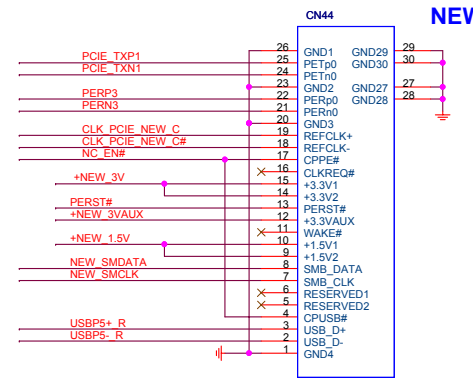
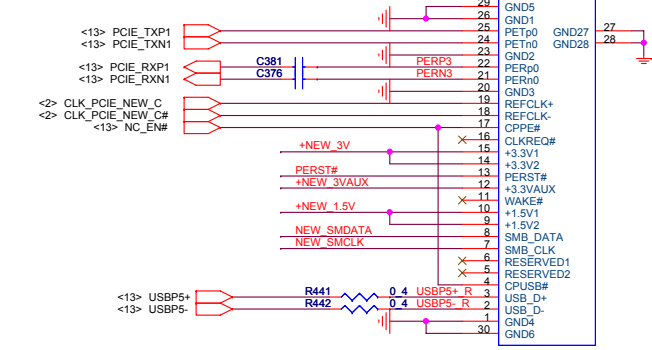
3G/TV MINI CARD



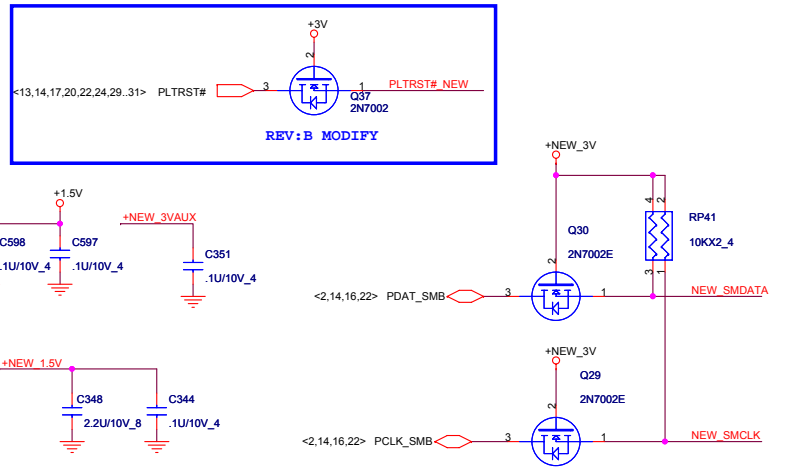
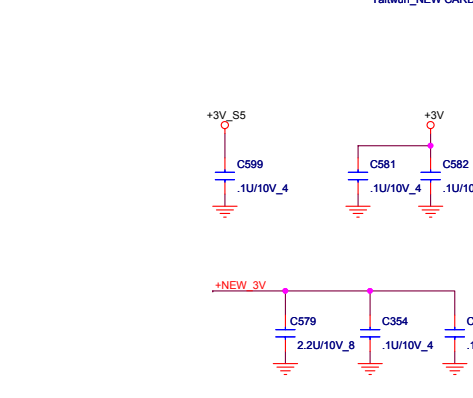
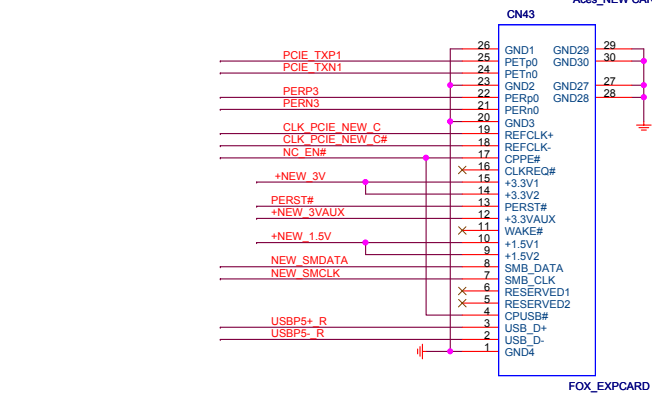
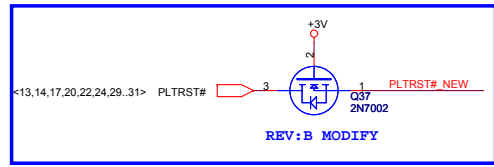
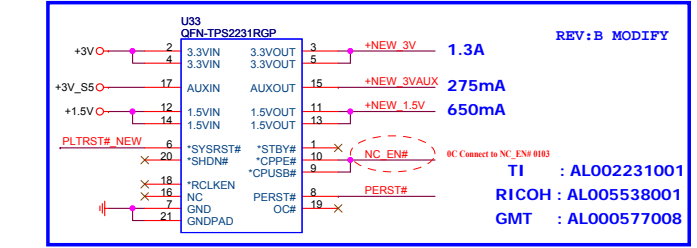
Media Key



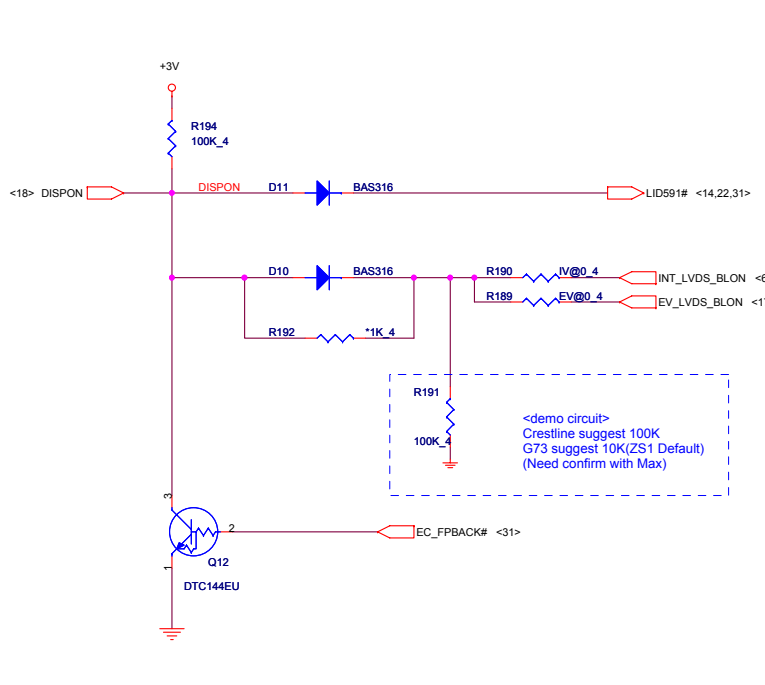
New card



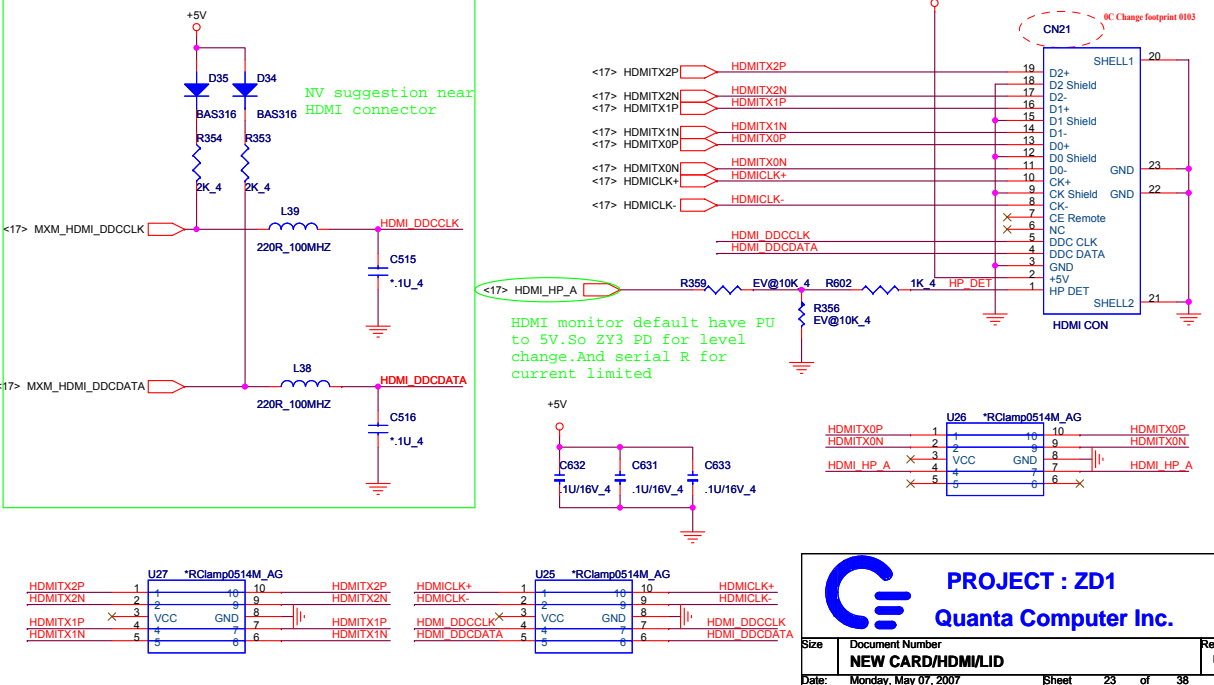
NEW CARD'S POWER SWITCH



LID SWITCH



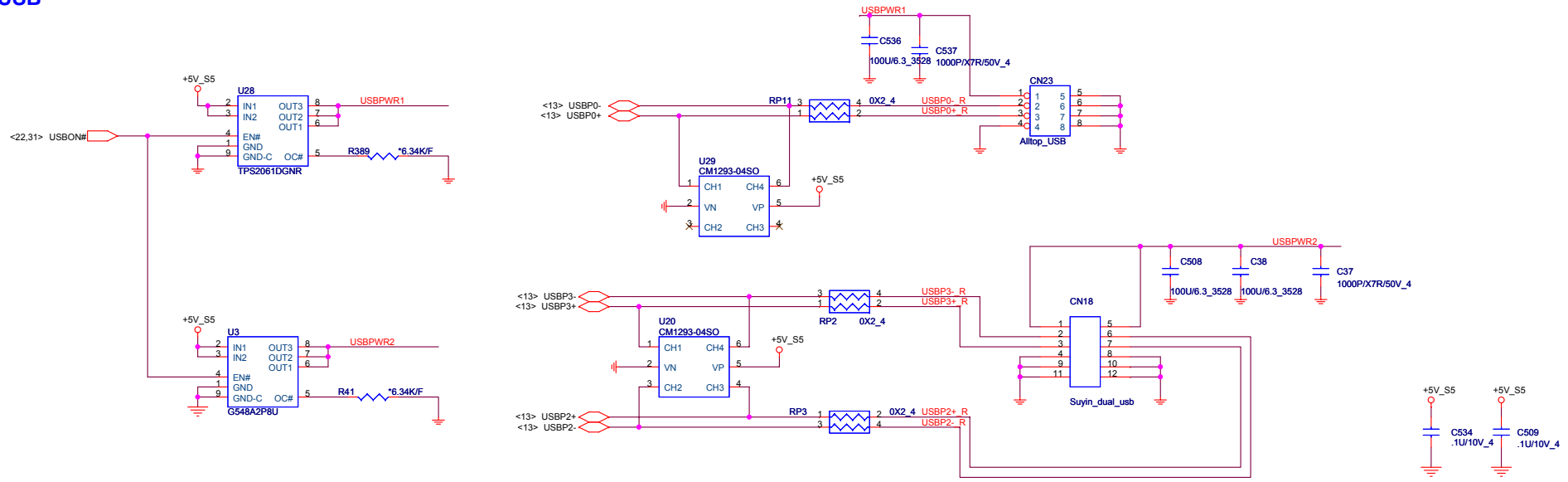
HDMI



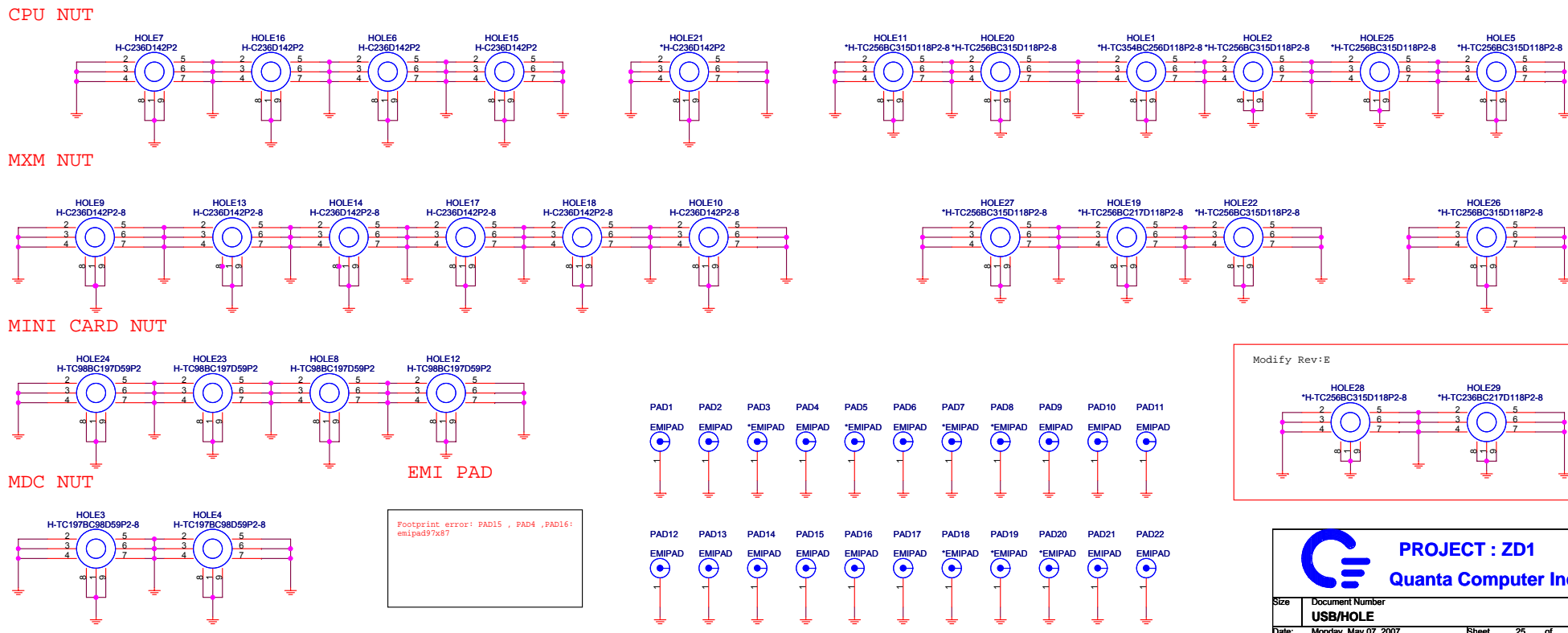
PROJECT : ZD1
Quanta Computer Inc.

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NEW CARD/HDMI/LID
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USB

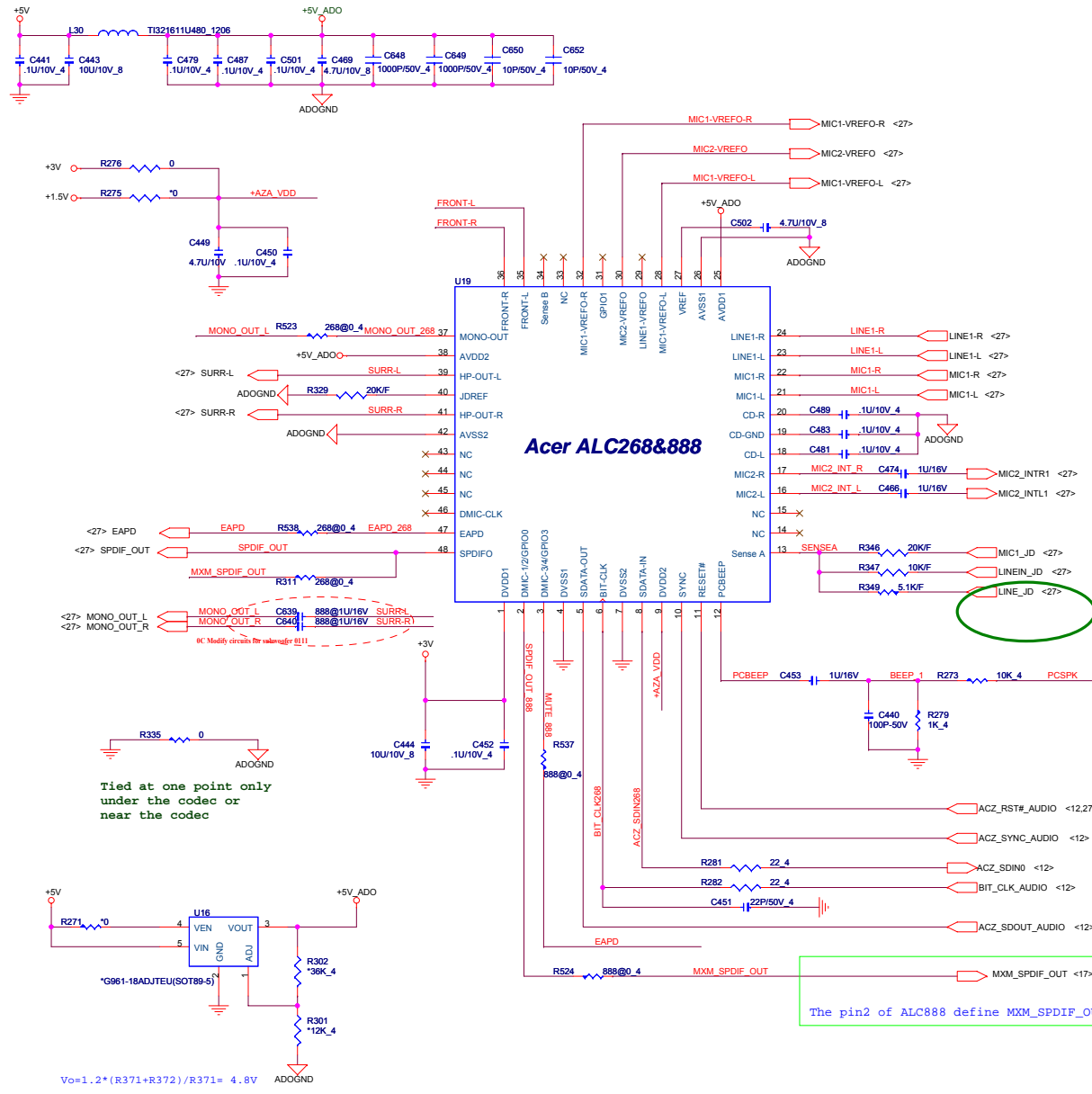


HOLES

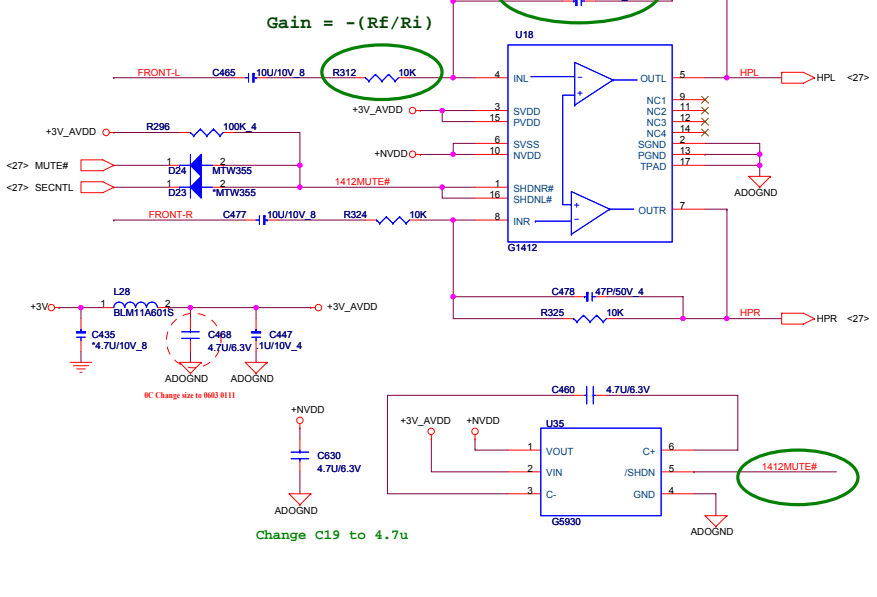


| | | | |
|-----------------------------------|--|---|------------------|
| | | PROJECT : ZD1 Quanta Computer Inc. | |
| | | Size: _____ Document Number: USB/HOLE | Rev: E |
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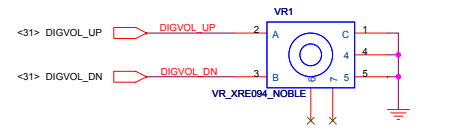
CODEC (ALC268)



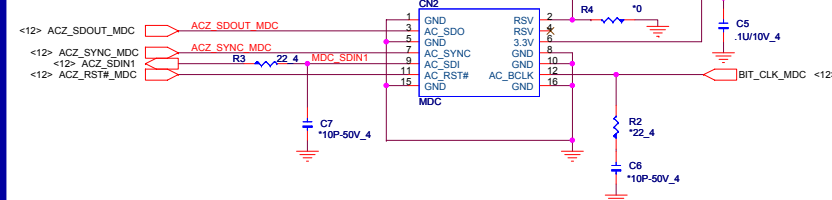
LINE OUT Amplifier



VR

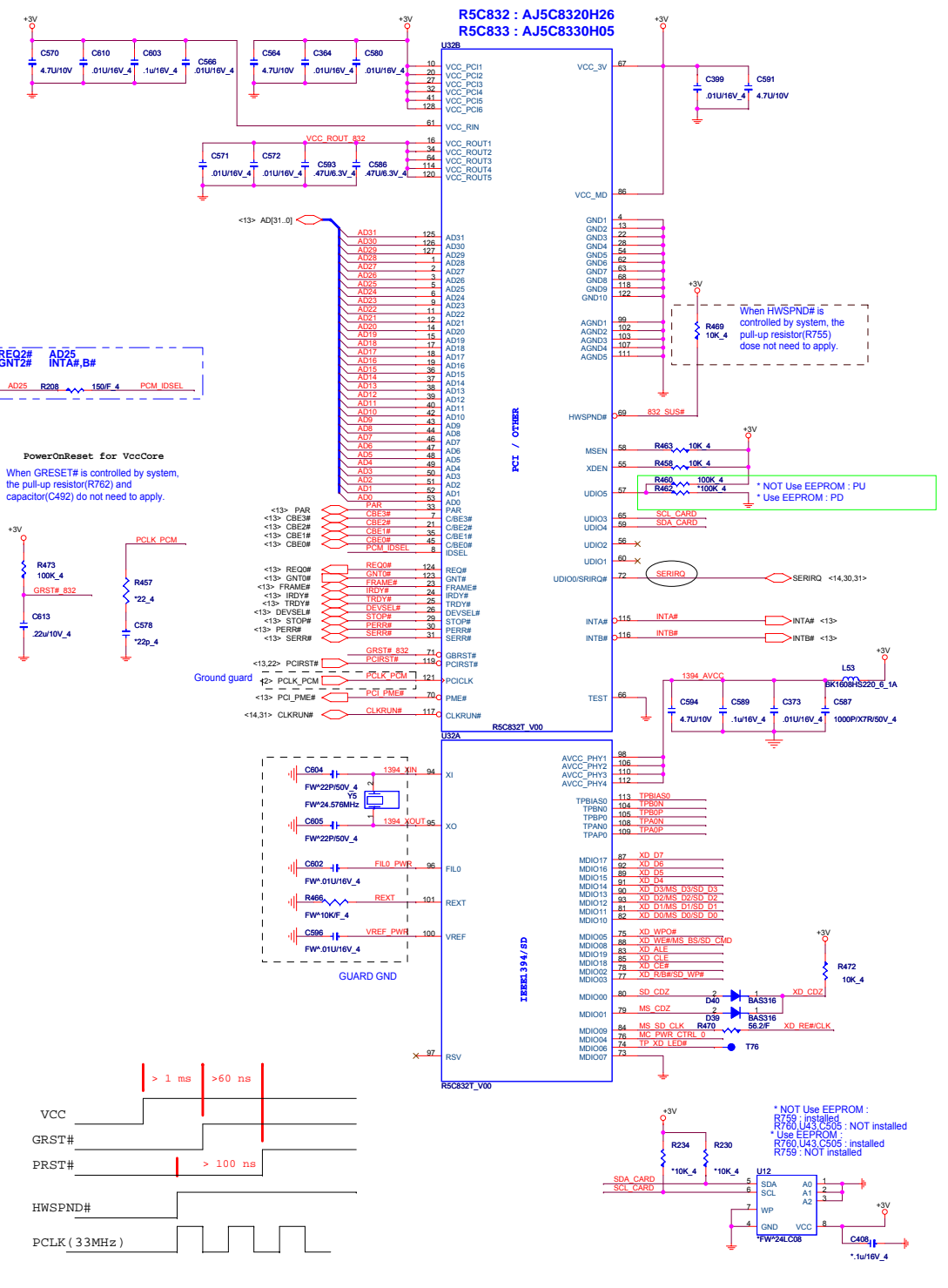


MDC

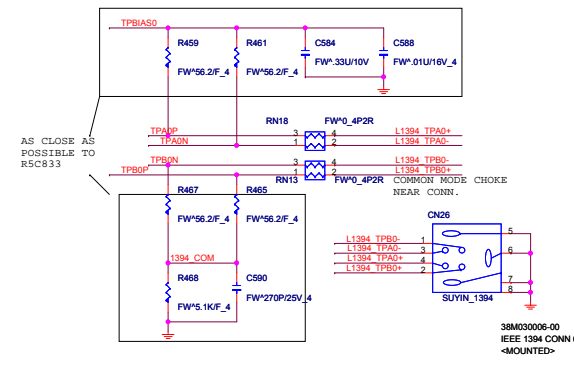


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Quanta Computer Inc.

| | | |
|-------|--------------------------------------|----------------|
| Size | Document Number | Rev |
| | REALTEK ALC268&888/MDC/VR | E |
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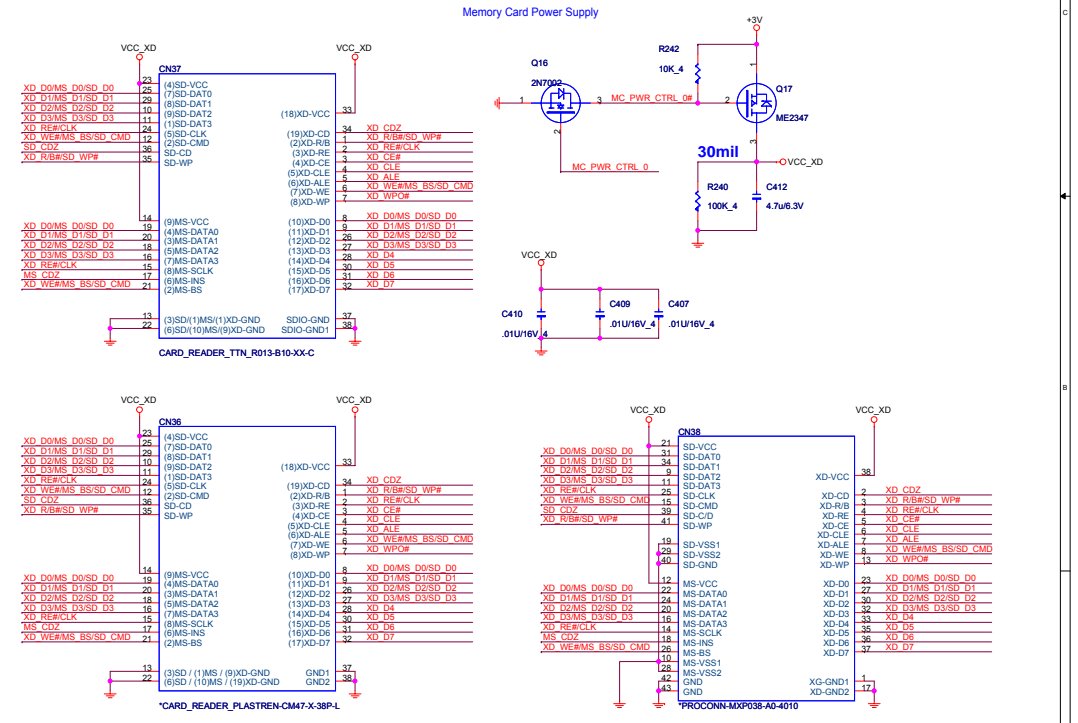


1394

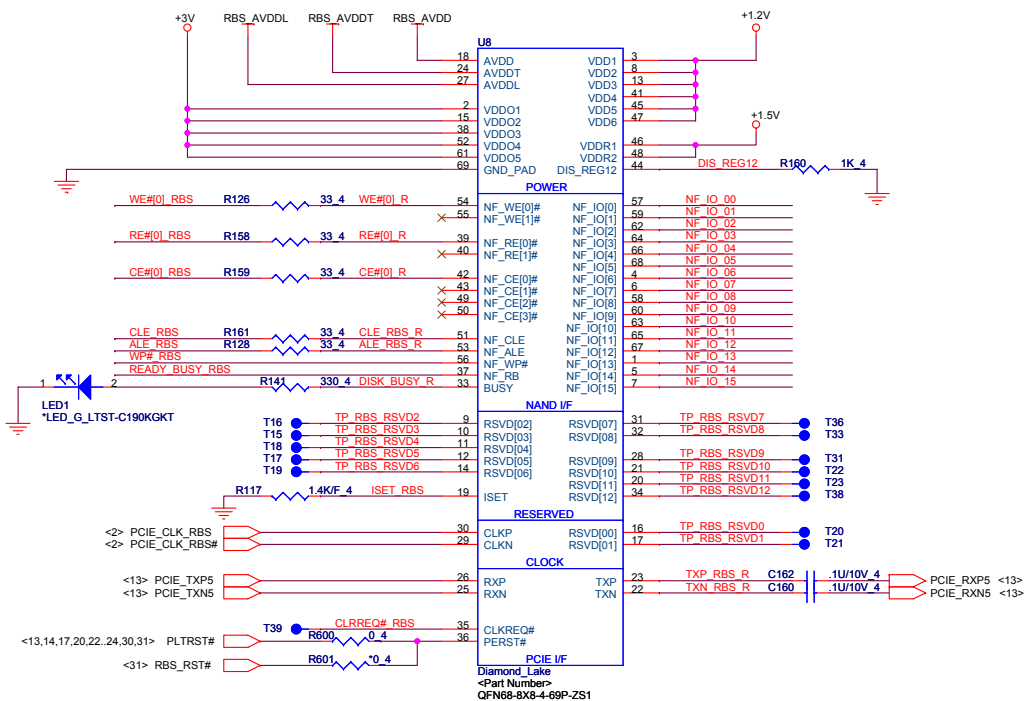


38M30006-00
IEEE 1394 CONN FOLE R/A 78756-1 DIP AMP
<MOUNTED>

5 IN 1 CARD READER



DIAMOND-LAKE ASIC

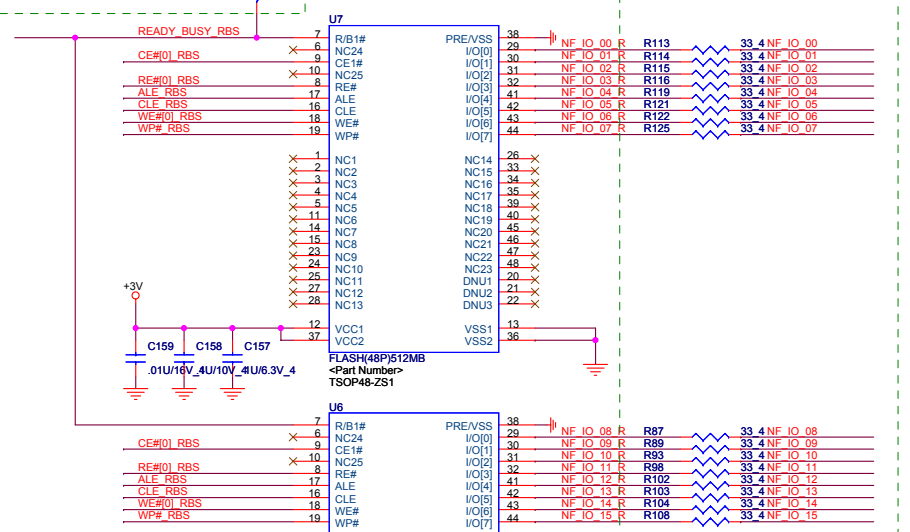


PLACE CLOSE TO NAND FLASH

INTEL NAND FLASH

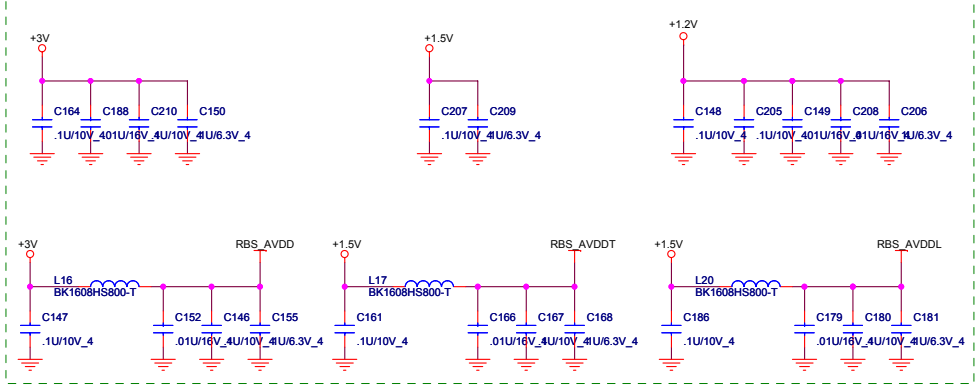
R120 1K_4

PLACEMENT NOTE:
PLACE TERMINATION RESISTORS
AT 10% TO 25% DISTANCE FROM
NAND FLASH.



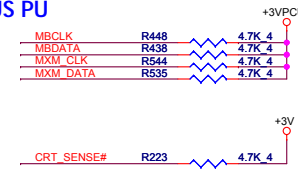
PLACE AS CLOSE AS POSSIBLE TO
DIAMOND-LAKE ASIC.

STUFF: INDICATES A 2KB VIRTUAL PAGE => 256MB
DESTUFF: INDICATES A 4KB VIRTUAL PAGE => 512MB & 1024MB



LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH
NEEDS TO HAVE A SOLDERMASK ON IT.

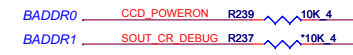
SM BUS PU



I/O ADDRESS SETTING

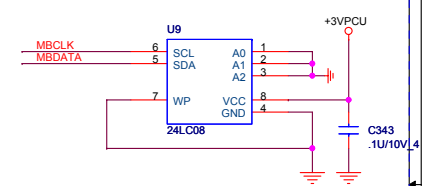
| I/O Address | |
|-------------|--------------------|
| BADDR1-0 | Data |
| 0 0 | XOR TREE TEST MODE |
| 0 1 | CORE DEFINED |
| 1 0 | 2Eh 2Fh |
| 1 1 | 164Eh 164Fh |

SHBM=0: Enable shared memory with host BIOS

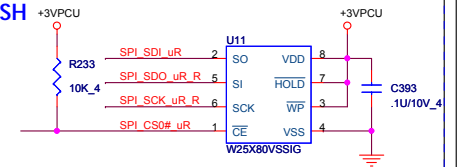


1/13 Confirm by vendor mail :
Disabled (*) if using FWH device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware

ACER ID

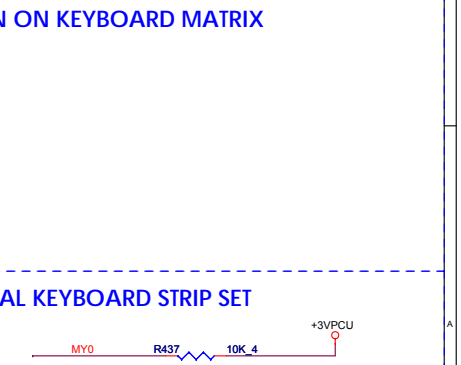


SPI FLASH

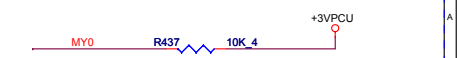


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

BUTTON ON KEYBOARD MATRIX



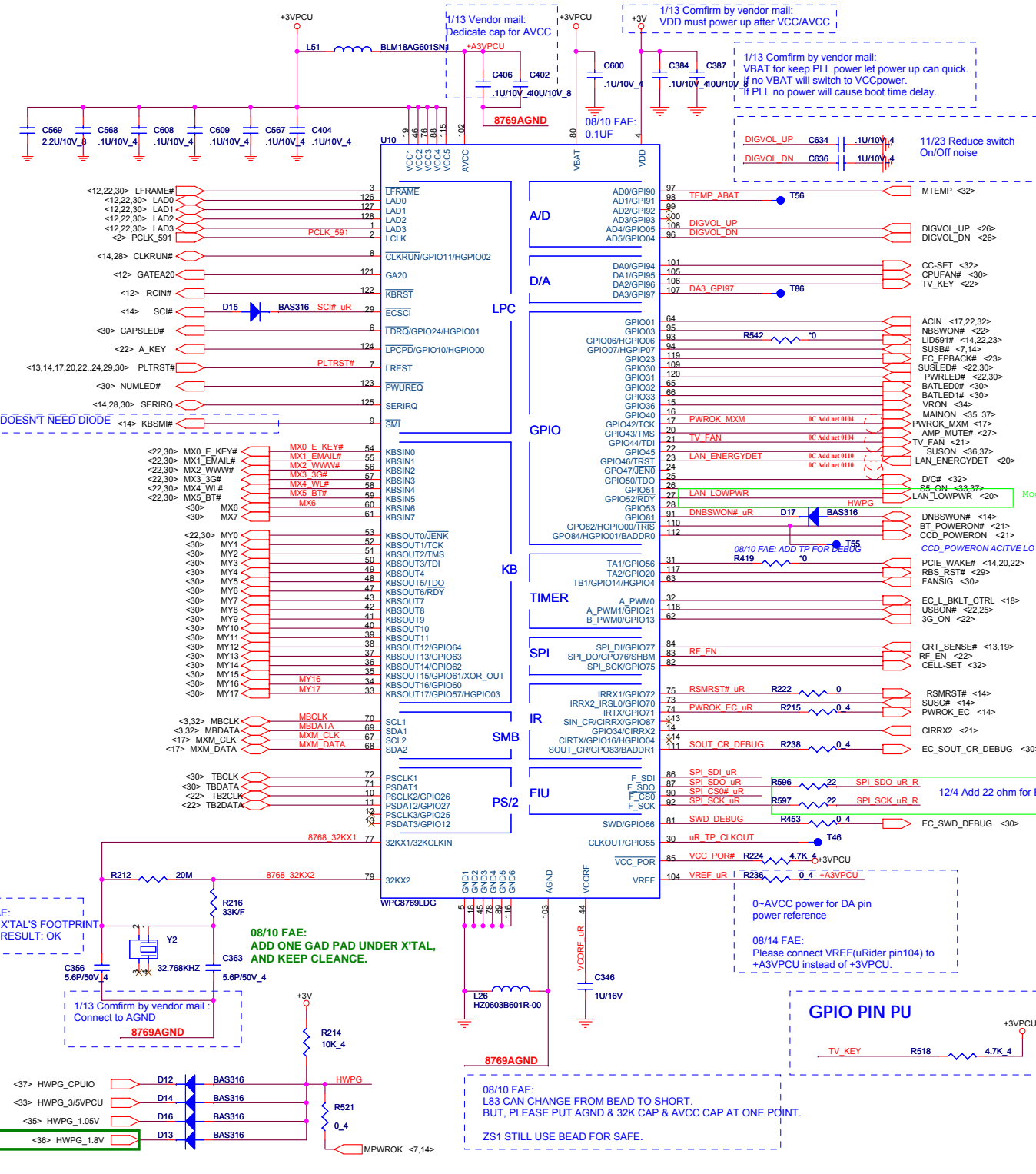
INTERNAL KEYBOARD STRIP SET



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Quanta Computer Inc.

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|-----------------|----------------------|----------------|
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| PC8769L & FLASH | | Sheet 31 of 38 |



08/10 FAE: SMI DOESN'T NEED DIODE

0810 FAE: CHECK XTAL'S FOOTPRINT
CEECK RESULT: OK

08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANSE.

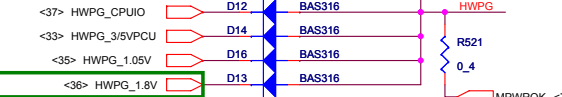
0-AVCC power for DA pin
power reference

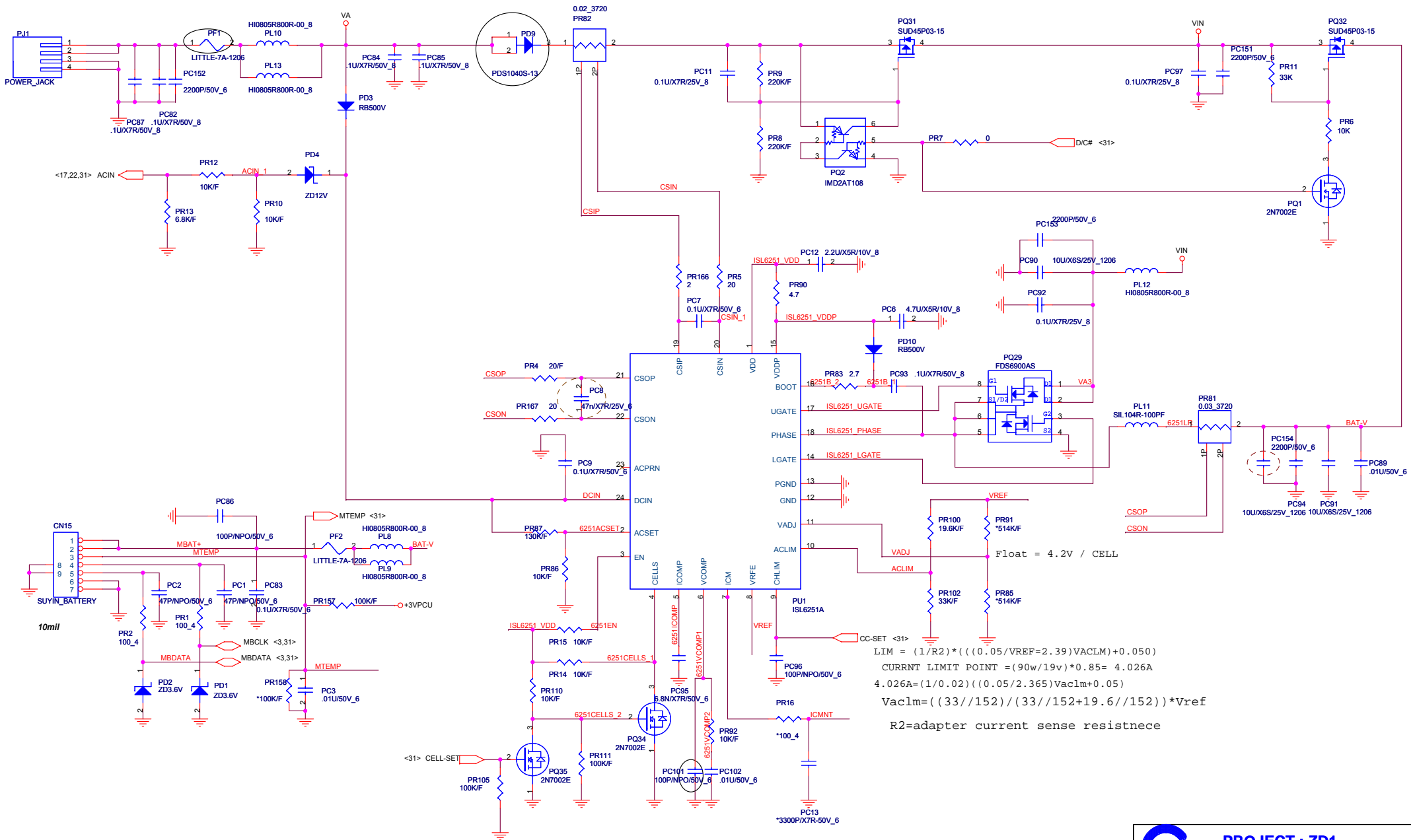
08/14 FAE:
Please connect VREF(uRider pin104) to
+A3VPCU instead of +3VPCU.

08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.

ZS1 STILL USE BEAD FOR SAFE.

GPIO PIN PU





$$LIM = (1/R2) * (((0.05/VREF=2.39) * VACLIM) + 0.050)$$

$$CURRENT\ LIMIT\ POINT = (90w/19v) * 0.85 = 4.026A$$

$$4.026A = (1/0.02) * ((0.05/2.365) * VACLIM + 0.05)$$

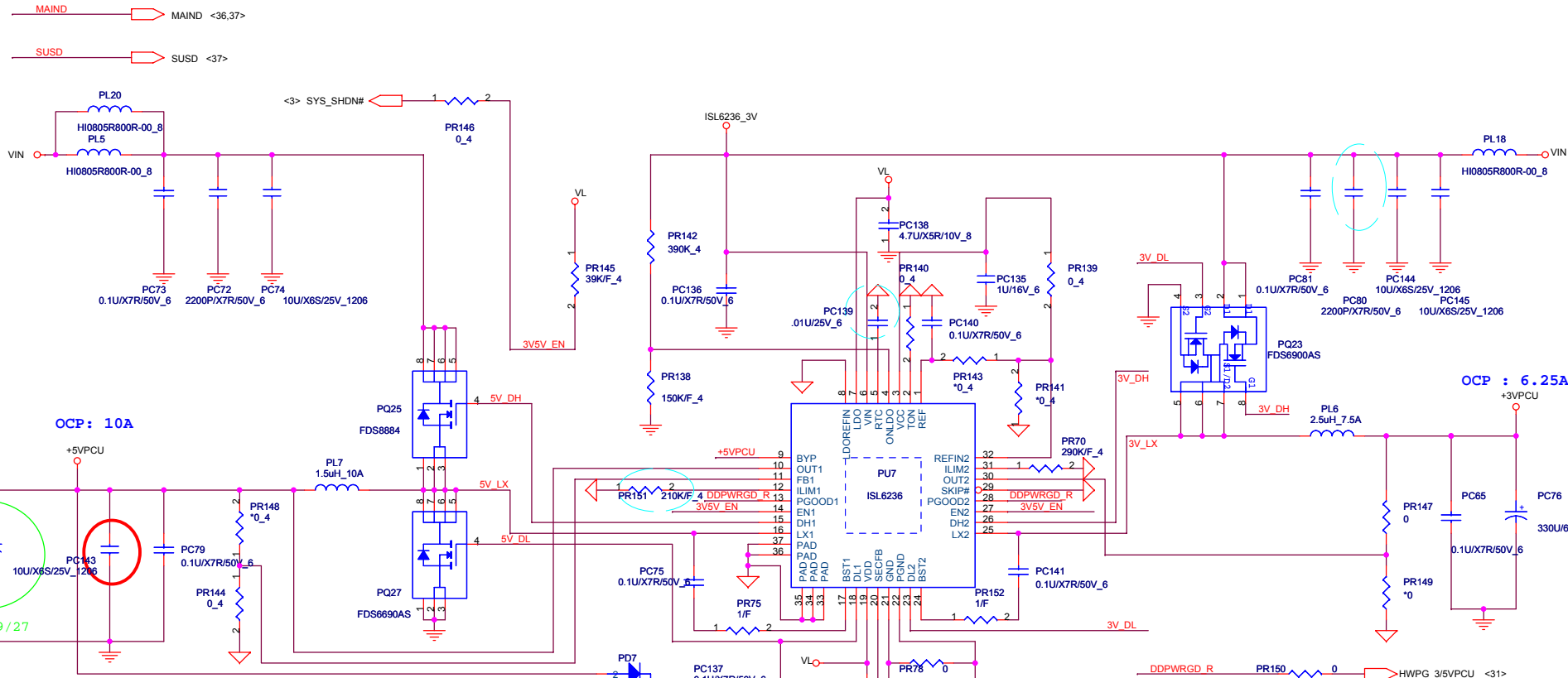
$$VACLIM = ((33//152) / ((33//152) + 19.6//152)) * VREF$$

R2=adapter current sense resistnece

CELL-SET = Hi -----> Cells = VDD ----->4S
 CELL-SET = Low -----> Cells = GND ----->3S

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OCP: 10A

OCP: 10A

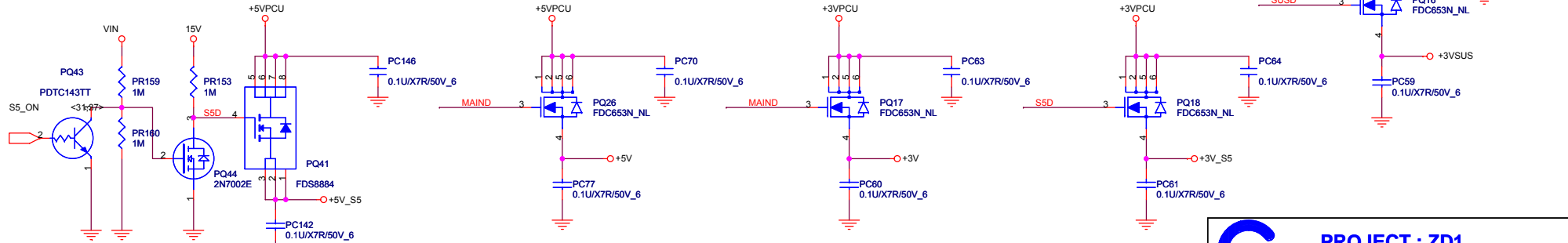
$\Delta IL(\text{ripple current}) = (V_{in} - V_{out}) * V_{out} / (L * f * V_{in})$
 $= (19 - 5) * 5 / (1.5 \mu * 0.4 \text{M} * 19)$
 $\sim 6\text{A}$

$I_{ocp} = OCP - (\Delta IL / 2) = 10 - (6 / 2) = 7\text{A}$
 $V_{th} = 7\text{A} * 15\text{m}\Omega = 105\text{mV}$
 $R(I_{lim}) = (105\text{mV} * 10) / 5\mu\text{A}$
 $\sim 210\text{K}$

OCP: 6.25A

$L(\text{ripple current}) = (19 - 3.3) * 3.3 / (2.5 \mu * 0.5 \text{M} * 19)$
 $\sim 2.18\text{A}$

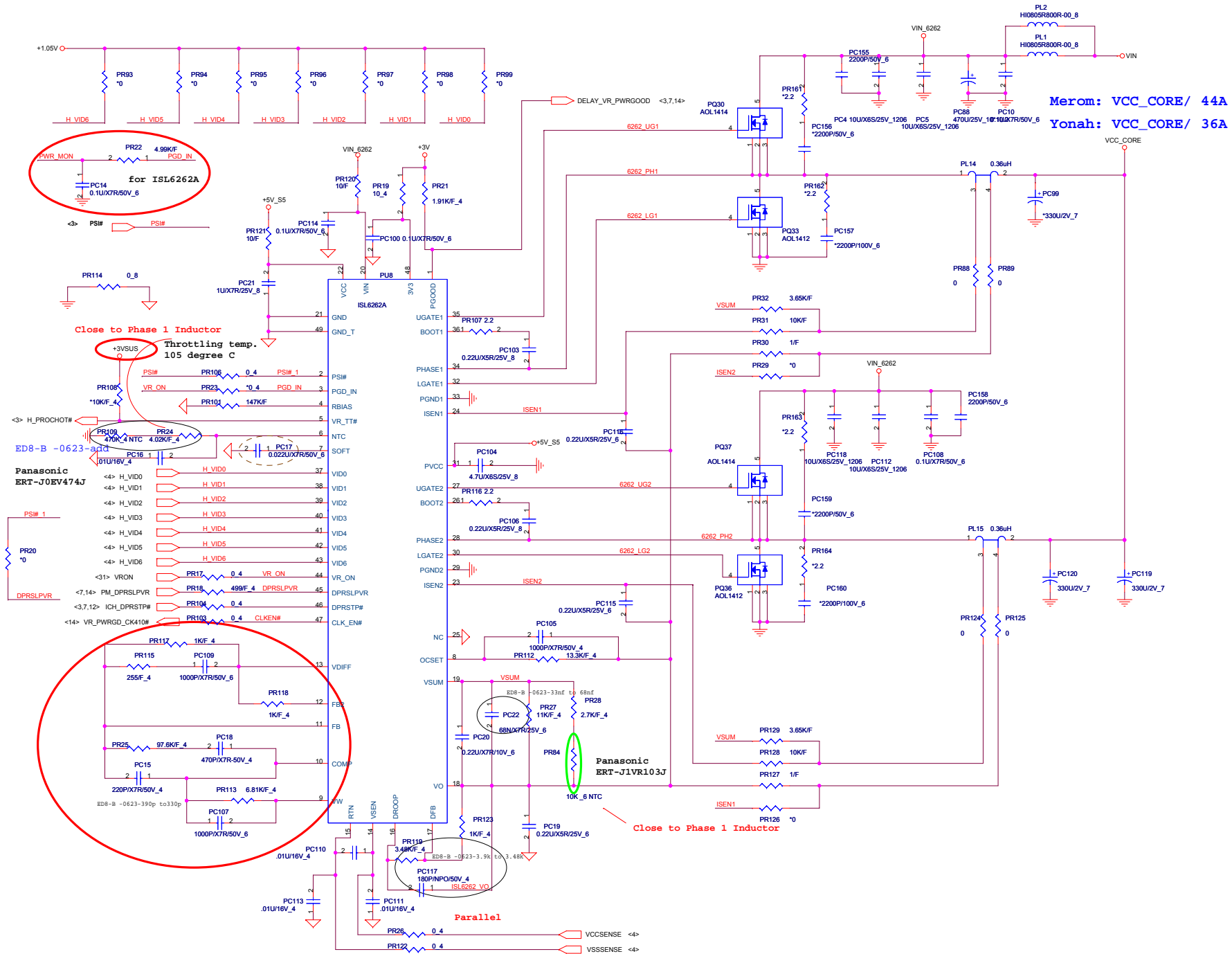
$I_{ocp} = 6.25 - (2.18 / 2) = 5.16\text{A}$
 $V_{th} = 5.16\text{A} * 28\text{m}\Omega = 145\text{mV}$
 $R(I_{lim}) = (145\text{mV} * 10) / 5\mu\text{A}$
 $\sim 294\text{K}$

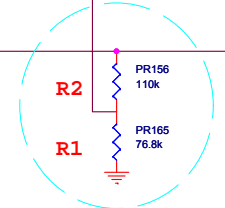
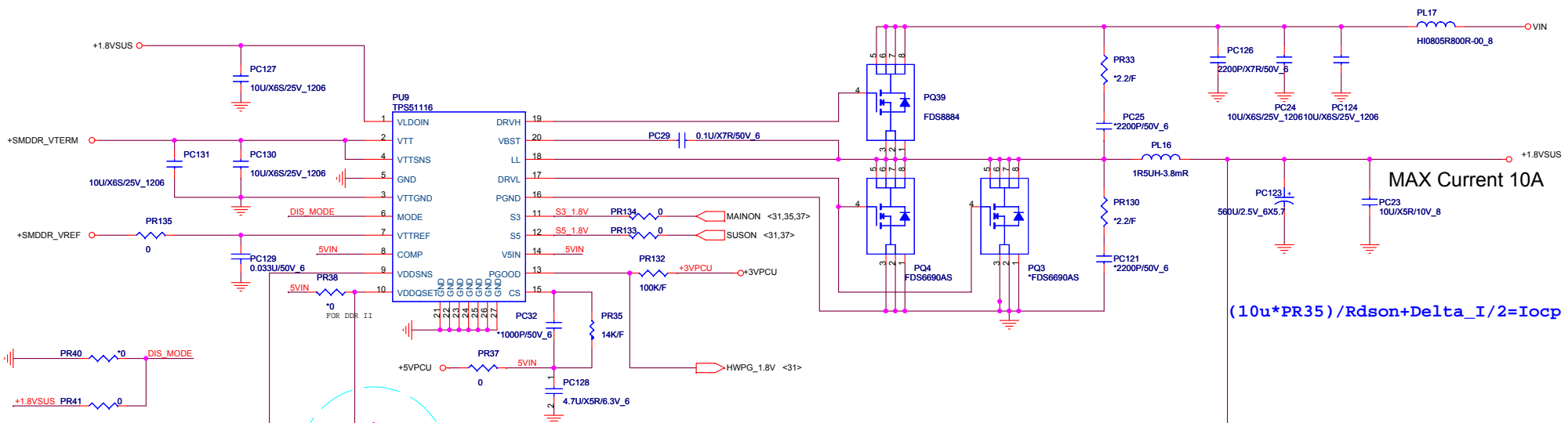


modify 0103 2007

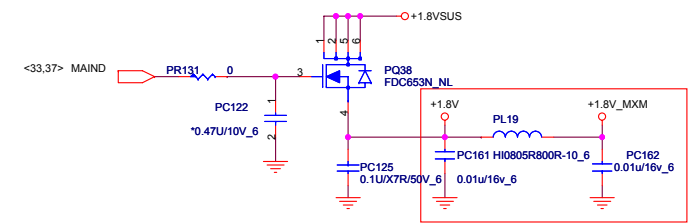
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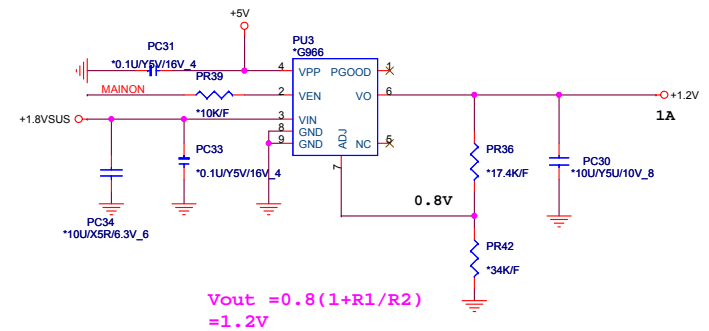
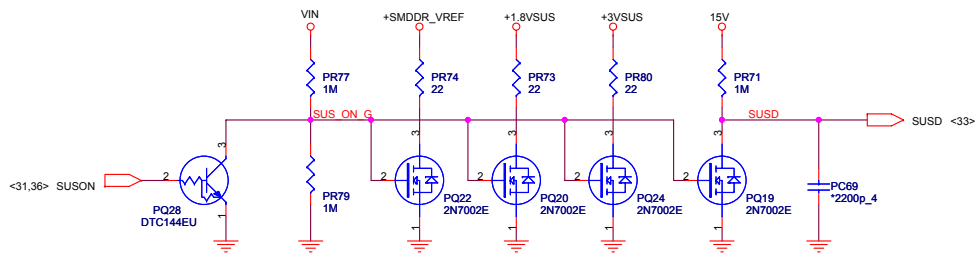
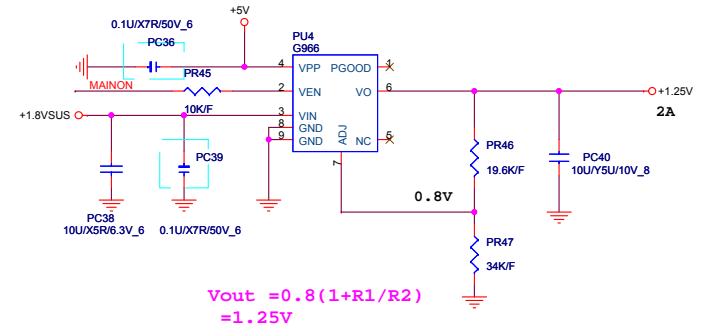
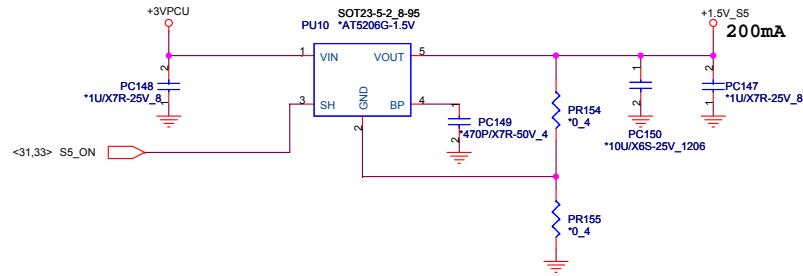
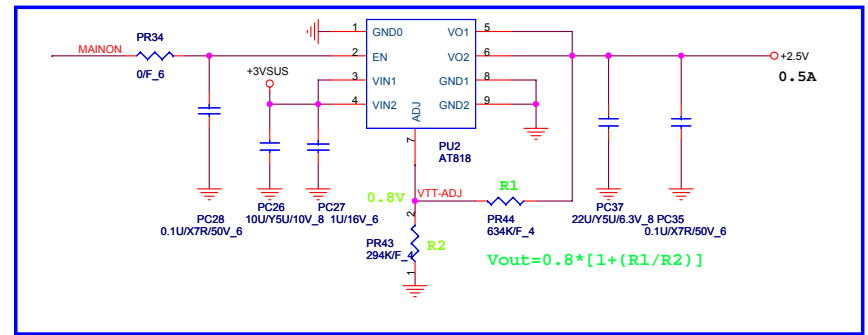
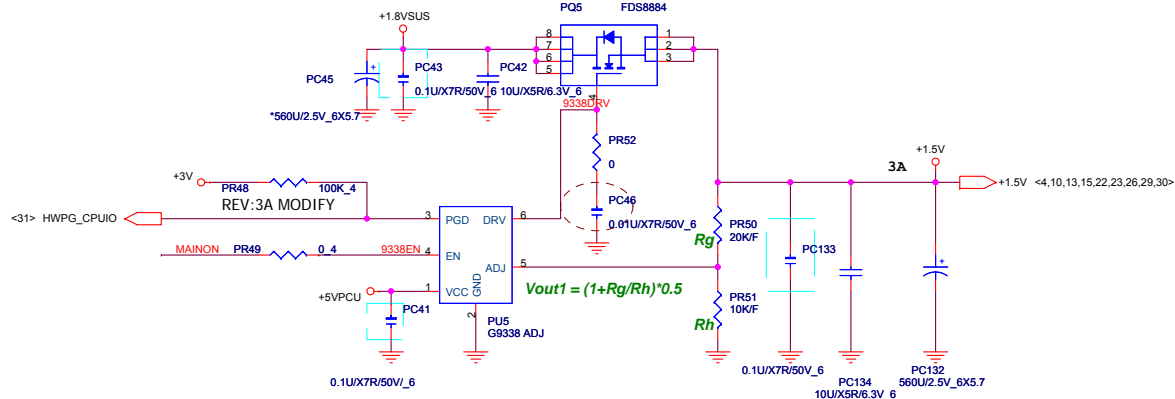




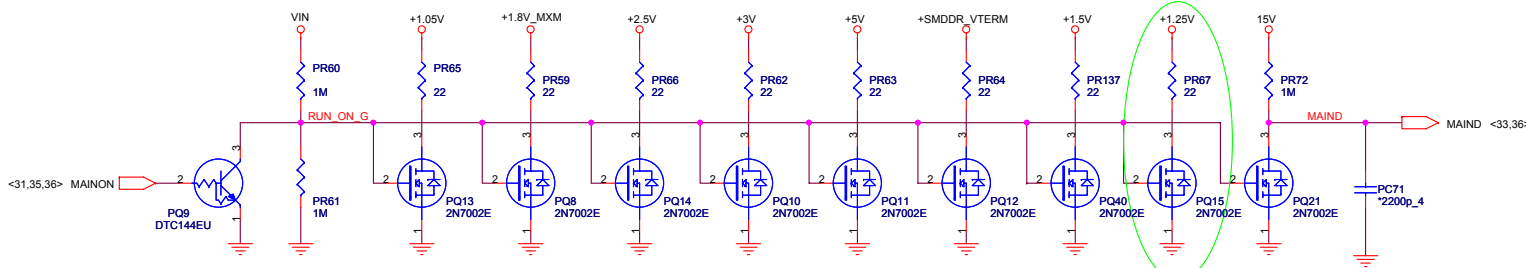
$R1 = (100 * V_{out} - R2) / K$
 if tune V_{out} PR38 un-mount, PR156 PR165 mount




MAX Current 3.5A
 PC161 ,PL19 & PC162 near CN27



Add by power on 10/19



| Model | REV | CHANGE LIST | MODEL | ZY3 | |
|--------|---|---|-------|------|----|
| | | | | FROM | To |
| ZD1 MB | 1A | FIRST RELEASED: E200610-3793 (PCB: DA0ZD1MB6A0) | X | 1A | |
| | 2A | <p>Page10 : Depop R153 & pop L23 for system can not boot</p> <p>Page14 : U36 package didn't math footprint, change P/N.</p> <p>Page26 : Remove R275, install R276; remove R4, install R16; Change R245, R247 power source from +1.5V_S5/+1.5V to +3V_S5/+3V , Follow customer request modem change support to +3VSUS.</p> <p>Page22 : MMB(CN8) PIN define error.</p> <p>Page22 : TV card change support to +1.5V.</p> <p>Page18 : Install R5, depop R7,: Follow customer request use EC to control backlight ON/OFF function.</p> <p>Page14 : GPIO10: Reserve PU, 10K +> It is GPO and OD; GPIO14: Reserve PD, 10K => It is GPI as AC present and active high;</p> <p>Page6 : TV_DCONSEL[0:1], UMA =>NC, External VGA tie to GND.</p> <p>Page31 : 2nd FAN change design</p> <p>Page23 : New card power SW (location: U33) change same as Z01</p> <p>Page31 : add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins</p> <p>Page26 : Co-layout ALC268 and 888S</p> <p>Page28 : SD card can not be detected , U32(ES2) sample will fix this issue.</p> <p>Page28 : MMC card can not be detected , U32(ES2) sample will fix this issue.</p> <p>Page14 : The CLPWROK pin of ICH8 connect with HWFG signal</p> <p>Page22 : change CN7 pin definition for T/P no function.</p> <p>Page24 : change CN8 pin definition MMB no function.</p> <p>Page14 : The signal of KBSMI#_ICH add diode , and it PU to +3V_S5 The signal of LID591#_ICH add diode , and it PU to +3V_S5 for ICH8 electric leakage issue.</p> <p>Page26 : Change subwoofer from 4pin to 5pin connector.</p> | X | 1A | |
| | | | 1A | 2A | |
| | | | 1A | 2A | |
| | | | 1A | 2A | |
| | | | 1A | 2A | |
| | | | 1A | 2A | |
| | | | 1A | 2A | |
| | | | 1A | 2A | |
| | | | 1A | 2A | |
| 1A | | | 2A | | |
| 2B | <p>Page 2 : Add C645 for EMI solution</p> <p>Page31 : Follow customer request 2nd FAN is controlled by EC</p> <p>Page19 : Floating CN13.16 & CN13.17 ,CN14.15 & CN14.16 for ESD test</p> <p>Page07 : DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK and DPLL_REF_SSCLK#. To GND</p> <p>Page36 : Add PI filter to reduce the power ripple of +1.8V.</p> <p>Page16 : Modify SMBus address A2 , The signal of B_SAL need to PU and B_SA0 need to PD</p> <p>Page26 : add 2 capacity 1uF(C639,C640) for subwoofer</p> <p>Page30 : add capacity 2.2uF(C638)</p> | 1A | 2A | | |
| | | 1A | 2A | | |
| | | 1A | 2A | | |
| | | 1A | 2A | | |
| | | 1A | 2A | | |
| | | 1A | 2A | | |
| | | 2A | 2B | | |
| | | 2A | 2B | | |
| | | 2A | 2B | | |
| | | 2A | 2B | | |
| 2C | <p>Page17 : Adding (Q52 & R541 & Q53) extra circuitry to prevent power leakage from system into MXM</p> <p>Page21 : Change power of CIR from +3VPCU and +5VPCU.</p> <p>Page31 : AEC pin24 is multi function pin, when EC power up, pin17 will change to JTAG/TCK function not GPIO. So,need to change from pin24 (GPIO47) to pin27 (GPIO52).</p> <p>Page22: Power/B connector add two LED control signal and change to 16 pin from 14-pin for meet ACER LED spec .</p> <p>Page22: Q35 change to AO3413 form DTAL14 for increase LED driving power.</p> <p>Page23: BL_ON pull up resistor from 10kohm to 100Kohm(R194).+3V pull up will cause power on leakage on BL_ON signal due to our VGA have 10kohm pull low.</p> | 2A | 2B | | |
| | | 2A | 2B | | |
| | | 2A | 2B | | |
| | | 2B | 3A | | |
| | | 2B | 3A | | |
| | | 2B | 3A | | |
| | | 2B | 3A | | |
| | | 2B | 3A | | |
| | | 2B | 3A | | |
| | | 2B | 3A | | |
| 2D | <p>Page19 : Connect CRT of CN13.16 & 17 to GND for ESD</p> <p>Page17 : Add capacity 330uF(C647) & Remove R541</p> <p>Page22 & 25: Combine USB/B (CN17) and TV/B(CN30) connector, Connector change to 16 pin. and +5_S5 from 1pin to 2pin.</p> <p>Page25 : Connect HOLE 28 & 29 to GND for ESD</p> <p>Page32-37 : Update power circuit</p> <p>Page37 : Remove 1.2V circuit</p> <p>Page26 : Add 1000pF and 10pF total 4 PCS Location: C648 , C649, C650, C652 (between +5V_ADOand AGND).</p> <p>Page22 : CN8.8 remove +5V & R540 & connect to +3V (K)</p> <p>Page27 : Modify and ADD. AGND bridge (R337,R284,C459 and C472 = 0 Ohm).</p> <p>Page34 : Remove PR16L, PR163, PC156, PC159</p> <p>Page22 : Add D45~D51 for ESD</p> <p>Page28 : Change CN36.37 & 38 ,CN37.37 & 38 ,CN38.42 & 43 from ADOGND and GND.</p> | | | | |
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| | | | | | |
| | | | | | |
| 3A | <p>Page32 : PD9 Change footprint</p> <p>Page25 : Add EMI Spring</p> <p>Page27 : Add GND & AGND bridge (R546,R540,R408)</p> <p>Page22 : Modify pin define (TV/B(CN30) connector)</p> | | | | |
| | | | | | |
| F | <p>Page23 & 17 : HDMI circuits modify: Add level-shifter for MXM_HDMI_DDCCLK and MXM_HDMI_DDCDATA.(Location: Q54 ,Q55 , R75, R63, R297, R410 & R602) .</p> | | | | |

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|---------|-----------------|-----|--------------|-----------|------------|
| DOC NO. | PROJECT MODEL : | ZD1 | APPROVED BY: | DATE: | 2007/ 2/15 |
| | PART NUMBER: | | DRAWING BY: | REVISION: | 3A |