Garda-5 Block Diagram

Project code: 91.4Q201.001
PCB P/N : 55.4Q201.XXX
REVISION : 06206-SA
(Hannstar, GCE)

-1-0426

CLK GEN.
ICS951413
(RTM865T-300/CY28RS400) 3

Mobile CPU
Yonah 478
4, 5

G792
20

AGTL+ 133/166MHz

ATI RC410ME
AGTL+ CPU I/F
SINGAL DDR2 CHANNEL
INTEGRATED GRAPHICS
LVDS/TVOUT/CRT
1 X4 PCIE SB I/F
6 X1 PCIE GPP I/F
Ver.:A13, 71.RC410.D0U
6,7,8,9,10

DDR2 x 2
11,12
533/667MHz

SVIDEO/COMP → TVOUT 14
LVDS → 14"WXGA+ LCD 13
RGB CRT → CRT 14
PCIE x 1 → Mini Card*1 802.11A/B/G 27
PCIE x 1 → New card 32
PWR SW TPS2231 32

A-Link Express X4

ATI SB460
USB2.0 8Ports
SATA II (4 PORTS)
AZALIA HD AUDIO 1.0
AC97 2.3
ATA 66/100/133
LPC I/F
ACPI 1.2
INT RTC
PCI/PCI BDGE
Lab Ver. :A11, 71.SB460.A0U
Eng Ver. :A12, 71.SB460.B0U
15,16,17,18,19

Line In 31
MIC In 31
Codec ALC883 30
AZALIA
INT.MIC
INT.SPKR 31
OP AMP G1432Q 31
Line Out (SPDIF) 31
MAX4411
RJ11
MODEM MDC Card 22

PCI BUS
CARDBUS ENE CB1410 25
PCMCIA I/F
PWR SW TPS2211 26
PCMCIA SLOT Support TypeII 26
RICOH R5C832 1394 CardReader 28,29
1394 CONN 29
MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 29
Mini-PCI 802.11A/B/G 32
LAN Reltek10/100 RTL8100CL 23
TXFM 24
RJ45 24

LPC BUS
SIO NS87381 35
KBC ENE 3910 33
BIOS MX29LV800 36
LPC DEBUG CONN. 36
FIR 35
Touch Pad 34
INT. KB 34

SATA
PATA
USB 3 PORT 22
HDD 21
CDROM 21
MINI USB Blue-tooth 22

PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51120 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124RGER 42	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0
APL5312 120mA	
3D3V_S0	1D5V_CPU_S0 43
APL5332 1A	
3D3V_S0	1D5V_NEW_MINI_S0 43
APL5912 3A	
1D2V_S0	1D05V_S0 43
TPS51100 1A	
1D8V_S3	DDR_VREF_S3 DDR_VREF_S0 43
APL5308 300mA	
3D3V_S5	1D8V_S5 43

MAXIM CHARGER MAX8725 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 39,40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 48A

<Variant Name>

Digitally signed by dd
DN: cn=dd, o=dddddddd, email=dddd@yahoo.com, c=US
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BLOCK DIAGRAM
Garda-5
Date: 2009.11.29 17:23:13 +07'00'
Rev: 1
Sheet 1 of 46

USB	
Pair	Device
0	USB1
1	BT
2	USB2
3	NEW C
4	USB3
5	CCD
6	MINIC1
7	NC

PCI_CLK0	PCM
PCI_CLK1	IEEE1394
PCI_CLK2	LAN
PCI_CLK3	MINI
PCI_CLK4	KBC
PCI_CLK5	FWH
PCI_CLK6	SIO
PCI_CLK7	SPDIFOUT

PCI ROUTING TABLE

DEVICE	IDSEL	IRQ(Default)	REQ# / GNT#
MiniPCI	AD22	H	REQ#1/ GNT#1
R5C832	AD20	F : 1394 H : 6 in 1	REQ#3/ GNT#3
LAN(RTL8100CL)	AD17	E	REQ#2/ GNT#2
CARDBUS CB1410	AD16	G	REQ#0 / GNT#0
USB UHCI	AD29	A, B, C, D	
USB 2.0 EHCI	AD29	A	
DMI-to-PCI AC97 Modem AC97 Audio	AD30	B A	REQ#1 / GNT#1
LPC Bridge IDE SATA SMBus	AD31	A B B	
PCI Express	AD28	A, B, C, D	
Azalia Controller	AD27	A	

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

Hist0ry

```
============================================================
2006/04/26 (-1 Modify)
1. page 27, change R8/R226 to 100 ohm due to power/email to dark.
2. page 15, change C286/C287 from 18pf to 15pf due to frequence shift(from -6.7 to 4ppm).
3. page 23, change C295/C294 from 15p to 12p due to frequence shift(from -23.3 to 7.9ppm).
4. EMI Solution for USB/MDC
        a. Change L23, L24, L31, L32 to "69.10084.071".
        b. del R353,R354,R356,R360,R445,R446.
        c. Change L1, L2 to "68.00331.011".
5. Page 44, change C12/C14 to 78.10699.43L due to 78.10699.42L Obsoleted.
============================================================
2006/04/13 (-1 Modify)
1. Page 31, R447/R448 tp 33ohm.
2. Page 45, Add D4:83.P4SSM.0AM.
3. Page 44, Change C321 from 78.10492.4BL to 78.10224.2BL(1000P, 50V, K0603).
4. Page 23, change R209 from 5.6K to 5.37K.
5. Page 24, change XF1 from 68.68161.30A to 68.01201.30A.
6. Page 46, Mini card stand-off(銅柱) need to be changed from 34.4P401.001 to 34.4A907.001.
7. change 84.27002.L04 to 84.27002.F31.
============================================================
2006/04/10 (-1 Modify)
1. Page 8, add "LVDS_DIGON" solution from ATI PA note.
2. Page 31, Add R to GND and serial R for U60 pin13/15.
============================================================
2006/04/03 (SB Modify)
1. Page 40,  Dummy C593.
2. Page 44, Del C32.
3. Page 41, DCBATOUT_51120 change to DCBATOUT (Del G4,G5,G6,G7,G8)
4. Page 4/5, updae CPU symbol.
5. Page 15, Change X5 to same as X1 due to ME high limit issue, Cap. the same as X1 but should fine-tune.
6. Page 39/41/42, change "GAP-CLOSE-PWR" to 0 ohm PAD due to layout concern.
============================================================
2006/03/31 (SB Modify)
1. Page 3, change R139 to bead and C211 to 2.2u for CRT Jitter.
2. Page 6, change R105 from 1.8K to 4.7K.
3. Page 8, change C165 to 2.2u for ATI recommend.
4. Page 8, SIV EDID_CLK/DAT issue, change RN53 to 4.7K.
5. Page 14, SIV RBG fail:
6. Page 15,
        a. PCIRST1#(1394) shoulder: Add 33 ohm @ SB.
        b. PLT_RST1# overshot : change R144 to 33ohm & R141 to 100P.
        c. Add 0ohm for RTC power for ATI recommend.
7. Page 40 , add 10U Cap.
8. Page 13/27, change Green LED4/LED5/LED1 to 83.00190.L70.
        (manual change yellow LED6/LED3/LED8/LED2 to 83.00190.S70).
9. EMI request:
        a. Page 13, USB_PP5,USB_PN5 add COMMON CHOKE.
        b. EC28,EC34,C208 add 0.1µCap.
        c. CLK48_ICH( near CLK GEN.),SB_CLK33_FWH(near R177) add 20p Cap..
============================================================
2006/03/28 (SB Modify)
1. Page 14, change Q15/Q14 to 2N7002 for SIV CRT SMBus bug.
2. Page 15, Change C248/C261/C264/C263/C252 from 78.10491.4FL to 78.10523.5F1,
        and C262 from 78.10693.41L to 78.10623.51L.
3. Page 8, Add "LCDVDD_ON" PL 100K.
4. Page 41, change U7 to AO4406(84.04406.A37).
5. Page 33, KBC GPIO09 for 1394.
6. Page 33, add 1u Cap. for ENE ECRST# spec. 2ms.
7. Page 31, add audio popo noise solution.
8. Page 25, change C520 to 1U for "GBRST#".
9. Page 28, change "GBUS_GRST#_1" timing.
============================================================
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<Variant Name>

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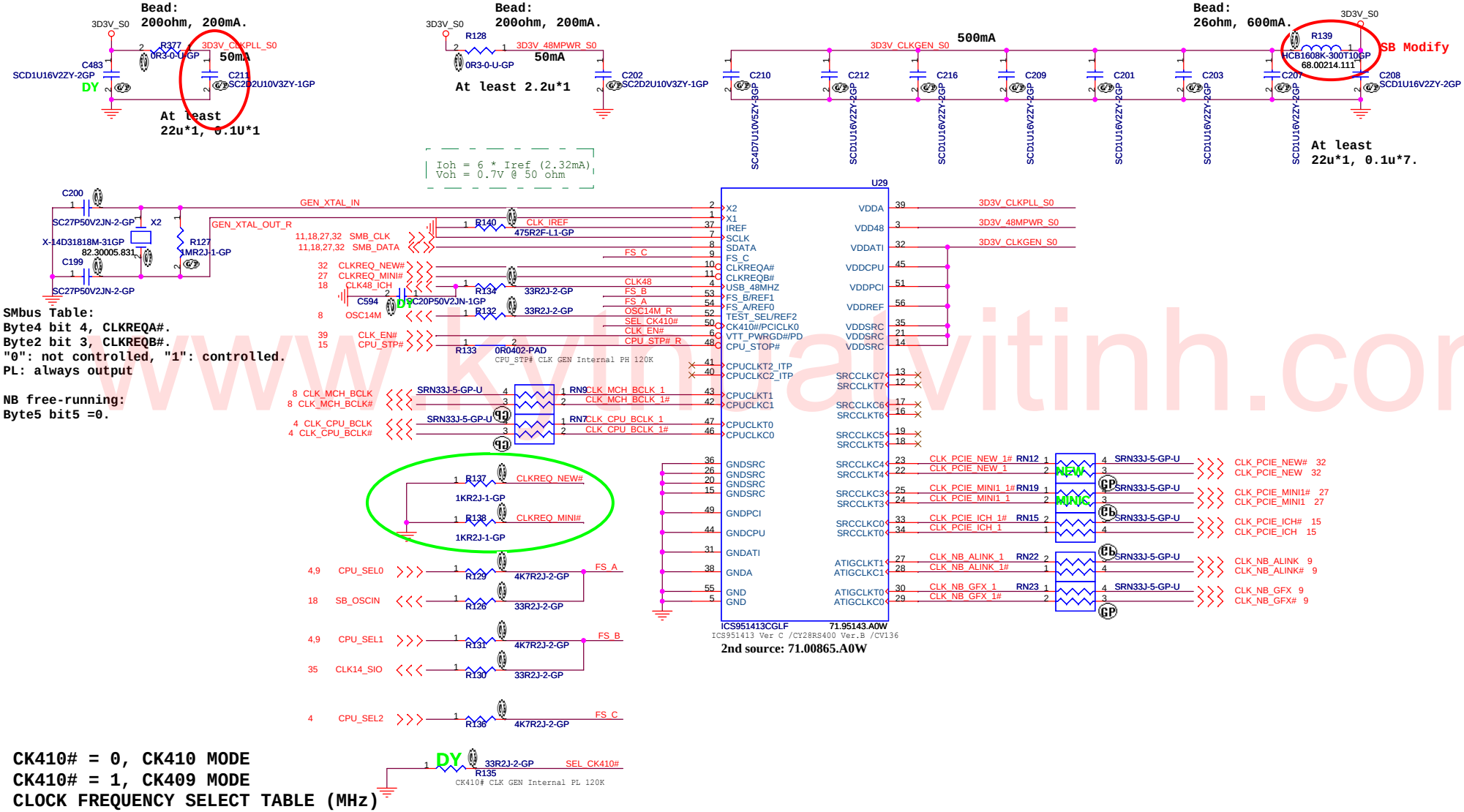
Title: ***Reference***

Size	Document Number	Rev
A3	Garda-5	-1

Date: Wednesday, April 26, 2006 Sheet 2 of 46



FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	RESV	100	33	14.31

<Variant Name>

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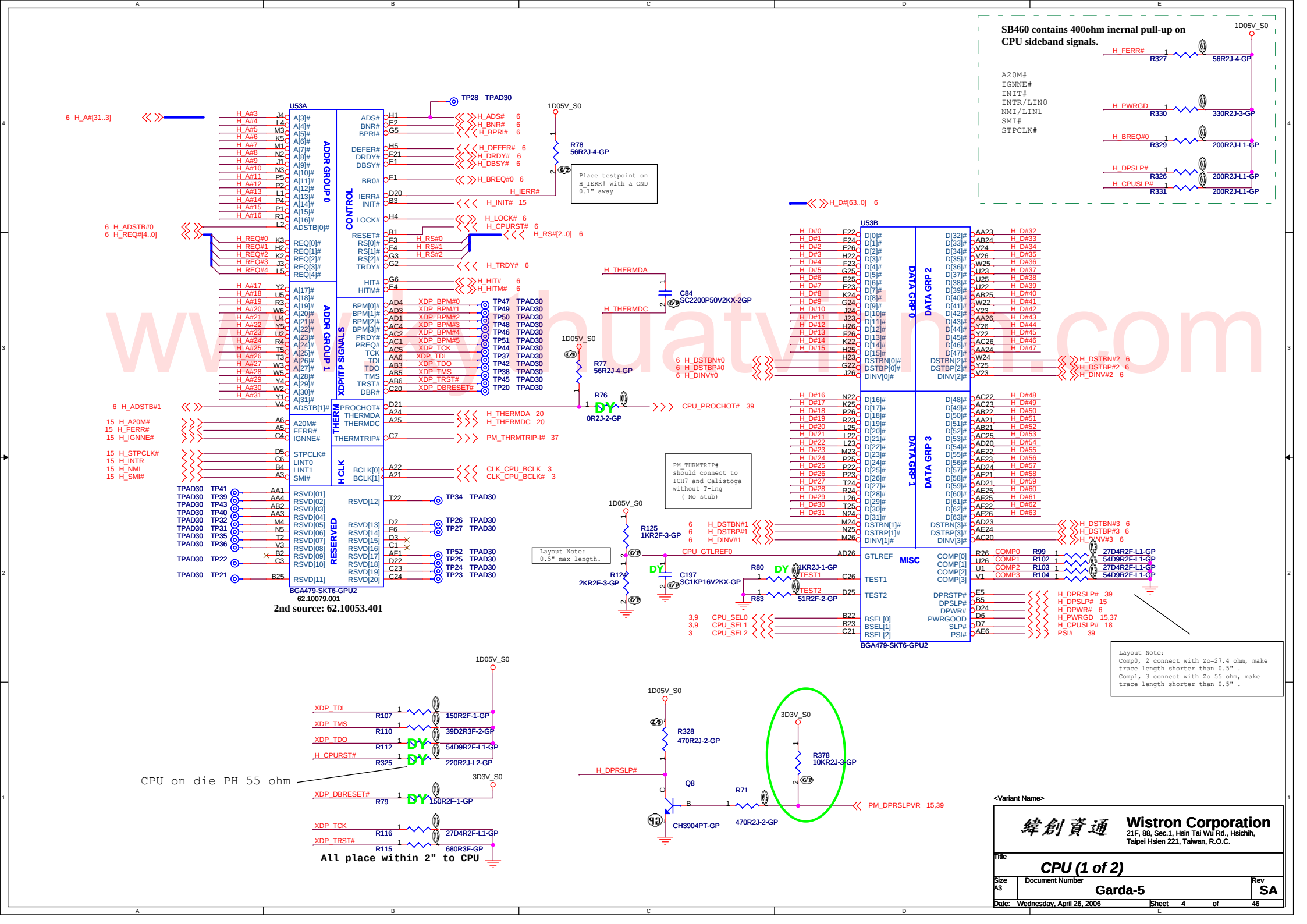
Title: Clock Generator -ICS951413

Size: A3 | Document Number: Garda-5 | Rev: SB

Date: Wednesday, April 26, 2006 | Sheet 3 of 46


SB460 contains 400ohm inernal pull-up on CPU sideband signals.
A20M#
IGNNE#
INIT#
INTR/LIN0
NMI/LIN1
SMI#
STPCLK#
H_FERR# R327 56R2J-4-GP
H_PWRGD R330 330R2J-3-GP
H_BREQ#0 R329 200R2J-L1-GP
H_DPSLP# R326 200R2J-L1-GP
H_CPUSLP# R331 200R2J-L1-GP
1D05V_S0
U53A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
BGA479-SKT6-GPU2
62.10079.001
2nd source: 62.10053.401
U53B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
BGA479-SKT6-GPU2
R78 56R2J-4-GP
R77 56R2J-4-GP
R76 0R2J-2-GP
C84 SC2200P50V2KX-2GP
C197 SC1KP16V2KX-GP
R125 1KR2F-3-GP
R124 2KR2F-3-GP
R80 1KR2J-1-GP
R83 51R2F-2-GP
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)
Layout Note: 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
CPU on die PH 55 ohm
All place within 2" to CPU
R107 150R2F-1-GP
R110 39D2R3F-2-GP
R112 54D9R2F-L1-GP
R325 220R2J-L2-GP
R79 150R2F-1-GP
R116 27D4R2F-L1-GP
R115 680R3F-GP
R328 470R2J-2-GP
R378 10KR2J-3-GP
R71 470R2J-2-GP
Q8 CH3904PT-GP
3D3V_S0
PM_DPRSLPVR 15,39
<Variant Name>
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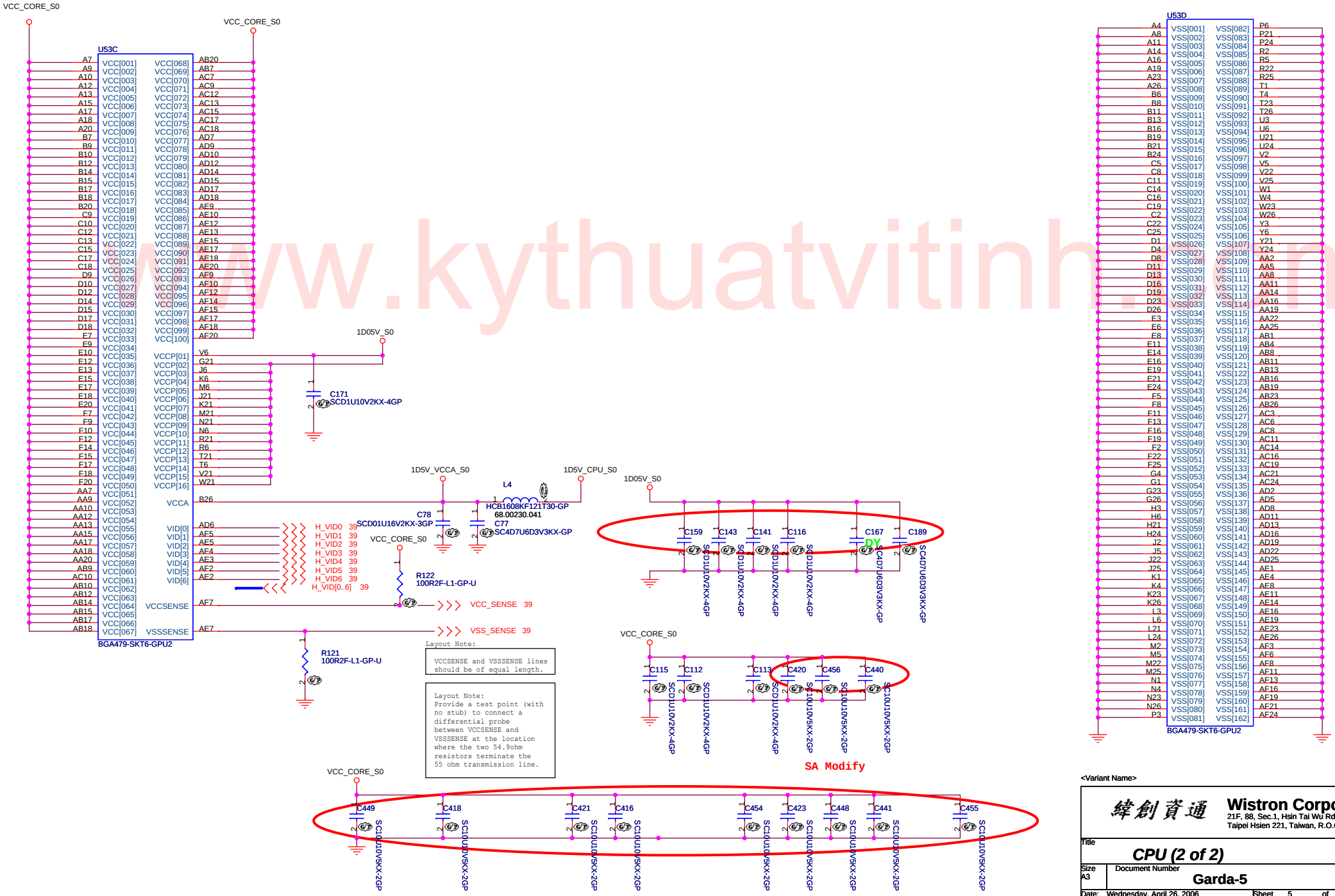
Title
CPU (1 of 2)
Size A3
Document Number Garda-5
Rev SA
Date: Wednesday, April 26, 2006
Sheet 4 of 46


VCC_CORE_S0
U53C
BGA479-SKT6-GPU2
1D05V_S0
C171
SCD1U10V2KX-4GP
1D5V_VCCA_S0
1D5V_CPU_S0
L4
HCB1608KF121T30-GP
68.00230.041
C78
SCD01U16V2KX-3GP
C77
SC4D7U6D3V3KX-GP
H_VID0 39
H_VID1 39
H_VID2 39
H_VID3 39
H_VID4 39
H_VID5 39
H_VID6 39
H_VID[0..6] 39
R122
100R2F-L1-GP-U
VCC_SENSE 39
VSS_SENSE 39
R121
100R2F-L1-GP-U
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
C159
C143
C141
C116
C167
DY
C189
SCD1U10V2KX-4GP
SC4D7U6D3V3KX-GP
C115
C112
C113
C420
C456
C440
SCD1U10V2KX-4GP
SC10U10V5KX-2GP
SA Modify
C449
C418
C421
C416
C454
C423
C448
C441
C455
SC10U10V5KX-2GP
U53D
BGA479-SKT6-GPU2
<Variant Name>
緯創資通
Wistron Corporation
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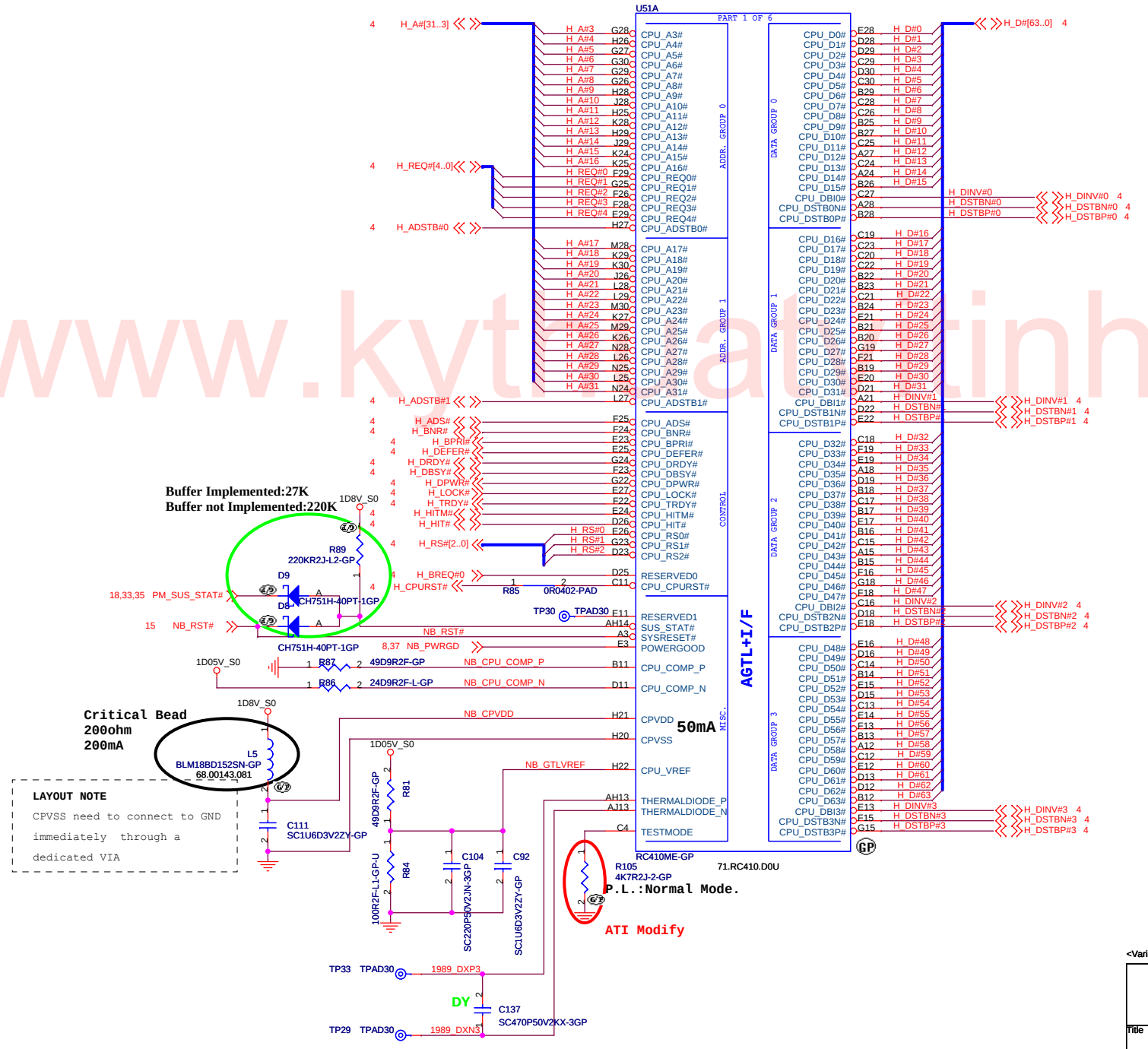
Title
CPU (2 of 2)
Size A3
Document Number
Garda-5
Rev SA
Date: Wednesday, April 26, 2006
Sheet 5 of 46



<Variant Name>

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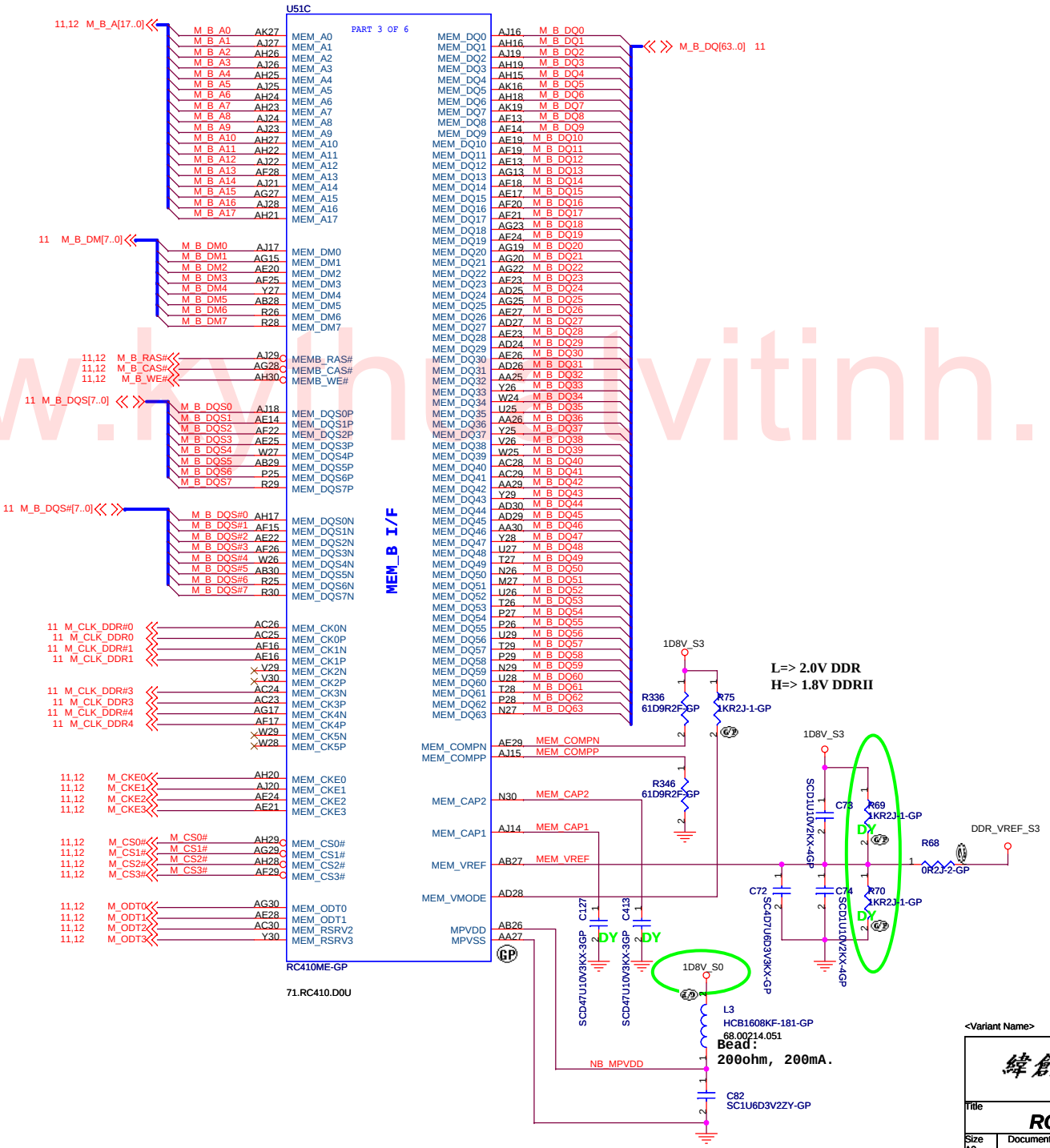
Title: RC410ME (1 of 5) Host I/F

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 6 of 46



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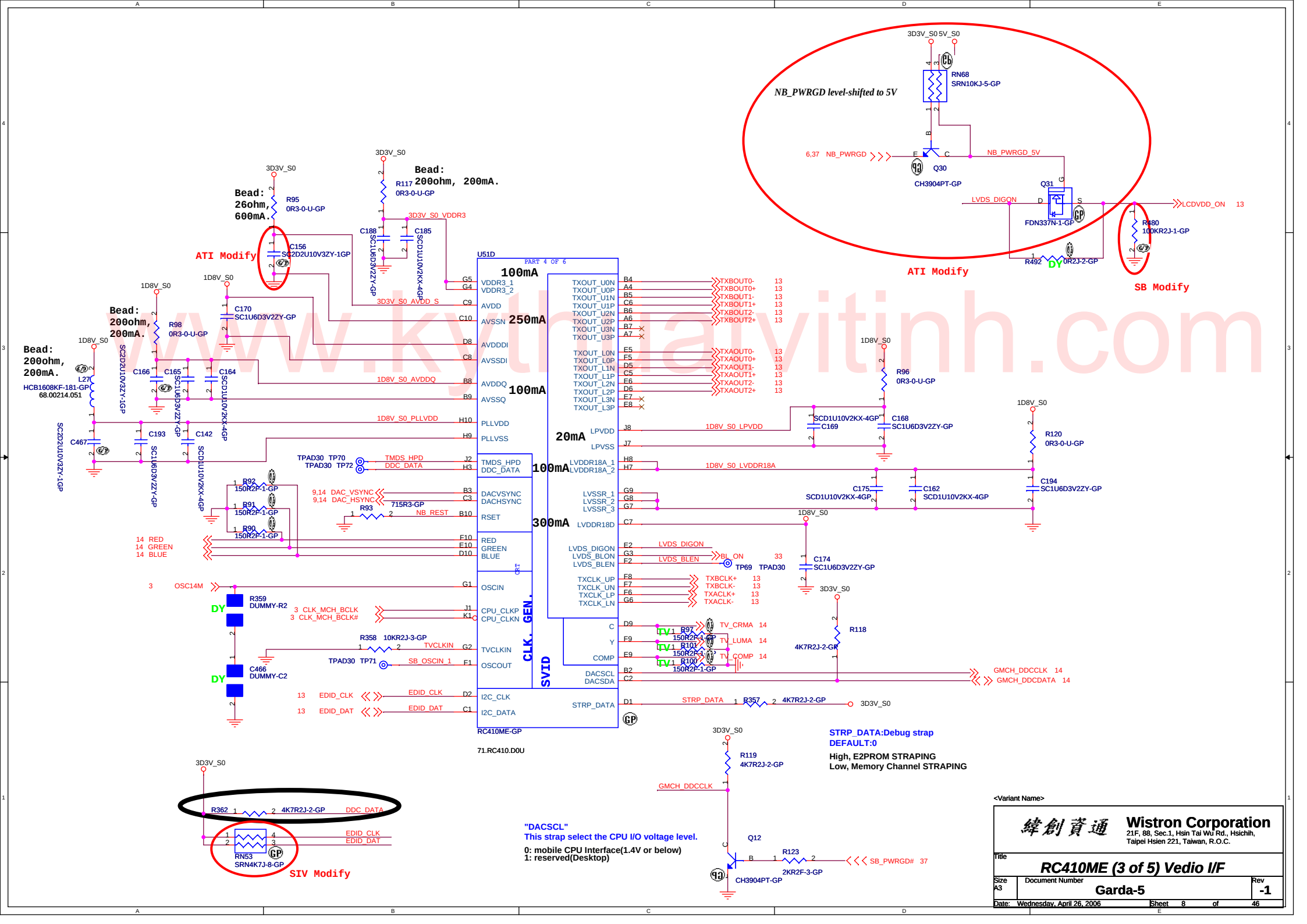
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RC410ME (2 of 5) Memory I/F

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 7 of 46


NB_PWRGD level-shifted to 5V
ATI Modify
SB Modify
SIV Modify
U51D
PART 4 OF 6
RC410ME-GP
71.RC410.D0U
CLK. GEN.
SVID
100mA
250mA
100mA
20mA
100mA
300mA
Bead: 200ohm, 200mA.
Bead: 26ohm, 600mA.
Bead: 200ohm, 200mA.
Bead: 200ohm, 200mA.
STRP_DATA:Debug strap
DEFAULT:0
High, E2PROM STRAPING
Low, Memory Channel STRAPING
"DACSCL"
This strap select the CPU I/O voltage level.
0: mobile CPU Interface(1.4V or below)
1: reserved(Desktop)
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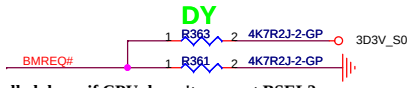
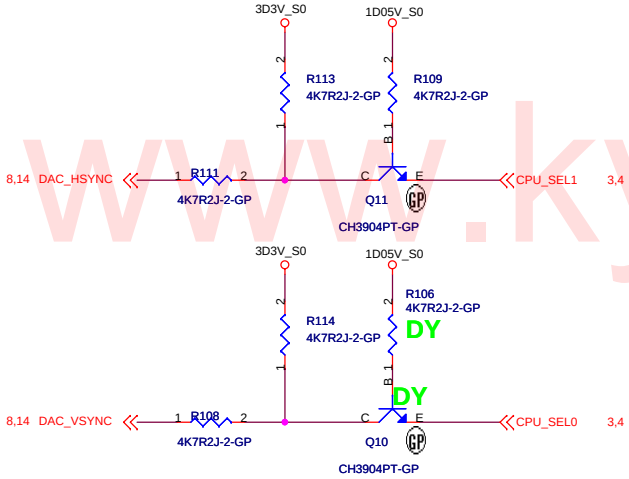
RC410ME (3 of 5) Vedio I/F
Garda-5
-1
Wednesday, April 26, 2006
Sheet 8 of 46

NB Strap pins

All pull-up and pull-down resistors are 4.7kohm.

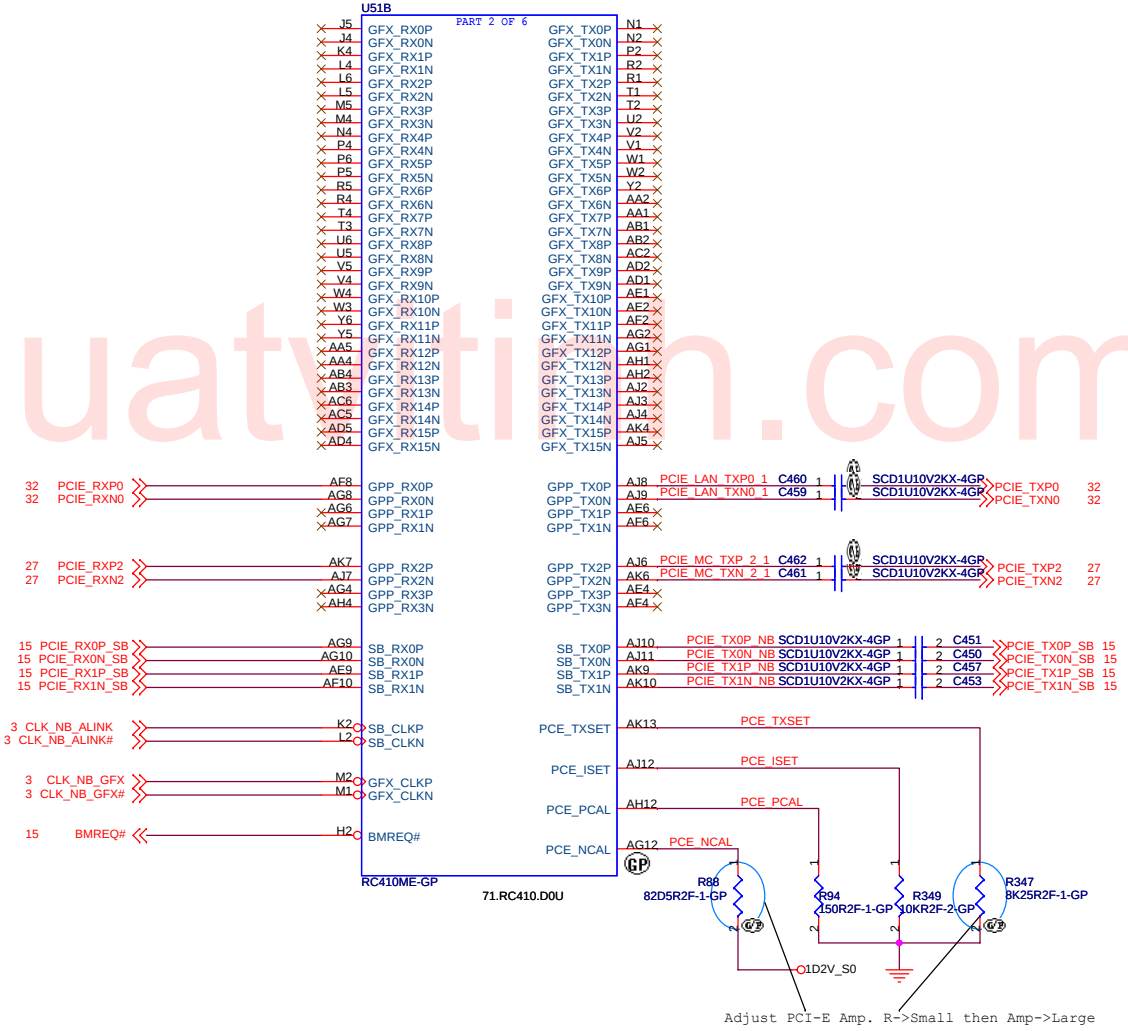


BMREQ# pulled down if CPU doesn't support BSEL2.



Select the FSB SPEED

BMREQ#	HSYNC	VSYNC	Freq.
0	0	0	100MHZ
0	0	1	133MHZ
0	1	0	------
0	1	1	166MHZ
1	0	0	100MHZ
1	0	1	100MHZ
1	1	0	------
1	1	1	------



<Variant Name>

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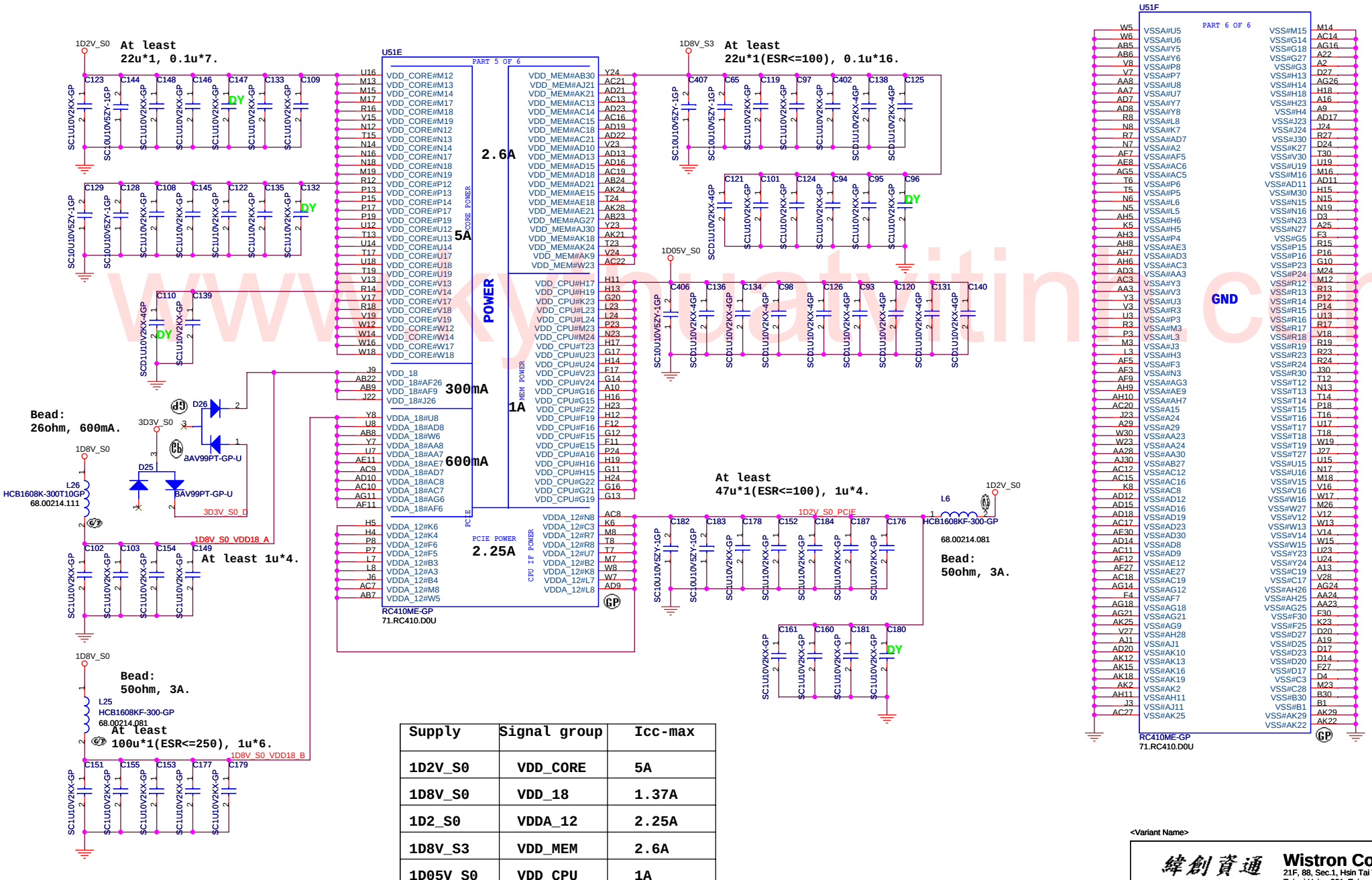
Title: RC410ME (4 of 5) PCI-E & Strap

Size: A3 | Document Number: Garda-5 | Rev: SA

Date: Wednesday, April 26, 2006 | Sheet 9 of 46



Supply	Signal group	Icc-max
1D2V_S0	VDD_CORE	5A
1D8V_S0	VDD_18	1.37A
1D2_S0	VDDA_12	2.25A
1D8V_S3	VDD_MEM	2.6A
1D05V_S0	VDD_CPU	1A

<Variant Name>

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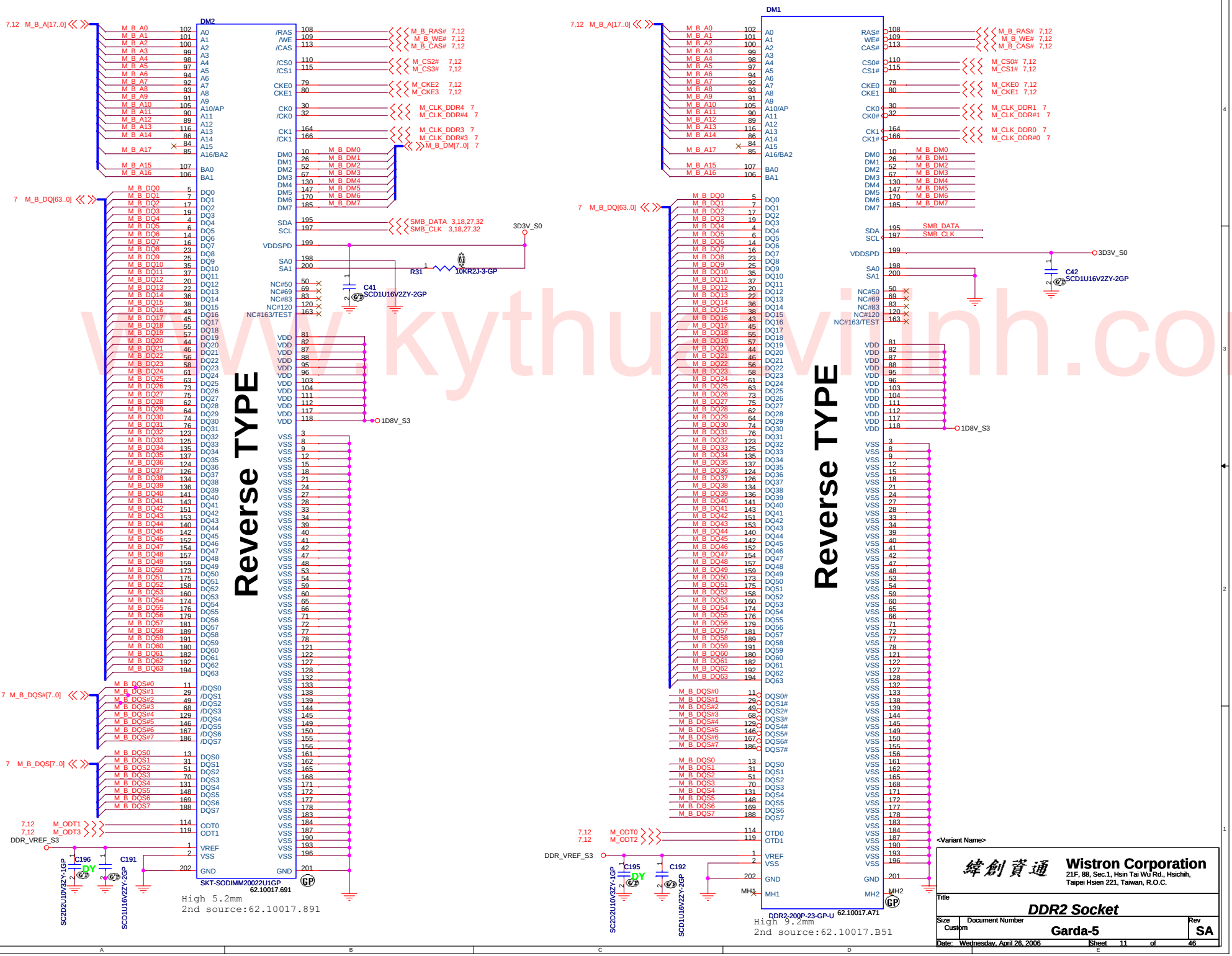
Title: RC410ME (5 of 5) Power

Size: A3 | Document Number: Garda-5 | Rev: SA

Date: Wednesday, April 26, 2006 | Sheet 10 of 46



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Taipei Hsien 221, Taiwan, R.O.C.

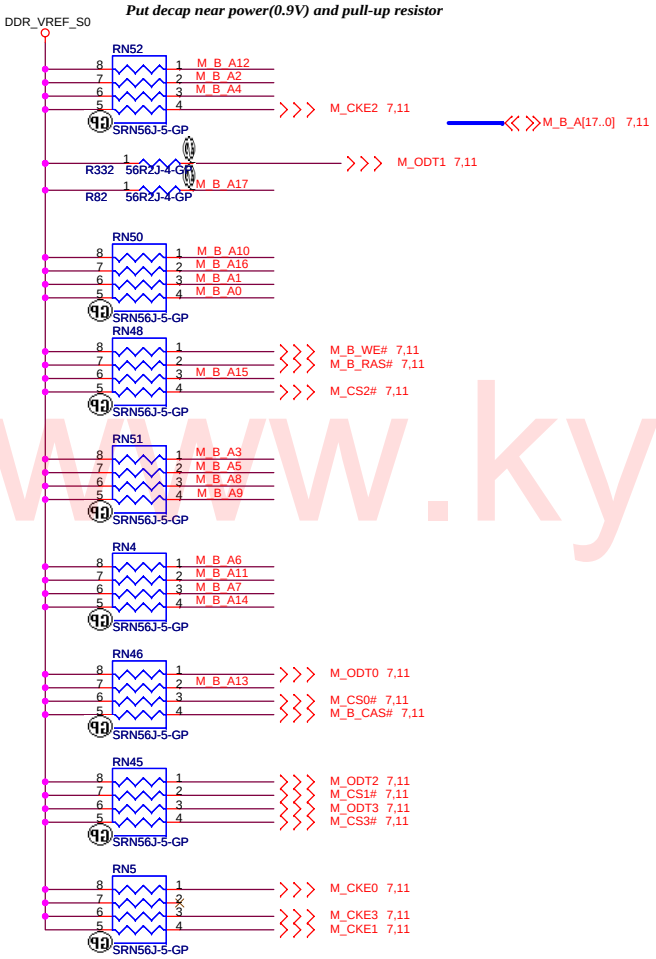
<variant_name>

Title: DDR2 Socket

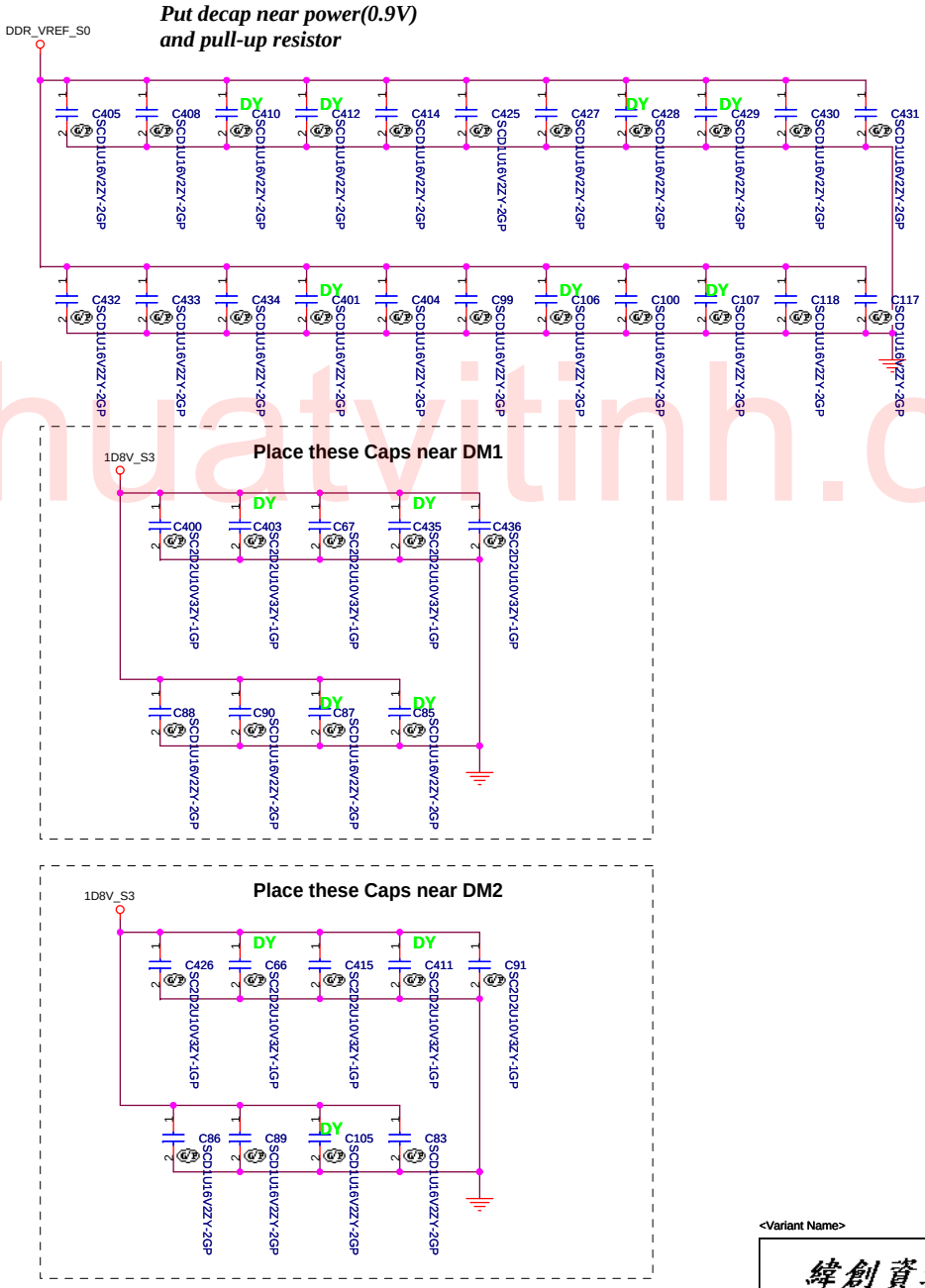
Size: Custom | Document Number: Garda-5 | Rev: SA

Date: Wednesday, April 26, 2006 | Sheet 11 of 46

PARALLEL TERMINATION



Decoupling Capacitor



<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	Garda-5	SA

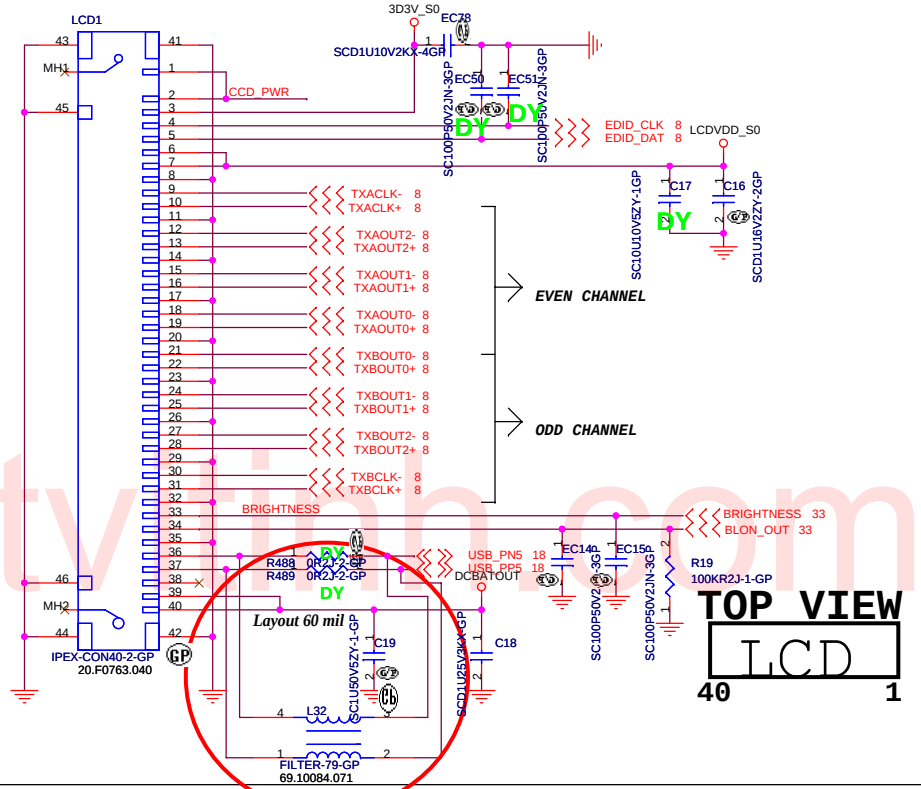
Date: Wednesday, April 26, 2006 Sheet 12 of 46

LCD/INVERTER/CCD CONN

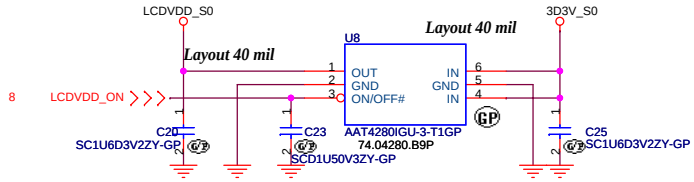
CCD Pin	
Pin	Symbol
1	3.3V
2	USB-
3	USB+
4	GND
5	GND

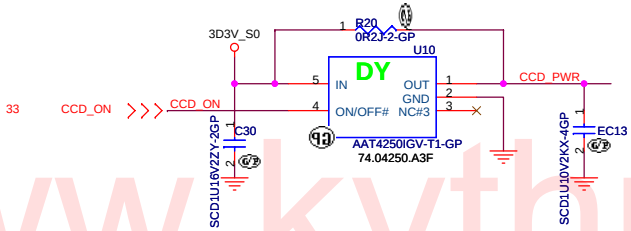
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

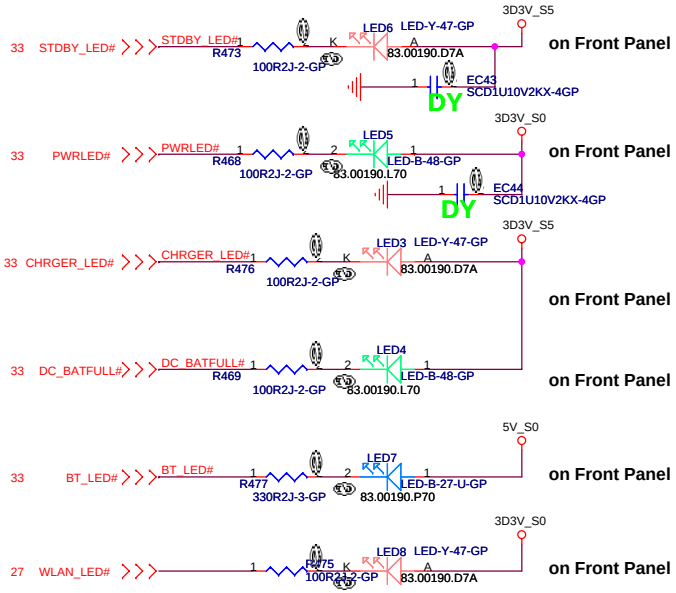
Launch BD	
Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN



-1 EMI Modify



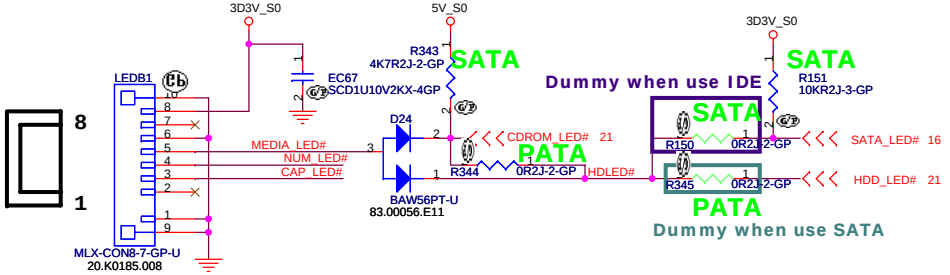




Charger:
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low

Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4

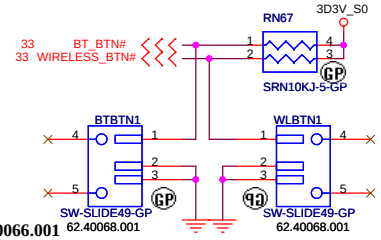
LED BD CONN



1st source: 20.K0228.008

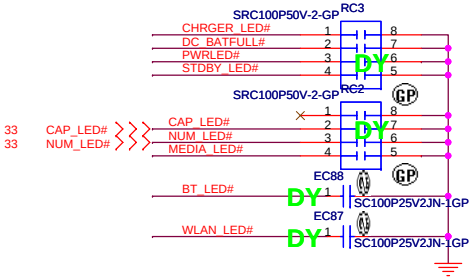
Front panel

LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2



2nd source: 62.40066.001

Edge Trigger



<Variant Name>

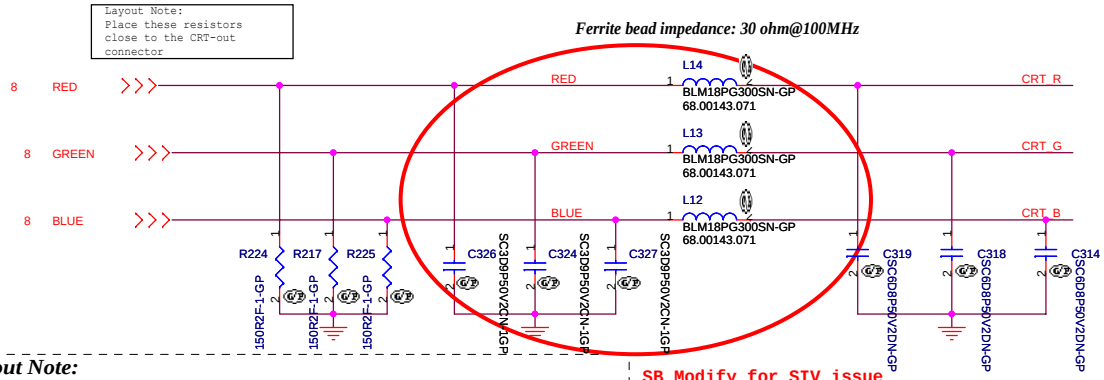
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LAUNCH / LEDs**

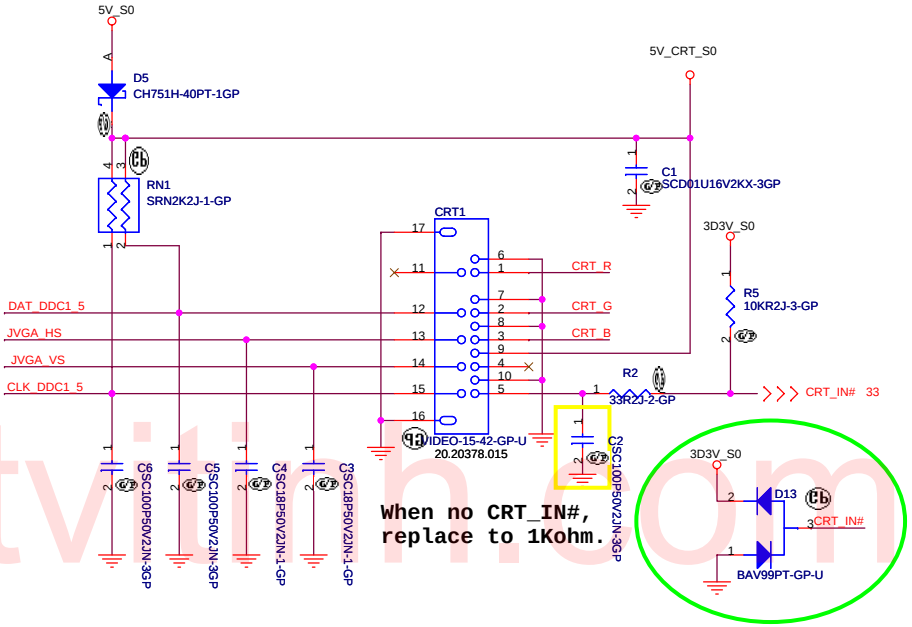
Size	Document Number	Rev
A3	Gards-5	-1

Date: Wednesday, April 26, 2006 Sheet 13 of 46

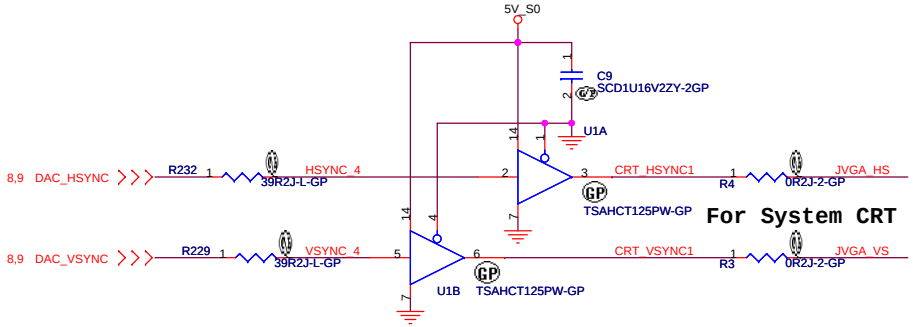
CRT I/F & CONNECTOR



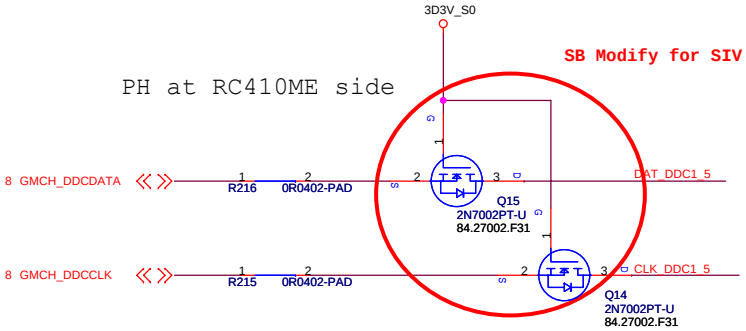
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



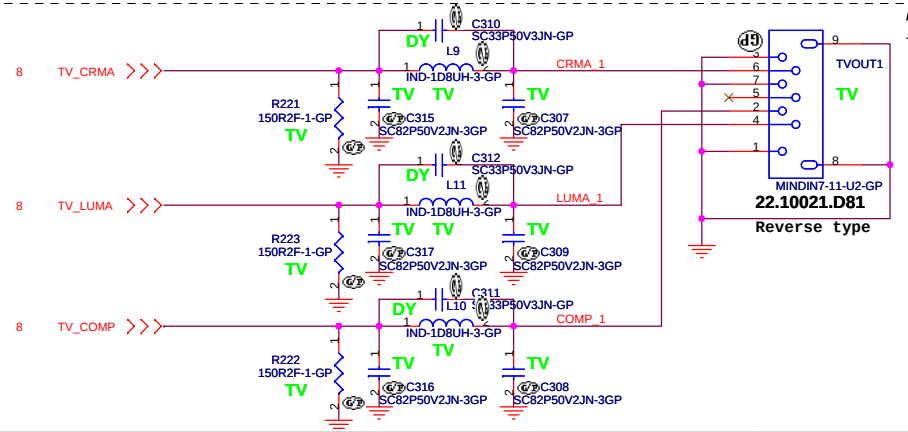
Hsync & Vsync level shift

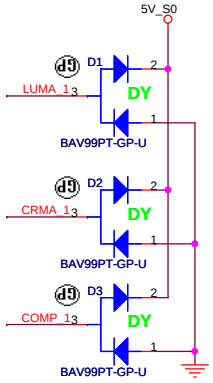


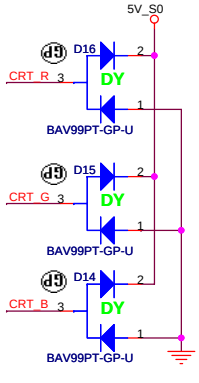
DDC_CLK & DATA level shift

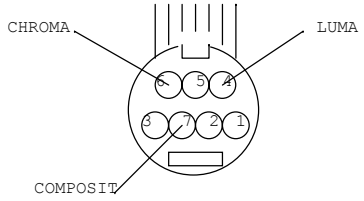


TV OUT CONN









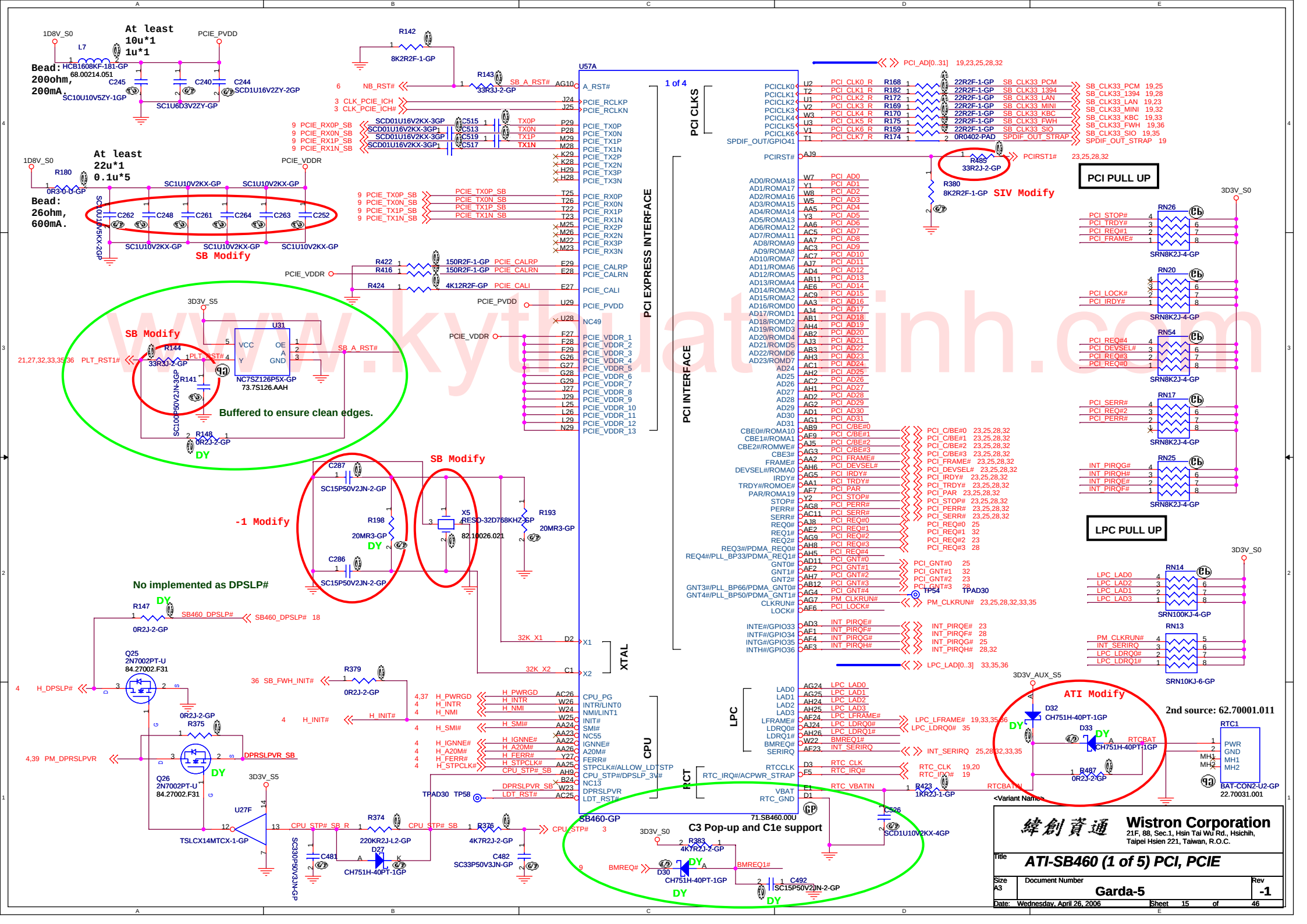
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

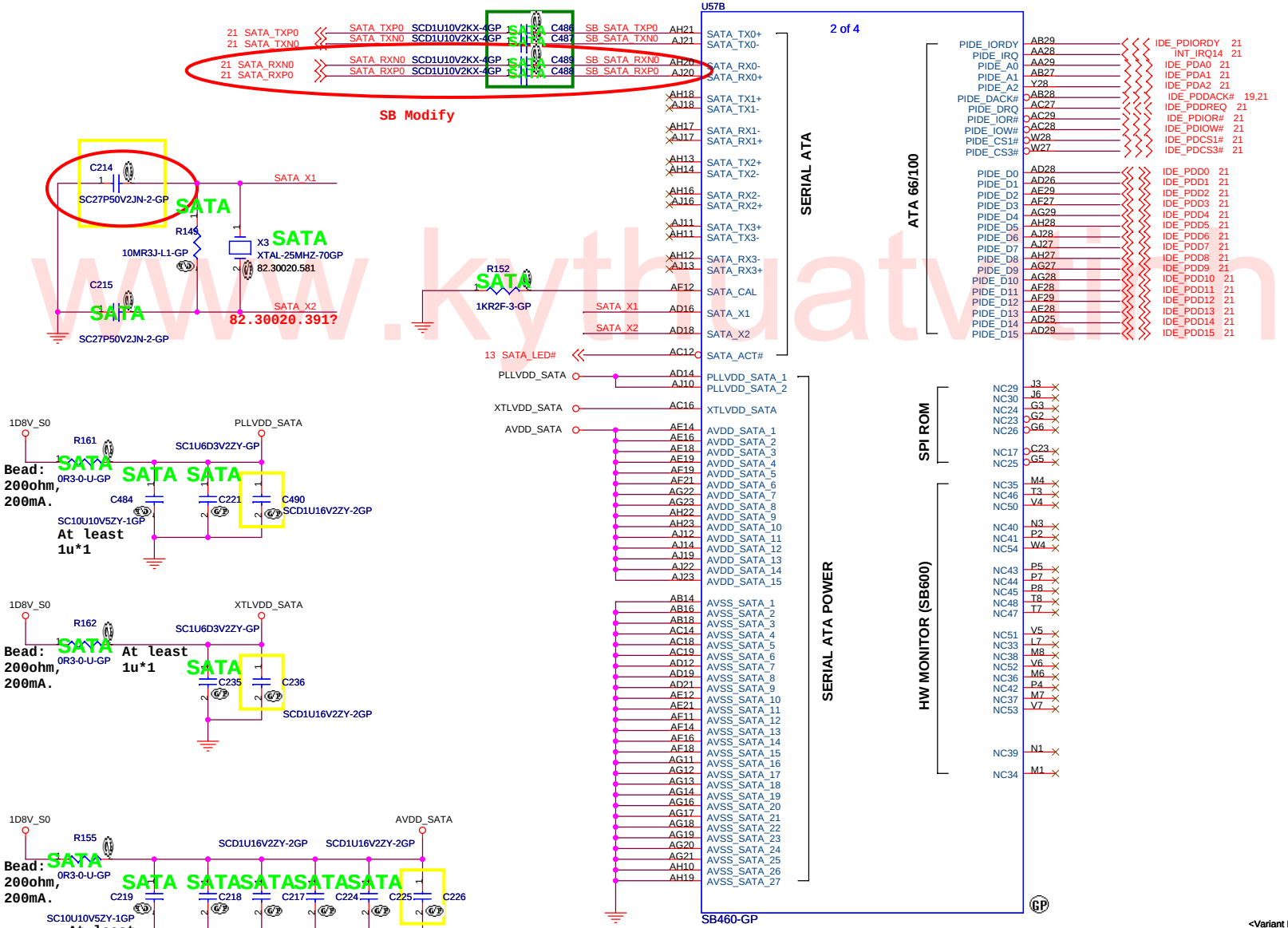
Title: **CRT/TV Connector**

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 14 of 46


U57A
1 of 4
SB460-GP
71.SB460.00U
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
CPU
LPC
RCT
PCI PULL UP
LPC PULL UP
SB Modify
SIV Modify
ATI Modify
-1 Modify
DY
Buffered to ensure clean edges.
No implemented as DPSLP#
C3 Pop-up and C1e support
Bead: 200ohm, 200mA.
Bead: 26ohm, 600mA.
At least 10u*1 1u*1
At least 22u*1 0.1u*5
2nd source: 62.70001.011
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB460 (1 of 5) PCI, PCIE
Garda-5
-1
Wednesday, April 26, 2006
15 of 46

When no SATA replace to 0 ohm.



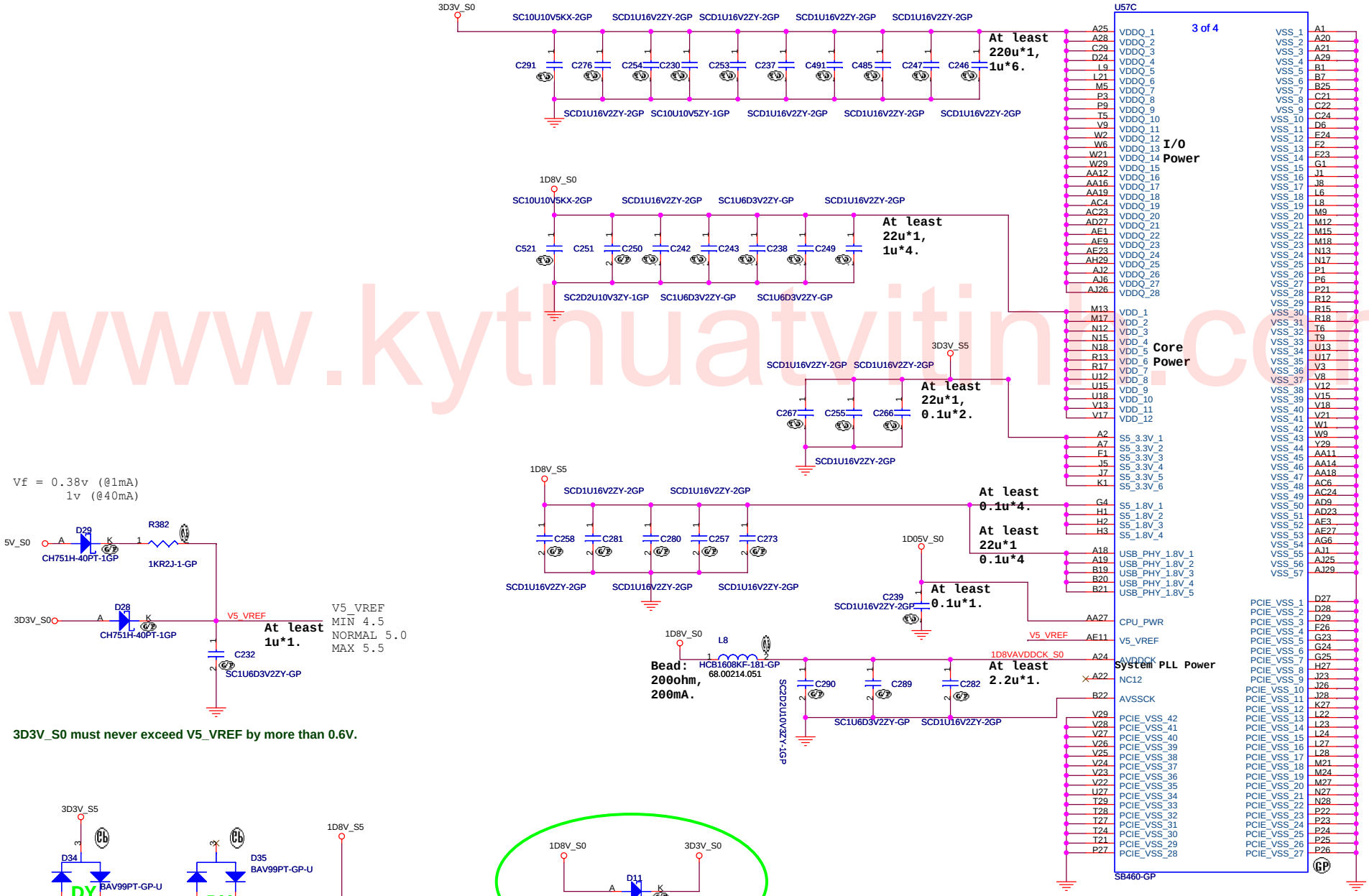
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB460 (2 of 5) IDE/SATA

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 16 of 46



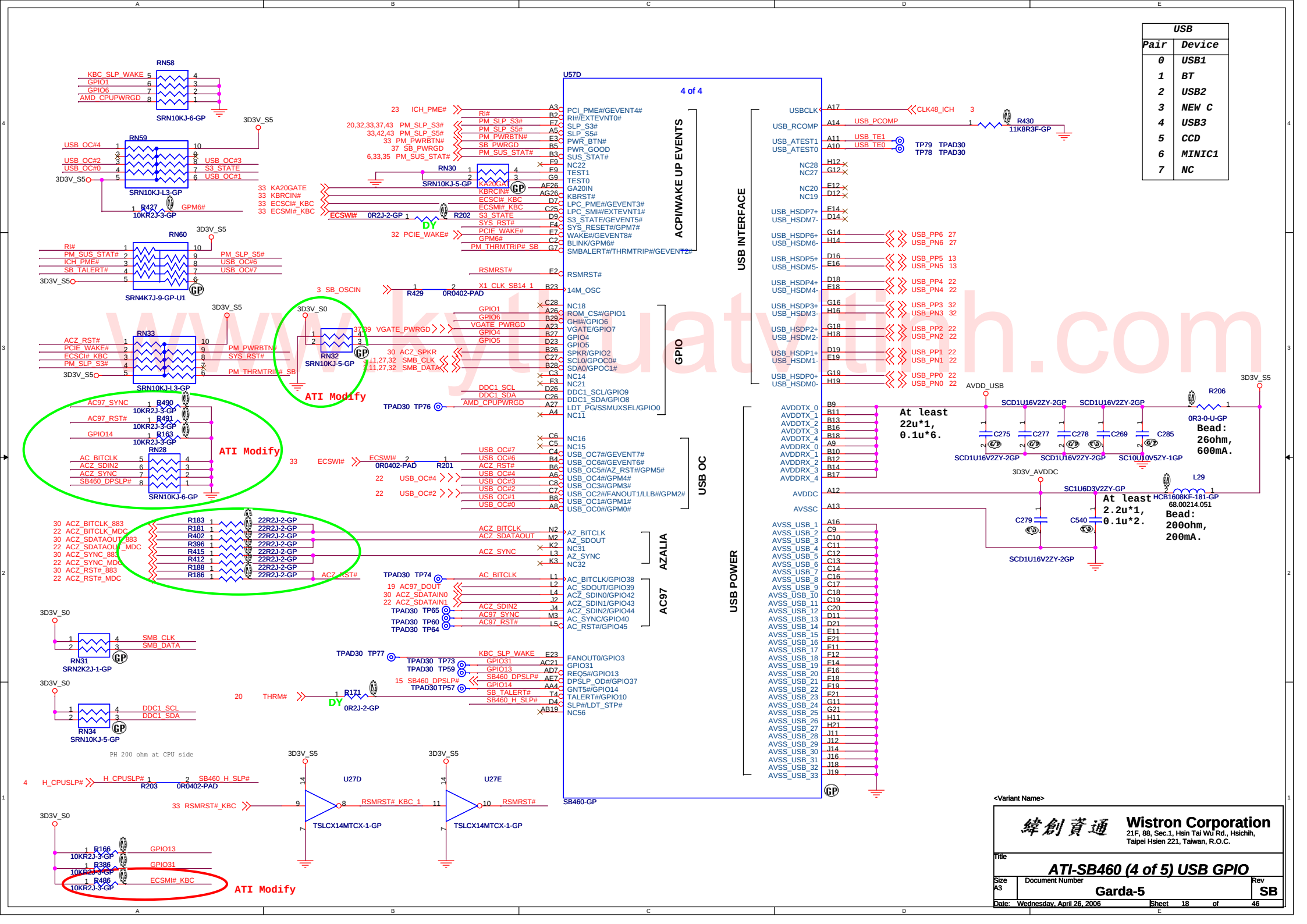
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

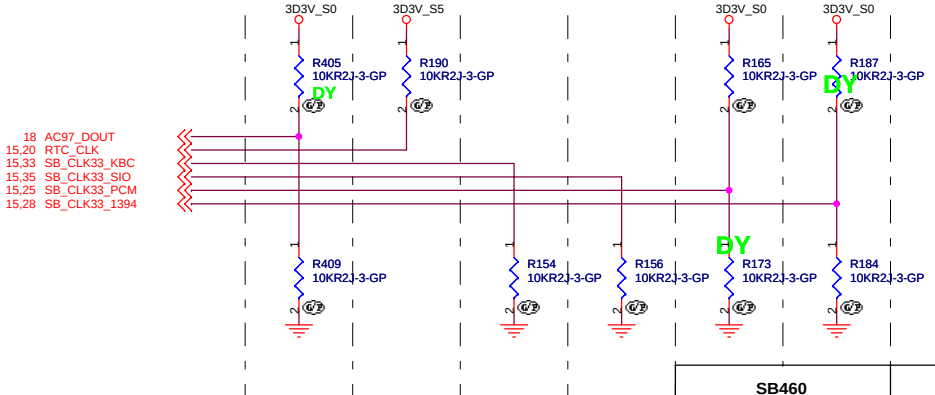
Title: ATI-SB460 (3 of 5) POWER

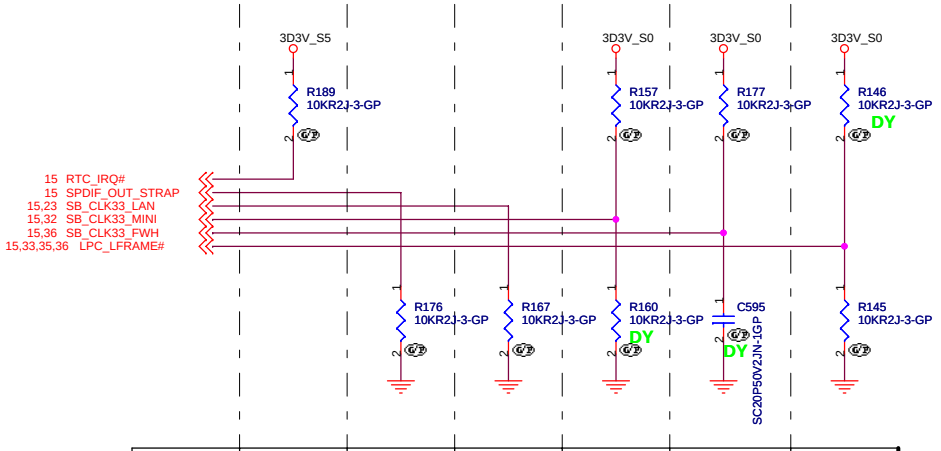
Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 17 of 46



REQUIRED STRAPS





PCI_CLK0 PCM
PCI_CLK1 IEEE1394
PCI_CLK2 LAN
PCI_CLK3 MINI
PCI_CLK4 KBC
PCI_CLK5 FWH
PCI_CLK6 SIO
PCI_CLK7 SPDIFOUT

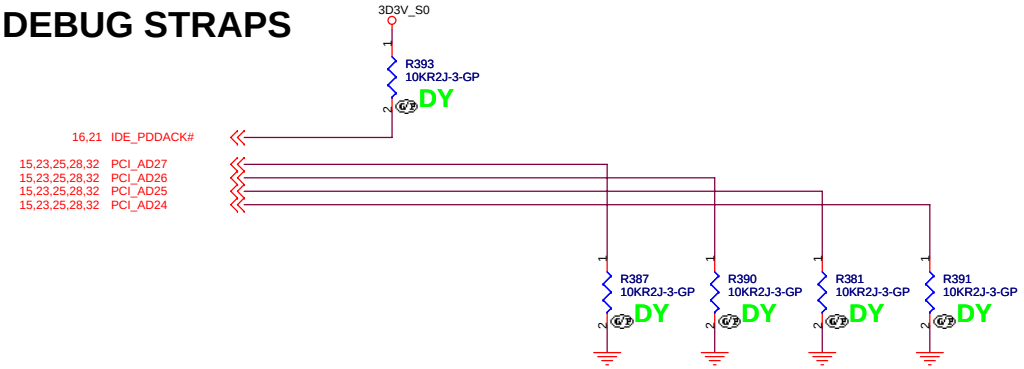
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	SB460 PCI_CLK0	SB460 PCI_CLK1	SB600 PCI_CLK0	SB600 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. USB PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM; H, L = LPC I ROM DEFAULT; L, H = LPC II ROM; L, L = FWH ROM		ROM TYPE: H, H = PCI ROM; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM	
PULL LOW	DISABLE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. USB 48MHZ SOURCE DEFAULT	CPU IF=P4 DEFAULT	NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]			

Require upper 12 addr bits set to "1".

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	48M XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE LANE AUTO DETECT DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE LANE FORCING TO 2 LANES DEBUG ONLY	DISABLE THERMTRIP#

USB wake from S5 supported.

DEBUG STRAPS



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT		BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY SB600 ONLY SB600 ONLY

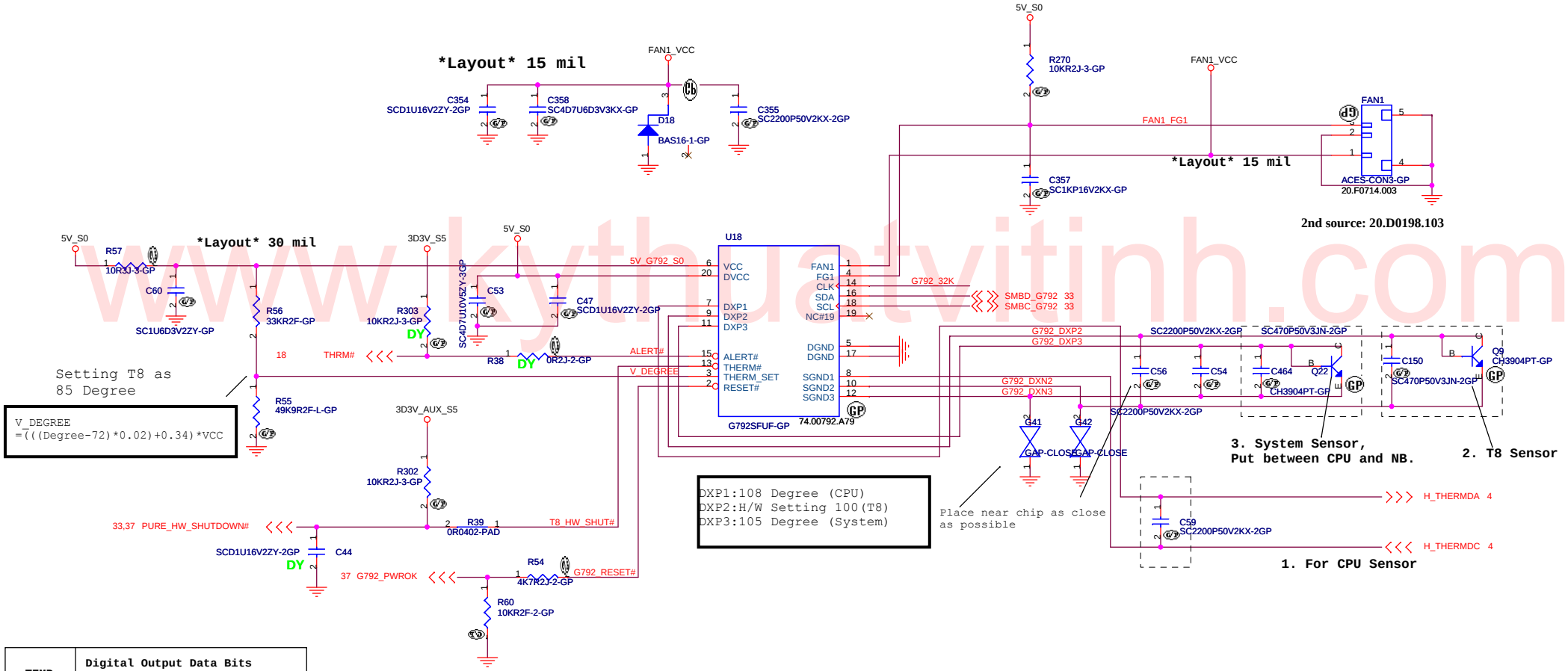
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB460 (5 of 5) STRAPPING

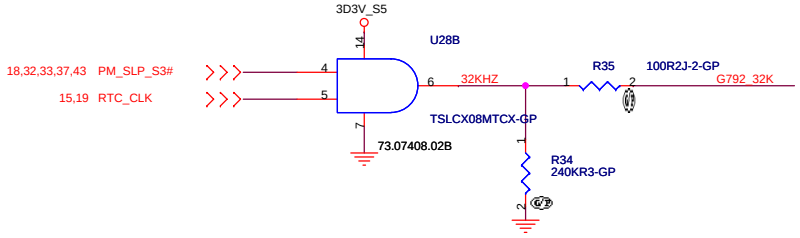
Size: A3 | Document Number: Garda5 | Rev: SA

Date: Wednesday, April 26, 2006 | Sheet 19 of 46



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

32K suspend clock output



<Variant Name>

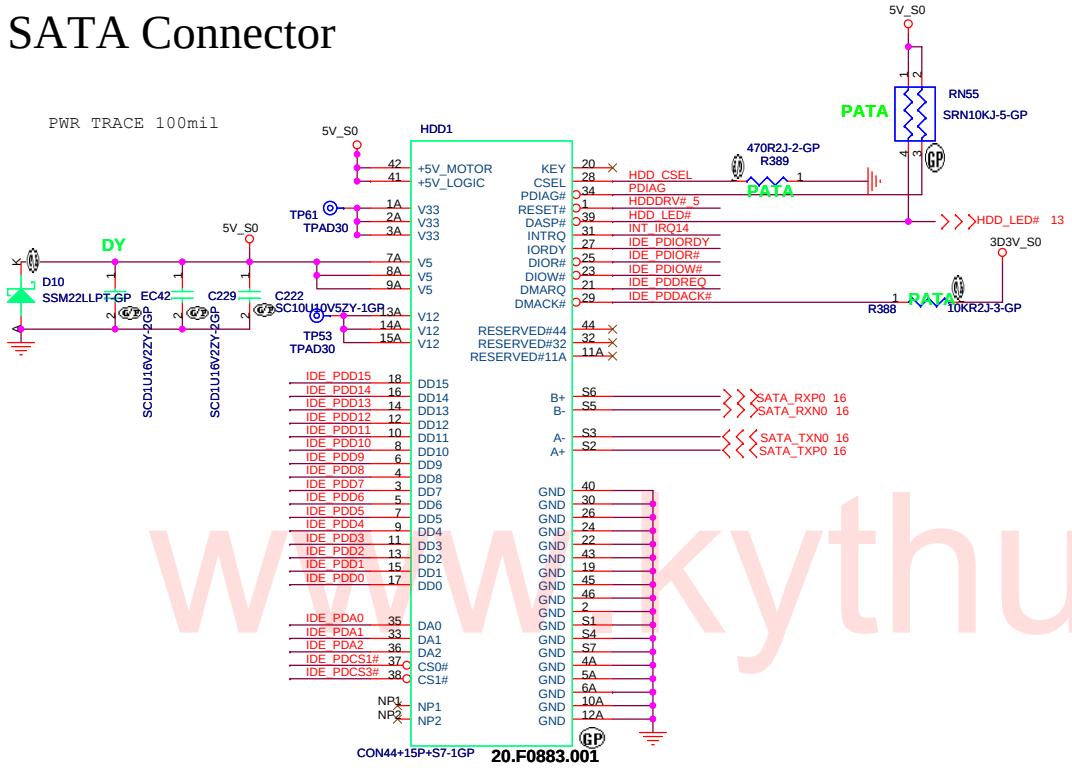
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor G792***

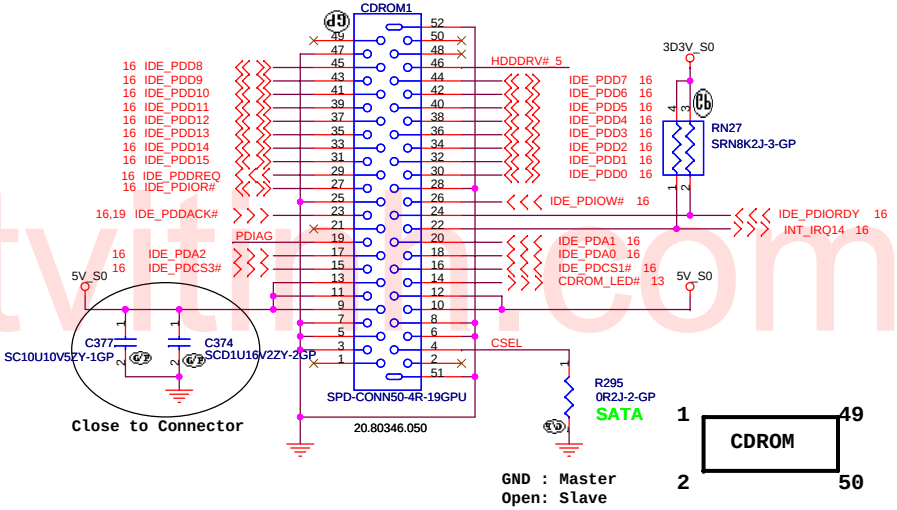
Size: Custom | Document Number: **Garda-5** | Rev: **SA**

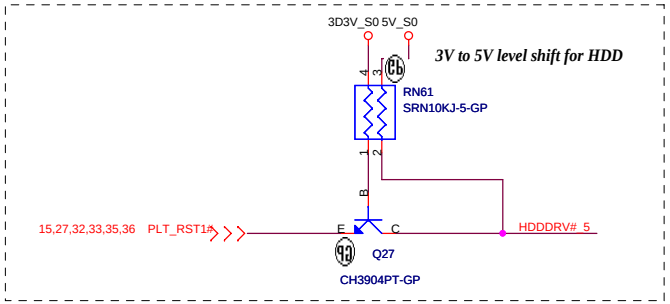
Date: Wednesday, April 26, 2006 | Sheet 20 of 46

SATA Connector



CDROM Connector





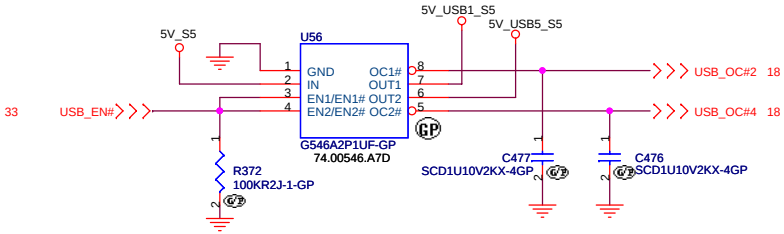
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

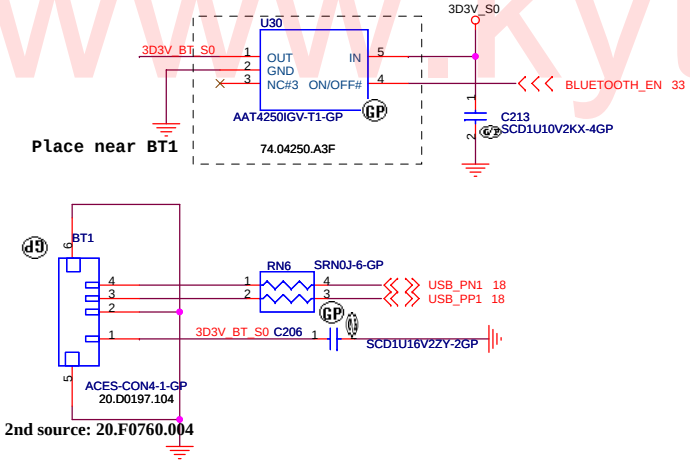
Title: SATA/PATA HDD / ODD

Size: A3 | Document Number: Garda-5 | Rev: SA

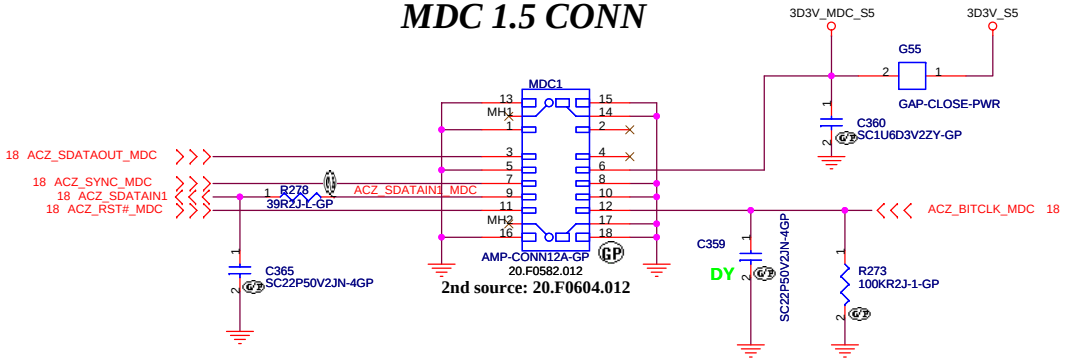
Date: Wednesday, April 26, 2006 | Sheet 21 of 46



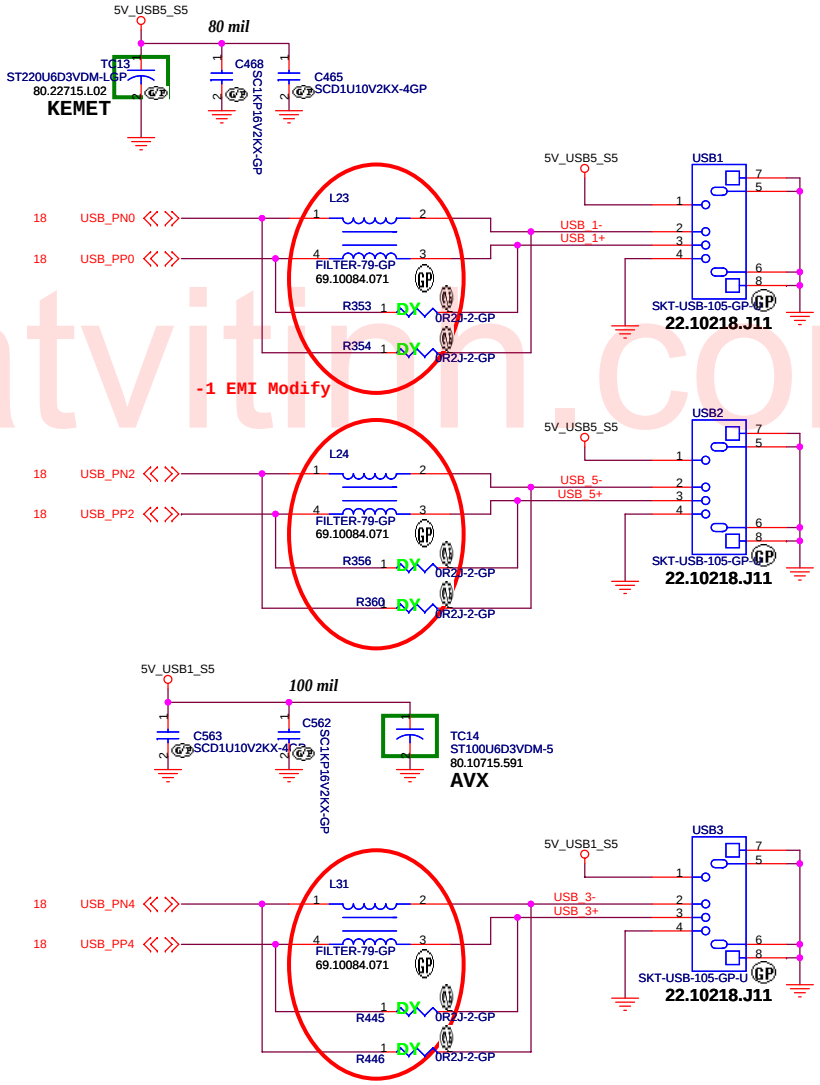
BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONN



USB PORT



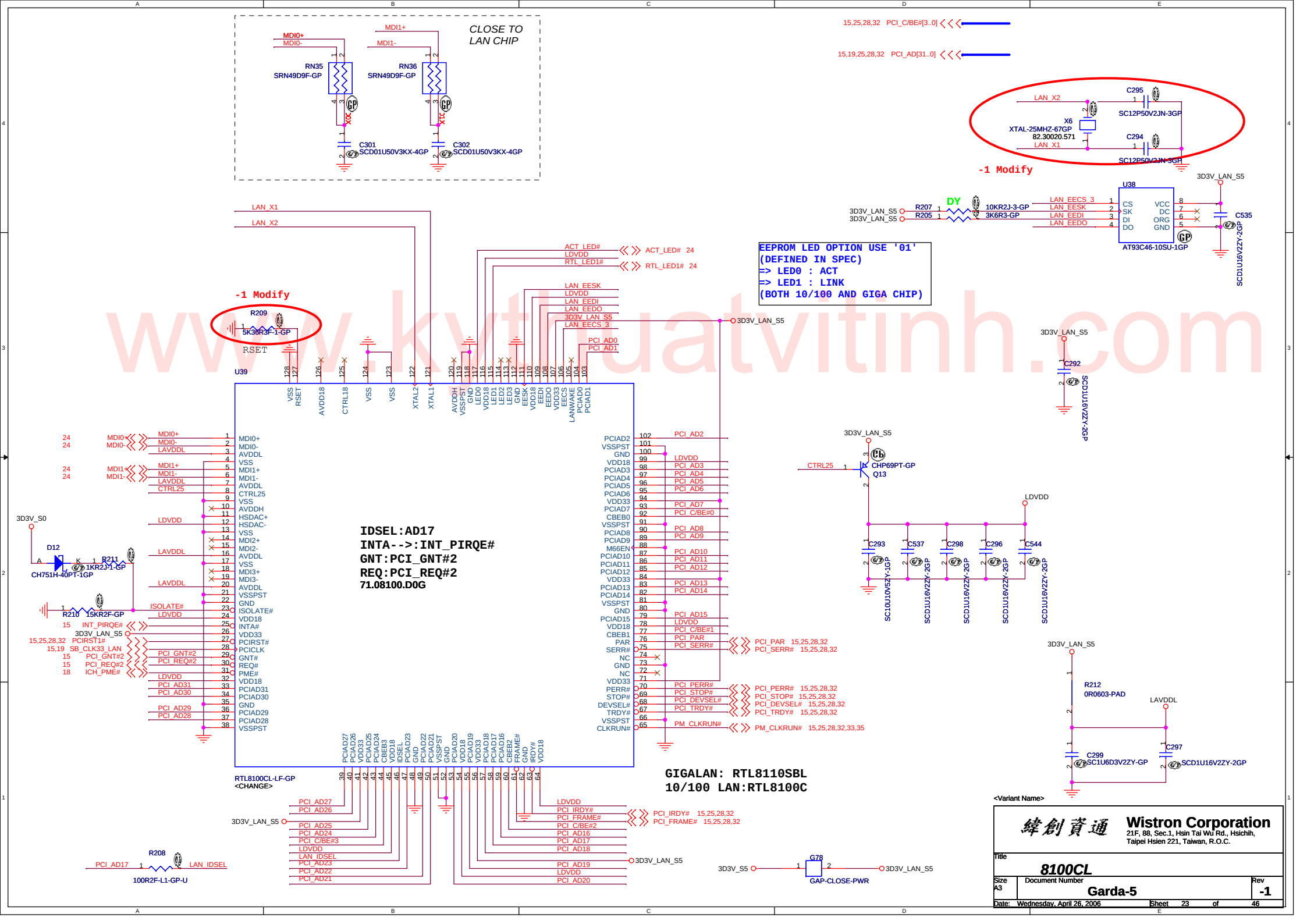
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

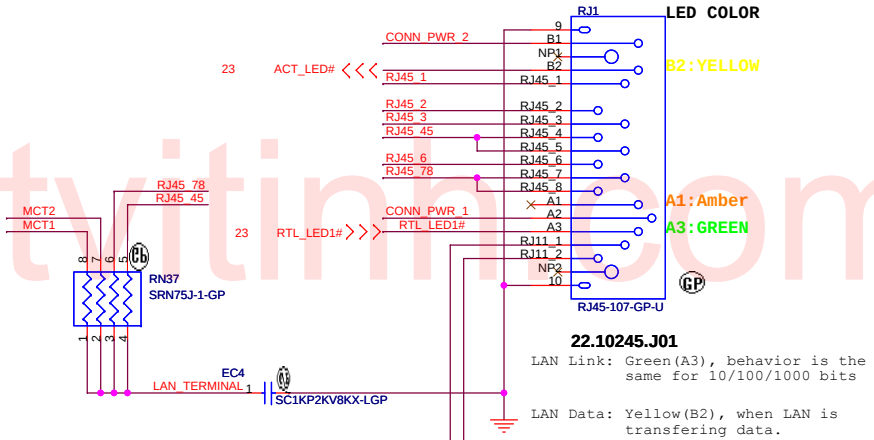
Title: USB and MDC I/F

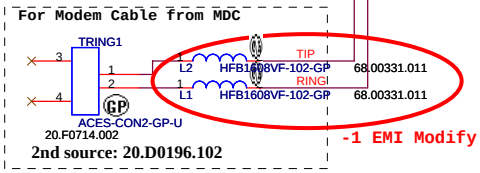
Size	Document Number	Rev
A3	Garda-5	-1

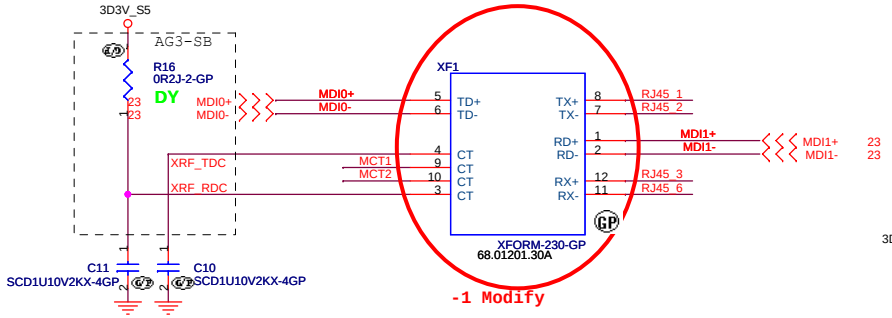
Date: Wednesday, April 26, 2006 Sheet 22 of 46

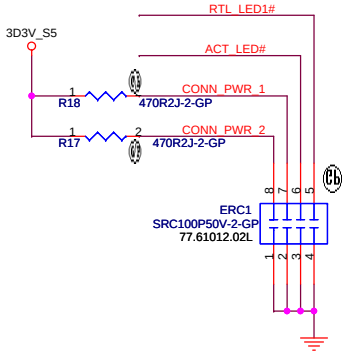


LAN Connector









1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

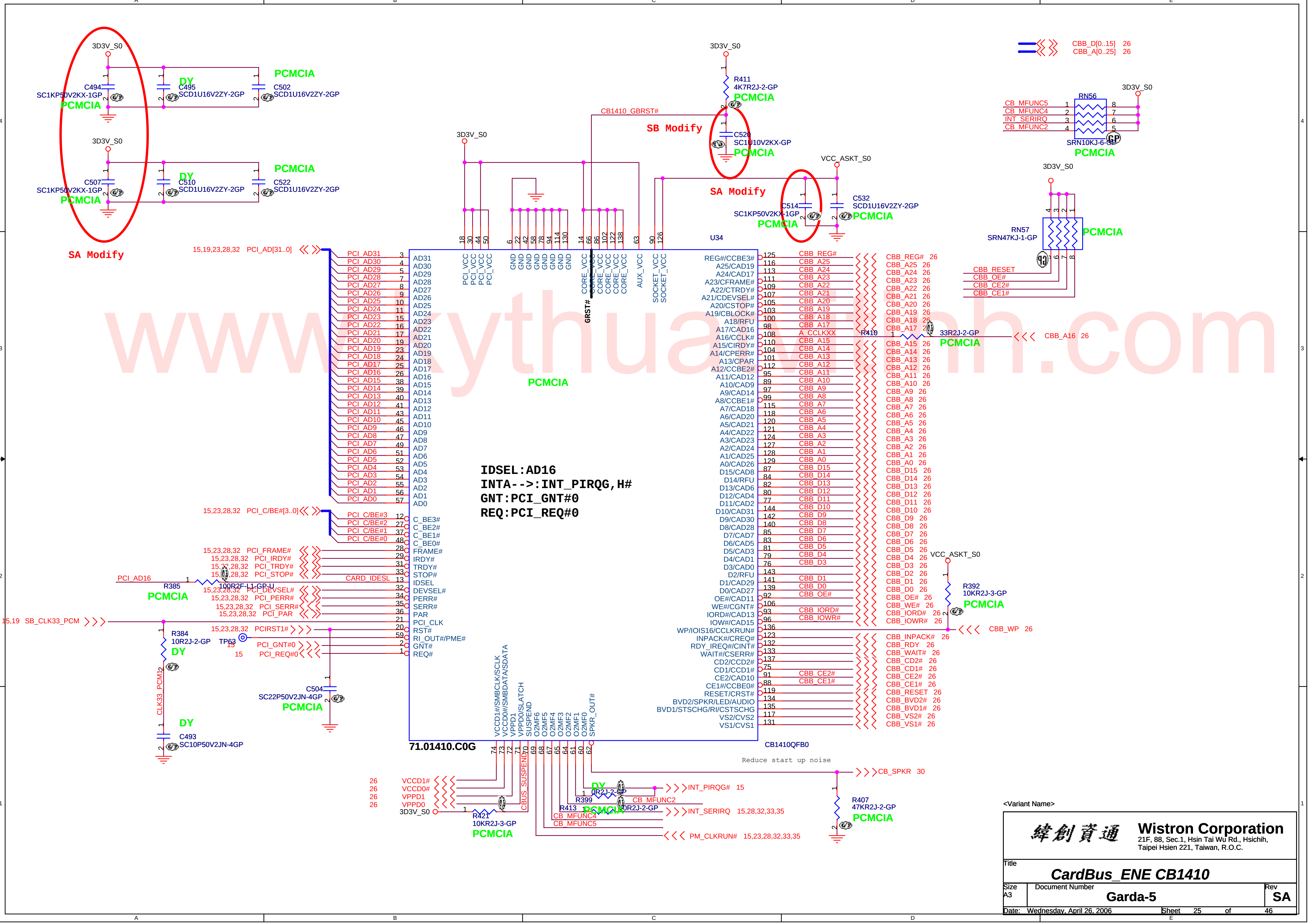
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

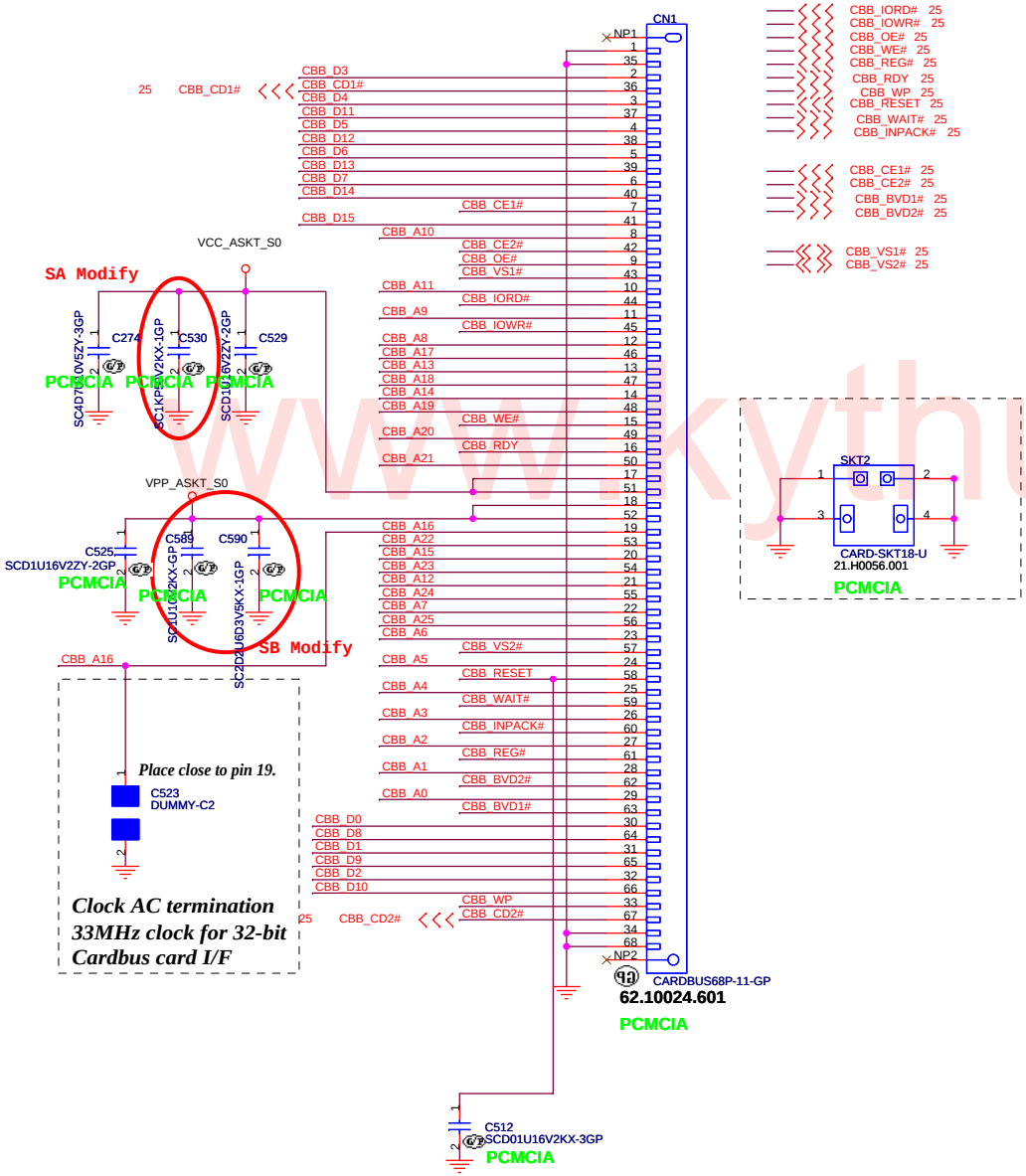
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

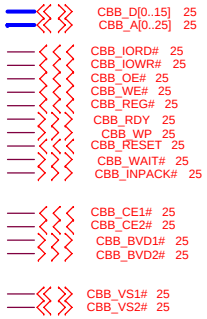
Title: LAN Connector
Size: A3 | Document Number: Garda-5 | Rev: -1
Date: Wednesday, April 26, 2006 | Sheet 24 of 46


www.kythuatvitinh.com
SA Modify
SB Modify
SA Modify
3D3V_S0
C494 SC1KP50V2KX-1GP
C495 SCD1U16V2ZY-2GP
C502 SCD1U16V2ZY-2GP
C507 SC1KP50V2KX-1GP
C510 SCD1U16V2ZY-2GP
C522 SCD1U16V2ZY-2GP
DY
PCMCIA
R411 4K7R2J-2-GP
CB1410_GBRST#
C520 SC1U10V2KX-GP
VCC_ASKT_S0
C514 SC1KP50V2KX-1GP
C532 SCD1U16V2ZY-2GP
U34
CBB_D[0..15] 26
CBB_A[0..25] 26
CB_MFUNC5
CB_MFUNC4
INT_SERIRQ
CB_MFUNC2
RN56 SRN10KJ-6-GP
RN57 SRN47KJ-1-GP
CBB_RESET
CBB_OE#
CBB_CE2#
CBB_CE1#
15,19,23,28,32 PCI_AD[31..0]
15,23,28,32 PCI_C/BE#[3..0]
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_AD16
R385 100R2F-L1-GP-U
CARD_IDESL
PCI_DEVSEL#
PCI_PERR#
PCI_SERR#
PCI_PAR
15,19 SB_CLK33_PCM
R384 10R2J-2-GP
TP63
PCIRST1#
PCI_GNT#0
PCI_REQ#0
C504 SC22P50V2JN-4GP
CLK33_PCM1
C493 SC10P50V2JN-4GP
IDSEL:AD16
INTA-->:INT_PIRQG,H#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
71.01410.C0G
CB1410QFB0
R410 33R2J-2-GP
CBB_A16 26
R392 10KR2J-3-GP
CBB_WP 26
Reduce start up noise
CB_SPKR 30
INT_PIRQG# 15
R399 0R2J-2-GP
R413 0R2J-2-GP
INT_SERIRQ 15,28,32,33,35
PM_CLKRUN# 15,23,28,32,33,35
R407 47KR2J-2-GP
VCCD1# VCCD0# VPPD1 VPPD0
R421 10KR2J-3-GP
CBUS_SUSPEND
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CardBus_ENE CB1410
Size A3
Document Number Garda-5
Rev SA
Date: Wednesday, April 26, 2006
Sheet 25 of 46

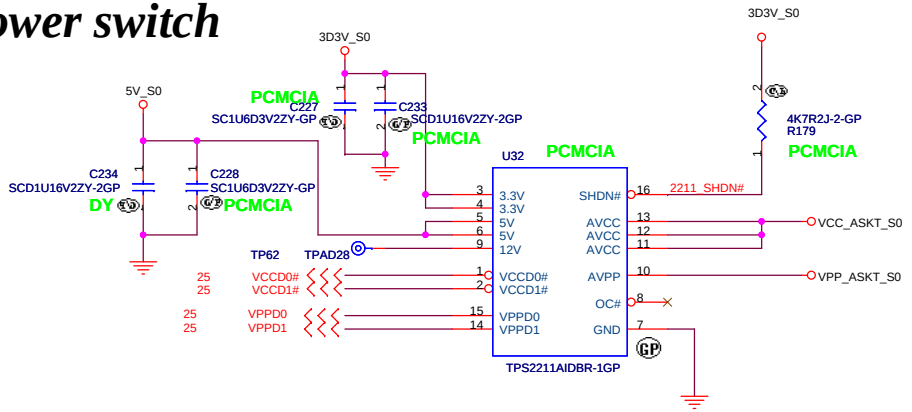
PCMCIA Socket



Cardbus I/F



Power switch

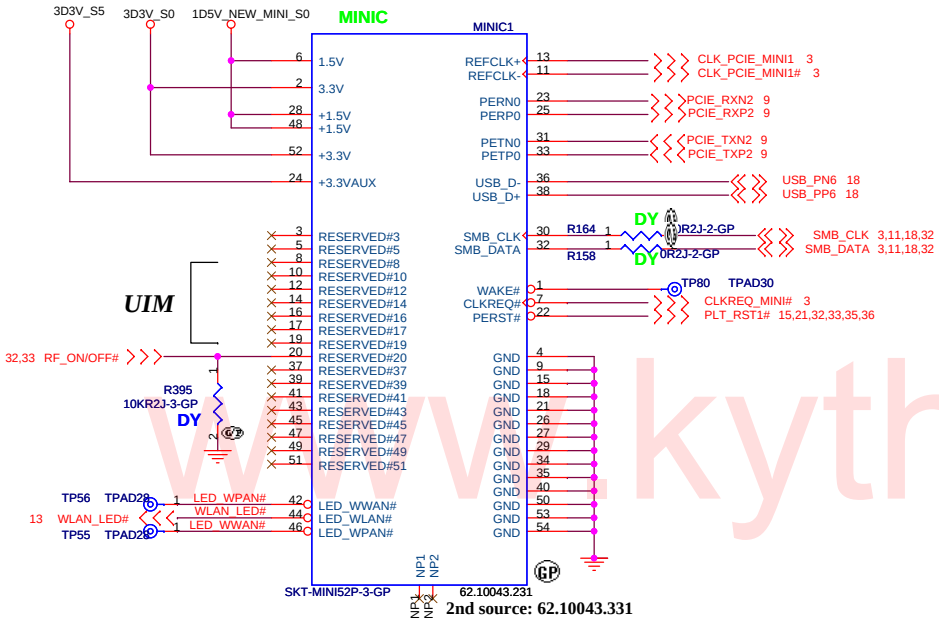


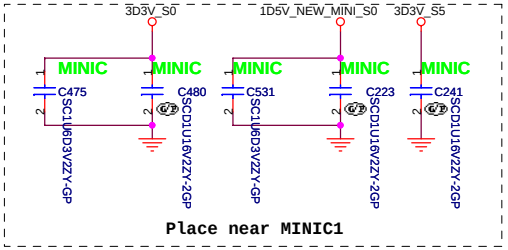
<Variant Name>

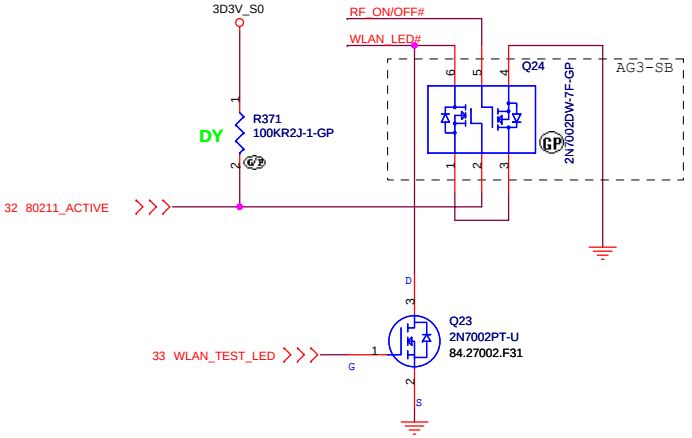
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

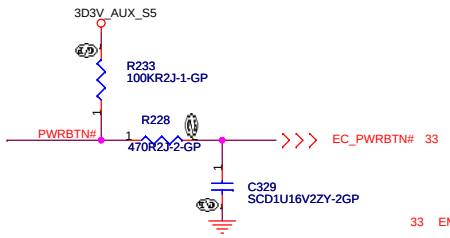
Title	PCMCIA	
Size A3	Document Number Garda-5	Rev SB
Date: Wednesday, April 26, 2006	Sheet 26 of 46	

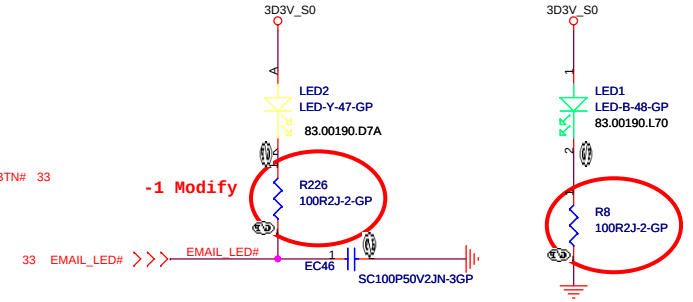
Mini Card Connector



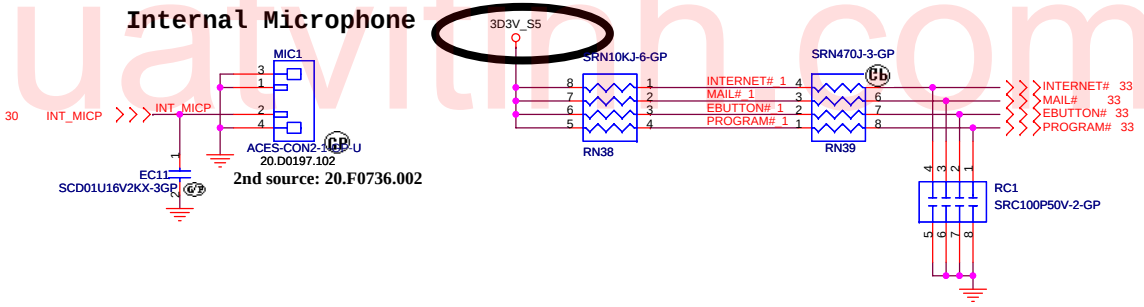






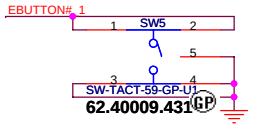


Internal Microphone



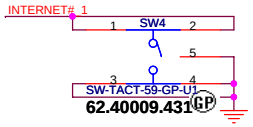
E-Button

TOP VIEW RIGHT 4



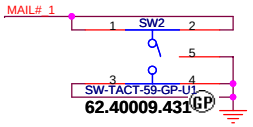
Internet Button

TOP VIEW RIGHT 3



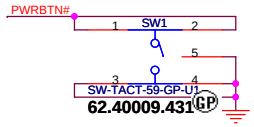
Mail Button

TOP VIEW RIGHT 2



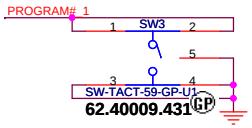
Power Button

TOP VIEW RIGHT 1



Program Button

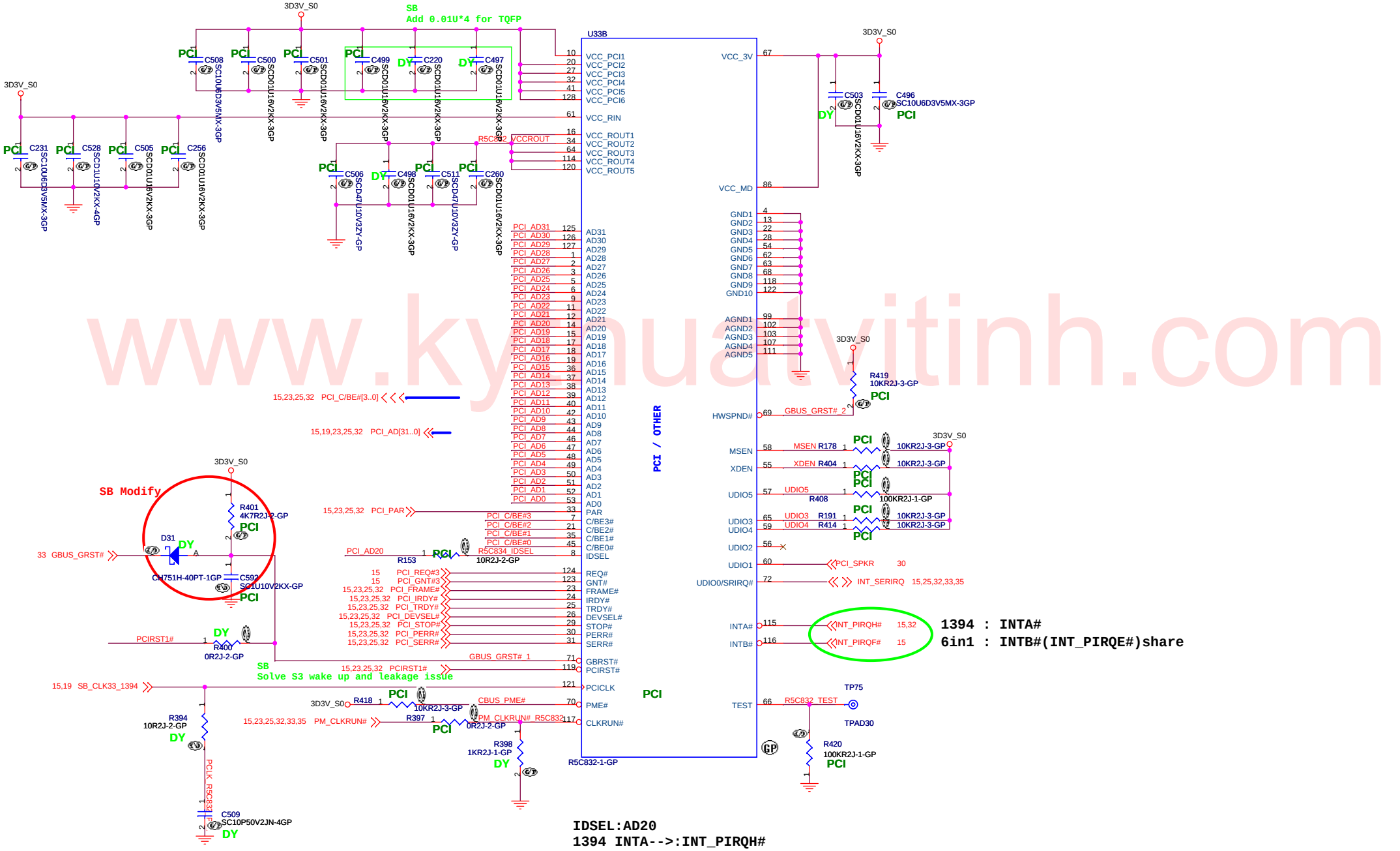
TOP VIEW RIGHT 5



LED					
Button	V	V	V	V	V
	Program Button	E-Button	Internet Button	Mail Button	Power Button

<Variant Name>

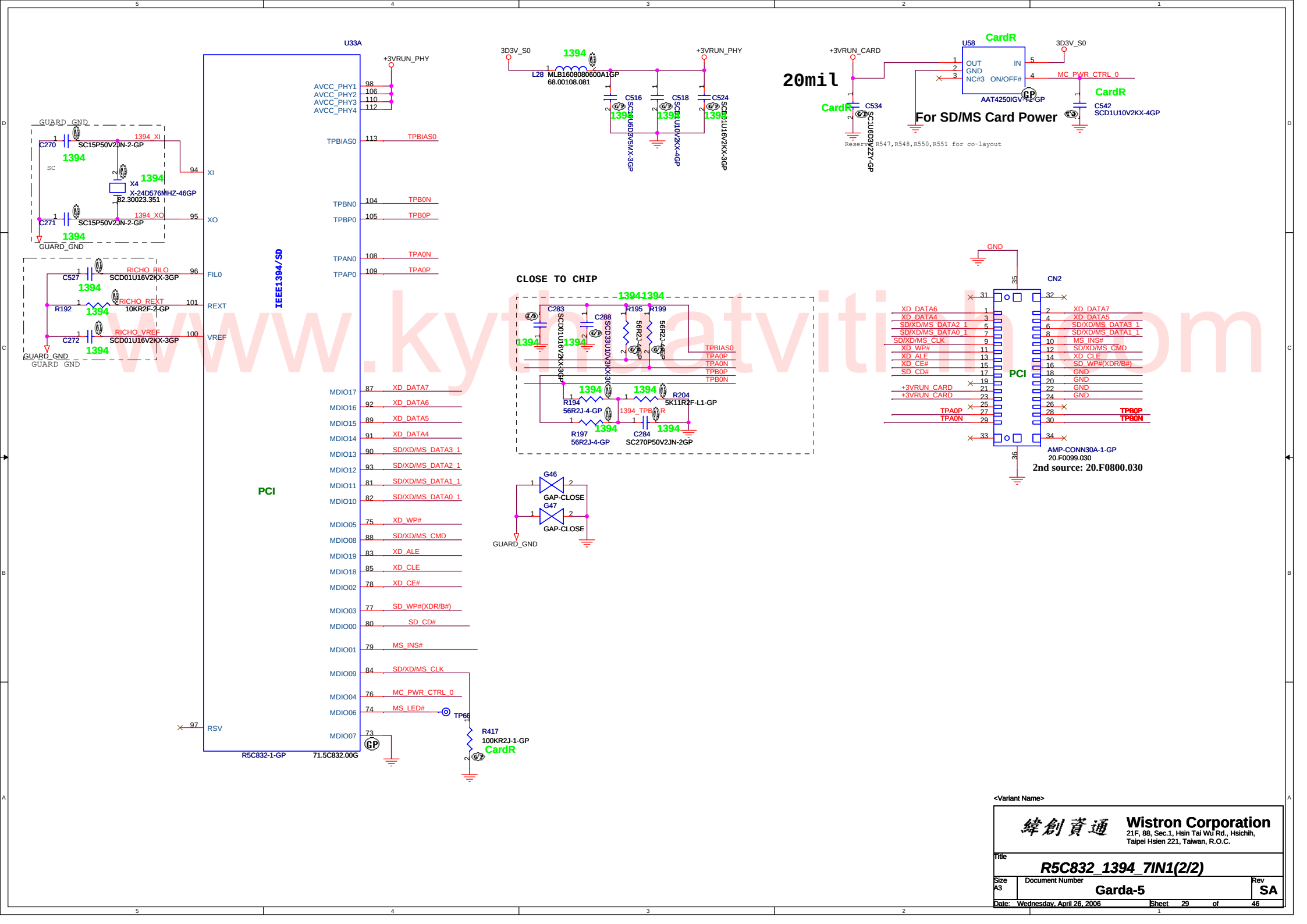
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD / Launch Button***	
Size A3	Document Number **Garda-5**	Rev **-1**
Date: Wednesday, April 26, 2006	Sheet 27 of 46	



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

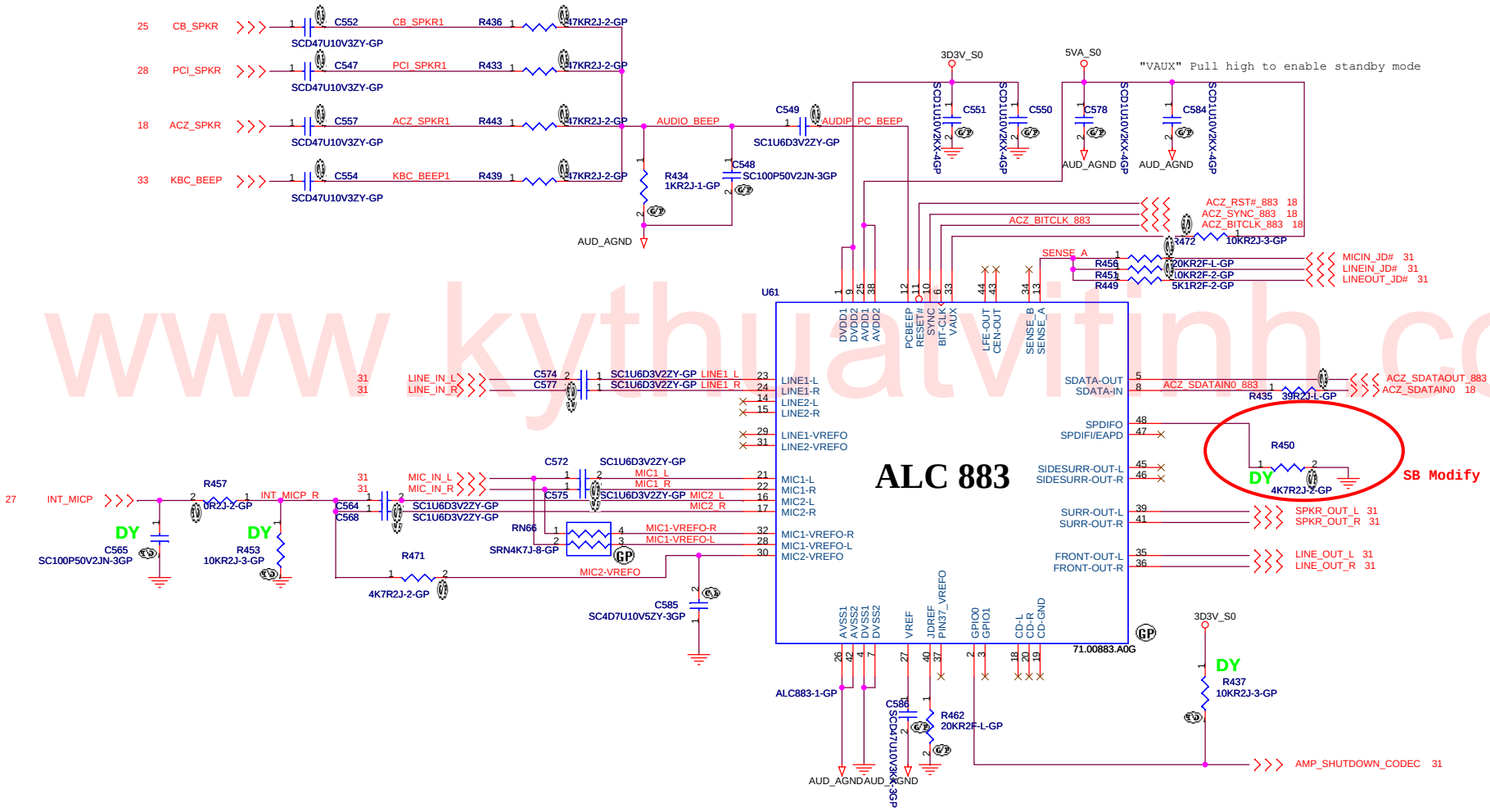
Title	R5C832_1394_7IN1(1/2)	
Size A3	Document Number Garda5	Rev SB
Date: Wednesday, April 26, 2006	Sheet 28 of 46	



<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	R5C832_1394_7IN1(2/2)	
Size A3	Document Number Garda-5	Rev SA
Date: Wednesday, April 26, 2006	Sheet 29 of 46	



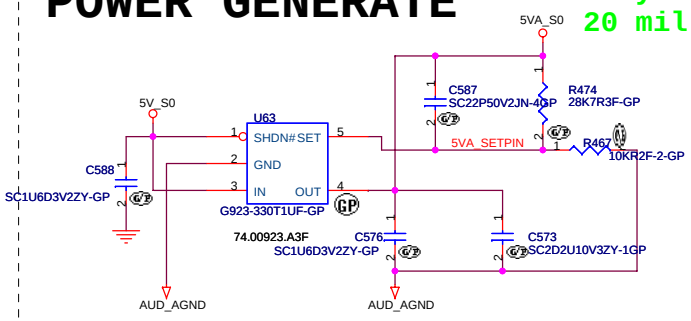
1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

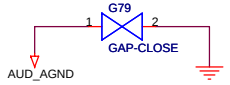
Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	*Symbol*	*Location*	*Re-tasking*
35/36	*FRONT*	*AMP,Jack1*	AMP output, line input
39/41	*SURR*	*X*	X
43/44	*CEN/LEFT*	*X*	SURR-VREFO-L/R
45/46	*SIDESURR*	*X*	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	*LINE1*	*Jack 2*	Line input, line output
21/22	*MIC1*	*Jack 3*	Mic input, line output
14/15	*LINE2*	*X*	X
16/17	*MIC2*	*Int. Mic*	Mic input

POWER GENERATE

Layout 20 mil





<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC883***	
Size A3	Document Number **Garda-5**	Rev **SB**
Date: Wednesday, April 26, 2006	Sheet 30 of 46	

AUDIO OP AMPLIFIER

I/P signal level need +5V level

Internal Speaker

SPKR_L-, SPKR_L+, SPKR_R-, SPKR_R+

SPKR1 ACES-CON4-1-GP

20.D0197.104

SRC100P50V-2-GP ERC2

2nd source: 20.F0760.004

EXT MIC IN

MICIN_JD#, MIC_IN_R, MIC_IN_L

R458, R459 0R2J-2-GP MIC_IN_R_1, MIC_IN_L_1

EC84 SC100P50V3JN-2GP, EC85 SC100P50V3JN-2GP, EC86 SC100P50V2JN-3GP

MIC2 PHONE-JK233-GP

22.10133.B01

LINE OUT

SB Modify

LINEOUT_JD=lOW after PLUG-IN

LINE_OUT_R_AMP, LINE_OUT_L_AMP

R447, R448 33R2J-2-GP

-1 Modify

LINEOUT_JD# → LINEOUT_JD#, LINE_OUT_R_AMP_1, LINE_OUT_L_AMP_1

RN65 SRN1KJ-7-GP

C555 SC680P50V2KX-2GP, C556 SC680P50V2KX-2GP, EC80 SC100P50V2JN-3GP

LOUT1 PHONE-JK235-GP

22.10133.B21

2ndsource: 22.10251.321

When has SPDIF replace to "22.10205.251".

LINE IN

LINEIN_JD#, LINE_IN_R, LINE_IN_L

R454, R455 0R2J-2-GP AUD_LINE_R, AUD_LINE_L

RN64 SRN10KJ-5-GP

EC83 SC100P50V2JN-3GP, EC82 SC100P50V2JN-3GP, EC81 SC100P50V2JN-3GP

PHONE-JK234-GP LIN1

22.10133.B11

Key components

U62 G1432Q5U-GP 74.01432.013

U60 MAX4411ETP-1-GP 74.04411.A13

L30 FCM1608KF-2-GP-U 68.00217.171

D37 BAV99PT-GP-U, D36 BAT54WCPT-GP

Q29 CH3906PT-GP

AG1-910-02

SB Modify / SA Modify / -1 Modify

SB Modify: R466 0R2J-2-GP, R464 100KR2J-1-GP DY

SA Modify: R465 7K5R2J-GP, R460 7K5R2J-GP

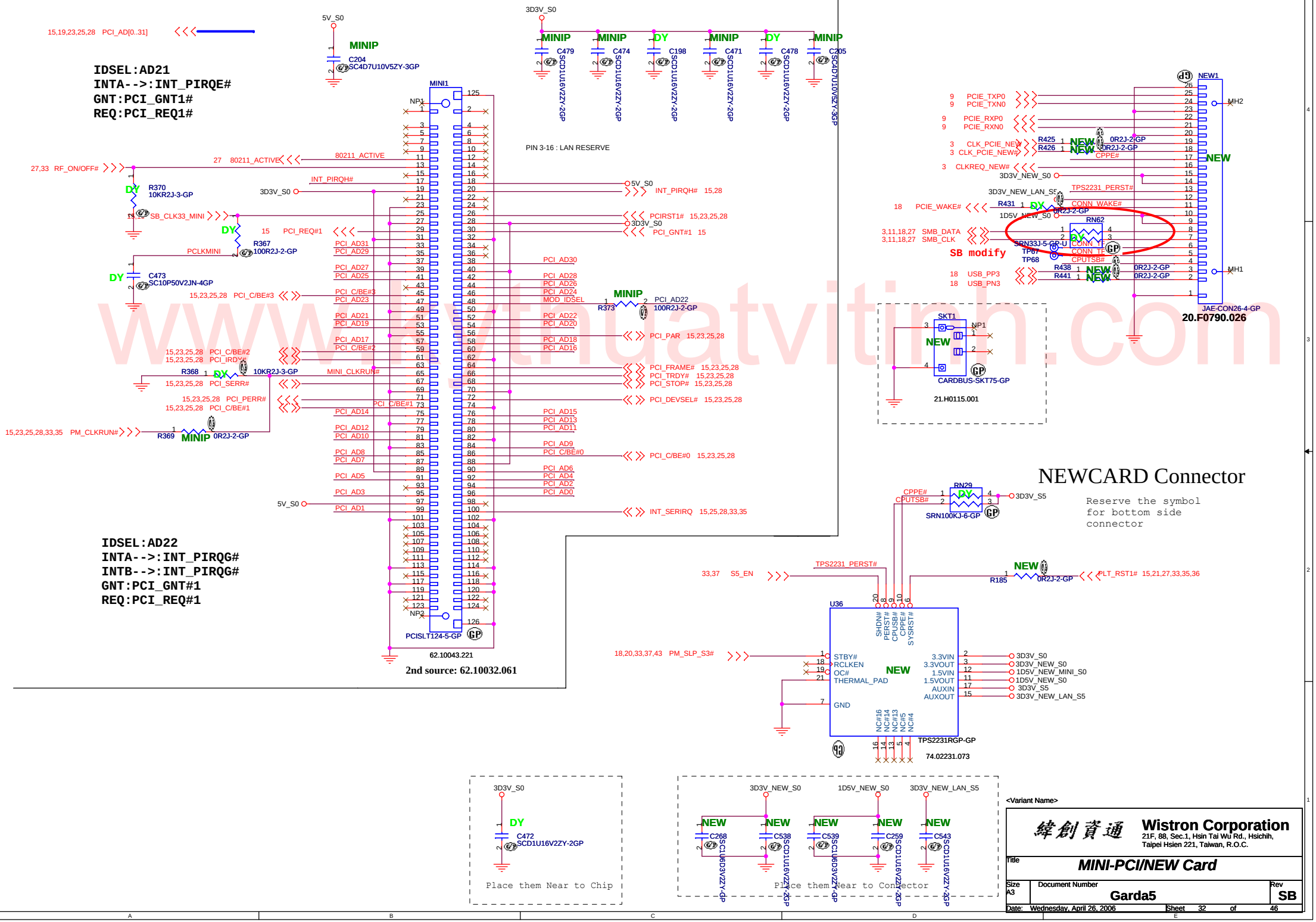
-1 Modify: R493, R494 10KR2J-3-GP; R496, R495 1KR2J-1-GP

0.11 * 1.5 =0.165

SB Modify: R484 100KR2J-1-GP, R483 1KR2J-1-GP, R444 100KR2J-1-GP

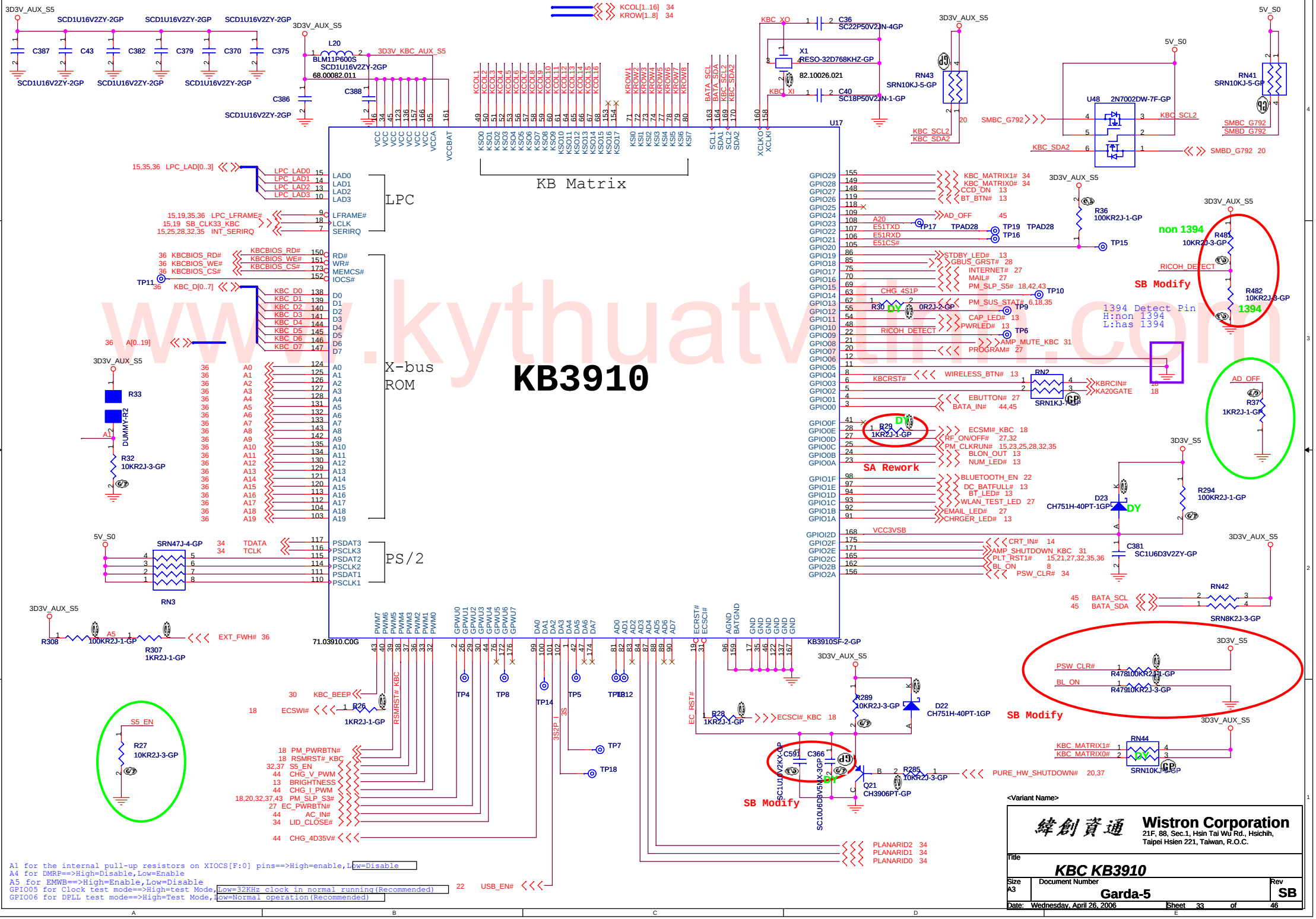
SB Modify FAE recommend: MAX4411_PVSS, C545 SC1U10V2KX-GP

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	AUDIO AMP AND JACK		
Size A3	Document Number Garda-5	Rev -1	
Date: Wednesday, April 26, 2006	Sheet 31 of 46		

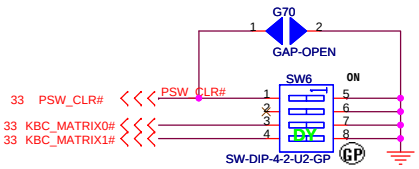


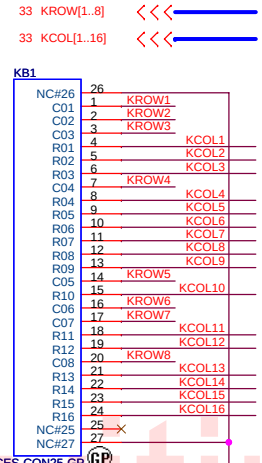
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>
Title: MINI-PCI/NEW Card
Size: A3
Document Number: Garda5
Rev: SB
Date: Wednesday, April 26, 2006
Sheet 32 of 46



Internal KeyBoard Connector



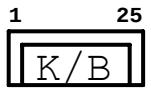


2nd source: 20.K0198.025

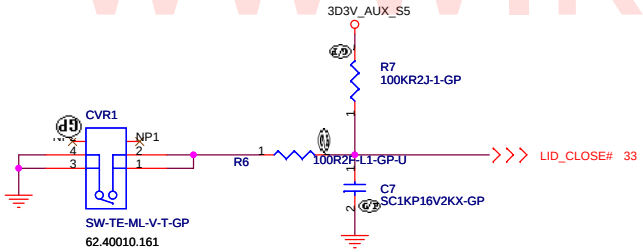
Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

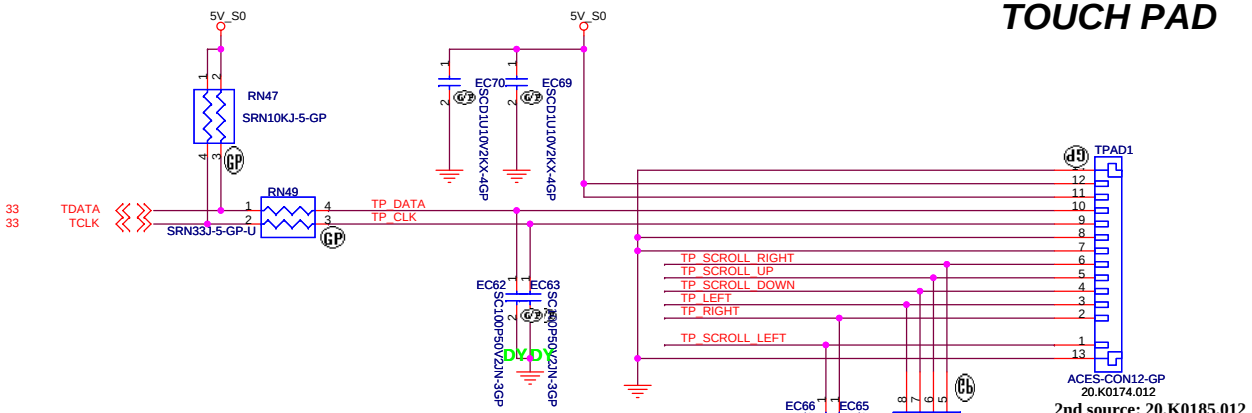
	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON



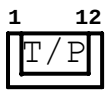
COVER SWITCH



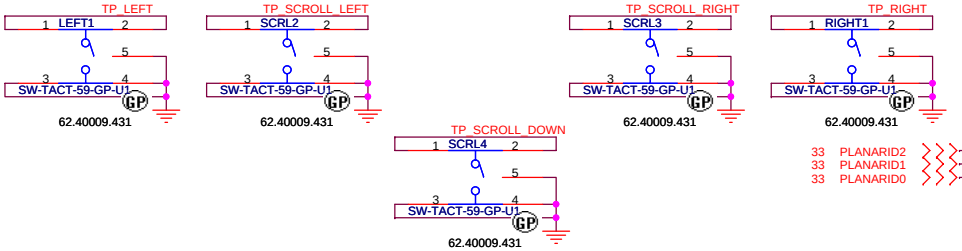
TOUCH PAD

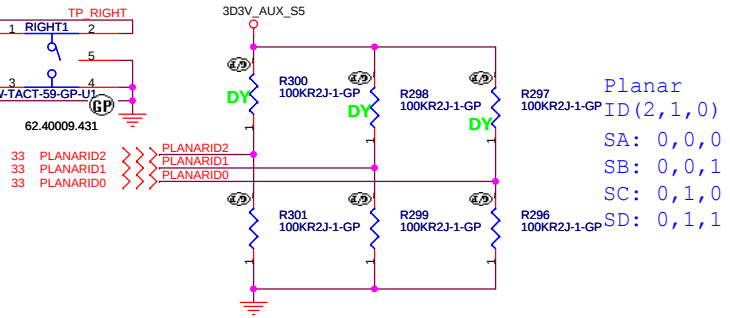


2nd source: 20.K0185.012



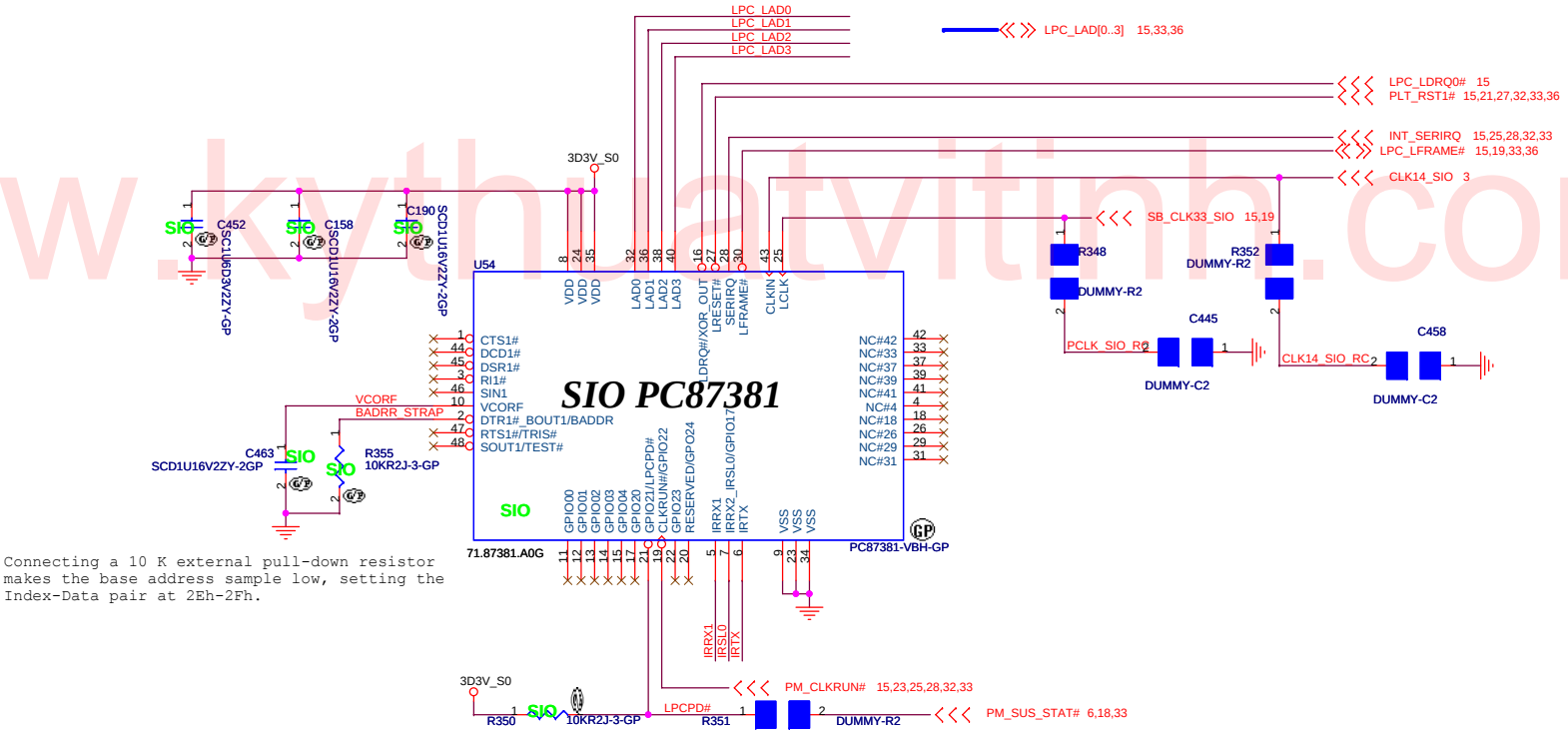
SCROLL KEY





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: KEYBOARD/TOUCHPAD		
Size: A3	Document Number: Garda-5	Rev: SA
Date: Wednesday, April 26, 2006	Sheet 34 of 46	

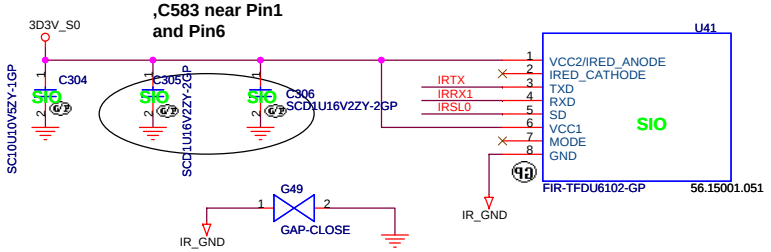


Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

VISHAY FIR/CIR Module

Place C581 ,C583 near Pin1 and Pin6

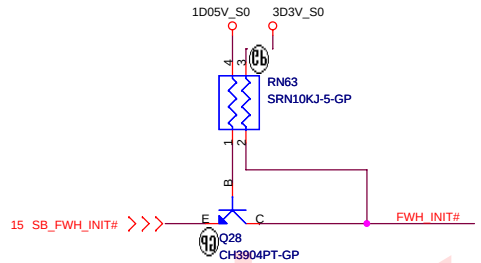
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

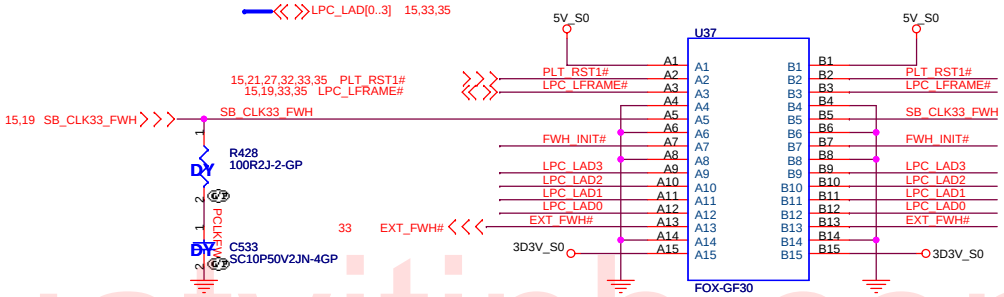


<Variant Name>

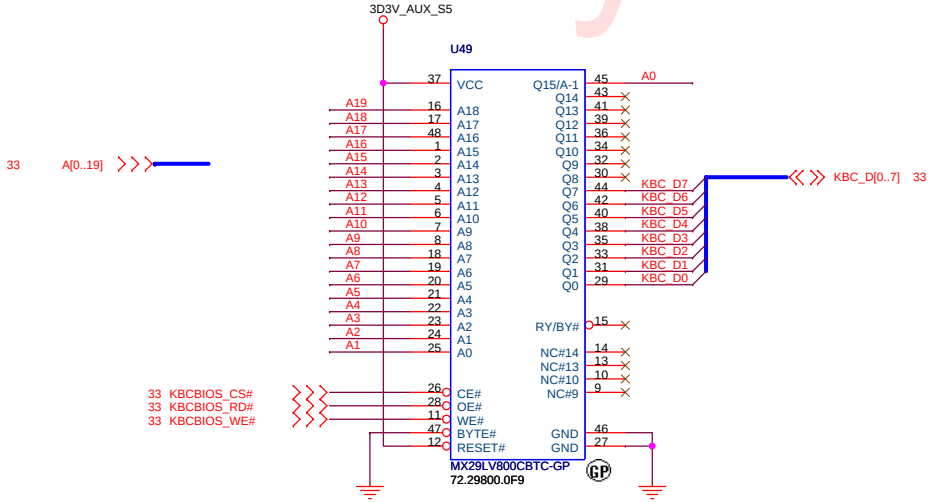
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***SIO 87381 / FIR***
Size A3	Document Number: **Garda-5**
Rev	**SA**
Date: Wednesday, April 26, 2006	Sheet 35 of 46

GOLDEN FINGER FOR DEBUG BOARD





Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

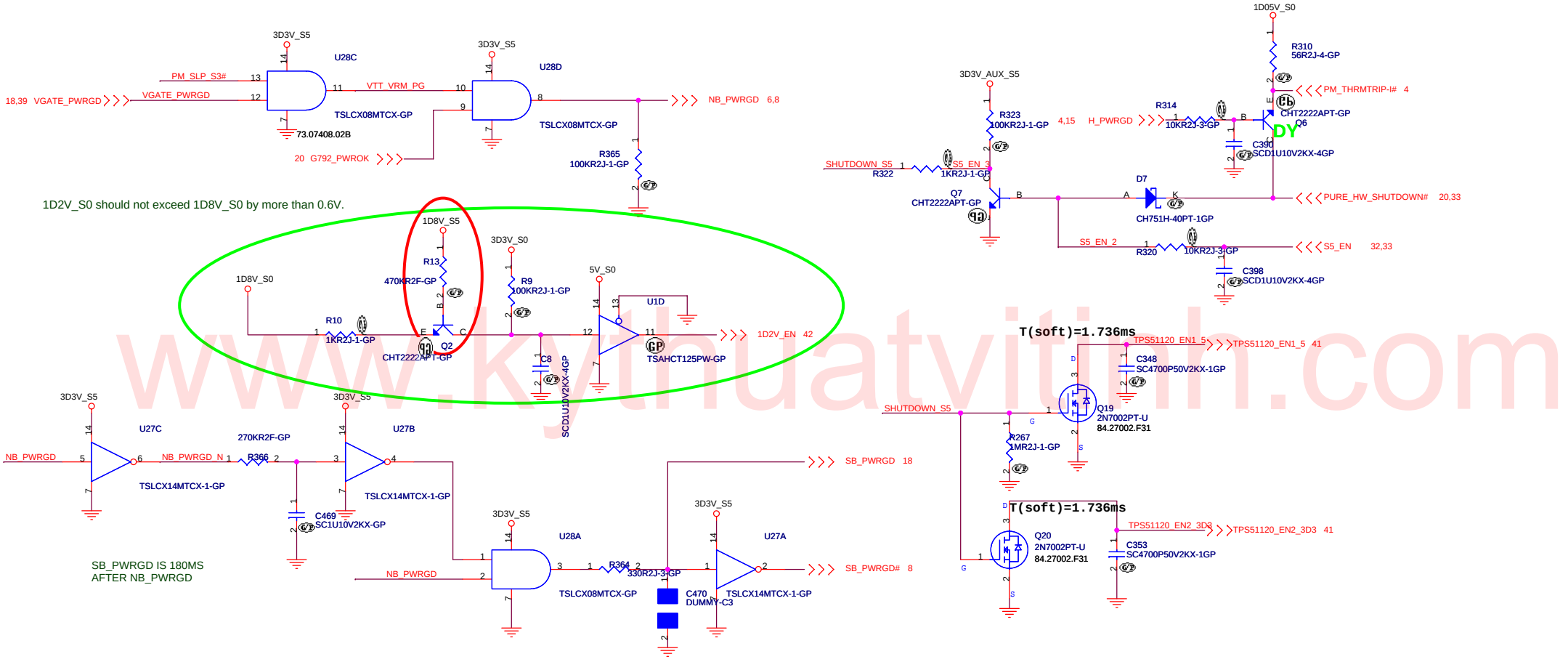
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

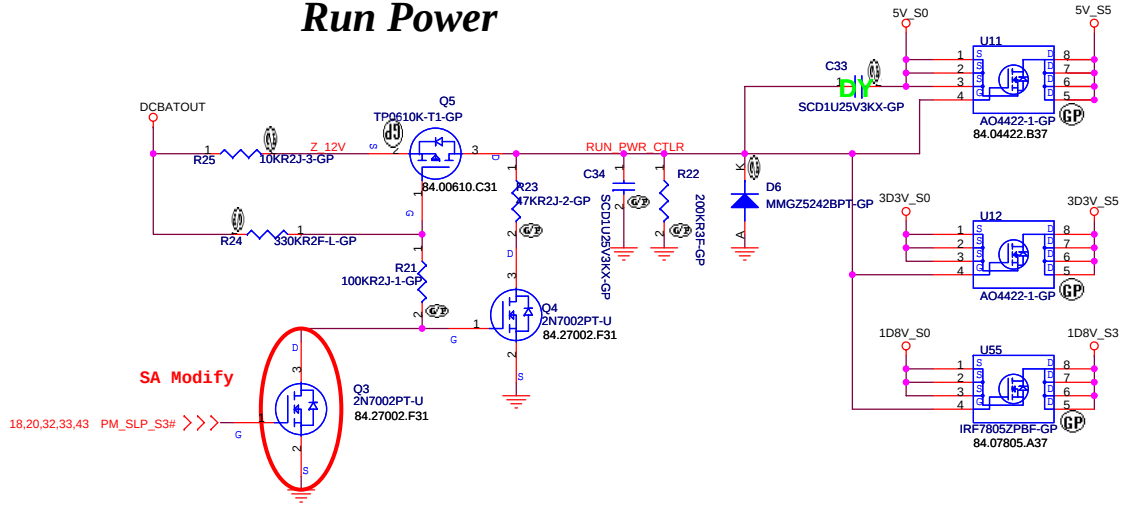
Title: ***BIOS ROM***

Size	Document Number	Rev
A3	Garda-5	SA

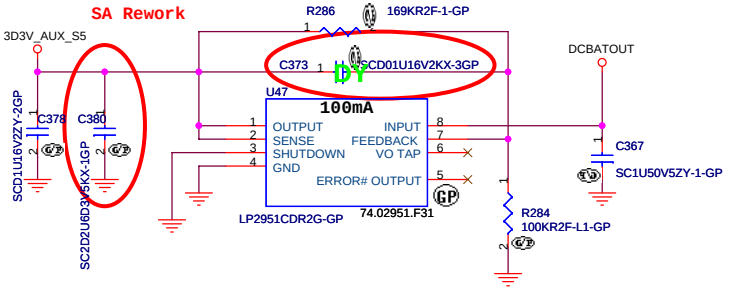
Date: Wednesday, April 26, 2006 Sheet 36 of 46



Run Power



Aux Power



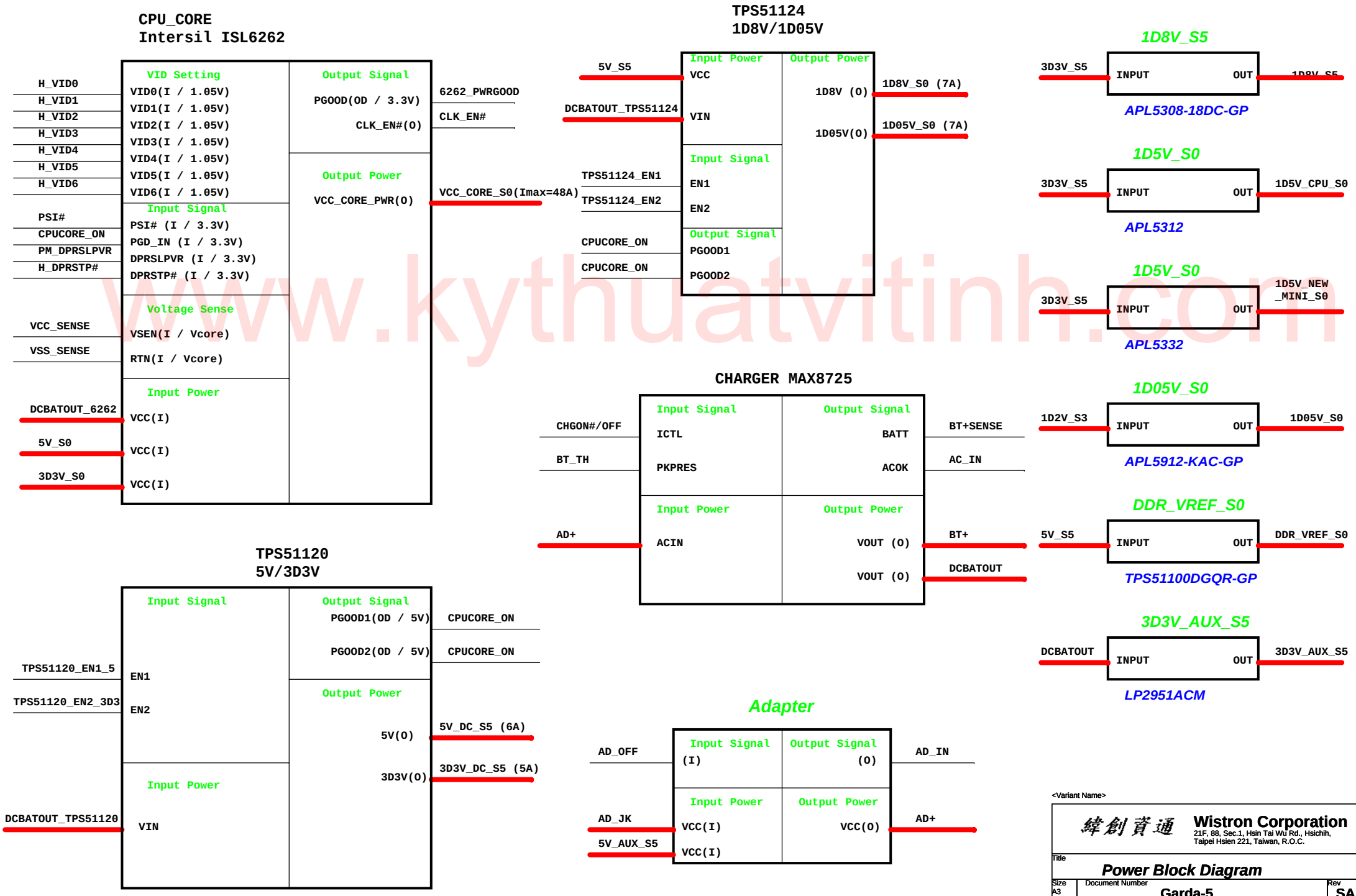
<Variant Name>

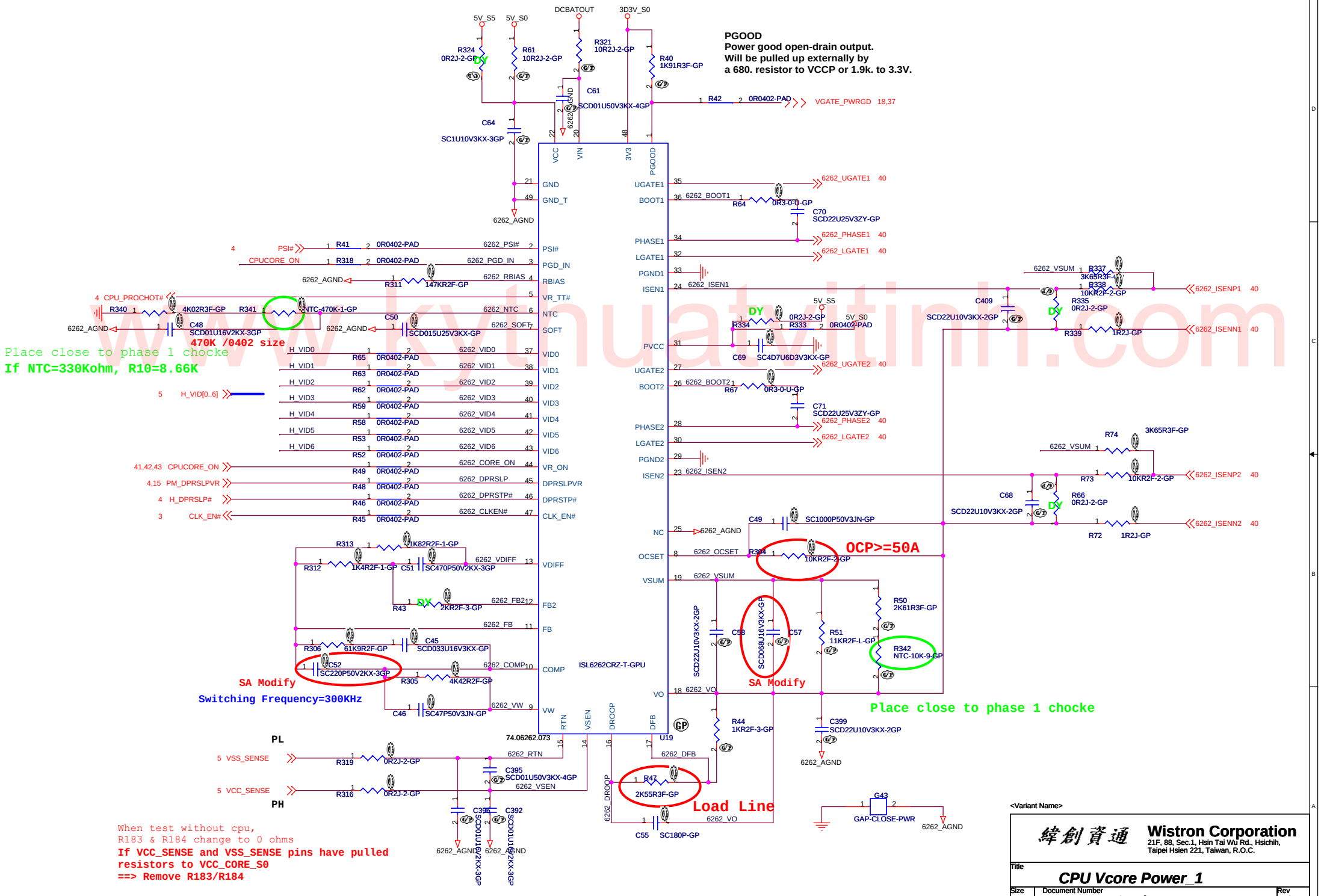
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

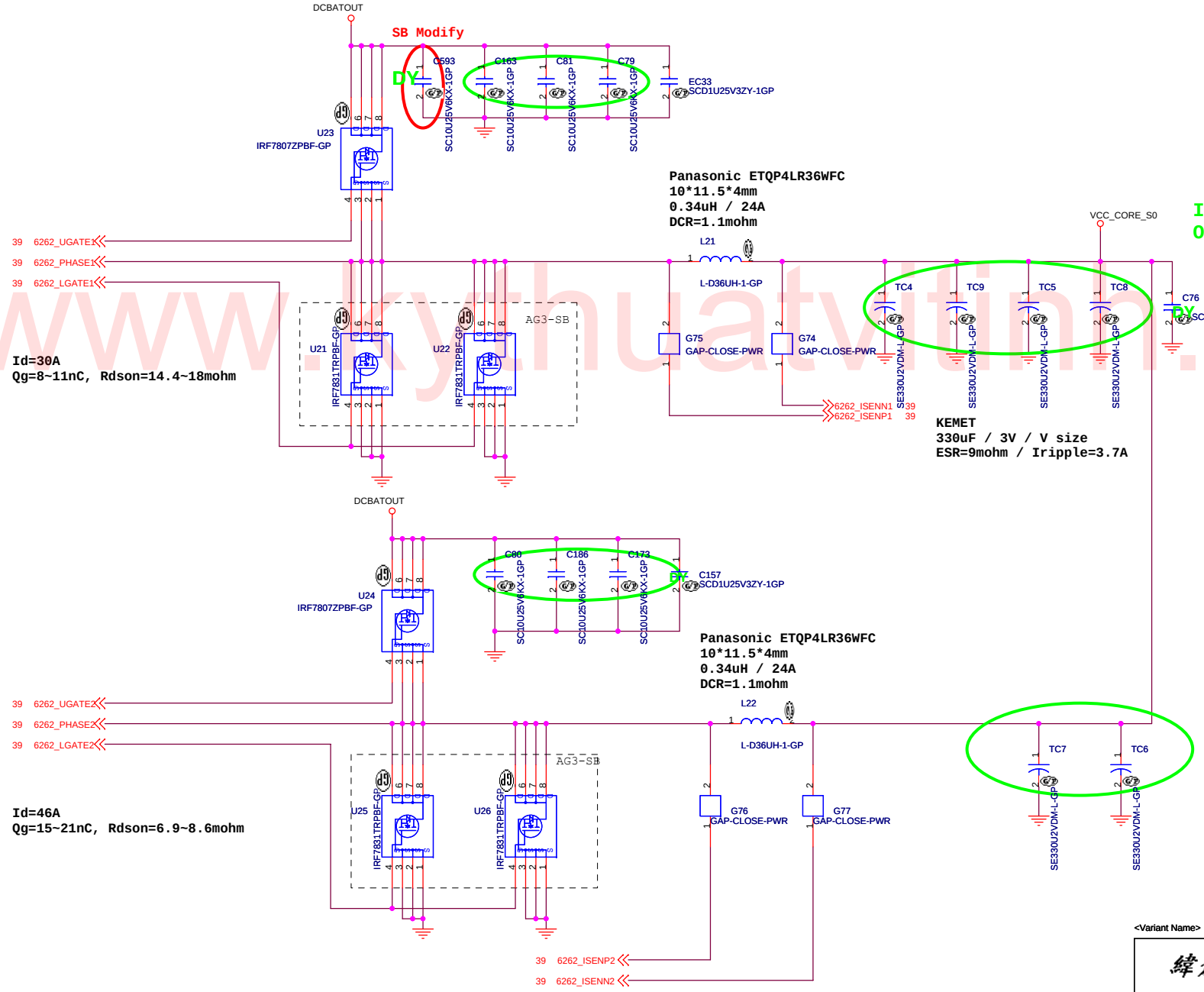
Title: **RUN and AUX POWER**

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 37 of 46







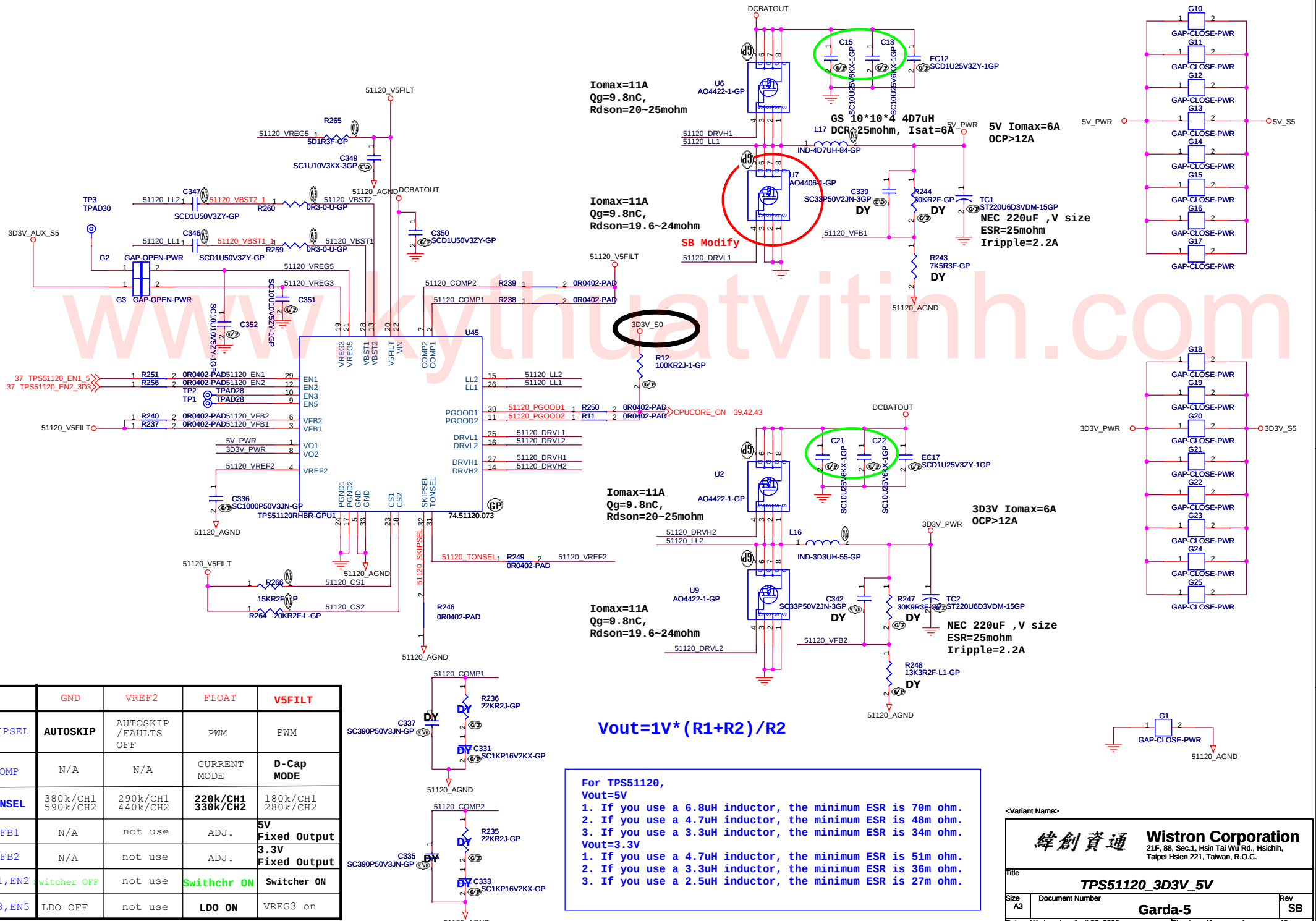
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_2/2

Size	Document Number	Rev
A3	Garda-5	SB

Date: Wednesday, April 26, 2006 Sheet 40 of 46



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

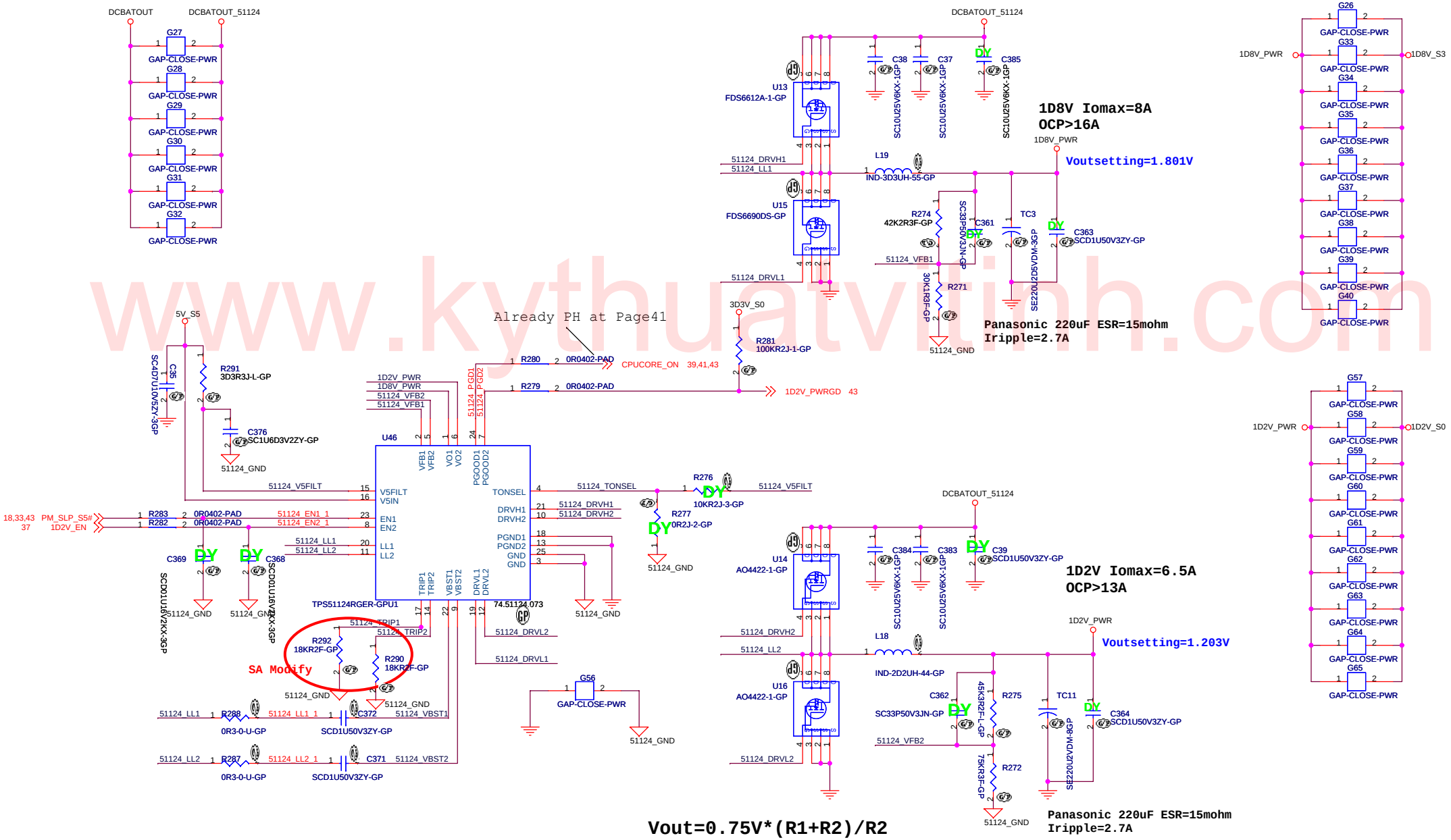
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51120_3D3V_5V***

Size: A3 | Document Number: **Garda-5** | Rev: SB

Date: Wednesday, April 26, 2006 | Sheet 41 of 46



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

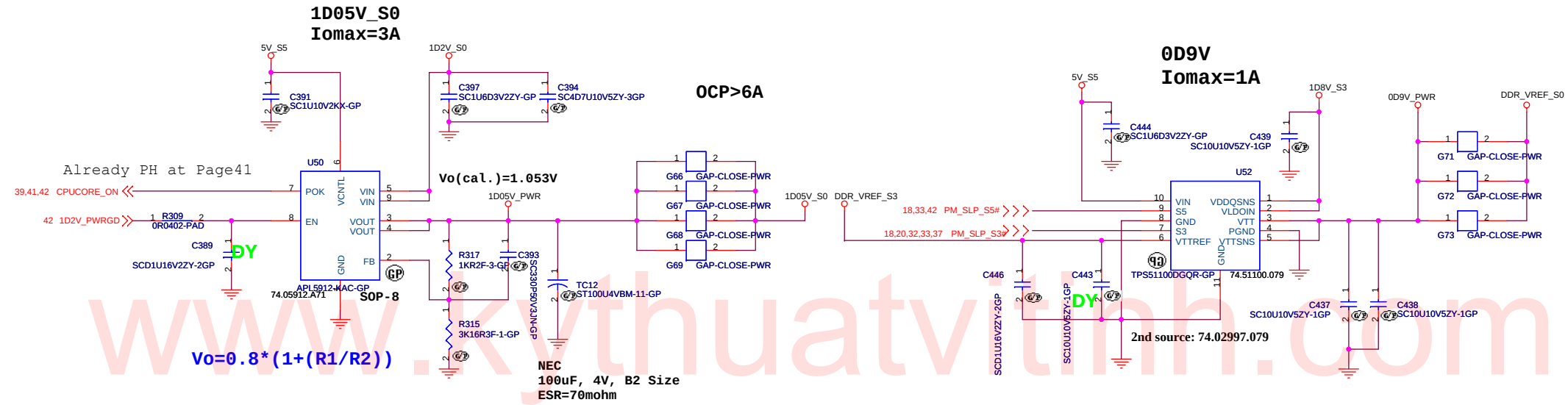
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

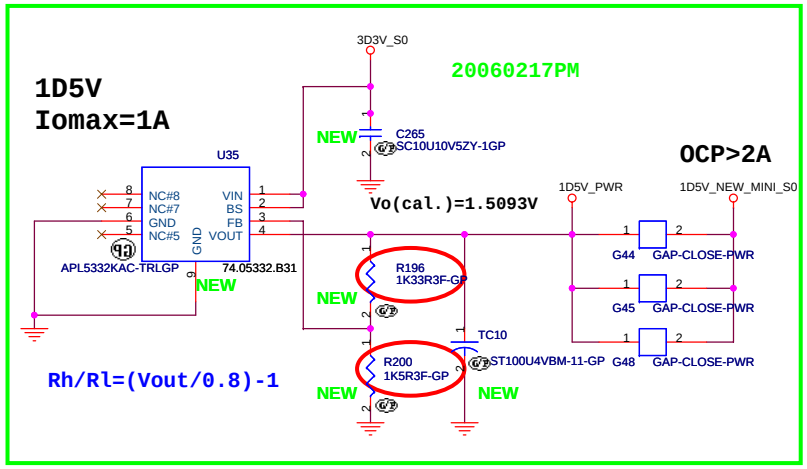
Title: TPS51124_1D8V_1D2V

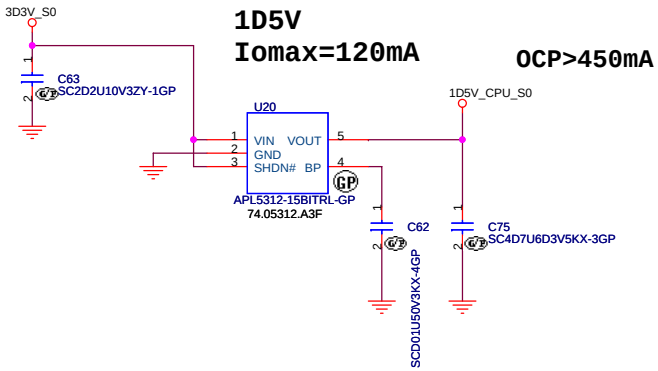
Size	Document Number	Rev
A3	Garda-5	SA

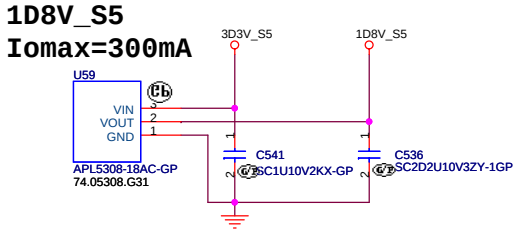
Date: Wednesday, April 26, 2006 Sheet 42 of 46



For New Card/MINI Card solution







<Variant Name>

緯創資通 **Wistron Corporation**
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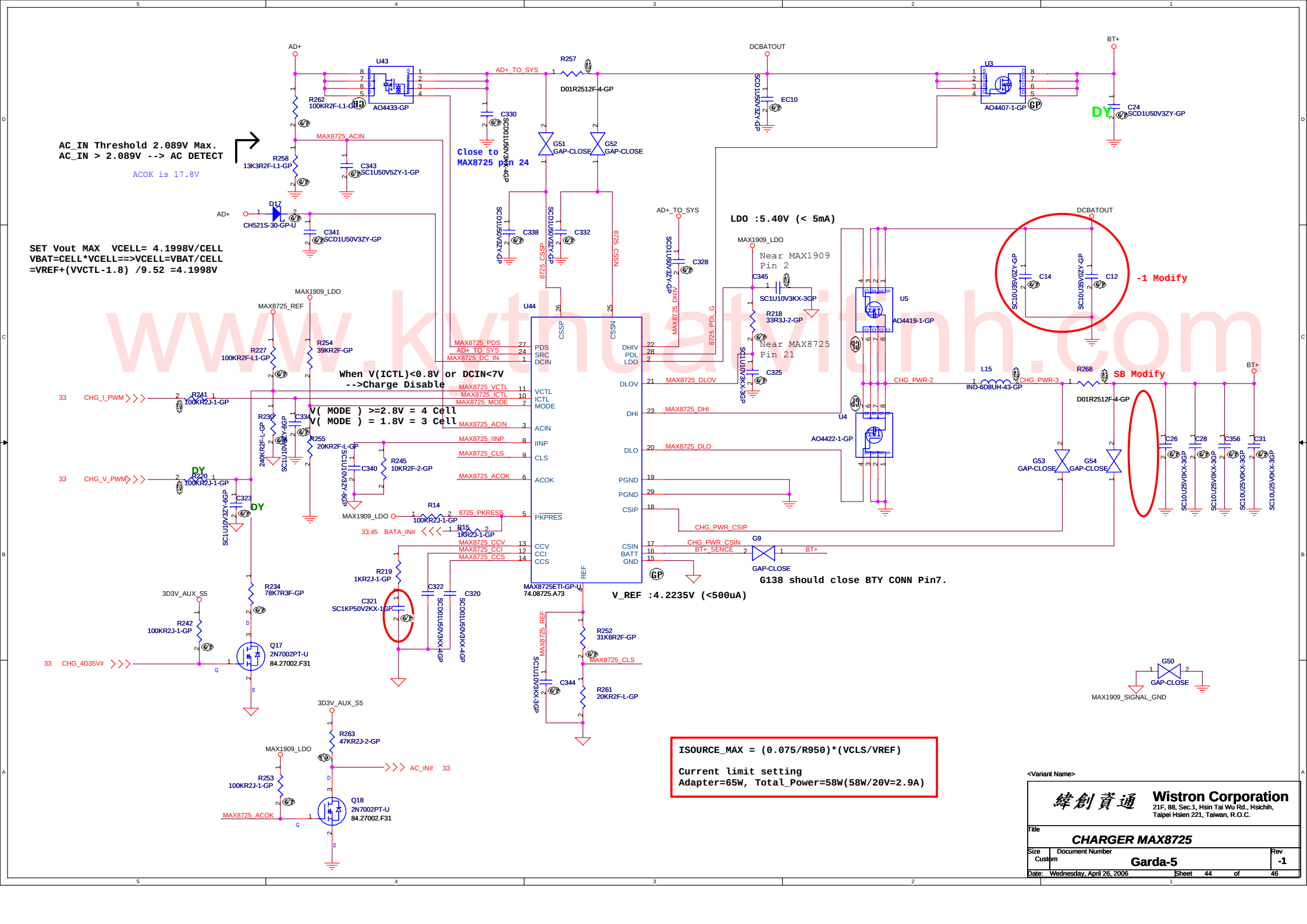
Taipei Hsien 221, Taiwan, R.O.C.

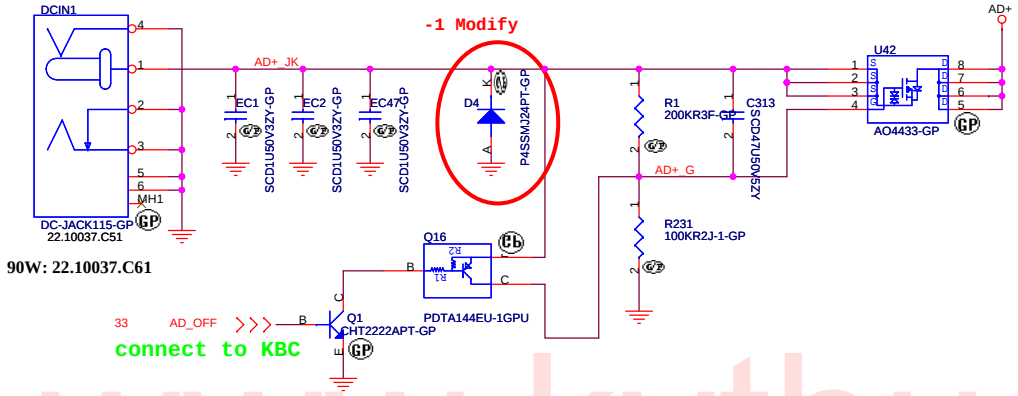
Title: *1D5V/0D9V/1D05V/1D8V*

Size	Document Number	Rev
A3	Garda-5	SA

Date: Wednesday, April 26, 2006 Sheet 43 of 46

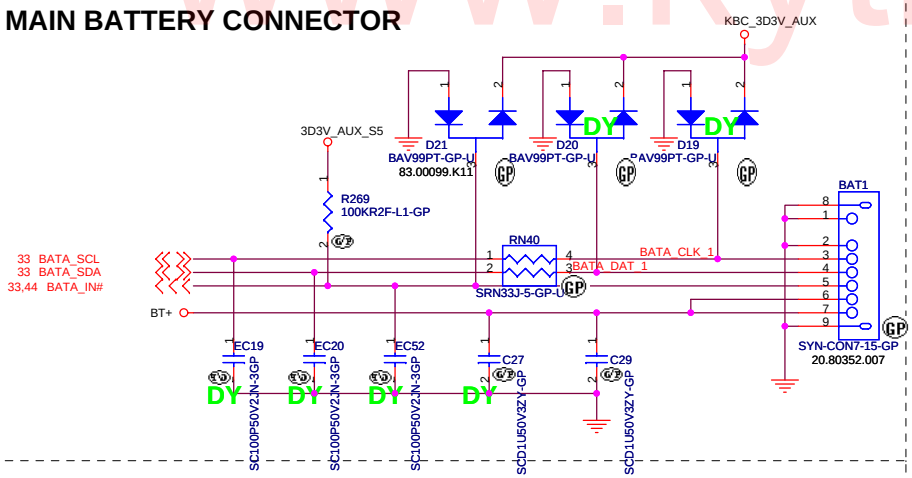

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
Close to MAX8725 pin 24
LDO :5.40V (< 5mA)
V_REF :4.2235V (<500uA)
G138 should close BTY CONN Pin7.
-1 Modify
SB Modify
ISOURCE_MAX = (0.075/R950)*(VCLS/VREF)
Current limit setting
Adapter=65W, Total_Power=58W(58W/20V=2.9A)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725
Garda-5
Wednesday, April 26, 2006
44
46

ADAPTER IN CIRCUIT



90W: 22.10037.C61

MAIN BATTERY CONNECTOR



<Variant Name>

緯創資通 **Wistron Corporation**
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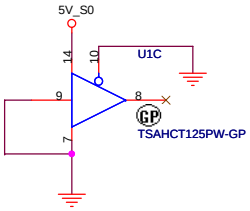
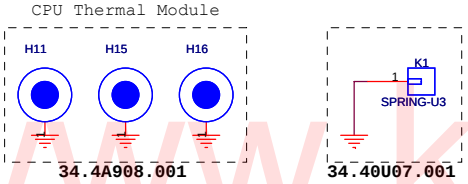
Taipei Hsien 221, Taiwan, R.O.C.

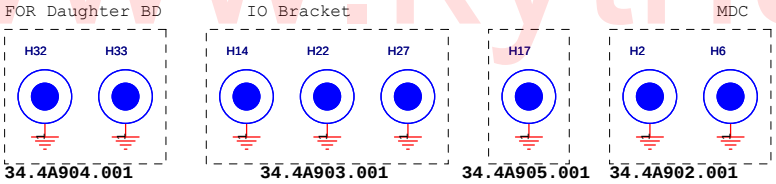
Title	***AD/BATT CONN***	
Size: A3	Document Number: **Garda-5**	Rev: **-1**
Date: Wednesday, April 26, 2006	Sheet 45 of 46	

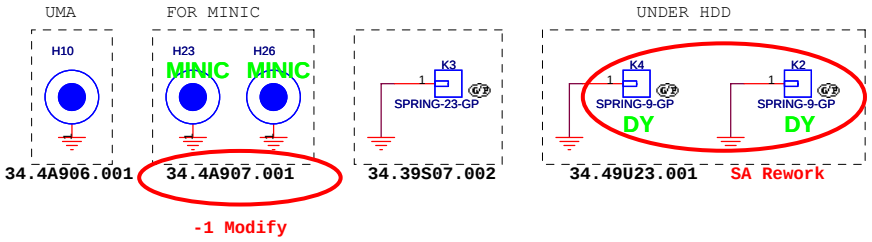


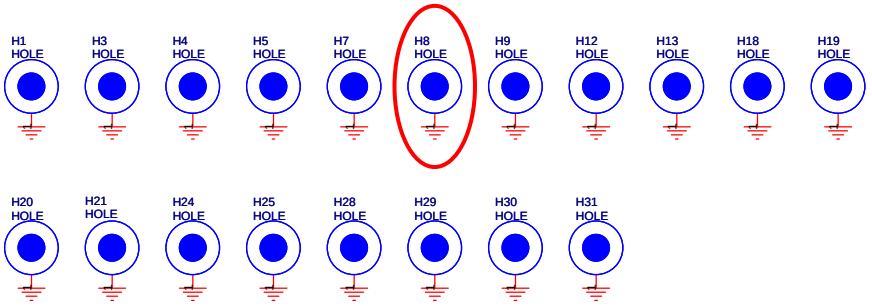
TOP SIDE:

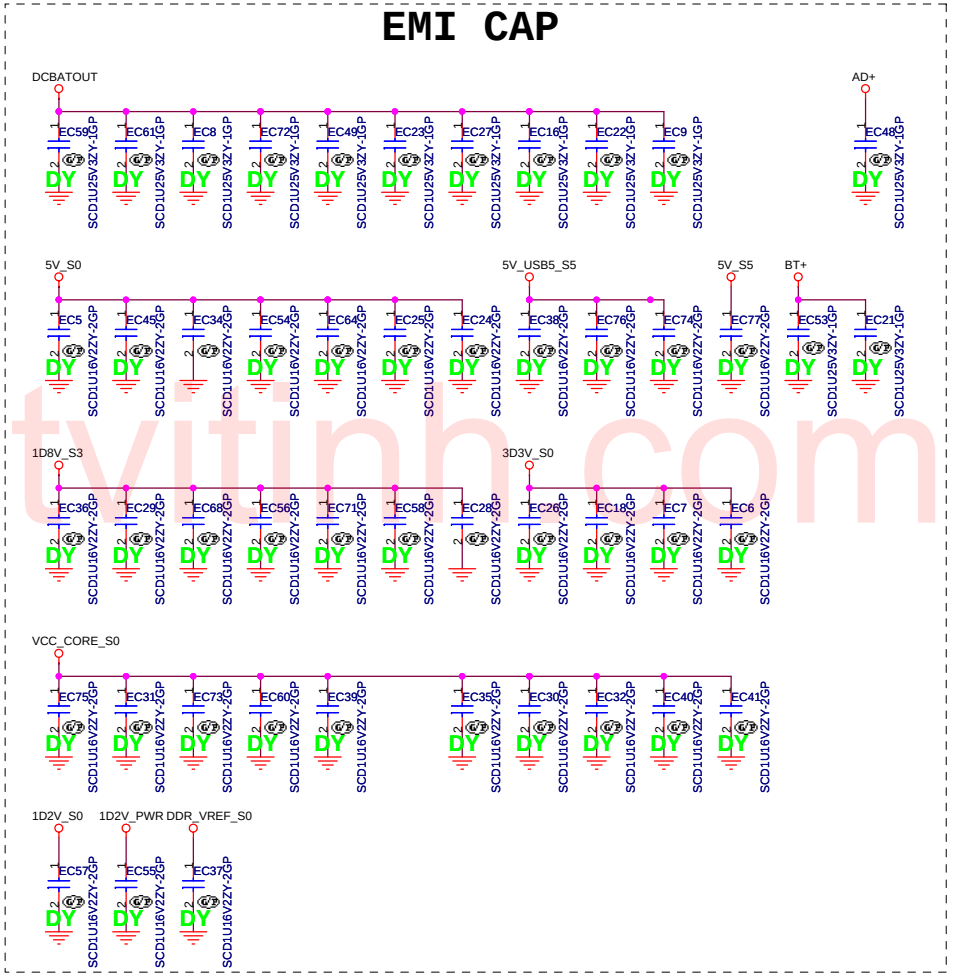


BOTTOM SIDE:









<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPRING & BOSS***

Size	Document Number	Rev
A3	Garda-5	-1

Date: Wednesday, April 26, 2006 Sheet 46 of 46