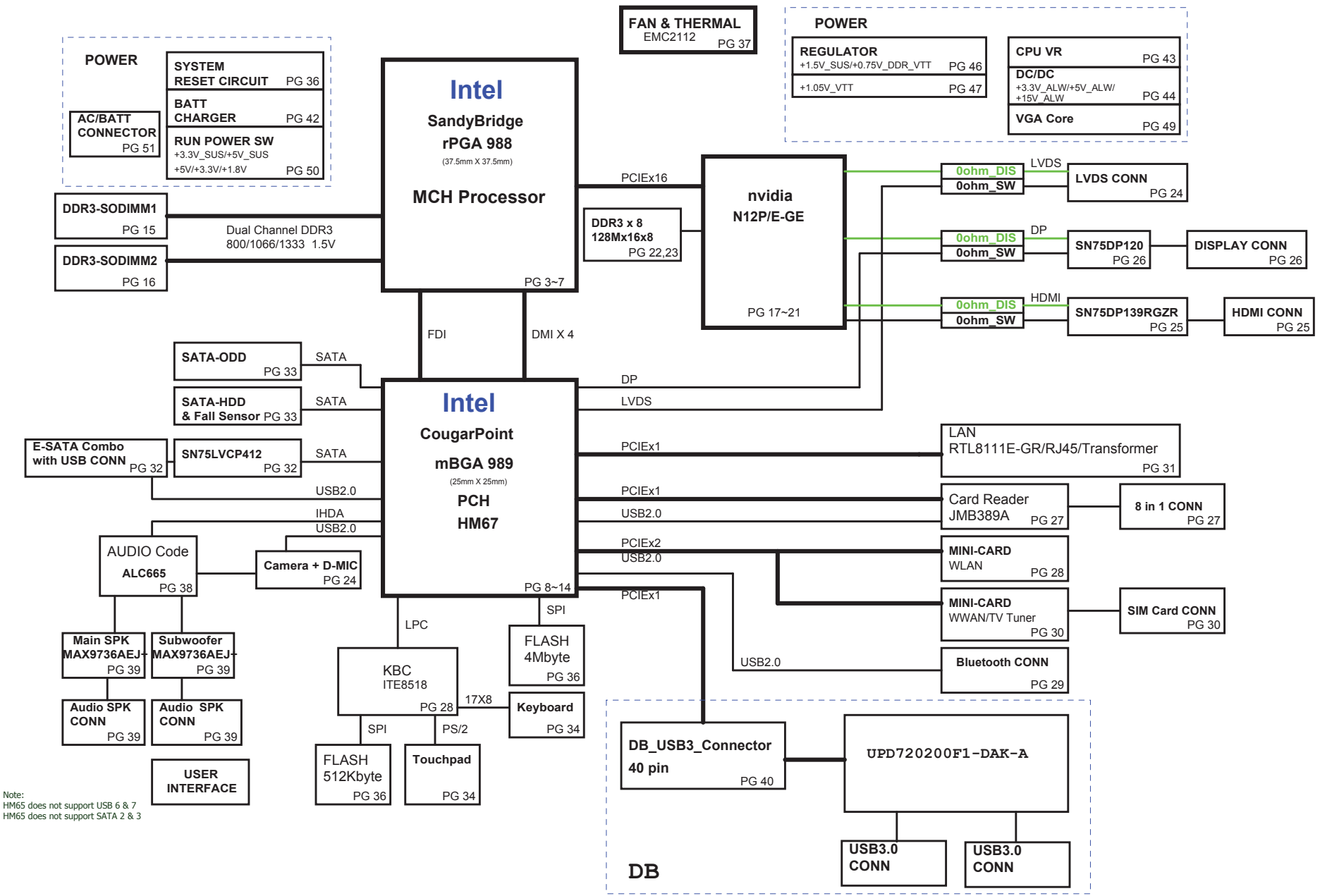
_DIS ==> Discrete Only
_SW ==> Optimus Only
_UMA ==> UMA Only

GM6C MLK Optimus, Discrete & UMA

VER : 1A
PWA:
PWB:



Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: Block Diagram | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 1 of 59

Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
⏚ GND	ALL	

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

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	Frontage	1A

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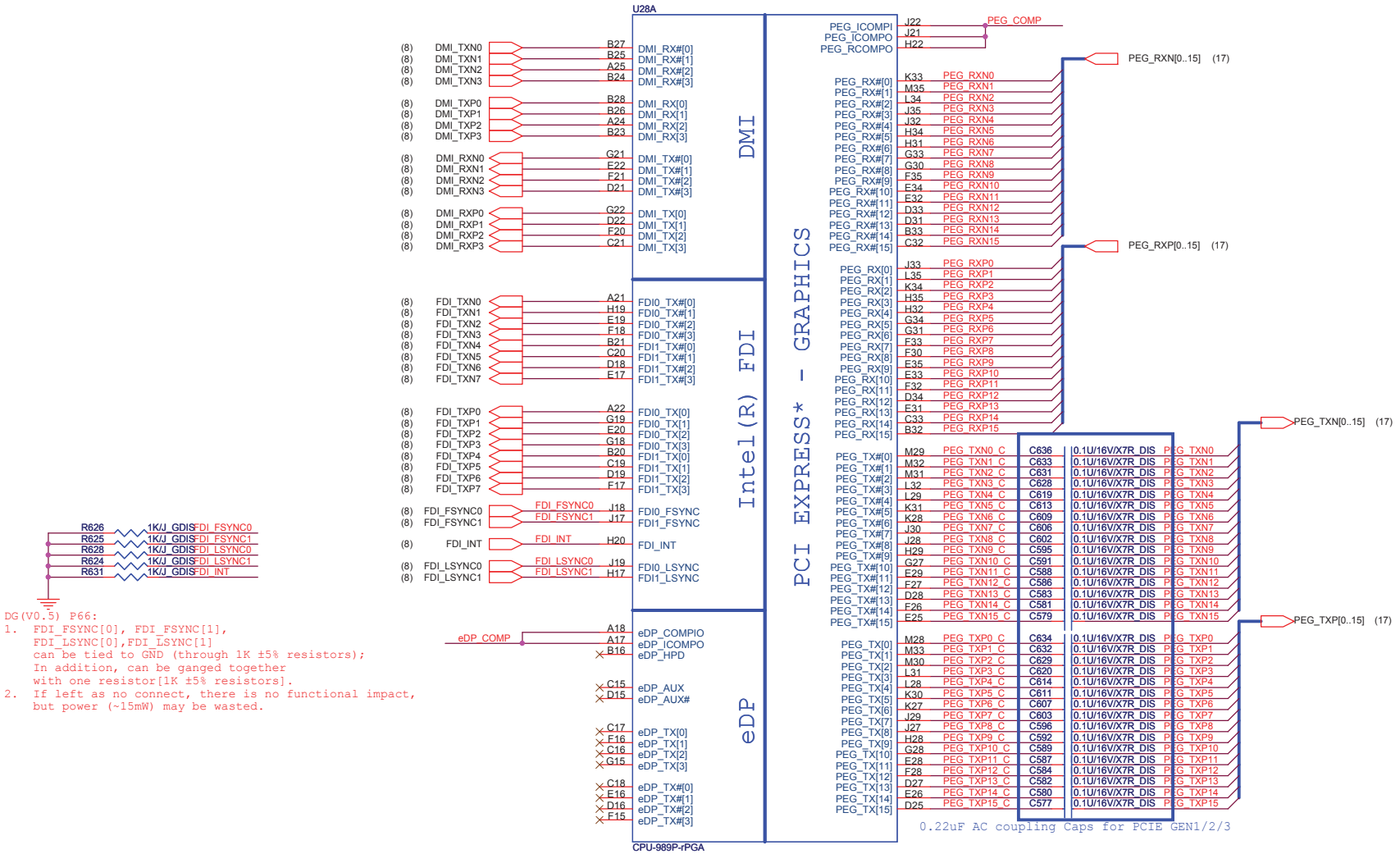
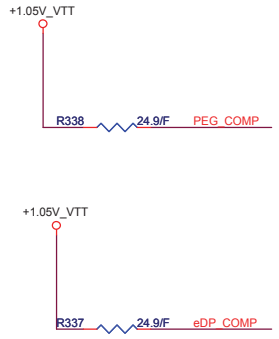
Sandy Bridge Processor (DMI,PEG,FDI)



DG(V0.5) P66:
1. FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be tied to GND (through 1K ±5% resistors); In addition, can be ganged together with one resistor[1K ±5% resistors].
2. If left as no connect, there is no functional impact, but power (~15mW) may be wasted.

DP & PEG Compensation



Quanta Computer Inc.		
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Sandy Bridge Processor (CLK,MISC,JTAG)

WW31.MOW Page 5 (SNB_IVB# N.A at SNB EDS #27637 0.7v1)

U28B

MISC: PROC_SELECT#, SKTOCC#

THERMAL: CATERR#, PECI, PROCHOT#, THERMTRIP#

PWR MANAGEMENT: PM_SYNC, UNCOREPWRGOOD, SM_DRAMPWROK, RESET#

CLOCKS: BCLK, BCLK#, DPLL_REF_CLK, DPLL_REF_CLK#

DDR3 MISC: SM_DRAMRST#, SM_RCOMP[0], SM_RCOMP[1], SM_RCOMP[2]

JTAG & BPM: PRDY#, PREQ#, TCK, TMS, TRST#, TDI, TDO, DBR#, BPM#[0:7]

CPU-989P-rPGA

TP19 H_SNB_IVB# C26 PROC_SELECT#

(28) H_CPUDET# AN34 SKTOCC#

TP21 TP_CATERR# AL33 CATERR#

(28) EC_PECI R352 43/J H_PECI AN33 PECI

(28,42,43) VR_HOT# R358 56/J H_PROCHOT# AL32 PROCHOT#

shut down when asserted

Over 130 degree C will drive low

(12) H_THERM# AN32 THERMTRIP#

provide power management status (form PCH to CPU)

(8) PM_SYNC R372 *0/J_short_NC PM_SYNC_R AM34 PM_SYNC

(12) H_PWRGOOD R373 *0/J_short_NC PWRGOOD_R AP33 UNCOREPWRGOOD

R374 10K/J

PM_DRAM_PWRGD_R V8 SM_DRAMPWROK

+1.05V_VTT R368 *75/J_NC

CPU_PLTRST# R359 *43/J_NC CPU_PLTRST#_R AR33 RESET#

BCLK A28, BCLK# A27 → CLK_CPU_BCLKP (10), CLK_CPU_BCLKN (10) DMI clock

DPLL_REF_CLK A16, DPLL_REF_CLK# A15 → CLK_DPLL_SSCLKP_R, CLK_DPLL_SSCLKN_R

R629 Ra *0_NC

R627 Rb 1K/J

R630 Rc 1K/J

+1.05V_VTT

CLK_DPLL_SSCLKP (10), CLK_DPLL_SSCLKN (10) eDP clock

	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

SM_DRAMRST# R8 CPU_DRAMRST# **S3 Power reduce**

SM_RCOMP[0] AK1 SM_RCOMP_0 R322 140/F

SM_RCOMP[1] A5 SM_RCOMP_1 R312 25.5/F

SM_RCOMP[2] A4 SM_RCOMP_2 R313 200/F

26.1 change to 25 ohm

PRDY# AP29, PREQ# AP27 XDP_PREQ# → T5

TCK AR26 XDP_TCLK, TMS AR27 XDP_TMS, TRST# AP30 XDP_TRST#

TDI AR28 XDP_TDI, TDO AP26 → T2

DBR# AL35 → T11

BPM#[0] AT28 → T3, BPM#[1] AR29 → T6, BPM#[2] AR30 → T7, BPM#[3] AT30 → T10, BPM#[4] AP32 → T9, BPM#[5] AR31 → T4, BPM#[6] AT31 → T12, BPM#[7] AR32 → T8

+1.05V_VTT

XDP_TMS R364 51/J

XDP_TDI R363 51/J

XDP_PREQ# R365 *51/J_NC

XDP_TCLK R341 51/J

XDP_TRST# R375 51/J

Option for Prochot# function

68 ohm for unused, 62 ohm for used

+1.05V_VTT

H_PROCHOT# R367 *68/J_NC

VR_HOT# R366 62/J

IN	OUT
L	L
H	High-Z

+3.3V_SUS

C414 *0.1U/16V/X7R_NC

U19 *74LVC1G07GW_NC

(11,17,27,28,29,30,31,40) PLTRST#

CPU_PLTRST#

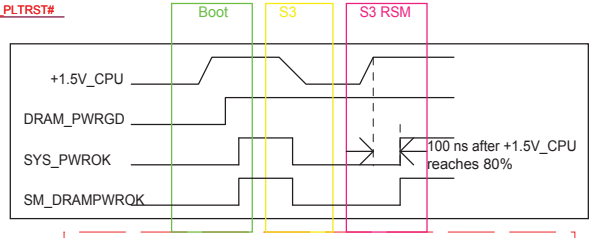
level shift for reset pin(07/12)

R714 1.5K/F

CPU_PLTRST#_R

R723 750/F

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	High-Z



+1.5V_SUS keep DDR3_DRAMRST# high to avoid CPU_DRAMRST# low when into S3 (Because can't reset DRAM when into S3)

3/16 Change topology; Add AND gate based on DG rev0.9

+3.3V_SUS

C574 0.1U/16V/X7R

R489 200/J

U27 74AHC1G09GW

(8) PM_DRAM_PWRGD

(8) SYS_PWROK

PM_DRAM_PWRGD_Q

+1.5V_SUS_CPU

02/25 Update R8232, R8233 value and routing, Add R8583 follow PDG 0.71 #440484

R613 200/F

R615 130/F PM_DRAM_PWRGD_R

R616 *39/J_NC

Q68 *2N7002K_NC

PS_S3CNTRL (6,8,15)

S3 Power reduce

+1.5V_SUS

R293 1K/J

Q33 BSS138-7-F

CPU_DRAMRST#

DDR3_DRAMRST#_R R289 1K/J → DDR3_DRAMRST# (15,16)

R701 1K/J +3.3V_SUS

DDR_HVREF_RST_PCH (10)

R299 4.99K/F

C237 0.047U/10V/X7R 10

Quanta Computer Inc.

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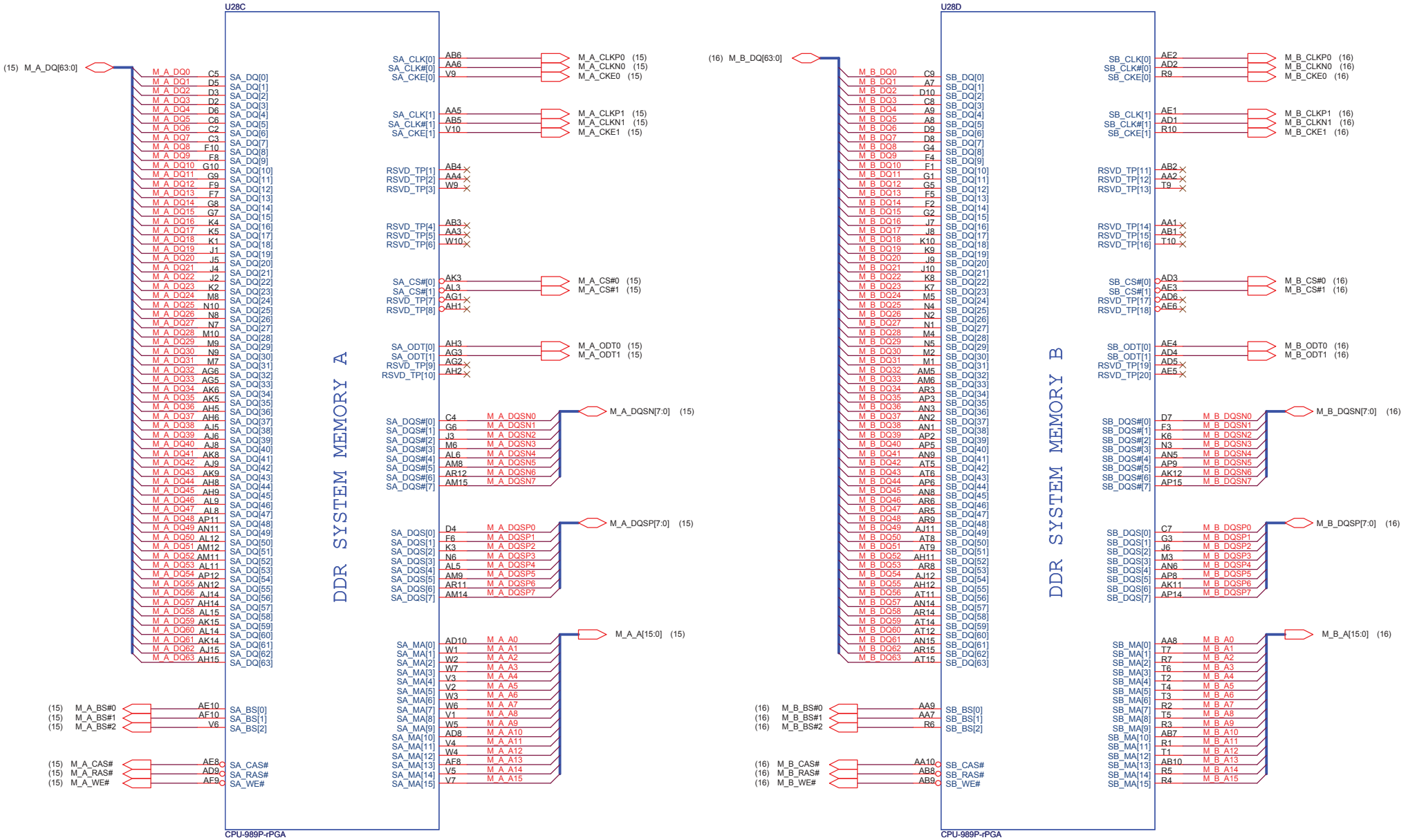
Sandy Bridge Processor (DDR3)



Quanta Computer Inc.

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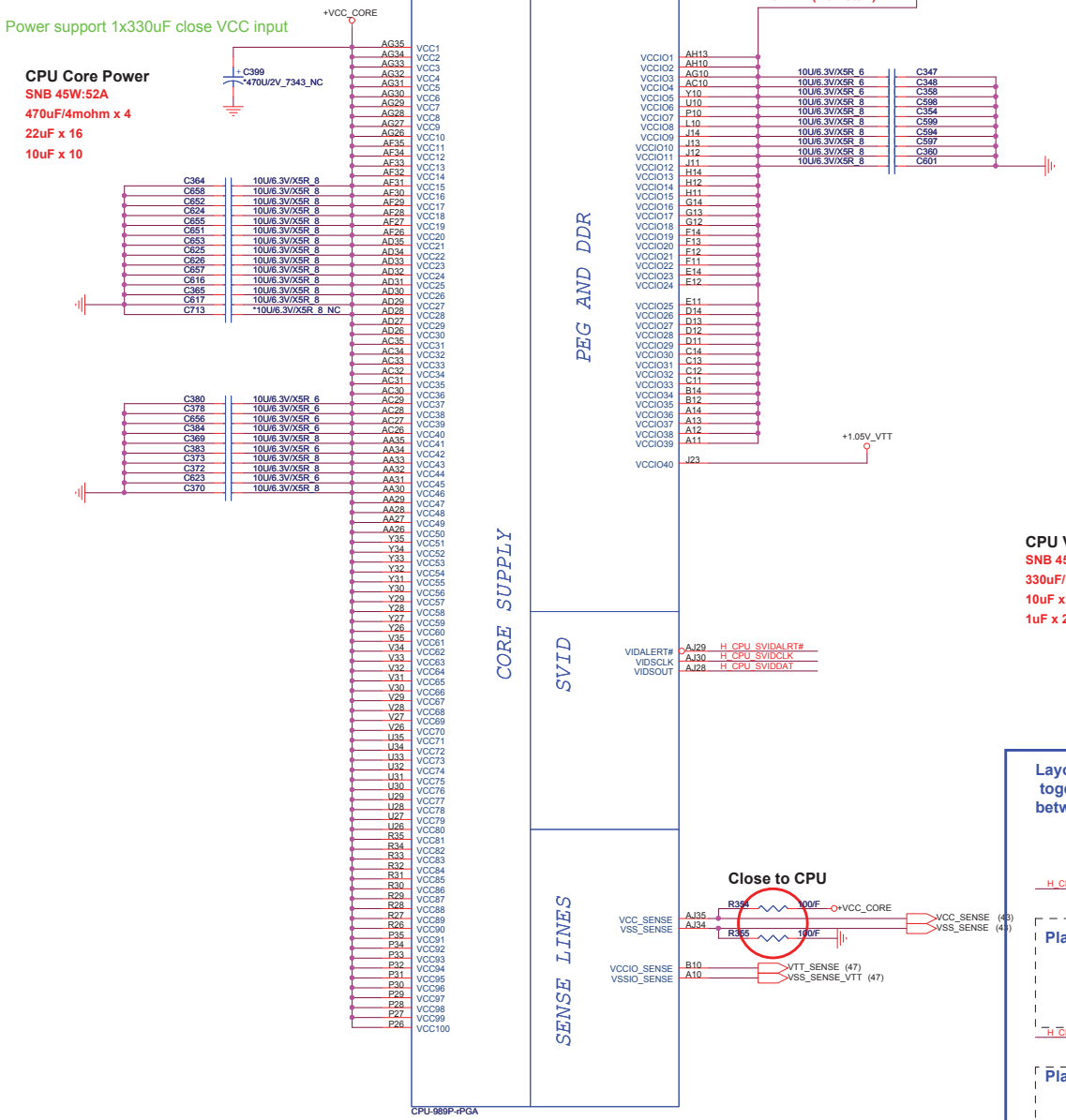
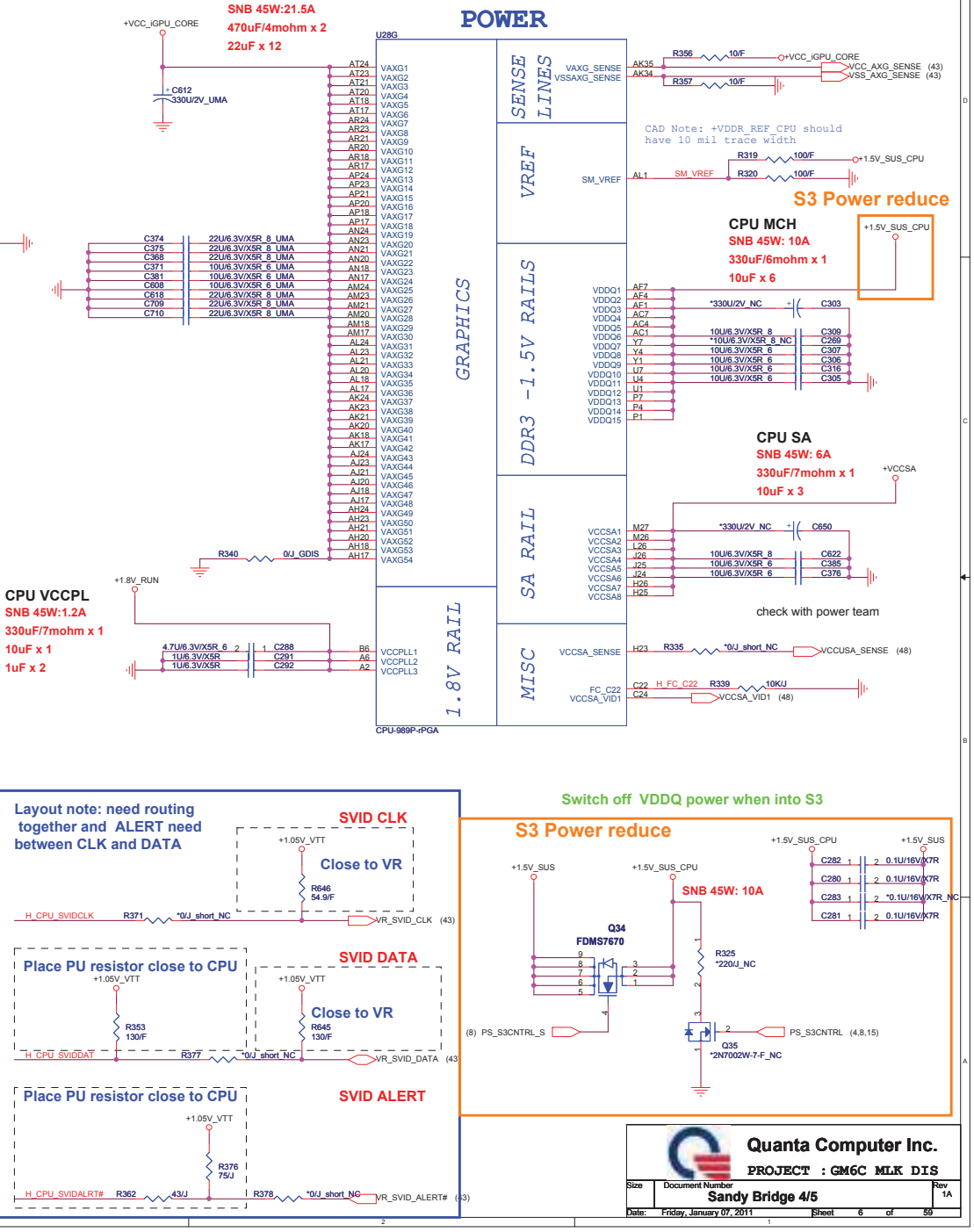
Sandy Bridge Processor (POWER)



Sandy Bridge Processor (GRAPHIC POWER)



Quanta Computer Inc.

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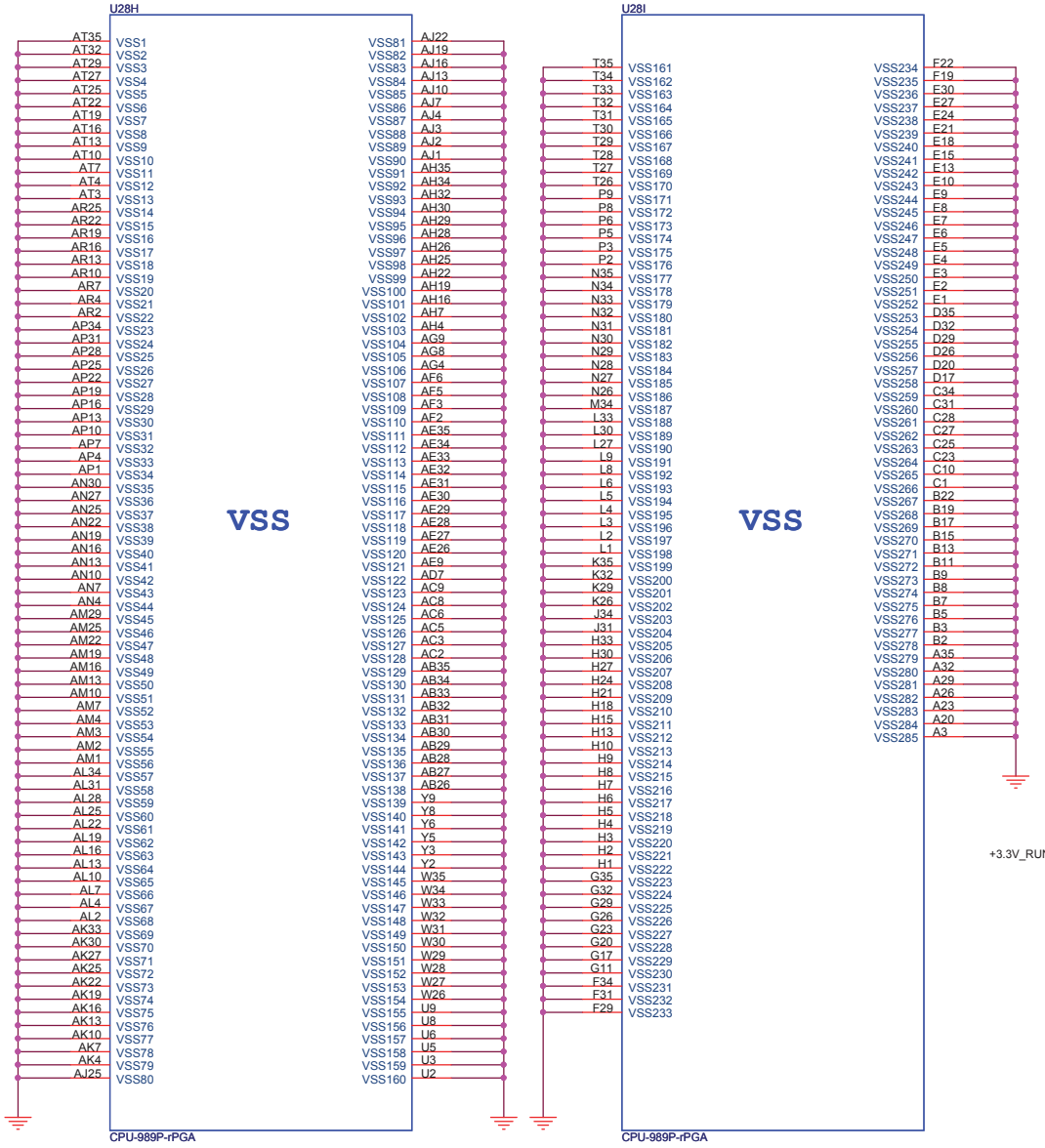
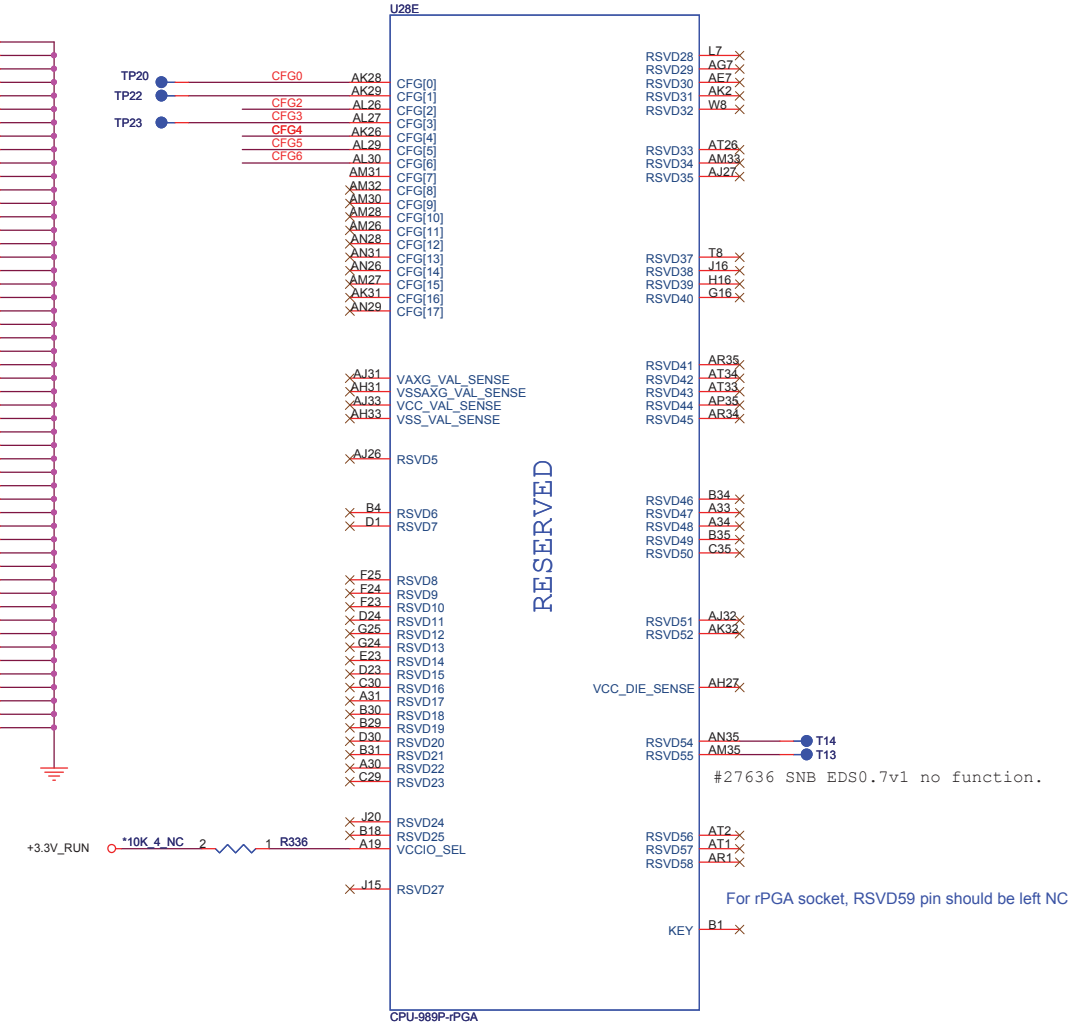
Sandy Bridge Processor (GND)



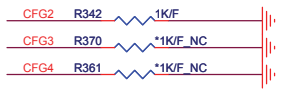
Sandy Bridge Processor (RESERVED, CFG)

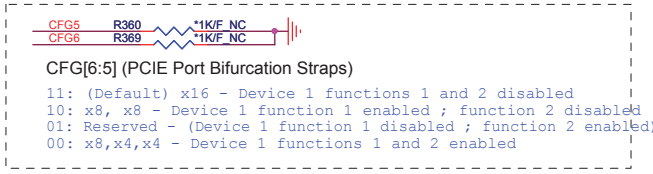


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Number Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	PCI-E Static x4 Lane Reversal	PEG wait for BIOS training
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP





Quanta Computer Inc.

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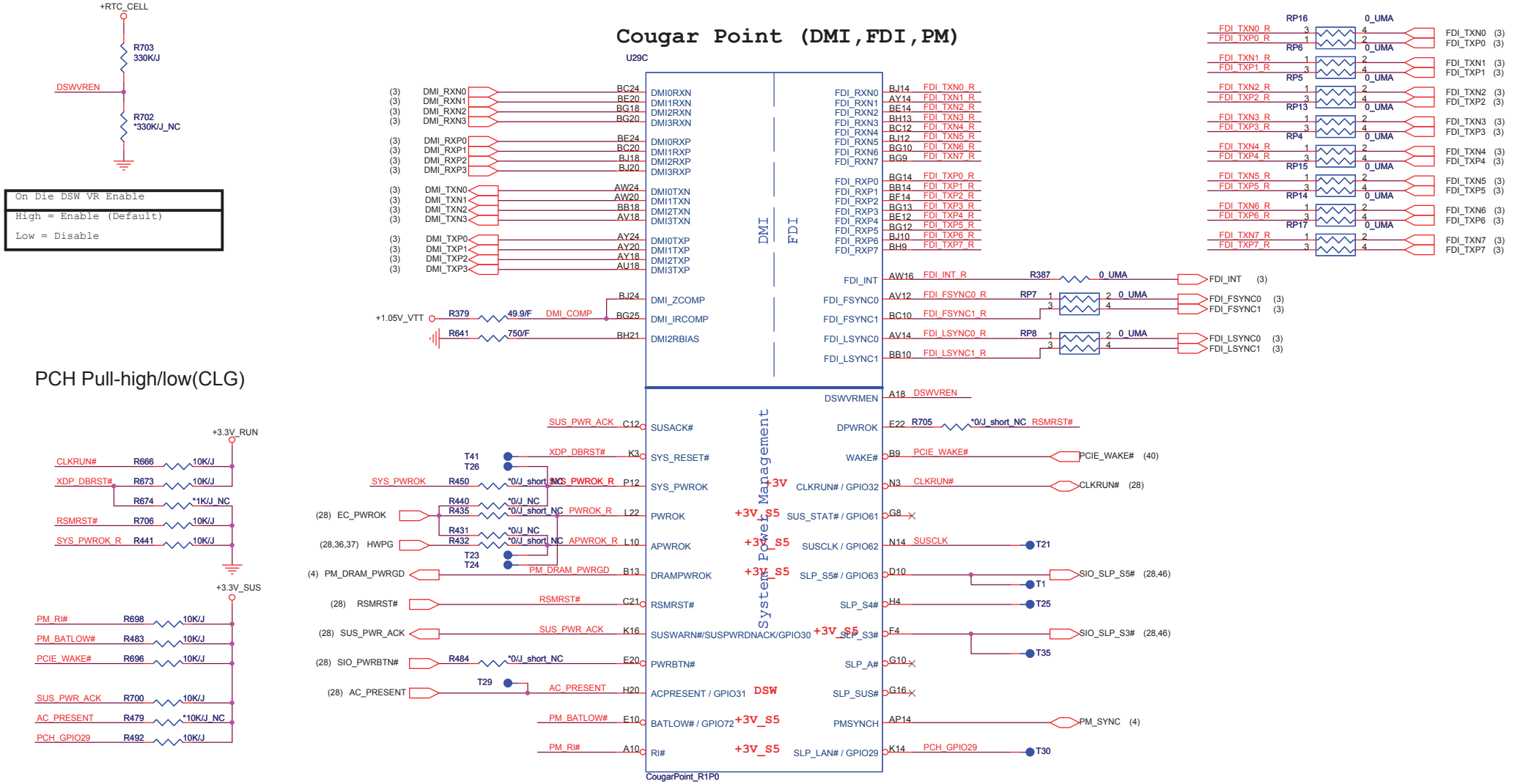
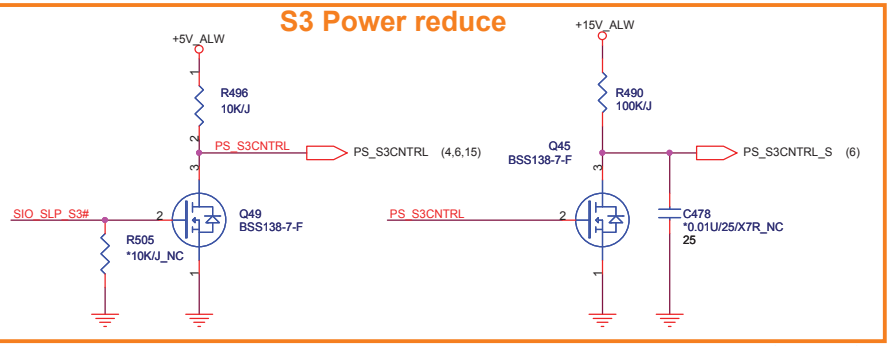
Cougar Point (DMI,FDI,PM)

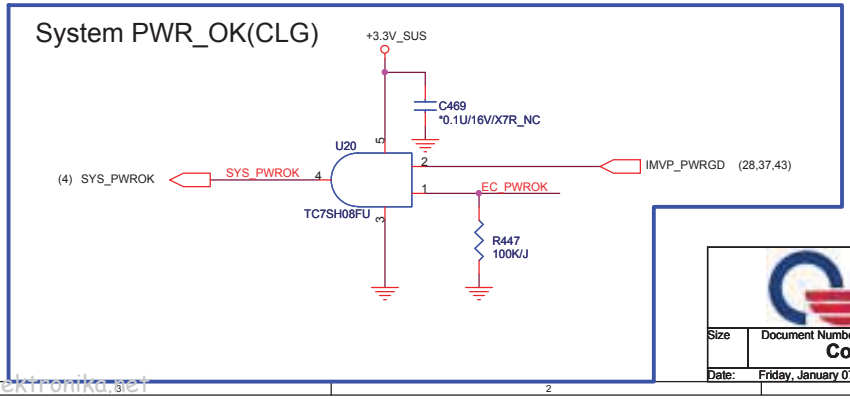


PCH Pull-high/low(CLG)

S3 Power reduce



System PWR_OK(CLG)



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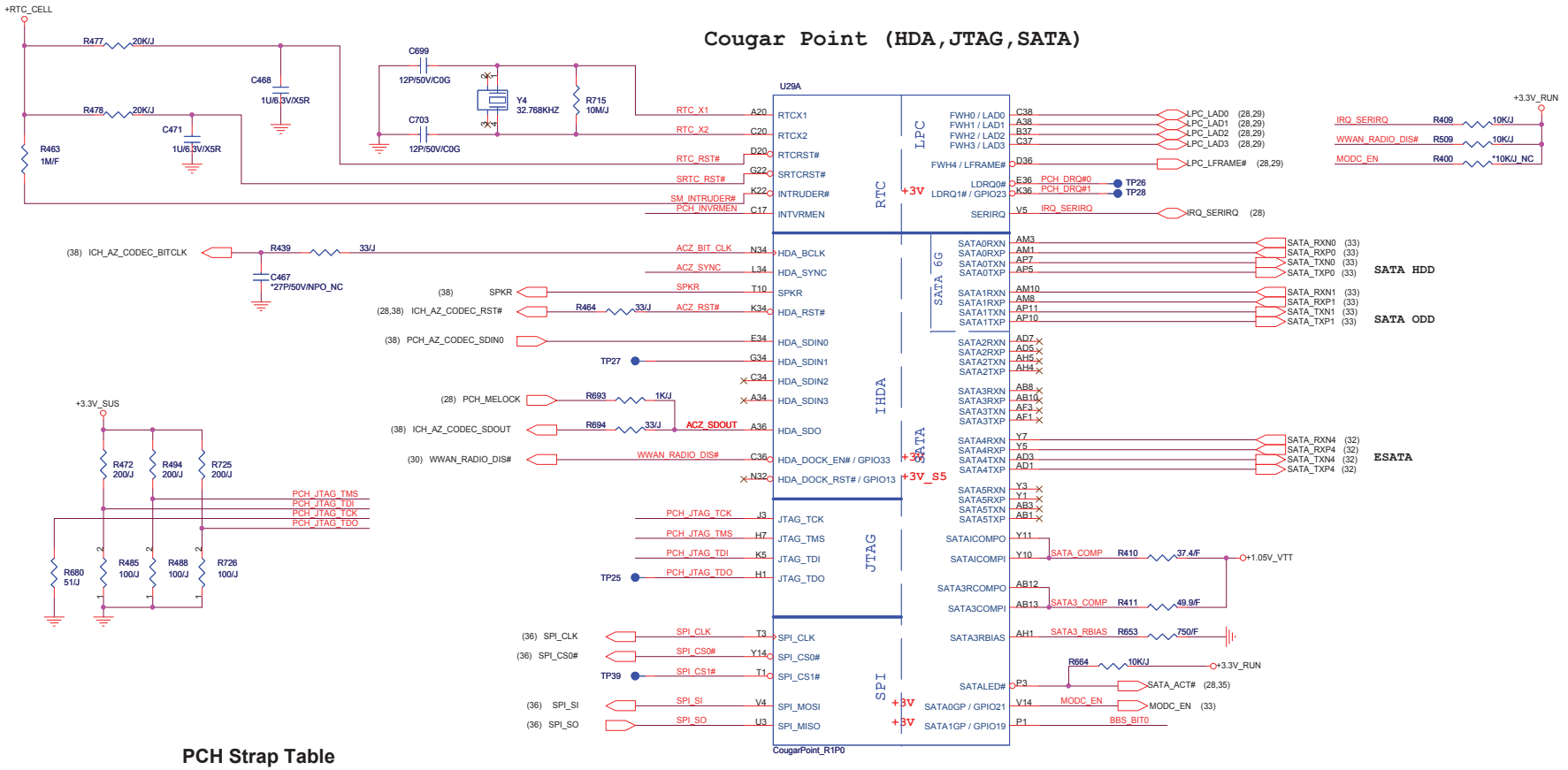
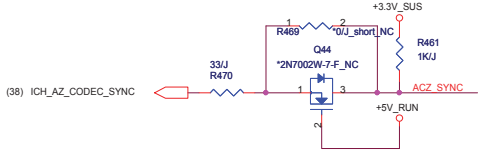
Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm 0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)

GNT1#	GNT0#	Boot Location
1	1	SPI *
0	0	LPC



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Cougar Point-M (PCI-E,SMBUS,CLK)

Note:Place TX DC blocking caps close to PCH.

U29B

Mini WWAN
Mini WLAN
USB 3.0
Card Reader
Giga Bit LOM
Mini WLAN
Card Reader
Mini WWAN
USB3.0
Giga Bit LOM

Enable Free-Running
(confirm with BIOS) 0628

WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor

EC

PCIE Clock Request

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Change as big package (UM9)

25MHz Clock for DCI Function

CougarPoint_R1P0

Quanta Computer Inc.		
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Cougar Point (LVDS,DDI)

Cougar Point-M (PCI,USB,NVRAM)

U29D

U29E

LVDS_IBG to other single 20 mils

TBC if there's OC issue 0629 (It's OK, DP has redriver IC)

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

change to R01 schematic

Quanta Computer Inc.	
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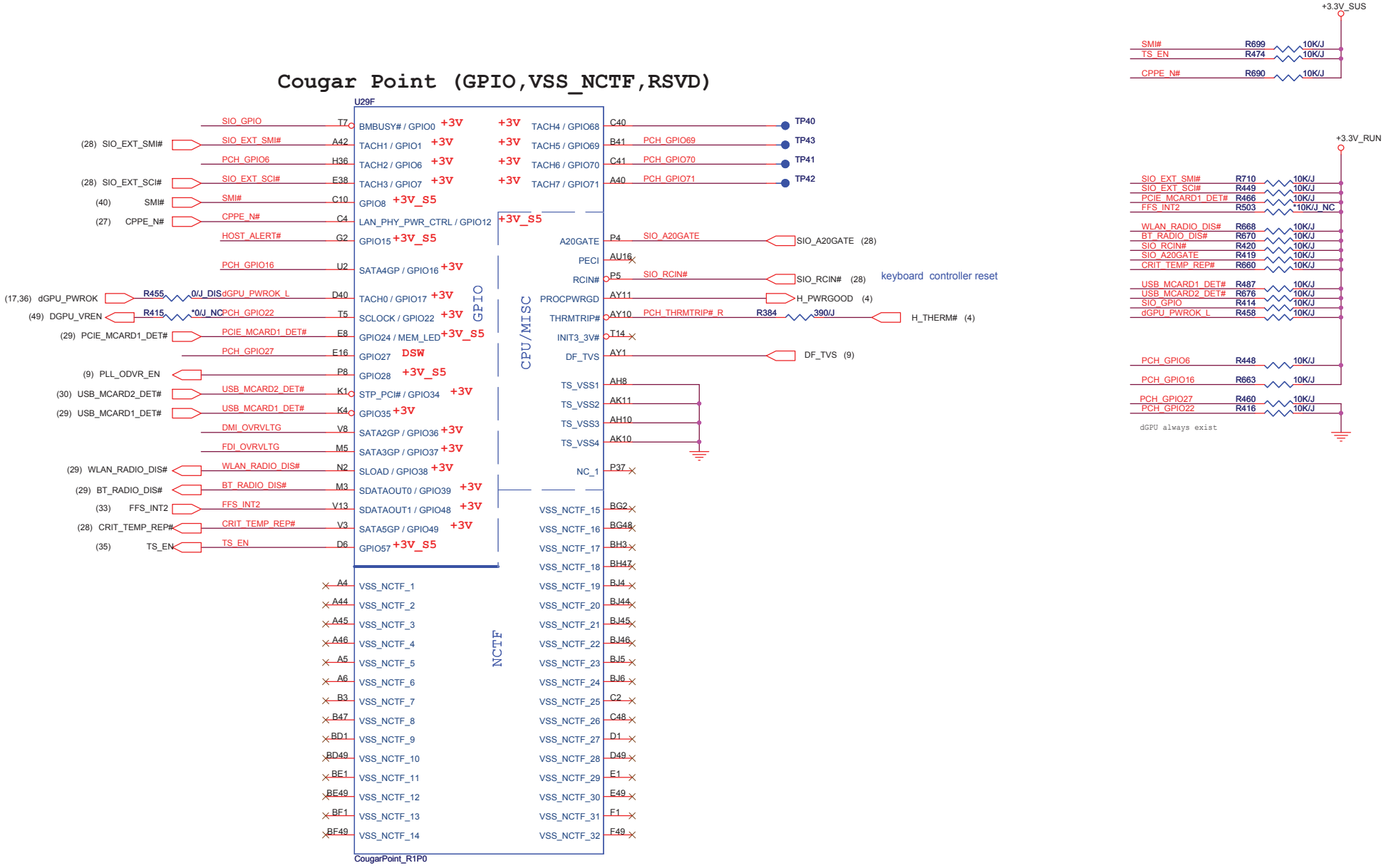
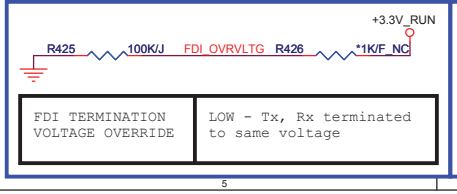
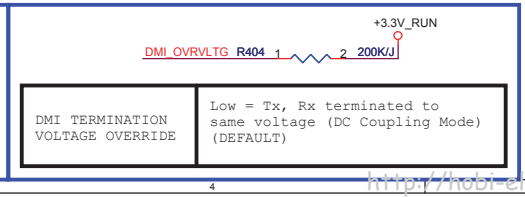
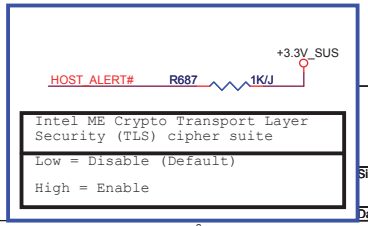
Cougar Point (GPIO,VSS_NCTF,RSVD)







internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)



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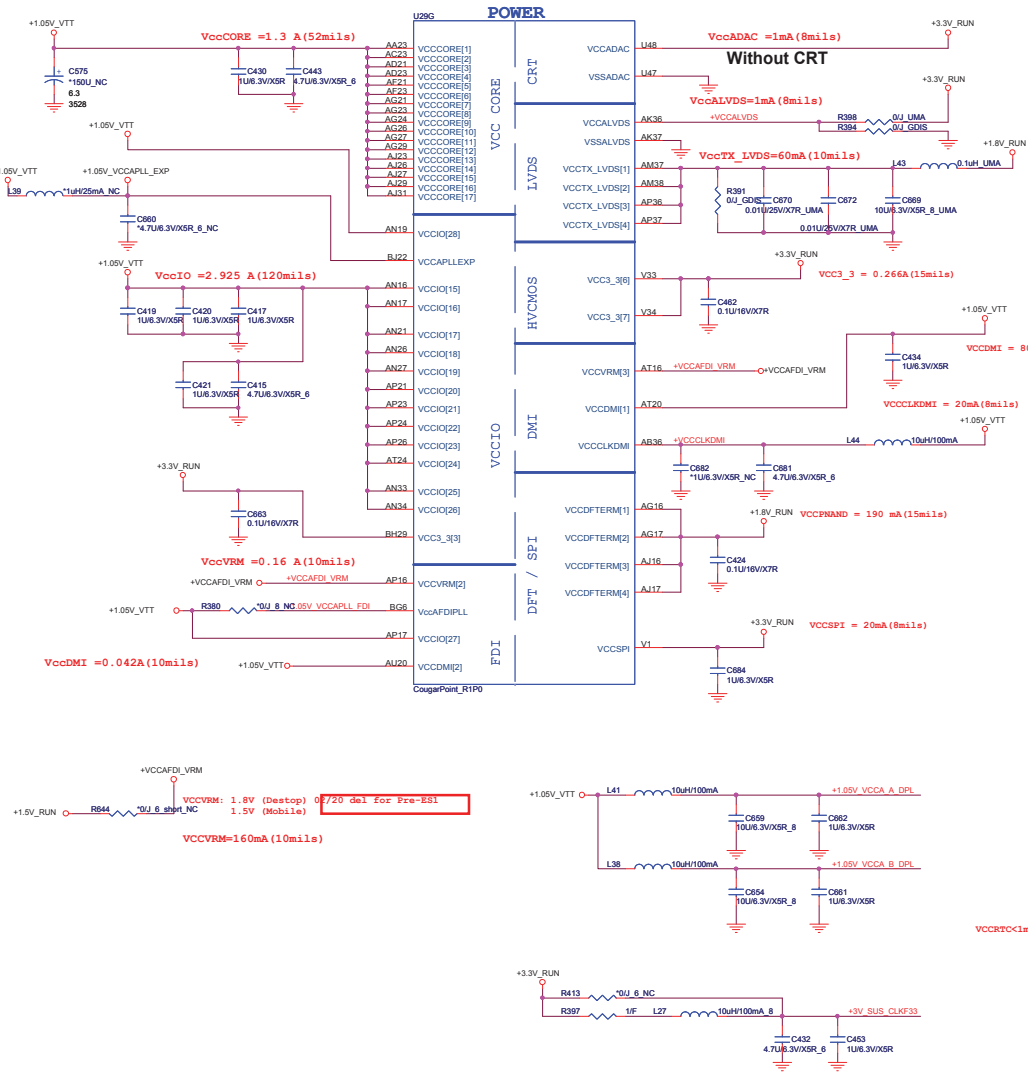
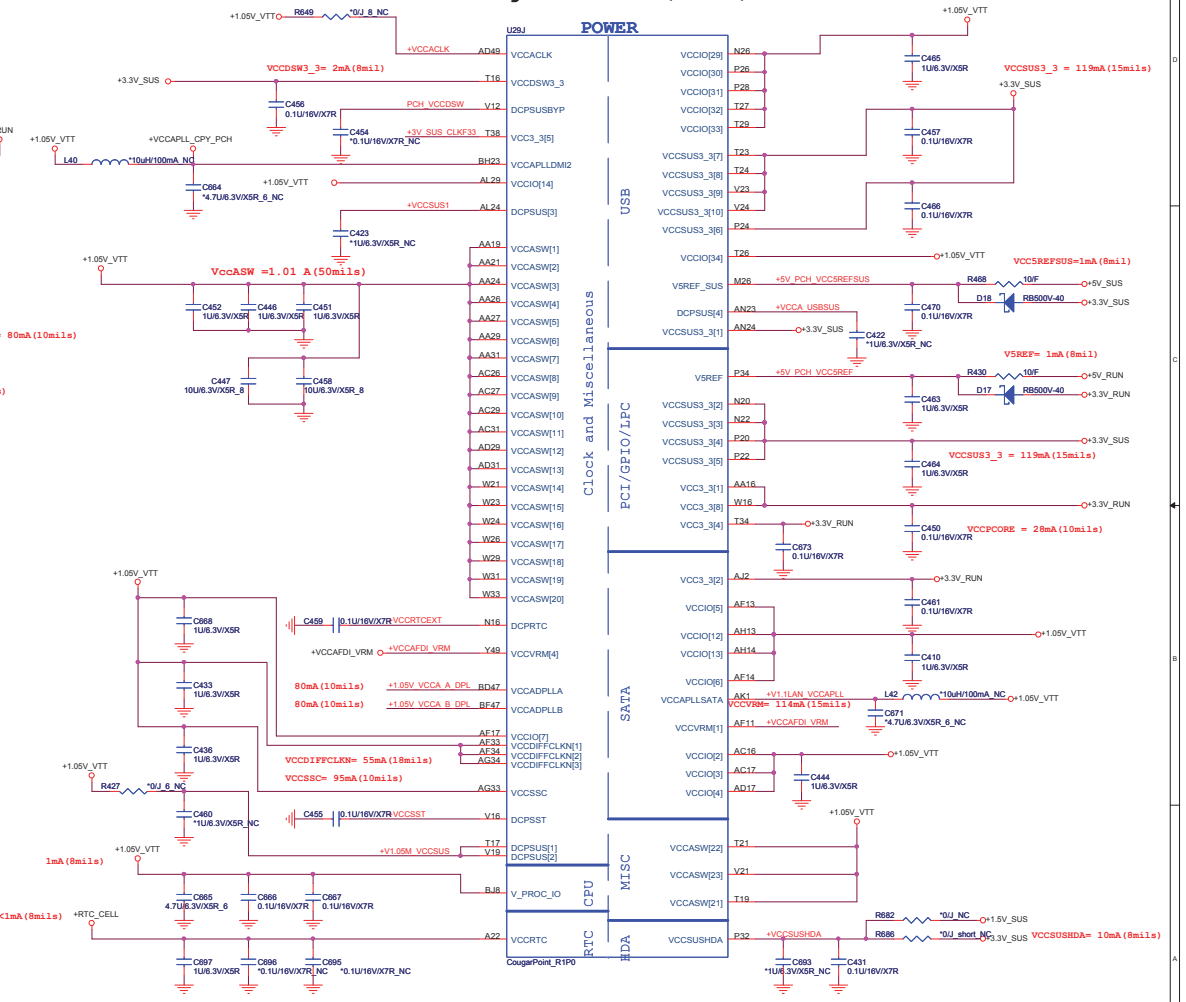
COUGAR POINT (POWER)



Cougar Point-M (POWER)



Quanta Computer Inc.			
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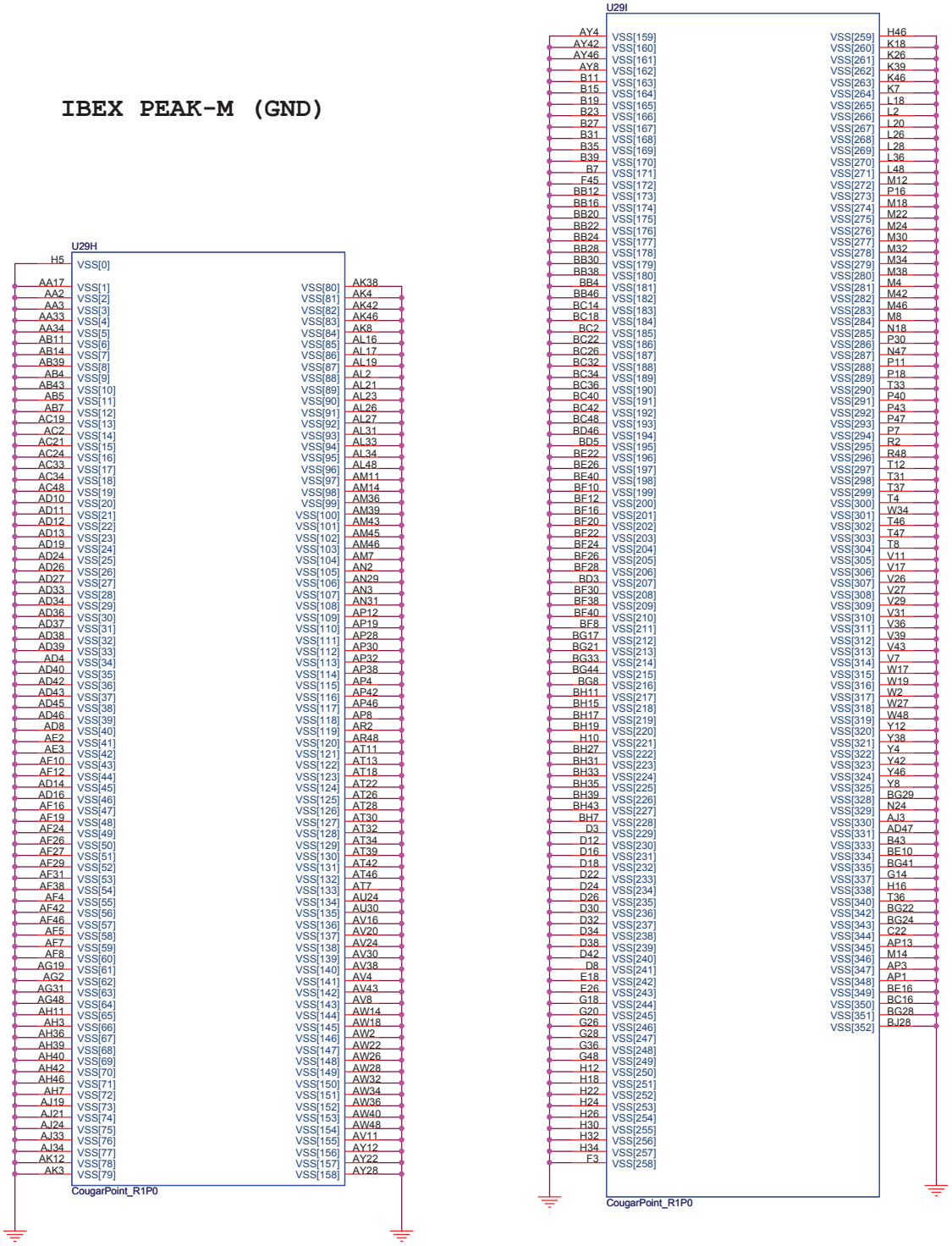
PCH6 (CLG)

IBEX PEAK-M (GND)



Quanta Computer Inc.

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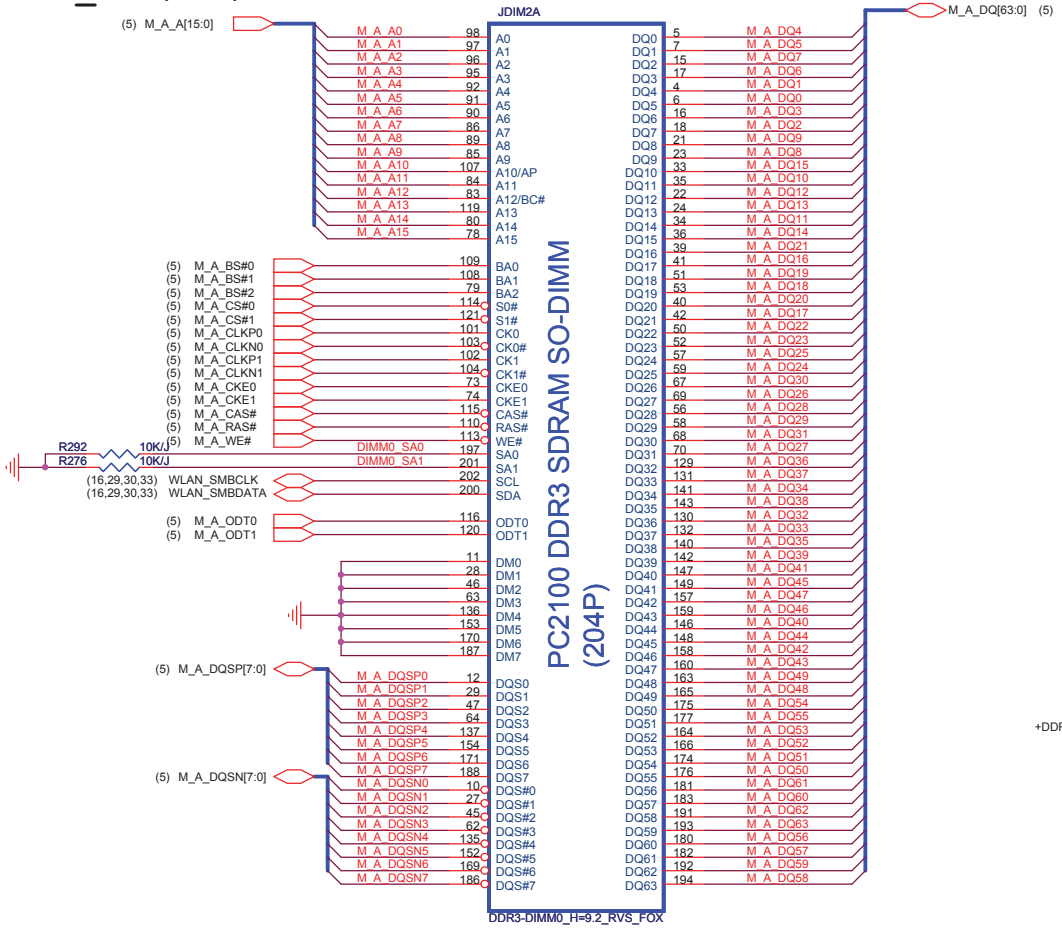
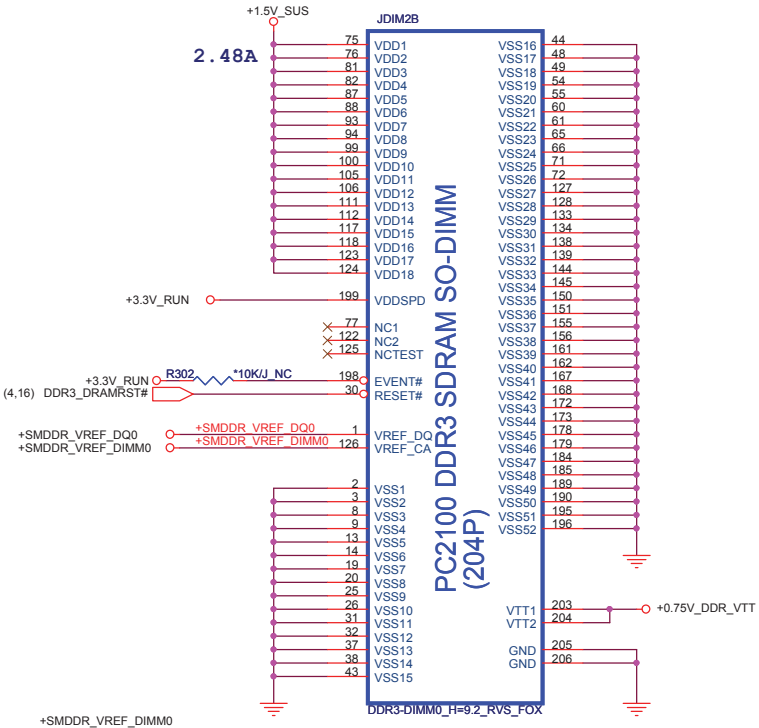
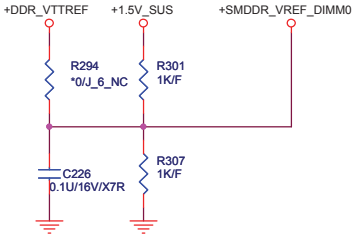
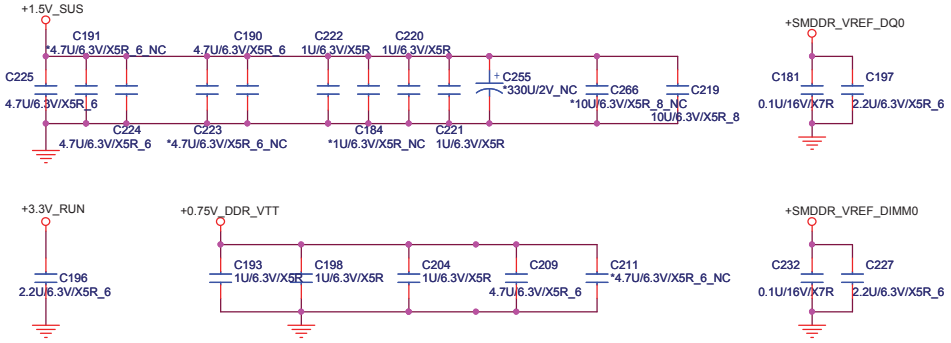
DDR_STD (DDR)



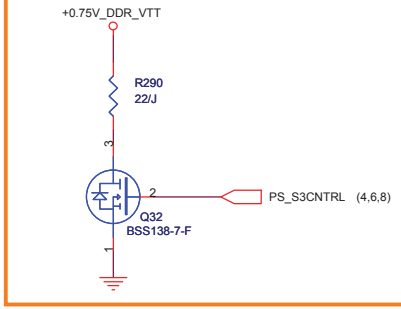




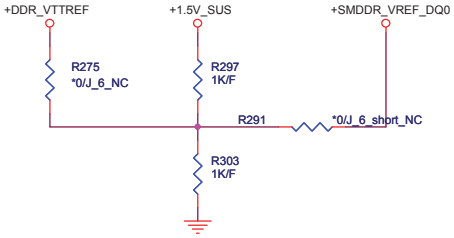
Place these Caps near So-Dimm0.



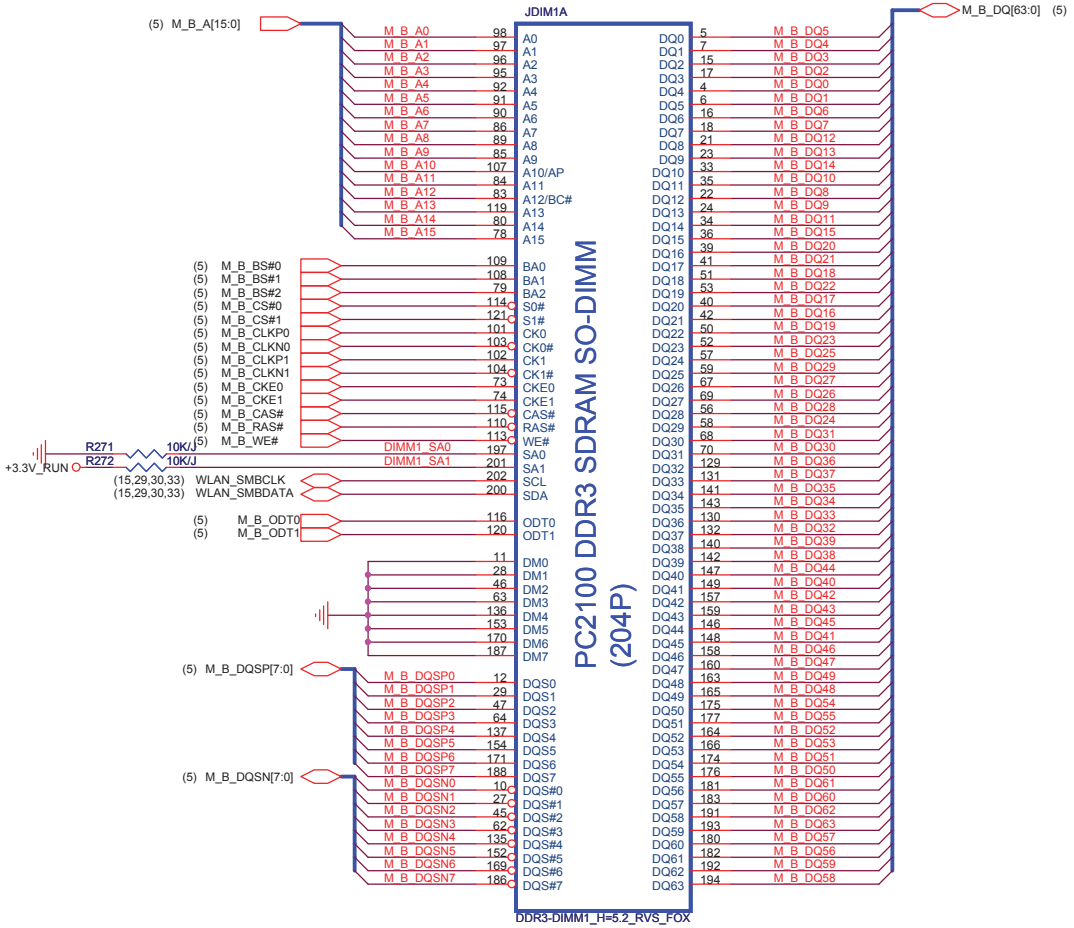
S3 Power reduce

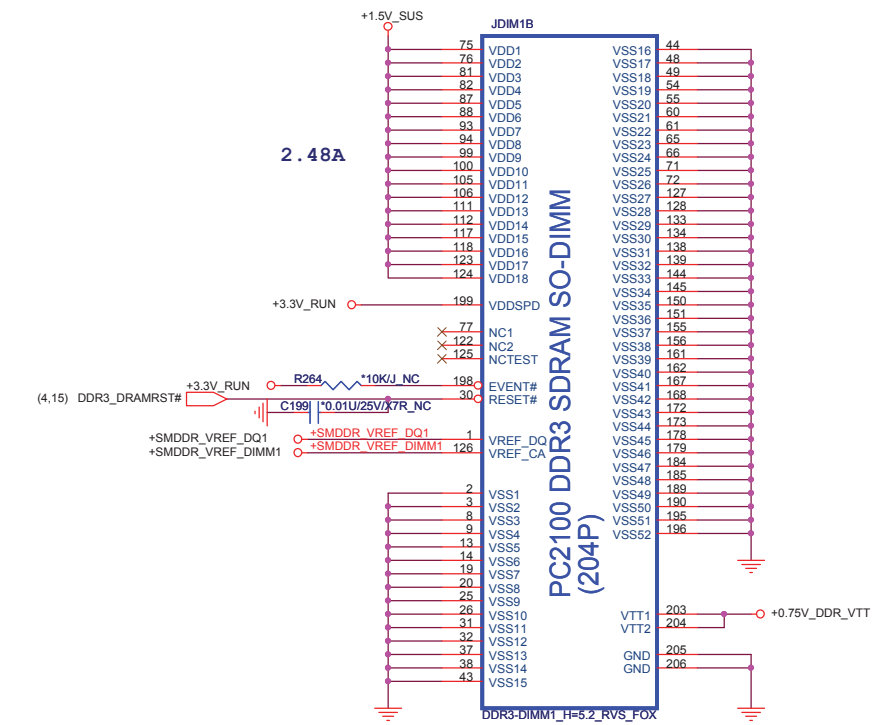


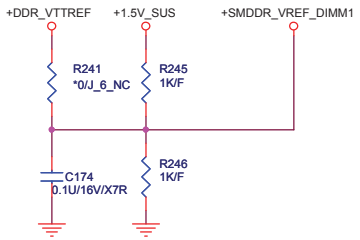
M1 VREF Solution

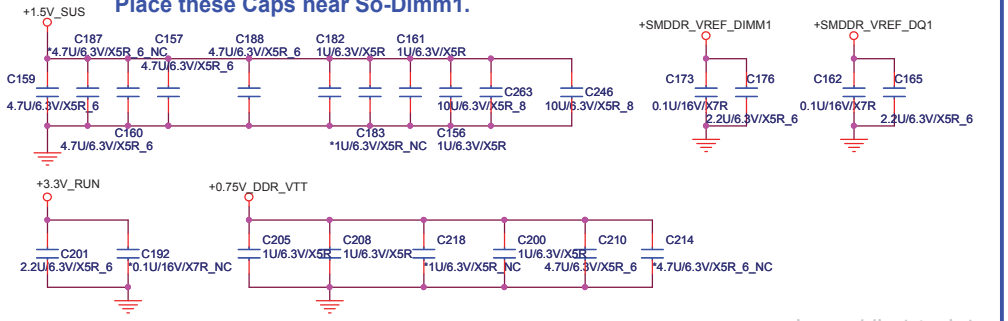


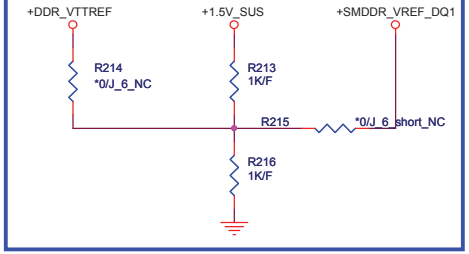
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
Date: Friday, January 07, 2011	Sheet 15 of 59	









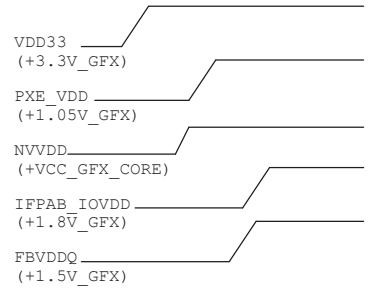


Quanta Computer Inc.

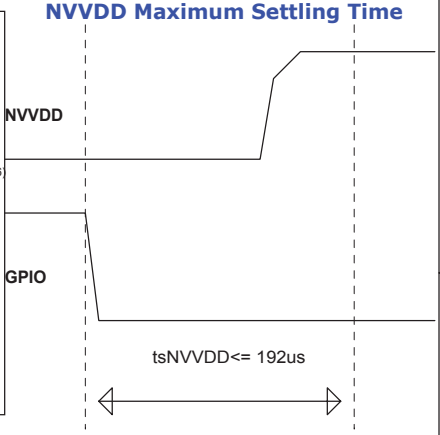
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Friday, January 07, 2011	Sheet 16 of 59	

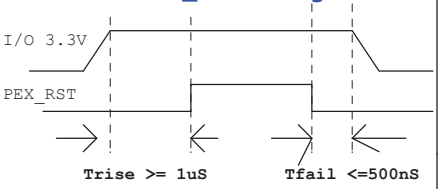
power up sequence

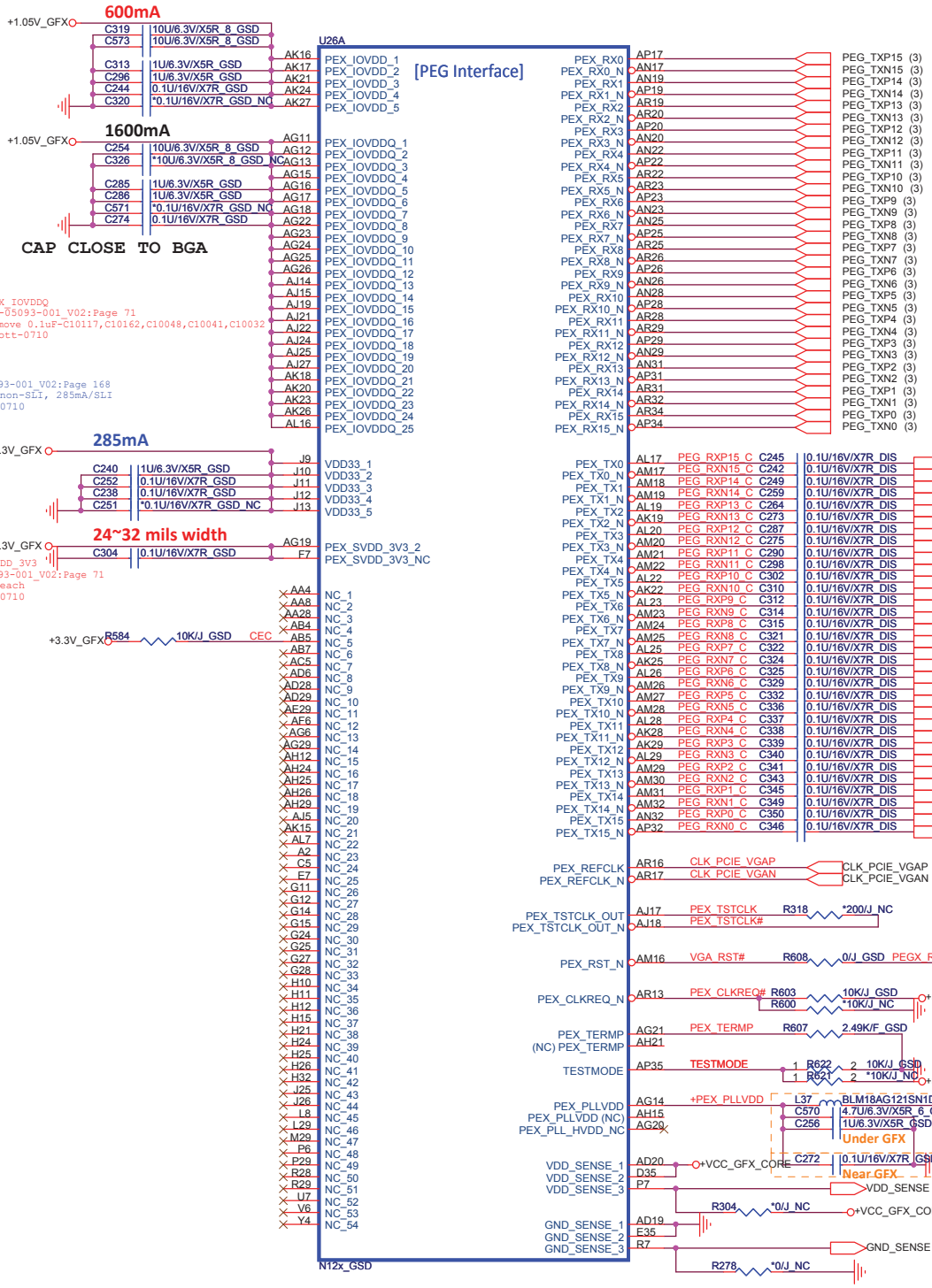


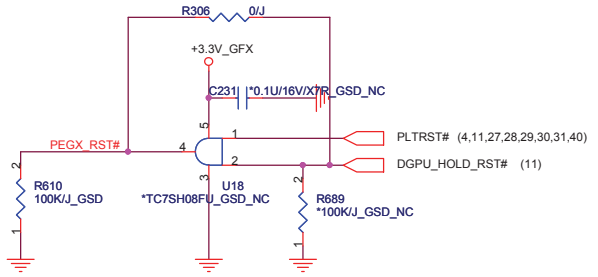
NVVDD Maximum Settling Time



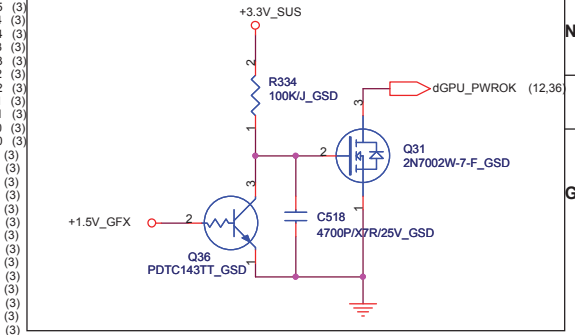
PEX_RST timing

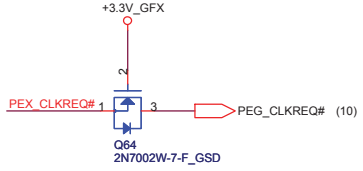






GPU all PWROK



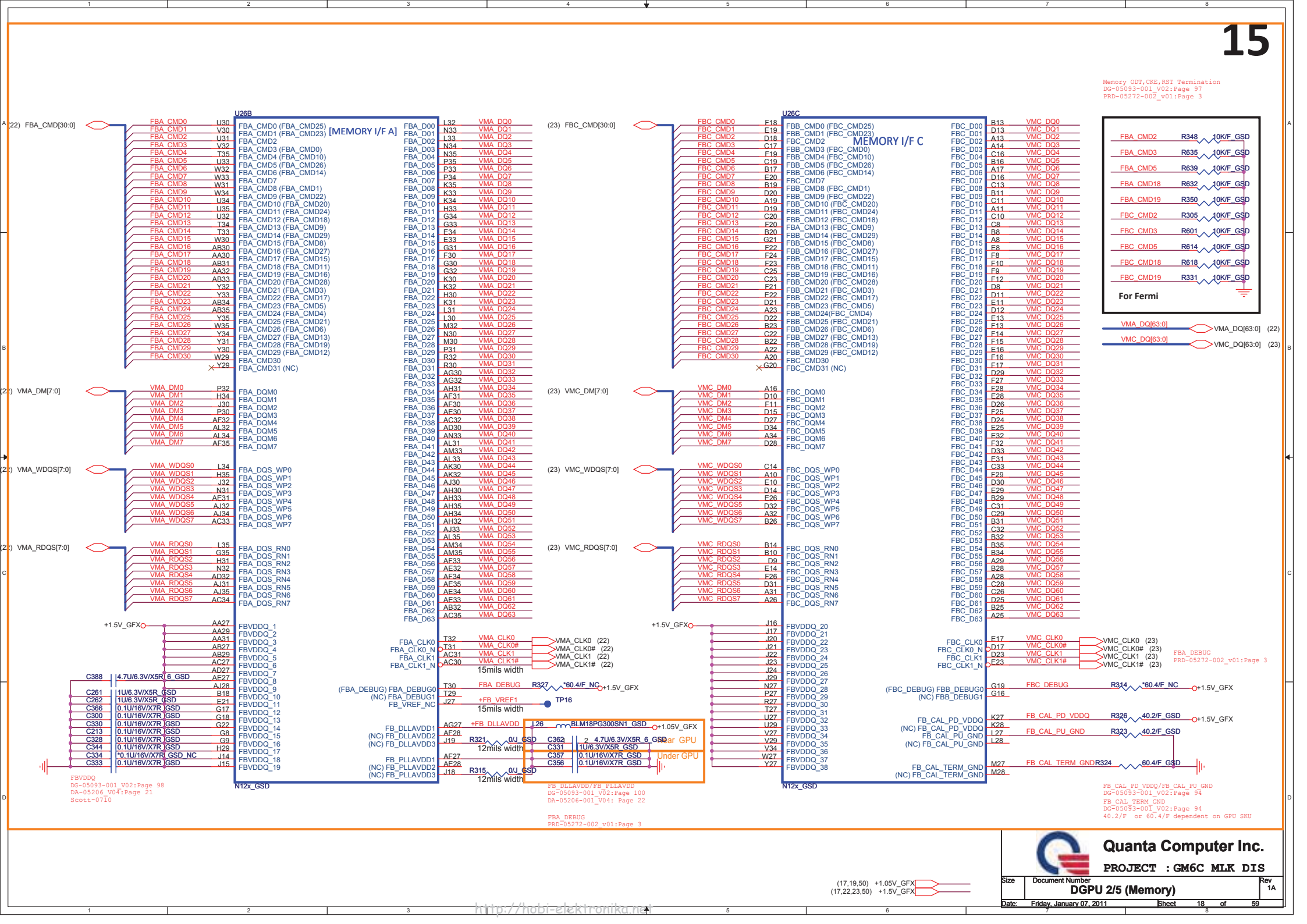


PEX_CLKREQ# circute is different with GM6.
Confirm with GM6

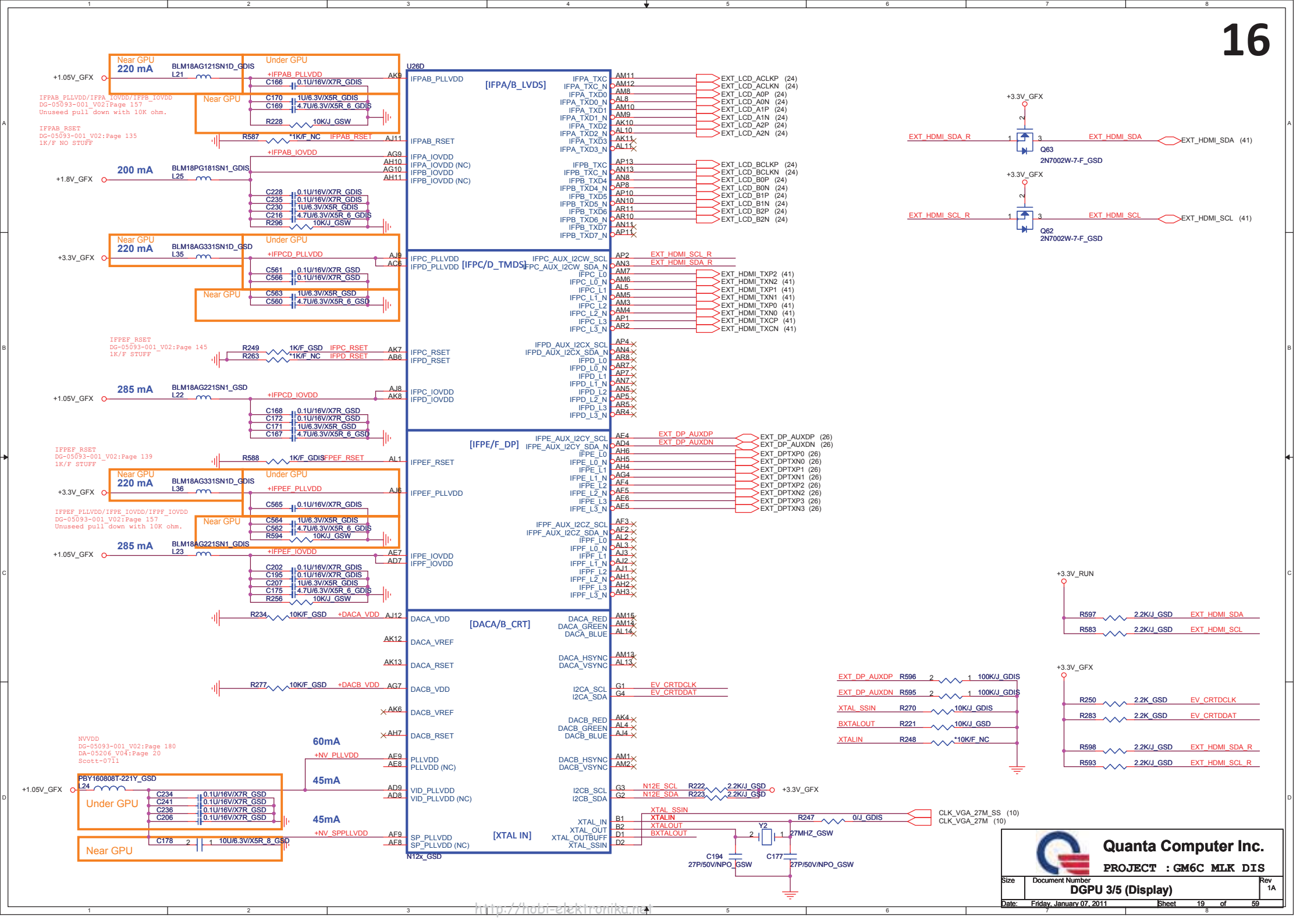
240mA
24~32 mils width

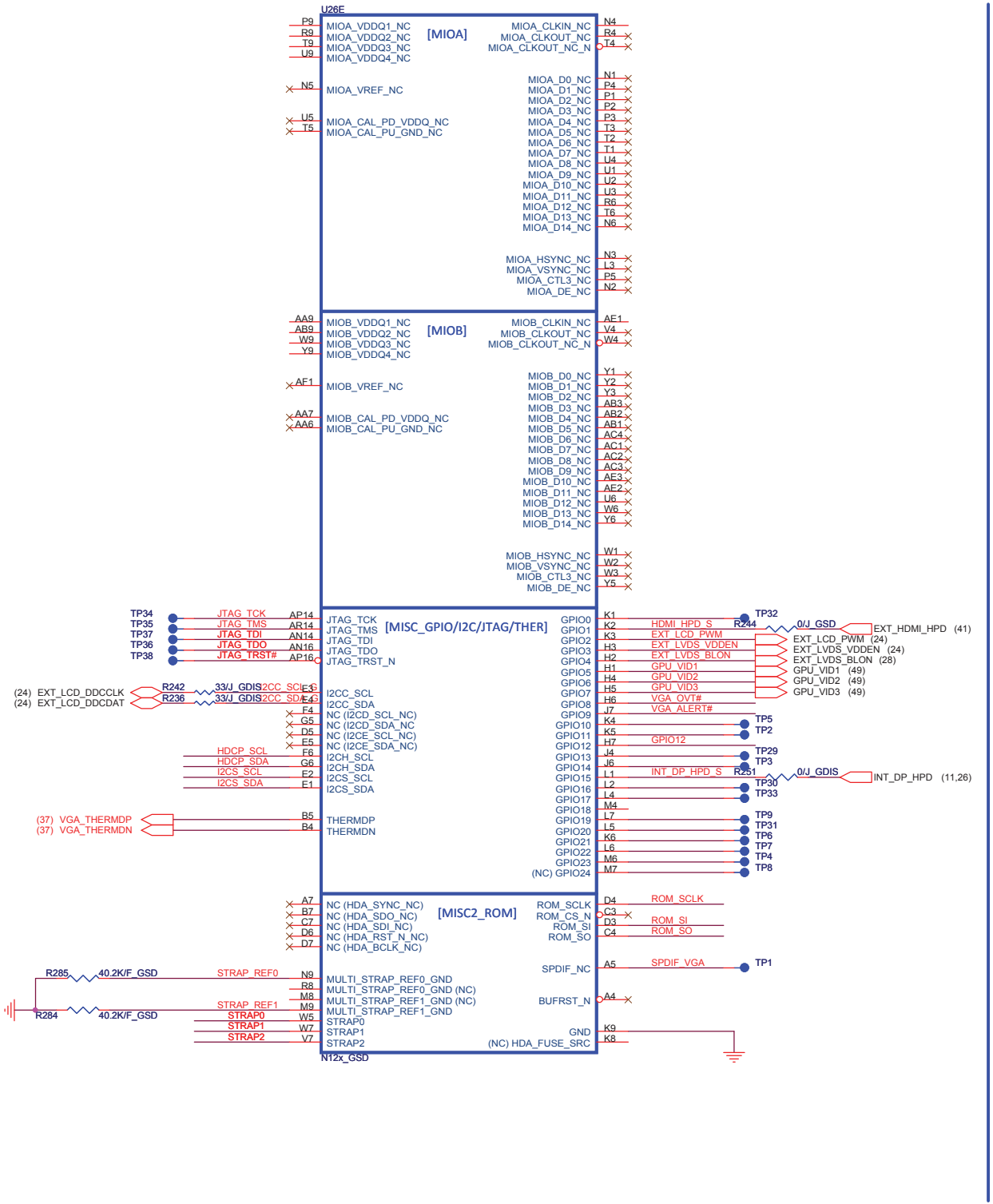
PEX_PLLVDD
DG-05093-001_V02:Page 71,72
120mA each
Scott-0710

Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: DGPU 1/5 (PEG)	Rev: 1A
Date: Friday, January 07, 2011	Sheet 17 of 59	



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A
Date: Friday, January 07, 2011	Sheet 18 of 59	





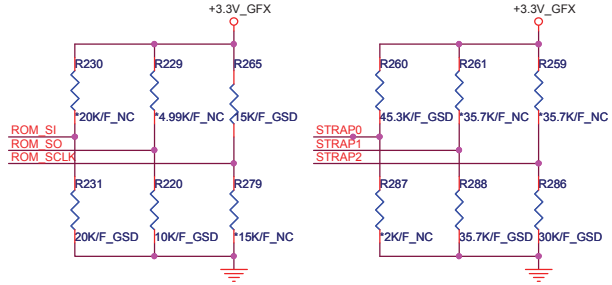
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C
0x6(0110)	900MHz 1GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 1GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

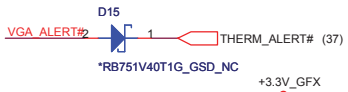
ROM_SI Strap Bit for RAM Mapping

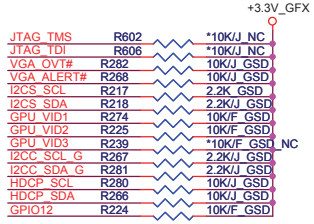
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

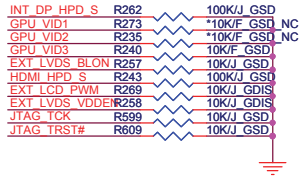


STRAP2 ROM_SCLK

N12P-GE (AJ0N12P0T02)	PD 30K	PU 15K	0xDF5	
N12P-GT (AJ0N12P0T03)	PD 35K	PU 15K	0xDF6	
N12P-GS (AJ0N12P0T04)	PD 25K	PU 15K	0xDF4	







GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI Raster Sync
12	IN	N/A	AC PWR Detect Input
13	OUT	N/A	Power Supply Control
14	OUT	N/A	Power Supply Control
15	OUT	N/A	Hot plug detect for IFP link E
16	OUT	N/A	Programmable Fan Control
17	OUT	N/A	Reserved
19	OUT	N/A	Reserved
20	OUT	N/A	Hot plug detect for IFP link D
21	OUT	N/A	Reserved
22	OUT	N/A	Hot plug detect for IFP link F
23	OUT	N/A	SLI Swap Ready single
23	OUT	N/A	

Quanta Computer Inc.
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Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

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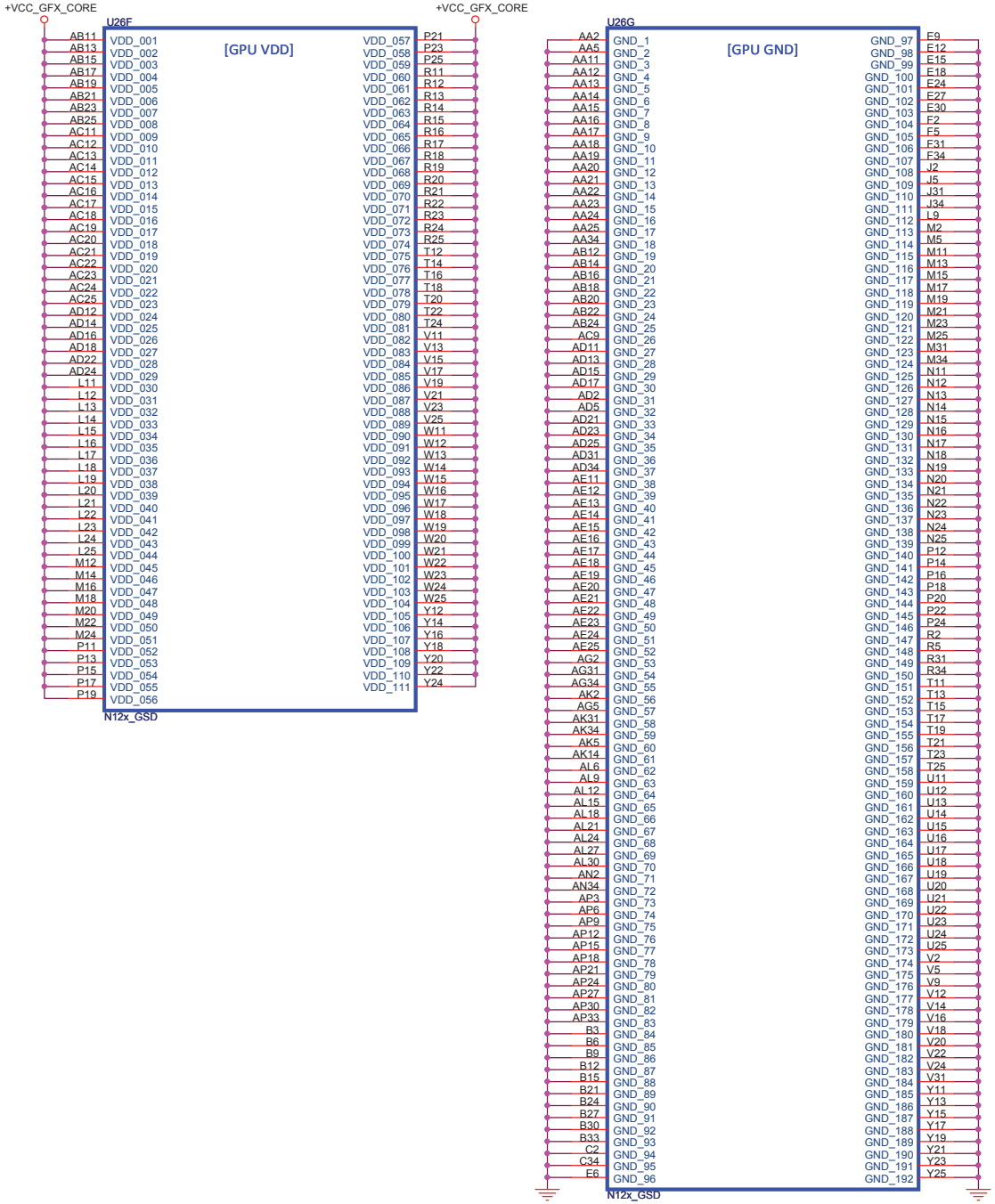
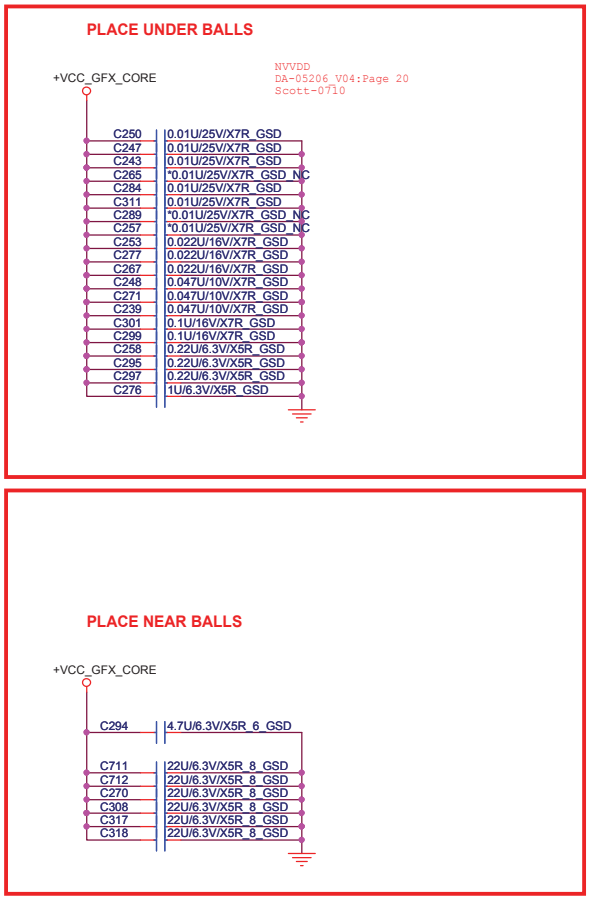
31.56A





Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A

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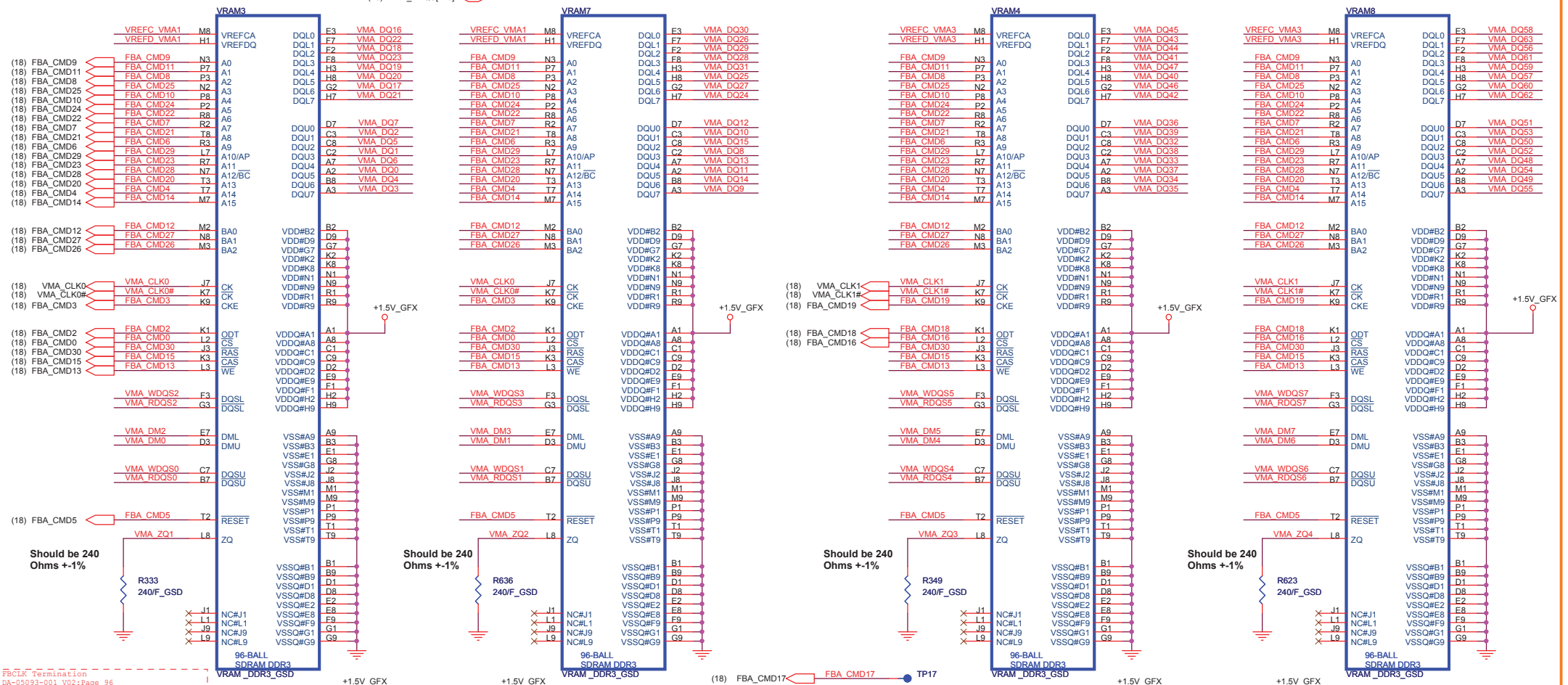
CHANNEL A: 256MB/512MB DDR3

(18) VMA_DQ[63..0]
(18) VMA_DM[7..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]



PROJECT : TWH Quanta Computer Inc.		
NB5	Size: Custom Document Number: DGPU Memory 1/2 (DDR3)	Rev: 1A
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CHANNEL B: 256MB/512MB DDR3

(18) VMC_DQ[63..0]
(18) VMC_DM[7..0]
(18) VMC_WDQS[7..0]
(18) VMC_RDQS[7..0]

VRAM5 / VRAM1 / VRAM2 / VRAM6 — 96-BALL SDRAM DDR3 — VRAM_DDR3_GSD

Should be 240 Ohms +-1%

R604 240/F_GSD
R316 240/F_GSD
R330 240/F_GSD
R617 240/F_GSD

FBCLK Termination
DA-05093-001_V02:Page 96
R=160/F
Scott-0710

Placement has to be close to VRAM

R308 162/F_GSD
R332 162/F_GSD

R612 1.33K/F_GSD
R295 1.33K/F_GSD
R328 1.33K/F_GSD
R620 1.33K/F_GSD

C572 0.01U/25V/X7R_GSD
C229 0.01U/25V/X7R_GSD
C342 0.01U/25V/X7R_GSD
C585 0.01U/25V/X7R_GSD

C576 *4.7U/6.3V/X5R_6_NC

TP13 FBC_CMD17
TP10 FBC_CMD1

C610 10U/6.3V/X5R_8_GSD
C387 10U/6.3V/X5R_8_GSD
C635 10U/6.3V/X5R_8_GSD
C279 *0.1U/16V/X7R_GSD_NC
C647 0.1U/16V/X7R_GSD
C648 0.1U/16V/X7R_GSD

C393 1U/6.3V/X5R_GSD
C646 1U/6.3V/X5R_GSD
C621 1U/6.3V/X5R_GSD
C278 1U/6.3V/X5R_GSD

C212 0.1U/16V/X7R_GSD
C351 0.1U/16V/X7R_GSD
C293 *0.1U/16V/X7R_GSD_NC
C396 *0.1U/16V/X7R_GSD_NC
C382 0.1U/16V/X7R_GSD
C593 0.1U/16V/X7R_GSD
C395 0.1U/16V/X7R_GSD
C217 0.1U/16V/X7R_GSD

C590 0.1U/16V/X7R_GSD
C644 0.1U/16V/X7R_GSD
C605 0.1U/16V/X7R_GSD
C367 *0.1U/16V/X7R_GSD_NC
C268 *0.1U/16V/X7R_GSD_NC
C643 0.1U/16V/X7R_GSD
C600 0.1U/16V/X7R_GSD
C335 0.1U/16V/X7R_GSD

PROJECT : TWH	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: DGPU Memory 2/2 (DDR3)
Rev: 1A	
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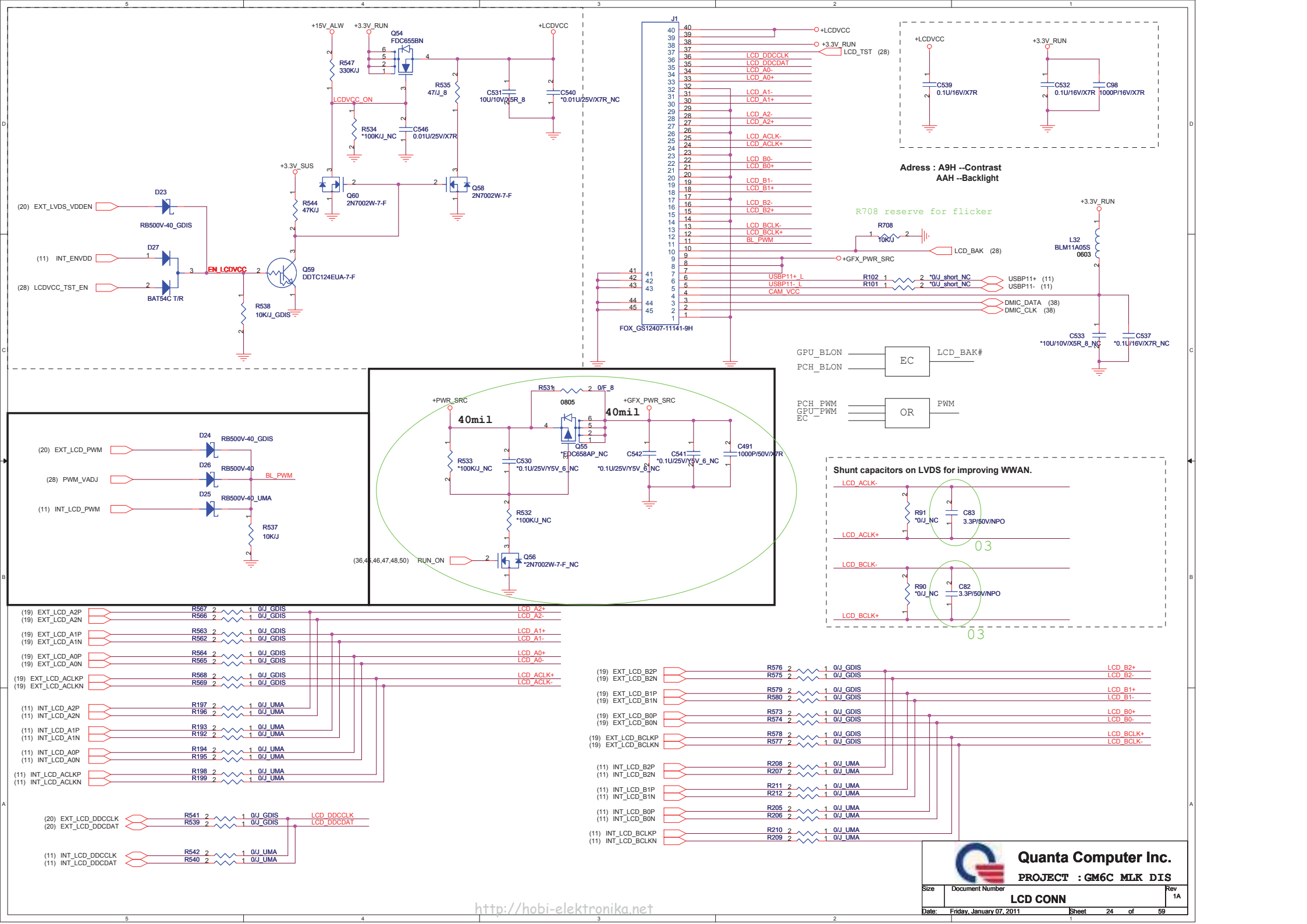
+15V_ALW
+3.3V_RUN
Q54
FDC655BN
R547
330K/J
LCDVCC_ON
R535
47/J_8
C531
10U/10V/X5R_8
C540
*0.01U/25V/X7R_NC
R534
*100K/J_NC
C546
0.01U/25V/X7R
+LCDVCC
+3.3V_SUS
R544
47K/J
Q60
2N7002W-7-F
Q58
2N7002W-7-F
D23
RB500V-40_GDIS
(20) EXT_LVDS_VDDEN
D27
(11) INT_ENVDD
BAT54C T/R
(28) LCDVCC_TST_EN
EN_LCDVCC
Q59
DDTC124EUA-7-F
R538
10K/J_GDIS
J1
FOX_GS12407-11141-9H
+LCDVCC
+3.3V_RUN
LCD_TST (28)
LCD_DDCCLK
LCD_DDCDAT
LCD_A0-
LCD_A0+
LCD_A1-
LCD_A1+
LCD_A2-
LCD_A2+
LCD_ACLK-
LCD_ACLK+
LCD_B0-
LCD_B0+
LCD_B1-
LCD_B1+
LCD_B2-
LCD_B2+
LCD_BCLK-
LCD_BCLK+
BL_PWM
+GFX_PWR_SRC
USBP11+_L
USBP11-_L
CAM_VCC
C539
0.1U/16V/X7R
C532
0.1U/16V/X7R
C98
1000P/16V/X7R
Adress : A9H --Contrast
AAH --Backlight
R708 reserve for flicker
R708
10K/J
LCD_BAK (28)
R102
R101
*0/J_short_NC
USBP11+ (11)
USBP11- (11)
DMIC_DATA (38)
DMIC_CLK (38)
L32
BLM11A05S
0603
C533
*10U/10V/X5R_8_NC
C537
*0.1U/16V/X7R_NC
GPU_BLON
PCH_BLON
EC
LCD_BAK#
PCH_PWM
GPU_PWM
EC_
OR
PWM
D24
RB500V-40_GDIS
(20) EXT_LCD_PWM
D26
RB500V-40
(28) PWM_VADJ
BL_PWM
D25
RB500V-40_UMA
(11) INT_LCD_PWM
R537
10K/J
+PWR_SRC
40mil
R531
0/F_8
0805
+GFX_PWR_SRC
40mil
Q55
*EDC658AP_NC
R533
*100K/J_NC
C530
*0.1U/25V/Y5V_6_NC
C542
*0.1U/25V/Y5V_6_NC
C541
*0.1U/25V/Y5V_6_NC
C491
1000P/50V/X7R
R532
*100K/J_NC
(36,45,46,47,48,50) RUN_ON
Q56
*2N7002W-7-F_NC
Shunt capacitors on LVDS for improving WWAN.
LCD_ACLK-
LCD_ACLK+
R91
*0/J_NC
C83
3.3P/50V/NPO
03
LCD_BCLK-
LCD_BCLK+
R90
*0/J_NC
C82
3.3P/50V/NPO
03
(19) EXT_LCD_A2P
(19) EXT_LCD_A2N
R567
R566
0/J_GDIS
LCD_A2+
LCD_A2-
(19) EXT_LCD_A1P
(19) EXT_LCD_A1N
R563
R562
LCD_A1+
LCD_A1-
(19) EXT_LCD_A0P
(19) EXT_LCD_A0N
R564
R565
LCD_A0+
LCD_A0-
(19) EXT_LCD_ACLKP
(19) EXT_LCD_ACLKN
R568
R569
LCD_ACLK+
LCD_ACLK-
(11) INT_LCD_A2P
(11) INT_LCD_A2N
R197
R196
0/J_UMA
(11) INT_LCD_A1P
(11) INT_LCD_A1N
R193
R192
(11) INT_LCD_A0P
(11) INT_LCD_A0N
R194
R195
(11) INT_LCD_ACLKP
(11) INT_LCD_ACLKN
R198
R199
(20) EXT_LCD_DDCCLK
(20) EXT_LCD_DDCDAT
R541
R539
LCD_DDCCLK
LCD_DDCDAT
(11) INT_LCD_DDCCLK
(11) INT_LCD_DDCDAT
R542
R540
(19) EXT_LCD_B2P
(19) EXT_LCD_B2N
R576
R575
LCD_B2+
LCD_B2-
(19) EXT_LCD_B1P
(19) EXT_LCD_B1N
R579
R580
LCD_B1+
LCD_B1-
(19) EXT_LCD_B0P
(19) EXT_LCD_B0N
R573
R574
LCD_B0+
LCD_B0-
(19) EXT_LCD_BCLKP
(19) EXT_LCD_BCLKN
R578
R577
LCD_BCLK+
LCD_BCLK-
(11) INT_LCD_B2P
(11) INT_LCD_B2N
R208
R207
(11) INT_LCD_B1P
(11) INT_LCD_B1N
R211
R212
(11) INT_LCD_B0P
(11) INT_LCD_B0N
R205
R206
(11) INT_LCD_BCLKP
(11) INT_LCD_BCLKN
R210
R209
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
LCD CONN
Rev
1A
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http://hobi-elektronika.net

HDMI

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V

+3.3V_RUN
L9 *BLM18PG181SN1_NC
+VCC_HDMI
C46 *1U/6.3V/X5R_NC
C78 *0.1U/16V/X7R_NC
C63 *0.1U/16V/X7R_NC

U5 *SN75DP139RGZR_NC
POWER: VCC x8
GND: GND x16, EPAD
CONTROL: RT_EN#, OE#, REXT, DDC_EN, PC0, PC1, DDCBUF_EN, CFG

(41) HDMI_TXCP_L / HDMI_TXCN_L — C51 / C49 0.1U/16V/X7R — HDMI_TXCP_R / HDMI_TXCN_R — IN_D1+ / IN_D1- — OUT_D1+ / OUT_D1- — HDMI_CLK+_C / HDMI_CLK-_C
(41) HDMI_TXP0_L / HDMI_TXN0_L — C55 / C52 0.1U/16V/X7R — HDMI_TXP0_R / HDMI_TXN0_R — IN_D2+ / IN_D2- — OUT_D2+ / OUT_D2- — HDMI_TX0+_C / HDMI_TX0-_C
(41) HDMI_TXP1_L / HDMI_TXN1_L — C60 / C56 0.1U/16V/X7R — HDMI_TXP1_R / HDMI_TXN1_R — IN_D3+ / IN_D3- — OUT_D3+ / OUT_D3- — HDMI_TX1+_C / HDMI_TX1-_C
(41) HDMI_TXP2_L / HDMI_TXN2_L — C64 / C61 0.1U/16V/X7R — HDMI_TXP2_R / HDMI_TXN2_R — IN_D4+ / IN_D4- — OUT_D4+ / OUT_D4- — HDMI_TX2+_C / HDMI_TX2-_C
(41) HDMI_SCL_S — HDMI_SCL_S — SCL — SCL_SINK — HDMI_CLK
(41) HDMI_SDA_S — HDMI_SDA_S — SDA — SDA_SINK — HDMI_DAT
(11,41) INT_HDMI_HPD — INT_HDMI_HPD — HPD — HPD_SINK — HDMI_DET_L — R38 *1K/J_NC — HDMI_DET
R388 *100K/J_NC

+3.3V_RUN
R40 *4.7K/J_NC DDC_EN
R86 *4.7K/J_NC PC0
R73 *4.7K/J_NC PC1
CFG00
R49 *100K/J_NC
(10) HDMI_PWR_CTRL — R37 *0/J_NC — OE#
R74 *3.9K/J_NC
R72 *4.7K/J_NC PC0
R47 *0/J_NC
R46 *4.7K/J_NC CFG00
PQ1 *2N7002W-7-F_NC — HDMI_DET

+5V_HDMI
R7 2.2K/J
R3 2.2K/J
CN2 LTS_ABA-HDM-024-P07
HDMI_TX2+ / HDMI_TX2- / HDMI_TX1+ / HDMI_TX1- / HDMI_TX0+ / HDMI_TX0- / HDMI_CLK+ / HDMI_CLK-
HDMI_CLK / HDMI_DAT
HDMI_DET
+5V_HDMI
+5V_RUN — HDMIF1 NANOSMDC110F-2
C513 *0.1U/16V/X7R_NC
C514 0.1U/16V/X7R

Reserve for EMI and close to HDMI CONN
*EXC24CG900U_NC L1: HDMI_TX2+_C / HDMI_TX2-_C — HDMI_TX2+ / HDMI_TX2-
*EXC24CG900U_NC L4: HDMI_TX0+_C / HDMI_TX0-_C — HDMI_TX0+ / HDMI_TX0-
*EXC24CG900U_NC L2: HDMI_TX1+_C / HDMI_TX1-_C — HDMI_TX1+ / HDMI_TX1-
*EXC24CG900U_NC L3: HDMI_CLK+_C / HDMI_CLK-_C — HDMI_CLK+ / HDMI_CLK-

change
HDMI_TXCP_R / HDMI_TXCN_R — HDMI_CLK+_C / HDMI_CLK-_C
HDMI_TXP0_R / HDMI_TXN0_R — HDMI_TX0+_C / HDMI_TX0-_C
HDMI_TXP1_R / HDMI_TXN1_R — HDMI_TX1+_C / HDMI_TX1-_C
HDMI_TXP2_R / HDMI_TXN2_R — HDMI_TX2+_C / HDMI_TX2-_C

UMA change to 680ohm
R736 499/F HDMI_TX2+
R734 499/F HDMI_TX2-
R737 499/F HDMI_TX1+
R731 499/F HDMI_TX1-
R729 499/F HDMI_TX0+
R733 499/F HDMI_TX0-
R735 499/F HDMI_CLK+
R730 499/F HDMI_CLK-
+3.3V_RUN — Q75 2N7002W-7-F — R732 1M

+3.3V_RUN
Q74 MMST3904-7-F
(11,41) INT_HDMI_HPD — HDMI_HPD — R727 150K — HDMI_DET
R728 10K

+3.3V_RUN
R709 2.2K/J
R437 2.2K/J
(41) HDMI_SCL_S — HDMI_SCL_S — Q73 FDV301N — HDMI_CLK
+3.3V_RUN
(41) HDMI_SDA_S — HDMI_SDA_S — Q72 FDV301N — HDMI_DAT

Quanta Computer Inc.
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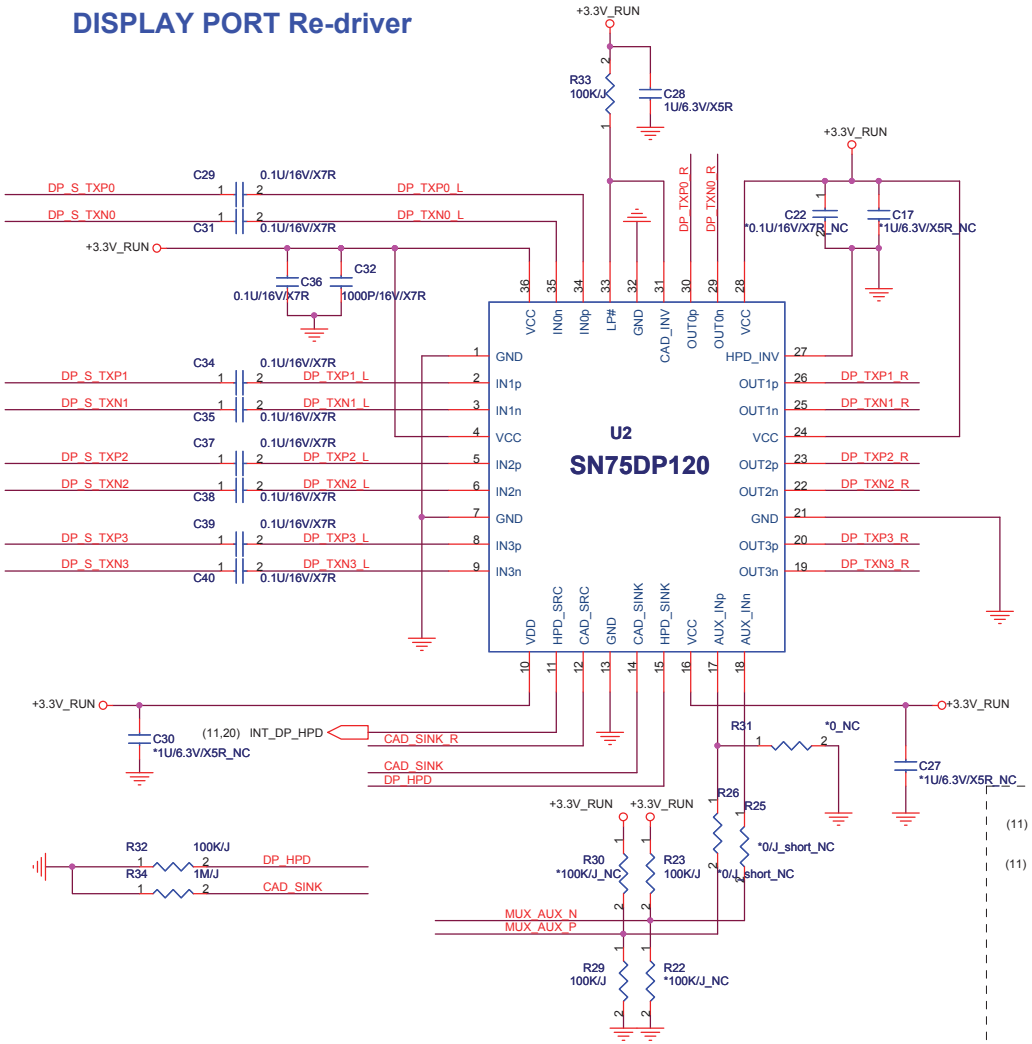
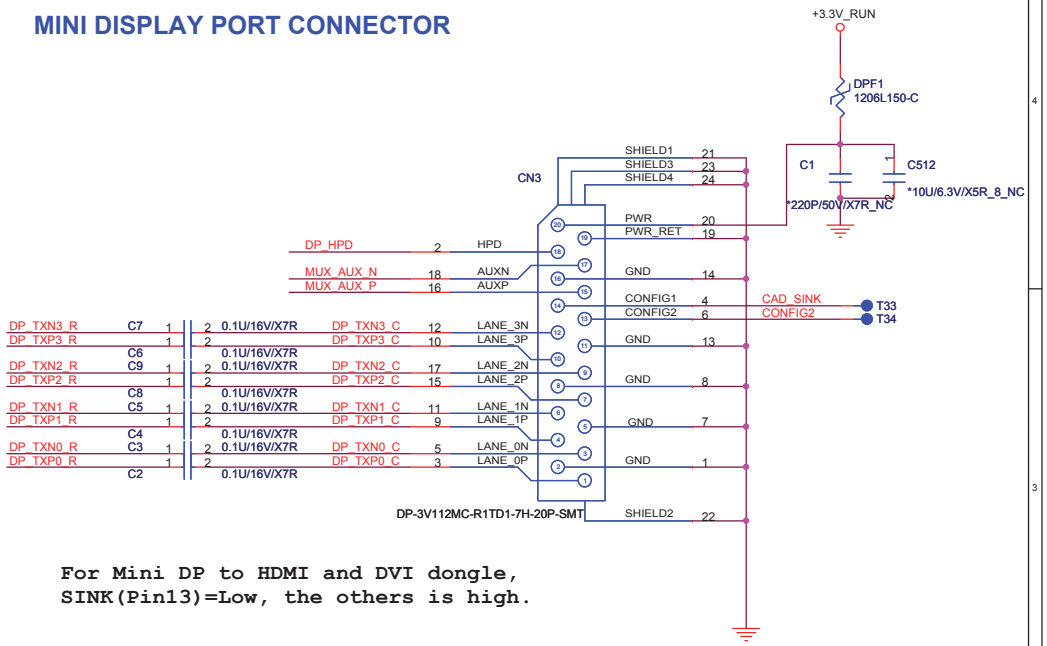
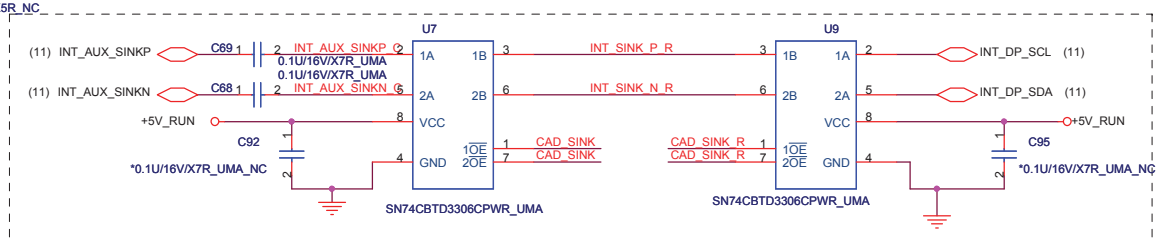
DISPLAY PORT Re-driver

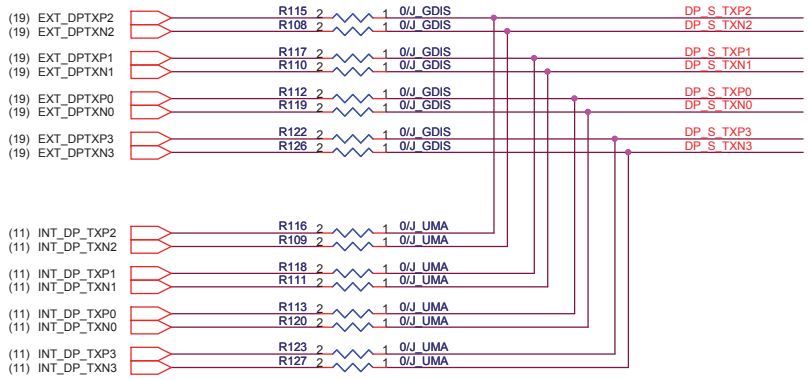


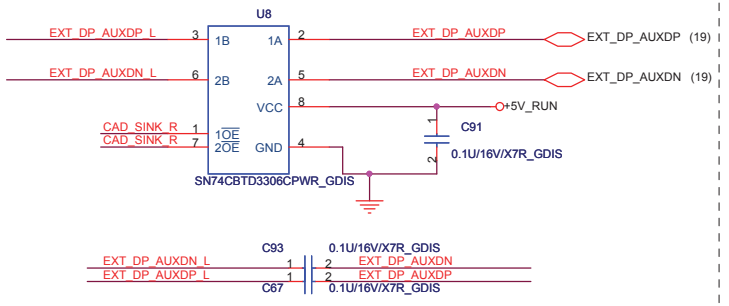
MINI DISPLAY PORT CONNECTOR



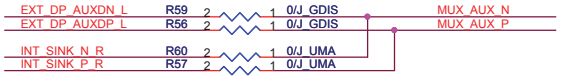
For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.







OE	Output
L	A=B
H	Z



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	MINI DP CONN	1A
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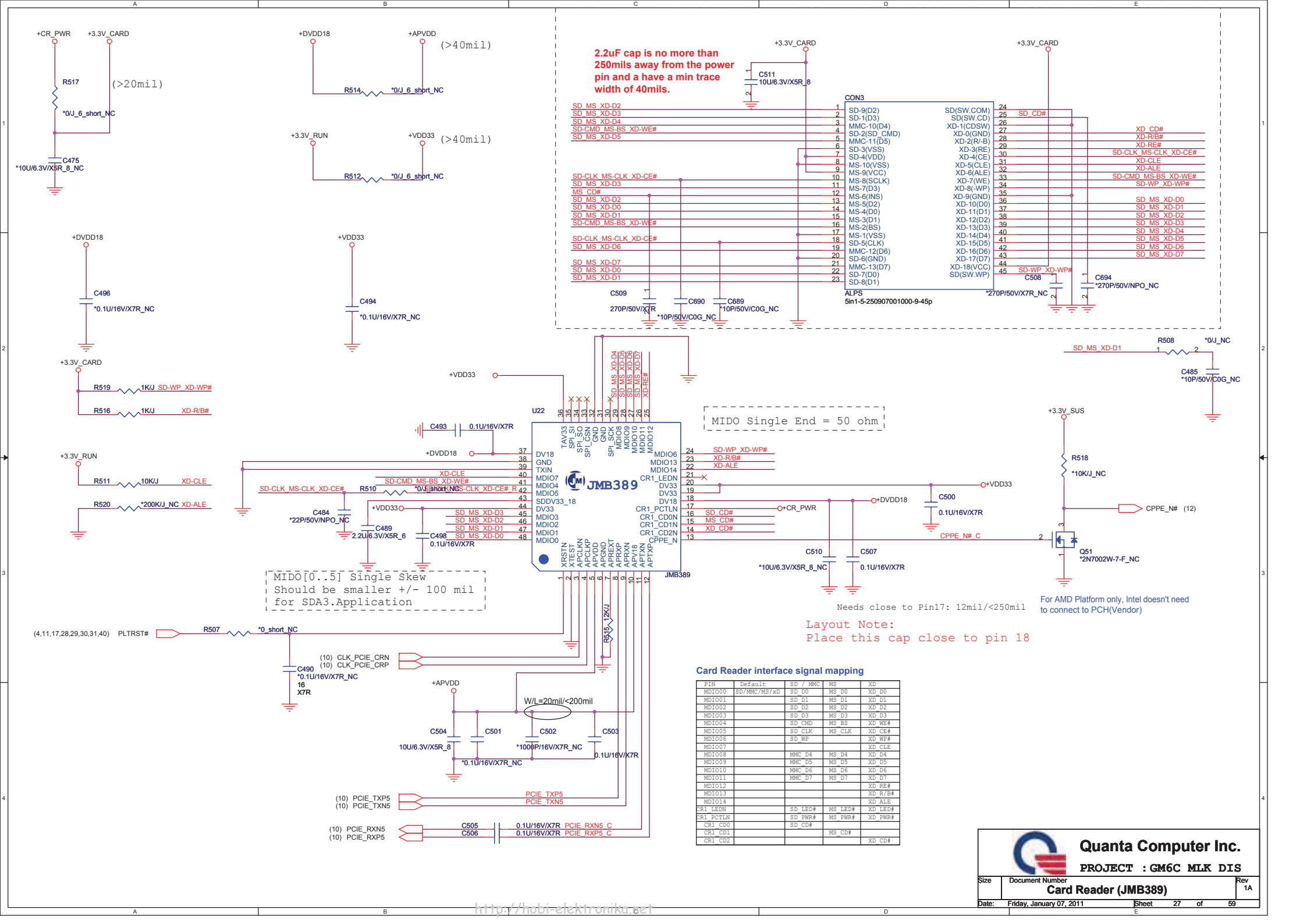

Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

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BX1 leakage issue workaround circuit
R96,C104 no stuff,R100 stuff
BX2 will close it.
R96,C104 stuff,R100 no stuff

Layout Note: Place these caps close to ITE8502

Layout Note: Place PC169 close to ITE8502

IT8518E/CX

prochot pin level shift

Board ID Straps

Config_0	Config_1	GM6/GM6C
0	0	UMA
0	1	Optimum-GE
1	0	Studio Discrete
1	1	Optimum-GS

USB_BACK_EN#	BID1	GM6/GM6C
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	QT (A00)
0	0	(A01)

Quanta Computer Inc.
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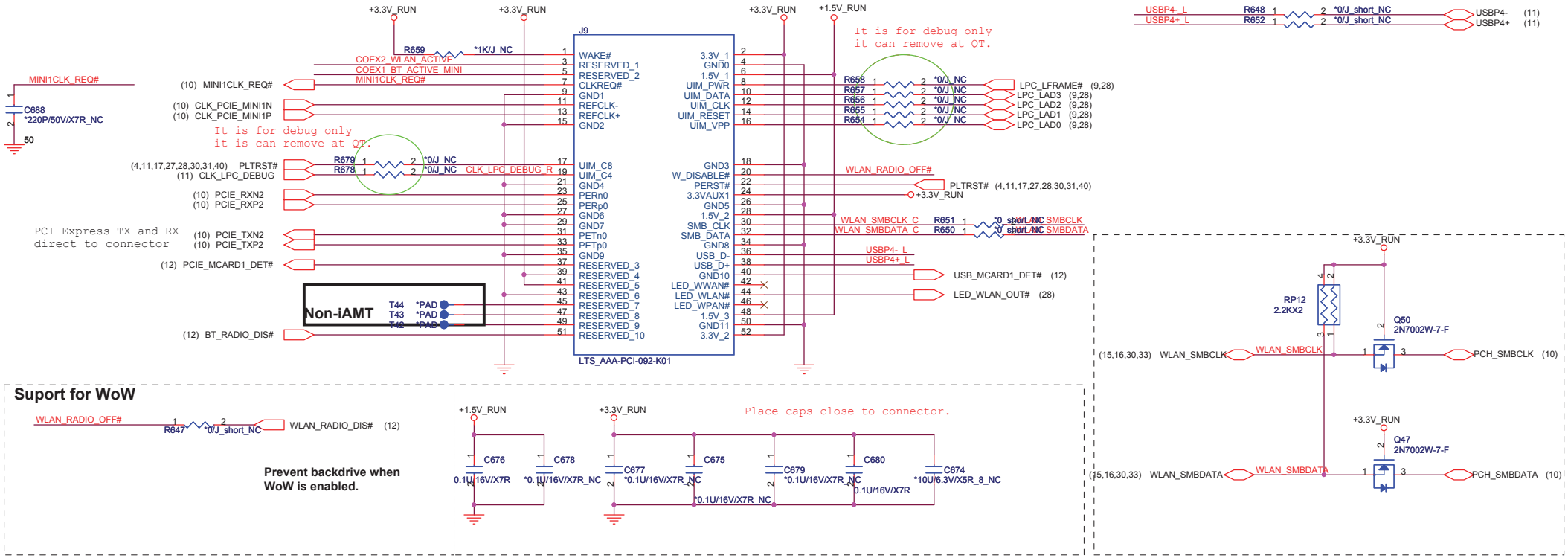
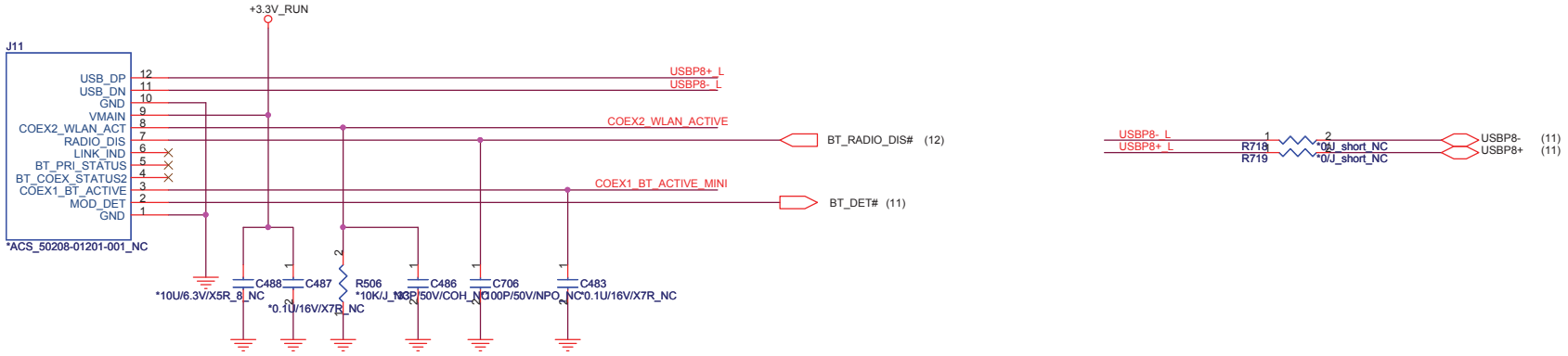
MiniCard WLAN connector



Suport for WoW

Support Dell BT375 (Little Stone) module (XPS) W TO B



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: MINI-Card (WLAN/WPAN)	Rev 1A
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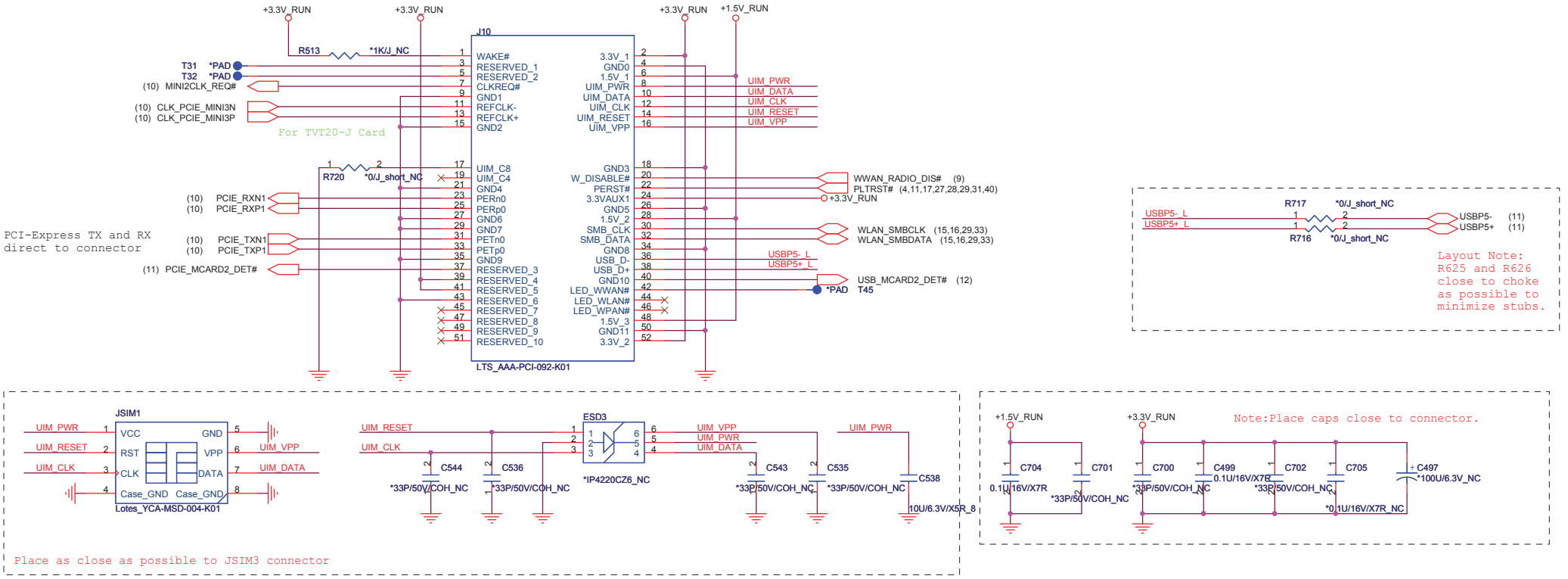
MiniCard WWAN connector



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	MINI-Card (WWAN)	1A
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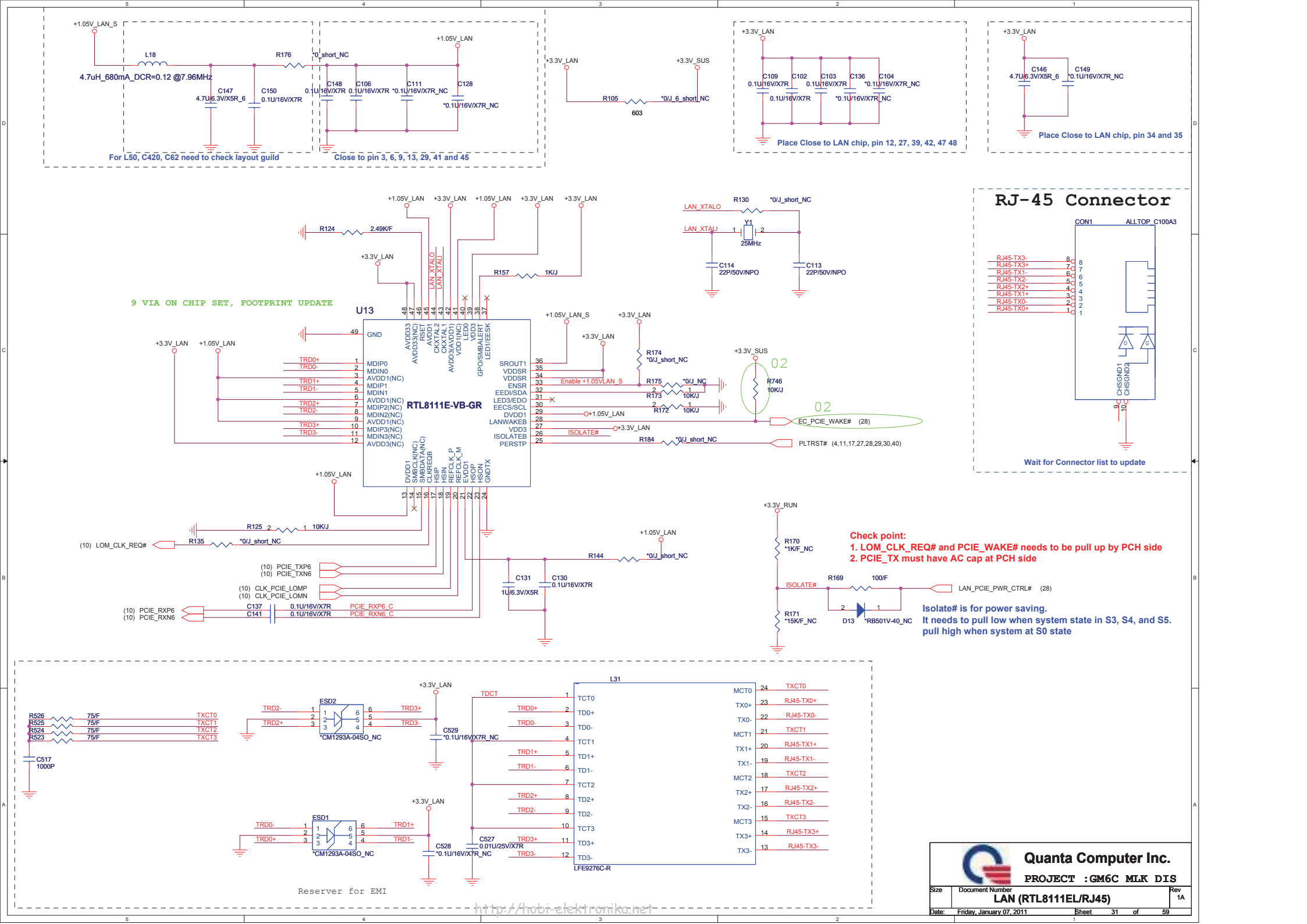
+1.05V_LAN_S
L18
4.7uH_680mA_DCR=0.12 @7.96MHz
R176
*0_short_NC
+1.05V_LAN
C147
4.7U/6.3V/X5R_6
C150
0.1U/16V/X7R
C148
0.1U/16V/X7R
C106
0.1U/16V/X7R
C111
*0.1U/16V/X7R_NC
C128
*0.1U/16V/X7R_NC
For L50, C420, C62 need to check layout guild
Close to pin 3, 6, 9, 13, 29, 41 and 45
+3.3V_LAN
R105
603
+3.3V_SUS
*0/J_6_short_NC
+3.3V_LAN
C109
0.1U/16V/X7R
C102
0.1U/16V/X7R
C103
0.1U/16V/X7R
C136
0.1U/16V/X7R
C104
*0.1U/16V/X7R_NC
Place Close to LAN chip, pin 12, 27, 39, 42, 47 48
+3.3V_LAN
C146
4.7U/6.3V/X5R_6
C149
*0.1U/16V/X7R_NC
Place Close to LAN chip, pin 34 and 35
RJ-45 Connector
CON1
ALLTOP_C100A3
RJ45-TX3-
RJ45-TX3+
RJ45-TX1-
RJ45-TX2-
RJ45-TX2+
RJ45-TX1+
RJ45-TX0-
RJ45-TX0+
CHSGND1
CHSGND2
Wait for Connector list to update
9 VIA ON CHIP SET, FOOTPRINT UPDATE
U13
RTL8111E-VB-GR
+1.05V_LAN
+3.3V_LAN
R124
2.49K/F
R157
1K/J
LAN_XTALO
LAN_XTALI
R130
*0/J_short_NC
Y1
25MHz
C114
22P/50V/NPO
C113
22P/50V/NPO
+1.05V_LAN_S
R174
*0/J_short_NC
Enable +1.05VLAN_S
R175
*0/J_NC
R173
10K/J
R172
10K/J
+3.3V_SUS
R746
10K/J
02
EC_PCIE_WAKE# (28)
ISOLATE#
R184
*0/J_short_NC
PLTRST# (4,11,17,27,28,29,30,40)
R125
10K/J
R135
*0/J_short_NC
(10) LOM_CLK_REQ#
(10) PCIE_TXP6
(10) PCIE_TXN6
(10) CLK_PCIE_LOMP
(10) CLK_PCIE_LOMN
(10) PCIE_RXP6
(10) PCIE_RXN6
C137
0.1U/16V/X7R
C141
0.1U/16V/X7R
PCIE_RXP6_C
PCIE_RXN6_C
C131
1U/6.3V/X5R
C130
0.1U/16V/X7R
R144
*0/J_short_NC
+3.3V_RUN
R170
*1K/F_NC
R171
*15K/F_NC
ISOLATE#
R169
100/F
LAN_PCIE_PWR_CTRL# (28)
D13
*RB501V-40_NC
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needs to be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side
Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state
R526
R525
R524
R523
75/F
TXCT0
TXCT1
TXCT2
TXCT3
C517
1000P
ESD2
*CM1293A-04SO_NC
TRD2-
TRD2+
TRD3+
TRD3-
C529
*0.1U/16V/X7R_NC
ESD1
*CM1293A-04SO_NC
TRD0-
TRD0+
TRD1+
TRD1-
C528
*0.1U/16V/X7R_NC
C527
0.01U/25V/X7R
L31
LFE9276C-R
TDCT
TCT0
TD0+
TD0-
TCT1
TD1+
TD1-
TCT2
TD2+
TD2-
TCT3
TD3+
TD3-
MCT0
TX0+
TX0-
MCT1
TX1+
TX1-
MCT2
TX2+
TX2-
MCT3
TX3+
TX3-
TXCT0
RJ45-TX0+
RJ45-TX0-
TXCT1
RJ45-TX1+
RJ45-TX1-
TXCT2
RJ45-TX2+
RJ45-TX2-
TXCT3
RJ45-TX3+
RJ45-TX3-
Reserver for EMI
Quanta Computer Inc.
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LAN (RTL8111EL/RJ45)
Rev
1A
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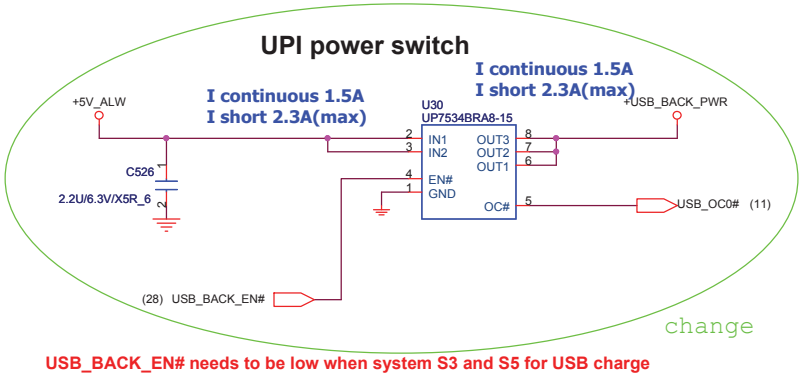
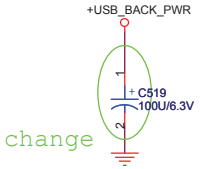
http://hobi-elektronika.net

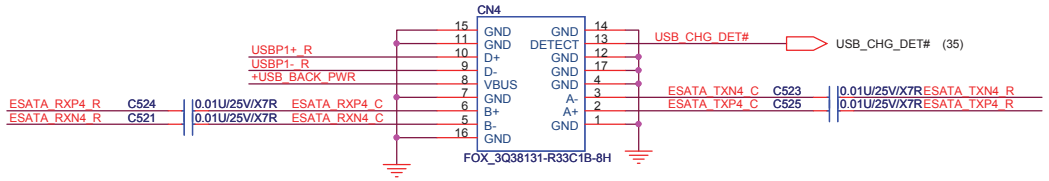
ESATA + USB Conn + Power Share

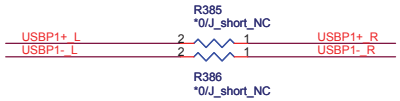


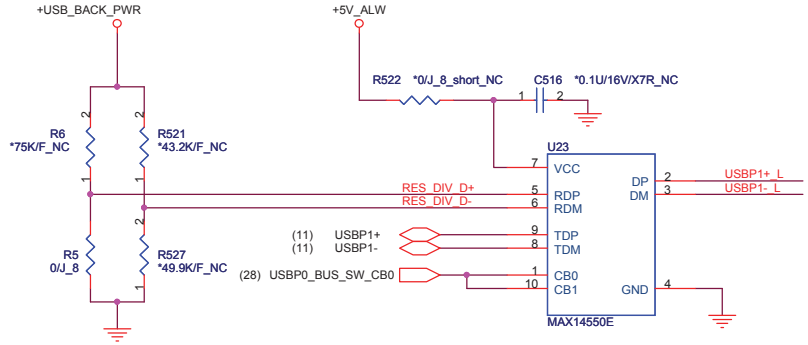
USB_BACK_EN# needs to be low when system S3 and S5 for USB charge



This pin connects to 3VALW ON POWER LOGIC







EC needs to drive CB0/CB1 pins to low
when system S3/S5 and dirve high when system S0.

U49 PN and Footprint needs to double check

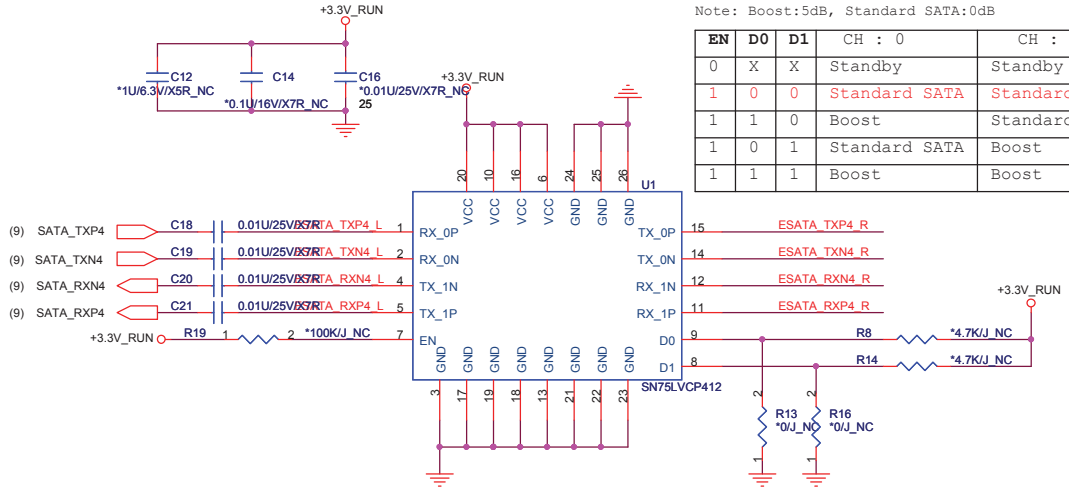
R15 needs to be 49.9K_F if we use external resisters.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

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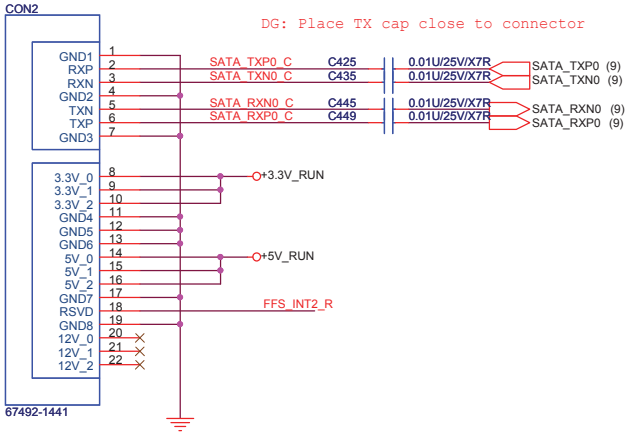
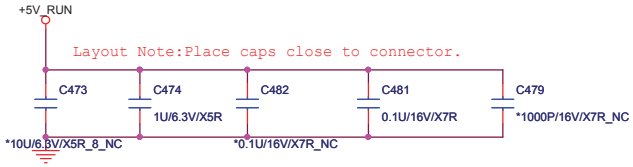
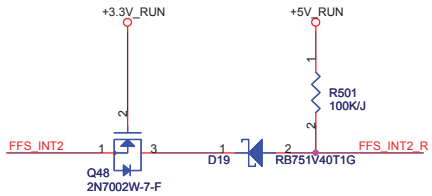
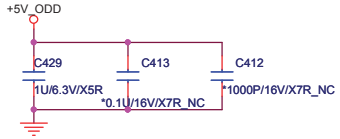
SATA Connector.

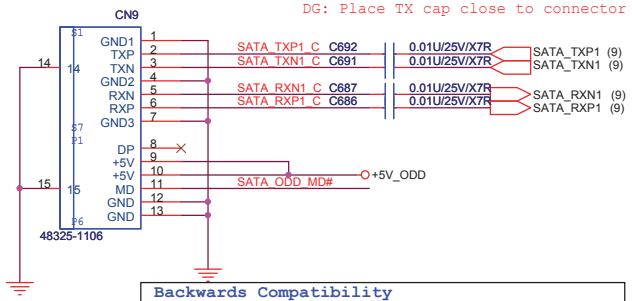




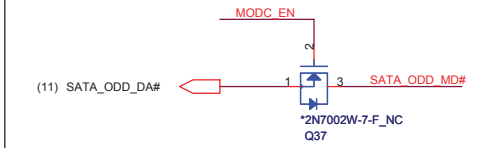


ODD Connector





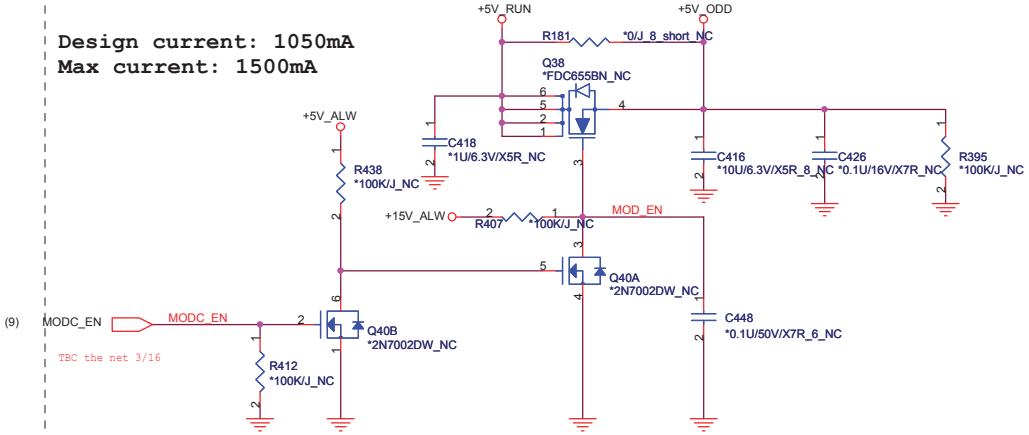
Backwards Compatibility



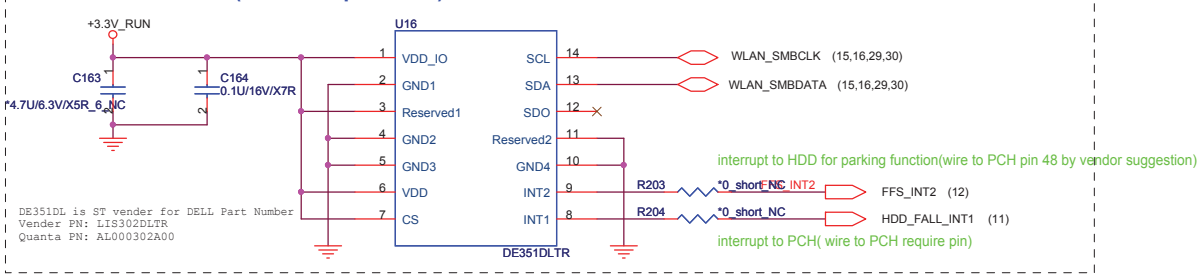
Drive powered on, MD# is High
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

Design current: 1050mA
Max current: 1500mA



3-axis Fall Sensor (HDD data protector)

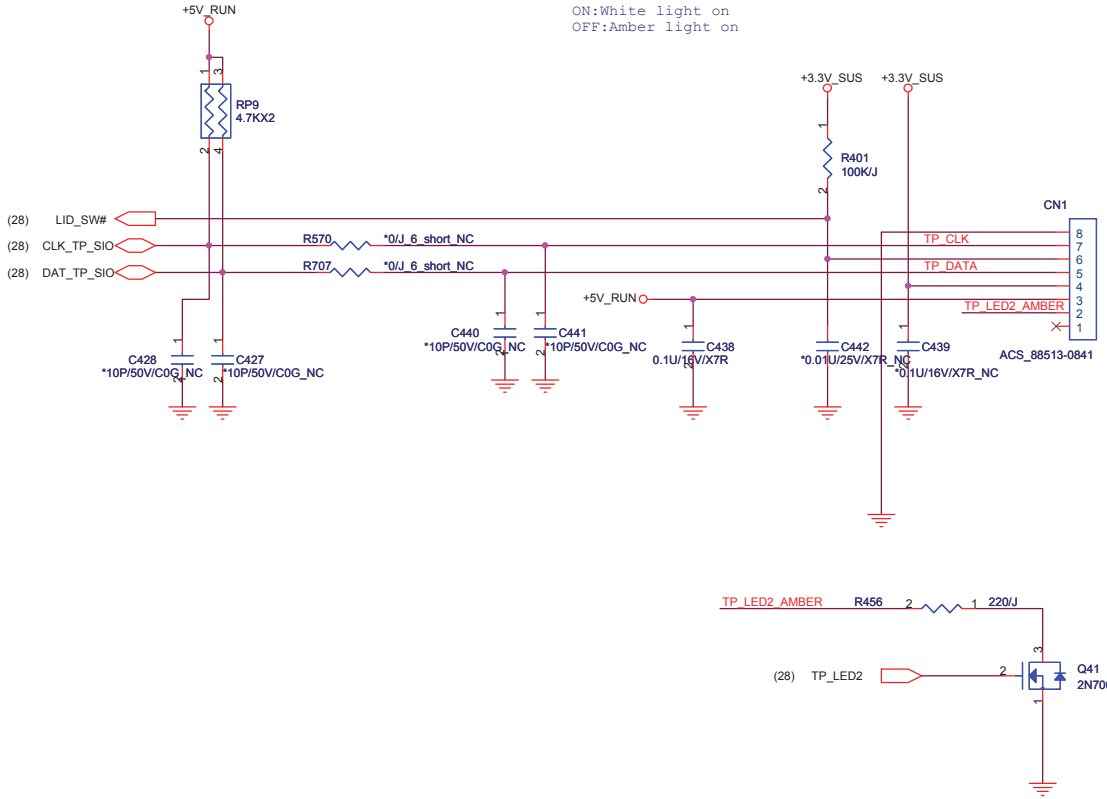


Quanta Computer Inc.
PROJECT : GM6C MLK DIS

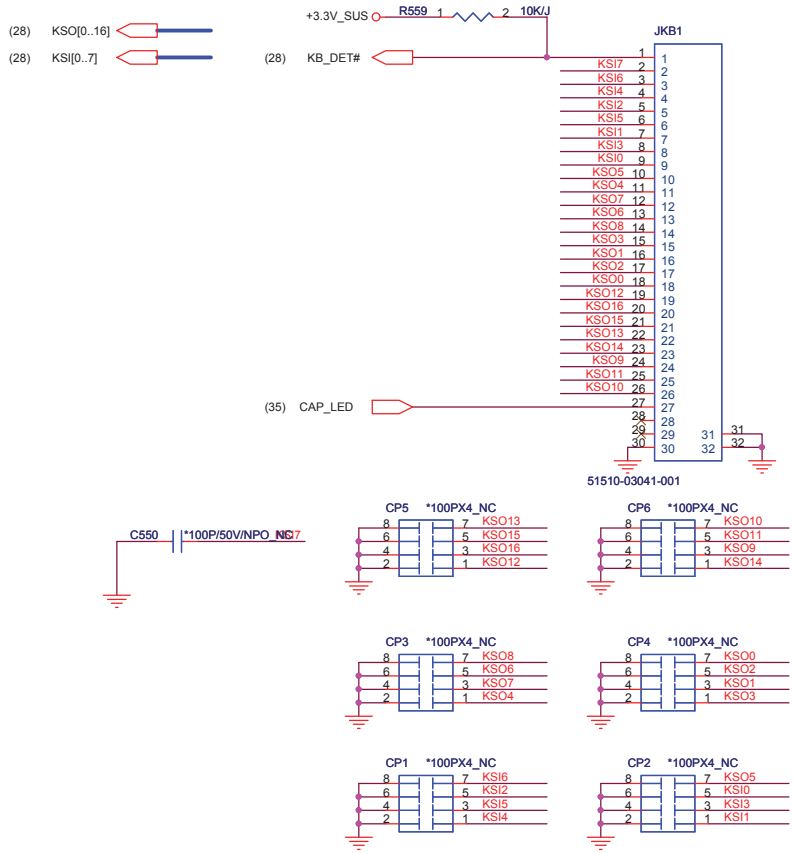
Size	Document Number	Rev
	SATA (HDD&ODD)	1A
Date: Friday, January 07, 2011	Sheet 33 of 59	

Touch Pad

ON:White light on
OFF:Amber light on



KEYBOARD CONNECTOR



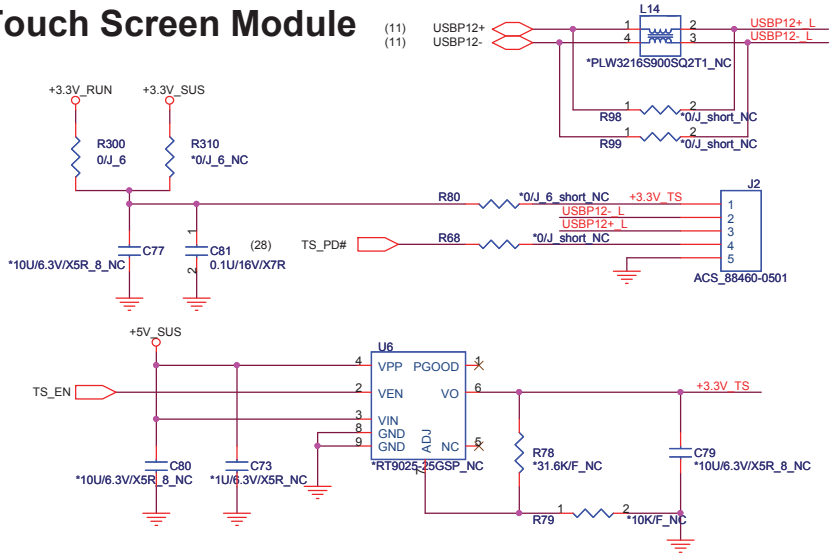
Layout Note: 100P CAPS CLOSE TO JKB3

Key board illumination

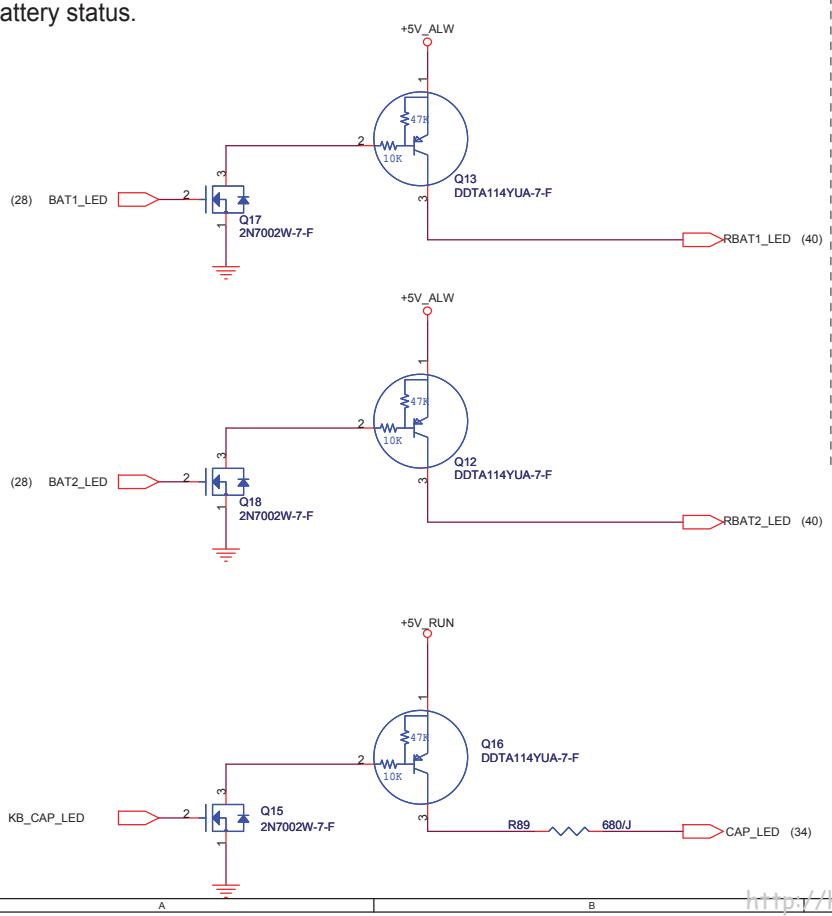
+KB_LED power trace width >10 mil

Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number TP/KB	Rev 1A
Date: Friday, January 07, 2011	Sheet 34 of 59	

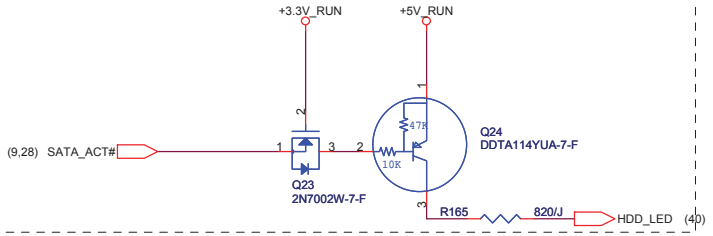
Touch Screen Module



Battery status.

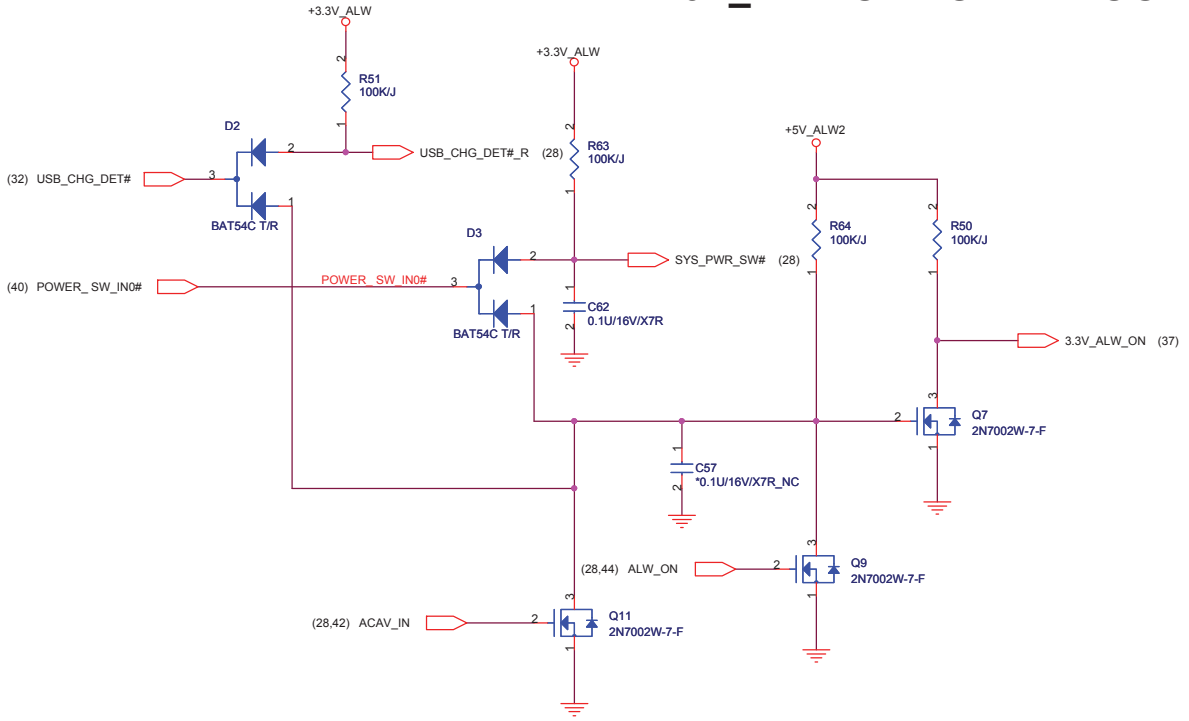


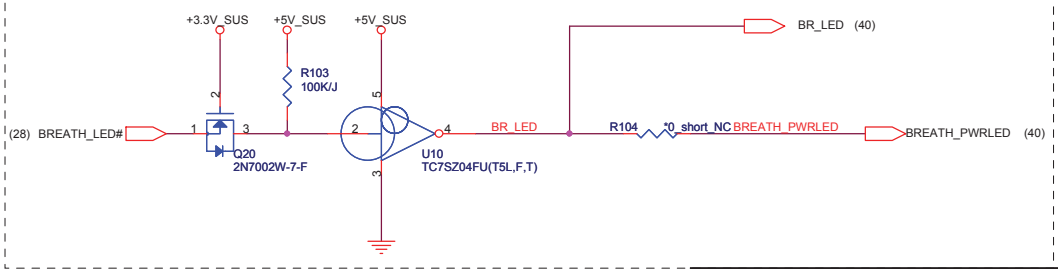
HDD activity LED.



Power button for Engineer

3V_ALW ON POWER LOGIC





Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	SWITCH/LED/T-Screen	1A
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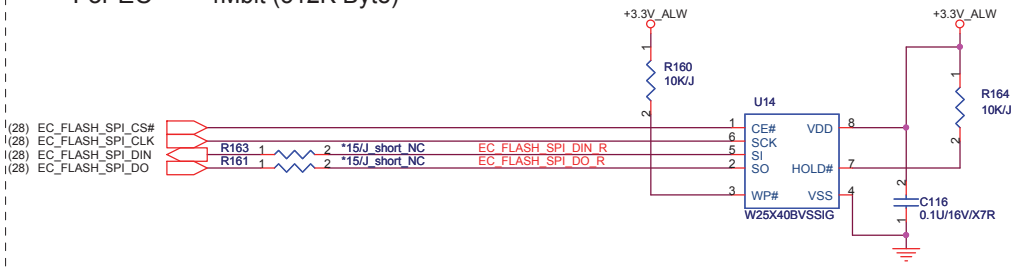
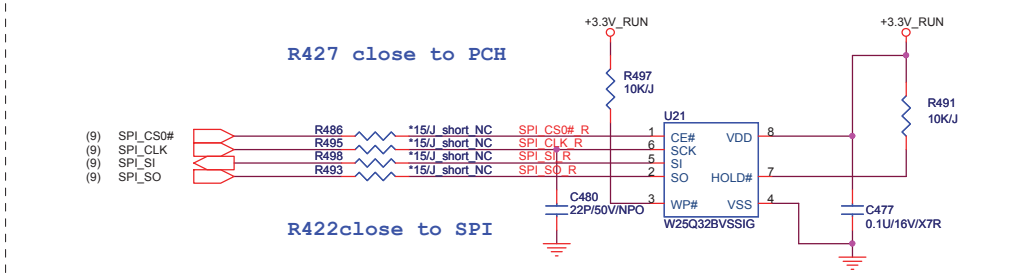
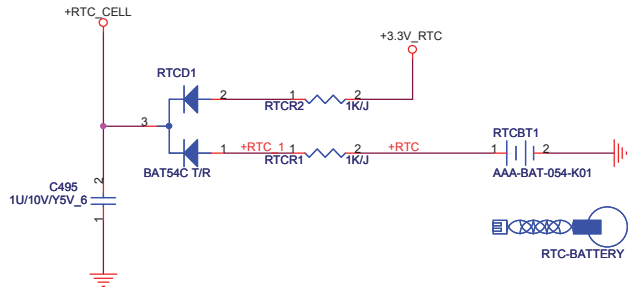
For EC 4Mbit (512K Byte)



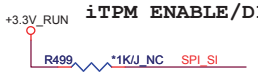
For PCH 32Mbit (4M Byte)



RTC BATTERY

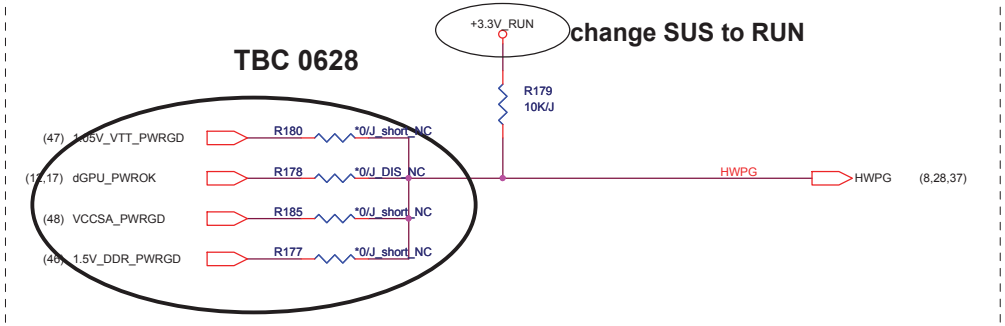


iTPM ENABLE/DISABLE

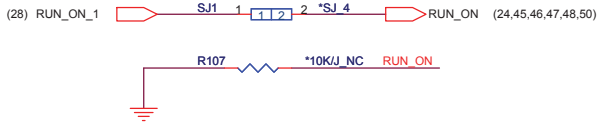


TPM Function	R428
Enable	Mount
Disable	NC (Default)

RESET CIRCUIT



delet VTT_POWERGOOD(07/12)



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	FLASH/RTC/RESET CIRCUIT	1A

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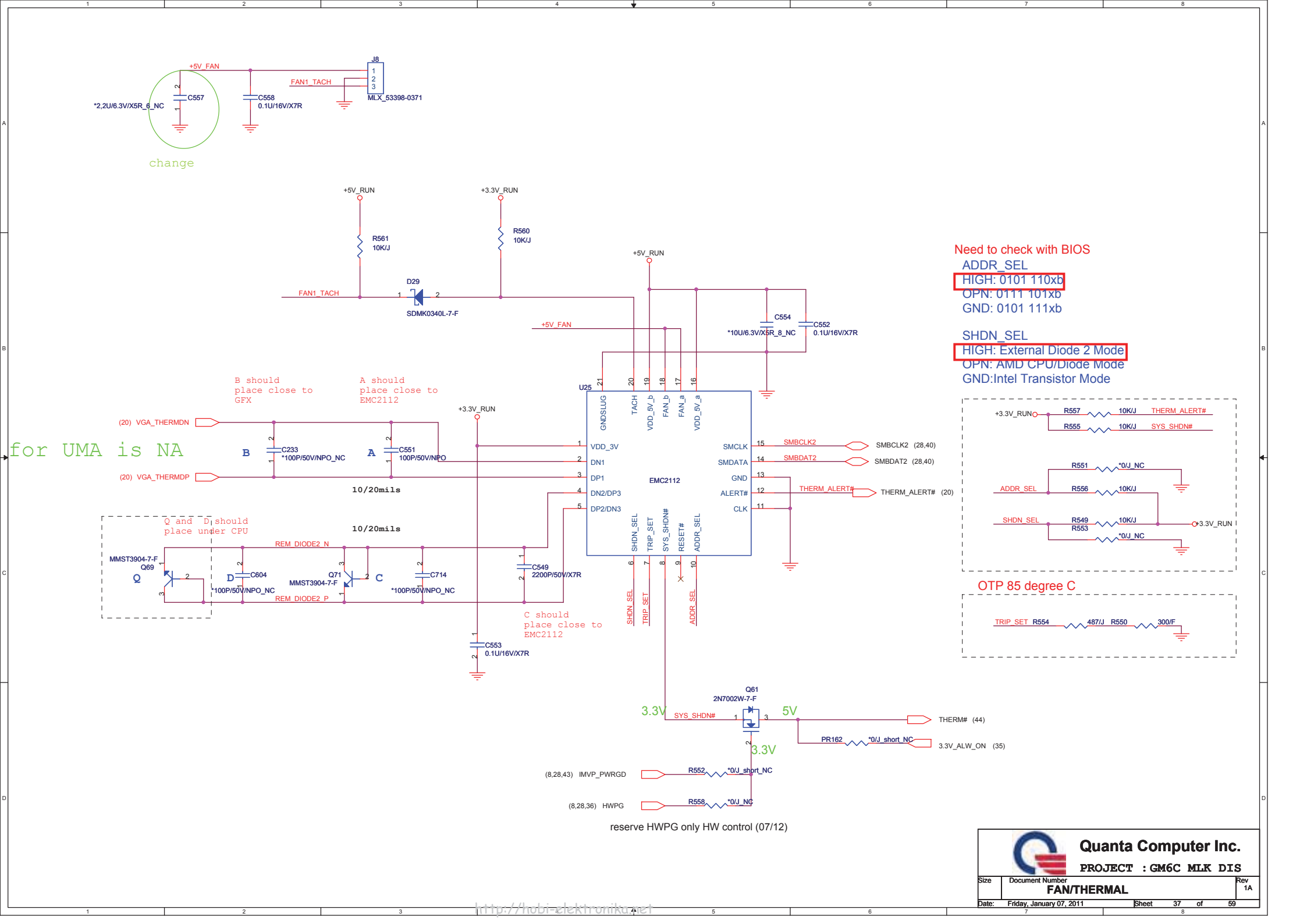
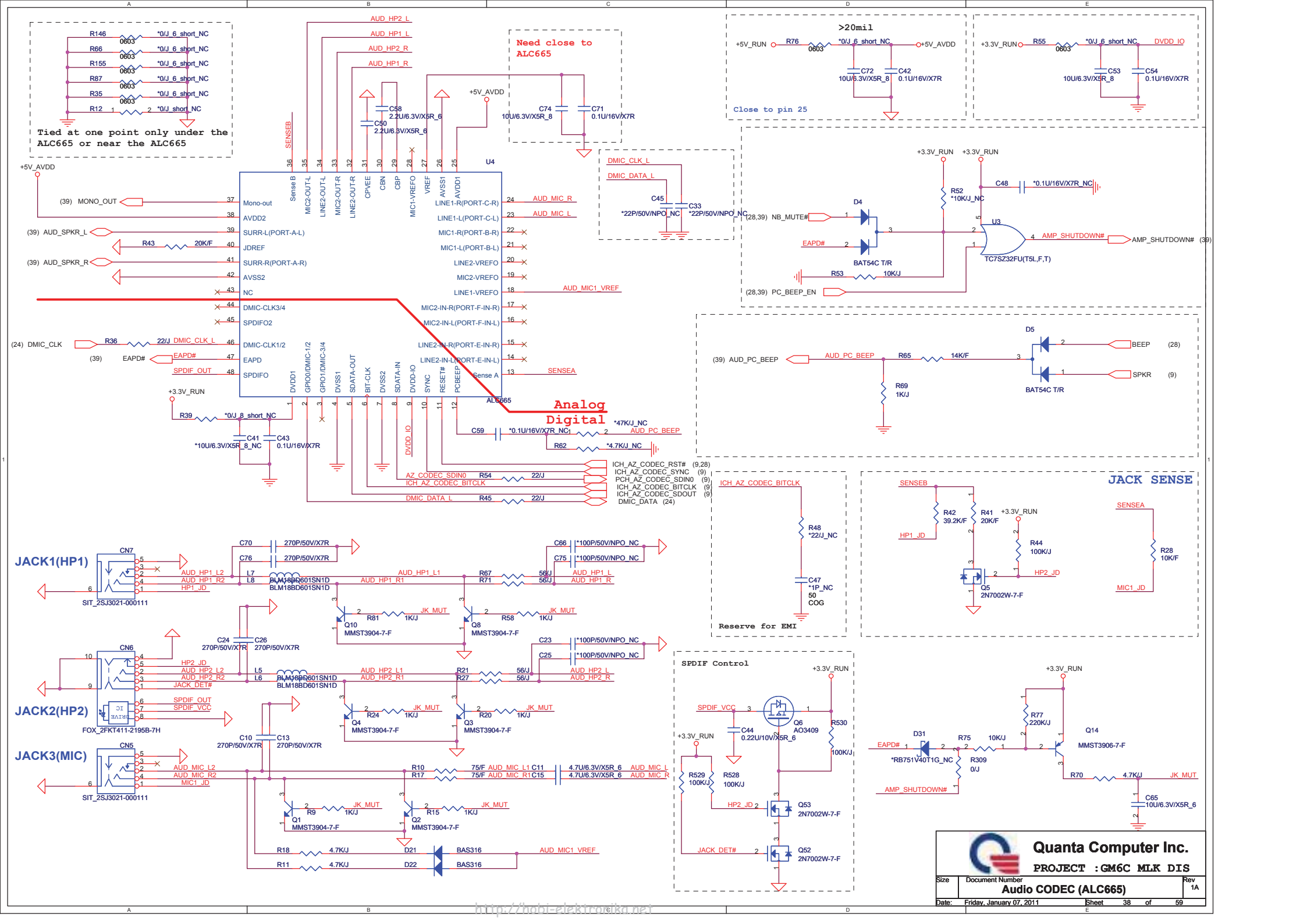


Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: FAN/THERMAL	Rev: 1A
Date: Friday, January 07, 2011	Sheet 37 of 59	


Tied at one point only under the ALC665 or near the ALC665
Need close to ALC665
>20mil
Close to pin 25
U4
ALC665
Analog
Digital
JACK1(HP1)
JACK2(HP2)
JACK3(MIC)
JACK SENSE
SPDIF Control
Reserve for EMI
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Audio CODEC (ALC665)
Date: Friday, January 07, 2011
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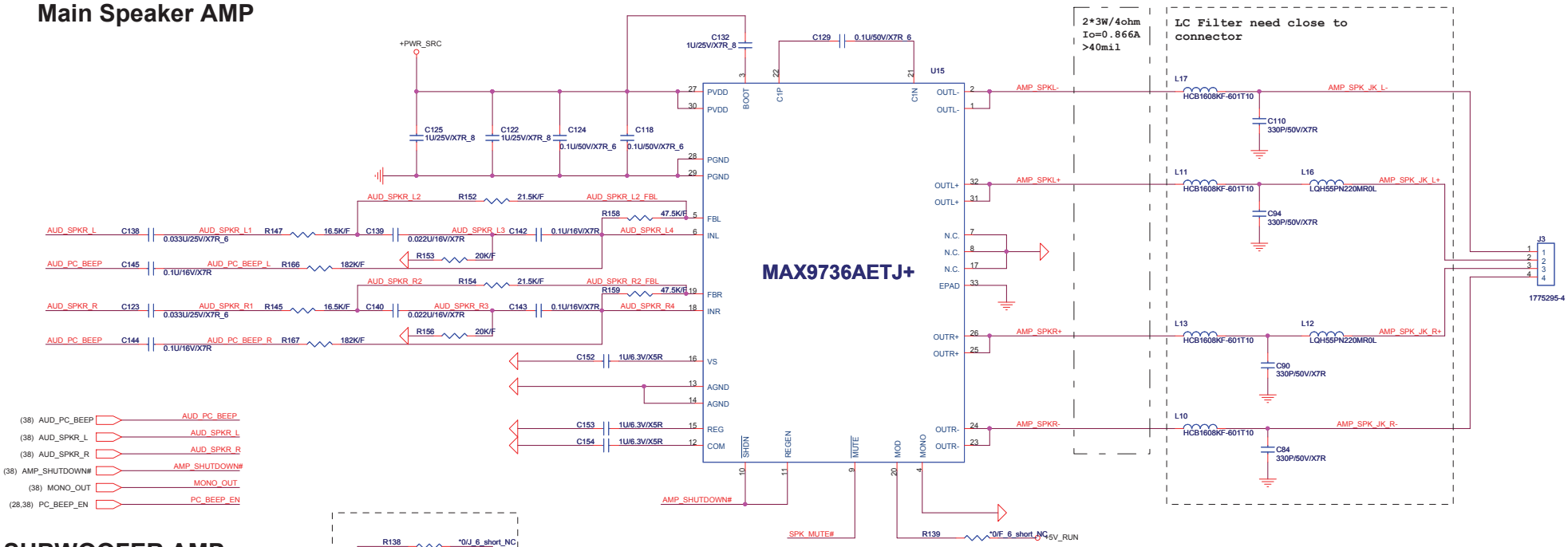
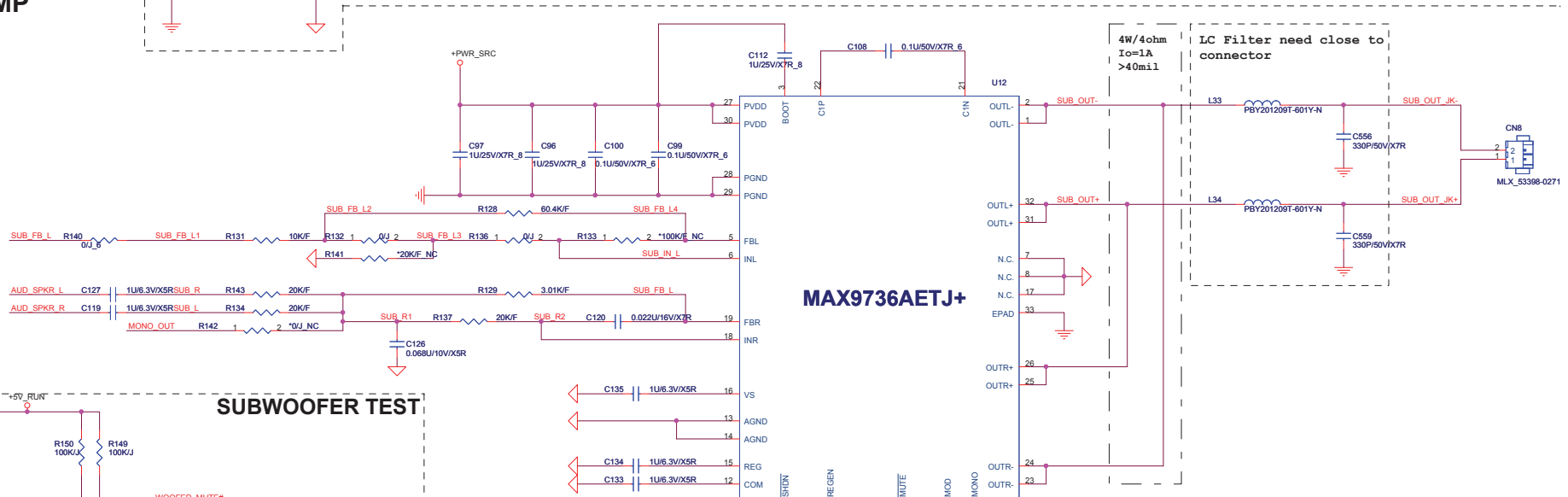
http://bobi-elektronika.net

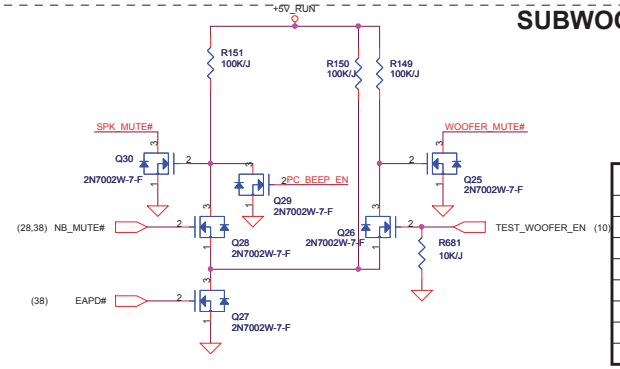
Main Speaker AMP



SUBWOOFER AMP



SUBWOOFER TEST



EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: Audio AMP (MAX9736A) | Rev 1A
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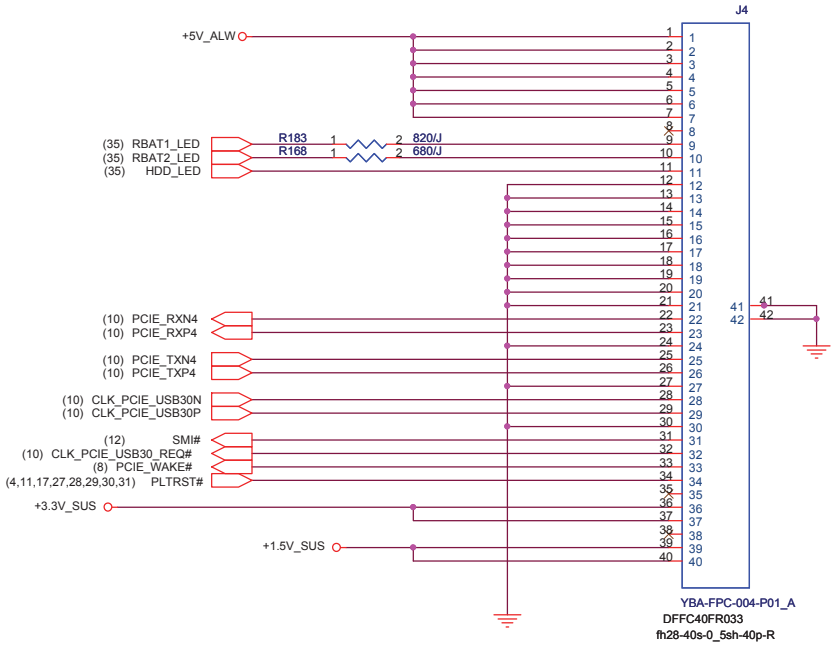
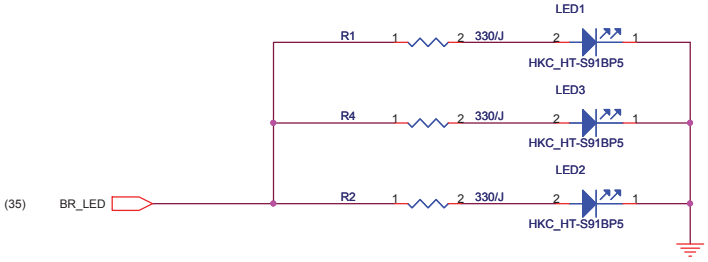
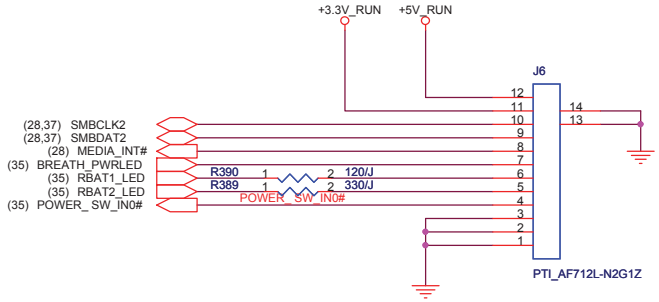




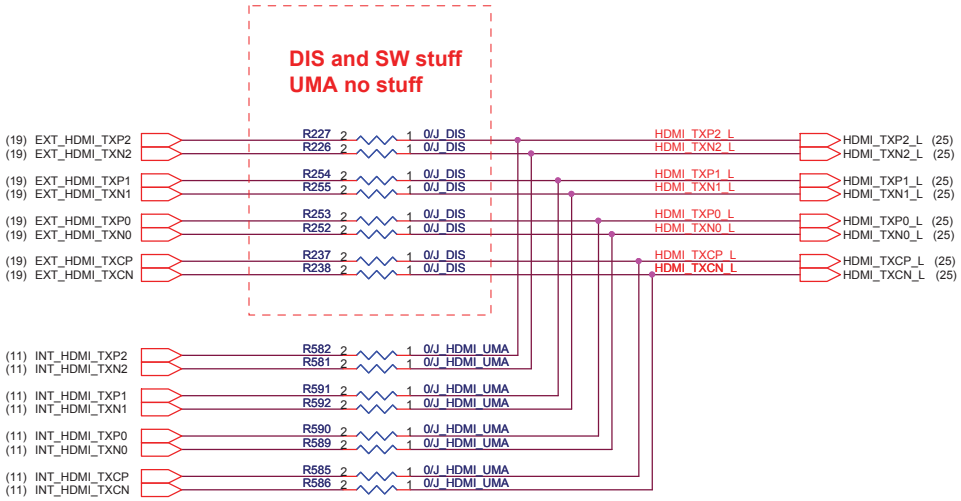


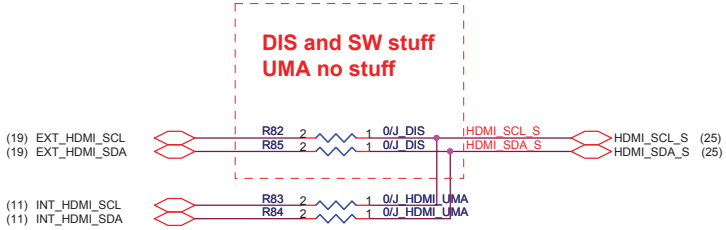
Quanta Computer Inc.

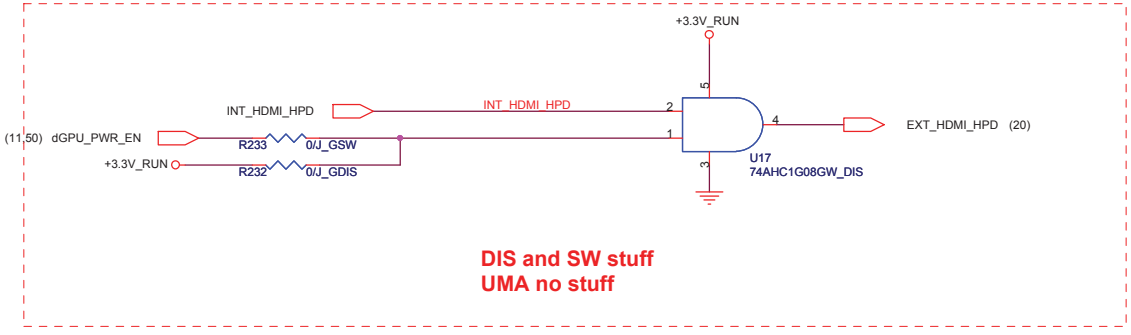
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Left USB/MMB CONN	1A
Date: Friday, January 07, 2011	Sheet 40 of 59	

HDMI Switch





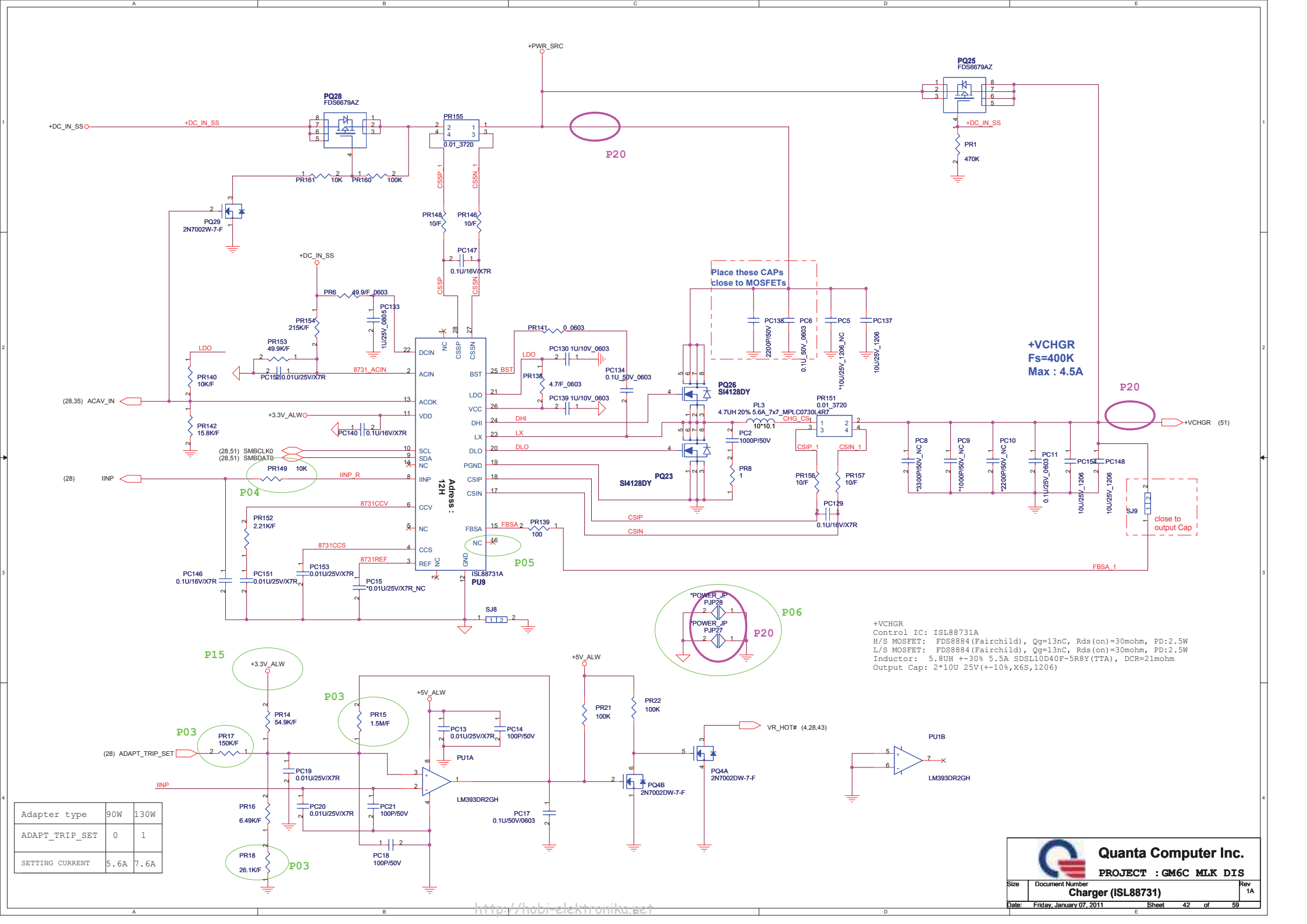


Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	BLANK	1A

Date: Friday, January 07, 2011 Sheet 41 of 59

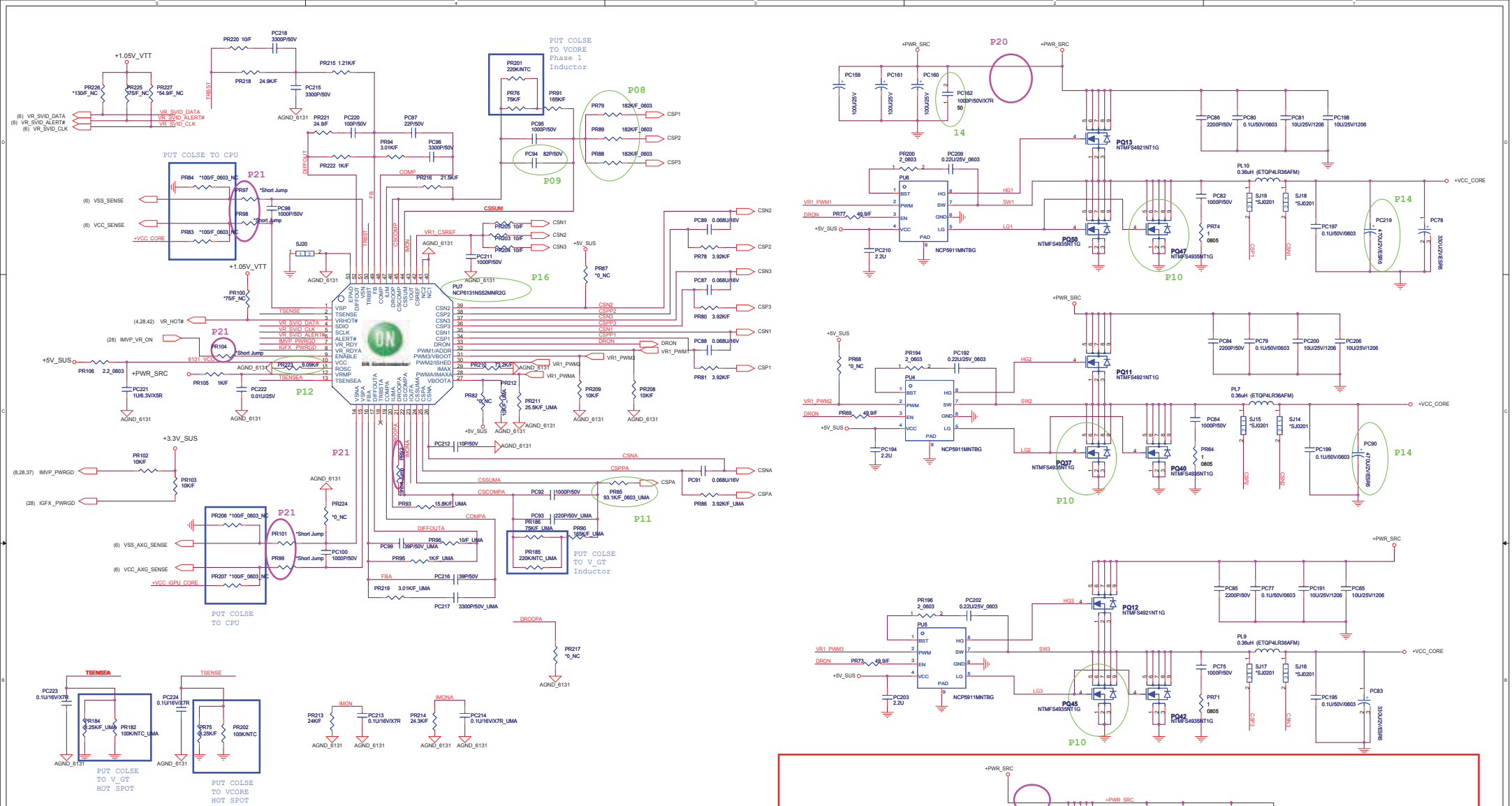


Adapter type	90W	130W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	5.6A	7.6A

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Charger (ISL88731)	1A
Date: Friday, January 07, 2011	Sheet 42 of 59	



Reference	Discrete	UMA	Optimus
PR82	0(CS00002JB38)	NC	NC
PC91	0(CS00002JB38)	0.068U/16V(CH3683K1B09)	0.068U/16V(CH3683K1B09)
PC92	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PC212	0(CS00002JB38)	10P/50V(CH01006JB08)	10P/50V(CH01006JB08)
PR217	0(CS00002JB38)	NC	NC
PC216	0(CS00002JB38)	39P/50V(CH03906JB06)	39P/50V(CH03906JB06)
PC100	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PR224	0(CS00002JB38)	NC	NC
PR214	0(CS00002JB38)	24.3K/F(CS32432FB19)	24.3K/F(CS32432FB19)
PC223	0(CS00002JB38)	0.1U/10V(CH4102K1B03)	0.1U/10V(CH4102K1B03)

	UMA	Optimus
PC180, C612	470uF CH747RM8800	330uF CH733RM8831

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
CPU_VCORE (NCP6131S)
Size | Document Number | Rev 1A
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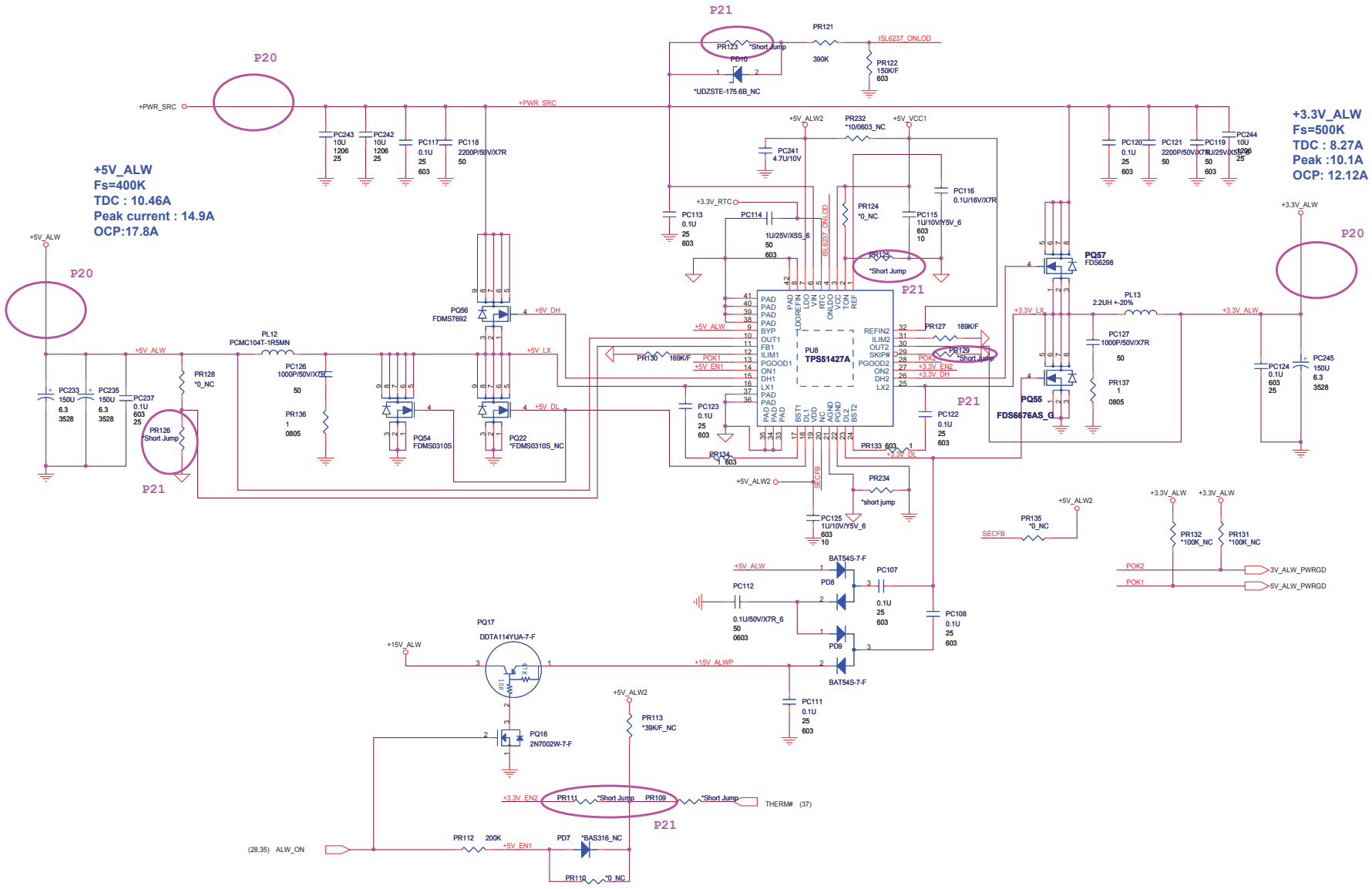

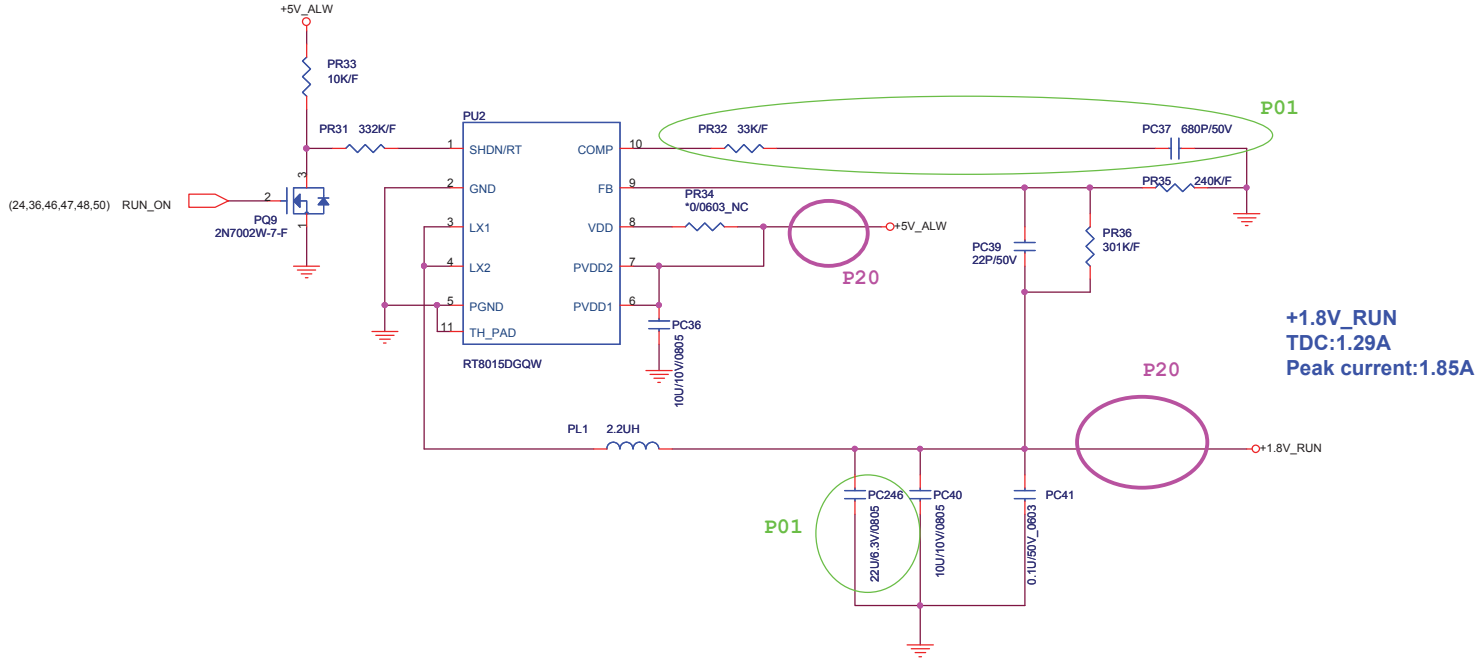

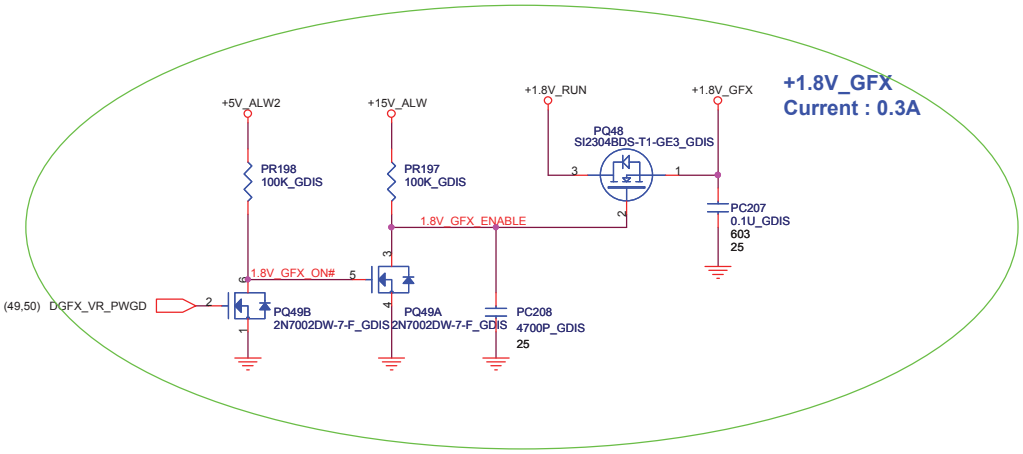

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	1.8V_RUN & 1.8V_RUN_GFX	1A

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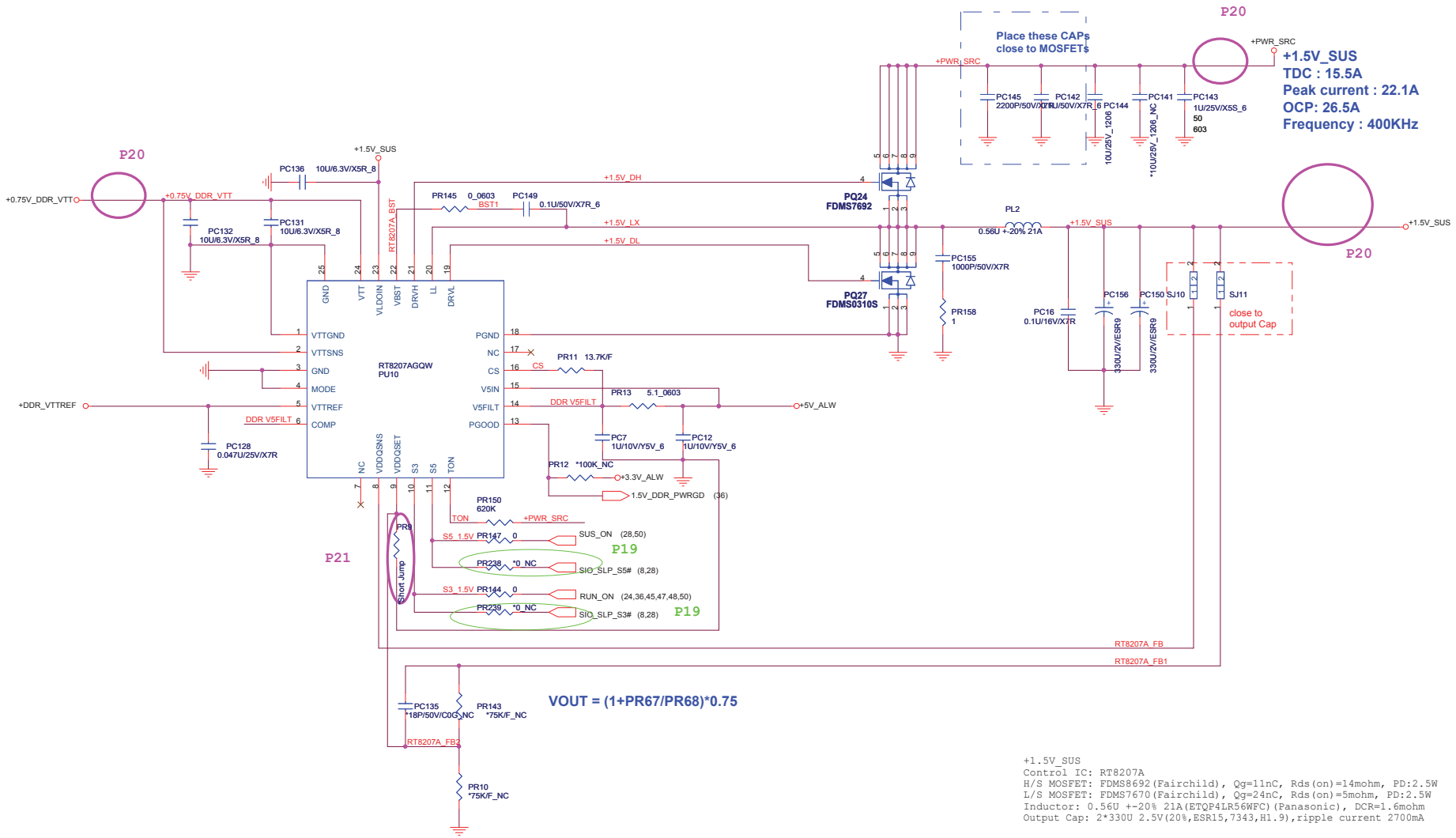

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: 1.5V_SUS & 0.75_DDR_VTT (RT8207) | Rev 1A
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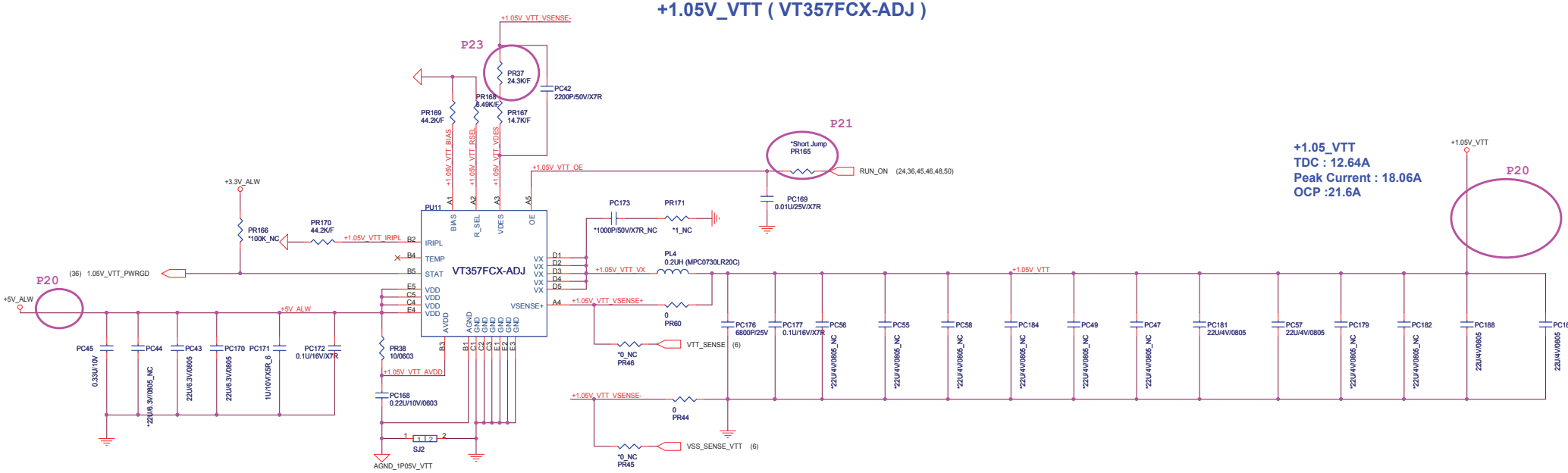
+1.05V_VTT (VT357FCX-ADJ)



Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE-
as differential pair

Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number		Rev
	1.05V_VTT		1A
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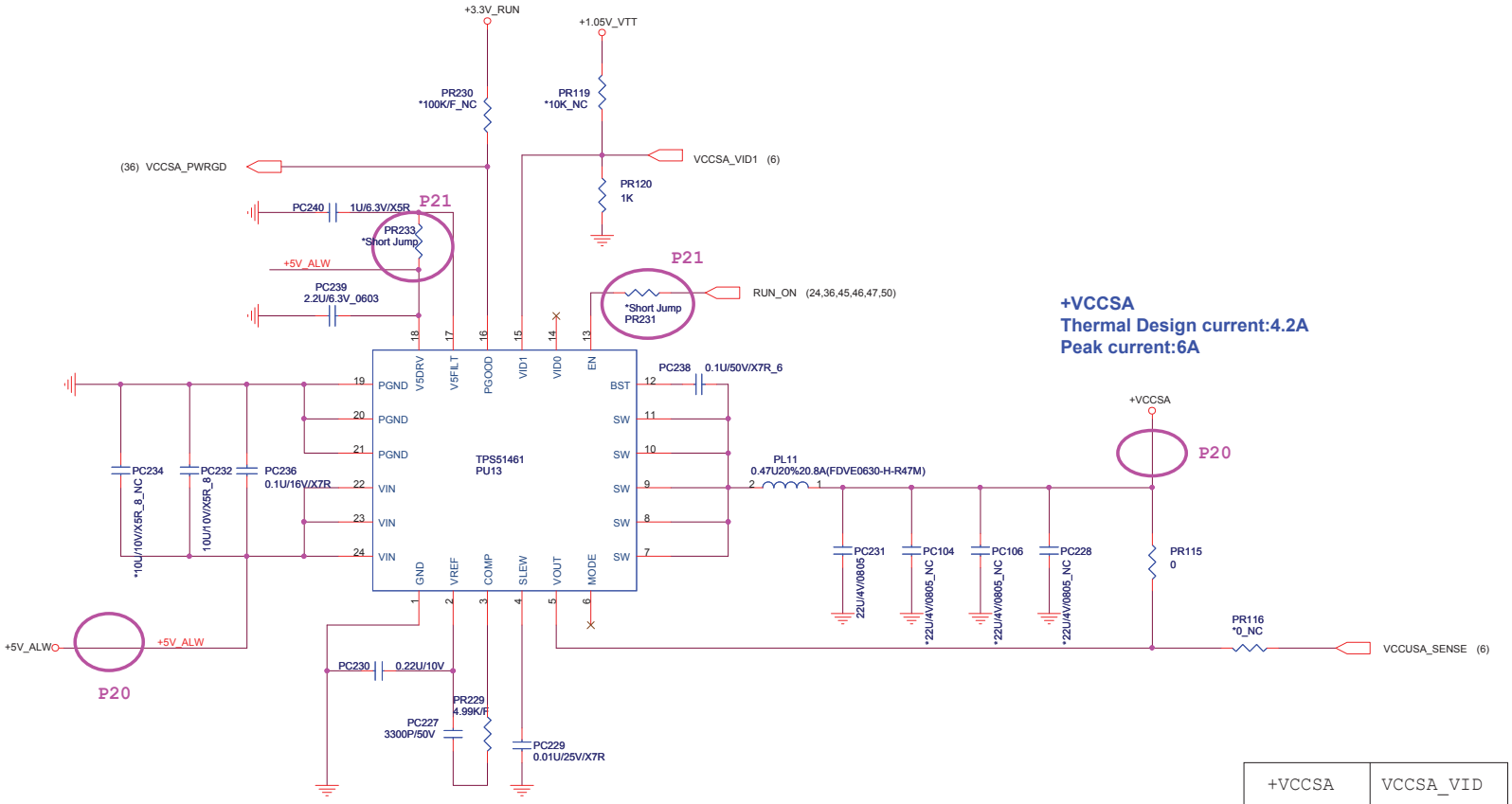

+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	VCCSA (TPS51461)	1A

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N12P-GE:

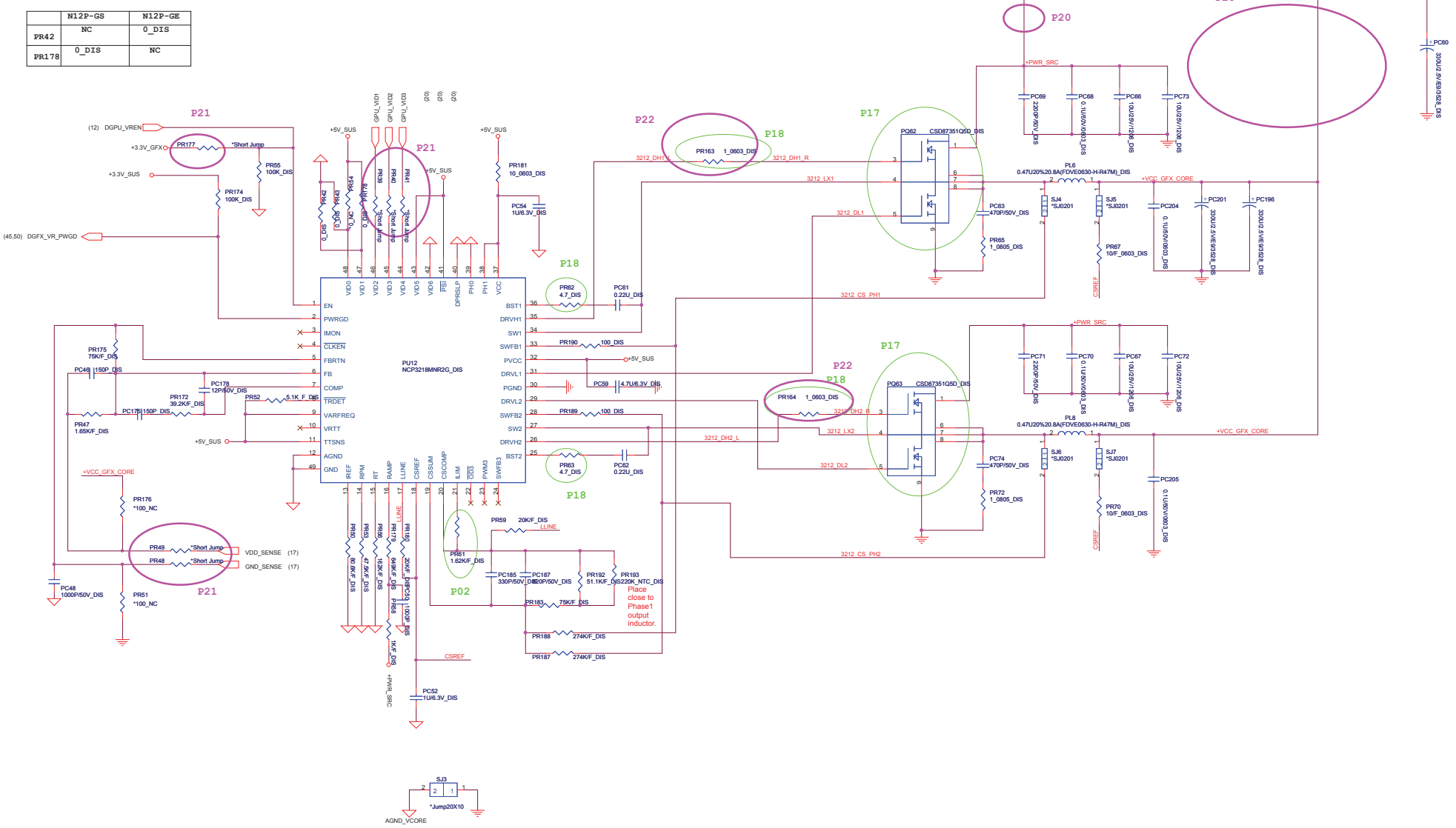
	GPU_VID3	GPU_VID2	GPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

N12P-GS:

	GPU_VID3	GPU_VID2	GPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

	N12P-GS	N12P-GE
PR42	NC	0_DIS
PR178	0_DIS	NC

+VCC_GFX_CORE
Fs=300K
Current:21.81A
OCP:52A



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	VGA_N11P-dGFX (NCP3218MNR2G)	1A

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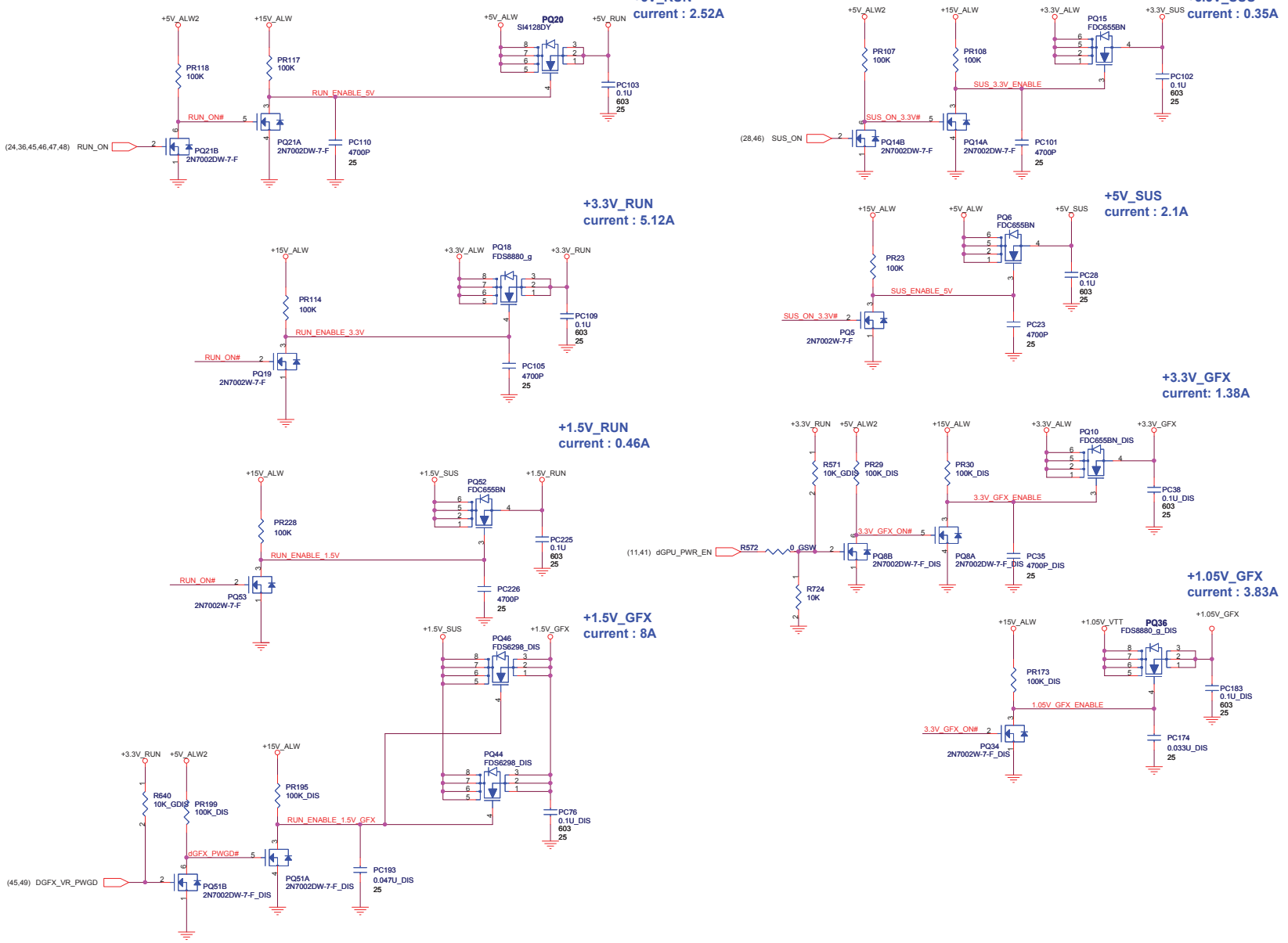
+5V_RUN
current : 2.52A
+3.3V_SUS
current : 0.35A
+3.3V_RUN
current : 5.12A
+5V_SUS
current : 2.1A
+3.3V_GFX
current: 1.38A
+1.5V_RUN
current : 0.46A
+1.5V_GFX
current : 8A
+1.05V_GFX
current : 3.83A
Reserve discharge path
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Run Power Switch
Rev 1A
Date: Friday, January 07, 2011
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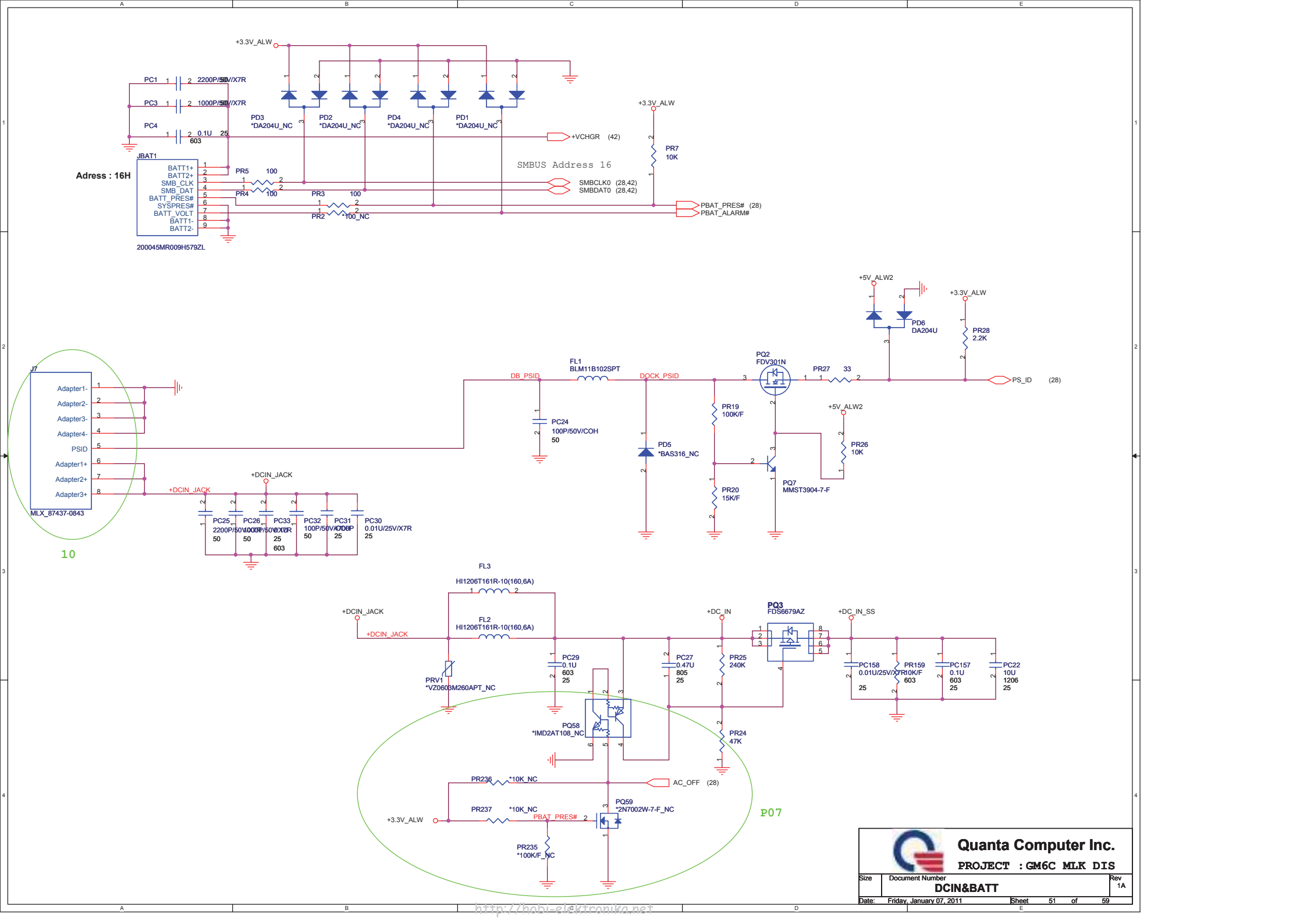
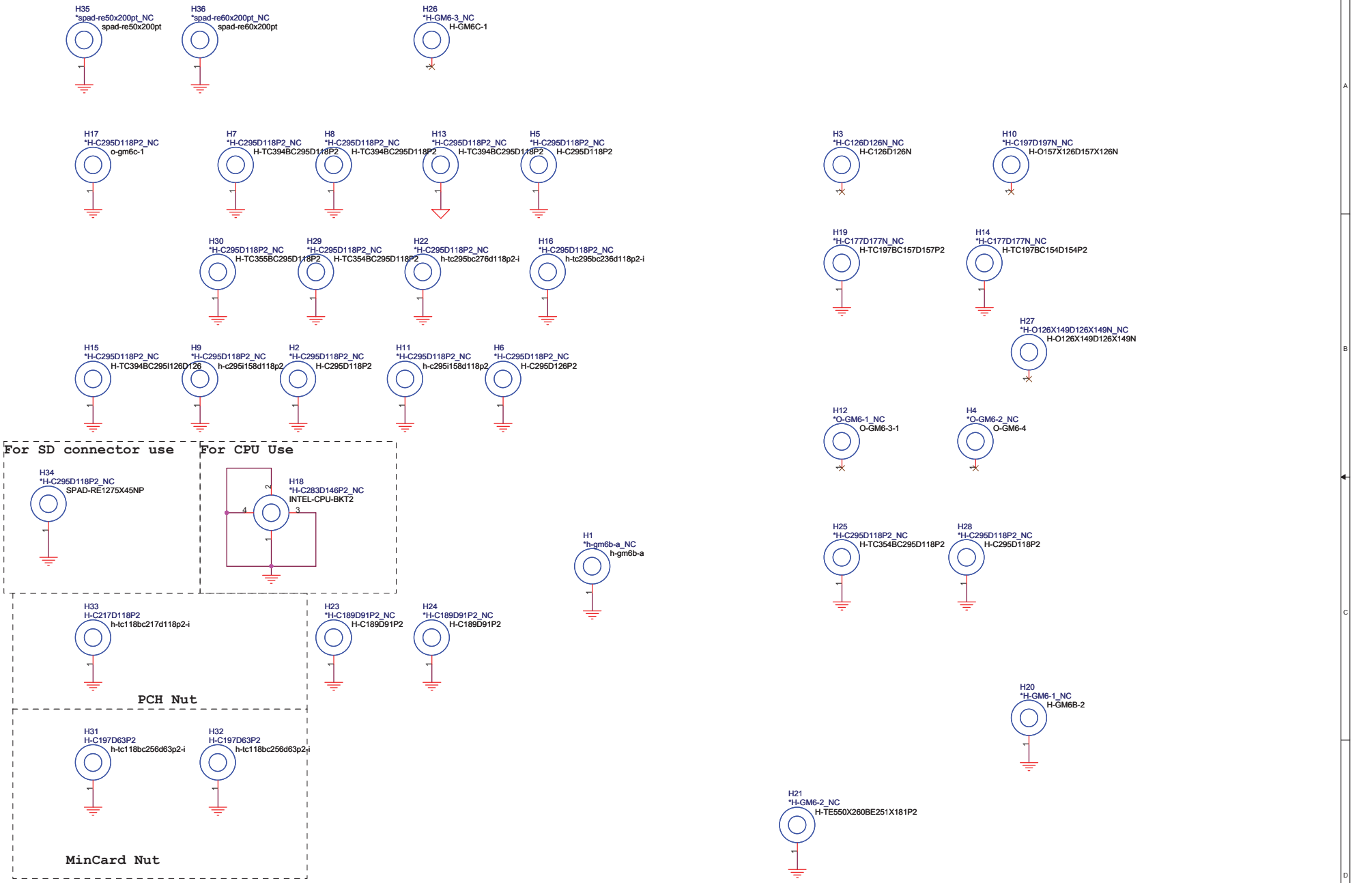
http://hobi-elektronika.net





Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: PAD & SCREW	Rev: 1A
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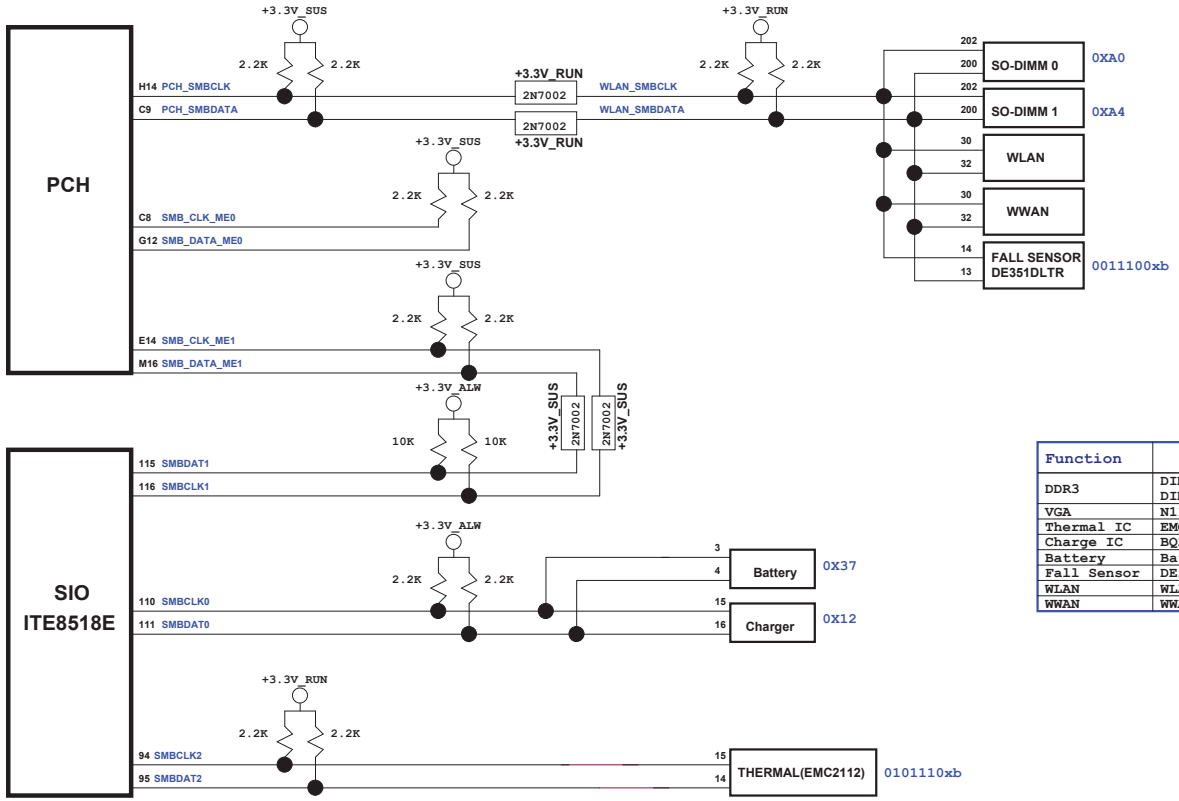

Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC2112	0011100xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0X37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X

Quanta Computer Inc.
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Size | Document Number: SMBUS | Rev 1A
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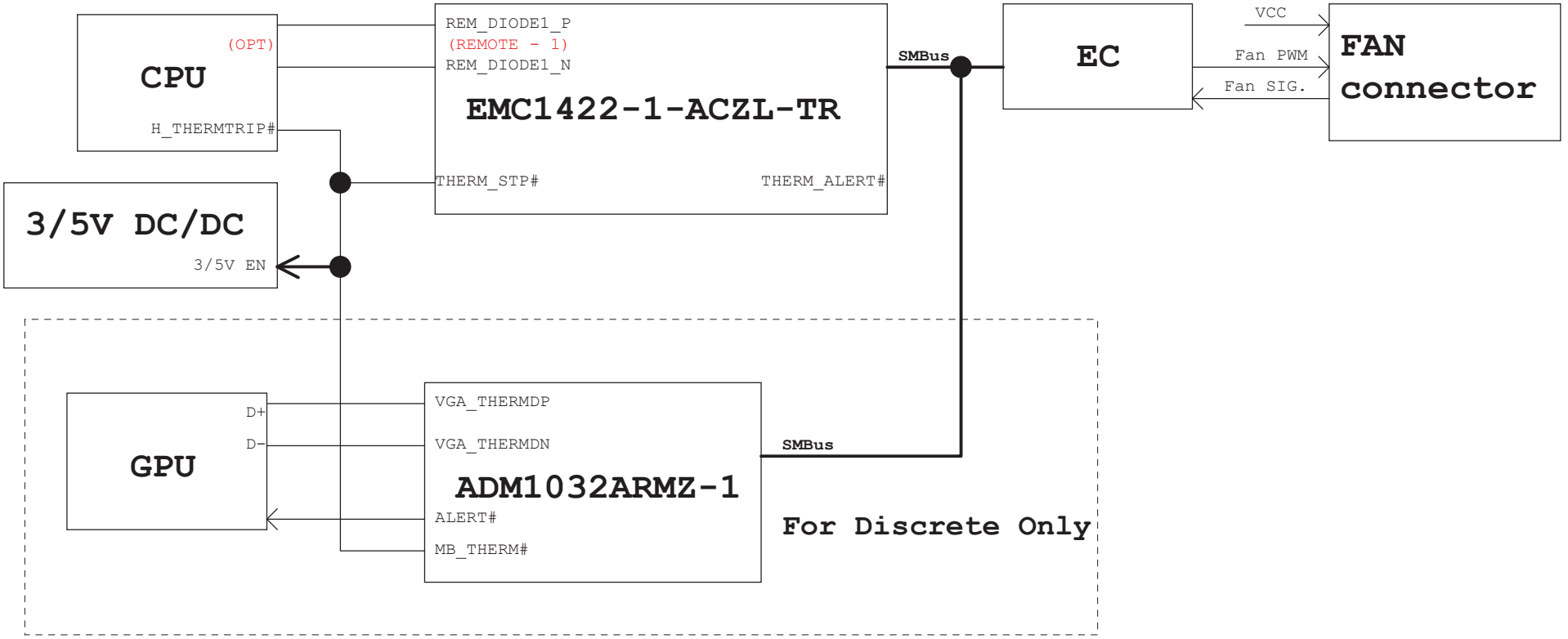

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	THERMAL MAP	1A

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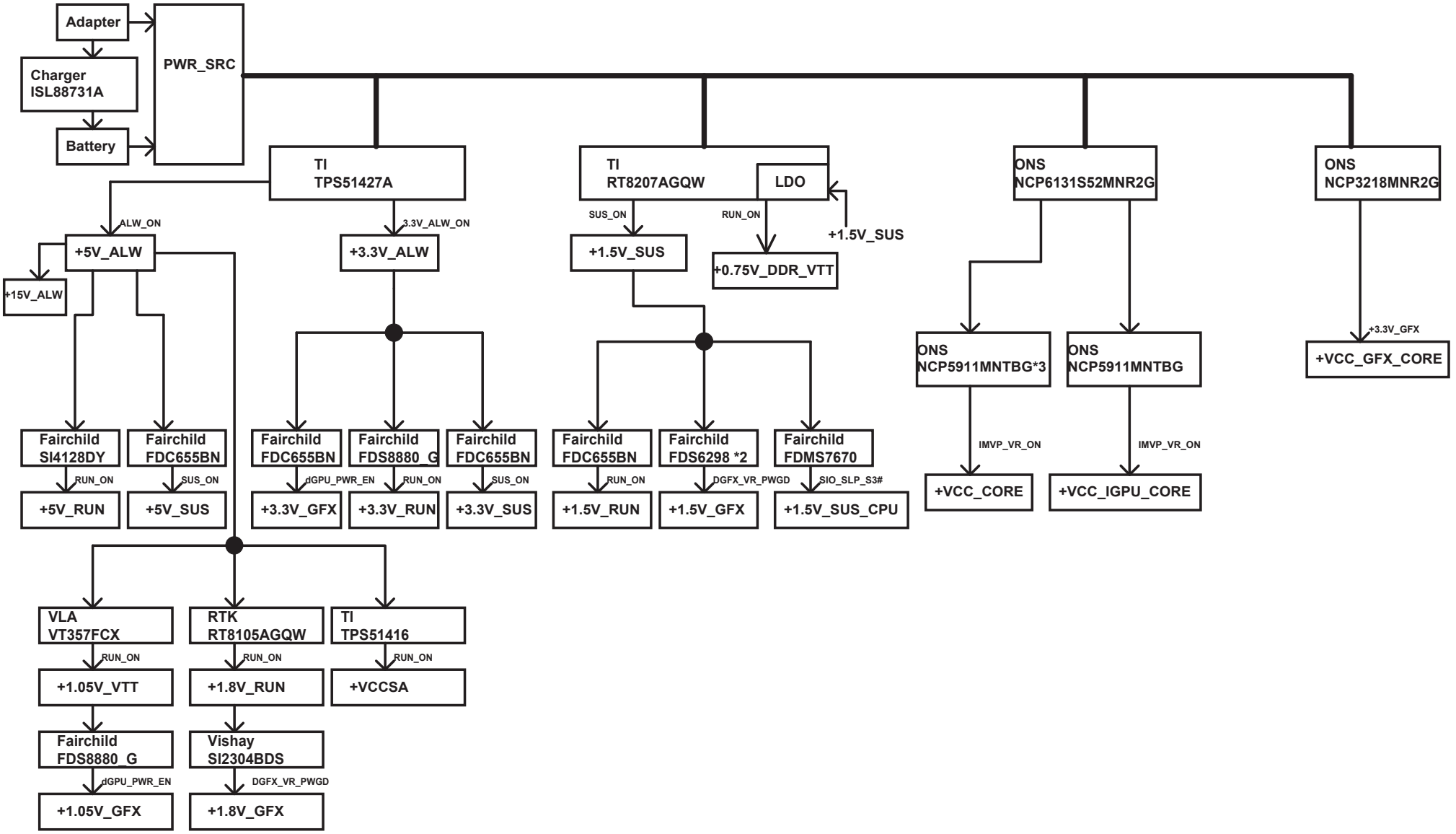
VER : 1A



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

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	Power Block Diagram	1A

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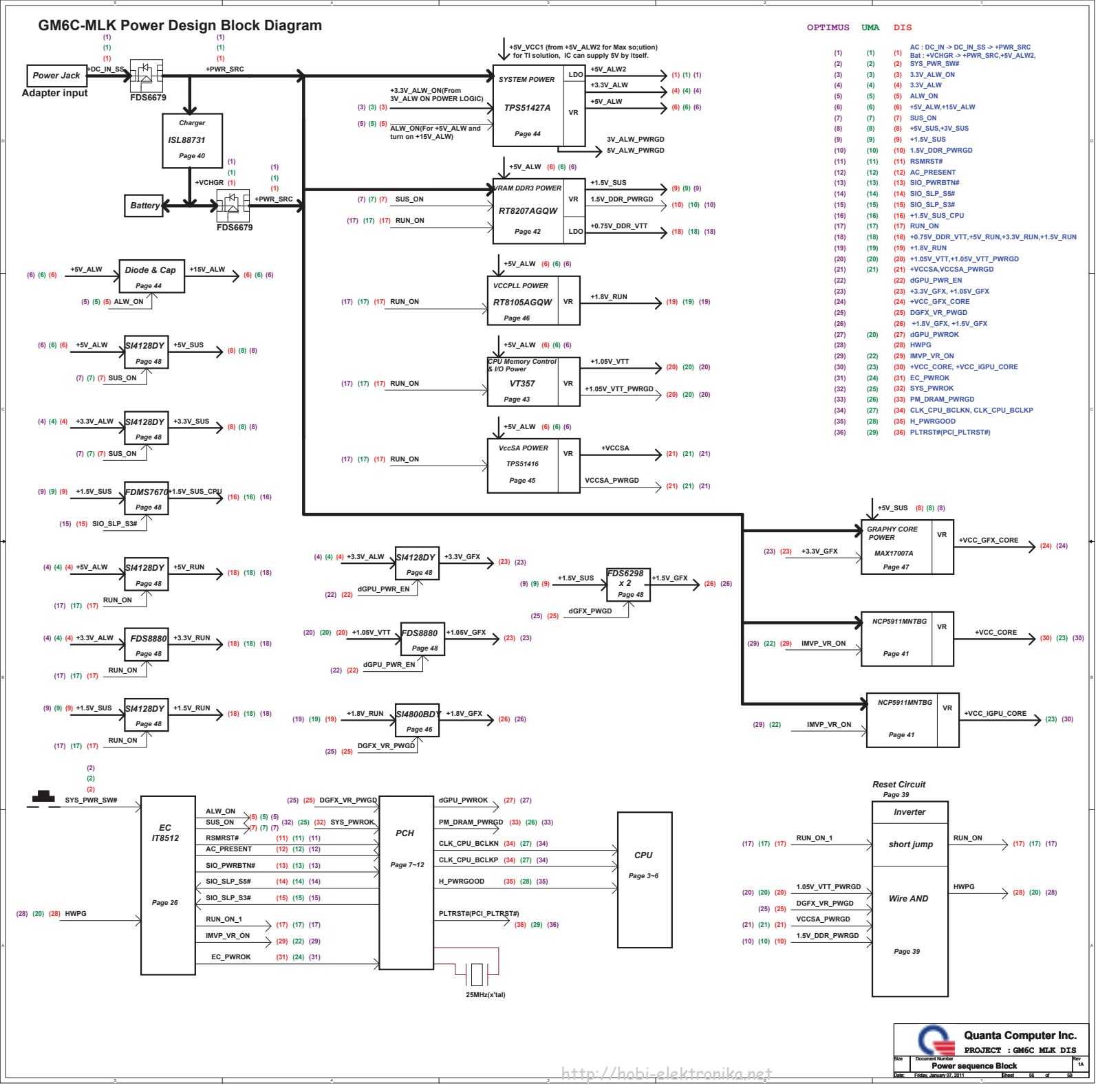
GM6C-MLK Power Design Block Diagram



OPTIMUS	UMA	DIS	
(1)	(1)	(1)	AC : DC_IN -> DC_IN_SS -> +PWR_SRC Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2)	(2)	(2)	SYS_PWR_SW#
(3)	(3)	(3)	3.3V_ALW_ON
(4)	(4)	(4)	3.3V_ALW
(5)	(5)	(5)	ALW_ON
(6)	(6)	(6)	+5V_ALW,+15V_ALW
(7)	(7)	(7)	SUS_ON
(8)	(8)	(8)	+5V_SUS,+3V_SUS
(9)	(9)	(9)	+1.5V_SUS
(10)	(10)	(10)	1.5V_DDR_PWRGD
(11)	(11)	(11)	RSMRST#
(12)	(12)	(12)	AC_PRESENT
(13)	(13)	(13)	SIO_PWRBTN#
(14)	(14)	(14)	SIO_SLP_S5#
(15)	(15)	(15)	SIO_SLP_S3#
(16)	(16)	(16)	+1.5V_SUS_CPU
(17)	(17)	(17)	RUN_ON
(18)	(18)	(18)	+0.75V_DDR_VTT,+5V_RUN,+3.3V_RUN,+1.5V_RUN
(19)	(19)	(19)	+1.8V_RUN
(20)	(20)	(20)	+1.05V_VTT,+1.05V_VTT_PWRGD
(21)	(21)	(21)	+VCCSA,VCCSA_PWRGD
(22)		(22)	dGPU_PWR_EN
(23)		(23)	+3.3V_GFX, +1.05V_GFX
(24)		(24)	+VCC_GFX_CORE
(25)		(25)	DGFX_VR_PWGD
(26)		(26)	+1.8V_GFX, +1.5V_GFX
(27)	(20)	(27)	dGPU_PWROK
(28)		(28)	HWPG
(29)	(22)	(29)	IMVP_VR_ON
(30)	(23)	(30)	+VCC_CORE, +VCC_iGPU_CORE
(31)	(24)	(31)	EC_PWROK
(32)	(25)	(32)	SYS_PWROK
(33)	(26)	(33)	PM_DRAM_PWRGD
(34)	(27)	(34)	CLK_CPU_BCLKN, CLK_CPU_BCLKP
(35)	(28)	(35)	H_PWRGOOD
(36)	(29)	(36)	PLTRST#(PCI_PLTRST#)

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Power sequence Block
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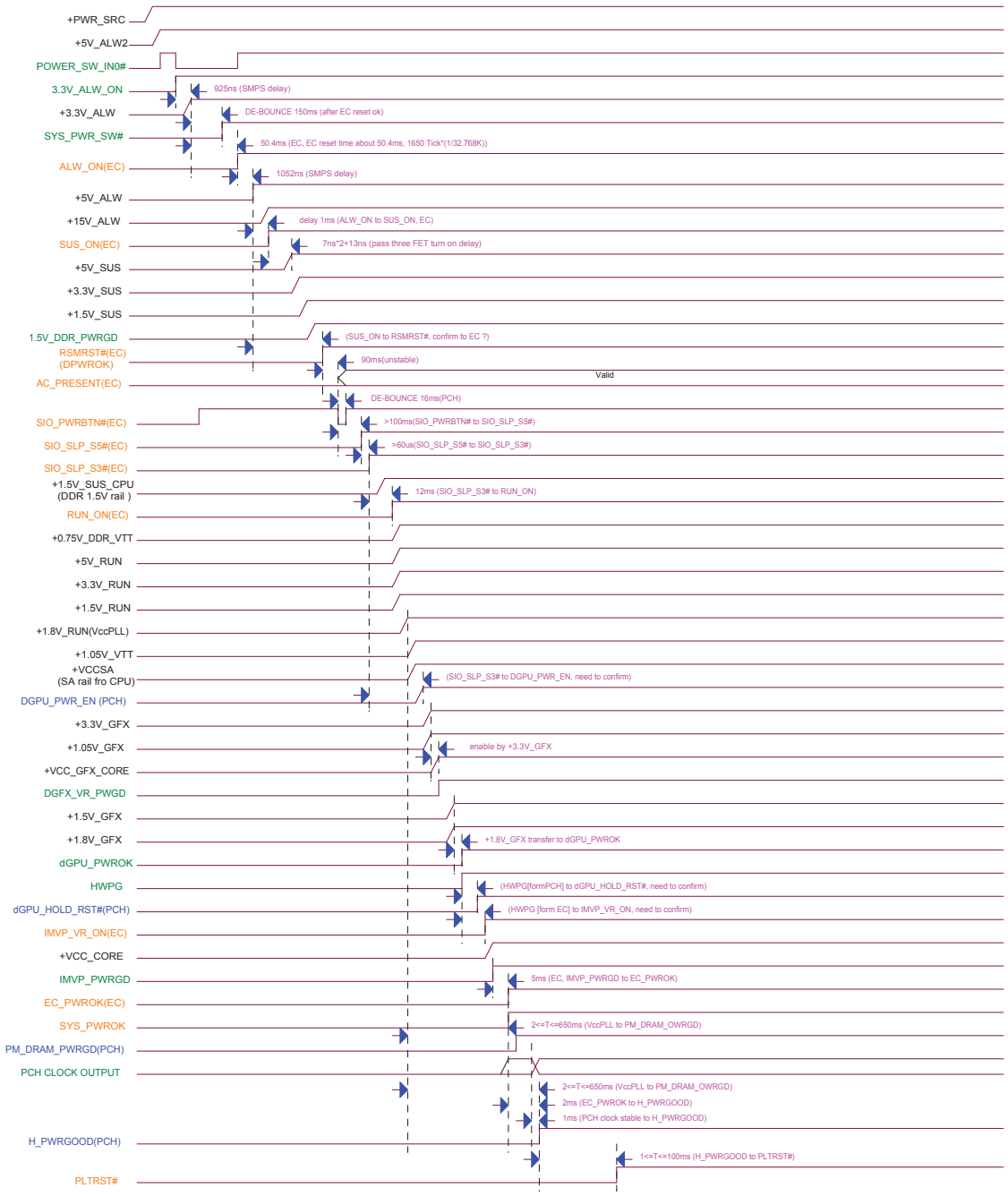
GM6C_MLK_DIS Power on Timing(BATTERY MODE)



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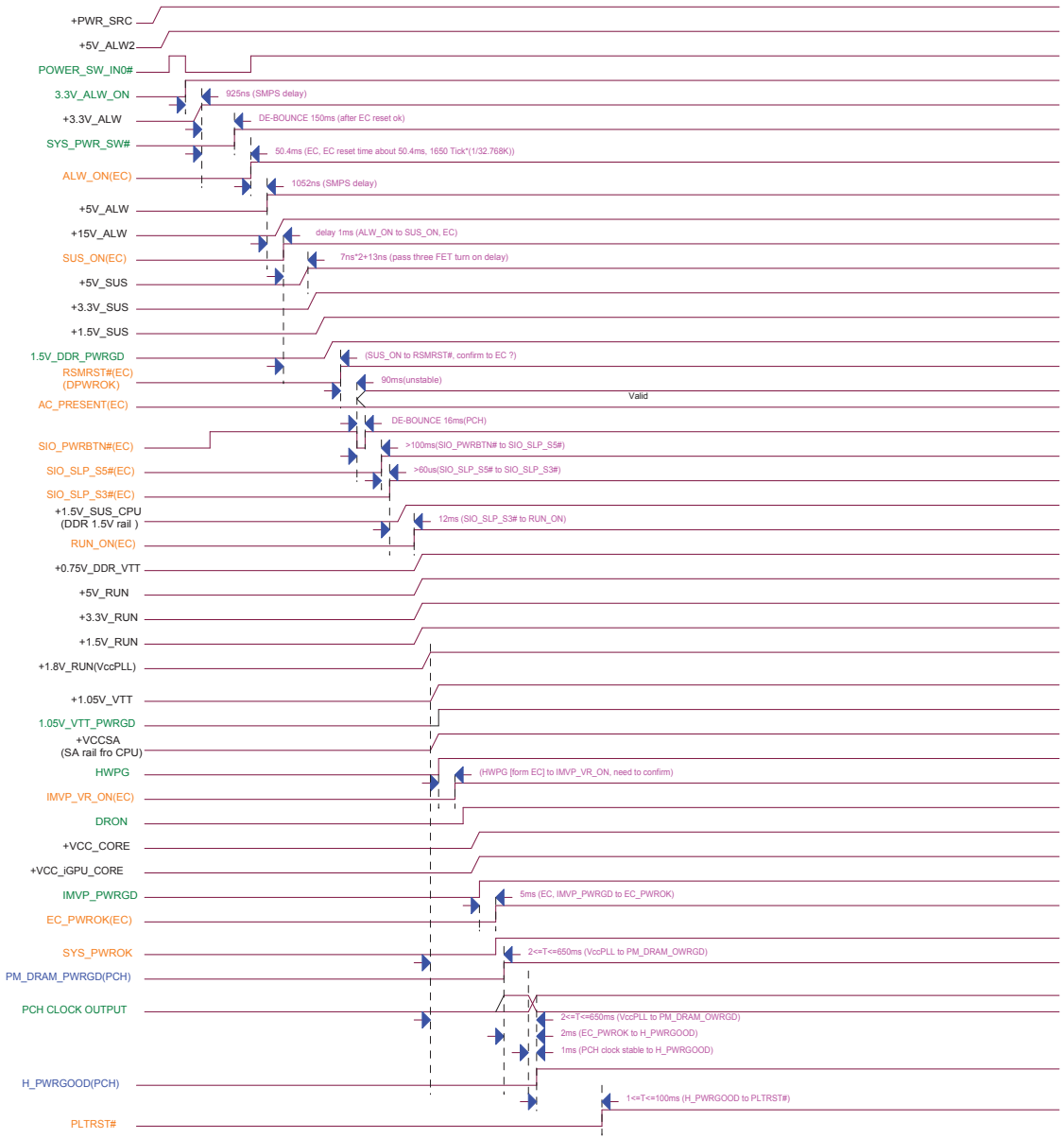
GM6C_MLK_UMA Power on Timing(BATTERY MODE)



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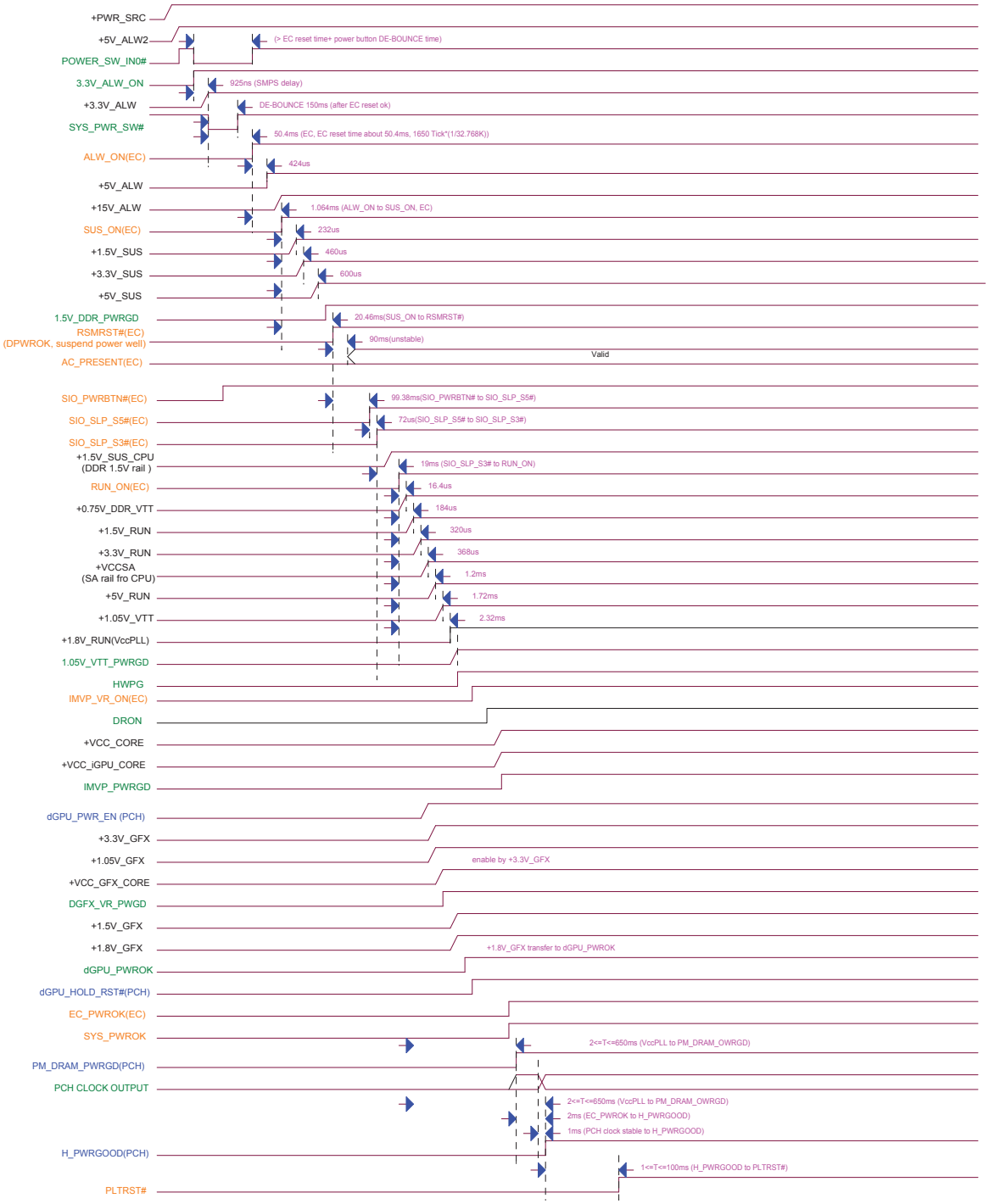
GM6C_MLK_OPTIMUS Power on Timing(BATTERY MODE)



Quanta Computer Inc.		
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Size	Document Number: POWER SEQUENCE(OPTIMUS)	Rev: 1A
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