Compal Confidential

NEW70 / 80 / 90 / 50 <LA-5892P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-01-21

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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Title: Cover Page		
Size: Custom	Document Number: NEW70 M/B LA-5892P Schematic	Rev: 1.0
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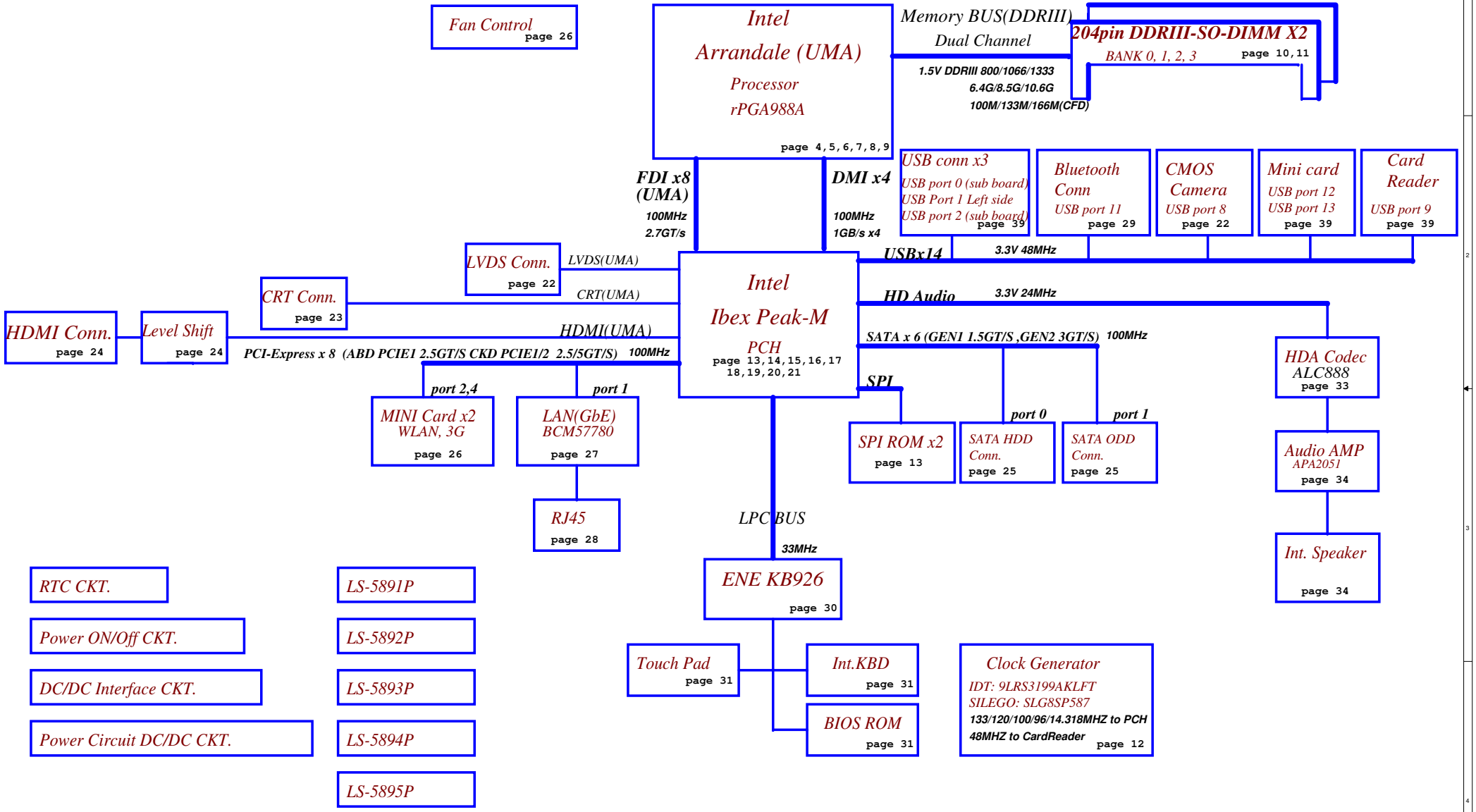
Model Name NEW70 / 80 / 90 / 50
File Name : LA-5892P

ZZ
DAZ0C900200
PCB NEW70 LA-5892P

46@ ZZZ1
RO0000003HM
HDMI+HDCP LOGO



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Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%
Ra/Rc	100K +/- 5%

	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	NEW70
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	NEW80
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	NEW90
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		
7	NC	2.500 V	3.300 V	3.300 V		

Not Used

BTO Option Table

BOM Config

BTO Item	BOM Structure
HDMI	HDMI@
3G	3G@
9050@	NEW90 / NEW50
7080@	NEW70 / NEW80

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 USB	Ext1 USB
		1	Ext3 HS USB	Ext3 HS USB
	UHCI1	2	Ext2 USB	Ext2 USB
		3		
	UHCI2	4		
		5		
	UHCI3	6		
		7		
EHCI2	UHCI4	8	Camera	Camera
		9	Card Reader	Card Reader
	UHCI5	10	SIM CARD	SIM CARD
		11	Blue Tooth	Blue Tooth
	UHCI6	12	1st Min-Card	1st Min-Card
		13	2st Min-Card	2st Min-Card

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Title: Notes List

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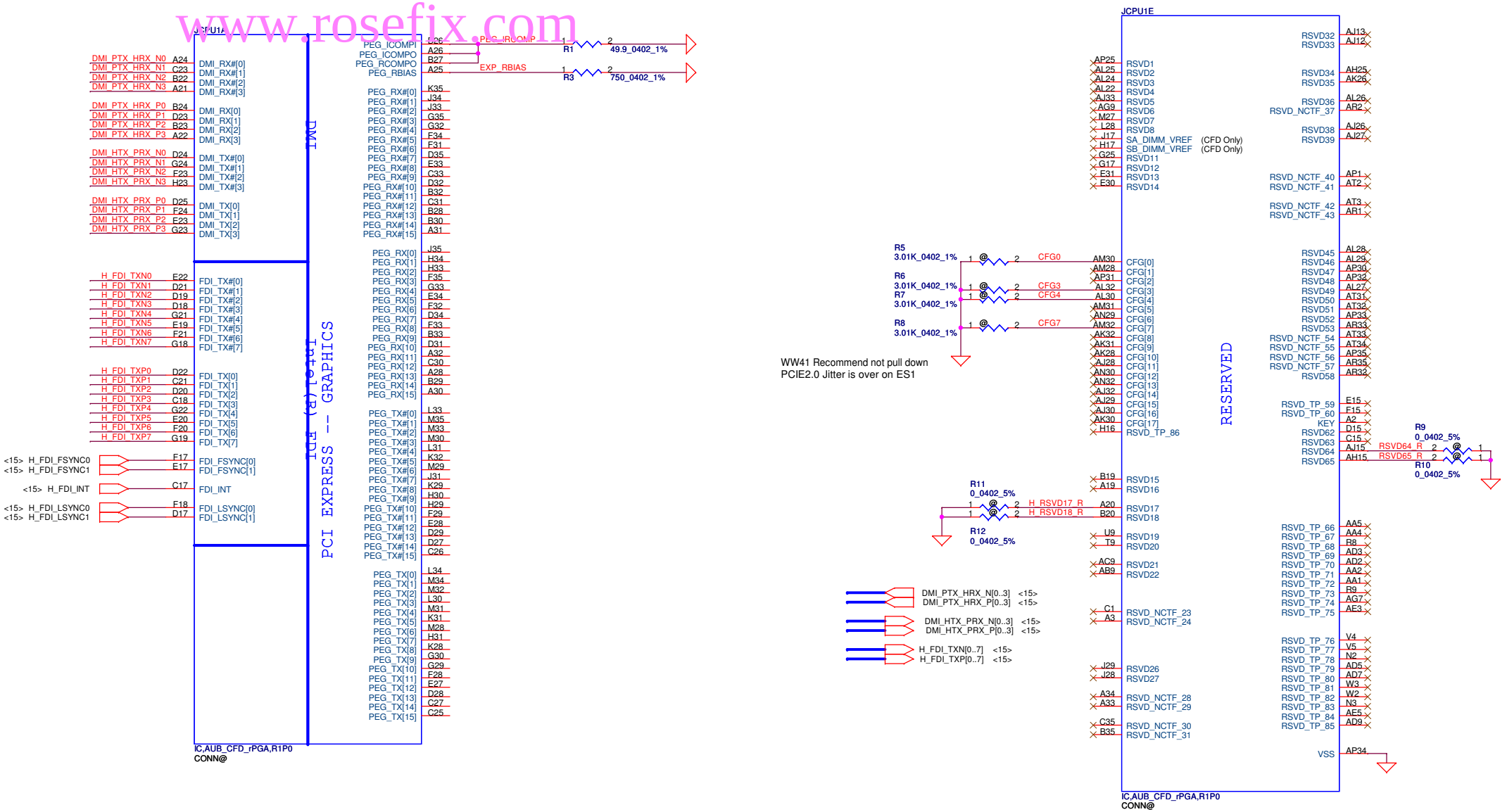

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Title: PROCESSOR (1/6) DMI,FDI,PEG

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B	NEW70 M/B LA-5892P Schematic	1.0

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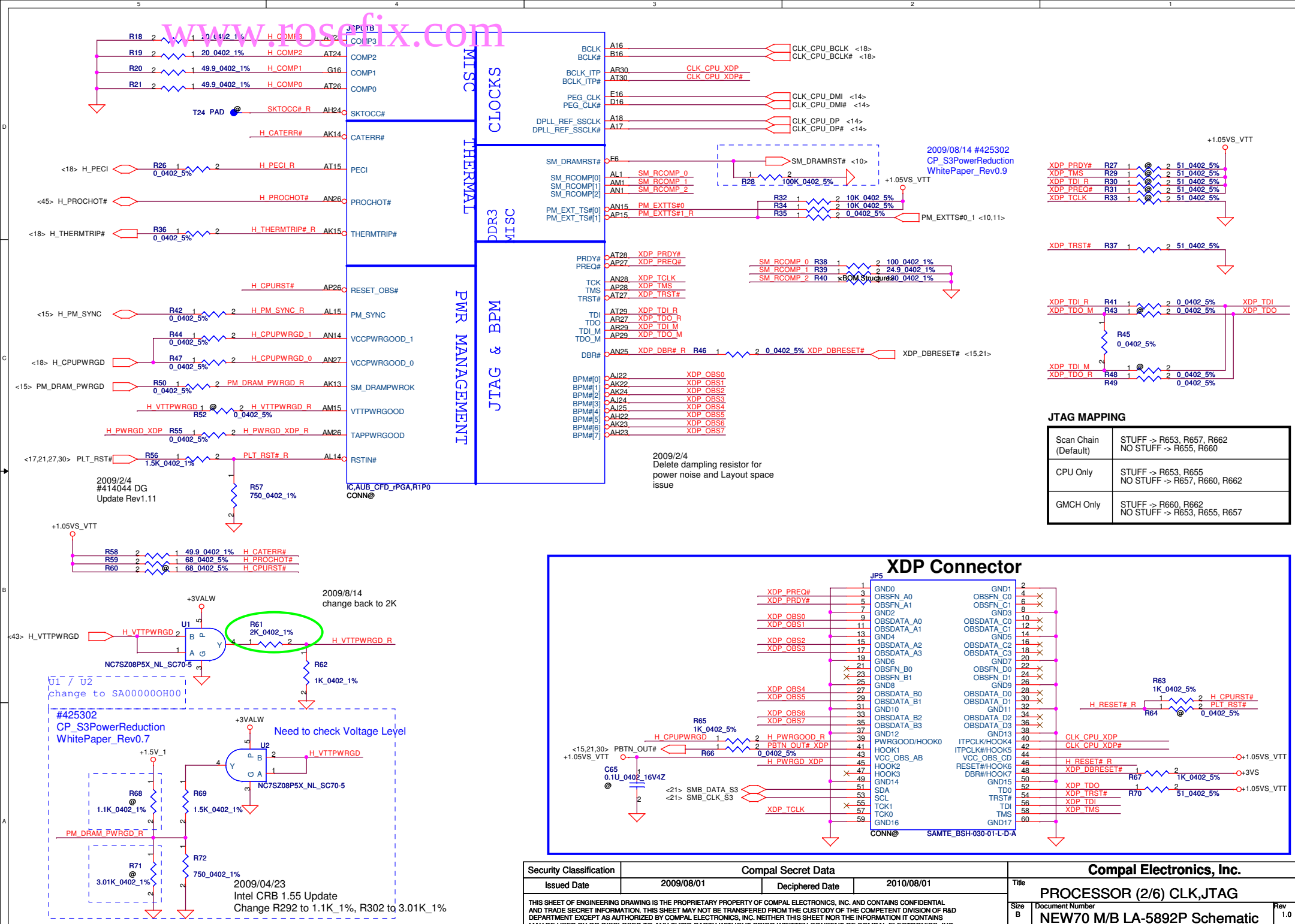

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

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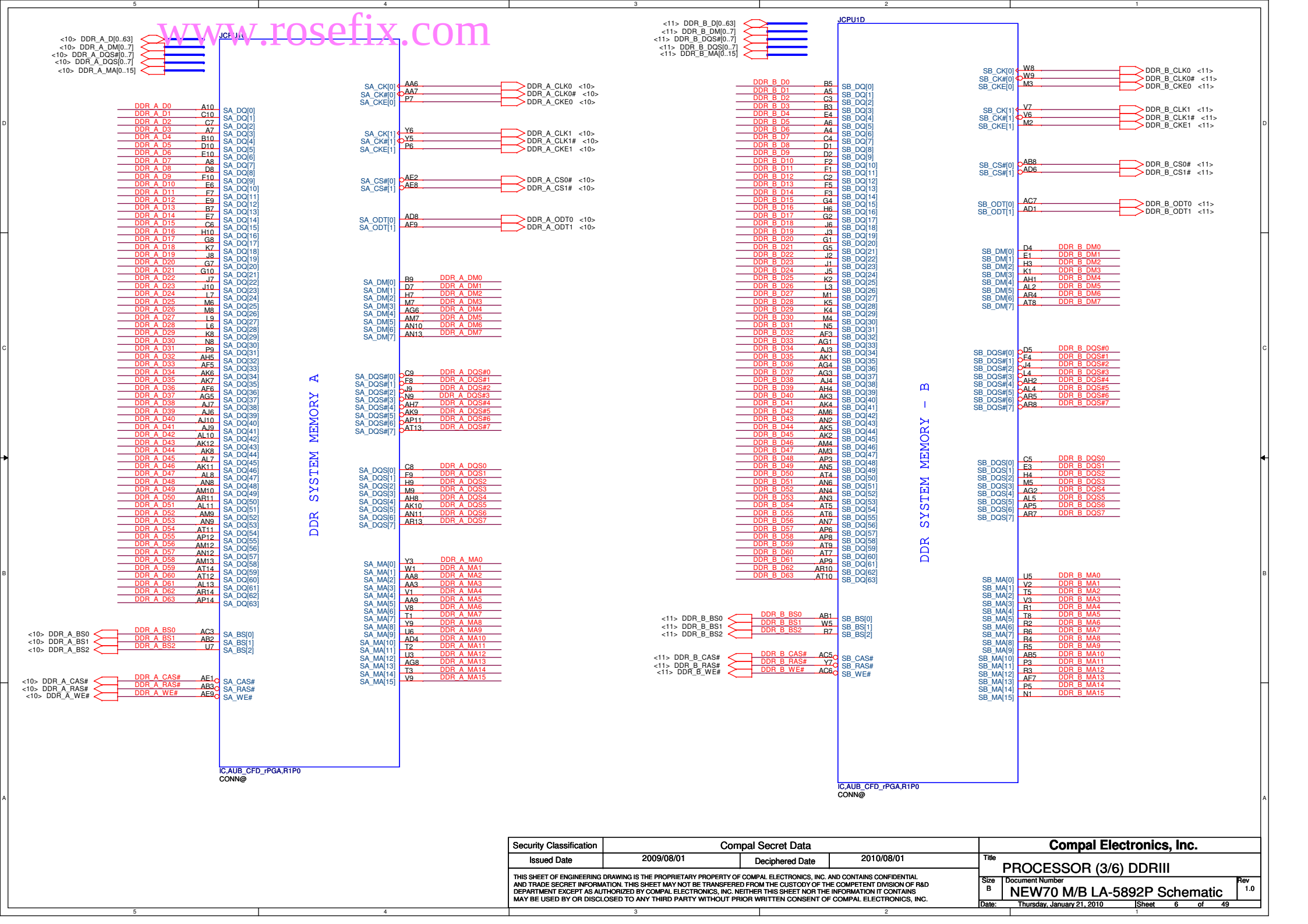

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

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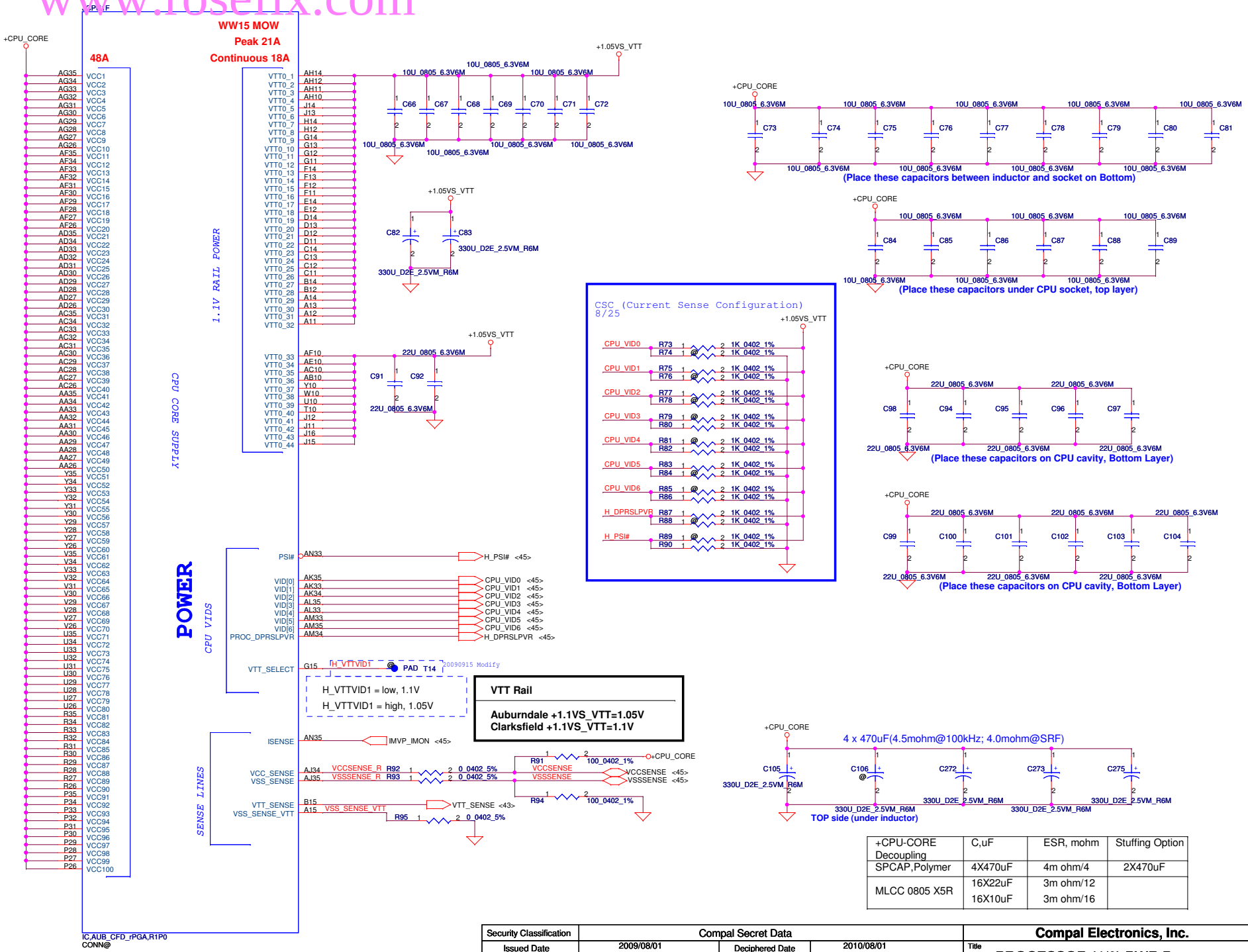

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

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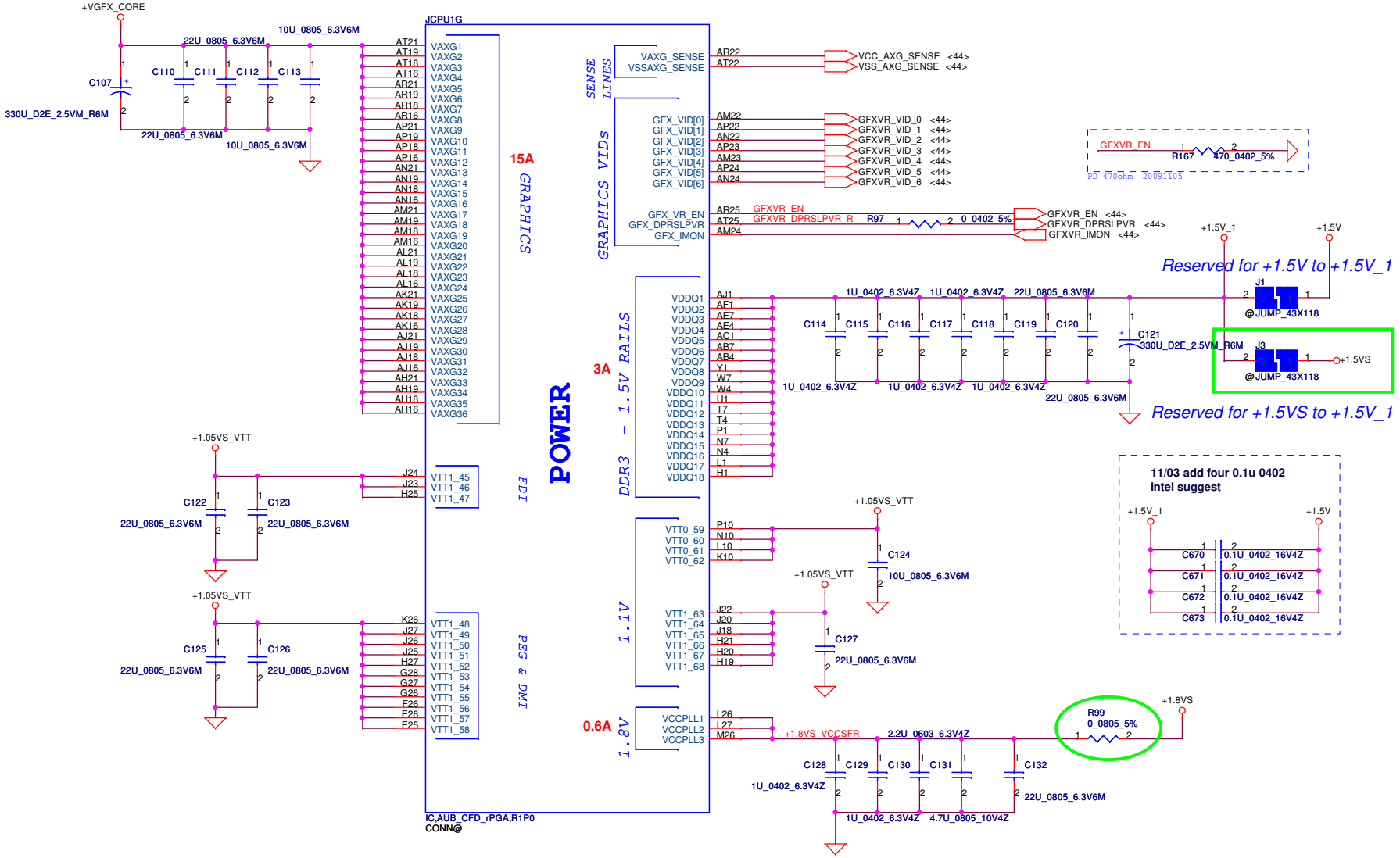

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

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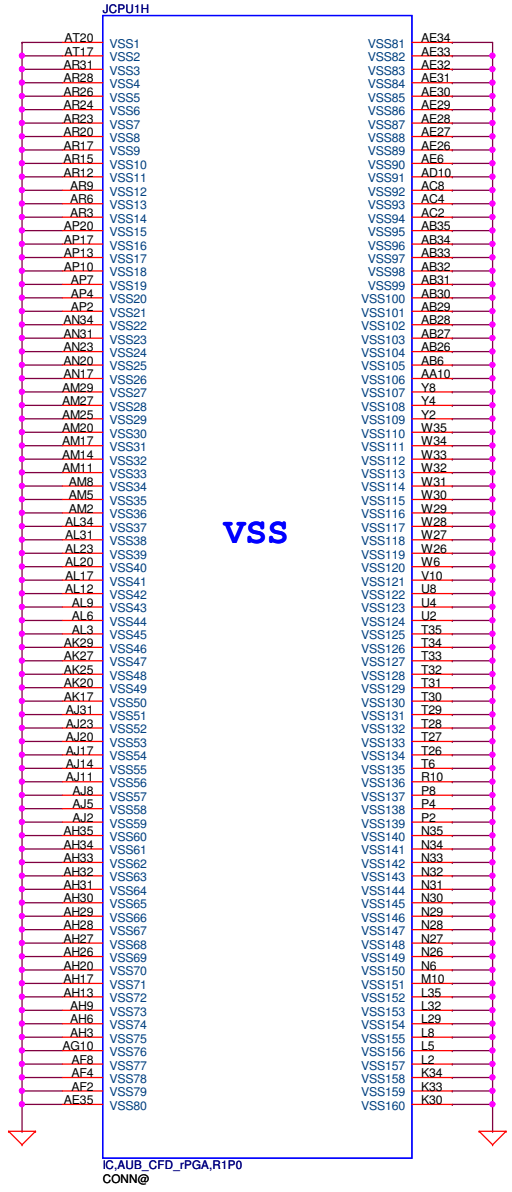

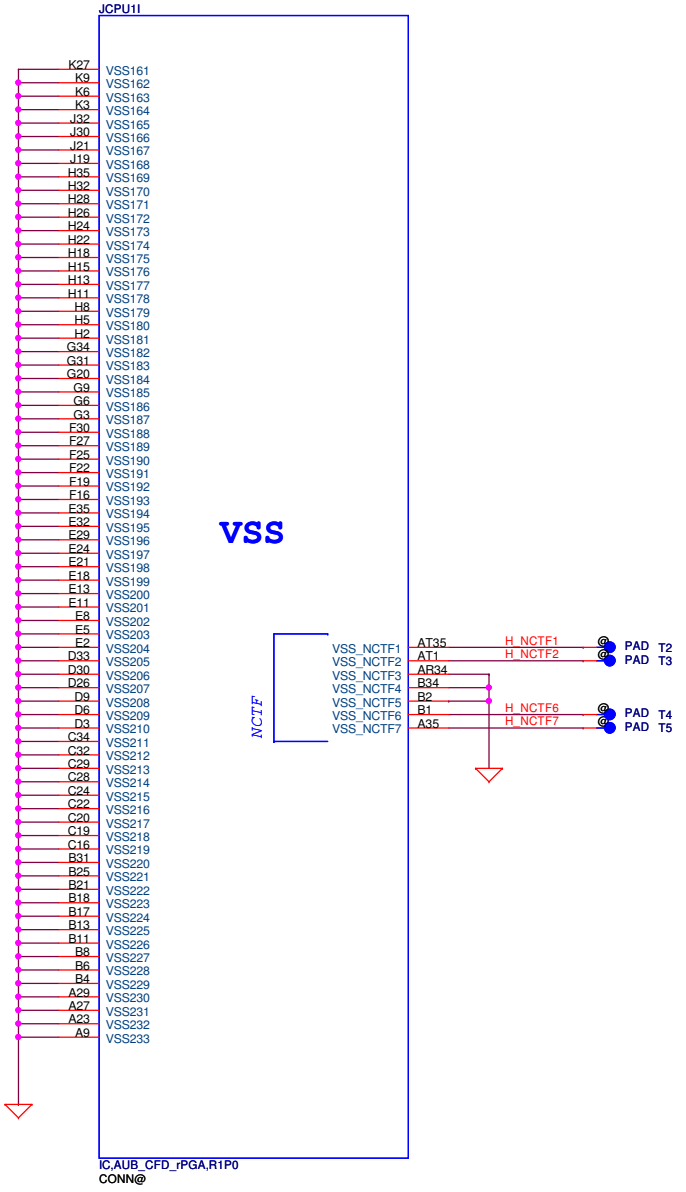

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Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

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DIMMA VREFDQ M1 Circuit

+1.5V
R101 1K_0402_1%
+DIMM_VREFDQA
R104 1K_0402_1%

DIMMA & DIMMB VREFCA circuit

+1.5V
R106 1K_0402_1%
+DIMM_VREFCA
R107 1K_0402_1%

<6> DDR_A_DQ[0..63]
<6> DDR_A_DM[0..7]
<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]

M1 Circuit

+DIMM_VREFDQA
C134 0.1U_0402_16V4Z
C133 2.2U_0805_16V4Z

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0

+1.5V
R102 0_0402_5% @
R103 1K_0402_1%
<5> SM_DRAMRST#
Q2 BSS138LT1G_SOT23-3
DIMM_DRAMRST#
DIMM_DRAMRST# <11>
C617 0.047U_0402_16V7K
<18> RST_GATE
RST_GATE

JDIMM1

+DIMM_VREFDQA	1	VREF_DQ	VSS1	2	
	3	VSS2	DQ4	4	DDR_A_D4
DDR_A_D0	5	DQ0	DQ5	6	DDR_A_D5
DDR_A_D1	7	DQ1	VSS3	8	
	9	VSS4	DQS#0	10	DDR_A_DQS#0
DDR_A_DM0	11	DM0	DQS0	12	DDR_A_DQS0
	13	VSS5	VSS6	14	
DDR_A_D2	15	DQ2	DQ6	16	DDR_A_D6
DDR_A_D3	17	DQ3	DQ7	18	DDR_A_D7
	19	VSS7	VSS8	20	
DDR_A_D8	21	DQ8	DQ12	22	DDR_A_D12
DDR_A_D9	23	DQ9	DQ13	24	DDR_A_D13
	25	VSS9	VSS10	26	
DDR_A_DQS#1	27	DQS#1	DM1	28	DDR_A_DM1
DDR_A_DQS1	29	DQS1	RESET#	30	DIMM_DRAMRST#
	31	VSS11	VSS12	32	
DDR_A_D10	33	DQ10	DQ14	34	DDR_A_D14
DDR_A_D11	35	DQ11	DQ15	36	DDR_A_D15
	37	VSS13	VSS14	38	
DDR_A_D16	39	DQ16	DQ20	40	DDR_A_D20
DDR_A_D17	41	DQ17	DQ21	42	DDR_A_D21
	43	VSS15	VSS16	44	
DDR_A_DQS#2	45	DQS#2	DM2	46	DDR_A_DM2
DDR_A_DQS2	47	DQS2	VSS17	48	
	49	VSS18	DQ22	50	DDR_A_D22
DDR_A_D18	51	DQ18	DQ23	52	DDR_A_D23
DDR_A_D19	53	DQ19	VSS19	54	
	55	VSS20	DQ28	56	DDR_A_D28
DDR_A_D24	57	DQ24	DQ29	58	DDR_A_D29
DDR_A_D25	59	DQ25	VSS21	60	
	61	VSS22	DQS#3	62	DDR_A_DQS#3
DDR_A_DM3	63	DM3	DQS3	64	DDR_A_DQS3
	65	VSS23	VSS24	66	
DDR_A_D26	67	DQ26	DQ30	68	DDR_A_D30
DDR_A_D27	69	DQ27	DQ31	70	DDR_A_D31
	71	VSS25	VSS26	72	
<6> DDR_A_CKE0 DDR_A_CKE0	73	CKE0	CKE1	74	DDR_A_CKE1 DDR_A_CKE1 <6>
	75	VDD1	VDD2	76	
	77	NC1	A15	78	DDR_A_MA15
<6> DDR_A_BS2 DDR_A_BS2	79	BA2	A14	80	DDR_A_MA14
	81	VDD3	VDD4	82	
DDR_A_MA12	83	A12/BC#	A11	84	DDR_A_MA11
DDR_A_MA9	85	A9	A7	86	DDR_A_MA7
	87	VDD5	VDD6	88	
DDR_A_MA8	89	A8	A6	90	DDR_A_MA6
DDR_A_MA5	91	A5	A4	92	DDR_A_MA4
	93	VDD7	VDD8	94	
DDR_A_MA3	95	A3	A2	96	DDR_A_MA2
DDR_A_MA1	97	A1	A0	98	DDR_A_MA0
	99	VDD9	VDD10	100	
<6> DDR_A_CLK0 DDR_A_CLK0	101	CK0	CK1	102	DDR_A_CLK1 DDR_A_CLK1 <6>
<6> DDR_A_CLK0# DDR_A_CLK0#	103	CK0#	CK1#	104	DDR_A_CLK1# DDR_A_CLK1# <6>
	105	VDD11	VDD12	106	
DDR_A_MA10	107	A10/AP	BA1	108	DDR_A_BS1 DDR_A_BS1 <6>
<6> DDR_A_BS0 DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS# DDR_A_RAS# <6>
	111	VDD13	VDD14	112	
<6> DDR_A_WE# DDR_A_WE#	113	WE#	S0#	114	DDR_A_CS0# DDR_A_CS0# <6>
<6> DDR_A_CAS# DDR_A_CAS#	115	CAS#	ODT0	116	DDR_A_ODT0 DDR_A_ODT0 <6>
	117	VDD15	VDD16	118	
DDR_A_MA13	119	A13	ODT1	120	DDR_A_ODT1 DDR_A_ODT1 <6>
<6> DDR_A_CS1# DDR_A_CS1#	121	S1#	NC2	122	
	123	VDD17	VDD18	124	
	125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA R108 1 2 0_0402_5%
	127	VSS27	VSS28	128	
DDR_A_D32	129	DQ32	DQ36	130	DDR_A_D36
DDR_A_D33	131	DQ33	DQ37	132	DDR_A_D37
	133	VSS29	VSS30	134	
DDR_A_DQS#4	135	DQS#4	DM4	136	DDR_A_DM4
DDR_A_DQS4	137	DQS4	VSS31	138	
	139	VSS32	DQ38	140	DDR_A_D38
DDR_A_D34	141	DQ34	DQ39	142	DDR_A_D39
DDR_A_D35	143	DQ35	VSS33	144	
	145	VSS34	DQ44	146	DDR_A_D44
DDR_A_D40	147	DQ40	DQ45	148	DDR_A_D45
DDR_A_D41	149	DQ41	VSS35	150	
	151	VSS36	DQS#5	152	DDR_A_DQS#5
DDR_A_DM5	153	DM5	DQS5	154	DDR_A_DQS5
	155	VSS37	VSS38	156	
DDR_A_D42	157	DQ42	DQ46	158	DDR_A_D46
DDR_A_D43	159	DQ43	DQ47	160	DDR_A_D47
	161	VSS39	VSS40	162	
DDR_A_D48	163	DQ48	DQ52	164	DDR_A_D52
DDR_A_D49	165	DQ49	DQ53	166	DDR_A_D53
	167	VSS41	VSS42	168	
DDR_A_DQS#6	169	DQS#6	DM6	170	DDR_A_DM6
DDR_A_DQS6	171	DQS6	VSS43	172	
	173	VSS44	DQ54	174	DDR_A_D54
DDR_A_D50	175	DQ50	DQ55	176	DDR_A_D55
DDR_A_D51	177	DQ51	VSS45	178	
	179	VSS46	DQ60	180	DDR_A_D60
DDR_A_D56	181	DQ56	DQ61	182	DDR_A_D61
DDR_A_D57	183	DQ57	VSS47	184	
	185	VSS48	DQS#7	186	DDR_A_DQS#7
DDR_A_DM7	187	DM7	DQS7	188	DDR_A_DQS7
	189	VSS49	VSS50	190	
DDR_A_D58	191	DQ58	DQ62	192	DDR_A_D62
DDR_A_D59	193	DQ59	DQ63	194	DDR_A_D63
	195	VSS51	VSS52	196	
R109 1 2 10K_0402_5%	197	SA0	EVENT#	198	PM_EXTTS#0_1 PM_EXTTS#0_1 <5,11>
+3VS	199	VDDSPD	SDA	200	D_CK_SDATA D_CK_SDATA <11,12>
	201	SA1	SCL	202	D_CK_SCLK D_CK_SCLK <11,12>
	203	VTT1	VTT2	204	+0.75VS
	205	G1	G2	206	

FOX_AS0A626-U8RN-7F

C148 2.2U_0603_6.3V4Z
C149 0.1U_0402_16V4Z
R110 10K_0402_5%

+DIMM_VREFCA
C135 2.2U_0603_6.3V4Z
C136 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C137 10U_0805_6.3V6M
C138 10U_0805_6.3V6M
C139 10U_0805_6.3V6M
C140 10U_0805_6.3V6M
C141 10U_0805_6.3V6M
C142 10U_0805_6.3V6M
C143 0.1U_0402_16V4Z
C144 0.1U_0402_16V4Z
C145 0.1U_0402_16V4Z
C146 0.1U_0402_16V4Z
@C147 330U_2.5V_M_R15

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS
C150 1U_0402_6.3V4Z
C151 1U_0402_6.3V4Z
C152 1U_0402_6.3V4Z
C153 1U_0402_6.3V4Z
C154 10U_0805_6.3V6M

DDR3 SO-DIMM A
Change to Reverse Type
8mm High

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

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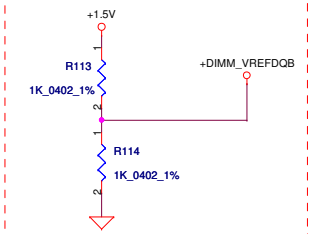
2008/9/3 400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

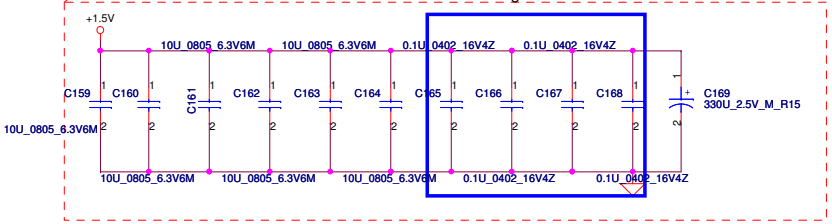
<6> DDR_B_DQS#[0..7]
<6> DDR_B_D[0..63]
<6> DDR_B_DM[0..7]
<6> DDR_B_DQS[0..7]
<6> DDR_B_MA[0..15]

DIMMB VREFDQ M1 Circuit

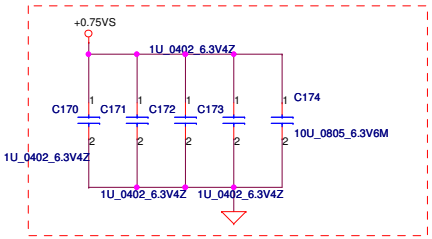


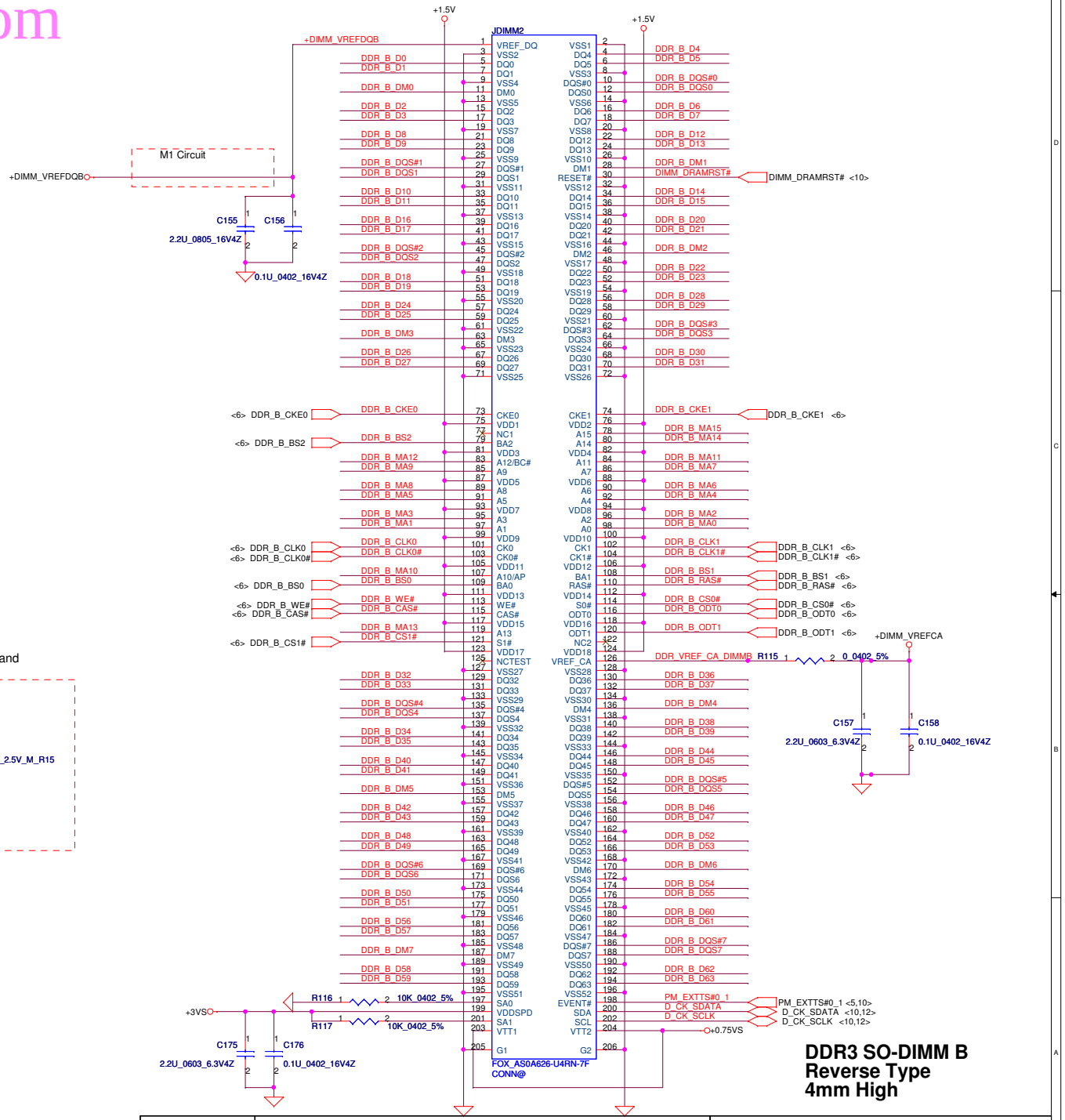
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDIMM2.203 & JDIMM2.204





DDR3 SO-DIMM B
Reverse Type
4mm High

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number	NEW70 M/B LA-5892P Schematic	Rev 1.0
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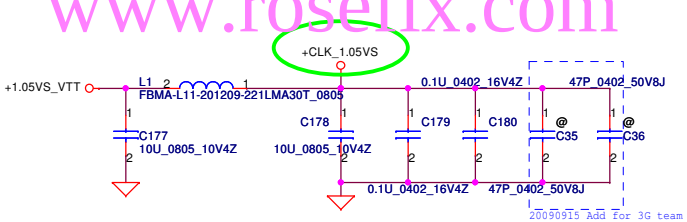
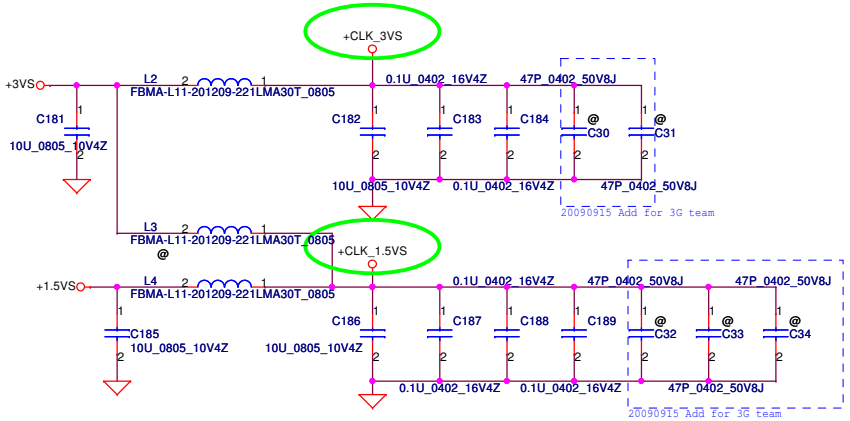
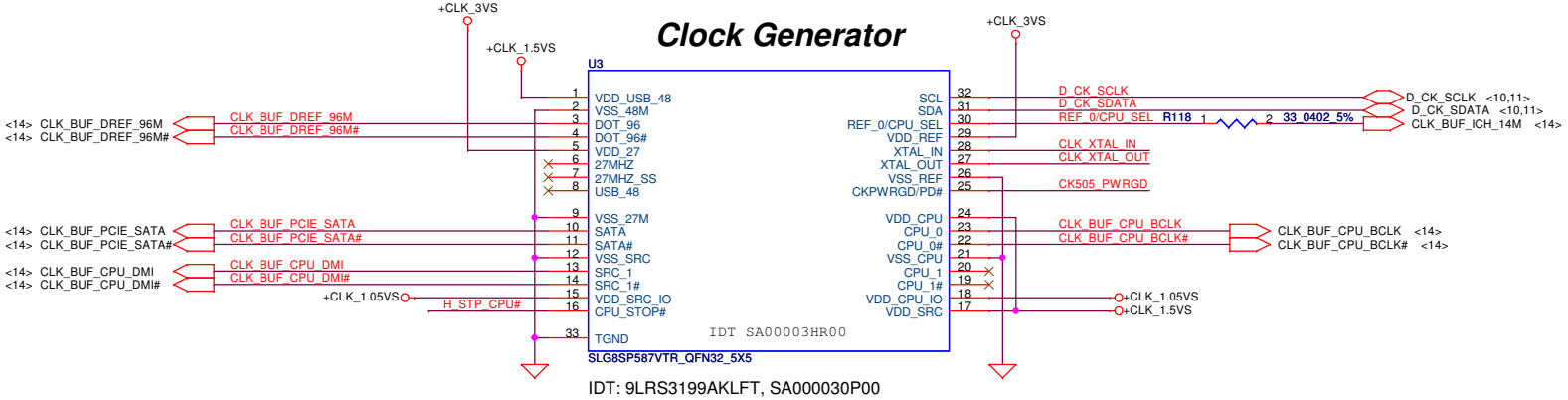




Clock Generator



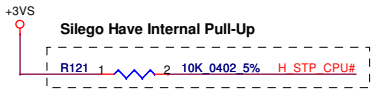
IDT: 9LRS3199AKLFT, SA000030P00

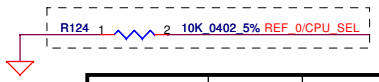
SILEGO: SLG8SP587V(WF), SA00002XY10

Low Power:

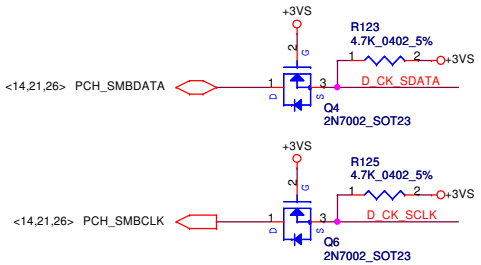
IDT: 9LVS3199AKLFT, SA00003HR00

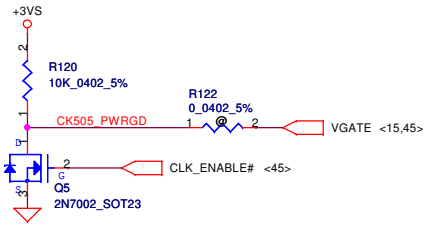
Realtek: RTM890N-631-GRT, SA00003HQ00

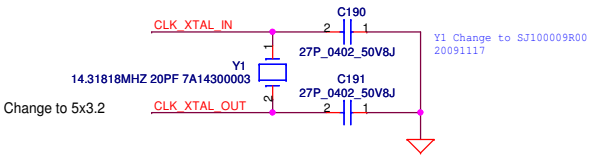




PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz







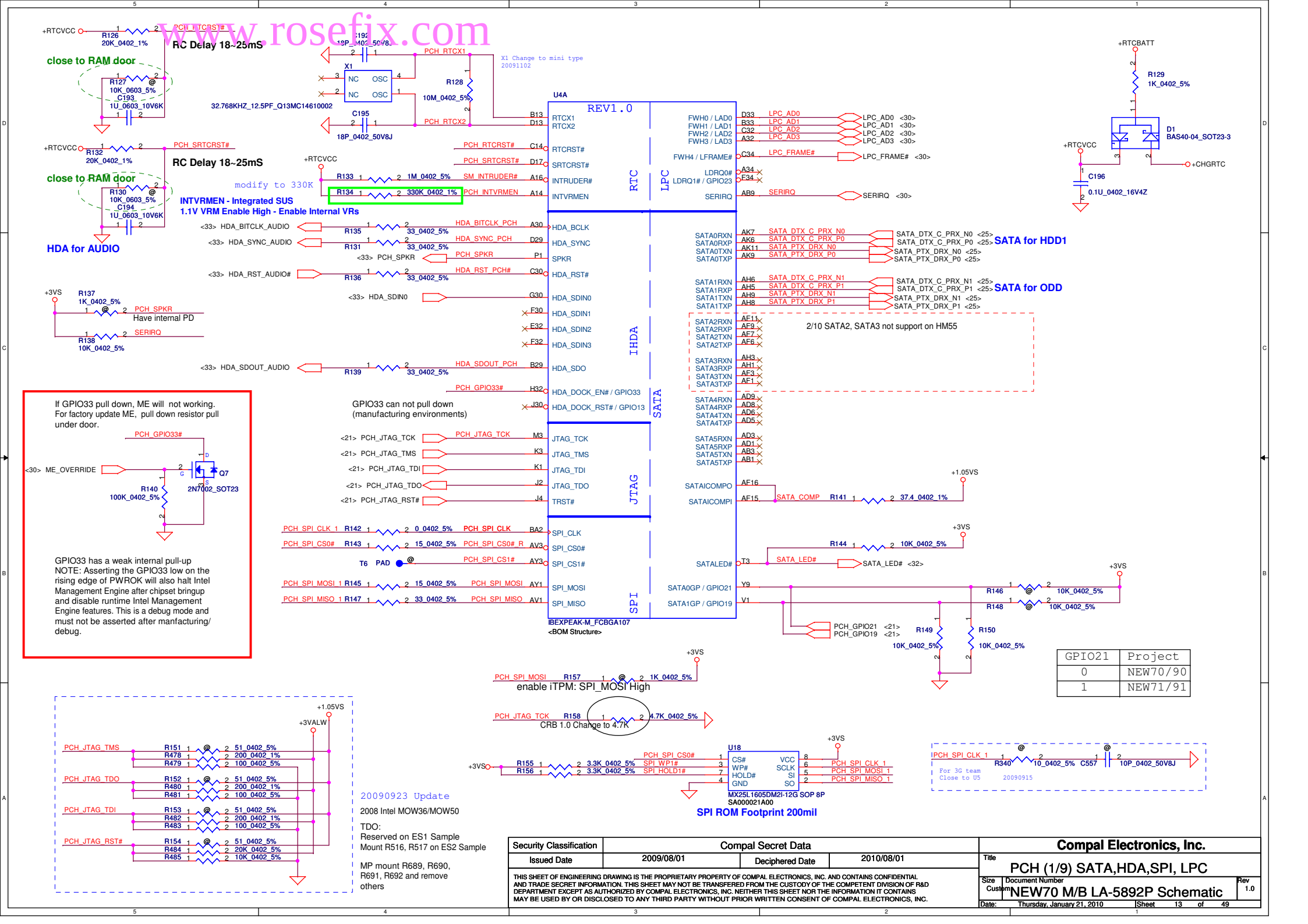
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 12 of 49



GPIO21	Project
0	NEW70/90
1	NEW71/91

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

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U4B

REV1.0

IBEXPEAK-M_FCBGA107

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

For PCIE LAN

<27> PCIE_DTX_C_PRX_N1
<27> PCIE_DTX_C_PRX_P1
<27> PCIE_PTX_C_DRX_N1
<27> PCIE_PTX_C_DRX_P1
C197 0.1U_0402_16V7K PCIE_PTX_DRX_N1
C198 0.1U_0402_16V7K PCIE_PTX_DRX_P1
PCIE_DTX_C_PRX_N1 BG30
PCIE_DTX_C_PRX_P1 BJ30
PCIE_PTX_C_DRX_N1 BF29
PCIE_PTX_C_DRX_P1 BH29

For Wireless LAN

<26> PCIE_DTX_C_PRX_N2
<26> PCIE_DTX_C_PRX_P2
<26> PCIE_PTX_C_DRX_N2
<26> PCIE_PTX_C_DRX_P2
C199 0.1U_0402_16V7K PCIE_PTX_DRX_N2
C200 0.1U_0402_16V7K PCIE_PTX_DRX_P2
PCIE_DTX_C_PRX_N2 AW30
PCIE_DTX_C_PRX_P2 BA30
PCIE_PTX_C_DRX_N2 BC30
PCIE_PTX_C_DRX_P2 BD30

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

PCI-E* Controller Link

2/10 PCIE7, PCIE8 not support on HM55

SMBus

SMBALERT# / GPIO11 B9 EC_LID_OUT# → EC_LID_OUT# <30>
SMBCLK H14 PCH_SMBCLK → PCH_SMBCLK <12,21,26>
SMBDATA C8 PCH_SMBDATA → PCH_SMBDATA <12,21,26>
SML0ALERT# / GPIO60 J14 PCH_GPIO60
SML0CLK C6
SML0DATA G8
SML1ALERT# / GPIO74 M14 PCH_GPIO74
SML1CLK / GPIO58 E10 PCH_SML1CLK
SML1DATA / GPIO75 G12 PCH_SML1DAT

CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9

+3VALW
R159 10K_0402_5%
20090915 Add

PEG_A_CLKRQ# / GPIO47 H1 PEG_CLKREQ#

PEG

CLKOUT_PEG_A_N AD43
CLKOUT_PEG_A_P AD45
CLKOUT_DMI_N AN4 → CLK_CPU_DMI# <5>
CLKOUT_DMI_P AN2 → CLK_CPU_DMI <5>
CLKOUT_DP_N / CLKOUT_BCLK1_N AT1 → CLK_CPU_DP# <5>
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3 → CLK_CPU_DP <5>

From CLK BUFFER

For PCIE LAN

<27> CLK_PCIE_LAN# AK48 CLKOUT_PCIE0N
<27> CLK_PCIE_LAN AK47 CLKOUT_PCIE0P
<27> LAN_CLKREQ# R164 0_0402_5% PCH_GPIO73 P9 PCIECLKRQ0# / GPIO73

For Wireless LAN

<26> CLK_PCIE_MINI1# AM43 CLKOUT_PCIE1N
<26> CLK_PCIE_MINI1 AM45 CLKOUT_PCIE1P
<26> MINI1_CLKREQ# R165 0_0402_5%
<21> PCH_GPIO18 PCH_GPIO18 U4 PCIECLKRQ1# / GPIO18
AM47 CLKOUT_PCIE2N
AM48 CLKOUT_PCIE2P
<21> PCH_GPIO20 PCH_GPIO20 N4 PCIECLKRQ2# / GPIO20
AH42 CLKOUT_PCIE3N
AH41 CLKOUT_PCIE3P
PCH_GPIO25 A8 PCIECLKRQ3# / GPIO25
AM51 CLKOUT_PCIE4N
AM53 CLKOUT_PCIE4P
PCH_GPIO26 M9 PCIECLKRQ4# / GPIO26
AJ50 CLKOUT_PCIE5N
AJ52 CLKOUT_PCIE5P
PCH_GPIO44 H6 PCIECLKRQ5# / GPIO44
AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P
PCH_GPIO56 P13 PEG_B_CLKRQ# / GPIO56

CLKIN_DMI_N AW24 → CLK_BUF_CPU_DMI# <12>
CLKIN_DMI_P BA24 → CLK_BUF_CPU_DMI <12>
CLKIN_BCLK_N AP3 → CLK_BUF_CPU_BCLK# <12>
CLKIN_BCLK_P AP1 → CLK_BUF_CPU_BCLK <12>
CLKIN_DOT_96N F18 → CLK_BUF_DREF_96M# <12>
CLKIN_DOT_96P E18 → CLK_BUF_DREF_96M <12>
CLKIN_SATA_N / CKSSCD_N AH13 → CLK_BUF_PCIE_SATA# <12>
CLKIN_SATA_P / CKSSCD_P AH12 → CLK_BUF_PCIE_SATA <12>
REFCLK14IN P41 R338 10_0402_5% C555 10P_0402_50V8J → CLK_BUF_ICH_14M <12>
CLKIN_PCILOOPBACK J42 → CLK_PCI_FB <17>

XTAL25_IN AH51 XTAL25_IN
XTAL25_OUT AH53 XTAL25_OUT
XCLK_RCOMP AF38 XCLK_RCOMP R169 90.9_0402_1% +1.05VS

CLKOUTFLEX0 / GPIO64 T45
CLKOUTFLEX1 / GPIO65 P43 PROJECT_ID1
CLKOUTFLEX2 / GPIO66 T42 PROJECT_ID0
CLKOUTFLEX3 / GPIO67 N50

Clock Flex

Project Port ID

+3VS
R171 10K_0402_5%
@R172 10K_0402_5%
@R174 10K_0402_5%
R175 10K_0402_5%

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

C203 27P_0402_50V8J
R170 1M_0402_5%
Y2 25MHZ_20PF_7A25000012
C204 27P_0402_50V8J
Change to 5x3.2

+3VS
MINI1_CLKREQ# R177 10K_0402_5%
PCH_GPIO20 R178 10K_0402_5%

+3VALW
2009/09/23:Change to +3VALW
PCH_GPIO26 R166 10K_0402_5%
PCH_GPIO25 R186 10K_0402_5%
2009/08/13: Change back to +3VALW

+3VALW
EC_LID_OUT# R179 10K_0402_5%
PCH_SMBCLK R180 2.2K_0402_5%
PCH_SMBDATA R181 2.2K_0402_5%
PCH_GPIO60 R182 10K_0402_5%
PCH_SML1CLK R183 2.2K_0402_5%
PCH_SML1DAT R184 2.2K_0402_5%
PCH_GPIO74 R185 10K_0402_5%
PCH_GPIO44 R187 10K_0402_5%
PCH_GPIO56 R188 10K_0402_5%
PCH_GPIO73 R189 10K_0402_5%

Board ID

	LOW	HIGH
ID1 GPIO65	A & B test	C test

PROJECT ID

ID2 GPIO21	ID1 GPIO65	ID0 GPIO66	PROJECT
0	0	0	NEW70
0	0	1	NEW80
0	1	0	NEW90
0	1	1	
1	0	0	

+3VS
PCH_SML1CLK 6 2N7002DW-T/R7_SOT363-6 Q9A 1 EC_SMB_CK2 → EC_SMB_CK2 <30>

+3VS
Pull high +3VS at KB926 side
PCH_SML1DAT 3 2N7002DW-T/R7_SOT363-6 Q9B 4 EC_SMB_DA2 → EC_SMB_DA2 <30>

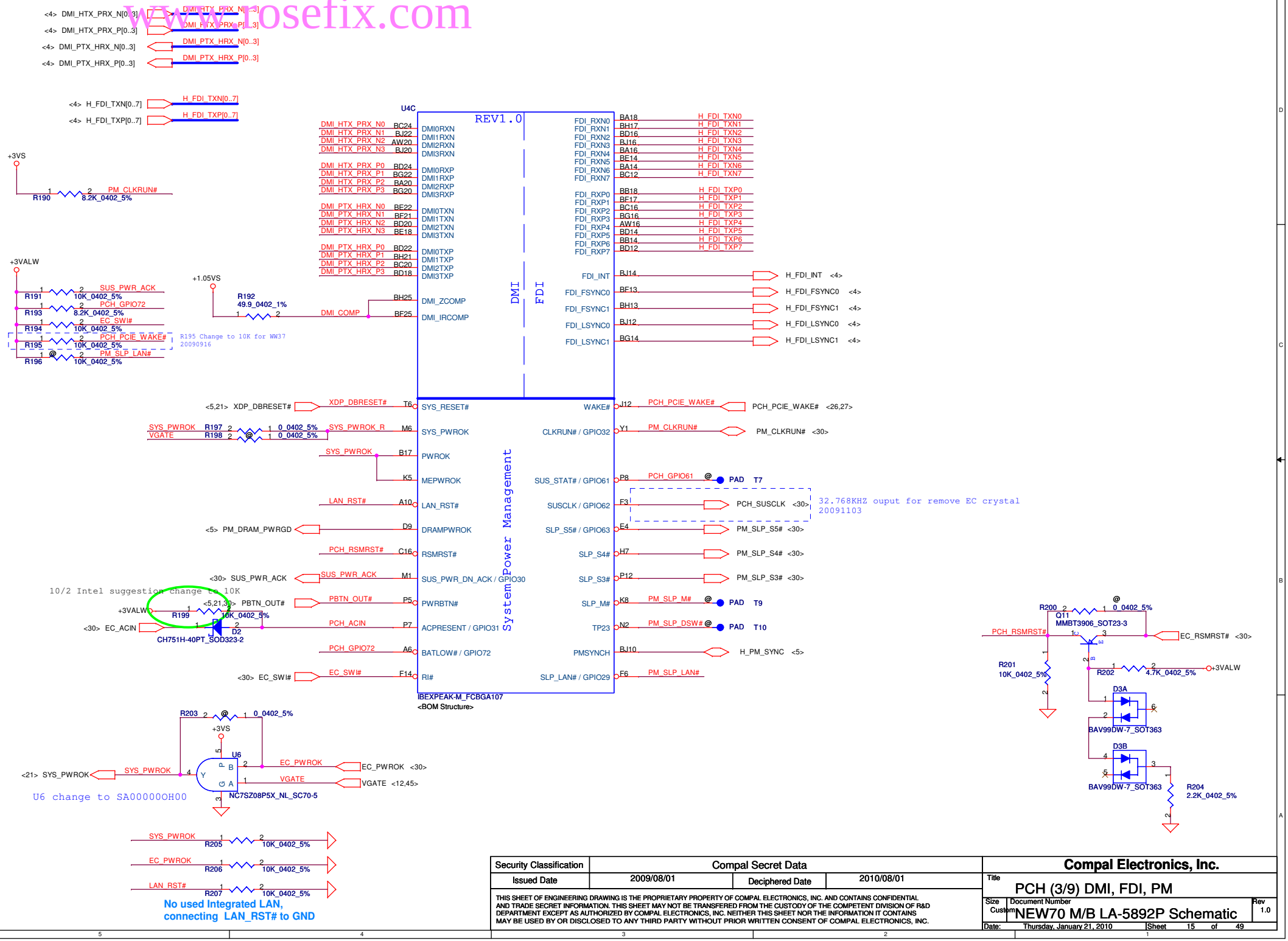
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 14 of 49



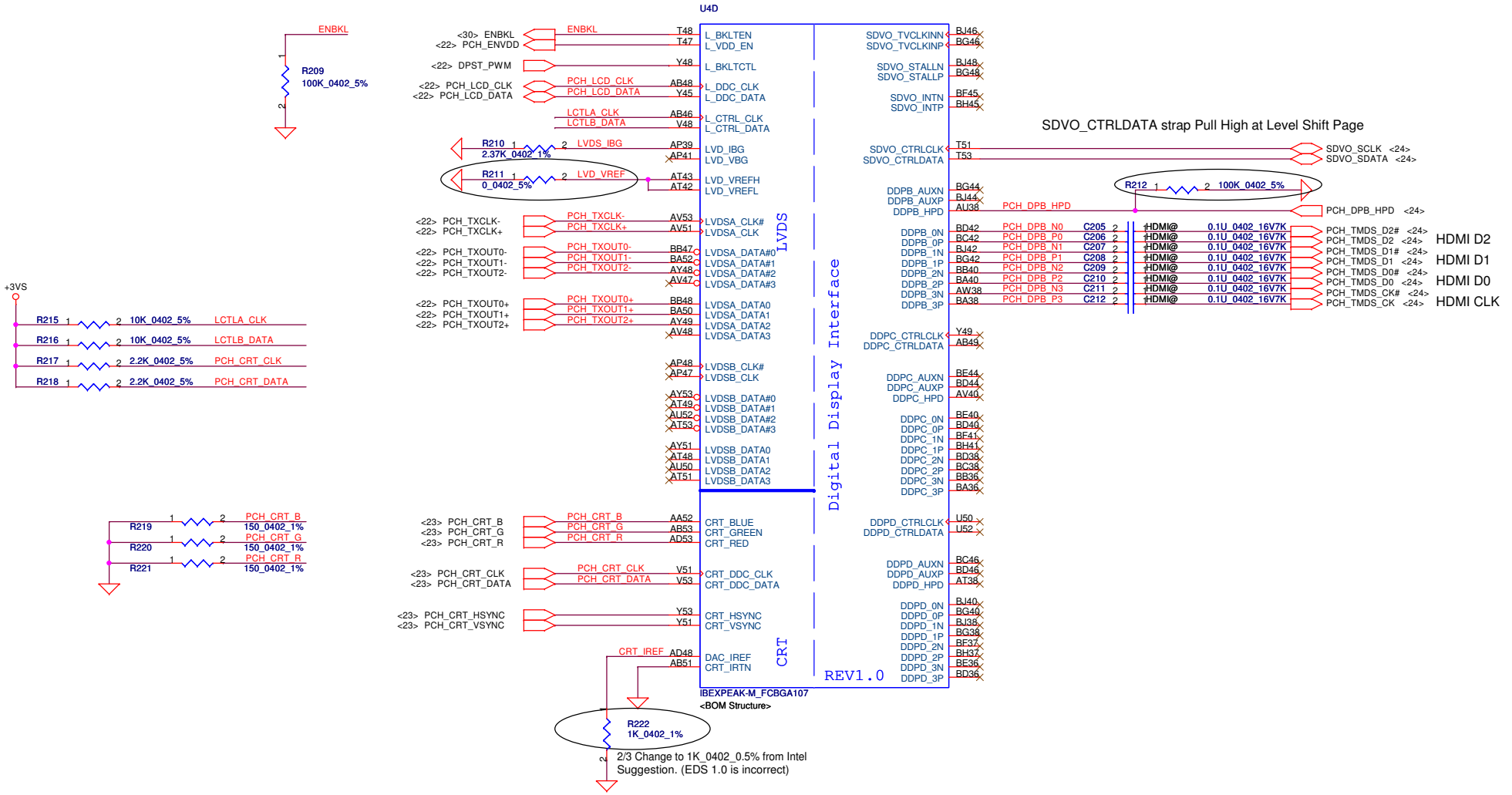
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 15 of 49



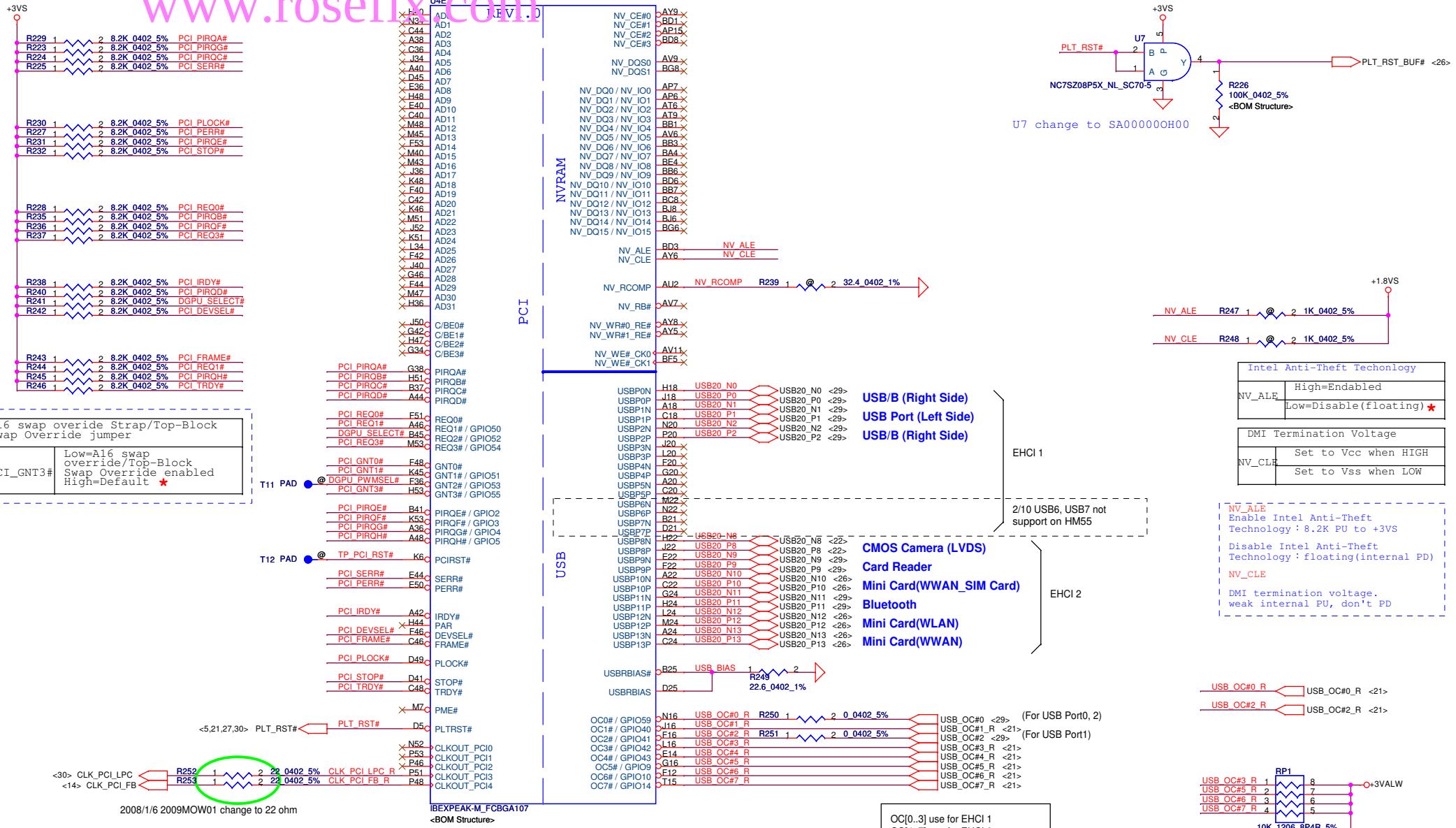
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 16 of 49



Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

* default

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

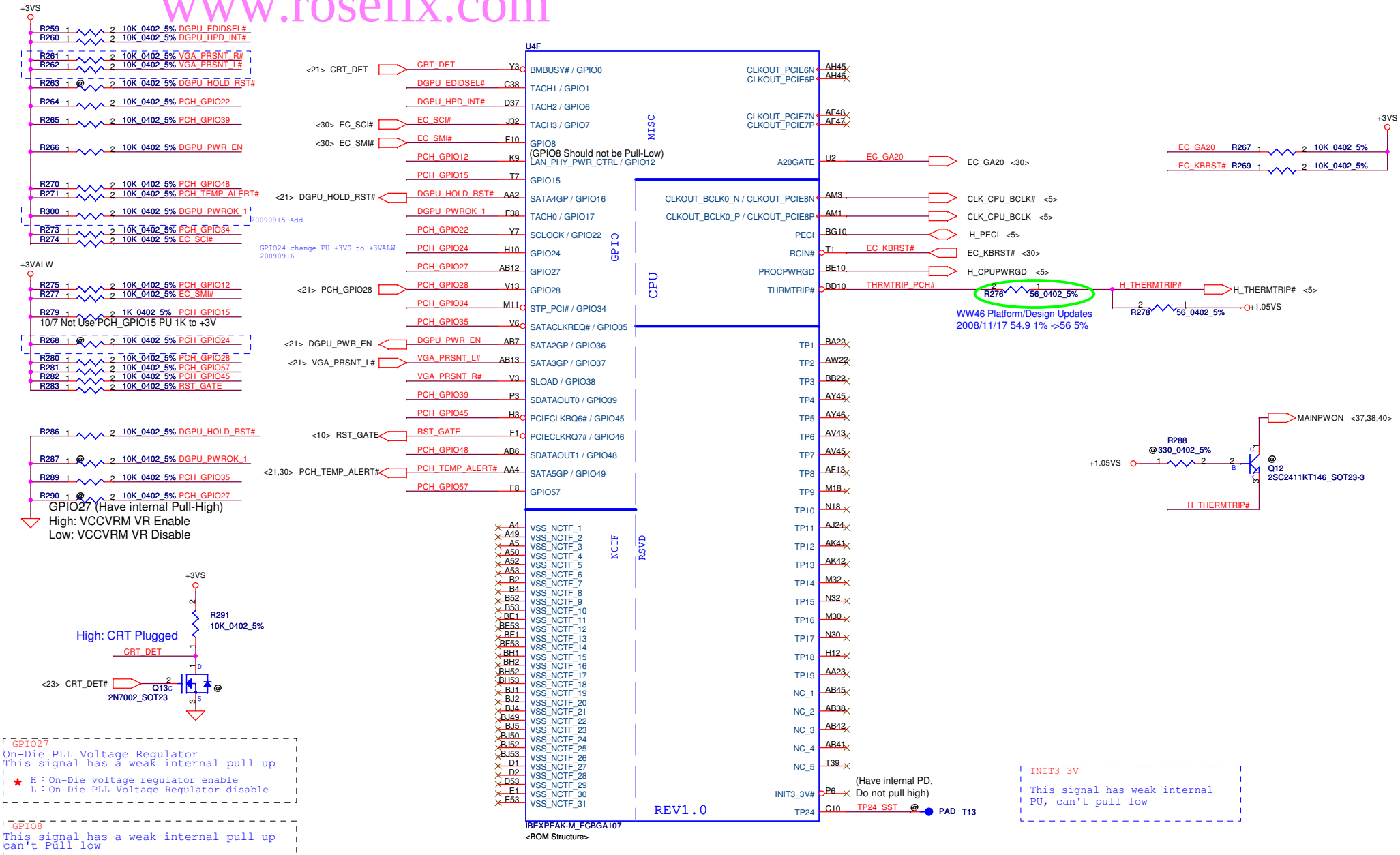
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 17 of 49



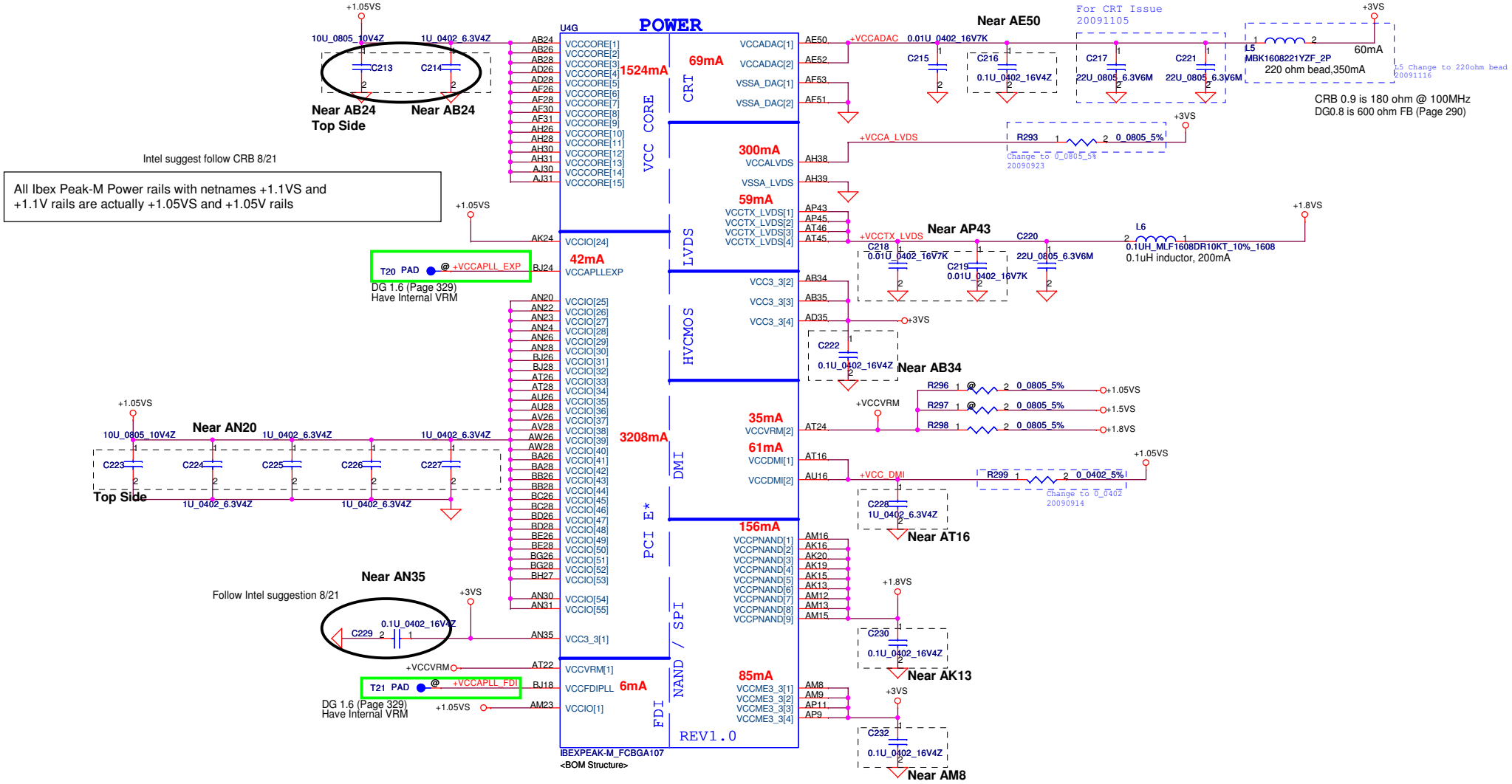
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 18 of 49



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

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POWER

U4J — REV1.0

All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

09/09/21 WW37 remove +VCCADPLLA,+VCCADPLLB external 1U

Follow Intel suggestion

2/12 Follow EDS1.11 Change to 100 ohm

Change to 1U for power sequence issue on ICH9

DG 1.6 (Page 329) Have Internal VRM

IBEXPEAK-M_FCBGA107
<BOM Structure>

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

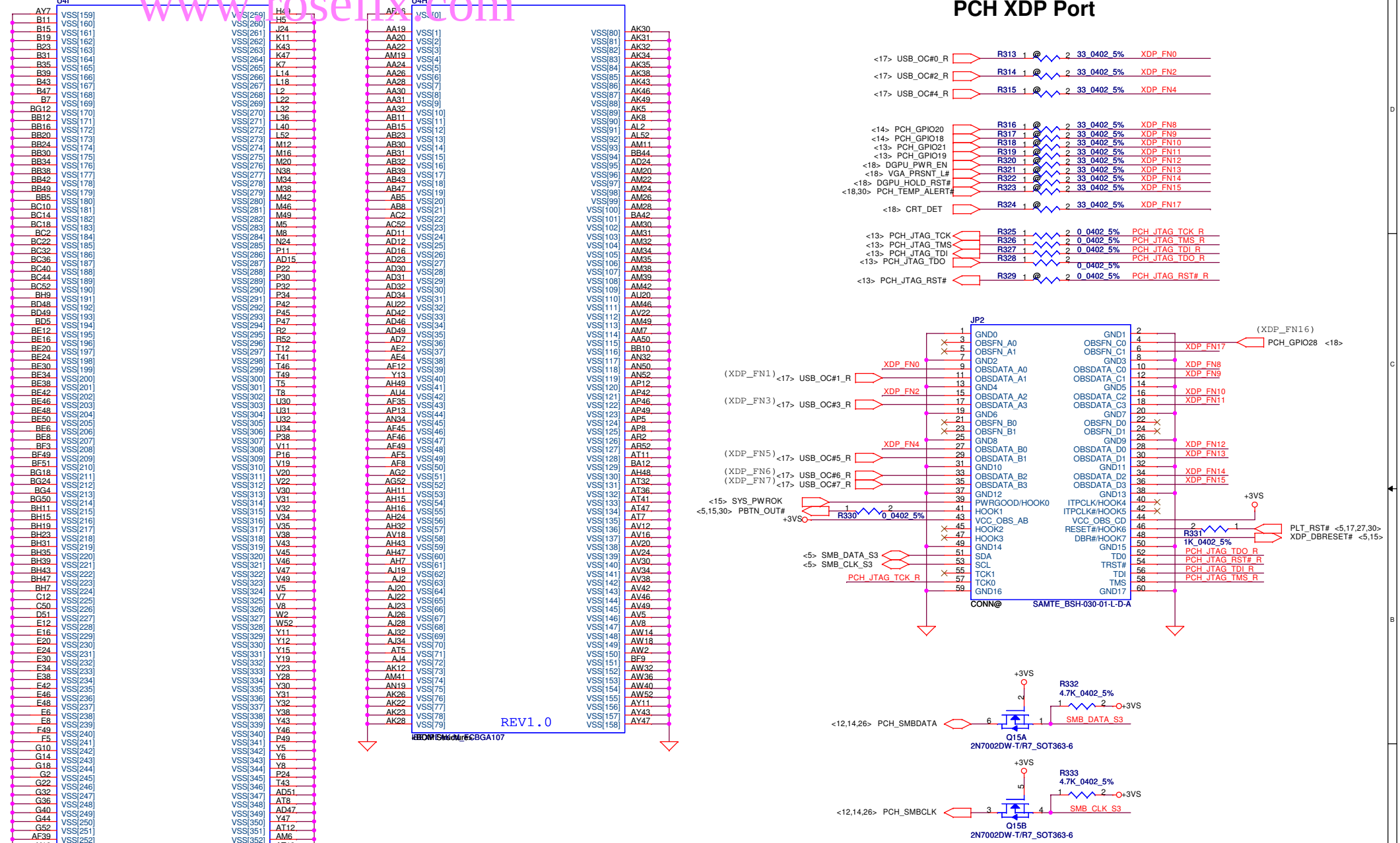
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 20 of 49

PCH XDP Port



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

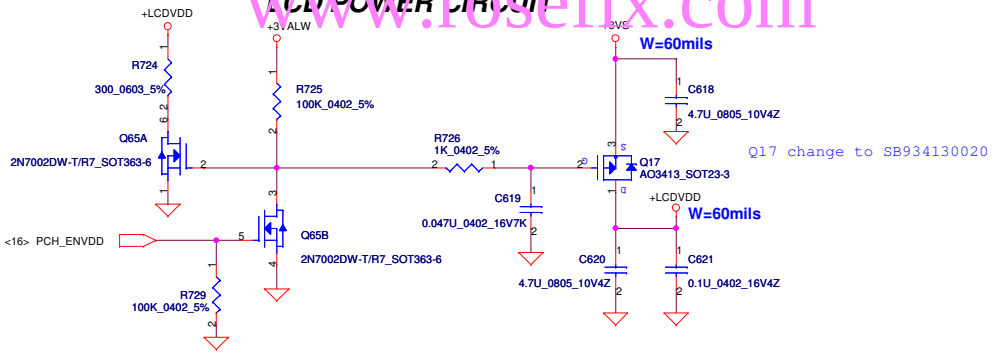
Compal Electronics, Inc.

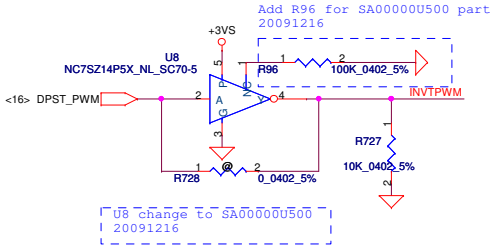
Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

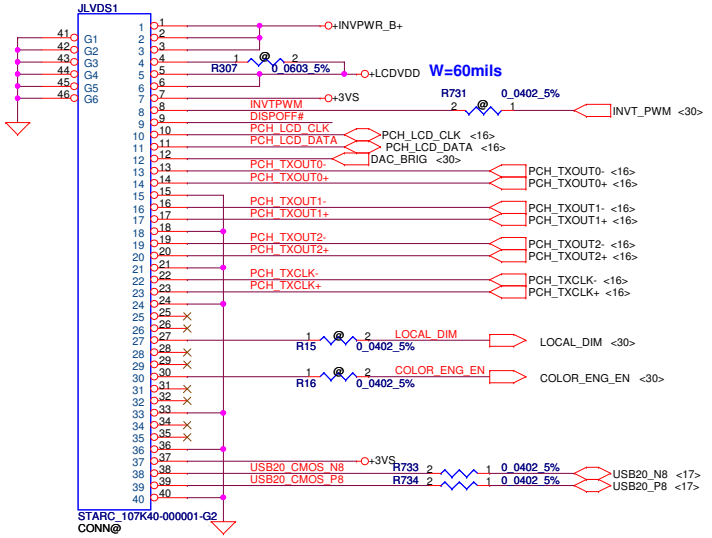
Date: Thursday, January 21, 2010 | Sheet 21 of 49

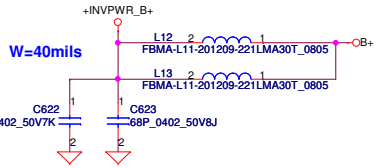
LCD POWER CIRCUIT

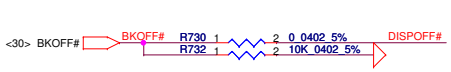


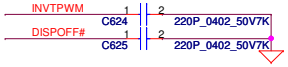


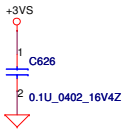
LED PANEL Conn.

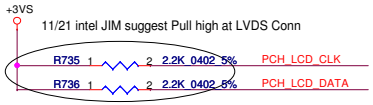


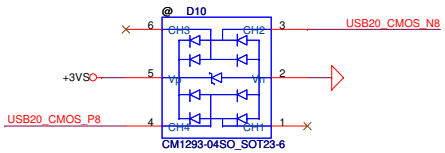












Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

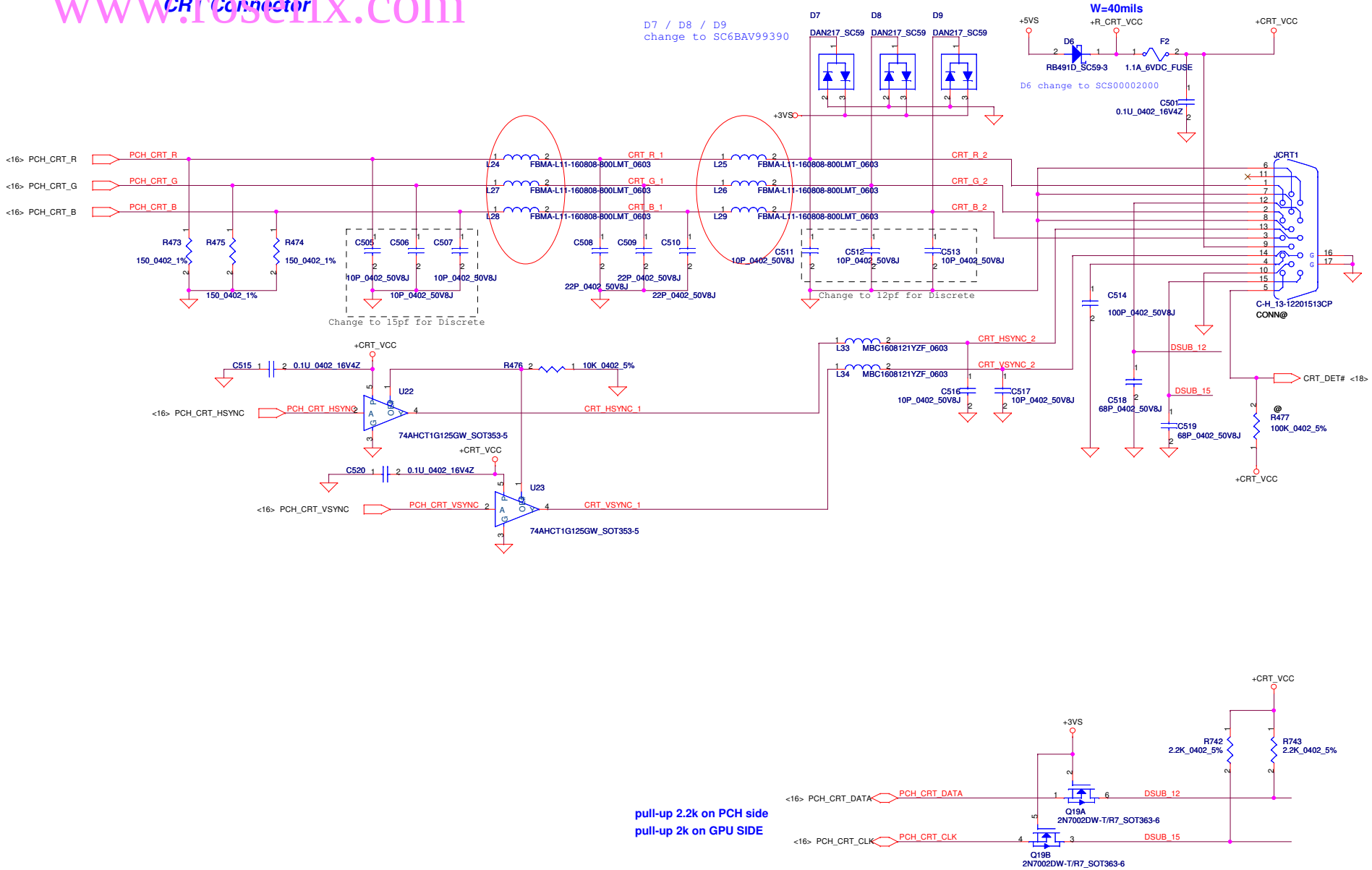
Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 22 of 49

CRT Connector



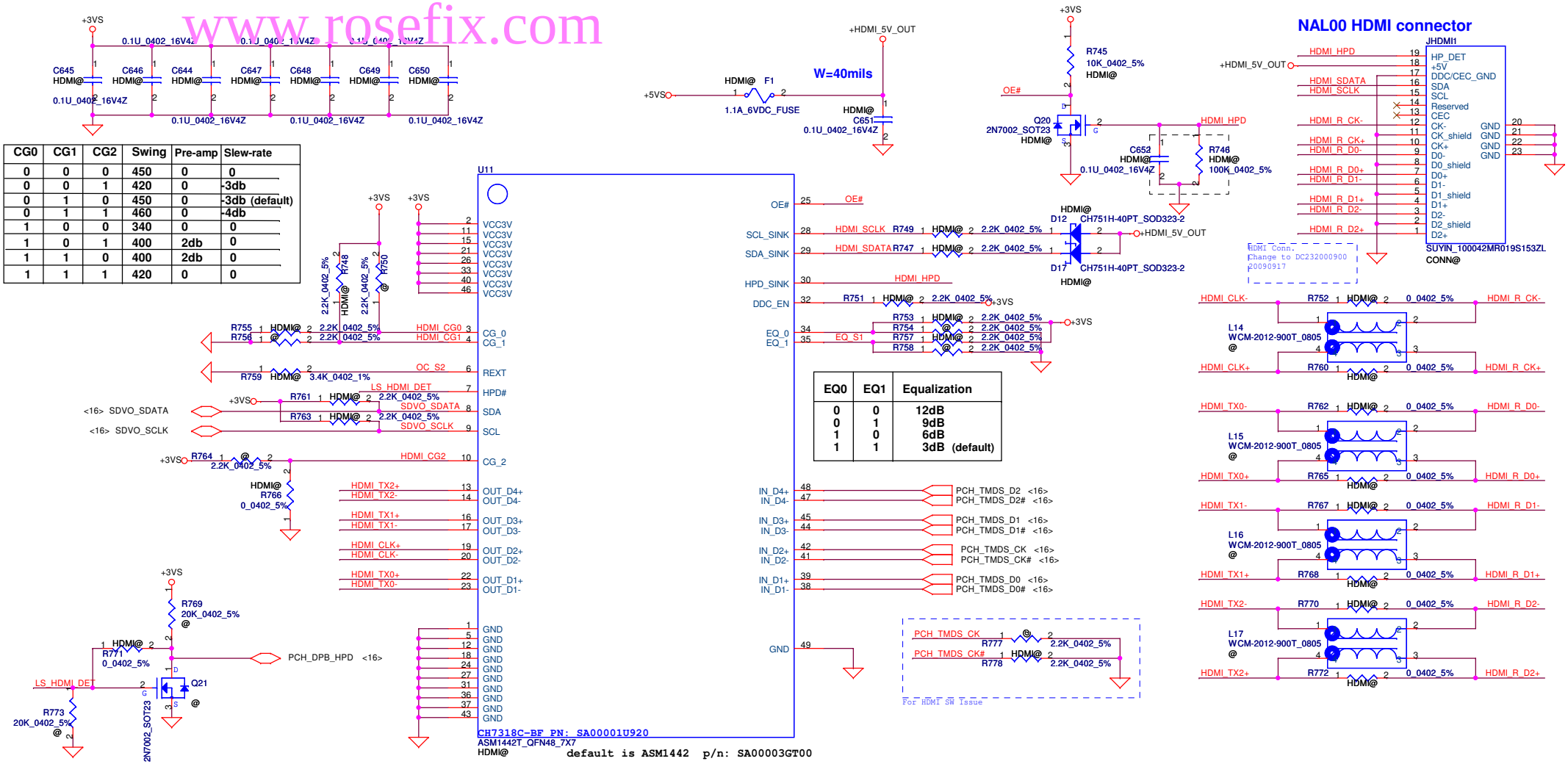
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

Date: Thursday, January 21, 2010 | Sheet 23 of 49



CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: HDMI Level Shife & Conn

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

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H1 H_3P0 H2 H_3P0 H3 H_3P0 H4 H_3P0 H6 H_3P0 H7 H_3P0 H8 H_3P0 H9 H_3P0 H10 H_3P0 H11 H_3P0 H12 H_3P0
H13 H_3P0 @ GNDA for AUDIO
H14 H_3P0

H21 H_4P2 H22 H_4P2 H23 H_4P2 H24 H_4P2

H18 H_3P4 @ JMINI1 Stand-off
H41 H_3P0X3P5N
H42 H_3P0N

FD8 FIDUCIAL_C40M80
FD7 FIDUCIAL_C40M80
FD5 FIDUCIAL_C40M80
FD6 FIDUCIAL_C40M80

SATA HDD1 Conn.

CL 4.0 mm

+3VS — C653 0.1U_0402_16V4Z
+5VS_HDD — C654 C655 C656 C657 — 0.1U_0402_16V4Z — 10U_0805_10V4Z — 1000P_0402_50V7K — 1U_0402_6.3V4Z

<13> SATA_PTX_DRX_P0 — C658 0.01U_0402_16V7K — SATA_PTX_C_DRX_P0
<13> SATA_PTX_DRX_N0 — C659 0.01U_0402_16V7K — SATA_PTX_C_DRX_N0
<13> SATA_DTX_C_PRX_N0 — C661 0.01U_0402_16V7K — SATA_DTX_PRX_N0
<13> SATA_DTX_C_PRX_P0 — C660 0.01U_0402_16V7K — SATA_DTX_PRX_P0

+3VS
+5VS — R774 0_0805_5% — +5VS_HDD

JHDD1
1 GND
2 A+
3 A-
4 GND
5 B-
6 B+
7 GND
8 V33
9 V33
10 V33
11 GND
12 GND
13 GND
14 V5
15 V5
16 V5
17 GND
18 Reserved
19 GND
20 V12
21 V12
22 V12
GND 24
GND 23

SANTA_192301-1
CONN@

20090915 Update to SANTA

Placea caps. near ODD CONN.

SATA ODD Conn.

+5VS_ODD — C662 C663 C664 C665 — 0.1U_0402_16V4Z — 10U_0805_10V4Z — 1000P_0402_50V7K — 1U_0402_6.3V4Z

<13> SATA_PTX_DRX_P1 — C666 0.01U_0402_16V7K — SATA_PTX_C_DRX_P1
<13> SATA_PTX_DRX_N1 — C667 0.01U_0402_16V7K — SATA_PTX_C_DRX_N1
<13> SATA_DTX_C_PRX_N1 — C668 0.01U_0402_16V7K — SATA_DTX_PRX_N1
<13> SATA_DTX_C_PRX_P1 — C669 0.01U_0402_16V7K — SATA_DTX_PRX_P1

+5VS — R775 @ 1K_0402_1% — +5VS_ODD
R776 0_0805_5%

JODD1
1 GND
2 A+
3 A-
4 GND
5 B-
6 B+
7 GND
8 DP
9 +5V
10 +5V
11 MD
12 GND
13 GND
GND 17
GND 16
GND 15
GND 14

OCTEK_SLS-13SB1G_RV
CONN@

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

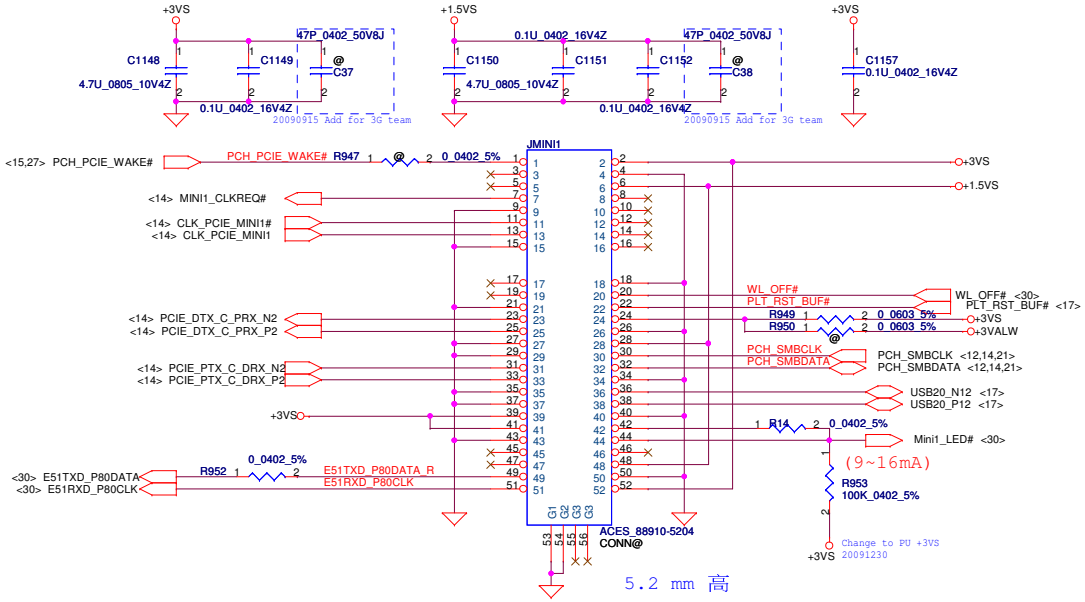
Compal Electronics, Inc.

Title: HDD & ODD & Screw Hole

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

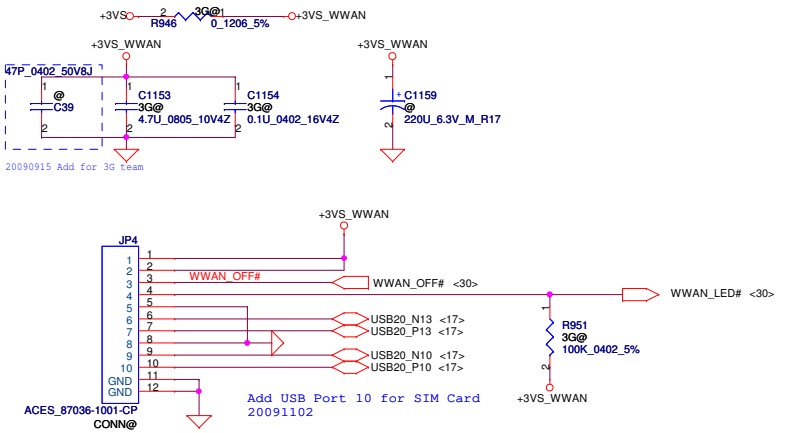
Date: Thursday, January 21, 2010 | Sheet 25 of 49

For Wireless LAN

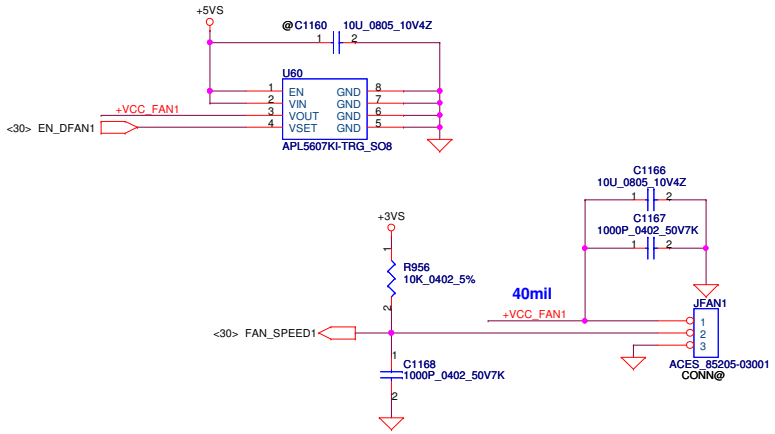


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

To 3G / GPS Module Connect



FAN1 Conn



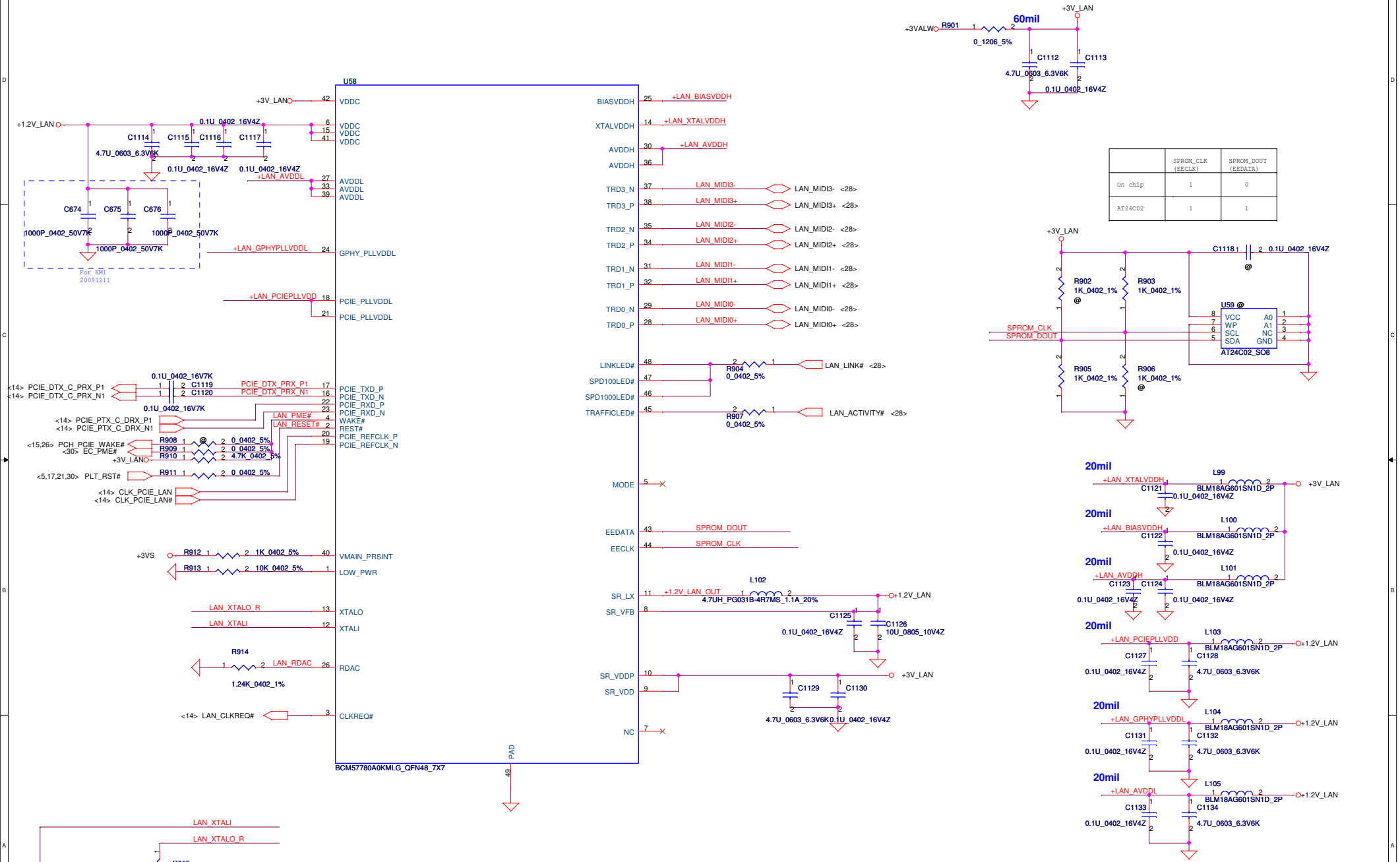
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: MINI CARD (WLAN & 3G)/FAN

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

Date: Thursday, January 21, 2010 Sheet 26 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

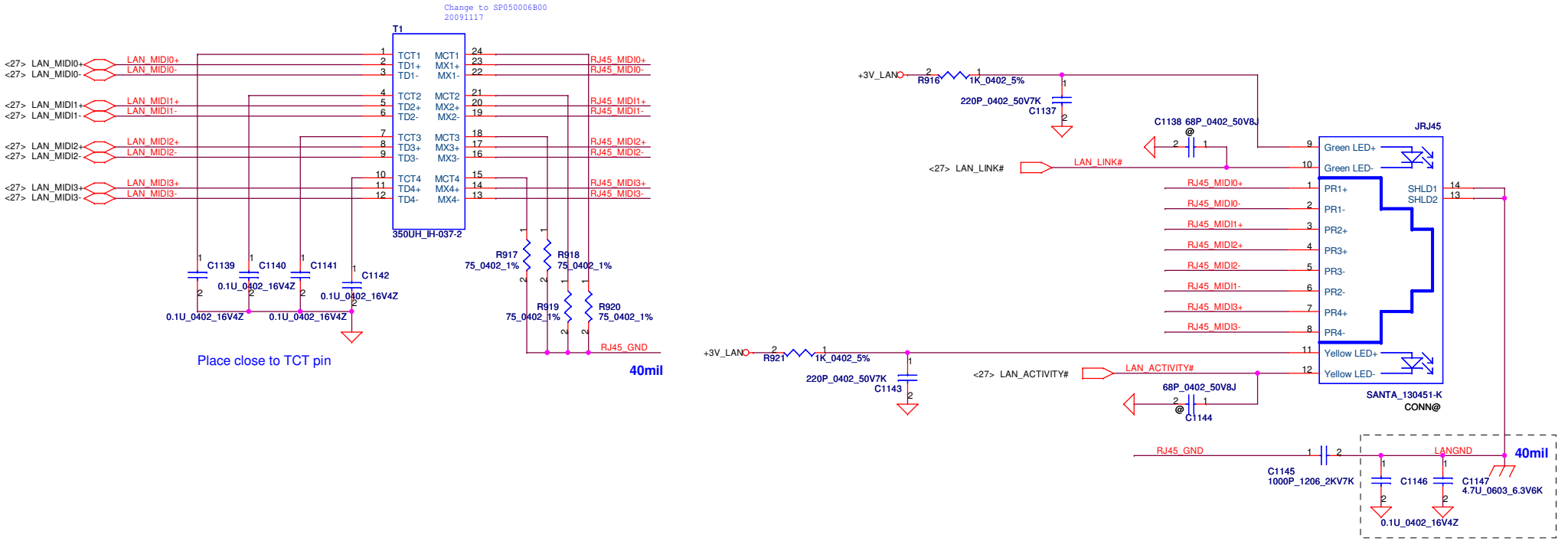
Compal Electronics, Inc.

Title: Broadcom BCM57780

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 27 of 49

LAN Connector



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

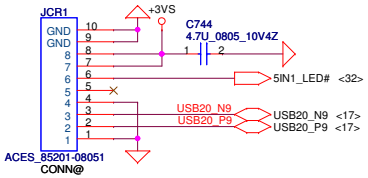
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

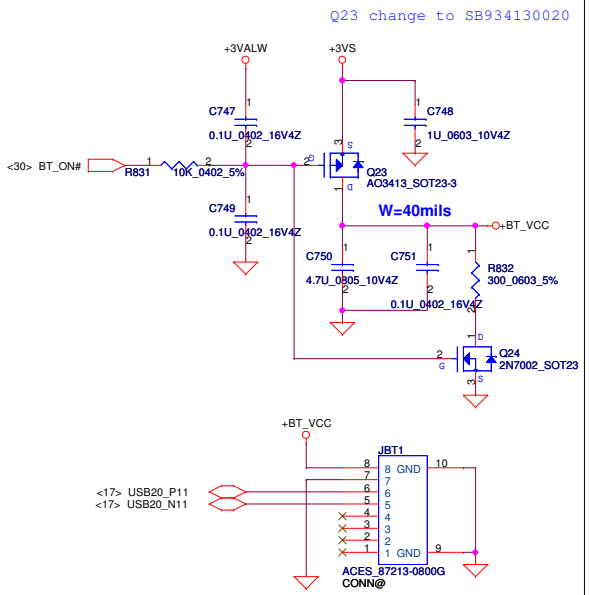
Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

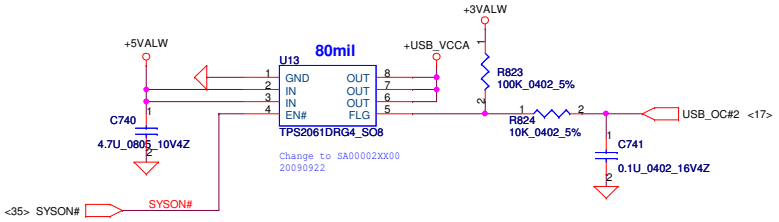
Date: Thursday, January 21, 2010 | Sheet 28 of 49

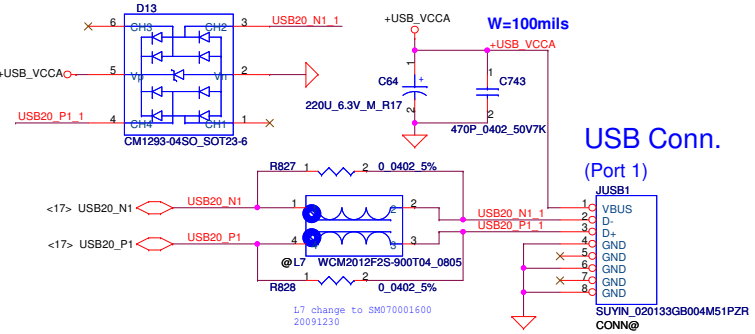
Card Reader Conn.

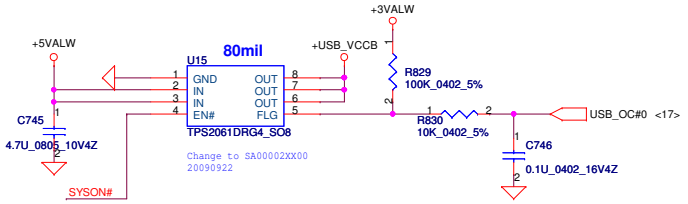


Bluetooth Conn.



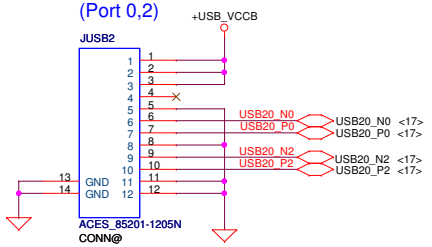






USB/B Conn.

(Port 0,2)



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: NEW CARD & eSATA Connector

Size: B | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 29 of 49

For EC Tools

U16 — KB926QFD3_LQFP128_14X14 — 20mil

GPIO: GA20/GPIO00, KBRST#/GPIO01, SERIRQ#, LFRAME#, LAD3, LAD2, LAD1, LAD0, PCICLK, PCIRST#/GPIO05, ECRST#, SCI#/GPIO0E, CLKRUN#/GPIO1D, KSI0/GPIO30, KSI1/GPIO31, KSI2/GPIO32, KSI3/GPIO33, KSI4/GPIO34, KSI5/GPIO35, KSI6/GPIO36, KSI7/GPIO37, KSO0/GPIO20, KSO1/GPIO21, KSO2/GPIO22, KSO3/GPIO23, KSO4/GPIO24, KSO5/GPIO25, KSO6/GPIO26, KSO7/GPIO27, KSO8/GPIO28, KSO9/GPIO29, KSO10/GPIO2A, KSO11/GPIO2B, KSO12/GPIO2C, KSO13/GPIO2D, KSO14/GPIO2E, KSO15/GPIO2F, KSO16/GPIO48, KSO17/GPIO49, SCL1/GPIO44, SDA1/GPIO45, SCL2/GPIO46, SDA2/GPIO47, PM_SLP_S3#/GPIO04, PM_SLP_S5#/GPIO07, EC_SMI#/GPIO08, LID_SW#/GPIO0A, SUSP#/GPIO0B, PBTN_OUT#/GPIO0C, EC_PME#/GPIO0D, EC_THERM#/GPIO11, FAN_SPEED1/FANFB1/GPIO14, FANFB2/GPIO15, EC_TX/GPIO16, EC_RX/GPIO17, ON_OFF/GPIO18, PWR_LED#/GPIO19, NUMLED#/GPIO1A, XCLK1, XCLK0, INVT_PWM/PWM1/GPIO0F, BEEP#/PWM2/GPIO10, FANPWM1/GPIO12, ACOFF/FANPWM2/GPIO13, BATT_TEMP/AD0/GPIO38, BATT_OVP/AD1/GPIO39, ADP_I/AD2/GPIO3A, AD3/GPIO3B, AD4/GPIO42, SELIO2#/AD5/GPIO43, DAC_BRIG/DA0/GPIO3C, EN_DFAN1/DA1/GPIO3D, IREF/DA2/GPIO3E, DA3/GPIO3F, PSCLK1/GPIO4A, PSDAT1/GPIO4B, PSCLK2/GPIO4C, PSDAT2/GPIO4D, TP_CLK/PSCLK3/GPIO4E, TP_DATA/PSDAT3/GPIO4F, SDICS#/GPXOA00, SDICLK/GPXOA01, SDIDO/GPXOA02, SDIDI/GPXID0, SPIDI/RD#, SPIDO/WR#, SPICLK/GPIO58, SPICS#, CIR_RX/GPIO40, CIR_RLC_TX/GPIO41, FSTCHG/SELIO#/GPIO50, BATT_CHGI_LED#/GPIO52, CAPS_LED#/GPIO53, BATT_LOW_LED#/GPIO54, SUSP_LED#/GPIO55, SYSON/GPIO56, VR_ON/XCLK32K/GPIO57, AC_IN/GPIO59, EC_RSMRST#/GPXO03, EC_LID_OUT#/GPXO04, EC_ON/GPXO05, EC_SWI#/GPXO06, ICH_PWROK/GPXO06, BKOFF#/GPXO08, WL_OFF#/GPXO09, GPXO10, GPXO11, PM_SLP_S4#/GPXID1, ENBKL/GPXID2, GPXID3, GPXID4, GPXID5, GPXID6, GPXID7, V18R

Power Rails: +3VALW, +3VALW_EC, +EC_VCCA, +3VS, +5VS, ECAGND, AVCC, VCC, GND, AGND

Crystal: X2 32.768KHZ_12.5PF_Q13MC14610002 — C764 15P_0402_50V8J — C765 15P_0402_50V8J — R13 0_0402_5%

Notes:
- 1.Use crystal X2,remove R13.
- 2.Use PCH_SUSCLK,remove X1. 20091103
- P80DATA PD 100K for EC common design 20091105
- For LVDS Function 20091209 Add
- 10/1 ENE Recommand
- EC suggested 2.2K for SMBus
- 10/1 EC Recommand

Analog Board ID definition, Please see page 3.

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: EC ENE KB926

Size: B | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

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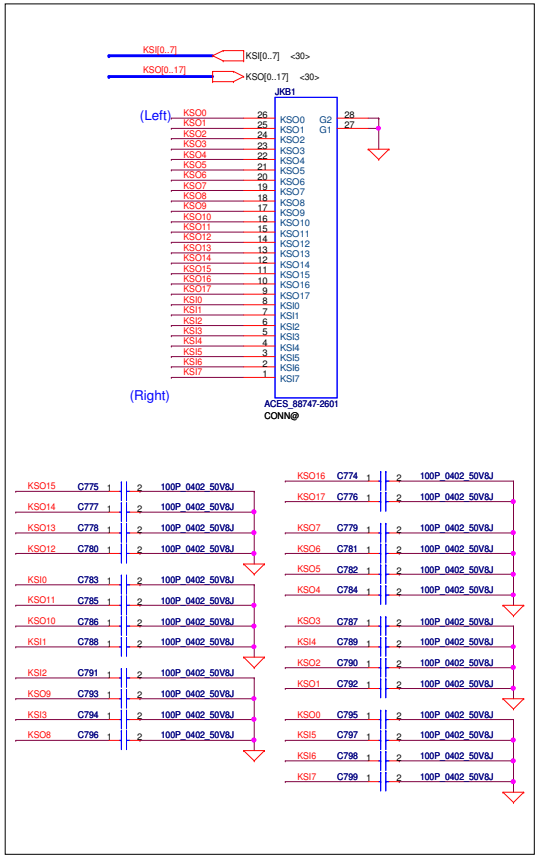

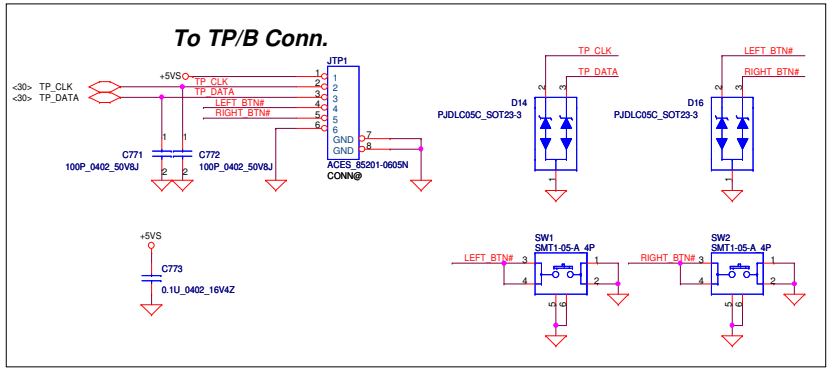

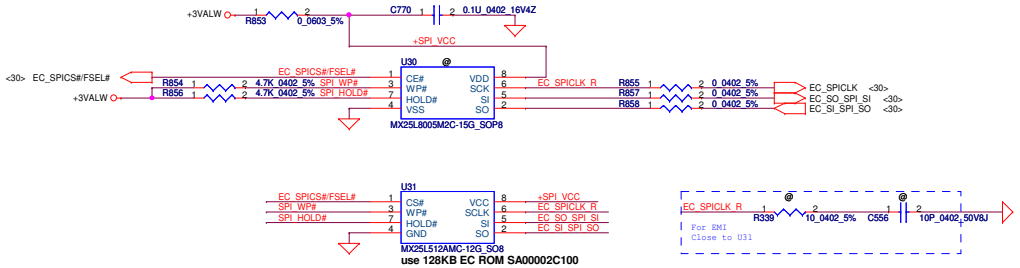

ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

To BTN/B Conn.

	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size: C | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

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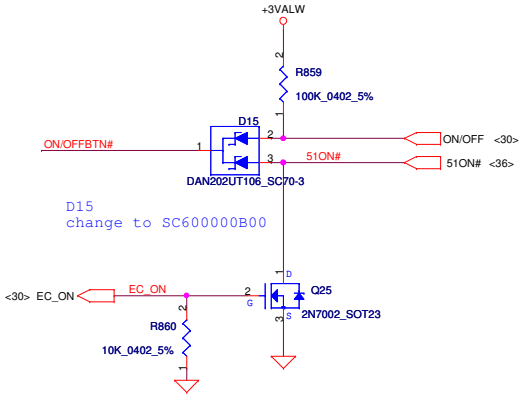
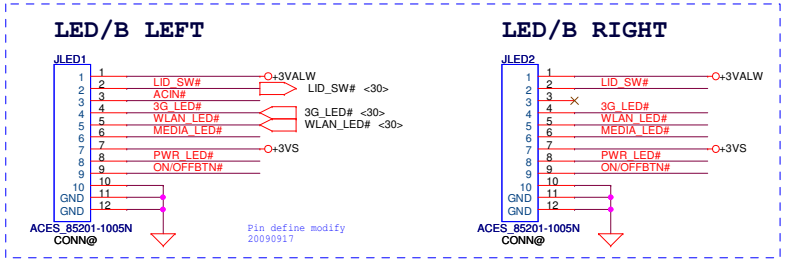
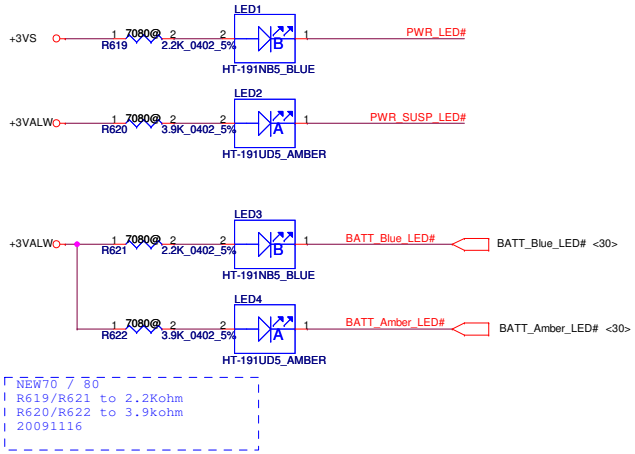
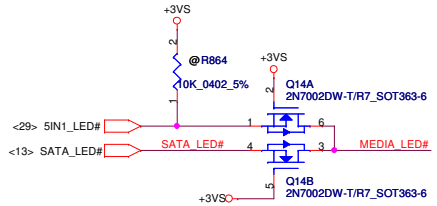
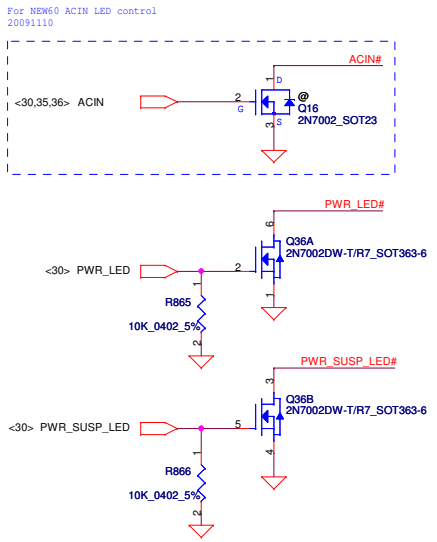
Power Button











Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: <Title>

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

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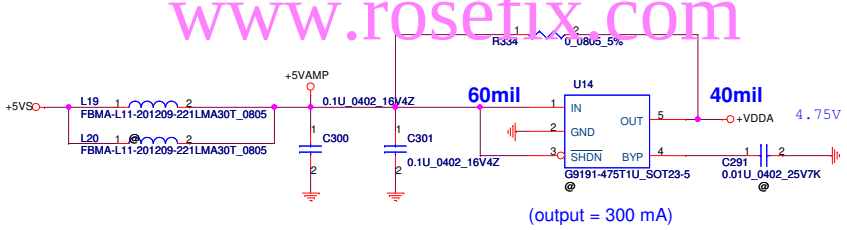
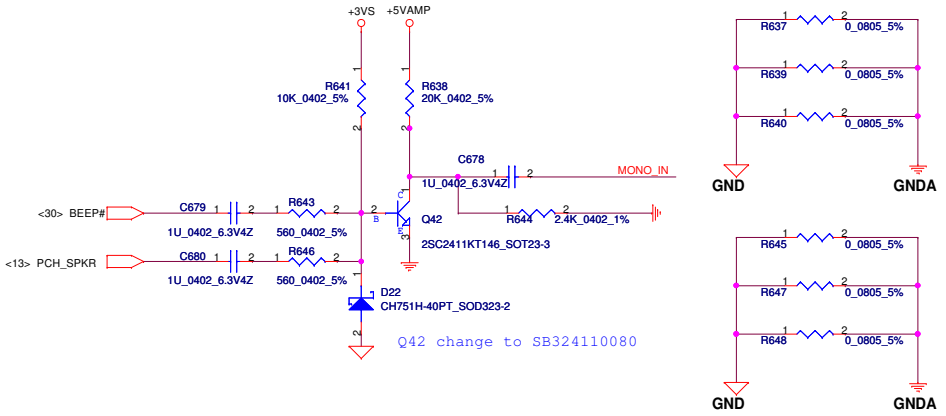
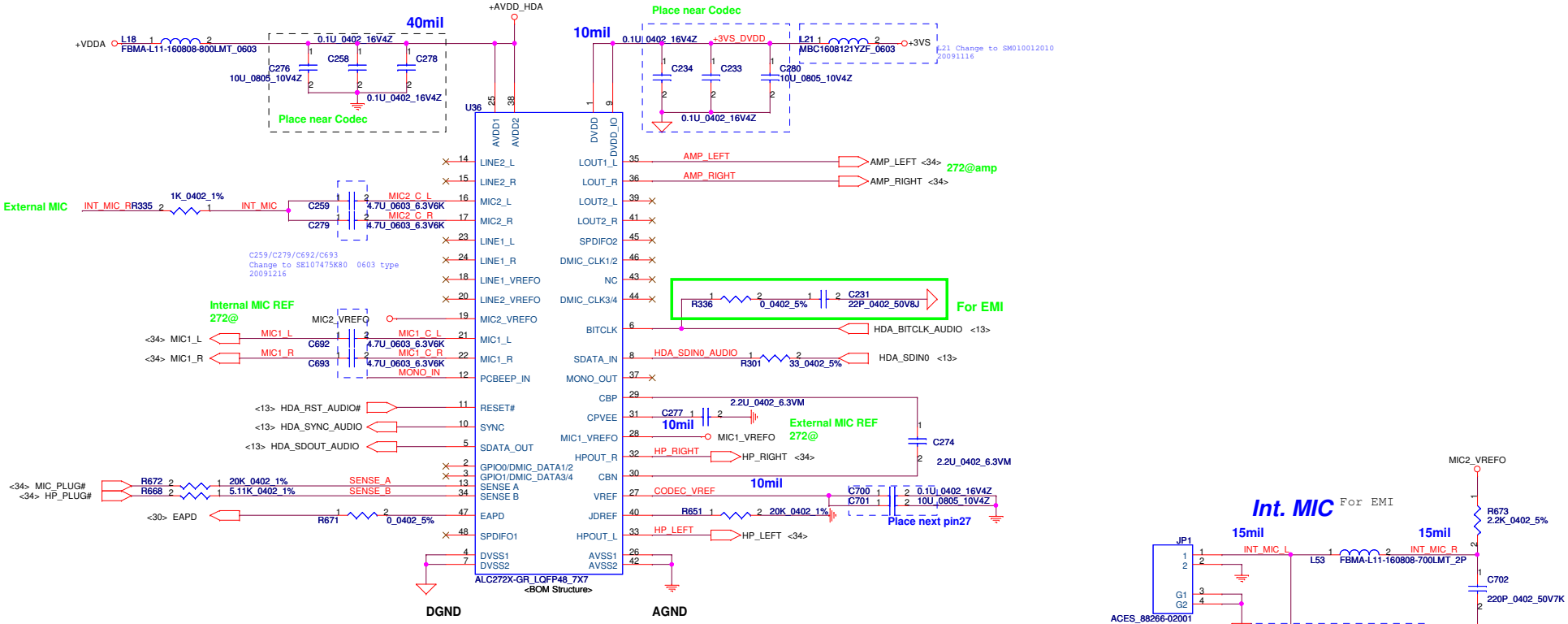




HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: HD Audio Codec ALC271X/272X

Size: Custom | Document Number: NEW70 M/B LA-5892P Schematic | Rev: 1.0

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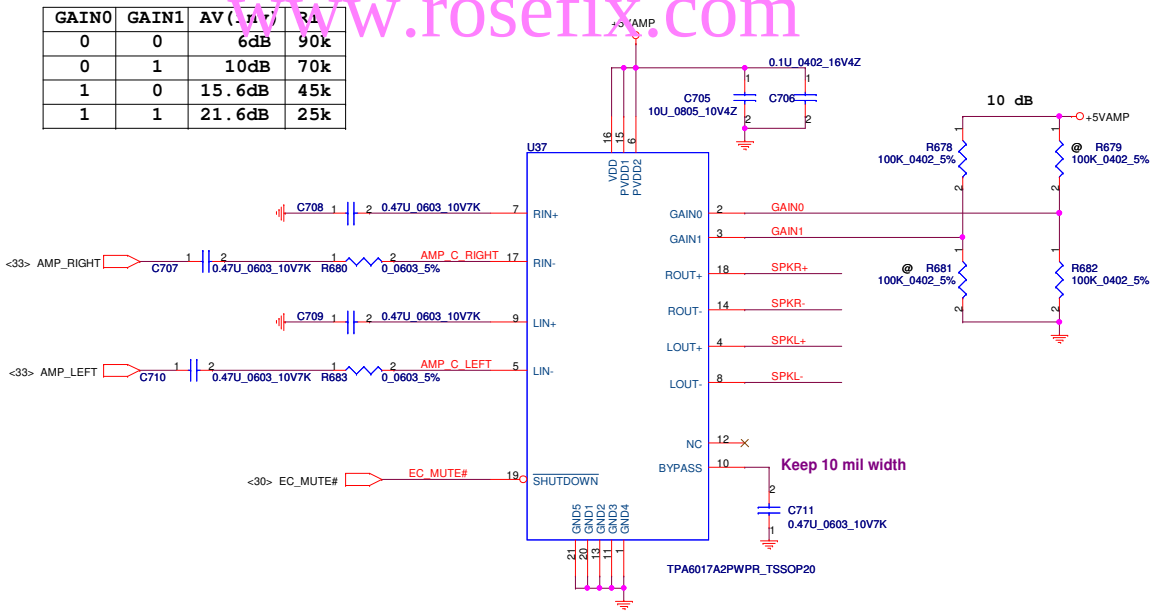
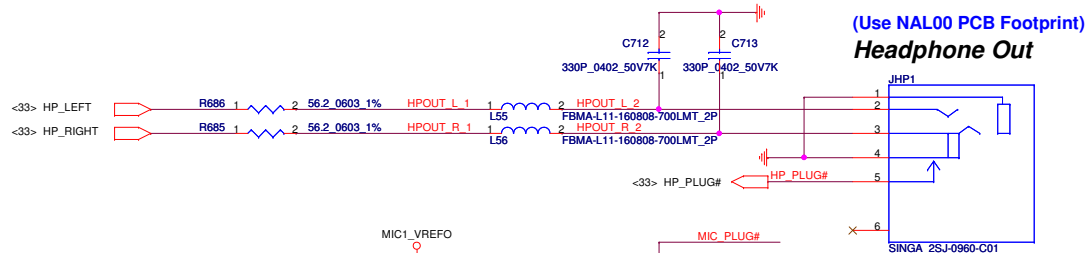
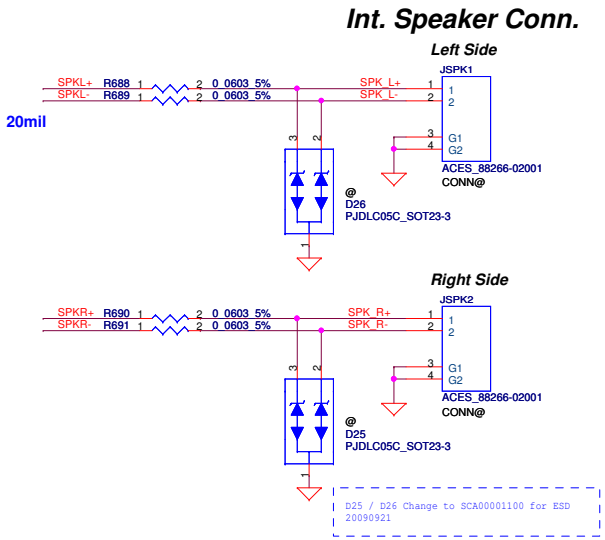
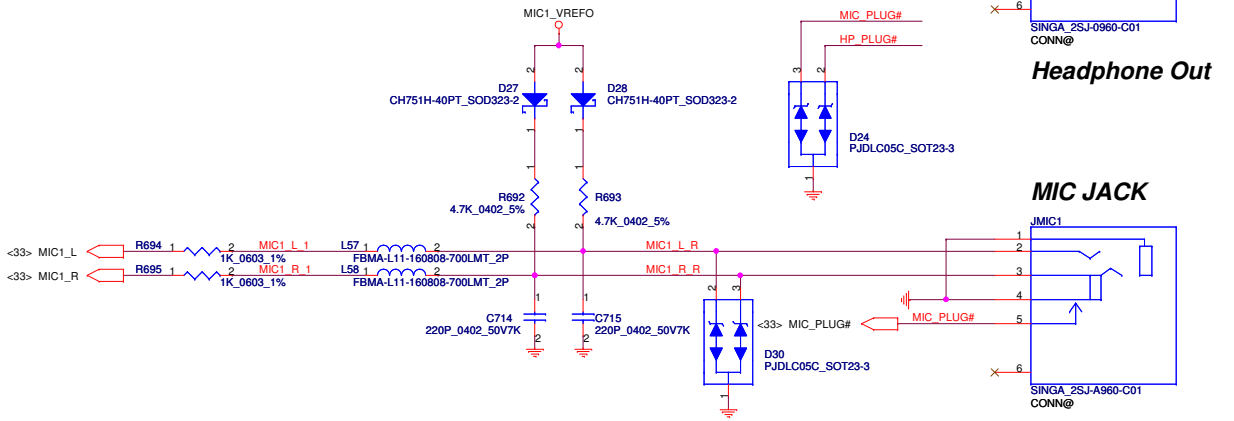
GAIN0	GAIN1	AV(...)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k









Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size	Document Number	Rev
Custom	NEW70 M/B LA-5892P Schematic	1.0

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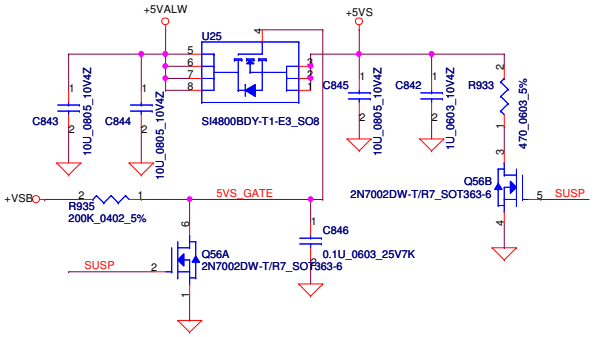
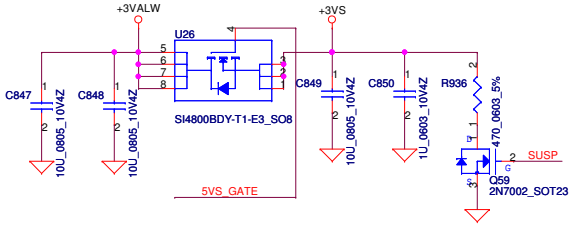
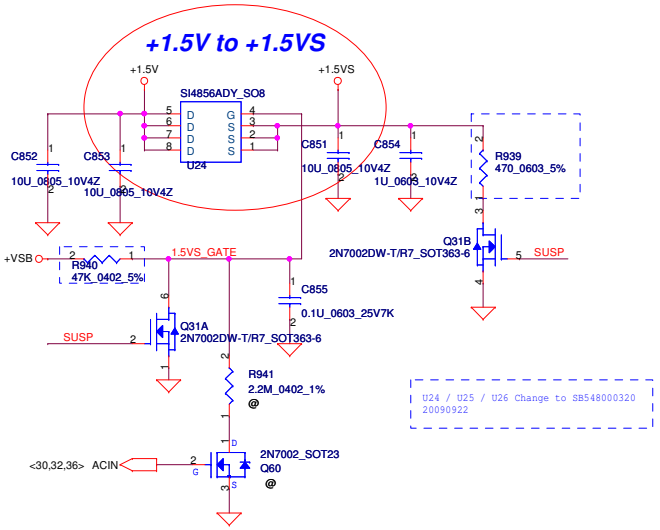
+5VALW TO +5VS



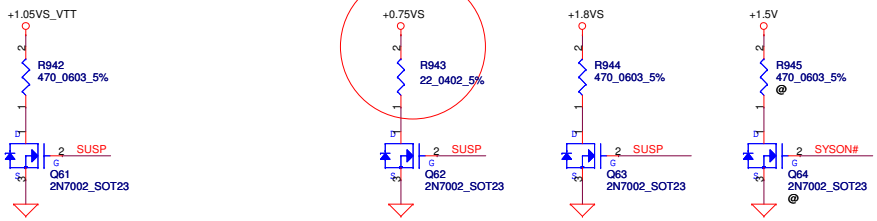
+3VALW TO +3VS

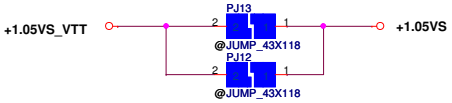


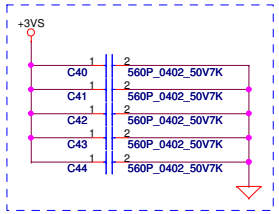
+1.5V to +1.5VS



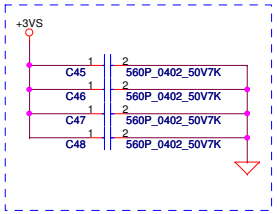
U24 / U25 / U26 Change to SB548000320
20090922



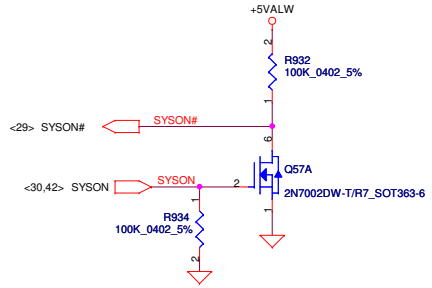


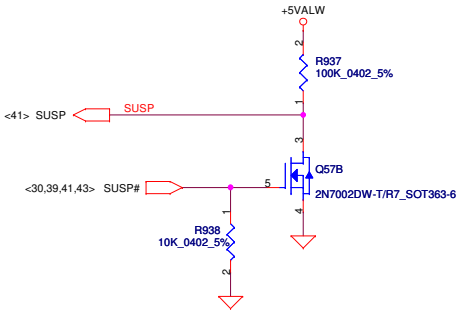


For EMI
200911092130



For LAM Common mode noise
200911102330





Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	NEW70 M/B LA-5892P Schematic	1.0

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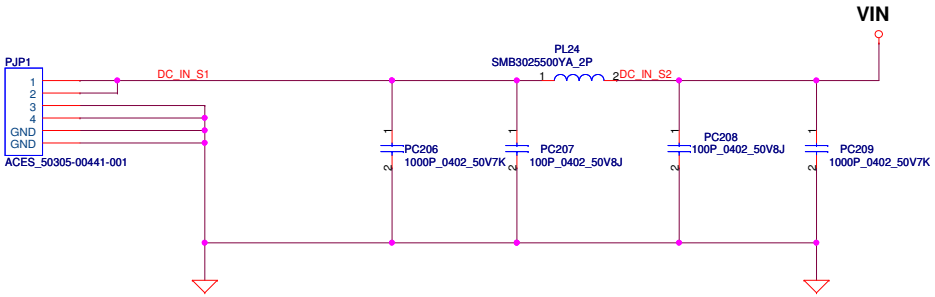
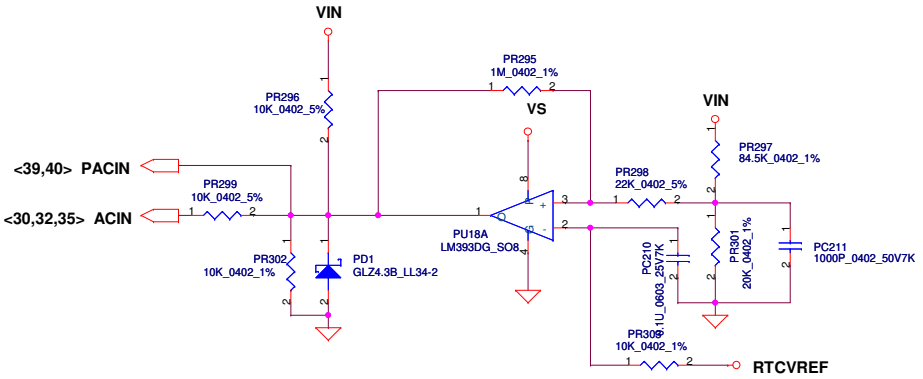
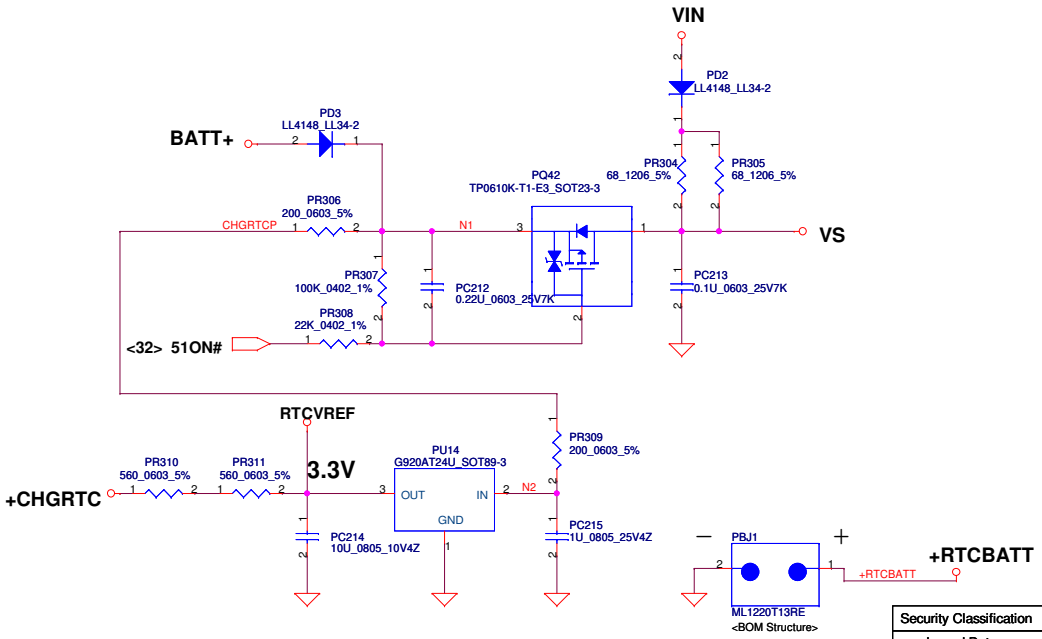
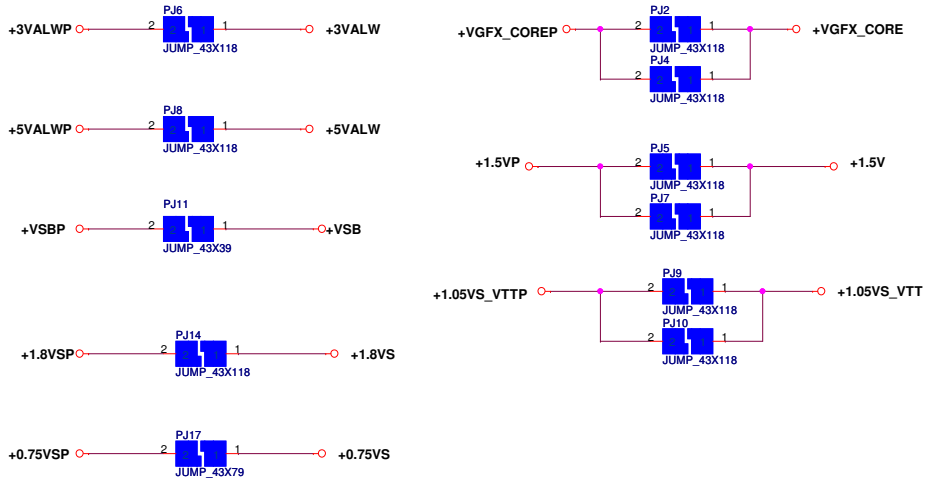




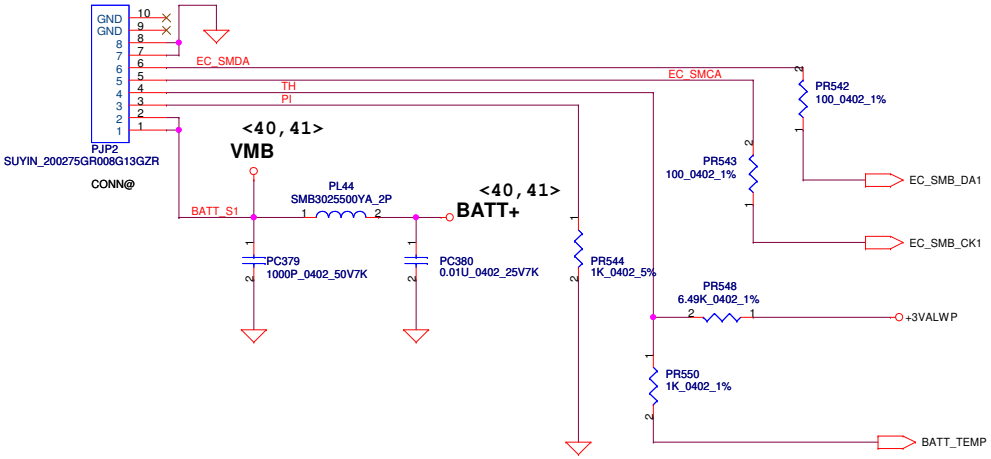
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

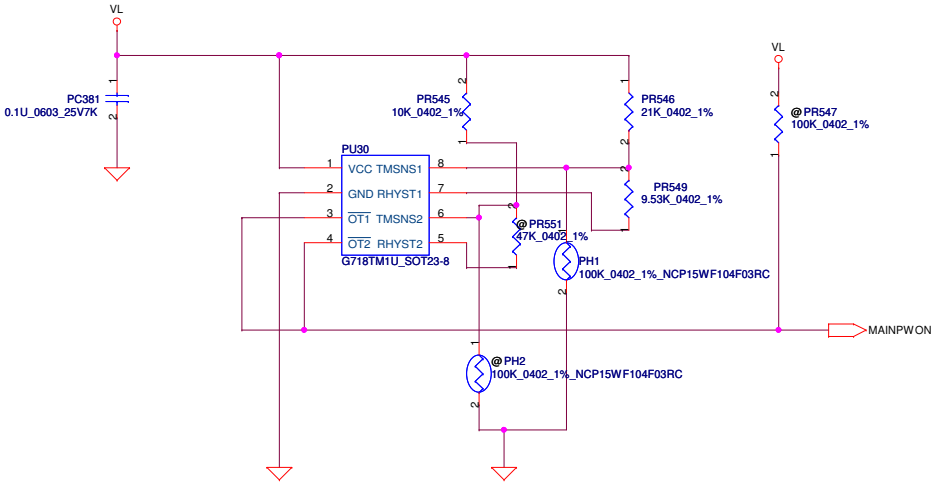
Compal Electronics, Inc.	
Title	DCIN & DETECTOR
Size: Custom	Document Number: NALG0
Rev	1.0
Date: Thursday, January 21, 2010	Sheet 36 of 49

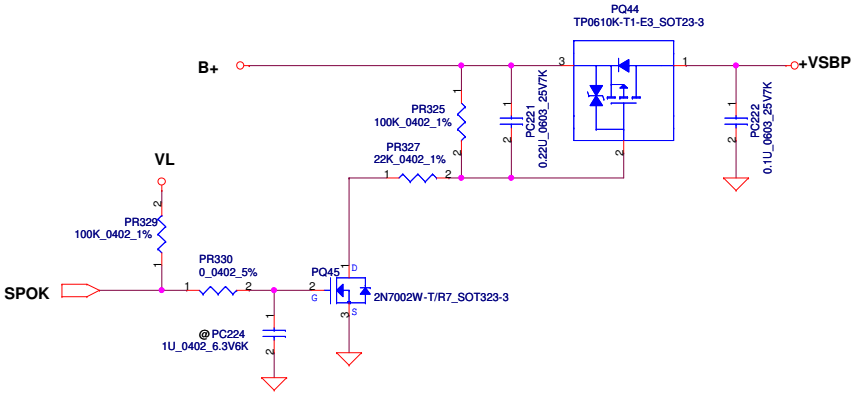


PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C





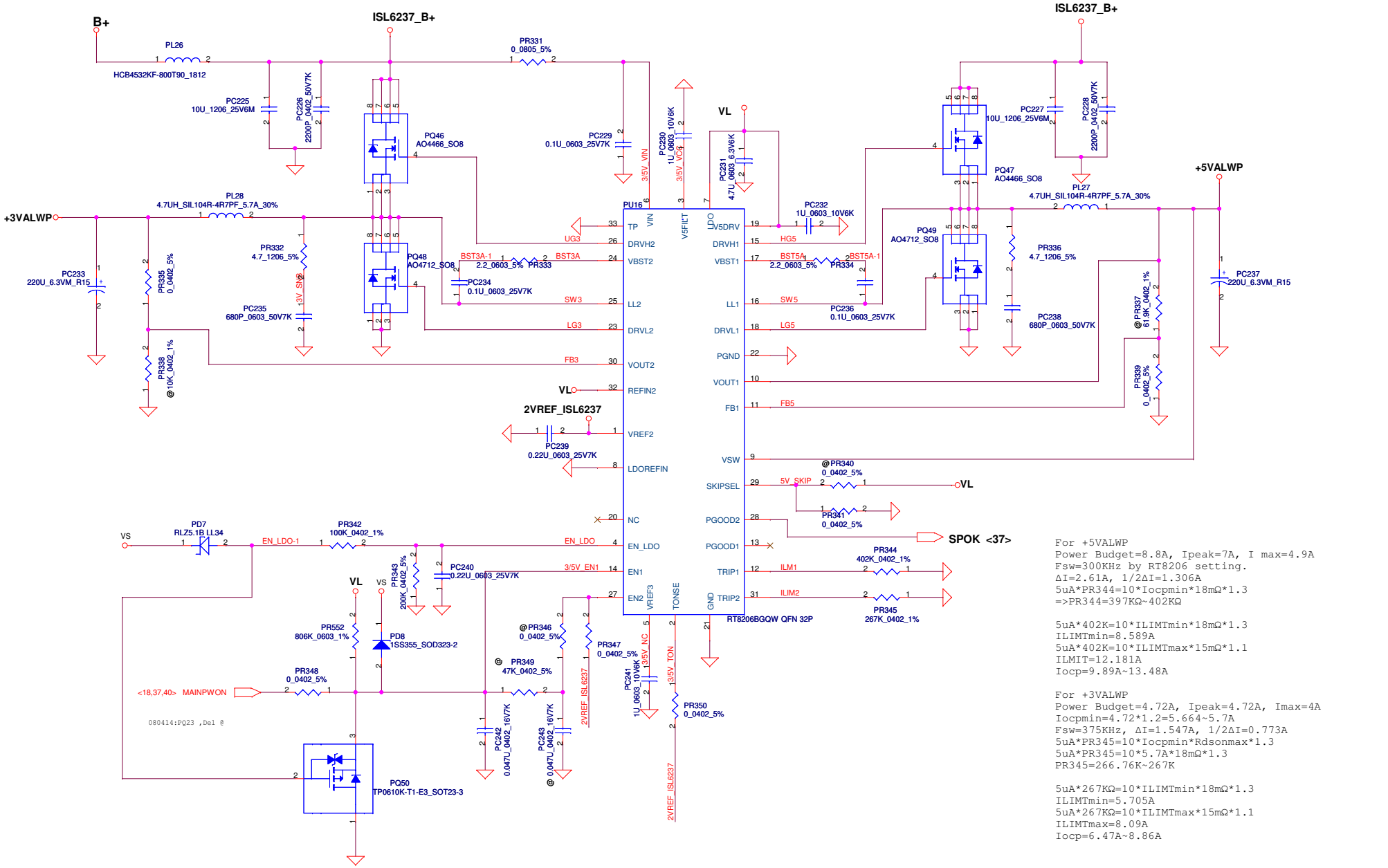
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	NALG0	1.0

Date: Thursday, January 21, 2010 | Sheet 37 of 49



For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=300KHz by RT8206 setting.
ΔI=2.61A, 1/2ΔI=1.306A
5uA*PR344=10*Iocpmin*18mΩ*1.3
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.3
ILIMTmin=8.589A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=9.89A~13.48A

For +3VALWP
Power Budget=4.72A, Ipeak=4.72A, Imax=4A
Iocpmin=4.72*1.2=5.664~5.7A
Fsw=375KHz, ΔI=1.547A, 1/2ΔI=0.773A
5uA*PR345=10*Iocpmin*Rdsonmax*1.3
5uA*PR345=10*5.7A*18mΩ*1.3
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ*1.3
ILIMTmin=5.705A
5uA*267KΩ=10*ILIMTmax*15mΩ*1.1
ILIMTmax=8.09A
Iocp=6.47A~8.86A

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: MB Schematic | Rev: 1.0

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Iada=0~4.74A(90W/19V=4.73A)
Iada=0~3.42A(90W/19V=3.42A)

CC = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A

VIN
B+
P2
P3
CHG_B+
PQ51 AO4407A_SO8
PQ52 AO4407A_SO8
PR351 0.02_2512_1%
PL45 HCB4532KF-800T90_1812
PQ53 AO4407A_SO8
PR352 47K_0402_1%
PR353 47K_0402_1%
PR354 200K_0402_1%
PC248 5600P_0402_25V7K
PC249 0.1U_0603_25V7K
PQ54 TP0610K-T1-E3_SOT23-3
PR355 100K_0402_1%
PQ55 PDTC115EU_SOT323
PR356 10K_0402_1%
PD9 1SS355_SOD323-2
PR357 200K_0402_1%
PQ56 PDTA144EU_SOT323-3
PD10 BAS40CW_SOT323-3
PD11 1SS355_SOD323-2
PR358 100K_0402_1%
PQ57 PDTC115EU_SOT323
PD12 1SS355_SOD323-2
PR359 10K_0402_5%
PC250 2.2U_0603_6.3V6K
PC252 0.1U_0603_25V7K
PR360 47K_0402_5%
PC251 0.1U_0402_16V7K
PR361 150K_0402_1%
PR362 100K_0402_1%
PQ58 PDTC115EU_SOT323
PQ59 2N7002W-T/R7_SOT323-3
PQ60 PDTC115EU_SOT323
PQ61 2N7002W-T/R7_SOT323-3
PC253 0.1U_0603_25V7K
PQ62 AO4466_SO8
PR363 20_0402_5%
PC254 0.047U_0402_16V7K
PR364 20_0402_5%
PC255 6800P_0402_25V7K
PC257 0.1U_0603_25V7K
PR365 20_0402_5%
PR367 2_0402_5%
PQ63 2N7002W-T/R7_SOT323-3
PR366 10K_0402_1%
PR368 100_0402_1%
PC256 0.01U_0402_25V7K
PC258 @100P_0402_50V8J
PC259 0.1U_0402_16V7K
PR369 0.02_1206_1%
PL29 10UH_PCMB104T-100MS_6A_20%
PR370 4.7_1206_5%
PQ64 AO4466_SO8
PC260 0.1U_0603_25V7K
PR371 22K_0402_5%
PR372 80.6K_0402_1%
PR373 0_0603_5%
PD13 RB751V-40_SOD323-2
PC262 680P_0402_50V7K
PC263 10U_1206_25V6M
PC264 10U_1206_25V6M
PQ65 PDTC115EU_SOT323
PR374 100K_0402_1%
PC261 0.01U_0402_25V7K
PR375 12.1K_0402_1%
PR376 4.7_0603_5%
PC265 4.7U_0603_6.3V6K
PR377 255K_0402_1%
PR378 20K_0402_1%
PQ66 2N7002W-T/R7_SOT323-3
PU17 ISL6251AHAZ-T_QSOP24
PR379 15.4K_0402_1%
PR381 31.6K_0402_1%
PC266 0.01U_0402_25V7K
PR380 340K_0402_1%
PR382 499K_0402_1%
PR383 10K_0402_1%
PU13B LM358DT_SO8
PR384 105K_0402_1%
PC267 0.01U_0402_25V7K

<30> FSTCHG
FSTCHG <30>
SUSP# <30,35,41,43>
<30> 3S/4S#
<40> ACON
<36,40> PACIN
<30> IREF
<30,40> ACOFF
<30> ADP_I
<30> 65W/90W#
<30> CALIBRATE#
<30> BATT_OVP
VMB <40,41>
VS
<40,41> BATT+
TCR=50ppm / C

CSIN
CSIP
DCIN
FSTCHG
SUSP#
6251VDD
6251_EN
CSON
CSOP
LX_CHG
DH_CHG
BST_CHG
BST_CHGA
6251VDDP
DL_CHG
6251VREF
6251aclim
ACON
PACIN
ACOFF
CHG

wrong Value

VDD DCIN ACSET ACPRN EN CSON CELLS CSOP ICOMP CSIN VCOMP CSIP ICM PHASE VREF UGATE CHLIM BOOT ACLIM VDDP VADJ LGATE GND PGND

CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
IREF=0.7224*Icharge
Ki=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//((15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

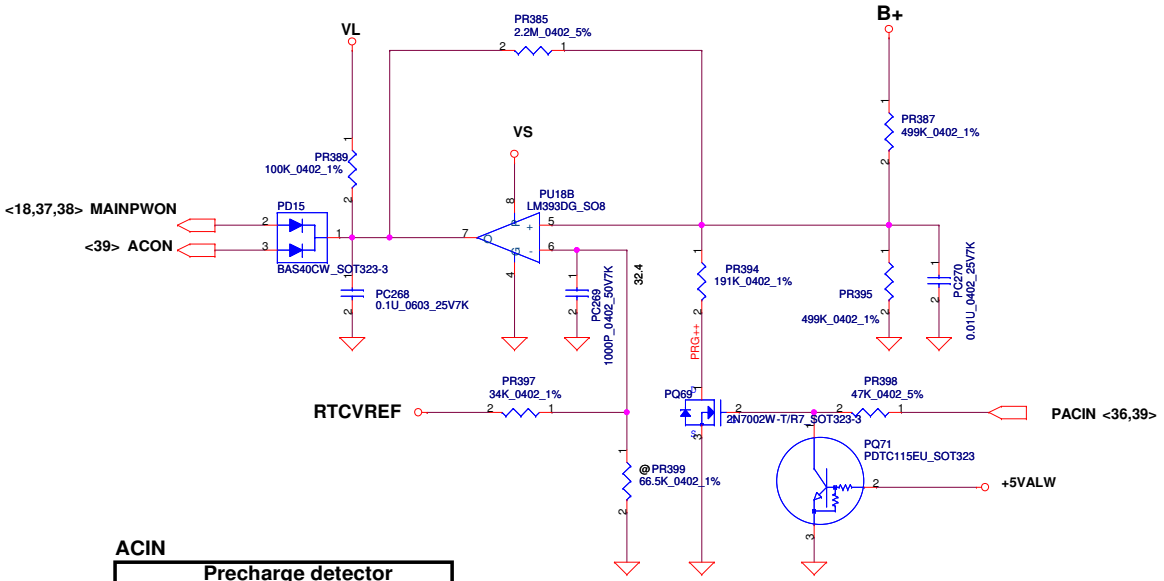
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

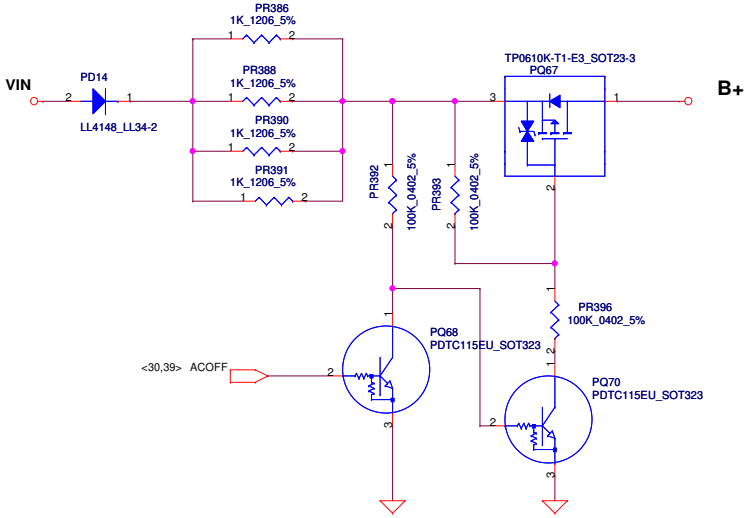
Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NALG0 | Rev: 1.0

Date: Thursday, January 21, 2010 | Sheet 39 of 49





ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

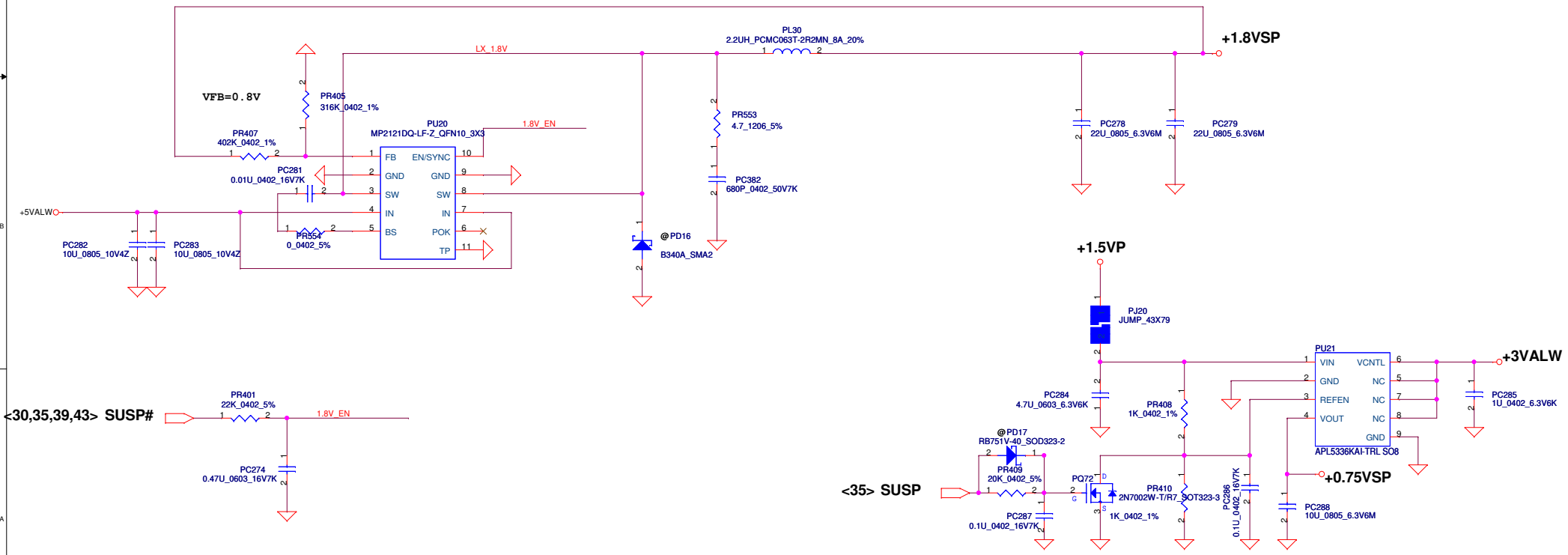
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **PRECHARGE**

Size	Document Number	Rev
Custom	NALG0	1.0

Date: Thursday, January 21, 2010 | Sheet 40 of 49



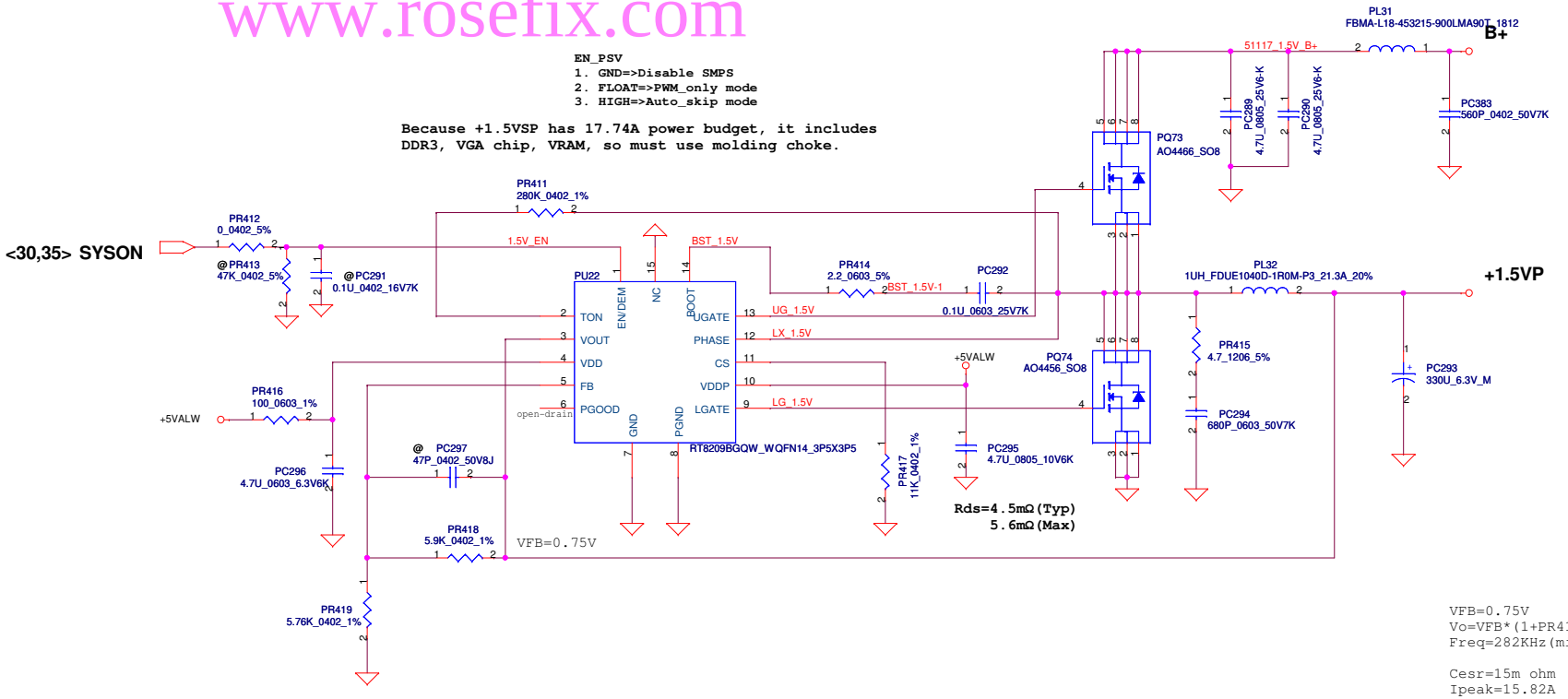
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NALG0	1.0

Date: Thursday, January 21, 2010 | Sheet 41 of 49



VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

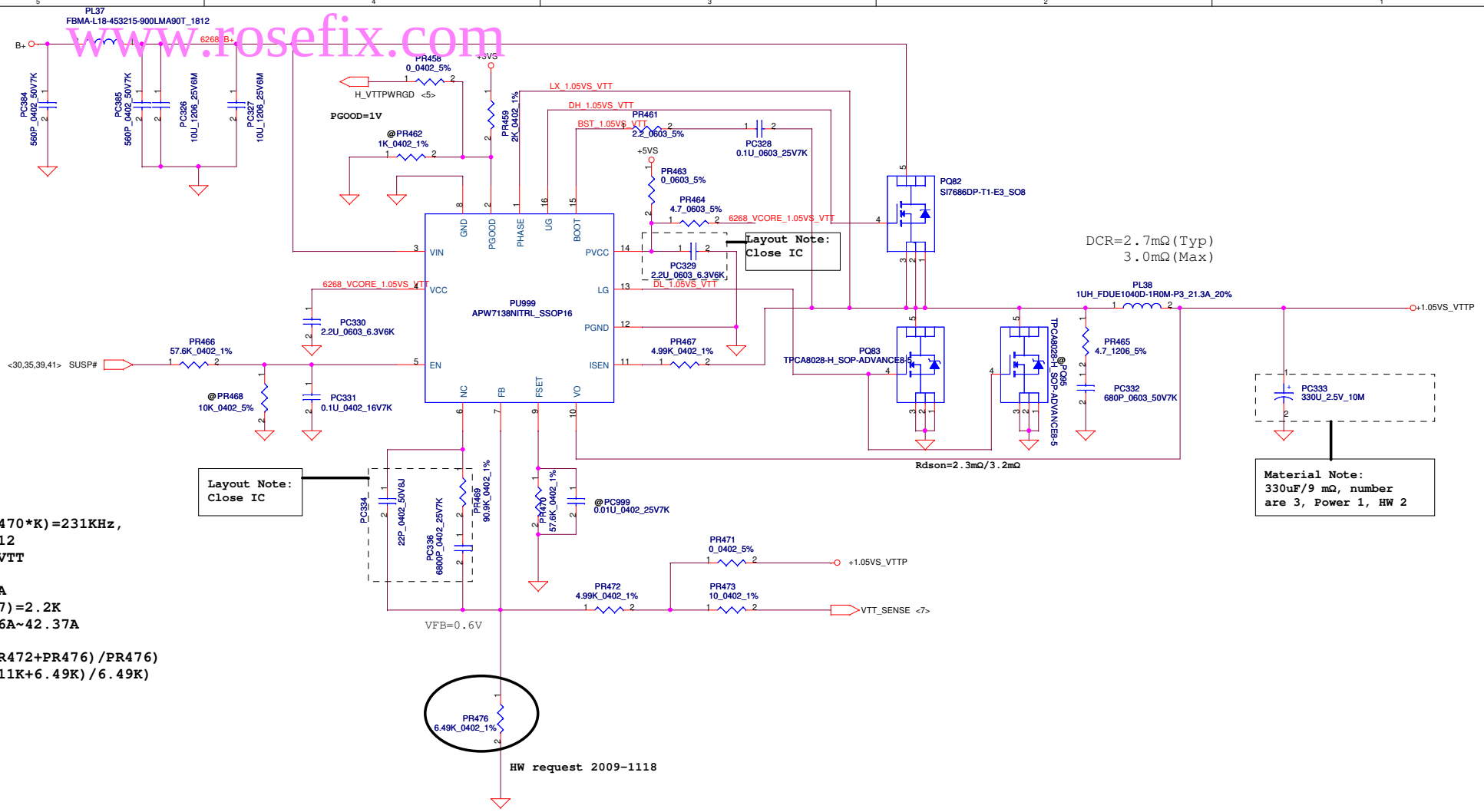
Cesr=15m ohm
Ipeak=15.82A
Iocpmin=18.98A
ΔI=((19-1.5)*(1.5/19))/(L*Freq)=4.899A
1/2ΔI=2.449A

Iocp=18.09A~29.13A

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title	1.5VP	
Size: Custom	Document Number: NALG0	Rev: 1.0
Date: Thursday, January 21, 2010	Sheet 42 of 49	



Fsw=1/(PR470*K)=231KHz,
K=75*10^-12
+1.05VSP_VTT
Ipeak=25A
Imax=17.5A
Rsen(PR467)=2.2K
Iocp=30.96A~42.37A

Vo=Vr*((PR472+PR476)/PR476)
=0.6*((5.11K+6.49K)/6.49K)
1.07V

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

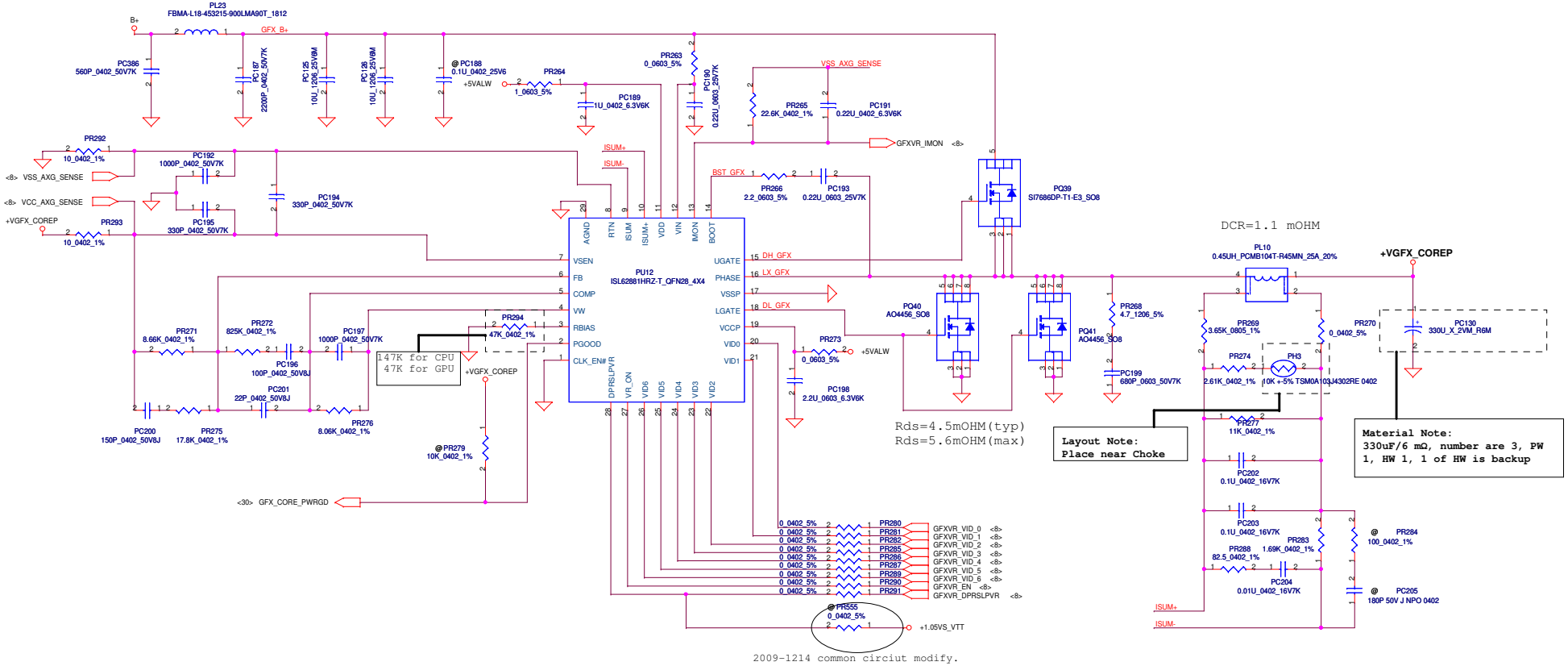
Compal Electronics, Inc.

Title: +1.1VS_VTTP

Size	Document Number	Rev
Custom	NALG0	1.0

Date: Thursday, January 21, 2010 | Sheet 43 of 49

Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

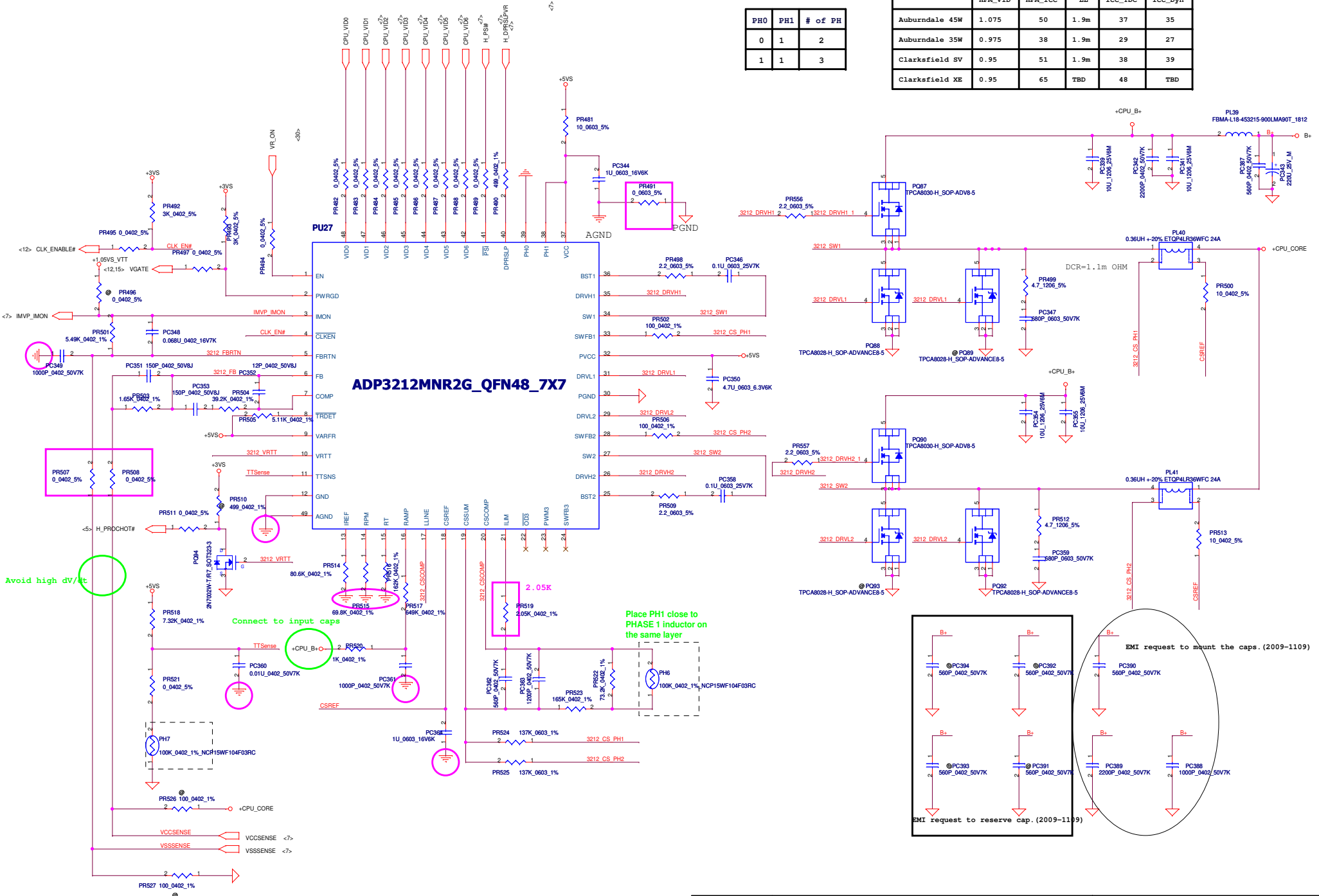
Title: GFX_COREP

Size	Document Number	Rev
C	NALG0	1.0

Date: Thursday, January 21, 2010 | Sheet 44 of 49

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.	
Title	CPU_CORE
Size C	Document Number NAV70 M/B LA-5892P Schematic
Rev	1.0
Date: Thursday, January 21, 2010	Sheet 45 of 49

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Arrandale CPU of UMA SKU only use 1 LS MOS	Arrandale CPU of UMA SKU only use 1 LS MOS	0.1	45	1 pop PQ87,PQ90, un-pop PQ86. 2 Delete PQ89, PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP ADVANCE 4 PC A false)	2009-1019	to DVT
2	BOM unique.	In order to BOM unique for 1SS355, re-link PD8.	0.1	38	Change PD8 from SC1SS355003 to SC100001K00	2009-1019	to DVT
3	CIS link error.	CIS link error.	0.1	45	Chnage PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1019	to DVT
4	BOM unique.	BOM unique.	0.1	39	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
5	BOM unique.	BOM unique.	0.1	41	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
6	BOM unique.	BOM unique.	0.1	45	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
7	BOM unique.	BOM unique.	0.1	38	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1019	to DVT
8	BOM unique.	BOM unique.	0.1	45	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1019	to DVT
9	BOM unique.	BOM unique.	0.1	43	Change PQ83 from SB00000I900(S TR AON6704L 1N DFN) to SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1019	to DVT
10	VTT Power rail commond design.	VTT Power rail commond design.	0.1	43	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)-X63826BOL11 Delete PQ95 SB00000I900(S TR AON6704L 1N DFN)-OTHERS	2009-1019	to DVT
11	Charger, EMI request.	EMI request to add a bead to replace Jump to PASS EMI test.	0.2	39	Add PL45 SM010018210(S SUPPRE_ TAI-TECH HCB4532KF-800T90 1812)	2009-1105	to DVT
12	+VSBP, EMI request.	EMI request to add PC221/PC222 to PASS EMI test	0.2	37	Add PC221 SE000005Z80 S CER CAP .22U 25V K X7R 0603 Add PC222 SE042104K80 S CER CAP .1U 25V K X7R 0603	2009-1105	to DVT
13	+1.8VSP, BOM error.	+1.8VSP EN delete wrong. Must add PR401 and PC274 for SUSP# enable.	0.2	41	Add PR401 SD028220280 S RES 1/16W 22K 0402 5% Add PC274 SE026474K80 S CER CAP 0.47U 16V K X7R 0603	2009-1105	to DVT
14	+1.5VP, EMI request.	EMI request add snubber for +1.5VP to PASS EMIU test.	0.2	42	Add PR415 SD001470B80 S RES 1/4W 4.7 +-5% 1206 Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603	2009-1105	to DVT
15	+1.5VP, EMI request.	EMI request add a small cap to reduce high Freq noise. EMI request change boost R to 2.2 ohm.	0.2	42	Add PC383 SE074561K80 S CER CAP 560P 50V K X7R 0402 Change PR414 from SD013000080 to SD013220B80	2009-1105	to DVT
16	+1.05VS_VTTP EMI request.	EMI request add two small cap to reduce high Freq noise.	0.2	43	Add PC384 SE074561K80 S CER CAP 560P 50V K X7R 0402 Add PC385 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
17	+1.05VS_VTTP EMI request.	EMI request add snubber for +1.05VS_VTTP to PASS EMIU test.	0.2	43	Add PR465 SD001470B80 S RES 1/4W 4.7 +-5% 1206 Add PC332 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
18	+1.05VS_VTTP EMI request.	EMI request change boost R to 2.2 ohm.	0.2	43	Change PR461 from SD013000080 to SD013220B80	2009-1105	to DVT
19	+1.05VS_VTTP, HW request.	HW request to increase +1.05VS_VTTP voltage.	0.2	43	Change PR472 from SD034499180 to SD034649180.	2009-1105	to DVT
20	+GFX_COREP, EMI request.	EMI request add a small cap to reduce high Freq noise.	0.2	44	Add PC386 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
21	+GFX_COREP, EMI request.	EMI request add snubber for +1.05VS_VTTP to PASS EMIU test.	0.2	44	Add PR268 SD001470B80 S RES 1/4W 4.7 +-5% 1206 Add PC199 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
22	+GFX_COREP, EMI request.	EMI request change boost R to 2.2 ohm.	0.2	44	Change PR266 from SD013000080 to SD013220B80	2009-1105	to DVT

Compal Electronics, Inc.			
Title: PIR (PWR)			
Size: Custom	Document Number		Rev: 1.0
Date: Thursday, January 21, 2010		Sheet 46 of 49	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	+CPU_COREP, EMI request.	EMI request add a small cap to reduce high Freq noise.	0.2	45	Add PC387 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
25	+CPU_COREP, EMI request.	EMI request change boost R to 2.2 ohm.	0.2	45	Change PR498/PR509 from SD013000080 to SD013220B80	2009-1105	to DVT
26	+CPU_COREP, EMI request.	EMI request add snubber for +CPU_COREP to PASS EMIU test.	0.2	45	Add PR499/PR512 SD001470B80 S RES 1/4W 4.7 +-5% 1206 Add PC347/PC359 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
27	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PL40/PL41 from SH000005680 to SH0000012036BM00.	2009-1105	to DVT
28	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PR524/PR525 from SD013120380 to SD013137380.	2009-1105	to DVT
29	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PC362 from SE074391K80 S CER CAP 390P 50V K X7R 0402 to SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
30	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PR501 from SD034536180 S RES 5.36K 0402 1% to SD034549180 S RES 1/16W 5.49K 0402 1%	2009-1105	to DVT
31	+CPU_COREP, EMI request.	+CPU_COREP, EMI request.	0.3	45	Add PC388 SE074102K80 S CER CAP 1000P 50V K X7R 0402	2009-1113	to DVT
32	+CPU_COREP, EMI request.	+CPU_COREP, EMI request.	0.3	45	Add PC389 SE074222K80 S CER CAP 2200P 50V K X7R 0402 Add PC390 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1113	to DVT
33	+CPU_COREP, cost issue.	Becuase SF000000G80 will cost uo, change to SF22004M210.'	0.3	45	Change PC343 from SF000000G80 to SF22004M210.	2009-1113	to DVT
34	+CPU_COREP, IMON issue.	Because Intel update IMON RC time constant, update PC348 to 0.068u to meet spec.	0.3	45	Change PC348 from SE076103K80 S CER CAP .01U 16V K X7R 0402 to SE000003J80 S CER CAP 0.068U 16V K X7R 0402	2009-1113	to DVT
35	+3V/+5V cost issue.	Because Nippon cost up thier OS-CON cap, so we change Nippon cap to Sanyo cap by sourcer request.	0.4	38	Change PC233/PC237 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SF22001M200 S ELE CAP 220U 6.3V M B C6 SVPC ESR15	2009-1118	to DVT
36	+1.05VS_VTTP issue.	HW request to increase +1.05VS_VTTP voltage.	0.4	43	Change PR472 from SD034649180 to SD034511180.	2009-1118	to DVT
37	+1.05VS_VTTP issue.	HW request to increase +1.05VS_VTTP voltage.	0.4	43	Chnage PR476 from SD034665180 to SD034649180.	2009-1118	to DVT
38	+0.75VSP power sequence issue.	HW request to adjust power sequence.	0.4	47	change PR409 from SD028000080 S RES 0 0402 5% to SD028200280 S RES 1/16W 20K 0402 5%.	2009-1118	to DVT
39	+1.05VS_VTTP issue.	+1.05VS_VTTP choke unique to +1.5VP.	0.4	43	Change PL38 from SH000008V80 S COIL 1UH +-20% PCMB103E-1R0MS 20A to SH000009U00 S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A	2009-1118	to DVT
40	+1.05VS_VTTP 2nd source issue.	In order to phase in 2nd source, change ISL6268 to APW7138.	0.5	43	Change PU26 from SA00001HT80 S IC ISL6268CAZ-T SSOP 16P to PU999 SA00002O600 S IC APW7138NITRL SSOP 16P	2009-1208	to PVT
41	+1.05VS_VTTP 2nd source issue.	APW7138 needn't pop PC335.	0.5	43	Delete PC335 SE075103K80 S CER CAP .01U 25V K X7R 0402 and change location to PC999.	2009-1208	to PVT
42	HDD LED flash issue.	HDD LED will flash when plug in adapter, because +3VS rise a little. HW request add PC224 to solve it.	0.5	37	Add PC224 SE000000K80 S CER CAP 1U 6.3V X5R 0402	2009-1208	to PVT
43	HDD LED flash issue.	If add PC224, must change PR330 from 0 to 1K to avoid SPOK pin fail. that is add a current limit R on SPOK pin.	0.5	37	Chnage PR330 from SD028000080 to SD028100180.	2009-1208	to PVT
44	BOM error.	+1.8VSP choke use wrong material. Unique MP2121 to other project.	0.5	41	Change PL30 from SH000006I80 S COIL 2.2UH +-20% PCMC063T -2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A Add PR554 SD028000080 0 0402 5%	2009-1208	to PVT
45	+1.05VS_VTTP issue.	HW request to adjust +1.05VS_VTTP Vout.	0.5	43	Change PR472 from SD034511180 to SD034499180.	2009-1208	to PVT
46	+VGFX_COREP issue	ISL62881 common circiut update.	0.5	44	Delete PR291 SD028000080. Add PR555 SD028000080.	2009-1208	to PVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Sequense issue.	Modify sequense by HW request.	0.6	37	Chnage PR330 from SD028100180 S RES 1/16W 1K +-5% 0402 to SD028000080 S RES 1/16W 0 +-5% 0402.	2010-0112	to Pre-MP
25	Sequense issue.	Modify sequense by HW request.	0.6	37	Delete PC224 SE000000K80 S CER CAP 1U 6.3V K X5R 0402	2010-0112	to Pre-MP
26	EMI issue.	Because EMI has power BB on 250MHz, add HS gate R to solve.	0.6	45	Add PR556/PR557 SD013220B80 S RES 1/10W 2.2 +-5% 0603	2010-0112	to Pre-MP
27	BOM loss update in DVT.	BOM loss update in DVT, change 1.8V choke.	0.6	41	Change PL30 from SH000006180 S COIL 2.2UH +-20% PCMC063T-2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A	2010-0112	to Pre-MP
28	Common circiut update.	GFX_COREP common circiut update.	0.6	44	Add PR291 SD028000080 0 0402 5% Delete PR555 SD028000080 0 0402 5%	2010-0112	to Pre-MP
29	Changer choke issue.	Because Cyntec has qulity issue and can't use in MFG, in order to prevent shortage issue, change to Maglayer.	0.6	39	Chnage PL29 from SH000005Z80 S COIL 10UH +-20% PCMB104T-100MS 6A to SH000009R00 S COIL 10UH +-20% MMD-10DZ-100M-X1 6A	2010-0112	to Pre-MP
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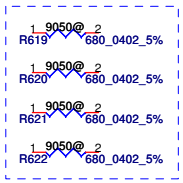
Version change list (P.I.R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1			09 / 30	Q9 / Q15 / Q65 / Q14 / Q36 / Q19 / Q31 / Q56 / Q57 Change to SB00000AR10 Q4/Q5/Q6/Q7/Q13/Q24/Q25/Q59/Q61/Q62/Q63/Q20 Change to SB570020120	
2	DVT		11 / 03	Modify WWAN Mini catd PIN define. X1 / X2 Change to SJ132P7KW10 Add PCH_SUSCLK net for remove EC crystal. Remove C147 Add F2 for RF team.	
			11 / 05	Add C670 / C671 / C672 / C673 For INTEL Change C217 to 22U and add C221 22U for CRT issue. Add P80DATA PD 100Kohm(R51) for EC common design.	
			11 / 09	Add C40 / C41 / C42 / C43 / C44 for EMI.	
			11 / 10	Add ACIN#(Q16) for ACIN LED(NEW60) Add C45 / C46 / C47 / C48 for LAN Common mode noise Remove net BT_LED#.	
			11 / 11	Add R14 for MINI1 LED Function.	
			11 / 16	Add D13/D14/D16/D23/D24/D25/D26/D30 for ESD Add R836/C760 R338/C555 for RF. L21 Change to SM010012010 L5 Change to SM01000AX00 Change R619/R621 to 680ohm Change R620/R622 to 3.9kohm	
			11 / 16	Y1 Change to SJ100009R00	
			11 / 17	R841 Change to 8.2k ohm Update Power SCH Change T1 to SP050006B00	
			11 / 18	Change PCH P/N to SA00003N7B0 Change R167 to 470 ohm.	
			11 / 19	Update Power SCH	
3	PVT		12 / 07	C259 / C279 / C692 / C693 Change to SE107475K80 0603 type	
			12 / 09	Reserved R15 (net LOCAL_DIM) / R16 (net COLOR_ENG_EN) for LVDS function. Reserved R307 for +LCDVDD. EC Pin36 for WLAN_LED# (output), Pin 17 for MINI1_LED# (input) EC Pin91 for 3G_LED#(output) & Pin85 for WWAN_LED# (input)	
			12 / 10	Update Power SCH	
			12 / 11	Update Power SCH Add R96 PD 100K for LVDS Panel issue. Add C674 / C675 / C676 For EMI. Del SW3 Power on SW	
			12 / 14	Update Power SCH	
			12 / 16	U8 change to SA00000U500	
			12 / 17	R619 / R621 change to 2.2K SD028220180 for LED Q13 / R477 Change to unpop R171 Change to pop,R172 change to unpop for Board ID. Add R777 / R778 For HDMI Issue.Only pop R778. R751 Change to 2.2K.	
4	PRE MP			ADD PU R951 / R953 UNPOP D23 for MIC noise issue. UNPOP R827 / R828, ADD L7 SM070001600 for USB.	
			01 / 06	Update Power SCH	
			01 / 11	Change Q9,Q65,Q15,Q14,Q36,Q19,Q31,Q56,Q57 to SB00000DH00 Change LED1 / LED3 to SC591NB5A30 Del L7, Add R827 / R828. Del D26 / D25	
			01 / 21	Update Power SCH	

For NEW50 / NEW90 LED



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