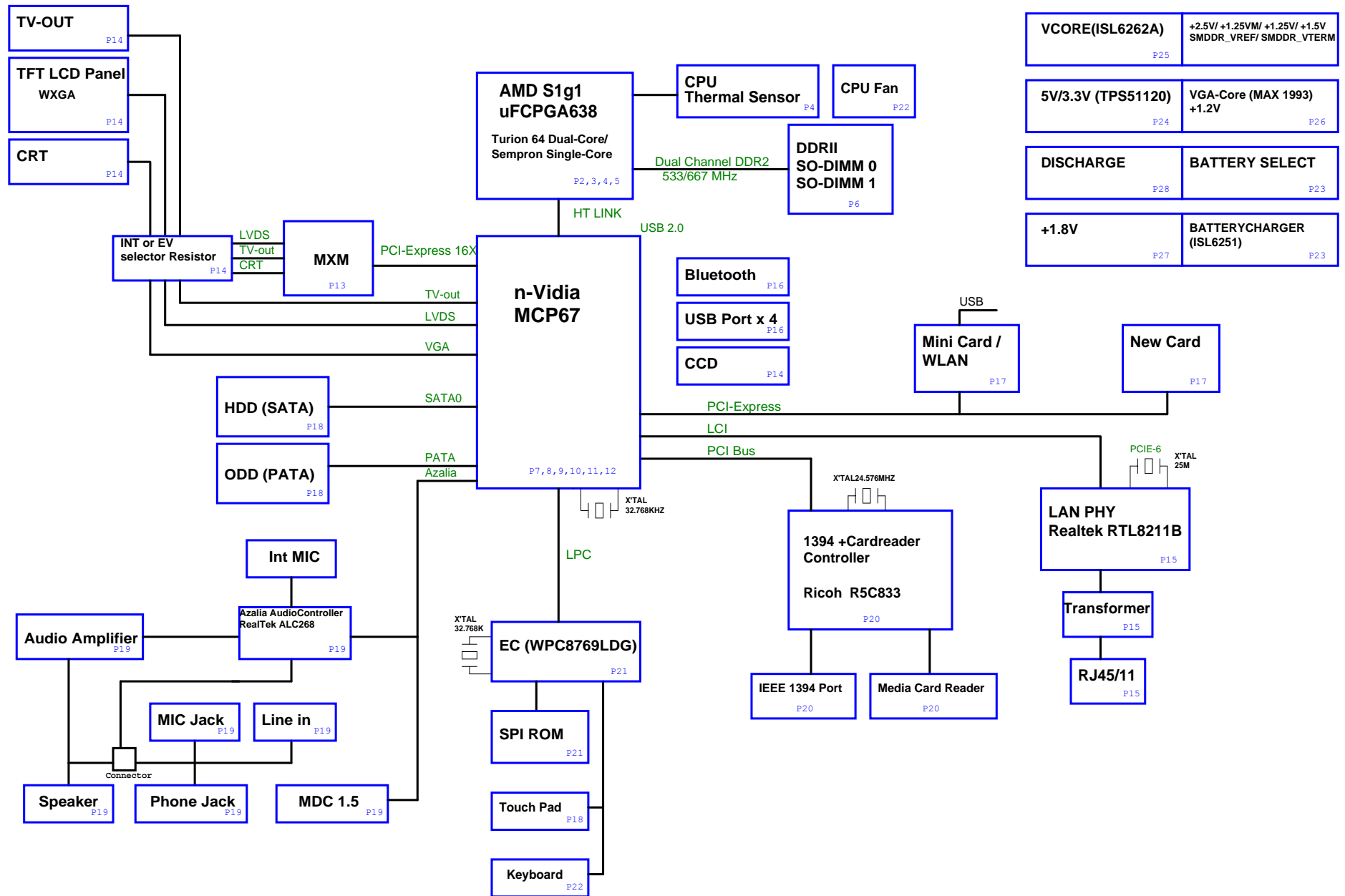
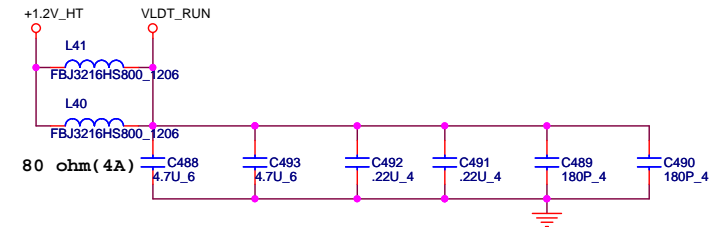
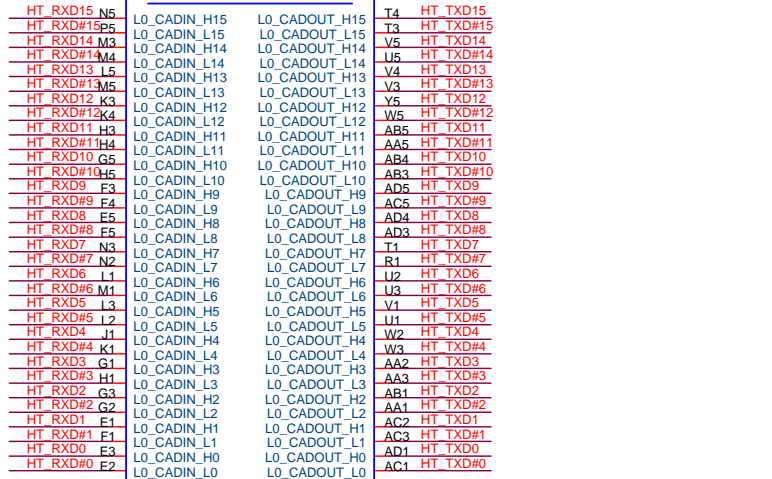
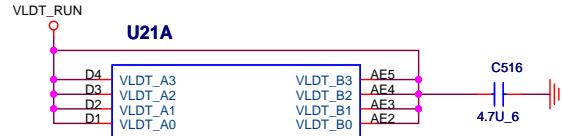


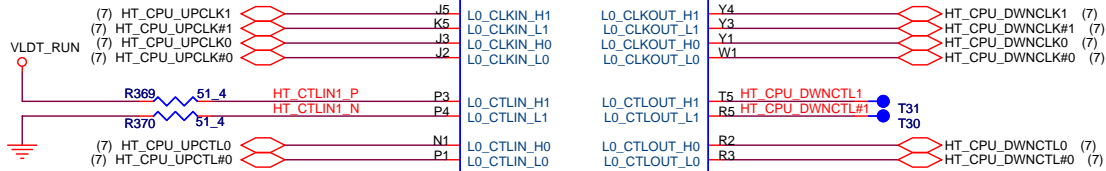
ZO3 SYSTEM BLOCK DIAGRAM





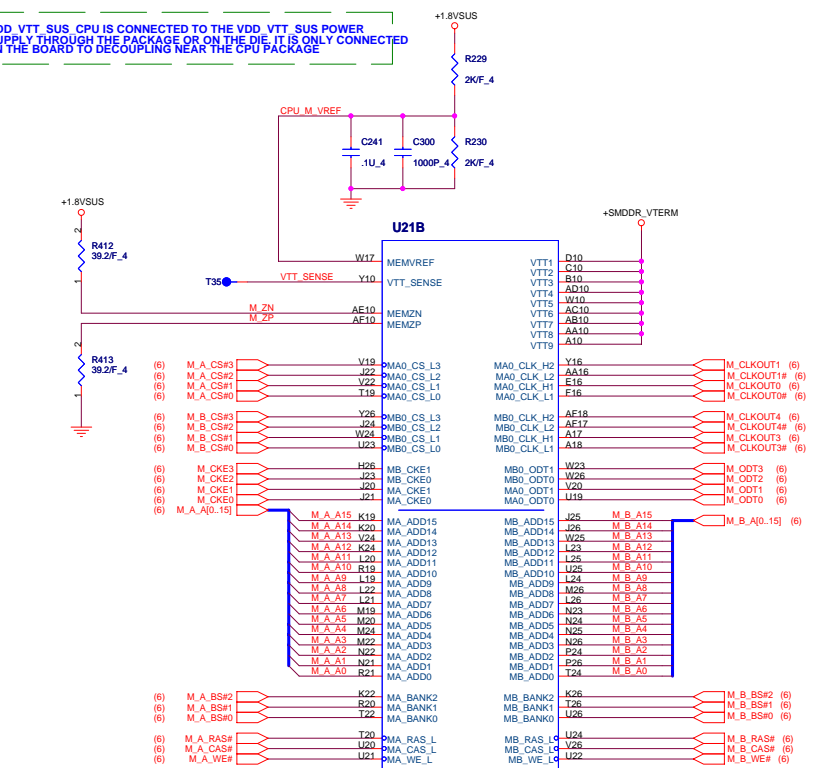
LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDT0 POWER PINS

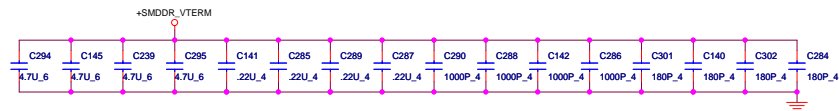
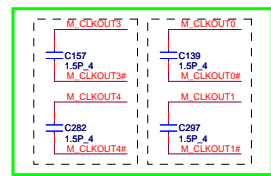


Athlon 64 S1
 Processor Socket

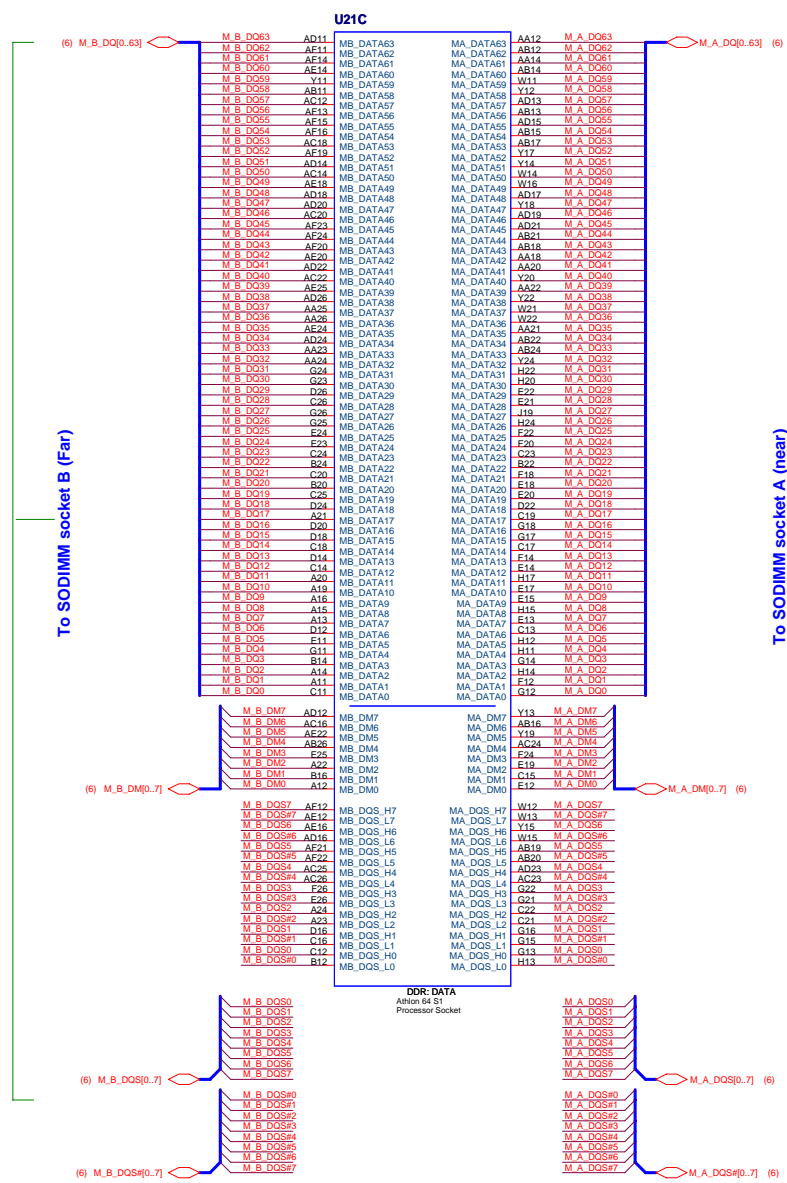
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Near CPU L<1200mil



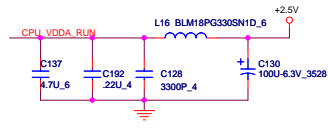
Processor DDR2 Memory Interface



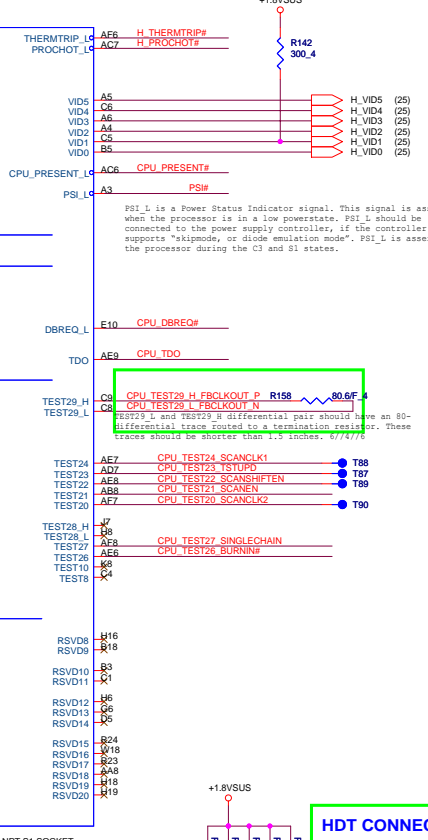
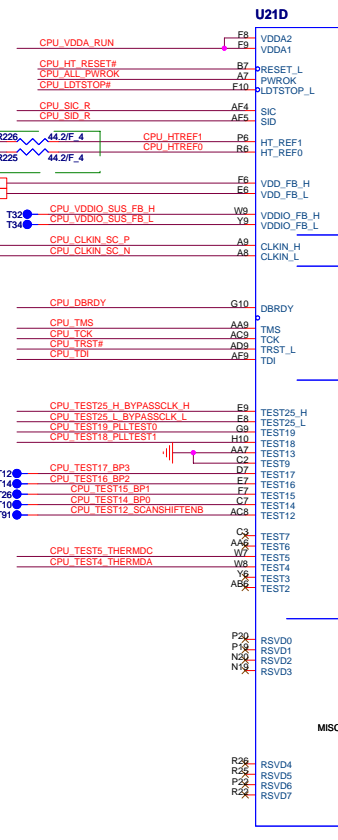
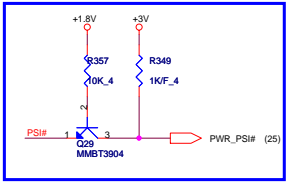
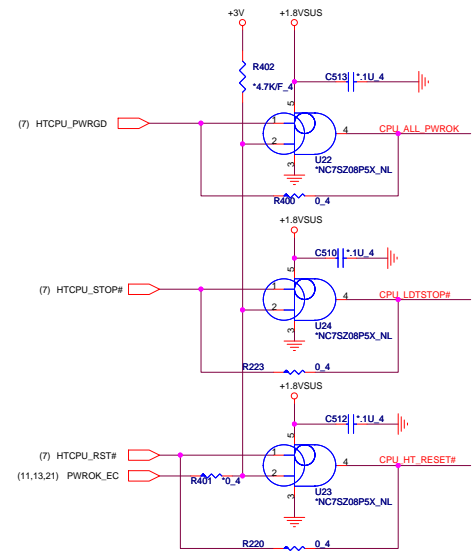
ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

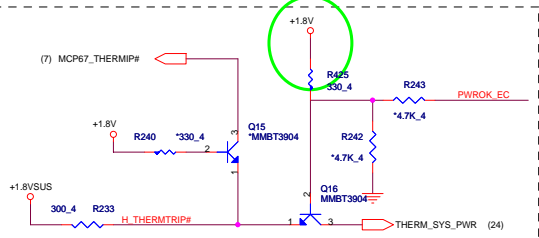
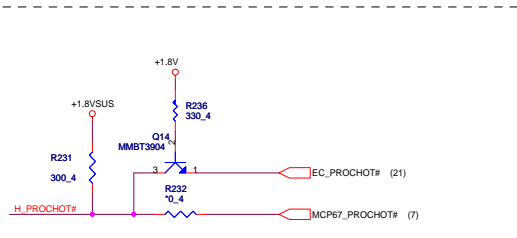


If AMD SI is not used, the SID pin can be left unconnected and S_{IC} should have a 300-Ω (±5%) pulldown to VSS.

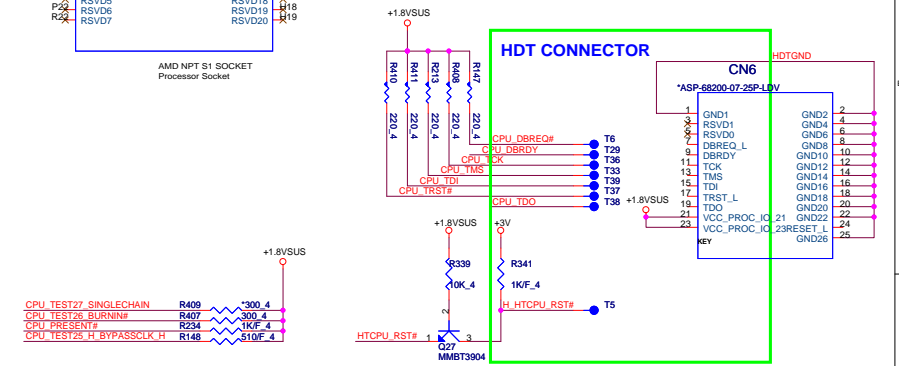
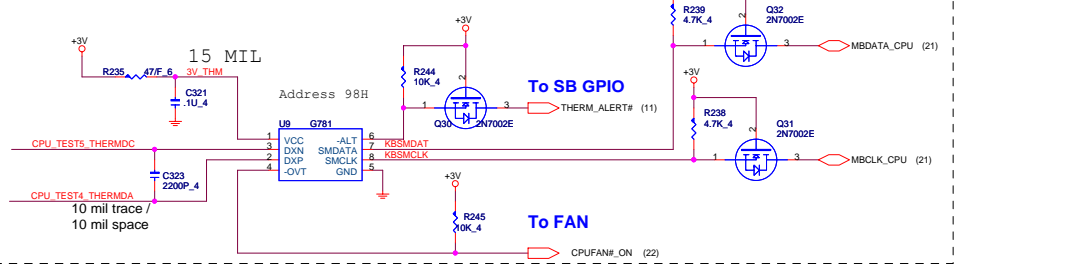


PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low power state. PSI_L should be connected to the power supply controller, if the controller supports "skippable" or "diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

TEST29_L and TEST29_H differential pair should have an 80-ohm differential trace routed to a termination resistor. These traces should be shorter than 1.5-inches. 6/15/11

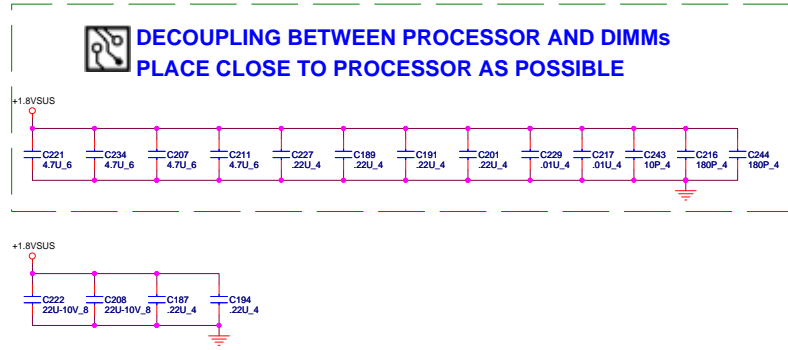
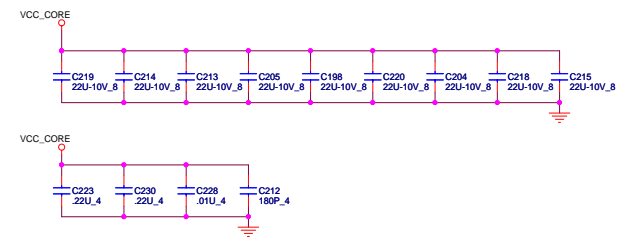
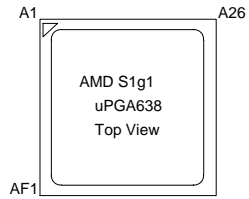
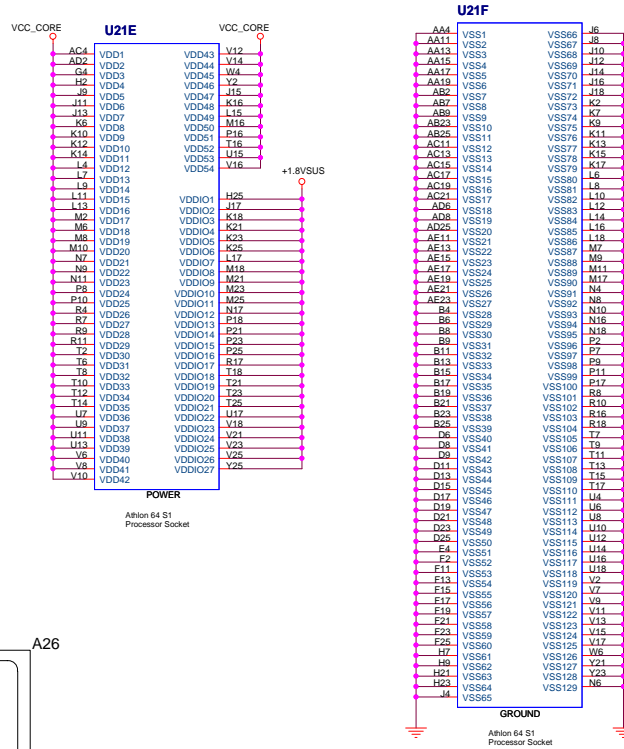


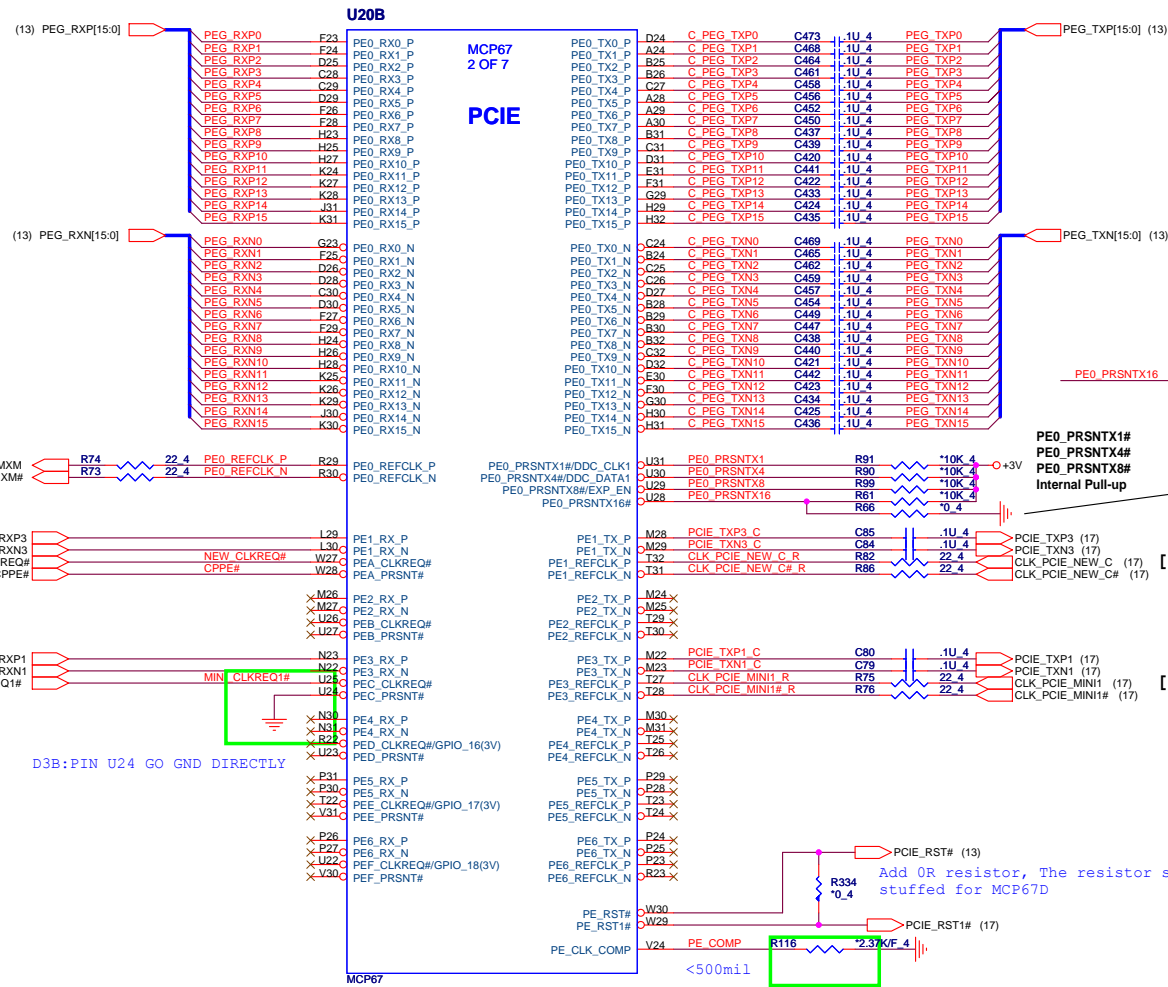
CPU H/W MONITOR



- CPU_TEST21_SCANEN R405 ~300_4
- CPU_TEST25_L_BYPASSCLK_L R187 ~300_4
- CPU_TEST19_PLITEST0 R185 ~300_4
- CPU_TEST18_PLITEST1 R187 ~300_4
- CPU_TEST27_SINGLECHAIN R408 ~300_4
- CPU_TEST26_BURNIN R407 ~300_4
- CPU_PRESENT# R234 ~1Kf_4
- CPU_TEST25_H_BYPASSCLK_H R148 ~310f_4

PROCESSOR POWER AND GROUND





[MXM]

[NEW CARD]

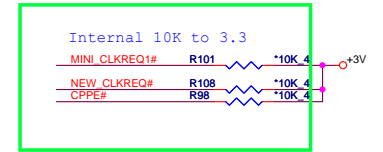
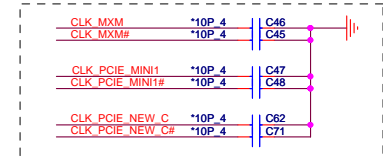
[TV]

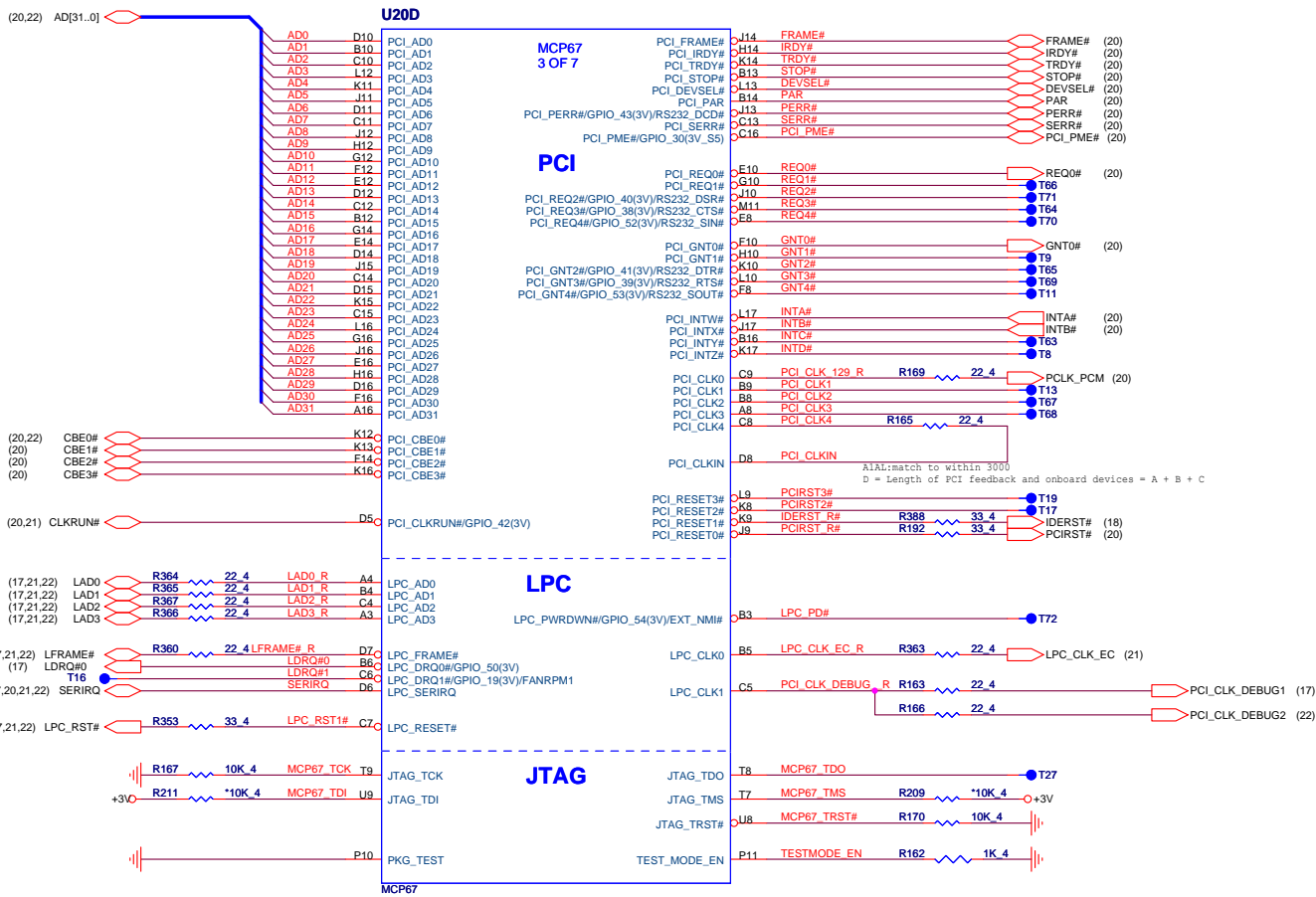
[MINI CARD]

[NEW CARD]

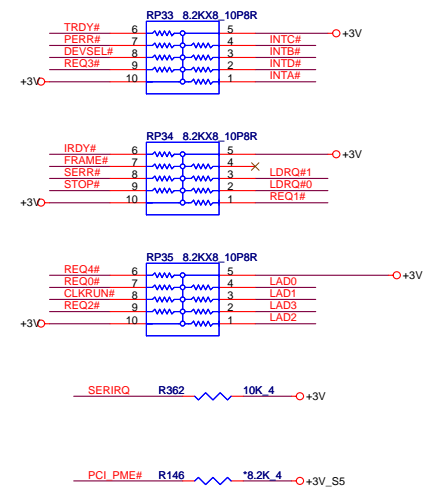
[MINI CARD]

NET NAME	MCP67D (DISCRETE)	MCP67M (GPU)
PE0_PRSNTX16	LOW	N/A

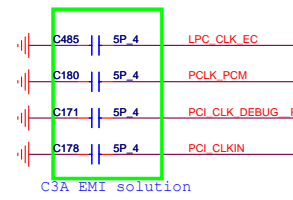


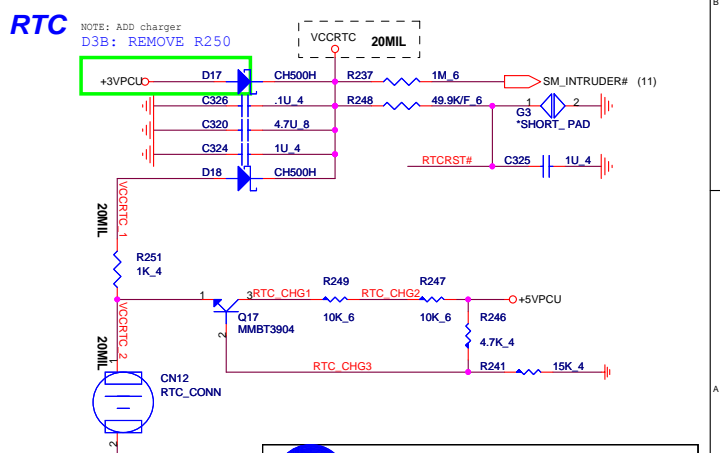
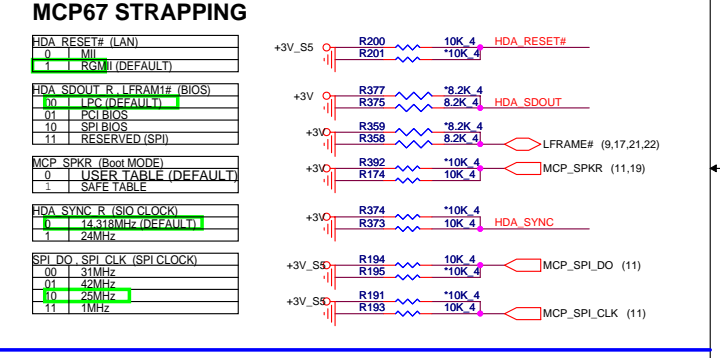
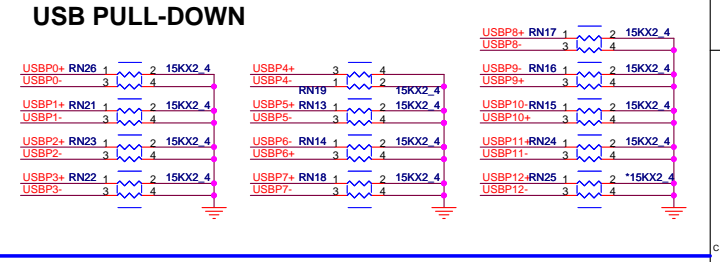
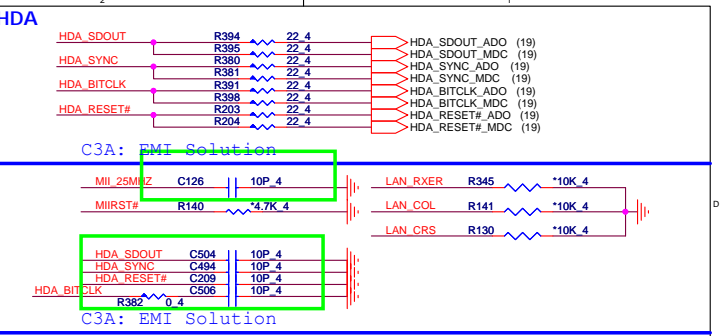
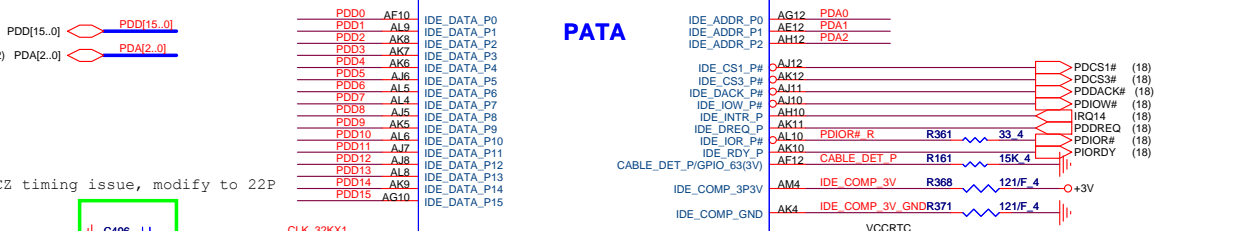
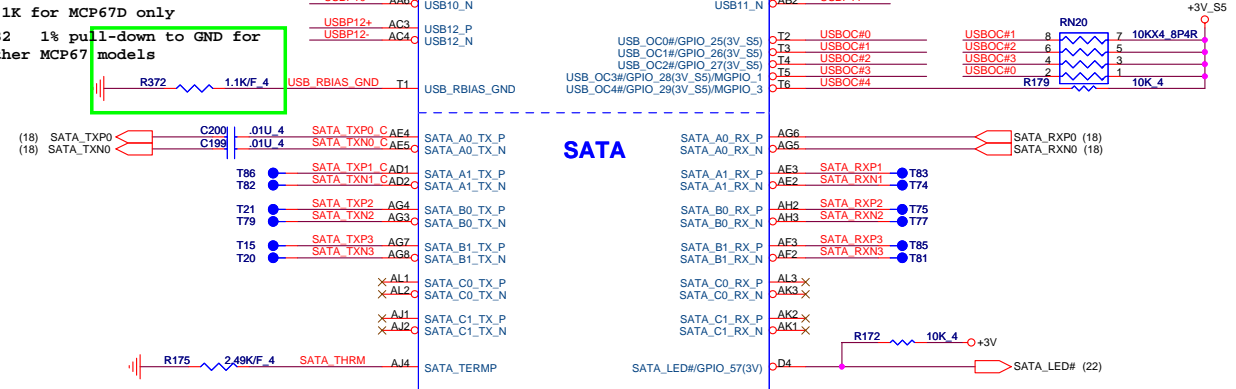
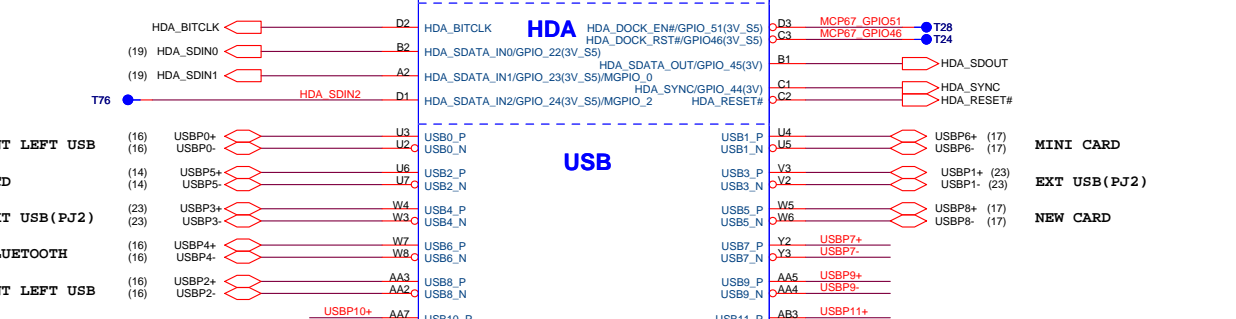
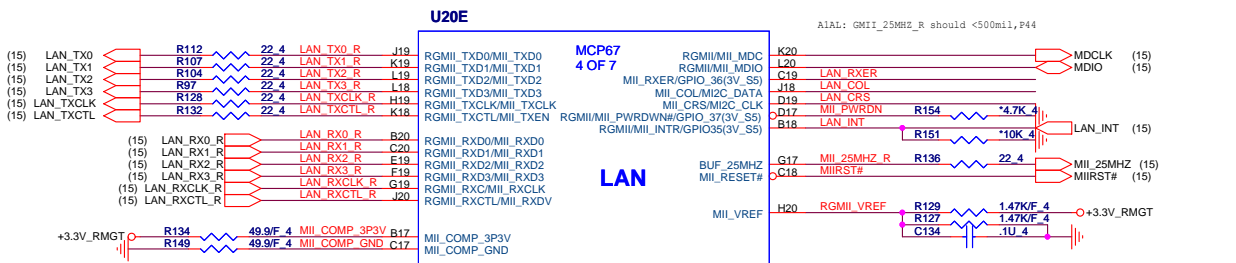


PCI/LPC PULL-UP



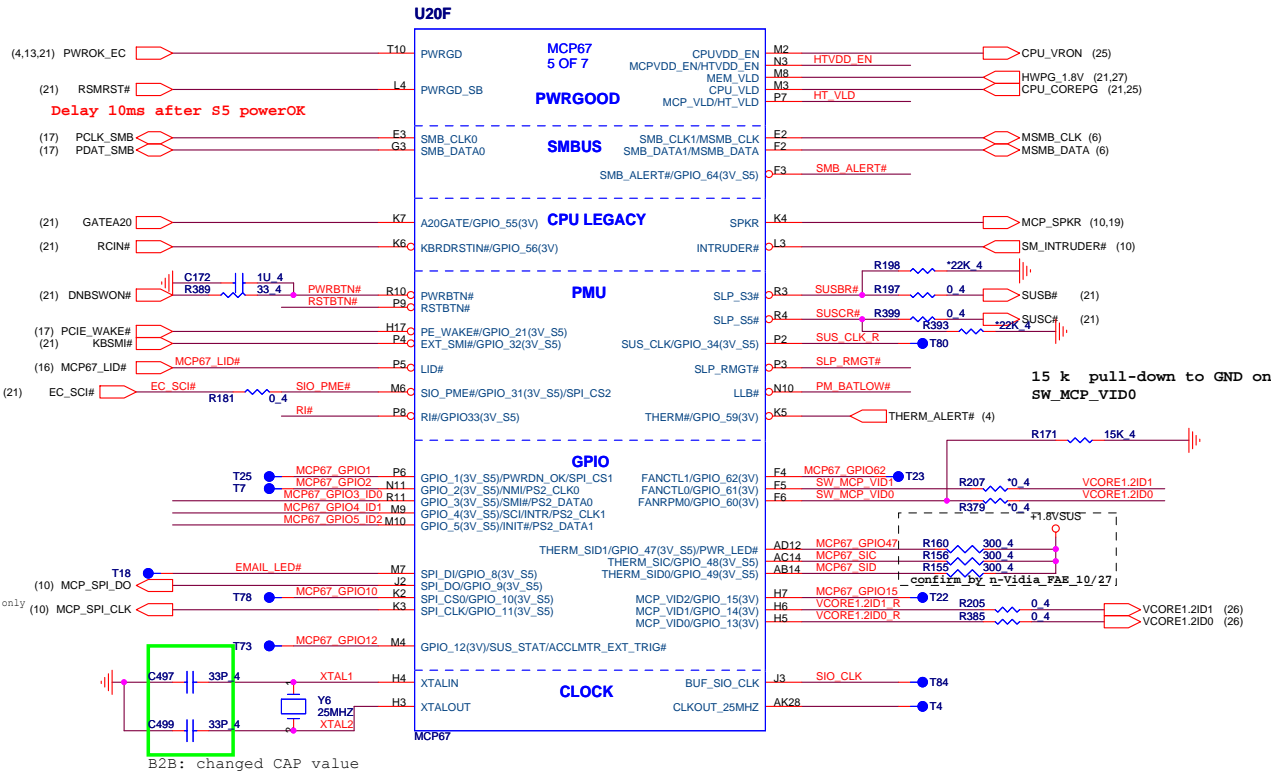
CLOCK BYPASS



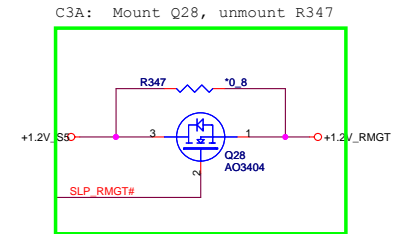


PROJECT : Z03
Quanta Computer Inc.

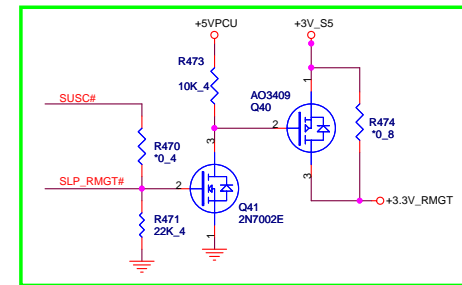
Size	Document Number	Rev
	MCP67(LAN/HDA/USB/HDD/RTC)	1A
Date:	Wednesday, April 25, 2007	Sheet 10 of 30



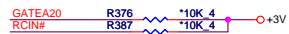
FOR SLEEP MODE CORE POWER CIRCUIT



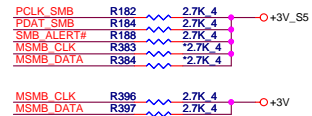
C3A: Mount Q40, Q41, R473, R471, unmount RR74



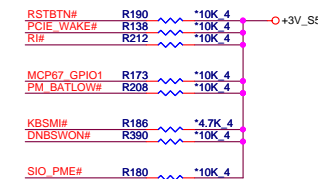
CPU LEGACY PULL-UP



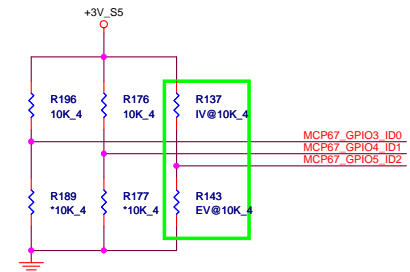
SMB/I2C PULL-UP



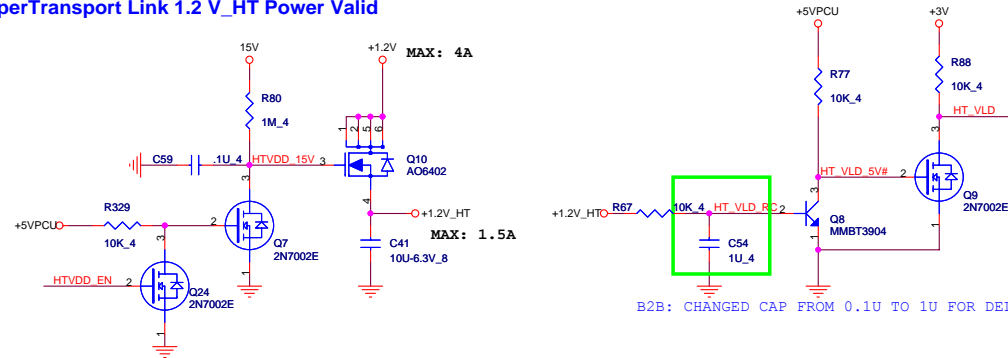
PMU PULL-UP



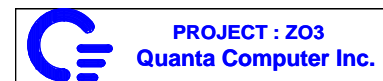
M/B ID for 14"/15"/17"



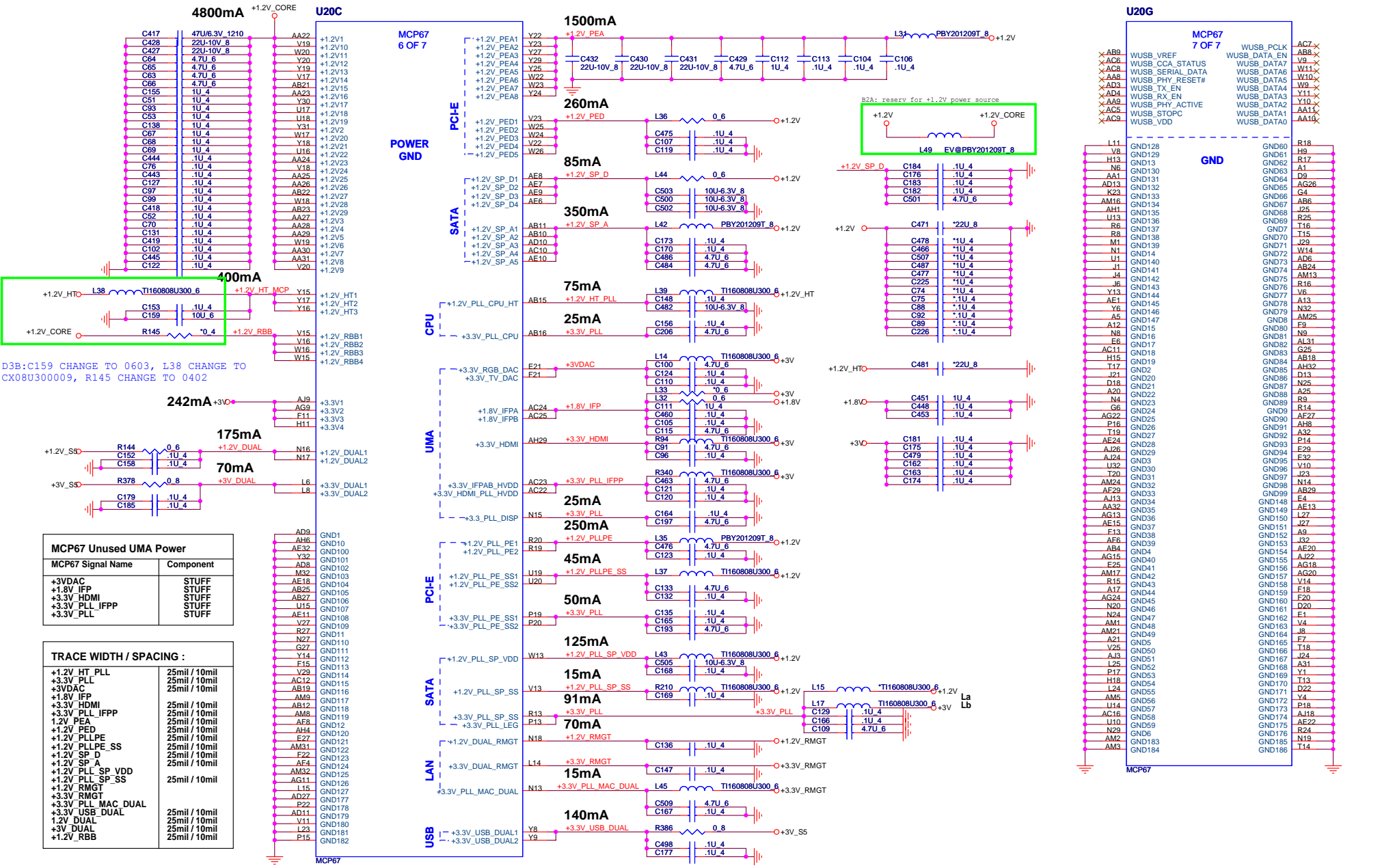
HyperTransport Link 1.2 V_HT Power Valid



ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	X
1	1	0	14" D
1	1	1	14" U



MCP67 POWER PLANE/GND & BYPASS

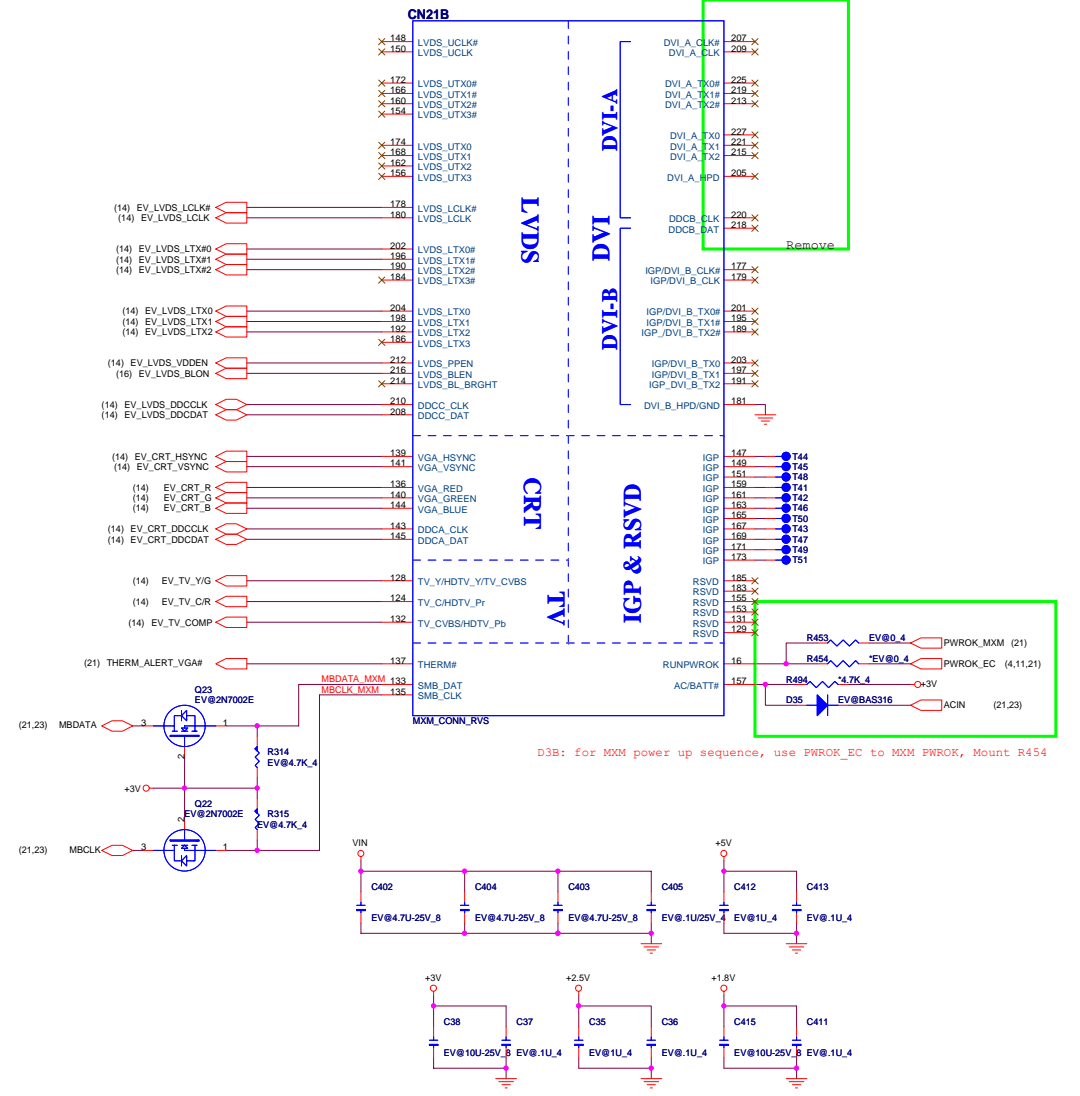
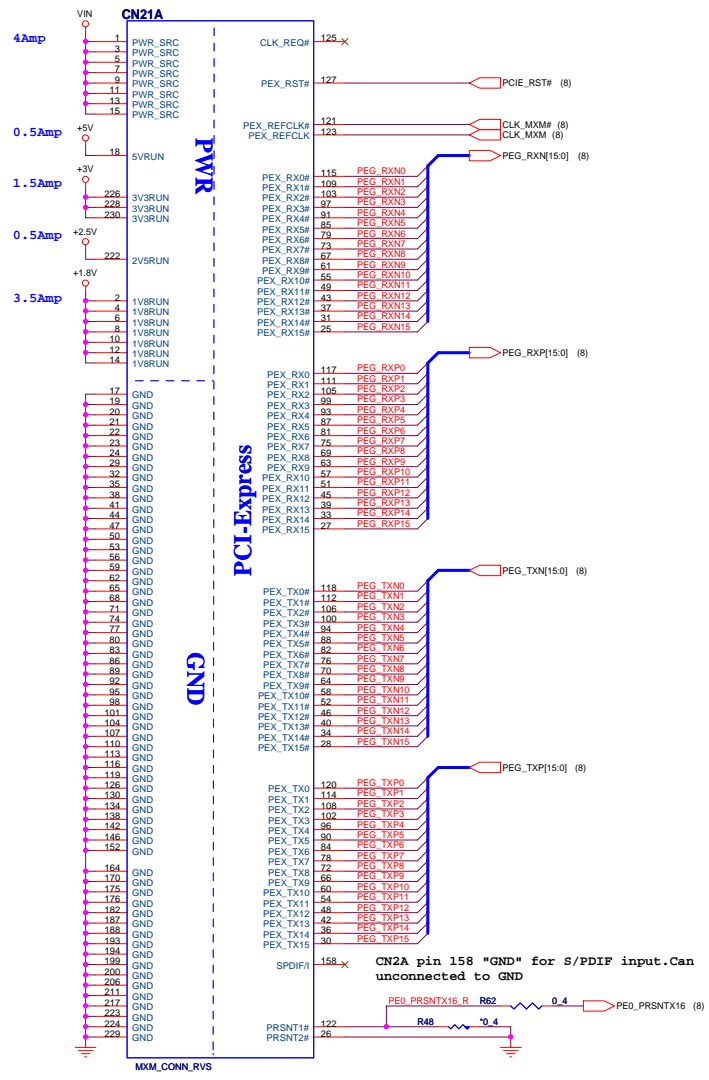


D3B:C159 CHANGE TO 0603, L38 CHANGE TO CX080300009, R145 CHANGE TO 0402

MCP67 Unused UMA Power	
MCP67 Signal Name	Component
+3VDAC	STUFF
+1.8V_IFFP	STUFF
+3.3V_HDMI	STUFF
+3.3V_PLL_IFPP	STUFF
+3.3V_PLL	STUFF

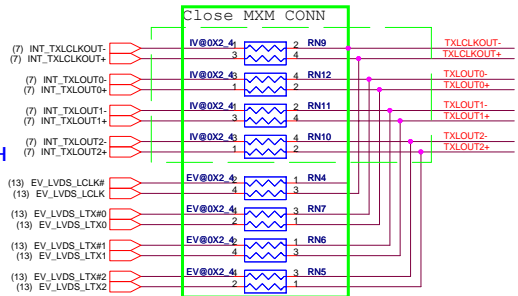
TRACE WIDTH / SPACING :	
+1.2V_HT_PLL	25mil / 10mil
+3.3V_PLL	25mil / 10mil
+3VDAC	25mil / 10mil
+1.8V_IFFP	25mil / 10mil
+3.3V_HDMI	25mil / 10mil
+3.3V_PLL_IFPP	25mil / 10mil
1.2V_PEA	25mil / 10mil
+1.2V_PED	25mil / 10mil
+1.2V_PLLPE	25mil / 10mil
+1.2V_PLLPE_SS	25mil / 10mil
+1.2V_SP_D	25mil / 10mil
+1.2V_SP_A	25mil / 10mil
+1.2V_PLL_SP_VDD	25mil / 10mil
+1.2V_PLL_SP_SS	25mil / 10mil
+3.3V_RMGT	25mil / 10mil
+3.3V_PLL_MAC_DUAL	25mil / 10mil
+3.3V_USB_DUAL	25mil / 10mil
1.2V_DUAL	25mil / 10mil
+3V_DUAL	25mil / 10mil
+1.2V_RBB	25mil / 10mil

PROJECT : Z03
Quanta Computer Inc.

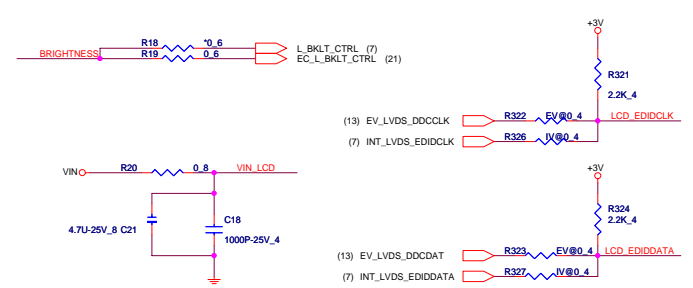
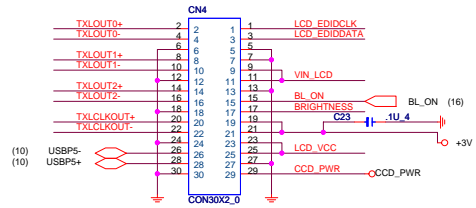


LVDS

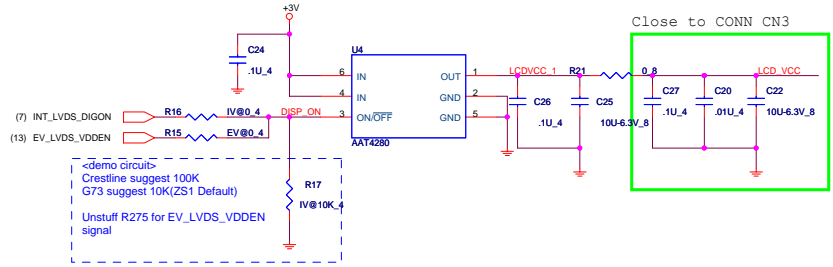
SINGLE_CH



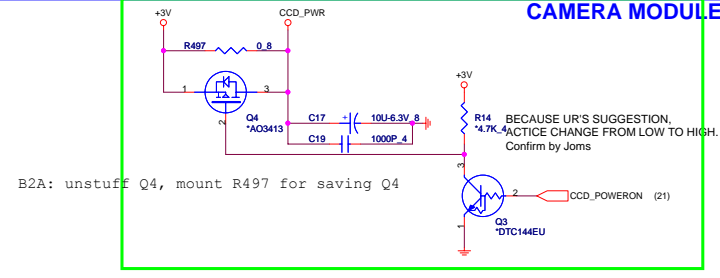
Edison-- 1025 Modify the LVDS pin definition



LCD POWER

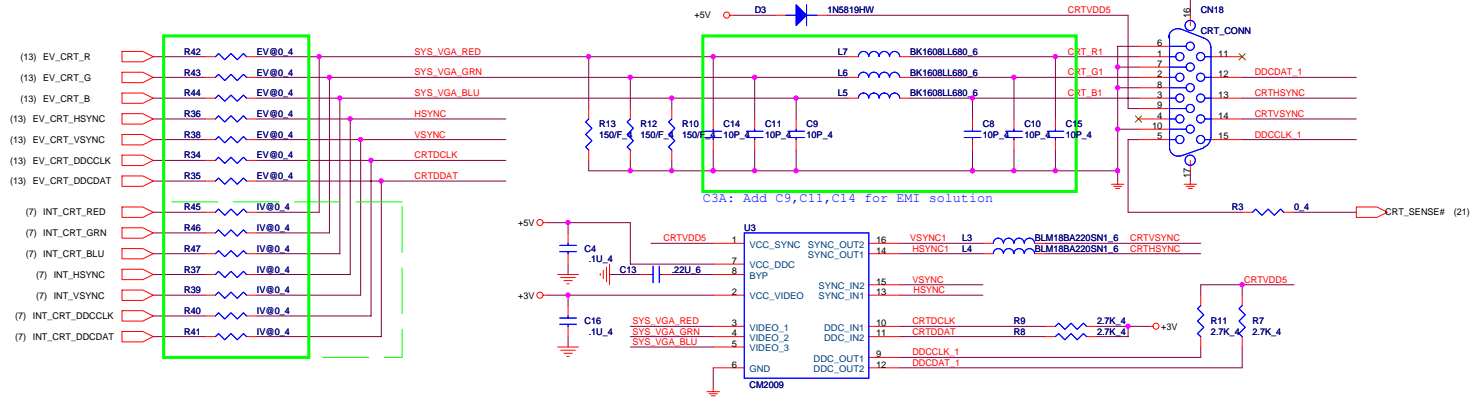


CAMERA MODULE POWER

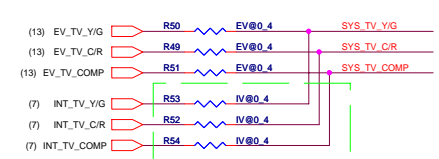


CRT

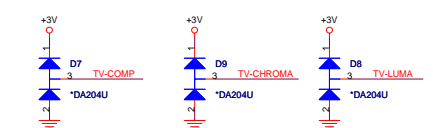
Close MXM CONN



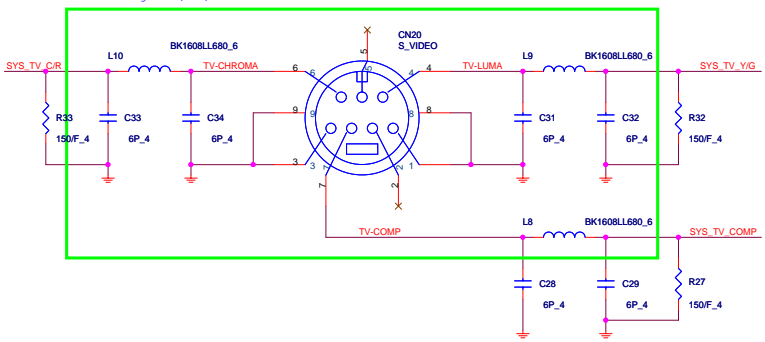
TV Out (SVHS) MiniDIN 7-pin



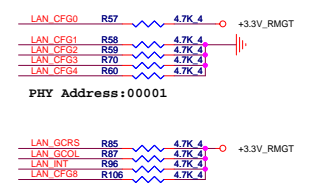
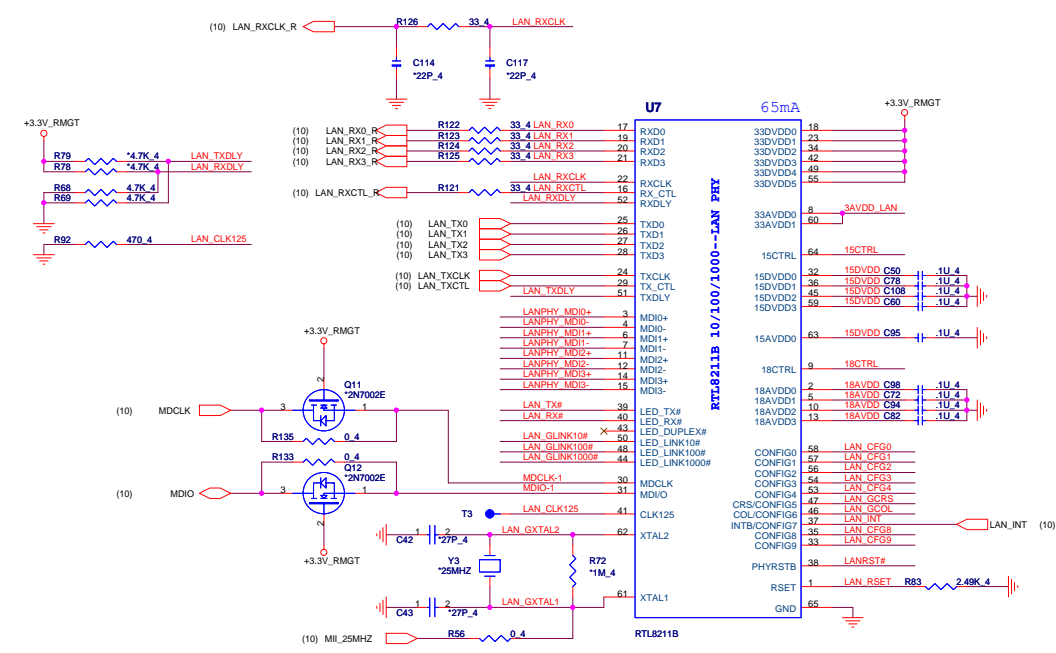
ESD Protect



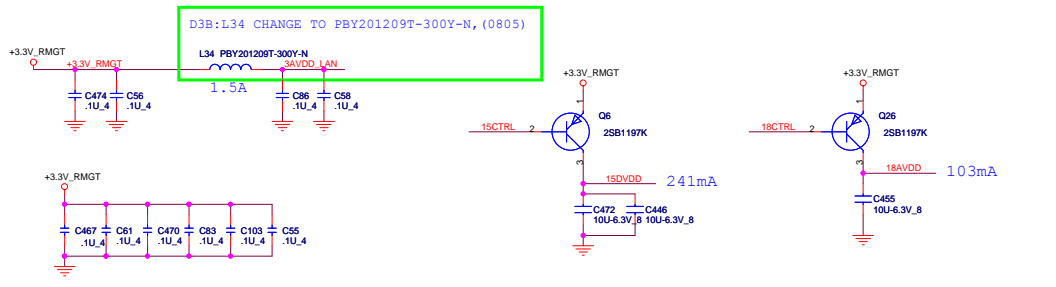
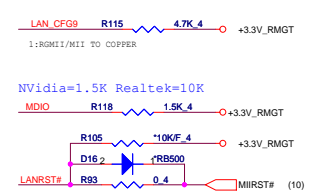
D3B: Change L8,L9,L10 P/N



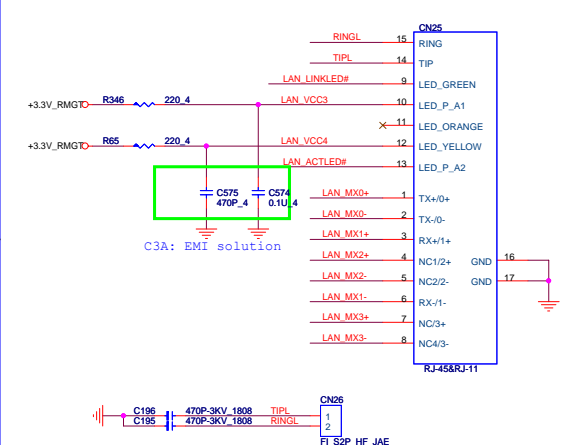
Remove HDMI



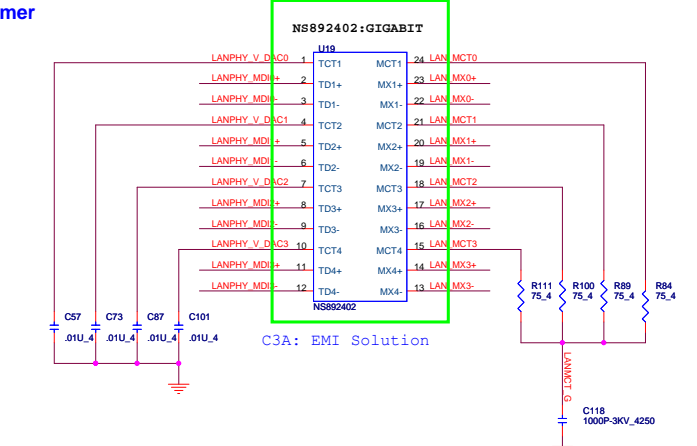
LAN_CRIS	1	auto-na	Advertise All Capabilities, Prefer Slave
LAN_COL	1	auto-na	
LAN_INT	1	auto-na	
CONFIG8	1	auto-na	



RJ45-11

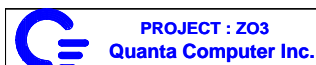
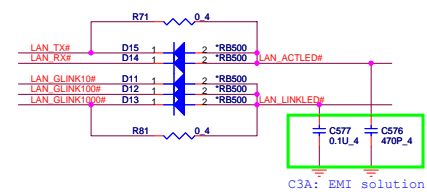


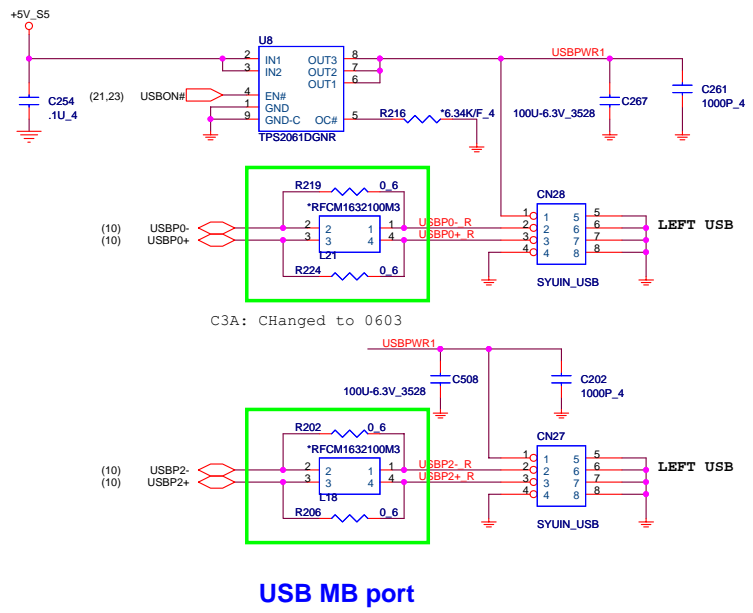
Transformer



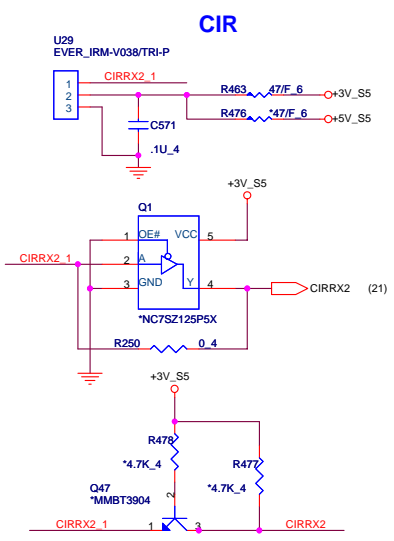
LED Configuration

	Set Register 24 Control Bit=1
LED_LINK1000	LOW=LINK UP (ANY SPEED)
LED_TX	BLINKING=TRANSMITTING OR RECEIVING

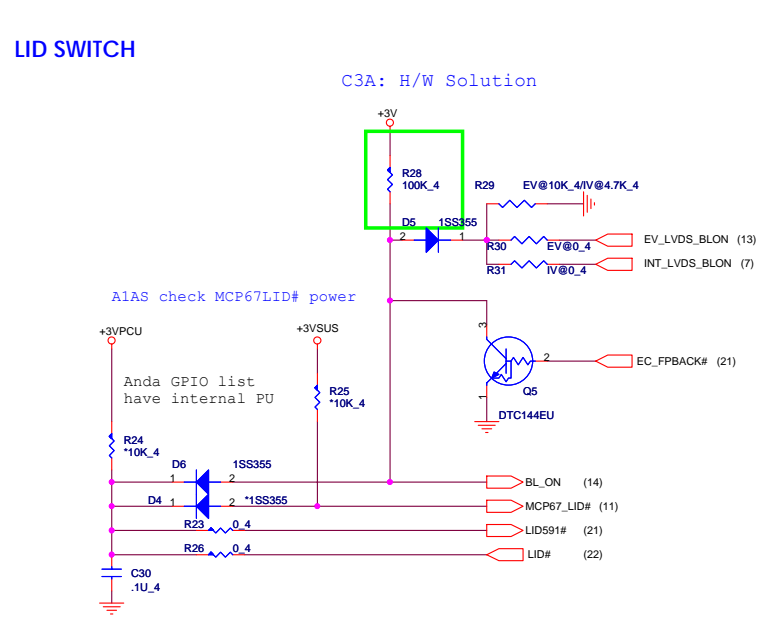




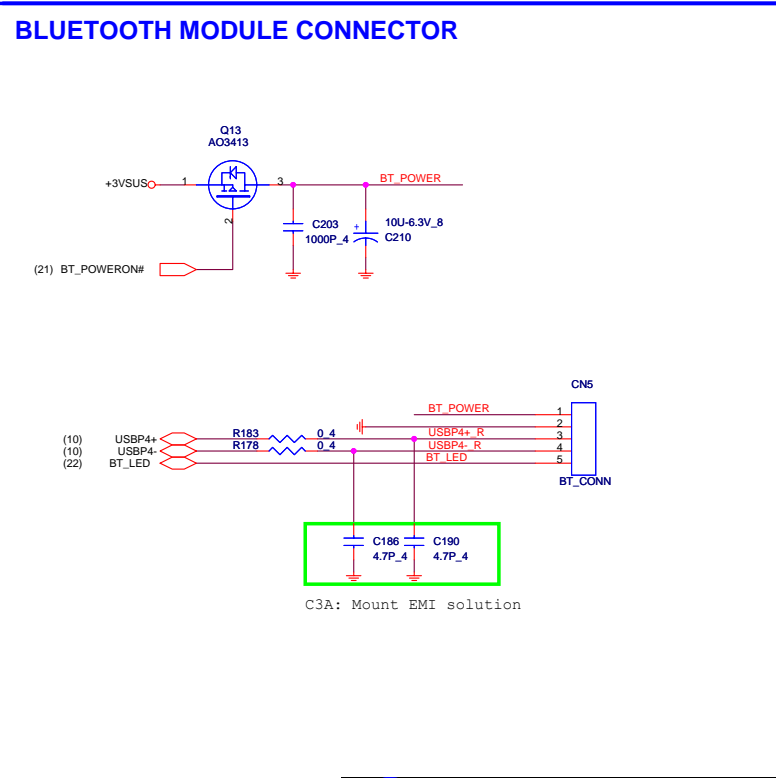
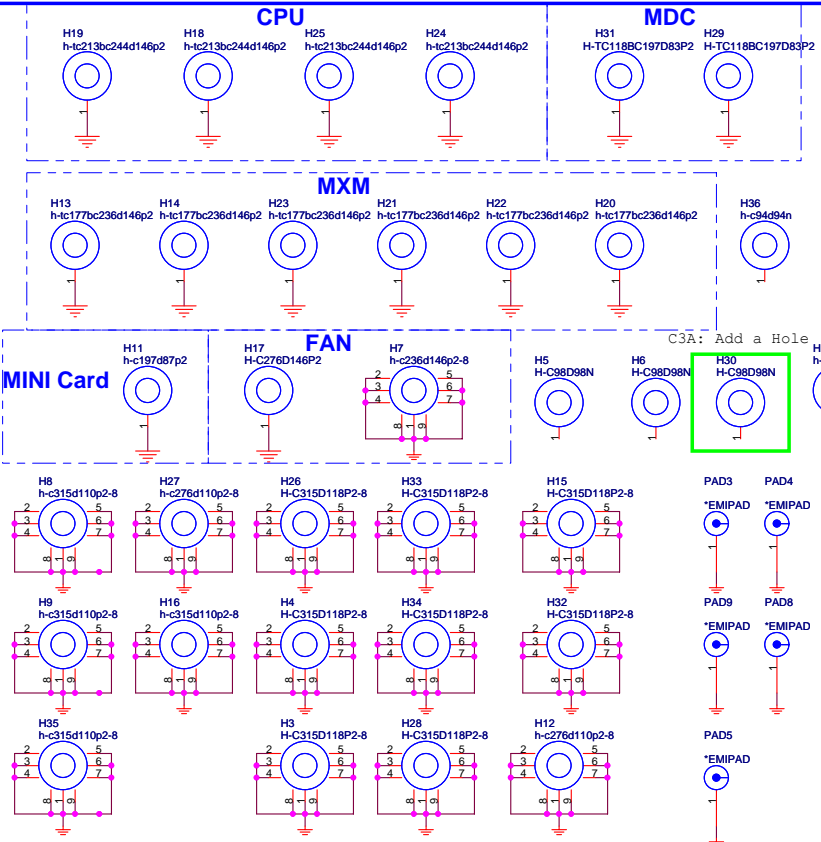
USB MB port



CIR

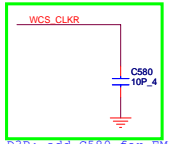


LID SWITCH

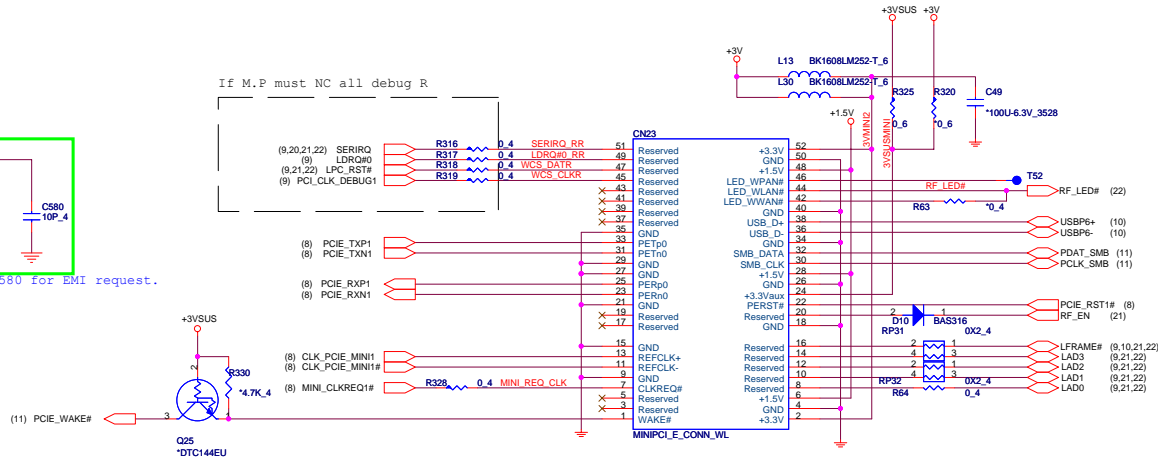


BLUETOOTH MODULE CONNECTOR

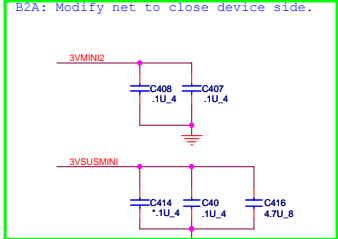
MINI-Card



D3B: add C580 for EMI request.



If M.P must NC all debug R

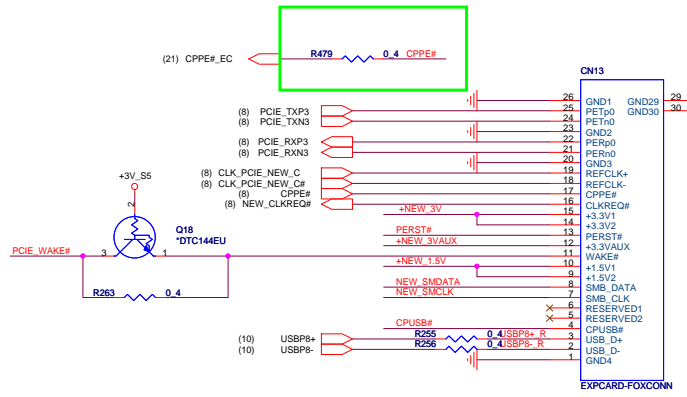


B2A: Modify net to close device side.

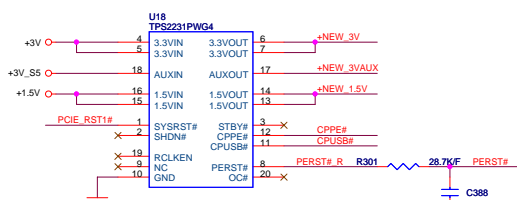
Need reserve 3G pin define
Check Footprint

New card

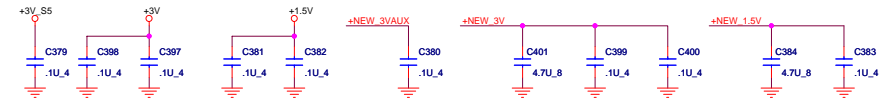
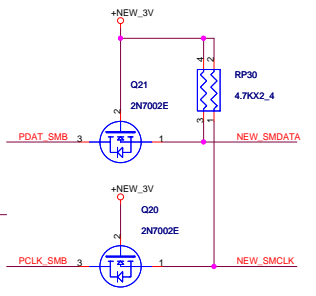
D3B: Add R479 for NEW card CPPE#



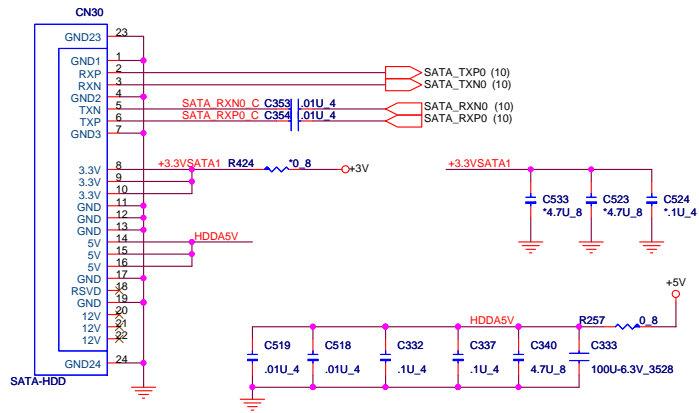
NEW CARD'S POWER SWITCH



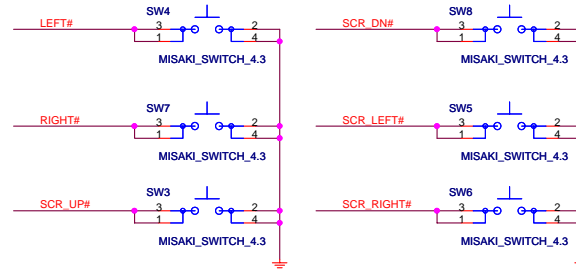
CPPE# : (Internal Pull Up , active low when card support PCIE)
 CPUSB# : (Internal Pull Up , active low when card support USB)
 SHDN# : (Internal Pull Up)



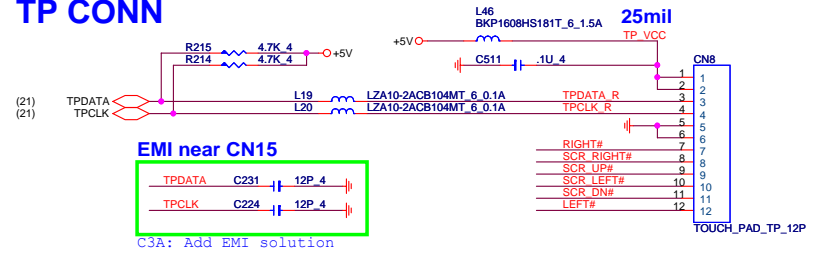
SATA HDD1



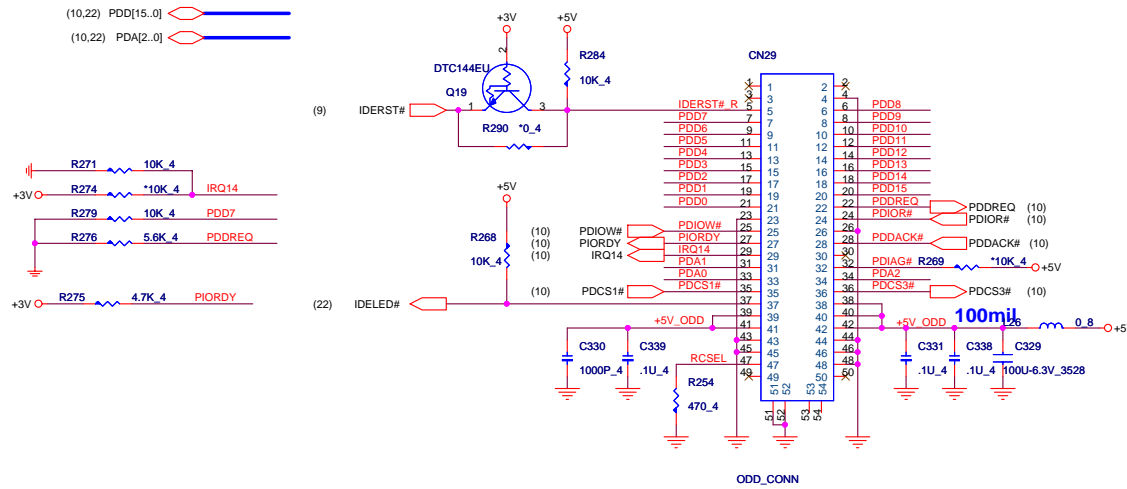
TP SWITCH



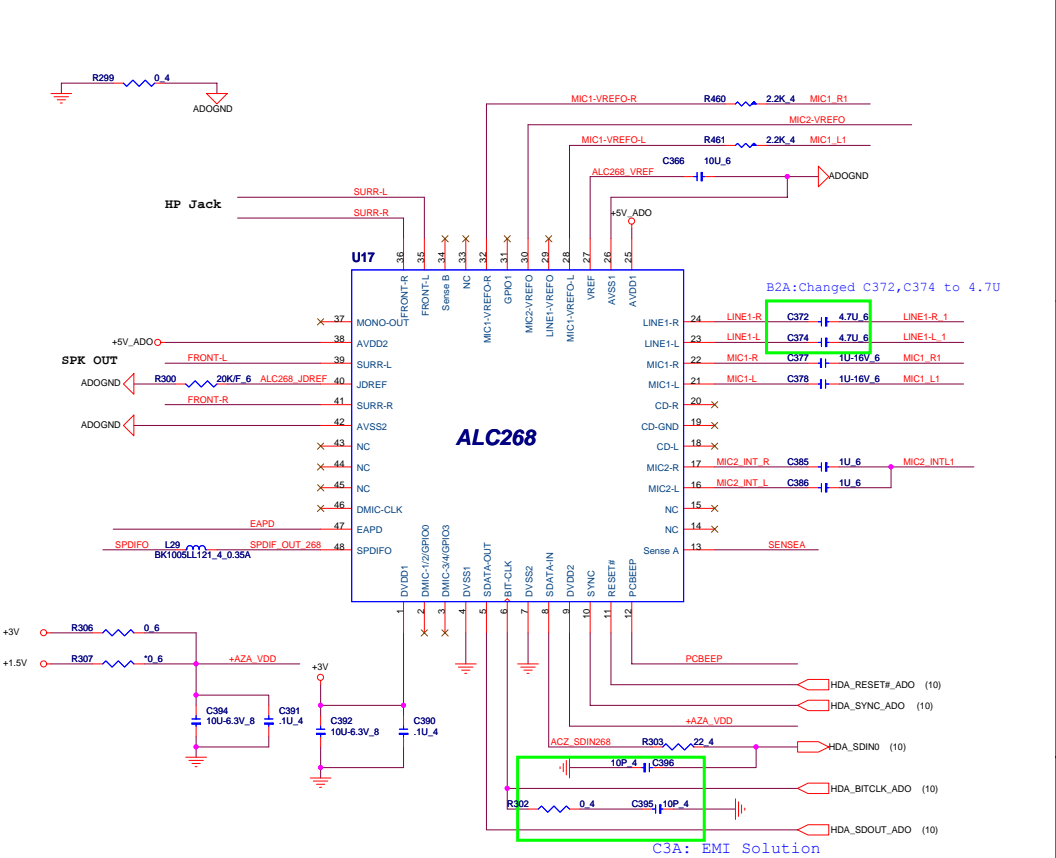
TP CONN



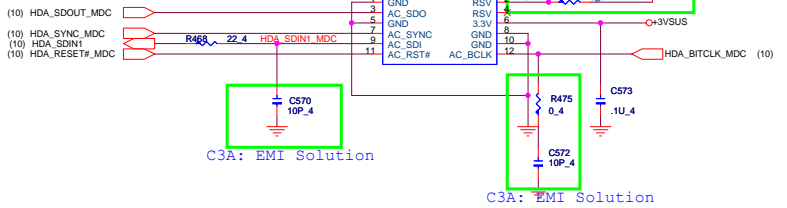
ODD (PATA)



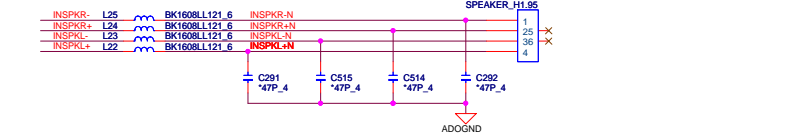
CODEC (ALC268)



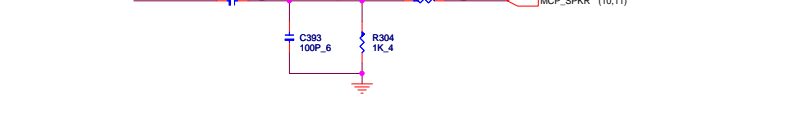
MDC



SPK



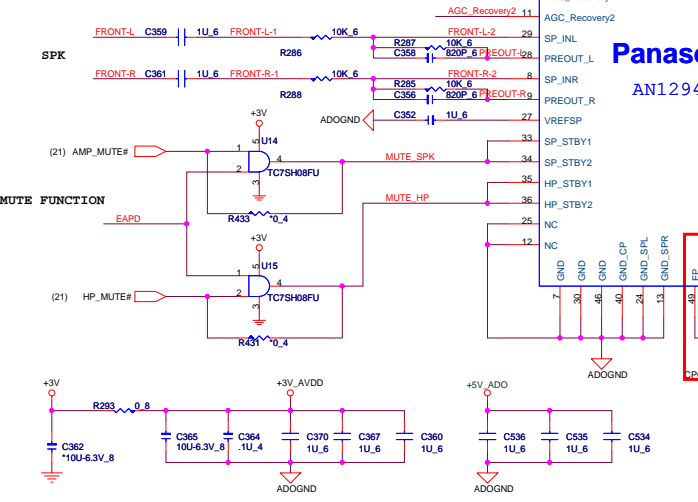
Beep



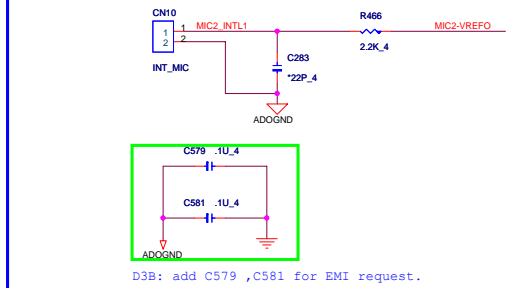
SP_STBY ON/OFF & HP_STBY ON/OFF

SP_STBY1 (33 pin)	SP_STBY2 (34 pin)	SP_STBY ON/OFF
LOW	LOW	ON
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF

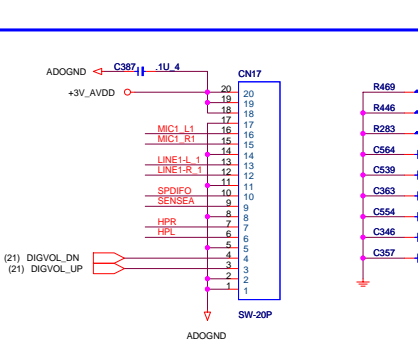
HP_STBY1 (35 pin)	HP_STBY2 (36 pin)	HP_STBY ON/OFF
LOW	LOW	ON
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF



INT MIC array



CODEC (ALC268) Power



AGC-attack-time selection

AGC_Attack (4 pin)	Attack time
Hi	3 ms
Lo	2 ms

AGC ON/OFF selection

AGC_ON/OFF (6 pin)	AGC ON/OFF
LOW	ON
HI	OFF

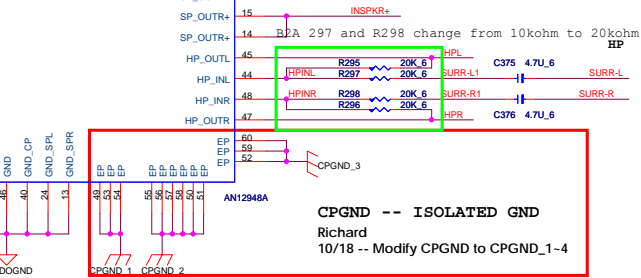
AGC-recovery-time selection

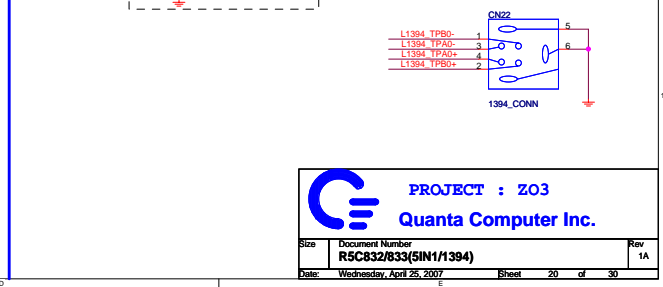
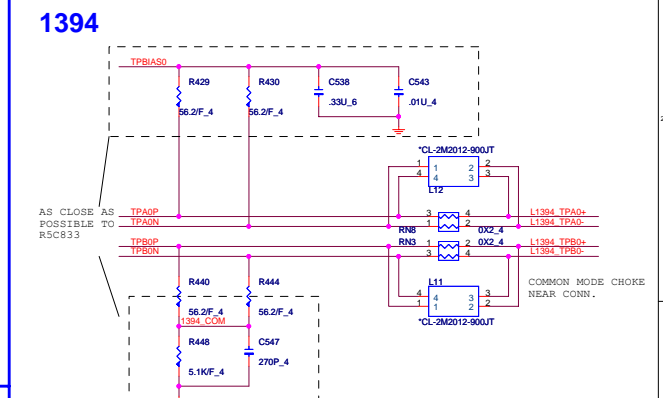
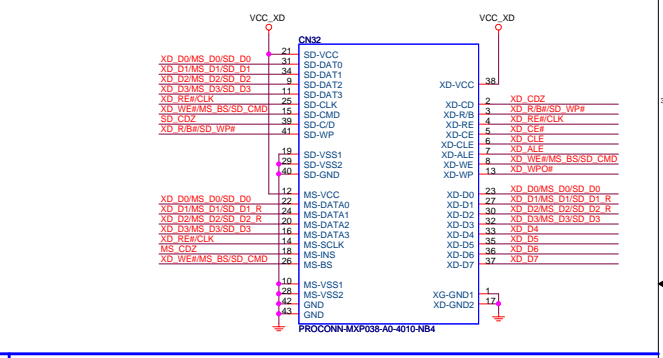
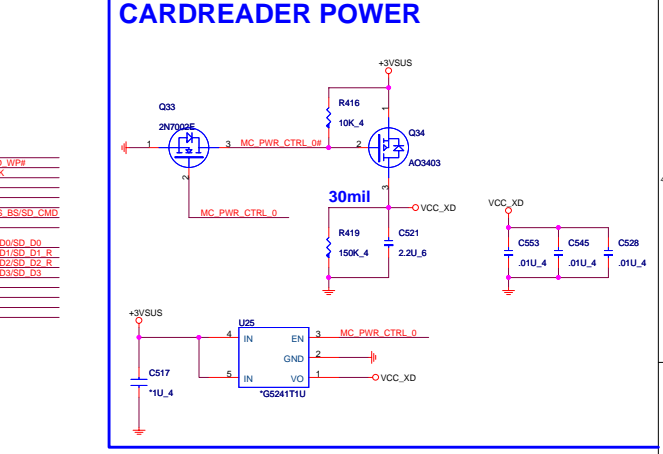
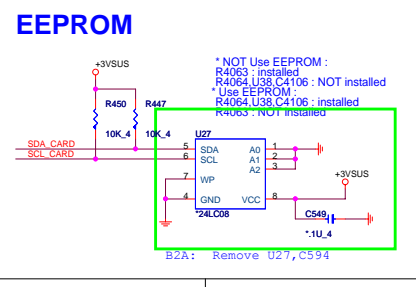
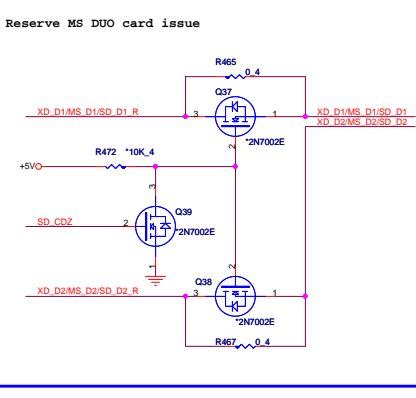
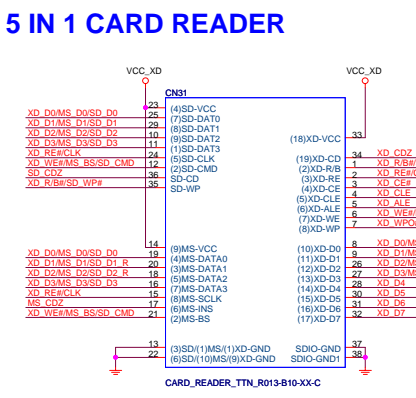
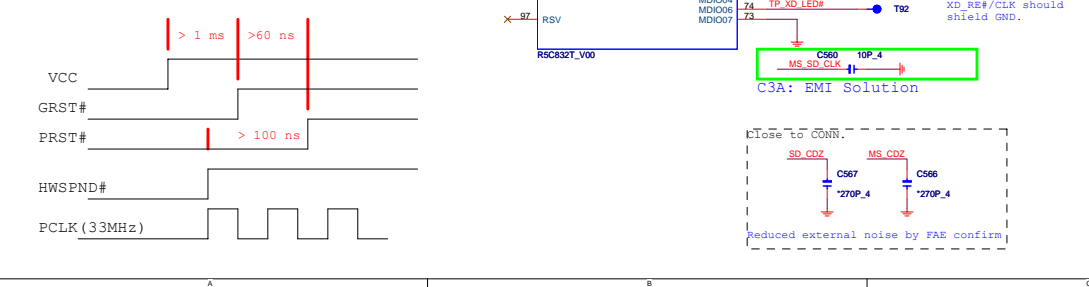
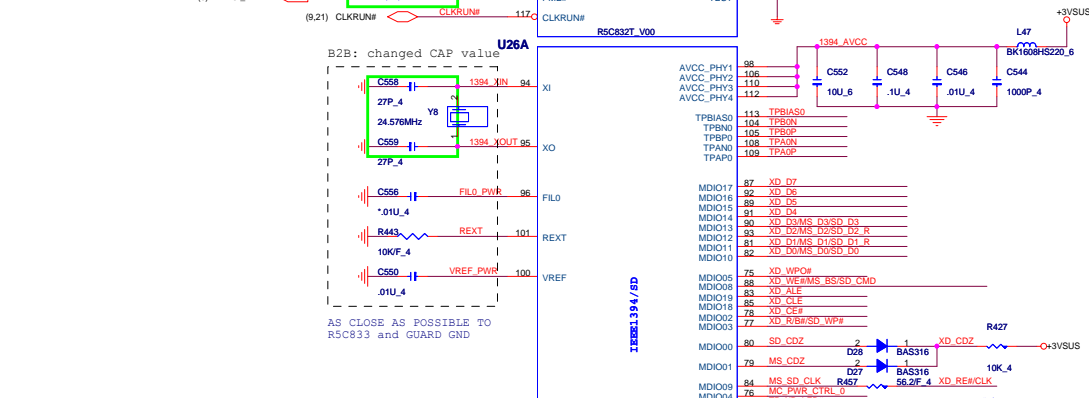
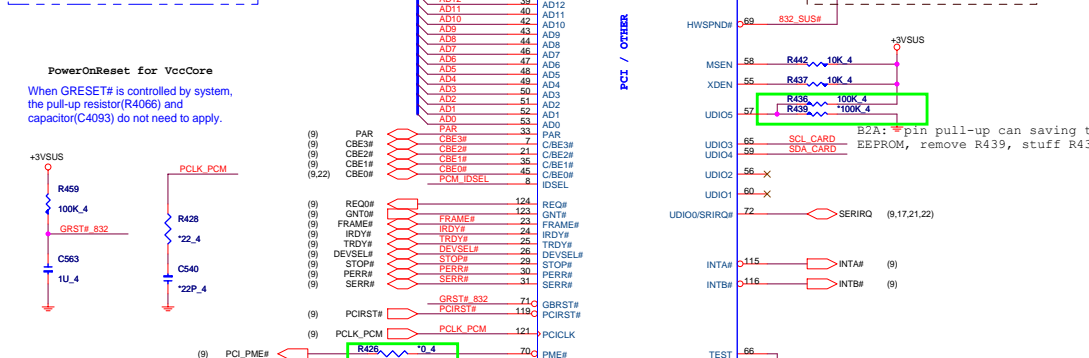
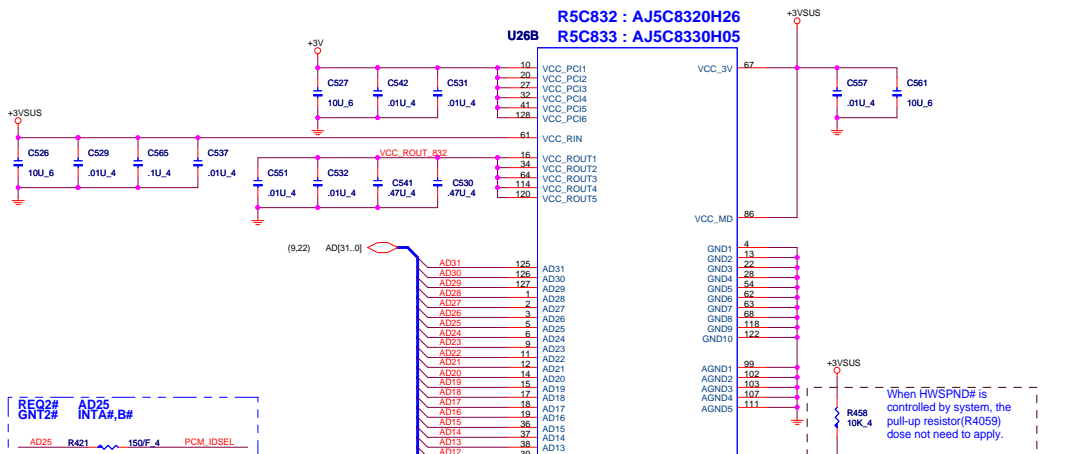
AGC_Recovery1 (10 pin)	AGC_Recovery2 (11 pin)	Recovery Time
LOW	LOW	1.0s
LOW	HI	2.0s
HI	LOW	4.0s
HI	HI	8.0s

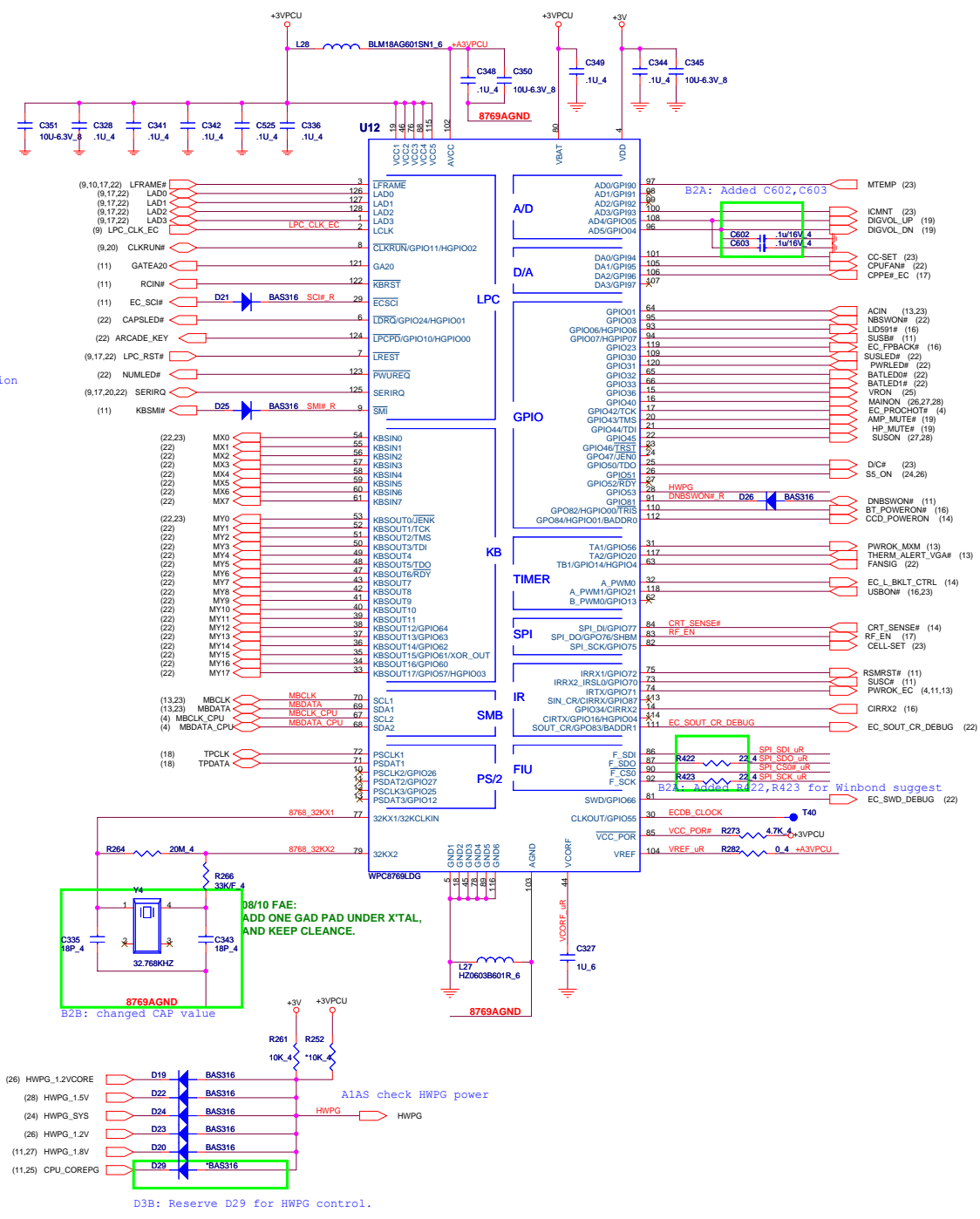
AGC-on-level selection

AGC_Lv1 (2 pin)	AGC_Lv2 (3 pin)	AGC ON Level	Output Po (RL=8 ohm)
LOW	LOW	9.0dBV	1.2 W
LOW	HI	9.0dBV	1.0 W
HI	LOW	8.1dBV	0.8 W
HI	HI	6.0dBV	0.5 W

Panasonic AN12948A



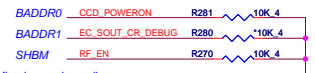




I/O ADDRESS SETTING

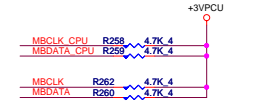
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

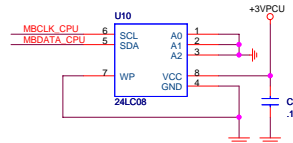


1/13 Confirm by vendor mail :
Disabled (*) if using FWB device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware

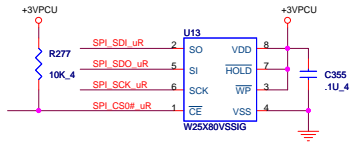
SMBUS PULL-UP



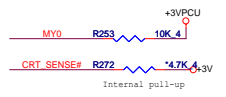
ACER ID



SPI FLASH



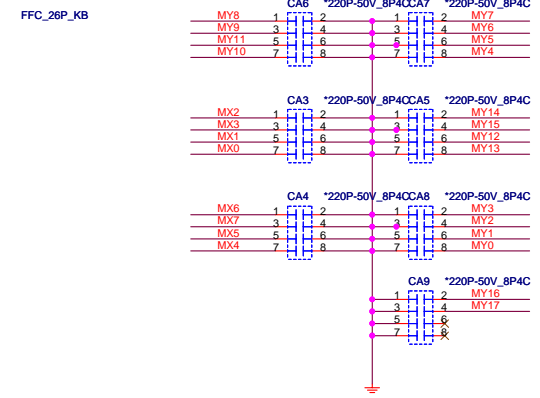
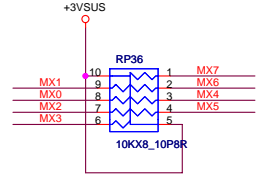
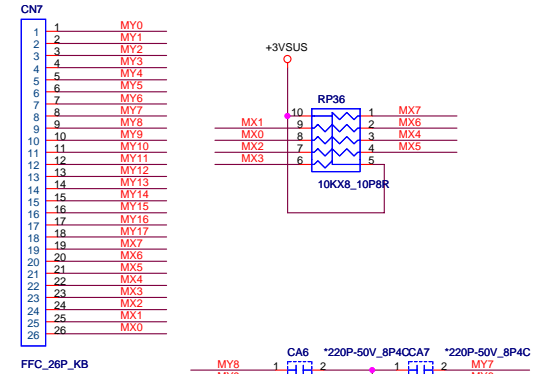
INTERNAL KEYBOARD STRIP SET



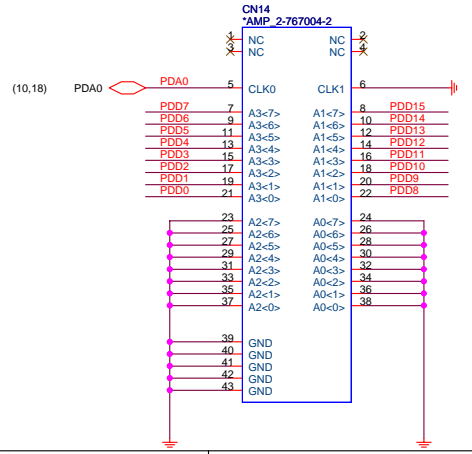
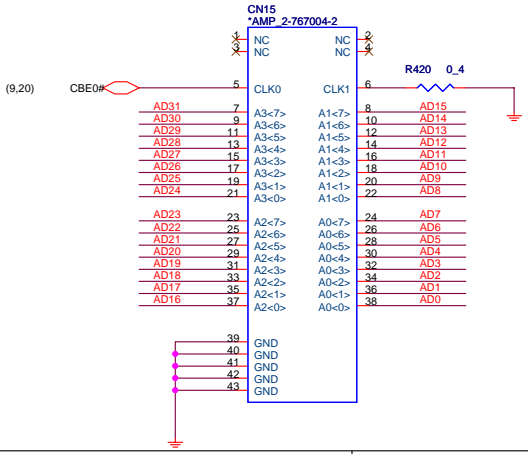
PROJECT : Z03
Quanta Computer Inc.

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	PC8769L & FLASH	1A
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INT K/B

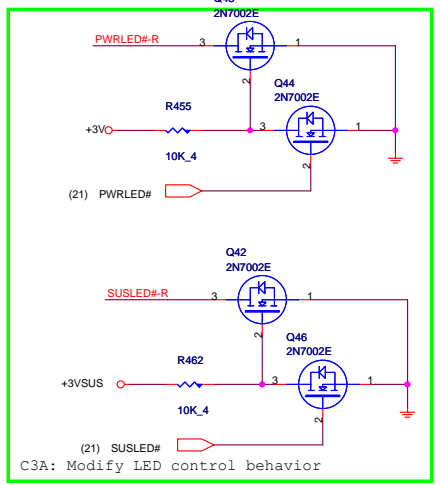
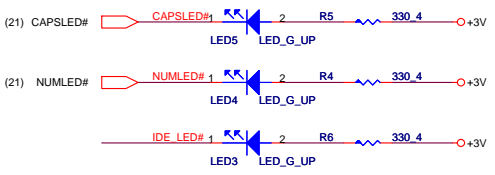
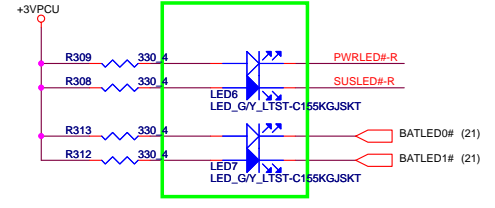


Debug



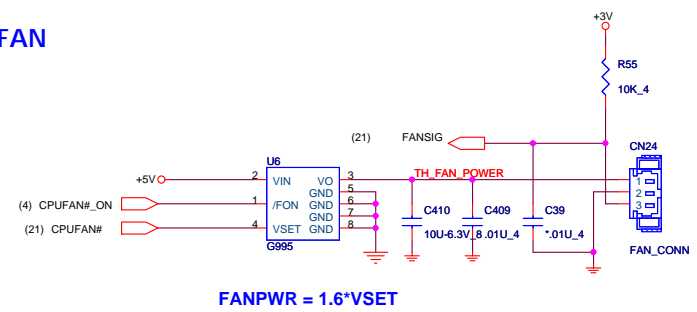
LED

10/16:Changed. Follow BL3 LED



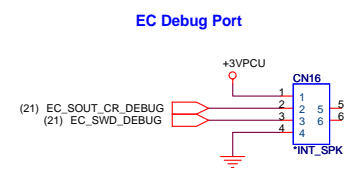
C3A: Modify LED control behavior

CPU FAN

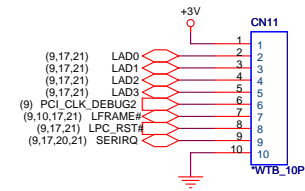


FANPWR = 1.6 * VSET

DEBUG PORT



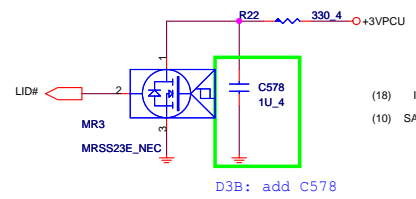
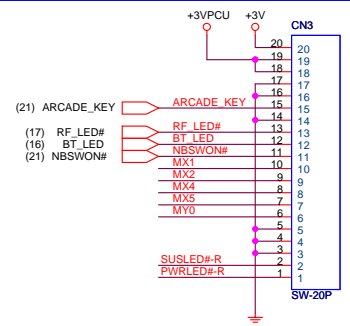
Reserved for LPC debug card



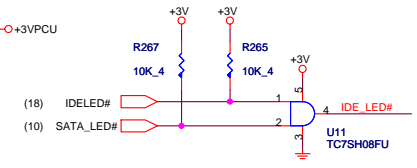
Button

BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH

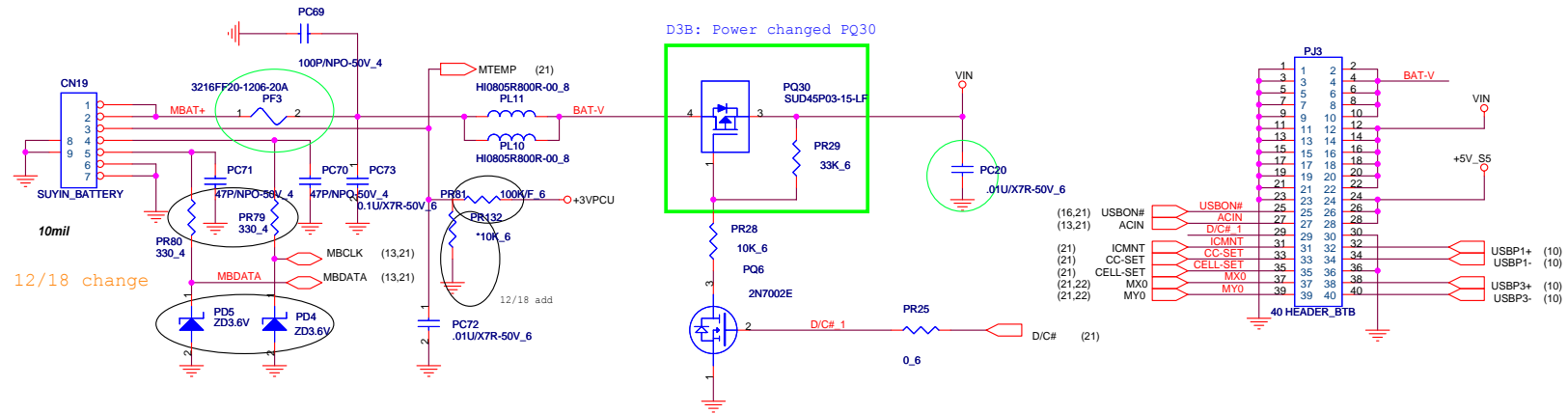


D3B: add C578



PROJECT : ZO3
Quanta Computer Inc.

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	FAN,SWITCH,LED,KB,DEBUG PORT,TP	1A
Date:	Wednesday, April 25, 2007	Sheet 22 of 30

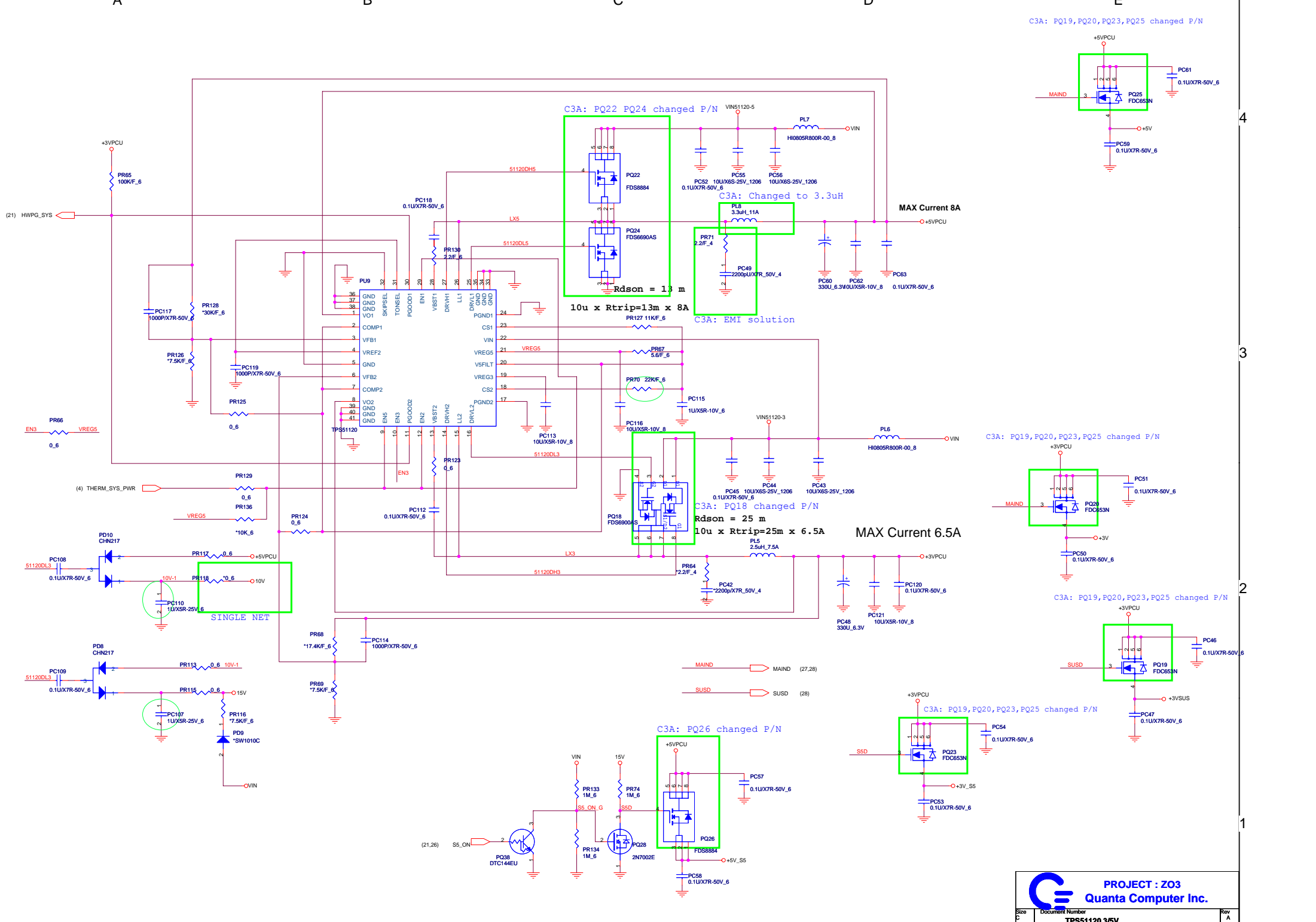


12/18 change

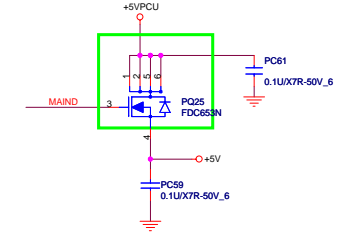
CELL-SET = Hi ----> Cells = VDD ---->4S
 CELL-SET = Low ----> Cells = GND ---->3S

PROJECT : Z03
Quanta Computer Inc.

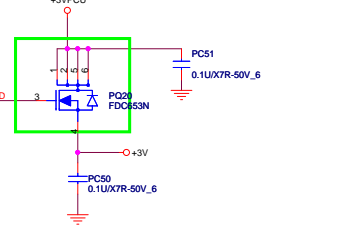
Size	Document Number	Rev
Custom	ISL6251 CHARGER	A
Date:	Wednesday, April 25, 2007	Sheet 23 of 30



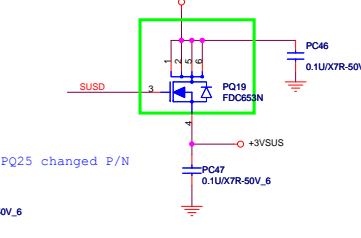
C3A: PQ19, PQ20, PQ23, PQ25 changed P/N



C3A: PQ19, PQ20, PQ23, PQ25 changed P/N

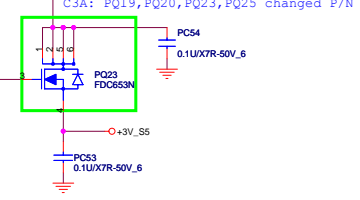


C3A: PQ19, PQ20, PQ23, PQ25 changed P/N

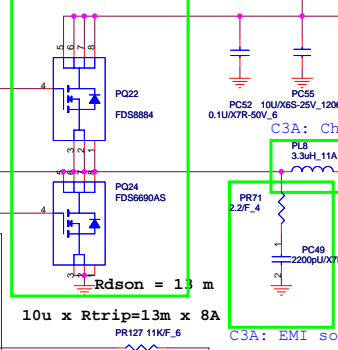


C3A: PQ19, PQ20, PQ23, PQ25 changed P/N

C3A: PQ19, PQ20, PQ23, PQ25 changed P/N



C3A: PQ22 PQ24 changed P/N

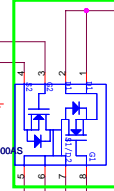


C3A: Changed to 3.3uH

C3A: EMI solution

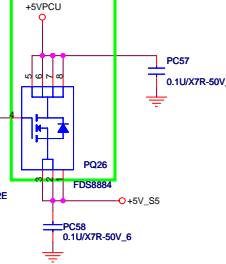
$R_{ds(on)} = 13\text{ m}$
 $10\text{u} \times R_{trip} = 13\text{m} \times 8\text{A}$

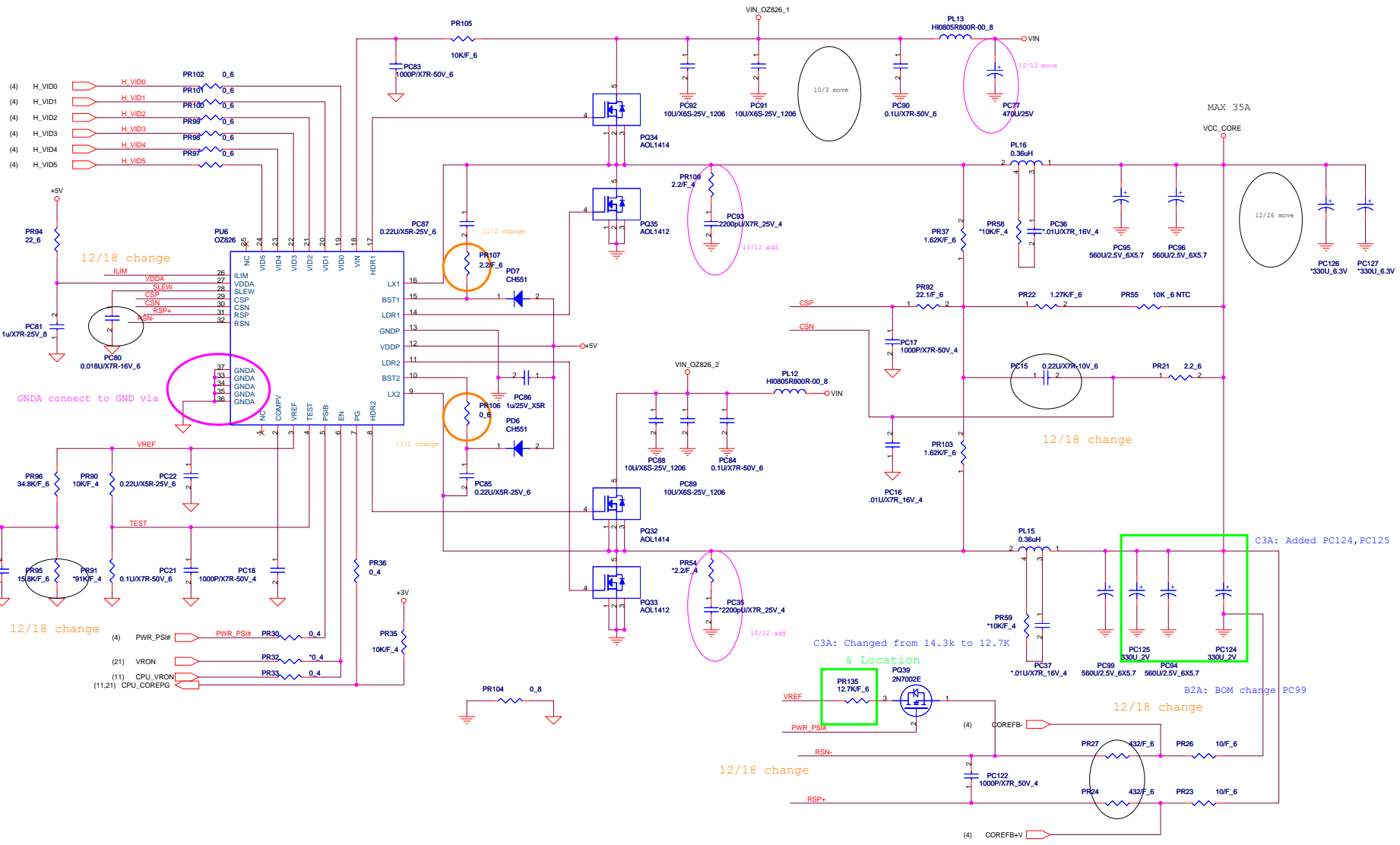
C3A: PQ18 changed P/N

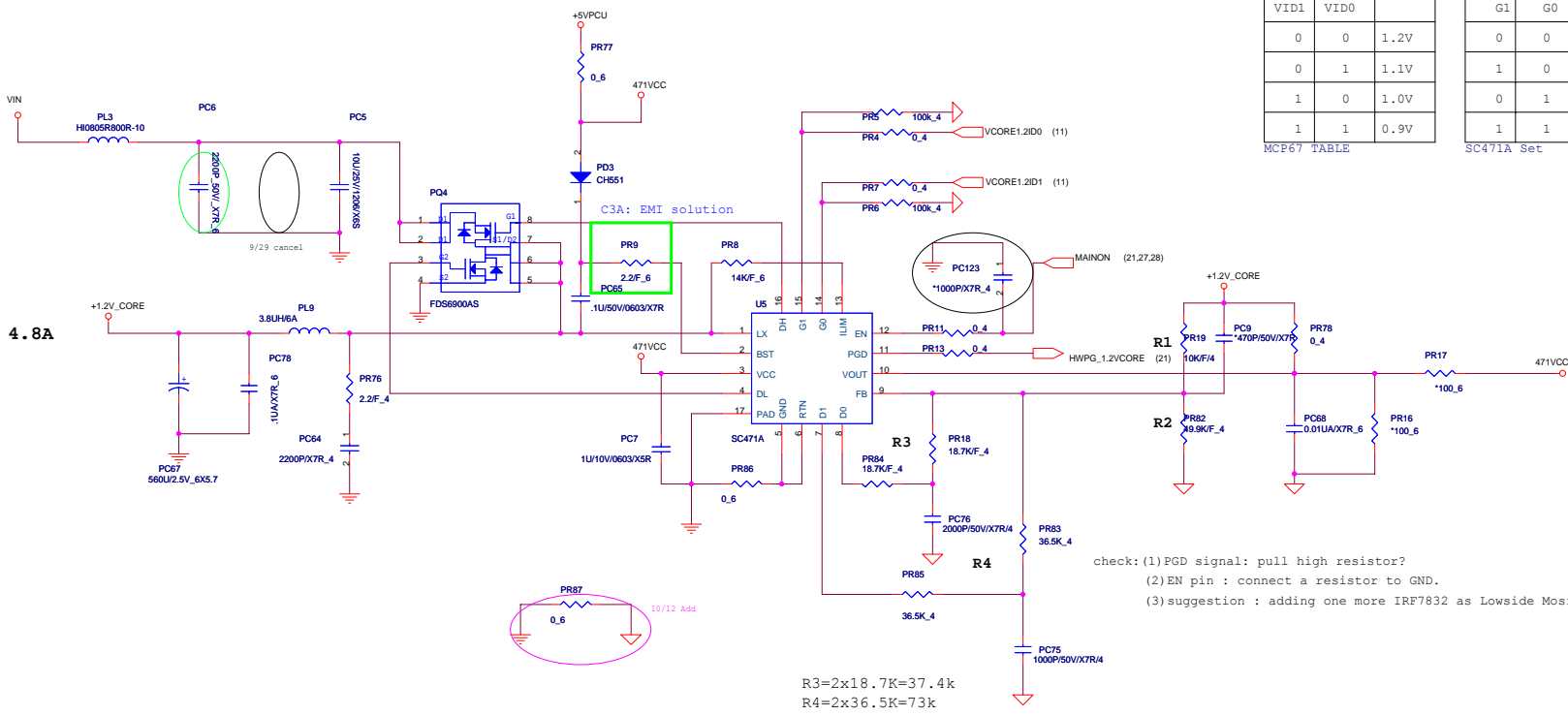


$R_{ds(on)} = 25\text{ m}$
 $10\text{u} \times R_{trip} = 25\text{m} \times 6.5\text{A}$

C3A: PQ26 changed P/N







VID[1:0]		
VID1	VID0	
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS			VOUT1
G1	G0	OD1	OD2	OD3	
0	0	0.75x(1+R1/R2+R1/R3+R1/R4)			1.2V
1	0	0.75x(1+R1/R2+R1/R3)			1.1V
0	1	0.75x(1+R1/R2+R1/R4)			1.0V
1	1	0.75x(1+R1/R2)			0.9V

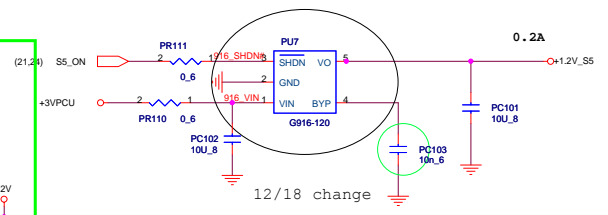
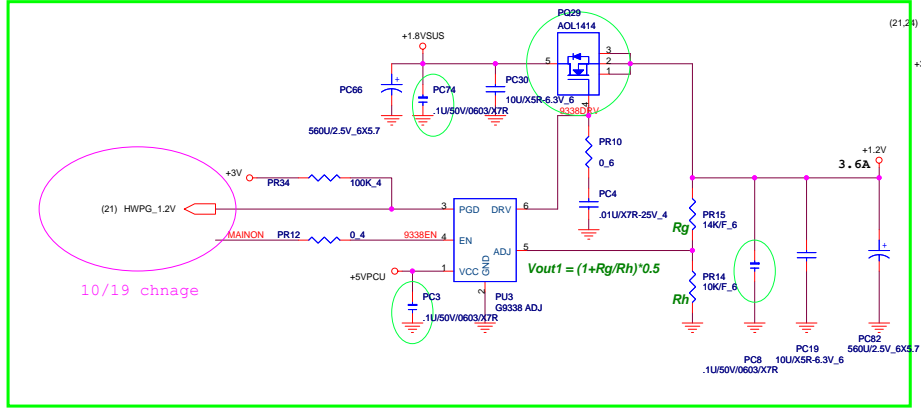
SC471A Set

4.8A

- check: (1) PGD signal: pull high resistor?
- (2) EN pin : connect a resistor to GND.
- (3) suggestion : adding one more IRF7832 as Lowside Mosfet.

R3=2x18.7k=37.4k
R4=2x36.5k=73k

B2B: FOR UMA ONLY



10/19 chnagne

12/18 change

