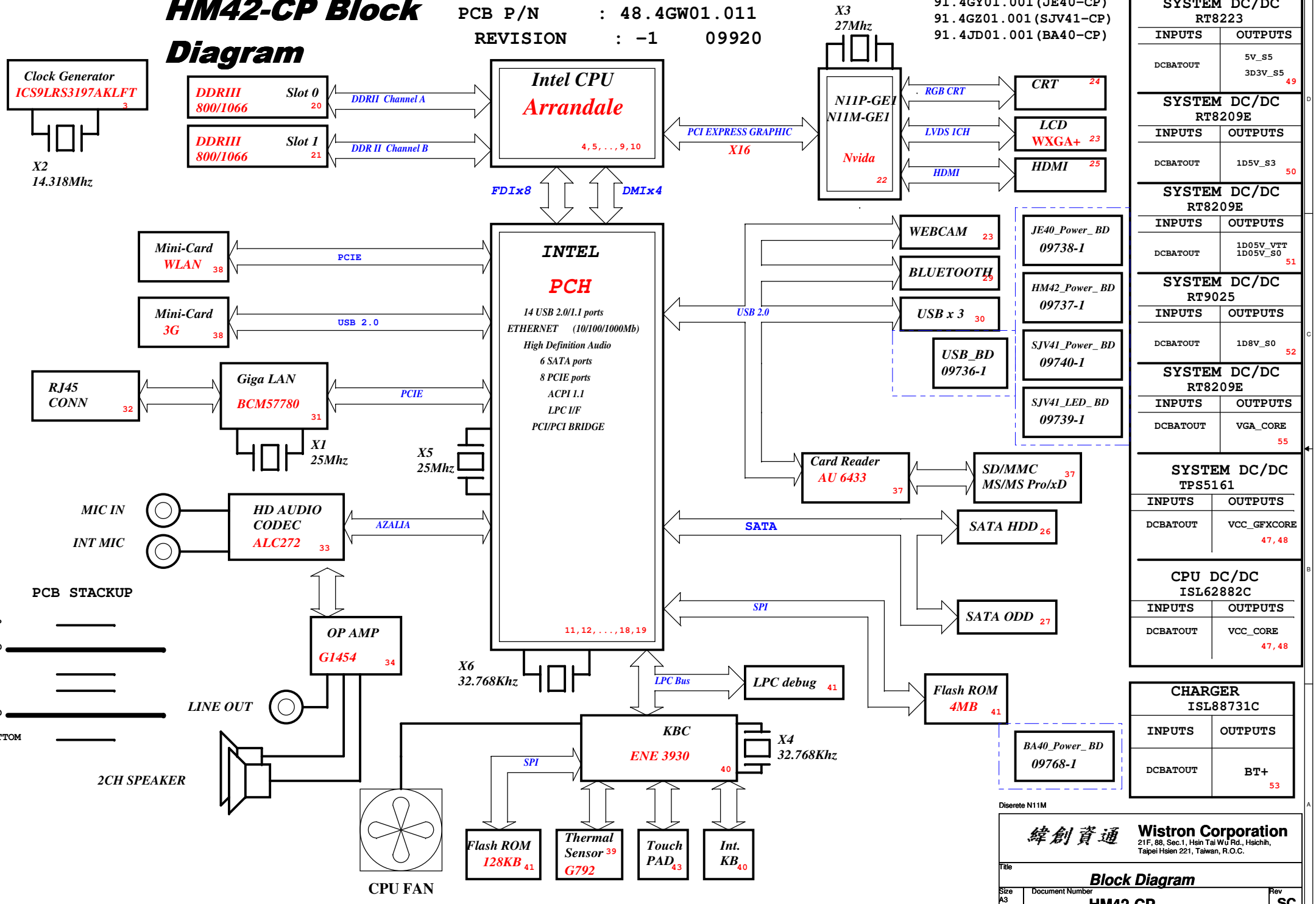
HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
REVISION : -1 09920

Project code: 91.4GW01.001(HM42-CP)
91.4GY01.001(JE40-CP)
91.4GZ01.001(SJV41-CP)
91.4JD01.001(BA40-CP)



SYSTEM DC/DC RT8223

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0 51

SYSTEM DC/DC RT9025

INPUTS	OUTPUTS
DCBATOUT	1D8V_S0 52

SYSTEM DC/DC RT8209E

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 55

SYSTEM DC/DC TPS5161

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 47,48

CPU DC/DC ISL62882C

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

CHARGER ISL88731C

INPUTS	OUTPUTS
DCBATOUT	BT+ 53

Diserete N11M

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

<Variant Name>

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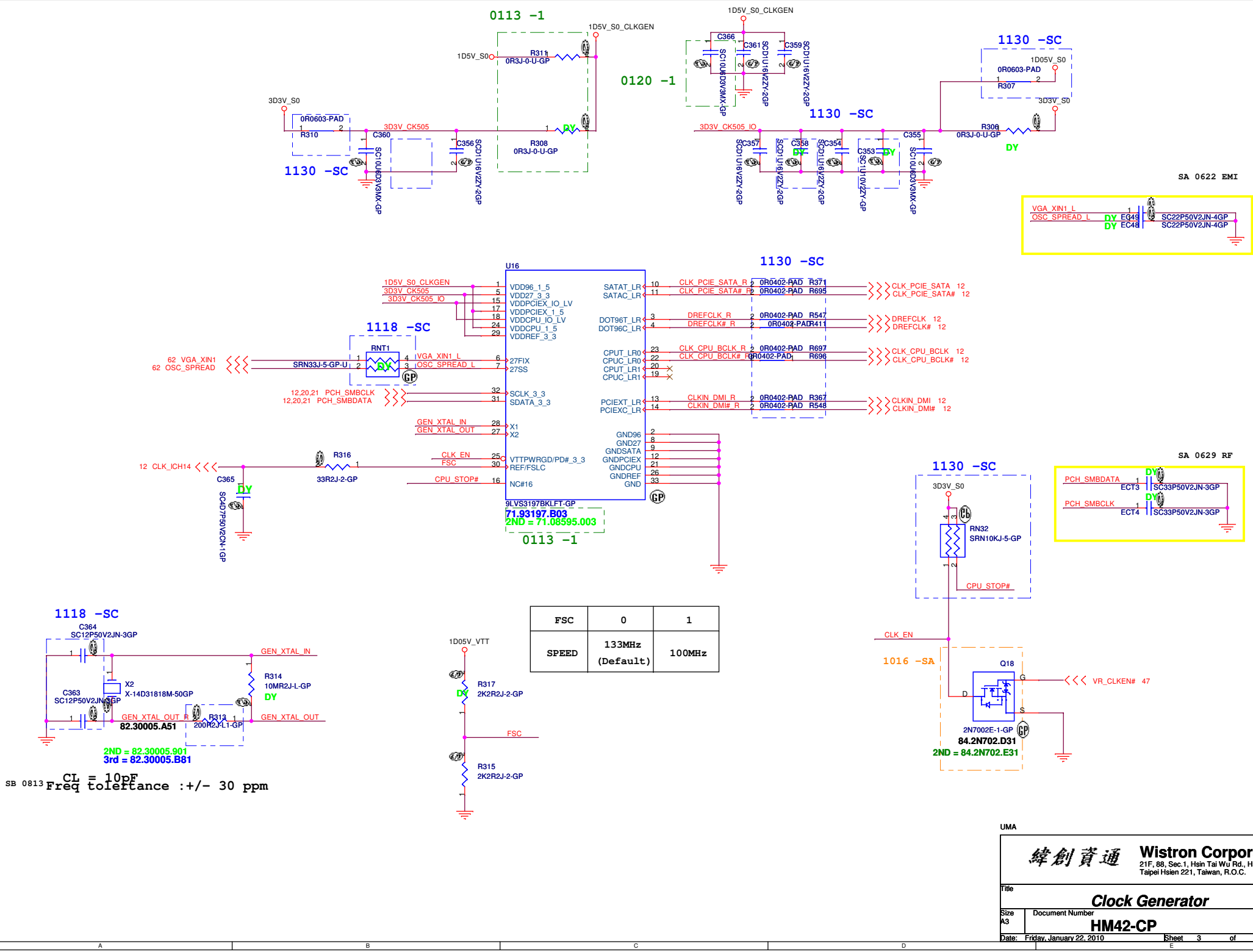
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1D5V_S0
R311
0R3J-0-U-GP
3D3V_S0
0R0603-PAD
R310
3D3V_CK505
C360
SC10U6D3V3MX-GP
C356
SCD1U16V2ZY-2GP
R308
0R3J-0-U-GP
DY
1130 -SC
0120 -1
C366
C361
C359
SCD1U16V2ZY-2GP
1130 -SC
1D05V_S0
0R0603-PAD
R307
3D3V_S0
3D3V_CK505_IO
C357
C358
C354
C353
C355
R306
0R3J-0-U-GP
DY
SA 0622 EMI
VGA_XIN1_L
OSC_SPREAD_L
EC49
EC48
SC22P50V2JN-4GP
U16
1130 -SC
1118 -SC
RNT1
SRN33J-5-GP-U
62 VGA_XIN1
62 OSC_SPREAD
VGA_XIN1_L
OSC_SPREAD_L
27FIX
27SS
12,20,21 PCH_SMBCLK
12,20,21 PCH_SMBDATA
SCLK_3_3
SDATA_3_3
GEN_XTAL_IN
GEN_XTAL_OUT
X1
X2
12 CLK_ICH14
R316
33R2J-2-GP
C365
SCAD7P50V2CN-1GP
CLK_EN
FSC
CPU_STOP#
VTTPWRGD/PD#_3_3
REF/FSLC
NC#16
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71.93197.B03
2ND = 71.08595.003
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VDD96_1_5
VDD27_3_3
VDDPCIEX_IO_LV
VDDPCIEX_1_5
VDDCPU_IO_LV
VDDCPU_1_5
VDDREF_3_3
SATAT_LR
SATAC_LR
DOT96T_LR
DOT96C_LR
CPUT_LR0
CPUC_LR0
CPUT_LR1
CPUC_LR1
PCIEXT_LR
PCIEXC_LR
GND96
GND27
GNDSATA
GNDPCIEX
GNDCPU
GNDREF
GND
CLK_PCIE_SATA_R
CLK_PCIE_SATA# R
0R0402-PAD
R371
R695
CLK_PCIE_SATA 12
CLK_PCIE_SATA# 12
DREFCLK_R
DREFCLK# R
R547
R411
DREFCLK 12
DREFCLK# 12
CLK_CPU_BCLK_R
CLK_CPU_BCLK# R
R697
R696
CLK_CPU_BCLK 12
CLK_CPU_BCLK# 12
CLKIN_DMI_R
CLKIN_DMI# R
R367
R548
CLKIN_DMI 12
CLKIN_DMI# 12
SA 0629 RF
PCH_SMBDATA
PCH_SMBCLK
ECT3
ECT4
SC33P50V2JN-3GP
1130 -SC
3D3V_S0
RN32
SRN10KJ-5-GP
CPU_STOP#
CLK_EN
1016 -SA
Q18
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
VR_CLKEN# 47
1118 -SC
C364
SC12P50V2JN-3GP
C363
SC12P50V2JN-3GP
X2
X-14D31818M-50GP
GEN_XTAL_IN
GEN_XTAL_OUT
R314
10MR2J-L-GP
DY
R313
200R2J-L1-GP
82.30005.A51
2ND = 82.30005.901
3rd = 82.30005.B81
1D05V_VTT
R317
2K2R2J-2-GP
FSC
R315
2K2R2J-2-GP
FSC
0
1
SPEED
133MHz (Default)
100MHz
SB 0813
CL = 10pF
Freq tolerance :+/- 30 ppm
UMA
緯創資通
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Title
Clock Generator
Size
A3
Document Number
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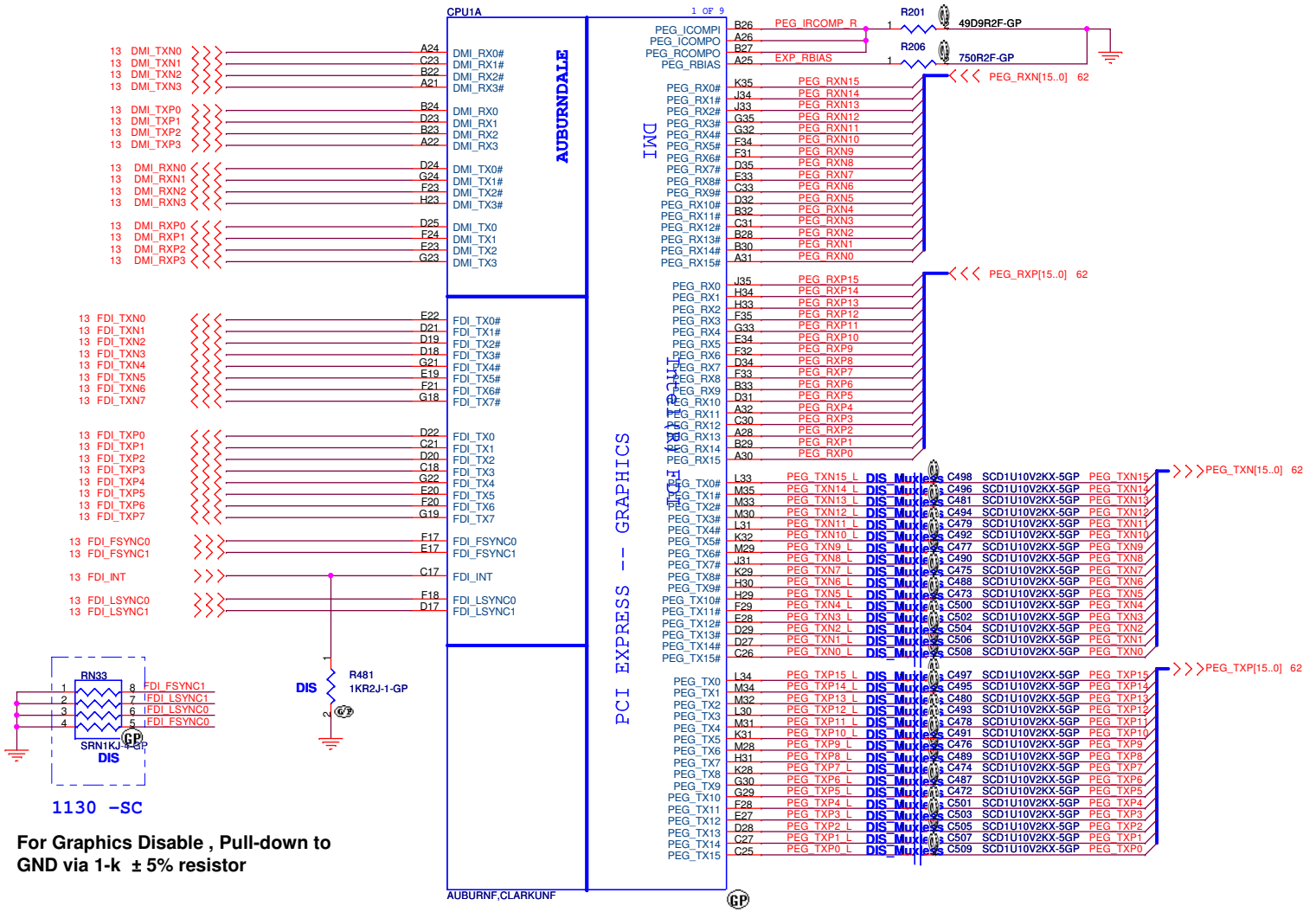

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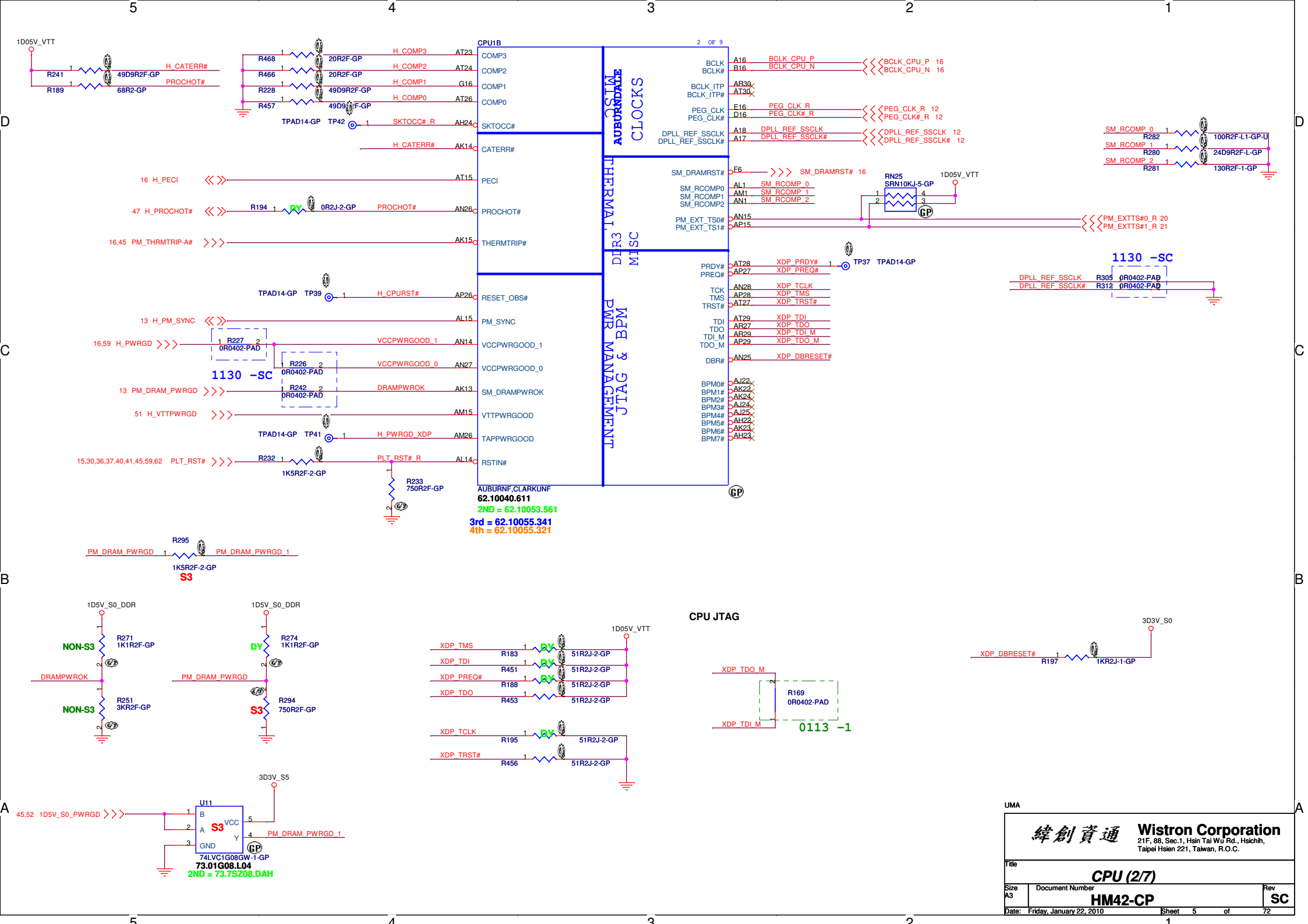
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R189 68R2-GP
H_CATERR#
PROCHOT#
R468 20R2F-GP
R466 20R2F-GP
R228 49D9R2F-GP
R457 49D9R2F-GP
H_COMP3
H_COMP2
H_COMP1
H_COMP0
TPAD14-GP TP42
SKTOCC# R
CPU1B
COMP3 AT23
COMP2 AT24
COMP1 G16
COMP0 AT26
SKTOCC# AH24
CATERR# AK14
PECI AT15
PROCHOT# AN26
THERMTRIP# AK15
RESET_OBS# AP26
PM_SYNC AL15
VCCPWRGOOD_1 AN14
VCCPWRGOOD_0 AN27
SM_DRAMPWROK AK13
VTTPWRGOOD AM15
TAPPWRGOOD AM26
RSTIN# AL14
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2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
2 OF 9
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AUBURNDALE
CLOCKS
DIR3
MISC
THERMAL
JTAG & BPM
PWR MANAGEMENT
BCLK BCLK# A16 B16
BCLK_ITP BCLK_ITP# AR30 AT30
PEG_CLK PEG_CLK# E16 D16
DPLL_REF_SSCLK DPLL_REF_SSCLK# A18 A17
SM_DRAMRST# F6
SM_RCOMP0 AL1
SM_RCOMP1 AM1
SM_RCOMP2 AN1
PM_EXT_TS0# AN15
PM_EXT_TS1# AP15
PRDY# AT28
PREQ# AP27
TCK AN28
TMS AP28
TRST# AT27
TDI AT29
TDO AR27
TDI_M AP29
TDO_M AP29
DBR# AN25
BPM0# AJ22
BPM1# AK22
BPM2# AK24
BPM3# AJ24
BPM4# AJ25
BPM5# AH22
BPM6# AK23
BPM7# AH23
BCLK_CPU_P 16
BCLK_CPU_N 16
PEG_CLK_R 12
PEG_CLK#_R 12
DPLL_REF_SSCLK 12
DPLL_REF_SSCLK# 12
SM_DRAMRST# 16
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
RN25 SRN10KJ-5-GP
PM_EXTTS#0_R 20
PM_EXTTS#1_R 21
SM_RCOMP_0 R282 100R2F-L1-GP-U
SM_RCOMP_1 R280 24D9R2F-L-GP
SM_RCOMP_2 R281 130R2F-1-GP
TP37 TPAD14-GP
1130 -SC
DPLL_REF_SSCLK R305 0R0402-PAD
DPLL_REF_SSCLK# R312 0R0402-PAD
16 H_PECI
47 H_PROCHOT#
R194 DY 0R2J-2-GP
16,45 PM_THRMTRIP-A#
TPAD14-GP TP39
H_CPURST#
13 H_PM_SYNC
16,59 H_PWRGD
R227 0R0402-PAD
1130 -SC
R226 0R0402-PAD
R242 0R0402-PAD
13 PM_DRAM_PWRGD
51 H_VTTPWRGD
TPAD14-GP TP41
H_PWRGD_XDP
15,30,36,37,40,41,45,59,62 PLT_RST#
R232 1K5R2F-2-GP
PLT_RST#_R
R233 750R2F-GP
R295 1K5R2F-2-GP
PM_DRAM_PWRGD
PM_DRAM_PWRGD_1
S3
1D5V_S0_DDR
NON-S3 R271 1K1R2F-GP
DRAMPWROK
NON-S3 R251 3KR2F-GP
DY R274 1K1R2F-GP
PM_DRAM_PWRGD
S3 R294 750R2F-GP
XDP_TMS R183 DY 51R2J-2-GP
XDP_TDI R451 DY 51R2J-2-GP
XDP_PREQ# R188 DY 51R2J-2-GP
XDP_TDO R453 51R2J-2-GP
XDP_TCLK R195 DY 51R2J-2-GP
XDP_TRST# R456 51R2J-2-GP
CPU JTAG
XDP_TDO_M
R169 0R0402-PAD
XDP_TDI_M
0113 -1
3D3V_S0
XDP_DBRESET# R197 1KR2J-1-GP
3D3V_S5
45,52 1D5V_S0_PWRGD
U11
B
A S3
GND
VCC
Y
PM_DRAM_PWRGD_1
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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CPU (2/7)
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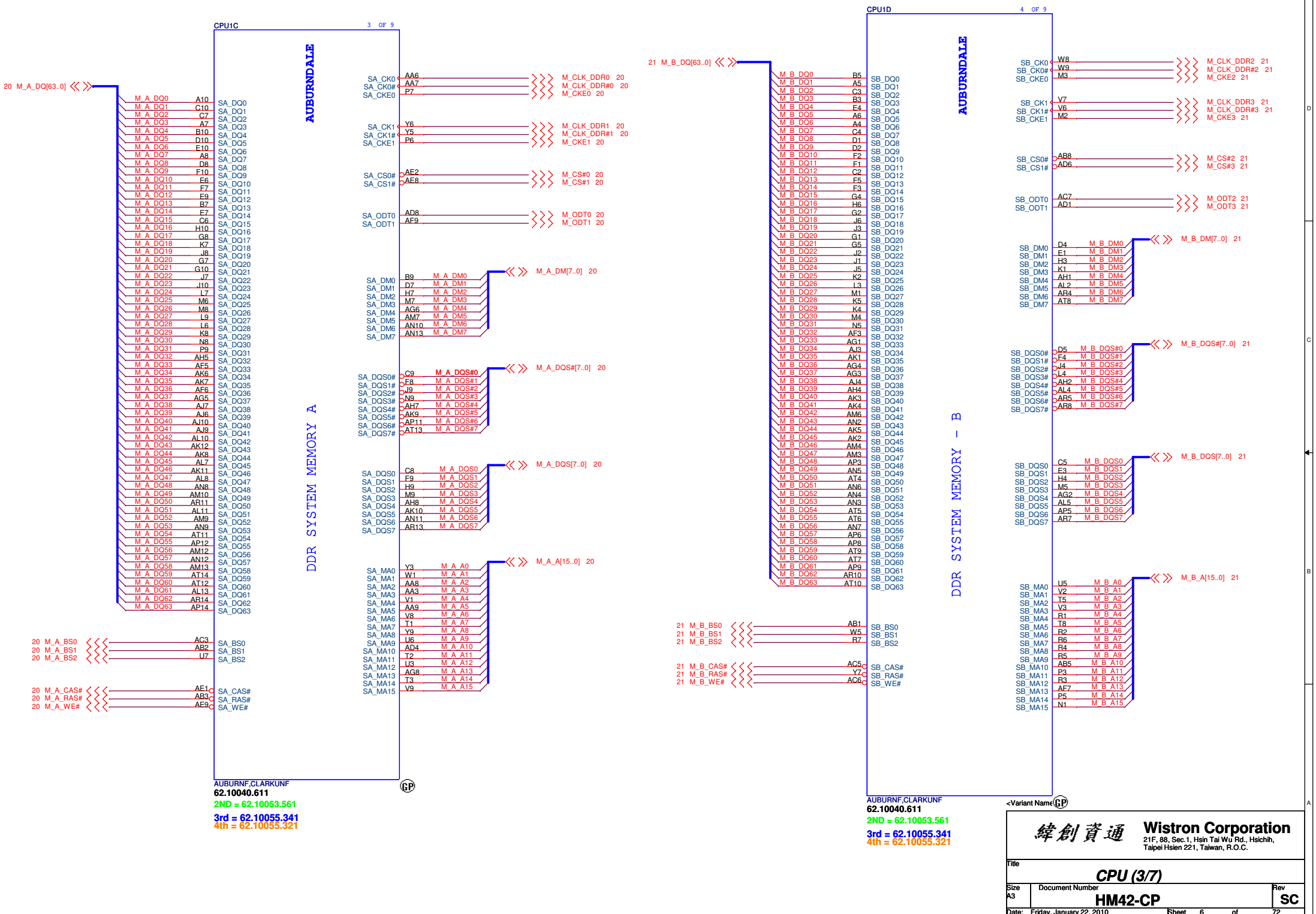
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3 OF 9
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DDR SYSTEM MEMORY A
20 M_A_DQ[63..0]
M_A_DQ0 A10
M_A_DQ1 C10
M_A_DQ2 C7
M_A_DQ3 A7
M_A_DQ4 B10
M_A_DQ5 D10
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M_A_DQ7 A8
M_A_DQ8 D8
M_A_DQ9 F10
M_A_DQ10 E6
M_A_DQ11 F7
M_A_DQ12 E9
M_A_DQ13 B7
M_A_DQ14 E7
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M_A_DQ27 L9
M_A_DQ28 L6
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SA_DQ56
SA_DQ57
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SA_DQ60
SA_DQ61
SA_DQ62
SA_DQ63
20 M_A_BS0
20 M_A_BS1
20 M_A_BS2
AC3 SA_BS0
AB2 SA_BS1
U7 SA_BS2
20 M_A_CAS#
20 M_A_RAS#
20 M_A_WE#
AE1 SA_CAS#
AB3 SA_RAS#
AE9 SA_WE#
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SA_CK0# AA7 M_CLK_DDR#0 20
SA_CKE0 P7 M_CKE0 20
SA_CK1 Y6 M_CLK_DDR1 20
SA_CK1# Y5 M_CLK_DDR#1 20
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SA_CS0# AE2 M_CS#0 20
SA_CS1# AE8 M_CS#1 20
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SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
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SA_DM4 AG6 M_A_DM4
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SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7
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SA_DQS5# AK9 M_A_DQS#5
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SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15
M_A_A[15..0] 20
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2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
CPU1D
4 OF 9
AUBURNDALE
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M_B_DQ1 A5
M_B_DQ2 C3
M_B_DQ3 B3
M_B_DQ4 E4
M_B_DQ5 A6
M_B_DQ6 A4
M_B_DQ7 C4
M_B_DQ8 D1
M_B_DQ9 D2
M_B_DQ10 F2
M_B_DQ11 F1
M_B_DQ12 C2
M_B_DQ13 F5
M_B_DQ14 F3
M_B_DQ15 G4
M_B_DQ16 H6
M_B_DQ17 G2
M_B_DQ18 J6
M_B_DQ19 J3
M_B_DQ20 G1
M_B_DQ21 G5
M_B_DQ22 J2
M_B_DQ23 J1
M_B_DQ24 J5
M_B_DQ25 K2
M_B_DQ26 L3
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M_B_DQ59 AT9
M_B_DQ60 AT7
M_B_DQ61 AP9
M_B_DQ62 AR10
M_B_DQ63 AT10
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SB_DQ1
SB_DQ2
SB_DQ3
SB_DQ4
SB_DQ5
SB_DQ6
SB_DQ7
SB_DQ8
SB_DQ9
SB_DQ10
SB_DQ11
SB_DQ12
SB_DQ13
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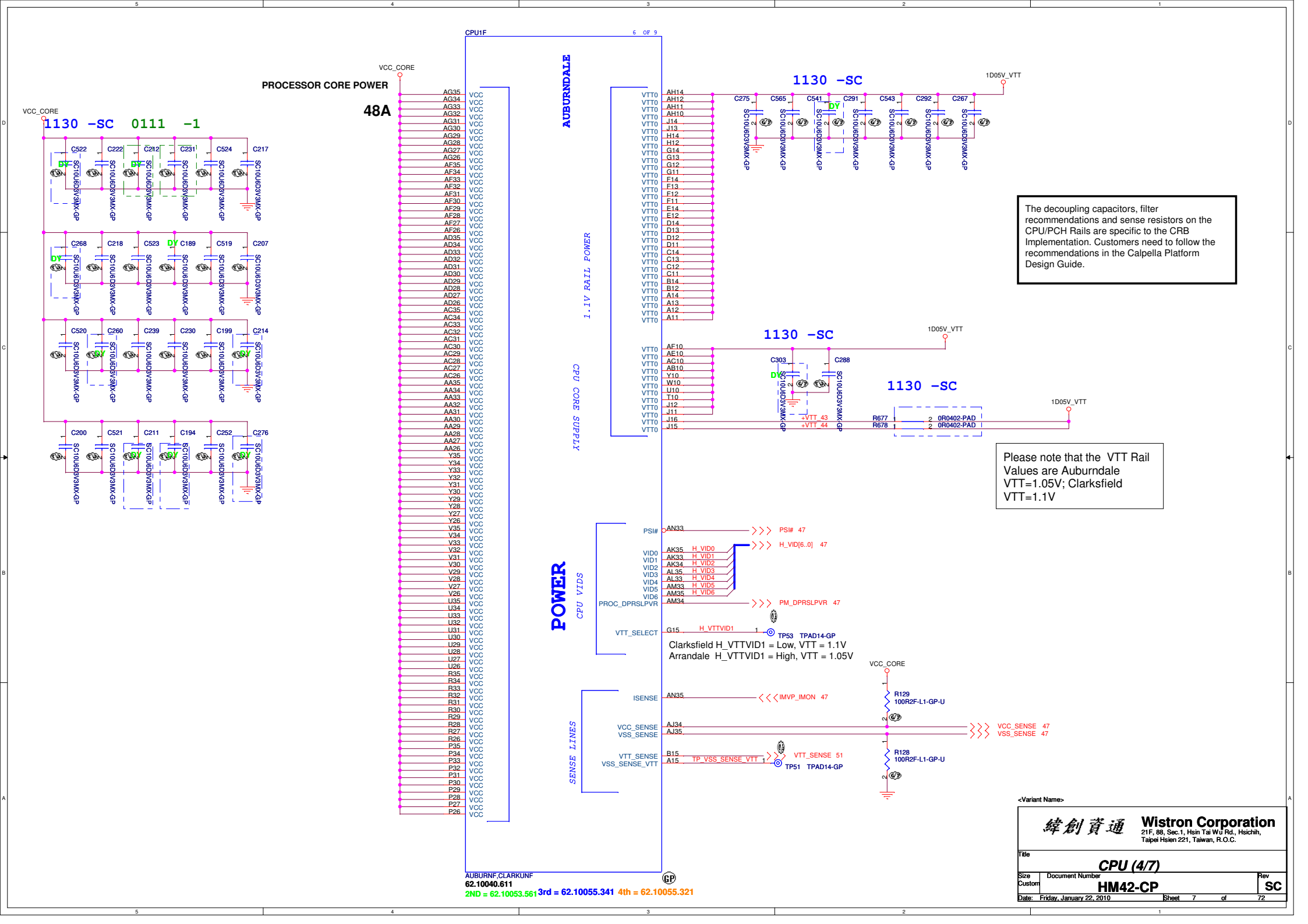
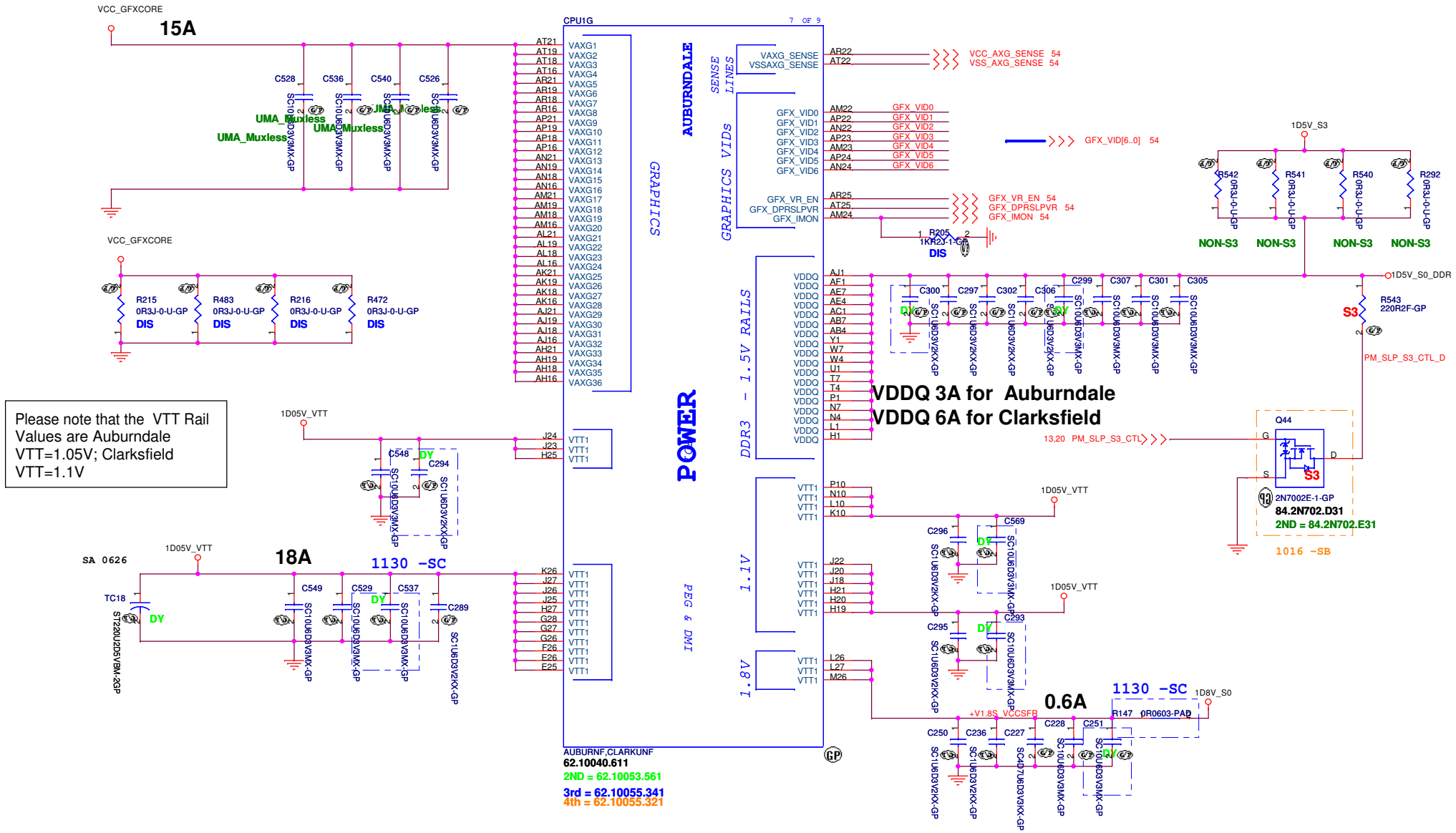
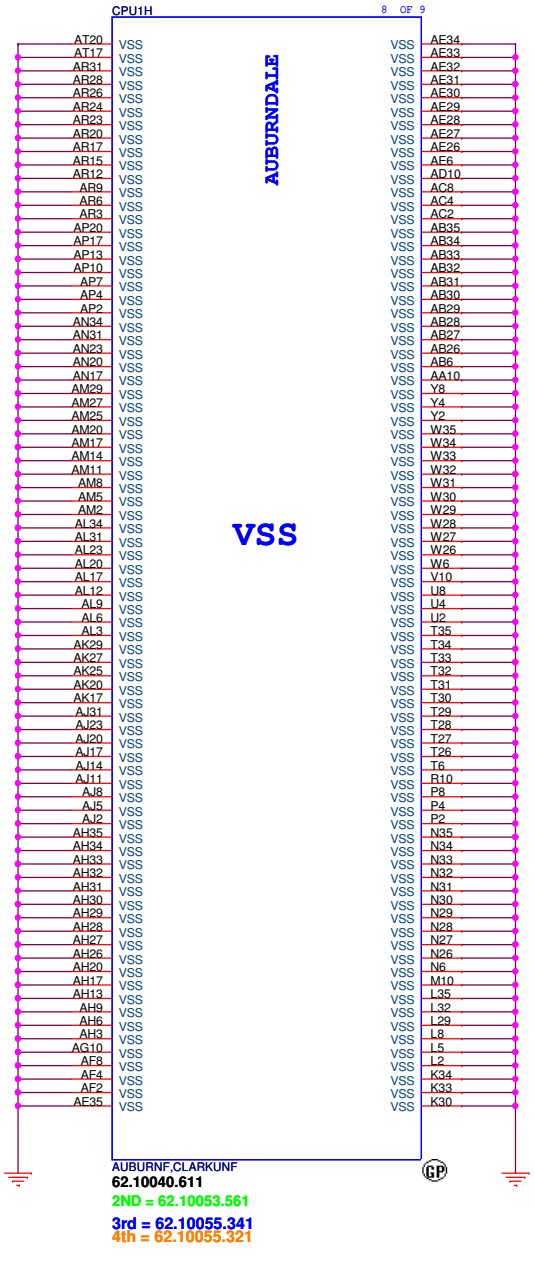
SB_DQ16
SB_DQ17
SB_DQ18
SB_DQ19
SB_DQ20
SB_DQ21
SB_DQ22
SB_DQ23
SB_DQ24
SB_DQ25
SB_DQ26
SB_DQ27
SB_DQ28
SB_DQ29
SB_DQ30
SB_DQ31
SB_DQ32
SB_DQ33
SB_DQ34
SB_DQ35
SB_DQ36
SB_DQ37
SB_DQ38
SB_DQ39
SB_DQ40
SB_DQ41
SB_DQ42
SB_DQ43
SB_DQ44
SB_DQ45
SB_DQ46
SB_DQ47
SB_DQ48
SB_DQ49
SB_DQ50
SB_DQ51
SB_DQ52
SB_DQ53
SB_DQ54
SB_DQ55
SB_DQ56
SB_DQ57
SB_DQ58
SB_DQ59
SB_DQ60
SB_DQ61
SB_DQ62
SB_DQ63
21 M_B_BS0
21 M_B_BS1
21 M_B_BS2
AB1 SB_BS0
W5 SB_BS1
R7 SB_BS2
21 M_B_CAS#
21 M_B_RAS#
21 M_B_WE#
AC5 SB_CAS#
Y7 SB_RAS#
AC6 SB_WE#
SB_CK0 W8 M_CLK_DDR2 21
SB_CK0# W9 M_CLK_DDR#2 21
SB_CKE0 M3 M_CKE2 21
SB_CK1 V7 M_CLK_DDR3 21
SB_CK1# V6 M_CLK_DDR#3 21
SB_CKE1 M2 M_CKE3 21
SB_CS0# AB8 M_CS#2 21
SB_CS1# AD6 M_CS#3 21
SB_ODT0 AC7 M_ODT2 21
SB_ODT1 AD1 M_ODT3 21
SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
SB_DM4 AH1 M_B_DM4
SB_DM5 AL2 M_B_DM5
SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7
M_B_DM[7..0] 21
SB_DQS0# D5 M_B_DQS#0
SB_DQS1# F4 M_B_DQS#1
SB_DQS2# J4 M_B_DQS#2
SB_DQS3# L4 M_B_DQS#3
SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7
M_B_DQS#[7..0] 21
SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7
M_B_DQS[7..0] 21
SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AF7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (3/7)
Size A3
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010
Sheet 6 of 72

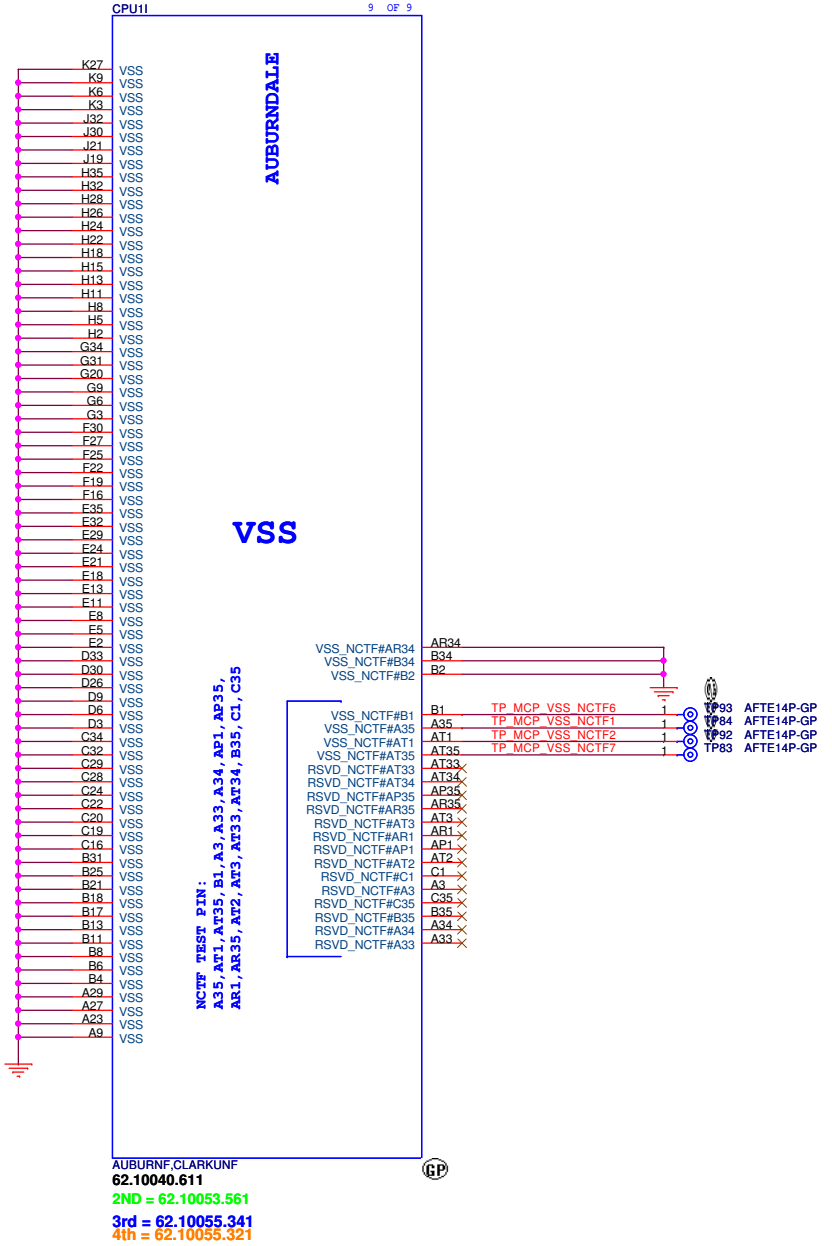

VCC_CORE
1130 -SC 0111 -1
C522 C222 C212 C231 C524 C217
C268 C218 C523 C189 C519 C207
C520 C260 C239 C230 C199 C214
C200 C521 C211 C194 C252 C276
SC10U6D3V3MX-GP
DY
PROCESSOR CORE POWER
48A
CPU1F
6 OF 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
VCC_CORE
AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
VCC
1130 -SC
1D05V_VTT
C275 C565 C541 C291 C543 C292 C267
SC10U6D3V3MX-GP
VTT0
AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11
AF10 AE10 AC10 AB10 V10 W10 U10 T10 J12 J11 J16 J15
C303 C288
+VTT_43 +VTT_44
R677 R678
0R0402-PAD
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
POWER
CPU VIDS
PSI# AN33 PSI# 47
H_VID[6..0] 47
VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6
PROC_DPRSLPVR AM34 PM_DPRSLPVR 47
VTT_SELECT G15 H_VTTVID1
TP53 TPAD14-GP
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
SENSE LINES
ISENSE AN35 IMVP_IMON 47
VCC_SENSE AJ34
VSS_SENSE AJ35
VCC_SENSE 47
VSS_SENSE 47
R129 100R2F-L1-GP-U
R128 100R2F-L1-GP-U
VTT_SENSE VSS_SENSE_VTT B15 A15 TP_VSS_SENSE_VTT
VTT_SENSE 51
TP51 TPAD14-GP
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561 3rd = 62.10055.341 4th = 62.10055.321
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (4/7)
Size Custom
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010 Sheet 7 of 72



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (5/7)***	
Size A3	Document Number **HM42-CP**	Rev **SC**
Date: Friday, January 22, 2010	Sheet 8 of 72	





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (6/7)***

Size	Document Number	Rev
A3	HM42-CP	SC

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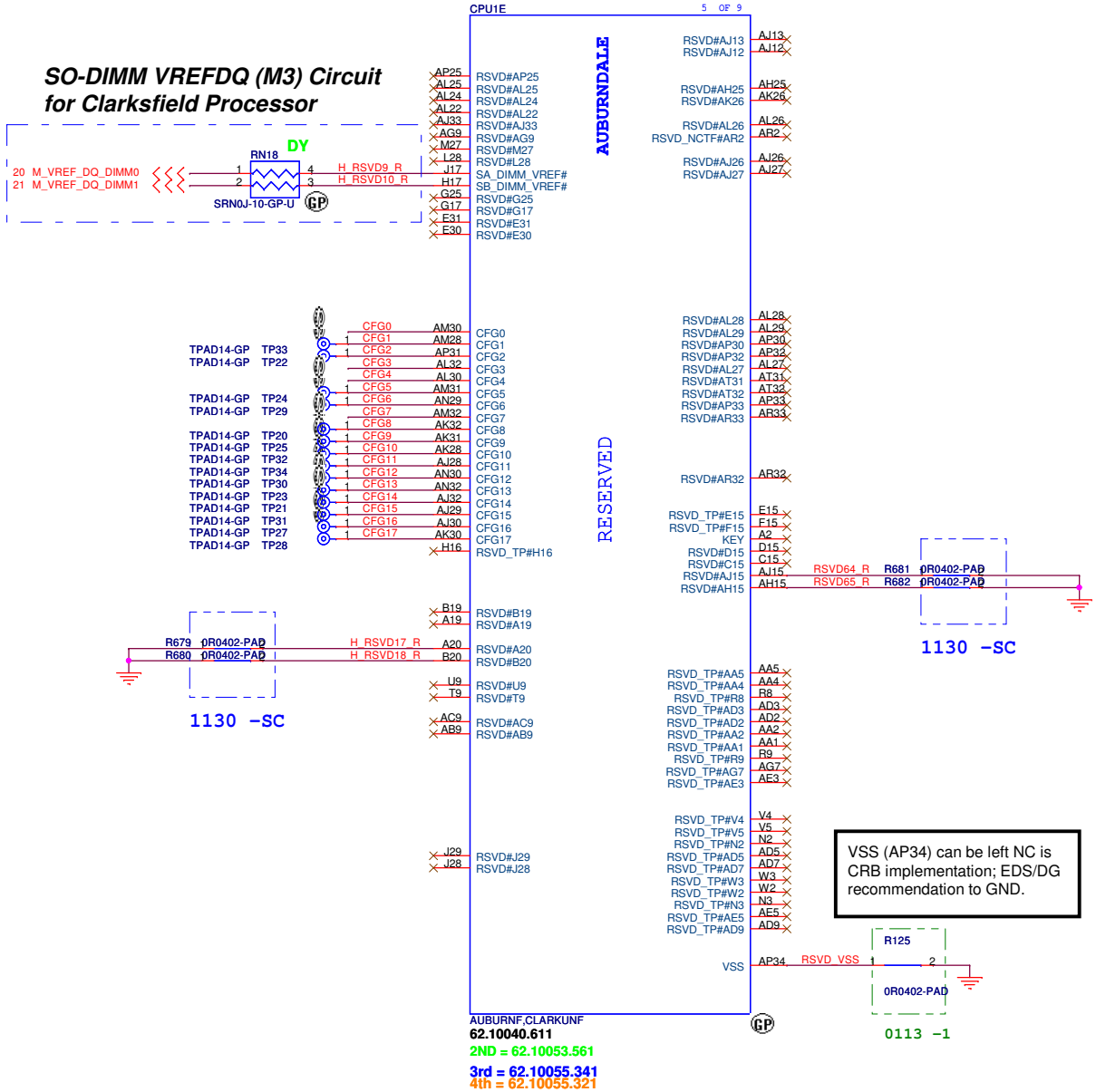
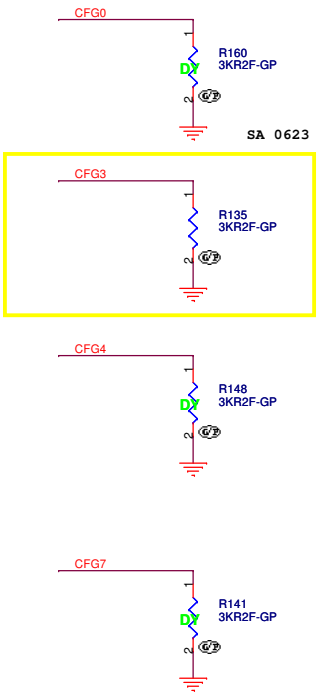




Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

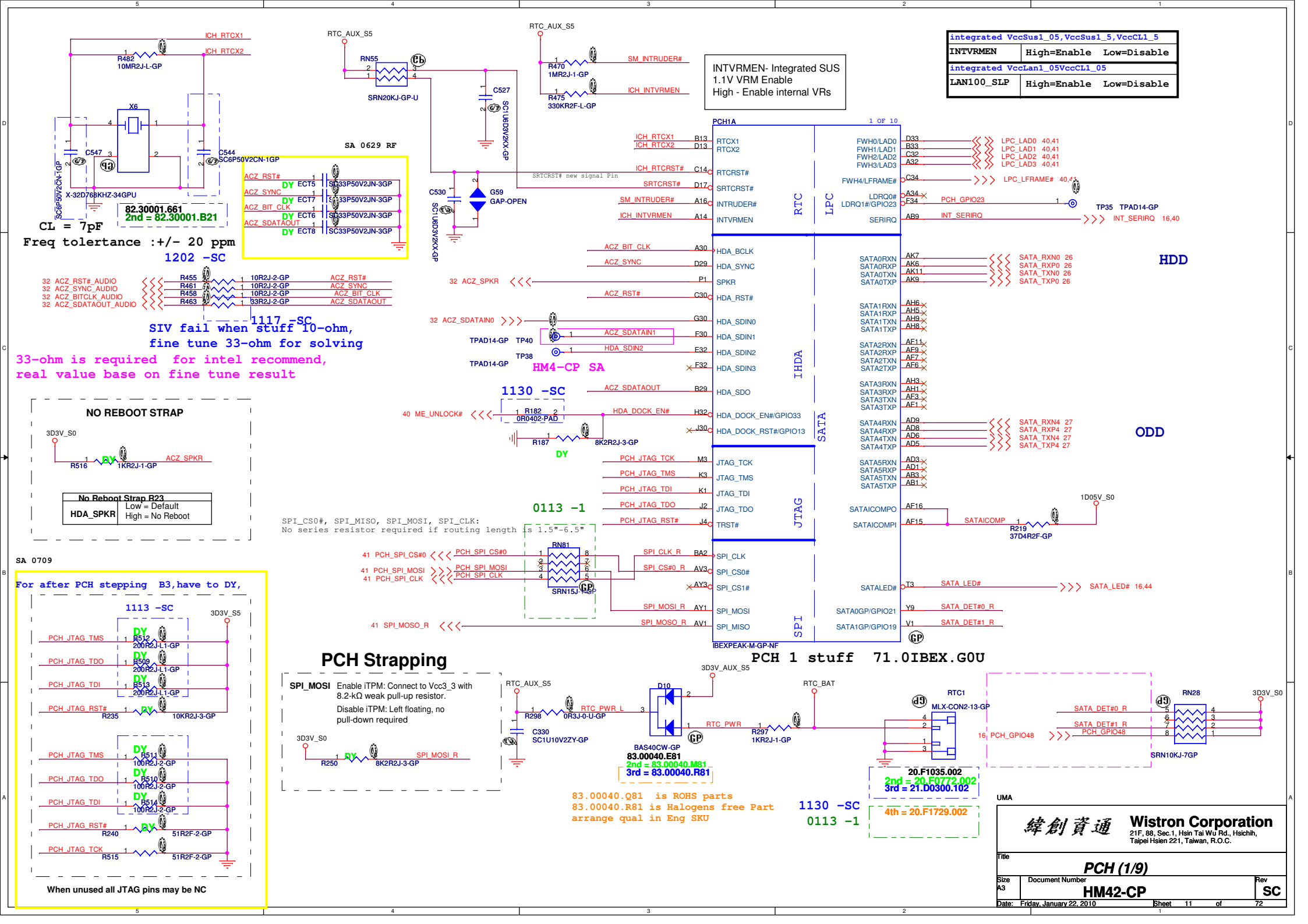
<Variant Name>

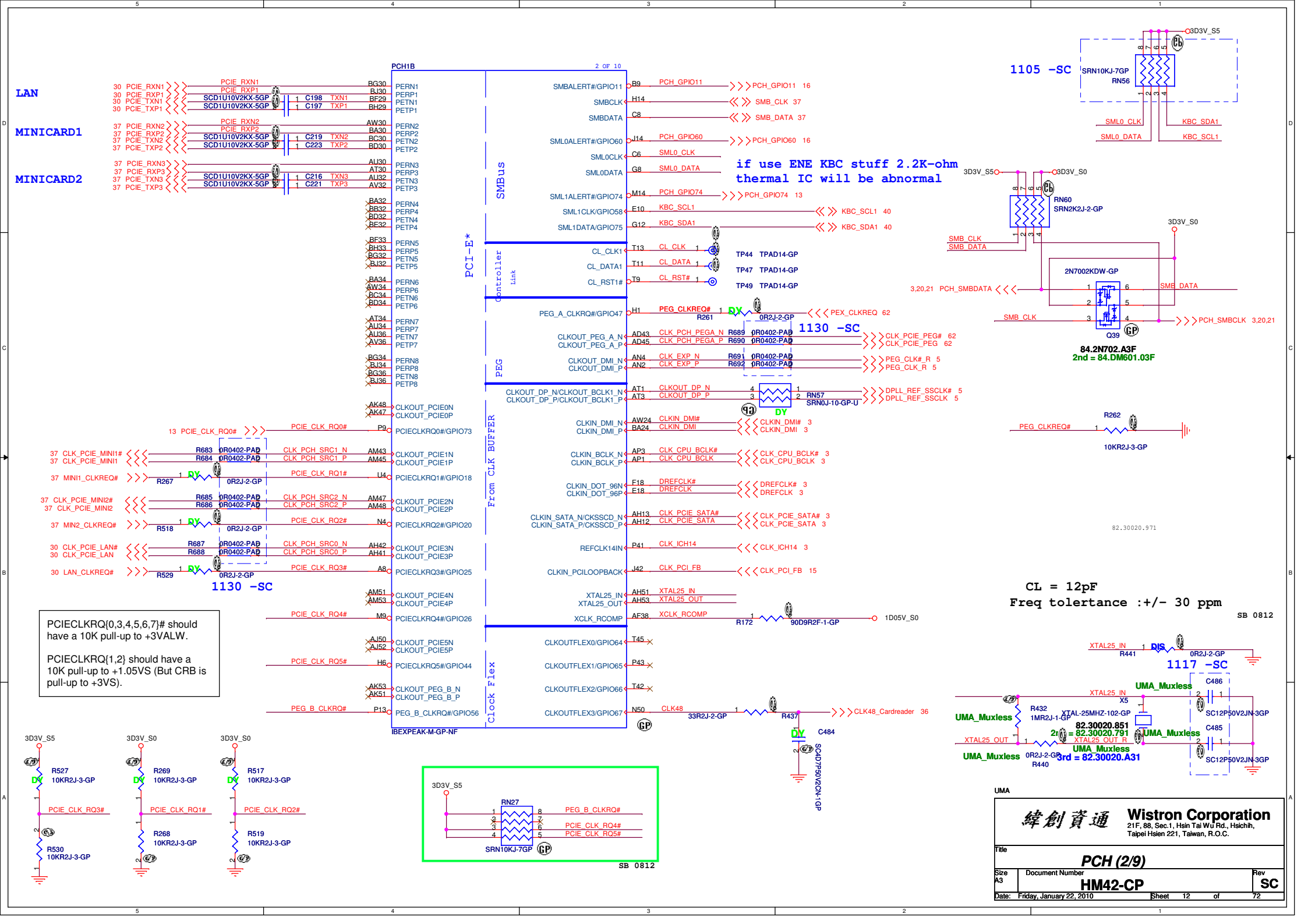
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (7/7)

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 10 of 72


integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
IBEXPEAK-M-GP-NF
SA 0629 RF
82.30001.661
2nd = 82.30001.B21
X-32D768KHZ-34GPU
CL = 7pF
Freq tolertance :+/- 20 ppm
1202 -SC
1117 -SC
SIV fail when stuff 10-ohm,
fine tune 33-ohm for solving
33-ohm is required for intel recommend,
real value base on fine tune result
HM4-CP SA
1130 -SC
0113 -1
HDD
ODD
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
SA 0709
For after PCH stepping B3,have to DY,
1113 -SC
When unused all JTAG pins may be NC
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
PCH Strapping
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
PCH 1 stuff 71.0IBEX.G0U
83.00040.Q81 is ROHS parts
83.00040.R81 is Halogens free Part
arrange qual in Eng SKU
BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
3rd = 83.00040.R81
20.F1035.002
2nd = 20.F0772.002
3rd = 21.D0300.102
4th = 20.F1729.002
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (1/9)
Size A3
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010
Sheet 11 of 72


LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
PEG
From CLK BUFFER
Clock Flex
Controller Link
IBEXPEAK-M-GP-NF
if use ENE KBC stuff 2.2K-ohm thermal IC will be abnormal
1105 -SC
1130 -SC
1130 -SC
1117 -SC
CL = 12pF
Freq tolertance :+/- 30 ppm
SB 0812
SB 0812
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
84.2N702.A3F
2nd = 84.DM601.03F
82.30020.971
82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (2/9)
HM42-CP
Rev SC
Date: Friday, January 22, 2010
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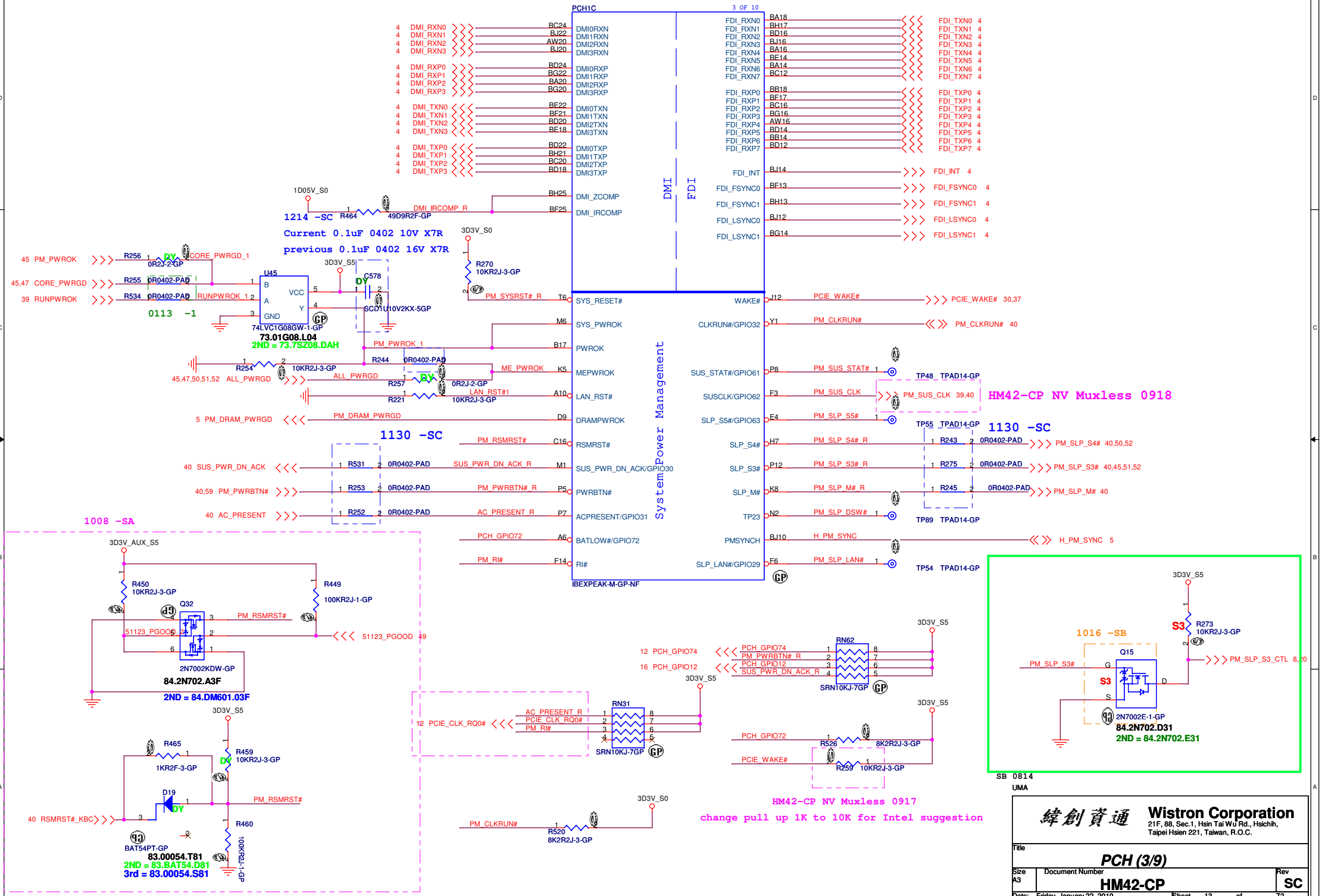

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (3/9)

Size	Document Number	Rev
A3	HM42-CP	SC

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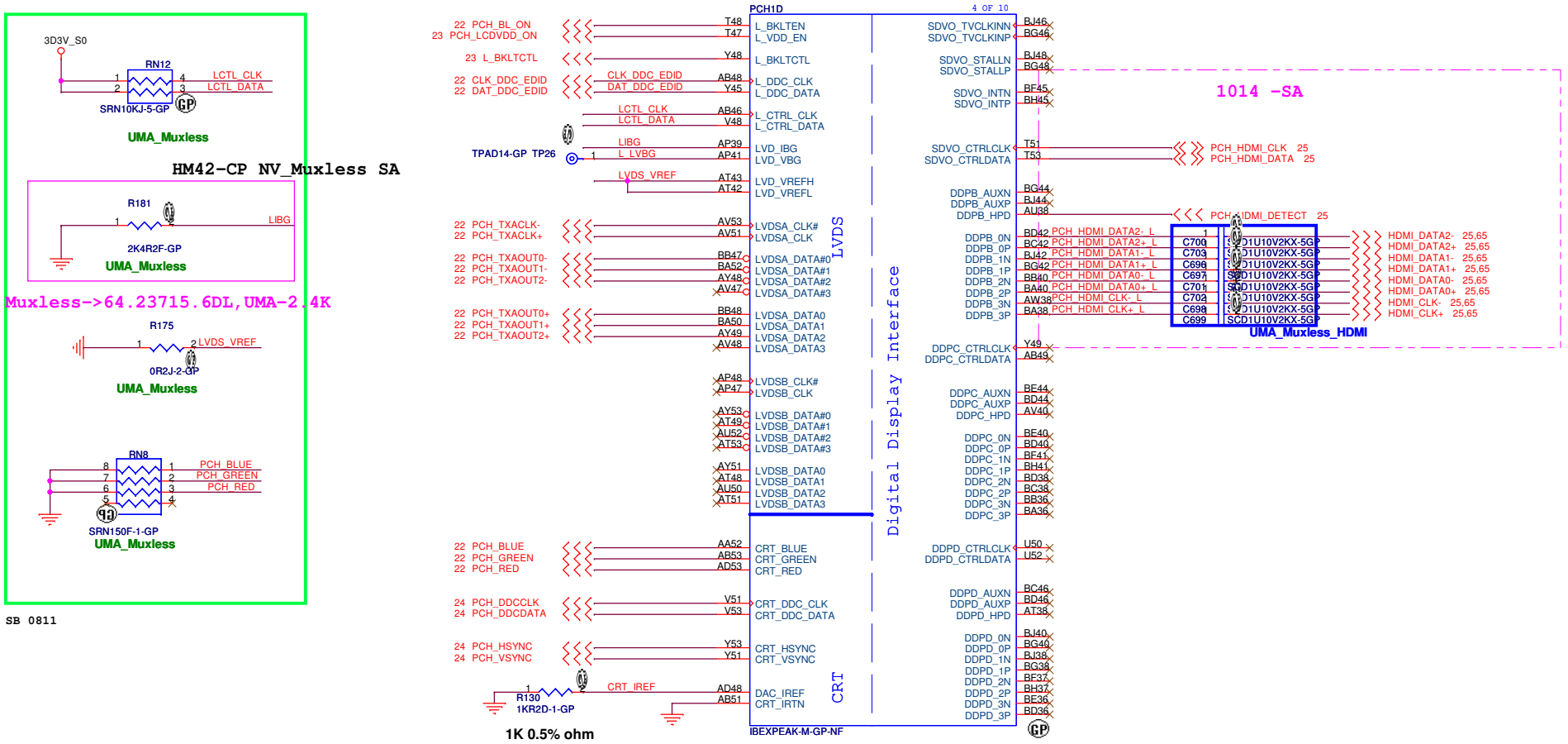

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (4/9)

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 14 of 72

HM42 NV Muxless SA 0925

1209 -SC

These pins are left as NC, because the function is disable.

HM42 NV Muxless SA 0924

1016 -SB

These pins are left as NC, because the function is disable.

PCH strapping

BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI(Default)

USE SPI

PCI_GNT#1	
1	Default (internal pull up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

41 PCLK_FWH
12 CLK_PCI_FB
40 CLK_PCI_KBC

PCH strapping

NV_CLE	DMI termination voltage
floating	internal pull-up

NV_ALE	
1	Enable Anti-Theft Tech
floating	Disable (internal pull down)

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

USB

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1(WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2(3G)
13	Cardreader

-SA 1001

HM42-CP SA

1006 -SA swap net

1204 -SC

Near R439

PCH strapping

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (5/9)

Size: A3 | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 15 of 72

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

HM42-CP_NV _Muxless SA

PCH1F

6 OF 10

BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57

MISC

CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
PECI
RCIN#
PROCPWRGD
THRMTRIP#

CPU

TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
NC_1
NC_2
NC_3
NC_4
NC_5
INIT3_3V#
TP24

VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_28
VSS_NCTF#A4
VSS_NCTF#A49
VSS_NCTF#A5
VSS_NCTF#A50
VSS_NCTF#A52
VSS_NCTF#A53
VSS_NCTF#B2
VSS_NCTF#B53
VSS_NCTF#BE1
VSS_NCTF#BE53
VSS_NCTF#BF1
VSS_NCTF#BF53
VSS_NCTF#BH1
VSS_NCTF#BH53
VSS_NCTF#BJ1
VSS_NCTF#BJ2
VSS_NCTF#BJ4
VSS_NCTF#BJ49
VSS_NCTF#BJ5
VSS_NCTF#BJ50
VSS_NCTF#BJ52
VSS_NCTF#BJ53
VSS_NCTF#D1
VSS_NCTF#D53
VSS_NCTF#E1
VSS_NCTF#E53

NCTF

RSVD

NCTF TEST PIN:
A4,A49,A5,A50,A52,A53,B2,B53,BE1,
BE53,BF1,BF53,BH1,BH53,BJ1,BJ2,BJ4,
BJ49,BJ5,BJ50,BJ52,BJ53,D1,D53,E1,E53

IBEXPEAK-M-GP-NF

PCH_GPIO0 Y3
EC_SMI# C38
PX_HDMI# D37
EC_SCI# J32
EC_SWI# F10
PCH_GPIO12 K9
PCH_GPIO15 T7
DGPU_HOLD_RST# AA2
DGPU_PWROK F38
PCH_GPIO22 Y7
PCH_GPIO24 H10
PCH_GPIO27 AB12
PCH_GPIO28 V13
STP_PCI# M11
PCH_GPIO35 V6
DGPU_PWR_EN# AB7
dGPU_PRSNT# AB13
dGPU_EDID V3
PCH_GPIO39 P3
PCH_GPIO45 H3
RST_GATE F1
PCH_GPIO48 AB6
PSW_CLR# AA4
PCH_GPIO57 F8

TPAD14-GP TP36
TPAD14-GP TP46
TPAD14-GP TP45
TPAD14-GP TP56
TPAD14-GP TP105

40 EC_SCI#
40 EC_SWI#
13 PCH_GPIO12
62 DGPU_HOLD_RST#
55,61,62 DGPU_PWROK
61 DGPU_PWR_EN#
11 PCH_GPIO48

1016 -SB
SB 0814

U2 KA20GATE 40
AM3 BCLK_CPU_N_R
AM1 BCLK_CPU_P_R
SRN0J-10-GP-U RN58
BCLK_CPU_N 5
BCLK_CPU_P 5
BG10 H_PECI 5
T1 KBRCIN# 40
BE10 H_PWRGD 5,59
BD10 PCH_THERMTRIP_R
R236 56R2J-4-GP
1D05V_VTT
R230 54D9R2F-L1-GP
PM_THRMTRIP-A# 5,45

Placed Within 2" from PCH

3D3V_S5
RN30 SRN10KJ-7GP
12 PCH_GPIO11
12 PCH_GPIO60
PCH_GPIO28
PCH_GPIO45 R508 8K2R2J-3-GP
SB 0819
PCH_GPIO15 R266 1KR2J-1-GP

PSW_CLR#
GAP-OPEN
G111

3D3V_S0
RN29 SRN10KJ-7GP
11,44 SATA_LED#
11,40 INT_SERIRQ
PCH_GPIO39
PSW_CLR#

SB 0722
AFTE14P-GP TP80
AFTE14P-GP TP88
PCH_TP95
PCH_TP96
AFTE14P-GP TP87
PCH_TP97
AFTE14P-GP TP82
PCH_TP98

RP1 SRN10KJ-L3-GP
STP_PCI#
PCH_GPIO22
PCH_GPIO0
dGPU_EDID
EC_SMI#
EC_SCI#
PX_HDMI#

PCH_GPIO35 R265 10KR2J-3-GP

1D5V_S3
R279 1KR2F-3-GP
DDR3_DRAMRST# 20,21
0121 -1
NON-S3
R278 0R2J-2-GP
2ND = 84.2N702.E31
84.2N702.D31
2N7002E-1-GP
Q14
R272 10KR2F-2-GP
RST_GATE
C298 SCD047U25V2KX-GP
SM_DRAMRST# 5
R277 100KR2F-L1-GP
TP52 TPAD14-GP

HM42-CP_NV _Muxless SA

3D3V_S0
R263 10KR2J-3-GP
DY
DGPU_PWR_EN#
R264 10KR2J-3-GP

3D3V_S0
R532 10KR2J-3-GP
DY
DGPU_HOLD_RST#
R533 10KR2J-3-GP

H: No SG function
L: SG Support

3D3V_S0
DIS_UMA
R224 10KR2J-3-GP
dGPU_PRSNT#
R225 10KR2J-3-GP
Muxless

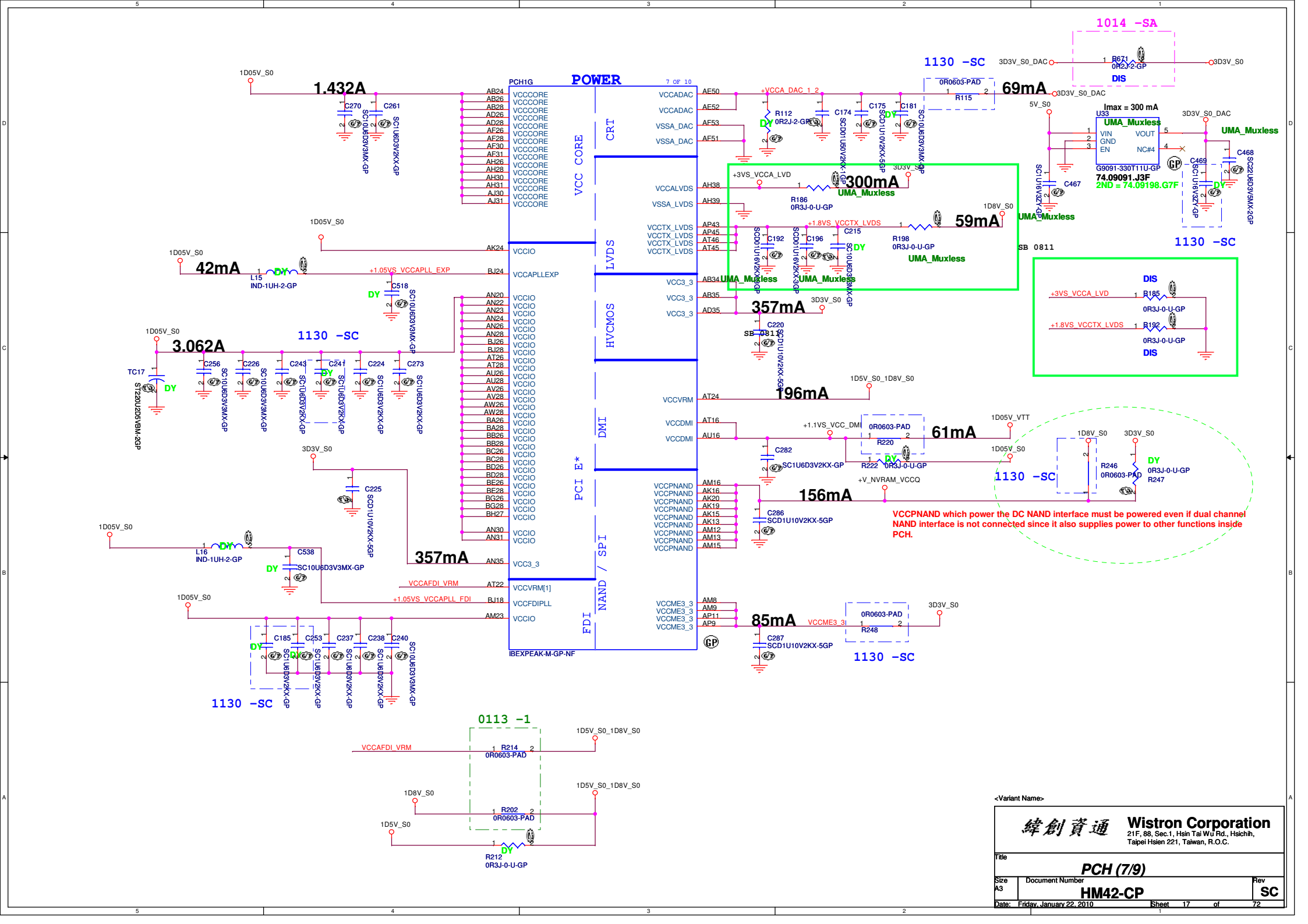
SB 0812

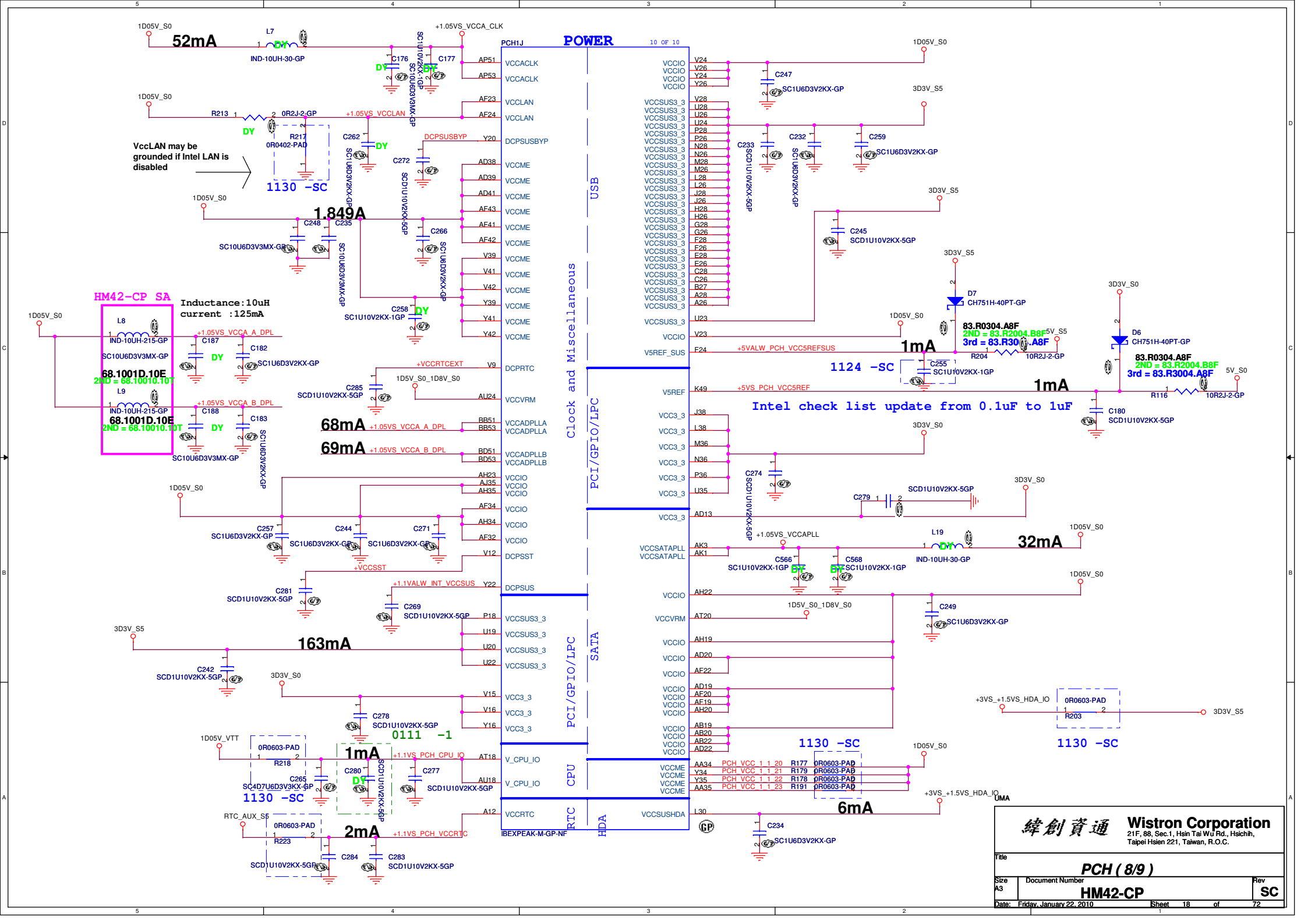
3D3V_S5
UMA_Muxless
R239 10KR2J-3-GP
PCH_GPIO57
R238 10KR2J-3-GP
DIS
UMA_DISCRETE#
Optimus: HIGH
UMA: HIGH
DIS ONLY: LOW

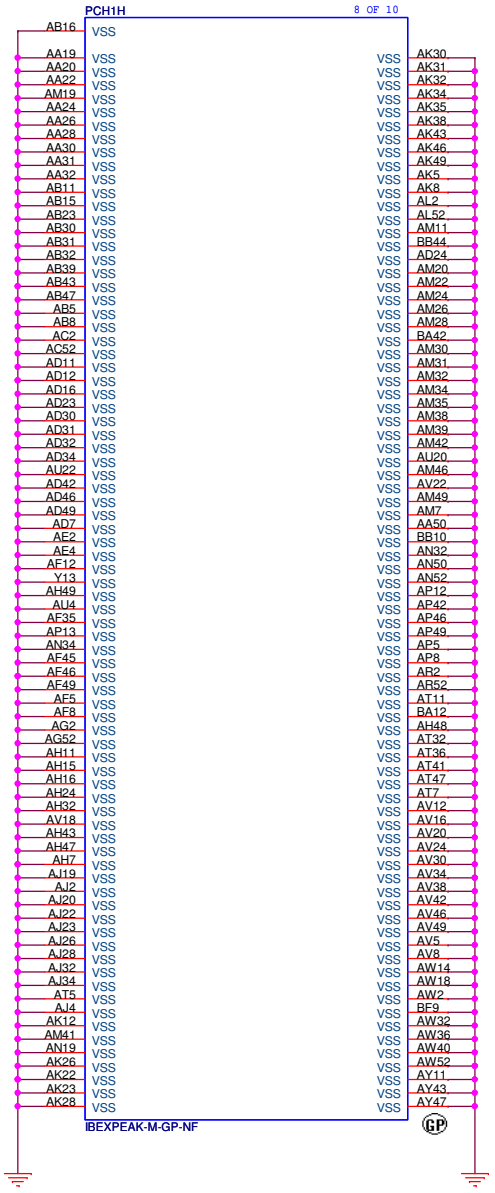
UMA

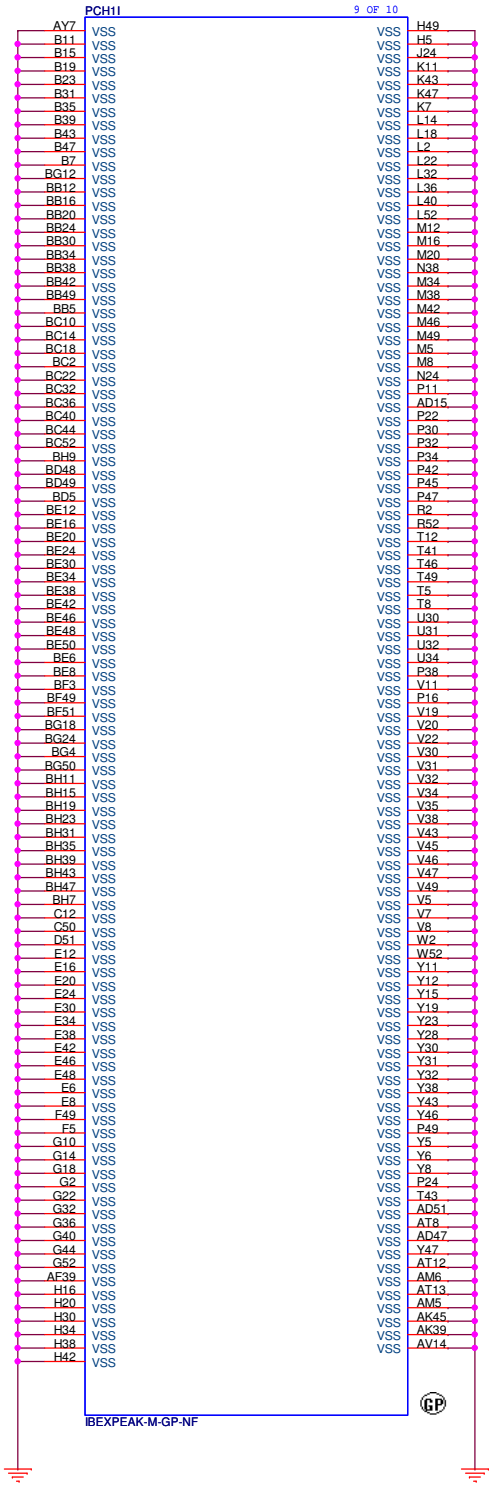
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (6/9)
Size: A3
Document Number: HM42-CP
Rev: SC
Date: Friday, January 22, 2010
Sheet 16 of 72

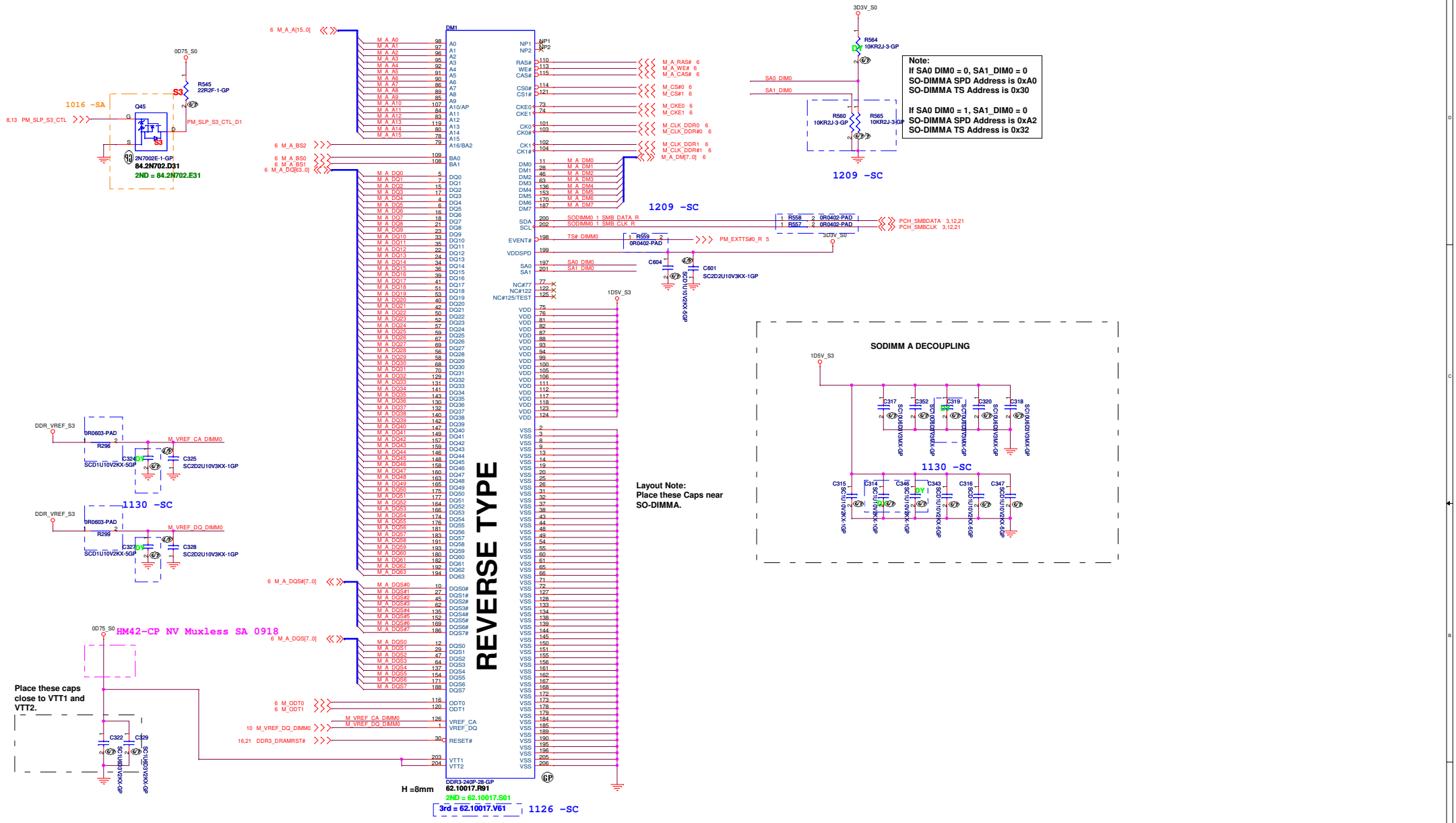

POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
357mA
1014 -SA
1130 -SC
0113 -1
SB 0811
UMA_Muxless
DIS
DY
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
IBEXPEAK-M-GP-NF
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (7/9)
Size A3
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010
Sheet 17 of 72


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
HM42-CP SA
Inductance:10uH
current :125mA
68.1001D.10E
2ND = 68.10010.10T
52mA
1.849A
68mA
69mA
163mA
1mA
2mA
6mA
32mA
1130 -SC
0111 -1
Intel check list update from 0.1uF to 1uF
VccLAN may be grounded if Intel LAN is disabled
83.R0304.A8F
2ND = 83.R2004.B8F
3rd = 83.R3004.A8F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010
Sheet 18 of 72


PCH1H
8 OF 10
IBEXPEAK-M-GP-NF


PCH1I
9 OF 10
IBEXPEAK-M-GP-NF

<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (9/9)
Size
A3
Document Number
HM42-CP
Rev
SC
Date: Friday, January 22, 2010
Sheet 19 of 72



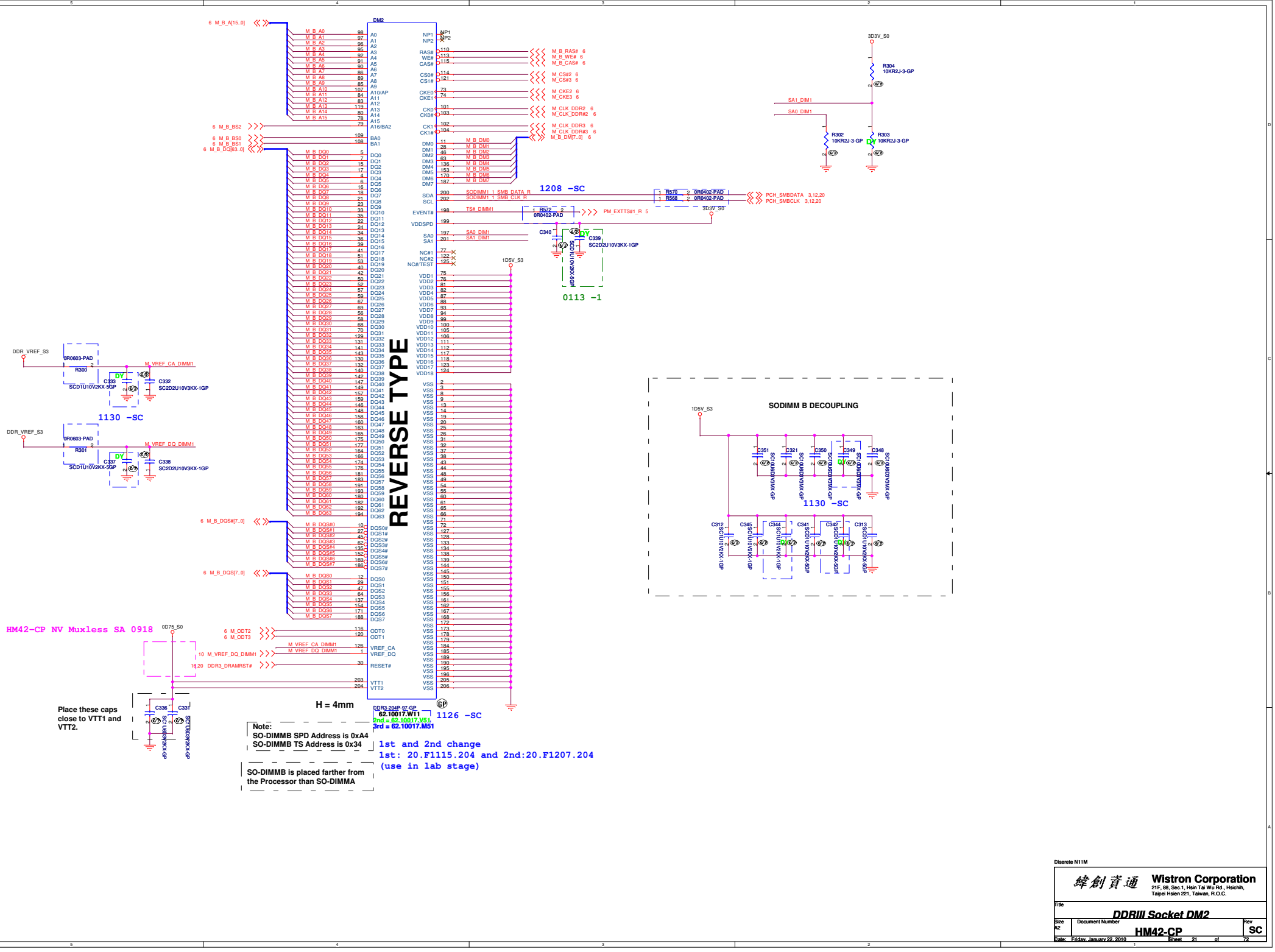
Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII Socket DM1

Size	Document Number	Rev
A2	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 20 of 72



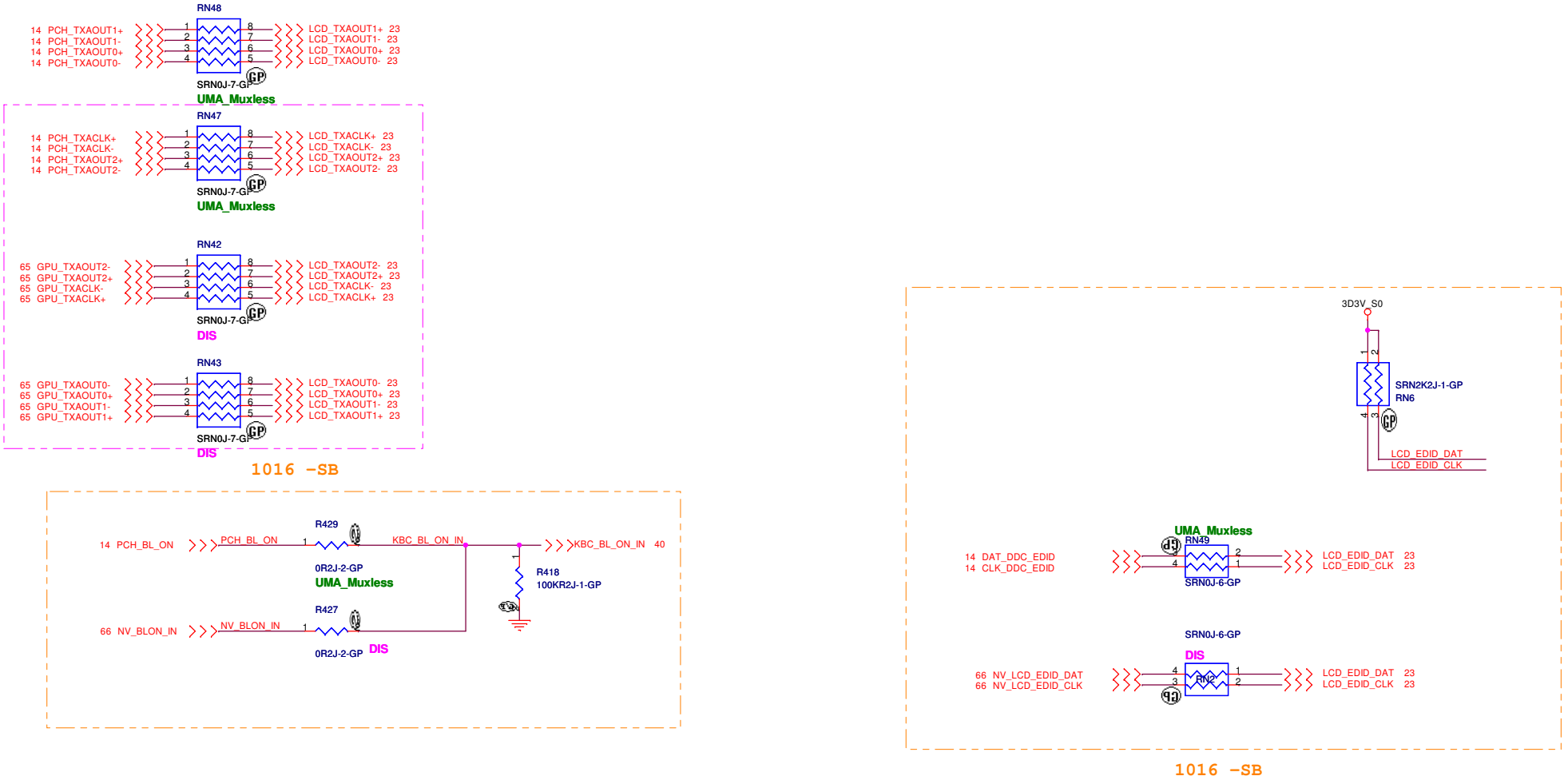
Diserete N11M

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII Socket DM2

Size	Document Number	Rev
A2	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 21 of 72



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

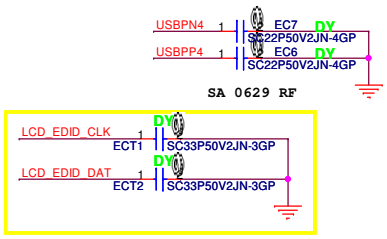
Title: ***Function***

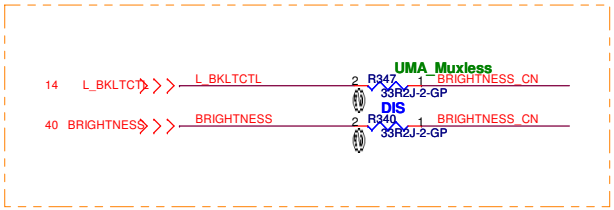
Size	Document Number	Rev
A3	HM42-CP	SC

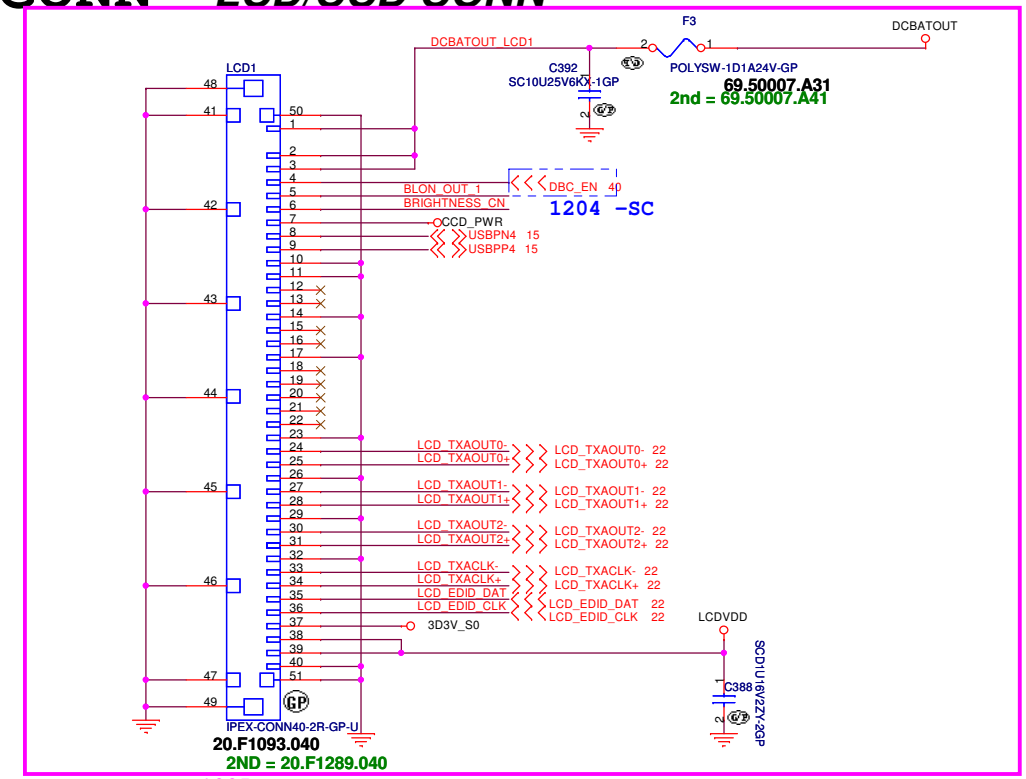
Date: Friday, January 22, 2010 Sheet 22 of 72

LCD/INVERTER/CCD CONN

LCD/CCD CONN

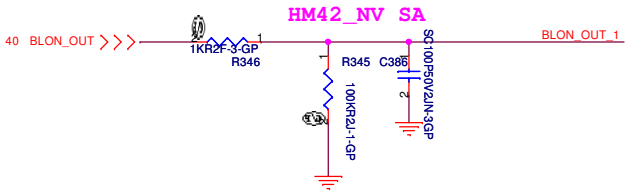


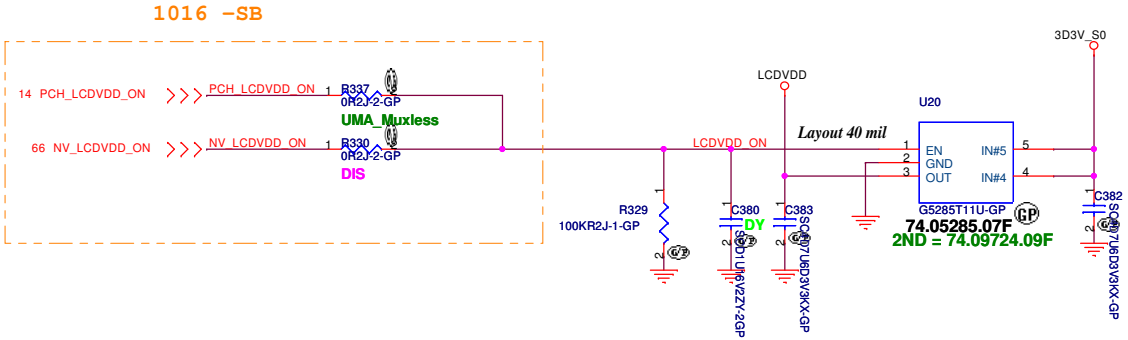




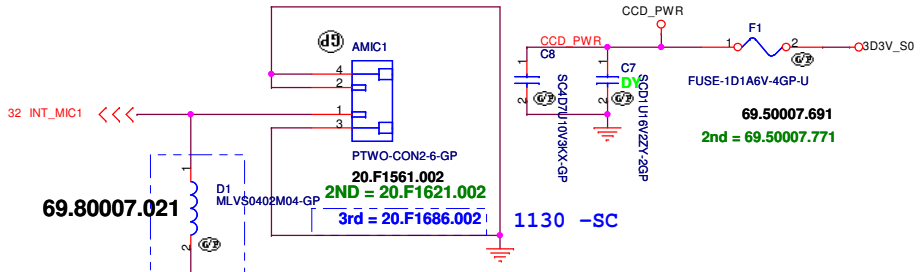
1005 -SA

define same as SJM50-PU,can use SJM50 Cable





Internal Mic



Pin 1- >right side

1209 -SC 20.F1240.002 Pin1->left side

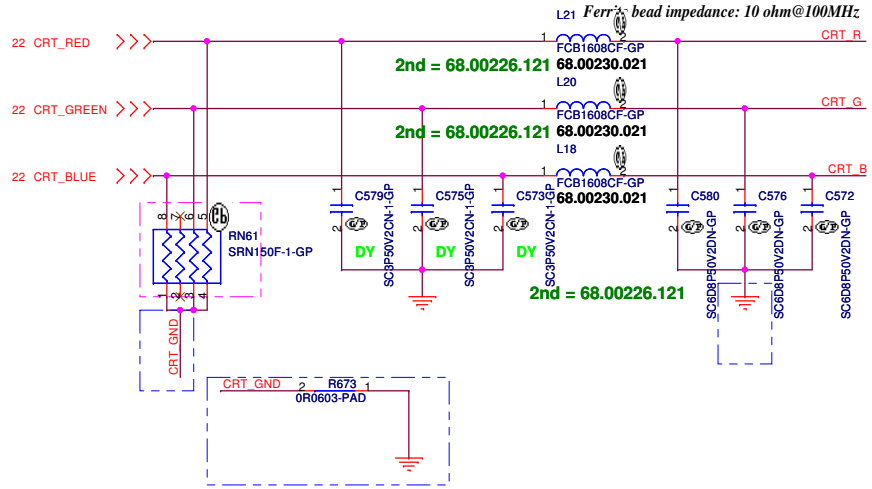
request by EMI Aaron

same as JV70-CP

Diserete N11M

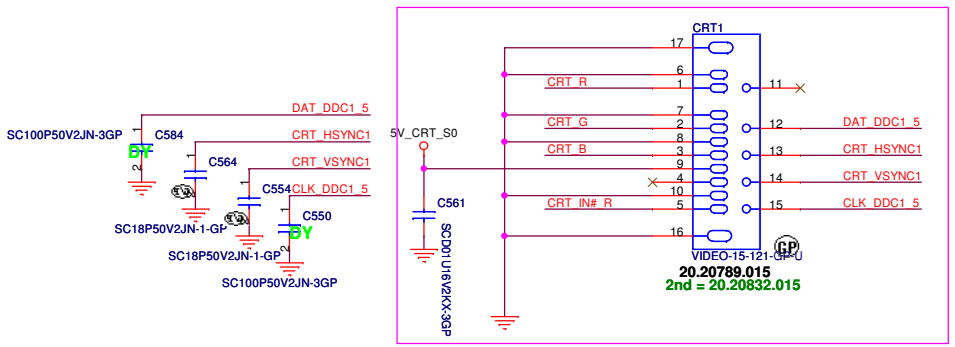
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 23 of 72	

Layout Note:
Place these resistors close to the CRT-out connector

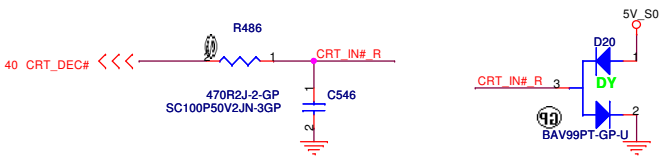


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

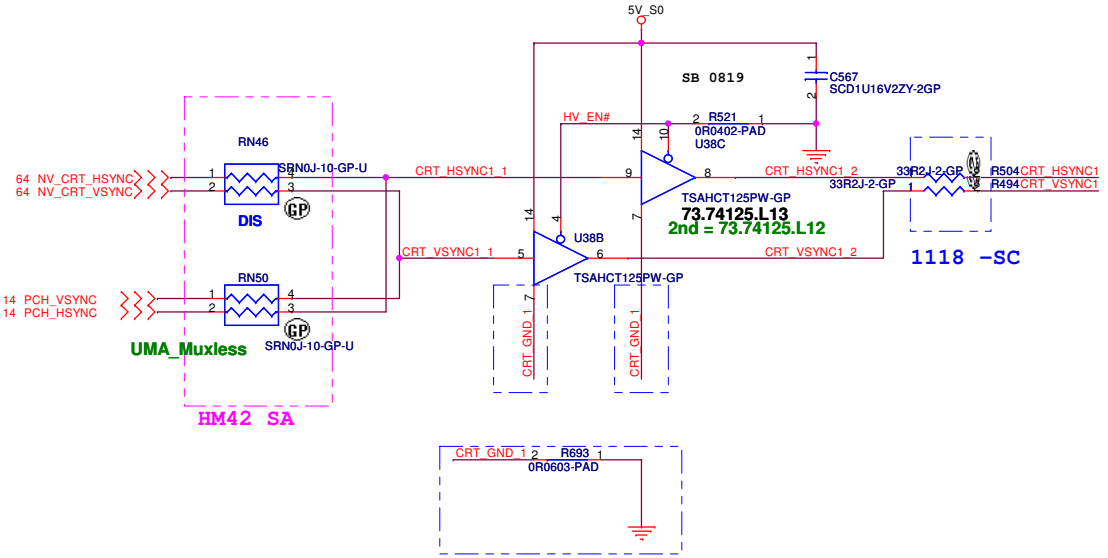
CRT I/F & CONNECTOR



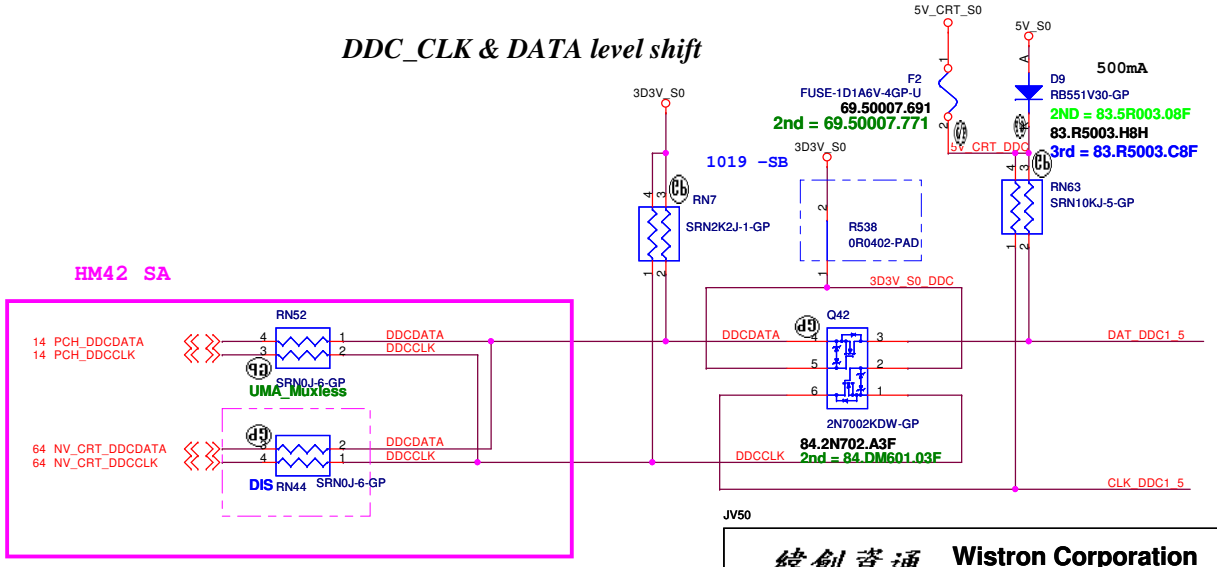
HM42 CP NV Muxless



Hsync & Vsync level shift



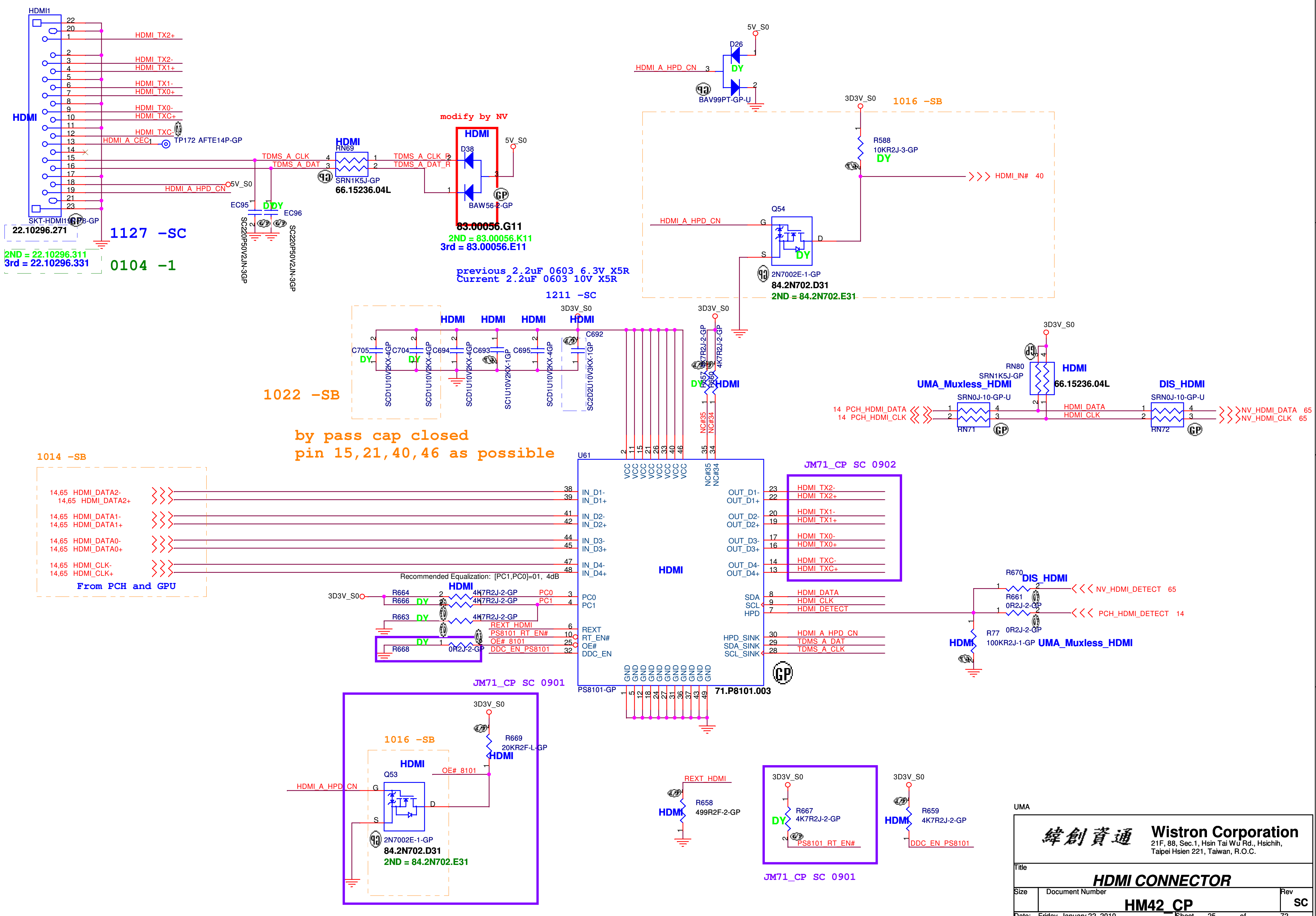
DDC_CLK & DATA level shift



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CRT CONN**		
Size	Document Number: **HM42-CP**	Rev: SC
Date: Friday, January 22, 2010	Sheet 24 of 72	

6 1 7 2 8 3 9 4 10 5



HDMI1
HDMI
SKT-HDMI19P-8-GP
22.10296.271
2ND = 22.10296.311
3rd = 22.10296.331
1127 -SC
0104 -1
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TP172 AFTE14P-GP
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_HPD_CN
5V_S0
EC95
EC96
SC220P50V2JN-3GP
RN69
SRN1K5J-GP
66.15236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
modify by NV
D38
BAW56-2-GP
83.00056.G11
2ND = 83.00056.K11
3rd = 83.00056.E11
D26
BAV99PT-GP-U
DY
3D3V_S0
1016 -SB
R588
10KR2J-3-GP
HDMI_IN# 40
Q54
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
previous 2.2uF 0603 6.3V X5R
Current 2.2uF 0603 10V X5R
1211 -SC
C705
C704
C694
C693
C695
C692
SCD1U10V2KX-4GP
SC1U10V2KX-1GP
SC2D2U10V3KX-1GP
1022 -SB
by pass cap closed
pin 15,21,40,46 as possible
R657
R660
4K7R2J-2-GP
NC#35
NC#34
RN80
SRN1K5J-GP
66.15236.04L
UMA_Muxless_HDMI
DIS_HDMI
SRN0J-10-GP-U
RN71
RN72
14 PCH_HDMI_DATA
14 PCH_HDMI_CLK
HDMI_DATA
HDMI_CLK
NV_HDMI_DATA 65
NV_HDMI_CLK 65
1014 -SB
14,65 HDMI_DATA2-
14,65 HDMI_DATA2+
14,65 HDMI_DATA1-
14,65 HDMI_DATA1+
14,65 HDMI_DATA0-
14,65 HDMI_DATA0+
14,65 HDMI_CLK-
14,65 HDMI_CLK+
From PCH and GPU
U61
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
Recommended Equalization: [PC1,PC0]=01, 4dB
PC0
PC1
REXT
RT_EN#
OE#
DDC_EN
SDA
SCL
HPD
HPD_SINK
SDA_SINK
SCL_SINK
HDMI_DETECT
PS8101-GP
71.P8101.003
JM71_CP SC 0902
R664
R666
R663
R668
0R2J-2-GP
REXT_HDMI
PS8101_RT_EN#
OE# 8101
DDC_EN_PS8101
R670
R661
NV_HDMI_DETECT 65
PCH_HDMI_DETECT 14
R77
100KR2J-1-GP
JM71_CP SC 0901
R669
20KR2F-L-GP
Q53
R658
499R2F-2-GP
R667
R659

UMA

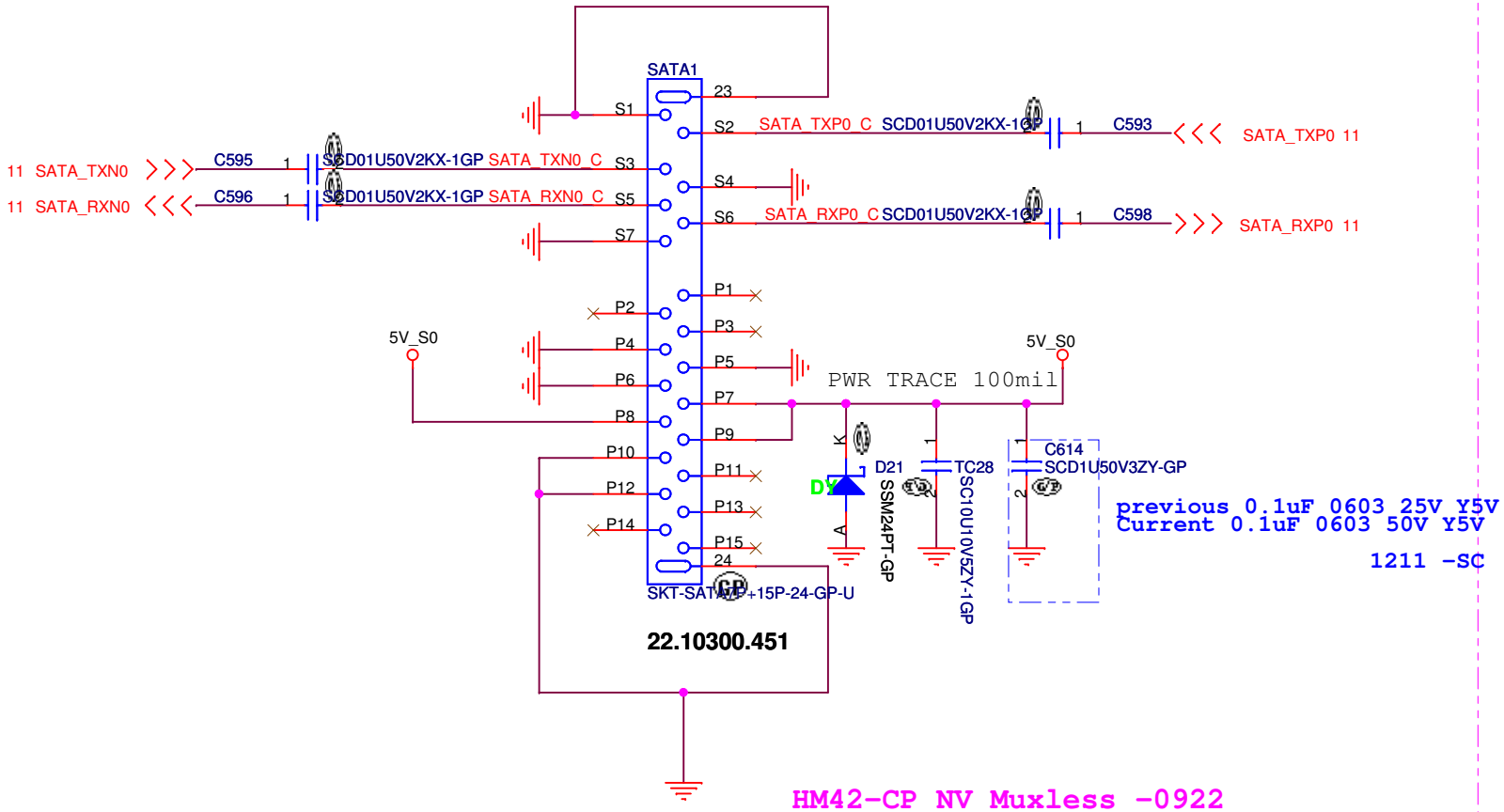
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI CONNECTOR**

Size | Document Number: HM42_CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 25 of 72

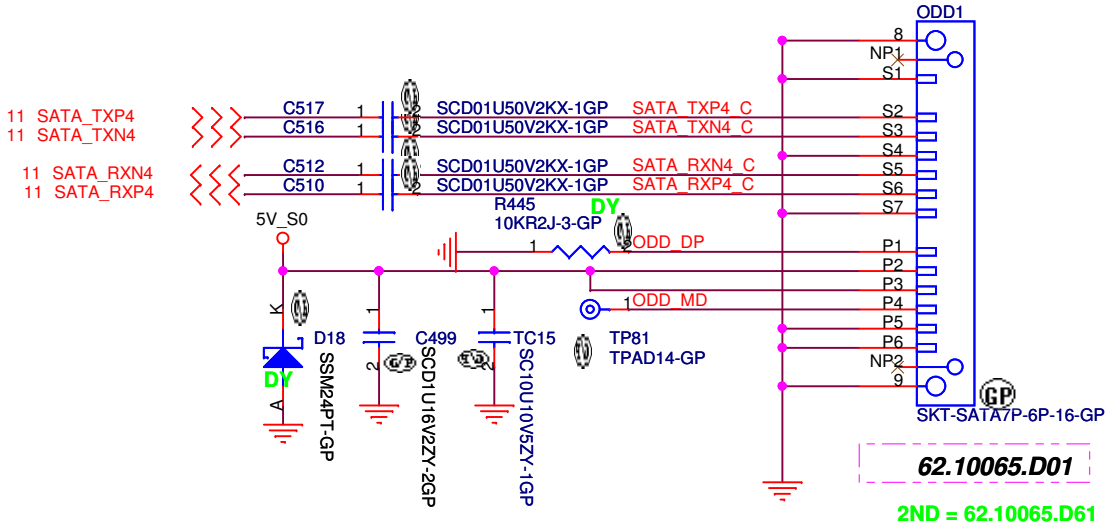
SATA Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **HM42-CP**	Rev SC
Date: Friday, January 22, 2010	Sheet 26 of 72	

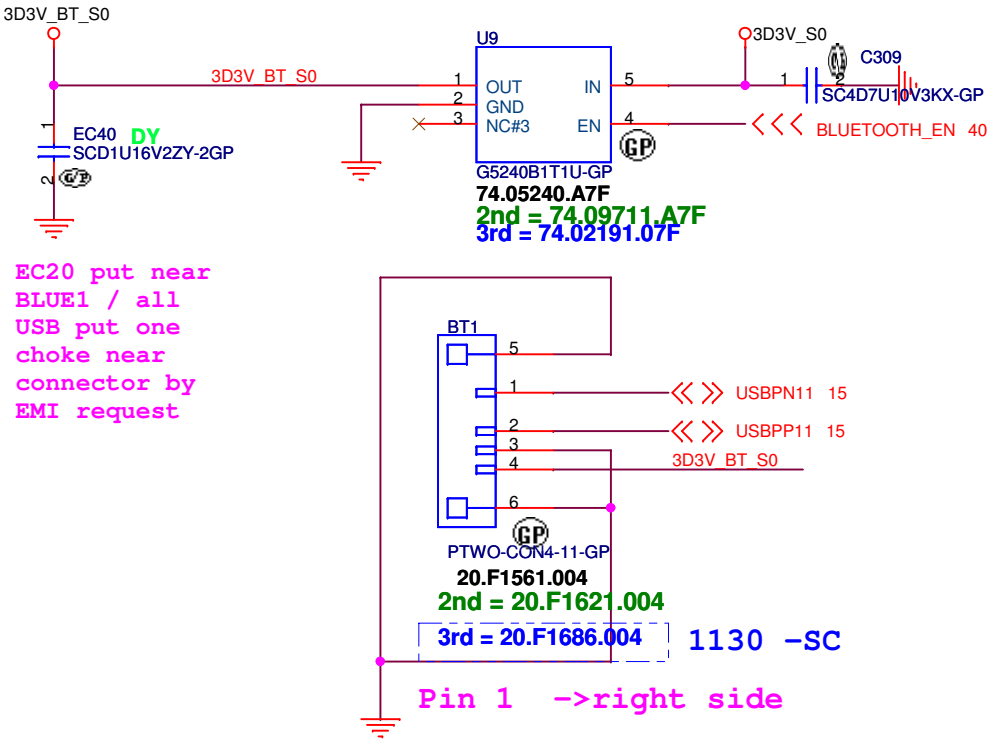
ODD Connector



UMA

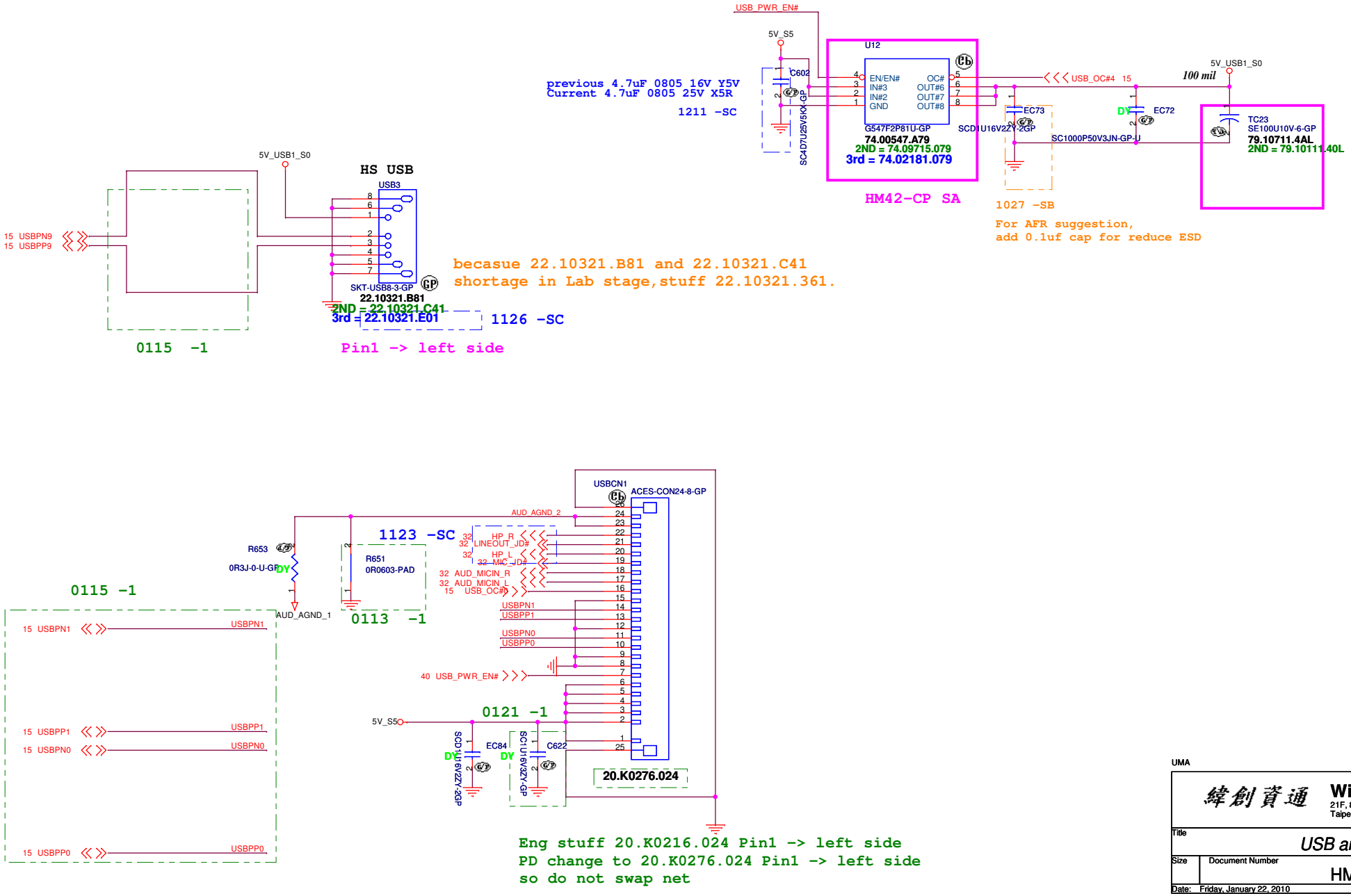
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ODD***	
Size	Document Number **HM42-CP**	Rev SC
Date: Friday, January 22, 2010	Sheet 27 of 72	

BLUETOOTH MODULE



JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 28 of 72	



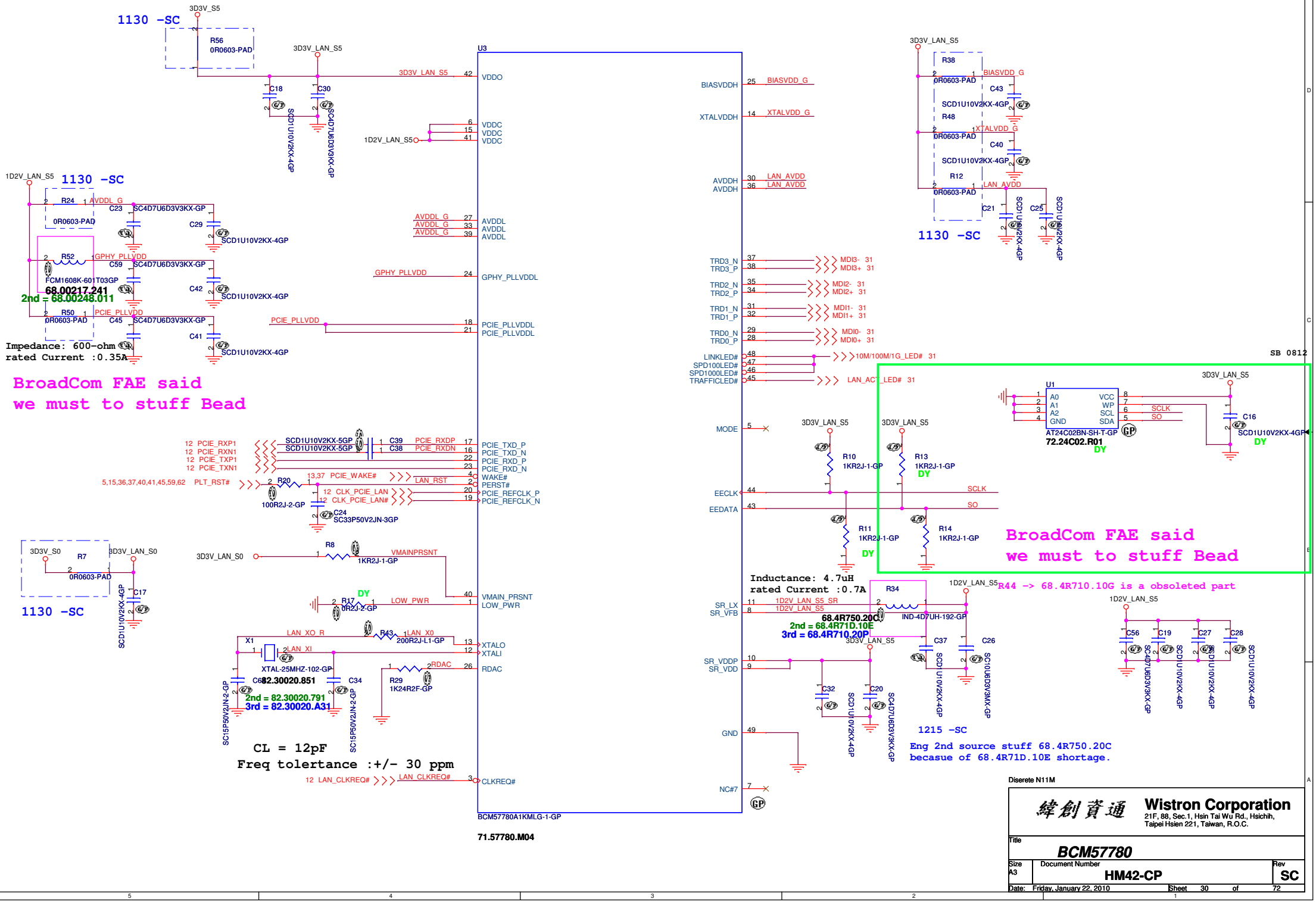
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and Audio CONN

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 29 of 72



Diserete N11M

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BCM57780***	
Size A3	Document Number **HM42-CP**	Rev **SC**
Date: Friday, January 22, 2010	Sheet 30 of 72	

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector

GIGA Lan Transformer

XF2

30 MDI1+ 1 12 RJ45_3
XRF_TDC1 3 10 MCT2
30 MDI1- 2 11 RJ45_6
30 MDI0- 5 8 RJ45_2
XRF_TDC2 4 9 MCT1
30 MDI0+ 6 7 RJ45_1

XFORM-276-GP-U
68.68160.30B
2ND = 68.HD081.30B
3rd = 68.0NS14.301

XF1

30 MDI3+ 1 12 RJ45_7
XRF_TDC3 3 10 MCT4
30 MDI3- 2 11 RJ45_8
30 MDI2- 5 8 RJ45_5
XRF_TDC4 4 9 MCT3
30 MDI2+ 6 7 RJ45_4

XFORM-276-GP-U
68.68160.30B
2ND = 68.HD081.30B
3rd = 68.0NS14.301

C14 DY SCD1U10V2KX-4GP
C15 DY SCD1U10V2KX-4GP
C12 DY SCD1U10V2KX-4GP
C13 DY SCD1U10V2KX-4GP

RJ45

30 10M/100M/1G_LED#
CONN_PWR
RJ45_1
RJ45_2
RJ45_3
RJ45_4
RJ45_5
RJ45_6
RJ45_7
RJ45_8
CONN_PWR2
30 LAN_ACT_LED#

RJ45-13P-5-GP

22.10177.C01
2ND = 22.10177.B51
3rd = 22.10177.C21
4th = 22.10177.B81
5th = 22.10177.H31

2 LED LAYOUT

13 12

NODE	COLOR
12(+) 13(-)	YELLOW

3 LED LAYOUT

11 ORANGE 9 GREEN 10

NODE	COLOR
9(-) 10(+)	GREEN
11(-) 10(+)	ORANGE

3D3V_S5

RN36 SRN470J-4-GP-U

CONN_PWR2
CONN_PWR

SB 1208

EC52 SC100P50V2JN-3GP
EC53 DY SC100P50V2JN-3GP

HM42 CP NV Muxless SA

MCT1
MCT2
MCT3
MCT4

RN39 SRN75J-1-GP

MCT_R

C385 SC1KP2KV6KX-GP

LAN_ACT_LED#
10M/100M/1G_LED#

C368 SC1KP50V2KX-1GP DY
C389 SC1KP50V2KX-1GP DY

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

Size	Document Number	Rev
A3	HM42-CP	SC

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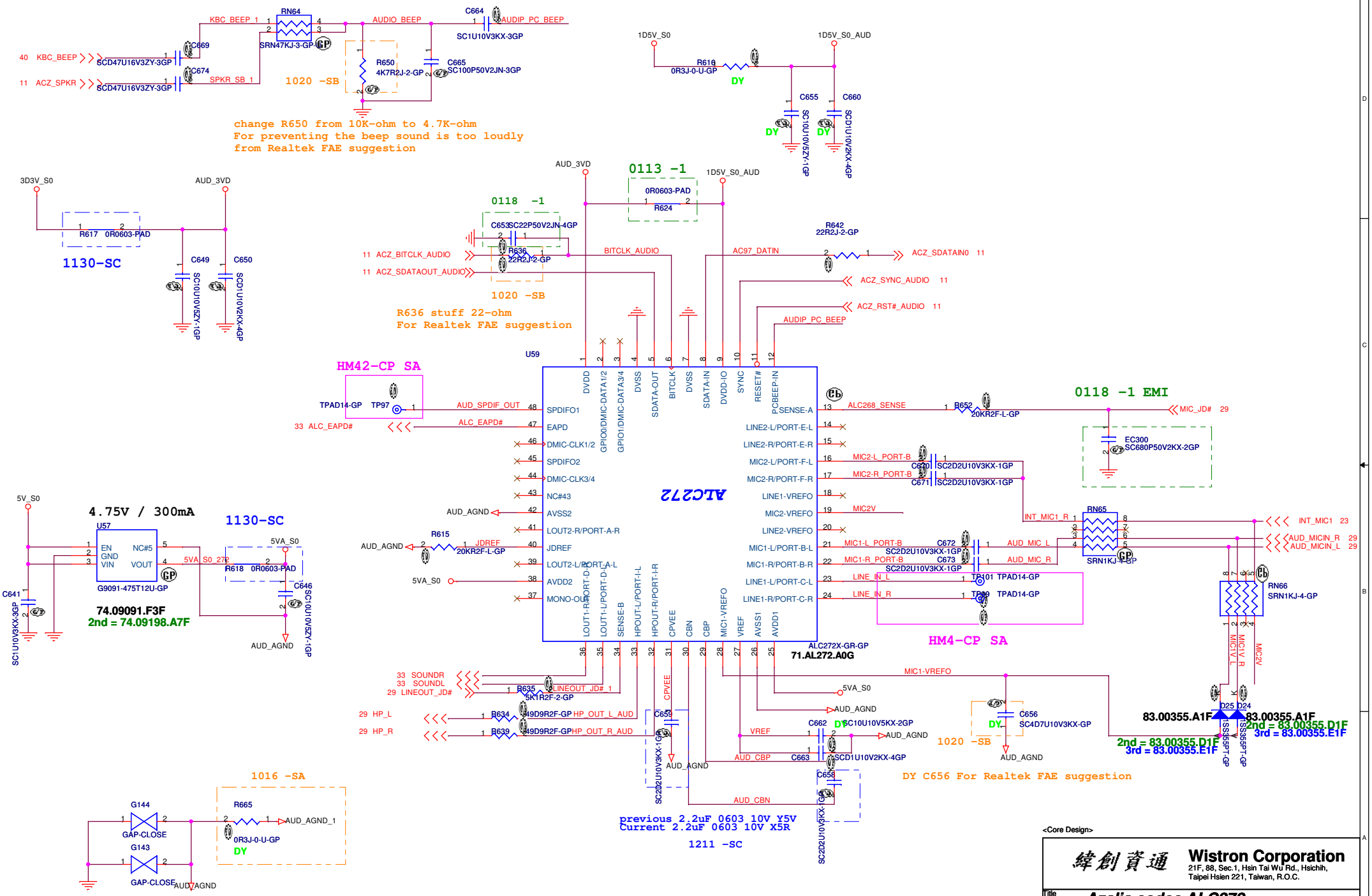


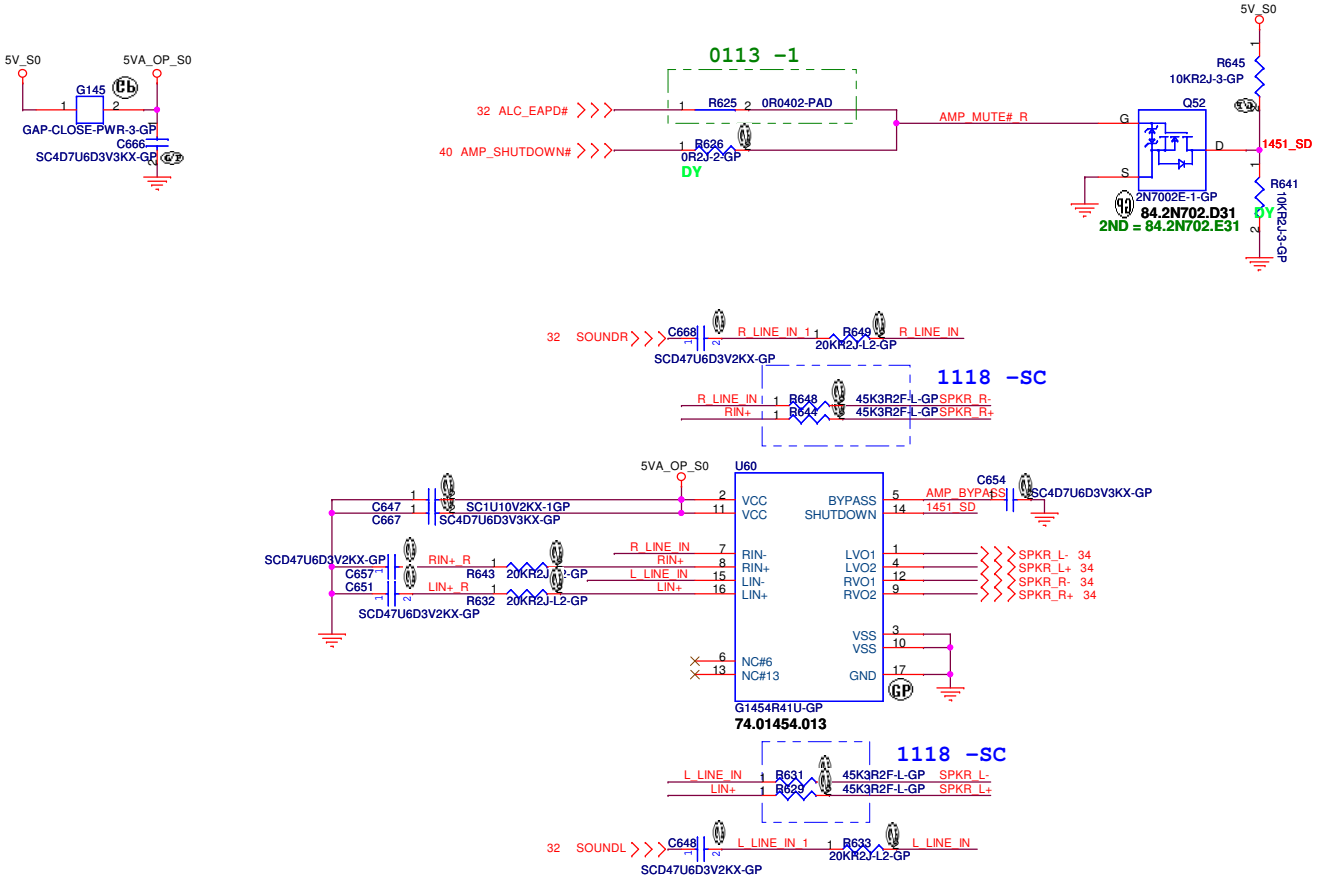
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Azalia codec ALC272

Size: A3 | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 32 of 72



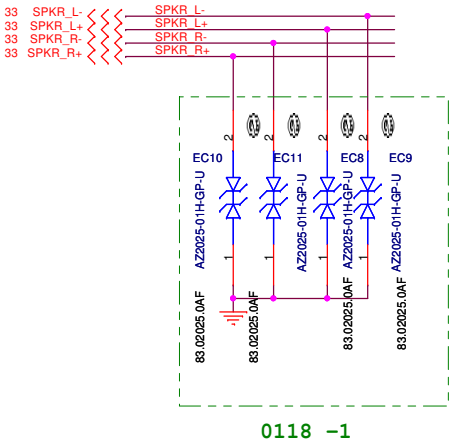

```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.446^2/4=1.5W
```

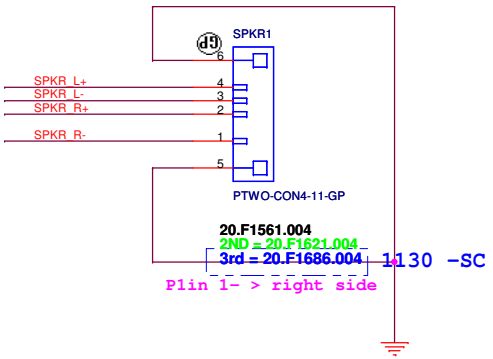
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO AMP		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 33 of 72	

Internal Speaker





Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO SPEARK*		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 34 of 72	

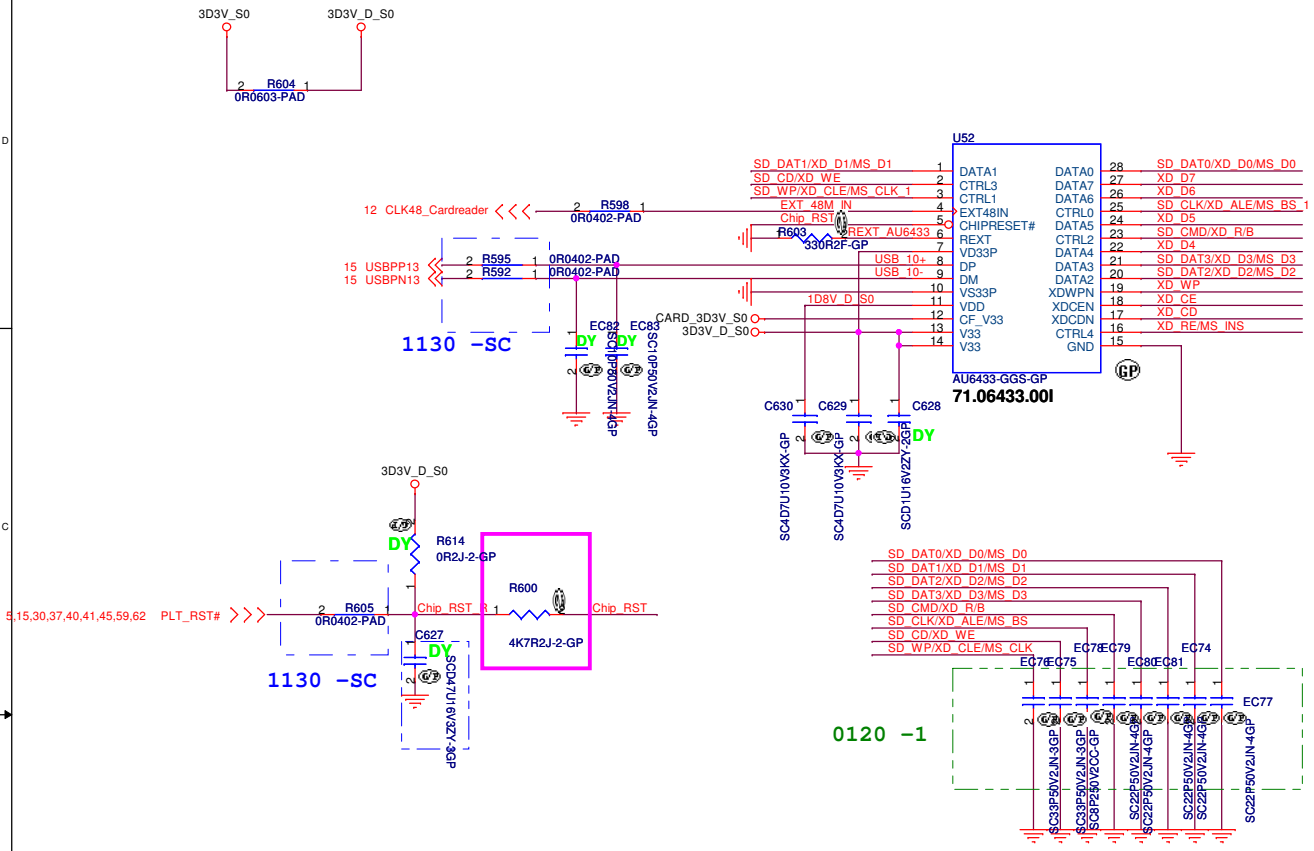
JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Resrve_MDC

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 35 of 72

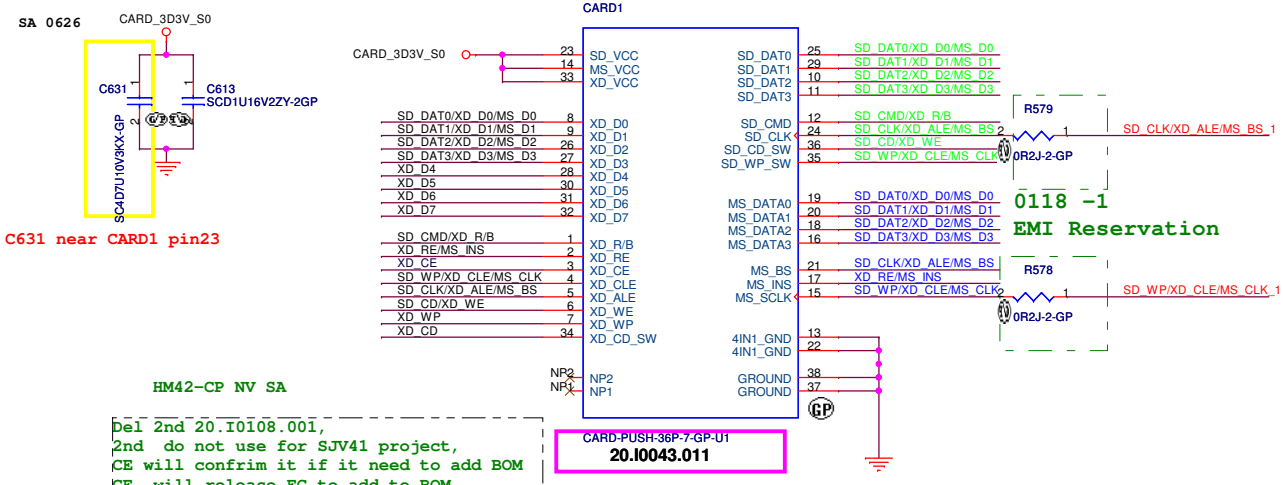


Pin	SD Mode	
	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1 xD-R/B			2P
P2 xD-RE			3P
P3 xD-CE			4P
P4 xD-CLE			5P
P5 xD-ALE			6P
P6 xD-WE			7P
P7 xD-WP			8P
P8 xD-D0			10P
P9 xD-D1			11P
P10 SD-DAT2	9P		
P11 SD-DAT3	1P		
P12 SD-CMD	2P		
P13 4in1-GND	3P/6P	1P/10P	1P/9P
P14 MS-VCC		9P	
P15 MS-SCLK		8P	
P16 MS-DATA3		7P	
P17 MS-INS		6P	
P18 MS-DATA2		5P	
P19 MS-DATA0		4P	

Pin No.	SD/MMC	MS/MS PRO	xD
P20 MS-DATA1		3P	
P21 MS-BS		2P	
P22 4in1-GND	3P/6P	1P/10P	1P/9P
P23 SD-VCC	4P		
P24 SD-CLK	5P		
P25 SD-DAT0	7P		
P26 xD-D2			12P
P27 xD-D3			13P
P28 xD-D4			14P
P29 SD-DAT1	8P		
P30 xD-D5			15P
P31 xD-D6			16P
P32 xD-D7			17P
P33 xD-VCC			18P
P34 XD-CD-SW			19P
P35 SD-WP-SW	SD-WP-SW		
P36 SD-CD-SW	SD-CD-SW		
P37 P38	4 IN 1-GND	SD-WP/CD-SW-GND	

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Del 2nd 20.I0108.001,
2nd do not use for SJV41 project,
CE will confrim it if it need to add BOM
CE will release EC to add to BOM

Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2,7V - 3,6V)
10	VSS	Vss

UMA

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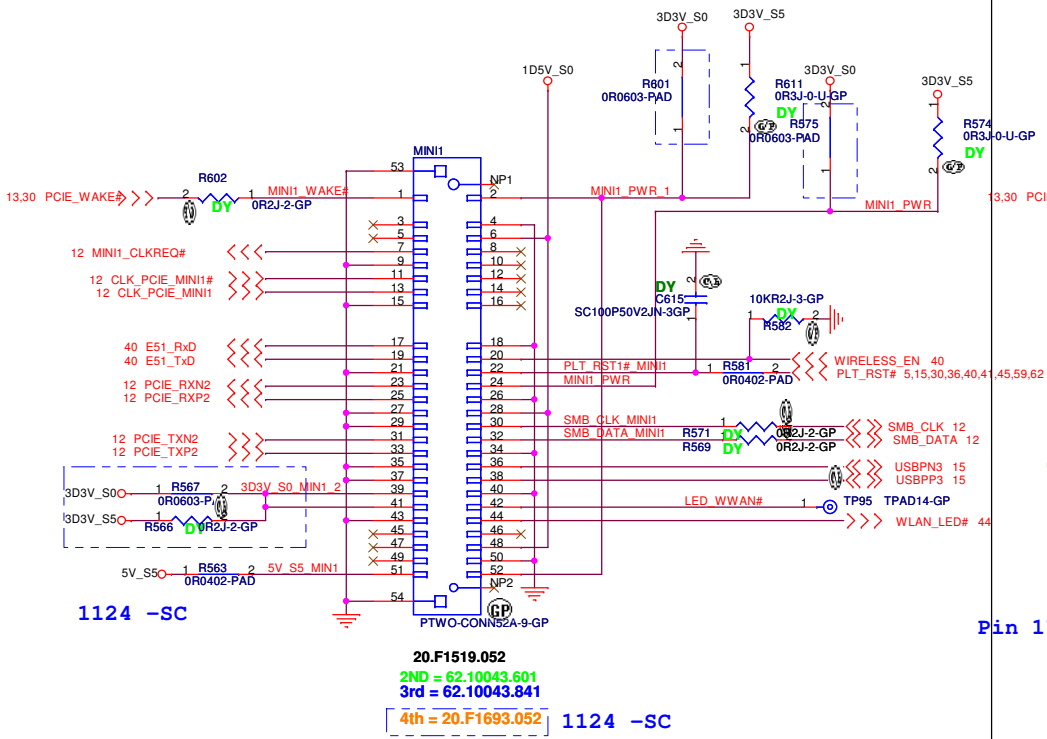
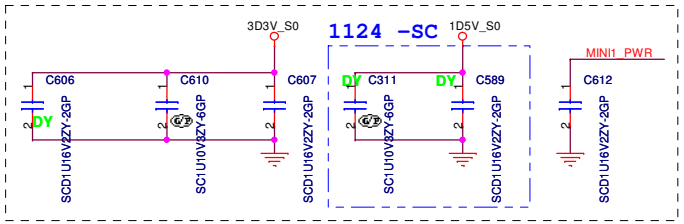
Title: Cardreader
Size | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 36 of 72

Mini Card Connector(WLAN)
Support debug-card

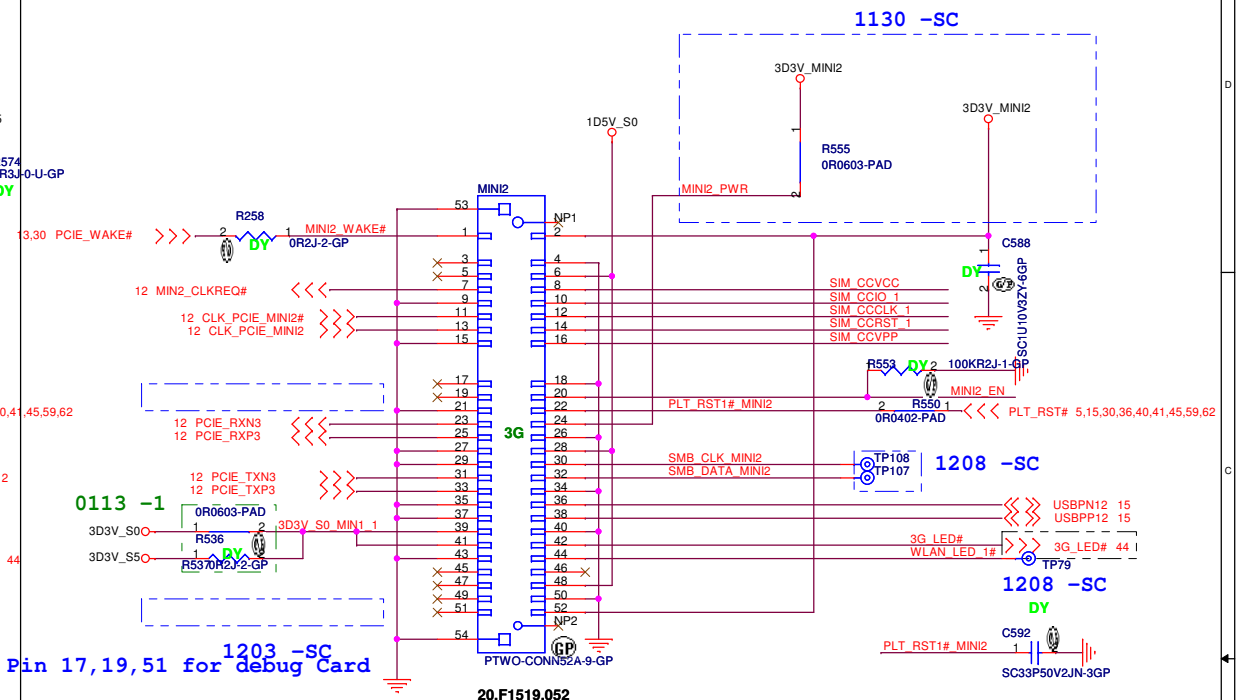


20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC

Place near MINI1

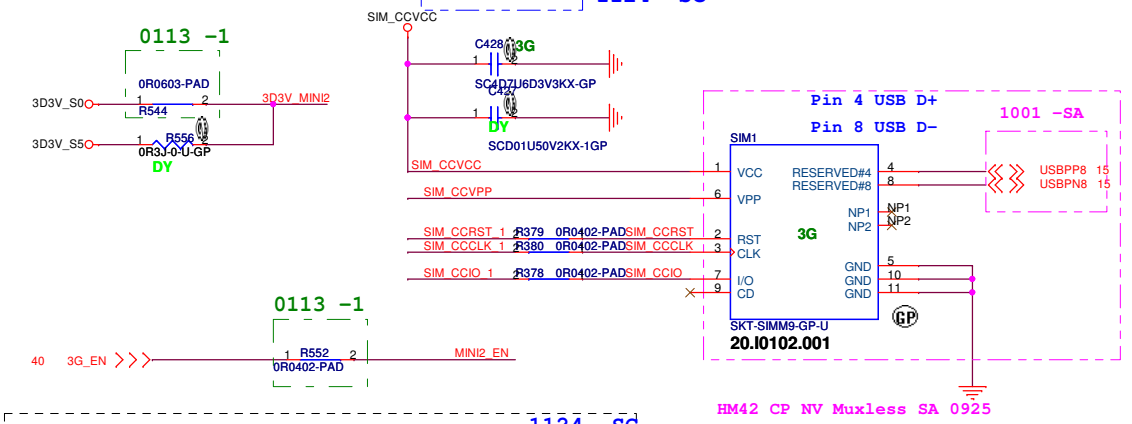


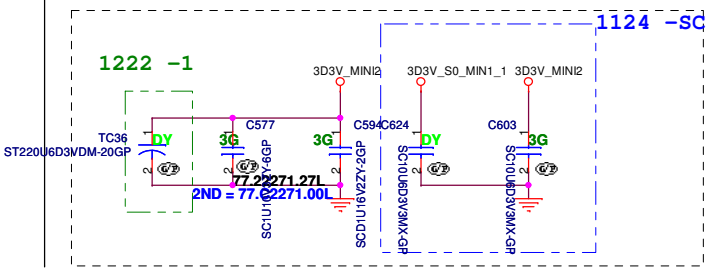
Mini Card Connector(Robson2 and 3G)



Pin 17,19,51 for debug Card

20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC





Diserete N11M

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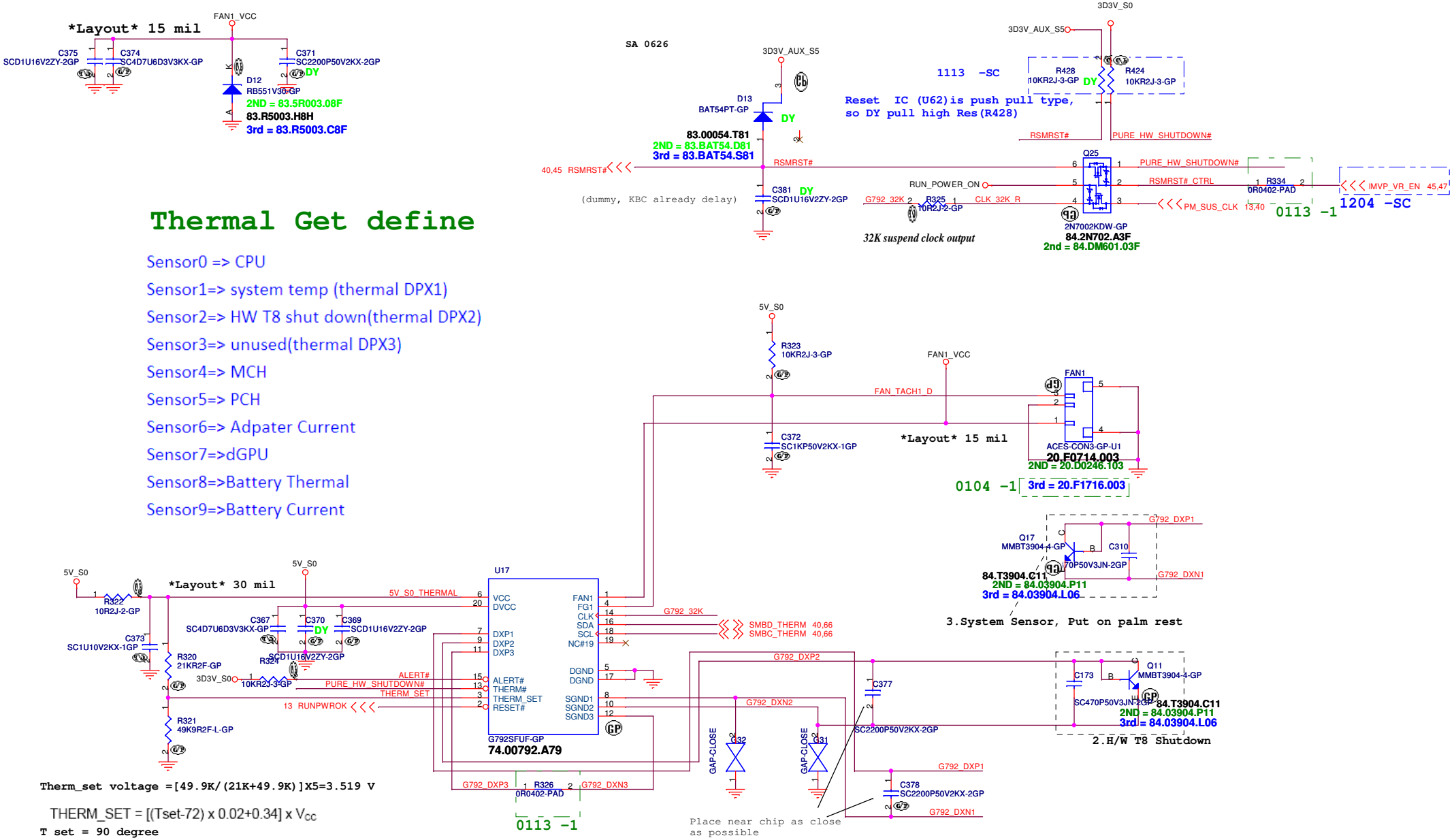
Title: MINI CARD		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 37 of 72	



UMA

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Title: ***Thermal/Fan Connector***

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 39 of 72

Prevent BIOS data loss solution
1019 -SB

L16 -> 68.00082.011 is a obsoleted part
0930 -SA

Impedance: 60-ohm
rated Current :3A

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	10.0 K	1.0 K	3.0 V
SB	10.0 K	2.0 K	2.75 V
SC	10.0 K	3.0 K	2.54 V
-1	10.0 K	4.7 K	2.24 V
Reserved	10.0 K	6.98 K	1.94 V
Reserved	10.0 K	8.2 K	1.81 V
Reserved	10.0 K	10.0 K	1.65 V

Model ID
14" PH 10K 3.3V_AUX_S5
17" PL 10K GND

Value	PN
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

FOR KBC DEBUG

SA 0928
ENE suggest 1pF if stuff

add test point for debug

Internal KeyBoard Connector

U31 stuff 71.03930.A0G,we can DY X4 'tal

CL = 7pF
Freq tolertance :+/- 20 ppm

Cover Up Switch

change connect to FPC (Same as Lab)
20.K0251.026 Pin 1 ->left side
20.K0320.026 Pin 1 -> right side(use in lab stage)
so swap net

do not use 74.00268.07B in project for Deark suggestion
10-28 -SB

UMA

Wistron Corporation
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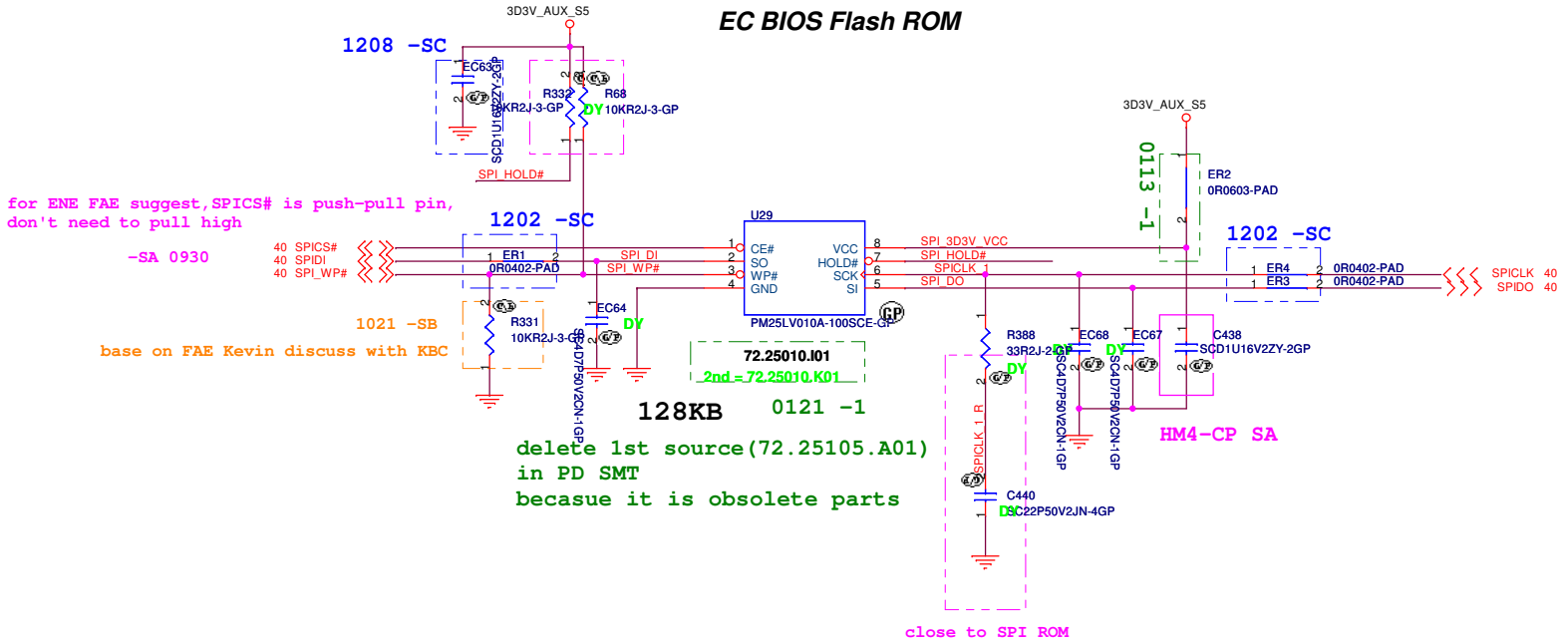
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_KB3930

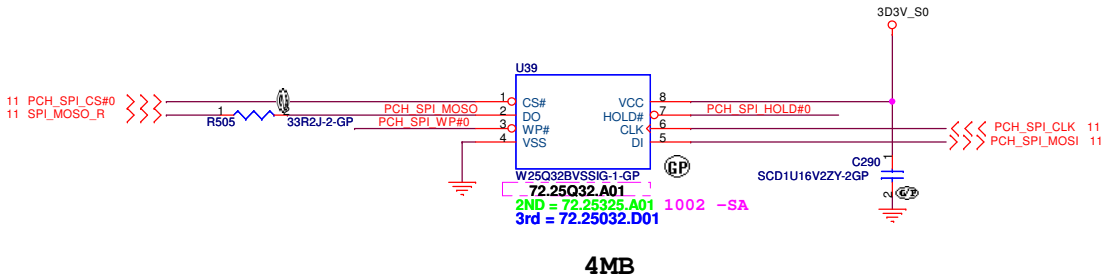
Size: | Document Number: 1 | Rev: SC

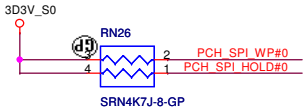
Date: Friday, January 22, 2010 | Sheet 40 of 72

EC BIOS Flash ROM

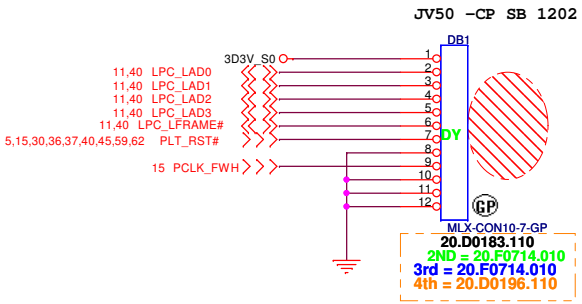


System BIOS Flash ROM





GOLDEN FINGER FOR DEBUG BOARD



Lab only stuff 4th source(20.D0196.110)
Eng and PD DY DB1

Diserete N11M

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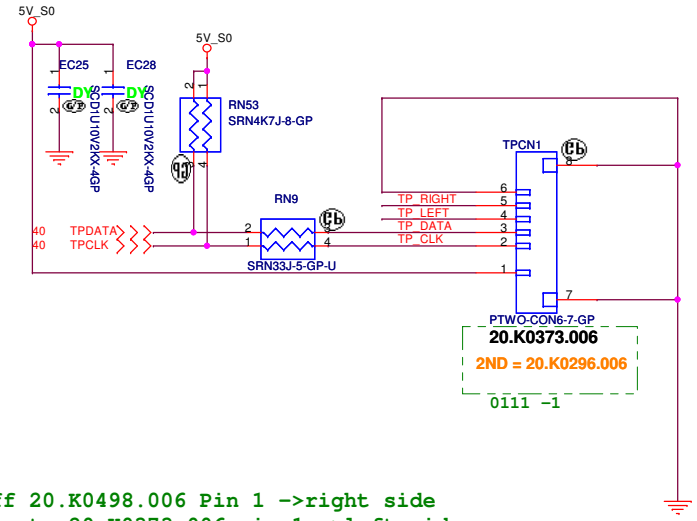
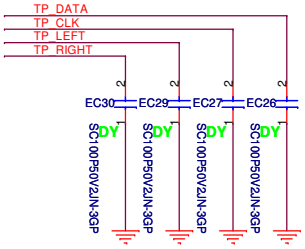
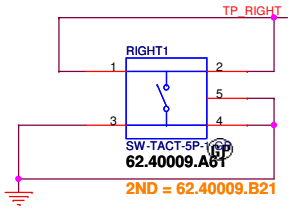
Title		
BIOS		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 41 of 72	



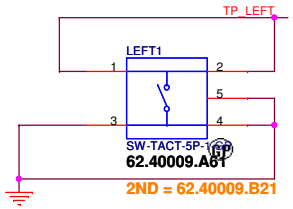


Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically

RIGHT



LEFT



Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Touch PAD*		
Size	Document Number: HM42-CP	Rev: SC
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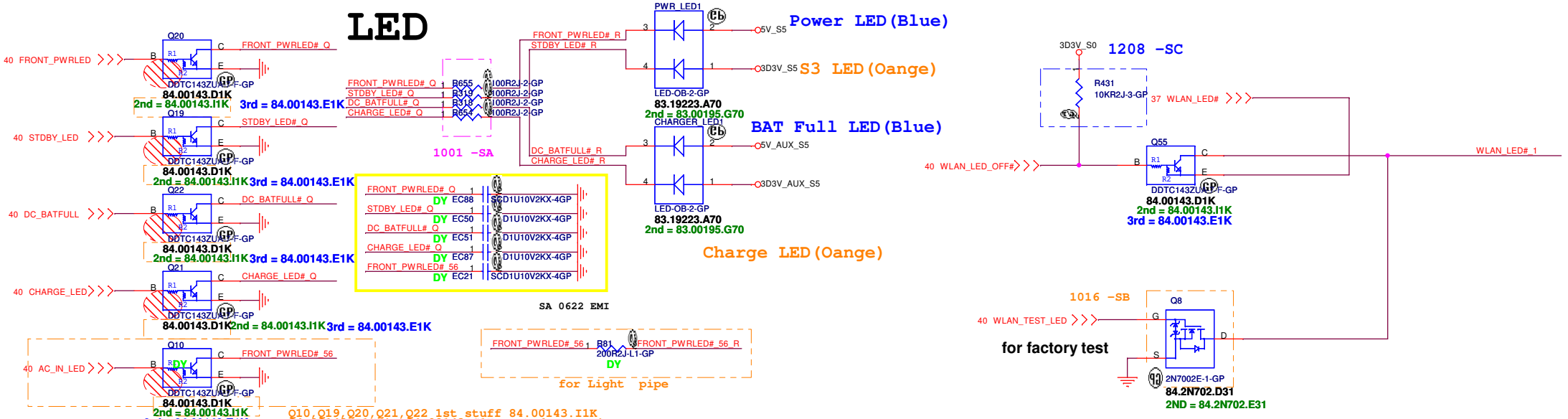
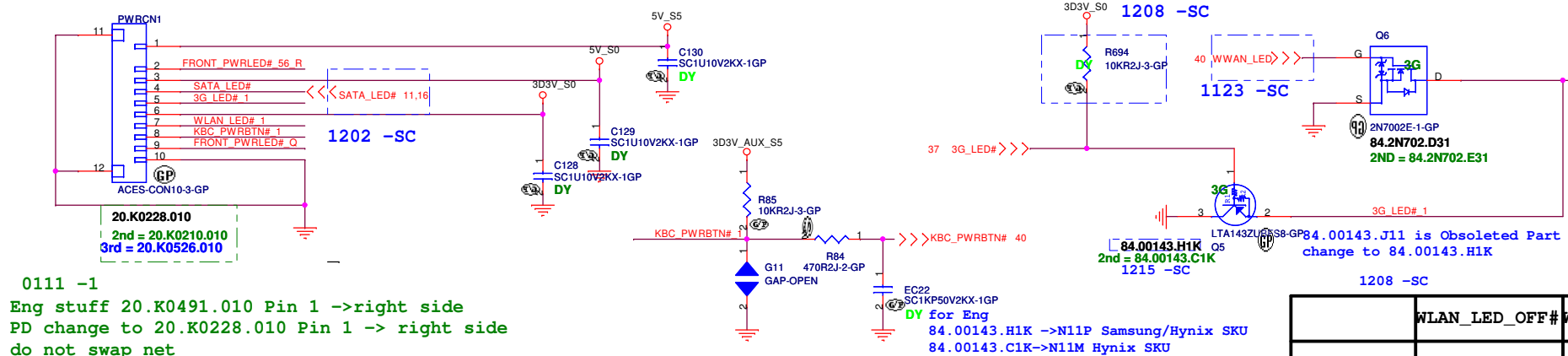
LED



For 2010 Acer Project, WLAN and 3G LED control by KBC



0111 -1
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net

84.00143.H1K ->N11P Samsung/Hynix SKU
84.00143.C1K->N11M Hynix SKU

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

<Core Design>

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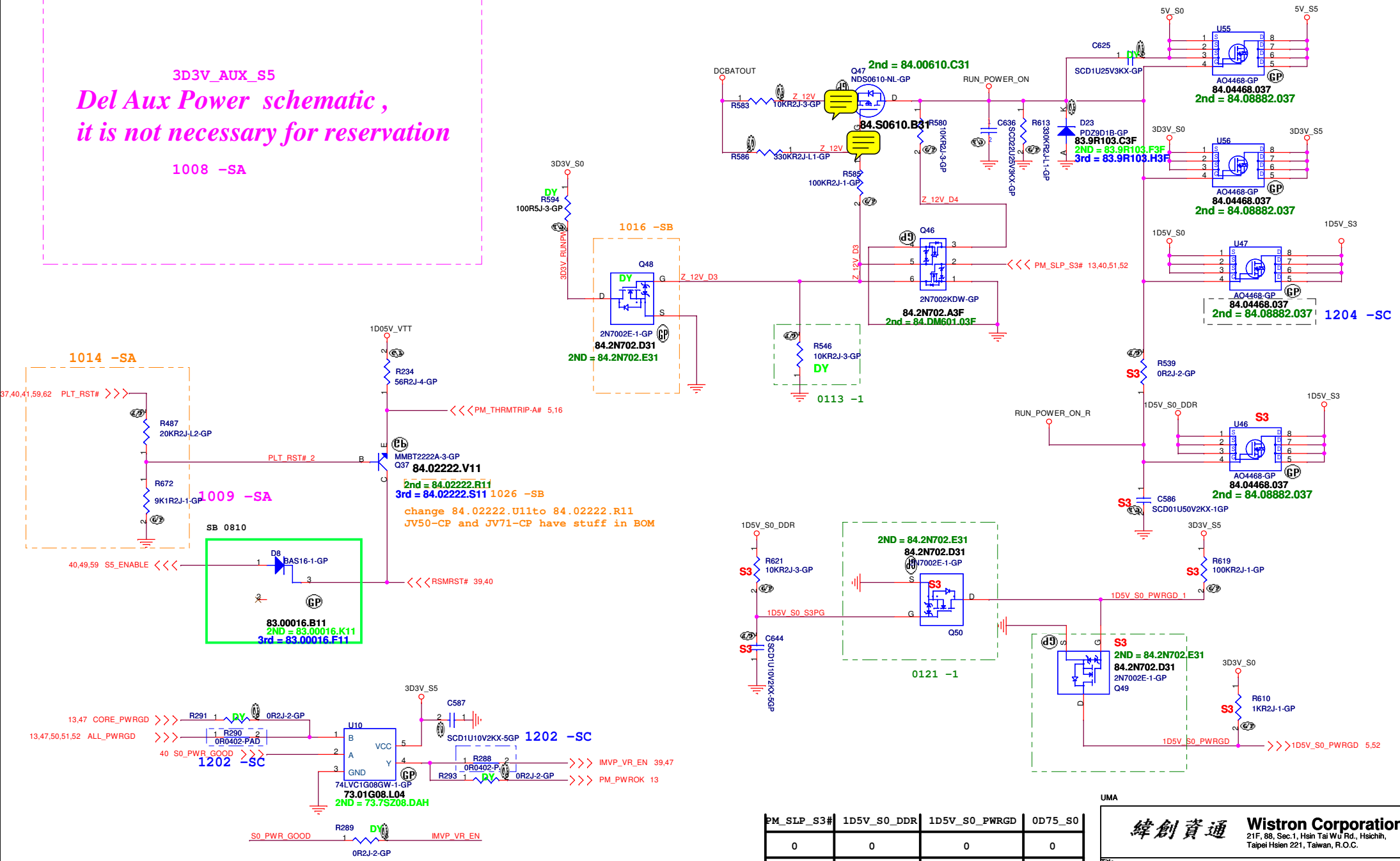
Title: LED&POWERBD CONN
Size | Document Number: HM42-CP | Rev: SC
Date: Friday, January 22, 2010 | Sheet 44 of 72

Run Power

3D3V_AUX_S5

Del Aux Power schematic ,
it is not necessary for reservation

1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

UMA

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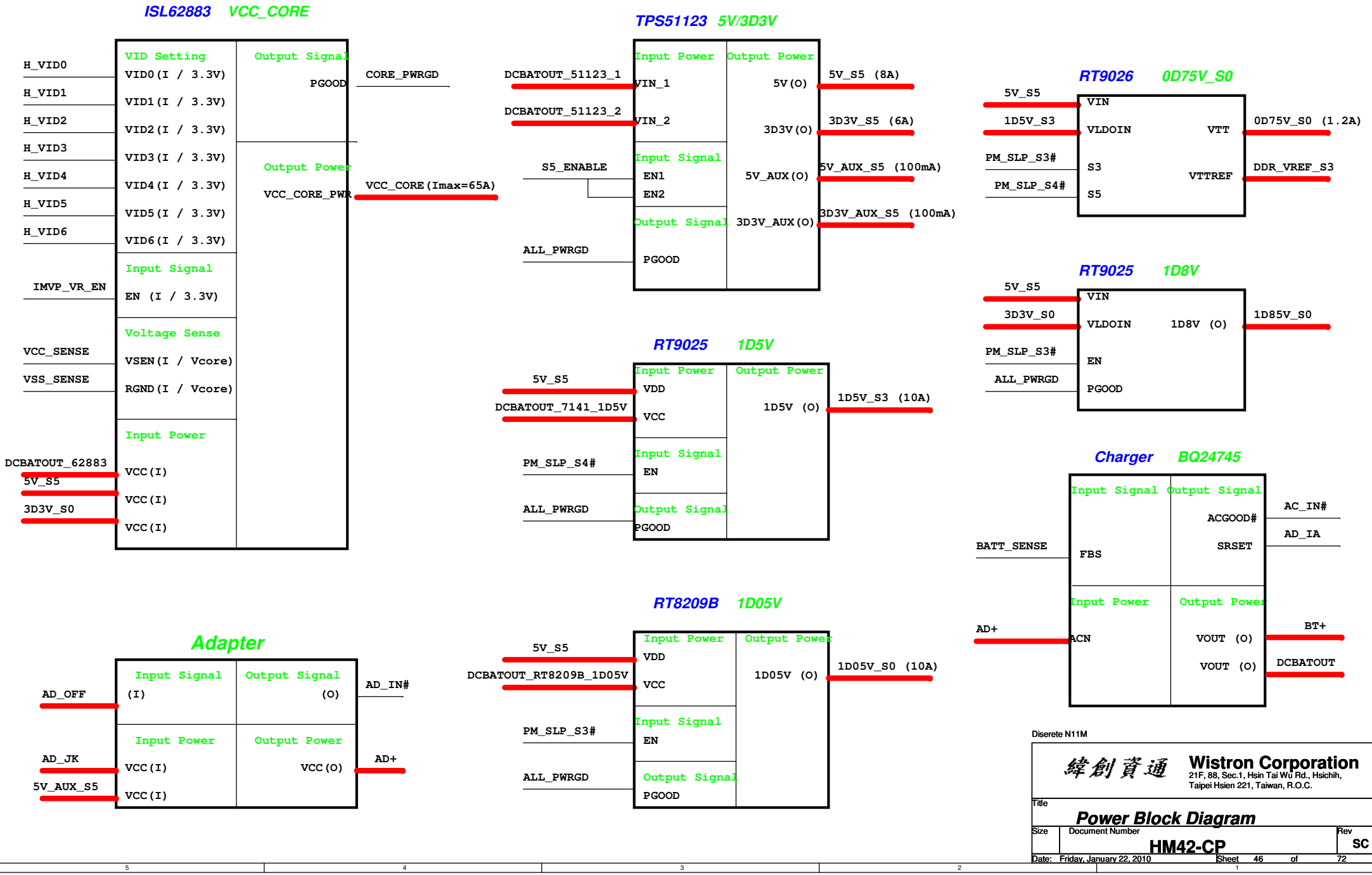
Title: **RUN POWER and 3D3V_AUX_S5**

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 45 of 72



Diserete N11M

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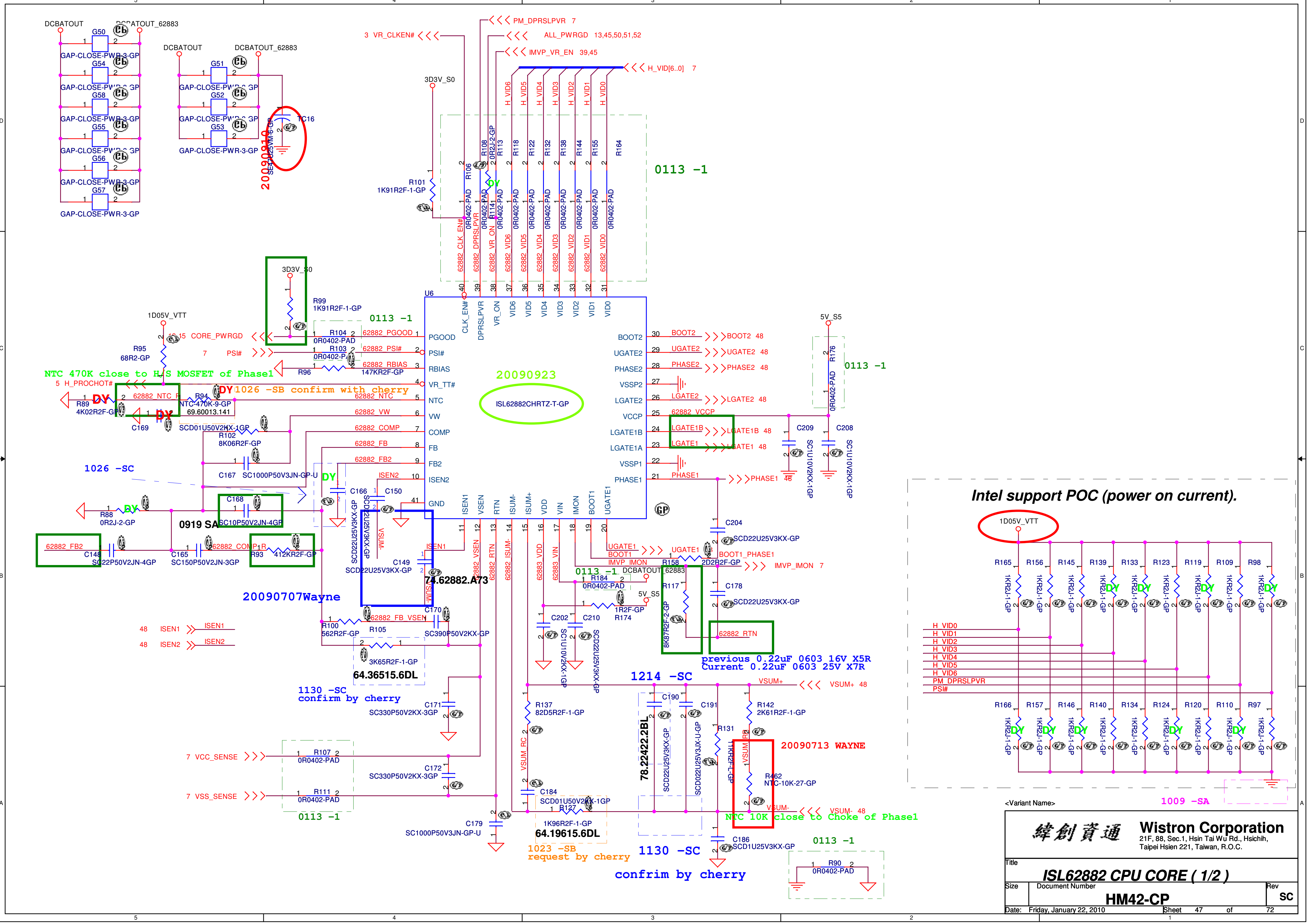
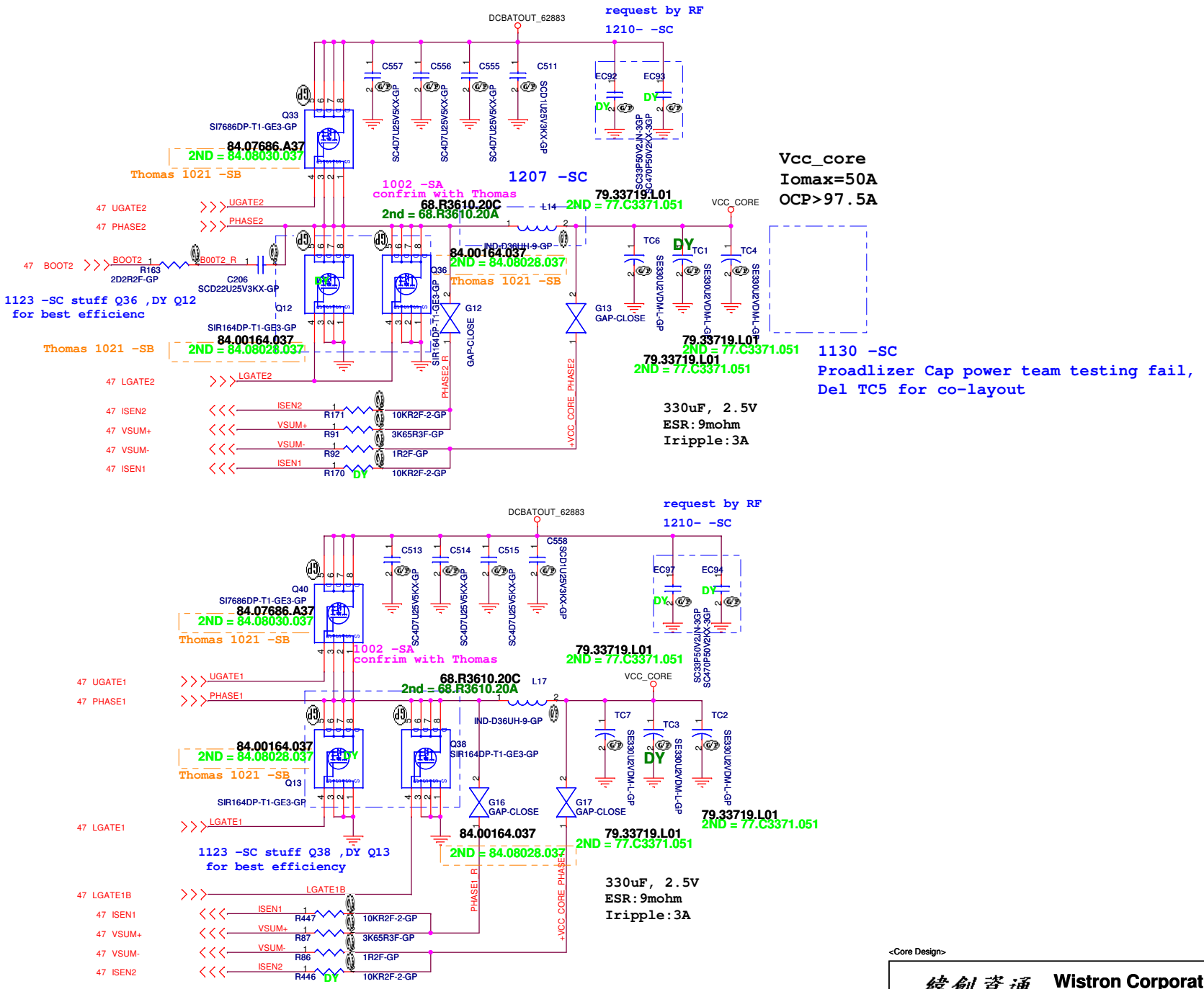
Title: **Power Block Diagram**

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 46 of 72



ISL62882CHRTZ-T-GP
20090923
0113 -1
1026 -SB confirm with cherry
NTC 470K close to H/S MOSFET of Phase1
NTC 10K close to Choke of Phase1
1026 -SC
0919 SA
20090707Wayne
20090713 WAYNE
20090910
1214 -SC
1130 -SC confirm by cherry
1023 -SB request by cherry
1130 -SC
confrim by cherry
previous 0.22uF 0603 16V X5R
Current 0.22uF 0603 25V X7R
74.62882.A73
64.36515.6DL
64.19615.6DL
78.22422.2BL
Intel support POC (power on current).
1009 -SA
PM_DPRSLPVR 7
ALL_PWRGD 13,45,50,51,52
IMVP_VR_EN 39,45
H_VID[6..0] 7
3 VR_CLKEN#
CORE_PWRGD
PSI#
5 H_PROCHOT#
BOOT2 48
UGATE2 48
PHASE2 48
LGATE2 48
LGATE1B 48
LGATE1 48
PHASE1 48
IMVP_IMON 7
VSUM+ 48
VSUM- 48
7 VCC_SENSE
7 VSS_SENSE
48 ISEN1
48 ISEN2
DCBATOUT
DCBATOUT_62883
3D3V_S0
1D05V_VTT
5V_S5
GAP-CLOSE-PWR-3-GP
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: ISL62882 CPU CORE (1/2)
Size
Document Number: HM42-CP
Rev: SC
Date: Friday, January 22, 2010
Sheet 47 of 72



<Core Design>

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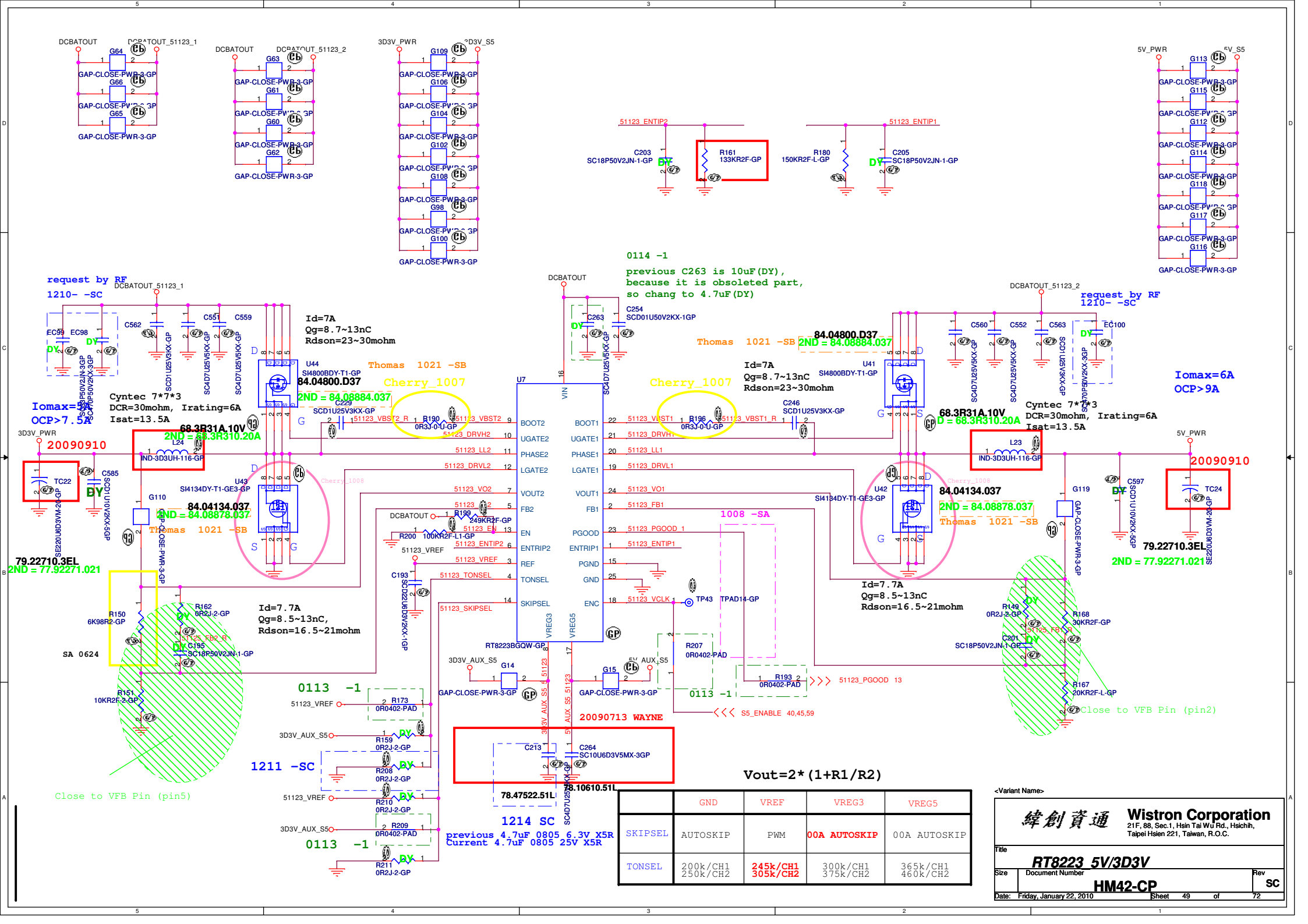
Title: ISL62882 CPU CORE (1/2)

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 48 of 72



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>

緯創資通 Wistron Corporation
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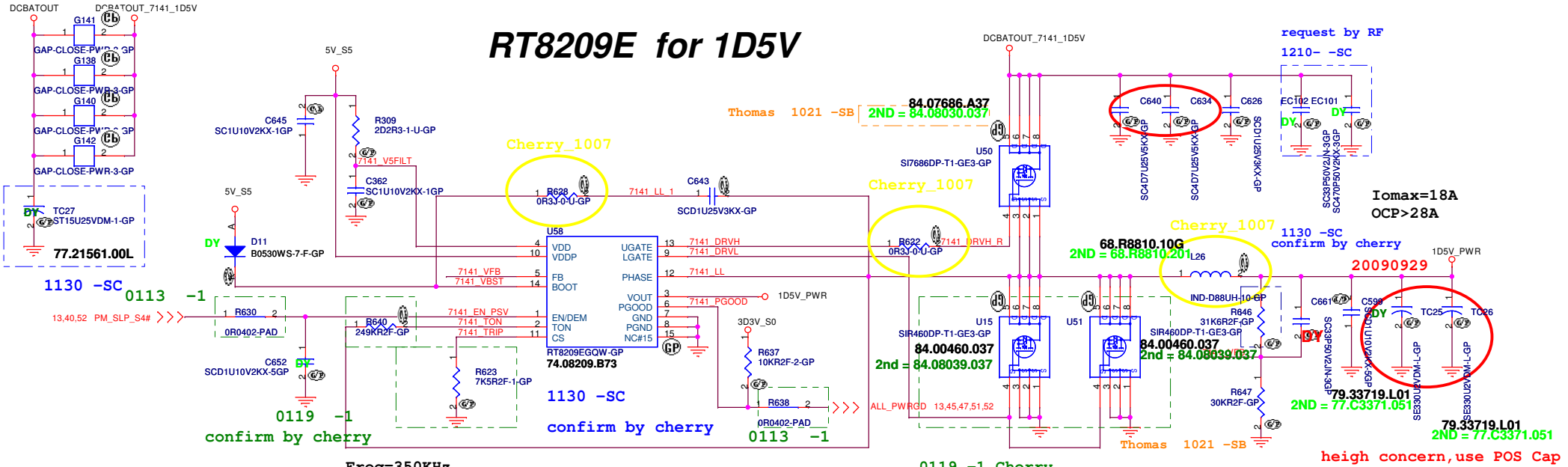
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 49 of 72

RT8209E for 1D5V



Freq=350KHz

$$V_{CS}\,(mV) = R_{CS}\,(k\Omega) \times 10\,(\mu A)$$

$$I_{LOAD\_OC} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{I_{Ripple}}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{V_{IN}}$$

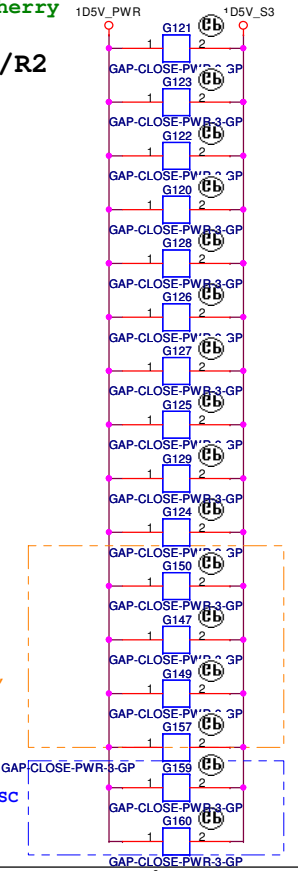
VCS(mV)=9.09KX10uA=90.9mV

I_OCP=[(90.9mV/3.2mohm)+(1/2*350Khz* 0.88uH)*[(19-1.5)*1.5/19]

=28.4 +1.623 *1.38 =30A

Iocp = Io *1.5

Vout=0.75V*(R1+R2)/R2

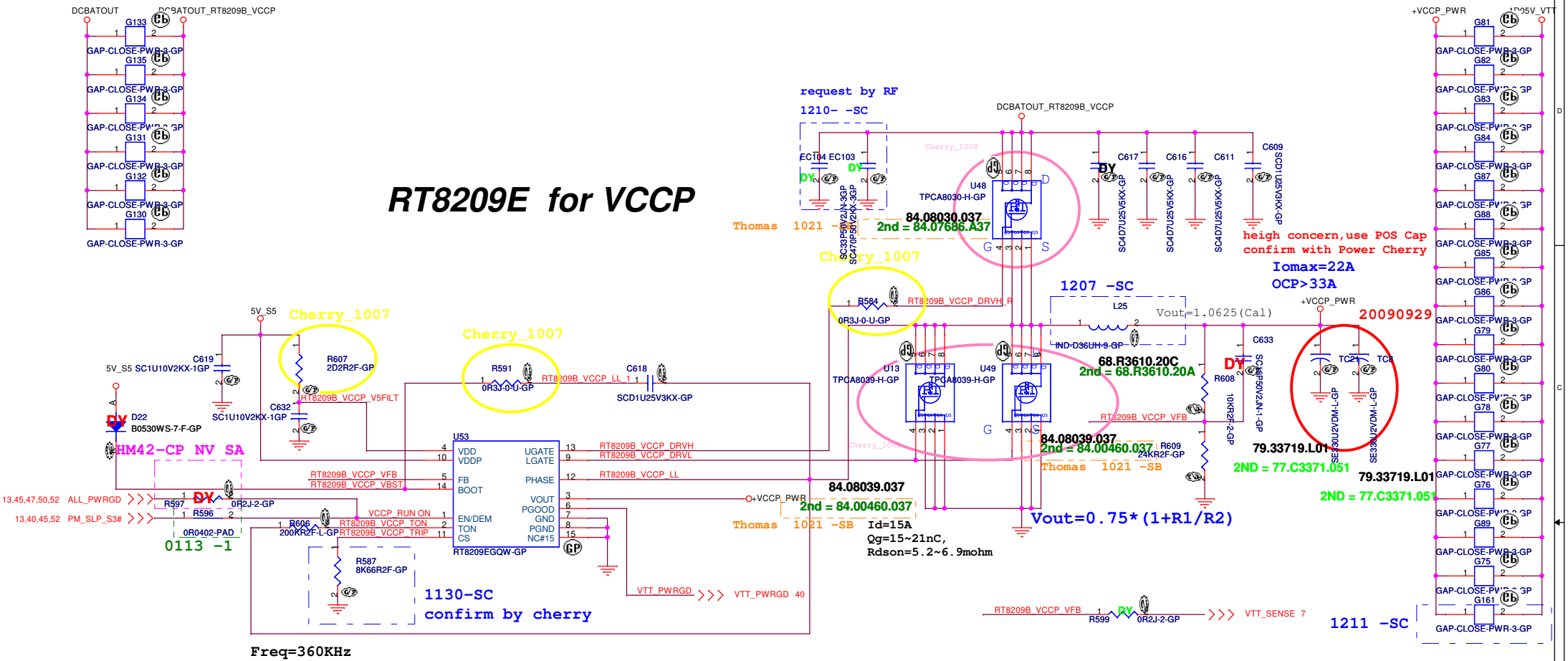


1022 -SB
cherry request 8 pcs Gap,
becasue of space concern,
only add 4pcs Cap.

Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8209B_1D5V		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 50 of 72	

RT8209E for VCCP



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Title: RT8209B +VCCP	
Size	Document Number: HM42-CP
Rev: SC	
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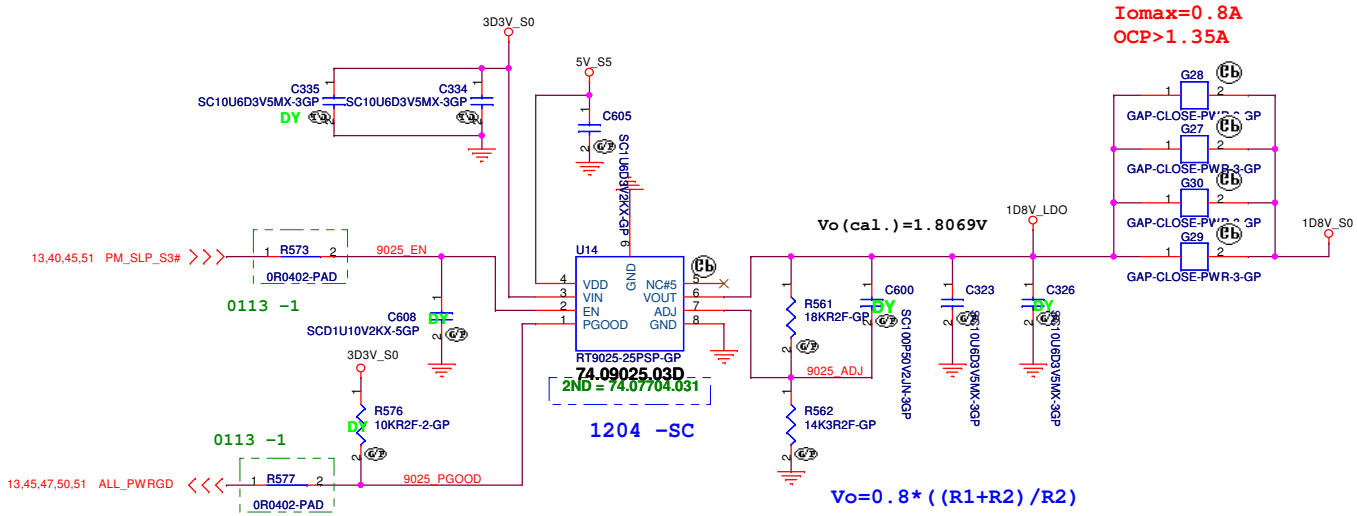
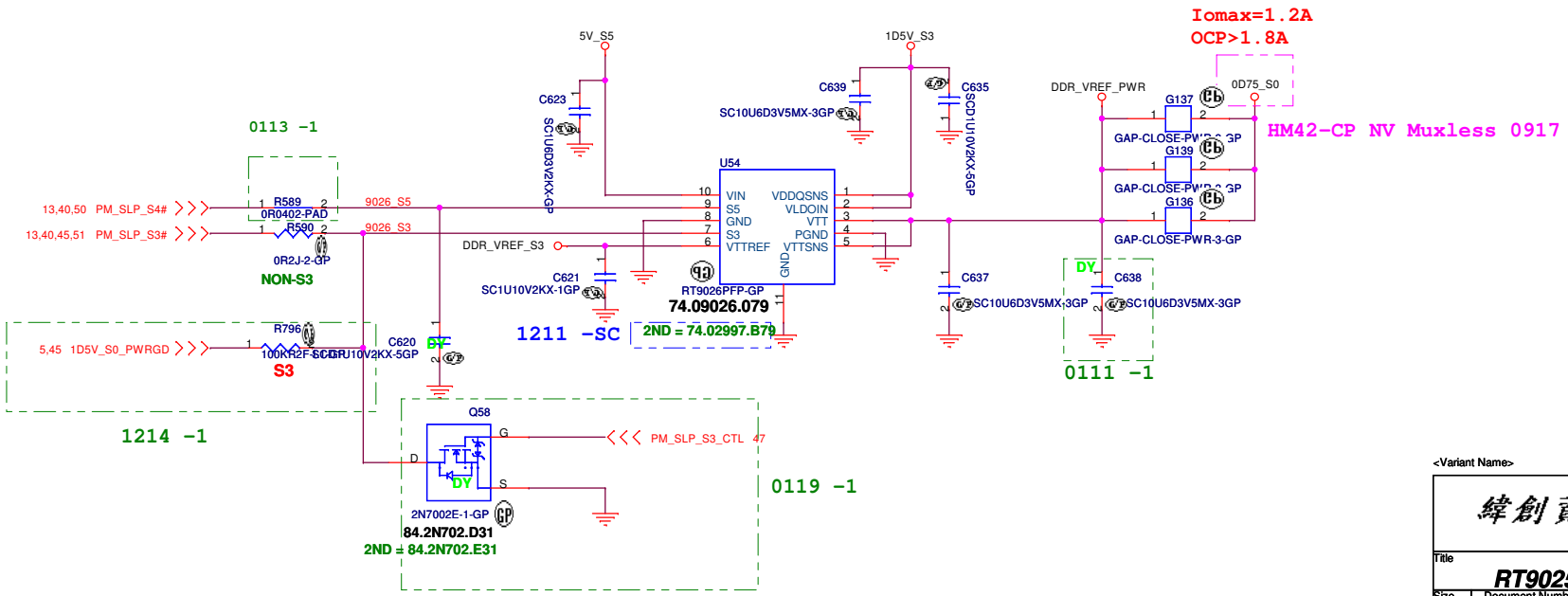
RT9025 for 1D8V_S0

20090915



RT9026 for 0D75V_S0



<Variant Name>

緯創資通 Wistron Corporation
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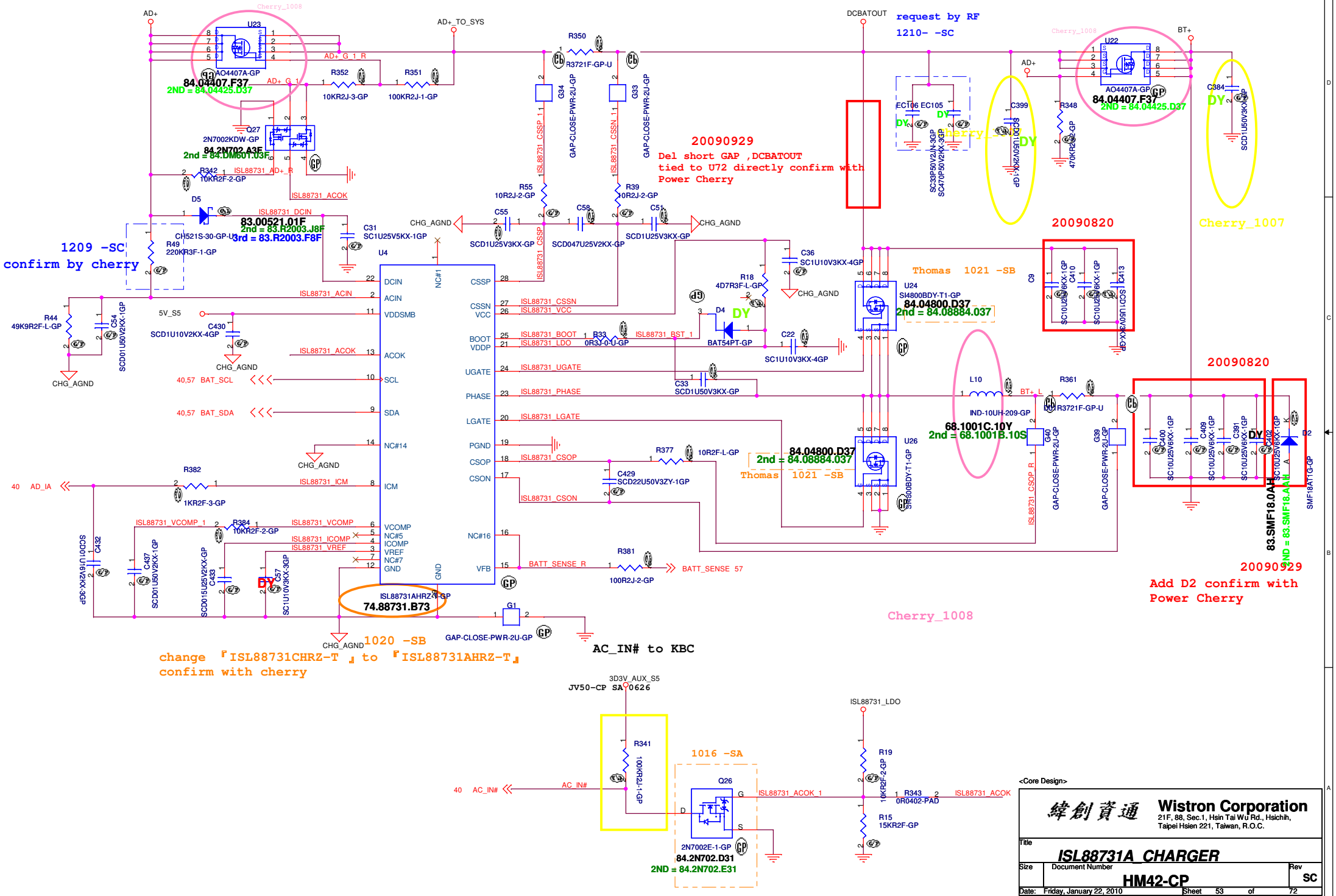
Title: RT9025_1D8V/RT9026_0D75

Size | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 52 of 72



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ISL88731A_CHARGER

Size | Document Number: HM42-CP | Rev: SC

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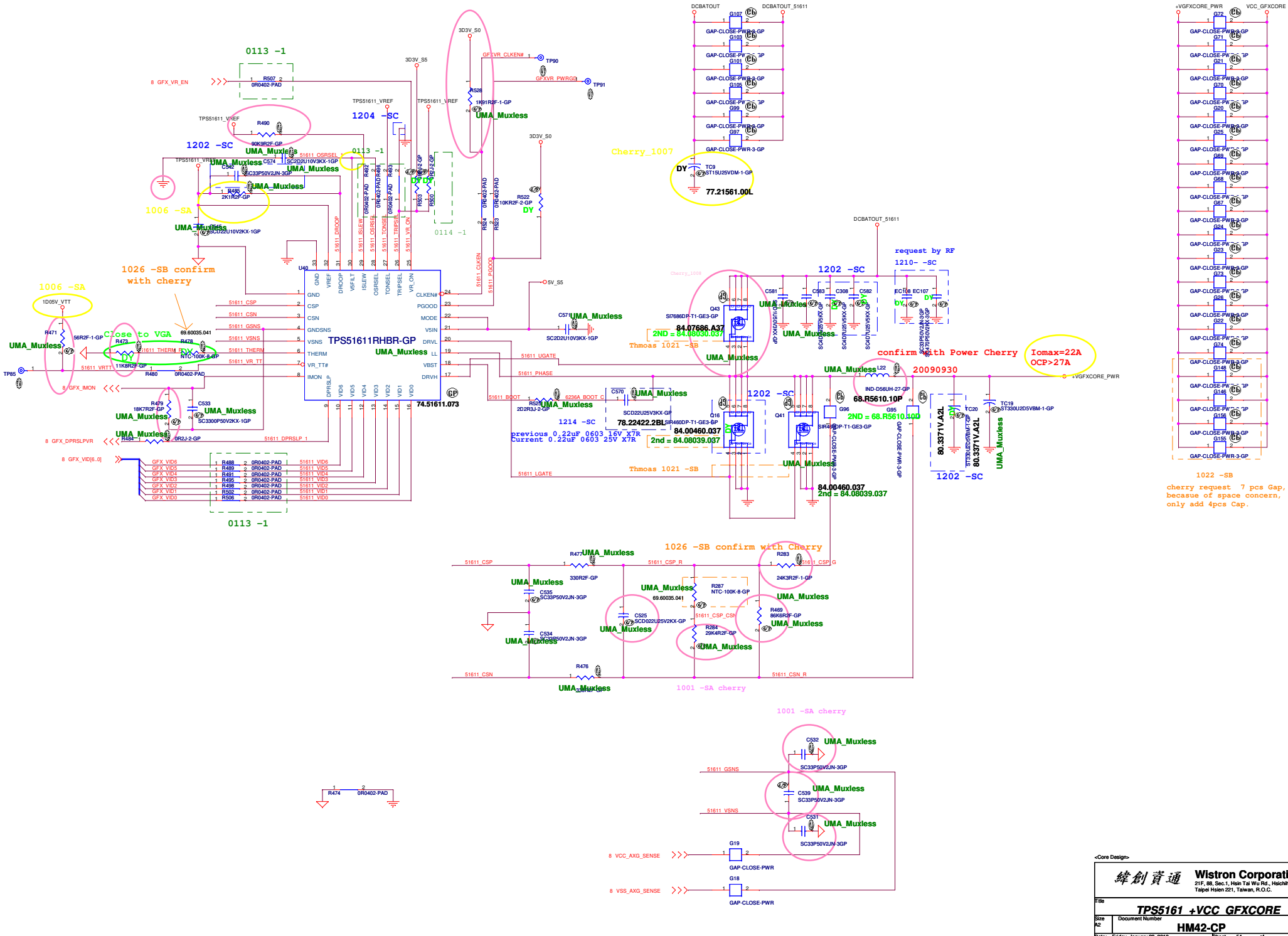
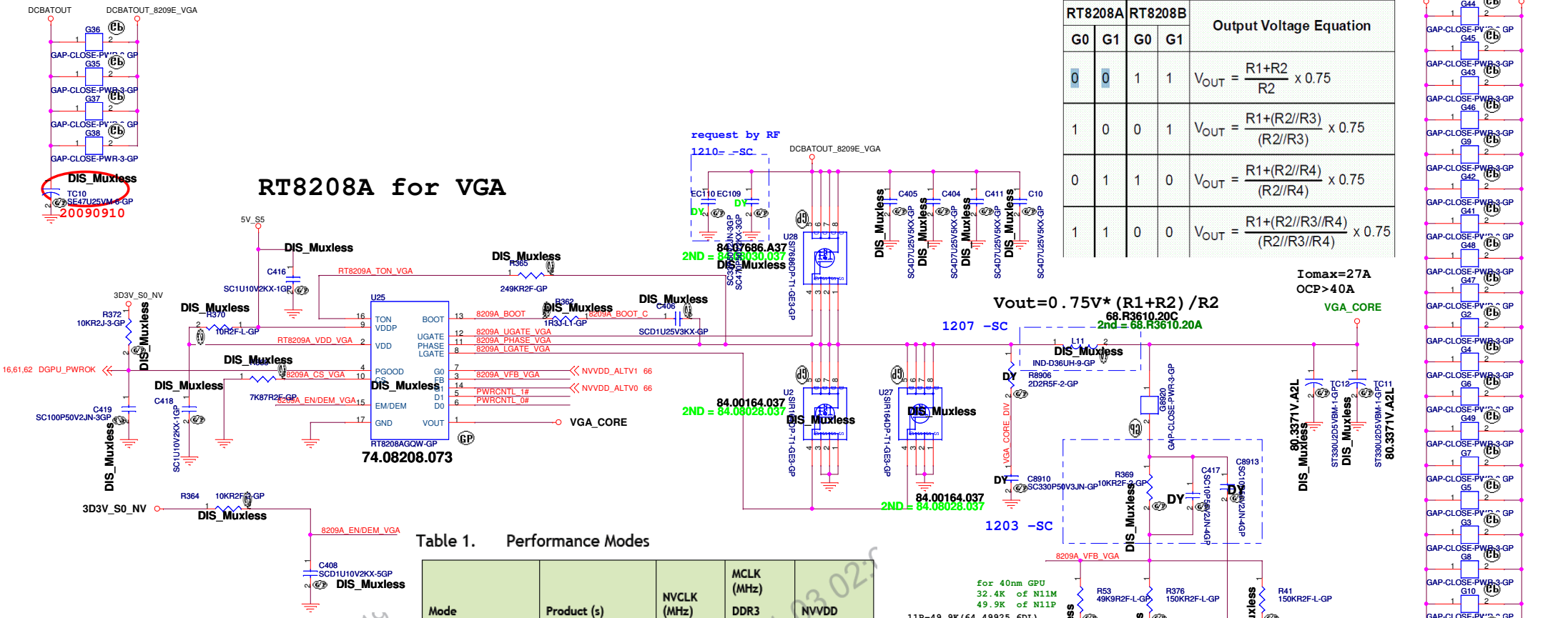

0113 -1
1204 -SC
1202 -SC
1006 -SA
1026 -SB confirm with cherry
Close to VGA
TPS51611RHBR-GP
74.51611.073
Cherry_1007
77.21561.00L
request by RF
1210- -SC
confirm with Power Cherry
Iomax=22A
OCP>27A
20090930
68.R5610.10P
84.07686.A37
84.00460.037
2nd = 84.08039.037
78.22422.2BL
1214 -SC
previous 0.22uF 0603 16V X7R
Current 0.22uF 0603 25V X7R
1001 -SA cherry
1022 -SB
cherry request 7 pcs Gap, becasue of space concern, only add 4pcs Cap.
UMA_Muxless
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
TPS5161 +VCC_GFXCORE
HM42-CP
Friday, January 22, 2010

RT8208A for VGA



RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-OP1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1, N11M-OP2	405	405	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

N11P-GE1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5//NVVDD_ALTV0	NVVDD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5/NVVDD_ALTV0	NVVDD
0	1	0.85
1	0	1.03

cherry request 9 pcs Gap, becasue of space concern, only add 5pcs Cap.

UMA

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Title: RT8209A_VGA_CORE

Size: Custom | Document Number: HM42-CP | Rev:

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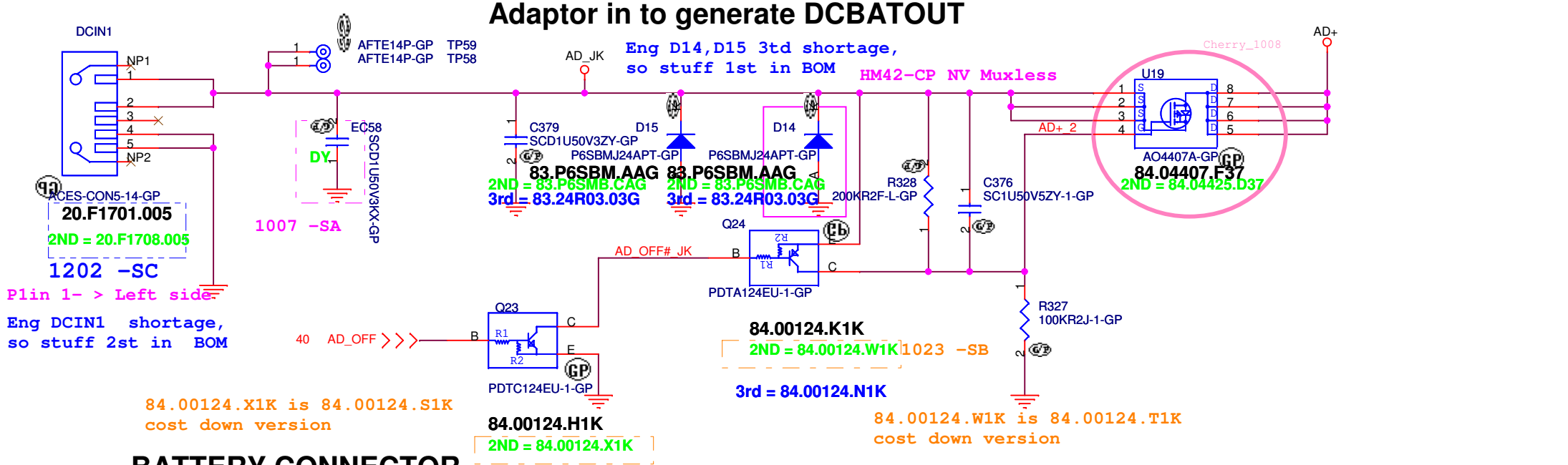
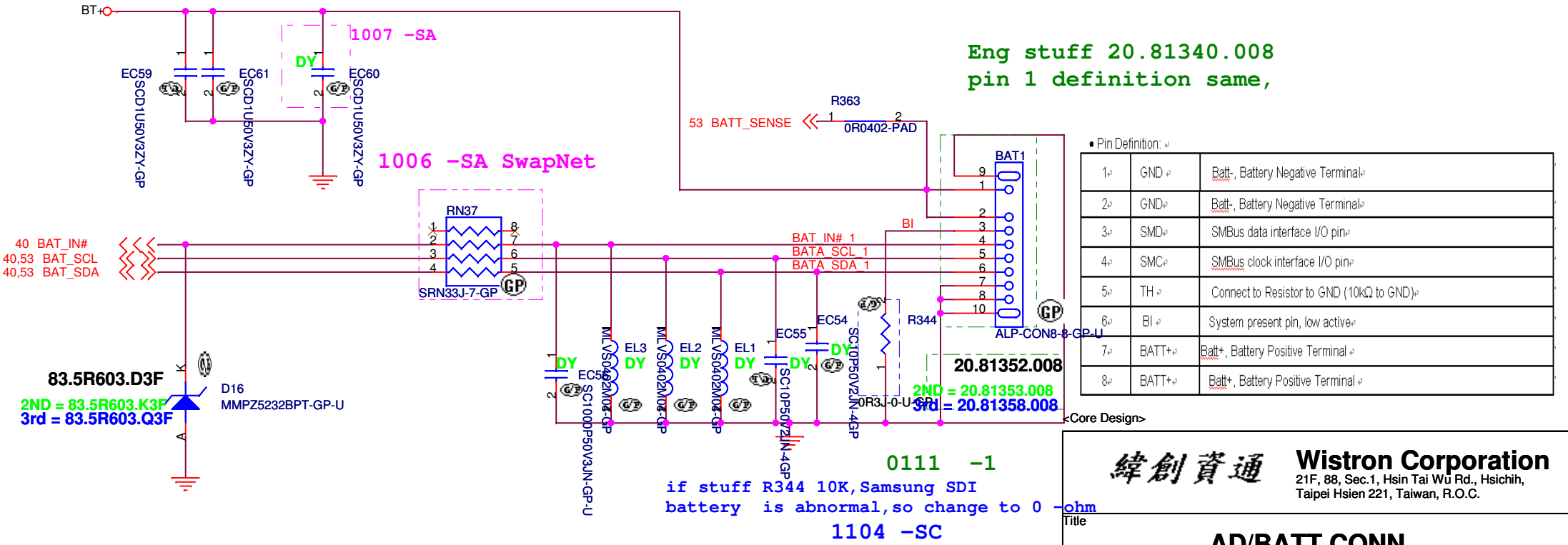
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

<Core Design>

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Title: **AD/BATT CONN**

Size	Document Number	Rev
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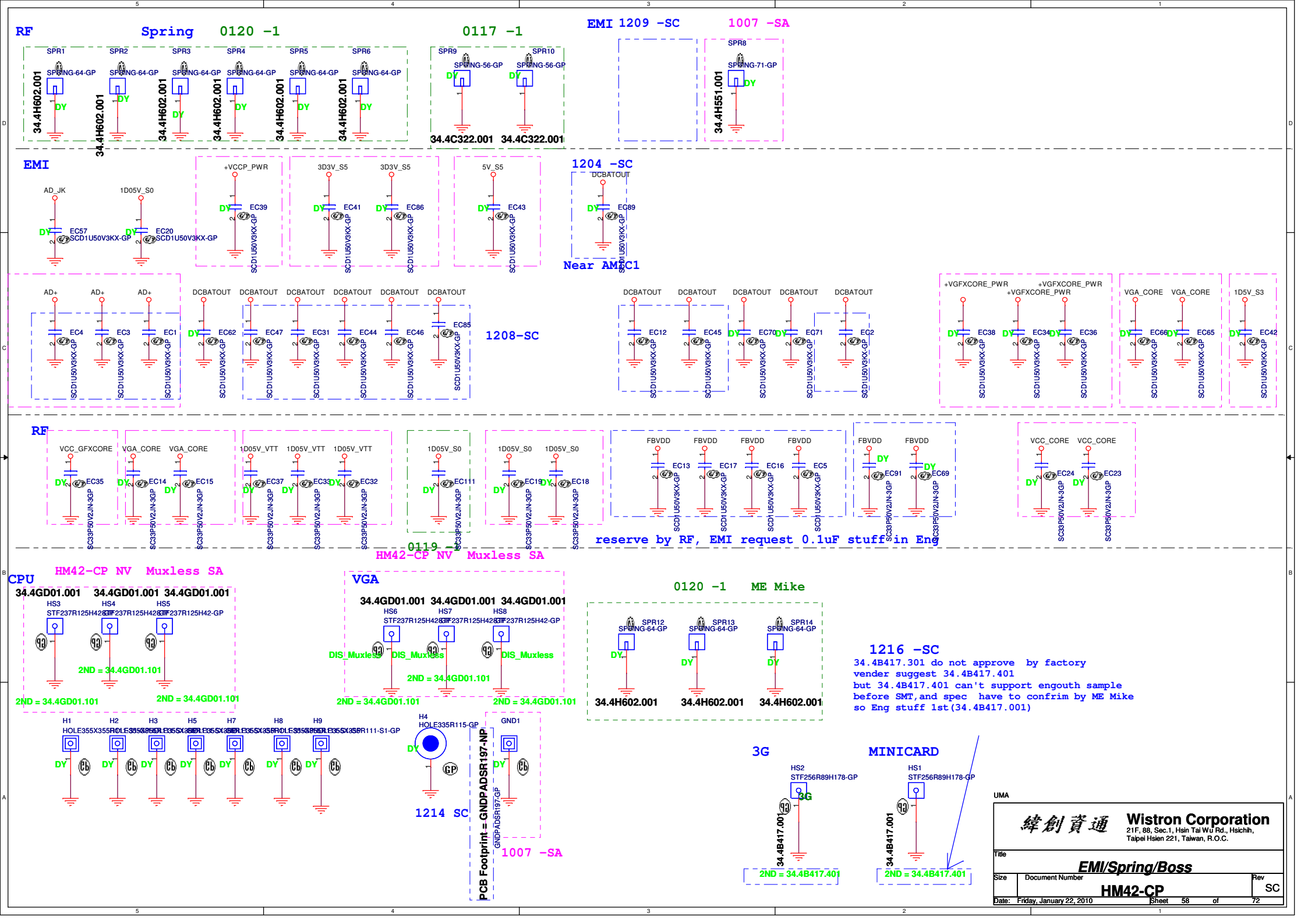
RF
Spring
0120 -1
0117 -1
EMI 1209 -SC
1007 -SA
SPR1
SPR2
SPR3
SPR4
SPR5
SPR6
SPRING-64-GP
34.4H602.001
DY
SPR9
SPR10
SPRING-56-GP
34.4C322.001
SPR8
SPRING-71-GP
34.4H551.001
EMI
AD_JK
1D05V_S0
EC57
EC20
SCD1U50V3KX-GP
+VCCP_PWR
EC39
3D3V_S5
EC41
EC86
5V_S5
EC43
1204 -SC
DCBATOUT
EC89
Near AMEC1
AD+
EC4
EC3
EC1
EC62
EC47
EC31
EC44
EC46
EC85
1208-SC
EC12
EC45
EC70
EC71
EC2
+VGFXCORE_PWR
EC38
EC34
EC36
VGA_CORE
EC66
EC65
1D5V_S3
EC42
RF
VCC_GFXCORE
EC35
EC14
EC15
1D05V_VTT
EC37
EC33
EC32
EC111
EC19
EC18
FBVDD
EC13
EC17
EC16
EC5
EC91
EC69
VCC_CORE
EC24
EC23
SC33P50V2JN-3GP
reserve by RF, EMI request 0.1uF stuff in Eng
0119 -1
HM42-CP NV Muxless SA
CPU
34.4GD01.001
HS3
HS4
HS5
STF237R125H42-GP
2ND = 34.4GD01.101
VGA
HS6
HS7
HS8
DIS_Muxless
0120 -1 ME Mike
SPR12
SPR13
SPR14
34.4H602.001
1216 -SC
34.4B417.301 do not approve by factory
vender suggest 34.4B417.401
but 34.4B417.401 can't support engouth sample
before SMT,and spec have to confrim by ME Mike
so Eng stuff 1st(34.4B417.001)
H1
H2
H3
H5
H7
H8
H9
HOLE355X355R111-S1-GP
CB
H4
HOLE335R115-GP
GP
GND1
1214 SC
PCB Footprint = GNDPADSR197-NP
GNDPADSR197-GP
1007 -SA
3G
MINICARD
HS2
HS1
STF256R89H178-GP
34.4B417.001
2ND = 34.4B417.401
UMA
緯創資通
Wistron Corporation
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Title
EMI/Spring/Boss
Size
Document Number
HM42-CP
Rev
SC
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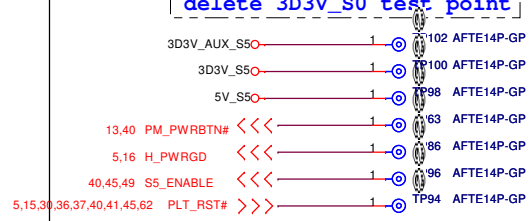
Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AFTE_TP***

Size | Document Number: **HM42-CP** | Rev: **SC**

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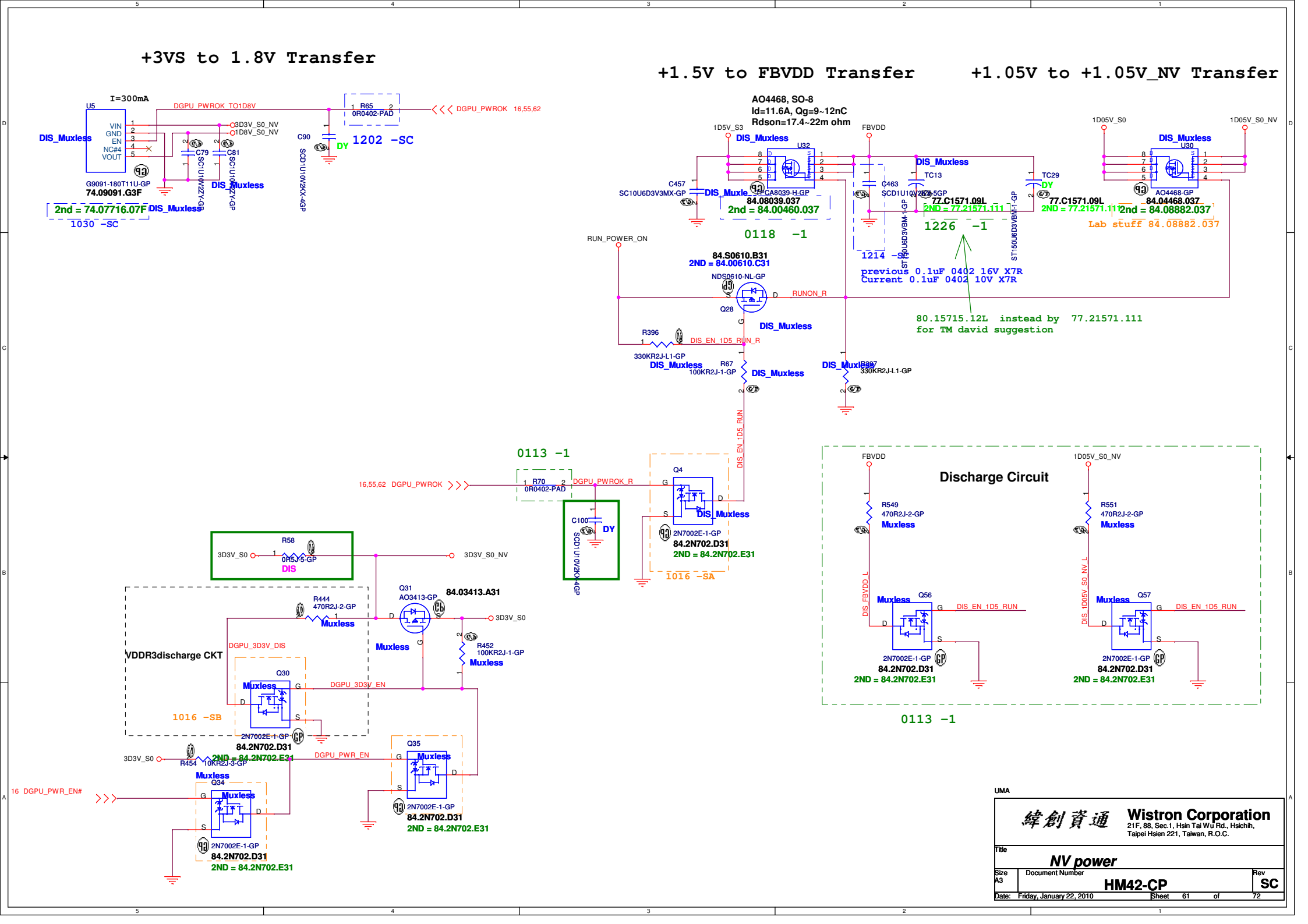

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***NV power***

Size	Document Number	Rev
A3	HM42-CP	SC

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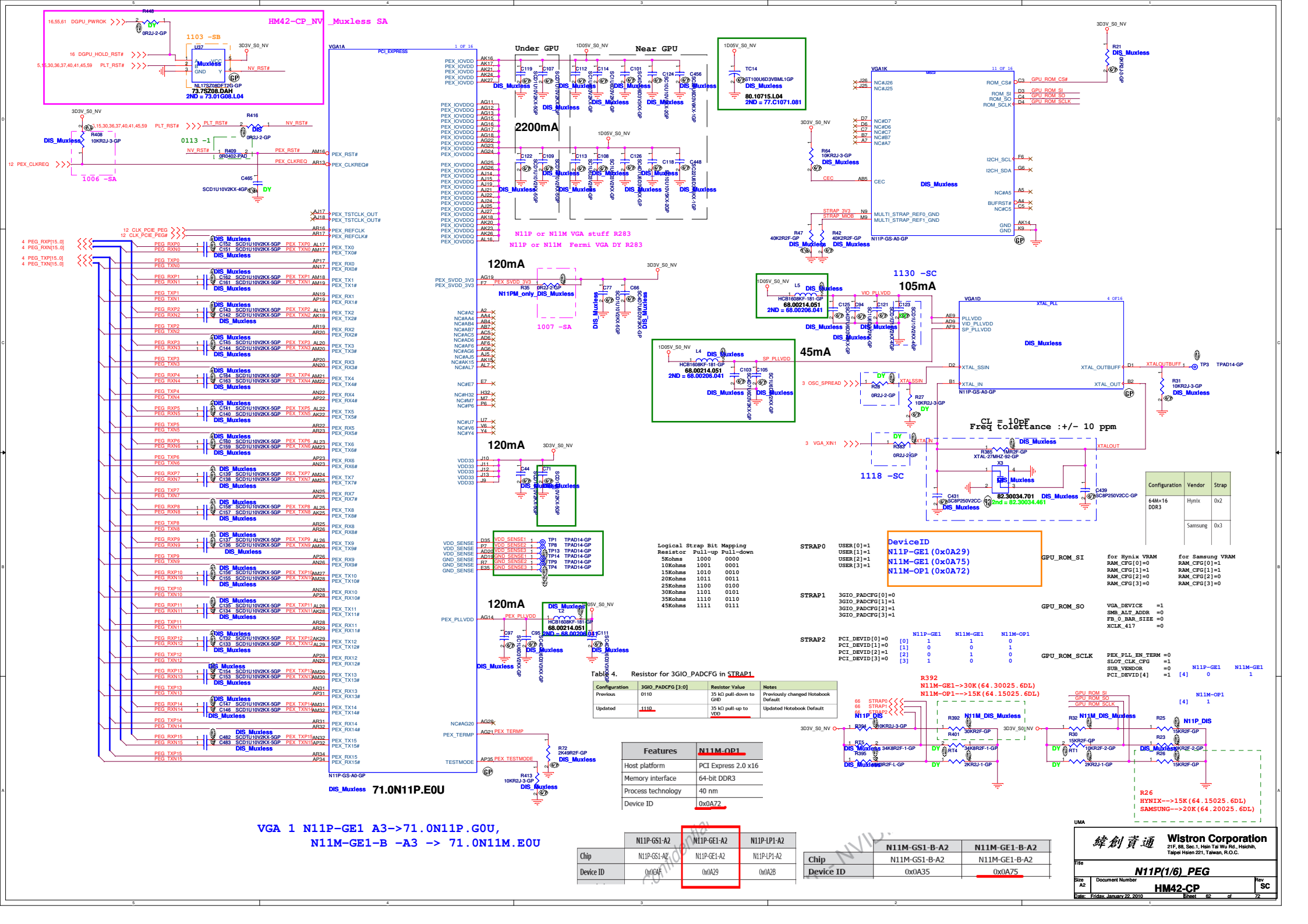

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

STRAP0
USER[0]=1
USER[1]=1
USER[2]=1
USER[3]=1

STRAP1
3GIO_PADCFG[0]=0
3GIO_PADCFG[1]=1
3GIO_PADCFG[2]=1
3GIO_PADCFG[3]=1

STRAP2

	N11P-GE1	N11M-GE1	N11M-OP1
PCI_DEVID[0]=0 [0]	1	1	0
PCI_DEVID[1]=0 [1]	0	0	1
PCI_DEVID[2]=1 [2]	0	1	0
PCI_DEVID[3]=0 [3]	1	0	0

GPU_ROM_SI
for Hynix VRAM
RAM_CFG[0]=0
RAM_CFG[1]=1
RAM_CFG[2]=0
RAM_CFG[3]=0
for Samsung VRAM
RAM_CFG[0]=1
RAM_CFG[1]=1
RAM_CFG[2]=0
RAM_CFG[3]=0

GPU_ROM_SO
VGA_DEVICE =1
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0

GPU_ROM_SCLK
PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1 [4] N11P-GE1 0 N11M-GE1 1 N11M-OP1 1

Configuration	Vendor	Strap
64M×16 DDR3	Hynix	0x2
	Samsung	0x3

Table 4. Resistor for 3GIO_PADCFG in STRAP1

Configuration	3GIO_PADCFG [3:0]	Resistor Value	Notes
Previous	0110	35 kΩ pull-down to GND	Previously changed Notebook Default
Updated	1110	35 kΩ pull-up to VDD	Updated Notebook Default

Features	N11M-OP1
Host platform	PCI Express 2.0 x16
Memory interface	64-bit DDR3
Process technology	40 nm
Device ID	0x0A72

	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Chip	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Device ID	0x0CA0	0x0A29	0x0A2B

	N11M-GS1-B-A2	N11M-GE1-B-A2
Chip	N11M-GS1-B-A2	N11M-GE1-B-A2
Device ID	0x0A35	0x0A75

UMA

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Title: N11P(1/6)_PEG
Size: A2 | Document Number: HM42-CP | Rev: SC
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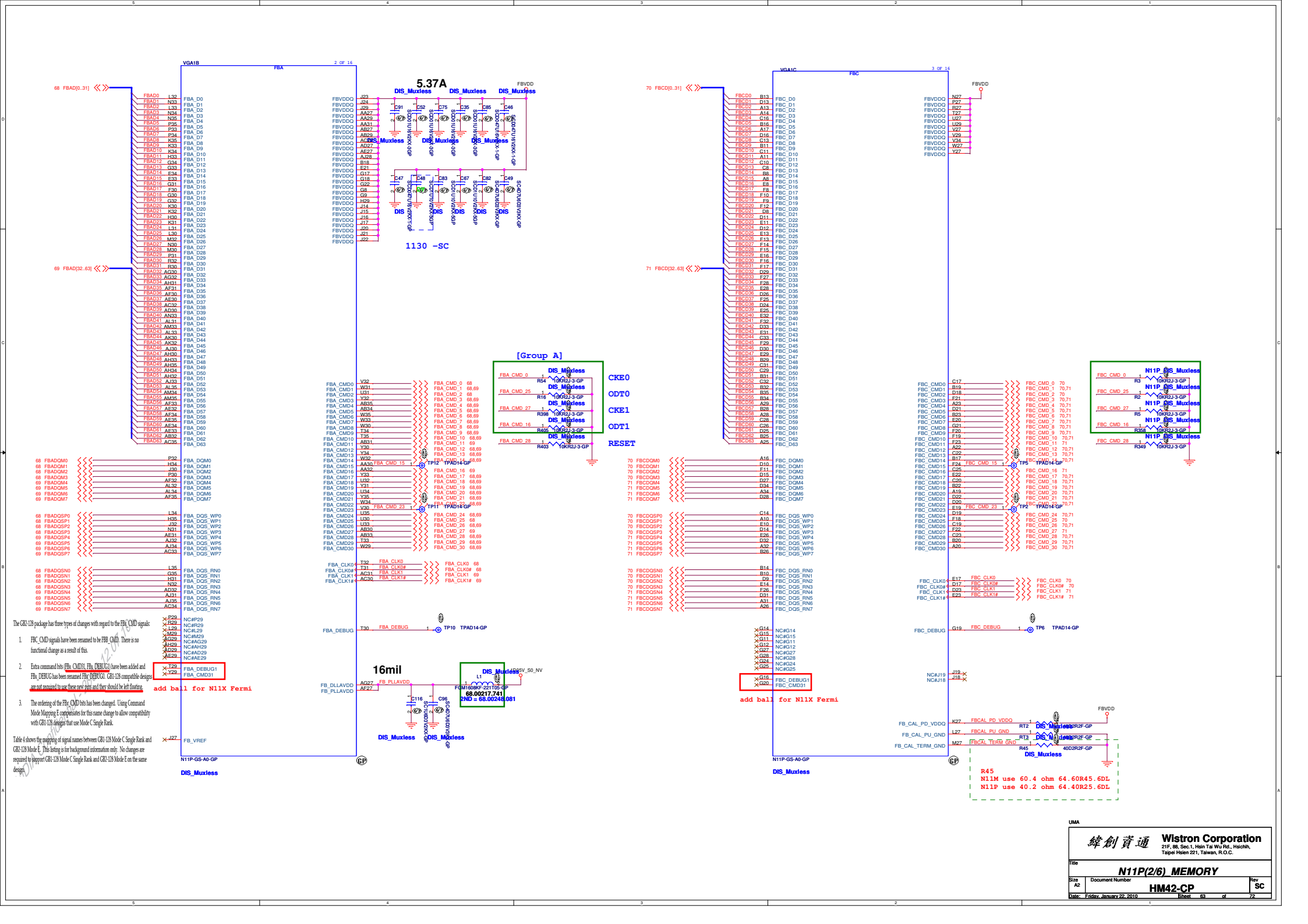
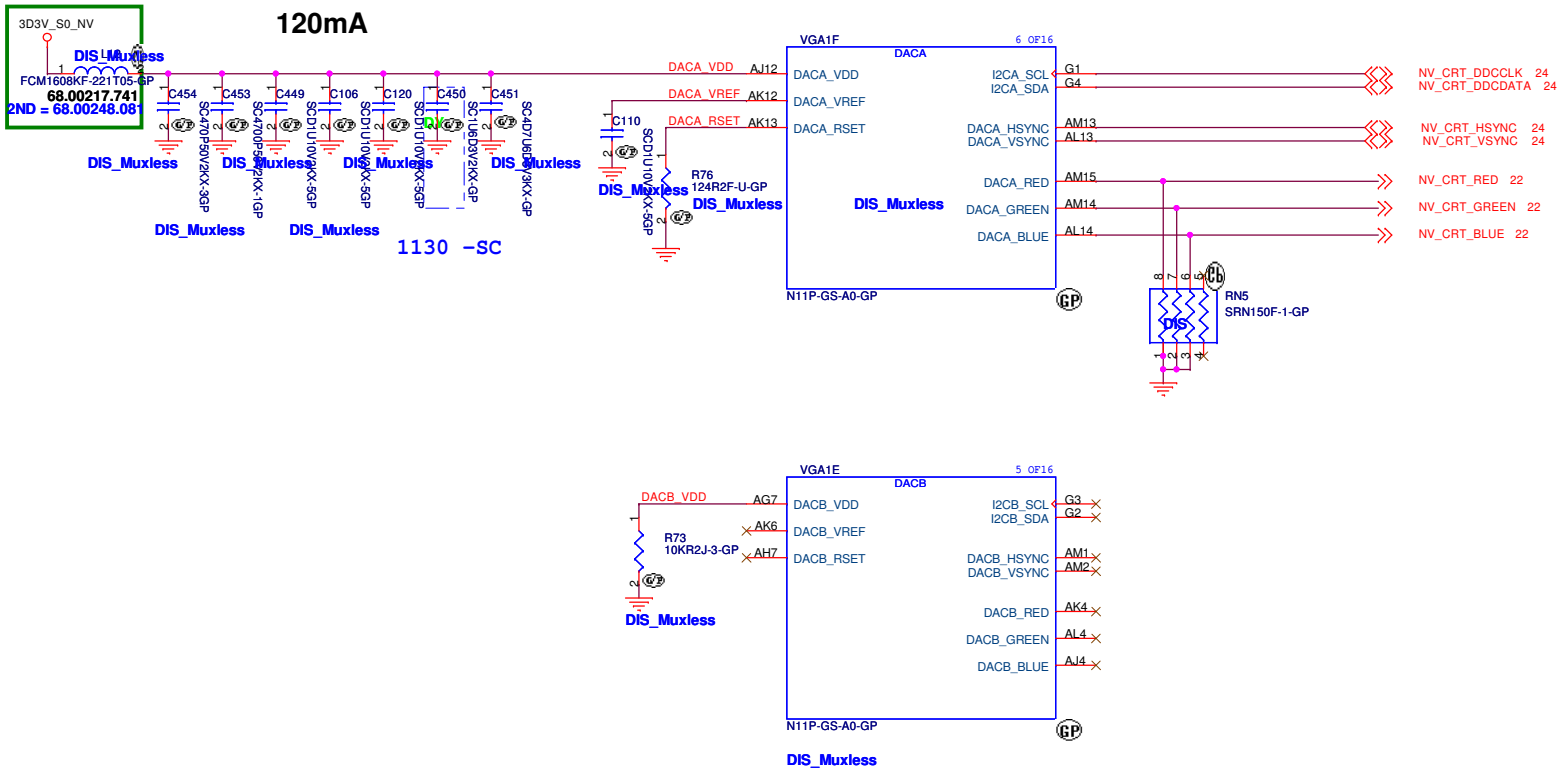
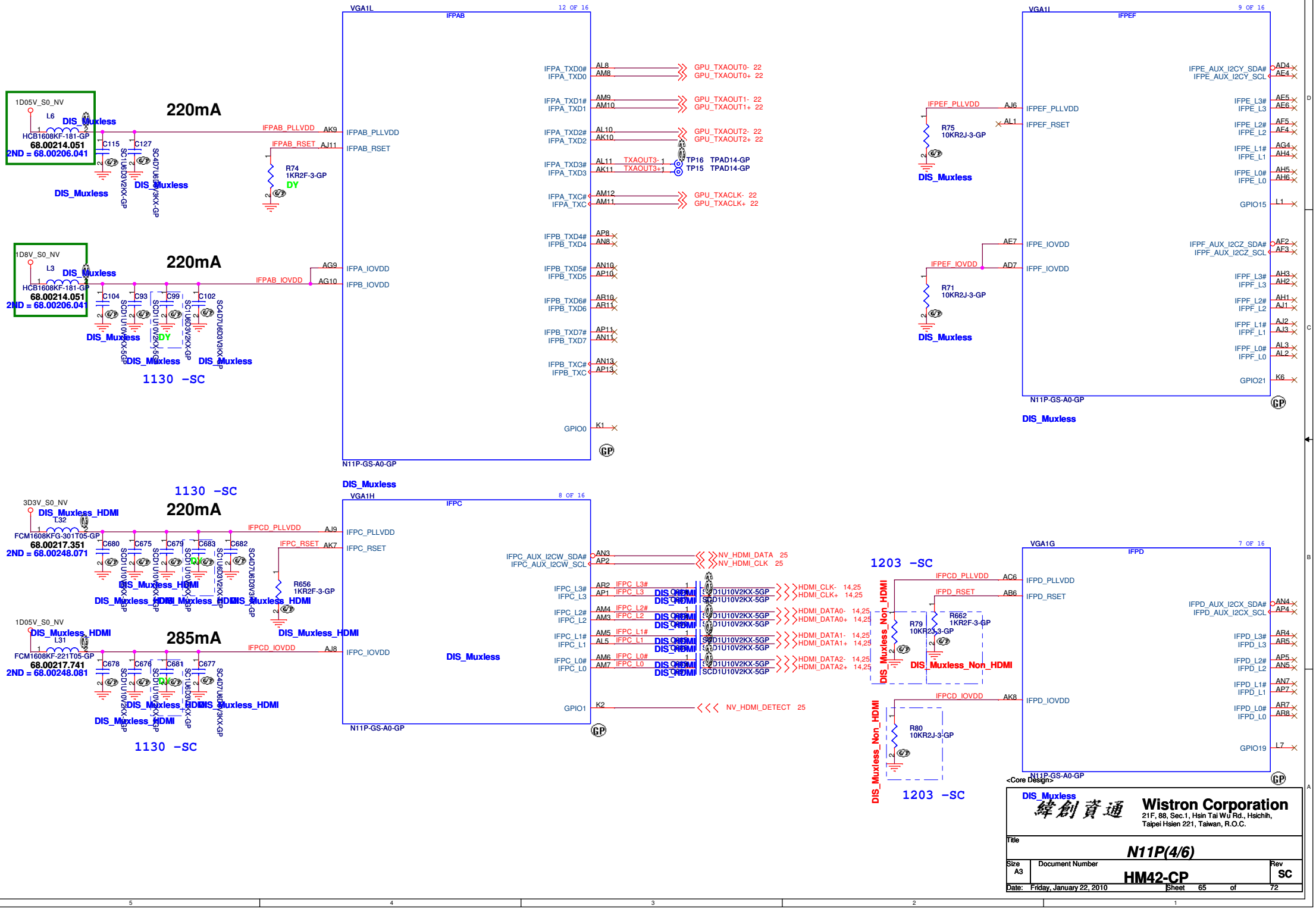

VGA1B
FBA
2 OF 16
68 FBAD[0..31]
69 FBAD[32..63]
FBA_D0
FBA_D1
FBA_D2
FBA_D3
FBA_D4
FBA_D5
FBA_D6
FBA_D7
FBA_D8
FBA_D9
FBA_D10
FBA_D11
FBA_D12
FBA_D13
FBA_D14
FBA_D15
FBA_D16
FBA_D17
FBA_D18
FBA_D19
FBA_D20
FBA_D21
FBA_D22
FBA_D23
FBA_D24
FBA_D25
FBA_D26
FBA_D27
FBA_D28
FBA_D29
FBA_D30
FBA_D31
FBA_D32
FBA_D33
FBA_D34
FBA_D35
FBA_D36
FBA_D37
FBA_D38
FBA_D39
FBA_D40
FBA_D41
FBA_D42
FBA_D43
FBA_D44
FBA_D45
FBA_D46
FBA_D47
FBA_D48
FBA_D49
FBA_D50
FBA_D51
FBA_D52
FBA_D53
FBA_D54
FBA_D55
FBA_D56
FBA_D57
FBA_D58
FBA_D59
FBA_D60
FBA_D61
FBA_D62
FBA_D63
68 FBADQM0
68 FBADQM1
68 FBADQM2
68 FBADQM3
69 FBADQM4
69 FBADQM5
69 FBADQM6
69 FBADQM7
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
68 FBADQSP0
68 FBADQSP1
68 FBADQSP2
68 FBADQSP3
69 FBADQSP4
69 FBADQSP5
69 FBADQSP6
69 FBADQSP7
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
68 FBADQSN0
68 FBADQSN1
68 FBADQSN2
68 FBADQSN3
69 FBADQSN4
69 FBADQSN5
69 FBADQSN6
69 FBADQSN7
FBA_DQS_RN0
FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7
NC#P29
NC#R29
NC#L29
NC#M29
NC#AG29
NC#AH29
NC#AD29
NC#AE29
FBA_DEBUG1
FBA_CMD31
FB_VREF
N11P-GS-A0-GP
DIS_Muxless
FBVDD
5.37A
DIS_Muxless
1130 -SC
FBVDDQ
FBVDDO
[Group A]
FBA_CMD_0
FBA_CMD_25
FBA_CMD_27
FBA_CMD_16
FBA_CMD_28
R54 10KR2J-3-GP
R16 10KR2J-3-GP
R398 10KR2J-3-GP
R405 10KR2J-3-GP
R403 10KR2J-3-GP
CKE0
ODT0
CKE1
ODT1
RESET
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
FBA_CMD27
FBA_CMD28
FBA_CMD29
FBA_CMD30
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
FBA_DEBUG
TP12 TPAD14-GP
TP11 TPAD14-GP
TP10 TPAD14-GP
16mil
FB_PLLAVDD
FB_DLLAVDD
FCM1608KF-221T05-GP
68.00217.741
2ND = 68.00248.081
1.5V_S0_NV
C116
C96
DIS_Muxless
add ball for N11X Fermi
The GB2-128 package has three types of changes with regard to the FBx_CMD signals:
1. FBC_CMD signals have been renamed to be FBB_CMD. There is no functional change as a result of this.
2. Extra command bits (FBx_CMD51, FBx_DEBUG1) have been added and FBx_DEBUG has been renamed FBx_DEBUG1. GB1-128 compatible designs are not required to use these new pins and they should be left floating.
3. The ordering of the FBx_CMD bits has been changed. Using Command Mode Mapping E compensates for this name change to allow compatibility with GB1-128 designs that use Mode C Single Rank.
Table 4 shows the mapping of signal names between GB1-128 Mode C Single Rank and GB2-128 Mode E. This listing is for background information only. No changes are required to support GB1-128 Mode C Single Rank and GB2-128 Mode E on the same design.
VGA1C
FBC
3 OF 16
70 FBCD[0..31]
71 FBCD[32..63]
FBC_D0
FBC_D1
FBC_D2
FBC_D3
FBC_D4
FBC_D5
FBC_D6
FBC_D7
FBC_D8
FBC_D9
FBC_D10
FBC_D11
FBC_D12
FBC_D13
FBC_D14
FBC_D15
FBC_D16
FBC_D17
FBC_D18
FBC_D19
FBC_D20
FBC_D21
FBC_D22
FBC_D23
FBC_D24
FBC_D25
FBC_D26
FBC_D27
FBC_D28
FBC_D29
FBC_D30
FBC_D31
FBC_D32
FBC_D33
FBC_D34
FBC_D35
FBC_D36
FBC_D37
FBC_D38
FBC_D39
FBC_D40
FBC_D41
FBC_D42
FBC_D43
FBC_D44
FBC_D45
FBC_D46
FBC_D47
FBC_D48
FBC_D49
FBC_D50
FBC_D51
FBC_D52
FBC_D53
FBC_D54
FBC_D55
FBC_D56
FBC_D57
FBC_D58
FBC_D59
FBC_D60
FBC_D61
FBC_D62
FBC_D63
70 FBCDQM0
70 FBCDQM1
70 FBCDQM2
70 FBCDQM3
71 FBCDQM4
71 FBCDQM5
71 FBCDQM6
71 FBCDQM7
FBC_DQM0
FBC_DQM1
FBC_DQM2
FBC_DQM3
FBC_DQM4
FBC_DQM5
FBC_DQM6
FBC_DQM7
70 FBCDQSP0
70 FBCDQSP1
70 FBCDQSP2
70 FBCDQSP3
71 FBCDQSP4
71 FBCDQSP5
71 FBCDQSP6
71 FBCDQSP7
FBC_DQS_WP0
FBC_DQS_WP1
FBC_DQS_WP2
FBC_DQS_WP3
FBC_DQS_WP4
FBC_DQS_WP5
FBC_DQS_WP6
FBC_DQS_WP7
70 FBCDQSN0
70 FBCDQSN1
70 FBCDQSN2
70 FBCDQSN3
71 FBCDQSN4
71 FBCDQSN5
71 FBCDQSN6
71 FBCDQSN7
FBC_DQS_RN0
FBC_DQS_RN1
FBC_DQS_RN2
FBC_DQS_RN3
FBC_DQS_RN4
FBC_DQS_RN5
FBC_DQS_RN6
FBC_DQS_RN7
NC#G14
NC#G15
NC#G11
NC#G12
NC#G27
NC#G28
NC#G24
NC#G25
FBC_DEBUG1
FBC_CMD31
N11P-GS-A0-GP
DIS_Muxless
FBVDDQ
FBC_CMD0
FBC_CMD1
FBC_CMD2
FBC_CMD3
FBC_CMD4
FBC_CMD5
FBC_CMD6
FBC_CMD7
FBC_CMD8
FBC_CMD9
FBC_CMD10
FBC_CMD11
FBC_CMD12
FBC_CMD13
FBC_CMD14
FBC_CMD15
FBC_CMD16
FBC_CMD17
FBC_CMD18
FBC_CMD19
FBC_CMD20
FBC_CMD21
FBC_CMD22
FBC_CMD23
FBC_CMD24
FBC_CMD25
FBC_CMD26
FBC_CMD27
FBC_CMD28
FBC_CMD29
FBC_CMD30
FBC_CLK0
FBC_CLK0#
FBC_CLK1
FBC_CLK1#
FBC_DEBUG
TP5 TPAD14-GP
TP2 TPAD14-GP
TP6 TPAD14-GP
N11P_DIS_Muxless
R3 10KR2J-3-GP
R2 10KR2J-3-GP
R5 10KR2J-3-GP
R358 10KR2J-3-GP
R349 10KR2J-3-GP
add ball for N11X Fermi
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
RT2 40D2R2F-GP
RT3 40D2R2F-GP
R45 40D2R2F-GP
R45
N11M use 60.4 ohm 64.60R45.6DL
N11P use 40.2 ohm 64.40R25.6DL
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N11P(2/6)_MEMORY
Size
A2
Document Number
HM42-CP
Rev
SC
Date: Friday, January 22, 2010
Sheet 63 of 72



Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *N11P(3/6)_DAC*		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 64 of 72	


VGA1L
IFPAB
12 OF 16
N11P-GS-A0-GP
1D05V_S0_NV
220mA
L6
HCB1608KF-181-GP
68.00214.051
2ND = 68.00206.041
DIS_Muxless
C115
C127
IFPAB_PLLVDD
IFPAB_RSET
R74
1KR2F-3-GP
DY
1D8V_S0_NV
L3
C104
C93
C99
C102
IFPAB_IOVDD
1130 -SC
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPA_TXC#
IFPA_TXC
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
IFPB_TXC#
IFPB_TXC
GPIO0
GPU_TXAOUT0- 22
GPU_TXAOUT0+ 22
GPU_TXAOUT1- 22
GPU_TXAOUT1+ 22
GPU_TXAOUT2- 22
GPU_TXAOUT2+ 22
TXAOUT3-
TXAOUT3+
TP16 TPAD14-GP
TP15 TPAD14-GP
GPU_TXACLK- 22
GPU_TXACLK+ 22
VGA1H
IFPC
8 OF 16
3D3V_S0_NV
DIS_Muxless_HDMI
L32
FCM1608KFG-301T05-GP
68.00217.351
2ND = 68.00248.071
C680
C675
C679
C683
C682
IFPCD_PLLVDD
IFPC_RSET
R656
1KR2F-3-GP
1130 -SC
1D05V_S0_NV
285mA
L31
FCM1608KF-221T05-GP
68.00217.741
2ND = 68.00248.081
C678
C676
C681
C677
IFPCD_IOVDD
IFPC_PLLVDD
IFPC_RSET
IFPC_IOVDD
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
IFPC_L3#
IFPC_L3
IFPC_L2#
IFPC_L2
IFPC_L1#
IFPC_L1
IFPC_L0#
IFPC_L0
GPIO1
NV_HDMI_DATA 25
NV_HDMI_CLK 25
NV_HDMI_DETECT 25
HDMI_CLK- 14,25
HDMI_CLK+ 14,25
HDMI_DATA0- 14,25
HDMI_DATA0+ 14,25
HDMI_DATA1- 14,25
HDMI_DATA1+ 14,25
HDMI_DATA2- 14,25
HDMI_DATA2+ 14,25
VGA1I
IFPEF
9 OF 16
N11P-GS-A0-GP
IFPEF_PLLVDD
IFPEF_RSET
IFPEF_IOVDD
R75
10KR2J-3-GP
R71
10KR2J-3-GP
IFPE_IOVDD
IFPF_IOVDD
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
IFPE_L3#
IFPE_L3
IFPE_L2#
IFPE_L2
IFPE_L1#
IFPE_L1
IFPE_L0#
IFPE_L0
GPIO15
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
IFPF_L3#
IFPF_L3
IFPF_L2#
IFPF_L2
IFPF_L1#
IFPF_L1
IFPF_L0#
IFPF_L0
GPIO21
1203 -SC
VGA1G
IFPD
7 OF 16
N11P-GS-A0-GP
IFPCD_PLLVDD
IFPD_RSET
IFPCD_IOVDD
R79
10KR2J-3-GP
R662
1KR2F-3-GP
R80
10KR2J-3-GP
DIS_Muxless_Non_HDMI
IFPD_PLLVDD
IFPD_IOVDD
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
IFPD_L3#
IFPD_L3
IFPD_L2#
IFPD_L2
IFPD_L1#
IFPD_L1
IFPD_L0#
IFPD_L0
GPIO19
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N11P(4/6)
Size A3
Document Number
HM42-CP
Rev SC
Date: Friday, January 22, 2010
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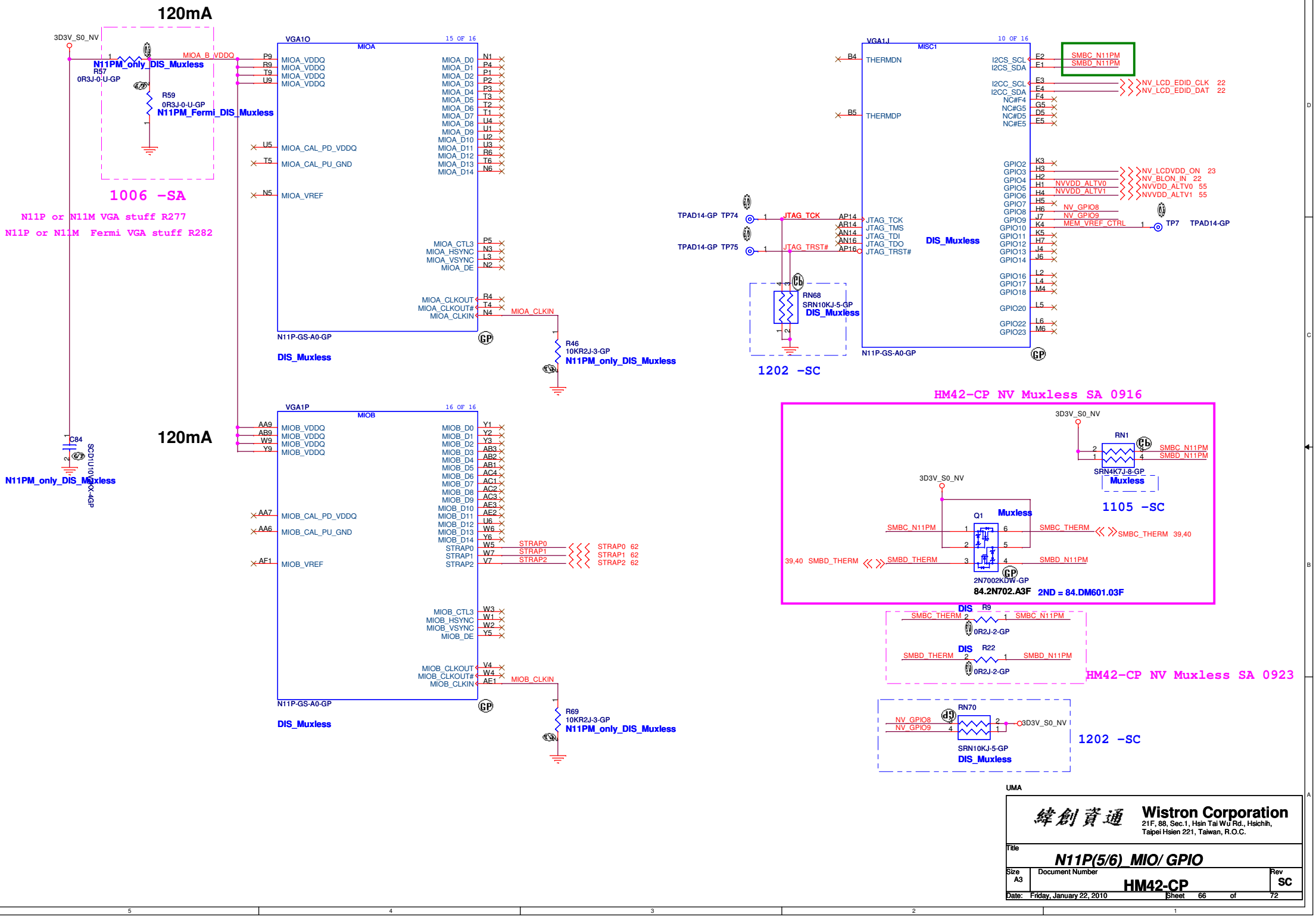
120mA
3D3V_S0_NV
MIOA_B_VDDQ
N11PM_only_DIS_Muxless
R57
0R3J-0-U-GP
R59
0R3J-0-U-GP
N11PM_Fermi_DIS_Muxless
1006 -SA
N11P or N11M VGA stuff R277
N11P or N11M Fermi VGA stuff R282
VGA1O
MIOA
15 OF 16
MIOA_VDDQ
MIOA_CAL_PD_VDDQ
MIOA_CAL_PU_GND
MIOA_VREF
MIOA_CTL3
MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
MIOA_CLKOUT
MIOA_CLKOUT#
MIOA_CLKIN
MIOA_D0
MIOA_D1
MIOA_D2
MIOA_D3
MIOA_D4
MIOA_D5
MIOA_D6
MIOA_D7
MIOA_D8
MIOA_D9
MIOA_D10
MIOA_D11
MIOA_D12
MIOA_D13
MIOA_D14
N11P-GS-A0-GP
DIS_Muxless
R46
10KR2J-3-GP
N11PM_only_DIS_Muxless
C84
SCD1U10V2KX-4GP
N11PM_only_DIS_Muxless
120mA
VGA1P
MIOB
16 OF 16
MIOB_VDDQ
MIOB_CAL_PD_VDDQ
MIOB_CAL_PU_GND
MIOB_VREF
MIOB_CTL3
MIOB_HSYNC
MIOB_VSYNC
MIOB_DE
MIOB_CLKOUT
MIOB_CLKOUT#
MIOB_CLKIN
MIOB_D0
MIOB_D1
MIOB_D2
MIOB_D3
MIOB_D4
MIOB_D5
MIOB_D6
MIOB_D7
MIOB_D8
MIOB_D9
MIOB_D10
MIOB_D11
MIOB_D12
MIOB_D13
MIOB_D14
STRAP0
STRAP1
STRAP2
STRAP0 62
STRAP1 62
STRAP2 62
N11P-GS-A0-GP
DIS_Muxless
R69
10KR2J-3-GP
N11PM_only_DIS_Muxless
VGA1J
MISC1
10 OF 16
THERMDN
THERMDP
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
SMBC_N11PM
SMBD_N11PM
NV_LCD_EDID_CLK 22
NV_LCD_EDID_DAT 22
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO16
GPIO17
GPIO18
GPIO20
GPIO22
GPIO23
NV_LCDVDD_ON 23
NV_BLON_IN 22
NVVDD_ALTV0
NVVDD_ALTV0 55
NVVDD_ALTV1
NVVDD_ALTV1 55
NV_GPIO8
NV_GPIO9
MEM_VREF_CTRL
TP7 TPAD14-GP
TPAD14-GP TP74
TPAD14-GP TP75
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
RN68
SRN10KJ-5-GP
DIS_Muxless
N11P-GS-A0-GP
1202 -SC
HM42-CP NV Muxless SA 0916
3D3V_S0_NV
RN1
SRN4K7J-8-GP
Muxless
1105 -SC
Q1
Muxless
SMBC_N11PM
SMBD_N11PM
SMBC_THERM
SMBD_THERM
SMBC_THERM 39,40
SMBD_THERM 39,40
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
DIS
R9
0R2J-2-GP
R22
0R2J-2-GP
HM42-CP NV Muxless SA 0923
RN70
NV_GPIO8
NV_GPIO9
SRN10KJ-5-GP
DIS_Muxless
1202 -SC
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N11P(5/6)_MIO/ GPIO
Size
A3
Document Number
HM42-CP
Rev
SC
Date: Friday, January 22, 2010
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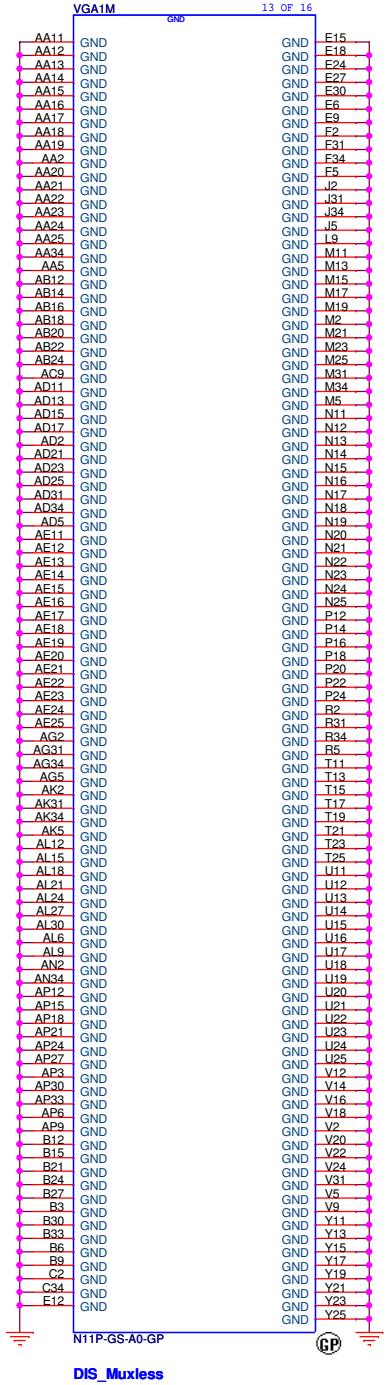

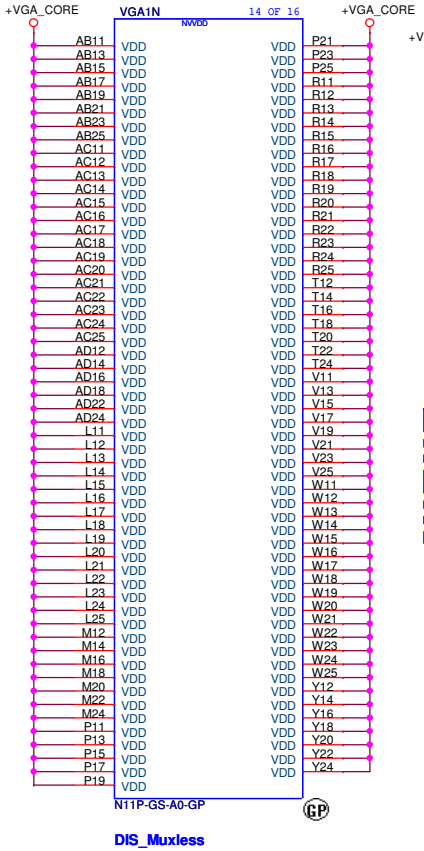

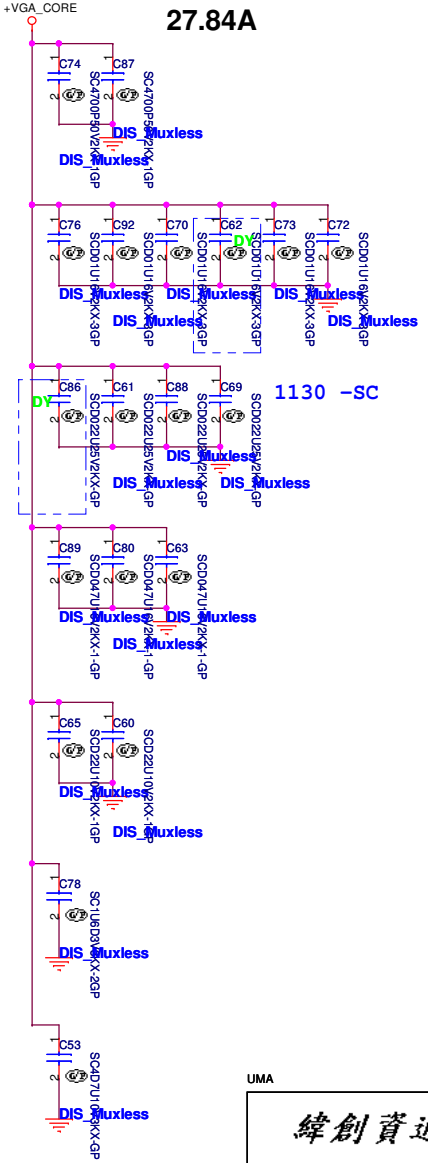

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N11P(6/6)_POWER

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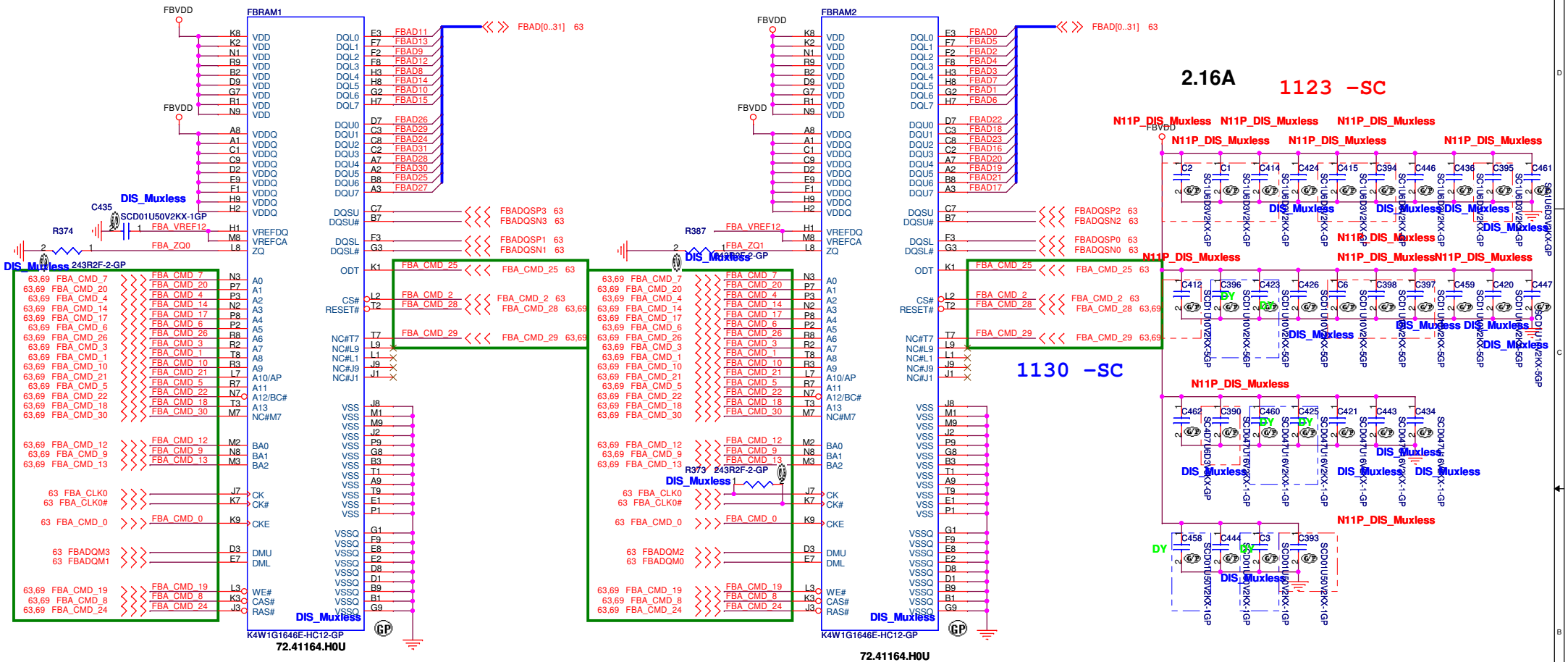
DDR3



SAMSUNG: 72.41164.H0U(Use OEM PN:VR.1GB0B.006)
HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	VRAM(1/4)	
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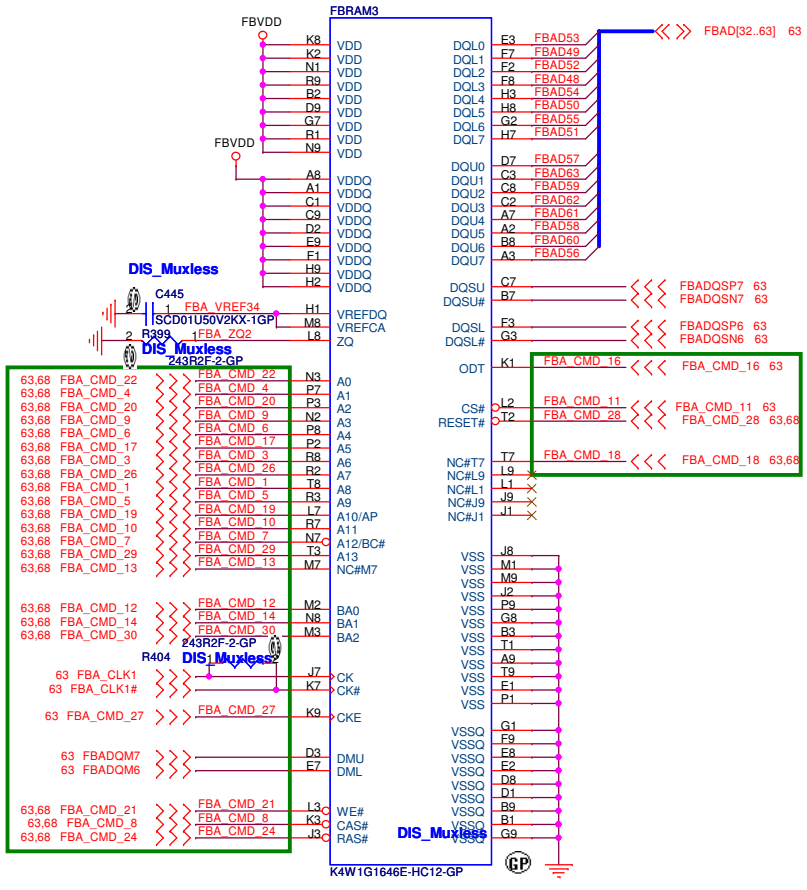
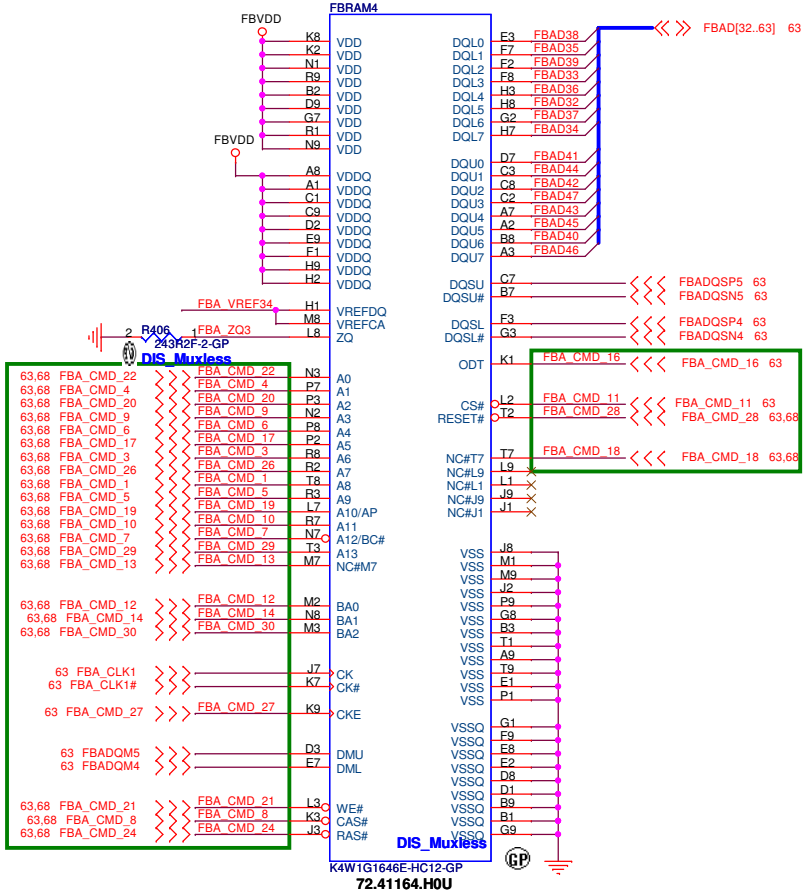
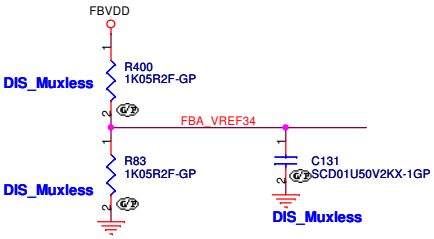
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



HM42-CP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM(2/4)*	
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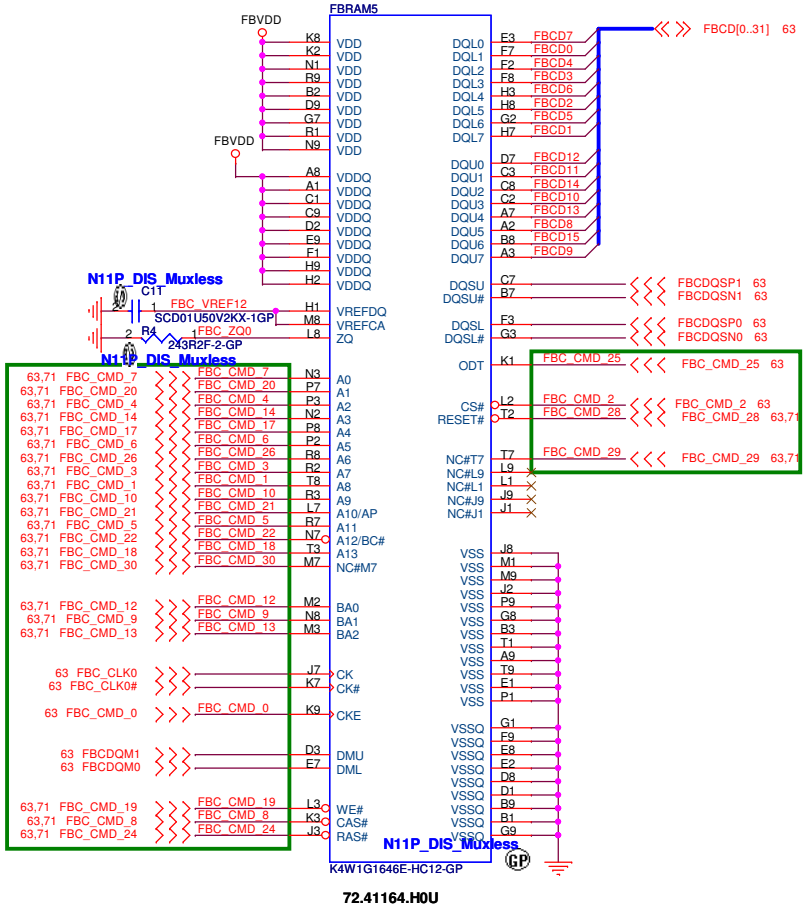
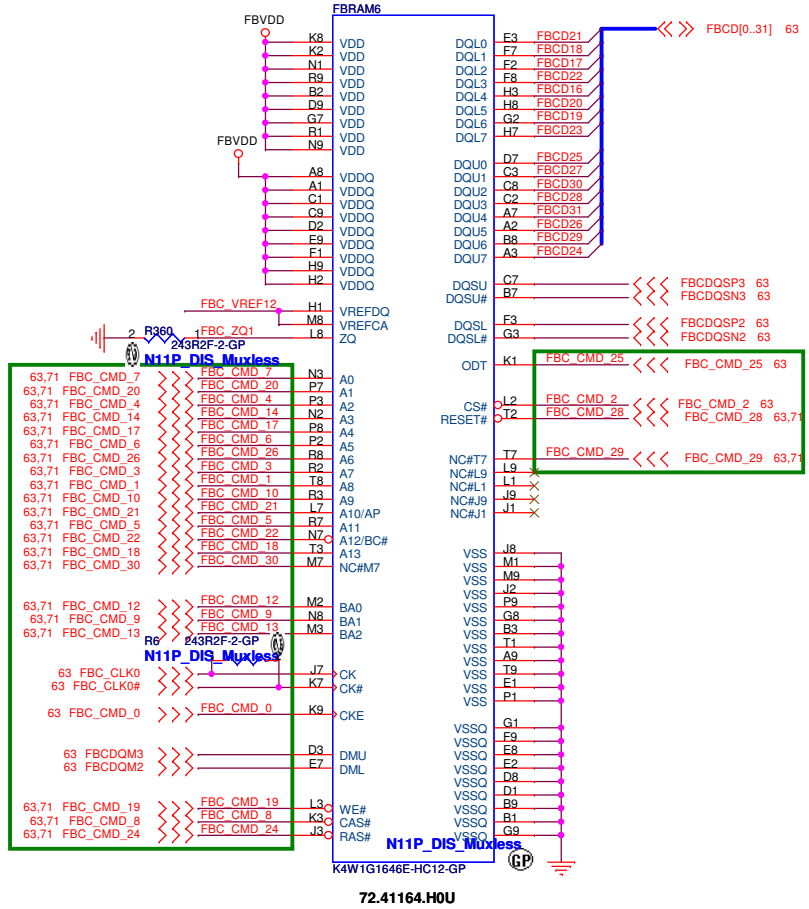
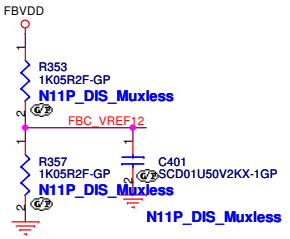
DDR3





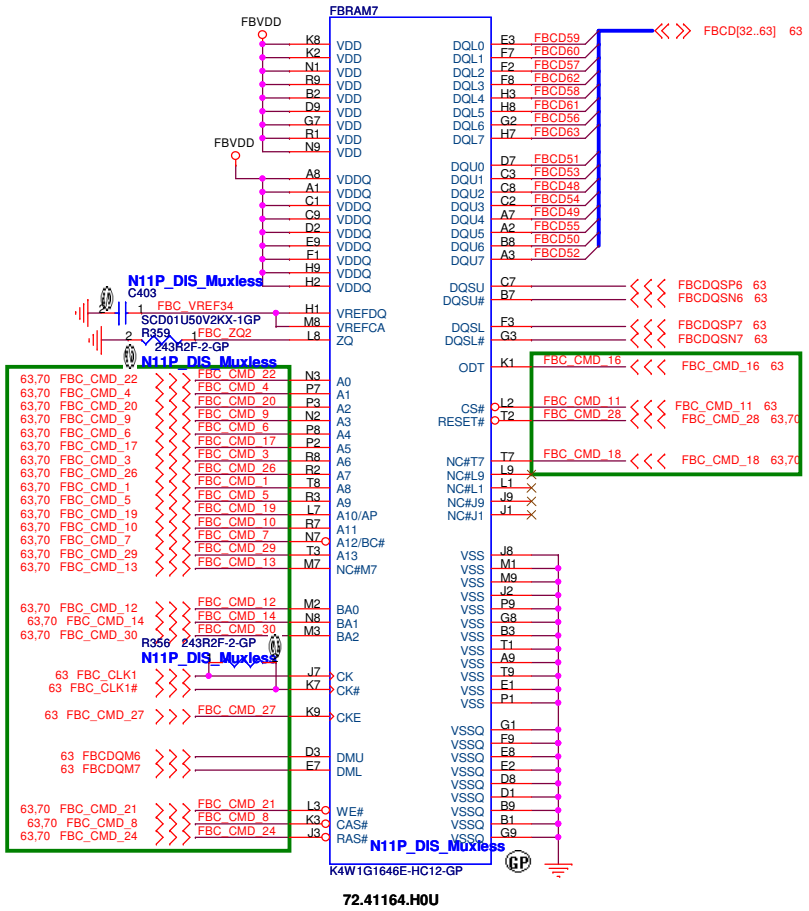
SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

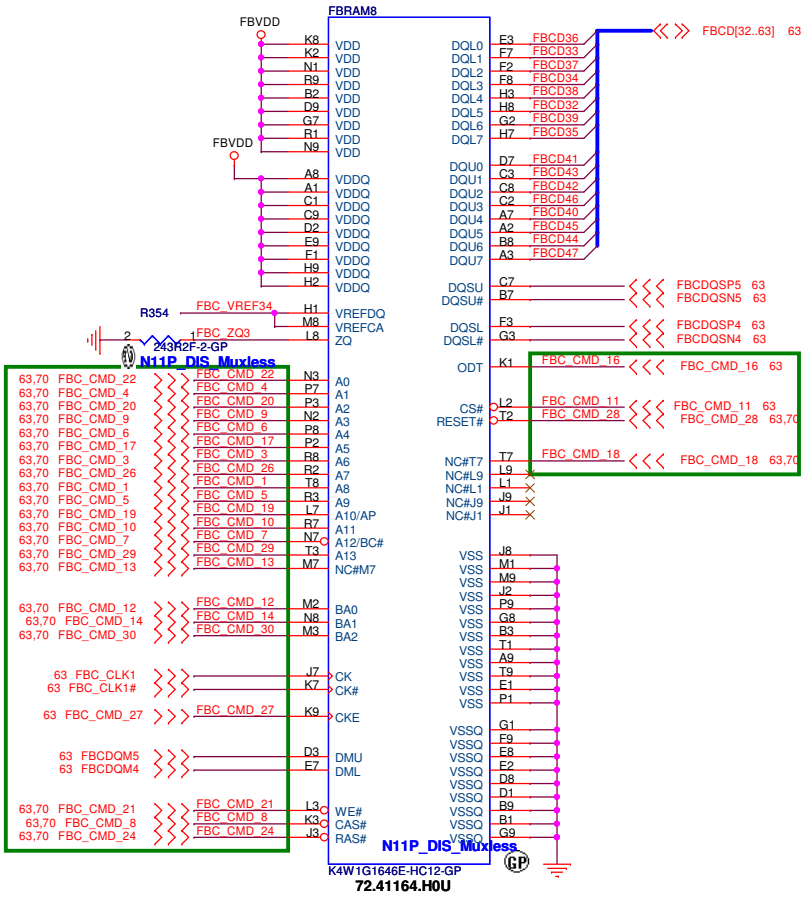


HM42-CP

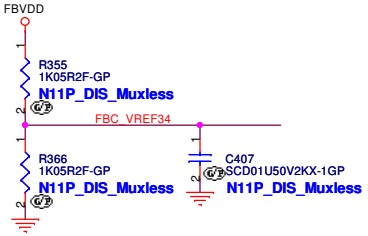
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(3/4)***	
Size A3	Document Number **HM42-CP**	Rev SC
Date: Friday, January 22, 2010	Sheet 70 of 72	

DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(4/4)***

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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006
Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[lab -SB]

2nd -> UMA (S01G)

1st -> Diserete N11P Hynix(S02G)
1st +3rd -> Diserete N11M Hynix(S03G)
2nd +4th -> Diserete N11M Samsung(S04G)
1st -> Diserete N11P Samsung (S05G)

2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]

2nd -> UMA Non 3G (55.4GY01.S07G)

1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)
1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)
2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)
1st + 5th -> Diserete N11P Samsung _3G(55.4GY01.S10G)
1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]

UMA 3G (55.4GY01.M01G)
Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st
Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd
UMA Non 3G (55.4GY01.M04G)
Diserete N11M Hynix_3G(55.4GY01.M05G)
Diserete N11P Samsung _3G(55.4GY01.M06G) =>1 st
Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]

qual TPCN1 2nd source(20.K0296.006)
qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd

qual ODD1 3rd source(62.10065.E01)

qual PWRCN1 2nd and 3rd
qual RTC1 4th source
qual BT1 2nd and 3 source

[Old]
PCH1 PN : 71.0IBEX.A0U
[New]
PCH1 PN : 71.0HM55.00U(KI.G5501.002)

qual U51 and U15 2nd source
qual TC13 2nd source(77.21571.111)
qual U32 2nd source
Qual HS1,HS2 2nd: 34.4B417.401

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Modify History
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