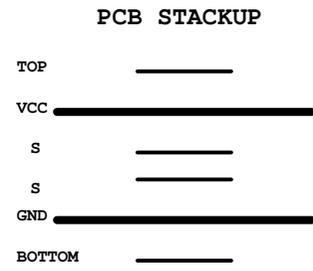
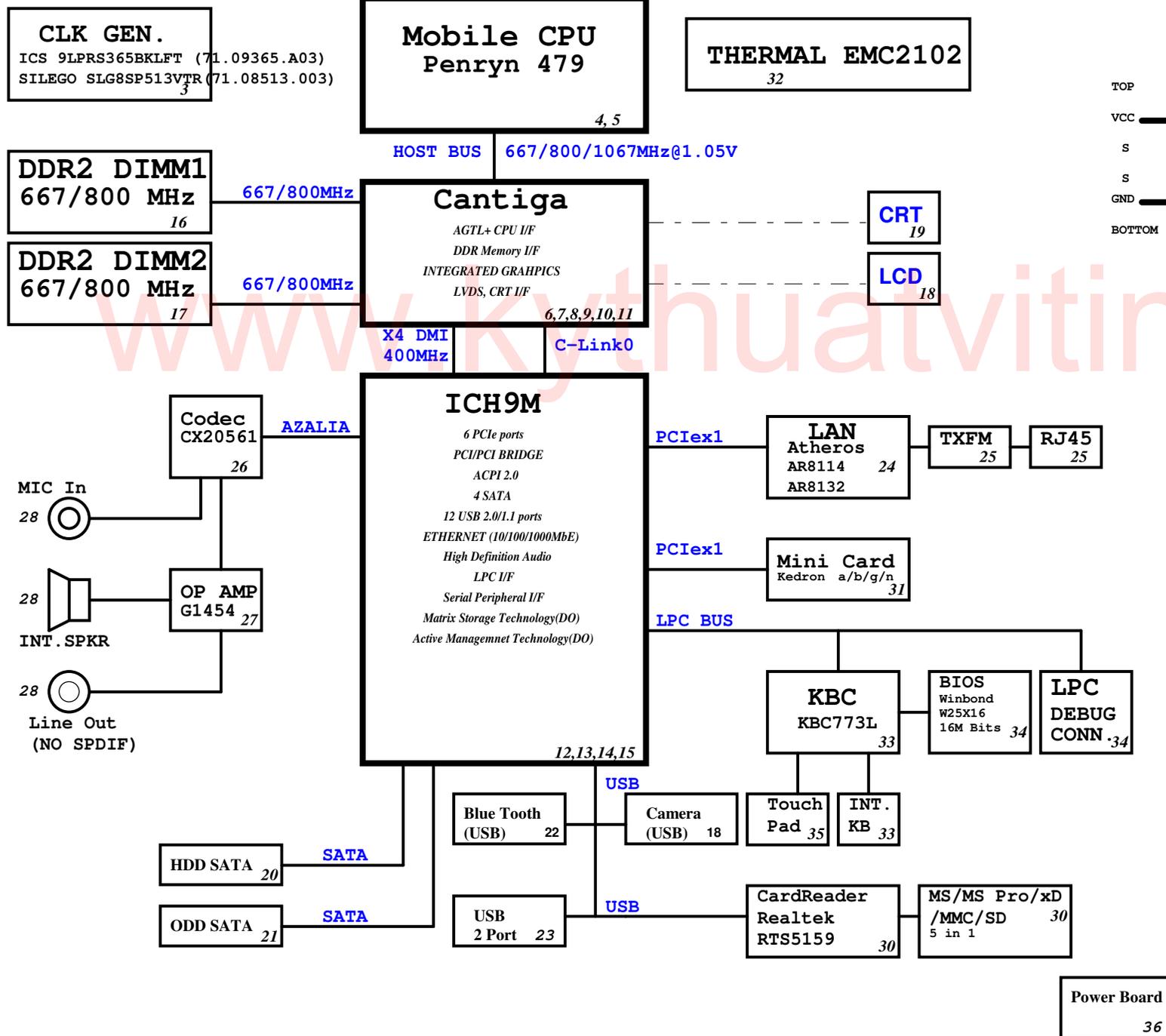


# HM40-MV Block Diagram

Project code: 91.4BW01.001  
 PCB P/N : 48.4BW01.0SB  
 REVISION : 08242-SB



SYSTEM DC/DC TPS51125 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC TPS51124 44	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026	43
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3
RT9018A	43
1D8V_S3	1D5V_S0
CPU DC/DC ISL6266A 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V
CHARGER BQ24745 46	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

UMA Two Phase 2

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size A3 Document Number **HM40-MV** Rev SB

Date: Monday, November 24, 2008 Sheet 1 of 51

# ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

# ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation(Default): Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALL2 mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode[MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

### NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

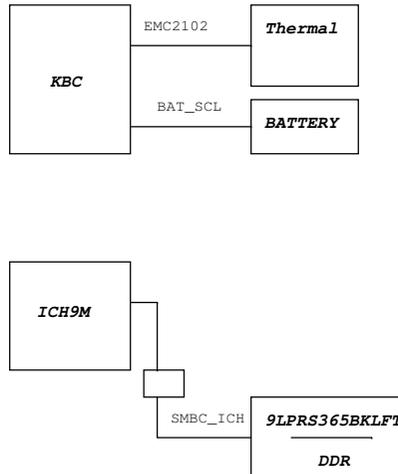
## USB Table

USB	
Pair	Device
0	USB1
1	NC
2	NC
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	Bluetooth
8	NC
9	USB2 (High speed)
10	NC
11	CardReader

## PCIE Routing

LANE1	LAN Atheros AR8114A
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NC
LANE6	NC

## SMBus



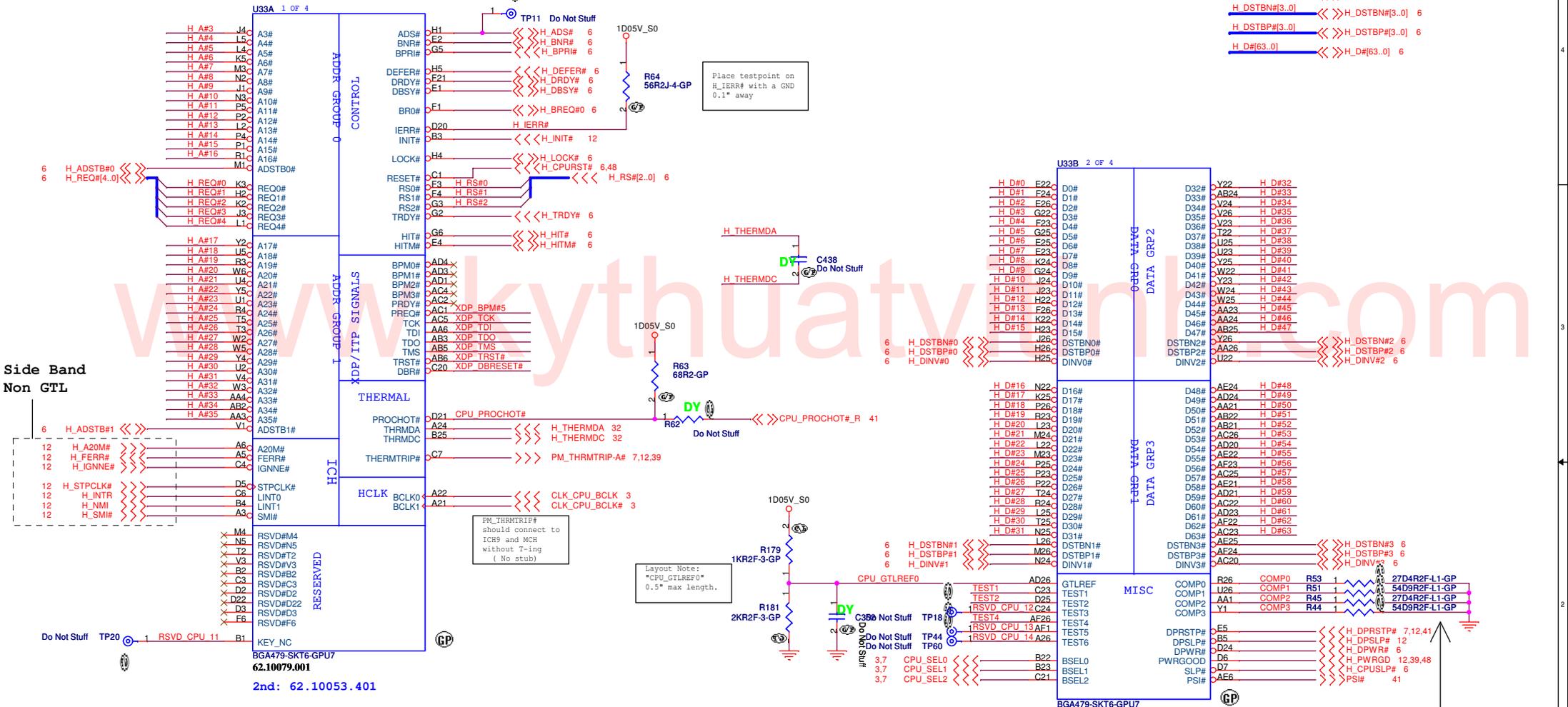
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<b>Reference</b>			
Size A3	Document Number	Rev	
	<b>HM40-MV</b>	<b>SB</b>	
Date:	Monday, November 24, 2008	Sheet	2 of 51



6 H\_A#(35..3) <<<>> H\_A#(35..3)

H\_DINV#(3..0) <<>> H\_DINV#(3..0) 6  
H\_DSTBN#(3..0) <<>> H\_DSTBN#(3..0) 6  
H\_DSTBP#(3..0) <<>> H\_DSTBP#(3..0) 6  
H\_D#(63..0) <<>> H\_D#(63..0) 6



Side Band  
Non GTL

6 H\_ADSTB#0 <<>> H\_REQ#(4..0) 6  
6 H\_ADSTB#1 <<>> H\_A#(35..3) 6  
12 H\_A20M# <<>> A20M# 12  
12 H\_FERR# <<>> FERR# 12  
12 H\_IGNNE# <<>> IGNNE# 12  
12 H\_STPCLK# <<>> STPCLK# 12  
12 H\_INTR# <<>> LINT0 12  
12 H\_NMI# <<>> LINT1 12  
12 H\_SMI# <<>> SMI# 12

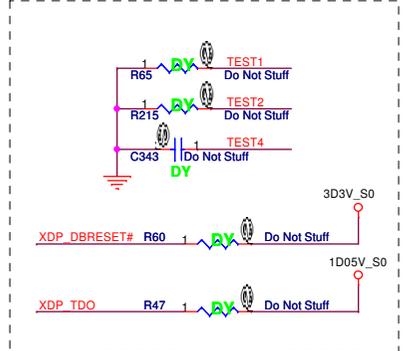
M4 RSVD#M4  
N5 RSVD#N5  
T2 RSVD#T2  
V3 RSVD#V3  
C3 RSVD#C3  
D2 RSVD#D2  
D22 RSVD#D22  
D3 RSVD#D3  
D6 RSVD#D6

Do Not Stuff TP20 1 RSVD\_CPU\_11 B1  
BGA479-SKT6-GPU7  
62.10079.001  
2nd: 62.10053.401

Layout Note:  
\*CPU\_GTLREF0\*  
0.5" max length.

PM\_THRMTRIP#  
should connect to  
ICH9 and MCH  
without T-ling  
(No stub)

### Follow Demo Circuit



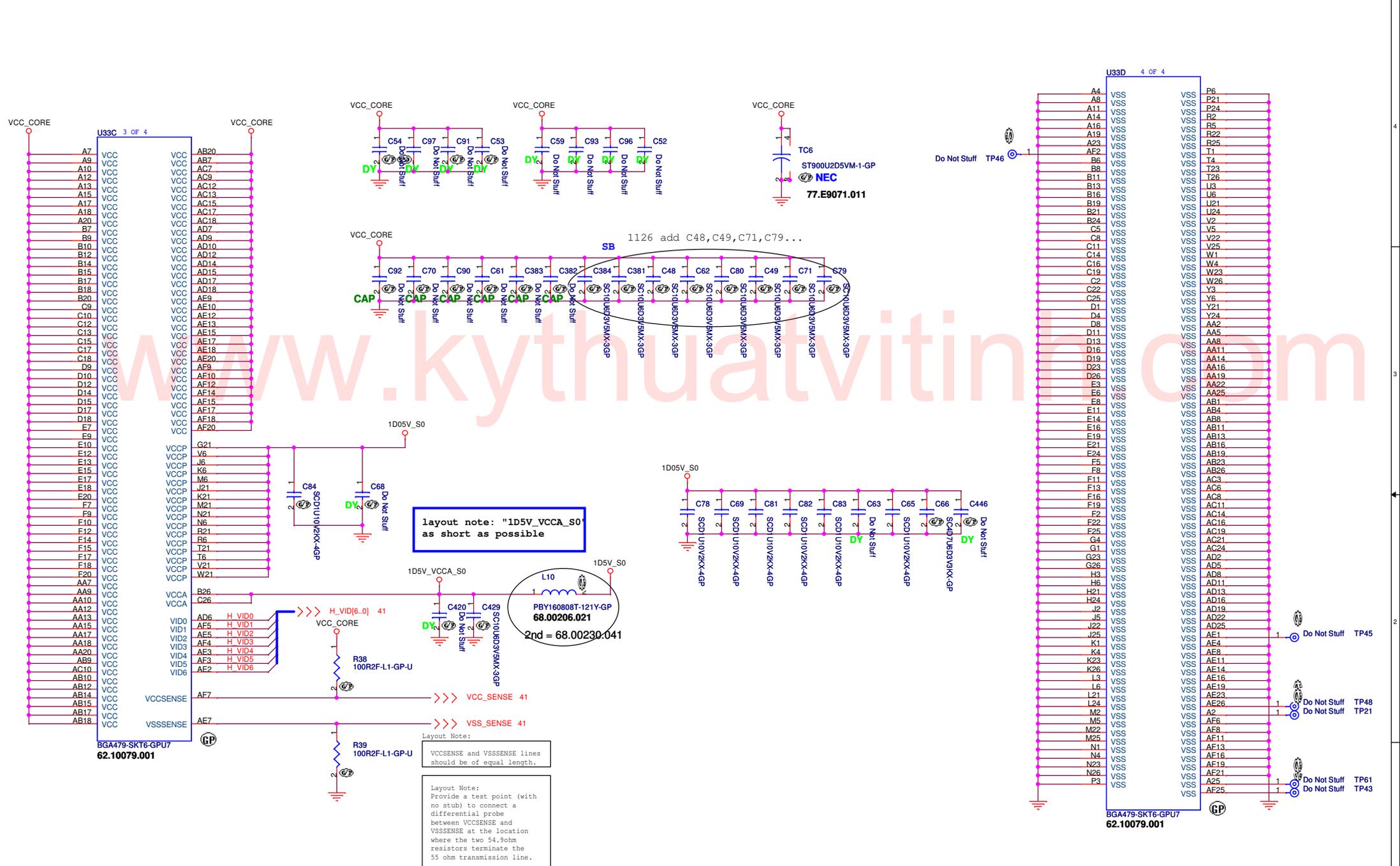
Net "TEST4" as short as possible,  
make sure "TEST4" routing is  
reference to GND and away other  
noisy signals

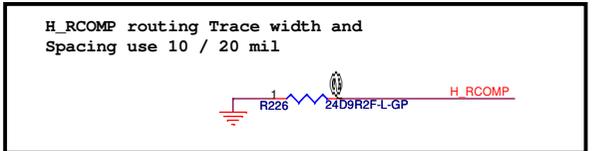
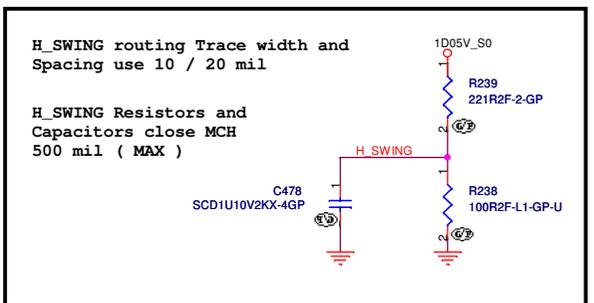
Layout Note:  
Comp0, 2 connect with 20-27.4 ohm, make  
trace length shorter than 0.5"  
Comp1, 3 connect with 20-55 ohm, make  
trace length shorter than 0.5"

UMA Two Phase 2

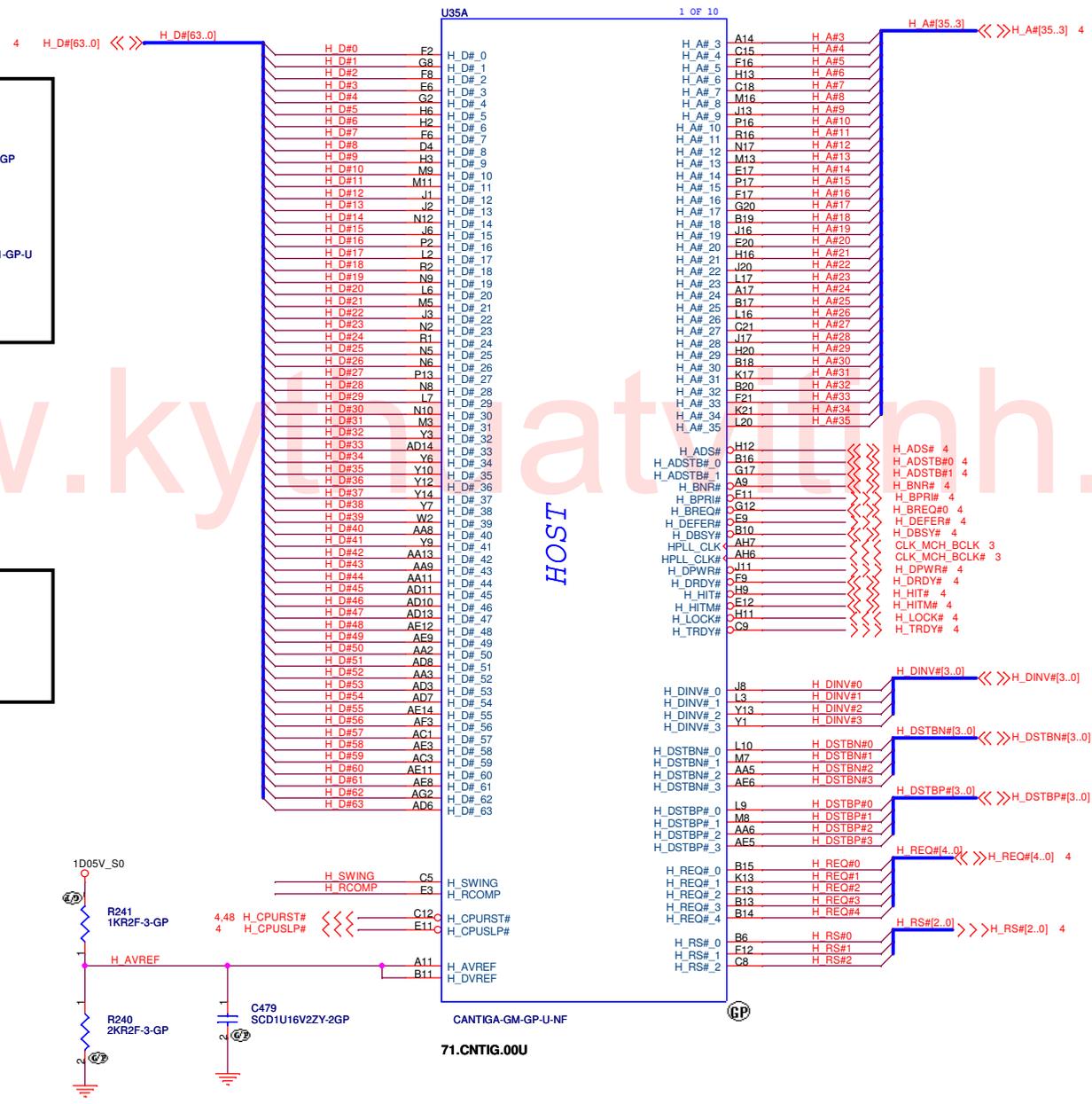
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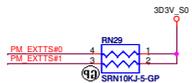
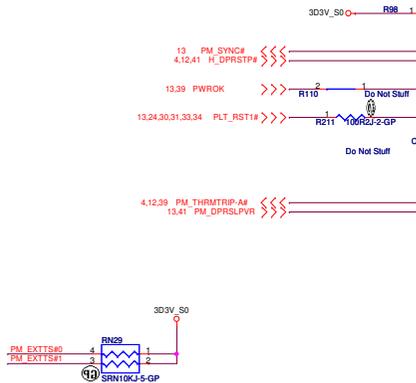
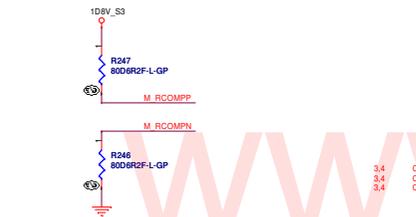
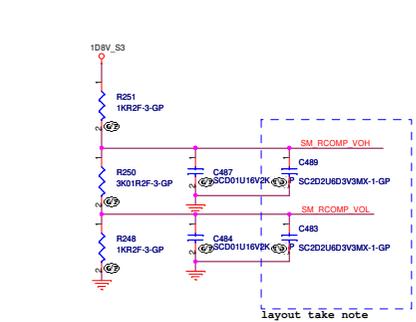
Title			<b>CPU (1 of 2)</b>
Size	Document Number	Rev	
	<b>HM40-MV</b>	<b>SB</b>	
Date:	Monday, December 01, 2008	Sheet	4 of 51





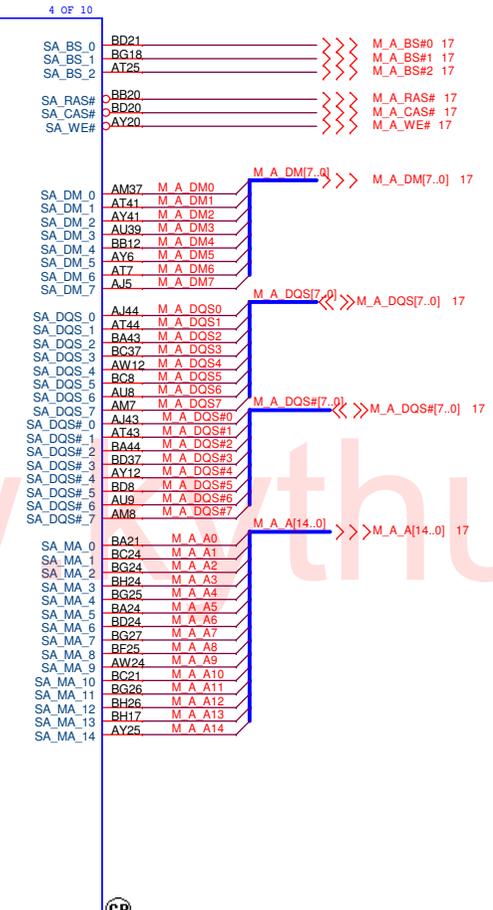
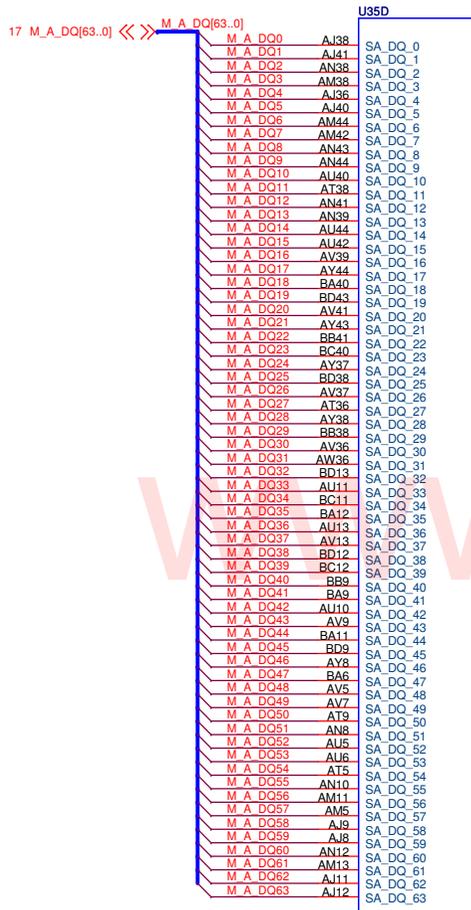
Place them near to the chip ( < 0.5" )



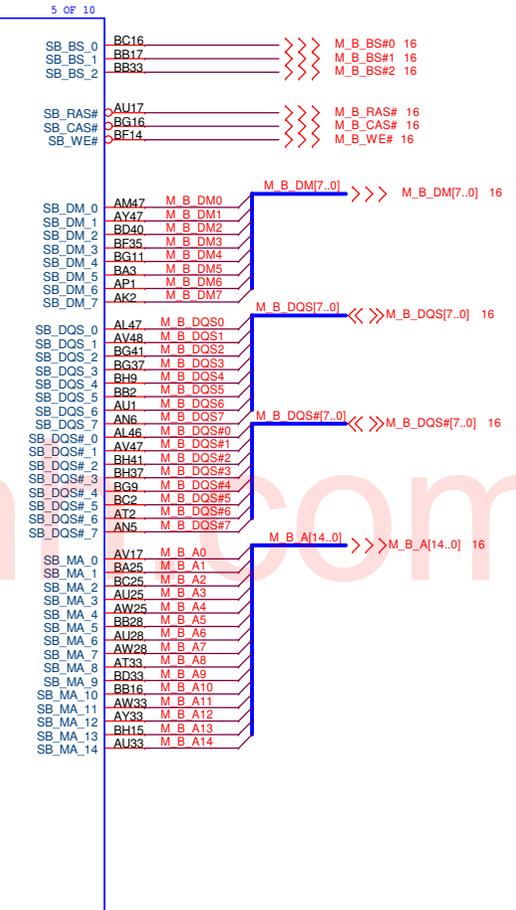
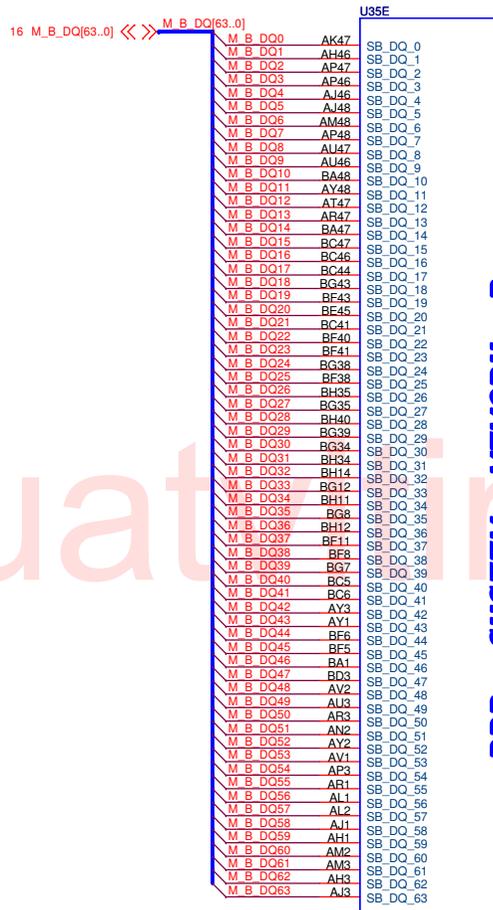


Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG strap

Pin Name	Strap Description	Configuration
M36	RESERVEDM36	
M37	RESERVEDM37	
M38	RESERVEDM38	
M39	RESERVEDM39	
M40	RESERVEDM40	
M41	RESERVEDM41	
M42	RESERVEDM42	
M43	RESERVEDM43	
M44	RESERVEDM44	
M45	RESERVEDM45	
M46	RESERVEDM46	
M47	RESERVEDM47	
M48	RESERVEDM48	
M49	RESERVEDM49	
M50	RESERVEDM50	
M51	RESERVEDM51	
M52	RESERVEDM52	
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M66	RESERVEDM66	
M67	RESERVEDM67	
M68	RESERVEDM68	
M69	RESERVEDM69	
M70	RESERVEDM70	
M71	RESERVEDM71	
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M330	RESERVEDM330	
M331	RESERVEDM331	
M332	RESERVEDM332	
M333	RESERVEDM333	
M334	RESERVEDM334	
M335	RESERVEDM335	
M336	RESERVEDM336	
M337	RESERVEDM337	
M338	RESERVEDM338	
M339	RESERVEDM339	
M340	RESERVEDM340	
M341	RESERVEDM341	
M342	RESERVEDM342	
M343	RESERVEDM343	
M344	RESERVEDM344	
M345	RESERVEDM345	
M346	RESERVEDM346	
M347	RESERVEDM347	
M348	RESERVEDM348	
M349	RESERVEDM349	
M350	RESERVEDM350	
M351	RESERVEDM351	
M352	RESERVEDM352	
M353	RESERVEDM353	
M354	RESERVEDM354	
M355	RESERVEDM355	
M356	RESERVEDM356	
M357	RESERVEDM357	
M358	RESERVEDM358	
M359	RESERVEDM359	
M360	RESERVEDM360	
M361	RESERVEDM361	
M362	RESERVEDM362	
M363	RESERVEDM363	
M364	RESERVEDM364	
M365	RESERVEDM365	
M366	RESERVEDM366	
M367	RESERVEDM367	
M368	RESERVEDM368	
M369	RESERVEDM369	
M370	RESERVEDM370	
M371	RESERVEDM371	
M372	RESERVEDM372	
M373	RESERVEDM373	
M374	RESERVEDM374	
M375	RESERVEDM375	
M376	RESERVEDM376	
M377	RESERVEDM377	
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M382	RESERVEDM382	
M383	RESERVEDM383	
M384	RESERVEDM384	
M385	RESERVEDM385	
M386	RESERVEDM386	
M387	RESERVEDM387	
M388	RESERVEDM388	
M389	RESERVEDM389	
M390	RESERVEDM390	
M391	RESERVEDM391	
M392	RESERVEDM392	
M393	RESERVEDM393	
M394	RESERVEDM394	
M395		

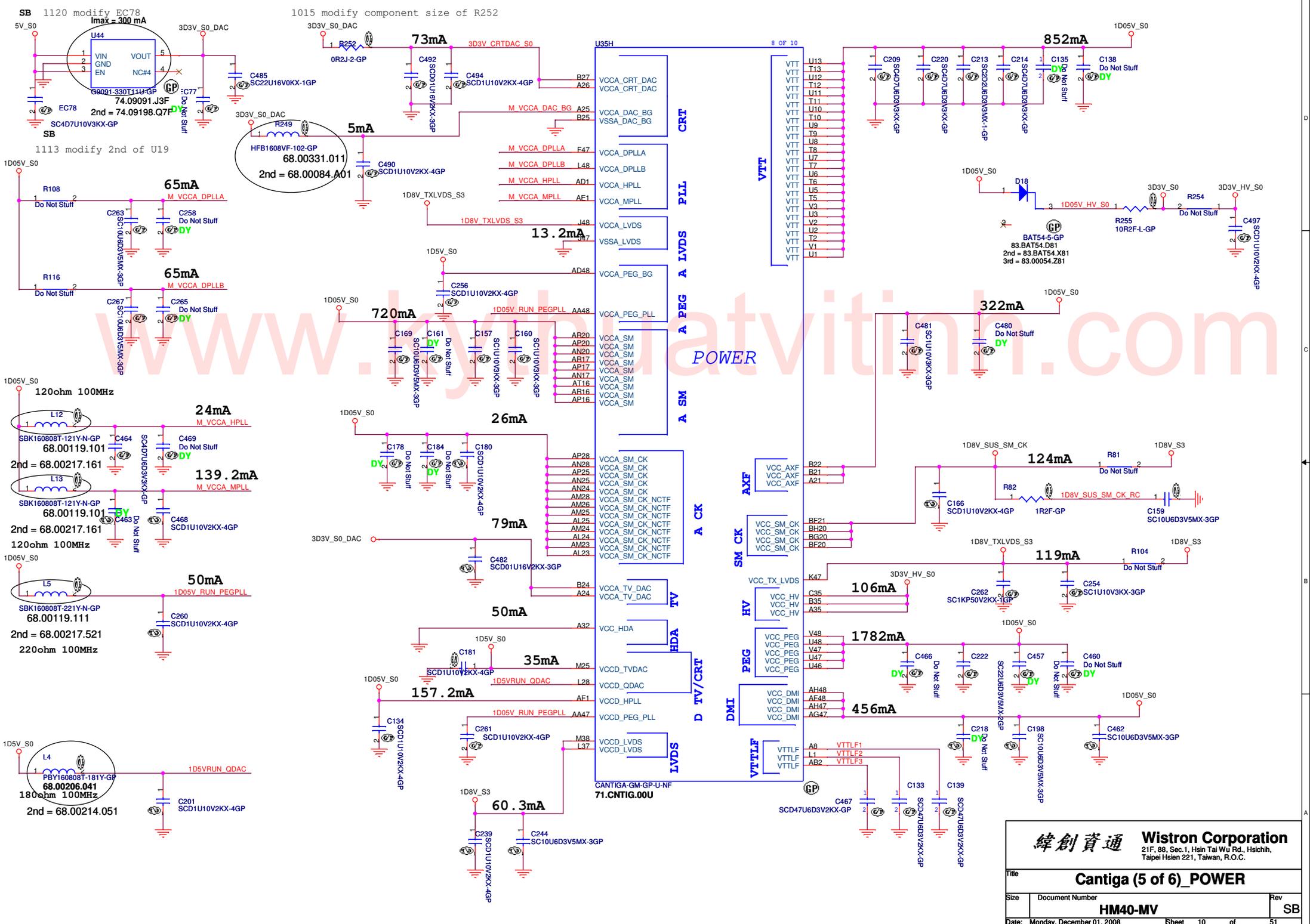


CANTIGA-GM-GP-U-NF  
71.CNTIG.00U



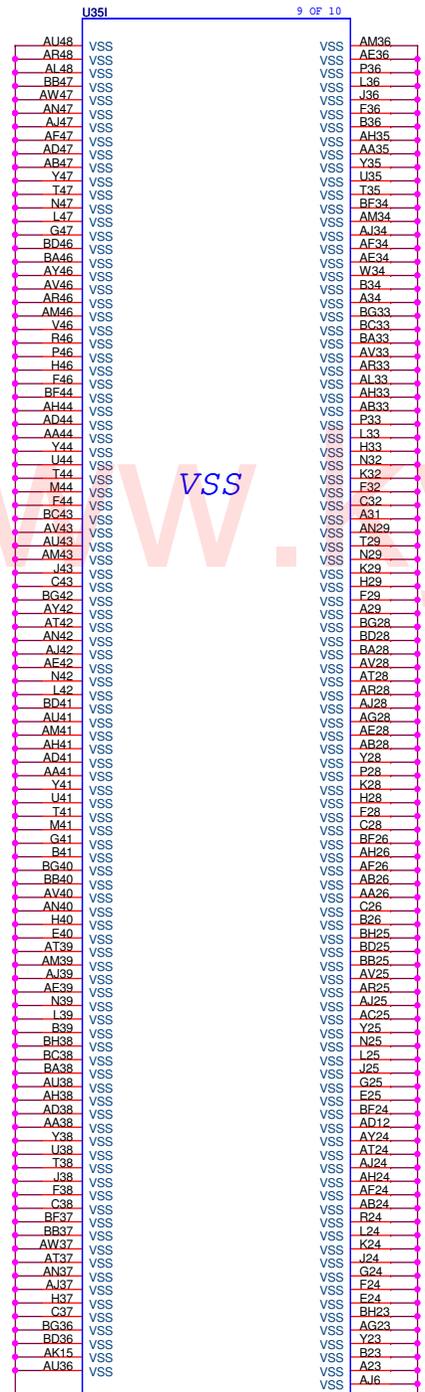
CANTIGA-GM-GP-U-NF  
71.CNTIG.00U



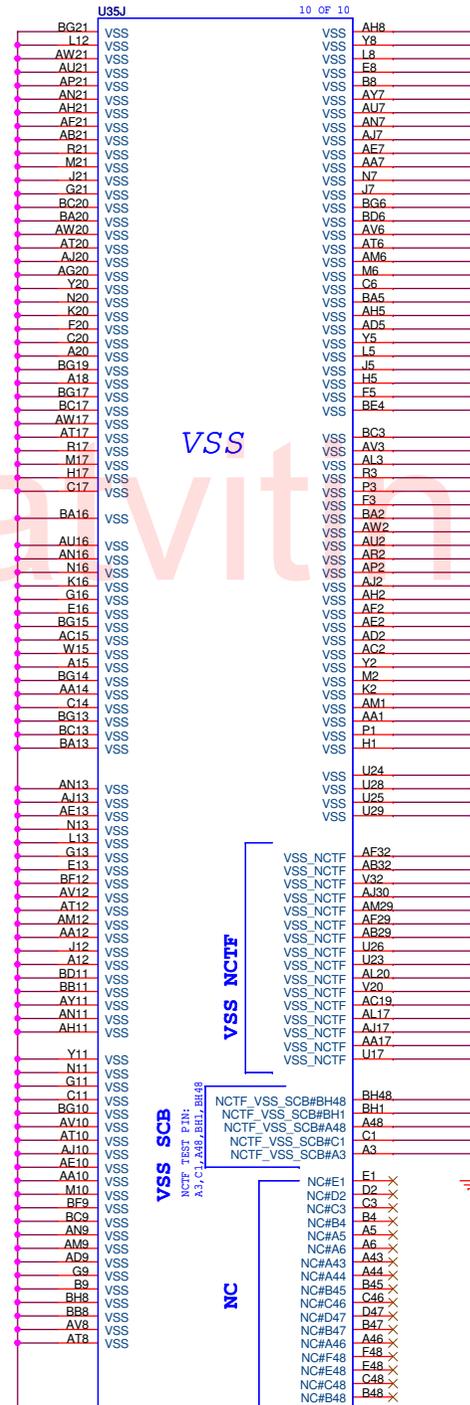


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<b>Title</b>		
<b>Cantiga (5 of 6)_POWER</b>		
Size	Document Number	Rev
	<b>HM40-MV</b>	<b>SB</b>
Date: Monday, December 01, 2008		
Sheet	10	of 51



CANTIGA-GM-GP-U-NF  
71.CNTIG.00U

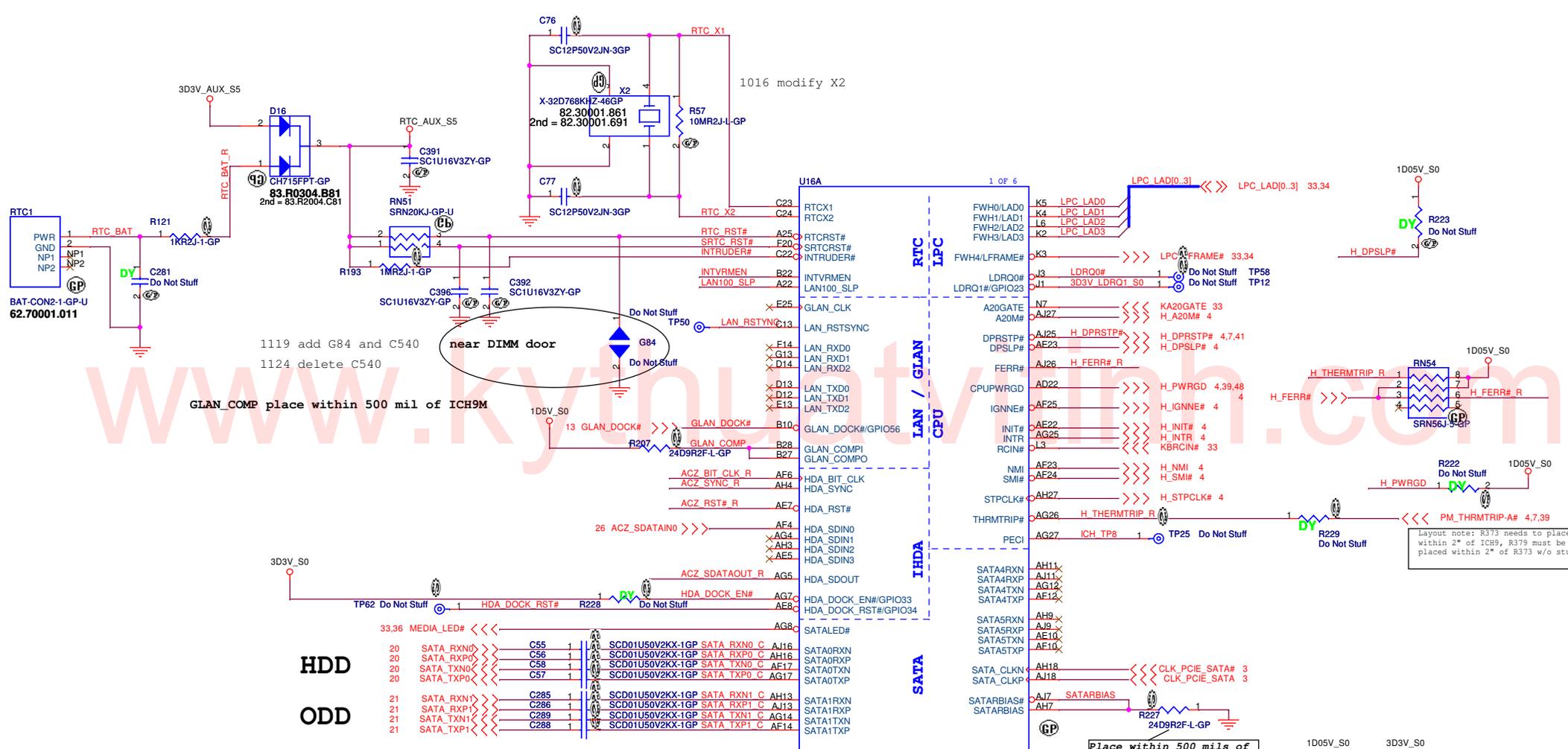


CANTIGA-GM-GP-U-NF  
71.CNTIG.00U

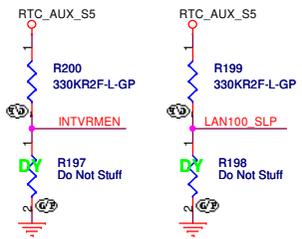


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Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>Cantiga (6 of 6)</b>	
Size	Document Number	Rev	SB
Date: Monday, December 01, 2008		Sheet	11 of 51

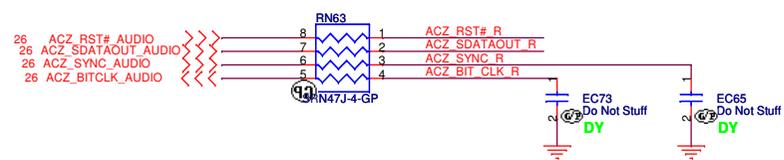


1119 add G84 and C540  
 1124 delete C540  
 GLAN\_COMP place within 500 mil of ICH9M



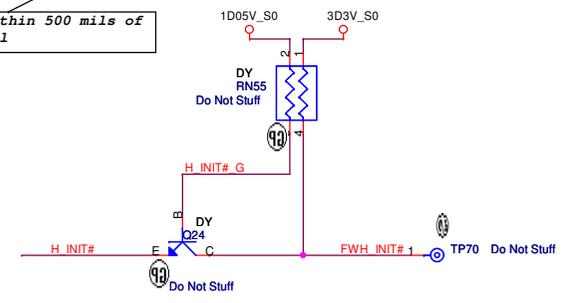
integrated VccSus1_05, VccSus1_5, VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

SB  
 1117 delete MDC function (R231, R237, R232, R234)  
 SB  
 1126 delete R230, R233, R235, R236 and RN63



0915 add EC73 for EMI demand

Place within 500 mils of ICH9 ball



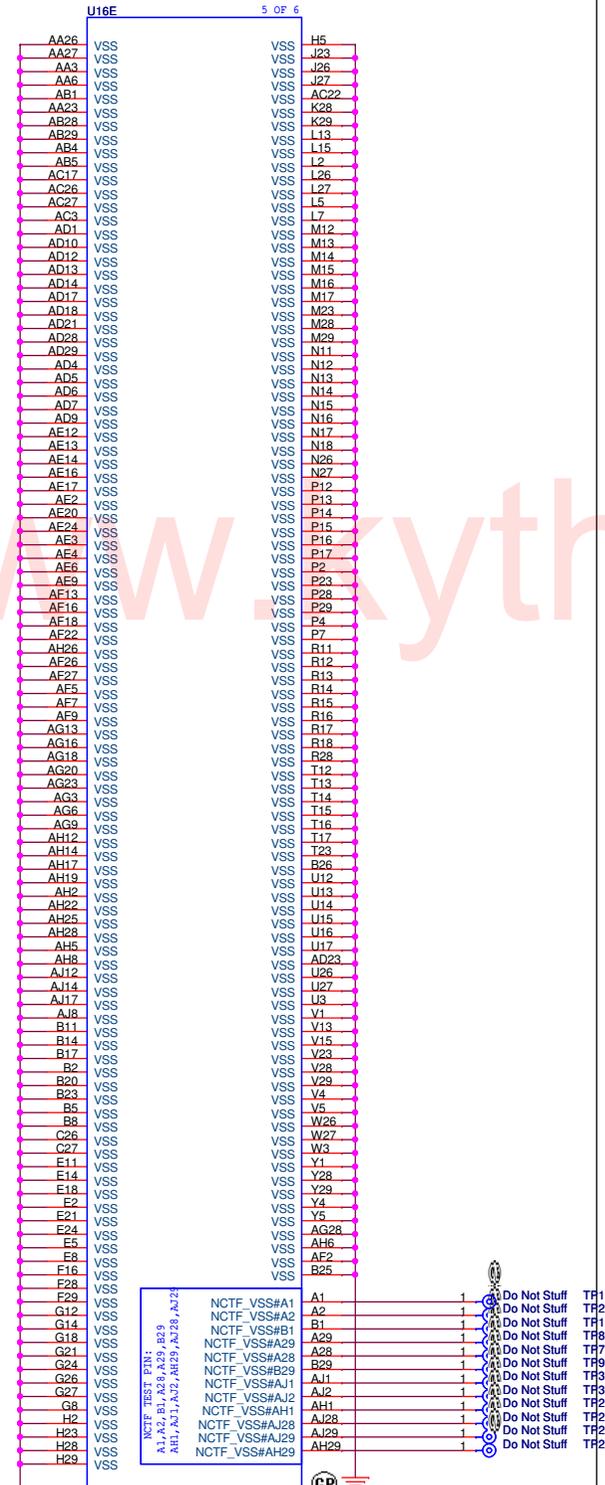
UMA Two Phase 2

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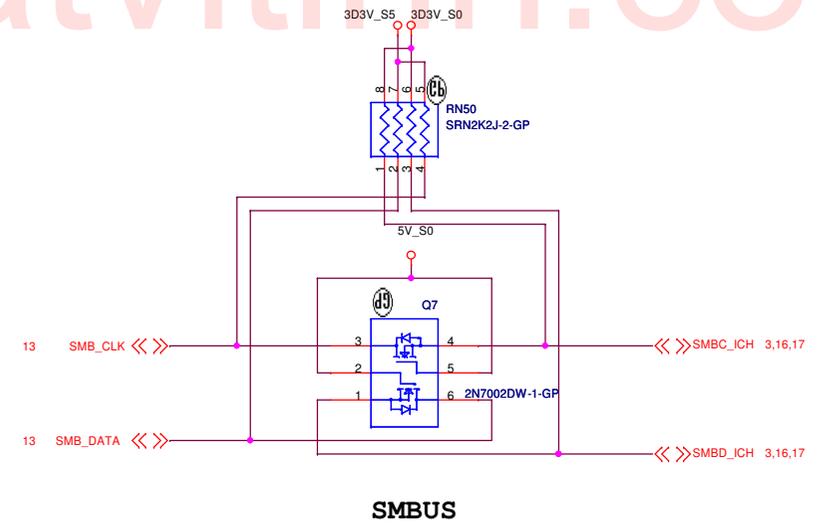
File: **ICH9-M (1 of 4) SATA/HDA/RTC**  
 Size: Document Number: **HM40-MV** Rev: **SB**  
 Date: Wednesday, November 26, 2008 Sheet 12 of 51







ICH9M-GP-NF  
71.ICH9M.00U



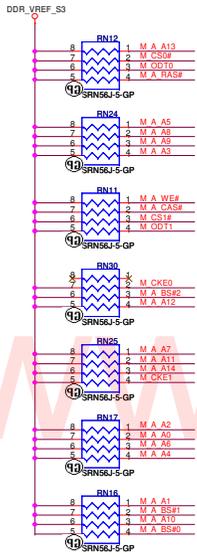
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: <b>ICH9-M (4 of 4)</b>			
Size	Document Number	Rev	
	<b>HM40-MV</b>	<b>SB</b>	
Date: Monday, December 01, 2008	Sheet 15	of 51	



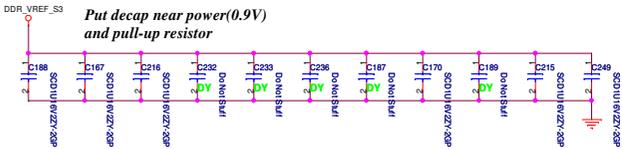
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

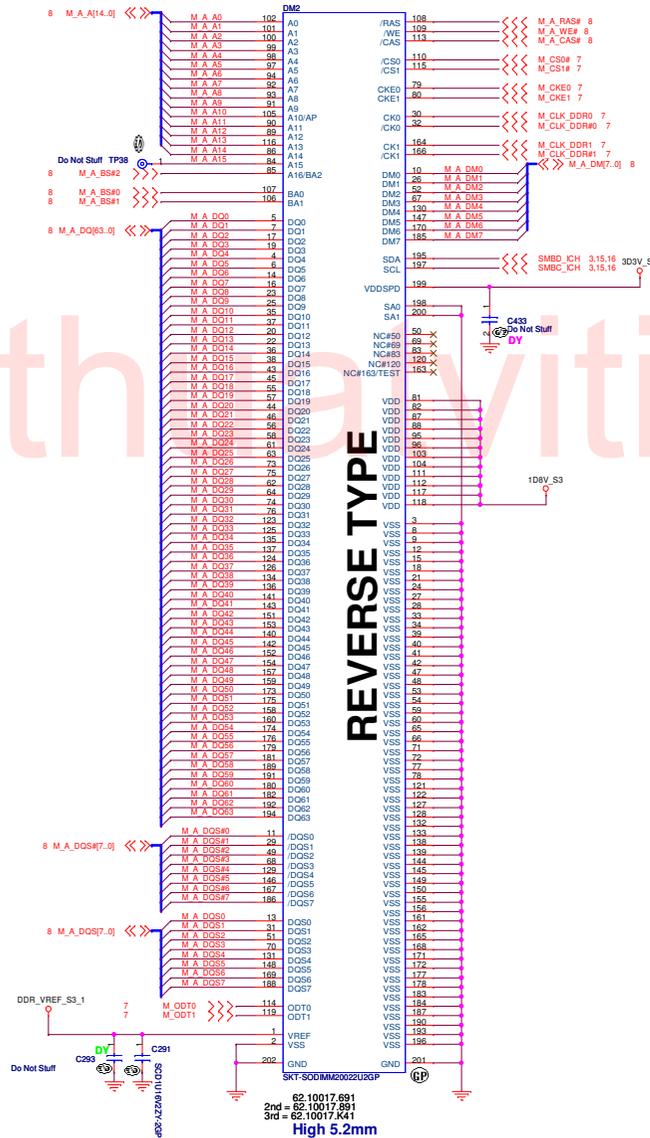
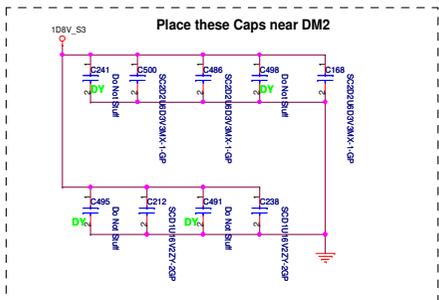


# Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM2

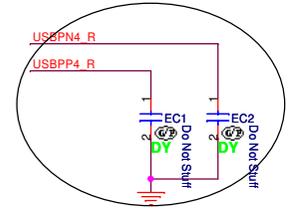
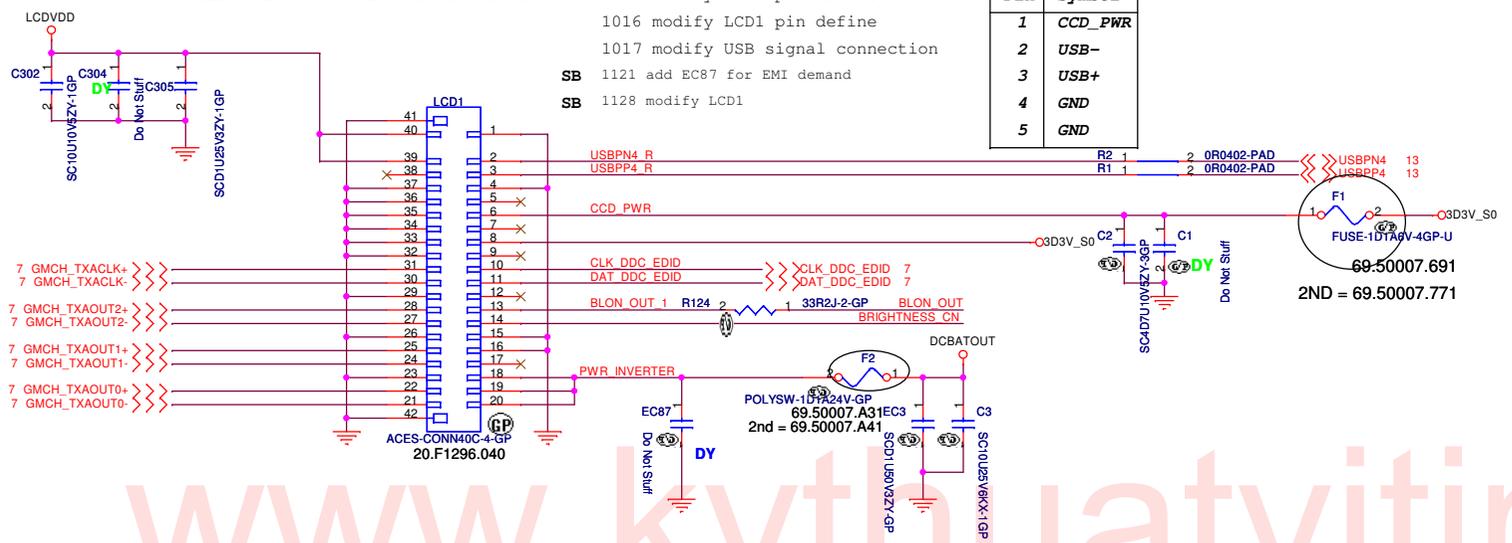


REVERSE TYPE

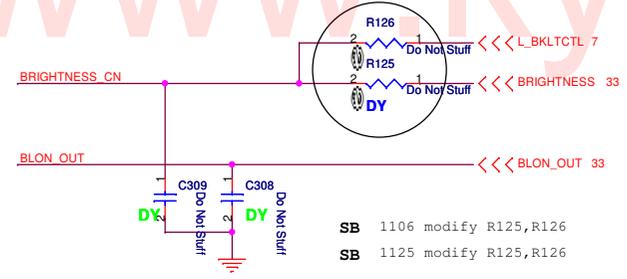
# LCD/CCD CONN

- 1015 modify LCD1 pin define
- 1016 modify LCD1 pin define
- 1017 modify USB signal connection
- SB 1121 add EC87 for EMI demand
- SB 1128 modify LCD1

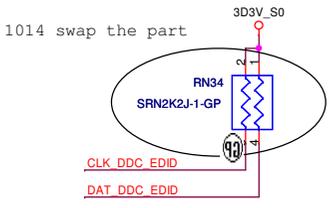
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



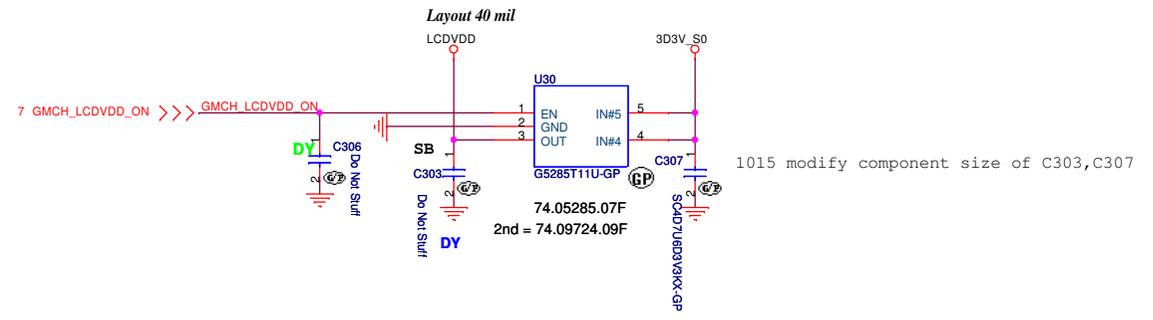
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- SB 1106 modify R125,R126
- SB 1125 modify R125,R126



1014 swap the part

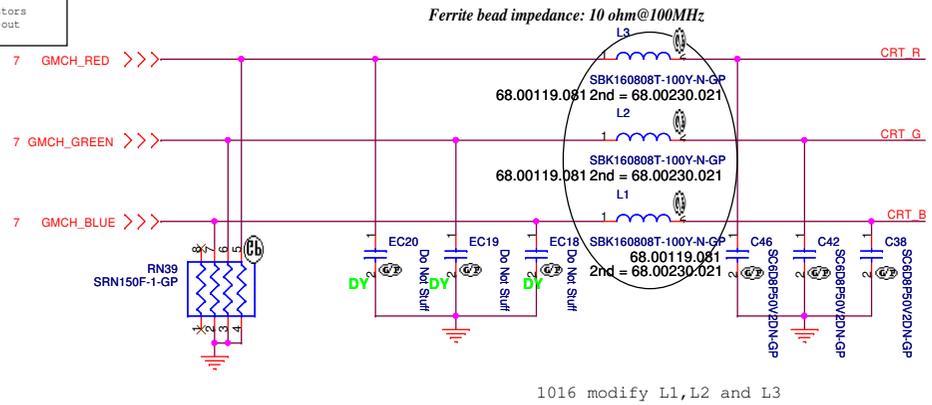


1015 modify component size of C303,C307

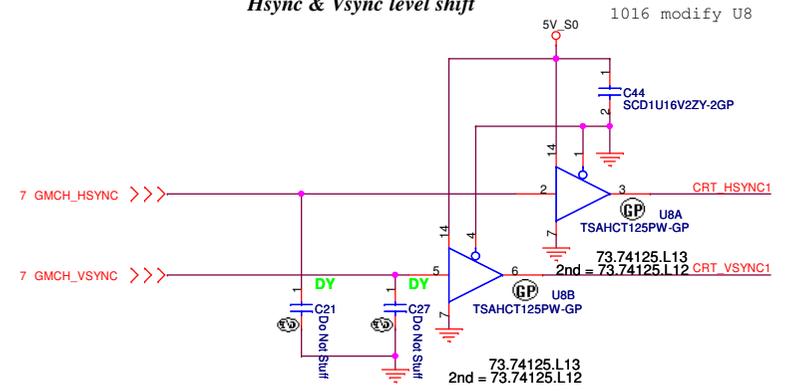
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<b>LCD CONN</b>	
File	Rev
Size	Document Number
<b>HM40-MV</b>	
Date: Friday, November 28, 2008	Sheet 18 of 51

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

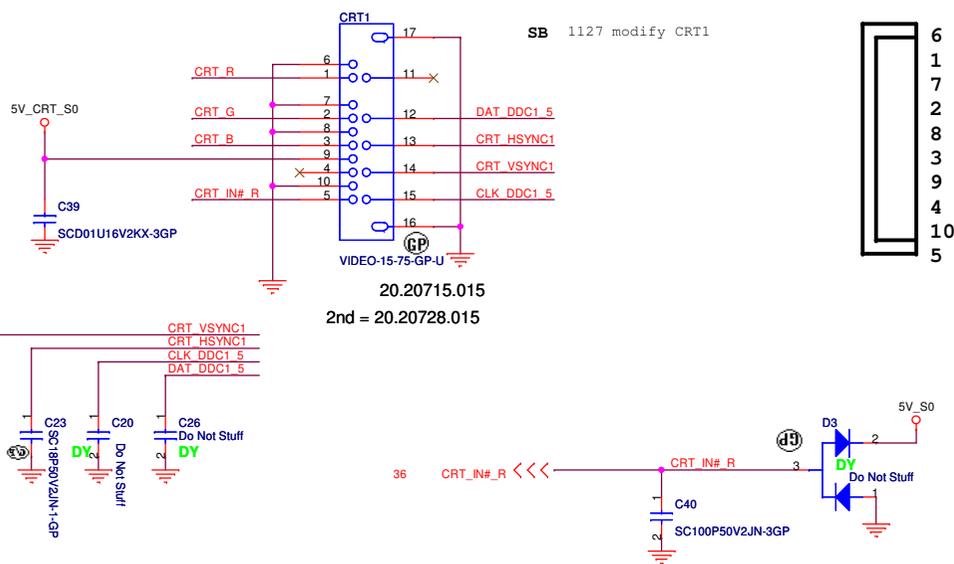


### Hsync & Vsync level shift

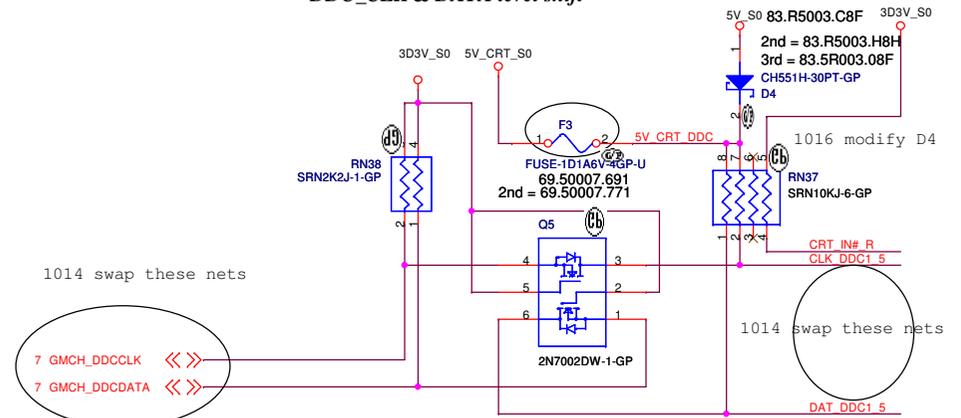


Layout Note:  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

### CRT I/F & CONNECTOR



### DDC\_CLK & DATA level shift



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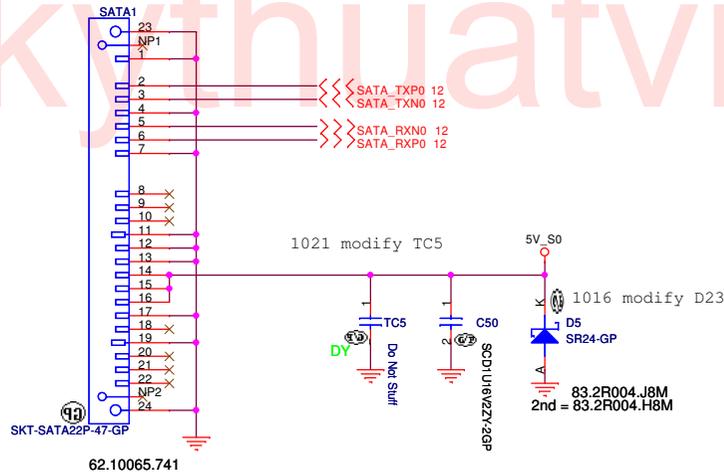
Title: **CRT Connector**

Size: Document Number: **HM40-MV** Rev: **SB**

Date: Monday, December 01, 2008 Sheet 19 of 51

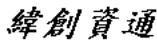
# SATA Connector

0912 add these parts for EMI demand  
 1001 delete these parts for EMI demand  
 1021 modify SATA1

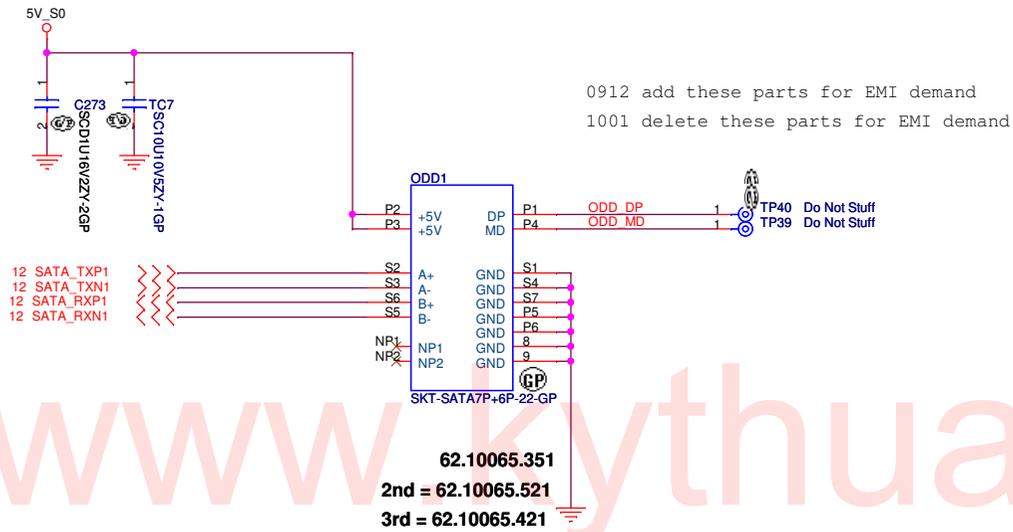


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Title	
<b>HDD</b>	
Size	Document Number
	<b>HM40-MV</b>
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	Rev <b>SB</b>

# SATA ODD Connector



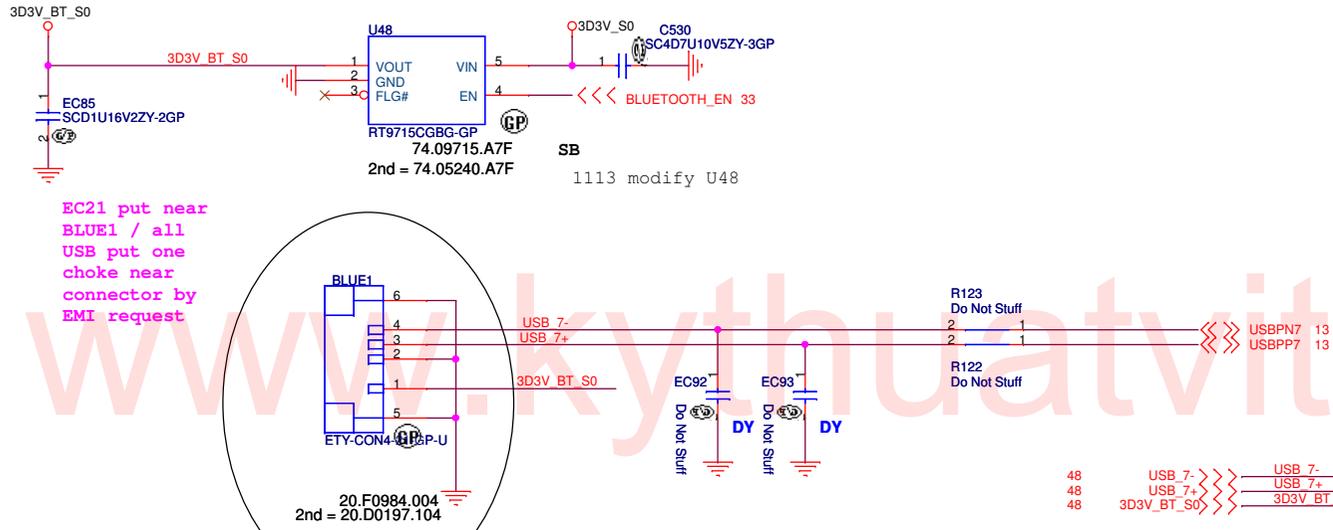
UMA Two Phase 2

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Taipei Hsien 221, Taiwan, R.O.C.

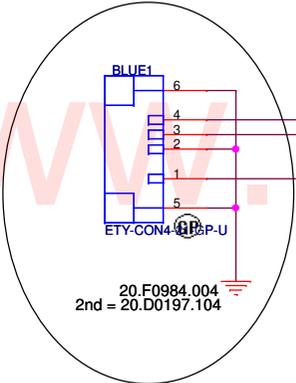
Title		<b>ODD</b>	
Size	Document Number	Rev	SB
	<b>HM40-MV</b>		
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# BLUETOOTH MODULE

1.5A / High Active Voltage 2V



EC21 put near  
BLUE1 / all  
USB put one  
choke near  
connector by  
EMI request

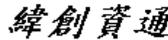


SB 1125 add EC92 and EC93

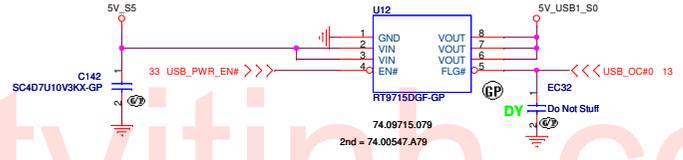
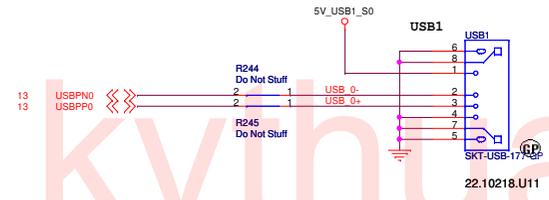
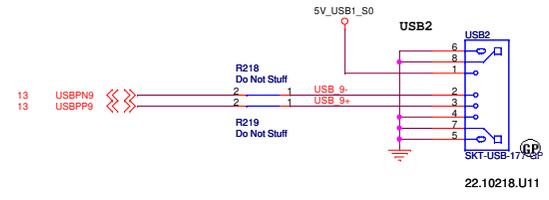
0930 modify BLUE1  
1017 modify BLUE1

1017 modify USB signal connection

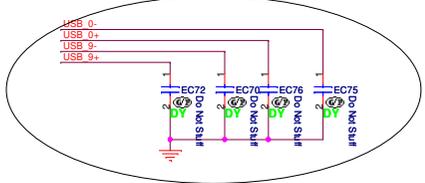
UMA Two Phase 2

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<b>Bluetooth</b>	
Size	Document Number
	<b>HM40-MV</b>
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Rev <b>SB</b>	

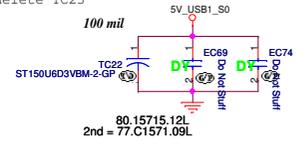
1017 modify USB signal connection  
 1021 modify and swap these parts(USB1 and USB2)



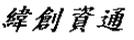
0912 add these parts for EMI demand



1021 delete TC23

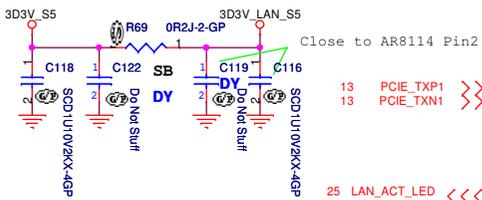


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File	
<b>USB</b>	
Size	Document Number
	<b>HM40-MV</b>
Date: Monday, December 01, 2008	Rev <b>SB</b>
Sheet	51

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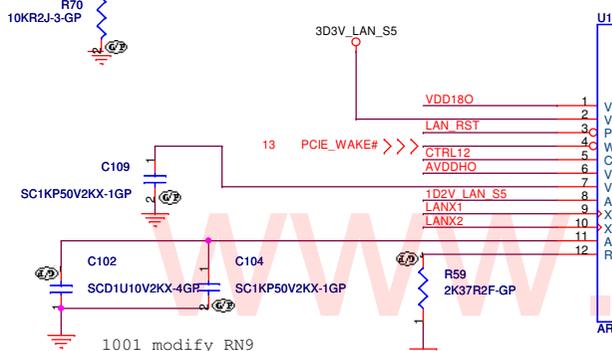
1015 modify component size of R69



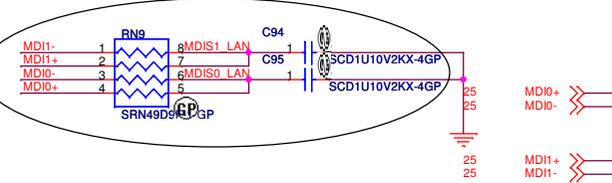
Close to AR8114 Pin2

13 PCIE\_TXP1  
13 PCIE\_TXN1  
25 LAN\_ACT\_LED  
25 10M/100M\_LED#

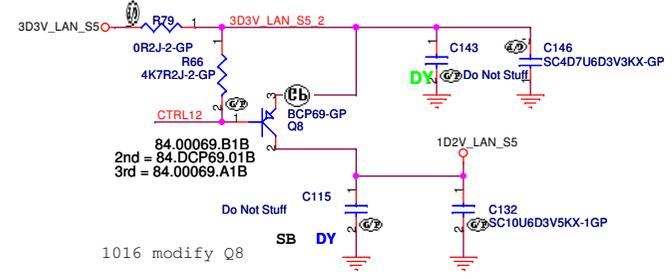
LAN ACT LED FOR AR8114A LAN\_ACT\_LED is high enable pin



1001 modify RN9  
1014 swap these nets



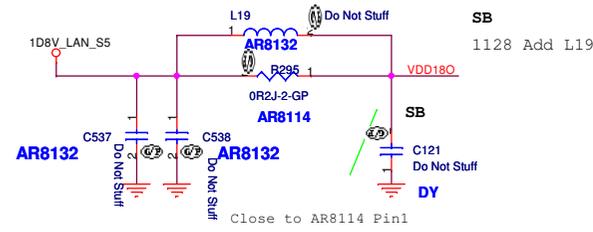
1015 modify component size of R79



1016 modify Q8

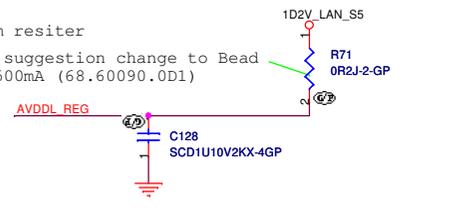
Atheros suggestion change to Bead  
60 ohms/100Mhz 500mA (68.60090.0D1)

AR8114 use 0ohm resistor  
AR8132 Atheros suggest to change 4.7uH choke

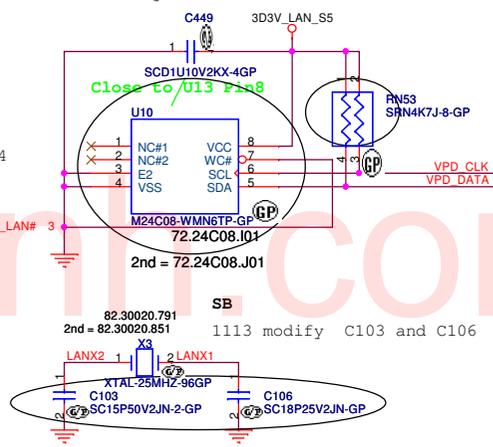


Close to AR8114 Pin6

AR8132 use 0 ohm resister  
AR8114A Atheros suggestion change to Bead  
60 ohms/100Mhz 500mA (68.60090.0D1)



1016 modify RN53 and U10



Close to AR8114 Pin28  
Close to AR8114 Pin32  
Close to AR8114 Pin45  
Close to AR8114 Pin46

Close to AR8114 Pin8  
Close to AR8114 Pin16  
Close to AR8114 Pin22  
Close to AR8114 Pin36  
Close to AR8114 Pin39

Close to AR8114 Pin6  
Close to AR8114 Pin15  
Close to AR8114 Pin19  
Close to AR8114 Pin25

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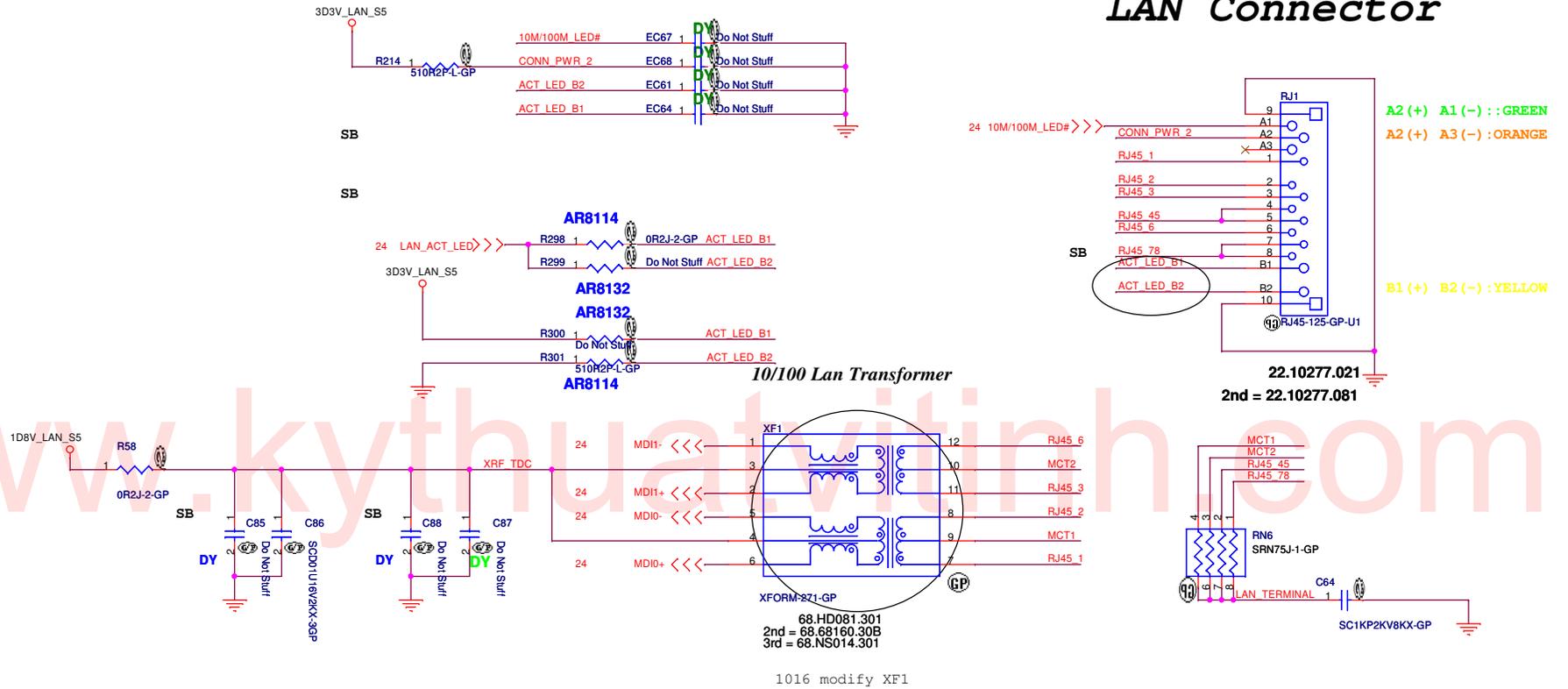
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Title: **Atheros AR8114/8132**

Size A3	Document Number	Rev
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# LAN Connector



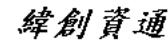
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

**RJ11 signal must leave the other signal or power plane 100mil.**

DOC\_TIP, DOC\_RING, TIP, RING:  
 W/S : 10/100 @ Surface layers  
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

UMA Two Phase 2

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<b>LAN Connector</b>	
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Rev <b>SB</b>	

SB 1118 delete C245 and C270

0911 add net name(DVDD\_1\_8)

0911 add net name(ACZ\_SDATAIN0\_R)

12 ACZ\_RST#\_AUDIO >>>  
 12 ACZ\_BITCLK\_AUDIO >>>  
 12 ACZ\_SYNC\_AUDIO >>>  
 12 ACZ\_SDATAIN0 >>>  
 12 ACZ\_SDATAOUT\_AUDIO >>>

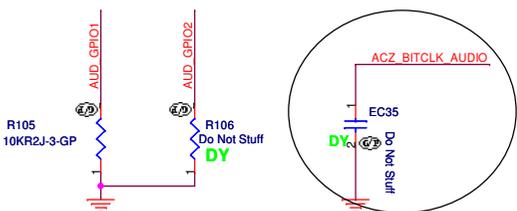
SB 1126 add C541 and modify R101

27 EAPD# <<<<

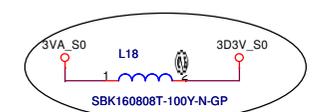
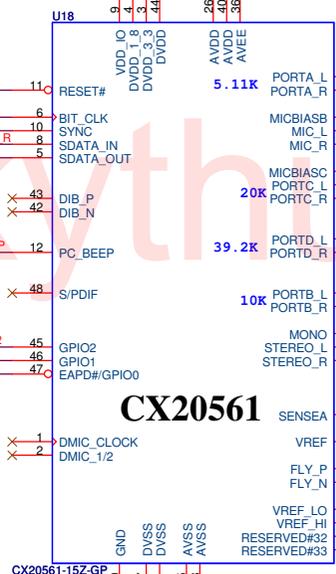
0912 add the part for EMI demand

## PC BEEP GAIN CONTROL

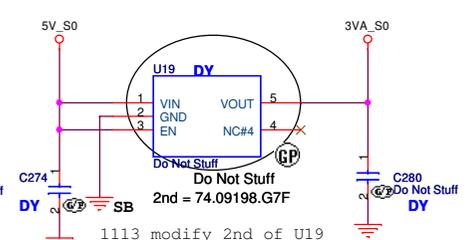
Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.



GAIN	10K GPIO RESISTORS	
	R615	R614
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate



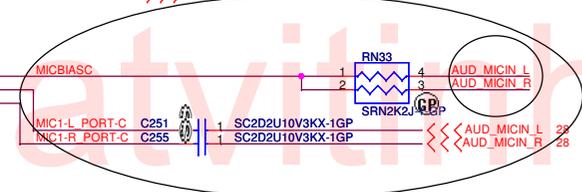
68.00119.081  
 2nd = 68.00230.021  
 1001 Add R107  
 SB 1113 modify 2nd of U19  
 SB 1118 delete R107 and add L18



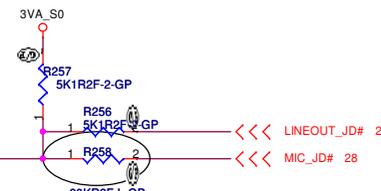
1113 modify 2nd of U19

1014 swap these nets

1014 modify these nets

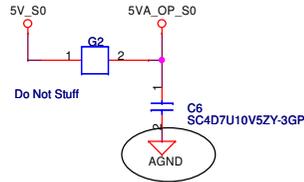


0911 add net name(FLY\_P, FLY\_N, VREF\_LO, VREF\_HI)

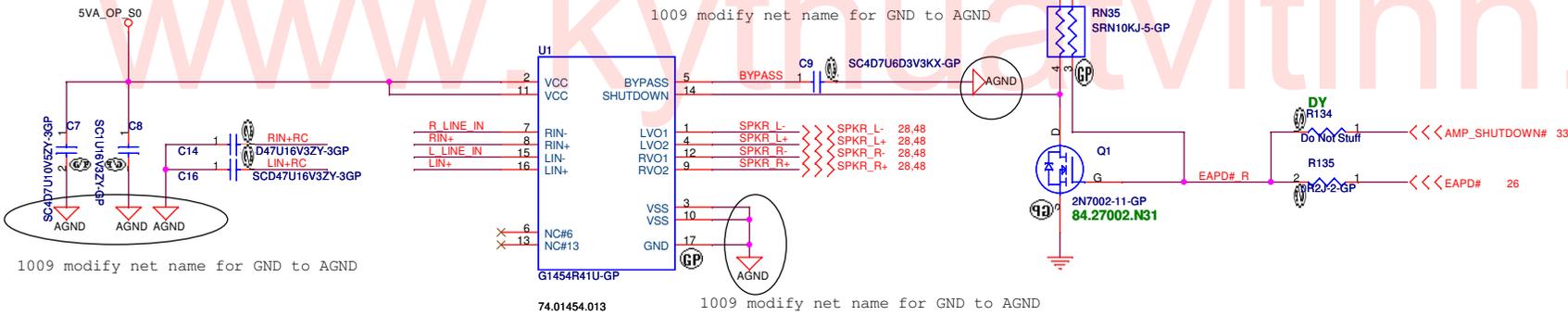


1014 modify R258 from 10k to 20k ohm

# AUDIO OP AMPLIFIER



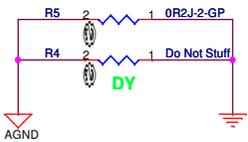
1009 modify net name for GND to AGND



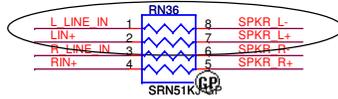
1009 modify net name for GND to AGND

1009 modify net name for GND to AGND

## AC decoupling



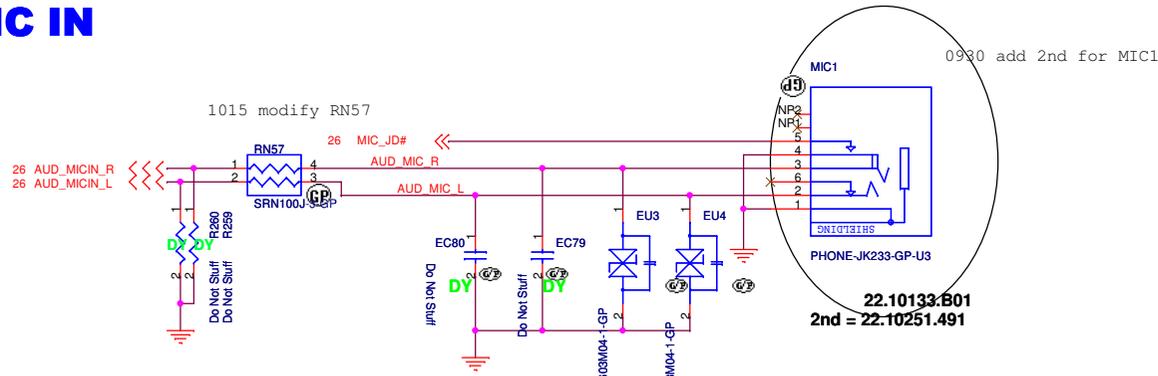
1014 swap these nets



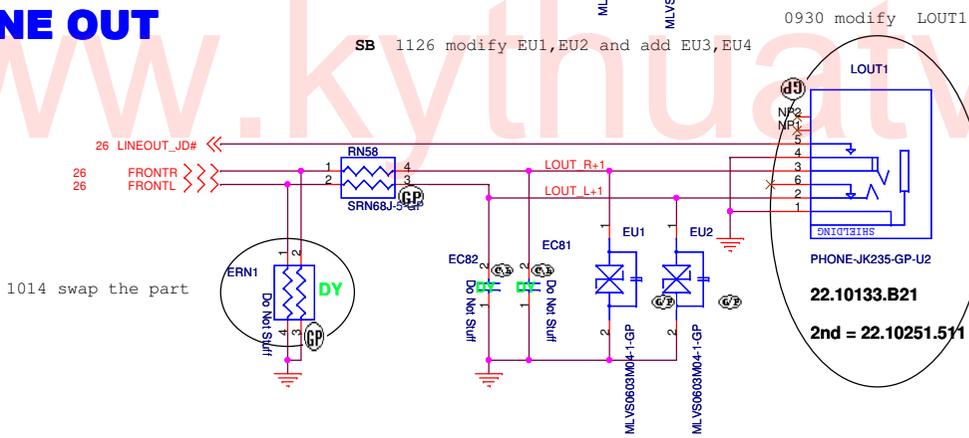
UMA Two Phase 2

		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>AUDIO AMP</b>		
Size	Document Number	Rev
	<b>HM40-MV</b>	<b>SB</b>
Date: Monday, December 01, 2008		Sheet 27 of 51

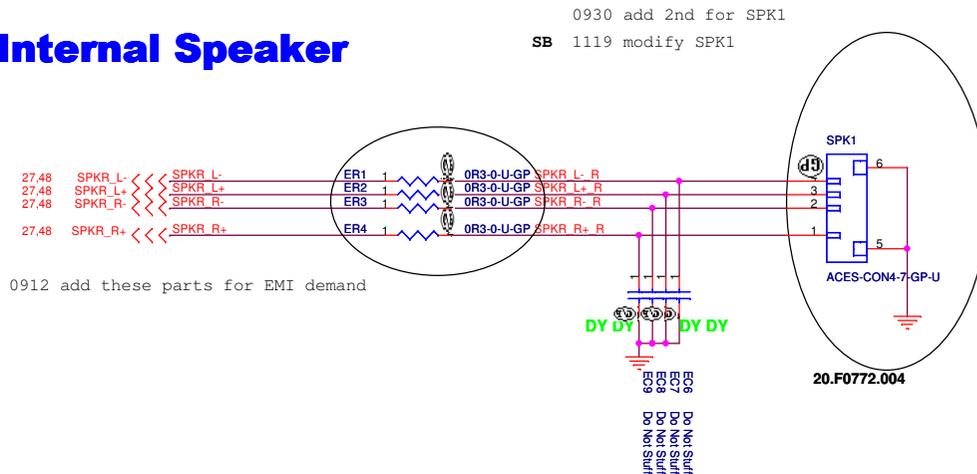
# MIC IN



# LINE OUT



# Internal Speaker



UMA Two Phase 2

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO JACK**

Size: Document Number: **HM40-MV** Rev: **SB**

Date: Monday, December 01, 2008 Sheet 28 of 51

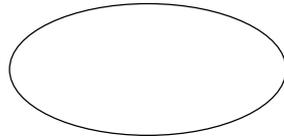
# MDC 1.5 CONN

0912 add the part for EMI demand

1002 modify MDC1

**SB**

1112 delete MDC function

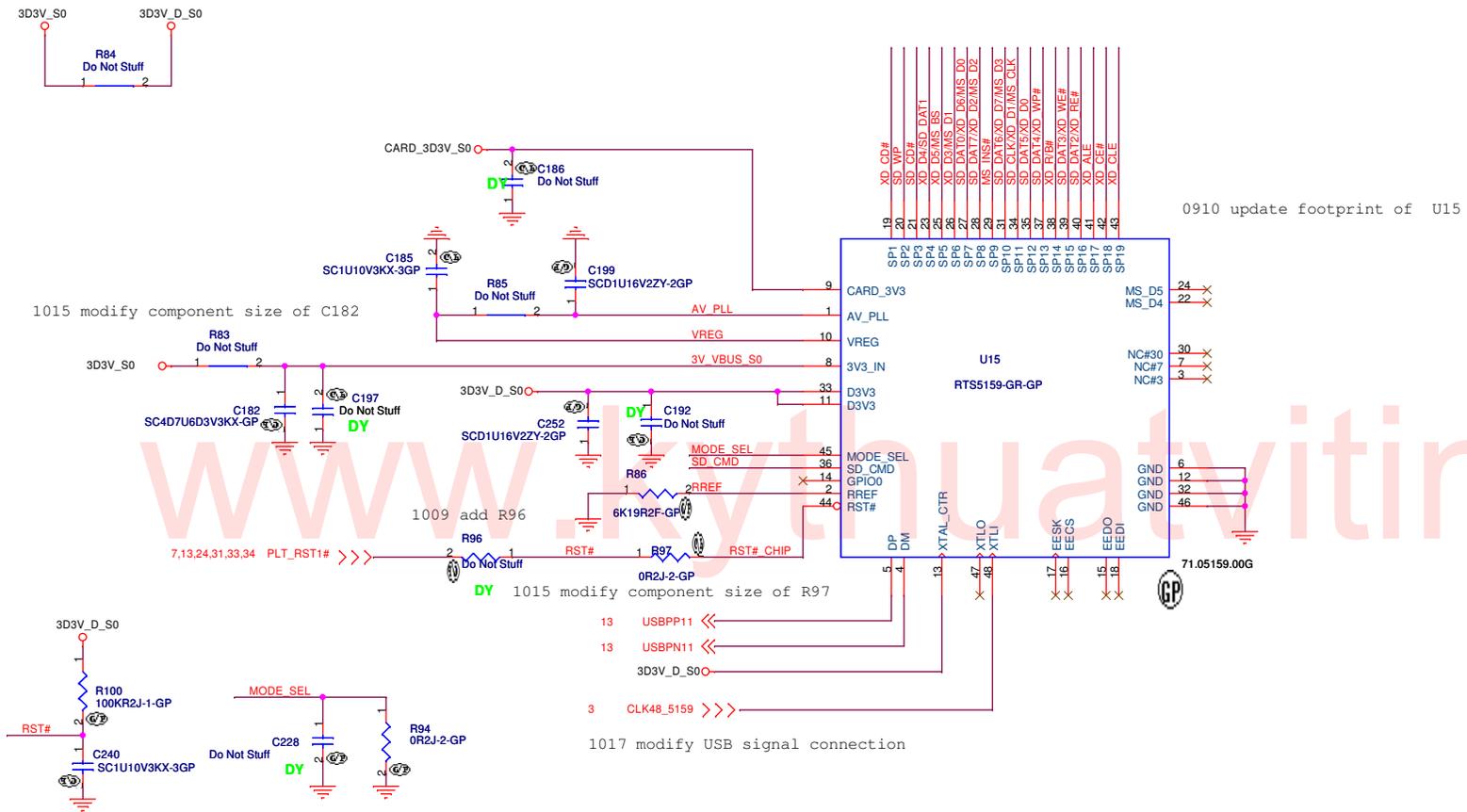


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UMA Two Phase 2

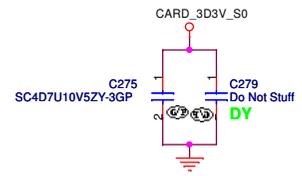
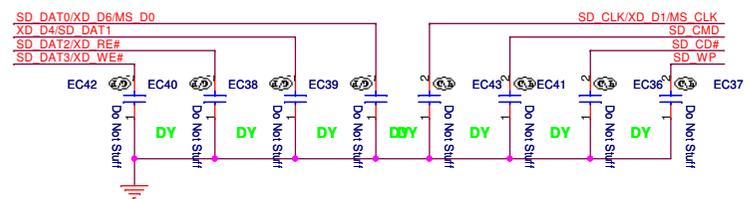
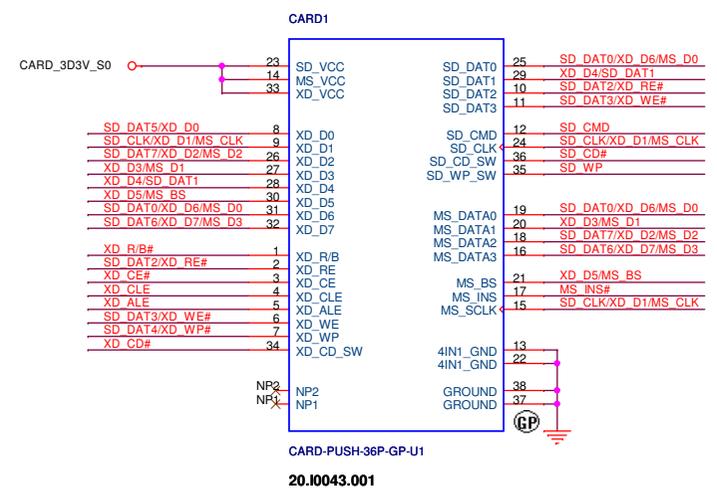
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>MDC</b>		
Size	Document Number	HM40-MV		Rev	SB
Date:	Monday, November 24, 2008	Sheet	29	of	51



### 5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)

1009 modify this net  
1013 modify card1



UMA Two Phase 2

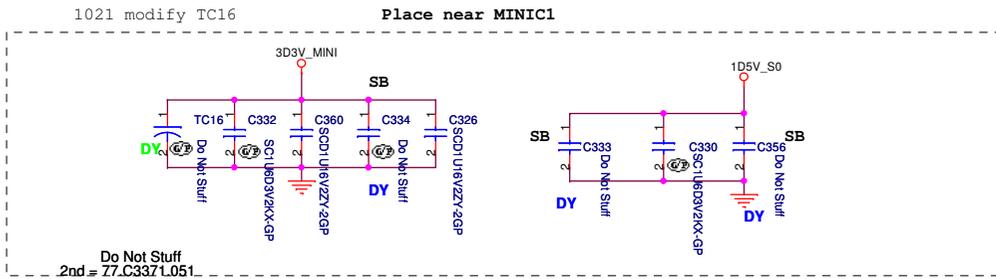
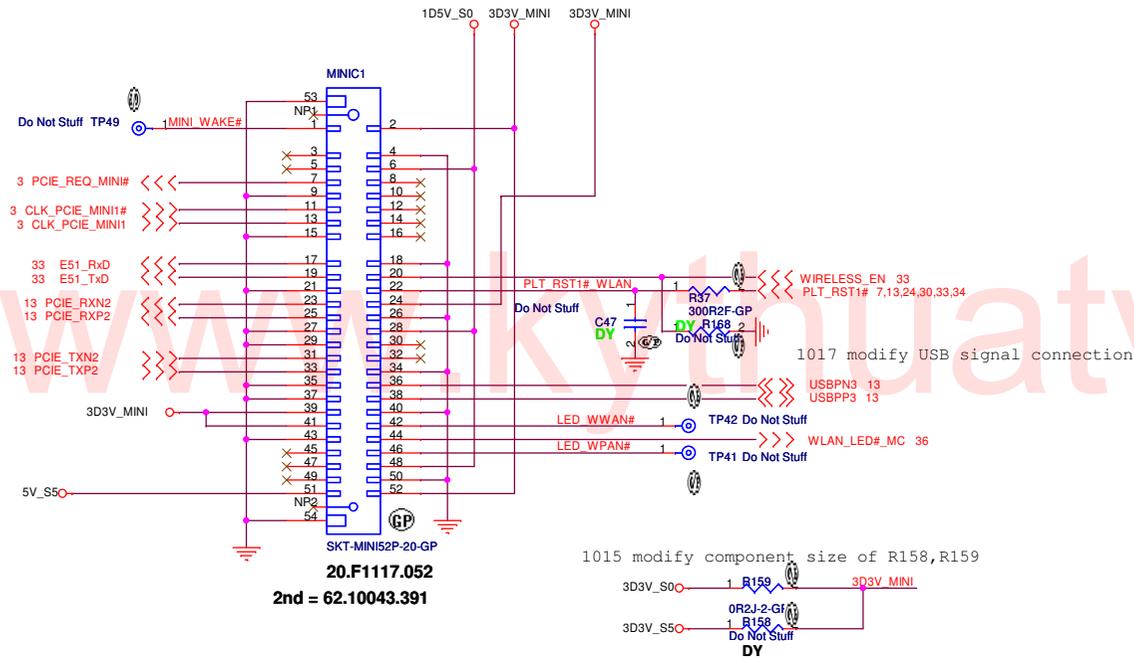
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

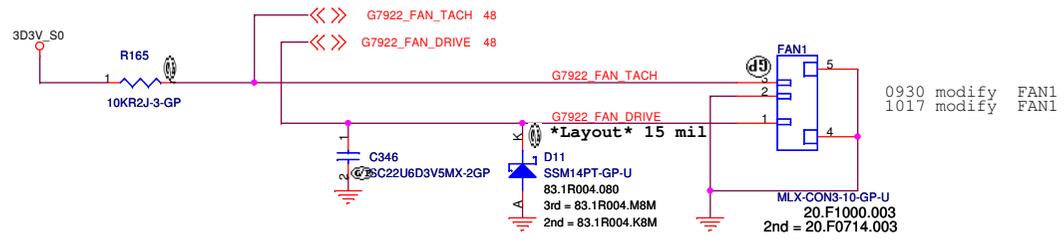
Title: **CARD READER- RTS5159**

Size	Document Number	Rev
	<b>HM40-MV</b>	<b>SB</b>

Date: Monday, December 01, 2008 Sheet 30 of 51

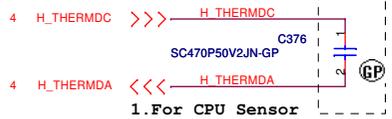
# Mini Card Connector(WLAN)





0930 modify FAN1  
1017 modify FAN1

Layout notice :  
Both H\_THERMDA and THERMDC routing  
10 mil trace width and 10 mil spacing

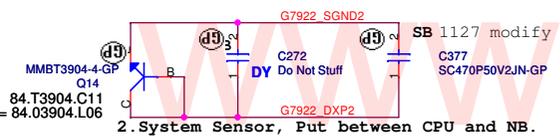


1. For CPU Sensor

C374 must be near Q7

C373 must be near EMC2102

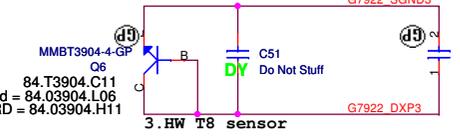
Layout notice : Both SGND2 and DXP2 routing  
10 mil trace width and 10 mil spacing



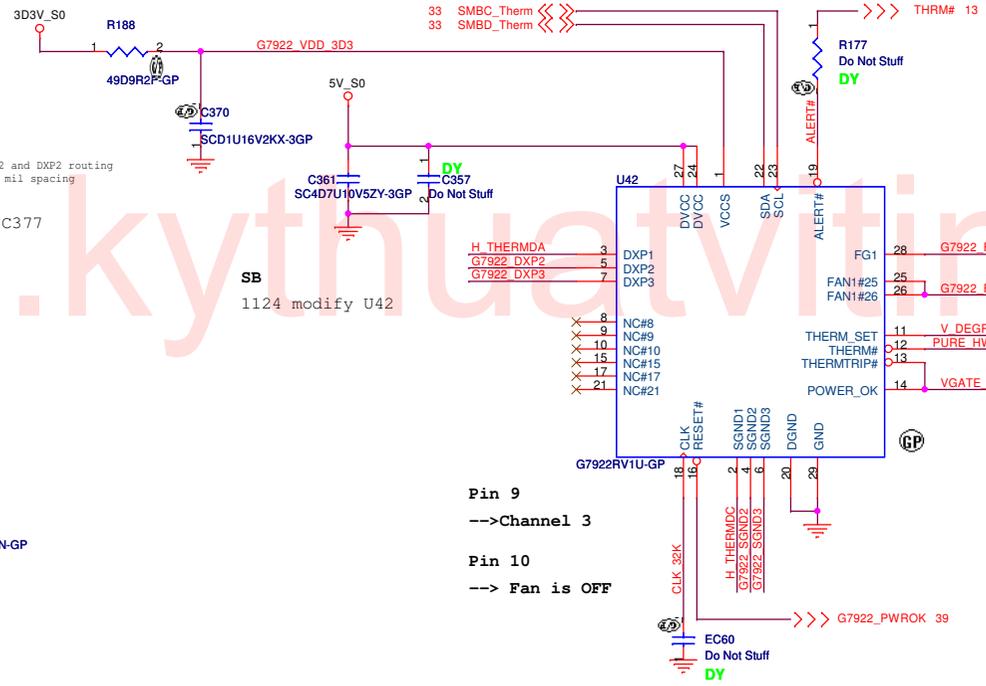
2. System Sensor, Put between CPU and NB.

Layout notice : Both SGND3 and DXP3 routing  
10 mil trace width and 10 mil spacing

C372 must be near EMC2102  
C375 must be near Q8



3. HW T8 sensor



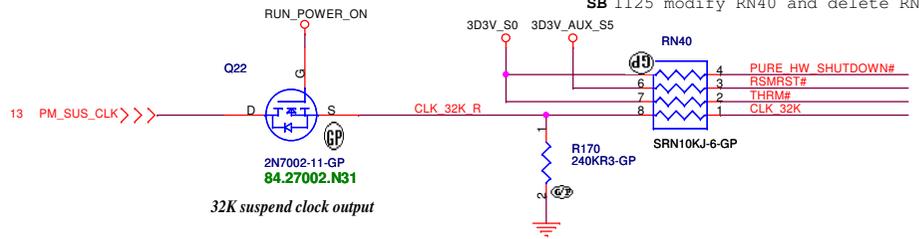
$$\text{TRIP\_SET Pin Voltage } V\_DEGREE = ((\text{Degree} - 75) / 21)$$

$$\text{THERM\_SET} = (\text{Test} - 75) * (1/32) * (15/33) \text{VCCS}$$

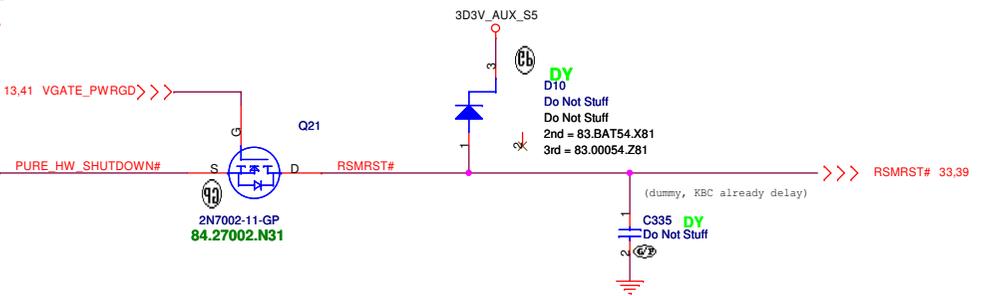
Pin 9  
--> Channel 3

Pin 10  
--> Fan is OFF

SB 1125 modify RN40 and delete RN42



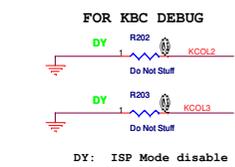
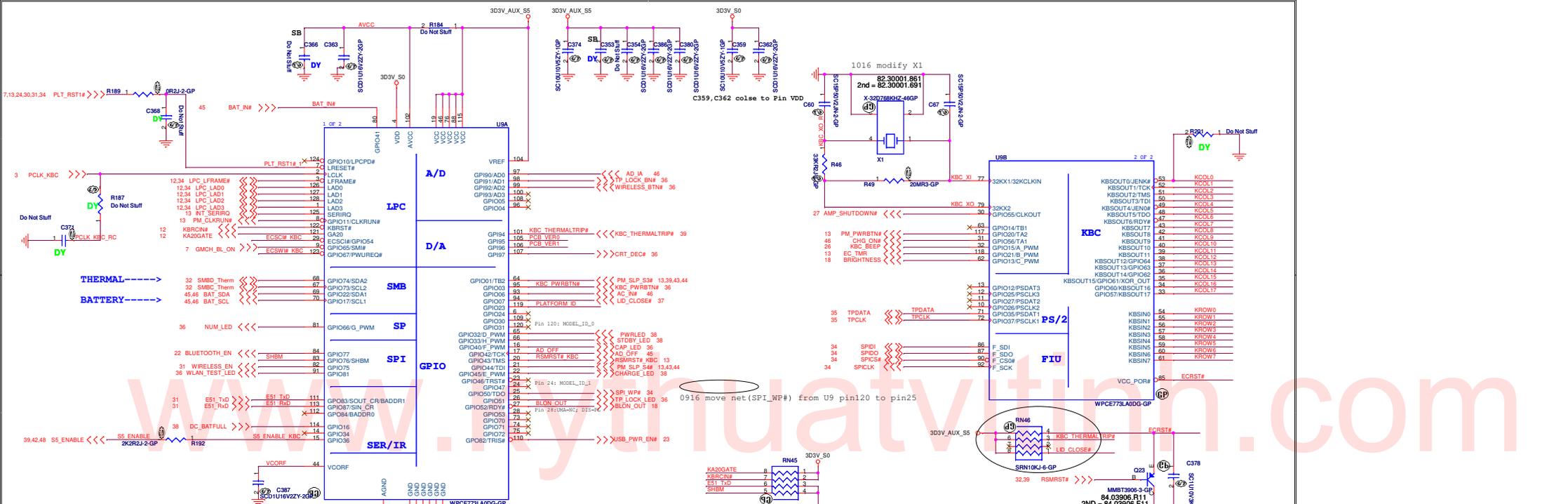
32K suspend clock output



(dummy, XBC already delay)

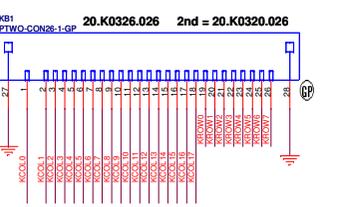
UMA Two Phase 2

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Thermal/Fan Controller</b>			
File	Document Number		Rev
	<b>HM40-MV</b>		<b>SB</b>
Date: Monday, December 01, 2008	Sheet	32 of	51



Do Not Stuff

### Internal Keyboard Connector

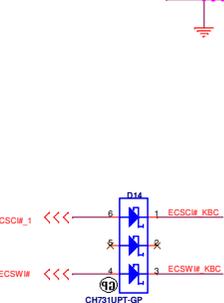


0930 modify KB1

### Internal Keyboard CONN



CHECK KB SPEC. AND PIN DEFINE



0930 modify net name for BIOS demand

PlanarID (0,1)

SA: 0,0

SB: 0,1

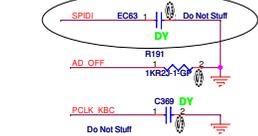
SC: 1,0

SD: 1,1

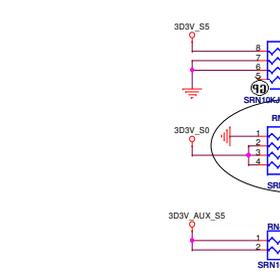
1118 modify PCB Ver. from SA to SB

0930 modify KB1

0912 add the part for EMI demand



1106 modify net connection of RN46 and RN44



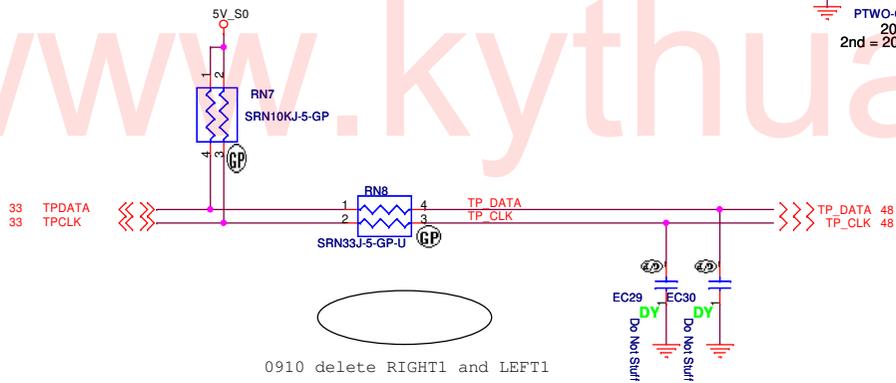
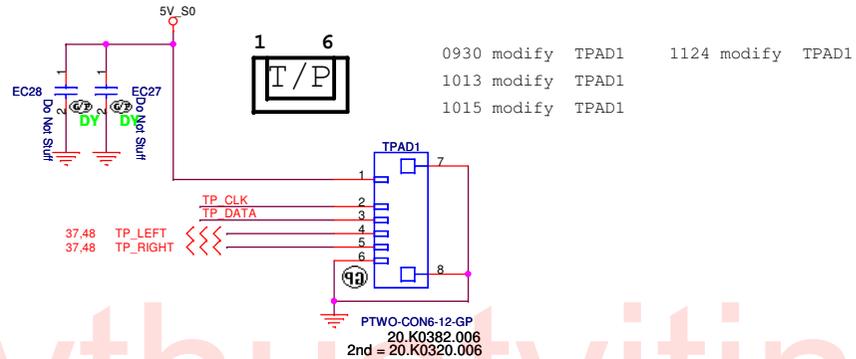
UMA Two Phase 2

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File	KBC WPCE773L		Rev	SB
Size	Document Number	HM40-MV		
Customer				
Date	Wednesday, November 28, 2008	Sheet	33	of 51

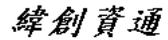


# TOUCH PAD

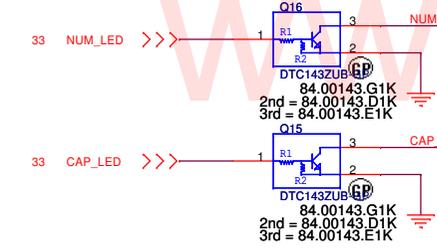
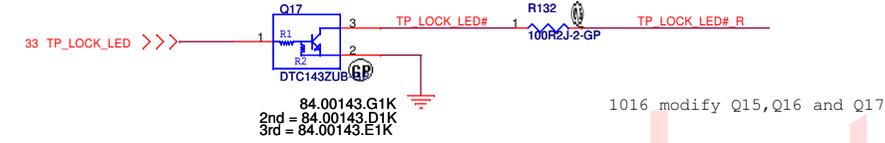
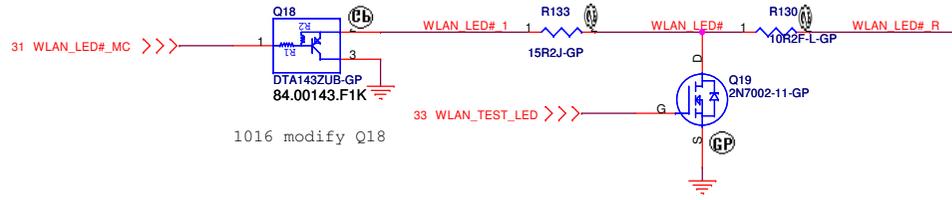


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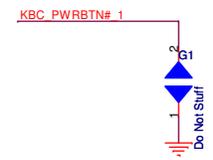
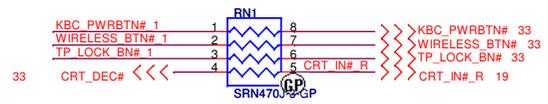
UMA Two Phase 2

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>Touch pad</b>		
Size	Document Number	Rev
	<b>HM40-MV</b>	<b>SB</b>
Date: Monday, December 01, 2008		
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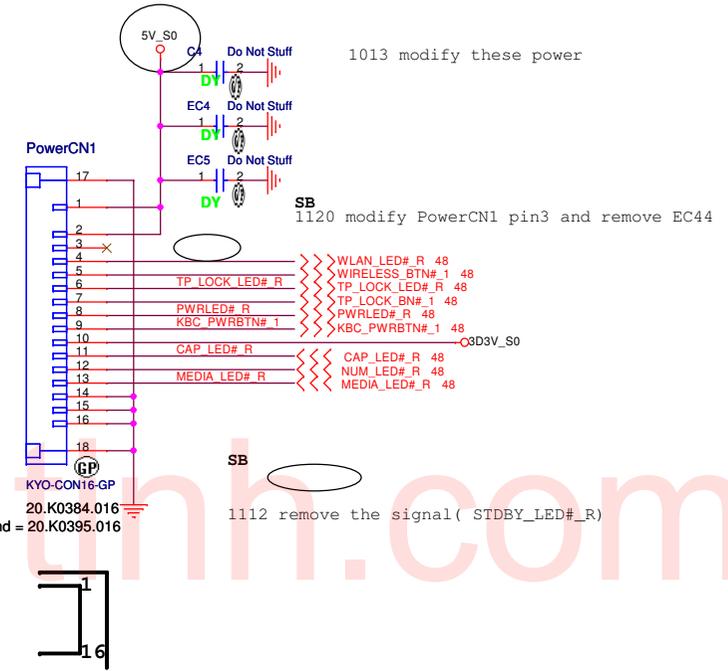
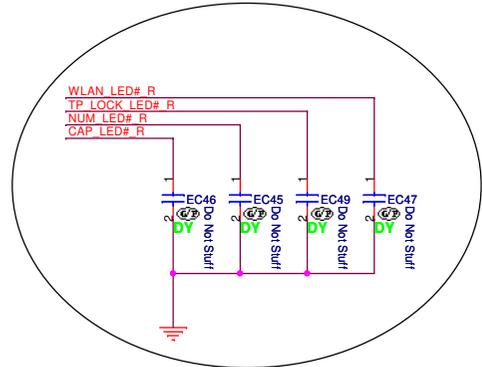
SB 1119 modify R130 and R133

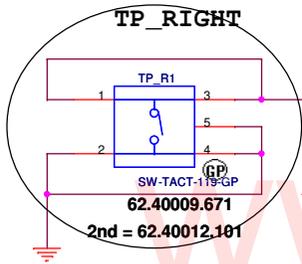
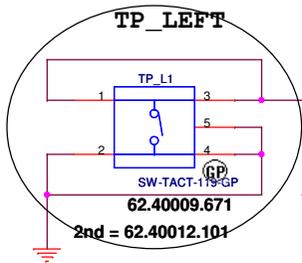


SB  
1112 remove these signals ( STDBY\_LED#\_FR and STDBY\_LED#\_R) and R131



0912 add these parts for EMI demand



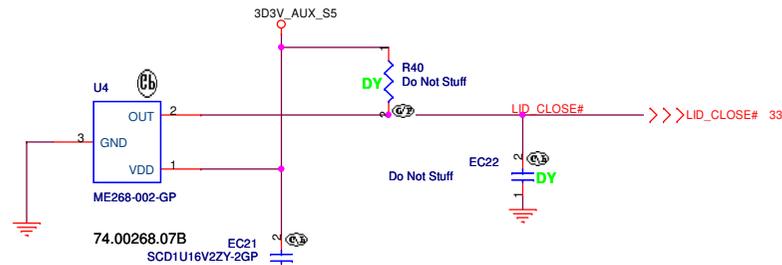


1017 modify RN60



TP\_LEFT 35,48  
TP\_RIGHT 35,48

### Cover Up Switch

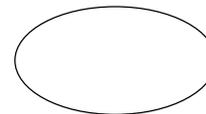


1016 modify U4

1017 modify U4

1017 add U61,R52,EC24 and EC23

1020 delete U61,R52,EC24 and EC23

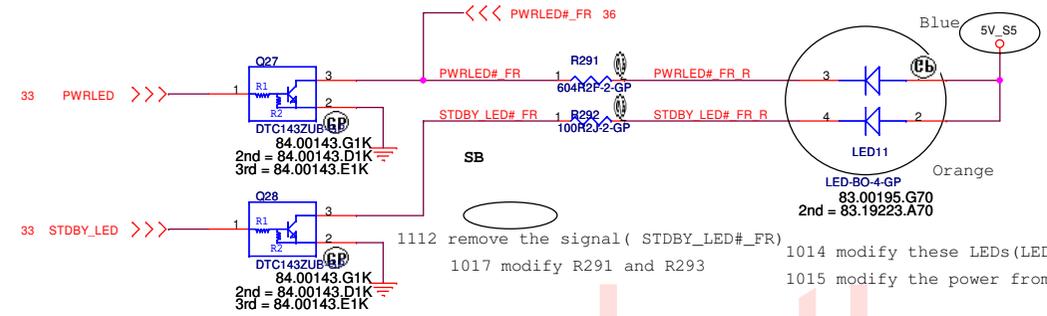


UMA Two Phase 2

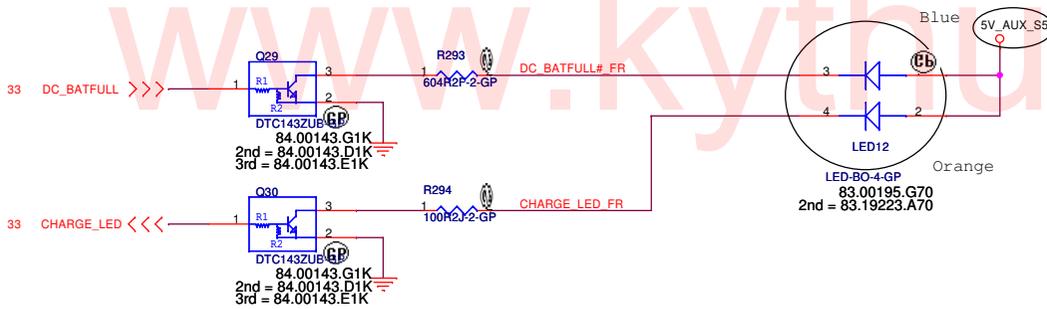
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>SWITCHS</b>			
Size	Document Number	Rev	
	<b>HM40-MV</b>	<b>SB</b>	
Date: Monday, December 01, 2008		Sheet	51

1015 modify the power from 3D3V\_S5 to 5V\_S5

SB 1106 modify LED11

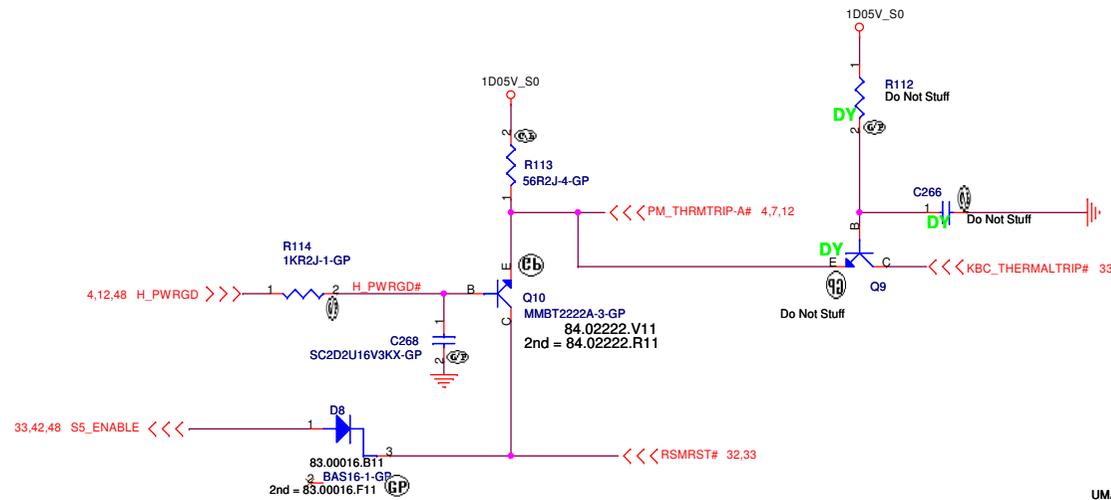
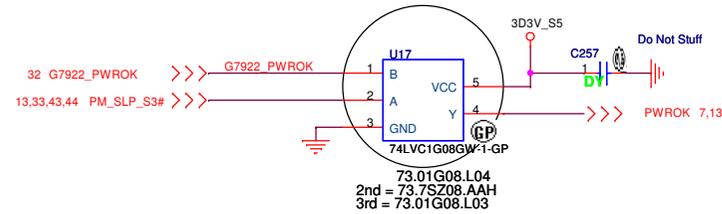
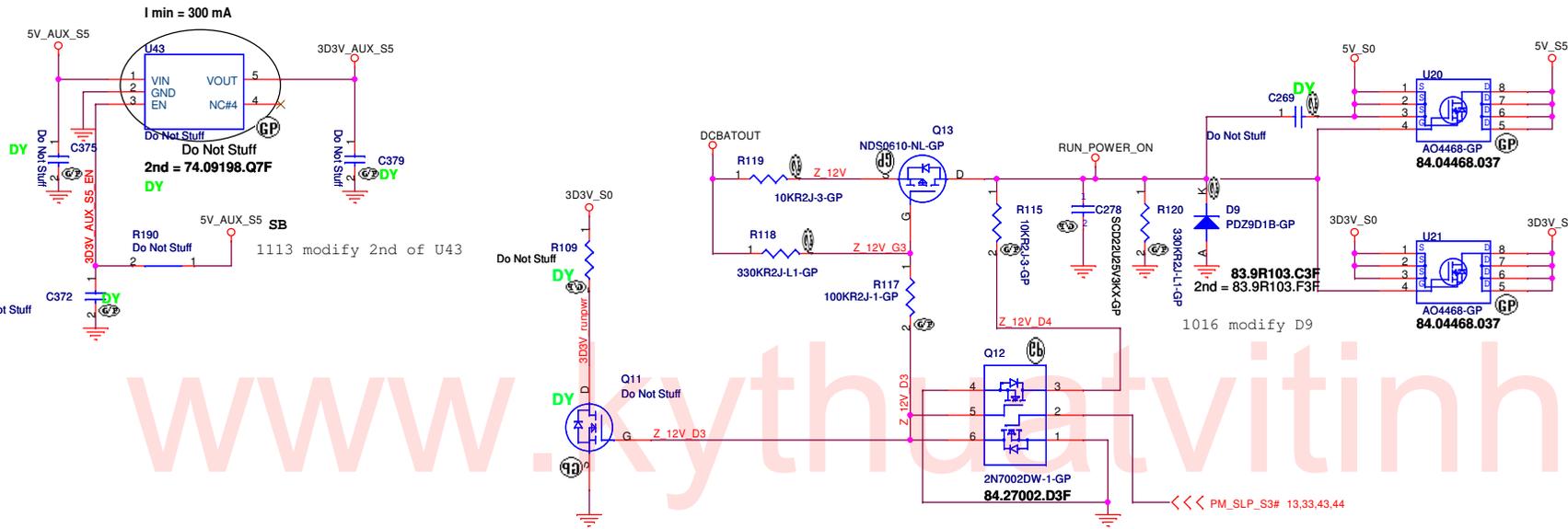


1014 modify these LEDs(LED11,LED12)  
1015 modify the power from 3D3V\_S5 to 5V\_S5



1016 modify Q27~Q30

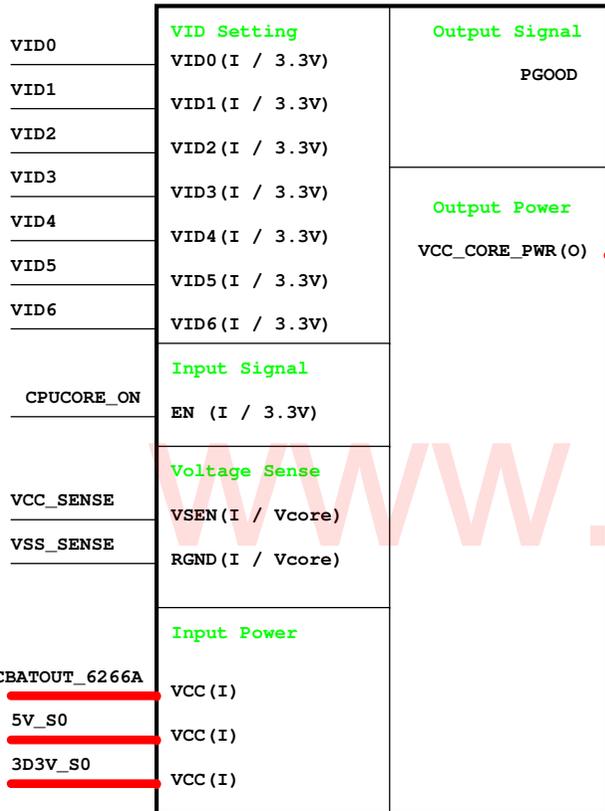
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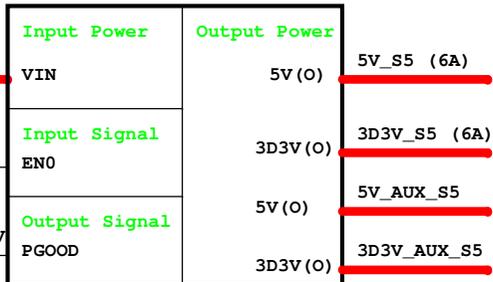
UMA Two Phase 2

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>File</b> RUN POWER and 3D3V_AUX_S5			
Size	Document Number	Rev	SB
<b>HM40-MV</b>			
Date:	Monday, December 01, 2008	Sheet	39 of 51

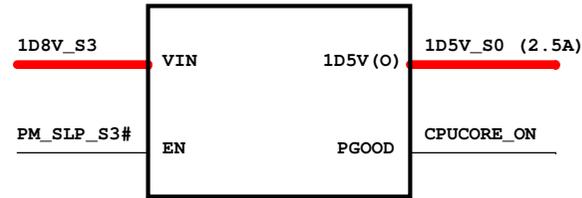
**CPU\_CORE**  
ISL6266A



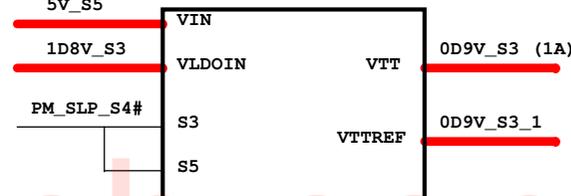
**TPS51125**  
5V/3D3V



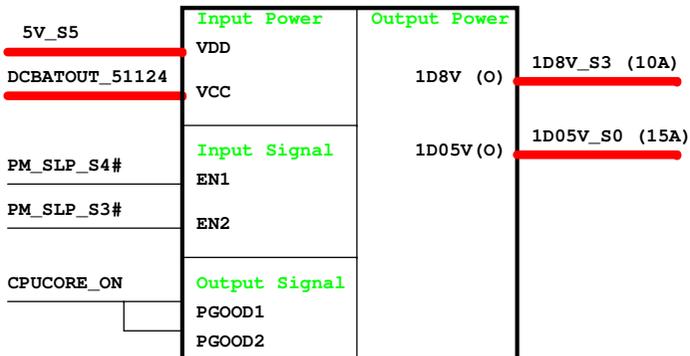
**RT9018A**  
1D5V\_S0



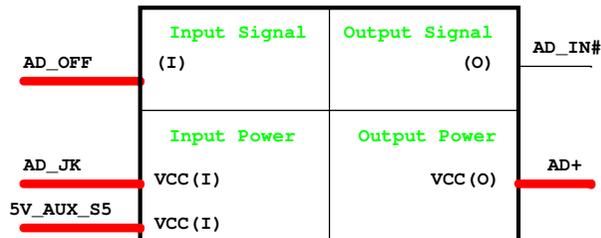
**RT9026** 0D9V\_S0



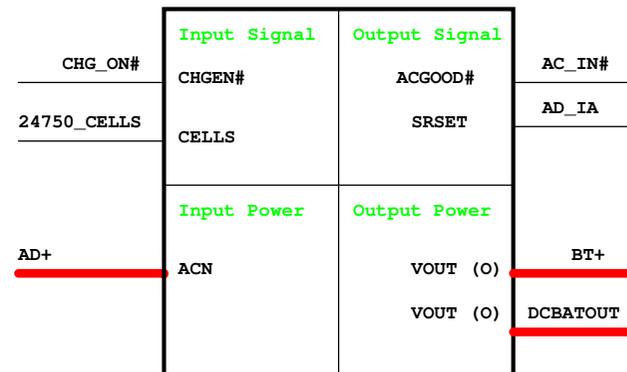
**TPS51124**  
1D8V/1D05V



**Adapter**



**Charger BQ24745**

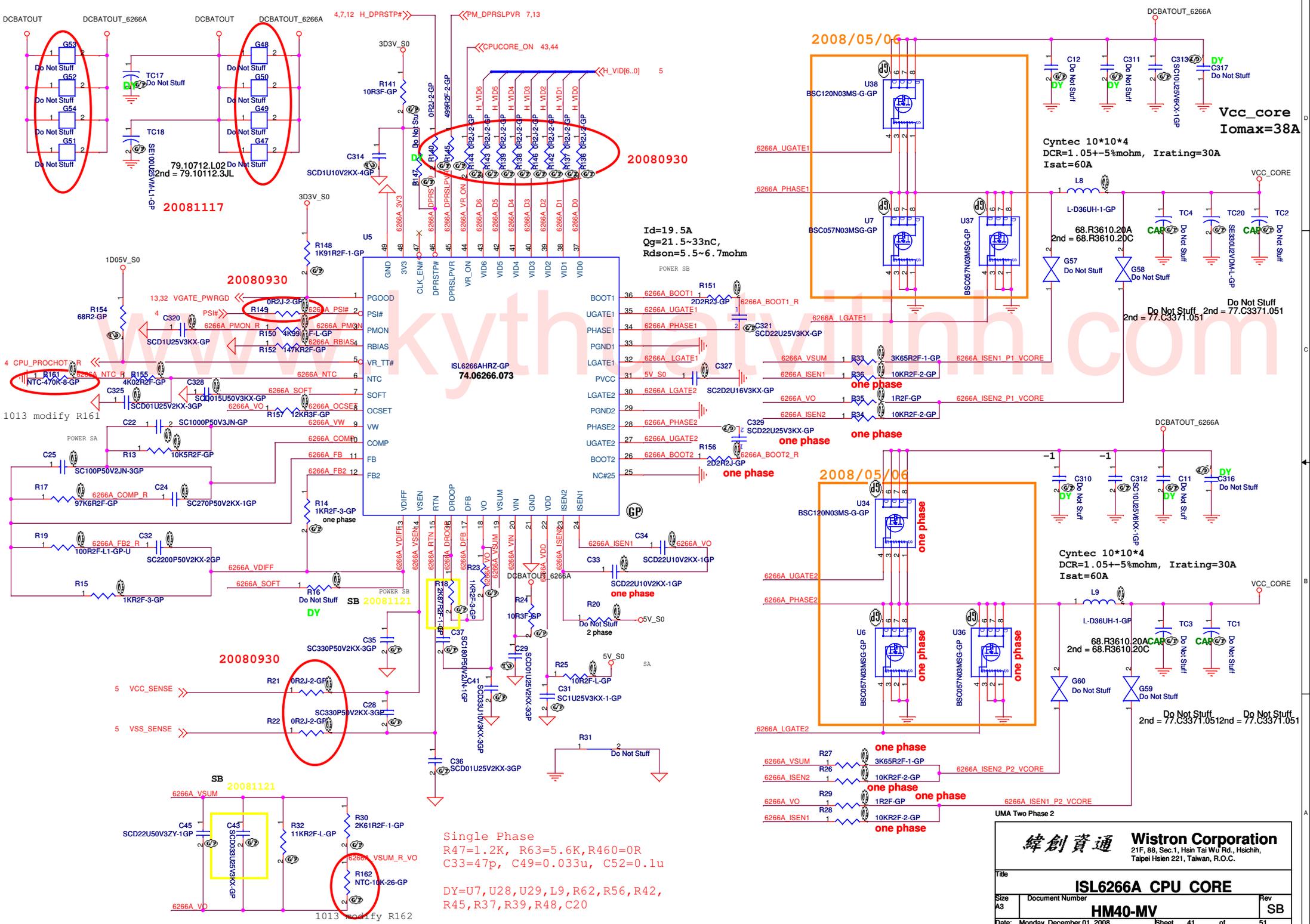


UMA Two Phase 2

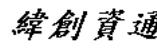
緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **Power Sequence Logic**

Size B	Document Number	Rev
	<b>HM40-MV</b>	<b>SB</b>
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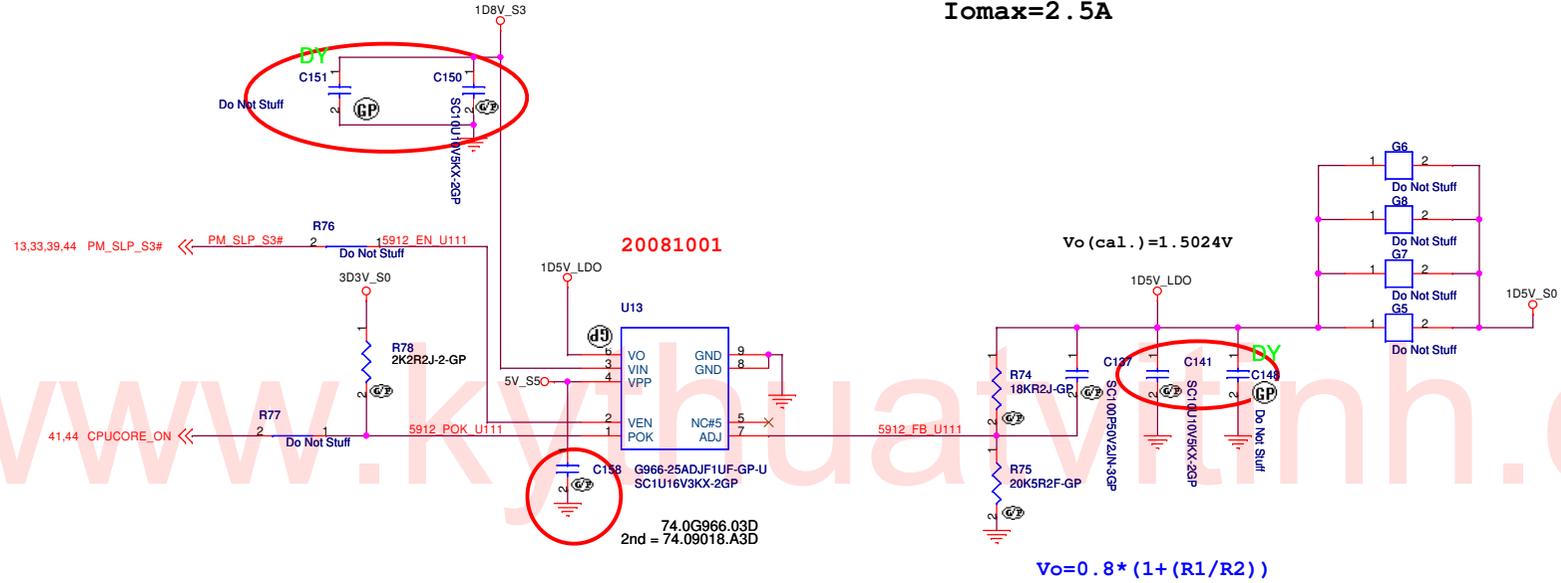


Single Phase  
 R47=1.2K, R63=5.6K, R460=0R  
 C33=47p, C49=0.033u, C52=0.1u  
 DY=U7, U28, U29, L9, R62, R56, R42,  
 R45, R37, R39, R48, C20

 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>ISL6266A CPU CORE</b>	
Title <b>ISL6266A CPU CORE</b>	Document Number <b>HM40-MV</b>
Size A3	Rev <b>SB</b>
Date: Monday, December 01, 2008	Sheet 41 of 51

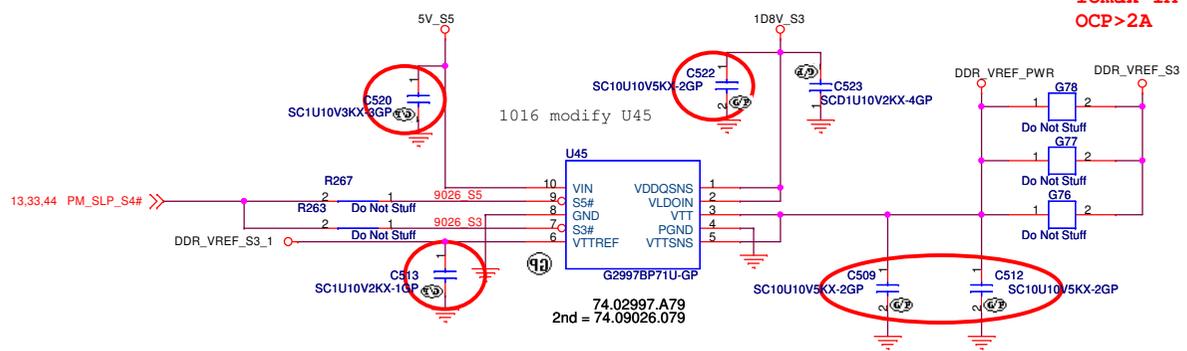


**1D5V\_S0**  
**I<sub>omax</sub>=2.5A**



**20081001**

**I<sub>omax</sub>=1A**  
**OCP > 2A**

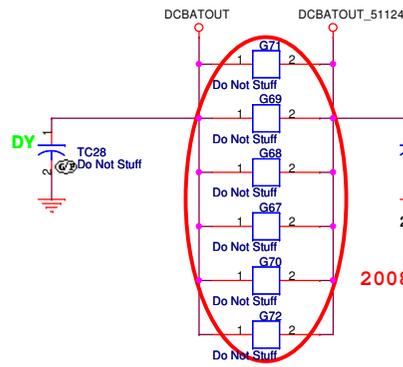


UMA Two Phase 2

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

File: **1D5V & 0D9V**

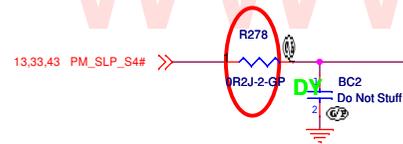
Size A3	Document Number <b>HM40-MV</b>	Rev <b>SB</b>
Date: Monday, December 01, 2008	Sheet 43 of	51



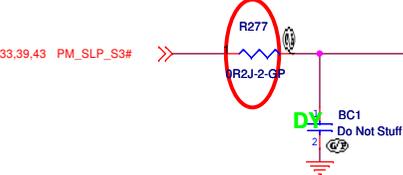
$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$   
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$   
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

20081117

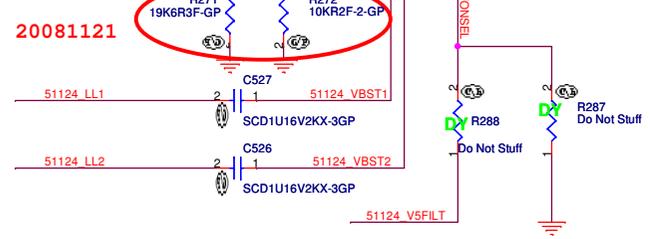
2008/06/16



20080930



20081121



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2) / R2$  --> PWM mode  
 $V_{out} = 0.764V * (R1+R2) / R2$  --> Skip Mode

$I_d = 7A$   
 $Q_g = 8.7 \sim 13nC$   
 $R_{dson} = 23 \sim 30mohm$

$I_d = 7.7A$   
 $Q_g = 8.5 \sim 13nC$   
 $R_{dson} = 16.5 \sim 21mohm$

$I_d = 7.7A$   
 $Q_g = 8.5 \sim 13nC$   
 $R_{dson} = 16.5 \sim 21mohm$

SB 1128 add TC26

$79.3971V.EOL$   
 $2nd = 79.3971V.EOL$

Cyntec 10\*10\*4  
 $DCR = 4.2mohm$ ,  $I_{rating} = 16A$   
 $I_{sat} = 33A$

$1D8V I_{omax} = 10A$   
 $OCP > 15A$

$1D05V I_{omax} = 14A$   
 $OCP > 24A$

SB 1128 add TC25

1017 add TC25

Do Not Stuff  
2nd = 79.3971V.EOL

UMA Two Phase 2

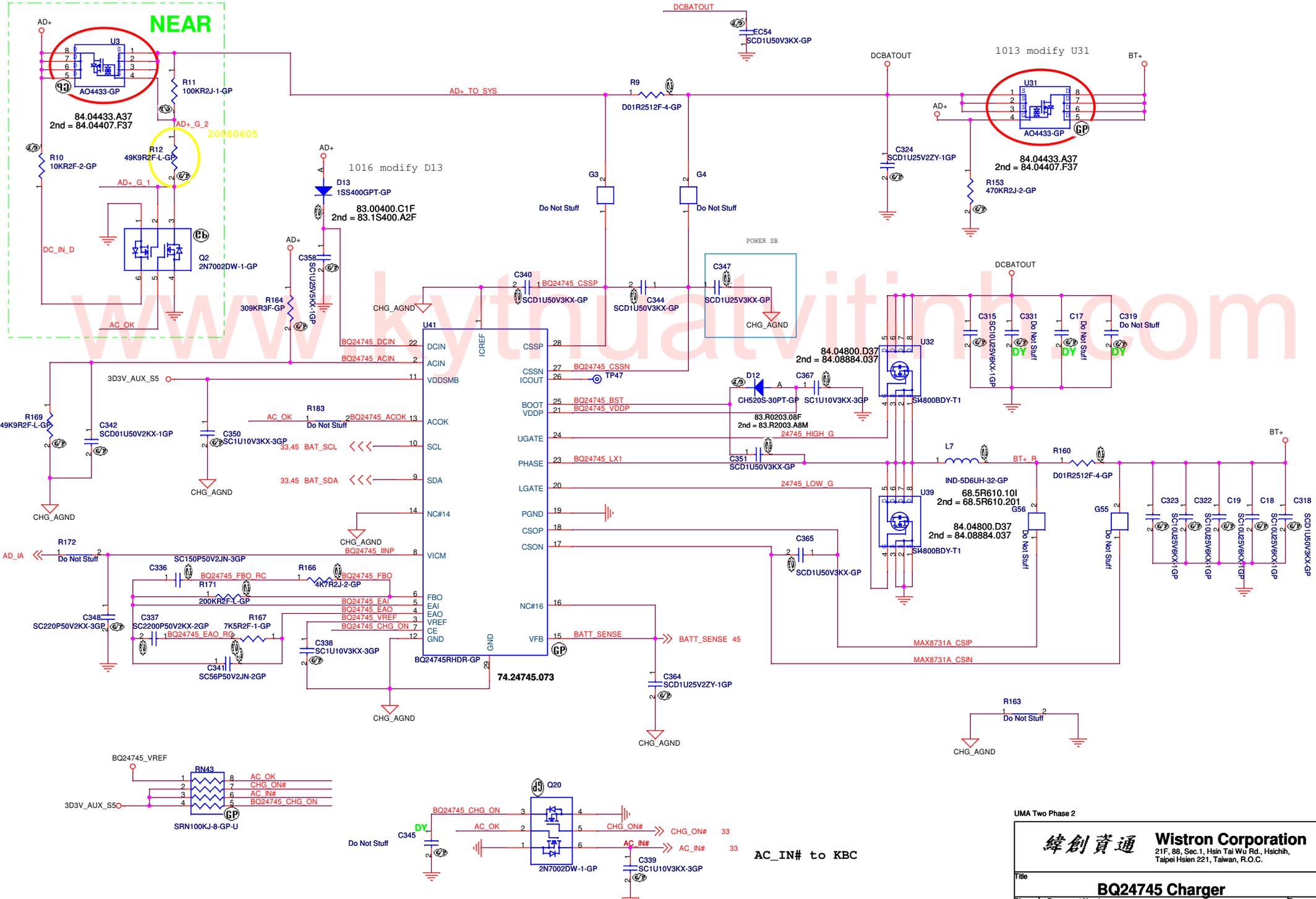
緯創資通 Wistron Corporation  
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Title			TPS51124 1D8V 1D05V		
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1013 modify U3

NEAR

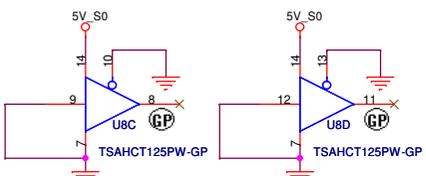


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Title		<b>BQ24745 Charger</b>	
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AC\_IN# to KBC



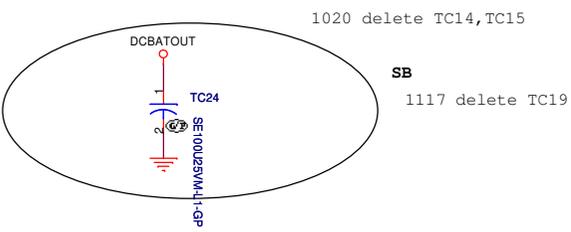
73.74125.L13  
2nd = 73.74125.L12

73.74125.L13  
2nd = 73.74125.L12

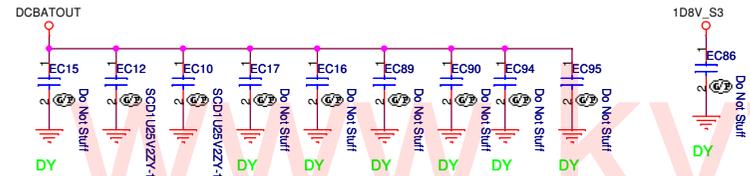
1016 modify U32

1017 add these parts (EC10, EC12, EC15~EC17, EC86) for EMI demand

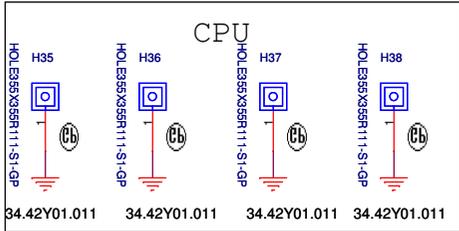
1020 add the part (EC86) for EMI demand      1125 add the part (EC90) for EMI demand  
**SB** 1121 add the part (EC89) for EMI demand      1128 add EC94, EC95 for EMI demand



79.10712.L02  
2nd = 79.10112.3JL

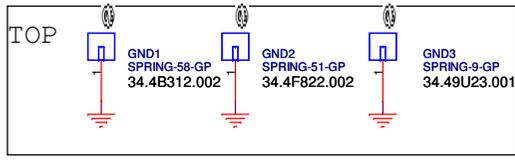


1016 add GND1 and GND2 for EMI demand  
 1017 add GND3 and modify GND2 for EMI demand

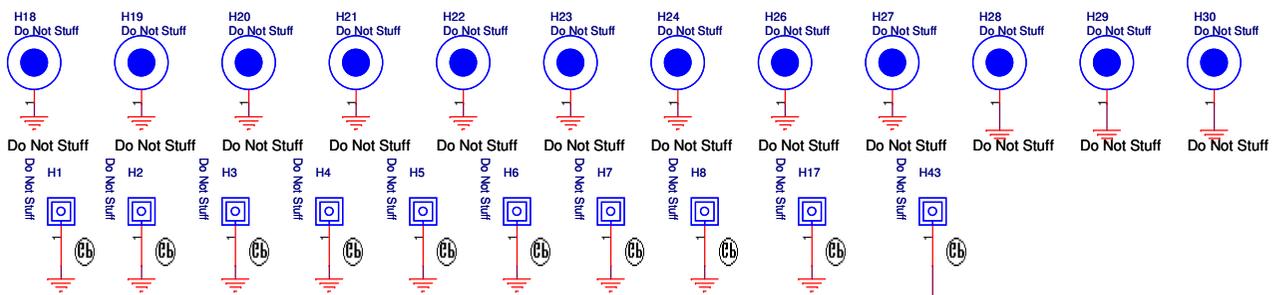


1016 modify H35-H38  
 1016 delete H9-H12

1016 modify H31 and H32  
**SB** 1120 remove H31 and H32



**SB** 1128 Add GND4, GND7, GND8



**SB** 1128 Add H43

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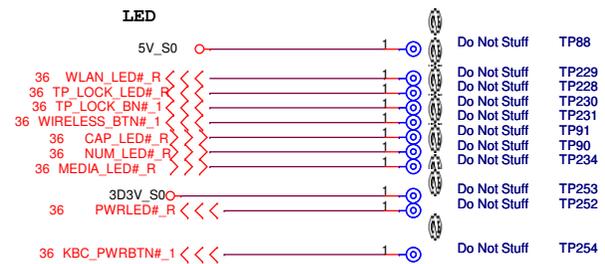
Title: **EMI/Spring/Boss**

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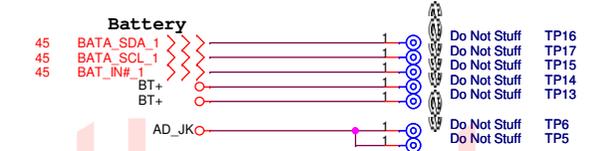
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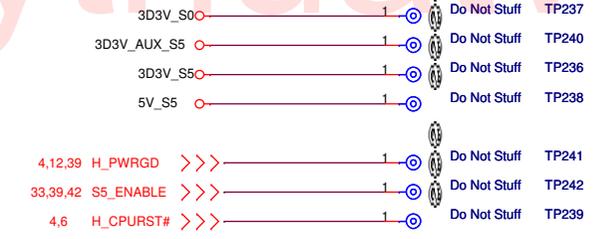
1017 modify USB signal connection



SB  
1112 remove the signal( STDBY\_LED#\_R)



**Check test point**



**Test Point放在Dimm Door打開可量測處**

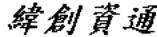


UMA Two Phase 2

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<b>AFTE test point</b>			
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0910 delete F4(Page 18)  
 0910 update footprint of U15(Page 30)  
 0910 delete RIGHT1 and LEFT1(Page 33)  
 0910 modify net names of TP\_LEFT and TP\_RIGHT(Page 36)  
 0910 modify test points of AFTE and TPAD  
 0911 modify net name from LPC\_RST to PLT\_RST1#(Page 24)  
 0911 add net name(RBIAS,LED\_DUPLEX#,SMDATA,SMCLK)(Page 24)  
 0911 add net name(DVDD\_1\_8,ACZ\_SDATAIN0\_R,FLY\_P,FLY\_N,VREF\_LO,VREF\_HI)(Page 26)  
 0911 add net name(EAPD#\_R)(Page 27)  
 0912 modify the schematic of Page 33  
 0912 delete GMCH\_TXB\*(Page 7& 18)  
 0912 add these parts for EMI demand(page 7,18,20,21,23,26,28,29,30,32,33,34,35)  
 0915 modify net name from 10M/100M/1G\_LED# to 10M/100M\_LED#(page24,25)  
 0915 delete these parts for EMI demand(page 30)  
 0915 add EC34 for EMI demand(page3)  
 0915 add EC73 for EMI demand(page 12)  
 0915 modify LEDs port  
 0916 move net (SPI\_WP#) from U9 pin120 to pin25(page33)  
 0930 modify BLUE1(page22)  
 0930 add 2nd for SPK1, MIC1 and modify LOUT1 (page28)  
 0930 modify FAN1(page32)  
 0930 modify TPAD1(page35)  
 0930 modify KB1(page33)  
 0930 modify net name for BIOS demand(page33)  
 1001 delete these parts for EMI demand(ED1~8)  
 1009 modify net name for GND to AGND(page27)  
 1009 add R4,R5 for AC decoupling(page27)  
 1009 add R96(page30)  
 1013 modify TPAD1(page35)  
 1013 modify U40 from 72.25X16.001 to 72.25X16.A01(page 34)  
 1013 modify TC11 and add TC12(page42)  
 1013 modify TC10 and add TC26(page44)  
 1013 modify U2(page45)  
 1013 modify U3 and U31(page 46)  
 1013 modify R161 and R162(page41)  
 1013 modify card1(page 30)  
 1014 modify these LEDs(LED11,LED12)(page38)  
 1014 modify these nets(page 26)  
 1014 modify R258 from 10k to 20k ohm(page26)  
 1014 add ER5 for EMI deamnd(page3)  
 1015 modify LCD1 pin define(page 18)  
 1015 modify the power from 3D3V\_S5 to 5V\_S5(page38)  
 1015 modify TPAD1(page35)  
 1015 modify RN57(page28)  
 1015 modify F1(page18)

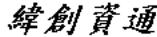
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1016 modify L1,L2 and L3(page 19)  
 1016 modify XF1(page 25)  
 1016 modify RN53 and U10(page 24)  
 1016 modify U8 (page19,47)  
 1016 modify U4(page 37)  
 1016 modify U23(page 43)  
 1016 modify X2(page12)  
 1016 modify X1(page 33)  
 1016 modify X3(page 3)  
 1016 modify D13(page 46)  
 1016 modify D23(page 20)  
 1016 modify D9(page 39)  
 1016 modify D4(page 19)  
 1016 modify Q3 and Q4(page45)  
 1016 modify Q18(page 36)  
 1016 modify Q15~Q17(page 36)  
 1016 modify Q27~Q30(page38)  
 1016 modify Q6 and Q14(page 32)  
 1016 modify Q8(PAGE 24)  
 1016 add GND1 nad GND2 for EMI demand(page 47)  
 1016 modify LCD1 pin define(page 18)  
 1016 delete H9-H12 and modify H35-H38,H31,H32(page 47)  
 1017 add these parts for EMI demand(page 47)  
 1017 delete these parts(EC208~EC210) (page 7)  
 1017 modify BLUE1(page 22)  
 1017 modify FAN1 (page 32)  
 1017 modify R291 and R293(page 38)  
 1017 add U61,R52,EC23 and EC24(page 37)  
 1017 modify RN60(page37)  
 1017 add TC25(page 44)  
 1017 add GND3 and modify GND2 for EMI demand(page 47)  
 1017 modify USB signal connection(page13,18,22,23,30,31,48)  
 1020 delete C537 for Power demand(page42)  
 1020 add the part(EC86) for EMI demand(page 47)  
 1020 delete U61,R52,EC24 and EC23(page 37)  
 1020 delete TC14,TC15(page 47)  
 1021 modify TC16(page 31)  
 1021 delete TC23(page 23)  
 1021 modify TC5(page 20)  
 1021 modify and swap these parts(USB1 and USB2) (page 23)  
 1021 modify SATA1(page 20)  
 1022 modify DC1(page 45)

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1106 modify net connection of RN46 and RN44(page33) for layout demand  
 1106 modify LED11 and LED12(page38) for fixing issue  
 1106 modify LED power from 5V\_S5 to 5V\_AUX\_S5(page38) for customer demand  
 1112 remove the signal(STDBY\_LED#\_FR)page38 for customer demand  
 1112 remove these signals( STDBY\_LED#\_FR and STDBY\_LED#\_R) and R131(page36) for customer demand  
 1112 remove the signal( STDBY\_LED#\_R)page36 for customer demand  
 1112 remove the signal( STDBY\_LED#\_R)and TP253(page48) for customer demand  
 1113 modify C103 and C106(page24) for crystal issue  
 1113 modify 2nd of U19(page26)  
 1113 modify 2nd of U43(page39)  
 1113 modify 2nd of U44(page10)  
 1113 modify U48(page22)  
 1117 delete MDC function(R231,R237,R232,R234) (page12)  
 1117 delete TC19(page 47) for ME deamnd  
 1118 modify PCB Ver. from SA to SB(page33)  
 1118 delete TC12(page42) for layout demand  
 1118 delete TC27(page9) for layout demand  
 1118 delete R107 and add L18 for cost down  
 1119 modify R130 and R133(page 36) for LED brightness  
 1119 modify EC52 and EL3(page45) for EMI demand  
 1119 modify SPK1(page 28) for ME deamnd  
 1119 add G84 for RTC reset demand  
 1120 modify EC78for EMI demand((page10)  
 1120 modify PowerCN1 pin3 and remove EC44(page36) fro LED function  
 1120 remove H31 and H32(page47)for ME demand  
 1120 add RN61 and RN62(page3) for layout demand  
 1120 swap these nets(CLK\_MCH\_3GPLL,CLK\_MCH\_3GPLL#, CLK\_PCIE\_MINI1,CLK\_PCIE\_MINI1#) (page3)for CLK REQ demand  
 1120 add the net( SATACLKREQ#) (page3,13)for CLK REQ demand  
 1120 move these nets (CLK\_PCIE\_MINI1,CLK\_PCIE\_MINI1#) (page3)for CLK REQ demand  
 1120 modify RN61 and RN62(page3)for CLK REQ demand  
 1121 add EC87 for EMI demand(page18)  
 1121 add the part(EC89) for EMI demand(page47)  
 1121 add the part(EC88) for EMI demand(page45)  
 1121 modify R18,C43(page41) for Power demand  
 1121 modify R275 (page42)for Power demand  
 1121 modify R271,R272,R286 and L16(page44) for Power demand  
 1124 modify U42 and delete R182,R185 (page32) for thermal function  
 1124 modify these names of these nets(G7922\_SGND2,G7922\_SGND3...) (page32) for thermal function  
 1124 add R302(page3) for clock gen function  
 1125 add the part(EC90) for EMI demand(page47)  
 1125 add the part(EC91) for EMI demand(page45)  
 1125 modify R125,R126(page18) for LCD brightness control  
 1125 modify RN40 and delete RN42(page32) for layout demand  
 1125 add EC92 and EC93 for EMI demand(page 22)  
 1126 add these nets (PCIE\_REQ\_LAN#,PCIE\_REQ\_MINI#) (page3)for CLK REQ demand  
 1126 delete R230,R233,R235,R236 and RN63(page12) for removing MDC function  
 1126 add C541 and modify R101(page26) for codec function  
 1126 modify RN61 and RN62(page3) for layout demand  
 1126 modify EU1,EU2 and add EU3,EU4 for EMI demand(page28)  
 1127 modify CRT1(page19) for customer demand  
 1127 swap the nets of RN61 and RN62 for layout demand(page3)  
 1127 modify BAT1(page45) for ME demand  
 1127 modify U27(page44) for power demand

1127 modify C377(page32) for thermal function  
 1128 Add H43,GND4,GND7,GND8(page47) for EMI demand  
 1128 modify LCD1(page18) for cost down  
 1128 Add L19(page24) for vender demand  
 1128 add EC94,EC95 for EMI demand(page47) demand

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<b>Change List</b>			
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