Model Name: KML50 DIS
PCB NO: LA-4595PR04
BOM P/N: DA80000DR00

Half Penny Bridge 15.4
Compal Confidential

Schematic Document

Cantiga + ICH9

2009 / 02 / 17 Rev:1.0(A00)

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

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Title: *Cover Sheet*

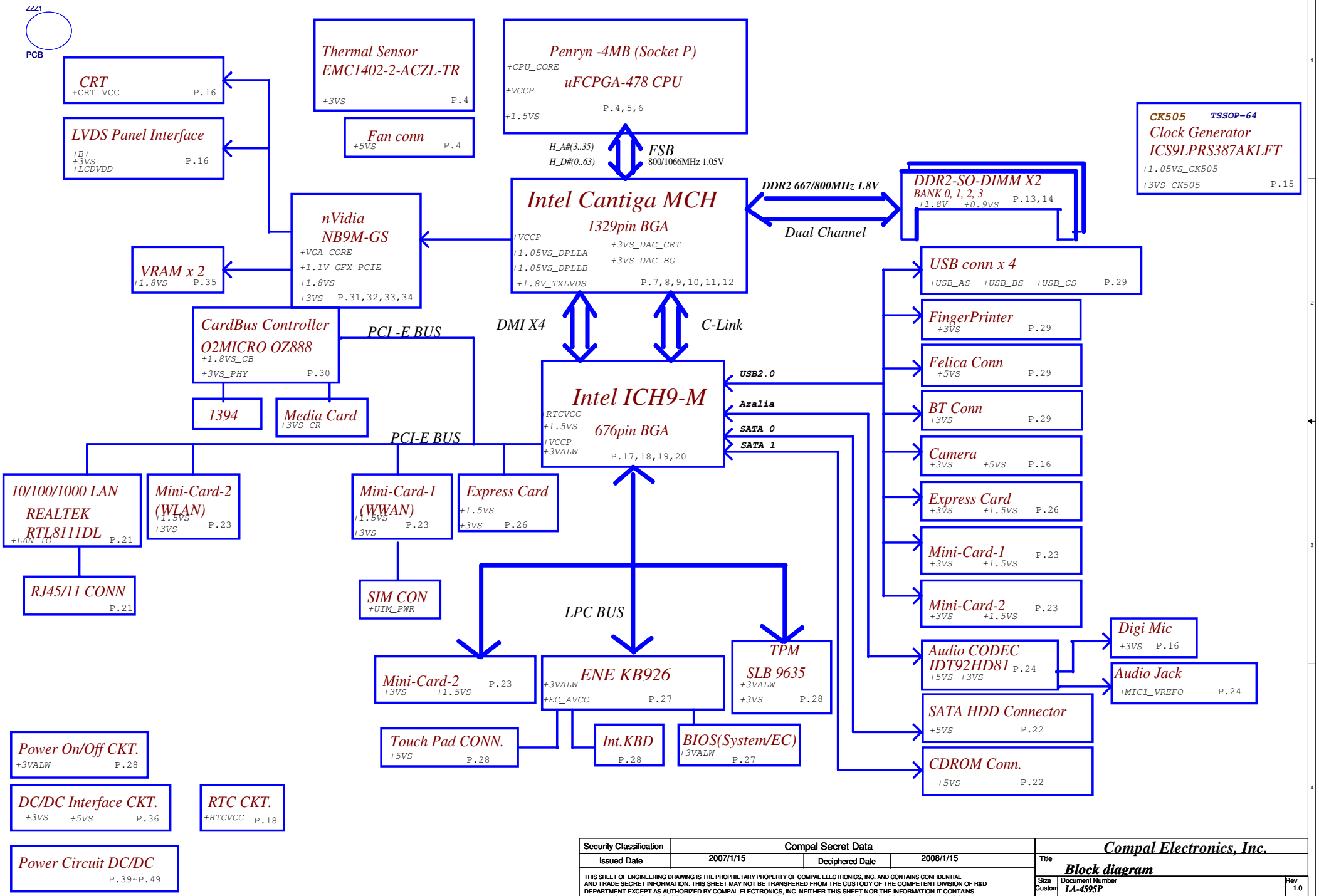
Size: Custom | Document Number: *LA-4595P* | Rev: 1.0

Date: Tuesday, February 17, 2009 | Sheet 1 of 49

Compal confidential

File Name : LA-4595P

Half Penny Bridge 15.4 DIS



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

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Title: Block diagram

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 2 of 49

Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +1.1V_GFX_PCIEP
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CON@ : means ME connectors
TPM@ : means TPM function

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

	USB PORT#	DESTINATION
ICH9-M	0	JUSBP1
	1	CAMERA
	2	JUSBP3 TOP
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3 BOT
	9	JMINI1-WWAN
	10	JUSBP4
	11	NA

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
LED panel	58	01011000

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

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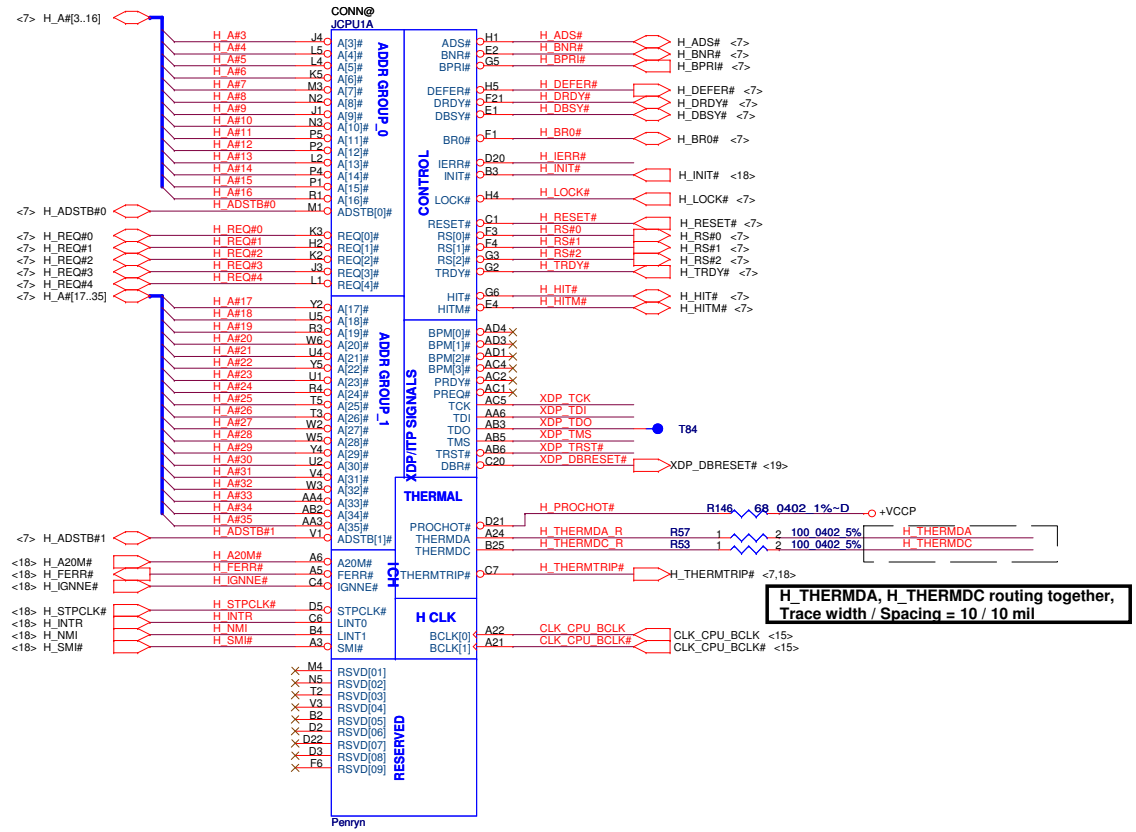
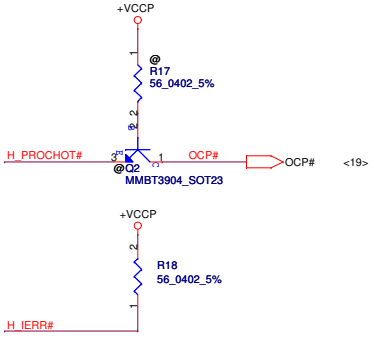
Title: Notes List

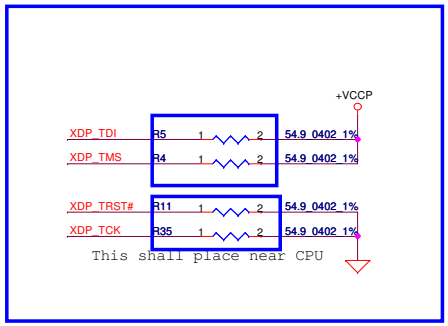
Size: Custom | Document Number: LA-4595P | Rev: 1.0

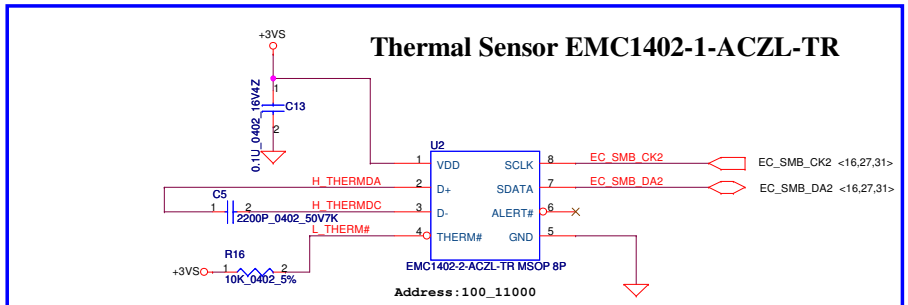
Date: Tuesday, February 17, 2009 | Sheet 3 of 49

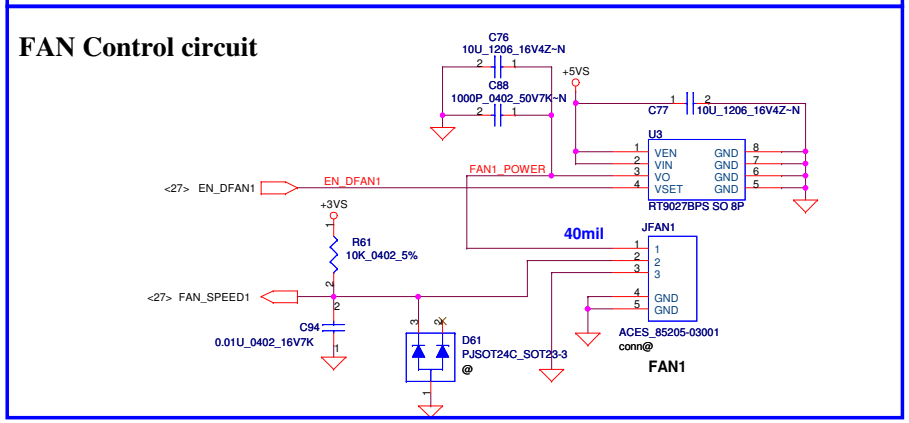


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



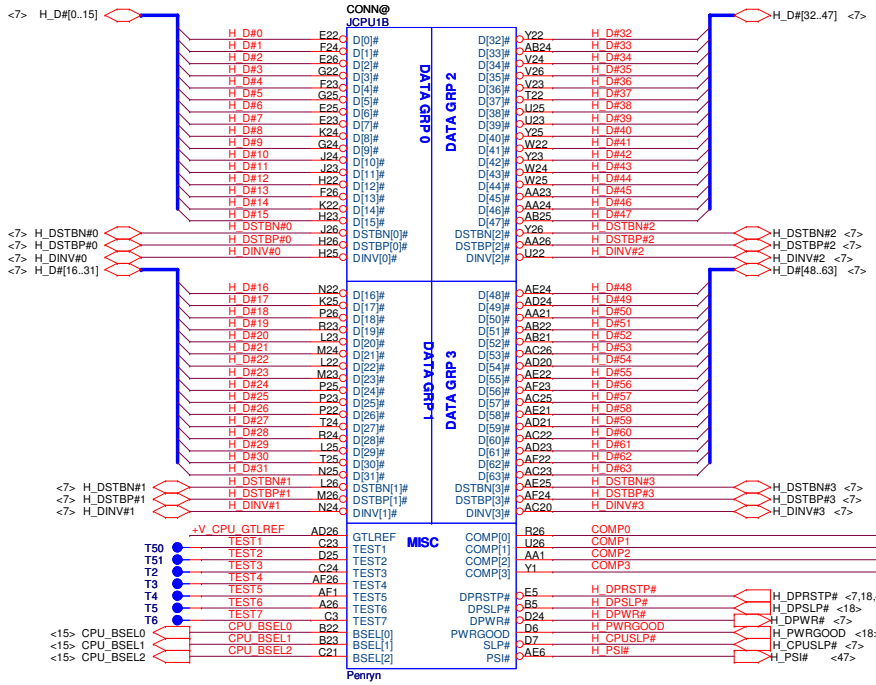


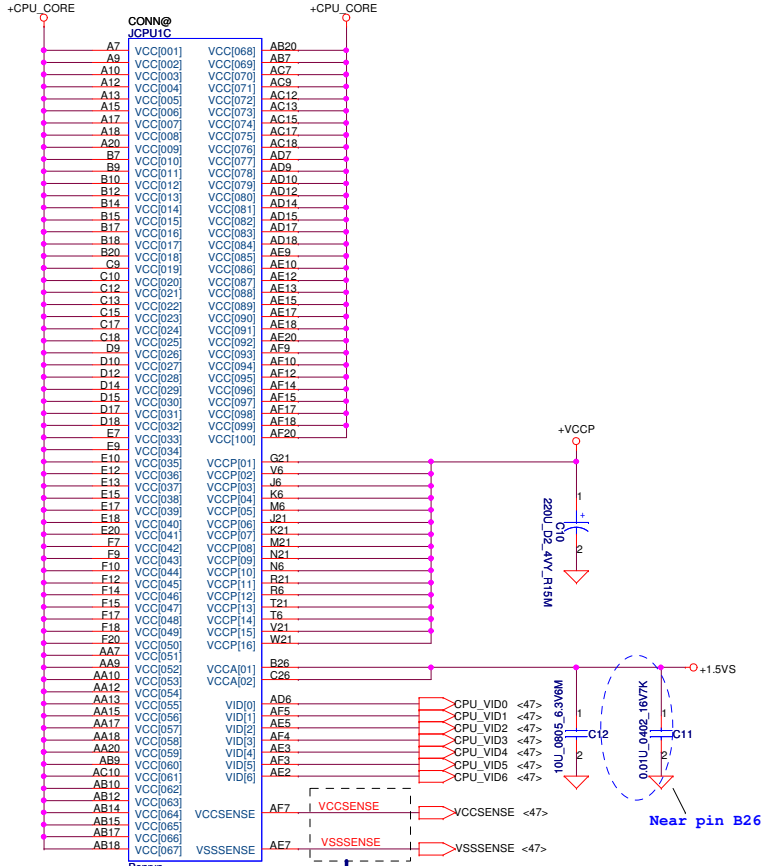




Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title	Penryn(1/3)-AGTL+/ITP-XDP		
Size: Custom	Document Number: LA-4595P		Rev: 1.0
Date: Tuesday, February 17, 2009	Sheet 4 of 49		



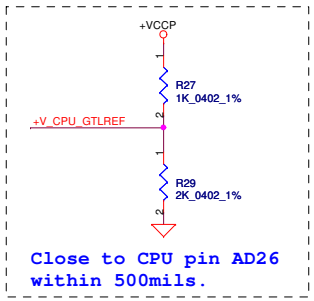


layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

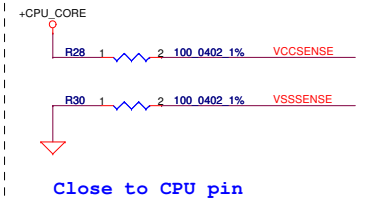
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4



Close to CPU pin AD26 within 500mils.

For 8 layer condition
Length match within 25 mils.Z0=27.4 ohm
The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Penryn(2/3)-AGTL+/ITP-XDP

Size	Document Number	Rev
Custom	LA-4595P	1.0

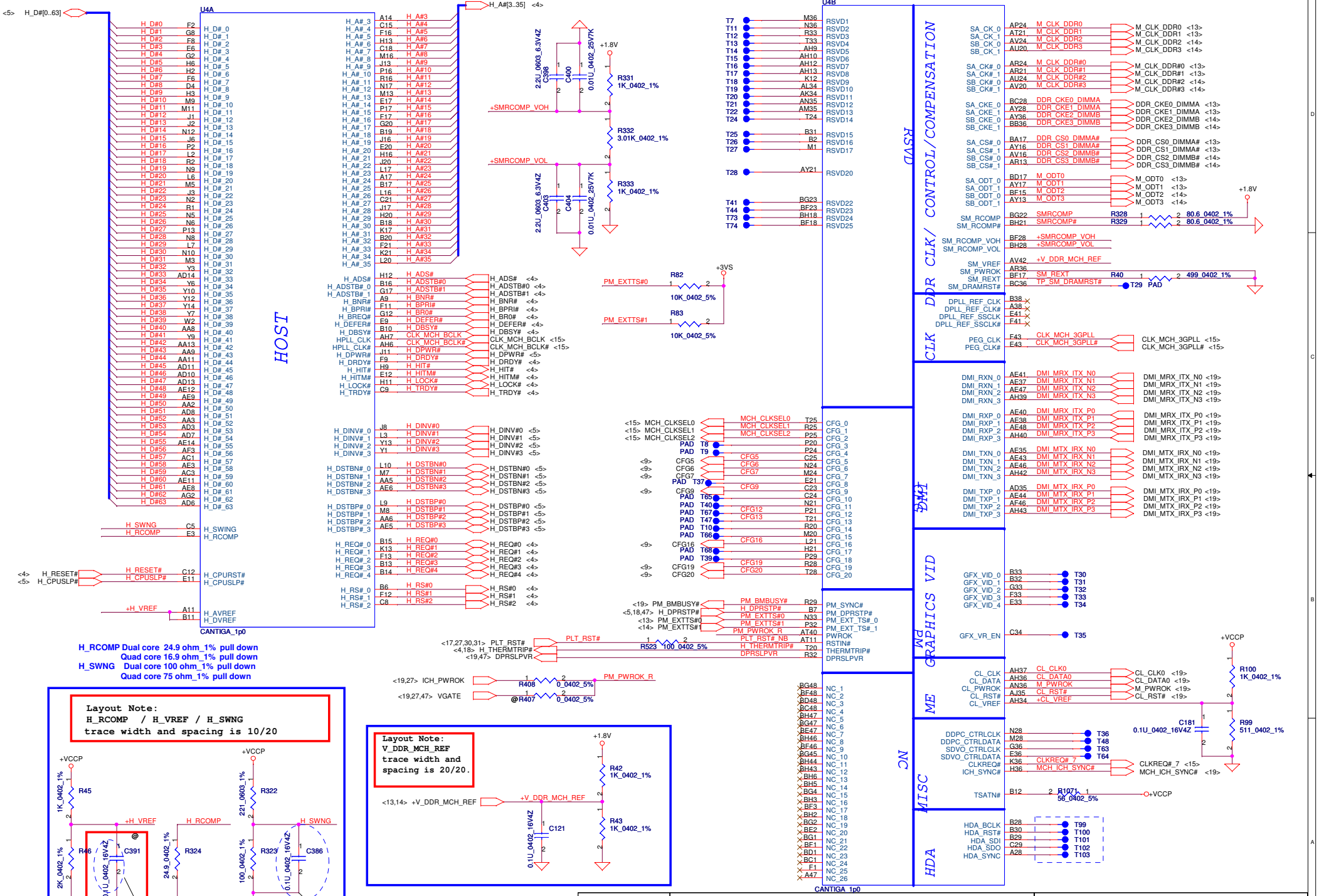
Date: Tuesday, February 17, 2009 | Sheet 5 of 49

High Frequence Decoupling

10uF 0805 X5R -> 85 degree.

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: Penryn(3/3)-AGTL+/ITP-XDP			
Size: Custom	Document Number: LA-4595P		Rev: 1.0
Date: Tuesday, February 17, 2009	Sheet 6 of 49		



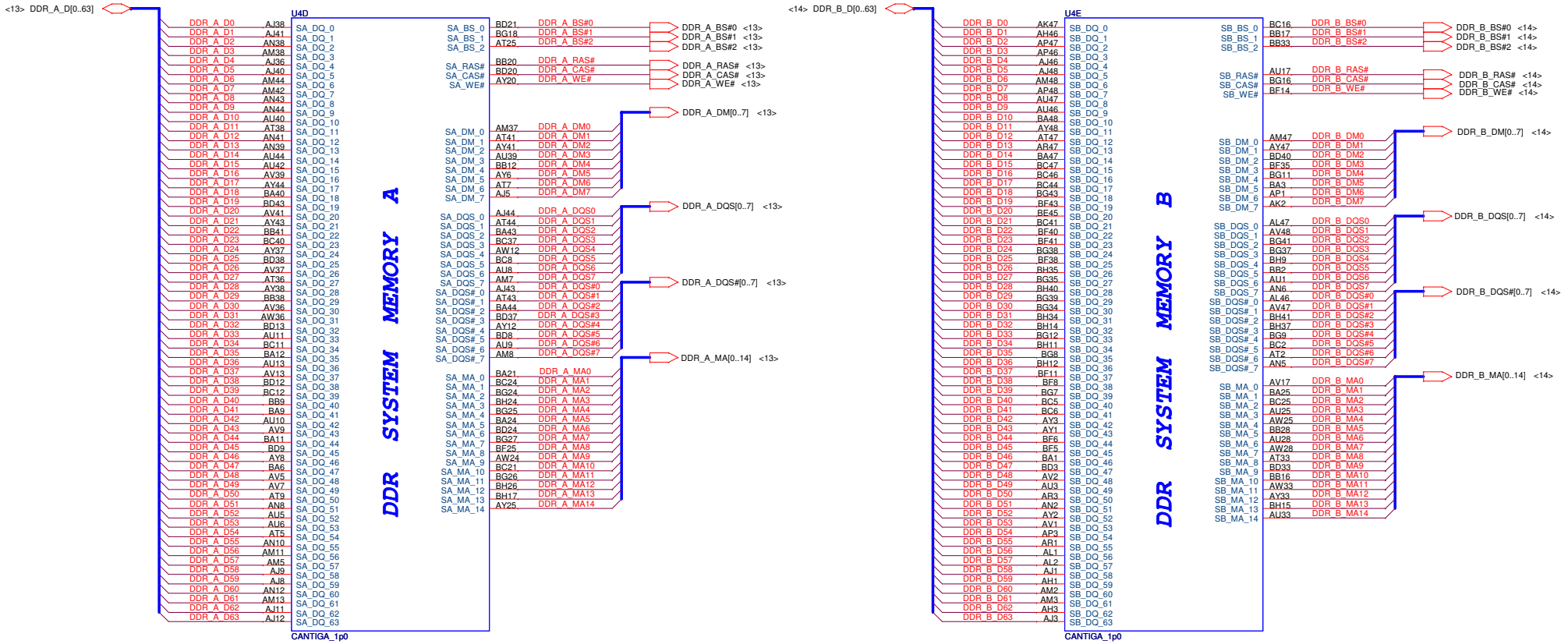
Security Classification	Compal Secret Data		
Issued Date	2008/09/24	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(1/6)-AGTL/DMI/DDR**

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 7 of 49



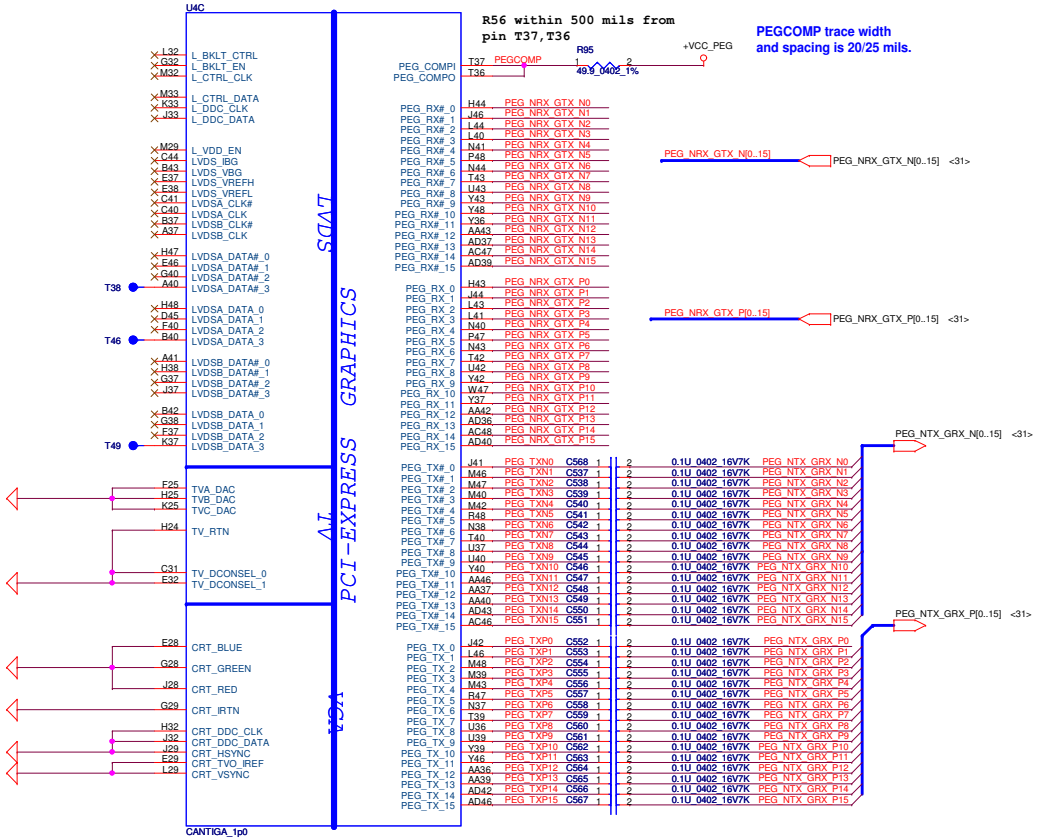
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: Cantiga(2/6)-DDR2 A/B CH

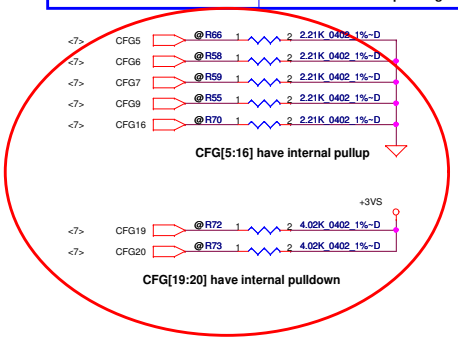
Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 8 of 49



Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable * 1 = The iTPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.



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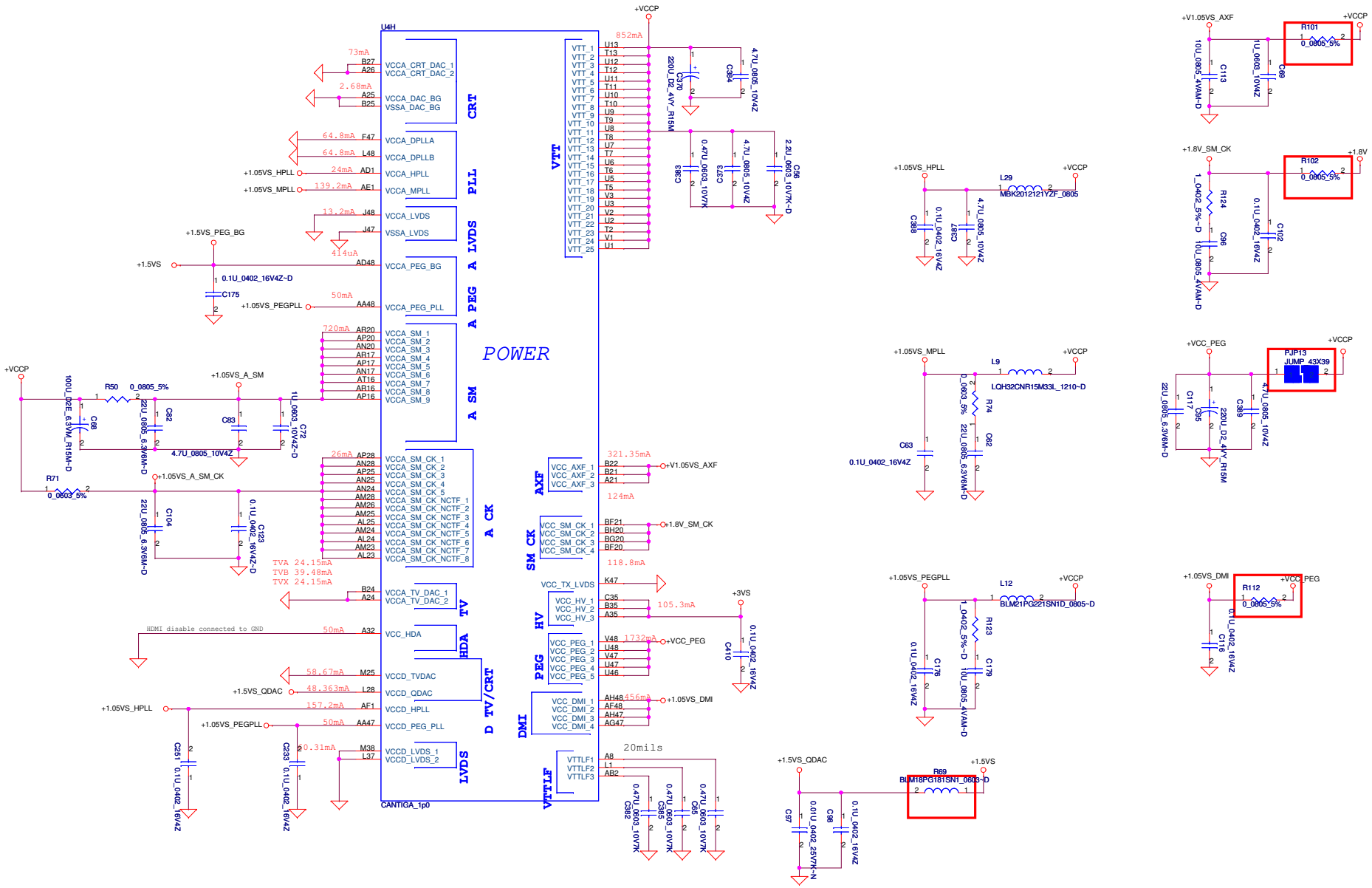
Title: *Cantiga(3/6)-VGA/LVDS/TV*

Size: Custom | Document Number: *LA-4595P* | Rev: 1.0

Date: Tuesday, February 17, 2009 | Sheet 9 of 49



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

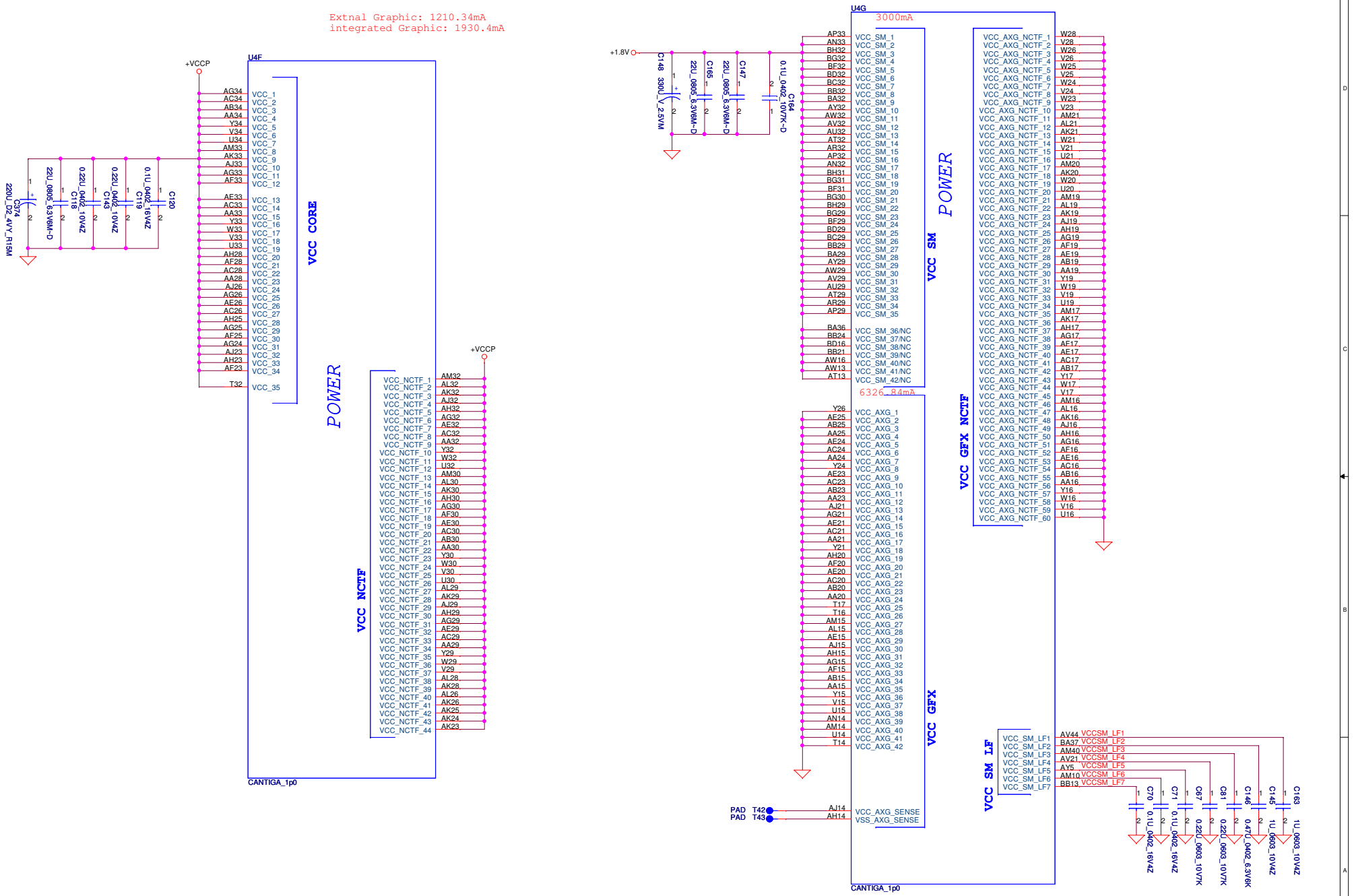
Compal Electronics, Inc.

Title: **Cantiga(4/6)-PWR**

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 10 of 49

Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



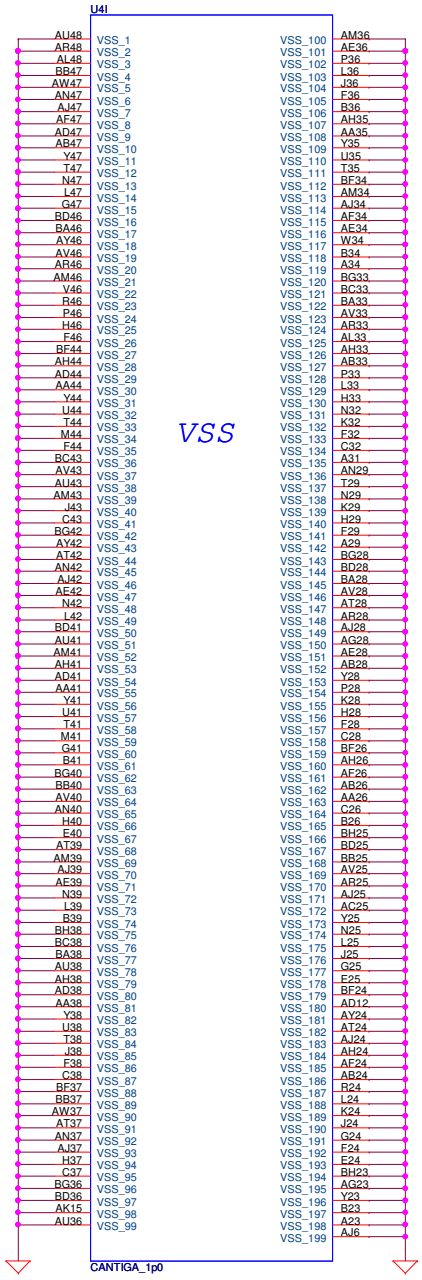
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

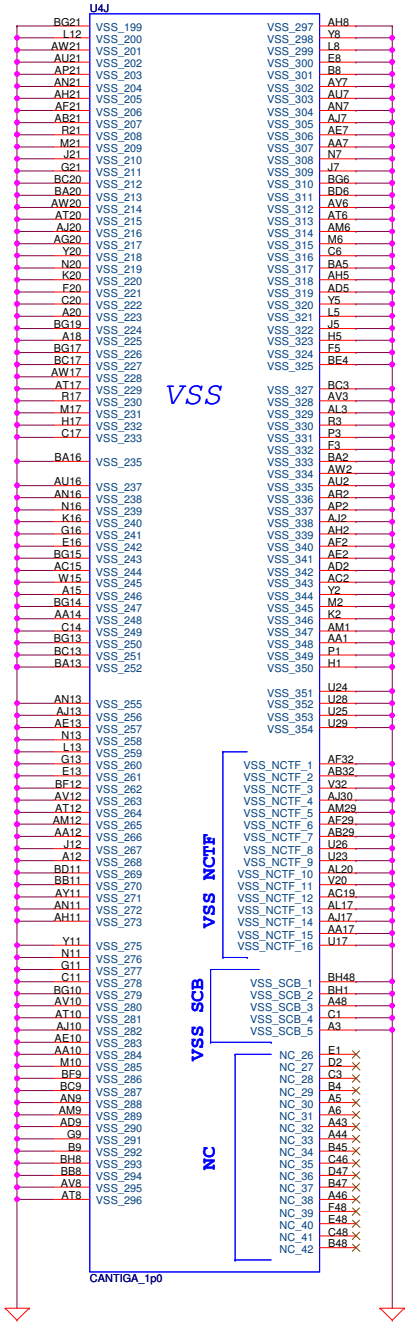
Compal Electronics, Inc.

Title: **Cantiga(5/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 | Sheet 11 of 49





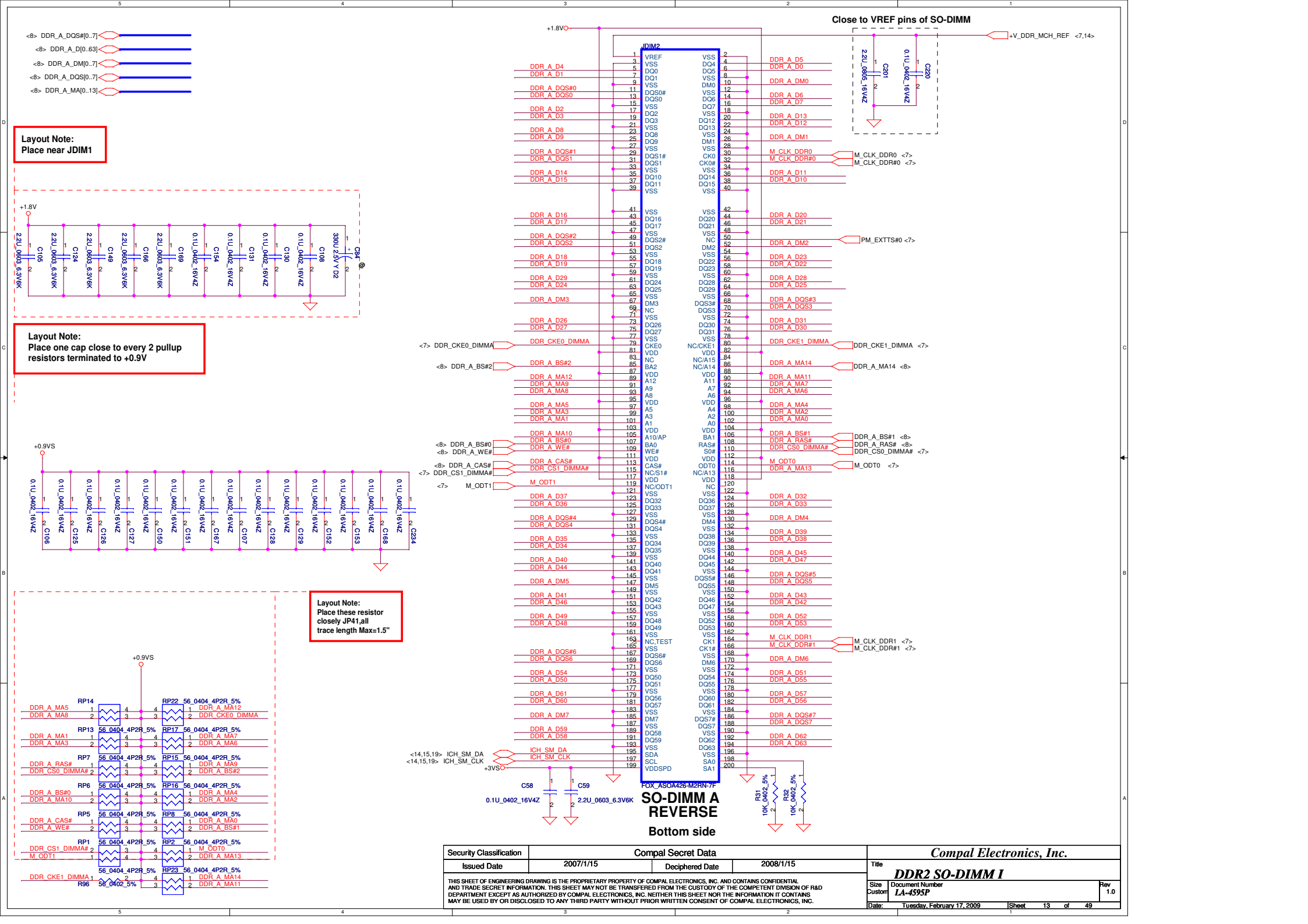
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(6/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 | Sheet 12 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: DDR2 SO-DIMM I

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 13 of 49

<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DM[0..7]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V
2.2U_0603_6.3V6K C112
2.2U_0603_6.3V6K C139
2.2U_0603_6.3V6K C160
2.2U_0603_6.3V6K C138
2.2U_0603_6.3V6K C177
0.1U_0402_16V4Z C109
0.1U_0402_16V4Z C132
0.1U_0402_16V4Z C133
0.1U_0402_16V4Z C155
330U 2.5V Y D2 C189 @

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS
0.1U_0402_16V4Z C110
0.1U_0402_16V4Z C134
0.1U_0402_16V4Z C135
0.1U_0402_16V4Z C156
0.1U_0402_16V4Z C157
0.1U_0402_16V4Z C170
0.1U_0402_16V4Z C171
0.1U_0402_16V4Z C111
0.1U_0402_16V4Z C136
0.1U_0402_16V4Z C158
0.1U_0402_16V4Z C137
0.1U_0402_16V4Z C172
0.1U_0402_16V4Z C159

Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"

+0.9VS
RP18: DDR_B_MA1, DDR_B_MA3 — RP24_56_0404_4P2R_5%: DDR_B_MA9, DDR_B_MA12
RP10: DDR_B_MA10, DDR_B_BS#0 — RP26_56_0404_4P2R_5%: DDR_B_MA14, DDR_B_MA11
RP12: DDR_B_BS#1, DDR_B_MA0 — RP19_56_0404_4P2R_5%: DDR_B_MA5, DDR_B_MA8
RP11: DDR_B_RAS#, DDR_CS2_DIMMB# — RP21_56_0404_4P2R_5%: DDR_B_MA7, DDR_B_MA6
RP9: DDR_B_CAS#, DDR_B_WE# — RP20_56_0404_4P2R_5%: DDR_B_MA4, DDR_B_MA2
RP3: DDR_CS3_DIMMB#, M_ODT3 — RP4_56_0404_4P2R_5%: DDR_B_MA13, M_ODT2
56_0404_4P2R_5% RP25: DDR_B_BS#2, DDR_CKE3_DIMMB
R335 56_0402_5% — 56_0404_4P2R_5%

+1.8V
JDIM1 FOX_AS0A426-NARN-7F~N

	VREF	1	2	VSS	
	VSS	3	4	DQ4	DDR_B_D5
DDR_B_D0	DQ0	5	6	DQ5	DDR_B_D4
DDR_B_D1	DQ1	7	8	VSS	
	VSS	9	10	DM0	DDR_B_DM0
DDR_B_DQS#0	DQS0#	11	12	VSS	
DDR_B_DQS0	DQS0	13	14	DQ6	DDR_B_D6
	VSS	15	16	DQ7	DDR_B_D7
DDR_B_D2	DQ2	17	18	VSS	
DDR_B_D3	DQ3	19	20	DQ12	DDR_B_D12
	VSS	21	22	DQ13	DDR_B_D13
DDR_B_D8	DQ8	23	24	VSS	
DDR_B_D9	DQ9	25	26	DM1	DDR_B_DM1
	VSS	27	28	VSS	
DDR_B_DQS#1	DQS1#	29	30	CK0	M_CLK_DDR2 <7>
DDR_B_DQS1	DQS1	31	32	CK0#	M_CLK_DDR#2 <7>
	VSS	33	34	VSS	
DDR_B_D10	DQ10	35	36	DQ14	DDR_B_D14
DDR_B_D11	DQ11	37	38	DQ15	DDR_B_D15
	VSS	39	40	VSS	
	VSS	41	42	VSS	
DDR_B_D17	DQ16	43	44	DQ20	DDR_B_D21
DDR_B_D20	DQ17	45	46	DQ21	DDR_B_D16
	VSS	47	48	VSS	
DDR_B_DQS#2	DQS2#	49	50	NC	
DDR_B_DQS2	DQS2	51	52	DM2	DDR_B_DM2 PM_EXTTS#1 <7>
	VSS	53	54	VSS	
DDR_B_D18	DQ18	55	56	DQ22	DDR_B_D22
DDR_B_D19	DQ19	57	58	DQ23	DDR_B_D23
	VSS	59	60	VSS	
DDR_B_D28	DQ24	61	62	DQ28	DDR_B_D29
DDR_B_D25	DQ25	63	64	DQ29	DDR_B_D24
	VSS	65	66	VSS	
DDR_B_DM3	DM3	67	68	DQS3#	DDR_B_DQS#3
	NC	69	70	DQS3	DDR_B_DQS3
	VSS	71	72	VSS	
DDR_B_D30	DQ26	73	74	DQ30	DDR_B_D26
DDR_B_D31	DQ27	75	76	DQ31	DDR_B_D27
	VSS	77	78	VSS	
<7> DDR_CKE2_DIMMB DDR_CKE2_DIMMB	CKE0	79	80	NC/CKE1	DDR_CK3_DIMMB DDR_CKE3_DIMMB <7>
	VDD	81	82	VDD	
	NC	83	84	NC/A15	
<8> DDR_B_BS#2 DDR_B_BS#2	BA2	85	86	NC/A14	DDR_B_MA14 DDR_B_MA14 <8>
	VDD	87	88	VDD	
DDR_B_MA12	A12	89	90	A11	DDR_B_MA11
DDR_B_MA9	A9	91	92	A7	DDR_B_MA7
DDR_B_MA8	A8	93	94	A6	DDR_B_MA6
	VDD	95	96	VDD	
DDR_B_MA5	A5	97	98	A4	DDR_B_MA4
DDR_B_MA3	A3	99	100	A2	DDR_B_MA2
DDR_B_MA1	A1	101	102	A0	DDR_B_MA0
	VDD	103	104	VDD	
DDR_B_MA10	A10/AP	105	106	BA1	DDR_B_BS#1 <8>
<8> DDR_B_BS#0 DDR_B_BS#0	BA0	107	108	RAS#	DDR_B_RAS# <8>
<8> DDR_B_WE# DDR_B_WE#	WE#	109	110	S0#	DDR_CS2_DIMMB# DDR_CS2_DIMMB# <7>
	VDD	111	112	VDD	
<8> DDR_B_CAS# DDR_B_CAS#	CAS#	113	114	ODT0	M_ODT2
<7> DDR_CS3_DIMMB# DDR_CS3_DIMMB#	NC/S1#	115	116	DDR_B_MA13	M_ODT2 <7>
	VDD	117	118	VDD	
<7> M_ODT3 M_ODT3	NC/ODT1	119	120	NC	
	VSS	121	122	VSS	
DDR_B_D32	DQ32	123	124	DQ36	DDR_B_D36
DDR_B_D33	DQ33	125	126	DQ37	DDR_B_D37
	VSS	127	128	VSS	
DDR_B_DQS#4	DQS4#	129	130	DM4	DDR_B_DM4
DDR_B_DQS4	DQS4	131	132	VSS	
	VSS	133	134	DQ38	DDR_B_D39
DDR_B_D34	DQ34	135	136	DQ39	DDR_B_D38
DDR_B_D35	DQ35	137	138	VSS	
	VSS	139	140	DQ44	DDR_B_D44
DDR_B_D40	DQ40	141	142	DQ45	DDR_B_D45
DDR_B_D41	DQ41	143	144	VSS	
	VSS	145	146	DQS5#	DDR_B_DQS#5
DDR_B_DM5	DM5	147	148	DQS5	DDR_B_DQS5
	VSS	149	150	VSS	
DDR_B_D42	DQ42	151	152	DQ46	DDR_B_D46
DDR_B_D43	DQ43	153	154	DQ47	DDR_B_D47
	VSS	155	156	VSS	
DDR_B_D48	DQ48	157	158	DQ52	DDR_B_D52
DDR_B_D49	DQ49	159	160	DQ53	DDR_B_D53
	VSS	161	162	VSS	
	NC,TEST	163	164	CK1	M_CLK_DDR3 <7>
	VSS	165	166	CK1#	M_CLK_DDR#3 <7>
DDR_B_DQS#6	DQS6#	167	168	VSS	
DDR_B_DQS6	DQS6	169	170	DM6	DDR_B_DM6
	VSS	171	172	VSS	
DDR_B_D51	DQ50	173	174	DQ54	DDR_B_D54
DDR_B_D50	DQ51	175	176	DQ55	DDR_B_D55
	VSS	177	178	VSS	
DDR_B_D56	DQ56	179	180	DQ60	DDR_B_D60
DDR_B_D61	DQ57	181	182	DQ61	DDR_B_D57
	VSS	183	184	VSS	
DDR_B_DM7	DM7	185	186	DQS7#	DDR_B_DQS#7
	VSS	187	188	DQS7	DDR_B_DQS7
DDR_B_D59	DQ58	189	190	VSS	
DDR_B_D58	DQ59	191	192	DQ62	DDR_B_D62
	VSS	193	194	DQ63	DDR_B_D63
<13,15,19> ICH_SM_DA ICH_SM_DA	SDA	195	196	VSS	
<13,15,19> ICH_SM_CLK ICH_SM_CLK	SCL	197	198	SA0	
+3VS	VDDSPD	199	200	SA1	R33 1 2 +3VS 10K_0402_5%

C61 0.1U_0402_16V4Z — C60 2.2U_0603_6.3V6K
R34 10K_0402_5%

SO-DIMM B
REVERSE
Bottom side

Close to VREF pins of SO-DIMM
+V_DDR_MCH_REF
+V_DDR_MCH_REF <7,13>
2.2U_0805_16V4Z C221
0.1U_0402_16V4Z C222

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.
Title: DDR2 SO-DIMM II
Size: Custom | Document Number: LA-4595P | Rev: 1.0
Date: Tuesday, February 17, 2009 | Sheet 14 of 49

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	*
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						

Routing the trace at least 10mil

0905 Connect to +VCCP

Place close to U55

NB CPU

CardBus OZ888

Express Card

SB, MINI PCI

CPU_STP

MiniCard_WWAN

ICH_SATA

GLAN

MiniCard_WLAN

ICH

NB_3GPLL

VGA (Discrete)

VGA_27M (DIS)

S IC ICS9LPRS387AKLFT MLF 72P CLK GEN

ITP_EN	*0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) *1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed *1 = Overclocking of CPU and SRC NOT allowed

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

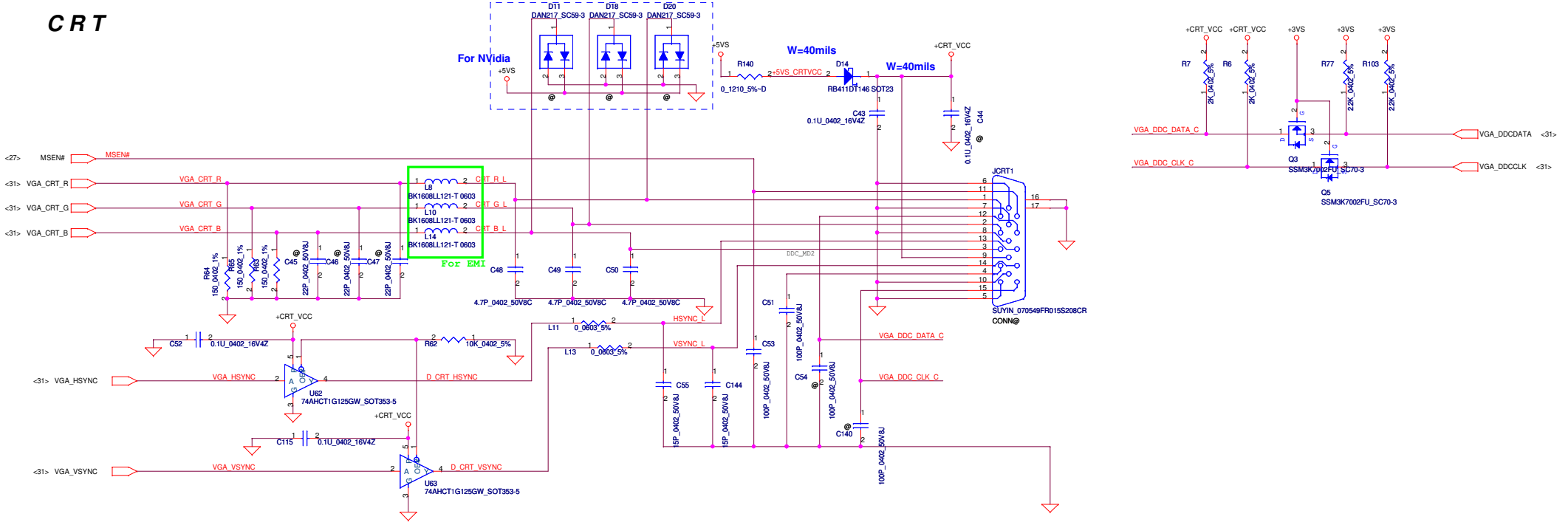
Compal Electronics, Inc.

Title: Clock Generator CK505

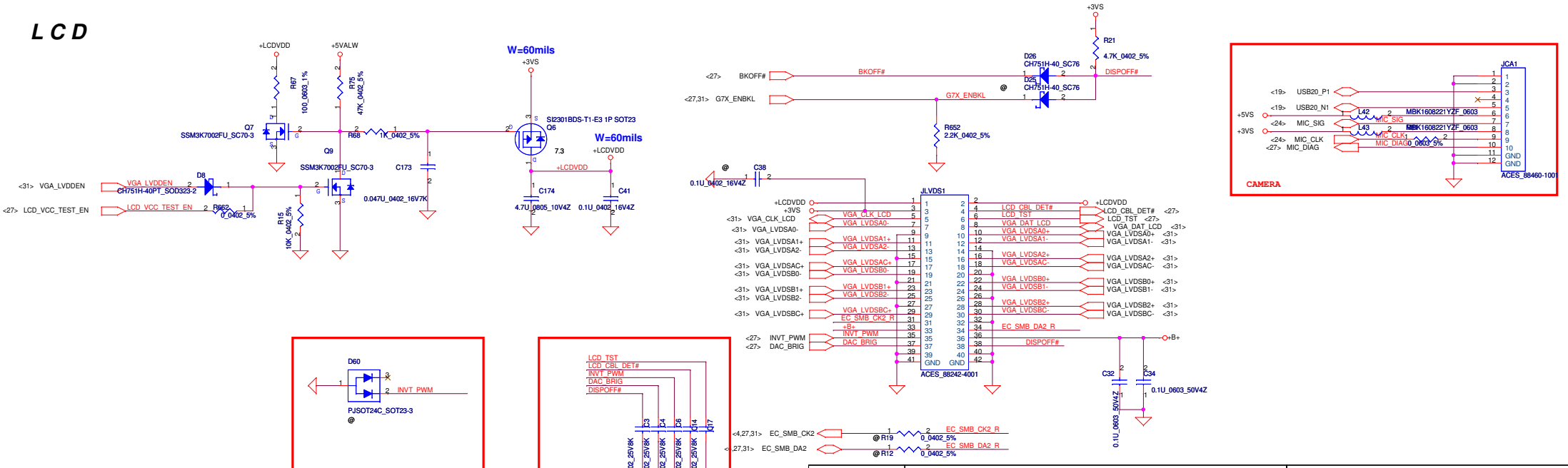
Size	Document Number	Rev
	LA-4595P	1.0

Date: Tuesday, February 17, 2009 | Sheet 15 of 49

CRT



LCD



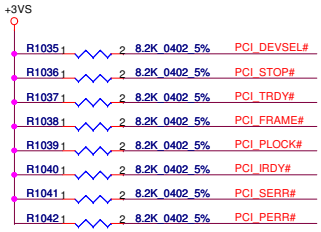
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

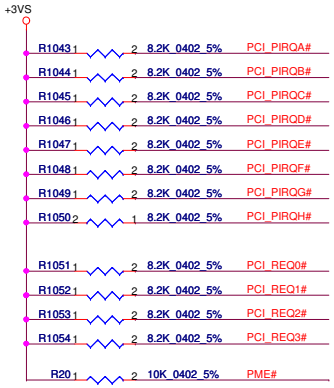
Compal Electronics, Inc.

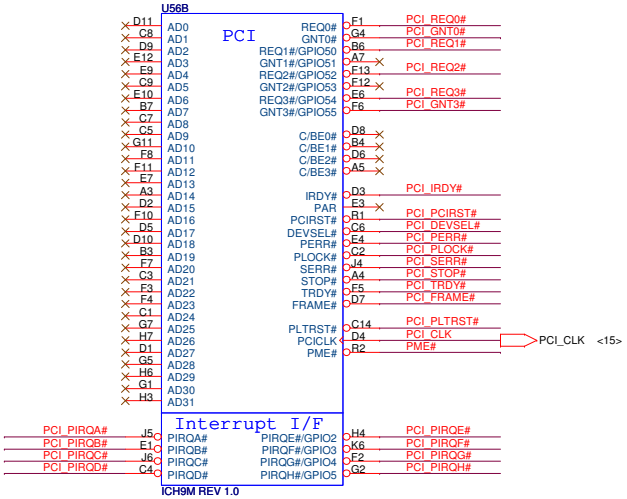
Title: CRT CONN/LCD CONN

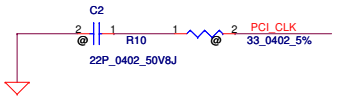
Size	Document Number	Rev
Custom	LA-4595P	1.0

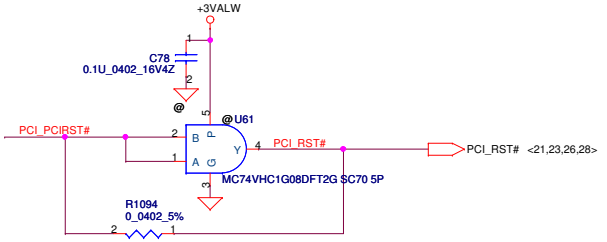
Date: Tuesday, February 17, 2009 | Sheet 16 of 49

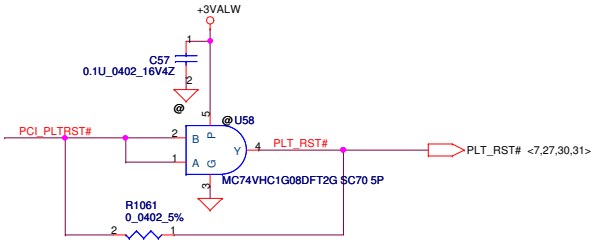




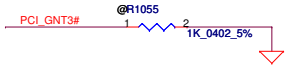




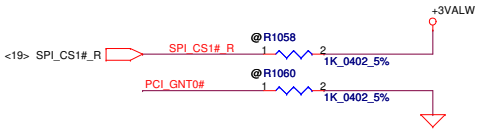




A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

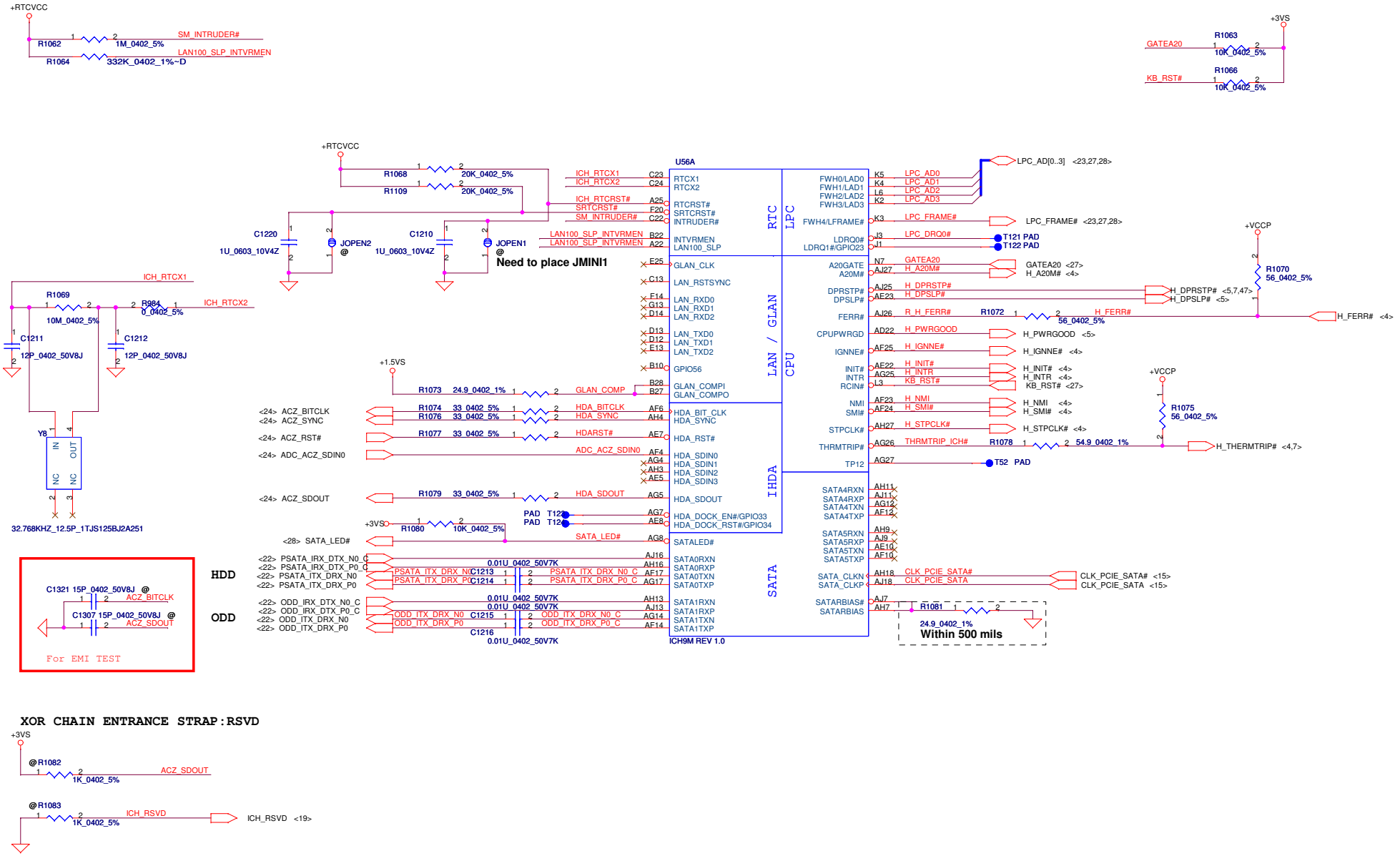


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



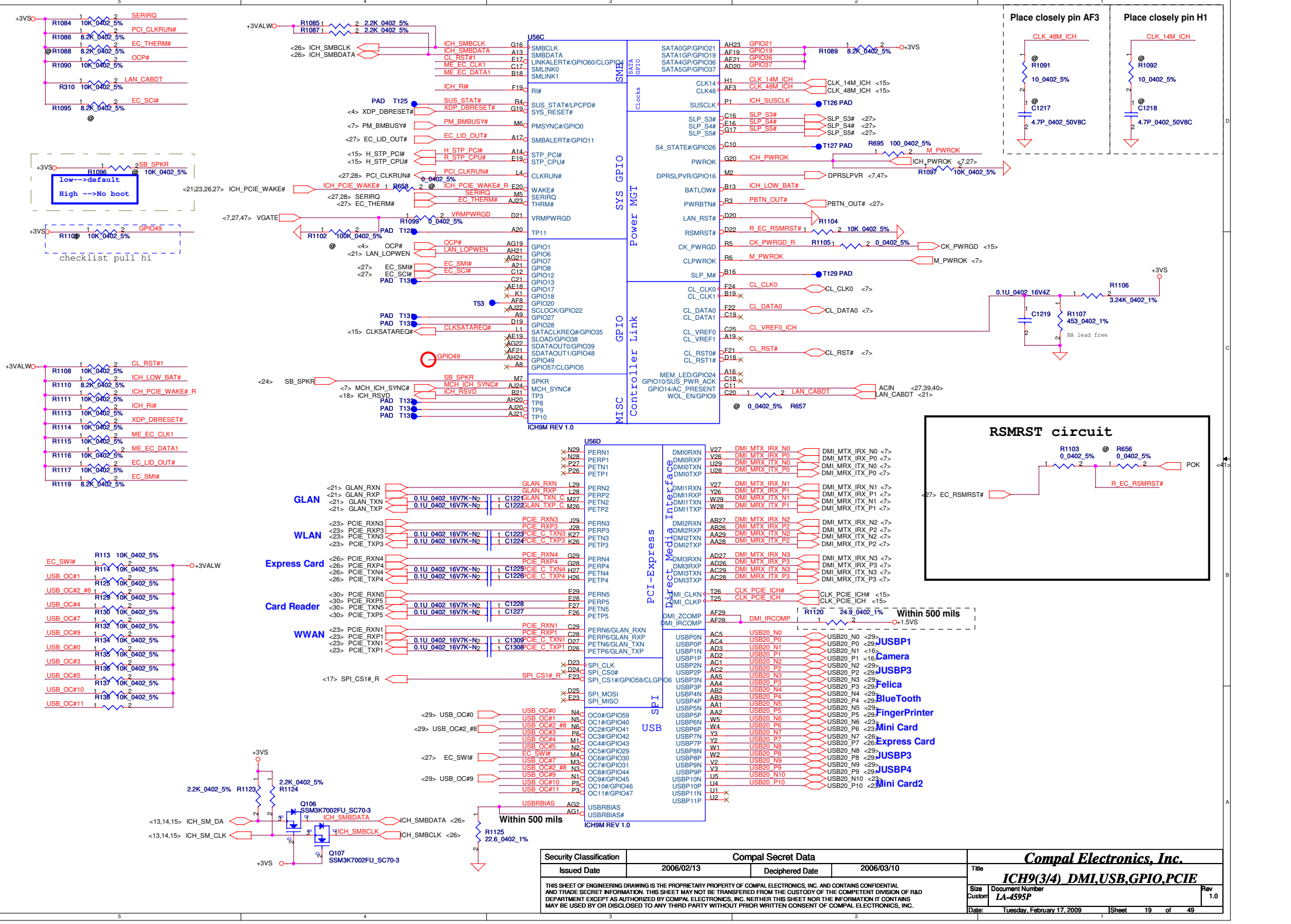
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: ICH9(1/4)-PCI/INT			
Size	Document Number: LA-4595P		Rev: 1.0
Date: Tuesday, February 17, 2009		Sheet 17 of 49	



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title	ICH9(2/4)_LAN,HD,IDE,LPC		
Size: Custom	Document Number: LA-4595P		Rev: 1.0
Date: Tuesday, February 17, 2009	Sheet 18 of 49		


Place closely pin AF3
Place closely pin H1
CLK_48M_ICH
CLK_14M_ICH
R1091 10_0402_5%
R1092 10_0402_5%
C1217 4.7P_0402_50V8C
C1218 4.7P_0402_50V8C
U56C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
SMB
SATA GPIO
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
GPIO21
GPIO19
GPIO36
GPIO37
R1089 8.2K_0402_5%
Clocks
CLK14
CLK48
SUSCLK
CLK_14M_ICH
CLK_48M_ICH
ICH_SUSCLK
T126 PAD
SYS GPIO
Power MGT
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
T127 PAD
R695 100_0402_5%
M_PWROK
PWROK
ICH_PWROK
R1097 10K_0402_5%
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
PBTN_OUT#
LAN_RST#
R1104
RSMRST#
R_EC_RSMRST#
10K_0402_5%
CK_PWRGD
CK_PWRGD_R
R1105 0_0402_5%
CLPWROK
SLP_M#
T129 PAD
GPIO Controller Link
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
CL_VREF_ICH
CL_RST#
MEM_LED/GPIO24
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
WOL_EN/GPIO9
ACIN
LAN_CABDT
R657
MISC
SPKR
MCH_SYNC#
TP3
TP8
TP9
TP10
ICH9M REV 1.0
R1085 2.2K_0402_5%
R1087 2.2K_0402_5%
ICH_SMBCLK
ICH_SMBDATA
CL_RST#1
ME_EC_CLK1
ME_EC_DATA1
ICH_RI#
SUS_STAT#
XDP_DBRESET#
PM_BMBUSY#
EC_LID_OUT#
H_STP_PCI#
H_STP_CPU#
PCI_CLKRUN#
ICH_PCIE_WAKE#
SERIRQ
EC_THERM#
VRMPWRGD
VGATE
OCP#
LAN_LOPWEN
EC_SMI#
EC_SCI#
GPIO49
CLKSATAREQ#
SB_SPKR
MCH_ICH_SYNC#
ICH_RSVD
R1102 100K_0402_5%
R1099 0_0402_5%
R658 0_0402_5%
R1106 3.24K_0402_1%
0.1U_0402_16V4Z
C1219
R1107 453_0402_1%
NA lead free
RSMRST circuit
R1103 0_0402_5%
R656 0_0402_5%
POK
R_EC_RSMRST#
EC_RSMRST#
U56D
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
PCI-Express
Direct Media Interface
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
R1120 24.9_0402_1%
Within 500 mils
+1.5VS
GLAN
WLAN
Express Card
Card Reader
WWAN
0.1U_0402_16V7K-N2
C1221
C1222
C1223
C1224
C1225
C1226
C1228
C1227
C1309
C1308
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO
SPI_CS1#_R
SPI
USB
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBRBIAS
USBRBIAS#
R1125 22.6_0402_1%
Within 500 mils
Q106 SSM3K7002FU_SC70-3
Q107 SSM3K7002FU_SC70-3
R1123 2.2K_0402_5%
R1124 2.2K_0402_5%
ICH_SM_DA
ICH_SM_CLK
ICH_SMBDATA
ICH_SMBCLK
USB20_N0
USB20_P0
USB20_N1
USB20_P1
USB20_N2
USB20_P2
USB20_N3
USB20_P3
USB20_N4
USB20_P4
USB20_N5
USB20_P5
USB20_N6
USB20_P6
USB20_N7
USB20_P7
USB20_N8
USB20_P8
USB20_N9
USB20_P9
USB20_N10
USB20_P10
JUSBP1
Camera
JUSBP3
Felica
BlueTooth
FingerPrinter
Mini Card
Express Card
JUSBP3
JUSBP4
Mini Card2
R1088 8.2K_0402_5%
R1090 10K_0402_5%
R310 10K_0402_5%
R1095 8.2K_0402_5%
R1096 10K_0402_5%
low-->default
High -->No boot
R1100 10K_0402_5%
checklist pull hi
R1108 10K_0402_5%
R1110 8.2K_0402_5%
R1111 10K_0402_5%
R1113 10K_0402_5%
R1114 10K_0402_5%
R1115 10K_0402_5%
R1116 10K_0402_5%
R1117 10K_0402_5%
R1119 8.2K_0402_5%
R113 10K_0402_5%
R114 10K_0402_5%
R125 10K_0402_5%
R129 10K_0402_5%
R130 10K_0402_5%
R132 10K_0402_5%
R134 10K_0402_5%
R135 10K_0402_5%
R136 10K_0402_5%
R137 10K_0402_5%
R138 10K_0402_5%
EC_SW1#
USB_OC#1
USB_OC#2_#8
USB_OC#4
USB_OC#7
USB_OC#9
USB_OC#0
USB_OC#3
USB_OC#5
USB_OC#10
USB_OC#11
Security Classification
Compal Secret Data
Issued Date
2006/02/13
Deciphered Date
2006/03/10
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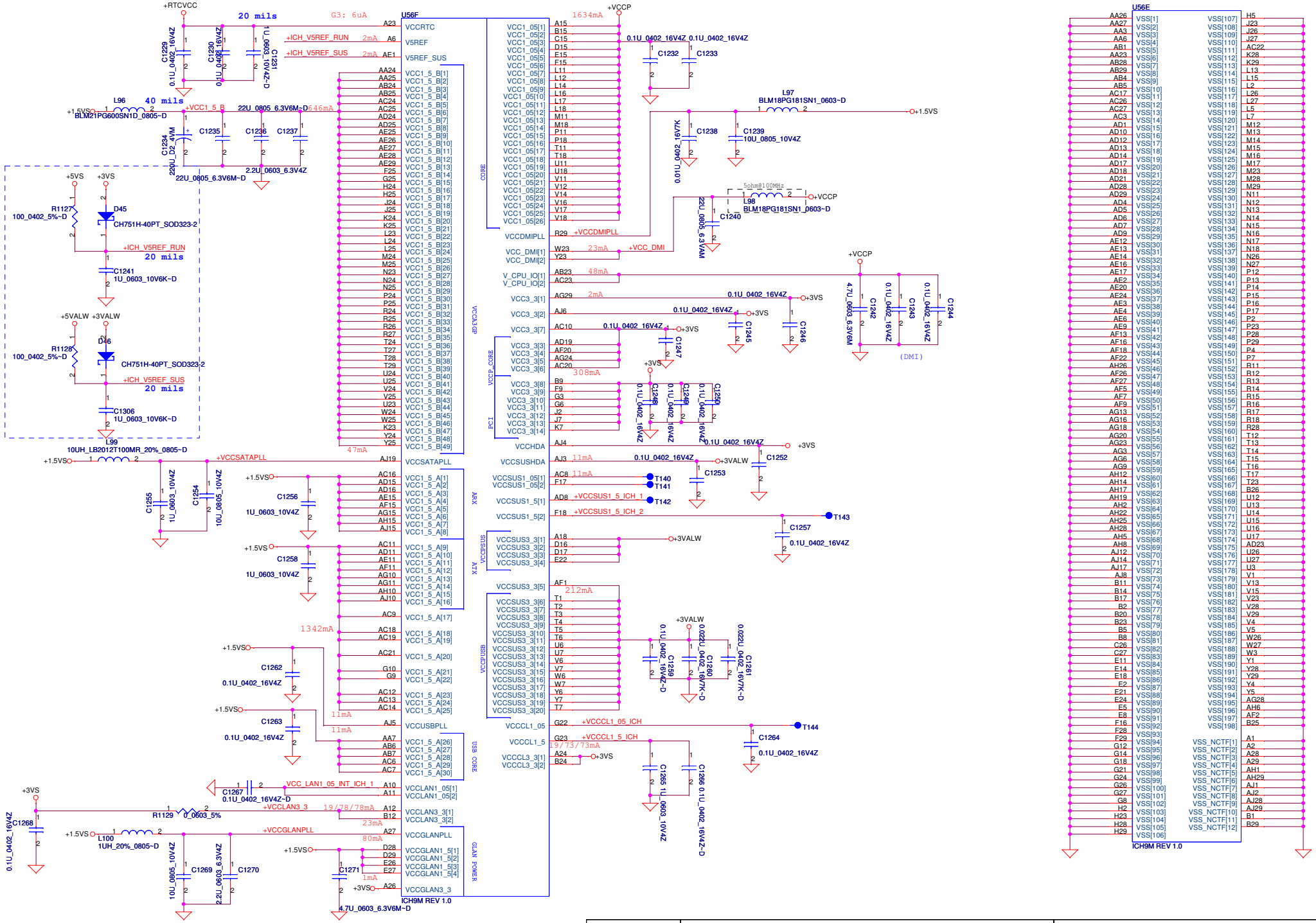
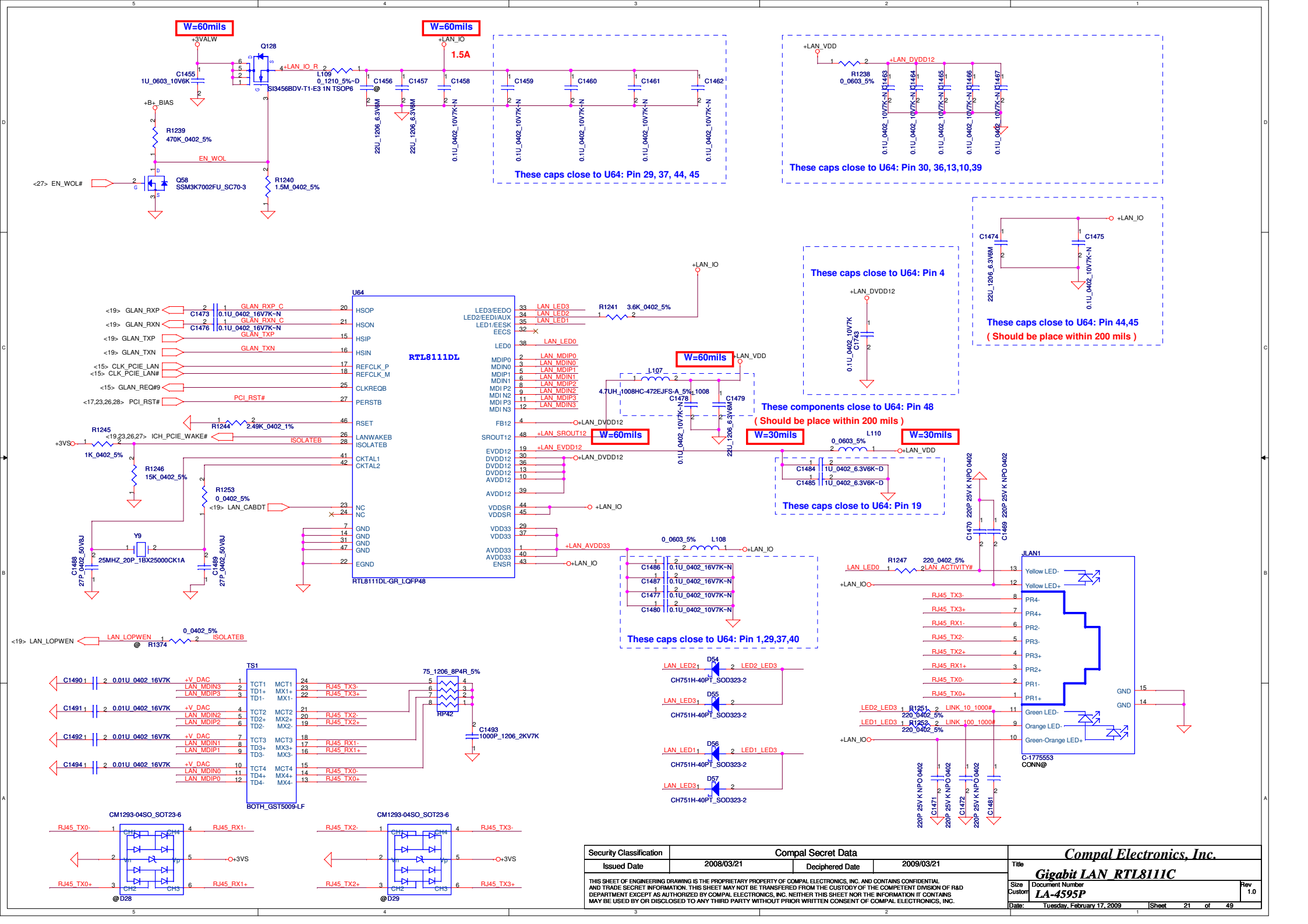
Compal Electronics, Inc.
Title
ICH9(3/4)_DMI,USB,GPIO,PCIE
Size Custom
Document Number
LA-4595P
Rev 1.0
Date: Tuesday, February 17, 2009
Sheet 19 of 49



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Title	Compal Electronics, Inc.		
	ICH9(4/4)_POWER&GND		
Size: Custom	Document Number: LA-4595P		Rev: 1.0
Date: Tuesday, February 17, 2009	Sheet 20 of 49		



Security Classification	Compal Secret Data		
Issued Date	2008/03/21	Deciphered Date	2009/03/21

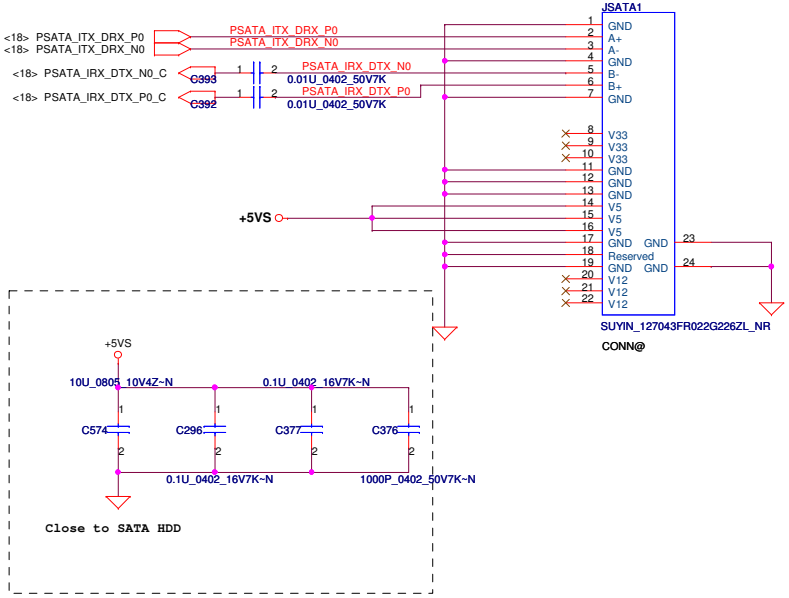
Compal Electronics, Inc.

Title: Gigabit LAN RTL8111C

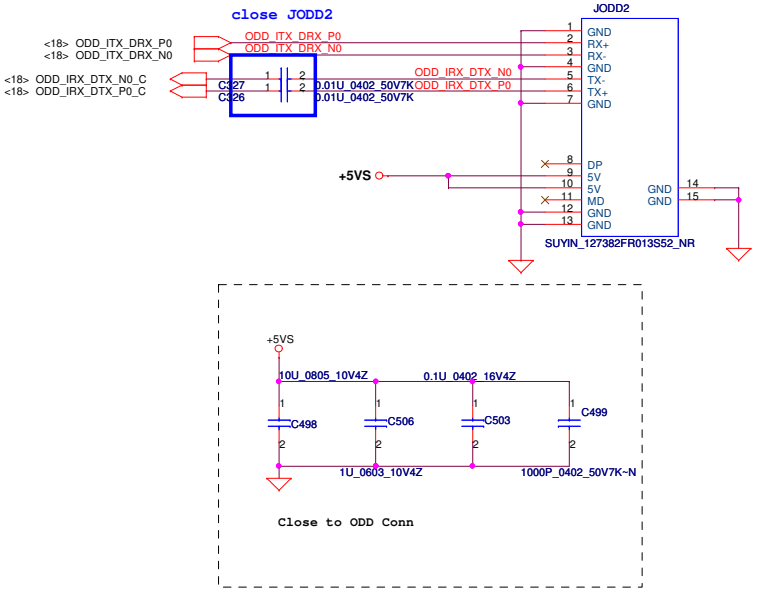
Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 21 of 49

SATA HDD CONN



SATA ODD CONN



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

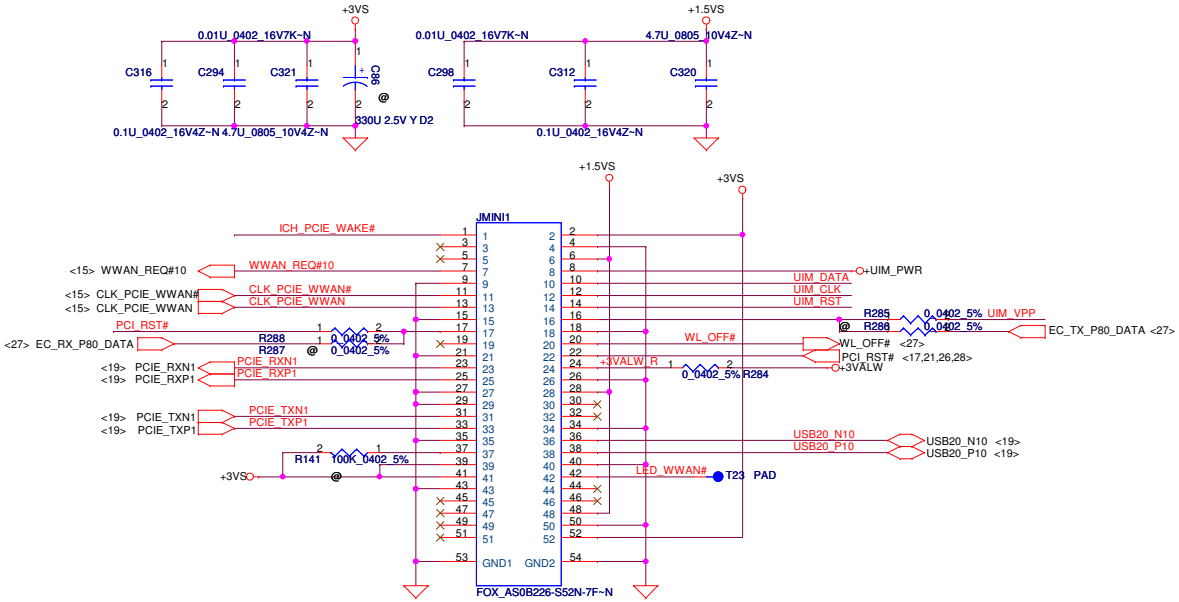
Compal Electronics, Inc.

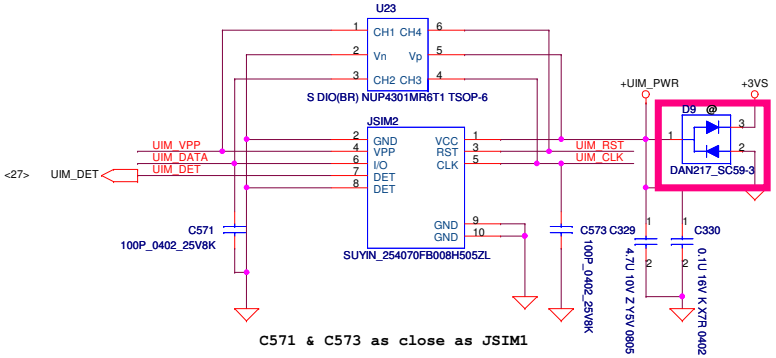
Title: HDD/CDROM

Size	Document Number	Rev
Custom	LA-4595P	1.0

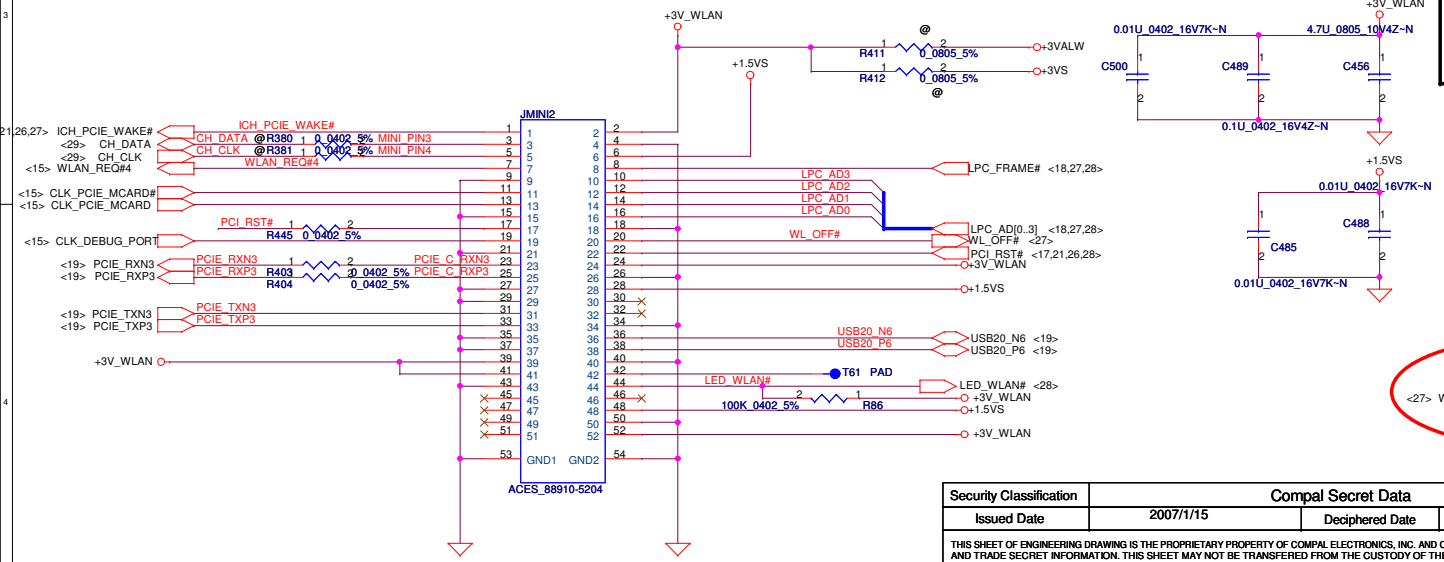
Date: Tuesday, February 17, 2009 Sheet 22 of 49

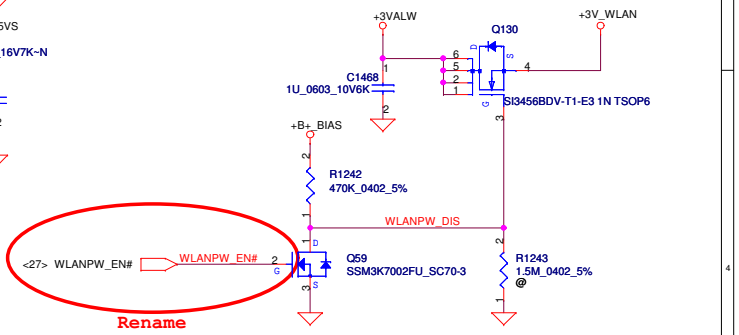
WWAN

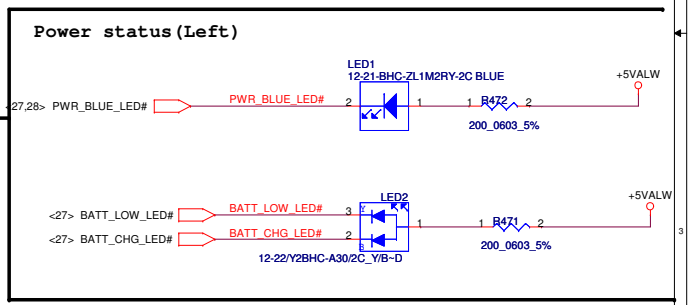




Mini-Express Card---WLAN







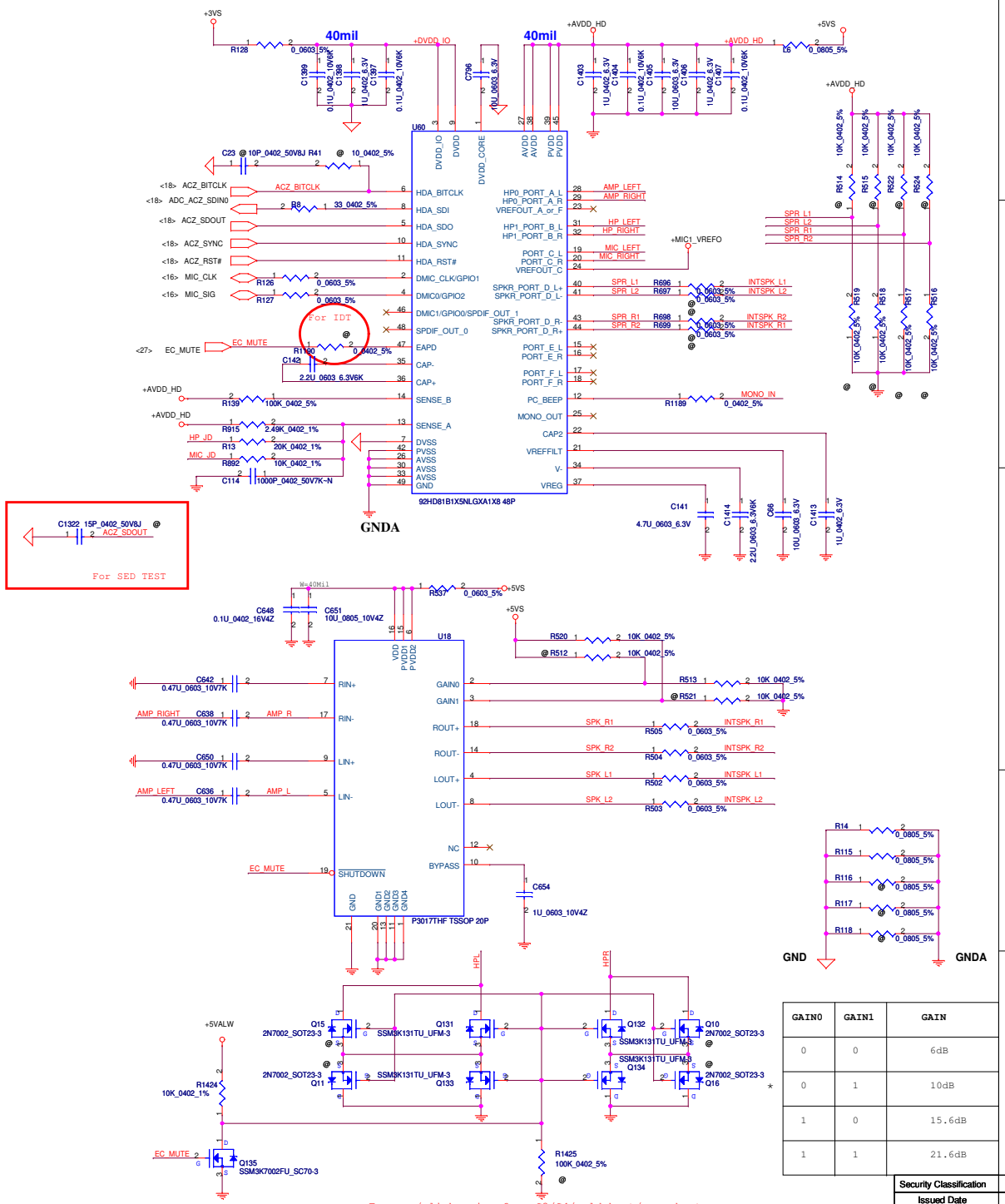
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

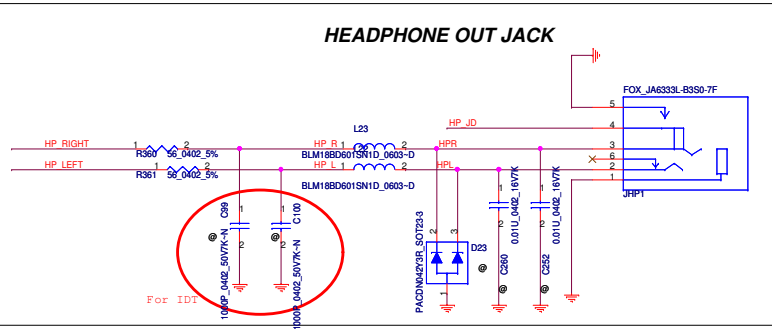
Title: Mini-Card/LED

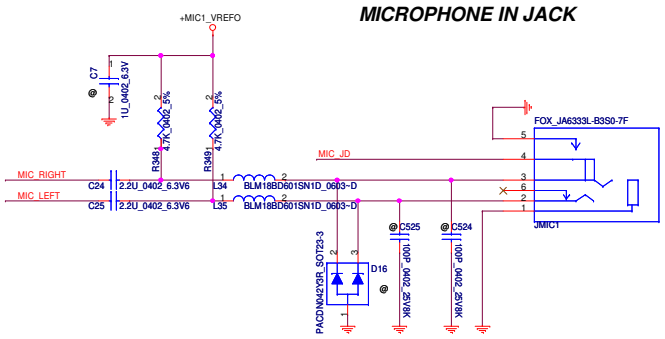
Size	Document Number	Rev
Custom	LA-4595P	1.0

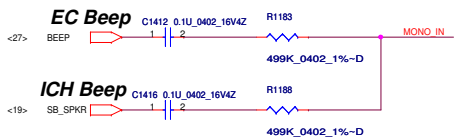
Date: Tuesday, February 17, 2009 Sheet 23 of 49

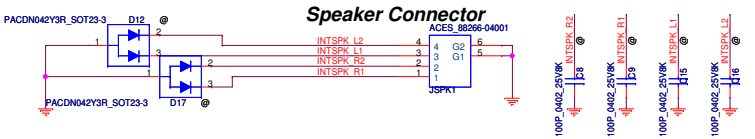


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





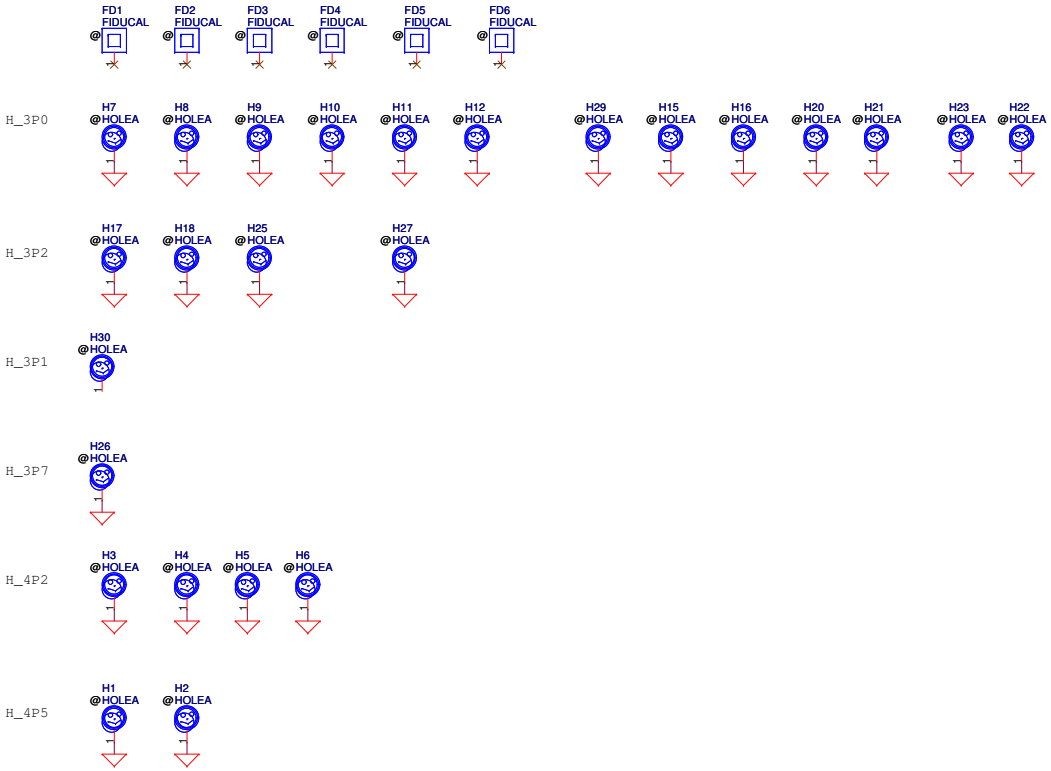




Compal Electronics, Inc.

Security Classification	Compal Secret Data		
Issued Date	2008/05/07	Deciphered Date	2009/05/07

Title	HD CODEC 92HD81		
Size	Document Number		Rev
	LA-4595P		1.0
Date:	Tuesday, February 17, 2009	Sheet	24 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

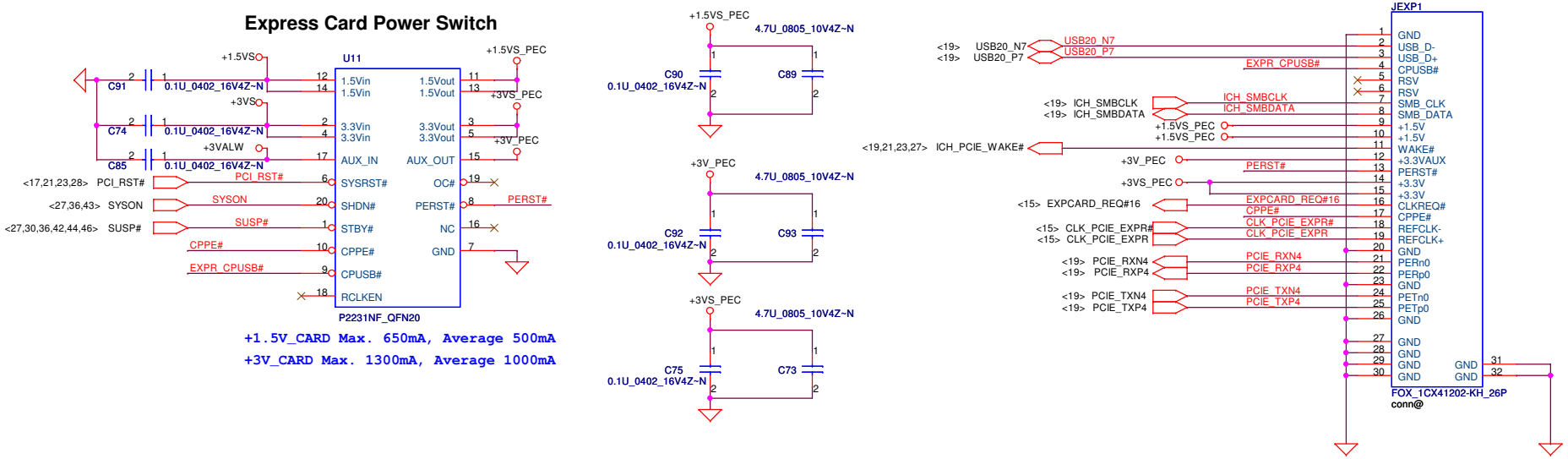
Compal Electronics, Inc.

Title: ***Screws***

Size	Document Number	Rev
Custom	*LA-4595P*	1.0

Date: Tuesday, February 17, 2009 Sheet 25 of 49

Express card

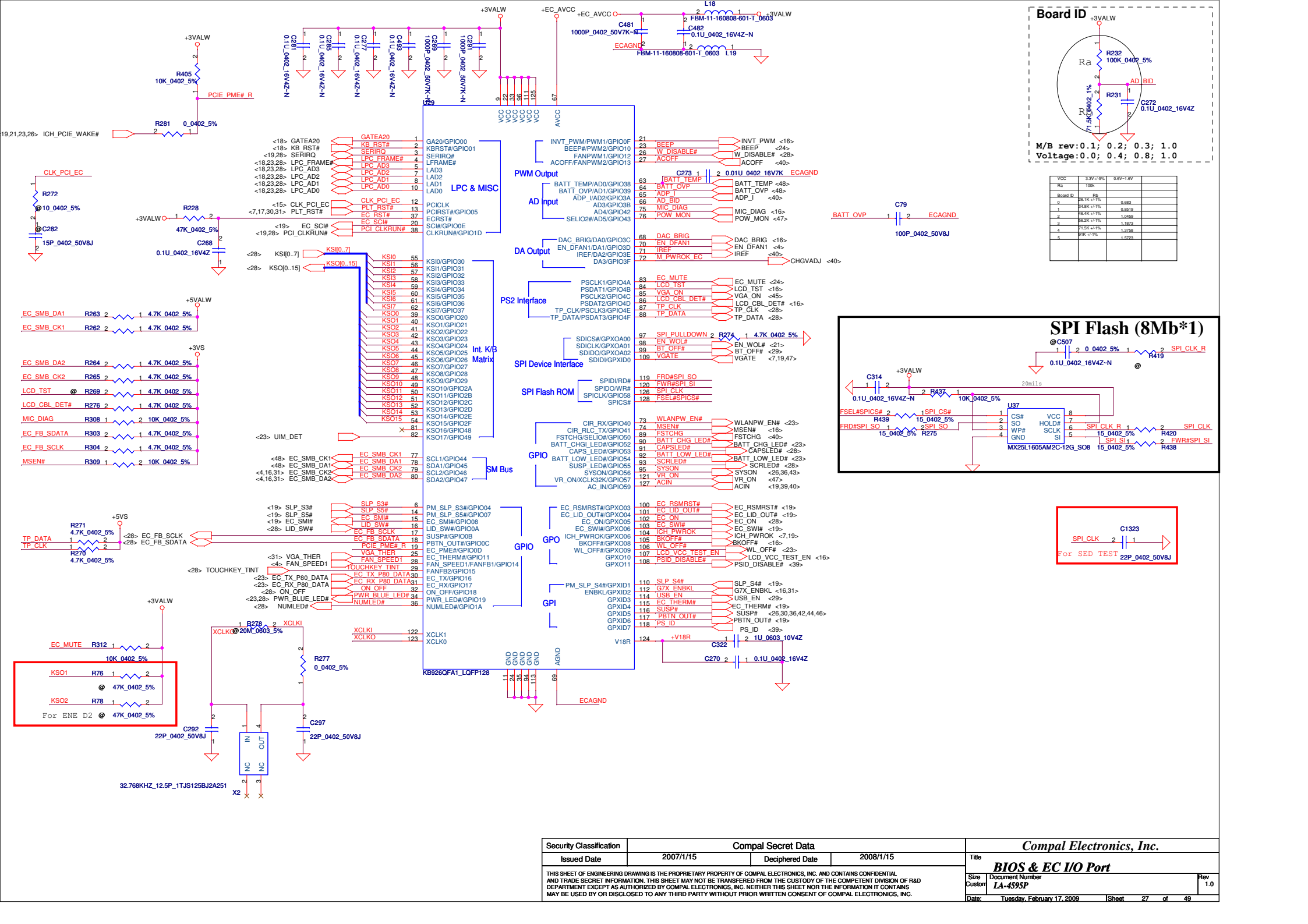


Compal Electronics, Inc.

Title: EXPRESS CARD

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 26 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

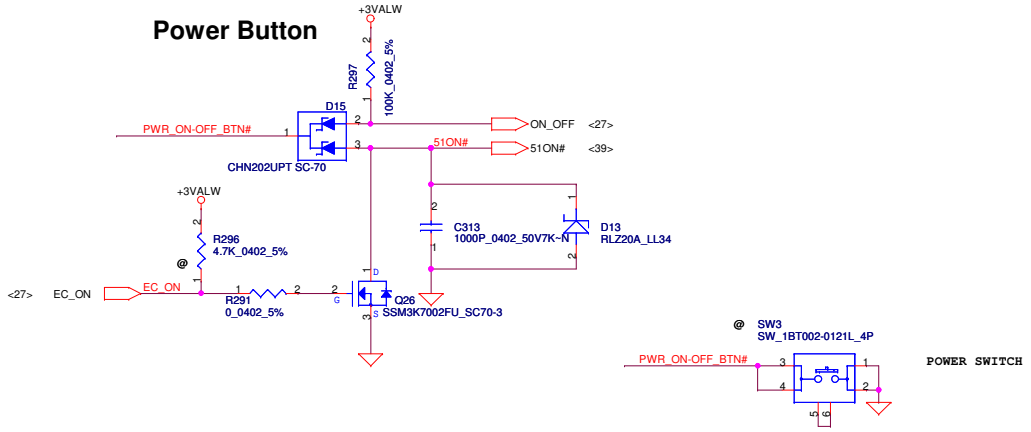
Compal Electronics, Inc.

Title: BIOS & EC I/O Port

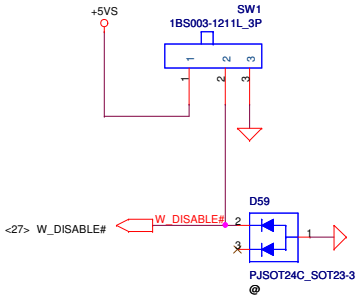
Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 27 of 49

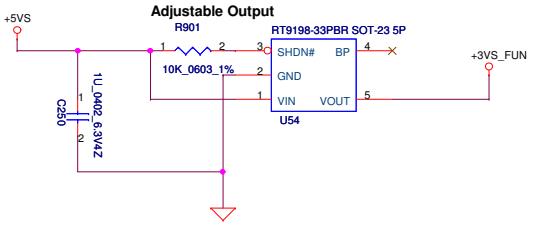
Power Button



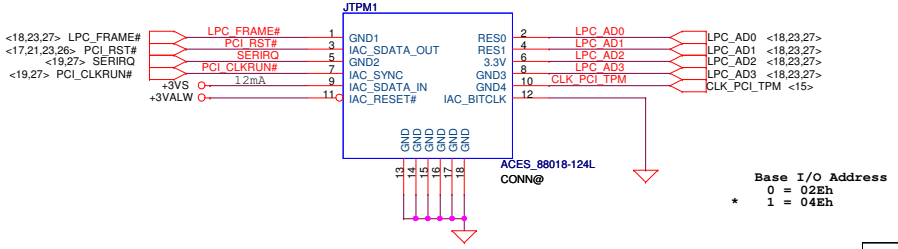
Wireless_BTN



Regulator for ENE sensor

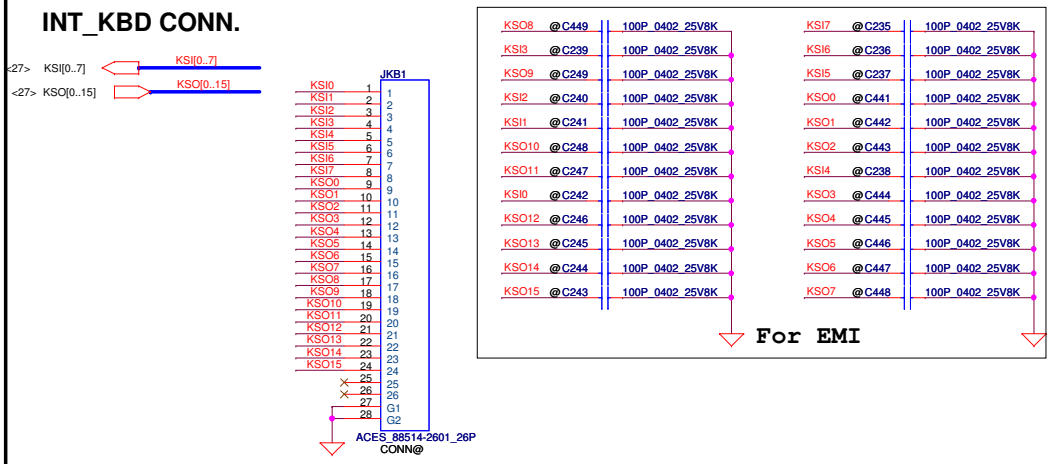


TPM 1.2

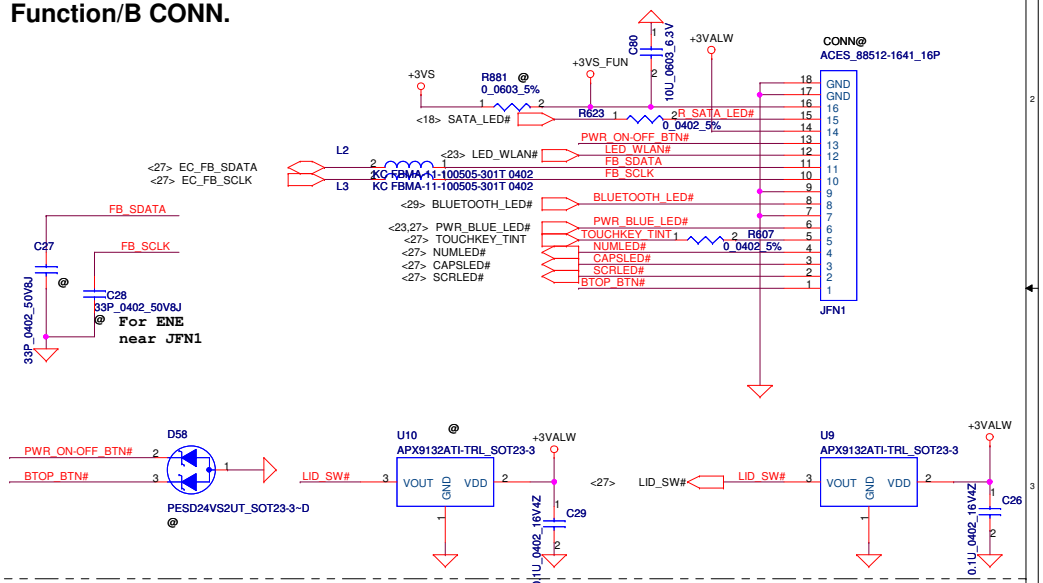


Base I/O Address
0 = 02Eh
* 1 = 04Eh

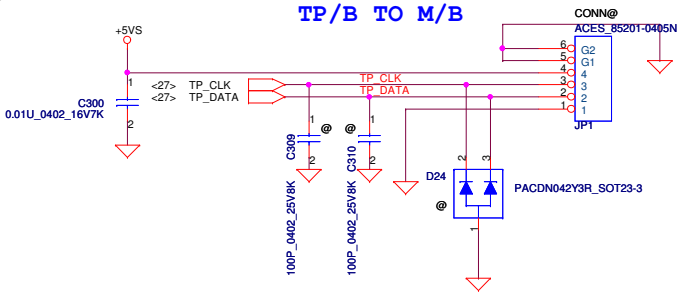
INT_KBD CONN.



Function/B CONN.



Touch PAD/B CONN.



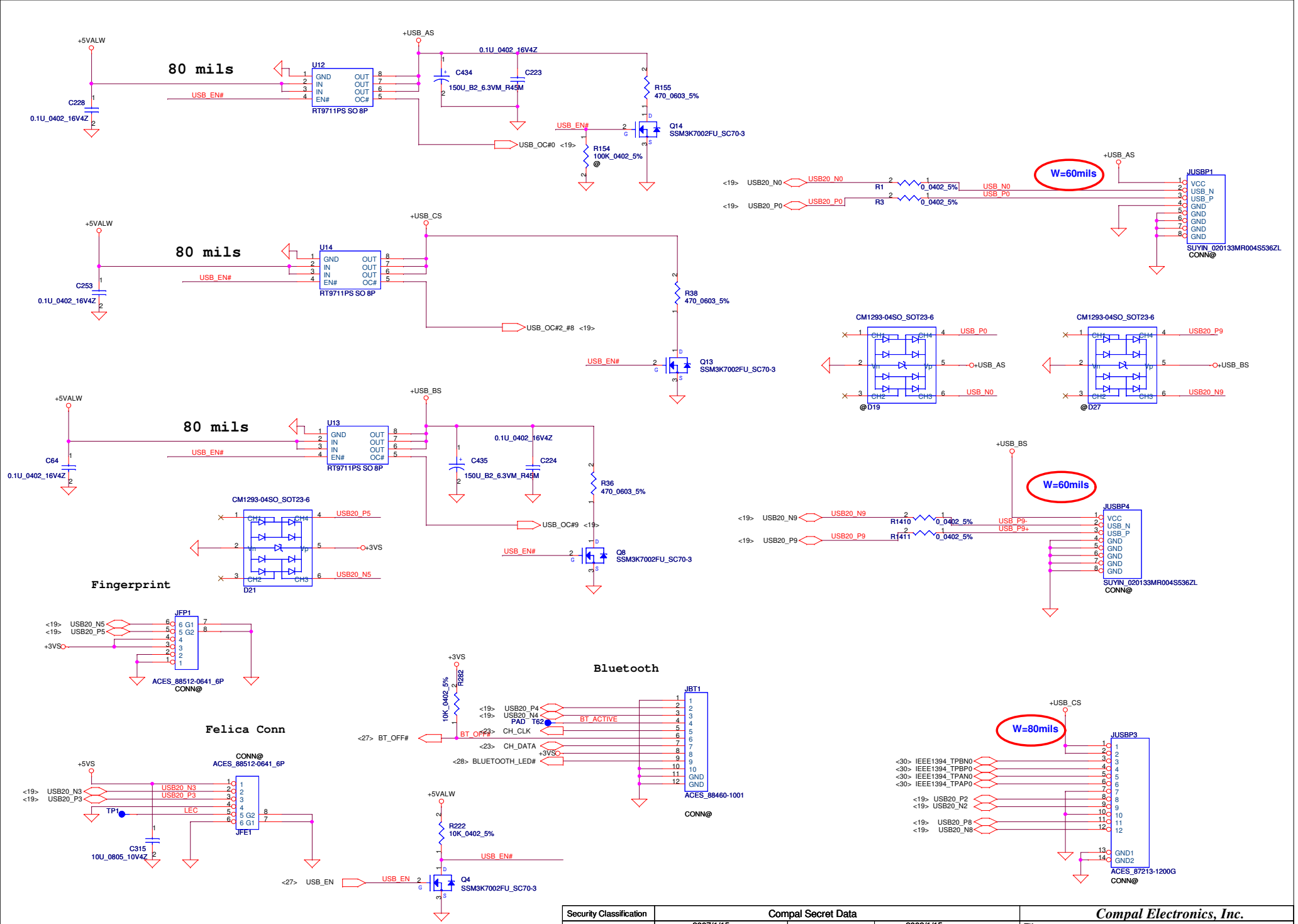
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: *PWR_OK/BTN/TP*

Size	Document Number	Rev
Custom	*LA-4595P*	1.0

Date: Tuesday, February 17, 2009 Sheet 28 of 49



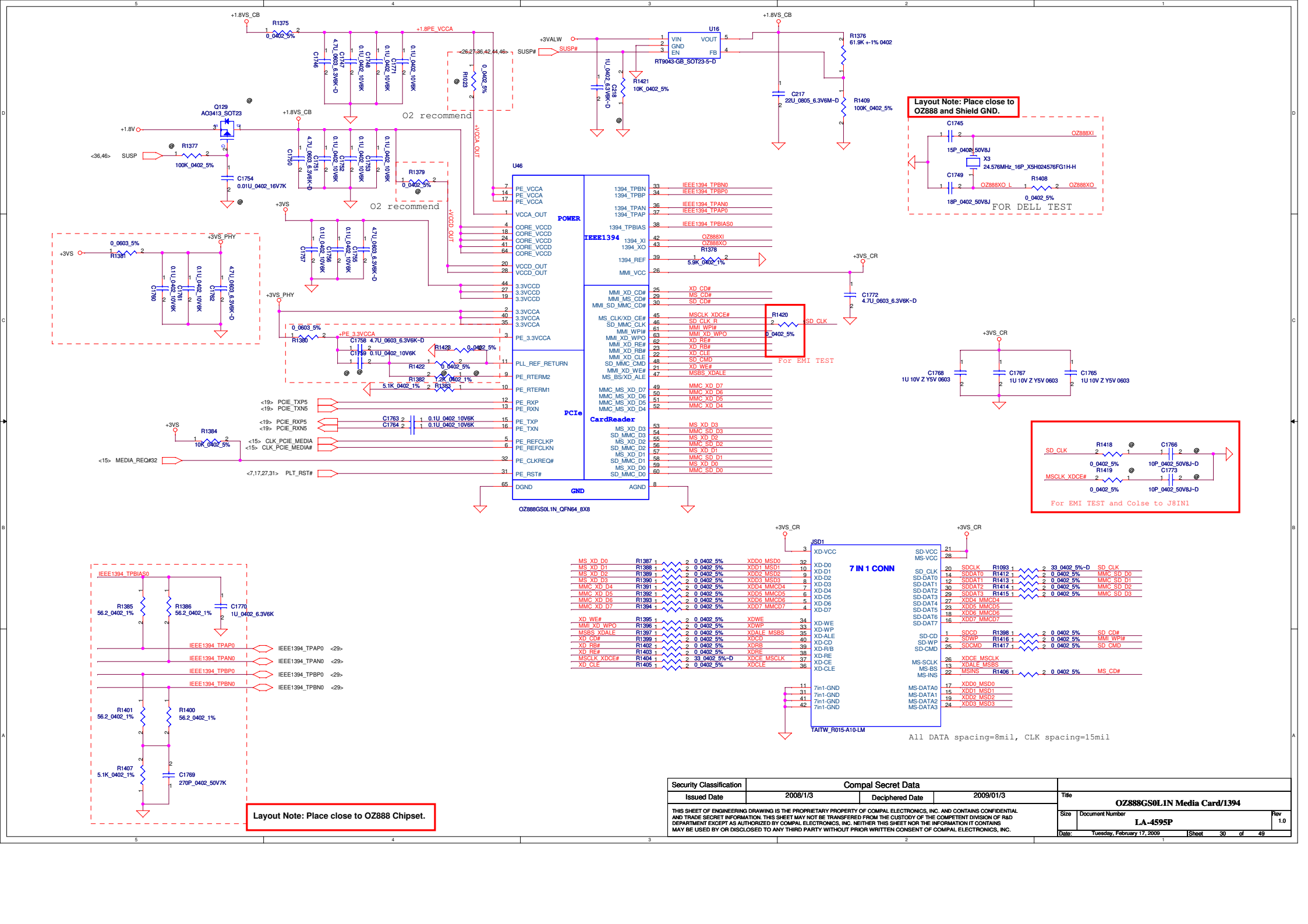
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: USB/BlueTooth/FP/Felcia

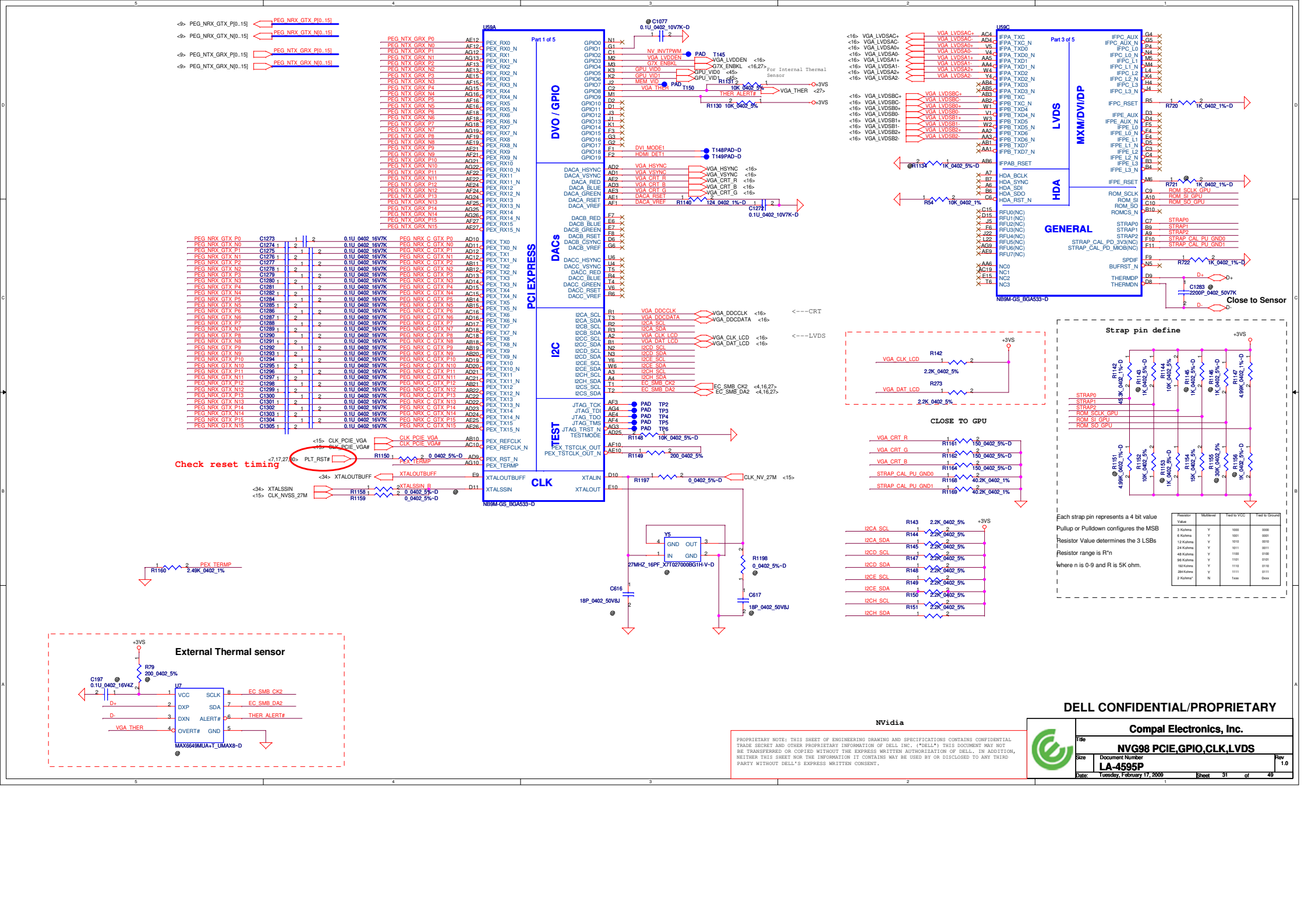
Size	Document Number	Rev
Custom	LA-4595P	1.0

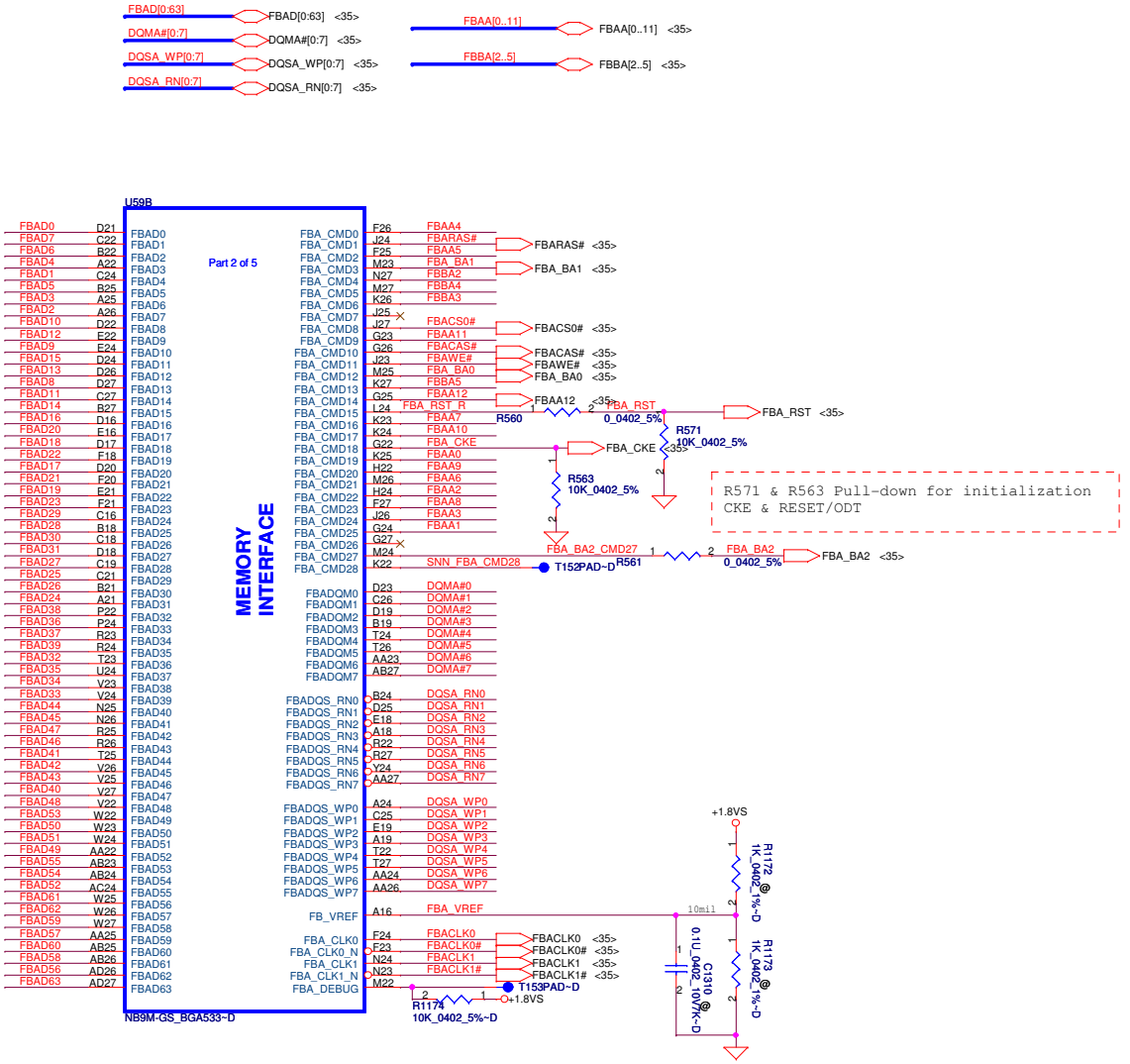
Date: Tuesday, February 17, 2009 Sheet 29 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/1/3	Deciphered Date	2009/01/3

Title	OZ888GS0L1N Media Card/1394		
Size	Document Number		Rev
	LA-4595P		1.0
Date:	Tuesday, February 17, 2009	Sheet	30 of 49


PEG_NRX_GTX_P[0..15]
PEG_NRX_GTX_N[0..15]
PEG_NTX_GRX_P[0..15]
PEG_NTX_GRX_N[0..15]
U59A
Part 1 of 5
PCI EXPRESS
DVO / GPIO
DACs
I2C
TEST
CLK
NB9M-GS_BGA533-D
U59C
Part 3 of 5
LVDS
MXM/DVI/DP
HDA
GENERAL
NB9M-GS_BGA533-D
Close to Sensor
Check reset timing
CLOSE TO GPU
Strap pin define
Each strap pin represents a 4 bit value
Pullup or Pulldown configures the MSB
Resistor Value determines the 3 LSBs
Resistor range is R*n
where n is 0-9 and R is 5K ohm.
External Thermal sensor
MAX6649MUA+T_UMAX8-D
NVidia
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
NVG98 PCIE,GPIO,CLK,LVDS
LA-4595P
Tuesday, February 17, 2009



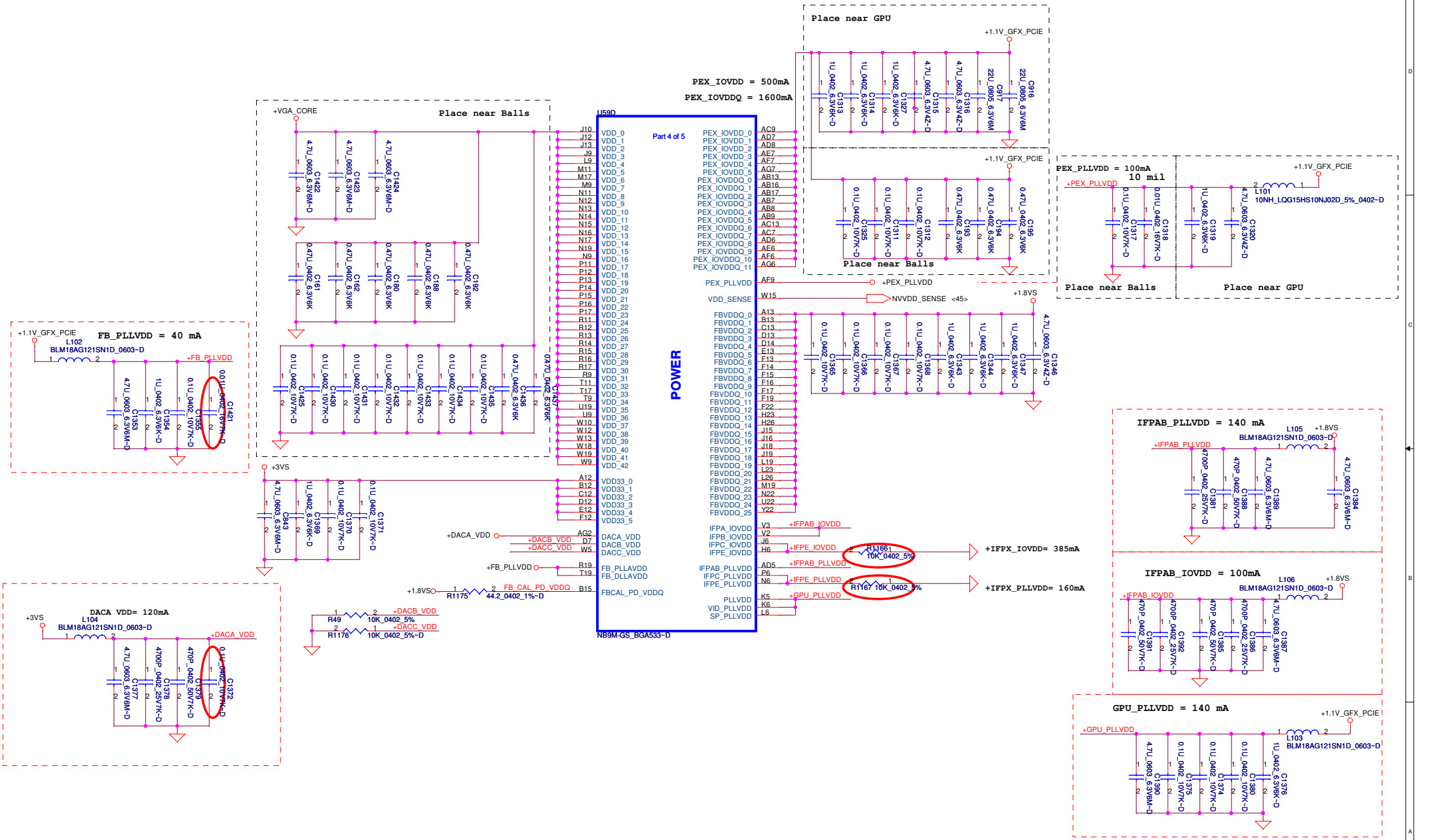
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: NVG98 Memory Interface

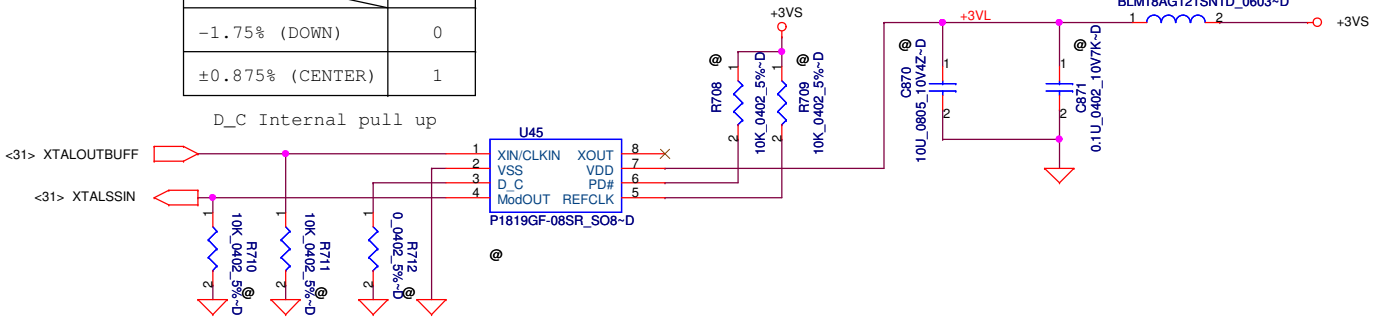
Size | Document Number: LA-4595P | Rev: 1.0

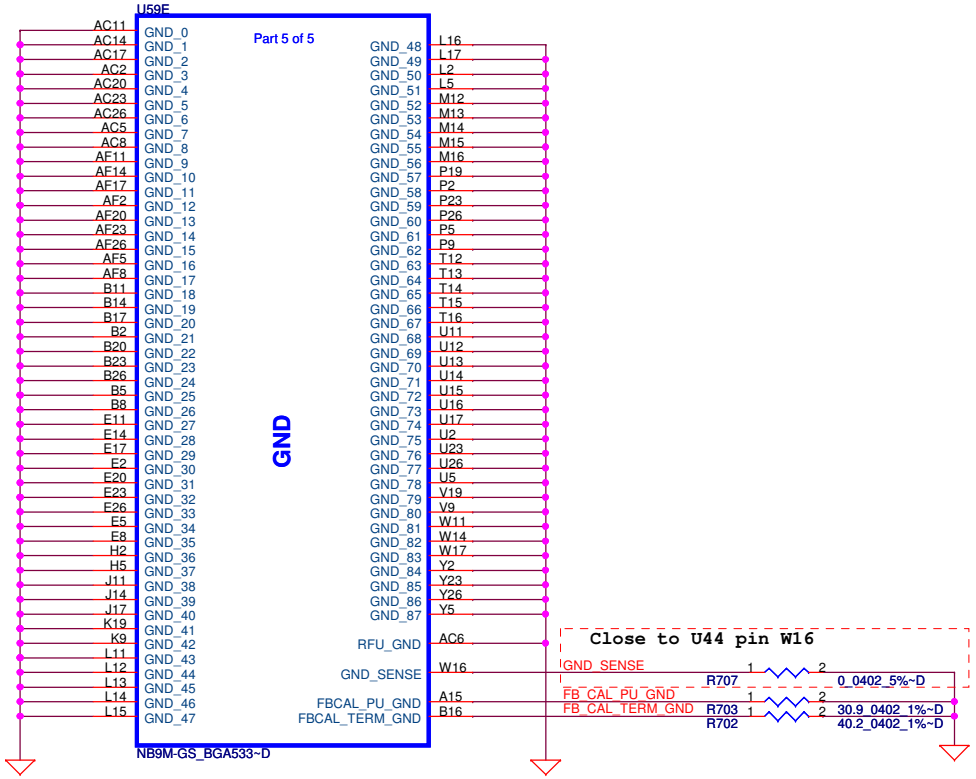
Date: Tuesday, February 17, 2009 | Sheet 32 of 49



	D_C
-1.75% (DOWN)	0
±0.875% (CENTER)	1

D_C Internal pull up



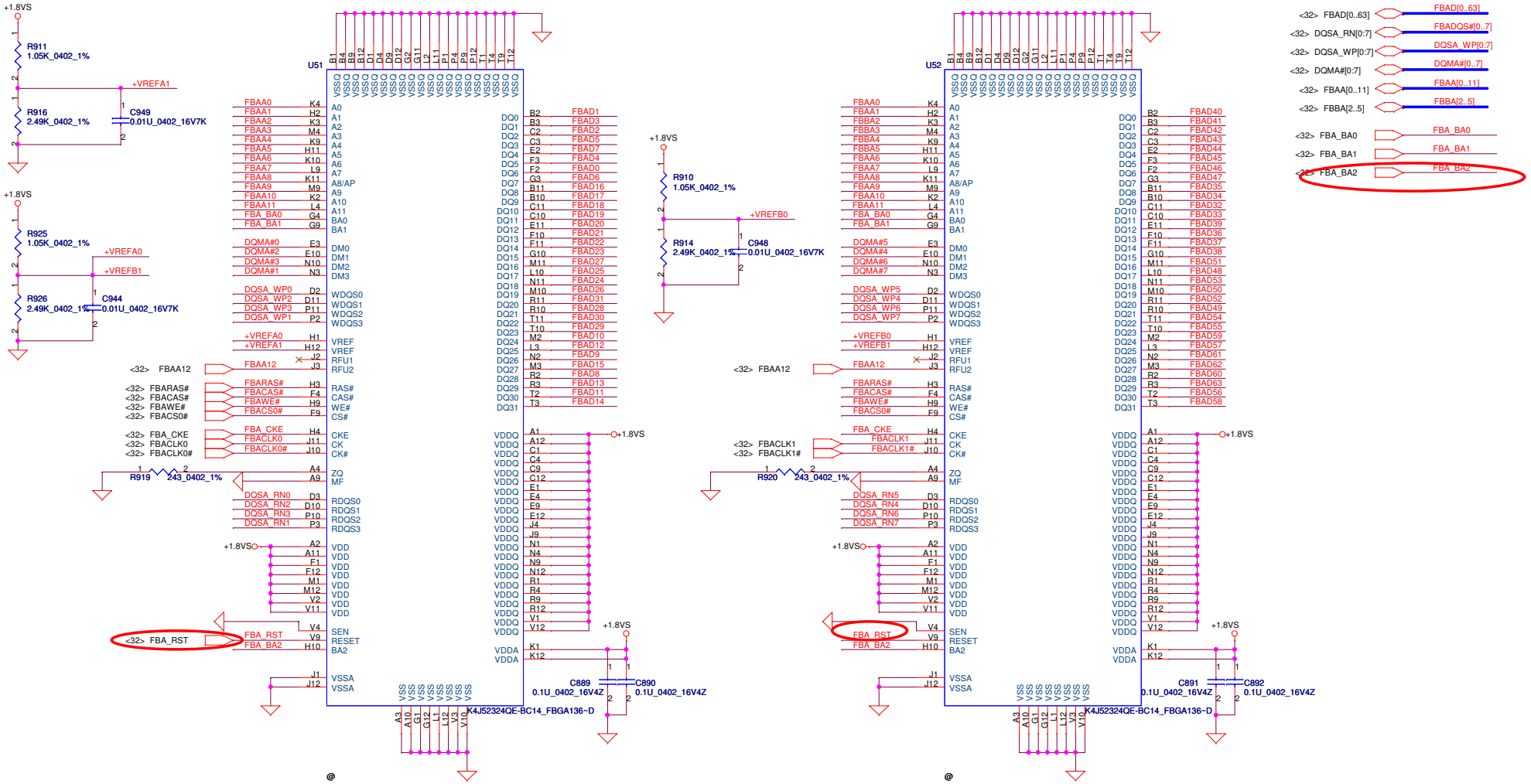


Compal Electronics, Inc.

Title: NVG98 GND

Size: | Document Number: LA-4595P | Rev: 1.0

Date: Tuesday, February 17, 2009 | Sheet 34 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/02/12	Deciphered Date	2008/02/12

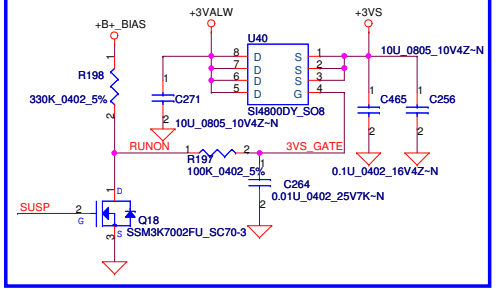
Compal Electronics, Inc.

Title: VRAM GDDR3 A

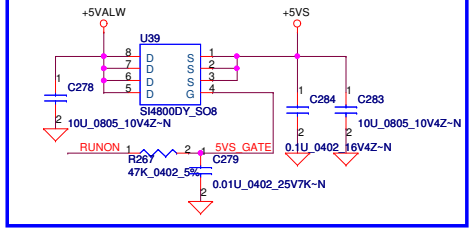
Size	Document Number	Rev
	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 35 of 49

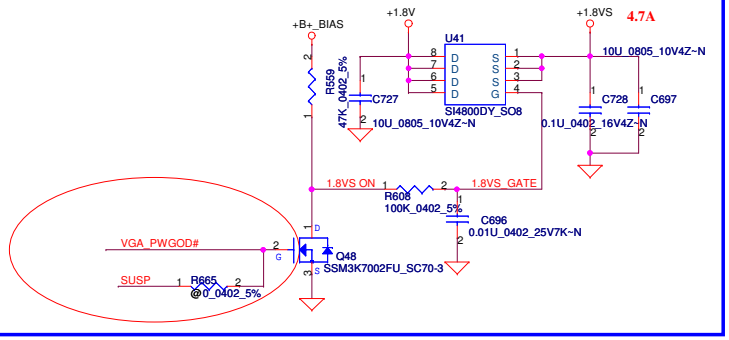
+3VALW to +3VS Transfer

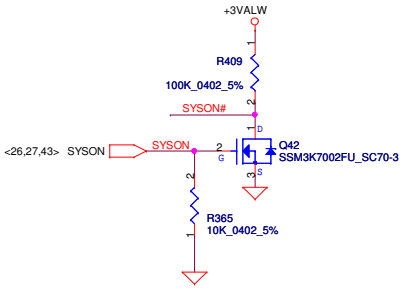


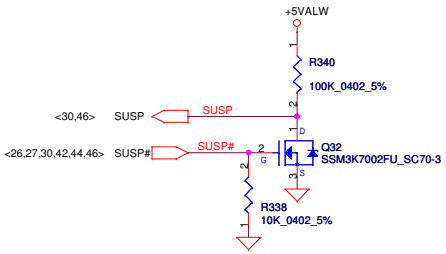
+5VALW to +5VS Transfer

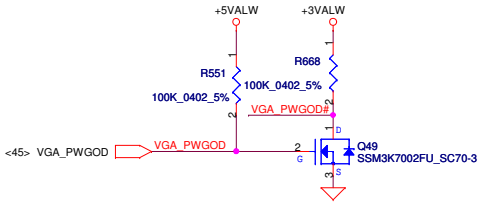


+1.8V to +1.8VS Transfer



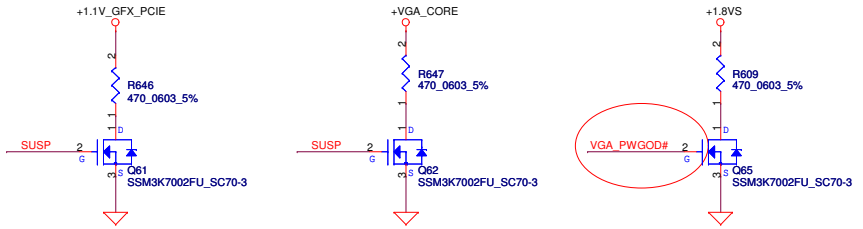




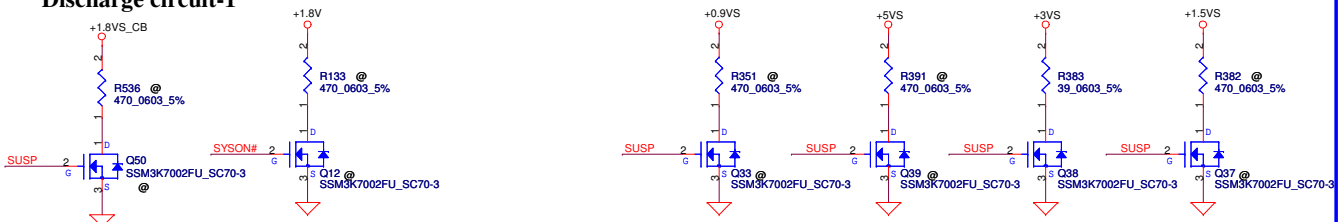


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

VGA Discharge circuit



Discharge circuit-1



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

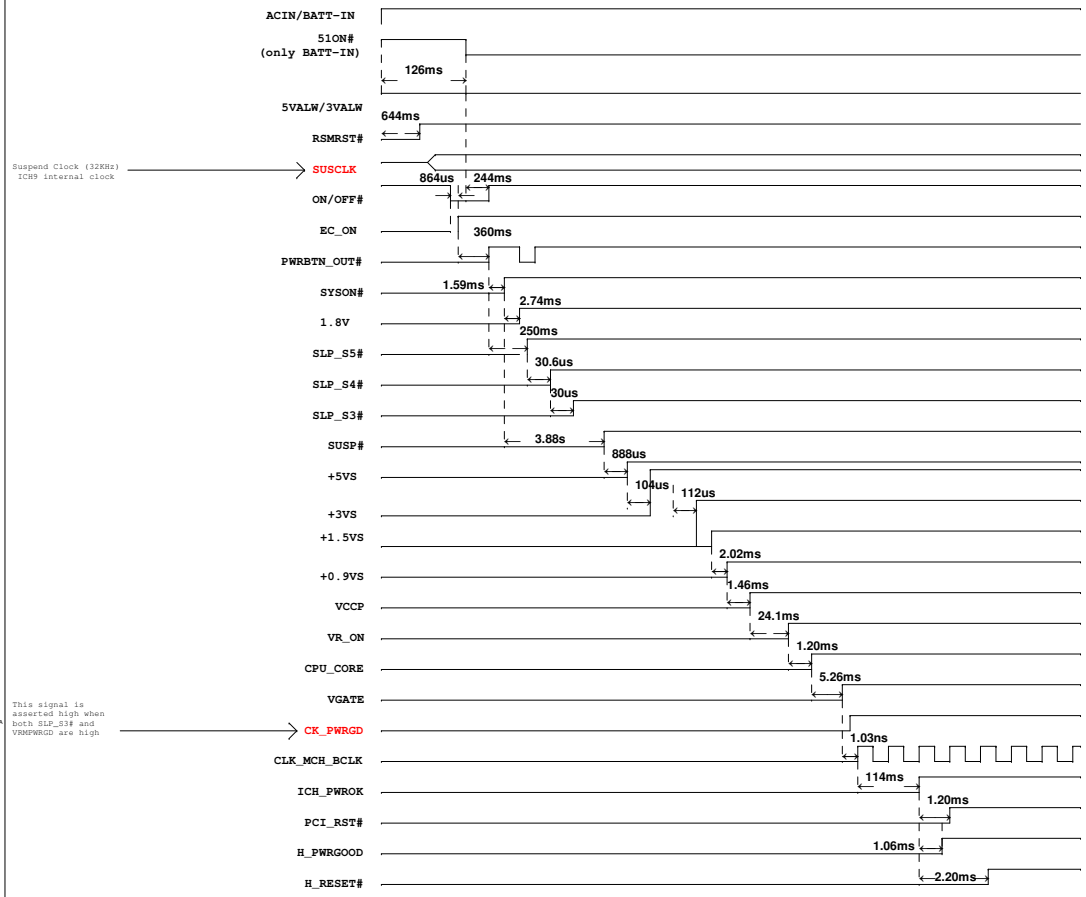
Compal Electronics, Inc.

Title: DC/DC Circuits

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 | Sheet 36 of 49

KAL80 POWER UP SEQUENCE



Title: Power Sequence		
Size: Custom	Document Number: LA-4595P	Rev: 1.0
Date: Tuesday, February 17, 2009	Sheet 37 of 49	

Version Change List (P. I. R. List)

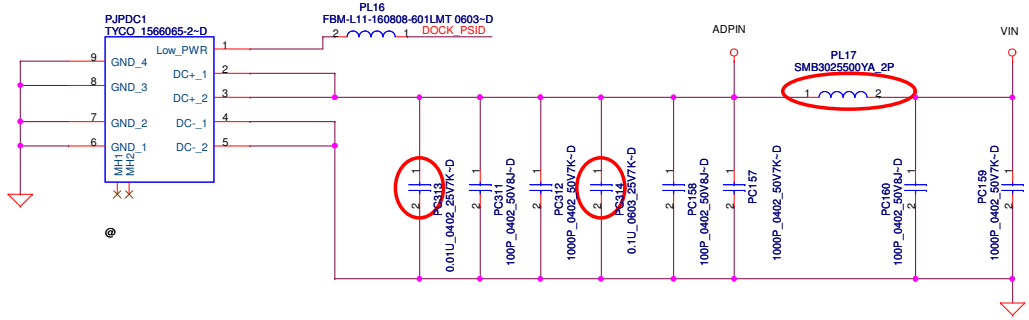
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1		Swap SW1	12/02	EE			
2		Update JUSBP3 pin define	12/02	EE			
3		R405 POP	12/02	EE			
4		U50 unPOP & R1190 POP	12/02	EE			
5		WWAN move to PORT6	12/02	BIOS			
6		Add C1391 & C1392	12/02	NVidia	LVDS single channel issue	Short U59.V2 & U59.V3. Add C1391 C1392 for IFPB_IOVDD	
7		Swap JSPK1 Pin	12/02	EE			
8		R101	12/04	EE	Change to 0805		
9		TPM Con	12/04	EE	Modify to Con		
10		R76 & R78 UnPOP	12/09	EE	EC update to Rev:C1		
11		Q7 & Q9	12/09	EE	Update Q7 & 9 footprint		
12		R658 & R281	12/11	EE	R685 UnPOP & R281 UnPOP for wake on LAN		
13		U89 & WLANPW_DIS#	12/11	EE	Add U89 for wake on LAN. Add WLANPW_DIS# of EC		
14		C1484 & C1485	12/11	EE	C1484 & C1485 modify to 1U form LAN vendor		
15		Update PW schematic	12/12	PW			
16		C260 & C252	12/15	EE	IDT ask UnPop		
17		Add D29 D28	12/15	ESD	ESD for LAN		
18		U9 Pop & U10 UnPop	12/15	ME			
19		Wake On WLAN	12/16	EE	Modify WLANPW_DIS# circuit		
20		Add T49 & T53	12/16	Layout			
21		C696	12/16	EE	Update PN		
22		WLANPW_DIS#	12/17	EE	Move WLANPW_DIS# to EC-GPIO40 and Del BTOP_ON		
23		L42 & L43	12/17	EMI	L42 & L43 update to Bead from 0 ohm		
24		C3 C4 C6 C14 C17	12/17	EMI	POP 100 P		
25		R69	12/17	EE	Update to Bead drom 100 ohm		
26		Cap	12/17	EMI	Add C1469 C1470 C1471 C1472 C1481 R81		
27		D21 D12 D17	12/17	ESD	ESD ask POP		
28		Update PW schematic	12/17	PW			
29		Update Q128 Q130 PN	12/18	EE			
30		Update Board ID	12/18	EE	R231		
31		Add U16 for OZ888	12/18	EE			
32		C1323 POP	12/18	EE	For Kepart		
33		R1421 UnPOP	12/22	EE			
34		C292 C297	12/22	EE	Modify to 22P form 18P (Crystal Vendor)		
35		C1745 C1749	12/22	EE	Modify to 18P form 10P(C1749) and 15P from 10P(C1745)(Crystal Vendor)		
36		C1211	12/22	EE	Modify to 12P form 15P (Crystal Vendor)		
37		R1423 & R1422	01/07	EE	Add for O2		
38		L6 & R1190	01/10	EE	Change to 0805		
39		Modify LDO to +5VS	01/12	EE			
40		Add C80 & D59 & D60	01/12	EE			
41		Add components of JHP1	01/13	EE	For vendor		
42		R360 & R361	01/19	EE	Update R360 & R361 to 56 ohm		
43		U37	01/19	EE	Update U37 to SA00001KN10		
44		R231	01/19	EE	Update Board ID		

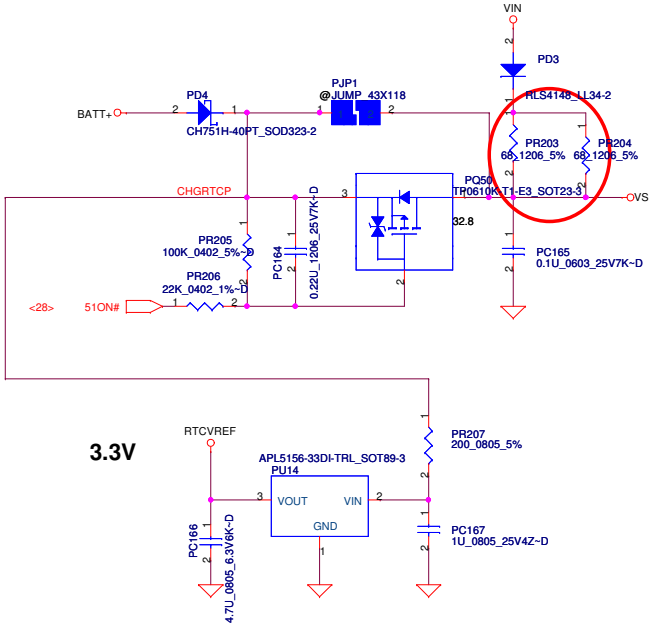
Compal Electronics, Inc.

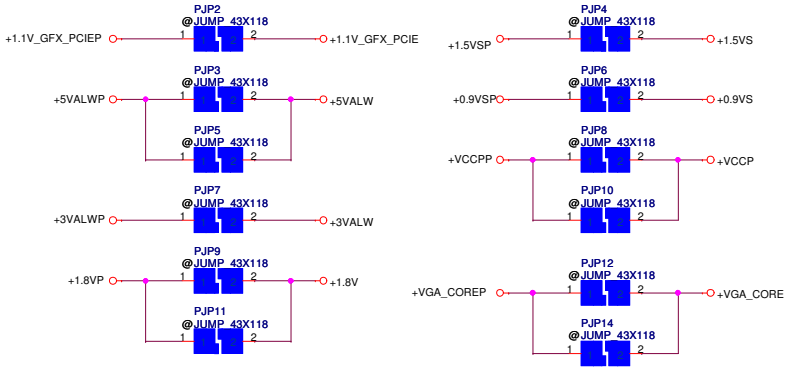
Title: EEW PIR-1

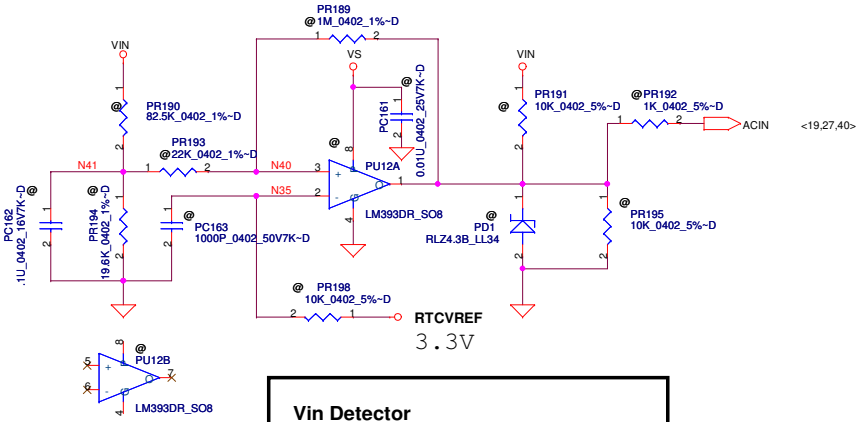
Size: Custom | Document Number: LA-4595P | Rev: 1.0

Date: Tuesday, February 17, 2009 | Sheet 38 of 49



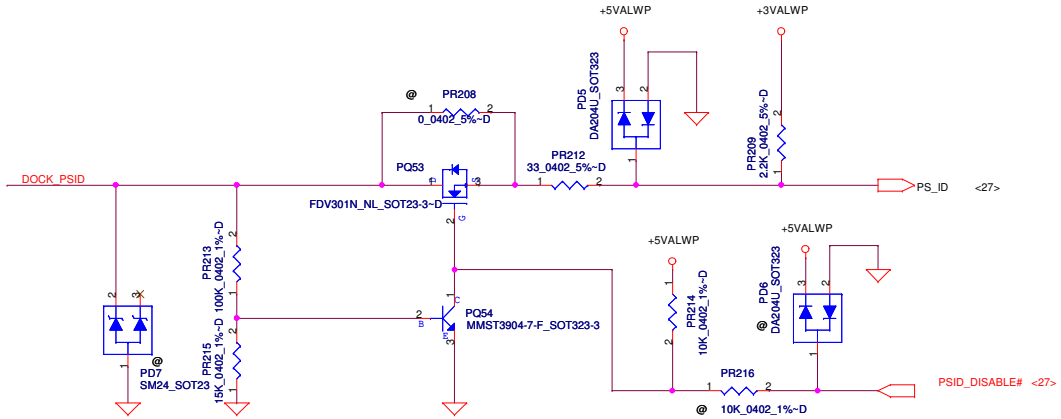






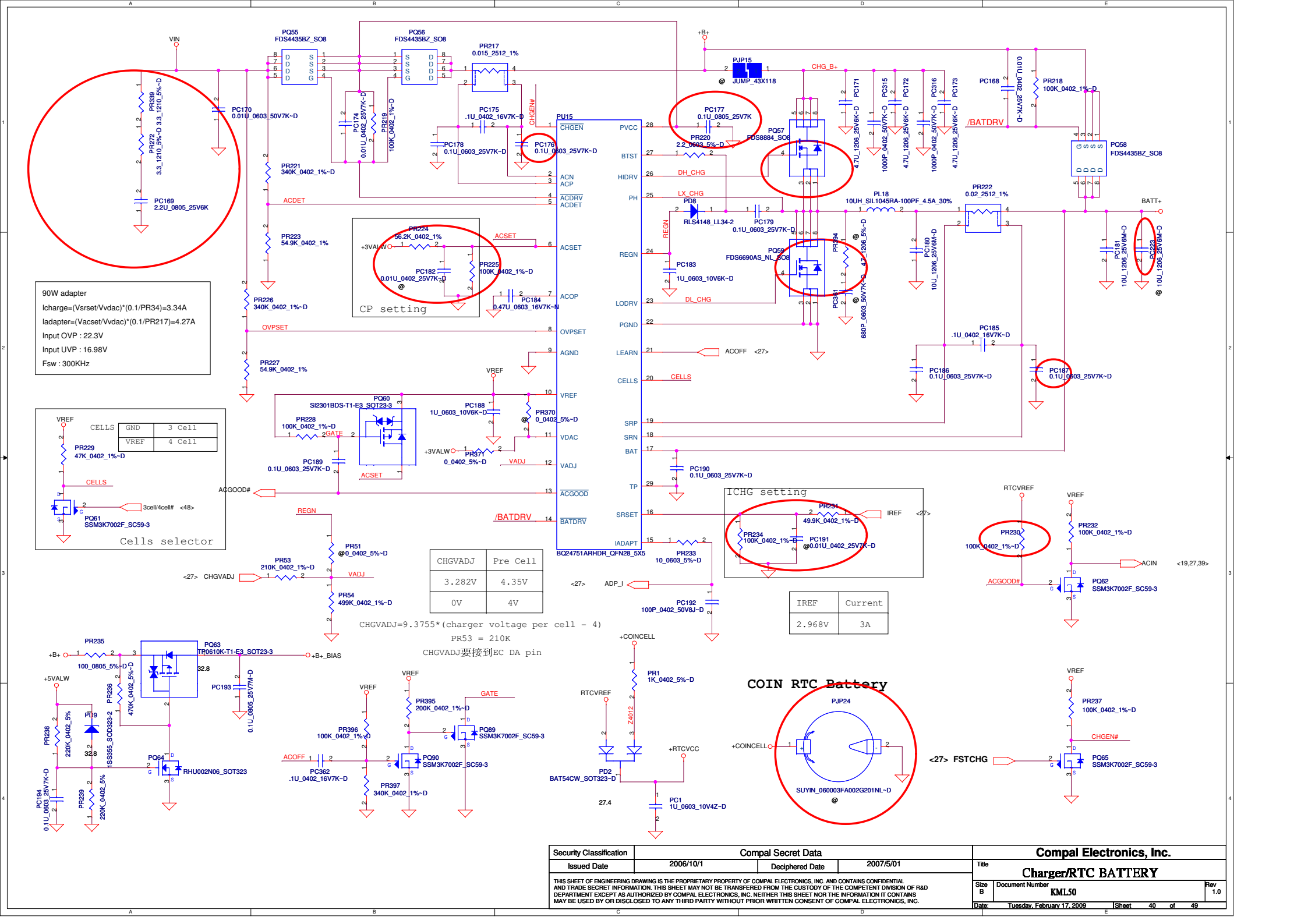
Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	DCIN / Vin Detector		
Size	Document Number		Rev
Custom	LA-4595P		1.0
Date:	Tuesday, February 17, 2009	Sheet	39 of 49


90W adapter
Icharge=(Vsrset/Vvdac)*(0.1/PR34)=3.34A
Iadapter=(Vacset/Vvdac)*(0.1/PR217)=4.27A
Input OVP : 22.3V
Input UVP : 16.98V
Fsw : 300KHz
CP setting
Cells selector
ICHG setting
COIN RTC Battery
CHGVADJ=9.3755*(charger voltage per cell - 4)
PR53 = 210K
CHGVADJ要接到EC DA pin
CELLS | GND | 3 Cell
VREF | 4 Cell
CHGVADJ | Pre Cell
3.282V | 4.35V
0V | 4V
IREF | Current
2.968V | 3A
BQ24751ARHDR_QFN28_5X5
Security Classification | Compal Secret Data
Issued Date | 2006/10/1 | Deciphered Date | 2007/5/01
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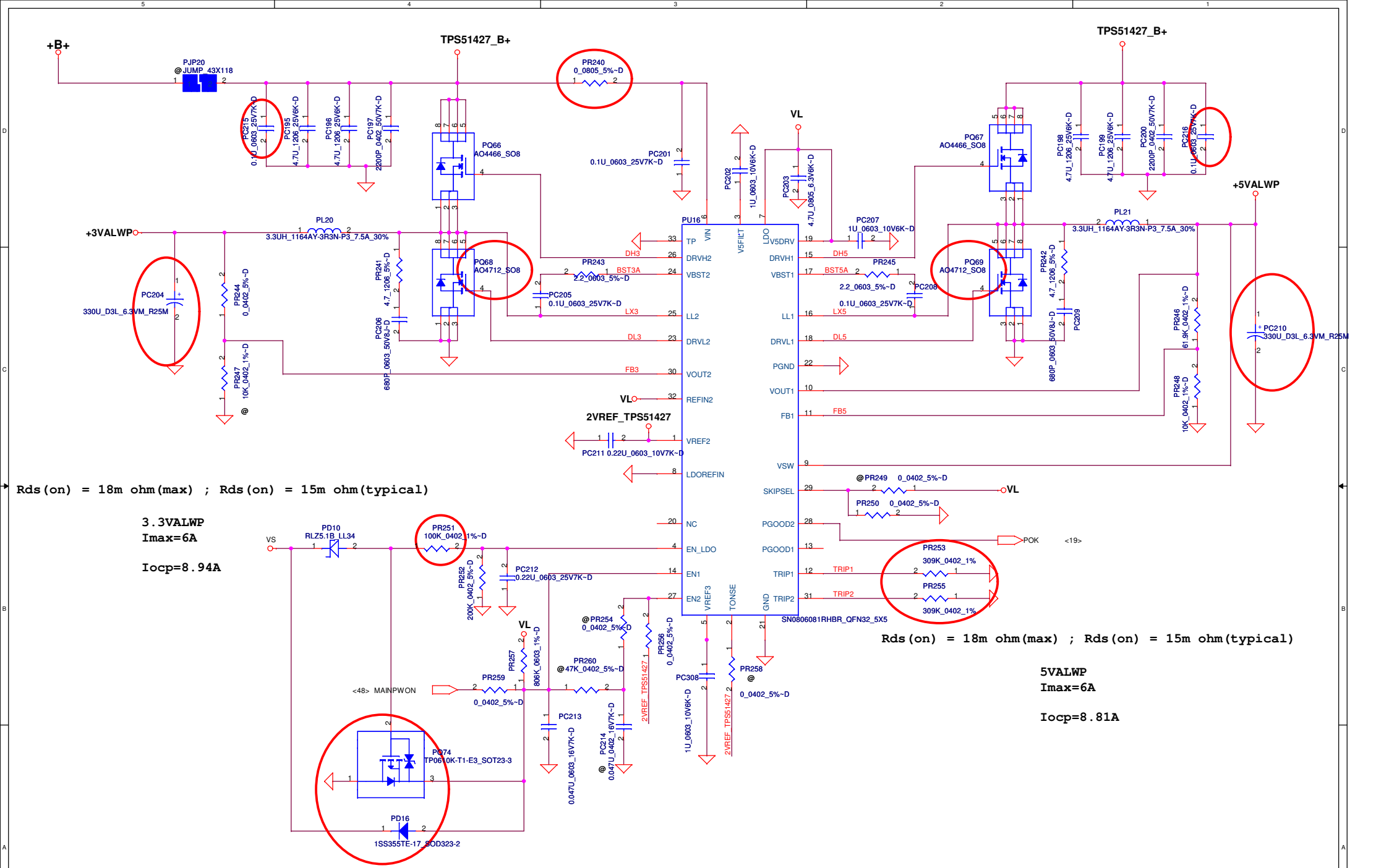
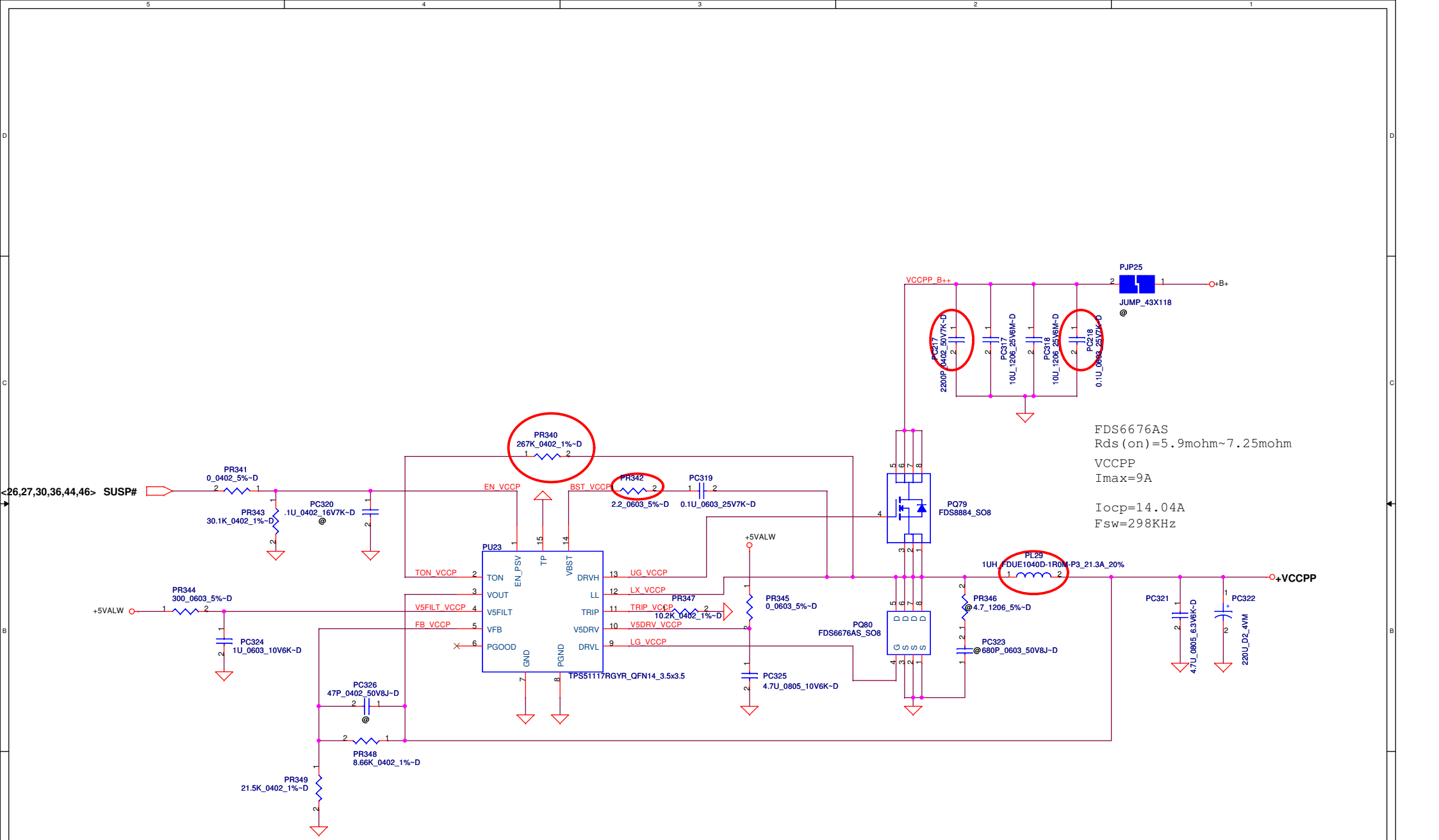
Compal Electronics, Inc.
Title: Charger/RTC BATTERY
Size: B | Document Number: KML50 | Rev: 1.0
Date: Tuesday, February 17, 2009 | Sheet 40 of 49



Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

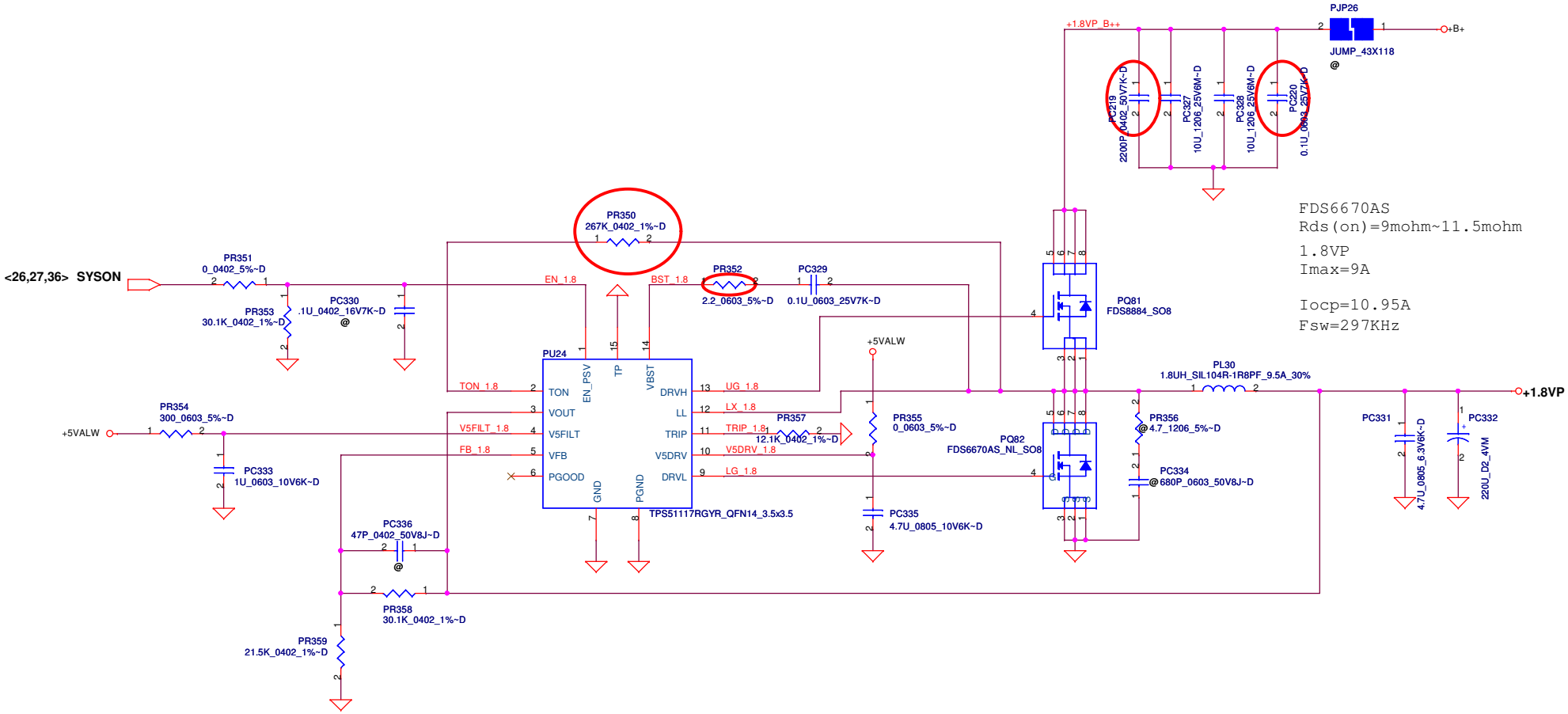
Compal Electronics, Inc.

Title	+3VALWP, +5VALWP	
Size: Custom	Document Number: LA-4595P	Rev: 1.0
Date: Tuesday, February 17, 2009	Sheet 41 of 49	



Security Classification	Compal Secret Data		
Issued Date	2008/2/5	Deciphered Date	2009/2/5

Compal Electronics, Inc.			
Title	+VCCPP		
Size	Document Number	LA-4595P	Rev 1.0
Date:	Tuesday, February 17, 2009	Sheet 42 of 49	



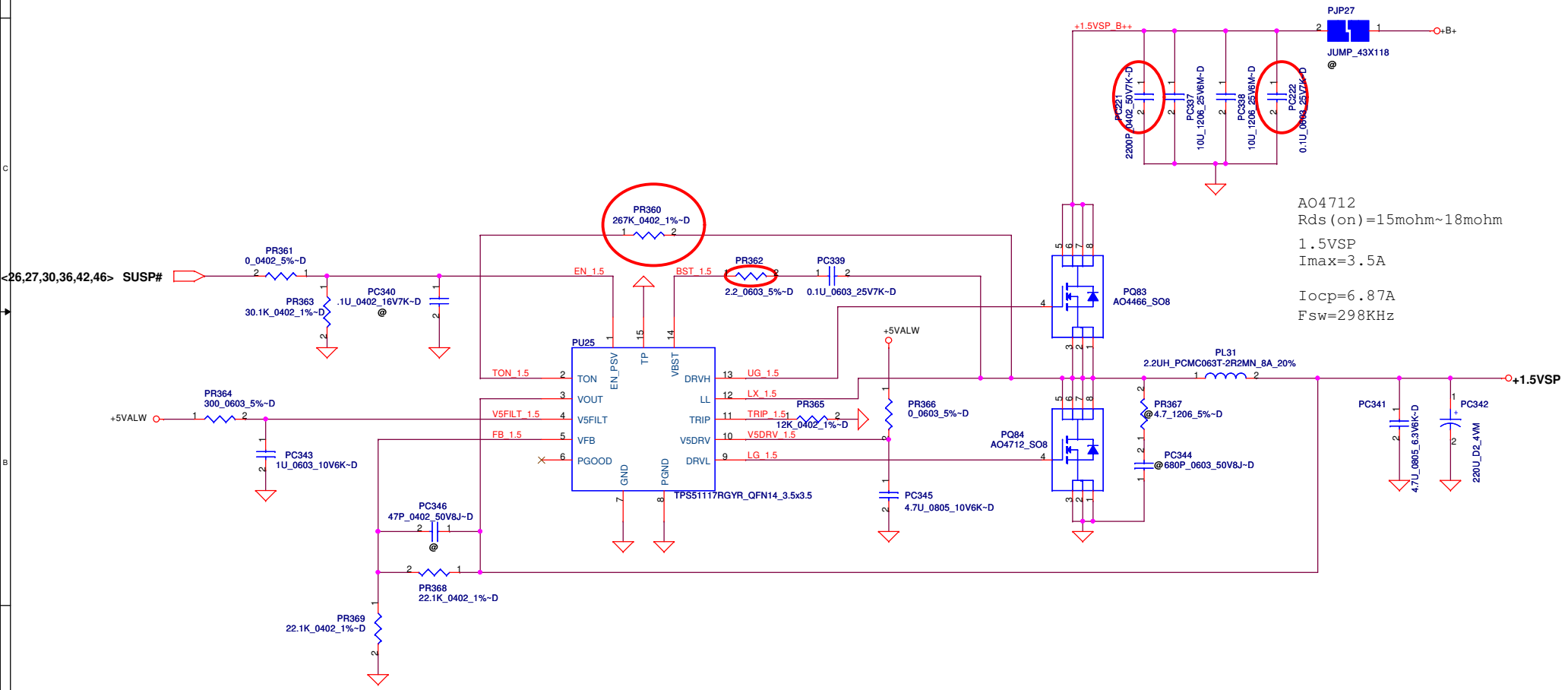
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: +1.8VP

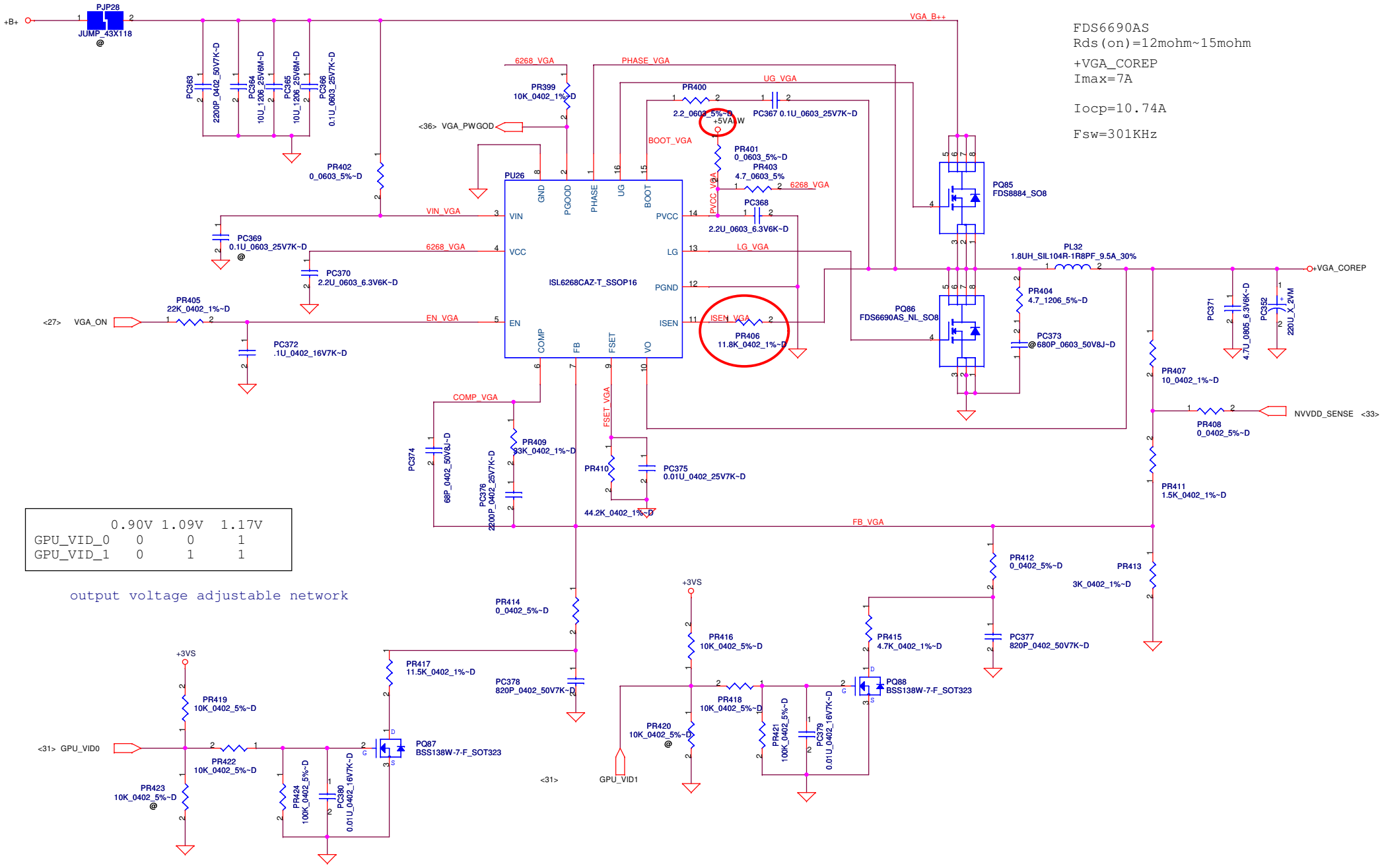
Size | Document Number: LA-4595P | Rev: 1.0

Date: Tuesday, February 17, 2009 | Sheet 43 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/2/5	Deciphered Date	2009/2/5

Compal Electronics, Inc.			
Title	+1.5VSP		
Size	Document Number	LA-4595P	Rev 1.0
Date: Tuesday, February 17, 2009	Sheet 44 of 49		



	0.90V	1.09V	1.17V
GPU_VID_0	0	0	1
GPU_VID_1	0	1	1

output voltage adjustable network

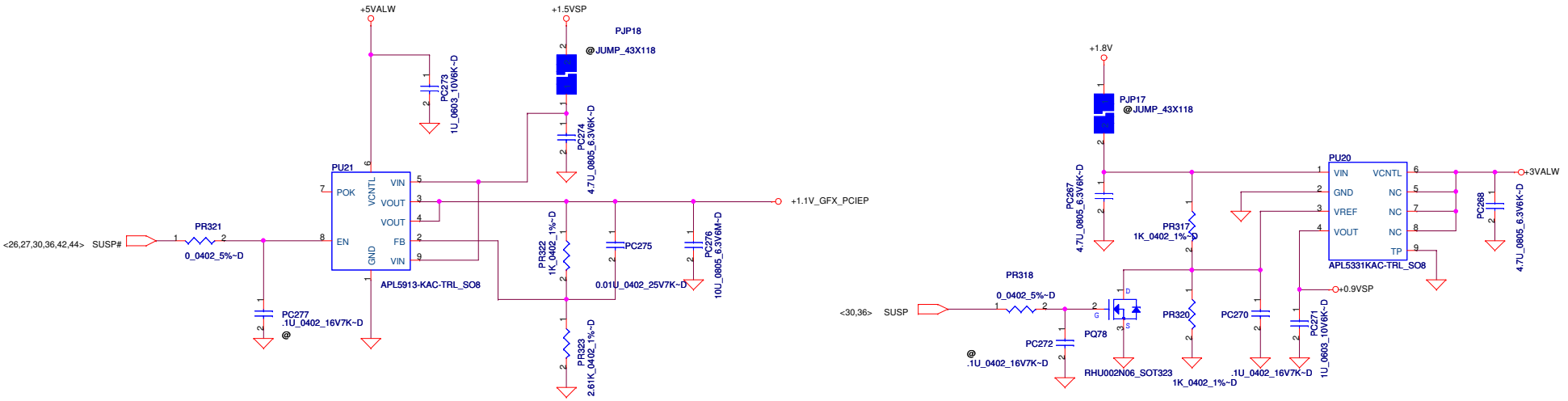
Security Classification	Compal Secret Data		
Issued Date	2008/2/5	Deciphered Date	2009/2/5

Compal Electronics, Inc.

Title: +VGA_CORE

Size | Document Number: LA-4595P | Rev: 1.0

Date: Tuesday, February 17, 2009 | Sheet 45 of 49



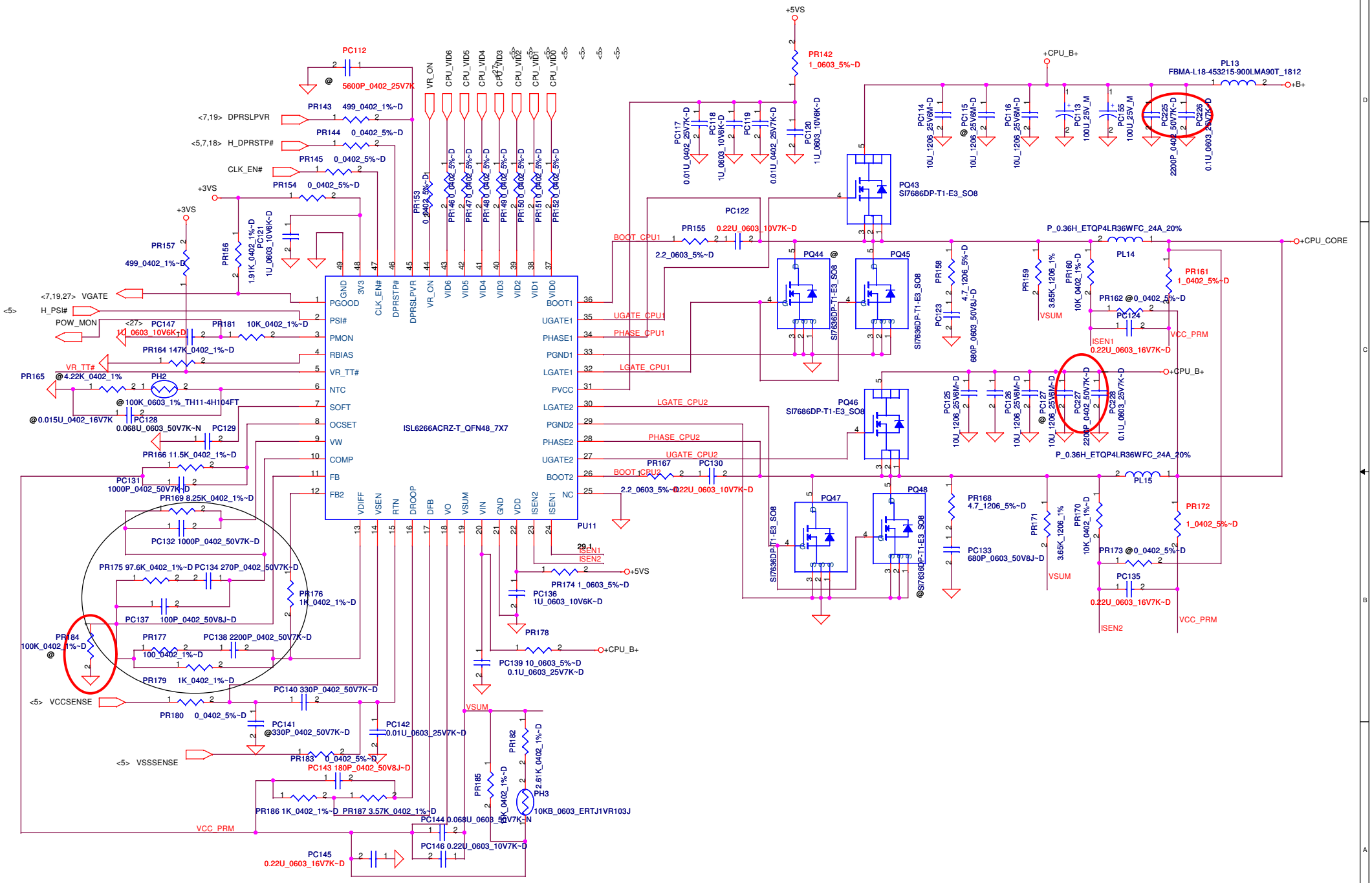
Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: +0.9VSP/+1.1V_GFX_PCIEP

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 Sheet 46 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

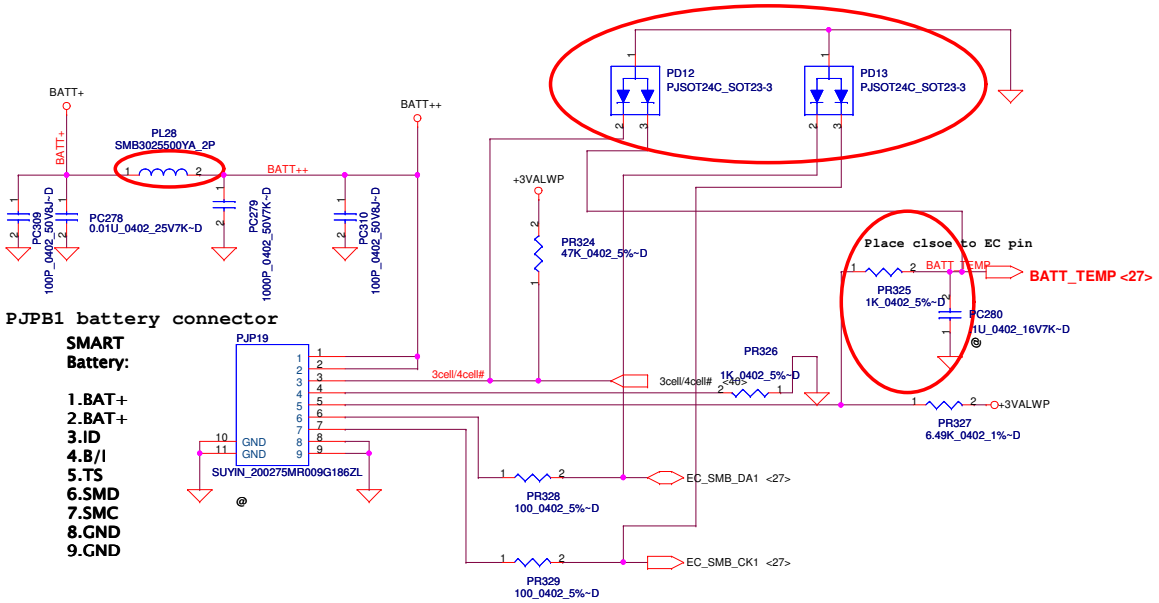
Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
Custom	LA-4595P	1.0

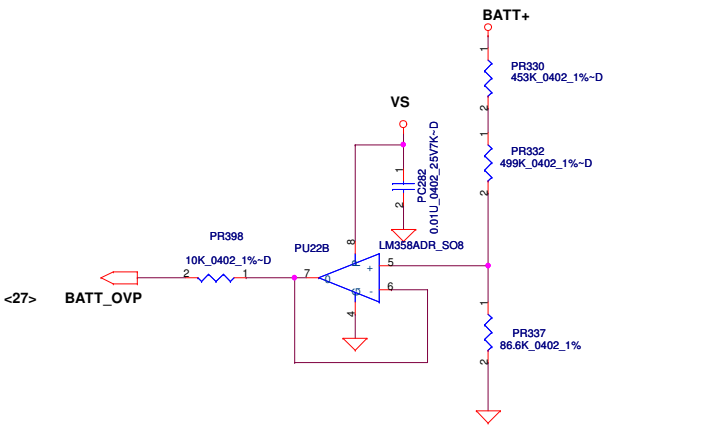
Date: Tuesday, February 17, 2009 Sheet 47 of 49

Battery Connect/OTP

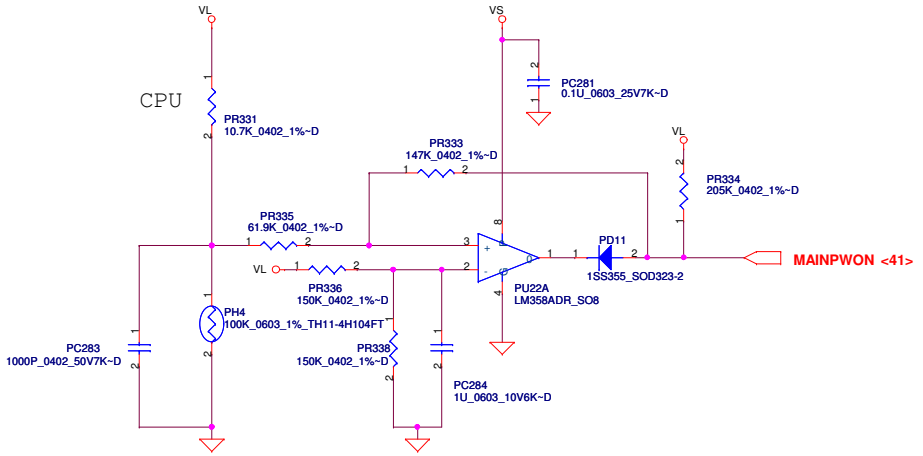


CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Compal Electronics, Inc.

Title: BATTERY CONN

Size: Custom | Document Number: LA-4595P | Rev: 1.0

Date: Tuesday, February 17, 2009 | Sheet 48 of 49

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	40	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	48	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	39	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	42	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	43	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	44	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
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Compal Electronics, Inc.

Title: PW PIR-1

Size	Document Number	Rev
Custom	LA-4595P	1.0

Date: Tuesday, February 17, 2009 | Sheet 49 of 49