Compal Confidential

KALH0 /KAL90+ /KALG0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-3-4

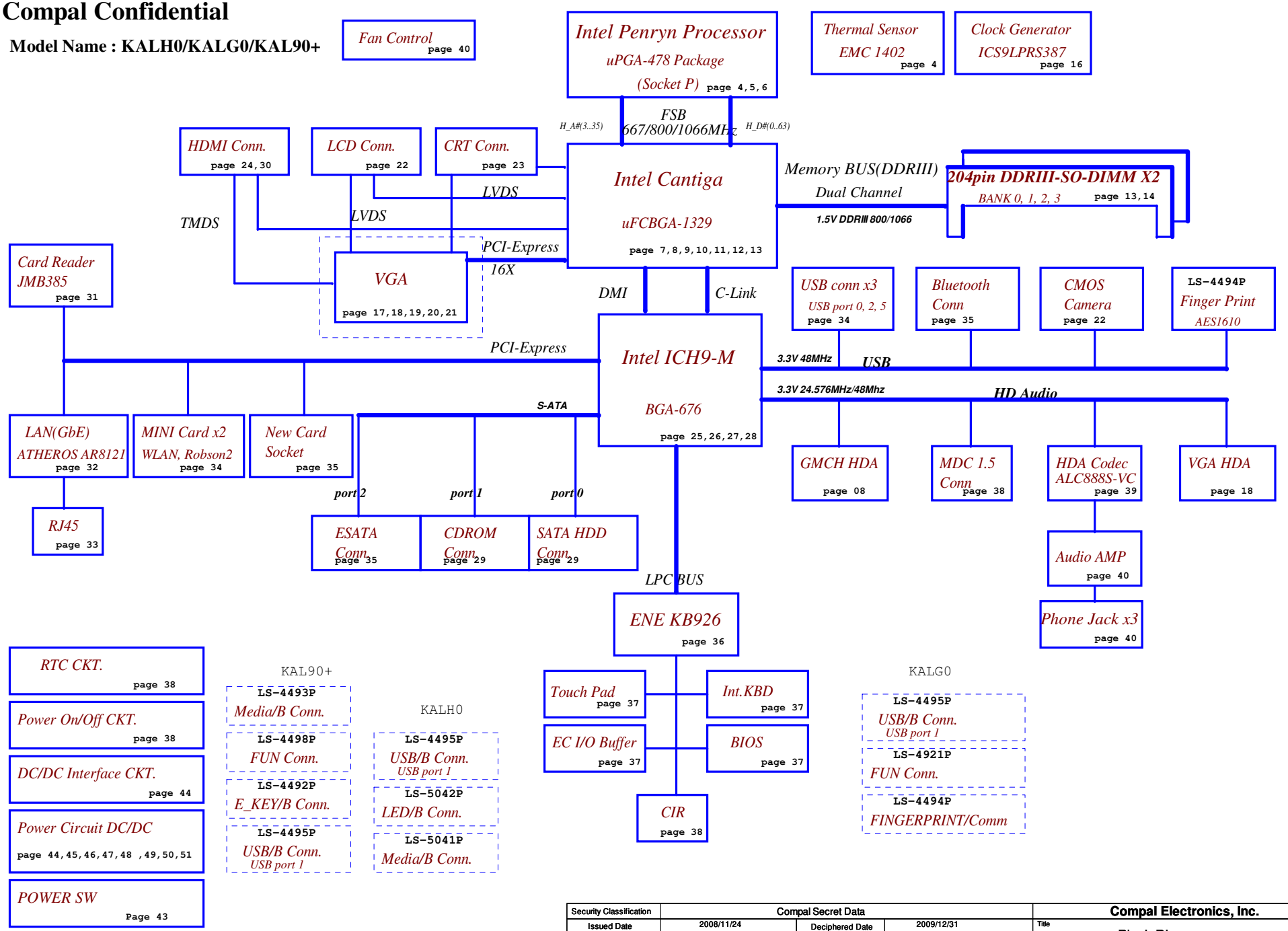
REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: KALH0/KALG0/KAL90+	Rev: 1.0
Date: Monday, April 27, 2009	Sheet 1 of 53	

Compal Confidential

Model Name : KALH0/KALG0/KAL90+



Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 2 of 53

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA/DDR3	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V GM LVDS MODULE	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
KAL90	KAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@
KAL90-G0	KAL90_G0@
KAL90-H0	KAL90_H0@
KALG0	KALG0@
KALH0	KALH0@
ALC268	268@
	KAL90_90+@
	KAL90_H0_G0@
	KAL90+_G0
	KALH0_G0
	KAL90_G0_90+@
	KAL90_H0_90+@
	KAL90+_PCB@
	KALG0_PCB@

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
MEDIA CONSOLE	1010 000X b

EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b
NB9M THERMAL SENSOR	

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Configuration Table

Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX:KAL90@/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX:KAL90@/PM@/888VC@/8121@
KALH0-GM45	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GM45@
KALH0-GL40	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GL40@
KALH0-PM45	XXXXXXXXXX:KALH0@/PM@/888VC@/8121@
KAL90+ -UMA	GM@/888VC@/8121@/GM45@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@
KAL90+ -Dis	PM@/888VC@/8121@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@/PM45@
KALG0 -UMA(GL40)	KALG0@/GM@/888VC@/8121@/GL40@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -Dis	KALG0@/PM@/888VC@/8121@/PM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -UMA(GM45)	KALG0@/GM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -DIS(GM45)	KALG0@/PM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@

KALG0 LAN to AR-8131------- 8121@ Change to 8131@

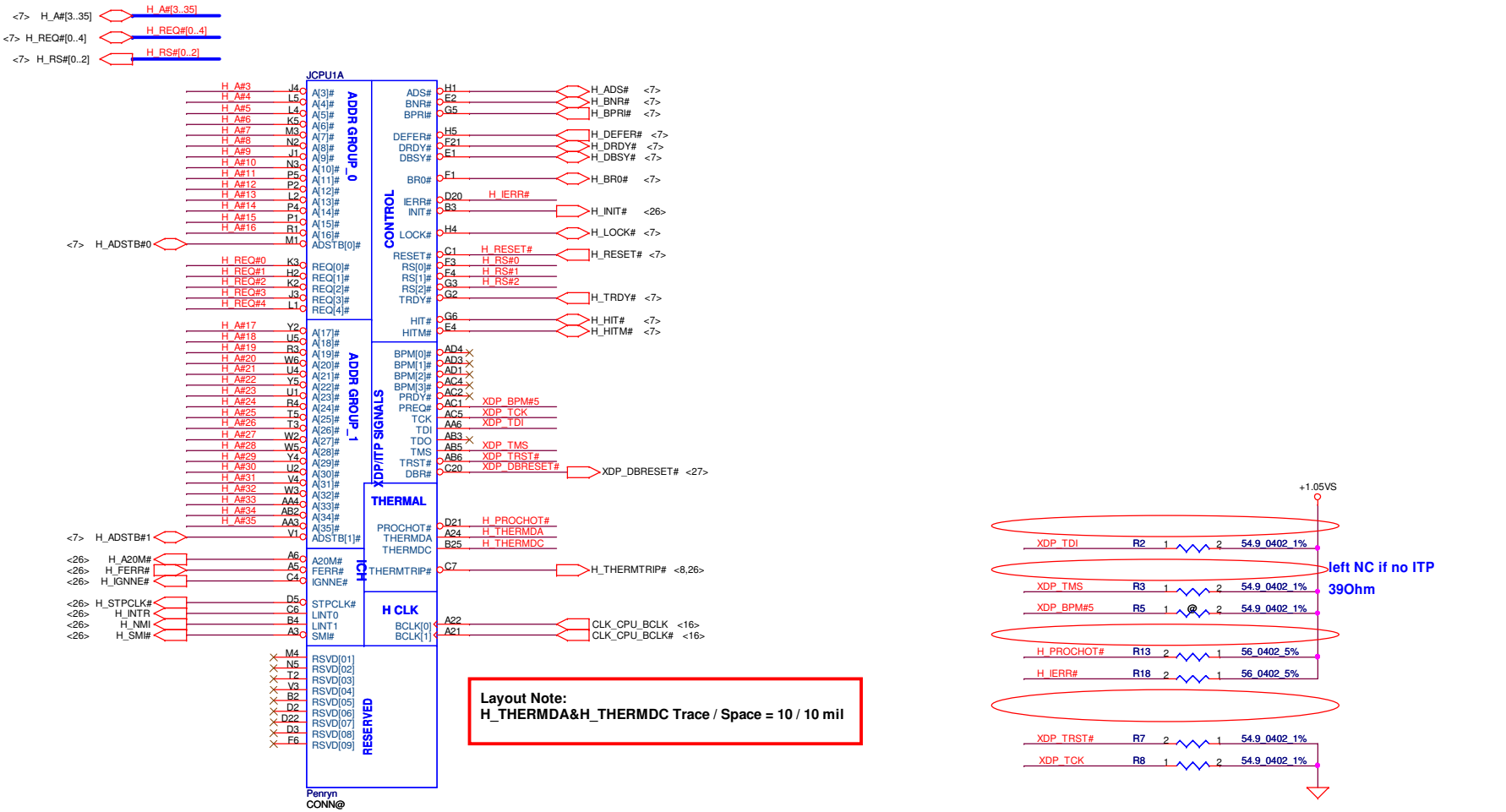
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

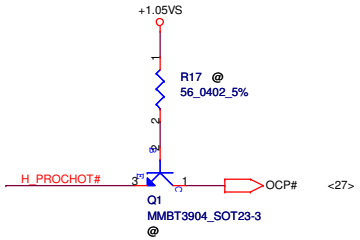
Title: Notes List

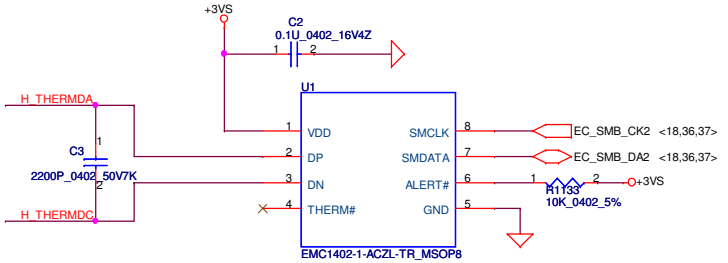
Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 3 of 53



BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166





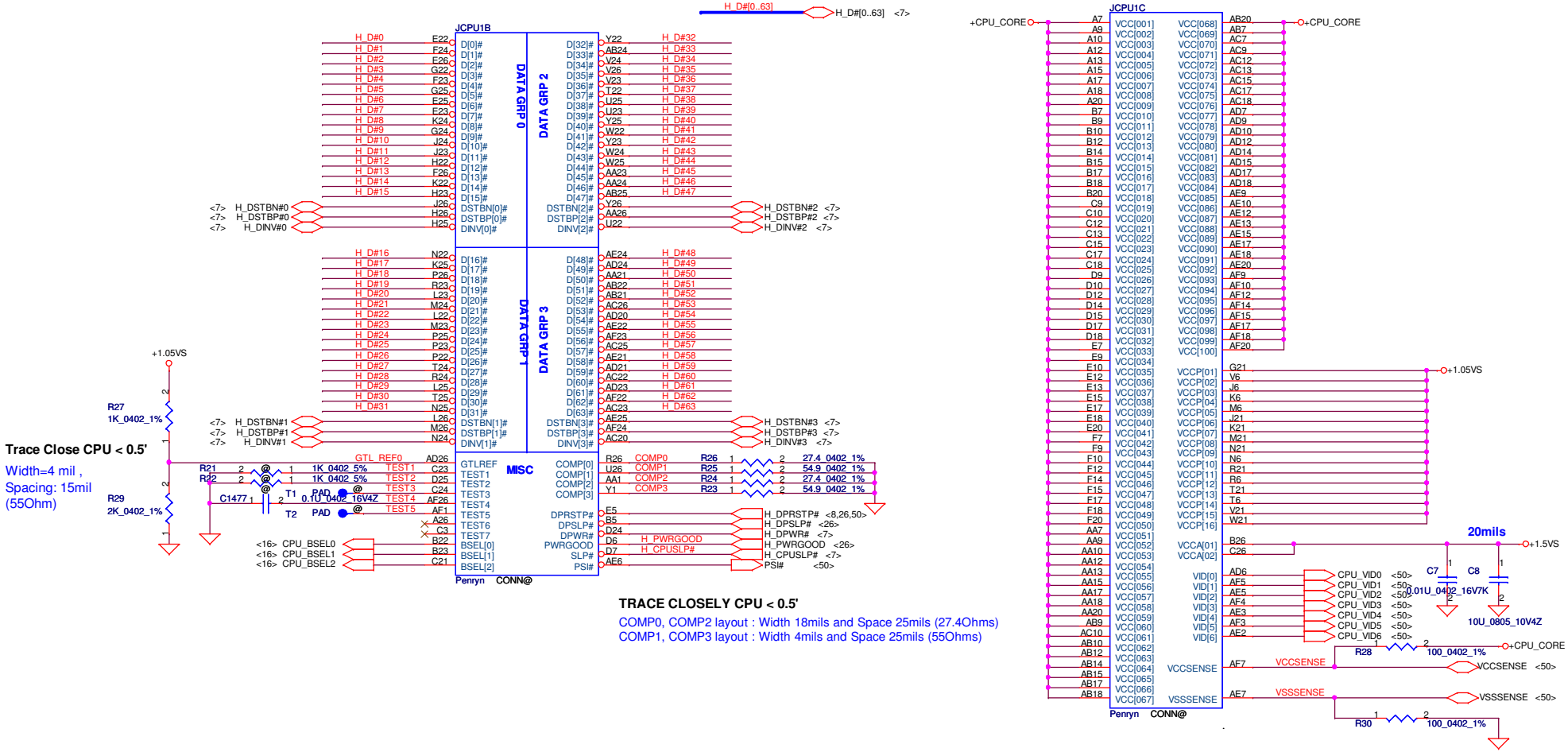
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Penryn (1/3)

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 4 of 53



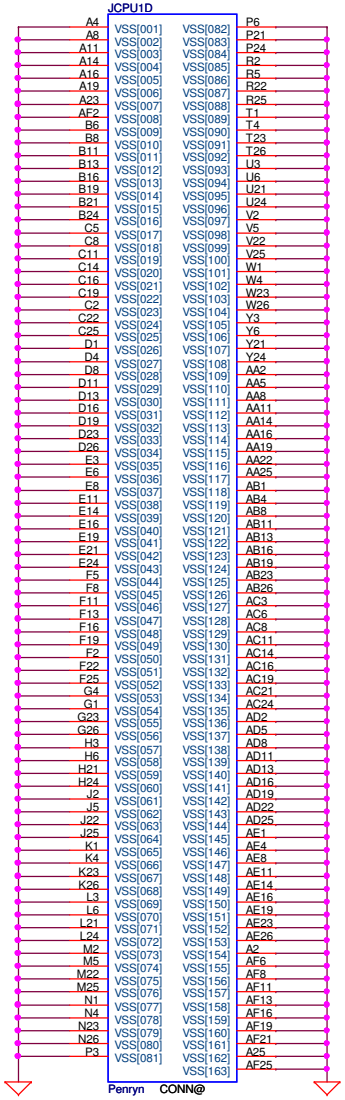
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

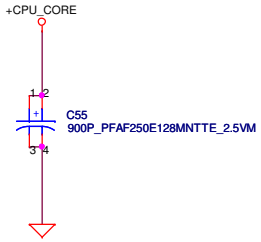
Compal Electronics, Inc.

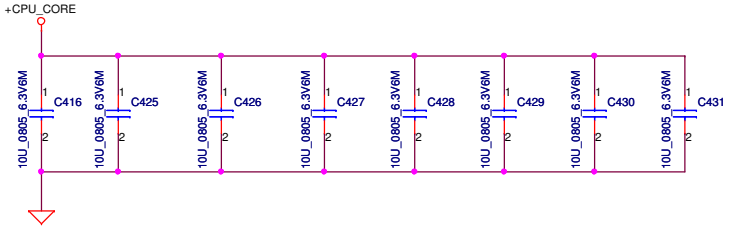
Title: Penryn (2/3)

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

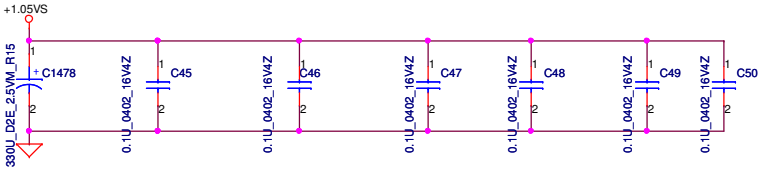
Date: Monday, April 27, 2009 Sheet 5 of 53







+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



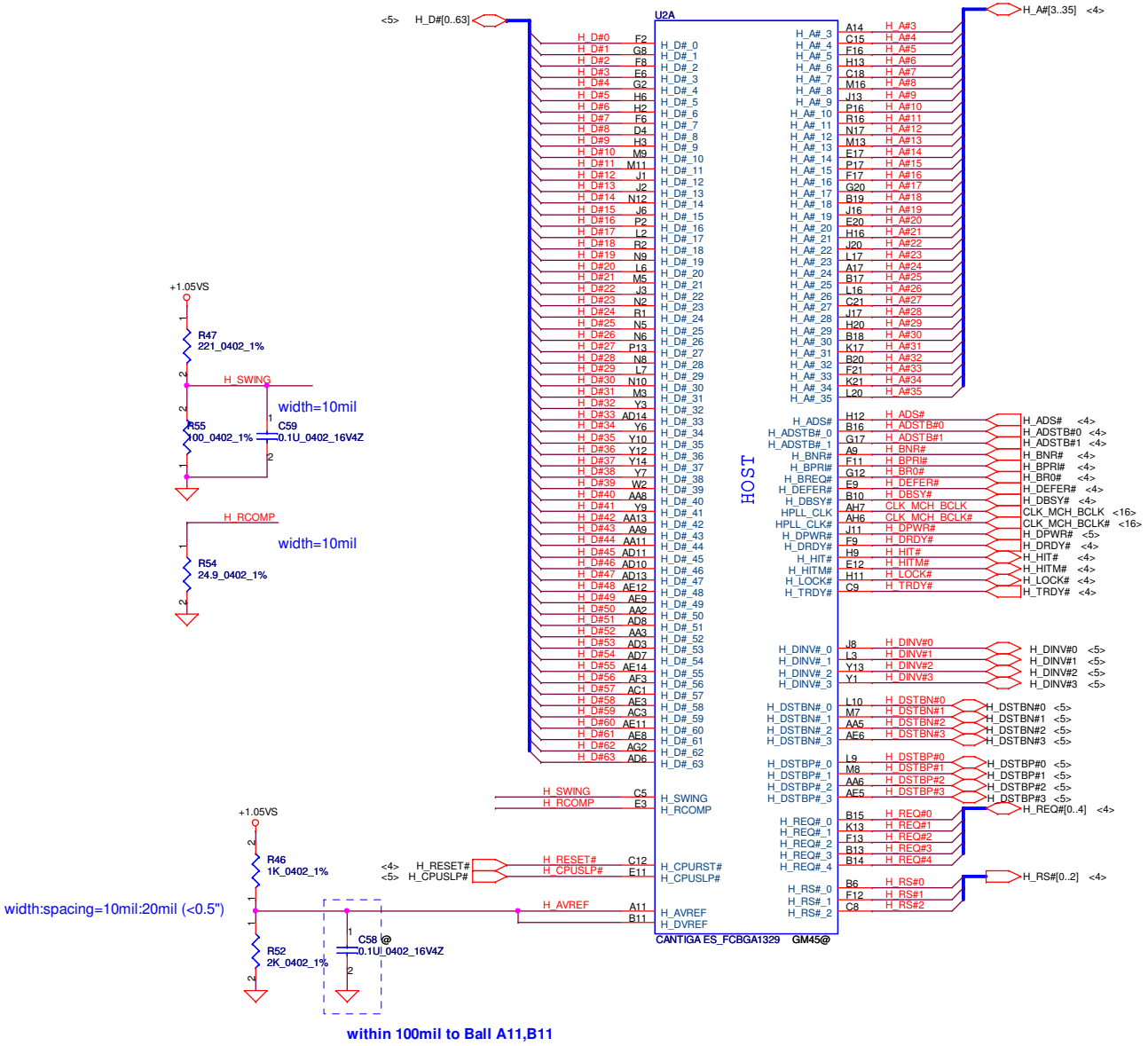
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Penryn (3/3)

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 Sheet 6 of 53



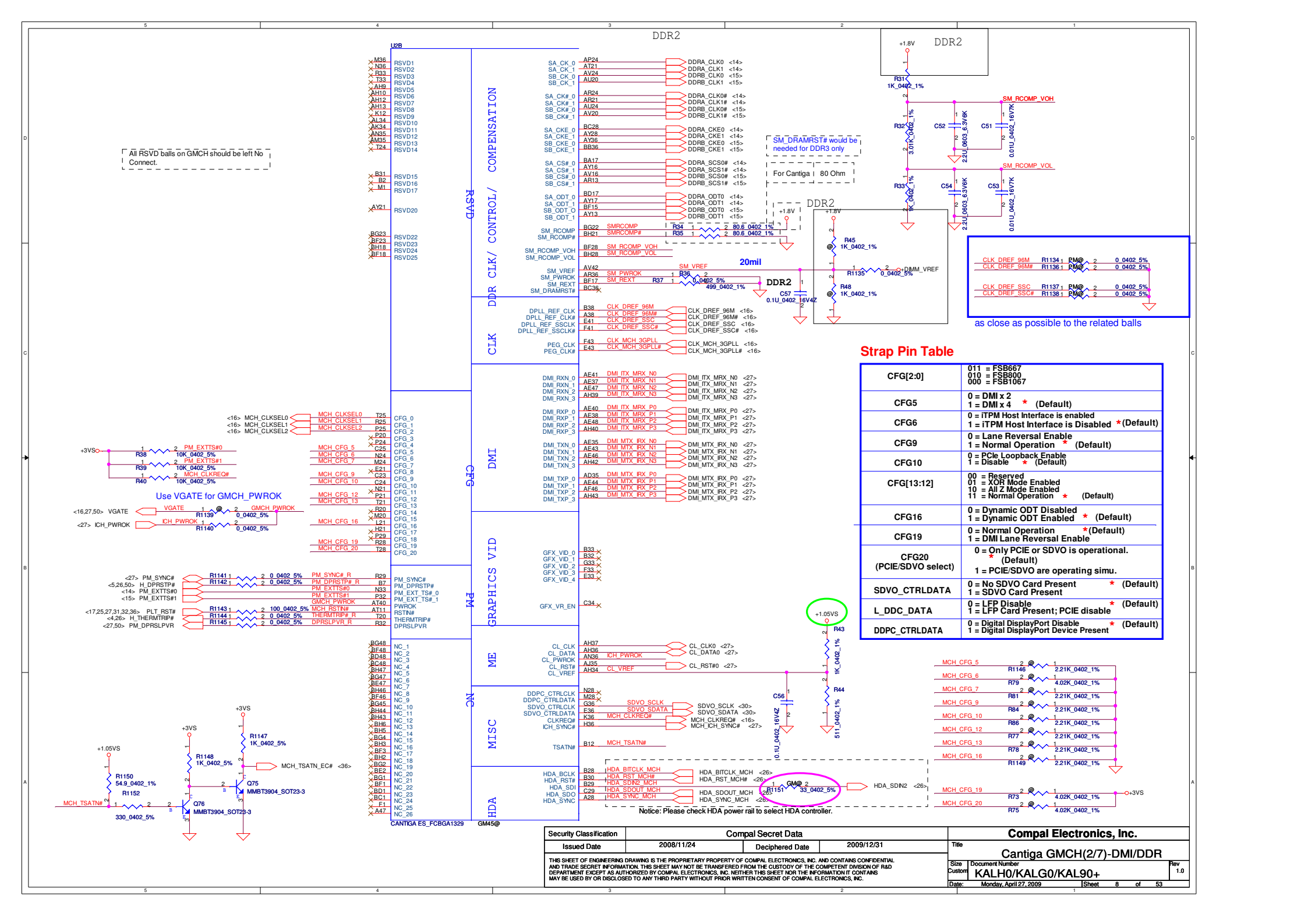
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Cantiga GMCH(1/7)-GTL

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 Sheet 7 of 53



Strap Pin Table	
CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIE disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

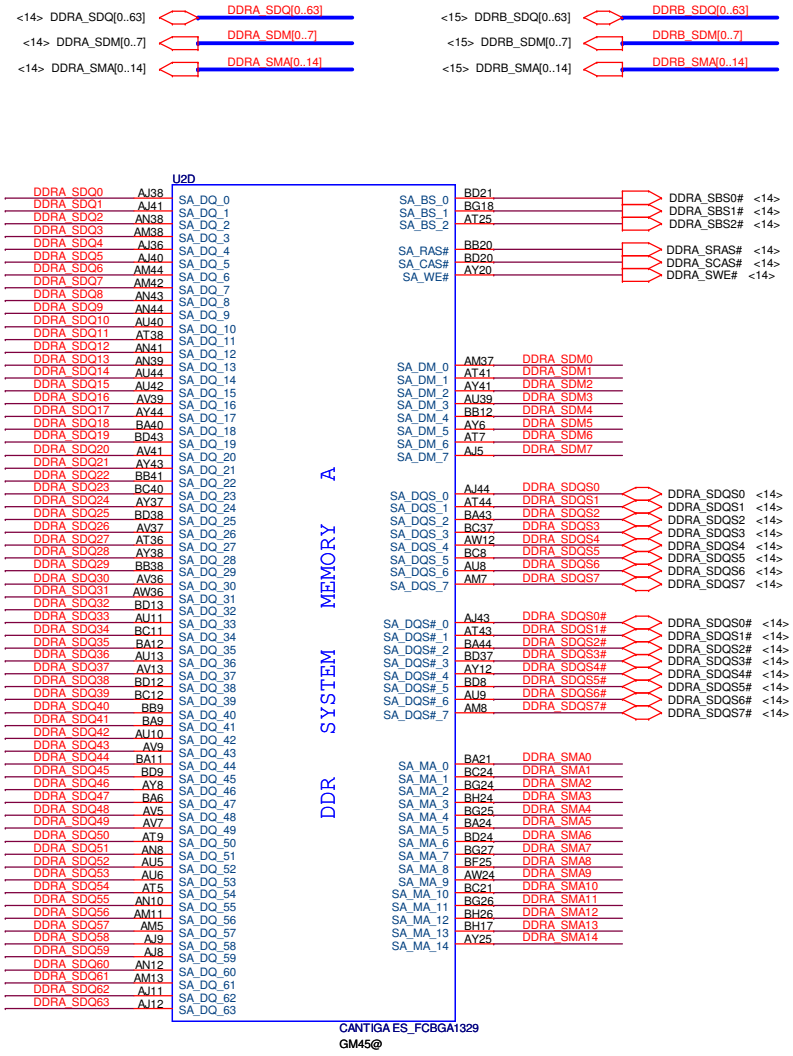
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Cantiga GMCH(2/7)-DMI/DDR

Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 8 of 53



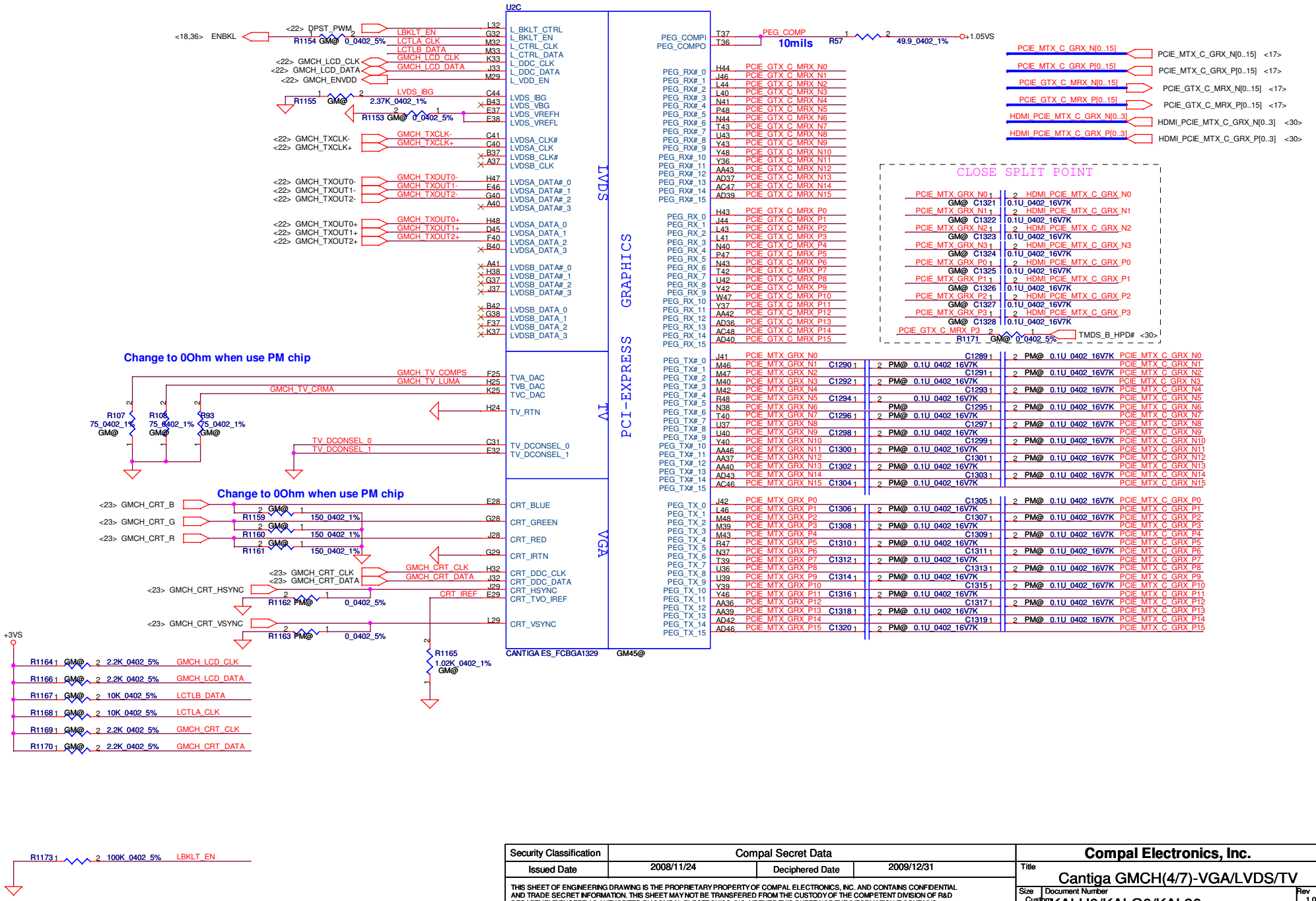
Security Classification	Compal Secret Data		
Issued Date	2008/03/28	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: Cantiga GMCH(3/7)-DDR

Size	Document Number	Rev
B	KAL90	0.1

Date: Monday, April 27, 2009 Sheet 9 of 53



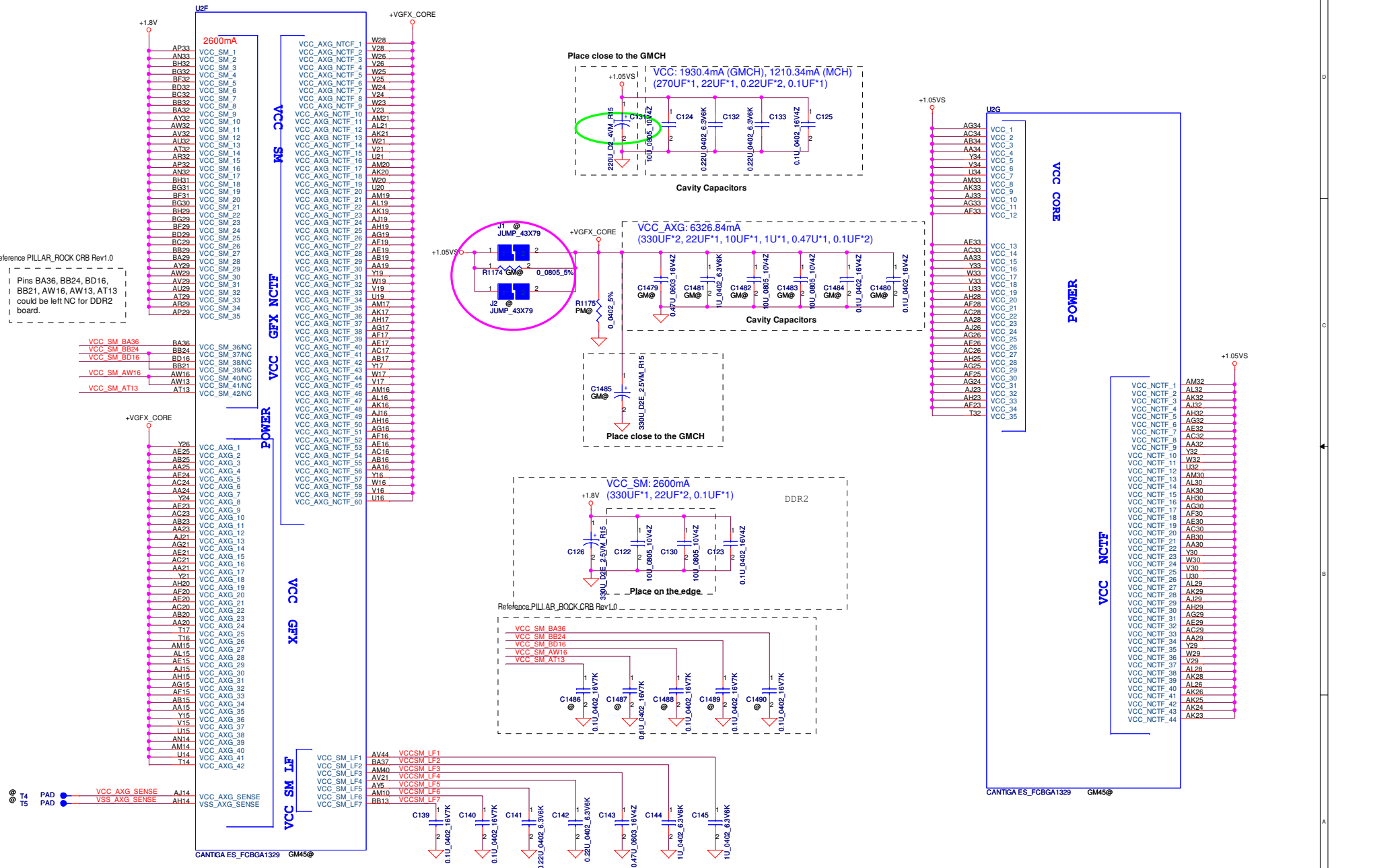
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Cantiga GMCH(4/7)-VGA/LVDS/TV

Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 Sheet 10 of 53



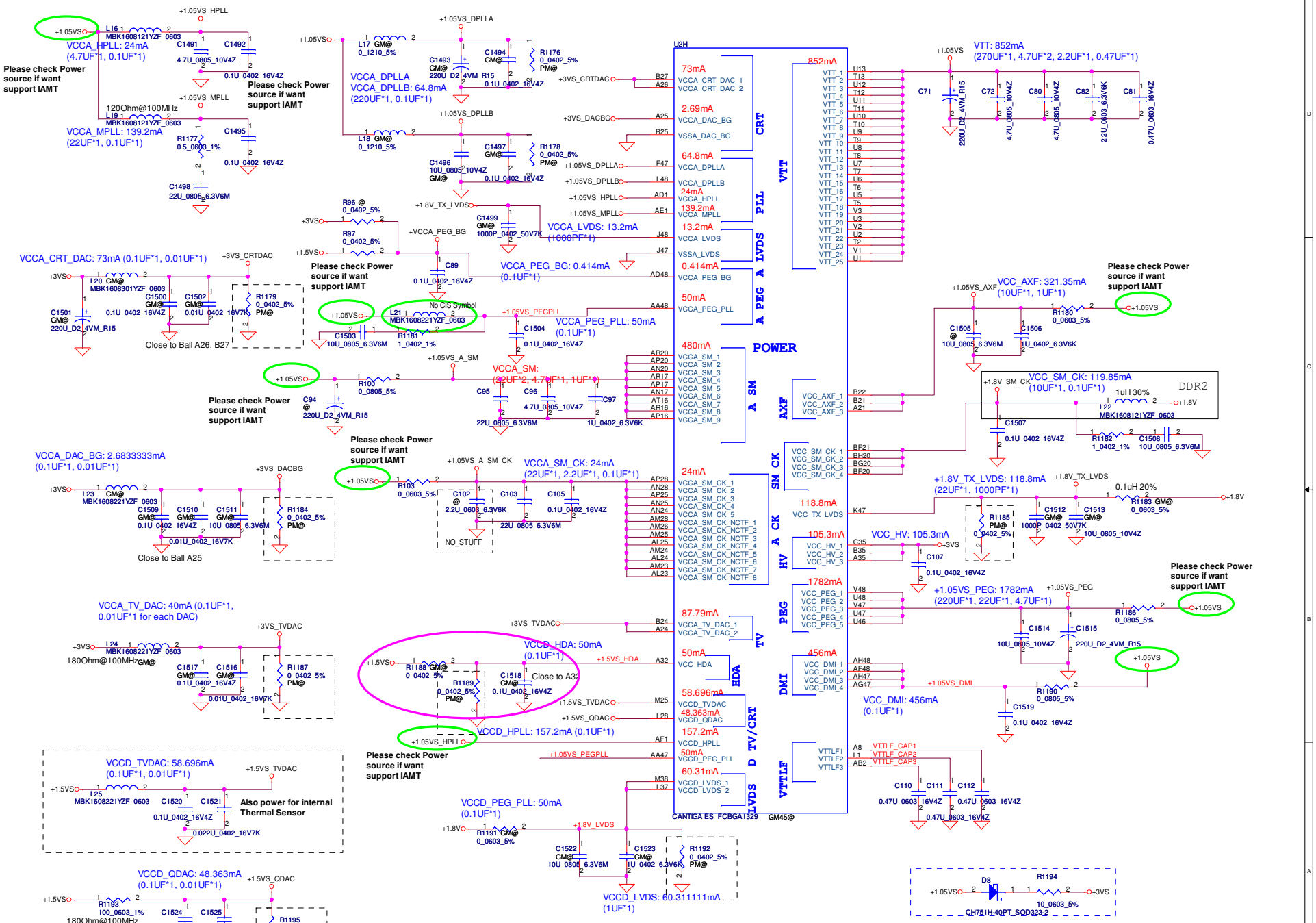
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

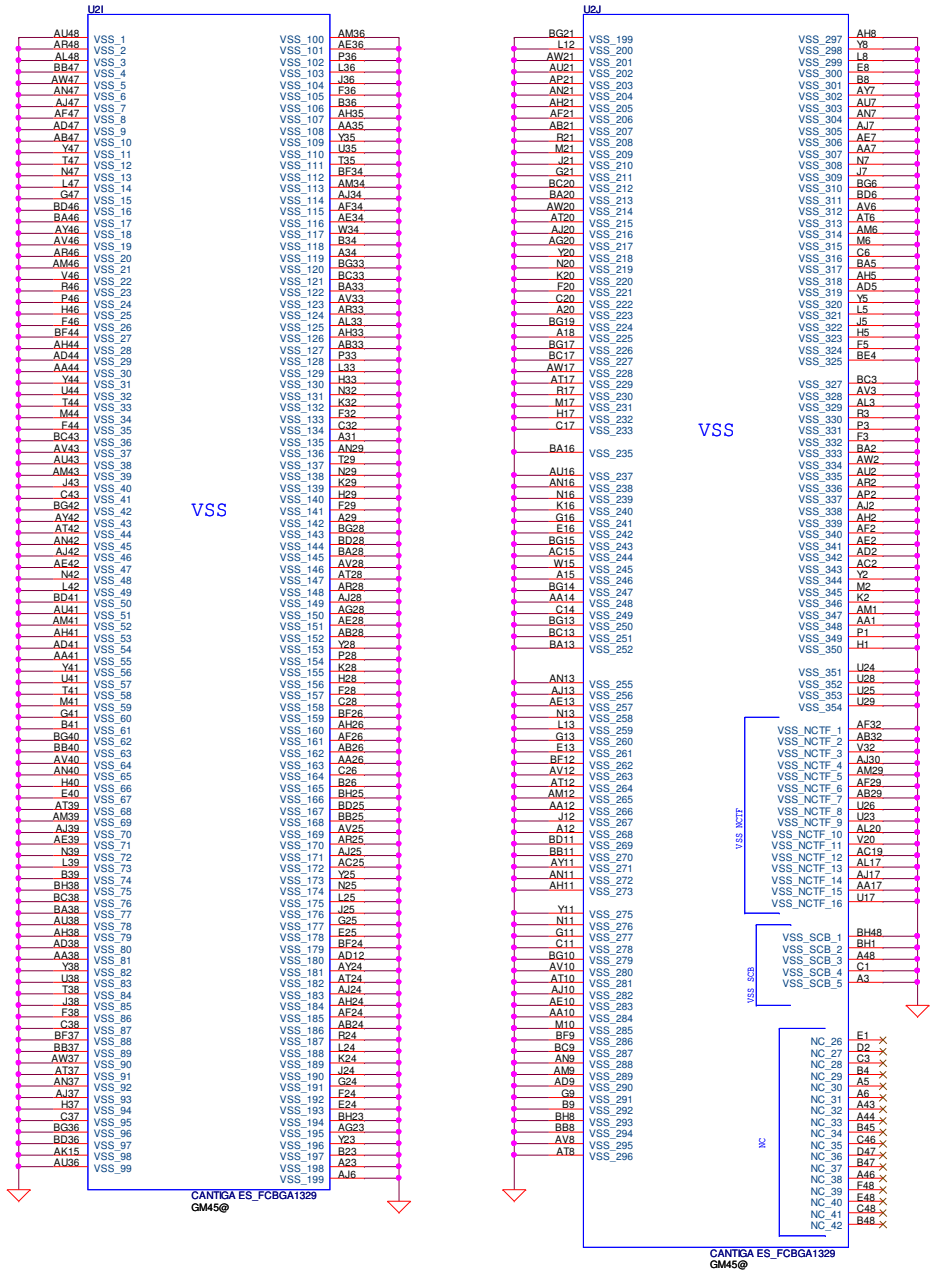
Compal Electronics, Inc.

Title: Cantiga GMCH(5/7)-VCC

Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 11 of 53


VCCA_HPLL: 24mA (4.7UF*1, 0.1UF*1)
VCCA_MPLL: 139.2mA (22UF*1, 0.1UF*1)
VCCA_DPLLA VCCA_DPLLB: 64.8mA (220UF*1, 0.1UF*1)
VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
VCCA_LVDS: 13.2mA (1000PF*1)
VCCA_PEG_BG: 0.414mA (0.1UF*1)
VCCA_PEG_PLL: 50mA (0.1UF*1)
VCCA_SM: (22UF*2, 4.7UF*1, 1UF*1)
VCCA_SM_CK: 24mA (22UF*1, 2.2UF*1, 0.1UF*1)
VCCA_DAC_BG: 2.6833333mA (0.1UF*1, 0.01UF*1)
VCCA_TV_DAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)
VCCD_HDA: 50mA (0.1UF*1)
VCCD_HPLL: 157.2mA (0.1UF*1)
VCCD_TVDAC: 58.696mA (0.1UF*1, 0.01UF*1)
VCCD_QDAC: 48.363mA (0.1UF*1, 0.01UF*1)
VCCD_PEG_PLL: 50mA (0.1UF*1)
VCCD_LVDS: 60.311111mA (1UF*1)
VTT: 852mA (270UF*1, 4.7UF*2, 2.2UF*1, 0.47UF*1)
VCC_AXF: 321.35mA (10UF*1, 1UF*1)
VCC_SM_CK: 119.85mA (10UF*1, 0.1UF*1)
+1.8V_TX_LVDS: 118.8mA (22UF*1, 1000PF*1)
VCC_HV: 105.3mA (0.1UF*1)
+1.05VS_PEG: 1782mA (220UF*1, 22UF*1, 4.7UF*1)
VCC_DMI: 456mA (0.1UF*1)
Please check Power source if want support IAMT
Close to Ball A26, B27
Close to Ball A25
NO_STUFF
No CIS Symbol
Also power for internal Thermal Sensor
U2H
CANTIGA ES_FCBGA1329 GM45@
CRT
PLL
LVDS
PEG
SM
SM_CK
HV
DMI
TV
HDA
TV/CRT
VTTLF
POWER
DDR2
Security Classification
Compal Secret Data
Issued Date
2008/11/24
Deciphered Date
2009/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
Crestline GMCH (6/7)-VCC
Size
Document Number
KALH0/KALG0/KAL90+
Rev
1.0
Date: Monday, April 27, 2009
Sheet 12 of 53



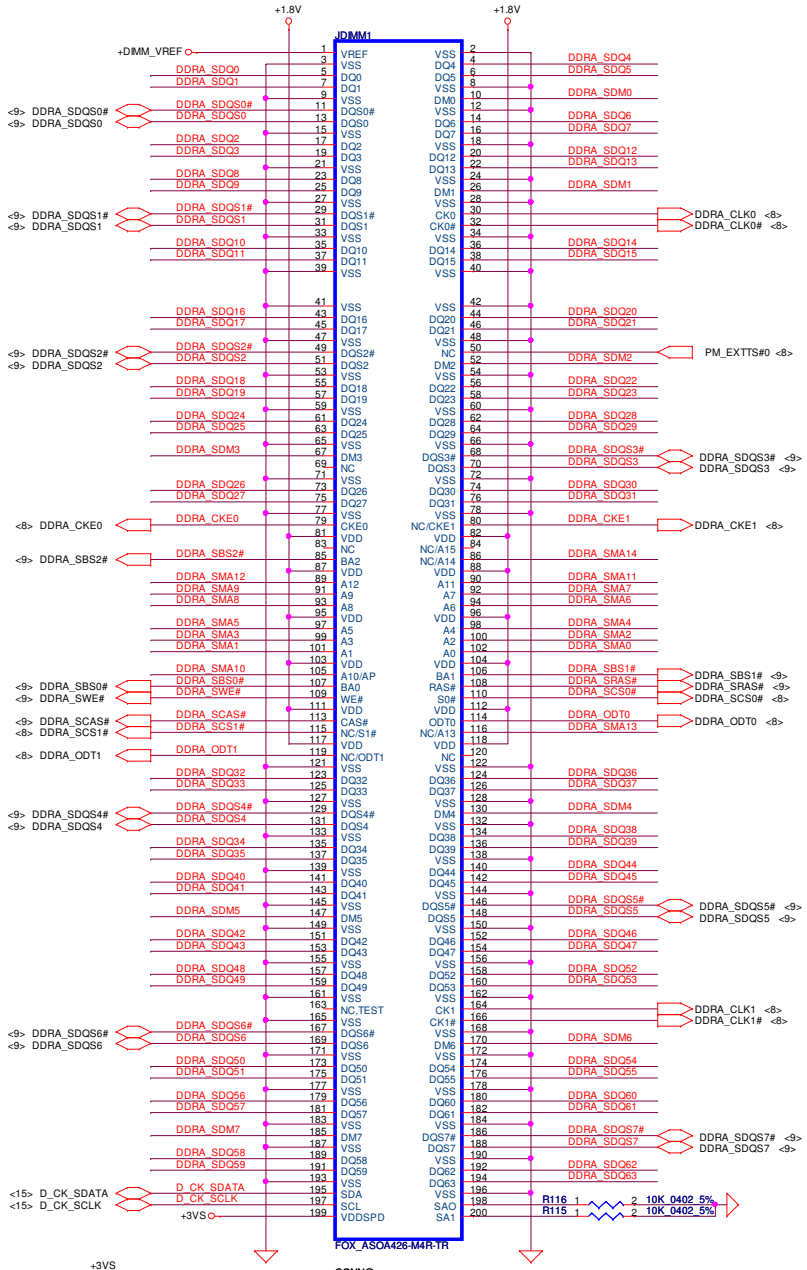
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Cantiga GMCH(1/7)-GTL

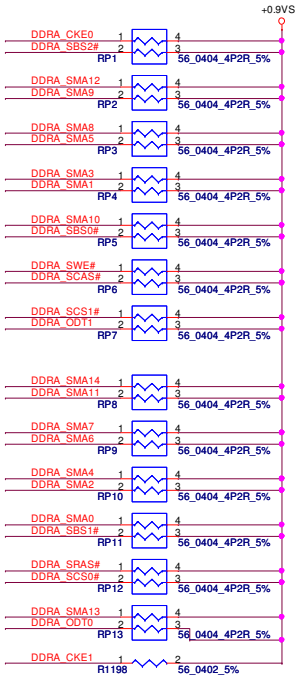
Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

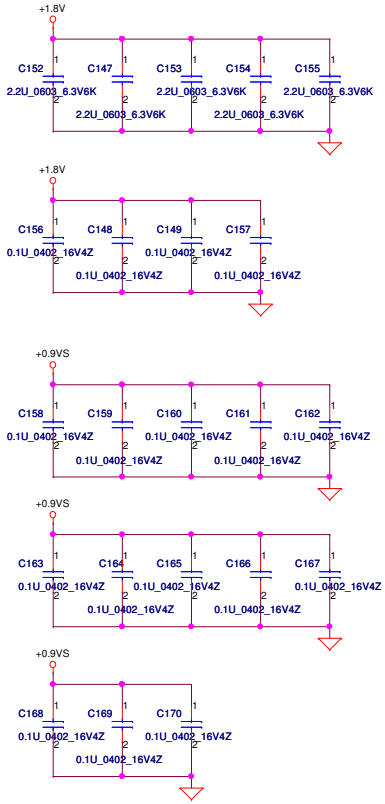
Date: Monday, April 27, 2009 | Sheet 13 of 53



DIMM1 REV H:5.6mm (BOT)

<9> DDRA_SMA[0..14] DDRA_SMA[0..14]
<9> DDRA_SDQ[0..63] DDRA_SDQ[0..63]
<9> DDRA_SDM[0..7] DDRA_SDM[0..7]





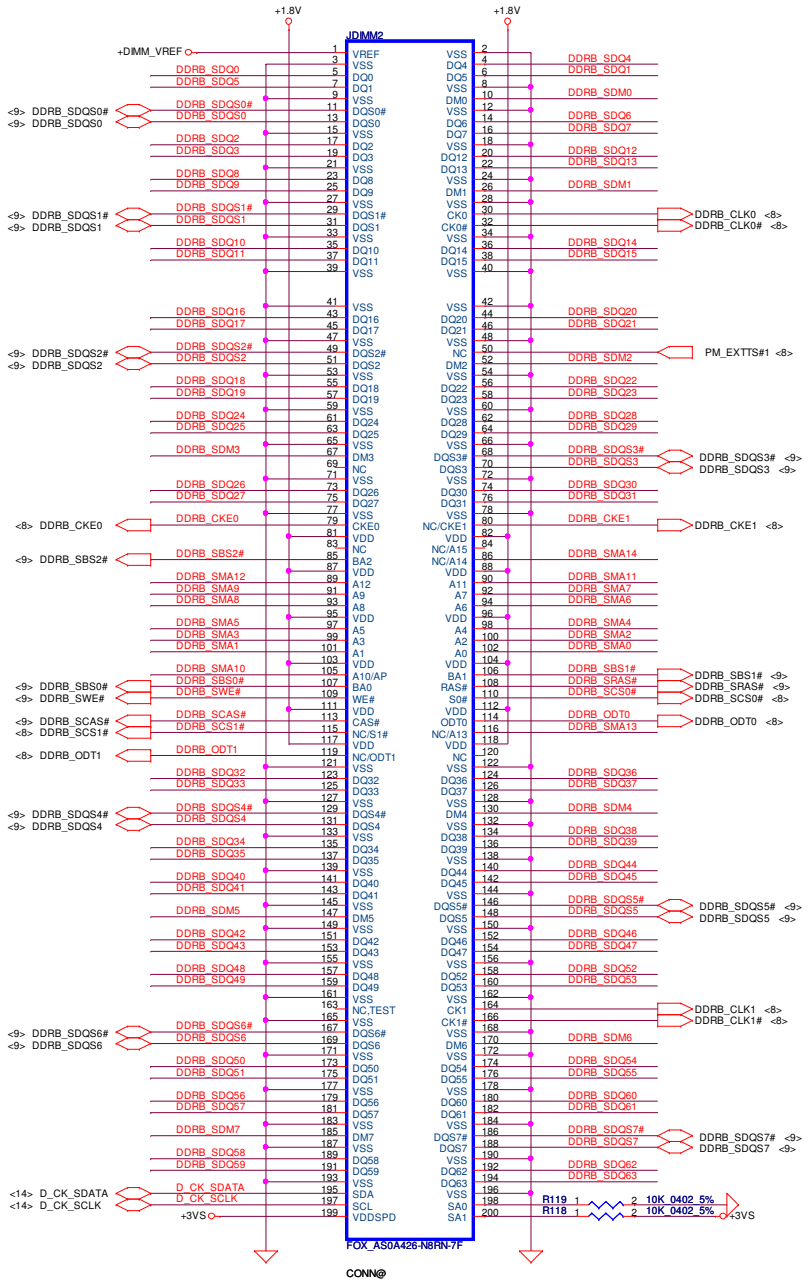
Security Classification	Compal Secret Data		
Issued Date	2008/03/28	Deciphered Date	2008/09/20

Compal Electronics, Inc.

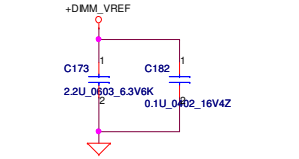
Title: DDRII-SODIMM0

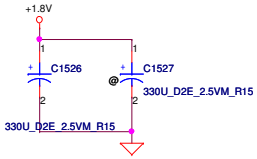
Size	Document Number	Rev
B	KAL90	0.1

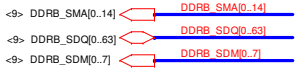
Date: Monday, April 27, 2009 Sheet 14 of 53

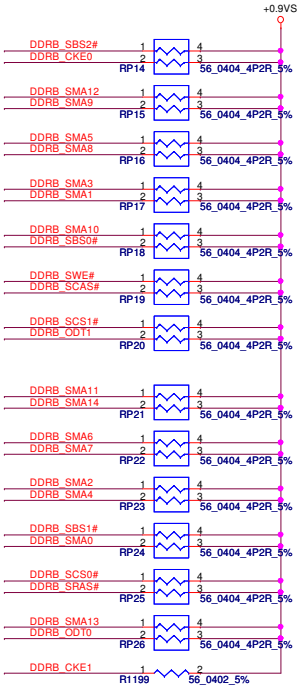


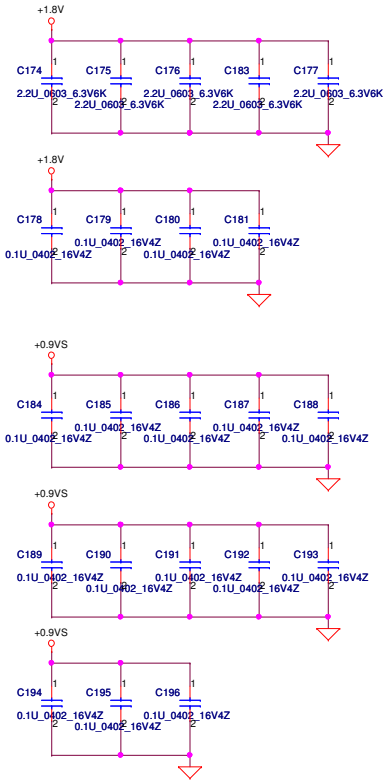
DIMM2 REV H:10.1mm (BOT)











Security Classification	Compal Secret Data		
Issued Date	2008/03/28	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: DDRII-SODIMM1

Size	Document Number	Rev
B	KAL90	0.1

Date: Monday, April 27, 2009 | Sheet 15 of 53

Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)

mount to Enable ITP_CLK

CLK_PCI5=0, Pin63,64 is SRC_CLK
CLK_PCI5=1, Pin63,64 is ITP_CLK

CLK_PCI4=0, Pin28, 29 is SRC_CLK
Pin24, 25 is DOT96_CLK

For EMI 10/9

Must Close to CLKGEN PIN 28,29

U43
ICS9LPRS387, PN:SA000020H10
SLG8SP556V, PN:SA000020K00

VGA: disable this pair by BIOS

VGA: disable this pair by BIOS

UMA: disable this pair by BIOS

ICS9LPRS387BKLFT_MLF72_10x10

Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

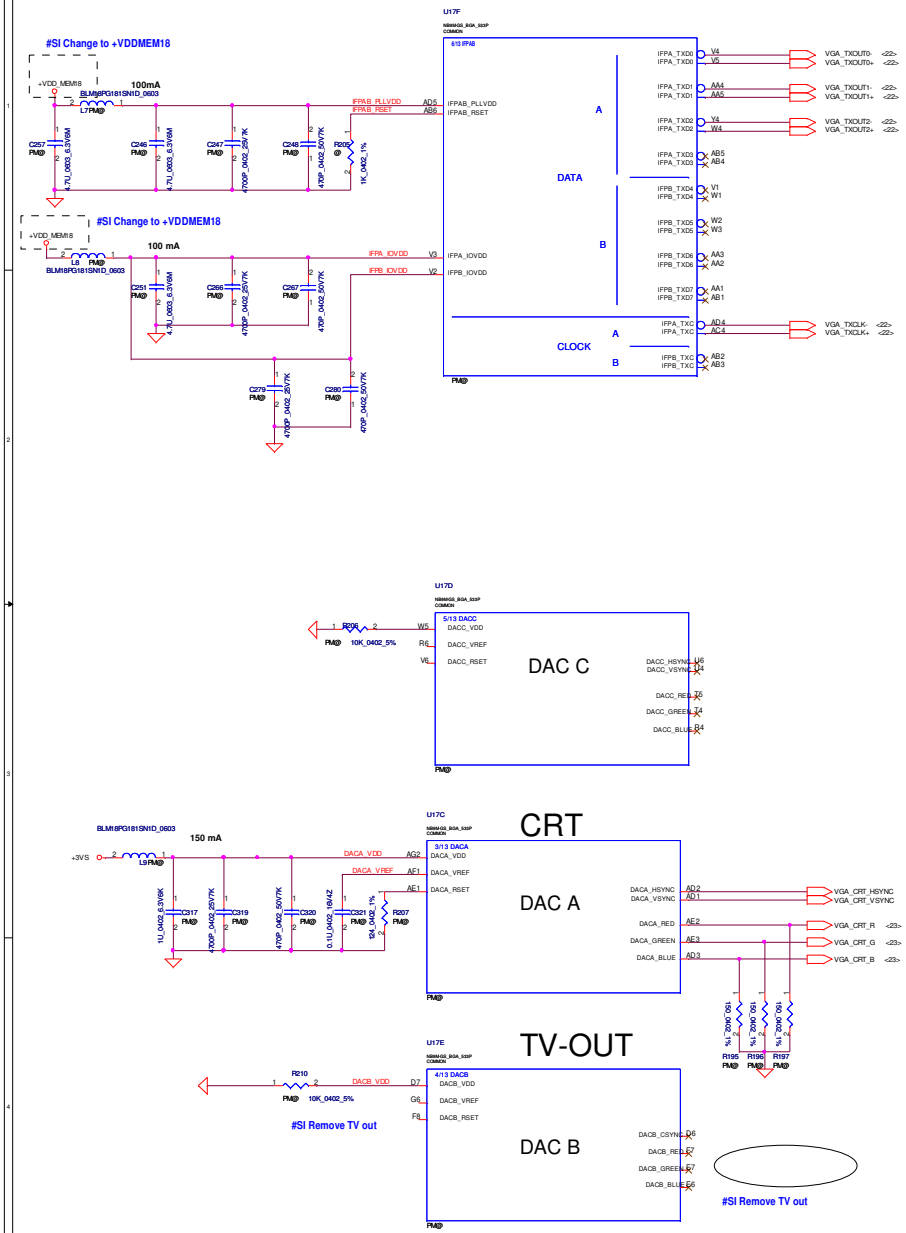
Compal Electronics, Inc.

Title: Clock Generator (CK505)

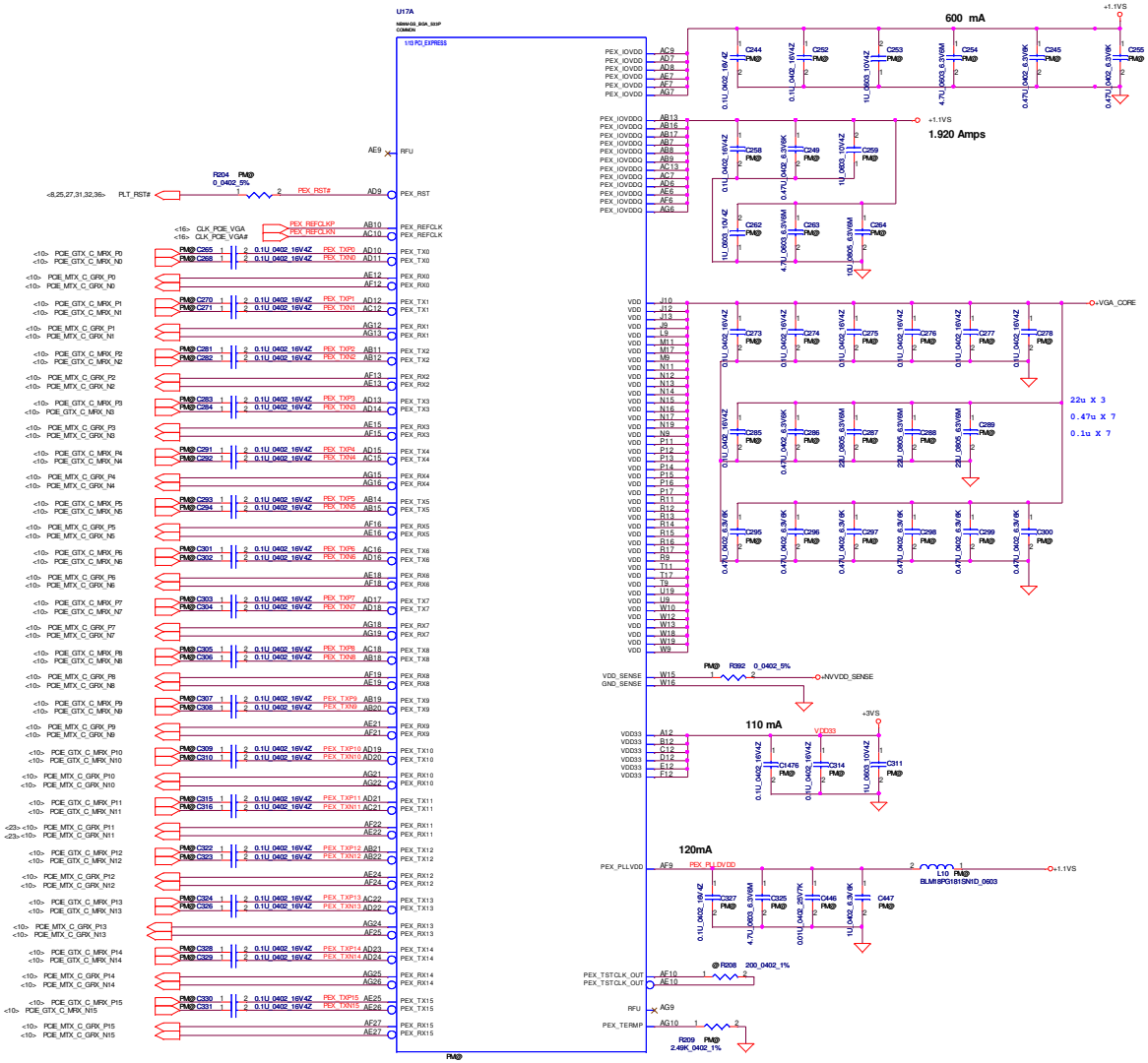
Size: Custom | Document Number: KALH0/KALG0/KAL90+ | Rev: 1.0

Date: Monday, April 27, 2009 | Sheet 16 of 53

LVDS & DAC Interface

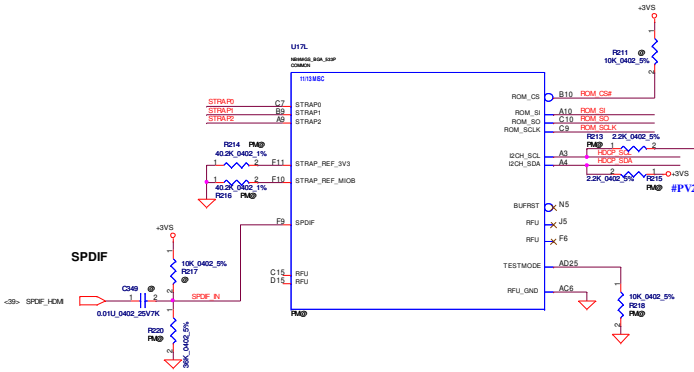


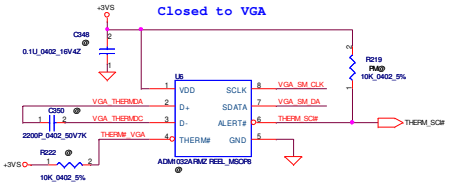
PEG Interface

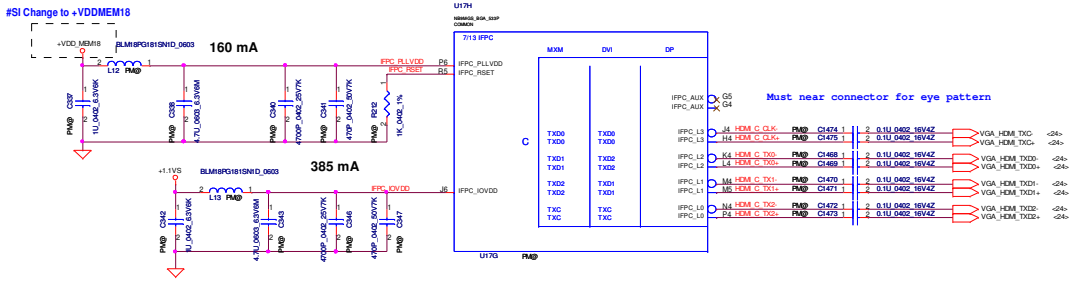


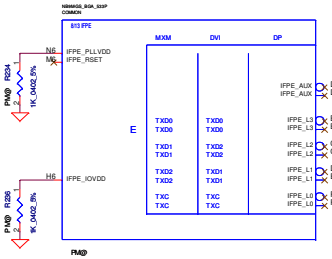
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

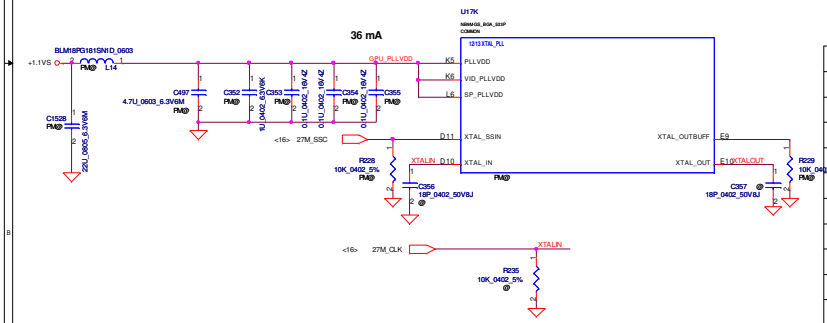
Compal Electronics, Inc.			
Title	PEG & LVDS & DAC		
Size: Custom	Document Number: KALH9/KALG9/KAL90+		Rev: 1.0
Date: Monday, April 27, 2009	Sheet 17 of 53		



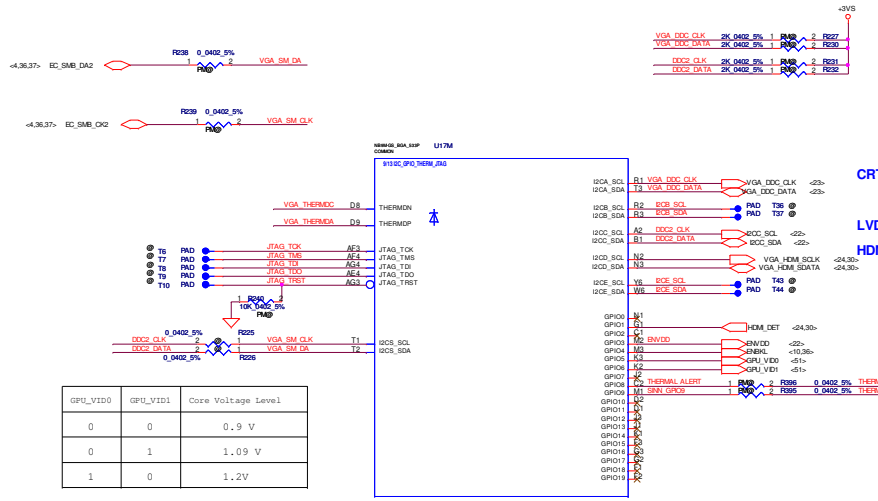




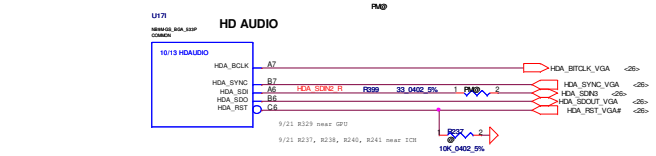




GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control

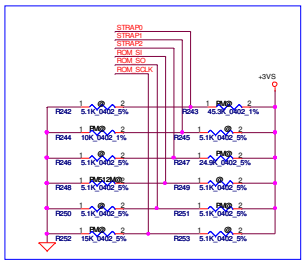


GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.9 V
0	1	1.09 V
1	0	1.2V



Straps

MULTI LEVEL STRAPS



DDR2

Locating
16MX16 Hynix
16MX16 Samsung
32MX16 Hynix
32MX16 Samsung
64MX16 Samsung
64MX16 Hynix

Resistor Value
R248
20 Kohms
10 Kohms
45 Kohms
30 Kohms
10 Kohms
5.1 Kohms

Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

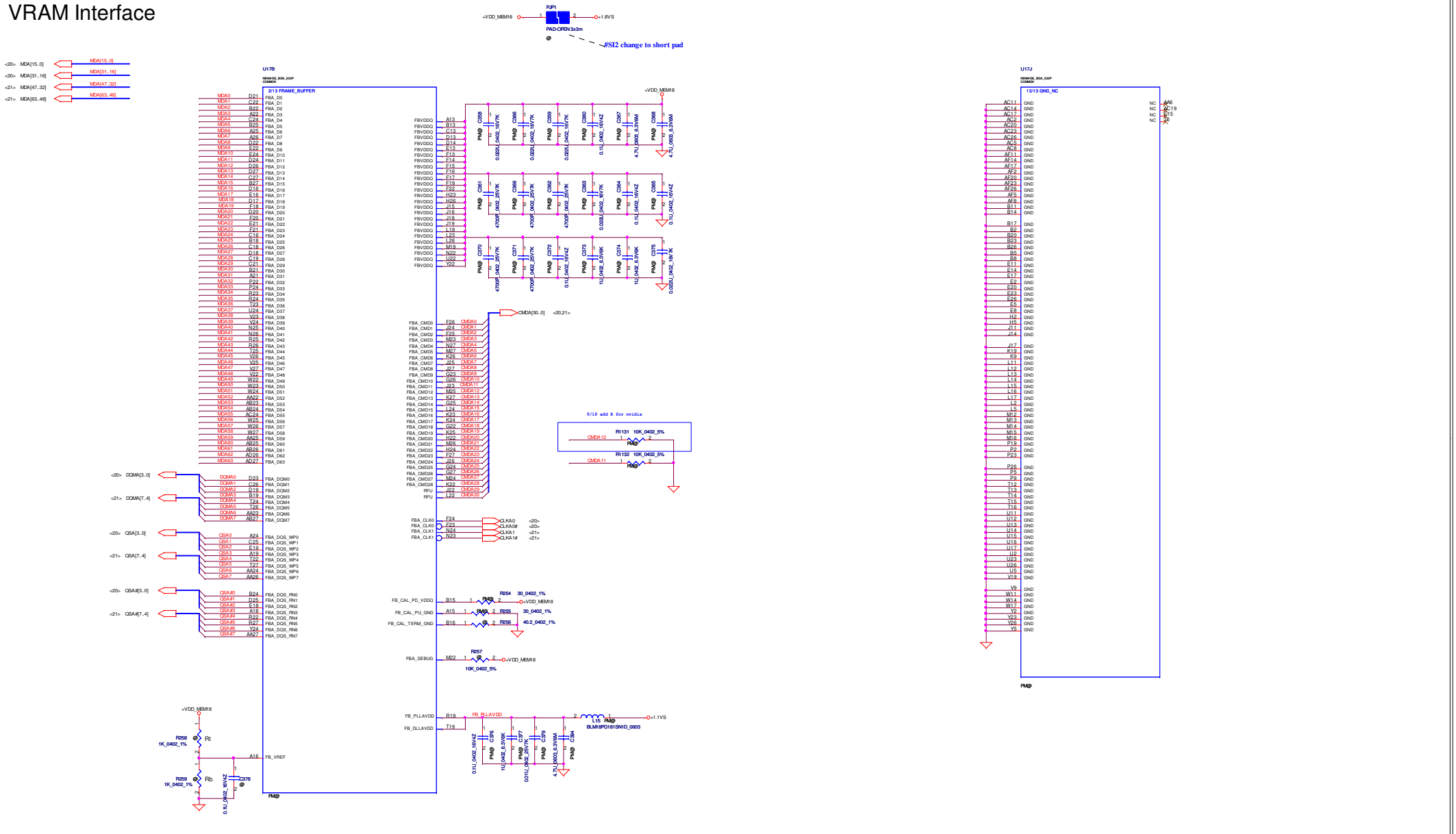
Compal Electronics, Inc.

Title: **Straps & HDMI**

Size	Document Number	Rev
Custom	KALH00/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 18 of 53

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: **VRAM / GND**

Size	Document Number	Rev
Custom	KALH9/KALG9/KAL90+	1.0

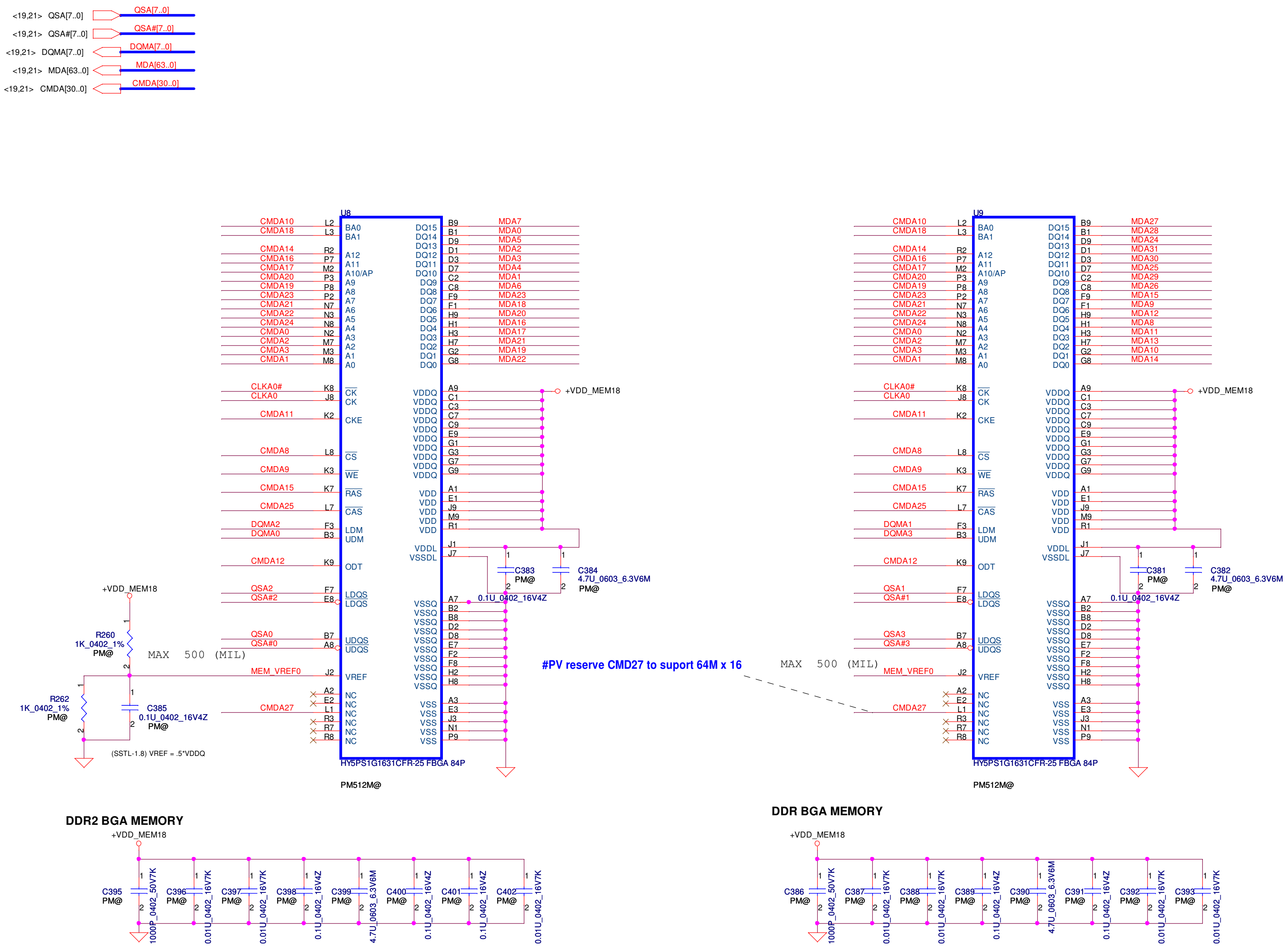
Date: Monday, April 27, 2009 Sheet 19 of 53

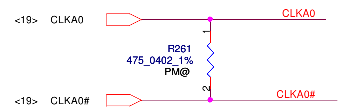
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

64Mx16 DDR2 400MHz*4==>512MB

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		





Compal Electronics, Inc.

Title: VRAM 1

Size | Document Number: KAL90 | Rev 0.1

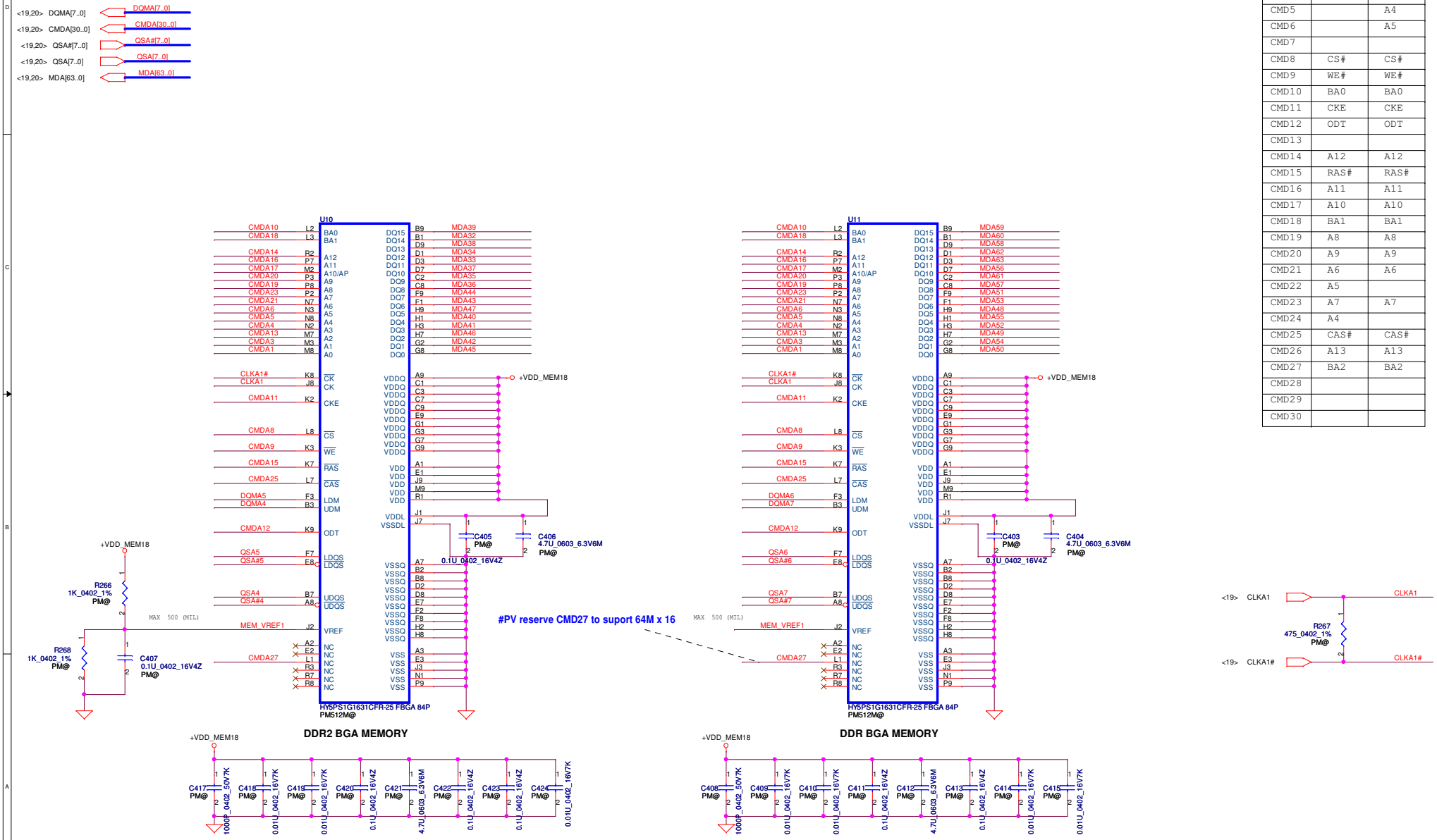
Date: Monday, April 27, 2009 | Sheet 7 of 16

VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

64Mx16 DDR2 400MHz*4==>512MB

	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



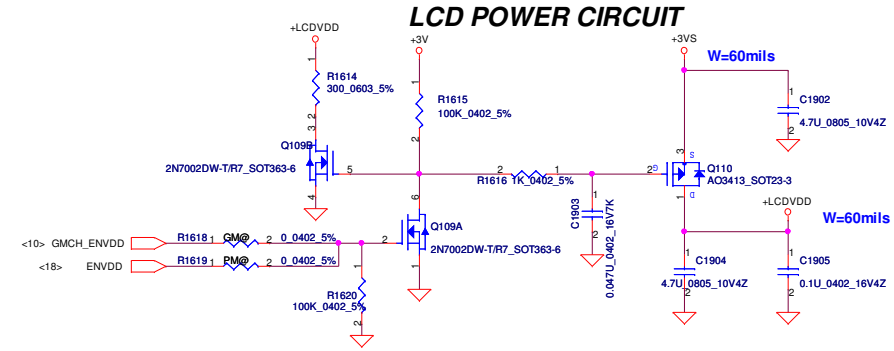
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

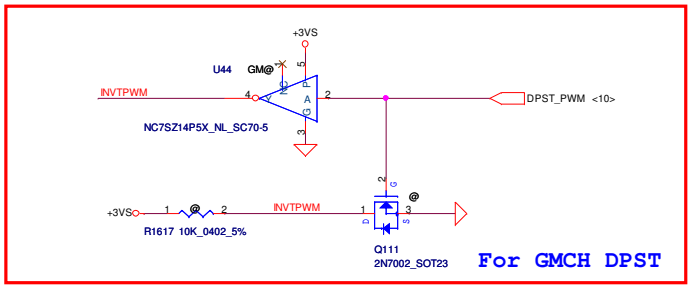
Compal Electronics, Inc.

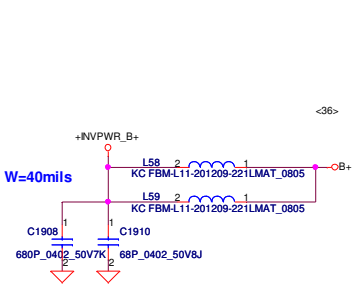
Title: **VRAM 2**

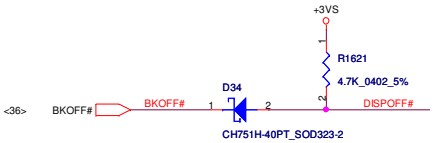
Size: | Document Number: **KAL90** | Rev: 0.1

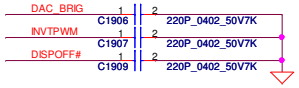
Date: Monday, April 27, 2009 | Sheet 8 of 16

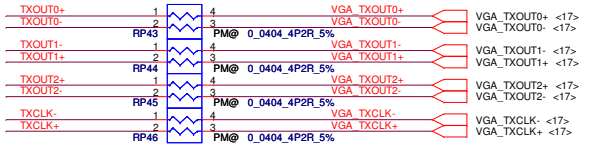


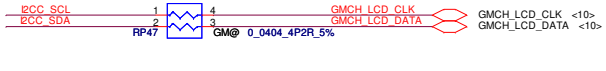


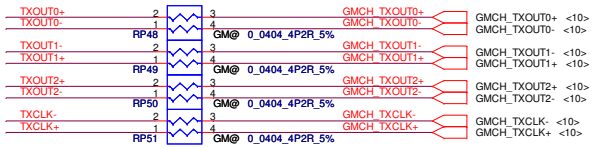




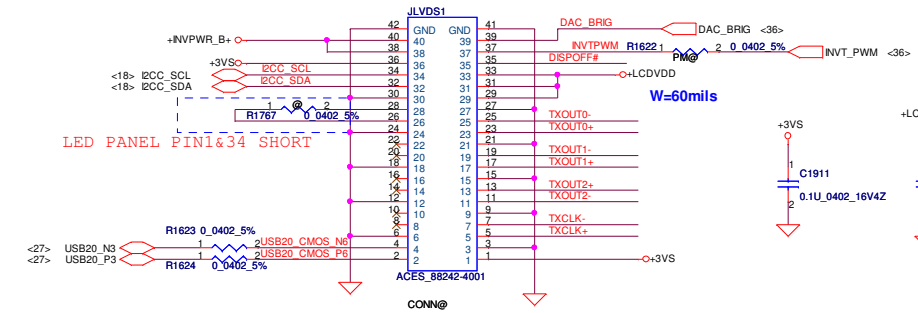


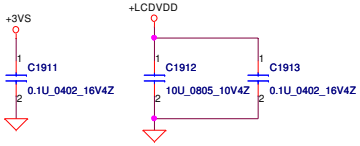






LCD/PANEL BD. Conn.





Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

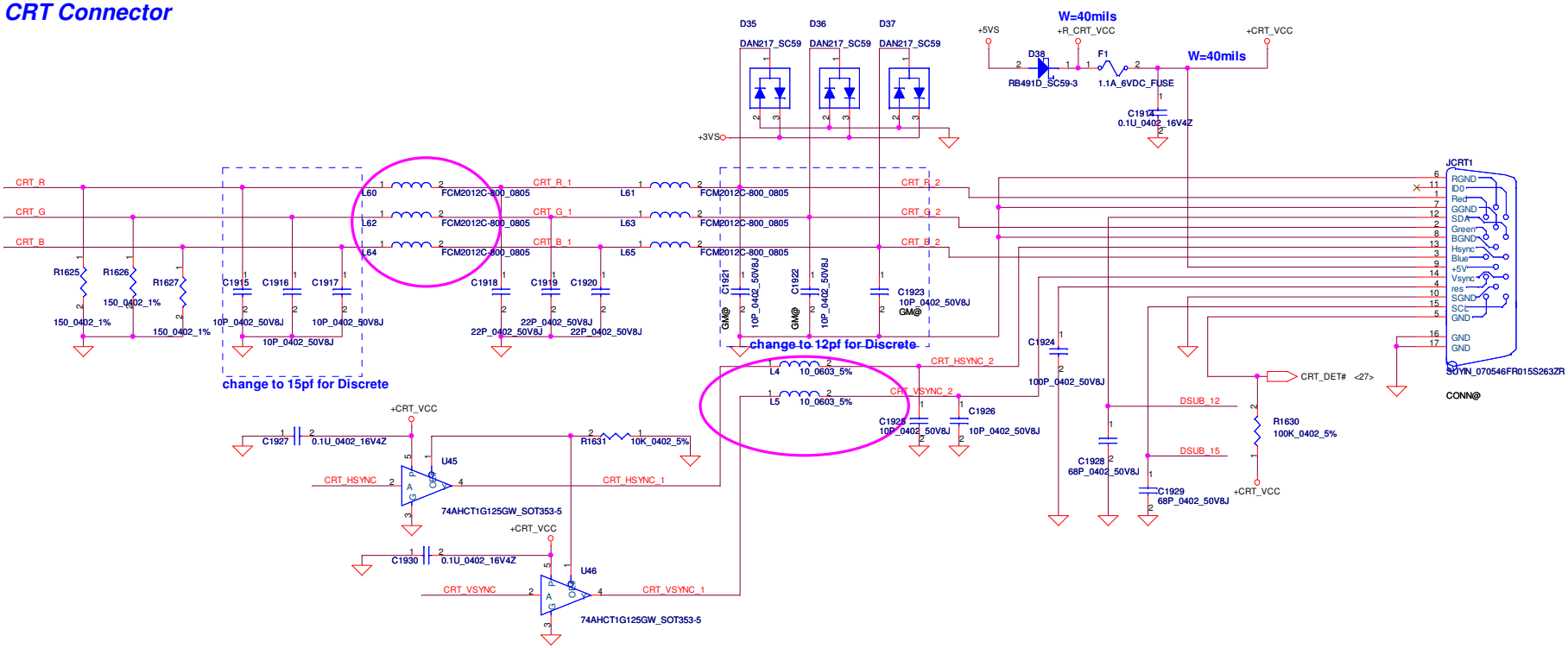
Compal Electronics, Inc.

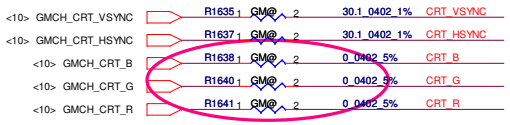
Title: LVDS Connector

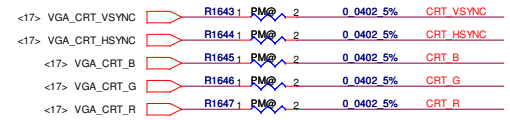
Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

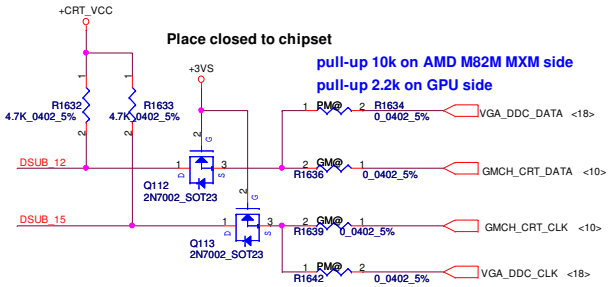
Date: Monday, April 27, 2009 | Sheet 22 of 53

CRT Connector









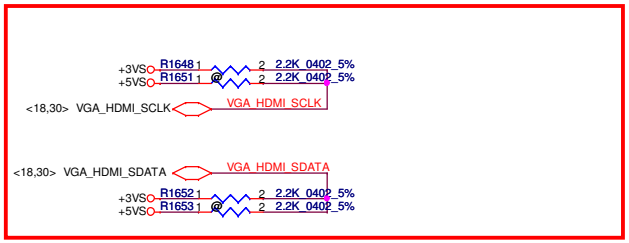
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

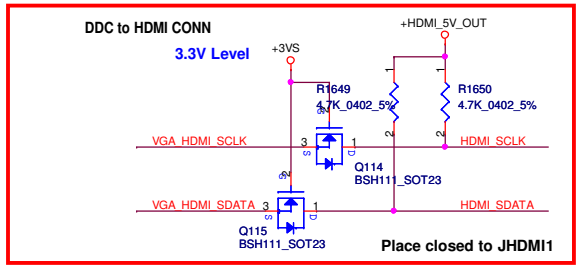
Compal Electronics, Inc.

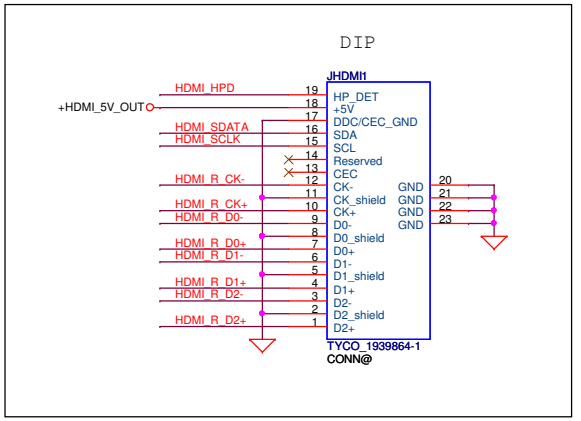
Title: CRT Connector

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

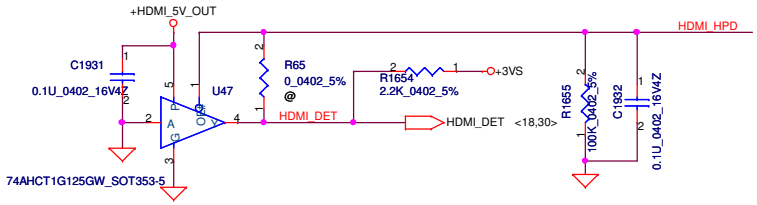
Date: Monday, April 27, 2009 | Sheet 23 of 53

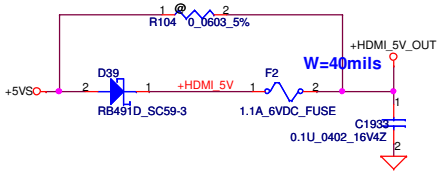


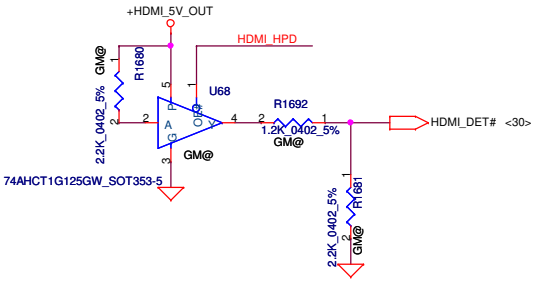


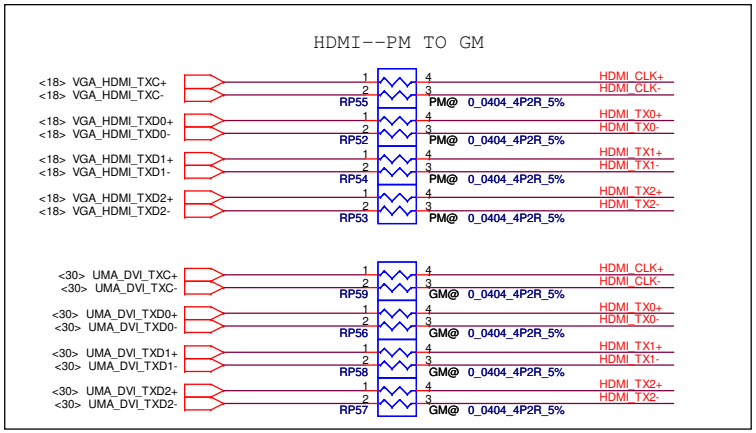


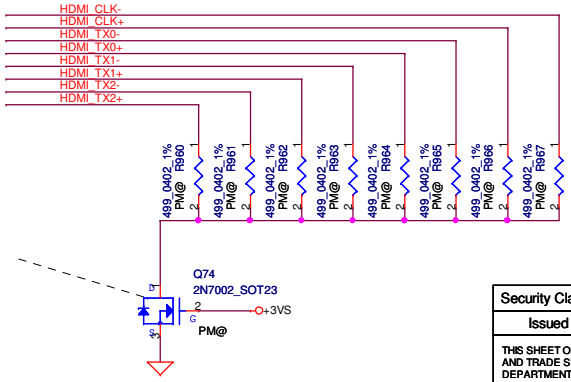
MP:Update HDMI Hot Plug DET circuit.

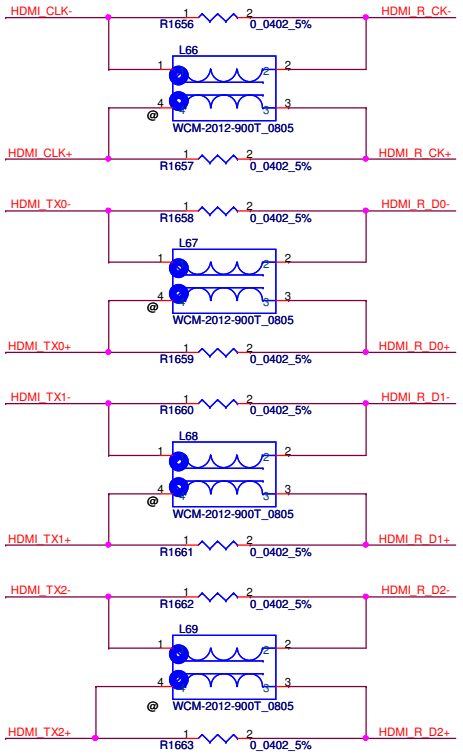












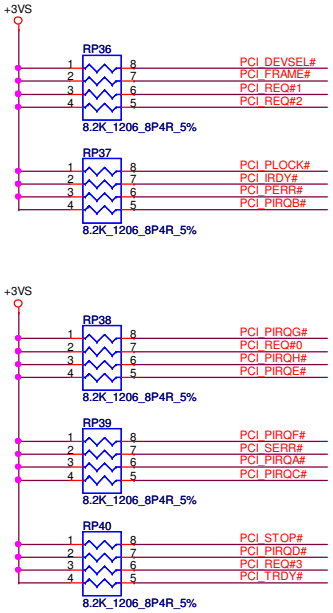
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

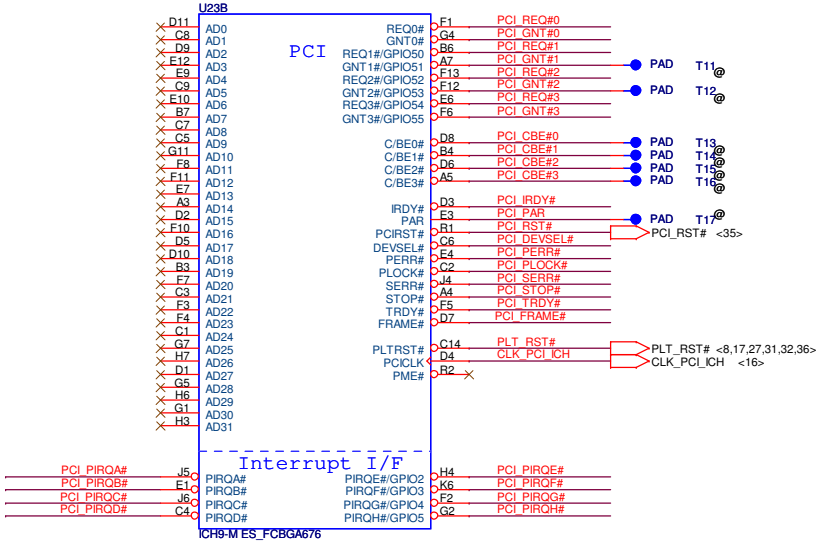
Title: HDMI Connector

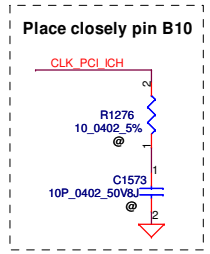
Size: Custom | Document Number: KALH0/KALG0/KAL90+ | Rev: 1.0

Date: Monday, April 27, 2009 | Sheet 24 of 53

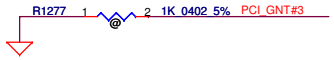


DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)

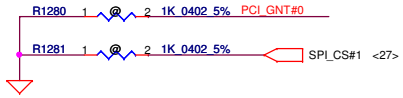


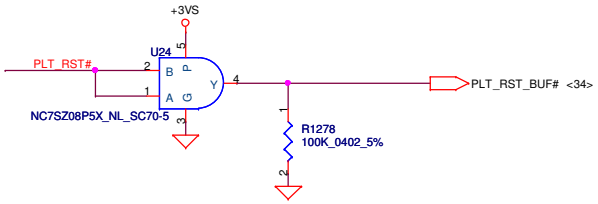


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*





Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.			
Title	ICH9M(1/4)-PCI		
Size	Document Number		Rev
	KALH0/KALG0/KAL90+		1.0
Date:	Monday, April 27, 2009	Sheet	25 of 53

CMOS Settings	R1290
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	R1291
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN

Reset r1290 for power on then shut down issue

High = Internal VR Enable

close to RAM door

close to RAM door

SATA for HDD

SATA for ODD

HDA for AUDIO

HDA for GMCH

HDA for VGA

close ICH9

10mils width less than 500mils

R258 need to place within 2" of ICH9M
R257 must be place within 2" of R258 w/o stub.

PROJECT_ID	ID0	ID1	ID2
KAL90	0	0	0
KAL90+	1	0	0
KALH0	0	1	0
KALG0	1	1	0

Flash Descriptor Security Override Strap

GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

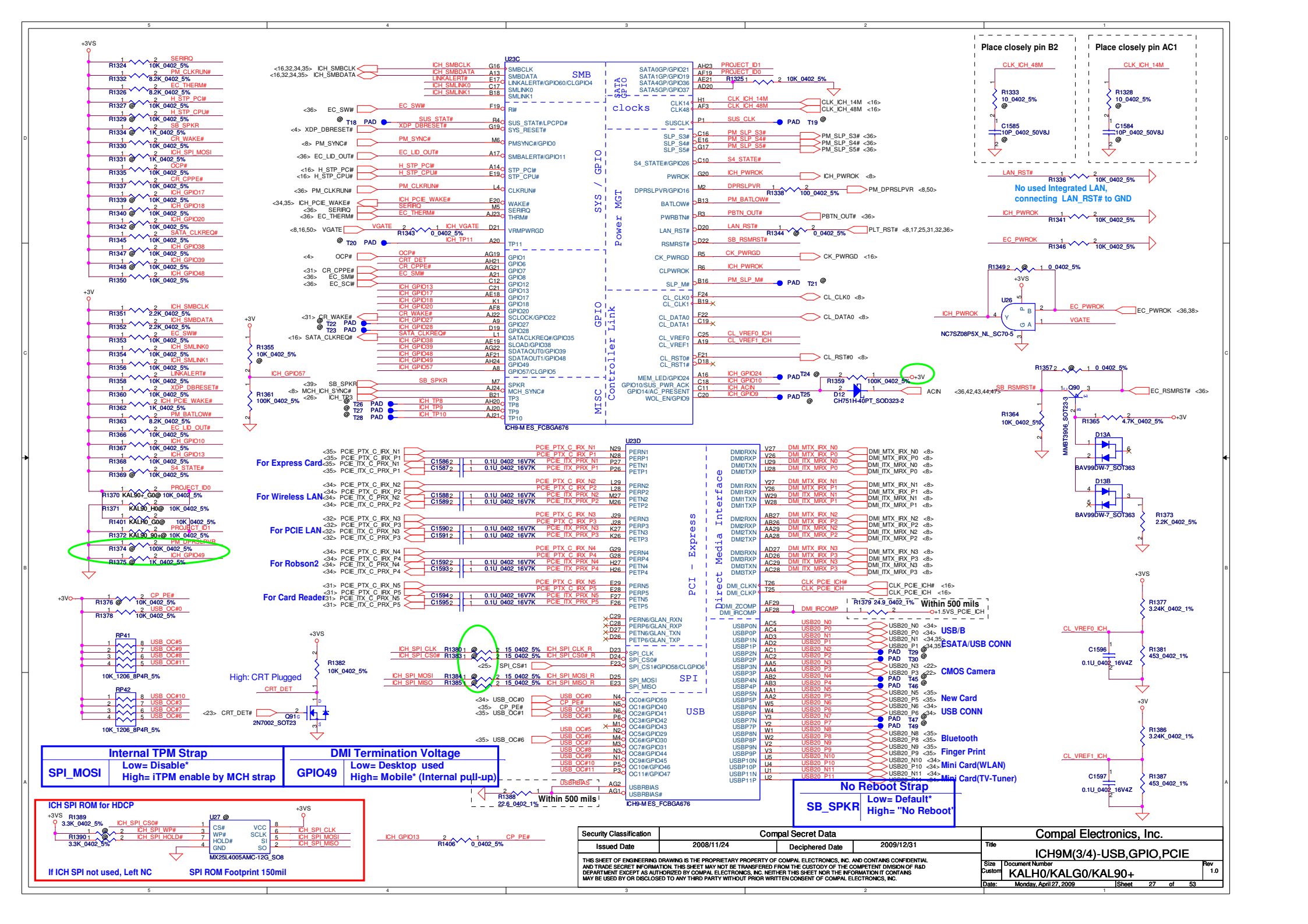
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KALH0/KALG0/KAL90+ | Rev: 1.0

Date: Monday, April 27, 2009 | Sheet 26 of 53



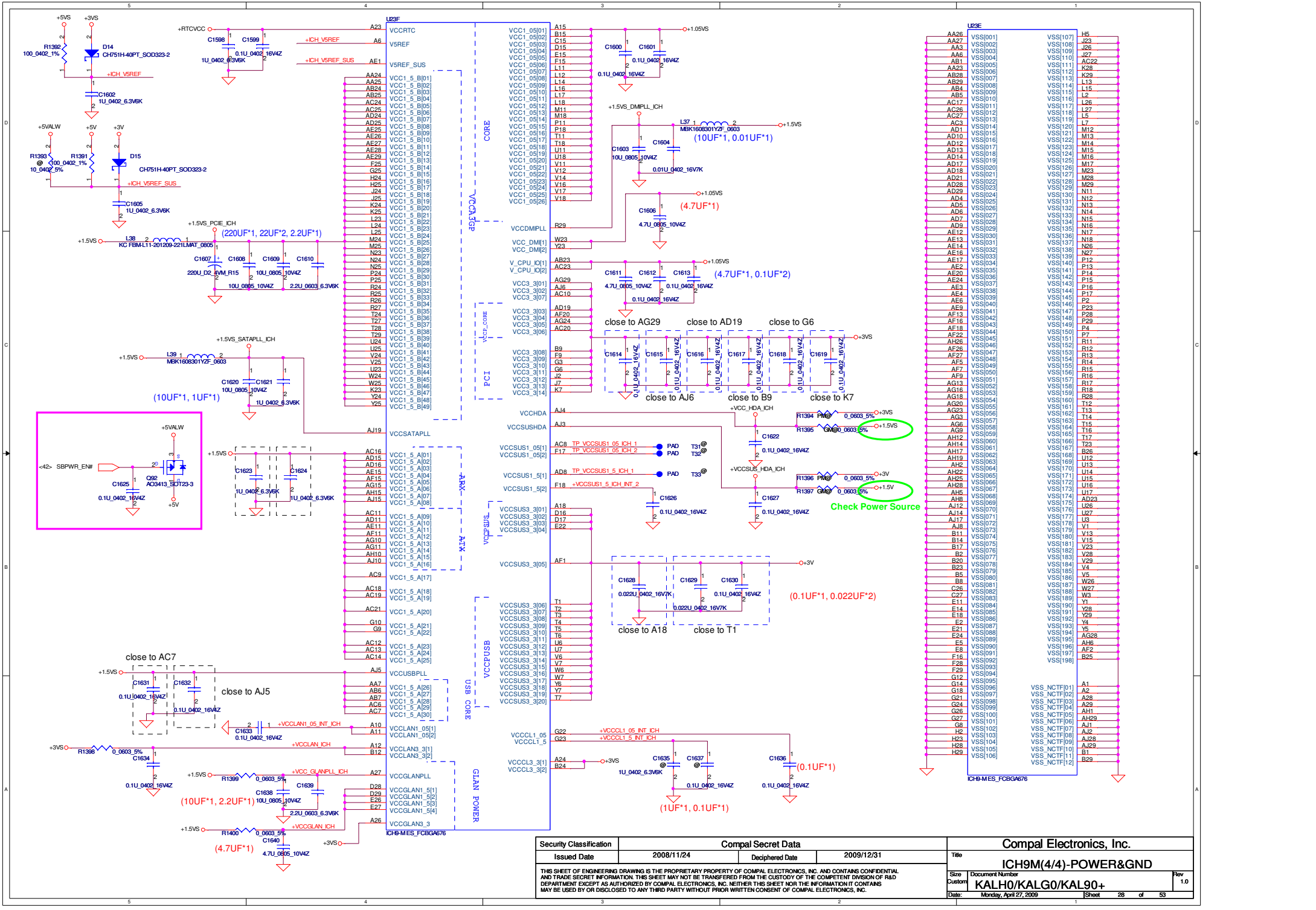
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size: Custom | Document Number: KALH0/KALG0/KAL90+ | Rev: 1.0

Date: Monday, April 27, 2009 | Sheet 27 of 53



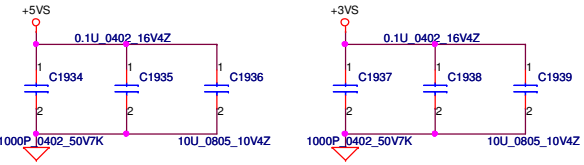
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

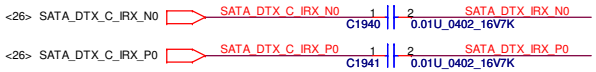
Title: ICH9M(4/4)-POWER&GND

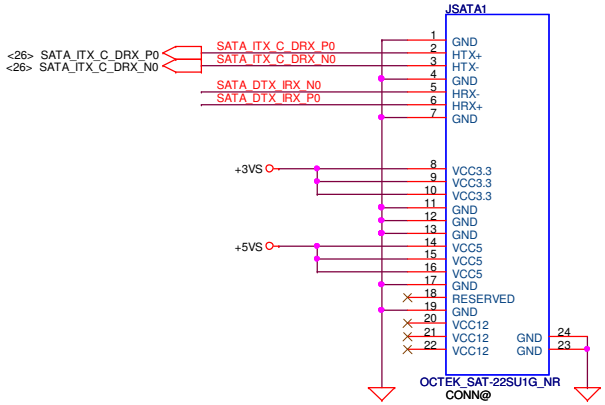
Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

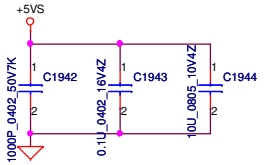
Date: Monday, April 27, 2009 | Sheet 28 of 53



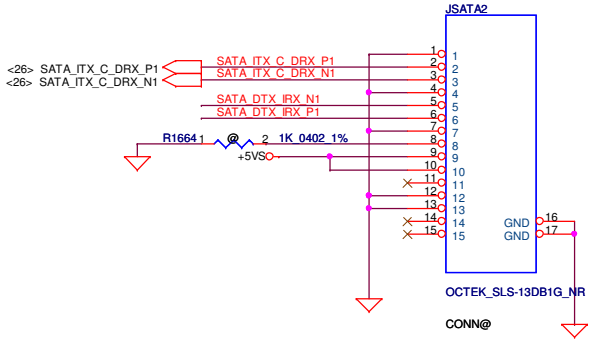
SATA HDD Conn.

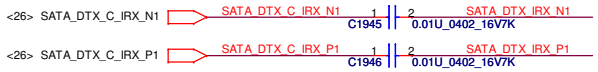






SATA ODD Conn.





Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 Sheet 29 of 53

20071029:
C1 (10U_0805) close to JP1.Pin 226, 228, 230

20071029:
C2, C3, C4, C5, C6, C7, C8 (0.1U_0402) close to U1 VCC (+3VS) pins (one Pin one Capacitor)

PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15] <10,17>
PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15] <10,17>

20071210:
R3 change to 0_0402_1%
(Old-10K)

20071210:
R6 change to 1K_0402_1%
(Old - 1.2K)

20071026:
Del R4 (0_0402_5%) for D_DVI_DET remove.

20071031:
Add U1. 49 (THERMAL_GND) to GND Plane

20071210:
R9~R12 change to 68_0402_5%
(Old - 6.8)

Trace AS Short PASSS

20080128_PVT (change to B version):
SA00001U900 (CH7318A-BF-TR)
SA00001U910 (CH7318B-BF-TR)

20080118 (JAL90_PVT):
Add R17 for Inverting Current

20071026:
C9,C10,C11,C12-
Change P/N to SA00000AU00 (0.5P_0402_50V8D)
20080130_PVT
C9,C10,C11,C12-
Change P/N to SE00000HA00 (0.5P 50V C NPO 0402)

Intel Cantiga TMDS Pin Definition

TMDS_B_CLK TMDS_B_CLK#	PEG_TXP_3 PEG_TXN_3
TMDS_B_DATA0 TMDS_B_DATA0#	PEG_TXP_2 PEG_TXN_2
TMDS_B_DATA1 TMDS_B_DATA1#	PEG_TXP_1 PEG_TXN_1
TMDS_B_DATA2 TMDS_B_DATA2#	PEG_TXP_0 PEG_TXN_0
TMDS_B_HPD#	PEG_RXP_3

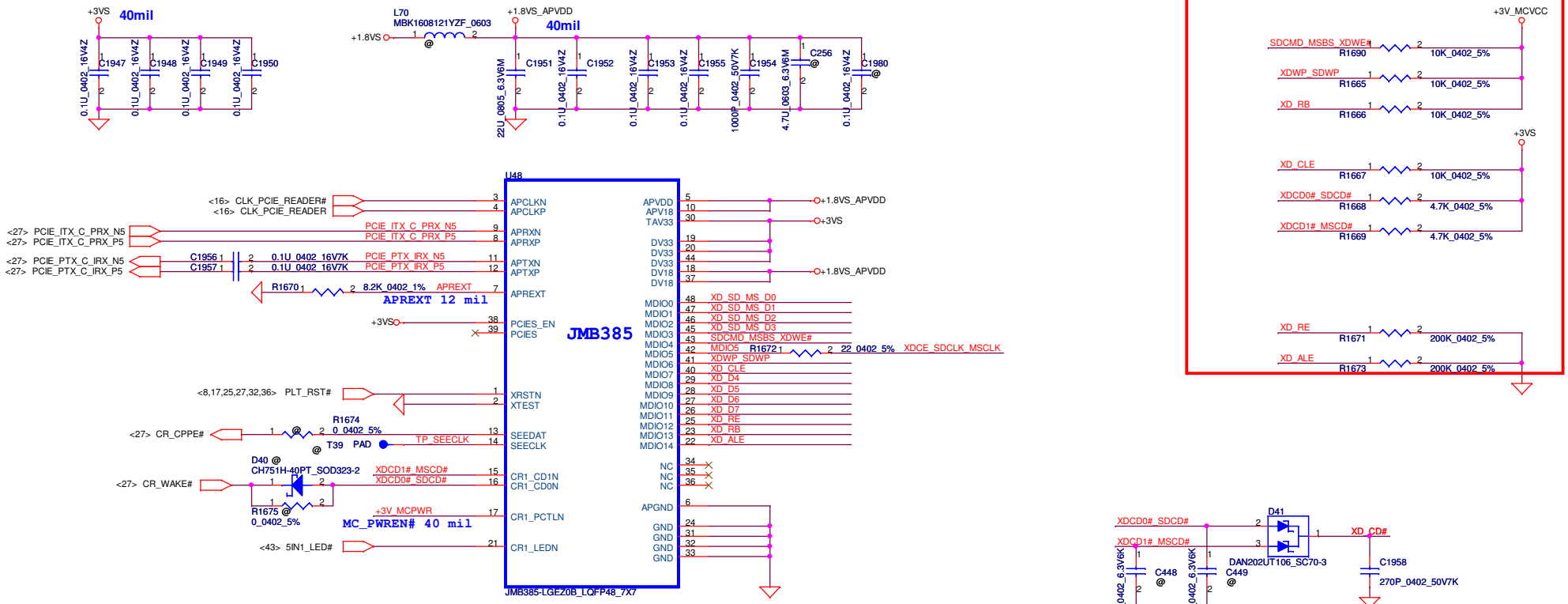
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: HDMI/DVI CH7318

Size: C | Document Number: KALH0/KALG0/KAL90+ | Rev: 1.0

Date: Monday, April 27, 2009 | Sheet 30 of 53



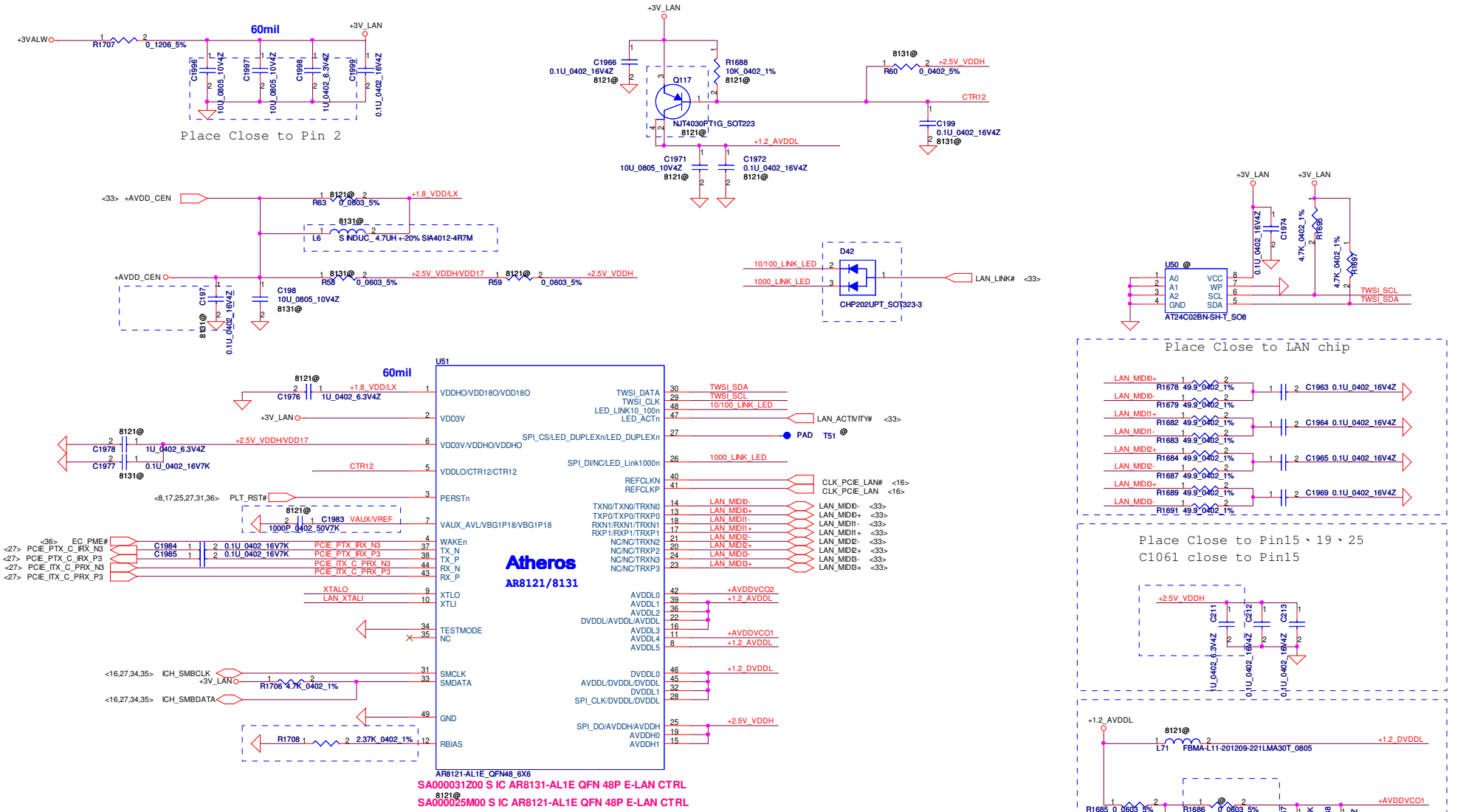
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Card Reader JMB385

Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 Sheet 31 of 53



Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

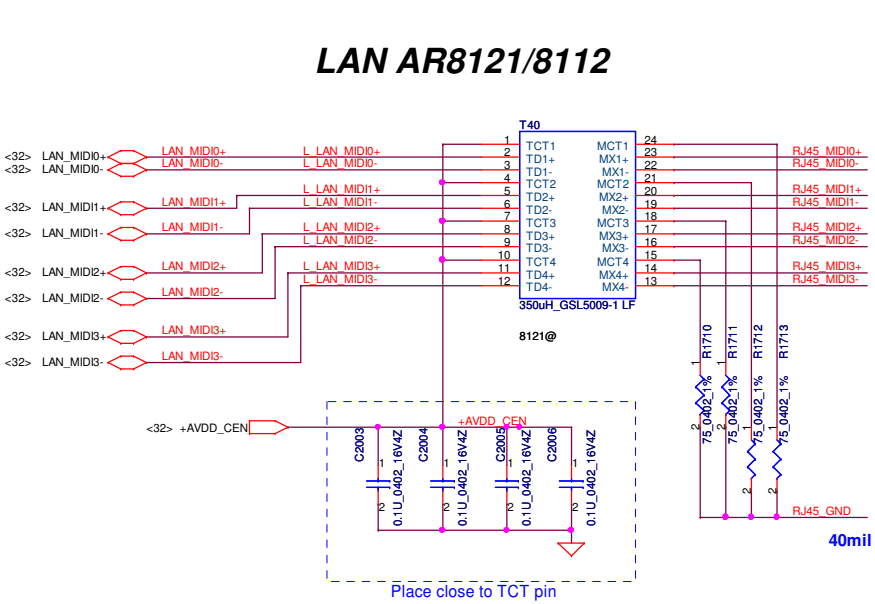
Compal Electronics, Inc.

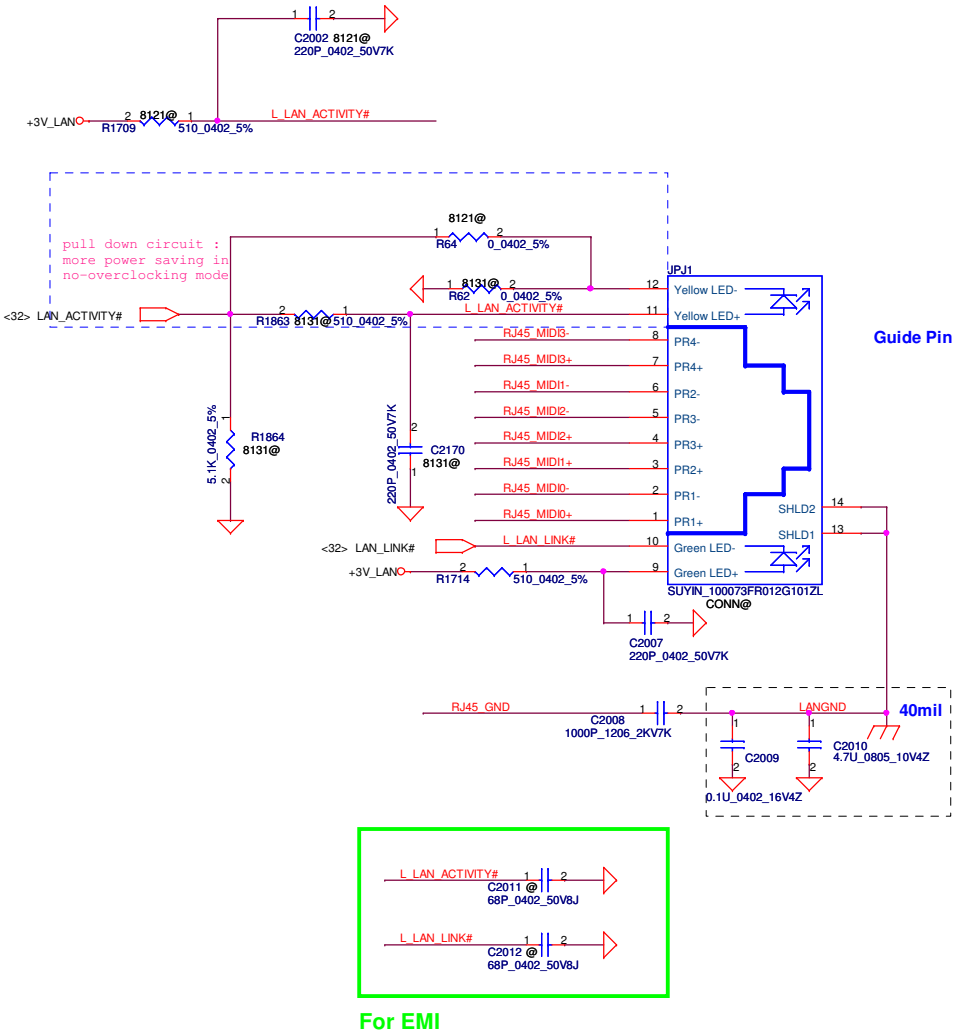
Title: Atheros AR8131

Size	Document Number	Rev
Custom	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 32 of 53

LAN AR8121/8112





Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

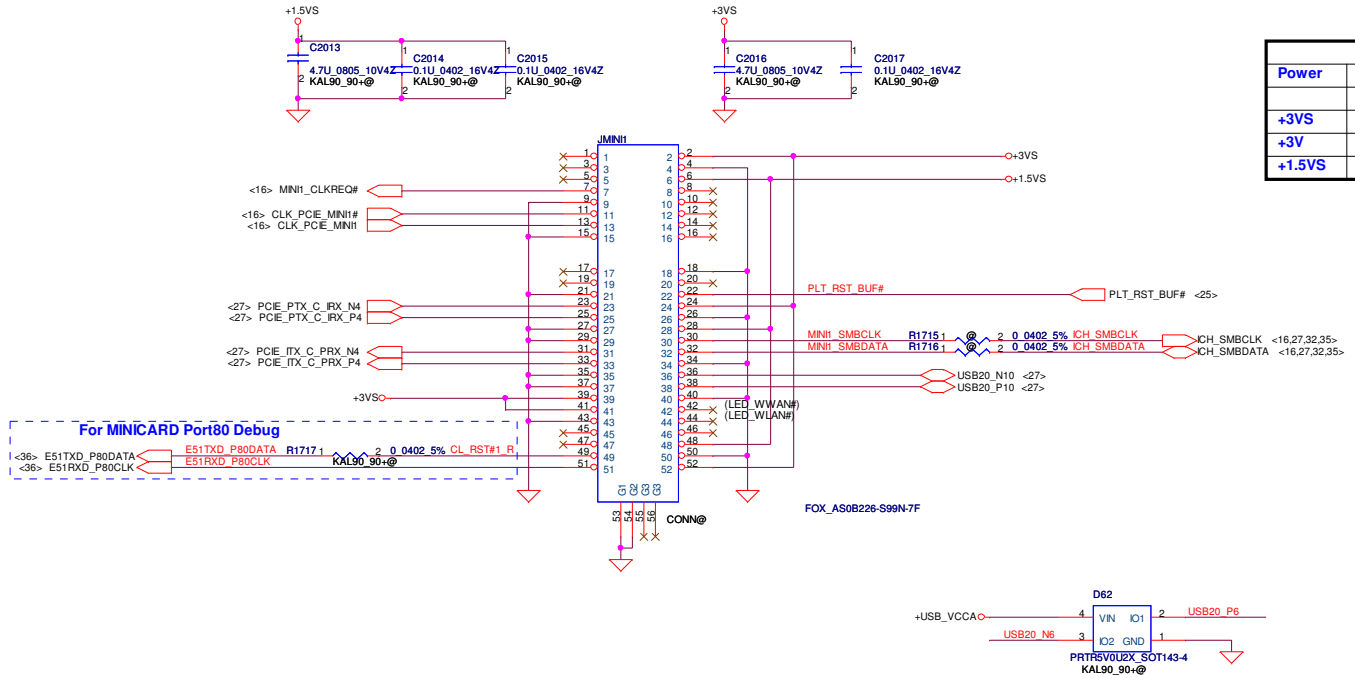
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

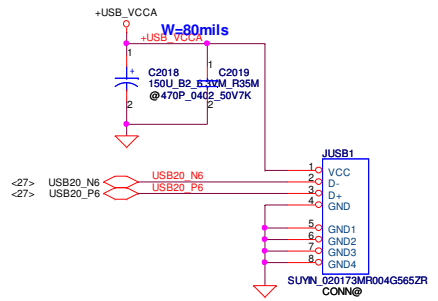
Date: Monday, April 27, 2009 Sheet 33 of 53

For Robson2

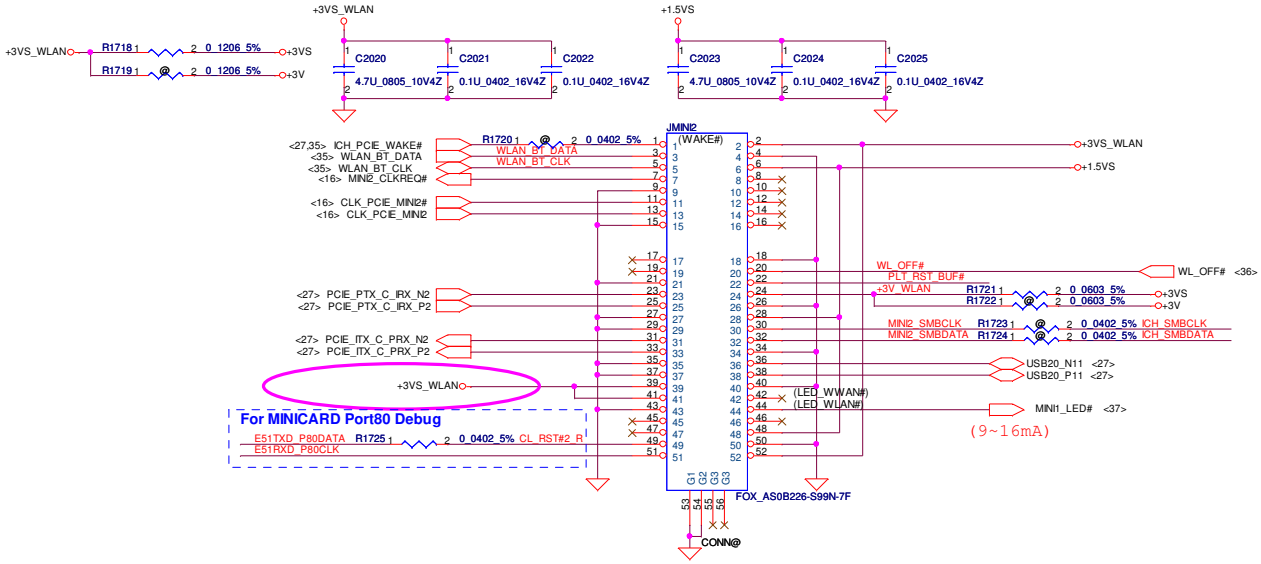


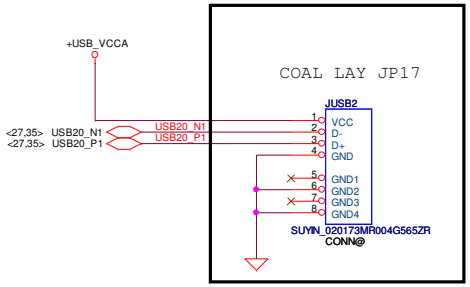
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

USB CONN.

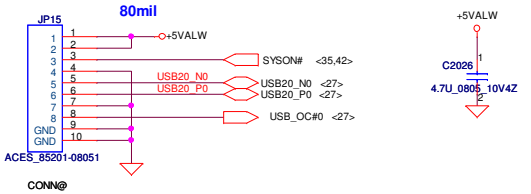


For Wireless LAN





To USB/B Connector



Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

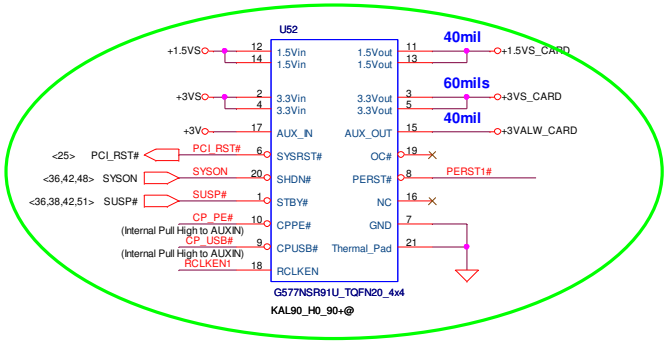
Compal Electronics, Inc.

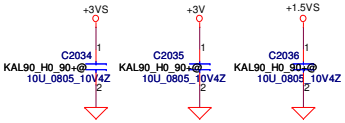
Title: MINI CARD (WLAN & Robson2)

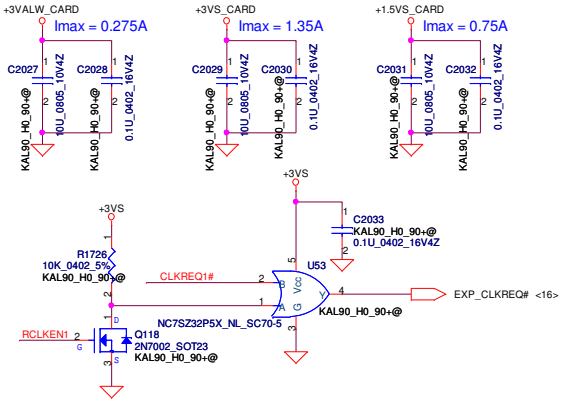
Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 34 of 53

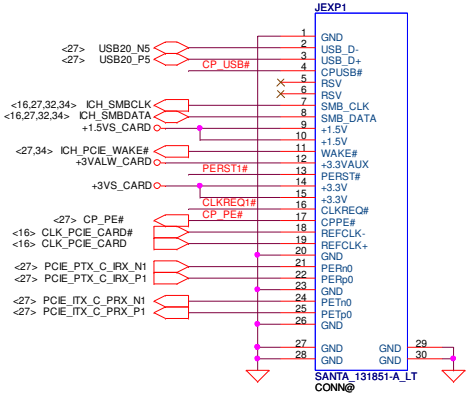
New Card Power Switch



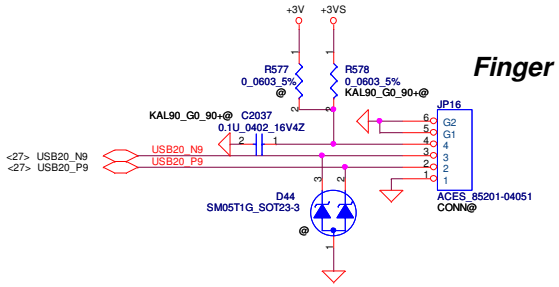




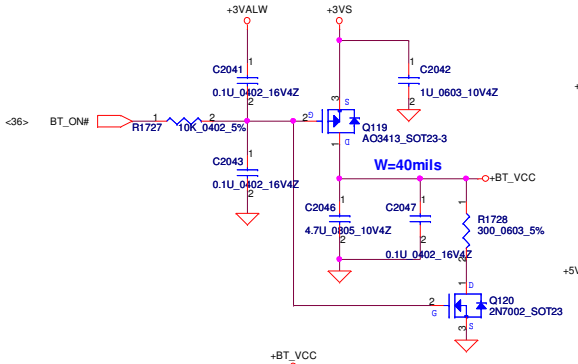
New Card Socket (Left/TOP)

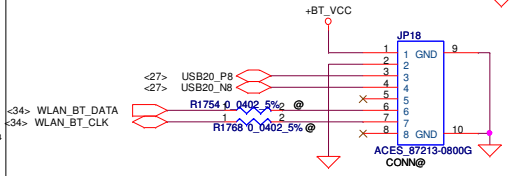


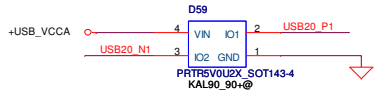
Finger Print Conn.

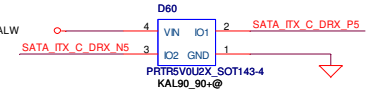


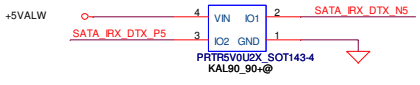
Bluetooth Conn.



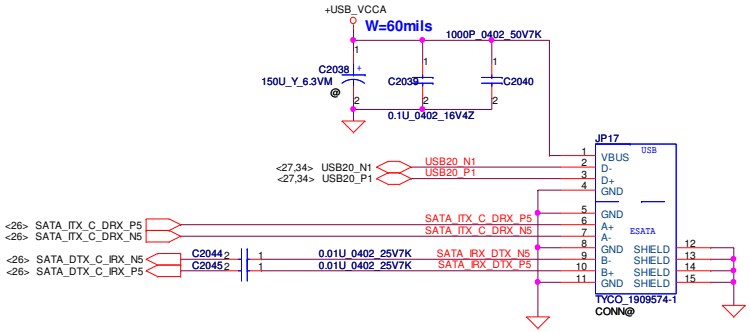


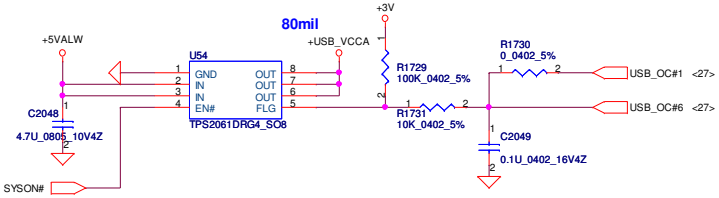






ESATA CONN





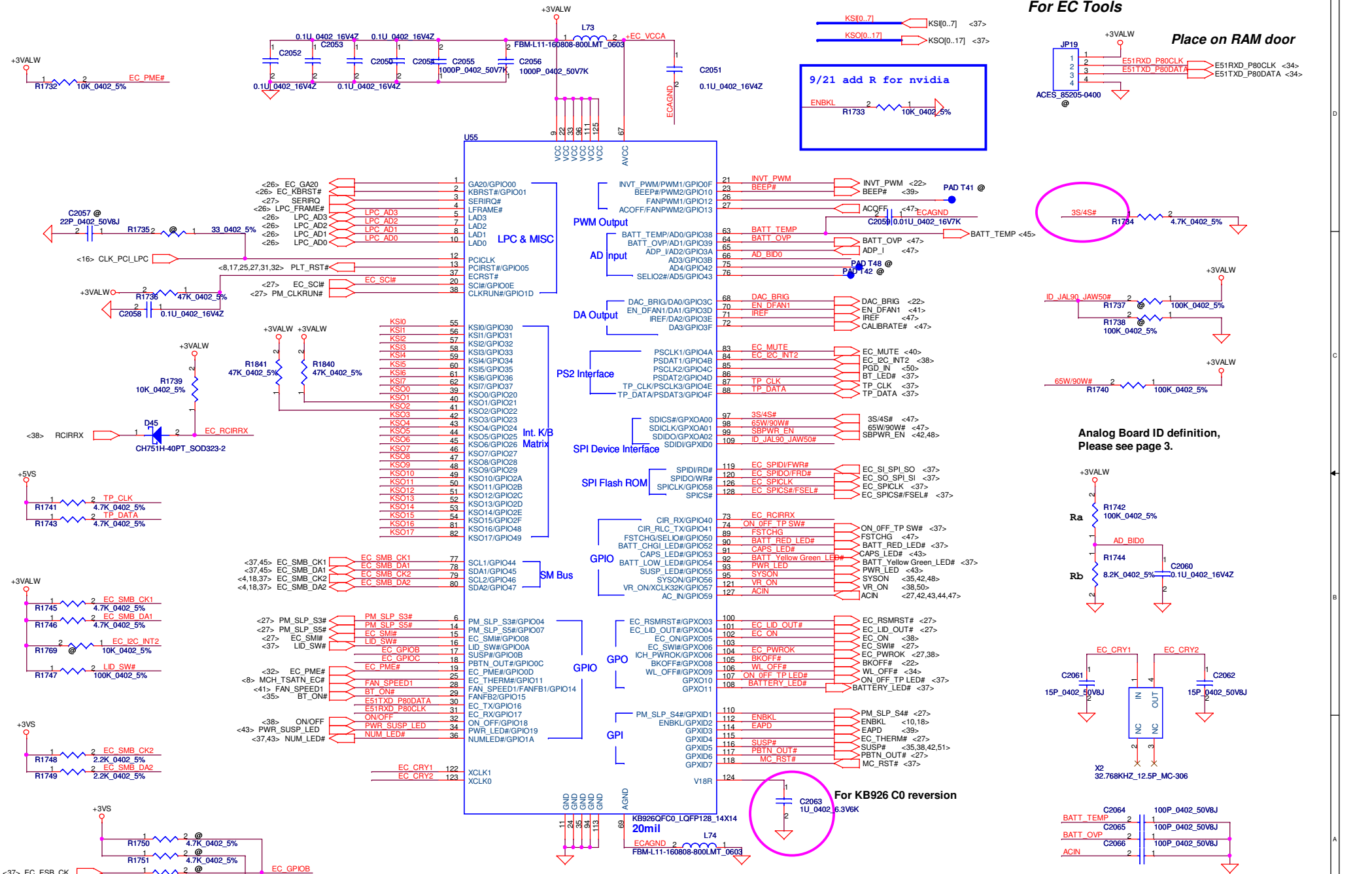
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

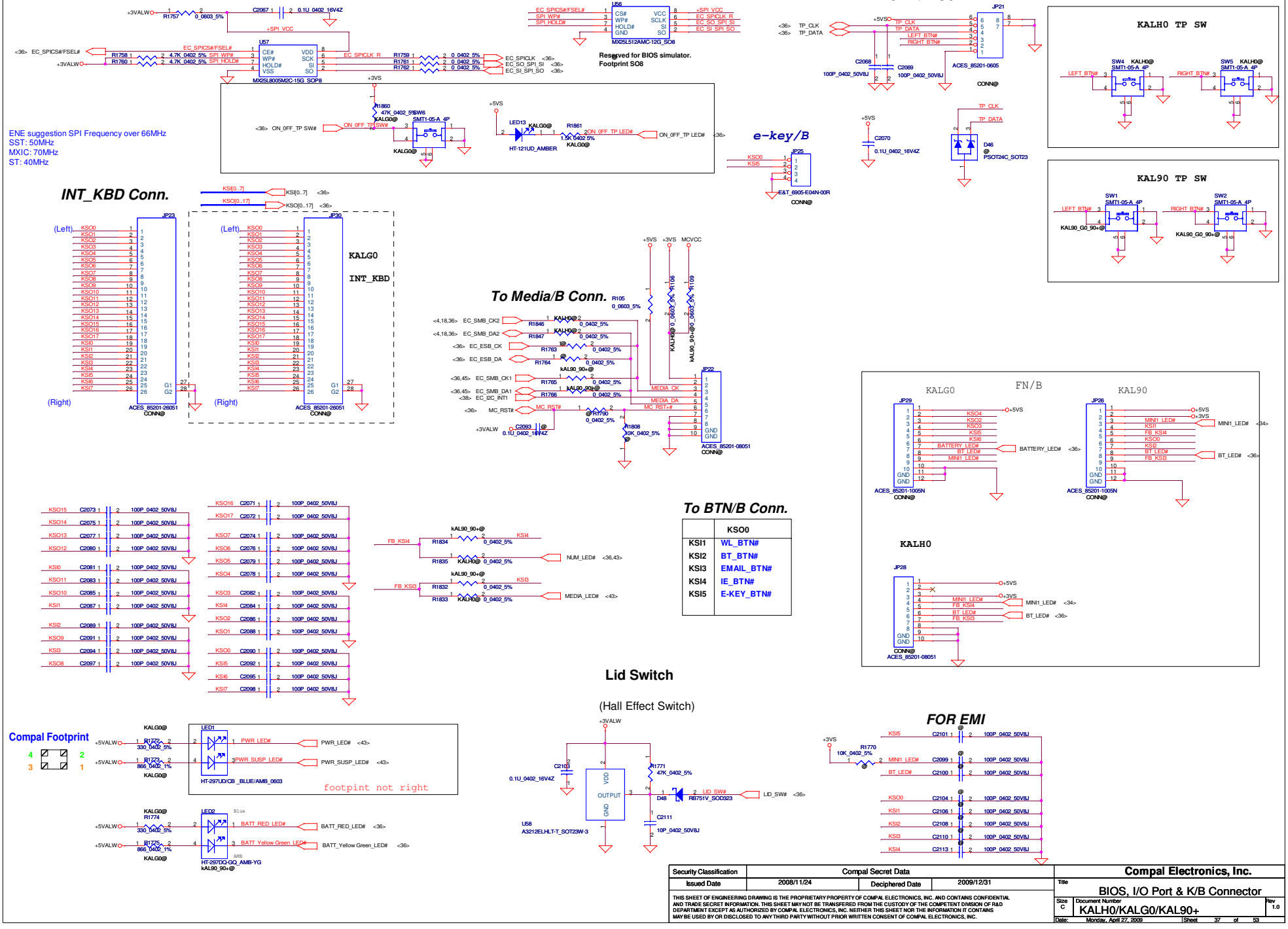
Compal Electronics, Inc.

Title: NEW CARD & eSATA Connector

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 35 of 53


For EC Tools
Place on RAM door
9/21 add R for nvidia
U55
KB926QFC0_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
For KB926 C0 reversion
Analog Board ID definition, Please see page 3.
Compal Secret Data
Compal Electronics, Inc.
EC ENE KB926
KALH0/KALG0/KAL90+
2008/11/24
2009/12/31
Monday, April 27, 2009
36 of 53



Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

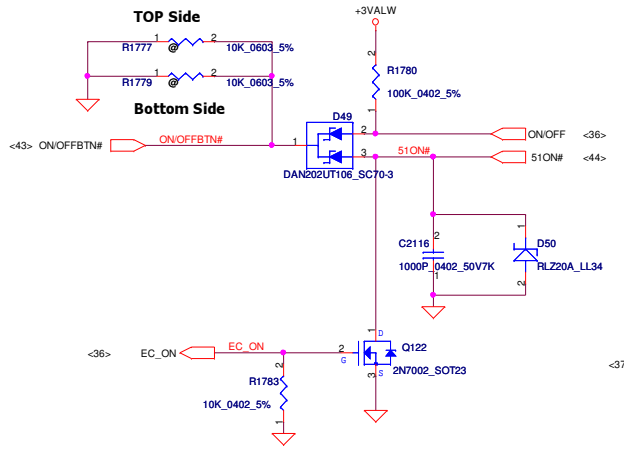
Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
C	KALH0/KALG0/KAL90+	1.0

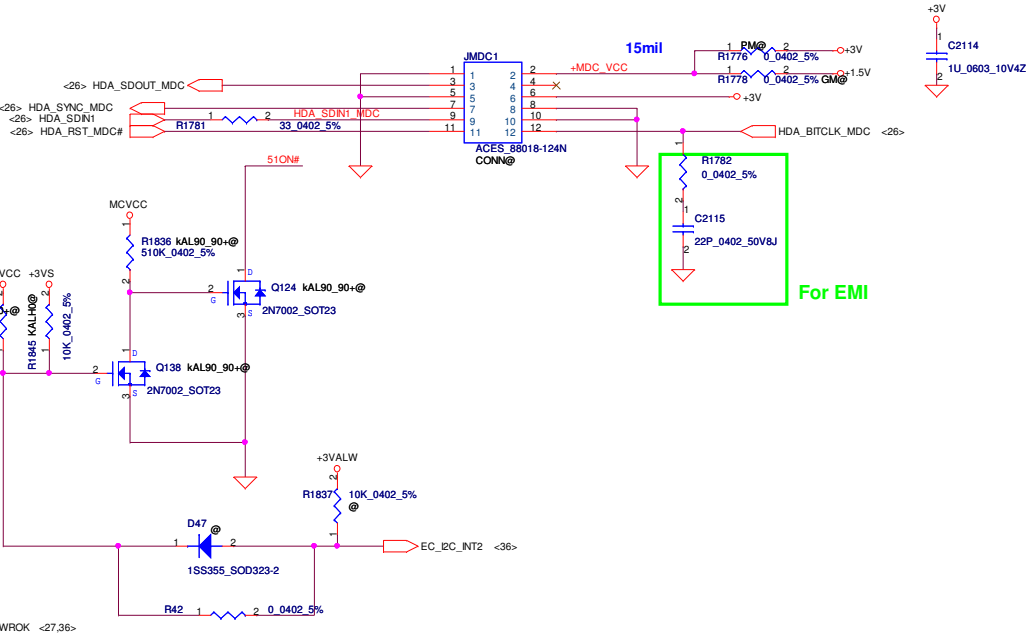
Date: Monday, April 27, 2009 Sheet 37 of 53

Power Button

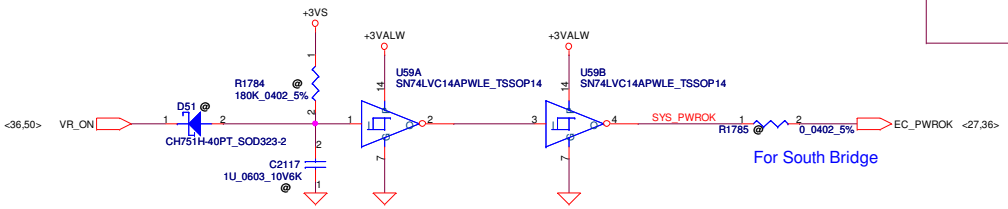
ON/OFF switch

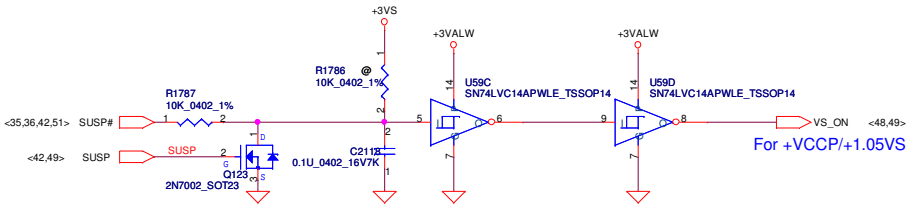


HDA MDC Conn.

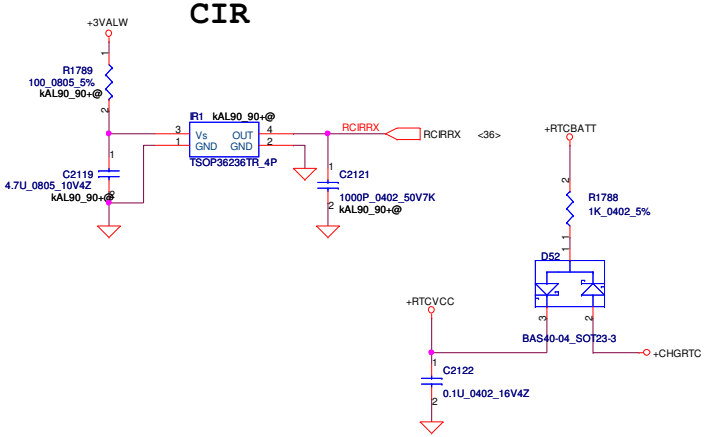


Power ON Circuit





CIR



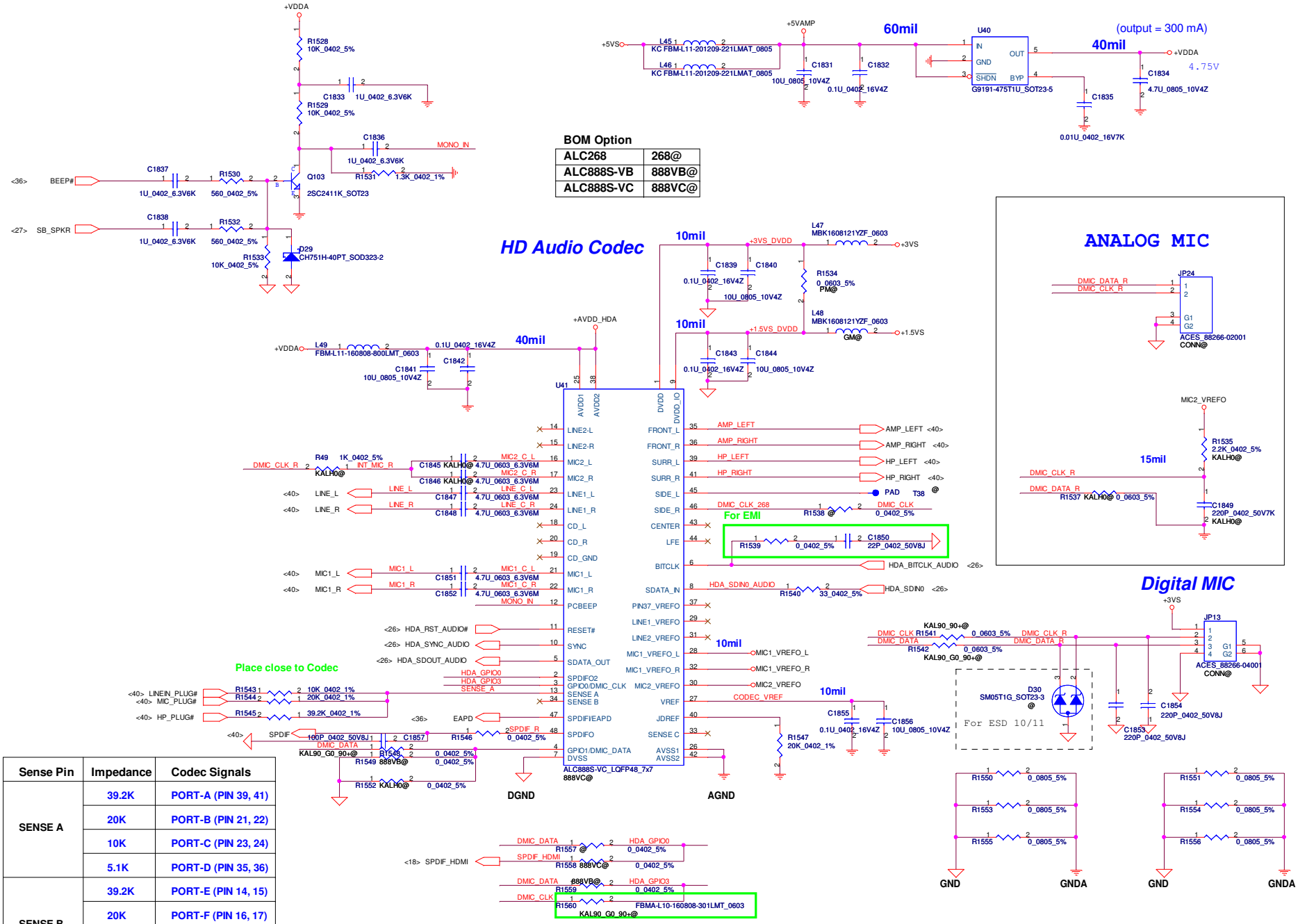
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Power OK, Reset,RTC, CIR, MDC

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 38 of 53



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

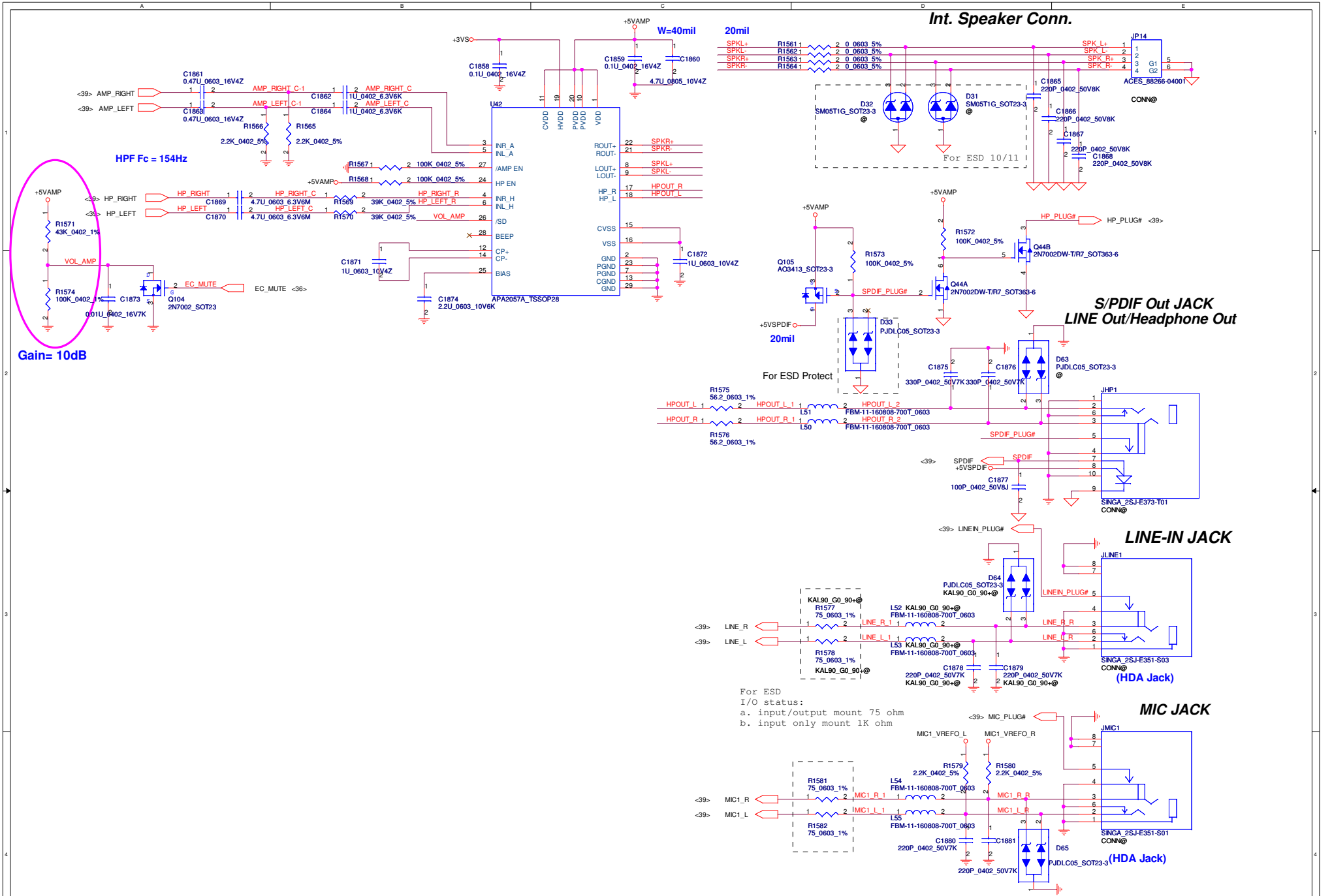
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: HD Audio Codec ALC888S-VC

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 39 of 53



Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

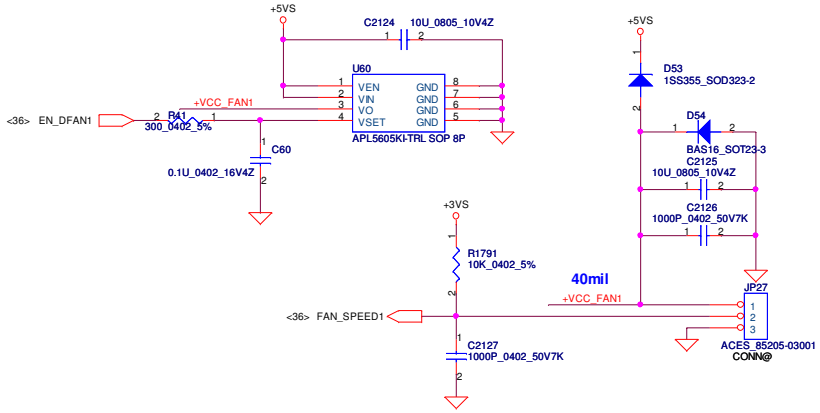
Compal Electronics, Inc.

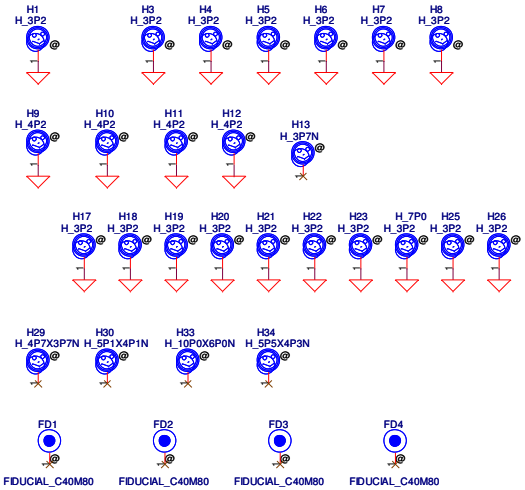
Title: Amplifier & Audio Jack

Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 40 of 53

FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

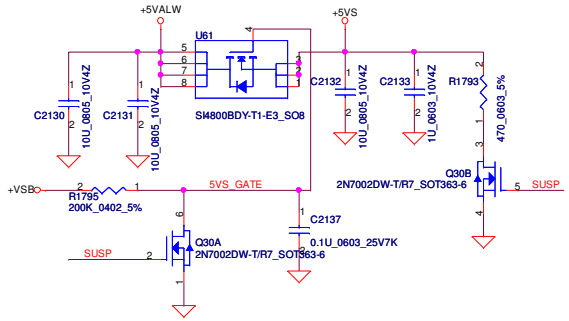
Compal Electronics, Inc.

Title: FAN & COVER LIGHT& Screw Hole

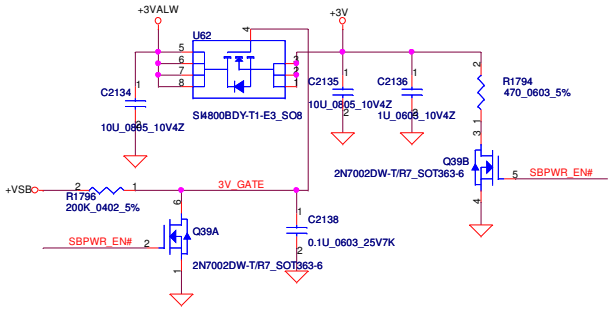
Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

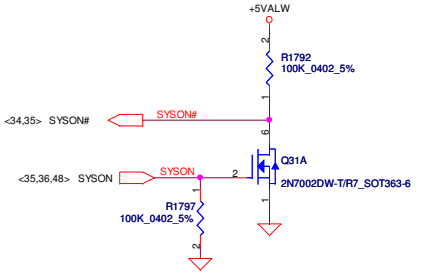
Date: Monday, April 27, 2009 Sheet 41 of 53

+5VALW TO +5VS

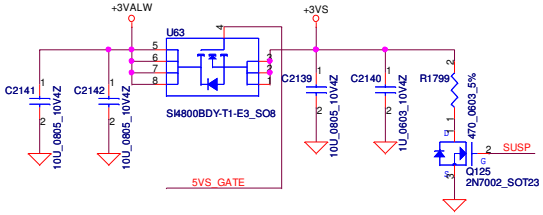


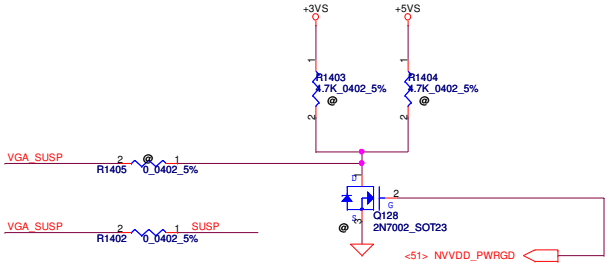
+3VALW TO +3V_SB(ICH8M AUX Power)



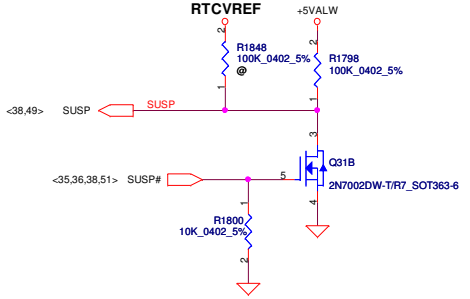


+3VALW TO +3VS

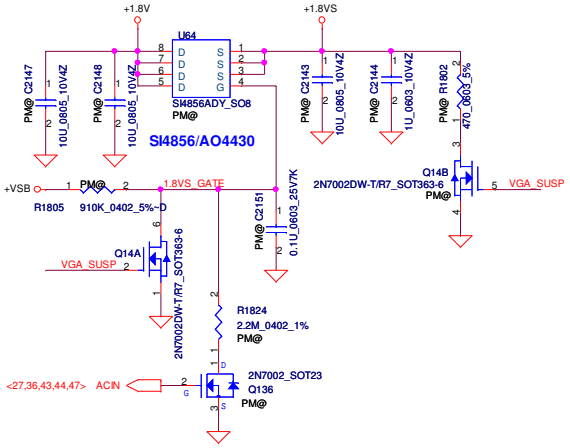




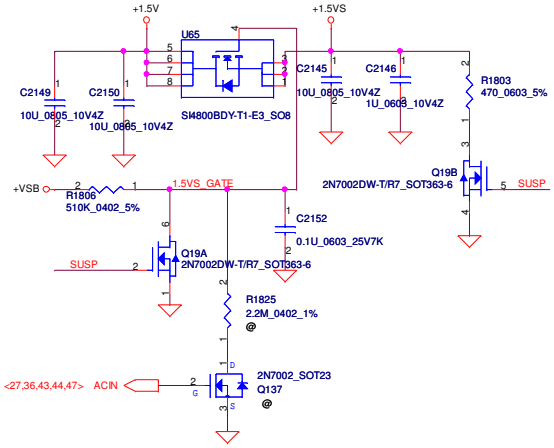
RTCVREF

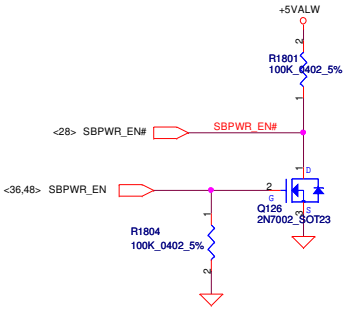


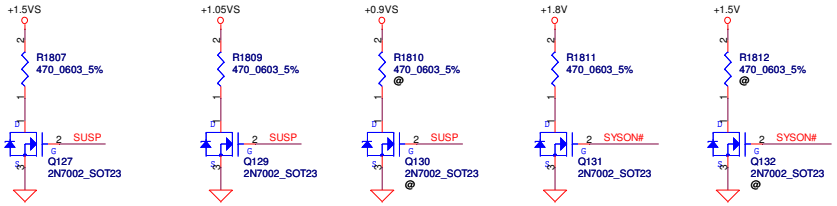
+1.8V to +1.8VS



+1.5V to +1.5VS







Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

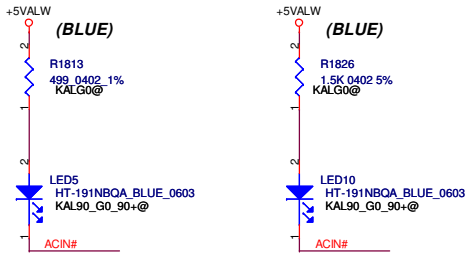
Compal Electronics, Inc.

Title: DC Interface

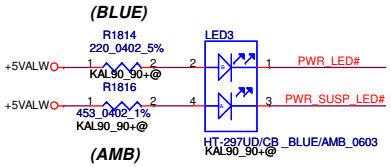
Size	Document Number	Rev
B	KALH0/KALG0/KAL90+	1.0

Date: Monday, April 27, 2009 | Sheet 42 of 53

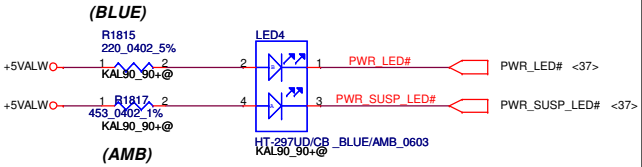
Enlightener LED



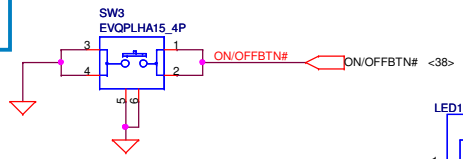
ON/OFF LED LEFT

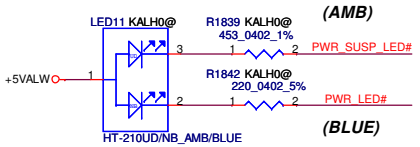


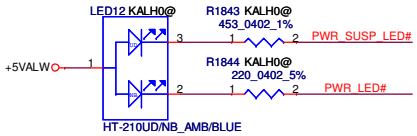
ON/OFF LED RIGHT



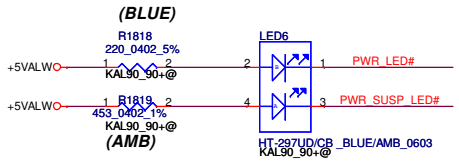
ON/OFF Button



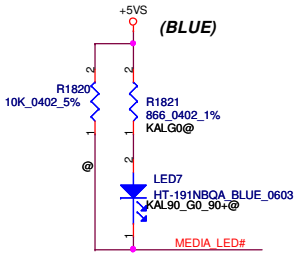




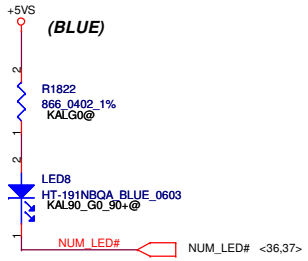
ON/OFF LED DOWN



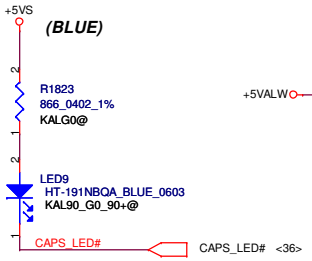
MEDIA_LED



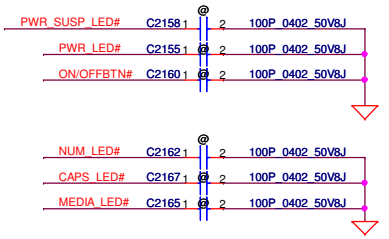
NUM_LED

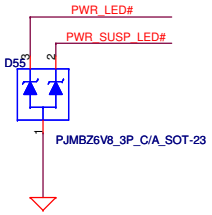


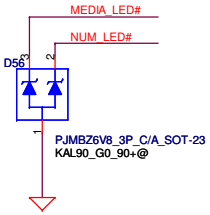
CAPS_LED

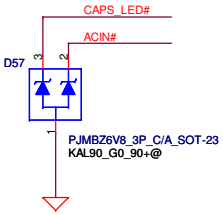


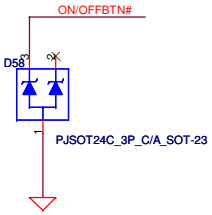
FOR EMI

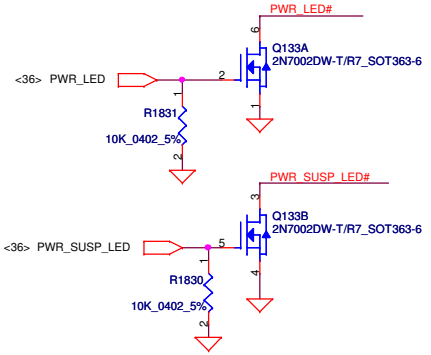






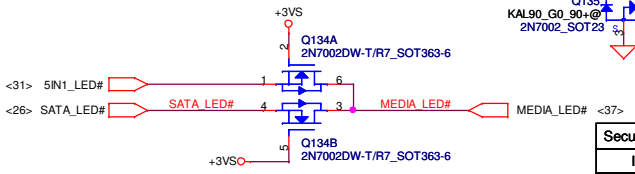






D1 D2 D3 USE PANJIT PJMBZ6V8
SCA00000I00
6.8V

D4 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V



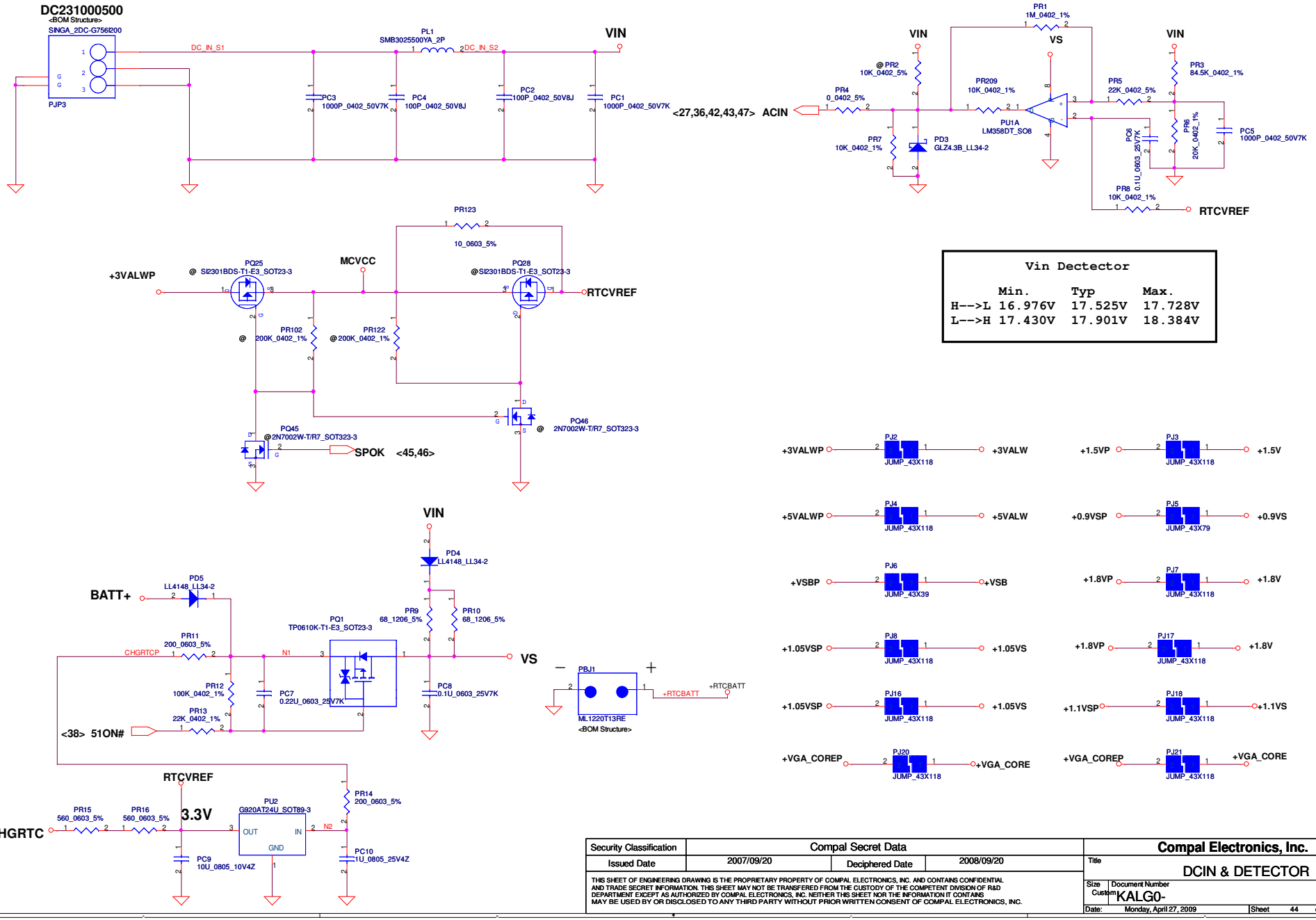
Security Classification	Compal Secret Data		
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: PWR/B

Size: Custom | Document Number: KALH0/KALG0/KAL90+ | Rev: 1.0

Date: Monday, April 27, 2009 | Sheet 43 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: DCIN & DETECTOR

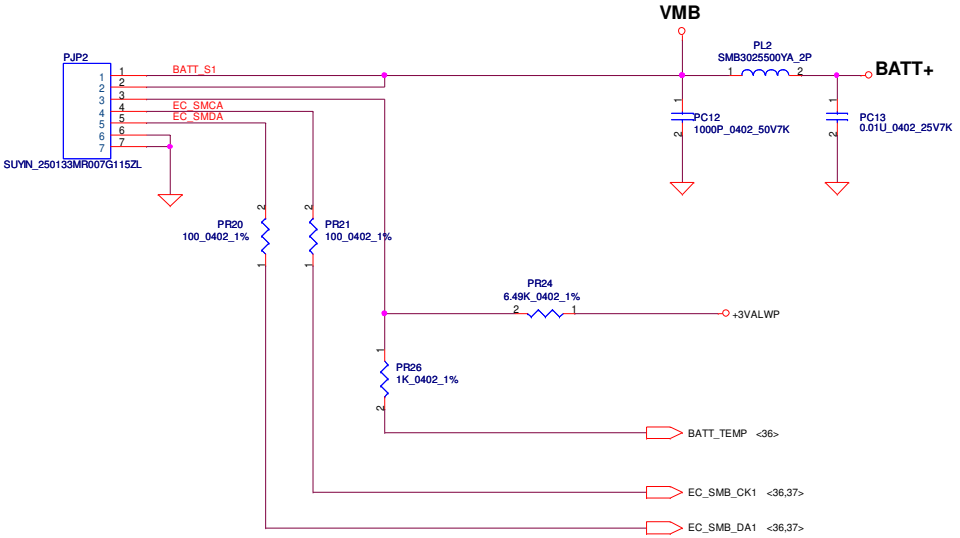
Size	Document Number	Rev
Custom	KALG0-	0.1

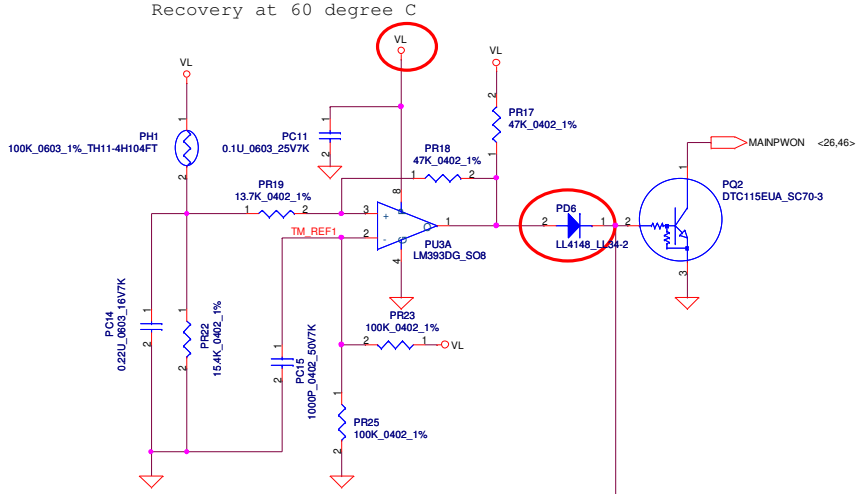
Date: Monday, April 27, 2009 | Sheet 44 of 53

PH1 under CPU botten side :

CPU thermal protection at 96 degree C

Recovery at 60 degree C

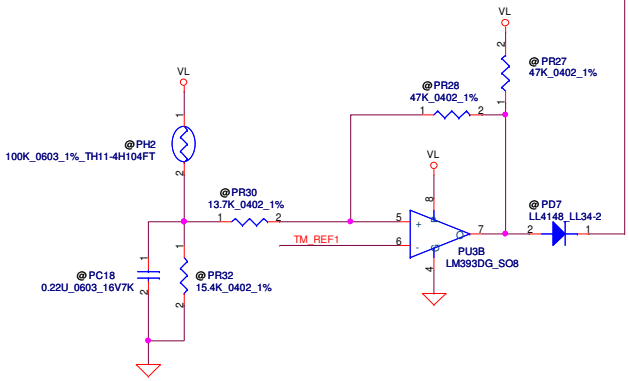


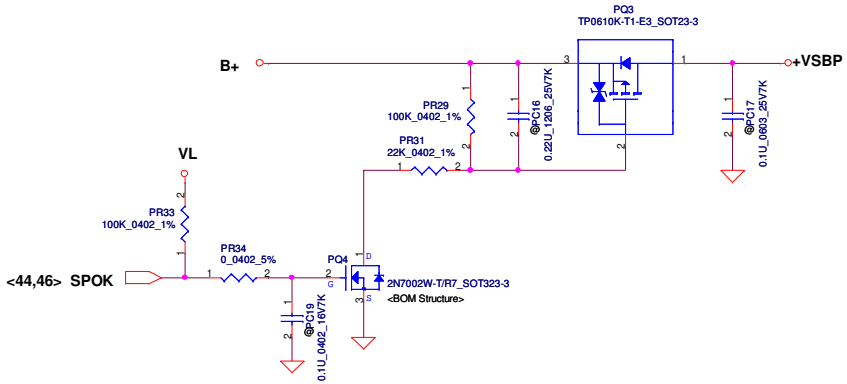


PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C

Recovery at 47 degree C





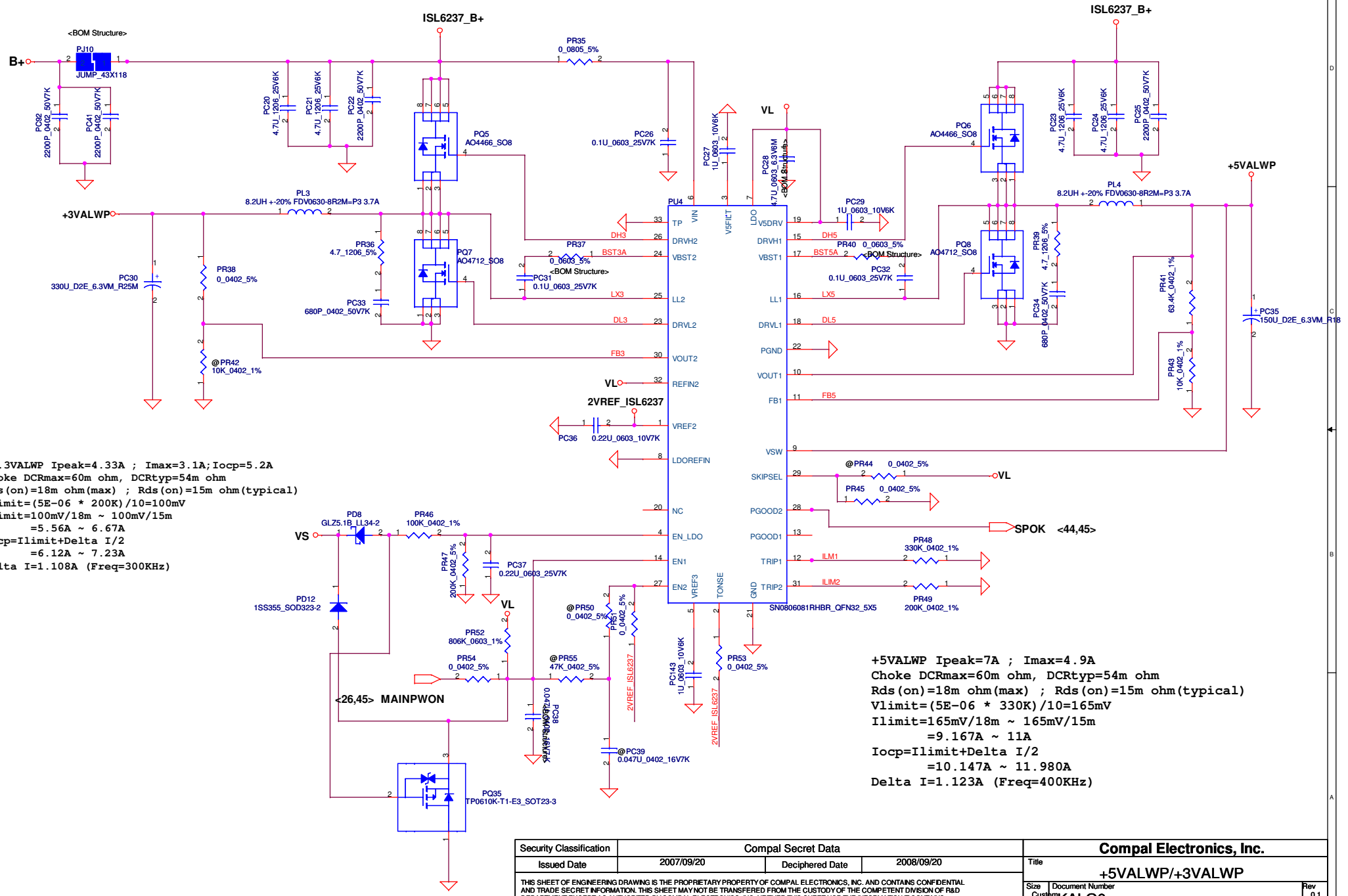
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
Custom	KALG0-	0.1

Date: Monday, April 27, 2009 | Sheet 45 of 53



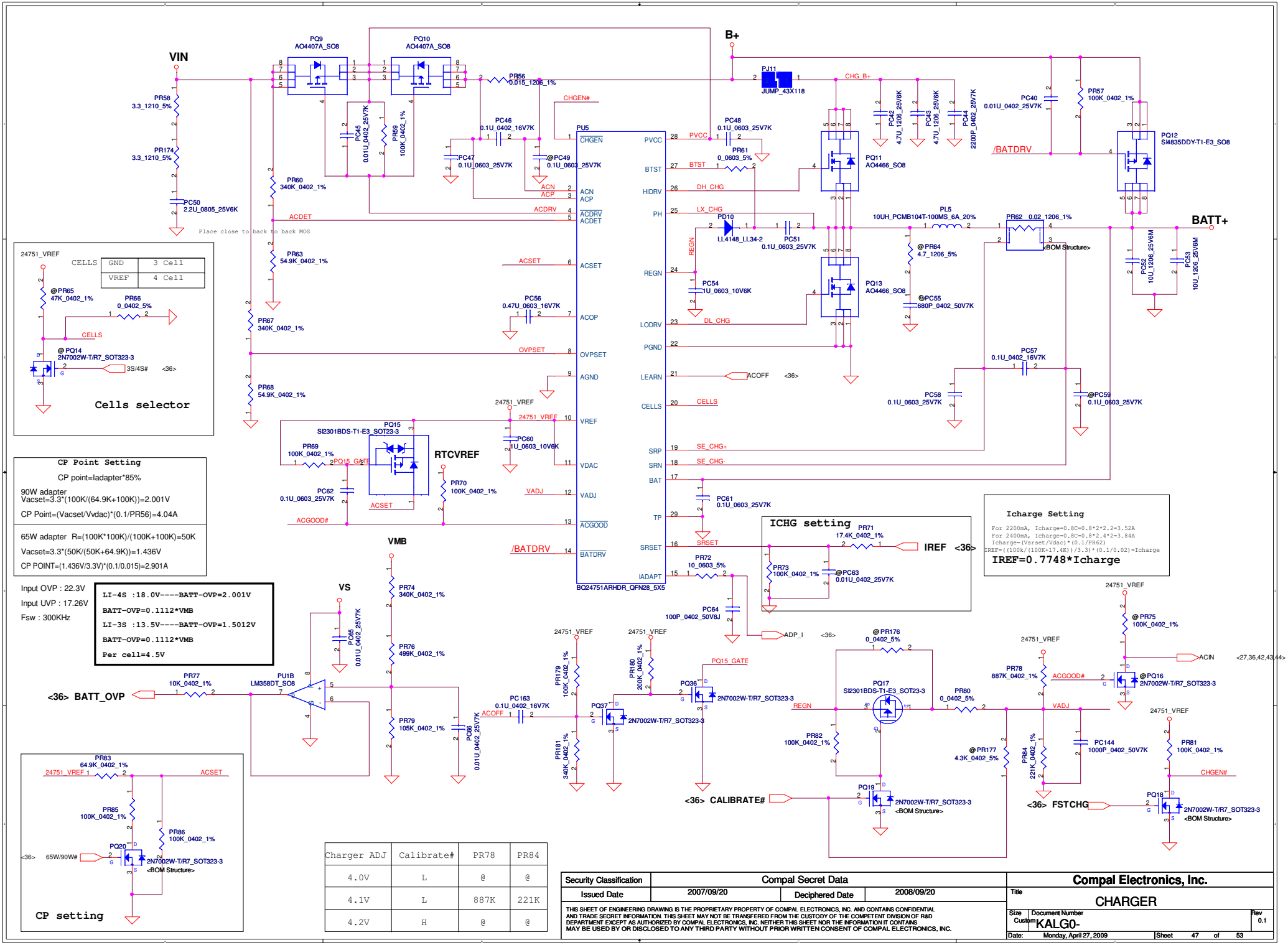
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size	Document Number	Rev
Custom	KALG0-	0.1

Date: Monday, April 27, 2009 Sheet 46 of 53



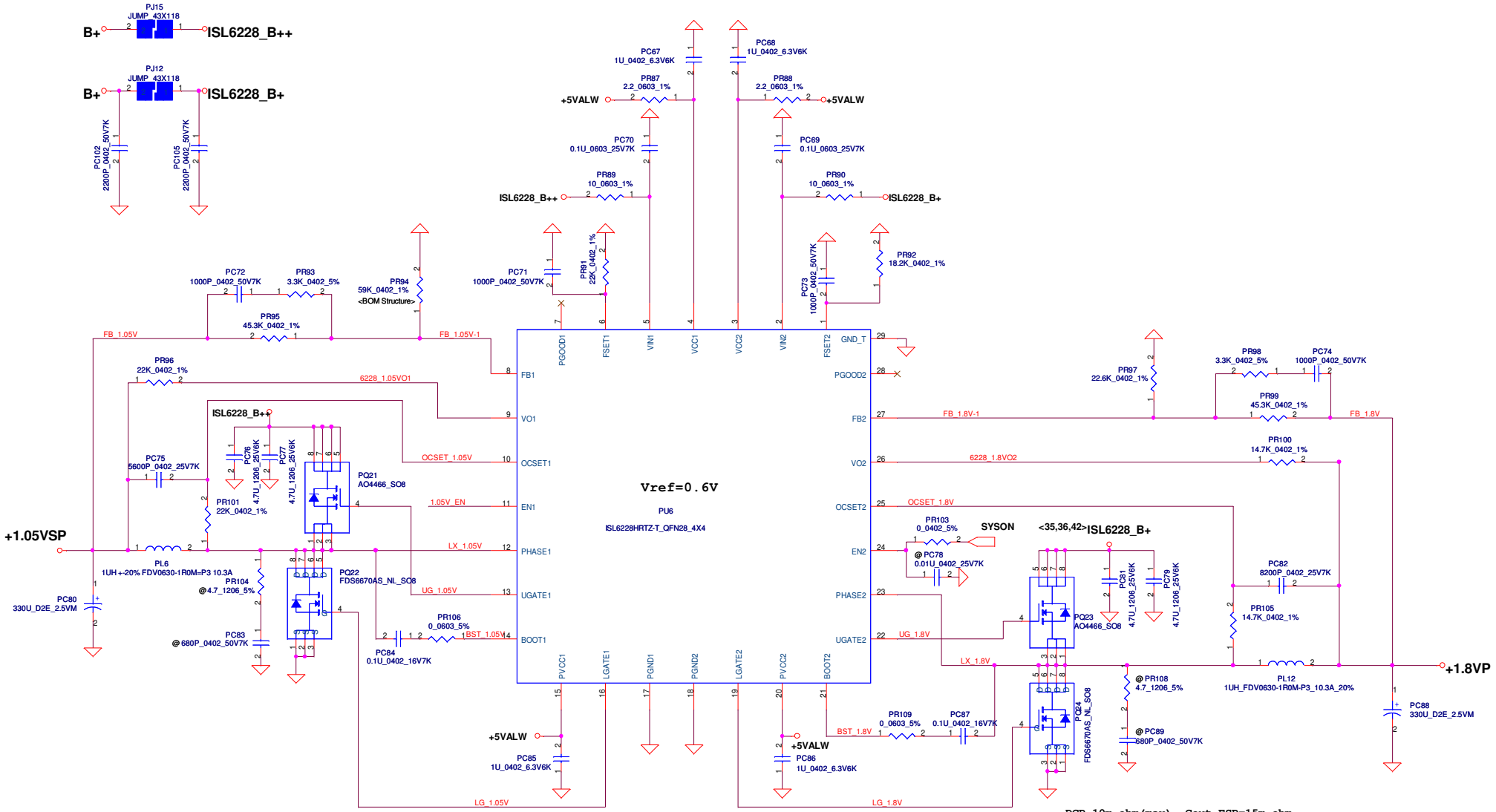
Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
Custom	KALG0-	0.1

Date: Monday, April 27, 2009 | Sheet 47 of 53



DCR 10m ohm(max) Cout ESR=15m ohm

1.05VSP (Ibudget=17.47A) OCP Seting
Fsw=1/1.5E-10*22k =303K
Vo=Vref*((PR95+PR94)/PR94)
Ipeak=13.29A, Imax=9.31A
Iocp=13.29*1.2=15.95A
Delta I=4.09A
Iocp*DCR=(Rocset*9.5uA)=(15.95*1.3*10m; Roset=21.8K
now chose Roset=22K
Csen=L/(DCR*Roset)=1uH/(10m*22k); Csen=0.00523uF
now chose Csen=5600pF
Iocp_min=(22K*9.5uA)/(10m ohm*1.3) =16.07A
Iocp_max=(22K*10.5uA/(10m ohm)=23.1A

<36,42> SBPWR_EN
@PR178 0_0402_5%
1.05V_EN
@PC94 0.1U_0402_16V7K
PR112 0_0402_5%
<38,49> VS_ON

DCR 10m ohm(max) Cout ESR=15m ohm
1.8VP(Ibudget=9.91A) Ipeak=9A, Imax=6.3 A
Fsw=1/1.5E-10*18.2k =366K
Vo=Vref*((PR97+PR99)/PR97)
Iocp=9*1.2=10.8A
Iocp*DCR=(Rocset*9.5uA)=10.67*1.3*10m; Roset=14.78K
now chose Roset=14.7K
Csen=L/(DCR*Roset)=1uH/(10m*14.7k); Csen=8.16nF
now chose Csen=8200pF
Iocp_min=(14.7K*9.5uA)/(10m ohm*1.3) =10.74A
Iocp_max=(14.7*10.5uA)/(10m ohm)=15.43A

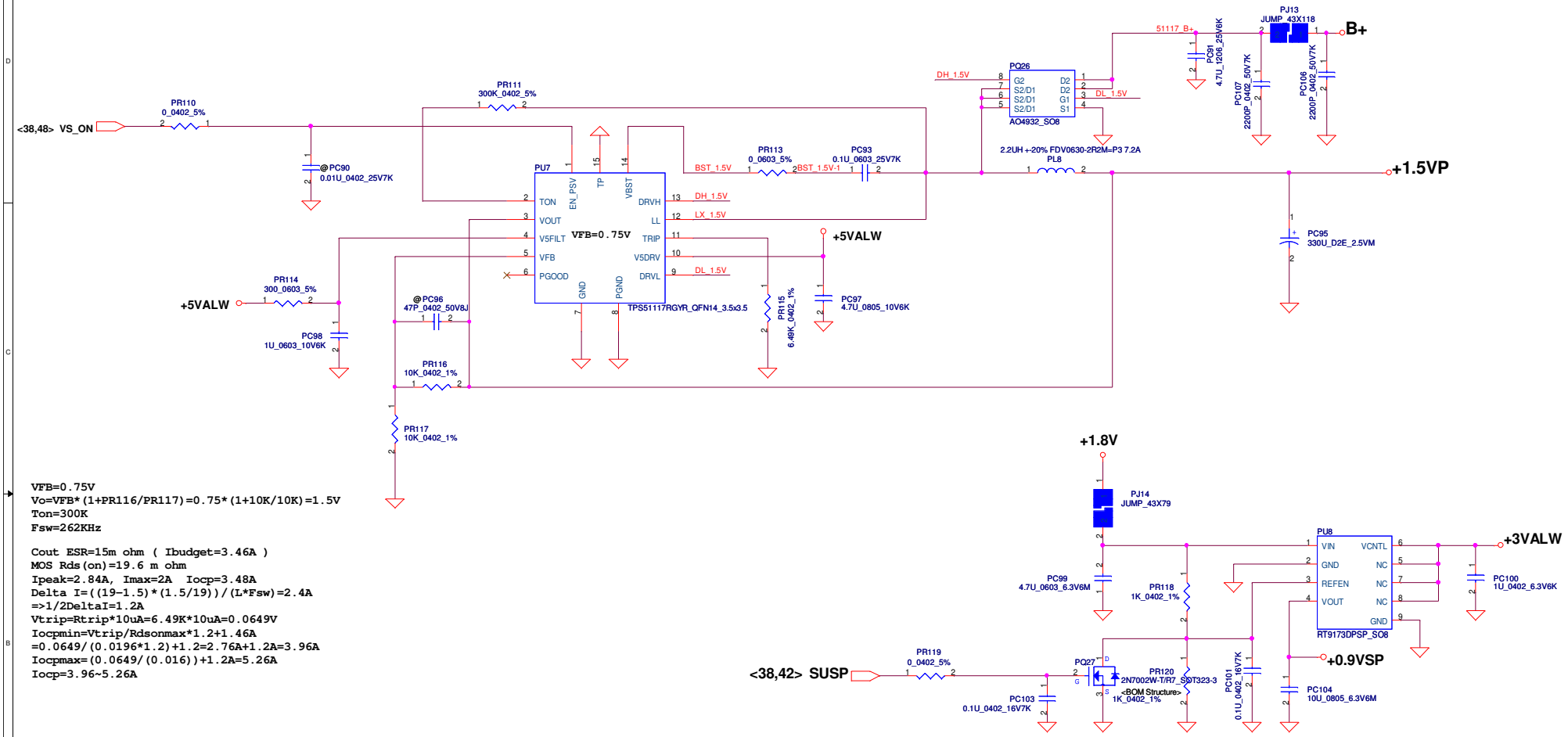
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: 1.8VP / 1.05VSP

Size	Document Number	Rev
Custom	KALG0-	0.1

Date: Monday, April 27, 2009 Sheet 48 of 53



VFB=0.75V
Vo=VFB*(1+PR116/PR117)=0.75*(1+10K/10K)=1.5V
Ton=300K
Fsw=262KHz

Cout ESR=15m ohm (Ibudget=3.46A)
MOS Rds(on)=19.6 m ohm
Ipeak=2.84A, Imax=2A Iocp=3.48A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=2.4A
=>1/2DeltaI=1.2A
Vtrip=Rtrip*10uA=6.49K*10uA=0.0649V
Iocpmin=Vtrip/Rdsonmax*1.2+1.46A
=0.0649/(0.0196*1.2)+1.2=2.76A+1.2A=3.96A
Iocpmax=(0.0649/(0.016))+1.2A=5.26A
Iocp=3.96~5.26A

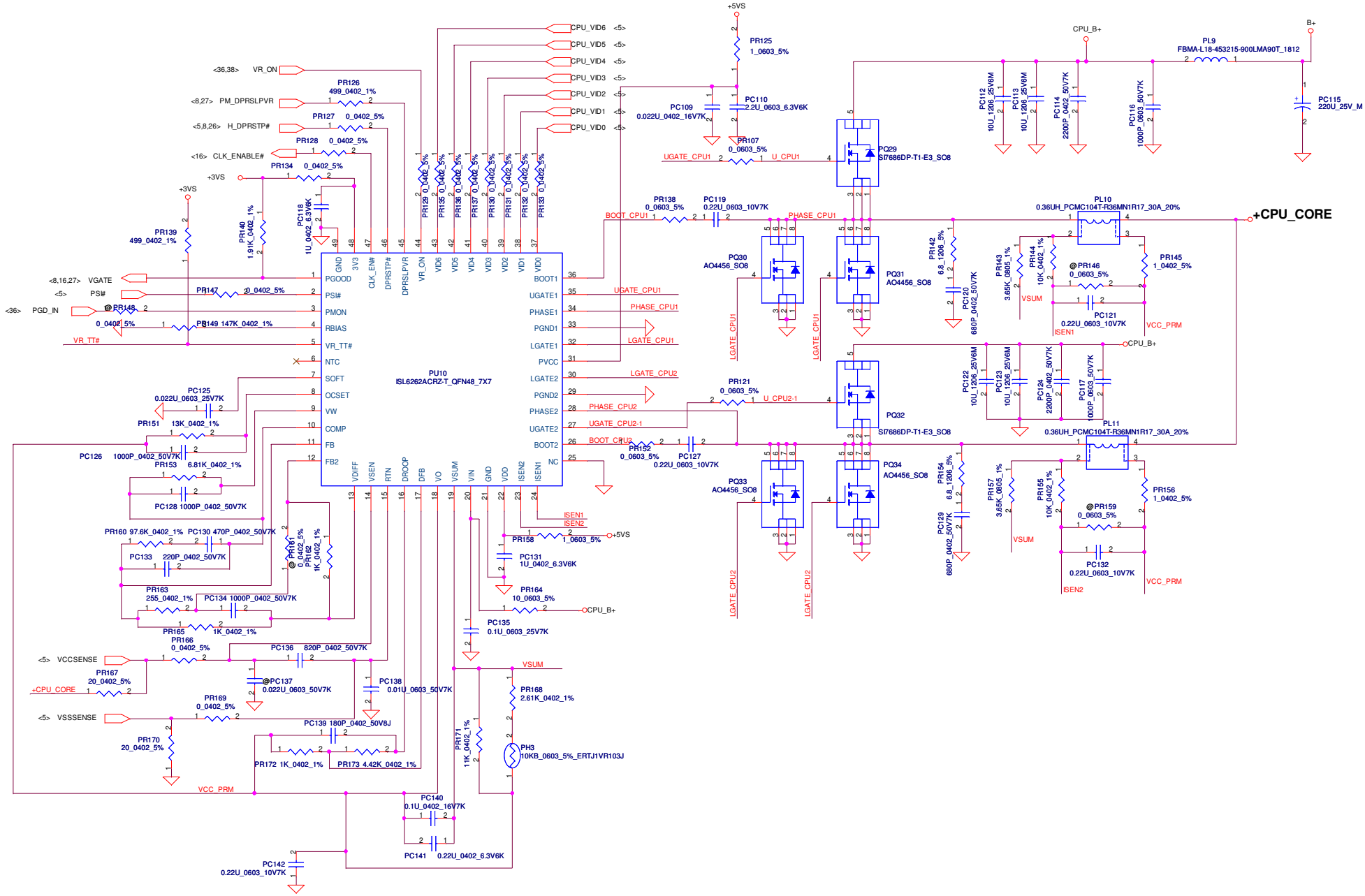
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +1.5VP/+0.9VSP

Size	Document Number	Rev
Custom	KALG0-	0.1

Date: Monday, April 27, 2009 | Sheet 49 of 53



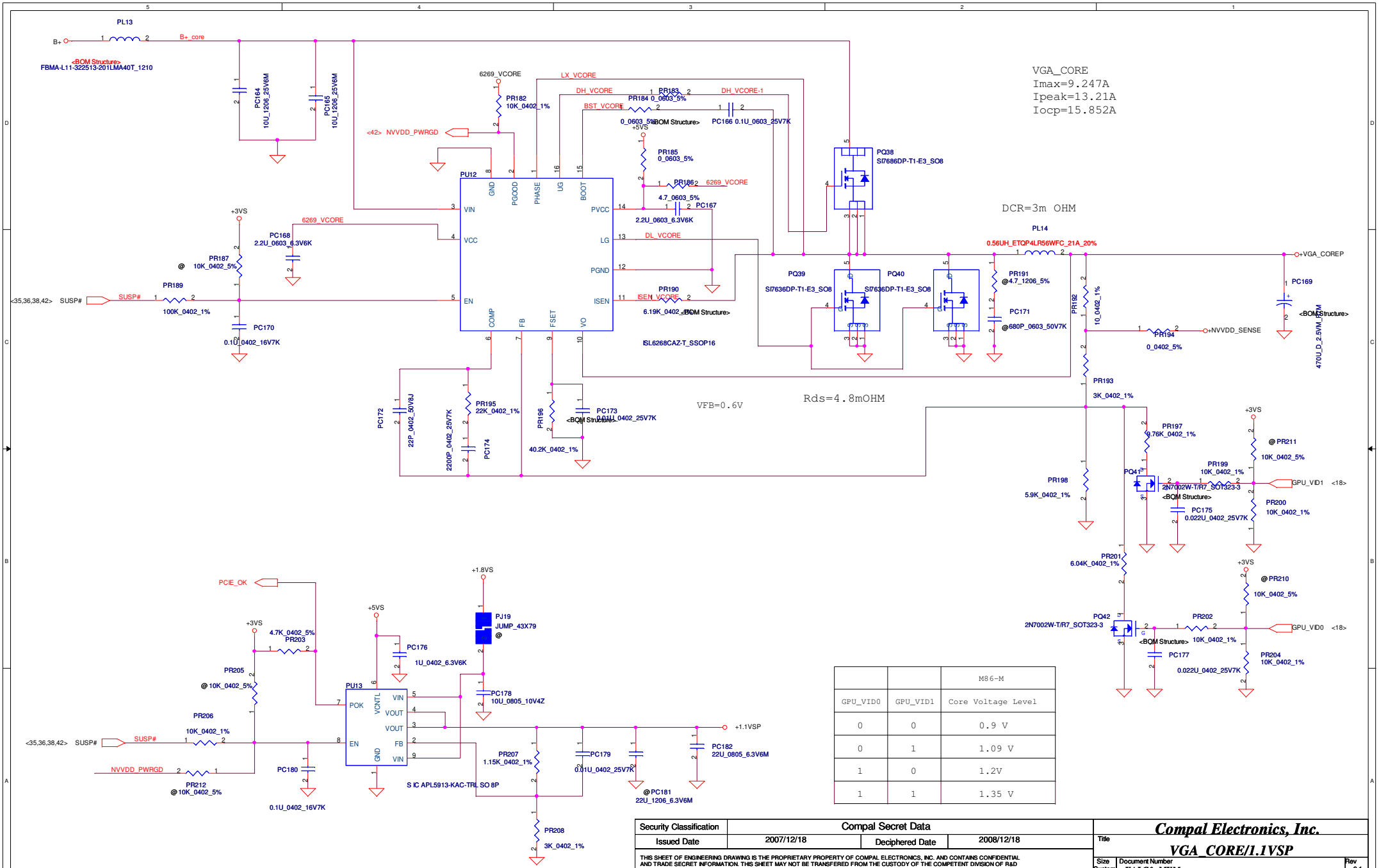
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
Custom	KALG0-	0.1

Date: Monday, April 27, 2009 | Sheet 50 of 53



		M86-M
GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.9 V
0	1	1.09 V
1	0	1.2V
1	1	1.35 V

Security Classification	Compal Secret Data		
Issued Date	2007/12/18	Deciphered Date	2008/12/18

Compal Electronics, Inc.

Title: VGA_CORE/1.1VSP

Size: Custom | Document Number: KALG0- MXM | Rev: 0.1

Date: Monday, April 27, 2009 | Sheet 51 of 53

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR196 value	VGA OCP	0.3	50	change the resistance value of pr196 from 57.6K to 40.2K	2009/02/06	PVT
2	Change PL14 value	prevent OVP occur	0.3	50	change the inductance value of pL14 from 1uH to 0.56 uH	2009/02/06	PVT
3	Change PU4 IC part number	vender suggestion	0.3	45	change part number to SA00002V400	2009/02/06	PVT
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: KAL90 | Rev: 0.1

Date: Monday, April 27, 2009 | Sheet 52 of 53

B --> C Change List

0220----------
Page 6, Change C98 BOM structure to @

0218----------
Page 20, Add R569 with BOM structure @
Page 23, R34, R38, R40, R53, R54, R55 change BOM structure to @
Page 31, Change R215 to 18K
Update Power Schematics

0213----------
Page 11, Delete R113
Add J1 JUMP_43X79 with BOM structure @
Page 31, R558, R559 0 ohm with BOM structure @
R560, R561 4.7K with BOM structure @
Page 32, R562, R563 0 ohm with BOM Structure @
R564, R565 0 ohm
Page 38, Delete C619
Add R566, R567, R568 0_0603 with BOM Structure JAL90@
0204----------
Page 12, Change L31 to MBK1608301YZF_0603 with BOM structure GM@
Change R163 to 0_0805_5%
Page 23, Change BOM Structure of U5 to @
Page 27, Change BOM Structure of R555 and R550 to @
Page 33, Change R217 to 31.6K_0402_1%
Change C313 to 1U_0603_10V6K
Page 34, Change R503 to FBMA-L10-160808-301LMT_0603
01/31----------
Page 23, Delete U10
01/29----------
Page 23, Change R152 BOM Structure to @
01/24----------
Page 4, Change U8 to SA00001Z700 (EMC1402)
Page 33, Change C338 to SE076104K80
Page 35, Mount C584
01/23----------
Page 38 Delete F3, R558~560, C609~614
01/22----------
Page 11, Delete R79
Change J1 Symbol to JUMP_43X79
Page 33, Add R557 10K (Check)
Change R245 BOM Structure with @
Page 38, Add C609~614, R558~560 (Check)
C607,608, 615~619 (Check)
01/17----------
Page 11, Add R79 0_0805
Update Power Schematics
01/16----------
Page 11, Delete R79 0_0805
Add J1 JUMP_43X79
Page 16, Change C296, R301 to 27P_0402
Page 19, Change L17, L19, L21 BOM structure to GM@
Page 23, Mount U29, R339
Add U10 with BOM structure @ (Co-lay with U5)
Change R340 Bom structure to @
Change U5 to MX25L4005AMC-12G_SO8 (SA00002A900)
Page 27, Change U26, C420 BOM structure to @
Change R550 to 0_0402
Add R555 0_0402
Page 32, Change R269 to 240_0402_5%, R267 to 453_0402_1%
Change R268 pin1 connect to +5VALW
Page 33, Change R217 to 18K_0402_1% with BOM structure PM@
Page 35, Add R551,R552, R553, R554 75_0603_1% with BOM structure JAL90@
Add D32 PJDLC05_SOT23-3
Page 38, Add F3 3A_15VDC_SMD2920P300TF/15
Page 49, Add R551,R552, R553, R554 1K_0603_1% with BOM structure 268@
Add L17, L19, L21 0_0805 with BOM structure PM@
Update U38 (ALC268-VB1-GR) PN:SA00001GD10 for JAW50

Security Classification	Compal Secret Data		
Issued Date	2008/03/28	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: HW PIR1

Size	Document Number	Rev
Custom	KAL90	0.1

Date: Monday, April 27, 2009 Sheet 53 of 53