

Compal Confidential

KALH0 /KAL90+ /KALG0 M/B Schematics Document Intel Penryn Processor with Cantiga + DDRIII + ICH9M

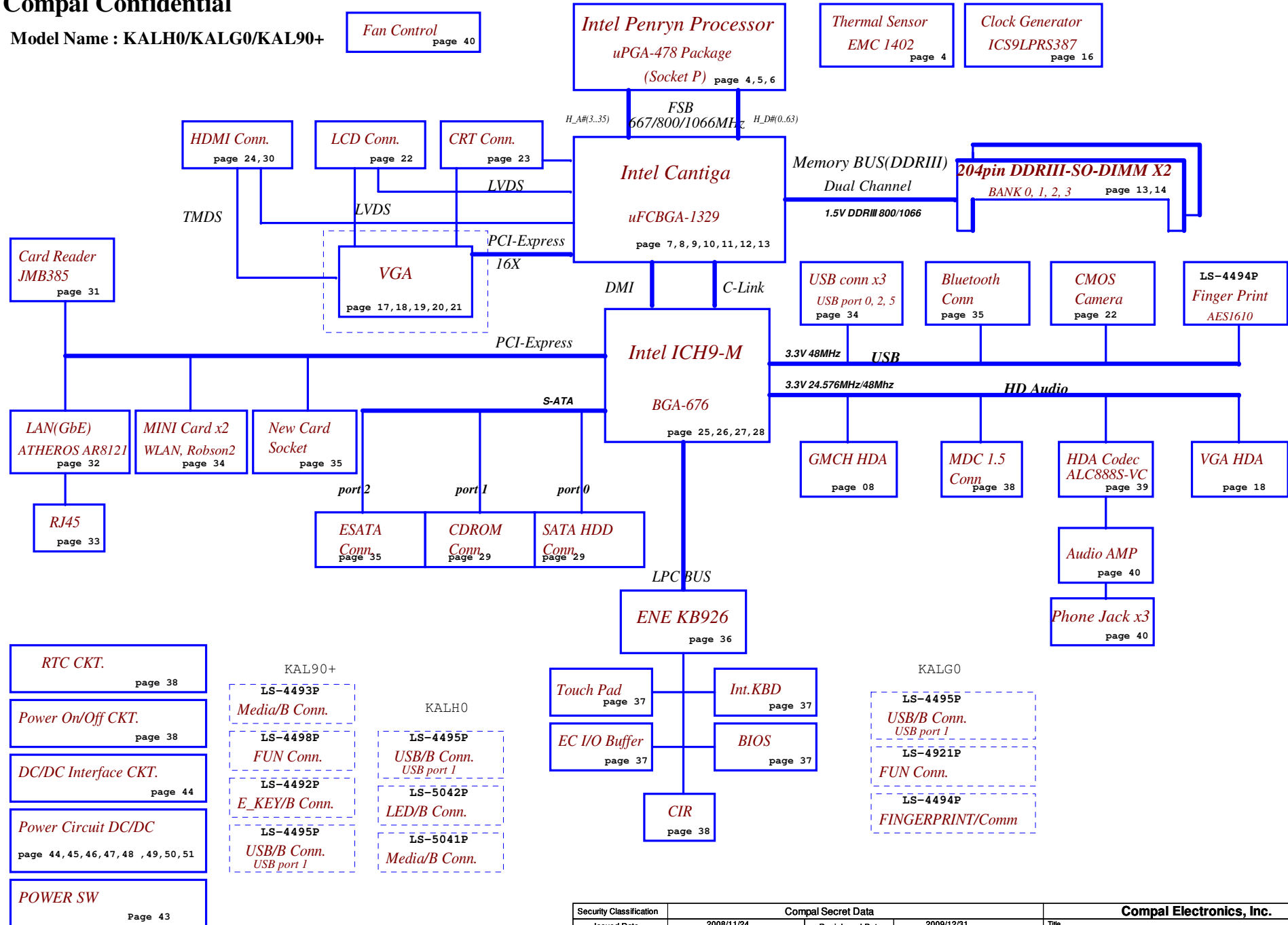
2009-3-4

REV: 1.0

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- Power On/Off CKT. page 38
- DC/DC Interface CKT. page 44
- Power Circuit DC/DC page 44, 45, 46, 47, 48, 49, 50, 51
- POWER SW Page 43

- KAL90+
- LS-4493P Media/B Conn.
 - LS-4498P FUN Conn.
 - LS-4492P E_KEY/B Conn.
 - LS-4495P USB/B Conn. USB port 1
- KALH0
- LS-4495P USB/B Conn. USB port 1
 - LS-5042P LED/B Conn.
 - LS-5041P Media/B Conn.

- KALG0
- LS-4495P USB/B Conn. USB port 1
 - LS-4921P FUN Conn.
 - LS-4494P FINGERPRINT/Comm

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA/DDR3	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V GM LVDS MODULE	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	USB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG6SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Configuration Table

Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX: KAL90/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX: KAL90/PM@/888VC@/8121@
KALH0-GM45	XXXXXXXXXX: KALH0/GM@/888VC@/8121@/GM45@
KALH0-GL40	XXXXXXXXXX: KALH0/GM@/888VC@/8121@/GL40@
KALH0-PM45	XXXXXXXXXX: KALH0/PM@/888VC@/8121@
KAL90+ -UMA	GM@/888VC@/8121@/GM45@/KAL90+_G0@/KAL90+_90@/KAL90_G0_90@/KAL90_H0_90@/KAL90+_PCB@
KAL90+ -Dis	PM@/888VC@/8121@/KAL90+_G0@/KAL90+_90@/KAL90_G0_90@/KAL90_H0_90@/KAL90+_PCB@/PM45@
KALG0 -UMA (GL40)	KALG0@/GM@/888VC@/8121@/GL40@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90@/KALG0_DDR2 PCB RV0 @/KALG0@
KALG0 -Dis	KALG0@/PM@/888VC@/8121@/PM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90@/KALG0_DDR2 PCB RV0 @/KALG0@
KALG0 -UMA (GM45)	KALG0@/GM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90@/KALG0_DDR2 PCB RV0 @/KALG0@
KALG0 -DIS (GM45)	KALG0@/PM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90@/KALG0_DDR2 PCB RV0 @/KALG0@

KALG0 LAN to AR-8131----- 8121@ Change to 8131@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table




Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

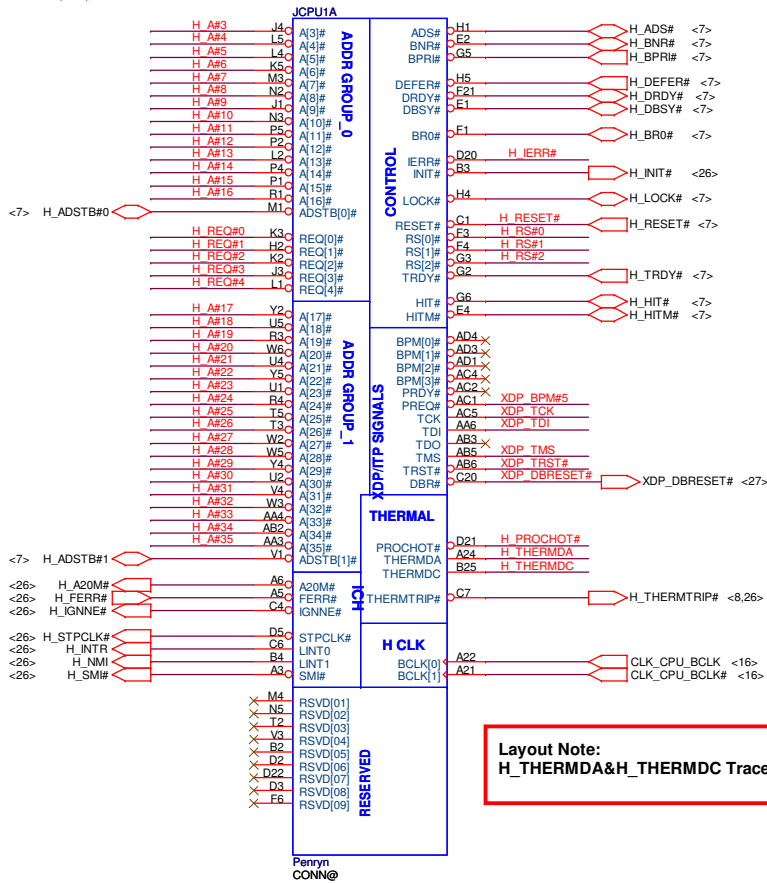
BTO Option Table

BTO Item	BOM Structure
KAL90	KAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@
KAL90-G0	KAL90_G0@
KAL90-H0	KAL90_H0@
KALG0	KALG0@
KALH0	KALH0@
ALC268	268@
	KAL90_90@
	KAL90_H0_G0@
	KAL90+_G0
	KALH0_G0
	KAL90_G0_90@
	KAL90_H0_90@
	KAL90+_PCB@
	KALG0_PCB@

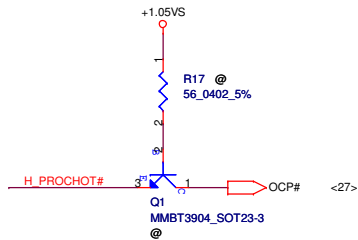
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Notes List		
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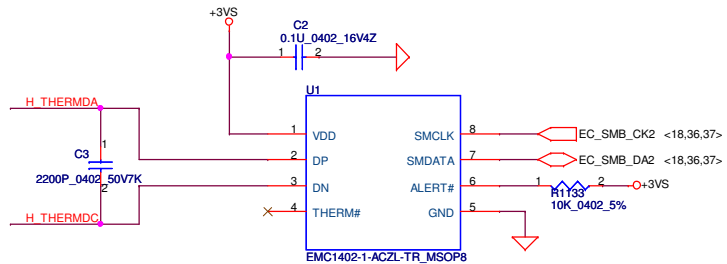
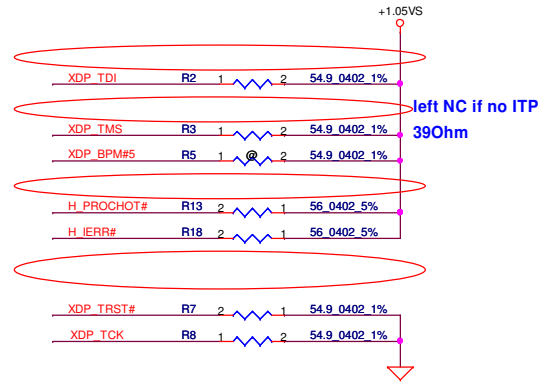
<7> H_A#[3..35]  H_A#[3..35]
 <7> H_REQ#[0..4]  H_REQ#[0..4]
 <7> H_RS#[0..2]  H_RS#[0..2]



BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil



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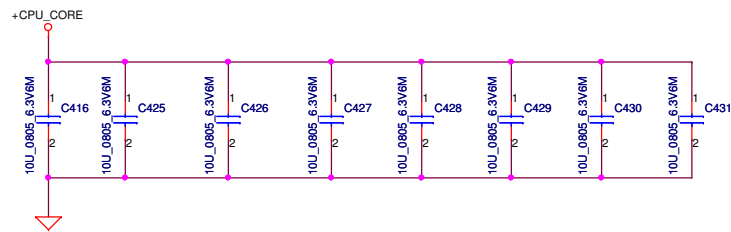
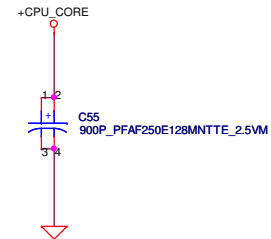
TRACE CLOSELY CPU < 0.5"
 COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
 COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

Trace Close CPU < 0.5"
 Width=4 mil ,
 Spacing: 15mil
 (55Ohm)

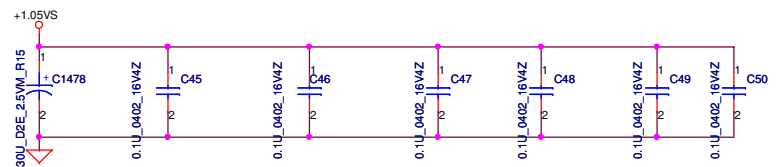
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JCPU1D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
A27	VSS[008]	VSS[089]
B8	VSS[009]	VSS[090]
B11	VSS[010]	VSS[091]
B13	VSS[011]	VSS[092]
B16	VSS[012]	VSS[093]
B19	VSS[013]	VSS[094]
B21	VSS[014]	VSS[095]
B24	VSS[015]	VSS[096]
C3	VSS[016]	VSS[097]
C8	VSS[017]	VSS[098]
C11	VSS[018]	VSS[099]
C14	VSS[019]	VSS[100]
C16	VSS[020]	VSS[101]
C19	VSS[021]	VSS[102]
C2	VSS[022]	VSS[103]
C22	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F3	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
		VSS[163]

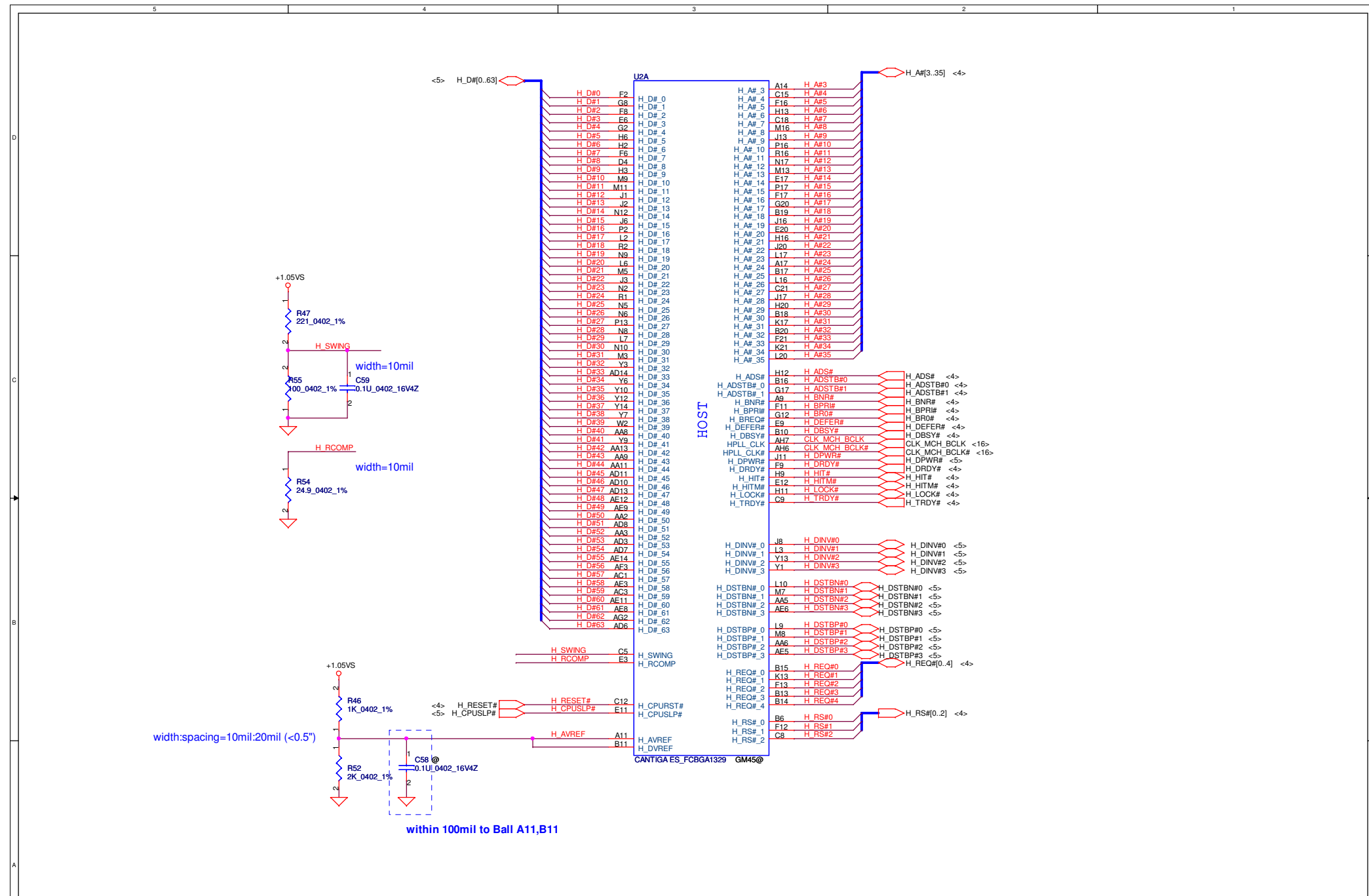
Penryn CONN@



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

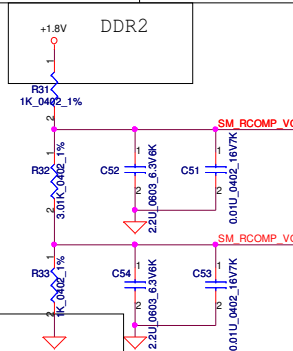


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DDR2



For Cantiga | 80 Ohm

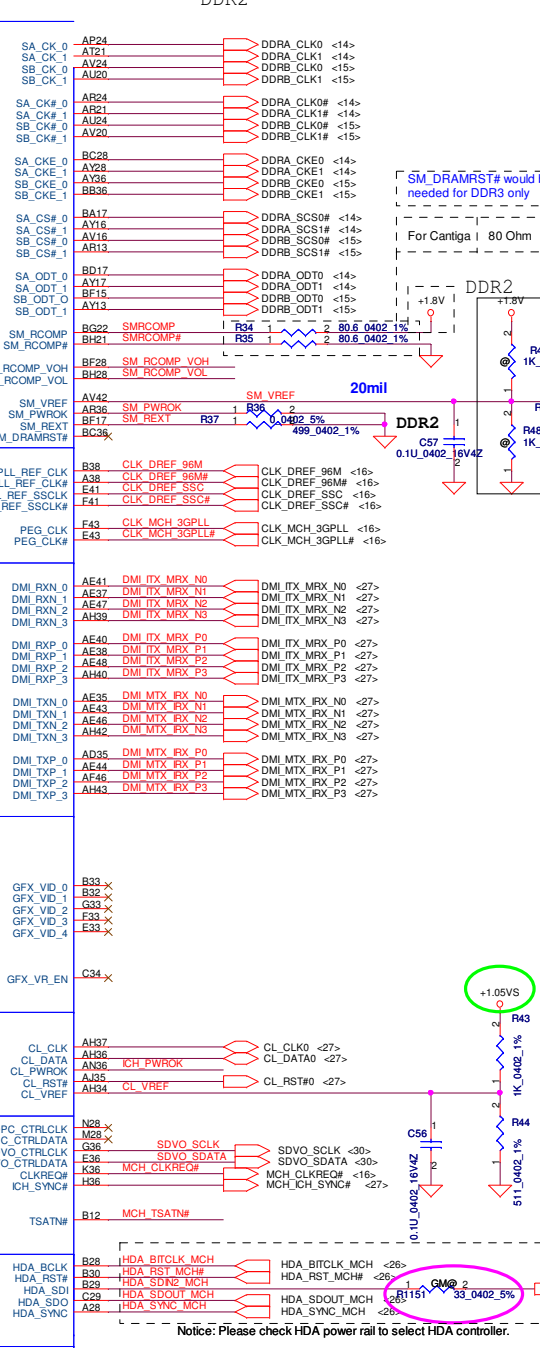
CLK_DREF_96M	R1134	PM	2	0.0402_5%
CLK_DREF_96M#	R1136	PM	2	0.0402_5%
CLK_DREF_SSC	R1137	PM	2	0.0402_5%
CLK_DREF_SSC#	R1138	PM	2	0.0402_5%

as close as possible to the related balls

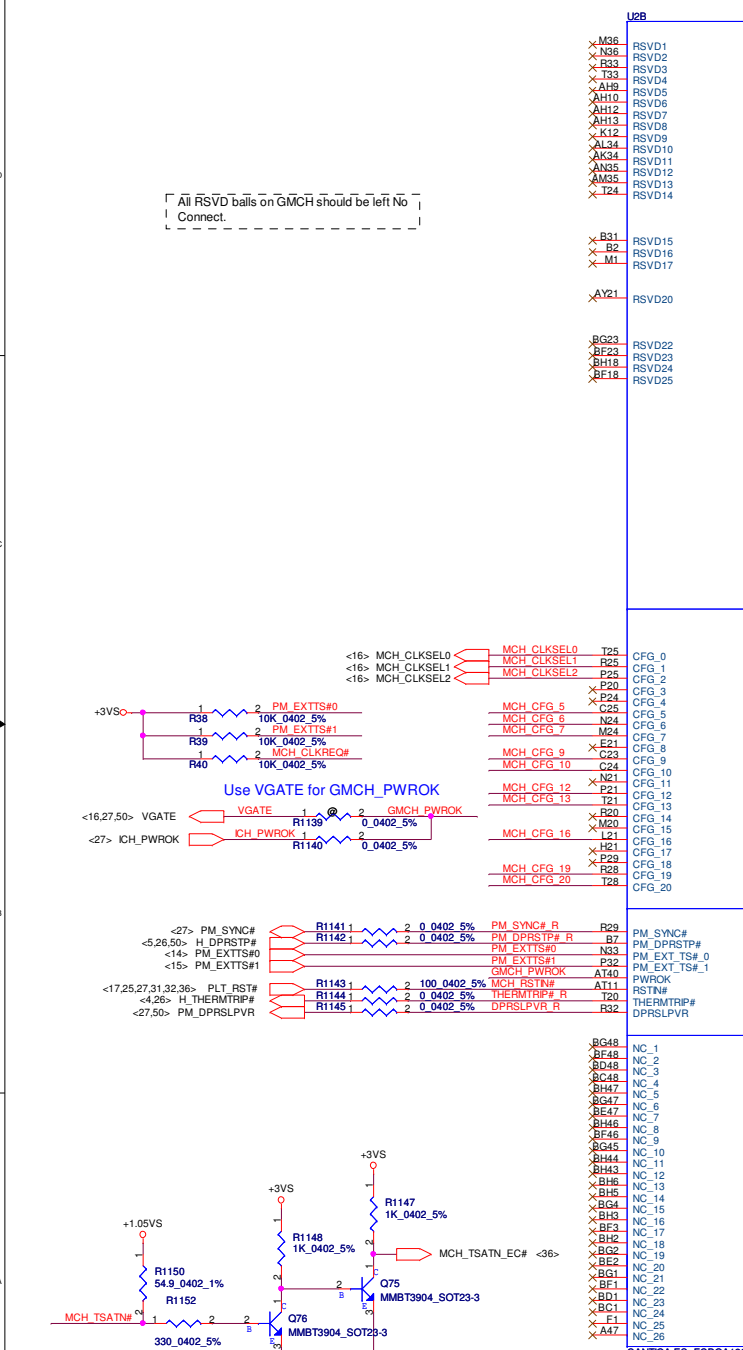
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simul.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIe disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

RSVD
DDR CLK/ CONTROL/ COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
HDA



Notice: Please check HDA power rail to select HDA controller.



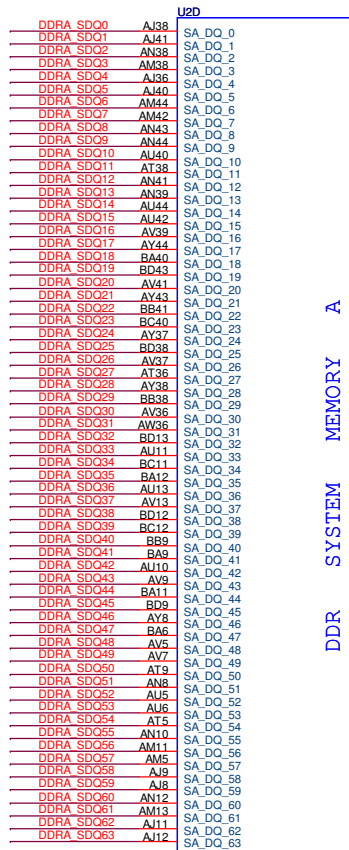
All RSVD balls on GMCH should be left No Connect.

Use VGATE for GMCH_PWROK

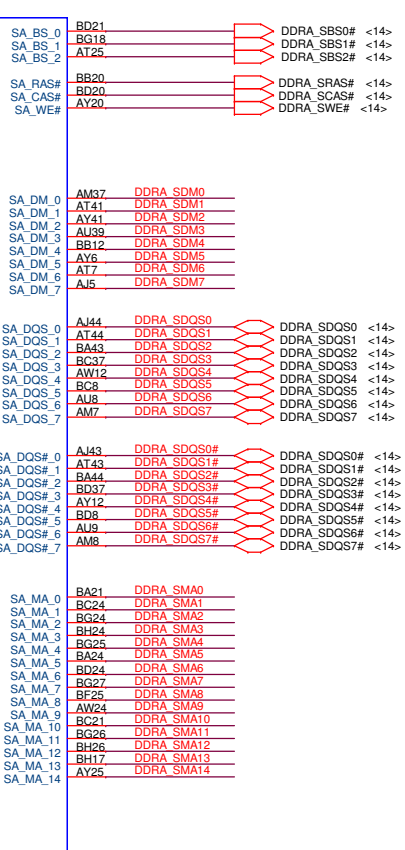
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<14> DDRA_SDQ[0..63] <--> DDRA_SDQ[0..63]
 <14> DDRA_SDM[0..7] <--> DDRA_SDM[0..7]
 <14> DDRA_SMA[0..14] <--> DDRA_SMA[0..14]

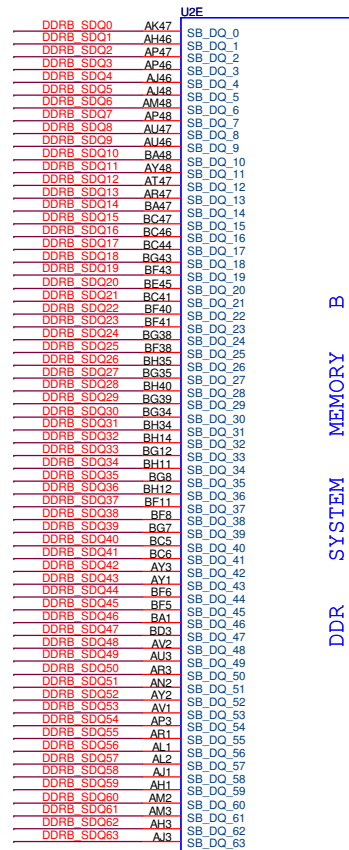
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 <15> DDRB_SDM[0..7] <--> DDRB_SDM[0..7]
 <15> DDRB_SMA[0..14] <--> DDRB_SMA[0..14]



DDR SYSTEM MEMORY A



CANTIGA ES_FCBGA1329
GM45@

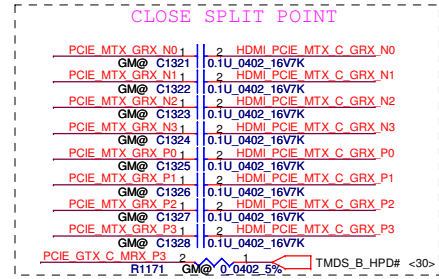


DDR SYSTEM MEMORY B

CANTIGA ES_FCBGA1329
GM45@

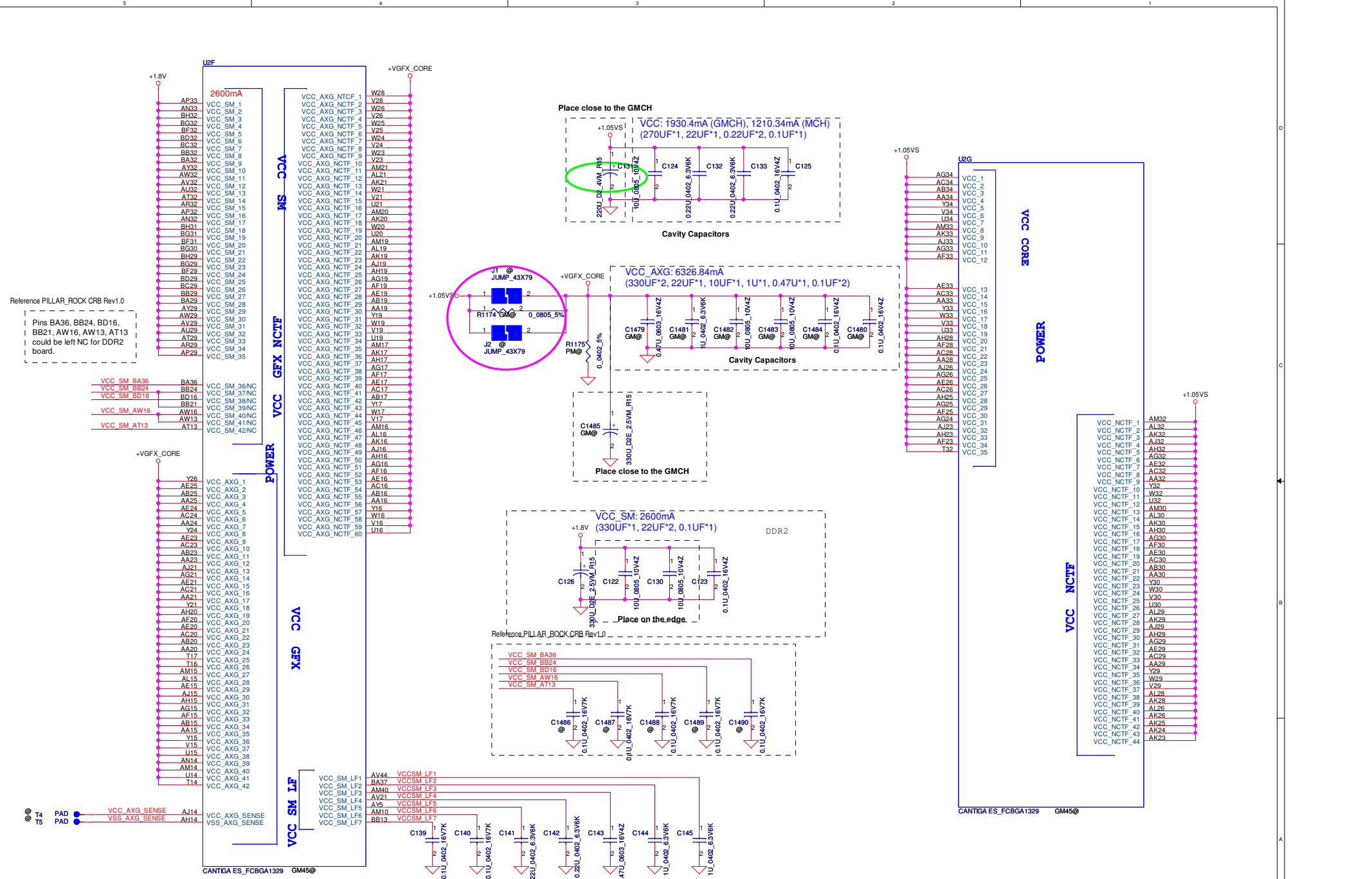


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Size	Document Number	Date		Sheet	Rev
B	KAL90	Monday, April 27, 2009		9	0.1
				of	53



Component	Value	PCIE MTX C GRX	PCIE MTX C GRX
C1289	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N0
C1290	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N1
C1291	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N2
C1292	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N3
C1293	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N4
C1294	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N5
C1295	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N6
C1296	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N7
C1297	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N8
C1298	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N9
C1299	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N10
C1300	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N11
C1301	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N12
C1302	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N13
C1303	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N14
C1304	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N15
C1305	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P0
C1306	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P1
C1307	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P2
C1308	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P3
C1309	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P4
C1310	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P5
C1311	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P6
C1312	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P7
C1313	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P8
C1314	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P9
C1315	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P10
C1316	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P11
C1317	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P12
C1318	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P13
C1319	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P14
C1320	2	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P15

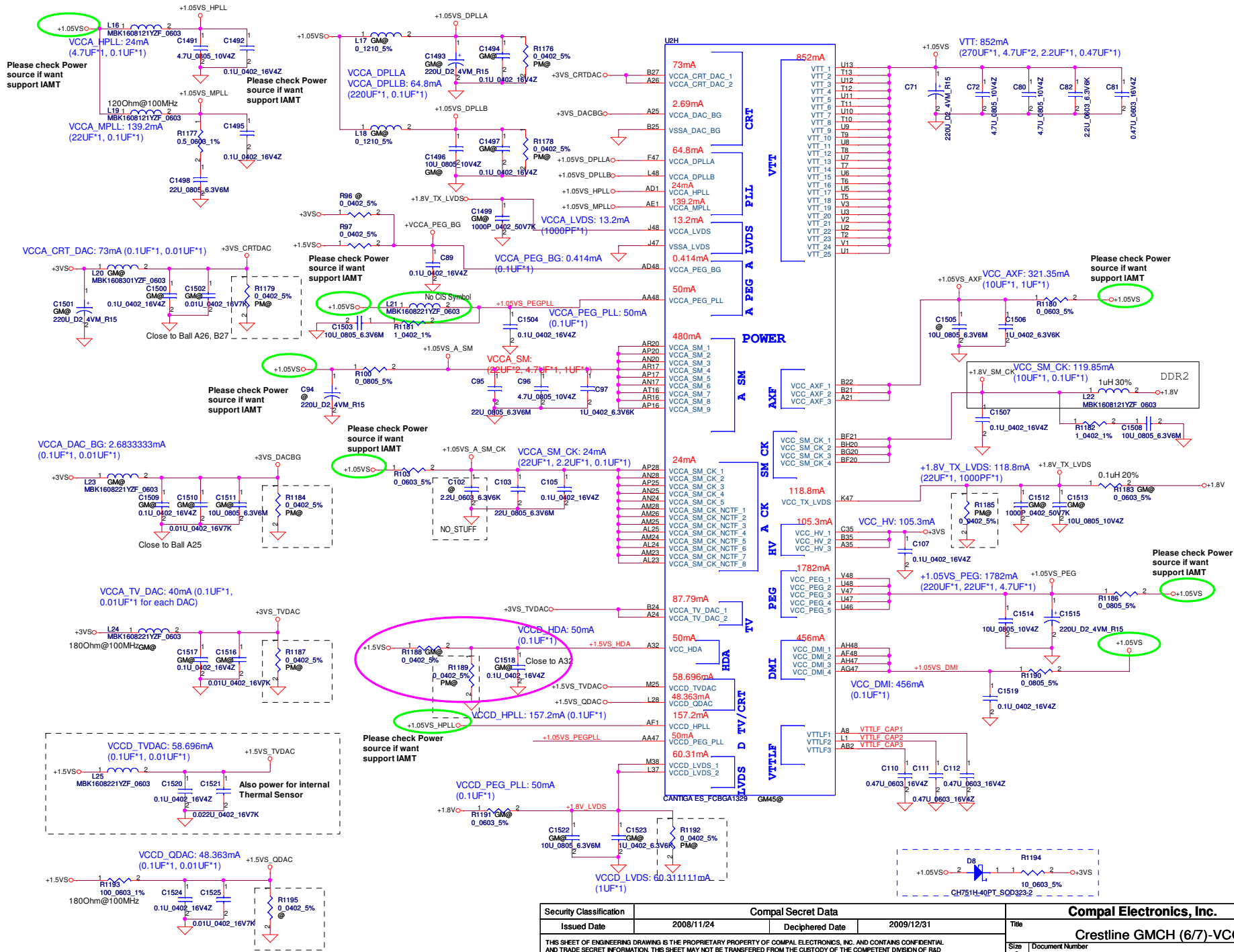
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	Cantiga GMCH(4/7)-VGA/LVDS/TV
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Size	Custom	Document Number	KALH0/KALGO/KAL90+	Rev	1.0
Date	Monday, April 27, 2009	Sheet	10	of	53



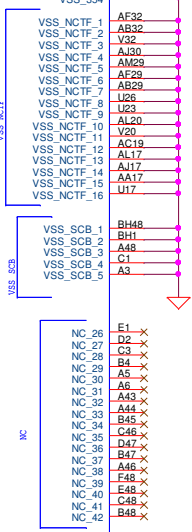
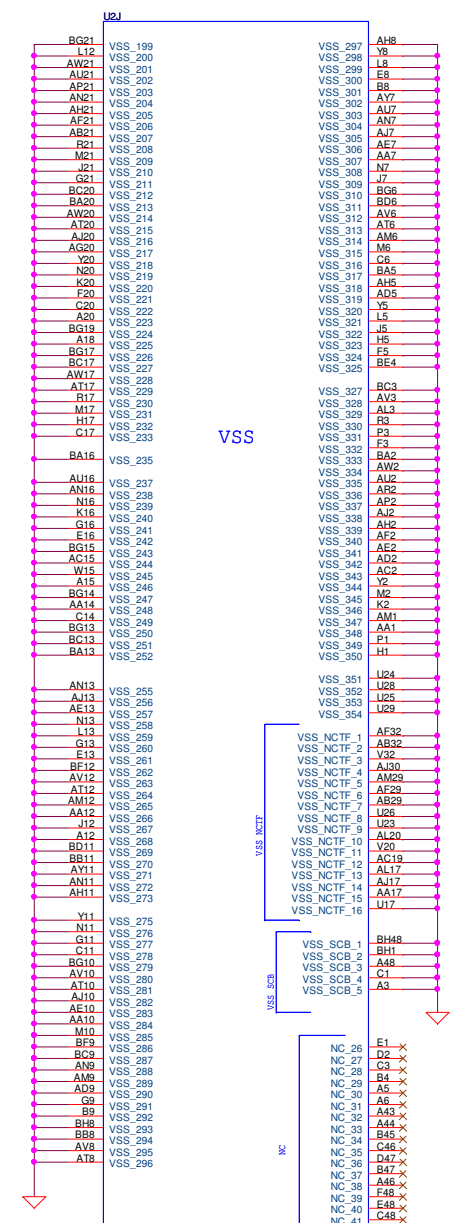
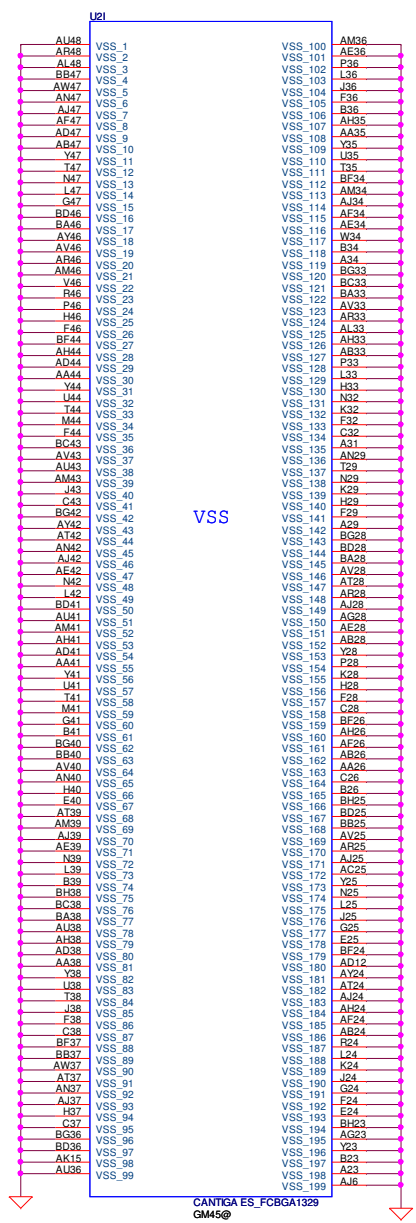
Security Classification		Compal Secret Data	
Issued Date	2008/11/24	Deciphered Date	2009/12/31

Compal Electronics, Inc.			
Cantiga GMCH(5/7)-VCC			
Size	Document Number	Rev	
Customer	KALHO/KALGO/KAL90+	1.0	
Date:	Monday, April 27, 2009	Sheet	11 of 53

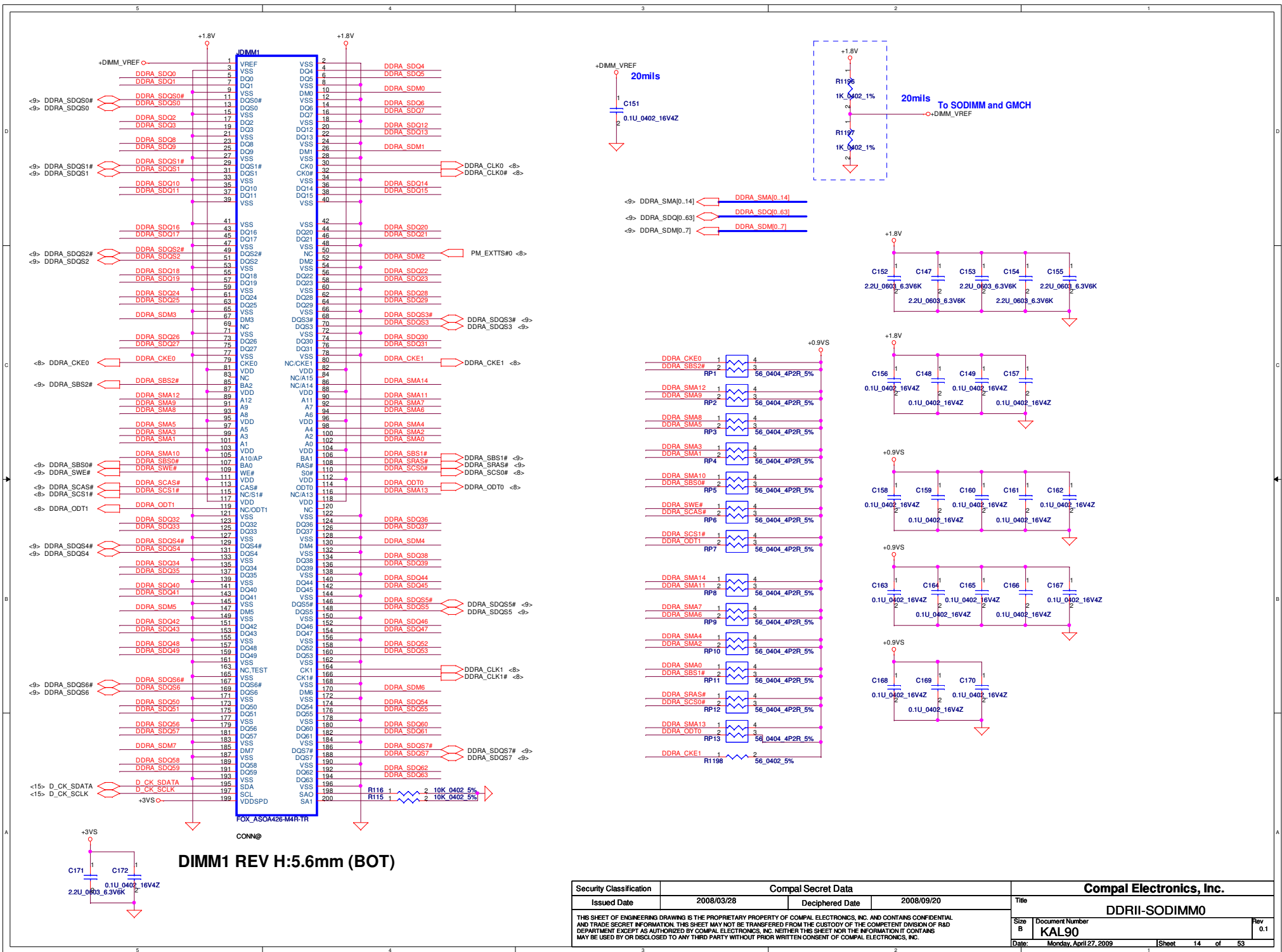
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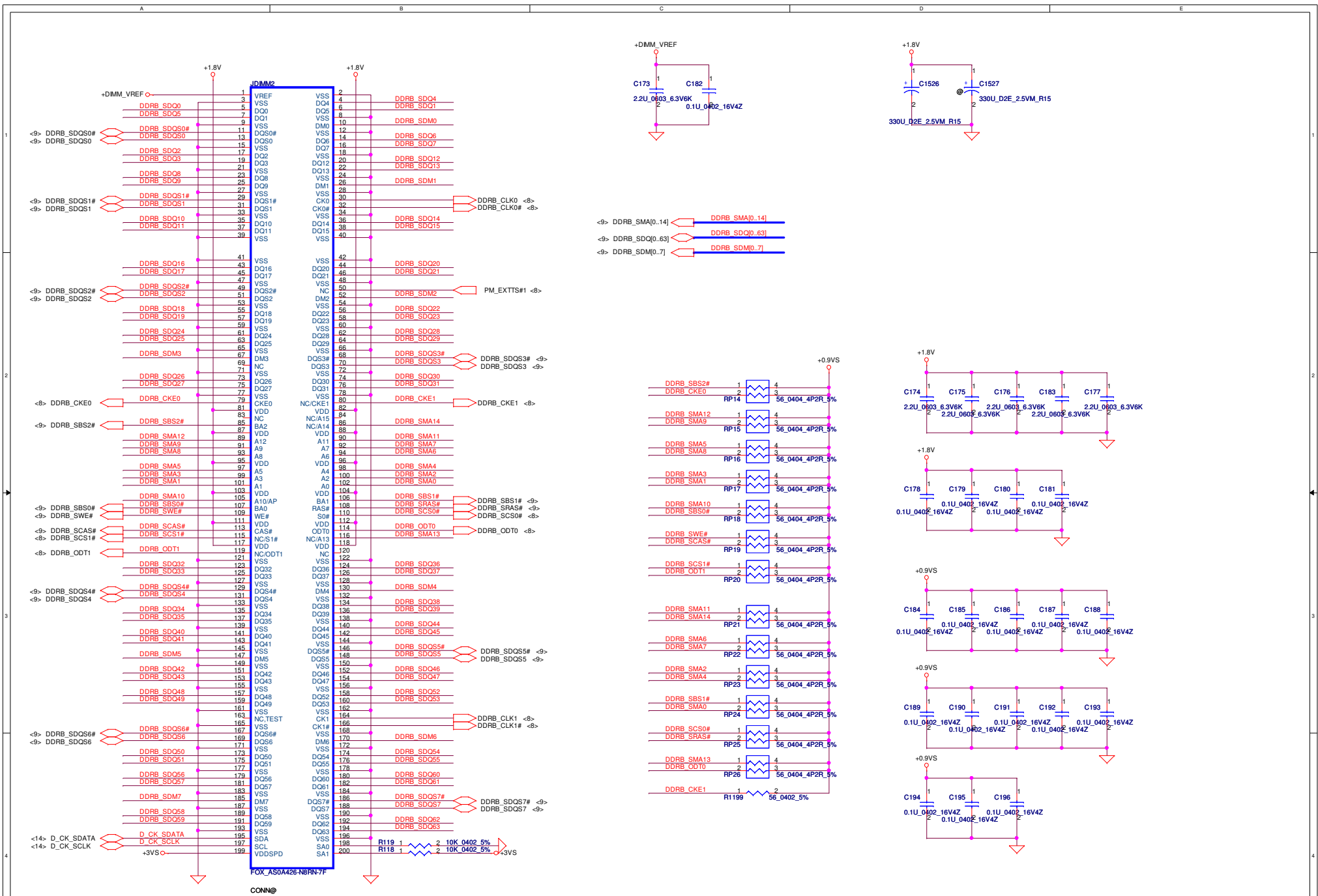


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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Crestline GMCH (6/7)-VCC	
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Cantiga GMCH(1/7)-GTL	
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				KALHO/KALGO/KAL90+	1.0
Date: Monday, April 27, 2009				Sheet	13 of 53



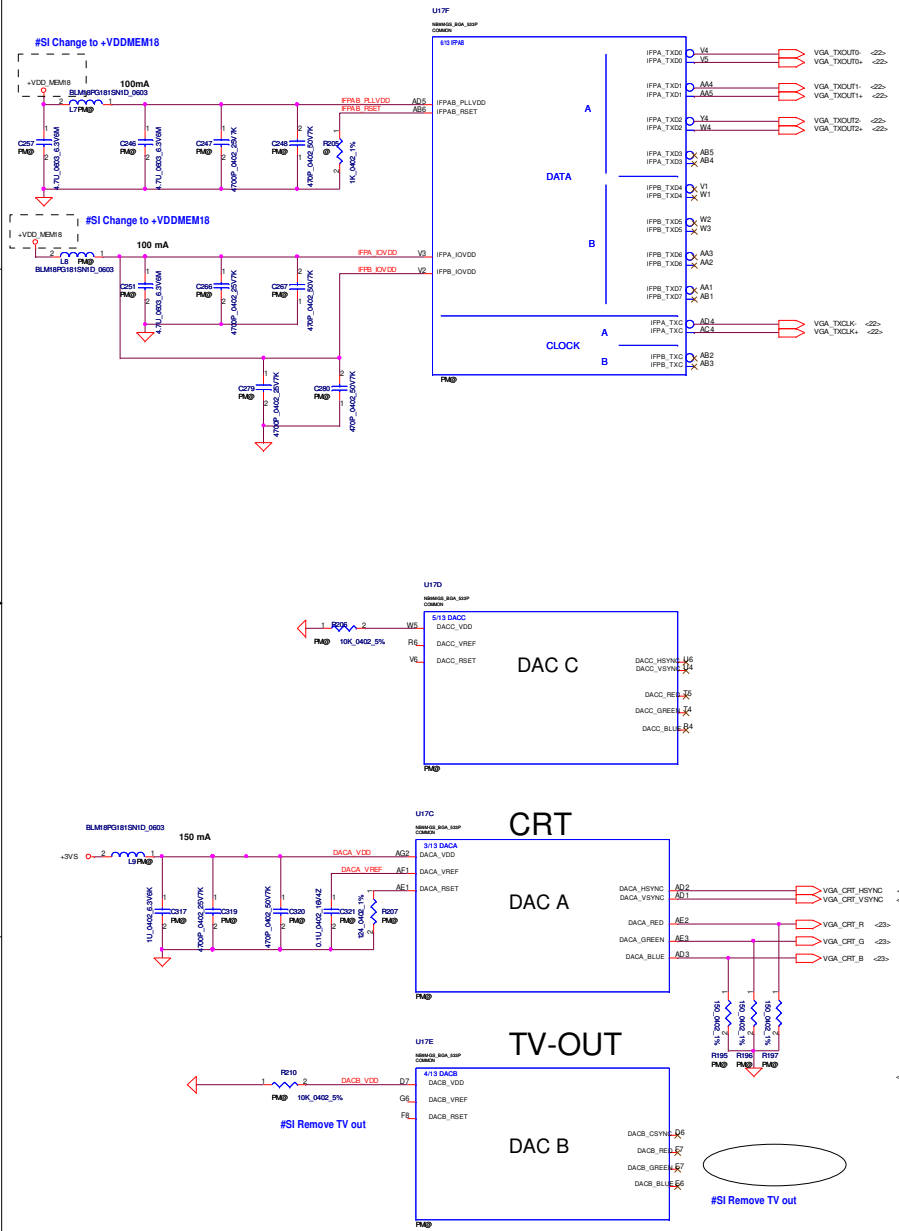


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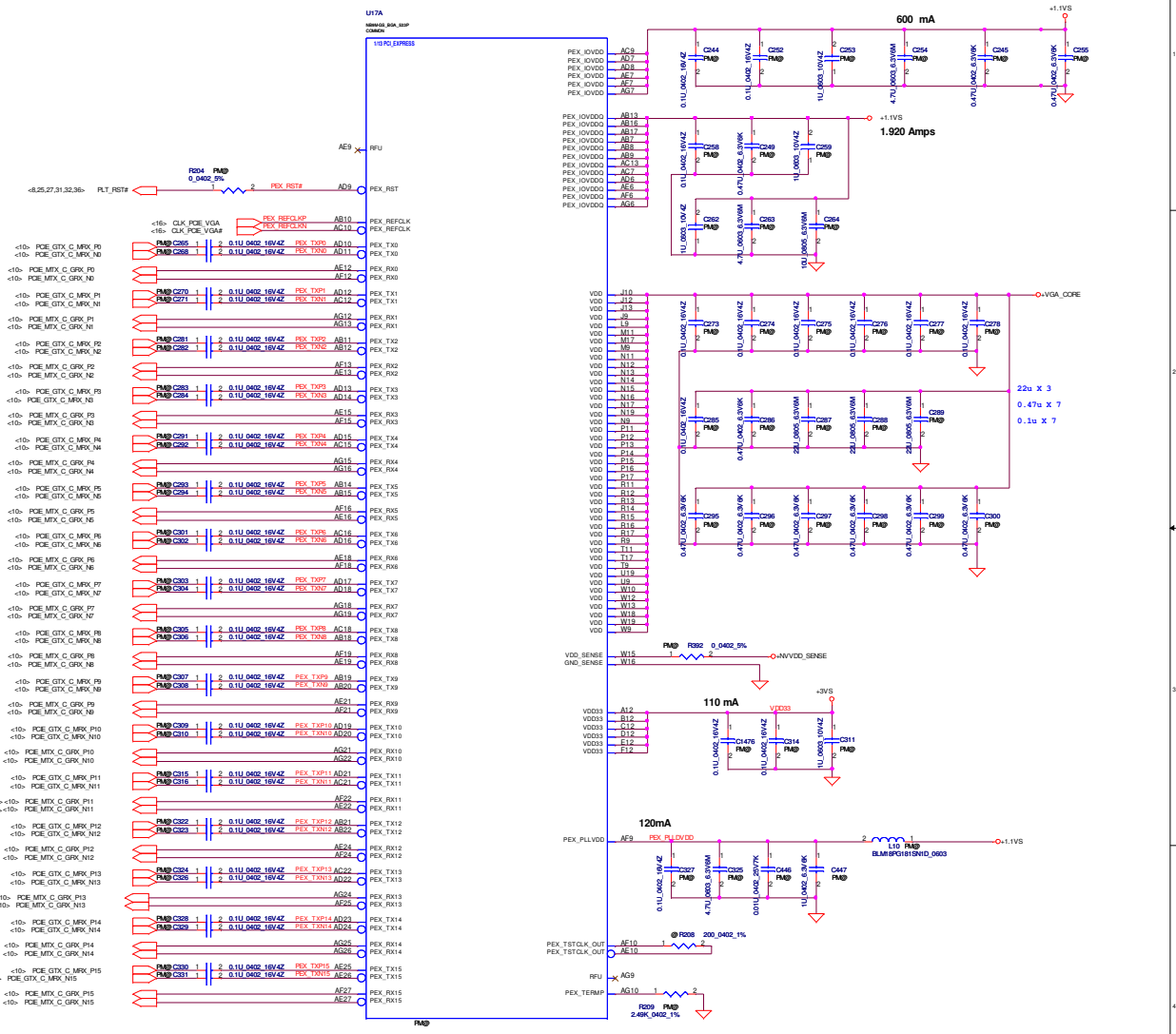
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Issued Date	2008/03/28	Deciphered Date	2008/09/20
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Compal Electronics, Inc.		
Title DDRII-SODIMM1		
Size B	Document Number KAL90	Rev 0.1
Date:	Monday, April 27, 2009	Sheet 15 of 53

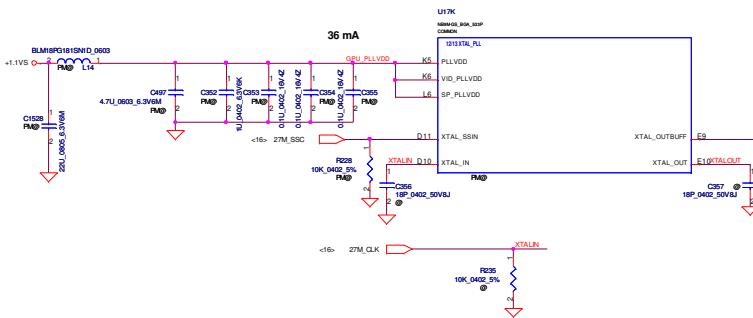
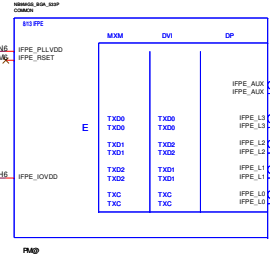
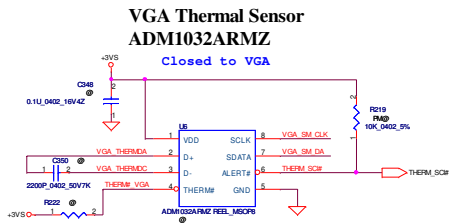
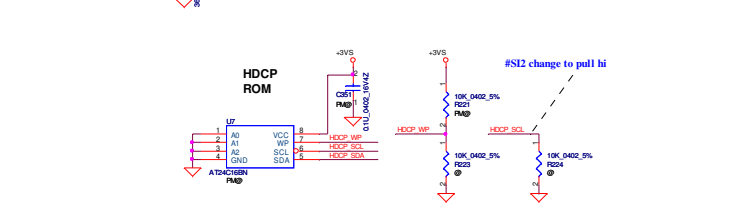
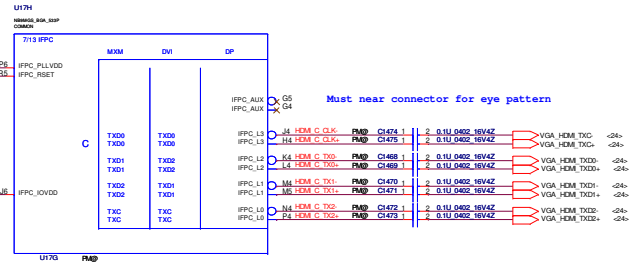
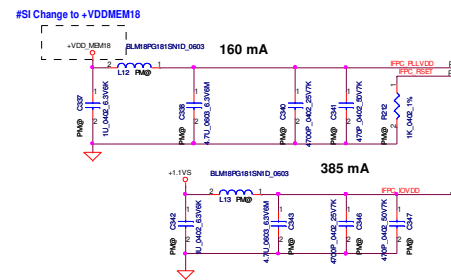
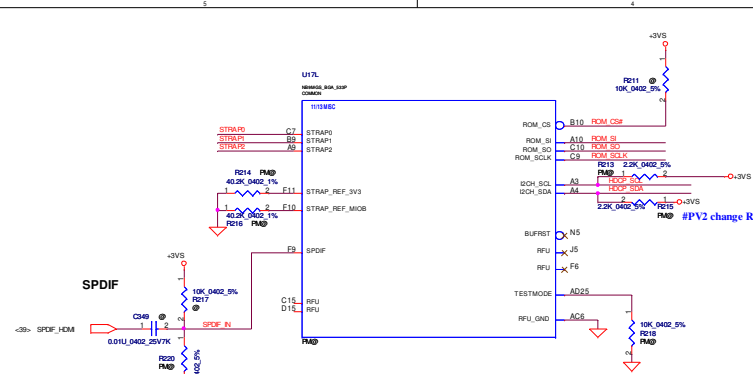
LVDS & DAC Interface



PEG Interface



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Issued Date	2008/11/24	Deciphered Date	
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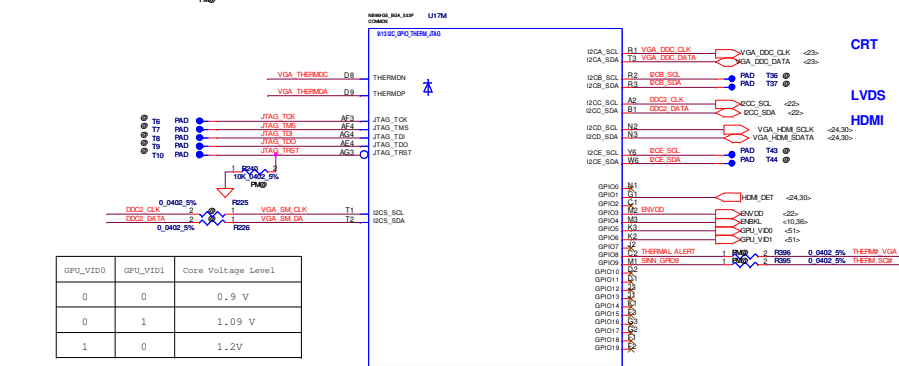
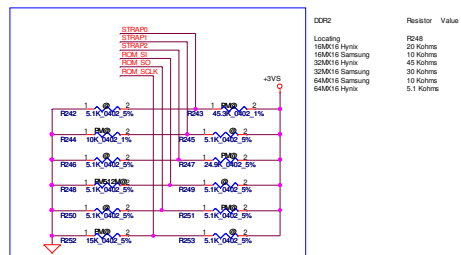


GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VIDO
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VIDO
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	SL SYNC0
GPIO11	OUT	N/A	AC Detect
GPIO12	IN	N/A	PS Control
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



Straps

MULTI LEVEL STRAPS



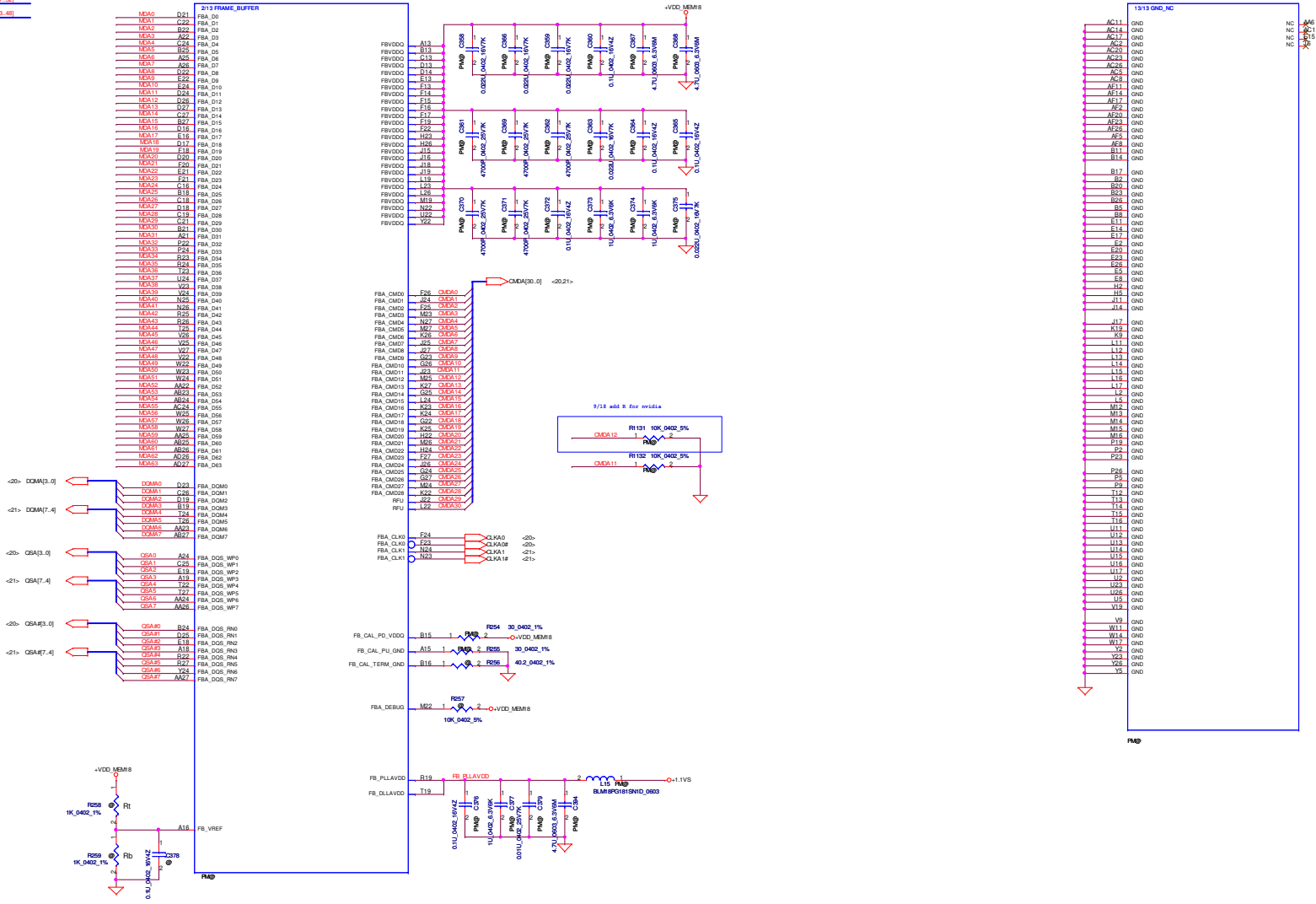
GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.9 V
0	1	1.09 V
1	0	1.2V

Security Classification	Compal Secret Data	
Issued Date	2008/11/24	Deciphered Date
2008/11/24		2009/12/31

Compal Electronics, Inc.
Straps & HDMI
 Drawing Number: **KALHWALG00KAL90**
 Date: **Monday, April 27, 2009** | Sheet: **18** of **33**

VRAM Interface

- <20> MDA[15..0] \leftarrow MDA[15..0]
- <20> MDA[31..16] \leftarrow MDA[31..16]
- <21> MDA[47..32] \leftarrow MDA[47..32]
- <21> MDA[63..48] \leftarrow MDA[63..48]

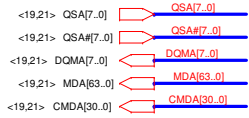


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Rev	Document Number	Rev		
001	KAL2HWALGND190+	1.0		
Date	Rev. April 27, 2009	Issue	19	of 50

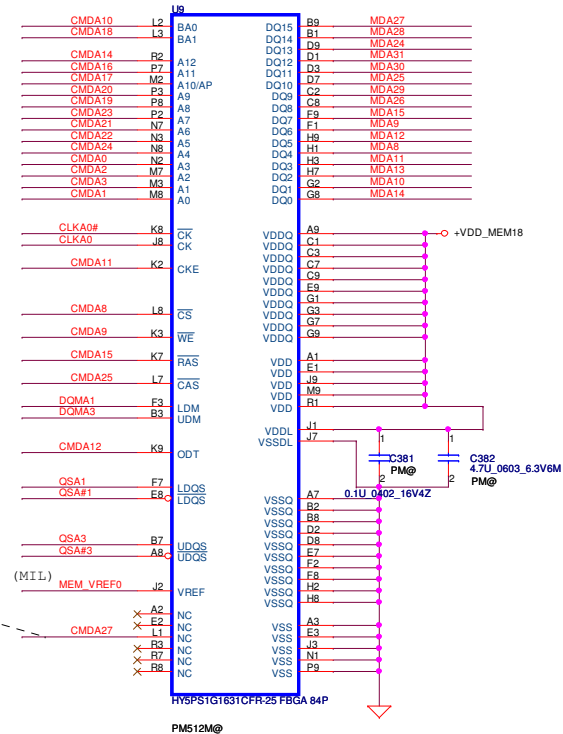
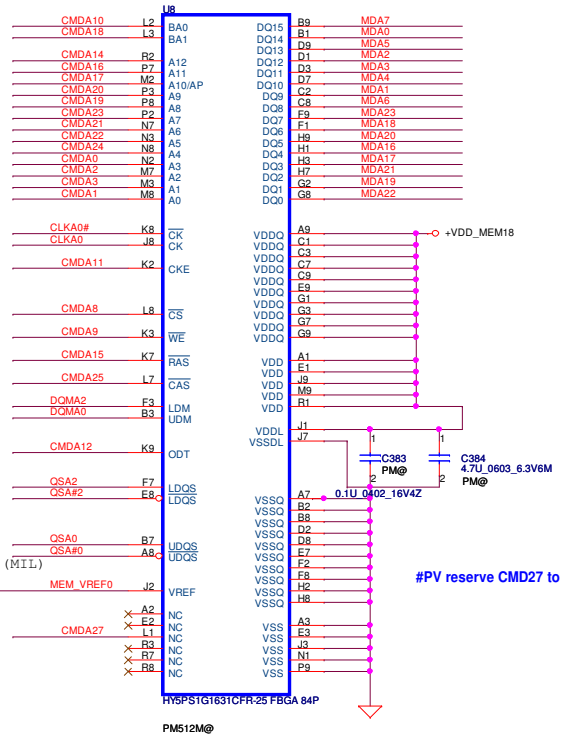
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

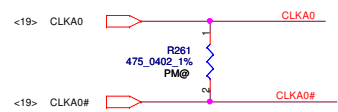
64Mx16 DDR2 400MHz*4==>512MB



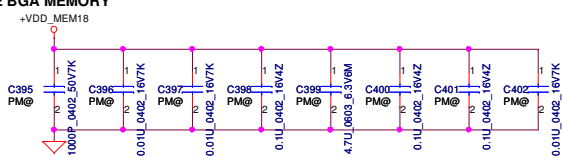
DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



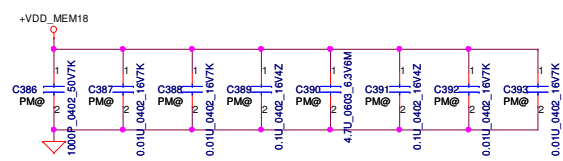
#PV reserve CMD27 to suport 64M x 16



DDR2 BGA MEMORY



DDR2 BGA MEMORY

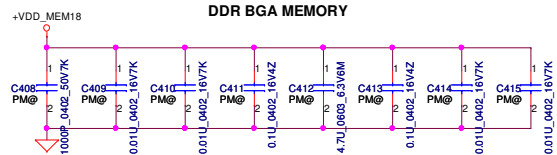
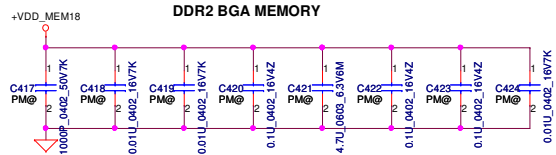
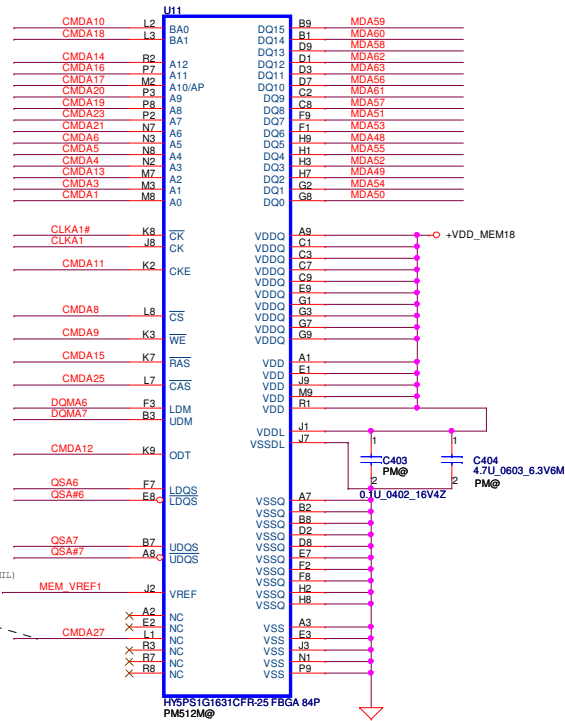
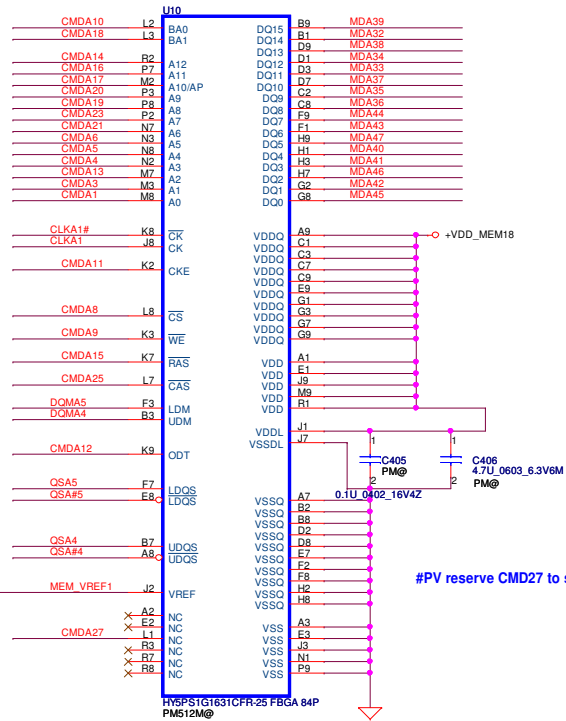
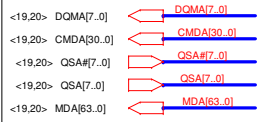


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					KAL90
Date:	Monday, April 27, 2009	Sheet	7	of	16

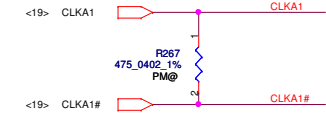
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

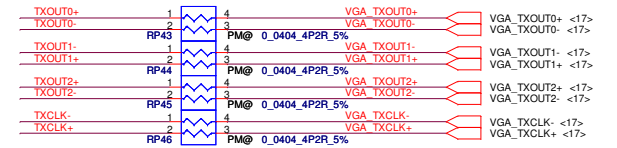
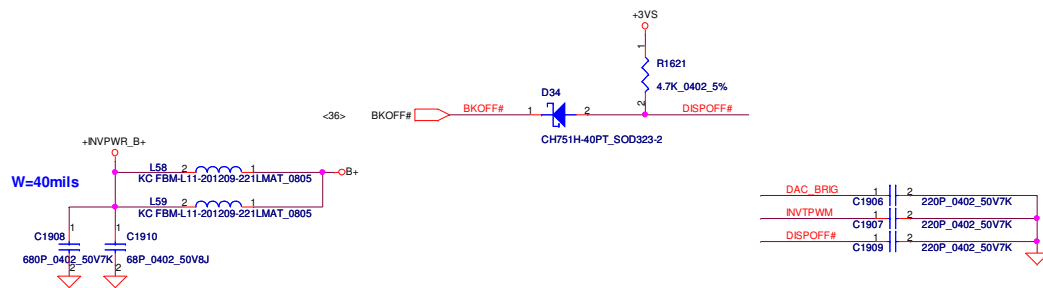
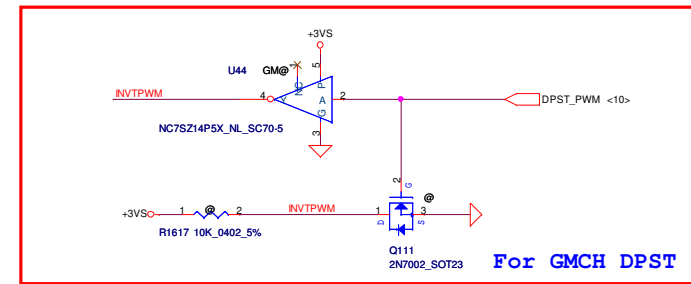
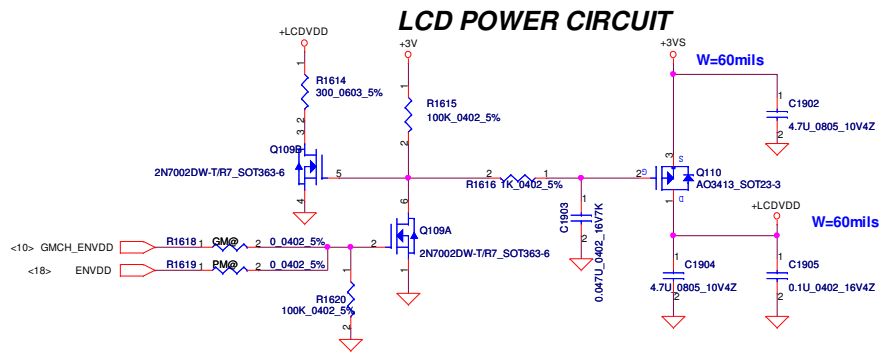
64Mx16 DDR2 400MHz*4==>512MB



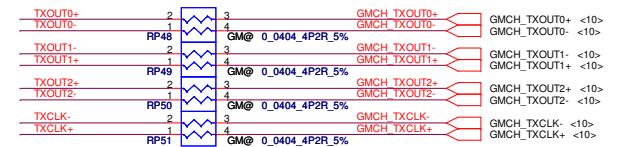
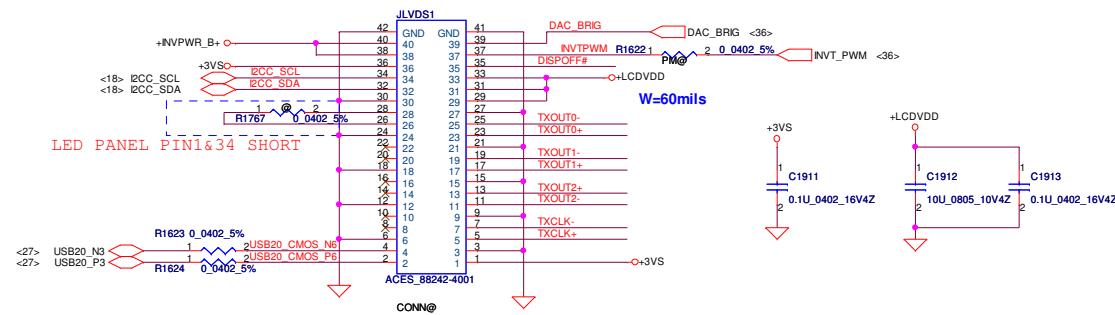
DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	A5
CMD23	A7	A7
CMD24	A4	A4
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



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Date: Monday, April 27, 2009				Sheet 8 of 16

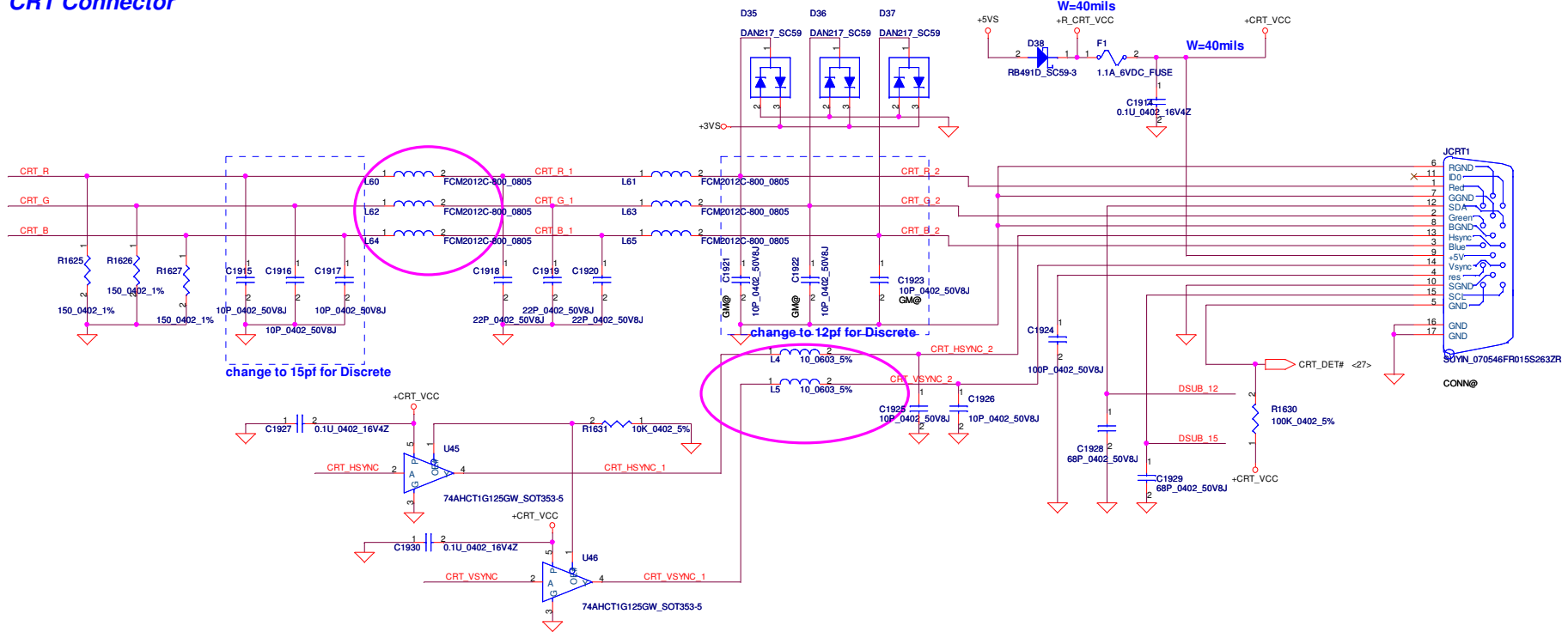


LCD/PANEL BD. Conn.

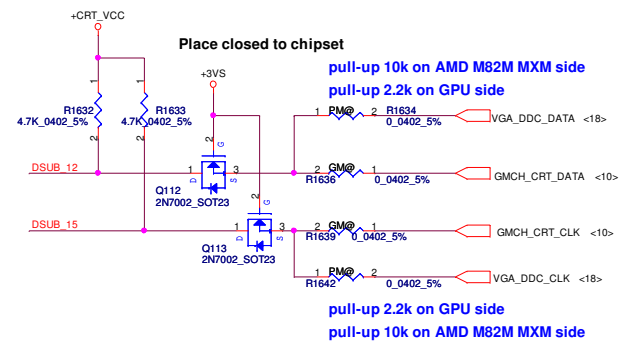


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				LVDS Connector
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				Sheet 22 of 53

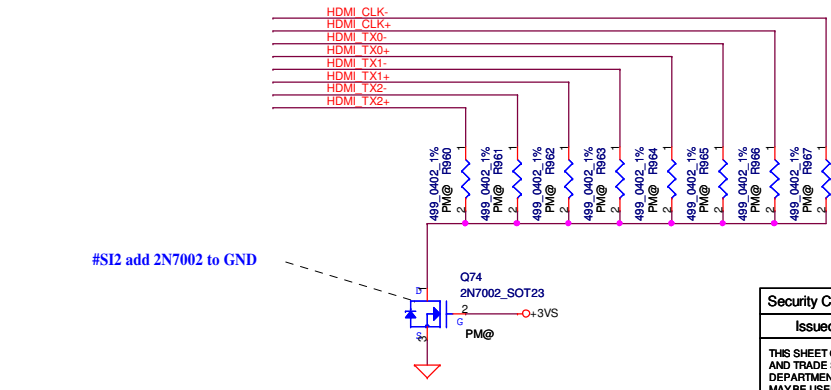
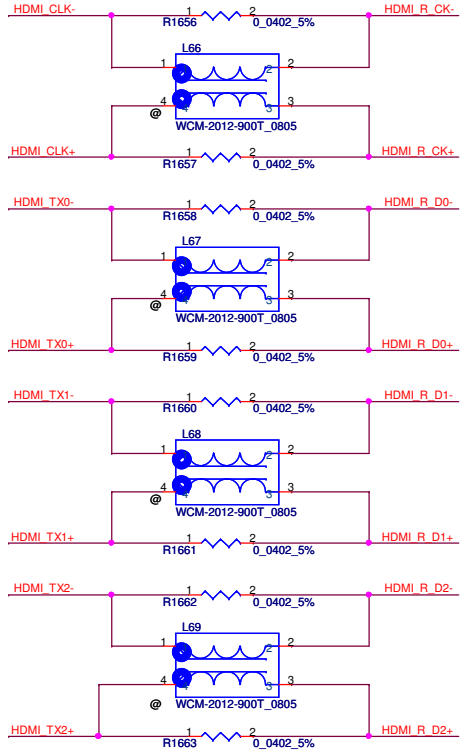
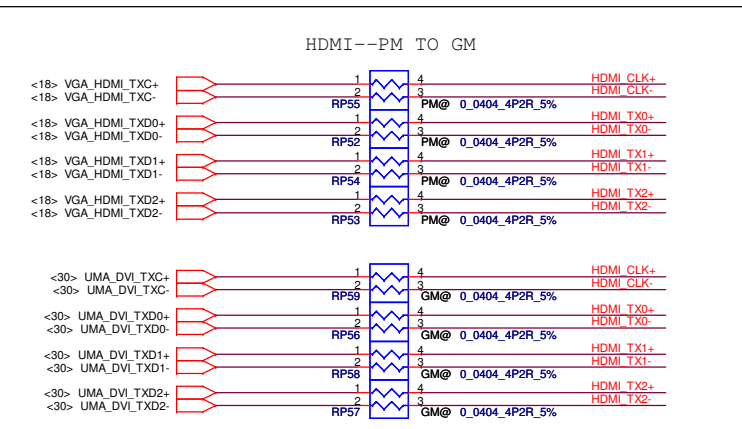
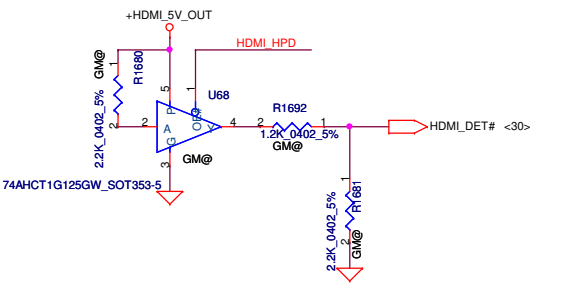
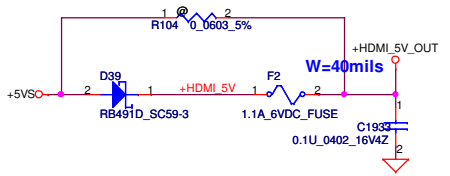
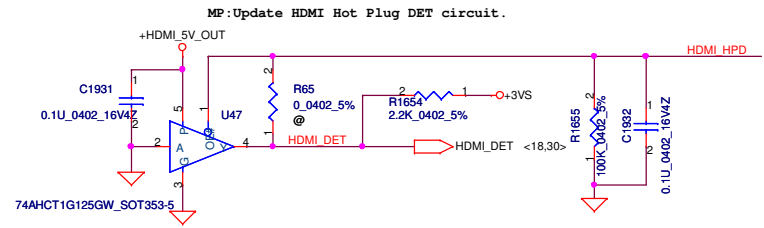
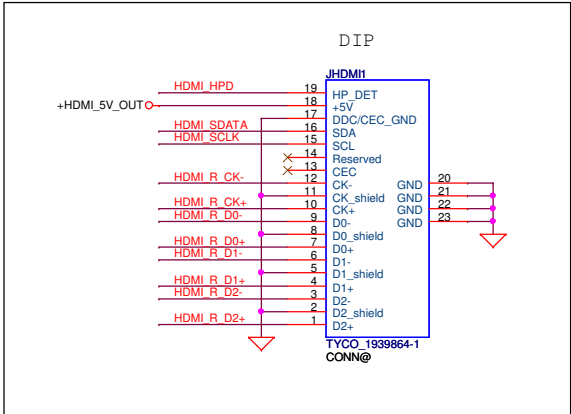
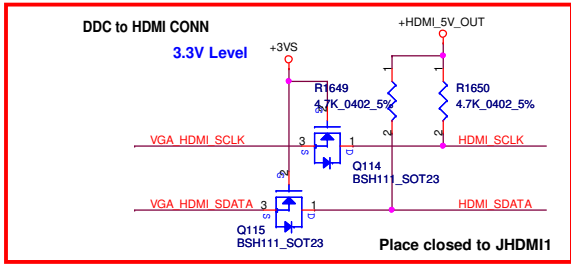
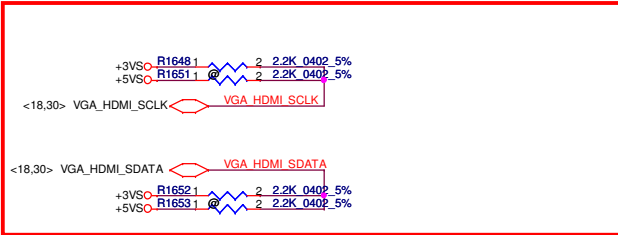
CRT Connector



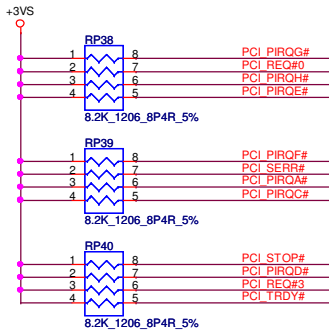
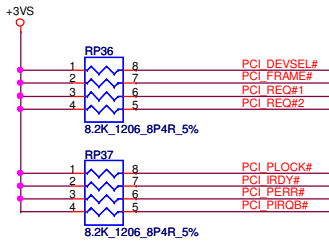
<10>	GMCH_CRT_VSYNC	R1635	1	GM@	2	30.1_0402_1%	CRT_VSYNC
<10>	GMCH_CRT_HSYNC	R1637	1	GM@	2	30.1_0402_1%	CRT_HSYNC
<10>	GMCH_CRT_B	R1638	1	GM@	2	0_0402_5%	CRT_B
<10>	GMCH_CRT_G	R1640	1	GM@	2	0_0402_5%	CRT_G
<10>	GMCH_CRT_R	R1641	1	GM@	2	0_0402_5%	CRT_R
<17>	VGA_CRT_VSYNC	R1643	1	RM@	2	0_0402_5%	CRT_VSYNC
<17>	VGA_CRT_HSYNC	R1644	1	RM@	2	0_0402_5%	CRT_HSYNC
<17>	VGA_CRT_B	R1645	1	RM@	2	0_0402_5%	CRT_B
<17>	VGA_CRT_G	R1646	1	RM@	2	0_0402_5%	CRT_G
<17>	VGA_CRT_R	R1647	1	RM@	2	0_0402_5%	CRT_R



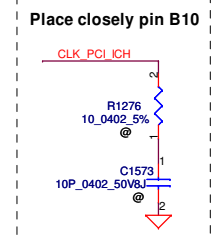
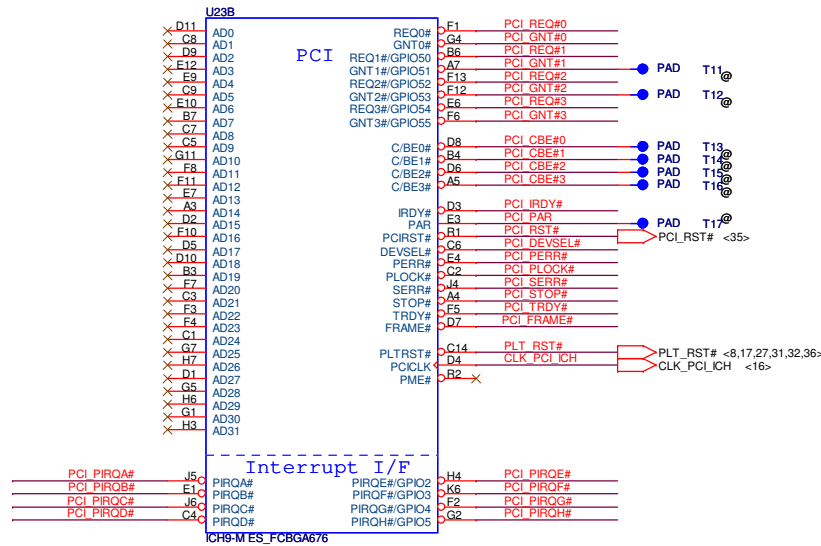
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	CRT Connector	
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Size B	Document Number	Date		Sheet	Rev
	KALHO/KALGO/KAL90+	Monday, April 27, 2009		23	1.0
				of	53



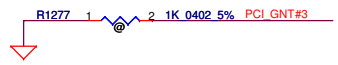
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
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Size	Document Number	Date		Rev	1.0
Custom	KALH0/KALGO/KAL90+	Monday, April 27, 2009		Sheet	24 of 53



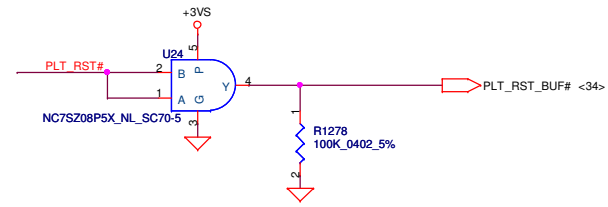
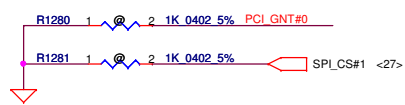
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)



A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



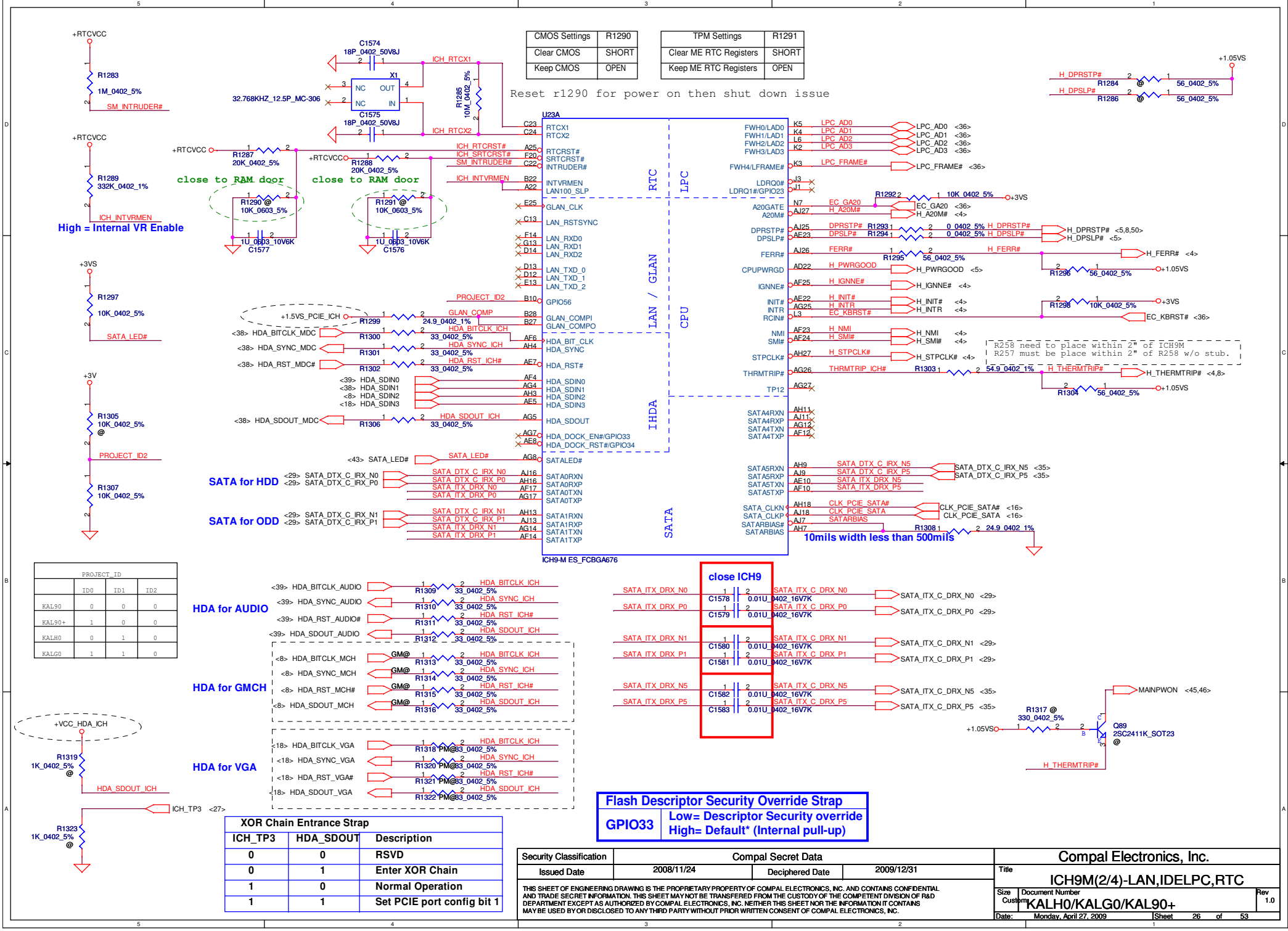
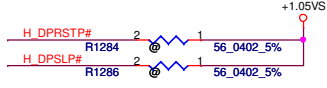
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



CMOS Settings		R1290	
Clear CMOS		SHORT	
Keep CMOS		OPEN	

TPM Settings		R1291	
Clear ME RTC Registers		SHORT	
Keep ME RTC Registers		OPEN	

Reset r1290 for power on then shut down issue



close to RAM door

close to RAM door

High = Internal VR Enable

SATA for HDD

SATA for ODD

HDA for AUDIO

HDA for GMCH

HDA for VGA

close ICH9

10mils width less than 500mils

PROJECT_ID			
ID0	ID1	ID2	
KAL90	0	0	0
KAL90+	1	0	0
KAL80	0	1	0
KAL80+	1	1	0

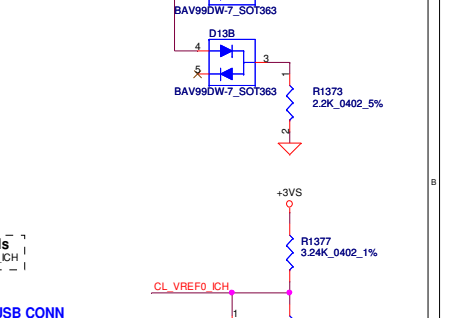
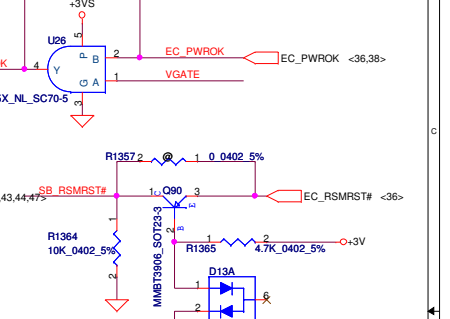
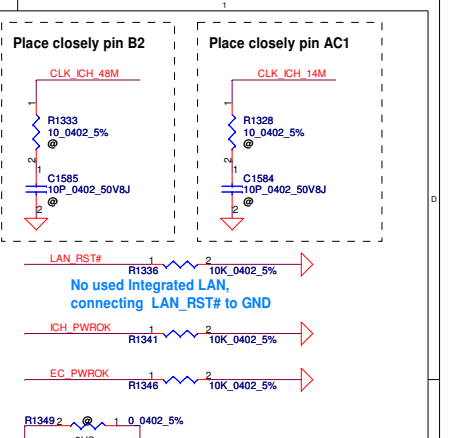
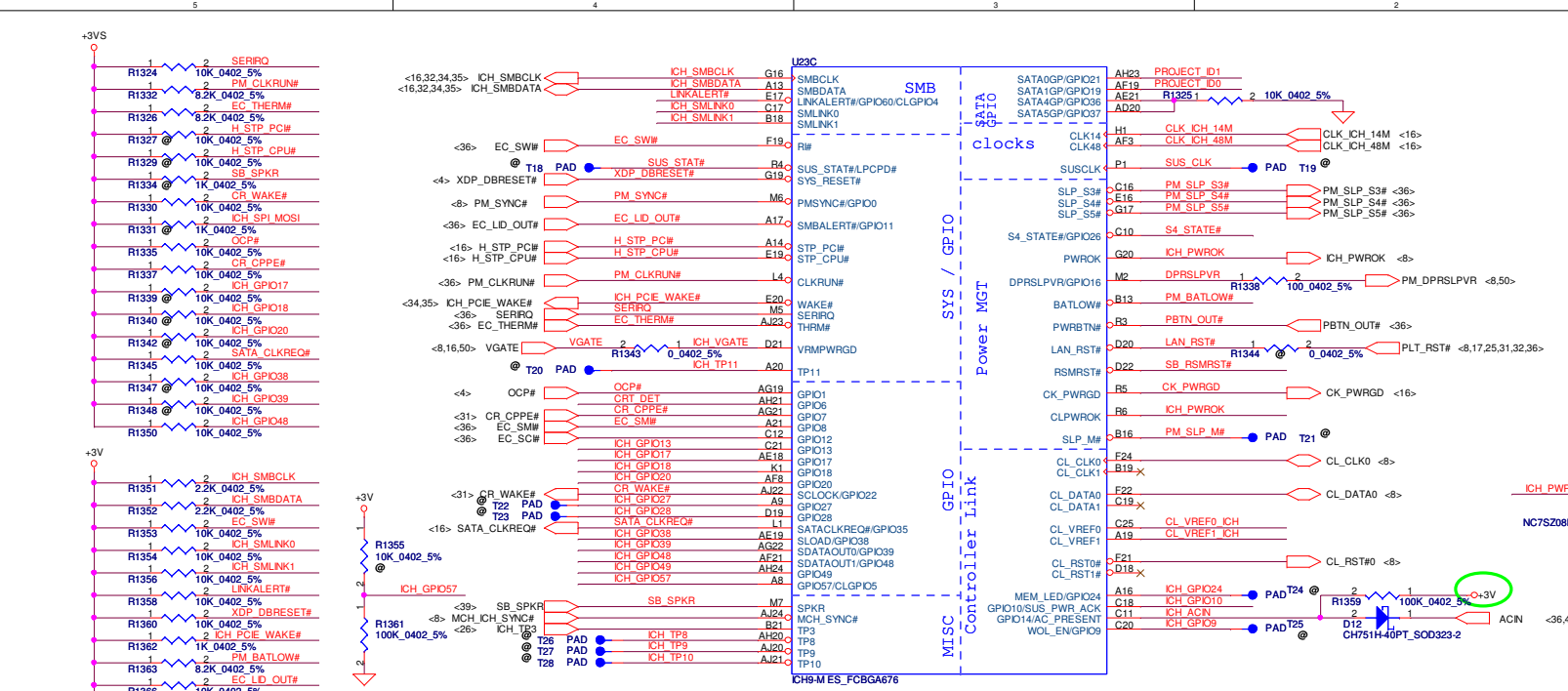
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIe port config bit 1

Flash Descriptor Security Override Strap
GPIO33
Low= Descriptor Security override
High= Default* (Internal pull-up)

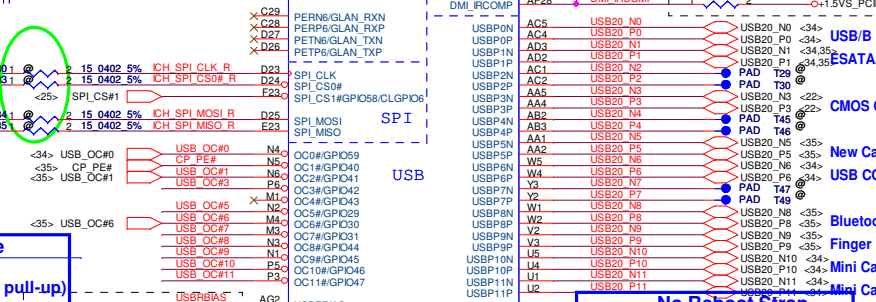
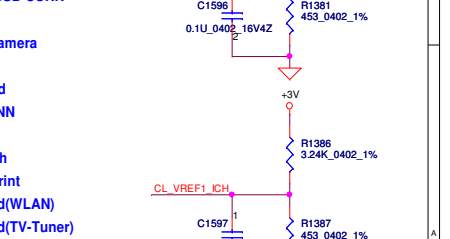
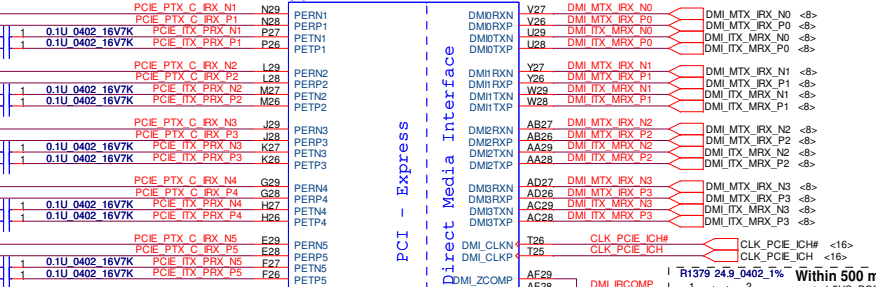
Security Classification	Compal Secret Data	
Issued Date	2008/11/24	Deciphered Date
		2009/12/31

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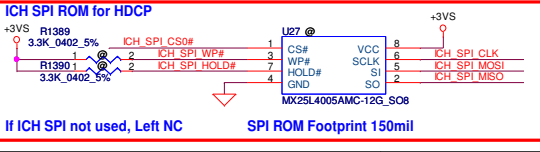
Compal Electronics, Inc.			
Title			
ICH9M(2/4)-LAN, IDELPC, RTC			
Size	Document Number		Rev
Custom	KALH0/KALG0/KAL90+		1.0
Date:	Monday, April 27, 2009	Sheet	26 of 53



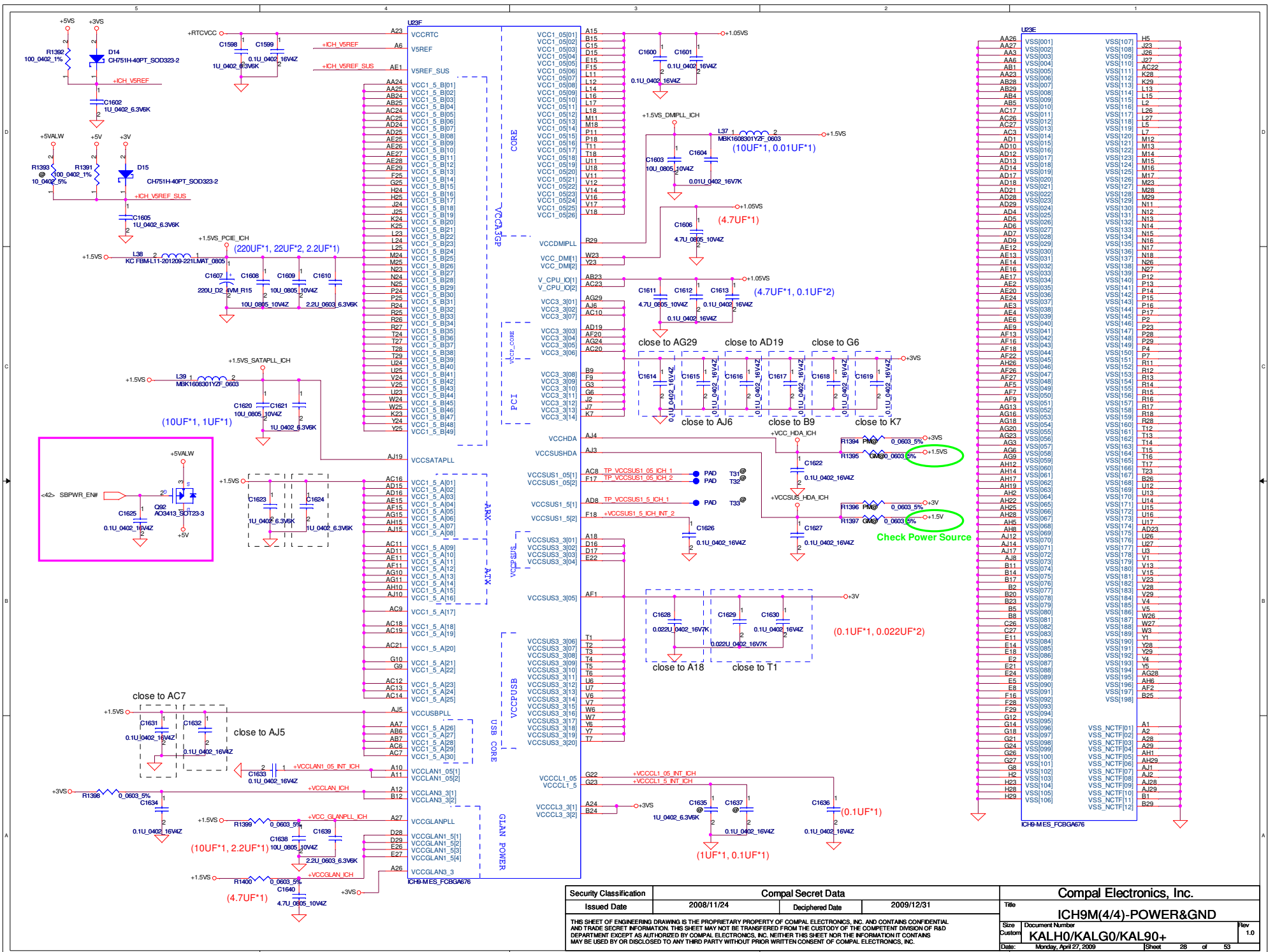
- For Express Card**
- For Wireless LAN**
- For PCIE LAN**
- For Robson2**
- For Card Reader**



<p>Internal TPM Strap</p> <p>SPI_MOSI Low= Disable* High= iTPM enable by MCH strap</p>	<p>DMI Termination Voltage</p> <p>GPIO49 Low= Desktop used High= Mobile* (Internal pull-up)</p>
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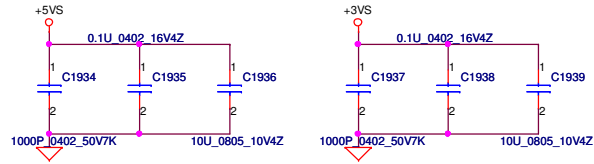


Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Compal Electronics, Inc.	
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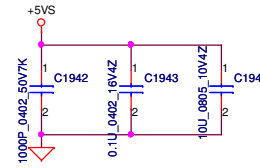
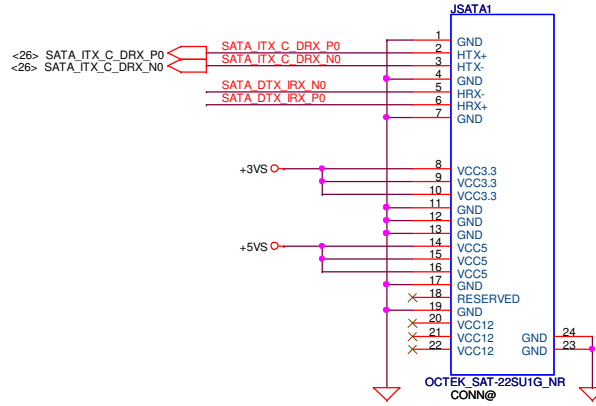
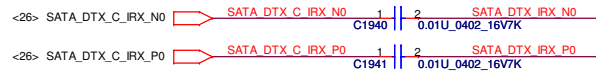


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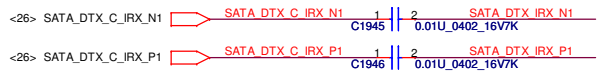
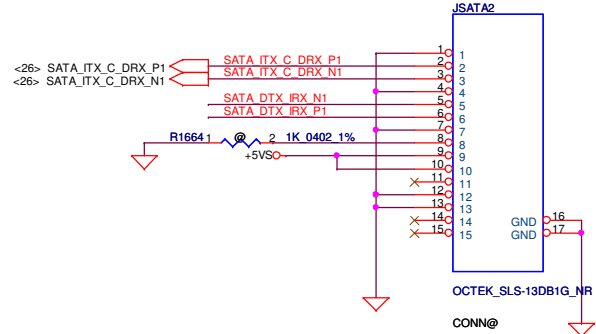
Compal Electronics, Inc.	
Title ICH9M(4/4)-POWER&GND	
Size	Document Number
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SATA HDD Conn.



SATA ODD Conn.

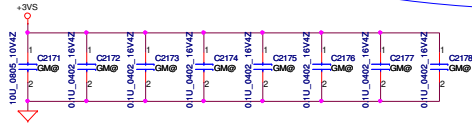


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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title		
				HDD & ODD Connector		
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				Custom	KALH0/KALG0/KAL90+	1.0
				Date:	Monday, April 27, 2009	Sheet 29 of 53

20071029:
C1 (10U_0805) close to JP1.Pin 226, 228, 230

20071029:
C2, C3, C4, C5, C6, C7, C8 (0.1U_0402) close to U1 VCC (+3VS) pins (one Pin one Capacitor)

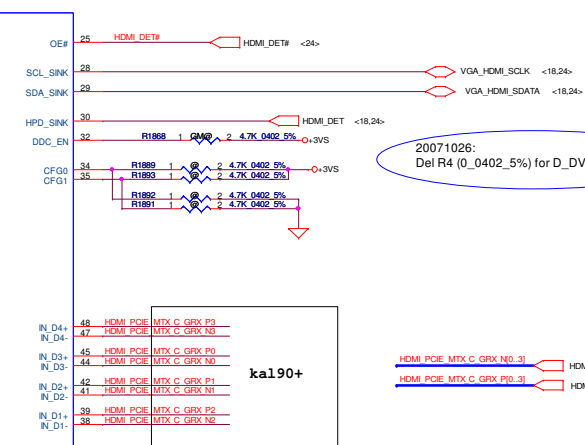
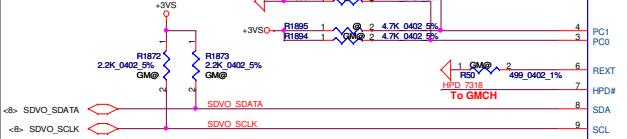
PCE_MTX_C_GRX_N0_1S] <10,17>
PCE_MTX_C_GRX_P0_1S] <10,17>



20071210:
R6 change to 1K_0402_1%
(Old - 1.2K)

20071210:
R3 change to 0_0402_1%
(Old-10K)

20071026:
Del R4 (0_0402_5%) for D_DVI_DET remove.

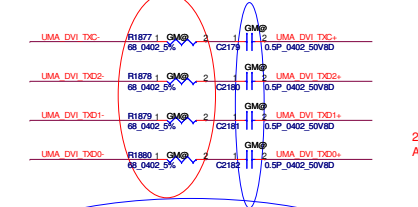


ka190+

HDMI_PCIE_MTX_C_GRX_N0_3] <10>
HDMI_PCIE_MTX_C_GRX_P0_3] <10>

20071210:
Trace AS Short PASSS
R9-R12 change to 68_0402_5%
(Old - 6.8)

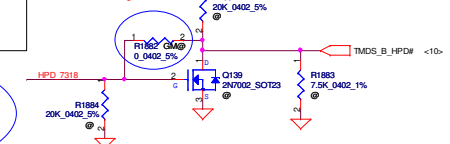
20071031:
Add U1_49 (THERMAL_GND) to GND Plane



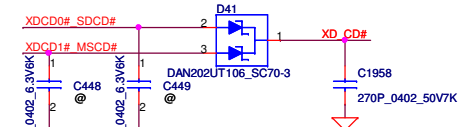
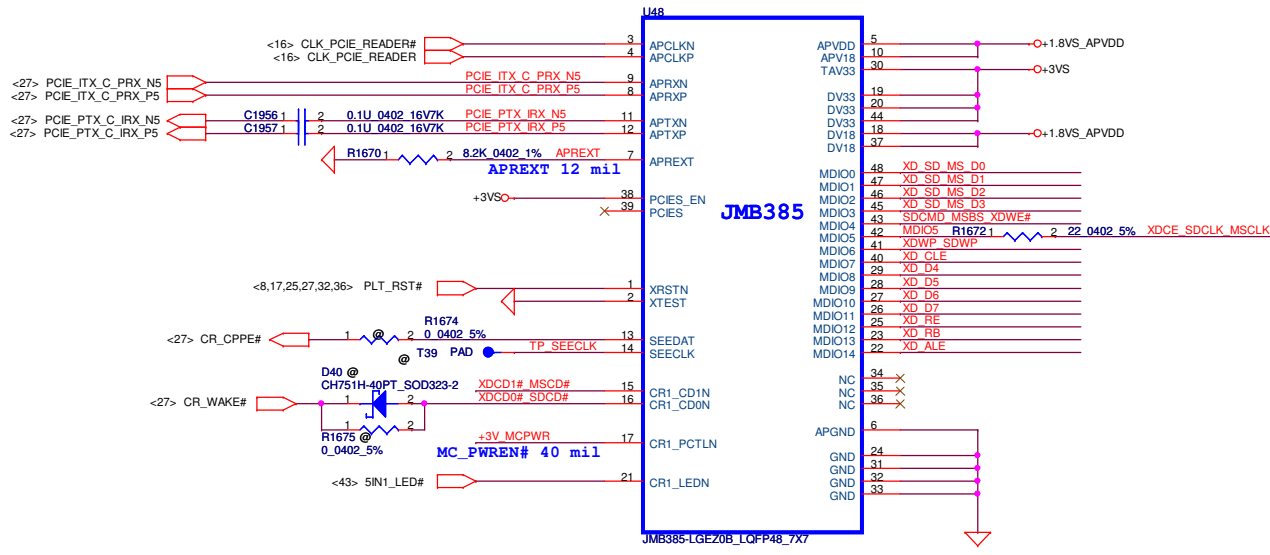
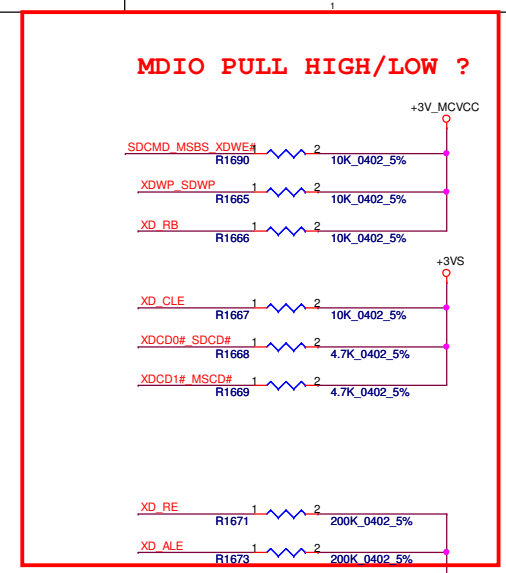
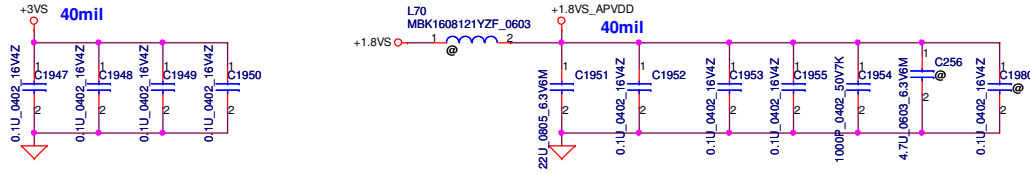
20080128_PVT (change to B version):
SA00001U900 (CH7318A-BF-TR)
SA00001U910 (CH7318B-BF-TR)

20080130_PVT
Add R17 for Inverting Current

20071026:
C9,C10,C11,C12
Change P/N to SA00000AU00 (0.5P_0402_50V8D)
20080130_PVT
C9,C10,C11,C12
Change P/N to SE00000HA00 (0.5P 50V C NPO 0402)

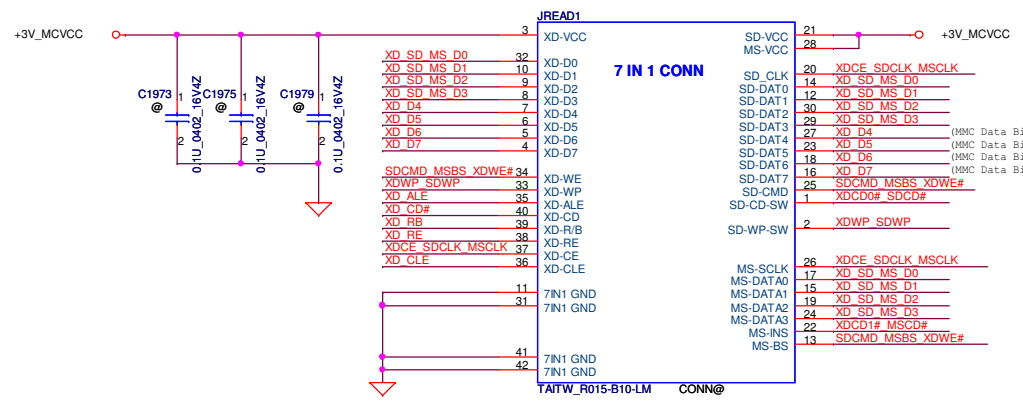
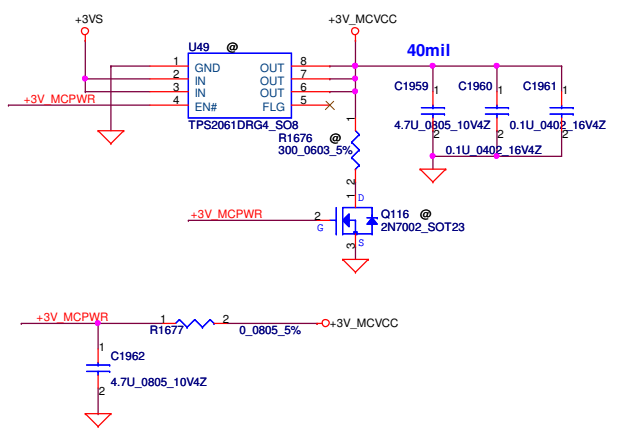


Intel Cantiga TMDS Pin Definition	
TMDS_B_CLK	PEG_TXP_3
TMDS_B_CLK#	PEG_TXN_3
TMDS_B_DATA0	PEG_TXP_2
TMDS_B_DATA0#	PEG_TXN_2
TMDS_B_DATA1	PEG_TXP_1
TMDS_B_DATA1#	PEG_TXN_1
TMDS_B_DATA2	PEG_TXP_0
TMDS_B_DATA2#	PEG_TXN_0
TMDS_B_HPD#	PEG_RXP_3

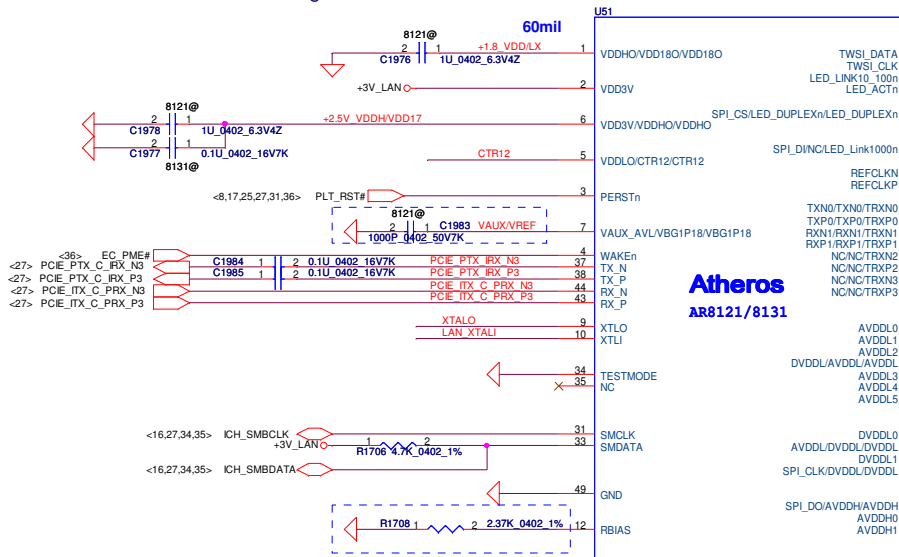
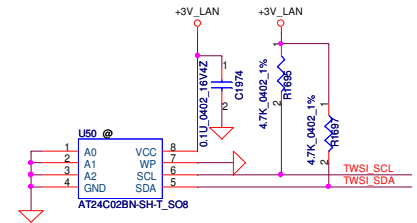
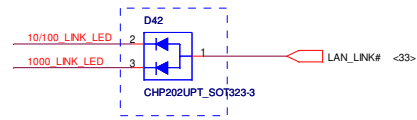
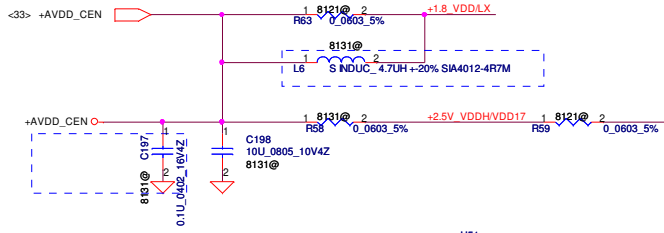
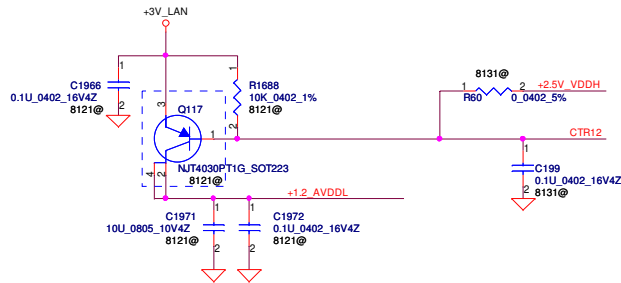
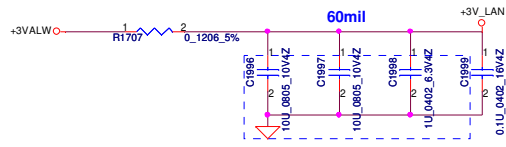


4 IN 1 Socket Push Type(New)

Memory Card Power Switch

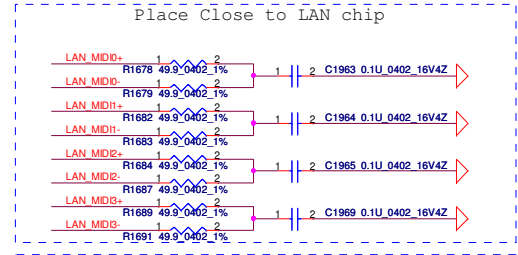


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Size	Document Number	Date		Rev	1.0
Custom	KALH0/KALGO/KAL90+	Monday, April 27, 2009		Sheet	31 of 53

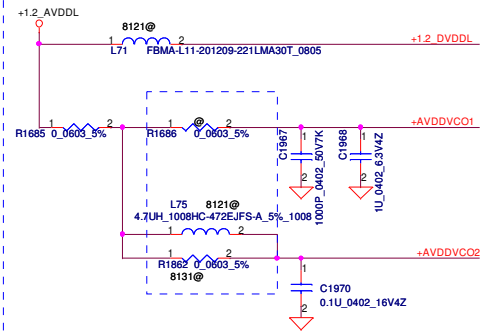
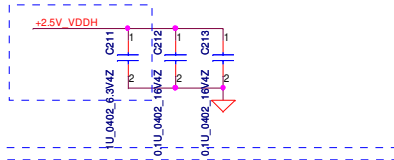


Atheros
AR8121/8131

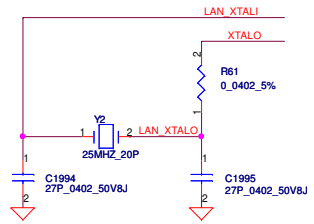
AR8121-AL1E_QFN48_6X6
SA000031Z00 S IC AR8131-AL1E_QFN 48P E-LAN CTRL
8121@
SA000025M00 S IC AR8121-AL1E_QFN 48P E-LAN CTRL



Place Close to Pin15、19、25
C1061 close to Pin15

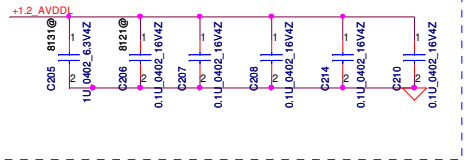
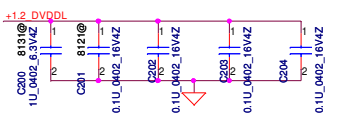


8121 If not overclocking , R1685 & L75 stuffed and R1686 & R1682 removed
8131 If not overclocking , R1685 & R1682 stuffed and R1686 & L75 removed



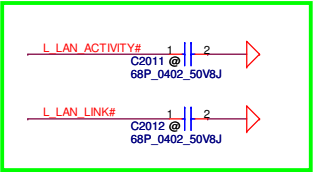
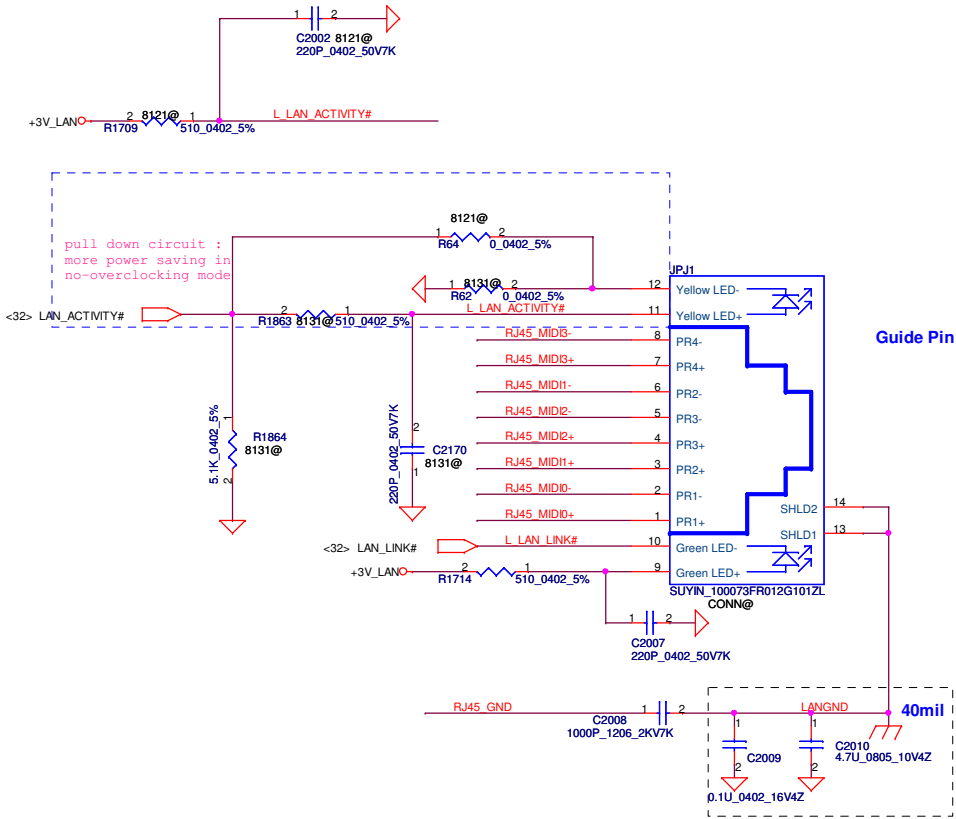
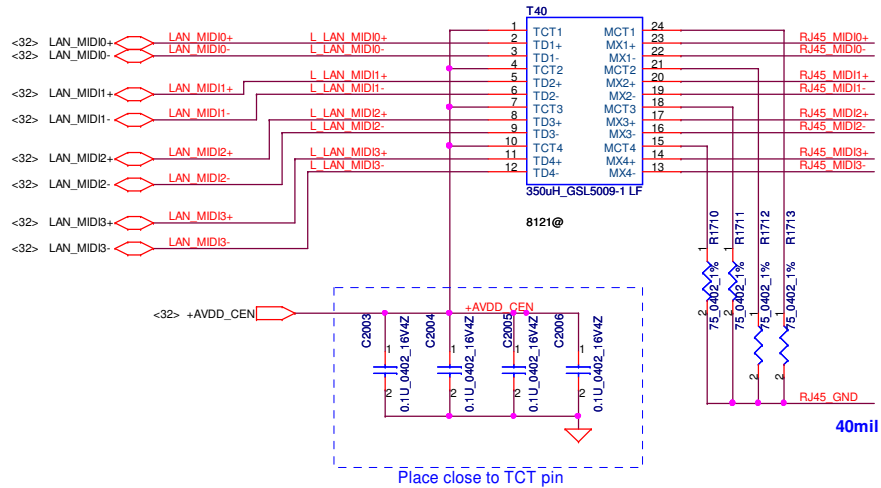
Place Close to Pin 28、32、45、46
C1750 and C1730 close to Pin46
C1072 close to Pin45

Place Close to Pin8、16、22、36、39
C1066 and C1067 close to Pin8



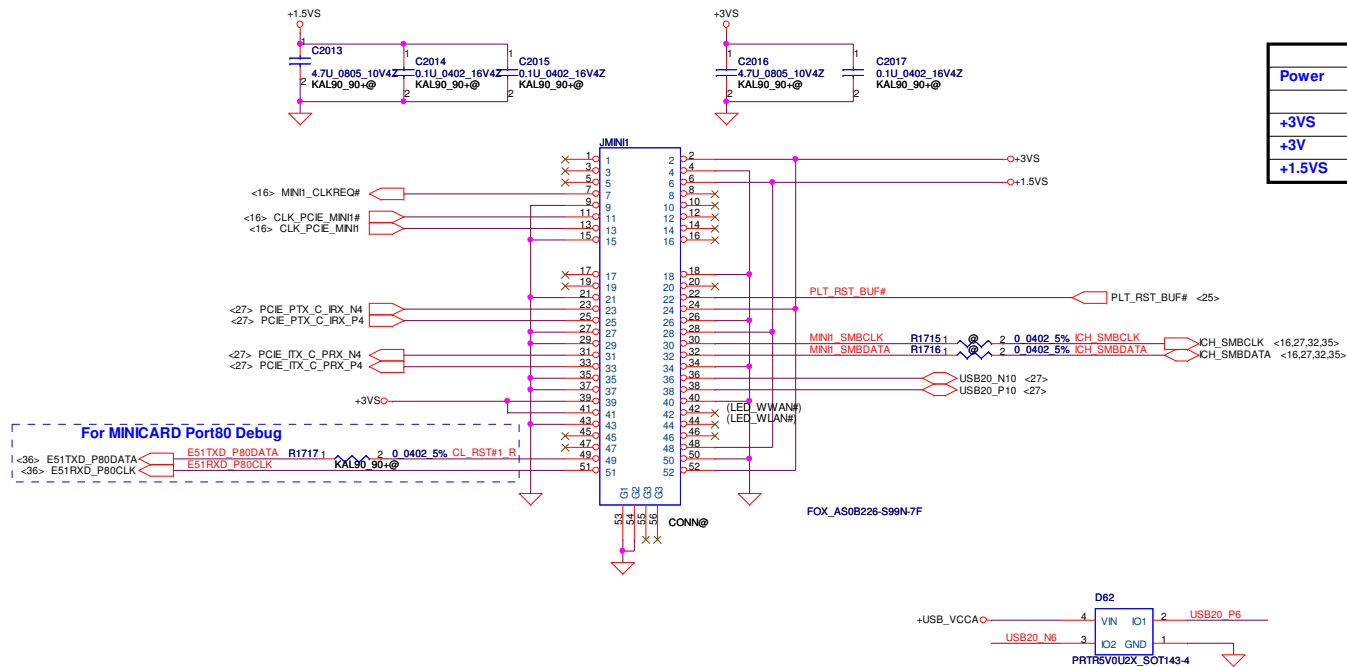
Security Classification	Compal Secret Data		Title	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Atheros AR8131
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Size	Document Number	KALH0/KALG0/KAL90+		Rev
Custom				1.0
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LAN AR8121/8112



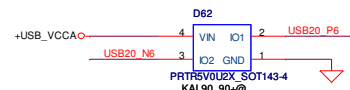
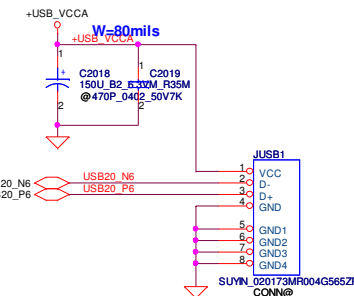
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	LAN Magnetic & RJ45	
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				B	KALH0/KALG0/KAL90+	1.0
				Date:	Monday, April 27, 2009	Sheet 33 of 53

For Robson2

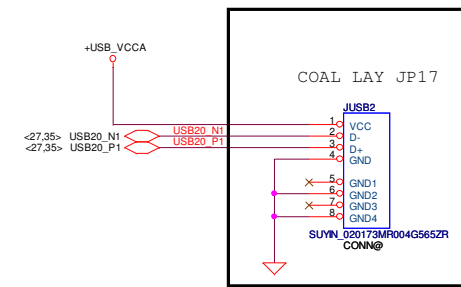
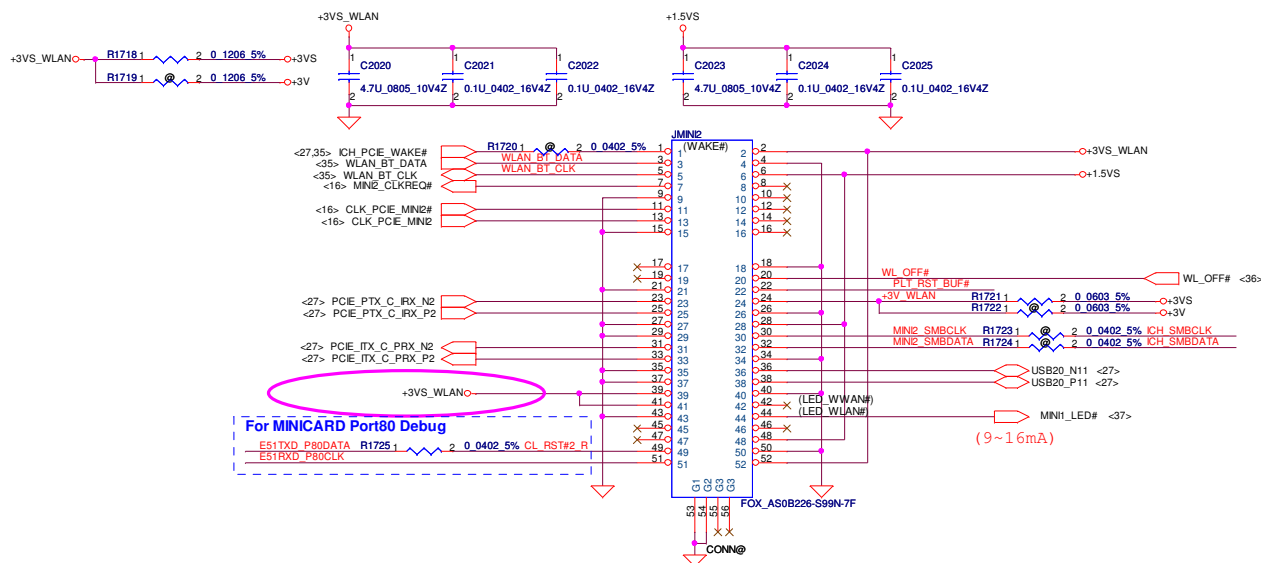


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

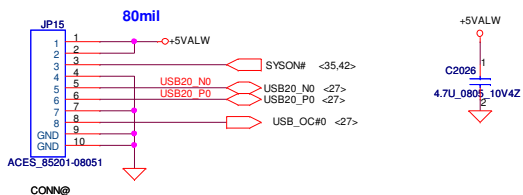
USB CONN.



For Wireless LAN

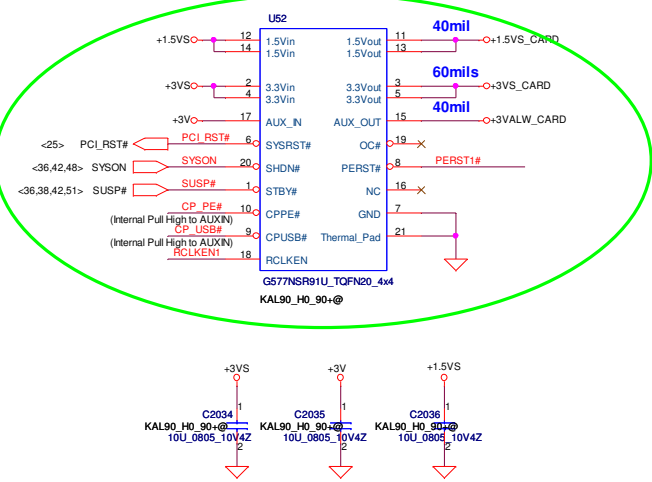


To USB/B Connector

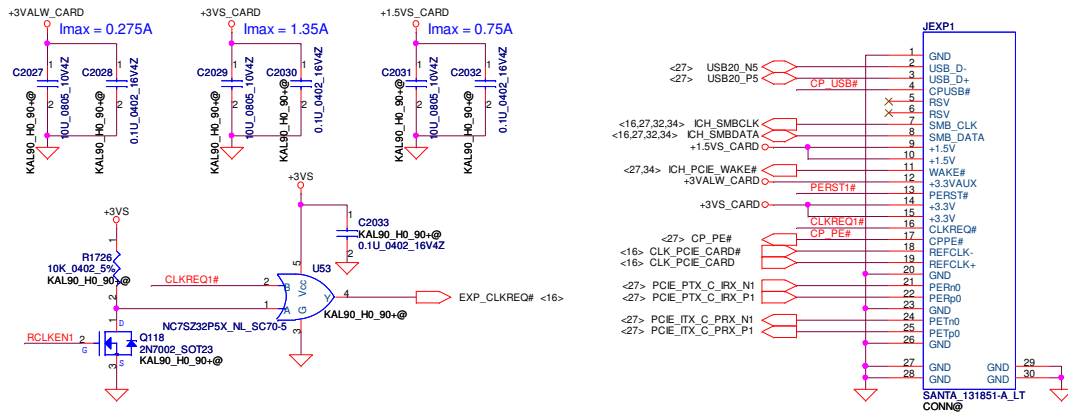


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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
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				Size B	Document Number
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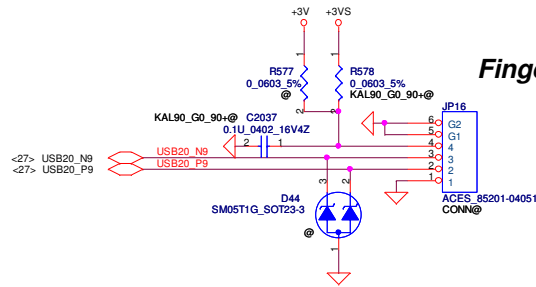
New Card Power Switch



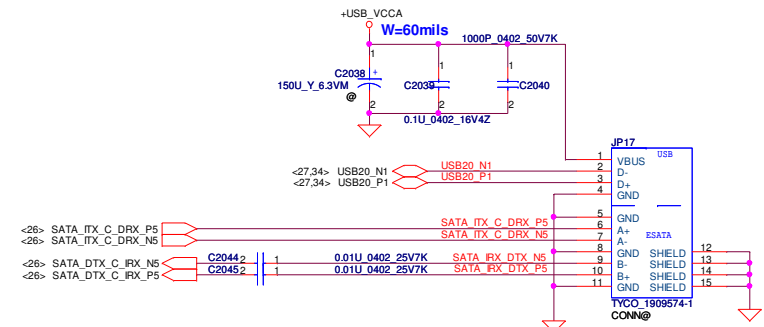
New Card Socket (Left/TOP)



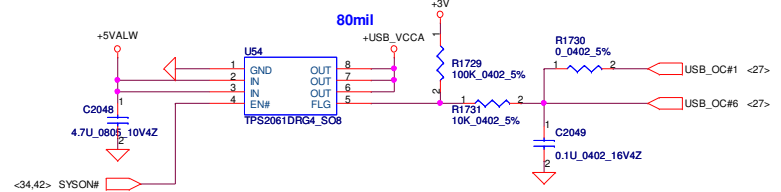
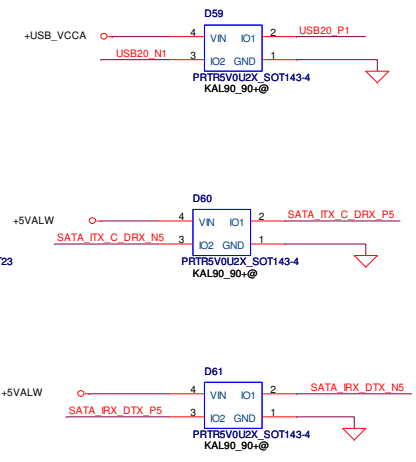
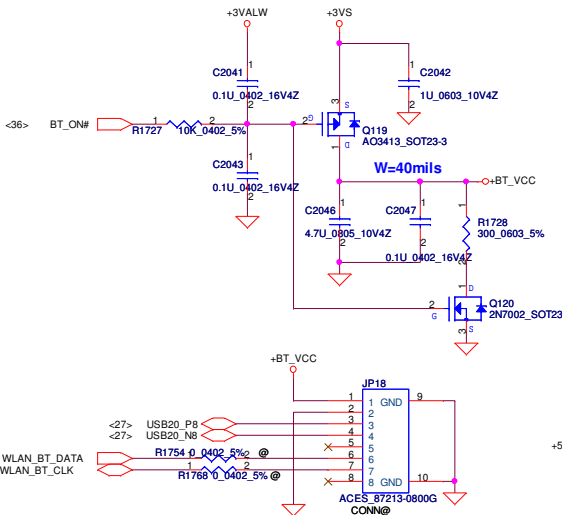
Finger Print Conn.



ESATA CONN



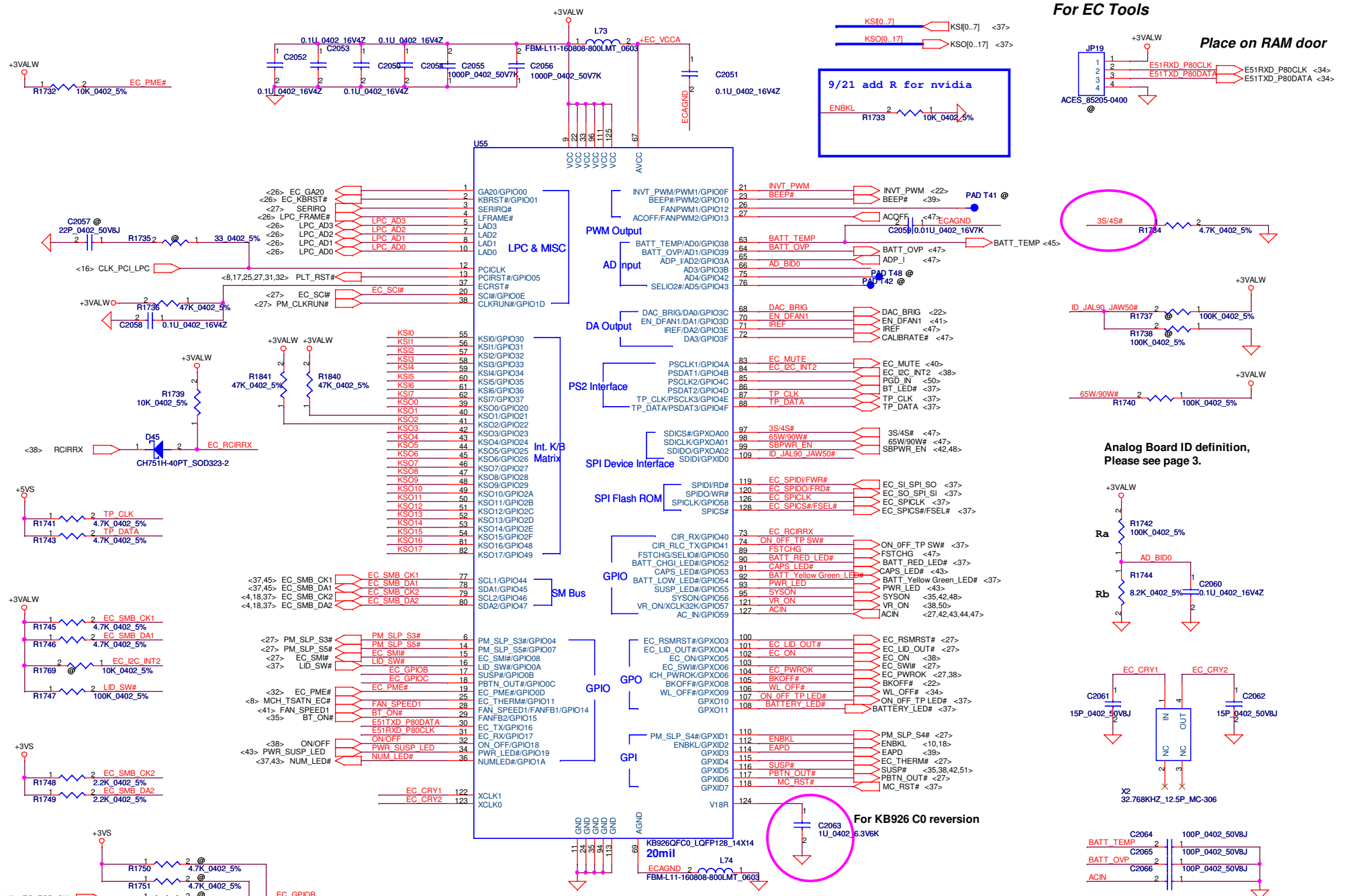
Bluetooth Conn.



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Compal Electronics, Inc.

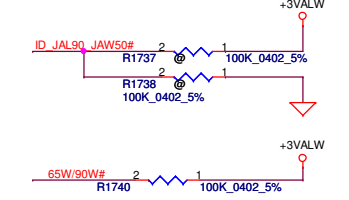
NEW CARD & eSATA Connector



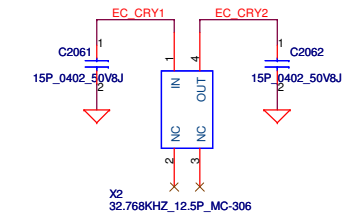
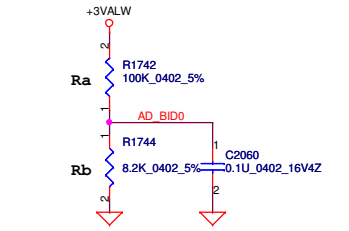
For EC Tools

Place on RAM door

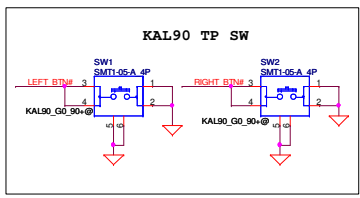
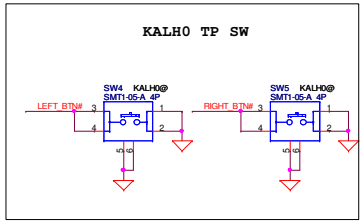
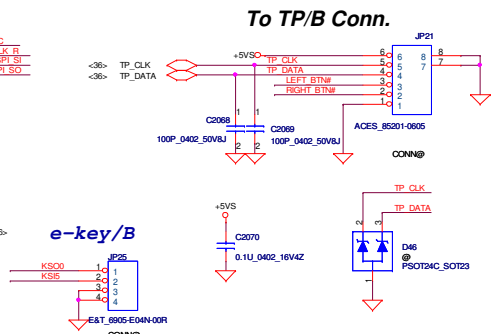
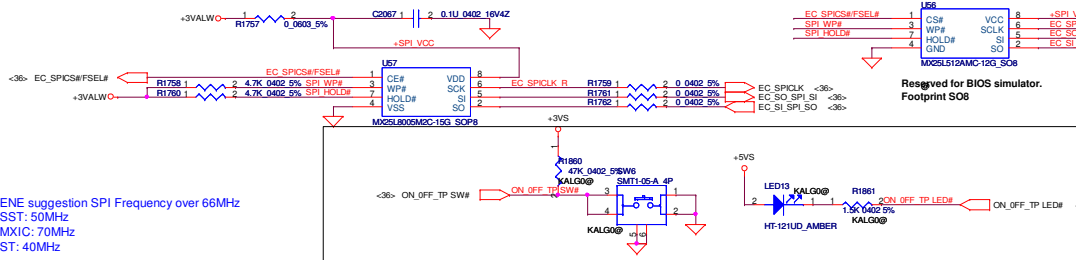
9/21 add R for nvidia
ENBKL R1733 10K_0402_5%



Analog Board ID definition, Please see page 3.

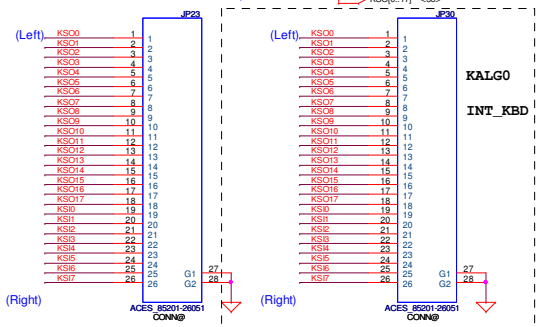


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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	
				EC ENE KB926	
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Size	Document Number			Rev	
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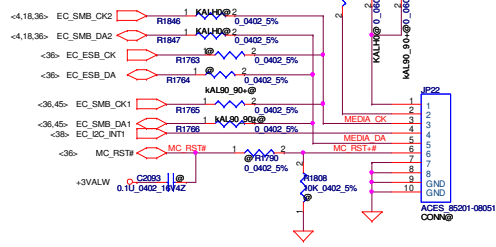


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

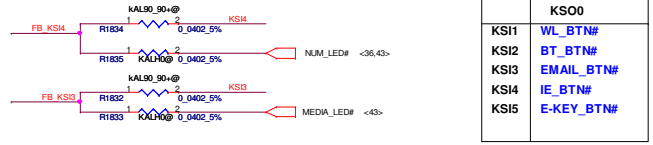
INT_KBD Conn.



To Media/B Conn.

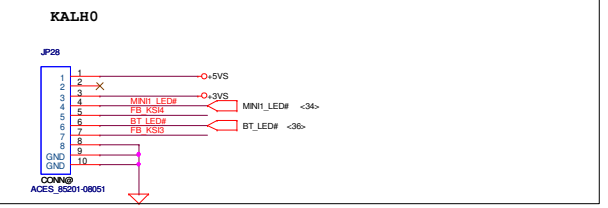
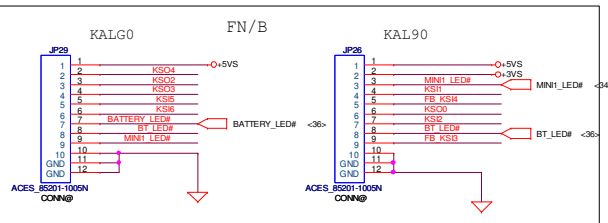
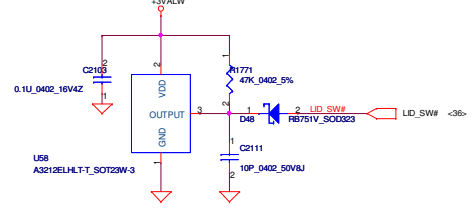


To BTN/B Conn.

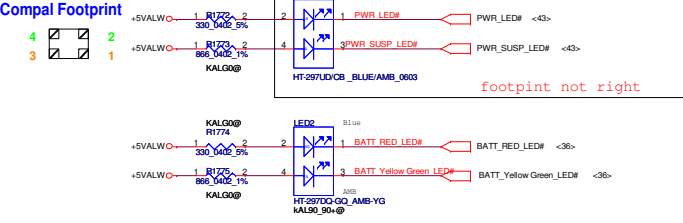
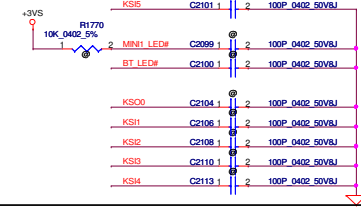


Lid Switch

(Hall Effect Switch)



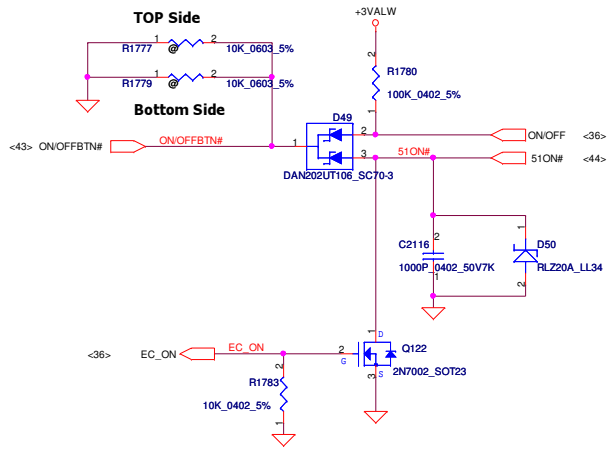
FOR EMI



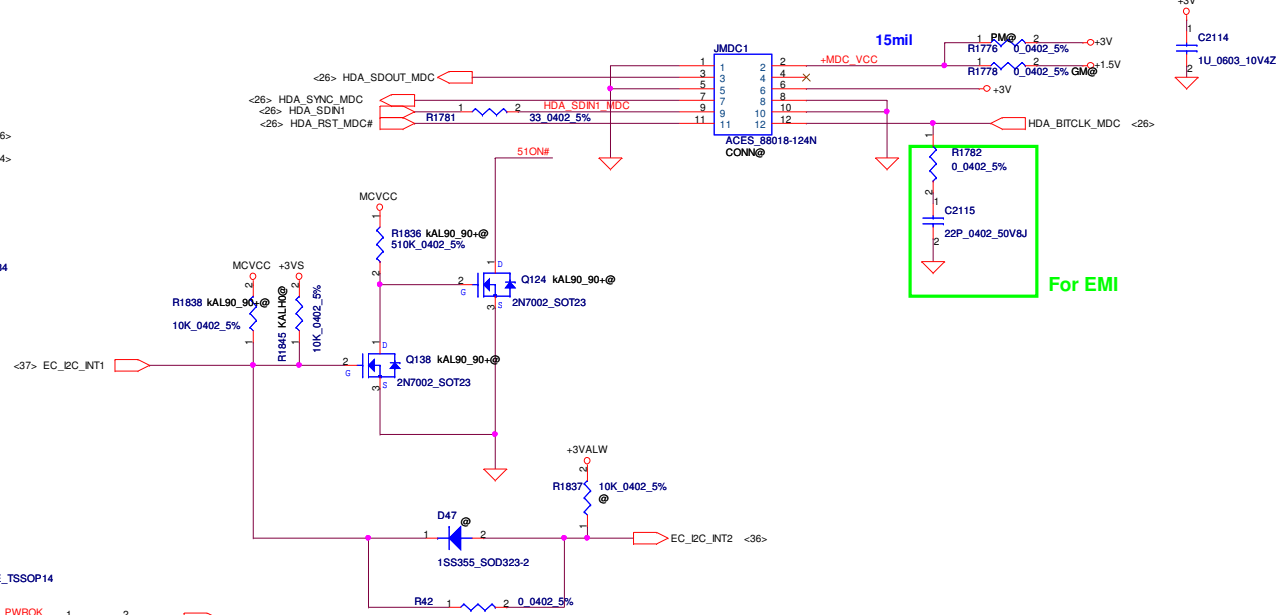
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/1/24	Deciphered Date	2009/12/31	Title	BIOS, I/O Port & K/B Connector
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Size C	Document Number	KALHO/KALGO/KAL90+		Rev	1.0
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ON/OFF switch

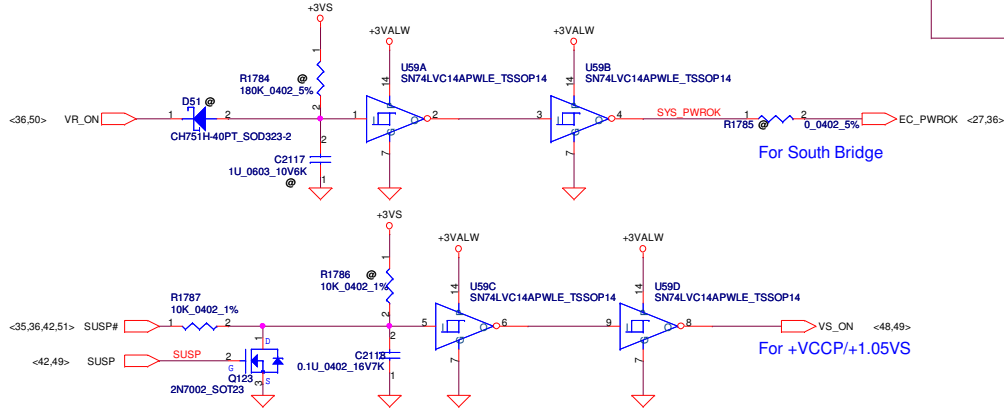
Power Button



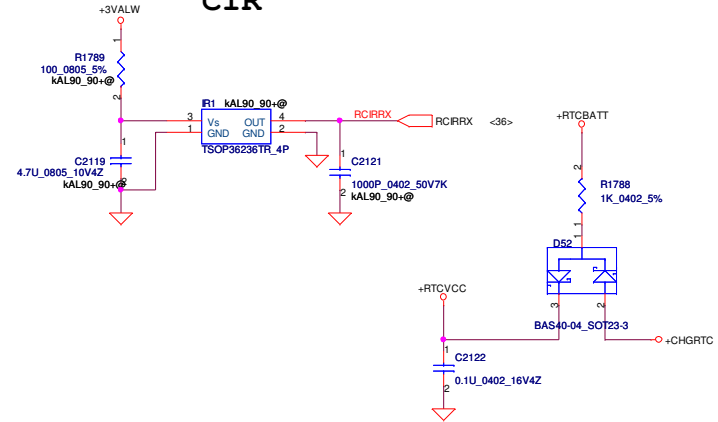
HDA MDC Conn.



Power ON Circuit

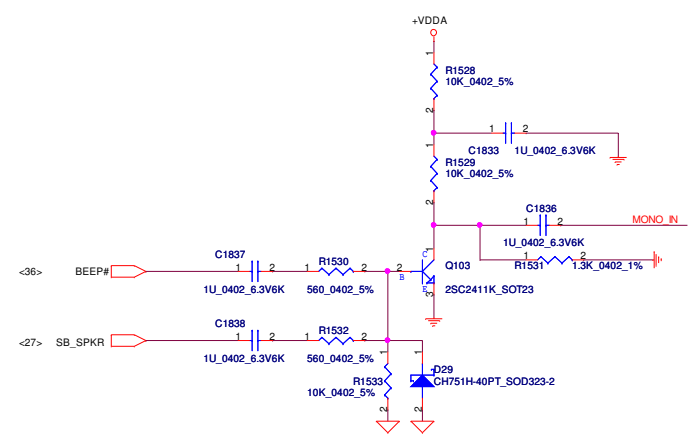


CIR



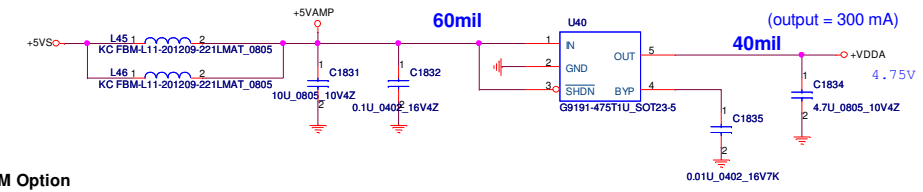
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title		
				Power OK, Reset, RTC, CIR, MDC		
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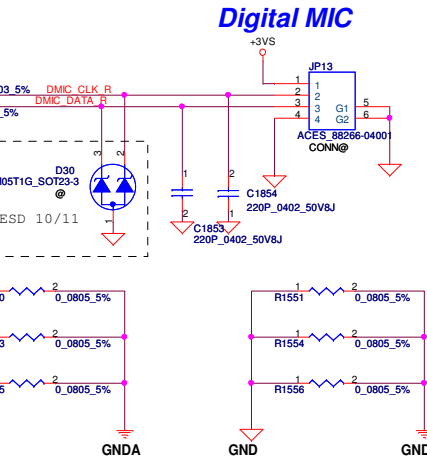
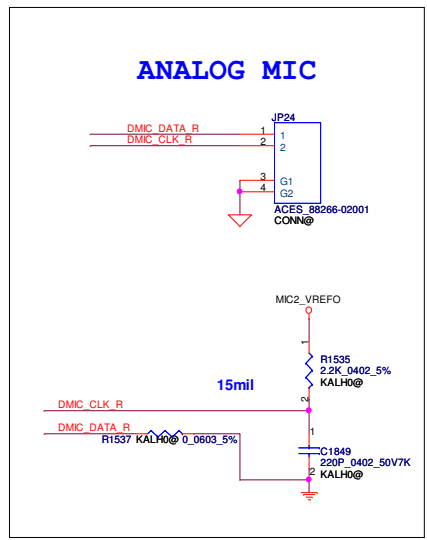
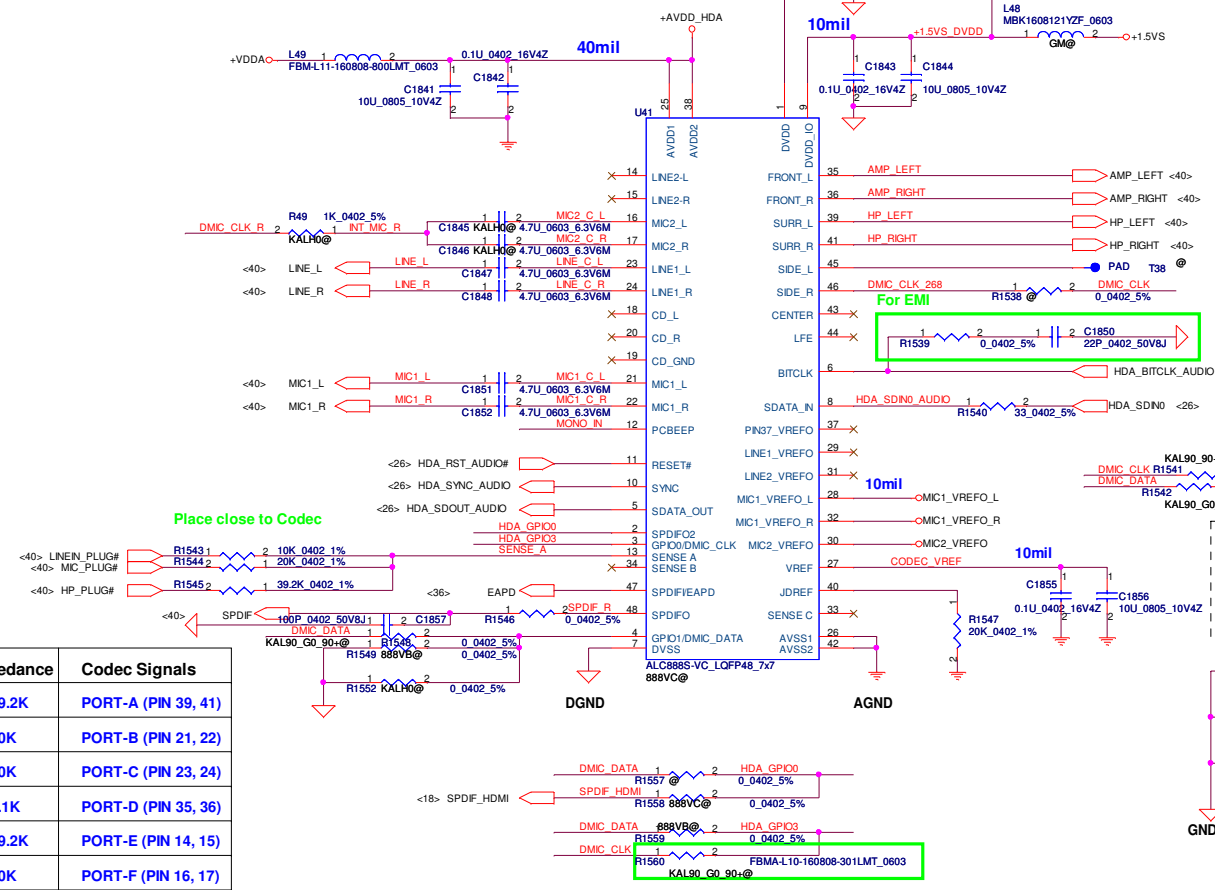


BOM Option

ALC268	268@
ALC888S-VB	888VB@
ALC888S-VC	888VC@



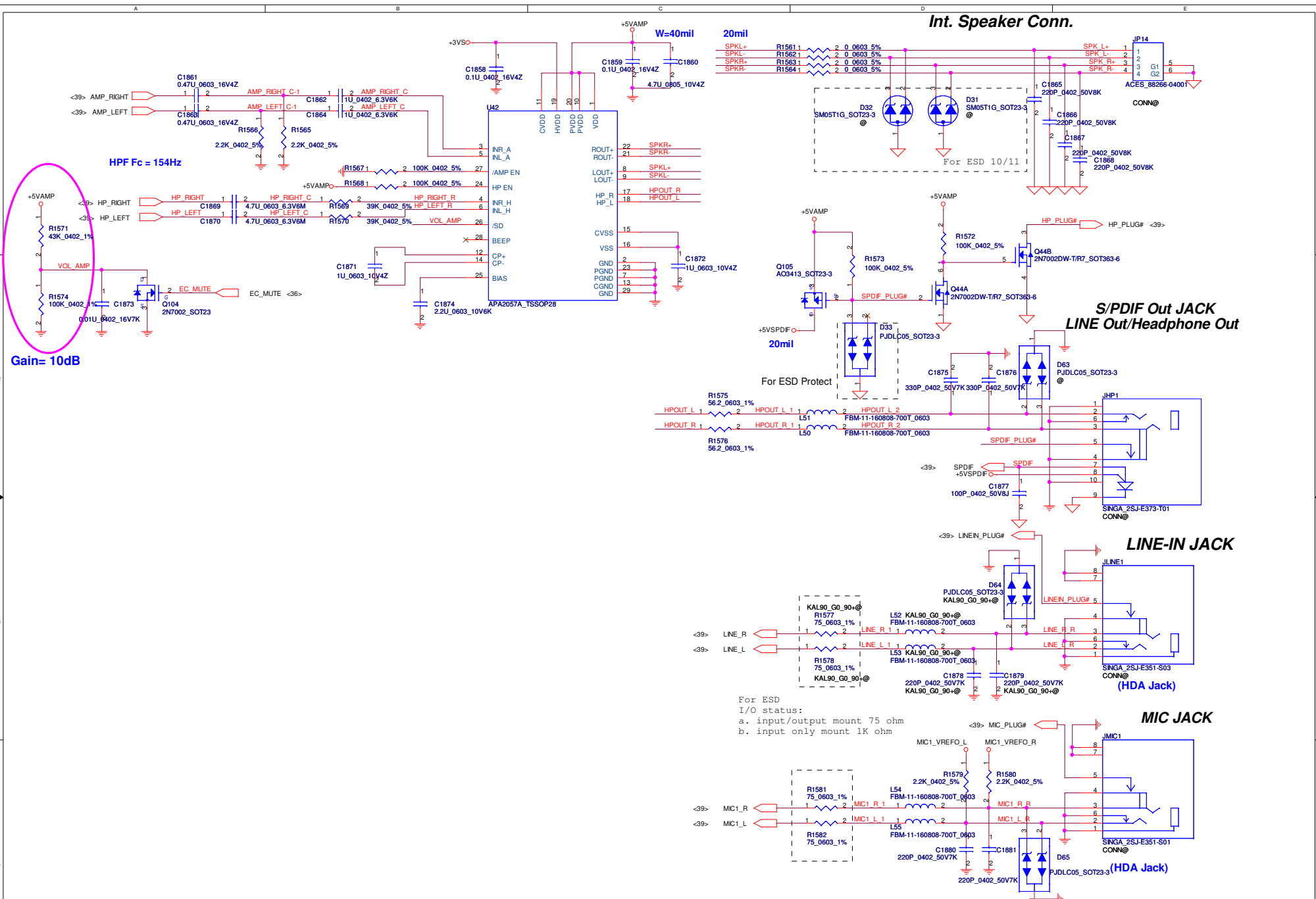
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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Title		
HD Audio Codec ALC888S-VC		
Size	Document Number	Rev
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Gain= 10dB

Int. Speaker Conn.

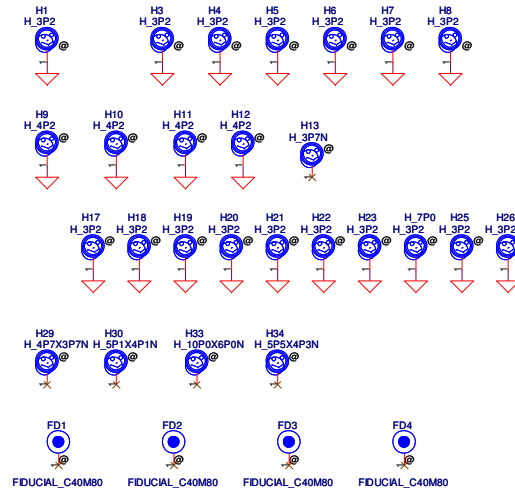
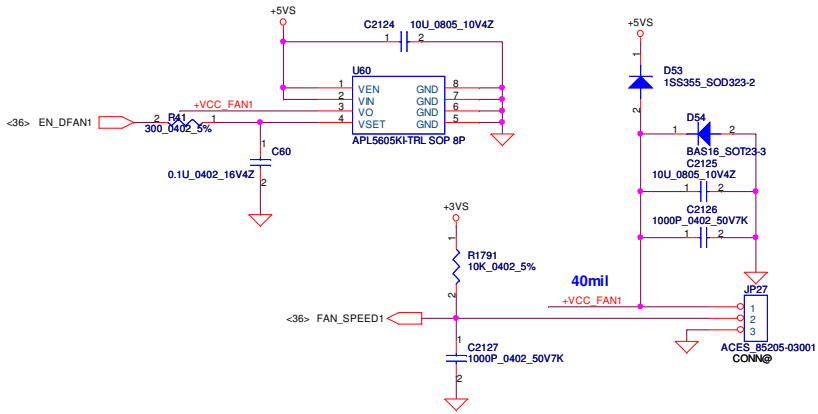
S/PDIF Out JACK
LINE Out/Headphone Out

LINE-IN JACK

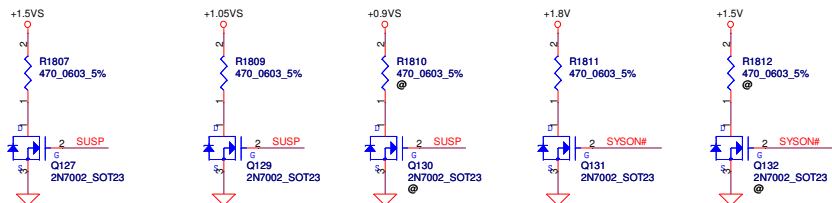
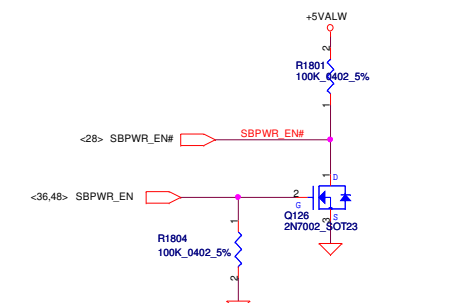
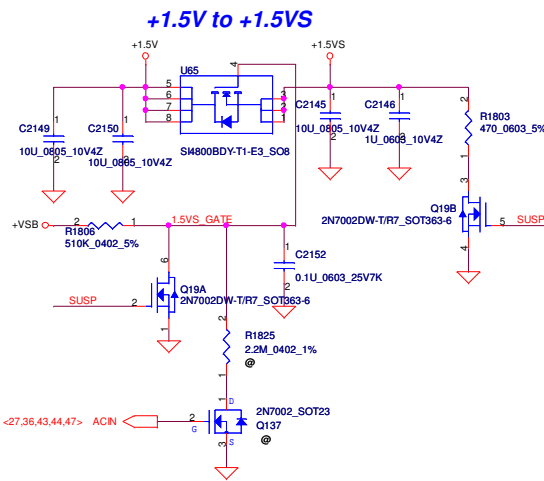
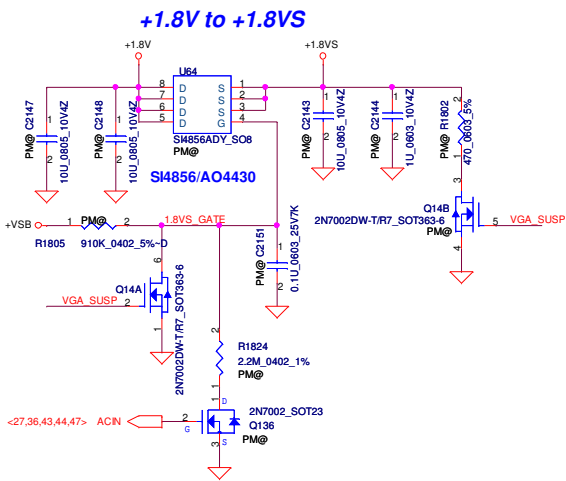
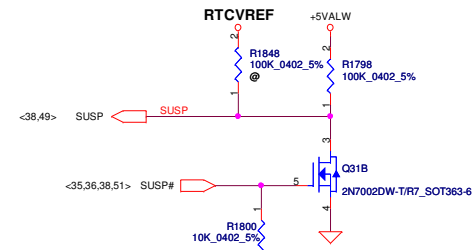
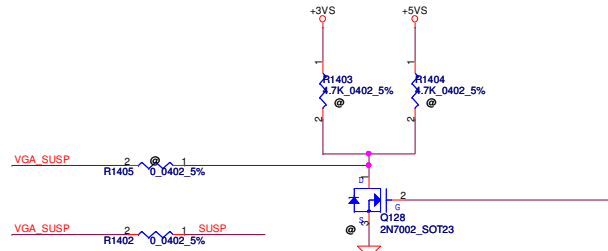
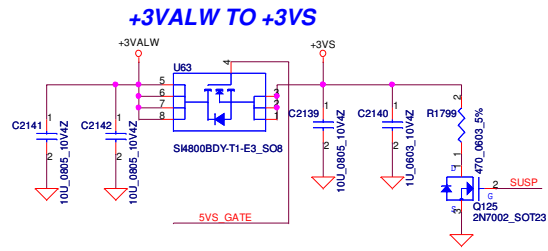
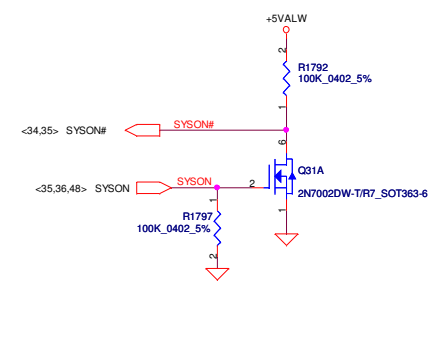
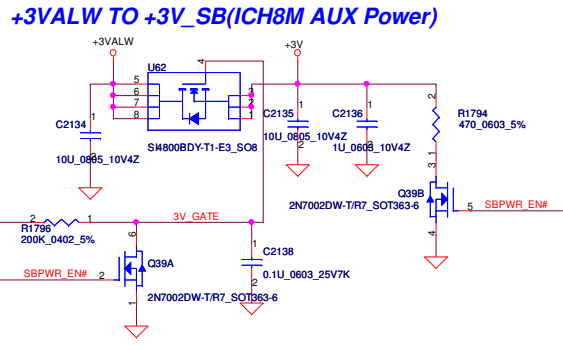
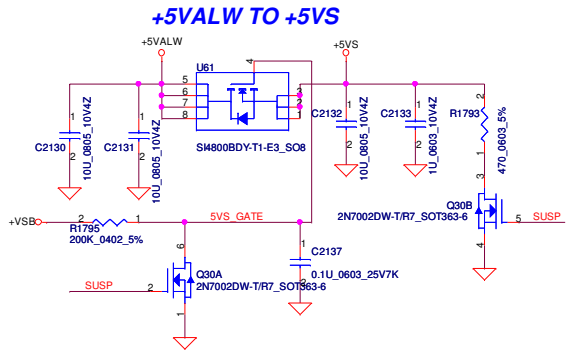
MIC JACK

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FAN1 Conn



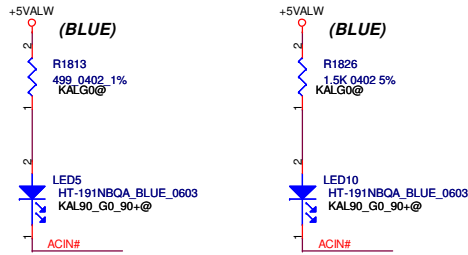
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Issued Date	2008/11/24	Deciphered Date	2009/12/31	
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Title	FAN & COVER LIGHT & Screw Hole			
Size	Document Number			Rev
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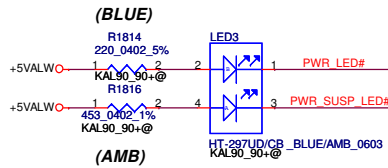
Security Classification	Compal Secret Data	
Issued Date	2008/11/24	Deciphered Date
		2009/12/31
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Compal Electronics, Inc.		
DC Interface		
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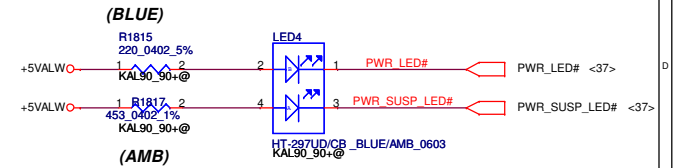
Enlightener LED



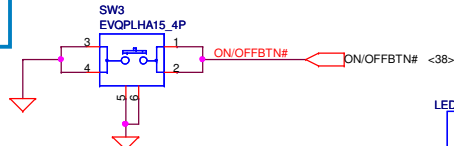
ON/OFF LED LEFT



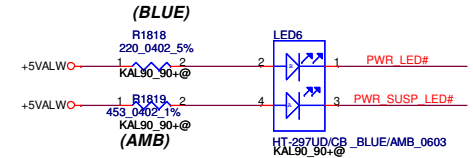
ON/OFF LED RIGHT



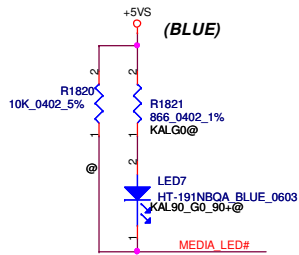
ON/OFF Button



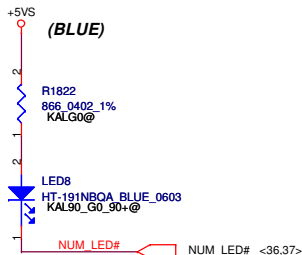
ON/OFF LED DOWN



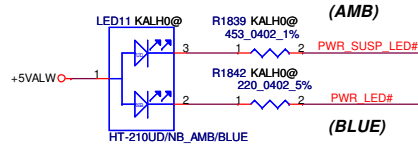
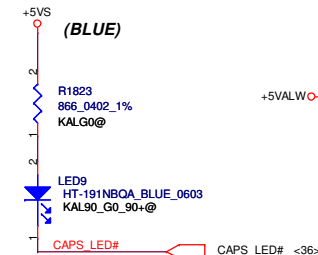
MEDIA_LED



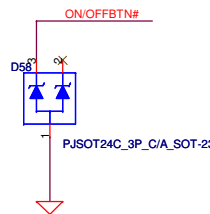
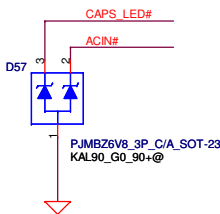
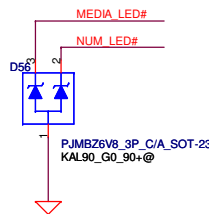
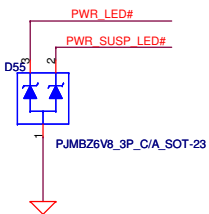
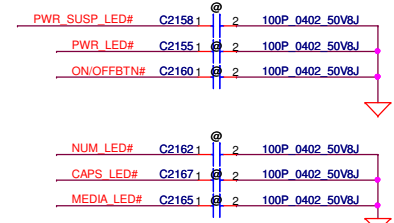
NUM_LED



CAPS_LED

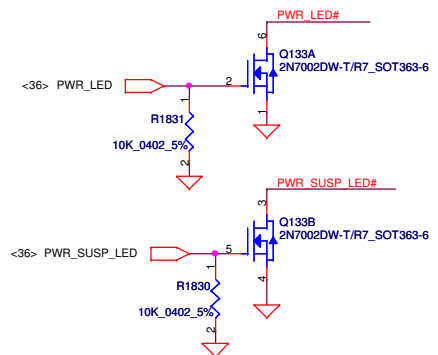
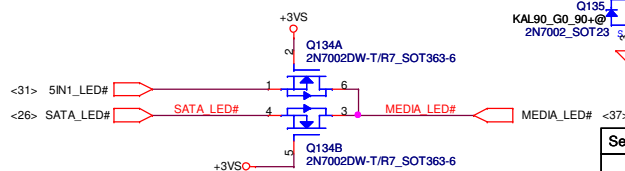


FOR EMI

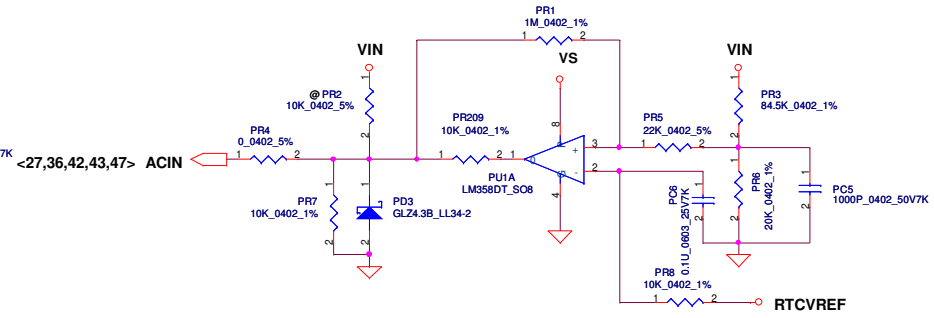
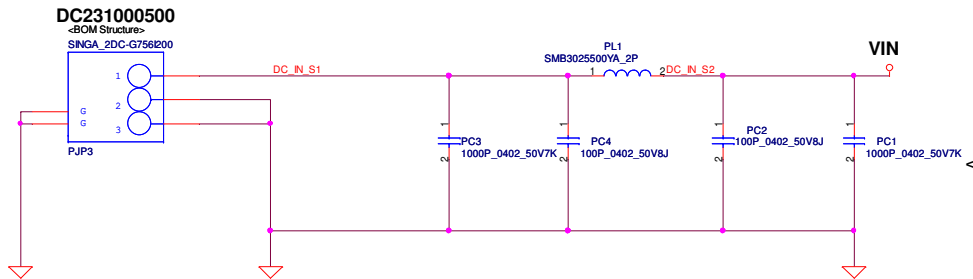


**D1 D2 D3 USE PANJIT PJMBZ6V8
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6.8V**

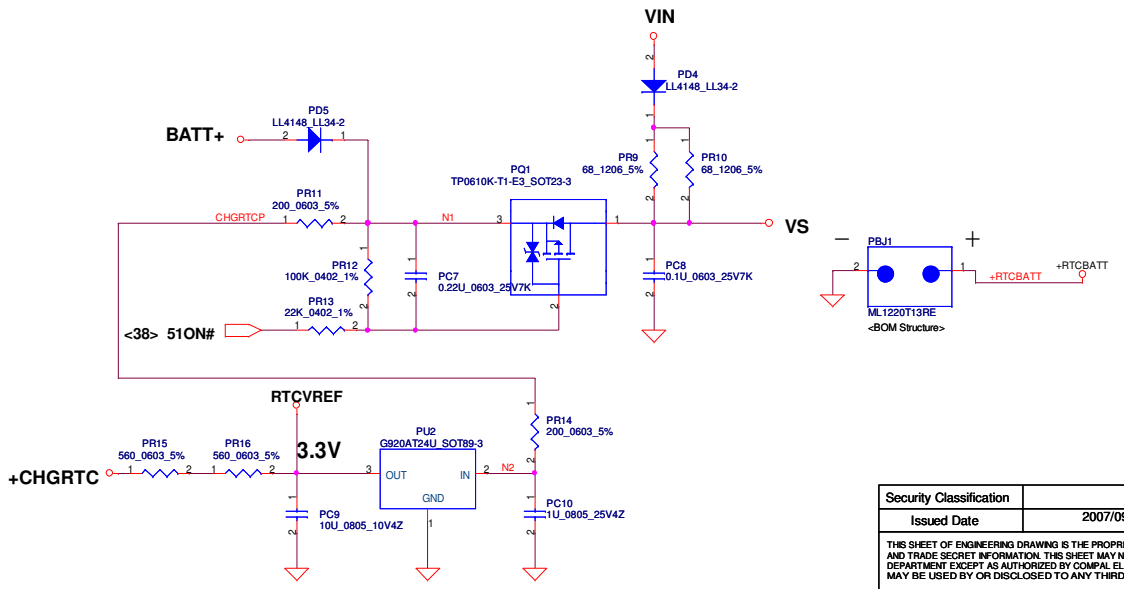
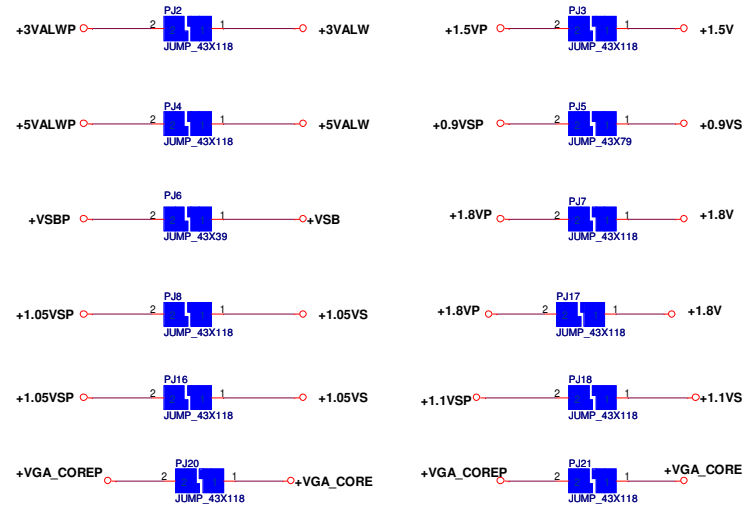
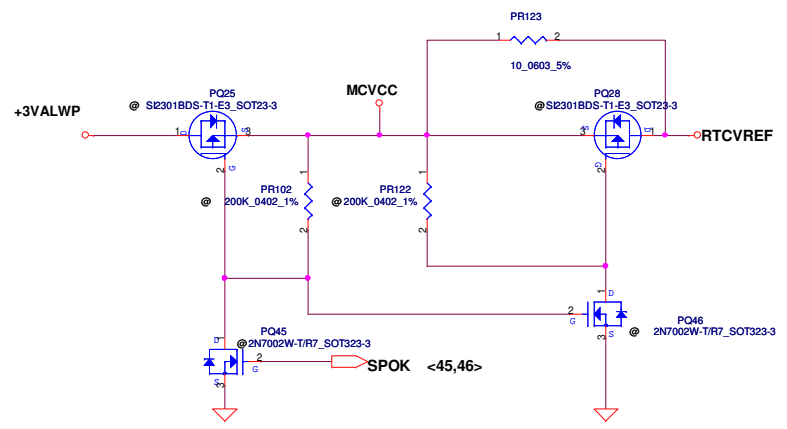
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PJSOT24C 3P C/A SOT-23
SCA00000E00
24V**



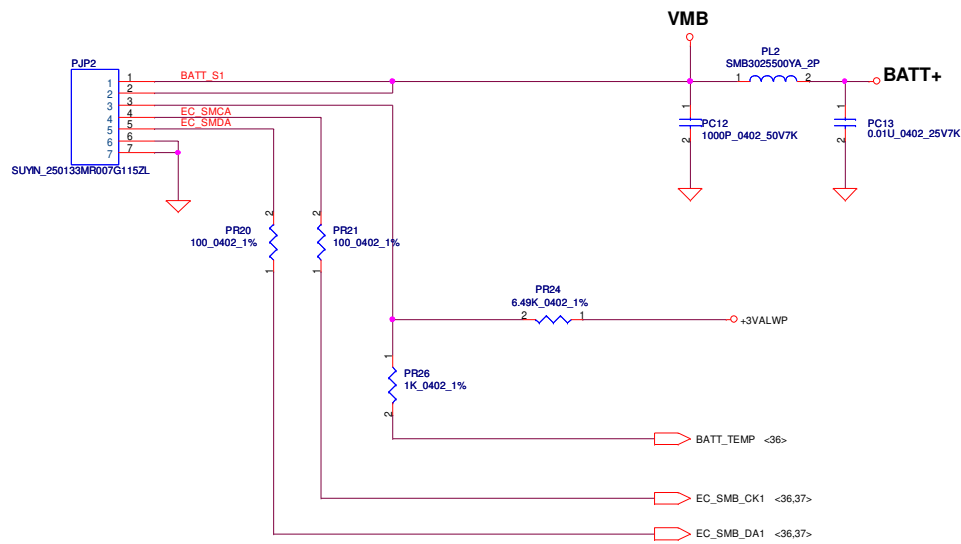
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	PWR/B	
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Size Custom	Document Number	KALH0/KALG0/KAL90+		Rev	1.0
Date:	Monday, April 27, 2009	Sheet	43	of	53



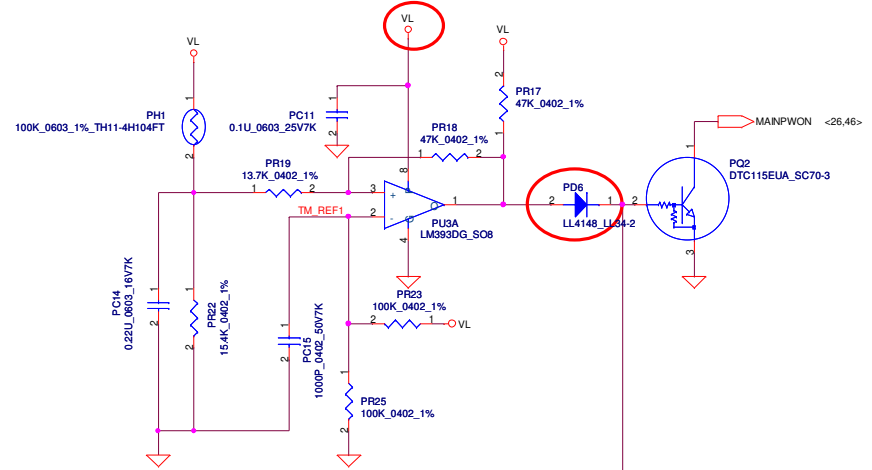
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



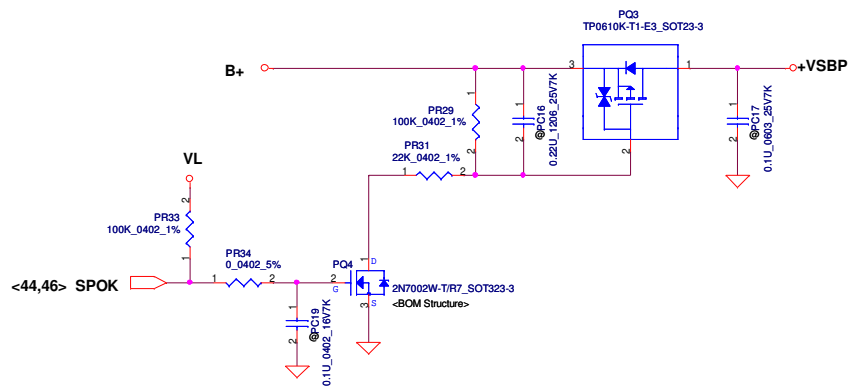
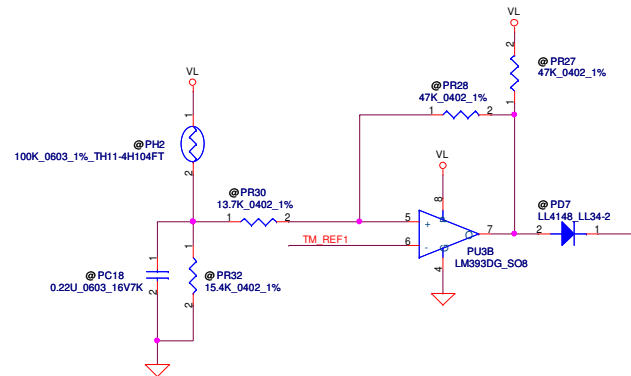
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	DCIN & DETECTOR
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PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C

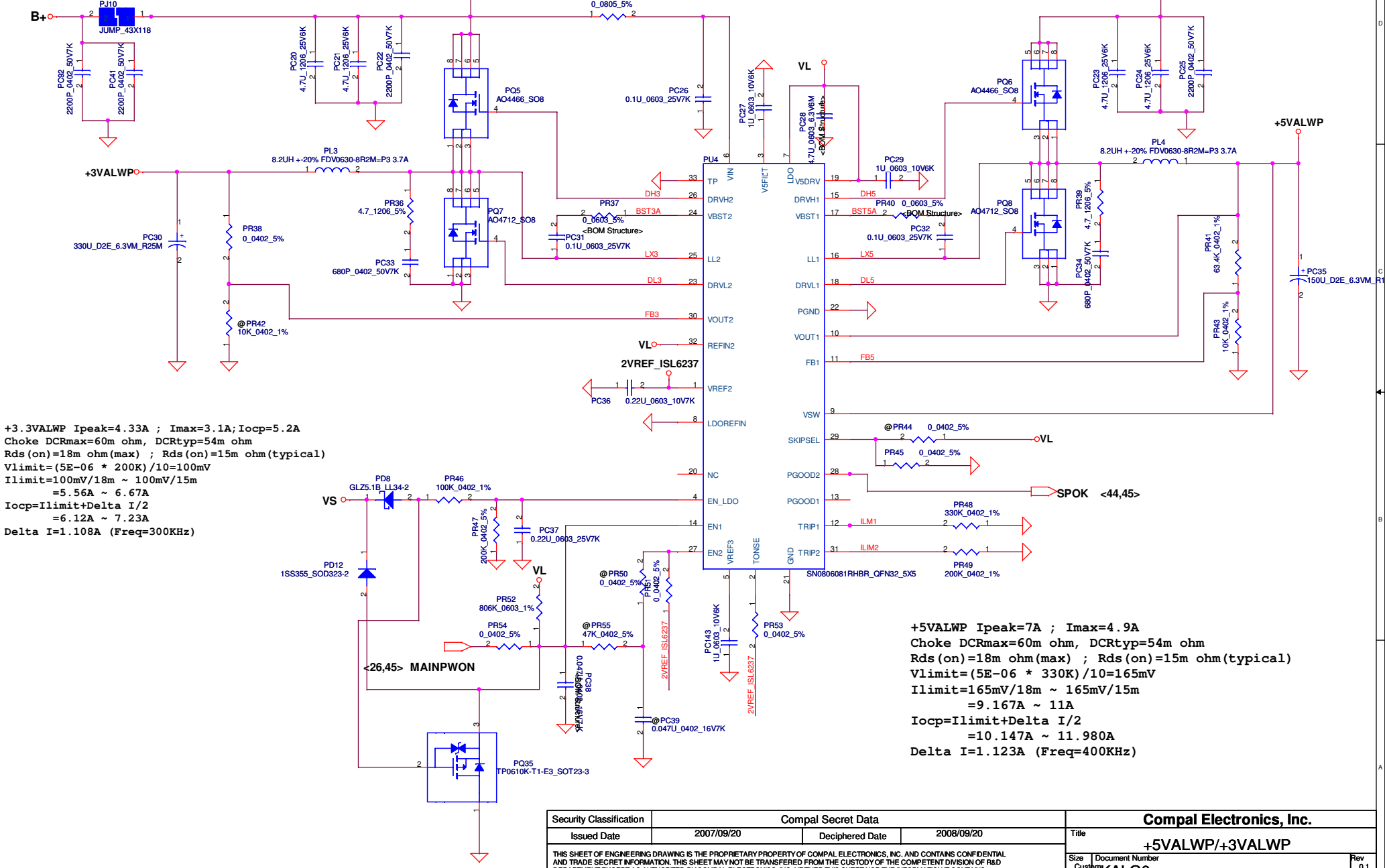


PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



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				Size
				Customer
				KALGO-
				Date: Monday, April 27, 2009
				Sheet 45 of 53

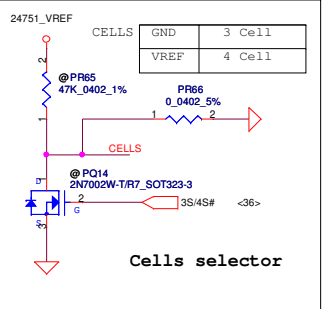
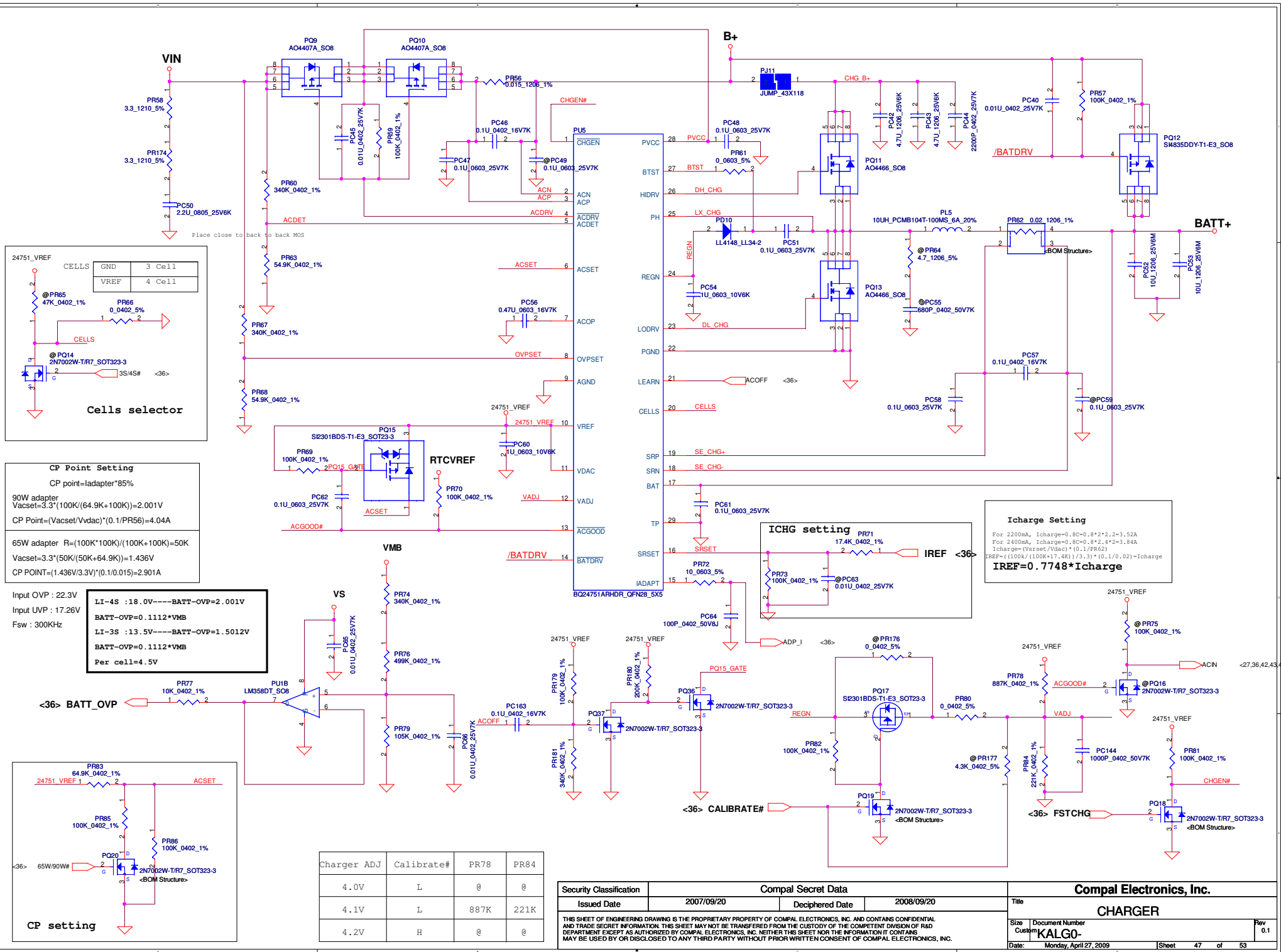
<BOM Structure>



+3.3VALWP Ipeak=4.33A ; Imax=3.1A; Iocp=5.2A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 200K)/10=100mV
 Ilimit=100mV/18m ~ 100mV/15m
 =5.56A ~ 6.67A
 Iocp=Ilimit+Delta I/2
 =6.12A ~ 7.23A
 Delta I=1.108A (Freq=300KHz)

+5VALWP Ipeak=7A ; Imax=4.9A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.123A (Freq=400KHz)

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Size	Document Number	Date		Sheet	Rev
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CP Point Setting

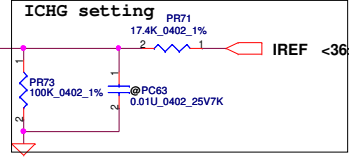
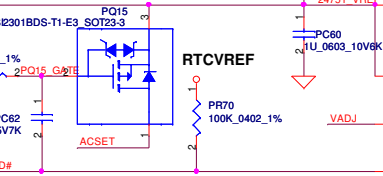
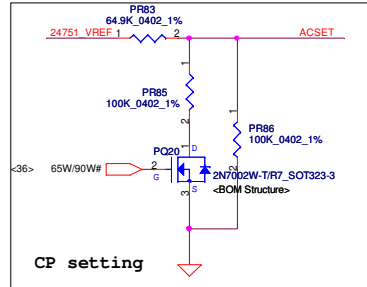
CP point=ladapter*85%

90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
 $CP\ Point=(V_{acset}/V_{dacc}) \cdot (0.1/PR56)=4.04A$

65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
 $CP\ POINT=(1.436V/3.3V) \cdot (0.1/0.015)=2.901A$

Input OVP : 22.3V
 Input LVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V---BATT-OVP=2.001V
 BATT-OVP=0.1112*VMB
 LI-3S : 13.5V---BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=4.5V

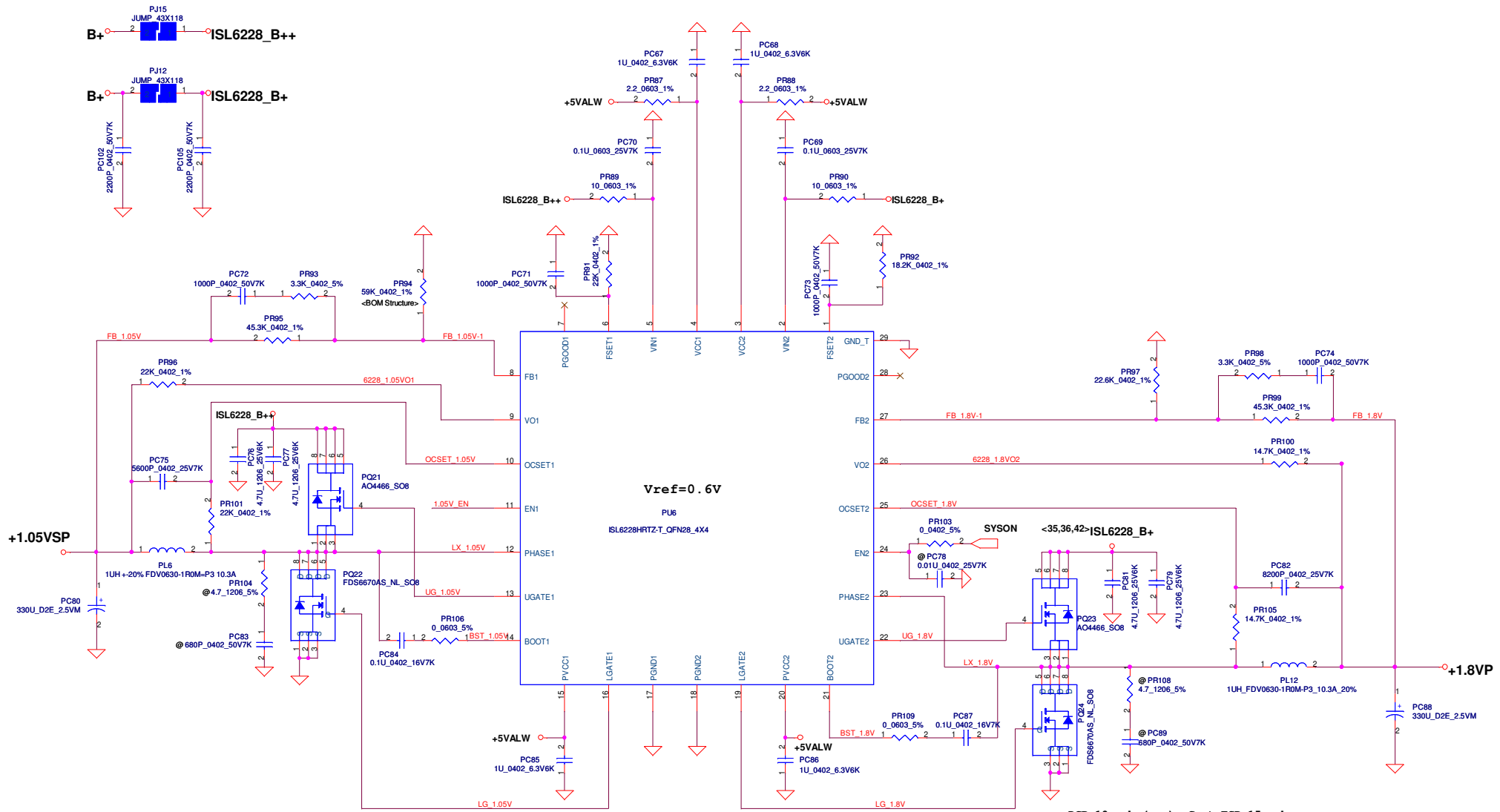


Icharge Setting

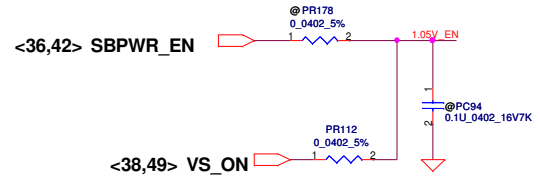
For 2200mA, Icharge=0.8c=0.8*2+2.2=3.52A
 For 2400mA, Icharge=0.8c=0.8*2.4+2=3.84A
 $I_{charge}=(V_{acset}/V_{dacc}) \cdot (0.1/PR62)$
 $IREF=(100K/(100K+17.4K)) \cdot (3.3) \cdot (0.1/0.02)=I_{charge}$
IREF=0.7748*Icharge

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

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Issued Date	2007/09/20	Deciphered Date	2008/09/20	CHARGER
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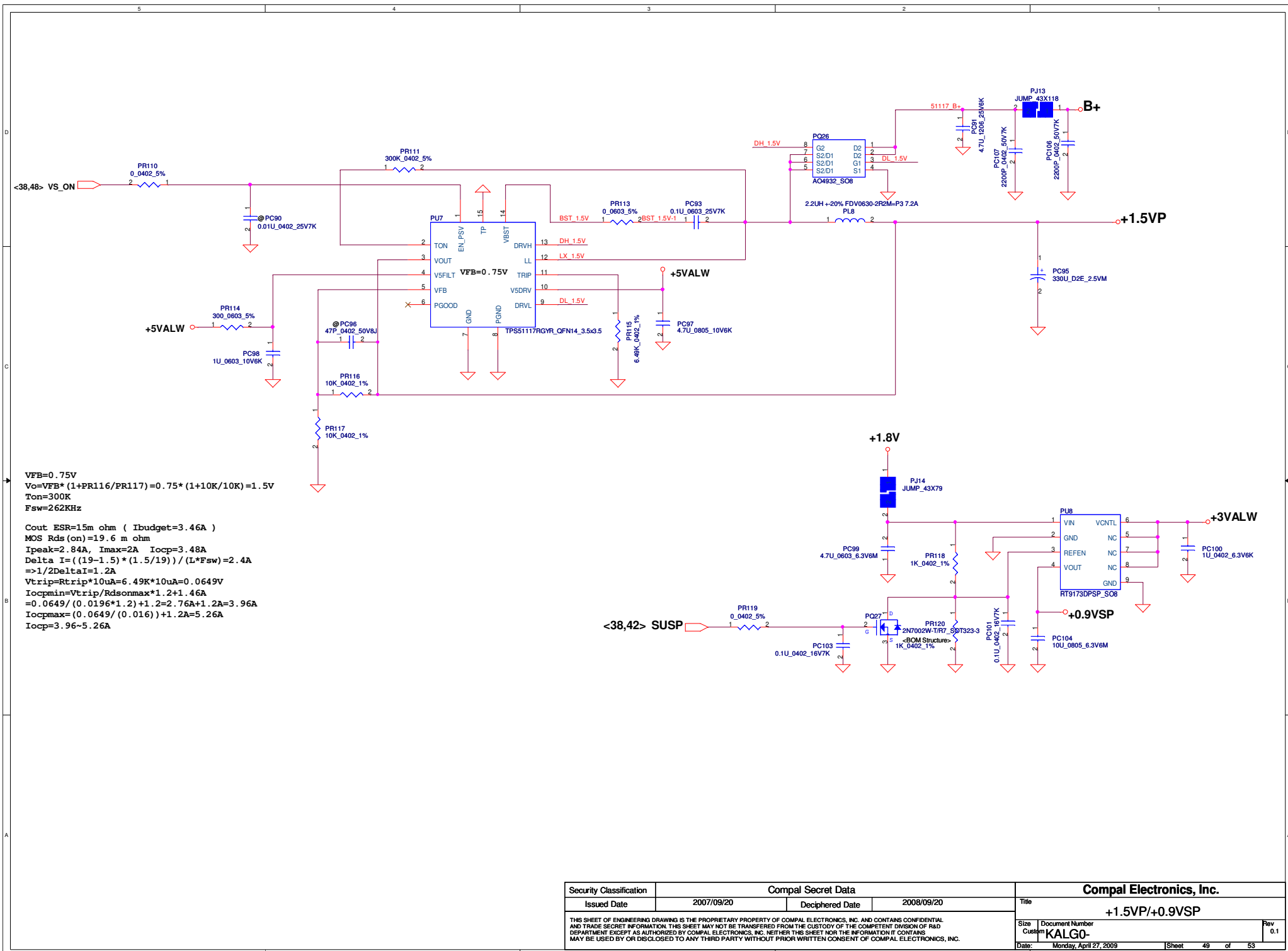


DCR 10m ohm(max) Cout ESR=15m ohm
 1.05VSP (Ibudget=17.47A) OCP Setting
 $F_{sw}=1/1.5E-10*22k = 303K$
 $V_o=V_{ref} * ((PR95+PR94)/PR94)$
 $I_{peak}=13.29A, I_{max}=9.31A$
 $I_{ocp}=13.29*1.2=15.95A$
 $\Delta I = 4.09A$
 $I_{ocp} * DCR = (Rocset * 9.5uA) = (15.95 * 1.3 * 10m; Roset = 21.8K$
 now chose Roset=22K
 $C_{sen} = L / (DCR * Roset) = 1uH / (10m * 22k); C_{sen} = 0.00523uF$
 now chose Csen=5600pF
 $I_{ocp_min} = (22K * 9.5uA) / (10m \text{ ohm} * 1.3) = 16.07A$
 $I_{ocp_max} = (22K * 10.5uA) / (10m \text{ ohm}) = 23.1A$



DCR 10m ohm(max) Cout ESR=15m ohm
 1.8VP (Ibudget=9.91A) Ipeak=9A, Imax=6.3 A
 $F_{sw}=1/1.5E-10*18.2k = 366K$
 $V_o=V_{ref} * ((PR97+PR99)/PR97)$
 $I_{ocp}=9*1.2=10.8A$
 $I_{ocp} * DCR = (Rocset * 9.5uA) = 10.67 * 1.3 * 10m; Roset = 14.78K$
 now chose Roset=14.7K
 $C_{sen} = L / (DCR * Roset) = 1uH / (10m * 14.7k); C_{sen} = 8.16nF$
 now chose Csen=8200pF
 $I_{ocp_min} = (14.7K * 9.5uA) / (10m \text{ ohm} * 1.3) = 10.74A$
 $I_{ocp_max} = (14.7 * 10.5uA) / (10m \text{ ohm}) = 15.43A$

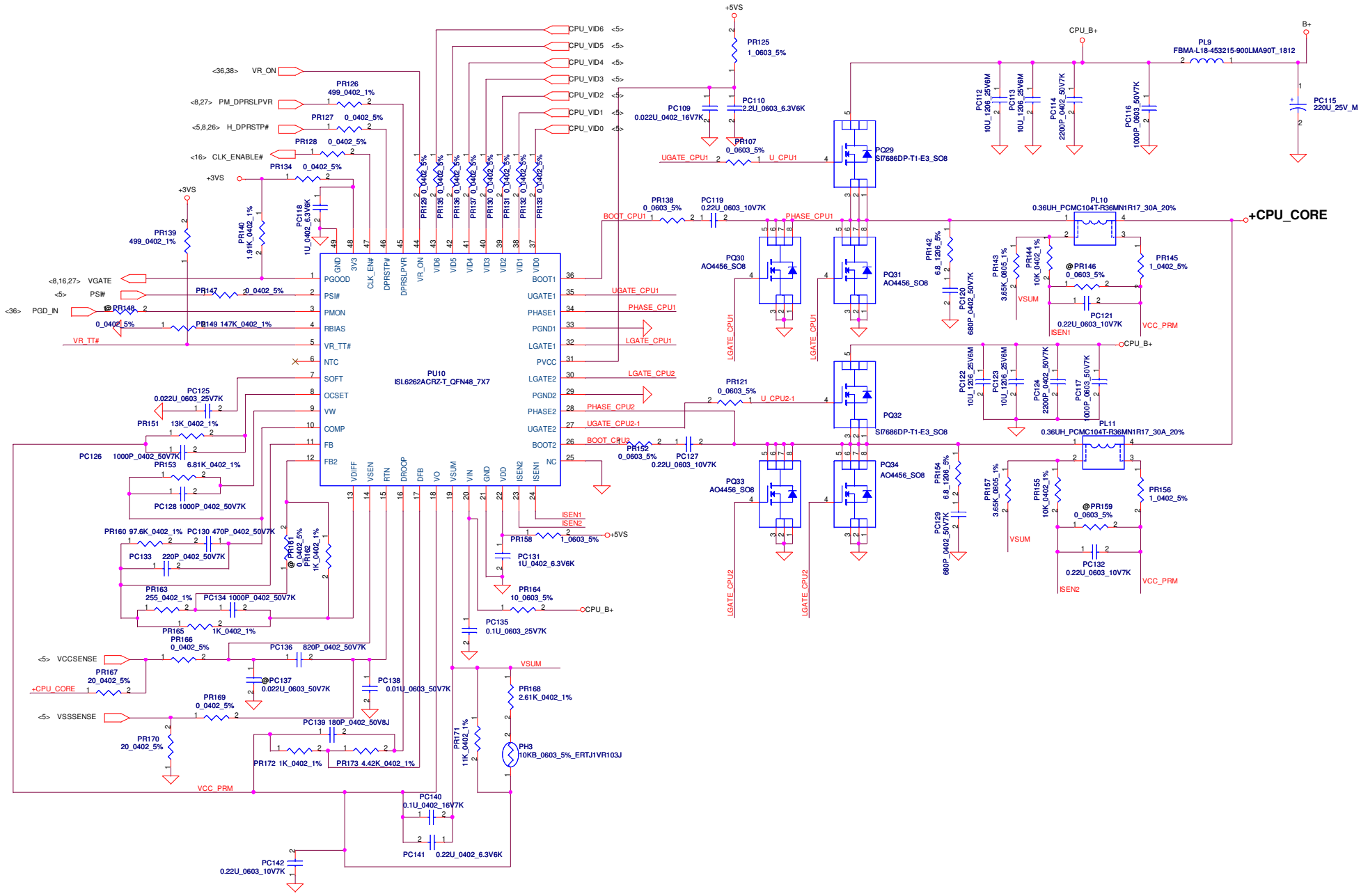
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	1.8VP / 1.05VSP
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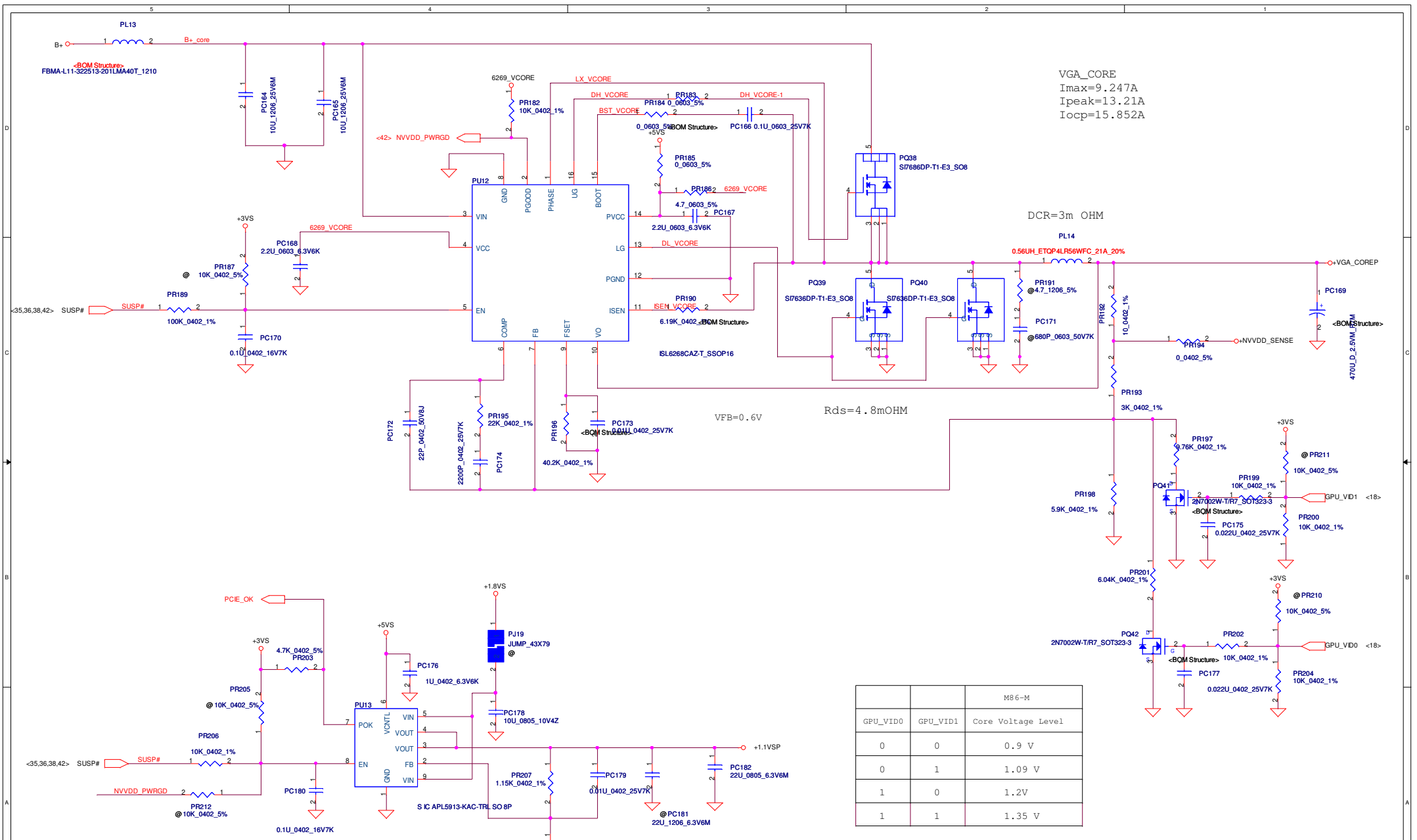
VFB=0.75V
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$
 $Ton = 300K$
 $Fsw = 262KHz$

Cout ESR=15m ohm (Ibudget=3.46A)
MOS Rds(on)=19.6 m ohm
Ipeak=2.84A, Imax=2A Iocp=3.48A
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Fsw) = 2.4A$
 $\Rightarrow 1/2 \Delta I = 1.2A$
 $V_{trip} = R_{trip} * I_{ocp} = 6.49K * 10uA = 0.0649V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.46A$
 $= 0.0649 / (0.0196 * 1.2) + 1.2 = 2.76A + 1.2A = 3.96A$
 $I_{ocpmax} = (0.0649 / (0.016)) + 1.2A = 5.26A$
 $I_{ocp} = 3.96 - 5.26A$

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VGA_CORE
 I_{max}=9.247A
 I_{peak}=13.21A
 I_{ocp}=15.852A

DCR=3m OHM

VFB=0.6V

R_{ds}=4.8mOHM

GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.9 V
0	1	1.09 V
1	0	1.2 V
1	1	1.35 V

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				VGA_CORE/1.1VSP	
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Version change list (P.I.R. List)

**Page 1 of 2
for PWR**

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR196 value	VGA OCP	0.3	50	change the resistance value of pr196 from 57.6K to 40.2K	2009/02/06	PVT
2	Change PL14 value	prevent OVP occur	0.3	50	change the inductance value of pl14 from 1uH to 0.56 uH	2009/02/06	PVT
3	Change PU4 IC part number	vender suggestion	0.3	45	change part number to SA00002V400	2009/02/06	PVT
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5							
6							

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				Rev	0.1

B --> C Change List

0220-----

Page 6, Change C98 BOM structure to @

0218-----

Page 20, Add R569 with BOM structure @

Page 23, R34, R38, R40, R53, R54, R55 change BOM structure to @

Page 31, Change R215 to 18K

Update Power Schematics

0213-----

Page 11, Delete R113

Add J1 JUMP_43X79 with BOM structure @

Page 31, R558, R559 0 ohm with BOM structure @

R560, R561 4.7K with BOM structure @

Page 32, R562, R563 0 ohm with BOM Structure @

R564, R565 0 ohm

Page 38, Delete C619

Add R566, R567, R568 0_0603 with BOM Structure JAL90@

0204-----

Page 12, Change L31 to MBK1608301YZF_0603 with BOM structure GM@

Change R163 to 0_0805_5%

Page 23, Change BOM Structure of U5 to @

Page 27, Change BOM Structure of R555 and R550 to @

Page 33, Change R217 to 31.6K_0402_1%

Change C313 to 1U_0603_10V6K

Page 34, Change R503 to FBMA-L10-160808-301LMT_0603

01/31-----

Page 23, Delete U10

01/29-----

Page 23, Change R152 BOM Structure to @

01/24-----

Page 4, Change U8 to SA00001Z700 (EMC1402)

Page 33, Change C338 to SE076104K80

Page 35, Mount C584

01/23-----

Page 38 Delete F3, R558-560, C609-614

01/22-----

Page 11, Delete R79

Change J1 Symbol to JUMP_43X79

Page 33, Add R557 10K (Check)

Change R245 BOM Structure with @

Page 38, Add C609-614, R558-560 (Check)

C607,608, 615-619 (Check)

01/17-----

Page 11, Add R79 0_0805

Update Power Schematics

01/16-----

Page 11, Delete R79 0_0805

Add J1 JUMP_43X79

Page 16, Change C296, R301 to 27P_0402

Page 19, Change L17, L19, L21 BOM structure to GM@

Page 23, Mount U29, R339

Add U10 with BOM structure @ (Co-lay with U5)

Change R340 Bom structure to @

Change U5 to MX25L4005AMC-12G_SO8 (SA00002A900)

Page 27, Change U26, C420 BOM structure to @

Change R550 to 0_0402

Add R555 0_0402

Page 32, Change R269 to 240_0402_5%, R267 to 453_0402_1%

Change R268 pin1 connect to +5VALW

Page 33, Change R217 to 18K_0402_1% with BOM structure PM@

Page 35, Add R551,R552, R553, R554 75_0603_1% with BOM structure JAL90@

Add D32 PJDLC05_SOT23-3

Page 38, Add F3 3A_15VDC_SMD2920P300TF15

Page 49, Add R551,R552, R553, R554 1K_0603_1% with BOM structure 268@

Add L17, L19, L21 0_0805 with BOM structure PM@

Update U38 (ALC268-VB1-GR) PN:SA00001GD10 for JAW50

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