Compal Confidential

PEW72/82/92 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2010-07-09

REV:1.0

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Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: Cover Page
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			Date: Friday, July 09, 2010; Sheet 1 of 44

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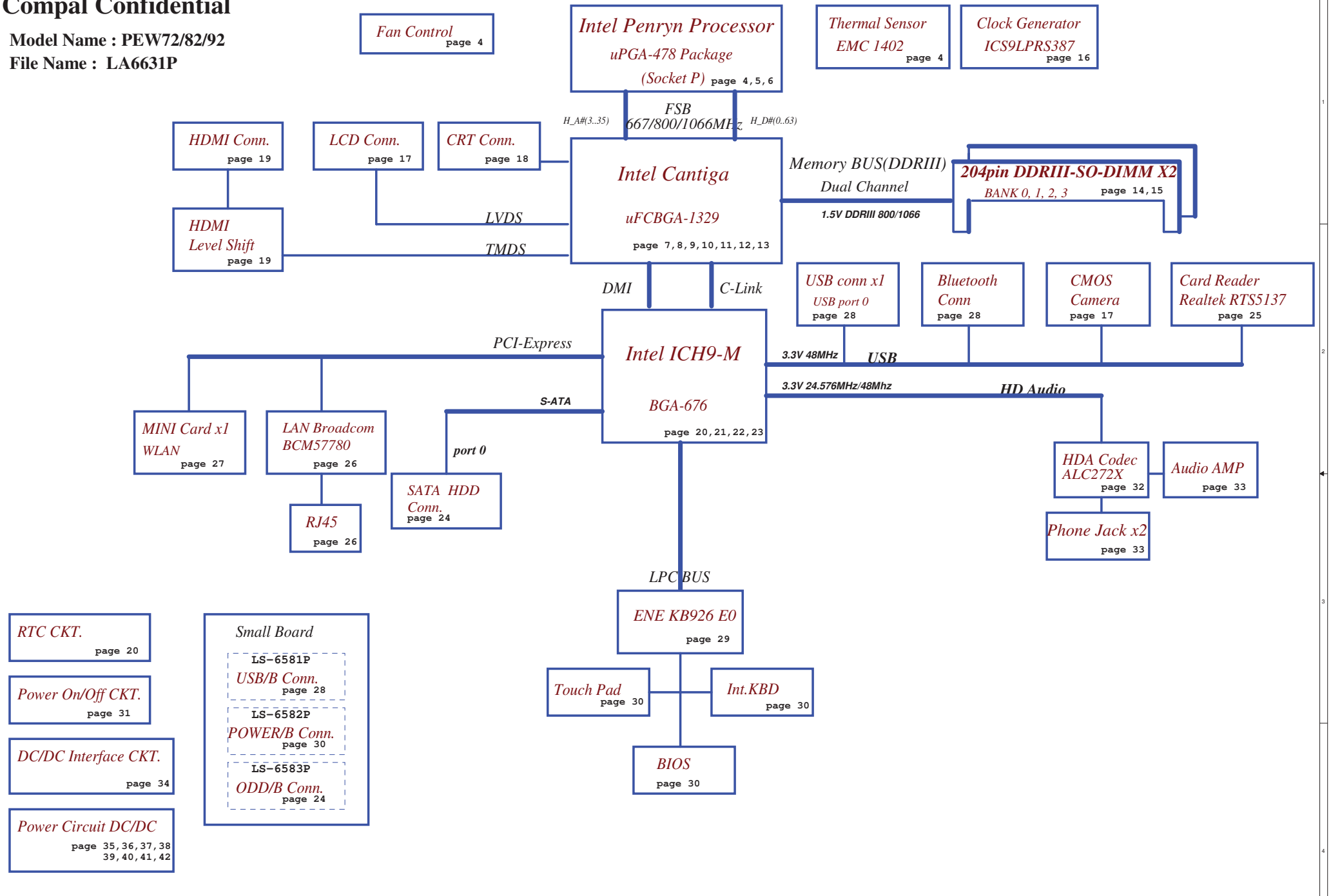
Model Name : PEW72/82/92
File Name : LA6631P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
SMSC EMC1402	100 1100 b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LVRS387, RTM890N)	1101 001Xb
DDR DIMM1	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45 B3	GM@
GM45 A1	GMA1@
GL40 B3	GL@
GM40 A1	GLA1@
Bluetooth	BT@

USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	USB/B Conn.
	UHCI2	Port2	
		Port3	CMOS Camera
	UHCI3	Port4	Card Reader
		Port5	
EHCI2	UHCI4	Port6	USB/B Conn.
		Port7	
	UHCI5	Port8	Blue Tooth
		Port9	
	UHCI6	Port10	Wireless Card
		Port11	

PCIE table

PCIE port1	
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

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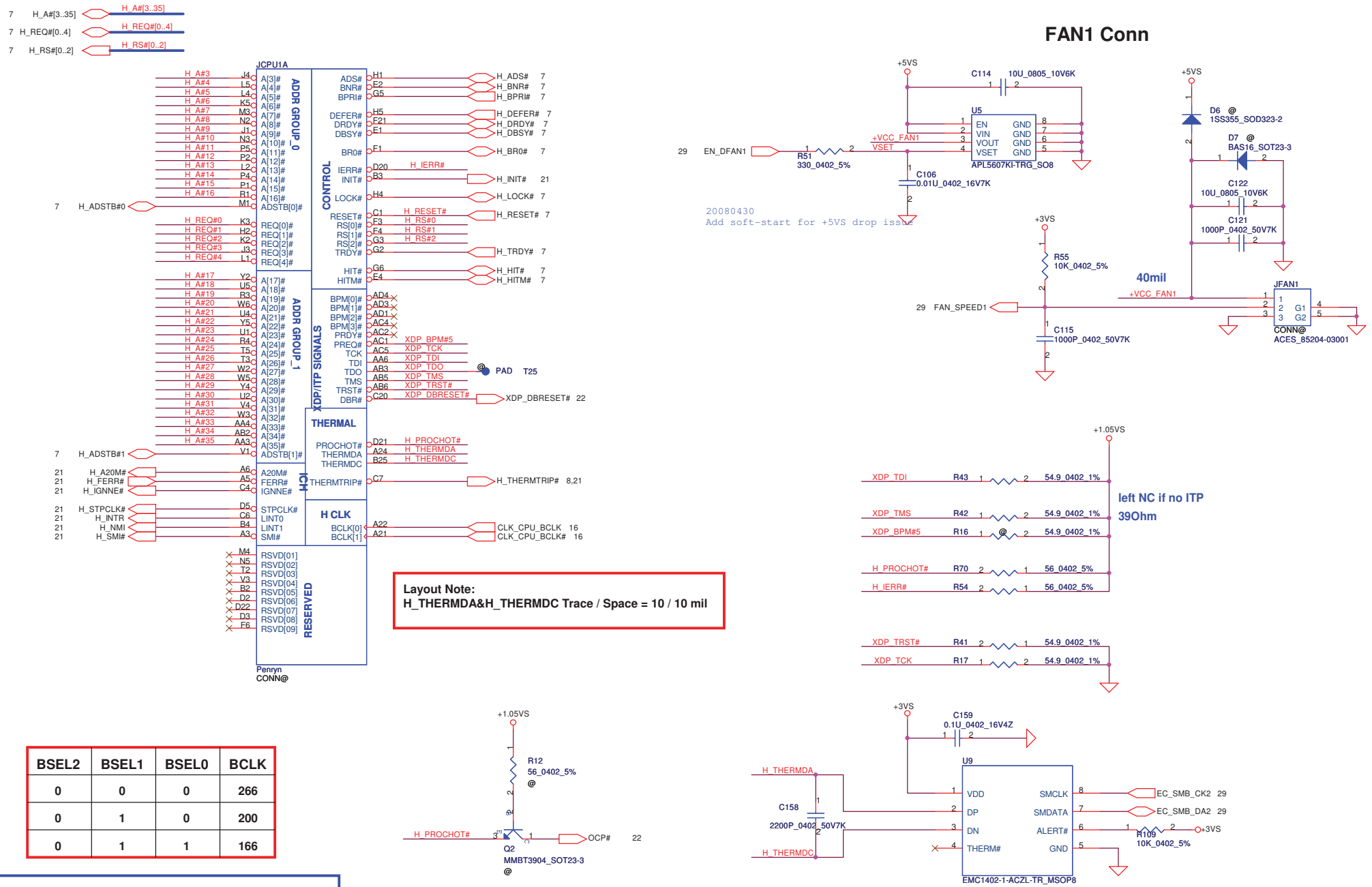

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

PCB

ZZZ

LA-6631P MB Rev1

DAZ0FZ00100

PCB PEW72 LA-6631P LS-6581P/6582P/6583P

LA-6631P MB Rev0: DA60000IU00

LA-6631P MB Rev1: DA60000IU10

LA-6631P MB with Small Board Rev1: DAZ0FZ00100

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Compal Electronics, Inc.

Title: Penryn (1/3) & FAN

Size: B | Document Number: PEW72/82 M/B LA-6631P Schematic | Rev: 1.0

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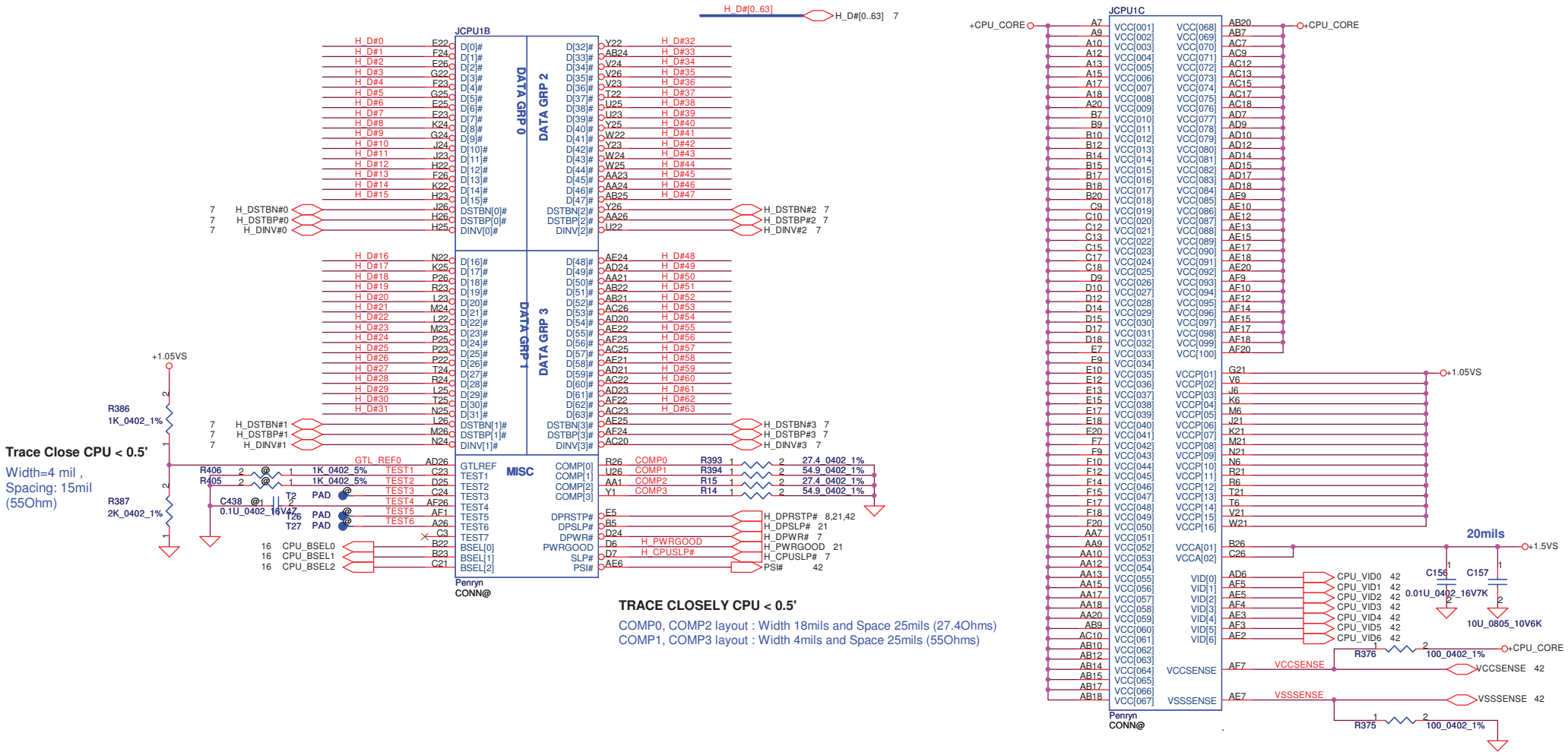

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Compal Electronics, Inc.

Title: Penryn (2/3)

Size	Document Number	Rev
B	PEW72/82 M/B LA-6631P Schematic	1.0

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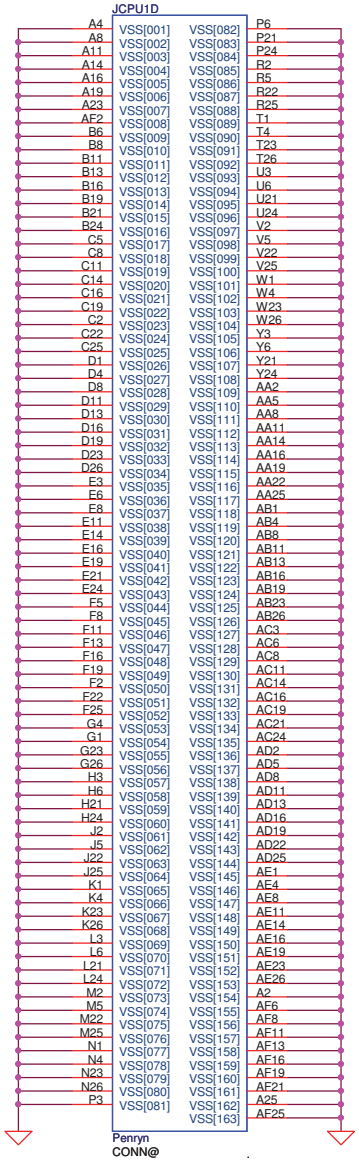
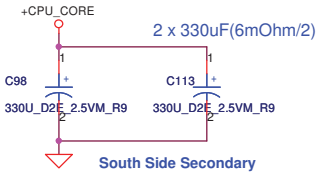
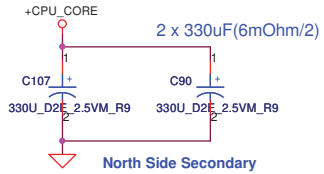
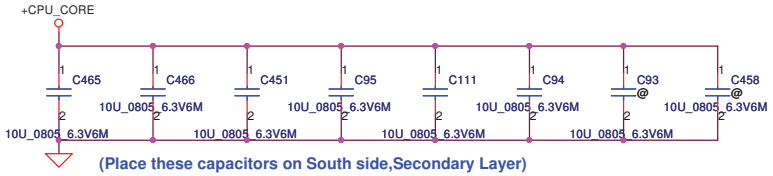
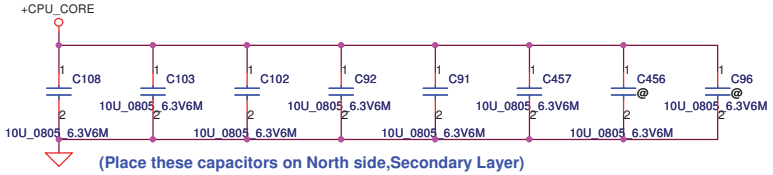
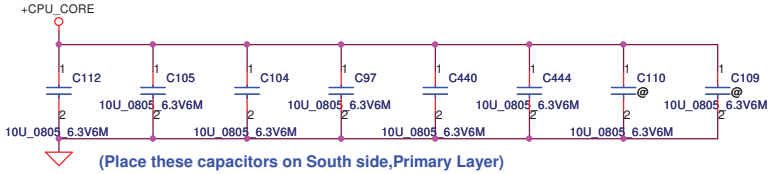


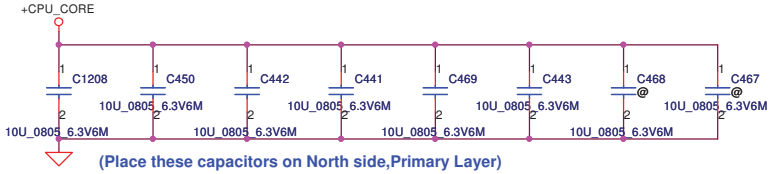




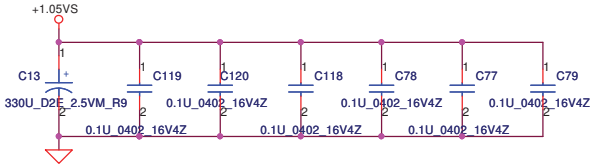








+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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Title: Penryn (3/3)

Size	Document Number	Rev
B	PEW72/82 M/B LA-6631P Schematic	1.0

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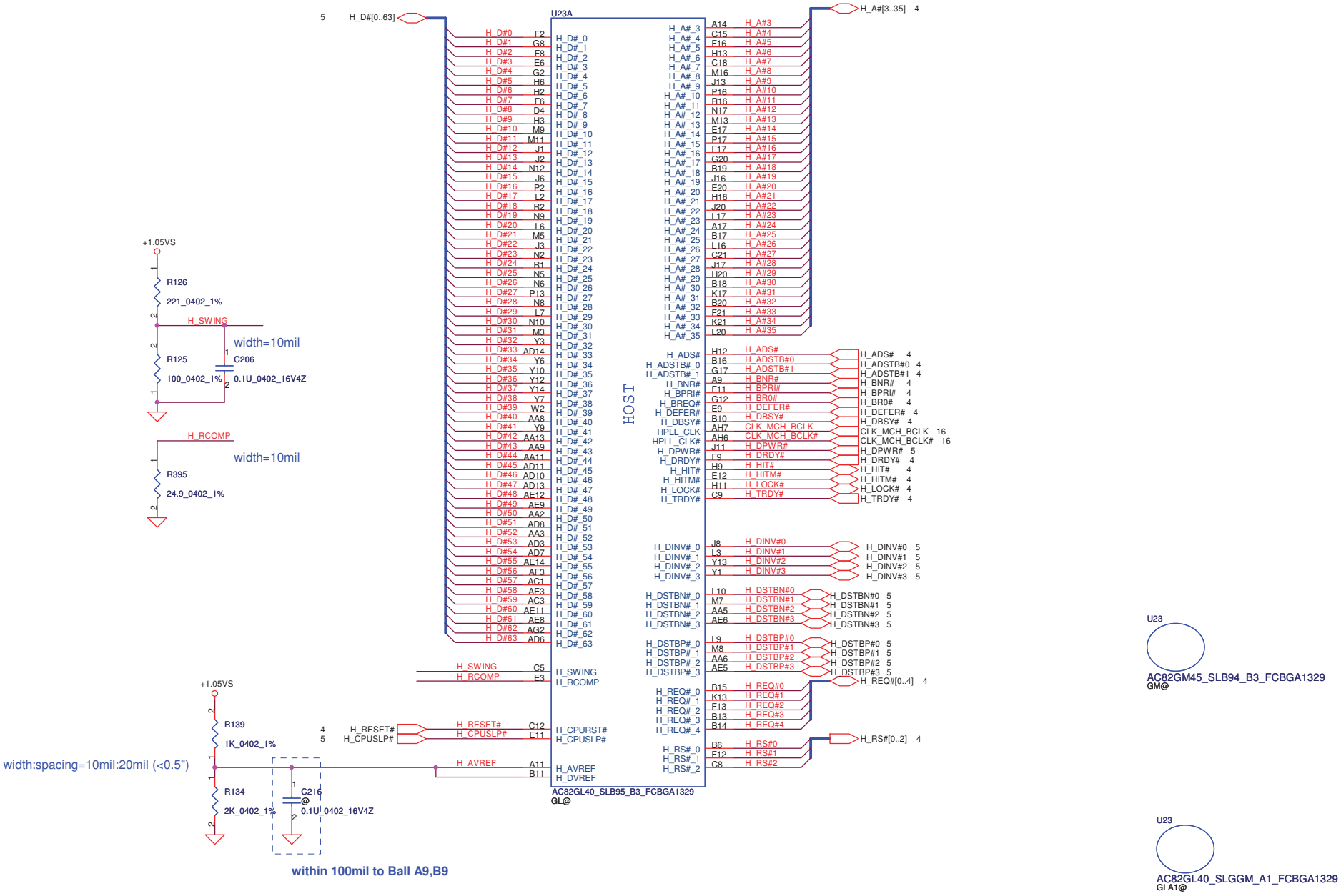

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Compal Electronics, Inc.	
Title	Cantiga GMCH(1/7)-GTL
Size B	Document Number PEW72/82 M/B LA-6631P Schematic
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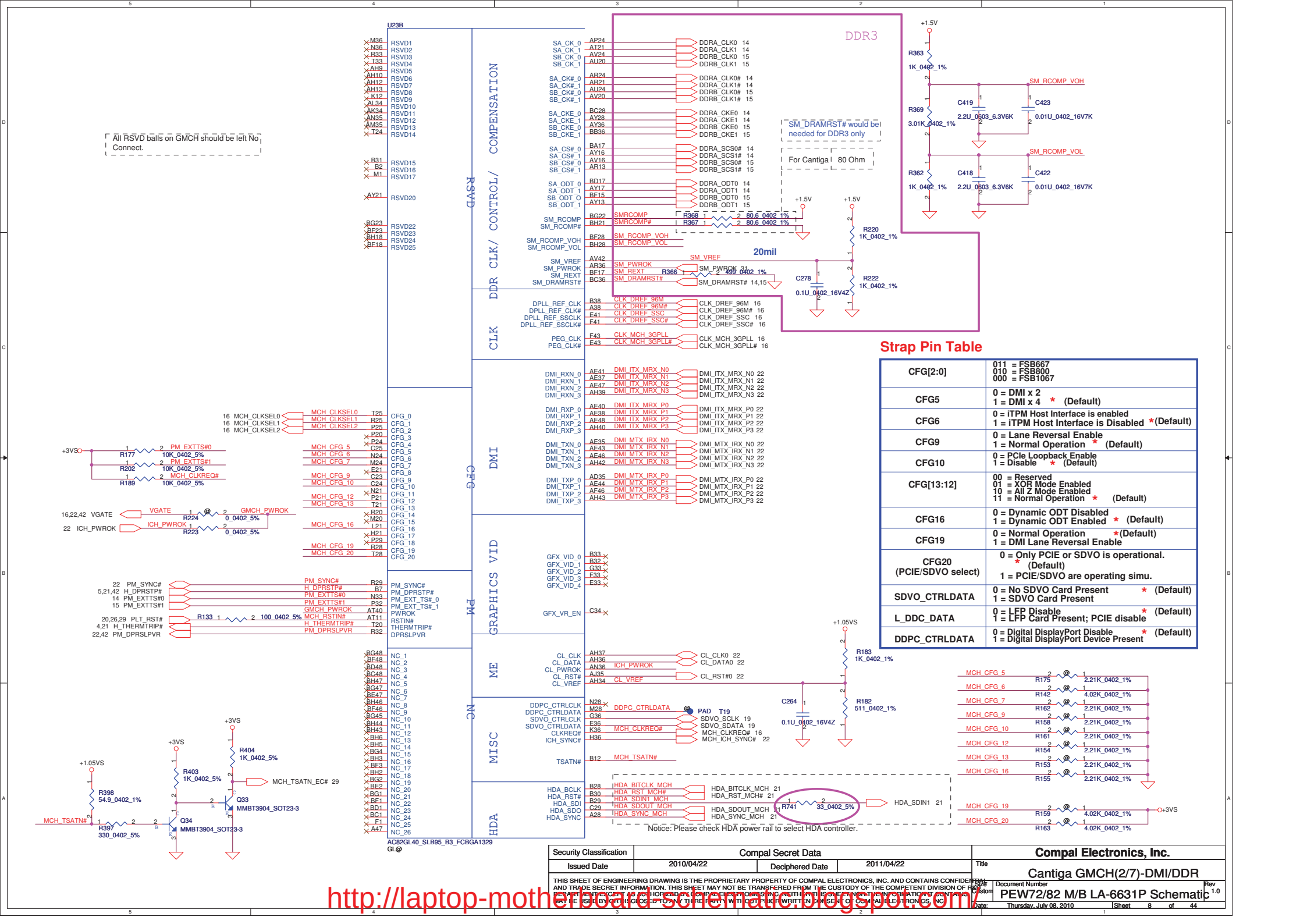
U23B
All RSVD balls on GMCH should be left No Connect.
RSVD
CFG
DMI
PM
GRAPHICS VID
ME
NC
MISC
HDA
CLK DDR CLK/ CONTROL/ COMPENSATION
DDR3
SM_DRAMRST# would be needed for DDR3 only
For Cantiga 80 Ohm
20mil
Strap Pin Table
CFG[2:0] 011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6 0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9 0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10 0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12] 00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19 0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select) 0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA 0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA 0 = LFP Disable * (Default) 1 = LFP Card Present; PCIE disable
DDPC_CTRLDATA 0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present
Notice: Please check HDA power rail to select HDA controller.
AC82GL40_SLB95_B3_FCBGA1329
GL@
Security Classification Compal Secret Data
Issued Date 2010/04/22 Deciphered Date 2011/04/22
Compal Electronics, Inc.
Title Cantiga GMCH(2/7)-DMI/DDR
Size B Document Number PEW72/82 M/B LA-6631P Schematic Rev 1.0
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http://laptop-motherboard-schematic.blogspot.com/

14 DDR_A_D[0..63] → DDR_A_D[0..63]
14 DDR_A_DM[0..7] → DDR_A_DM[0..7]
14 DDR_A_MA[0..14] → DDR_A_MA[0..14]
14 DDR_A_DQS#[0..7] → DDR_A_DQS#[0..7]

15 DDR_B_D[0..63] → DDR_B_DQ[0..63]
15 DDR_B_DM[0..7] → DDR_B_DM[0..7]
15 DDR_B_MA[0..14] → DDR_B_MA[0..14]
15 DDR_B_DQS#[0..7] → DDR_B_DQS#[0..7]

U23D

DDR_A_D0	AJ38	SA_DQ_0			
DDR_A_D1	AJ41	SA_DQ_1			
DDR_A_D2	AN38	SA_DQ_2			
DDR_A_D3	AM38	SA_DQ_3			
DDR_A_D4	AJ36	SA_DQ_4			
DDR_A_D5	AJ40	SA_DQ_5			
DDR_A_D6	AM44	SA_DQ_6			
DDR_A_D7	AM42	SA_DQ_7			
DDR_A_D8	AN43	SA_DQ_8			
DDR_A_D9	AN44	SA_DQ_9			
DDR_A_D10	AU40	SA_DQ_10			
DDR_A_D11	AT38	SA_DQ_11			
DDR_A_D12	AN41	SA_DQ_12			
DDR_A_D13	AN39	SA_DQ_13			
DDR_A_D14	AU44	SA_DQ_14			
DDR_A_D15	AU42	SA_DQ_15			
DDR_A_D16	AV39	SA_DQ_16			
DDR_A_D17	AY44	SA_DQ_17			
DDR_A_D18	BA40	SA_DQ_18			
DDR_A_D19	BD43	SA_DQ_19			
DDR_A_D20	AV41	SA_DQ_20			
DDR_A_D21	AY43	SA_DQ_21			
DDR_A_D22	BB41	SA_DQ_22			
DDR_A_D23	BC40	SA_DQ_23			
DDR_A_D24	AY37	SA_DQ_24			
DDR_A_D25	BD38	SA_DQ_25			
DDR_A_D26	AV37	SA_DQ_26			
DDR_A_D27	AT36	SA_DQ_27			
DDR_A_D28	AY38	SA_DQ_28			
DDR_A_D29	BB38	SA_DQ_29			
DDR_A_D30	AV36	SA_DQ_30			
DDR_A_D31	AW36	SA_DQ_31			
DDR_A_D32	BD13	SA_DQ_32			
DDR_A_D33	AU11	SA_DQ_33			
DDR_A_D34	BC11	SA_DQ_34			
DDR_A_D35	BA12	SA_DQ_35			
DDR_A_D36	AU13	SA_DQ_36			
DDR_A_D37	AV13	SA_DQ_37			
DDR_A_D38	BD12	SA_DQ_38			
DDR_A_D39	BC12	SA_DQ_39			
DDR_A_D40	BB9	SA_DQ_40			
DDR_A_D41	BA9	SA_DQ_41			
DDR_A_D42	AU10	SA_DQ_42			
DDR_A_D43	AV9	SA_DQ_43			
DDR_A_D44	BA11	SA_DQ_44			
DDR_A_D45	BD9	SA_DQ_45			
DDR_A_D46	AY8	SA_DQ_46			
DDR_A_D47	BA6	SA_DQ_47			
DDR_A_D48	AV5	SA_DQ_48			
DDR_A_D49	AV7	SA_DQ_49			
DDR_A_D50	AT9	SA_DQ_50			
DDR_A_D51	AN8	SA_DQ_51			
DDR_A_D52	AU5	SA_DQ_52			
DDR_A_D53	AU6	SA_DQ_53			
DDR_A_D54	AT5	SA_DQ_54			
DDR_A_D55	AN10	SA_DQ_55			
DDR_A_D56	AM11	SA_DQ_56			
DDR_A_D57	AM5	SA_DQ_57			
DDR_A_D58	AJ9	SA_DQ_58			
DDR_A_D59	AJ8	SA_DQ_59			
DDR_A_D60	AN12	SA_DQ_60			
DDR_A_D61	AM13	SA_DQ_61			
DDR_A_D62	AJ11	SA_DQ_62			
DDR_A_D63	AJ12	SA_DQ_63			

		SA_BS_0	BD21	DDR_A_BS0	14
		SA_BS_1	BG18	DDR_A_BS1	14
		SA_BS_2	AT25	DDR_A_BS2	14
		SA_RAS#	BB20	DDR_A_RAS#	14
		SA_CAS#	BD20	DDR_A_CAS#	14
		SA_WE#	AY20	DDR_A_WE#	14
		SA_DM_0	AM37	DDR_A_DM0	
		SA_DM_1	AT41	DDR_A_DM1	
		SA_DM_2	AY41	DDR_A_DM2	
		SA_DM_3	AU39	DDR_A_DM3	
		SA_DM_4	BB12	DDR_A_DM4	
		SA_DM_5	AY6	DDR_A_DM5	
		SA_DM_6	AT7	DDR_A_DM6	
		SA_DM_7	AJ5	DDR_A_DM7	
		SA_DQS_0	AJ44	DDR_A_DQS0	14
		SA_DQS_1	AT44	DDR_A_DQS1	14
		SA_DQS_2	BA43	DDR_A_DQS2	14
		SA_DQS_3	BC37	DDR_A_DQS3	14
		SA_DQS_4	AW12	DDR_A_DQS4	14
		SA_DQS_5	BC8	DDR_A_DQS5	14
		SA_DQS_6	AU8	DDR_A_DQS6	14
		SA_DQS_7	AM7	DDR_A_DQS7	14
		SA_DQS#_0	AJ43	DDR_A_DQS#0	
		SA_DQS#_1	AT43	DDR_A_DQS#1	
		SA_DQS#_2	BA44	DDR_A_DQS#2	
		SA_DQS#_3	BD37	DDR_A_DQS#3	
		SA_DQS#_4	AY12	DDR_A_DQS#4	
		SA_DQS#_5	BD8	DDR_A_DQS#5	
		SA_DQS#_6	AU9	DDR_A_DQS#6	
		SA_DQS#_7	AM8	DDR_A_DQS#7	
		SA_MA_0	BA21	DDR_A_MA0	
		SA_MA_1	BC24	DDR_A_MA1	
		SA_MA_2	BG24	DDR_A_MA2	
		SA_MA_3	BH24	DDR_A_MA3	
		SA_MA_4	BG25	DDR_A_MA4	
		SA_MA_5	BA24	DDR_A_MA5	
		SA_MA_6	BD24	DDR_A_MA6	
		SA_MA_7	BG27	DDR_A_MA7	
		SA_MA_8	BF25	DDR_A_MA8	
		SA_MA_9	AW24	DDR_A_MA9	
		SA_MA_10	BC21	DDR_A_MA10	
		SA_MA_11	BG26	DDR_A_MA11	
		SA_MA_12	BH26	DDR_A_MA12	
		SA_MA_13	BH17	DDR_A_MA13	
		SA_MA_14	AY25	DDR_A_MA14	

DDR SYSTEM MEMORY A

AC82GL40_SLB95_B3_FCBGA1329
GL@

U23E

DDR_B_D0	AK47	SB_DQ_0			
DDR_B_D1	AH46	SB_DQ_1			
DDR_B_D2	AP47	SB_DQ_2			
DDR_B_D3	AP46	SB_DQ_3			
DDR_B_D4	AJ46	SB_DQ_4			
DDR_B_D5	AJ48	SB_DQ_5			
DDR_B_D6	AM48	SB_DQ_6			
DDR_B_D7	AP48	SB_DQ_7			
DDR_B_D8	AU47	SB_DQ_8			
DDR_B_D9	AU46	SB_DQ_9			
DDR_B_D10	BA48	SB_DQ_10			
DDR_B_D11	AY48	SB_DQ_11			
DDR_B_D12	AT47	SB_DQ_12			
DDR_B_D13	AR47	SB_DQ_13			
DDR_B_D14	BA47	SB_DQ_14			
DDR_B_D15	BC47	SB_DQ_15			
DDR_B_D16	BC46	SB_DQ_16			
DDR_B_D17	BC44	SB_DQ_17			
DDR_B_D18	BG43	SB_DQ_18			
DDR_B_D19	BF43	SB_DQ_19			
DDR_B_D20	BF45	SB_DQ_20			
DDR_B_D21	BC41	SB_DQ_21			
DDR_B_D22	BF40	SB_DQ_22			
DDR_B_D23	BF41	SB_DQ_23			
DDR_B_D24	BG38	SB_DQ_24			
DDR_B_D25	BF38	SB_DQ_25			
DDR_B_D26	BH35	SB_DQ_26			
DDR_B_D27	BG35	SB_DQ_27			
DDR_B_D28	BH40	SB_DQ_28			
DDR_B_D29	BG39	SB_DQ_29			
DDR_B_D30	BG34	SB_DQ_30			
DDR_B_D31	BH34	SB_DQ_31			
DDR_B_D32	BH14	SB_DQ_32			
DDR_B_D33	BG12	SB_DQ_33			
DDR_B_D34	BH11	SB_DQ_34			
DDR_B_D35	BG8	SB_DQ_35			
DDR_B_D36	BH12	SB_DQ_36			
DDR_B_D37	BF11	SB_DQ_37			
DDR_B_D38	BF8	SB_DQ_38			
DDR_B_D39	BG7	SB_DQ_39			
DDR_B_D40	BC5	SB_DQ_40			
DDR_B_D41	BC6	SB_DQ_41			
DDR_B_D42	AY3	SB_DQ_42			
DDR_B_D43	AY1	SB_DQ_43			
DDR_B_D44	BF6	SB_DQ_44			
DDR_B_D45	BF5	SB_DQ_45			
DDR_B_D46	BA1	SB_DQ_46			
DDR_B_D47	BD3	SB_DQ_47			
DDR_B_D48	AV2	SB_DQ_48			
DDR_B_D49	AU3	SB_DQ_49			
DDR_B_D50	AR3	SB_DQ_50			
DDR_B_D51	AN2	SB_DQ_51			
DDR_B_D52	AY2	SB_DQ_52			
DDR_B_D53	AV1	SB_DQ_53			
DDR_B_D54	AP3	SB_DQ_54			
DDR_B_D55	AR1	SB_DQ_55			
DDR_B_D56	AL1	SB_DQ_56			
DDR_B_D57	AL2	SB_DQ_57			
DDR_B_D58	AJ1	SB_DQ_58			
DDR_B_D59	AH1	SB_DQ_59			
DDR_B_D60	AM2	SB_DQ_60			
DDR_B_D61	AM3	SB_DQ_61			
DDR_B_D62	AH3	SB_DQ_62			
DDR_B_D63	AJ3	SB_DQ_63			

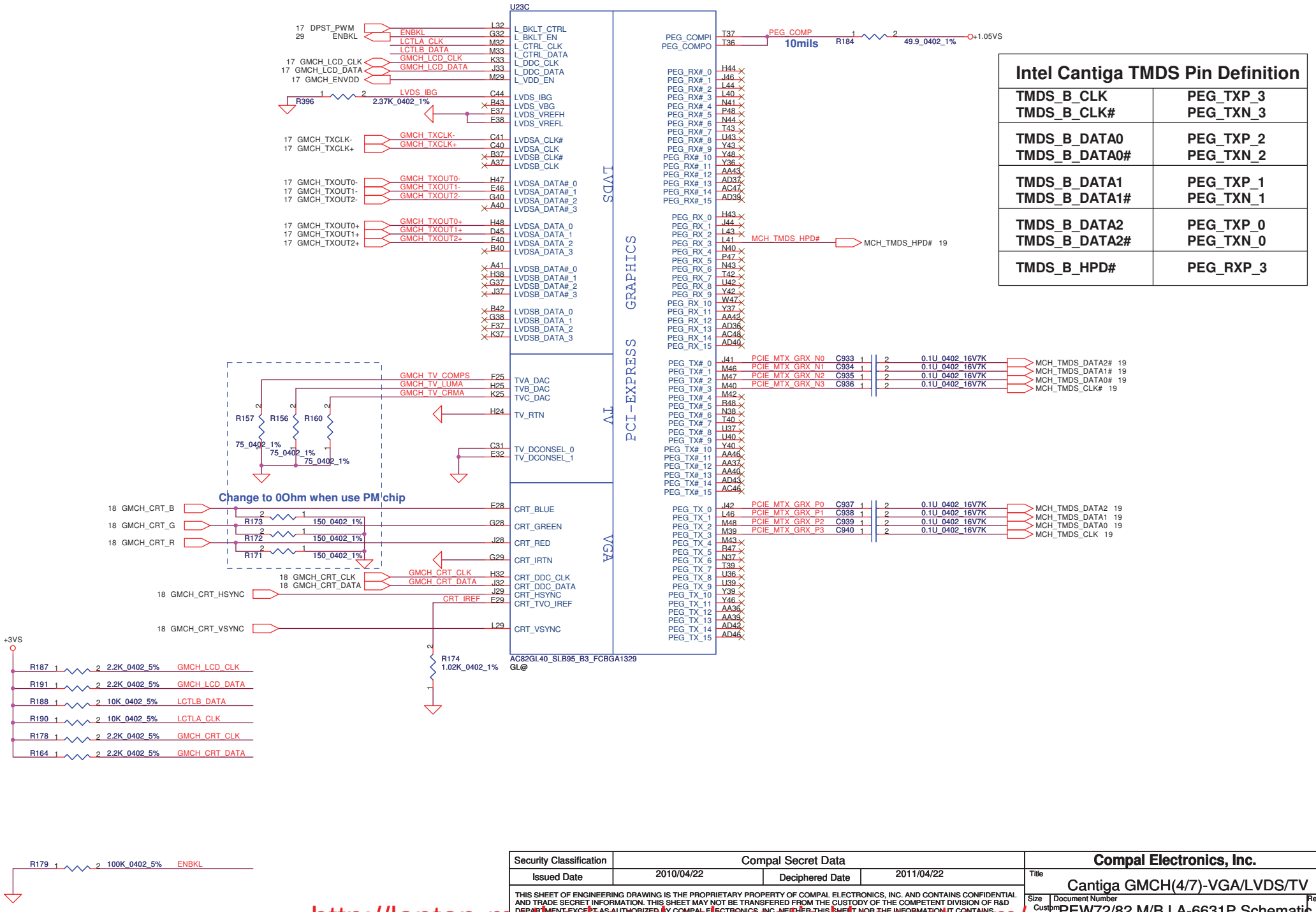
		SB_BS_0	BC16	DDR_B_BS0	15
		SB_BS_1	BB17	DDR_B_BS1	15
		SB_BS_2	BB33	DDR_B_BS2	15
		SB_RAS#	AU17	DDR_B_RAS#	15
		SB_CAS#	BG16	DDR_B_CAS#	15
		SB_WE#	BF14	DDR_B_WE#	15
		SB_DM_0	AM47	DDR_B_DM0	
		SB_DM_1	AY47	DDR_B_DM1	
		SB_DM_2	BD40	DDR_B_DM2	
		SB_DM_3	BF35	DDR_B_DM3	
		SB_DM_4	BG11	DDR_B_DM4	
		SB_DM_5	BA3	DDR_B_DM5	
		SB_DM_6	AP1	DDR_B_DM6	
		SB_DM_7	AK2	DDR_B_DM7	
		SB_DQS_0	AL47	DDR_B_DQS0	15
		SB_DQS_1	AV48	DDR_B_DQS1	15
		SB_DQS_2	BG41	DDR_B_DQS2	15
		SB_DQS_3	BG37	DDR_B_DQS3	15
		SB_DQS_4	BH9	DDR_B_DQS4	15
		SB_DQS_5	BB2	DDR_B_DQS5	15
		SB_DQS_6	AU1	DDR_B_DQS6	15
		SB_DQS_7	AN6	DDR_B_DQS7	15
		SB_DQS#_0	AL46	DDR_B_DQS#0	
		SB_DQS#_1	AV47	DDR_B_DQS#1	
		SB_DQS#_2	BH41	DDR_B_DQS#2	
		SB_DQS#_3	BH37	DDR_B_DQS#3	
		SB_DQS#_4	BG9	DDR_B_DQS#4	
		SB_DQS#_5	BC2	DDR_B_DQS#5	
		SB_DQS#_6	AT2	DDR_B_DQS#6	
		SB_DQS#_7	AN5	DDR_B_DQS#7	
		SB_MA_0	AV17	DDR_B_MA0	
		SB_MA_1	BA25	DDR_B_MA1	
		SB_MA_2	BC25	DDR_B_MA2	
		SB_MA_3	AU25	DDR_B_MA3	
		SB_MA_4	AW25	DDR_B_MA4	
		SB_MA_5	BB28	DDR_B_MA5	
		SB_MA_6	AU28	DDR_B_MA6	
		SB_MA_7	AW28	DDR_B_MA7	
		SB_MA_8	AT33	DDR_B_MA8	
		SB_MA_9	BD33	DDR_B_MA9	
		SB_MA_10	BB16	DDR_B_MA10	
		SB_MA_11	AW33	DDR_B_MA11	
		SB_MA_12	AY33	DDR_B_MA12	
		SB_MA_13	BH15	DDR_B_MA13	
		SB_MA_14	AU33	DDR_B_MA14	

DDR SYSTEM MEMORY B

AC82GL40_SLB95_B3_FCBGA1329
GL@

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.	
Title	Cantiga GMCH(3/7)-DDR
Size B	Document Number PEW72/82 M/B LA-6631P Schematic
Rev	1.0
Date: Thursday, July 08, 2010	Sheet 9 of 44



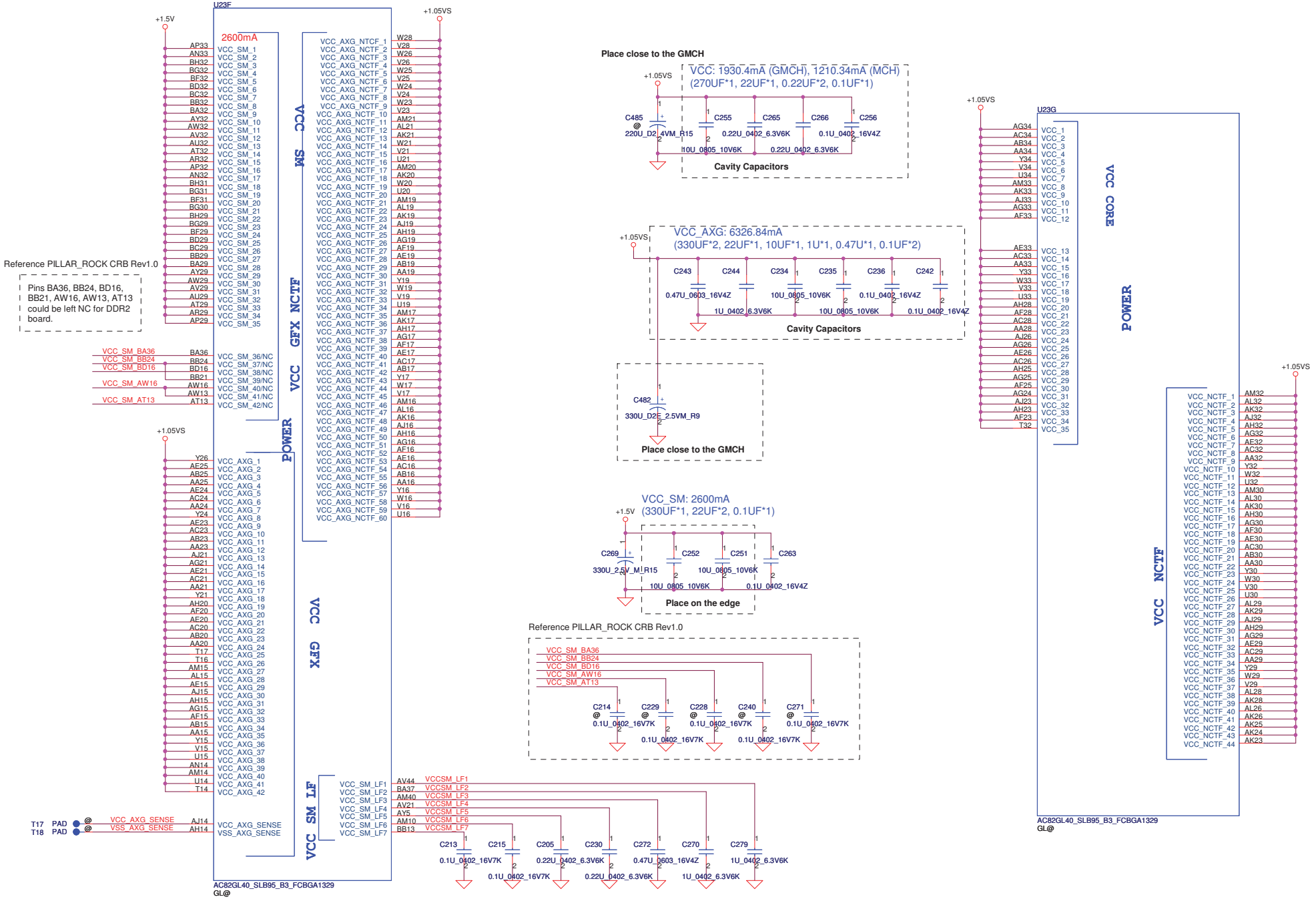
Intel Cantiga TMDS Pin Definition

TMDS_B_CLK TMDS_B_CLK#	PEG_TXP_3 PEG_TXN_3
TMDS_B_DATA0 TMDS_B_DATA0#	PEG_TXP_2 PEG_TXN_2
TMDS_B_DATA1 TMDS_B_DATA1#	PEG_TXP_1 PEG_TXN_1
TMDS_B_DATA2 TMDS_B_DATA2#	PEG_TXP_0 PEG_TXN_0
TMDS_B_HPD#	PEG_RXP_3

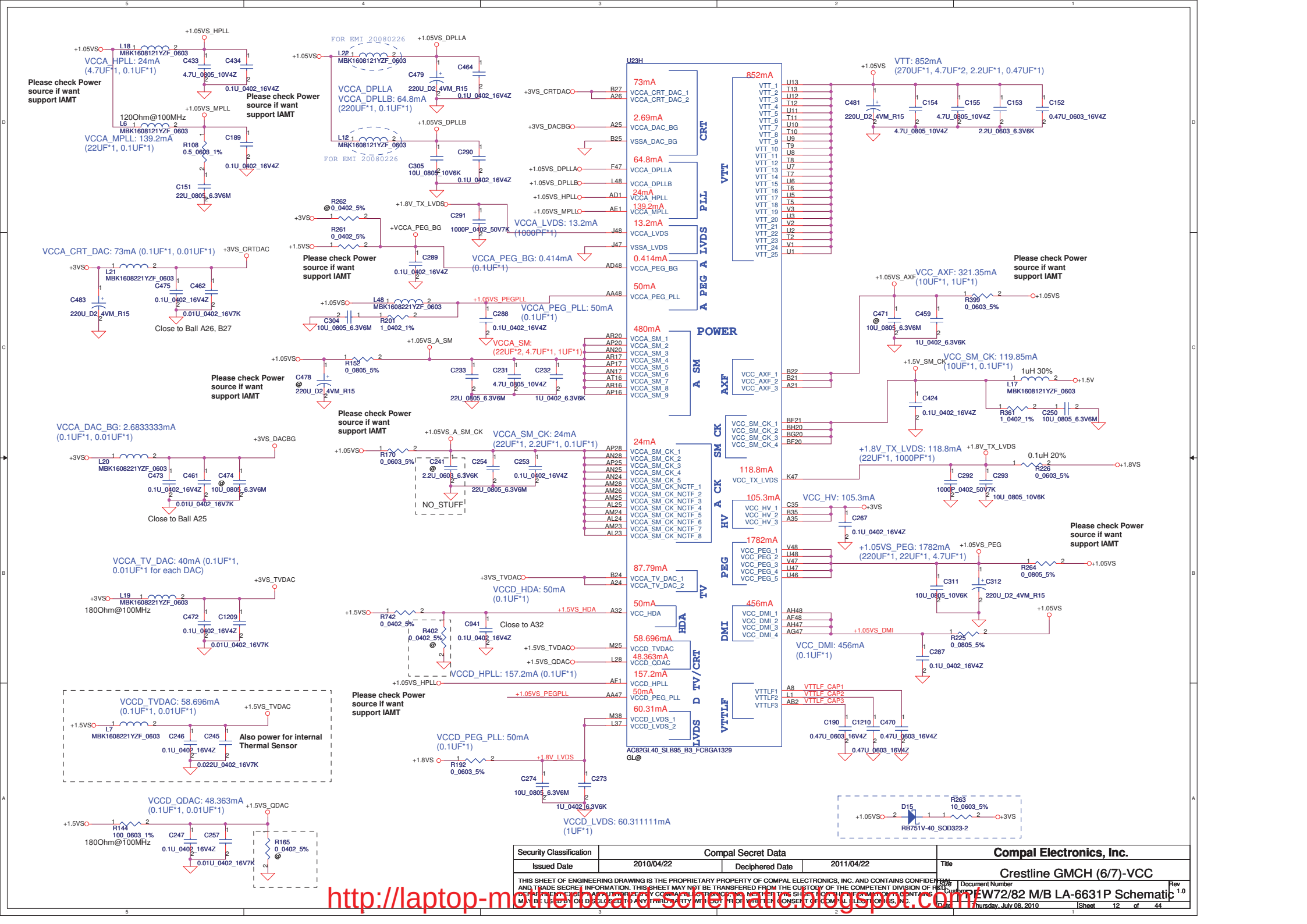
Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

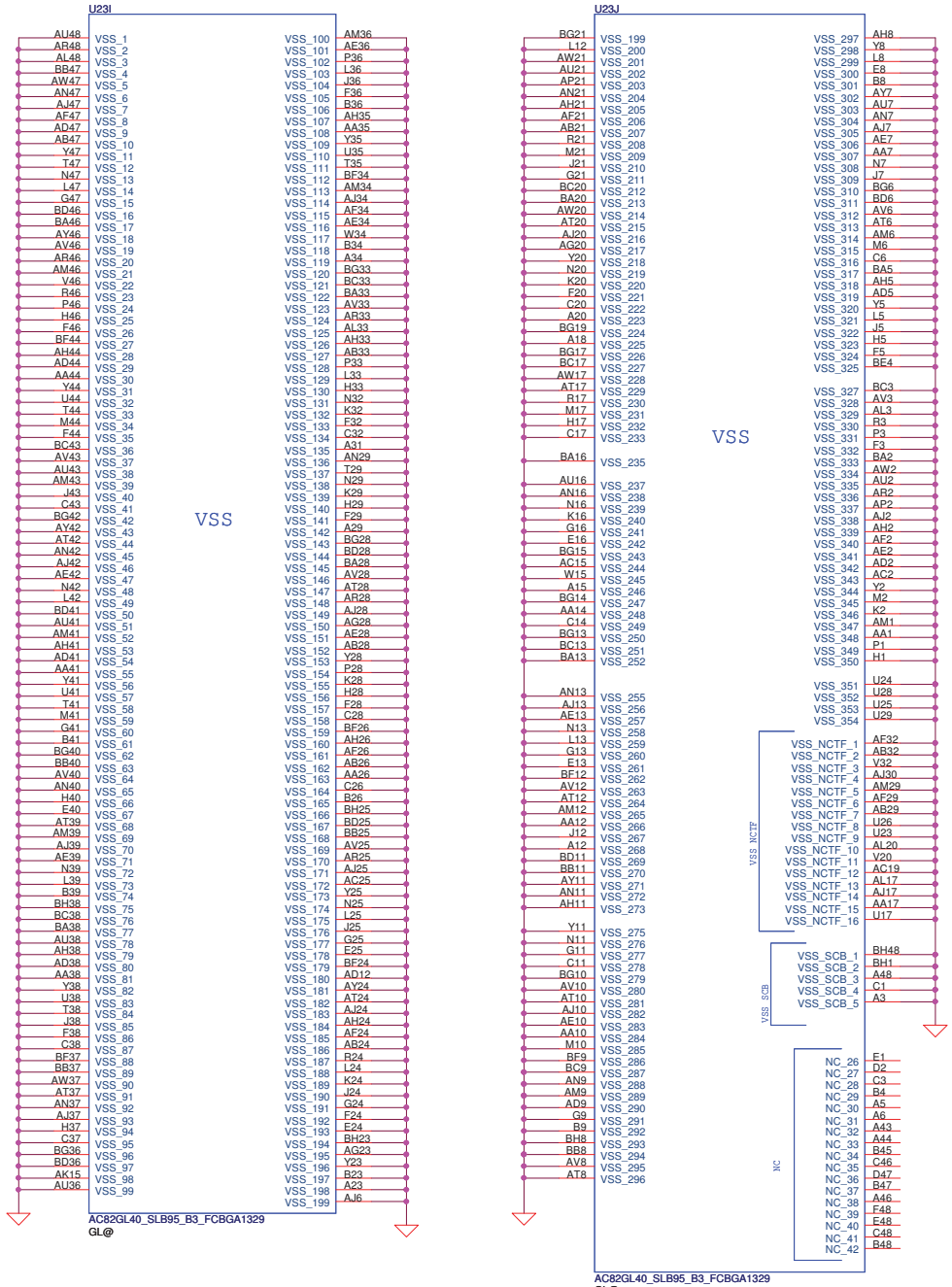
Compal Electronics, Inc.

Title	Cantiga GMCH(4/7)-VGA/LVDS/TV
Size: Custom	Document Number: PEW72/82 M/B LA-6631P Schematic
Rev	1.0
Date: Thursday, July 08, 2010	Sheet 10 of 44



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: Cantiga GMCH(5/7)-VCC
Size: B/28 Custom	Document Number: PEW72/82 M/B LA-6631P Schematic		Rev: 1.0
Date: Thursday, July 08, 2010	Sheet 11 of 44		





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: Cantiga GMCH(7/7)-GND
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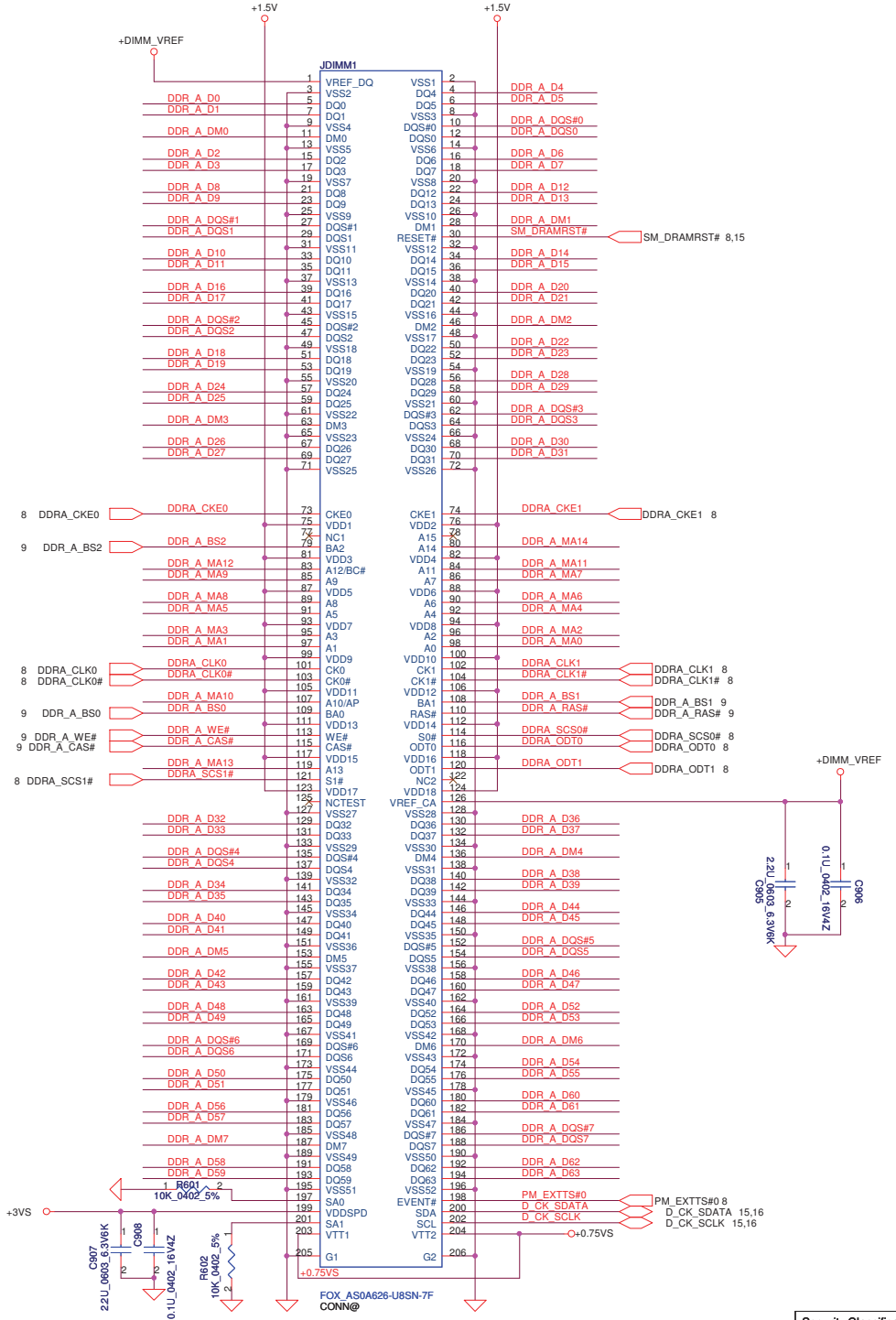
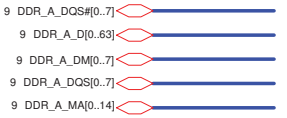
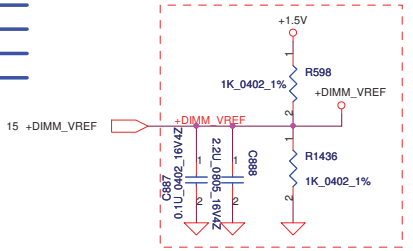
			Date: Thursday, July 08, 2010; Sheet 13 of 44



DIMM_A STD H:8mm

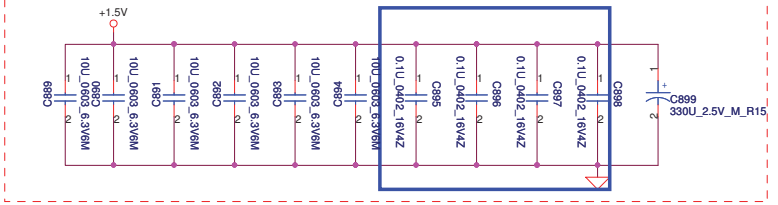
<Address: 00>



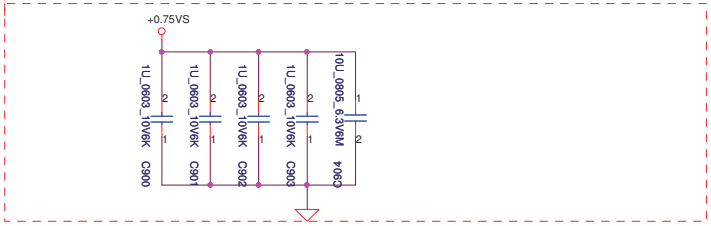


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDIMM2.203 & JDIMM2.204



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Issued Date	2010/04/22	Deciphered Date	2011/04/22

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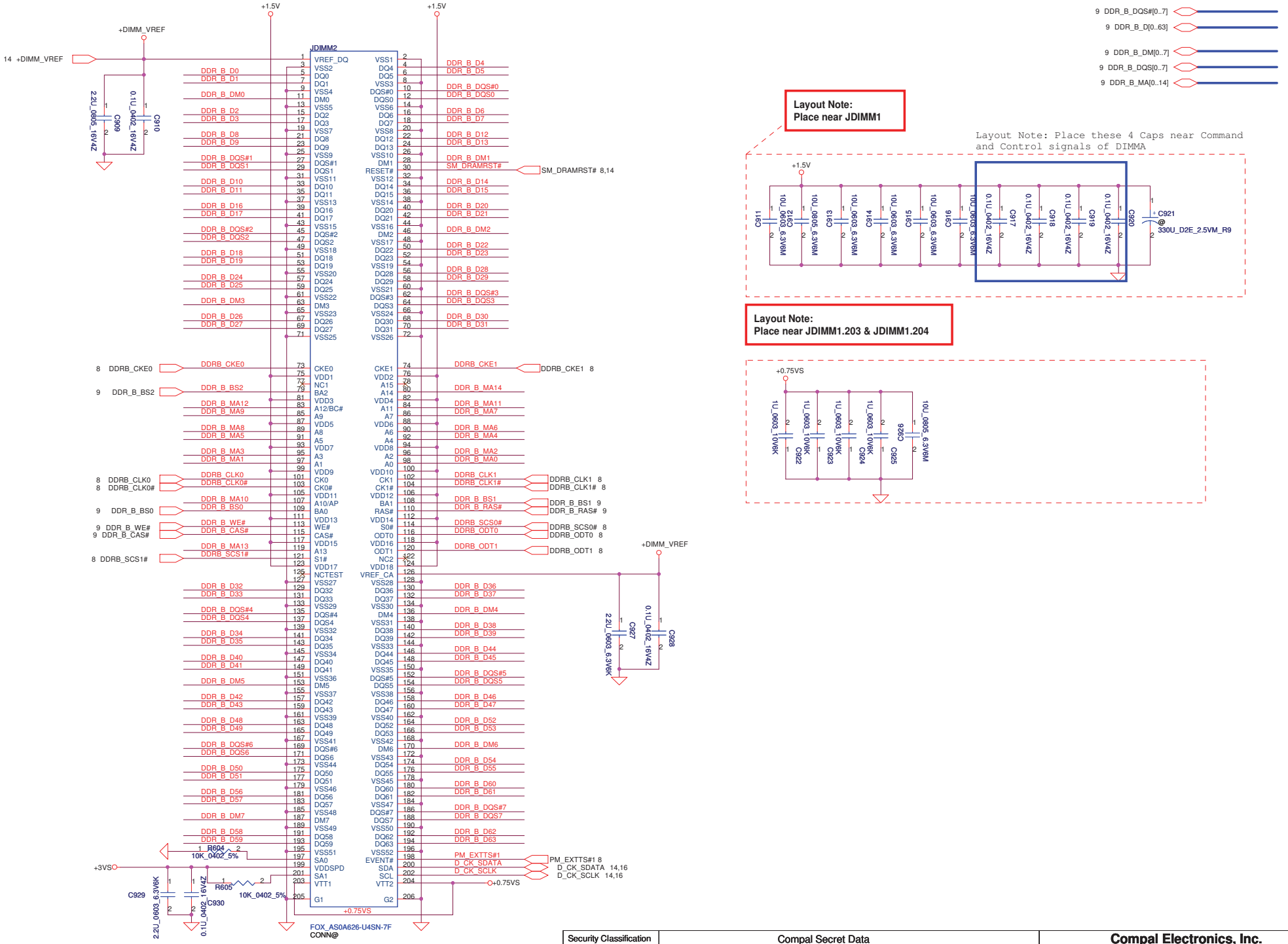
Compal Electronics, Inc.	
Title	DDRIII-SODIMM0
Size B	Document Number PEW72/82 M/B LA-6631P Schematic
Rev	1.0
Date: Thursday, July 08, 2010	Sheet 14 of 44



Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

+3VS CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)

R306 10K_0402_5% CLK_PCI2

mount to Enable ITP_CLK

R312 @ 10K_0402_5%

R310 10K_0402_5% CLK_PCI5

CLK_PCI5=0, Pin63,64 is SRC_CLK
CLK_PCI5=1, Pin63,64 is ITP_CLK

R308 10K_0402_5% CLK_PCI4

CLK_PCI4=0, Pin28, 29 is SRC_CLK
Pin24, 25 is DOT96_CLK

R292 @ 10K_0402_5% CK_PWRGD

C345 @ 10P_0402_50V8J CLK_PCI_LPC
C346 @ 10P_0402_50V8J CLK_PCI_ICH
For EMI 10/9

+3VS R301 10K_0402_5% @ CK505_PWRGD
Q28 2N7002-7-F_SOT23-3 @ CLK_ENABLE# 42

+1.05VS
R327 @56_0402_5%
R326 2.2K_0402_5% CLKSEL0
R313 1K_0402_5% MCH_CLKSEL0 8
R328 @1K_0402_5% CPU_BSEL0 5

+1.05VS
R384 @1K_0402_5%
R383 1K_0402_5% CLKSEL1 MCH_CLKSEL1 8
R379 @ 0_0402_5%
R380 0_0402_5% CPU_BSEL1 5

+1.05VS
R389 @1K_0402_5%
R388 10K_0402_5% CLKSEL2
R392 1K_0402_5% MCH_CLKSEL2 8
R390 @ 0_0402_5% CPU_BSEL2 5

+1.05VS +CLK_VDDSRC
L15 FBMA-L11-201209-221LMA30T_0805
C347 10U_0805_10V6K
C358 10U_0805_10V6K
C371 0.1U_0402_16V4Z
C387 0.1U_0402_16V4Z
C370 0.1U_0402_16V4Z
C380 0.1U_0402_16V4Z
C381 0.1U_0402_16V4Z

+3VS +CLK_VDD
L16 FBMA-L11-201209-221LMA30T_0805
C390 10U_0805_10V6K
C384 10U_0805_10V6K
C356 0.1U_0402_16V4Z
C357 0.1U_0402_16V4Z
C355 0.1U_0402_16V4Z

+3VS +CLK_VDD1
L32 FBMA-L11-201209-221LMA30T_0805
+1.5VS L33 @ FBMA-L11-201209-221LMA30T_0805
For Low Power CLK GEN
C388 10U_0805_10V6K
C1211 0.1U_0402_16V4Z
C372 0.1U_0402_16V4Z
C385 0.1U_0402_16V4Z

+CLK_VDDSRC R400 0_0402_5% +CLK_VDDSRC_R
+CLK_VDD1 R401 @ 0_0402_5%
For Low Power CLK GEN
C386 0.1U_0402_16V4Z

22 H_STP_CPU# H_STP_CPU#
22 H_STP_PCI# H_STP_PCI#

29 CLK_PCI_LPC CLK_PCI_LPC R307 33_0402_5% CLK_PCI3
20 CLK_PCI_ICH CLK_PCI_ICH R309 33_0402_5% CLK_PCI5

22 CK_PWRGD 8,22,42 VGATE
0_0402_5% R303 CK505_PWRGD
0_0402_5% @ R302

C354 27P_0402_50V8J CLK_XTALIN
C353 27P_0402_50V8J CLK_XTALOUT
Y2 14.31818MHz_20P_FSX8L14.318181M20FDB

22 CLK_ICH_48M CLK_ICH_48M R325 22_0402_5% CLKSEL0
25 CLK_SD_48M CLK_SD_48M R311 22_0402_5% CLKSEL1

22 CLK_ICH_14M CLK_ICH_14M R304 33_0402_5% CLKSEL2

+3VS R305 4.7K_0402_5% +3VS
22,27 ICH_SMBDATA D_CK_SDATA
Q22 2N7002-7-F_SOT23-3

+3VS R1430 4.7K_0402_5% +3VS
22,27 ICH_SMBCLK D_CK_SCLK
Q23 2N7002-7-F_SOT23-3

U16

+CLK_VDD	6	VDDREF	
+CLK_VDD1	19	VDD48	
	72	VDDCPU	
	12	VDDPCI	
	27	VDDPLL3	
	55	VDDSRC	
+CLK_VDDSRC	52	VDDSRC_IO	
	38	VDDSRC_IO	
	62	VDDSRC_IO	
	31	VDDPLL3_IO	
	66	VDDCPU_IO	
	23	VDD96_IO	
	53	CPU_STOP#	
	54	PCI_STOP#	
	13	PCI1	
CLK_PCI2	14	PCI2/TME	
CLK_PCI3	15	PCI3	
CLK_PCI4	16	PCI4/27_SELECT	
CLK_PCI5	17	PCI_F5/ITP_EN	
CK505_PWRGD	1	CK_PWRGD/PD#	
CLK_XTALIN	5	X1	
CLK_XTALOUT	4	X2	
	11	NC	
CLKSEL0	20	USB_48MHz/FSLA	
CLKSEL1	2	FSLB/TEST_MODE	
CLKSEL2	7	FSLC/TEST_SEL/REF0	
	8	REF1	
	69	GNDCPU	
	3	GNDREF	
	18	GNDPCI	
	22	GND48	
	30	GND	
	26	GND	
	34	GNDSRC	
	59	GNDSRC	
	42	GNDSRC	
	73	GND_THERMAL_PAD	

ICS9LPRS387, PN:SA000020H10
SLG8SP556V, PN:SA000020K00
RTM875N, PN:SA000020N00
LOW Power
RTM890N, PN:SA00003H730
ICS9LVRS387, PN:SA00003H610
ICS9LPRS387BKLFT_MLF72_10x10

SDATA	9	D_CK_SDATA	D_CK_SDATA 14,15
SCLK	10	D_CK_SCLK	D_CK_SCLK 14,15
CPUT0_LPR_F	71	CLK_CPU_BCLK	CLK_CPU_BCLK 4
CPUC0_LPR_F	70	CLK_CPU_BCLK#	CLK_CPU_BCLK# 4
CPUT1_LPR_F	68	CLK_MCH_BCLK	CLK_MCH_BCLK 7
CPUC1_LPR_F	67	CLK_MCH_BCLK#	CLK_MCH_BCLK# 7
SRCT0_LPR/DOTT_96_LPR	24	CLK_DREF_96M	CLK_DREF_96M 8
SRCC0_LPR/DOTC_96_LPR	25	CLK_DREF_96M#	CLK_DREF_96M# 8
27MHz_NonSS/SRCT1_LPR/SE1	28	CLK_DREF_SSC	CLK_DREF_SSC 8
27MHz_SS/SRCC1_LPR/SE2	29	CLK_DREF_SSC#	CLK_DREF_SSC# 8
SRCT2_LPR/SATAT_LPR	32	CLK_PCIE_SATA	CLK_PCIE_SATA 21
SRCC2_LPR/SATAC_LPR	33	CLK_PCIE_SATA#	CLK_PCIE_SATA# 21
SRCT3_LPR	35	CLK_PCIE_ICH	CLK_PCIE_ICH 22
SRCC3_LPR	36	CLK_PCIE_ICH#	CLK_PCIE_ICH# 22
SRCT4_LPR	39		
SRCC4_LPR	40		
SRCT6_LPR	57	CLK_MCH_3GPLL	CLK_MCH_3GPLL 8
SRCC6_LPR	56	CLK_MCH_3GPLL#	CLK_MCH_3GPLL# 8
SRCT7_LPR	61		
SRCC7_LPR	60		
CPUT2_ITP_LPR/SRCT8_LPR	64		
CPUC2_ITP_LPR/SRCC8_LPR	63		
SRCT9_LPR	44	CLK_PCIE_MINI2	CLK_PCIE_MINI2 27
SRCC9_LPR	45	CLK_PCIE_MINI2#	CLK_PCIE_MINI2# 27
SRCT10_LPR	50		
SRCC10_LPR	51		
SRCT11_LPR	48	CLK_PCIE_LAN	CLK_PCIE_LAN 26
SRCC11_LPR	47	CLK_PCIE_LAN#	CLK_PCIE_LAN# 26
CR#3	37		
CR#4	41		
CR#6	58		MCH_CLKREQ# 8 (Pull High to +3VS at GMCH side)
CR#7	65		
CR#9	43	R336 10K_0402_5% +3VS	MINI2_CLKREQ# 27
CR10#	49		
CR#11	46	R364 10K_0402_5% +3VS	LAN_CLKREQ# 26
CR#A	21		SATA_CLKREQ# 22 (Pull High to +3VS at ICH side)

VGA: disable this pair by BIOS

VGA: disable this pair by BIOS

UMA: disable this pair by BIOS

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

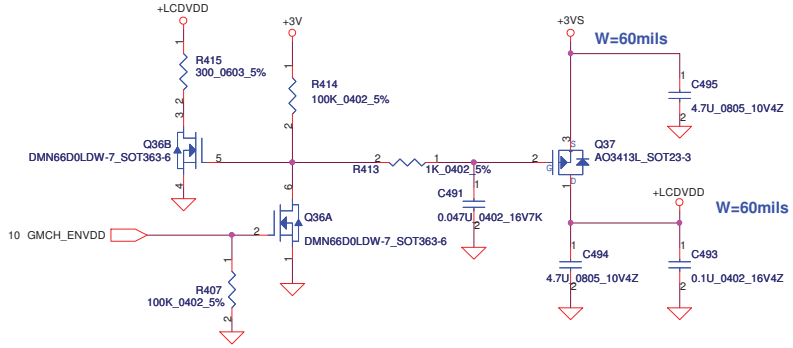
Compal Electronics, Inc.

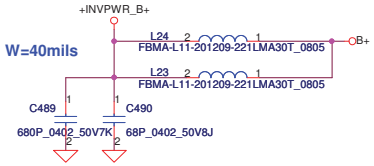
Title: Clock Generator (CK505)

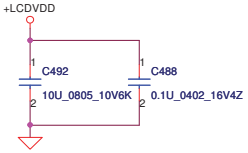
Size: Custom | Document Number: PEW72/82 M/B LA-6631P Schematic | Rev: 1.0

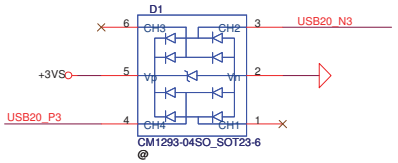
Date: Thursday, July 08, 2010 | Sheet 16 of 44

LCD POWER CIRCUIT

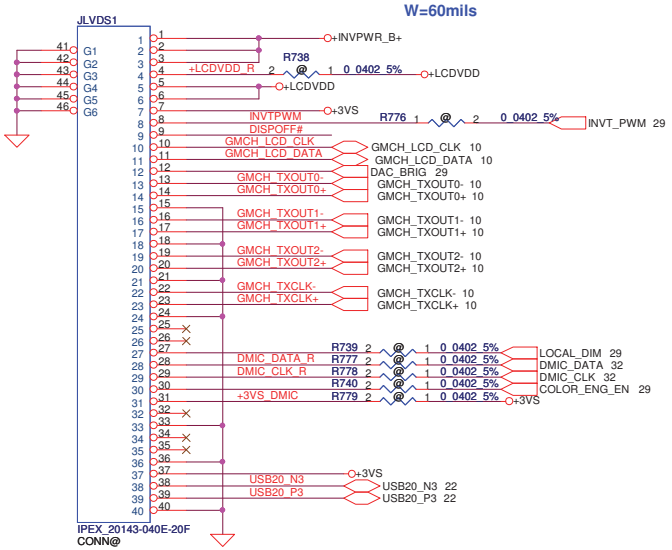


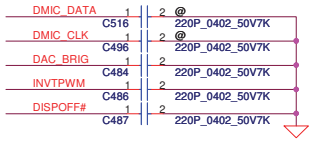


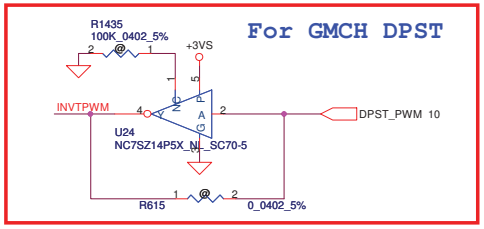




LCD/PANEL BD. Conn.



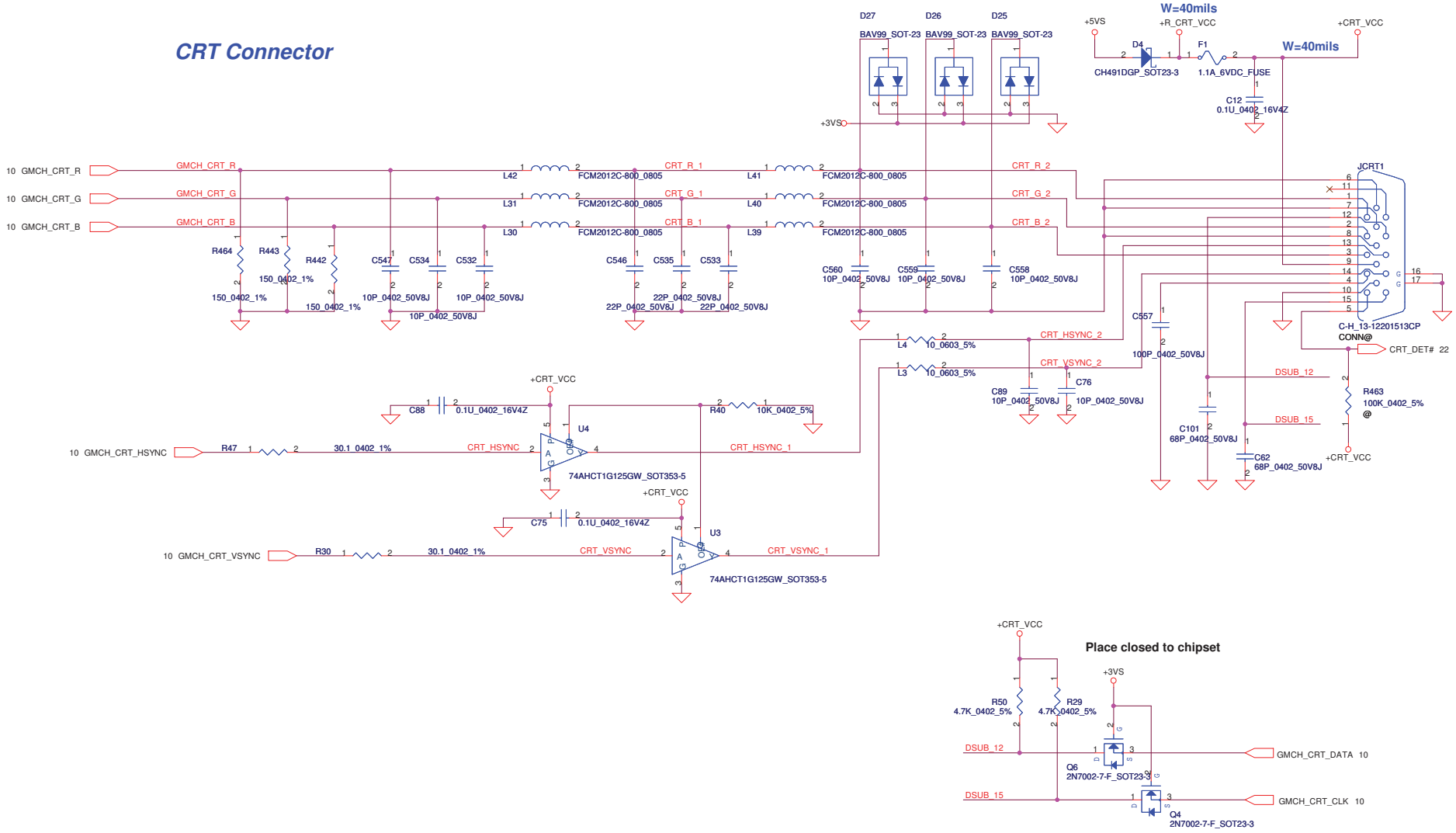




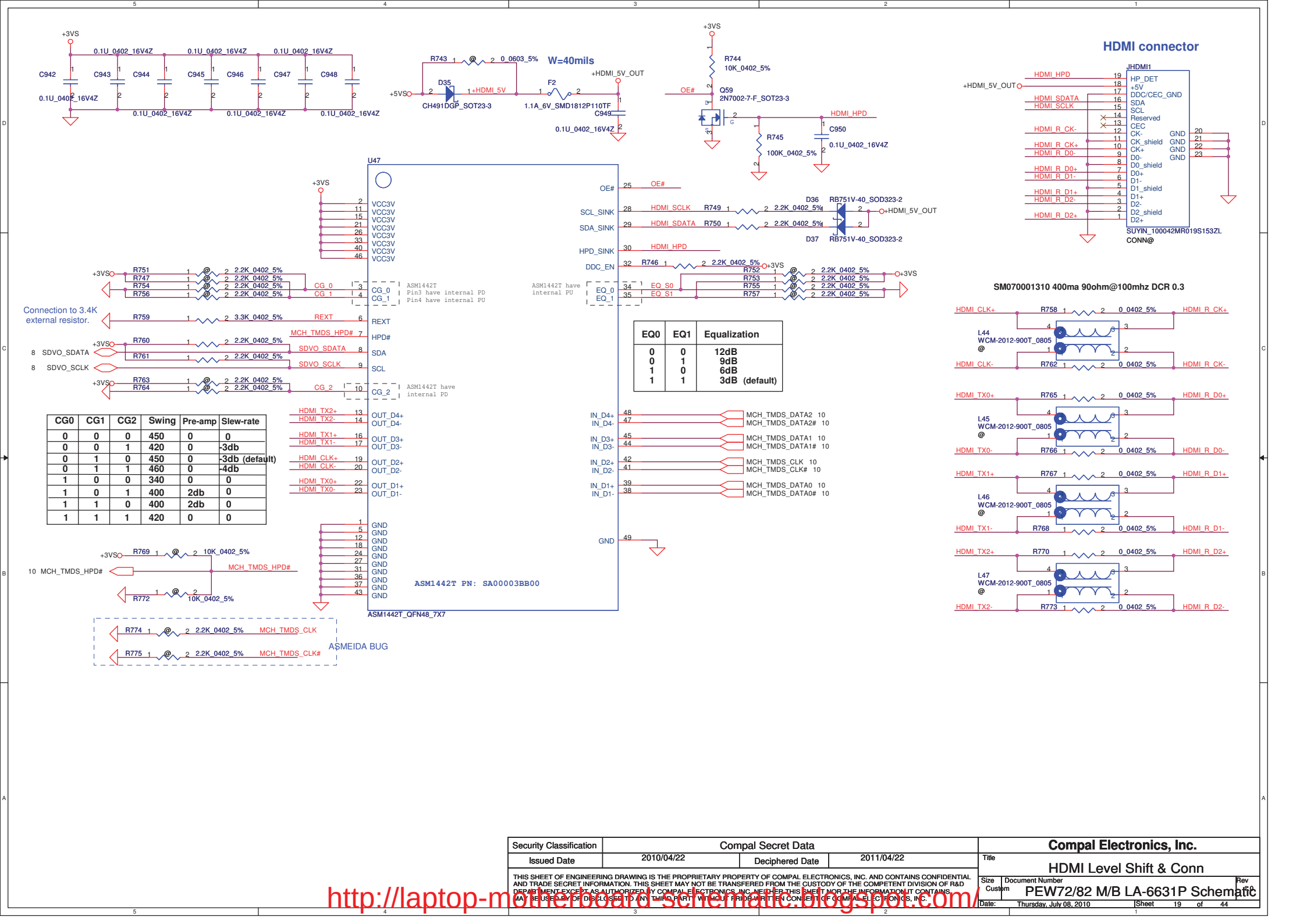
Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.	
Title	LVDS Connector
Size	Custom
Document Number	PEW72/82 M/B LA-6631P Schematic
Rev	1.0
Date:	Thursday, July 08, 2010
Sheet	17 of 44

CRT Connector



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: CRT Connector
Size: B	Document Number: PEW72/82 M/B LA-6631P Schematic		Rev: 1.0
Date: Thursday, July 08, 2010	Sheet 18 of 44		



EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

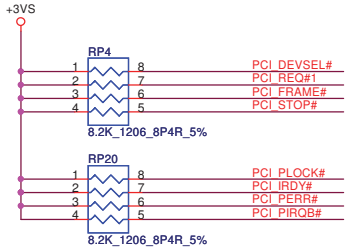
Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

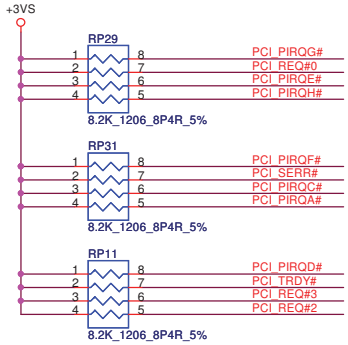
Compal Electronics, Inc.

Title: HDMI Level Shift & Conn

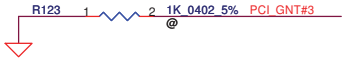
Size: Custom | Document Number: PEW72/82 M/B LA-6631P Schematic | Rev: 0.4

Date: Thursday, July 08, 2010 | Sheet 19 of 44

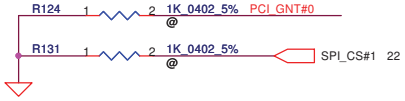




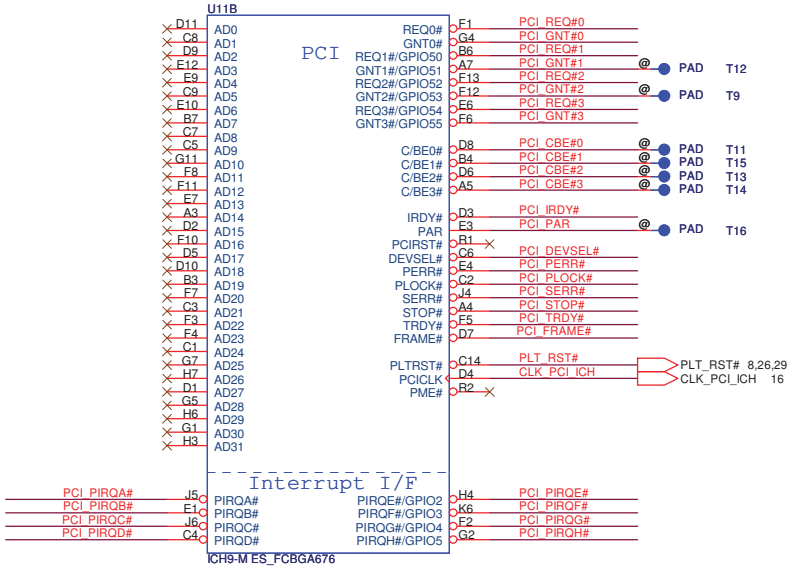
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

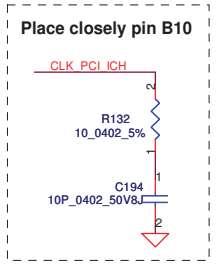


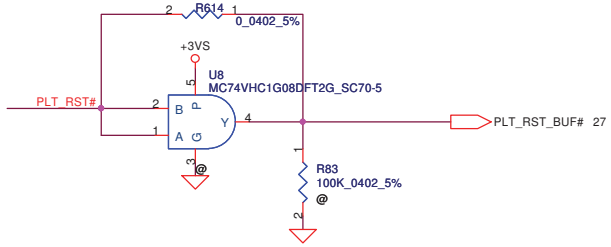
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*



DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)

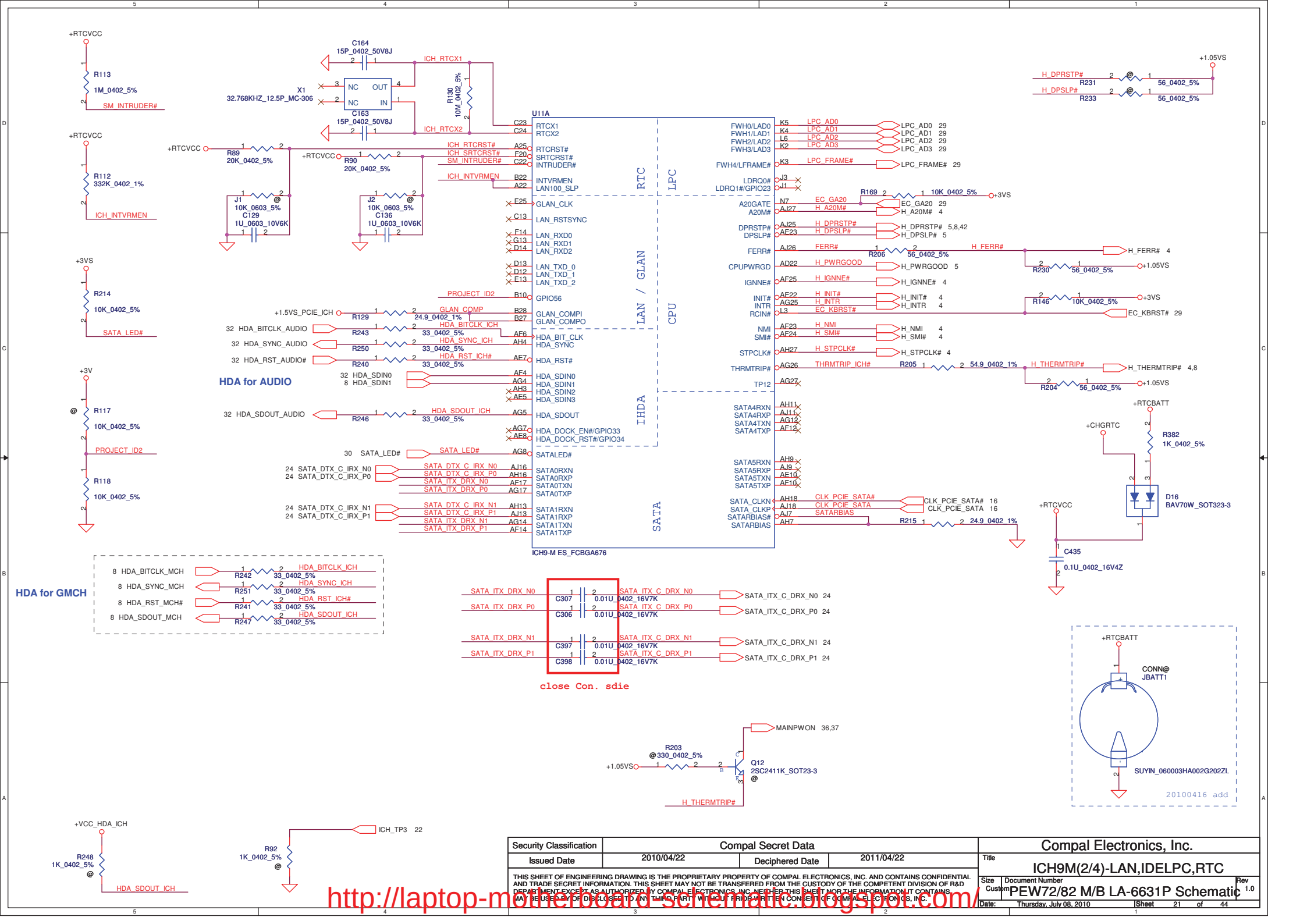






Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.			
Title	ICH9M(1/4)-PCI		
Size	Document Number		Rev
	PEW72/82 M/B LA-6631P Schematic		1.0
Date: Thursday, July 08, 2010		Sheet 20 of 44	



Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

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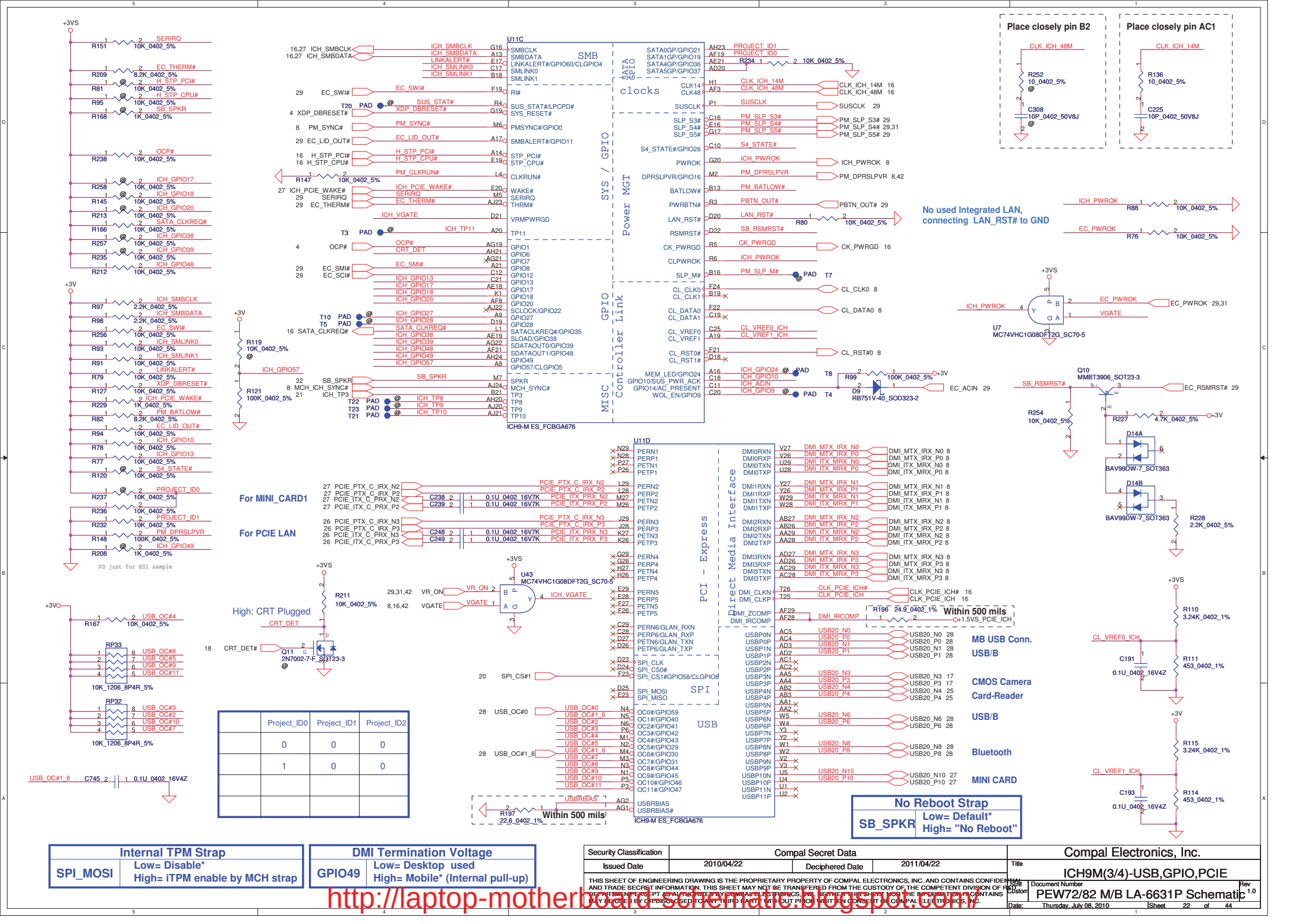
Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: PEW72/82 M/B LA-6631P Schematic | Rev: 1.0

Date: Thursday, July 08, 2010 | Sheet 21 of 44



	Project_ID0	Project_ID1	Project_ID2
	0	0	0
	1	0	0

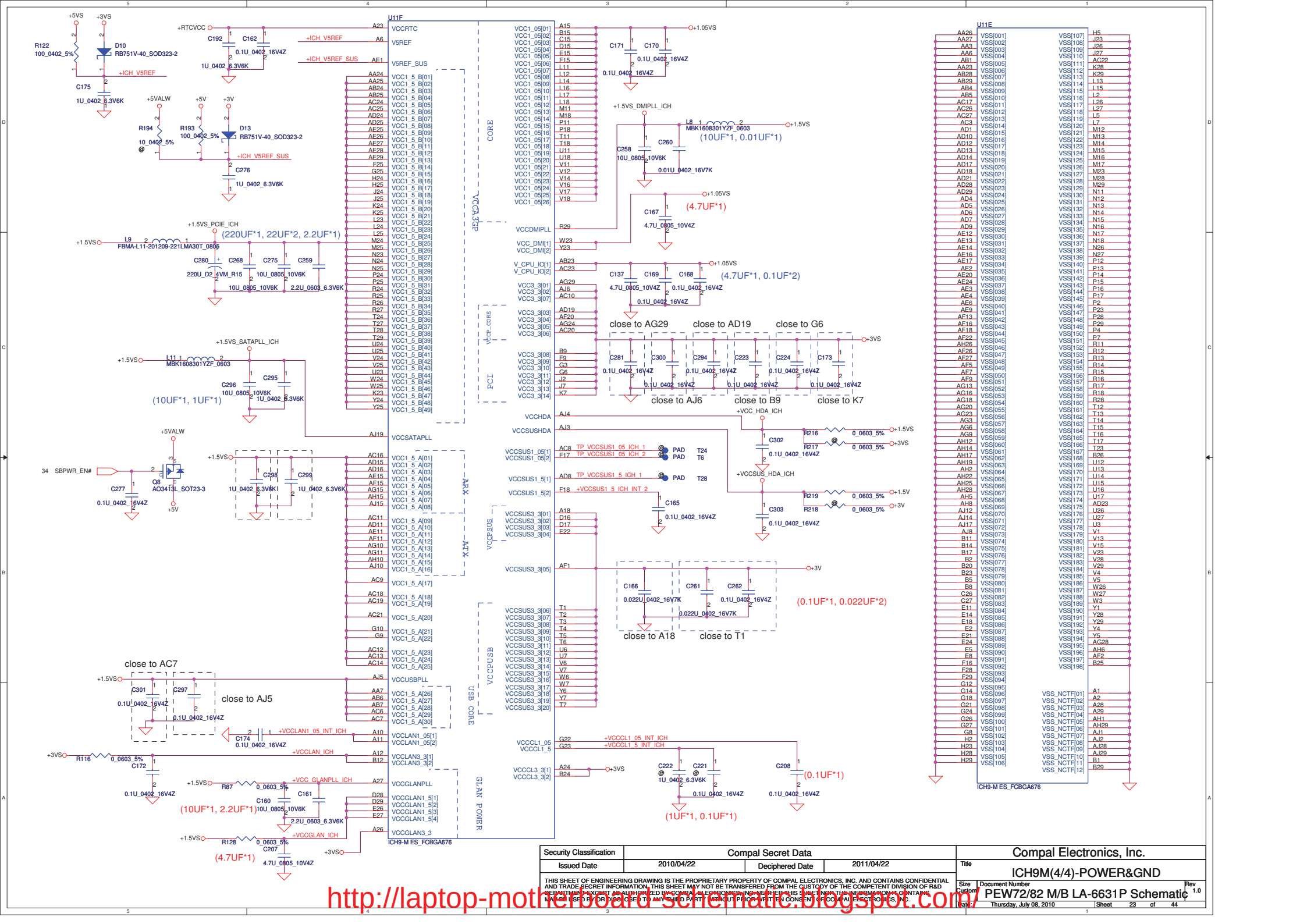
Internal TPM Strap	
SPI_MOSI	Low= Disable* High= iTPM enable by MCH strap

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

No Reboot Strap	
SB_SPKR	Low= Default* High= "No Reboot"

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.	
Title	ICH9M(3/4)-USB,GPIO,PCIE
Size: Custom	Document Number: PEW72/82 M/B LA-6631P Schematic
Rev	1.0
Date: Thursday, July 08, 2010	Sheet 22 of 44

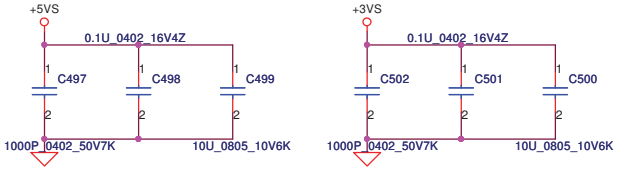


Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

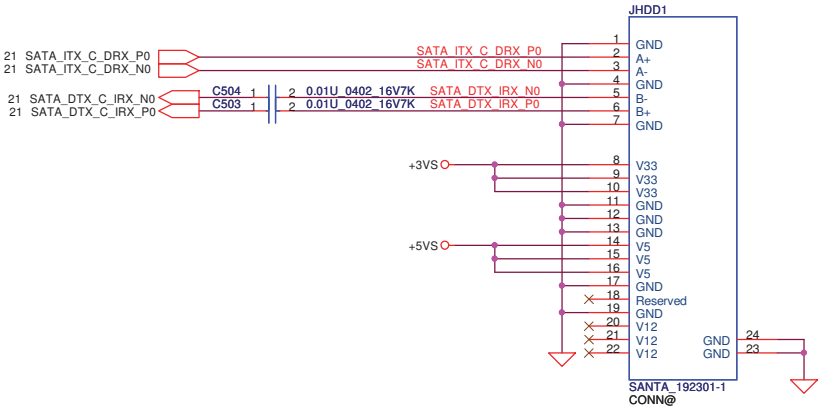
Compal Electronics, Inc.

Title: ICH9M(4/4)-POWER&GND

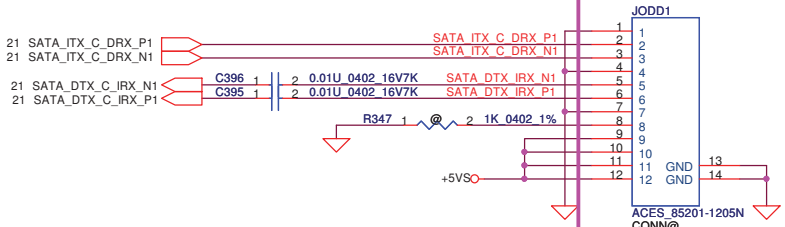
Size	Document Number	Rev
Custom	PEW72/82 M/B LA-6631P Schematic	1.0
Date: Thursday, July 08, 2010	Sheet 23 of 44	



SATA HDD Conn.



SATA ODD Conn. LS-6583



Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: PEW72/82 M/B LA-6631P Schematic | Rev: 1.0

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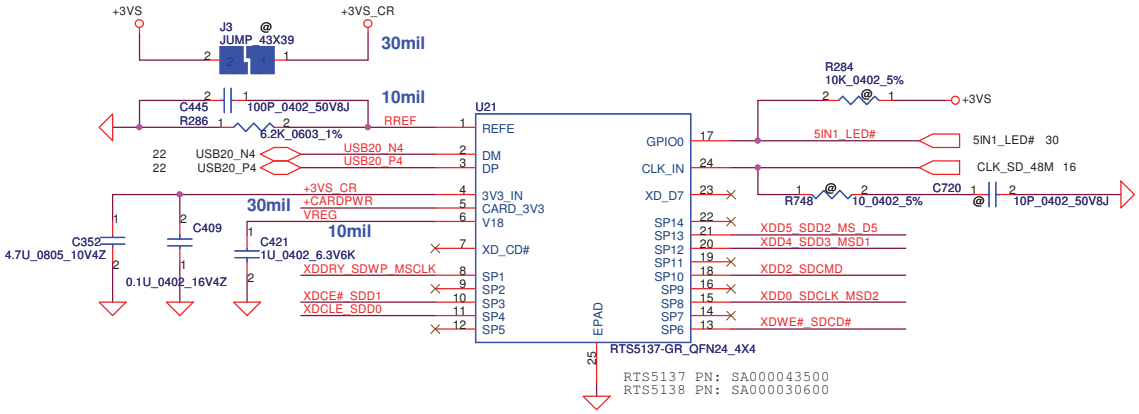
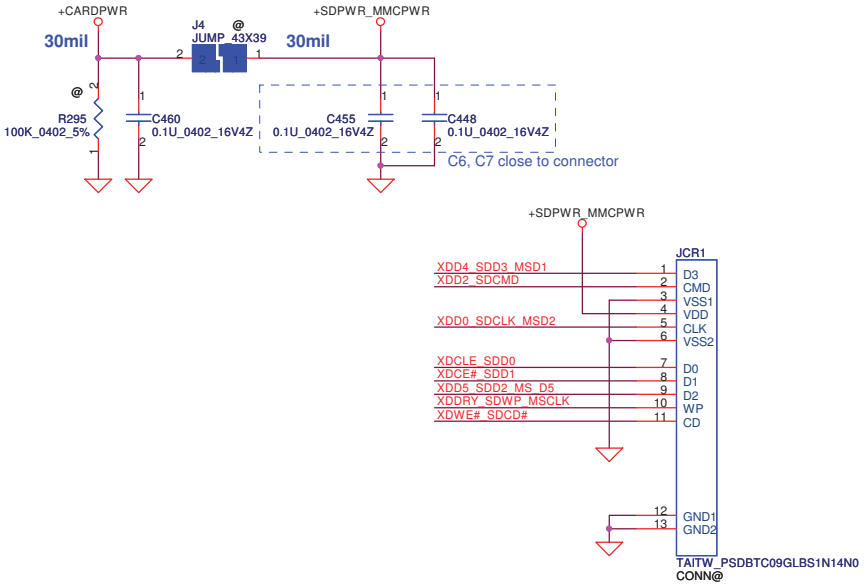
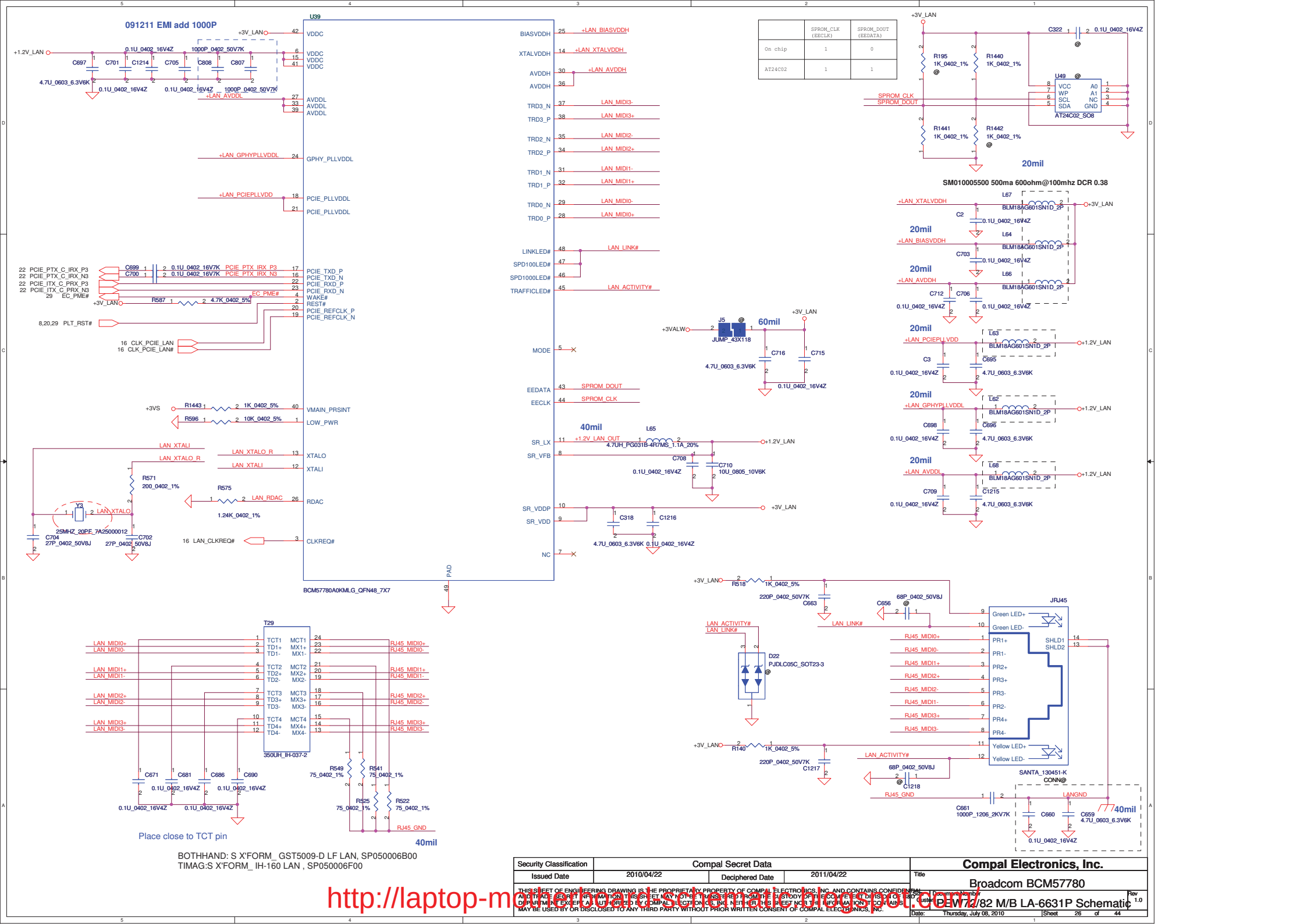
Card Reader RTS5138 / RTS5137
(only SD+MMC function)



Card Reader Connector



Compal Electronics, Inc.			
Title: CardReader RTS5137			
Size: Custom	Document Number: PEW72/82 M/B LA-6631P Schematic		Rev: 1.0
Date: Thursday, July 08, 2010	Sheet 25 of 44		



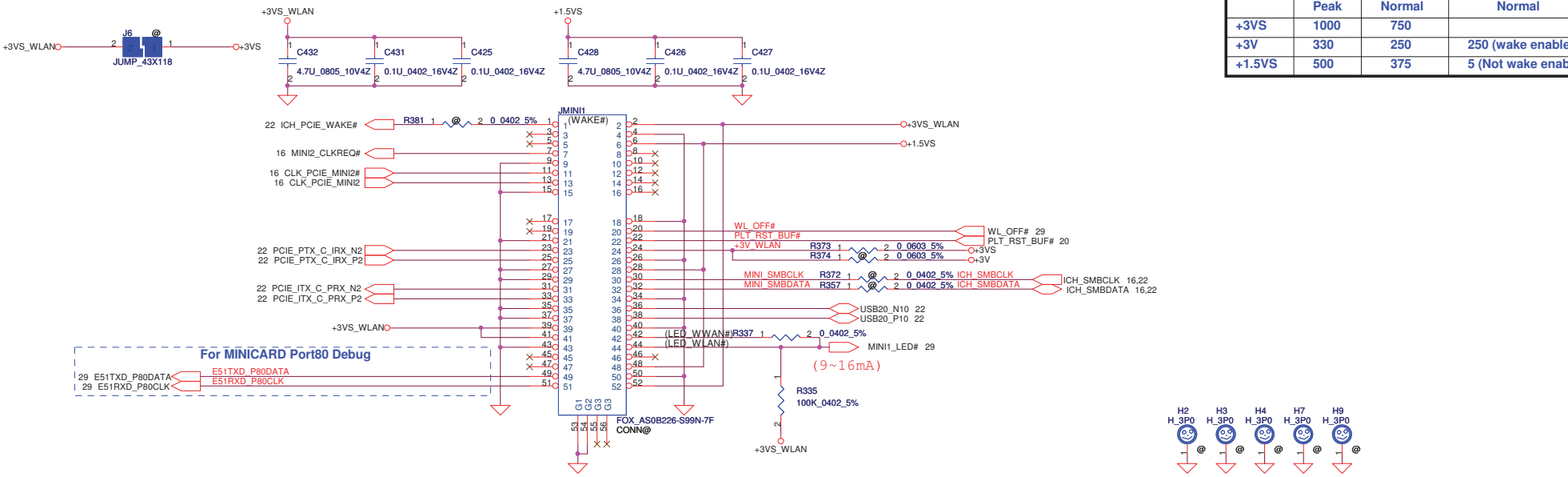
BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

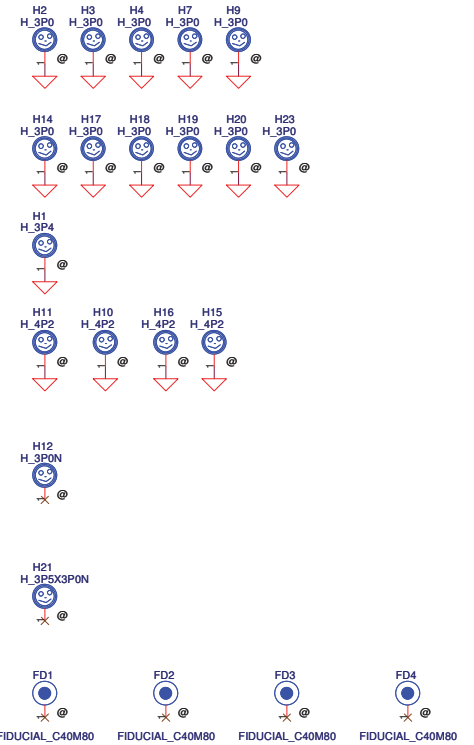
Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.		
Title: Broadcom BCM57780		
Size: C	Document Number: DEW72/82 M/B LA-6631P Schematic	Rev: 1.0
Date: Thursday, July 08, 2010	Sheet 26 of 44	

For Wireless LAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: MINI CARD (WLAN & TV-Tuner)
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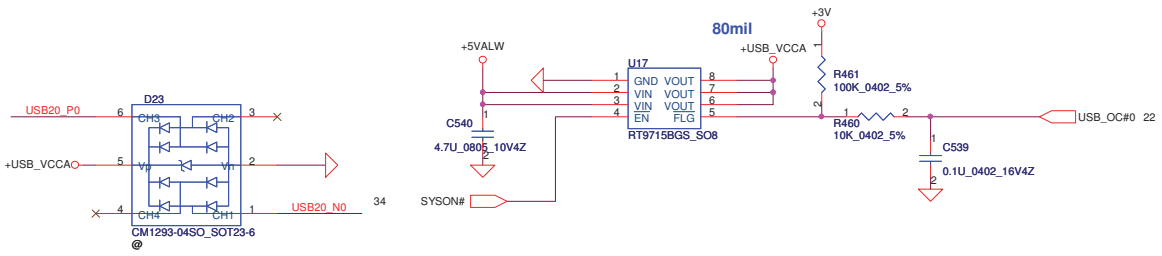
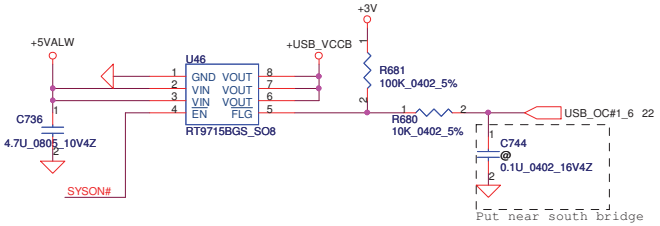
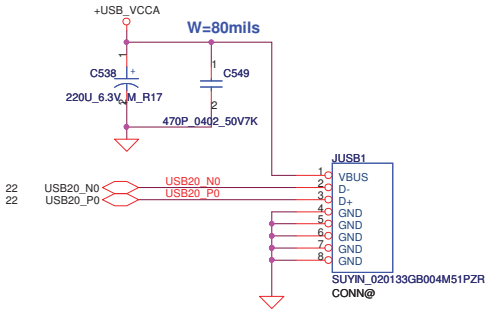
			Date: Thursday, July 08, 2010; Sheet 27 of 44



USB Conn.

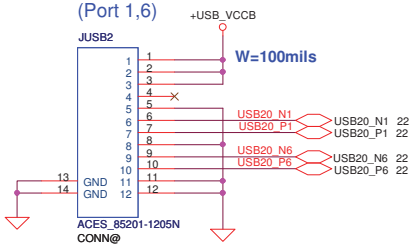
(Port 0)



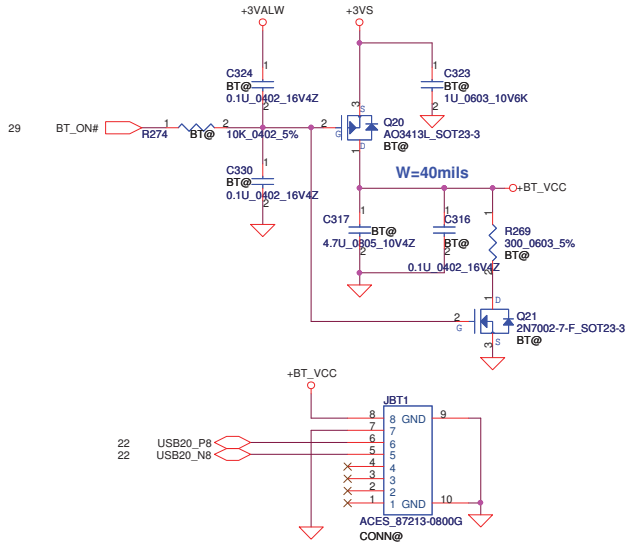


USB/B Conn. LS-6581

(Port 1,6)



Bluetooth Conn.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: BT & USB Connector

Size: B	Document Number: PEW72/82 M/B LA-6631P Schematic		Rev: 1.0
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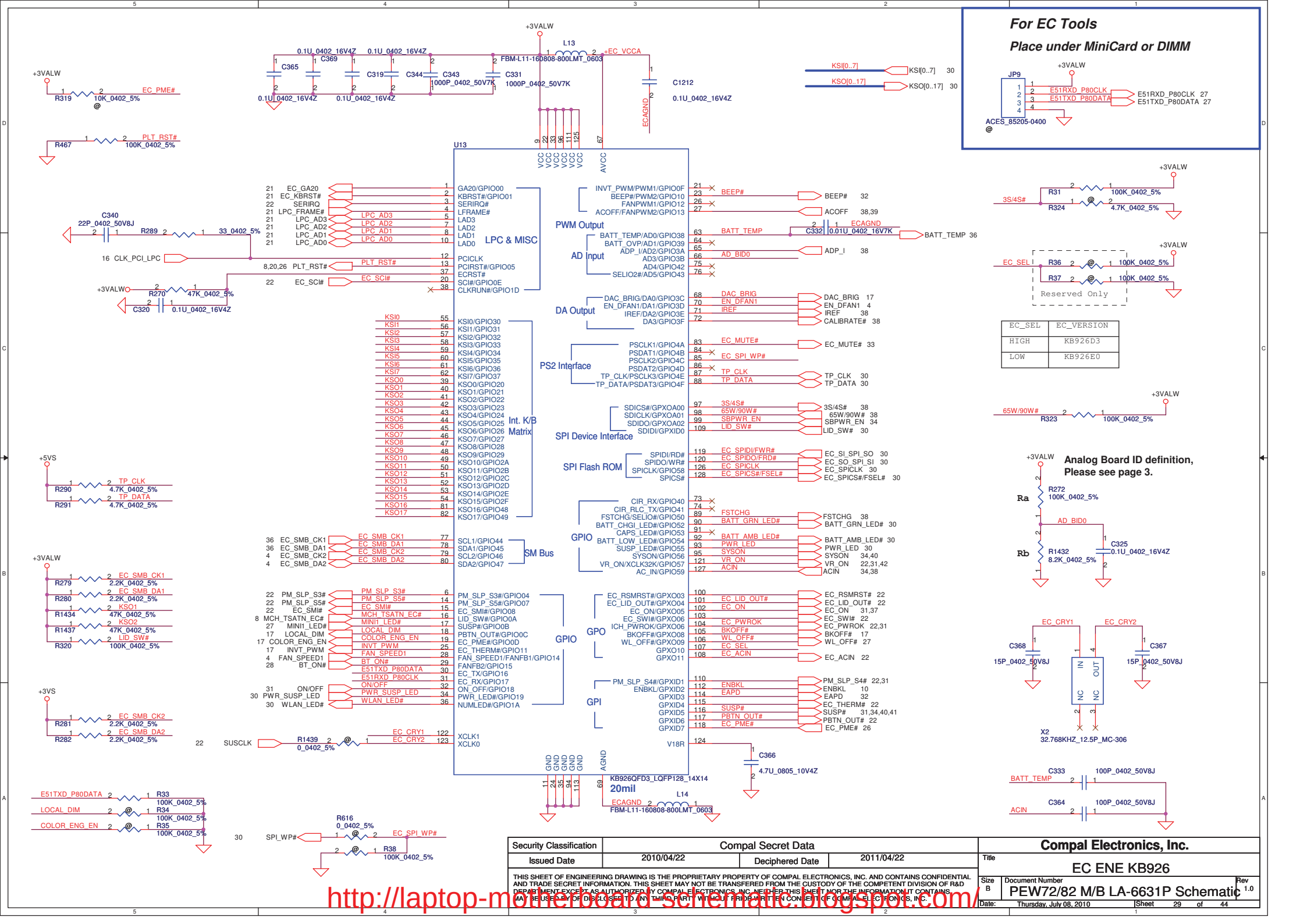
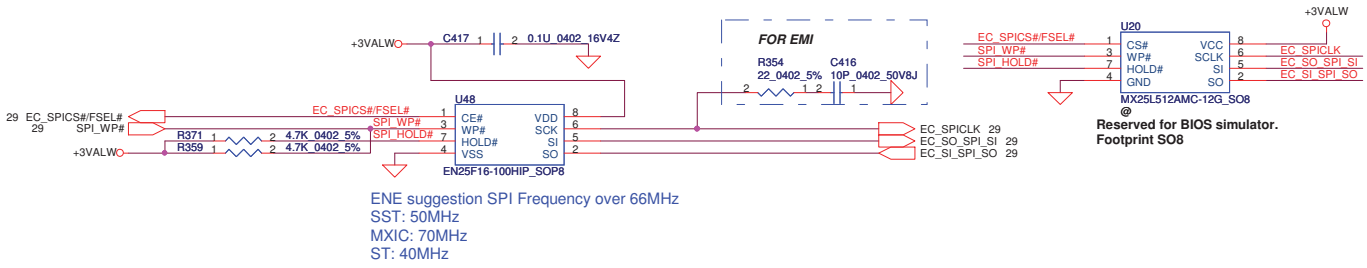
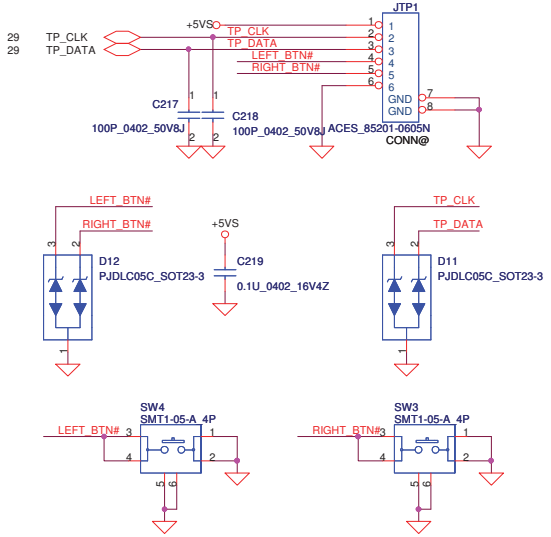


EC_SEL	EC_VERSION
HIGH	KB926D3
LOW	KB926E0

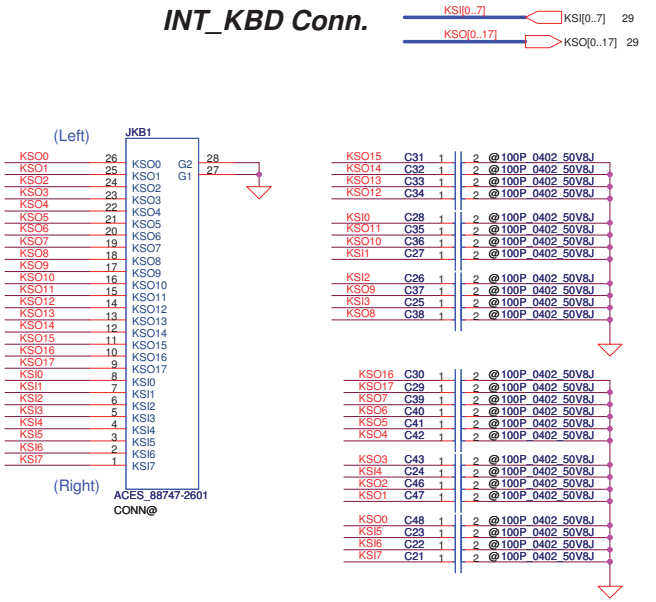


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

To TP/B Conn.

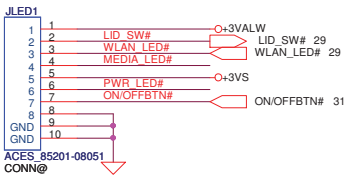


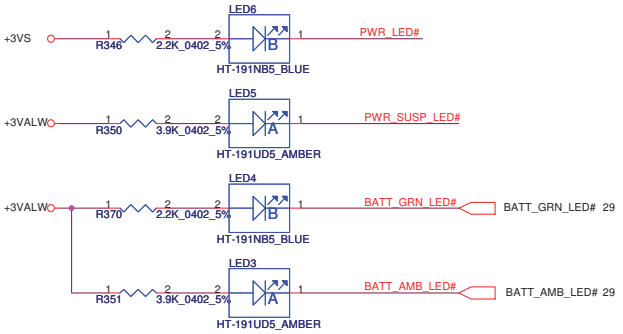
INT_KBD Conn.

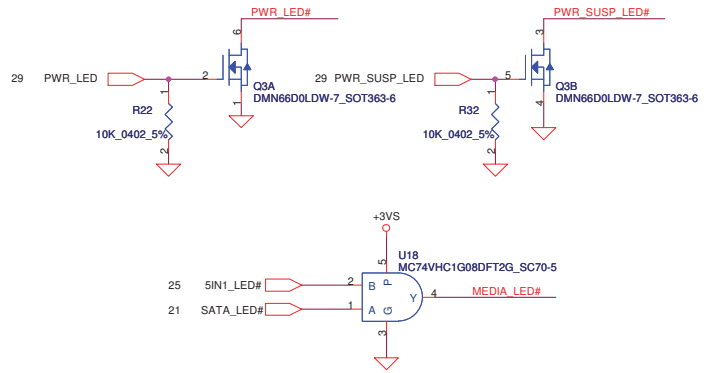


LS-6582

Power/B







Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.	
Title	BIOS, I/O Port & K/B Connector
Size	B
Document Number	PEW72/82 M/B LA-6631P Schematic
Rev	1.0
Date:	Thursday, July 08, 2010
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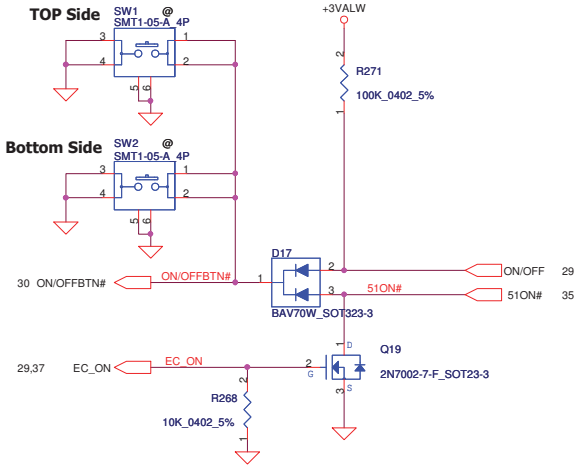
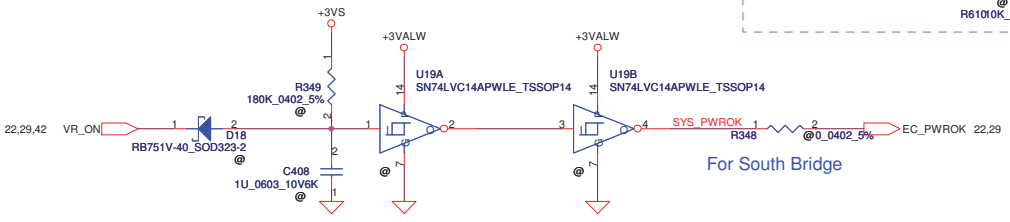
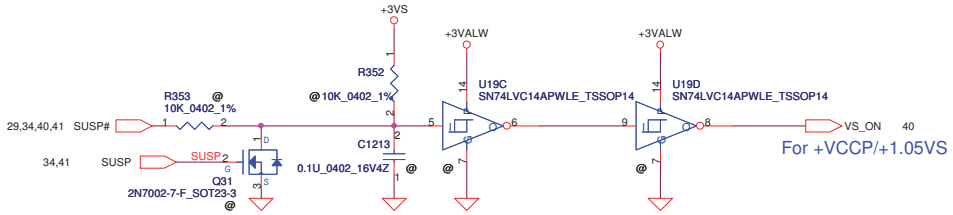
Power Button

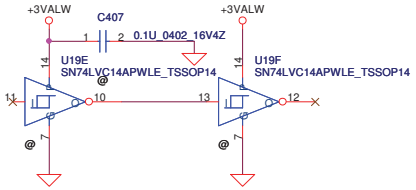
ON/OFF switch



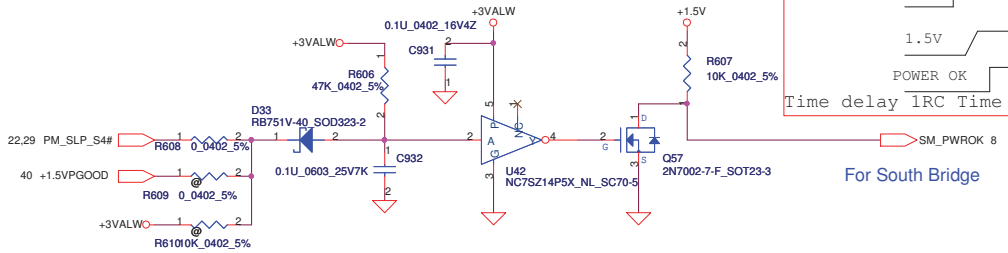
Power ON Circuit







DDR3

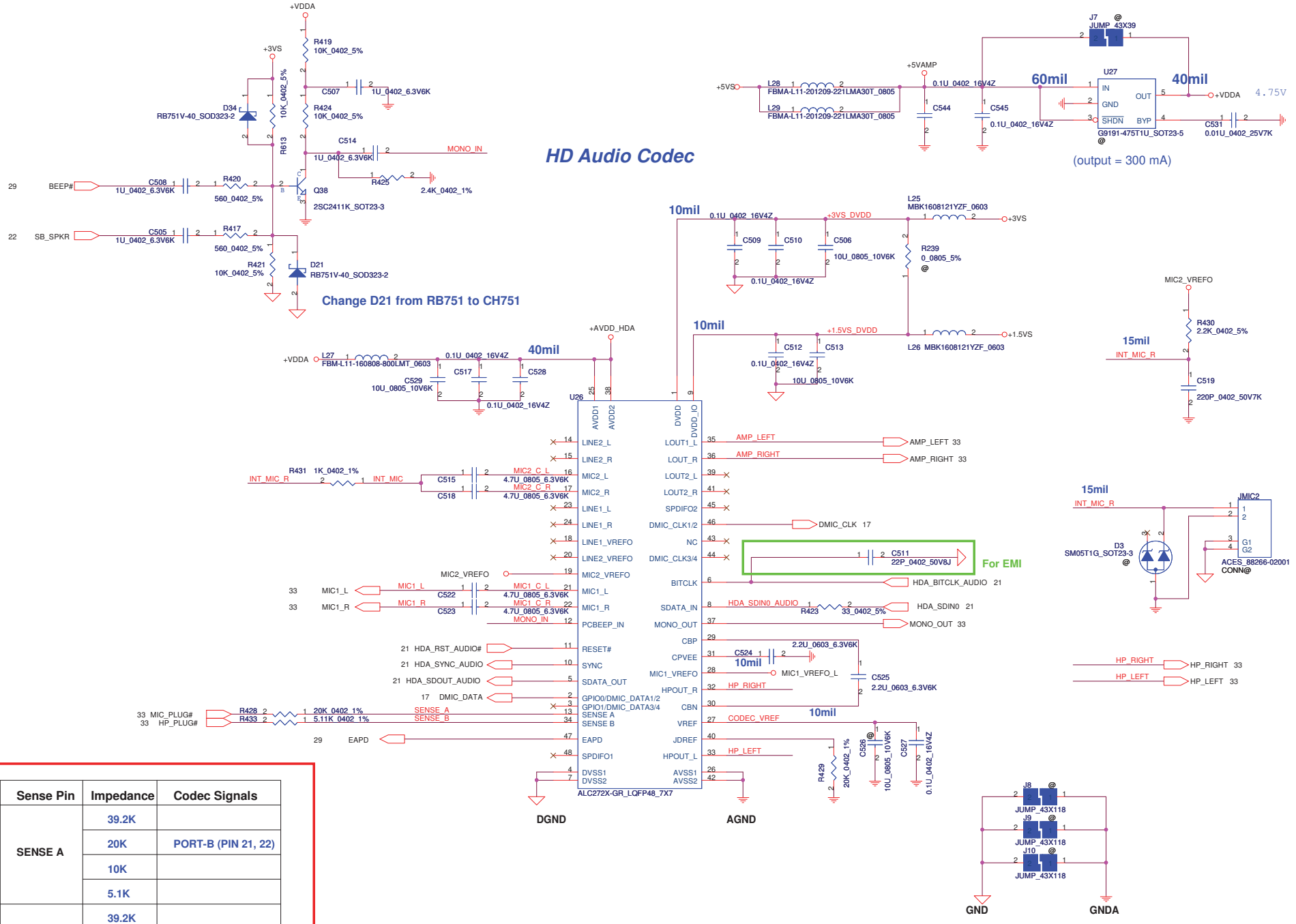


Compal Electronics, Inc.

Title: Power OK, Reset

Size: B | Document Number: PEW72/82 M/B LA-6631P Schematic | Rev: 1.0

Date: Thursday, July 08, 2010 | Sheet 31 of 44



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	
	20K	PORT-B (PIN 21, 22)
	10K	
	5.1K	
SENSE B	39.2K	
	20K	
	10K	
	5.1K	PORT-H (PIN 32,33)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: HD Audio Codec ALC272X
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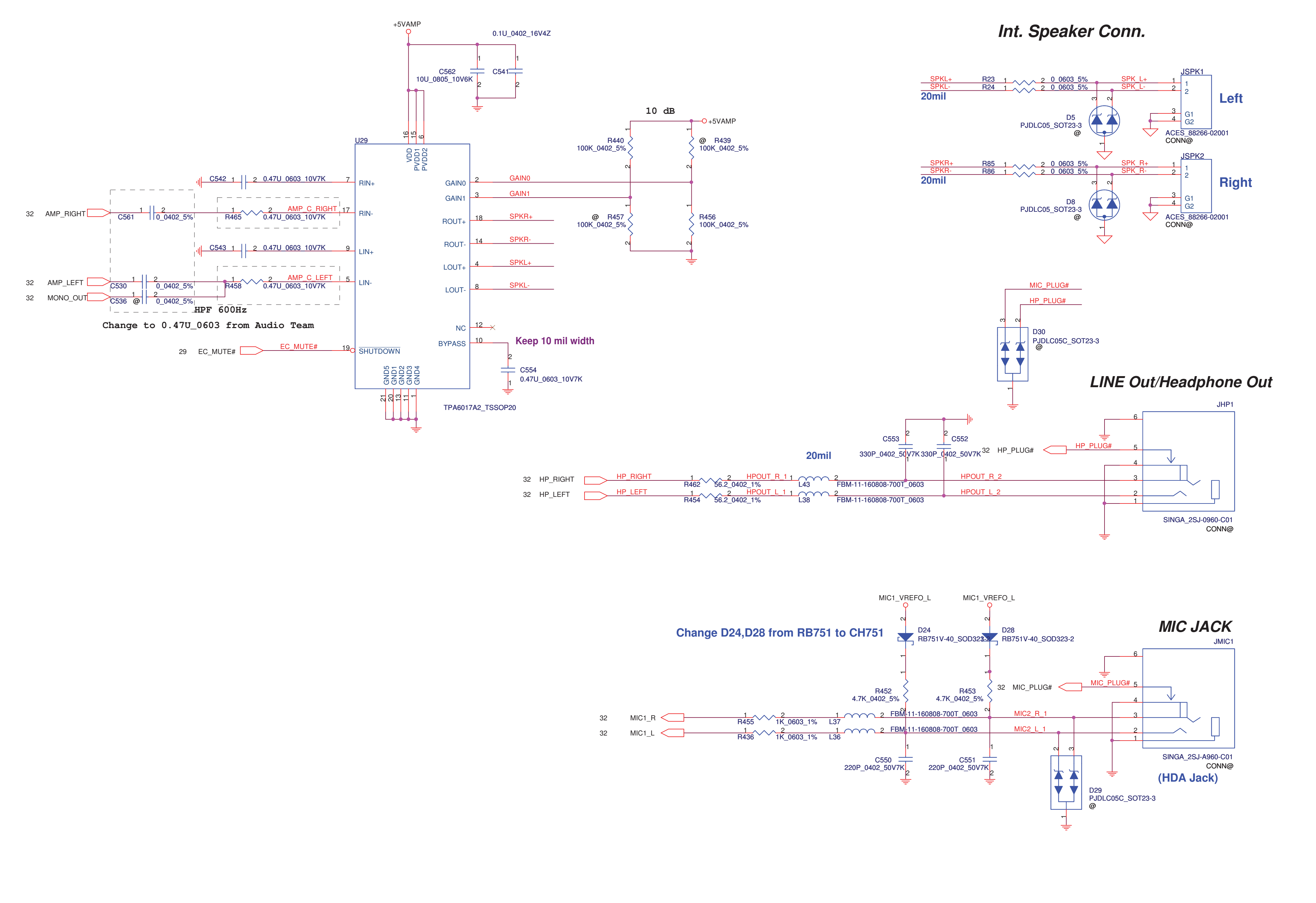
			Date: Thursday, July 08, 2010; Sheet 32 of 44



Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

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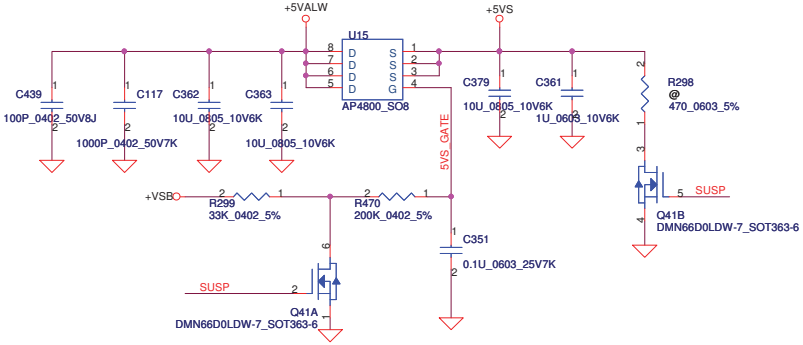
Compal Electronics, Inc.

Title: Amplifier & Audio Jack

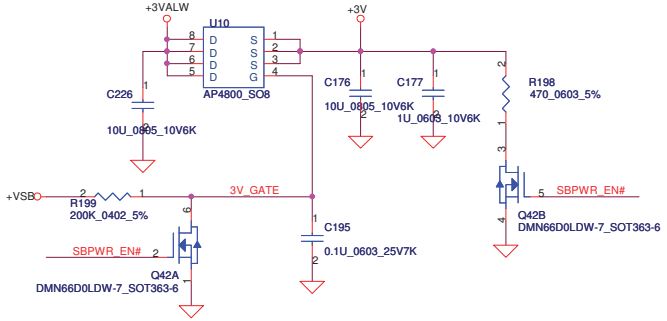
Size: B | Document Number: PEW72/82 M/B LA-6631P Schematic | Rev: 1.0

Date: Friday, July 09, 2010 | Sheet 33 of 44

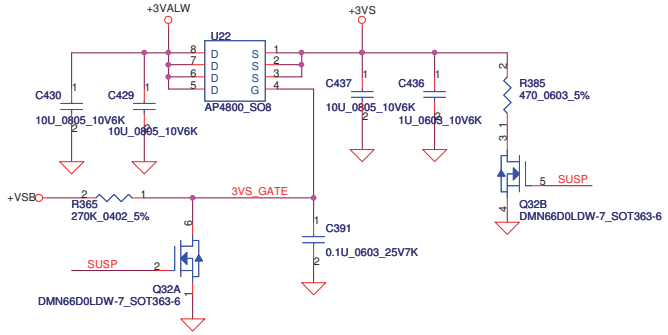
+5VALW TO +5VS



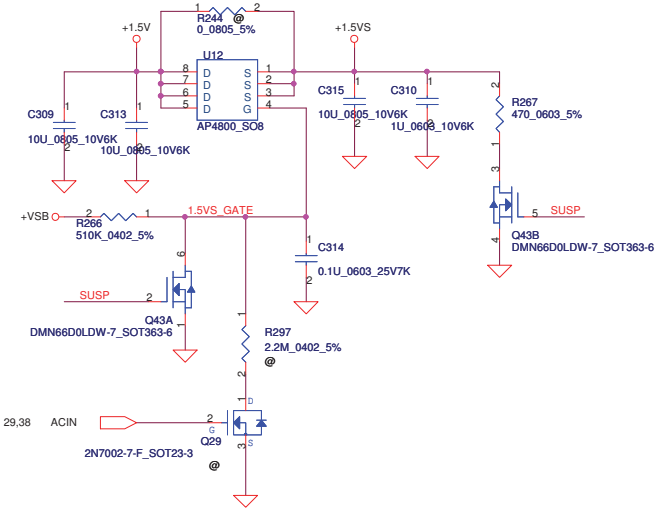
+3VALW TO +3V_SB(ICH8M AUX Power)

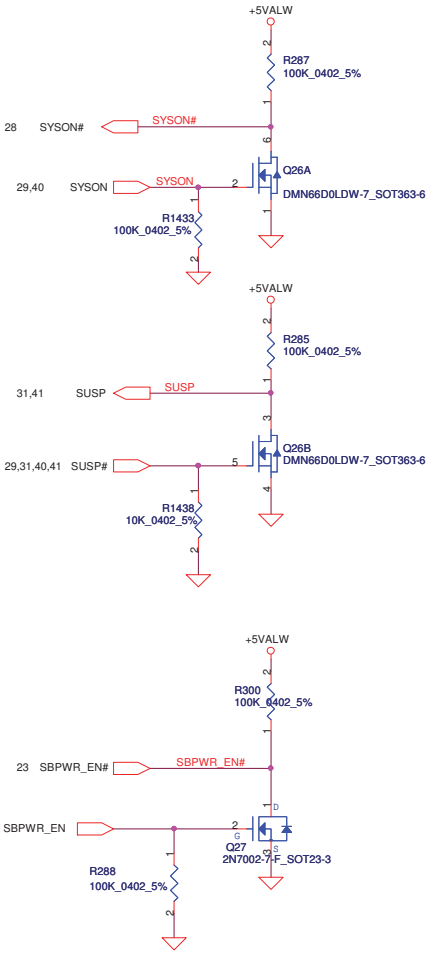


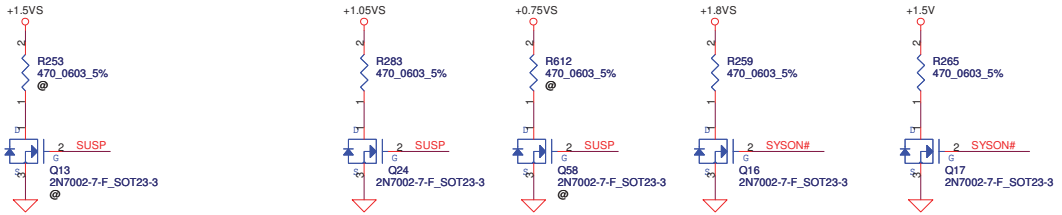
+3VALW TO +3VS

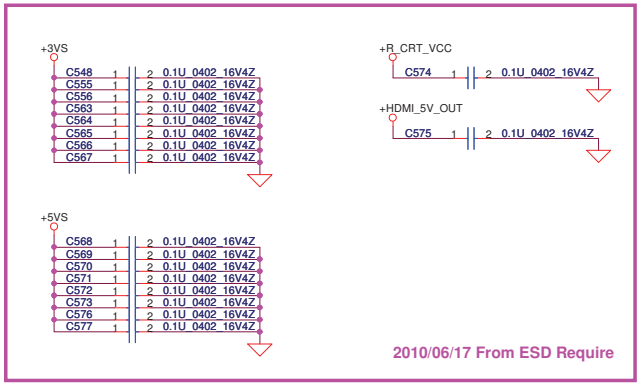


+1.5V to +1.5VS

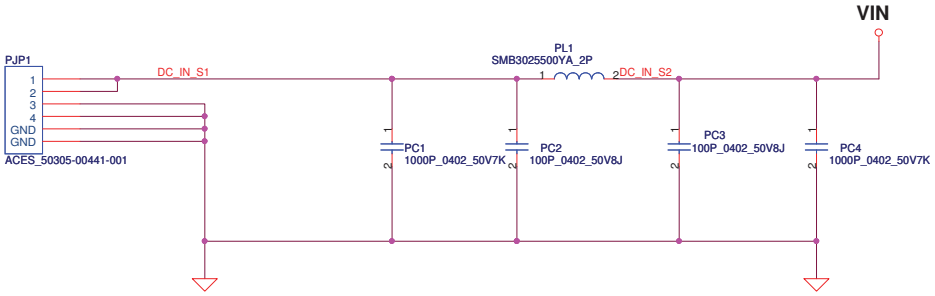


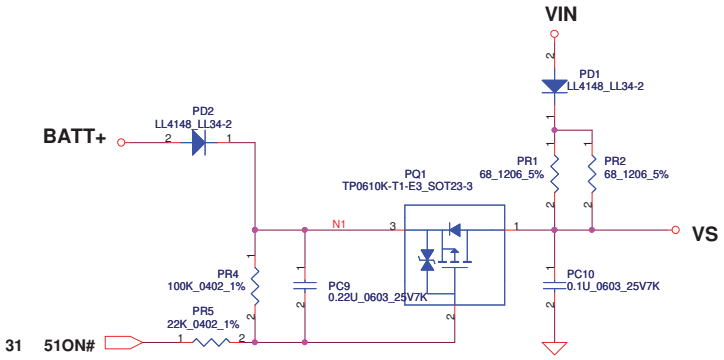


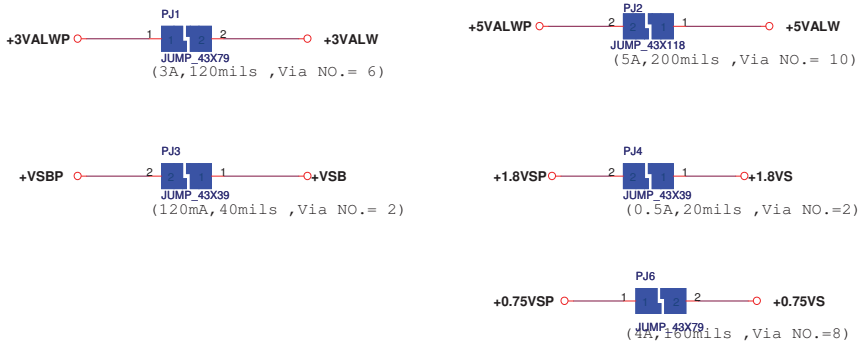


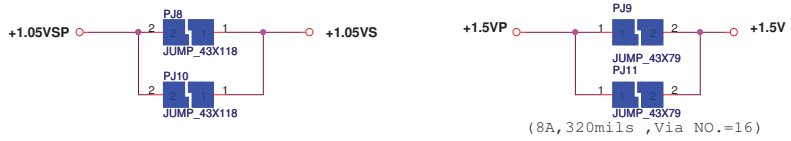


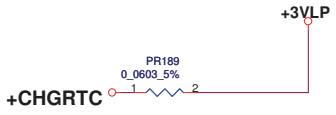
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/04/22	Deciphered Date 2011/04/22	Title: DC Interface
Document Number: PEW72/82 M/B LA-6631P Schematic			Rev: 1.0
Date: Thursday, July 08, 2010		Sheet 34 of 44	











Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title: DCIN

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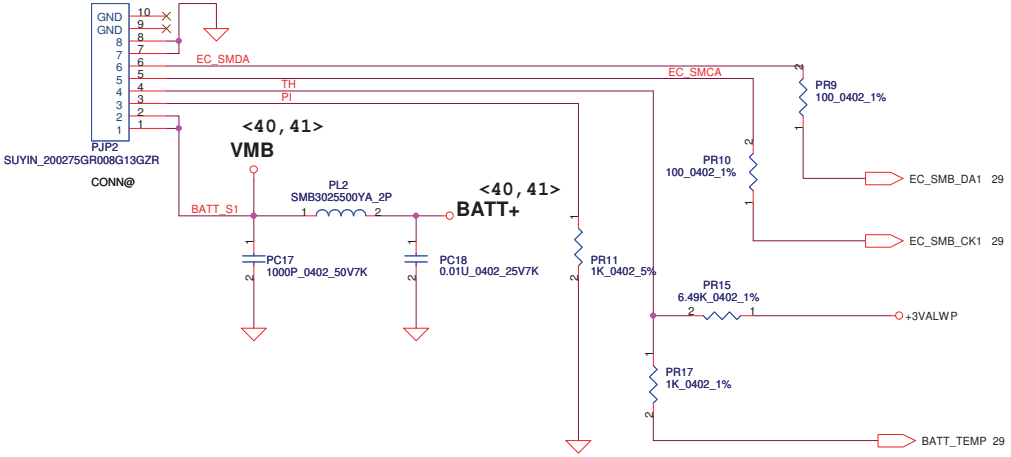
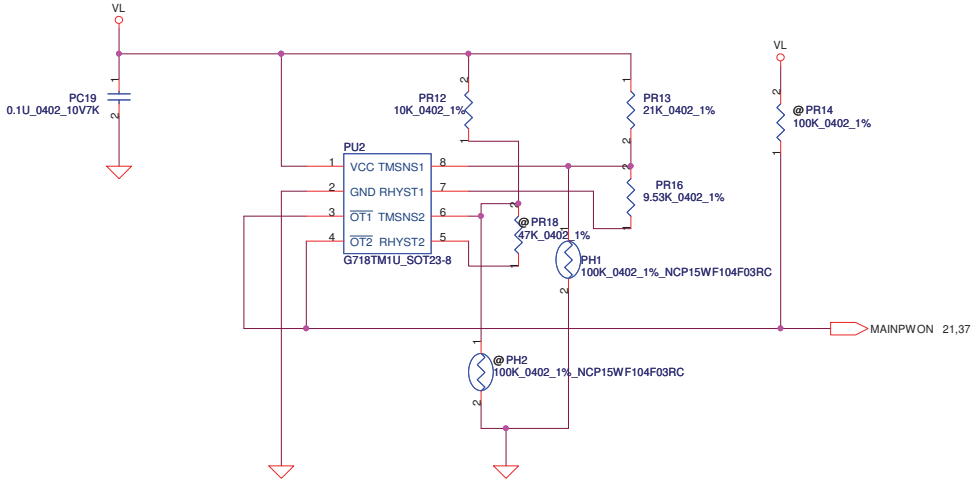
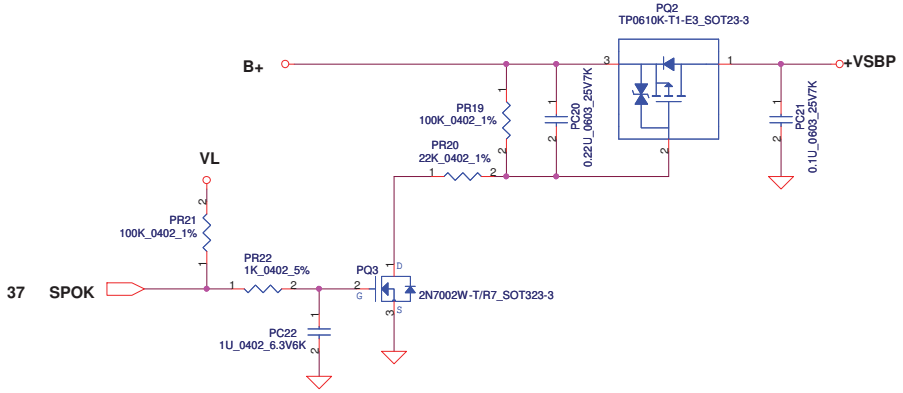


PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.	
Title	BATTERY CONN / OTP
Size: Custom	Document Number: PEW72
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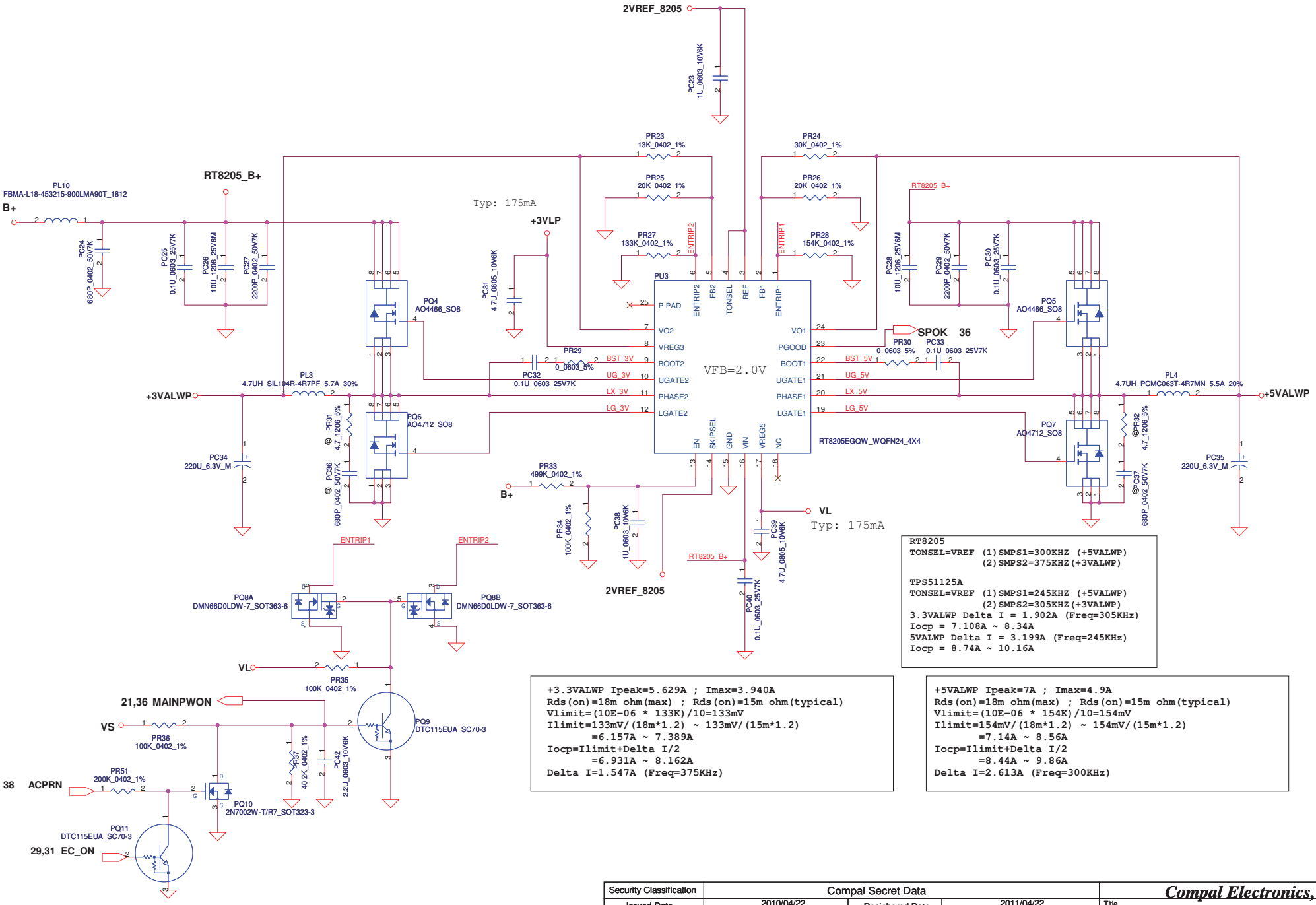
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 7.108A ~ 8.34A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.74A ~ 10.16A

+3.3VALWP Ipeak=5.629A ; Imax=3.940A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(10E-06 * 133K)/10=133mV
Ilimit=133mV/(18m*1.2) ~ 133mV/(15m*1.2)
=6.157A ~ 7.389A
Iocp=Ilimit+Delta I/2
=6.931A ~ 8.162A
Delta I=1.547A (Freq=375KHz)

+5VALWP Ipeak=7A ; Imax=4.9A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(10E-06 * 154K)/10=154mV
Ilimit=154mV/(18m*1.2) ~ 154mV/(15m*1.2)
=7.14A ~ 8.56A
Iocp=Ilimit+Delta I/2
=8.44A ~ 9.86A
Delta I=2.613A (Freq=300KHz)

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title: 3VALW/5VALW

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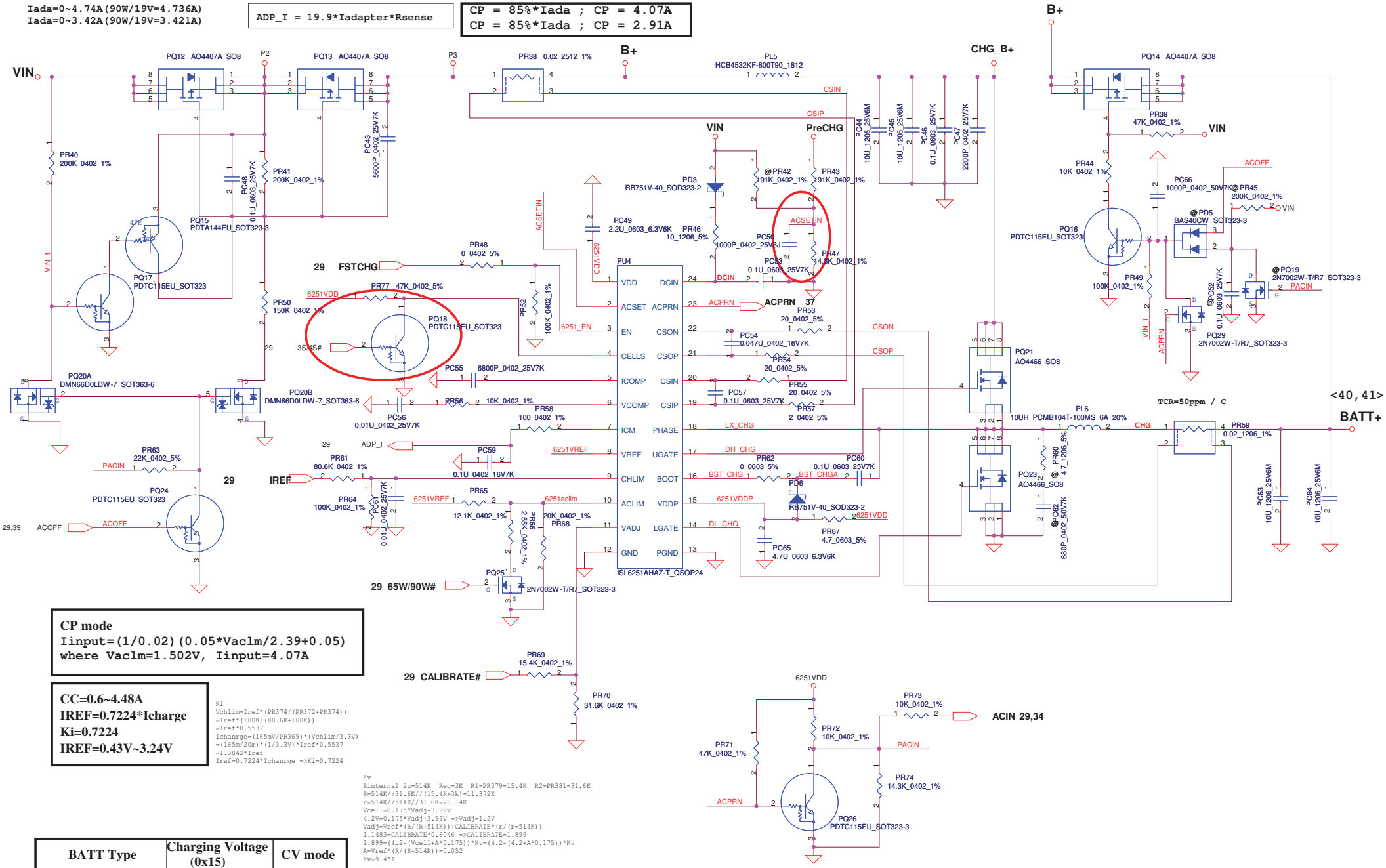
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
IREF=0.7224*Icharge
Ki=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//((15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: PEW72 | Rev: 1.0

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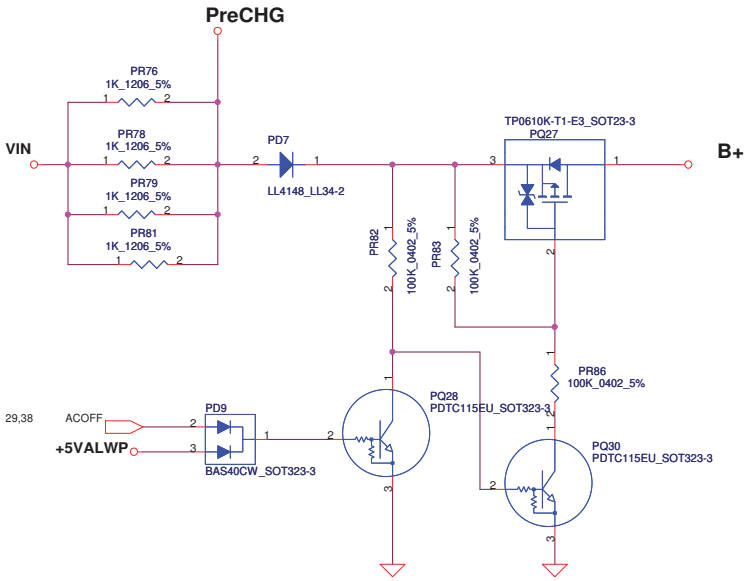


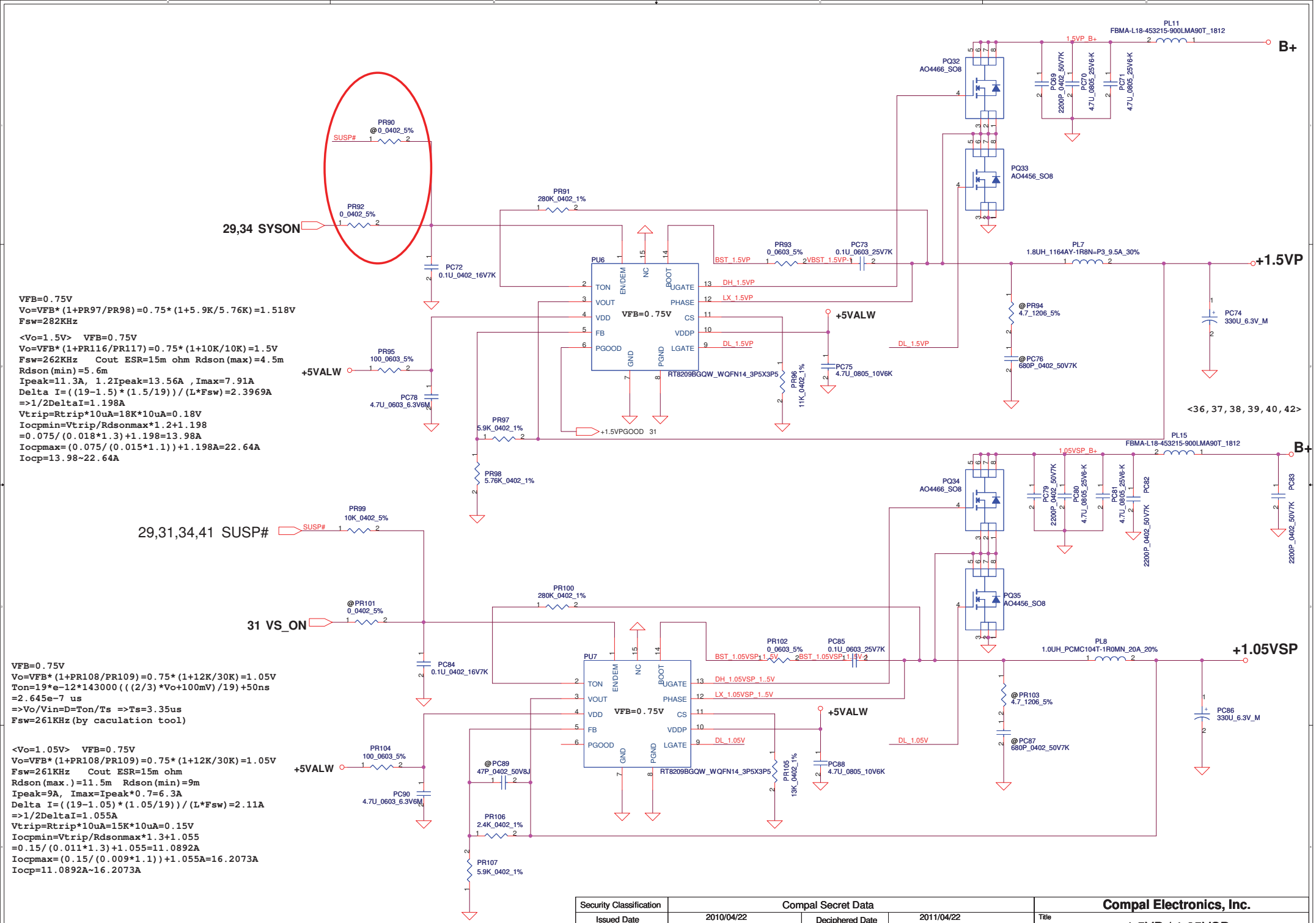
Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title: PRECHARGE

Size	Document Number	Rev
Custom	PEW72	1.0

Date: Thursday, July 08, 2010 | Sheet 39 of 44

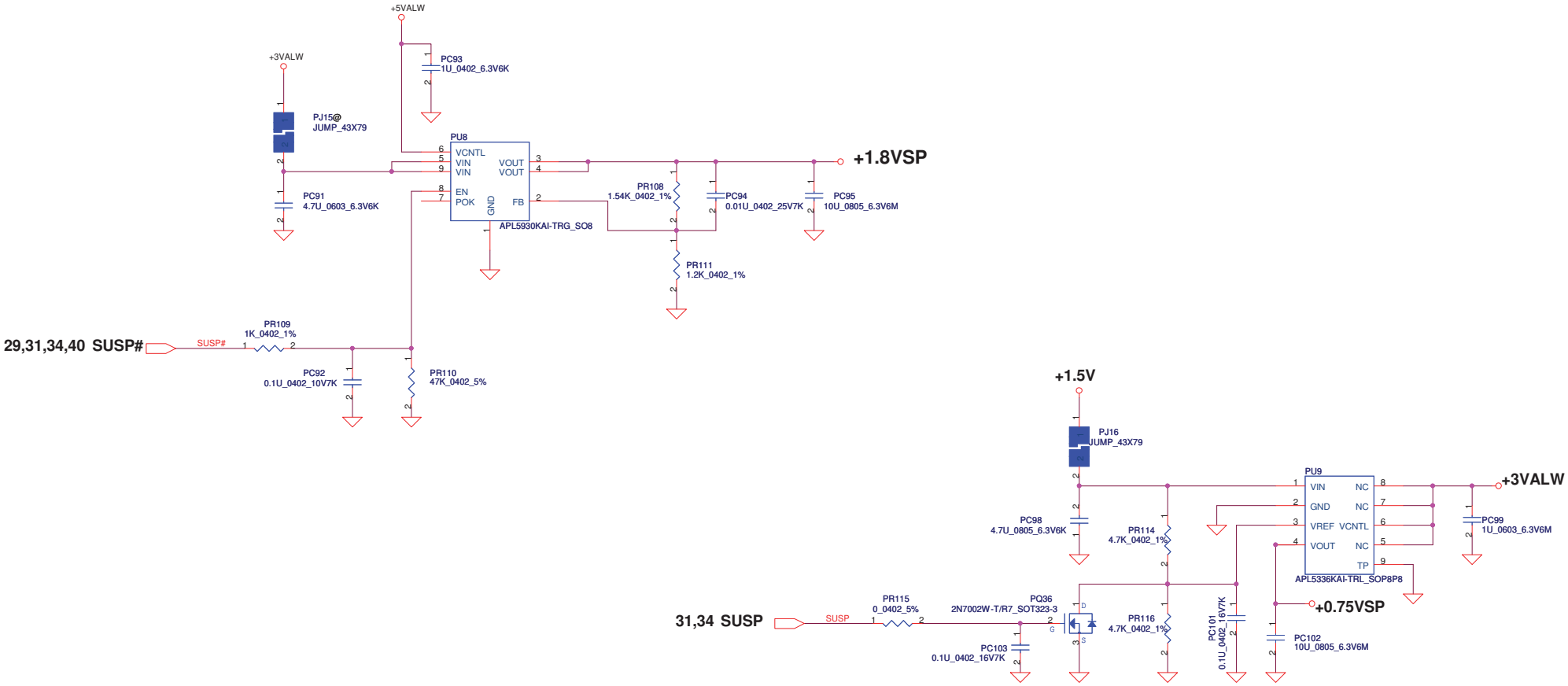



```
VFB=0.75V
Vo=VFB*(1+PR97/PR98)=0.75*(1+5.9K/5.76K)=1.518V
Fsw=282KHz

<Vo=1.5V>  VFB=0.75V
Vo=VFB*(1+PR116/PR117)=0.75*(1+10K/10K)=1.5V
Fsw=262KHz   Cout ESR=15m ohm Rdson(max)=4.5m
Rdson(min)=5.6m
Ipeak=11.3A, 1.2Ipeak=13.56A ,Imax=7.91A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=2.3969A
=>1/2DeltaI=1.198A
Vtrip=Rtrip*10uA=18K*10uA=0.18V
Iocpmin=Vtrip/Rdsonmax*1.2+1.198
=0.075/(0.018*1.3)+1.198=13.98A
Iocpmax=(0.075/(0.015*1.1))+1.198A=22.64A
Iocp=13.98~22.64A
```

```
VFB=0.75V
Vo=VFB*(1+PR108/PR109)=0.75*(1+12K/30K)=1.05V
Ton=19*e-12*143000(((2/3)*Vo+100mV)/19)+50ns
=2.645e-7 us
=>Vo/Vin=D=Ton/Ts =>Ts=3.35us
Fsw=261KHz(by caculation tool)

<Vo=1.05V>  VFB=0.75V
Vo=VFB*(1+PR108/PR109)=0.75*(1+12K/30K)=1.05V
Fsw=261KHz   Cout ESR=15m ohm
Rdson(max.)=11.5m  Rdson(min)=9m
Ipeak=9A, Imax=Ipeak*0.7=6.3A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.11A
=>1/2DeltaI=1.055A
Vtrip=Rtrip*10uA=15K*10uA=0.15V
Iocpmin=Vtrip/Rdsonmax*1.3+1.055
=0.15/(0.011*1.3)+1.055=11.0892A
Iocpmax=(0.15/(0.009*1.1))+1.055A=16.2073A
Iocp=11.0892A~16.2073A
```

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

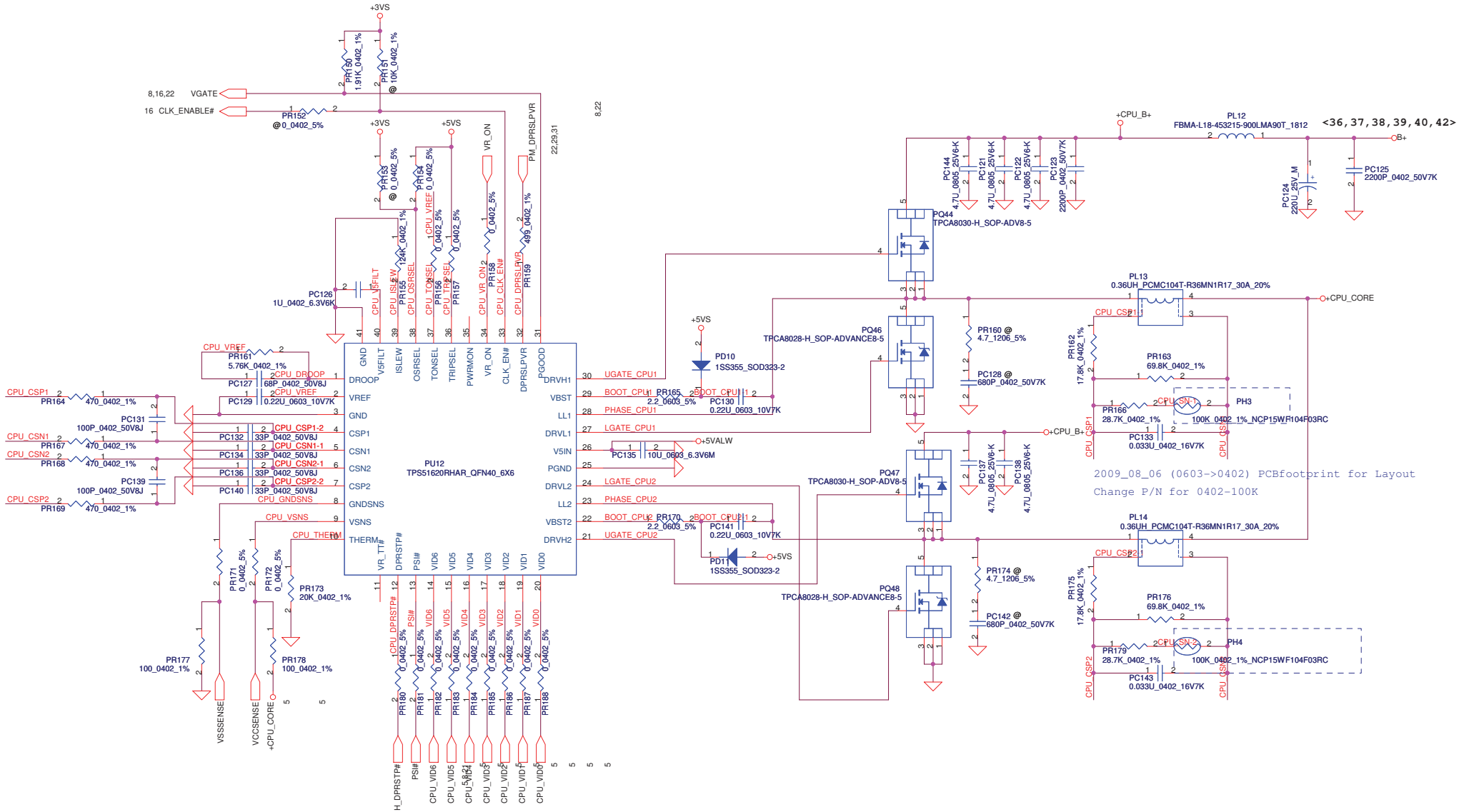
Compal Electronics, Inc.			
Title	1.5VP / 1.05VSP		
Size: Custom	Document Number: PEW72		Rev: 1.0
Date: Thursday, July 08, 2010	Sheet 40 of 44		



Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title	+1.5VP/+1.8VSP/+1.0VSDGPU		
Size: Custom	Document Number: PEW72		Rev: 1.0
Date: Thursday, July 08, 2010	Sheet 41 of 44		



Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.			
Title: +CPU_CORE			
Size: Custom	Document Number: PEW72		Rev: 1.0
Date: Thursday, July 08, 2010	Sheet 42 of 44		

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add 3S/4S pin function	add 4 cell battery	0.2	45	add PQ18 PDTC115EU_SOT323 (SB301150200) and PR77 47K +-5% 0402(SD028470280)	2010/06/11	EVT
2	ACSETIN net	ACSETIN net no connect	0.2	45		2010/06/11	EVT
3	1.5V enable	1.5V enable BOM error	0.2	45	add PR92 and delete PR90 0_0402_5% (SD028000080)	2010/06/11	EVT
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
16							
17							

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom	PEW72/82 M/B LA-6631P Schematic	1.0
Date: Thursday, July 08, 2010	Sheet 43 of 44	

A --> C Change List

20100622----------
1. Change U48 to SA00002KI00 (EON EN25F16-100HIP)
2. Populate D11, D12
3. Populate R132, C194, R136, C225, R354, C416
20100618----------
1. Page 30, For EMI reuqire populate C31, C32, C33, C34, C28, C35, C36, C27, C30, C29, C39, C40, C41,
   C42, C43, C24, C46, C47, C48 C23, C22, C21
2. Page 12, Populate C483
20100617----------
1. Add T19, T25 for boundary scan (CIT Factory)
2. Page 34, Add 0.1U_0402_16V4Z x 16 for +3VS/+5VS/+R_CRT_VCC/+HDMI_5V_OUT
C548, C555, C556, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577
3. Page 29, Reserved R38, R616 for SPI_WP#
20100615----------
1. Page22, Add C745 for USB_OC#1_6 at chipset side.
2. Page28, Change C744 BOM Structure to @
20100614----------
1. Page29, Change U13 to KB926QFD3 (SA00001J580)
   Change R1432 to 8.2K_0402_5% (SD028820180)
2. Page16, Change U16 to ICS9LPRS387 (SA000020H10)
   Change BOM Structure of L33 and R401 to @
   Populate L32 and R400
3. Page31, Change BOM Structure of SW1 and SW2 to @
4. Change U7, U8, U43 to MC74VHC1G08DFT2G (SA00000OH00)
5. Update Power Schematics

C --> MP Change List

20100709----------
1. Page33, Change C561, C530, C536 to 0 ohm (SD028000080)
   Change R465, R458 to 0.47U_0603 (SE080474K80)
20100708----------
1. Page28, Unpopulate D23 (follow ESD suggestion)
20100706----------
1. Page29, Populate R289 and C340.
2. Page30, Unpopulate C21 ~ C43 and C46 ~ C48.

Security Classification	Compal Secret Data		
Issued Date	2010/04/22	Deciphered Date	2011/04/22

Compal Electronics, Inc.

Title: HW (PWR)

Size	Document Number	Rev
Custom	PEW72/82 M/B LA-6631P Schematic	1.0

Date: Friday, July 09, 2010 Sheet 44 of 44