Compal Confidential

HCW50 Schematics Document

AMD/Sempron/ATI RX485/SB460 W/s M52/54/56P

2006 / 02 / 28 Rev:0.3 (For PVT)

Security Classification	Compal Secret Data		
Issued Date	2005/05/09	Deciphered Date	2006/03/08

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Date: 星期四, 三月 09, 2006	Sheet 1 of 55	

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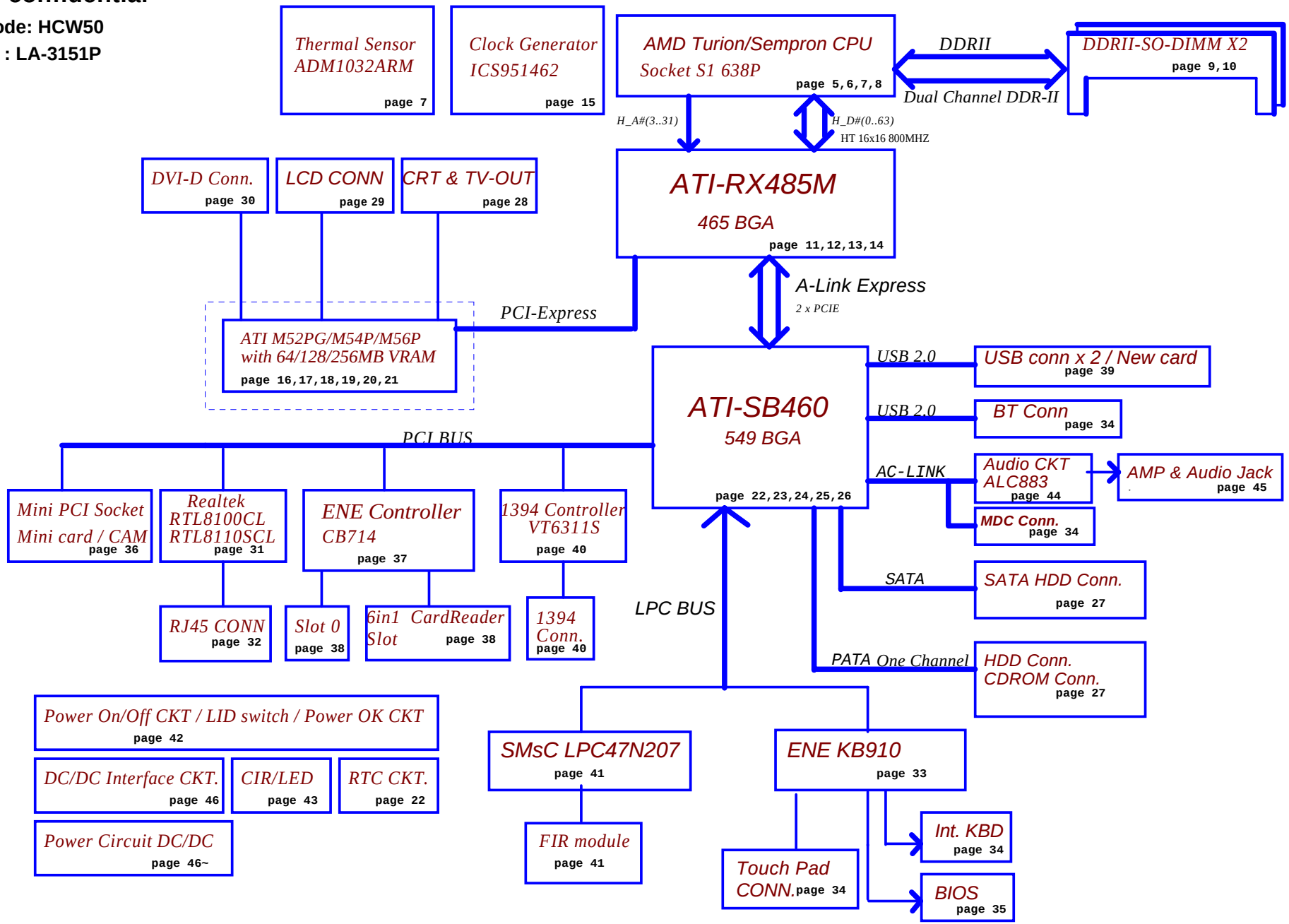
Project Code: HCW50

File Name : LA-3151P



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*
+1.2VS	1.2V switched power rail for PCIE	ON	OFF	OFF
+0.9VS	0.9V switched power rail for VRAM terminator	ON	OFF	OFF
+1.8VALW	1.8V switched power rail	ON	ON	ON*
+VDD_CORE	1.0~1.2V switched power rail for VGA	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
Fintek F75383M	1001 100X b

SB460 SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	
UMA	
UMA's DVI	
LAN(10/100)	
LAN(GIGA)	
MINI CARD1	
MINI CARD2	
SATA-to-IDE	
PATA	
GRAPEVINE	
G72MV Only	
G73 Only	
VRAM	
VRAM 64M	
VRAM 128M	
VRAM 256M	
MEDIA/B	
CIR	
FIR	
GENEVA	
LCM	
Sub-woofer	

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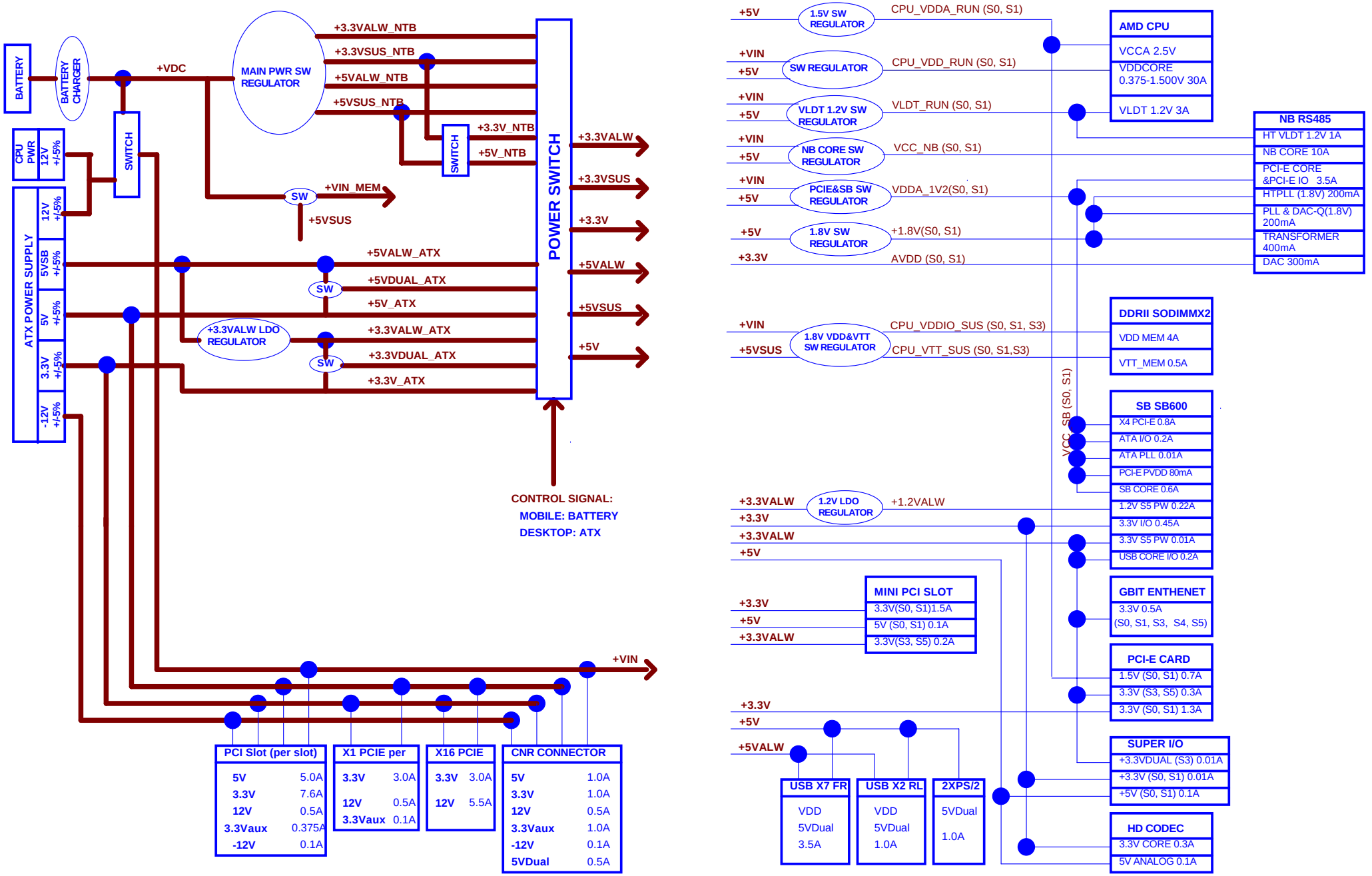

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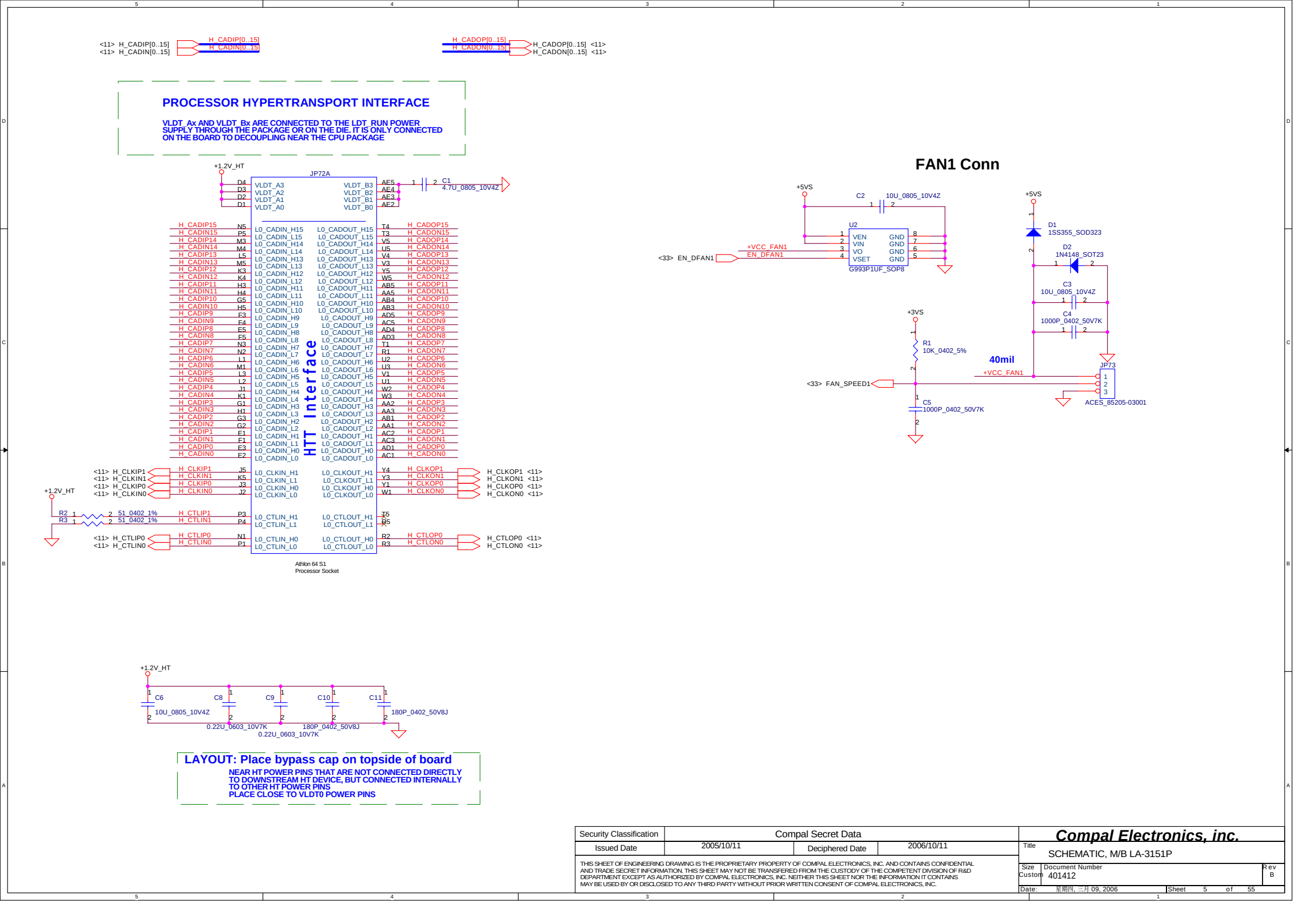

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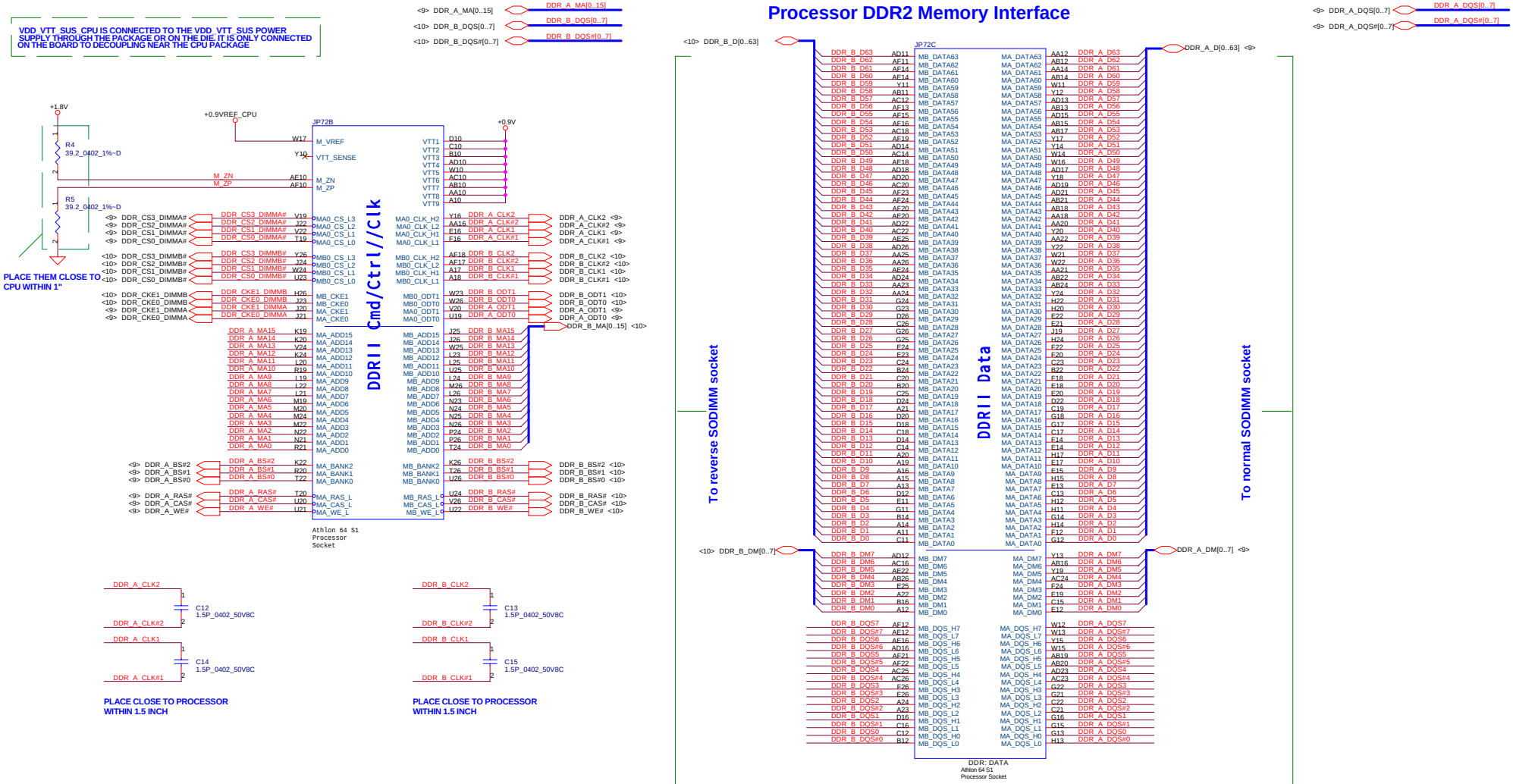
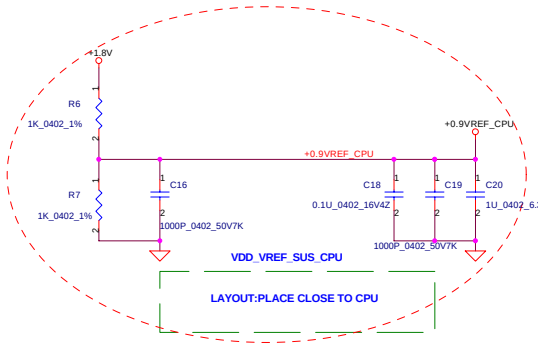
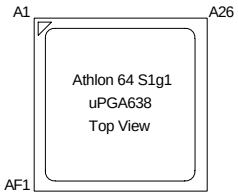
Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



ATI check ,Use +0.9V PWR , can delete or not





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ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

50mil width(600mA)

SB460 ONLY

place them to CPU within 1"

Modify 11/22

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

Place within 0.5" from CPU
25mil/6mil/6mil/6mil/25mil

AMD NPT S1 SOCKET
Processor Socket

HDT Connector

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

@SAMTEC_ASP-68200-07

F75383M_MSOP8

SMBus Address: 1001110X (b)

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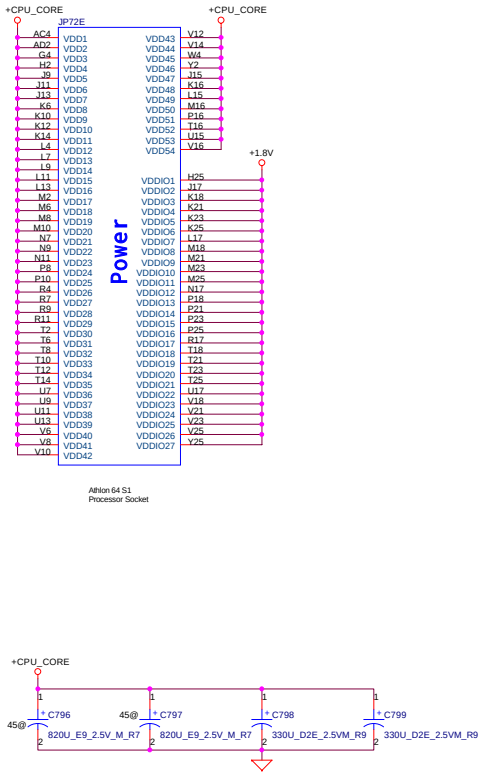
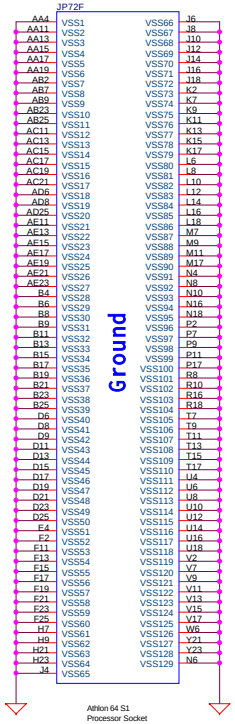
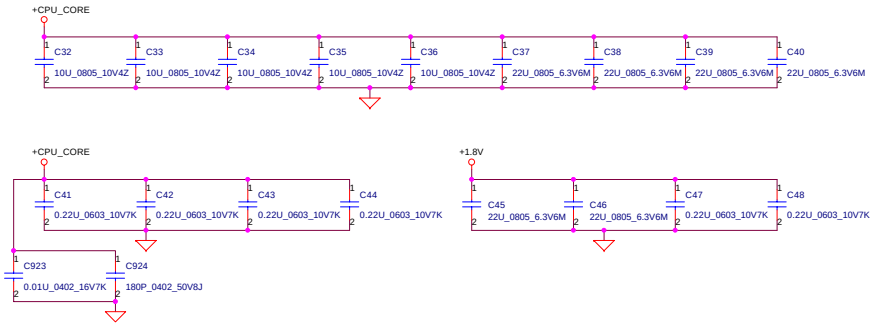
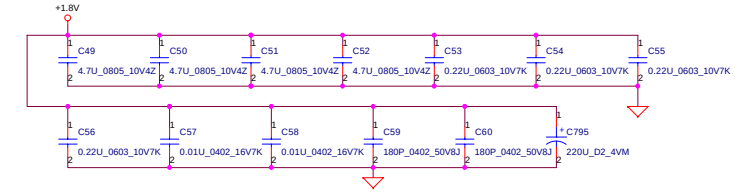




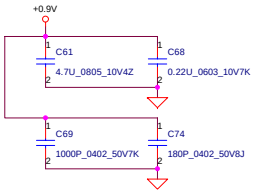
BOTTOMSIDE DECOUPLING



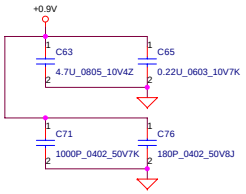
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

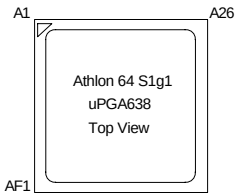


CPU left-hand side



CPU right-hand side





PROCESSOR POWER AND GROUND

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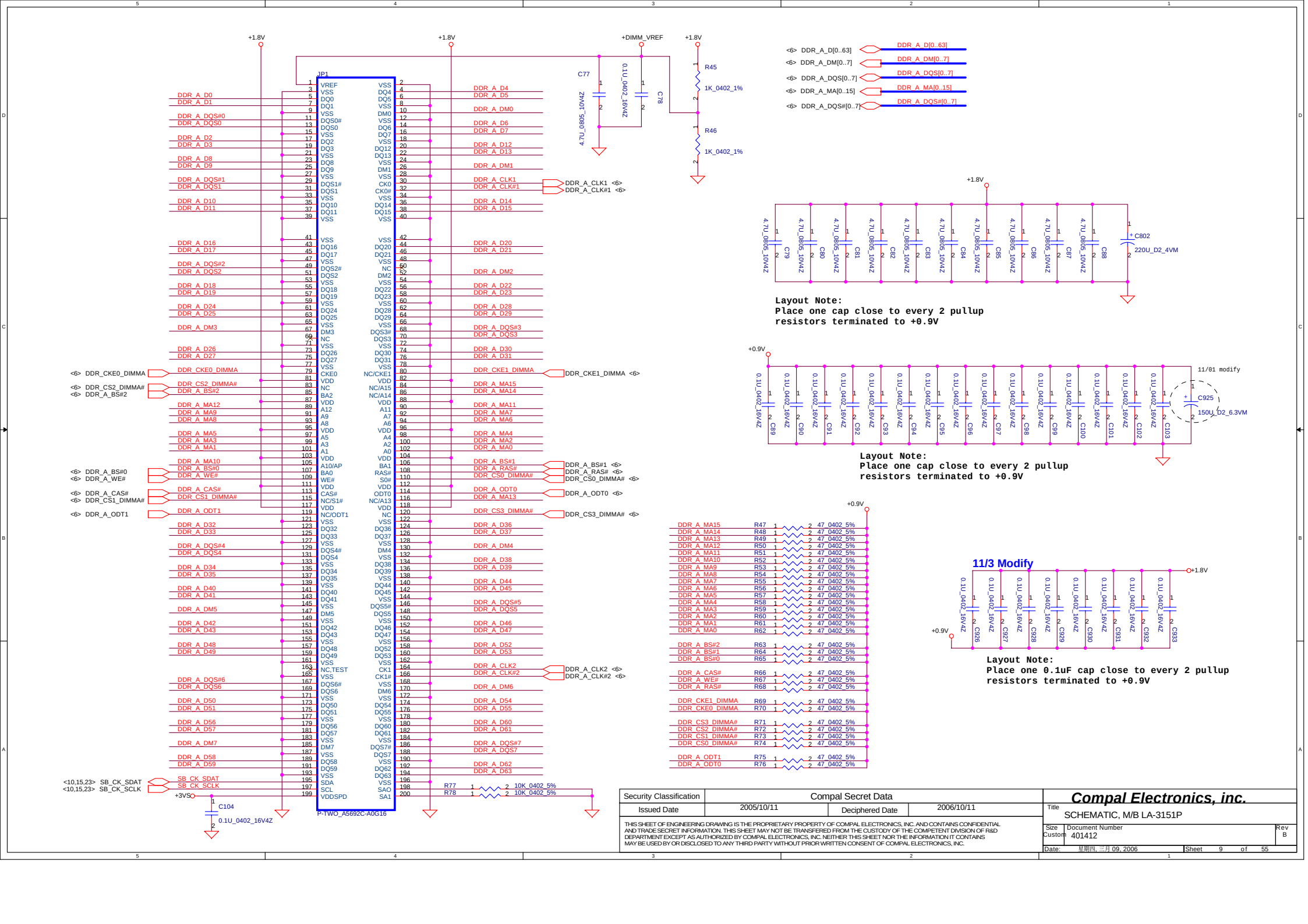

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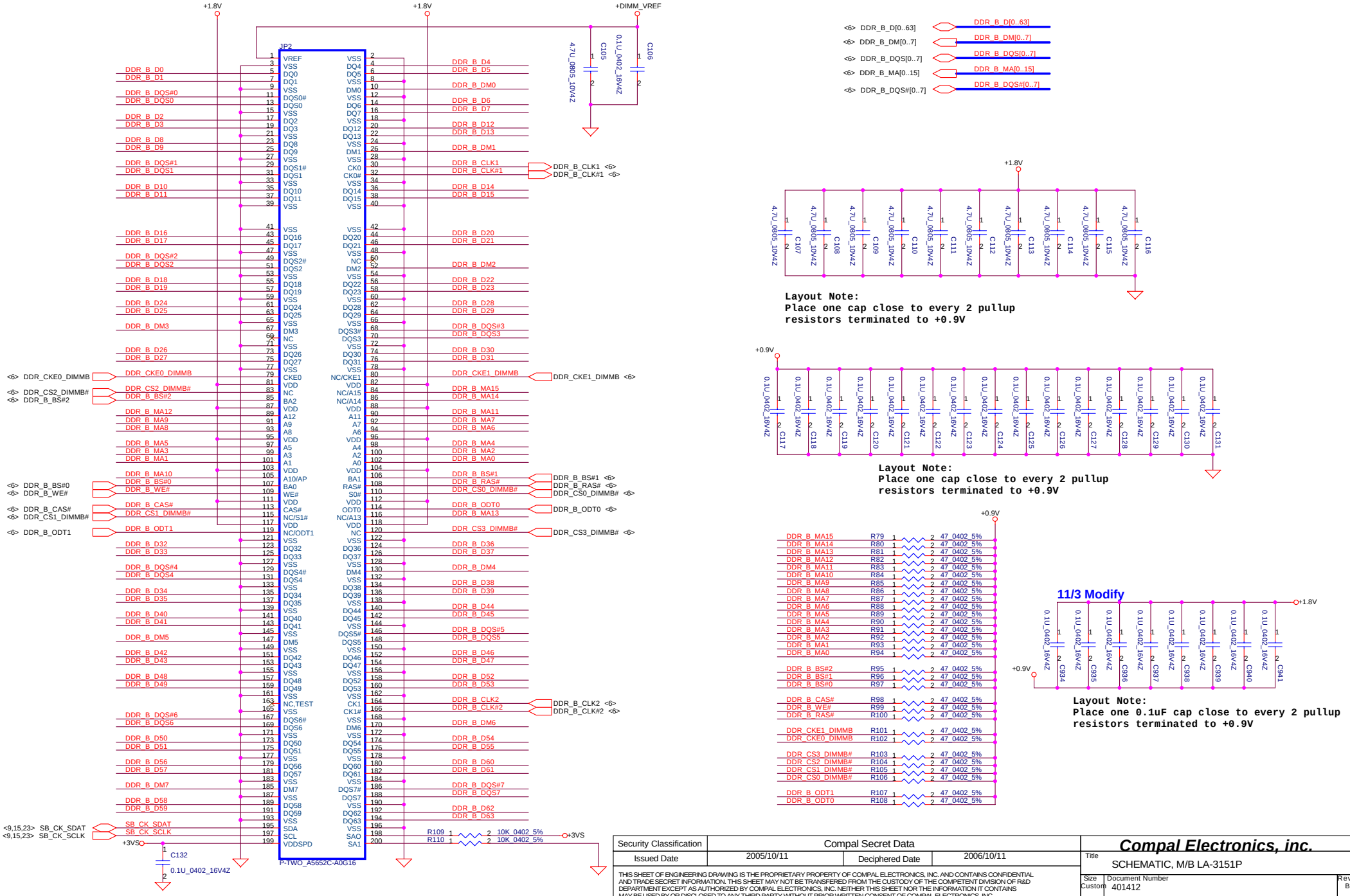

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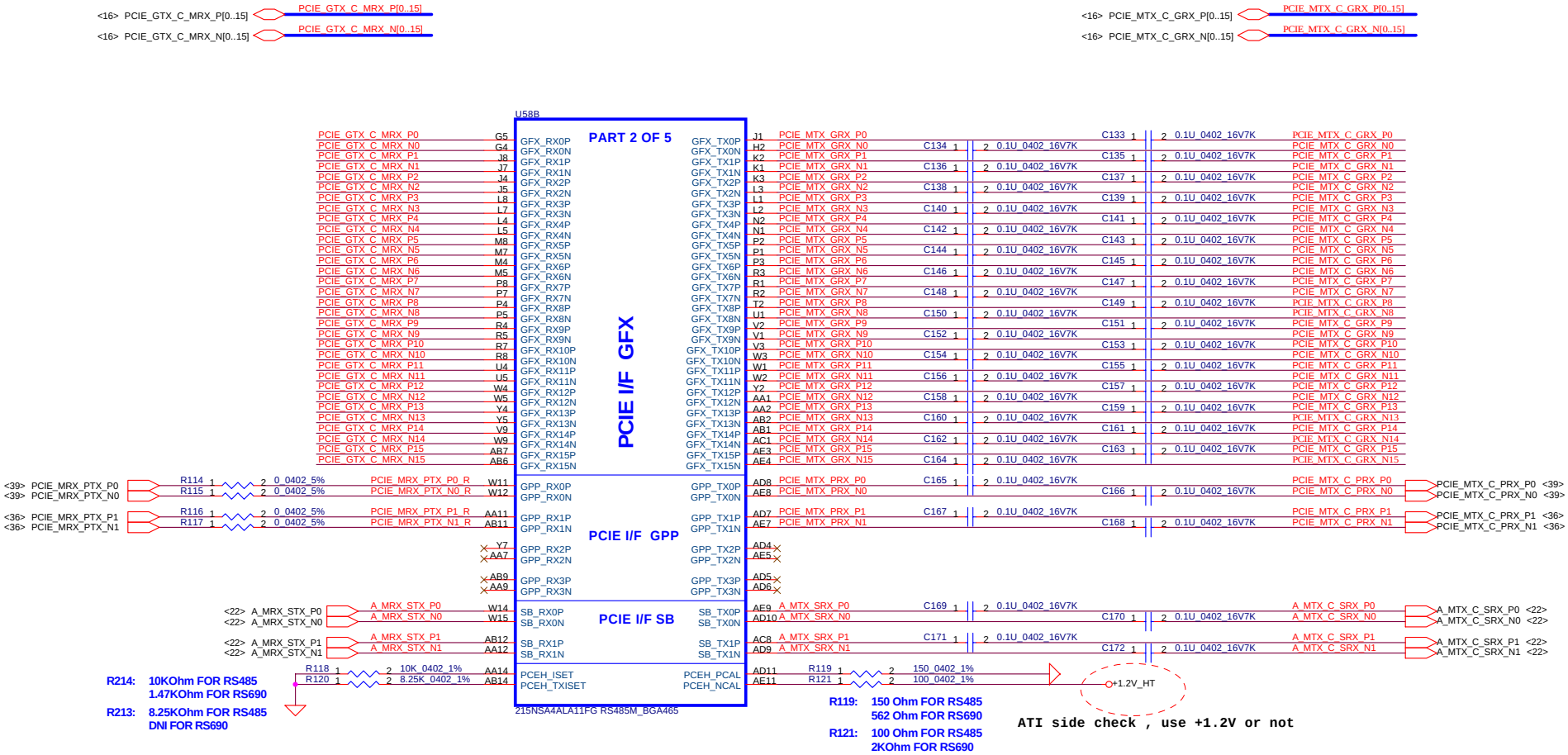

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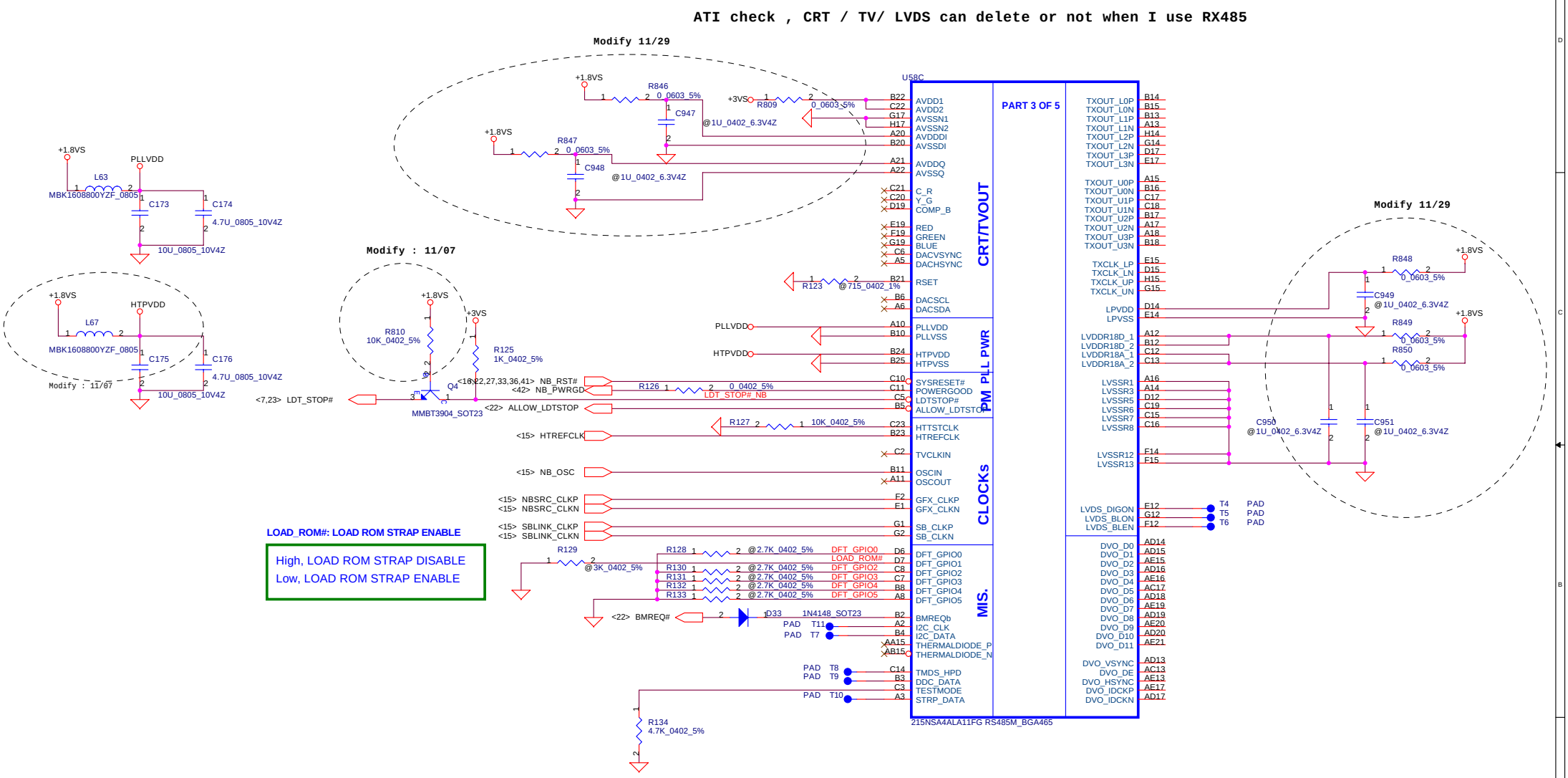

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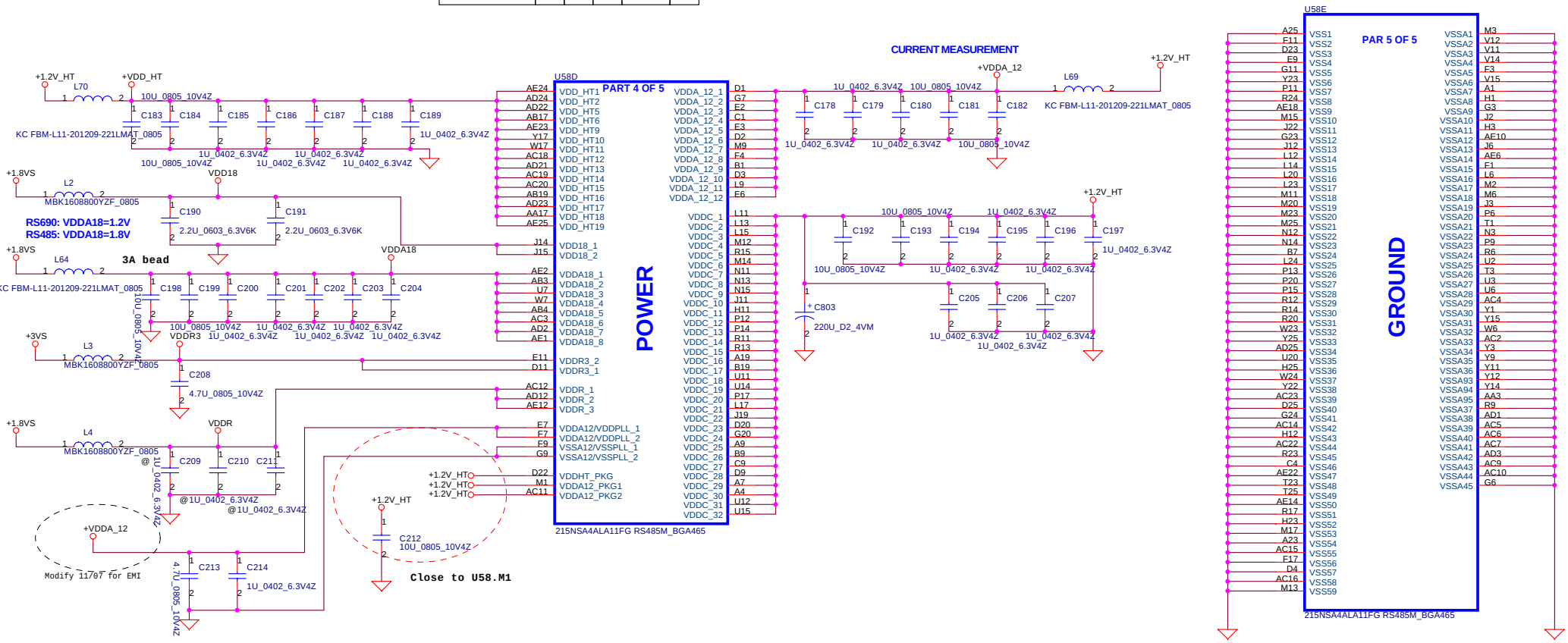
NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



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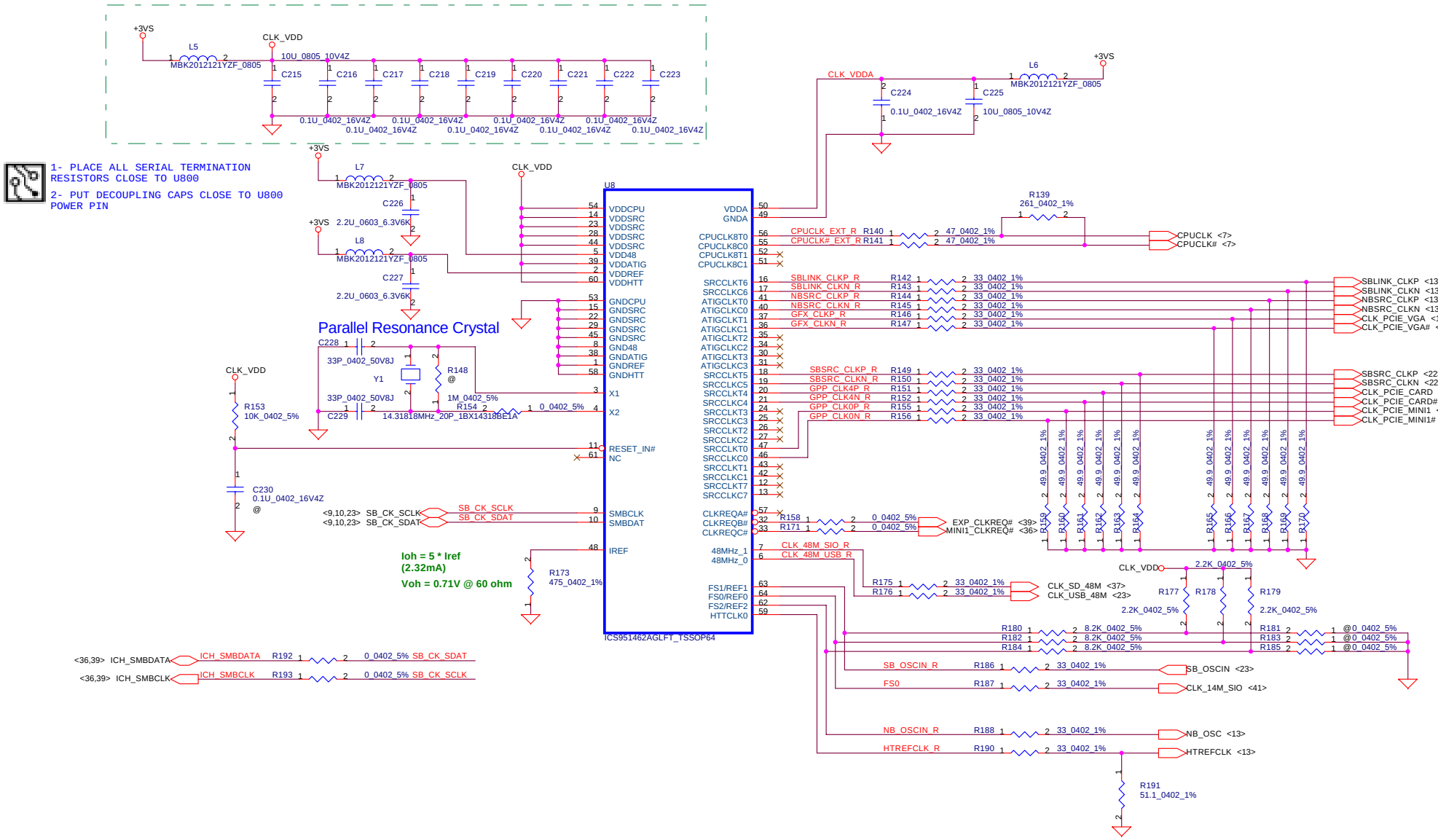

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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PCIE Lane Reversal

<15> CLK_PCIE_VGA
<15> CLK_PCIE_VGA#

PCIE_GTX_C_MRX_N15 C232 0.1U_0402_16V7K PCIE_GTX_MRX_N15 AK27
PCIE_GTX_C_MRX_P15 C231 0.1U_0402_16V7K PCIE_GTX_MRX_P15 AJ27
PCIE_GTX_C_MRX_N14 C234 0.1U_0402_16V7K PCIE_GTX_MRX_N14 AJ25
PCIE_GTX_C_MRX_P14 C233 0.1U_0402_16V7K PCIE_GTX_MRX_P14 AH25
PCIE_GTX_C_MRX_N13 C236 0.1U_0402_16V7K PCIE_GTX_MRX_N13 AH28
PCIE_GTX_C_MRX_P13 C235 0.1U_0402_16V7K PCIE_GTX_MRX_P13 AG28
PCIE_GTX_C_MRX_N12 C238 0.1U_0402_16V7K PCIE_GTX_MRX_N12 AG27
PCIE_GTX_C_MRX_P12 C237 0.1U_0402_16V7K PCIE_GTX_MRX_P12 AF27
PCIE_GTX_C_MRX_N11 C240 0.1U_0402_16V7K PCIE_GTX_MRX_N11 AF25
PCIE_GTX_C_MRX_P11 C239 0.1U_0402_16V7K PCIE_GTX_MRX_P11 AE25
PCIE_GTX_C_MRX_N10 C242 0.1U_0402_16V7K PCIE_GTX_MRX_N10 AE28
PCIE_GTX_C_MRX_P10 C241 0.1U_0402_16V7K PCIE_GTX_MRX_P10 AD28
PCIE_GTX_C_MRX_N9 C244 0.1U_0402_16V7K PCIE_GTX_MRX_N9 AD27
PCIE_GTX_C_MRX_P9 C243 0.1U_0402_16V7K PCIE_GTX_MRX_P9 AC27
PCIE_GTX_C_MRX_N8 C246 0.1U_0402_16V7K PCIE_GTX_MRX_N8 AC25
PCIE_GTX_C_MRX_P8 C245 0.1U_0402_16V7K PCIE_GTX_MRX_P8 AB25
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PCIE_GTX_C_MRX_P4 C254 0.1U_0402_16V7K PCIE_GTX_MRX_P4 V28
PCIE_GTX_C_MRX_N3 C257 0.1U_0402_16V7K PCIE_GTX_MRX_N3 V27
PCIE_GTX_C_MRX_P3 C256 0.1U_0402_16V7K PCIE_GTX_MRX_P3 U27
PCIE_GTX_C_MRX_N2 C259 0.1U_0402_16V7K PCIE_GTX_MRX_N2 U25
PCIE_GTX_C_MRX_P2 C258 0.1U_0402_16V7K PCIE_GTX_MRX_P2 T25
PCIE_GTX_C_MRX_N1 C261 0.1U_0402_16V7K PCIE_GTX_MRX_N1 T28
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PCIE_GTX_C_MRX_N0 C263 0.1U_0402_16V7K PCIE_GTX_MRX_N0 R27
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PCIE_MTX_C_GRX_P14 AG30
PCIE_MTX_C_GRX_N13 AG32
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PCIE_MTX_C_GRX_N9 AC31
PCIE_MTX_C_GRX_P9 AB31
PCIE_MTX_C_GRX_N8 AB30
PCIE_MTX_C_GRX_P8 AA30
PCIE_MTX_C_GRX_N7 AA32
PCIE_MTX_C_GRX_P7 Y32
PCIE_MTX_C_GRX_N6 Y31
PCIE_MTX_C_GRX_P6 W31
PCIE_MTX_C_GRX_N5 W30
PCIE_MTX_C_GRX_P5 V30
PCIE_MTX_C_GRX_N4 V32
PCIE_MTX_C_GRX_P4 U32
PCIE_MTX_C_GRX_N3 U31
PCIE_MTX_C_GRX_P3 T31
PCIE_MTX_C_GRX_N2 T30
PCIE_MTX_C_GRX_P2 R30
PCIE_MTX_C_GRX_N1 R32
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PCIE_MTX_C_GRX_P0 N31

<12> PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]
<12> PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
<12> PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
<12> PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]

U9A

PCIE_REFCLKP
PCIE_REFCLKN
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N

PCI EXPRESS

PCIE_CALRN
PCIE_CALRP
PCIE_CALI
PERST#
PCIE_TEST
PERST#_MASK

GPIO

GPIO_0 AD4 R194 1 2 10K_0402_5%
GPIO_1 AD2 R195 1 2 10K_0402_5%
GPIO_2 AD1
GPIO_3 AD3
GPIO_4 AC1 R196 1 2@10K_0402_5%
GPIO_5 AC2 R197 1 2 10K_0402_5%
GPIO_6 AC3
GPIO_7_BLON AB2 R198 1 2@10K_0402_5%
GPIO_8 AC6
GPIO_9 AC5 R199 1 @ 2 10K_0402_5%
GPIO_10 AC4 TP1
GPIO_11 AB3 R200 1 @ 2 10K_0402_5%
GPIO_12 AB4 R201 1 X76@ 2 10K_0402_5%
GPIO_13 AB5 R202 1 X76@ 2 10K_0402_5%
GPIO_14 AD5
GPIO_15 AB8 POWER_SEL
GPIO_16 AA8 OSC_SPREAD
GPIO_17 AB7 THER_ALERT#
NC AB6
VREFG AC8 R203 2 1 499_0402_1%
R204 1 2 499_0402_1%
C250 1 2 0.1U_0402_16V4Z

+3VS
POWER_SEL <53>
Low -> VDDC=1.2V
High -> VDDC=1.0V

VIP HOST/ EXTERNAL TMDS

NC_DVOVMODE_0 AK4
NC_DVOVMODE_1 AL4

DVPCNTL_0 AF2
DVPCNTL_1 AE1
DVPCNTL_2 AF3
DVPCLK AG1
DVPDATA_0 AG2
DVPDATA_1 AG3
DVPDATA_2 AH2
DVPDATA_3 AH3
DVPDATA_4 AJ2
DVPDATA_5 AJ1
DVPDATA_6 AK2
DVPDATA_7 AK1
DVPDATA_8 AK3
DVPDATA_9 AL2
DVPDATA_10 AL3
DVPDATA_11 AM3
DVPDATA_12 AE6
DVPDATA_13 AF4
DVPDATA_14 AE5
DVPDATA_15 AG4
DVPDATA_16 AJ3 TP2 R205 2 4.7K_0402_5%
DVPDATA_17 AH4 TP3 R206 2 4.7K_0402_5%
DVPDATA_18 AJ4 I2C_DAT
DVPDATA_19 AG5 I2C_CLK
DVPDATA_20 AH5 MEMID0 R207 1 2 10K_0402_5% X76@ +3VS
DVPDATA_21 AF6 MEMID1 R208 1 2 10K_0402_5% X76@
DVPDATA_22 AE7 MEMID2 R209 1 2 10K_0402_5% X76@
DVPDATA_23 AG6 TP4

I2C_DAT <29>
I2C_CLK <29>

CRT

R AK24 VGA_CRT_R
G AM24 VGA_CRT_G
B AL24 VGA_CRT_B

VGA_CRT_R <28>
VGA_CRT_G <28>
VGA_CRT_B <28>

HSYNC AJ23 CRT_HSYNC
VSYNC AJ22 CRT_VSYNC

CRT_HSYNC <28>
CRT_VSYNC <28>
Need Level Shift

DDC1DATA AH22 R213 2 4.7K_0402_5% +3VS
DDC1CLK AH23 R214 2 4.7K_0402_5%
VGA_CRT_DAT
VGA_CRT_CLK
Need Level Shift

VGA_CRT_DAT <28>
VGA_CRT_CLK <28>

GENERICA AK22
GENERICB AF23 R216 2 1 1K_0402_5%
GENERICA NC,GENERICB Grounded -->Internal SS LVDS Bus
RSET AL22 R219 2 1 499_0402_1%

TV

R2 AK15
G2 AM15
B2 AL15
H2SYNC AF15
V2SYNC AG15
Y AJ15 VGA_TV_Y
C AJ13 VGA_TV_C
COMP AH15 VGA_TV_COMP
R2SET AK14 R223 2 1 715_0402_1%

VGA_TV_Y <28>
VGA_TV_C <28>
VGA_TV_COMP <28>

ROMCS# AC7
PLLTEST AG14
TESTEN AG22 R228 2 1 1K_0402_5%

THERMAL

DPLUS AG12 D+
DMINUS AH12 D-
DDC3DATA AE12 R224 2 4.7K_0402_5% THERM_SDA
DDC3CLK AE12 R225 2 4.7K_0402_5% THERM_SCL

XTAL

XTALIN AL26 OSC_IN 1 R227 2 121_0402_1%
XTALOUT AM26 R229 71.5_0402_1%

M56P
M56@

+1.2VS
R215 2 2K_0402_1% AE24
R217 2 562_0603_1% AD24
R218 2 1.47K_0603_1% AB24

<13,22,27,33,36,41> NB_RST#
R220 1 2 0_0402_5% AG24
R221 1 2 10K_0402_5% AA24 AF24

Thermal sensor

+3VS
R210 2.2K_0402_5% THM@
U10
VDD SCLK THERM_SCL
D+ SDATA THERM_SDA
D- ALERT# THER_ALERT#
OVERT# GND
R212 0_0402_5% THM@
R211 2.2K_0402_5% THM@
C264 THM@ 2200P_0402_50V7K
THM@ MAX6649MUA_8UMAX

Spread spectrum

+3VS
SSC@ 0_0603_5% R222
U11
VDD REF
XIN MODOUT
XOUT NC
VSS PD#
ASM3P1819N-SR_SO8
SSC@
Memory Interface SS
R226 1 2 22_0402_5% OSC_SPREAD SSC@
C265 SSC@ 0.1U_0402_16V4Z
Minimize distance from X1 pin3 to U3 pin1
+3VS
C266 0.1U_0402_16V4Z
R230 1K_0402_5%
X1
VDD OUT
OE GND
27MHZ_15P
OSC_IN

Keep away from other signal at last 25mils

Straps: (Internal pull down)

Transmitter power saving enable	GPIO[0]	0: 50% TX output swing 1: Full TX output swing
Transmitter de-emphasis enable	GPIO[1]	0: TX de-emphasis disable 1: TX de-emphasis enable
Debug Access	GPIO[4]	0: OFF Pad must be available 1: ON
PLL_IBIAS_RD	GPIO[6,5]	Default : 01
ROM ID Config	GPIO[9, 13:11]	000X: No ROM, AP_SIZE=00 128M share 001X: No ROMMemory AP_SIZE=01 256M share 010X: No ROMMemory AP_SIZE=10 64M share 011X: No ROMMemory AP_SIZE=11 Reserved

Vedio Memory Config. (VGA Internal PD)

MEMID[2:0]	Size	Size	Vender	Chips	VGA	Frequence
0 0 0	64MB	16M16	Hynix	2		
0 0 1	64MB	16M16	Samsung	2		
0 1 0	128MB	16M16	Hynix	4		A-test
0 1 1	128MB	16M16	Samsung	4		
1 0 0	256MB	32M16	Hynix	4		A-test
1 0 1	256MB	32M16	Samsung	4		
1 1 0		Resreved				
1 1 1		Resreved				

TBD

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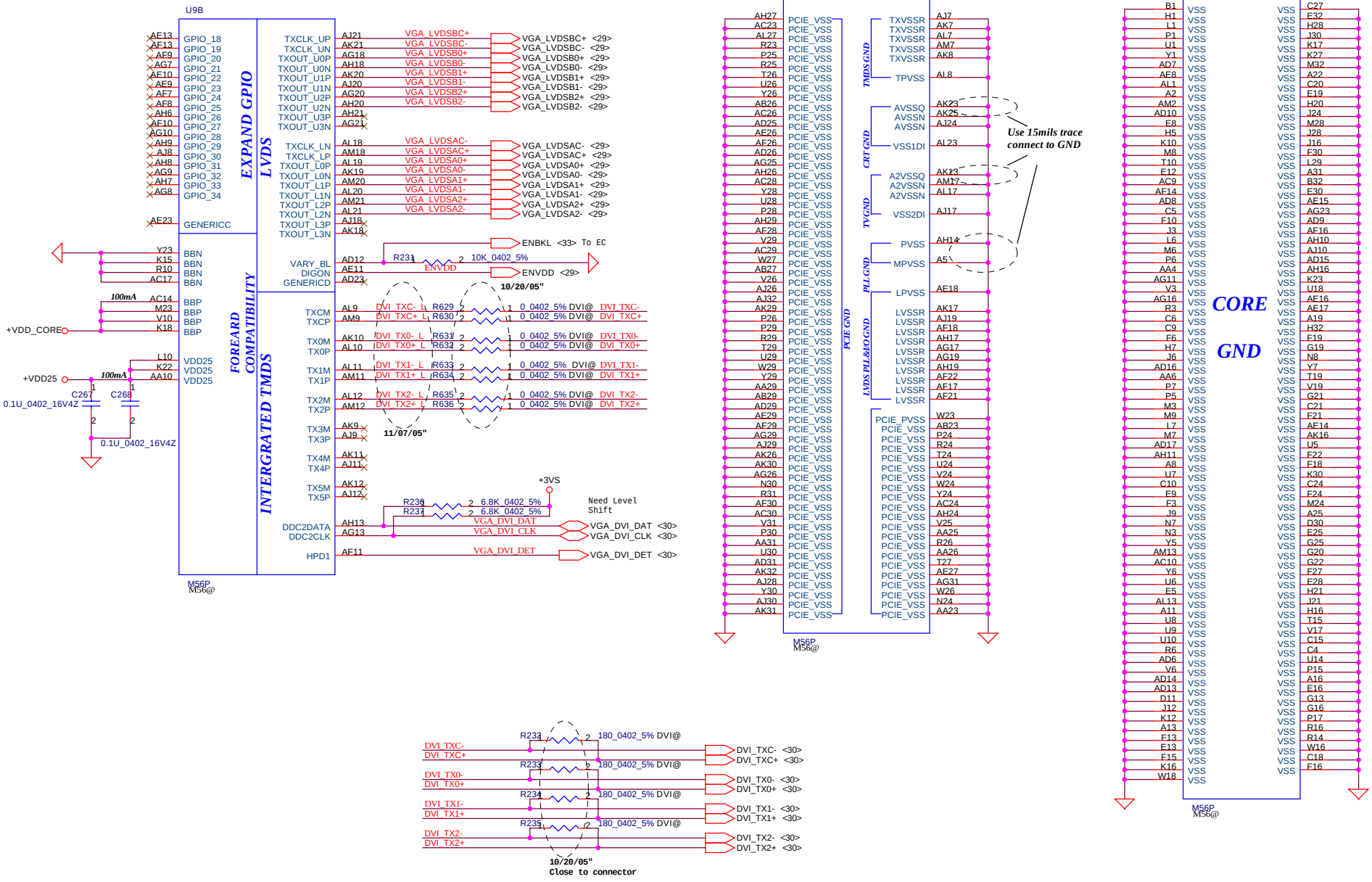

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Issued Date	2005/09/10	Deciphered Date	2006/09/10

Compal Electronics, Inc.

Title: **SCHEMATIC, M/B LA-3151P**

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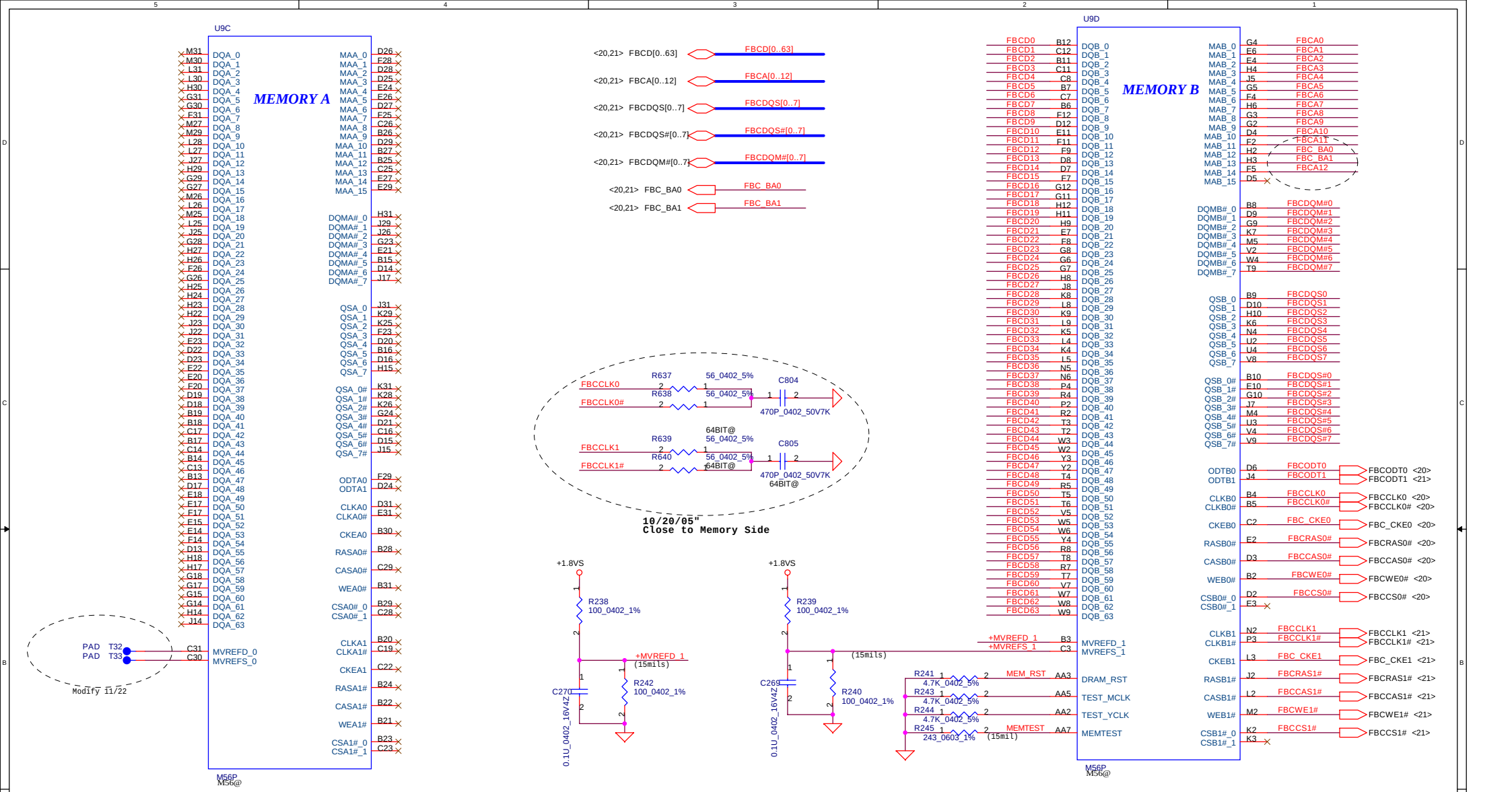

GDDR2

Security Classification	Compal Secret Data		
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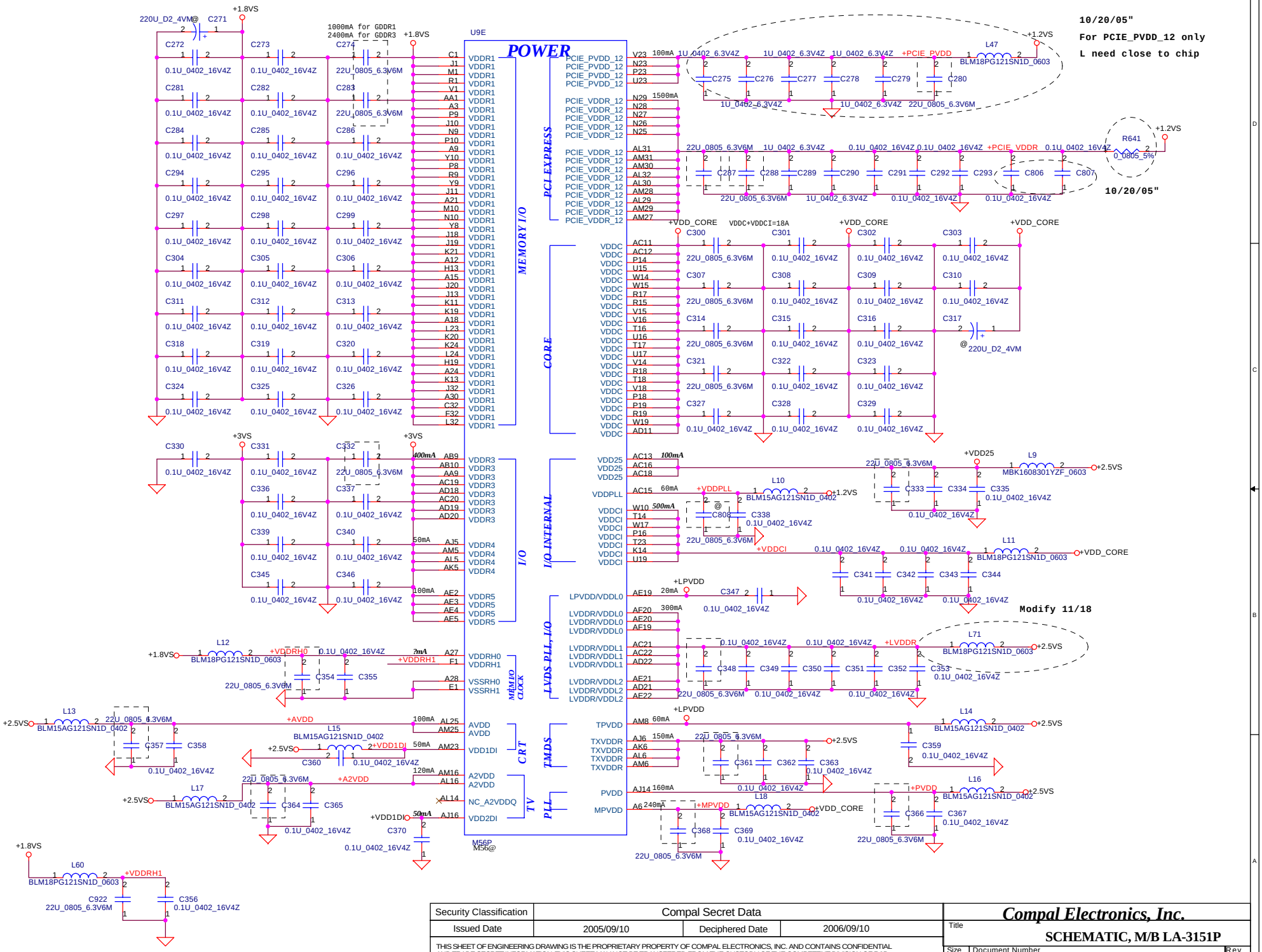

Security Classification	Compal Secret Data		
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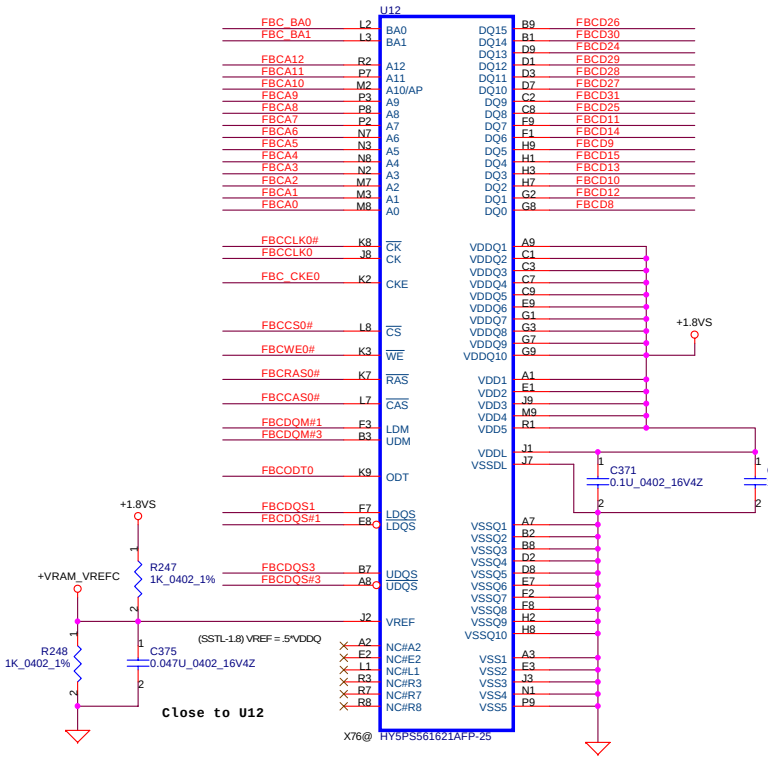
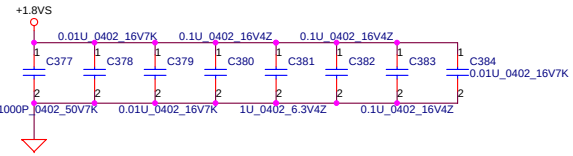
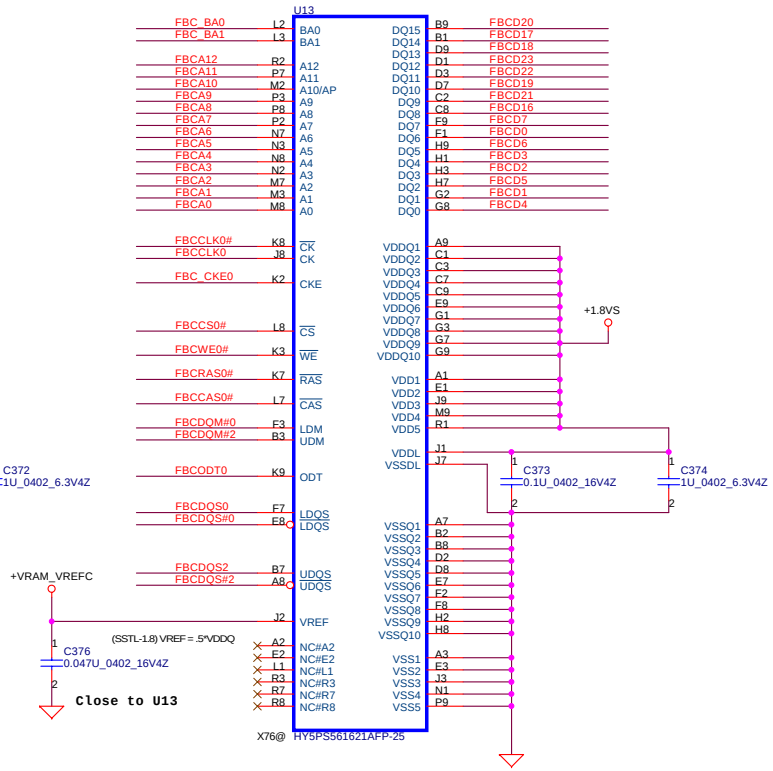
11/03/05' SWAP NET
11/04/05' SWAP NET
11/08/05' SWAP NET



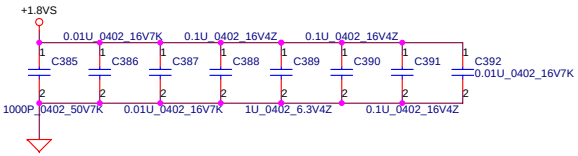
DDR2 BGA MEMORY

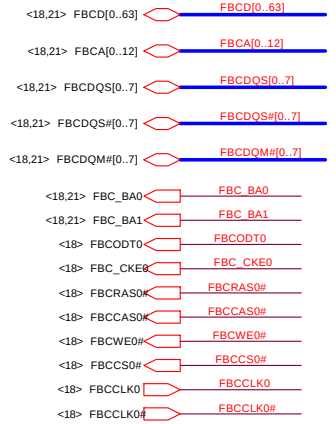


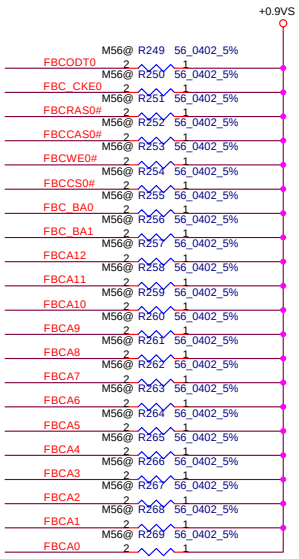
11/03/05' SWAP NET



DDR2 BGA MEMORY







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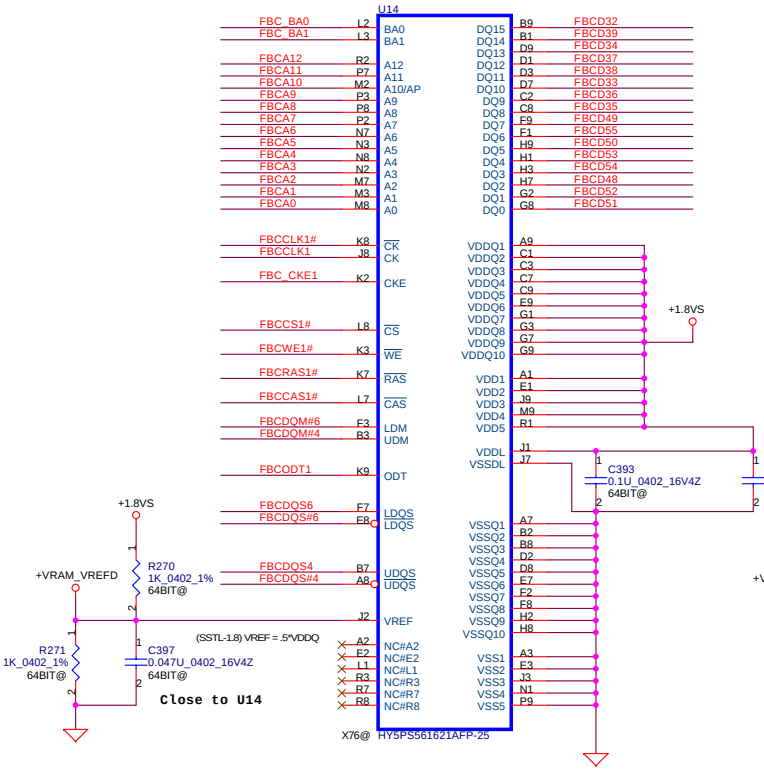
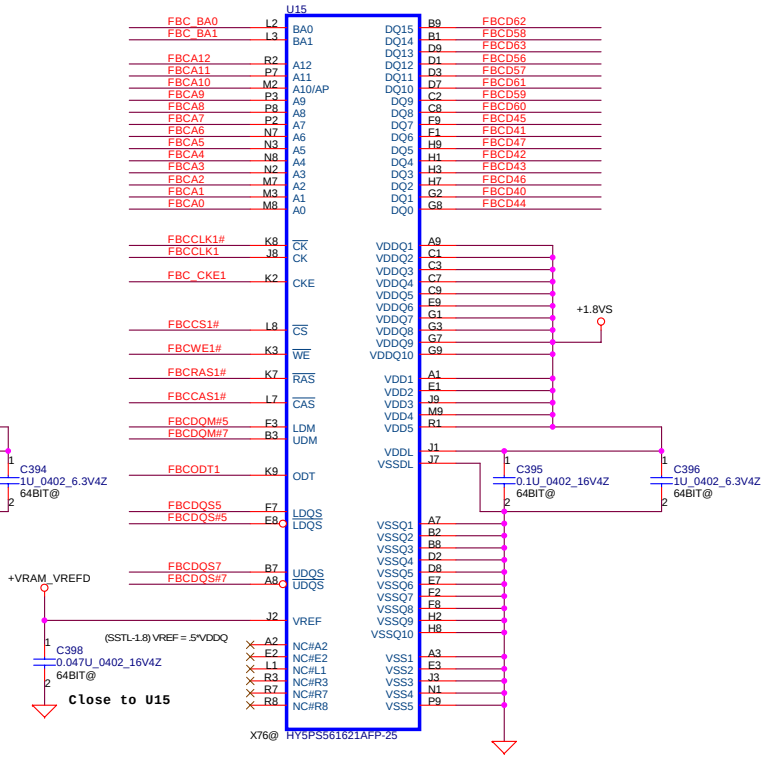
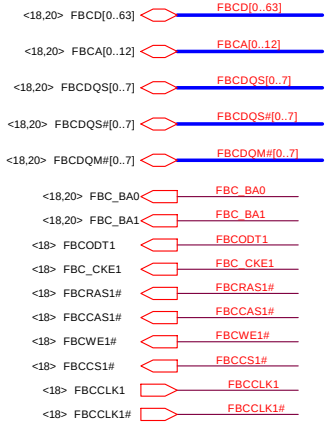
11/03/05' SWAP NET

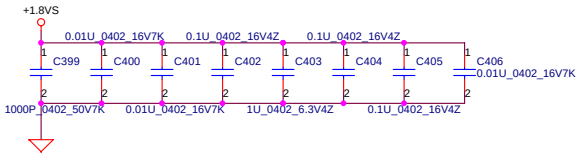


11/03/05' SWAP NET

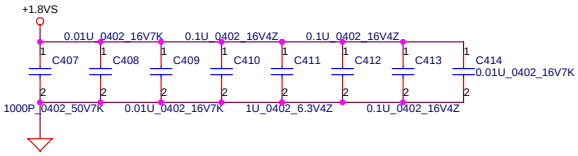


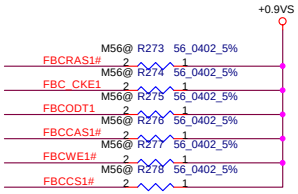


DDR2 BGA MEMORY



DDR2 BGA MEMORY





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Issued Date	2005/06/20	Deciphered Date	2006/06/20

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Title: SCHEMATIC, M/B LA-3151P

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

FOR SB600 VCC_SB= 1.2V
FOR SB460 VCC_SB= 1.8V

R294 CALRP: SB600=562R 1%, SB460=150R 1%
R295 CALRN: SB600=2.05K 1%, SB460=150R 1%
R296 CALRN: SB600=0R 1%, SB460=4.12K 1%

C608 AND C609 CLOSE TO U600.U29

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

FOR SB600, CONNECT TO CPU_PG/LDT_PG
FOR SB460, CONNECT TO SSMUXSEL/GPIO0

FOR SB460, THIS BALL IS LDT_RST# ONLY

SB460 ONLY

LPC PULL UPS

SB460
Part 1 of 4

218S4RASA11GS SB460_BGA549

EMI 11/2 Modify

RTC Battery

@JUMP_43X39
Please Closed RAM Door

Modify 11/07

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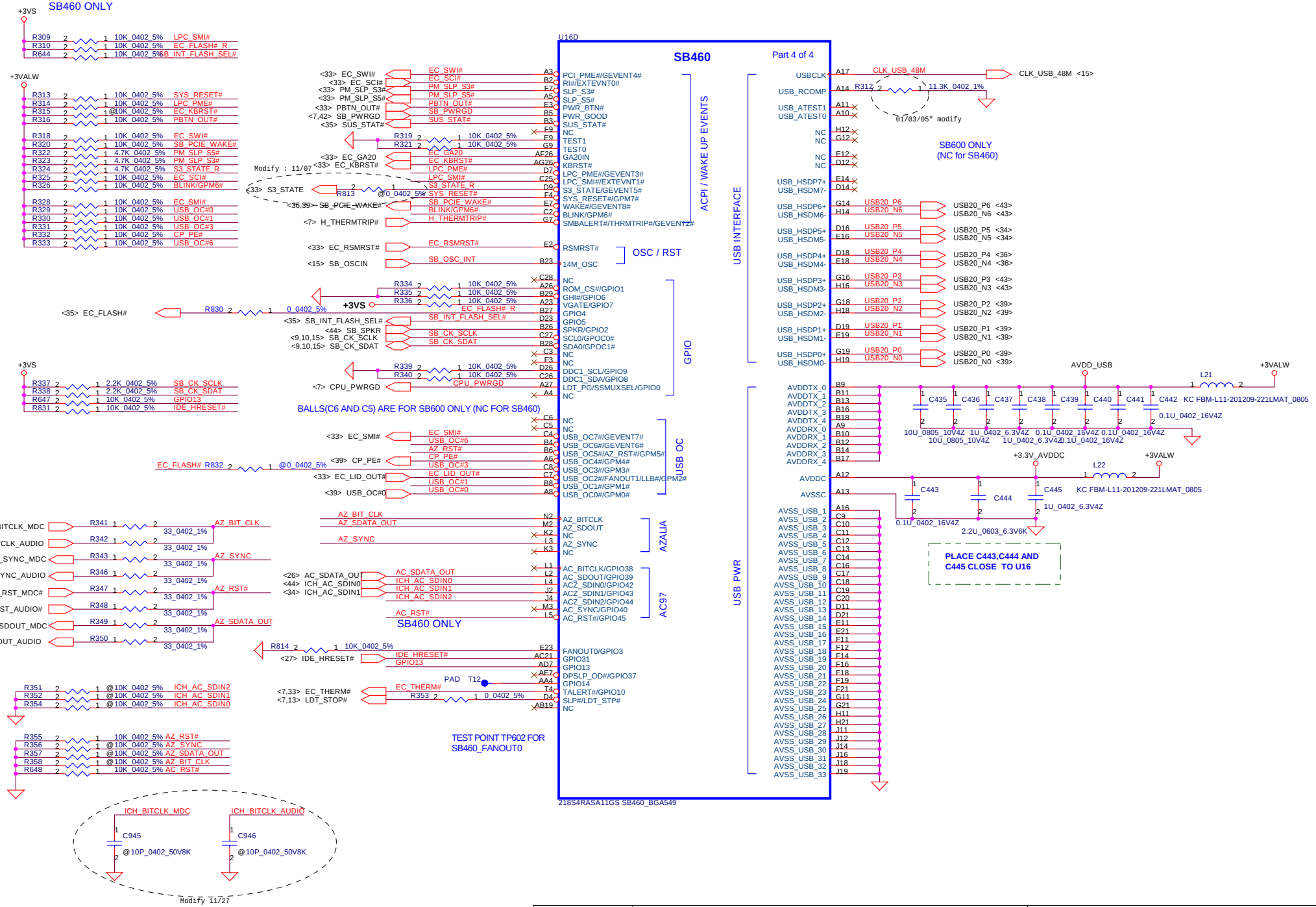

Security Classification	Compal Secret Data		
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Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

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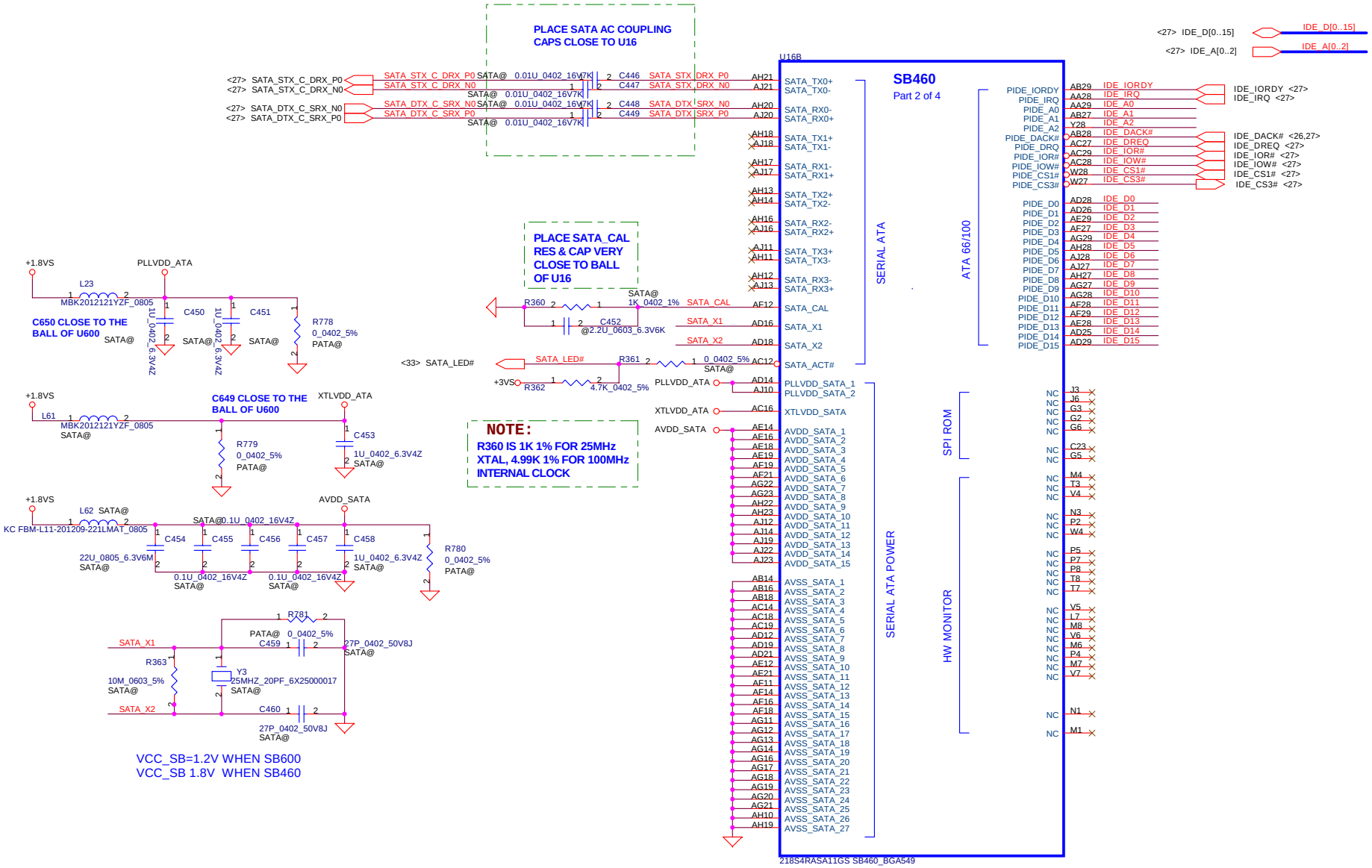

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

Title: SCHEMATIC, M/B LA-3151P

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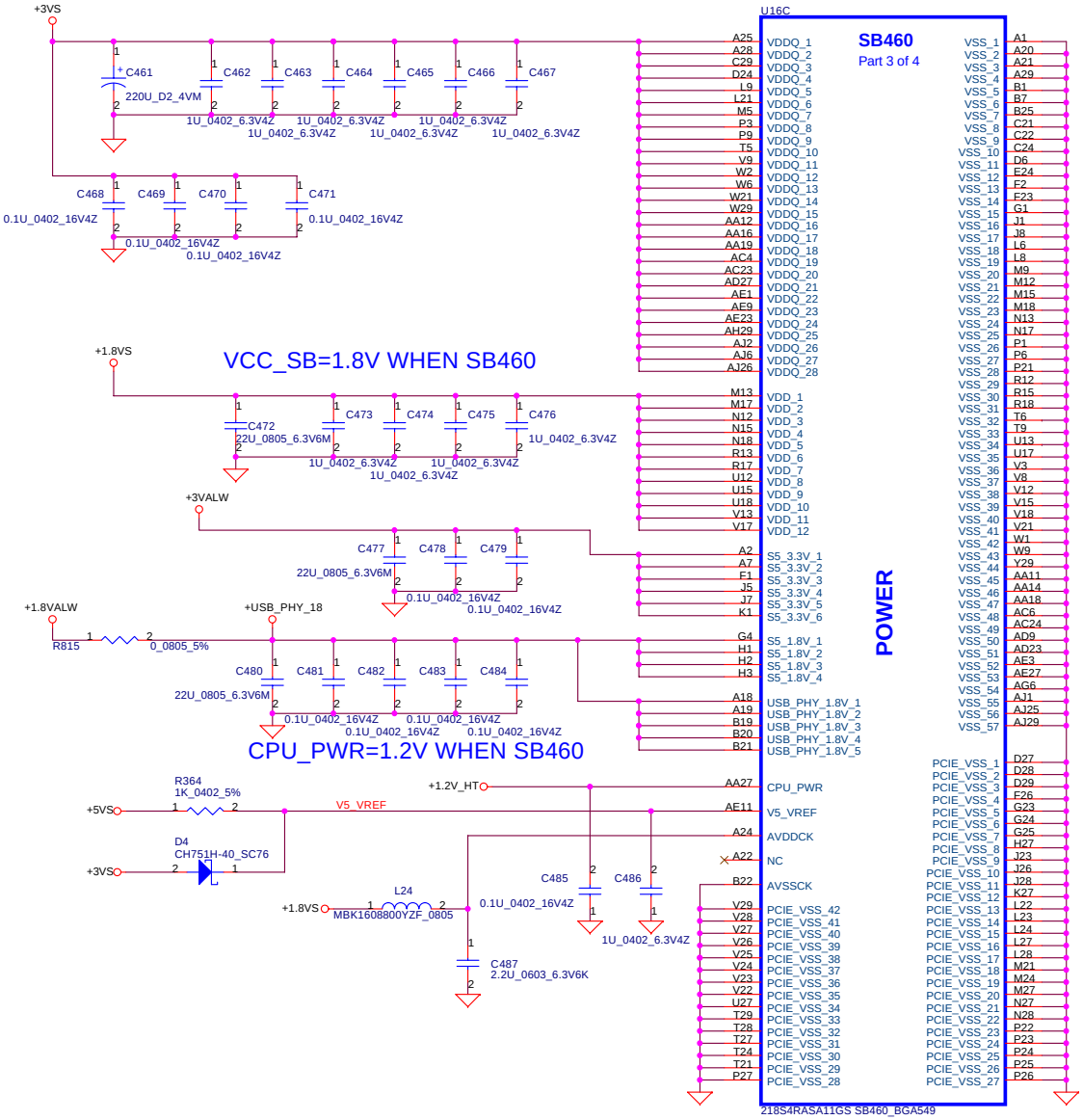

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

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Title: SCHEMATIC, M/B LA-3151P

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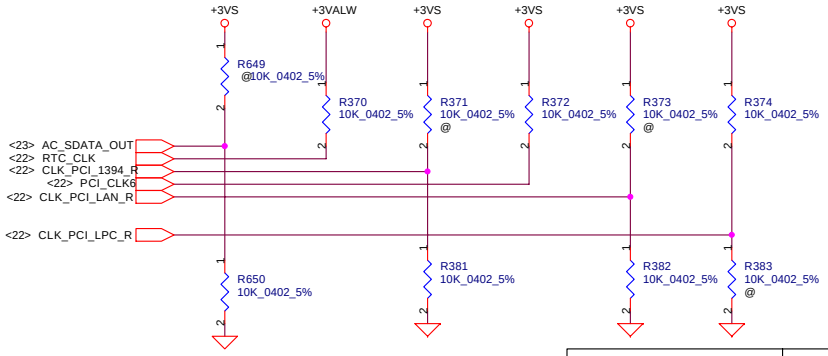
REQUIRED STRAPS

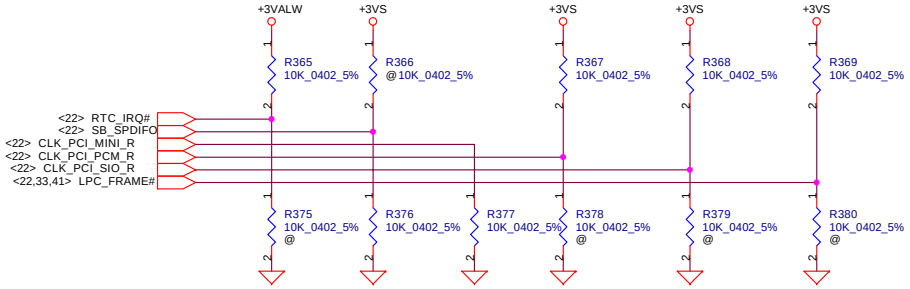
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



	AC_SDATA_OUT	RTC_CLK	PCI_CLK4 CLK_PCI_1394	PCI_CLK6	SB600 PCI_CLK0 PCI_CLK1 CLK_PCI_LAN CLK_PCI_LPC	SB460 PCI_CLK0 PCI_CLK1 CLK_PCI_LAN CLK_PCI_LPC
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM DEFAULT L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

NOTE: R365 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB460 TO KEEP THE INPUT FROM FLOATING.

SB460 ONLY

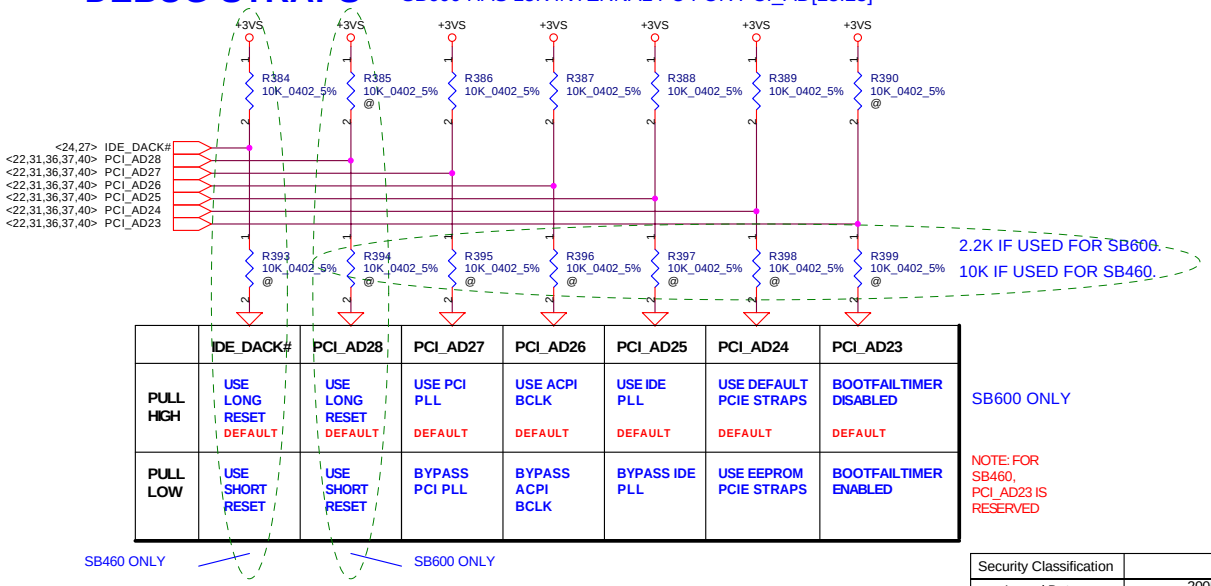


	ACPWRON RTC_IRQ#	SPDIF_OUT SB_SPDIFO	PCI_CLK2 CLK_PCI_MINI	PCI_CLK3 CLK_PCI_PCM	PCI_CLK5 CLK_PCI_SIO	LFRAME# LPC_FRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB460 ONLY — SB600 ONLY

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

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Title: SCHEMATIC, M/B LA-3151P

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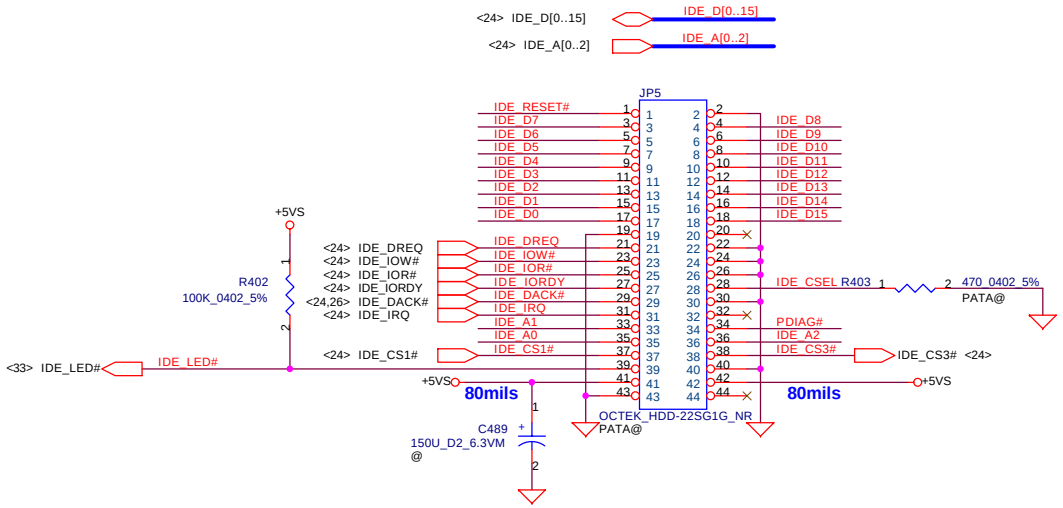
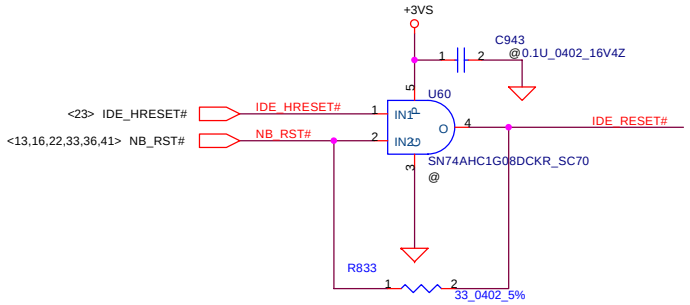
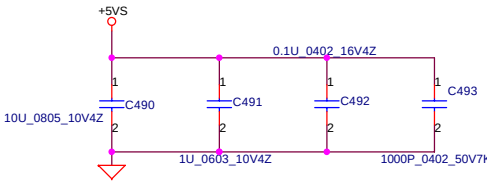
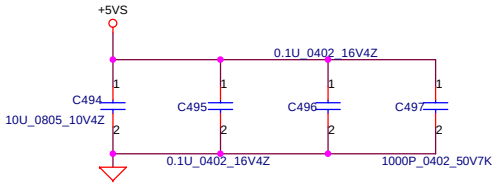
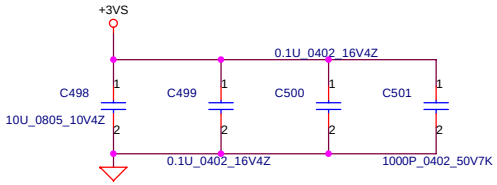
HDD CONN



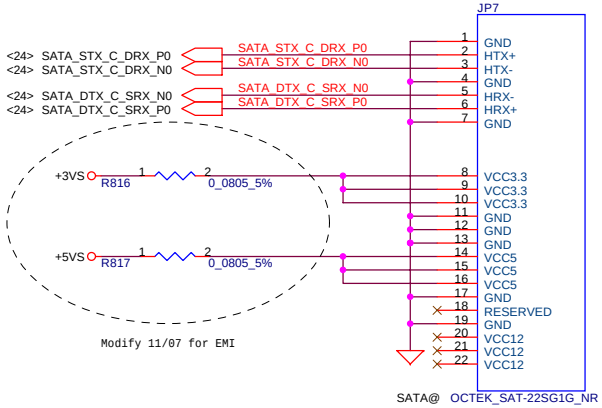






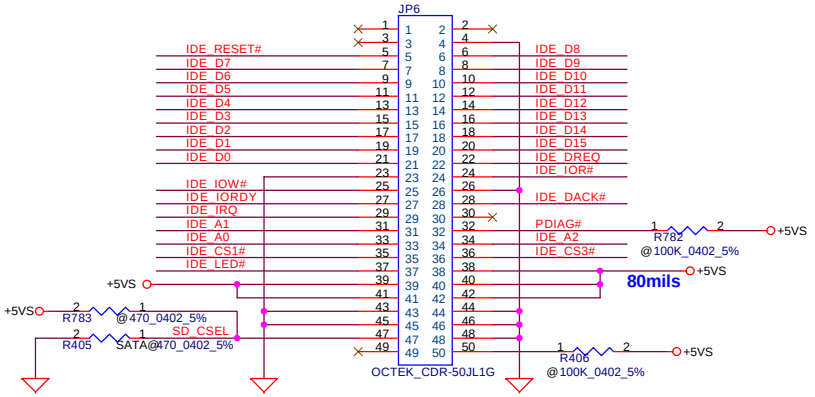


SATA HDD Conn.



(NEW)

CDROM CONN



IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

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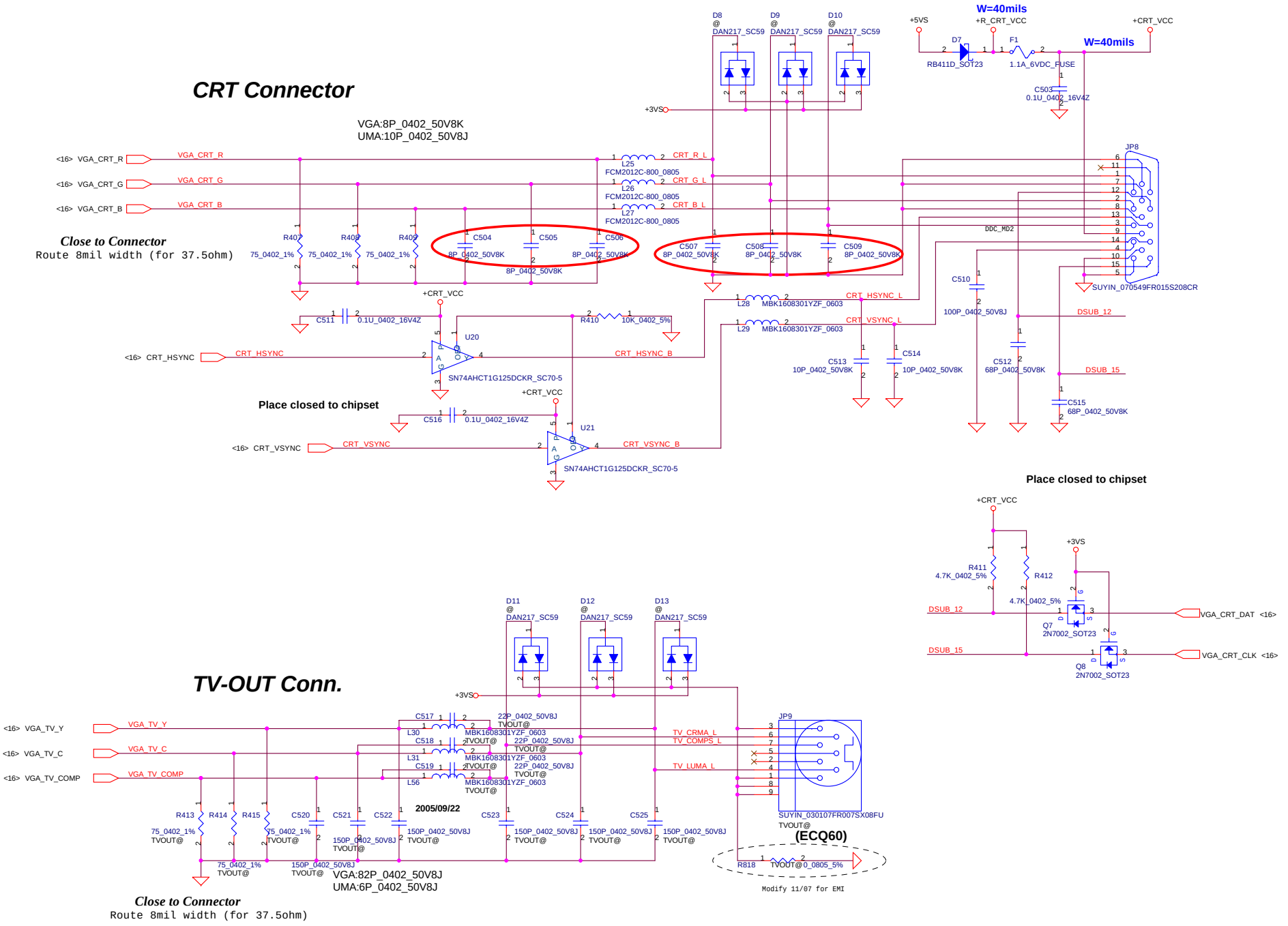

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

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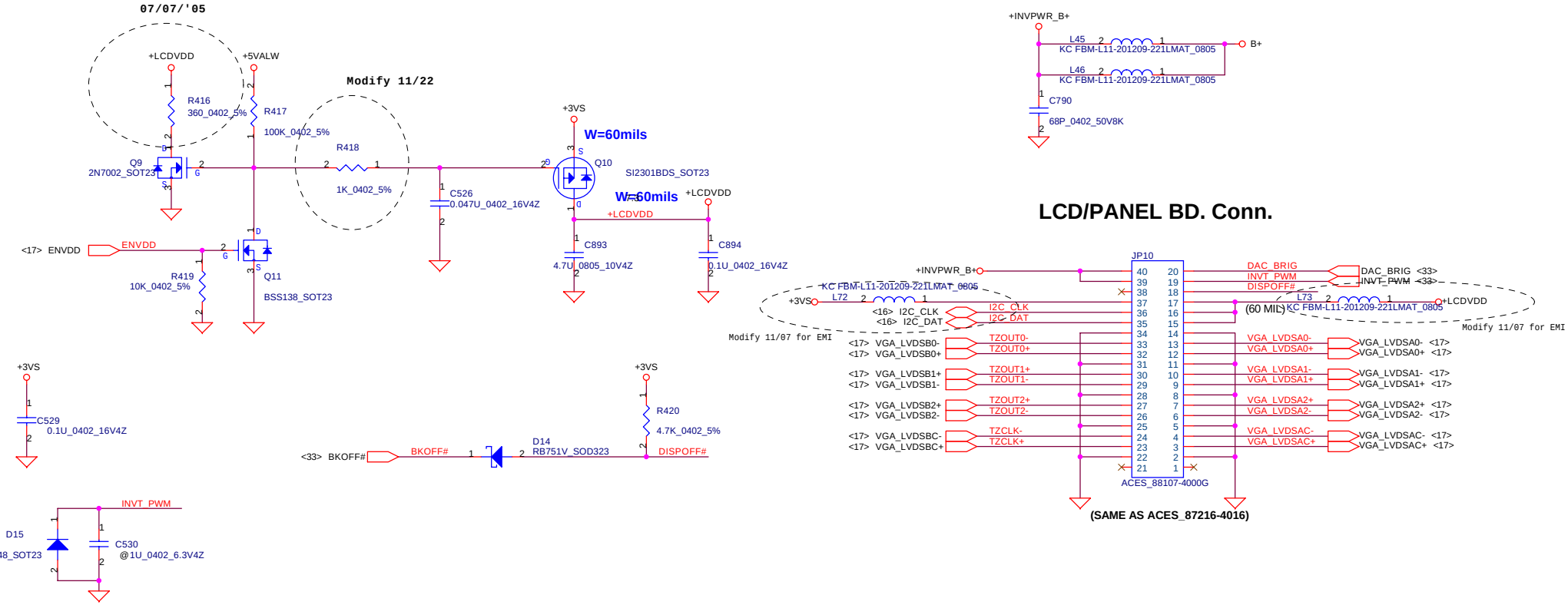
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

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Title: SCHEMATIC, M/B LA-3151P

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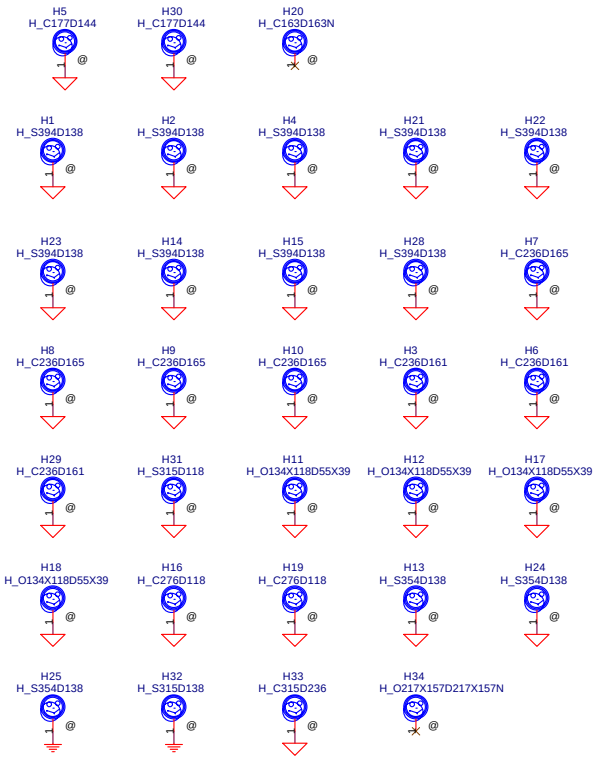

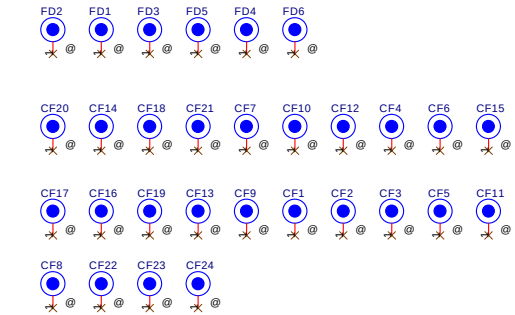

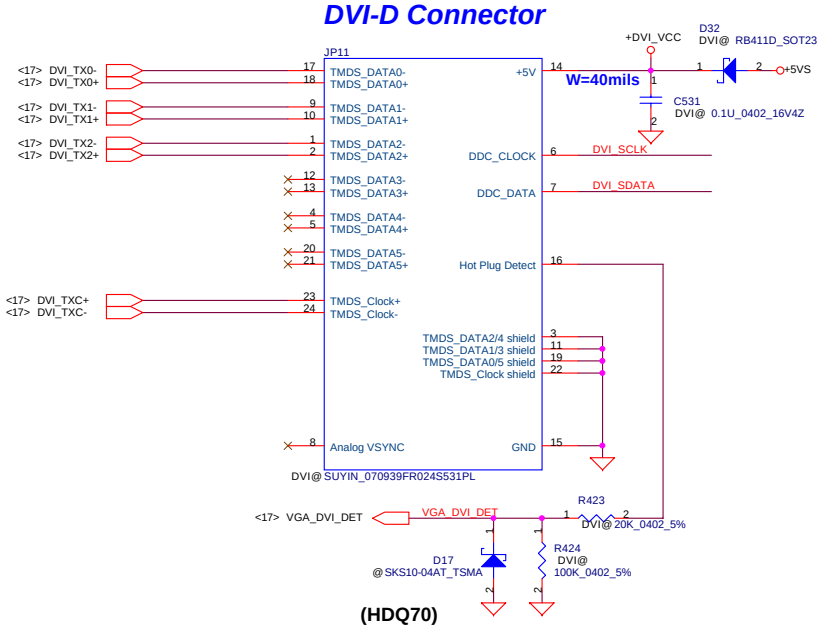

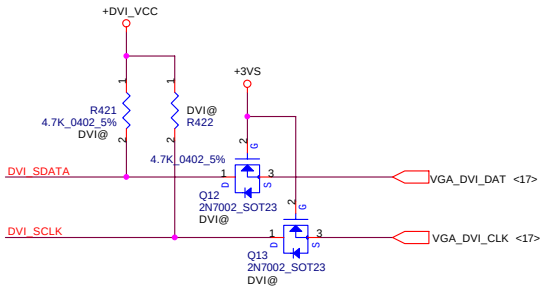

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

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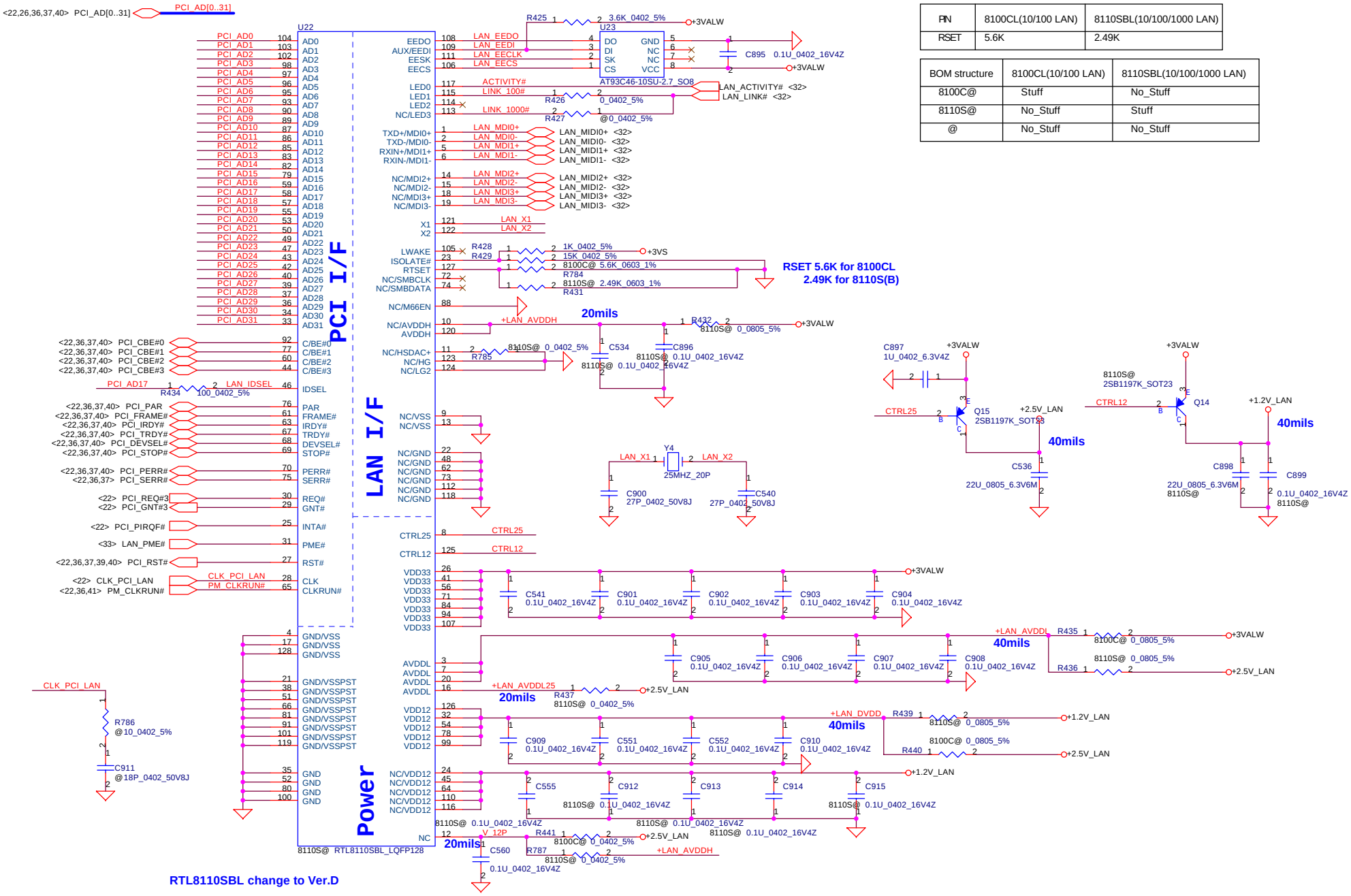

PIN	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
RSET	5.6K	2.49K

BOM structure	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
8100C@	Stuff	No_Stuff
8110S@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

Security Classification	Compal Secret Data		
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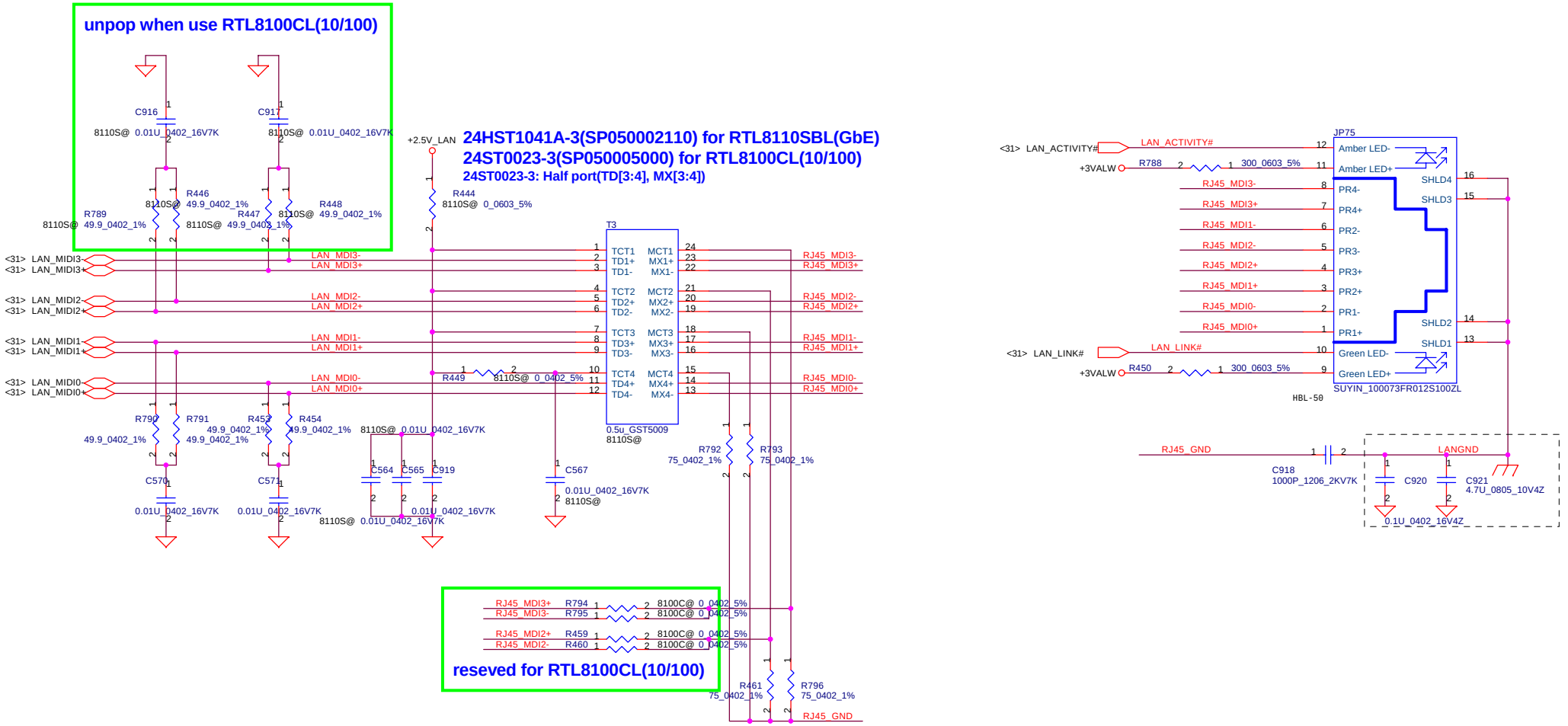
LAN RTL8110SBL/RTL8100CL



Security Classification	Compal Secret Data		
Issued Date	2005/07/29	Deciphered Date	2006/07/29

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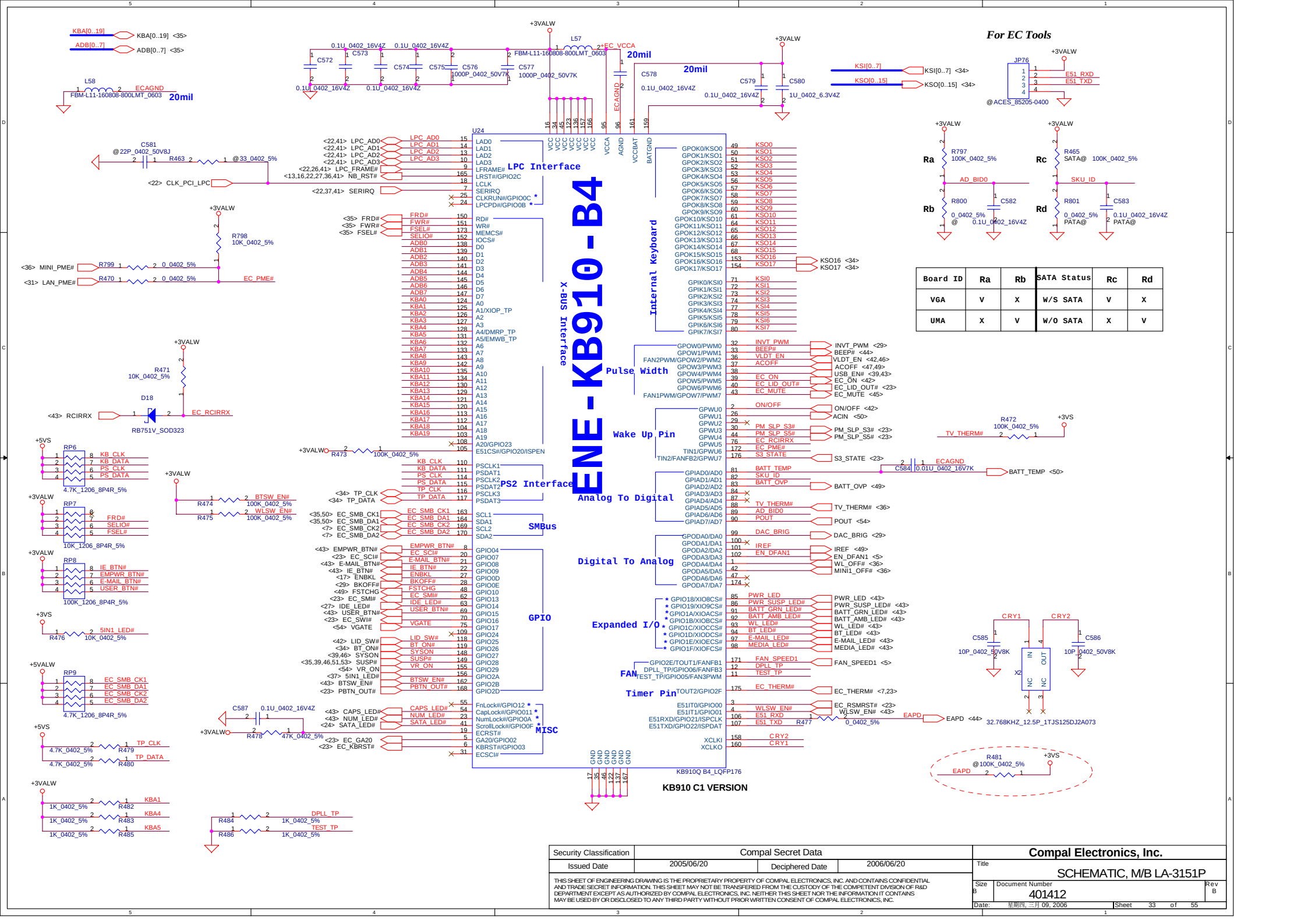
ENE-KB910-B4
U24
LPC Interface
X-BUS Interface
PS2 Interface
SMBus
GPIO
MISC
Internal Keyboard
Pulse Width
Wake Up Pin
Analog To Digital
Digital To Analog
Expanded I/O
FAN
Timer Pin
KB910Q B4_LQFP176
KB910 C1 VERSION
For EC Tools
Board ID | Ra | Rb | SATA Status | Rc | Rd
VGA | V | X | W/S SATA | V | X
UMA | X | V | W/O SATA | X | V
Security Classification | Compal Secret Data
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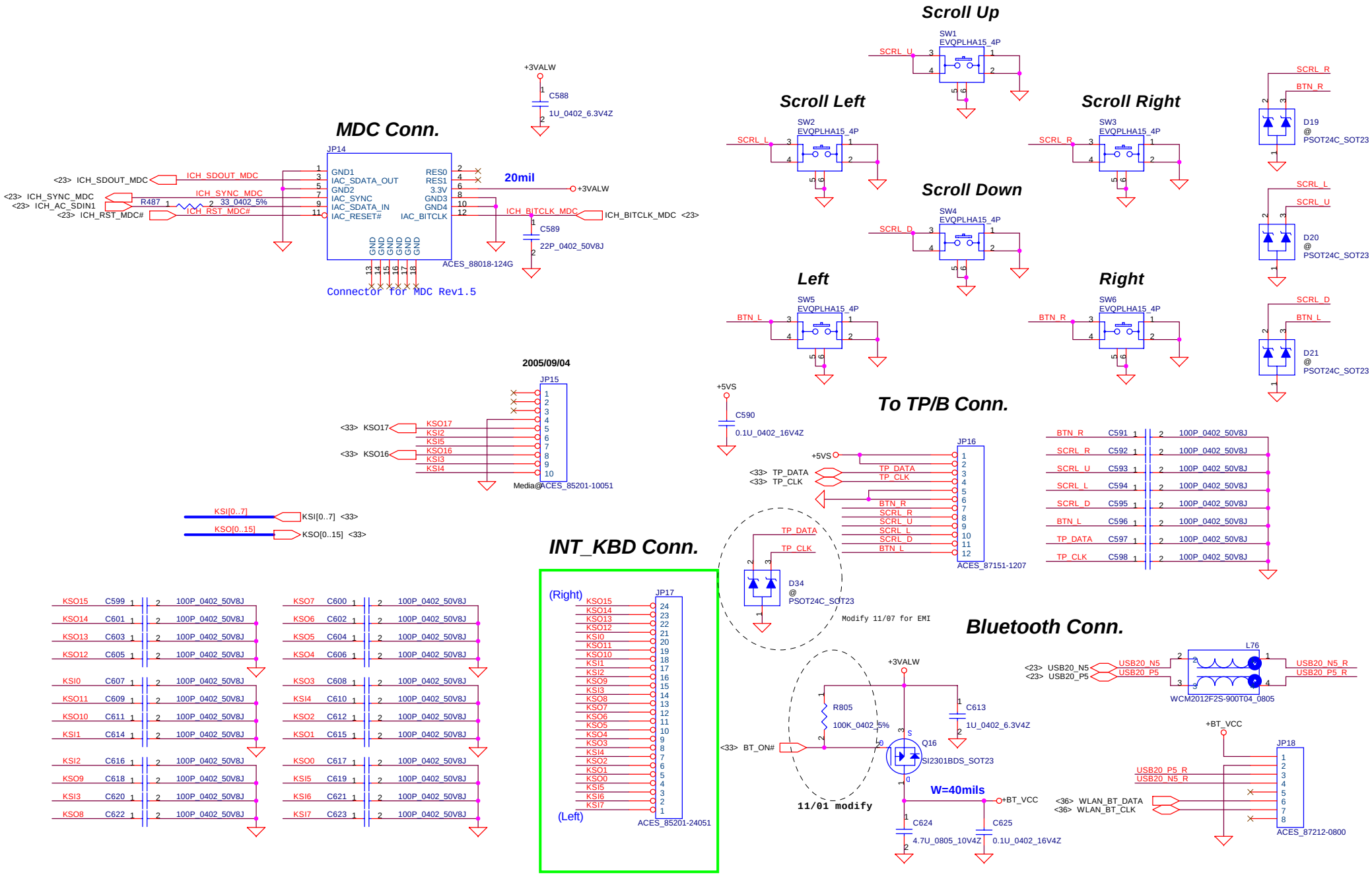

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

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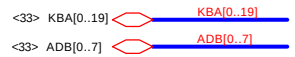

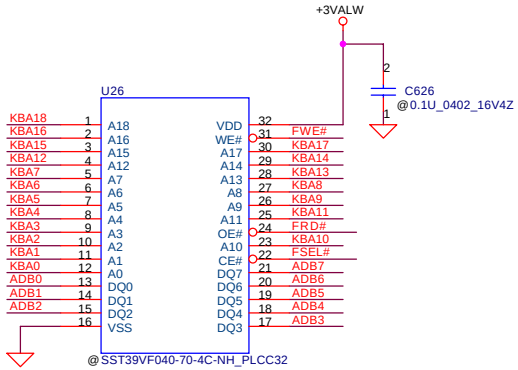

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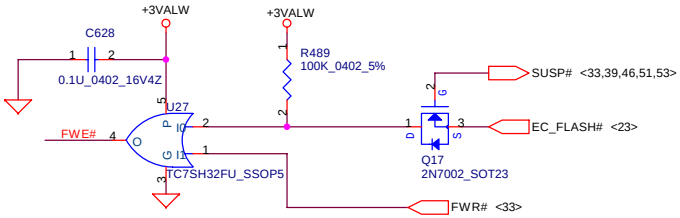
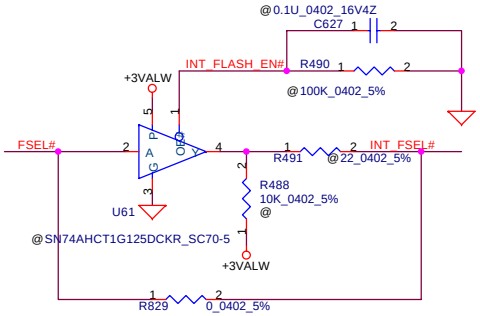
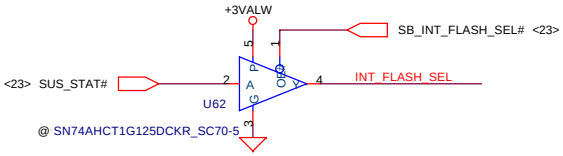
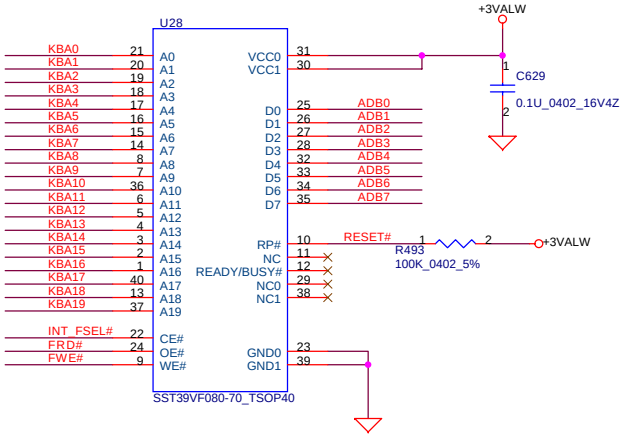




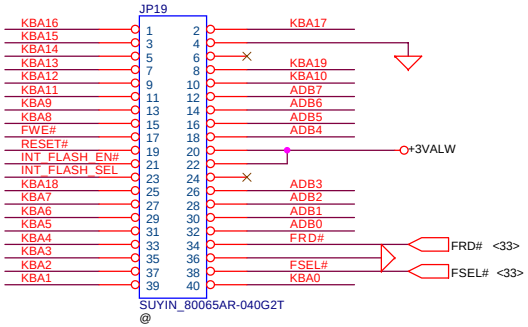
FOR DEBUG ONLY

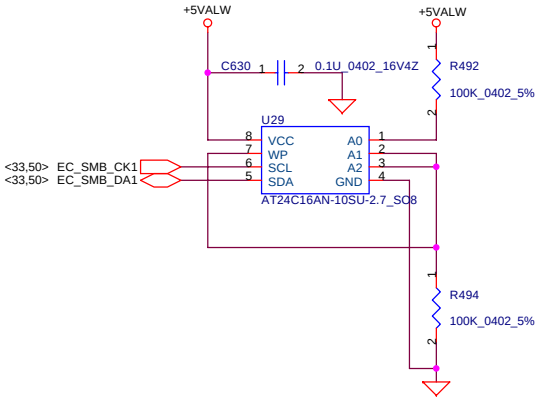


1MB Flash ROM



1MB Flash ROM





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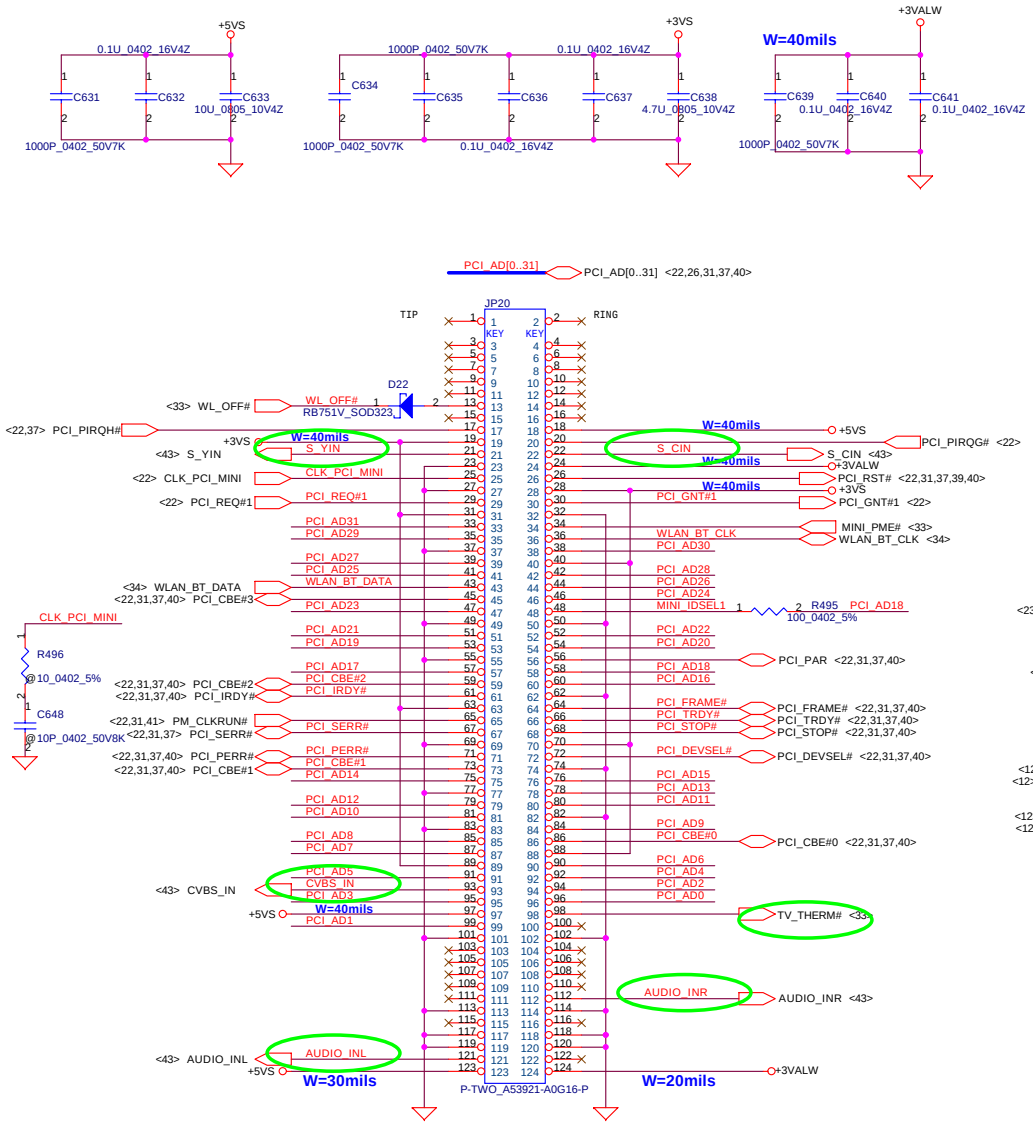

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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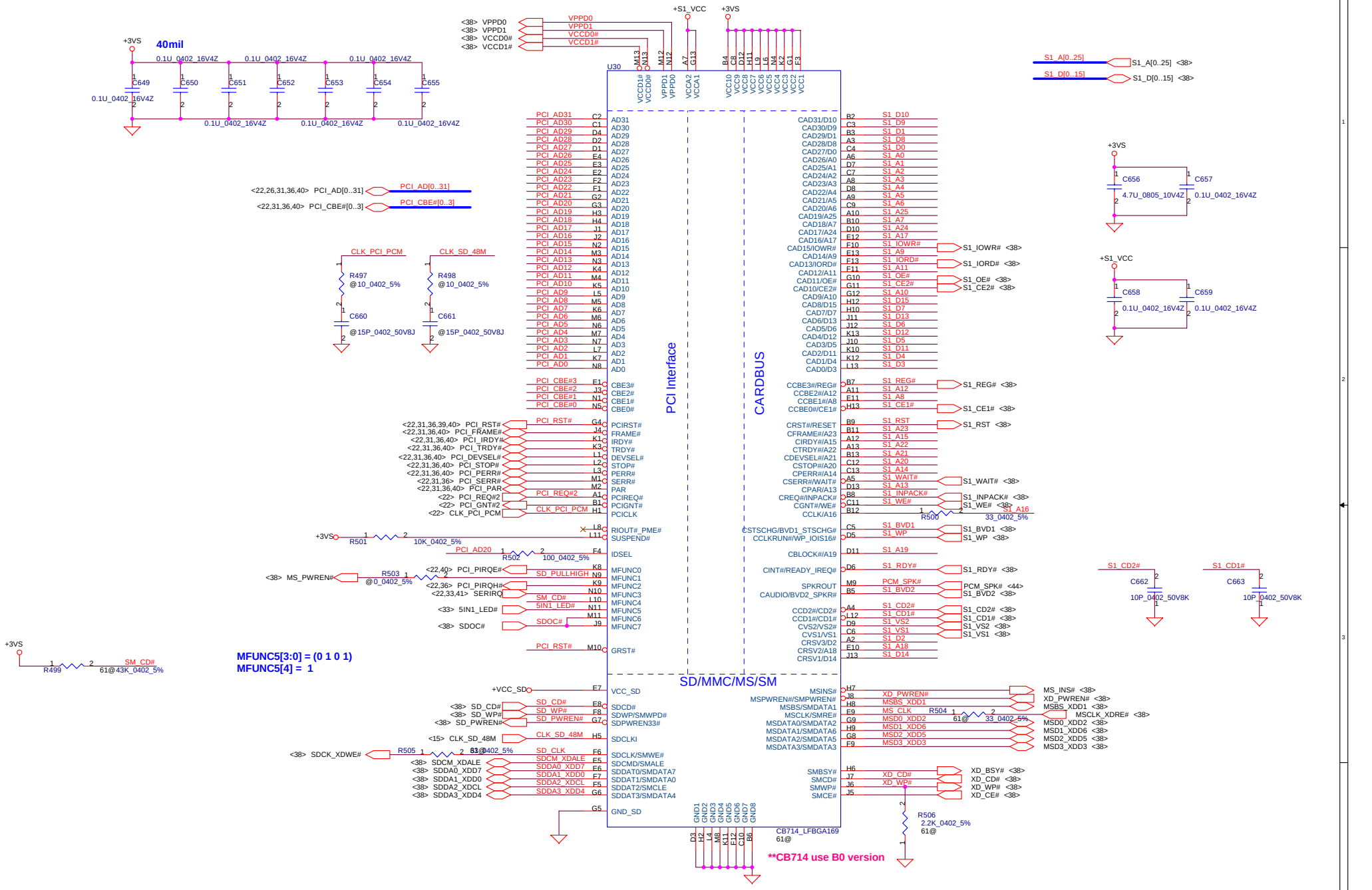

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Compal Electronics, Inc.

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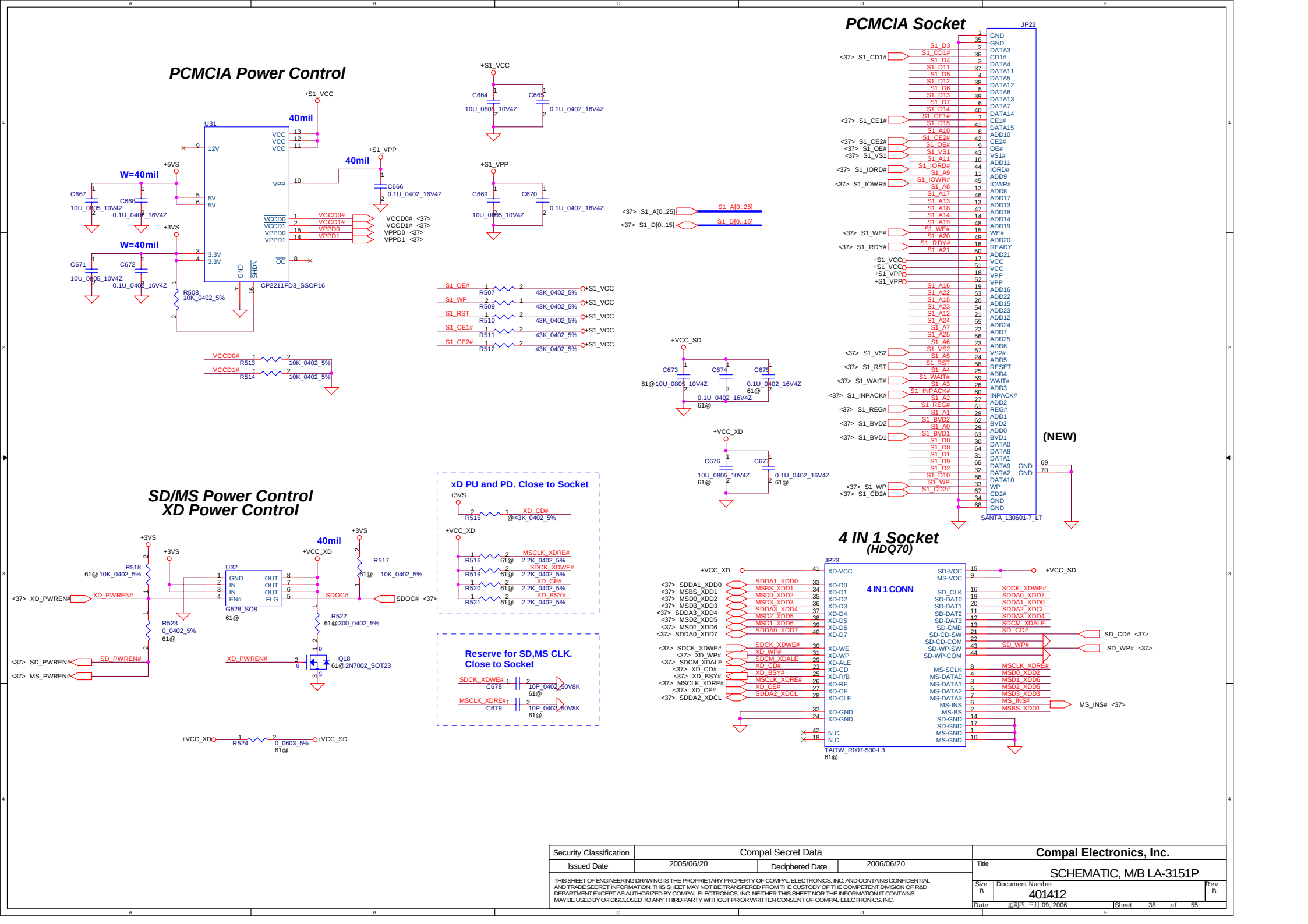

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Issued Date	2005/06/20	Deciphered Date	2006/06/20

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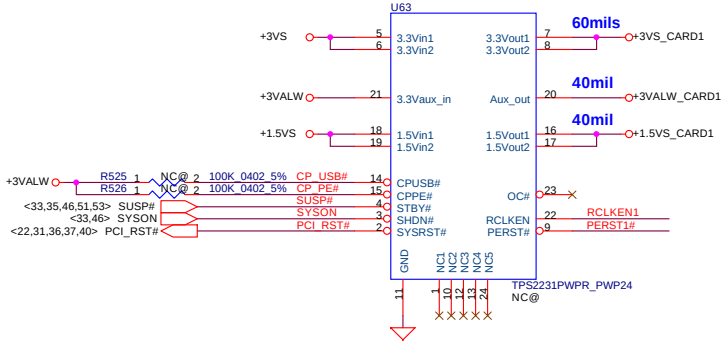
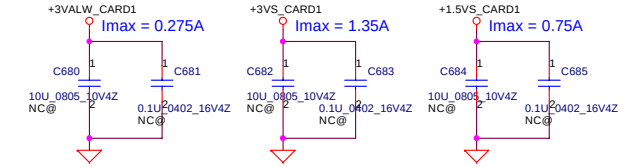
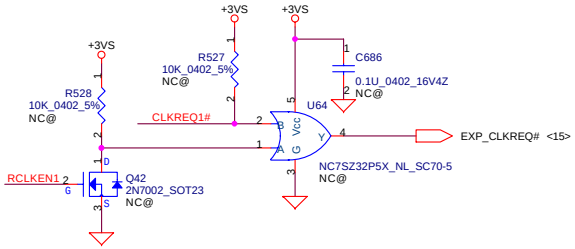
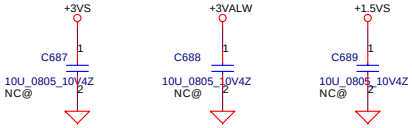
New Card Power Switch

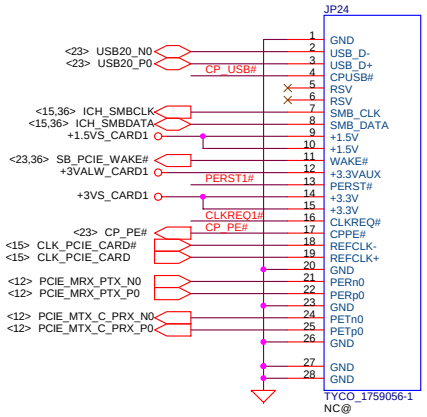








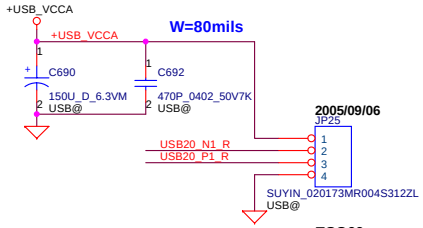
New Card Socket (Left)



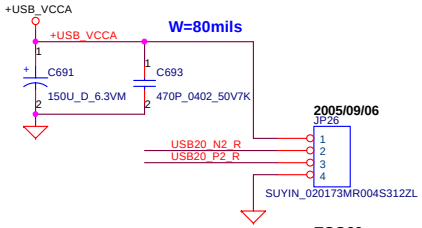
(NEW)

USB Component co-layout

USB CONN. 1 & 2



ECQ60



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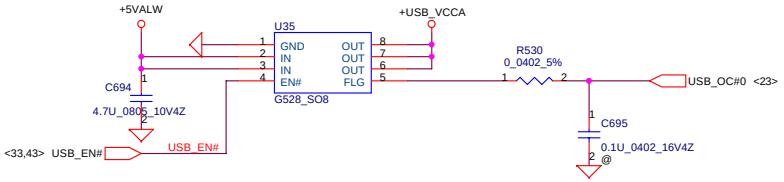

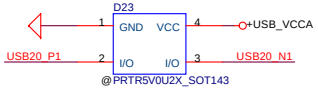

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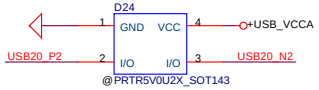

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Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

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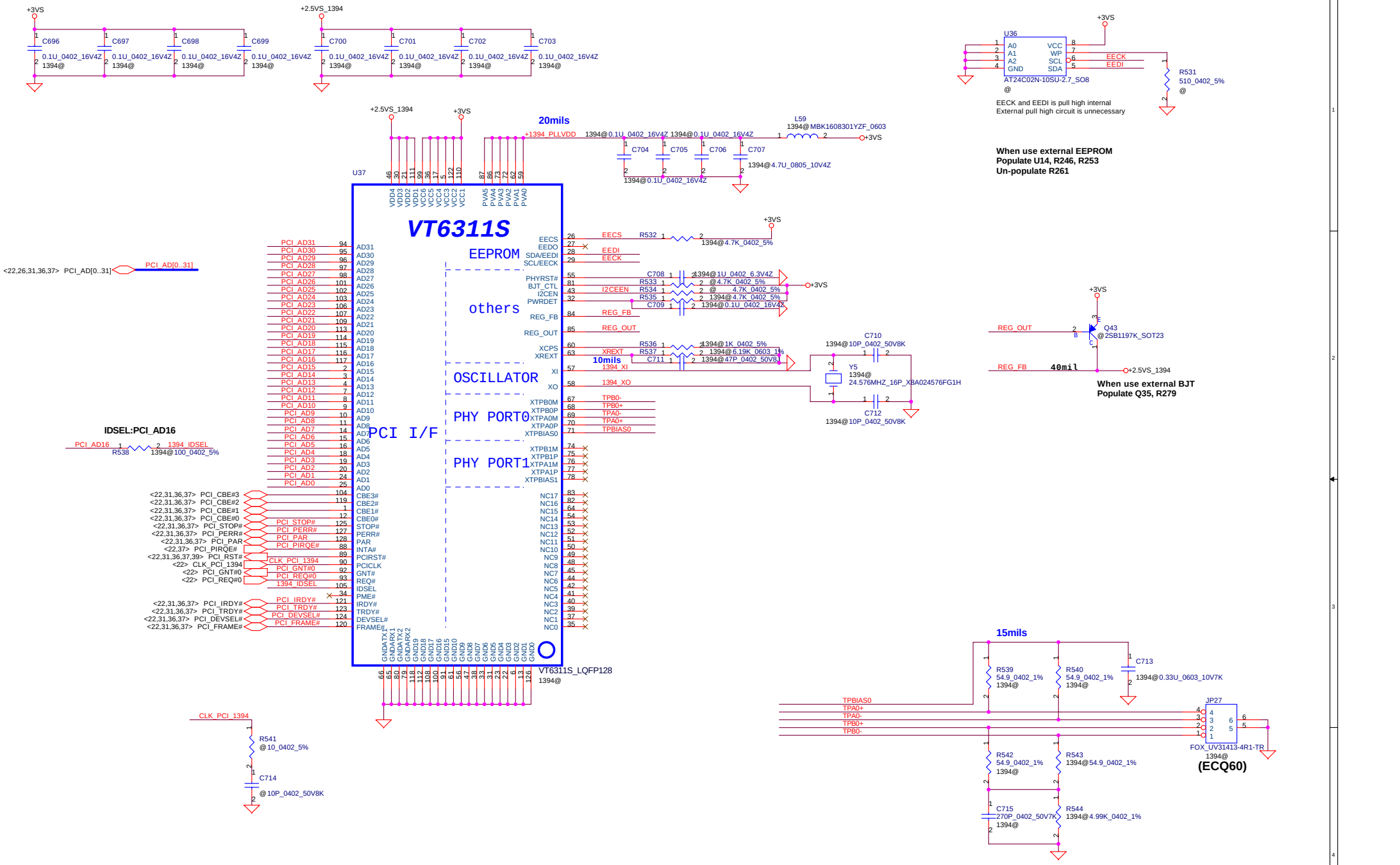

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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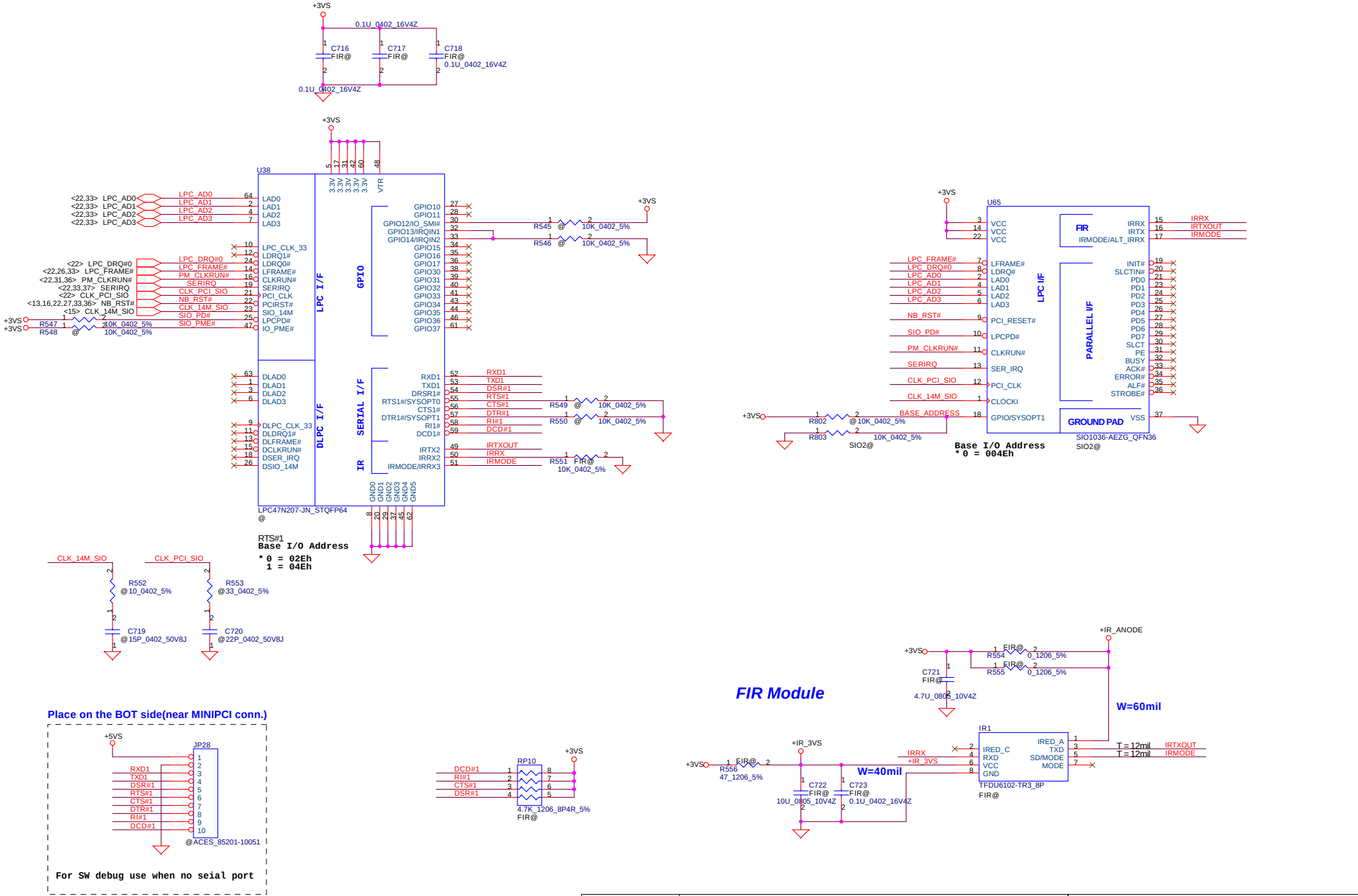
SUPER I/O SMsC LPC47N207



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

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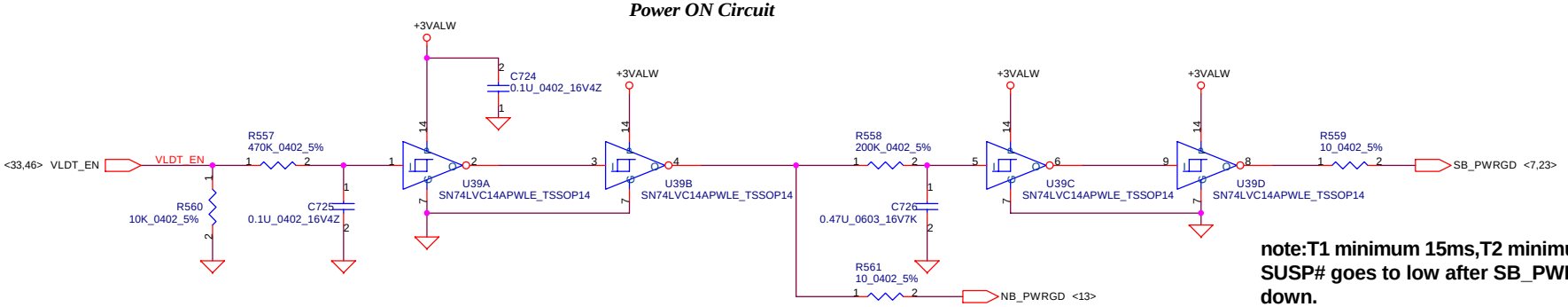
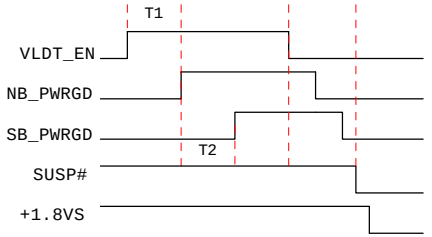
Power ON Circuit



note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



ON/OFF switch

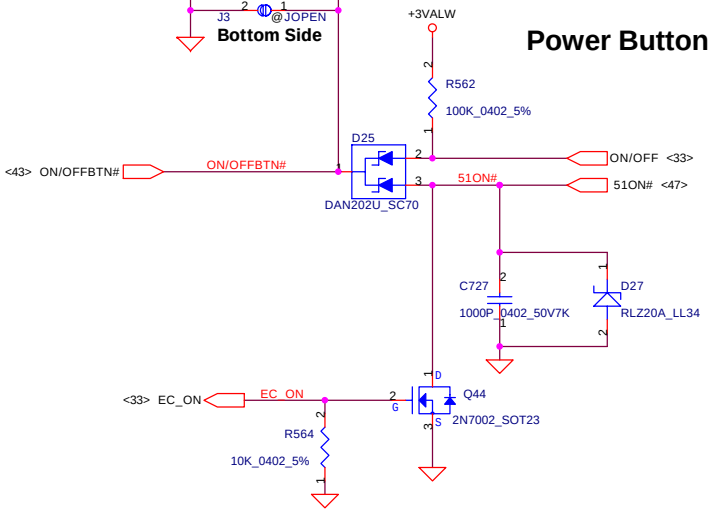
TOP Side

J2 @JOPEN

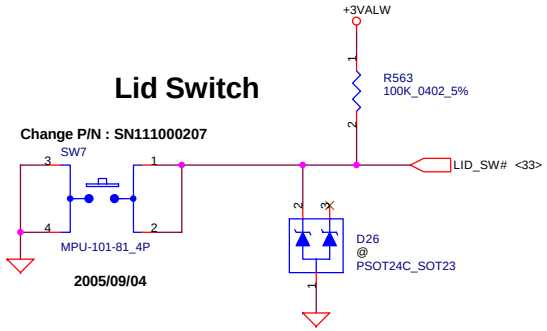
J3 @JOPEN

Bottom Side

Power Button



Lid Switch



Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

Compal Electronics, inc.

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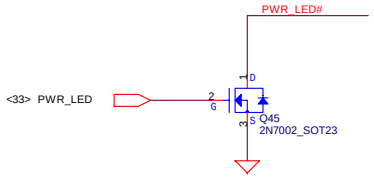

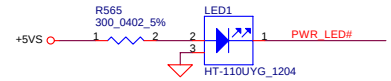

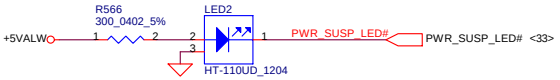

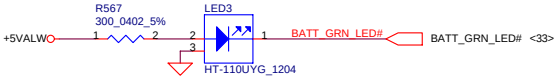

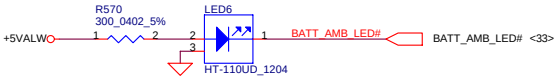

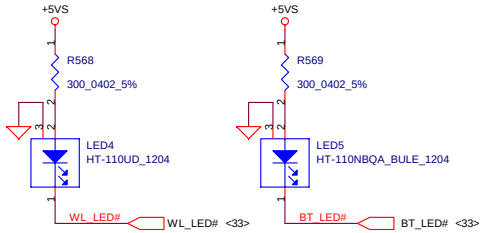

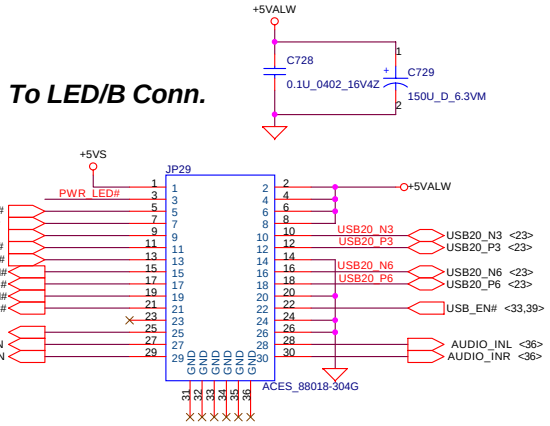

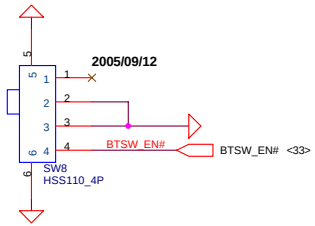

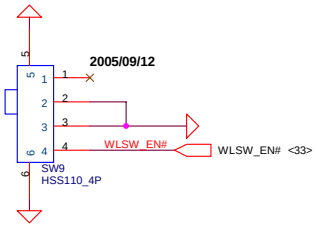

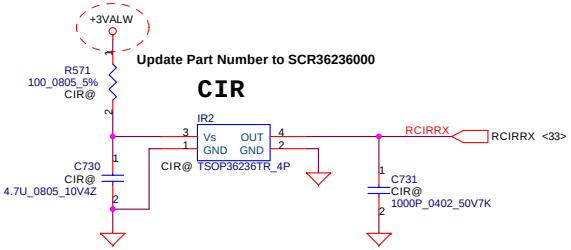

Geneva 2005/09/04 **Grapevine**

	KSO16	KSO17
KSI0	VOL_UP	LEFT
KSI1	RIGHT	VOL_DOWN
KSI2	PLAY	ENTER
KSI3	STOP	
KSI4	NEXT	
KSI5	REV	
KSI6		RECORD

	KSO16	KSO17
KSI2	PLAY	
KSI3	STOP	VOL_UP
KSI4	NEXT	VOL_DOWN
KSI5	REV	ARCADE_TV

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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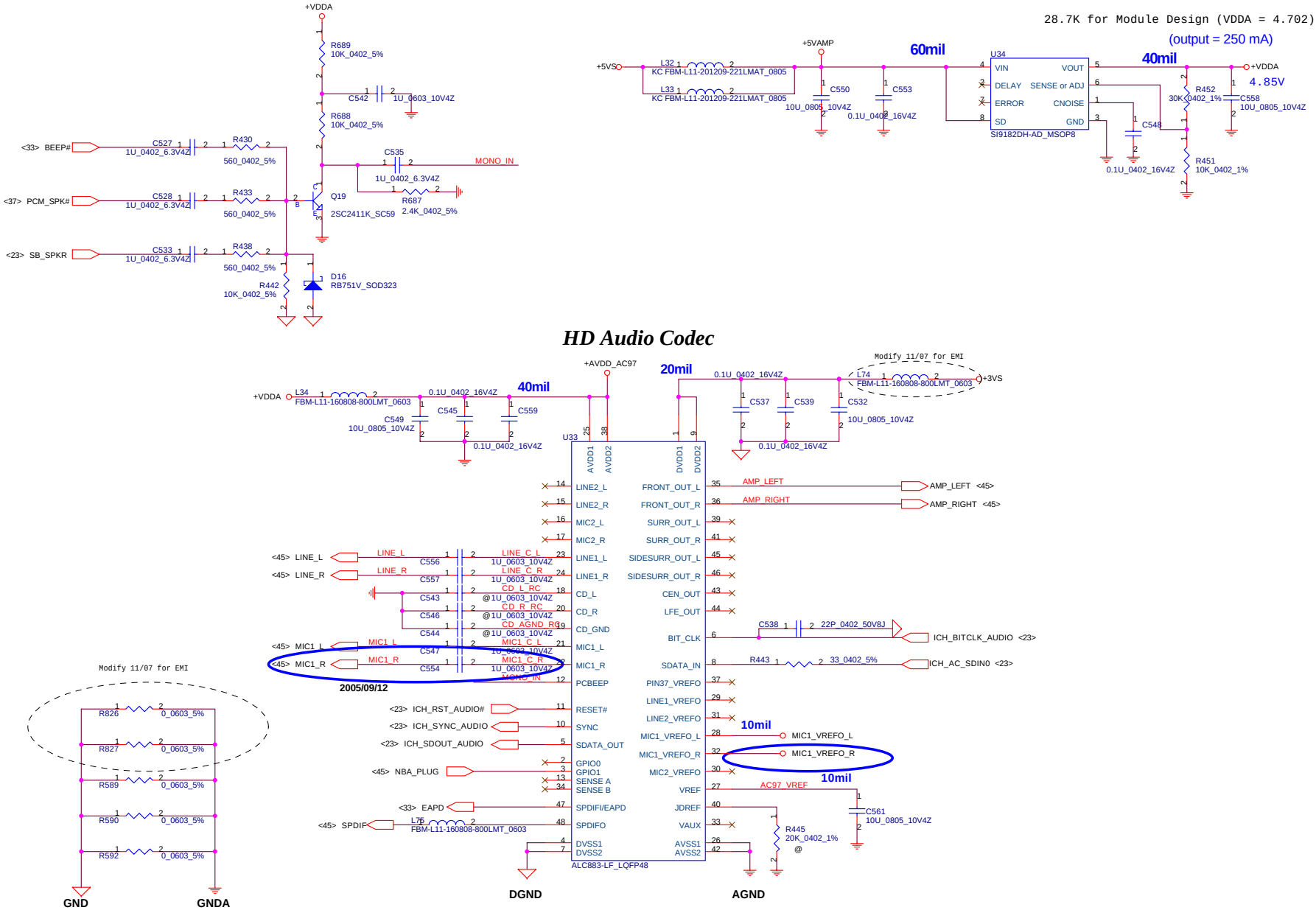

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

Size	Document Number	Rev
Custom	401412	B

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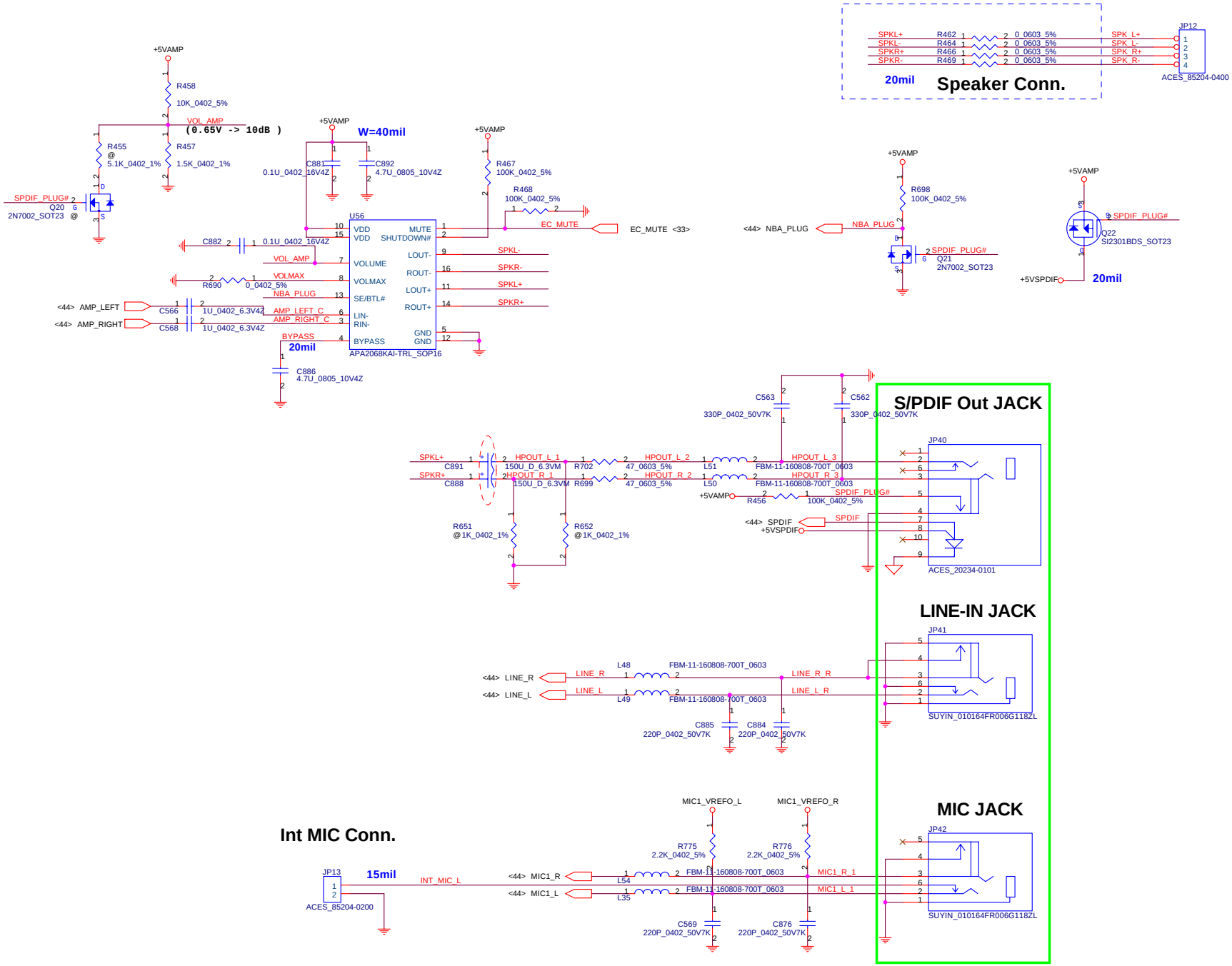

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

Size	Document Number	Rev
Custom	401412	B

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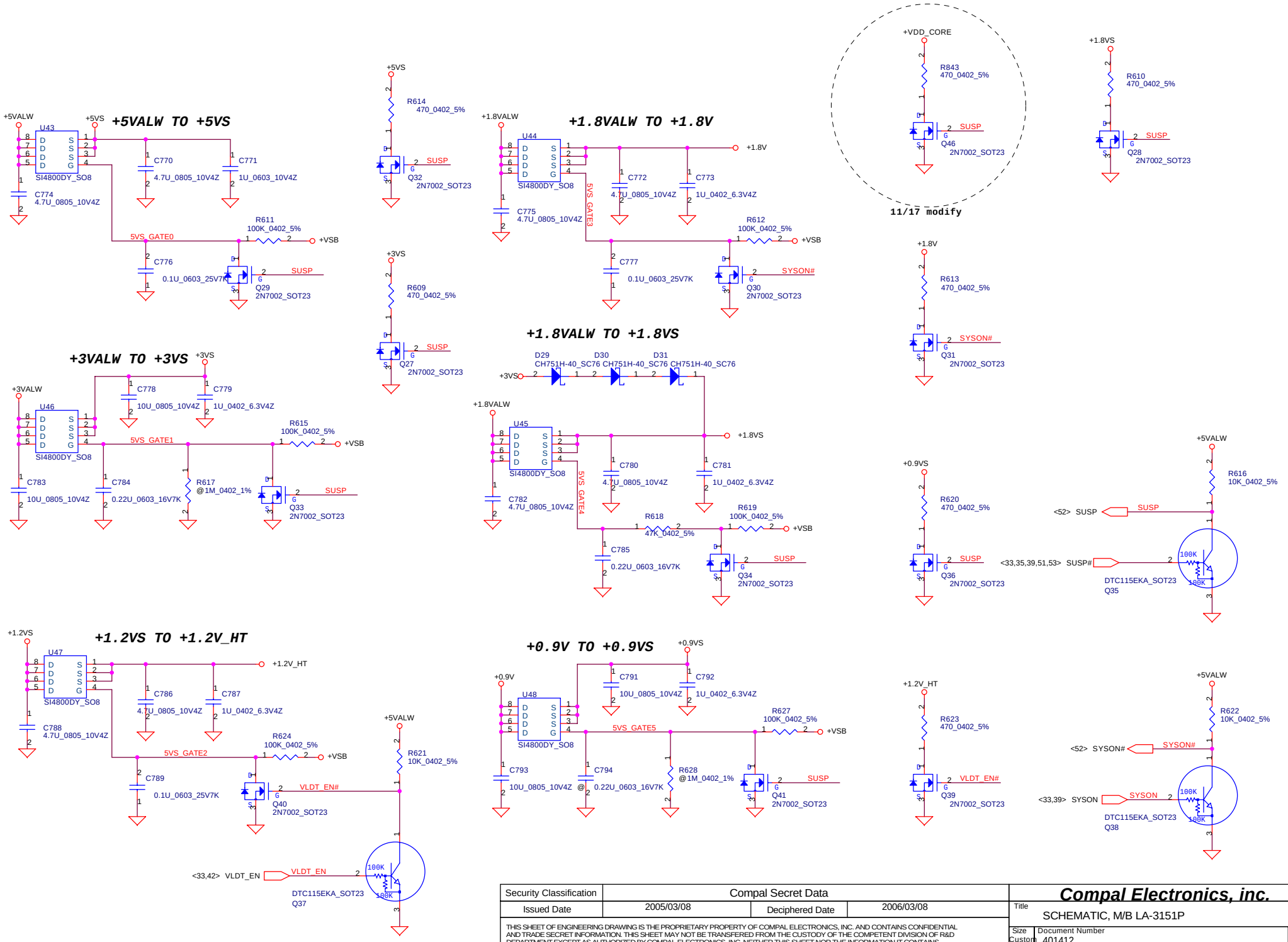

Security Classification	Compal Secret Data		
Issued Date	2005/03/08	Deciphered Date	2006/03/08

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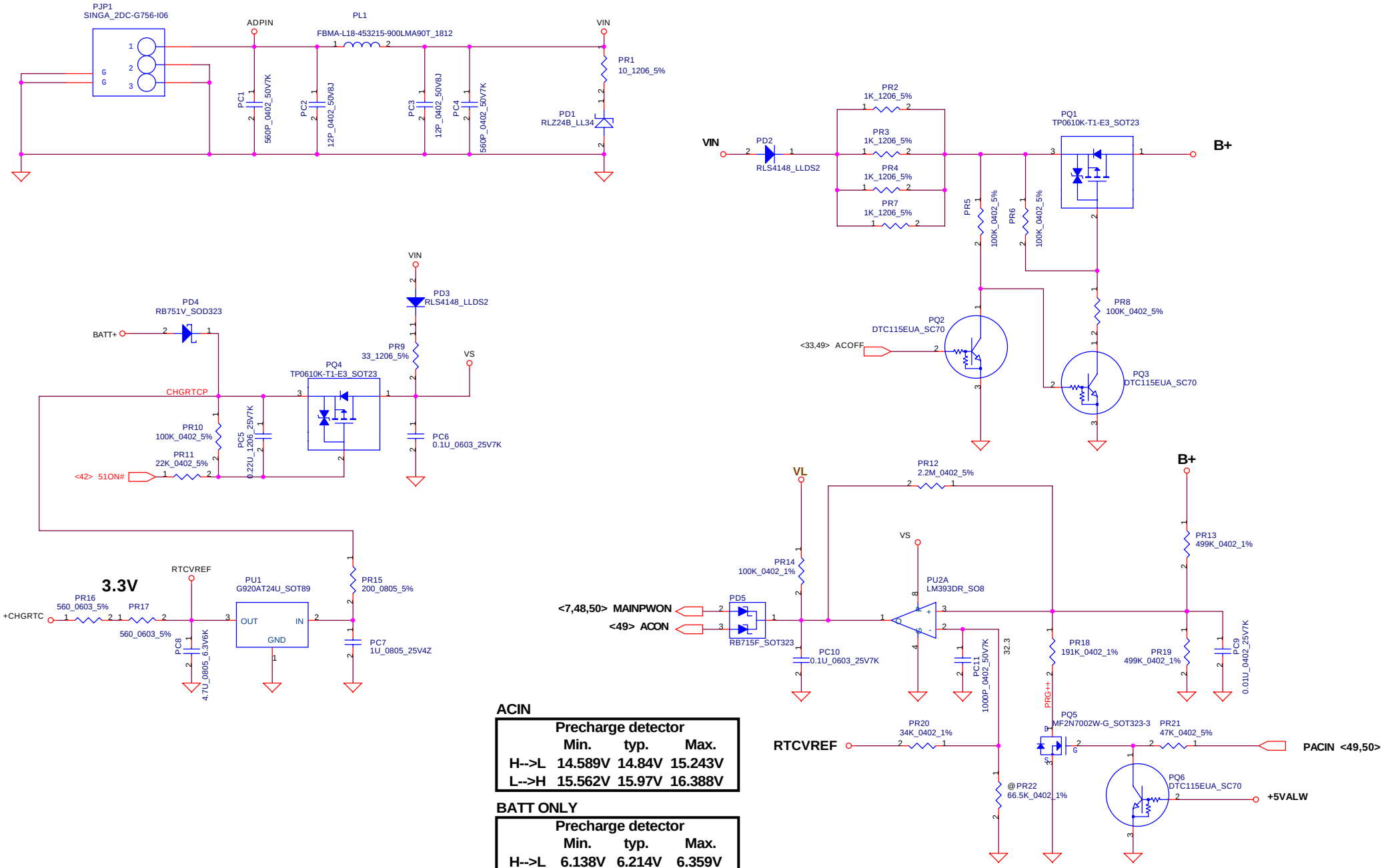

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2005/0926	Deciphered Date	2006/0926

Compal Electronics, Inc.

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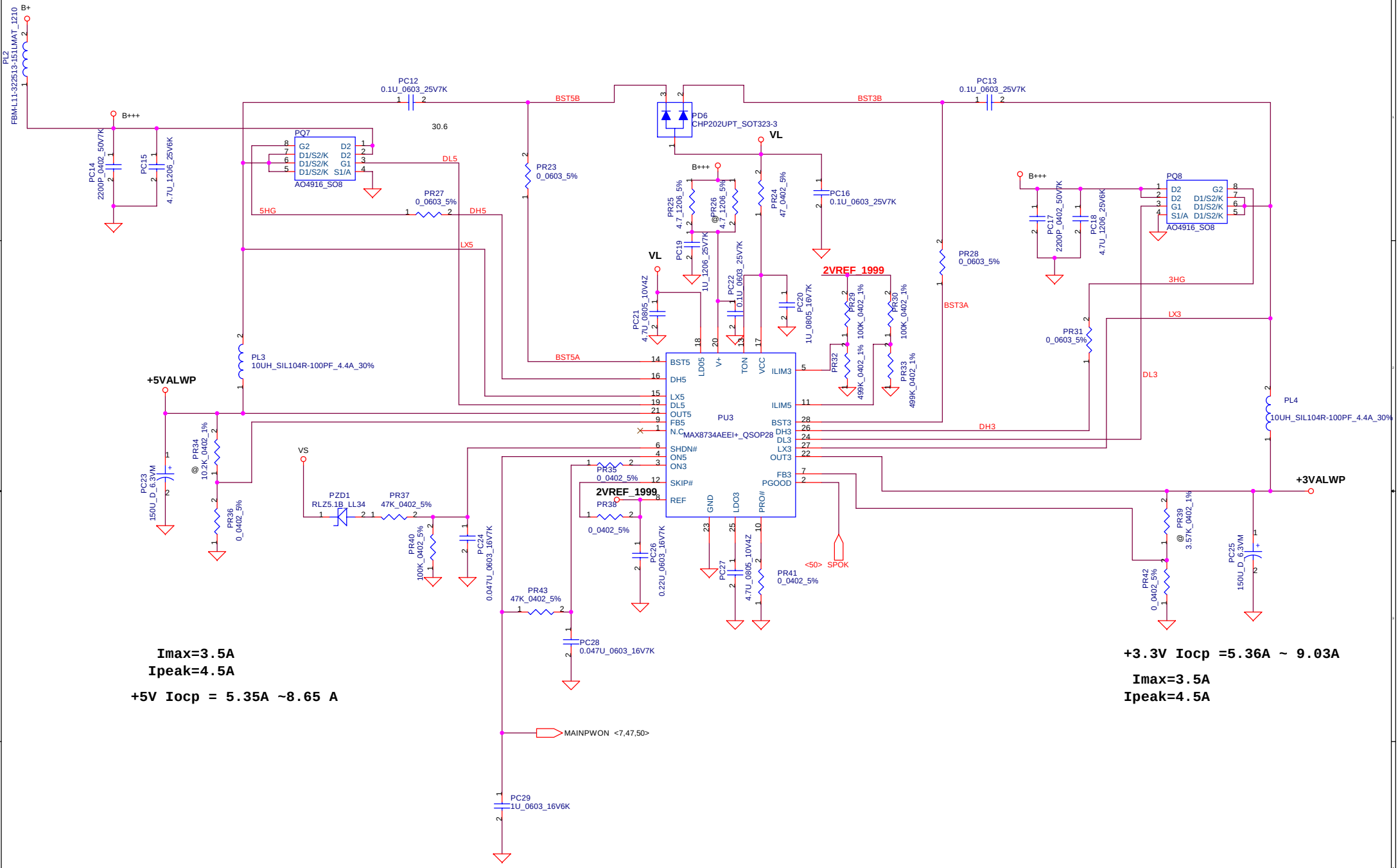

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

Title: SCHEMATIC, M/B LA-3151P

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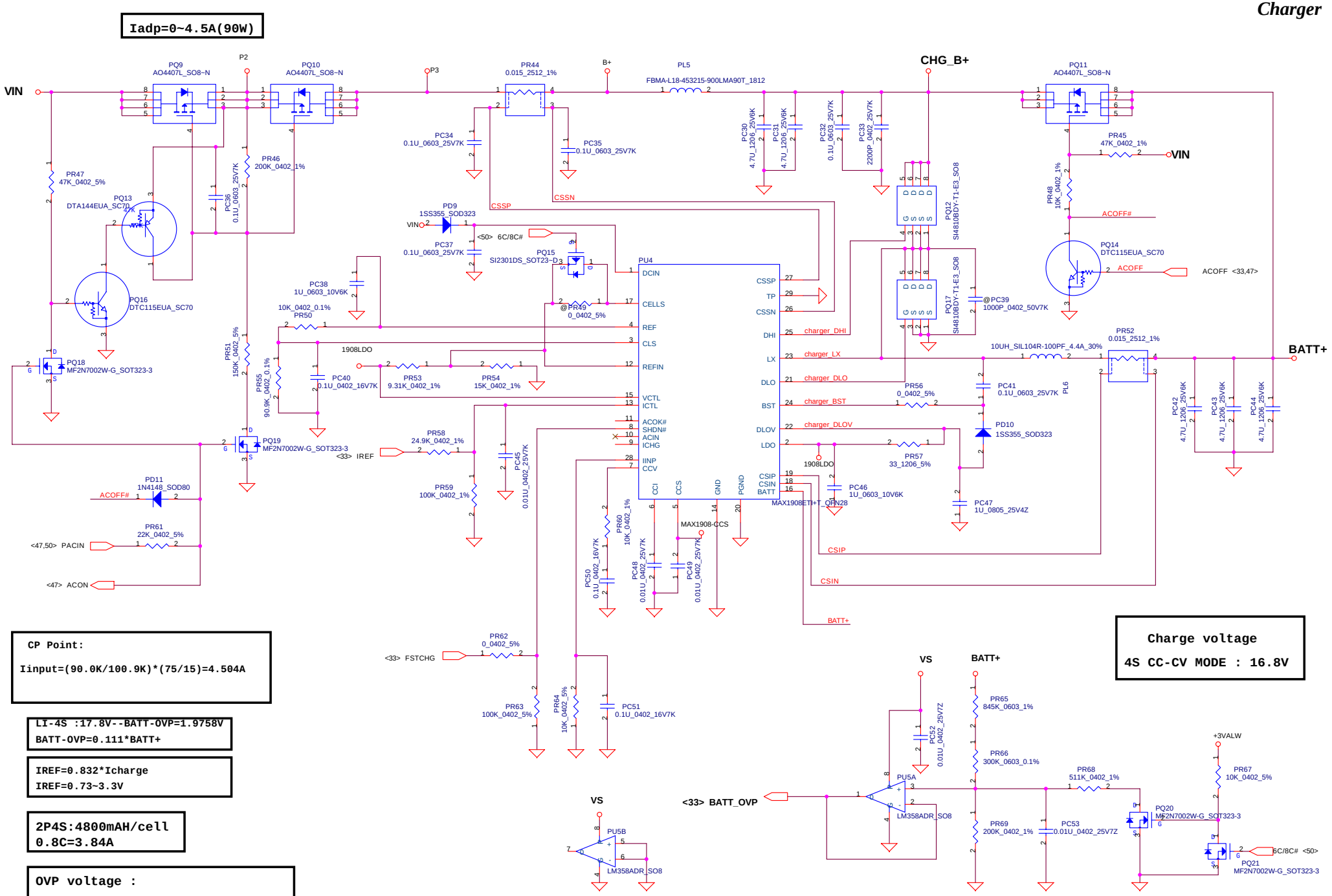
Charger



Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

Title: **SCHEMATIC, M/B LA-3151P**

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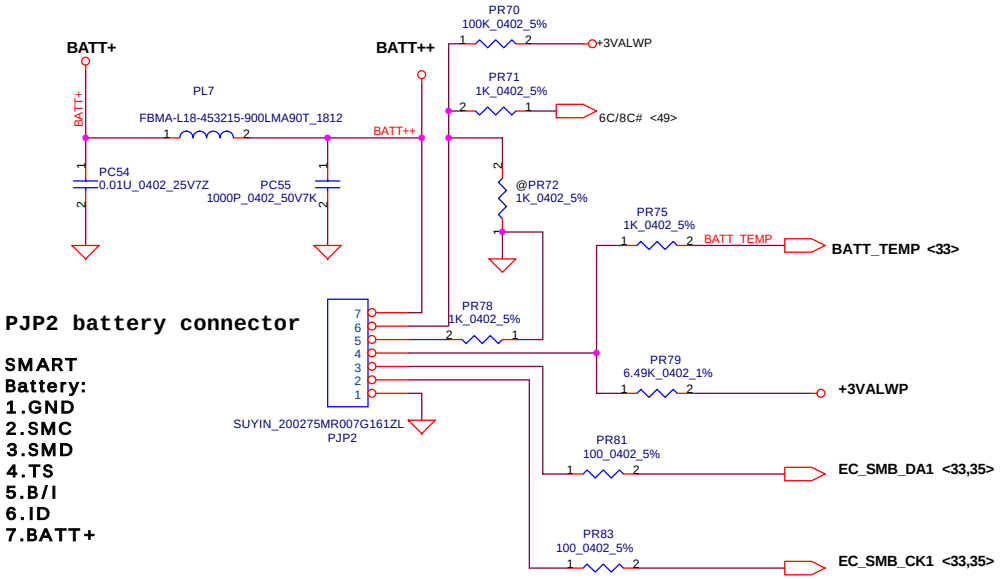
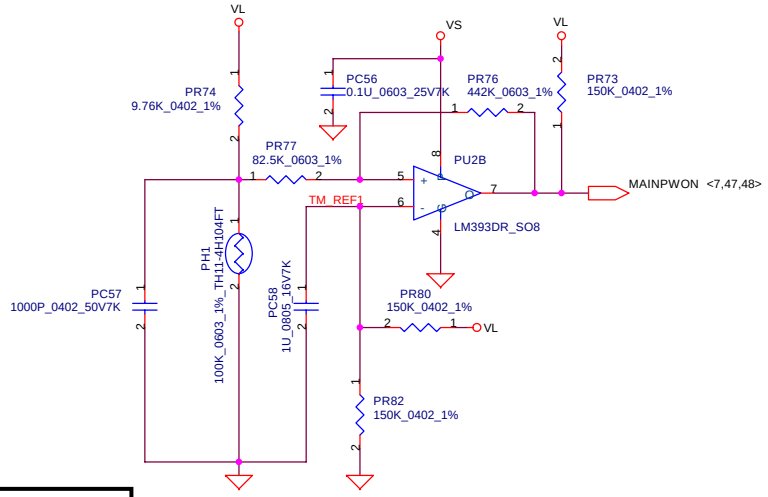


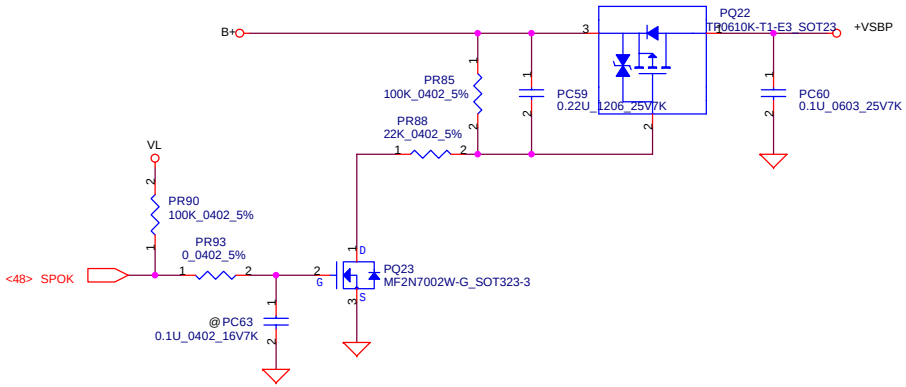
PJP2 battery connector

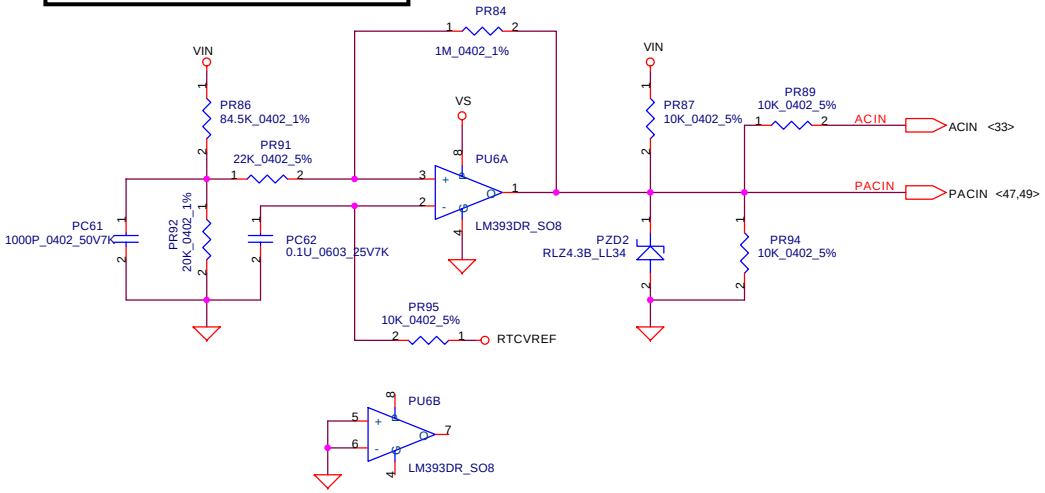
SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+

PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C



Vin Detector	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V





Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

Compal Electronics, Inc.

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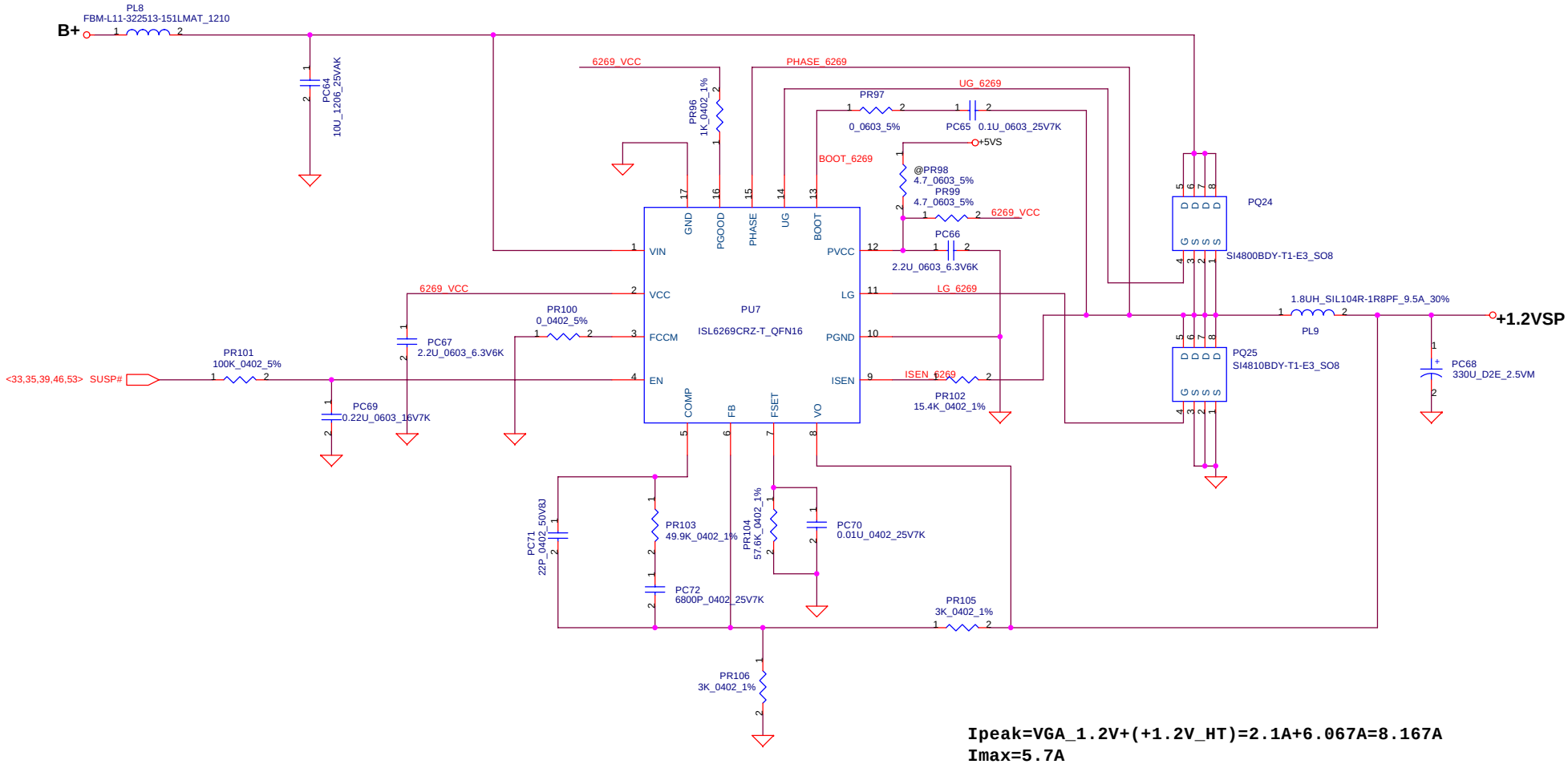

Ipeak=VGA_1.2V+(+1.2V_HT)=2.1A+6.067A=8.167A
Imax=5.7A
Iocmin=9.23A
Iocmax=19.23A

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

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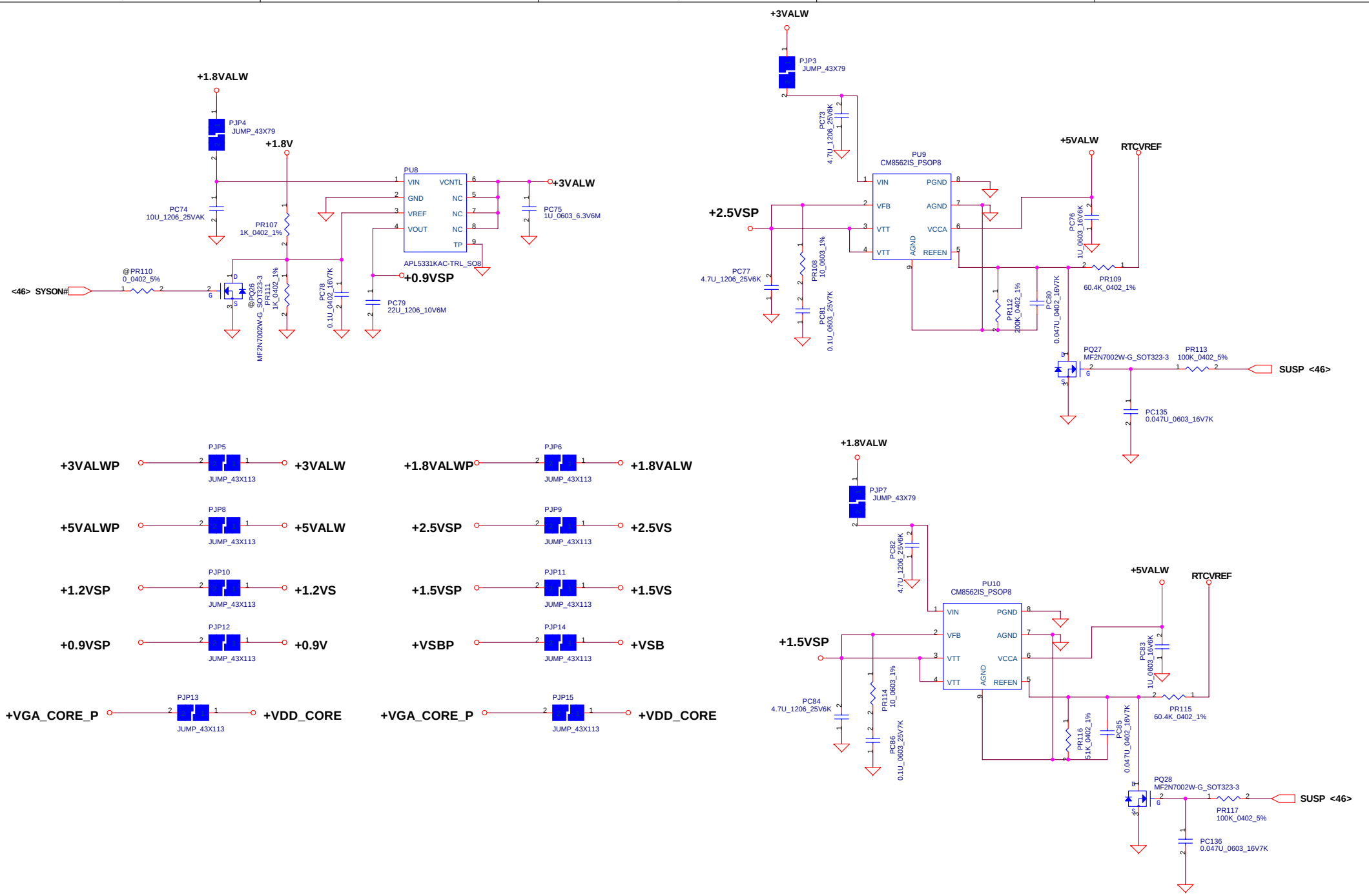

Security Classification	Compal Secret Data		
Issued Date	2005/09/26	Deciphered Date	2006/09/26

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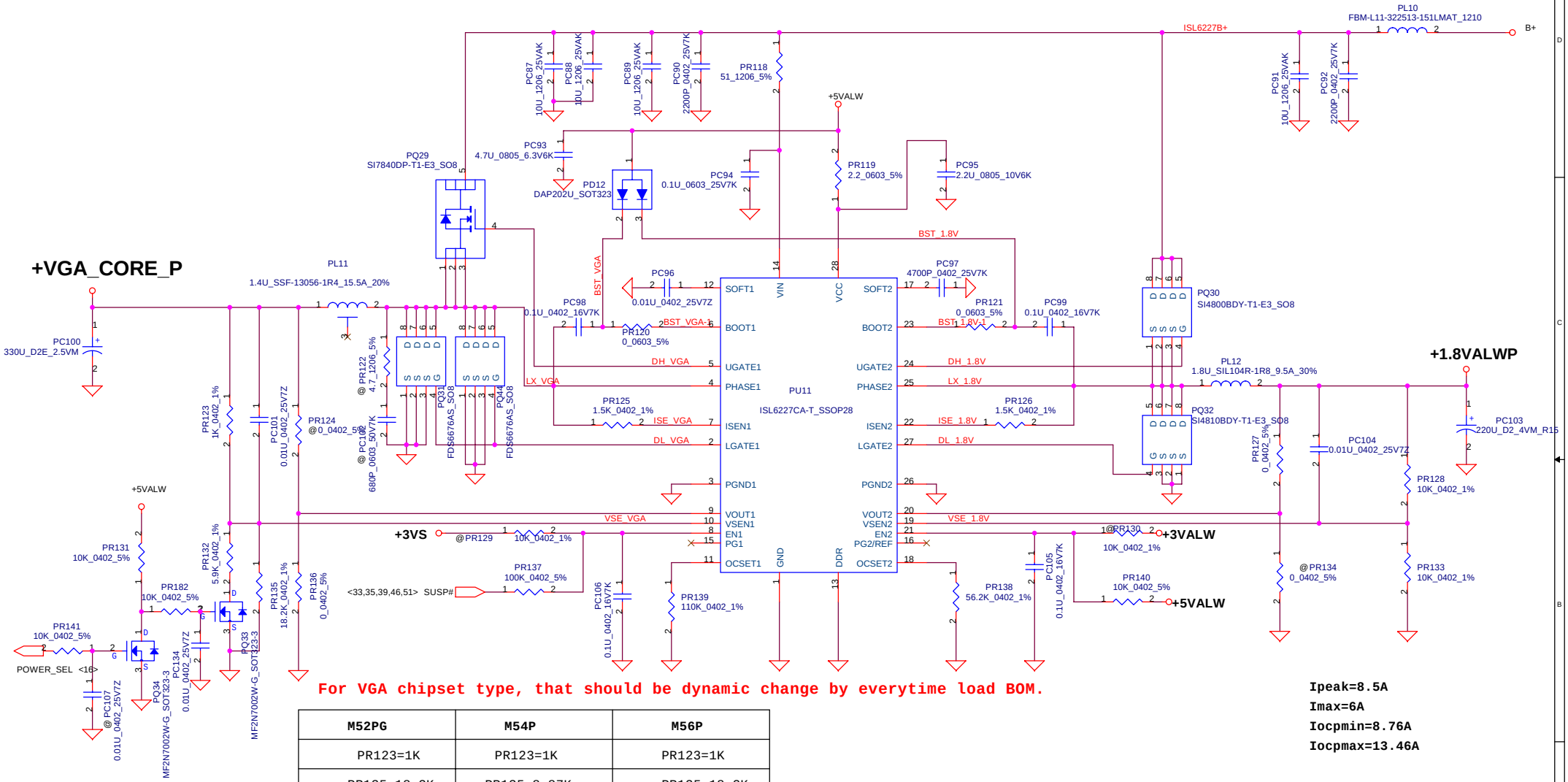

For VGA chipset type, that should be dynamic change by everytime load BOM.

M52PG	M54P	M56P
PR123=1K	PR123=1K	PR123=1K
PR135=18.2K	PR135=8.87K	PR135=18.2K
PR132=17.8K	PR132=8.87K	PR132=5.9K
L=1.000V	**L=1.102V**	**L=1.102V**
H=0.949V	**H=1.001V**	**H=0.949V**

Ipeak=16.40A
Imax=12.25A
Iocpmin=22.07A
Iocpmax=38.67A

Ipeak=8.5A
Imax=6A
Iocpmin=8.76A
Iocpmax=13.46A

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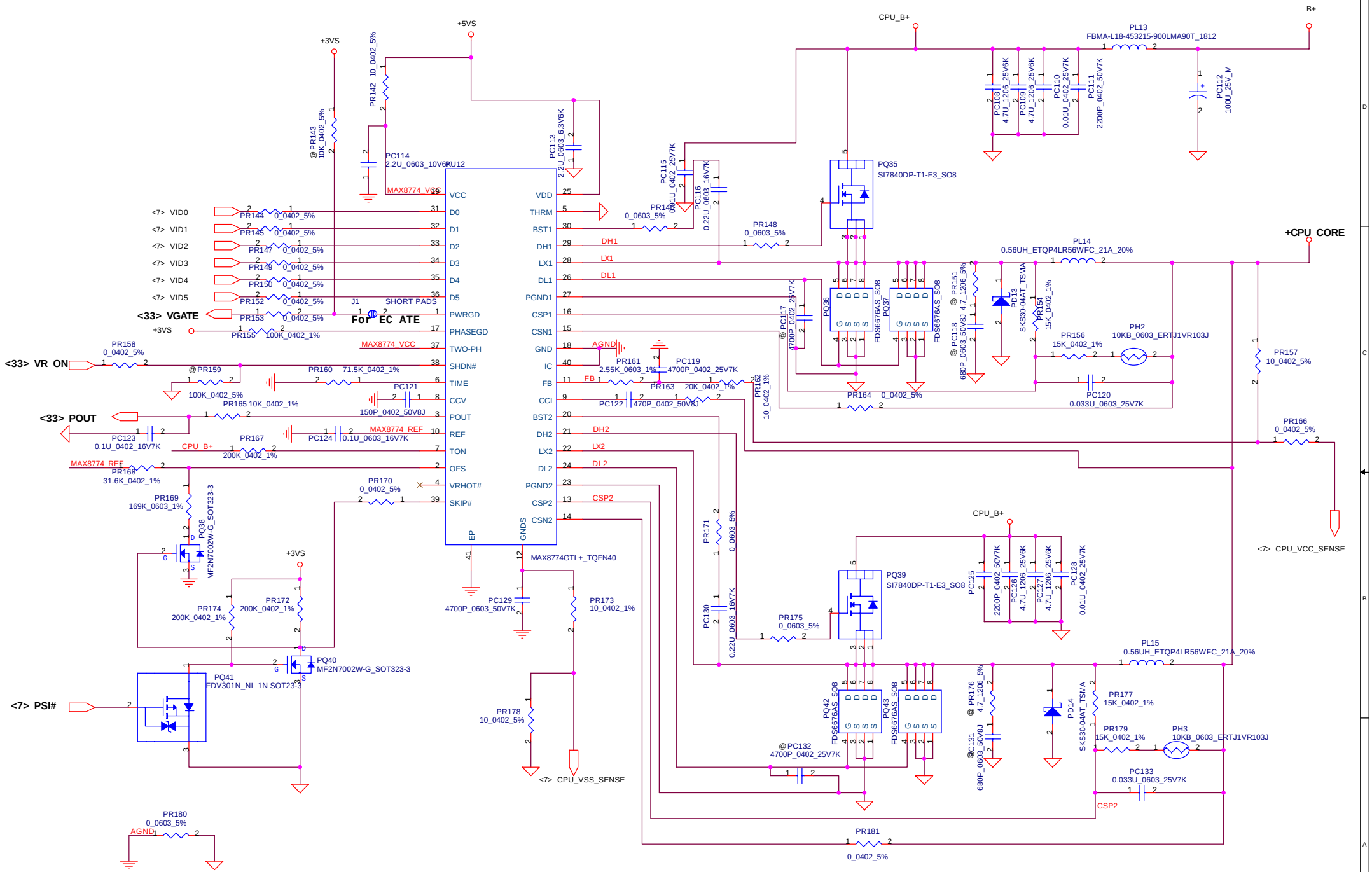

Security Classification	Compal Secret Data		
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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
8							
9							

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