

Compal Confidential

Model Name : P5WE0
File Name : LA-6901P
BOM P/N:43

Compal Confidential

P5WE0 M/B Schematics Document

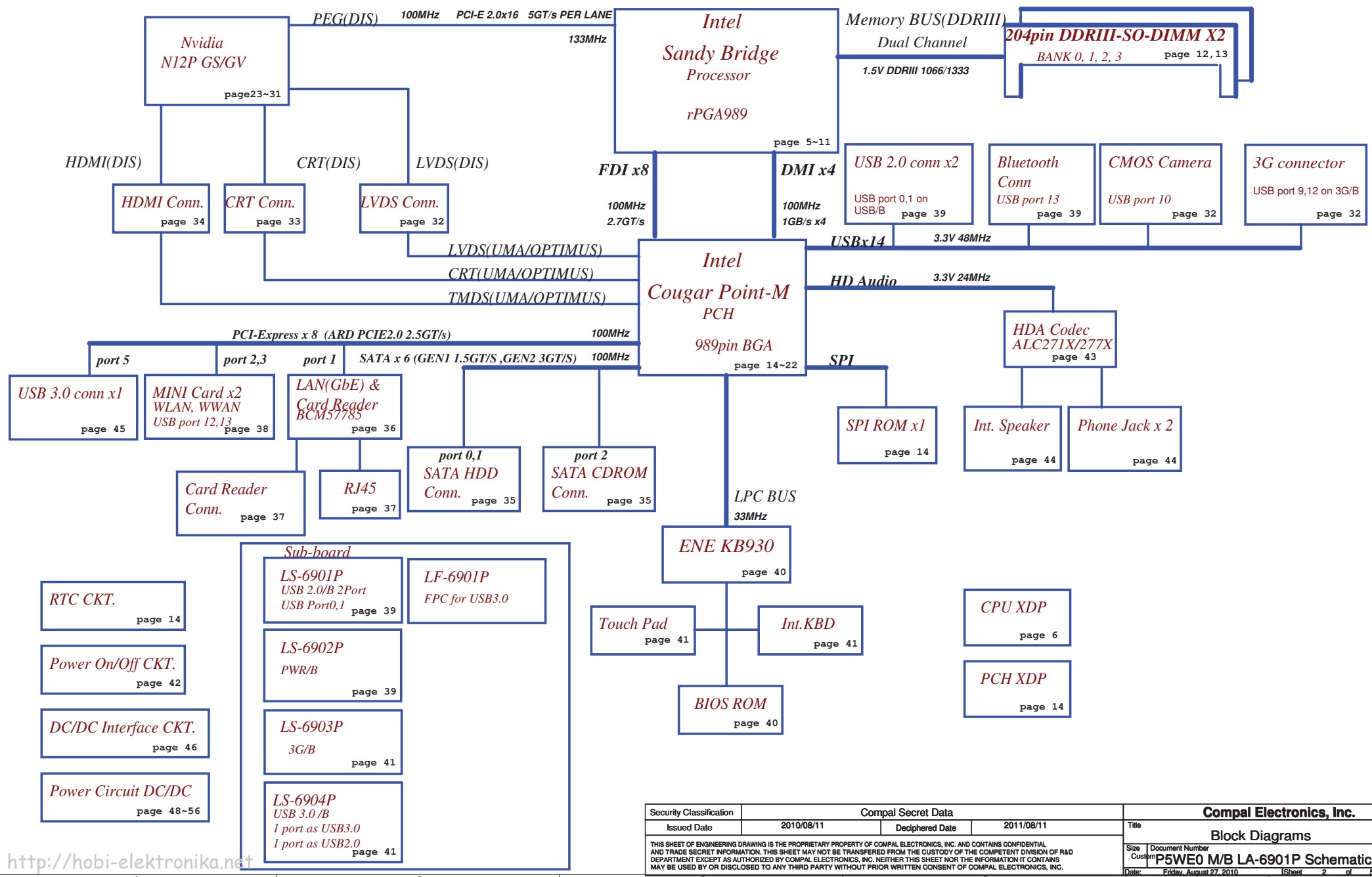
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2010-08-11

REV: 0.1

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Fan Control
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ **USB30 SKU:** USB30@ **OPTIMUS SKU:** OPT@
BT SKU: BT@ **USB20 SKU:** USB20@ **Non-OPTIMUS SKU:** NOPT@
LAN Chip A0 version: A0@
LAN chip B0 Version: B0@

BOM Config

UMA Only: BT@3G@/USB30@/UMA@/UMAO@/NOPT@/A0@
OPTIMUS: BT@3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@
DIS Only: BT@3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@

VRAM BOM Config

X76*BOL01:** Samsung
X76*BOL02:** Hynix

VRAM P/N :

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

<http://hobi-elektronika.net>

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
 DVT
 PVT
 Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

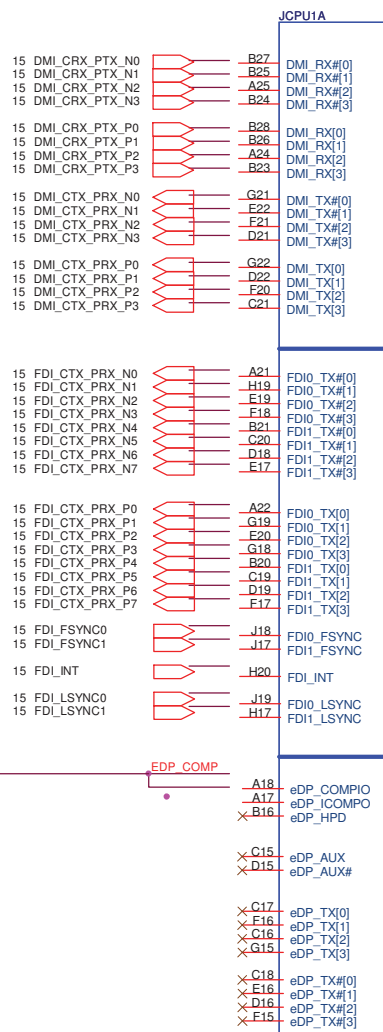
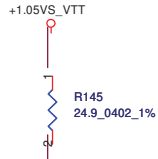
BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@

USB Port Table

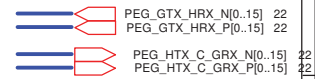
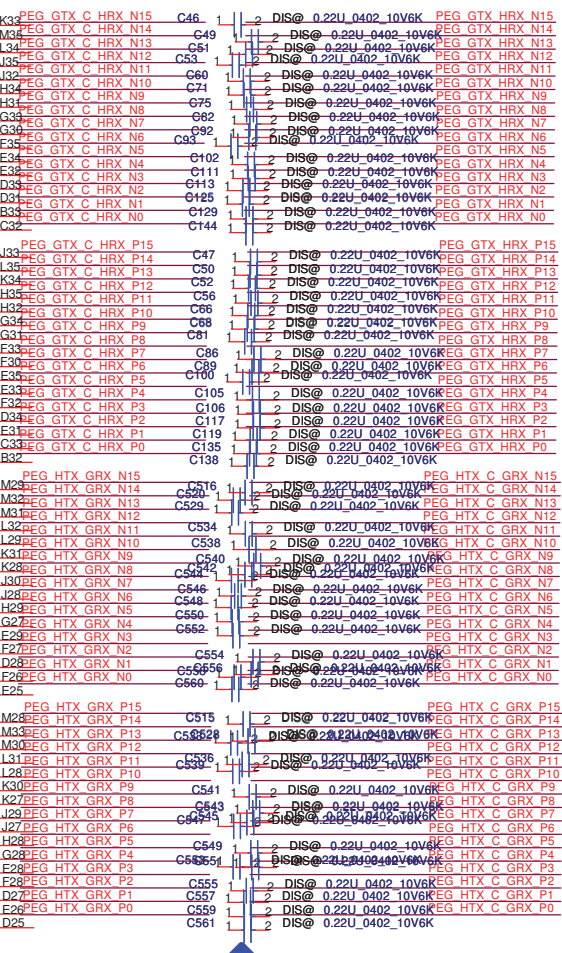
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
		2	USB 2.0 & USB3.0 Conn.
	UHCI1	3	
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Mini Card 1(WLAN)
	UHCI3	9	3G/B(WWAN)
		10	Camera
		11	Mini Card 2(Reserved)
UHCI6	12	SIM Card (3G/B)	
	13	Blue Tooth	

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eDP_COMPIO and ICOMPO signals should be shorted near balls, Trace Width for EDP_COMPIO=4mils, EDP_ICOMPO=12mils, and both length less than 500 mils... should not be left floating ,even if disable eDP function...

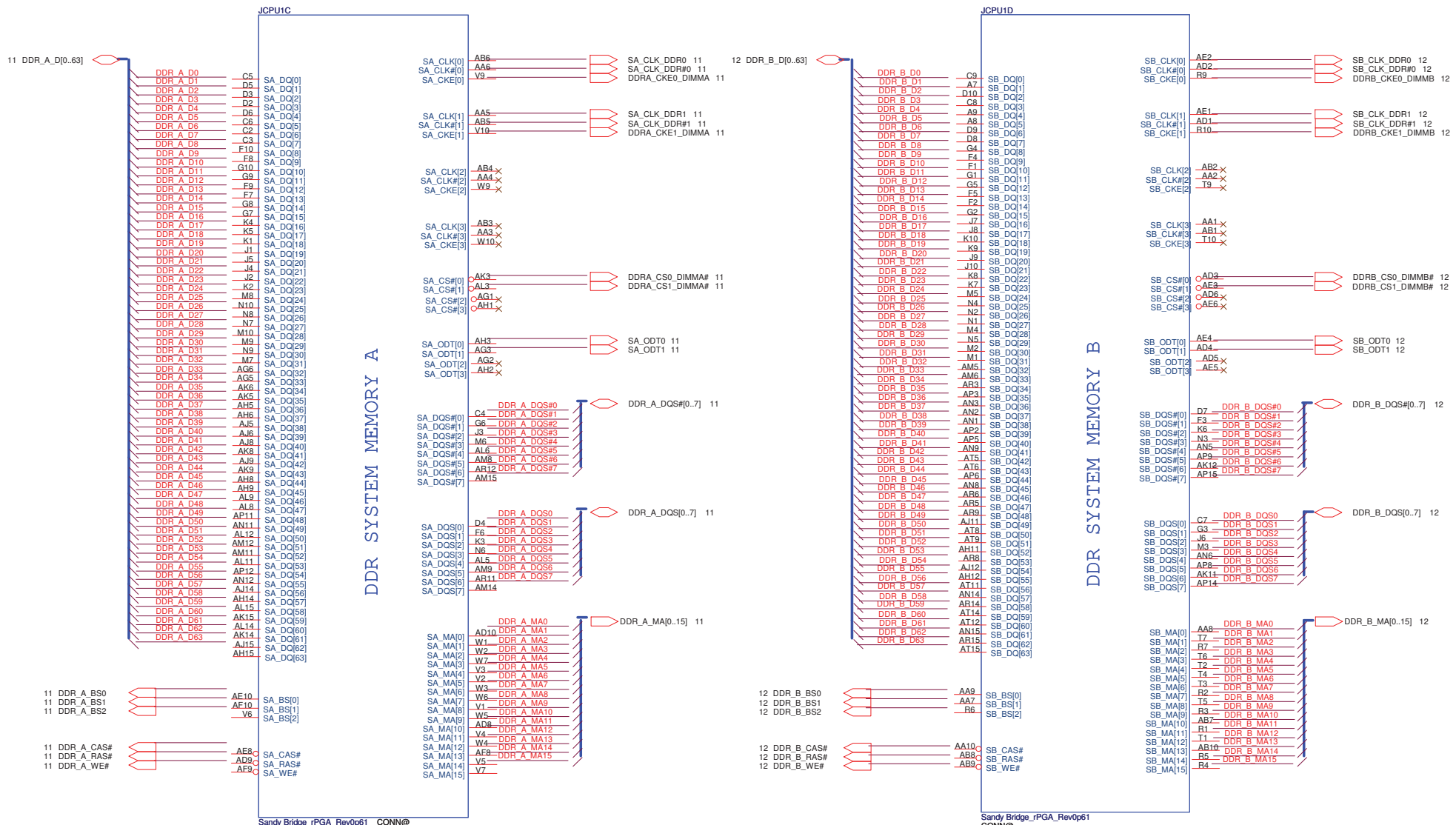


PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed, max length = 500 mils, trace width=4mils
PEG_ICOMPO signals should be routed with - max length = 500 mils, trace width=12mils spacing =15mils



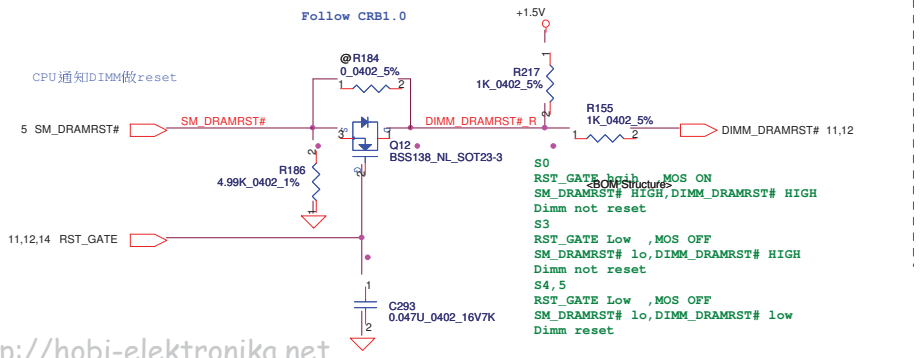
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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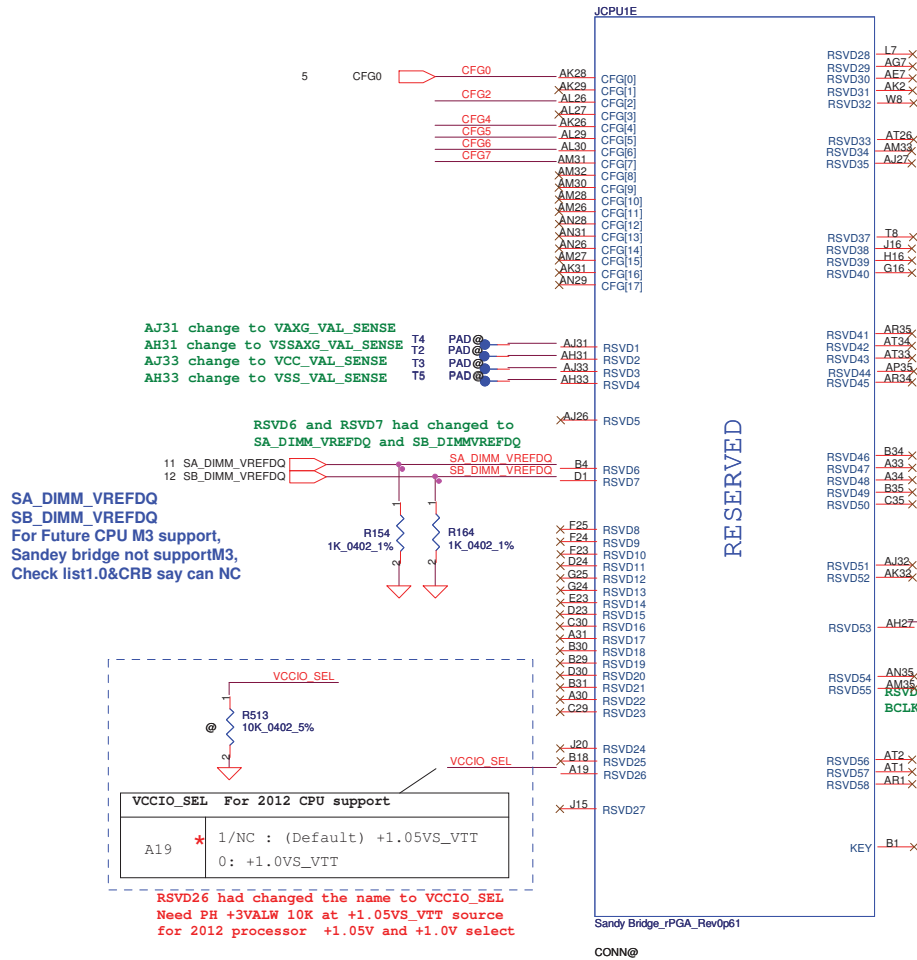
Sandy Bridge_rPGA_Rev0p61 CONN@

Sandy Bridge_rPGA_Rev0p61 CONN@



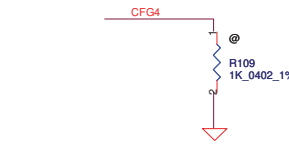
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CFG Straps for Processor



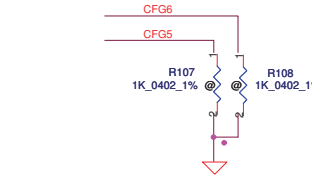
CFG2

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



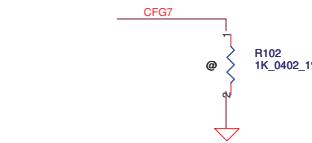
CFG4

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



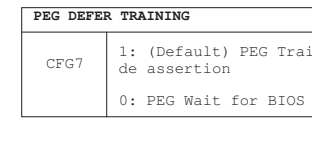
CFG6

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



CFG7

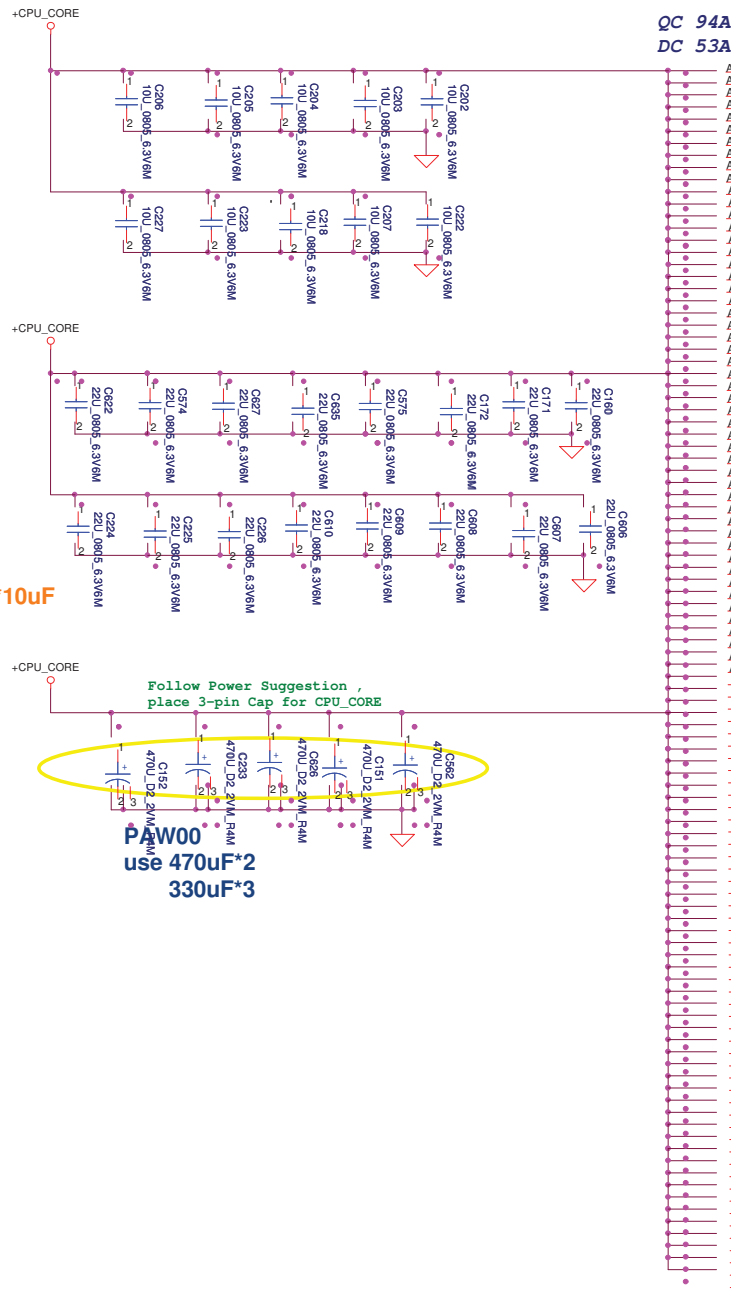
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



SV type CPU

JCPU1F

POWER



INTEL Recommend
4*470uF, 16*22uF and 10*10uF
from PDDG 1.0

Follow Power Suggestion,
place 3-pin Cap for CPU_CORE

PAW00
use 470uF*2
330uF*3

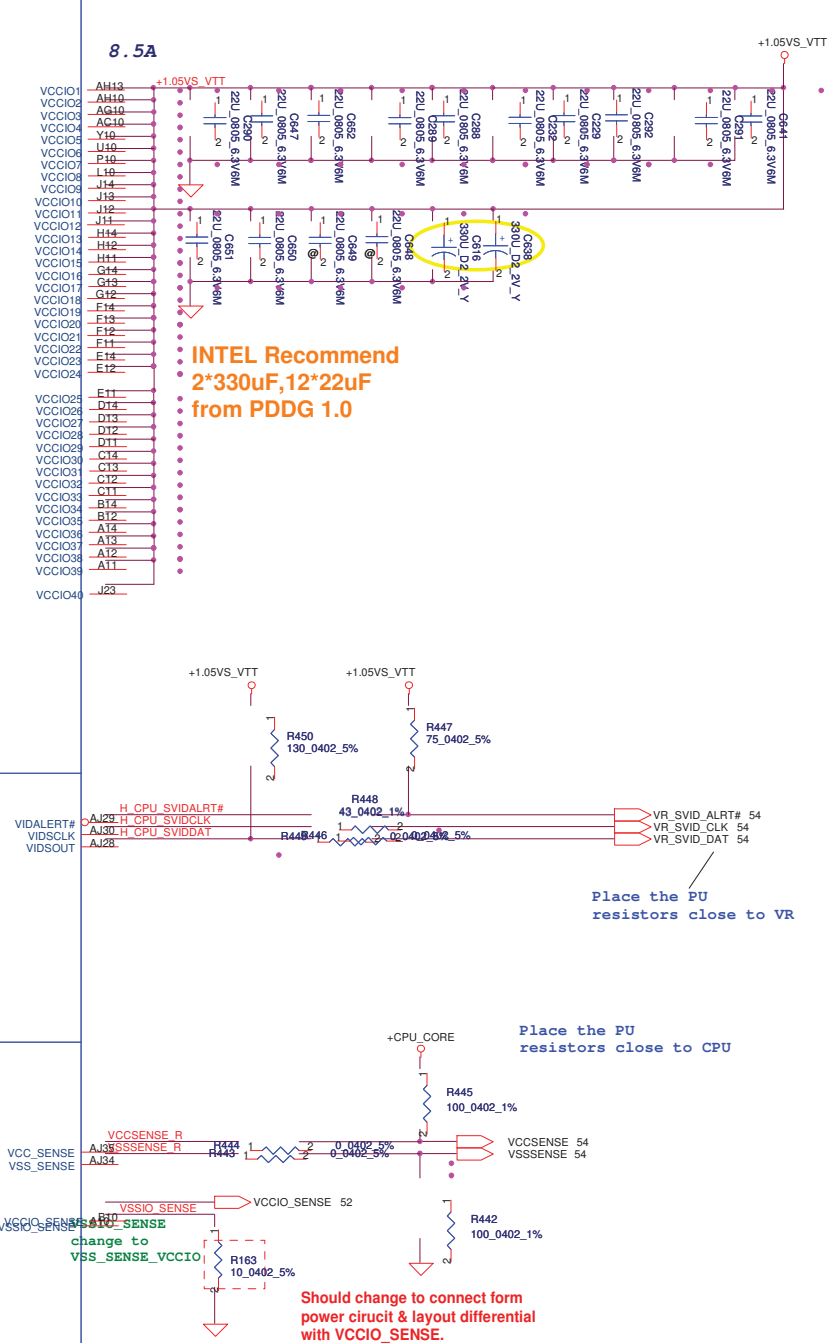
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AF34 VCC10
- AF33 VCC11
- AF32 VCC12
- AF31 VCC13
- AF30 VCC14
- AF29 VCC15
- AF28 VCC16
- AF27 VCC17
- AD35 VCC18
- AD34 VCC19
- AD33 VCC20
- AD32 VCC21
- AD31 VCC22
- AD30 VCC23
- AD29 VCC24
- AD28 VCC25
- AD27 VCC26
- AD26 VCC27
- AD25 VCC28
- AD24 VCC29
- AD23 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- R35 VCC80
- R34 VCC81
- R33 VCC82
- R32 VCC83
- R31 VCC84
- R30 VCC85
- R29 VCC86
- R28 VCC87
- R27 VCC88
- R26 VCC89
- P35 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- P26 VCC99
- P25 VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES



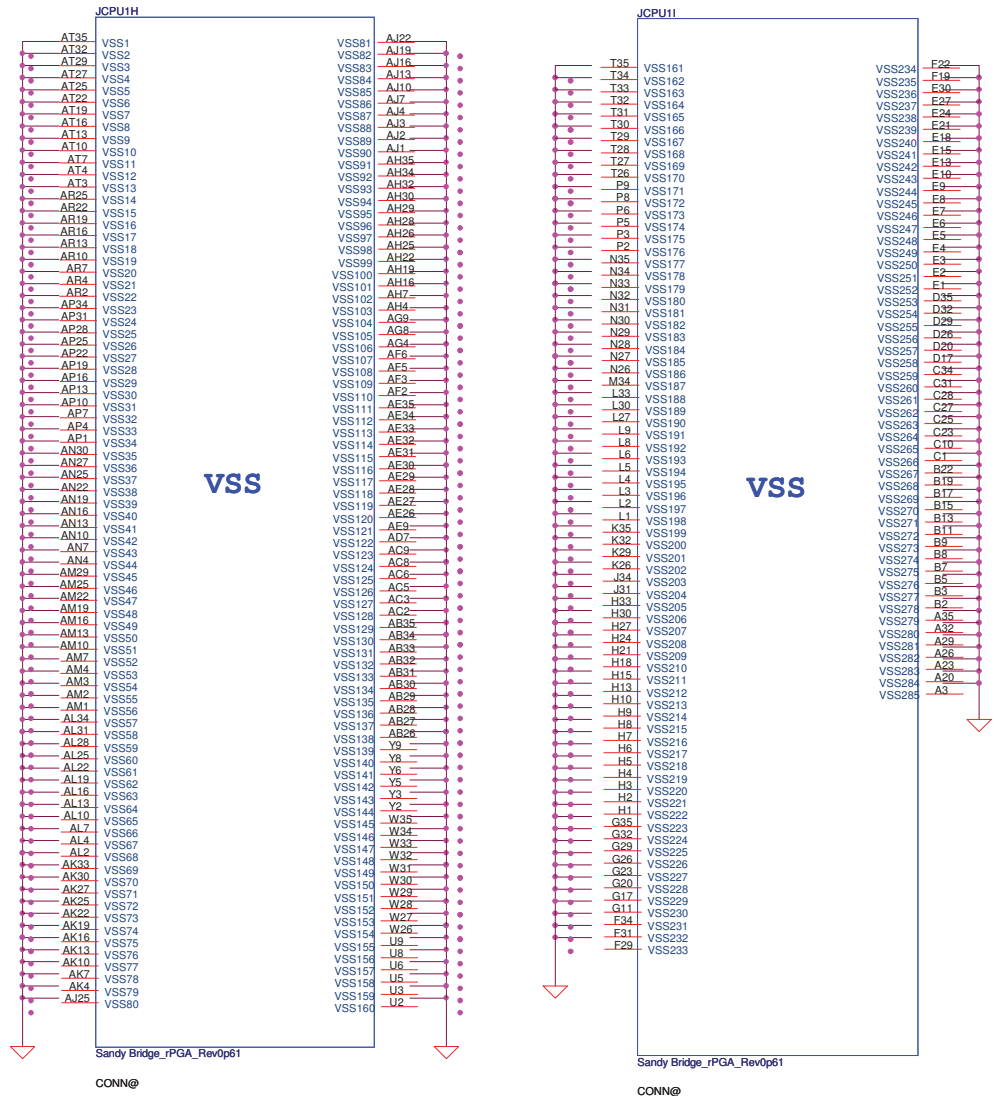
INTEL Recommend
2*330uF, 12*22uF
from PDDG 1.0

Place the PU
resistors close to VR

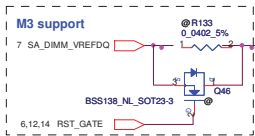
Place the PU
resistors close to CPU

Should change to connect form
power circuit & layout differential
with VCCIO_SENSE.

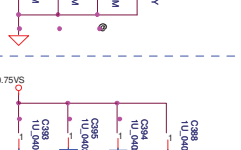
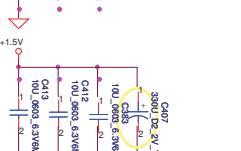
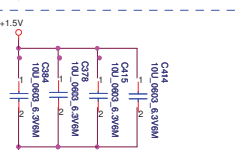
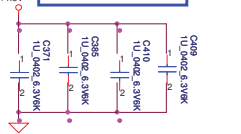
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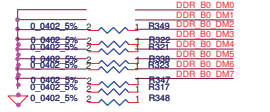
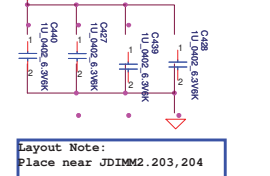
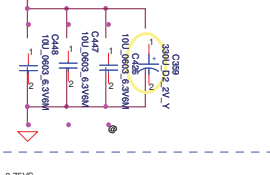
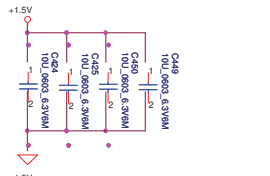
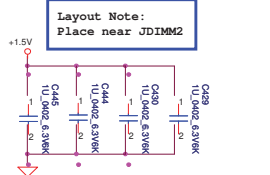
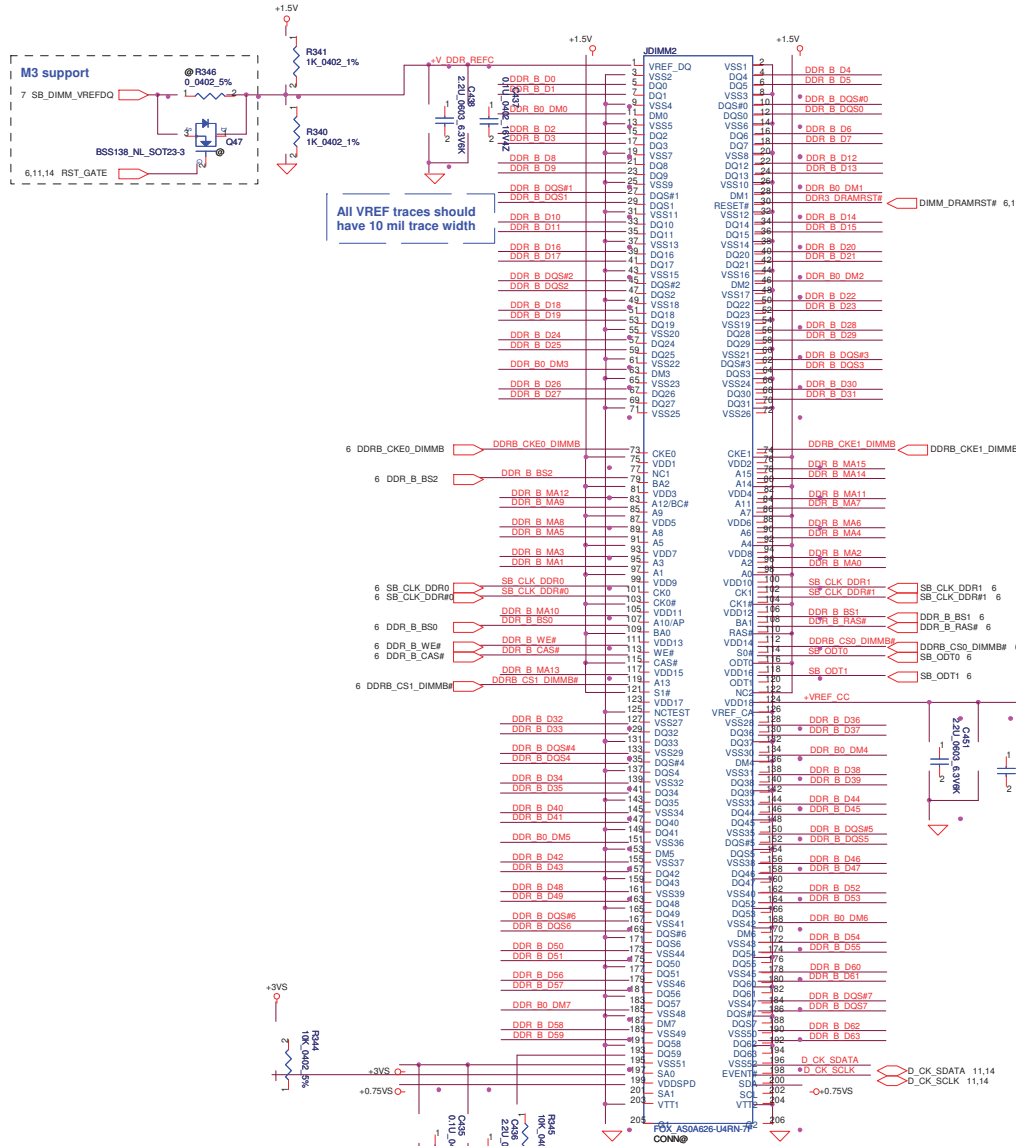


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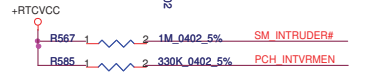
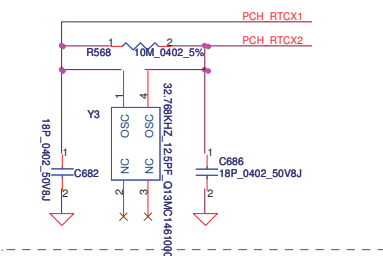


Layout Note:
Place near JDIMM1

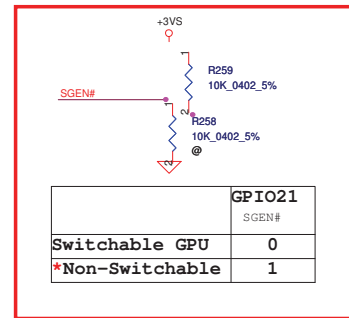
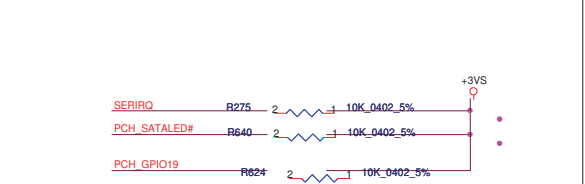
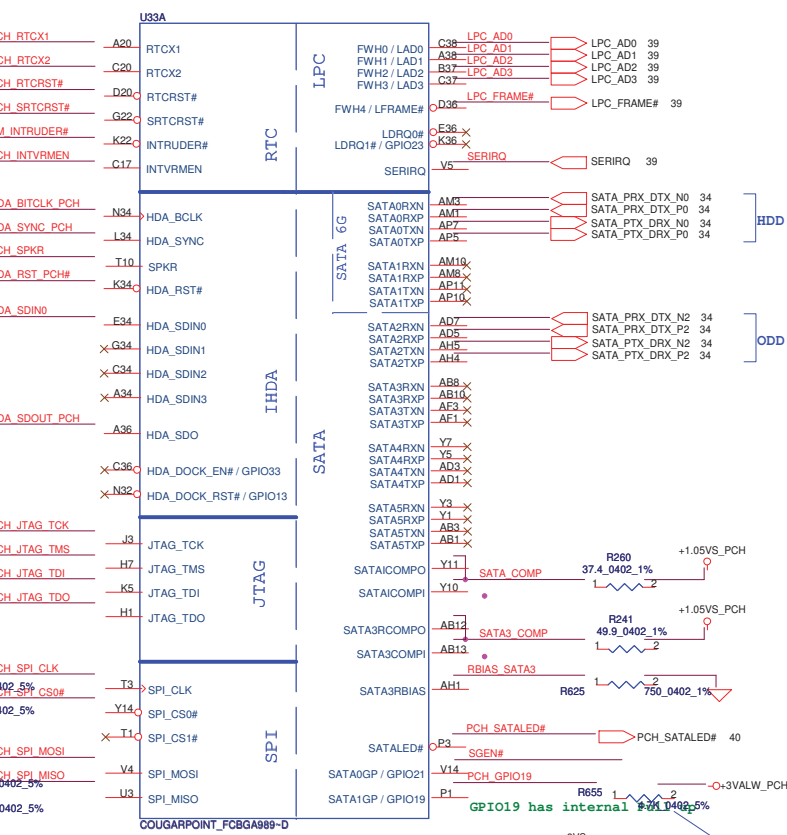
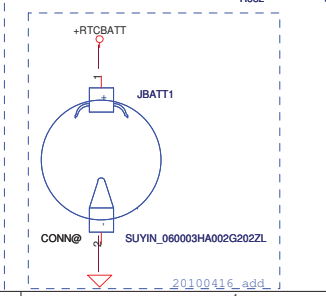
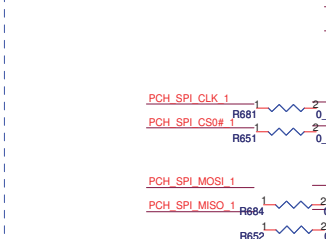
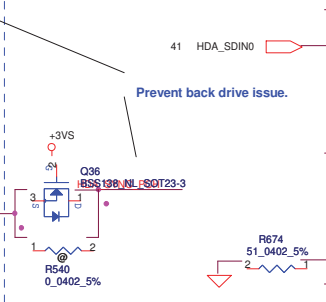
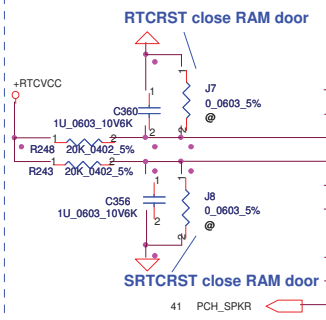
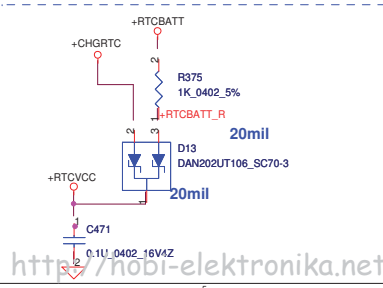
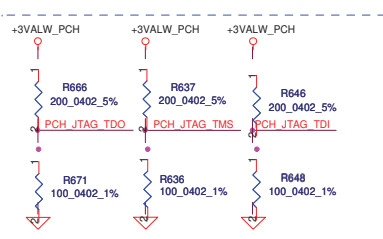
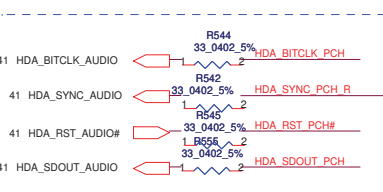
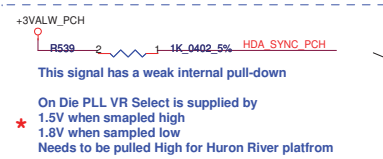
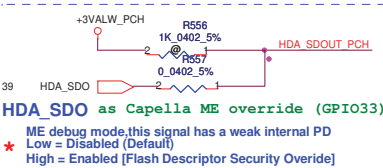
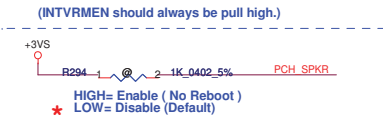




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Size	Document Number	Rev	PSWE0 M/B LA-6901P Schematic		
Custom		0.1			
Date:	Friday, August 27, 2010	Sheet	12	of 50	



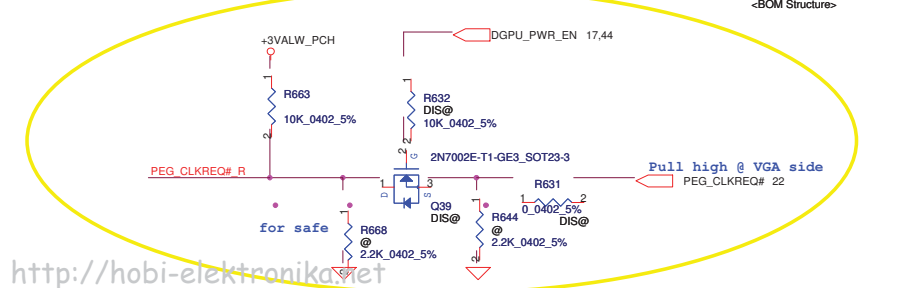
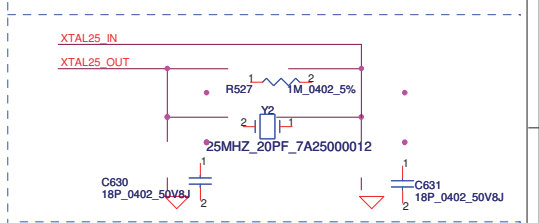
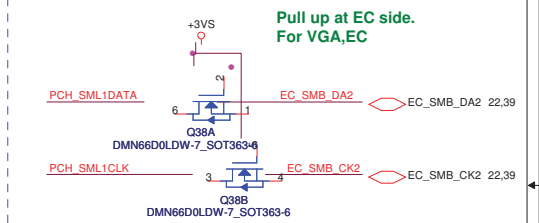
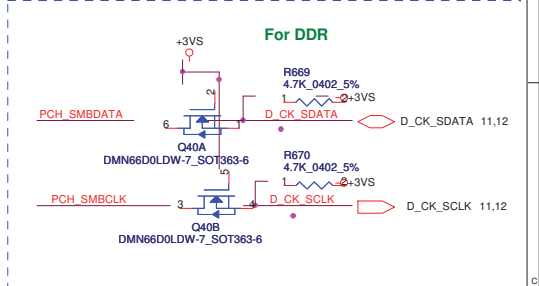
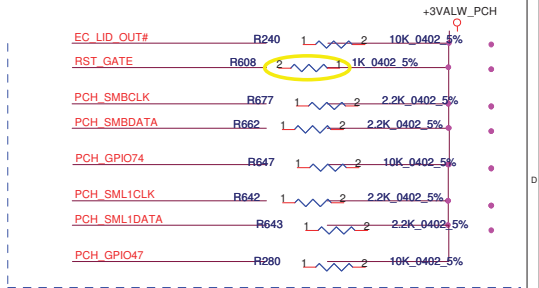
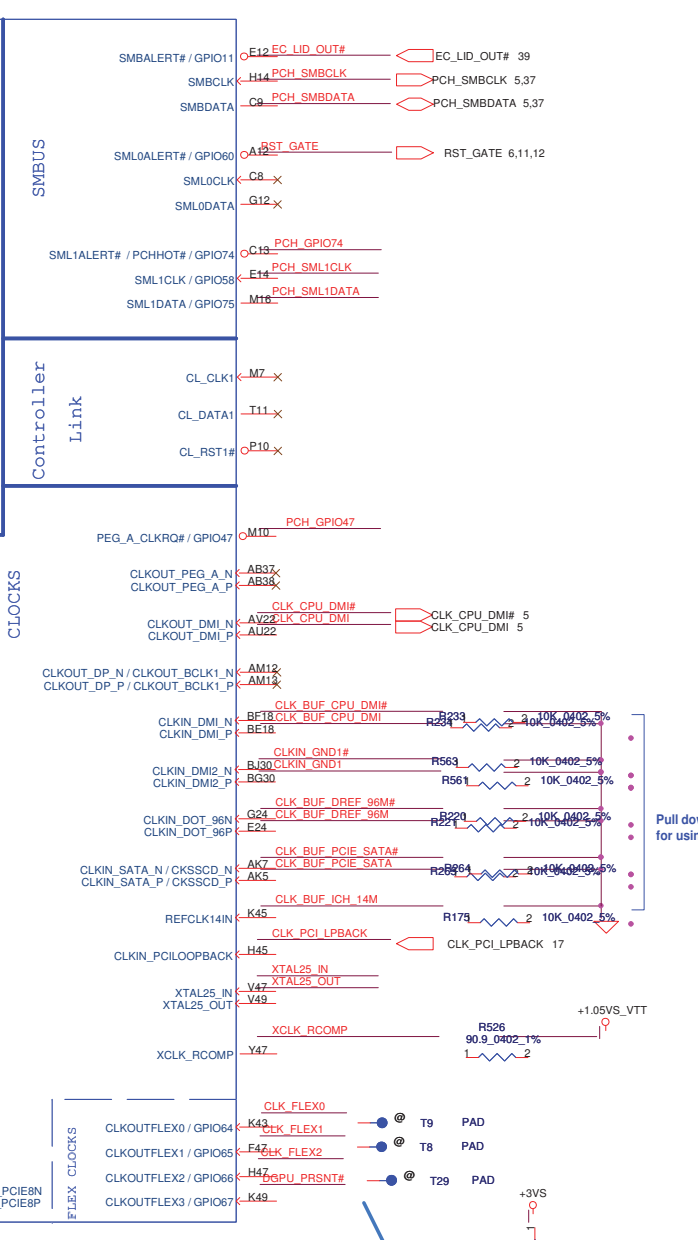
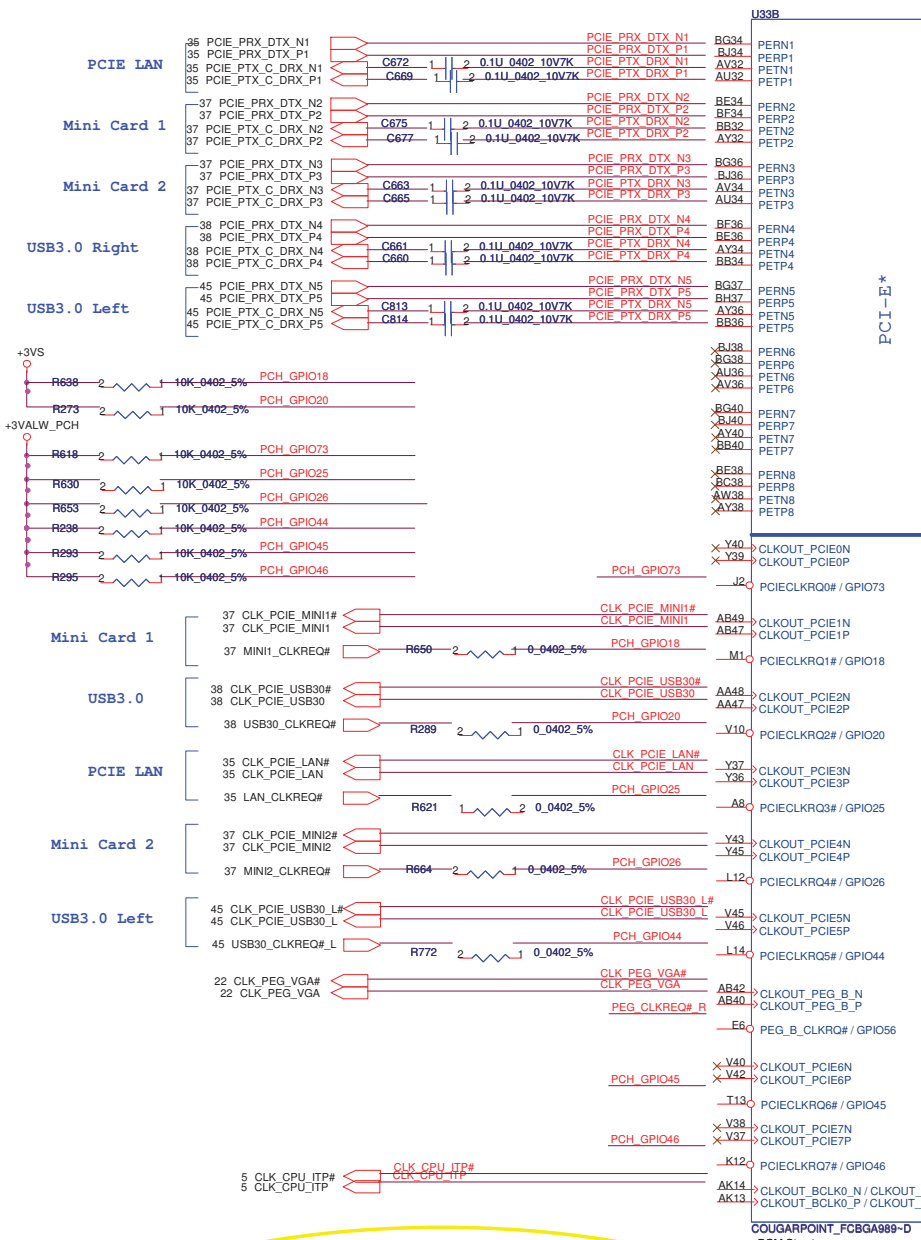
INTVRMEN
 * H : Integrated VRM enable
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1

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Compal Electronics, Inc.
 Title: **PCH (1/8) SATA, HDA, SPI, LPC, XDP**
 Size: Custom
 Document Number: **P5WE0 M/B LA-6901P Schematic**
 Date: Friday, August 27, 2010
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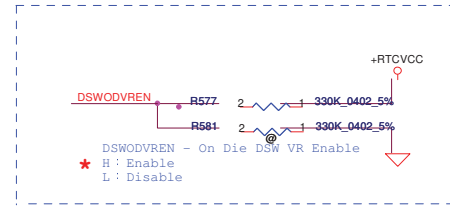
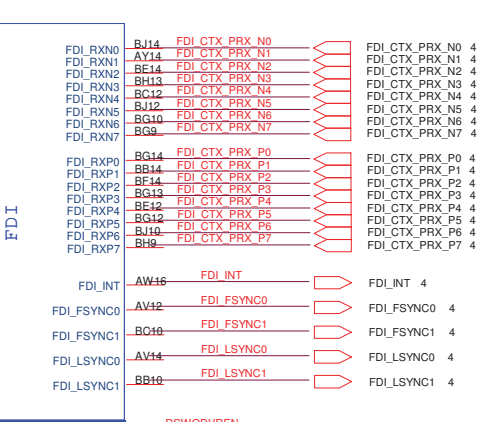
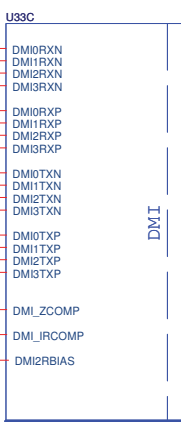
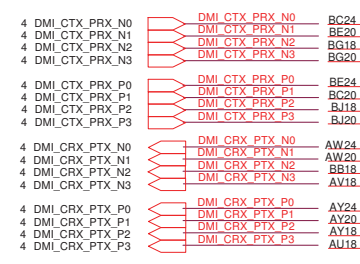
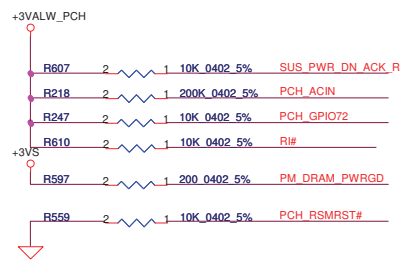
	GPIO67
DGPU_PRSN#	
DIS, OPTIMUS	0
UMA	1

Security Classification	Compal Secret Data	
Issued Date	2010/08/11	Deciphered Date
		2011/08/11

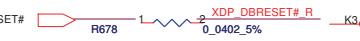
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Compal Electronics, Inc.		
PCH (2/8) PCIE, SMBUS, CLK		
Size	Document Number	Rev
Custom	PSWE0 M/B LA-6901P Schematic	0.1
Date:	Friday, August 27, 2010	Sheet 14 of 59

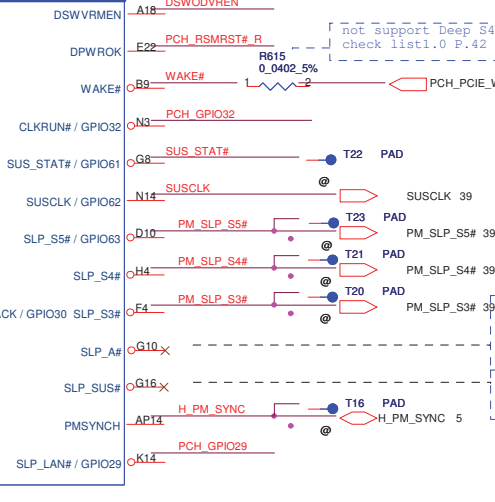
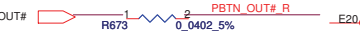
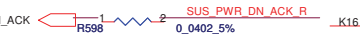
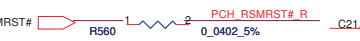
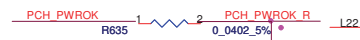
<http://hobi-elektronika.net>



not support Deep S4,S5 mux with SUS_PWR_DN_ACK



not support AMT APWROK can mux with PWROK (check list1.0 P.40)

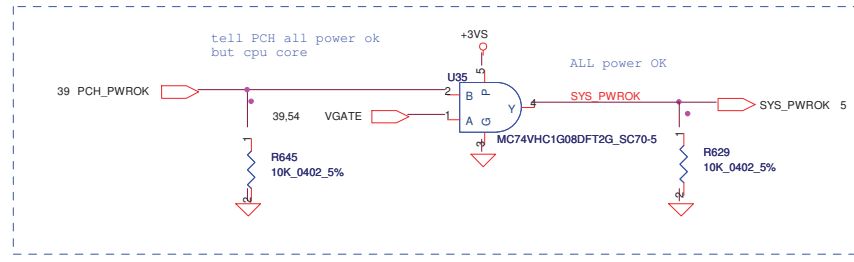


not support Deep S4,S5 DPWROK mux with PWROK check list1.0 P.42

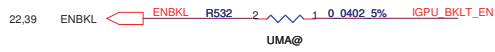


Can be left NC when IMT is not support on the platform

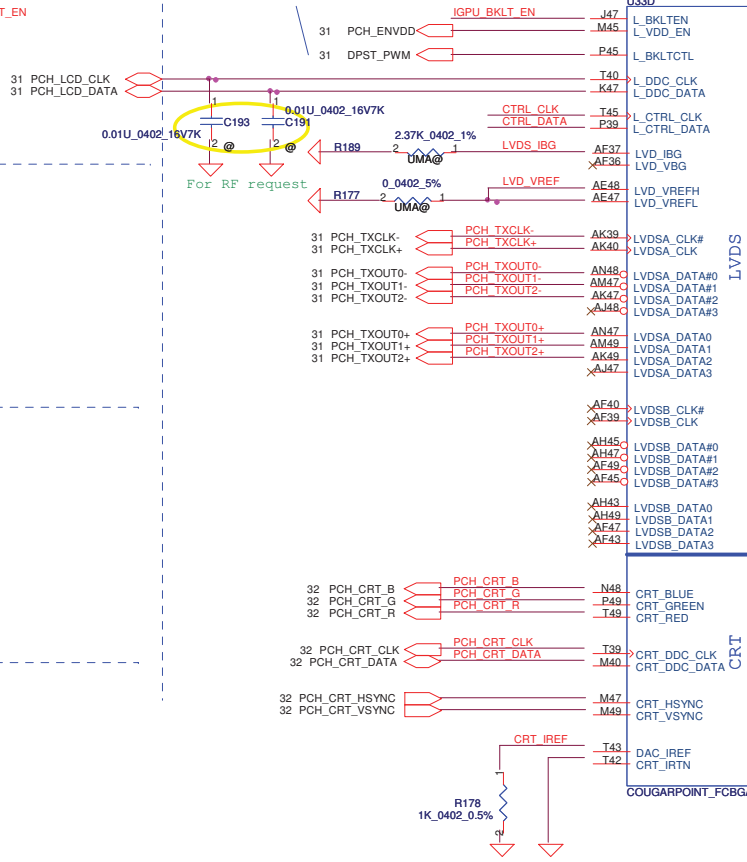
not support Deep S4,S5 can NC PCH EDS1.2 P.74



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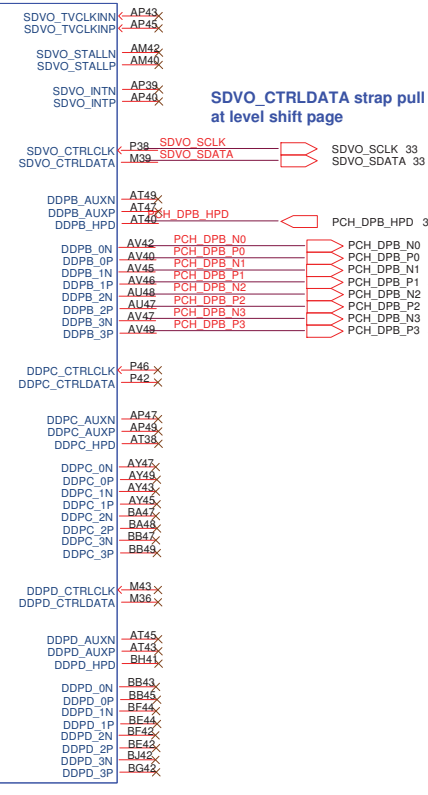


Pull high at LVDS conn side.



U33D

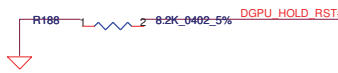
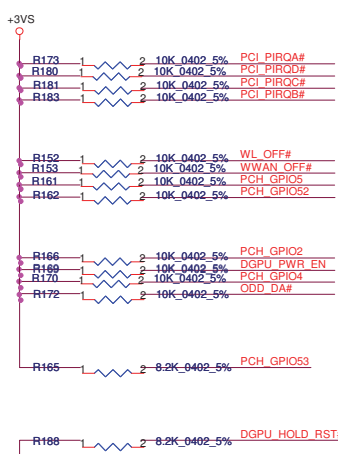
Digital Display Interface



SDVO_CTRLDATA strap pull high at level shift page

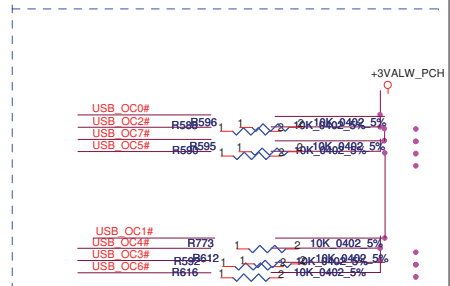
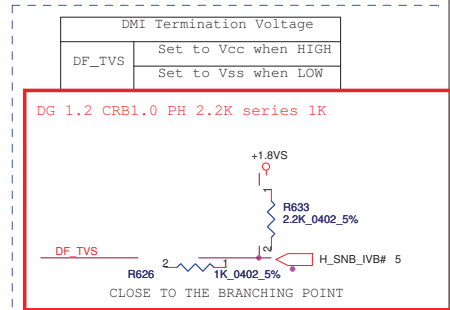
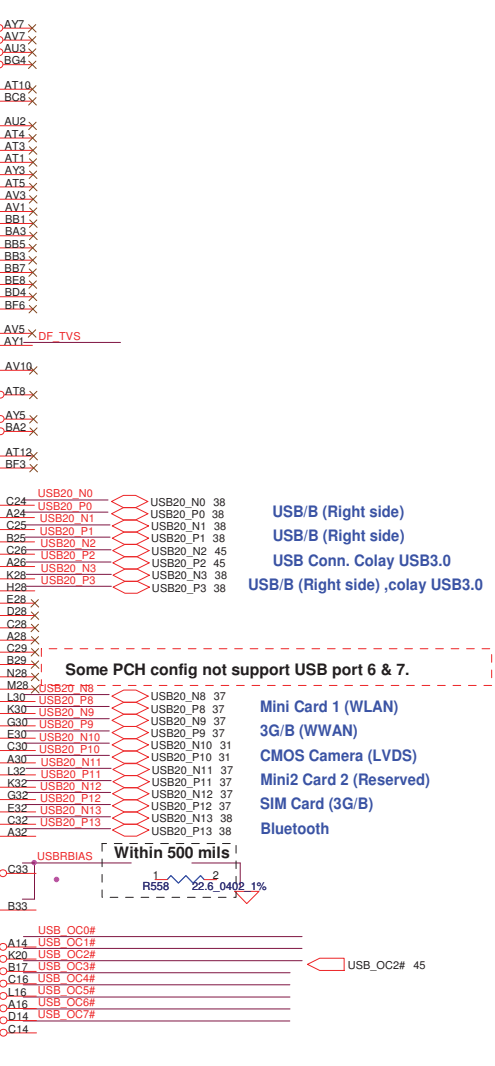
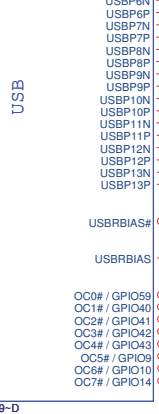
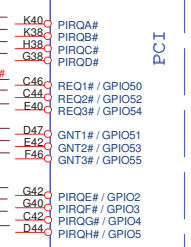
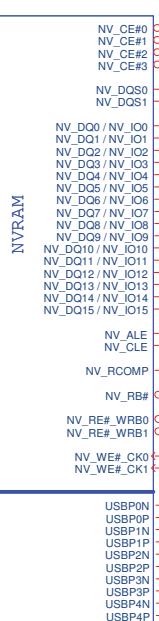
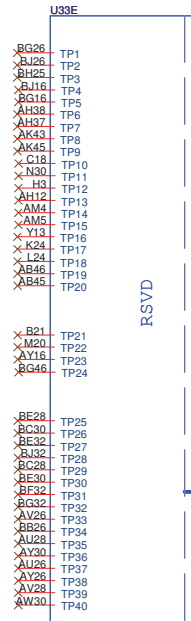
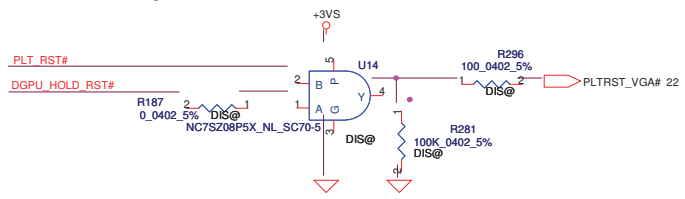
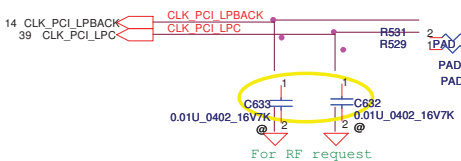
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

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				P5WE0 M/B LA-6901P Schematic
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				Date: Friday, August 27, 2010 Sheet 16 of 39



GPIO51 Internal pull high

Boot BIOS Strap bit1 BBS1			
Bit11	Bit10	Boot BIOS Destination	
GNT1#/GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC



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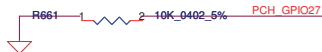
Compal Electronics, Inc.	
PCH (5/9) PCI, USB, NVRAM	
Title	P5WE0 M/B LA-6901P Schematic
Size	0.1
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HDA_SYNC PH (PLL =+1.5VS)
 GPIO28
 On-Die PLL Voltage Regulator
 This signal has a weak internal pull up

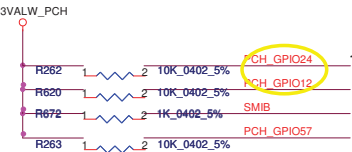
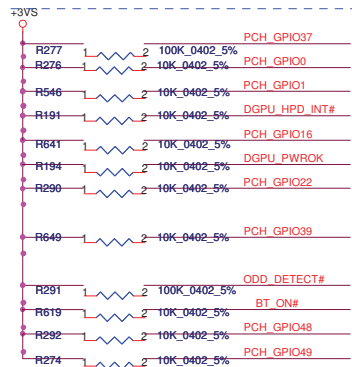
★ H : On-Die voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal
 No use PD to GND Check list1.0 P.70

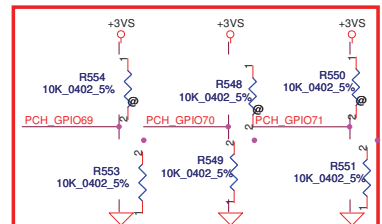
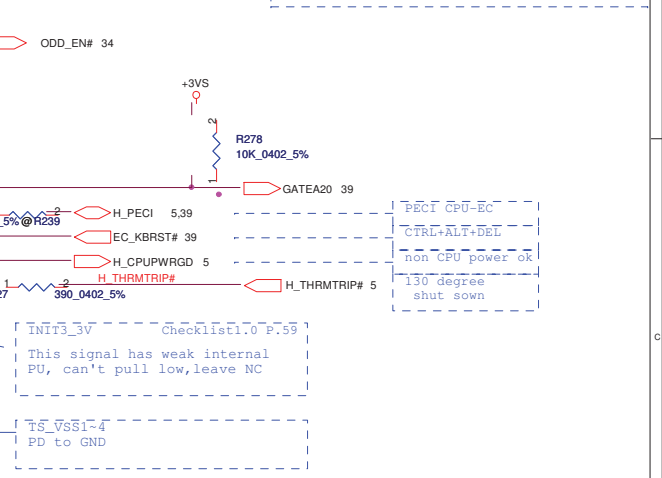
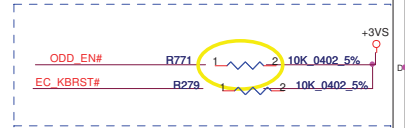
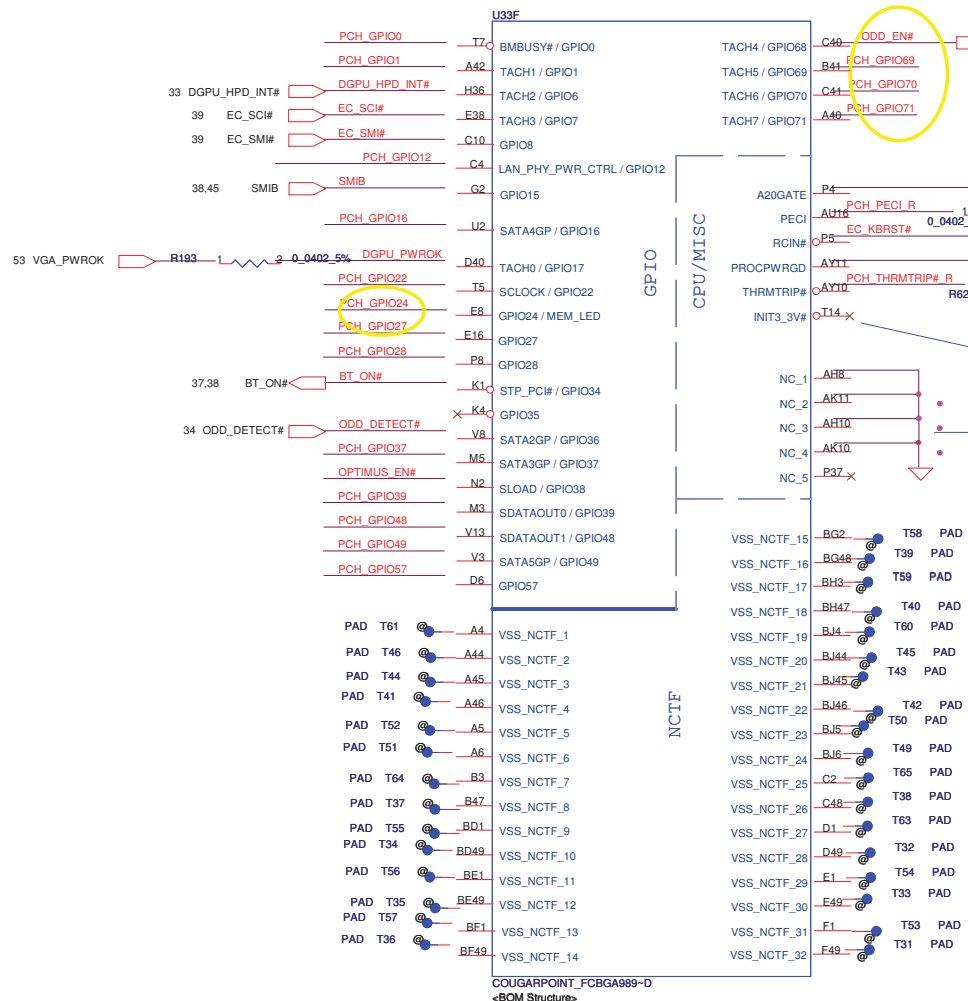


GPIO38	
OPTIMUS_EN#	
★ OPTIMUS	0
Non-OPTIMUS	1

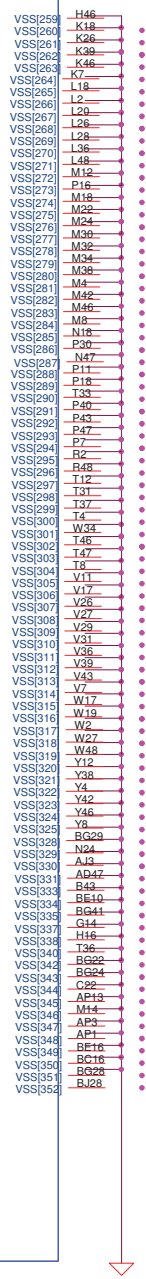
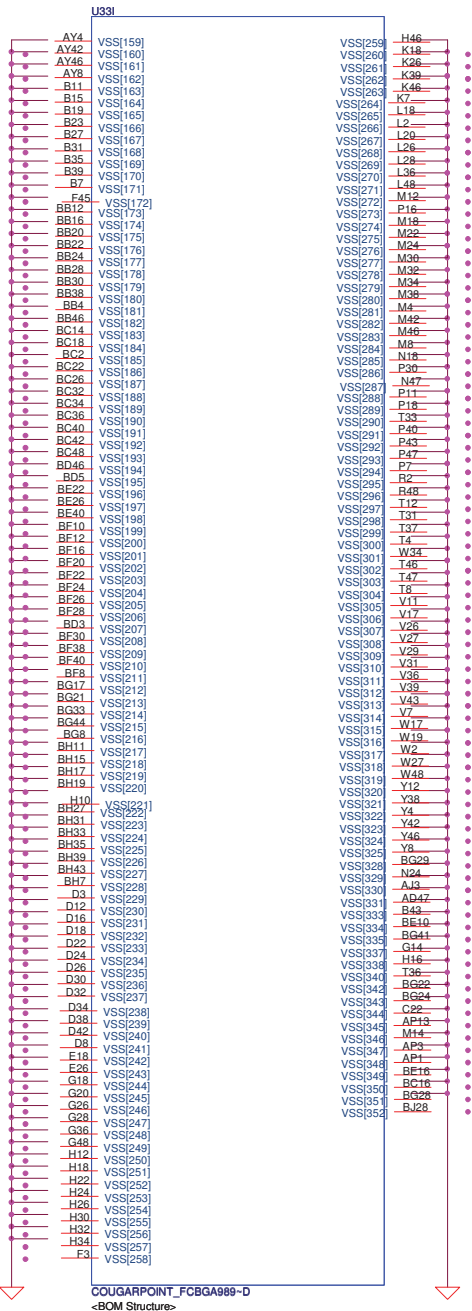
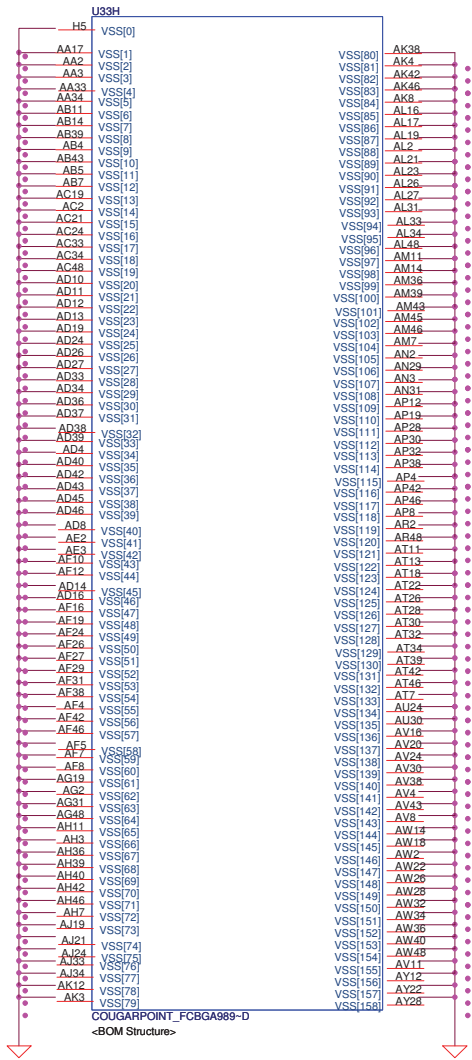


GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

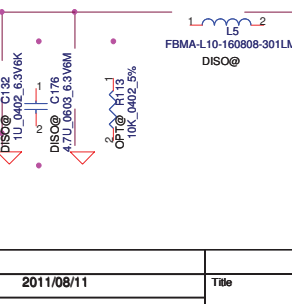
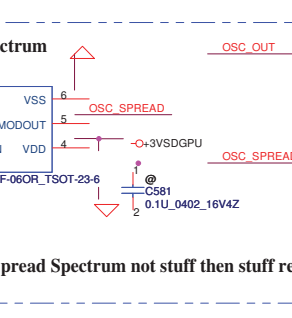
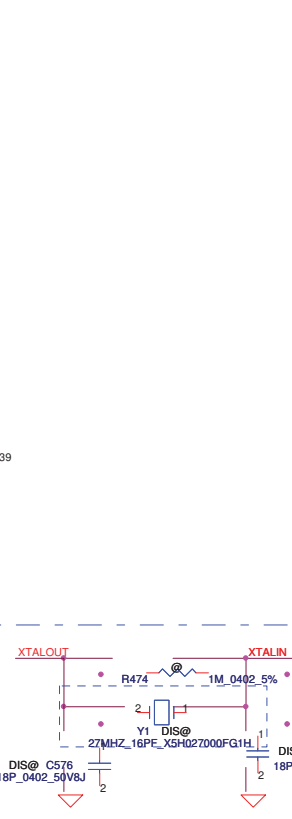
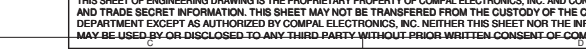
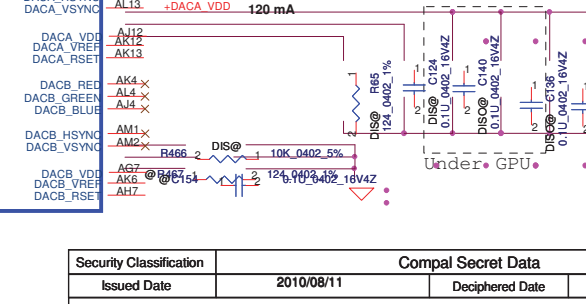
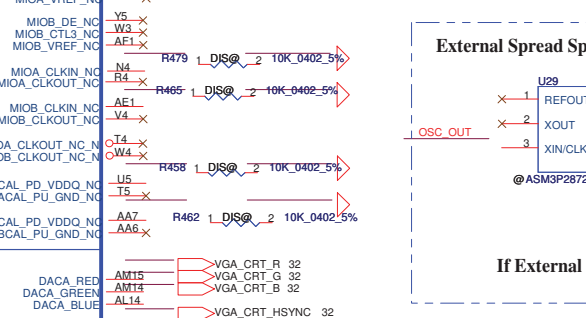
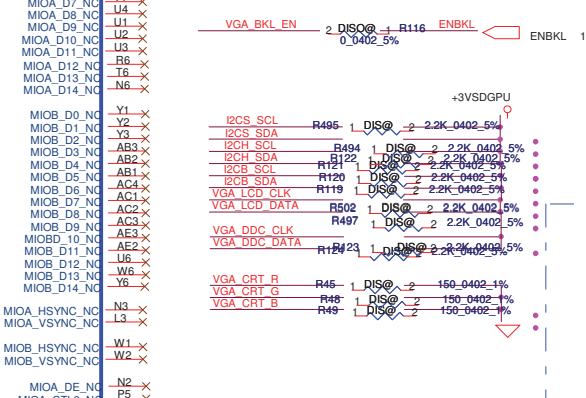
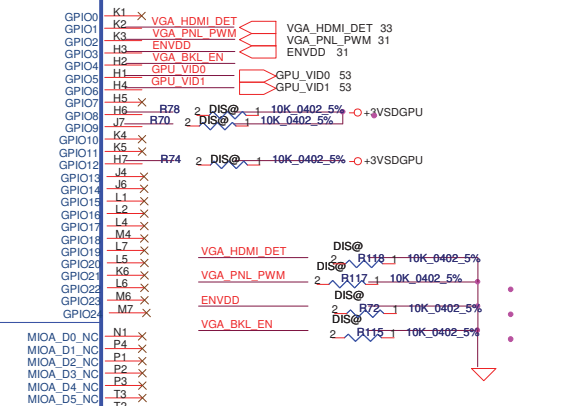
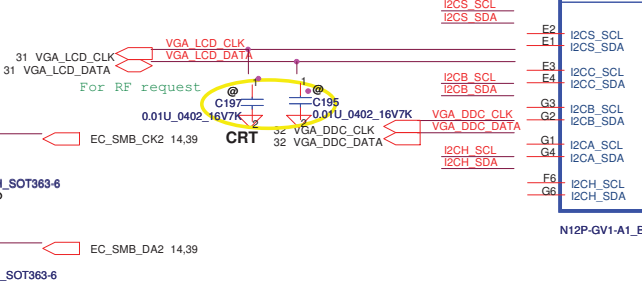
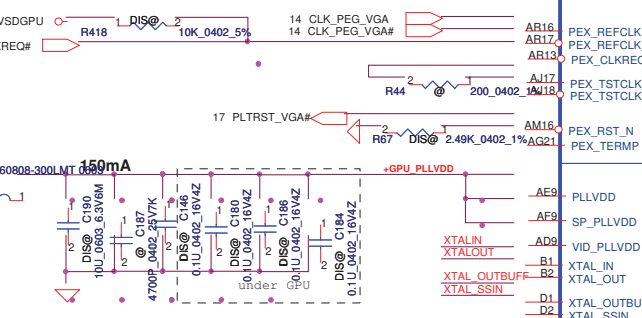
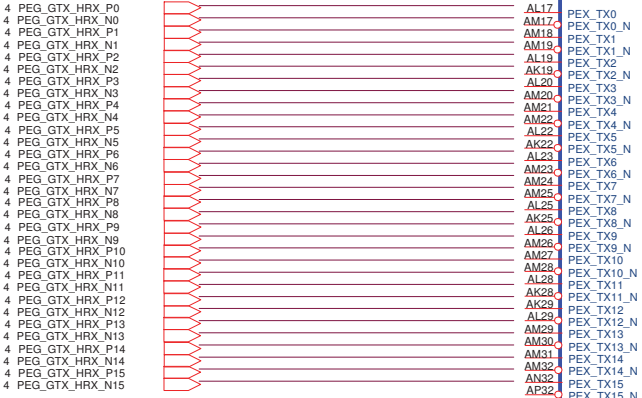
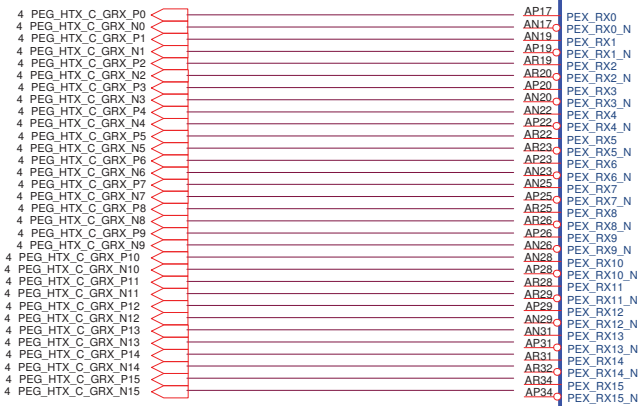
CRB1.0 PH10K to +3VALW



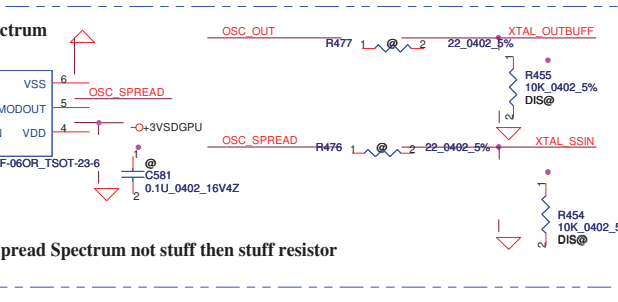
Project ID	GPIO69	GPIO70	GPIO71
★ P5WE0	0	0	0
P7YE0	0	0	0
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1



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GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A



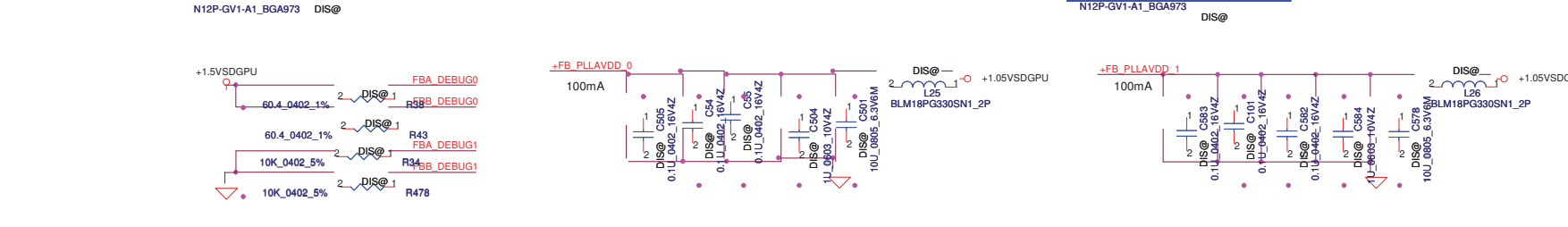
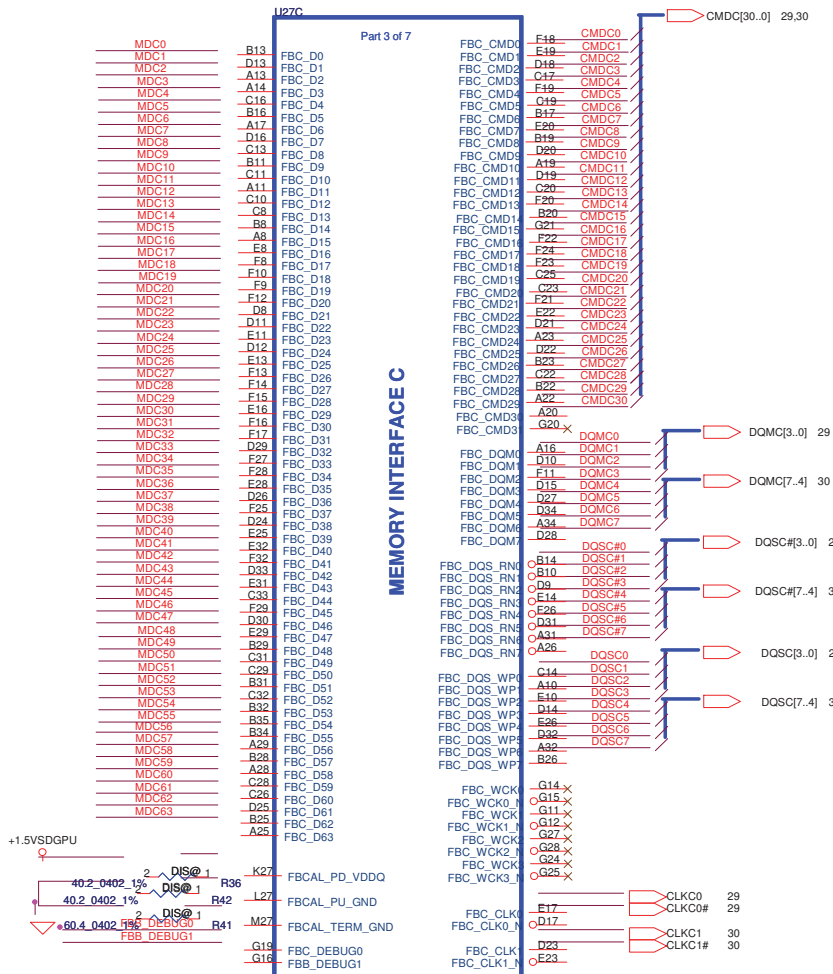
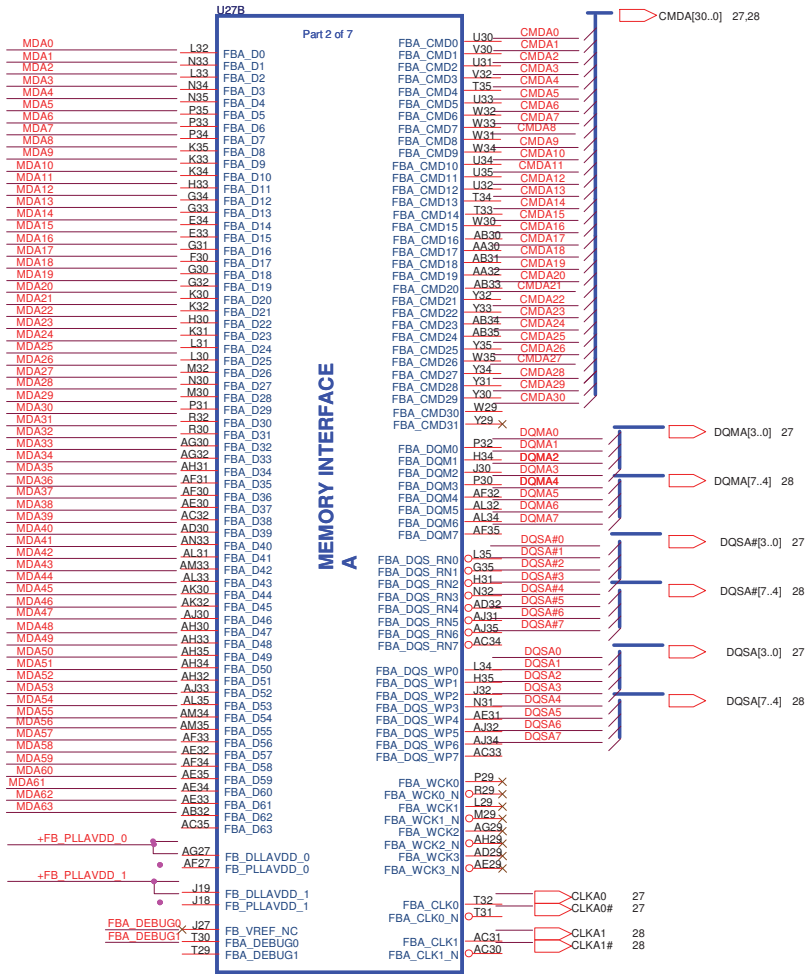
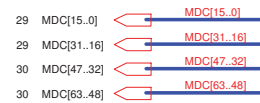
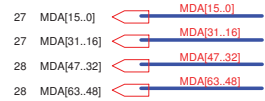
N12P-GV1-A1_BGA973 DIS@

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Issued Date	2010/08/11	Deciphered Date
		2011/08/11

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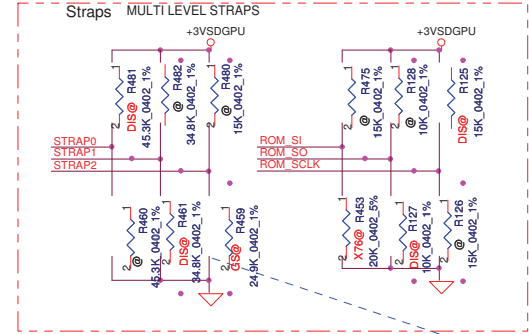
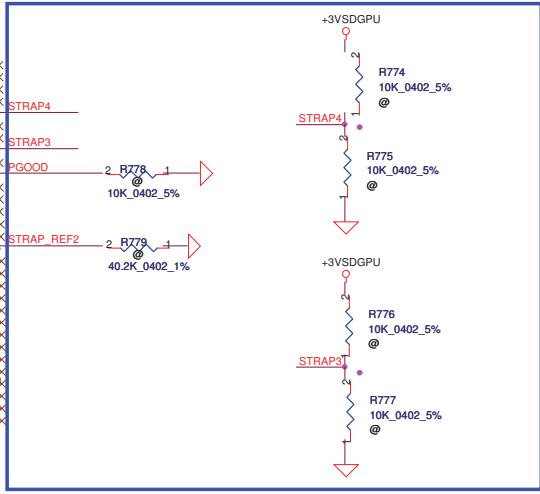
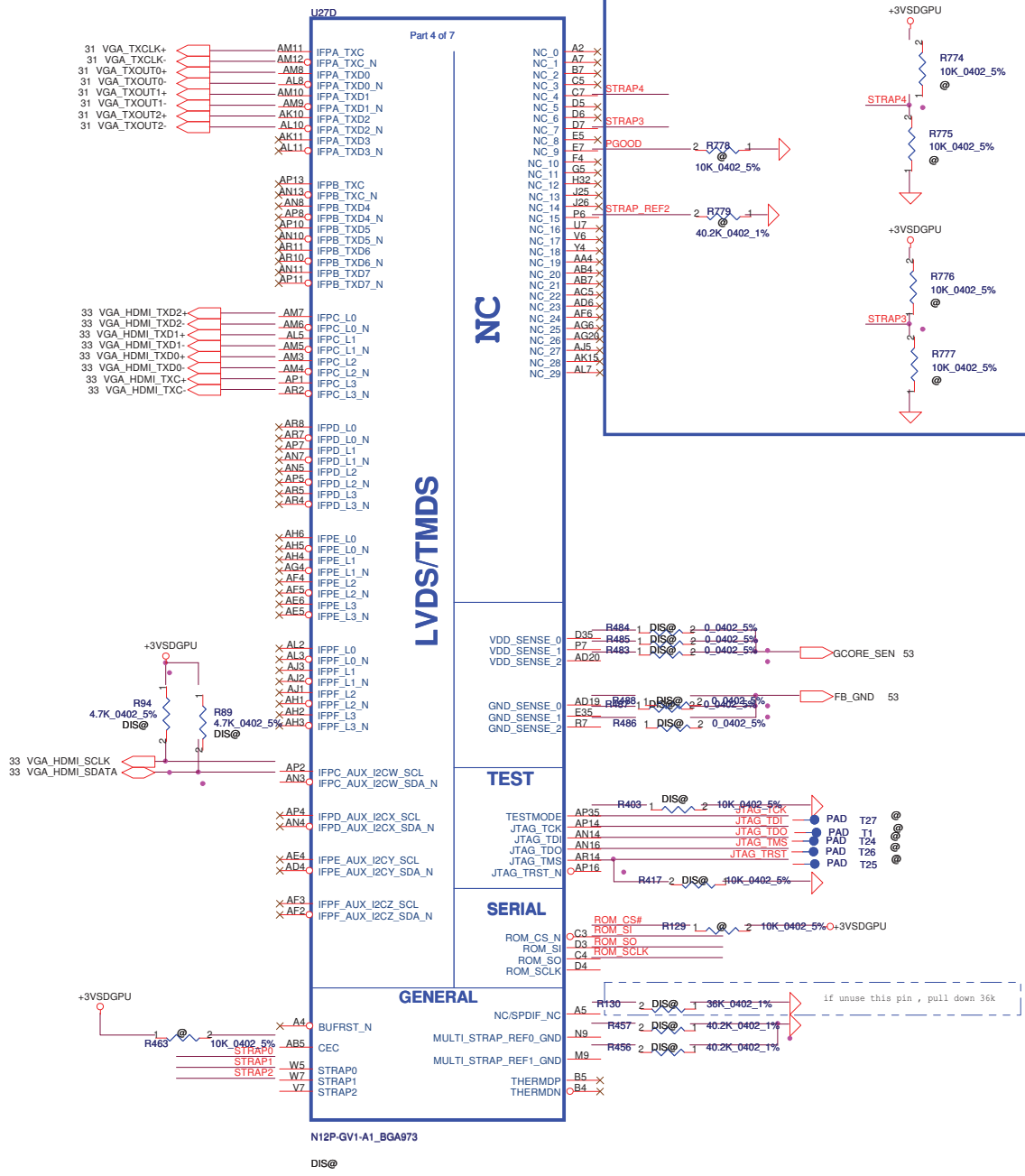
Compal Electronics, Inc.	
N12P PEG 1/9	
Size	Document Number
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VRAM Interface



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Size	Custom	Document Number	PSWE0 M/B LA-6901P Schematic		Rev
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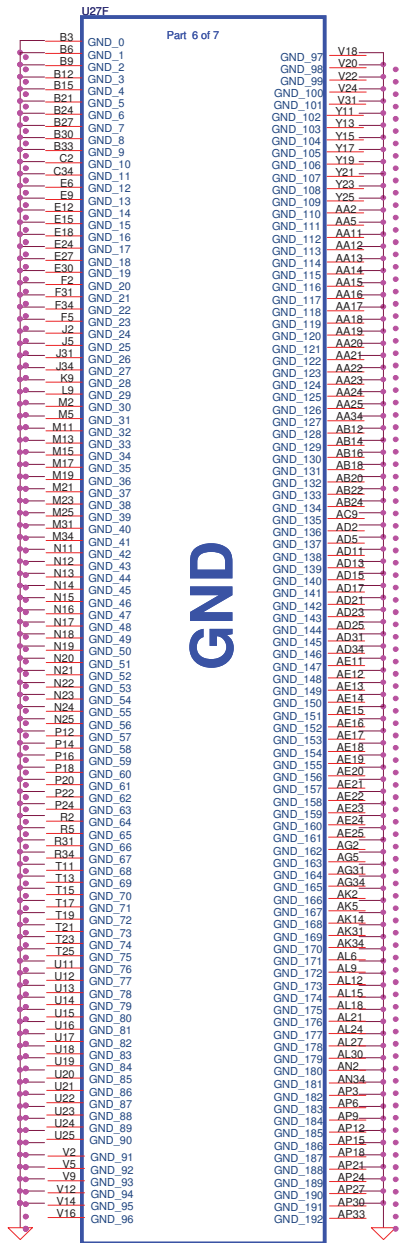
For GB2-128 & GB2b-128 colayout....



N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
128MX16 Samsung	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

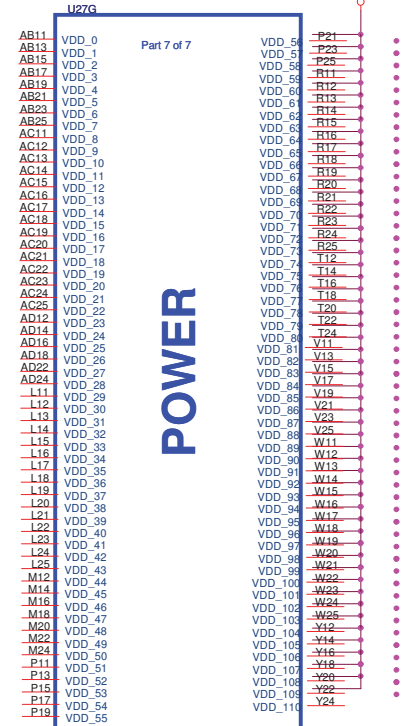
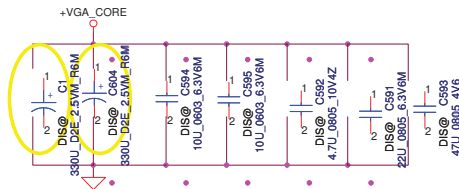
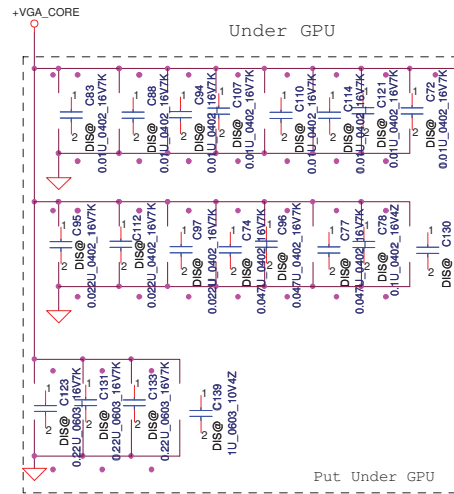
GV@ R459 45K_0402_1%

Strap 2 for GV1, Pull low 45K Ohm



N12P-GV1-A1_BGA973

DIS@



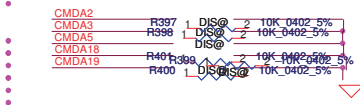
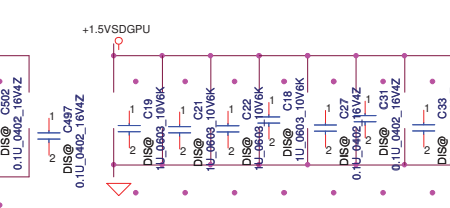
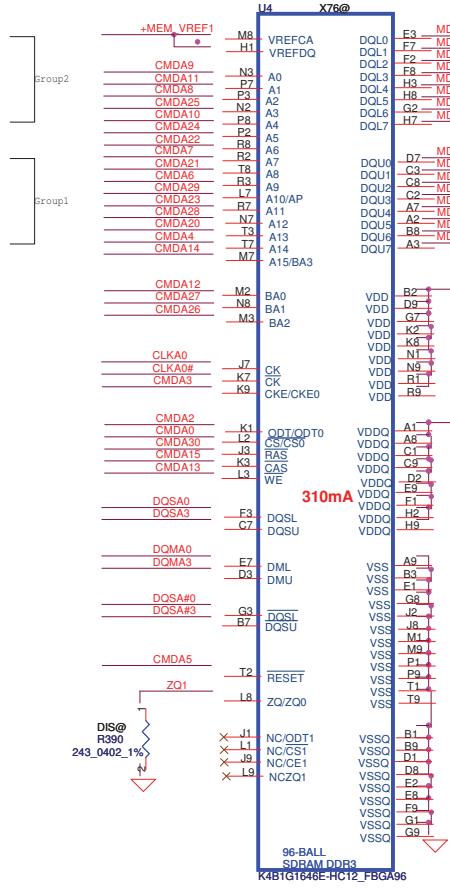
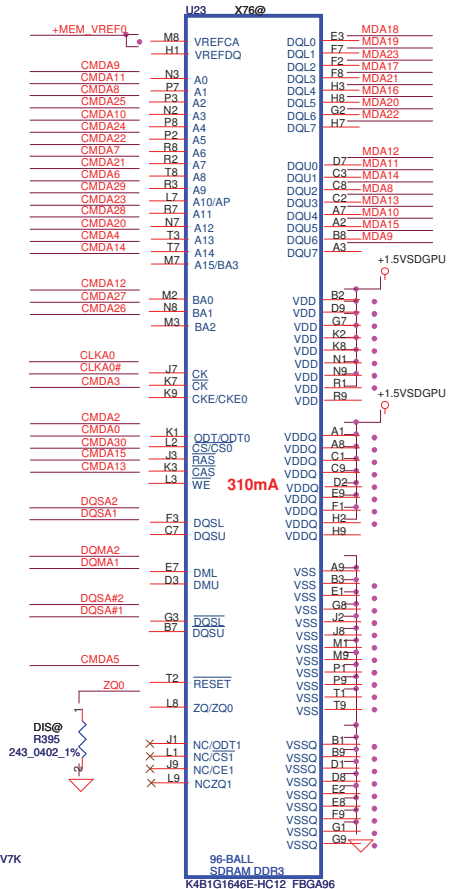
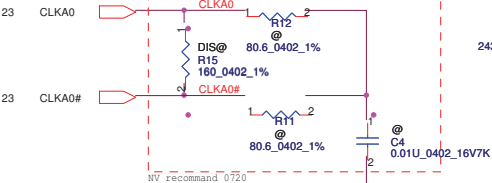
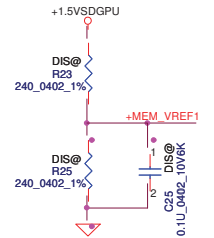
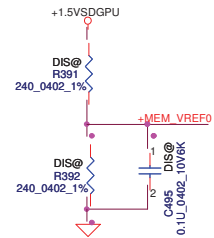
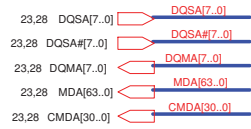
N12P-GV1-A1_BGA973

DIS@

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Size	Document Number	Date		Rev	
Custom	PSWEO/MB LA-6901P Schematic	Friday, August 27, 2010		0.1	
				Sheet	26 of 59

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16	CS0_H#	
CMD17		
CMD18	ODT_H	
CMD19	CKE_H	
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

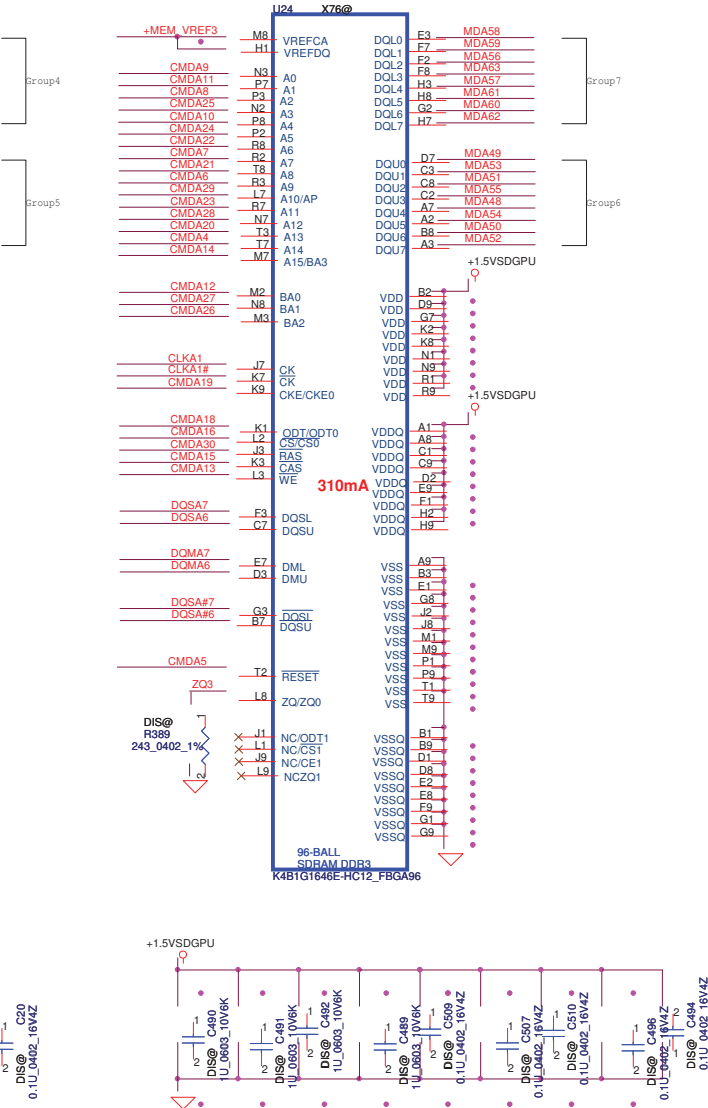
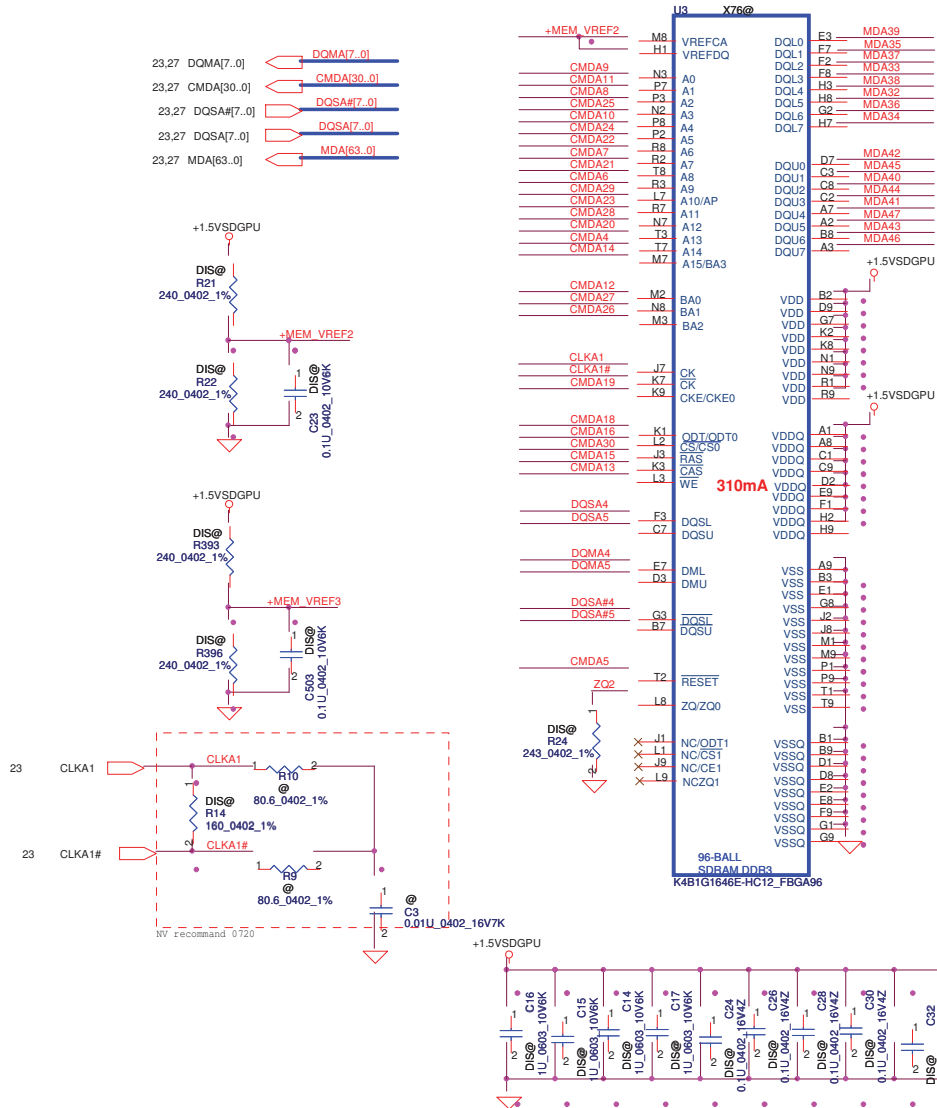
Samsung : SA000035700 (S IC D3 64Mx16 K4W1G1646E-HC12 FBGA 96P)
 Hynix : SA000032400 (S IC D3 64Mx16 H5TQ1G63BFR-12C FBGA 1.5V)
 AMD : SA00003PF10
 (S IC D3 64M16/800 23EY2387MB-12 PG-TFPGA 96P 1.5V)

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

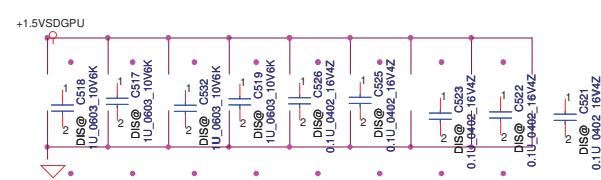
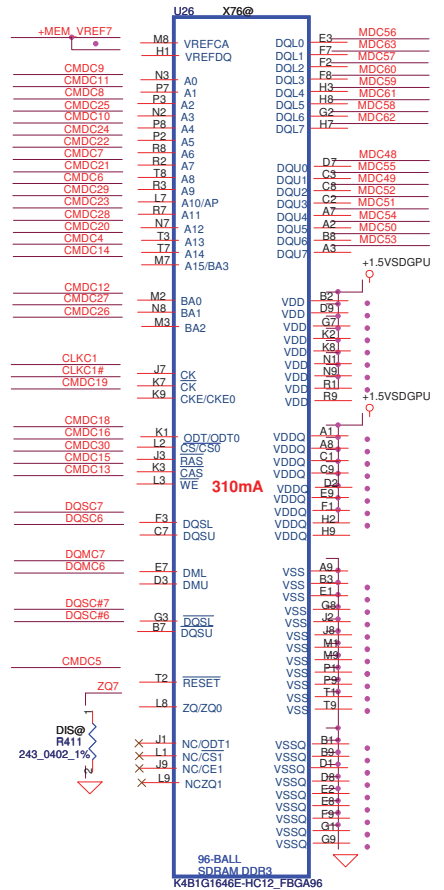
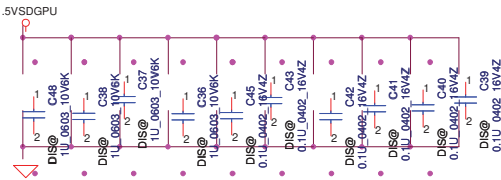
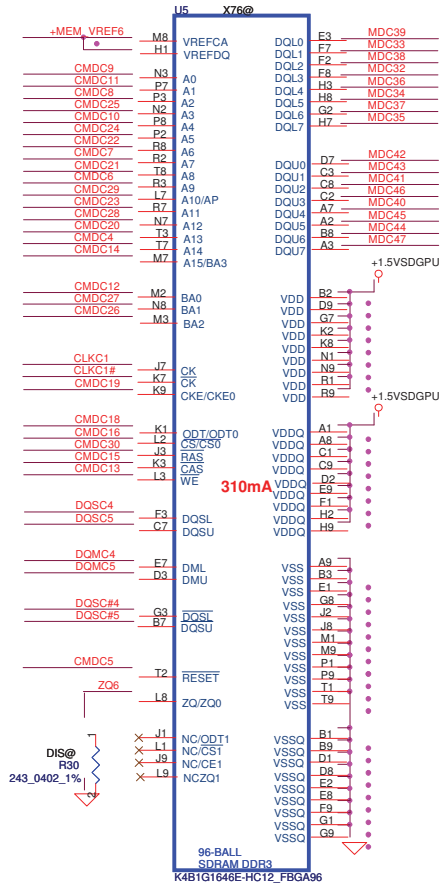
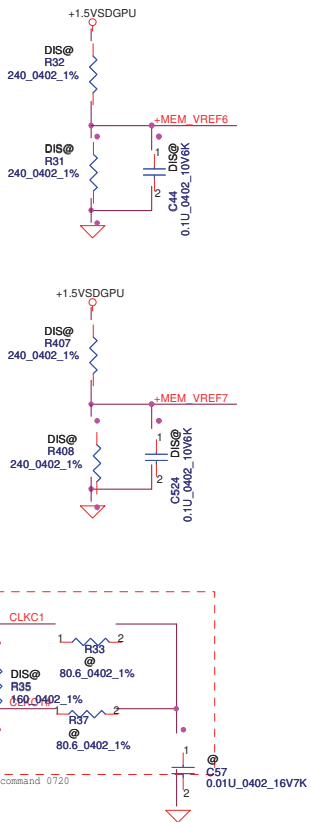
LOW HIGH



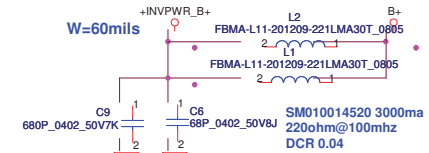
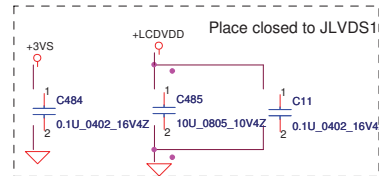
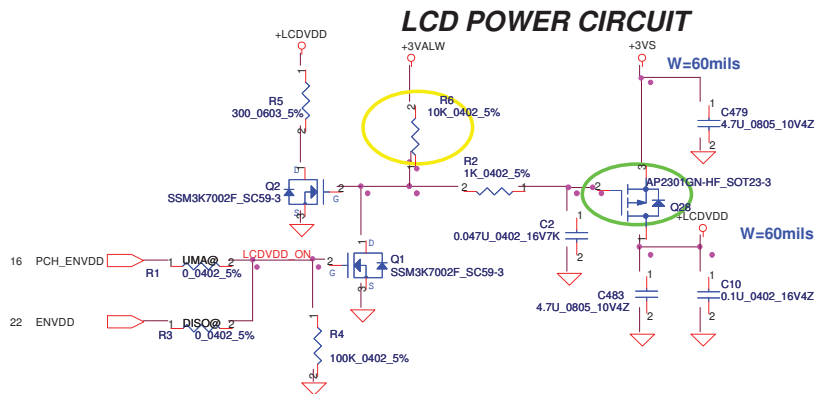
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

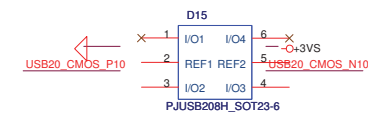
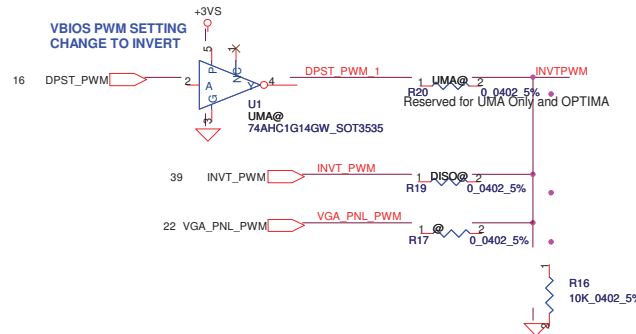
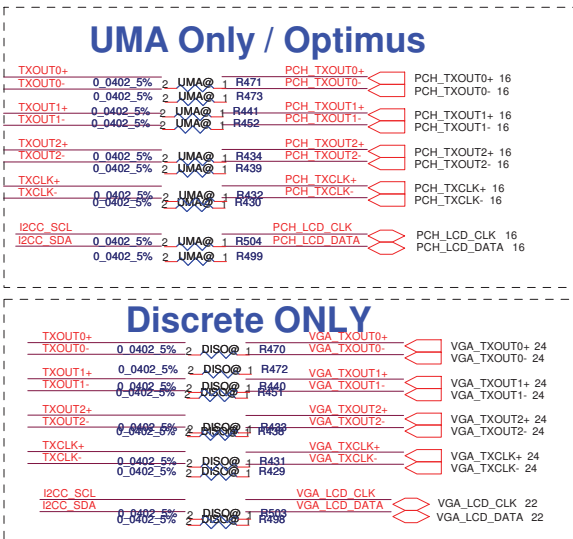
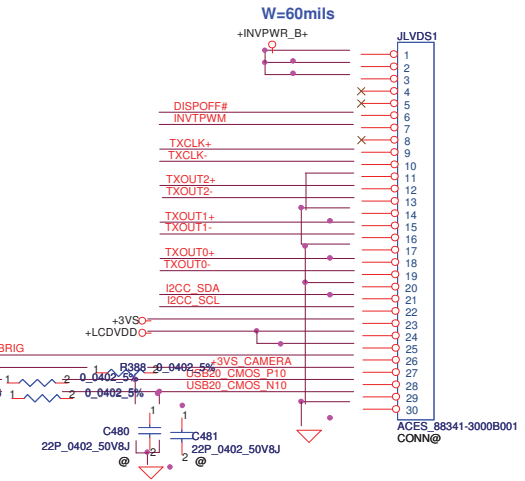
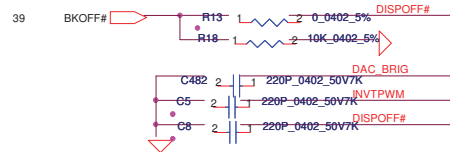
- 23.29 DQMC[7..0] DOMC[7..0]
- 23.29 CMDC[30..0] CMDC[30..0]
- 23.29 DQSC# [7..0] DQSC# [7..0]
- 23.29 DQSC[7..0] DQSC[7..0]
- 23.29 MDC[63..0] MDC[63..0]



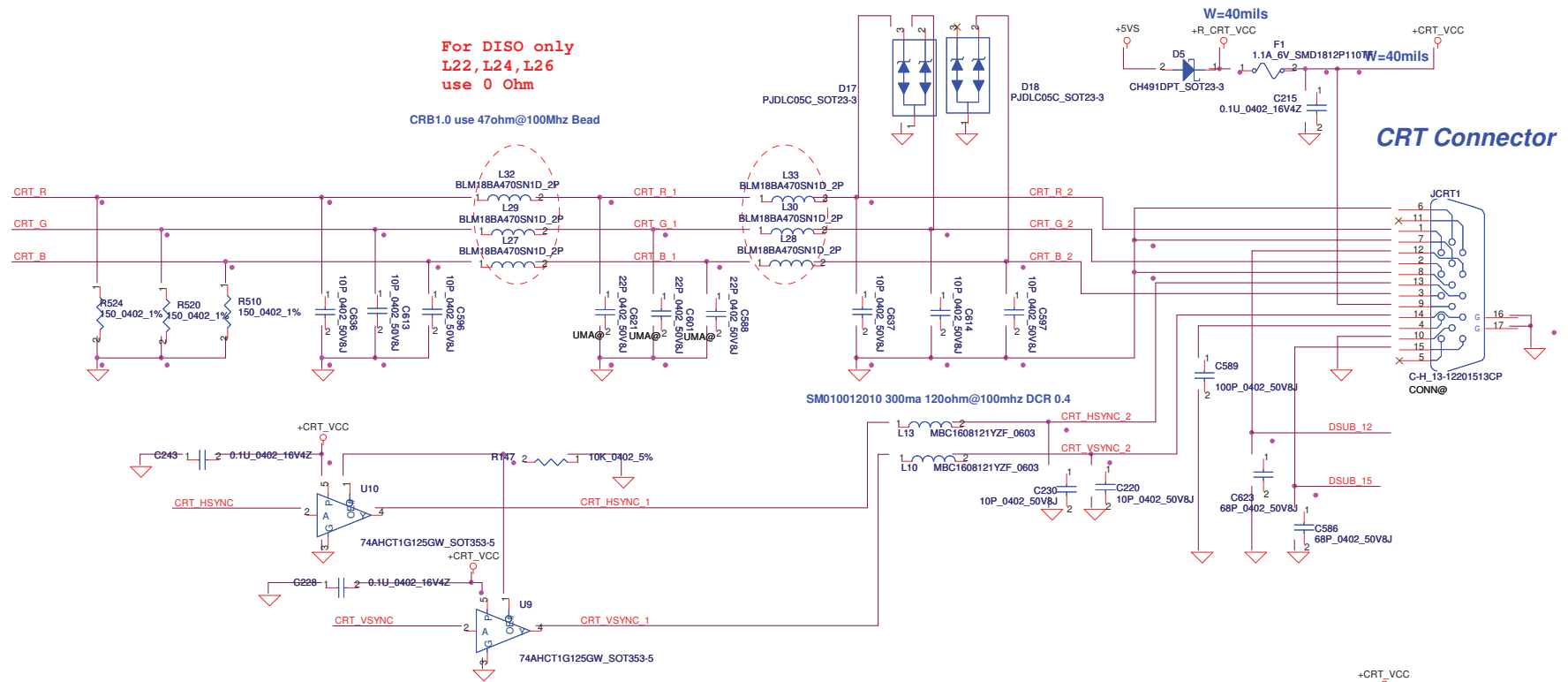
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18	ODT_H	
CMD19	CKE_H	
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH



LCD/LED PANEL Conn.



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For DISO only
L22, L24, L26
use 0 Ohm

CRB1.0 use 47ohm@100Mhz Bead

W=40mils

CRT Connector

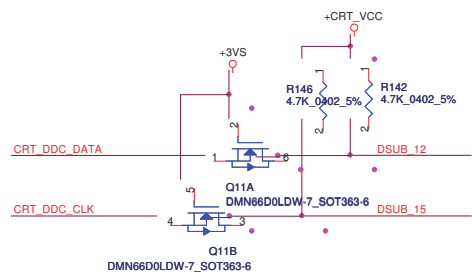
SM010012010 300ma 120ohm@100mhz DCR 0.4

UMA Only / OPTIMUS

16	PCH_CRT_R	PCH_CRT_R	R420	UMA@	0_0402_5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R424	UMA@	0_0402_5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R422	UMA@	0_0402_5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R428	UMA@	33_0402_5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R426	UMA@	33_0402_5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R506	UMA@	0_0402_5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R501	UMA@	0_0402_5%	CRT_DDC_DATA

Discrete only

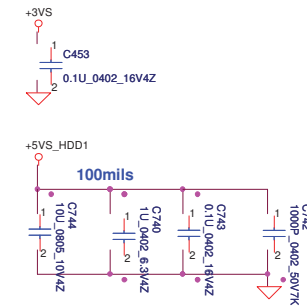
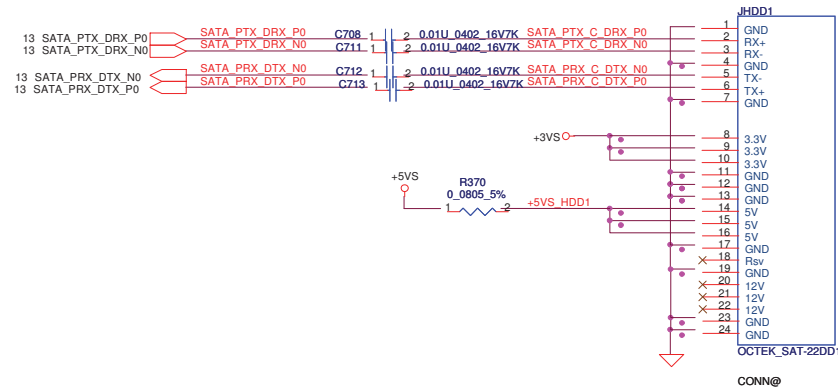
22	VGA_CRT_R	VGA_CRT_R	R419	DISO@	0_0402_5%	CRT_R
22	VGA_CRT_G	VGA_CRT_G	R423	DISO@	0_0402_5%	CRT_G
22	VGA_CRT_B	VGA_CRT_B	R421	DISO@	0_0402_5%	CRT_B
22	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R427	DISO@	0_0402_5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R425	DISO@	0_0402_5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA_DDC_CLK	R505	DISO@	0_0402_5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA_DDC_DATA	R500	DISO@	0_0402_5%	CRT_DDC_DATA



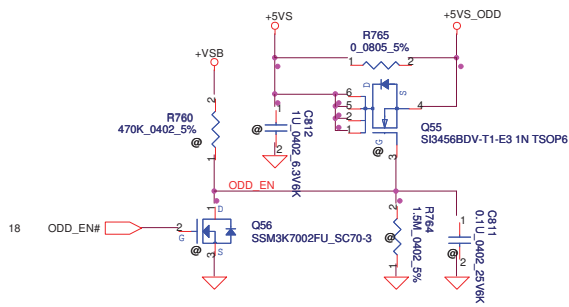
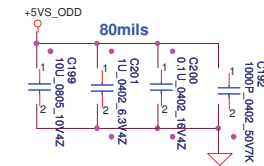
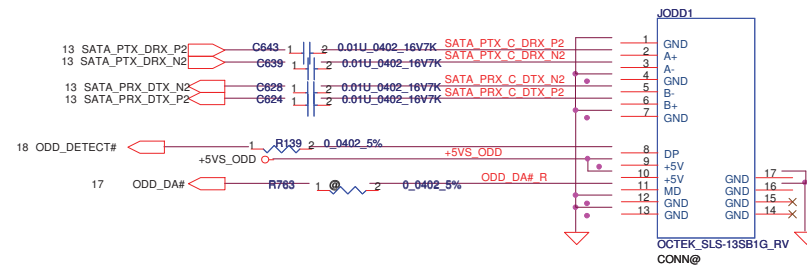
Security Classification		Compal Secret Data		Title	
Issued Date	2010/08/11	Deciphered Date	2011/08/11	CRT Connector	
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				Customer	0.1
				Date	Sheet
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SATA HDD1 Conn.

CL 4.0 mm

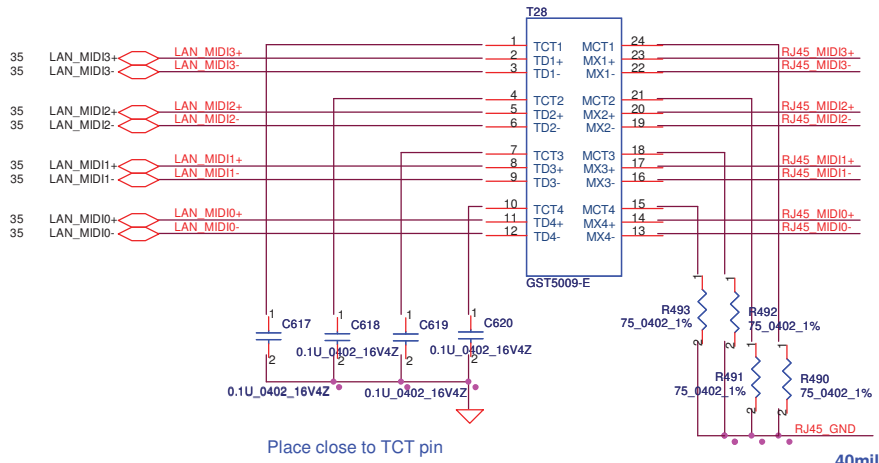


SATA ODD Conn.

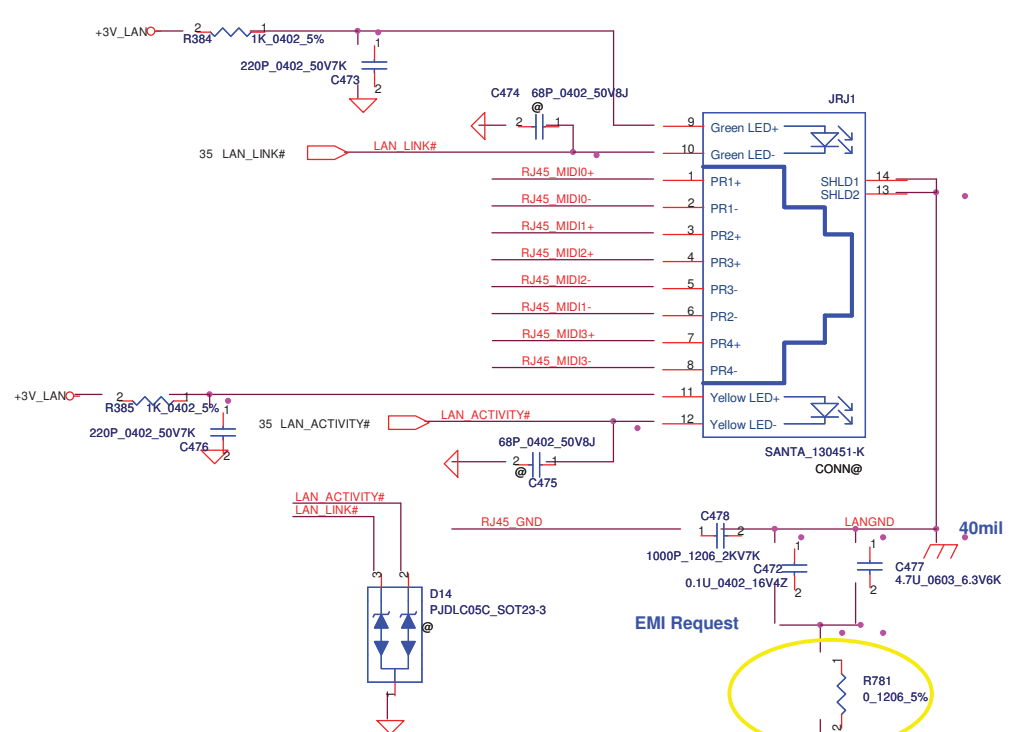


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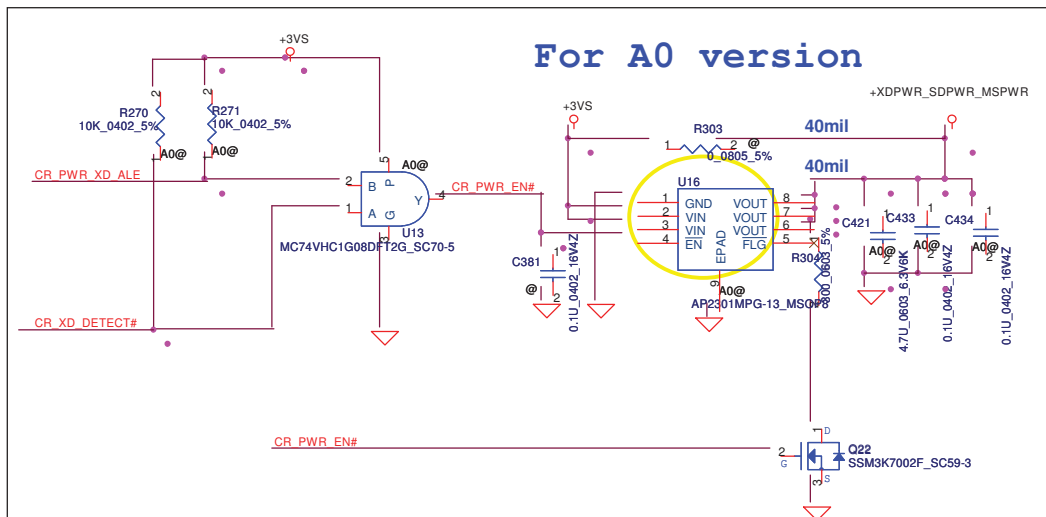
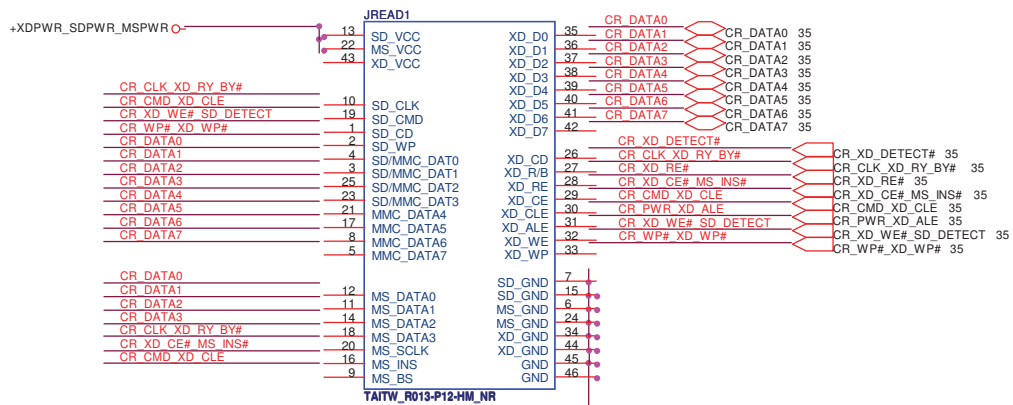
LAN Connector



BOTHHAND: S X'FORM_GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_IH-160 LAN, SP050006F00

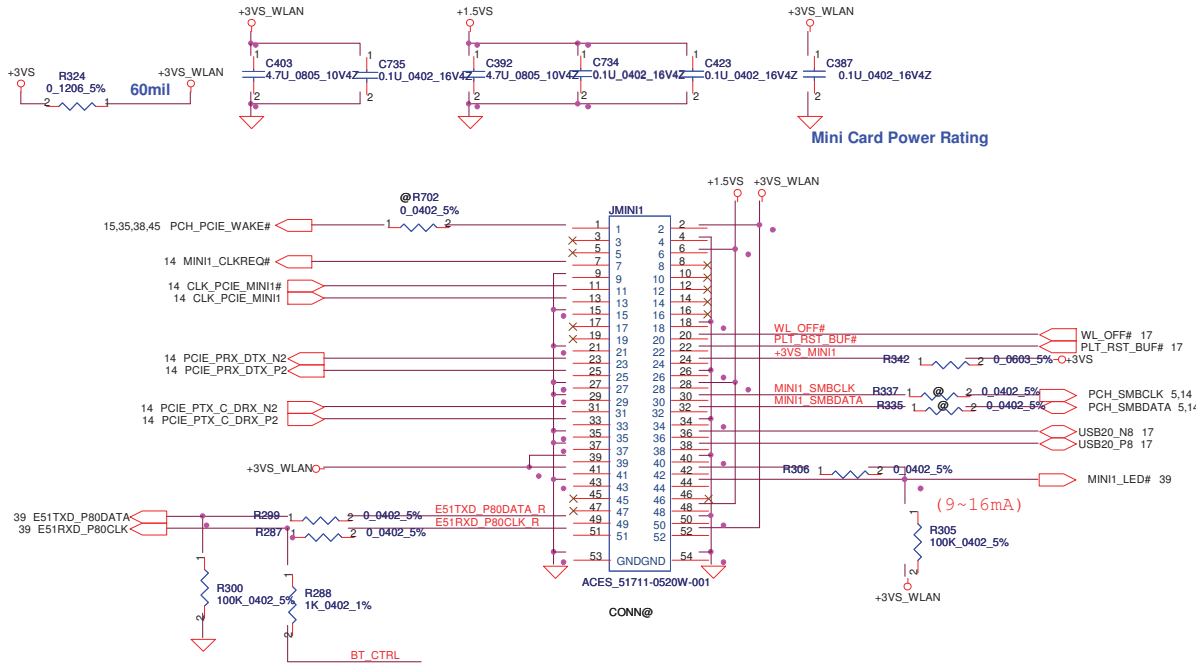


Card Reader Connector

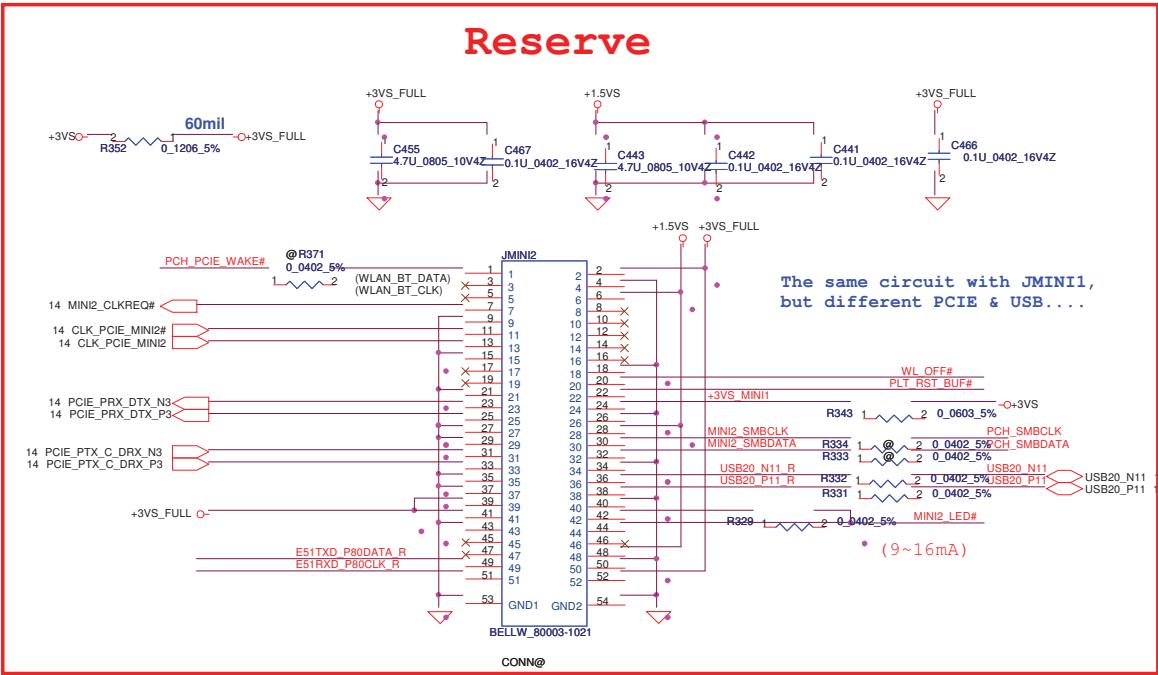
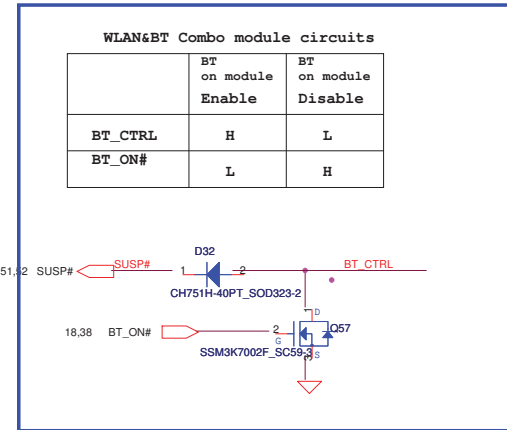


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				LAN Magnetic & RJ45	
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				Custom	P5WE0 M/B LA-6901P Schematic
				Date:	Friday, August 27, 2010
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For Wireless LAN

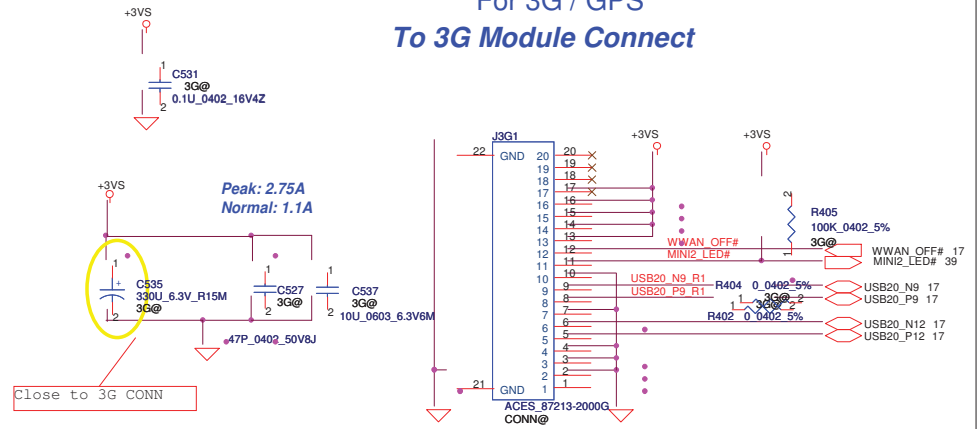


Mini Card Power Rating



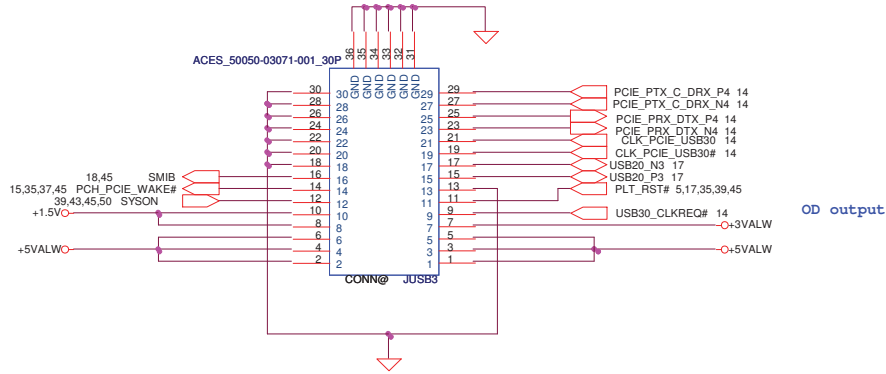
The same circuit with JMINI1, but different PCIE & USB....

For 3G / GPS To 3G Module Connect

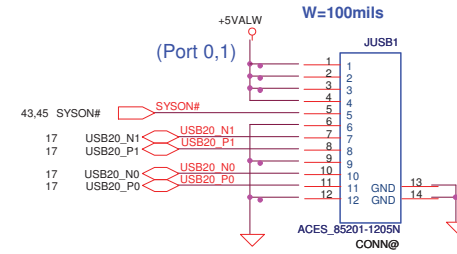


Close to 3G CONN

USB3.0 Conn.

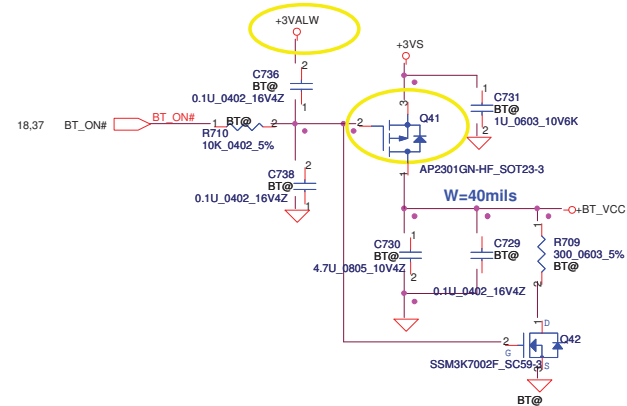
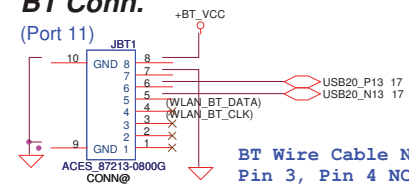


USB/B Conn.

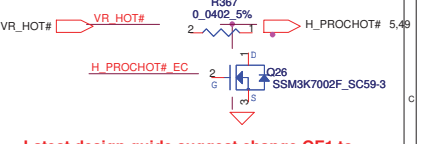
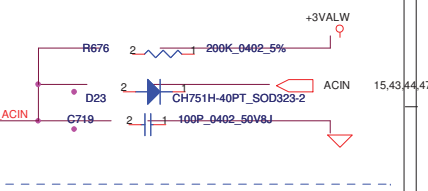
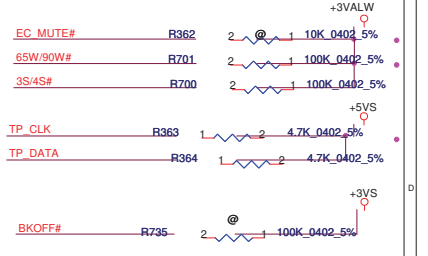
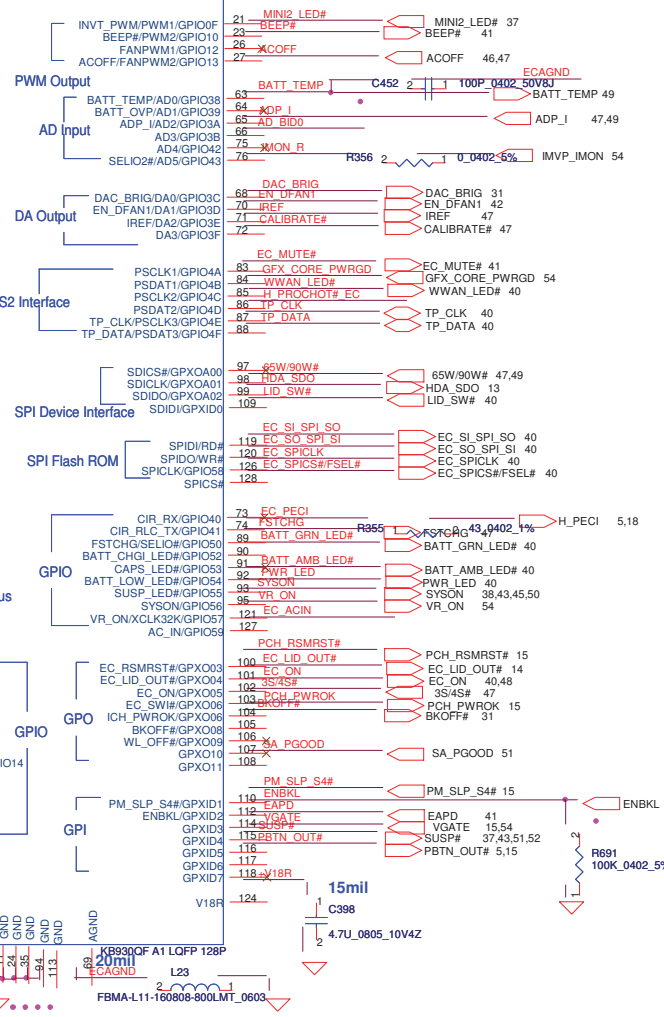
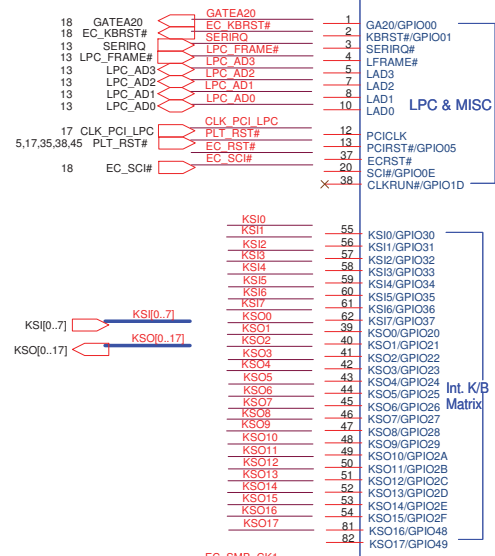
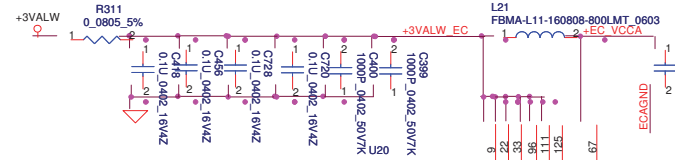
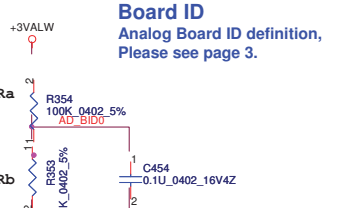
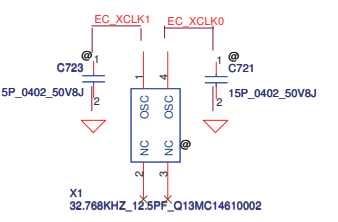
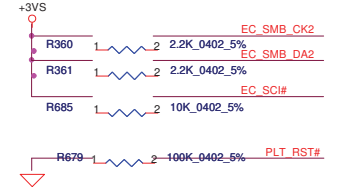
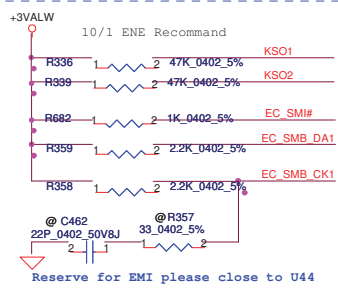
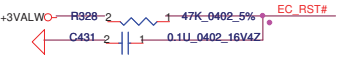
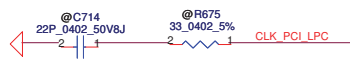


BT Conn.

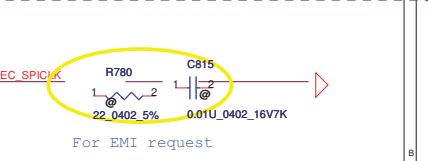
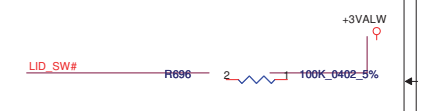
(Port 11)



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Date: Friday, August 27, 2010				Sheet 38 of 50

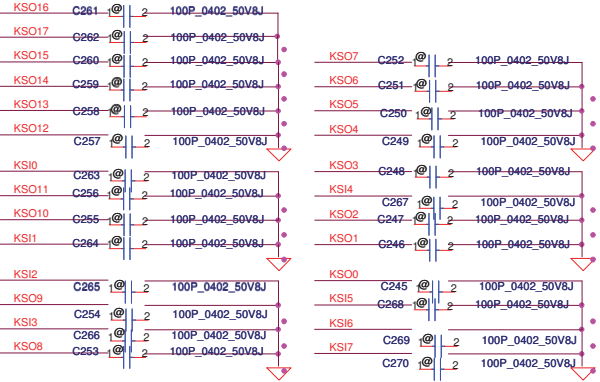
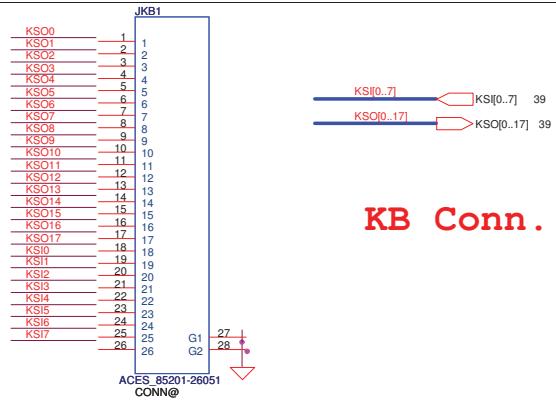
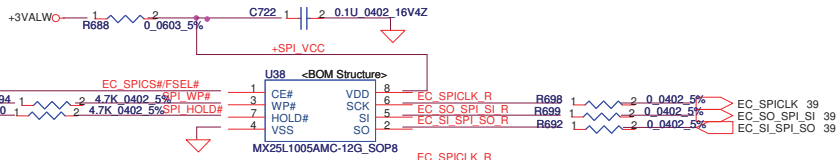


Latest design guide suggest change QE1 to 74LVC1G06.



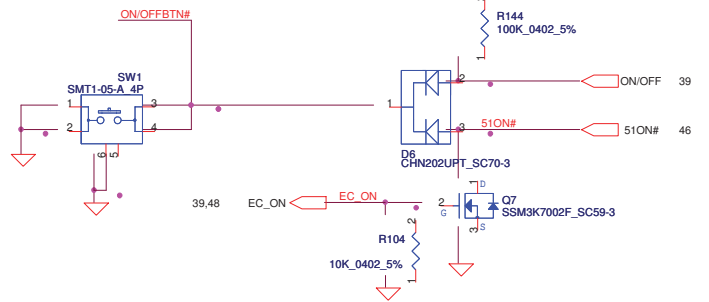
Board ID Analog Board ID definition, Please see page 3.

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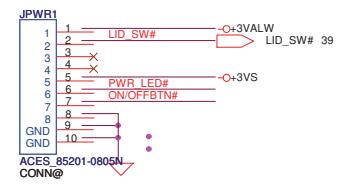


KB Conn.

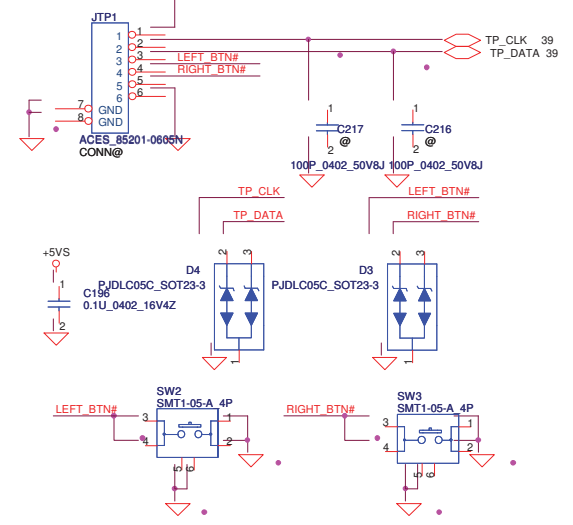
ON/OFF BTN



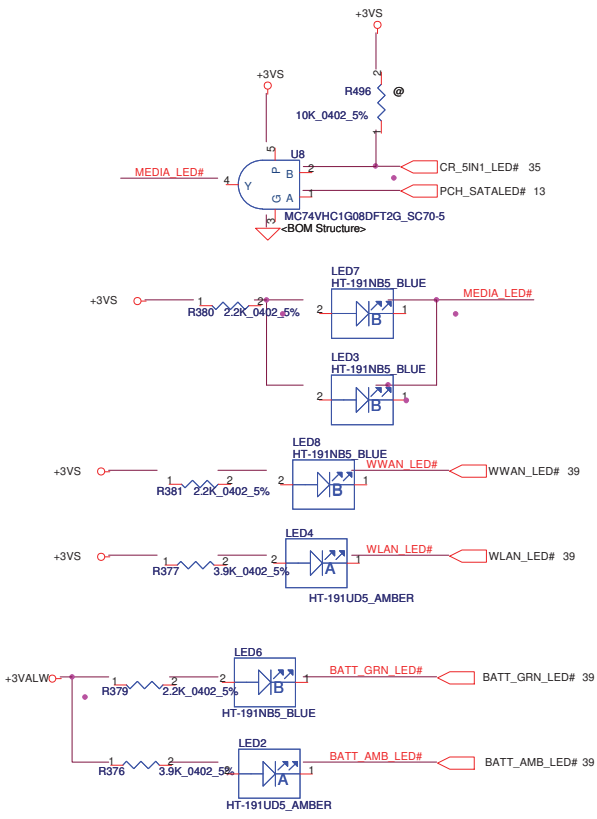
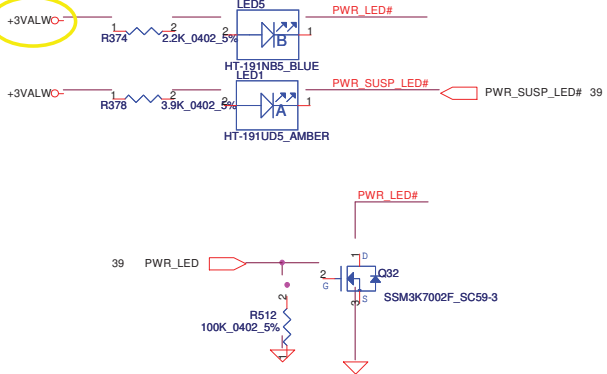
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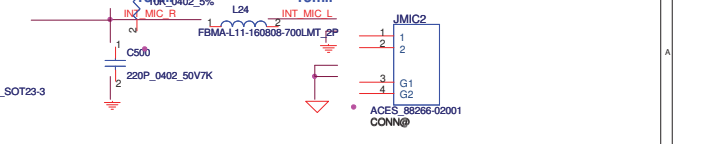
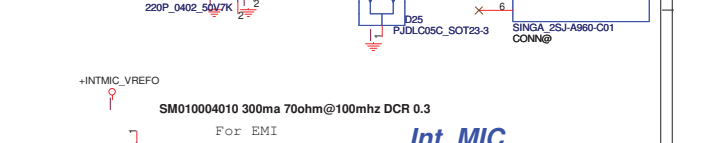
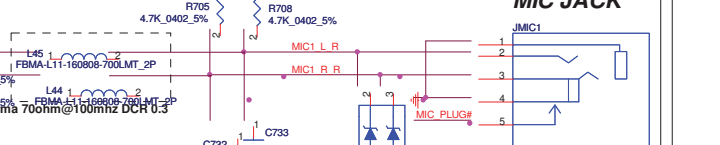
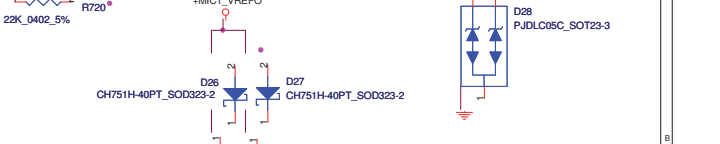
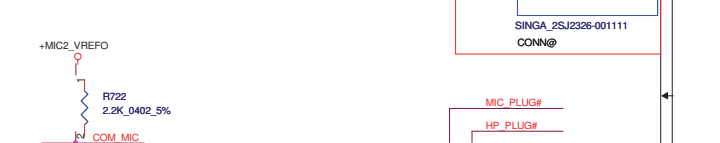
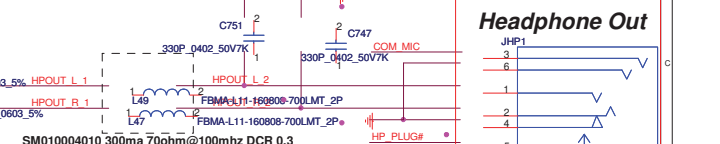
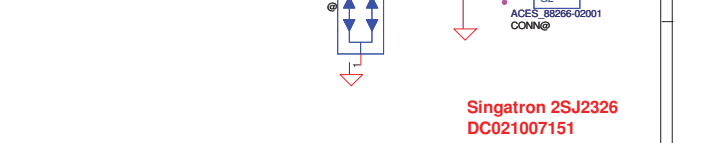
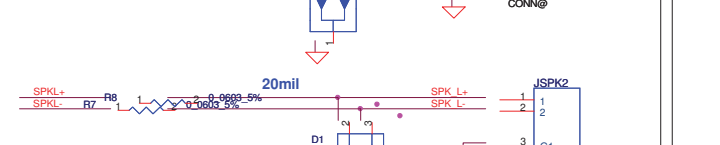
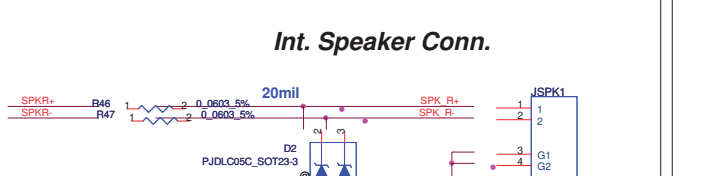
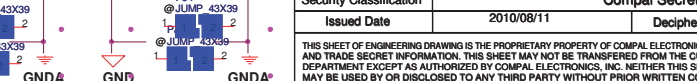
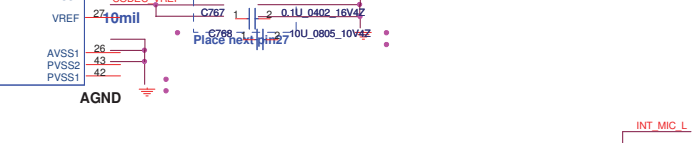
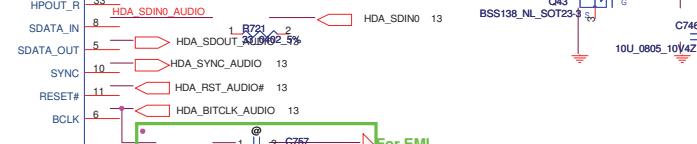
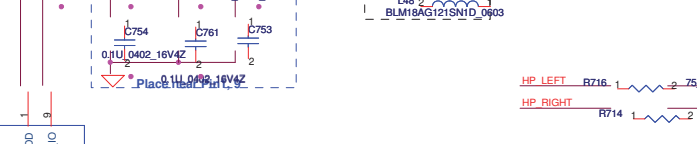
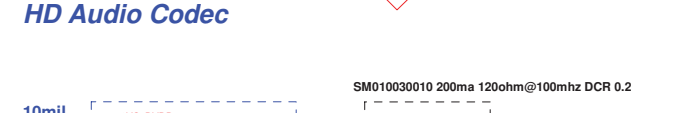
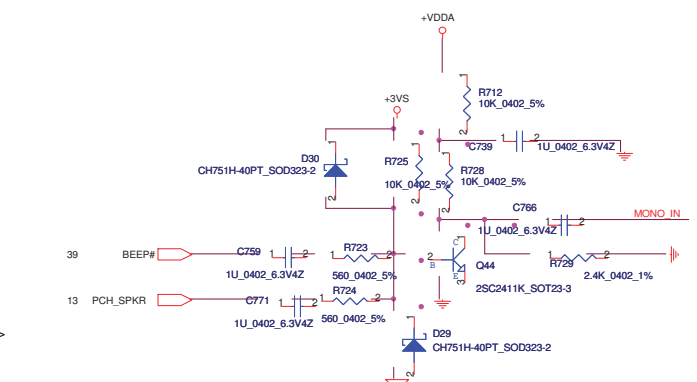
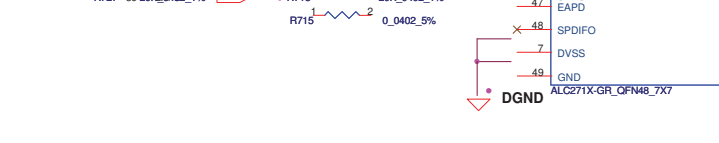
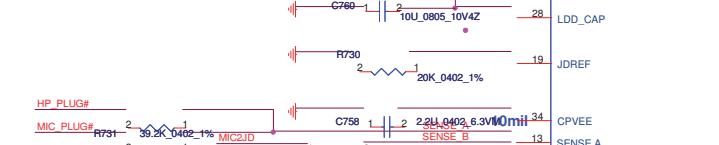
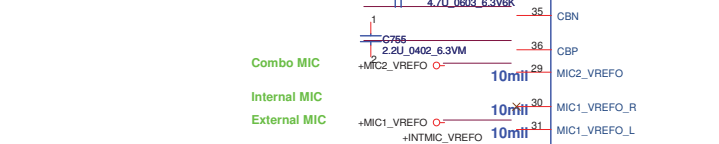
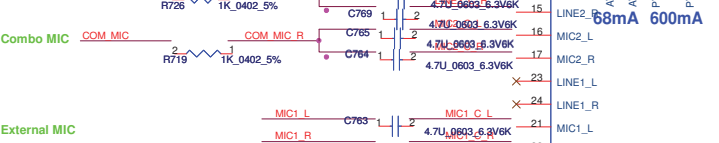
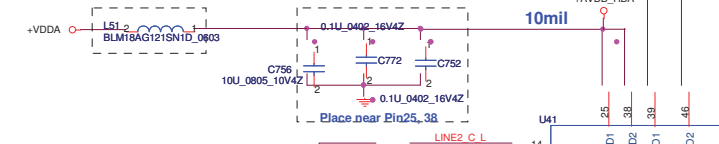
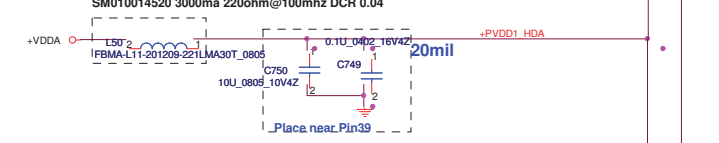
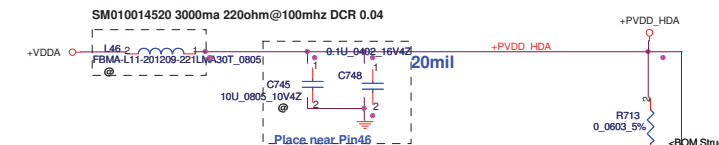
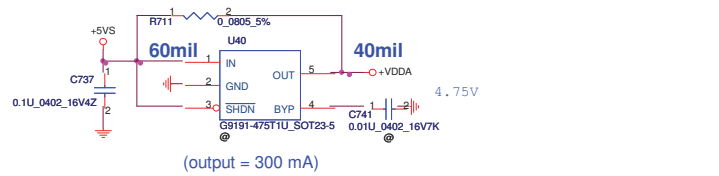
TP Conn.



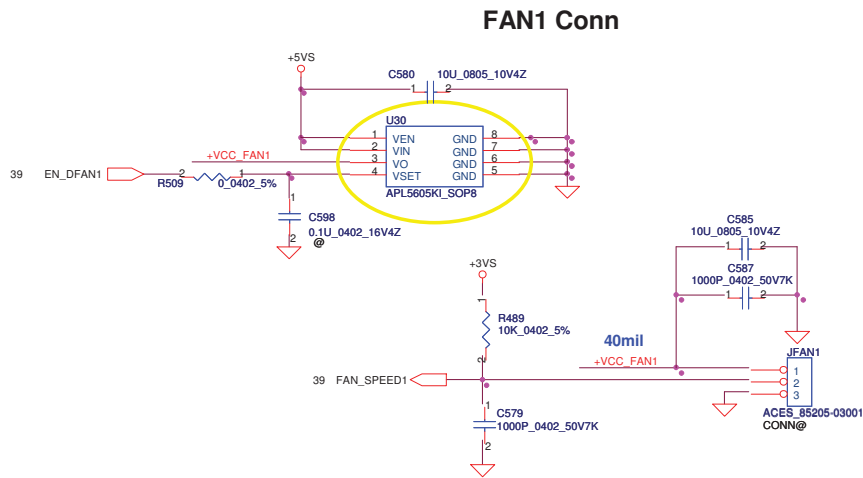
EC Request



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Customer # P5WE0 M/B LA-6901P Schematic				Rev 0.1
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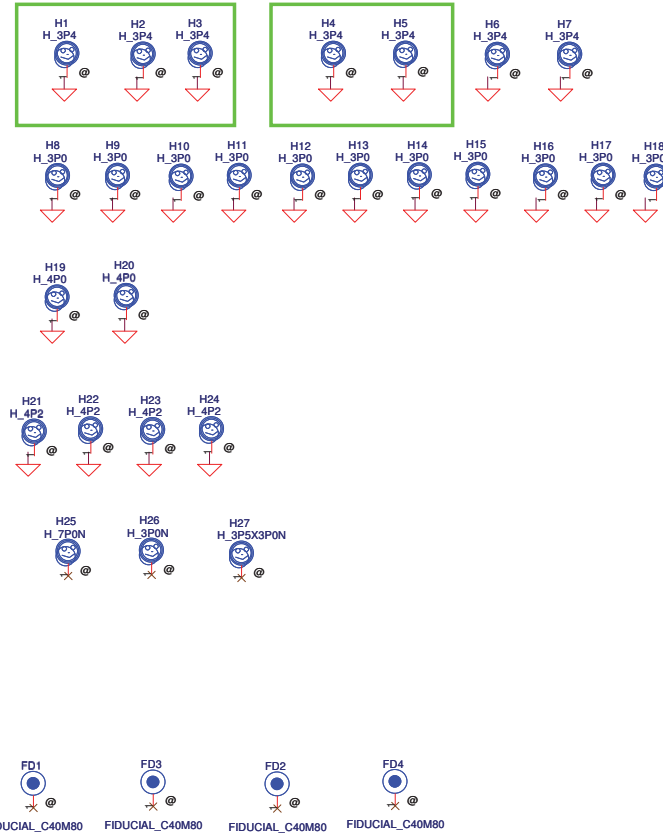


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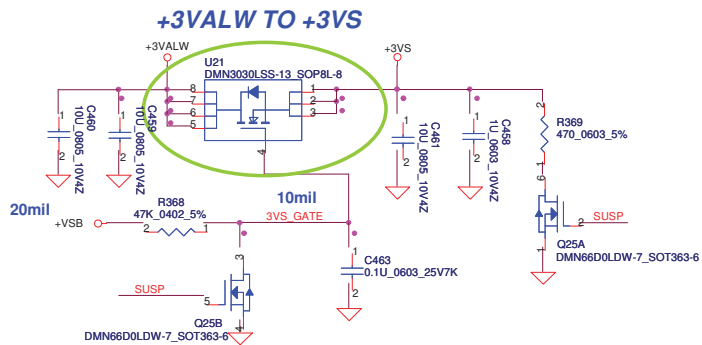
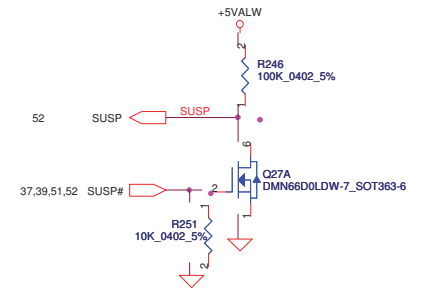
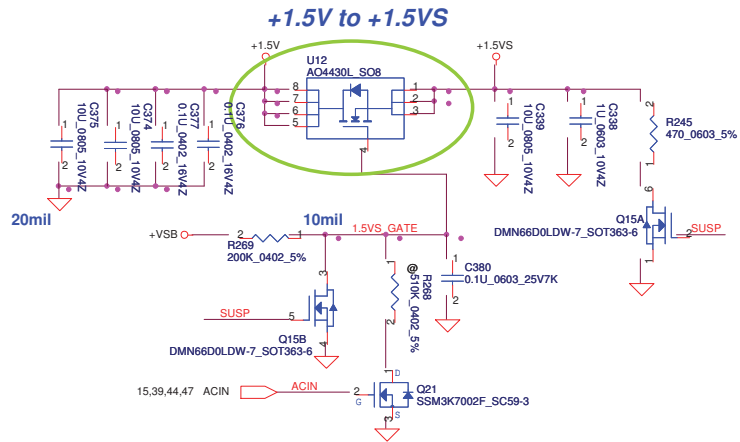
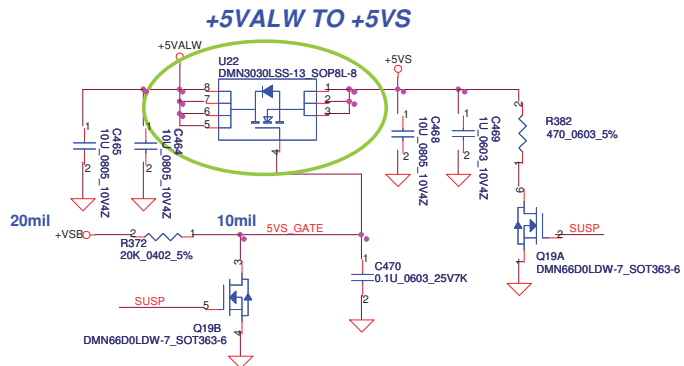


FAN Stand-Off

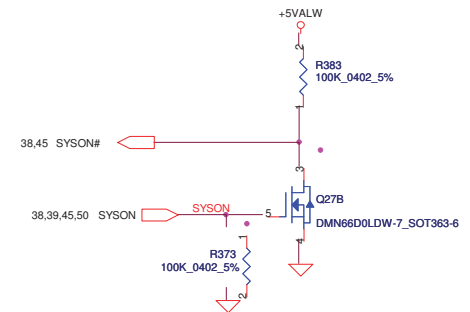
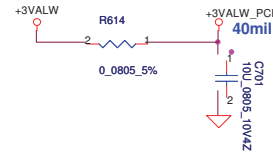
JUSB3 Stand-Off



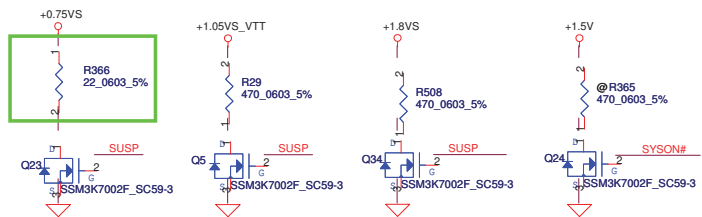
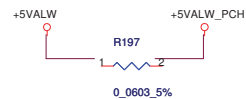
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+3VALW TO +3VALW_PCH(PCH AUX Power)

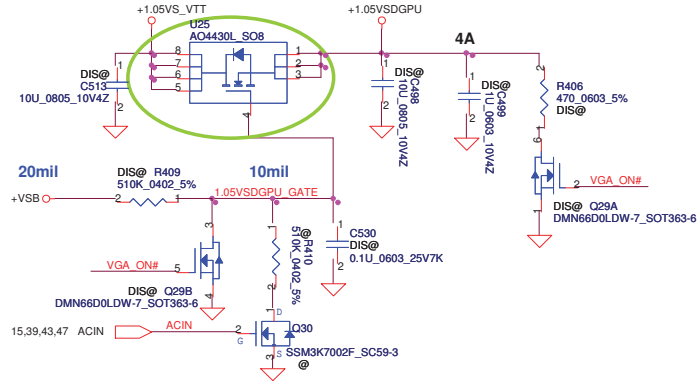


+5VALW TO +5VALW_PCH(PCH AUX Power)

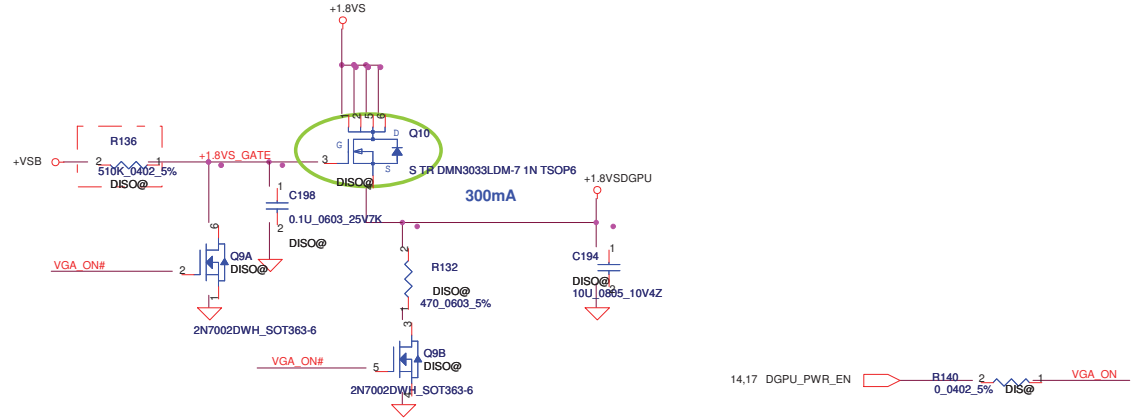


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Customer			Document Number	Rev
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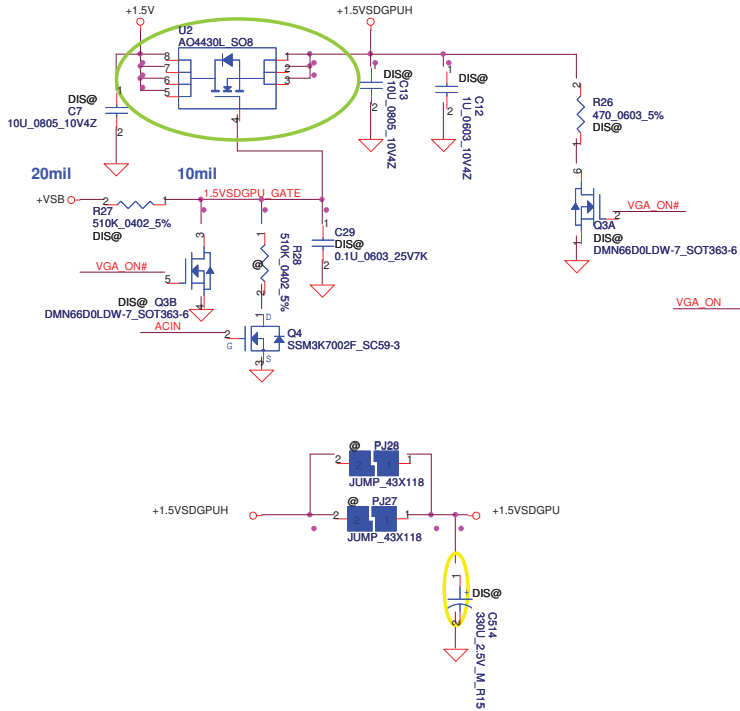
+1.05VS_VTT to +1.05VSDGPU for GPU



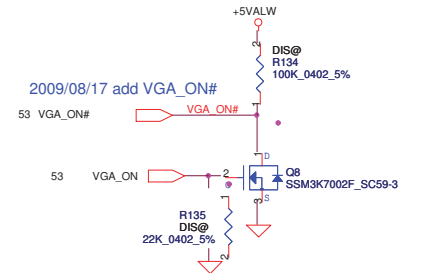
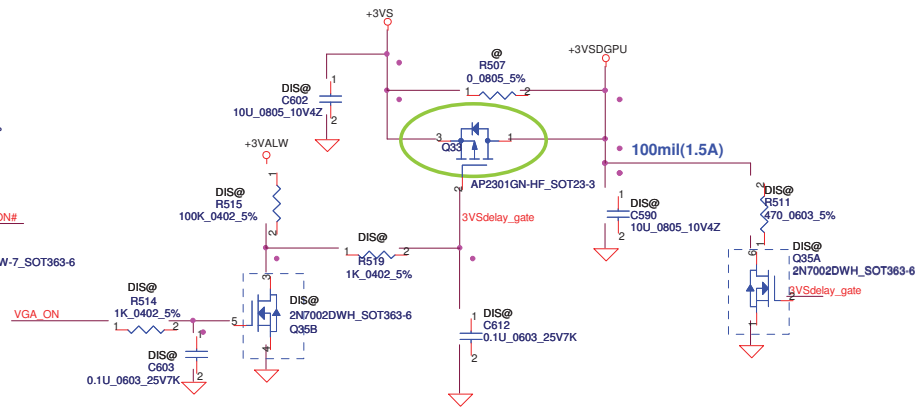
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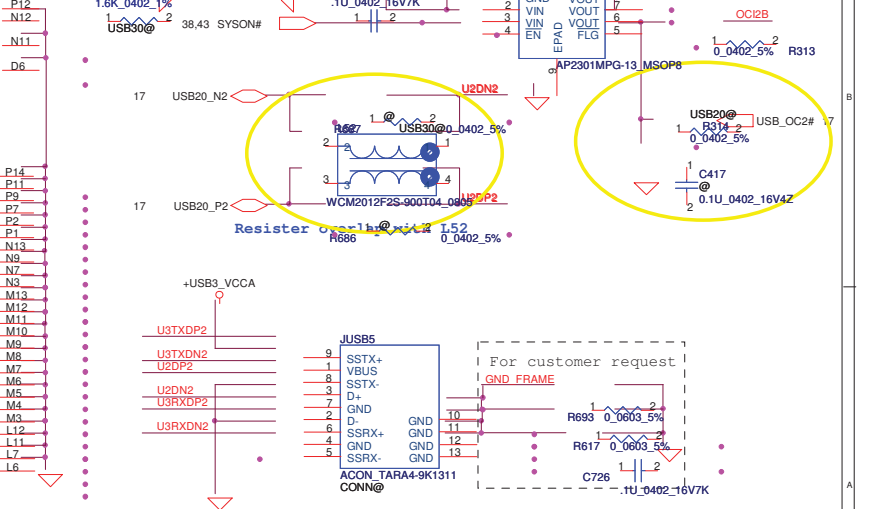
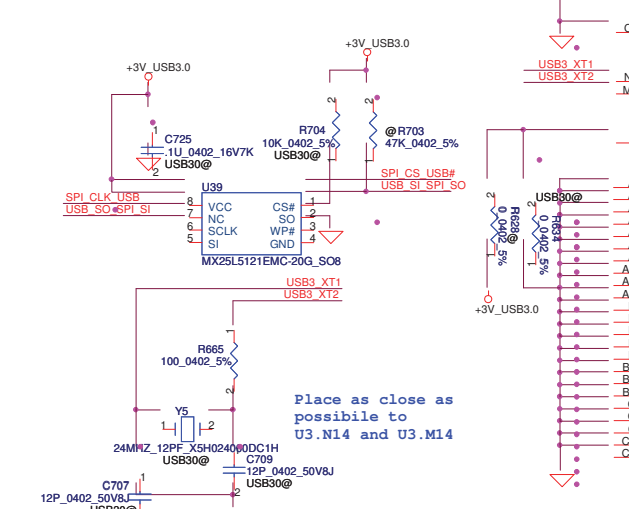
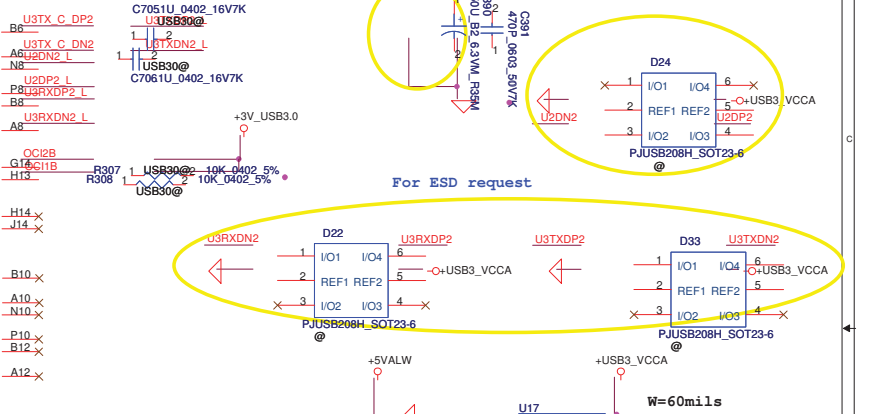
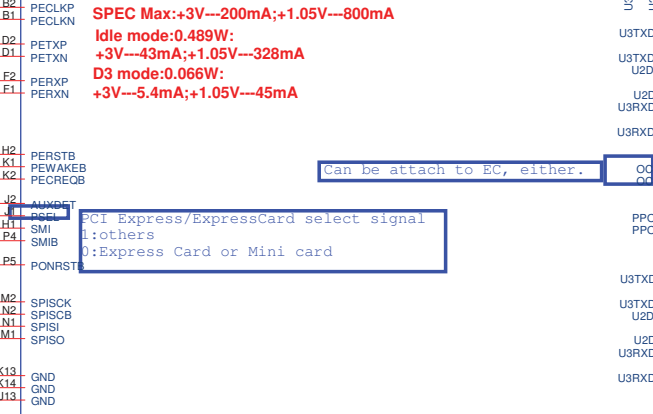
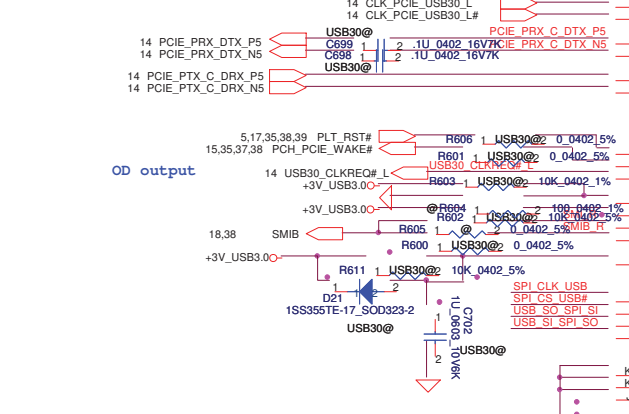
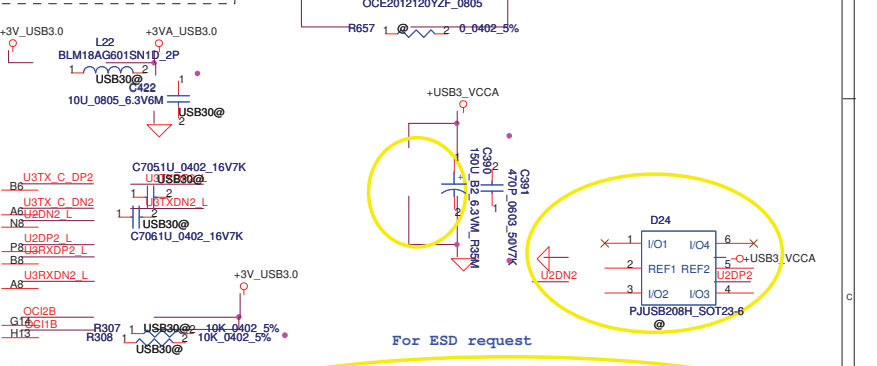
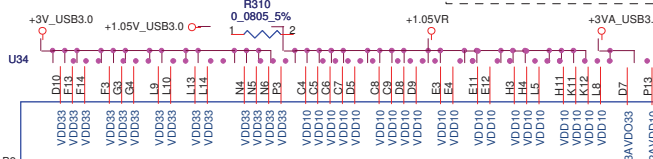
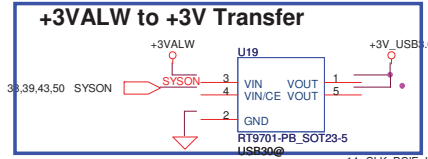
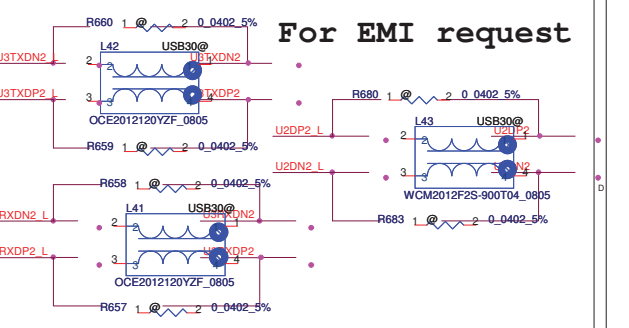
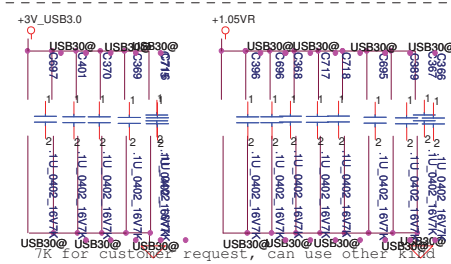
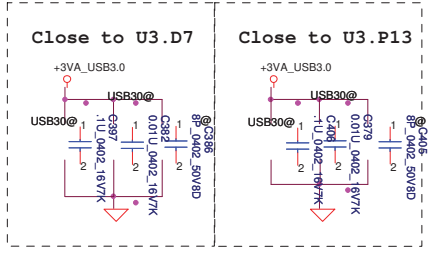
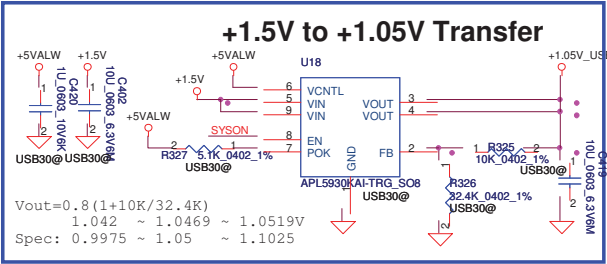
+1.5V to +1.5VSDGPUH for GPU



+3VS to +3VSDGPU for GPU



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Customer			Document Number	Rev
P5WE0 M/B LA-6901P Schematic			0.1	
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Pin compare table for support USB remote wakeup or not

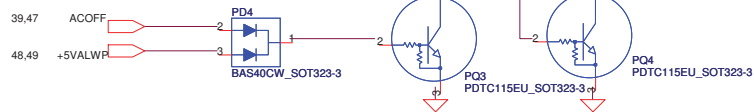
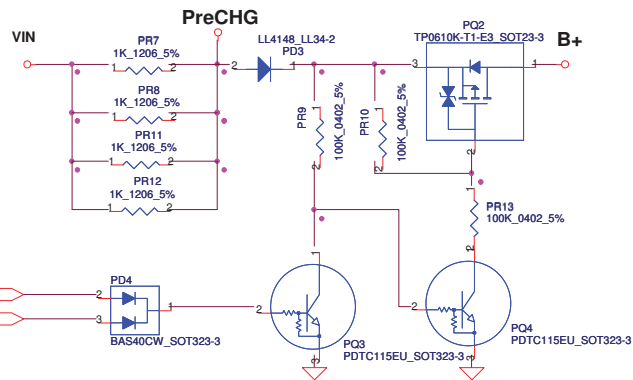
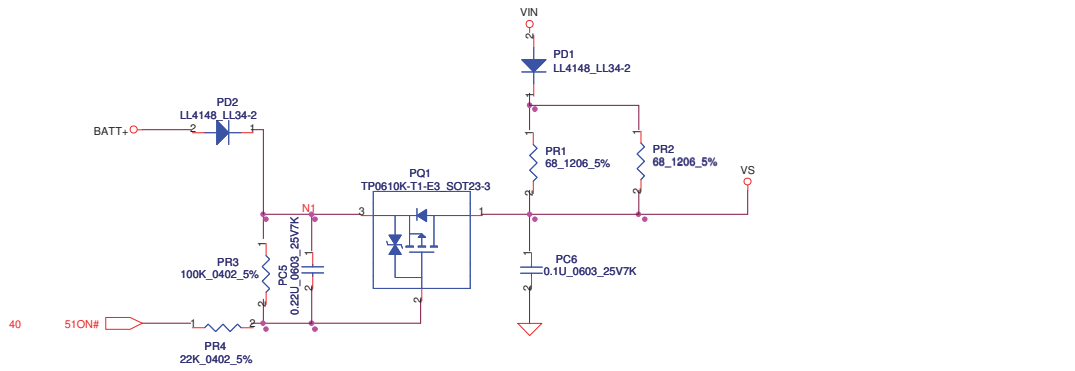
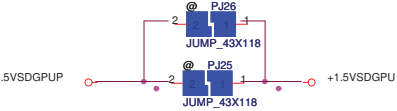
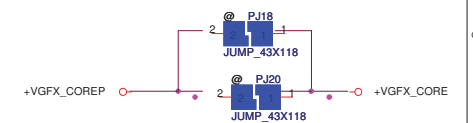
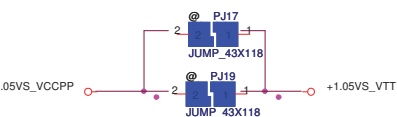
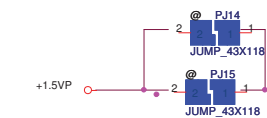
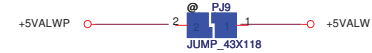
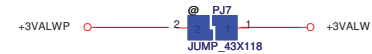
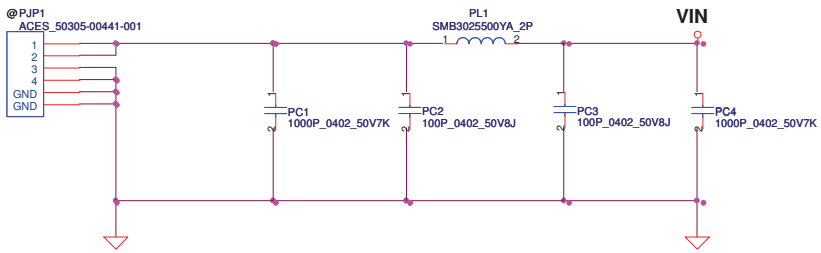
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

UPD72020AF1-DAP-A_FPGA176-USB30@

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Title	USB3.0 PD720200	Rev	0.1
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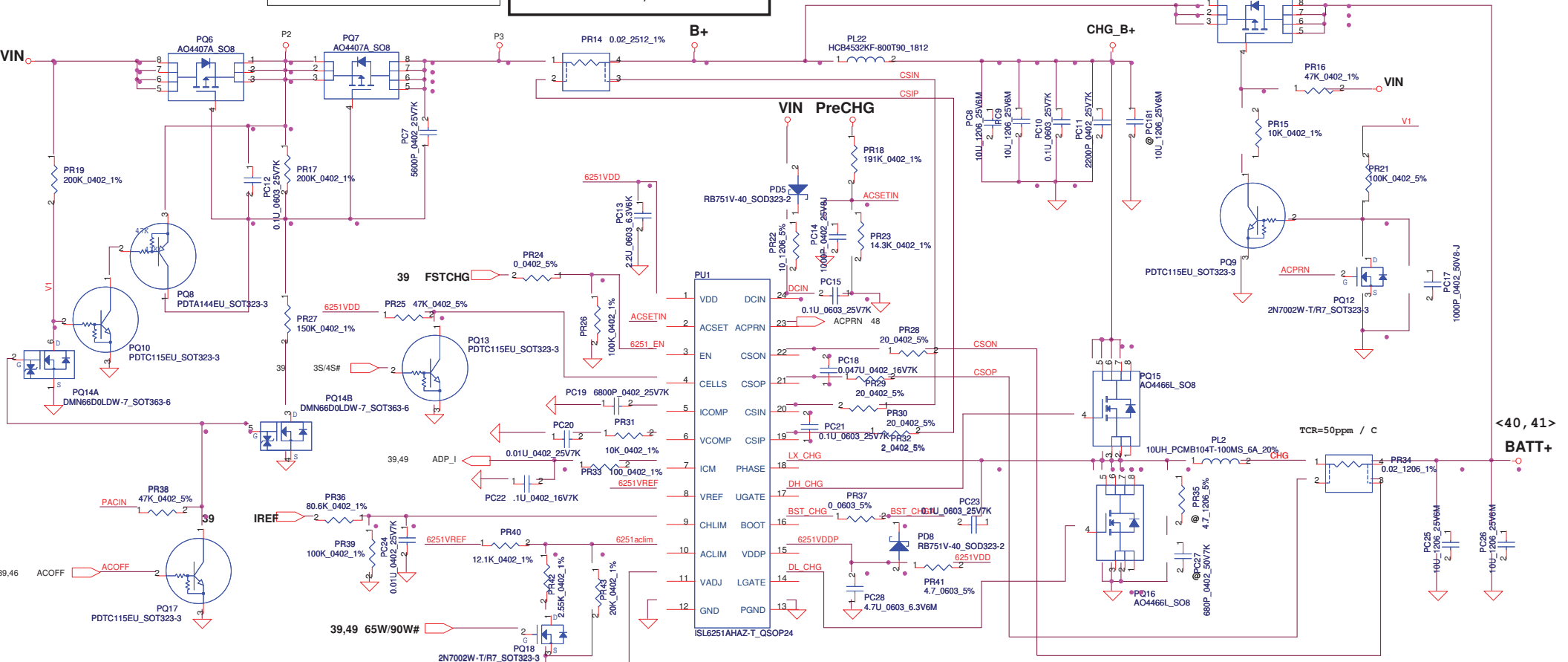
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Iada=0~4.74A (90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A

PC181 reserve for EMI Isen solution



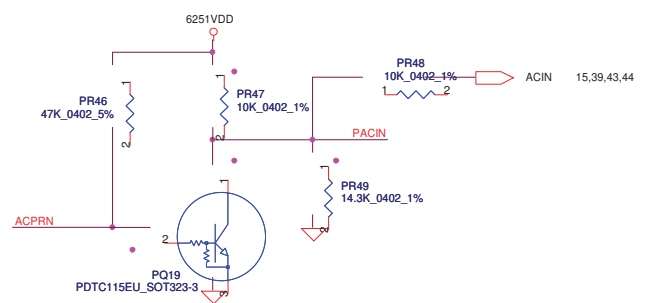
CP mode
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$
 where $V_{aclm} = 1.502V$, $I_{input} = 4.07A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

Ki
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow Ki = 0.7224$

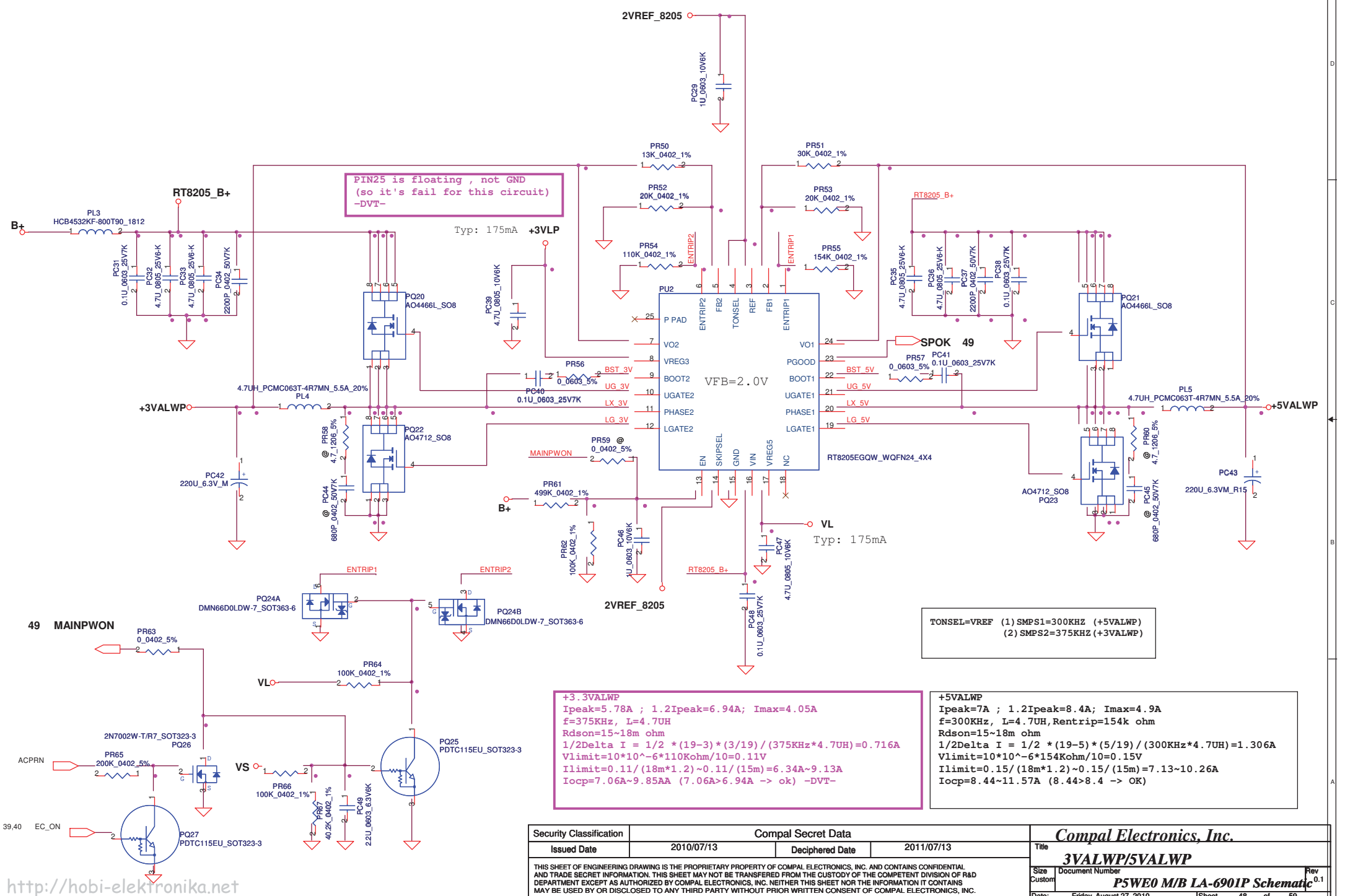
Kv
 $R_{internal} = ic = 514k$ $R_{ec} = 3k$ $R_1 = PR379 = 15.4k$ $R_2 = PR381 = 31.6k$
 $R = 514k // 31.6k // (15.4k + 3k) = 11.372k$
 $r = 514k // 514k // 31.6k = 28.14k$
 $V_{cell} = 0.175 * V_{adj} + 3.99v$
 $4.2V = 0.175 * V_{adj} + 3.99v \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514k)) + CALIBRATE * (r / (r + 514k))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$
 $A = V_{ref} * (R / (R + 514k)) = 0.052$
 $Kv = 9.451$



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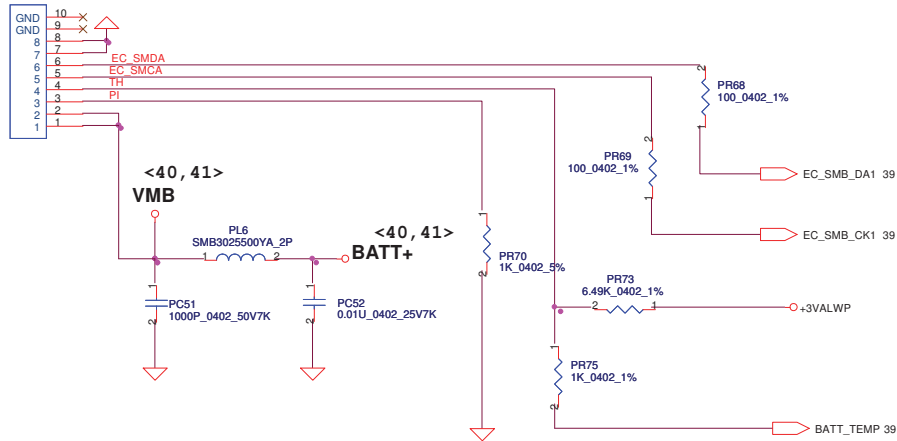
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Compal Electronics, Inc.			
PWR-CHARGER			
Size	Document Number	Rev	
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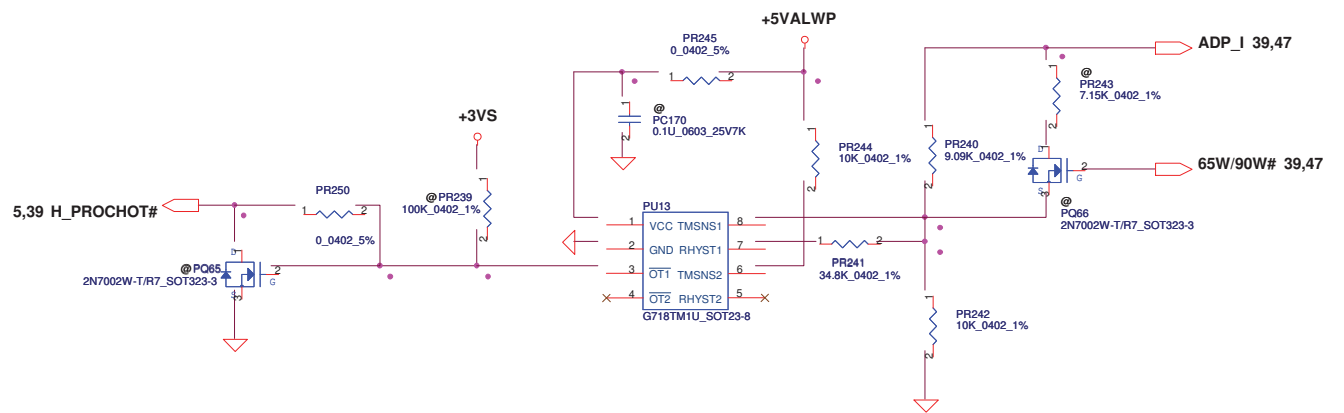
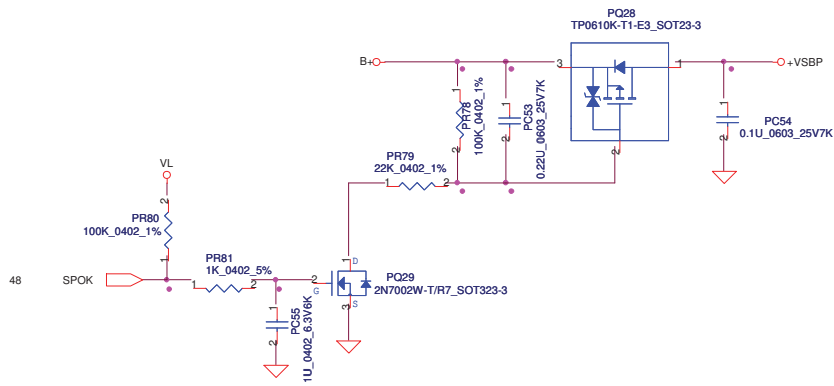
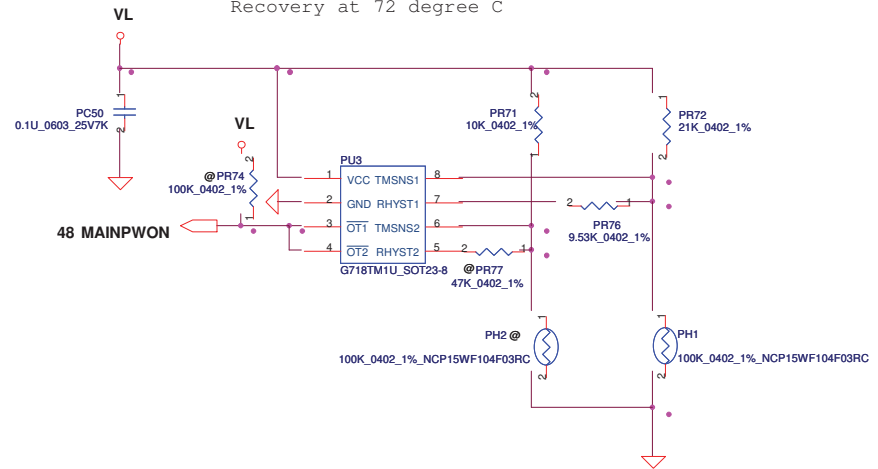


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				Custom	P5WE0 M/B LA-6901P Schematic
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PJP2
SUYIN_200275GR008G13GZR

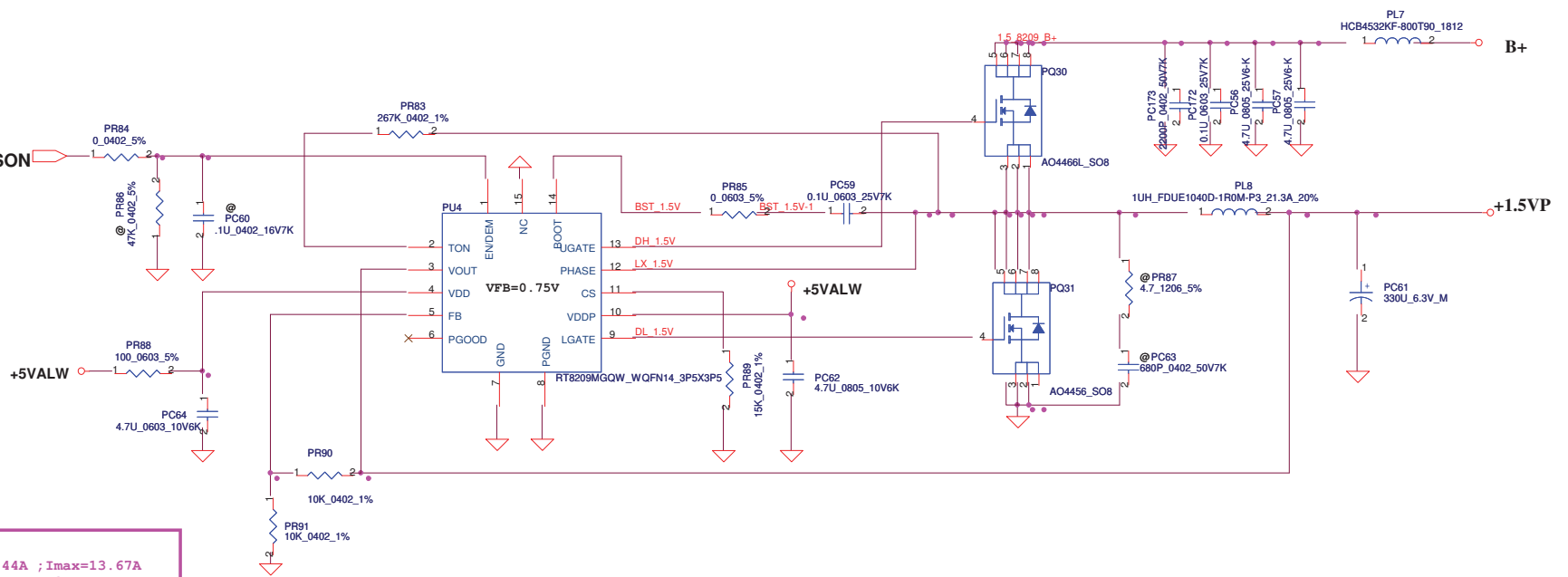


PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C

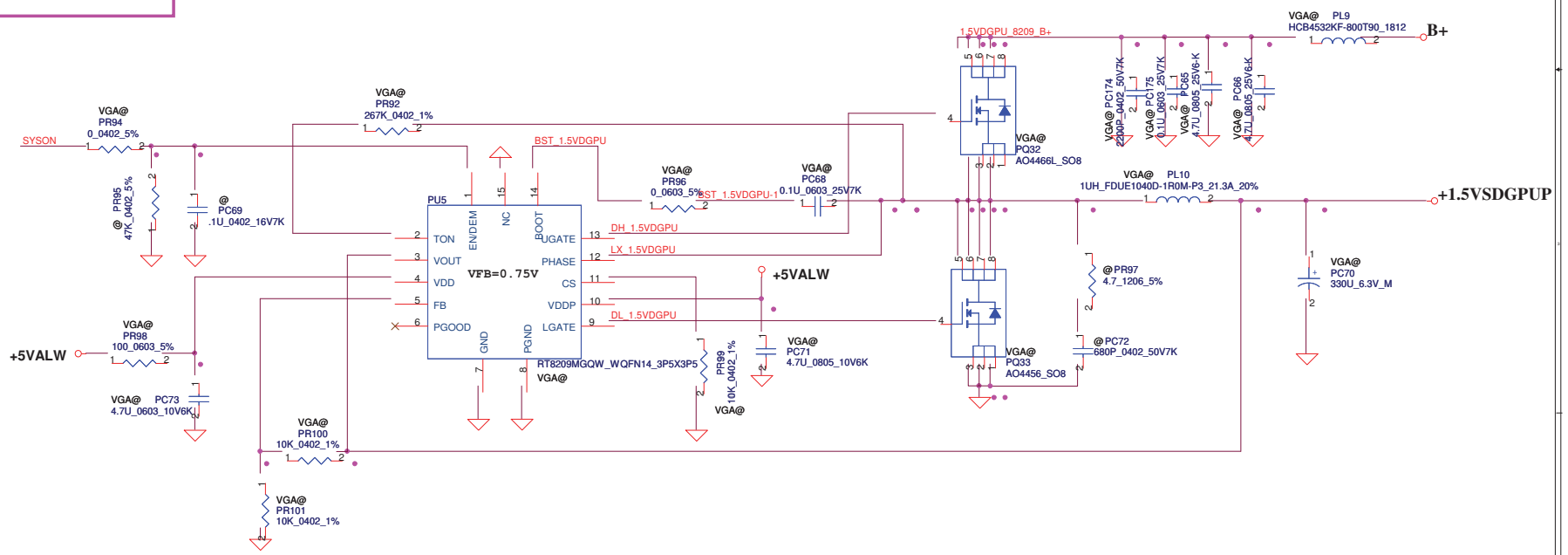


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38,39,43,45 SYSON



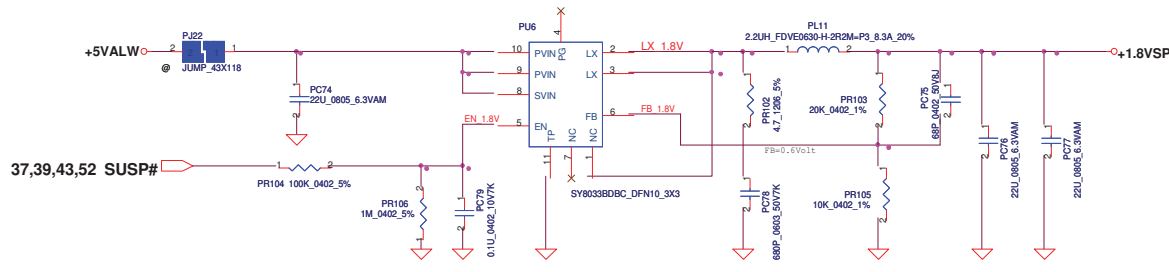
+1.5VP
 Ipeak=19.53A; 1.2Ipeak=23.44A ; Imax=13.67A
 Rton=267K, Fsw=298KHz , Rdson=5.3~7mohm
 Rtrip=12K
 Iocp=18.17~28.98A



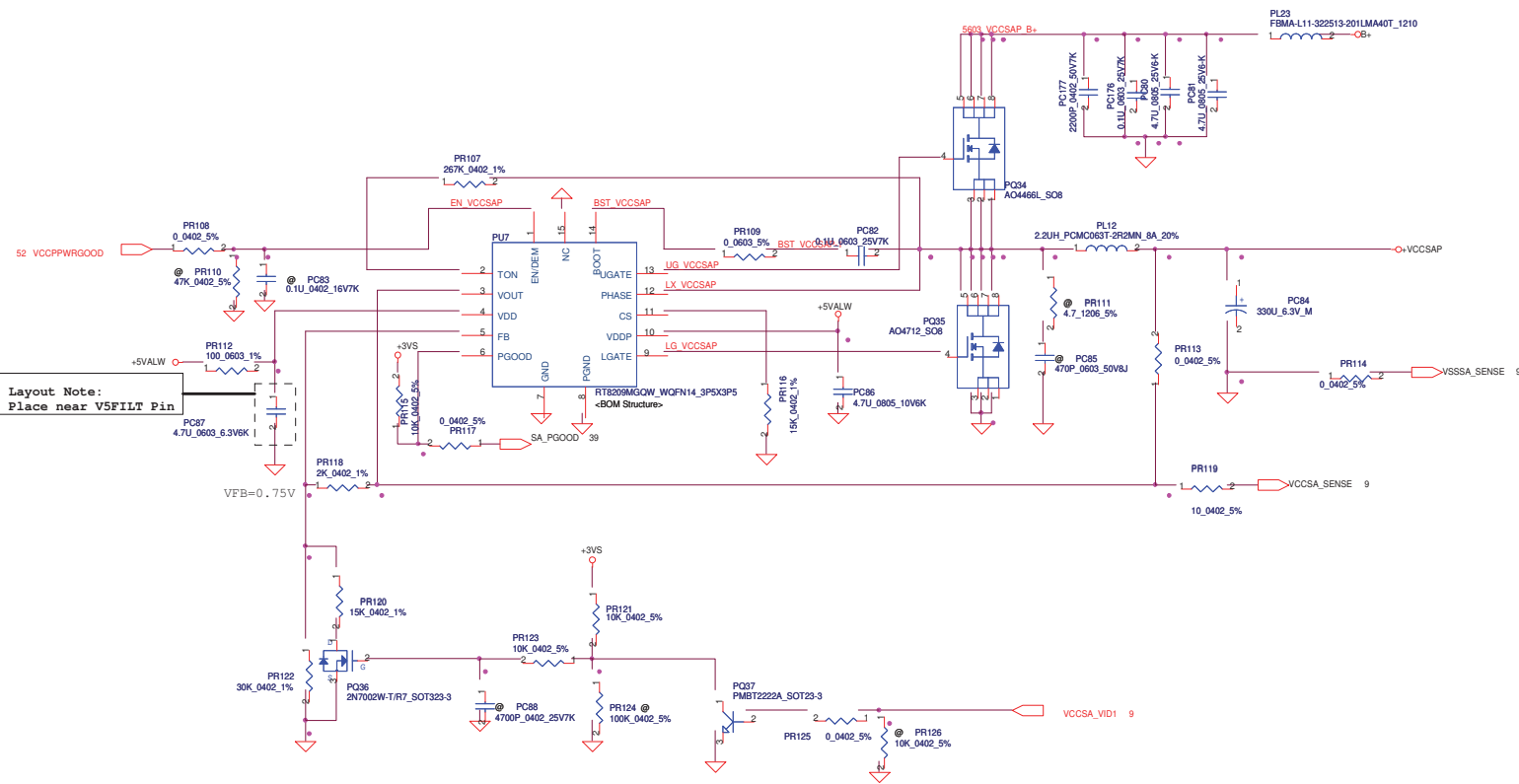
+1.5VSDGPU
 Ipeak=10.4A; 1.2Ipeak=12.48A ; Imax=7.28A
 Rton=267K, Fsw=298KHz , Rdson=4.5~5.6mohm
 Rtrip=10K
 Iocp=14.68~26.29A

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Compal Electronics, Inc.		
Title PWR-+1.5VP/+1.5VSDGPU		
Size Custom	Document Number PSWE0 M/B LA-6901P Schematic	Rev 0.1
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1.8VSP
 Ipeak=3.35A ; 1.2Ipeak=4.02 ; Imax=2.345A
 Vout=0.6*(1+(20K/10K))=1.8V
 -DVT-



Layout Note:
 Place near VSFILT Pin

VFB=0.75V
 $V_o = VFB * (1 + PR156 / PR150) = 1.1V$
 $Ton = 19E-12 * Ron * ((2/3) * Vo + 150mV) / Vin + 50ns = 2.4E-7$
 Freq=282KHz

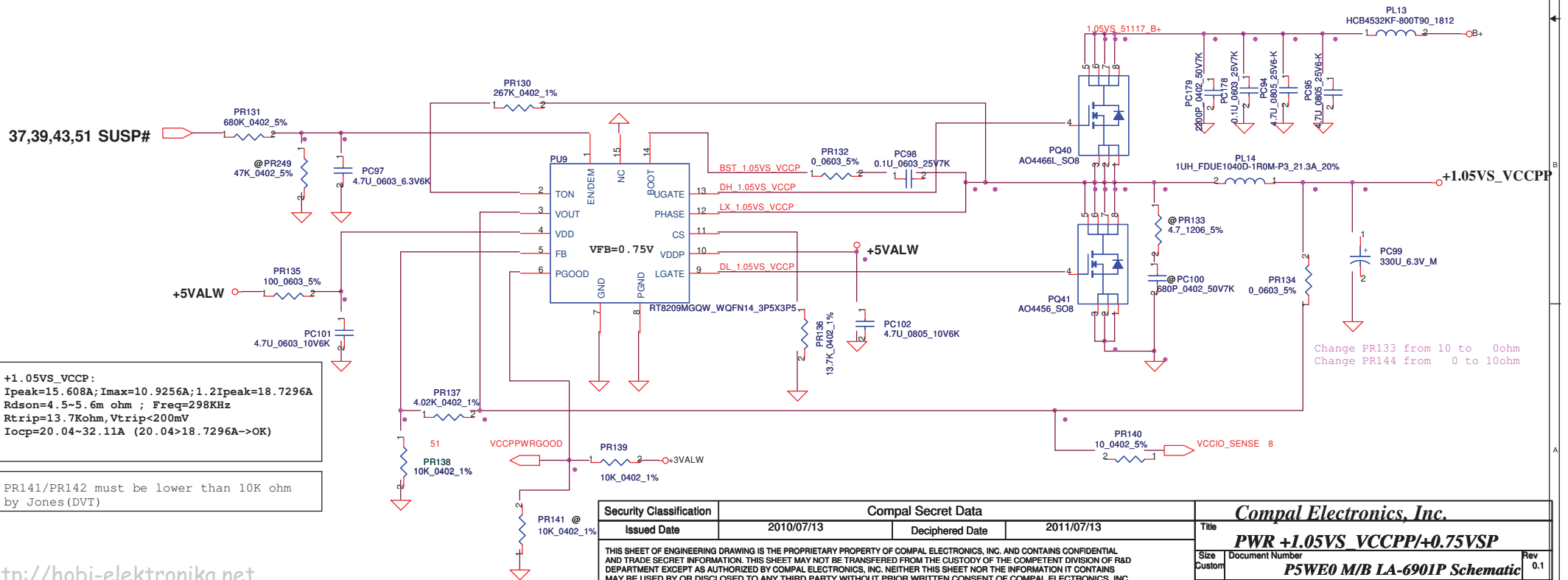
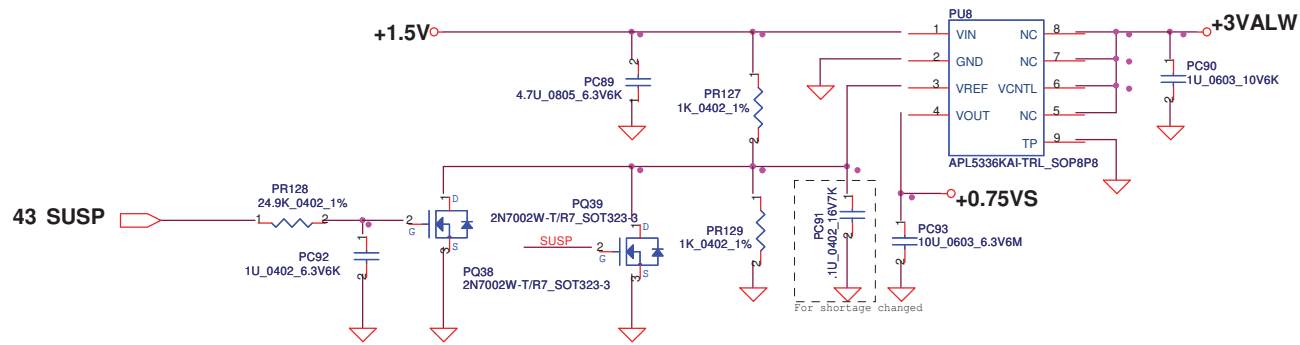
Cesr=15m ohm
 Ipeak=4.60A Imax=2.70A
 $\Delta I = ((19.5 - 1.0) * (1.0 / 19.5)) / (L * Freq) = 1.48A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.0787V$
 Iocp-min=5.96A
 Iocp-max=6.01A
 Iocp=5.96-6.01A

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	Yes/Yes
0	1	0.8 V	Yes/Yes	Yes/Yes
1	1	0.75V	No/Yes	No/Yes
1	1	0.65V	No/Yes	No/Yes

Note: Use VCCSA_SEL to switch High & Low Level for VID[1]
 (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

+VCCSAP
 Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A
 DCR= 9 m(typ)~10 m(max)
 Rlimit=12K, Rds(on)=15-18mohm
 Ilimit=10uA
 $I_{ocp} = R_{limit} / R_{ds(on)} * 10^{-5} = 7.59-10.654A$

the resistor change
 from @ to pop component
 Add two jumpers on the HW's output cap of the
 +VCCSA's PFM(+) and PFM(-) to sense the
 feedback voltage for VCCSA_SENSE & VSSA_SENSE.

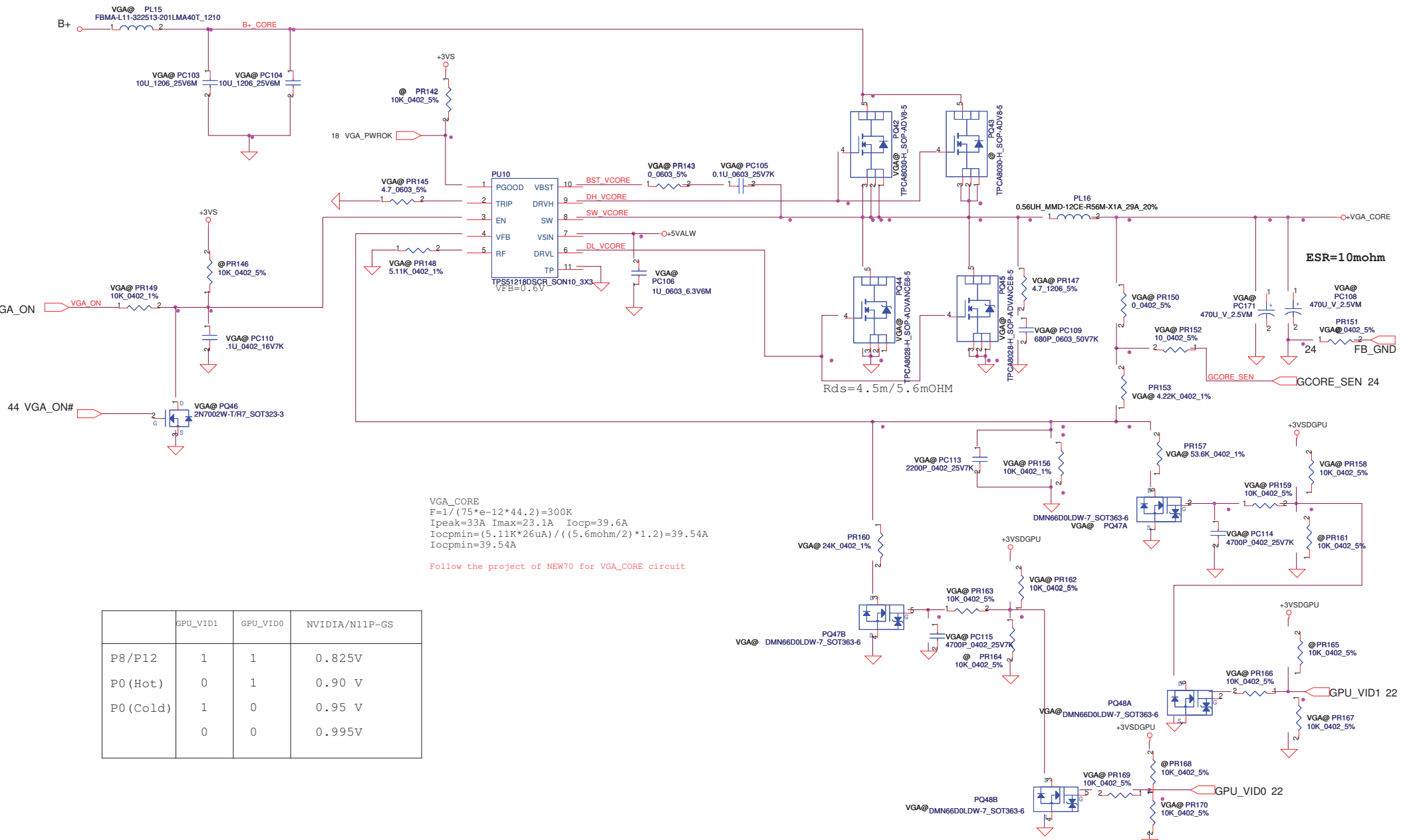


+1.05VS_VCCP:
 Ipeak=15.608A; Imax=10.9256A; 1.2Ipeak=18.7296A
 Rdsn=4.5~5.6m ohm ; Freq=298KHz
 Rtrip=13.7Kohm, Vtrip<200mV
 Iocp=20.04~32.11A (20.04>18.7296A->OK)

PR141/PR142 must be lower than 10K ohm
 by Jones (DVT)

Change PR133 from 10 to 0ohm
 Change PR144 from 0 to 10ohm

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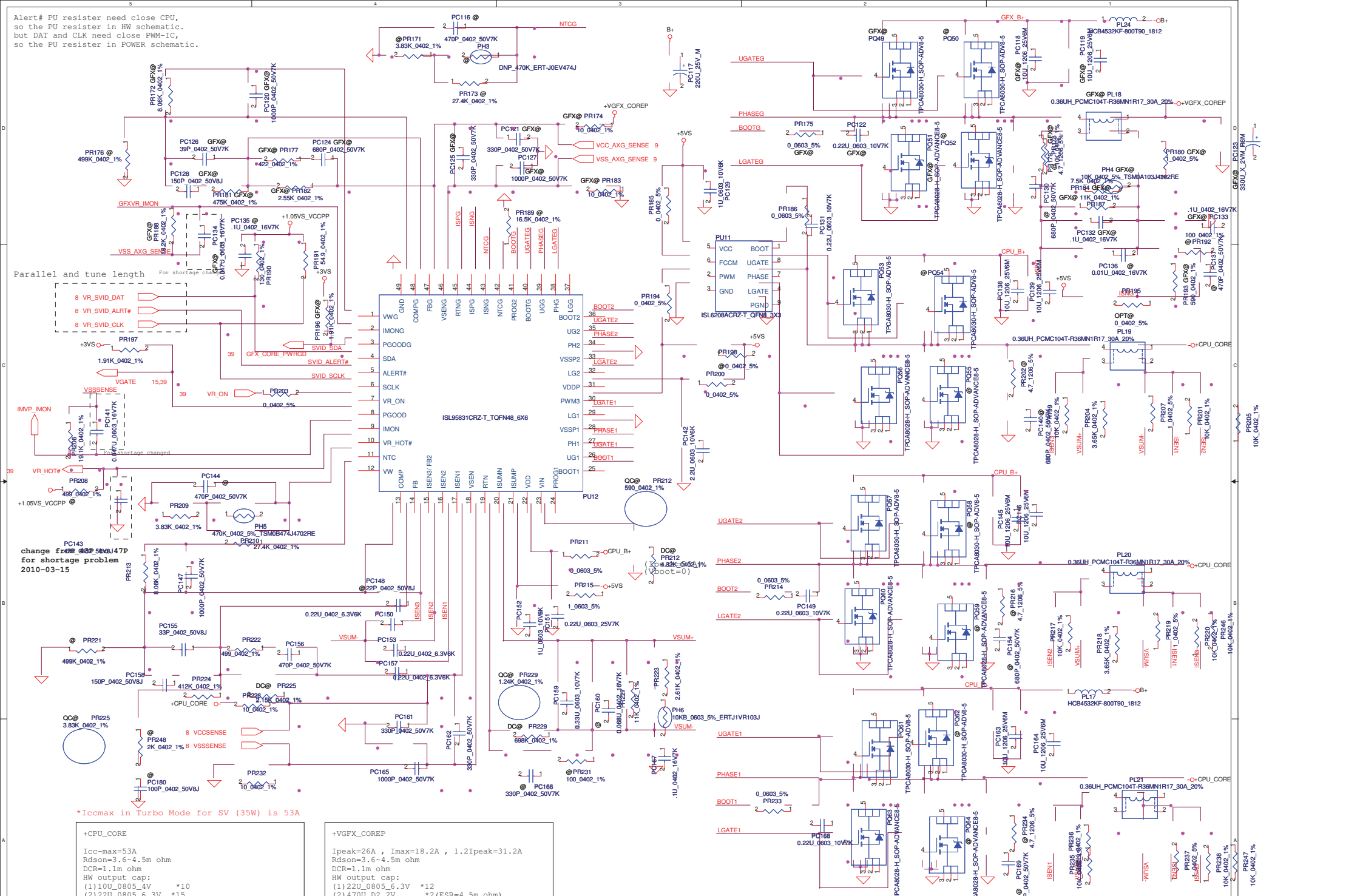
VGA_CORE
 $F=1/(75 \times e^{-12 \times 44.2})=300K$
 $I_{peak}=33A$ $I_{max}=23.1A$ $I_{ocp}=39.6A$
 $I_{ocpmin}=(5.11K \times 26\mu A) / ((5.6m\Omega / 2) \times 1.2)=39.54A$
 $I_{ocpmin}=39.54A$

Follow the project of NEW70 for VGA_CORE circuit

	GPU_VID1	GPU_VID0	NVIDIA/N11P-GS
P8/P12	1	1	0.825V
P0 (Hot)	0	1	0.90 V
P0 (Cold)	1	0	0.95 V
	0	0	0.995V

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Alert# PU resistor need close CPU, so the PU resistor in HW schematic. but DAT and CLK need close PWM-IC, so the PU resistor in POWER schematic.



Parallel and tune length For shortage change

change for shortage problem 2010-03-15

*Iccmax in Turbo Mode for SV (35V) is 53A

+CPU_CORE	
Icc-max=53A	
Rdson=3.6~4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 10U_0805_4V *10	
(2) 22U_0805_6.3V *15	
(3) 470U_D2_2V *4 (ESR=4.5m ohm)	

+VGFX_COREP	
Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A	
Rdson=3.6~4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 22U_0805_6.3V *12	
(2) 470U_D2_2V *2 (ESR=4.5m ohm)	

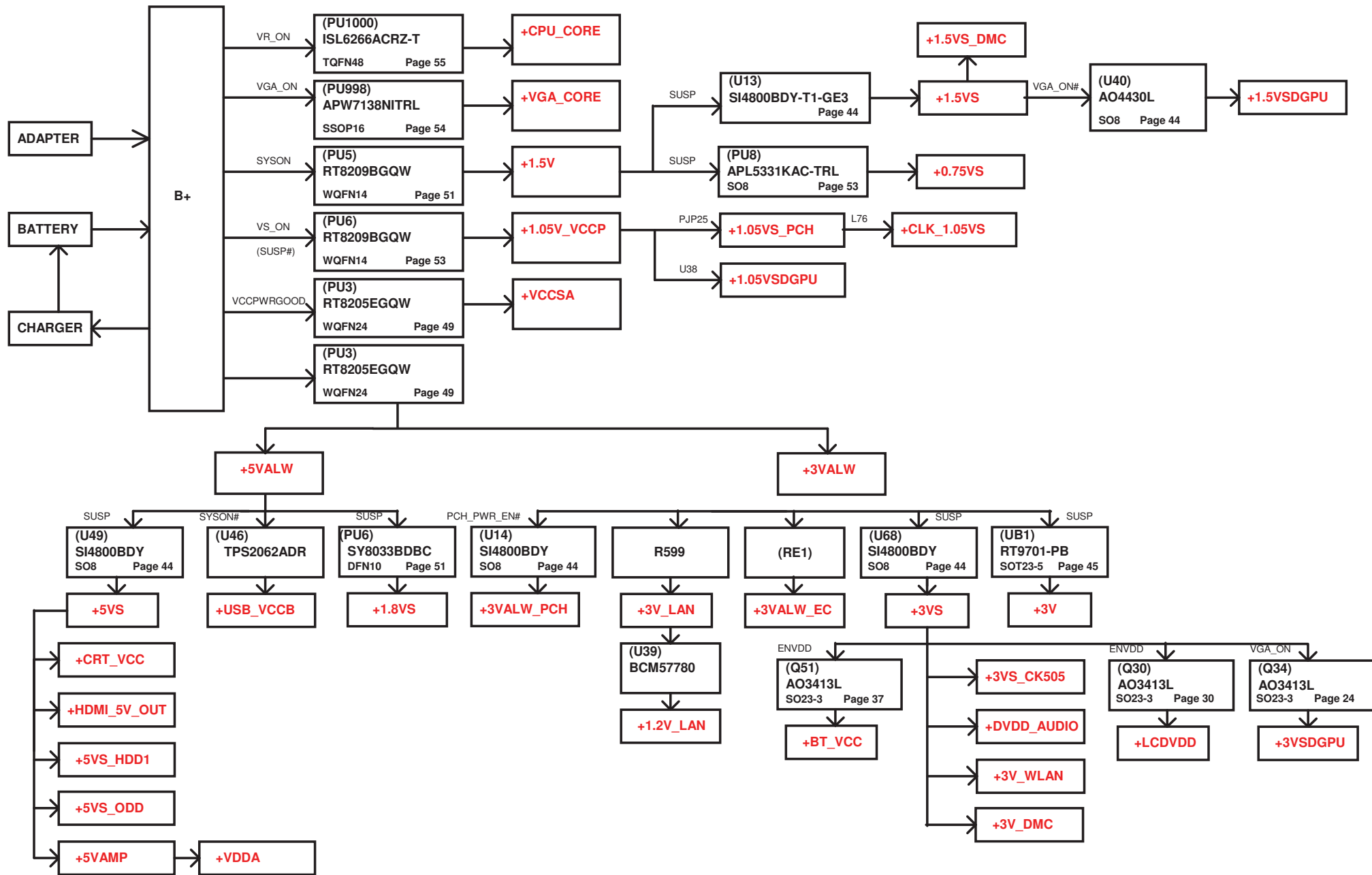
*OCP setting value=37A

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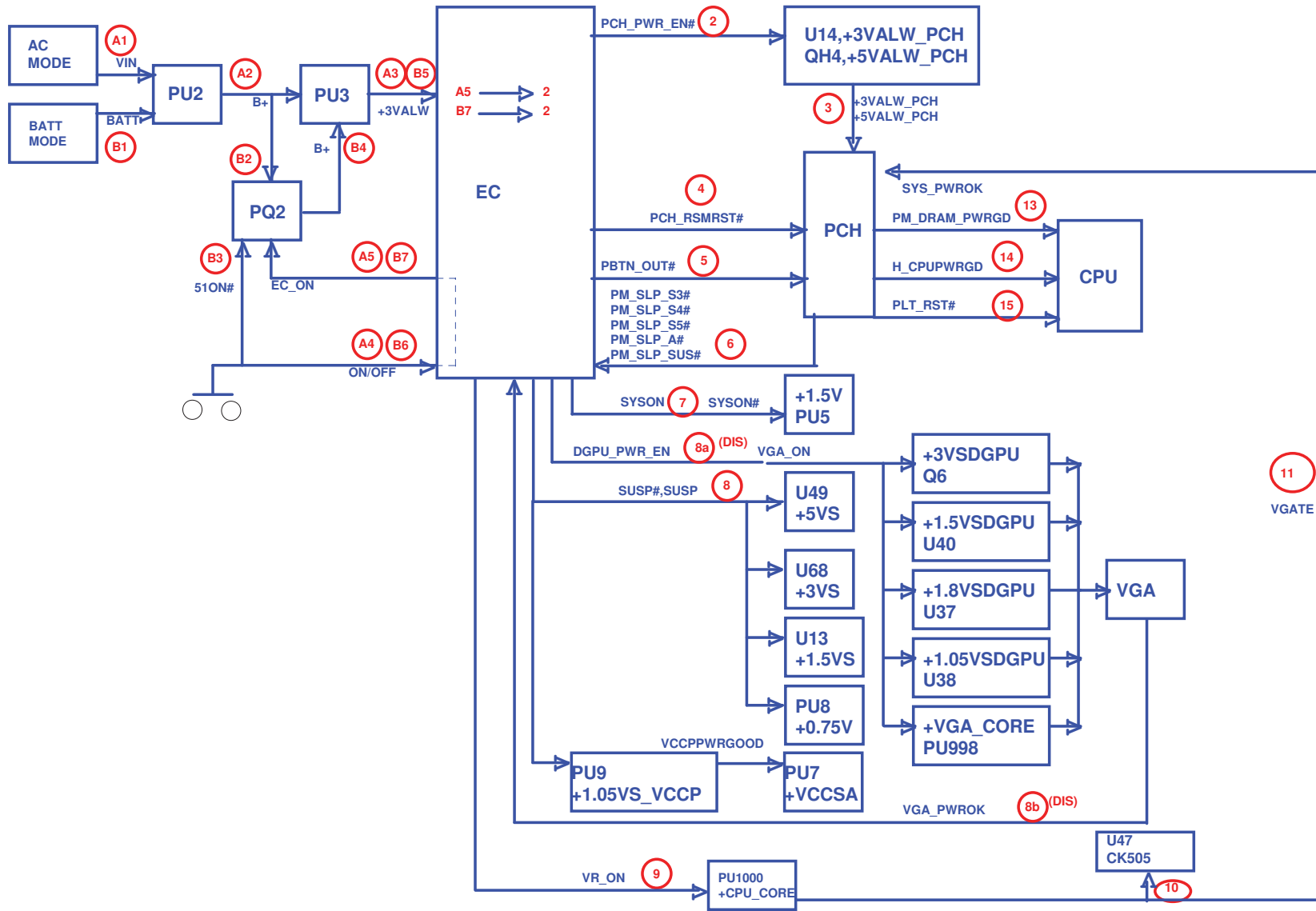
Compal Electronics, Inc.	
Title	PWR +CPU CORE/+VGFX CORE
Size	Document Number
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Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
1	Shut down for PWM3 pin floating	IF the PWM3 no used, please pull high it for +5VS and not floating	0.1	P.55	(1)Add PR638(0_0603_5%) between PWM3 and +5VS (2)connect the ISNG to +5VS	2010-03-29	DVT
2	OVP problem with PWR and HW side	If the HW side is 0V, through the jumper will cause the sense pin to over the votage setting and it may happen OVP problem.	0.1	P.55	Change the +VGFX_CORE to +VGFX_COREP	2010-03-29	DVT
3							

COMPAL ELECTRONICS		
Title		<Title> PIR POWER1
Size	Document Number	Rev
A	PAW00 (LA-6361P)	0.1
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Size	Document Number	Rev		
Custom	PSWEO M/B LA-6901P Schematic	0.1		
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